TEXAS INSTRUMENTS

Interface Circuits

Data Transmission and Control Circuits, Peripheral Drivers/Power Actuators, Display Drivers

Data Book

Data Book

Interface Circuits
Data Transmission and Control Circuits,
Peripheral Drivers/Power Actuators, Display Drivers

1991

1991

Linear Products

Linear Products Quick Reference Guide

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• Linear Circuits Vol 2 Data Acquisition and Conversion	A/D and D/A Converters DSP Analog Interface Analog Switches and Multiplexers Switched-Capacitor Filters	SLYD004, 1989
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INTRODUCTION

In the 1990 *Interface Circuits Data Book*, the Linear Products Division of Texas Instruments presents technical information on various products for electronic media and electronic devices.

TI's Interface circuits represent technologies from classic bipolar through BIDFET, Advanced Low-Power Schottky (ALS), IMPACT™, LinBiCMOS™, and Advanced LinCMOS™ processes. The ALS and IMPACT™ oxide-isolated technologies provide the Interface family with improved speed-power characteristics. LinBiCMOS™ and Advanced LinCMOS™ technologies feature a step-function improvement in impedance, speed, power dissipation, and threshold stability.

This data book provides information on the following types of products:

- Data-Transmission Circuits
- High-Current Actuators and Peripheral Drivers
- High-Voltage Display Drivers
- Asynchronous Communication Elements
- Intelligent-Power Devices

The data-transmission line drivers, receivers, and transceivers, which support many popular data transmission standards, connect electronic devices and systems at high data rates over significant cable lengths. The high-current actuators and peripheral drivers combine both logic control and high-current drive capability in a single package. For flat-panel, AC-plasma, vacuum fluorescent, and electroluminescent display applications, the high-voltage display drivers provide cost-effective and reliable service.

Among TI's new products in the 1990 *Interface Data Book* are Asynchronous Communication Elements (ACEs) and Intelligent-Power devices. The ACEs provide complete universal interface capabilities between electronic systems, which minimize device components and power dissipation while increasing data rates. The Intelligent-Power devices are useful for applications that require high energy loads and load protection circuits operating in harsh electrical environments.

These Interface products range from the classic line driver to the Asynchronous Communication Element. New surface-mounted packages (8 to 68 leads) include both ceramic and plastic chip carriers, and the small-outline (D) plastic packages that optimize board density with minimum impact on power dissipation capability.

The alphanumeric index provides a quick method of locating the correct device type, with new products as indicated. The selection guide includes a functional description of each product with information on key parameters and packaging types. A cross-reference table listing other manufacturers with the TI direct or nearest replacement devices is also available. Ordering information and mechanical data are in the last section of this data book.

While this volume offers design and specification data only for Interface components, complete technical data for any TI semiconductor product is available from your nearest TI Field Sales Office, local authorized TI distributor, or by writing directly to:

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We sincerely feel that you will discover the new 1990 *Interface Circuits Data Book* to be a significant addition to your collection of technical literature.

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† *New devices added to this volume*

ALPHANUMERIC INDEX

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line drivers

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†ACE—Asynchronous Communications Element
‡FIFO—First In First Out

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electroluminescent display drivers

DESC.	PRODUCT FEATURES	DRIVERS PER PKG	INPUT COMPATIBILITY	POWER SUPPLY	TYPE	PKG
ROW DRIVERS	• 225-V open-drain DMOS outputs • Serial-in, parallel-out architecture • 50-mA current sink output capability • Extremely low steady-state power consumption • Left side (SNXX551) and right side (SNXX552) drivers enhance circuit layout	32	CMOS	V_{CC1} (logic) = 10.8 V to 15 V	SN55551 SN55552	FD
					SN65551 SN65552 SN75551 SN75552	FN, N
	• Monolithic BIDFET integrated circuits • Very low steady-state power consumption • 300-mA output capability • High-voltage open-collector N-P-N outputs				SN65557 SN65558 SN75557 SN75558	FN
	• 225-V totem-pole BIDFET output structures • 70-mA output source/sink capability • Very low steady-state power consumption • 3-state capabilities • Selectable open-source or open-drain output	34			SN55563A SN55564A	FJ
					SN65563A SN65564A SN75563A SN75564A	FN
COLUMN DRIVERS	• 60-V totem-pole BIDFET output structures • Serial-in, parallel-out architecture • 15-mA sink or source output capability • Top (SNXX553) and bottom (SNXX5554) drivers enhance circuit layout	32	CMOS	V_{CC1} (logic) = 10.8 V to 15 V	SN55553 SN55554	FD
					SN65553 SN65554 SN75553 SN75554	FN, N
	• 90-V output voltage swing capability • 15-mA output source and sink current capability • High-speed serially-shifted data input • Totem-pole outputs • Latches on all driver outputs				SN65555 SN65556 SN75555 SN75556	FN, N

TEXAS INSTRUMENTS
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vacuum fluorescent display drivers

DESC.	PRODUCT FEATURES	DRIVERS PER PKG	INPUT COMPATIBILITY	POWER SUPPLY	TYPE	PKG
ANODE, GRID DRIVERS FOR SEGMENT OR DOT MATRIX FORMATS	• Serial-in, parallel-out architecture • 60-V totem-pole outputs • 25-mA current source output capability • On-board latches	12	TTL	V_{CC1} (logic) = 5 V to 15 V, V_{CC2} (display) = 0 to 60 V	SN65512B SN75512B	DW,N
	All features same as SN65512B except: • 32 bits for large format displays	32	CMOS, TTL	V_{CC1} (logic) = 5 V to 15 V, V_{CC2} (display) = 0 to 130 V	SN65518 SN75518	FN,N
	• Serial-in, parallel-out architecture • 60-V totem-pole outputs • 40-mA current source output • Improved direct replacement for UCN4810A and TL4810A	10	CMOS	V_{CC1} (logic) = 5 V to 15 V, V_{CC2} (display) = 0 to 60 V	TL4810B TL4810BI	DW,N
	• 70-V output voltage swing capability • Drives up to 20 lines • Direct replacement for Sprague UCN5812	20			TL5812 TL5812I	FN,N

dc plasma and gas discharge display drivers

DESC.	PRODUCT FEATURES	DRIVERS PER PKG	INPUT COMPATIBILITY	POWER SUPPLY	TYPE	PKG
SCAN LINE DRIVERS	• 180-V open drain parallel outputs • 220-mA parallel output sink current • Left side (SN751506) and right side (SN751516) drivers enhance circuit layout	32	CMOS	V_{CC} (logic) = 4 V to 6 V	SN751506 SN751516	FT
DATA LINE DRIVERS	• −120-V open collector P-N-P parallel outputs • Two parallel high-speed 16-bit shift registers • Latches on all driver outputs • Top (SN751508) and bottom (SN751518) drivers enhance circuit layout			V_{CC} (logic) = 4.5 V to 5.5 V	SN751508 SN751518	FT

ac plasma display drivers

DESC.	PRODUCT FEATURES	DRIVERS PER PKG	INPUT COMPATIBILITY	POWER SUPPLY	TYPE	PKG
AXIS DRIVERS	• High-speed serial-in, parallel-out architecture (8 MHz) • Fast output transitions (150 ns typ) • 15-mA output current capability • X-axis driver (SNXX500) • Y-axis driver (SNXX501) • Military temperature packages available (SN55500, SN55501)	32 (8 bits with 1 of 4 selectors)	CMOS	V_{CC1} (logic) = 10.8 V to 13.2 V V_{CC2} (display) = 0 to 100 V	SN55500E	FD, JD
					SN65500E	FN, N
					SN75500E	
		32 32 × 1			SN55501E	FD, JD
					SN65501E	FN, N
					SN75501E	

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Manufacturers are arranged in alphabetical order.

GOULD/AMI	SUGGESTED TI REPLACEMENT	PAGE NO.
S4535	SN75518	3-55

SILICONIX	SUGGESTED TI REPLACEMENT	PAGE NO.
SI9551	SN75551	3-63
SI9552	SN75552	3-63
SI9553	SN75553	3-73
SI9554	SN75554	3-73

SPRAGUE	SUGGESTED TI REPLACEMENT	PAGE NO.
UCN5810A	TL4810B	3-123
UCN5812A	TL5812	3-129
UCN5818A	SN75518	3-55
UCN5851A	SN75551	3-63
UCN5852A	SN75552	3-63
UCN5853A	SN75553	3-73
UCN5854A	SN75554	3-73

SUPERTEX	SUGGESTED TI REPLACEMENT	PAGE NO.
HV51	SN75551	3-63
HV52	SN75552	3-63
HV53	SN75553	3-73
HV54	SN75554	3-73

General-Purpose Drivers and Actuators

SWITCHING VOLTAGE MAX (V)	OFF-STATE VOLTAGE MAX (V)	OUTPUT CURRENT (mA)	DRIVERS PER PACKAGE	OUTPUT CLAMP DIODES	INPUT CAPABILITY	FUNCTION	DELAY TIME TYP (ns)	TYPE	PKG	PAGE
20	30	300	2	NO	TTL	AND	18	SN55451B	FK,JG	4-23
20	30	300	2	NO	TTL	NAND	25	SN55452B	FK,JG	4-23
20	30	300	2	NO	TTL	OR	18	SN55453B	FK,JG	4-23
20	30	300	2	NO	TTL	NOR	26	SN55454B	FK,JG	4-23
20	30	300	2	NO	TTL	AND	18	SN75451B	D,P	4-23
20	30	300	2	NO	TTL	NAND	25	SN75452B	D,P	4-23
20	30	300	2	NO	TTL	OR	18	SN75453B	D,P	4-23
20	30	300	2	NO	TTL	NOR	26	SN75454B	D,P	4-23
24	24	500	2	YES	TTL	MOS DRIVER	35	SN75372	D,P	4-39
24	24	500	4	YES	TTL	MOS DRIVER	35	SN75374	D,N	4-49
30	35	300	2	NO	TTL	AND	28	SN55461	FK,JG	4-31
30	35	300	2	NO	TTL	NAND	38	SN55462	FK,JG	4-31
30	35	300	2	NO	TTL	OR	28	SN55463	FK,JG	4-31
30	35	300	2	NO	TTL	NOR	35	SN55464	FK,JG	4-31
30	35	300	2	NO	TTL	AND	28	SN75461	D,P	4-31
30	35	300	2	NO	TTL	NAND	38	SN75462	D,P	4-31
30	35	300	2	NO	TTL	OR	28	SN75463	D,P	4-31
30	24	1000	8	YES	TTL,CMOS	SERIAL TO PARALLEL POWER CHIP	2000	TPIC2801	KV	4-141
35	70	500	4	YES	TTL,CMOS	INVERT W ENAB	1050	SN75437A	NE	4-65
35	70	600	4	YES	TTL,CMOS	INVERT W ENAB	750	SN75435	NE	4-59
35	70	1000	4	YES	TTL,CMOS	INVERT W ENAB	1050	SN75438	NE	4-65
35	50	1250	4	YES	TTL	INVERT	500	ULN2064	NE	4-163
35	50	1250	4	YES	MOS	INVERT	500	ULN2066	NE	4-163
35	50	1250	4	YES	TTL,CMOS	INVERT	500	ULN2068	NE	4-169
35	50	1250	4	NO	TTL,CMOS	INVERT	500	ULN2074	NE	4-175
45	45	1000	4	YES	TTL,CMOS	AND	2000	TPIC2404	KN	4-123
55	70	350	2	YES	TTL,CMOS	AND	300	SN75446	D,P	4-77
55	70	350	2	YES	TTL,CMOS	NAND	300	SN75447	D,P	4-77
55	70	350	2	YES	TTL,CMOS	OR	300	SN75448	D,P	4-77
55	70	350	2	YES	TTL,CMOS	NOR	300	SN75449	D,P	4-77
50	70	500	4	YES	TTL,CMOS	INVERT W ENAB	1050	SN75436	NE	4-65
50	50	350	7	YES	TTL,CMOS,PMOS	INVERT	250	ULN2001A	D,N	4-155
50	50	350	7	YES	25 V PMOS	INVERT	250	ULN2002A	D,N	4-155
50	50	350	7	YES	TTL,CMOS	INVERT	250	ULN2003A	D,N	4-155
50	50	350	7	YES	15 V MOS	INVERT	250	ULN2004A	D,N	4-155
50	50	350	7	YES	TTL	INVERT	250	ULN2005A	D,N	4-155
50	50	1300	4	YES	TTL,CMOS	INVERT W ENAB	1500	SN75439	NE	4-71
50	80	1500	4	YES	TTL	INVERT	500	ULN2065	NE	4-163
50	80	1500	4	YES	MOS	INVERT	500	ULN2067	NE	4-163
50	80	1500	4	YES	TTL,5 V MOS	INVERT	500	ULN2069	NE	4-169
50	80	1500	4	NO	TTL,5 V MOS	INVERT	500	ULN2075	NE	4-175

General-Purpose Drivers and Actuators (Continued)

SWITCHING VOLTAGE MAX (V)	OFF-STATE VOLTAGE MAX (V)	OUTPUT CURRENT (mA)	DRIVERS PER PACKAGE	OUTPUT CLAMP DIODES	INPUT CAPABILITY	FUNCTION	DELAY TIME TYP (ns)	TYPE	PKG	PAGE
55	70	300	2	NO	TTL	AND	28	SN75471	D,P	4-91
55	70	300	2	NO	TTL	NAND	38	SN75472	D,P	4-91
55	70	300	2	NO	TTL	OR	28	SN75473	D,P	4-91
55	70	300	2	YES	TTL,CMOS	AND	200	SN75476	D,P	4-97
55	70	300	2	YES	TTL,CMOS	NAND	200	SN75477	D,P	4-97
55	70	300	2	YES	TTL,CMOS	OR	200	SN75478	D,P	4-97
55	70	300	2	YES	TTL,CMOS	NOR	200	SN75479	D,P	4-97
60	60	100	4	YES	TTL,CMOS,MOS	TELECOM RY DRV	1000	DS3680I	D,J,N	4-3
60	60	1000	4	YES	TTL,CMOS	INVERT		TPIC2406	KN	4-129
60	100	350	7	YES	TTL	INVERT	250	SN75465	D,N	4-83
60	100	350	7	YES	TTL,CMOS,PMOS	INVERT	250	SN75466	D,N	4-83
60	100	350	7	YES	25 V PMOS	INVERT	250	SN75467	D,N	4-83
60	100	350	7	YES	TTL,CMOS	INVERT	250	SN75468	D,N	4-83
60	100	350	7	YES	15 V MOS	INVERT	250	SN75469	D,N	4-83

Motor Drivers and Power Actuators

SWITCHING VOLTAGE MAX (V)	OFF-STATE VOLTAGE MAX (V)	OUTPUT CURRENT (mA)	DRIVERS PER PACKAGE	OUTPUT CLAMP DIODES	INPUT CAPABILITY	FUNCTION	DELAY TIME TYP (ns)	TYPE	PKG	PAGE
36	36	600	4	YES	TTL	HALF-H DRIVER	600	L293D	NE	4-11
36	36	1000	4	NO	TTL	HALF-H DRIVER	600	L293	NE	4-7
36	36	1000	4	YES	TTL,CMOS	HALF-H DRIVER	600	SN754410	NE	4-103
36	36	1000	4	NO	TTL,CMOS	HALF-H DRIVER	600	SN754411	NE	4-109
46	46	2000	2	NO	TTL	FULL-H DRIVER		L298	KV	4-15
46	46	2000	2	NO	TTL	FULL-H DRIVER		TPIC0298	KV	4-115

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Manufacturers are arranged in alphabetical order.

FAIRCHILD	SUGGESTED TI REPLACEMENT	PAGE NO.
μA75451	SN75451B	4-23
μA75452	SN75452B	4-23
μA75453	SN75453B	4-23
μA75454	SN75454B	4-23
μA75461	SN75461	4-31
μA75462	SN75462	4-31
MC1412	ULN2002A	4-155
MC1413	ULN2003A	4-155
μA3680	DS3680	4-3
μA9665	ULN2001A	4-155
μA9666	ULN2002A	4-155
μA9667	ULN2003A	4-155
μA9668	ULN2004A	4-155
μA75471	SN75471	4-91
μA75472	SN75472	4-91
μA75473	SN75473	4-91

MOTOROLA	SUGGESTED TI REPLACEMENT	PAGE NO.
MC1411	ULN2001A	4-155
MC1412	ULN2002A	4-155
MC1413	ULN2003A	4-155
MC1413T	SN75468	4-83
MC1416	ULN2004A	4-155
MC1471	SN75476	4-97
MC1473	SN75478	4-97
MC1474	SN75479	4-97
SN75451B	SN75451B	4-23
SN75452B	SN75452B	4-23
SN75453B	SN75453B	4-23
SN75454B	SN75454B	4-23
ULN2001	ULN2001A	4-155
ULN2002	ULN2002A	4-155

MOTOROLA	SUGGESTED TI REPLACEMENT	PAGE NO.
ULN2003	ULN2003A	4-155
ULN2004	ULN2004A	4-155
ULN2064	ULN2064	4-163
ULN2065	ULN2065	4-163
ULN2066	ULN2066	4-163
ULN2067	ULN2067	4-163
ULN2068	ULN2068	4-169
ULN2069	ULN2069	4-169
ULN2074	ULN2074	4-175
ULN2075	ULN2075	4-175

NATIONAL	SUGGESTED TI REPLACEMENT	PAGE NO.
DS3611	SN75471	4-91
DS3612	SN75472	4-91
DS3613	SN75473	4-91
DS3658	SN75437A	4-65
DS3668	SN75435	4-59
DS3680	DS3680	4-3
DS75361	SN75372	4-39
DS75365	SN75374	4-49
DS75451	SN75451B	4-23
DS75452	SN75452B	4-23
DS75453	SN75453B	4-23
DS75454	SN75454B	4-23
DS75461	SN75461	4-31
DS75462	SN75462	4-31
DS75463	SN75463	4-31
LM3611	SN75471	4-91
LM3612	SN75472	4-91
LM3613	SN75473	4-91
LM75453	SN75453B	4-23

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RIFA	SUGGESTED TI REPLACEMENT	PAGE NO.
PBD352301	ULN2001A	4-155
PBD352302	ULN2004A	4-155
PBD352303	ULN2003A	4-155
PBD352304	ULN2002A	4-155
PBD352311	SN75466	4-83
PBD352312	SN75469	4-83
PBD352313	SN75468	4-83
PBD352314	SN75467	4-83

SGS-ATES	SUGGESTED TI REPLACEMENT	PAGE NO.
L201	ULN2001A	4-155
L202	ULN2002A	4-155
L203	ULN2003A	4-155
L204	ULN2004A	4-155
L293	L293	4-7
L293	SN754411†	4-109
L293D	L293D	4-11
L293D	SN754410†	4-103
L298	L298	4-15
ULN2001	ULN2001A	4-155
ULN2002	ULN2002A	4-155
ULN2003	ULN2003A	4-155
ULN2004	ULN2004A	4-155
ULN2064	ULN2064	4-163
ULN2065	ULN2065	4-163
ULN2066	ULN2066	4-163
ULN2067	ULN2067	4-163
ULN2068	ULN2068	4-169
ULN2069	ULN2069	4-169
ULN2074	ULN2074	4-175
ULN2075	ULN2075	4-175

SILICON GENERAL	SUGGESTED TI REPLACEMENT	PAGE NO.
SG2001	ULN2001A	4-155
SG2002	ULN2002A	4-155
SG2003	ULN2003A	4-155
SG2004	ULN2004A	4-155
SG2022	SN75467	4-83
SG2023	SN75468	4-83
SG2024	SN75469	4-83
SG75451	SN75451B	4-23
SG75452	SN75452B	4-23
SG75453	SN75453B	4-23
SG75454	SN75454B	4-23
SG75461	SN75461	4-31
SG75462	SN75462	4-31
SG75463	SN75463	4-31
SG75473	SN75473	4-91

SPRAGUE	SUGGESTED TI REPLACEMENT	PAGE NO.
UDN-2541	SN75437A	4-65
UDN-3611	SN75471	4-91
UDN-3612	SN75472	4-91
UDN-3613	SN75473	4-91
UDN-5711	SN75476	4-97
UDN-5713	SN75478	4-97
UDN-5714	SN75479	4-97
UDN-5722	SN75477	4-97
ULN-2001	ULN2001A	4-155
ULN-2002	ULN2002A	4-155
ULN-2003	ULN2003A	4-155
ULN-2004	ULN2004A	4-155
ULN-2005	ULN2005A	4-155
ULN-2021	SN75466	4-83
ULN-2022	SN75467	4-83
ULN-2023	SN75468	4-83
ULN-2024	SN75469	4-83
ULN-2025	SN75465	4-83
ULN-2064	ULN2064	4-163
ULN-2065	ULN2065	4-163
ULN-2066	ULN2066	4-163
ULN-2067	ULN2067	4-163
ULN-2068	ULN2068	4-169
ULN-2069	ULN2069	4-169
ULN-2074	ULN2074	2-175
ULN-2075	ULN2075	2-175

†Consult product data sheet for possible slight product differences.

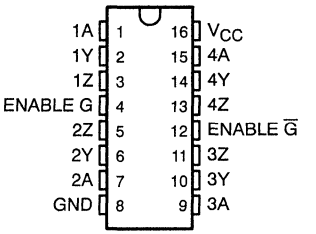
UNITRODE	SUGGESTED TI REPLACEMENT	PAGE NO.
L293	L293	4-7
L293	SN754411†	4-109
L293D	L293D	4-11
L293D	SN754410†	4-103
L298	L298	4-15

†Consult product data sheet for possible slight product differences.

D2433, JANUARY 1979–REVISED MAY 1990

- **Meets EIA Standard RS-422-A**
- **Operates From a Single 5-V Supply**
- **TTL Compatible**
- **Complementary Outputs**
- **High Output Impedance in Power-Off Conditions**
- **Complementary Output Enable Inputs**

D, J, OR N PACKAGE
(TOP VIEW)



description

The AM26LS31C is a quadruple complementary-output line driver designed to meet the requirements of EIA Standard RS-422-A and Federal Standard 1020. The 3-state outputs have high-current capability for driving balanced lines such as twisted-pair or parallel-wire transmission lines, and they provide a high-impedance state in the power-off condition. The enable function is common to all four drivers and offers the choice of an active-high or active-low enable input. Low-power Schottky circuitry reduces power consumption without sacrificing speed.

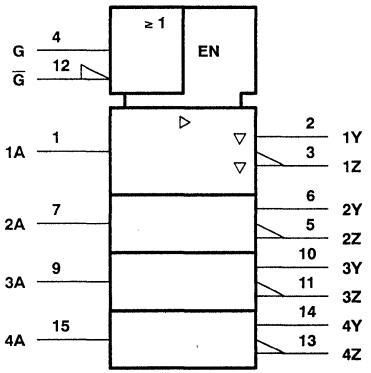
The AM26LS31C is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH DRIVER)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

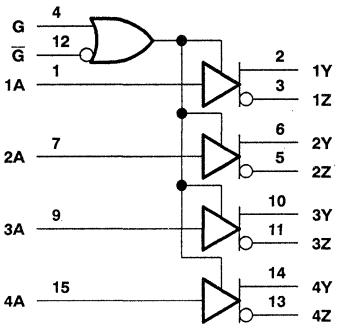
H = high level
L = low level
X = irrelevant
Z = high impedance (off)

logic symbol†

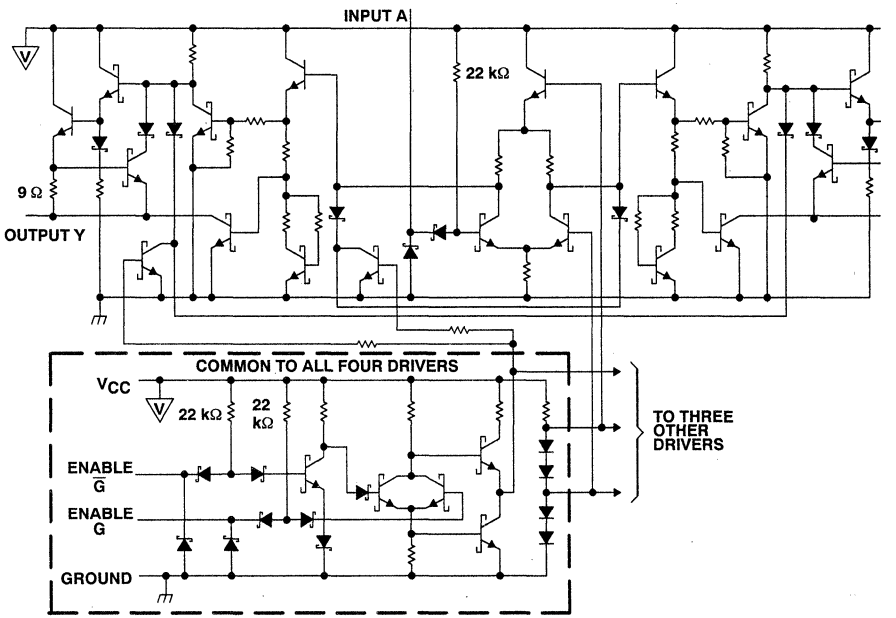


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each driver)



All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage ..... 7 V
Output off-state voltage ..... 5.5 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0 to 70°C
Storage temperature range ..... −65 to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C

NOTE 1: All voltage values, except differential output voltage V_{OD}, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

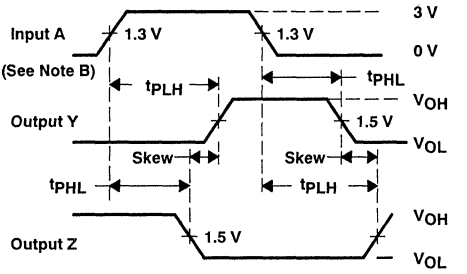
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = – 18 mA			– 1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V,	I_{OH} = – 20 mA	2.5			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V,	I_{OL} = 20 mA			0.5	V
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = 4.75 V	V_O = 0.5 V			– 20	μA
			V_O = 2.5 V			20	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V,	V_I = 7 V			0.1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 2.7 V			20	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.4 V			– 0.36	mA
I_{OS}	Short-circuit output current‡	V_{CC} = 5.25 V		– 30		– 150	mA
I_{CC}	Supply current	V_{CC} = 5.25 V,	All output disabled		32	80	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

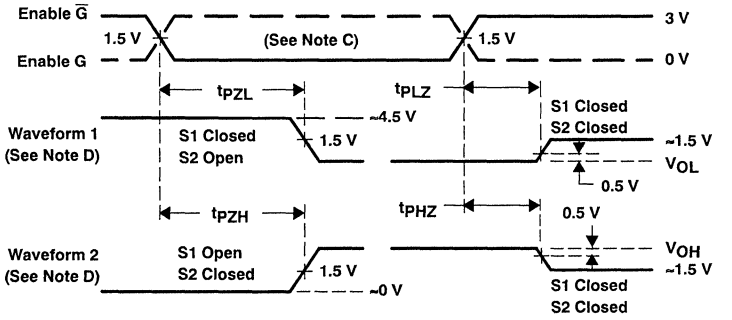
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF,	See Figure 1,	S1 and S2 open		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					14	20	ns
	Output-to-output skew					1	6	ns
t_{PZH}	Output enable time to high level	C_L = 30 pF,	R_L = 75 Ω,	See Figure 1		25	40	ns
t_{PZL}	Output enable time to low level	C_L = 30 pF,	R_L =180 Ω,	See Figure 1		37	45	ns
t_{PHZ}	Output disable time from high level	C_L = 10 pF,	See Figure 1,	S1 and S2 closed		21	30	ns
t_{PLZ}	Output disable time from low level					23	35	ns

PARAMETER MEASUREMENT INFORMATION

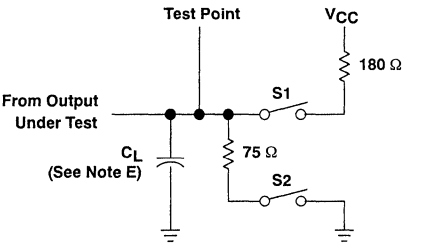


PROPAGATION DELAY TIMES AND SKEW



ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS



TEST CIRCUIT

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$, $t_r \leq 15$ ns, and $t_f \leq 6$ ns.
B. When measuring propagation delay times and skew, switches S1 and S2 are open.
C. Each enable is tested separately.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. C_L includes probe and jig capacitance.

Figure 1. Switching Times

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

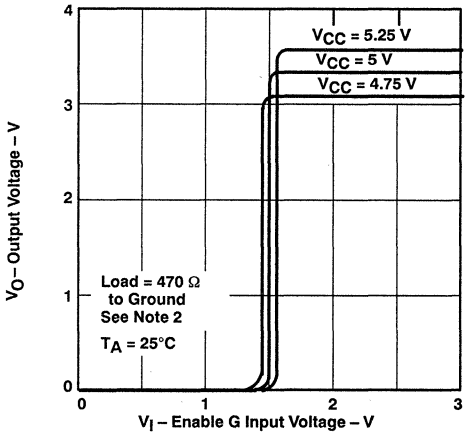


Figure 2

OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

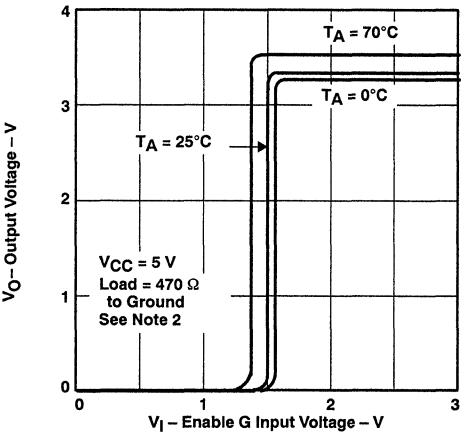


Figure 3

OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

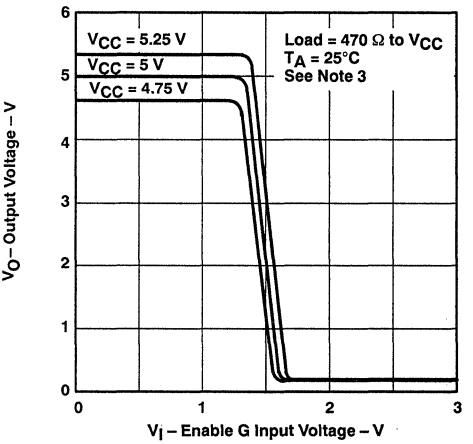


Figure 4

OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

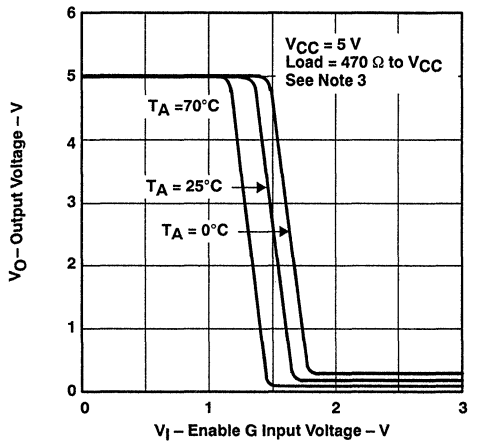


Figure 5

NOTES: 2. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.
3. The A input is connected to ground during the testing of the Y ouputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

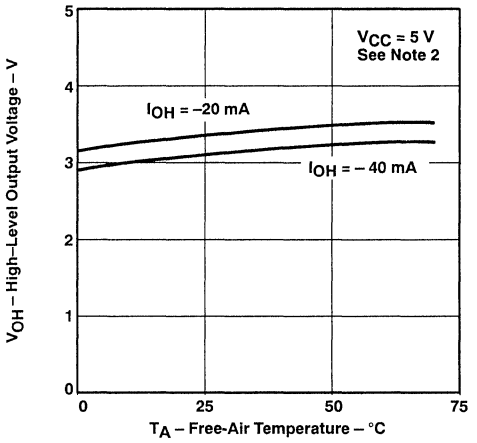


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

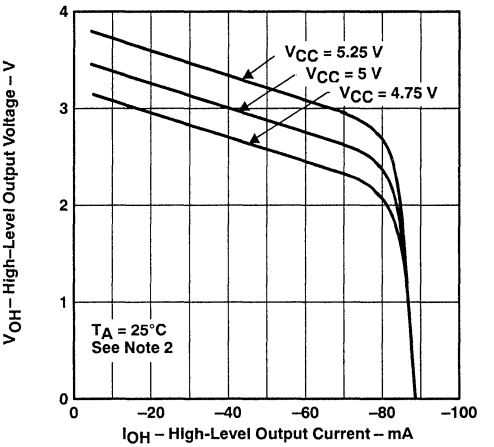


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

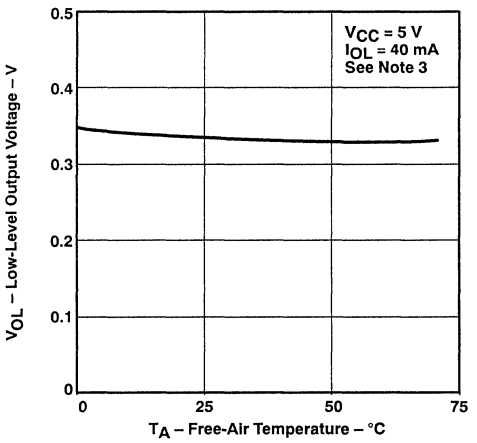


Figure 8

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

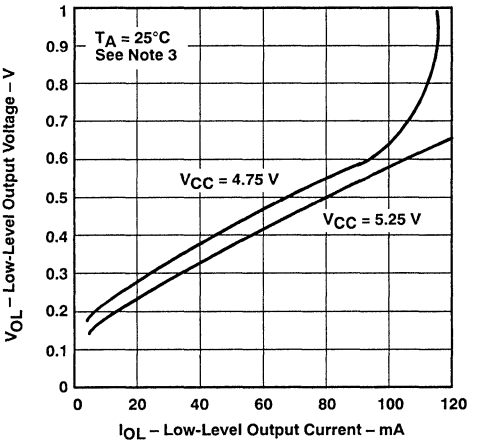


Figure 9

NOTES: 2. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.
3. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

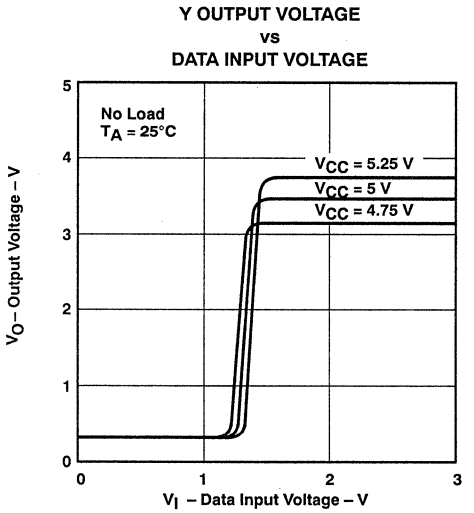


Figure 10

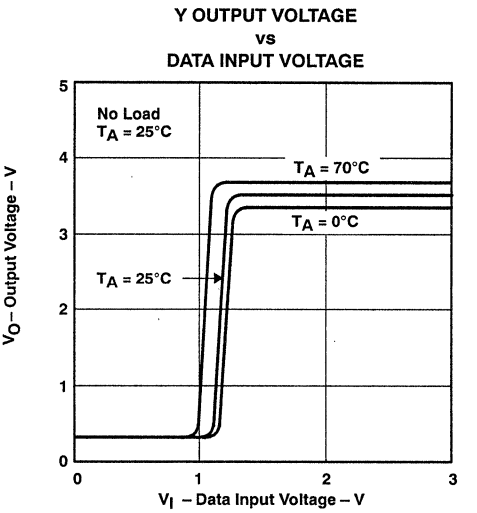
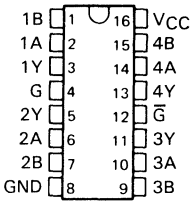


Figure 11

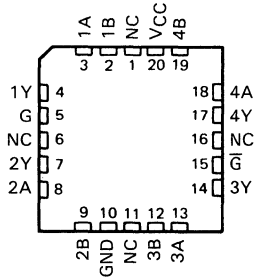
D2434, OCTOBER 1980—REVISED SEPTEMBER 1986

- **AM26LS32A Meets EIA Standards RS-422-A and RS-423-A**
- **AM26LS32A Has ±7-V Common-Mode Range With ±200-mV Sensitivity**
- **AM26LS33A Has ±15-V Common-Mode Range With ±500 mV Sensitivity**
- **Input Hysteresis . . . 50 mV Typical**
- **Operates From a Single 5-V Supply**
- **Low-Power Schottky Circuitry**
- **3-State Outputs**
- **Complementary Output Enable Inputs**
- **Input Impedance . . . 12 kΩ Min**
- **Designed to Be Interchangeable With Advanced Micro Devices AM26LS32C and AM26LS33C**

AM26LS32AC, AM26LS33AC . . . D, J, OR N PACKAGE
AM26LS32AM, AM26LS33AM . . . J PACKAGE
(TOP VIEW)



AM26LS32AM, AM26LS33AM . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The AM26LS32A and AM26LS33A are quadruple line receivers for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. Three-state outputs permit connection directly to a bus-organized system. Fail-safe design ensures that if the inputs are open, the outputs will always be high.

Compared to the AM26LS32C and the AM26LS33C, the AM26LS32A and AM26LS33A incorporate an additional stage of amplification to improve sensitivity. The input impedance has been increased resulting in less loading of the bus line. The additional stage has increased propagation delay; however, this will not affect interchangeability in most applications.

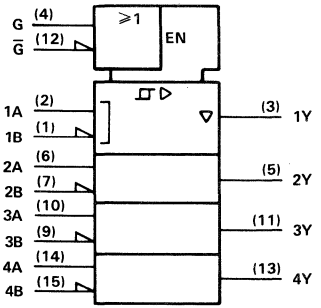
The AM26LS32AC and AM26LS33AC are characterized for operation from 0°C to 70°C. The AM26LS32AM and the AM26LS33AM are characterized for operation over the full military temperature range of −55°C to 125°C.

FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUT	ENABLES G	ENABLES $\overline{G}$	OUTPUT
$V_{ID} \geq V_{TH}$	H	X	H
	X	L	H
$V_{TL} \leq V_{ID} \leq V_{TH}$	H	X	?
	X	L	?
$V_{ID} \leq V_{TL}$	H	X	L
	X	L	L
X	L	H	Z

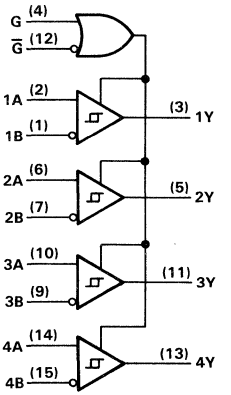
H = high level, L = low level, X = irrelevant
Z = high impedance (off), ? = indeterminate

logic symbol†

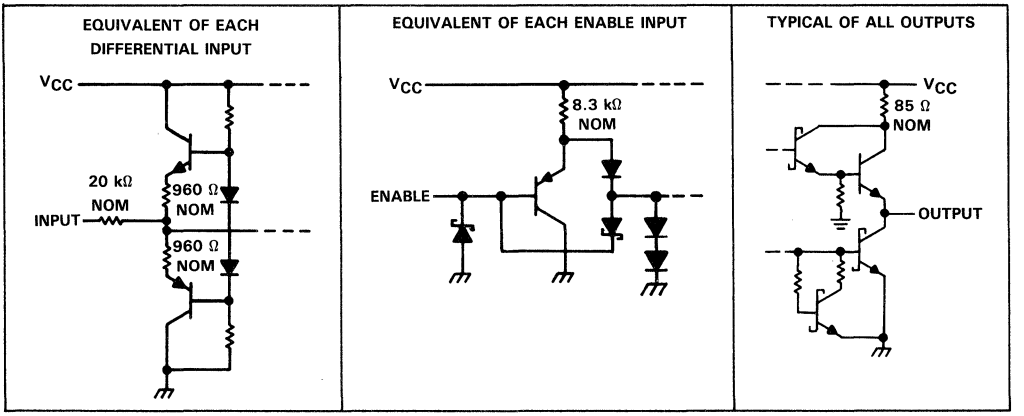


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		AM26LS32AC AM26LS33AC	AM26LS32AM AM26LS33AM	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage, any differential input		±25	±25	V
Differential input voltage (see Note 2)		±25	±25	V
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range		0 to 70	−55 to 125	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package	260		°C
Case temperature for 60 seconds	FK package		260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package	300	300	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltage values are at the noninverting (A) input terminals with respect to the inverting (B) input terminals.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	–
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (C-SUFFIX)	1025 mW	8.2 mW/°C	656 mW	–
J (M-SUFFIX)	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	–

recommended operating conditions

		AM26LS32AC AM26LS33AC			AM26LS32AM AM26LS33AM			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.25	4.5	5	5.5	V
High-level input voltage, V_{IH}		2			2			V
Low-level input voltage, V_{IL}				0.8			0.8	V
Common-mode input voltage, V_{IC}	AM26LS32AC, AM26LS32AM			±7			±7	V
	AM26LS33AC, AM26LS33AM			±15			±15	
High-level output current, I_{OH}				−440			−440	μA
Low-level output current, I_{OL}				8			8	mA
Operating free-air temperature, T_A		0		70	−55		125	°C

electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

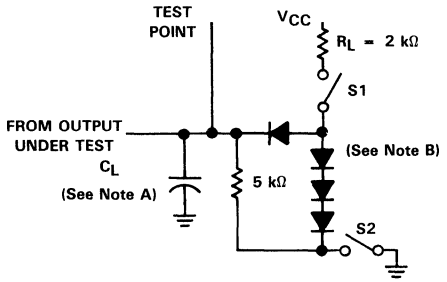
PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{TH}	Differential input high-threshold voltage	$V_O = V_{OH}$min,	$I_{OH} = -440\ \mu A$	AM26LS32A			0.2	V
				AM26LS33A			0.5	
V_{TL}	Differential input low-threshold voltage	$V_O = 0.45$ V,	$I_{OL} = 8$ mA	AM26LS32A	−0.2‡			V
				AM26LS33A	−0.5‡			
V_{hys}	Hysteresis, $V_{T+} - V_{T-}$§					50		mV
V_{IK}	Enable input clamp voltage	$V_{CC} = $ MIN,	$I_I = -18$ mA				−1.5	V
V_{OH}	High-level output voltage	$V_{CC} = $ MIN, $V_{I(\overline{G})} = 0.8$ V,	$V_{ID} = 1$ V, $I_{OH} = -440\ \mu A$	'32AC, '33AC	2.7			V
				'32AM, '33AM	2.5			
V_{OL}	Low-level output voltage	$V_{CC} = $ MIN, $V_{I(\overline{G})} = 0.8$ V	$V_{ID} = -1$ V,	$I_{OL} = 4$ mA			0.4	V
				$I_{OL} = 8$ mA			0.45	
I_{OZ}	Off-state (high-impedance-state) output current	$V_{CC} = $ MAX		$V_O = 2.4$ V			20	μA
				$V_O = 0.4$ V			−20	
I_I	Line input current	$V_I = 15$ V,	Other input at −10 V to 15 V				1.2	mA
		$V_I = -15$ V,	Other input at −15 V to 10 V				−1.7	
$I_{I(EN)}$	Enable input current	$V_I = 5.5$ V					100	μA
I_{IH}	High-level enable current	$V_I = 2.7$ V					20	μA
I_{IL}	Low-level enable current	$V_I = 0.4$ V					−0.36	mA
r_i	Input resistance	$V_{IC} = -15$ V to 15 V, One input to AC ground			12	15		kΩ
I_{OS}	Short-circuit output current¶	$V_{CC} = $ MAX			−15		−85	mA
I_{CC}	Supply current	$V_{CC} = $ MAX,	All outputs disabled			52	70	mA

†All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$, and $V_{IC} = 0$.
‡The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figures 10 and 11.
¶Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

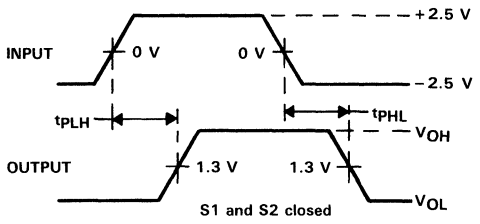
switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L = 15$ pF, See Figure 1		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			22	35	ns
t_{PZH}	Output enable time to high level	$C_L = 15$ pF, See Figure 1		17	22	ns
t_{PZL}	Output enable time to low level			20	25	ns
t_{PHZ}	Output disable time from high level	$C_L = 5$ pF, See Figure 1		21	30	ns
t_{PLZ}	Output disable time from low level			30	40	ns

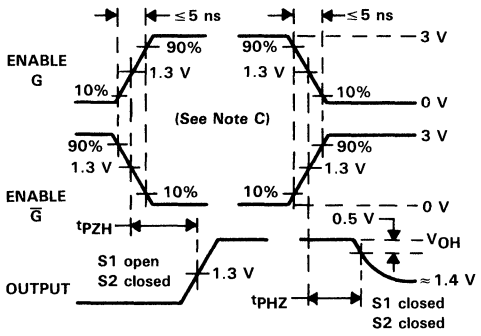
PARAMETER MEASUREMENT INFORMATION



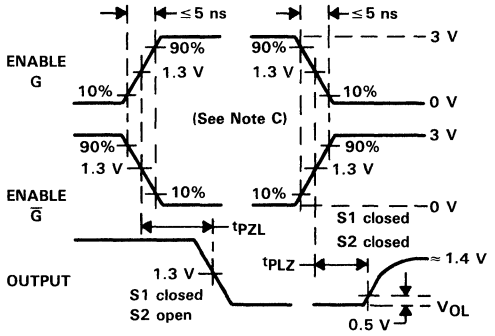
TEST CIRCUIT



VOLTAGE WAVEFORMS FOR t_{PLH}, t_{PHL}



VOLTAGE WAVEFORMS FOR t_{PHZ}, t_{PZH}



VOLTAGE WAVEFORMS FOR t_{PLZ}, t_{PZL}

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

FIGURE 1

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

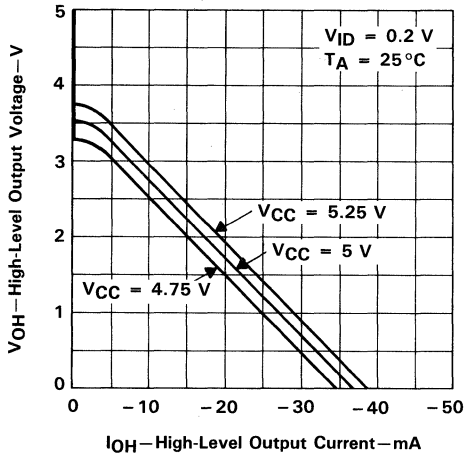


FIGURE 2

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

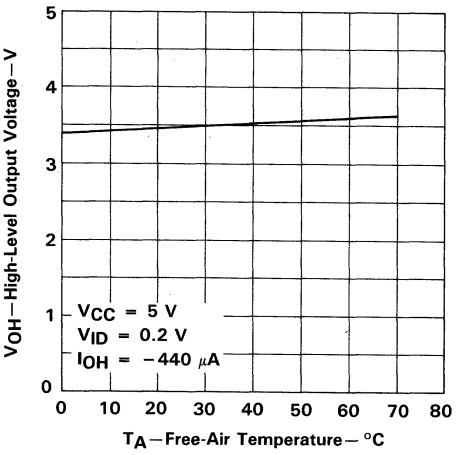


FIGURE 3

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

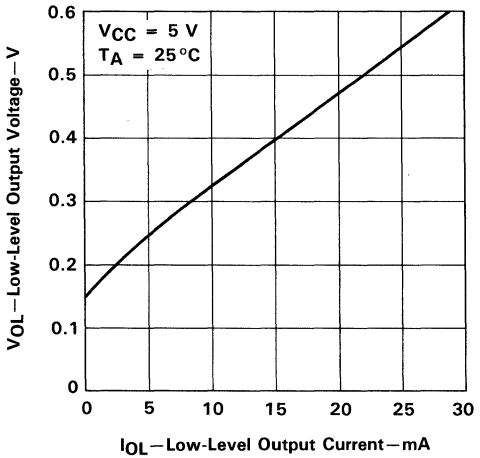


FIGURE 4

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

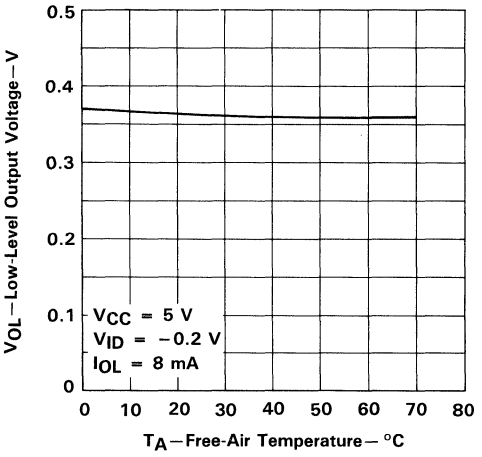


FIGURE 5

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

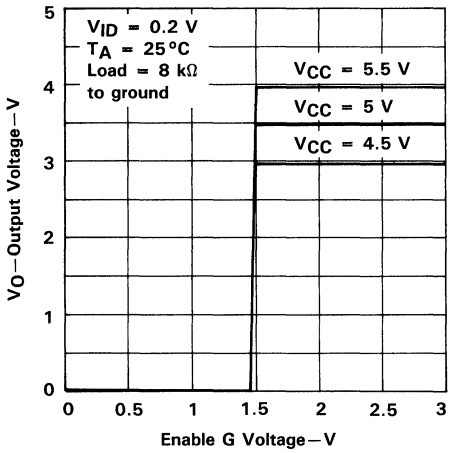


FIGURE 6

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

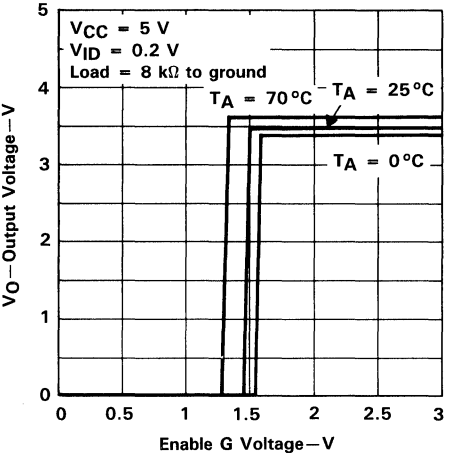


FIGURE 7

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

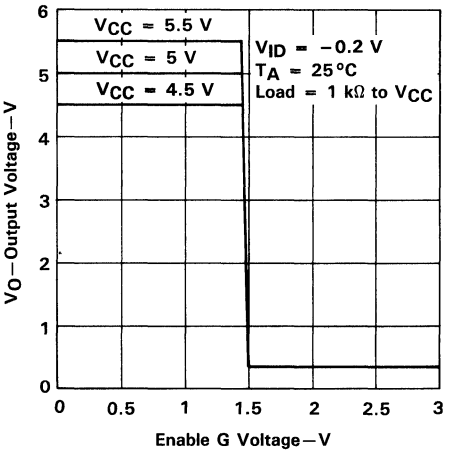


FIGURE 8

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

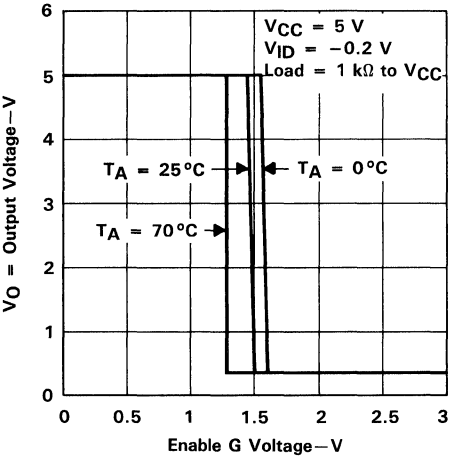


FIGURE 9

TYPICAL CHARACTERISTICS

AM26LS32A
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

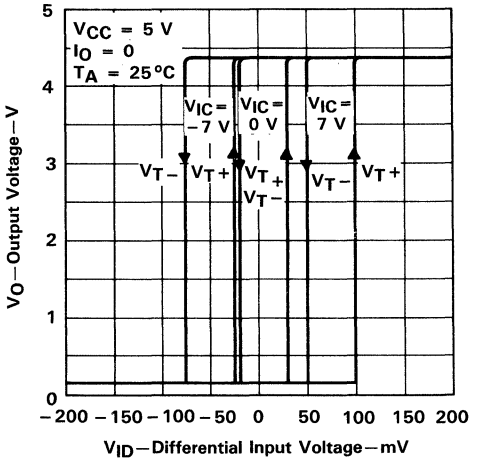


FIGURE 10

AM26LS33A
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

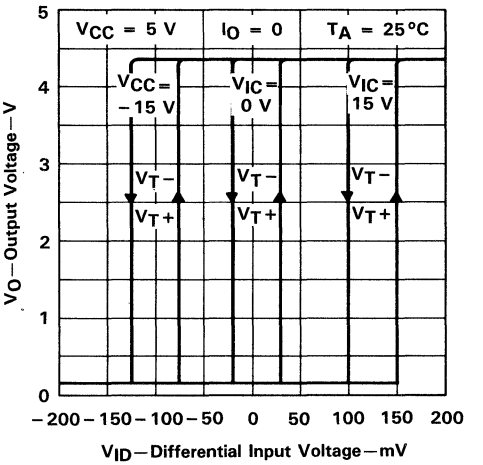


FIGURE 11

INPUT CURRENT
vs
INPUT VOLTAGE

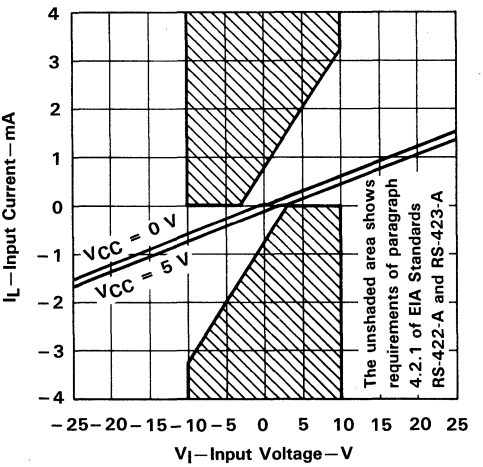
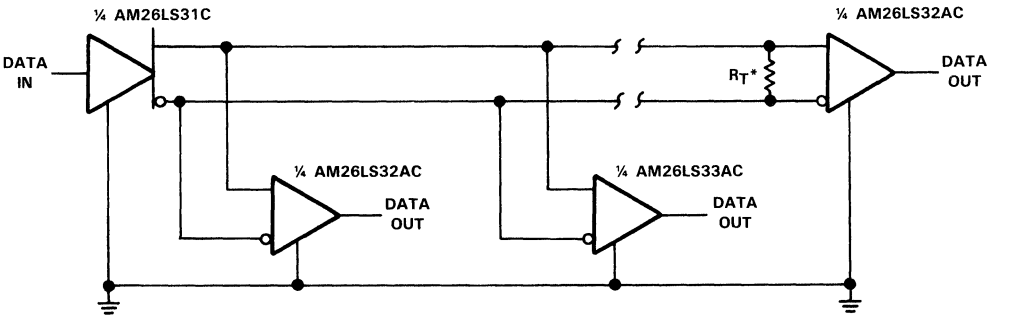


FIGURE 12

APPLICATION INFORMATION



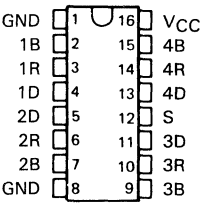
*R_T equals the characteristic impedance of the line.

FIGURE 13. CIRCUIT WITH MULTIPLE RECEIVERS

D2298, JANUARY 1977—REVISED MAY 1990

- **Schottky Circuitry for High Speed, Typical Propagation Delay Time . . . 12 ns**
- **Drivers Feature Open-Collector Outputs for Party-Line (Data Bus) Operation**
- **Driver Outputs Can Sink 100 mA at 0.8 V Maximum**
- **P-N-P Inputs for Minimal Input Loading**
- **Designed to Be Interchangeable With Advanced Micro Devices AM26S10 and AM26S11**

AM26S10C, AM26S11C . . . D, J, OR N PACKAGE
(TOP VIEW)



description

The AM26S10 and AM26S11 are quadruple bus transceivers utilizing Schottky-diode-clamped transistors for high speed. The drivers feature open-collector outputs capable of sinking 100 mA at 0.8 V maximum. The driver and strobe inputs use p-n-p transistors to reduce the input loading.

The driver of the AM26S10 is inverting; the driver of the AM26S11 is noninverting. Each device has two ground connections for improved ground current-handling capability. For proper operation, the ground pins should be tied together.

The AM26S10C and AM26S11C are characterized for operation over the temperature range of 0°C to 70°C.

AM26S10
FUNCTION TABLE
(TRANSMITTING)

INPUTS		OUTPUTS	
S	D	B	R
L	H	L	H
L	L	H	L

AM26S11
FUNCTION TABLE
(TRANSMITTING)

INPUTS		OUTPUTS	
S	D	B	R
L	H	H	L
L	L	L	H

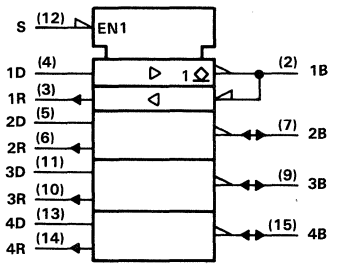
AM26S10 AND AM26S11
FUNCTION TABLE
(RECEIVING)

INPUTS			OUTPUT
S	B	D	R
H	H	X	L
H	L	X	H

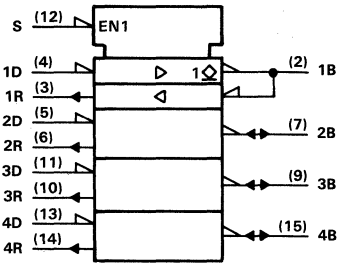
H = high level, L = low level, X = irrelevant

logic symbols†

AM26S10



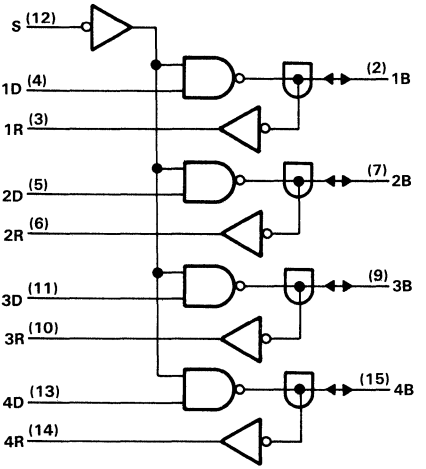
AM26S11



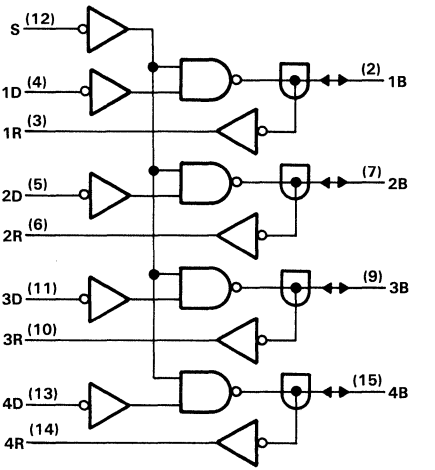
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

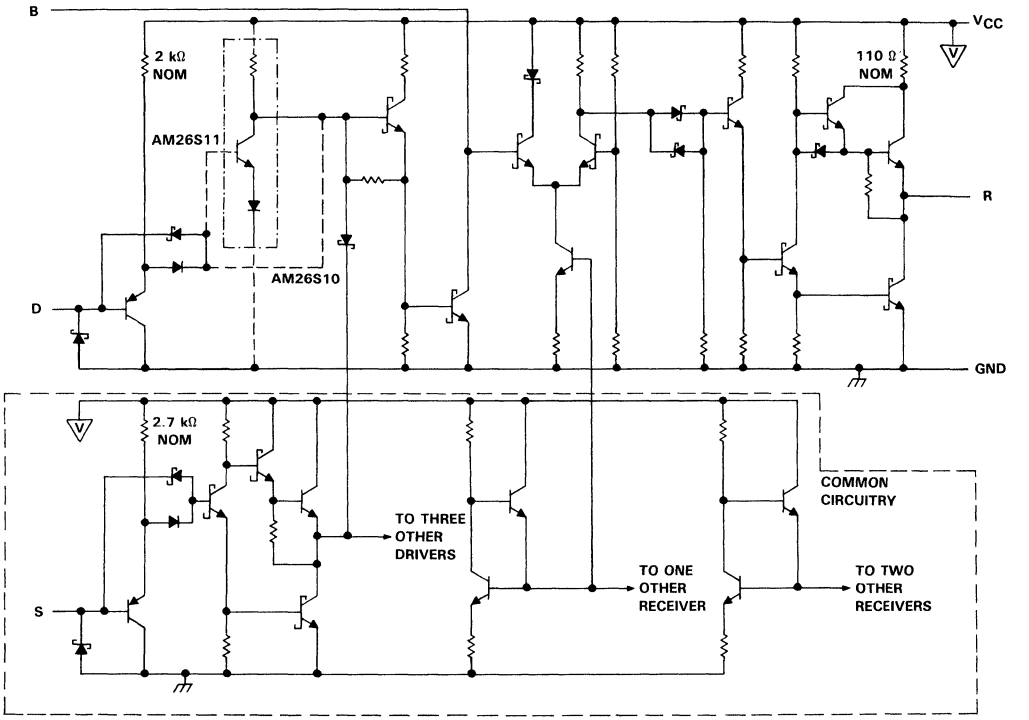
AM26S10



AM26S11



schematic (each transceiver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Driver or strobe input voltage range . . . . . −0.5 V to 5.5 V
Bus voltage range, driver output off . . . . . −0.5 V to 5.25 V
Driver or strobe input current range . . . . . −30 mA to 5 mA
Driver output current . . . . . 200 mA
Receiver output current . . . . . 30 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminals connected together.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
J	1025 mW	8.2 mW/°C	656 mw
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	D or S	2			V
	B	2.25			
Low-level input voltage, V_{IL}	D or S			0.8	V
	B			1.75	
Receiver high-level output current, I_{OH}				−1	mA
Low-level output current, I_{OL}	Driver			100	mA
	Receiver			20	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

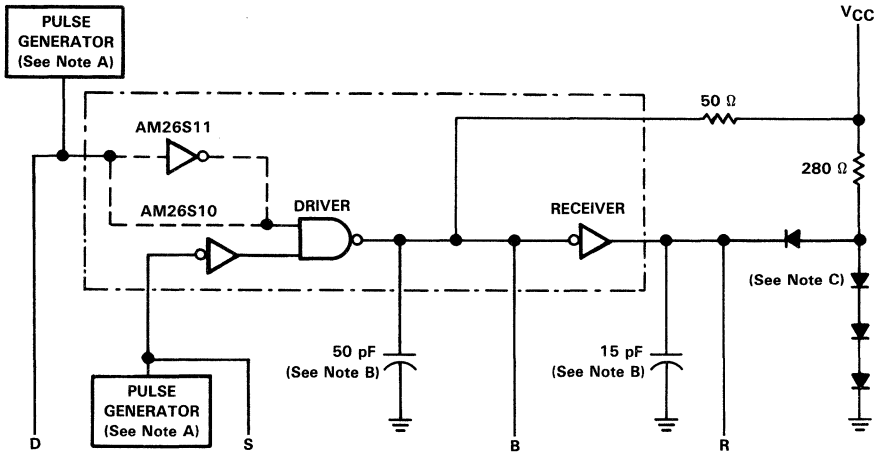
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	D or S	V_{CC} = 4.75 V, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	R	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA		2.7	3.4		V
V_{OL}	Low-level output voltage	R	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 20 mA			0.5	V
		B		I_{OL} = 40 mA		0.33	0.5	
				I_{OL} = 70 mA		0.42	0.7	
				I_{OL} = 100 mA		0.51	0.8	
$I_{O(off)}$	Off-state output current	B	V_{IH} = 2 V, V_{IL} = 0.8 V	V_{CC} = 5.25 V, V_O = 0.8 V			−50	μA
				V_{CC} = 5.25 V, V_O = 4.5 V			100	
				V_{CC} = 0, V_O = 4.5 V			100	
I_{IH}	High-level input current	D	V_{CC} = 5.25 V, V_I = 2.7 V				30	μA
		S					20	
I_I	Input current at maximum input voltage	D or S	V_{CC} = 5.25 V, V_I = 5.5 V				100	μA
I_{IL}	Low-level input current	D	V_{CC} = 5.25 V, V_I = 0.4 V				−0.54	mA
		S					−0.36	
I_{OS}	Short-circuit output current‡	R	V_{CC} = 5.25 V		−18		−60	mA
I_{CC}	Supply current		V_{CC} = 5.25 V, Strobe at 0 V, No load, All driver outputs low			45	70	mA
							80	

†All typical values are at T_A = 25°C and V_{CC} = 5 V.
‡Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

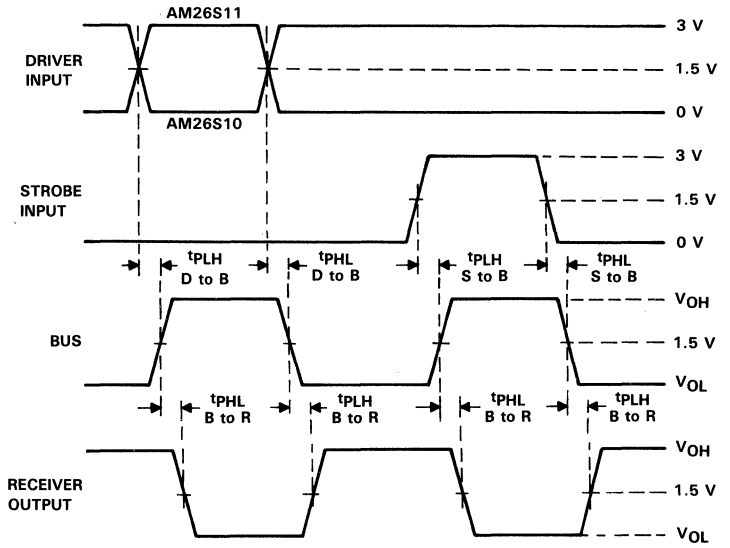
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM	TO	TEST CONDITIONS	AM26S10			AM26S11			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	D	B	See Figure 1		10	15		12	19	ns
t_{PHL}	Propagation delay time, high-to-low-level output					10	15		12	19	
t_{PLH}	Propagation delay time, low-to-high-level output	S	B			14	18		15	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					13	18		14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	B	R			10	15		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output					10	15		10	15	
t_{TLH}	Transition time, low-to-high-level output		B		4	10		4	10		ns
t_{THL}	Transition time, high-to-low-level output				2	4		2	4		

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, t_r = 10 ± 5 ns.
B. Includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

FIGURE 1

APPLICATION INFORMATION

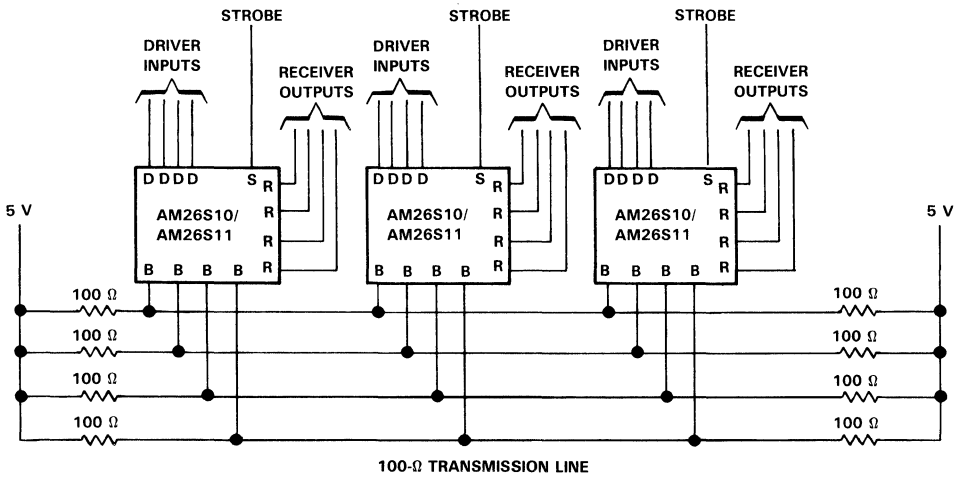
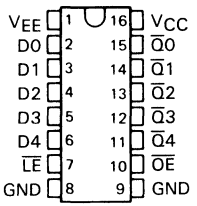


FIGURE 2. PARTY-LINE SYSTEM

D3058, NOVEMBER 1987--REVISED DECEMBER 1988

- **ECL Control Inputs**
- **3-State Outputs**
- **10K ECL Input Compatible**
- **Package Options Include Plastic "Small Outline" Package and Standard Plastic 300-mil DIPs**
- **Direct Replacement for National Semiconductor DP8480**

D OR N PACKAGE
(TOP VIEW)



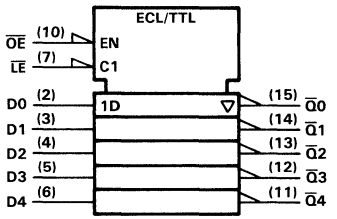
description

This circuit translates ECL input levels to TTL output levels and provides an inverting transparent latch. The 3-state outputs are designed to drive highly capacitive loads. All inputs operate at ECL levels.

If Latch Enable ($\overline{LE}$) is low, the latches are transparent and the $\overline{Q}$ outputs follow the complement of the D inputs. If $\overline{LE}$ is high, the outputs are latched. If output enable ($\overline{OE}$) is high, the outputs are in the high-impedance state, as they are during power up and power down.

The DP8480 is characterized for operation from 0°C to 75°C.

logic symbol†

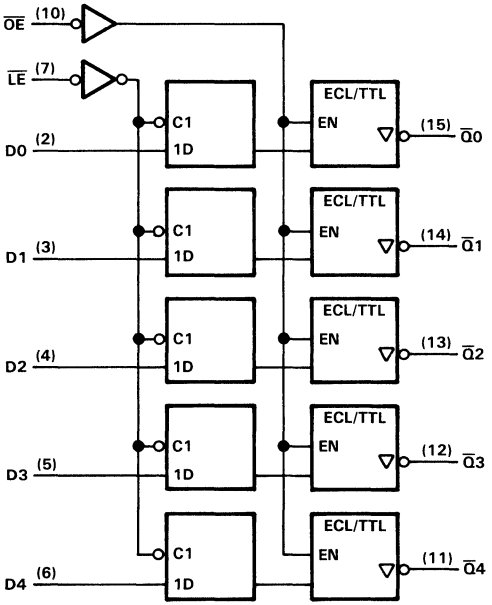


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(EACH LATCH/TRANSLATOR)

$\overline{OE}$	$\overline{LE}$	D	$\overline{Q}$
H	X	X	Z
L	L	L	H
L	L	H	L
L	H	X	Q_0

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Supply voltage, V_{EE} . . . . . −8 V
Input voltage, V_I . . . . . 0 V to V_{EE}
Output voltage, V_O . . . . . 5.5 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 75°C$ POWER RATING
D	950 mW	7.6 mW/°C	570 mW
N	1150 mW	9.2 mW/°C	690 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Supply voltage, V_{EE}		−4.68	−5.20	−5.72	V
High-level input voltage, V_{IH} (see Note 1)	T_A = 0°C	−1145		−840	mV
	T_A = 25°C	−1105		−810	
	T_A = 75°C	−1045		−720	
Low-level input voltage, V_{IL} (see Note 1)	T_A = 0°C	−1870		−1490	mV
	T_A = 25°C	−1850		−1475	
	T_A = 75°C	−1830		−1450	
Pulse duration, $\overline{LE}$ low, t_w (see Figure 1)		5			ns
Setup time, data before $\overline{LE}$↑, t_{su} (see Figure 1)		3			ns
Hold time, data after $\overline{LE}$↑, t_h (see Figure 1)		3			ns
Operating free-air temperature, T_A		0		75	°C

NOTE 1: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −10 mA	$V_{CC}-2$			V
V_{OL}	Low-level output voltage	I_{OL} = 12 mA		0.2	0.5	V
I_{IH}	High level input current	$V_{IH} = V_{IH}$ max		75	350	μA
I_{IL}	Low-level input current	$V_{IL} = V_{IL}$ min		50	85	μA
I_{OHS}	High-state short-circuit output current	V_{OHS} = 0, See Note 2	−70	−150		mA
I_{OLS}	Low-state short-circuit output current	V_{OLS} = 2.5 V, See Note 2	70	150		mA
I_{OZ}	High-impedance state output current	V_O = 0 to 5 V		±1	±50	μA
I_{CC}	Supply current from V_{CC}	Outputs open, Inputs = V_{IL}		16	35	mA
I_{EE}	Supply current from V_{EE}	Outputs open, Inputs = V_{IL}		−30	−50	mA

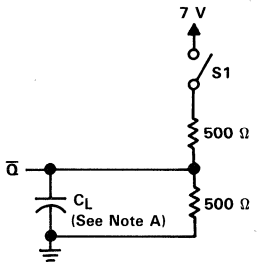
†Typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.
NOTE 2: During testing of I_{OHS} or I_{OLS}, only one output should be tested at a time and the current should be limited to a maximum of ±120 mA.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{LE}$ input	C_L = 50 pF, See Figure 1	4	10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{LE}$ input		4	11	15	ns
t_{PLH}	Propagation delay time, low-to-high-level output from D input		3.5	10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output from D input		3.5	11	15	ns
t_{en}	Output enable time from $\overline{OE}$ input		6	12	25	ns
t_{dis}	Output disable time from $\overline{OE}$ input		4.5	8	22	ns

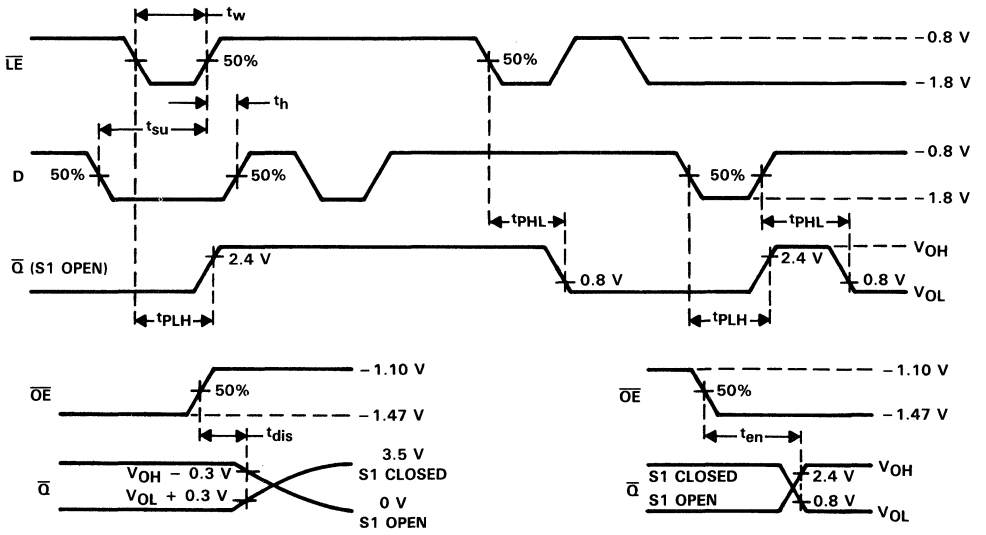
†Typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C, and with all channels switched simultaneously.

PARAMETER MEASUREMENT INFORMATION



OUTPUT LOAD CIRCUIT

NOTE A: C_L includes probe and jig capacitance.



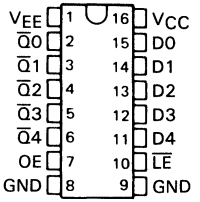
NOTE B: ECL input rise times and fall time are 2 ns ±0.2 ns from 20% to 80%.

FIGURE 1. SWITCHING CHARACTERISTICS

D3059, NOVEMBER 1987 – REVISED AUGUST 1989

- **ECL Control Inputs**
- **10K ECL Compatible**
- **Propagation Delay . . . 4 ns Typ**
- **Package Options Include Plastic "Small Outline" Package and Standard Plastic 300-mil DIPs**
- **Direct Replacement for National Semiconductor DP8481**

D OR N PACKAGE
(TOP VIEW)



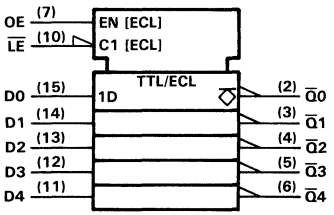
description

This circuit translates TTL input levels to ECL output levels and provides a 5-bit transparent latch. The outputs are gated by Output Enable (OE) and can be wire-OR connected. The Latch Enable ($\overline{LE}$) and OE inputs are ECL.

If Latch Enable ($\overline{LE}$) is low, the latches are transparent and the $\overline{Q}$ outputs follow the complement of the D inputs. If $\overline{LE}$ is high, the outputs are latched. If Output Enable (OE) is low, the outputs are forced to the low level.

The DP8481 is characterized for operation from 0°C to 75°C.

logic symbol†

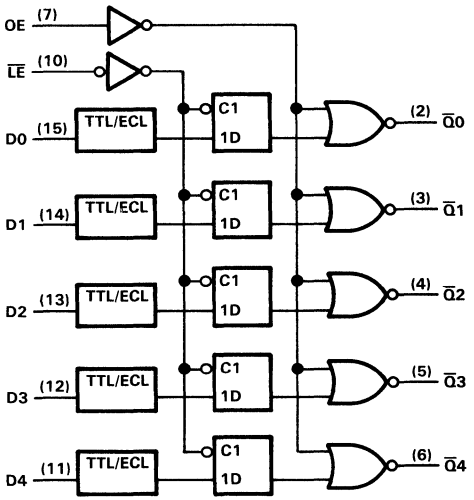


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(EACH LATCH/TRANSLATOR)

OE	$\overline{LE}$	D	$\overline{Q}$
H	L	H	L
H	L	L	H
H	H	X	Q_0
L	X	X	L

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Supply voltage, V_{EE} . . . . . −8 V
Input voltage, V_I: OE or $\overline{LE}$ input . . . . . 0 V to V_{EE}
D inputs . . . . . −1 V to 5.5 V
Output current, I_O . . . . . −50 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating temperature range, T_A . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 75°C$ POWER RATING
D	950 mW	7.6 mW/°C	570 mW
N	1150 mW	9.2 mW/°C	690 mW

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			4.5	5	5.5	V
Supply voltage, V_{EE}			−4.68	−5.20	−5.72	V
High-level input voltage, V_{IH} (TTL-level D inputs)			2			V
Low-level input voltage, V_{IL} (TTL-level D inputs)					0.8	V
High-level input voltage, V_{IH} (ECL-level OE and $\overline{LE}$ inputs) (see Note 1)	T_A = 0°C		−1145		−840	mV
	T_A = 25°C		−1105		−810	
	T_A = 75°C		−1045		−720	
Low-level input voltage, V_{IL} (ECL-level OE and $\overline{LE}$ Inputs) (see Note 1)	T_A = 0°C		−1870		−1490	mV
	T_A = 25°C		−1850		−1475	
	T_A = 75°C		−1830		−1450	
Pulse duration, $\overline{LE}$ low, t_w		(see Figure 1)	5			ns
Setup time, t_{su}	Data before $\overline{LE}$↑	(see Figure 1)	5			ns
	Data before OE↑ (see Note 2)	(see Figure 1)	5.5			
Hold time, data after $\overline{LE}$↑, t_h		(see Figure 1)	1			ns
Operating free-air temperature, T_A			0		75	°C

NOTES: 1. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.
2. This setup time applies when operating in the transparent mode ($\overline{LE}$ is low) and it is necessary that valid data be available at the output immediately after the outputs are enabled.

electrical characteristics over recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	D0-D4	I_I = −12 mA		−0.8	−1.2	V
I_{IH}	High-level input current	D0-D4	V_I = 2.5 V		1	40	μA
		OE, $\overline{LE}$	V_I = −0.8 V			200	
I_{IL}	Low-level input current	D0-D4	V_I = 0.5 V		−50	−200	μA
		OE,$\overline{LE}$	V_I = −1.8 V			150	
V_{OH}	High-level output voltage (see Notes 1 and 3)		V_{EE} = −5.2 V, T_A = 0°C	−1000		−840	mV
			V_{EE} = −5.2 V, T_A = 25°C	−960		−810	
			V_{EE} = −5.2 V, T_A = 75°C	−900		−720	
V_{OHC}	Critical high-level output voltage (see Notes 1 and 3)		V_{EE} = −5.2 V, T_A = 0°C	−1020			mV
			V_{EE} = −5.2 V, T_A = 25°C	−980			
			V_{EE} = −5.2 V, T_A = 75°C	−920			
V_{OL}	Low-level output voltage (see Notes 1 and 3)		V_{EE} = −5.2 V, T_A = 0°C	−1870		−1665	mV
			V_{EE} = −5.2 V, T_A = 25°C	−1850		−1650	
			V_{EE} = −5.2 V, T_A = 75°C	−1830		−1625	
V_{OLC}	Critical low-level output voltage (see Notes 1 and 3)		V_{EE} = −5.2 V, T_A = 0°C			−1645	mV
			V_{EE} = −5.2 V, T_A = 25°C			−1630	
			V_{EE} = −5.2 V, T_A = 75°C			−1605	
I_{CC}	Supply current from V_{CC}		V_{CC} = 5.5 V			20	mA
I_{EE}	Supply current from V_{EE}		V_{EE} = −5.7 V			−90	mA

NOTES: 1. The algebraic convention, in which the least positive (most negative) value is designated one minimum, is used in this data sheet for logic levels only.

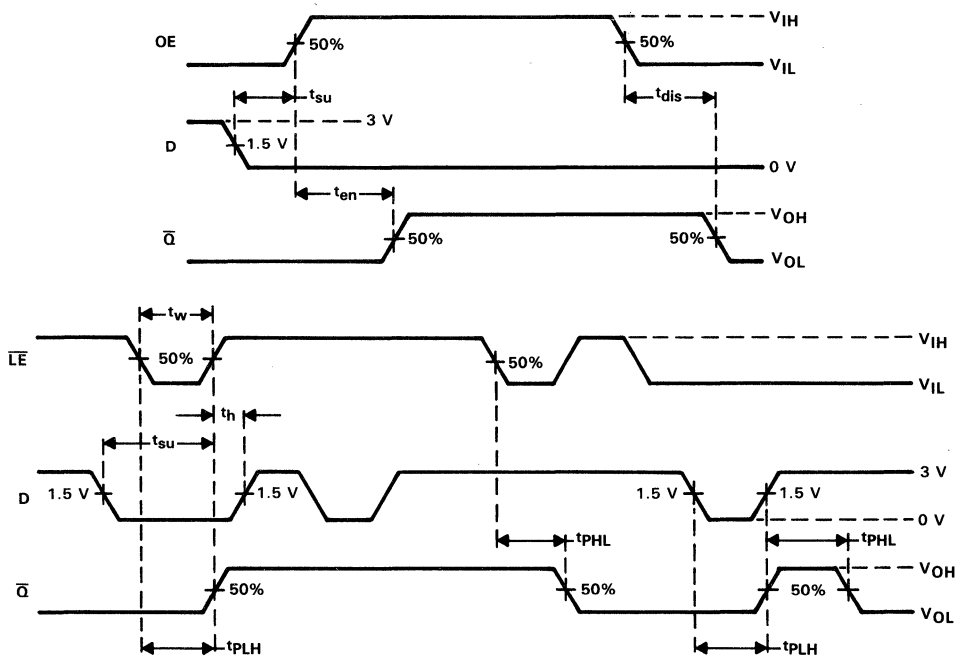
3. V_{OH} and V_{OL} are tested using the "outer-limit" values V_{IH} max and V_{IL} min. The "critical" values V_{OHC} and V_{OLC} are tested using the "inner-limit" values V_{IH} min and V_{IL} max. The latter values ensure the noise margins of 155 mV high and 125 mV low associated with 10K ECL.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output from $\overline{LE}$ input	R_L = 50 Ω to −2 V, See Figure 1	1.5	4	6	ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{LE}$ input		1.5	4	6	ns
t_{PLH}	Propagation delay time, low-to-high-level output from D input		2.5	4	7.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output from D input		2.5	4	7.5	ns
t_{en}	Output enable time from OE input		1	3	4	ns
t_{dis}	Output disable time from OE input		1	3	4	ns

†Typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



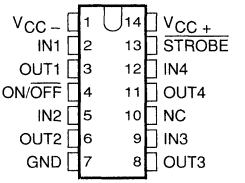
NOTE A: ECL input rise and fall times at OE and $\overline{LE}$ are 2 ns ±0.2 ns from 20% to 80%. TTL input rise and fall times at D inputs are 3 ns maximum measured between 10% and 90%.

FIGURE 1. SWITCHING TIME WAVEFORMS

D3297, APRIL 1989—REVISED JULY 1989

- **Low Supply Voltage ... ±5 V to ±15 V**
- **Supply Current ... 500 μA Typ**
- **Zero Supply Current When Shut Down**
- **Outputs Can Be Driven ±30 V**
- **Output Open When Off (3-State)**
- **10-mA Output Drive**
- **Output of Several Devices Can Be Paralleled**
- **Meets ANSI/EIA-232-D-1986 Specifications (Revision of EIA Std RS-232-C)**
- **Designed to Be Interchangeable With Linear Technology LT1030**

LT1030 ... D OR N PACKAGE
(TOP VIEW)



NC – No internal connection

AVAILABLE OPTIONS

T_A	PACKAGE	
	SMALL OUTLINE (D)	PLASTIC DIP (N)
0°C to 70°C	LT1030CD	LT1030CN

The D package is available taped and reeled. Add the suffix R to the device type (i.e., LT1030CDR).

description

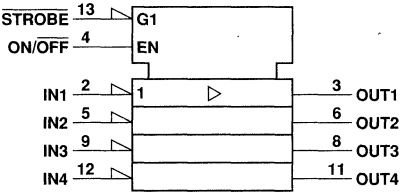
The LT1030 is an EIA-232 line driver that operates over a ±5-V to ±15-V supply voltage range on low supply current. The device can be shut down to zero supply current. Current-limiting fully protects the outputs from externally applied voltages of ±30 V. Since the output swings to within 200 mV of the positive supply and to within 1 V of the negative supply, supply voltage requirements are minimized.

A major advantage of the LT1030 is the high-impedance output state when the device is off or powered down. This feature allows several different drivers on the same bus.

The device can be used as an EIA-232 driver, micropower interface, or level translator, among others.

The LT1030 is characterized for operation from 0°C to 70°C.

logic symbol†

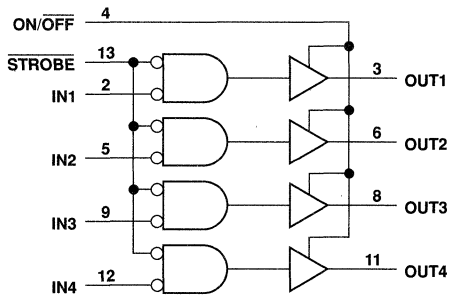


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

pin descriptions

PIN NAME	PIN NO	DESCRIPTION
GND	7	Ground pin.
IN1, IN2, IN3, IN4	2, 5, 9, 12	Logic inputs. Operate properly on TTL or CMOS levels. Output valid from V_I = V_{CC-} + 2 V to 15 V. Connect to 5 V when not used.
ON/$\overline{OFF}$	4	Shuts down entire circuit. Cannot be left open. For "normally on" operation, connect between 5 V and 10 V. If V_{IL} is at or near 0.8 V, significant settling time may be required.
OUT1, OUT2, OUT3, OUT 4	3, 6, 8, 11	Line driver outputs.
$\overline{STROBE}$	13	Forces all outputs low. Drive with 3 V. Strobe terminal input impedance is approximately 2 kΩ to GND. Leave open when not used.
V_{CC+}	14	Positive supply.
V_{CC-}	1	Negative supply.

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC+} (see Note 1) . . . . . 0 V to 15 V
Supply voltage range, V_{CC-} . . . . . 0 V to –15 V
Input voltage range, logic inputs . . . . . V_{CC-} to 25 V
Input voltage range, ON/$\overline{OFF}$ pin . . . . . 0 V to 12 V
Output voltage range (any output) . . . . . V_{CC+} – 30 V to V_{CC-} + 30 V
Duration of output short-circuit at (or below) 25°C (to ±30 V, see Note 2) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the GND terminal.
2. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply voltage, V_{CC+}	5		15	V
Supply voltage, V_{CC-}	–5		–15	V
High-level input voltage, V_{IH} (see Note 3)	2		15	V
Low-level input voltage, V_{IL} (see Note 3)			0.8	V
Operating free-air temperature, T_A	0		70	°C

NOTE 3: These V_{IH} and V_{IL} specifications apply only for inputs IN1-IN4. For operating levels for ON/$\overline{OFF}$, see Figure 2.

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electrical characteristics over operating free-air temperature range, $V_{CC\pm}$ = ±5 V to ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OM+}	Maximum positive peak output voltage swing	I_O = −2 mA, T_A = 25°C	V_{CC+} − 0.3 V_{CC+} − 0.1			V
V_{OM-}	Maximum negative peak output voltage swing	I_O = 2 mA, T_A = 25°C		V_{CC-} + 0.9 V_{CC-} + 1.4		V
I_{IH}	High-level input current	$V_I \geq$ 2 V, T_A = 25°C		2	20	µA
I_{IL}	Low-level input current	$V_I \leq$ 0.8 V, T_A = 25°C		10	20	µA
I_I	ON/$\overline{OFF}$ terminal current	V_I = 0		−0.1	−10	µA
		V_I = 5 V		30	65	
I_O	Output current	T_A = 25°C	5	12		mA
I_{OZ}	Off-state output current	V_O = ±30 V, T_A = 25°C		±2	±100	µA
I_{CC}	Supply current (all outputs low)	$V_I \geq$ at 2.4 V, I_O = 0		500	1000	µA
$I_{CC(off)}$	Off-state supply current	ON/$\overline{OFF}$ at 0.4 V			10	µA
		ON/$\overline{OFF}$ at 0.1 V		10	150	

operating characteristics, $V_{CC\pm}$ = ±5 V to ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
SR	Driver slew rate	R_L = 3 kΩ, C_L = 51 pF	4	15	30	V/µs

†All typical values are at $V_{CC\pm}$ = ±12 V, T_A = 25°C.

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE SWING
vs
OUTPUT CURRENT

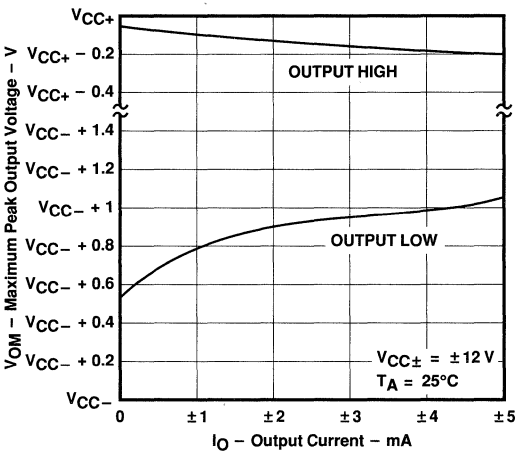

FIGURE 1

ON/$\overline{\text{OFF}}$ TERMINAL VOLTAGE
vs
FREE-AIR TEMPERATURE

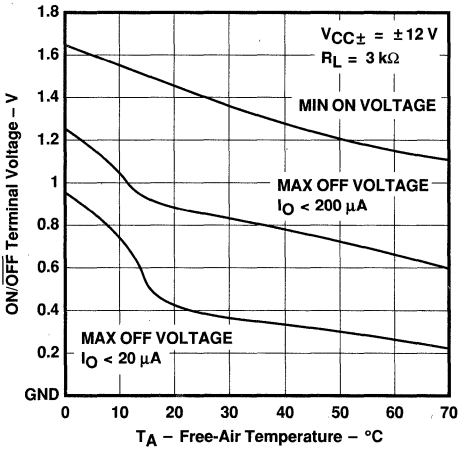

FIGURE 2

MAXIMUM PEAK OUTPUT VOLTAGE SWING
vs
FREE-AIR TEMPERATURE

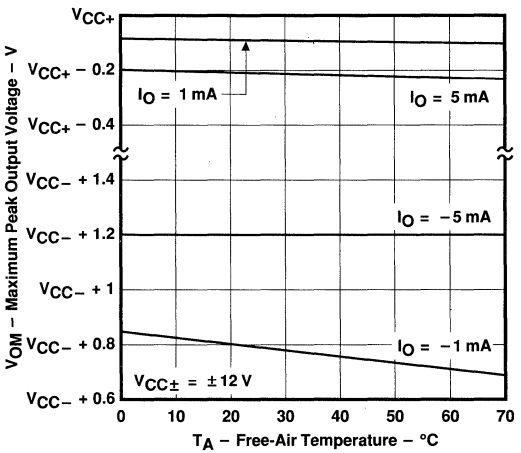

FIGURE 3

ON/$\overline{\text{OFF}}$ TERMINAL CURRENT
vs
ON/$\overline{\text{OFF}}$ TERMINAL VOLTAGE

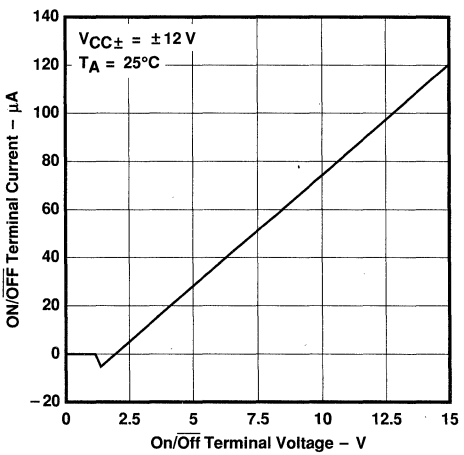

FIGURE 4

TYPICAL CHARACTERISTICS

OUTPUT CURRENT LIMIT
vs
FREE-AIR TEMPERATURE

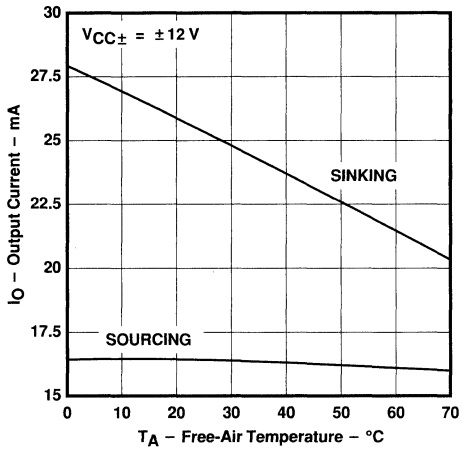

FIGURE 5

OFF-STATE OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

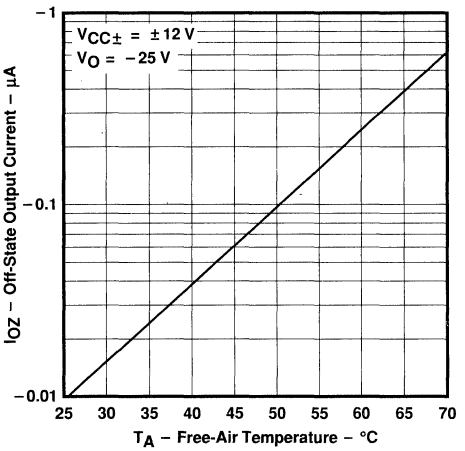

FIGURE 6

OFF-STATE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

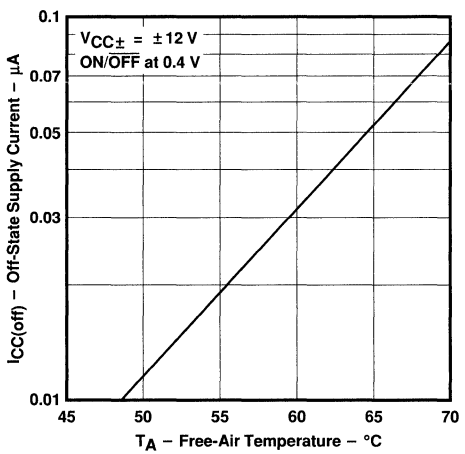

FIGURE 7

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

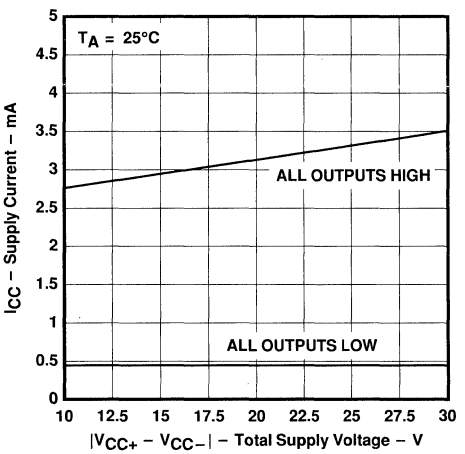

FIGURE 8

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

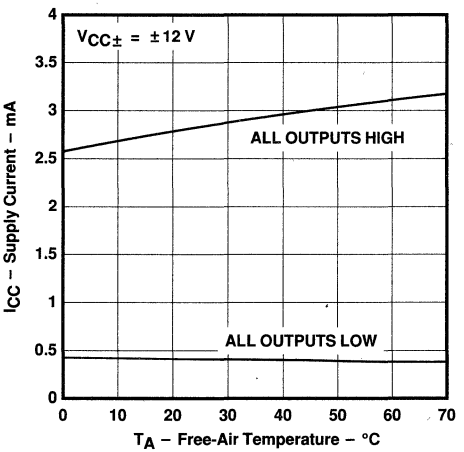

FIGURE 9

SLEW RATE
vs
FREE-AIR TEMPERATURE

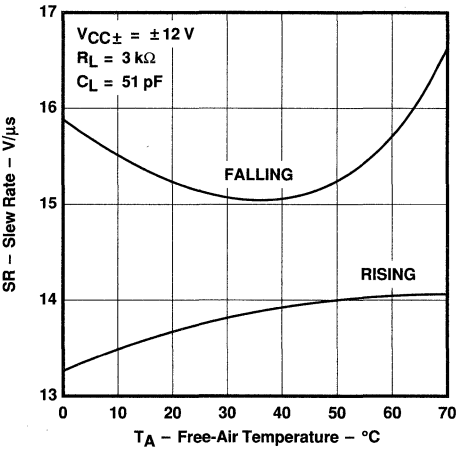

FIGURE 10

TYPICAL APPLICATION DATA

forward biasing the substrate

As with other bipolar integrated circuits, forward biasing the substrate diode can cause problems. The LT1030 will draw high current from V_{CC+} to ground if the V_{CC-} terminal is open-circuited or pulled above ground. If this is possible, connecting a diode from V_{CC-} to ground will prevent the high-current state. Any low-cost diode can be used (see Figure 11).

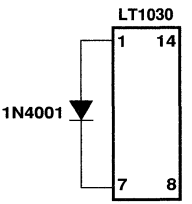

FIGURE 11. CONNECTING A DIODE FROM V_{CC-} TO GROUND

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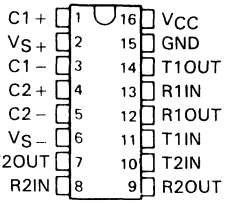
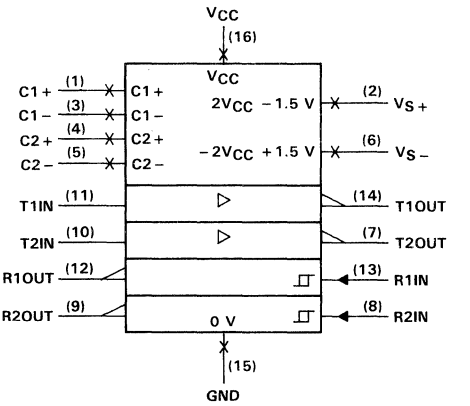
D3120, FEBRUARY 1989—REVISED JUNE 1989

- **Operates with Single 5-V Power Supply**
- **LinBiCMOS™ Process Technology**
- **Two Drivers and Two Receivers**
- **±30-V Input Levels**
- **Low Supply Current . . . 8 mA Typ**
- **Meets ANSI/EIA-232-D-1986 Specifications (Revision of EIA Standard RS-232-C)**
- **Designed to be Interchangeable with Maxim MAX232**
- **Applications**
  - **EIA-232 Interface**
  - **Battery-Powered Systems**
  - **Terminals**
  - **Modems**
  - **Computers**

D OR N PACKAGE
(TOP VIEW)



logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The MAX232 is a dual driver/receiver that includes a capacitive voltage generator to supply EIA-232 voltage levels from a single 5-V supply. Each receiver converts EIA-232 inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V and a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into EIA-232 levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Input supply voltage, V_{CC} (see Note 1) . . . . . −0.3 V to 6 V
Positive output supply voltage, V_{S+} . . . . . V_{CC} −0.3 V to 15 V
Negative output supply voltage, V_{S-} . . . . . 0.3 V to −15 V
Input voltage range: Driver . . . . . −0.3 V to V_{CC} + 0.3 V
Receiver . . . . . ±30 V
Output voltage range: T1OUT, T2OUT . . . . . V_{S-} − 0.3 V to V_{S+} + 0.3 V
R1OUT, R2OUT . . . . . −0.3 V to V_{CC} + 0.3 V
Short-circuit duration: V_{S+} . . . . . 30 s
V_{S-} . . . . . 30 s
T1OUT, T2OUT . . . . . unlimited
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH} (T1IN, T2IN)	2			V
Low-level input voltage, V_{IL} (T1IN, T2IN)			0.8	V
Receiver input voltage, R1IN, R2IN			±30	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	T1OUT, T2OUT	R_L = 3 kΩ to GND	5	7		V
		R1OUT, R2OUT	I_{OH} = −1 mA	3.5			
V_{OL}	Low-level output voltage‡	T1OUT, T2OUT	R_L = 3 kΩ to GND		−7	−5	V
		R1OUT, R2OUT	I_{OL} = 3.2 mA			0.4	
V_{T+}	Receiver positive-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V, T_A = 25°C		1.7	2.4	V
V_{T-}	Receiver negative-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V, T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis	R1IN, R2IN	V_{CC} = 5 V	0.2	0.5	1	kΩ
r_i	Receiver input resistance	R1IN, R2IN	V_{CC} = 5 V, T_A = 25°C	3	5	7	kΩ
r_o	Output resistance	T1OUT, T2OUT	V_{S+} = V_{S-} = 0, V_O = ±2 V	300			Ω
I_{OS}§	Short-circuit output current	T1OUT, T2OUT	V_{CC} = 5.5 V, V_O = 0		±10		mA
I_{IS}	Short-circuit input current	T1IN, T2IN	V_I = 0			200	μA
I_{CC}	Supply current		V_{CC} = 5.5 V, All outputs open, T_A = 25°C		8	10	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(R)}$	Receiver propagation delay time, low-to-high-level output	See Figure 2		500		ns
$t_{PHL(R)}$	Receiver propagation delay time, high-to-low-level output	See Figure 2		500		ns
SR	Driver slew rate	R_L = 3 kΩ to 7 kΩ, See Figure 3			30	V/μs
SR(tr)	Driver transition region slew rate	See Figure 4		3		V/μs

TYPICAL APPLICATION DATA

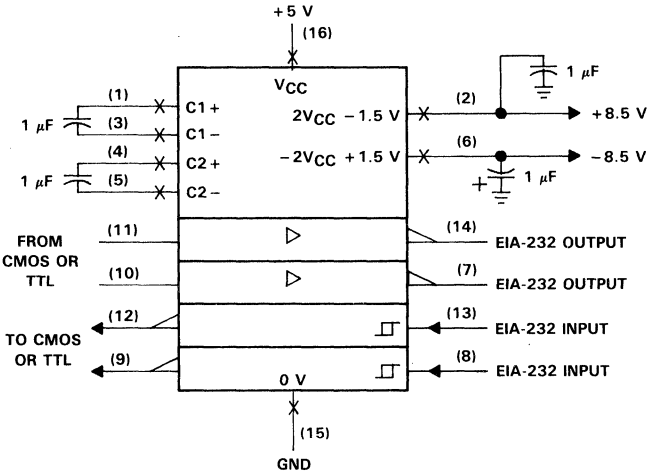
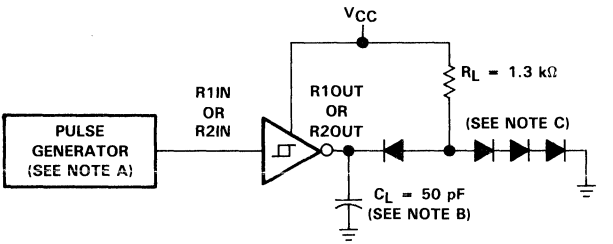
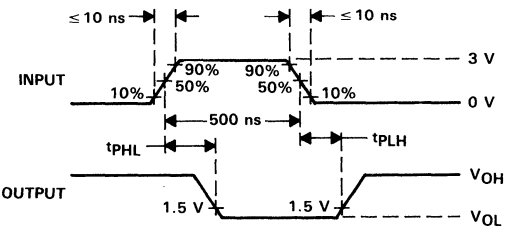


FIGURE 1. TYPICAL OPERATING CIRCUIT

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

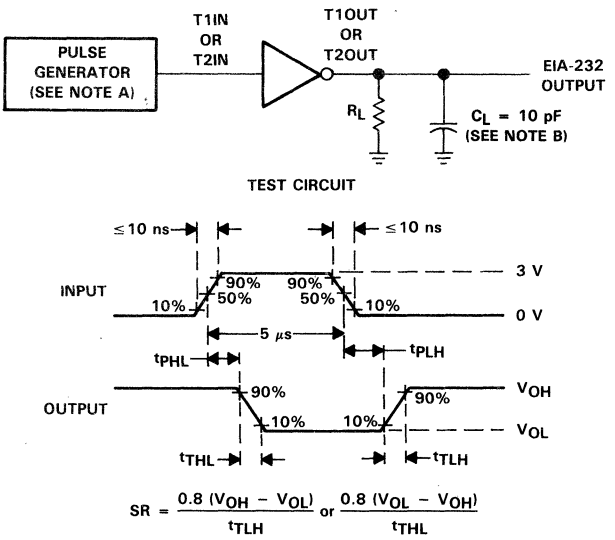


WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, Duty Cycle ≤50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

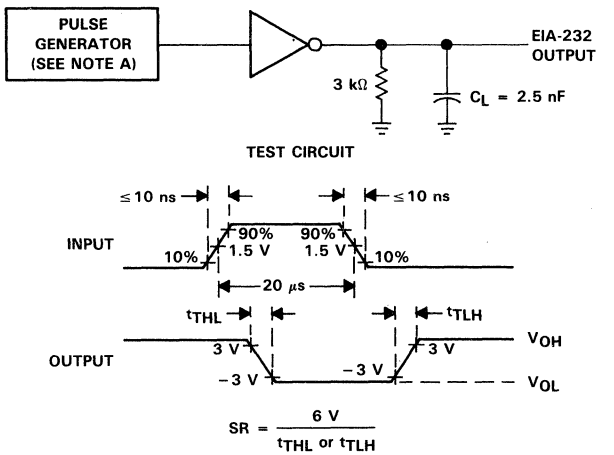
FIGURE 2. RECEIVER TEST CIRCUIT AND WAVEFORMS FOR t_{PHL} AND t_{PLH} MEASUREMENT

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, Duty Cycle ≤50%.
B. C_L includes probe and jig capacitance.

FIGURE 3. DRIVER TEST CIRCUIT AND WAVEFORMS FOR t_{PHL} AND t_{PLH} MEASUREMENT (5-μs INPUT)



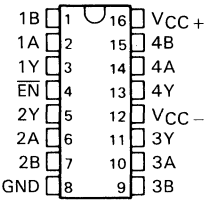
NOTE A: The pulse generator has the following characteristics: Z_{OUT} = 50 Ω, Duty Cycle ≤50%

FIGURE 4. TEST CIRCUIT AND WAVEFORMS FOR t_{THL} AND t_{TLH} MEASUREMENT (20-μs INPUT)

D3006, FEBRUARY 1986—REVISED OCTOBER 1986

- **Four Independent Receivers with Common Enable Input**
- **High Input Sensitivity . . . 25 mV Max**
- **High Input Impedance**
- **MC3450 has Three-State Outputs**
- **MC3452 has Open-Collector Outputs**
- **Glitch-Free Power-Up/Power-Down Operation**

D, J, OR N PACKAGE
(TOP VIEW)



description

The MC3450 and MC3452 are quadruple differential line receivers designed for use in balanced and unbalanced digital data transmission. The MC3450 and MC3452 are the same except that the MC3450 has three-state ouputs whereas the MC3452 has open-collector outputs, which permit the wire-AND function with similar output devices. Three-state and open-collector outputs permit connection directly to a bus-organized system.

The MC3450 and MC3452 are designed for optimum performance when used with either the MC3453 quadruple differential line driver or SN75109A, SN75110A, and SN75112 dual differential drivers.

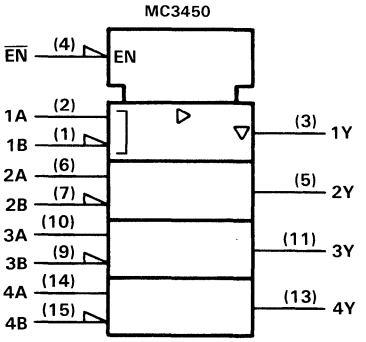
The MC3450 and MC3452 are characterized for operation from 0°C to 70°C.

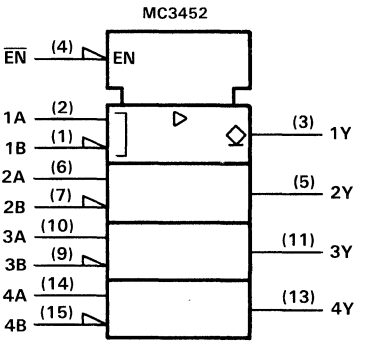
FUNCTION TABLE

DIFFERENTIAL INPUTS A-B	ENABLE $\overline{EN}$	OUTPUT Y
$V_{ID} \geq 25$ mV	L	H
-25 mV $< V_{ID} <$ 25 mV	L	?
$V_{ID} \leq 25$ mV	L	L
X	H	Z

H = high level, L = low level, ? = indeterminate, Z = impedance (off)

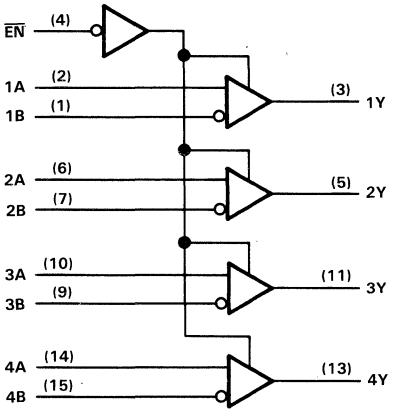
logic symbols†



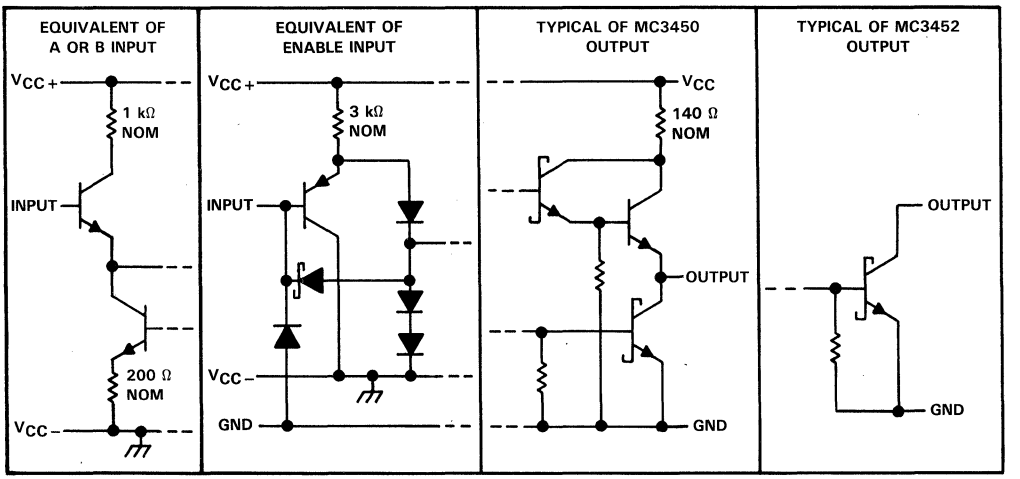


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 7 V
Supply voltage, V_{CC-} . . . . . −7 V
Differential input voltage (see Note 2) . . . . . ±6 V
Common-mode input voltage (see Note 3) . . . . . ±5 V
Enable input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4):
D package . . . . . 950 mW
J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. Common-mode input voltage is the average of the voltages at the A and B inputs.
4. For operation above 25°C free-air temperature, derate the D package to 608 mW at 70°C at the rate of 7.6 mW/°C, the J package to 656 mW at 70°C at the rate of 8.2 mW/°C, and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, MC3450 and MC3452 chips are glass mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4.75	5	5.25	V
Supply voltage, V_{CC-}	−4.75	−5	−5.25	V
High-level enable input voltage, V_{IH}	2			V
Low-level enable input voltage, V_{IL}			0.8	V
Low-level output current, I_{OL}			−16	mA
Differential input voltage, V_{ID} (see Note 5)	−5†		5	V
Common-mode input voltage, V_{IC} (see Note 5)	−3†		3	V
Input voltage range, any differential input to ground	−5†		3	V
Operating free-air temperature, T_A	0		70	°C

† The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage.
NOTE 5: The recommended combinations of input voltages fall within the shaded area of Figure 1.

RECOMMENDED COMBINATIONS OF INPUT VOLTAGES

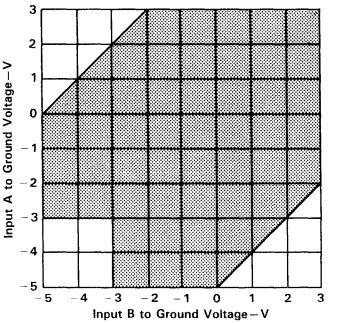


FIGURE 1

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±5.25 V (unless otherwise noted)

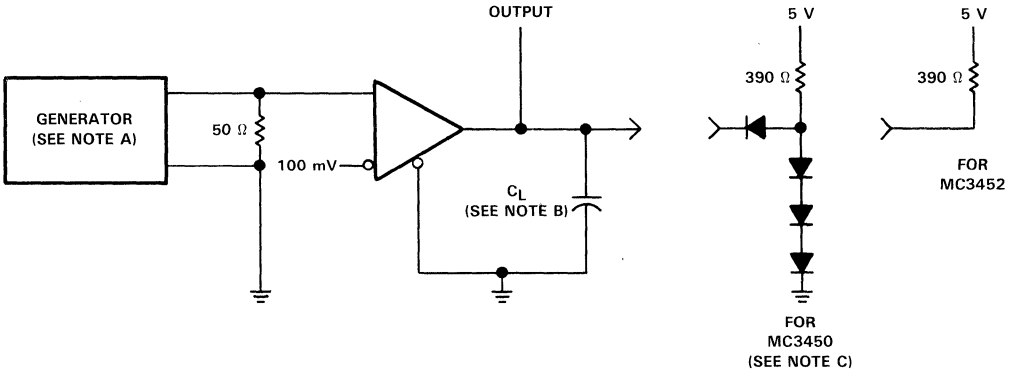
PARAMETER			TEST CONDITIONS	MC3450			MC3452			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{IH}	High-level input current	A inputs	V_{ID} = −2 V		30	75		30	75	μA
		B inputs	V_{ID} = −2 V		30	75		30	75	μA
		$\overline{EN}$	V_{IH} = 2.4 V			40			40	μA
			V_{IH} = 5.25 V			1			1	mA
I_{IL}	Low-level input current	A inputs	V_{ID} = 2 V			−10			−10	μA
		B inputs	V_{ID} = 2 V			−10			−10	μA
		$\overline{EN}$	V_{IL} = 0.4 V			−1.6			−1.6	mA
V_{OH}	High-level output voltage		$V_{CC\pm}$ = ±4.75 V, V_{ID} = 25 mV, $\overline{EN}$ at 0.8 V, I_{OH} = −400 μA, V_{IC} = −3 V to 3 V	2.4						V
I_{OH}	High-level output current		$V_{CC\pm}$ = ±4.75 V, V_{OH} = 5.25 V						250	μA
V_{OL}	Low-level output voltage		$V_{CC\pm}$ = ±4.75 V, V_{ID} = −25 mV, $\overline{EN}$ at 2 V, I_{OL} = 16 mA, V_{IC} = −3 V to 3 V			0.5			0.5	V
I_{OZ}	High-impedance-state output current		V_O = 2.4 V			40				μA
			V_O = 0.4 V			−40				μA
I_{OS}	Short-circuit output current‡		V_{ID} = 25 mV, V_O = 0, $\overline{EN}$ at 0.8 V	−18		−70				mA
I_{CCH+}	Supply current from V_{CC+}, outputs high					60			60	mA
I_{CCH-}	Supply current from V_{CC-}, outputs high					−30			−30	mA

† All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.
‡ Not more one output should be shorted at a time.

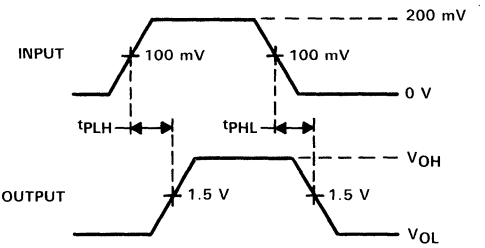
switching characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MC3450			MC3452			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A and B	Y	C_L = 50 pF, See Figure 2		17	25				ns
			C_L = 15 pF, See Figure 2					19	25	ns
t_{PHL}	A and B	Y	C_L = 50 pF, See Figure 2		17	25				ns
			C_L = 15 pF, See Figure 2					19	25	ns
t_{PZH}	$\overline{EN}$	Y	C_L = 50 pF, See Figure 2			21				ns
t_{PZL}	$\overline{EN}$	Y				27				ns
t_{PHZ}	$\overline{EN}$	Y	C_L = 15 pF, See Figure 3			18				ns
t_{PLZ}	$\overline{EN}$	Y				29				ns
t_{PLH}	$\overline{EN}$	Y	C_L = 15 pF, See Figure 4						25	ns
t_{PHL}	$\overline{EN}$	Y	C_L = 15 pF, See Figure 4						25	ns

† All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.



TEST CIRCUIT

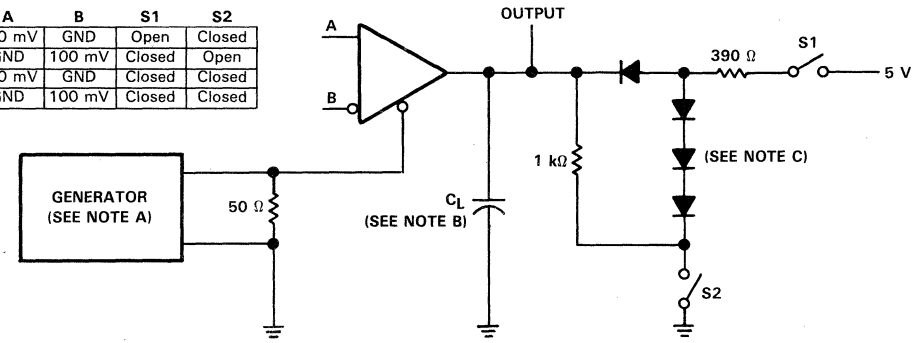


VOLTAGE WAVEFORMS

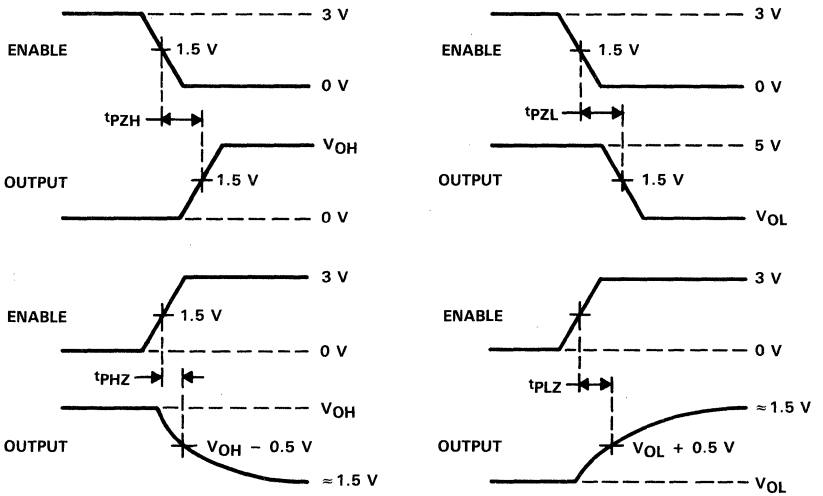
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

FIGURE 2. PROPAGATION DELAY TIMES

	A	B	S1	S2
t_{PZH}	100 mV	GND	Open	Closed
t_{PZL}	GND	100 mV	Closed	Open
t_{PHZ}	100 mV	GND	Closed	Closed
t_{PLZ}	GND	100 mV	Closed	Closed



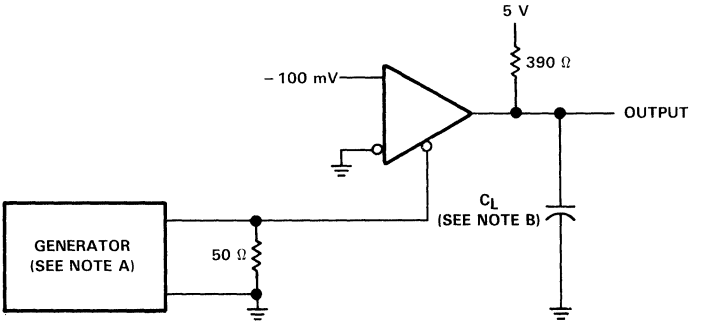
TEST CIRCUIT



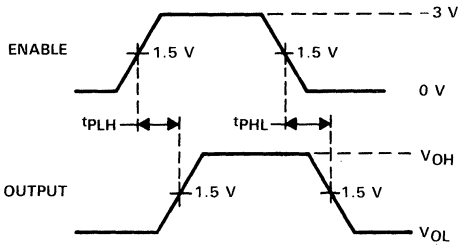
VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

FIGURE 3. MC3450 ENABLE AND DISABLE TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

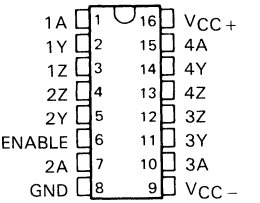
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

FIGURE 4. MC3452 PROPAGATION DELAY TIMES FROM ENABLE

D3000, FEBRUARY 1986—REVISED JULY 1990

- **Similar to a Dual Version of SN75110A Line Driver**
- **Improved Stability Over Supply Voltage and Temperature Ranges**
- **Constant-Current Outputs**
- **High Output Impedance**
- **High Common-Mode Output Voltage Range (−3 V to 10 V)**
- **Glitch-Free Power-Up/Power-Down Operation**
- **TTL Input Compatibility**
- **Common Enable Circuit**
- **Designed to be Interchangeable with Motorola MC3453**

D, J, OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



FUNCTION TABLE

LOGIC INPUT	ENABLE INPUT	OUTPUT CURRENT Z	OUTPUT CURRENT Y
H	H	ON	OFF
L	H	OFF	ON
H	L	OFF	OFF
L	L	OFF	OFF

L = low logic level
H = high logic level

description

The MC3453 features four line drivers with a common enable input. When the enable input is high, a constant output current is switched between each pair of output terminals in response to the logic level at that channel's input. When the enable is low, all channel outputs are nonconductive (transistors biased to cutoff). This minimizes loading in party-line systems where a large number of drivers share the same line.

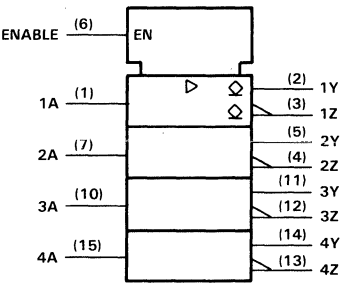
The driver outputs have a common-mode voltage range of −3 volts to 10 volts, allowing common-mode voltages on the line without affecting driver performance.

All outputs should be maintained within the recommended common-mode output voltage range to ensure that the channels do not interact with each other. To minimize power dissipation, all unused outputs should be grounded.

All inputs are diode clamped and are designed to satisfy TTL-system requirements. The inputs are tested at 2 volts for high-logic-level input conditions and 0.8 volt for low-logic-level input conditions. These tests guarantee 400 millivolts of noise margin when interfaced with Series 54/74 TTL.

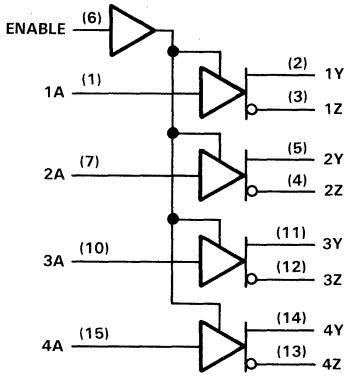
The MC3453 is characterized for operation from 0°C to 70°C.

logic symbol†

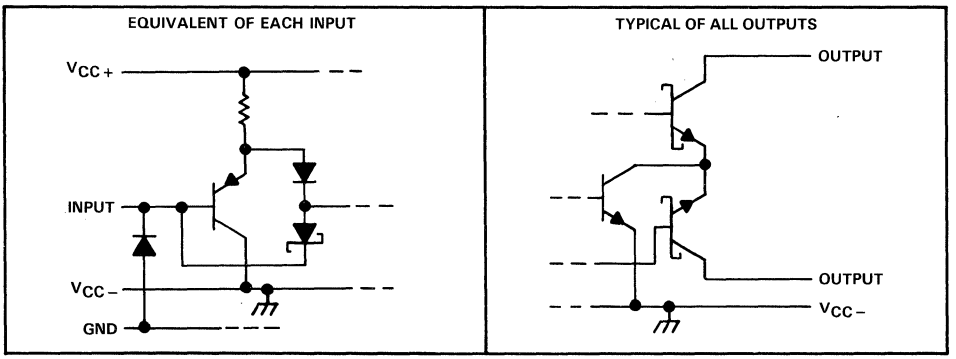


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 7 V
Supply voltage, V_{CC-} . . . . . −7 V
Input voltage (any input) . . . . . 5.5 V
Output voltage range (any output) . . . . . −5 V to 12 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
D package . . . . . 950 mW
J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the D package to 608 mW at 70°C at the rate of 7.6 mW/°C, derate the J package to 656 mW at 70°C at the rate of 8.2 mW/°C, and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package the MC3453 is glass mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}		4.75	5	5.25	V
Supply voltage, V_{CC-}		−4.75	−5	−5.25	V
High-level input voltage, V_{IH}		2		5.5	V
Low-level input voltage, V_{IL}		0		0.8	V
Common-mode output voltage range	V_{OCR+}	0		10	V
	V_{OCR-}	0		−3	V
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5.25 V, V_{CC-} = −5.25 V (unless otherwise noted)

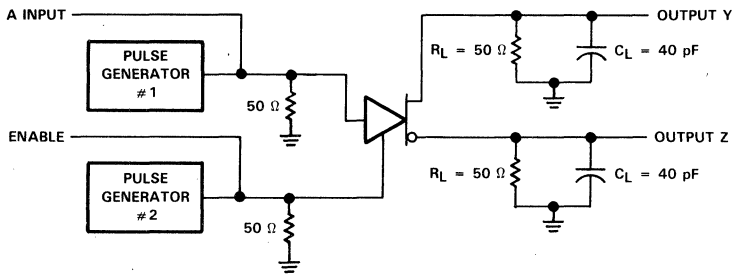
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −12 mA			−0.9	−1.5	V
$I_{O(on)}$	On-state output current	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V			11	15	mA
		V_{CC+} = 4.75 V, V_{CC-} = −4.75 V		6.5	11		
$I_{O(off)}$	Off-state output current	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, V_O = 10 V				100	μA
I_{IH}	High-level input current	V_I = 2.4 V				40	μA
		V_I = 5.25 V				1	mA
I_{IL}	Low-level input current	V_I = 0.4 V				−1.6	mA
I_{CC+}	Supply current from V_{CC+}	A inputs at 0.4 V	Enable at 2 V		33	50	mA
			Enable at 0.4 V		33	50	
I_{CC-}	Supply current from V_{CC-}	A inputs at 0.4 V	Enable at 2 V		−68	−90	mA
			Enable at 0.4 V		−31	−40	

†All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, and T_A = 25°C.

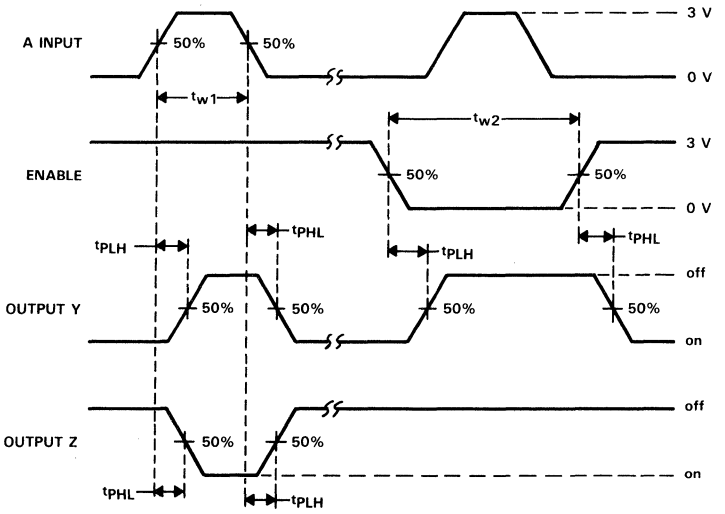
switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, R_L = 50 Ω, C_L = 40 pF, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y or Z	See Figure 1		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output	A	Y or Z			7	15	ns
t_{PLH}	Propagation delay time, low-to-high-level output	Enable	Y or Z			14	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output	Enable	Y or Z			15	25	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

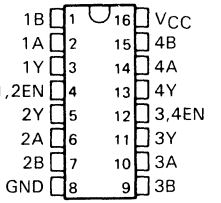
NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, $t_r = t_f$ = 10 ±5 ns, t_{W1} = 200 ns, PRR ≤ 1 MHz, t_{W2} = 1 μs, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

FIGURE 1. PROPAGATION DELAY TIMES

D2434, JUNE 1980—REVISED SEPTEMBER 1986

- **Meets EIA Standards RS-422-A and RS423-A and Federal Standards 1020 and 1030**
- **3-State, TTL-Compatible Outputs**
- **Fast Transition Times**
- **Operates from Single 5-V Supply**
- **Designed to be Interchangeable with Motorola MC3486**

D, J OR N PACKAGE
(TOP VIEW)



description

The MC3486 is a monolithic quadruple differential line receiver designed to meet the specifications of EIA Standards RS-422-A and RS-423-A and Federal Standards 1020 and 1030. The MC3486 offers four independent differential-input line receivers that have TTL-compatible outputs. The outputs utilize 3-state circuitry to provide a high-impedance state at any output when the appropriate output enable is at a low logic level.

The MC3486 is designed for optimum performance when used with the MC3487 quadruple differential line driver. It is supplied in a 16-pin package and operates from a single 5-V supply.

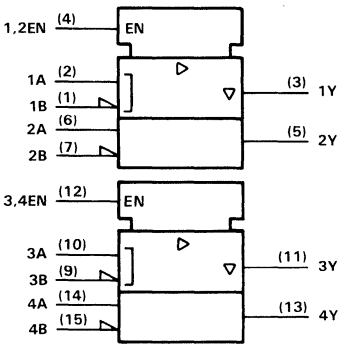
The MC3486 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUTS A-B	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
Irrelevant	L	Z

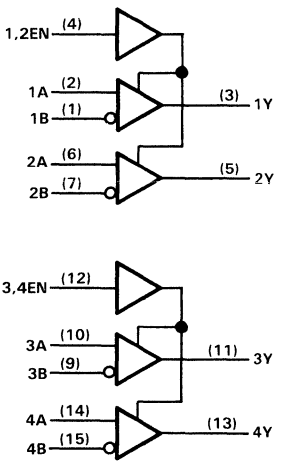
H = high level, L = low level, Z = high-impedance (off), ? = indeterminate

logic symbol†

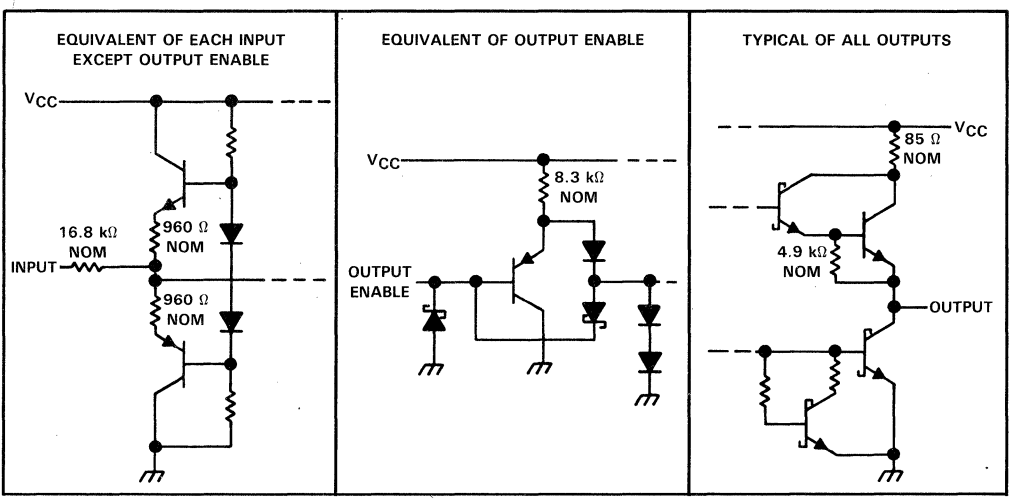


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage, A or B inputs . . . . . ±15 V
Differential input voltage (see Note 2) . . . . . ±25 V
Enable input voltage . . . . . 8 V
Low-level output current . . . . . 50 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltage values, except differential-input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Differential input voltage, V_{ID}			±6	V
High-level enable input voltage, V_{IH}	2			V
Low-level enable input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V, I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V, I_O = 8 mA		−0.2†		V
V_{IK}	Enable-input clamp voltage	I_I = −10 mA			−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 0.4 V, I_O = −0.4 mA, See Note 3 and Figure 1		2.7		V
V_{OL}	Low-level output voltage	V_{ID} = −0.4 V, I_O = 8 mA, See Note 3 and Figure 1			0.5	V
I_{OZ}	High-impedance-state output current	V_{IL} = 0.8 V, V_{ID} = −3 V, V_O = 2.7 V			40	μA
		V_{IL} = 0.8 V, V_{ID} = 3 V, V_O = 0.5 V			−40	
I_{IB}	Differential-input bias current	V_{CC} = 0 V or 5.25 V, Other inputs at 0 V	V_I = −10 V		−3.25	mA
			V_I = −3 V		−1.5	
			V_I = 3 V		1.5	
			V_I = 10 V		3.25	
I_{IH}	High-level enable input current	V_I = 5.25 V			100	μA
		V_I = 2.7 V			20	
I_{IL}	Low-level enable input current	V_I = 0.5 V			−100	μA
I_{OS}	Short-circuit output current	V_{ID} = 3 V, V_O = 0, See Note 4		−15	−100	mA
I_{CC}	Supply current	V_{IL} = 0			85	mA

†The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

NOTES: 3. Refer to EIA Standards RS-422-A and RS-423-A for exact conditions.
4. Only one output at a time should be shorted.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, See Figure 2		28	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output			27	30	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 3		13	30	ns
t_{PZL}	Output enable time to low level			20	30	ns
t_{PHZ}	Output disable time from high level			26	35	ns
t_{PLZ}	Output disable time from low level			27	35	ns

PARAMETER MEASUREMENT INFORMATION

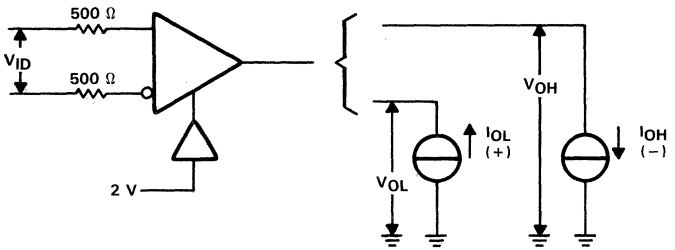
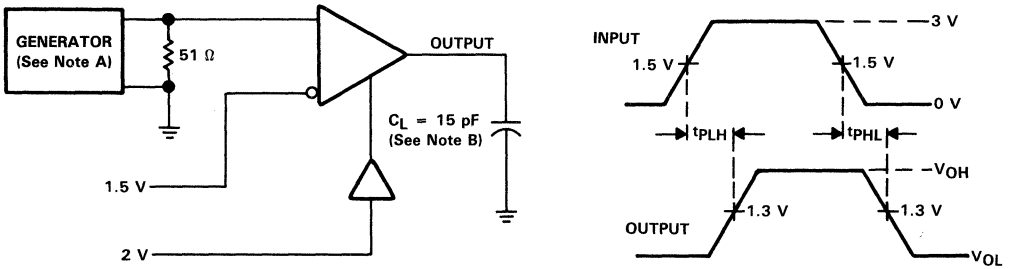


FIGURE 1. V_{OH}, V_{OL}



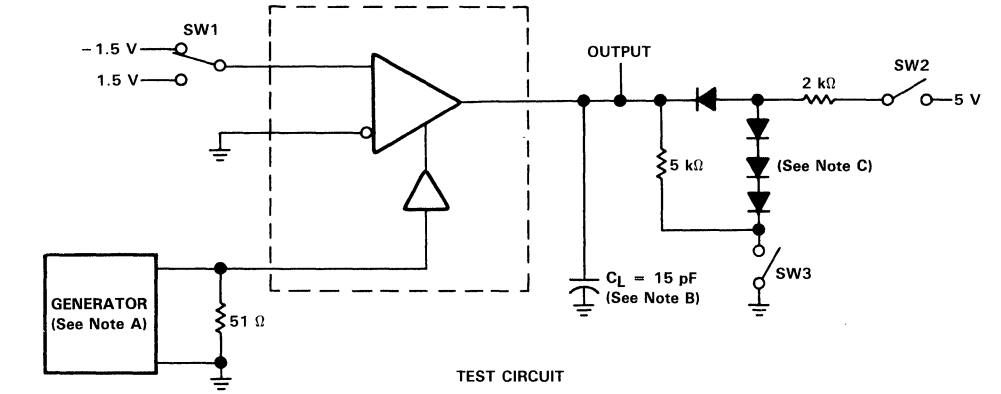
TEST CIRCUIT

VOLTAGE WAVEFORMS

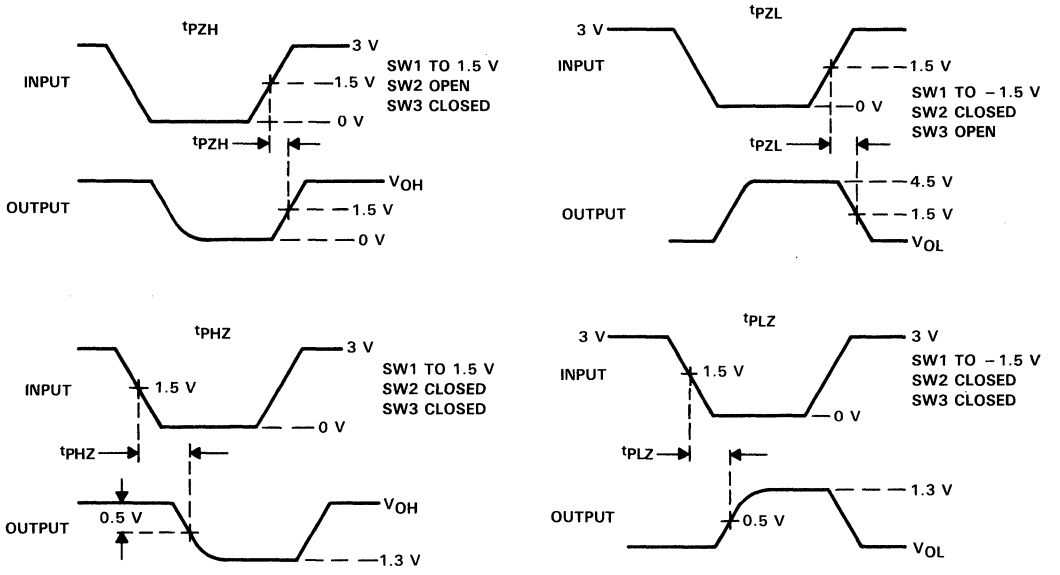
FIGURE 2. PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≈ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and stray capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

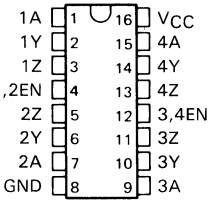
FIGURE 3. ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≈ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or equivalent.

D2578, MAY 1980—REVISED SEPTEMBER 1986

- **Meets EIA Standard RS-422-A and Federal Standard 1020**
- **3-State, TTL-Compatible Outputs**
- **Fast Transition Times**
- **High-Impedance Inputs**
- **Single 5-V Supply**
- **Power-Up and Power-Down Protection**
- **Designed to Be Interchangeable with Motorola MC3487**

D, J, OR N PACKAGE
(TOP VIEW)



description

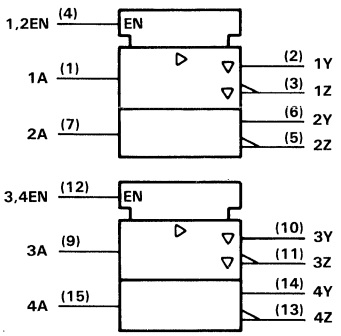
The MC3487 offers four independent differential line drivers designed to meet the specifications of EIA Standard RS-422-A and Federal Standard 1020. Each driver has a TTL-compatible input buffered to reduce current and minimize loading.

The driver outputs utilize 3-state circuitry to provide high-impedance states at any pair of differential outputs when the appropriate output enable is at a low logic level. Internal circuitry is provided to ensure a high-impedance state at the differential outputs during power-up and power-down transition times, provided the output enable is low. The outputs are capable of source or sink currents of 48 mA.

The MC3487 is designed for optimum performance when used with the MC3486 quadruple line receiver. It is supplied in a 16-pin dual-in-line package and operates from a single 5-V supply.

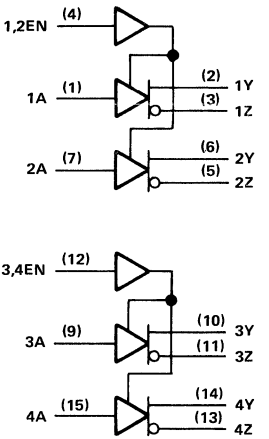
The MC3487 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

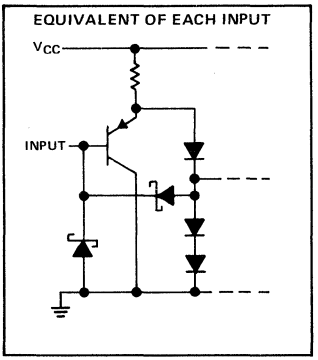


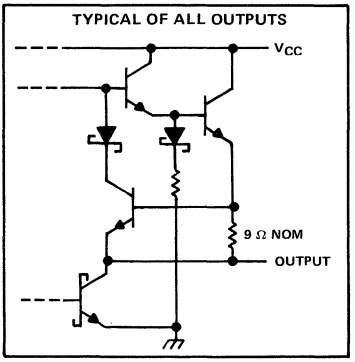
FUNCTION TABLE (EACH DRIVER)

INPUT	OUTPUT ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	High-Impedance	High-Impedance

H = TTL high level X = irrelevant
L = TTL low level

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage . . . . . 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N packages . . . . . 260°C

NOTE 1: All voltage values, except differential output voltage, V_{OD}, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	V_{IH} = 2 V,	I_{OH} = −20 mA	2.5		V
V_{OL}	Low-level output voltage	V_{IL} = 0.8 V,	V_{IH} = 2 V,	I_{OL} = 48 mA		0.5	V
$\lvert V_{OD}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1		2		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage†	R_L = 100 Ω,	See Figure 1			±0.4	V
V_{OC}	Common-mode output voltage‡	R_L = 100 Ω,	See Figure 1			3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage†	R_L = 100 Ω,	See Figure 1			±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			100	μA
			V_O = −0.25 V			−100	
I_{OZ}	High-impedance-state output current	Output enables at 0.8 V	V_O = 2.7 V			100	
			V_O = 0.5 V			−100	
I_I	Input current at maximum input voltage	V_I = 5.5 V				100	μA
I_{IH}	High-level input current	V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_I = 0.5 V				−400	μA
I_{OS}	Short-circuit output current§	V_I = 2 V			−40	−140	mA
I_{CC}	Supply current (all drivers)	Outputs disabled				105	mA
		Outputs enabled,	No load			85	

†$\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
‡In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
§Only one output at a time should be shorted and duration of the short-circuit should not exceed one second.

switching characteristics over recommended range of operating free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITION	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 2		20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			20	ns
	Skew			6	ns
t_{TD}	Differential-output transition time	C_L = 15 pF, See Figure 3		20	ns
t_{PZH}	Output enable time to high level	C_L = 50 pF, See Figure 4		30	ns
t_{PZL}	Output enable time to low level			30	ns
t_{PHZ}	Output disable time from high level			25	ns
t_{PLZ}	Output disable time from low level			30	ns

PARAMETER MEASUREMENT INFORMATION

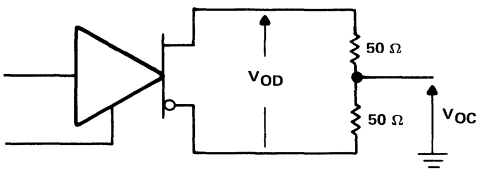


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES

PARAMETER MEASUREMENT INFORMATION

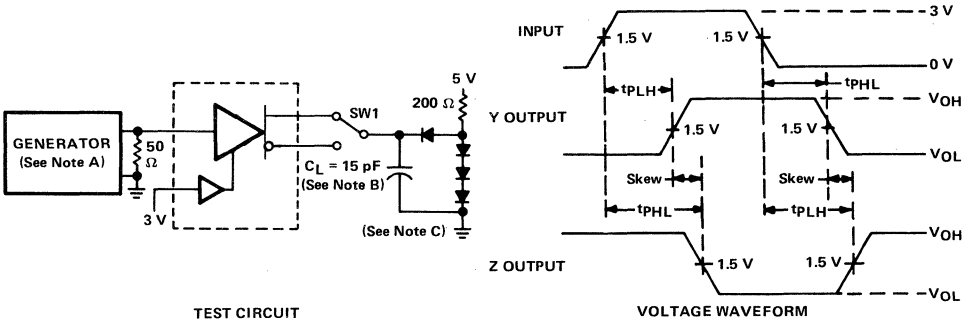


FIGURE 2. PROPAGATION DELAY TIMES

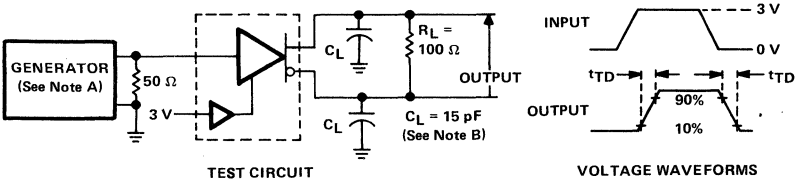


FIGURE 3. DIFFERENTIAL-OUTPUT TRANSITION TIMES

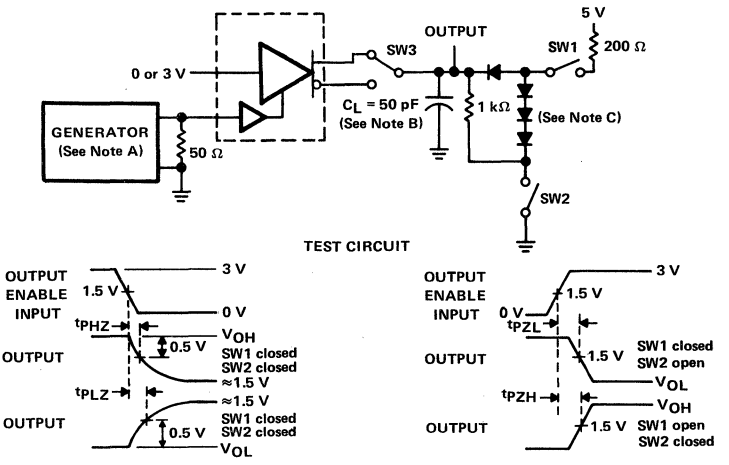


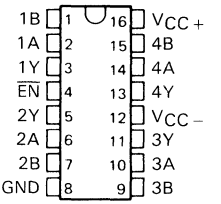
FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_o = 50\ \Omega$.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

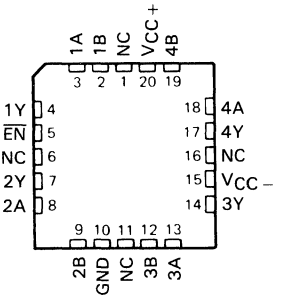
D3171, FEBRUARY 1989

- **Four Independent Receivers with Common Enable Input**
- **High Input Sensitivity . . . 25 mV Max**
- **High Input Impedance**
- **MC3550 has Three-State Outputs**
- **MC3552 has Open-Collector Outputs**
- **Glitch-Free Power-Up/Power-Down Operation**
- **Military-Temperature-Range Versions of MC3450 and MC3452**

J PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The MC3550 and MC3552 are quadruple differential line receivers designed for use in balanced and unbalanced digital data transmission. The two devices are the same except that the MC3550 has three-state outputs whereas the MC3552 has open-collector outputs, which permit the wire-AND function with similar output devices. Three-state and open-collector outputs permit direct connection to a bus-organized system.

The MC3550 and MC3552 are designed for optimum performance when used with either the MC3553 quadruple differential line driver or SN55109A, SN55110A, and SN55112 dual differential drivers.

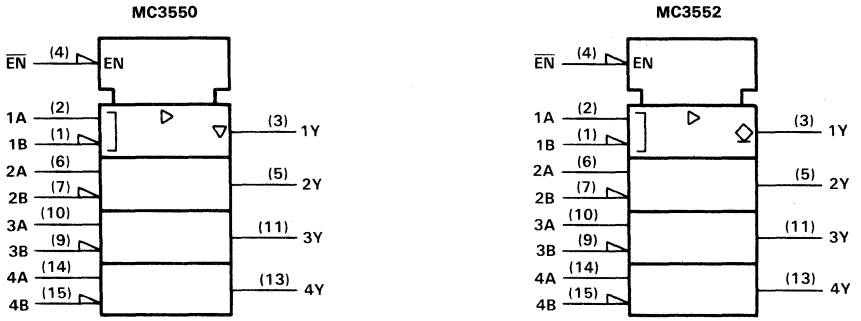
The MC3550 and MC3552 are characterized for operation over the full military temperature range of −55°C to 125°C.

FUNCTION TABLE

DIFFERENTIAL INPUTS A-B	ENABLE $\overline{EN}$	OUTPUT Y
V_{ID} > 25 mV	L	H
−25 mV < V_{ID} < 25 mV	L	?
V_{ID} ≤ 25 mV	L	L
X	H	Z

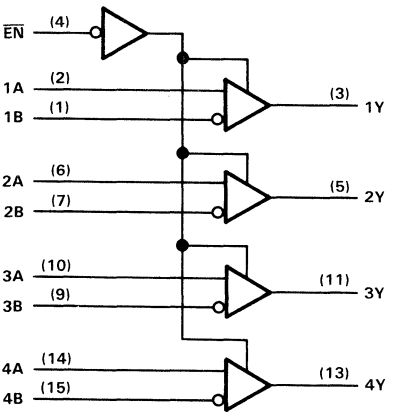
H = high level, L = low level, ? = indeterminate,
Z = impedance (off)

logic symbols†

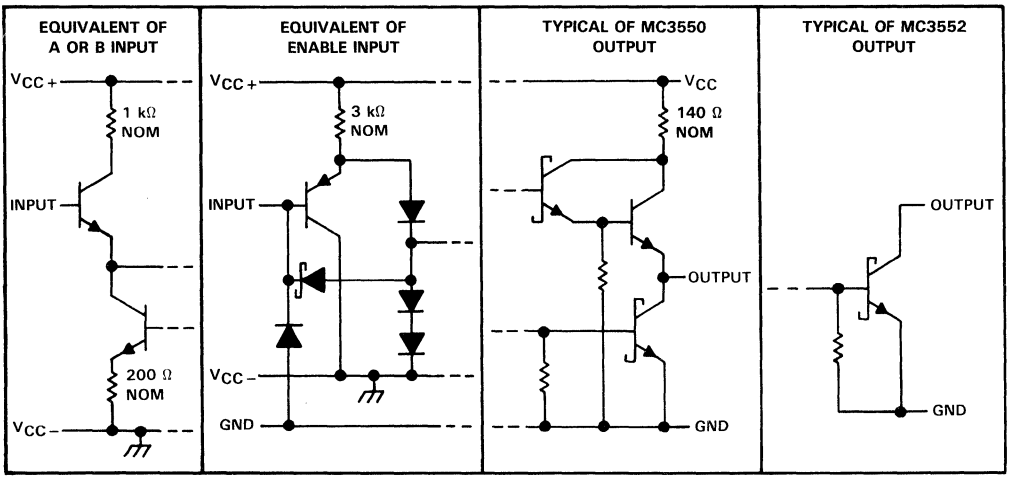


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	7 V
Supply voltage, V_{CC-}	−7 V
Differential input voltage (see Note 2)	±6 V
Common-mode input voltage (see Note 3)	±5 V
Enable input voltage	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4)	1375 mW
Operating free-air temperature range	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. Common-mode input voltage is the average of the voltages at the A and B inputs.
4. For operation above 25°C free-air temperature, derate to 275 mW at 125°C at the rate of 11.0 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	$T_A \geq 25°C$	4.5	5	5.5	V
	$T_A < 25°C$	4.75	5	5.5	
Supply voltage, V_{CC-}	$T_A \geq 25°C$	−4.5	−5	−5.5	V
	$T_A < 25°C$	−4.75	−5	−5.5	
High-level enable input voltage, V_{IH}		2			V
Low-level enable input voltage, V_{IL}				0.8	V
Low-level output current, I_{OL}				−16	mA
Differential input voltage, V_{ID} (see Note 5)		−5†		5	V
Common-mode input voltage, V_{IC} (see Note 5)		−3†		3	V
Input voltage range, any differential input to ground		−5†		3	V
Operating free-air temperature, T_A		−55		125	°C

† The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage.

NOTE 5: The recommended combinations of input voltages fall within the shaded area of Figure 1.

RECOMMENDED COMBINATIONS OF INPUT VOLTAGES

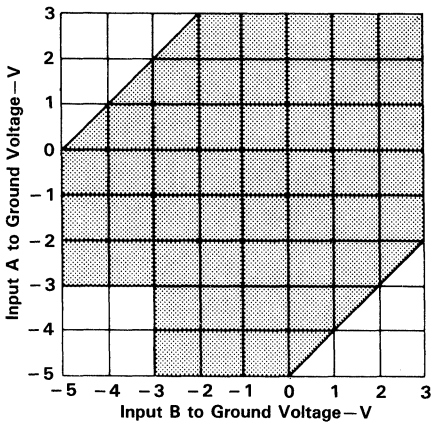


FIGURE 1

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = MAX (unless otherwise noted)

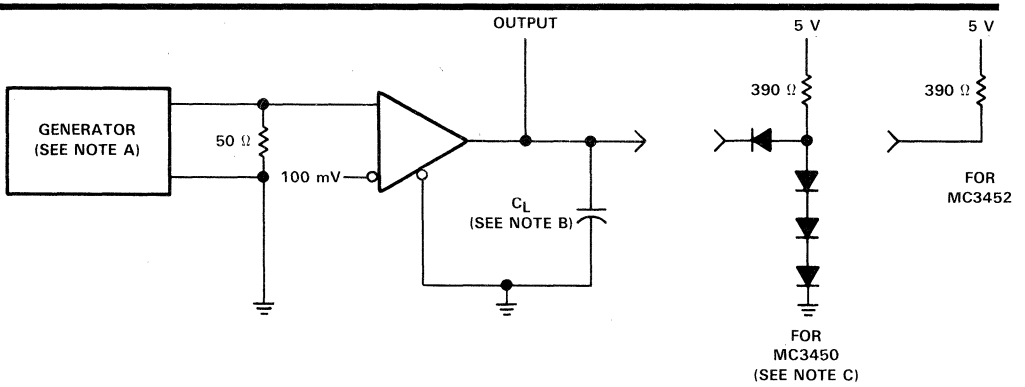
PARAMETER			TEST CONDITIONS†	MC3550			MC3552			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
I_{IH}	High-level input current	A inputs	V_{ID} = −2 V		30	75		30	75	μA
		B inputs	V_{ID} = −2 V		30	75		30	75	μA
		$\overline{EN}$	V_{IH} = 2.4 V			40			40	μA
			V_{IH} = V_{CC+}MAX			1			1	mA
I_{IL}	Low-level input current	A inputs	V_{ID} = 2 V			−10			−10	μA
		B inputs	V_{ID} = 2 V			−10			−10	μA
		$\overline{EN}$	V_{IL} = 0.4 V			−1.6			−1.6	mA
V_{OH}	High-level output voltage		$V_{CC\pm}$ = MIN, V_{ID} = 25 mV, $\overline{EN}$ at 0.8 V, I_{OH} = −400 μA, V_{IC} = −3 V to 3 V	2.4						V
I_{OH}	High-level output current		$V_{CC\pm}$ = MIN, V_{OH} = V_{CC+}MAX						250	μA
V_{OL}	Low-level output voltage		$V_{CC\pm}$ = MIN, V_{ID} = −25 mV, $\overline{EN}$ at 0.8 V, I_{OL} = 16 mA, V_{IC} = −3 V to 3 V			0.5			0.5	V
I_{OZ}	High-impedance-state output current		V_O = 2.4 V			40				μA
			V_O = 0.4 V			−40				μA
I_{OS}	Short-circuit output current§		V_{ID} = 25 mV, V_O = 0, $\overline{EN}$ at 0.8 V	−18		−70				mA
I_{CCH+}	Supply current from V_{CC+}, outputs high		A inputs at GND, B inputs at 3 V, $\overline{EN}$ at 3 V			60			60	mA
I_{CCH-}	Supply current from V_{CC-}, outputs high					−30			−30	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

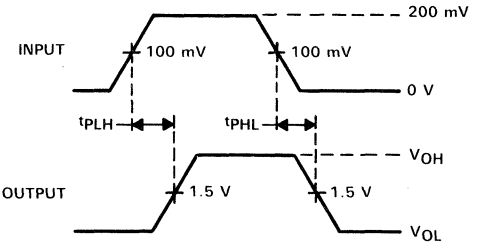
switching characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MC3550			MC3552			UNIT
				MIN	TYP¶	MAX	MIN	TYP¶	MAX	
t_{PLH}	A and B	Y	C_L = 50 pF, See Figure 2		17	25				ns
			C_L = 15 pF, See Figure 2					19	25	ns
t_{PHL}	A and B	Y	C_L = 50 pF, See Figure 2		17	25				ns
			C_L = 15 pF, See Figure 2					19	25	ns
t_{PZH}	$\overline{EN}$	Y	C_L = 50 pF, See Figure 2			21				ns
t_{PZL}	$\overline{EN}$	Y				27				ns
t_{PHZ}	$\overline{EN}$	Y	C_L = 15 pF, See Figure 3			18				ns
t_{PLZ}	$\overline{EN}$	Y				29				ns
t_{PLH}	$\overline{EN}$	Y	C_L = 15 pF, See Figure 4						25	ns
t_{PHL}	$\overline{EN}$	Y	C_L = 15 pF, See Figure 4						25	ns

¶All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.



TEST CIRCUIT

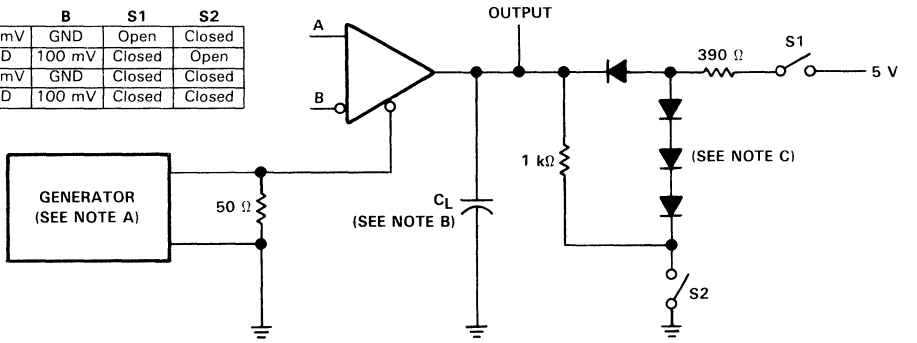


NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

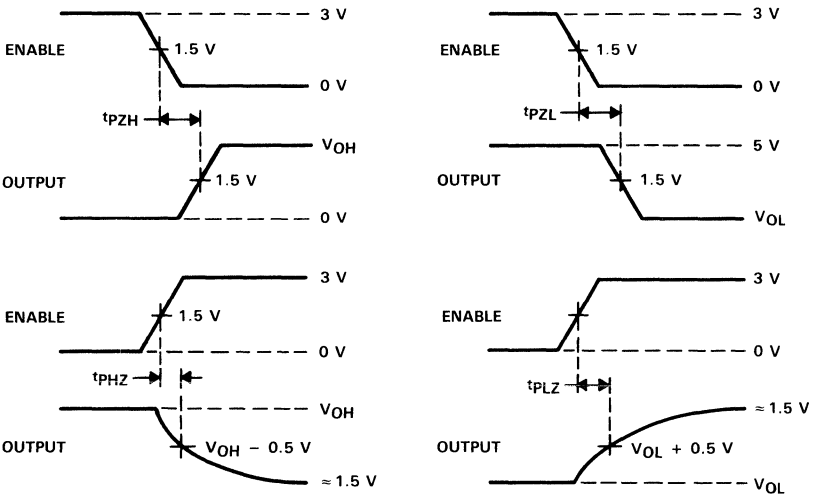
VOLTAGE WAVEFORMS

FIGURE 2. PROPAGATION DELAY TIMES

	A	B	S1	S2
t_{PZH}	100 mV	GND	Open	Closed
t_{PZL}	GND	100 mV	Closed	Open
t_{PHZ}	100 mV	GND	Closed	Closed
t_{PLZ}	GND	100 mV	Closed	Closed



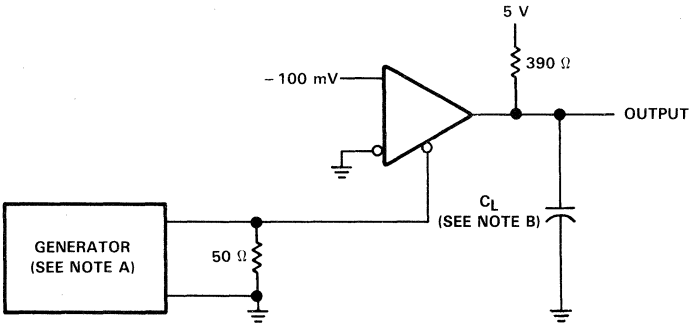
TEST CIRCUIT



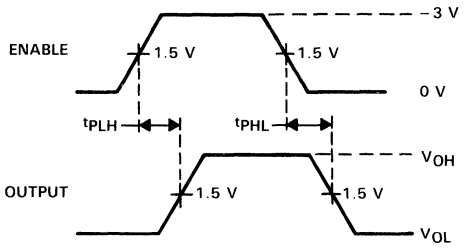
VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

FIGURE 3. MC3550 ENABLE AND DISABLE TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

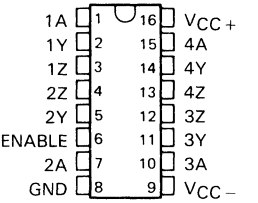
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

FIGURE 4. MC3552 PROPAGATION DELAY TIMES FROM ENABLE

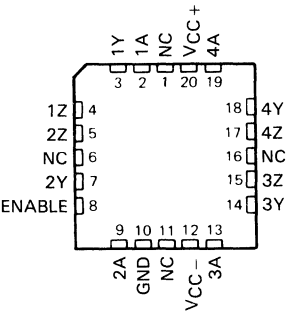
D3170, OCTOBER 1988

- **Similar to a Dual Version of SN55110A Line Driver**
- **Improved Stability Over Supply Voltage and Temperature Ranges**
- **Constant-Current Outputs**
- **High Output Impedance**
- **High Common-Mode Output Voltage Range (−3 V to 10 V)**
- **Glitch-Free Power-Up/Power-Down Operation**
- **TTL Input Compatibility**
- **Common Enable Circuit**
- **Military-Temperature-Range Version of MC3453**

J PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The MC3553 features four line drivers with a common enable input. When the enable input is high, a constant output current is switched between each pair of output terminals in response to the logic level at that channel's input. When the enable is low, all channel outputs are nonconductive (transistors biased to cutoff). This feature minimizes loading in party-line systems where a large number of drivers share the same line.

The driver outputs have a common-mode voltage range of −3 V to 10 V, allowing common-mode voltages on the line without affecting driver performance.

All outputs should be maintained within the recommended common-mode output voltage range to ensure that the channels do not interact with each other. To minimize power dissipation, all unused outputs should be grounded.

All inputs are diode clamped and are designed to satisfy TTL-system requirements. The inputs are tested at 2 V for high-logic-level input conditions and 0.8 V for low-logic-level input conditions. These tests guarantee 400 mV of noise margin when interfaced with Series 54 TTL.

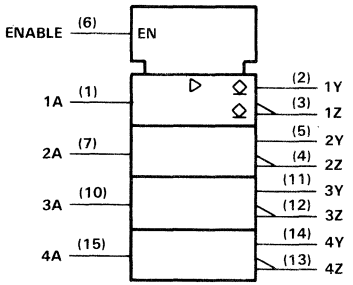
The MC3553 is characterized for operation over the full military temperature range of −55°C to 125°C.

FUNCTION TABLE

LOGIC INPUT	ENABLE INPUT	OUTPUT CURRENT	
		Z	Y
H	H	ON	OFF
L	H	OFF	ON
H	L	OFF	OFF
L	L	OFF	OFF

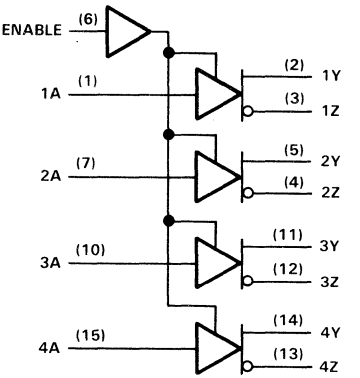
L = low logic level
H = high logic level

logic symbol†

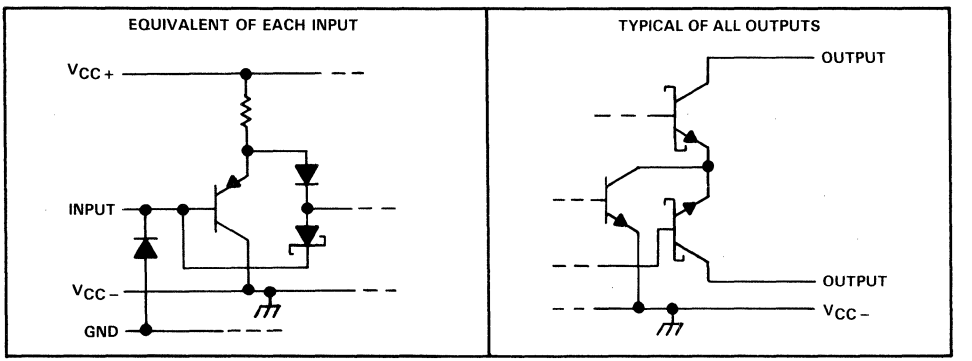


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 7 V
Supply voltage, V_{CC-} . . . . . −7 V
Input voltage (any input) . . . . . 5.5 V
Output voltage range (any output) . . . . . −5 V to 12 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1375 mW
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate to 275 mW at 125°C at the rate of 11.0 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	$T_A \geq 25°C$	4.5	5	5.5	V
	$T_A < 25°C$	4.75	5	5.5	
Supply voltage, V_{CC-}	$T_A \geq 25°C$	−4.5	−5	−5.5	V
	$T_A < 25°C$	−4.75	−5	−5.5	
High-level input voltage, V_{IH}		2		5.5	V
Low-level input voltage, V_{IL}		0		0.8	V
Common-mode output voltage range	V_{OCR+}	0		10	V
	V_{OCR-}	0		−3	V
Operating free-air temperature, T_A		−55		125	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = MAX, V_{CC-} = −MAX (unless otherwise noted)

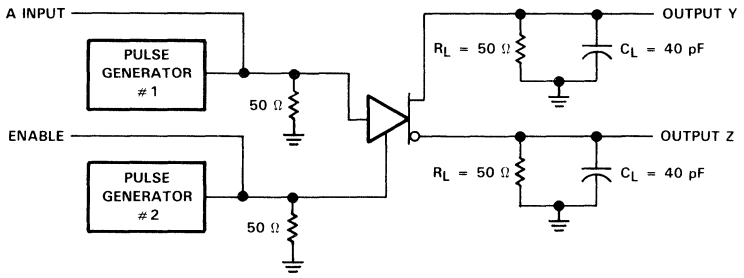
PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −12 mA			−0.9	−1.5	V
$I_{O(on)}$	On-state output current	V_{CC+} = MAX, V_{CC-} = MAX			11	15	mA
		V_{CC+} = MIN, V_{CC-} = MIN		6.5	11		
$I_{O(off)}$	Off-state output current	V_{CC+} = MIN, V_{CC-} = MIN, V_O = 10 V				100	μA
I_{IH}	High-level input current	V_I = 2.4 V				40	μA
		$V_I = V_{CC+}$ MAX				1	mA
I_{IL}	Low-level input current	V_I = 0.4 V				−1.6	mA
I_{CC+}	Supply current from V_{CC+}	A inputs at 0.4 V	Enable at 2 V		33	50	mA
			Enable at 0.4 V		33	50	
I_{CC-}	Supply current from V_{CC-}	A inputs at 0.4 V	Enable at 2 V		−68	−90	mA
			Enable at 0.4 V		−31	−40	

†For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, and T_A = 25°C.

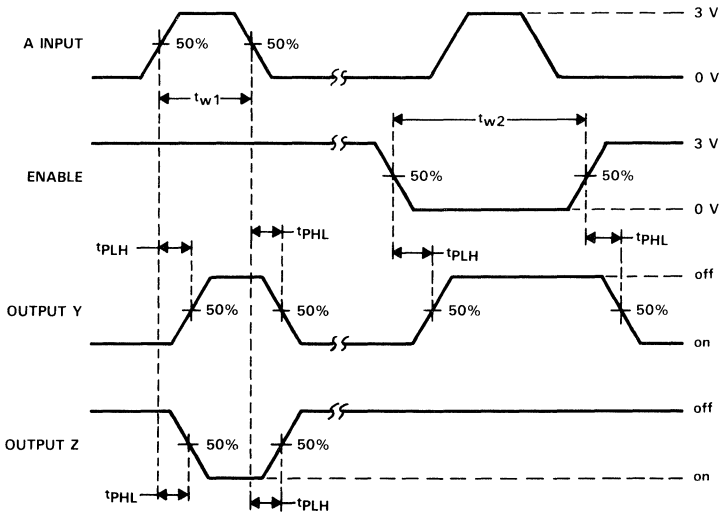
switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, R_L = 50 Ω, C_L = 40 pF, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y or Z	See Figure 1		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output	A	Y or Z			7	15	ns
t_{PLH}	Propagation delay time, low-to-high-level output	Enable	Y or Z			14	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output	Enable	Y or Z			15	25	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



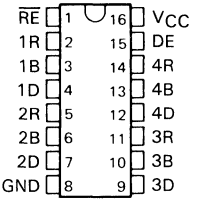
VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_O \approx 50\ \Omega$, $t_r = t_f = 10 \pm 5$ ns, $t_{w1} \leq 200$ ns, PRR ≤ 1 MHz, $t_{w2} \leq 1\ \mu s$, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

FIGURE 1. PROPAGATION DELAY TIMES

- **P-N-P Inputs for Minimal Input Loading (200 μA Maximum)**
- **High-Speed Schottky Circuitry**
- **3-State Outputs for Driver and Receiver**
- **Party-Line (Data-Bus) Operation**
- **Single 5-V Supply**
- **Designed to Be Interchangeable with Signetics N8T26, also Called 8T26**

D, J, OR N PACKAGE
(TOP VIEW)



description

The N8T26 is a quadruple transceiver utilizing Schottky-diode-clamped transistors. Both the driver and receiver have 3-state outputs. With p-n-p inputs, the input loading is reduced to a maximum input current of 200 μA. This device is capable of high switching rates into high-capacitance loads and are suitable for driving long bus lines.

The N8T26 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (DRIVER)

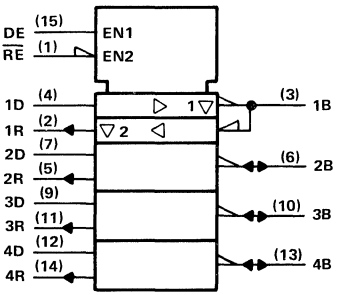
INPUT		OUTPUT
DE	D	B
H	L	H
H	H	L
L	X	Z

FUNCTION TABLE (RECEIVER)

INPUT		OUTPUT
RE	B	R
L	L	H
L	H	L
H	X	Z

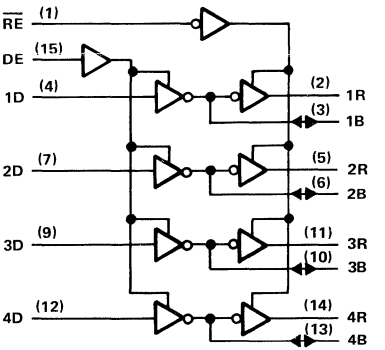
H = high level
L = low level
X = irrelevant
Z = high impedance

logic symbol†

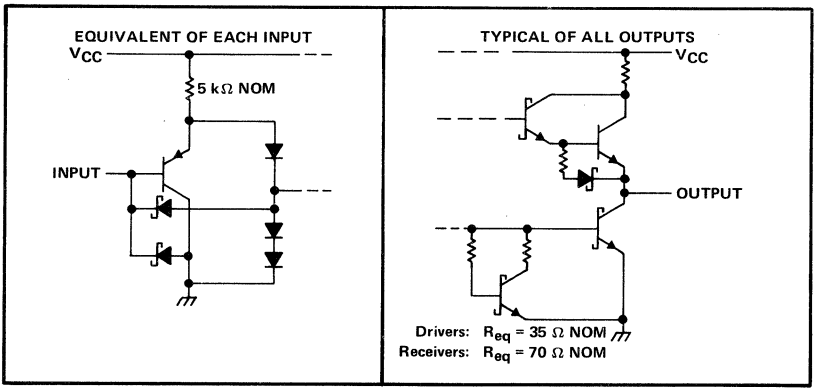


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	B, D, DE, $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	B, D, DE, $\overline{RE}$			0.85	V
High-level output current, I_{OH}	Driver, B			−10	mA
	Receiver, R			−2	
Low-level output current, I_{OL}	Driver, B			40	mA
	Receiver, R			16	
Operating free-air temperature, T_A		0		70	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature and supply voltage range (unless otherwise noted)

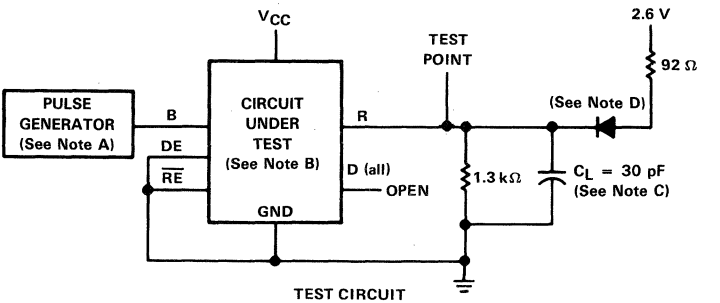
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	B,D,DE,$\overline{RE}$	I_I = −5 mA					−1	V
V_{OH}	High-level output voltage	B	V_{IH} = 2 V,	V_{IL} = 0.85 V,	I_{OH} = −10 mA	2.6	3.1		V
		R	V_{IL} = 0.85 V	I_{OH} −2 mA		2.6	3.1		
V_{OL}	Low-level output voltage	B	V_{IH} = 2 V,	I_{OL} = 40 mA				0.5	V
		R	V_{IH} = 2 V,	V_{IL} = 0.85 V,	I_{OL} = 16 mA			0.5	
I_{OZ}	Off-state (high-impedance state) output current	B,R	DE at 0.85 V	RE at 2 V,	V_O = 2.6 V			100	μA
		R	RE at 2 V,	V_O = 0.5 V				−100	
I_{IH}	High-level input current	D,DE,$\overline{RE}$	V_I = 5.25 V					25	μA
I_{IL}	Low-level input current	B,D,DE,$\overline{RE}$	V_I = 0.4 V					−200	μA
I_{OS}	Short-circuit output current‡	B	V_{CC} = 5.25 V			−50		−150	mA
		R				−30		−75	
I_{CC}	Supply current		V_{CC} = 5.25 V, No load					87	mA

†All typical values are at T_A = 25°C and V_{CC} = 5 V.
‡Only one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

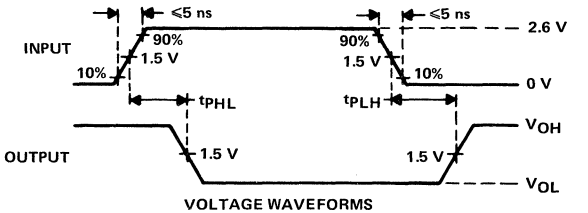
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	B	R	C_L = 30 pF,		8	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output			See Figure 1		7	10	
t_{PLH}	Propagation delay time, low-to-high-level output	D	B	C_L = 300 pF,		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			See Figure 2		12	20	
t_{PLZ}	Output disable time from low level	$\overline{RE}$	R	C_L = 30 pF,		9	17	ns
t_{PZL}	Output enable time to low level			See Figure 3		15	30	
t_{PLZ}	Output disable time from low level	DE	B	C_L = 300 pF,		20	43	ns
t_{PZL}	Output enable time to low level			See Figure 4		20	38	

PARAMETER MEASUREMENT INFORMATION

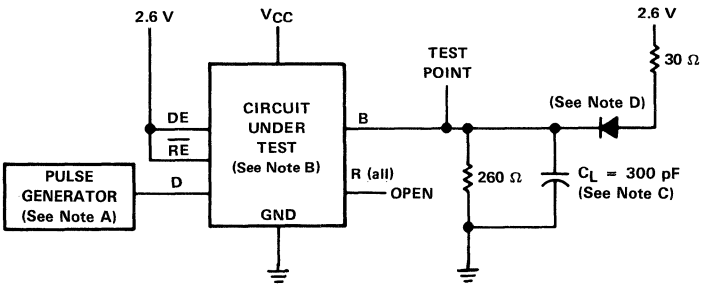


TEST CIRCUIT

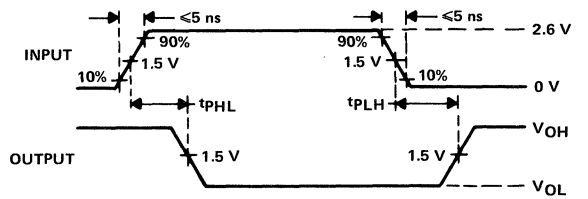


VOLTAGE WAVEFORMS

FIGURE 1. PROPAGATION DELAY TIMES FROM BUS TO RECEIVER OUTPUT



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2. PROPAGATION DELAY TIMES FROM DRIVER INPUT TO BUS

NOTES: A. The pulse generator in Figures 1 and 2 has the following characteristics: PRR ≤ 10 MHz, duty cycle = 50%, $Z_O \approx 50\ \Omega$.
B. All inputs and outputs not shown are open.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916 or 1N3064.

PARAMETER MEASUREMENT INFORMATION

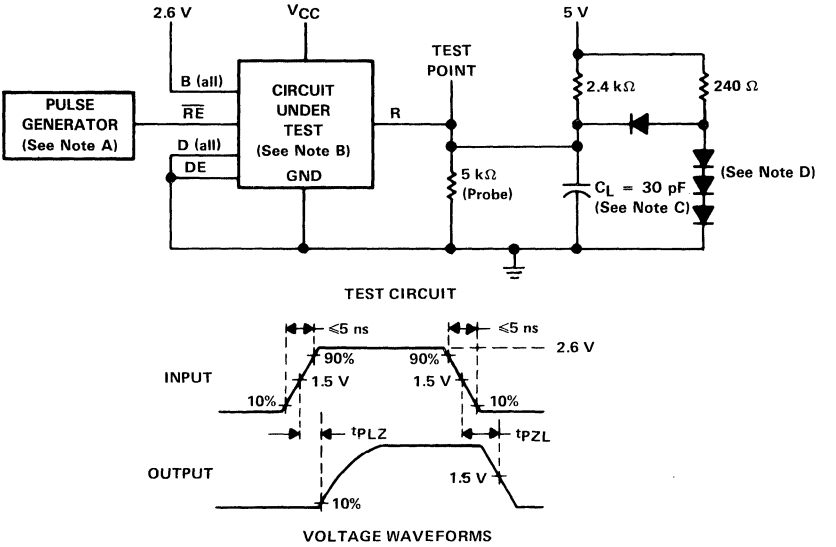


FIGURE 3. RECEIVER ENABLE AND DISABLE TIMES

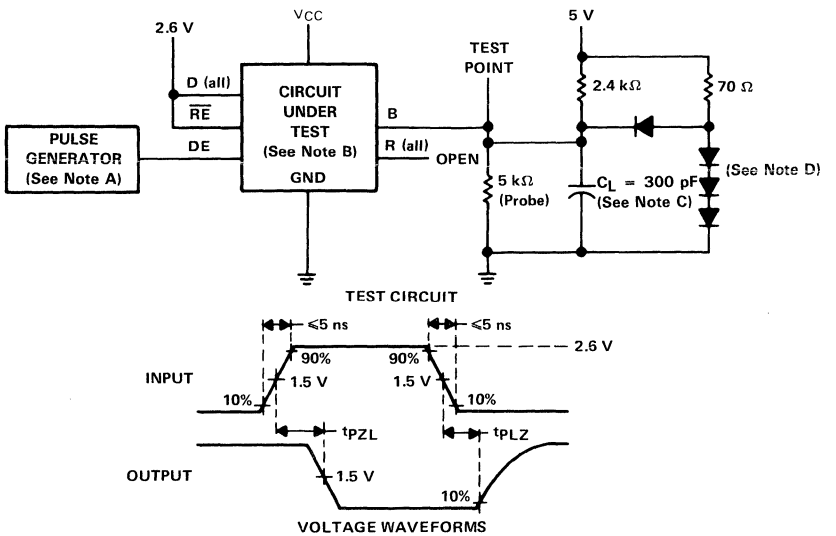
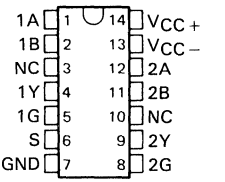


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

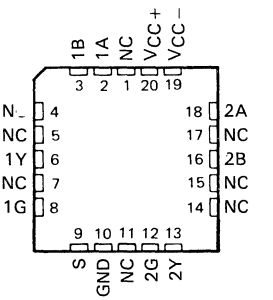
NOTES: A. The pulse generator in Figures 3 and 4 has the following characteristics: PRR ≤ 5 MHz, duty cycle = 50%, $Z_O \approx 50\ \Omega$.
B. All inputs and outputs not shown are open.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916 or 1N3064.

- High Speed
- Standard Supply Voltage
- Dual Channels
- High Common-Mode Rejection Ratio
- High Input Impedance
- High Input Sensitivity
- Differential Input Common-Mode Range of ±3 V
- Strobe Inputs for Receiver Selection
- Gate Inputs for Logic Versatility
- TTL Drive Capability
- High DC Noise Margin
- '107A and '107B Have Totem-Pole Outputs
- '108A and '108B Have Open-Collector Outputs
- "B" Versions Have Diode-Protected Input for Power-Off Condition

SN55107A, SN55107B, SN55108A
SN55108B . . . J PACKAGE
SN75107A, SN75107B, SN75108A
SN75108B . . . D, J, OR N PACKAGE
(TOP VIEW)



SN55107A, SN55107B, SN55108A,
SN55108B . . . FK PACKAGE
(TOP VIEW)



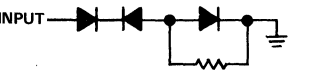
NC—No internal connection

description

These circuits are TTL-compatible high-speed line receivers. Each is a monolithic dual circuit featuring two independent channels. They are designed for general use as well as such specific applications as data comparators and balanced, unbalanced, and party-line transmission systems. These devices are unilaterally interchangeable with and are replacements for the SN55107, SN55108, SN75107, and SN75108, but offer diode-clamped strobe inputs to simplify circuit design.

The essential difference between the "A" and "B" versions can be seen in the schematics. Input-protection diodes are in series with the collectors of the differential-input transistors of the "B" versions. These diodes are useful in certain "party-line" systems that may have multiple V_{CC+} power supplies and may be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:

"A" VERSION



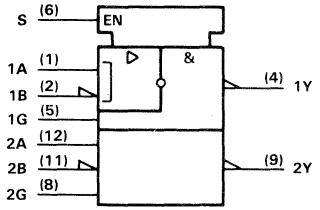
"B" VERSION

This would be a problem in specific systems that might possibly have the transmission lines biased to some potential greater than 1.4 V.

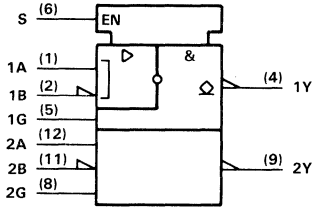
The SN55107A, SN55107B, SN55108A, and SN55108B are characterized for operation over the full military temperature range of −55°C to 125°C. The SN75107A, SN75107B, SN75108A, and SN75108B are characterized for operation from 0°C to 70°C.

logic symbols†

SN55107
SN75107

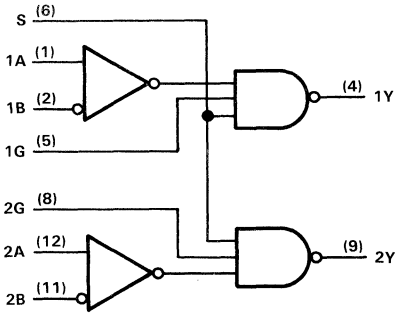


SN55108
SN75108



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)

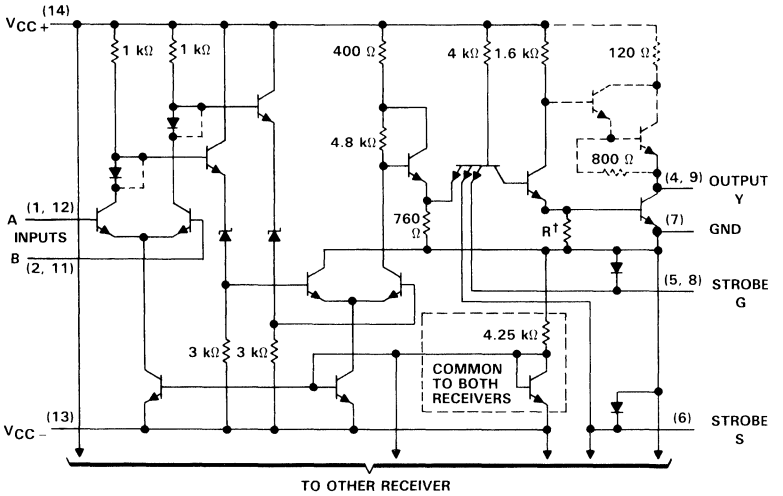


FUNCTION TABLE

DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 25$ mV	X	X	H
-25 mV $< V_{ID} <$ 25 mV	X	L	H
	L	X	H
	H	H	Indeterminate
$V_{ID} \leq -25$ mV	X	L	H
	L	X	H
	H	H	L

H = high level, L = low level, X = irrelevant

schematic (each receiver)



Pin numbers shown are for D, J, and N packages.

†R = 1 kΩ for '107A and '107B, 750 Ω for '108A and '108B.

NOTES: 1. Resistor values shown are nominal.

2. Components shown with dashed lines in the output circuitry are applicable to the '107A and '107B only. Diodes in series with the collectors of the differential input transistors are short circuited on '107A and '108A.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 3)	7 V
Supply voltage, V_{CC-}	−7 V
Differential input voltage (see Note 4)	±6 V
Common-mode input voltage (see Note 5)	+5 V
Strobe input voltage	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 6):	
D package	950 mW
FK or J package: Series 55	1375 mW
J package: Series 75	1025 mW
N package	1150 mW
Operating free-air temperature range: Series 55	−55°C to 125°C
Series 75	0°C to 70°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C

NOTES: 3. All voltage values, except differential voltages, are with respect to network ground terminal.

4. Differential voltage values are at the noninverting (A) terminal with respect to the inverting (B) terminal.

5. Common-mode input voltage is the average of the voltages at the A and B inputs.

6. For operation above 25°C free-air temperature, derate linearly at the following rates: 7.6 mW/°C for the D package, 11.0 mW/°C for the FK and J packages with series 55 chips, 8.2 mW/°C for the J package with series 75 chips, and 9.2 mW/°C for the N package.

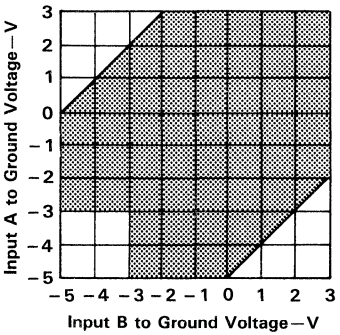
recommended operating conditions (see Note 7)

	SN55107A, SN55107B SN55108A, SN55108B			SN75107A, SN75107B SN75108A, SN75108B			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}	4.5	5	5.5	4.75	5	5.25	V
Supply voltage, V_{CC-}	−4.5	−5	−5.5	−4.75	−5	−5.25	V
High-level input voltage between differential inputs, V_{IDH} (see Note 8)	0.025		5	0.025		5	V
Low-level input voltage between differential inputs, V_{IDL} (see Note 8)	−5†		−0.025	−5†		−0.025	V
Common-mode input voltage, V_{IC} (see Notes 8 and 9)	−3†		3	−3†		3	V
Input voltage, any differential input to ground (see Note 8)	−5†		3	−5†		3	V
High-level input voltage at strobe inputs, $V_{IH(S)}$	2		5.5	2		5.5	V
Low-level input voltage at strobe inputs, $V_{IL(S)}$	0		0.8	0		0.8	V
Low-level output current, I_{OL}			−16			−16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for input voltage levels only.

NOTES: 7. When using only one channel of the line receiver, the strobe G of the unused channel should be grounded and at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 V and 3 V.
8. The recommended combinations of input voltages fall within the shaded area of the figure shown.
9. The common-mode voltage may be as low as −4 V provided that the more positive of the two inputs is not more negative than −3 V.

RECOMMENDED COMBINATIONS
OF INPUT VOLTAGES



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

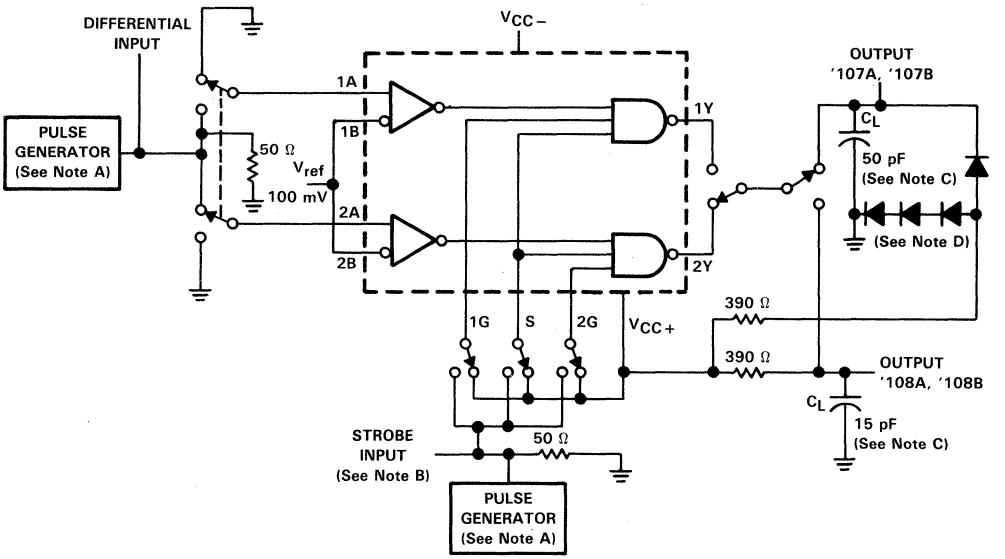
PARAMETER			TEST CONDITIONS†		'107A, '107B MIN	'107A, '107B TYP‡	'107A, '107B MAX	'108A, '108B MIN	'108A, '108B TYP‡	'108A, '108B MAX	UNIT
I_{IH}	High-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = 5 V		30	75		30	75	μA
		B		V_{ID} = −5 V		30	75		30	75	
I_{IL}	Low-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = −5 V			−10			−10	μA
		B		V_{ID} = 5 V			−10			−10	
I_{IH}	High-level input current into 1G or 2G		$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = 2.4 V				40			40	μA
			$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = MAX V_{CC+}				1			1	mA
I_{IL}	Low-level input current into 1G or 2G		$V_{CC\pm}$ = MAX, $V_{IL(S)}$ = 0.4 V				−1.6			−1.6	mA
I_{IH}	High-level input current into S		$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = 2.4 V				80			80	μA
			$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = MAX $V_{CC\pm}$				2			2	mA
I_{IL}	Low-level input current into S		$V_{CC\pm}$ = MAX, $V_{IL(S)}$ = 0.4 V				−3.2			−3.2	mA
V_{OH}	High-level output voltage		$V_{CC\pm}$ = MIN, $V_{IL(S)}$ = 0.8 V, V_{IDH} = 25 mV, I_{OH} = −400 μA, V_{IC} = −3 V to 3 V		2.4						V
V_{OL}	Low-level output voltage		$V_{CC\pm}$ = MIN, $V_{IH(S)}$ = 2 V, V_{IDL} = −25 mV, I_{OL} = 16 mA, V_{IC} = −3 V to 3 V				0.4			0.4	V
I_{OH}	High-level output current		$V_{CC\pm}$ = MIN, V_{OH} = MAX V_{CC+}							250	μA
I_{OS}	Short-circuit output current§		$V_{CC\pm}$ = MAX		−18		−70				mA
I_{CCH+}	Supply current from V_{CC+}, outputs high		$V_{CC\pm}$ = MAX, T_A = 25°C			18	30		18	30	mA
I_{CCH-}	Supply current from V_{CC-}, ouputs high		$V_{CC\pm}$ = MAX, T_A = 25°C			−8.4	−15		−8.4	−15	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

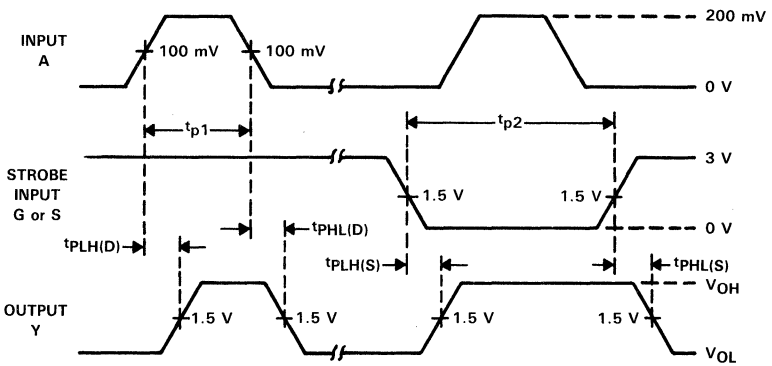
switching characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C (see Figure 1)

PARAMETER		TEST CONDITIONS	'107A, '107B MIN	'107A, '107B TYP	'107A, '107B MAX	'108A, '108B MIN	'108A, '108B TYP	'108A, '108B MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low-to-high-level output, from differential inputs A and B	R_L = 390 Ω, C_L = 50 pF		17	25				ns
		R_L = 390 Ω, C_L = 15 pF					19	25	
$t_{PHL(D)}$	Propagation delay time, high-to-low-level output, from differential inputs A and B	R_L = 390 Ω, C_L = 50 pF		17	25				ns
		R_L = 390 Ω, C_L = 15 pF					19	25	
$t_{PLH(S)}$	Propagation delay time, low-to-high-level output, from strobe input G or S	R_L = 390 Ω, C_L = 50 pF		10	15				ns
		R_L = 390 Ω, C_L = 15 pF					13	20	
$t_{PHL(S)}$	Propagation delay time, high-to-low-level output, from strobe input G or S	R_L = 390 Ω, C_L = 50 pF		8	15				ns
		R_L = 390 Ω, C_L = 15 pF					13	20	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1. PROPAGATION DELAY TIMES

NOTES: A. The pulse generators have the following characteristics: Z_o = 50 Ω, t_r = 10 ±5 ns, t_f = 10 ±5 ns, t_{pd1} = 500 ns, PRR ≤ 1 MHz, t_{pd2} = 1 μs, PRR ≤ 500 kHz.
B. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

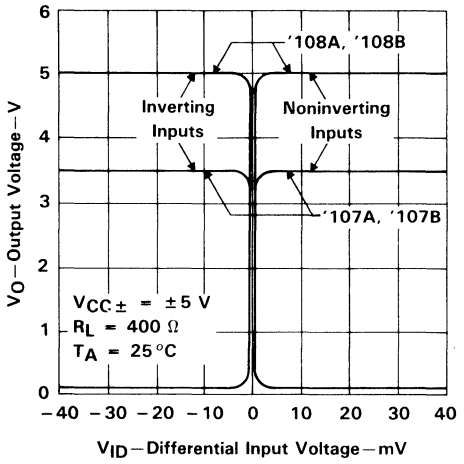


FIGURE 2

HIGH-LEVEL INPUT CURRENT INTO 1A or 2A
vs
FREE-AIR TEMPERATURE

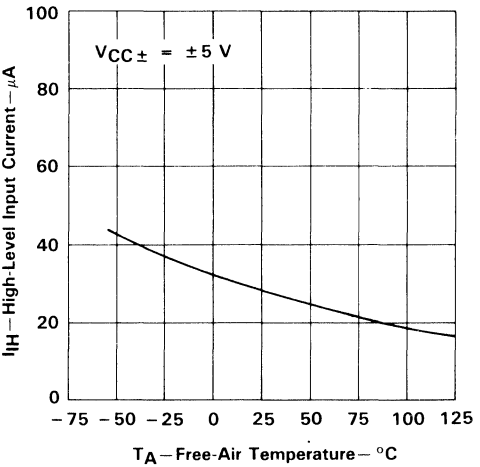


FIGURE 3

SUPPLY CURRENT, OUTPUTS HIGH
vs
FREE-AIR TEMPERATURE

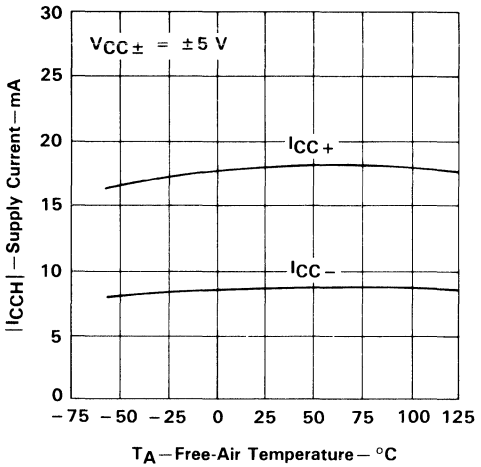


FIGURE 4

'107A, '107B
PROPAGATION DELAY TIME
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

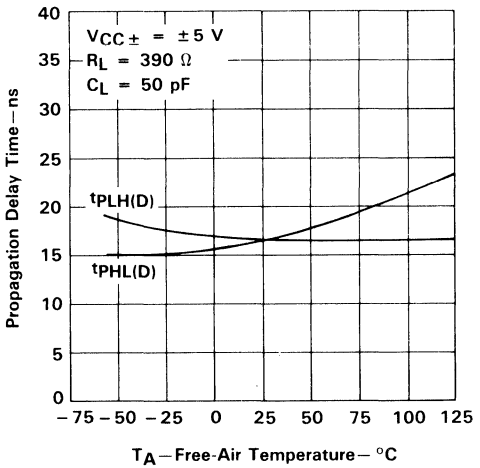


FIGURE 5

† Values below 0°C and above 70°C apply to SN55 Series only.

TYPICAL CHARACTERISTICS†

'108A, '108B
PROPAGATION DELAY TIME, LOW-TO-HIGH LEVEL
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

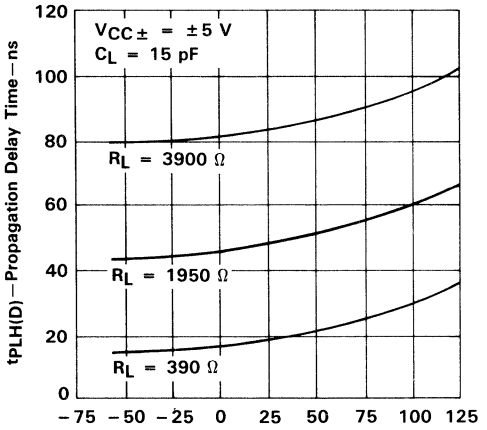


FIGURE 6

'108A, '108B
PROPAGATION DELAY TIME, HIGH-TO-LOW LEVEL
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

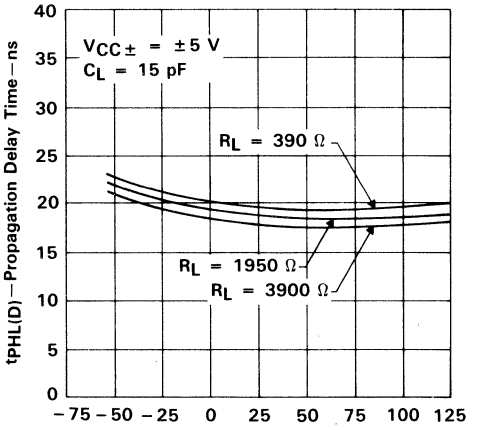


FIGURE 7

'107A, '107B
PROPAGATION DELAY TIME (STROBE INPUTS)
vs
FREE-AIR TEMPERATURE

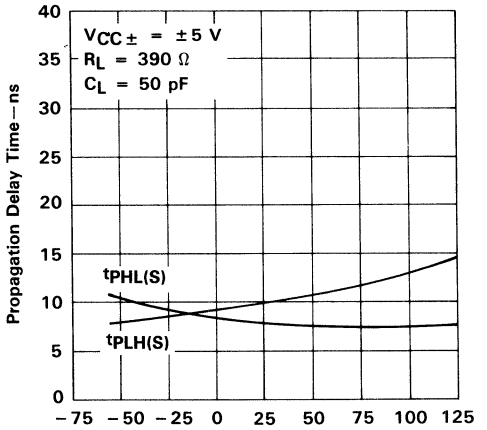


FIGURE 8

'108A, '108B
PROPAGATION DELAY TIME (STROBE INPUTS)
vs
FREE-AIR TEMPERATURE

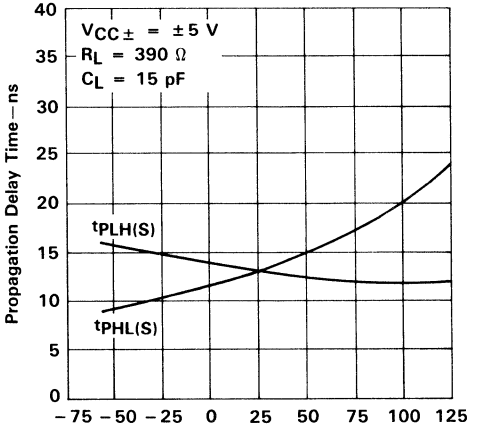


FIGURE 9

† Values below 0°C and above 70°C apply to SN55 Series only.

APPLICATION INFORMATION

basic balanced-line transmission system

The '107A, '107B, '108A, and '108B dual line circuits are designed specifically for use in high-speed data transmission systems that utilize balanced, terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so noise induced on one line is also induced on the other. The noise appears common mode at the receiver input terminals where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver-output circuit allows terminated transmission lines to be driven at normal line impedances. High-speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Crosstalk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately (30 + 1.3 L) ns, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver-input logic levels. The voltage difference is approximately:

$$V_{DIFF} \approx 1/2 I_{O(on)} \cdot R_T.$$

High series line resistance will cause degradation of the signal. The receivers, however, will detect signals as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

Line-termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately:

$$V_{DIFF} \approx I_{O(on)} \cdot R_T.$$

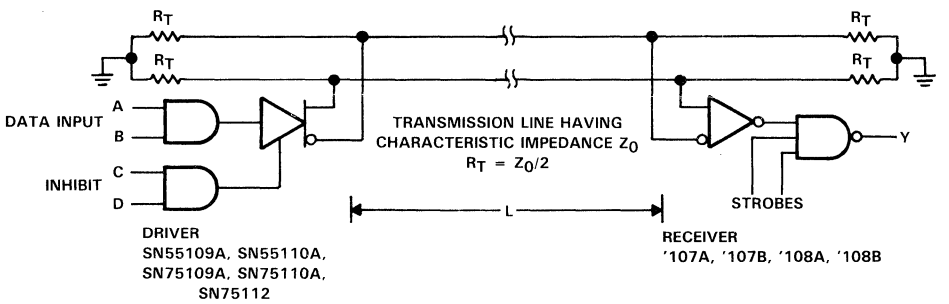


FIGURE 10

data-bus or party-line system

The strobe feature of the receivers and the inhibit feature of the drivers allow these dual line circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data is thus time-multiplexed on the transmission line. The device specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The data-bus system offers maximum performance at minimum cost.

APPLICATION INFORMATION

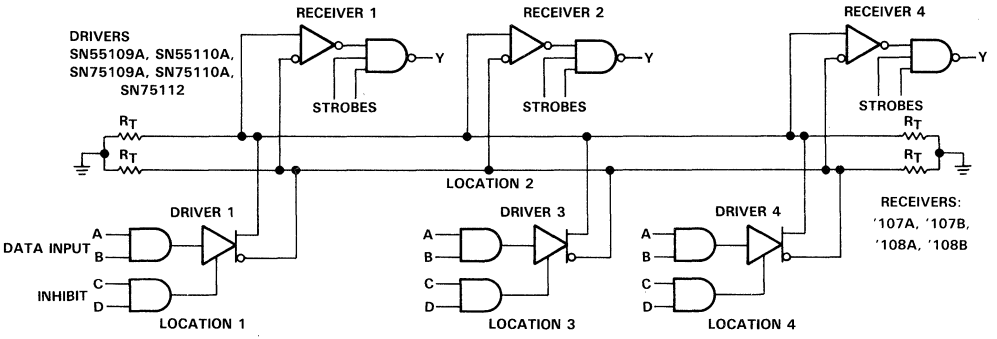


FIGURE 11

unbalanced or single-line systems

These dual line circuits may also be used in unbalanced or single-line systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environmental noise is not severe.

The receiver threshold level is established by applying a dc reference voltage to one receiver input terminal. The signal from the transmission line is applied to the remaining input. The reference voltage should be optimized so that signal swing is symmetrical about it for maximum noise margin. The reference voltage should be in the range of −3 V to 3 V. It can be provided by a voltage supply or by a voltage divider from an available supply voltage.

A single-ended output from a driver may be used in single-line systems. Coaxial or shielded line is preferred for minimum noise and crosstalk problems. For large signal swings, the high output current (typically 27 mA) of the SN75112 is recommended. Drivers may be paralleled for higher current. When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

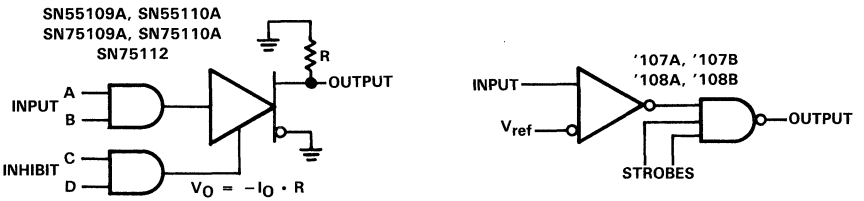


FIGURE 12

APPLICATION INFORMATION

'108A, '108B dot-AND output connections

The '108A, '108B line receivers feature an open-collector-output circuit that can be connected in the dot-AND logic configuration with other similar open-collector outputs. This allows a level of logic to be implemented without additional logic delay.

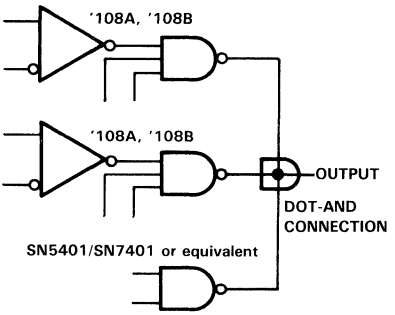


FIGURE 13

increasing common-mode input voltage range of receiver

The common-mode voltage range or CMVR is defined as the range of voltage applied simultaneously to both input terminals that if exceeded does not allow normal operation of the receiver.

The recommended operating CMVR is ±3 V, making it useful in all but the noisiest environments. In extremely noisy environments, common-mode voltage can easily reach ±10 V to ±15 V if some precautions are not taken to reduce ground and power supply noise, as well as crosstalk problems. When the receiver must operate in such conditions, input attenuators should be used to decrease the system common-mode noise to a tolerable level at the receiver inputs. Differential noise is also reduced by the same ratio.

These attenuators have been intentionally omitted from the receiver input terminals so the designer may select resistors that will be compatible with his particular application or environment. Furthermore, the use of attenuators adversely affects the input sensitivity, the propagation delay time, the power dissipation, and in some cases (depending on the selected resistor values) the input impedance, therefore reducing the versatility of the receiver.

The ability of the receiver to operate with approximately ±15 V common-mode voltage at the inputs has been checked using the circuit shown in Figure 14. The resistors R1 and R2 provide a voltage divider network. Dividers with three different values presenting a 5-to-1 attenuation were used so as to operate the differential inputs at approximately ±3 V common-mode voltage. Careful matching of the two attenuators is needed so as to balance the overdrive at the input stage. The resistors used are shown in Table A.

TABLE A

Attenuator 1:	R1 = 2 kΩ, R2 = 0.5 kΩ
Attenuator 2:	R1 = 6 kΩ, R2 = 1.5 kΩ
Attenuator 3:	R1 = 12 kΩ, R2 = 3 kΩ

Table B shows some of the typical switching results obtained under such conditions.

TABLE B. TYPICAL PROPAGATION DELAYS FOR RECEIVER WITH ATTENUATOR TEST CIRCUIT SHOWN IN FIGURE 14

DEVICE	PARAMETERS	INPUT ATTENUATOR	TYPICAL (ns)
'107A, '107B	t_{PLH}	1	20
		2	32
		3	42
	t_{PHL}	1	22
		2	31
		3	33
'108A, '108B	t_{PLH}	1	36
		2	47
		3	57
	t_{PHL}	1	29
		2	38
		3	41

APPLICATION INFORMATION

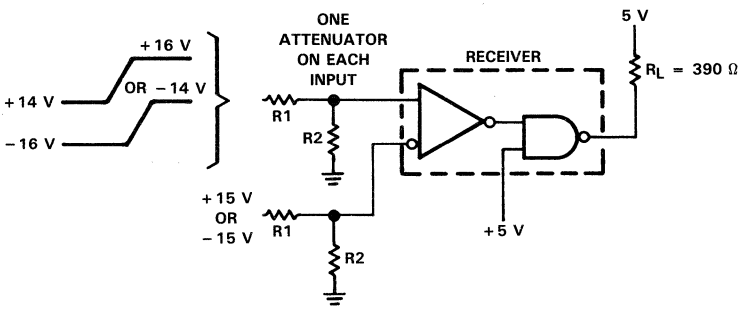


FIGURE 14. COMMON-MODE CIRCUIT FOR TESTING INPUT ATTENUATORS, WITH RESULTS SHOWN IN TABLE B

Two methods of terminating a transmission line to reduce reflections are:

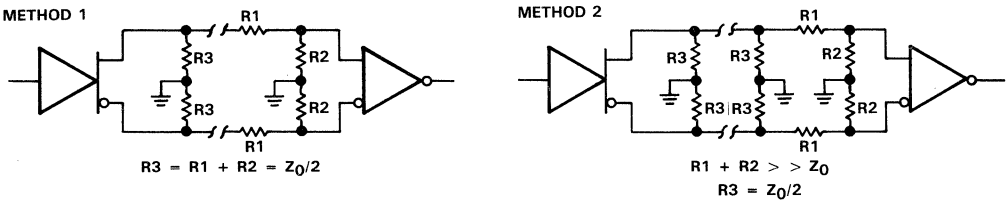


FIGURE 15

The first method uses the resistors as the attenuation network and line termination. The second method uses two additional resistors for the line terminations.

APPLICATION INFORMATION

For party-line operation, method 2 should be used as follows:

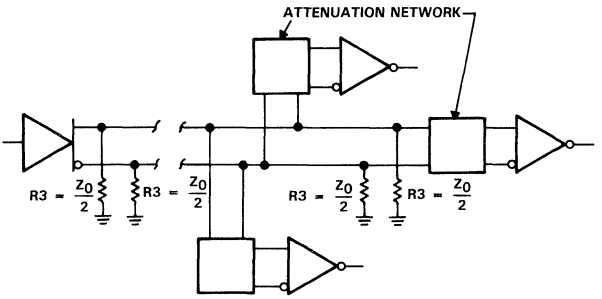


FIGURE 16

To minimize the loading, the values of R1 and R2 should be fairly large. Examples of possible values are shown in Table A.

furnace control using the SN75108A

The furnace control circuit in Figure 17 is an example of the possible use of the SN55107A Series in areas other than what would normally be considered electronic systems. Basically the operation of this control is as follows. When the room temperature is below the desired level, the resistance of the room temperature sensor is high and channel 1 noninverting input is below (less positive than) the reference level set on the input differential amplifier. This situation causes a low output, operating the "heat on" relay and turning on the heat. The channel 2 noninverting input is below the reference level when the bonnet temperature of the furnace reaches the desired level. This causes a low output, thus operating the blower relay. Normally the furnace is shut down when the room temperature reaches the desired level and the channel 1 output goes high, turning the heat off. The blower remains on as long as the bonnet temperature is high, even after the "heat on" relay is off. There is also a safety switch in the bonnet that shuts the furnace down if the temperature there exceeds desired limitations. The types of temperature-sensing devices and bias-resistor values used are determined by the particular operating conditions encountered.

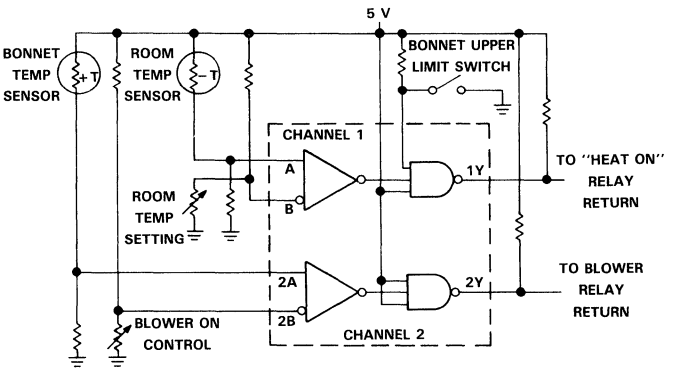


FIGURE 17. FURNACE CONTROL USING SN75108A

APPLICATION INFORMATION

repeaters for long lines

In some cases, the driven line may be so long that the noise level on the line reaches the common-mode limits or the attenuation becomes too large and results in poor reception. In such a case, a simple application of a receiver and a driver as repeaters [shown in Figure 18(a)] restores the signal level and allows an adequate signal level at the receiving end. If multichannel operation is desired, then proper gating for each channel must be sent through the repeater station using another repeater set as in Figure 18(b).

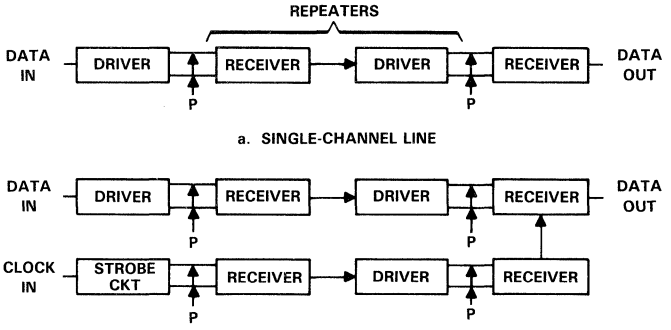


FIGURE 18. RECEIVER-DRIVER REPEATERS

receiver as dual differential comparator

There are many applications for differential comparators, such as voltage comparison, threshold detection, controlled Schmitt triggering, and pulse width control.

As a differential comparator, a '107A or '108A may be connected so as to compare the noninverting input terminal with the inverting input as shown in Figure 19. Thus the output will be high or low resulting from the A input being greater or less than the reference. The strobe inputs allow additional control over the circuit so that either output or both may be inhibited.

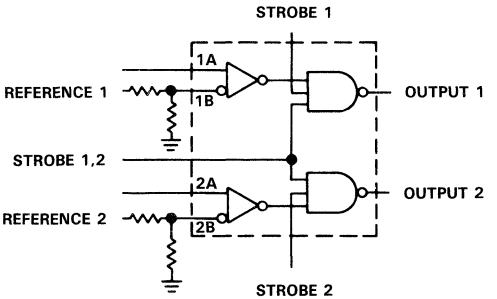
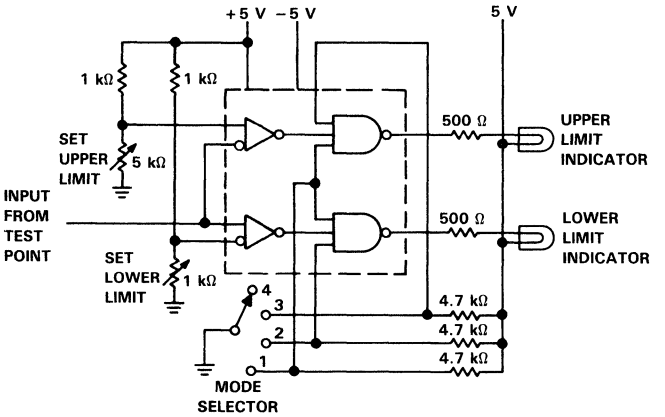


FIGURE 19. SN55107A SERIES RECEIVER AS A DUAL DIFFERENTIAL COMPARATOR

APPLICATION INFORMATION

window detector

The window detector circuit in Figure 20 has a large number of applications in test equipment and in determining upper limits, lower limits, or both at the same time — such as detecting whether a voltage or signal has exceeded its limits or "window". Illumination of the upper-limit (lower-limit) indicator shows that the input voltage is above (below) the selected upper (lower) limit. A mode selector is provided for selecting the desired test. For window detecting, the "upper and lower limits" test position is used.



MODE SELECTOR LEGEND

POSITION	CONDITION
1	OFF
2	TEST FOR UPPER LIMIT
3	TEST FOR LOWER LIMIT
4	TEST FOR UPPER AND LOWER LIMITS

FIGURE 20. WINDOW DETECTOR USING SN75108A

APPLICATION INFORMATION

temperature controller with zero-voltage switching

The circuit in Figure 21 switches an electric resistive heater on or off by providing negative-going pulses to the gate of a triac during the time interval when the line voltage is passing through zero. The pulse generator is the 2N5447 and four diodes. This portion of the circuit provides negative-going pulses during the short time (approximately 100 μs) when the line voltage is near zero. These pulses are fed to the inverting input of one channel of the '108A. If the room temperature is below the desired level, the resistance of the thermistor is high and the noninverting input of channel 2 is above the reference level determined by the thermostat setting. This provides a high-level output from channel 2. This output is AND'ed with the positive-going pulses from the output of channel 1, which are reinverted in the 2N5449.

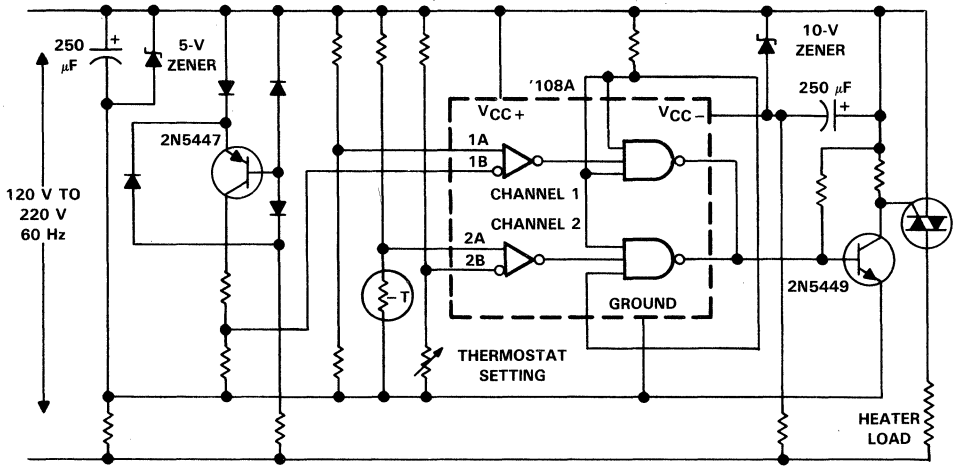
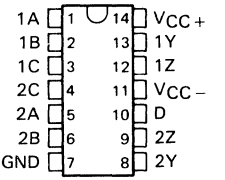


FIGURE 21. ZERO-VOLTAGE SWITCHING TEMPERATURE CONTROLLER

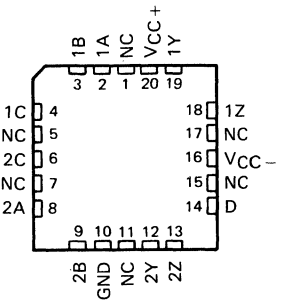
- Improved Stability over Supply Voltage and Temperature Ranges
- Constant-Current Outputs
- High Speed
- Standard Supply Voltages
- High Output Impedance
- High Common-Mode Output Voltage Range (−3 V to 10 V)
- TTL Input Compatibility
- Inhibitor Available for Driver Selection
- Glitch-Free During Power-Up/Down

−55°C to 125°C J or FK PACKAGE	0°C to 70°C J or N PACKAGE	OUTPUT FUNCTION
SN55109A	SN75109A	6-mA Current Switch
SN55110A	SN75110A	12-mA Current Switch
	SN75112	27-mA Current Switch

SN55109A, SN55110A, . . . J PACKAGE
SN75109A, SN75110A, SN75112 . . .
D, J, OR N PACKAGE
(TOP VIEW)



SN55109A, SN55110A . . . FK PACKAGE
(TOP VIEW)

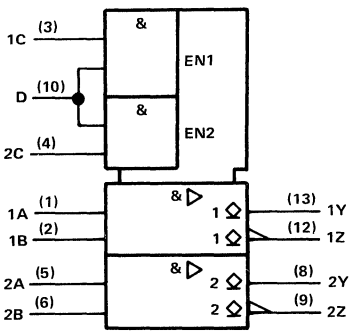


NC—No internal connection

description

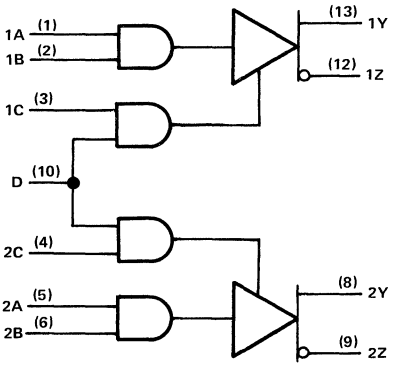
The SN55109A, SN55110A, SN75109A, SN75110A, and SN75112 have improved output current regulation with supply voltage and temperature variations. In addition, the higher current of the SN75112 (27 mA) allows data to be transmitted over longer lines. These drivers offer optimum performance when used with the SN55107A, SN55108A, SN75107A, and SN75108A line receivers.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IED Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

description (continued)

These drivers feature independent channels with common voltage supply and ground terminals. The significant difference between the three drivers is in the output current specification. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by low logic levels on the enable inputs. The output current is nominally 6 mA for the '109A, 12 mA for the '110A, and 27 mA for the SN75112.

The enable/inhibit feature is provided so the circuits can be used in party-line or data-bus applications. A strobe or inhibitor (enable D), common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode, $I_{O(off)}$, is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The output impedance of the driver in the inhibited mode is very high—the output impedance of a transistor biased to cutoff.

The driver outputs have a common-mode voltage range of −3 V to 10 V, allowing common-mode voltage on the line without affecting driver performance.

All inputs are diode clamped and are designed to satisfy TTL-system requirements. The inputs are tested at 2 V for high-logic-level input conditions and 0.8 V for low-logic-level input conditions. These tests assure 400 mV of noise margin when interfaced with Series 54/74 TTL.

The SN55109A and SN55110A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN75109A, SN75110A, and SN75112 are characterized for operation from 0°C to 70°C.

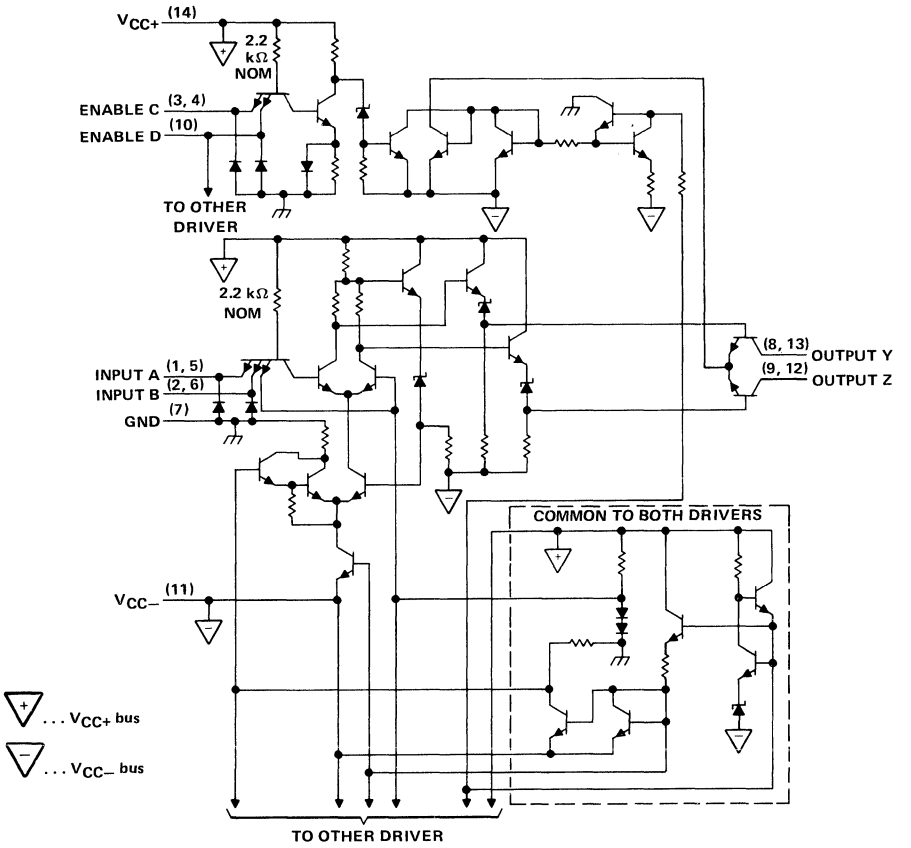
FUNCTION TABLE (EACH DRIVER)

LOGIC INPUTS		ENABLE INPUTS		OUTPUTS†	
A	B	C	D	Y	Z
X	X	L	X	OFF	OFF
X	X	X	L	OFF	OFF
L	X	H	H	ON	OFF
X	L	H	H	ON	OFF
H	H	H	H	OFF	ON

H = high level, L = low level, X = irrelevant

†When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

schematic (each driver)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55109A SN55110A	SN75109A SN75110A	SN75112	UNIT
V_{CC+} Supply voltage (see Note 1)		7	7	7	V
V_{CC-} Supply voltage		−7	−7	−7	V
V_I Input voltage		5.5	5.5	5.5	V
Output voltage range		−5 to 12	−5 to 12	−5 to 12	V
Continuous total power dissipation (see Note 2)		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	0 to 70	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package		260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package		300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D package		260	260	°C
	N package		260	260	

NOTES: 1. Voltage values are with respect to network ground terminal.
2. In the FK or J package, SN55109A and SN55110A chips are either silver glass or alloy mounted, and SN75109A, SN75110A, and SN75112 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55 ____ A)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75 _____)	1025 mW	8.2 mW/°C	656 mW	—
N	1150 mW	9.2 mW/°C	736 mW	—

recommended operating conditions (see Note 3)

		SN55109A, SN55110A			SN75109A, SN75110A SN75112			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC+}	$T_A \geq 0°C$	4.5	5	5.5	4.75	5	5.25	V
	$T_A < 0°C$	4.75	5	5.5				
Supply voltage V_{CC-}	$T_A \geq 0°C$	−4.5	−5	−5.5	−4.75	−5	−5.25	V
	$T_A < 0°C$	−4.75	−5	−5.5				
Positive common-mode output voltage		0		10	0		10	V
Negative common-mode output voltage		0		−3	0		−3	V
High-level input voltage, V_{IH}		2			2			V
Low-level input voltage, V_{IL}				0.8			0.8	V
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 3: When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN55109A, SN75109A			SN55110A, SN75110A			SN75112			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage		$V_{CC\pm}$ = MIN, I_I = −12 mA		−0.9	−1.5		−0.9	−1.5		−0.9	−1.5	V
$I_{O(on)}$	On-state output current		$V_{CC\pm}$ = MAX, V_O = 10 V		6	7		12	15		27	36	mA
			$V_{CC\pm}$ = MIN, V_O = −3 V	3.5	6		6.5	12		18	27		
$I_{O(off)}$	Off-state output current		$V_{CC\pm}$ = MIN, V_O = 10 V			100			100			100	μA
I_I	Input current at maximum input voltage	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 5.5 V			1			1			1	mA
		D input				2			2			2	
I_{IH}	High-level input current	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 2.4 V			40			40			40	μA
		D input				80			80			80	
I_{IL}	Low-level input current	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 0.4 V			−3			−3			−3	mA
		D input				−6			−6			−6	
$I_{CC+(on)}$	Supply current from V_{CC+} with driver enabled		$V_{CC\pm}$ = MAX, A and B inputs at 0.4 V, C and D inputs at 2 V		18	30		23	35		25	40	mA
$I_{CC-(on)}$	Supply current from V_{CC-} with driver enabled				−18	−30		−34	−50		−65	−100	
$I_{CC+(off)}$	Supply current from V_{CC+} with driver inhibited		$V_{CC\pm}$ = MAX, A, B, C, and D inputs at 0.4 V		18			21			30		mA
$I_{CC-(off)}$	Supply current from V_{CC-} with driver inhibited				−10			−17			−32		

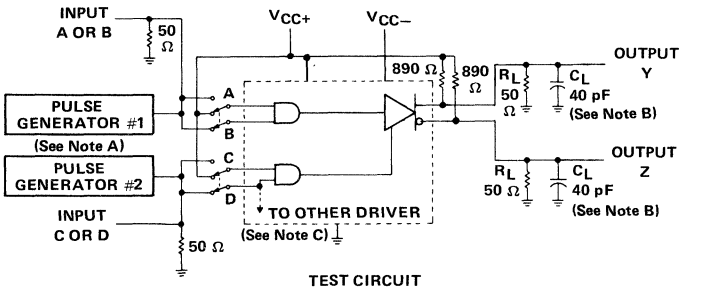
†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

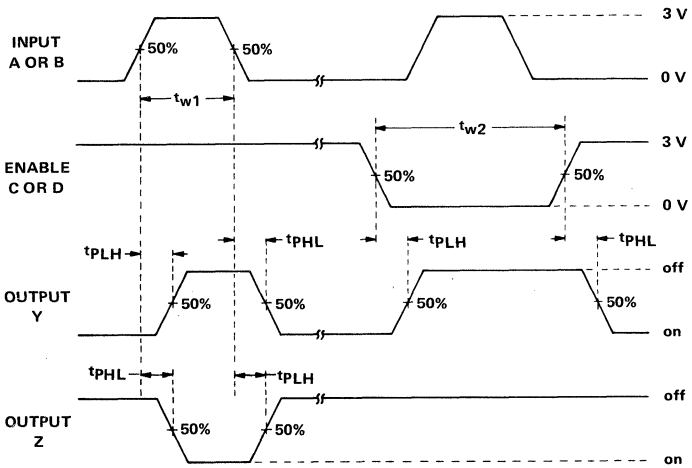
PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y or Z	C_L = 40 pF, R_L = 50 Ω, See Figure 1		9	15	ns
t_{PHL}					9	15	ns
t_{PLH}	C or D	Y or Z			16	25	ns
t_{PHL}					13	25	ns

†t_{PLH} = Propagation delay time, low-to-high-level output.
t_{PHL} = Propagation delay time, high-to-low-level output.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_o = 50 Ω, $t_e = t_f$ = 10 ±5 ns, t_{w1} = 500 ns, PRR ≤ 1 MHz, t_{w2} = 1 μs, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.
C. For simplicity, only one channel and the enable connections are shown.

FIGURE 1. PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

ON-STATE OUTPUT CURRENT
vs
NEGATIVE SUPPLY VOLTAGE

SN55109A, SN75109A

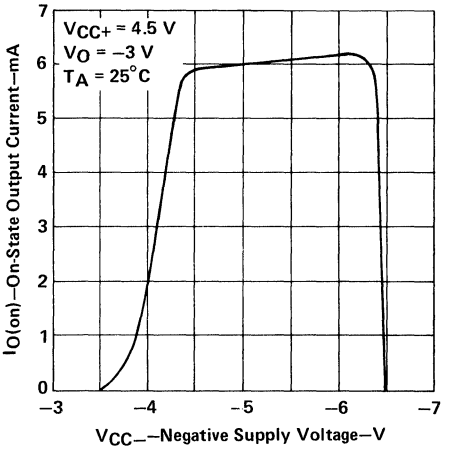


FIGURE 2

SN55110A, SN75110A

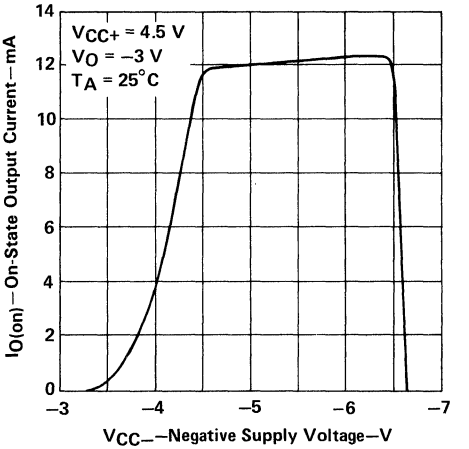


FIGURE 3

SN75112

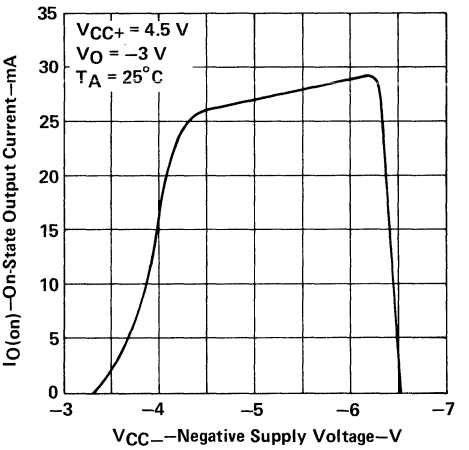


FIGURE 4

APPLICATION INFORMATION

special pulse-control circuit

Figure 5 shows a circuit that may be used as a pulse generator output or in many other testing applications.

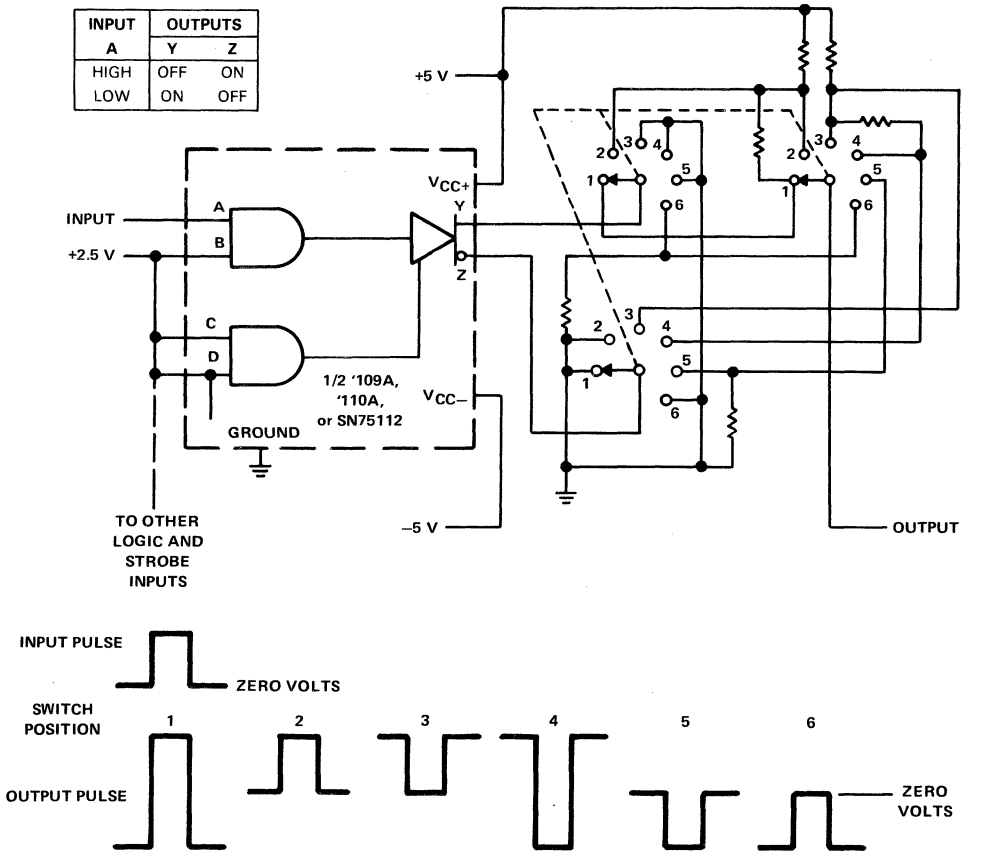


FIGURE 5. PULSE CONTROL CIRCUIT

D3000, FEBRUARY 1986—REVISED OCTOBER 1988

- **Similar to a Dual Version of the SN55109A/SN75109A Line Driver**
- **Improved Stability Over Supply Voltage and Temperature Ranges**
- **Constant-Current Outputs**
- **High Output Impedance**
- **High Common-Mode Output Voltage Range (−3 V to 10 V)**
- **Glitch-Free Power-Up/Power-Down Operation**
- **TTL Input Compatibility**
- **Common Enable Circuit**

description

The SN55111 and SN75111 feature four line drivers with a common enable input. When the enable input is high, a constant output current is switched between each pair of output terminals in response to the logic level at that channel's input. When the enable is low, all channel outputs are nonconductive (transistors biased to cutoff). This feature minimizes loading in party-line systems where a large number of drivers share the same line.

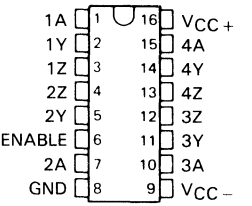
The driver outputs have a common-mode voltage range of −3 V to 10 V, allowing common-mode voltages on the line without affecting driver performance.

All outputs should be maintained within the recommended common-mode output voltage range to ensure that the channels do not interact with each other. To minimize power dissipation, all unused inputs should be grounded.

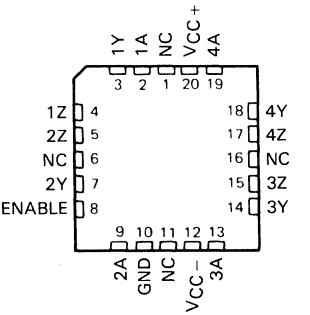
All inputs are diode clamped and are designed to satisfy TTL-system requirements. The inputs are tested at 2 V for high-logic-level input conditions and 0.8 V for low-logic-level input conditions. These tests guarantee 400 mV of noise margin when interfaced with Series 54/74 TTL.

The SN55111 is characterized for operation from −55°C to 125°C. The SN75111 is characterized for operation from 0°C to 70°C.

SN55111 . . . J PACKAGE
SN75111 . . . D, J, OR N PACKAGE
(TOP VIEW)

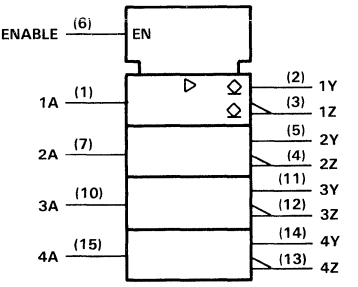


SN55111 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



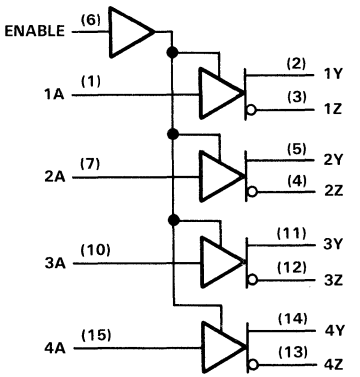
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

FUNCTION TABLE

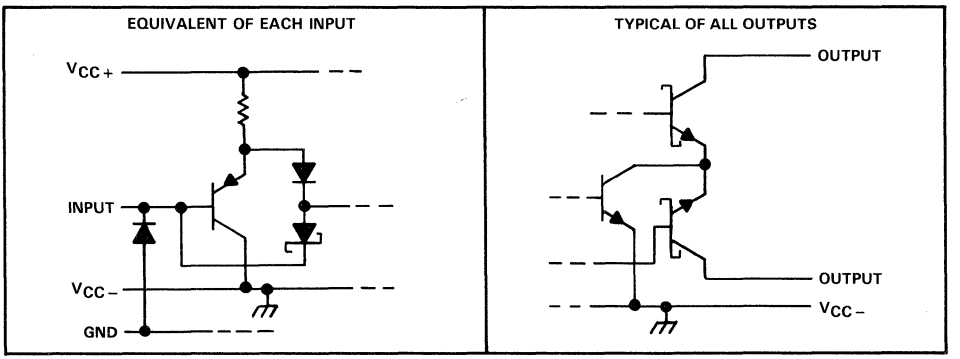
LOGIC INPUT	ENABLE INPUT	OUTPUT CURRENT Z	OUTPUT CURRENT Y
H	H	ON	OFF
L	H	OFF	ON
H	L	OFF	OFF
L	L	OFF	OFF

L = low logic level
H = high logic level

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 7 V
Supply voltage, V_{CC-} . . . . . −7 V
Input voltage (any input) . . . . . 5.5 V
Output voltage range (any output) . . . . . −5 V to 12 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN55111 . . . . . −55°C to 125°C
SN75111 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55111)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75111)	1025 mW	8.2 mW/°C	656 mW	N/A
N	1150 mW	9.2 mW/°C	736 mW	N/A

recommended operating conditions (see Note 2)

		SN55111			SN75111			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}	$T_A \ge 25°C$	4.5	5	5.5	4.75	5	5.25	V
	$T_A < 25°C$	4.75	5	5.5	4.75	5	5.25	
Supply voltage, V_{CC-}	$T_A \ge 25°C$	−4.5	−5	−5.5	−4.75	−5	−5.25	V
	$T_A < 25°C$	−4.75	−5	−5.5	−4.75	−5	−5.25	
High-level input voltage, V_{IH}		2		5.5	2		5.5	V
Low-level input voltage, V_{IL}		0		0.8	0		0.8	V
Common-mode output voltage range	V_{OCR+}	0		10	0		10	V
	V_{OCR-}	0		−3	0		−3	
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 2: All unused outputs should be grounded.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = MAX, V_{CC-} = MAX (unless otherwise noted)

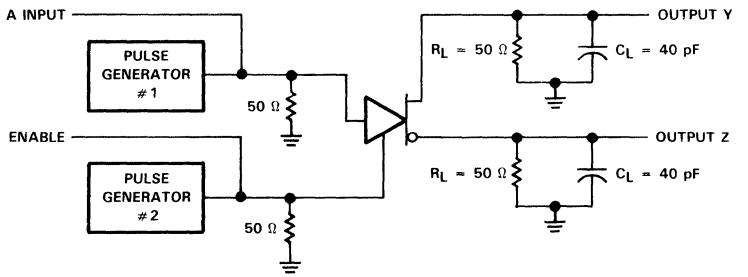
PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −12 mA			−0.9	−1.5	V
$I_{O(on)}$	On-state output current	V_{CC+} = MAX,	V_{CC-} = MAX		5.5	7	mA
		V_{CC+} = MIN,	V_{CC-} = MIN	3.5	5.5		
$I_{O(off)}$	Off-state output current	V_{CC+} = MIN,	V_{CC-} = MIN, V_O = 10V			100	μA
I_{IH}	High-level input current	V_I = 2.4 V				40	μA
		V_I = V_{CC+} MAX				1	mA
I_{IL}	Low-level input current	V_I = 0.4 V				−1.6	mA
I_{CC+}	Supply current from V_{CC+}	A inputs at 0.4 V	Enable at 2 V		28	40	mA
			Enable at 0.4 V		27	40	
I_{CC-}	Supply current from V_{CC-}	A inputs at 0.4 V	Enable at 2 V		−43	−55	mA
			Enable at 0.4 V		−25	−35	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, and T_A = 25°C.

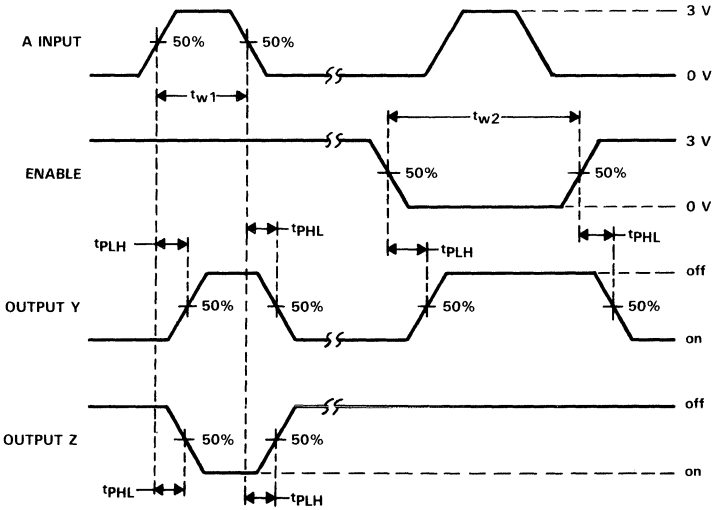
switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, R_L = 50 Ω, C_L = 40 pF, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y or Z	See Figure 1		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output	A	Y or Z			7	15	ns
t_{PLH}	Propagation delay time, low-to-high-level output	Enable	Y or Z			14	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output	Enable	Y or Z			15	25	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

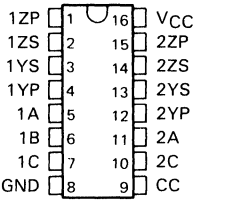
NOTES: A. The pulse generators have the following characteristics: $Z_O \approx 50\ \Omega$, $t_r = t_f = 10 \pm 5$ ns, $t_{w1} \leq 200$ ns, PRR ≤ 1 MHz, $t_{w2} \leq 1\ \mu s$, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

FIGURE 1. PROPAGATION DELAY TIMES

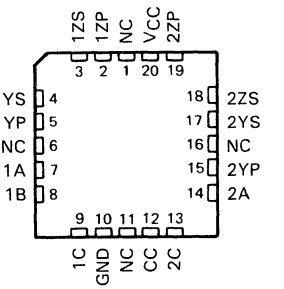
D1315, SEPTEMBER 1973—REVISED SEPTEMBER 1986

- **Choice of Open-Collector, Open-Emitter, or 3-State Outputs**
- **High-Impedance Output State for Party-Line Applications**
- **Single-Ended or Differential AND/NAND Outputs**
- **Single 5-V Supply**
- **Dual Channel Operation**
- **Compatible With TTL**
- **Short-Circuit Protection**
- **HIgh-Current Outputs**
- **Common and Individual Output Controls**
- **Clamp Diodes at Inputs and Outputs**
- **Easily Adaptable to SN55114 and SN75114 Applications**
- **Designed for Use With SN55115 and SN75115**

SN55113 . . . J PACKAGE
SN75113 . . . D, J, OR N PACKAGE
(TOP VIEW)



SN55113 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN55113 and SN75113 dual differential line drivers with 3-state outputs are designed to provide all the features of the SN55114 and SN75114 line drivers with the added feature of driver output controls. Individual controls are provided for each output pair, as well as a common control for both output pairs. If any output is low, the associated output is in a high-impedance state and the output can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pull-up terminals, YP and ZP, available on adjacent package pins.

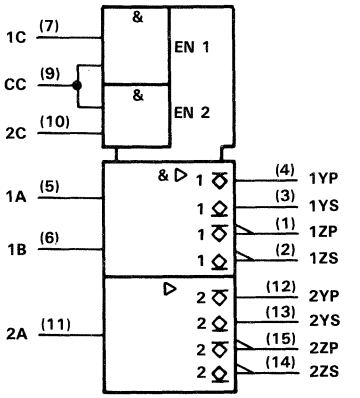
The SN55113 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75113 is characterized for operation over the temperature range of 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
OUTPUT CONTROL		DATA		AND	NAND
C	CC	A	B†	Y	Z
L	X	X	X	Z	Z
X	L	X	X	Z	Z
H	H	L	X	L	H
H	H	X	L	L	H
H	H	H	H	H	L

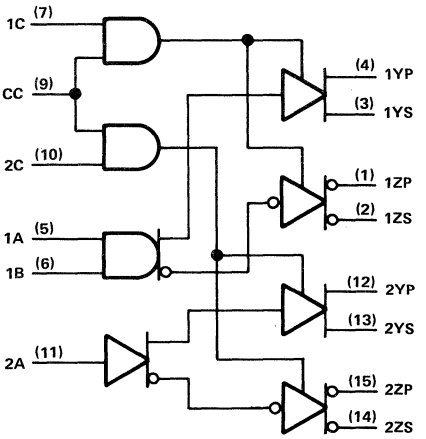
H = high level, L = low level, X = irrelevant,
Z = high impedance (off)
†B input and 4th line of function table are applicable only to driver number 1.

logic symbol†

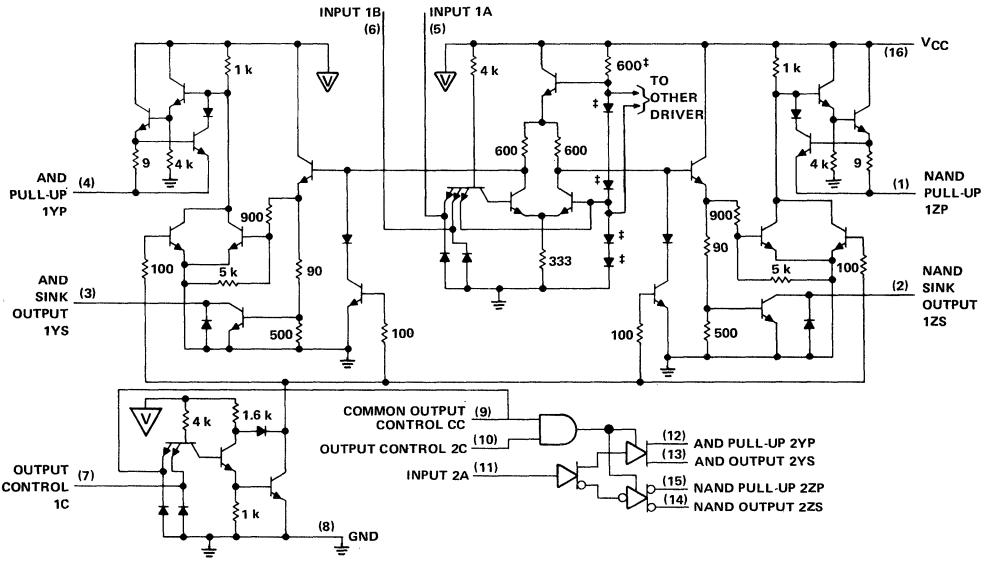


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



schematic



▽ . . . V_{CC} bus

‡These components common to both drivers.
Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state voltage applied to open-collector outputs . . . . . 12 V
Continuous total power dissipation (see Note 2) . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN55113 . . . . . −55°C to 125°C
SN75113 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. In the J and FK packages, SN55113 chips are alloy mounted; SN75113 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55113)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75113)	1025 mW	8.2 mW/°C	656 mW	N/A
N	1150 mW	9.2 mW/°C	736 mW	N/A

recommended operating conditions

	SN55113			SN75113			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

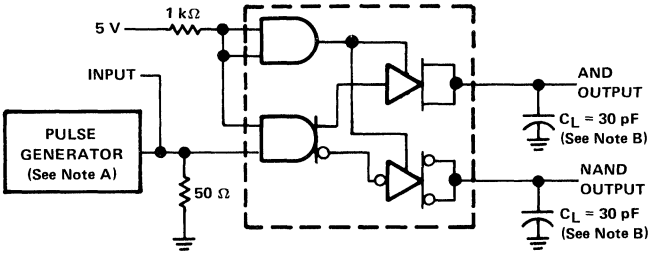
PARAMETER			TEST CONDITIONS†			SN55113			SN75113			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V		I_{OH} = −10 mA	2.4	3.4		2.4	3.4		V
					I_{OH} = −40 mA	2	3.0		2	3.0		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 40 mA				0.23	0.4		0.23	0.4	V
V_{OK}	Output clamp voltage		V_{CC} = MAX, I_O = −40 mA				−1.1	−1.5		−1.1	−1.5	V
$I_{O(off)}$	Off-state open-collector output current		V_{CC} = MAX	V_{OH} = 12 V	T_A = 25°C		1	10				μA
					T_A = 125°C			200				
				V_{OH} = 5.25 V	T_A = 25°C					1	10	
					T_A = 70°C						20	
I_{OZ}	Off-state (high-impedance-state) output current		V_{CC} = MAX, Output controls at 0.8 V	T_A = 25°C,	V_O = 0 to V_{CC}			±10			±10	μA
				T_A = MAX	V_O = 0			−150			−20	
					V_O = 0.4 V			±80			±20	
					V_O = 2.4 V			±80			±20	
					V_O = V_{CC}			80			20	
I_I	Input current at maximum input voltage	A, B, C	V_{CC} = MAX, V_I = 5.5 V					1			1	mA
		CC						2			2	
I_{IH}	High-level input current	A, B, C	V_{CC} = MAX, V_I = 2.4 V					40			40	μA
		CC						80			80	
I_{IL}	Low-level input current	A, B, C	V_{CC} = MAX, V_I = 0.4 V					−1.6			−1.6	mA
		CC						−3.2			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX, V_O = 0,		T_A = 25°C	−40	−90	−120	−40	−90	−120	mA
I_{CC}	Supply current (both drivers)		All inputs at 0 V, No load, T_A = 25°C		V_{CC} = MAX		47	65		47	65	mA
					V_{CC} = 7 V		65	85		65	85	

†All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output.
‡All typical values are at T_A = 25°C and V_{CC} = 5 V, with the exception of I_{CC} at 7 V.
§Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

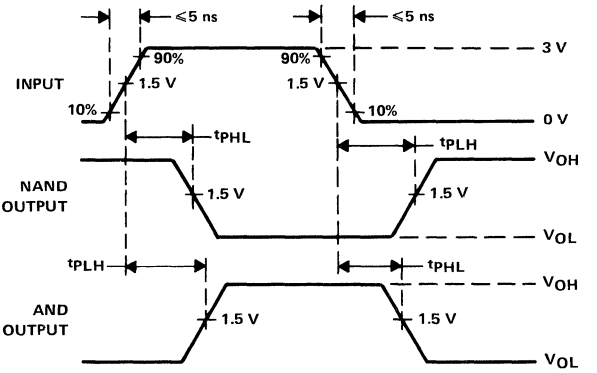
switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55113			SN75113			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 1		13	20		13	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	20		12	30	ns
t_{PZH}	Output enable time to high level	R_L = 180 Ω, See Figure 2		7	15		7	20	ns
t_{PZL}	Output enable time to low level	R_L = 250 Ω, See Figure 3		14	30		14	40	ns
t_{PHZ}	Output disable time from high level	R_L = 180 Ω, See Figure 2		10	20		10	30	ns
t_{PLZ}	Output disable time from low level	R_L = 250 Ω, See Figure 3		17	35		17	35	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



WAVEFORMS

FIGURE 1. t_{PLH} and t_{PHL}

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_W = 100 ns.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

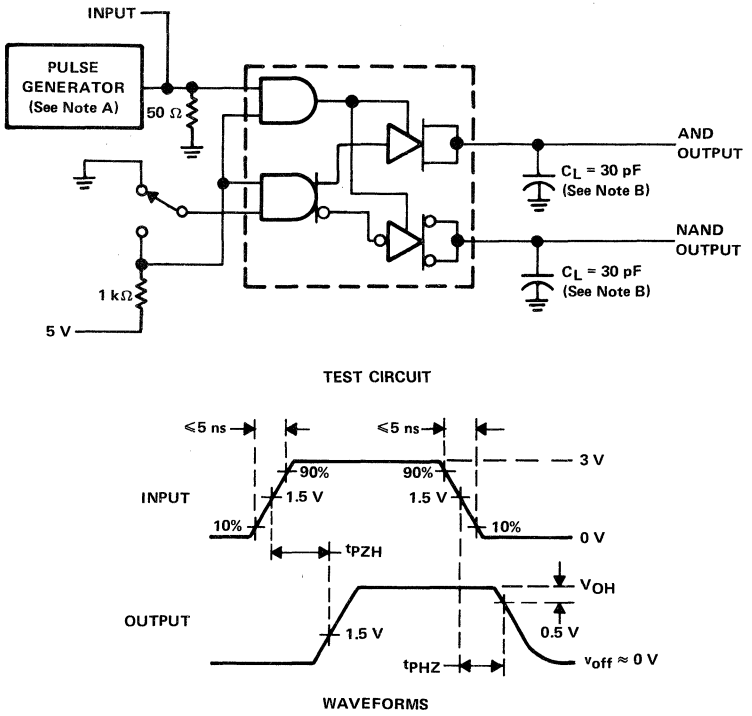
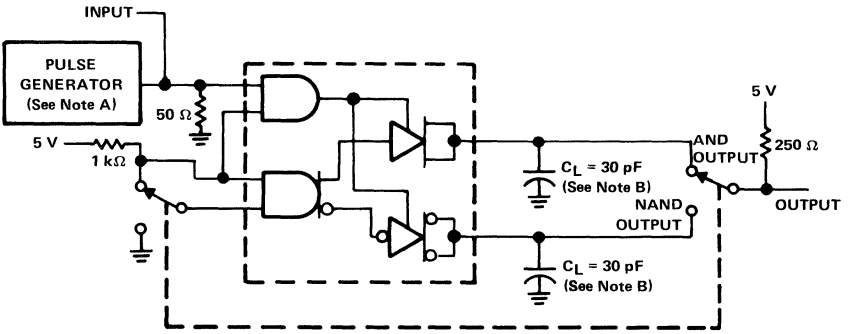


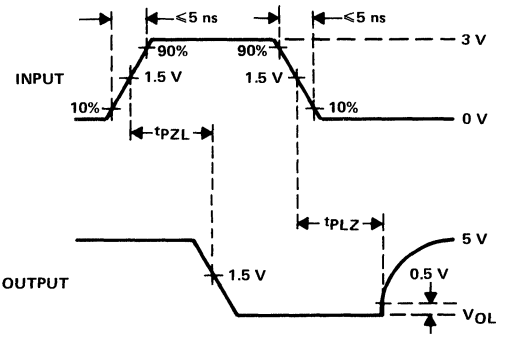
FIGURE 2. t_{PZH} and t_{PHZ}

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_W = 100 ns.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



WAVEFORMS

FIGURE 3. t_{PZL} and t_{PLZ}

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_W = 100 ns.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

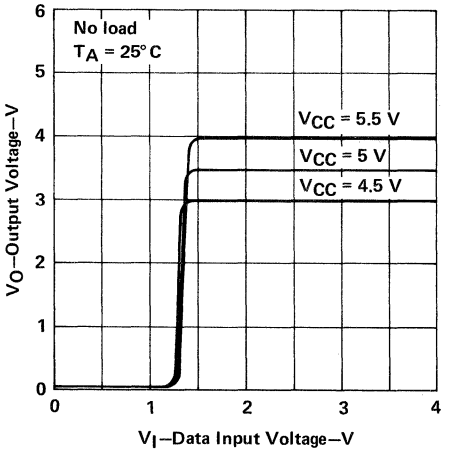


FIGURE 4

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

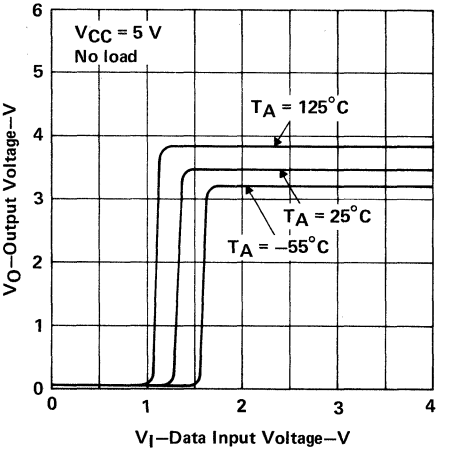


FIGURE 5

OUTPUT VOLTAGE
vs
OUTPUT CONTROL VOLTAGE

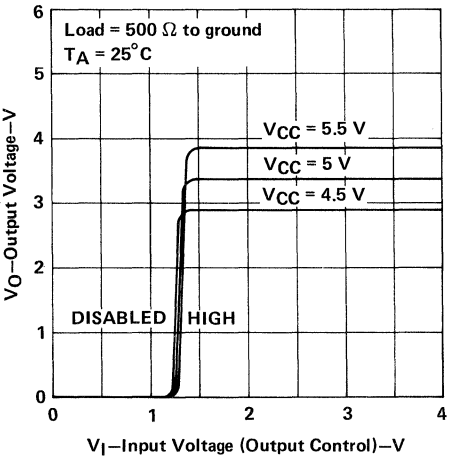


FIGURE 6

OUTPUT VOLTAGE
vs
OUTPUT CONTROL VOLTAGE

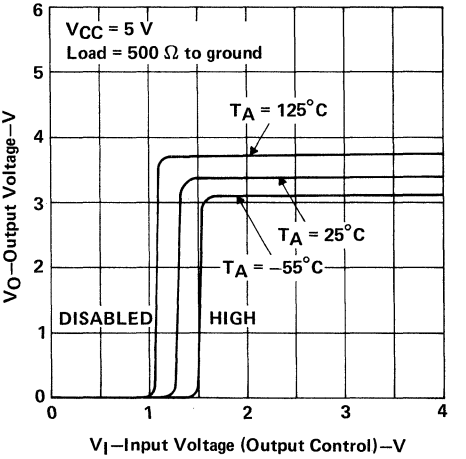


FIGURE 7

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
OUTPUT CONTROL VOLTAGE

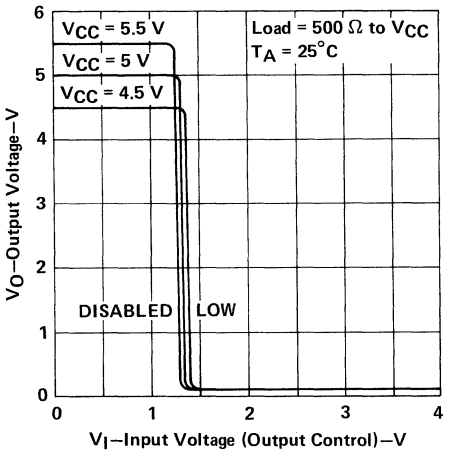


FIGURE 8

OUTPUT VOLTAGE
vs
OUTPUT CONTROL VOLTAGE

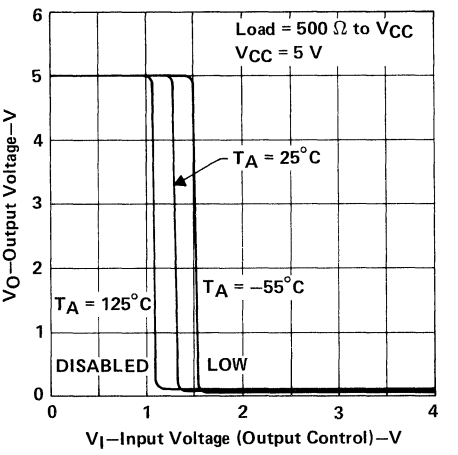


FIGURE 9

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

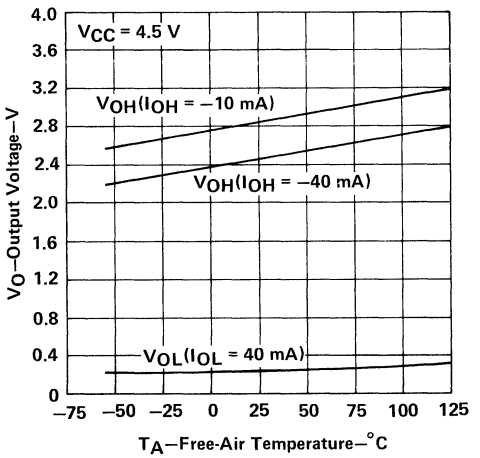


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

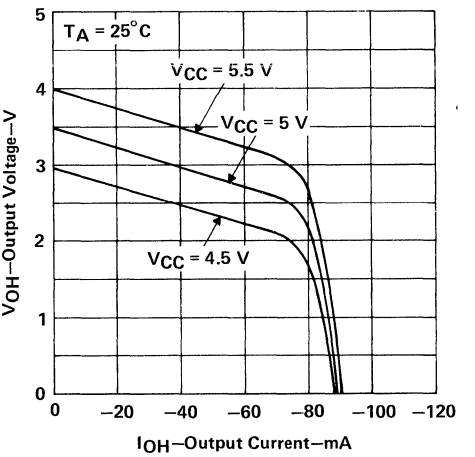


FIGURE 11

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

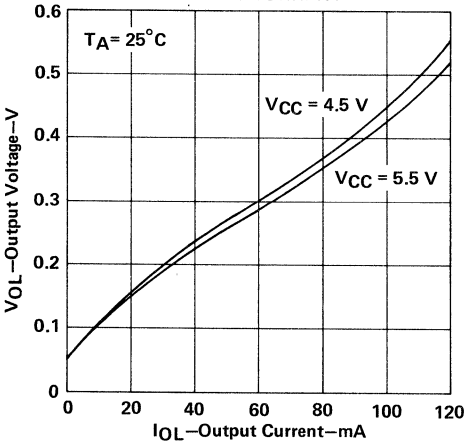


FIGURE 12

SUPPLY CURRENT
(BOTH DRIVERS)
vs
SUPPLY VOLTAGE

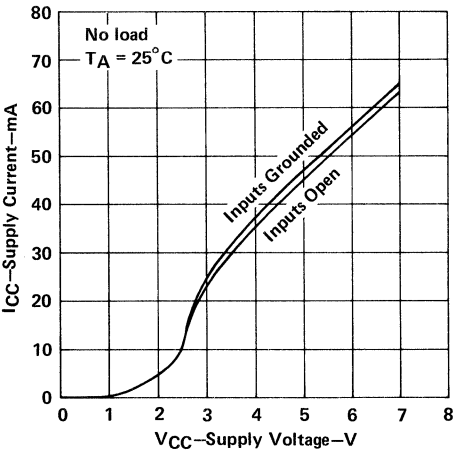


FIGURE 13

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREE-AIR TEMPERATURE

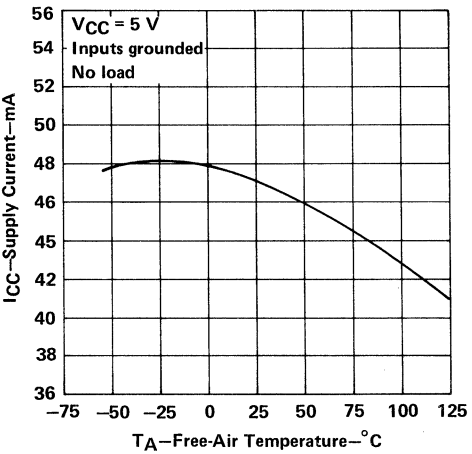


FIGURE 14

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREQUENCY

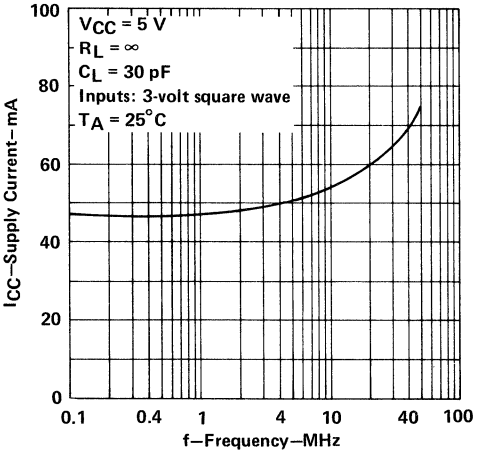


FIGURE 15

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIMES
FROM DATA INPUTS
vs
FREE-AIR TEMPERATURE

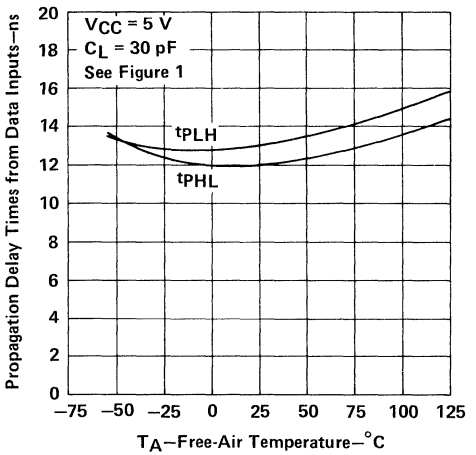


FIGURE 16

OUTPUT ENABLE AND DISABLE TIMES
vs
FREE-AIR TEMPERATURE

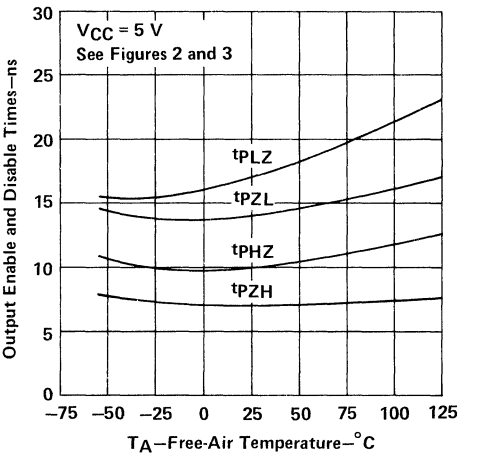
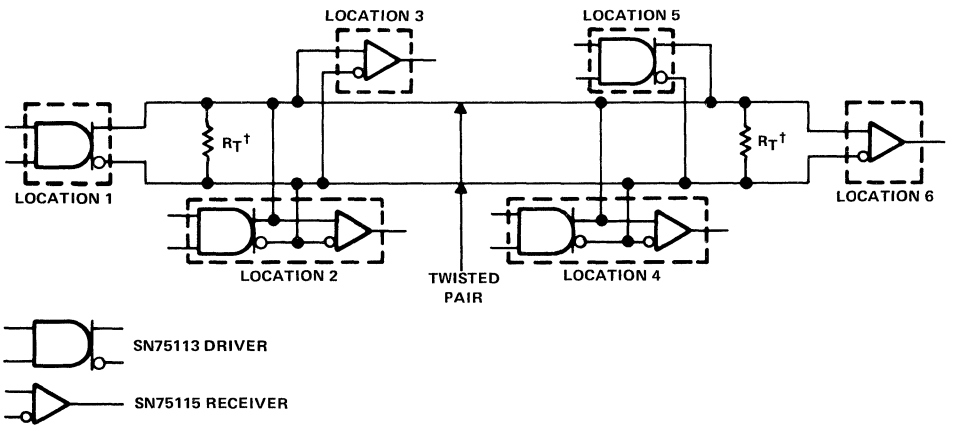


FIGURE 17

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

APPLICATION INFORMATION



†$R_T = Z_O$. A capacitor may be connected in series with R_T to reduce power dissipation.

FIGURE 18. BASIC PARTY-LINE OR DATA-BUS DIFFERENTIAL DATA TRANSMISSION

D1315, SEPTEMBER 1973—REVISED SEPTEMBER 1986

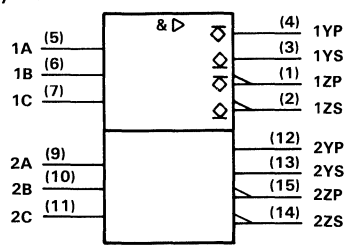
- **Choice of Open-Collector, Open-Emitter, or Totem-Pole Outputs**
- **Single-Ended or Differential AND/NAND Outputs**
- **Single 5-V Supply**
- **Dual-Channel Operation**
- **TTL-Compatible**
- **Short-Circuit Protection**
- **High-Current Outputs**
- **Triple Inputs**
- **Clamp Diodes at Inputs and Outputs**
- **Designed for Use with SN55115 and SN75115 Differential Line Receivers**
- **Designed to Be Interchangeable with Fairchild 9614 Line Driver**

description

The SN55114 and SN75114 dual differential line drivers are designed to provide differential output signals with the high-current capability for driving balanced lines, such as twisted pair, at normal line impedances without high power dissipation. The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pull-up terminals, YP and ZP, available on adjacent package pins. Since the output stages provide TTL-compatible output levels, these devices may also be used as TTL expanders or phase splitters.

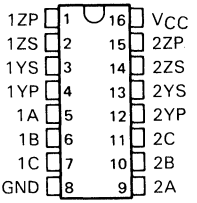
The SN55114 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75114 is characterized for operation from 0°C to 70°C.

logic symbol†

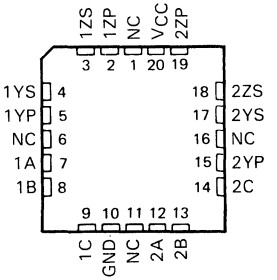


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN55114 . . . J PACKAGE
SN75114 . . . D, J, OR N PACKAGE
(TOP VIEW)



SN55114 . . . FK PACKAGE
(TOP VIEW)



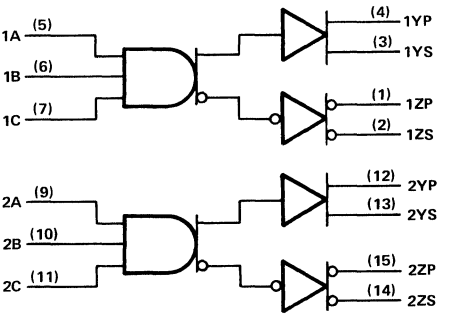
NC—No internal connection

FUNCTION TABLE

INPUTS			OUTPUTS	
A	B	C	Y	Z
H	H	H	H	L
ALL OTHER INPUT COMBINATIONS			L	H

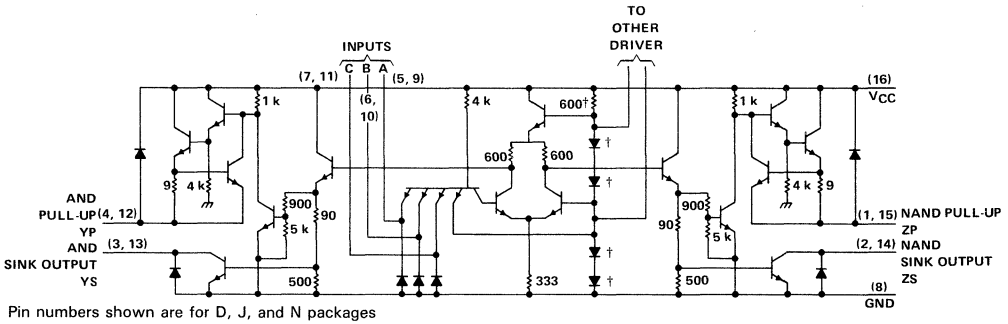
H = high level, L = low level

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

schematic (each driver)



Pin numbers shown are for D, J, and N packages

†These components are common to both drivers.
Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55114	SN75114	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	V
Input voltage	5.5	5.5	V
Off-state voltage applied to open-collector outputs	12	12	V
Continuous total power dissipation (see Note 2)	See Dissipation Rating Table		
Operating free-air temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. In the FK and J packages, SN55114 chips are either silver glass or alloy mounted. In the J package, SN75114 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°CC	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55114)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75115)	1025 mW	8.2 mW/°C	656 mw	—
N	1150 mW	9.2 mW/°C	736 mW	—

recommended operating conditions

	SN55114			SN75114			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC1}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

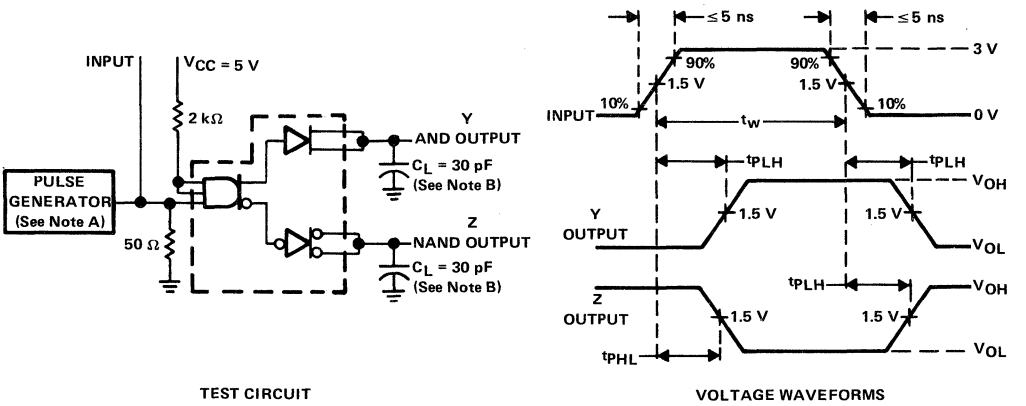
PARAMETER		TEST CONDITIONS†			SN55114			SN75114			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,		I_{OH} = −10 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = −40 mA	2	3		2	3		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 40 mA				0.2	0.4		0.2	0.45	V
V_{OK}	Output clamp voltage	V_{CC} = 5 V, I_O = 40 mA,		T_A = 25°C		6.1	6.5		6.1	6.5	V
		V_{CC} = MAX, I_O = −40 mA,		T_A = 25°C		−1.1	−1.5		−1.1	−1.5	
$I_{O(off)}$	Off-state open-collector output current	V_{CC} = MAX	V_{OH} = 12 V	T_A = 25°C		1	100				μA
				T_A = 125°C			200				
			V_{OH} = 5.25 V	T_A = 25°C					1	100	
				T_A = 70°C						200	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V					40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.1	−1.6		−1.1	−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_O = 0,		T_A = 25°C	−40	−90	−120	−40	−90	−120	mA
I_{CC}	Supply current (both drivers)	All inputs at 0 V, No load, T_A = 25°C		V_{CC} = MAX		37	50		37	50	mA
				V_{CC} = 7 V		47	65		47	70	

†All parameters with the exception of off-state open-collector output current are measured with the active pullup connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at T_A = 25°C and V_{CC} = 5 V, with the exception of I_{CC} at 7 V.
§Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55114			SN75114			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 1		15	20		15	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			11	20		11	30	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 500 Ω, PRR ≤ 500 kHz, t_W ≤ 100 ns.
B. C_L includes probe and jig capacitance.

FIGURE 1. PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS†

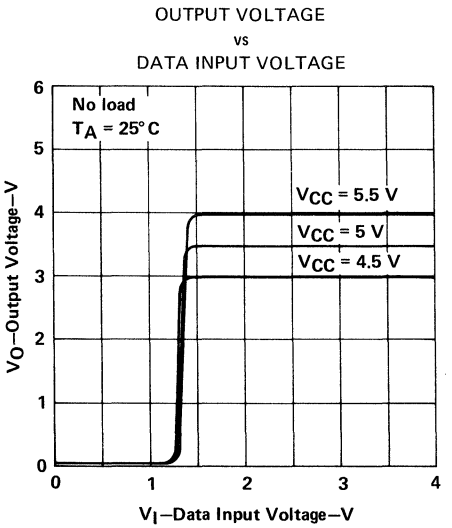


FIGURE 2

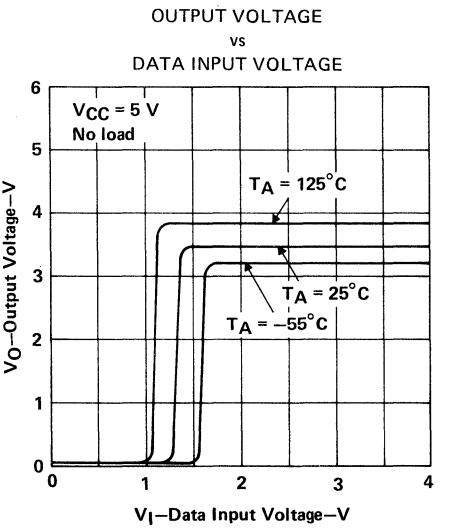


FIGURE 3

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55114 circuits only. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

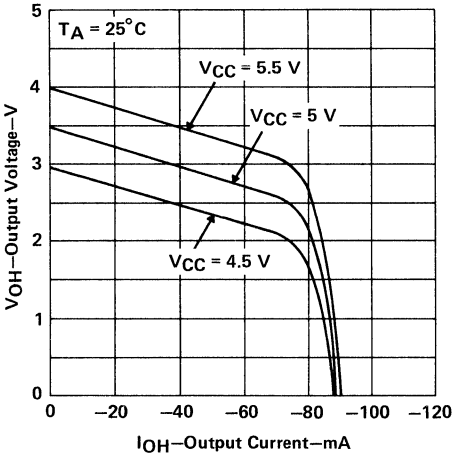


FIGURE 4

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

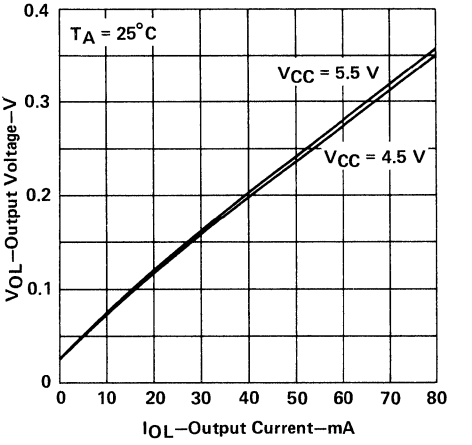


FIGURE 5

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

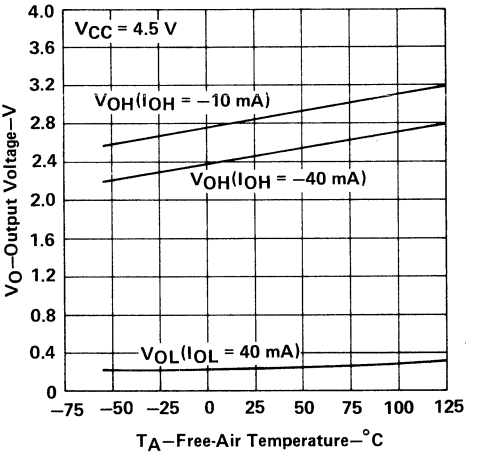


FIGURE 6

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

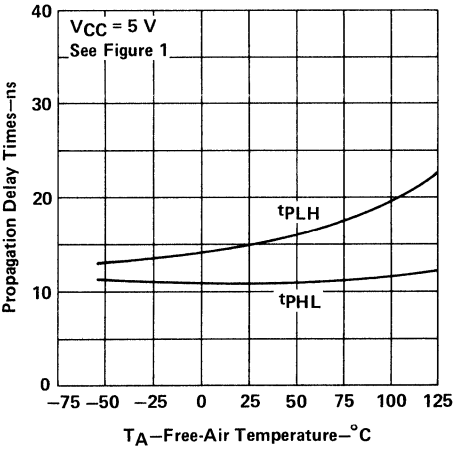


FIGURE 7

† Data for temperatures below 0°C and above 70°C are applicable to SN55114 circuits only. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
(BOTH DRIVERS)
vs
SUPPLY VOLTAGE

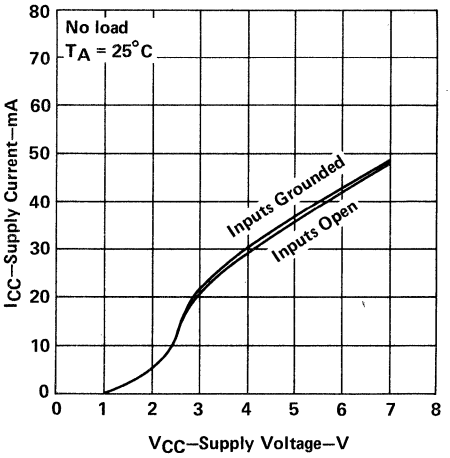


FIGURE 8

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREE-AIR TEMPERATURE

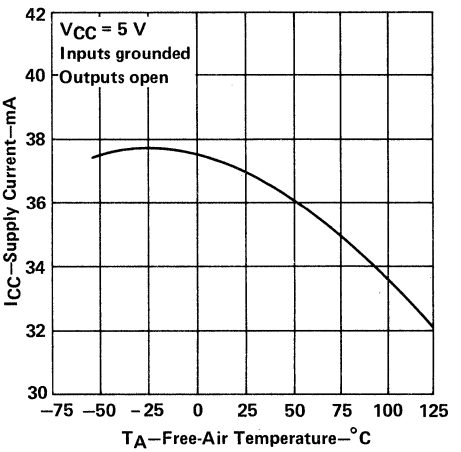


FIGURE 9

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREQUENCY

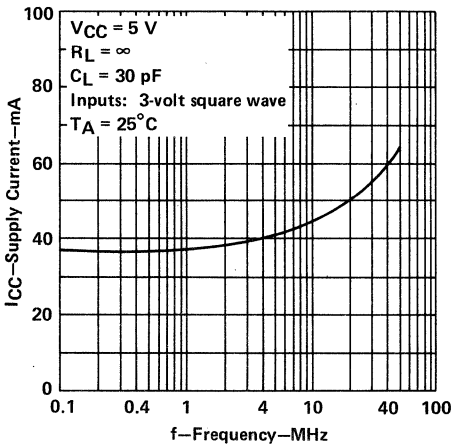
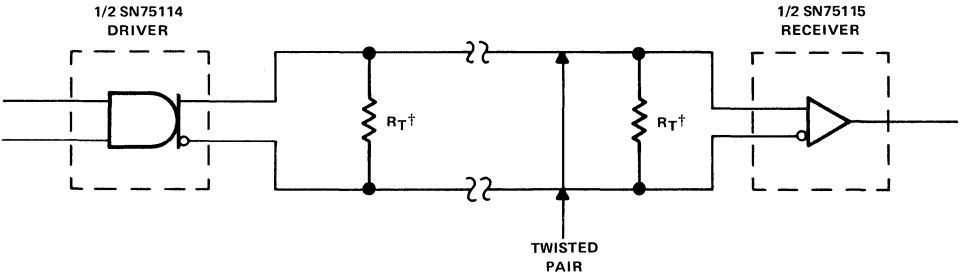


FIGURE 10

† Data for temperatures below 0°C and above 70°C are applicable to SN55114 circuits only. These parameters were measured with the active pullup connected to the sink output.

APPLICATION INFORMATION†



†$R_T = Z_O$. A capacitor may be connected in series with R_T to reduce power dissipation.

FIGURE 11. BASIC PARTY-LINE OR DATA-BUS DIFFERENTIAL DATA TRANSMISSION

D1315, SEPTEMBER 1973—REVISED OCTOBER 1986

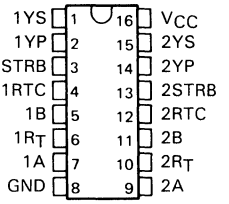
- **Choice of Open-Collector or Active Pull-Up (Totem-Pole) Outputs**
- **Single 5-V Supply**
- **Differential Line Operation**
- **Dual-Channel Operation**
- **TTL Compatible**
- **±15 V Common-Mode Input Voltage Range**
- **Optional-Use Built-In 130-Ω Line-Terminating Resistor**
- **Individual Frequency Response Controls**
- **Individual Channel Strobes**
- **Designed for Use With SN55113, SN75113, SN55114, and SN75114 Drivers**
- **Designed to Be Interchangeable With Fairchild 9615 Line Receivers**

description

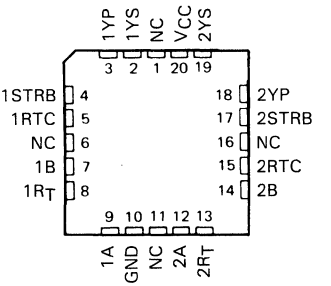
The SN55115 and SN75115 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL-compatible output signals as a function of the differential input voltage. The open-collector output configuration permits the wire-ANDing of similar TTL outputs (such as SN5401/SN7401) or other SN55115/SN75115 line receivers. This permits a level of logic to be implemented without extra delay. The output stages are similar to TTL totem-pole outputs, but with sink outputs, 1YS and 2YS, and the corresponding active pull-up terminals, 1YP and 2YP, available on adjacent package pins. The frequency response and noise immunity may be provided by a single external capacitor. A strobe input is provided for each channel. With the strobe in the low level, the receiver is disabled and the outputs are forced to a high level.

The SN55115 is characterized for operation over the full military range of −55°C to 125°C. The SN75115 is characterized for operation from 0°C to 70°C.

SN55115 . . . J PACKAGE
SN75115 . . . D, J, OR N PACKAGE
(TOP VIEW)



SN55115 . . . FK PACKAGE
(TOP VIEW)



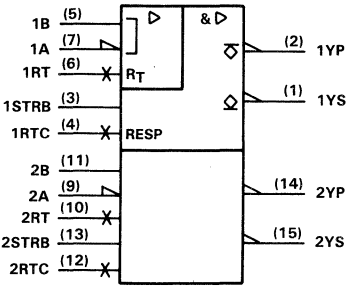
NC—No internal connection

FUNCTION TABLE

STROBE	DIFF INPUT	OUTPUT (YP AND YS TIED TOGETHER)
L	X	H
H	L	H
H	H	L

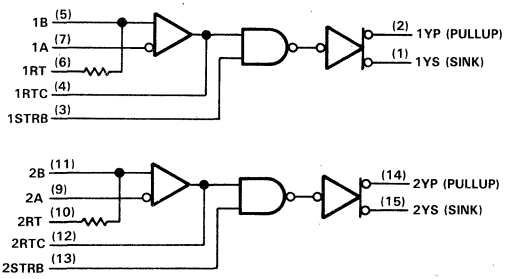
H = $V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max
L = $V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max
X = irrelevant

logic symbol†

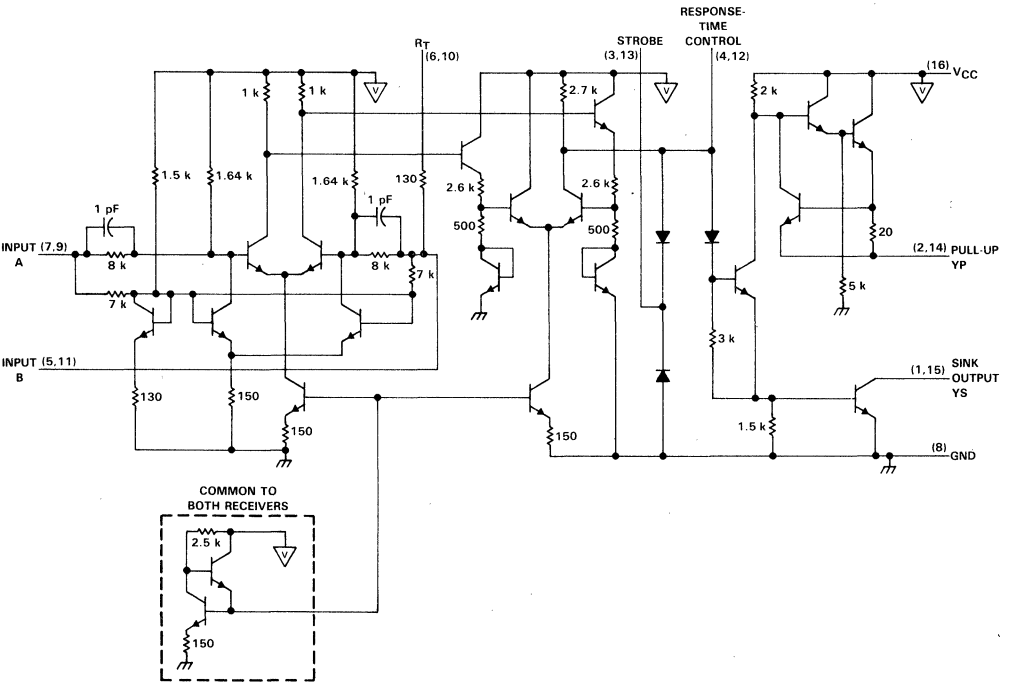


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each receiver)



Pin numbers shown are for D, J, and N packages.
Resistor values are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55115	SN75115	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	V
Input voltage at A, B, and R_T inputs	±25	±25	V
Input voltage at strobe input	5.5	5.5	V
Off-state voltage applied to open-collector outputs	14	14	V
Continuous total power dissipation (see Note 2)	See Dissipation Rating Table		
Operating free-air temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260	°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. In the FK and J packages, SN55115 chips are either silver glass or alloy mounted and SN75115 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55115)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75115)	1025 mW	8.2 mW/°C	656 mW	—
N	1150 mW	9.2 mW/°C	736 mW	—

recommended operating conditions

	SN55115			SN75115			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level (strobe) input voltage, V_{IH}	2.4			2.4			V
Low-level (strobe) input voltage, V_{IL}			0.4			0.4	V
High-level output current, I_{OH}			−5			−5	mA
Low-level output current, I_{OL}			15			15	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN55115			SN75115			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{TH}§	Differential input high-threshold voltage	V_O = 0.4 V, I_{OL} = 15 mA, V_{IC} = 0				500			500	mV
V_{TL}§	Differential input low-threshold voltage	V_O = 2.4 V, I_{OH} = −5 mA, V_{IC} = 0		−500¶			−500¶			mV
V_{ICR}	Common-mode input voltage range	V_{ID} = ±1 V		+15 to −15	+24 to −19		+15 to −15	+24 to −19		V
V_{OH}	HIgh-level output voltage	V_{CC} = MIN, V_{ID} = −0.5 V, I_{OH} = −5 mA	T_A = MIN	2.2			2.4			V
			T_A = 25°C	2.4	3.4		2.4	3.4		
			T_A = MAX	2.4			2.4			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{ID} = 0.5 V, I_{OL} = 15 mA			0.22	0.4		0.22	0.45	V
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V, Other input at 5.5 V	T_A = MIN			−0.9			−0.9	mA
			T_A = 25°C		−0.5	−0.7		−0.5	−0.7	
			T_A = MAX			−0.7			−0.7	
I_{SH}	High-level strobe current	V_{CC} = MIN, V_{ID} = −0.5 V, V_{strobe} = 4.5 V	T_A = 25°C			2			5	μA
			T_A = MAX			5			10	
I_{SL}	Low-level strobe current	V_{CC} = MAX, V_{ID} = 0.5 V, V_{strobe} = 0.4 V	T_A = 25°C		−1.15	−2.4		−1.15	−2.4	mA
$I_{(RTC)}$	Response-time-control current	V_{CC} = MAX, V_{ID} = 0.5 V, V_{RC} = 0	T_A = 25°C	−1.2	−3.4		−1.2	−3.4		mA
$I_{O(off)}$	Off-state open-collector output current	V_{CC} = MIN, V_{OH} = 12 V, V_{ID} = −4.5 V	T_A = 25°C			100				μA
			T_A = MAX			200				
		V_{CC} = MIN, V_{OH} = 5.25 V, V_{ID} = −4.75 V	T_A = 25°C						100	
			T_A = MAX						200	
R_T	Line-terminating resistance	V_{CC} = 5 V	T_A = 25°C	77	130	167	74	130	179	Ω
I_{OS}	Short-circuit output current‖	V_{CC} = MAX, V_O = 0, V_{ID} = −0.5 V	T_A = 25°C	−15	−40	−80	−14	−40	−100	mA
I_{CC}	Supply current (both receivers)	V_{CC} = MAX, V_{ID} = 0.5 V, V_{IC} = 0	T_A = 25°C		32	50		32	50	mA

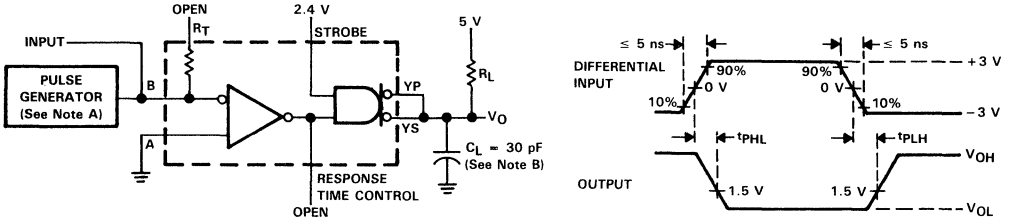
† Unless otherwise noted V_{strobe} = 2.4 V. All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.
§ Differential voltages are at the B input terminal with respect to the A input terminal.
¶ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.
‖ Only one output should be shorted to ground at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55115			SN75115			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 3.9 kΩ, See Figure 1		18	50		18	75	ns
t_{PHL}	Propagation delay time, high-to-low-level output	R_L = 390 Ω, See Figure 1		20	50		20	75	ns

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT **WAVEFORMS**

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_W ≤ 100 ns, duty cycle = 50%.
B. C_L includes probe and jig capacitance.

FIGURE 1. PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

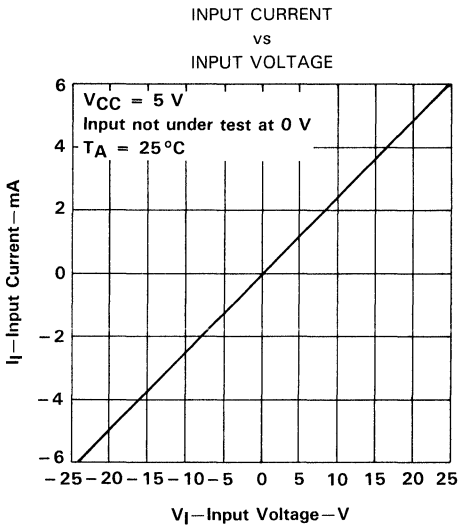


FIGURE 2

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

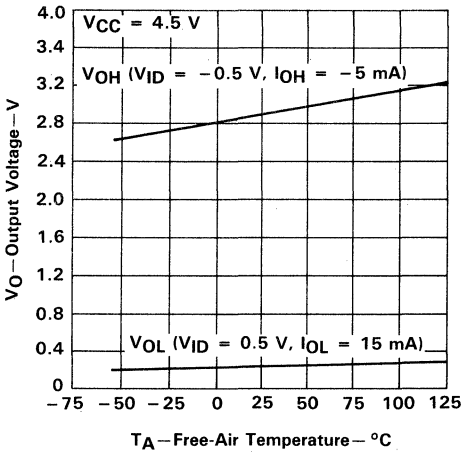


FIGURE 3

OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

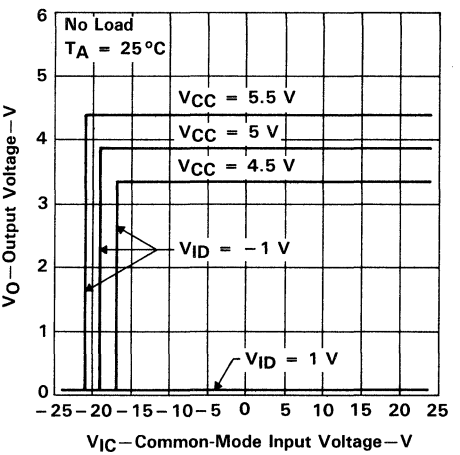


FIGURE 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

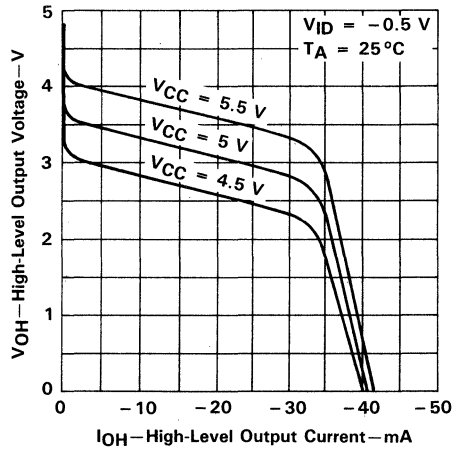


FIGURE 5

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

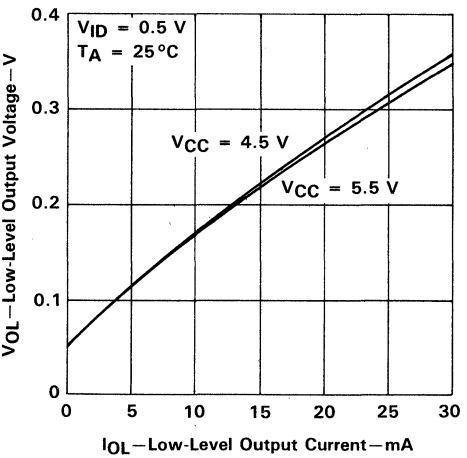


FIGURE 6

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pull-up connected to the sink output.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

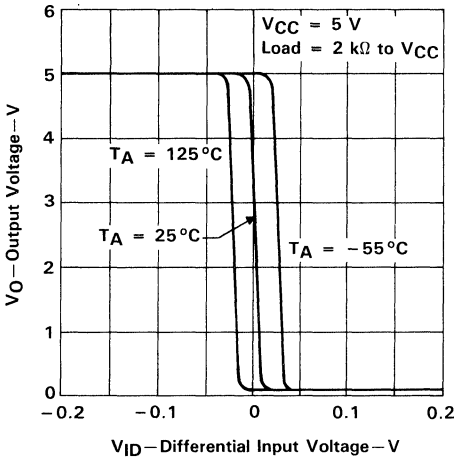


FIGURE 7

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

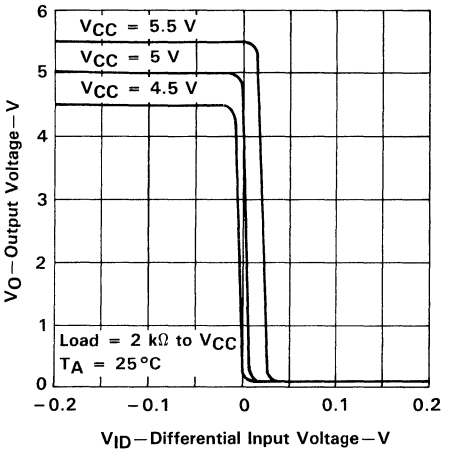


FIGURE 8

OUTPUT VOLTAGE
vs
STROBE INPUT VOLTAGE

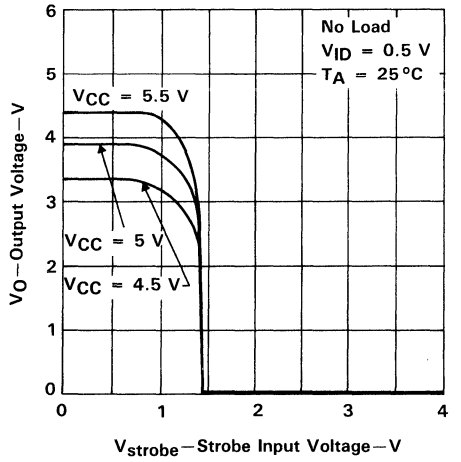


FIGURE 9

OUTPUT VOLTAGE
vs
STROBE INPUT VOLTAGE

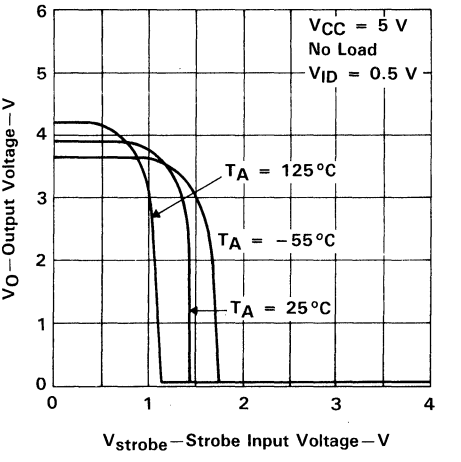


FIGURE 10

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pull up connected to the sink output.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
(BOTH RECEIVERS)
vs
SUPPLY VOLTAGE

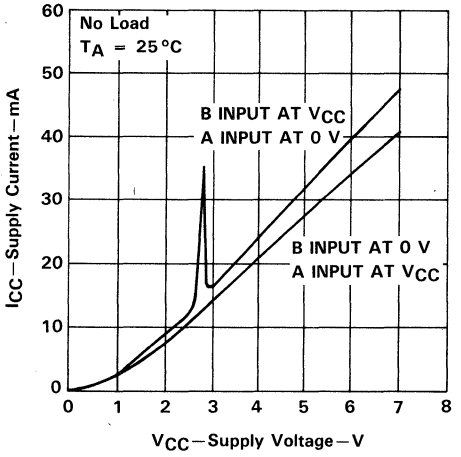


FIGURE 11

SUPPLY CURRENT
(BOTH RECEIVERS)
vs
FREE-AIR TEMPERATURE

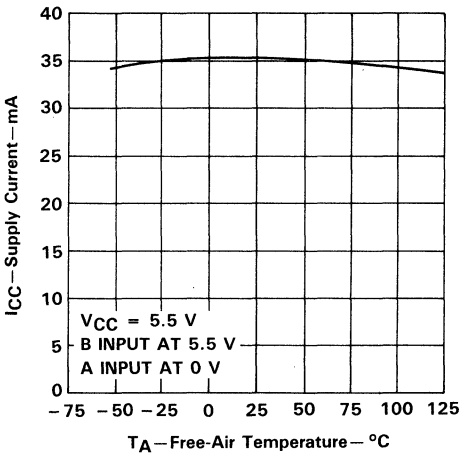


FIGURE 12

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

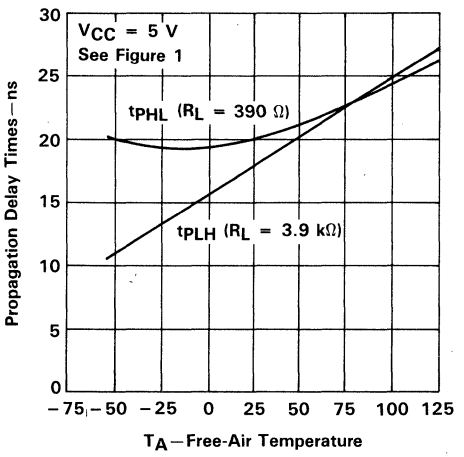


FIGURE 13

MAXIMUM OPERATING FREQUENCY
vs
RESPONSE-TIME-CONTROL CAPACITANCE

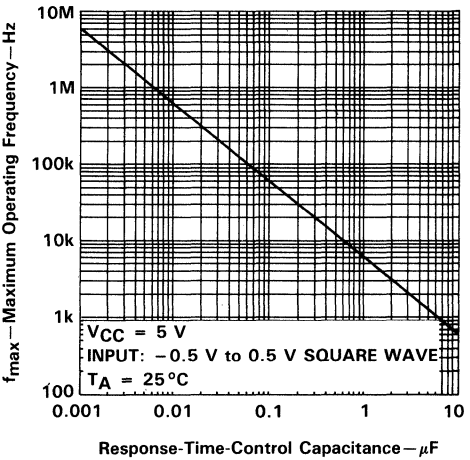
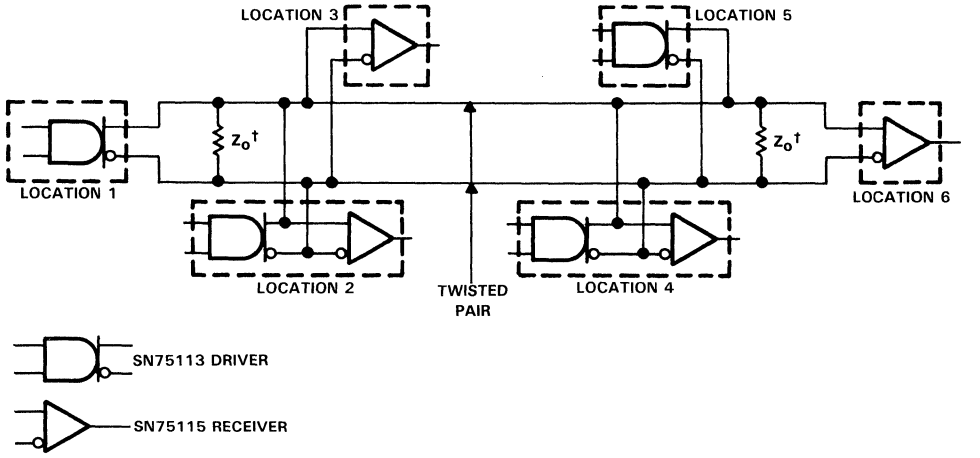


FIGURE 14

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pull-up connected to the sink output.

APPLICATION INFORMATION



†A capacitor may be connected in series with Z_O to reduce power dissipation.

FIGURE 15. BASIC PARTY-LINE OR DATA-BUS DIFFERENTIAL DATA TRANSMISSION

D2143, MAY 1976—REVISED MAY 1990

Features common to all types

- Single 5-V Supply
- 3-State Driver Output Circuitry
- TTL-Compatible Driver Inputs
- TTL-Compatible Receiver Output
- Differential Line Operation
- Receiver Output Strobe ('116, SN75117) or Enable (SN75118, SN75119)
- Designed for Party-Line (Data-Bus) Applications
- Choice of Ceramic or Plastic Packages

Additional features of the SN55116/SN75116

- Independent Driver and Receiver
- Choice of Open-Collector or Totem-Pole Outputs on Both Driver and Receiver
- Dual Data Inputs on Driver
- Optional Line-Termination Resistor in Receiver
- ±15-V Receiver Common-Mode Capability
- Receiver Frequency Response Control

Additional features of the SN75117

- Driver Output Internally Connected to Receiver Input

The SN75118 is an SN75116 with 3-State Receiver Output Circuitry
The SN75119 is an SN75117 with 3-State Receiver Output Circuitry

description

These integrated circuits are designed for use in interfacing between TTL-type digital systems and differential data transmission lines. They are especially useful for party-line (data-bus) applications. Each of these circuit types combine in one package a 3-state differential line driver and a differential-input line receiver, both of which operate from a single 5-V power supply. The driver inputs and receiver outputs are TTL compatible. The driver employed is similar to the SN55113/SN75113 3-state line driver, and the receiver is similar to the SN55115/SN75115 line receiver.

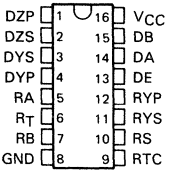
The '116 and SN75118 circuits offer all the features of the SN55113/SN75113 driver and the SN55115/SN75115 receiver combined. The driver performs the dual input AND and NAND functions when enabled, or presents a high impedance to the load when in the disabled state. The driver output stages are similar to TTL totem-pole outputs, but have the current-sink portion separated from the current-sourcing portion and both are brought out to adjacent package pins. This feature allows the user the option of using the driver in the open-collector output configuration, or, by connecting the adjacent source and sink pins together, of using the driver in the normal totem-pole output configuration.

The receiver portion of the '116 and SN75118 features a differential-input circuit having a common-mode voltage range of ±15 V. An internal 130-Ω resistor is also provided, which may optionally be used for terminating the transmission line. A frequency response control pin allows the user to reduce the speed of the receiver or to improve differential noise immunity. The receiver of the '116 also has an output strobe and a split totem-pole output. The receiver of the SN75118 has an output-enable for the 3-state split totem-pole output. The receiver section of either circuit is independent of the driver section except for the V_{CC} and ground pins.

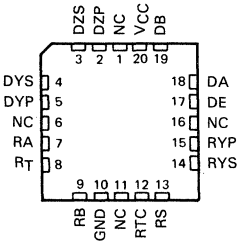
The SN75117 and SN75119 circuits provide the basic driver and receiver functions of the '116 and SN75118, but use a package that is only half as large. The SN75117 and SN75119 are intended primarily for party-line or bus-organized systems as the driver outputs are internally connected to the receiver inputs. The driver has a single data input and a single enable input, and the SN75117 receiver has an output strobe while the SN75119 receiver has a 3-state-output enable. These devices do not, however, provide output connection options, line termination resistors, or receiver frequency-response controls.

The SN55116 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN75116, SN75117, SN75118, and SN75119 are characterized for operation from 0°C to 70°C.

SN55116 . . . J PACKAGE
SN75116 . . . D, J, OR N PACKAGE
(TOP VIEW)

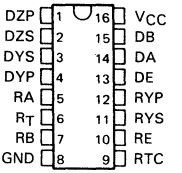


SN55116
FK PACKAGE
(TOP VIEW)

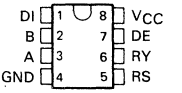


NC—No internal connection

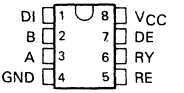
SN75118 . . . D, J, OR N PACKAGE
(TOP VIEW)



SN75117 . . . D, JG, OR P PACKAGE
(TOP VIEW)



SN75119 . . . D, JG, OR P PACKAGE
(TOP VIEW)



'116, SN75118
FUNCTION TABLE
OF DRIVER

INPUTS			OUTPUTS	
DE	DA	DB	DY	DZ
L	X	X	Z	Z
H	L	X	L	H
H	X	L	L	H
H	H	H	H	L

SN75117, SN75119
FUNCTION TABLE
OF DRIVER

INPUTS		OUTPUTS	
DI	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

'116, SN75118
FUNCTION TABLE OF RECEIVER

RS/RE	DIFF INPUT	OUTPUT RY	
		'116	SN75118
L	X	H	Z
H	L	H	H
H	H	L	L

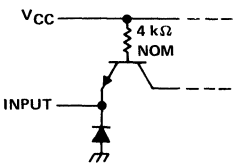
SN75117, SN75119
FUNCTION TABLE OF RECEIVER

INPUTS			OUTPUT RY	
A	B	RS/RE	SN75117	SN75119
H	L	H	H	H
L	H	H	L	L
X	X	L	H	Z

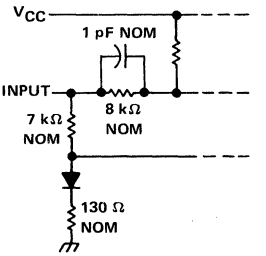
H = high level ($V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max)
L = low level ($V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max)
X = irrelevant
Z = high impedance (off)

schematics of inputs and outputs

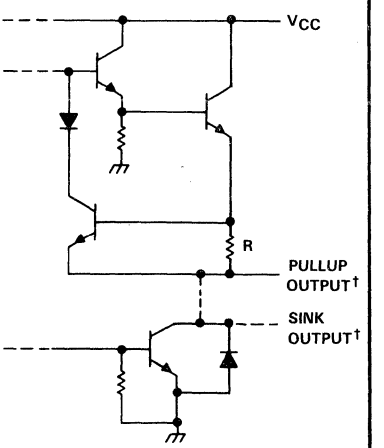
EQUIVALENT OF
EACH DRIVER INPUT
AND EACH RE AND RS INPUT



EQUIVALENT OF
EACH RECEIVER INPUT
(EXCLUDING ENABLES
AND STROBES)



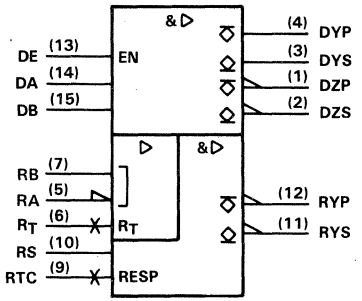
TYPICAL OF ALL OUTPUTS



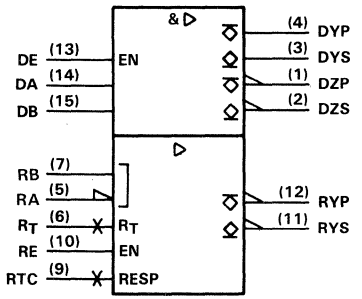
Driver output R = 9 Ω NOM
Receiver output R = 20 Ω NOM
†On SN75117 and SN75119, common outputs replace the separate pullup and sink outputs.

logic symbols†

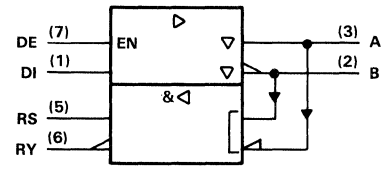
'116



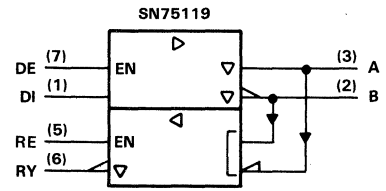
SN75118



SN75117

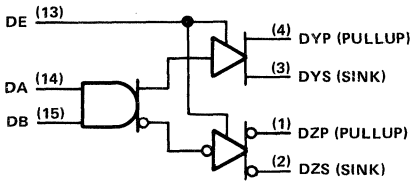


SN75119

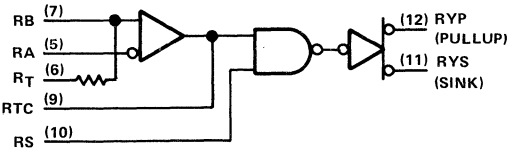


logic diagrams (positive logic)

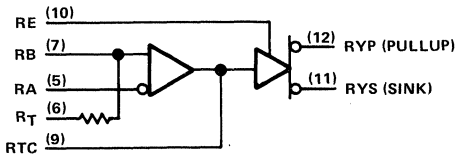
'116 AND SN75118



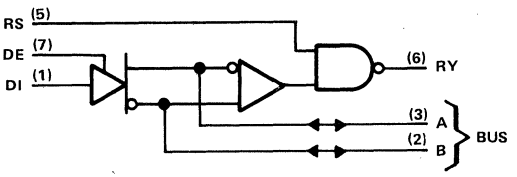
'116 RECEIVER



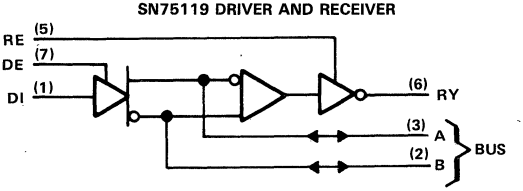
SN75118 RECEIVER



SN75117 DRIVER AND RECEIVER



SN75119 DRIVER AND RECEIVER



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown for '116 and SN75118 are for J and N packages; those shown for SN75117 and SN75119 are for JG and P packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		'116, SN75118	SN75117, SN75119	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage, V_I	DA, DB, DE, DI, RE, RS	5.5	5.5	V
	RA, RB, RT	±25		
	A and B		0 to 6	
Off-state voltage applied to open-collector outputs		12		V

	SN55116	SN75116 THRU SN75119	UNIT
Continuous total power dissipation (see Note 2)	See Dissipation Rating Table		
Operating free-air temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J and JG packages	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or P package		260	°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. In the FK and J packages, SN55116 chip is alloy mounted and SN75116 through SN75119 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8 pin)	725 mW	5.8 mW/°C	464 mW	—
D (16 pin)	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55116)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (all others)	1025 mW	8.2 mW/°C	656 mW	—
JG	825 mW	6.6 mW/°C	528 mW	—
N	1150 mW	9.2 mW/°C	736 mW	—
P	1000 mW	8.0 mW/°C	640 mW	—

recommended operating conditions

PARAMETER		SN55116			SN75'			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	All inputs except differential inputs	2			2			V
Low-level input voltage, V_{IL}				0.8			0.8	V
High-level output current, I_{OH}	Drivers			−40			−40	mA
	Receivers			−5			−5	
Low-level output current, I_{OL}	Drivers			40			40	mA
	Receivers			15			15	
Receiver input voltage, V_I	'116, '118			±15			±15	V
	'117, '119	0		6	0		6	
Common mode receiver input voltage, V_{ICR}	'116, '118			±15			±15	V
	'117, '119	0		6	0		6	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

driver section

PARAMETER		TEST CONDITIONS†			'116, SN75118			SN75117, SN75119			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	T_A = 25°C (SN55116)	I_{OH} = −10 mA	2.4	3.4		2.4	3.4		V
			T_A = 0°C to 70°C (SN75′)	I_{OH} = −40 mA	2	3		2	3		
			T_A = −55°C to 125°C	I_{OH} = −10 mA	2			2			
			(SN55116)	I_{OH} = −40 mA	1.8			1.8			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 40 mA					0.4			0.4	V
V_{OK}	Output clamp voltage	V_{CC} = MAX, I_O = −40 mA, DE at 0.8 V					−1.5			−1.5	V
$I_{O(off)}$	Off-state open-collector output current	V_{CC} = MAX, V_O = 12 V	T_A = 25°C			1	10				μA
			T_A = MAX	SN55116			200				
				SN75′			20				
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MAX, V_O = 0 to V_{CC}, DE at 0.8 V, T_A = 25°C					±10				μA
		V_{CC} = MAX, DE at 0.8 V, T_A = MAX	V_O = 0	SN55116			−300				
			V_O = 0.4 V to V_{CC}	SN55116			±150				
			V_O = 0 to V_{CC}	SN75′			±20				
I_I	Input current at maximum input voltage	Driver or enable input	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.4 V				40			40	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}	Short-circuit output current§		V_{CC} = MAX, V_O = 0, T_A = 25°C		−40		−120	−40		−120	mA
I_{CC}	Supply current (driver and receiver combined)	V_{CC} = MAX, T_A = 25°C				42	60		42	60	mA

†All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V and T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

driver section

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 13			14	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output				12	30	
t_{PZH}	Output enable time to high level	R_L = 180 Ω,	See Figure 14		8	20	ns
t_{PZL}	Output enable time to low level	R_L = 250 Ω,	See Figure 15		17	40	ns
t_{PHZ}	Output disable time from high level	R_L = 180 Ω,	See Figure 14		16	30	ns
t_{PLZ}	Output disable time from low level	R_L = 250 Ω,	See Figure 15		20	35	ns

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

receiver section

PARAMETER			TEST CONDITIONS†			'116, SN75118 MIN	'116, SN75118 TYP‡	'116, SN75118 MAX	SN75117, SN75119 MIN	SN75117, SN75119 TYP‡	SN75117, SN75119 MAX	UNIT
V_{TH}	Differential input high-threshold voltage§		V_O = 0.4 V, See Note 3	I_{OL} = 15 mA,	V_{CC} = MIN, V_{ICR} = 0, See Note 4			0.5			0.5	V
					V_{CC} = 5 V, V_{ICR} = MAX, See Note 5			1			1	
V_{TL}	Differential input low-threshold voltage§		V_O = 2.4 V, See Note 3	I_{OH} = −5 mA,	V_{CC} = MIN, V_{ICR} = 0, See Note 4	−0.5¶			−0.5¶			V
					V_{CC} = 5 V, V_{ICR} = MAX, See Note 5	−1¶			−1¶			
V_I	Input voltage range#		V_{CC} = 5 V,	V_{ID} = −1 V or 1 V,	See Note 3	15 to −15			6 to 0			V
V_{OH}	High-level output voltage		I_{OH} = −5 mA, See Note 3	V_{CC} = MIN, V_{ICR} = 0,	V_{ID} = −0.5 V, See Note 4	2.4			2.4			V
				V_{CC} = 5 V, V_{ICR} = MAX,	V_{ID} = −1 V, See Note 5	2.4			2.4			
V_{OL}	Low-level output voltage		I_{OL} = 15 mA, See Note 3	V_{CC} = MIN, V_{ICR} = 0,	V_{ID} = 0.5 V, See Note 4			0.4			0.4	V
				V_{CC} = 5 V, V_{ICR} = MAX,	V_{ID} = 1 V, See Note 5			0.4			0.4	
$I_{I(rec)}$	Receiver input current		V_{CC} = MAX, See Note 3	V_I = 0,	Other input at 0 V		−0.5	−0.9		−0.5	−1	mA
				V_I = 0.4 V,	Other input at 2.4 V		−0.4	−0.7		−0.4	−0.8	
				V_I = 2.4 V,	Other input at 0.4 V		0.1	0.3		0.1	0.4	
I_I	Input current at maximum input voltage	Strobe	V_{CC} = MIN, V_{strobe} = 4.5 V	V_{ID} = −0.5 V,	'116, SN75117			5			5	μA
		Enable	V_{CC} = MAX,	V_I = 5.5 V	SN75118, SN75119			1			1	mA

†Unless otherwise noted V_{strobe} = 2.4 V. All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.

§Differential voltages are at the B input terminal with respect to the A input terminal. Neither receiver input of the SN75117 or SN75119 should be taken negative with respect to GND.

¶The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

#Input voltage range is the voltage range that, if exceeded at either input, will cause the receiver to cease functioning properly.

NOTES: 3. Measurement of these characteristics on the SN75117 and SN75119 requires the driver to be disabled with the driver enable at 0.8 V.

4. This applies with the less positive receiver input grounded. For SN55116, V_{ID} = −1 V.

5. For '116 and SN75118, this applies with the more positive receiver input at 15 V or the more negative receiver input at −15 V. For SN75117 and SN75119, this applies with the more positive receiver input at 6 V.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

receiver section

PARAMETER			TEST CONDITIONS†			'116, SN75118			SN75117, SN75119			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
I_{IH}	High-level input current	Enable	V_{CC} = MAX,	V_I = 2.4 V	SN75118, SN75119			40			40	μA
I_{IL}	Low-level input current	Strobe	V_{CC} = MAX, V_{strobe} = 0.4 V,	V_{ID} = 0.5 V, See Note 4	'116, SN75117			−2.4			−2.4	mA
		Enable	V_{CC} = MAX,	V_I = 0.4 V	SN75118, SN75119			−1.6			−1.6	
$I_{(RC)}$	Response-time-control current (Pin 9)		V_{CC} = MAX, RC at 0 V,	V_{ID} = 0.5 V, See Note 4	T_A = 25°C	−1.2						mA
$I_{O(off)}$	Off-state open-collector output current		V_{CC} = MAX, V_O = 12 V, V_{ID} = −1 V	T_A = 25°C			1	10				μA
				T_A = MAX	SN55116			200				
					SN75__			20				
I_{OZ}	Off-state (high-impedance state) output current		V_{CC} = MAX, V_O = 0 to V_{CC}, RE at 0.4 V	T_A = 25°C	SN75118, SN75119			±10			±10	μA
				T_A = MAX	SN75118			±20				
					SN75119						±20	
R_T	Line-terminating resistance		V_{CC} = 5 V		T_A = 25°C	77		167				Ω
I_{OS}	Short-circuit output current§		V_{CC} = MAX, V_{ID} = −0.5 V,	V_O = 0, See Note 4	T_A = 25°C	−15		−80	−15		−80	mA
I_{CC}	Supply current (driver and receiver combined)		V_{CC} = MAX, See Note 4	V_{ID} = 0.5 V,	T_A = 25°C		42	60		42	60	mA

†Unless otherwise noted V_{strobe} = 2.4 V. All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.
§Not more than one output should be shorted at a time.
NOTE 4: This applies with the less positive receiver input grounded. For SN55116, V_{ID} = −1 V.

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switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

receiver section

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		R_L = 400 Ω, See Figure 16		20	75	ns
t_{PHL}	Propagation delay time, high-to-low-level output				17	75	ns
t_{PZH}	Output enable time to high level	SN75118	R_L = 480 Ω, See Figure 14		9	20	ns
t_{PZL}	Output enable time to low level	and	R_L = 250 Ω, See Figure 15		16	35	ns
t_{PHZ}	Output disable time from high level	SN75119	R_L = 480 Ω, See Figure 14		12	30	ns
t_{PLZ}	Output disable time from low level	only	R_L = 250 Ω, See Figure 15		17	35	ns

TYPICAL CHARACTERISTICS

DRIVER OUTPUT VOLTAGE
vs
DRIVER INPUT VOLTAGE

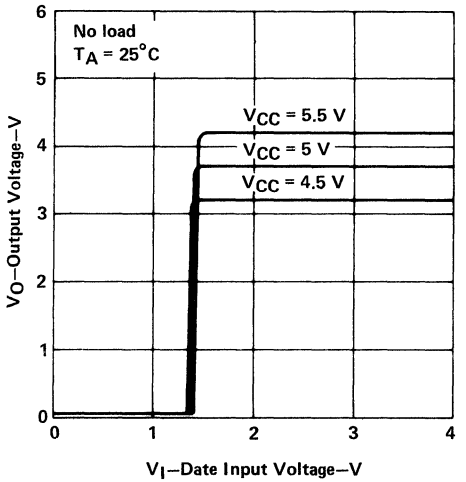


FIGURE 1

DRIVER OUTPUT VOLTAGE
vs
DRIVER INPUT VOLTAGE

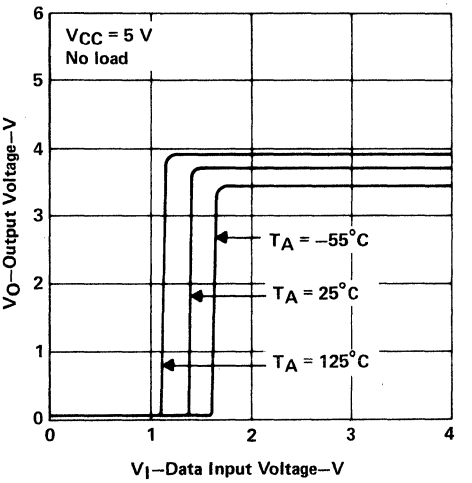


FIGURE 2

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

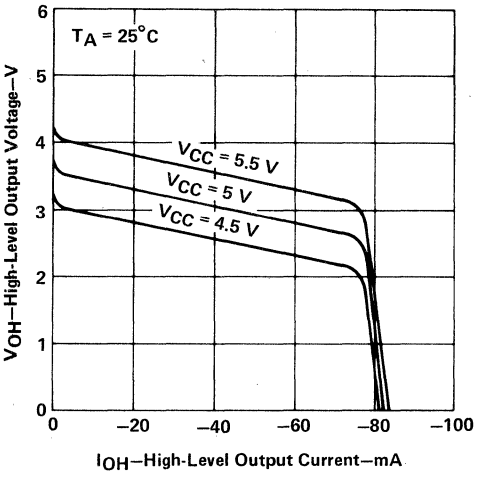


FIGURE 3

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

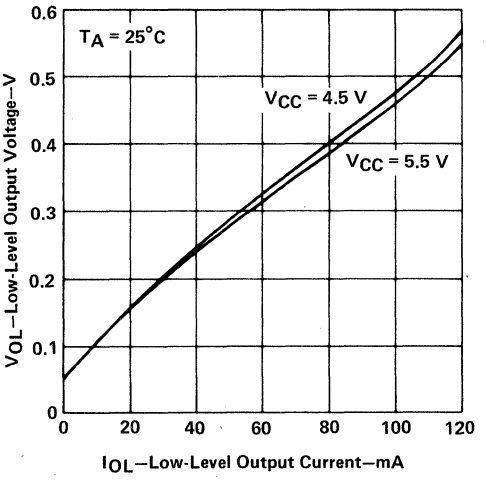


FIGURE 4

DRIVER PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE†

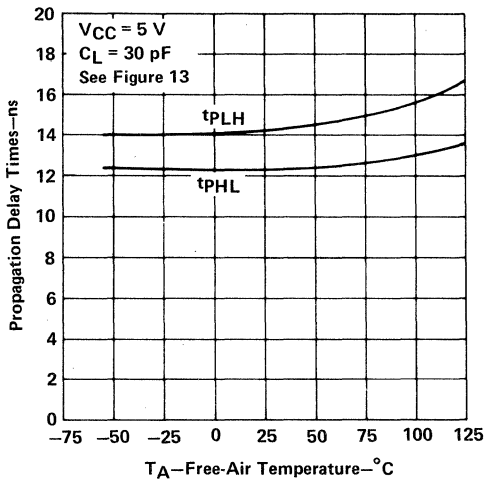


FIGURE 5

DRIVER OUTPUT ENABLE AND DISABLE TIMES
vs
FREE-AIR TEMPERATURE†

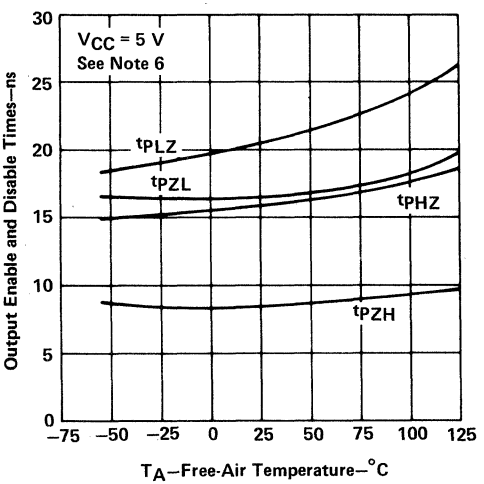


FIGURE 6

† Data for temperatures below 0°C and above 70°C are applicable to SN55116.
NOTE 6: For t_{PZH} and t_{PHZ}: R_L = 180 Ω, see Figure 14. For t_{PZL} and t_{PLZ}: R_L = 250 Ω, see Figure 15.

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

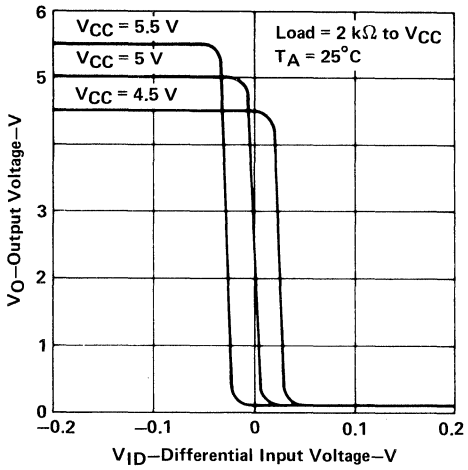


FIGURE 7

RECEIVER OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE†

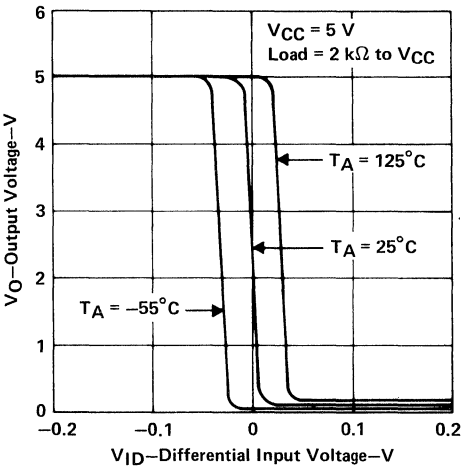


FIGURE 8

RECEIVER PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE†

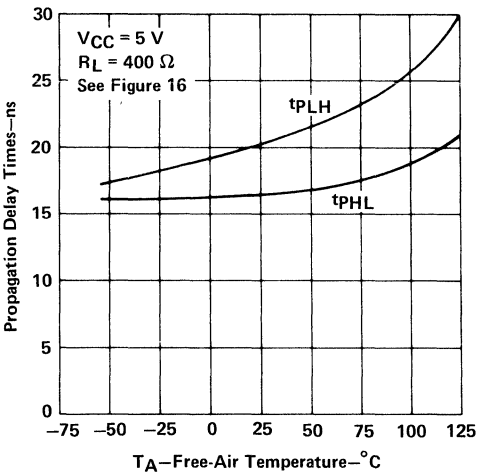


FIGURE 9

RECEIVER OUTPUT ENABLE AND DISABLE TIMES
vs
FREE-AIR TEMPERATURE†

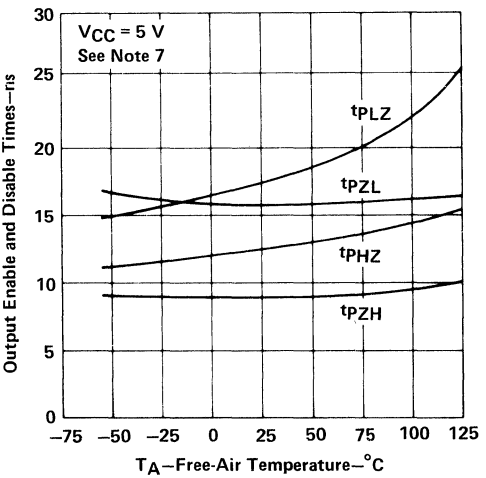


FIGURE 10

†Data for temperatures below 0°C and above 70°C are applicable to SN55116.
NOTE 7: For t_{PZH} and t_{PHZ}: R_L = 480 Ω, see Figure 14. For t_{PZL} and t_{PLZ}: R_L = 250 Ω, see Figure 15.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT (DRIVER AND RECEIVER)
vs
SUPPLY VOLTAGE

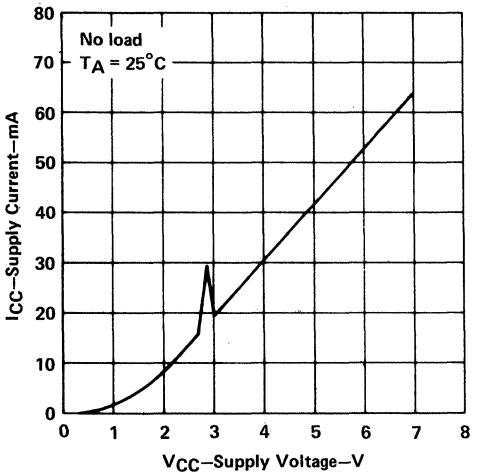


FIGURE 11

SUPPLY CURRENT (DRIVER & RECEIVER)
vs
FREE-AIR TEMPERATURE†

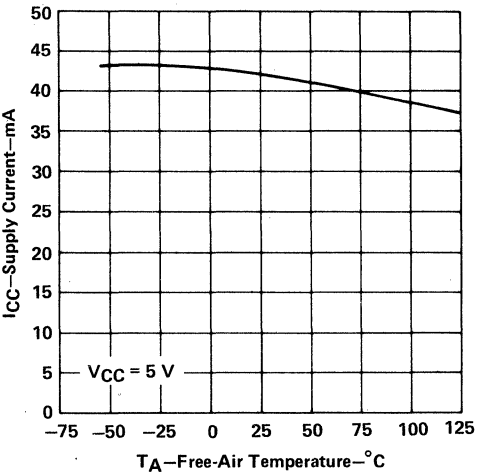


FIGURE 12

† Data for temperatures below 0°C and above 70°C are applicable to SN55116.

PARAMETER MEASUREMENT INFORMATION

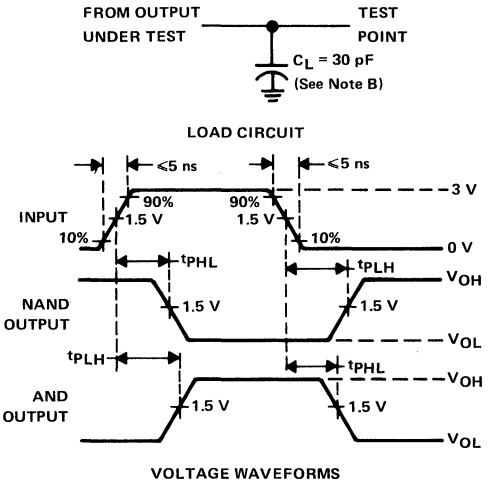


FIGURE 13. t_{PLH} and t_{PHL} (DRIVERS ONLY)

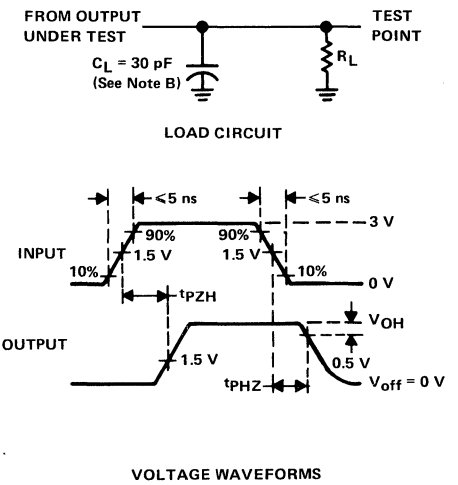


FIGURE 14. t_{PZH} and t_{PHZ}

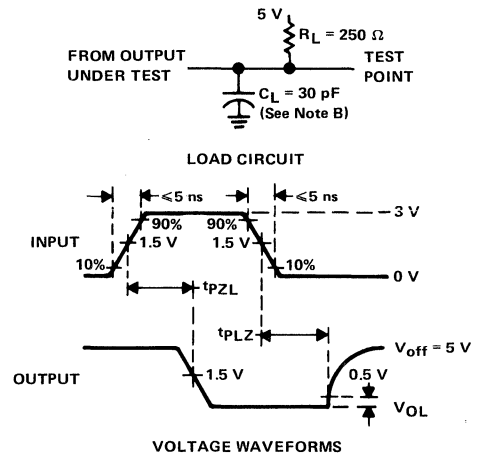


FIGURE 15. t_{PZL} and t_{PLZ}

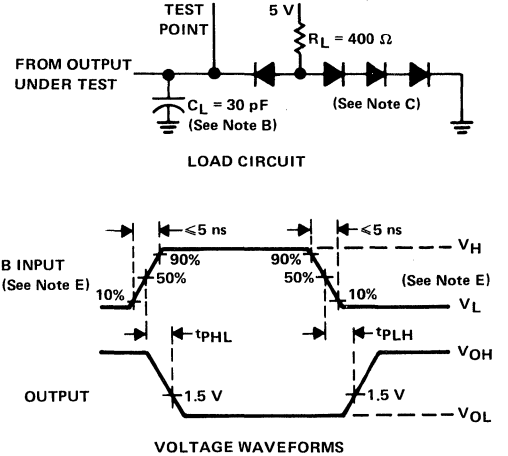


FIGURE 16. t_{PLH} and t_{PHL} (RECEIVERS ONLY)

NOTES: A. Input pulses are supplied by generators having the following characteristics Z_O = 50 Ω, PRR ≤ 500 kHz, t_W = 100 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. When testing the '116 and SN75118 receiver sections, the response-time control and the termination resistor pins are left open.
E. For '116 and SN75118, V_H = 3 V, V_L = −3 V, the A input is at 0 V.
For SN75117 and SN75119, V_H = 3 V, V_L = 0, the A input is at 1.5 V.

D1334, SEPTEMBER 1973—REVISED SEPTEMBER 1986

- **Designed for Digital Data Transmission over 50-Ω to 500-Ω Coaxial Cable, Strip Line, or Twisted Pair**
- **High-Speed**
  t_{pd} = 20 ns Max at C_L = 15 pF
- **TTL Compatible With Single 5-V Supply**
- **2.4-V Output at I_{OH} = −75 mA**
- **Uncommitted Emitter-Follower Output Structure for Party-Line Operation**
- **Short-Circuit Protection**
- **AND-OR Logic Configuration**
- **Designed for Use With Triple Line Receivers SN55122, SN75122**
- **Designed to Be Interchangeable With Signetics N8T13**

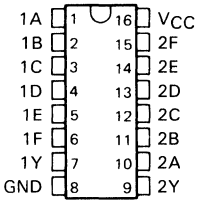
description

The SN55121 and SN75121 dual line drivers are designed for digital data transmission over lines having impedances from 50 to 500 ohms. They are also compatible with standard TTL logic and supply voltage levels.

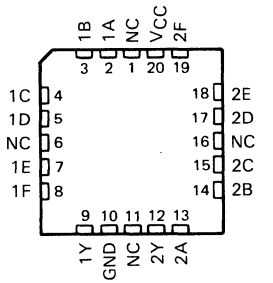
The low-impedance emitter-follower outputs of the SN55121 and SN75121 will drive terminated lines such as coaxial cable or twisted pairs. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network which turns on when the output voltage drops below approximately 1.5 V. All of the inputs are in conventional TTL configuration and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line.

The SN55121 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75121 is characterized for operation from 0°C to 70°C.

SN55121 . . . J PACKAGE
SN75121 . . . D, J, OR N PACKAGE
(TOP VIEW)



SN55121 . . . FK PACKAGE
(TOP VIEW)



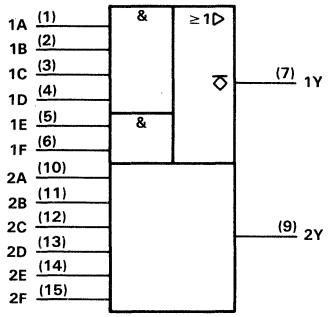
NC—No internal connection

FUNCTION TABLE

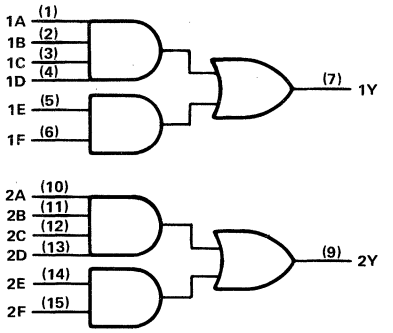
INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All other input combinations						L

H = high level
L = low level
X = irrelevant

logic symbol†

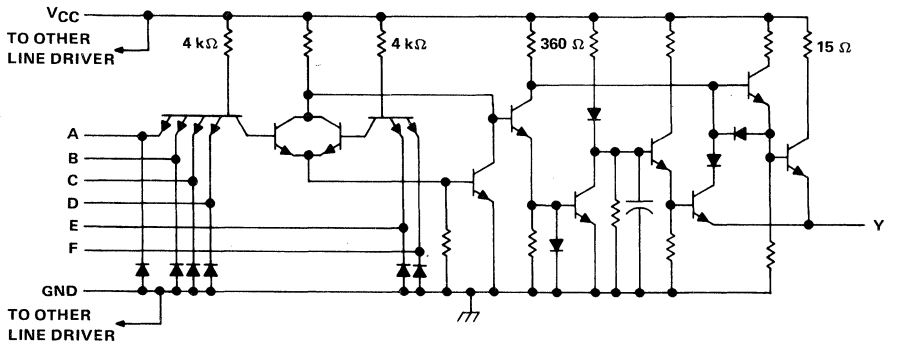


logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

schematic (each driver)



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55121	SN75121	UNIT
Supply voltage, V_{CC} (see Note 1)	6	6	V
Input voltage	6	6	V
Output voltage	6	6	V
Continuous total power dissipation (see Note 2)	See Dissipation Rating Table		
Operating free-air temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260	°C

NOTES: 1. All voltage values are with respect to both ground terminals connected together.
2. In the FK and J packages, SN55121 chips are either silver glass or alloy mounted and SN75121 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	–
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55121)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75121)	1025 mW	8.2 mW/°C	656 mW	–
N	1150 mW	9.2 mW/°C	736 mW	–

recommended operating conditions

	SN55121			SN75121			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−75			−75	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 5 V,	I_I = −12 mA			−1.5	V
$V_{(BR)I}$	Input breakdown voltage	V_{CC} = 5 V,	I_I = 10 mA		5.5		V
V_{OH}	High-level output voltage	V_{IH} = 2 V,	I_{OH} = −75 mA,	See Note 3	2.4		V
I_{OH}	High-level output current	V_{CC} = 5 V, T_A = 25°C,	V_{IH} = 4.5 V, See Note 3	V_{OH} = 2 V,	−100	−250	mA
I_{OL}	Low-level output current	V_{IL} = 0.8 V,	V_{OL} = 0.4 V,	See Note 3		−800	μA
$I_{O(off)}$	Off-state output current	V_{CC} = 3 V,	V_O = 3 V			500	μA
I_{IH}	High-level input current	V_I = 4.5 V				40	μA
I_{IL}	Low-level input current	V_I = 0.4 V			−0.1	−1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = 5 V,	T_A = 25°C			−30	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	All inputs at 2 V,	Outputs open		28	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	All inputs at 0.8 V,	Outputs open		60	mA

†Not more than one output should be shorted at a time.

NOTE 3: The output voltage and current limits are valid for any appropriate combination of high and low inputs specified by the function table for the desired output.

switching characteristics, V_{CC} = 5 V, T_A = 25C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 37 Ω, C_L = 15 pF, See Figure 1		11	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			8	20	
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 37 Ω, C_L = 1000 pF, See Figure 1		22	50	ns
t_{PHL}	Propagation delay time, high-to-low-level output			20	50	

PARAMETER MEASUREMENT INFORMATION

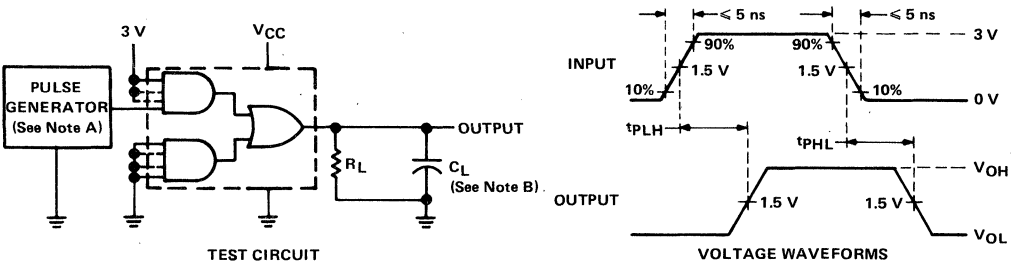


FIGURE 1. SWITCHING TIMES

NOTES: A. The pulse generators have the following characteristics: $Z_o \approx 50\ \Omega$, t_w = 200 ns, duty cycle ≤ 50%, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

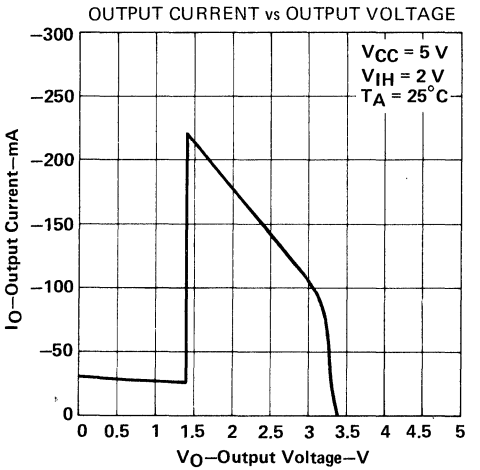


FIGURE 2

APPLICATION INFORMATION

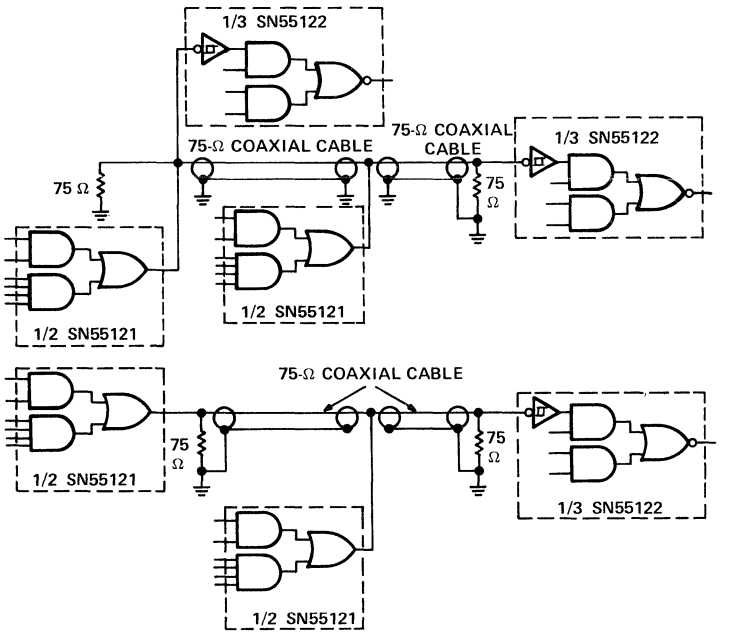
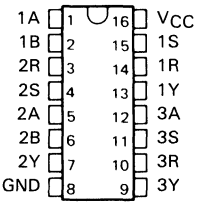


FIGURE 3. SINGLE-ENDED PARTY LINE CIRCUITS

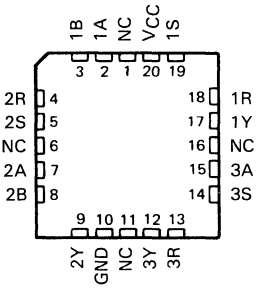
D1334, SEPTEMBER 1973—REVISED SEPTEMBER 1986

- **Designed for Digital Data Transmission Over Coaxial Cable, Strip Line, or Twisted Pair**
- **Designed for Operation With 50-Ω to 500-Ω Transmission Lines**
- **TTL Compatible**
- **Single 5-V Supply**
- **Built-In Input Threshold Hysteresis**
- **High Speed . . . Typical Propagation Delay Time = 20 ns**
- **Independent Channel Strobes**
- **Input Gating Increases Application Flexibility**
- **Fanout to 10 Series 54/74 Standard Loads**
- **Can Be Used With Dual Line-Drivers SN55121 and SN75121**
- **Interchangeable With Signetics N8T14**

SN55122 . . . J PACKAGE
SN75122 . . . D, J, OR N PACKAGE
(TOP VIEW)



SN55122 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

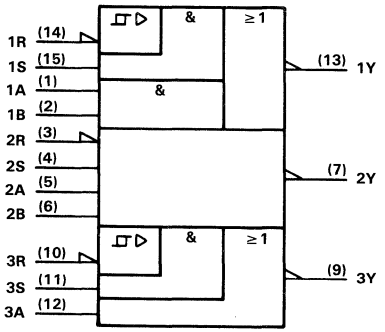
description

The SN55122 and SN75122 are triple line-receivers that are designed for digital data transmission over lines having impedances from 50 to 500 Ω. They are also compatible with standard TTL-logic and supply voltage levels.

The SN55122 and SN75122 have receiver inputs with built-in hysteresis to provide increased noise margin for single-ended systems. The high impedance of this input presents a minimum load to the driver and allows termination of the transmission line in its characteristic impedance to minimize line reflection. An open line will affect the receiver input as would a low-level voltage. The receiver can withstand a level of −0.15 V with power on or off. The other inputs are in TTL configuration. The S input must be high to enable the receiver input. Two of the line receivers have A and B inputs that, if both are high, will hold the output low. The third receiver has only an A input that, if high, will hold the output low.

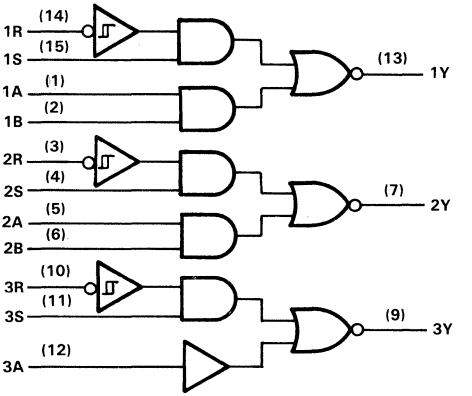
The SN55122 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75122 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram



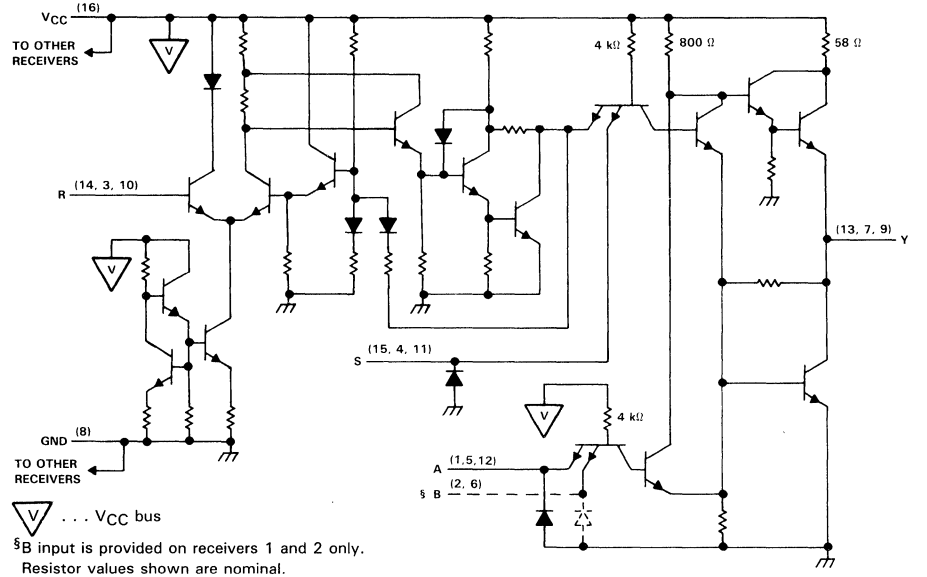
FUNCTION TABLE

INPUTS				OUTPUT
A	B‡	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

‡B input and last two lines of the function table are applicable to receivers 1 and 2 only.

H = high level
L = low level
X = irrelevant

schematic diagram (each receiver)



§B input is provided on receivers 1 and 2 only.
Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6 V
Input voltage: R input . . . . . 6 V
A, B, or S input . . . . . 5.5 V
Output voltage . . . . . 6 V
Output current . . . . . ±100 mA
Continuous total power dissipation (see Note 2) . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN55122 . . . . . −55°C to 125°C
SN75122 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. In the FK and J packages, SN55122 chips are alloy mounted and in the J package, SN75122 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55122)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75122)	1025 mW	8.2 mW/°C	656 mW	—
N	1150 mW	9.2 mW/°C	736 mW	—

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	A, B, R, or S	2			V
Low-level input voltage, V_{IL}	A, B, R, or S			0.8	V
High-level output current, I_{OH}				−500	μA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A	SN55122	−55		125	°C
	SN75122	0		70	°C

electrical characteristics over recommended operating free-air temperature, V_{CC} = 4.75 V to 5.25 V (unless otherwise noted)

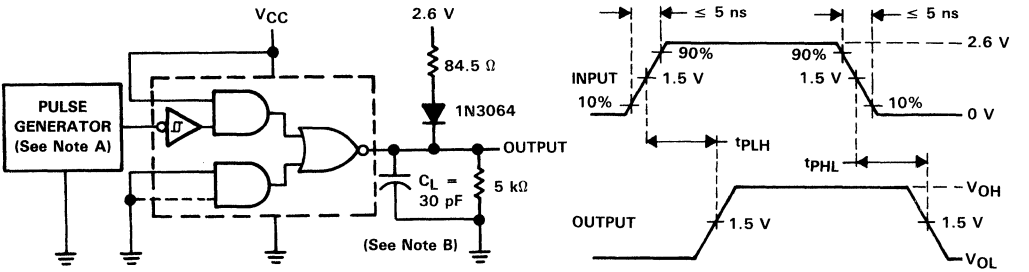
PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{hys}‡	Hysteresis	R	V_{CC} = 5 V, T_A = 25°C	0.3	0.6		V
V_{IK}	Input clamp voltage	A,B, or S	V_{CC} = 5 V, I_I = −12 mA			−1.5	V
$V_{I(BR)}$	Input breakdown voltage	A,B, or S	V_{CC} = 5 V, I_I = 10 mA	5.5			V
V_{OH}	High-level output voltage		V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −500 μA	2.6			V
			$V_{I(A)}$ = 0, $V_{I(B)}$ = 0, $V_{I(S)}$ = 2 V, $V_{I(R)}$ = 1.45 V (see Note 3), I_{OH} = −500 μA	2.6			
V_{OL}	Low-level output voltage		V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4	V
			$V_{I(A)}$ = 0, $V_{I(B)}$ = 0, $V_{I(S)}$ = 2 V, $V_{I(R)}$ = 1.45 V (see Note 4), I_{OL} = 16 mA			0.4	
I_{IH}	High-level input current	A,B, or S	V_I = 4.5 V			40	μA
		R	V_I = 3.8 V			170	
I_{IL}	Low-level input current	A,B, or S	V_I = 0.4 V, V_{IR} = 0.8 V	−0.1		−1.6	mA
I_{OS}§	Short-circuit output current		V_{CC} = 5 V, T_A = 25°C	−50		−100	mA
I_{CCH}	High-level supply current		V_{CC} = 5.25 V, All inputs at 0.8 V, Outputs open			72	mA
I_{CCL}	Low-level supply current		V_{CC} = 5.25 V, All inputs at 2 V, Outputs open (see Note 5)			100	mA

†All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
§Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
NOTES: 3. The receiver input was high immediately before being reduced to 1.45 V.
4. The receiver input was low immediately before being increased to 1.45 V.
5. For SN55122, V_{CC} = 5.5 V

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from R input	See Figure 1		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from R input	See Figure 1		20	30	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $Z_O \approx 50\ \Omega$, $t_W = 200$ ns, duty cycle = 50%, PRR = 500 kHz.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES

TYPICAL CHARACTERISTICS

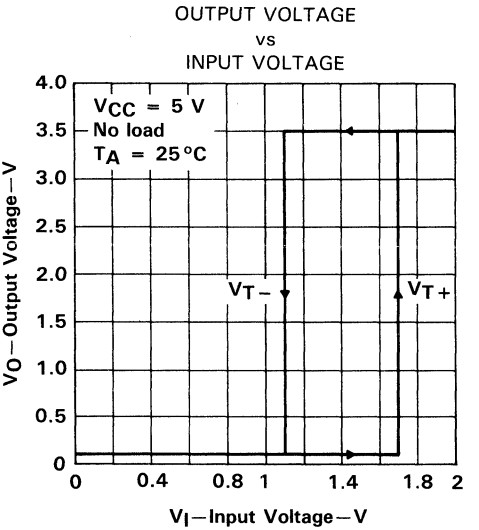


FIGURE 2

APPLICATION INFORMATION

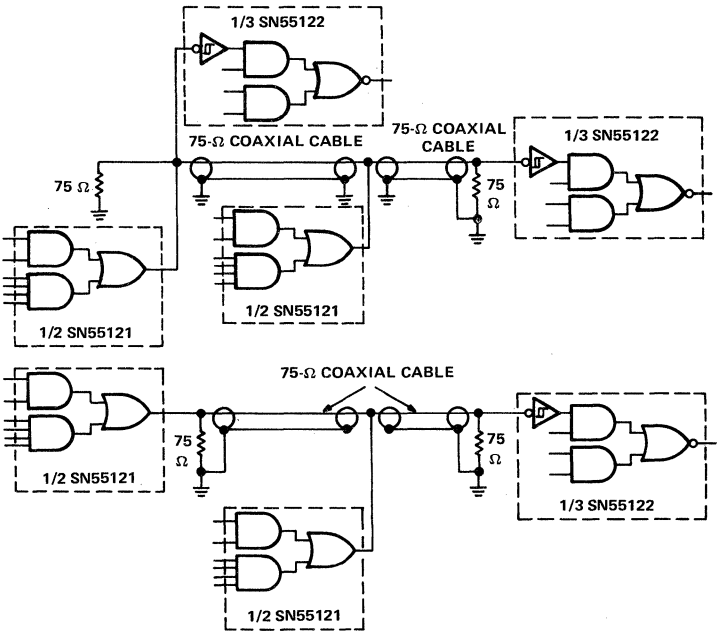
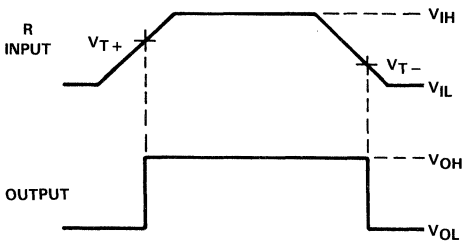


FIGURE 3. SINGLE-ENDED PARTY LINE CIRCUITS



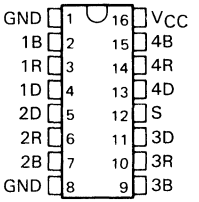
The high gain and built-in hysteresis of the SN55122 and SN75122 line receivers enable them to be used as Schmitt triggers in squaring pulses.

FIGURE 4. PULSE SQUARING

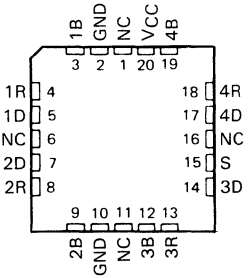
D1663, SEPTEMBER 1973—REVISED SEPTEMBER 1986

- **Single 5-V Supply**
- **High-Input-Impedance, High-Threshold Receivers**
- **Common Driver Strobe**
- **TTL-Compatible Driver and Strobe Inputs with Clamp Diodes**
- **High-Speed Operation**
- **100-mA Open-Collector Driver Outputs**
- **Four Independent Channels**
- **TTL-Compatible Receiver Output**

SN55138 . . . J PACKAGE
SN75138 . . . D, J, OR N PACKAGE
(TOP VIEW)



SN55138 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN55138 and SN75138 quad bus transceivers are designed for two-way data communication over single-ended transmission lines. Each of the four identical channels consists of a driver with TTL inputs and a receiver with a TTL output. The driver open-collector output is designed to handle loads of up to 100 mA open-collector. The receiver input is internally connected to the driver output, and has a high impedance to minimize loading of the transmission line. Because of the high driver-output current and the high receiver-input impedance, a very large number (typically hundreds) of transceivers may be connected to a single data bus.

The receiver design also features a threshold of 2.3 V (typical), providing a wider noise margin than would be possible with a receiver having the usual TTL threshold. A strobe turns off all drivers (high impedance) but does not affect receiver operation. These circuits are designed for operation from a single 5-V supply and include a provision to minimize loading of the data bus when the power-supply voltage is zero.

The SN55138 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75138 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(TRANSMITTING)

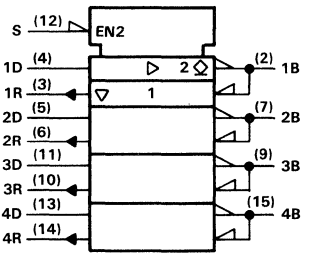
INPUTS		OUTPUTS	
S	D	B	R
L	H	L	H
L	L	H	L

FUNCTION TABLE
(RECEIVING)

INPUTS			OUTPUT
S	B	D	R
H	H	X	L
H	L	X	H

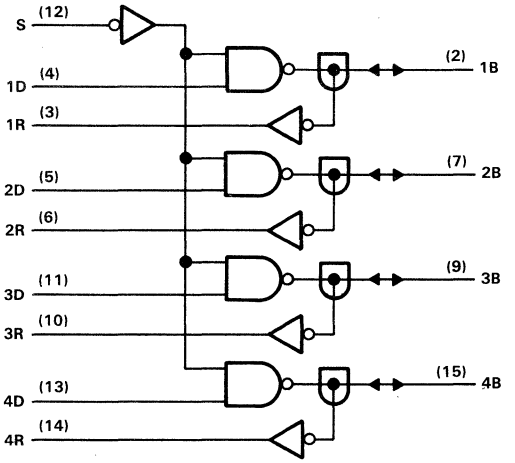
H = high level, L = low level, X = irrelevant

logic symbol†



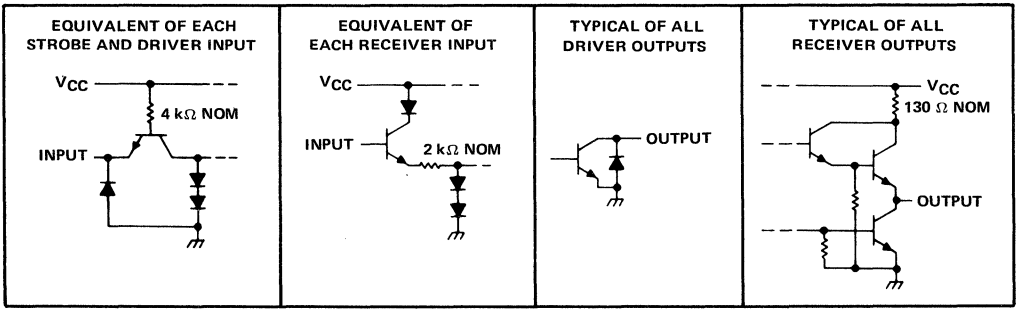
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers showns are for D, J, and N packages.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55138	SN75138	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	V
Input voltage	5.5	5.5	V
Driver off-state output voltage	7	7	V
Low-level output current into the driver output	150	150	mA
Continuous total power dissipation (see Note 2)	See Dissipation Rating Table		
Operating free-air temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260	°C
Case temperature for 60 seconds: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300	300	°C

NOTES: 1. All voltage values are with respect to both ground terminals connected together.
2. In the FK and J packages, SN55138 chips are alloy mounted and SN75138 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55138)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75138)	1025 mW	8.2 mW/°C	656 mW	—
N	1150 mW	9.2 mW/°C	736 mW	—

recommended operating conditions

		SN55138			SN75138			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	Driver or strobe	2			2			V
	Receiver	3.2			2.9			
Low-level input voltage, V_{IL}	Driver or strobe			0.8			0.8	V
	Receiver			1.5			1.8	
High-level output current, I_{OH}	Receiver output			−400			−400	μA
Low-level output current, I_{OL}	Driver output			100			100	mA
	Receiver output			16			16	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN55138			SN75138			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	Driver or strobe	V_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	Receiver	V_{CC} = MIN, $V_{IL(R)}$ = V_{IL} max,	$V_{IH(S)}$ = 2 V, I_{OH} = −400 μA	2.4	3.5		2.4	3.5		V
V_{OL}	Low-level output voltage	Driver	V_{CC} MIN, $V_{IL(S)}$ = 0.8 V,	$V_{IH(D)}$ = 2 V, I_{OL} = 100 mA			0.45			0.45	V
		Receiver	V_{CC} = MIN, $V_{IH(S)}$ = 2 V,	$V_{IH(R)}$ = V_{IH} min, I_{OL} = 16 mA			0.4			0.4	
I_I	Input current at maximum input voltage	Driver or strobe	V_{CC} = MAX,	V_I = V_{CC}			1			1	mA
I_{IH}	High-level input current	Driver or strobe	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
		Receiver	V_{CC} = 5 V, $V_{I(S)}$ = 2 V	$V_{I(R)}$ = 4.5 V,		25	300		25	300	
I_{IL}	Low-level input current	Driver or strobe	V_{CC} = MAX,	V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
		Receiver	V_{CC} = MAX, $V_{I(S)}$ = 2 V	$V_{I(R)}$ = 0.45 V,			−50			−50	μA
	Input current with power off	Receiver	V_{CC} = 0,	V_I = 4.5 V		1.1	1.5		1.1	1.5	mA
I_{OS}	Short-circuit output current§	Receiver	V_{CC} = MAX		−20		−55	−18		−55	mA
I_{CC}	Supply current	All driver outputs low	V_{CC} = MAX, $V_{I(S)}$ = 0.8 V	$V_{I(D)}$ = 2 V,		50	65		50	65	mA
		All driver outputs high	V_{CC} = MAX, $V_{I(S)}$ = 2 V, Receiver outputs open	$V_{I(R)}$ = 3.5 V,		42	55		42	55	

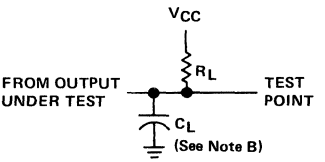
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. Parenthetical letters D, R, and S used with V_I refer to the driver input, receiver input, and strobe input, respectively.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Driver	Driver	C_L = 50 pF, R_L = 50 Ω, See Figure 1		15	24	ns
t_{PHL}					14	24	
t_{PLH}	Strobe	Driver			18	28	ns
t_{PHL}					22	32	
t_{PLH}	Receiver	Receiver	C_L = 15 pF, R_L = 400 Ω, See Figure 2		7	15	ns
t_{PHL}					8	15	

†t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output.

PARAMETER MEASUREMENT INFORMATION



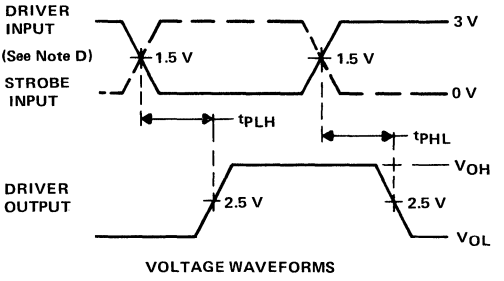
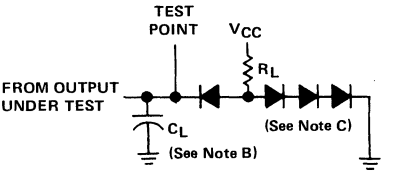


FIGURE 1. PROPAGATION DELAY TIMES FROM DATA AND STROBE INPUTS



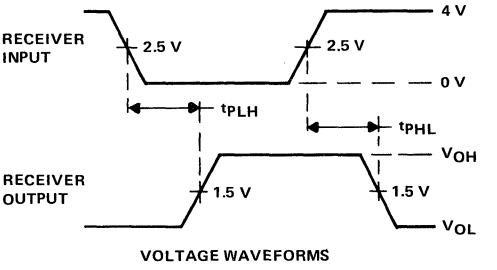


FIGURE 2. PROPAGATION DELAY TIMES FROM RECEIVER INPUT

NOTES: A. Input pulses are supplied by generators having the following characteristics: t_w = 100 ns, PRR ≤ 1 MHz, t_r ≤10 ns, t_f ≤10 ns, $Z_o \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or 1N3064.
D. When testing driver input (solid line) strobe must be low; when testing strobe input (dashed line) driver input must be high.

TYPICAL CHARACTERISTICS†

DRIVER TRANSFER CHARACTERISTICS

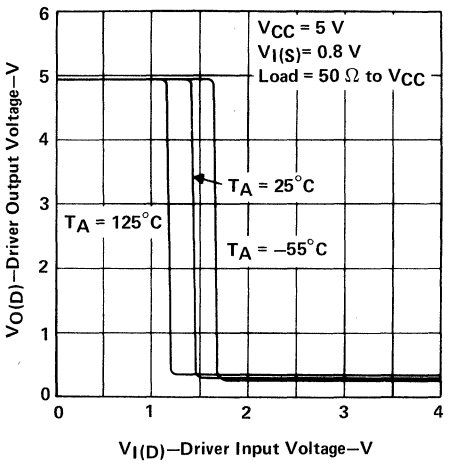


FIGURE 3

DRIVER TRANSFER CHARACTERISTICS

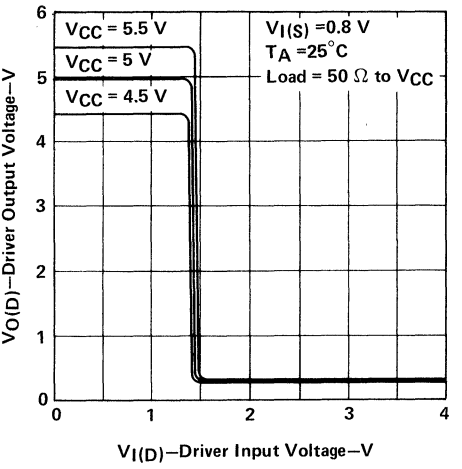


FIGURE 4

STROBE-TO-DRIVER OUTPUT
TRANSFER CHARACTERISTICS

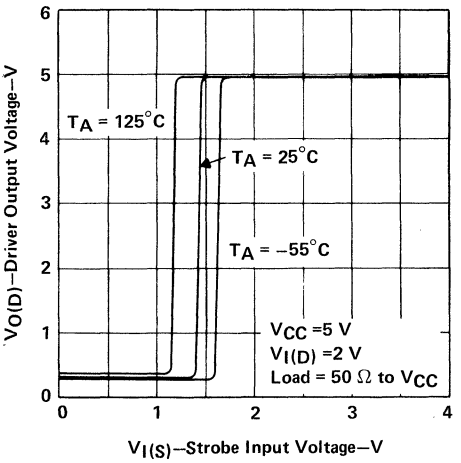


FIGURE 5

STROBE-TO-DRIVER OUTPUT
TRANSFER CHARACTERISTICS

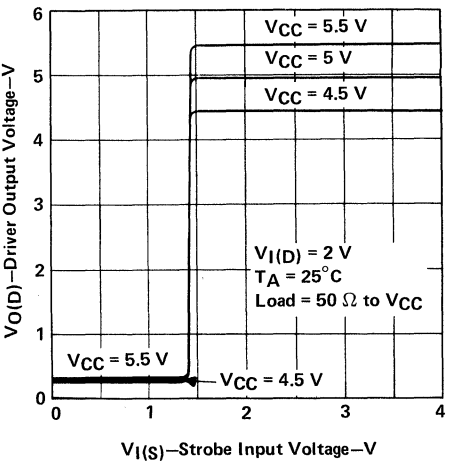


FIGURE 6

†Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS†

RECEIVER TRANSFER CHARACTERISTICS

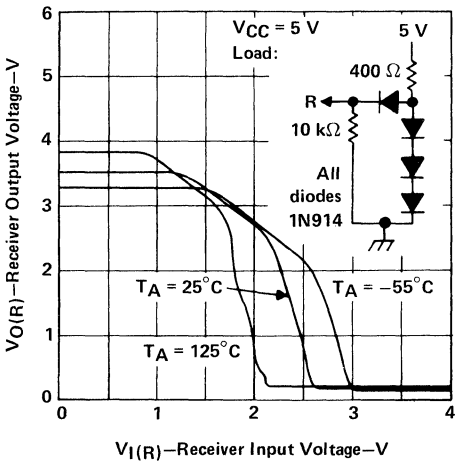


FIGURE 7

RECEIVER TRANSFER CHARACTERISTICS

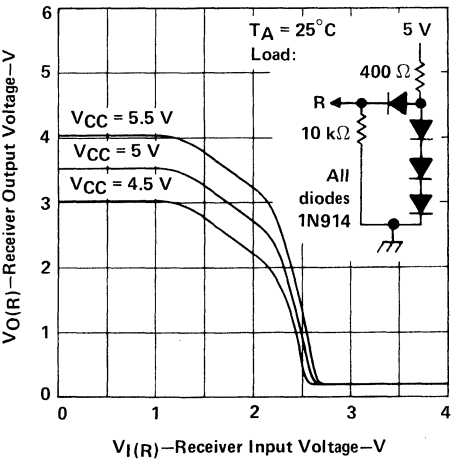


FIGURE 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT (RECEIVER)

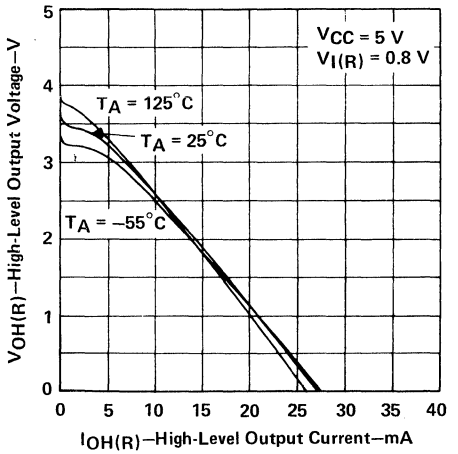


FIGURE 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT (RECEIVER)

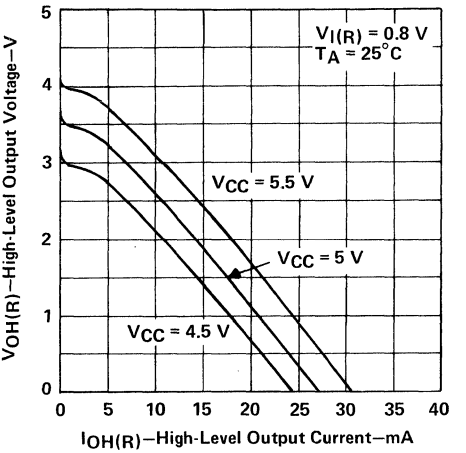


FIGURE 10

†Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT (RECEIVER)

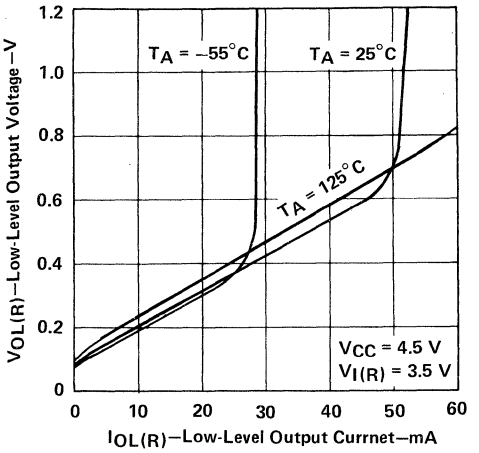


FIGURE 11

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT (DRIVER OUTPUT)

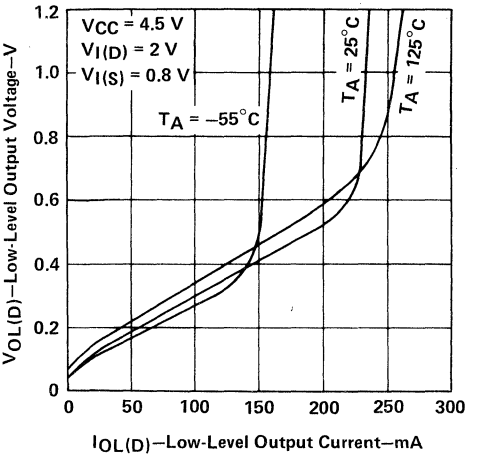


FIGURE 12

RECEIVER INPUT CURRENT
vs
RECEIVER INPUT VOLTAGE

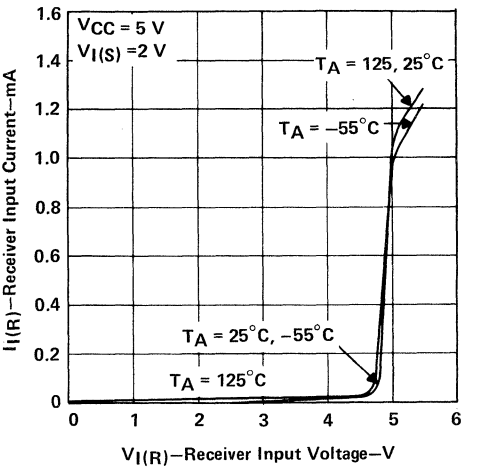


FIGURE 13

RECEIVER INPUT CURRENT
vs
RECEIVER INPUT VOLTAGE

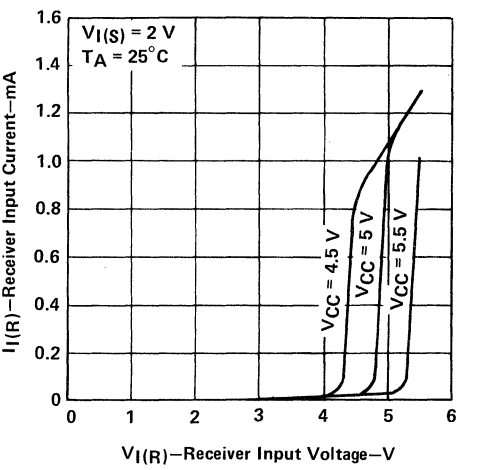


FIGURE 14

†Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE
(ALL DRIVER OUTPUTS LOW)

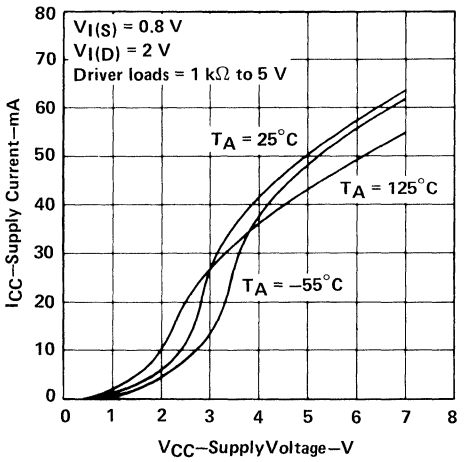


FIGURE 15

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

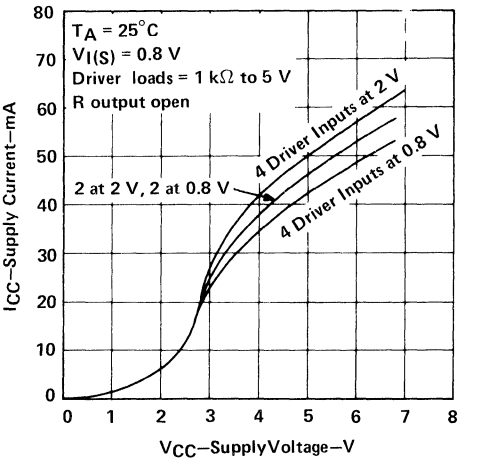


FIGURE 16

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

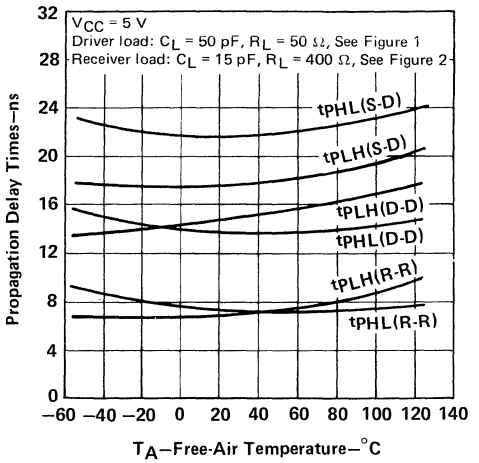


FIGURE 17

PROPAGATION DELAY TIMES
vs
SUPPLY VOLTAGE

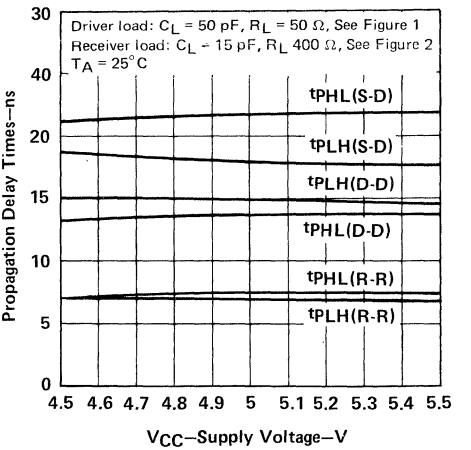


FIGURE 18

†Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS

DRIVER PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE

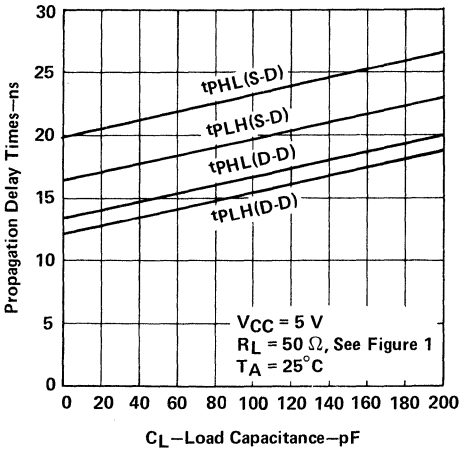


FIGURE 19

RECEIVER PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE

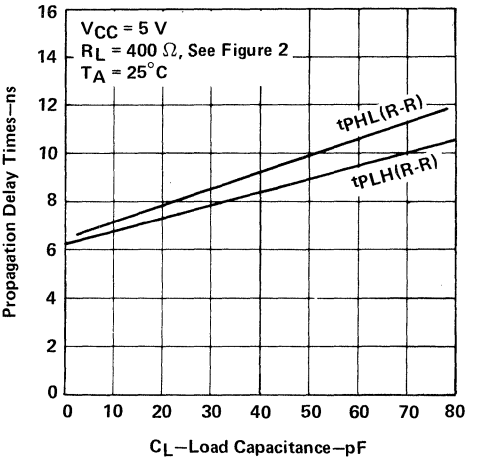
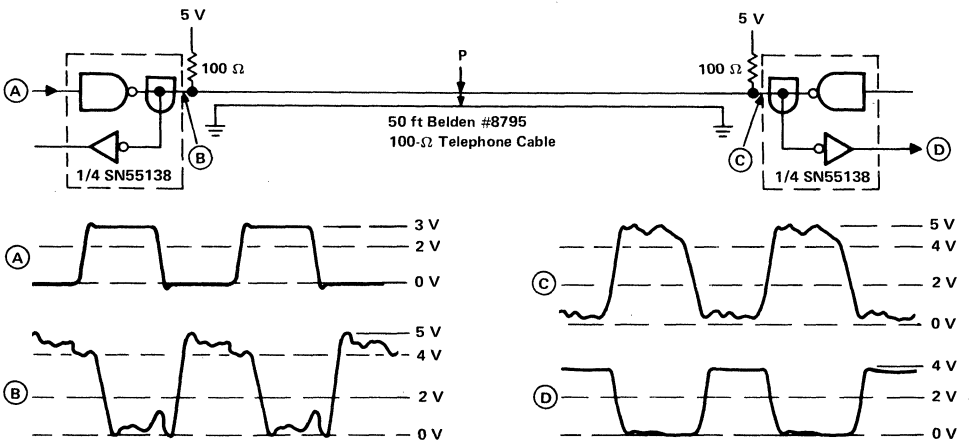


FIGURE 20

APPLICATION INFORMATION

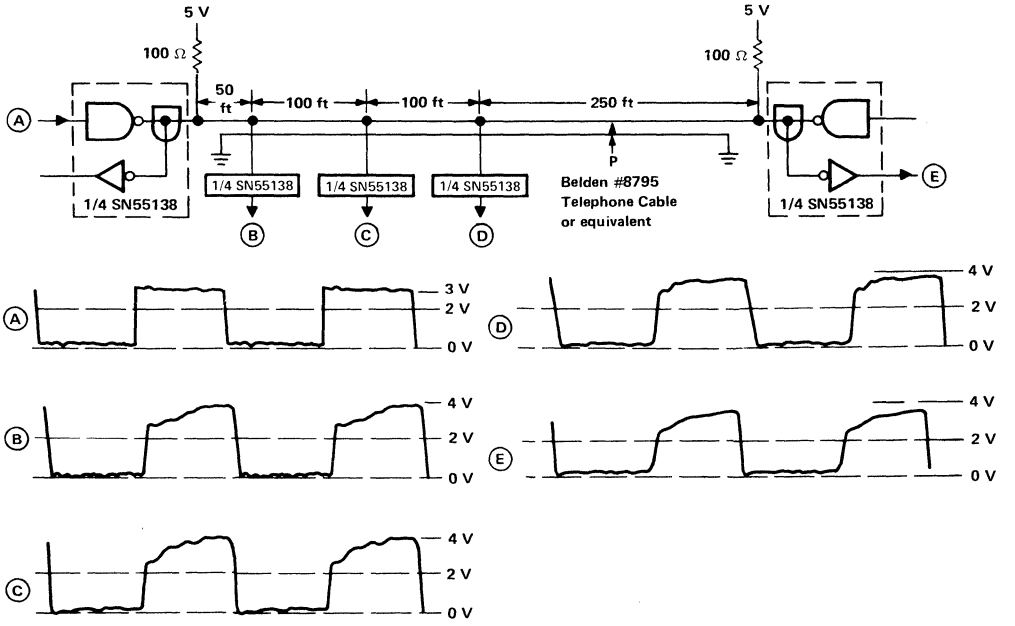


TYPICAL VOLTAGE WAVEFORMS

FIGURE 21. POINT-TO-POINT COMMUNICATION OVER 50 FEET OF TWISTED PAIR AT 5 MHz

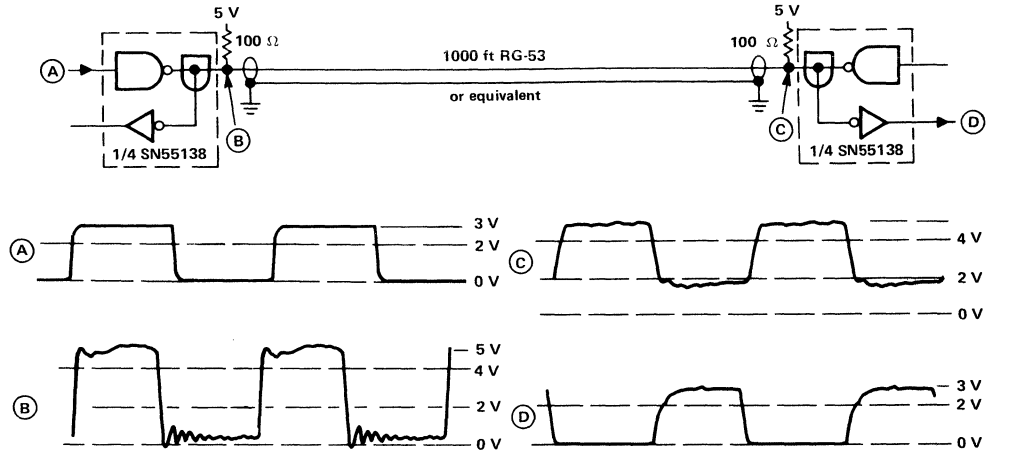
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

APPLICATION INFORMATION



TYPICAL VOLTAGE WAVEFORMS

FIGURE 22. PARTY-LINE COMMUNICATION ON 500 FEET OF TWISTED PAIR AT 1 MHz



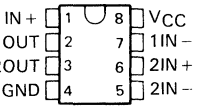
TYPICAL VOLTAGE WAVEFORMS

FIGURE 23. POINT-TO-POINT COMMUNICATION OVER 1000 FEET OF COAX AT 1 MHz

D2300, SEPTEMBER 1980—REVISED SEPTEMBER 1986

- Meets EIA Standards RS-422-A and RS-423-A
- Meets Federal Standards 1020 and 1030
- Operates from Single 5-V Power Supply
- Wide Common-Mode Voltage Range
- High Input Impedance
- TTL-Compatible Outputs
- High-Speed Schottky Circuitry
- 8-Pin Dual-In-Line Package
- Similar to uA9637AC except for Corner V_{CC} and Ground Pin Positions

SN55157 . . . JG PACKAGE
SN75157 . . . D, JG, OR P PACKAGE
(TOP VIEW)

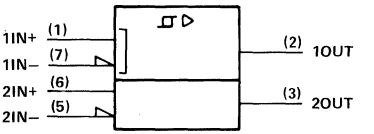


description

The SN75157 is a dual differential line receiver designed to meet EIA standards RS-422-A and RS-423-A and Federal Standards 1020 and 1030. It utilizes Schottky circuitry and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. The device operates from a single 5-volt power supply and is supplied in an 8-pin dual-in-line package and small outline package.

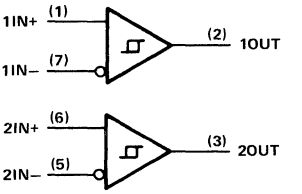
The SN55157 is characterized over the full military temperature range of −55°C to 125°C. The SN75157 is characterized for operation from 0°C to 70°C.

logic symbol†

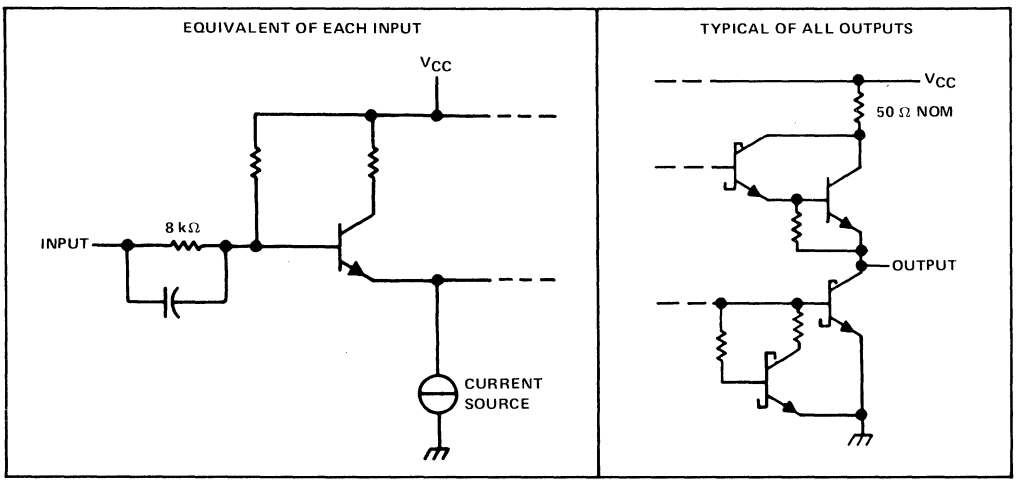


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage . . . . . ±15 V
Differential input voltage (see Note 2) . . . . . ±15 V
Output voltage (see Note 1) . . . . . −0.5 V to 5.5 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
SN55157 JG package . . . . . 1050 mW
SN75157 D package . . . . . 725 mW
JG package . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature range: SN55157 . . . . . −55°C to 125°C
SN75157 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds D or P package . . . . . 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the SN55157 JG package to 672 mW at 70°C at the rate of 8.4 mW/°C, the SN75157 JG package to 528 mW at 70°C at the rate of 6.6 mW/°C, the D package to 464 mW at 70°C at the rate of 5.8 mW/°C, and the P package to 640 mW at 70°C at the rate of 8.0 mW/°C. In the JG package, SN55157 chips are alloy mounted and SN75157 chips are glass mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}				±7	V
Operating free-air temperature, T_A	SN55157	−55	25	125	°C
	SN75157	0	25	70	

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

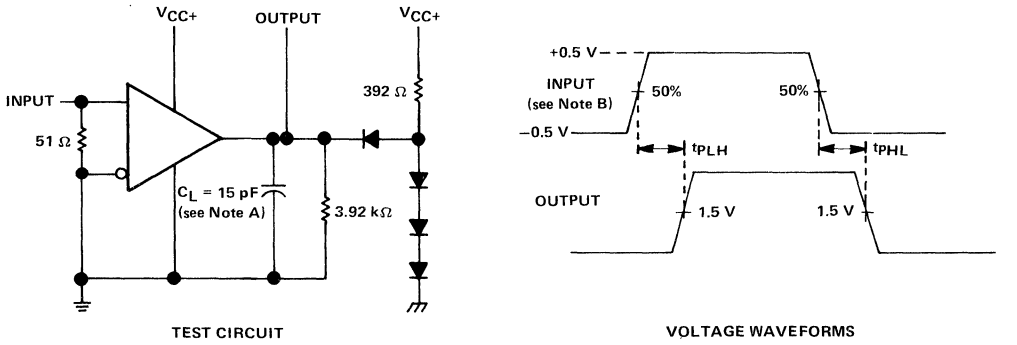
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
					See Note 4		
V_T	Threshold voltage (V_{T+} and V_{T-})			−0.2		0.2	V
		See Note 5		−0.4		0.4	
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				70		mV
V_{OH}	High-level output voltage	V_{ID} = 0.2 V,	I_O = −1 mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2 V,	I_O = 20 mA		0.35	0.5	V
I_I	Input current	V_{CC} = 0 to 5.5 V, See Note 6	V_I = 10 V		1.1	3.25	mA
			V_I = −10 V		−1.6	−3.25	
I_{OS}	Short-circuit output current‡	V_O = 0,	V_{ID} = 0.2 V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5 V,	No load		35	50	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTES: 4. The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
5. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
6. The input not under test is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 1		15	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			13	25	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 5 MHz, duty cycle = 50%.

FIGURE 1. TRANSITION TIMES

TYPICAL CHARACTERISTICS

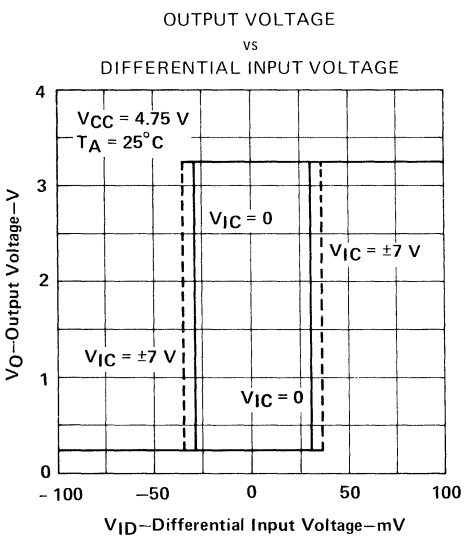


FIGURE 2

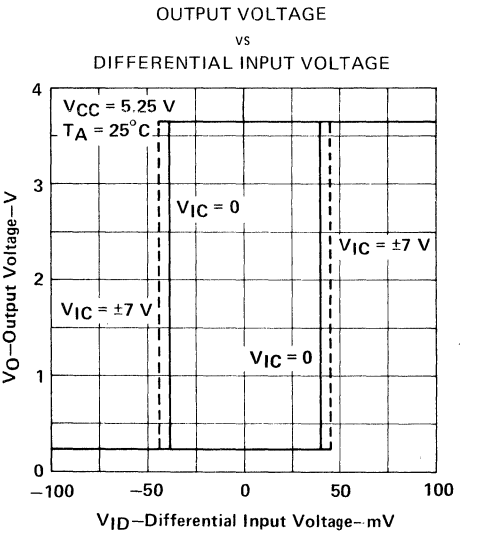


FIGURE 3

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

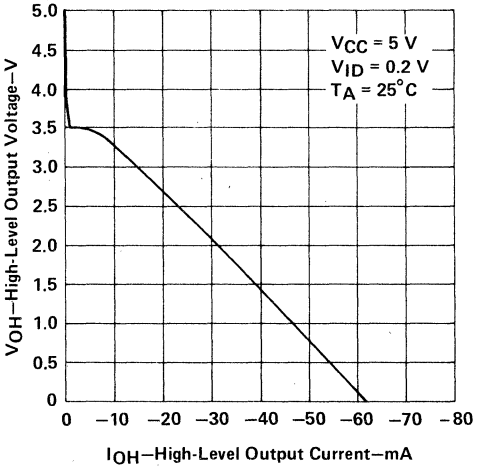


FIGURE 4

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

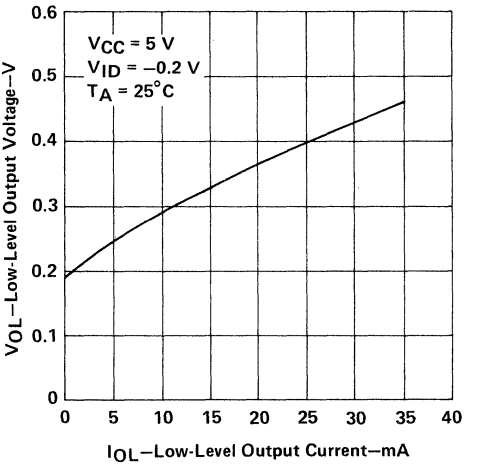


FIGURE 5

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

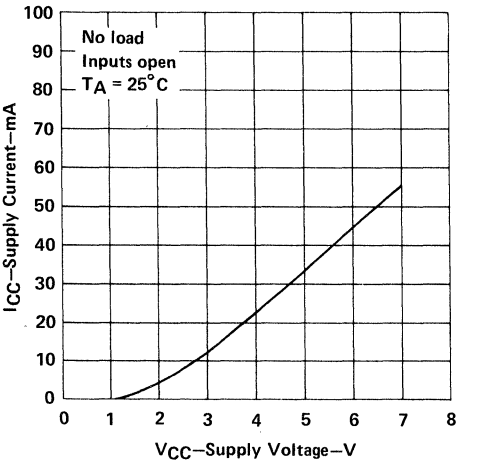


FIGURE 6

TYPICAL APPLICATION DATA

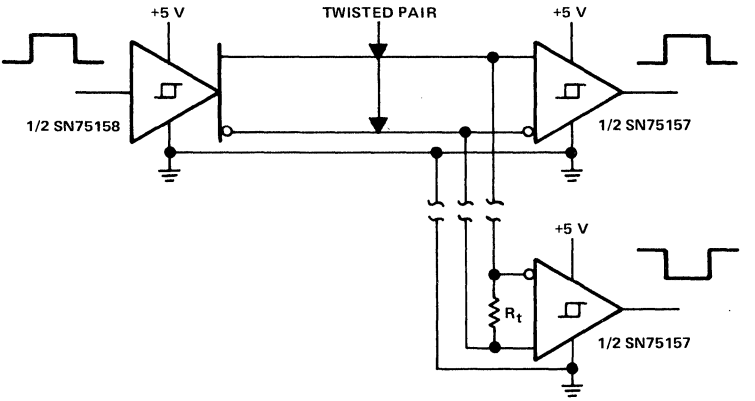
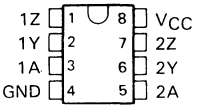


FIGURE 7. RS-422-A SYSTEM APPLICATIONS

D2292, JANUARY 1977—REVISED SEPTEMBER 1986

- Meets EIA Standard RS-422-A
- Single 5-V Supply
- Balanced-Line Operation
- TTL-Compatible
- High Output Impedance in Power-Off Condition
- High-Current Active-Pullup Outputs
- Short-Circuit Protection
- Dual Channels
- Input Clamp Diodes

SN55158 . . . JG PACKAGE
SN75158 . . . D, JG, OR P PACKAGE
(TOP VIEW)

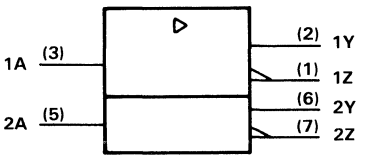


description

The SN55158 and SN75158 are dual complementary-output line drivers designed to satisfy the requirements set by the EIA Standard RS-422-A interface specifications. The outputs provide complementary signals with high-current capability for driving balanced lines, such as twisted pair, at normal line impedance without high power dissipation. The output stages are TTL totem-pole outputs providing a high-impedance state in the power-off condition.

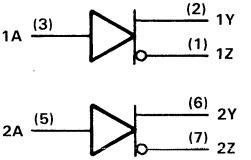
The SN55158 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75158 is characterized for operation from 0°C to 70°C.

logic symbol†

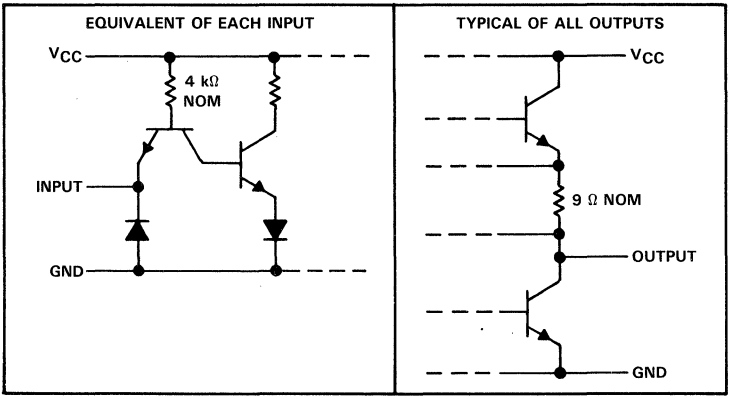


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous total power dissipation (see Note 2) . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN55158 . . . . . −55°C to 125°C
SN75158 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values except differential output voltage V_{OD} are with respect to network ground terminal. V_{OD} is at the Y output with respect to the Z output.
2. In the JG package, SN55158 chips are alloy mounted and SN75158 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	N/A
JG (SN55158)	1050 mW	8.4 mW/°C	672 mW	210 mW
JG (SN75158)	825 mW	6.6 mW/°C	528 mW	N/A
P	1000 mW	8.0 mW/°C	640 mW	N/A

recommended operating conditions

	SN55158			SN75158			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN55158			SN75158			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V, I_{OH} = −40 mA		2	3.0		2.4	3.0		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V, I_{OL} = 40 mA			0.2	0.4		0.2	0.4	V
$\lvert V_{OD1}\rvert$	Differential output voltage	V_{CC} = MAX, I_O = 0			3.5	$2V_{OD2}$		3.5	$2V_{OD2}$	V
$\lvert V_{OD2}\rvert$	Differential output voltage	V_{CC} = MIN	R_L = 100 Ω, See Figure 1	2	3.0		2	3.0		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage§	V_{CC} = MIN			±0.02	±0.4		±0.02	±0.4	V
V_{OC}	Common-mode output voltage¶	V_{CC} = MAX			1.9	3		1.8	3	V
		V_{CC} = MIN			1.4	3		1.5	3	
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage§	V_{CC} = MIN or MAX			±0.01	±0.4		±0.01	±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V		0.1	100		0.1	100	μA
			V_O = −0.25 V		−0.1	−100		−0.1	−100	
			V_O = −0.25 to 6 V			±100			±100	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1	−1.6		−1	−1.6	mA
I_{OS}	Short-circuit output current#	V_{CC} = MAX		−40	−90	−150	−40	−90	−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = MAX, No load,	Inputs grounded, T_A = 25°C		37	50		37	50	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C except for V_{OC}, for which V_{CC} is as stated under test conditions.
§ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitudes of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
# Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55158			SN75158			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 2, Termination A		16	25		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	20		10	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 2, Termination B		13	20		13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	15		9	15	ns
t_{TLH}	Transition time, low-to-high-level output	See Figure 2, Termination A		4	20		4	20	ns
t_{THL}	Transition time, high-to-low-level output			4	20		4	20	ns
	Overshoot factor	See Figure 2, Termination C			10			10	%

PARAMETER MEASUREMENT INFORMATION

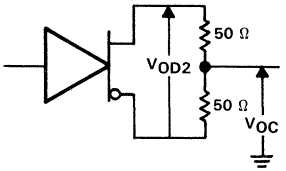
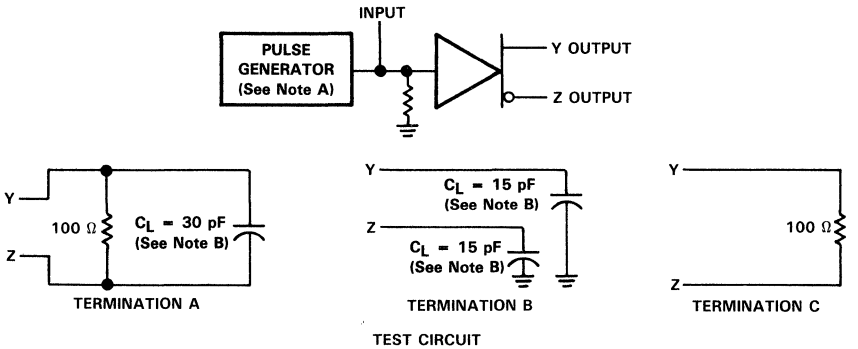


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, t_W = 25 ns, PRR ≤ 10 MHz.
B. C_L includes probe and jig capacitance.

FIGURE 2. SWITCHING TIMES

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

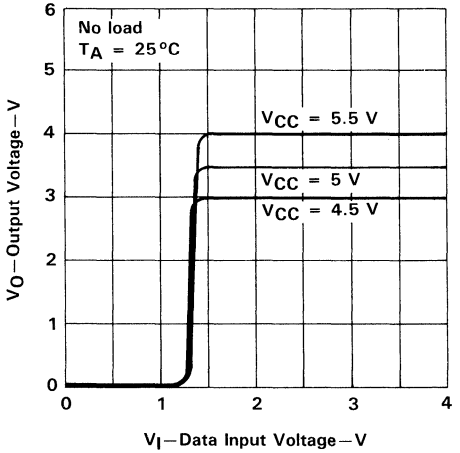


FIGURE 3

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

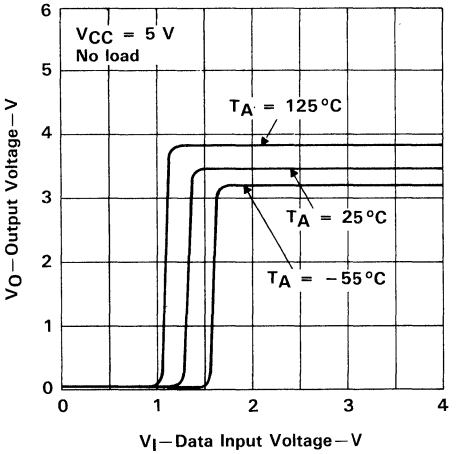


FIGURE 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

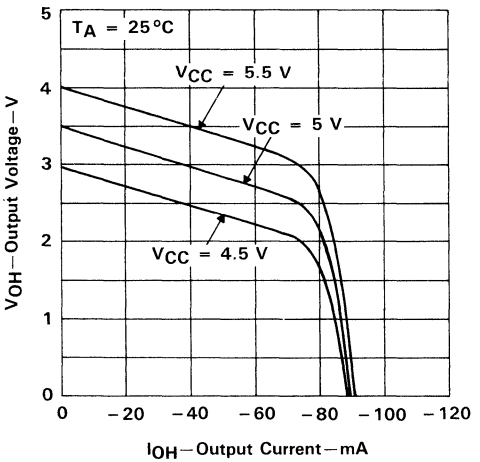


FIGURE 5

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

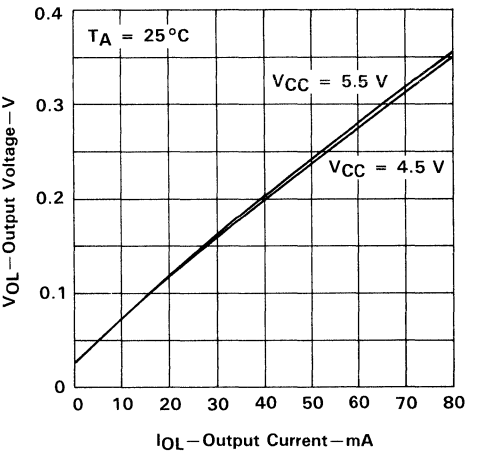


FIGURE 6

†Data for temperatures below 0°C and above 70°C are applicable to SN55158 circuits only.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

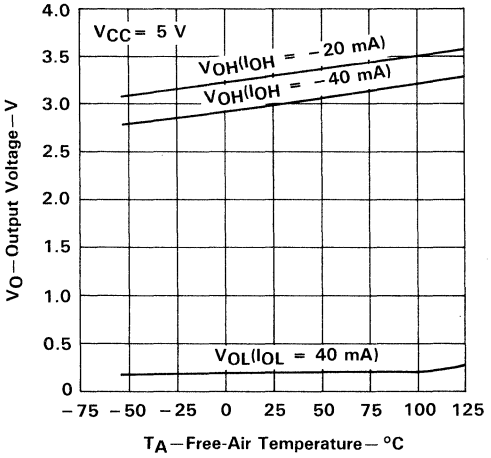


FIGURE 7

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

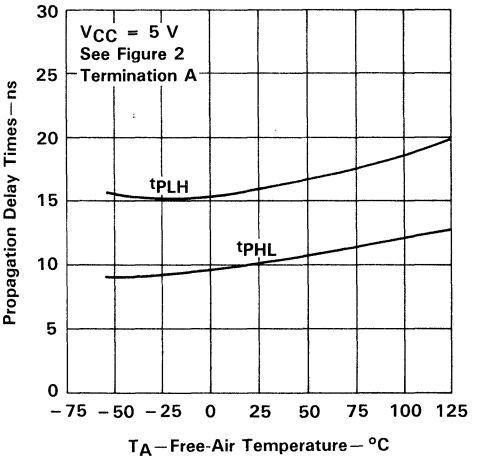


FIGURE 8

SUPPLY CURRENT
(BOTH DRIVERS)
vs
SUPPLY VOLTAGE

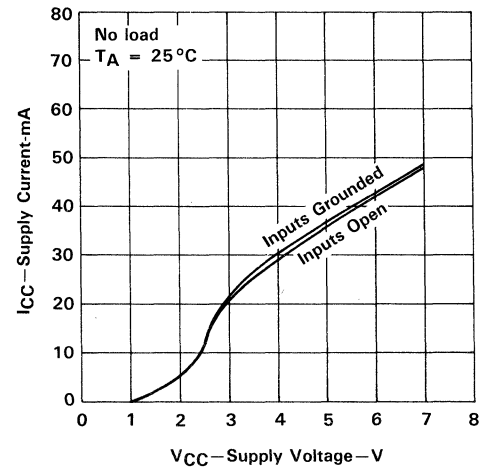


FIGURE 9

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREE-AIR TEMPERATURE

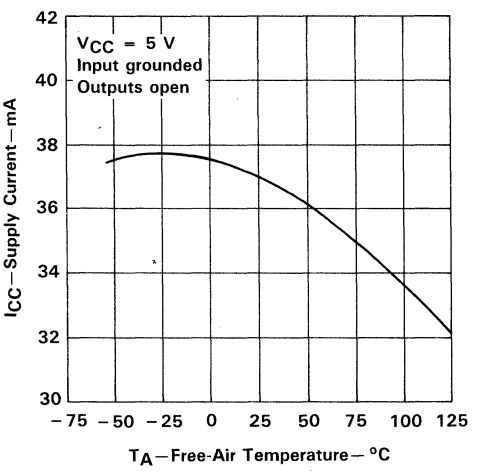


FIGURE 10

†Data for temperatures below 0°C and above 70°C are applicable to SN55158 circuits only.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREQUENCY

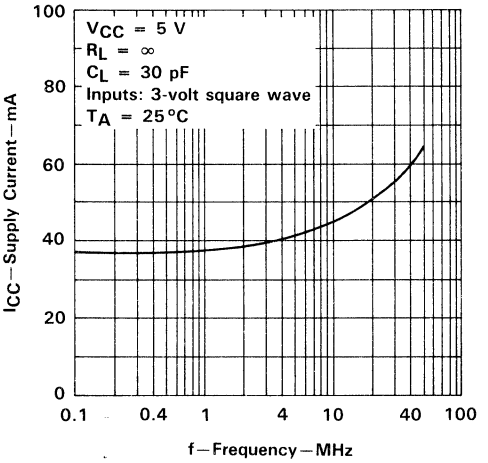
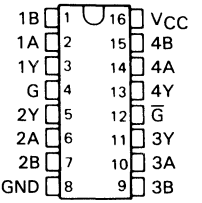


FIGURE 11

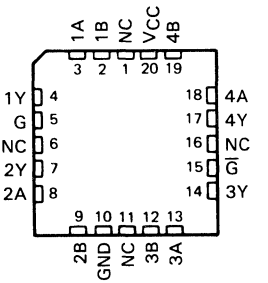
D3167, DECEMBER 1988

- Meets EIA Standards RS-422-A, RS-423-A, and RS-485
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range . . . −12 to 12 V
- Input Sensitivity . . . ±200 mV
- Input Hysteresis . . . 50 mV Typ
- High Input Impedance . . . 12 kΩ Min
- Operates from Single 5-Volt Supply
- Low Power Requirements
- Plug-In Replacement for AM26LS32

J PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



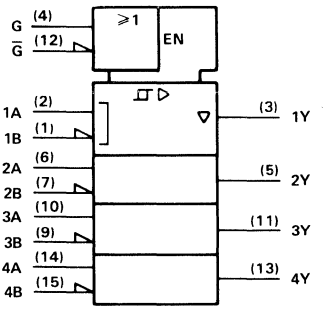
NC—No internal connection

description

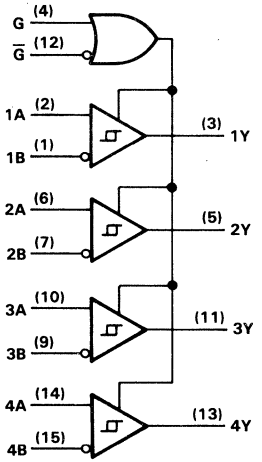
The SN55173 is a monolithic quadruple differential line receiver with three-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A, RS-423-A, and RS-485 and several CCITT recommendations. The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. The four receivers have an ORed pair of enables in common. Either G being high or $\overline{G}$ being low enables all of the receivers. The device features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of −12 to 12 V. The SN55173 is designed for optimum performance when used with the SN55172 or SN55174 quadruple differential line drivers.

The SN55173 is characterized for operation from −55°C to 125°C.

logic symbol



logic diagram (positive logic)

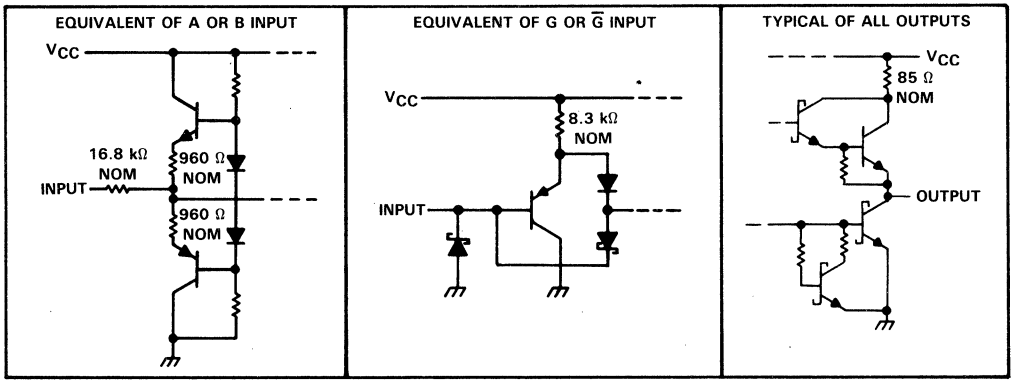


FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL A–B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V $< V_{ID} <$ 0.2 V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z

H = high level
L = low level
X = irrelevant
? = indeterminate
Z = high-impedance (off)

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, A or B inputs . . . . . ±25 V
Differential input voltage (see Note 2) . . . . . ±25 V
Enable input voltage . . . . . 7 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 1375 mW
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . 65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds . . . . . 300°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate to 275 mW at 125°C at the rate of 11.0 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Common-mode input voltage, V_{IC}			±12	V
Differential input voltage, V_{ID}			±12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	−55		125	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

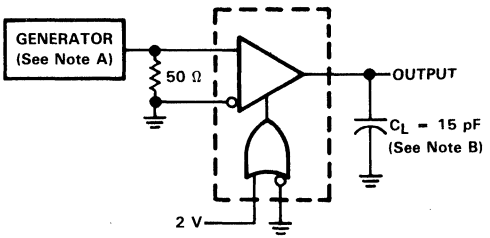
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 16 mA	−0.2‡			V
V_{hys}	Hysteresis§				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −400 μA	2.5			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input at 0 V,	V_I = 12 V			1	mA
		See Note 4	V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
I_{OS}	Short-circuit output current¶			−15		−85	mA
I_{CC}	Supply current	Outputs disabled				70	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for threshold voltage levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
¶Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
NOTE 4: Refer to EIA Standard RS-422-A and RS-423-A for exact conditions.

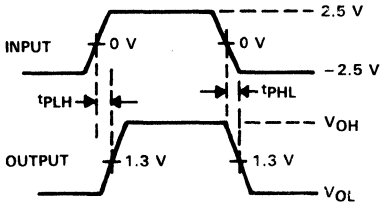
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF,			20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	See Figure 1			22	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 2		17	22	ns
t_{PZL}	Output enable time to low level	C_L = 15 pF,	See Figure 3		20	25	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF,	See Figure 2		21	30	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF,	See Figure 3		30	40	ns

PARAMETER MEASUREMENT INFORMATION

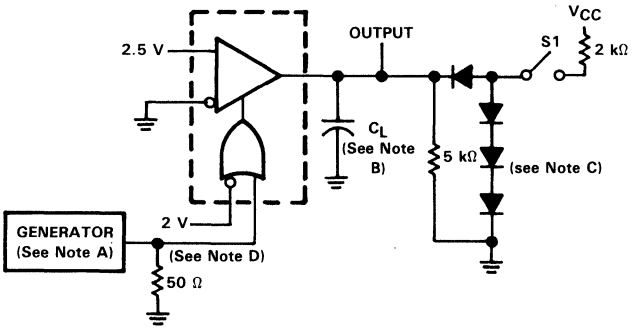


TEST CIRCUIT

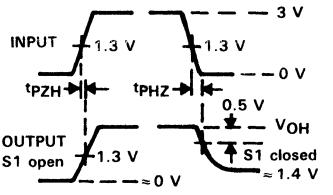


VOLTAGE WAVEFORMS

FIGURE 1. t_{PLH}, t_{PHL}



TEST CIRCUIT

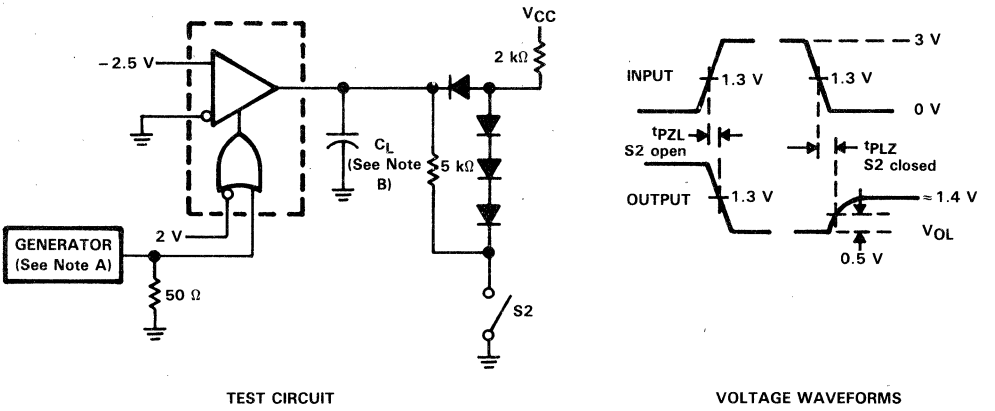


VOLTAGE WAVEFORMS

FIGURE 2. t_{PHZ}, t_{PZH}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 3. t_{PZL}, t_{PLZ}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

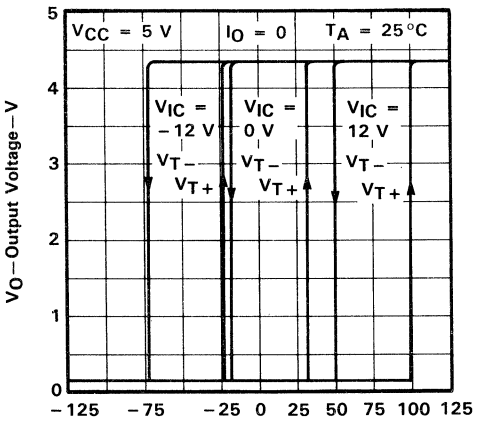


FIGURE 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

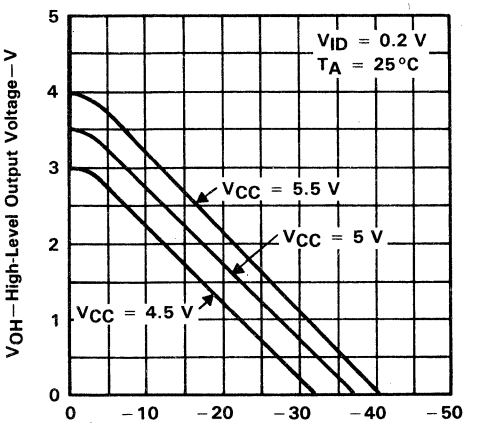


FIGURE 5

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

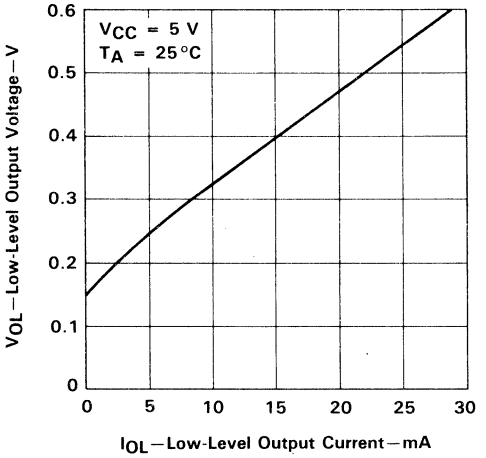


FIGURE 6

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

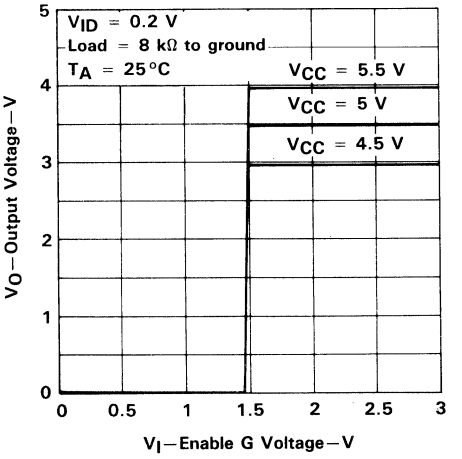


FIGURE 7

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

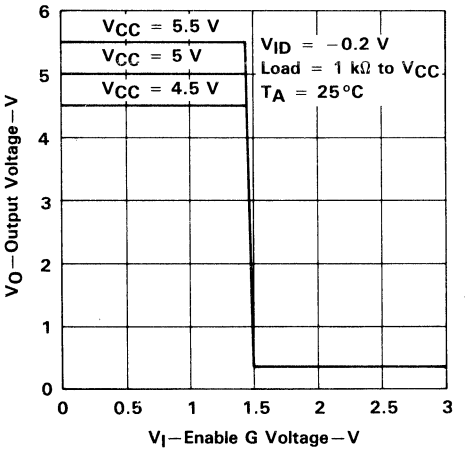


FIGURE 8

INPUT CURRENT
vs
INPUT VOLTAGE

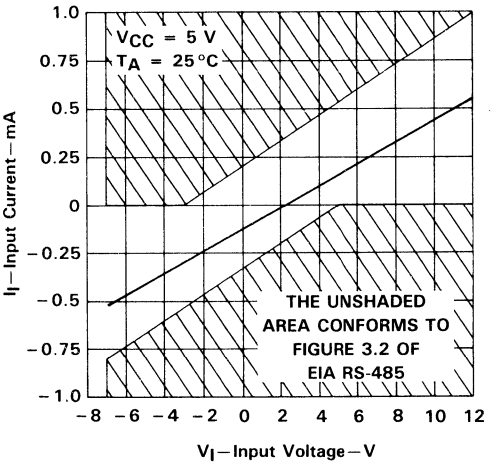
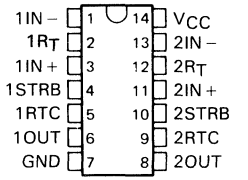


FIGURE 9

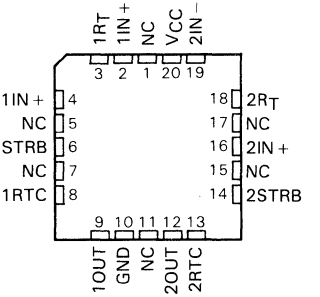
D1292, OCTOBER 1972—REVISED SEPTEMBER 1986

- **Single 5-V Supply**
- **Differential Line Operation**
- **Dual Channels**
- **TTL Compatibility**
- **±15 V Common-Mode Input Voltage Range**
- **±15 V Differential Input Voltage Range**
- **Individual Channel Strobes**
- **Built-In Optional Line-Termination Resistor**
- **Individual Frequency Response Controls**
- **Designed for Use With Dual Differential Drivers SN55183 and SN75183**
- **Designed to Be Interchangeable With National Semiconductor DS7820A and DS8820A**

SN55182 . . . J PACKAGE
SN75182 . . . D, J, OR N PACKAGE
(TOP VIEW)



SN55182 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

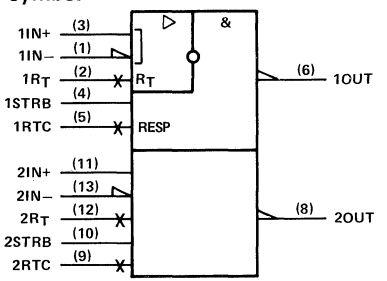
description

The SN55182 and SN75182 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL-compatible output signals as a function of the polarity of the differential input voltage. The frequency response of each channel may be easily controlled by a single external capacitor to provide immunity to differential noise spikes. The output goes to a high level when the inputs are open-circuited. A strobe input is provided which, when in the low level, disables the receiver and forces the output to a high level.

The receiver is of monolithic single-chip construction, and both halves of the dual circuits use common power supply and ground terminals.

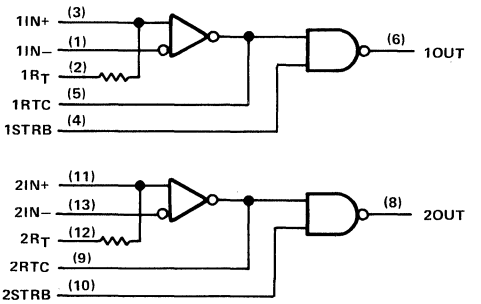
The SN55182 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75182 is characterized for operation from 0°C to 70°C.

logic symbol†

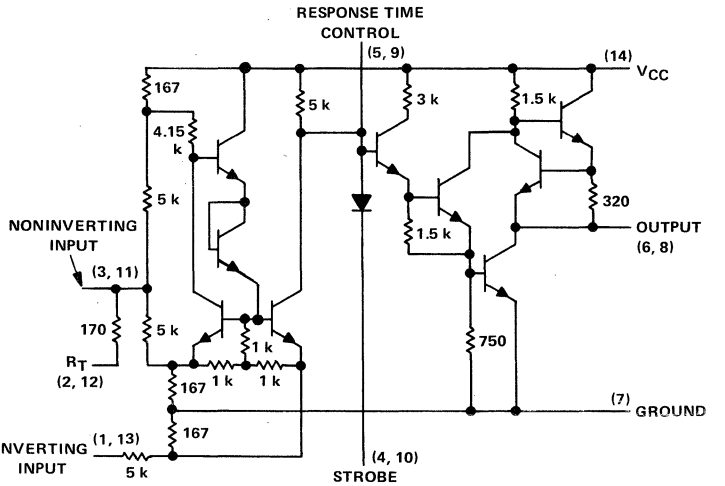


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J and N packages.

logic diagram (positive logic)



schematic (each receiver)



Resistor values shown are nominal and in ohms.

FUNCTION TABLE

STROBE	DIFF INPUT	OUTPUT
L	X	H
H	H	H
H	L	L

H = $V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max
L = $V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max
X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55182	SN75182	UNIT
Supply voltage, V_{CC1} (see Note 1)	8	8	V
Common-mode input voltage	±20	±20	V
Differential input voltage (see Note 2)	±20	±20	V
Strobe input voltage	8	8	V
Output sink current	50	50	mA
Continuous total power dissipation (see Note 3)	See Dissipation Rating Table		
Operating free-air temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260	°C
Case temperature for 60 seconds: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300	300	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.
3. In the FK and J packages, SN55182 chips are alloy mounted and SN75182 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55182)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75182)	1025 mW	8.2 mW/°C	656 mW	—
N	1150 mW	9.2 mW/°C	736 mW	—

recommended operating conditions

	SN55182			SN75182			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Common-mode input voltage, V_{IC}			±15			±15	V
High-level strobe input voltage, $V_{IH(strobe)}$	2.1		5.5	2.1		5.5	V
Low-level strobe input voltage, $V_{IL(strobe)}$	0		0.9	0		0.9	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

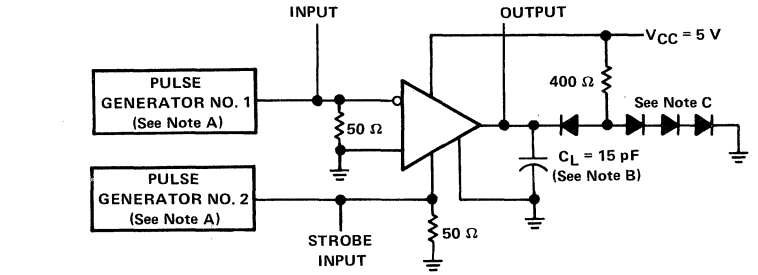
PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{TH}	Differential input high-threshold voltage		V_O = 2.5 V, I_{OH} = −400 μA	V_{IC} = −3 V to 3 V			0.5	V
				V_{IC} = −15 V to 15 V			1	
V_{TL}	Differential input low-threshold voltage		V_O = 0.4 V, I_{OL} = 16 mA	V_{IC} = −3 V to 3 V			−0.5	V
				V_{IC} = −15 V to 15 V			−1	
V_{OH}	High-level output voltage		V_{ID} = 1 V, I_{OH} = −400 μA	V_{strobe} = 2.1 V,	2.5	4.2	5.5	V
			V_{ID} = −1 V, I_{OH} = −400 μA	V_{strobe} = 0.4 V,	2.5	4.2	5.5	
V_{OL}	Low-level output voltage		V_{ID} = −1 V, I_{OL} = 16 mA	V_{strobe} = 2.1 V,		0.25	0.4	V
I_I	Input current	Inverting input	V_{IC} = 15 V			3	4.2	mA
			V_{IC} = 0			0	−0.5	
			V_{IC} = −15 V			−3	−4.2	
		Noninverting input	V_{IC} = 15 V			5	7	mA
			V_{IC} = 0			−1	−1.4	
			V_{IC} = −15 V			−7	−9.8	
I_{SH}	High-level strobe current		V_{strobe} = 5.5 V				5	μA
I_{SL}	Low-level strobe current		V_{strobe} = 0			−1	−1.4	mA
r_i	Input resistance	Inverting input			3.6	5		kΩ
		Noninverting input			1.8	2.5		kΩ
R_T	Line terminating resistance		T_A = 25°C		120	170	250	Ω
I_{OS}	Short-circuit output current		V_{CC} = 5.5 V,	V_O = 0	−2.8	−4.5	−6.7	mA
I_{CC}	Supply current (average per receiver)		V_{IC} = 15 V,	V_{ID} = −1 V		4.2	6	mA
			V_{IC} = 0,	V_{ID} = −0.5 V		6.8	10.2	
			V_{IC} = −15 V,	V_{ID} = −1 V		9.4	14	

†Unless otherwise noted, $V_{strobe} \geq 2.1$ V or open.
‡All typical values are at V_{CC} = 5 V, V_{IC} = 0, and T_A = 25°C.

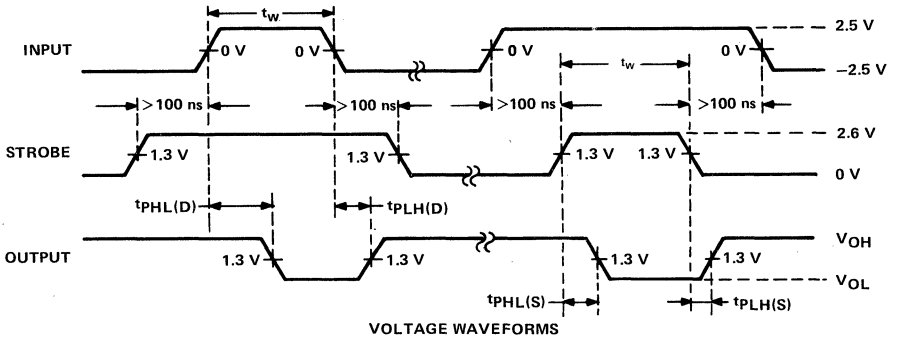
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low-to-high-level output from differential input	R_L = 400 Ω, C_L = 15 pF, See Figure 1		18	40	ns
$t_{PHL(D)}$	Propagation delay time, high-to-low-level output from differential input			31	45	ns
$t_{PLH(S)}$	Propagation delay time, low-to-high-level output from strobe input			9	30	ns
$t_{PHL(S)}$	Propagation delay time, high-to-low-level output from strobe input			15	25	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns, t_W = 0.5 ±0.1 μs, PRR ≤ 1 MHz.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

FIGURE 1. PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS†

DIFFERENTIAL INPUT THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

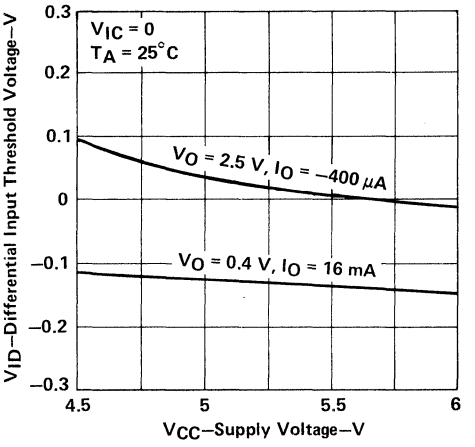


FIGURE 2

DIFFERENTIAL INPUT THRESHOLD VOLTAGE
vs
COMMON-MODE VOLTAGE

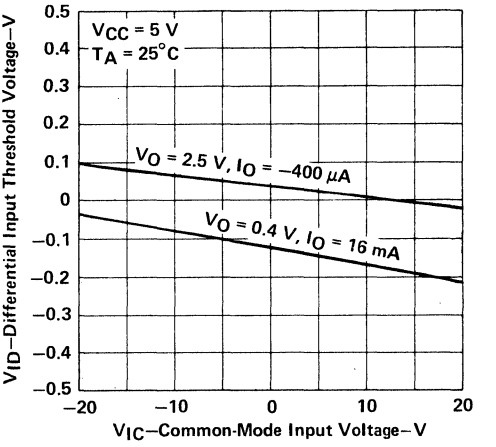


FIGURE 3

DIFFERENTIAL INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

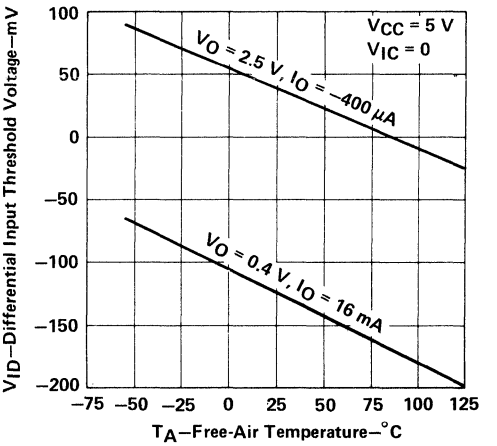


FIGURE 4

†Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

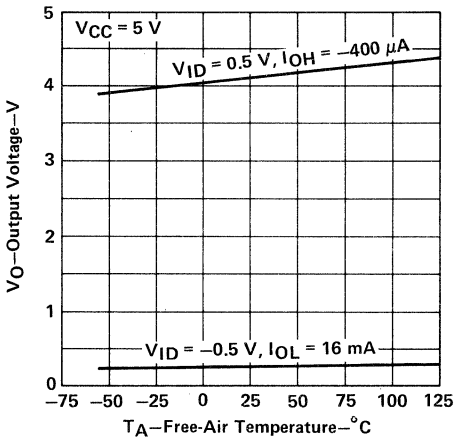


FIGURE 5

VOLTAGE TRANSFER CHARACTERISTICS

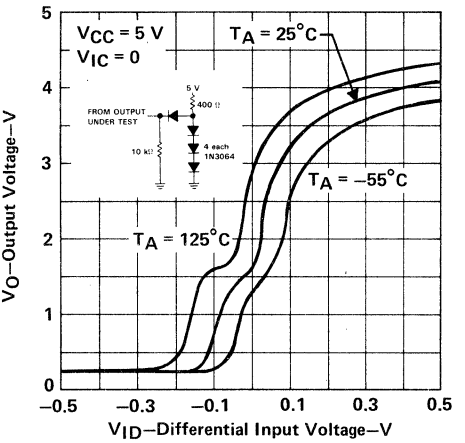


FIGURE 6

INPUT CURRENT
vs
INPUT VOLTAGE

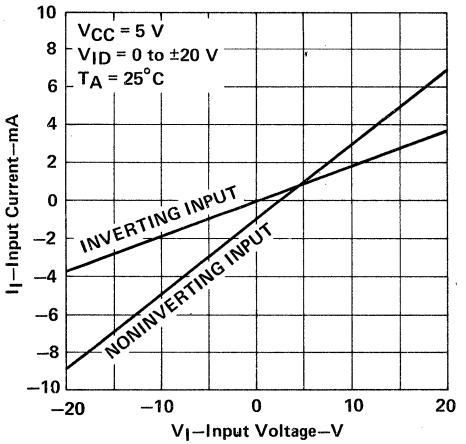


FIGURE 7

TERMINATING RESISTANCE
vs
FREE-AIR TEMPERATURE

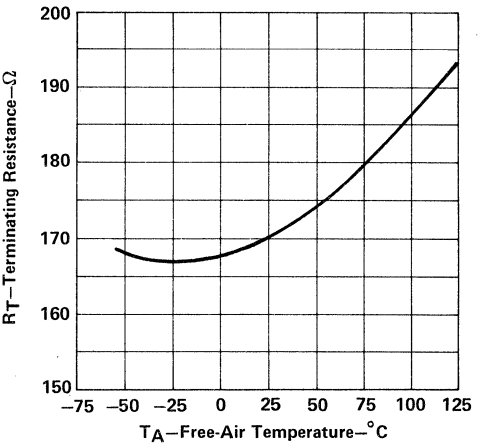


FIGURE 8

†Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
(AVERAGE PER RECEIVER)
vs
COMMON-MODE INPUT VOLTAGE

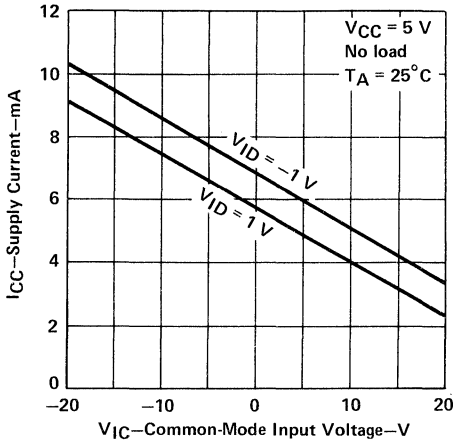


FIGURE 9

POWER DISSIPATION
(AVERAGE PER RECEIVER)
vs
COMMON-MODE INPUT VOLTAGE

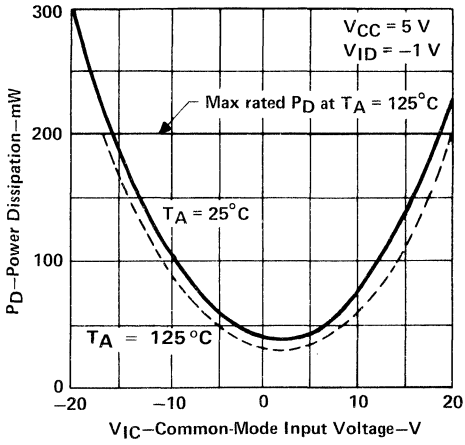


FIGURE 10

NOISE PULSE DURATION
vs
RESPONSE TIME-CONTROL CAPACITANCE

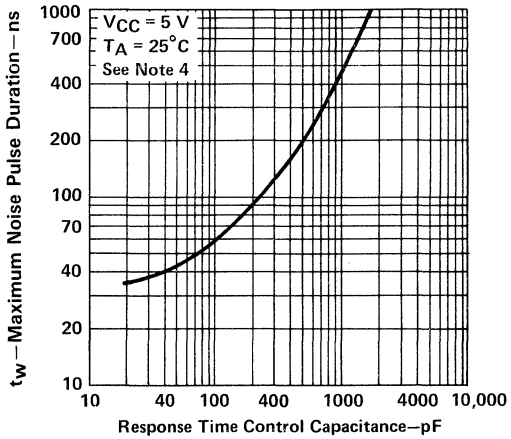
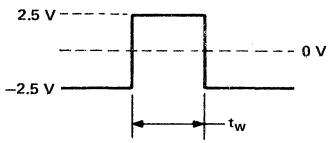


FIGURE 11



INPUT PULSE FOR FIGURE 11

†Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only.

NOTE 4: Figure 11 shows the maximum duration of the illustrated pulse that can be applied differentially without the output changing from the low to high level.

TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIMES FROM DIFFERENTIAL INPUT vs FREE-AIR TEMPERATURE

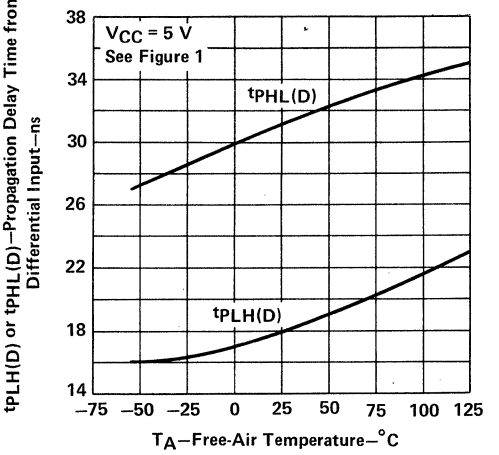


FIGURE 12

PROPAGATION DELAY TIMES FROM STROBE INPUT vs FREE-AIR TEMPERATURE

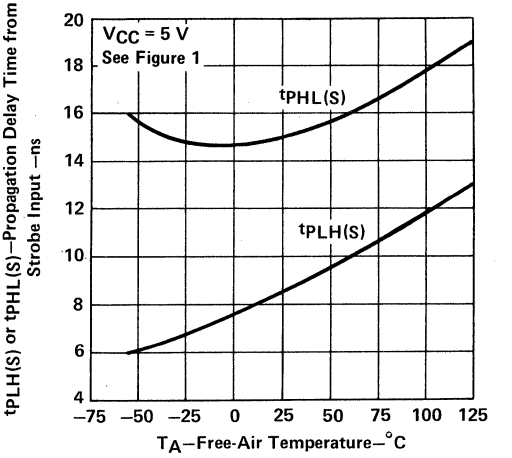


FIGURE 13

†Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only.

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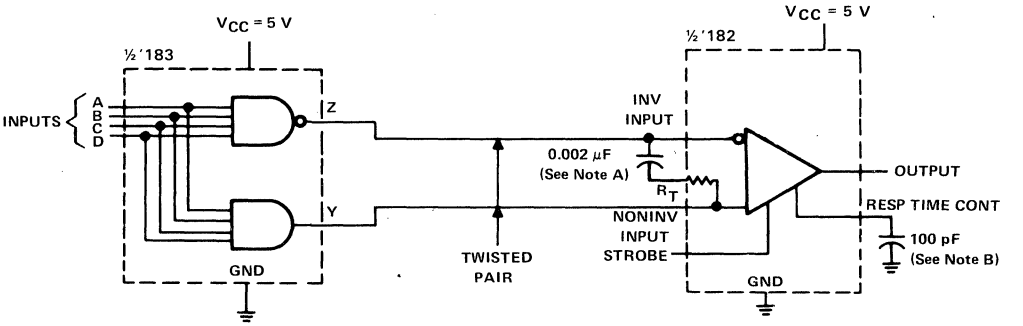
APPLICATION INFORMATION



NOTES: A. When the inputs are open circuited, the output will be high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let $f = 5$ MHz
$C = 0.002\ \mu F$

$$Z_C = \frac{1}{2\pi fC} = \frac{1}{2\pi\ (5 \times 10^6)\ (0.002 \times 10^{-6})}$$

$$Z_C \approx 16\ \Omega$$

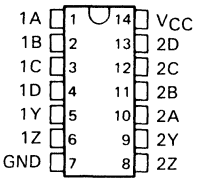
B. Use of a capacitor to control response time is optional.

FIGURE 14. TRANSMISSION OF DIGITAL DATA OVER TWISTED-PAIR LINE

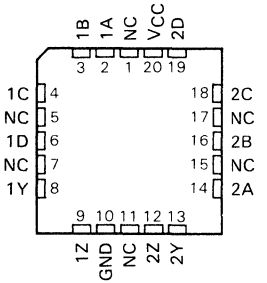
D1292, OCTOBER 1972—REVISED SEPTEMBER 1986

- **Single 5-V Supply**
- **Differential Line Operation**
- **Dual Channels**
- **TTL Compatibility**
- **Short-Circuit Protection of Outputs**
- **Output Clamp Diodes to Terminate Line Transients**
- **High-Current Outputs**
- **Quad Inputs**
- **Single-Ended or Differential AND/NAND Outputs**
- **Designed for Use With Dual Differential Drivers SN55182 and SN75182**
- **Designed to Be Interchangeable With National Semiconductor DS7830 and DS8830**

SN55183 . . . J PACKAGE
SN75183 . . . D, J, OR N PACKAGE
(TOP VIEW)



SN55183 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection.

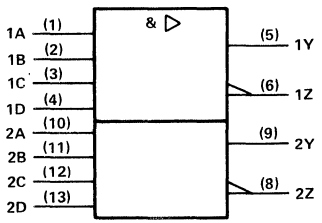
description

The SN55183 and SN75183 dual differential line drivers are designed to provide differential output signals with high-current capability for driving balanced lines, such as twisted-pair, at normal line impedances without high power dissipation. These devices may be used as TTL expander/phase splitters, as the output stages are similar to TTL totem-pole outputs.

The driver is of monolithic single-chip construction, and both halves of the dual circuits use common power supply and ground terminals.

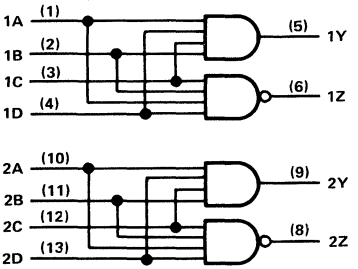
The SN55183 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75183 is characterized for operation from 0°C to 70°C.

logic symbol†



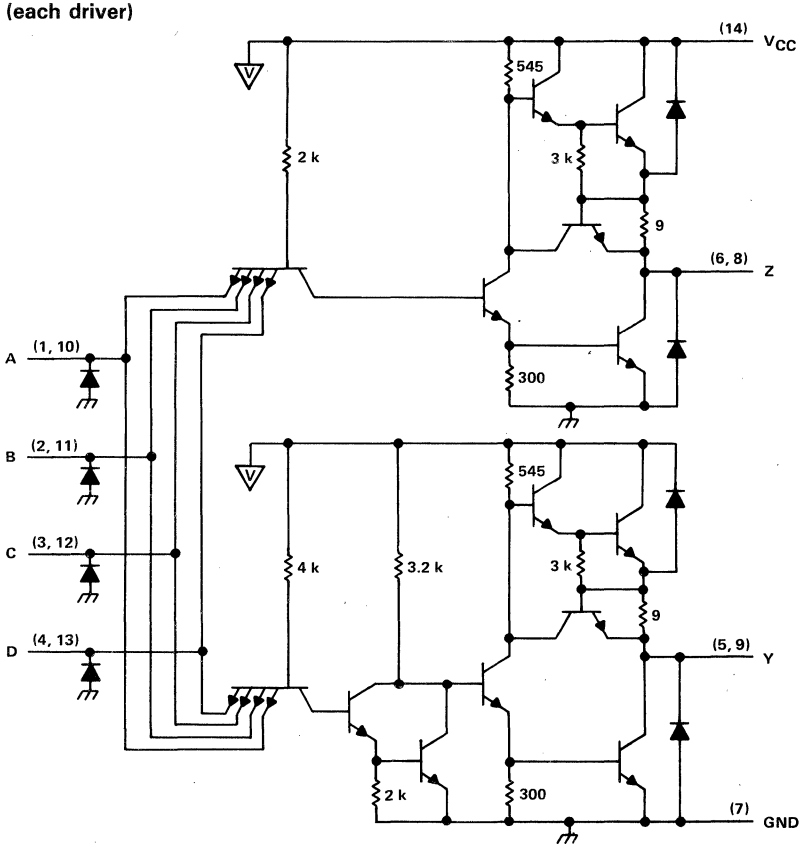
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



positive logic: $Y = \overline{ABCD}$
$Z = \overline{ABCD}$

schematic (each driver)



Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55183	SN75183	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	V
Input voltage	5.5	5.5	V
Duration of output short-circuit (see Note 2)	1	1	s
Continuous total power dissipation (see Note 3)	See Dissipation Rating Table		
Operating free-air temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260	°C
Case temperature for 60 seconds: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300	300	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Not more than one output should be shorted to ground at a time.
3. In the FK and J packages, SN55183 chips are alloy mounted and SN75183 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55183)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75183)	1025 mW	8.2 mW/°C	656 mW	—
N	1150 mW	9.2 mW/°C	736 mW	—

recommended operating conditions

	SN55183			SN75183			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended ranges of V_{CC} and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	Y (AND) OUTPUT	V_{IH} = 2 V,	I_{OH} = −0.8 mA	2.4			V
			V_{IH} = 2 V,	I_{OH} = −40 mA	1.8	3.3		
V_{OL}	Low-level output voltage		V_{IL} = 0.8 V,	I_{OL} = 32 mA		0.2		V
			V_{IL} = 0.8 V,	I_{OL} = 40 mA		0.22	0.4	
V_{OH}	High-level output voltage	Z (NAND) OUTPUT	V_{IL} = 0.8 V,	I_{OH} = −0.8 mA	2.4			V
			V_{IL} = 0.8 V,	I_{OH} = −40 mA	1.8	3.3		
V_{OL}	Low-levael output voltage		V_{IH} = 2 V,	I_{OL} = 32 mA		0.2		V
			V_{IH} = 2 V,	I_{OL} = 40 mA		0.22	0.4	
I_{IH}	High-level input current		V_{IH} = 2.4 V				120	μA
I_I	Input current at maximum input voltage		V_{IH} = 5.5 V				2	mA
I_{IL}	Low-level input current		V_{IL} = 0.4 V				−4.8	mA
I_{OS}	Short-circuit output current‡		V_{CC} = 5 V,	T_A = 125°C	−40	−100	−120	mA
I_{CC}	Supply current (average per driver)		V_{CC} = 5 V, No load	All inputs at 5 V,		10	18	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted to ground at a time and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level Y output	AND gates	C_L = 15 pF, See Figure 1(a)		8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level Y output				12	18	ns
t_{PLH}	Propagation delay time, low-to-high-level Z output	NAND gates			6	12	ns
t_{PHL}	Propagation delay time, high-to-low-level Z output				6	8	ns
t_{PLH}	Propagation delay time, low-to-high-level differential output	Y output with respect to Z output	Z_L = 100 Ω in series with 5000 pF, See Figure 1(b)		9	16	ns
t_{PHL}	Propagation delay time high-to-low-level differential output				8	16	ns

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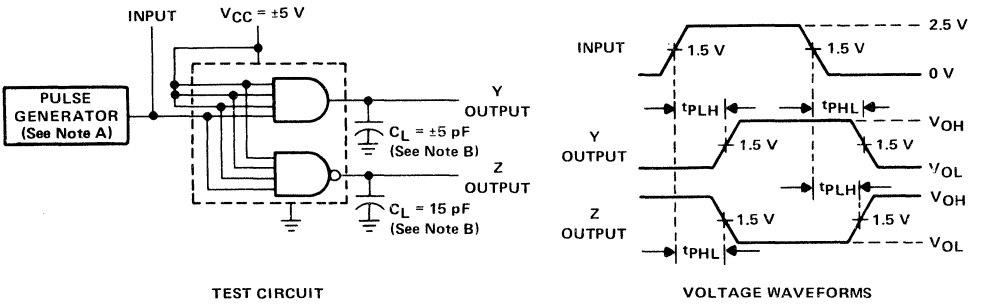
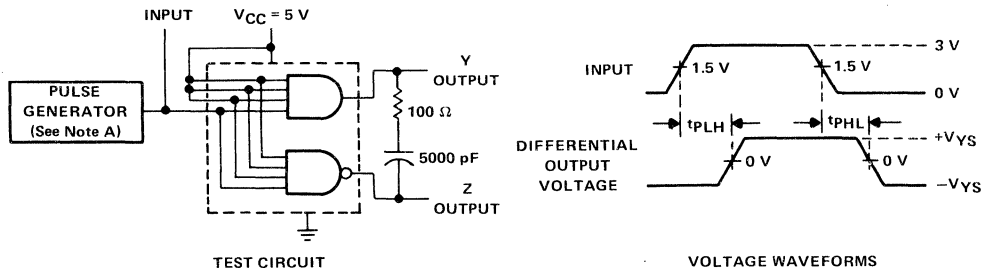
PARAMETER MEASUREMENT INFORMATION



(a) OUTPUTS Y AND Z



(b) DIFFERENTIAL OUTPUT

NOTES: A. The pulse generators have the following characteristics: Z_o = 50 Ω, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns, t_w = 0.5 μs, PRR ≤ 1 MHz.
B. C_L includes probe and jig capacitance.
C. Waveforms are monitored on an oscilloscope with $R_{in} \geq$ 1 MΩ.

FIGURE 1. PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS†

THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

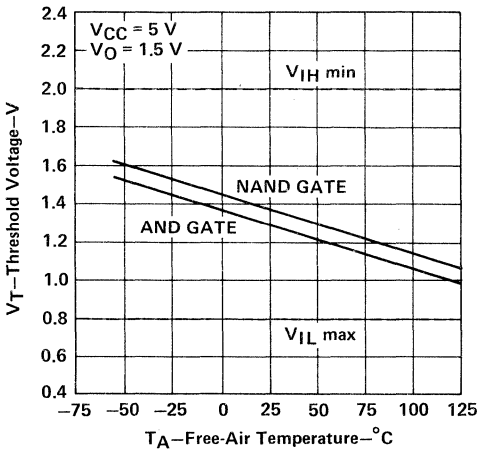


FIGURE 2

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

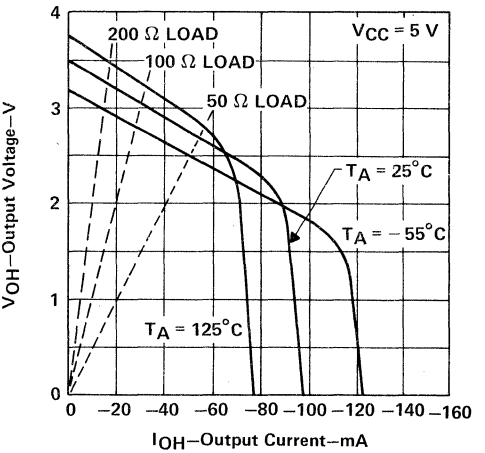


FIGURE 3

DIFFERENTIAL OUTPUT VOLTAGE
vs
DIFFERENTIAL OUTPUT CURRENT

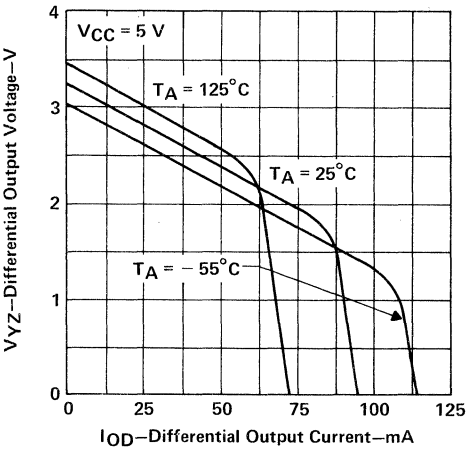


FIGURE 4

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

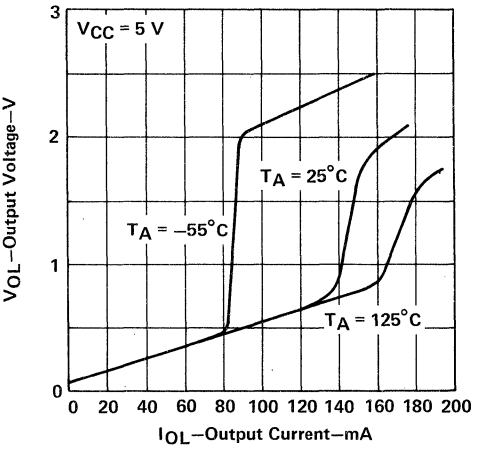


FIGURE 5

†Data for temperatures below 0°C and above 70°C are applicable to SN55183 circuits only.

TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIME OF DIFFERENTIAL OUTPUT vs FREE-AIR TEMPERATURE

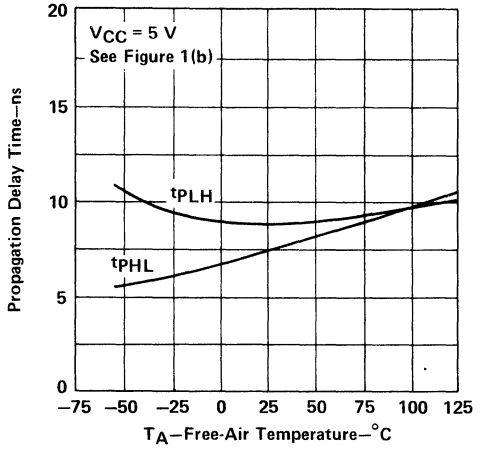


FIGURE 6

TOTAL POWER DISSIPATION (BOTH DRIVERS) vs FREQUENCY

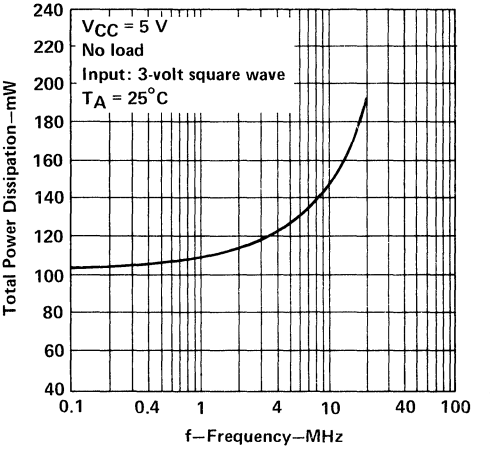
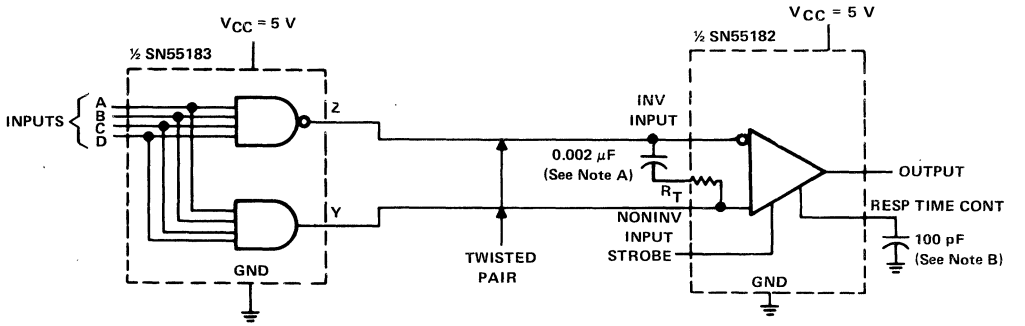


FIGURE 7

†Data for temperatures below 0°C and above 70°C are applicable to SN55183 circuits only.

APPLICATION INFORMATION



NOTES: A. When the inputs are open circuited, the output will be high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let $f = 5$ MHz
$C = 0.002\ \mu F$

$$Z_C = \frac{1}{2\pi fC} = \frac{1}{2\pi\,(5 \times 10^6)\,(0.002 \times 10^{-6})}$$

$$Z_C \approx 16\ \Omega$$

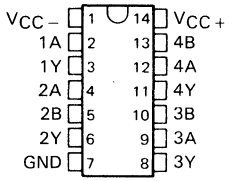
B. Use of a capacitor to control response time is optional.

FIGURE 8. TRANSMISSION OF DIGITAL DATA OVER TWISTED-PAIR LINE

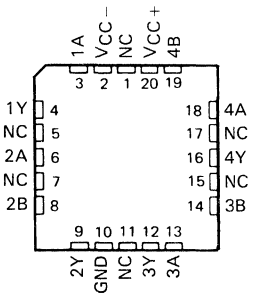
D1323, SEPTEMBER 1983—REVISED SEPTEMBER 1986

- **Meets Specifications of EIA RS-232-C**
- **Designed to Be Interchangeable With Motorola MC1488**
- **Current-Limited Output: 10 mA Typ**
- **Power-Off Output Impedance: 300 Ω Min**
- **Slew Rate Control by Load Capacitor**
- **Flexible Supply Voltage Range**
- **Input Compatible With Most TTL Circuits**

SN55188 . . . J PACKAGE
SN75188 . . . D OR J PACKAGE
(TOP VIEW)



SN55188 . . . FK
CHIP CARRIER PACKAGE
(TOP VIEW)



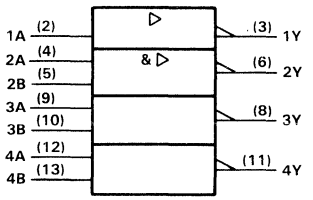
NC—No internal connection

description

The SN55188 and SN75188 are monolithic quadruple line drivers designed to interface data terminal equipment with data communications equipment in conformance with EIA Standard RS-232-C using a diode in series with each supply-voltage terminal as shown under typical applications.

The SN55188 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75188 is characterized for operation from 0°C to 70°C.

logic symbol†



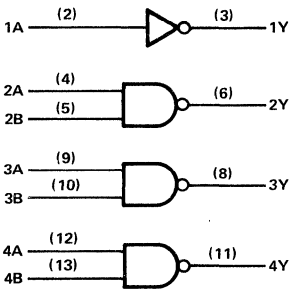
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(DRIVERS 2 THRU 4)

A	B	Y
H	H	L
L	X	H
X	L	H

H = high level,
L = low level,
X = irrelevant

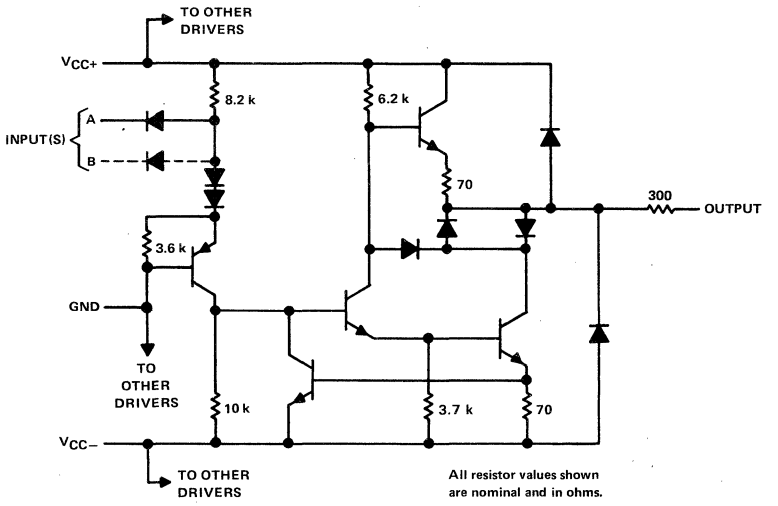
logic diagram (positive logic)



Positive logic
$Y = \overline{A}$ (driver 1)
$Y = \overline{AB}$ or $\overline{A}+\overline{B}$ (drivers 2 thru 4)

Pin numbers shown are for D and J packages.

schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55188	SN75188	UNIT
Supply voltage V_{CC+} at (or below) 25°C free-air temperature (see Notes 1 and 2)		15	15	V
Supply voltage V_{CC-} at (or below) 25°C free-air temperature (see Notes 1 and 2)		−15	−15	V
Input voltage range		−15 to 7	−15 to 7	V
Output voltage range		−15 to 15	−15 to 15	V
Continuous total power dissipation (see Note 2)		See Dissipation Rating Table		
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package	260		°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package	300	300	

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, refer to the maximum supply voltage curve, Figure 6. In the FK and J packages, SN55188 chips are alloy mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	–
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55188)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75188)	1025 mW	8.2 mW/°C	656 mW	–
N	1150 mW	9.2 mW/°C	736 mW	–

recommended operating conditions

	SN55188			SN75188			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}	7.5	9	15	7.5	9	15	V
Supply voltage, V_{CC-}	−7.5	−9	−15	−7.5	−9	−15	V
High-level input voltage, V_{IH}	1.9			1.9			V
Low-level input voltage, V_{IL}			0.8			0.8	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over operating free-air temperature range, V_{CC+} = 9 V, V_{CC-} = −9 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN55188 MIN	SN55188 TYP†	SN55188 MAX	SN75188 MIN	SN75188 TYP†	SN75188 MAX	UNIT
				(See Note 3)			(See Note 3)			
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ	V_{CC+} = 9 V, V_{CC-} = −9 V	6	7		6	7		V
			V_{CC+} = 13.2 V, V_{CC-} = −13.2 V	9	10.5		9	10.5		
V_{OL}	Low-level output voltage	V_{IH} = 1.9 V, R_L = 3 kΩ	V_{CC+} = 9 V, V_{CC-} = −9 V		−7	−6		−7	−6	V
			V_{CC+} = 13.2 V, V_{CC-} = −13.2 V		−10.5	−9		−10.5	−9	
I_{IH}	High-level input current	V_I = 5 V				10			10	μA
I_{IL}	Low-level input current	V_I = 0			−1	−1.6		−1	−1.6	mA
$I_{OS(H)}$	Short-circuit output current at high level‡	V_I = 0.8 V,	V_O = 0	−4.6	−9	−13.5	−6	−9	−12	mA
$I_{OS(L)}$	Short-circuit output current at low level‡	V_I = 1.9 V,	V_O = 0	4.6	9	13.5	6	9	12	mA
r_o	Output resistance, power off	V_{CC+} = 0, V_O = −2 V to 2 V	V_{CC-} = 0,	300			300			Ω
I_{CC+}	Supply current from V_{CC+}	V_{CC+} = 9 V, No load	All inputs at 1.9 V		15	20		15	20	mA
			All inputs at 0.8 V		4.5	6		4.5	6	
		V_{CC+} = 12 V, No load	All inputs at 1.9 V		19	25		19	25	
			All inputs at 0.8 V		5.5	7		5.5	7	
		V_{CC+} = 15 V, No load, T_A = 25°C	All inputs at 1.9 V			34			34	
			All inputs at 0.8 V			12			12	
I_{CC-}	Supply current from I_{CC-}	V_{CC-} = −9 V, No load	All inputs at 1.9 V		−13	−17		−13	−17	mA
			All inputs at 0.8 V			−0.5			−0.015	
		V_{CC-} = −12 V, No load	All inputs at 1.9 V		−18	−23		−18	−23	
			All inputs at 0.8 V			−0.5			−0.015	
		V_{CC-} = −15 V, No load, T_A = 25°C	All inputs at 1.9 V			−34			−34	
			All inputs at 0.8 V			−2.5			−2.5	
P_D	Total power dissipation	V_{CC+} = 9 V, No load	V_{CC-} = −9 V,			333			333	mW
		V_{CC+} = 12 V, No load	V_{CC-} = −12 V,			576			576	

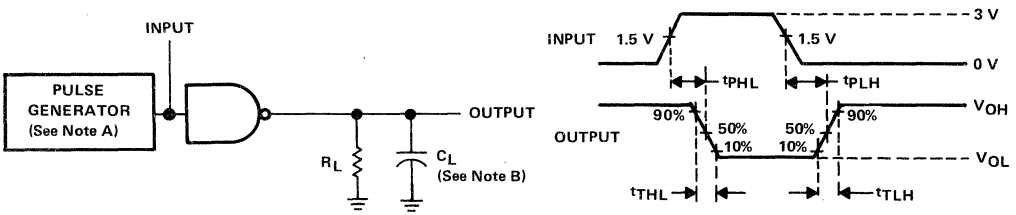
†All typical values are at T_A = 25°C.
‡Not more than one output should be shorted at a time.
NOTE 3: The algebraic convention in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only, e.g., if −6 V is a maximum, the typical value is a more negative voltage.

switching characteristics, V_{CC+} = 9 V, V_{CC-} = −9 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 3 kΩ, C_L = 15 pF, See Figure 1		220	350	ns
t_{PHL}	Propagation delay time, high-to-low-level output			100	175	ns
t_{TLH}	Transition time, low-to-high-level output†			55	100	ns
t_{THL}	Transition time, high-to-low-level output†			45	75	ns
t_{TLH}	Transition time, low-to-high-level output‡	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 1		2.5		μs
t_{THL}	Transition time, high-to-low-level output‡			3.0		μs

†Measured between 10% and 90% points of output waveform.
‡Measured between +3 V and −3 V points on the output waveform (EIA RS-232-C conditions)

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 0.5 μs, PRR ≤ 1 MHz, Z_o = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1. PROPAGATION AND TRANSITION TIMES

TYPICAL CHARACTERISTICS†

VOLTAGE TRANSFER CHARACTERISTICS

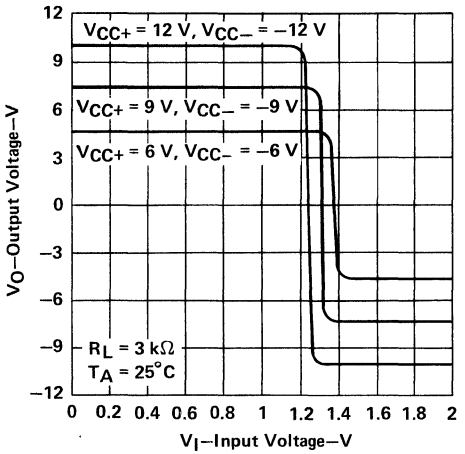


FIGURE 2

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

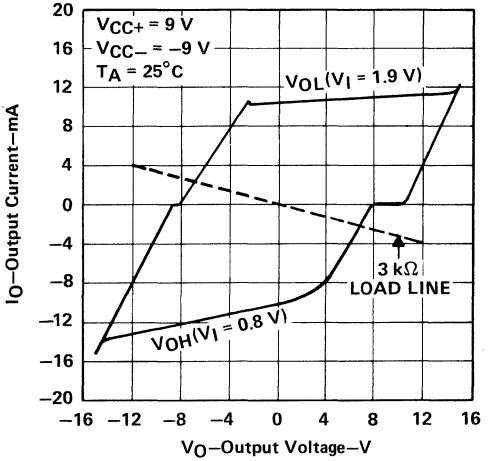


FIGURE 3

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

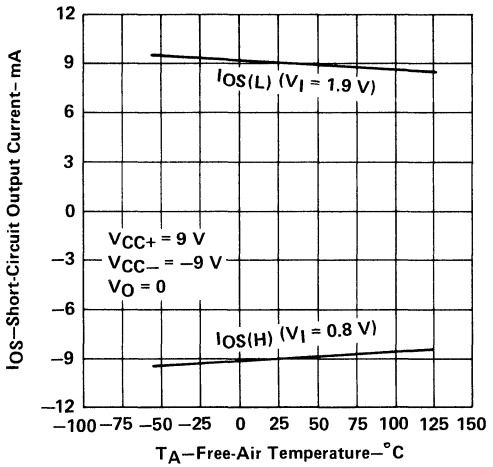


FIGURE 4

SLEW RATE
vs
LOAD CAPACITANCE

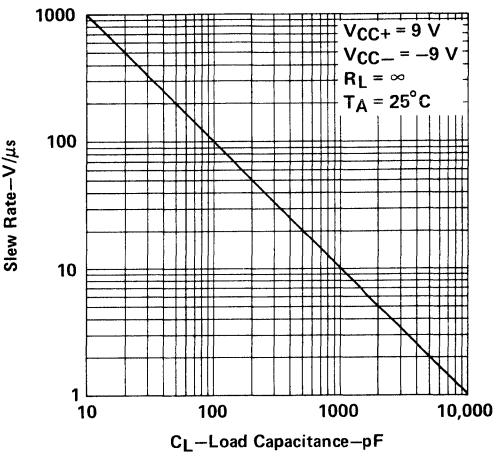


FIGURE 5

†Data for temperatures below 0°C and above 70°C are applicable to SN55188 circuit only.

THERMAL INFORMATION†

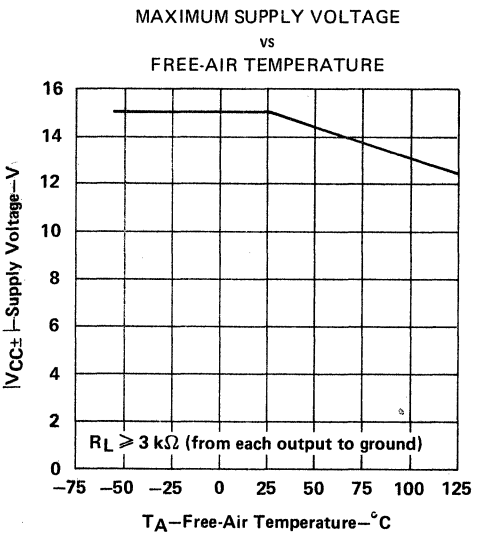


FIGURE 6

†Data for temperatures below 0°C and above 70°C are applicable to SN55188 circuit only.

APPLICATION INFORMATION

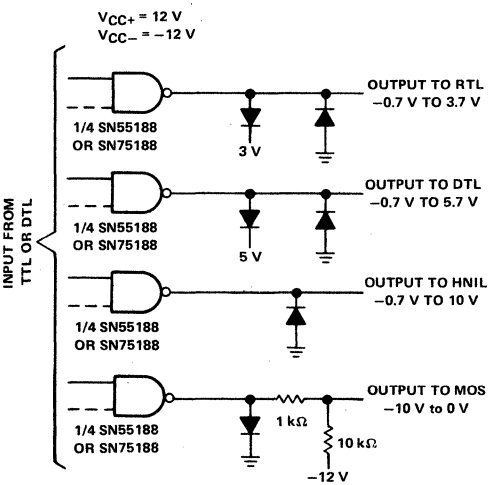


FIGURE 7. LOGIC TRANSLATOR APPLICATIONS

Diodes placed in series with the V_{CC+} and V_{CC-} leads will protect the SN55188/SN75188 in the fault condition in which the device outputs are shorted to ±15 V and the power supplies are at low voltage and provide low-impedance paths to ground.

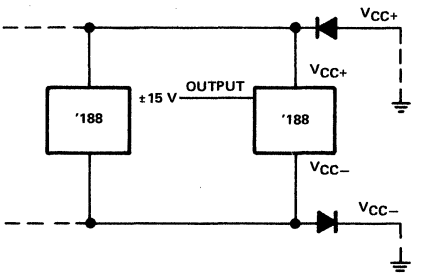
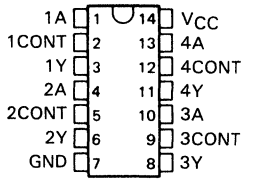


FIGURE 8. POWER SUPPLY PROTECTION TO MEET POWER-OFF FAULT CONDITIONS OF EIA STANDARD RS-232-C

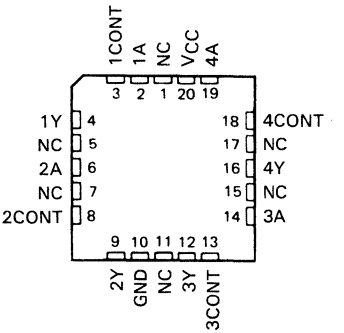
D1619, SEPTEMBER 1973—REVISED MAY 1990

- **Input Resistance . . . 3 kΩ to 7 kΩ**
- **Input Signal Range . . . ±30 V**
- **Operates from Single 5-V Supply**
- **Built-In Input Hysteresis (Double Thresholds)**
- **Response Control Provides:**
  Input Threshold Shifting
  Input Noise Filtering
- **Satisfies Requirements of EIA RS-232-C**
- **Fully Interchangeable with Motorola MC1489, MC1489A**

SN55189, SN55189A . . . J PACKAGE
SN75189, SN75189A . . . D, J, OR N PACKAGE
(TOP VIEW)



SN55189, SN55189A . . . FK PACKAGE
(TOP VIEW)



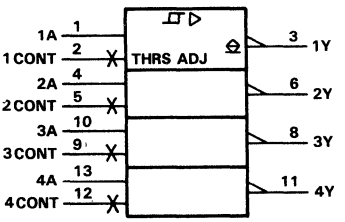
NC—No internal connection

description

These devices are monolithic low-power Schottky quadruple line receivers designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A separate response control terminal is provided for each receiver. A resistor or a resistor and bias voltage source can be connected between this terminal and ground to shift the input threshold levels. An external capacitor can be connected between this terminal and ground to provide input noise filtering.

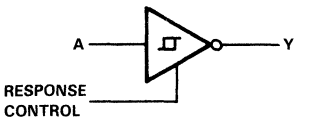
The SN55189 and SN55189A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN75189 and SN75189A are characterized for operation from 0°C to 70°C.

logic symbol†

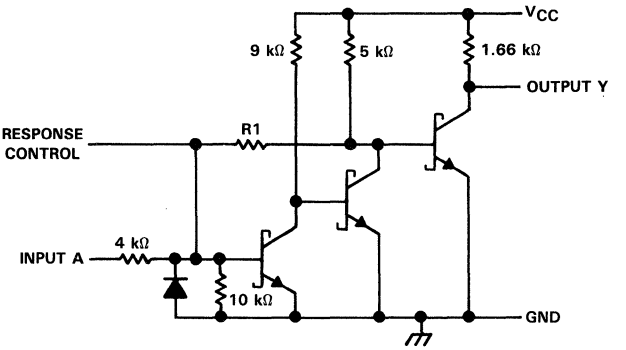


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (each receiver)



schematic (each receiver)



	SN55189 SN75189	SN55189A SN75189A
R1	8.4 kΩ	1.84 kΩ

Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55189 SN55189A	SN75189 SN75189A	UNIT
Supply voltage, V_{CC} (see Note 1)	10	10	V
Input voltage	±30	±30	V
Output current	20	20	mA
Continuous total power dissipation (see Note 2)	See Dissipation Rating Table		
Operating temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260	°C

NOTES: 1. All voltage values are with respect to network ground terminals.
2. In the J package, SN55189 and SN55189A chips are either silver glass or alloy mounted and SN75189 and SN75189A chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55_____)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75_____)	1025 mW	8.2 mW/°C	656 mW	N/A
N	1150 mW	9.2 mW/°C	736 mW	N/A

electrical characteristics over operating free-air temperature range, V_{CC} = 5 V ± 1%, (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SN55189 SN55189A			SN75189 SN75189A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	Positive-going threshold voltage	1	'189	T_A = 25°C	1	1.3	1.5	1	1.3	1.5	V
				T_A = 0°C to 70°C				0.9		1.6	
				T_A = −55°C to 125°C	0.6		1.9				
			'189A	T_A = 25°C	1.75	1.9	2.25	1.75	1.9	2.25	
				T_A = 0°C to 70°C				1.55		2.25	
				T_A = −55°C to 125°C	1.30		2.65				
V_{T-}	Negative-going threshold voltage	1	'189, '189A	T_A = 25°C	0.75	1.0	1.25	0.75	1.0	1.25	V
				T_A = 0°C to 70°C				0.65		1.25	
				T_A = −55°C to 125°C	0.35		1.6				
V_{OH}	High-level output voltage	1	V_I = 0.75 V, I_{OH} = −0.5 mA		2.6	4	5	2.6	4	5	V
			Input open, I_{OH} = −0.5 mA		2.6	4	5	2.6	4	5	
V_{OL}	Low-level output voltage	1	V_I = 3 V, I_{OL} = 10 mA			0.2	0.45		0.2	0.45	V
I_{IH}	High-level input current	2	V_I = 25 V		3.6		8.3	3.6		8.3	mA
			V_I = 3 V		0.43			0.43			
I_{IL}	Low-level input current	2	V_I = −25 V		−3.6		−8.3	−3.6		−8.3	mA
			V_I = −3 V		−0.43			−0.43			
I_{OS}	Short-circuit output current	3				−3			−3		mA
I_{CC}	Supply current	2	V_I = 5 V, Outputs open			20	26		20	26	mA

† All characteristics are measured with the response control terminal open.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	4	C_L = 15 pF, R_L = 3.9 kΩ		25	85	ns
t_{PHL}	Propagation delay time, high-to-low-level outut		C_L = 15 pF, R_L = 390 Ω		25	50	
t_{TLH}	Transition time, low-to-high-level output		C_L = 15 pF, R_L = 3.9 kΩ		120	175	ns
t_{THL}	Transition time, high-to-low-level output		C_L = 15 pF, R_L = 390 Ω		10	20	

PARAMETER MEASUREMENT INFORMATION†

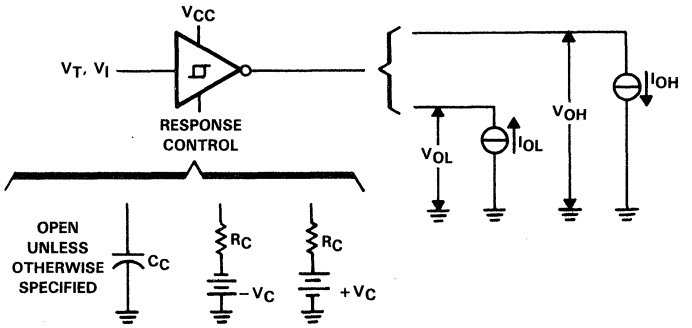
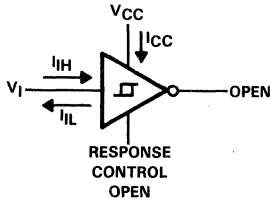


FIGURE 1. V_{T+}, V_{T-}, V_{OH}, V_{OL}



I_{CC} is tested for all four receivers simultaneously

FIGURE 2. I_{IH}, I_{IL}, I_{CC}

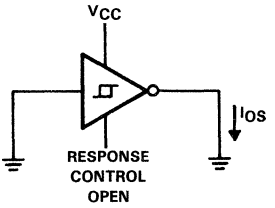
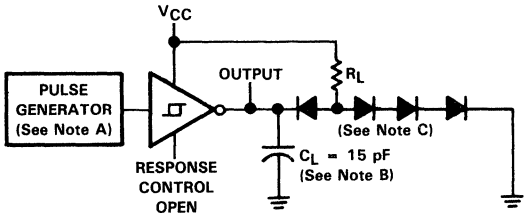


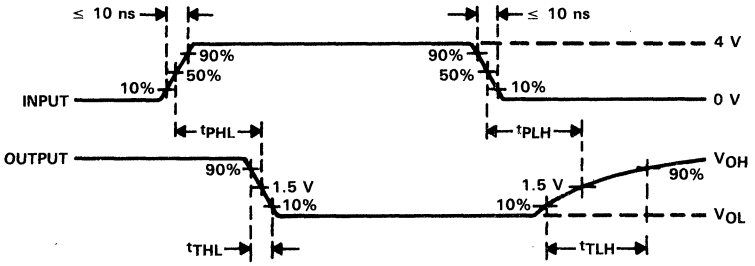
FIGURE 3. I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $Z_O \approx 50\ \Omega$, $t_W = 500$ ns.
B. C_L includes probe and jig capacitances.
C. All diodes are 1N3064 or equivalent.

FIGURE 4. SWITCHING TIMES

TYPICAL CHARACTERISTICS

SN55189, SN75189
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

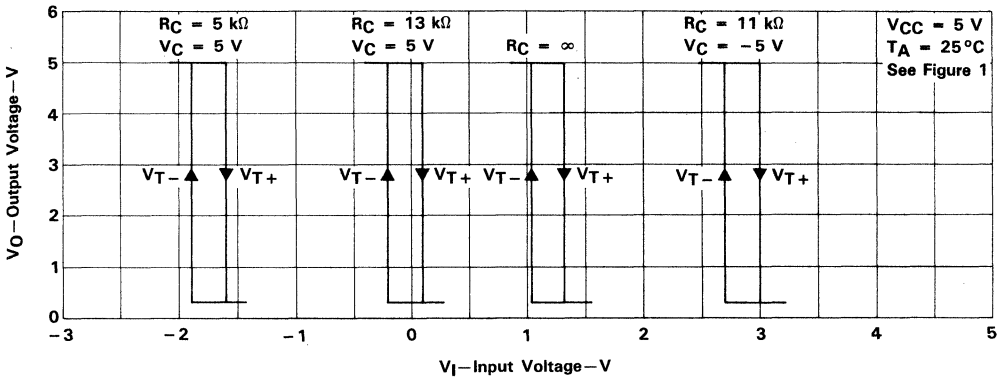


FIGURE 5

SN55189A, SN75189A
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

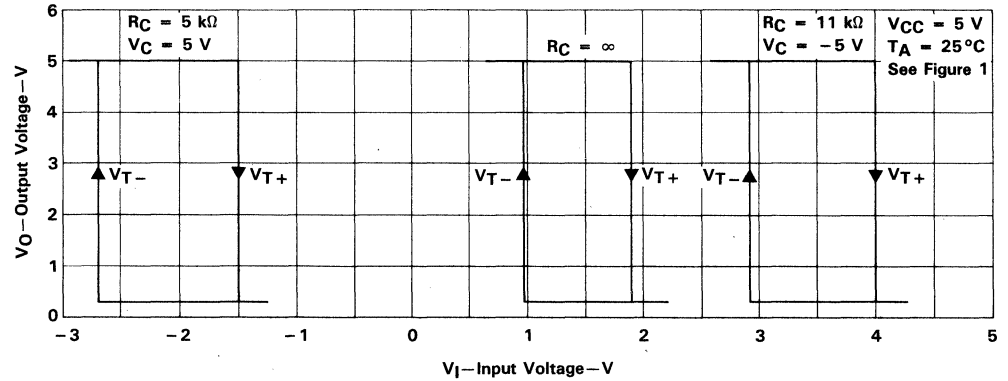


FIGURE 6

TYPICAL CHARACTERISTICS†

INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

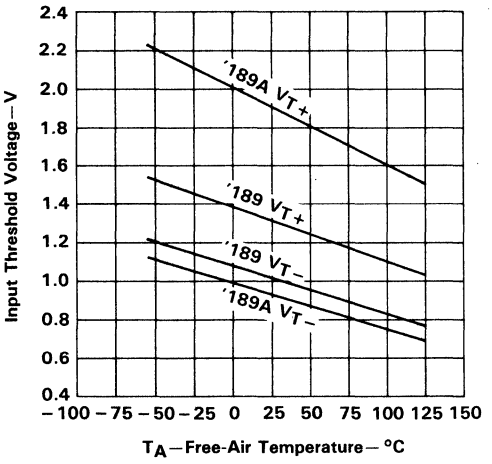


FIGURE 7

INPUT THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

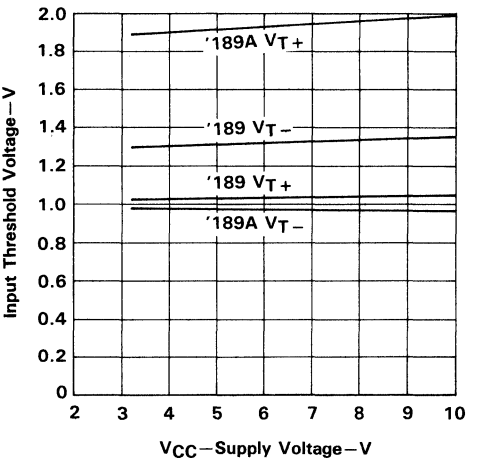


FIGURE 8

†Data for free-air temperatures below 0°C and above 70°C are applicable to SN55189 and SN55189A circuits only.

TYPICAL CHARACTERISTICS

SN75189
NOISE REJECTION

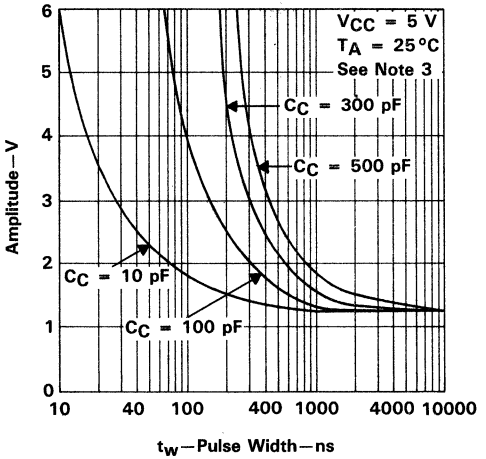


FIGURE 9

SN75189A
NOISE REJECTION

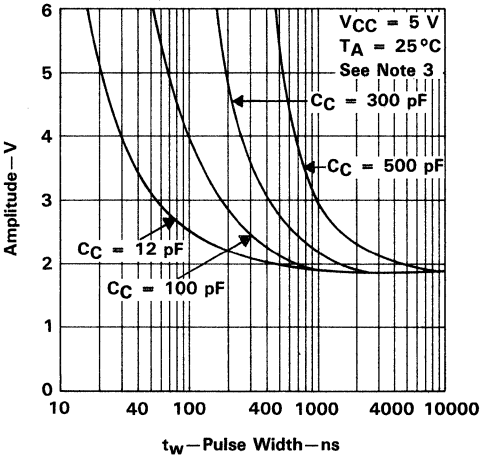


FIGURE 10

INPUT CURRENT
vs
INPUT VOLTAGE

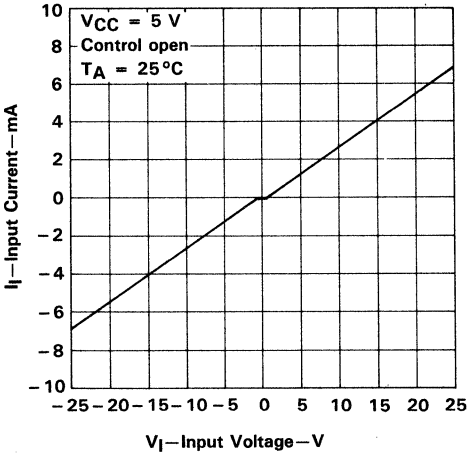


FIGURE 11

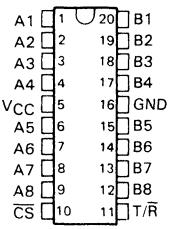
NOTE 3: This figure shows the maximum amplitude of a positive-going pulse that, starting from zero volts, will not cause a change of the output level.

D3275, APRIL 1989

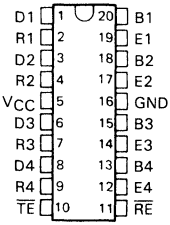
SUITABLE FOR IEEE STANDARD 896 APPLICATIONS†

- SN55ALS056 Is an Octal Transceiver
- SN55ALS057 Is a Quad Transceiver
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 60 mW/Channel Max
- High-Impedance P-N-P Inputs
- BTL™ Logic Level 1-V Bus Swing Reduces Power Consumption
- Trapezoidal Bus Output Waveform Reduces Noise Coupling to Adjacent Lines
- Power-Up/Down Protection (Glitch-Free)
- Open-Collector Driver Outputs Allow Wired-OR Connections

SN55ALS056 . . . J OR W PACKAGE
(TOP VIEW)



SN55ALS057 . . . J OR W PACKAGE
(TOP VIEW)



description

The SN55ALS056 is an 8-channel, monolithic, high-speed, Advanced Low-Power Schottky device designed for 2-way data communication in a densely populated backplane. The SN55ALS057 is a 4-channel version with independent driver input (Dn) and receiver output (Rn) pins and a separate driver disable for each driver (En). Both are compatible with Backplane Tranceiver Logic (BTL™) technology at significantly reduced power dissipation per channel.

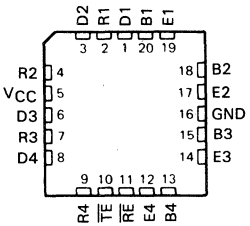
These transceivers feature open-collector driver outputs with a series Schottky diode to reduce capacitive loading to the bus. By using a 2-V pull-up termination on the bus, the output signal swing will be approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs generate trapezoidal waveforms that reduce crosstalk between channels. The drivers are capable of driving an equivalent dc load as low as 18.5 Ω. The receivers have internal low-pass filters to further improve noise immunity.

The SN55ALS056 and SN55ALS057 are characterized for operation from −55°C to 125°C.

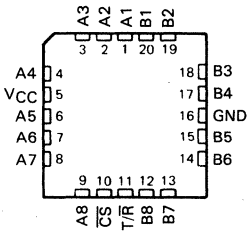
† The transceivers are suitable for IEEE Standard 896 applications to the extent of the operating conditions and characteristics specified in this data sheet. Certain limits contained in the IEEE specification are not met or cannot be tested over the entire military temperature range.

BTL is a trademark of National Semiconductor Corporation.

SN55ALS056 . . . FK PACKAGE
(TOP VIEW)

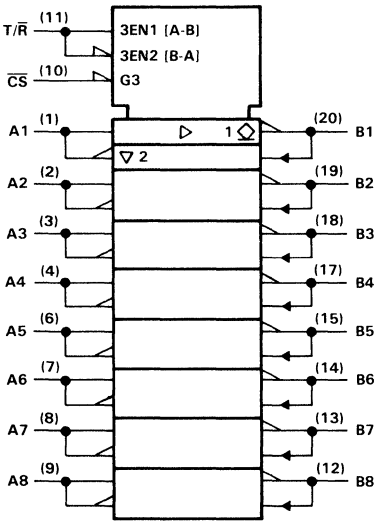


SN55ALS057 . . . FK PACKAGE
(TOP VIEW)

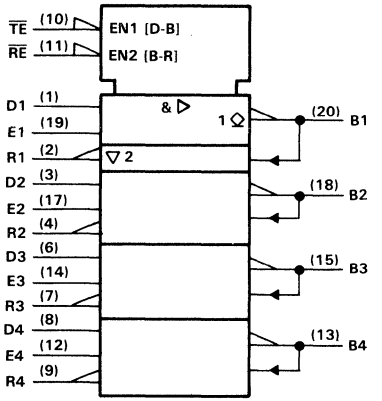


logic symbols†

SN55ALS056



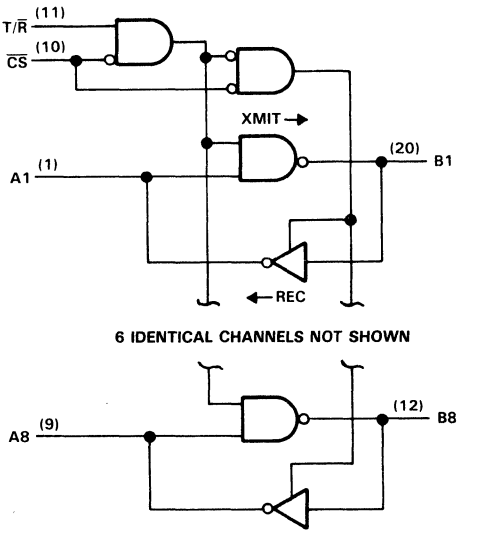
SN55ALS057



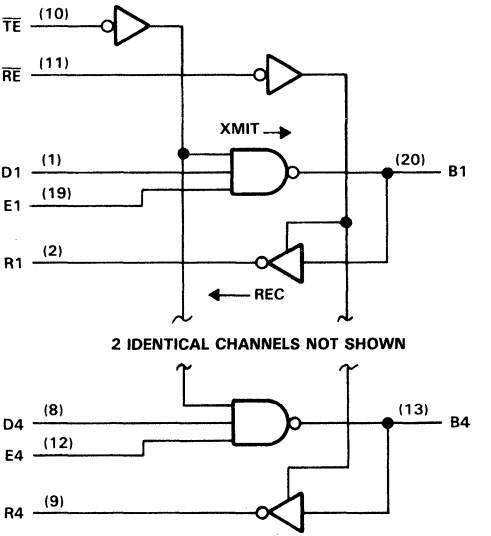
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

SN55ALS056



SN55ALS057



SN55ALS056
FUNCTION TABLE
TRANSMIT/RECEIVE

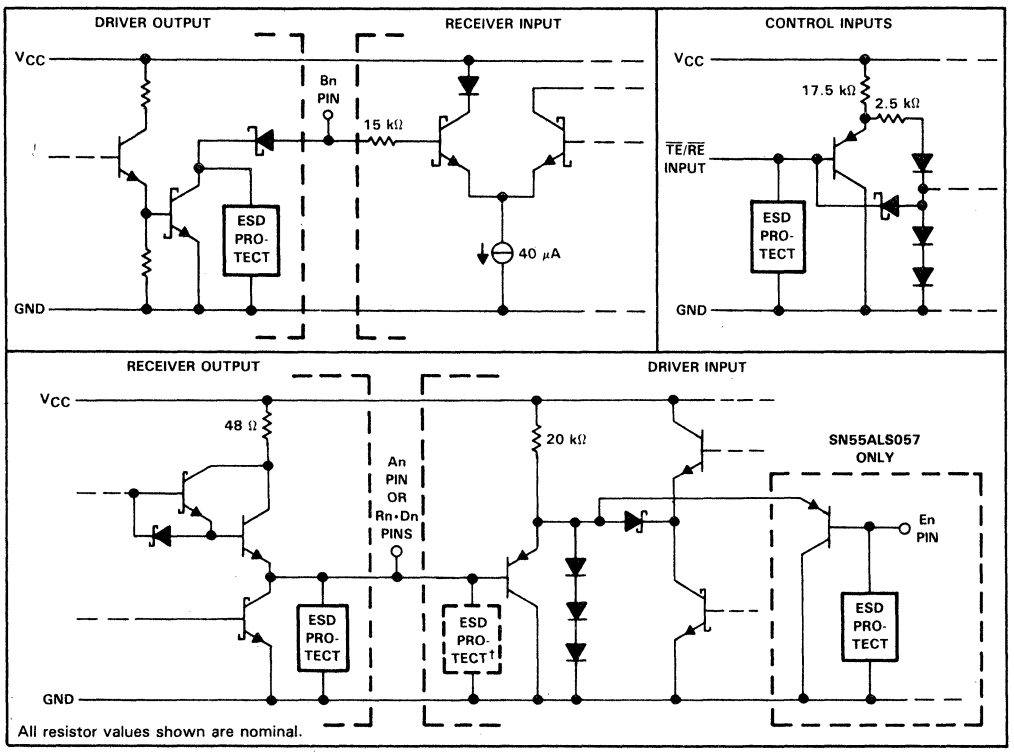
CONTROLS		CHANNELS
$\overline{CS}$	T/$\overline{R}$	A ↔ B
L	H	T (A → B)
L	L	R (B → A)
H	X	D

SN55ALS057
FUNCTION TABLE
TRANSMIT/RECEIVE

CONTROLS			CHANNELS	
$\overline{TE}$	$\overline{RE}$	En	D → B	B → R
L	L	L	D	R
L	L	H	T	R
L	H	L	D	D
L	H	H	T	D
H	L	X	D	R
H	H	X	D	D

H = high-level, L = low-level, R = receive, T = transmit, D = disable, X = irrelevant
Direction of data transmission is from An to Bn for the SN55ALS056 and from Dn to Bn for the SN55ALS057.
Direction of data reception is from Bn to An for the SN55ALS056 and from Bn to Rn for the SN55ALS057.
Data transfer is inverting in both directions.

schematics of inputs and outputs



†Additional ESD protection is on the SN55ALS057, which has separate receiver output and driver input pins.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6 V
Control input voltage . . . . . 5.5 V
Driver input voltage . . . . . 5.5 V
Driver output voltage . . . . . 2.5 V
Receiver input voltage . . . . . 2.5 V
Receiver output voltage . . . . . 5.5 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1375 mW
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds . . . . . 300°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate to 275 mW at 125°C at the rate of 11.0 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level driver and control input voltage, V_{IH}	2			V
Low-level driver and control input voltage, V_{IL}			0.8	V
Bus termination voltage	1.9		2.1	V
Operating free-air temperature, T_A	−55		125	°C

SN55ALS056 electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage at An, T/$\overline{R}$, or $\overline{CS}$		V_{CC} = 4.5 V, I_I = −18 mA			−1.5	V
V_T	Receiver input threshold at Bn		V_{CC} = 5 V, T_A = 25°C	1.45		1.65	V
			V_{CC} = 5 V, T_A = −55°C to 125°C	1.4		1.7	
V_{OH}	High-level output voltage at An		V_{CC} = 4.5, Bn at 1.2 V, $\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V, I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage	An	V_{CC} = 4.5 V, Bn at 2 V, $\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V, T/$\overline{R}$ at 0.8 V, I_{OL} = 16 mA			0.5	V
		Bn	V_{CC} = 4.5 V, An at 2 V, $\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 2 V, See Figure 1	0.75		1.2	
I_{IH}	High-level input current	An, T/$\overline{R}$, or $\overline{CS}$	V_I = V_{CC} = 5.5 V			40	μA
		Bn	V_{CC} = 5.5 V, V_I = 2 V, An at 0.8 V, T/$\overline{R}$ at 0.8 V			100	
I_{IL}	Low-level input current at An, T/$\overline{R}$, or $\overline{CS}$		V_{CC} = 5.5 V, V_I = 0.4 V			−400	μA
I_{OS}	Short-circuit output current at An		V_{CC} = 5.5 V, An at 0 V, Bn at 1.2 V, $\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V	−35		−125	μA
I_{CC}	Supply current		V_{CC} = 5.5 V			85	mA
$C_{o(B)}$	Driver output capacitance				4.5		pF

SN55ALS057 electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage at Dn, En, $\overline{TE}$, or $\overline{RE}$		V_{CC} = 4.5 V, I_I = −18 mA			−1.5	V
V_T	Receiver input threshold at Bn		V_{CC} = 5 V, T_A = 25°C	1.45		1.65	V
			V_{CC} = 5 V, T_A = −55°C to 125°C	1.4		1.7	
V_{OH}	High-level output voltage at Rn		V_{CC} = 4.5, Bn at 1.2 V, $\overline{RE}$ at 0.8 V, I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage	Rn	V_{CC} = 4.5 V, Bn at 2 V, $\overline{RE}$ at 0.8 V, I_{OL} = 16 mA			0.5	V
		Bn	V_{CC} = 4.5 V, Dn at 2 V, En at 2 V, $\overline{TE}$ at 0.8 V See Figure 1	0.75		1.2	
I_{IH}	High-level input current	Dn, En, $\overline{TE}$, or $\overline{RE}$	V_I = V_{CC} = 5.5 V			40	μA
		Bn	V_{CC} = 5.5 V, V_I = 2 V, Dn at 0.8 V, En at 0.8 V, $\overline{TE}$ at 0.8 V			100	
I_{IL}	Low-level input current at Dn, En, $\overline{TE}$, or $\overline{RE}$		V_{CC} = 5.5 V, V_I = 0.4 V			−400	μA
I_{OS}	Short-circuit output current at Rn		V_{CC} = 5.5 V, Rn at 0 V, Bn at 1.2 V, $\overline{RE}$ at 0.8 V	−35		−125	μA
I_{CC}	Supply current		V_{CC} = 5.5 V			45	mA
$C_{o(B)}$	Driver output capacitance				4.5		pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Bn	An	$\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V, V_L = 5 V, S1 closed, See Figure 4	25°C			20	ns
					Full range			22	
t_{PHL}	Propagation delay time, high- to low-level output				25°C			18	
					Full range			20	
t_{PLZ}	Output disable time from low level	$\overline{CS}$	An	Bn at 2 V, T/$\overline{R}$ at 0.8 V, V_L = 5 V, S1 closed, See Figure 5	25°C			20	ns
					Full range			22	
t_{PZL}	Output enable time to low level				25°C			13	
					Full range			14	
t_{PHZ}	Output disable time from high level	$\overline{CS}$	An	Bn at 0.8 V, T/$\overline{R}$ at 0.8 V, V_L = 0, S1 closed, See Figure 5	25°C			12	ns
					Full range			13	
t_{PZH}	Output enable time to high-level			Bn at 0.8 V, T/$\overline{R}$ at 0.8 V, S1 open, See Figure 5	25°C			14	
					Full range			22	
t_{PLZ}	Output disable time from low level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, VC at 2 V, V_L = 5 V, S1 closed, See Figure 5	25°C			17	ns
					Full range			20	
t_{PZL}	Output enable time to low level				25°C			25	
					Full range			40	
t_{PHZ}	Output disable time from high level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, V_L = 0 S1 closed, See Figure 5	25°C			12	ns
					Full range			13	
t_{PZH}	Output enable time to high level			$\overline{CS}$ at 0.8 V, S1 open, See Figure 5	25°C			15	
					Full range			22	
$t_{w(NR)}$	Receiver noise rejection pulse duration	Bn	An or Rn	V_L = 5 V, S1 closed, See Figure 6	25°C	4			ns
					Full range	2			

driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	TYP‡	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	An	Bn	$\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 2 V, V_L = 2 V, See Figure 2	25°C			10	ns
					Full range			40	
t_{PHL}	Propagation delay time, high- to low-level output				25°C			12	
					Full range			15	
t_{PLH}	Propagation delay time, low- to high-level output	$\overline{CS}$	Bn	An and T/$\overline{R}$ at 2 V, V_L = 2 V, See Figure 2	25°C			18	ns
					Full range			30	
t_{PHL}	Propagation delay time, high- to low-level output				25°C			20	
					Full range			22	
t_{PLH}	Propagation delay time, low- to high-level output	T/$\overline{R}$	Bn	$\overline{CS}$ at 0.8 V, V_L = 2 V, See Figure 3	25°C			18	ns
					Full range			37	
t_{PHL}	Propagation delay time, high- to low-level output				25°C			18	
					Full range			21	
t_{TLH}	Transition time, low- to high-level output	An	Bn	$\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 2 V, V_L = 2 V, See Figure 2	25°C	1	3	8	ns
					Full range	1		33	
t_{THL}	Transition time, high- to low-level output				25°C	1	3	10	
					Full range	1		13	

†Full range is −55°C to 125°C.
‡Typical values are at V_{CC} = 5.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Bn	Rn	$\overline{RE}$ at 0.8 V, $\overline{TE}$ at 2 V, V_L = 5 V, S1 closed, See Figure 4	25°C		20	ns
					Full range		22	
t_{PHL}	Propagation delay time, high- to low-level output				25°C		18	
					Full range		20	
t_{PLZ}	Output disable time from low level	$\overline{RE}$	Rn	Bn at 2 V, $\overline{TE}$ at 2 V, V_L = 5 V, S1 closed, See Figure 5	25°C		15	ns
					Full range		17	
t_{PZL}	Output enable time to low level				25°C		13	
					Full range		14	
t_{PHZ}	Output disable time from high level	$\overline{RE}$	Rn	Bn at 0.8 V, $\overline{TE}$ at 2 V, V_L = 0, S1 closed, See Figure 5	25°C		12	ns
					Full range		13	
t_{PZH}	Output enable time to high-level			Bn at 0.8 V, $\overline{TE}$ at 2 V, S1 closed, See Figure 5	25°C		14	
					Full range		15	
$t_{w(NR)}$	Receiver noise rejection pulse duration	Bn	Rn	V_L = 5 V, S1 closed, See Figure 6	25°C	4		ns
					Full range	2		

driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	TYP‡	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Dn or En	Bn	$\overline{TE}$ at 0.8 V, $\overline{RE}$ at 2 V, V_L = 2 V, See Figure 2	25°C			10	ns
					Full range			27	
t_{PHL}	Propagation delay time, high- to low-level output				25°C			12	
					Full range			15	
t_{PLH}	Propagation delay time, low- to high-level output	TE	Bn	Dn, En, $\overline{RE}$ at 2 V, V_L = 2 V, See Figure 2	25°C			10	ns
					Full range			27	
t_{PHL}	Propagation delay time, high- to low-level output				25°C			17	
					Full range			19	
t_{TLH}	Transition time, low- to high-level output	Dn or En	Bn	$\overline{RE}$ at 2 V, V_L = 2 V, See Figure 2	25°C	1	3	8	ns
					Full range	1		33	
t_{THL}	Transition time, high- to low-level output				25°C	1	3	10	
					Full range	1		13	

‡Typical values are at V_{CC} = 5 V.

driver plus receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Dn	Rn	$\overline{RE}$ at 0.8 V, $\overline{TE}$ at 0.8 V, V_L = 2 V, See Figure 7 (Both loads are used)	25°C		25	ns
					Full range		35	
t_{PHL}	Propagation delay time, high- to low-level output				25°C		25	
					Full range		35	

†Full range is −55°C to 125°C.

PARAMETER MEASUREMENT INFORMATION

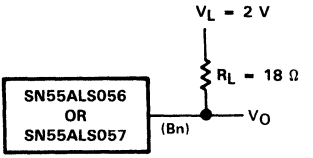
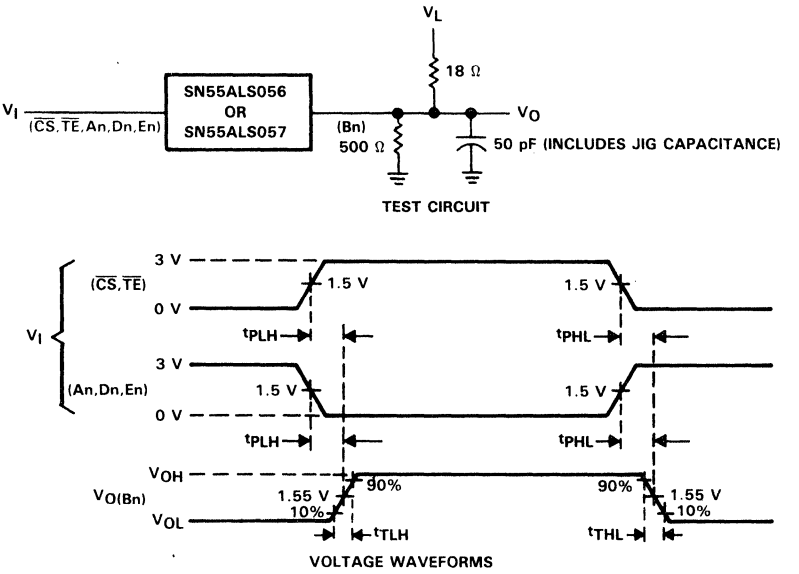


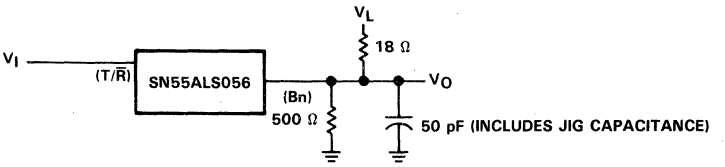
FIGURE 1. TEST CIRCUIT FOR DRIVER LOW-LEVEL OUTPUT VOLTAGE



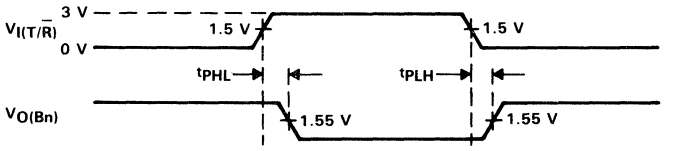
NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%.

FIGURE 2. DRIVER PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



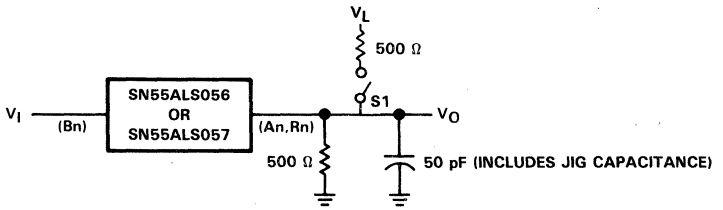
TEST CIRCUIT



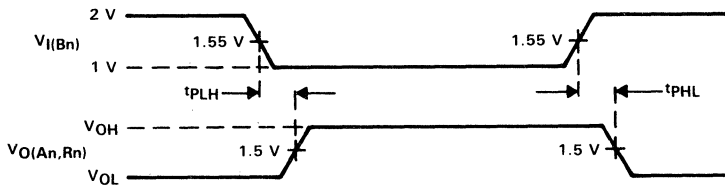
VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%.

FIGURE 3. PROPAGATION DELAY FROM T/$\overline{R}$ TO Bn



TEST CIRCUIT

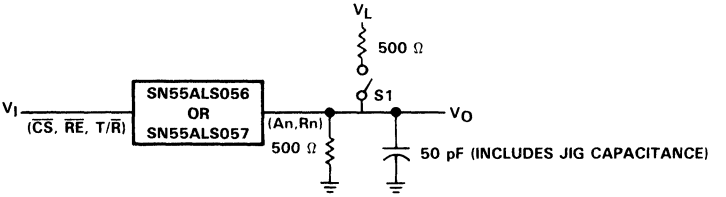


VOLTAGE WAVEFORMS

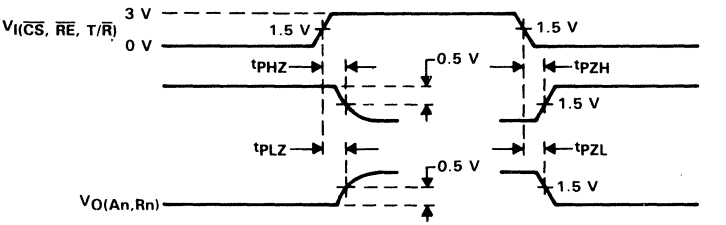
NOTE: $t_r = t_f \leq 10$ ns from 10% to 90%.

FIGURE 4. RECEIVER PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



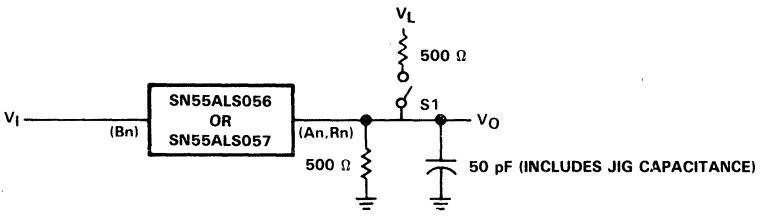
TEST CIRCUIT



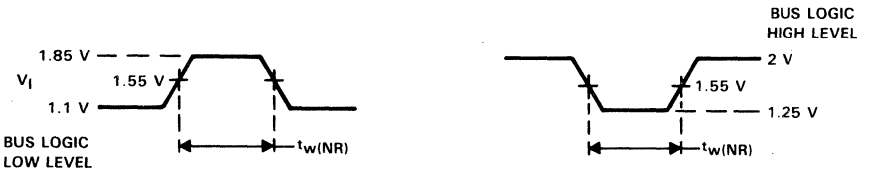
VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%.

FIGURE 5. PROPAGATION DELAY FROM $\overline{CS}$ OR T/$\overline{R}$ TO An OR FROM $\overline{RE}$ TO Rn



TEST CIRCUIT



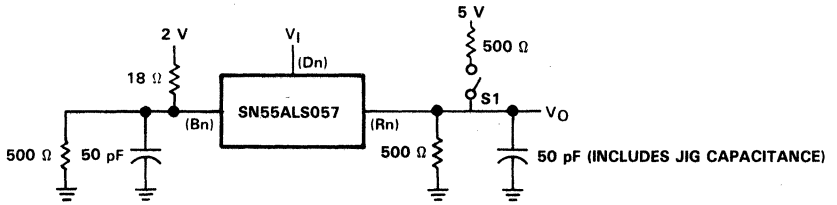
t_w is increased until the output voltage fall just reaches 2.0 V. t_w is increased until the output voltage rise just reaches 0.8 V.

VOLTAGE WAVEFORMS

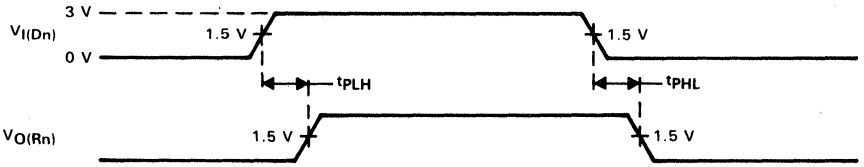
NOTE: $t_r = t_f \leq 2$ ns from 10% to 90%.

FIGURE 6. RECEIVER NOISE IMMUNITY

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

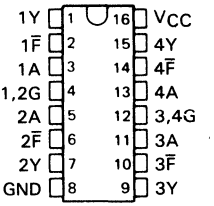
NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%.

FIGURE 7. DRIVER PLUS RECEIVER DELAY TIMES

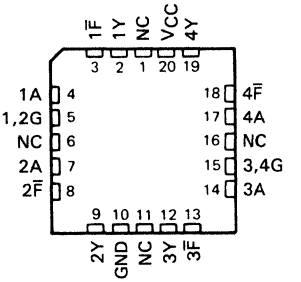
D2299, FEBRUARY 1986—REVISED OCTOBER 1989

- Meets IBM 360/370 I/O Interface Specification GA22-6974-3 (Also See SN55ALS130 and SN75ALS130)
- Minimum Output Voltage of 3.11 V at I_{OH} = −60 mA
- Fault Flag Circuit Output Signals Driver Output Fault
- Fault-Detection Current Limit Circuit Minimizes Power Dissipation During a Fault Condition
- Advanced Low-Power Schottky Circuitry
- Dual Common Enable
- Individual Fault Flags
- Designed to Be an Improved Replacement for the MC3481

SN55ALS126, SN75ALS126 . . . J PACKAGE
SN75ALS126 . . . D OR N PACKAGE
(TOP VIEW)



SN55ALS126 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

INPUTS		OUTPUTS	
G	A	Y	F̄
L	X	L	H
H	H	H	H
H	H	S	L

H = high level, L = low level,
X = irrelevant, S = shorted to ground

description

The SN55ALS126 and SN75ALS126 quadruple line drivers are designed to meet the IBM 360/370 I/O specification GA22-6974-3. The output voltage is 3.11 V minimum (at I_{OH} = −59.3 mA) over the recommended ranges of supply voltage (4.5 V to 5.95 V) and temperature. Driver outputs use a fault-detection current-limit circuit to allow high drive current but still minimize power dissipation when the output is shorted to ground. The SN55ALS126 and SN75ALS126 are compatible with standard TTL logic and supply voltages.

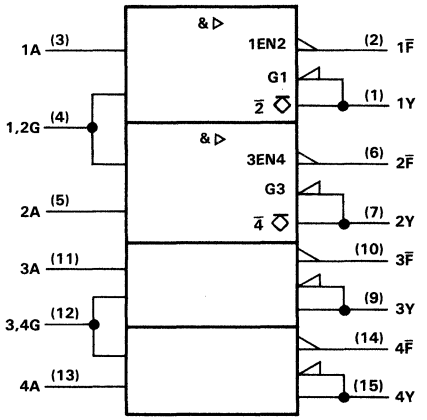
The SN55ALS126 and SN75ALS126 employ the IMPACT™ process to achieve fast switching speeds and low power dissipation. Fault-flag circuitry is designed to sense and signal a line short on any Y line. Upon detecting an output fault condition, the fault-flag circuit forces the driver output into a low state and signals a fault condition by causing the fault-flag output to go low.

The SN55ALS126 and SN75ALS126 can drive a 50-Ω load as required in the IBM GA22-6974-3 specification or a 90-Ω load as used in many I/O systems. Optimum performance can be achieved when the devices are used with either the SN75125, SN75127, SN75128, or SN75129 line receivers.

The SN55ALS126 is characterized for operation from −55°C to 125°C, and the SN75ALS126 is characterized for operation from 0°C to 70°C.

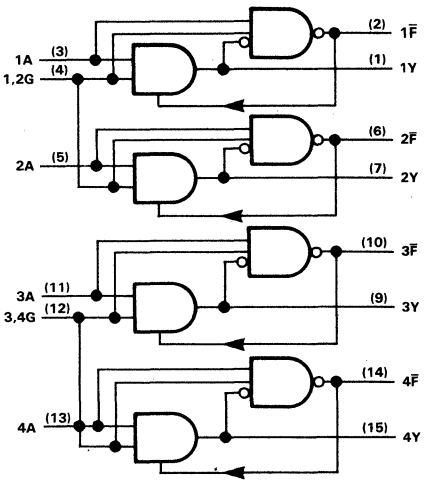
IMPACT is a trademark of Texas Instruments Incorporated

logic symbol†

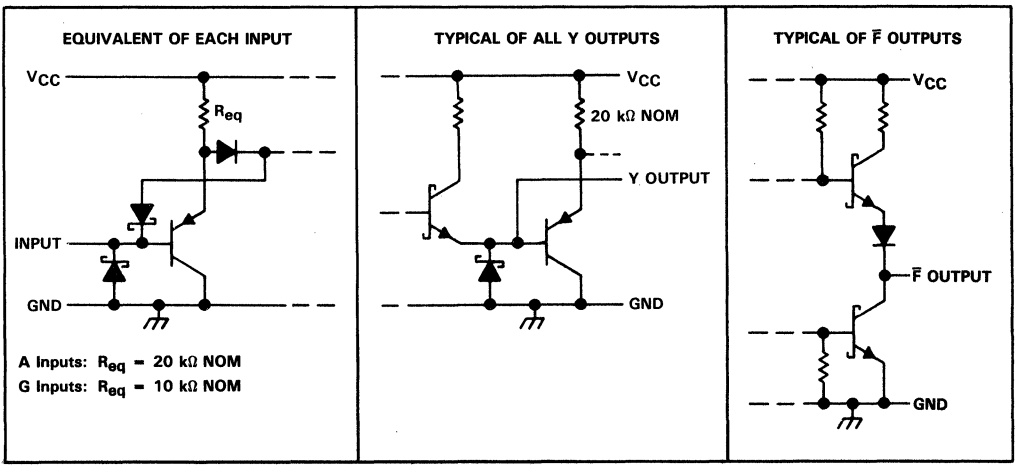


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN55ALS126 . . . . . −55°C to 125°C
SN75ALS126 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55ALS126)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75ALS126)	1025 mW	8.2 mW/°C	656 mW	N/A
N	1150 mW	9.2 mW/°C	736 mW	N/A

recommended operating conditions

	SN55ALS126			SN75ALS126			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.95	4.5	5	5.95	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−59.3			−59.3	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range

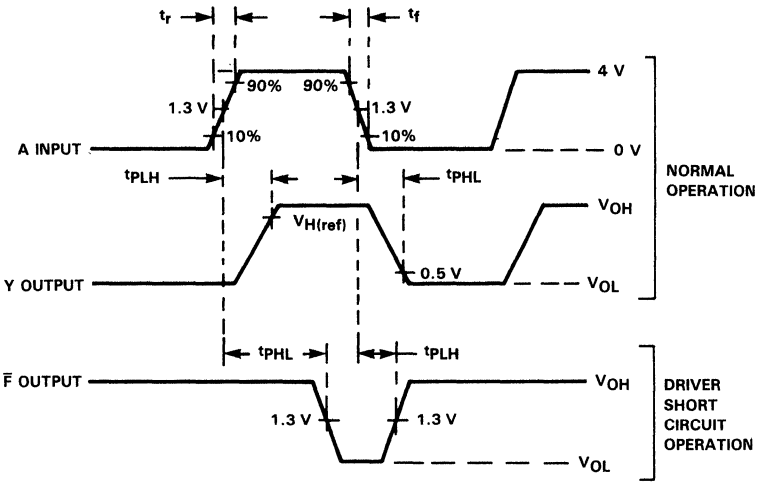
PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{IK}	Input clamp voltage	A,G	V_{CC} = 4.5 V, I_I = −18 mA		−1.5	V
V_{OH}	High-level output voltage	Y	V_{CC} = 4.5 V, I_{OH} = −59.3 mA, V_{IH} = 2 V	3.11		V
		Y	V_{CC} = 5.25 V, I_{OH} = −41 mA, V_{IH} = 2 V	3.9		
		$\overline{F}$	V_{CC} = 4.5 V, I_{OH} = −400 μA, V_{IH} = 2 V	2.5		
V_{OL}	Low-level output voltage	Y	V_{CC} = 5.5 V, I_{OL} = −240 μA, V_{IL} = 0.8 V		0.15	V
		Y	V_{CC} = 5.95 V, I_{OL} = −1 mA, V_{IL} = 0.8 V		0.15	
		$\overline{F}$	V_{CC} = 4.5 V, I_{OL} = 8 mA, Y at 0 V		0.5	
$I_{O(off)}$	Off-state output current	Y	V_{CC} = 4.5 V, V_I = 0, V_O = 3.11 V		100	μA
		Y	V_{CC} = 0, V_I = 0, V_O = 3.11 V		200	
I_I	Input current	A	V_{CC} = 4.5 V, V_I = 5.5 V		100	μA
		G			400	
I_{IH}	High-level input current	A	V_{CC} = 4.5 V, V_I = 2.7 V		20	μA
		G			80	
I_{IL}	Low-level input current	A	V_{CC} = 5.95 V, V_I = 0.4 V		−250	μA
		G			−1000	
I_{OS}	Short-circuit output	Y	V_{CC} = 5.5 V, V_O = 0, V_{IH} = 2.7 V		−5	mA
		$\overline{F}$	V_{CC} = 5.5 V, V_O = 0	−15	−100	
		Y	V_{CC} = 5.95 V, V_O = 0, V_{IH} = 2.7 V		−5	
		$\overline{F}$	V_{CC} = 5.95 V, V_O = 0	−15	−110	
I_{CCH}	Supply current, all outputs high		V_{CC} = 5.5 V, No load, V_{IH} = 2.7 V		25	mA
			V_{CC} = 5.95 V, No load, V_{IH} = 2.7 V		27	
I_{CCL}	Supply current, Y outputs low		V_{CC} = 5.5 V, No load, V_{IL} = 0.4 V		45	mA
			V_{CC} = 5.95 V, No load, V_{IL} = 0.4 V		47	

switching characteristics over recommended operating free-air temperature range

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y	V_{CC} = 4.5 V to 5.5 V, R_L = 50 Ω, C_L = 50 pF, $V_{H(ref)}$ = 3.11 V†, See Figures 1 and 2		30	ns
t_{PHL}	Propagation delay time, high-to-low-level output					28	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times				0.3	3	
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y	V_{CC} = 5.25 V to 5.95 V, R_L = 90 Ω, C_L = 50 pF, $V_{H(ref)}$ = 3.9 V See Figures 1 and 2		34	ns
t_{PHL}	Propagation delay time, high-to-low-level output					34	ns
t_{PLH}	Propagation delay time, low-to-high-level output	A	$\overline{F}$	V_{CC} = 5 V, R_L = 2 kΩ, C_L = 15 pF, See Figures 1 and 2		45	ns
t_{PHL}	Propagation delay time, high-to-low-level output					75	ns

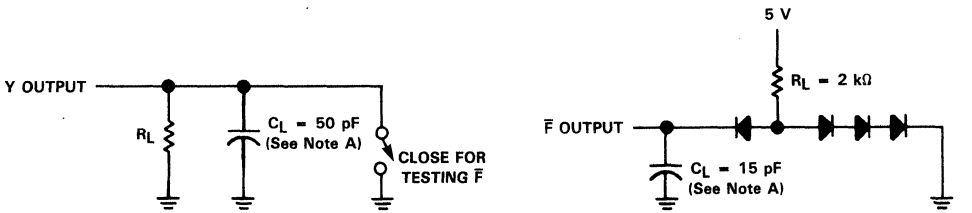
† For SN55ALS126 at T_A = −55°C, $V_{H(ref)}$ = 2.5 V.

PARAMETER MEASUREMENT INFORMATION



NOTE: The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} ≈ 50 Ω.

FIGURE 1. INPUT AND OUTPUT VOLTAGE WAVEFORMS



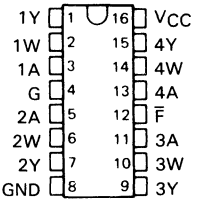
NOTE A: C_L includes probe and stray capacitance.

FIGURE 2. SWITCHING CHARACTERISTICS LOAD CIRCUITS

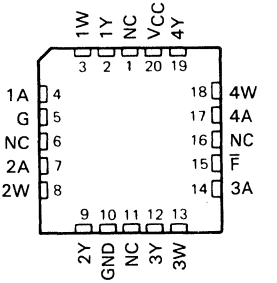
D2299, FEBRUARY 1986—REVISED AUGUST 1989

- **Meets IBM 360/370 I/O Interface Specification GA22-6974-3 (Also see SN55ALS126 and SN75ALS126)**
- **Minimum Output Voltage of 3.11 V at I_{OH} = −60 mA**
- **Fault-Flag Circuit Output Signals Driver Output Fault**
- **Fault-Detection Current Limit Circuit Minimizes Power Dissipation During a Fault Condition**
- **Advanced Low-Power Schottky Circuitry**
- **Common Enable and Common Fault Flag**
- **Designed to be an Improved Replacement for the MC3485**

SN55ALS130 . . . J PACKAGE
SN75ALS130 . . . D, J, OR N PACKAGE
(TOP VIEW)



SN55ALS130 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN55ALS130 and SN75ALS130 quadruple line drivers are designed to meet the IBM 360/370 I/O specification GA22-6974-3. The output voltage is 3.11 V minimum (at I_{OH} = −59.3 mA) over the recommended ranges of supply voltage (4.5 V to 5.95 V) and temperature. Driver outputs use a fault-detection current-limit circuit to allow high drive current but still minimize power dissipation when the output is shorted to ground. The SN55ALS130 and SN75ALS130 are compatible with standard TTL logic and supply voltages.

The SN55ALS130 and SN75ALS130 employ the IMPACT™ process to achieve fast switching speeds and low power dissipation. Fault-flag circuitry is designed to sense and signal a line short on any Y line. Upon detecting an output fault condition, the fault-flag circuit forces the driver output into a low state and signals a fault condition by causing the fault-flag output to go low.

The SN55ALS130 and SN75ALS130 can drive a 50-Ω load as required in the IBM GA22-6974-3 specification or a 90-Ω load as used in many I/O systems. Optimum performance can be achieved when the devices are used with either the SN75125, SN75127, SN75128, or SN75129 line receivers.

The SN55ALS130 is characterized for operation from −55°C to 125°C. The SN75ALS130 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS		OUTPUTS		
G†	A	Y	F̄	W
L	X	L	H	H
X	L	L	H	H
H	H	H	H	L
H	H	S	L	H

H = high level, L = low level, X = irrelevant, S = shorted to ground

†G and F̄ are common to the four drivers. If any of the four Y outputs is shorted, the Fault-Flag will respond.

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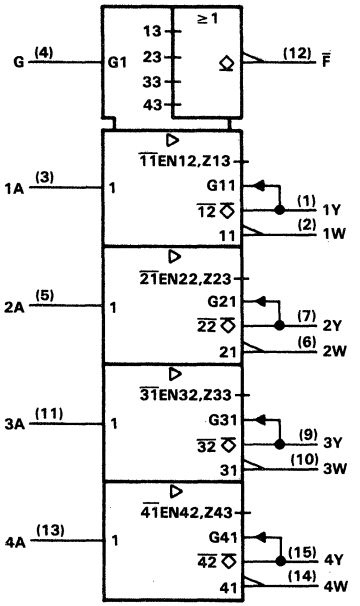
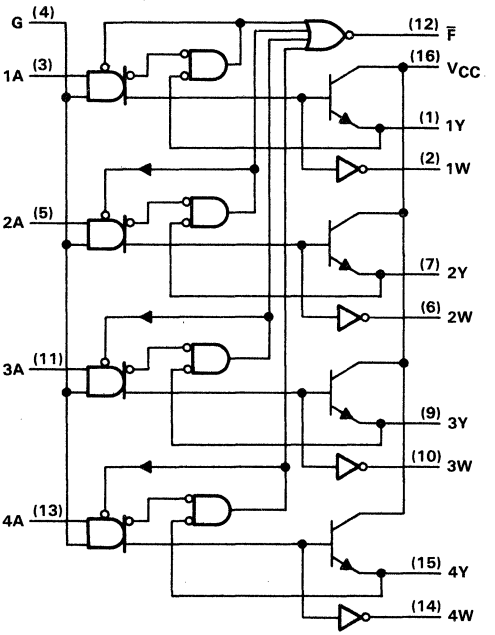
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

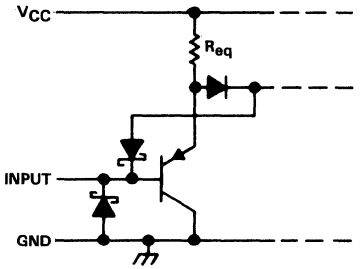
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



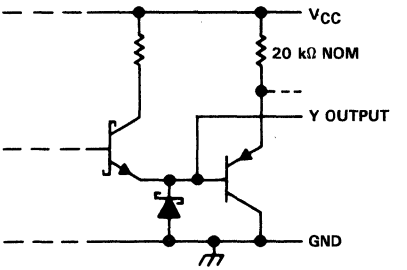
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

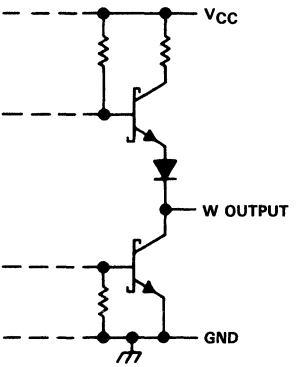


A Inputs: R_{eq} = 20 kΩ NOM
G Inputs: R_{eq} = 10 kΩ NOM

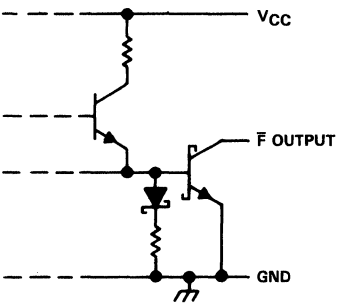
TYPICAL OF ALL Y OUTPUTS



TYPICAL OF ALL W OUTPUTS



TYPICAL OF $\overline{F}$ OUTPUT



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN55ALS130 . . . . . −55°C to 125°C
SN75ALS130 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55ALS130)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75ALS130)	1025 mW	8.2 mW/°C	656 mW	N/A
N	1150 mW	9.2 mW/°C	736 mW	N/A

recommended operating conditions

	SN55ALS130			SN75ALS130			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.95	4.5	5	5.95	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−59.3			−59.3	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range

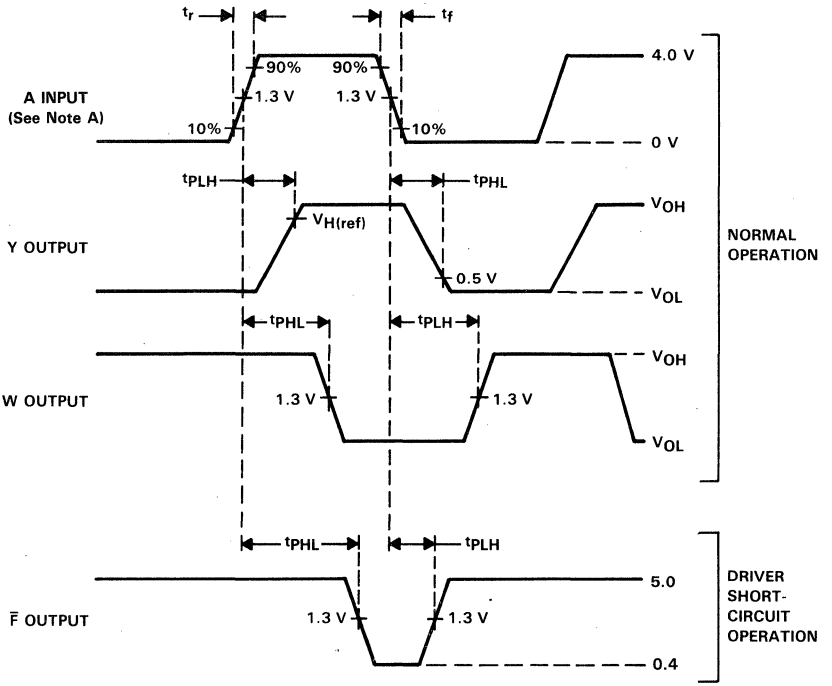
PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{IK}	Input clamp voltage	A,G	V_{CC} = 4.5 V, I_I = −18 mA		−1.5	V
V_{OH}	High-level output voltage	Y	V_{CC} = 4.5 V, I_{OH} = −59.3 mA, V_{IH} = 2 V	3.11		V
		Y	V_{CC} = 5.25 V, I_{OH} = −41 mA, V_{IH} = 2 V	3.9		
		W	V_{CC} = 4.5 V, I_{OH} = −400 μA, V_{IH} = 2 V	2.5		
V_{OL}	Low-level output voltage	Y	V_{CC} = 5.5 V, I_{OL} = −240 μA, V_{IL} = 0.8 V		0.15	V
		Y	V_{CC} = 5.95 V, I_{OL} = −1 mA, V_{IL} = 0.8 V		0.15	
		$\overline{F}$	V_{CC} = 4.5 V, I_{OL} = 8 mA, Y at 0 V		0.5	
		W	V_{CC} = 4.5 V, I_{OL} = 8 mA		0.5	
$I_{O(off)}$	Off-state output current	Y	V_{CC} = 4.5 V, V_{IL} = 0, V_O = 3.11 V		100	μA
		Y	V_{CC} = 0, V_{IL} = 0, V_O = 3.11 V		200	
I_{OH}	High-level output current	$\overline{F}$	V_{CC} = 5.95 V, V_{OH} = 5.95 V		100	μA
I_I	Input current	A	V_{CC} = 4.5 V, V_{IH} = 5.5 V		100	μA
		G			400	
I_{IH}	High-level input current	A	V_{CC} = 4.5 V, V_{IH} = 2.7 V		20	μA
		G			80	
I_{IL}	Low-level input current	A	V_{CC} = 5.95 V, V_{IL} = 0.4 V		250	μA
		G			−1000	
I_{OS}	Short-circuit output	Y	V_{CC} = 5.5 V, V_O = 0, V_{IH} = 2.7 V		−5	mA
		W	V_{CC} = 5.5 V, V_O = 0	−15	−100	
		Y	V_{CC} = 5.95 V, V_O = 0, V_{IH} = 2.7 V		−5	
		W	V_{CC} = 5.95 V, V_O = 0	−15	−110	
I_{CCH}	Supply current, all outputs high		V_{CC} = 5.5 V, No load, V_{IH} = 2.7 V		30	mA
			V_{CC} = 5.95 V, No load, V_{IH} = 2.7 V		32	
I_{CCL}	Supply current, Y outputs low		V_{CC} = 5.5 V, No load, V_{IL} = 0.4 V		45	mA
			V_{CC} = 5.95 V, No load, V_{IL} = 0.4 V		47	

switching characteristics over recommended operating free-air temperature range

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y	V_{CC} = 4.5 V to 5.5 V, R_L = 50 Ω, C_L = 50 pF, $V_{H(ref)}$ = 3.11 V†, Input f = 1 MHz, See Figures 1 and 2		30	ns
t_{PHL}	Propagation delay time, high-to-low-level output					28	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times				0.3	3	
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y	V_{CC} = 5.25 V to 5.95 V, R_L = 90 Ω, C_L = 50 pF, $V_{H(ref)}$ = 3.9 V, Input f = 5 MHz, See Figures 1 and 2		34	ns
t_{PHL}	Propagation delay time, high-to-low-level output					34	ns
t_{PLH}	Propagation delay time, low-to-high-level output	A	W	V_{CC} = 5 V, R_L = 2 kΩ, C_L = 15 pF, See Figures 1 and 2		34	ns
t_{PHL}	Propagation delay time, high-to-low-level output					21	ns
t_{PLH}	Propagation delay time, low-to-high-level output	A	$\overline{F}$	V_{CC} = 5 V, R_L = 2 kΩ, C_L = 15 pF, See Figures 1 and 2		45	ns
t_{PHL}	Propagation delay time, high-to-low-level output					75	ns

† For SN55ALS130 at T_A = −55°C, $V_{H(ref)}$ = 2.5 V.

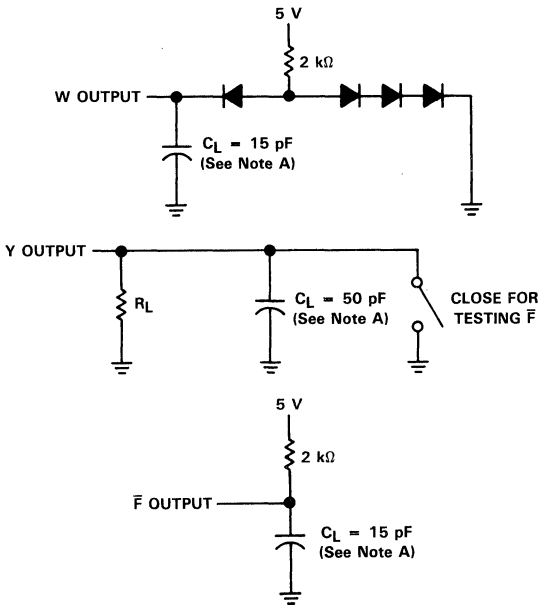
PARAMETER MEASUREMENT INFORMATION



NOTE A: The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} ≈ 50 Ω.

FIGURE 1. INPUT AND OUTPUT VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and stray capacitance.

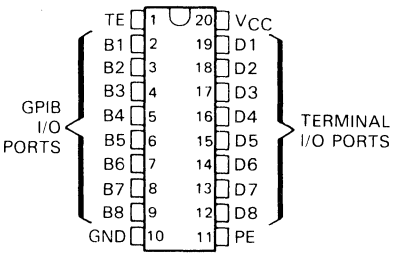
FIGURE 2. SWITCHING CHARACTERISTICS LOAD CIRCUITS

D3276, APRIL 1989

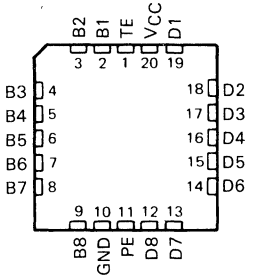
SUITABLE FOR IEEE STANDARD 488-1978 (GPIB)†

- 8-Channel Bidirectional Transceiver
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 56 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 550 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

J OR W PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



description

The SN55ALS160 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky device designed for two-way data communications over single-ended transmission lines. The transceiver features driver outputs that can be operated in either the passive-pullup or three-state mode. If Talk Enable (TE) is high, these ports have the characteristics of passive-pullup outputs when Pullup Enable (PE) is low and of three-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. The driver outputs are designed to handle loads up to 48 mA of sink current.

An active turn-off feature has been incorporated into the bus-terminating resistors so that the device exhibits a high impedance to the bus when V_{CC} = 0. When combined with the SN55ALS161 management bus transceiver, the device provides the complete 16-wire interface for the IEEE 488 bus.

The SN55ALS160 is characterized for operation from −55°C to 125°C.

FUNCTION TABLES

EACH DRIVER

INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z†
X	L	X	Z†

EACH RECEIVER

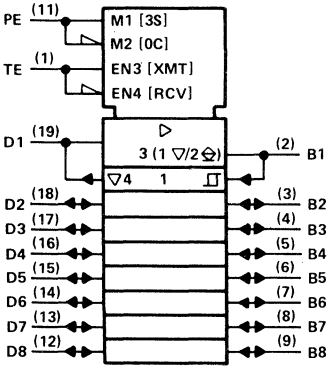
INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

H = high level, L = low level, X = irrelevant,
Z = high-impedance state.

† This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and ground.

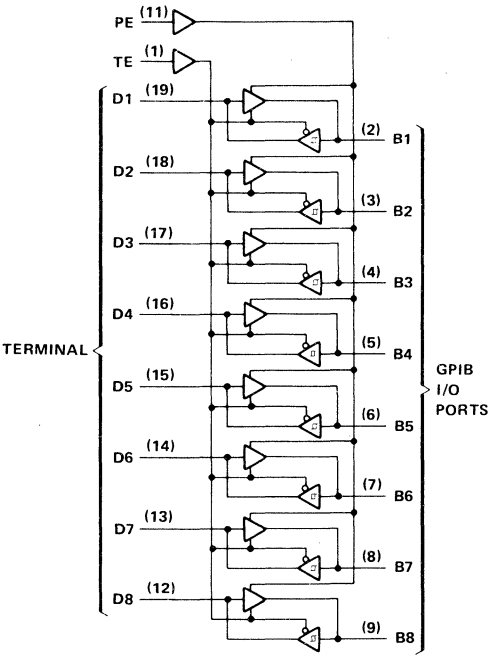
†The transceivers are suitable for IEEE Standard 896 applications to the extent of the operating conditions and characteristics specified in this data sheet. Certain limits contained in the IEEE specification are not met or cannot be tested over the entire military temperature range.

logic symbol†



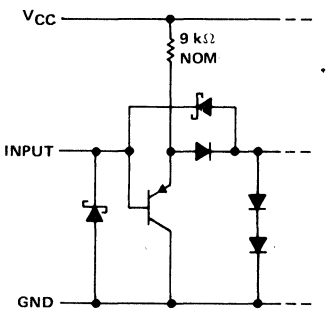
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

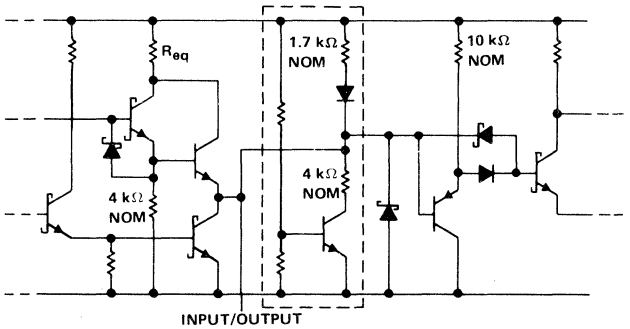


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): . . . . . 1375 mW
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J or W package . . . . . 300°C
Case temperature for 60 seconds: FK package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate to 275 mW at 125°C at the rate of 11.0 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	TE and PE at T_A = −55°C to 125°C	2			V
	Bus and terminal at T_A = 25°C or 125°C	2			
	Bus and terminal at T_A = −55°C	2.1			
Low-level input voltage, V_{IL}	TE and PE at T_A = −55°C to 125°C			0.8	V
	Bus and terminal at T_A = 25°C or −55°C			0.8	
	Bus and terminal at T_A = 125°C			0.7	
High-level output current, I_{OH}	Bus ports with pullups active (V_{CC} = 5 V)			−5.2	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V, I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus	V_{CC} = 5 V, T_A = 25°C		0.4	0.55		V
			V_{CC} = 5 V, T_A = 125°C		0.25			
			V_{CC} = 5 V, T_A = −55°C		0.4			
V_{OH}	High-level output voltage	Terminal	V_{CC} = 4.75 V, I_{OH} = −800 μA, TE at 0.8 V		2.7	3.5		V
		Bus	V_{CC} = 5 V, I_{OH} = −5.2 mA, PE and TE at 2 V		2.5	3.3		
			V_{CC} = 4.75 V, I_{OH} = −5.2 mA, PE and TE at 2 V		2.2			
V_{OL}	Low-level output voltage	Terminal	V_{CC} = 4.75 V, I_{OL} = 16 mA, TE at 0.8 V			0.3	0.5	V
		Bus	V_{CC} = 4.75 V, I_{OL} = 48 mA, TE at 2 V, T_A = 25°C or 125°C			0.35	0.5	
			V_{CC} = 4.75 V, I_{OL} = 48 mA, TE at 2 V, T_A = −55°C			0.35	0.55	
I_I	Input current at maximum input voltage	Terminal	V_{CC} = 5.25 V, V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal, PE, or TE	V_{CC} = 5.25 V, V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current		V_{CC} = 5.25 V, V_I = 0.5 V			−30	−100	μA
$V_{IO(bus)}$	Voltage at bus port		V_{CC} = 5 V, Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	V_{CC} = 5 V, Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			2.5	
							−3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0, $V_{I(bus)}$ = 0 to 2.5 V				40	μA
I_{OS}	Short-circuit output current	Terminal	V_{CC} = 5.25 V		−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		V_{CC} = 5.25 V, No load	Terminal outputs low and enabled		42	56	mA
				Bus outputs low and enabled		52	85	
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
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switching characteristics at V_{CC} = 4.75 V, 5 V, and 5.25 V and C_L = 50 pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	TYP‡	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus	See Figure 1	25°C		10	17	ns
					Full range			20	
t_{PHL}	Propagation delay time, high- to low-level output				25°C		10	14	
					Full range			16	
t_{PLH}	Propagation delay time, low- to high-level output	Bus	Terminal	See Figure 2	25°C		8	15	ns
					Full range			18	
t_{PHL}	Propagation delay time, high- to low-level output				25°C		8	15	
					Full range			18	
t_{PZH}	Output enable time to high level	TE	Bus	See Figure 3	25°C		24	30	ns
					Full range			41	
t_{PHZ}	Output disable time from high level				25°C		9	14	
					Full range			16	
t_{PZL}	Output enable time to low level				25°C		16	28	
					Full range			34	
t_{PLZ}	Output disable time from low level				25°C		12	19	
					Full range			24	
t_{PZH}	Output enable time to high level	TE	Terminal	See Figure 4	25°C		24	36	ns
					Full range			50	
t_{PHZ}	Output disable time from high level				25°C		10	18	
					Full range			23	
t_{PZL}	Output enable time to low level				25°C		15	26	
					Full range			30	
t_{PLZ}	Output disable time from low level				25°C		15	24	
					Full range			31	
t_{en}	Output pullup enable time	PE	Bus	See Figure 5	25°C		16	24	ns
					Full range			25	
t_{dis}	Output pullup disable time				25°C		9	16	
					Full range			20	

†Full range is −55°C to 125°C.
‡All typical values are at V_{CC} = 5 V.

PARAMETER MEASUREMENT INFORMATION

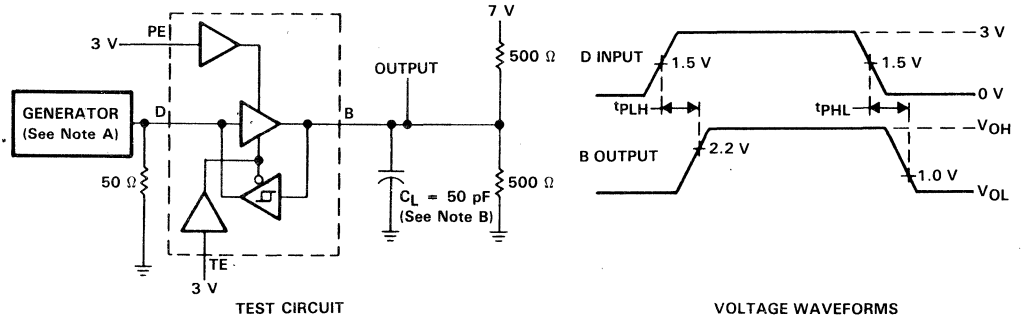


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

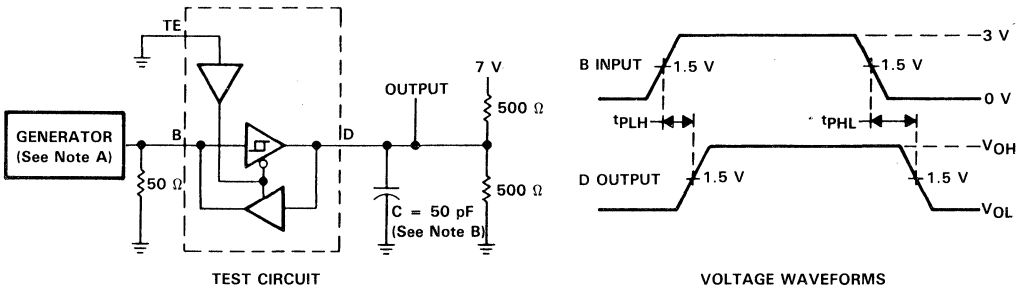


FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

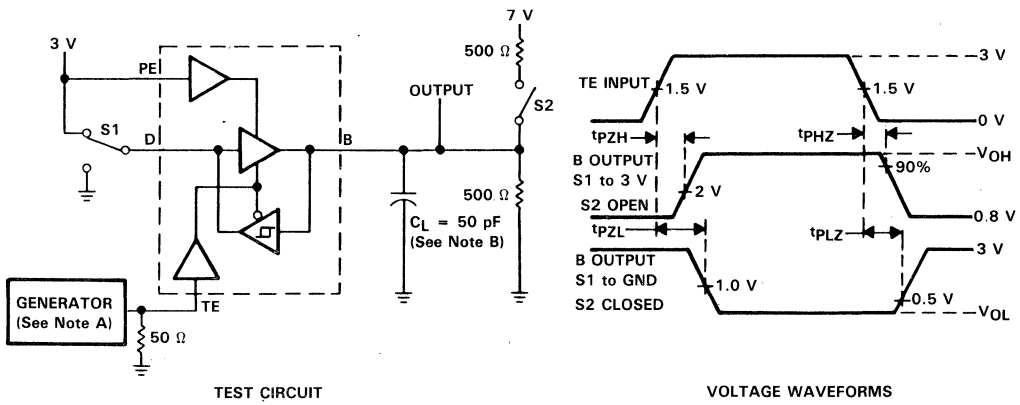
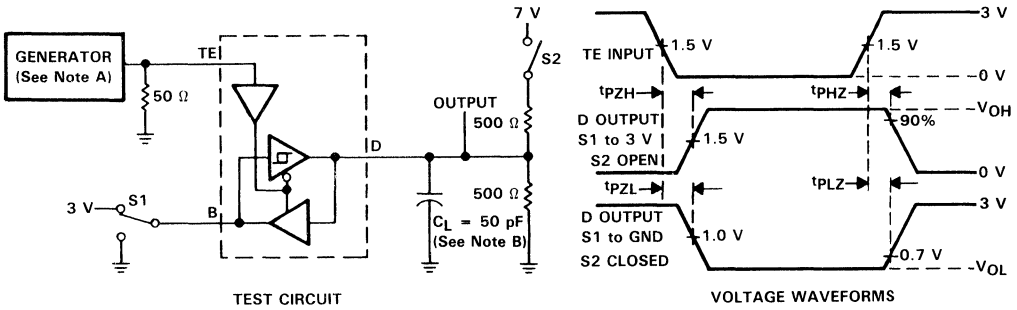


FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

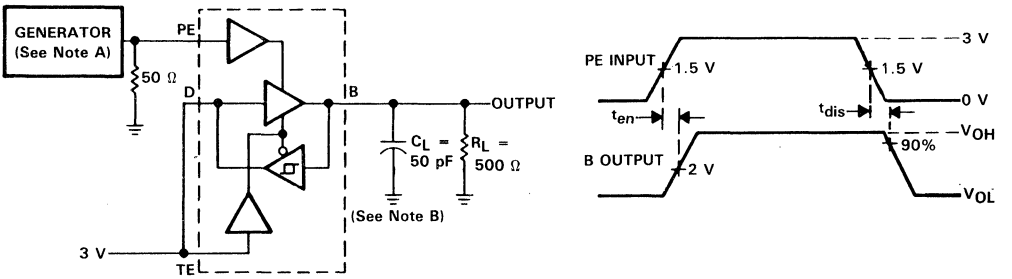
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

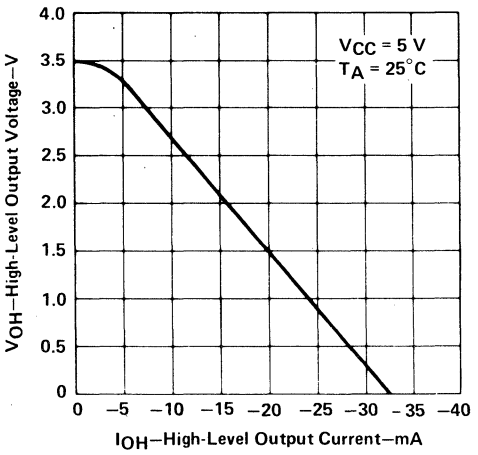


FIGURE 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

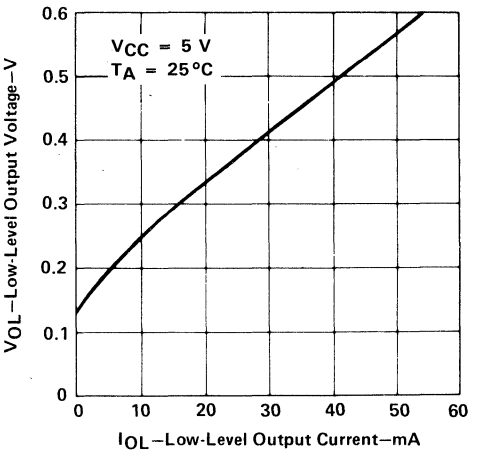


FIGURE 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

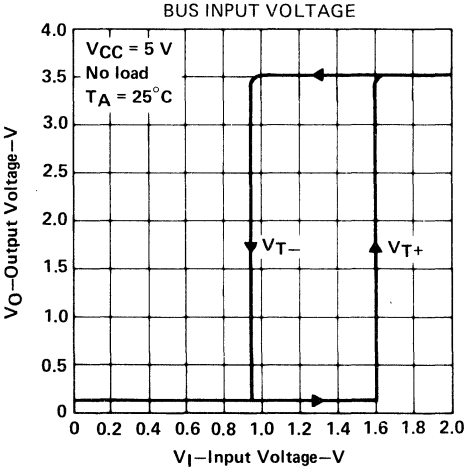


FIGURE 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

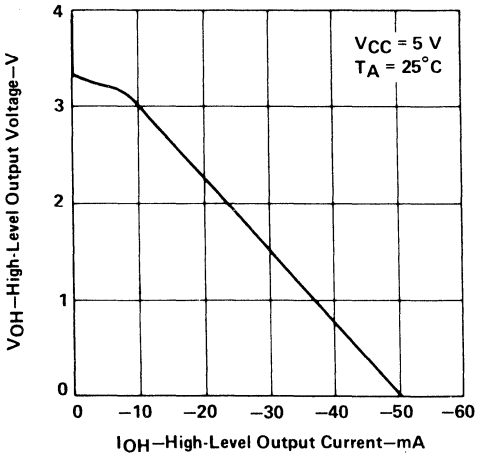


FIGURE 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

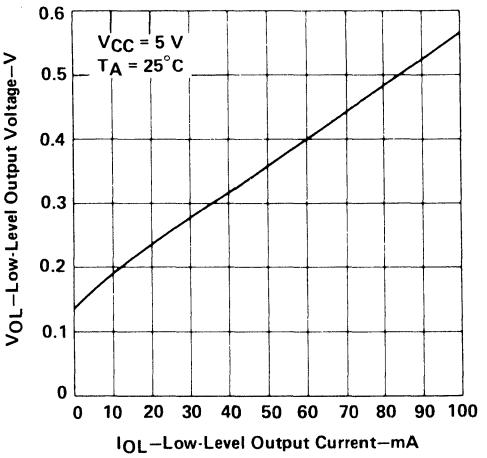


FIGURE 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

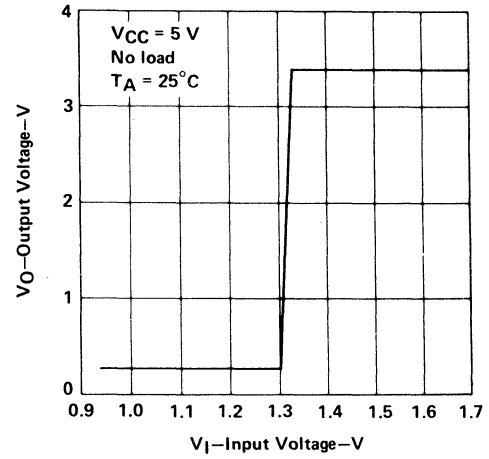


FIGURE 11

BUS CURRENT
vs
BUS VOLTAGE

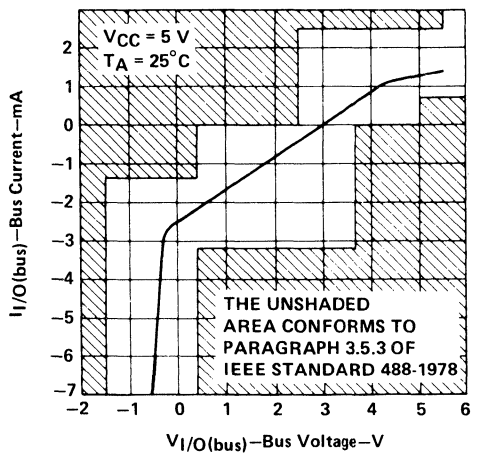


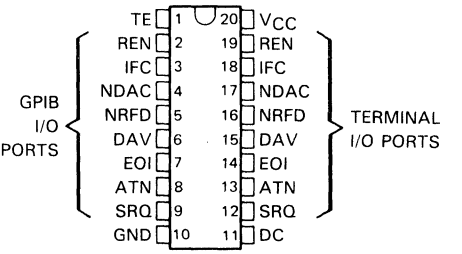
FIGURE 12

D3277, APRIL 1989

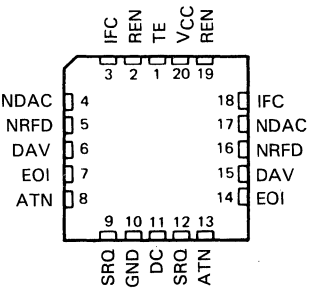
SUITABLE FOR IEEE STANDARD 488-1978 (GPIB) APPLICATIONS†

- 8-Channel Bidirectional Transceiver
- Designed to Implement Control Bus Interface
- Designed for Single Controller
- High-Speed Advanced Low Power Schottky Circuitry
- Low Power Dissipation . . . 59 mW Max per Channel
- Fast Propagation Times . . . 25 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 550 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

J OR W PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



description

The SN55ALS161 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky process device designed to provide the bus-management and data-transfer signals between operating units of a single controller instrumentation system. When combined with the SN55ALS160 octal bus transceiver, the SN55ALS161 provides the complete 16-wire interface for the IEEE 488 bus.†

The SN55ALS161 features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the DC and TE enable signals.

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when V_{CC} = 0. The drivers are designed to handle loads up to 48-mA sink current. Each receiver features p-n-p transistor inputs for high input impedance and a hysteresis of 250 mV minimum for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

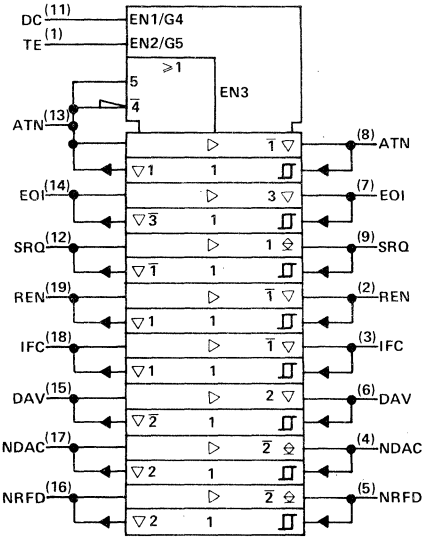
The SN55ALS161 is characterized for operation from −55°C to 125°C.

CHANNEL IDENTIFICATION TABLE

NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End or Identify	
DAV	Data Valid	Data Transfer
NDAC	Not Data Accepted	
NRFD	Not Ready for Data	

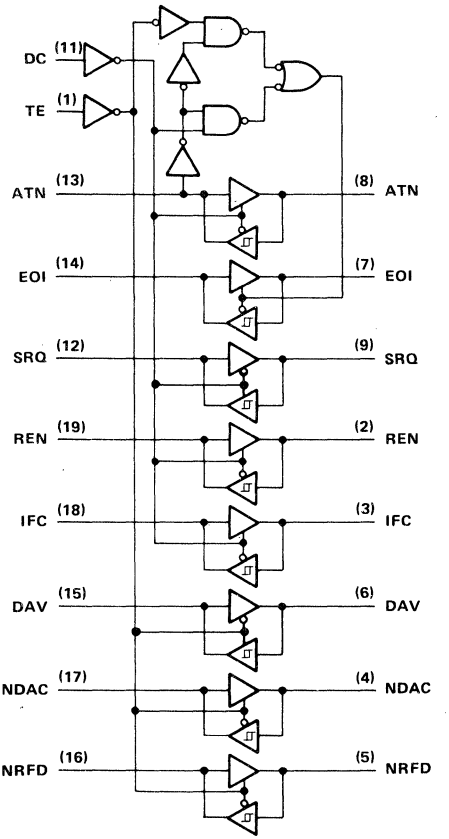
† The transceivers are suitable for IEEE Standard 488 applications to the extent of the operating conditions and characteristics specified in this data sheet. Certain limits contained in the IEEE specification are not met or cannot be tested over the entire military temperature range.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs.
⏀ Designates passive-pullup outputs.

logic diagram (positive logic)



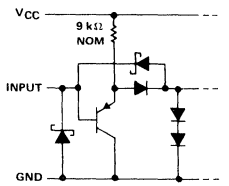
RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS			BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
			(Controlled by DC)					(Controlled by TE)		
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

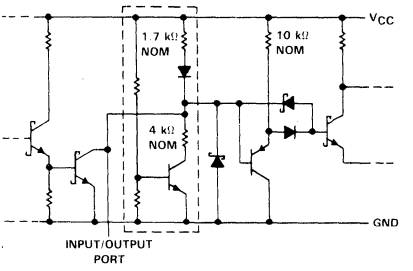
H = high level, L = low level, R = receive, T = transmit, X = irrelevant
Direction of data transmission is from the terminal side to the bus side, and the direction of data reception is from the bus side to the terminal side. Data transfer is noninverting in both directions.
†ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

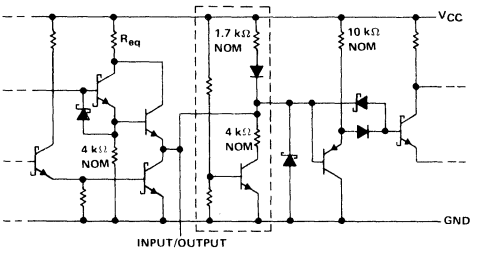


TYPICAL OF SRQ, NDAC, and NRFD GPIB I/O PORT



Circuit inside dashed lines is on the driver outputs only.

TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, and NRFD GPIB I/O PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Low-level driver output current	100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1375 mW
Operating free-air temperature range	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds	300°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate to 275 mW at 125°C at the rate of 11.0 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	TE and DC at T_A = −55°C to 125°C	2			V
	Bus and terminal at T_A = 25°C or 125°C	2			
	Bus and terminal at T_A = −55°C	2.1			
Low-level input voltage, V_{IL}	TE and DC at T_A = −55°C to 125°C			0.8	V
	Bus and terminal at T_A = 25°C or −55°C			0.8	
	Bus and terminal at T_A = 125°C			0.7	
High-level output current, I_{OH}	Bus ports with pullups active (V_{CC} = 5 V)			−5.2	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V, I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus	V_{CC} = 5 V, T_A = 25°C		0.4	0.55		V
			V_{CC} = 5 V, T_A = 125°C		0.25			
			V_{CC} = 5 V, T_A = −55°C		0.4			
V_{OH}‡	High-level output voltage	Terminal	V_{CC} = 4.75 V, I_{OH} = −800 μA		2.7	3.5		V
		Bus	V_{CC} = 5 V, I_{OH} = −5.2 mA		2.5	3.3		
			V_{CC} = 4.75 V, I_{OH} = −5.2 mA		2.2			
V_{OL}	Low-level output voltage	Terminal	V_{CC} = 4.75 V, I_{OL} = 16 mA			0.3	0.5	V
		Bus	V_{CC} = 4.75 V, I_{OL} = 48 mA, T_A = 25°C or 125°C			0.35	0.5	
			V_{CC} = 4.75 V, I_{IO} = 48 mA, T_A = −55°C			0.35	0.55	
I_I	Input current at maximum input voltage	Terminal	V_{CC} = 5.25 V, V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal and control inputs	V_{CC} = 5.25 V, V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current		V_{CC} = 5.25 V, V_I = 0.5 V			−30	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		V_{CC} = 5 V, Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	V_{CC} = 5 V, Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0	$V_{I(bus)}$ = 0 to 2.5 V			40	μA
I_{OS}‡	Short-circuit output current	Terminal	V_{CC} = 5.25 V		−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		V_{CC} = 5.25 V, No load, TE and DC low			55	90	mA
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{OH} and I_{OS} apply for three-state outputs only.

switching characteristics at V_{CC} = 4.75 V, 5 V, and 5.25 V and C_L = 50 pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	TYP‡	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus (Except SRQ, NDAC, and NRFD)	See Figure 1	25°C		10	17	ns
					Full range			20	
t_{PHL}	Propagation delay time, high- to low-level output				25°C		10	14	
					Full range			16	
t_{PLH}	Propagation delay time low- to high-level output	Terminal	Bus NRFD, SRQ, NDAC	See Figure 2	25°C			25	ns
					Full range			30	
t_{PHL}	Propagation delay time, high- to low-level output				25°C		10	14	
					Full range			16	
t_{PLH}	Propagation delay time, low- to high-level output	Bus	Terminal	See Figure 2	25°C		10	15	ns
					Full range			18	
t_{PHL}	Propagation delay time, high- to low-level output				25°C		10	15	
					Full range			18	
t_{PZH}	Output enable time to high level	TE or DC	Bus (ATN, REN, IFC, and DAV)	See Figure 3	25°C		20	30	ns
					Full range			41	
t_{PHZ}	Output disable time from high level				25°C		8	14	
					Full range			16	
t_{PZL}	Output enable time to low level				25°C		16	28	
					Full range			34	
t_{PLZ}	Output disable time from low level				25°C		10	19	
					Full range			24	
t_{PZH}	Output enable time to high level	TE or DC	Bus (EOI)	See Figure 3	25°C		24	30	ns
					Full range			48	
t_{PHZ}	Output disable time from high level				25°C		13	19	
					Full range			25	
t_{PZL}	Output enable time to low level				25°C		21	35	
					Full range			43	
t_{PLZ}	Output disable time from low level				25°C		13	20	
					Full range			27	
t_{PZH}	Output enable time to high level	TE or DC	Terminal	See Figure 4	25°C		24	36	ns
					Full range			50	
t_{PHZ}	Output disable time from high level				25°C		12	20	
					Full range			33	
t_{PZL}	Output enable time to low level				25°C		20	34	
					Full range			41	
t_{PLZ}	Output disable time from low level				25°C		13	24	
					Full range			35	

†Full range is −55°C to 125°C.
‡All typical values are at V_{CC} = 5 V.

PARAMETER MEASUREMENT INFORMATION

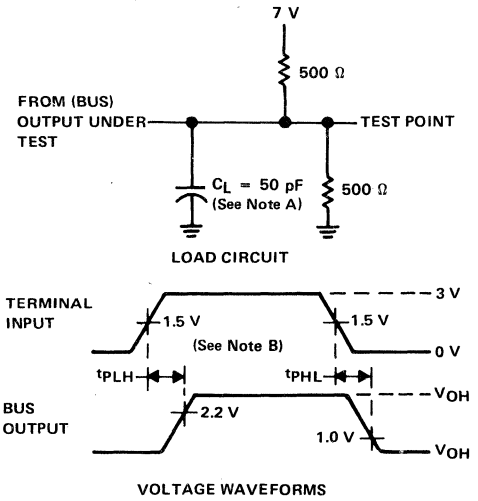


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

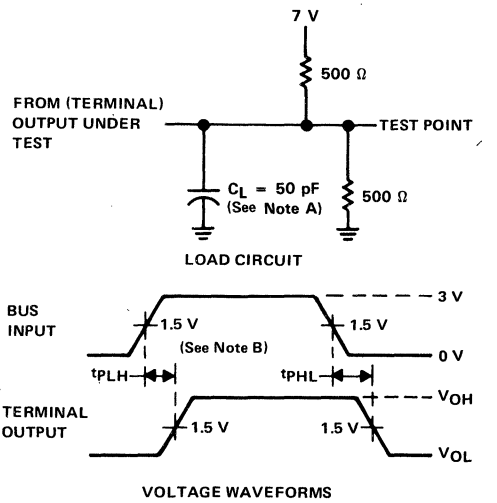
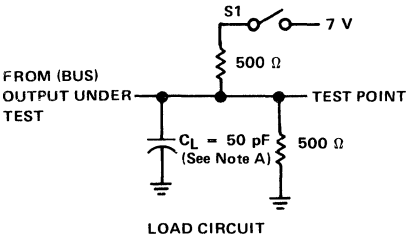


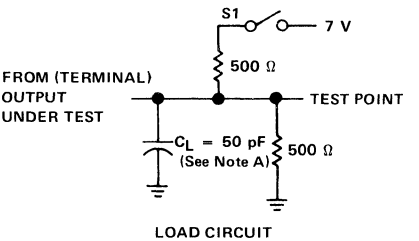
FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_O = 50 Ω.

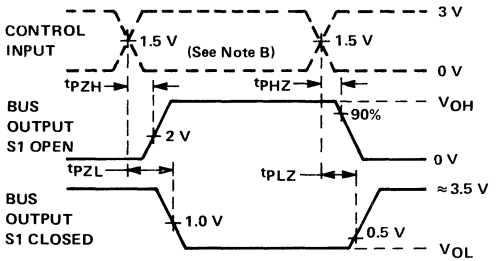
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

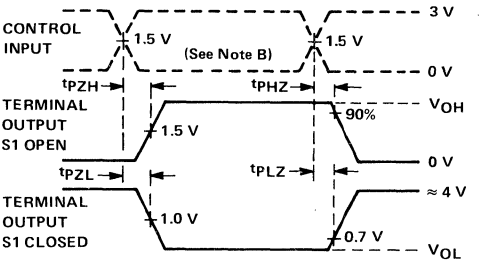


LOAD CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3. BUS ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS

FIGURE 4. TERMINAL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

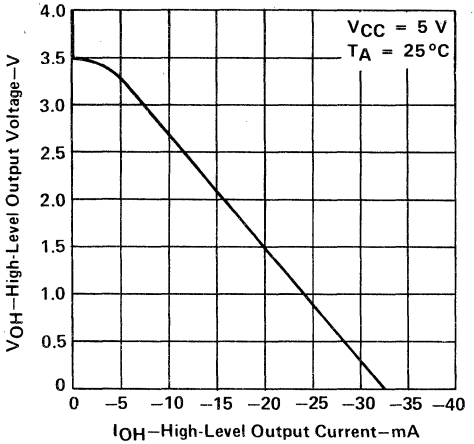


FIGURE 5

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

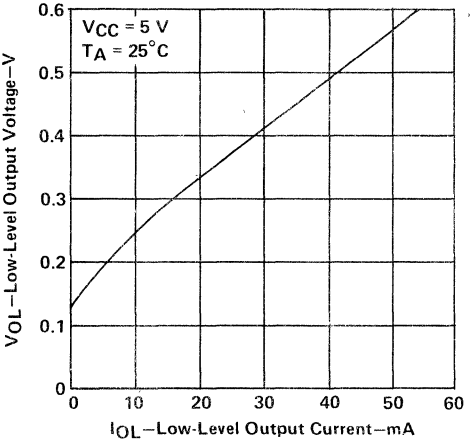


FIGURE 6

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

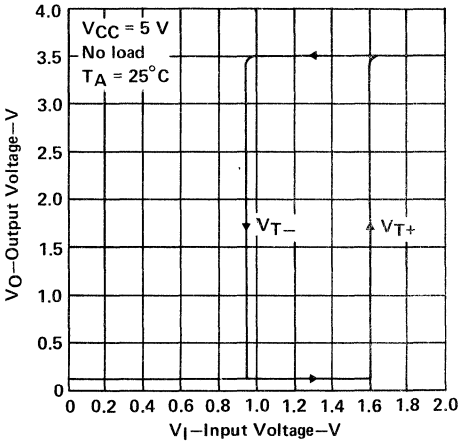


FIGURE 7

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

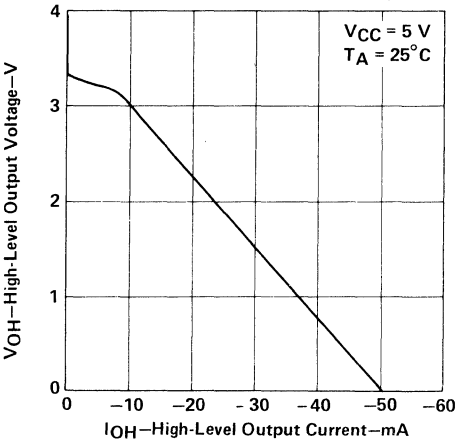


FIGURE 8

BUS-LOW LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

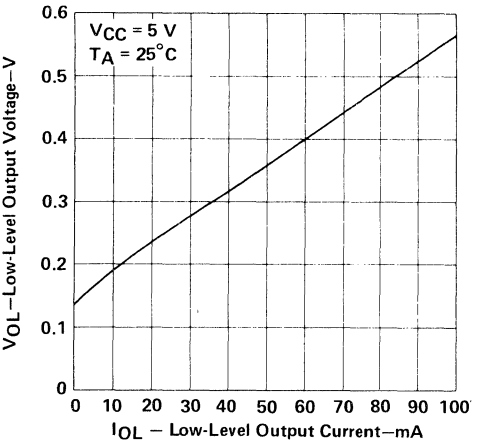


FIGURE 9

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

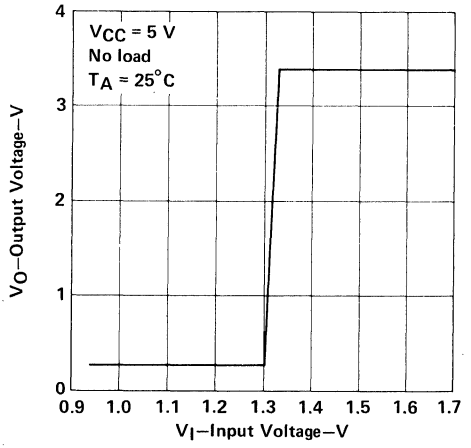


FIGURE 10

BUS CURRENT
vs
BUS VOLTAGE

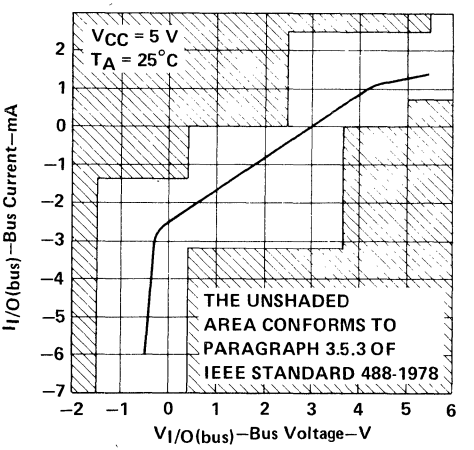
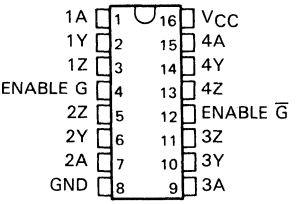


FIGURE 11

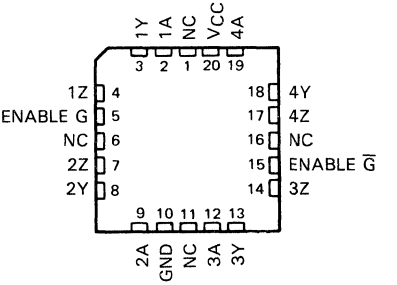
D2904, JULY 1985—REVISED JUNE 1986

- **Meets EIA Standard RS-422-A**
- **High-Speed, Low-Power ALS Design**
- **3-State TTL Compatible**
- **Single 5-V Supply Operation**
- **High Output Impedance in Power-Off Condition**
- **Complementary Output Enable Inputs**
- **Improved Replacement for the AM26LS31**

SN55ALS192 . . . J PACKAGE
SN75ALS192 . . . D, J, OR N PACKAGE
(TOP VIEW)



SN55ASL192 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These quadruple complementary-output line drivers are designed for data transmission over twisted-pair or parallel-wire transmission lines. They meet the requirements of EIA Standard RS-422-A and are compatible with 3-state TTL circuits. Advanced Low-Power Schottky technology provides high speed without the usual power penalties. Standby supply current is typically only 26 mA, while typical propagation delay time is less than 10 ns.

High-impedance inputs maintain input currents low, less than 1 μA for a high level and less than 100 μA for a low level. Complementary control inputs, G and $\overline{G}$, allow these devices to be enabled at either a high input level or low input level. The SN75ALS192 is capable of data rates in excess of 20 megabits per second and is designed to operate with the SN75ALS193 quadruple line receiver. The SN55ALS192 is also capable of data rates in excess of 20 megabits per second and designed to operate with the SN55ALS193; however, it may be limited to a lower bit rate based on the temperature. Reference should be made to the Dissipation Rating Table and Figure 15.

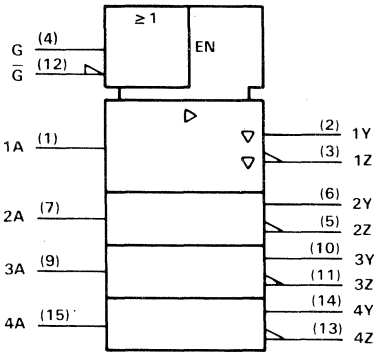
The SN55ALS192 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75ALS192 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH DRIVER)

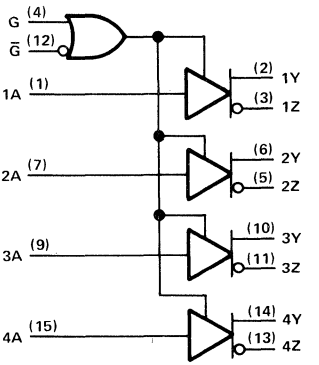
INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level,
Z = high impedance (off),
X = irrelevant

logic symbol†

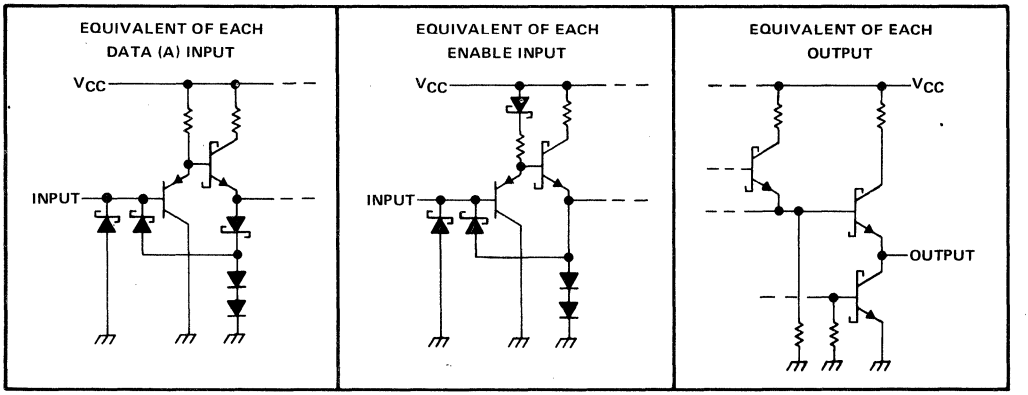


logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55ALS192	SN75ALS192	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage, V_I		7	7	V
Output off-state voltage		6	6	V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	D package		950	mW
	FK package	1375		
	J package	1375	1025	
	N package		1150	
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package	300	300	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package		260	°C

NOTES: 1. All voltage values except differential output voltage V_{OD} are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to the Dissipation Rating Table. In the J package, SN55ALS192 chips are either alloy or silver glass mounted and SN75ALS192 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	275 mW
FK or J (SN55ALS912)	1375 mW	11.0 mW/°C	880 mW	
J (SN75ALS192)	1025 mW	8.2 mW/°C	656 mW	
N	1150 mW	9.2 mW/°C	736 mW	

recommended operating conditions

	SN55ALS192			SN75ALS192			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−20			−20	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN55ALS192			SN75ALS192			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −20 mA		2.4			2.5			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20 mA				0.5			0.5	V
V_O	Output voltage	V_{CC} = MAX, I_O = 0		0		6	0		6	V
$\lvert V_{OD1}\rvert$	Differential output voltage	V_{CC} = MIN, I_O = 0		1.5		6	1.5		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω, See Figure 1		½ V_{OD1}			½ V_{OD1}			V
				2			2			
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage§	R_L = 100 Ω, See Figure 1				±0.2			±0.2	V
V_{OC}	Common-mode output voltage¶					±3			±3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage§					±0.2			±0.2	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			100			100	μA
			V_O = −0.25 V			−100			−100	
I_{OZ}	Off-state (high-impedance state) output current	V_{CC} = MAX	V_O = 0.5 V			−20			−20	μA
			V_O = 2.5 V			20			20	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.2			−0.2	mA
I_{OS}	Short-circuit output current#	V_{CC} = MAX		−30		−150	−30		−150	mA
I_{CC}	Supply current (all drivers)	V_{CC} = MAX, All outputs disabled			26	45		26	45	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
‡All typical values are at V_{CC} = 5 V and T_A = 25°C.
§$\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
#Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, S1 and S2 open		6	13	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	14	ns
	Output-to-output skew			3	6	ns
t_{PZH}	Output enable time to high level	R_L = 75 Ω		11	15	ns
t_{PZL}	Output enable time to low level	R_L = 180 Ω		16	20	ns
t_{PHZ}	Output disable time from high level	C_L = 10 pF, S1 and S2 closed		8	15	ns
t_{PLZ}	Output disable time from low level			18	20	ns

PARAMETER MEASUREMENT INFORMATION

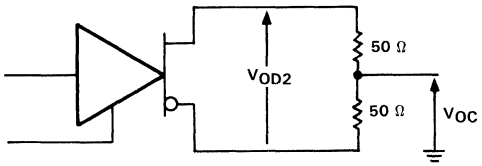
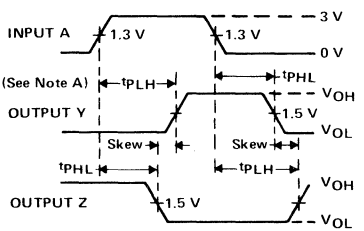
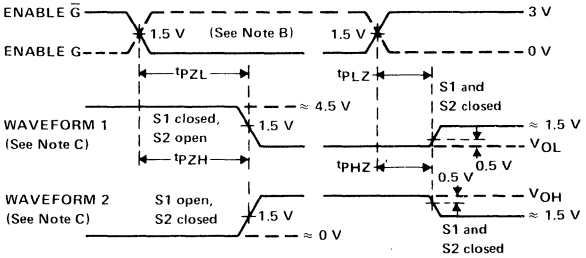


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES

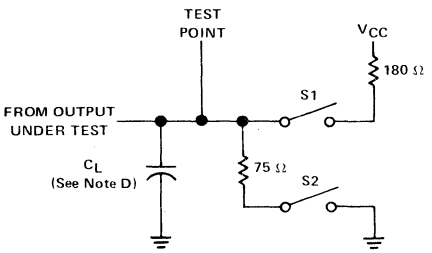


PROPAGATION DELAY TIMES AND SKEW



ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS



TEST CIRCUIT

NOTES: A. When measuring propagation delay times and skew, switches S1 and S2 are open.
B. Each enable is tested separately.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. C_L includes probe and jig capacitance.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω, t_r ≤ 15 ns, and t_f ≤ 6 ns.

FIGURE 2. SWITCHING TIMES

TYPICAL CHARACTERISTICS

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

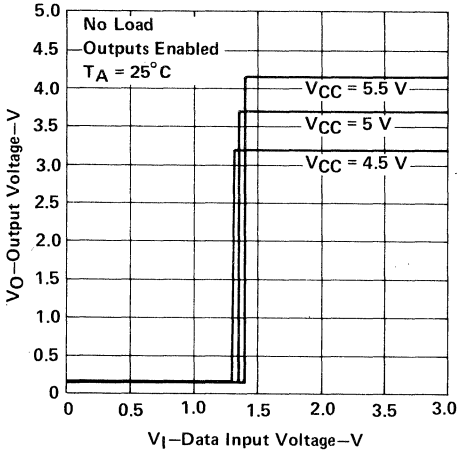


FIGURE 3

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

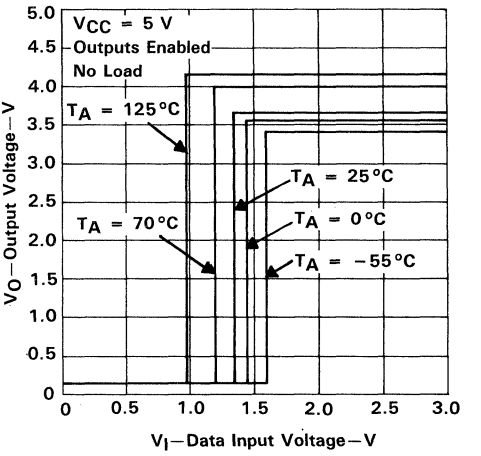


FIGURE 4

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

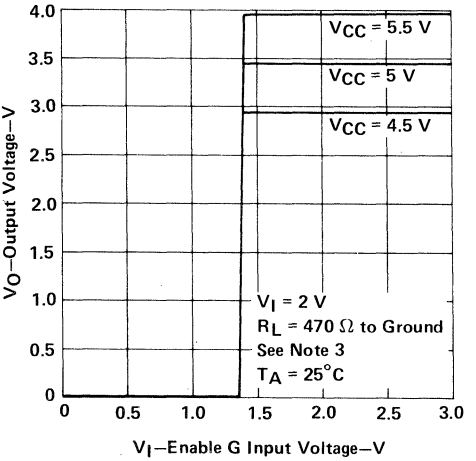


FIGURE 5

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

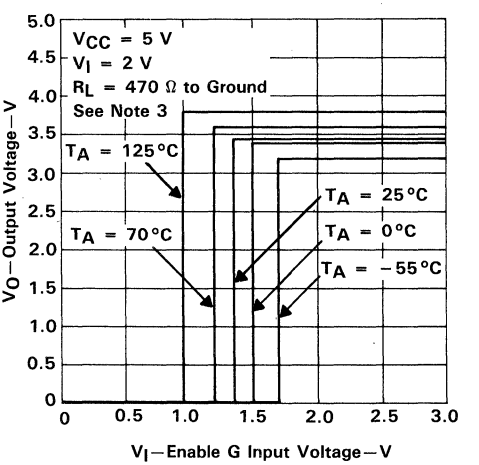


FIGURE 6

NOTE 3: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

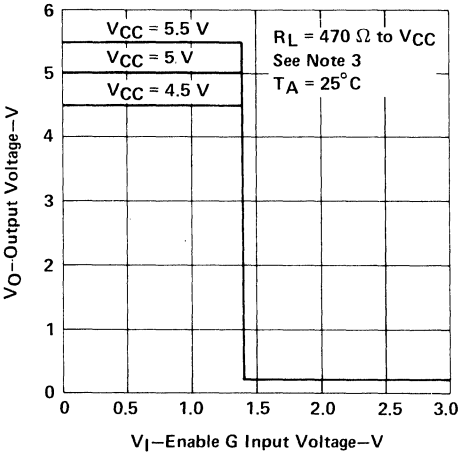


FIGURE 7

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

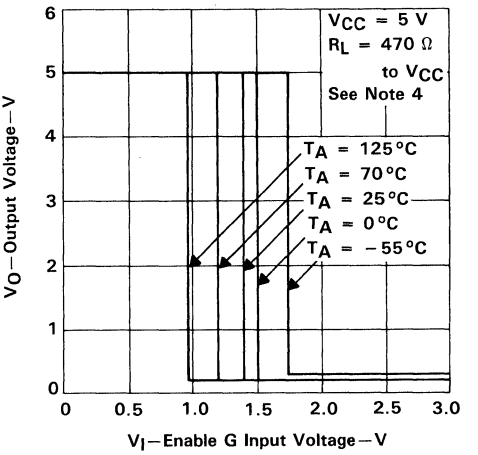


FIGURE 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

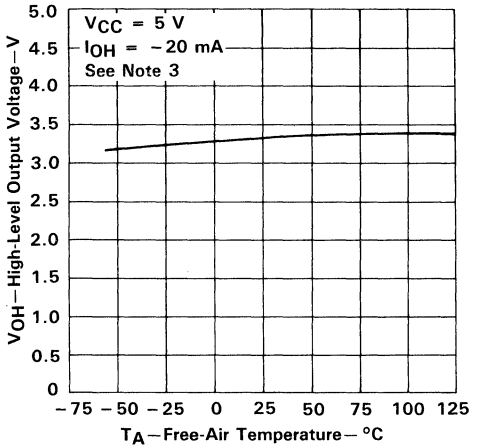


FIGURE 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

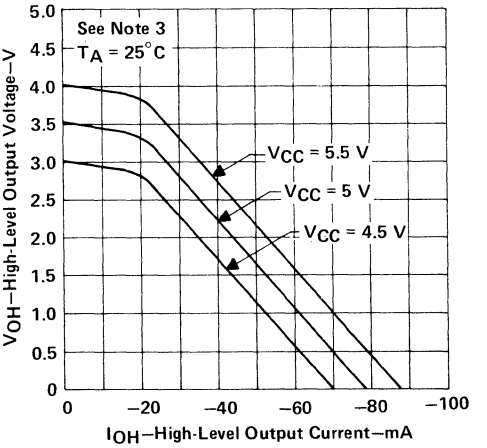


FIGURE 10

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.
4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

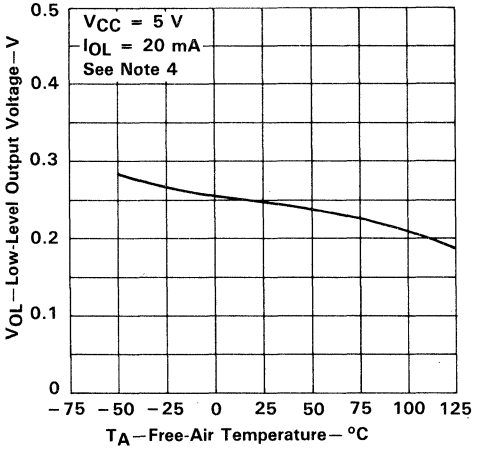


FIGURE 11

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

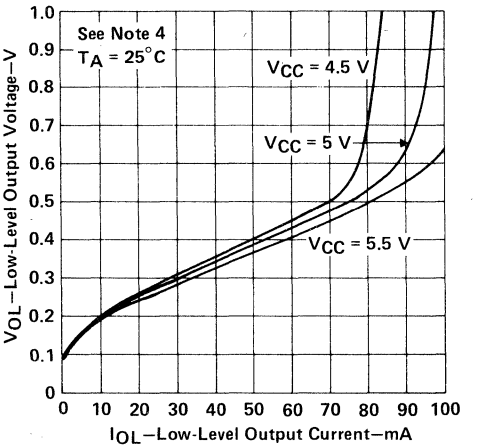


FIGURE 12

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

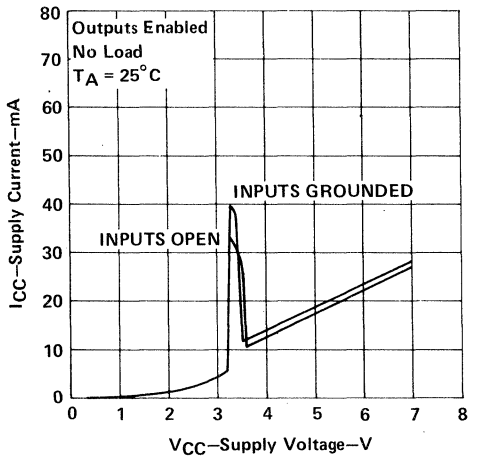


FIGURE 13

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

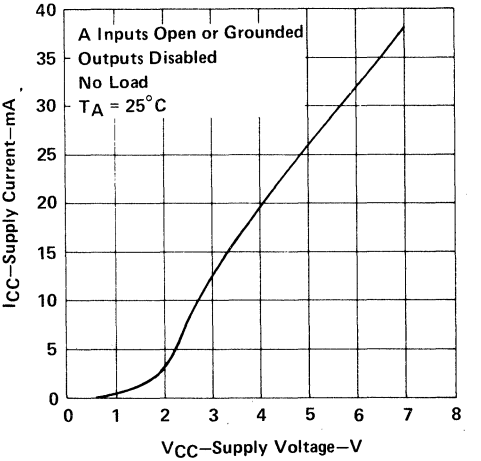


FIGURE 14

NOTE 4: The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREQUENCY

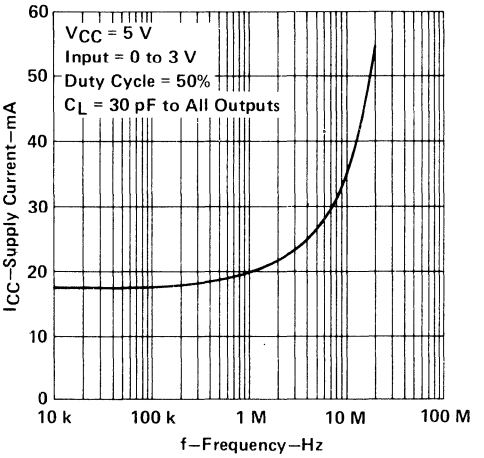
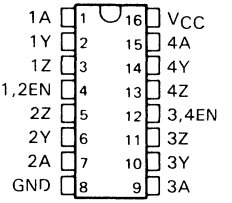


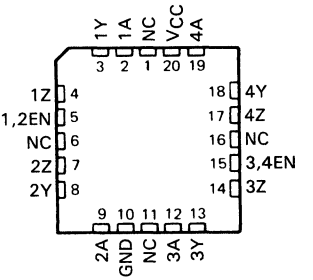
FIGURE 15

- Meets EIA Standard RS-422-A
- High-Speed ALS Design
- 3-State TTL-Compatible
- Single 5-V Supply Operation
- High Output Impedance in Power-Off Condition
- Two Pairs of Drivers Independently Enabled
- Designed as a Replacement for the MC3487 with Improvements: I_{CC} 50% Lower, Switching Speed 30% Faster, Full-Temperature-Range Version

SN55ALS194 . . . J PACKAGE
SN75ALS194 . . . D, J, OR N PACKAGE
(TOP VIEW)



SN55ALS194 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These quadruple complementary-output line drivers are designed for data transmission over twisted-pair or parallel-wire transmission lines. They meet the requirements of EIA Standard RS-422-A and are compatible with 3-state TTL circuits. Advanced Low-Power Schottky technology provides high speed without the usual power penalty. Standby supply current is typically only 26 mA, while typical propagation delay time is less than 10 ns and enable/disable times are typically less than 16 ns.

High-impedance inputs keep input currents low, less than 1 μA for a high level and less than 100 μA for a low level. The driver circuits can be enabled in pairs by separate active-high enable inputs. The SN55ALS194 and SN75ALS194 are capable of data rates in excess of 10 megabits per second and are designed to operate with the SN55ALS195 and SN75ALS195 quadruple line receivers.

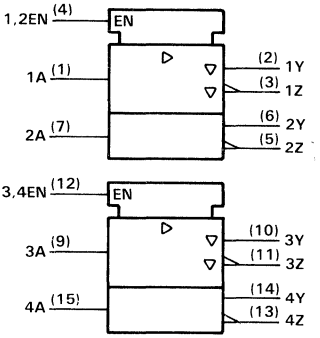
The SN55ALS194 is characterized for operation from −55°C to 125°C. The SN75ALS194 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH DRIVER)

INPUT	OUTPUT ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	High-Impedance	High-Impedance

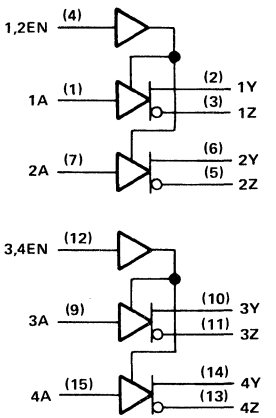
H = TTL high level, L = TTL low level, X = irrelevant

logic symbol†

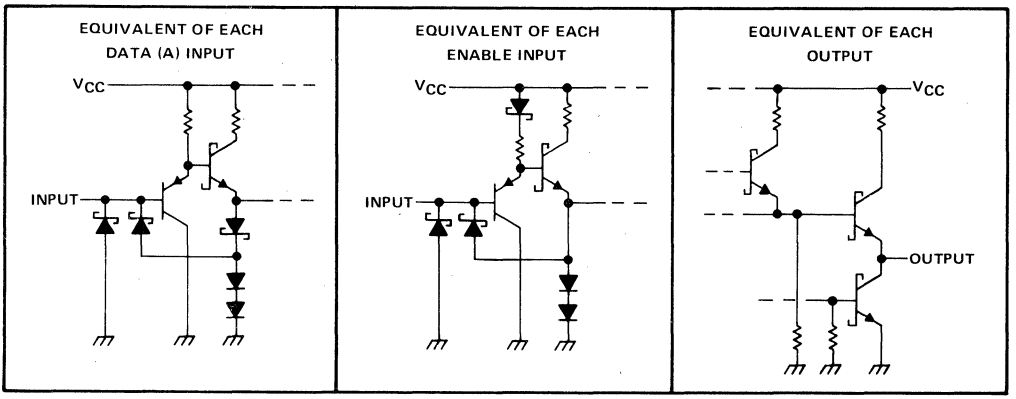


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN55ALS194 . . . . . −55°C to 125°C
SN75ALS194 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55ALS194)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75ALS194)	1025 mW	8.2 mW/°C	656 mW	N/A
N	1150 mW	9.2 mW/°C	736 mW	N/A

recommended operating conditions

		SN55ALS194			SN75ALS194			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	All inputs, T_A = 25°C	2			2			V
	A inputs, T_A = Full range	2			2			
	EN inputs, T_A = Full range	2.1			2			
Low-level input voltage, V_{IL}				0.8			0.8	V
High-level output current, I_{OH}				−20			−20	mA
Low-level output current, I_{OL}	T_A = 25°C			48			48	mA
	T_A = Full range			20			48	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −20 mA		SN55ALS194	2.4			V
				SN75ALS194	2.5			
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = MAX				0.5	V
VO	Output voltage	I_O = 0			0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0			2		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1			½ V_{OD1}			V
					2			
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡						±0.4	V
V_{OC}	Common-mode output voltage						±3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡						±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V				100	μA
			V_O = −0.25 V				−100	
I_{OZ}	High-impedance state output current	V_{CC} = MAX, Output enables at 0.8 V	V_O = 2.7 V				100	μA
			V_O = 0.5 V				−100	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V				−200	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX,	V_I = 2 V		−40		−140	mA
I_{CC}	Supply current (all drivers)	V_{CC} = MAX,	All outputs disabled			26	45	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55ALS194			SN75ALS194			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 2		6	13		6	13	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	14		9	14	ns
	Output-to-output skew			3.5	6		3.5	6	ns
t_{TD}	Differential-output transition time	C_L = 15 pF, See Figure 3		8	14		8	14	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 4		9	12		9	12	ns
t_{PZL}	Output enable time to low level			12	20		12	20	ns
t_{PHZ}	Output disable time from high level			9	15		9	14	ns
t_{PLZ}	Output disable time from low level			12	15		12	15	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A
V_O	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$

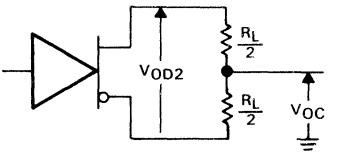


FIGURE 1. DRIVER V_{OD} AND V_{OC}

PARAMETER MEASUREMENT INFORMATION

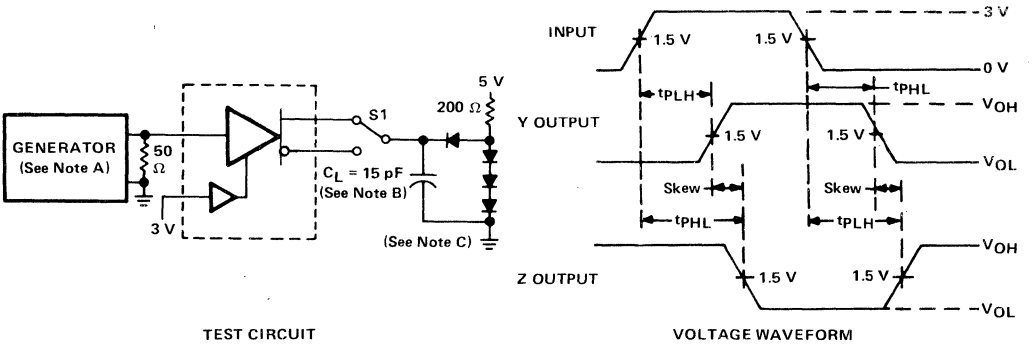


FIGURE 2. PROPAGATION DELAY TIMES

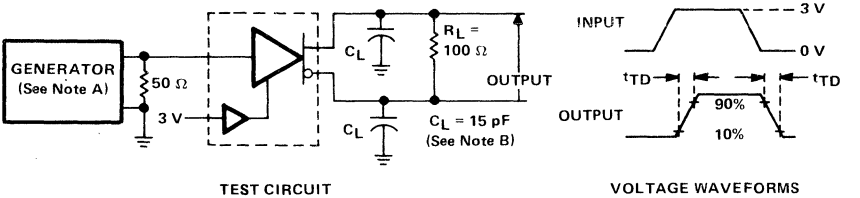
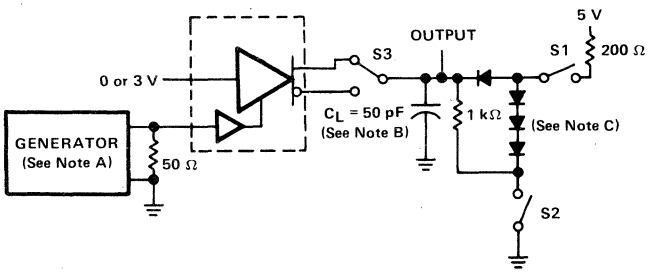


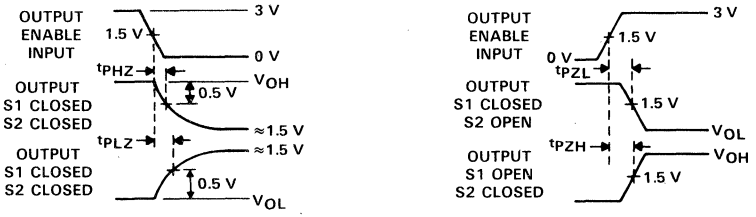
FIGURE 3. DIFFERENTIAL-OUTPUT TRANSITION TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_O \approx 50$ Ω.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_o \approx 50\ \Omega$.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

TYPICAL CHARACTERISTICS†

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

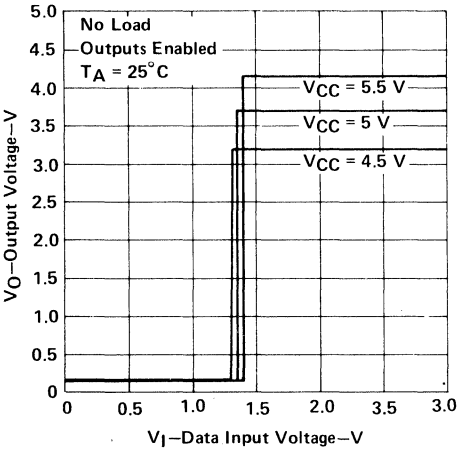


FIGURE 5

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

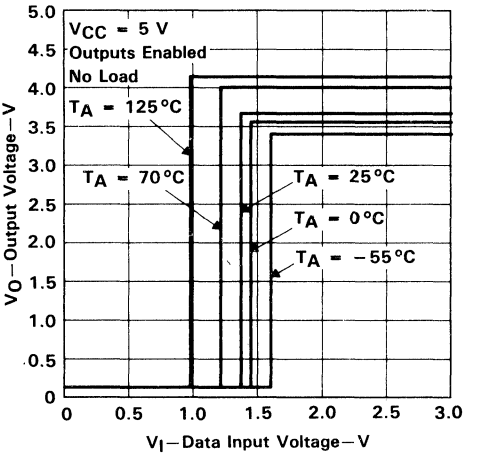


FIGURE 6

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

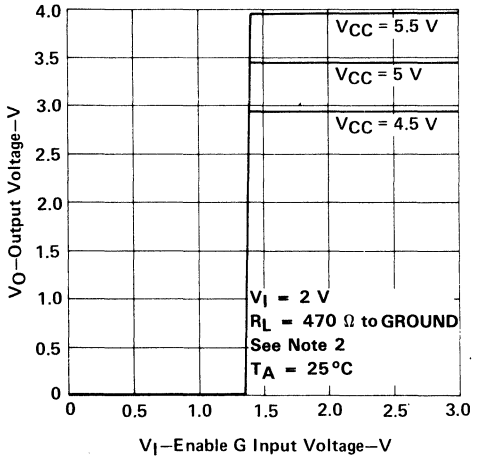


FIGURE 7

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

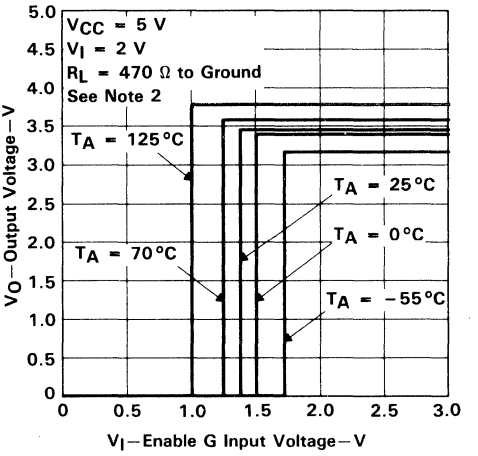


FIGURE 8

†Data for temperatures below 0°C and above 70°C are applicable to SN55ALS194 circuits only.
NOTE 2: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

TYPICAL CHARACTERISTICS†

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

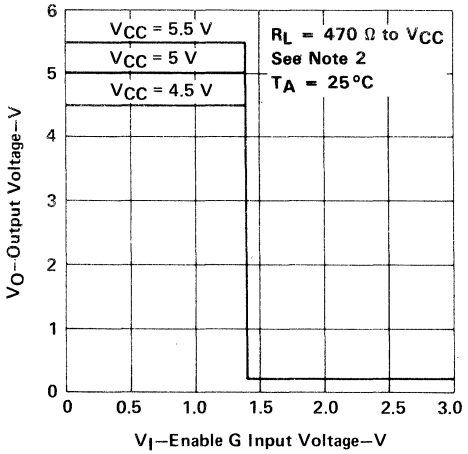


FIGURE 9

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

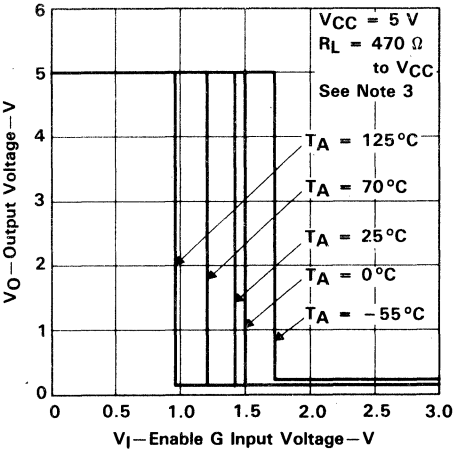


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

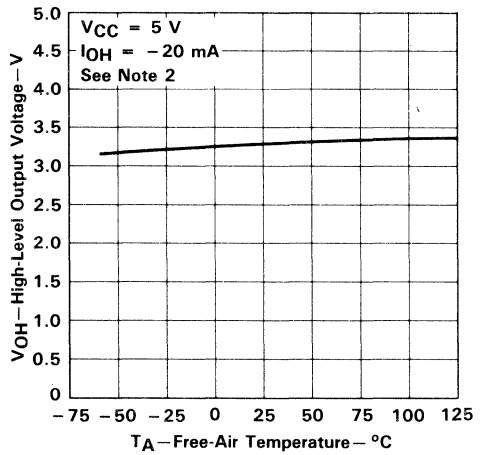


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

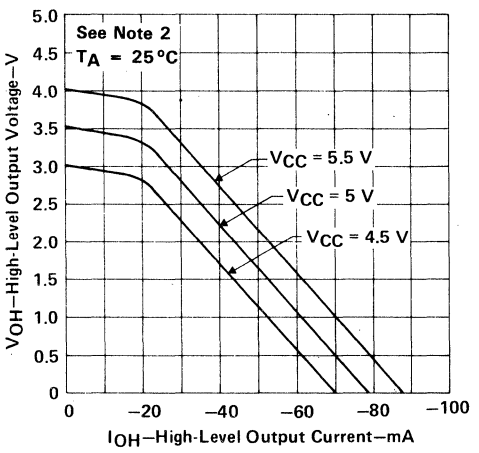


FIGURE 12

†Data for temperatures below 0°C and above 70°C are applicable to the SN55ALS194 circuits only.

NOTES: 2. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.
3. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

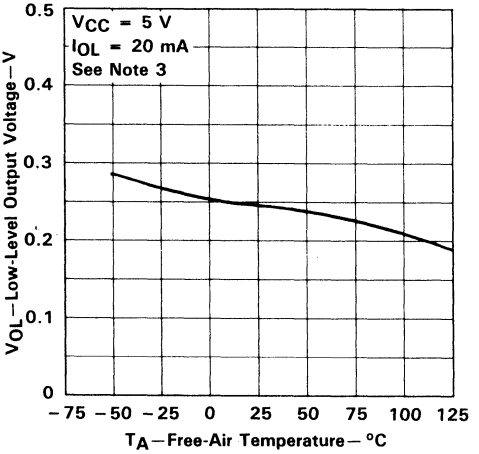


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

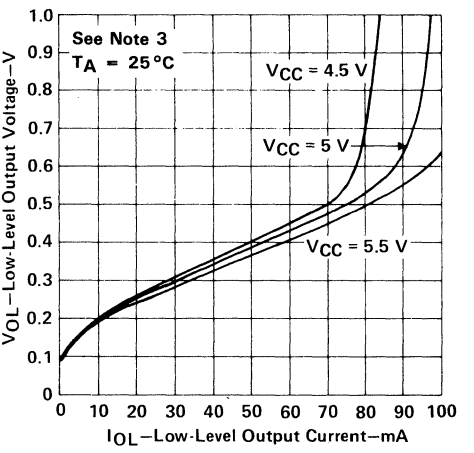


FIGURE 14

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

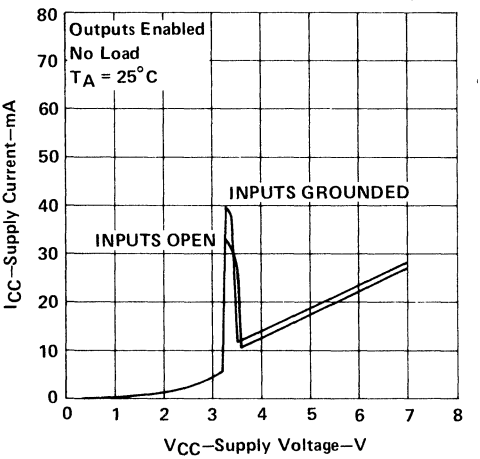


FIGURE 15

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

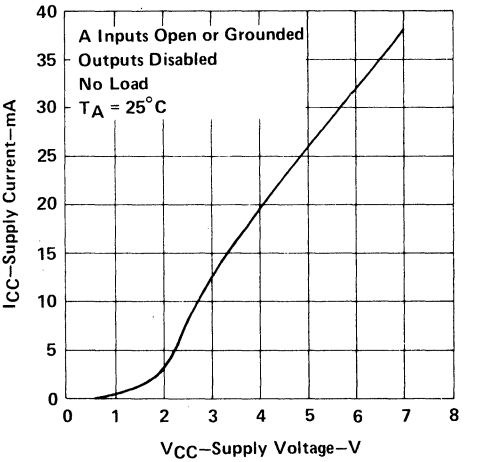


FIGURE 16

† Data for temperatures below 0°C and above 70°C are applicable to the SN55ALS194 circuits only.
NOTE 3: The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREQUENCY

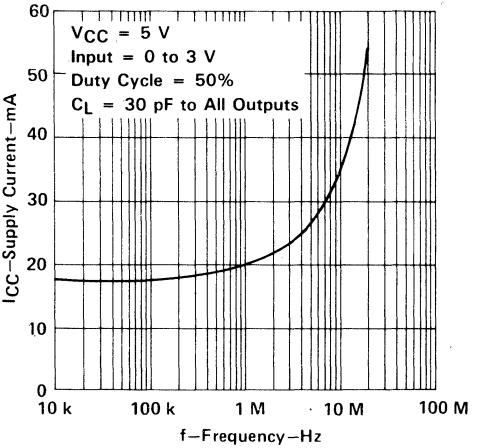
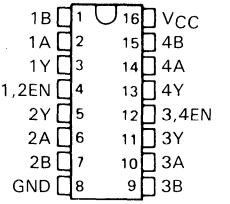


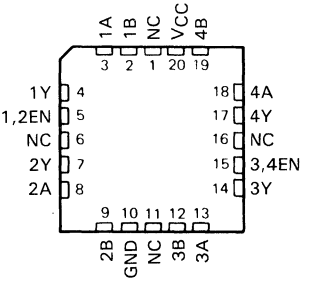
FIGURE 17

- Meets EIA Standards RS-422-A and RS-423-A
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- −7 V to 7 V Common-Mode Range With 200-mV Sensitivity
- 3-State TTL-Compatible Outputs
- High Input Impedance . . . 12 kΩ Min
- Input Hysteresis . . . 120 mV Typ
- Single 5-V Supply Operation
- Low Supply Current Requirement . . . 35 mA Max
- Improved Speed and Power Consumption Compared to MC3486

SN55ALS195, SN75ALS195 . . . J PACKAGE
(TOP VIEW)



SN55ALS195 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

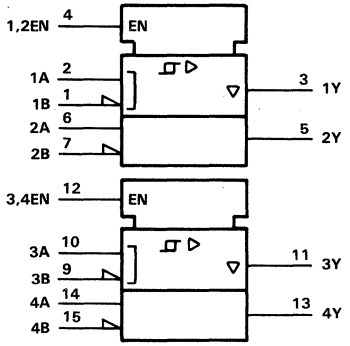
description

The SN55ALS195 and SN75ALS195 are monolithic quadruple line receivers with 3-state outputs designed using Advanced Low-Power Schottky technology. This technology provides combined improvements in die design, tooling production, and wafer fabrication, which in turn, provide lower power consumption and permit much higher data throughput than other designs. The devices meet the specifications of EIA Standards RS-422-A and RS-423-A. The 3-state outputs permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open.

The devices are optimized for balanced multipoint bus transmission at rates up to 20M b/s. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ±200 mV over a common-mode input voltage range of ±7 V. The devices also feature an active-high enable function for each of two receiver pairs. The SN55ALS195 and SN75ALS195 are designed for optimum performance when used with the SN55ALS194 and SN75ALS194 quadruple differential line drivers.

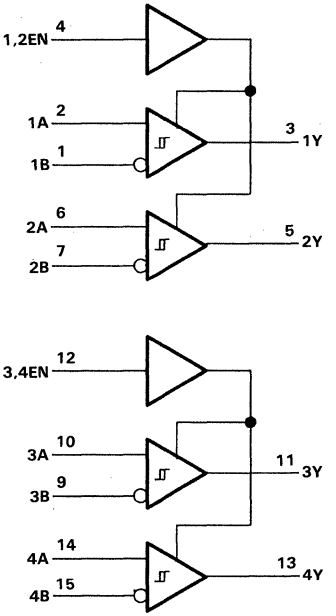
The SN55ALS195 is characterized for operation from −55°C to 125°C. The SN75ALS195 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J package.

logic diagram

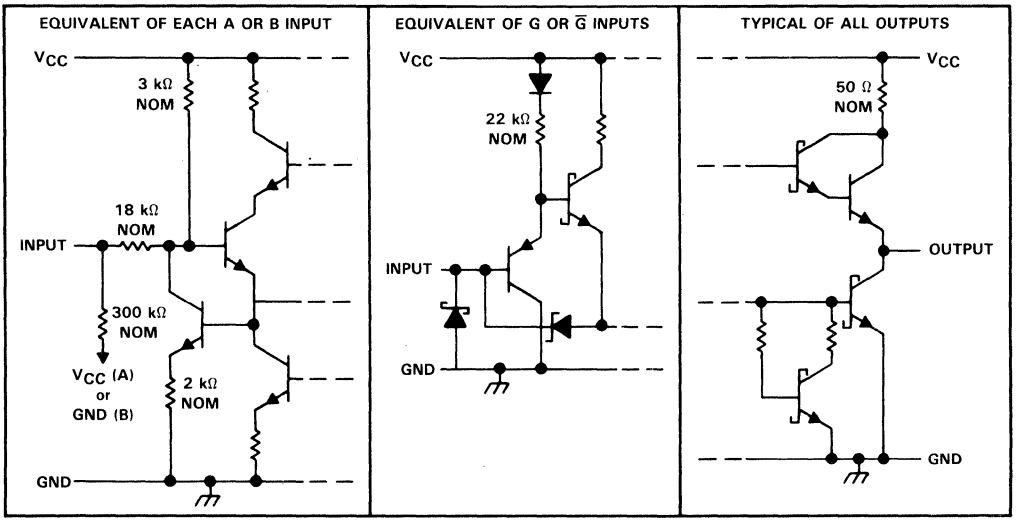


FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUTS A–B	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z

H = high level, L = low level, X = irrelevant,
? = indeterminate, and Z = high impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, A or B inputs, V_I . . . . . ±15 V
Differential input voltage (see Note 2) . . . . . ±15 V
Enable input voltage . . . . . 7 V
Low-level output current . . . . . 50 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN55ALS195 . . . . . −55°C to 125°C
SN75ALS195 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditons" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55ALS195)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75ALS195)	1025 mW	8.2 mW/°C	656 mW	N/A

recommended operating conditions

	SN55ALS195			SN75ALS195			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7			±7	V
Differential input voltage, V_{ID}			±12			±12	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{T+}	Positive-going threshold voltage					200	mV
V_{T-}	Negative-going threshold voltage			−200§			mV
V_{hys}	Hysteresis¶				120		mV
V_{IK}	Enable-input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} MIN, I_{OH} = −400 μA,	V_{ID} = 200 mV, See Figure 1	2.5	3.6		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{ID} = −200 mV, See Figure 1	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance state output current	V_{CC} = MAX, V_{ID} = −3 V,	V_{IL} = 0.8 V, V_O = 2.7 V			20	μA
		V_{CC} = MAX, V_{IO} = 3 V,	V_{IL} = 0.8 V, V_O = 0.5 V			−20	
I_I	Line input current	Other input at 0 V, See Note 3	V_{CC} = MIN, V_I = 15 V		0.7	1.2	mA
			V_{CC} = MAX, V_I = −15 V		−1.0	−1.7	
I_{IH}	High-level enable-input current	V_{CC} = MAX	V_{IH} = 2.7 V			20	μA
			V_{IH} = 5.25 V			100	
I_{IL}	Low-level enable-input current	V_{CC} = MAX,	V_{IL} = 0.4 V			−100	μA
	Input resistance			12	18		kΩ
I_{OS}	Short-circuit output current	V_{CC} = MAX, V_O = 0,	V_{ID} = 3 V, See Note 4	−15	−78	−130	mA
I_{CC}	Supply current	V_{CC} = MAX,	Outputs disabled		22	35	mA

†For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
¶Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.
NOTES: 3. Refer to EIA Standard RS-422-A and RS-423-A for exact conditions.
4. Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = 0 V to 3 V, C_L = 15 pF, See Figure 2		15	22	ns
t_{PHL}	Propagation delay time, high- to low-level output			15	22	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 3		13	25	ns
t_{PZL}	Output enable time to low level			10	25	
t_{PHZ}	Output disable time from high level	C_L = 15 pF, See Figure 3		19	25	ns
t_{PLZ}	Output disable time from low level			17	22	

PARAMETER MEASUREMENT INFORMATION

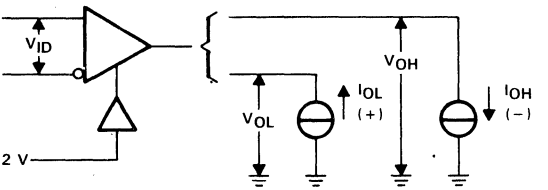
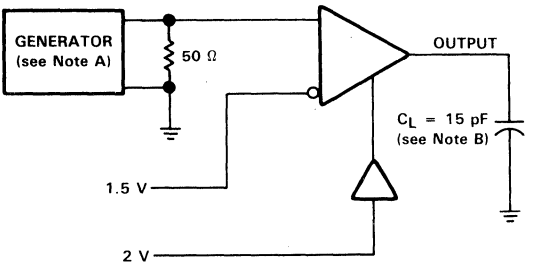
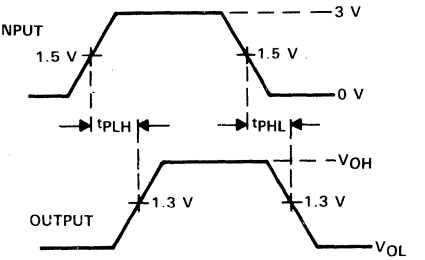


FIGURE 1. V_{OH}, V_{OL}



TEST CIRCUIT

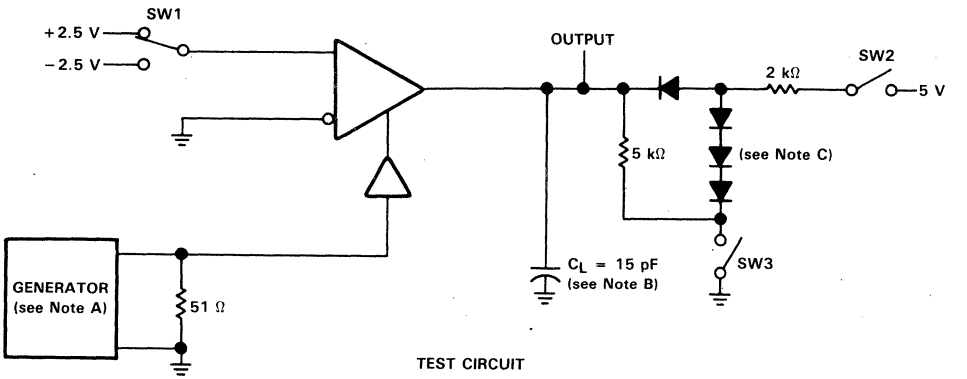


VOLTAGE WAVEFORMS

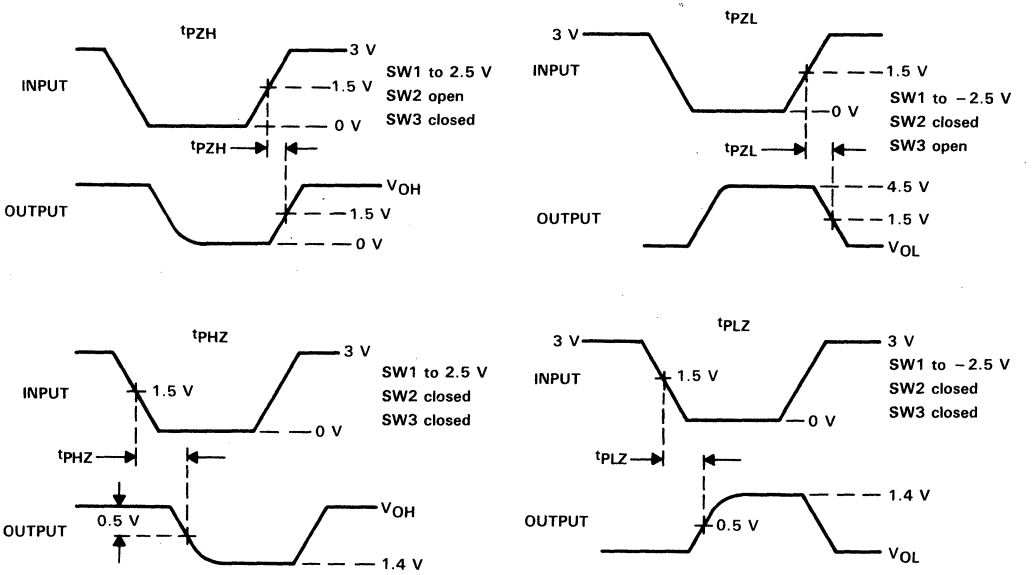
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_{out} = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

FIGURE 2. PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_{out} = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

FIGURE 3. ENABLE AND DISABLE TIMES

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

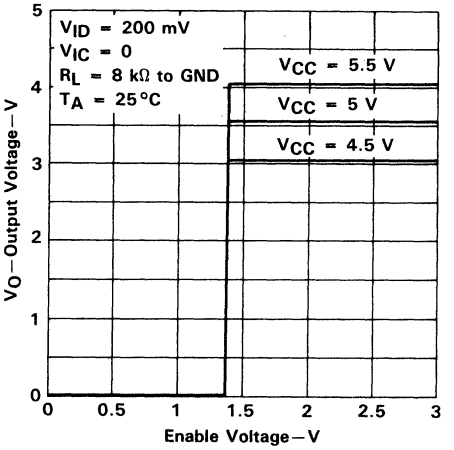


FIGURE 4

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

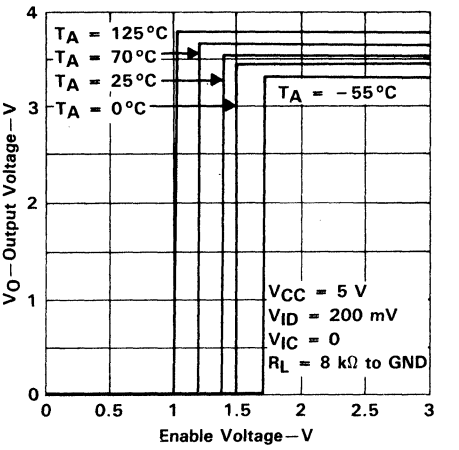


FIGURE 5

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

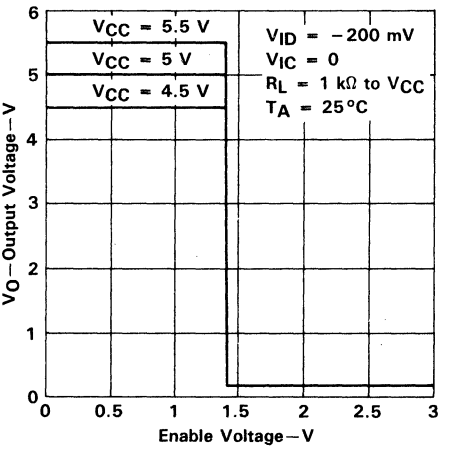


FIGURE 6

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

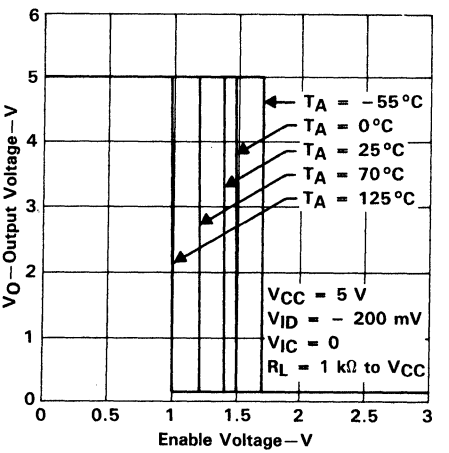


FIGURE 7

†Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

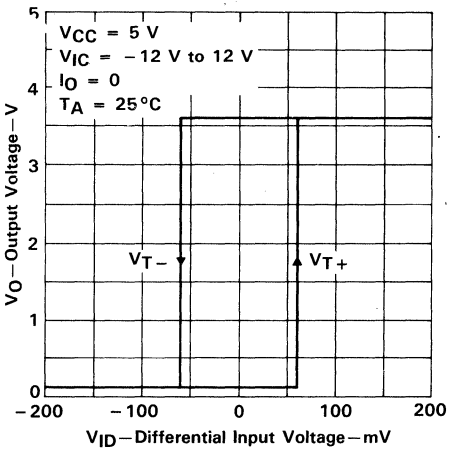


FIGURE 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

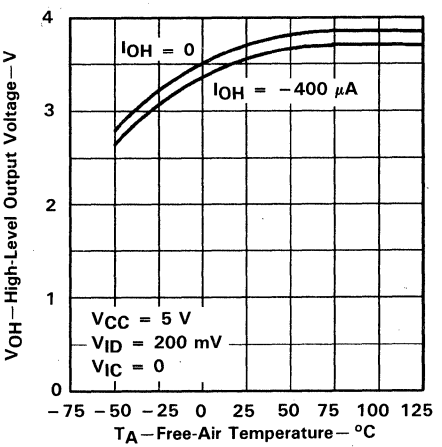


FIGURE 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

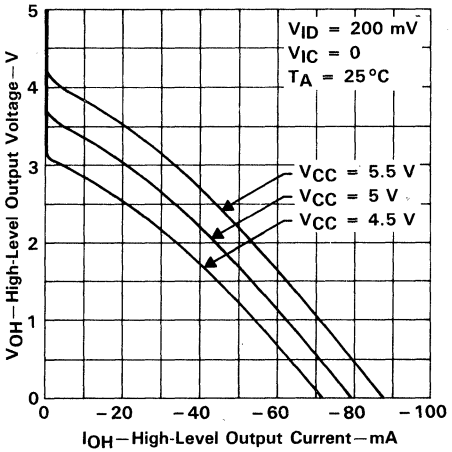


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

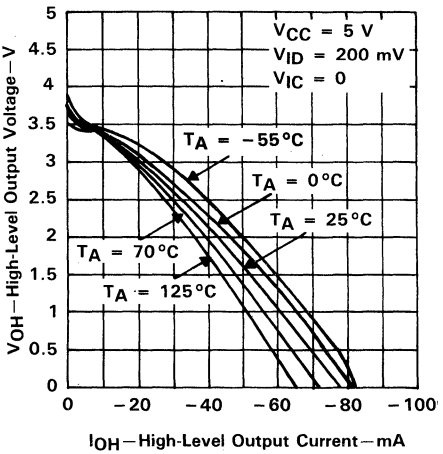


FIGURE 11

†Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

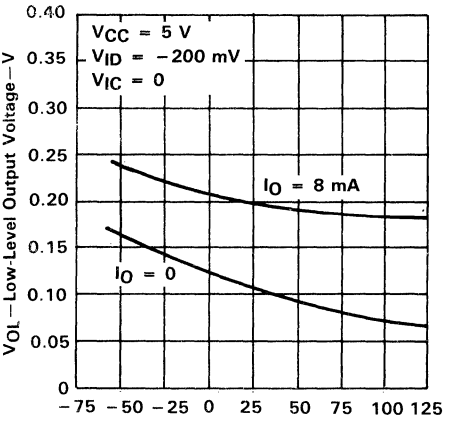


FIGURE 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

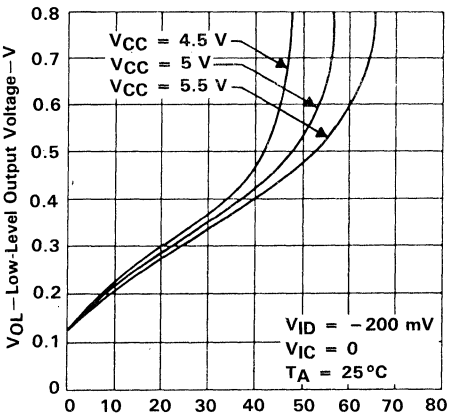


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

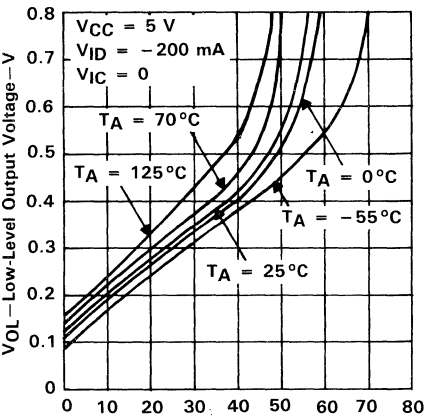


FIGURE 14

†Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

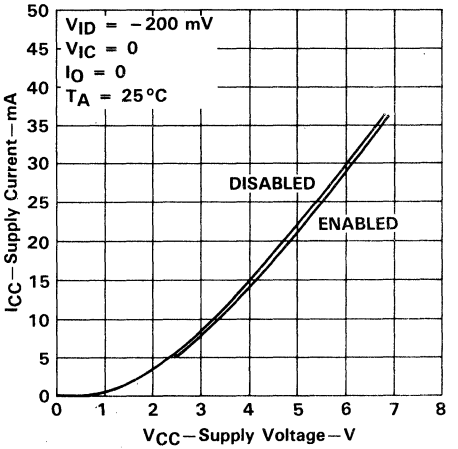


FIGURE 15

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

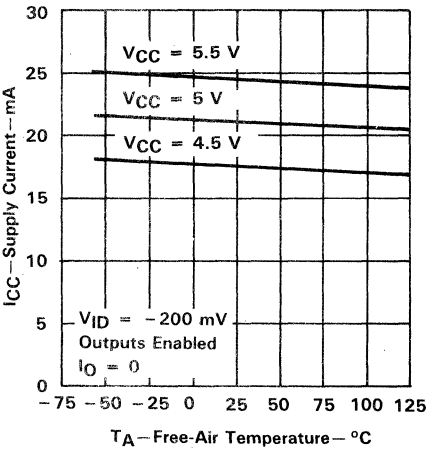


FIGURE 16

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

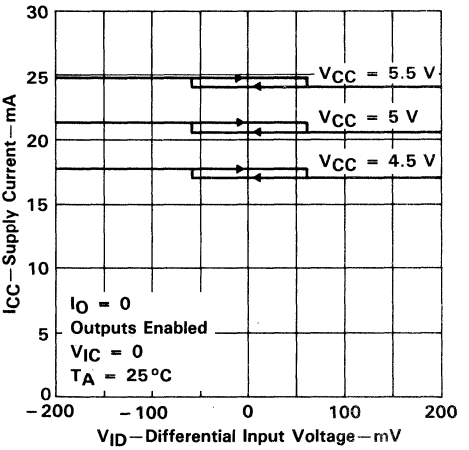


FIGURE 17

SUPPLY CURRENT
vs
FREQUENCY

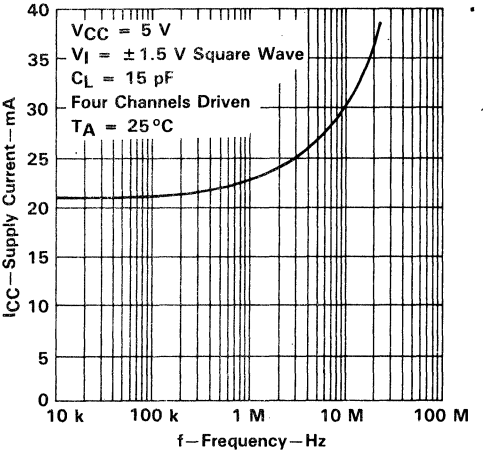


FIGURE 18

†Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

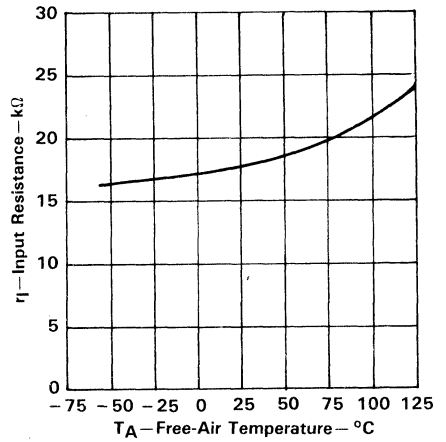


FIGURE 19

INPUT CURRENT
vs
INPUT VOLTAGE

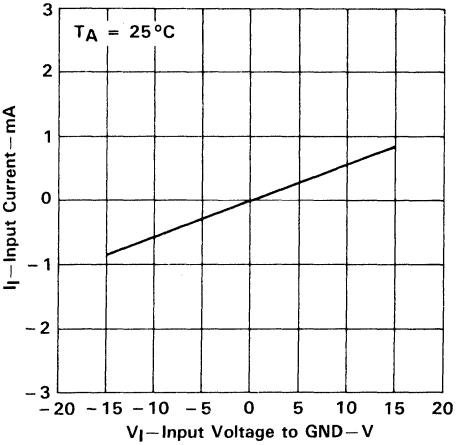


FIGURE 20

SWITCHING CHARACTERISTICS
vs
FREE-AIR TEMPERATURE

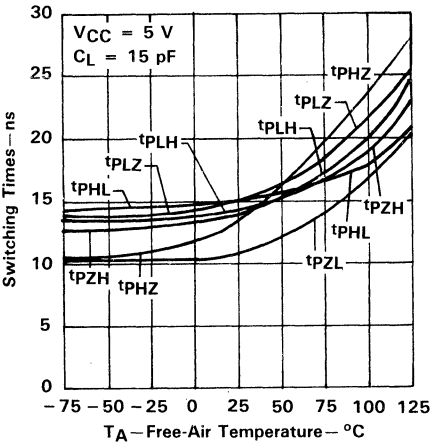


FIGURE 21

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

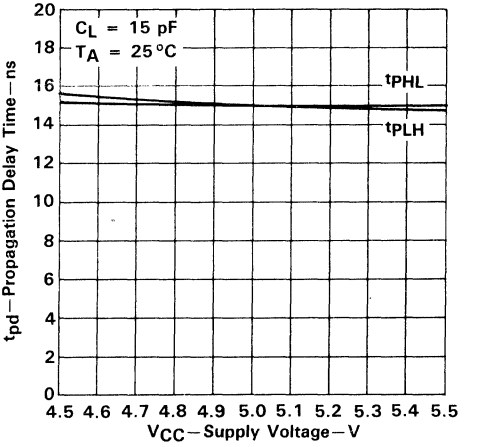


FIGURE 22

†Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

D3407, JANUARY 1990

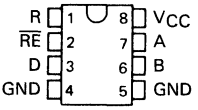
- Bidirectional Transceiver
- Designed for Multipoint Transmission in Noisy Environments Such as Automotive Applications
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability. . . ±10 mA Max
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-V Supply
- Low Power Requirements

description

The SN65076B and SN75076B differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for noisy environments, where a low-impedance termination to ground is required.

The SN65076B and SN75076B combine a differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The receiver has an active-low enable. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

D OR P PACKAGE
(TOP VIEW)



FUNCTION TABLE
(DRIVER)

INPUT	OUTPUTS	
D	A	B
H	H	L
L	L†	H†

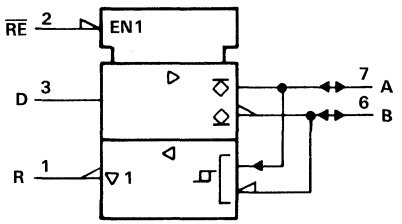
†These levels assume that the open-collector outputs (A) and the open-emitter outputs (B) are connected to a pullup and pull-down resistor, respectively.

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS A − B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	L
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	H
X	H	Z

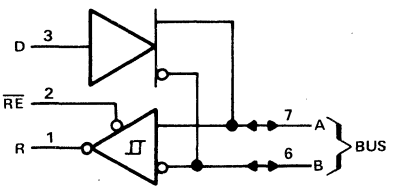
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

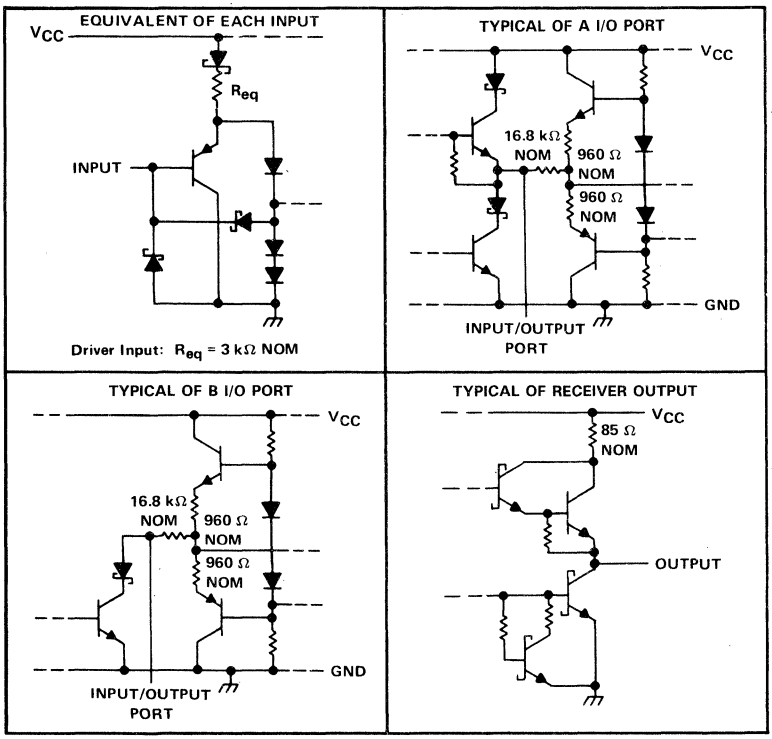
logic diagram (positive logic)



description (continued)

The driver is designed to handle loads up to 10 mA of sink and source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C in the P package and 170°C in the D package. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN65076B is characterized for operation from −40°C to 105°C and the SN75076B is characterized for operation from 0°C to 70°C.



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage at any bus terminal . . . . . −10 V to 15 V
Enable input voltage . . . . . 5.5 V
Continuous total power dissipation (see Note 2) . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN65076B . . . . . −40°C to 105°C
SN75076B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW
P	1100 mW	8.8 mW/°C	702 mW	396 mW

recommended operating conditions

			MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}			4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}					12	V
					−7	
High-level input voltage, V_{IH}		D and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}		D and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)					±12	V
High-level output current, I_{OH}		Driver (A)			−10	mA
		Receiver			−400	μA
Low-level output current, I_{OL}		Driver (B)			10	mA
		Receiver			8	
Operating free-air temperature, T_A	SN65076B		−40		105	°C
	SN75076B		0		70	

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	V_I = 2 V,	I_O = 0	0		6	V
V_{OD1}	Differential output voltage	I_O = 0		1.5		6	V
V_{OD2}	Differential output voltage	See Figure 1		1.5		5	V
I_O	Output current	V_I = 0.8 V	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = 0				−150	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current (total package)	No load				30	mA

†All typical values are at V_{CC} = 5 V and T_A = 25°C.

driver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{on}	Differential-output turn-on time	See Figure 3		60	90	ns
t_{off}	Differential-output turn-off time			75	110	ns

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V, I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V, I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis§			50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA			−1.5	V
V_{OH}	High-level output voltage	V_{ID} = −200 mV, I_{OH} = −400 μA, See Figure 2	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, I_{OL} = 8 mA, See Figure 2			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V			±20	μA
I_I	Line input current	Other input = 0 V, V_I = 12 V See Note 3 V_I = −7 V			1 −0.8	mA
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V			20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V			−100	μA
r_i	Input resistance		12			kΩ
I_{OS}	Short-circuit output current		−15		−85	mA
I_{CC}	Supply current (total package)	No load			30	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for threshold voltage levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.
NOTE 3: This applies for both power on and power off.

receiver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = 0 to 3 V, C_L = 15 pF, See Figure 4		21	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			23	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 5		10	20	ns
t_{PZL}	Output enable time to low level			12	20	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF, See Figure 5		20	35	ns
t_{PLZ}	Output disable time from low level			17	25	ns

PARAMETER MEASUREMENT INFORMATION

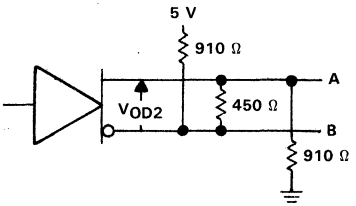


FIGURE 1. DRIVER V_{OD2}

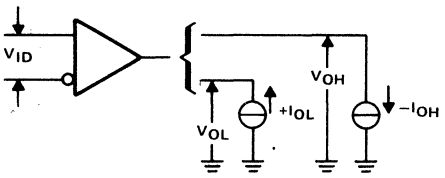
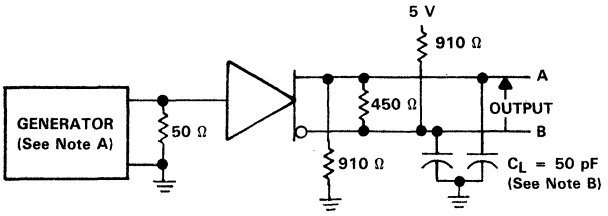
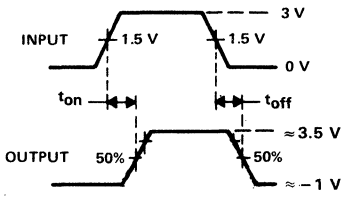


FIGURE 2. RECEIVER V_{OH} AND V_{OL}

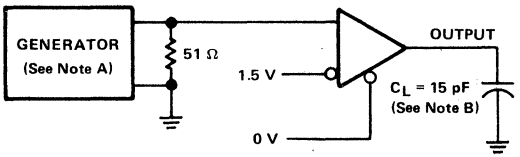


TEST CIRCUIT

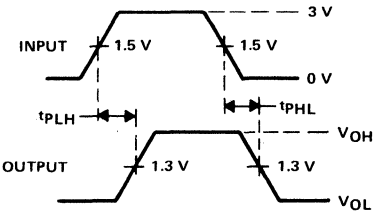


VOLTAGE WAVEFORMS

FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4. RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

TEXAS INSTRUMENTS
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PARAMETER MEASUREMENT INFORMATION

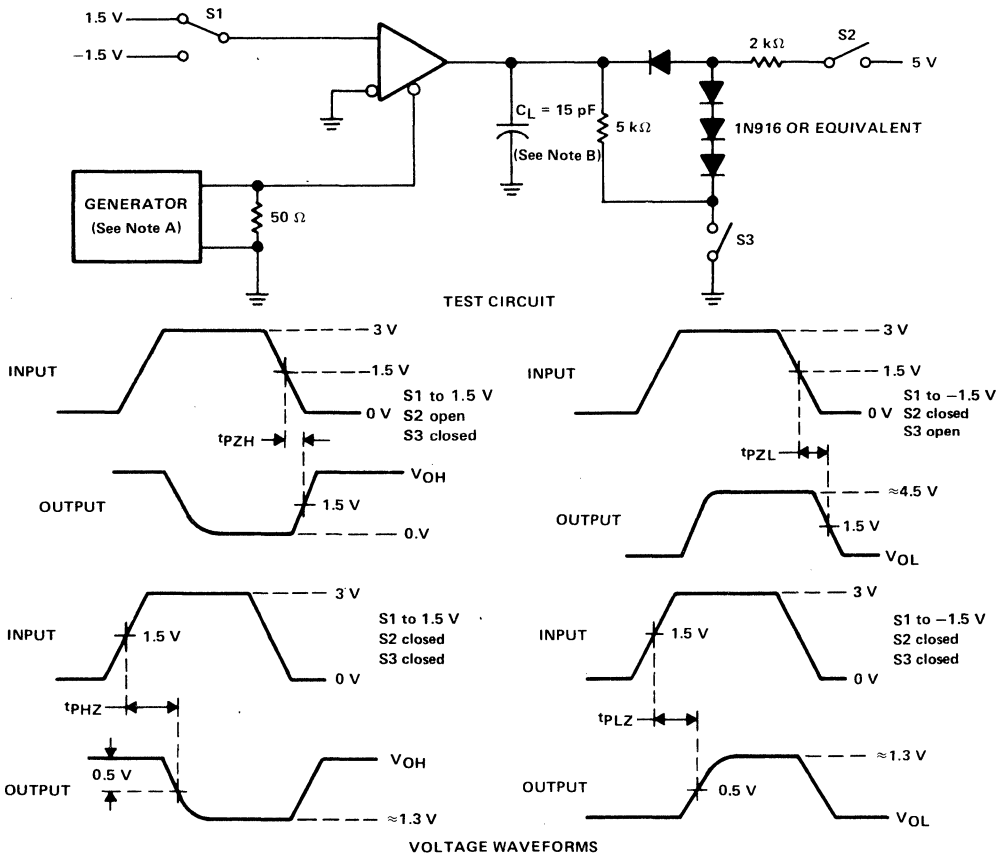


FIGURE 5. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

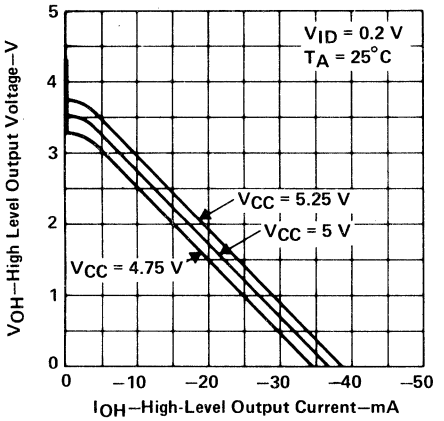


FIGURE 6

RECEIVER HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

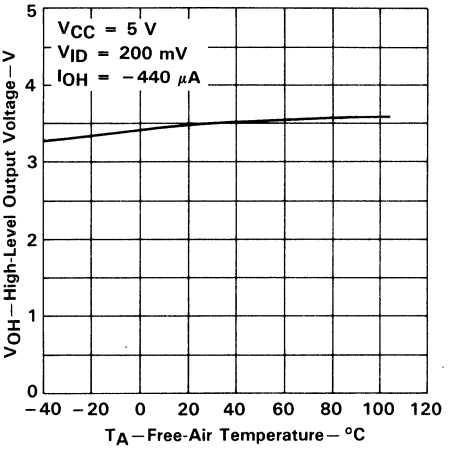


FIGURE 7

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

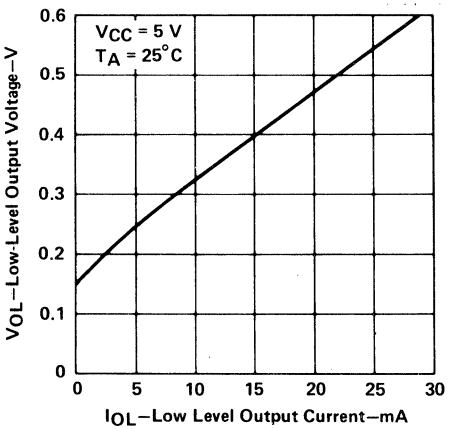


FIGURE 8

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

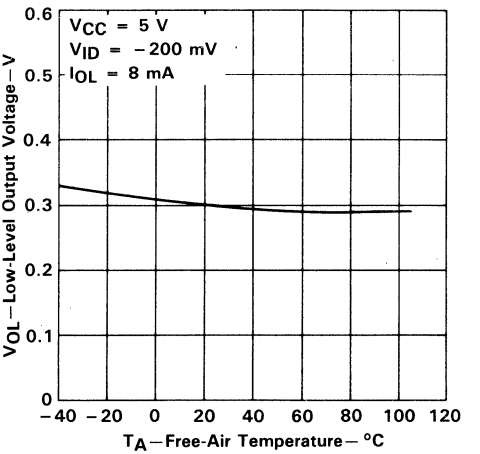


FIGURE 9

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

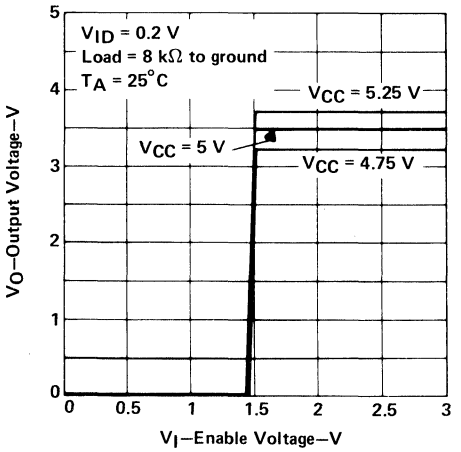


FIGURE 10

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

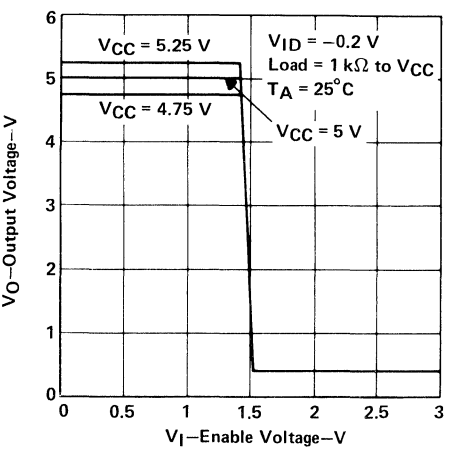


FIGURE 11

TYPICAL APPLICATION

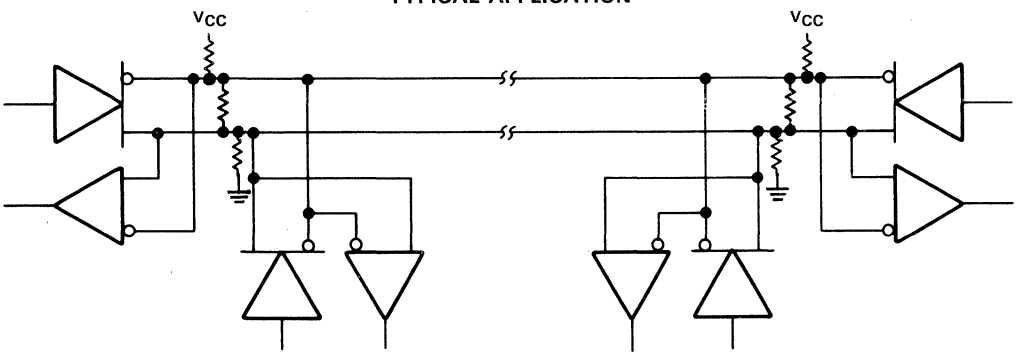
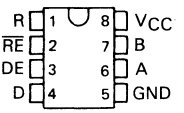


FIGURE 12. TYPICAL APPLICATION CIRCUIT

D2619, JULY 1985—REVISED SEPTEMBER 1989

- Bidirectional Transceiver
- Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability. . . ±60 mA Max
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-V Supply
- Low Power Requirements

D, JG, OR P PACKAGE
(TOP VIEW)



FUNCTION TABLE (DRIVER)

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A − B	$\overline{RE}$	R
$V_{ID} \geq 0.2$ V	L	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

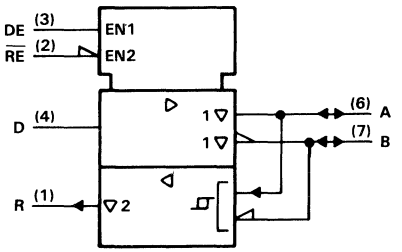
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

description

The SN65176B and SN75176B differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet EIA Standard RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27.

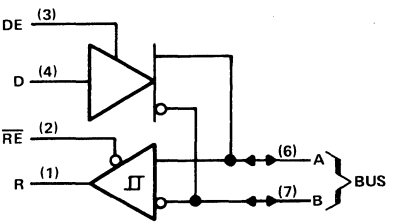
The SN65176B and SN75176B combine a 3-state differential line driver and a differential input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

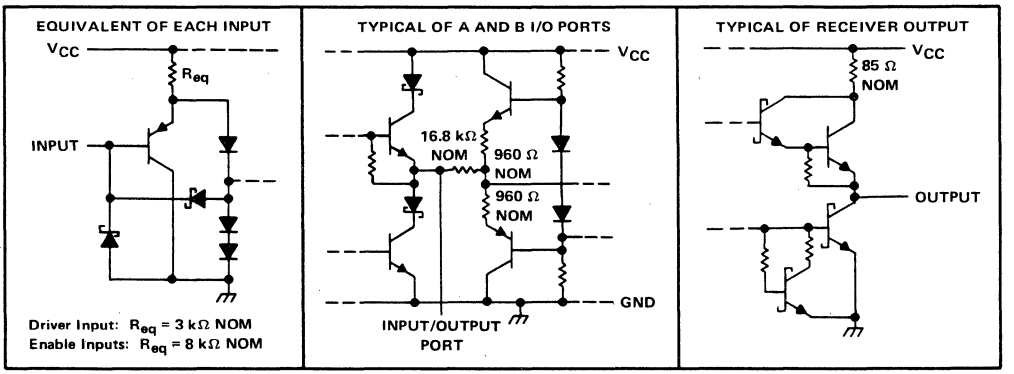


The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN65176B and SN75176B can be used in transmission line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

The SN65176B is characterized for operation from −40°C to 105°C and the SN75176B is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage at any bus terminal . . . . . −10 V to 15 V
Enable input voltage . . . . . 5.5 V
Continuous total power dissipation (see Note 2) . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN65176B . . . . . −40°C to 105°C
SN75176B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

NOTES: 1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
2. In the JG package, the chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 105°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW
JG	825 mW	6.6 mW/°C	528 mW	297 mW
P	1100 mW	8.8 mW/°C	702 mW	396 mW

recommended operating conditions

			MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}			4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}					12	V
					−7	
High-level input voltage, V_{IH}		D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}		D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 3)					±12	V
High-level output current, I_{OH}		Driver			−60	mA
		Receiver			−400	μA
Low-level output current, I_{OL}		Driver			60	mA
		Receiver			8	
Operating free-air temperature, T_A	SN65176B		−40		105	°C
	SN75176B		0		70	

NOTE 3: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1		½ V_{OD1}			
				2			V
		R_L = 54 Ω, See Figure 1		1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 4		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage					+3 −1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Output disabled, See Note 5	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = 0				−150	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	55	mA
			Outputs disabled		26	35	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

NOTES: 4. See EIA Standard RS-485 Figure 3.5, Test Termination Measurement 2.
5. This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

driver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω, See Figure 3			15	22	ns
t_{TD}	Differential-output transition time				20	30	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See Figure 4			85	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See Figure 5			40	60	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, See Figure 4			150	250	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See Figure 5			20	30	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V, I_O = −0.4 mA				0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V, I_O = 8 mA		−0.2‡			V
V_{hys}	Hysteresis§				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = −200 mV, I_{OH} = −400 μA, See Figure 2		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, I_{OL} = 8 mA, See Figure 2				0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 6	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	55	mA
			Outputs disabled		26	35	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
NOTE 6: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

receiver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = 0 to 3 V, C_L = 15 pF, See Figure 6			21	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				23	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 7			10	20	ns
t_{PZL}	Output enable time to low level				12	20	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF, See Figure 7			20	35	ns
t_{PLZ}	Output disable time from low level				17	25	ns

PARAMETER MEASUREMENT INFORMATION

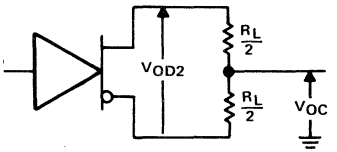


FIGURE 1. DRIVER V_{OD} AND V_{OC}

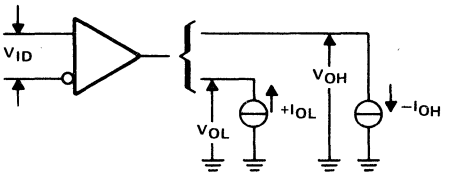
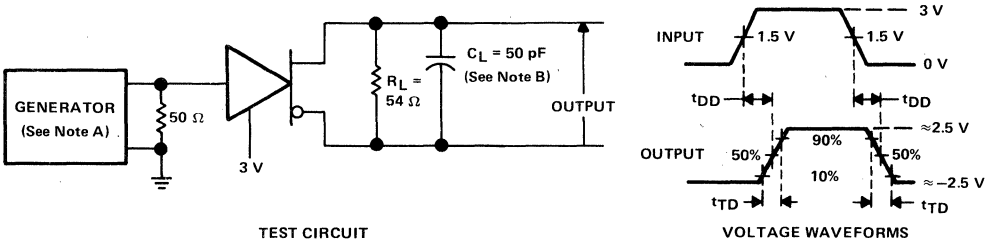
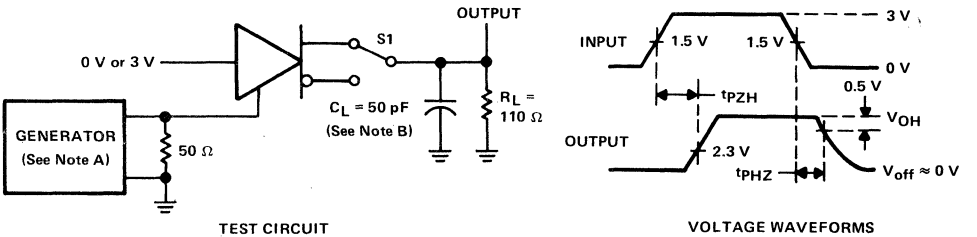


FIGURE 2. RECEIVER V_{OH} AND V_{OL}



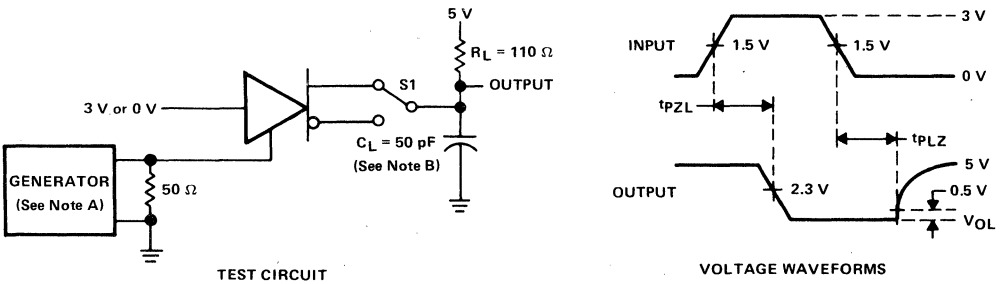
TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 4. DRIVER ENABLE AND DISABLE TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

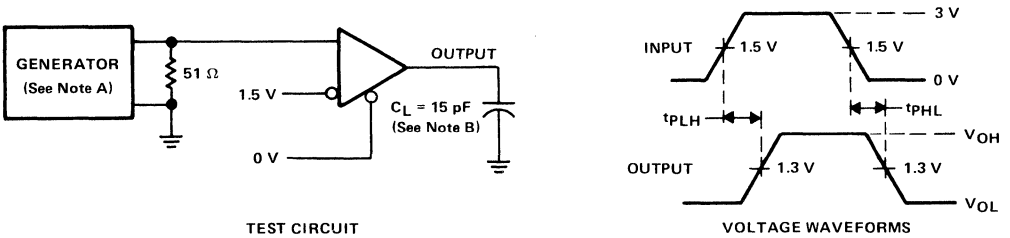


FIGURE 6. RECEIVER PROPAGATION DELAY TIMES

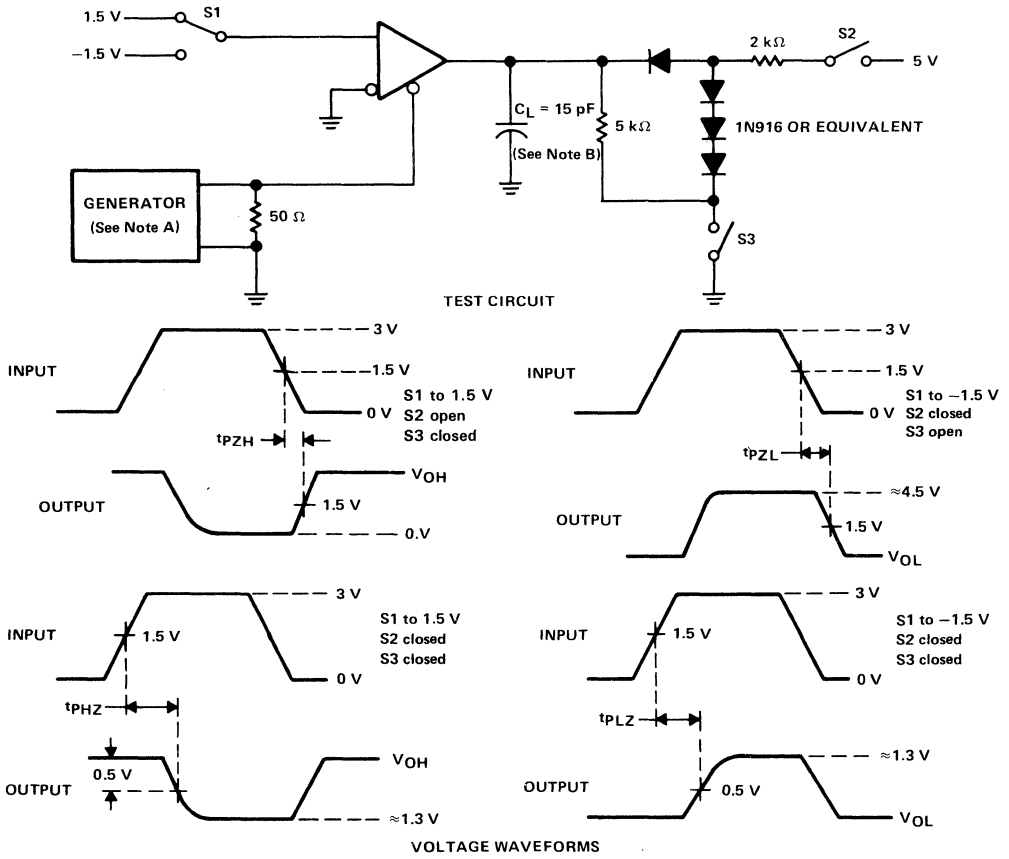


FIGURE 7. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

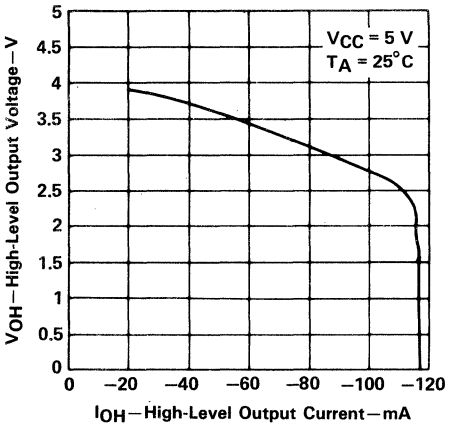


FIGURE 8

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

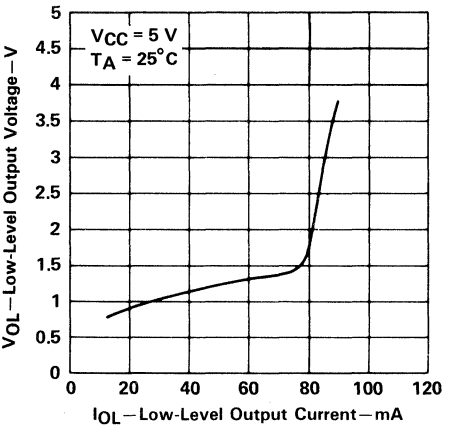


FIGURE 9

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

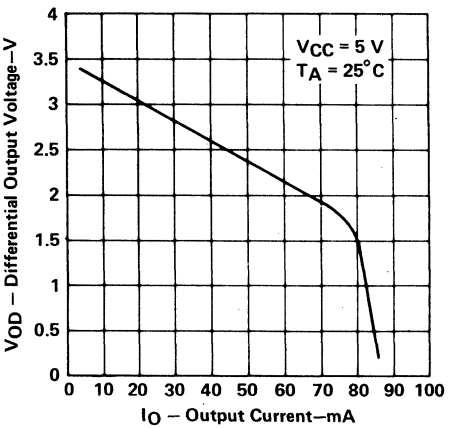


FIGURE 10

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

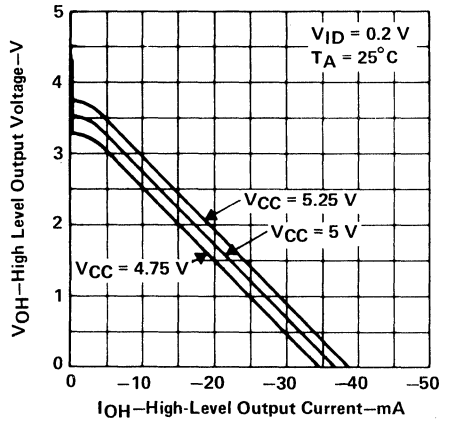


FIGURE 11

RECEIVER HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

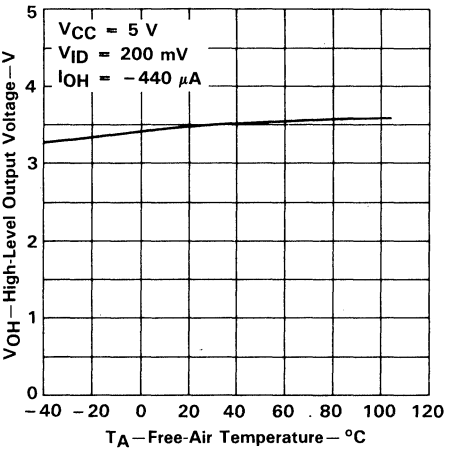


FIGURE 12

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

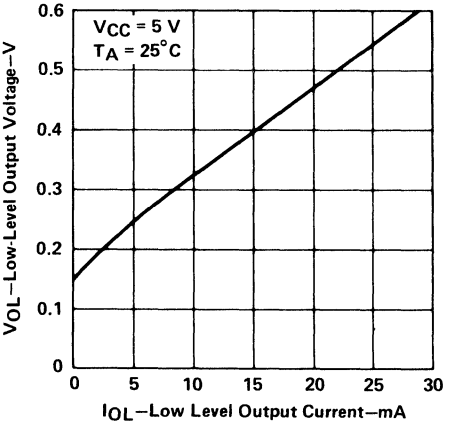


FIGURE 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

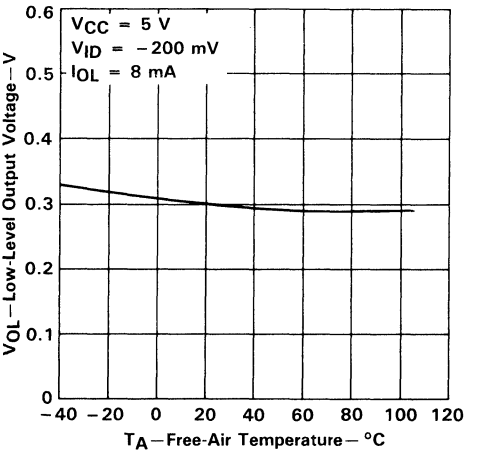


FIGURE 14

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

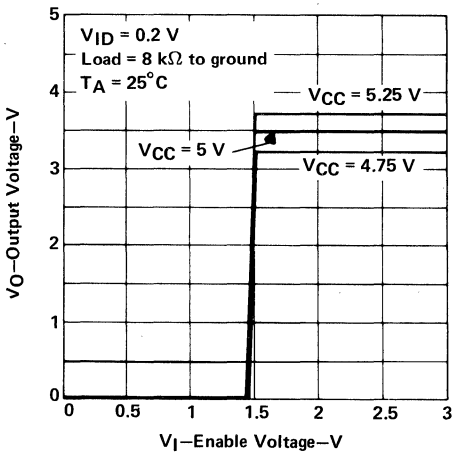


FIGURE 15

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

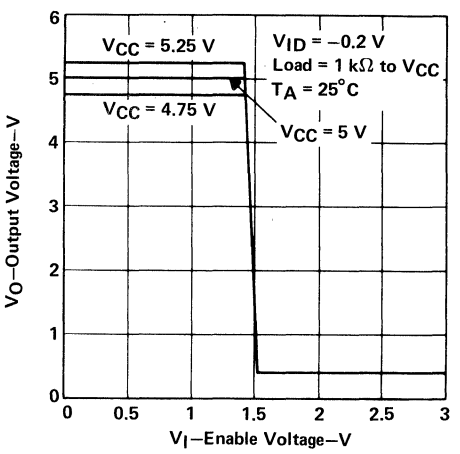


FIGURE 16

TYPICAL APPLICATION

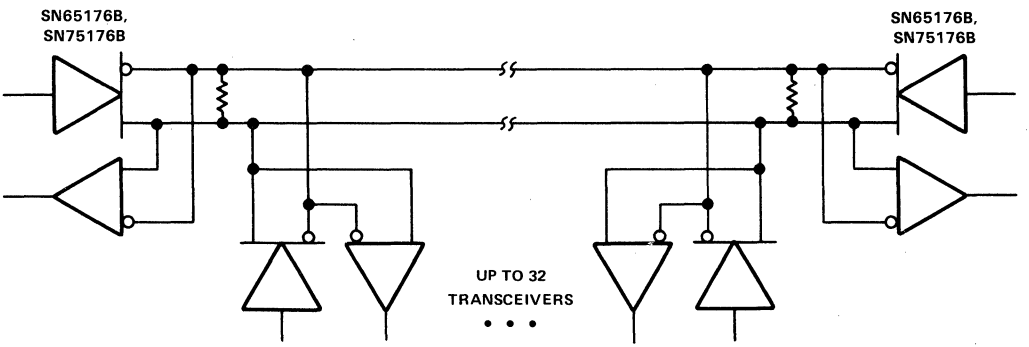


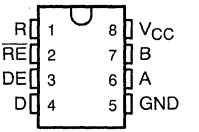
FIGURE 17. TYPICAL APPLICATION CIRCUIT

NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

D3042, AUGUST 1987–REVISED MAY 1990

- **Meets EIA Standards RS-422A and RS-485, CCITT Recommendations V.11 and X.27, and ISO 8482:1987(E)**
- **Designed and Tested for Data Rates up to 35 MBaud**
- **SN65ALS176 Operating Temperature – 40°C to 85°C**
- **Three Skew Limits Available:**
  'ALS176 . . . 10 ns
  'ALS176A . . . 7.5 ns
  'ALS176B . . . 5 ns
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply Current Requirements 30 mA Max**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Receiver Input Hysteresis**
- **Glitch-Free Power-Up and Power-Down Protection**
- **Receiver Open-Circuit Fail-Safe Design**

D OR P PACKAGE
(TOP VIEW)



FUNCTION TABLE (DRIVER)

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} <$ 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

AVAILABLE OPTIONS

T_A	$t_{pmax} - t_{pmin}$	PACKAGE	
	$t_{sk(1)}$‡	SMALL OUTLINE (D)†	PLASTIC DIP (P)
0°C	10	SN75ALS176D	SN75ALS176P
to	7.5	SN75ALS176AD	SN75ALS176AP
70°C	5	SN75ALS176BD	SN75ALS176BP
–40°C to 85°C	10	SN65ALS176D	SN65ALS176P

† The D package is available taped and reeled. Add the suffix R to the device type, (e.g., SN75ALS176DR).
‡ $t_{sk(1)}$ is the greater of 1) the difference between the maximum and minimum specified values of t_{PLH} of (t_{DDH}), and 2) the difference between the maximum and minimum specified values of t_{PHL} (or t_{DDL}). This is the maximum range that the driver or receiver delay time will vary over temperature, V_{CC}, and device-to-device.

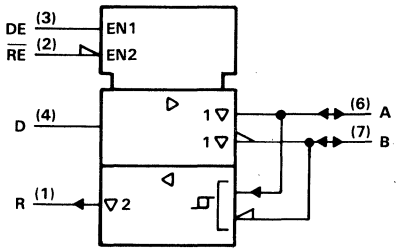
description

The SN65ALS176 and SN75ALS176 series Differential Bus Transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet EIA Standards RS-422-A and RS-485, CCITT recommendations V.11 and X.27, and ISO 8482:1987(E).

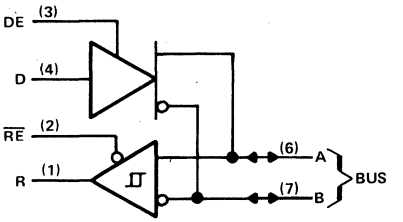
The SN65ALS176 and SN75ALS176 series combine a 3-state differential line driver and a differential input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. This port features wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN65ALS176 is characterized for operation from – 40°C to 85°C and the SN75ALS176 series is characterized for operation from 0°C to 70°C.

logic symbol†

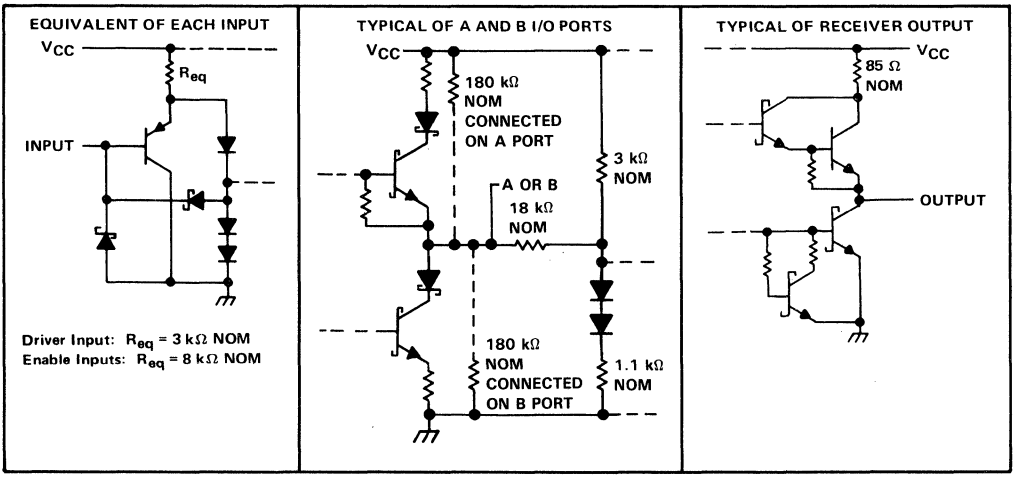


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage at any bus terminal ..... −10 V to 15 V
Enable input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65ALS176 ..... −40°C to 85°C
SN75ALS176 Series ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65ALS176	−40		85	°C
	SN75ALS176	0		70	

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	$I_O = 0$		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	$R_L = 100\ \Omega$, See Figure 1		1/2 V_{OD1}			
				2			V
		$R_L = 54\ \Omega$, See Figure 1		1.5	2.5	5	V
V_{OD3}	Differential output voltage	$V_{test} = -7$ V to 12 V, See Figure 2		1.5		5	V
$\Delta \lvert V_{OD} \rvert$	Change in magnitude of differential output voltage §	$R_L = 54\ \Omega$ or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage					3	V
						−1	
$\Delta \lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Output disabled,	$V_O = 12$ V			1	mA
		See Note 3	$V_O = -7$ V			−0.8	
I_{IH}	High-level input current	$V_I = 2.4$ V				20	μA
I_{IL}	Low-level input current	$V_I = 0.4$ V				−400	μA
I_{OS}	Short-circuit output current ¶	$V_O = -6$ V	SN65ALS176			−250	mA
		$V_O = -7$ V	SN75ALS176				
		$V_O = 0$	All			−150	
		$V_O = V_{CC}$	All				
		$V_O = 8$ V	SN65ALS176			250	
		$V_O = 12$ V	SN75ALS176				
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.
§ $\Delta \lvert V_{OD} \rvert$ and $\Delta \lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
¶ Duration of the short circuit should not exceed one second.
NOTE 3: This applies for both power on and off; refer to EIA standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

driver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

SN65ALS176

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{DD}	Differential output delay time	R_L = 54 Ω, C_L = 50 pF, See Figure 3			15	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{DDL} - t_{DDH} \rvert$)			0	2	ns
t_{TD}	Differential output transition time			8		ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, C_L = 50 pF, See Figure 4			80	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, C_L = 50 pF, See Figure 5			30	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, C_L = 50 pF, See Figure 4			50	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, C_L = 50 pF, See Figure 5			30	ns

SN75ALS176, SN75ALS176A, SN75ALS176B

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{DD}	Differential output delay time	'ALS176	R_L = 54 Ω, C_L = 50 pF, See Figure 3	3	8	13	ns
		'ALS176A		4	7	11.5	
		'ALS176B		5	8	10	
$t_{sk(p)}$	Pulse skew ($\lvert t_{DDL} - t_{DDH} \rvert$)				0	2	ns
t_{TD}	Differential output transition time				8		ns
t_{PZH}	Output enable time to high level		R_L = 110 Ω, C_L = 50 pF, See Figure 4		23	50	ns
t_{PZL}	Output enable time to low level		R_L = 110 Ω, C_L = 50 pF, See Figure 5		14	20	ns
t_{PHZ}	Output disable time from high level		R_L = 110 Ω, C_L = 50 pF, See Figure 4		20	35	ns
t_{PLZ}	Output disable time from low level		R_L = 110 Ω, C_L = 50 pF, See Figure 5		8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$		V_t (Test Termination Measurement 2)
$\Delta \lvert V_{OD} \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis§				60		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = −200 mV, See Figure 6	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 6	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = 7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12	20		kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0	−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

SN65ALS176

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd}	Propagation time	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF, See Figure 7			25	ns
$t_{sk(p)}$	Pulse skew (| $t_{PHL} - t_{PLH}$ |)			0	2	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 8		11	18	ns
t_{PZL}	Output enable time to low level			11	18	ns
t_{PHZ}	Output disable time from high level				50	ns
t_{PLZ}	Output disable time from low level				30	ns

SN75ALS176, SN75ALS176A, SN75ALS176B

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd}	Propagation time	'ALS176	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF, See Figure 7	9	14	19	ns
		'ALS176A		10.5	14	18	
		'ALS176B		11.5	13	16.5	
$t_{sk(p)}$	Pulse skew (| $t_{PHL} - t_{PLH}$ |)				0	2	ns
t_{PZH}	Output enable time to high level		C_L = 15 pF, See Figure 8		7	14	ns
t_{PZL}	Output enable time to low level				20	35	ns
t_{PHZ}	Output disable time from high level				20	35	ns
t_{PLZ}	Output disable time from low level				8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

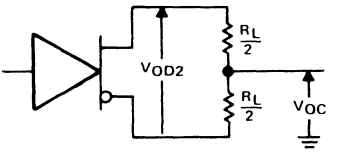


FIGURE 1. DRIVER V_{OD} AND V_{OC}

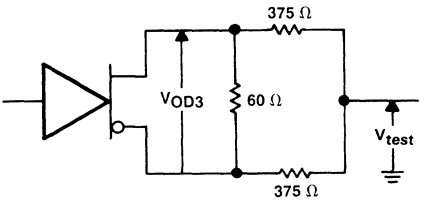
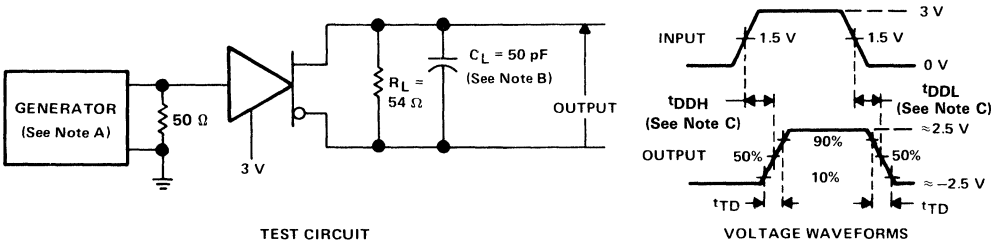


FIGURE 2. DRIVER V_{OD3}



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. t_{DD} = t_{DDH} or t_{DDL}

FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

PARAMETER MEASUREMENT INFORMATION

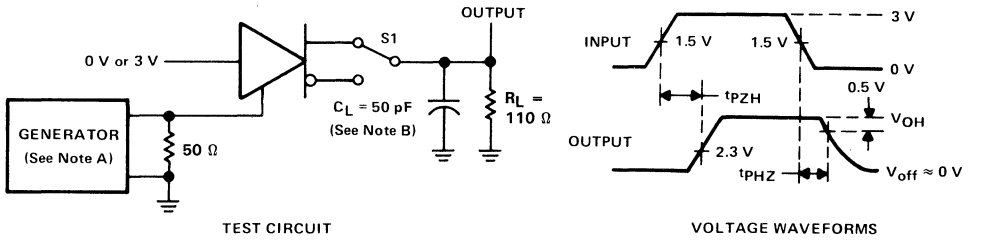


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

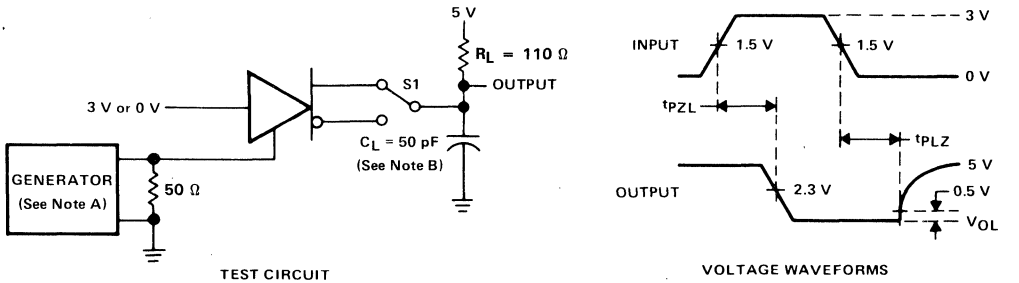


FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

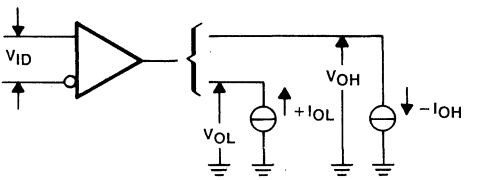
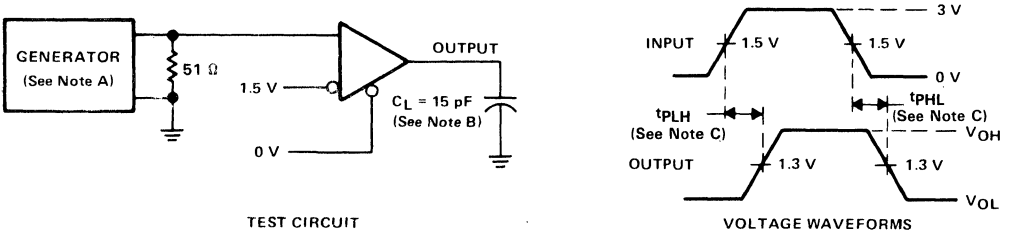


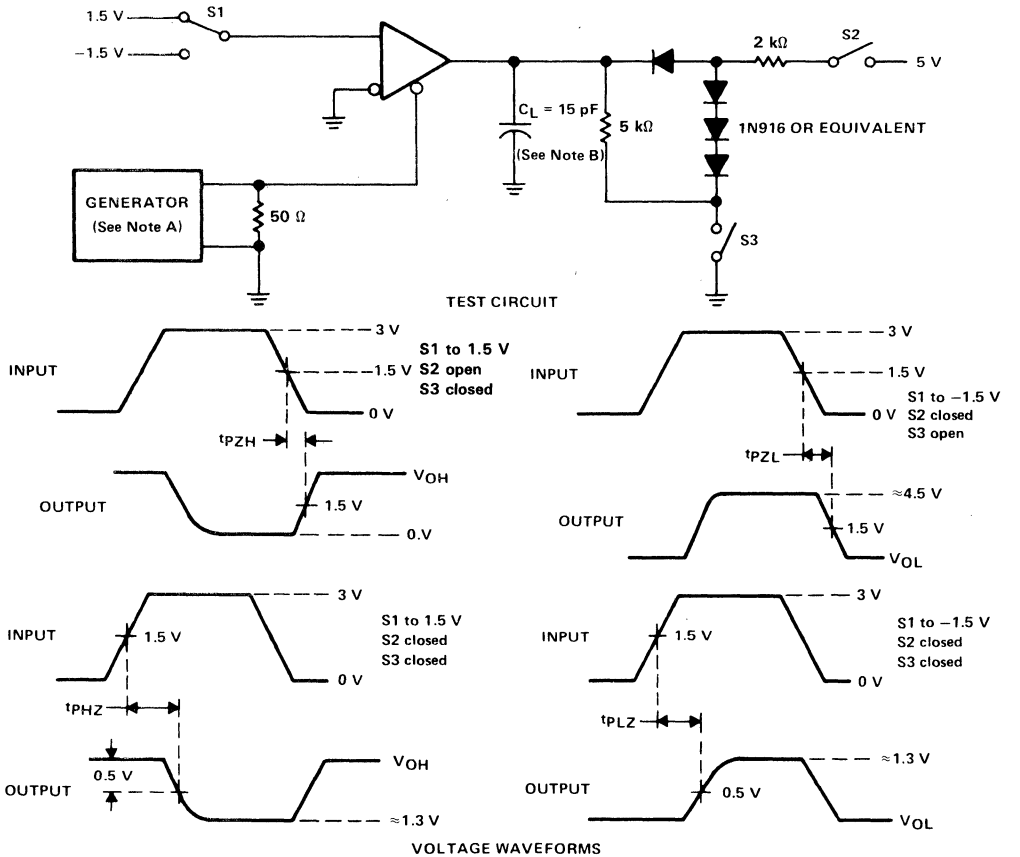
FIGURE 6. RECEIVER V_{OH} AND V_{OL}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 7. RECEIVER PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS

FIGURE 8. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. $t_{pd} = t_{PLH}$ or t_{PHL}

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

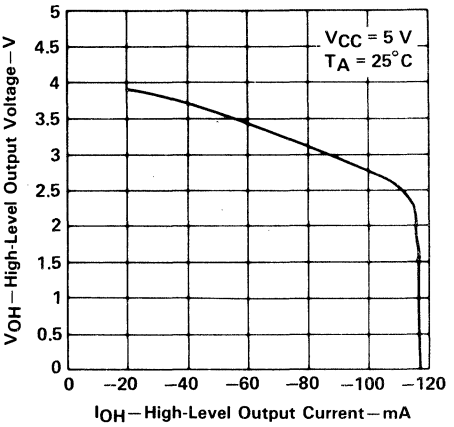


FIGURE 9

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

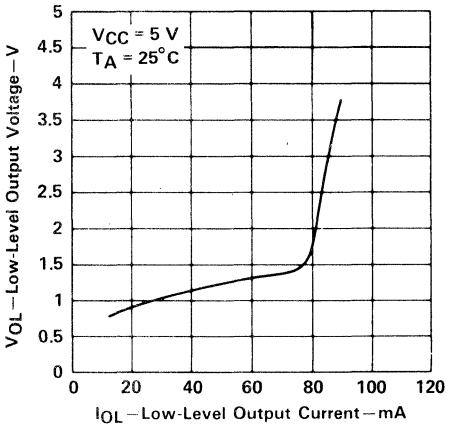


FIGURE 10

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

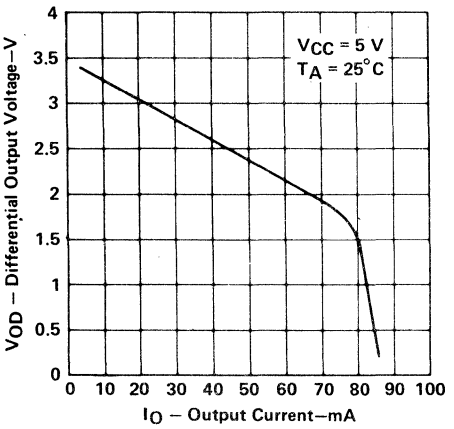


FIGURE 11

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

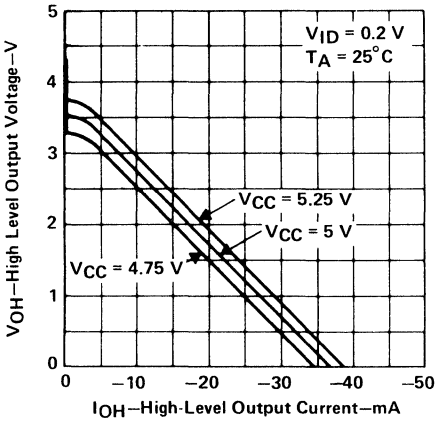


FIGURE 12

RECEIVER HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

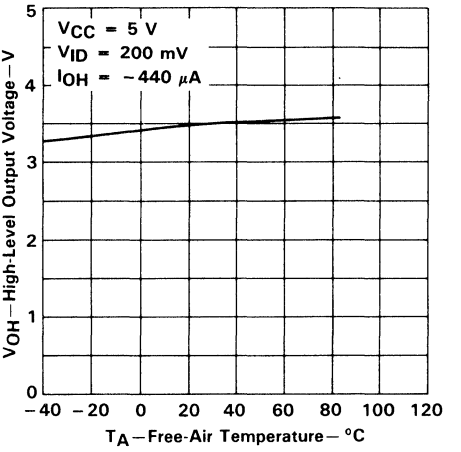


FIGURE 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

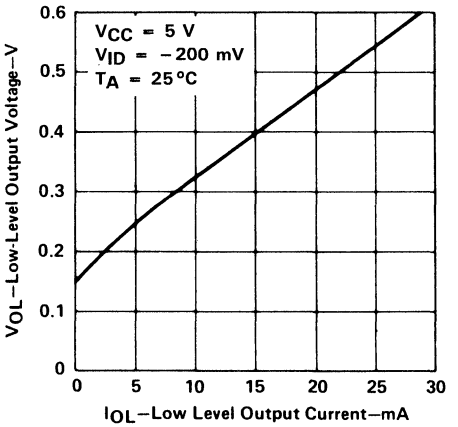


FIGURE 14

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

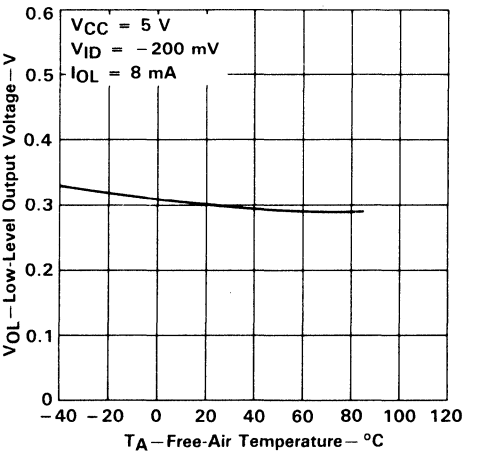


FIGURE 15

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

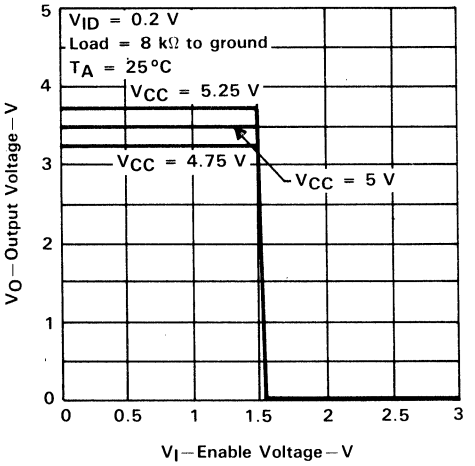


FIGURE 16

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

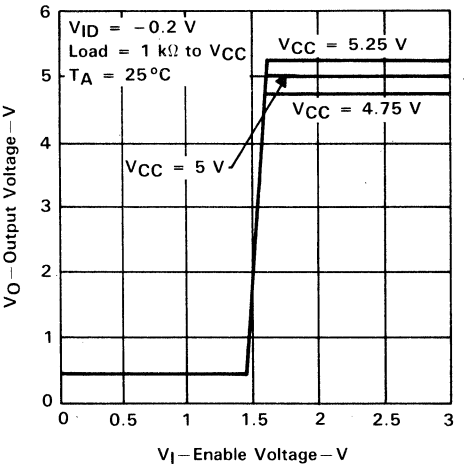


FIGURE 17

APPLICATION INFORMATION

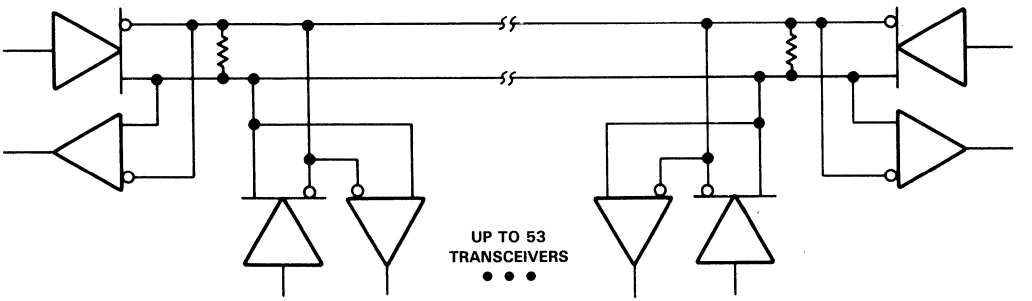


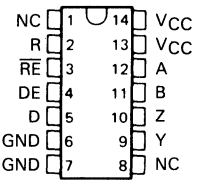
FIGURE 18. TYPICAL APPLICATION CIRCUIT

NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

D3043, AUGUST 1987 – REVISED DECEMBER 1989

- **Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Designed for 25-MBaud Operation in Both Serial and Parallel Applications**
- **Low Skew between Devices . . . 6 ns Max**
- **Low Supply Current Requirements 30 mA Max**
- **Individual Driver and Receiver I/O pins with Dual V_{CC} and Dual GND**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Receiver Input Impedances . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV Max**
- **Receiver Input Hysteresis . . . 60 mV Typ**
- **Operates from a Single 5-V Supply**
- **Glitch-Free Power-Up and Power-Down Protection**

D OR N PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE (DRIVER)

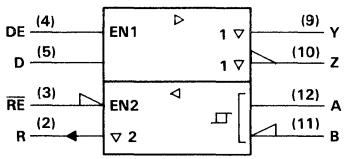
INPUT	ENABLE	OUTPUTS	
D	DE	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A – B	$\overline{RE}$	R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} <$ 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

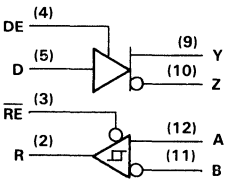
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



description

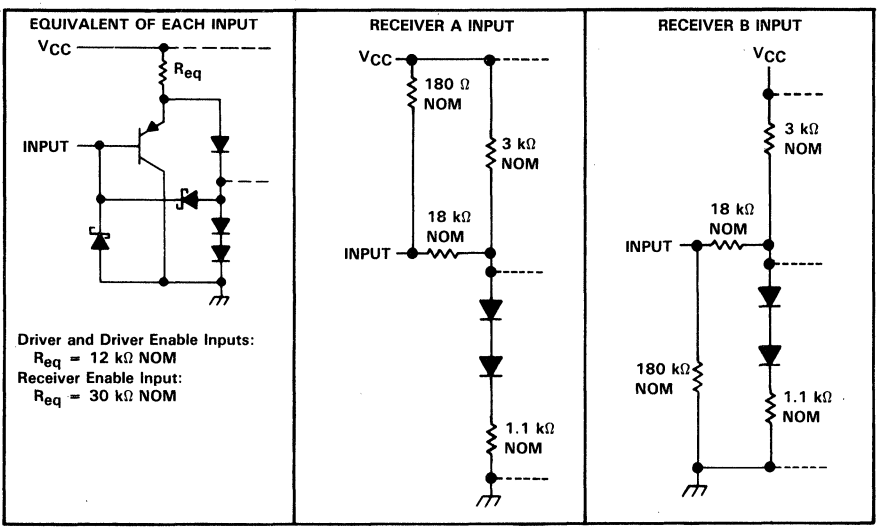
The SN65ALS180 and SN75ALS180 Differential Driver and Receiver Pairs are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet EIA Standards RS-422-A and RS-485 and CCITT recommendations V.11 and X.27.

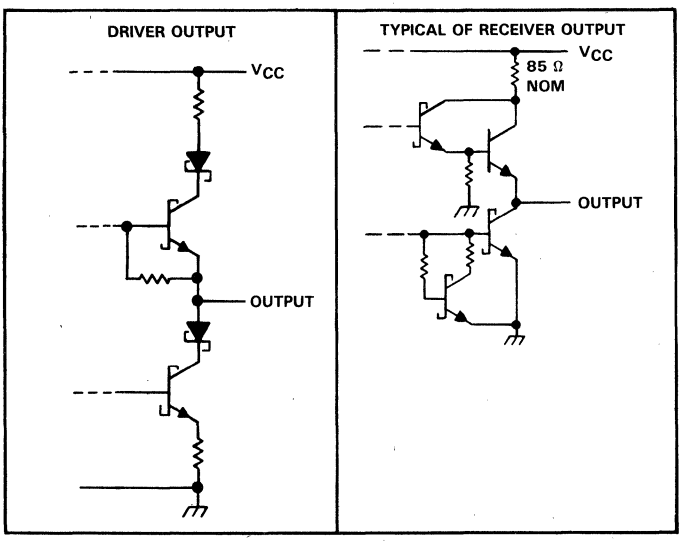
The SN65ALS180 and SN75ALS180 combine a 3-state differential line driver and a differential input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected to separate pins for greater flexibility and are designed to offer

minimum loading to the bus when the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN65ALS180 is characterized for operation from −40°C to 85°C and the SN75ALS180 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage at any bus terminal . . . . . −10 V to 15 V
Enable input voltage . . . . . 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65ALS180 . . . . . −40°C to 85°C
SN75ALS180 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

			MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}			4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}					12 −7	V
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$		2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$				0.8	V
Differential input voltage, V_{ID} (see Note 2)					±12	V
High-level output current, I_{OH}	Driver				−60	mA
	Receiver				−400	µA
Low-level output current, I_{OL}	Driver				60	mA
	Receiver				8	
Operating free-air temperature, T_A		SN65ALS180	−40		85	°C
		SN75ALS180	0		70	

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A/Y with respect to the inverting terminal B/Z.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	I_O = 0		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	1/2 V_{OD1}			V
				2			
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	V_{test} = −7 V to 12 V,	See Figure 2	1.5		5	V
$\Delta \lvert V_{OD} \rvert$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					+3 −1	V
$\Delta \lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Output disabled, See Note 3	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	µA
I_{OS}	Short-circuit output current¶	V_O = −7 V	SN75ALS180			−250	mA
		V_O = −6 V	SN65ALS180				
		V_O = 0	All			−150	
		V_O = V_{CC}	All			250	
		V_O = 8 V	SN65ALS180				
		V_O = 12 V	SN75ALS180				
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.

§ $\Delta \lvert V_{OD} \rvert$ and $\Delta \lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

¶ Duration of the short circuit should not exceed one second.

NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

driver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω, See Figure 3	C_L = 50 pF,	3	8	13	ns
	Skew ($\lvert t_{DDH} - t_{DDL} \rvert$)				1	6	ns
t_{TD}	Differential output transition time			3	8	13	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		23	50	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		19	24	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4		8	13	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5		8	13	ns

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$		V_t (Test Termination Measurement 2)
V_{test}		V_{tst}
$\Delta \lvert V_{OD} \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis§				60		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 6	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 6	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V,	V_I = 12 V			1	mA
		See Note 4	V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0	−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.

NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, See Figure 7, C_L = 15 pF	9	14	19	ns
t_{PHL}	Propagation delay time, high-to-low-level output		9	14	19	ns
	Skew ($\lvert t_{PLH} - t_{PHL} \rvert$)			2	6	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 8		7	14	ns
t_{PZL}	Output enable time to low level			7	14	ns
t_{PHZ}	Output disable time from high level			20	35	ns
t_{PLZ}	Output disable time from low level			8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

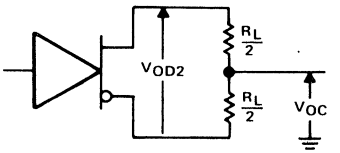


FIGURE 1. DRIVER V_{OD} AND V_{OC}

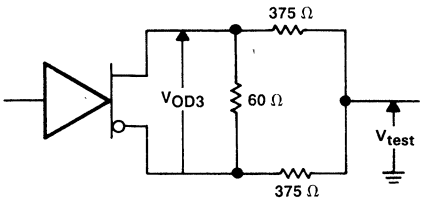


FIGURE 2. DRIVER V_{OD3}

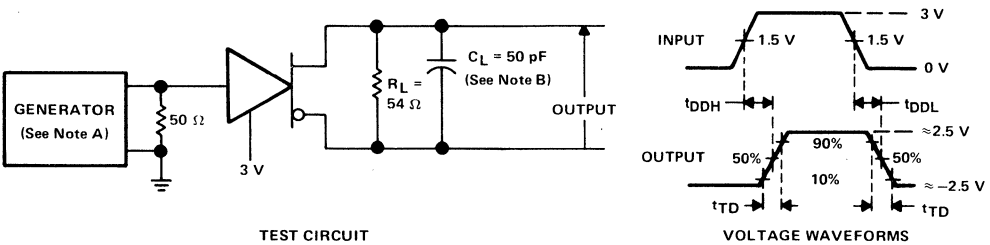


FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

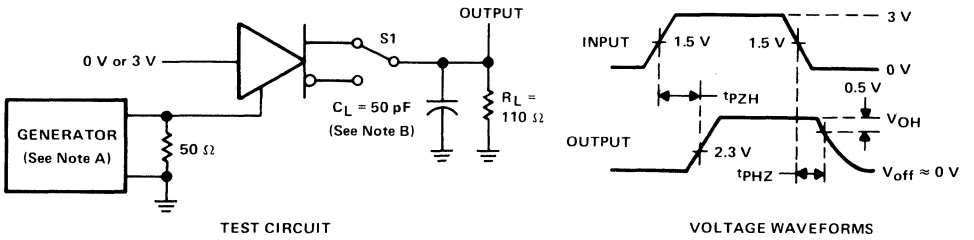


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

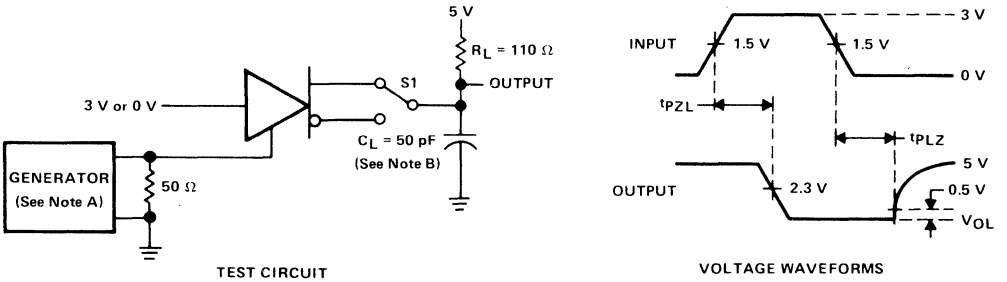


FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

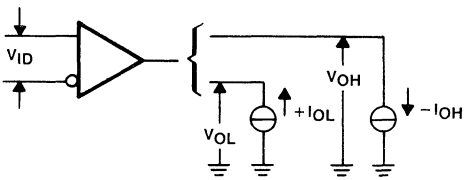
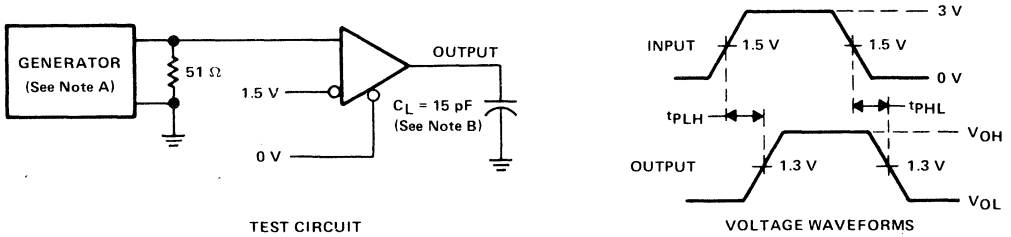


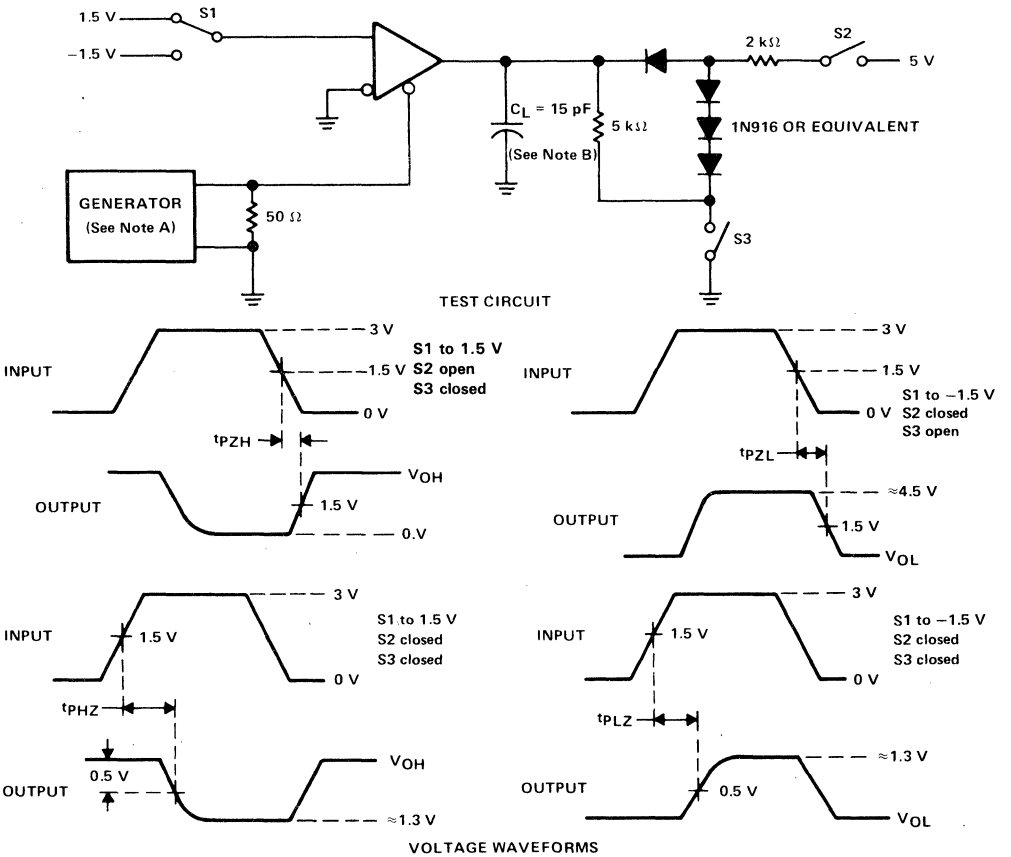
FIGURE 6. RECEIVER V_{OH} AND V_{OL}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 7. RECEIVER PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS

FIGURE 8. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 5 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

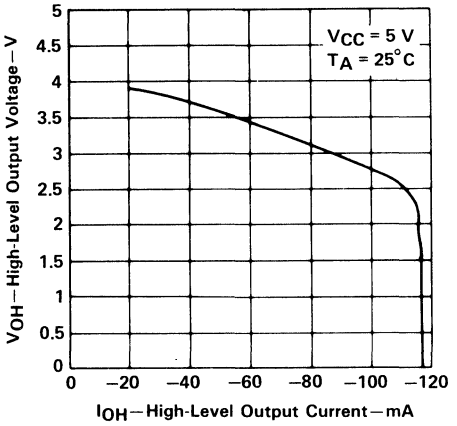


FIGURE 9

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

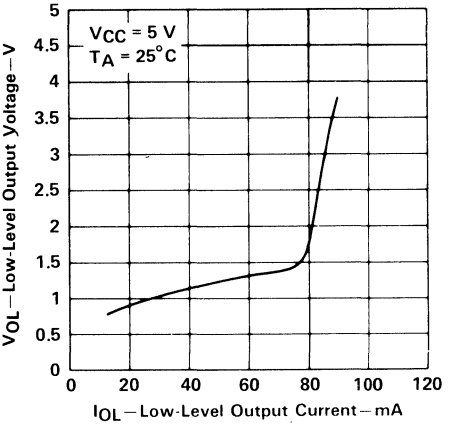


FIGURE 10

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

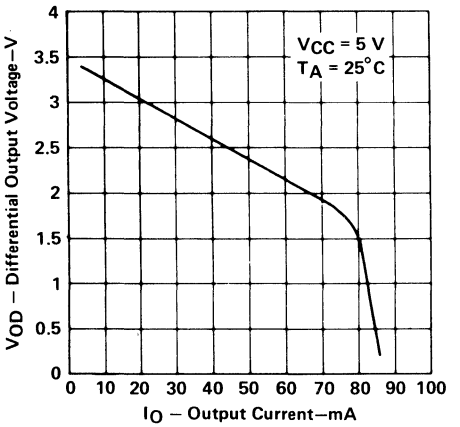


FIGURE 11

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

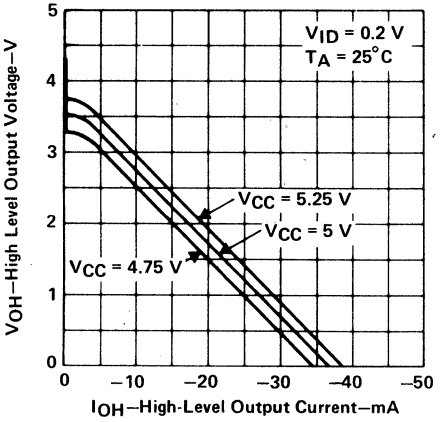


FIGURE 12

RECEIVER HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

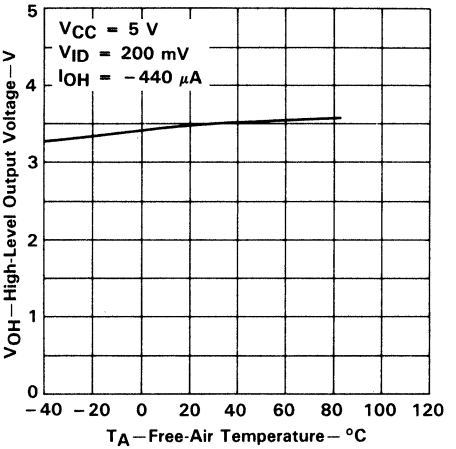


FIGURE 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

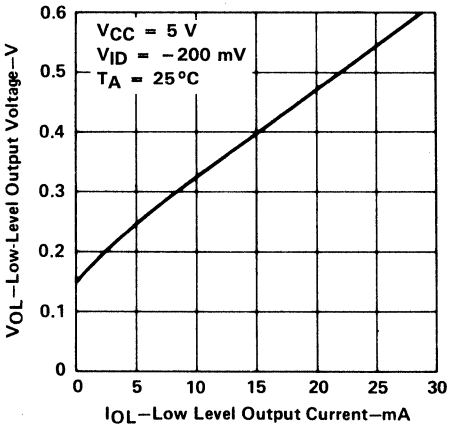


FIGURE 14

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

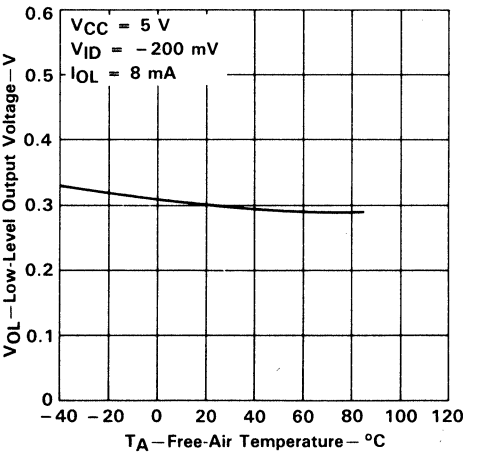


FIGURE 15

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

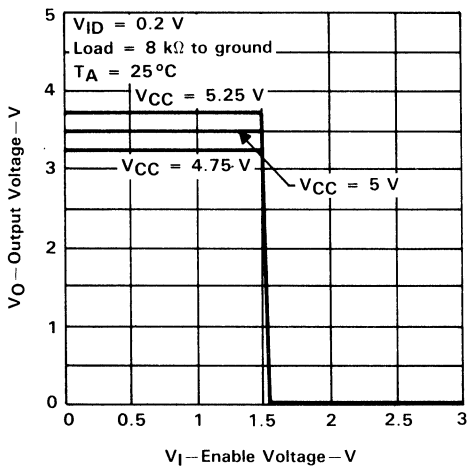


FIGURE 16

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

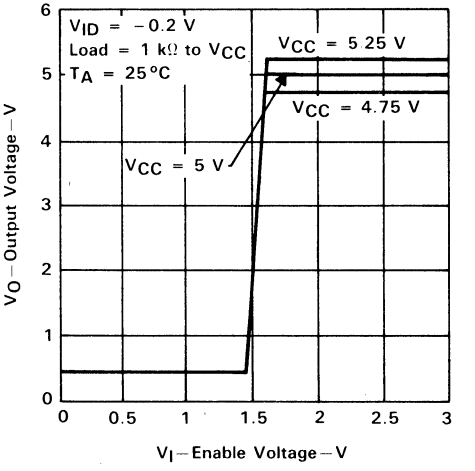
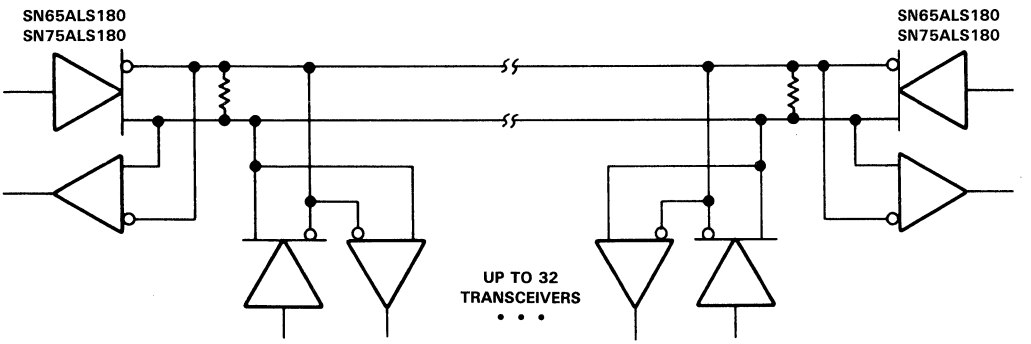


FIGURE 17

APPLICATION INFORMATION



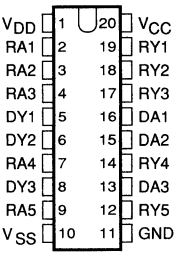
NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 18. TYPICAL APPLICATION CIRCUIT

D3325, AUGUST 1989 – REVISED JULY 1990

- **Meets Standard EIA-232-D (Revision of RS-232-C)**
- **Single Chip With Easy Interface Between UART and Serial Port Connector**
- **Less than 8-mW Power Consumption**
- **Wide Driver Supply Voltage . . . 4.5 V to 13.2 V**
- **Driver Output Slew Rate Limited to 30 V/µs Max**
- **Receiver Input Hysteresis . . . 800 mV Typ**
- **Push-Pull Receiver Outputs**
- **On-Chip Receiver 1-µs Noise Filter**
- **ESD Protection Exceeds 1000 V Per MIL-STD-883C, Method 3015**

DW OR N PACKAGE
(TOP VIEW)

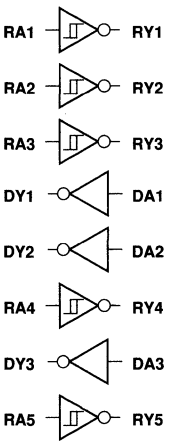


description

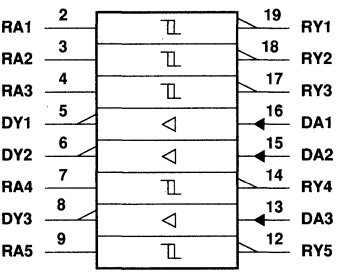
The SN65C185 and SN75C185 are low-power BIMOS devices containing three independent drivers and five receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). The SN65C185 and SN75C185 will typically replace one SN75188 and two SN75189 devices. These devices have been designed to conform to Standards ANSI/EIA-232-D-1986, which supersedes RS-232-C. The three drivers and five receivers of the SN65C185 and SN75C185 are similar to those of the SN75C188 quadruple drivers and SN75C189A quadruple receivers, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/µs and the receivers have filters that reject input noise pulses that are shorter than 1 µs. Both these features eliminate the need for external components.

The SN65C185 and SN75C185 have been designed using low-power techniques in a BI-MOS technology. In most applications the receivers contained in these devices will interface to single inputs of peripheral devices such as ACEs, UARTs, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN65C185 and SN75C185 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

logic diagram (positive logic)



logic symbol†

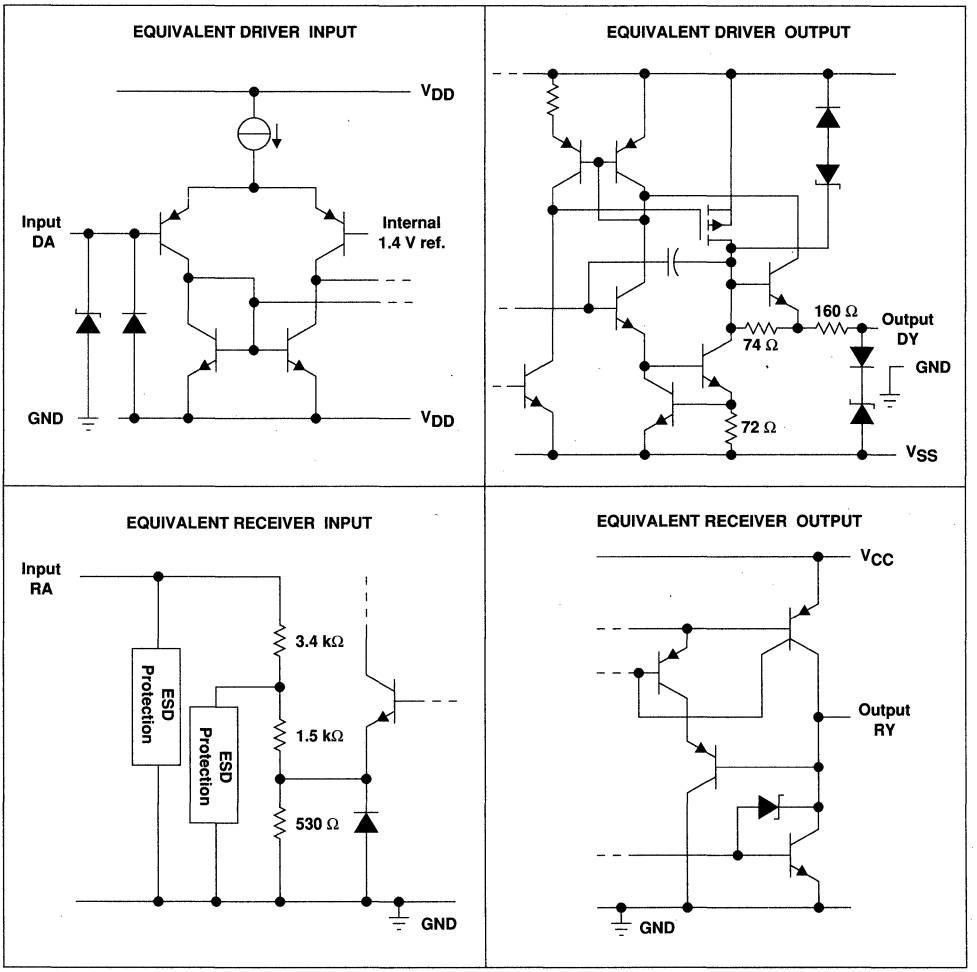


†This symbol in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-122.

description (continued)

The SN65C185 is characterized for operation from –40°C to 85°C. The SN75C185 is characterized for operation from 0°C to 70°C.

equivalent schematics of inputs and outputs



All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 13.5 V
Supply voltage, V_{SS} . . . . . −13.5 V
Supply voltage, V_{CC} . . . . . 7 V
Input voltage range, Driver . . . . . V_{SS} to V_{DD}
Receiver . . . . . −30 V to 30 V
Output voltage range, Driver . . . . . V_{SS} − 6 V to V_{DD} + 6 V
Receiver . . . . . −0.3 V to V_{CC} + 0.3 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65C185 . . . . . −40°C to 85°C
SN75C185 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	585 mW
N	1150 mW	9.2 mW/°C	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	12	13.2	V
Supply voltage, V_{SS}		−4.5	−12	−13.2	V
Supply voltage, V_{CC}		4.5	5	6	V
Input voltage, V_I (see Note 2)	Driver	V_{SS} + 2		V_{DD}	V
	Receiver	−25		25	
High-level input voltage, V_{IH}	Driver	2			V
Low-level input voltage, V_{IL}				0.8	
High-level output current, I_{OH}	Receiver			−1	mA
Low-level output current, I_{OL}				3.2	mA
Operating free-air temperature, T_A	SN65C185	−40		85	°C
	SN75C185	0		70	

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if −10 V is a maximum, the typical value is a more negative voltage.

SUPPLY CURRENTS

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Supply current from V_{DD}	No load, All inputs at 2 V or 0.8 V	V_{DD} = 5 V, V_{SS} = −5 V		115	200	µA
			V_{DD} = 12 V, V_{SS} = −12 V		115	200	
I_{SS}	Supply current from V_{SS}	No load, All inputs at 2 V or 0.8 V	V_{DD} = 5 V, V_{SS} = −5 V		−115	−200	µA
			V_{DD} = 12 V, V_{SS} = −12 V		−115	−200	
I_{CC}	Supply current from V_{CC}	No load, All inputs at 0 or 5 V	V_{DD} = 5 V, V_{SS} = −5 V			750	µA
			V_{DD} = 12 V, V_{SS} = −12 V			750	

DRIVER SECTION

driver electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 5 V, V_{SS} = −5 V	4	4.5		V
			V_{DD} = 12 V, V_{SS} = −12 V	10	10.8		
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 0.8 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 5 V, V_{SS} = −5 V		−4.4	−4	V
			V_{DD} = 12 V, V_{SS} = −12 V		−10.7	−10	
I_{IH}	High-level input current	V_I = 5 V, See Figure 2				1	µA
I_{IL}	Low-level input current	V_I = 0, See Figure 2				−1	µA
$I_{OS(H)}$	High-level short circuit output current (see Note 3)	V_I = 0.8 V, V_O = 0 or V_O = V_{SS}, See Figure 1		−4.5	−12	−19.5	mA
$I_{OS(L)}$	Low-level short circuit output current (see Note 3)	V_I = 2 V, V_O = 0 or V_O = V_{DD}, See Figure 1		4.5	12	19.5	mA
r_o	Output resistance	V_{DD} = V_{SS} = V_{CC} = 0, V_O = −2 V to 2 V, See Note 4		300	400		Ω

†All typical values are at T_A = 25°C.

NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if −10 V is a maximum, the typical value is a more negative voltage.
3. Not more than one output should be shorted at one time.
4. Test conditions are those specified by EIA-232-D.

driver switching characteristics, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10%, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output (see Note 5)	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3		1.2	3	µs
t_{PHL}	Propagation delay time, high-to-low-level output (see Note 5)			2.5	3.5	µs
t_{TLH}	Transition time, low-to-high-level output		0.53	2	3.2	µs
t_{THL}	Transition time, high-to-low-level output		0.53	2	3.2	µs
t_{TLH}	Transition time, low-to-high-level output (see Note 6)	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 3		1.0	3	µs
t_{THL}	Transition time, high-to-low-level output (see Note 6)			1.0	3	µs
SR	Output slew rate (see Note 6)	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3	4	10	30	V/µs

NOTES: 5. t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate and is measured at the 50% points.
6. Measured between 3-V and −3-V points of output waveform (EIA-232-D conditions), all unused inputs tied either high or low.

RECEIVER SECTION

receiver electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = −12V, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	See Figure 5		1.6	2.1	2.55	V
V_{T-}	Negative-going threshold voltage	See Figure 5		0.65	1	1.25	V
V_{hys}	Input hysteresis (see Note 7)			600	1000		mV
V_{OH}	High-level output voltage	V_I = 0.75 V, I_{OH} = −20 µA, See Figure 5 and Note 8		3.5			V
		V_I = 0.75 V, I_{OH} = −1 mA, See Figure 5	V_{CC} = 4.5 V	2.8	4.4		
			V_{CC} = 5 V	3.8	4.9		
			V_{CC} = 5.5 V	4.3	5.4		
V_{OL}	Low-level output voltage	V_I = 3 V, I_{OL} = 3.2 mA, See Figure 5			0.17	0.4	V
I_{IH}	High-level input current	V_I = 3 V		0.43	0.55	1	mA
		V_I = 25 V		3.6	4.6	8.3	
I_{IL}	Low-level input current	V_I = −3 V		−0.43	−0.55	−1	mA
		V_I = −25 V		−3.6	−5.0	−8.3	
$I_{OS(H)}$	Short-circuit output current at high-level	V_I = 0.75, V_O = 0, See Figure 4			−8	−15	mA
$I_{OS(L)}$	Short-circuit output current at low-level	V_I = V_{CC}, V_O = V_{CC}, See Figure 4			13	25	µA

†All typical values are at T_A = 25°C.

NOTES: 7. Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

8. If the inputs are left unconnected, the receiver interprets this as an input low, and the receiver outputs will remain in the high state.

receiver switching characteristics, V_{DD} = 12 V, V_{SS} = −12V, V_{CC} = 5 V ± 10%, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 5 kΩ, C_L = 50 pF, See Figure 6		3	4	µs
t_{PHL}	Propagation delay time, high-to-low-level output			3	4	µs
t_{TLH}	Transition time, low-to-high-level output			300	450	ns
t_{THL}	Transition time, high-to-low-level output			100	300	ns
$t_{w(N)}$	Pulse duration of longest pulse rejected as noise (see Note 9)	R_L = 5 kΩ, C_L = 50 pF, See Figure 6	1		4	µs

NOTE 9: The intent of this specification is that any input pulse of less than 1 µs will have no effect on the output, and any pulse duration of greater than 4 µs will cause the output to change state twice. Reaction to a pulse duration between 1 µs and 4 µs is uncertain.

PARAMETER MEASUREMENT INFORMATION

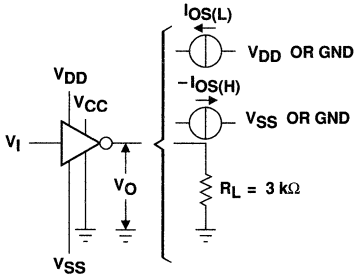


Figure 1. Driver Test Circuit for V_{OH}, V_{OL}, $I_{OS(H)}$, and $I_{OS(L)}$

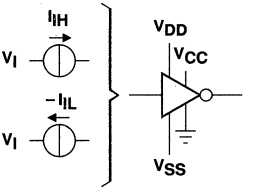
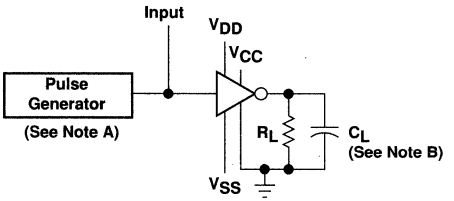
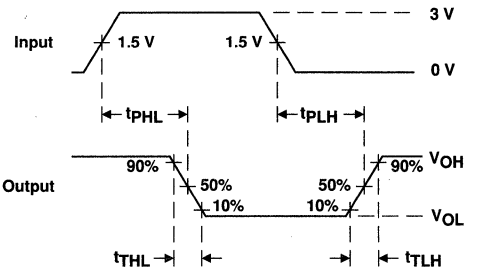


Figure 2. Driver Test Circuit for I_{IH} and I_{IL}



(a) DRIVER TEST CIRCUIT



(b) DRIVER VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, t_r = t_f < 50 ns.
B. CL includes probe and jig capacitance.

Figure 3. Driver Propagation and Transition Times

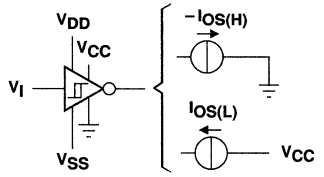


Figure 4. Receiver Test Circuit for $I_{OS(H)}$ and $I_{OS(L)}$

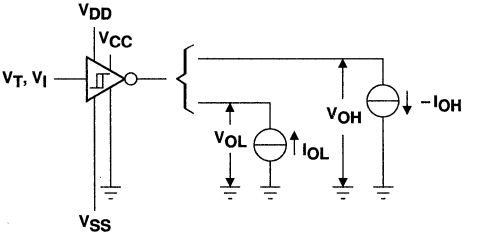
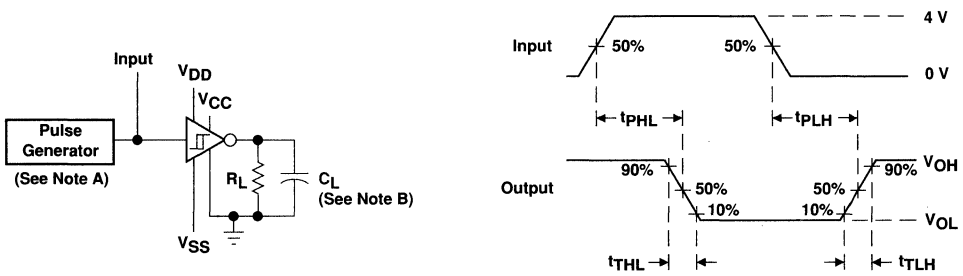


Figure 5. Receiver Test Circuit for V_T, V_{OH}, and V_{OL}

PARAMETER MEASUREMENT INFORMATION



(a) RECEIVER TEST CIRCUIT

(b) RECEIVER VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, t_r = t_f < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Propagation and Transition Times

APPLICATION INFORMATION

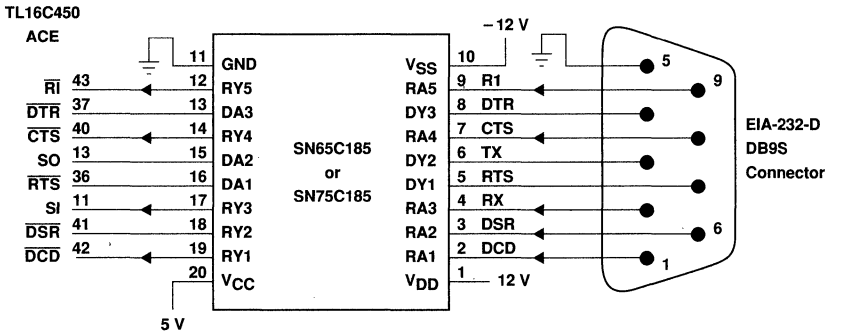
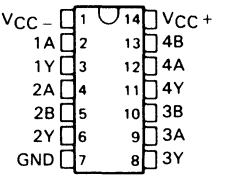


Figure 7. Typical Connection

D3075, JANUARY 1988—REVISED MAY 1990

- BiMOS Technology With TTL and CMOS Compatibility
- Meets Standard EIA-232-D (Revision of RS-232-C)
- Very Low Quiescent Current: 95 μA Typ
  $V_{CC\pm}$ = ±12 V
- Current-Limited Output: 10 mA Typ
- CMOS- and TTL-Compatible Inputs
- On-Chip Slew Rate Limited to 30 V/μs max
- Flexible Supply Voltage Range
- Characterized at V_{CC} ± of ± 4.5 V and ± 15 V
- Functionally Interchangeable With Texas Instruments SN75188, Motorola MC1488, and National Semiconductor DS14C88
- ESD Protection Exceeds 2000 V Per MIL-Std-883C Method 3015

D, DB, OR N PACKAGE
(TOP VIEW)



FUNCTION TABLES

DRIVER 1

A	Y
H	L
L	H

DRIVERS 2 THRU 4

A	B	Y
H	H	L
L	X	H
X	L	H

H = High Level L = Low Level X = Don't Care

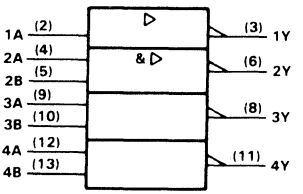
description

The SN65C188 and SN75C188 are monolithic, low-power, quadruple line drivers that interface data terminal equipment with data communications equipment. These devices are designed to conform to Standard ANSI/EIA-232-D-1986, which supercedes RS-232-C.

An external diode in series with each supply-voltage terminal is needed to protect the SN65C188 and SN75C188 under certain fault conditions to comply with EIA-232-D (refer to Application Information).

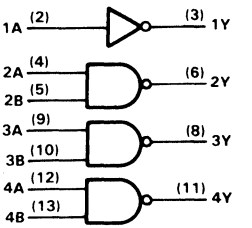
The SN65C188 is characterized for operation from −40°C to 85°C. The SN75C188 is characterized for operation from 0°C to 70°C.

logic symbol†



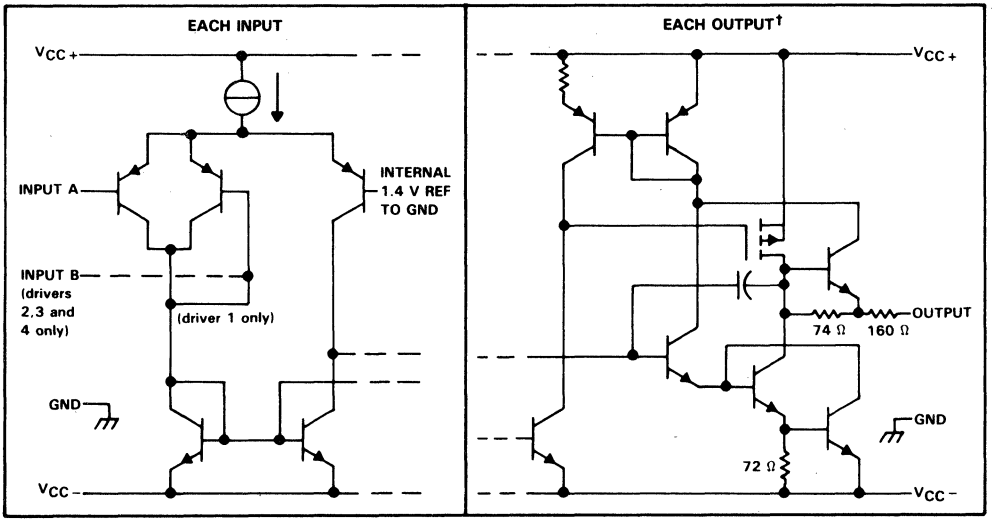
†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



positive logic
$Y = \overline{A}$ (driver 1)
$Y = \overline{AB}$ or $\overline{A} + \overline{B}$ (drivers 2 thru 4)

schematics of inputs and outputs



†All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −15 V
Input voltage range, V_I . . . . . V_{CC-} to V_{CC+}
Output voltage range, V_O . . . . . V_{CC-} − 6 V to V_{CC+} + 6 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65C188 . . . . . −40°C to 85°C
SN75C188 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1, 6 mm (1/16 in.) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
DB	525 mW	4.2 mW/°C	273 mW
N	1150 mW	9.2 mW/°C	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}		4.5	12	15	V
Supply voltage, V_{CC-}		−4.5	−12	−15	V
Input voltage, V_I		V_{CC-} +2		V_{CC+}	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Operating free-air temperature, T_A	SN65C188	−40		85	°C
	SN75C188	0		70	

electrical characteristics over operating free-air temperature range, V_{CC+} = 12 V, V_{CC-} = −12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ	V_{CC+} = 5 V, V_{CC-} = −5 V	4			V
			V_{CC+} = 12 V, V_{CC-} = −12 V	10			
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 2 V, R_L = 3 kΩ	V_{CC+} = 5 V, V_{CC-} = −5 V			−4	V
			V_{CC+} = 12 V, V_{CC-} = −12 V			−10	
I_{IH}	High-level input current	V_I = 5 V				10	μA
I_{IL}	Low-level input current	V_I = 0				−10	μA
$I_{OS(H)}$	Short-circuit output current at high level‡	V_I = 0.8 V, V_O = 0 or V_{CC-}		−5.5	−10	−19.5	mA
$I_{OS(L)}$	Short-circuit output current at low level‡	V_I = 2 V, V_O = 0 or V_{CC+}		5.5	10	19.5	mA
r_o	Output resistance, power off	V_{CC+} = 0, V_{CC-} = 0, V_O = −2 V to 2 V		300			Ω
I_{CC+}	Supply current from V_{CC+}	V_{CC+} = 5 V, V_{CC-} = −5 V, No load	All inputs at 2 V or 0.8 V		90	160	μA
		V_{CC+} = 12 V, V_{CC-} = −12 V No load	All inputs at 2 V or 0.8 V		95	160	
I_{CC-}	Supply current from V_{CC-}	V_{CC+} = 5 V, V_{CC-} = −5V, No load	All inputs at 2 V or 0.8 V		−90	−160	μA
		V_{CC+} = 12 V, V_{CC-} = −12 V No load	All inputs at 2 V or 0.8 V		−95	−160	

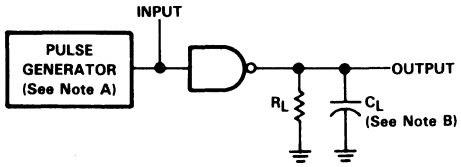
†All typical values are at T_A = 25°C.
‡Not more than one output should be shorted at one time.
NOTE 2: The algebraic convention, in which the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if a −4 V is a maximum, the typical value is a more negative voltage.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C

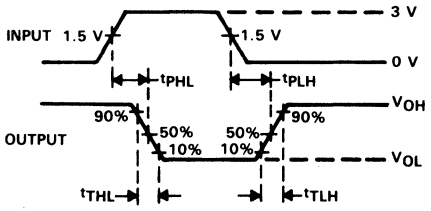
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output†	R_L = 3 kΩ, C_L = 15 pF, See Figure 1			3	μs
t_{PHL}	Propagation delay time, high-to-low level output†				3.5	μs
t_{TLH}	Transition time, low-to-high-level output‡		0.53		3.2	μs
t_{THL}	Transition time, high-to-low-level output‡		0.53		3.2	μs
t_{TLH}	Transition time, low-to-high-level output§	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 1		1.5	3	μs
t_{THL}	Transition time, high-to-low-level output§			1.5	3	μs
SR	Output slew rate§	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF	6	15	30	V/μs

†Measured at the 50% level.
‡Measured between the 10% and 90% points on the output waveform.
§Measured between the 3 V and −3 V points on the output waveform (EIA-232-D conditions), all unused inputs tied either high or low.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_o = 50 Ω, $t_r = t_f \leq 50$ ns.
B. C_L includes probe and jig capacitance.

FIGURE 1. PROPAGATION AND TRANSITION TIMES

TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

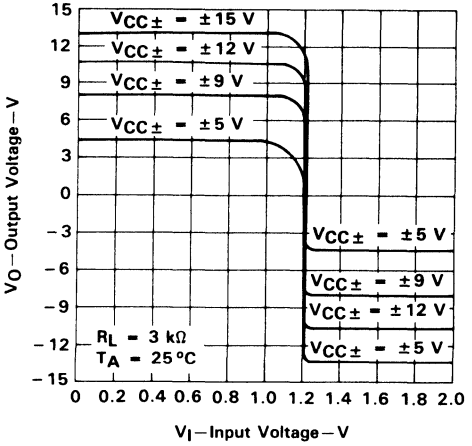


FIGURE 2

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

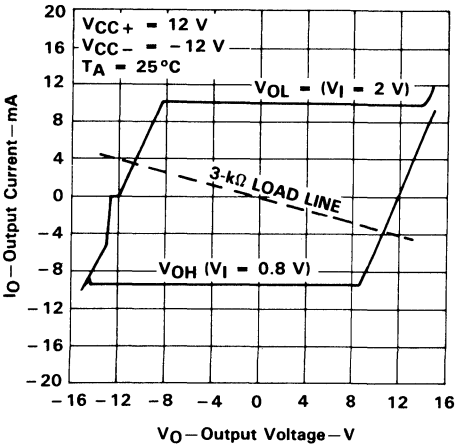


FIGURE 3

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

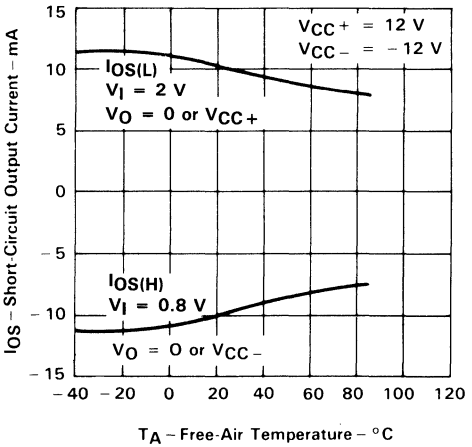


FIGURE 4

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

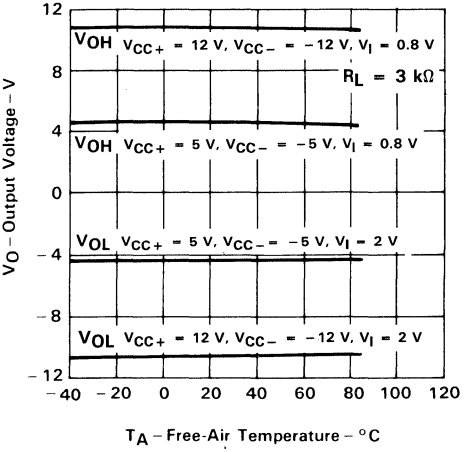


FIGURE 5

TYPICAL CHARACTERISTICS

INPUT CURRENT
vs
FREE-AIR TEMPERATURE

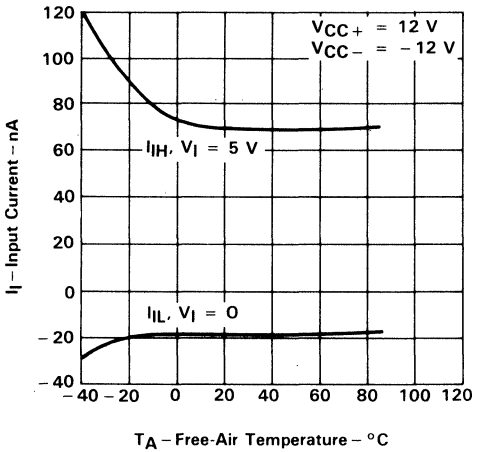


FIGURE 6

POWER-OFF OUTPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

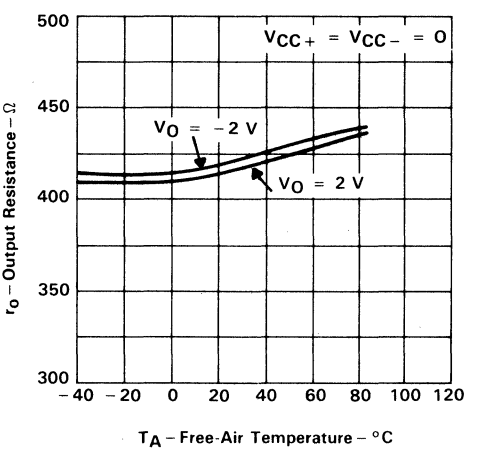


FIGURE 7

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

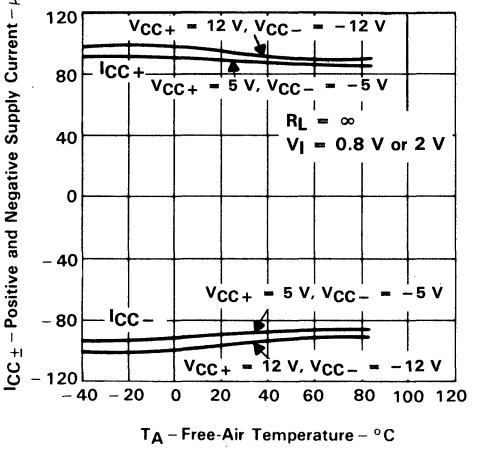


FIGURE 8

OUTPUT SLEW RATE
vs
FREE-AIR TEMPERATURE

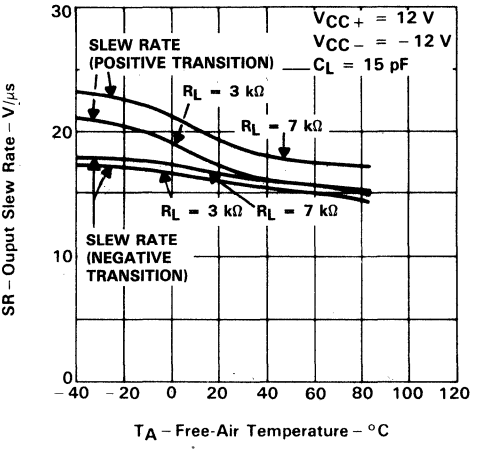


FIGURE 9

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

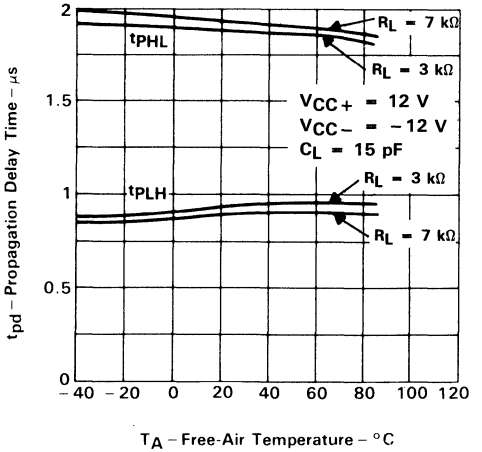


FIGURE 10

OUTPUT TRANSITION TIME
vs
FREE-AIR TEMPERATURE

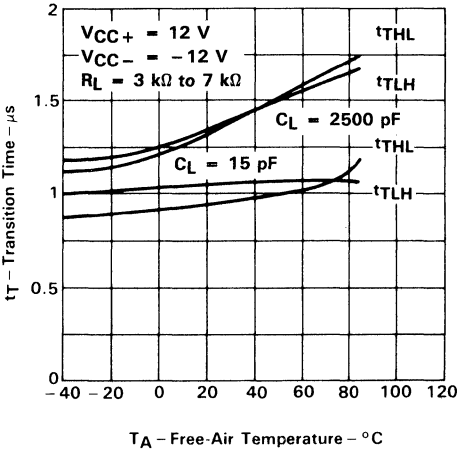


FIGURE 11

APPLICATION INFORMATION

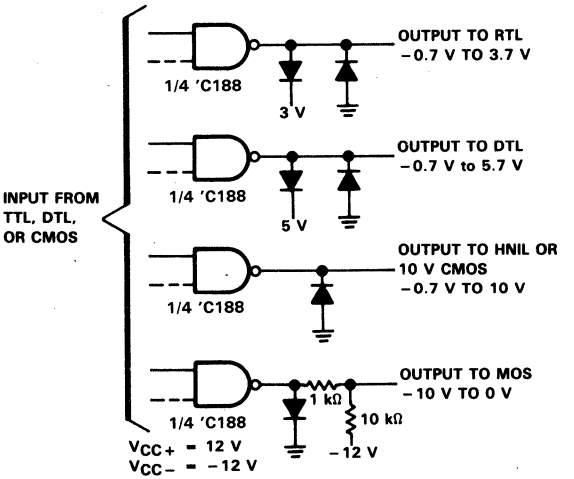
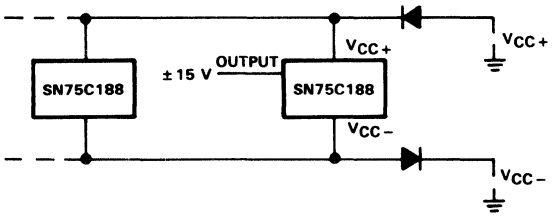


FIGURE 12. LOGIC TRANSLATOR APPLICATIONS

APPLICATION INFORMATION

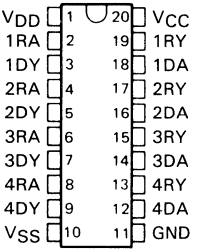


NOTE: External diodes placed in series with the V_{CC+} and V_{CC-} leads will protect the SN75C188 in the fault condition where the device outputs are shorted to ± 15 V and the power supplies are at low voltage and provide low-impedance paths to ground.

FIGURE 13. POWER SUPPLY PROTECTION TO MEET POWER-OFF FAULT CONDITIONS OF STANDARD EIA-232-D

- **Meets Standard EIA-232-D (Revision of RS-232-C)**
- **Very Low Power Consumption . . . 5 mW Typ**
- **Wide Driver Supply Voltage . . . ±4.5 V to ±15 V**
- **Driver Output Slew Rate Limited to 30 V/μs Max**
- **Receiver Input Hysteresis . . . 1000 mV Typ**
- **Push-Pull Receiver Outputs**
- **On-Chip Receiver 1-μs Noise Filter**
- **ESD Protection Exceeds 2000 V Per MIL-Std-833C Method 3015**

DW OR N PACKAGE
(TOP VIEW)



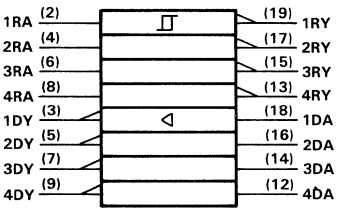
description

The SN65C1154 and SN75C1154 are low-power BI-MOS devices containing 4 independent drivers and receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). This device has been designed to conform to Standards ANSI/EIA-232-D-1986 (which supersedes RS-232-C). The drivers and receivers of the SN65C1154 and SN75C1154 are similar to those of the SN75C188 quadruple driver and SN75C189A quadruple receiver, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/μs and the receivers have filters that reject input noise pulses of shorter than 1 μs. Both these features eliminate the need for external components.

The SN65C1154 and SN75C1154 have been designed using low-power techniques in a BI-MOS technology. In most applications, the receivers contained in these devices interface to single inputs of peripheral devices such as ACEs, UARTs, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN65C1154 and SN75C1154 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

The SN65C1154 is characterized for operation from −40°C to 85°C. The SN75C1154 is characterized for operation from 0°C to 70°C.

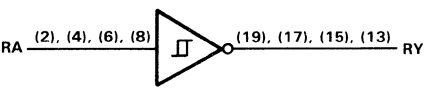
logic symbol†



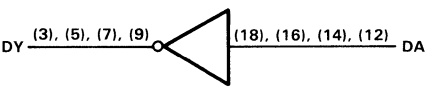
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

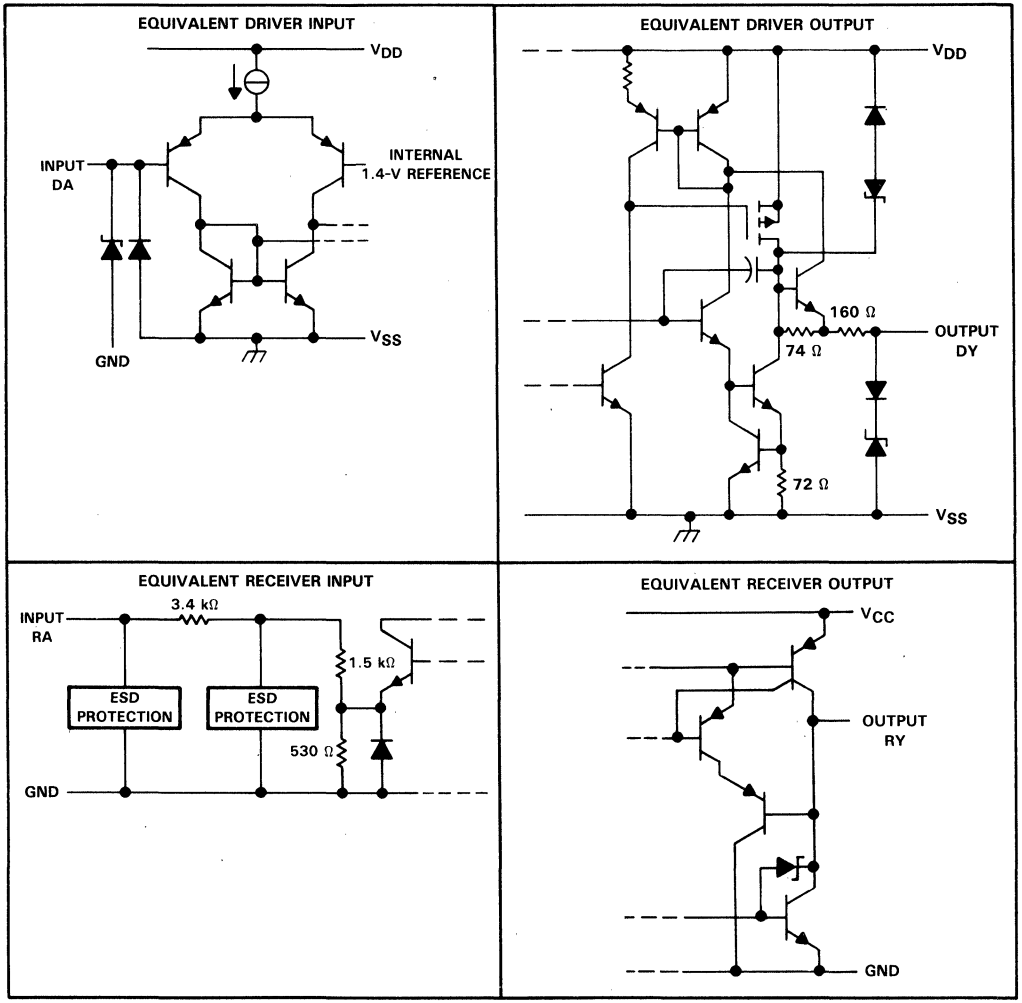
typical of each receiver



typical of each driver



schematics of inputs and outputs



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 15 V
Supply voltage, V_{SS} . . . . . −15 V
Supply voltage, V_{CC} . . . . . 7 V
Input voltage range: Driver . . . . . V_{SS} to V_{DD}
Receiver . . . . . −30 V to 30 V
Output voltage range: Driver . . . . . (V_{SS} − 6 V) to (V_{DD} + 6 V)
Receiver . . . . . −0.3 V to (V_{CC} + 0.3 V)
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN65C1154 . . . . . −40°C to 85°C
SN75C1154 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	585 mW
N	1150 mW	9.2 mW/°C	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	12	15	V
Supply voltage, V_{SS}		−4.5	−12	−15	V
Supply voltage, V_{CC}		4.5	5	6	V
Input voltage, V_I	Driver	$V_{SS}+2$		V_{DD}	V
	Receiver			±25	
High-level input voltage, V_{IH}	Driver	2			V
Low-level input voltage, V_{IL}				0.8	
High-level output current, I_{OH}	Receiver			−1	mA
Low-level output current, I_{OL}				3.2	mA
Operating free-air temperature, T_A	SN65C1154	−40		85	°C
	SN75C1154	0		70	

driver section

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 5 V, V_{SS} = −5 V	4	4.5		V
			V_{DD} = 12 V, V_{SS} = −12 V	10	10.8		
V_{OL}	Low-level output voltage (See Note 2)	V_{IH} = 2 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 5 V, V_{SS} = −5 V		−4.4	−4	V
			V_{DD} = 12 V, V_{SS} = −12 V		−10.7	−10	
I_{IH}	High-level input current	V_I = 5 V, See Figure 2				1	μA
I_{IL}	Low-level input current	V_I = 0, See Figure 2				−1	μA
I_{OSH}	High-level short circuit output current‡	V_I = 0.8 V, V_O = 0 or V_{SS}, See Figure 1		−7.5	−12	−19.5	mA
I_{OSL}	Low-level short circuit output current‡	V_I = 2 V, V_O = 0 or V_{DD}, See Figure 1		7.5	12	19.5	mA
I_{DD}	Supply current from V_{DD}	No load, All inputs at 2 V or 0.8 V	V_{DD} = 5 V, V_{SS} = −5 V		115	250	μA
			V_{DD} = 12 V, V_{SS} = −12 V		115	250	
I_{SS}	Supply current from V_{SS}	No load, All inputs at 2 V or 0.8 V	V_{DD} = 5 V, V_{SS} = −5 V		−115	−250	μA
			V_{DD} = 12 V, V_{SS} = −12 V		−115	−250	
r_o	Output resistance	V_{DD} = V_{SS} = V_{CC} = 0, V_O = −2 V to 2 V, See Note 3		300	400		Ω

†All typical values are at T_A = 25°C.
‡Not more than one output should be shorted at one time.
NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.
3. Test conditions are those specified by EIA-232-D.

switching characteristics at T_A = 25°C, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ±10%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output§	R_L = 3 to 7 kΩ, C_L = 15 pF, See Figure 3		1.2	3	μs
t_{PHL}	Propagation delay time, high-to-low level output§			2.5	3.5	μs
t_{TLH}	Transition time, low-to-high level output¶		0.53	2	3.2	μs
t_{THL}	Transition time, high-to-low level output¶		0.53	2	3.2	μs
t_{TLH}	Transition time, low-to-high level output#	R_L = 3 to 7 kΩ, C_L = 2500 pF, See Figure 3		1	2	μs
t_{THL}	Transition time, high-to-low level output#			1	2	μs
SR	Output slew rate	R_L = 3 to 7 kΩ, C_L = 150 pF, See Figure 3	4	10	30	V/μs

§t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate and are measured at the 50% points.
¶Measured between 10% and 90% points of output waveform.
#Measured between 3 V and −3 V points of output waveform (EIA-232-D conditions) with all unused inputs tied either high or low.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

receiver section

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	See Figure 5		1.7	2.1	2.55	V
V_{T-}	Negative-going threshold voltage	See Figure 5		0.65	1	1.25	V
V_{hys}	Input hysteresis‡			600	1000		mV
V_{OH}	High-level output voltage	V_I = 0.75 V, I_{OH} = −20 μA, See Figure 5 and Note 4		3.5			V
		V_I = 0.75 V, I_{OH} = −1 mA, See Figure 5	V_{CC} = 4.5 V	2.8	4.4		
			V_{CC} = 5 V	3.8	4.9		
			V_{CC} = 5.5 V	4.3	5.4		
V_{OL}	Low-level output voltage	V_I = 3 V, I_{OL} = 3.2 mA, See Figure 5			0.17	0.4	V
I_{IH}	High-level input current	V_I = 25 V		3.6	4.6	8.3	mA
		V_I = 3 V		0.43	0.55	1	
I_{IL}	Low-level input current	V_I = −25 V		−3.6	−5	−8.3	
		V_I = −3 V		−0.43	−0.55	−1	
I_{OSH}	Short-circuit output at high level	V_I = 0.75 V, V_O = 0, See Figure 4			−8	−15	mA
I_{OSL}	Short-circuit output current at low level	V_I = V_{CC}, V_O = V_{CC}, See Figure 4			13	25	mA
I_{CC}	Supply current from V_{CC}	No load, All inputs at 0 or 5 V	V_{DD} = 5 V, V_{SS} = −5 V		400	600	μA
			V_{DD} = 12 V, V_{SS} = −12 V		400	600	

†All typical values are at T_A = 25°C.
‡Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.
NOTE 4: If the inputs are left unconnected, the receiver interprets this as an input low and the receiver outputs will remain in the high state.

switching characteristics at T_A = 25°C, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	C_L = 50 pF, R_L = 5 kΩ, See Figure 6		3	4	μs
t_{PHL}	Propagation delay time, high-to-low level output			3	4	μs
t_{TLH}	Transition time, low-to-high level output§			300	450	ns
t_{THL}	Transition time, high-to-low level output§			100	300	ns
$t_{w(N)}$	Duration of longest pulse rejected as noise¶	C_L = 50 pF, R_L = 5 kΩ	1		4	μs

§Measured between 10% and 90% points of output waveforms.
¶The receiver ignores any positive- or negative-going pulse that is less than the minimum value of $t_{w(N)}$ and accepts any positive- or negative-going pulse greater than the maximum of $t_{w(N)}$.

PARAMETER MEASUREMENT INFORMATION

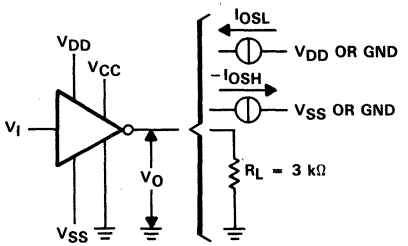


FIGURE 1. DRIVER TEST CIRCUIT, V_{OH}, V_{OL}, I_{OSL}, I_{OSH}

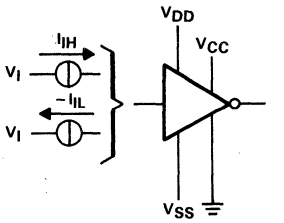
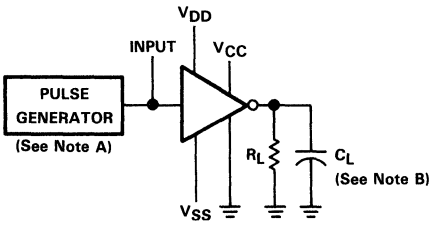
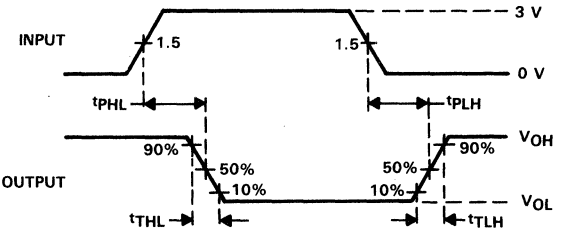


FIGURE 2. DRIVER TEST CIRCUIT, I_{IL}, I_{IH}



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

FIGURE 3. DRIVER PROPAGATION AND TRANSITION TIMES

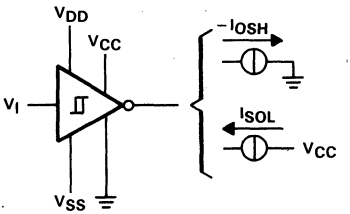


FIGURE 4. RECEIVER TEST CIRCUIT, I_{OSH}, I_{OSL}

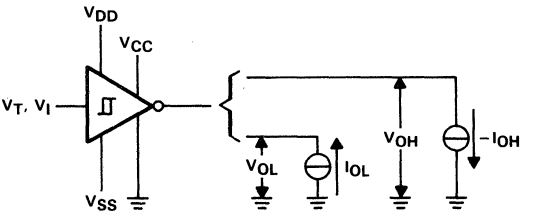
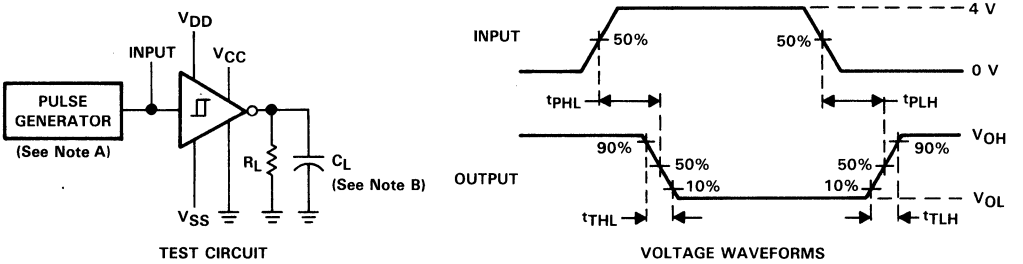


FIGURE 5. RECEIVER TEST CIRCUIT, V_T, V_{OL}, V_{OH}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_o = 50 Ω, t_r = t_f < 50 ns.
B. C_L includes probe and jig capacitance.

FIGURE 6. RECEIVER PROPAGATION AND TRANSITION TIMES

D3425, MAY 1990

- **Meets Standard EIA-232-D (Revision of RS-232-C)**
- **Very Low Power Consumption . . . 5 mW Typ**
- **Wide Driver Supply Voltage . . . ±4.5 V to ±15 V**
- **Driver Output Slew Rate Limited to 30 V/μs Max**
- **Receiver Input Hysteresis . . . 1000 mV Typ**
- **Push-Pull Receiver Outputs**
- **On-Chip Receiver 1-μs Noise Filter**
- **Functionally Interchangeable with Motorola MC145406**
- **ESD Protection Exceeds 2000 V Per MIL-Std-883C Method 3015**

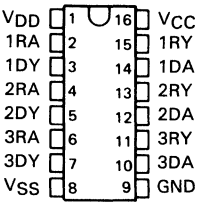
description

The SN65C1406 and SN75C1406 are low-power BI-MOS devices containing three independent drivers and receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). This device is designed to conform to Standards ANSI/EIA-232-D-1986 (which supersedes RS-232-C). The drivers and receivers of the SN65C1406 and SN75C1406 are similar to those of the SN75C188 quadruple driver and SN75C189A quadruple receiver, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/μs and the receivers have filters that reject input noise pulses of shorter than 1 μs. Both these features eliminate the need for external components.

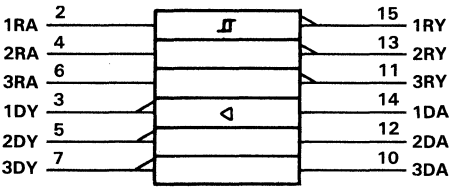
The SN65C1406 and SN75C1406 have been designed using low-power techniques in a BI-MOS technology. In most applications, the receivers contained in these devices interface to single inputs of peripheral devices such as ACEs, UARTs, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN65C1406 and SN75C1406 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

The SN65C1406 is characterized for operation from −40°C to 85°C. The SN75C1406 is characterized for operation from 0°C to 70°C.

D OR N PACKAGE
(TOP VIEW)



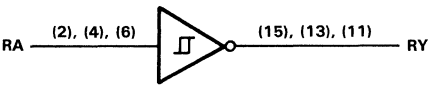
logic symbol†



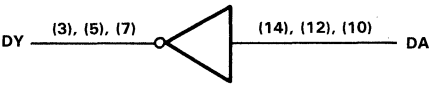
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

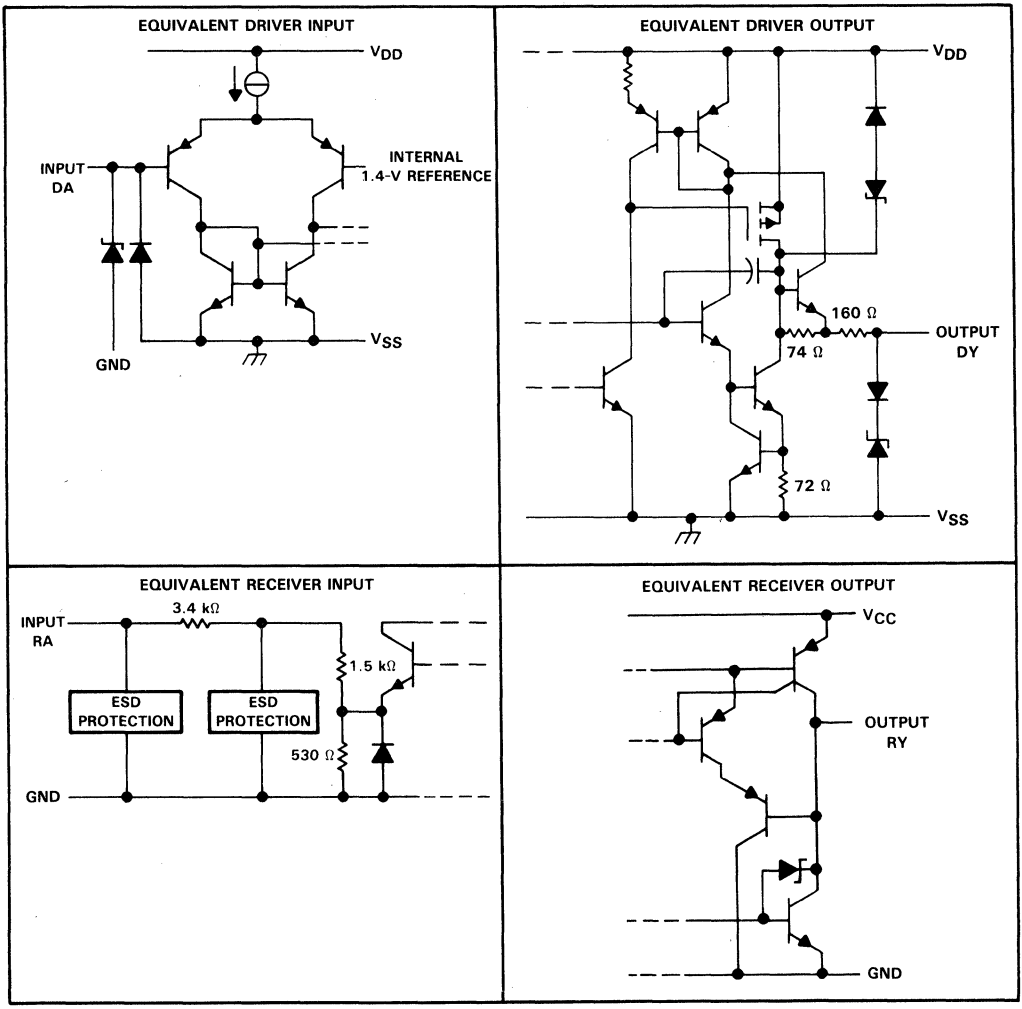
typical of each receiver



typical of each driver



schematics of inputs and outputs



All resistor values shown are nominal.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 15 V
Supply voltage, V_{SS} . . . . . −15 V
Supply voltage, V_{CC} . . . . . 7 V
Input voltage range: Driver . . . . . V_{SS} to V_{DD}
Receiver . . . . . −30 V to 30 V
Output voltage range: Driver . . . . . (V_{SS} − 6 V) to (V_{DD} + 6 V)
Receiver . . . . . −0.3 V to (V_{CC} + 0.3 V)
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN65C1406 . . . . . −40°C to 85°C
SN75C1406 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	12	15	V
Supply voltage, V_{SS}		−4.5	−12	−15	V
Supply voltage, V_{CC}		4.5	5	6	V
Input voltage, V_I	Driver	$V_{SS}+2$		V_{DD}	V
	Receiver			±25	
High-level input voltage, V_{IH}	Driver	2			V
Low-level input voltage, V_{IL}				0.8	
High-level output current, I_{OH}	Receiver			−1	mA
Low-level output current, I_{OL}				3.2	mA
Operating free-air temperature, T_A	SN65C1406	−40		85	°C
	SN75C1406	0		70	

driver section

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 5 V, V_{SS} = −5 V	4	4.5		V
			V_{DD} = 12 V, V_{SS} = −12 V	10	10.8		
V_{OL}	Low-level output voltage (See Note 2)	V_{IH} = 2 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 5 V, V_{SS} = −5 V		−4.4	−4	V
			V_{DD} = 12 V, V_{SS} = −12 V		−10.7	−10	
I_{IH}	High-level input current	V_I = 5 V, See Figure 2				1	μA
I_{IL}	Low-level input current	V_I = 0, See Figure 2				−1	μA
I_{OSH}	High-level short circuit output current‡	V_I = 0.8 V, V_O = 0 or V_{SS}, See Figure 1		−7.5	−12	−19.5	mA
I_{OSL}	Low-level short circuit output current‡	V_I = 2 V, V_O = 0 or V_{DD}, See Figure 1		7.5	12	19.5	mA
I_{DD}	Supply current from V_{DD}	No load, All inputs at 2 V or 0.8 V	V_{DD} = 5 V, V_{SS} = −5 V		115	250	μA
			V_{DD} = 12 V, V_{SS} = −12 V		115	250	
I_{SS}	Supply current from V_{SS}	No load, All inputs at 2 V or 0.8 V	V_{DD} = 5 V, V_{SS} = −5 V		−115	−250	μA
			V_{DD} = 12 V, V_{SS} = −12 V		−115	−250	
r_o	Output resistance	V_{DD} = V_{SS} = V_{CC} = 0, V_O = −2 V to 2 V, See Note 3		300	400		Ω

†All typical values are at T_A = 25°C.
‡Not more than one output should be shorted at one time.
NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.
3. Test conditions are those specified by EIA-232-D.

switching characteristics at T_A = 25°C, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ±10%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output§	R_L = 3 to 7 kΩ, C_L = 15 pF, See Figure 3		1.2	3	μs
t_{PHL}	Propagation delay time, high-to-low level output§			2.5	3.5	μs
t_{TLH}	Transition time, low-to-high level output¶		0.53	2	3.2	μs
t_{THL}	Transition time, high-to-low level output¶		0.53	2	3.2	μs
t_{TLH}	Transition time, low-to-high level output#	R_L = 3 to 7 kΩ, C_L = 2500 pF, See Figure 3		1	2	μs
t_{THL}	Transition time, high-to-low level output#			1	2	μs
SR	Output slew rate	R_L = 3 to 7 kΩ, C_L = 150 pF, See Figure 3	4	10	30	V/μs

§t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate and are measured at the 50% points.
¶Measured between 10% and 90% points of output waveform.
#Measured between 3 V and −3 V points of output waveform (EIA-232-D conditions) with all unused inputs tied either high or low.

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receiver section

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	See Figure 5		1.7	2.1	2.55	V
V_{T-}	Negative-going threshold voltage	See Figure 5		0.65	1	1.25	V
V_{hys}	Input hysteresis‡			600	1000		mV
V_{OH}	High-level output voltage	V_I = 0.75 V, I_{OH} = −20 μA, See Figure 5 and Note 4		3.5			V
		V_I = 0.75 V, I_{OH} = −1 mA, See Figure 5	V_{CC} = 4.5 V	2.8	4.4		
			V_{CC} = 5 V	3.8	4.9		
			V_{CC} = 5.5 V	4.3	5.4		
V_{OL}	Low-level output voltage	V_I = 3 V, I_{OL} = 3.2 mA, See Figure 5			0.17	0.4	V
I_{IH}	High-level input current	V_I = 25 V		3.6	4.6	8.3	mA
		V_I = 3 V		0.43	0.55	1	
I_{IL}	Low-level input current	V_I = −25 V		−3.6	−5	−8.3	
		V_I = −3 V		−0.43	−0.55	−1	
I_{OSH}	Short-circuit output at high level	V_I = 0.75 V, V_O = 0, See Figure 4			−8	−15	mA
I_{OSL}	Short-circuit output current at low level	V_I = V_{CC}, V_O = V_{CC}, See Figure 4			13	25	mA
I_{CC}	Supply current from V_{CC}	No load, All inputs at 0 or 5 V	V_{DD} = 5 V, V_{SS} = −5 V		320	450	μA
			V_{DD} = 12 V, V_{SS} = −12 V		320	450	

†All typical values are at T_A = 25°C.
‡Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.
NOTE 4: If the inputs are left unconnected, the receiver interprets this as an input low and the receiver outputs will remain in the high state.

switching characteristics at T_A = 25°C, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	C_L = 50 pF, R_L = 5 kΩ, See Figure 6		3	4	μs
t_{PHL}	Propagation delay time, high-to-low level output			3	4	μs
t_{TLH}	Transition time, low-to-high level output§			300	450	ns
t_{THL}	Transition time, high-to-low level output§			100	300	ns
$t_{w(N)}$	Duration of longest pulse rejected as noise¶	C_L = 50 pF, R_L = 5 kΩ	1		4	μs

§Measured between 10% and 90% points of output waveforms.
¶The receiver ignores any positive- or negative-going pulse that is less than the minimum value of $t_{w(N)}$ and accepts any positive- or negative-going pulse greater than the maximum of $t_{w(N)}$.

PARAMETER MEASUREMENT INFORMATION

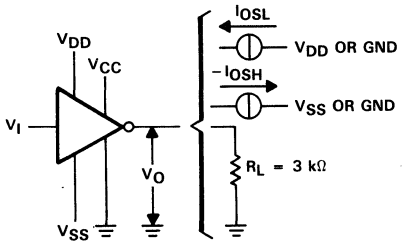


FIGURE 1. DRIVER TEST CIRCUIT, V_{OH}, V_{OL}, I_{OSL}, I_{OSH}

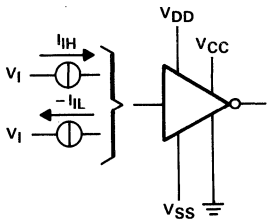
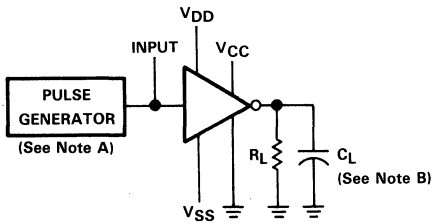
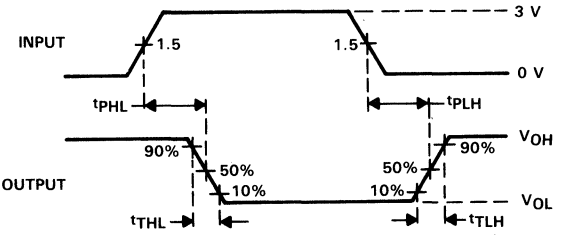


FIGURE 2. DRIVER TEST CIRCUIT, I_{IL}, I_{IH}



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_o = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

FIGURE 3. DRIVER PROPAGATION AND TRANSITION TIMES

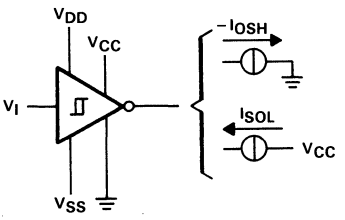


FIGURE 4. RECEIVER TEST CIRCUIT, I_{OSH}, I_{OSL}

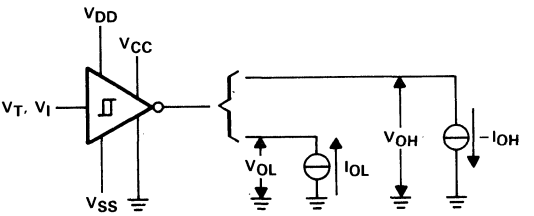


FIGURE 5. RECEIVER TEST CIRCUIT, V_T, V_{OL}, V_{OH}

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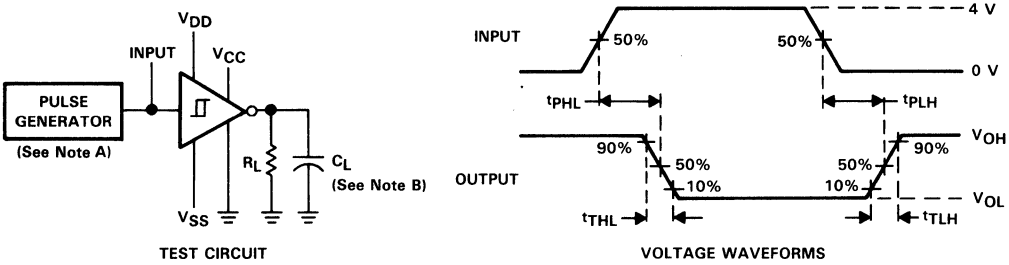
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

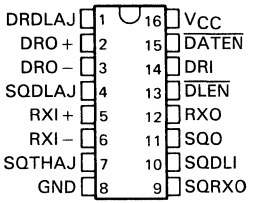
NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_o = 50 Ω, t_r = t_f < 50 ns.
B. C_L includes probe and jig capacitance.

FIGURE 6. RECEIVER PROPAGATION AND TRANSITION TIMES

D2959, JANUARY 1987—REVISED JULY 1990

- IEEE 802.3 1BASE5 Driver and Receiver
- On-Chip Receiver Squelch with Adjustable Threshold
- Adjustable Squelch Delay
- Direct TTL-Level Squelch Output
- Squelch Circuit Allows for External Noise Filtering
- Two Driver-Enable Options
- On-Chip Start-of-Idle Detection and Disable
- Driver Provides 2 V Minimum into a 50-Ω Differential Load to Allow for Use with Doubly-Terminated Lines and Multipoint Architectures
- On-Chip Driver Slew-Rate Control for Very Closely Matched Output Rise and Fall Times

N PACKAGE
(TOP VIEW)



PIN NAME	PIN NUMBER	DESCRIPTION
$\overline{\text{DATEN}}$	15	Driver Data Enable. When low, places driver outputs in an active state. When high, the driver outputs are in a high-impedance state if $\overline{\text{DLEN}}$ is also high.
$\overline{\text{DLEN}}$	13	Driver Delay Enable. When this signal is low and $\overline{\text{DATEN}}$ is high, the driver outputs are active for a period of time set by DRDLAJ after a positive-going transition on DRI. If there is no active data on DRI, the outputs are in a high-impedance state.
DRDLAJ	1	Driver Delay Adjust is a connection for the external R-C combination that determines the duration of the driver output active state after a positive transition on DRI when $\overline{\text{DLEN}}$ is low and $\overline{\text{DATEN}}$ is high.
DRI	14	Driver Data Input
DRO+	2	Noninverting Driver Output
DRO−	3	Inverting Driver Output
GND	8	Ground. Common for all voltages
RXI+	5	Noninverting Receiver Input
RXI−	6	Inverting Receiver Input
RXO	12	Main Receiver Output
SQDLAJ	4	Squelch Delay Adjust is a connection for an external R-C combination that determines the duration of the receiver unsquelch after a negative-going transition on SQDLI.
SQDLI	10	Squelch Delay Input is the input to the one-shot that controls the duration of the receiver unsquelch period. The main receiver output remains unsquelched as long as SQDLI is held high. Timing of the unsquelch period begins on the high-to-low transition of SQDLI.
SQO	11	Squelch Output is high while the receiver is squelched.
SQRXO	9	Squelch Receiver Output is high only when the differential receiver input exceeds the threshold set by SQTHAJ.
SQTHAJ	7	Squelch Receiver Threshold Adjust. The voltage at this input determines the threshold of the squelch receiver in a ratio of −2, SQTHAJ to threshold. If left open, the squelch receiver threshold defaults to −600 mV.
V_{CC}	16	Supply voltage input

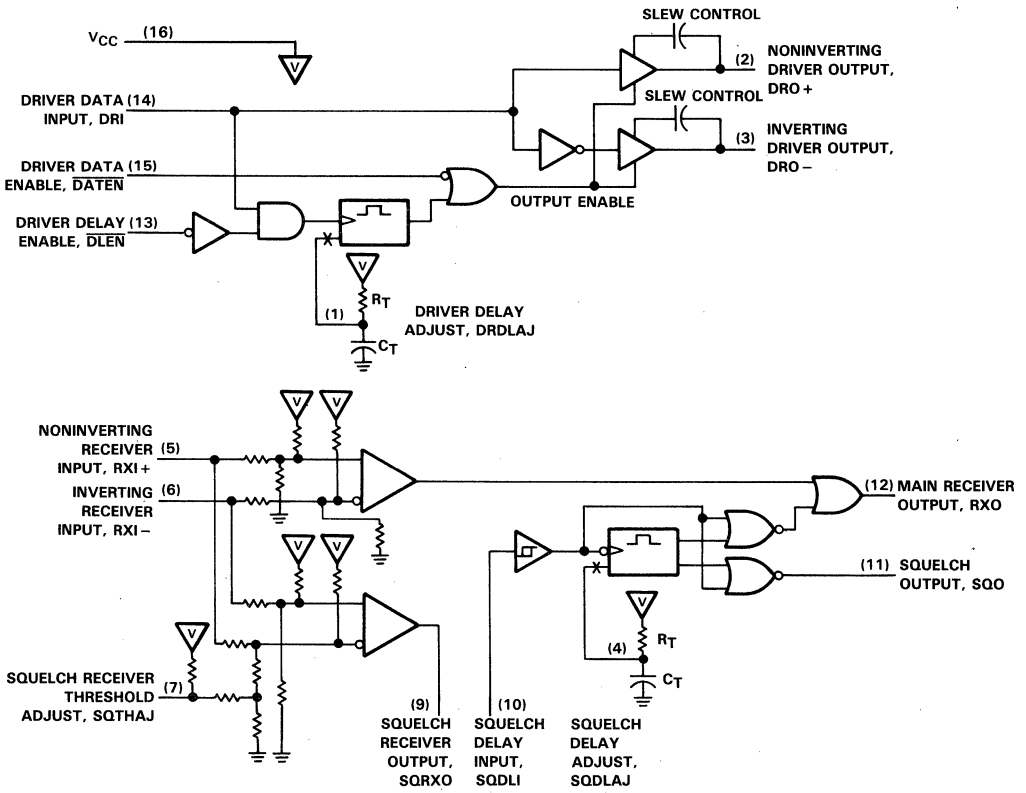
FUNCTION TABLES

DRIVER				
INPUTS			OUTPUTS	
DRI	$\overline{\text{DATEN}}$	$\overline{\text{DLEN}}$	DRO+	DRO−
L	L	X	L	H
H	L	X	H	L
X	H	H	Z	Z
H	H	L	H†	L†
L	H	L	L‡	H‡

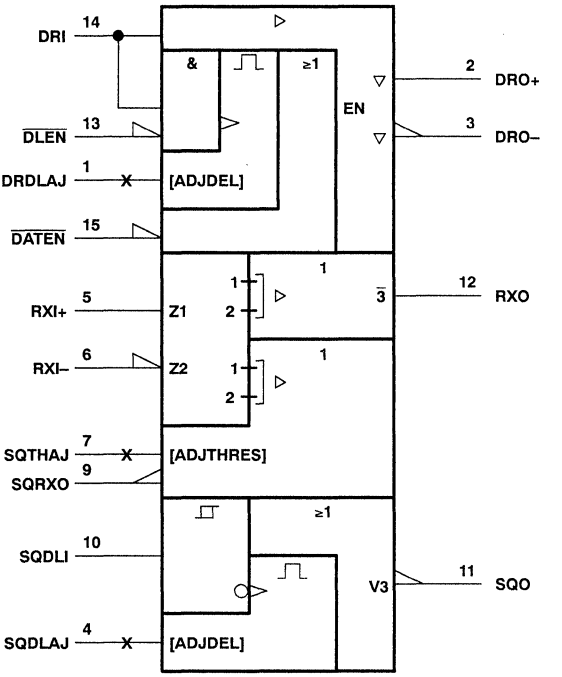
RECEIVER§				
CONDITION	INPUTS		OUTPUTS	
	RXI+	RXI−	RXO	SQO
No active signal¶	X	X	H	H
Active signal¶	L	H	L	L
	H	L	H	L

†This condition is valid during the time period set by Driver Delay Adjust following a rising transition on Driver In. Following this, if no subsequent positive transition occurs on Driver In, the outputs will go to the high impedance state.
‡This condition is valid if it occurs within the enable time set by Driver Delay Adjust after a rising transition on Driver In. Otherwise the outputs will be in the high-impedance state.
§Pins 9 and 10 are tied together.
¶An active signal is one that has an amplitude greater than the threshold level set by Squelch Threshold Adjust.

logic diagram (positive logic)



logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN75061 is a single-channel driver/receiver pair designed for use in IEEE 802.3, 1BASE5 applications as well as other general data communications circuits. The SN75061 offers the system designer both a driver and a receiver that are easily configured for use with a variety of controllers and data encoder/decoders.

The receiver features a full analog squelch circuit with an adjustable threshold and a programmable squelch delay. Internal nodes of the squelch circuitry are brought out to external connections to allow for the insertion of noise filtering circuitry of the designer's choice.

As with the receiver, the driver offers the user a variety of implementation options. Driver enabling may be controlled directly by an external logic input, or by use of an on-chip one-shot that is retriggered as long as data is being sent to the driver. The driver will then automatically go to the high-impedance state when end-of-packet occurs. The driver features internal slew-rate control for optimal matching of rise and fall times allowing for reduction of driver-induced jitter.

receiver

The SN75061 receiver implements full analog squelch functions by integrating both a separate, parallel squelch receiver with an externally programmable threshold, and a programmable one-shot. The output of the squelch receiver and the input to the high-level dc-triggered one-shot are brought out to external connections. These pins can be shorted for direct implementation, or used for the insertion of noise-filtering

circuitry of the implementer's design. The receiver one-shot can be effectively bypassed by applying a high logic level to Squelch Delay In. The squelch threshold may be set externally by applying an external voltage set to a level that is −2 times the desired threshold voltage. If Squelch Threshold Adjust is left open, the squelch receiver will default to its internal preset value of −600 mV. The receiver also outputs a high logic "squelch" signal when there is no active data present at the receiver inputs. When no data is present on the transmission line, the receiver output assumes a high level. The "unsquelch" duration is set externally with an R-C combination at Squelch Delay Adjust.

driver

The driver offers the user a variety of implementation options. Driver enabling may be controlled directly by an active-low external logic input on Data Enable, or by use of another on-chip one-shot that retriggers with positive-going transitions on the driver input line. If no positive transition occurs within the pulse duration set by an external R-C combination, the one-shot times out and the driver is automatically put into a high-impedance state. When operating in the delay-enable mode, the 2-bit-time high-level start-of-idle pulse prescribed by IEEE 802.3 1BASE5 causes the one-shot to time out and automatically place the driver outputs in the high-impedance state. This delay time is also adjustable for use in other applications. The driver implements an output slew-rate control that is internally set for nominally 40 mV/ns. (This is roughly a 100-ns peak-to-peak differential transition time.) The driver outputs are capable of driving a 50-Ω differential load with a minimum output level of 2 V. Short-circuit output current is greater than 100 mA.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage (any logic input) . . . . . 7 V
Receiver differential input voltage . . . . . ±25 V
Receiver input voltage . . . . . ±15 V
Driver output voltage . . . . . −0.5 V to 15 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1) . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: For operation above 25°C free-air temperature, derate to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Driver high-level input voltage, V_{IH}	2			V
Driver low-level input voltage, V_{IL}			0.8	V
Driver high-level output current, I_{OH}			−150	mA
Driver low-level output current, I_{OL}			150	mA
Receiver common-mode input voltage, V_{IC} (see Note 2)	−2.5		5	V
External timing resistance, R_{ext}	5		260	kΩ
External timing capacitance, C_{ext}	No restriction			
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage V_{IC} and threshold levels V_{TH} and V_{TL}.

electrical characteristics over recommended operating free-air and supply voltage range (unless otherwise noted)

driver

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OD}	Differential-output voltage	R_L = 50 Ω		2	2.4	3.3	V
		R_L = 115 Ω				3.65	
ΔV_{OD}	Change in differential-output voltage for a change in logic input state					50	mV
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.5 V				−35	μA
I_{OS}	Short-circuit output current	V_O = 0 or 6 V,	V_I = 0.8 V or 2.5 V	±100		±300	mA
I_{OZ}	High-impedance output current	V_{CC} = 5.25 V	V_{OC} = 10 V			100	μA
			V_{OC} = 0			−100	

receiver

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage, squelch delay		I_I = −18 mA				−1.5	V
V_{TH}	Differential-input high-threshold voltage		V_O = 2.7 V,	I_O = −0.4 mA			50	mV
V_{TL}	Differential-input low-threshold voltage (see Note 2)		V_O = 0.5 V,	I_O = 16 mA	−50			mV
V_{hys}	Hysteresis (V_{TH} − V_{TL})					50		mV
V_{IC}	Common-mode input voltage						5	V
V_{OH}	High-level output voltage	RXO	V_{CC} = 4.75 V, SQDLAJ at 0.8 V	I_{OH} = −400 μA,	2.7			V
		SQO			2.7	3.5		
		SQRXO	V_{CC} = 4.75 V, $V_{ID(RXI)}$ = −0.7 V,	I_{OH} = −20 μA, SQDLAJ open	2.7	4.65		
V_{OL}	Low-level output voltage	RXO	V_{CC} = 4.75 V, SQDLAJ at 2 V	I_{OL} = 8 mA			0.45	V
				I_{OL} = 16 mA			0.5	
		SQO		I_{OL} = 8 mA		0.35	0.5	
		SQRXO	V_{CC} = 4.75 V, $V_{ID(RXI)}$ = 50 mV	I_{OL} = 8 mA			0.45	
				I_{OL} = 16 mA			0.5	
I_{IH}	High-level input current	SQDLI	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current		V_I = 0.5 V				−35	μA
I_{OS}	Short-circuit output current	RXO	V_{CC} = 5.25 V,	V_O = 0	−15		−85	mA
		SQO			−15		−100	
		SQRXO	V_{CC} = 5 V,	V_O = 0	−0.8	−1	−1.2	
r_I	Input resistance					10		kΩ
$V_{TL(sq)}$	Squelch preset threshold voltage		V_{CC} = 5 V, SQTHAJ OPEN,	V_{IC} = 1.5 V to 3.5 V	−525	−600	−675	mV
				V_{IC} = −2.5 V to 1.5 V or 3.5 V to 5 V	−500		−700	mV
	Ratio of Squelch Threshold Adjust input voltage to actual squelch threshold voltage		SQTHAJ at 200 mV to 4 V		−1.9		−2.1	

driver and receiver

I_{CC}	Supply current	V_{CC} = 5.25 V, No loads	Driver outputs disabled,	70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: The algebraic convention, in which the less-positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage V_{IC} and threshold levels V_{TH} and V_{TL}.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

driver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Differential-output slew rate	V_O = −2 V to 2 V, R_L = 100 Ω (differential), See Figure 1	28	40	52	mV/ns
t_{DD}	Differential-output delay time (t_{DD+} and t_{DD-})	C_1 = 15 pF, R_L = 100 Ω (differential), See Figure 2			160	ns
$t_{DD+} - t_{DD-}$	Differential-output delay time difference	R_L = 100 Ω (differential), See Figure 2			5	ns
t_{PHZ}	Disable time from $\overline{DATEN}$	See Figures 3, 4, and 5			220	ns
t_{PLZ}					300	ns
t_{PZH}	Enable time from $\overline{DATEN}$				220	ns
t_{PZL}					290	ns
t_{PZH}	Enable time from $\overline{DLEN}$				250	ns
$t_{w(en)}$	Enable duration time (with $\overline{DLEN}$ low)	C_{ext} = 100 pF, R_{ext} = 62 kΩ, See Figure 6	2	2.5	3	μs

receiver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{en(RX)}$	Receiver enable time	Squelch off, See Figure 7		117		ns
t_{PLH}	Propagation delay time, low-to-high-level output	Squelch off, See Figure 8		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	Squelch off, See Figure 8		22	35	ns
t_{unsq}	Unsquelch duration time	C_{ext} = 50 pF, R_{ext} = 51 kΩ, See Figure 9	1	1.2	1.45	μs
		C_{ext} = 15 pF, R_{ext} = 6.8 kΩ, See Figure 9			180	ns

PARAMETER MEASUREMENT INFORMATION

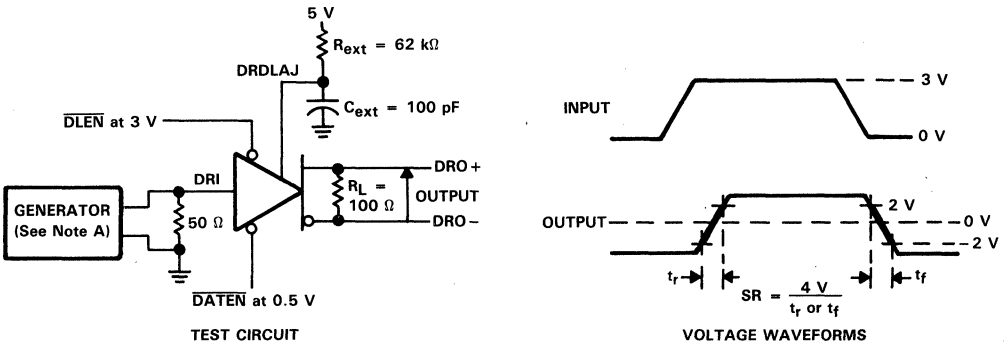


FIGURE 1. DRIVER SLEW RATE MEASUREMENTS

NOTE A: The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, Duty Cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.

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PARAMETER MEASUREMENT INFORMATION

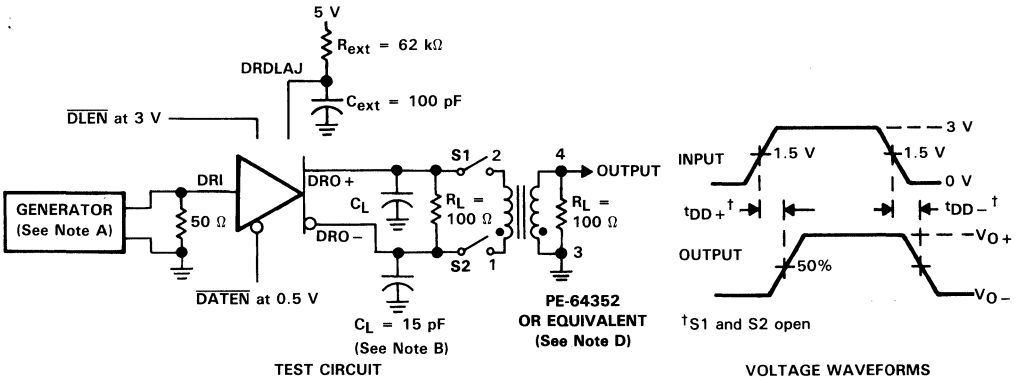


FIGURE 2. DRIVER DIFFERENTIAL DELAY TIMES

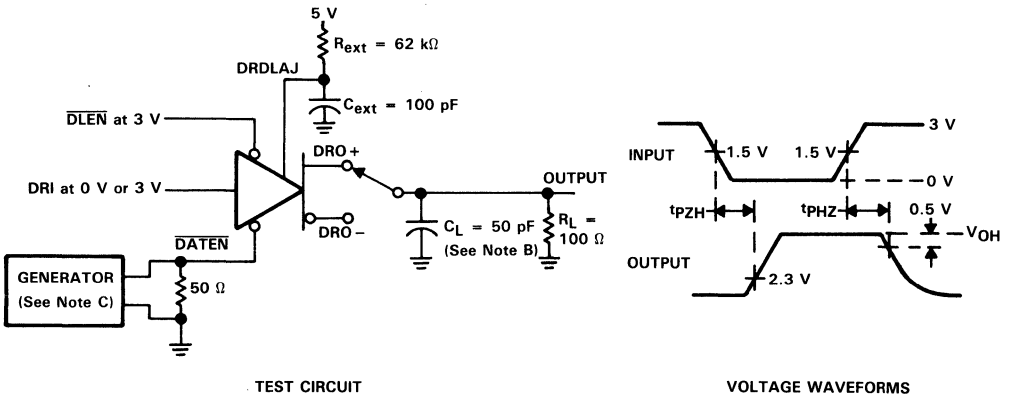
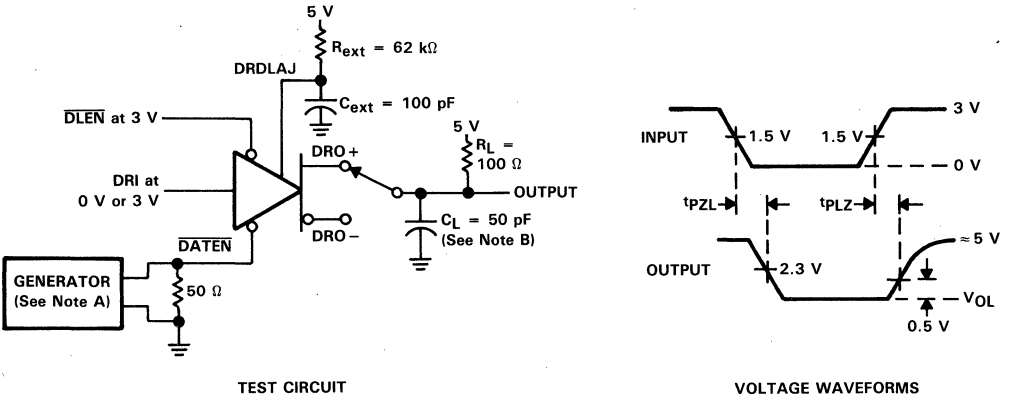


FIGURE 3. DRIVER ENABLE AND DISABLE TIMES

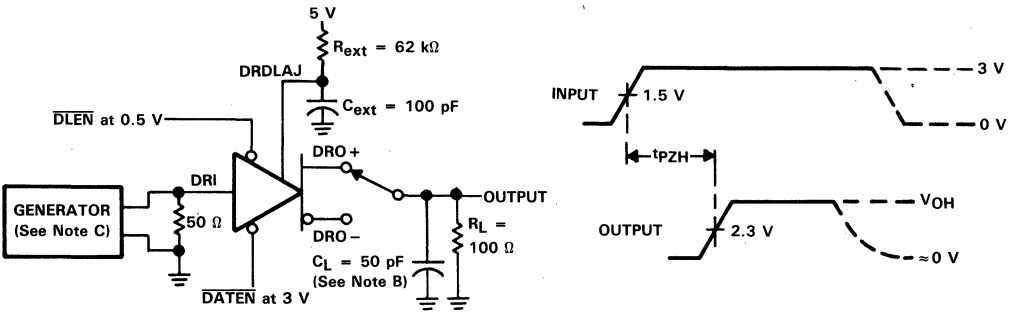
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, Duty Cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, Duty Cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6ns, Z_{out} = 50 Ω.
D. When measuring differential-output delay time difference, switches S1 and S2 are closed. (Isolation transformer from Pulse Engineering P/N PE-64352).

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

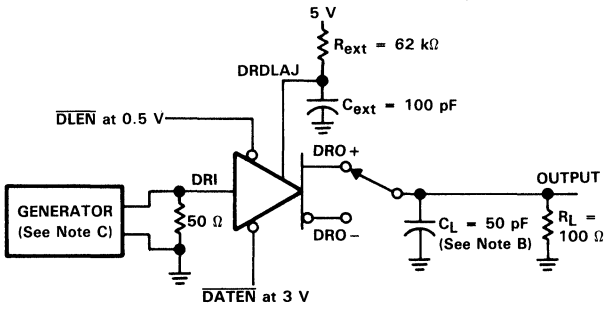


TEST CIRCUIT VOLTAGE WAVEFORMS

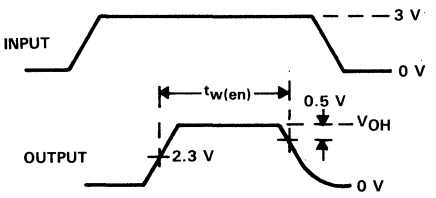
FIGURE 5. ENABLE TIMES FROM DELAY ENABLE

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 200 kHz, Duty Cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, Duty Cycle ≤ 50%, t_r ≤6 ns, t_f≤ 6 ns, Z_{out} = 50 Ω.

PARAMETER MEASUREMENT INFORMATION

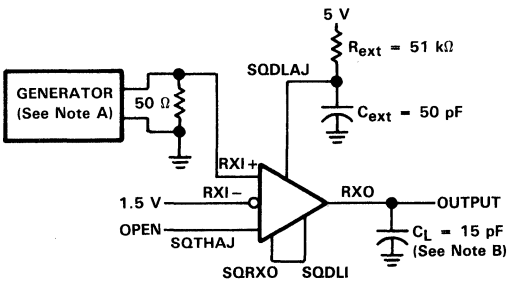


TEST CIRCUIT

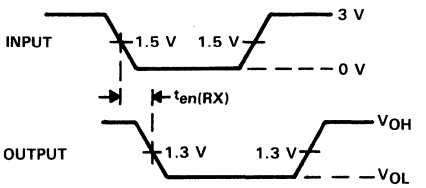


VOLTAGE WAVEFORMS

FIGURE 6. ENABLE DURATION TIME WITH DELAY ENABLE LOW



TEST CIRCUIT

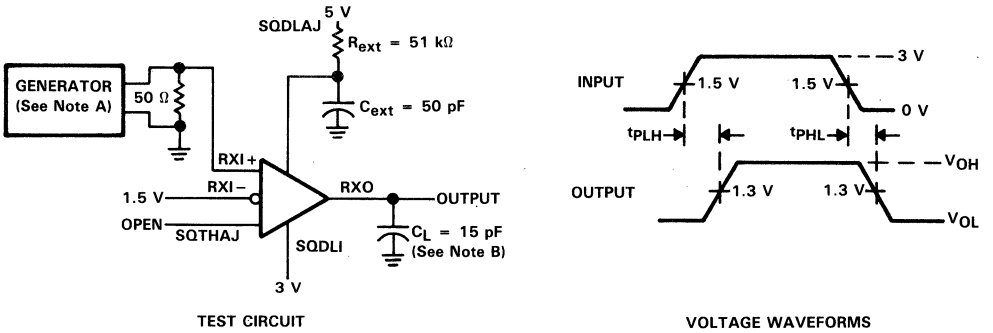


VOLTAGE WAVEFORMS

FIGURE 7. RECEIVER ENABLE (UNSQUELCH) TIMES

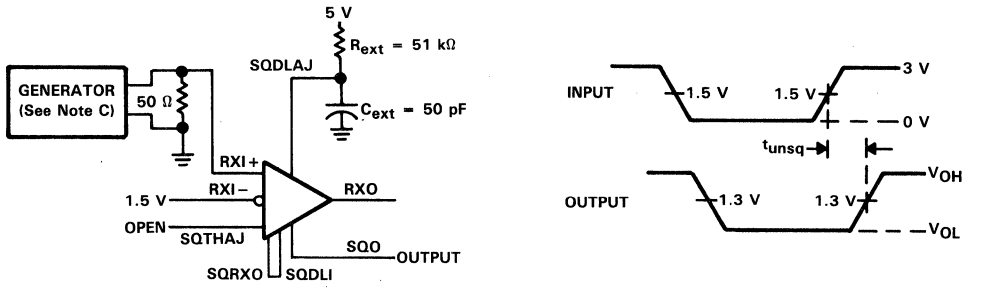
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, Duty Cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 200 kHz, Duty Cycle ≤ 50%, t_r ≤6 ns, t_f≤ 6 ns, Z_{out} = 50 Ω.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 8. RECEIVER PROPAGATION DELAY TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

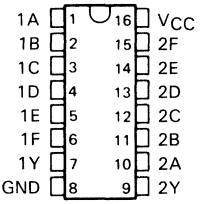
FIGURE 9. UNSQUELCH DURATION TIME

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, Duty Cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 100 kHz, Duty Cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.

D1322, SEPTEMBER 1973—REVISED SEPTEMBER 1986

- **Meets IBM System 360 Input/Output Interface Specifications**
- **Operates from Single 5-V Supply**
- **TTL Compatible**
- **3.11-V Output at I_{OH} = −59.3 mA**
- **Uncommitted Emitter-Follower Output Structure for Party-Line Operation**
- **Short-Circuit Protection**
- **AND-OR Logic Configuration**
- **Designed for Use With Triple Line Receiver SN75124**
- **Designed to Be Interchangeable With Signetics N8T23**

D, J, OR N PACKAGE
(TOP VIEW)



description

The SN75123 dual line driver is specifically designed to meet the input/output interface specifications for IBM System 360. It is also compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower outputs of the SN75123 will drive terminated lines such as coaxial cable or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 1.5 V. All the inputs are in conventional TTL configuration and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line.

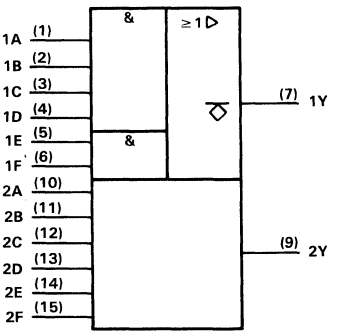
The SN75123 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All other input combinations						L

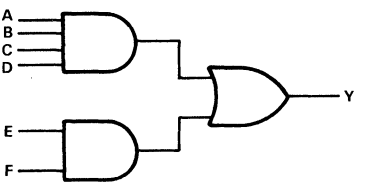
H = high level
L = low level
X = irrelevant

logic symbol†

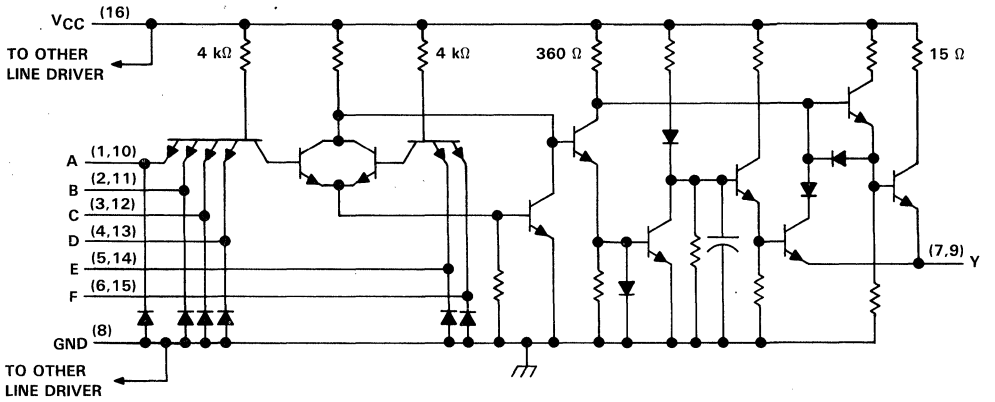


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each driver (positive logic)



schematic (each driver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Output voltage . . . . . 7 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
D package . . . . . 950 mW
J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the D package to 608 mW at 70°C at the rate of 7.6 mW/°C, the J package to 656 mW at 70°C at the rate of 8.2 mW/°C, and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75123 chips are glass mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−100	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics, V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 5 V,	I_I = −12 mA			−1.5	V
$V_{(BR)I}$	Input breakdown voltage	V_{CC} = 5 V,	I_I = 10 mA		5.5		V
V_{OH}	High-level output voltage	V_{CC} = 5 V,	V_{IH} = 2 V,	T_A = 25°C	3.11		V
		I_{OH} = −59.3 mA,	See Note 3,	T_A = 0°C to 70°C	2.9		
I_{OH}	High-level output current	V_{CC} = 5 V, T_A = 25°C,	V_{IH} = 4.5 V, See Note 3	V_{OH} = 2 V,	−100	−250	mA
V_{OL}	Low-level output voltage	V_{IL} = 0.8 V,	I_{OL} = −240 μA, See Note 3			0.15	V
$I_{O(off)}$	Off-state output current	V_{CC} = 0,	V_O = 3 V			40	μA
I_{IH}	High-level input current	V_I = 4.5 V				40	μA
I_{IL}	Low-level input current	V_I = 0.4 V			−0.1	−1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = 5 V,	T_A = 25°C			−30	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V, Outputs open	All inputs at 2 V,			28	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V, Outputs open	All inputs at 0.8 V,			60	mA

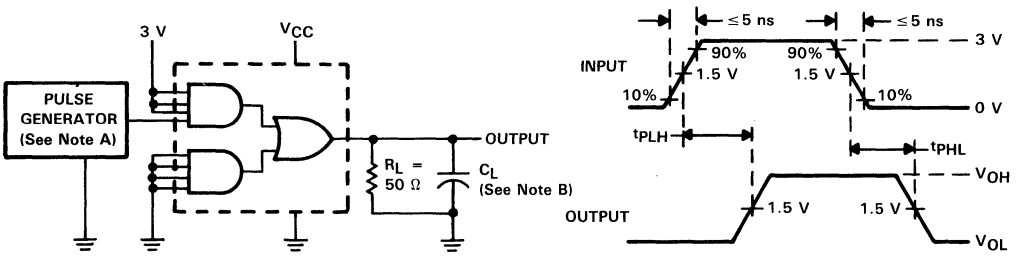
†Not more than one output should be shorted at a time.

NOTE 3: The output voltage and current limits are valid for any appropriate combination of high and low inputs specified by the function table for the desired output.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 50 Ω, C_L = 15 pF, See Figure 1		12	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	20	
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 50 Ω, C_L = 100 pF, See Figure 1		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			15	25	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $Z_O \approx 50\ \Omega$; t_W = 200 ns, duty cycle = 50%.

B. C_L includes probe and jig capacitance.

FIGURE 1. SN75123 SWITCHING TIMES

TYPICAL CHARACTERISTICS

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

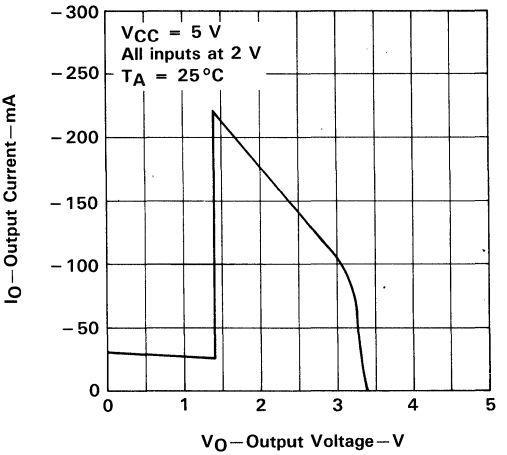


FIGURE 2

APPLICATION INFORMATION

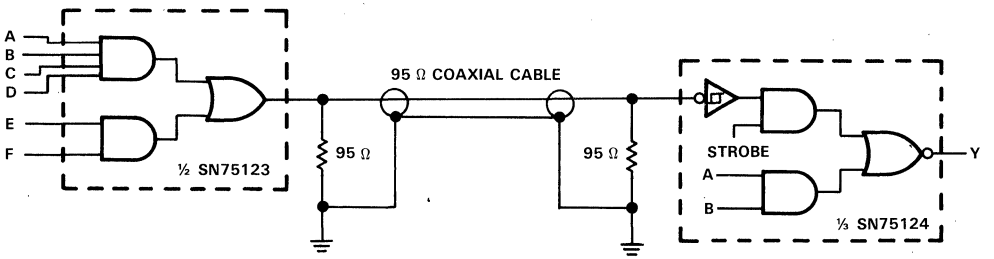
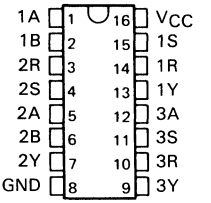


FIGURE 3. UNBALANCED LINE COMMUNICATION USING '123 AND '124

D1322, SEPTEMBER 1973—REVISED SEPTEMBER 1989

- **Meets IBM System 360 Input/Output Interface Specifications**
- **Operates from Single 5-V Supply**
- **TTL Compatible**
- **Built-In Input Threshold Hysteresis**
- **High Speed . . . Typical Propagation Delay Time = 20 ns**
- **Independent Channel Strobes**
- **Input Gating Increases Application Flexibility**
- **Designed for Use with Dual Line Driver SN75123**
- **Designed to Be Interchangeable with Signetics N8T24**

D, J, OR N PACKAGE
(TOP VIEW)



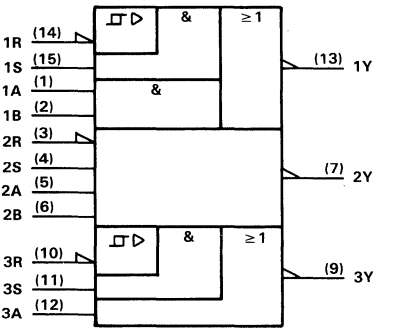
description

The SN75124 triple line receiver is specifically designed to meet the input/output interface specifications for IBM System 360. It is also compatible with standard TTL logic and supply voltage levels.

The SN75124 has receiver inputs with built-in hysteresis to provide increased noise margin for single-ended systems. An open line will affect the receiver input as would a low-level input voltage and the receiver input can withstand a level of −0.15 V with power on or off. The other inputs are in TTL configuration. The S input must be high to enable the receiver input. Two of the line receivers have A and B inputs that, if both are high, will hold the output low. The third receiver has only an A input that, if high, will hold the output low.

The SN75124 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS				OUTPUT
A	B‡	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

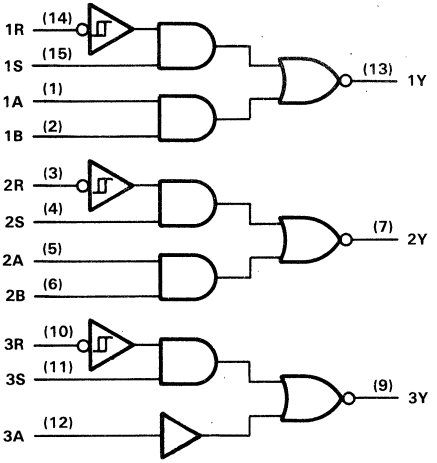
‡B input and last two lines of the function table are applicable to receivers 1 and 2 only.

AVAILABLE OPTIONS

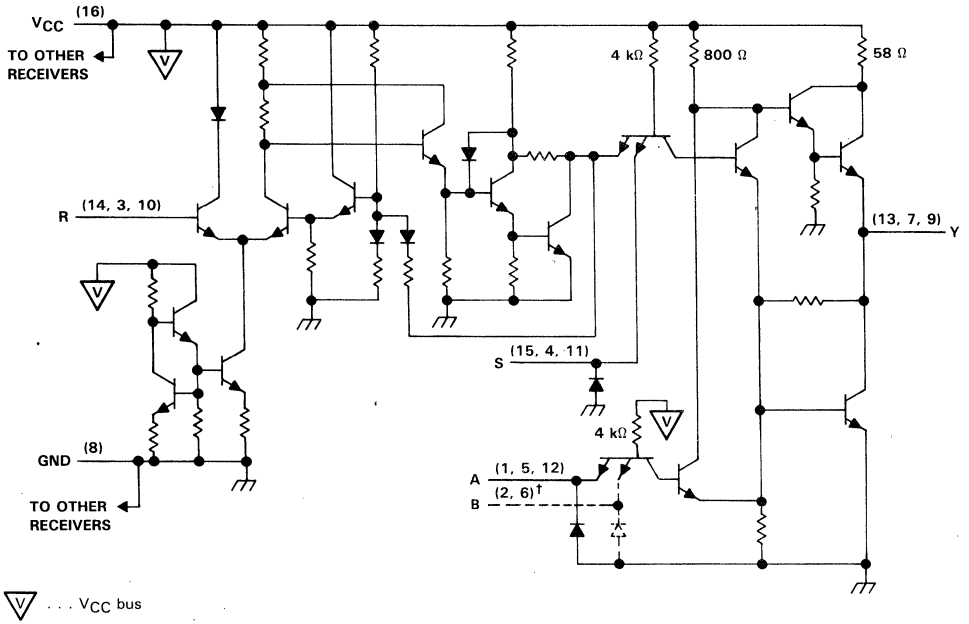
T_A	PACKAGE		
	SMALL OUTLINE (D)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	SN75124D	SN75124J	SN75124N

The D package is available taped and reeled. Add the suffix R to the device type (i.e., SN75124DR).

logic diagram (positive logic)



schematic (each receiver)



†B input is provided on receivers 1 and 2 only.
Resistor values shown are nominal.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: R input with V_{CC} applied . . . . . 7 V
R input with V_{CC} not applied . . . . . 6 V
A, B, or S input . . . . . 5.5 V
Output voltage . . . . . 7 V
Output current . . . . . ±100 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	A, B, or S	2			V
	R	1.7			
Low-level input voltage, V_{IL}	A, B, or S			0.8	V
	R			0.7	
High-level output current, I_{OH}				−800	μA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A		0		70	°C

electrical characteristics, V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 70°C (unless otherwise noted)

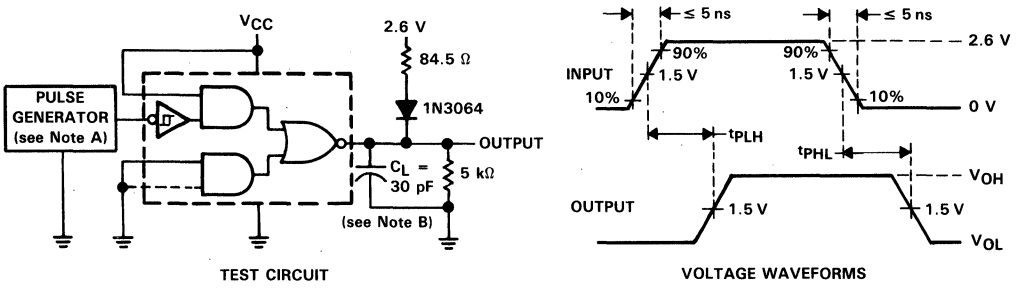
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	R	V_{CC} = 5 V,	T_A = 25°C	0.2	0.5		V
V_{IK}	Input clamp voltage	A,B, or S	V_{CC} = 5 V,	I_I = −12 mA			−1.5	V
$V_{(BR)I}$	Input breakdown voltage	A,B, or S	V_{CC} = 5 V,	I_I = 10 mA	5.5			V
V_{OH}	High-level output voltage		V_{IH} = V_{IH} min, I_{OH} = −800 μA,	V_{IL} = V_{IL} max, See Note 2	2.6			V
V_{OL}	Low-level output voltage		V_{IH} = V_{IH} min, I_{OL} = 16 mA,	V_{IL} = V_{IL} max, See Note 2			0.4	V
I_I	Input current at maximum input voltage	R	V_I = 7 V				5	mA
			V_I = 6 V,	V_{CC} = 0			5	
I_{IH}	High-level input current	A,B, or S	V_I = 4.5 V				40	μA
		R	V_I = 3.11 V				170	
I_{IL}	Low-level input current	A,B, or S	V_I = 0.4 V,	V_{IR} = 0.8 V	−0.1		−1.6	mA
I_{OS}	Short-circuit output current†		V_{CC} = 5 V,	T_A = 25°C	−50		−100	mA
I_{CC}	Supply current		All inputs = 0.8 V				72	mA
			All inputs = 2 V				100	

†Typical value is at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTE 2: The output voltage and current limits are characterized for any appropriate combination of high and low inputs specified by the function table for the desired output.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from R input	See Figure 1		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from R input			20	30	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$, PRR ≤ 5 MHz, duty cycle = 50%.
B. C_L includes probe and jig capacitance.

FIGURE 1. SN75124 SWITCHING TIMES

TYPICAL CHARACTERISTICS

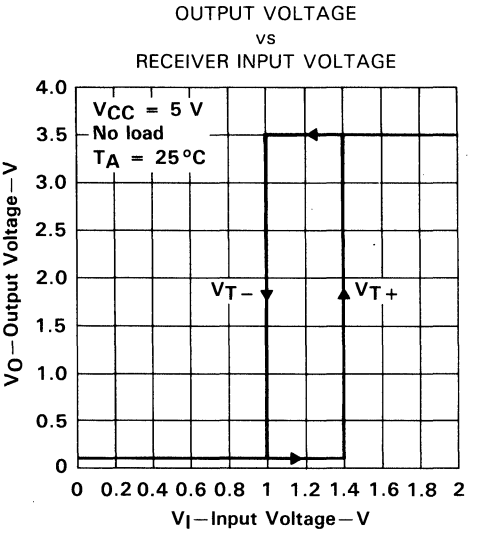


FIGURE 2

TYPICAL APPLICATION DATA

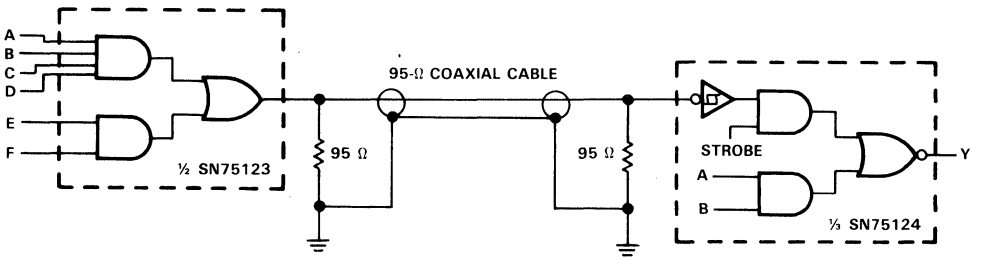
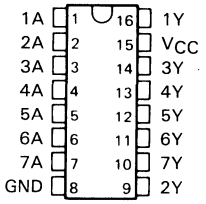


FIGURE 3. UNBALANCED LINE COMMUNICATION USING SN75123 AND SN75124

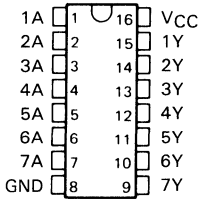
D2239, JANUARY 1977—REVISED SEPTEMBER 1986

- **Meets IBM 360/370 I/O Specification**
- **Input Resistance . . . 7 kΩ to 20 kΩ**
- **Output Compatible with TTL**
- **Schottky-Clamped Transistors**
- **Operates from Single 5-V Supply**
- **High Speed . . . Low Propagation Delay**
- **Ratio Specification for Propagation Delay Time, Low-to-High/High-to-Low**
- **Seven Channels in One 16-Pin Package**
- **Standard V_{CC} and Ground Positioning on SN75127**

SN75125 . . . D, J, OR N PACKAGE
(TOP VIEW)



SN75127 . . . D, J, OR N PACKAGE
(TOP VIEW)



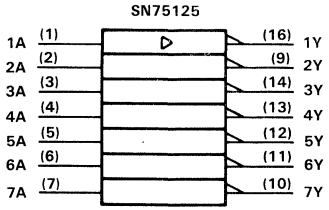
description

The SN75125 and SN75127 are monolithic seven-channel line receivers designed to satisfy the requirements of the IBM System 360/370 input/output interface specifications. Special low-power design and Schottky-clamped transistors allow for low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs.

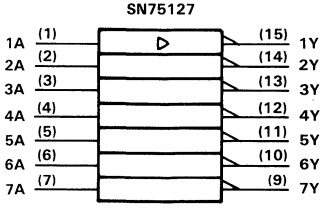
The SN75125 and SN75127 are characterized for operation from 0°C to 70°C.

logic symbols†

SN75125

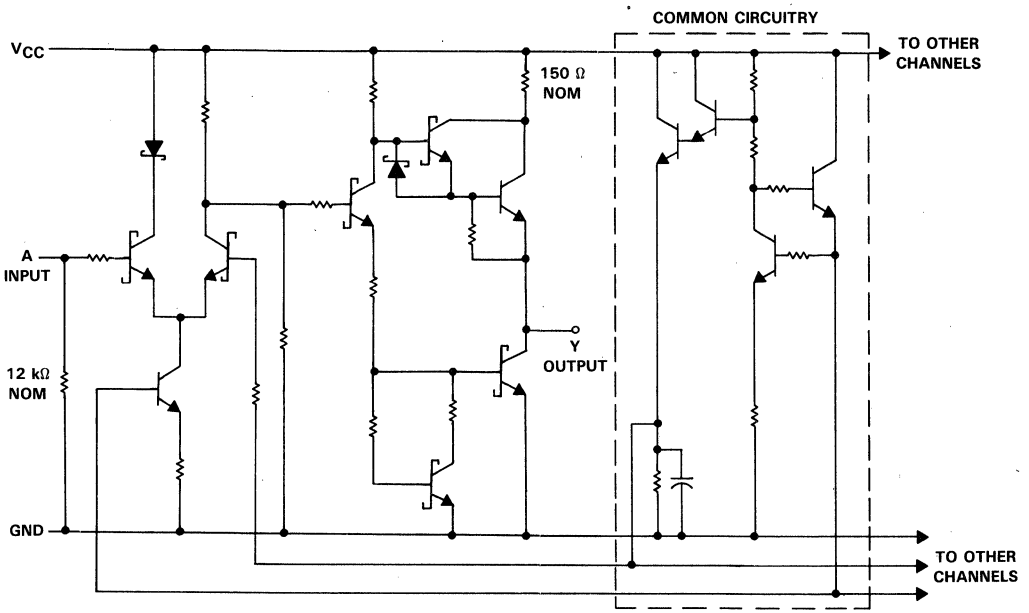


SN75127



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publicaiton 617-12.

schematic (each receiver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage range: SN75125 . . . . . −0.15 V to 7 V
SN75127 . . . . . −2 V to 7 V
Continuous total power dissipation (see Note 2) . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. In the J package, SN75125 and SN75127 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH}	1.7			V
Low-level input voltage, V_{IL}			0.7	V
High-level output current, I_{OH}			−0.4	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

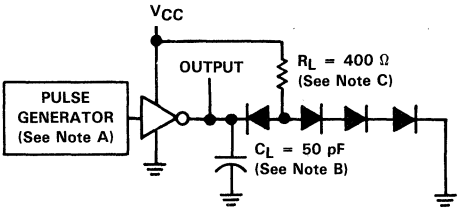
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V, V_{IL} = 0.7 V, I_{OH} = −0.4 mA	2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V, V_{IH} = 1.7 V, I_{OL} = 16 mA		0.4	0.5	V
I_{IH}	High-level input current	V_{CC} = 5.5 V, V_I = 3.11 V		0.3	0.42	mA
I_{IL}	Low-level input current	V_{CC} = 5.5 V, V_I = 0.15 V			30	μA
I_{OS}	Short-circuit output current‡	V_{CC} = 5.5 V, V_O = 0	−18		−60	mA
r_i	Input resistance	V_{CC} = 4.5 V, 0 V, or open, ΔV_I = 0.15 V to 4.15 V	7		20	kΩ
I_{CC}	Supply current	V_{CC} = 5.5 V, I_{OH} = −0.4 mA, All inputs at 0.7 V		15	25	mA
		V_{CC} = 5.5 V, I_{OL} = 16 mA, All inputs at 4 V		28	47	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time.

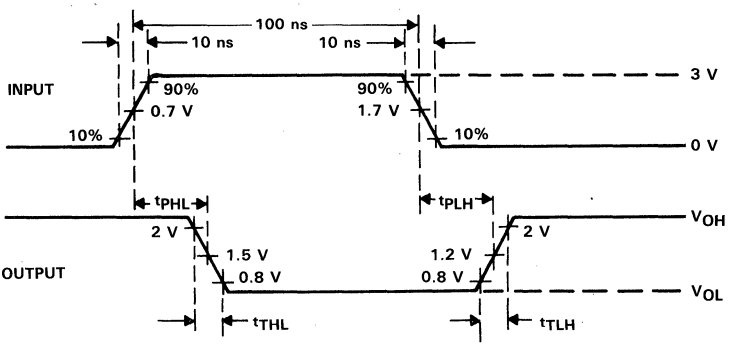
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 400 Ω, C_L = 50 pF, See Figure 1	7	14	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	18	30	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times		0.5	0.8	1.3	
t_{TLH}	Transition time, low-to-high-level output		1	7	12	ns
t_{THL}	Transition time, high-to-low-level output		1	3	12	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $Z_O \approx 50\ \Omega$, PRR $\leq$ 5 MHz.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

FIGURE 1

TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

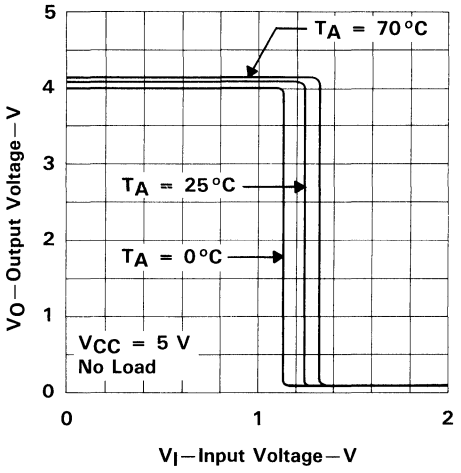


FIGURE 2

VOLTAGE TRANSFER CHARACTERISTICS

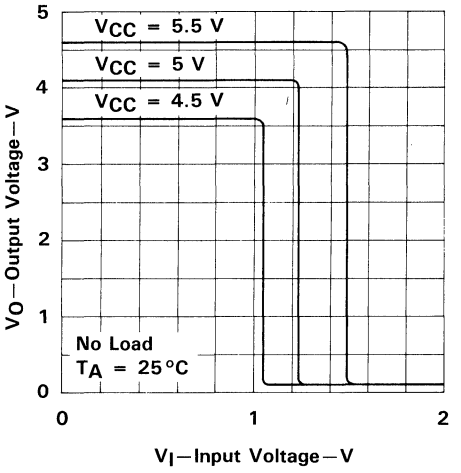


FIGURE 3

INPUT CURRENT
vs
INPUT VOLTAGE

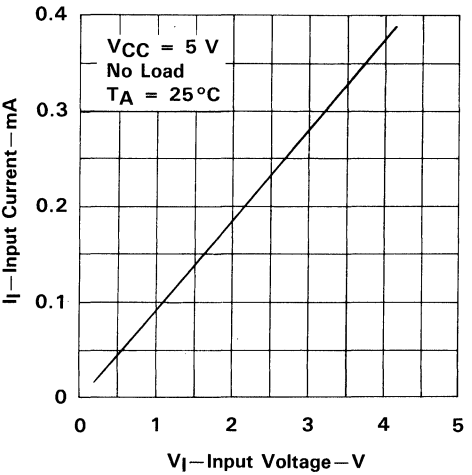


FIGURE 4

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

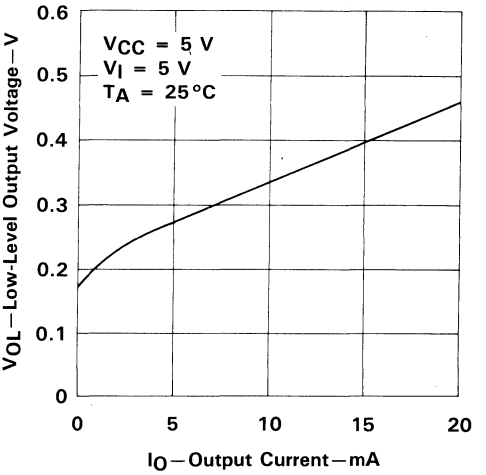


FIGURE 5

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

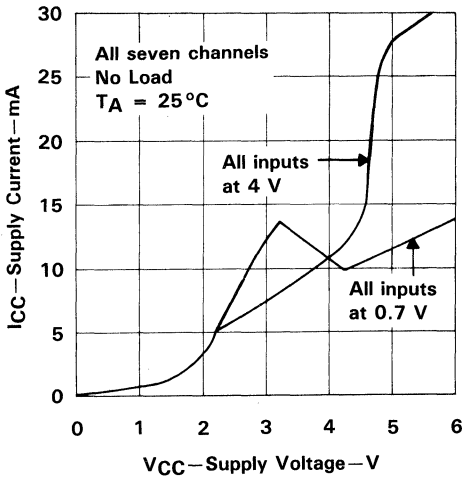
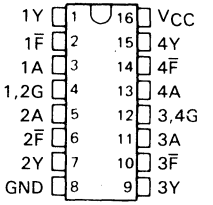


FIGURE 6

D3405, FEBRUARY 1990

- **Meets IBM 360/370 I/O Interface Specification GA22-6974-3 (Also See SN55ALS126 and SN75ALS126)**
- **Minimum Output Voltage of 3.11 V at I_{OH} = −60 mA**
- **Fault-Flag Circuit Output Signals Driver Output Fault**
- **Fault-Detection Current-Limit Circuit Minimizes Power Dissipation During a Fault Condition**
- **Dual Common Enable**
- **Individual Fault Flags**
- **Designed to Replace the MC3481**

D, J, OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OUTPUTS	
G	A	Y	F̄
L	X	L	H
H	H	H	H
H	H	S	L

H = high level, L = low level,
X = irrelevant, S = shorted to ground

description

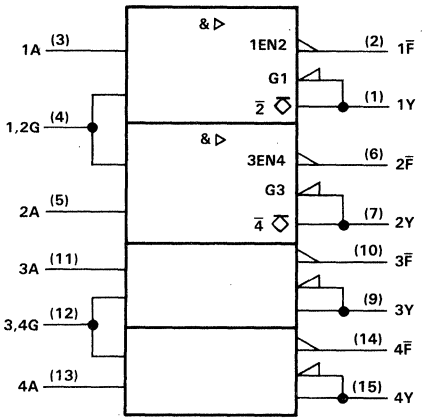
The SN75126 quadruple line driver is designed to meet the IBM 360/370 I/O specification GA22-6974-3. The output voltage is 3.11 V minimum (at I_{OH} = −59.3 mA) over the recommended ranges of supply voltage (4.5 V to 5.95 V) and temperature. Driver outputs use a fault-detection current-limit circuit to allow high drive current but still minimize power dissipation when the output is shorted to ground. The SN75126 is compatible with standard TTL logic and supply voltages.

Fault-flag circuitry is designed to sense and signal a line short on any Y line. Upon detecting an output fault condition, the fault-flag circuit forces the driver output into a low state and signals a fault condition by causing the fault-flag output to go low.

The SN75126 can drive a 50-Ω load as required in the IBM GA22-6974-3 specification or a 90-Ω load as used in many I/O systems. Optimum performance can be achieved when the device is used with either the SN75125, SN75127, SN75128, or SN75129 line receivers.

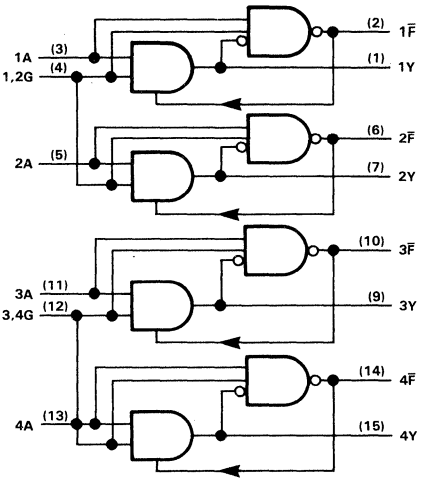
The SN75126 is characterized for operation from 0°C to 70°C.

logic symbol†

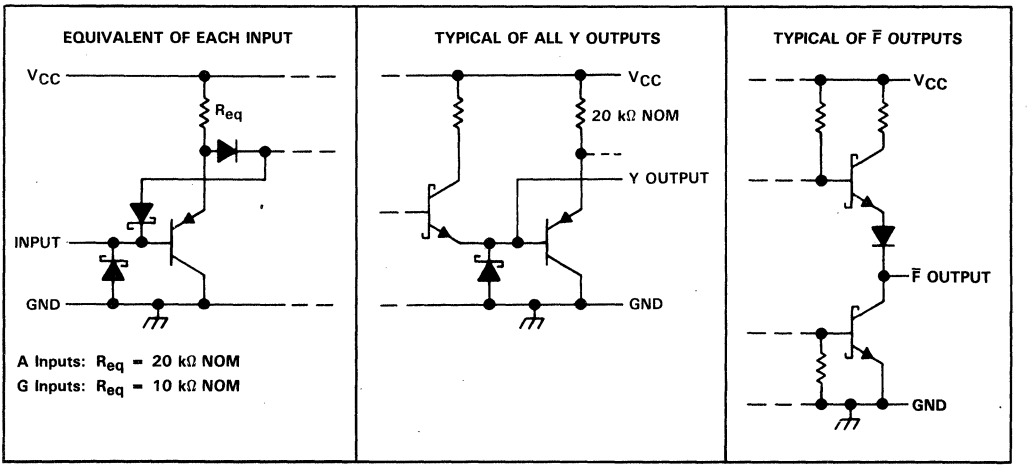


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.95	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−59.3	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	A,G	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
V_{OH}	High-level output voltage	Y	V_{CC} = 4.5 V,	I_{OH} = −59.3 mA,	V_{IH} = 2 V	3.11		V
		Y	V_{CC} = 5.25 V,	I_{OH} = −41 mA,	V_{IH} = 2 V	3.9		
		$\overline{F}$	V_{CC} = 4.5 V,	I_{OH} = −400 μA,	V_{IH} = 2 V	2.5		
V_{OL}	Low-level output voltage	Y	V_{CC} = 5.5 V,	I_{OL} = −240 μA,	V_{IL} = 0.8 V		0.15	V
		Y	V_{CC} = 5.95 V,	I_{OL} = −1 mA,	V_{IL} = 0.8 V		0.15	
		$\overline{F}$	V_{CC} = 4.5 V, V_{IH} = 2 V	I_{OL} = 8 mA,	Y at 0 V,		0.5	
$I_{O(off)}$	Off-state output current	Y	V_{CC} = 4.5 V,	V_I = 0,	V_O = 3.11 V		100	μA
		Y	V_{CC} = 0,	V_I = 0,	V_O = 3.11 V		200	
I_I	Input current	A	V_{CC} = 4.5 V,	V_I = 5.5 V			100	μA
		G					200	
I_{IH}	High-level input current	A	V_{CC} = 4.5 V,	V_I = 2.7 V			20	μA
		G					40	
I_{IL}	Low-level input current	A	V_{CC} = 5.95 V,	V_I = 0.4 V			−250	μA
		G					−500	
I_{OS}	Short-circuit output current	Y	V_{CC} = 5.5 V,	V_O = 0,	V_{IH} = 2.7 V		−5	mA
		$\overline{F}$	V_{CC} = 5.5 V,	V_O = 0		−15	−100	
		Y	V_{CC} = 5.95 V,	V_O = 0,	V_{IH} = 2.7 V		−5	
		$\overline{F}$	V_{CC} = 5.95 V,	V_O = 0		−15	−110	
I_{CCH}	Supply current, all outputs high		V_{CC} = 5.5 V,	No load,	V_{IH} = 2 V		70	mA
			V_{CC} = 5.95 V,	No load,	V_{IH} = 2 V		80	
I_{CCL}	Supply current, Y outputs low		V_{CC} = 5.5 V,	No load,	V_{IL} = 0.8 V		55	mA
			V_{CC} = 5.95 V,	No load,	V_{IL} = 0.8 V		70	

switching characteristics at T_A = 25°C

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y	V_{CC} = 4.5 V to 5.5 V, R_L = 50 Ω, C_L = 50 pF, $V_{H(ref)}$ = 3.11 V, See Figures 1 and 2		40	ns
t_{PHL}	Propagation delay time, high-to-low-level output					37	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times				0.3	3	
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y	V_{CC} = 5.25 V to 5.95 V, R_L = 90 Ω, C_L = 50 pF, $V_{H(ref)}$ = 3.9 V See Figures 1 and 2		45	ns
t_{PHL}	Propagation delay time, high-to-low-level output					45	ns
t_{PLH}	Propagation delay time, low-to-high-level output	A	$\overline{F}$	V_{CC} = 5 V, R_L = 2 kΩ, C_L = 15 pF, See Figures 1 and 2		60	ns
t_{PHL}	Propagation delay time, high-to-low-level output					100	ns

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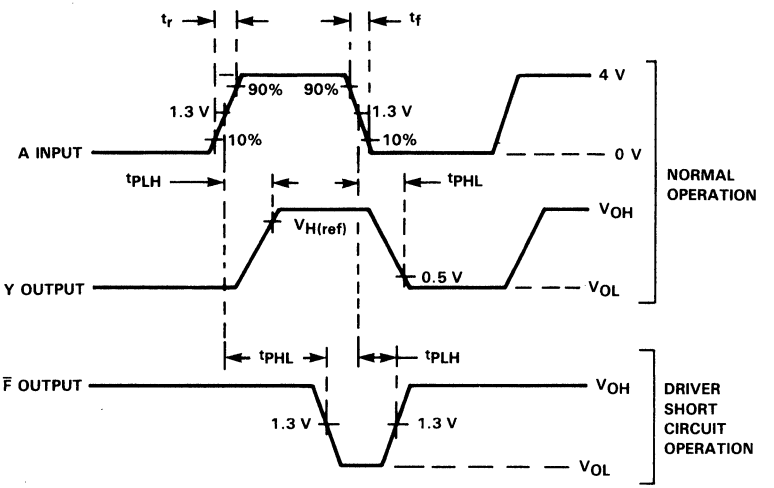
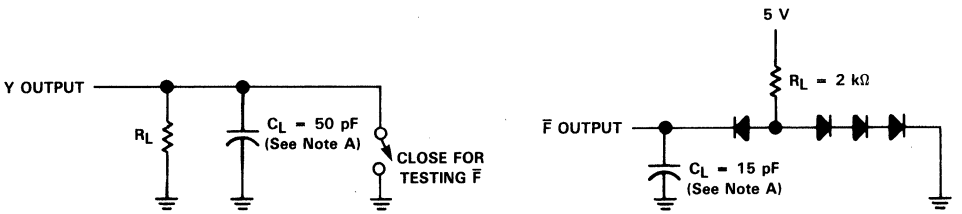
PARAMETER MEASUREMENT INFORMATION



NOTE: The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} ≈ 50 Ω.

FIGURE 1. INPUT AND OUTPUT VOLTAGE WAVEFORMS



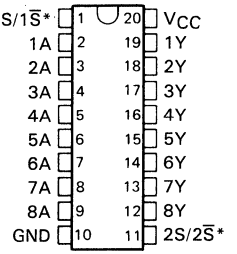
NOTE A: C_L includes probe and stray capacitance.

FIGURE 2. SWITCHING CHARACTERISTICS LOAD CIRCUITS

D2305, JANUARY 1977—REVISED SEPTEMBER 1986

- **Meets IBM 360/370 I/O Specification**
- **Input Resistance . . . 7 kΩ to 20 kΩ**
- **Output Compatible With TTL**
- **Schottky-Clamped Transistors**
- **Operates From a Single 5-Volt Supply**
- **High Speed . . . Low Propagation Delay**
- **Ratio Specification . . . t_{PLH}/t_{THL}**
- **Common Strobe for Each Group of Four Receivers**
- **SN75128 . . . Active-High Strobes**
  SN75129 . . . Active-Low Strobes

DW, J, OR N PACKAGE
(TOP VIEW)



*S and S̄ for SN75128 and SN75129, respectively

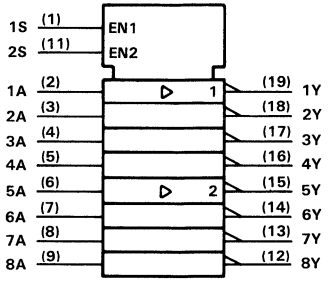
description

The SN75128 and SN75129 are eight-channel line receivers designed to satisfy the requirements of the input-output interface specification for IBM 360/370. Both devices feature common strobes for each group of four devices. The SN75128 has active-high strobes; the SN75129 has active-low strobes. Special low-power design and Schottky-diode-clamped transistors allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs.

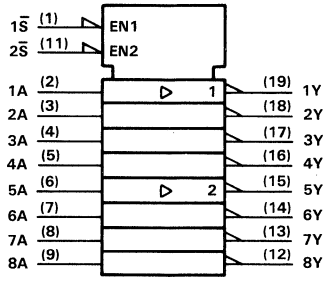
The SN75128 and SN75129 are characterized for operation from 0°C to 70°C.

logic symbols†

SN75128



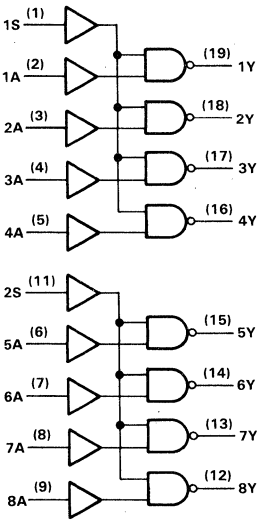
SN75129



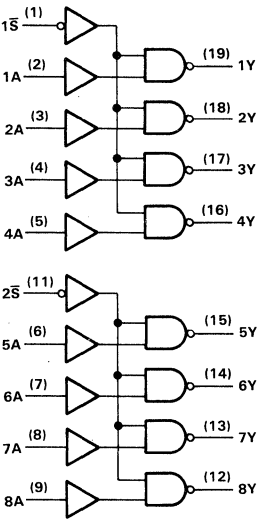
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

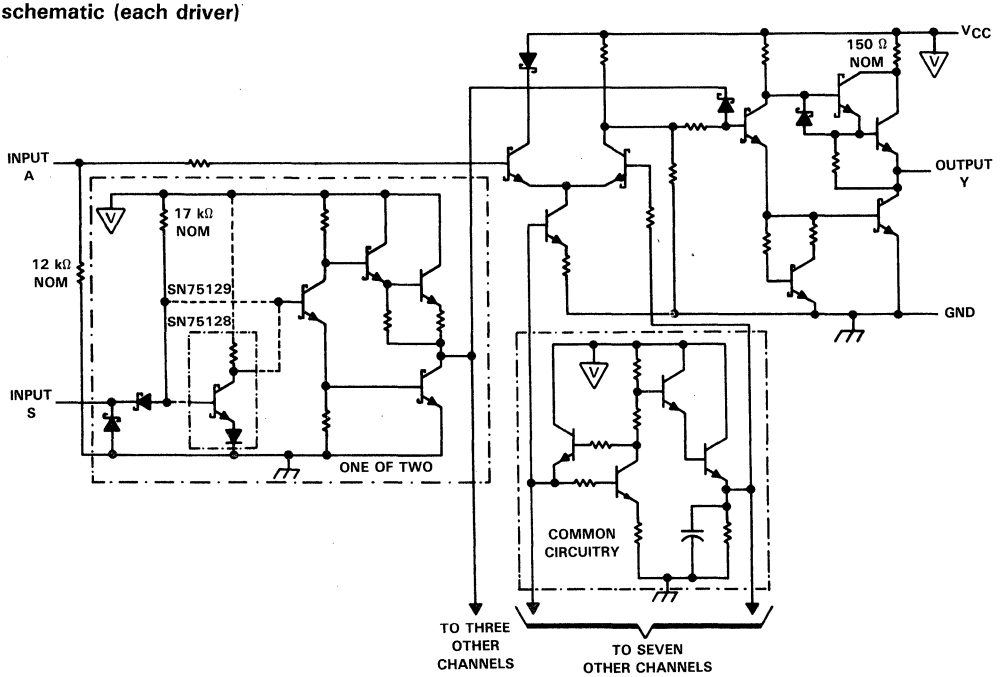
SN75128



SN75129



schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
A input voltage range . . . . . −0.15 V to 7 V
Strobe input voltage . . . . . 7 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}	A	1.7			V
	S	2			
Low-level input voltage, V_{IL}	A			0.7	V
	S			0.7	
High-level output current, I_{OH}				−0.4	mA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

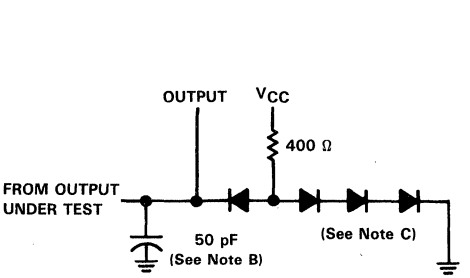
PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, V_{IL} = 0.7 V, I_{OH} = −0.4 mA	2.4	3.1		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, V_{IH} = 1.7 V, I_{OL} = 16 mA		0.4	0.5	V
V_{IK}	Input clamp voltage	S	V_{CC} = 4.5 V, I_I = −18 mA			−1.5	V
I_{IH}	High-level input current	A	V_{CC} = 5.5 V, V_I = 3.11 V		0.3	0.42	mA
		S	V_{CC} = 5.5 V, V_I = 2.7 V			20	μA
I_{IL}	Low-level input current	A	V_{CC} = 5.5 V, V_I = 0.15 V			30	μA
		S	V_{CC} = 5.5 V, V_I = 0.4 V			−0.4	mA
I_{OS}	Short-circuit output current‡		V_{CC} = 5.5 V, V_O = 0	−18		−60	mA
r_i	Input resistance		V_{CC} = 4.5 V, 0, or open; ΔV_I = 0.15 V to 4.15 V	7		20	kΩ
I_{CC}	Supply current	SN75128	V_{CC} = 5.5 V, Strobe at 2.4 V, All A inputs at 0.7 V		19	31	mA
		SN75129	V_{CC} = 5.5 V, Strobe at 0.4 V, All A inputs at 0.7 V		19	31	
		SN75128	V_{CC} = 5.5 V, Strobe at 2.4 V, All A inputs at 4 V		32	53	
		SN75129	V_{CC} = 5.5 V, Strobe at 0.4 V, All A inputs at 4 V		32	53	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time.

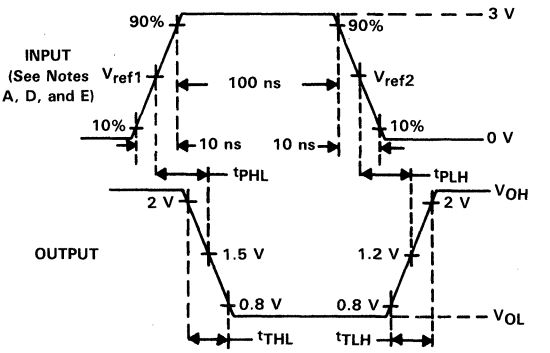
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM	TEST CONDITIONS	SN75128			SN75129			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	R_L = 400 Ω, C_L = 50 pF, See Figure 1	7	14	25	7	14	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	18	30	10	18	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output	S			26	40		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				22	35		16	30	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times	A		0.5	0.8	1.3	0.5	0.8	1.3	
t_{TLH}	Transition time, low-to-high-level output			1	7	12	1	7	12	ns
t_{THL}	Transition time, high-to-low-level output			1	3	12	1	3	12	ns

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by a generator having the following characteristics: Z_O = 50 Ω, PRR ≤ 5 MHz.
B. Includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. The strobe inputs of SN75129 are in-phase with the output.
E. V_{ref1} = 0.7 V and V_{ref2} = 1.7 V for testing data (A) inputs, V_{ref1} = V_{ref2} = 1.3 V for strobe inputs.

FIGURE 1

TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

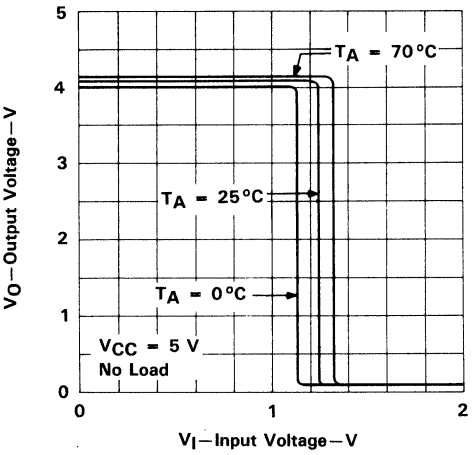


FIGURE 2

VOLTAGE TRANSFER CHARACTERISTICS
FROM A INPUTS

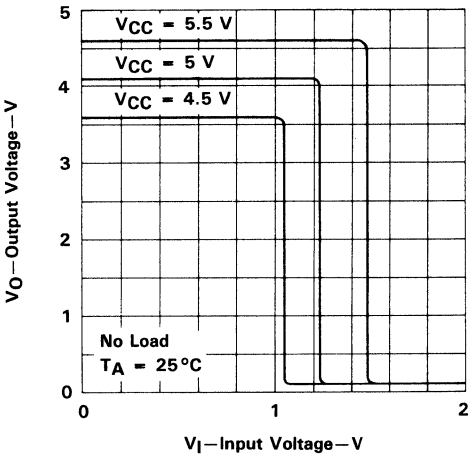


FIGURE 3

INPUT CURRENT
vs
INPUT VOLTAGE

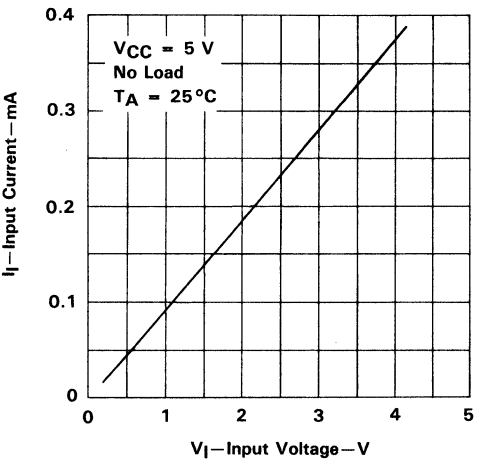


FIGURE 4

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

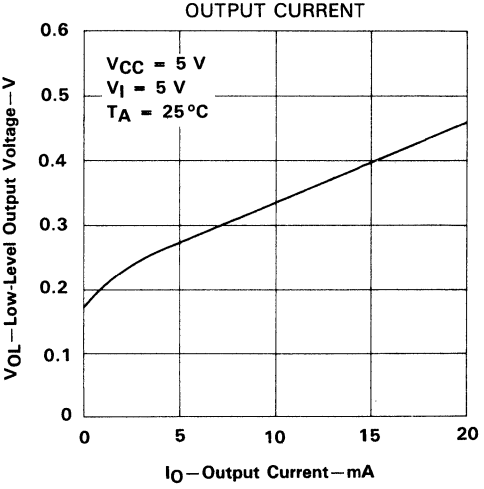
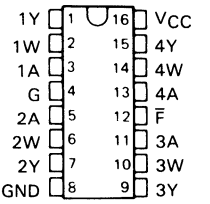


FIGURE 5

D3406, FEBRUARY 1990

- **Meets IBM 360/370 I/O Interface Specification GA22-6974-3 (Also see SN75ALS130)**
- **Minimum Output Voltage of 3.11 V at I_{OH} = −60 mA**
- **Fault-Flag Circuit Output Signals Driver Output Fault**
- **Fault-Detection Current-Limit Circuit Minimizes Power Dissipation During a Fault Condition**
- **Common Enable and Common Fault Flag**
- **Designed to Be an Improved Replacement for the MC3485**

D, J, OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OUTPUTS		
G†	A	Y	F̄	W
L	X	L	H	H
X	L	L	H	H
H	H	H	H	L
H	H	S	L	H

H = high level, L = low level, X = irrelevant, S = shorted to ground

†G and F̄ are common to the four drivers. If any of the four Y outputs is shorted, the Fault-Flag will respond.

description

The SN75130 quadruple line driver is designed to meet the IBM 360/370 I/O specification GA22-6974-3. The output voltage is 3.11 V minimum (at I_{OH} = −59.3 mA) over the recommended ranges of supply voltage (4.5 V to 5.5 V) and temperature (0°C to 70°C). Driver outputs use a fault-detection current-limit circuit to allow high drive current but still minimize power dissipation when the output is shorted to ground. The SN75130 is compatible with standard TTL logic and supply voltages.

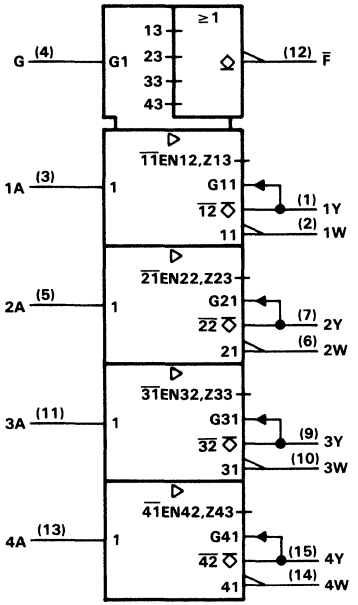
Fault-flag circuitry is designed to sense and signal a line short on any Y line. Upon detecting an output fault condition, the fault-flag circuit forces the driver output into the off (low) state and signals a fault condition by causing the fault-flag output to go low.

The SN75130 can drive a 50-Ω load as required in the IBM GA22-6974-3 specification or a 90-Ω load as used in many I/O systems. Optimum performance can be achieved when the device is used with either the SN75125, SN75127, SN75128, or SN75129 line receivers.

The SN75130 is characterized for operation from 0°C to 70°C.

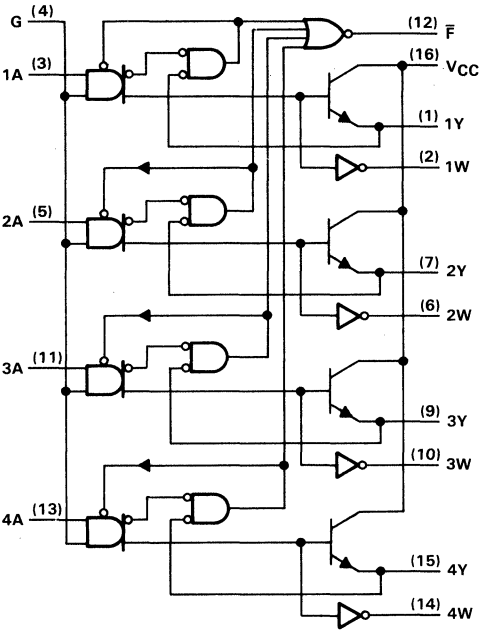
IMPACT is a trademark of Texas Instruments Incorporated

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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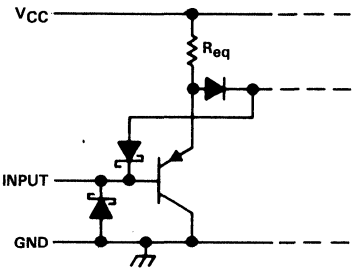
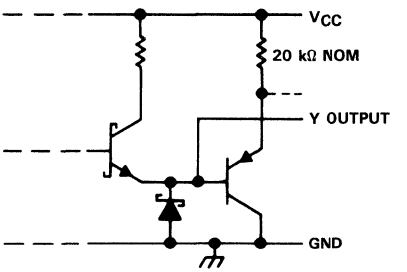
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

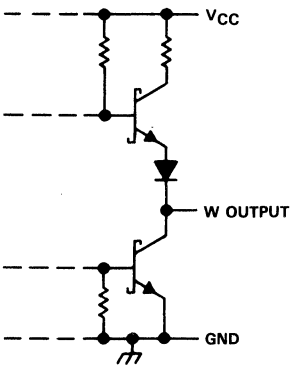


A Inputs: R_{eq} = 20 kΩ NOM
G Inputs: R_{eq} = 10 kΩ NOM

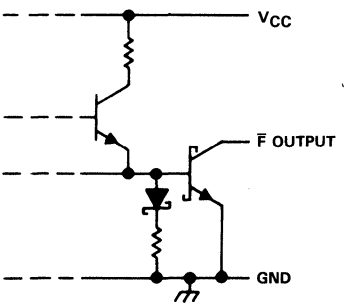
TYPICAL OF ALL Y OUTPUTS



TYPICAL OF ALL W OUTPUTS



TYPICAL OF $\overline{F}$ OUTPUT



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Continuous total dissipation at (or below): D package . . . . . 950 mW
J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: For operation above 15 °C free-air temperature, derate D package to 608 mW at 70 °C at the rate of 7.6 mW/ °C, the J package to 656 mW at 70 °C at the rate of 8.2 mW/ °C, and the N package to 736 mW at 70 °C at the rate of 9.2 mW/ °C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.95	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−59.3	mA
Operating free-air temperature, T_A	0		70	°C

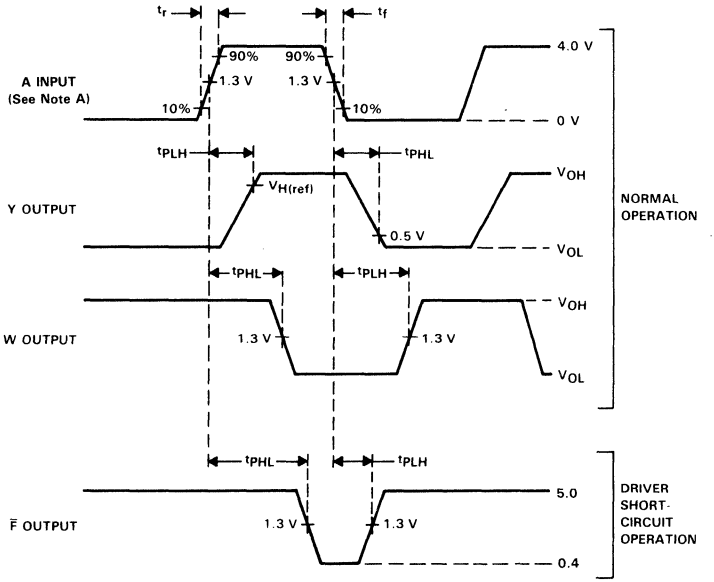
electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	A,G	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	Y	V_{CC} = 4.5 V,	I_{OH} = −59.3 mA,	V_{IH} = 2 V	3.11		V
		Y	V_{CC} = 5.25 V,	I_{OH} = −41 mA,	V_{IH} = 2 V	3.9		
		W	V_{CC} = 4.5 V,	I_{OH} = −400 μA,	V_{IH} = 2 V	2.5		
V_{OL}	Low-level output voltage	Y	V_{CC} = 5.5 V,	I_{OL} = −240 μA,	V_{IL} = 0.8 V		0.15	V
		Y	V_{CC} = 5.95 V,	I_{OL} = −1 mA,	V_{IL} = 0.8 V		0.15	
		$\overline{F}$	V_{CC} = 4.5 V,	I_{OL} = 8 mA,	Y at 0 V		0.5	
		W	V_{CC} = 4.5 V,	I_{OL} = 8 mA			0.5	
$I_{O(off)}$	Off-state output current	Y	V_{CC} = 4.5 V,	V_{IL} = 0,	V_O = 3.11 V		100	μA
		Y	V_{CC} = 0,	V_{IL} = 0,	V_O = 3.11 V		200	
I_{OH}	High-level output current	$\overline{F}$	V_{CC} = 5.95 V,	V_{OH} = 5.95 V			100	μA
I_I	Input current	A	V_{CC} = 4.5 V,	V_{IH} = 5.5 V			100	μA
		G					400	
I_{IH}	High-level input current	A	V_{CC} = 4.5 V,	V_{IH} = 2.7 V			20	μA
		G					80	
I_{IL}	Low-level input current	A	V_{CC} = 5.95 V,	V_{IL} = 0,4 V			250	μA
		G					−1000	
I_{OS}	Short-circuit output	Y	V_{CC} = 5.5 V,	V_O = 0			−5	mA
		W				−15	−100	
		Y	V_{CC} = 5.95 V,	V_O = 0V			−5	
		W				−15	−110	
I_{CCH}	Supply current, all outputs high		V_{CC} = 5.5 V,	V_I = 2 V			75	mA
			V_{CC} = 5.95 V,	V_I = 2 V			85	
I_{CCL}	Supply current, Y outputs low		V_{CC} = 5.5 V,	V_I = 0.8 V			55	mA
			V_{CC} = 5.95 V,	V_I = 0.8 V			70	

switching characteristics over recommended operating free-air temperature range

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y	V_{CC} = 4.5 V to 5.5 V, R_L = 50 Ω, C_L = 50 pF, $V_{H(ref)}$ = 3.11 V, Input f = 1 MHz, See Figures 1 and 2		40	ns
t_{PHL}	Propagation delay time, high-to-low-level output					37	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times				0.3	3	
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y	V_{CC} = 5.25 V to 5.95 V, R_L = 90 Ω, C_L = 50 pF, $V_{H(ref)}$ = 3.9 V, Input f = 5 MHz, See Figures 1 and 2		45	ns
t_{PHL}	Propagation delay time, high-to-low-level output					45	ns
t_{PLH}	Propagation delay time, low-to-high-level output	A	W	V_{CC} = 5 V, R_L = 2 kΩ, C_L = 15 pF, See Figures 1 and 2		45	ns
t_{PHL}	Propagation delay time, high-to-low-level output					28	ns
t_{PLH}	Propagation delay time, low-to-high-level output	A	$\overline{F}$	V_{CC} = 5 V, R_L = 2 kΩ, C_L = 15 pF, See Figures 1 and 2		60	ns
t_{PHL}	Propagation delay time, high-to-low-level output					100	ns

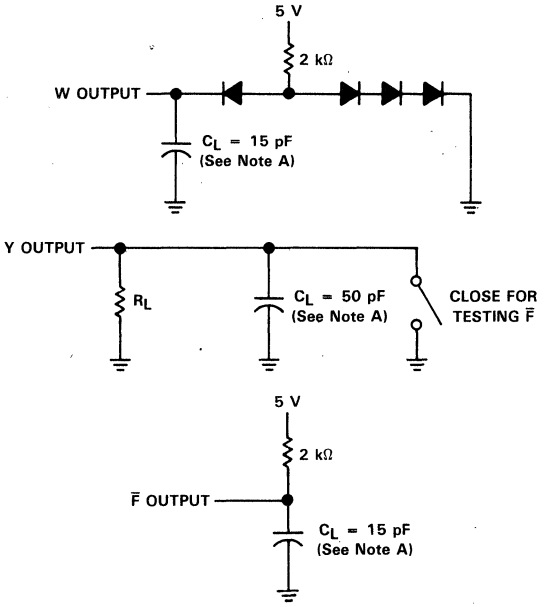
PARAMETER MEASUREMENT INFORMATION



NOTE A: The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, Z_{out} = 50 Ω.

FIGURE 1. INPUT AND OUTPUT VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



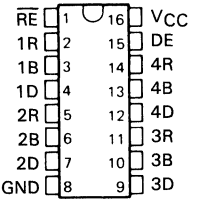
NOTE A: C_L includes probe and stray capacitance.

FIGURE 2. SWITCHING CHARACTERISTICS LOAD CIRCUITS

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

- **P-N-P Inputs for Minimal Input Loading (200 μA Maximum)**
- **High-Speed Schottky Circuitry**
- **3-State Outputs for Driver and Receiver**
- **Party-Line (Data-Bus) Operation**
- **Single 5-V Supply**
- **Driver Has 40-mA Current Sink Capability**
- **Designed to Be Functionally Interchangeable with Signetics N8T26, also Called 8T26**

D, J, OR N PACKAGE
(TOP VIEW)



description

The SN75136 is a quadruple transceiver utilizing Schottky-diode-clamped transistors. Both the driver and receiver have 3-state outputs. With p-n-p inputs, the input loading is reduced to a maximum input current of 200 μA.

The SN75136 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (DRIVER)

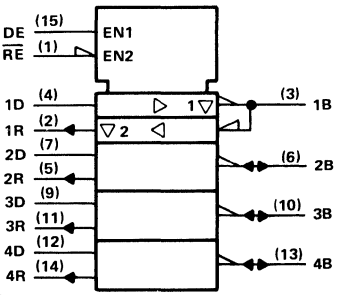
INPUTS		OUTPUT
D	DE	B
L	H	H
H	H	L
X	L	Z

FUNCTION TABLE (RECEIVER)

INPUTS		OUTPUT
B	$\overline{RE}$	R
L	L	H
H	L	L
X	H	Z

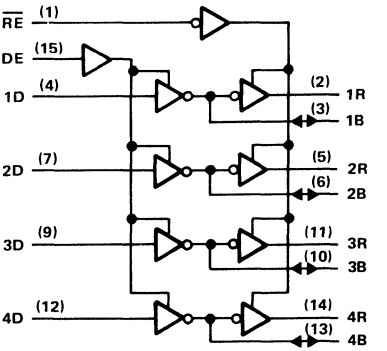
H = high level
L = low level
X = irrelevant
Z = high impedance

logic symbol†

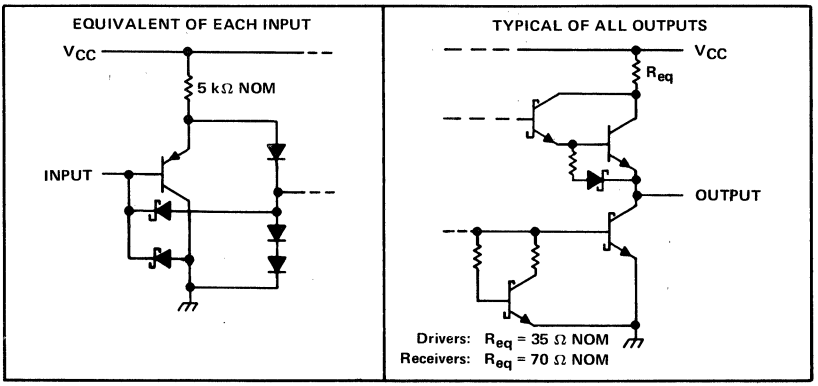


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schématics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	B, D, DE, $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	B, D, DE, $\overline{RE}$			0.85	V
High-level output current, I_{OH}	Driver, B			−10	mA
	Receiver, R			−2	
Low-level output current, I_{OL}	Driver, B			40	mA
	Receiver, R			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature and supply voltage range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	B,D,DE,$\overline{RE}$	I_I = −5 mA			−1	V
V_{OH}	High-level output voltage	B	V_{IH} = 2 V, V_{IL} = 0.85 V, I_{OH} = −10 mA	2.6	3.1		V
		R	V_{IL} = 0.85 V, I_{OH} = −2 mA	2.6	3.1		
V_{OL}	Low-level output voltage	B	V_{IH} = 2 V, I_{OL} = 40 mA			0.5	V
		R	V_{IH} = 2 V, V_{IL} = 0.85 V, I_{OL} = 16 mA			0.5	
I_{OZ}	Off-state (high-impedance state) output current	B,R	DE at 0.85 V, $\overline{RE}$ at 2 V, V_O = 2.6 V			100	μA
		R	$\overline{RE}$ at 2 V, V_O = 0.5 V			−100	
I_{IH}	High-level input current	D,DE,$\overline{RE}$	V_I = 5.25 V			25	μA
I_{IL}	Low-level input current	B,D,DE,$\overline{RE}$	V_I = 0.4 V			−200	μA
I_{OS}	Short-circuit output current‡	B	V_{CC} = 5.25 V	−50		−150	mA
		R		−30		−75	
I_{CC}	Supply current		V_{CC} = 5.25 V, No load			87	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	B	R	C_L = 30 pF, See Figure 1		8	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output					7	14	
t_{PLH}	Propagation delay time, low-to-high-level output	D	B	C_L = 300 pF, See Figure 2		11	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					16	24	
t_{PLZ}	Output disable time from low level	$\overline{RE}$	R	C_L = 30 pF, See Figure 3		16	24	ns
t_{PZL}	Output enable time to low level					15	30	
t_{PLZ}	Output disable time from low level	DE	B	C_L = 300 pF, See Figure 4		9	24	ns
t_{PZL}	Output enable time to low level					31	38	

†All typical values are at T_A = 25°C and V_{CC} = 5 V.
‡Only one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION

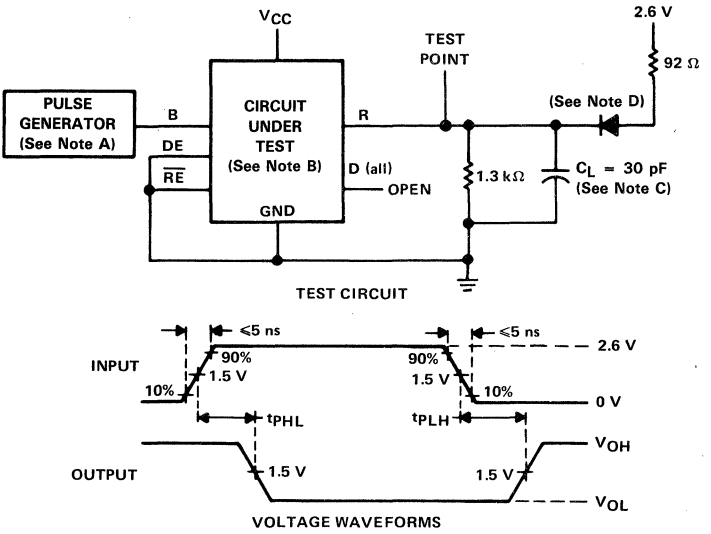


FIGURE 1. PROPAGATION DELAY TIMES FROM BUS TO RECEIVER OUTPUT

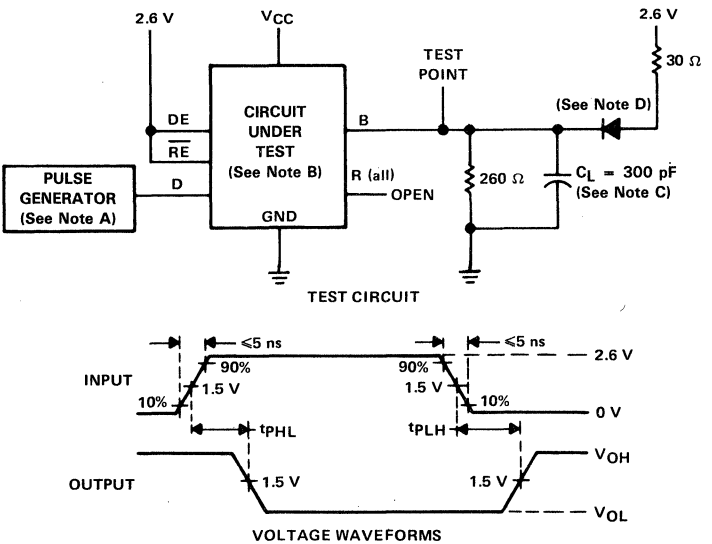


FIGURE 2. PROPAGATION DELAY TIMES FROM DRIVER INPUT TO BUS

NOTES: A. The pulse generator in Figures 1 and 2 has the following characteristics: PRR ≤ 10 MHz, duty cycle = 50%, $Z_O \approx 50\ \Omega$.
B. All inputs and outputs not shown are open.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916 or 1N3064.

PARAMETER MEASUREMENT INFORMATION

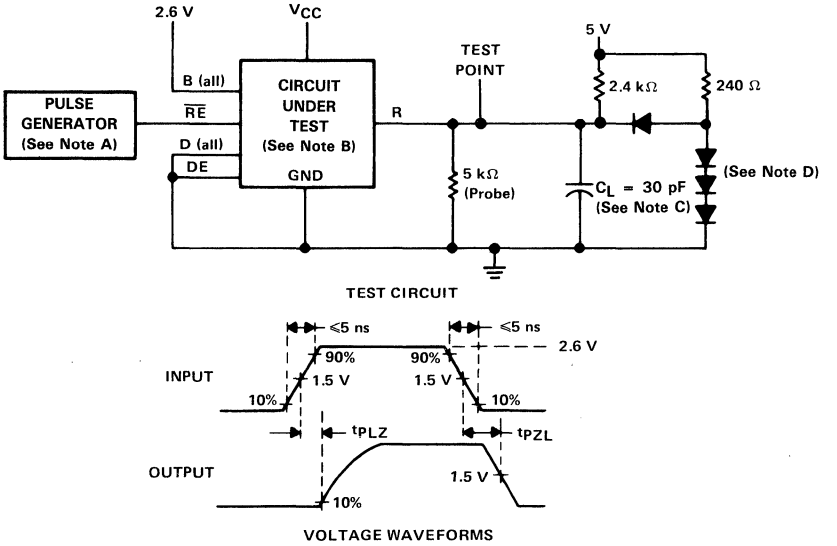


FIGURE 3. RECEIVER ENABLE AND DISABLE TIMES

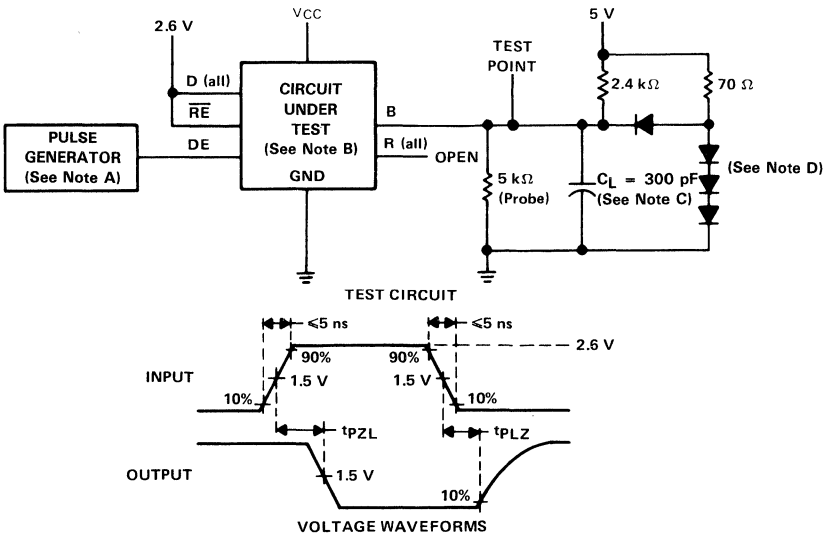


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The pulse generator in Figures 3 and 4 has the following characteristics: PRR ≤ 5 MHz, duty cycle = 50%, $Z_O \approx 50\ \Omega$.
B. All inputs and outputs now shown are open.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916 or 1N3064.

D2155, JANUARY 1977—REVISED OCTOBER 1986

- Single 5-V Supply
- ± 100 mV Sensitivity
- For Application As:
  Single-Ended Line Receiver
  Gated Oscillator
  Level Comparator
- Adjustable Reference Voltage
- TTL Outputs
- TTL-Compatible Strobe
- Designed for Party-Line (Data-Bus) Applications
- Common Reference Pin
- Common Strobe
- '141 Has Diode-Protected Input Stage for Power-Off Condition

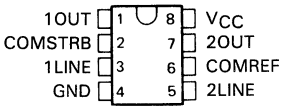
description

Each of these devices consists of a dual single-ended line receiver with TTL-compatible strobes and outputs. The reference voltage (switching threshold) is applied externally and can be adjusted from 1.5 V to 3.5 V, making it possible to optimize noise immunity for a given system design. Due to their low input current (less than 100 μA), they are ideally suited for party-line (bus-organized) systems.

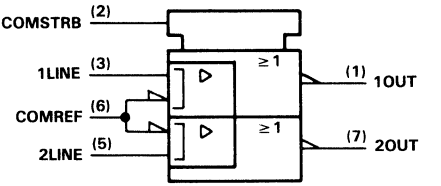
The '140 has a common reference voltage pin and a common strobe. The '141 is the same as the '140 except that the input stage is diode protected.

The SN75140 and SN75141 are characterized for operation from 0°C to 70°C.

D, JG, OR P PACKAGE
(TOP VIEW)

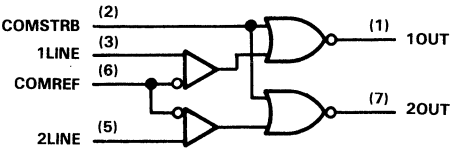


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

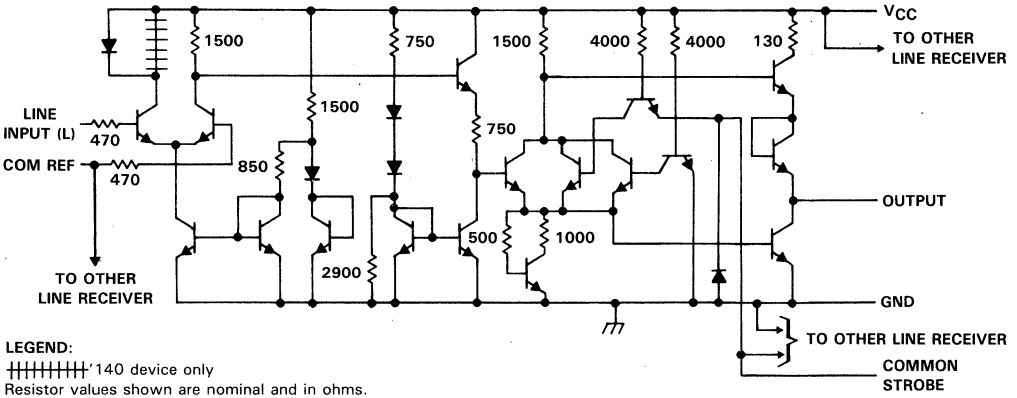


FUNCTION TABLE
(EACH RECEIVER)

LINE INPUT	STROBE	OUTPUT
≤ V_{ref} − 100 mV	L	H
≥ V_{ref} + 100 mV	X	L
X	H	L

H = high level, L = low level, X = irrelevant

schematic (each receiver)



LEGEND:
HHHHHHHH '140 device only
Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Reference input voltage, V_{ref} . . . . . 5.5 V
Line input voltage range with respect to ground . . . . . −2 V to 5.5 V
Line input voltage with respect to V_{ref} . . . . . ±5 V
Strobe input voltage . . . . . 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTE 1: Unless otherwise specified, voltage values are with respect to network terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
JG	1050 mW	8.4 mW/°C	672 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Reference input voltage, V_{ref}	1.5		3.5	V
High-level line input voltage, $V_{IH(L)}$	$V_{ref}+0.1$		$V_{CC}-1$	V
Low-level line input voltage, $V_{IL(L)}$	0		$V_{ref}-0.1$	V
High-level strobe input voltage, $V_{IH(S)}$	2		5.5	V
Low-level strobe input voltage, $V_{IL(S)}$	0		0.8	V

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 10%, V_{ref} = 1.5 V to 3.5 V (unless otherwise noted)

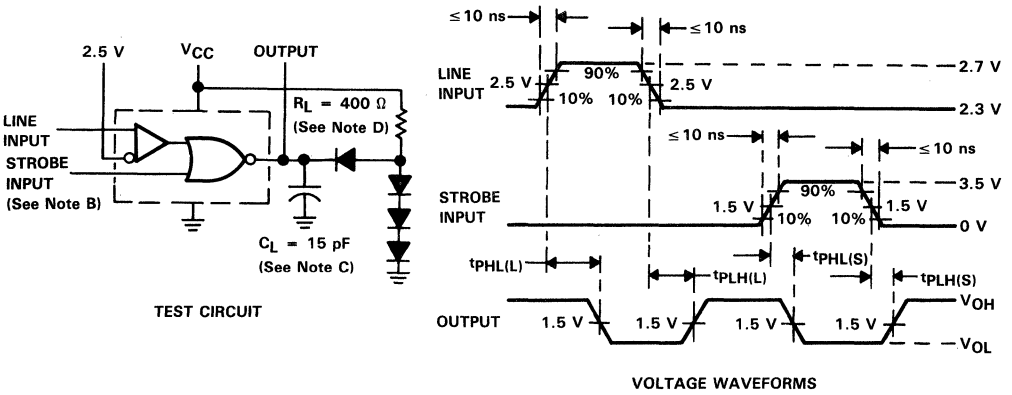
PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IK(S)}$	Strobe input clamp voltage		$I_{I(S)}$ = −12 mA			−1.5	V
V_{OH}	High-level output voltage		$V_{IL(L)} = V_{ref}$ − 100 mV, $V_{IL(S)}$ = 0.8 V, I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage		$V_{IH(L)} = V_{ref}$ + 100 mV, $V_{IL(S)}$ = 0.8 V, I_{OL} = 16 mA			0.4	V
			$V_{IL(L)} = V_{ref}$ − 100 mV, $V_{IH(S)}$ = 2 V, I_{OL} = 16 mA			0.4	
$I_{I(S)}$	Strobe input current at maximum input voltage	Strobe	$V_{I(S)}$ = 5.5 V			1	mA
		Com strb				2	
I_{IH}	High-level input current	Strobe	$V_{I(S)}$ = 2.4 V			40	μA
		Com strb				80	
		Line input	$V_{I(L)}$ = 3.5 V, V_{ref} = 1.5 V		35	100	
		Reference	$V_{I(L)}$ = 0, V_{ref} = 3.5 V		35	100	
		Com ref			70	200	
I_{IL}	Low-level input current	Strobe	$V_{I(S)}$ = 0.4 V			−1.6	mA
		Com strb				−3.2	
		Line input	$V_{I(L)}$ = 0, V_{ref} = 1.5 V			−10	μA
		Reference	$V_{I(L)}$ = 1.5 V, V_{ref} = 0			−10	
		Com ref				−20	
I_{OS}	Short-circuit output current‡		V_{CC} = 5.5 V	−18		−55	mA
I_{CCH}	Supply current, output high		$V_{I(S)}$ = 0, $V_{I(L)} = V_{ref}$ − 100 mV		18	30	mA
I_{CCL}	Supply current, output low		$V_{I(S)}$ = 0, $V_{I(L)} = V_{ref}$ + 100 mV		20	35	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Only one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, V_{ref} = 2.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(L)}$	Propagation delay time, low-to-high-level output from line input	C_L = 15 pF, R_L = 400 Ω, See Figure 1		22	35	ns
$t_{PHL(L)}$	Propagation delay time, high-to-low-level output from line input			22	30	
$t_{PLH(S)}$	Propagation delay time, low-to-high-level output from strobe input			12	22	ns
$t_{PHL(S)}$	Propagation delay time, high-to-low-level output from strobe input			8	15	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤50%, Z_O = 50 Ω.
B. Unused strobes are to be grounded.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N3064.

FIGURE 1

TYPICAL CHARACTERISTICS

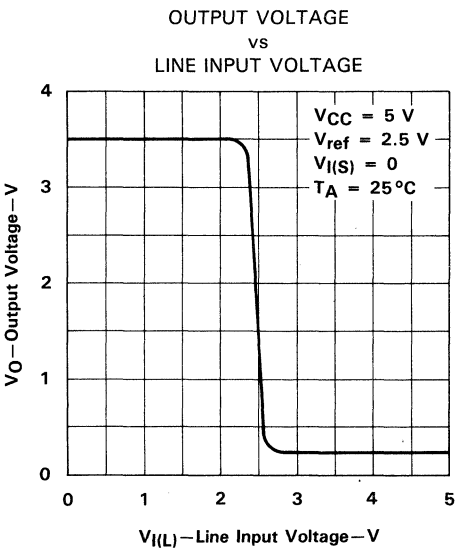
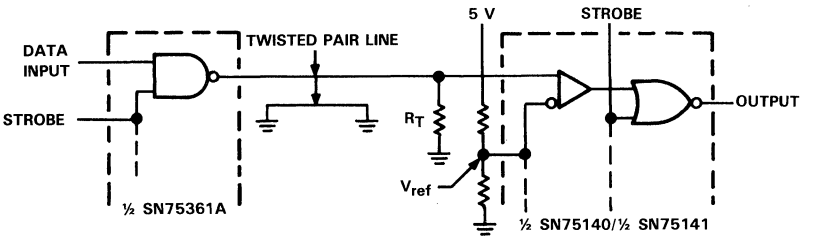


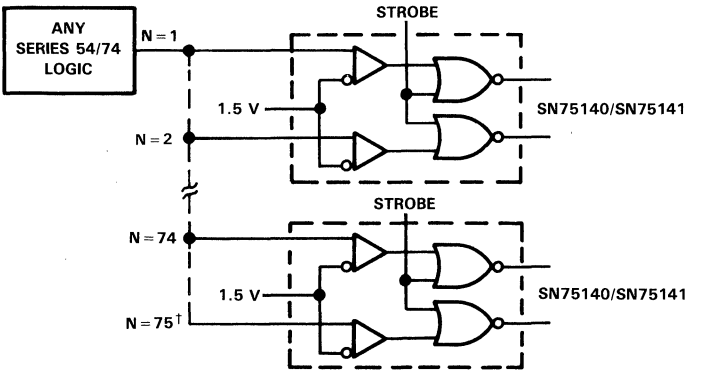
FIGURE 2

APPLICATION INFORMATION

line receiver

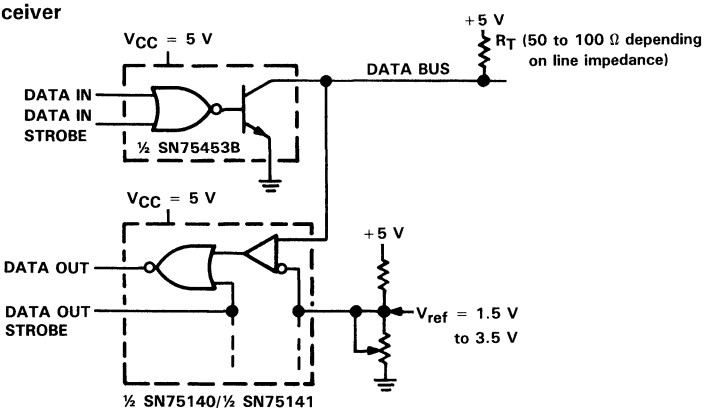


high fan-out from standard TTL gate



†Although most Series 54/74 circuits have a 2.4-V output at 400 μA, they are typically capable of maintaining a 2.4-V output level under a load of 7.5 mA.

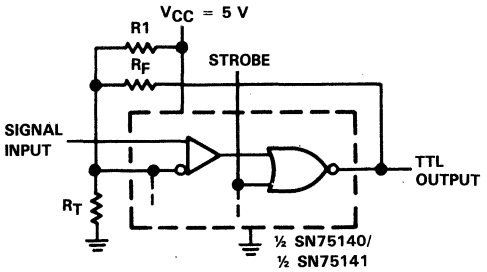
dual bus transceiver



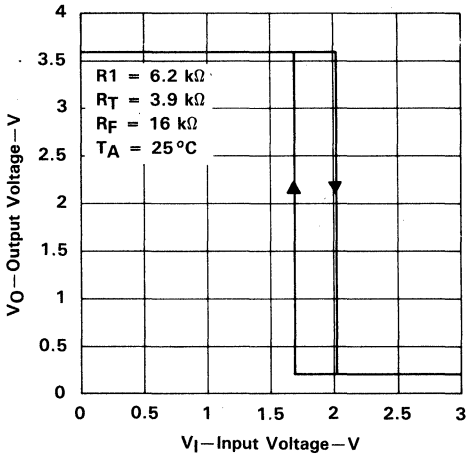
Using this arrangement, as many as 100 transceivers can be connected to a single data bus. The adjustable reference voltage feature allows the noise margin to be optimized for a given system. The complete dual bus transceiver (SN75453B driver and SN75140 receiver) can be assembled in approximately the same space required by a single 16-pin package and only one power supply is required (+5 V). Data In and Data Out terminals are TTL compatible.

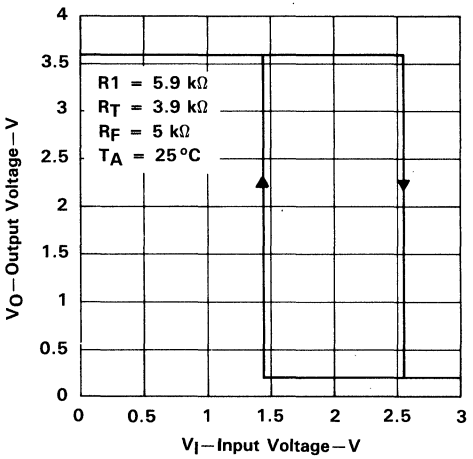
APPLICATION INFORMATION

schmitt trigger



EXAMPLES OF TRANSFER CHARACTERISTICS

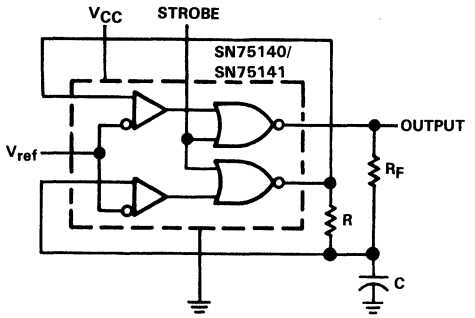


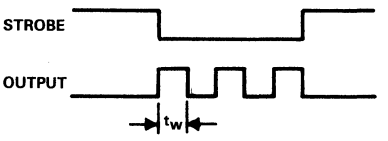


Slowly changing input levels from data lines, optical detectors, and other types of transducers may be converted to standard TTL signals with this Schmitt trigger circuit. R1, R_F, and R_T may be adjusted for the desired hysteresis and trigger levels.

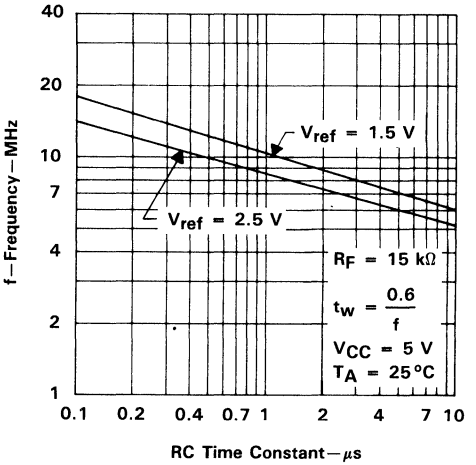
APPLICATION INFORMATION

gated oscillator





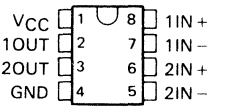
OSCILLATOR FREQUENCY
vs
RC TIME CONSTANT



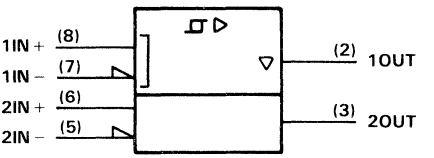
D2609, FEBRUARY 1986

- **Meets EIA Standards RS-422-A and RS-423-A**
- **Meets EIA Standards RS-232 and CCITT V.28 with External Components**
- **Meets Federal Standards 1020 and 1030**
- **Built-in 5-MHz Low-Pass Filter**
- **Operates from Single 5-V Power Supply**
- **Wide Common-Mode Voltage Range**
- **High Input Impedance**
- **TTL-Compatible Outputs**
- **8-Pin Dual-In-Line Package**
- **Pinout Compatible with the μA9637 and μA9639**

D, JG, OR P PACKAGE
(TOP VIEW)

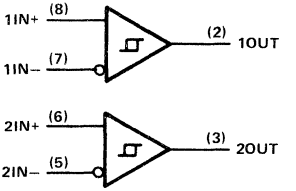


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram

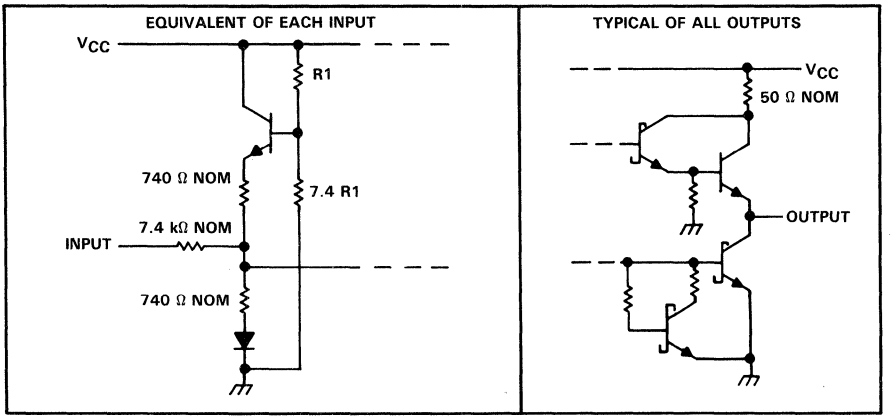


description

The SN75146 is a dual differential line receiver designed to meet EIA standards RS-422-A and RS-423-A. The receiver is designed to have a constant impedance with input voltages of ±3 volts to ±25 volts allowing it to meet the requirements of EIA standard RS-232-C and CCITT recommendation V.28 with the addition of an external bias resistor. This receiver is designed for low-speed operation below 355 kilohertz, and has a built-in 5-megahertz low-pass filter to attenuate high-frequency noise. The inputs are compatible with either a single-ended or a differential line system and the outputs are TTL compatible. This device operates from a single 5-volt power supply and is supplied in both the 8-pin dual-in-line and small outline packages.

The SN75146 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage . . . . . ±25 V
Differential input voltage (see Note 2) . . . . . ±25 V
Output voltage (see Note 1) . . . . . −0.5 V to 5.5 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
D package . . . . . 725 mW
JG package . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package . . . . . 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the JG package to 528 mW at 70°C at the rate of 6.6 mW/°C, the D package to 464 mW at 70°C at the rate of 5.8 mW/°C, and the P package to 640 mW at 70°C at the rate of 8 mW/°C. The SN75146 chips are glass mounted in the JG package.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Operating free-air temperature, T_A	0	25	70	°C

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

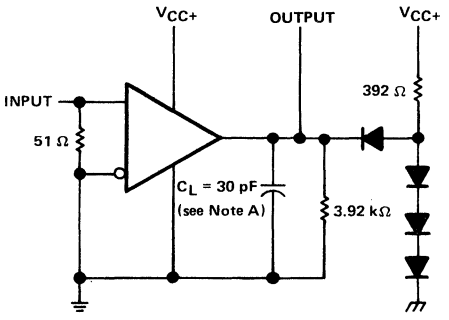
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_T	Threshold voltage (V_{T+} and V_{T-})	See Note 4		−0.2‡		0.2	V
				−0.4‡		0.4	
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)			70			mV
V_{IB}	Input bias voltage	I_I = 0		2		2.4	V
V_{OH}	High-level output voltage	V_{ID} = 0.2 V,	I_O = −1 mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2 V,	I_O = 20 mA		0.35	0.5	V
r_i	Input resistance	See Note 5,	V_I = 3 V to 25 V or V_I = −3 V to −25 V	6	7.8	9.5	kΩ
I_I	Input current	V_{CC} = 0 to 5.5 V, See Note 6	V_I = 10 V		1.1	3.25	mA
			V_I = −10 V		−1.6	−3.25	
I_{OS}	Short-circuit output current§	V_O = 0,	V_{ID} = 0.2 V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5 V,	No load		35	50	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
§ Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTES: 4. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
5. r_i is defined by $\Delta V_I/\Delta I_I$.
6. The input not under test is grounded.

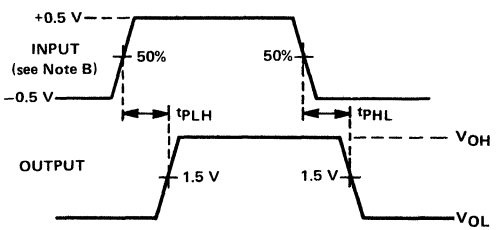
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 1	100	150	300	ns
t_{PHL}	Propagation delay time, high-to-low-level output		100	150	300	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORM

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 300 kHz, duty cycle = 50%.

FIGURE 1. TRANSITION TIMES

TYPICAL CHARACTERISTICS

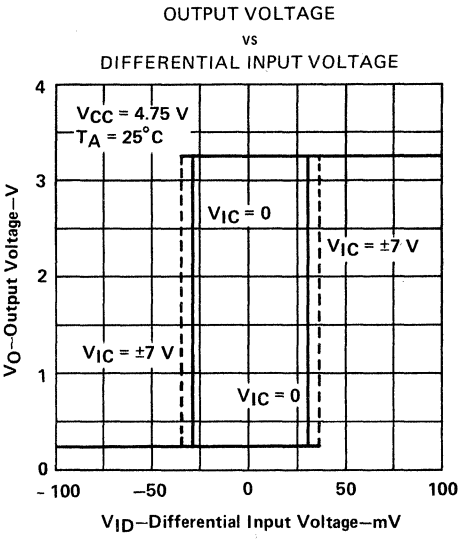


FIGURE 2

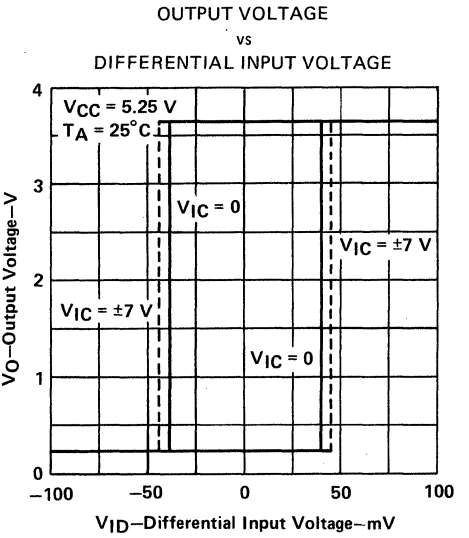
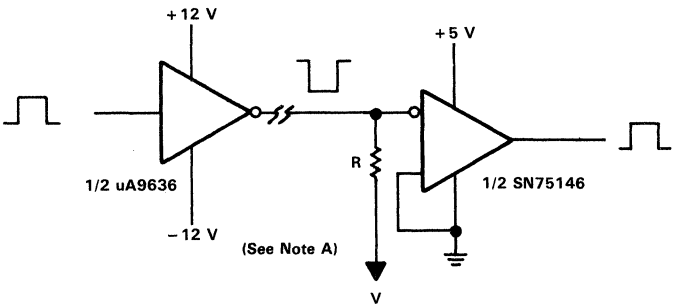


FIGURE 3

TYPICAL APPLICATION DATA



NOTE A: In order to meet the input-impedance and open-circuit-input voltage requirements of RS-232-C and CCITT V.28 and guarantee open-circuit-input failsafe operation, R and V are selected to satisfy the following equations:

$$V = -1.1 - 3.3\,\frac{R}{r_i} \text{ volts}$$

$$3\text{ k}\Omega \le \frac{R(r_i)}{R + r_i} \le 7\text{ k}\Omega$$

FIGURE 4. RS-232-C SYSTEM APPLICATIONS

TYPICAL APPLICATION DATA

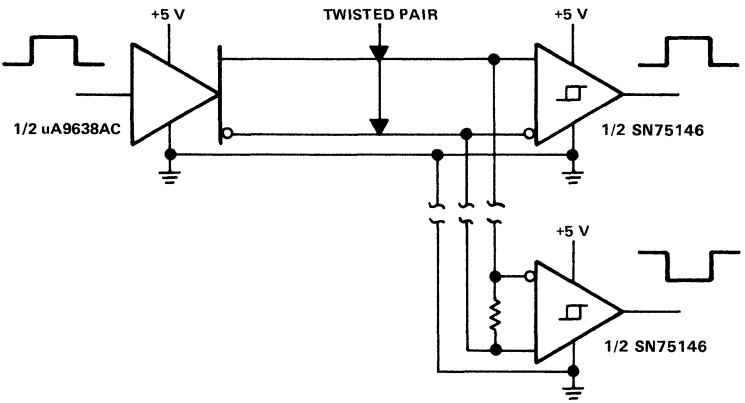


FIGURE 5. RS-422-A SYSTEM APPLICATIONS

D951, JANUARY 1971—REVISED MAY 1990

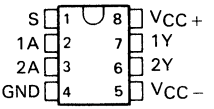
- **Satisfies Requirement of EIA Standard RS-232-C**
- **Withstands Sustained Output Short-Circuit to any Low-Impedance Voltage Between −25 V and 25 V**
- **2-μs Max Transition Time Through the 3 V to −3 V Transition Region Under Full 2500-pF Load**
- **Inputs Compatible With Most TTL Families**
- **Common Strobe Input**
- **Inverting Output**
- **Slew Rate Can Be Controlled With an External Capacitor at the Output**
- **Standard Supply Voltages . . . ±12 V**

description

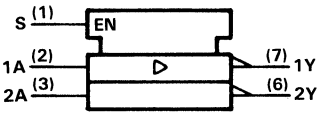
The SN75150 is a monolithic dual line driver designed to satisify the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA standard RS-232-C. A rate of 20,000 bits per second can be transmitted with a full 2500-pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL families. Operation is from 12-V and −12-V power supplies.

The SN75150 is characterized for operation from 0°C to 70°C.

D, JG, OR P PACKAGE
(TOP VIEW)

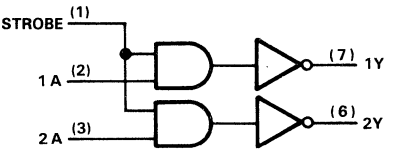


logic symbol†

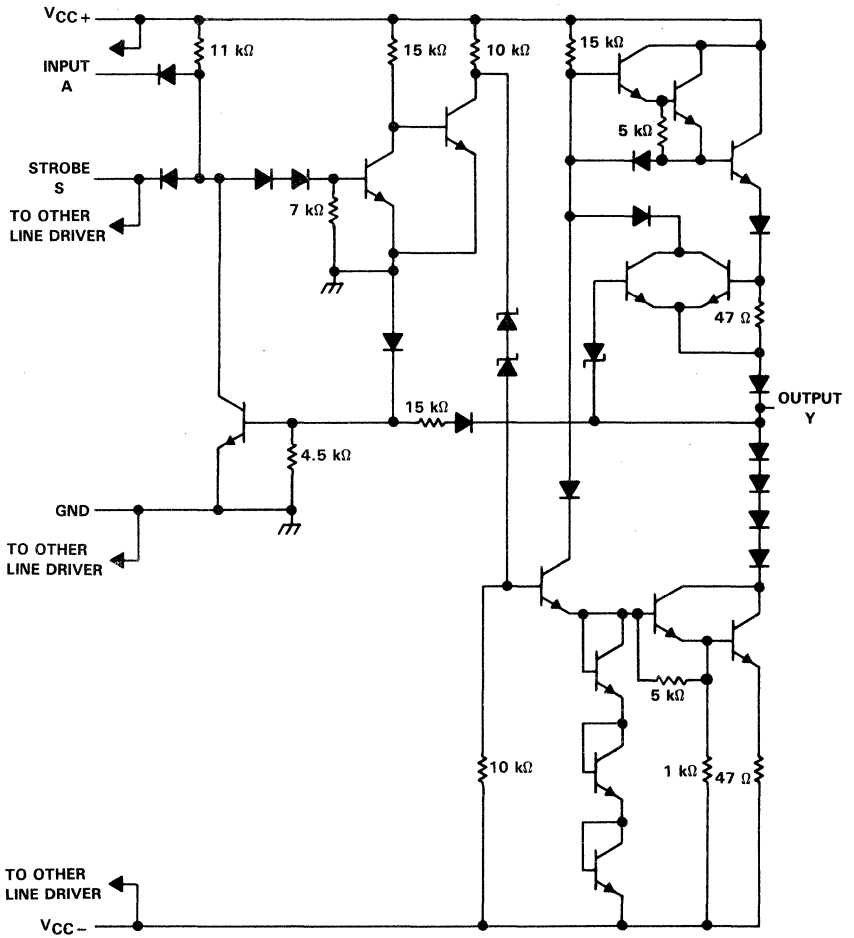


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

logic diagram (positive logic)



schematic (each line driver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC-} . . . . . −15 V
Input voltage . . . . . 15 V
Applied output voltage . . . . . ±25 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
JG	825 mW	6.6 mW/°C	528 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	10.8	12	13.2	V
Supply voltage, V_{CC-}	−10.8	−12	−13.2	V
High-level input voltage, V_{IH}	2		5.5	V
Low-level input voltage, V_{IL}	0		0.8	V
Applied output voltage, V_O			±15	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

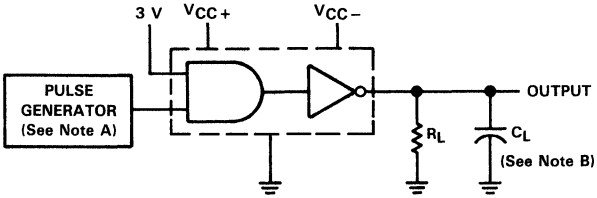
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC+} = 10.8 V, V_{CC-} = −13.2 V, V_{IL} = 0.8 V, R_L = 3 kΩ to 7 kΩ		5	8		V
V_{OL}	Low-level output voltage (see Note 2)	V_{CC+} = 10.8 V, V_{CC-} = −10.8 V, V_{IH} = 2 V, R_L = 3 kΩ to 7 kΩ			−8	−5	V
I_{IH}	High-level input current	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 2.4 V	Data input		1	10	μA
			Strobe input		2	20	
I_{IL}	Low-level input current	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 0.4 V	Data input		−1	−1.6	mA
			Strobe input		−2	−3.2	
I_{OS}	Short-circuit output current‡	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V	V_O = 25 V		2	8	mA
			V_O = −25 V		−3	−8	
			V_O = 0, V_I = 3 V	10	15	30	
			V_O = 0, V_I = 0	−10	−15	−30	
I_{CCH+}	Supply current from V_{CC+}, high-level output	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 0, R_L = 3 kΩ, T_A = 25°C			10	22	mA
I_{CCH-}	Supply current from V_{CC-}, high-level output				−1	−10	
I_{CCL+}	Supply current from V_{CC+}, low-level output	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 3 V, R_L = 3 kΩ, T_A = 25°C			8	17	mA
I_{CCL-}	Supply current from V_{CC-}, low-level output				−9	−20	

† All typical values are at V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time.
NOTE 2: The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic levels only, e.g., when −5 V is the maximum, the typical value is a more negative voltage.

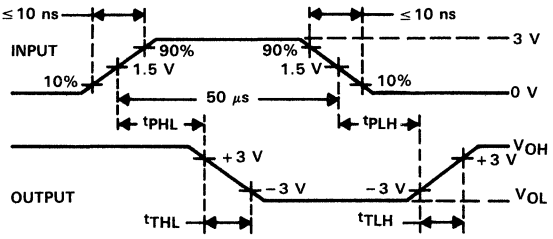
switching characteristics, V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C (see Figure 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{TLH}	Transition time, low-to-high-level output	C_L = 2500 pF, R_L = 3 kΩ to 7 kΩ	0.2	1.4	2	μs
t_{THL}	Transition time, high-to-low-level output		0.2	1.5	2	μs
t_{TLH}	Transition time, low-to-high-level output	C_L = 15 pF, R_L = 7 kΩ		40		ns
t_{THL}	Transition time, high-to-low-level output			20		ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 7 kΩ		60		ns
t_{PHL}	Propagation delay time, high-to-low-level output			45		ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 50%, $Z_O \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

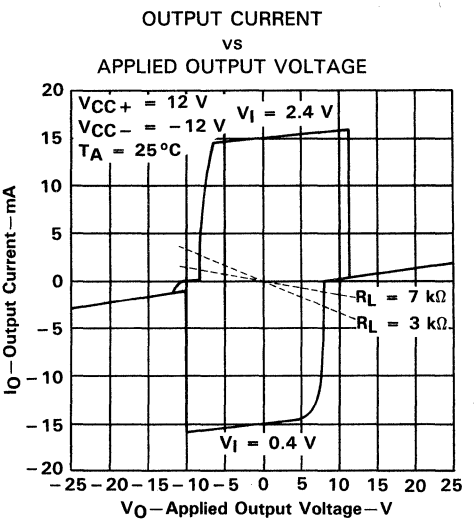


FIGURE 2

APPLICATION INFORMATION

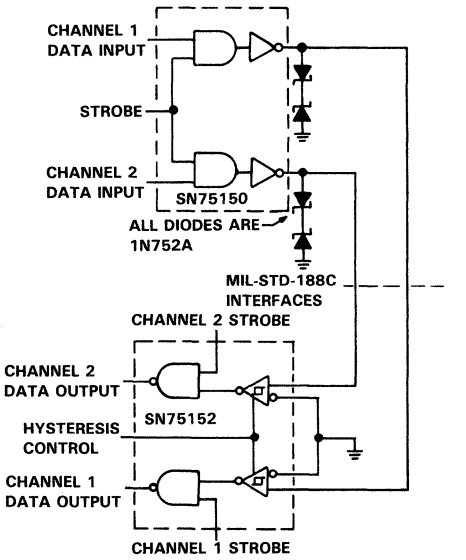
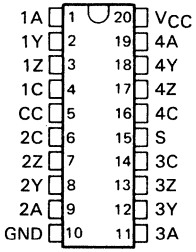


FIGURE 3. DUAL-CHANNEL SINGLE-ENDED INTERFACE CIRCUIT MEETING MIL-STD-188C, PARAGRAPH 7.2.

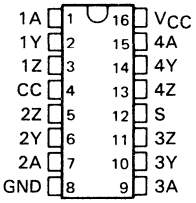
D2453, DECEMBER 1978—REVISED OCTOBER 1986

- **Meets EIA Standard RS-422-A**
- **High-Impedance Output State for Party-Line Operation**
- **High Output Impedance in Power-Off Condition**
- **Low Input Current to Minimize Loading**
- **Single 5-V Supply**
- **40-mA Sink- and Source-Current Capability**
- **High-Speed Schottky Circuitry**
- **Low Power Requirements**

SN75151
DW, J, OR N PACKAGE
(TOP VIEW)



SN75153
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

These line drivers are designed to provide differential signals with high current capability on balanced lines. These circuits provide strobe and enable inputs to control all four drivers, and the SN75151 provides an additional enable input for each driver. The output circuits have active pull-up and pull-down and are capable of sinking or sourcing 40 milliamperes.

The SN75151 and SN75153 meet all requirements of EIA Standard RS-422-A and Federal Standard 1020. They are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

SN75151

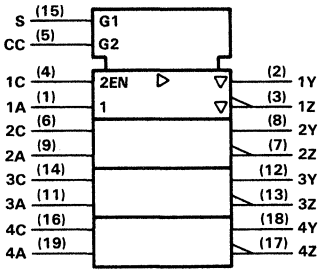
INPUTS				OUTPUTS	
ENABLE CC	ENABLE C	STROBE S	DATA A	Y	Z
L	X	X	X	Z	Z
X	L	X	X	Z	Z
H	H	L	X	L	H
H	H	X	L	L	H
H	H	H	H	H	L

SN75153

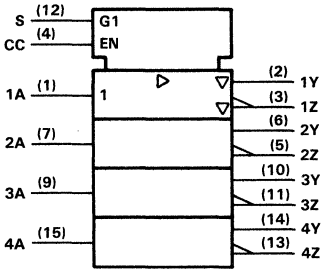
INPUTS			OUTPUTS	
ENABLE CC	STROBE S	DATA A	Y	Z
L	X	X	Z	Z
H	L	X	L	H
H	X	L	L	H
H	H	H	H	L

logic symbols†

SN75151



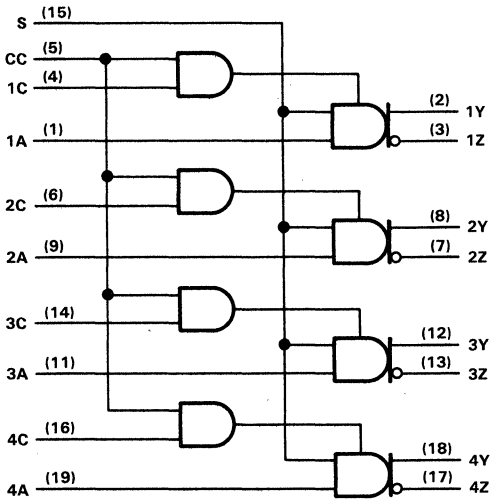
SN75153



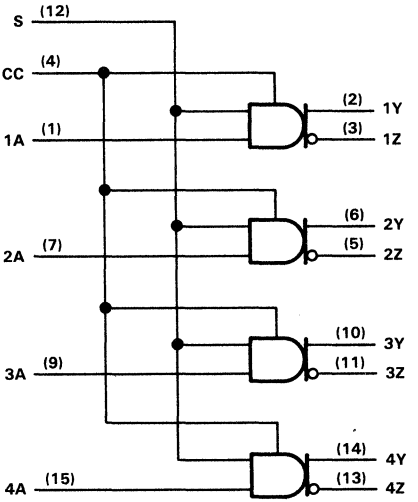
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

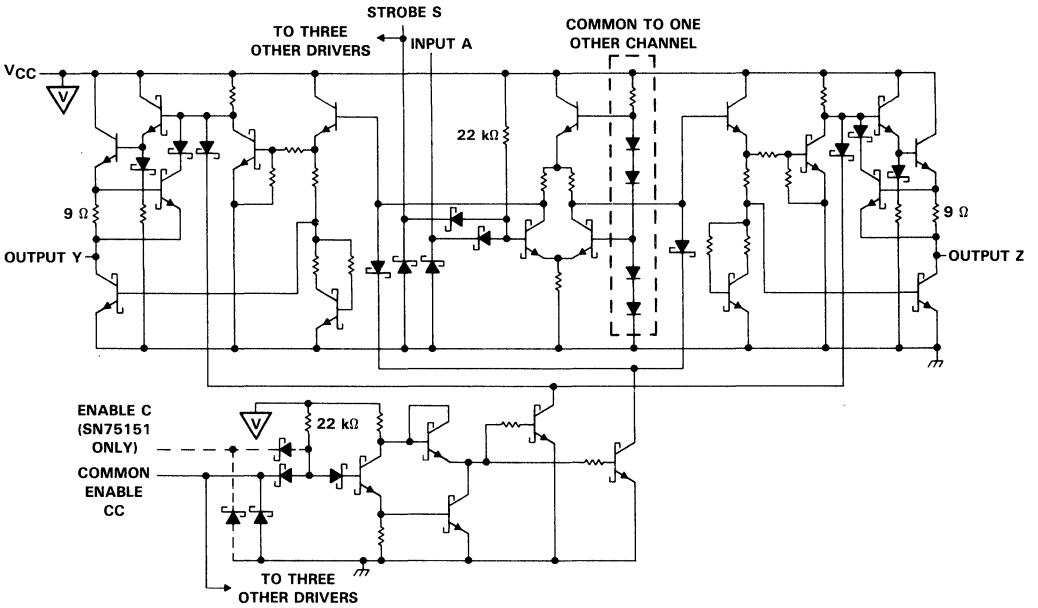
SN75151



SN75153



schematic



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
DW package . . . . . 1125 mW
J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

NOTES: 1. All voltage values, except differential output voltage V_{OD}, are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the DW package at the rate of 9 mW/°C, the J package at the rate of 8.2 mW/°C, and the N package at the rate of 9.2 mW/°C. In the J package, the chips are glass mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}	−0.25		6	V
High-level output current, I_{OH}			−40	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA	CC, S			−2	V
			All others		−0.9	−1.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = −20 mA	2.5			V
			I_{OH} = −40 mA	2.4			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = MAX, I_{OL} = 40 mA			0.5	V
$\|V_{OD1}\|$	Differential output voltage	V_{CC} = MAX,	I_O = 0		3.4	$2V_{OD2}$	V
$\|V_{OD2}\|$	Differential output voltage	V_{CC} = MIN	R_L = 100 Ω, See Figure 1	2	2.8		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§	V_{CC} = MIN			±0.01	±0.4	V
V_{OC}	Common-mode output voltage¶	V_{CC} = MAX			1.8	3	V
		V_{CC} = MIN			1.6	3	
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§	V_{CC} = MIN or MAX			±0.02	±0.4	V
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MAX, Enable at 0.8 V	V_O = 0.5 V			−20	μA
			V_O = 2.5 V			20	
			V_O = V_{CC}			20	
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V		0.1	100	μA
			V_O = −0.25 V		−0.1	−100	
			V_O = −0.25 V to 6 V			±100	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V	C('151), A			20	μA
			CC, S			80	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	C ('151), A			−0.36	mA
			CC,S			−1.6	
I_{OS}	Short-circuit output current#	V_{CC} = MAX		−50	−90	−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = MAX, No load	Outputs disabled		30	60	mA
			Outputs enabled		60	80	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C and V_{CC} = 5 V except for V_{OC}, for which V_{CC} is as stated under test conditions.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitudes of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
# Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 2, Termination A		15	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			15	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 2, Termination B		13	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			13	25	ns
t_{TLH}	Transition time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 2, Termination A		12	20	ns
t_{THL}	Transition time, high-to-low-level output			12	20	ns
t_{PZH}	Outut enable time to high level	C_L = 30 pF, R_L = 60 Ω, See Figure 3		18	35	ns
t_{PZL}	Output enable time to low level	C_L = 30 pF, R_L = 111 Ω, See Figure 4		20	35	ns
t_{PHZ}	Output disable time from high level	C_L = 30 pF, R_L = 60 Ω, See Figure 3		19	30	ns
t_{PLZ}	Output disable time from low level	C_L = 30 pF, R_L = 111 Ω, See Figure 4		13	30	ns
	Overshoot factor	R_L = 100 Ω, See Figure 2, Termination C			10	%

†All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

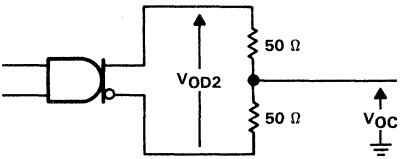
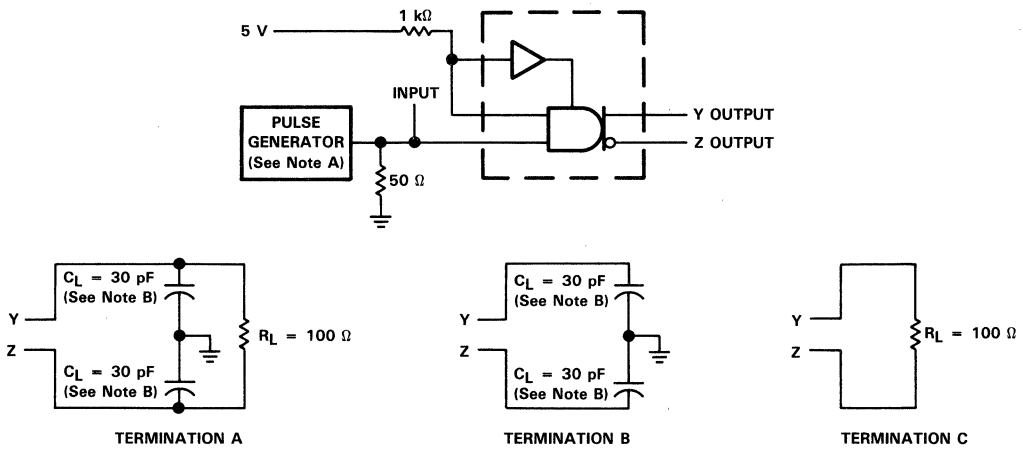
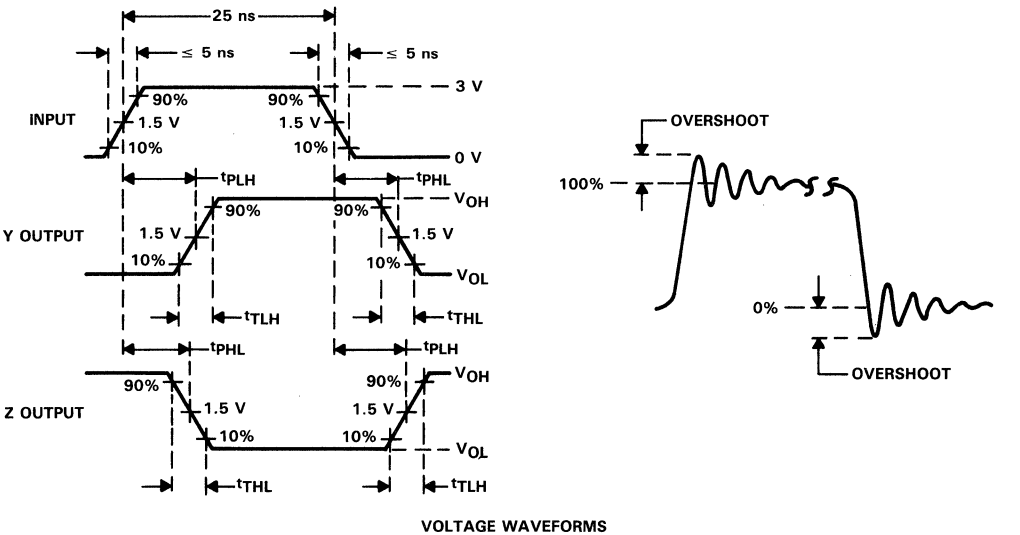


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUITS

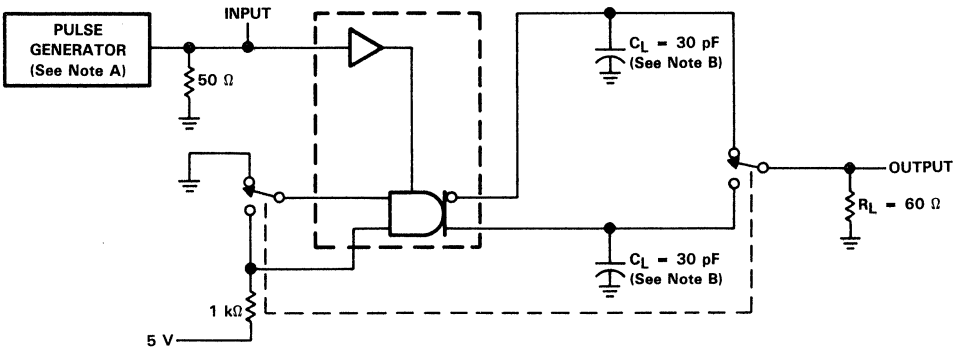


VOLTAGE WAVEFORMS

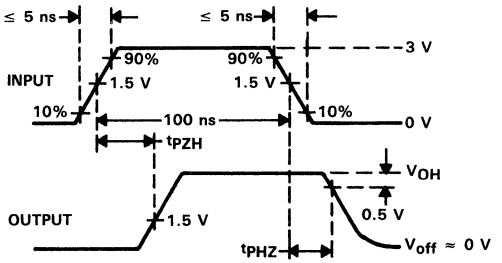
NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, PRR ≤ 10 MHz.
B. C_L includes probe and jig capacitance.

FIGURE 2. t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, AND OVERSHOOT FACTOR

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

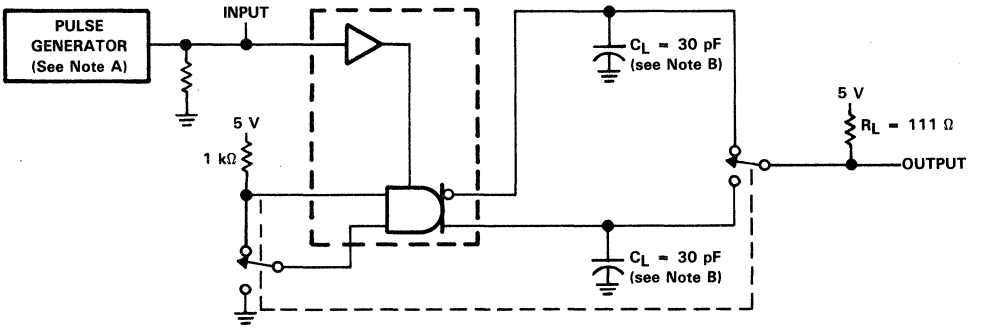


VOLTAGE WAVEFORMS

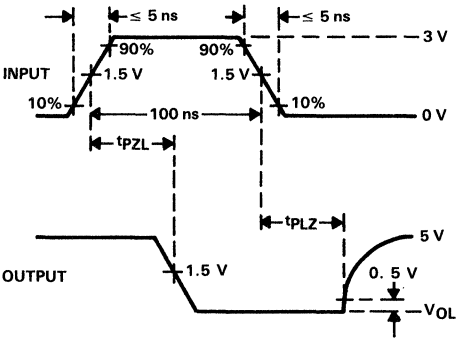
FIGURE 3. t_{PZH} AND t_{PHZ}

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4. t_{PZL} AND t_{PLZ}

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

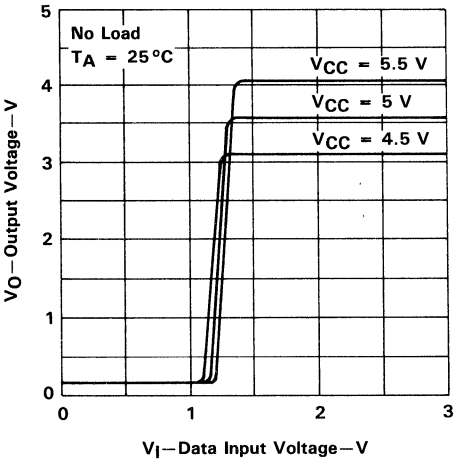


FIGURE 5

Y OR Z OUTPUT VOLTAGE
vs
ENABLE INPUT VOLTAGE

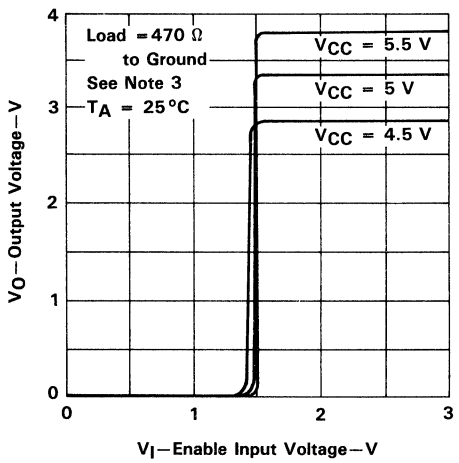


FIGURE 6

Y OR Z OUTPUT VOLTAGE
vs
ENABLE INPUT VOLTAGE

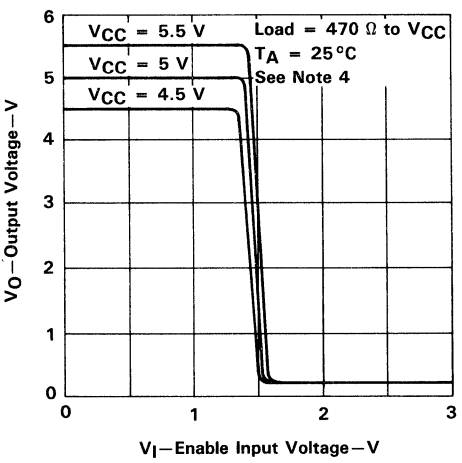


FIGURE 7

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.
4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

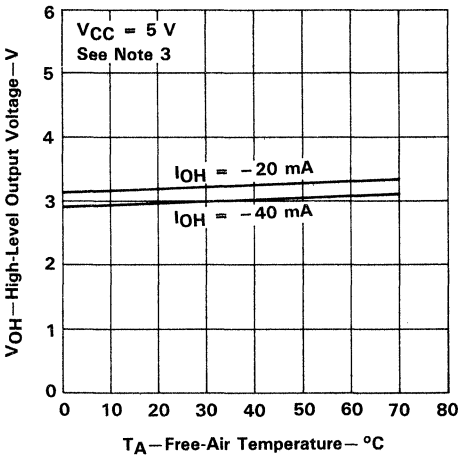


FIGURE 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

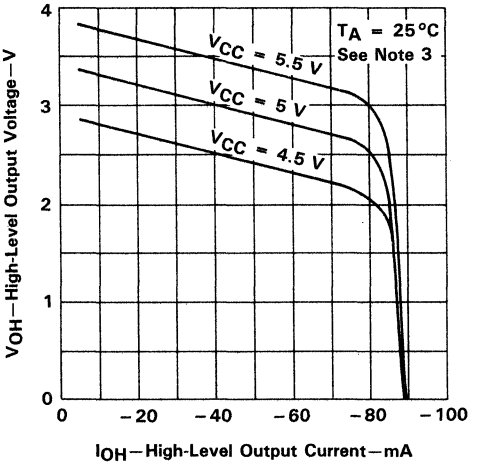


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

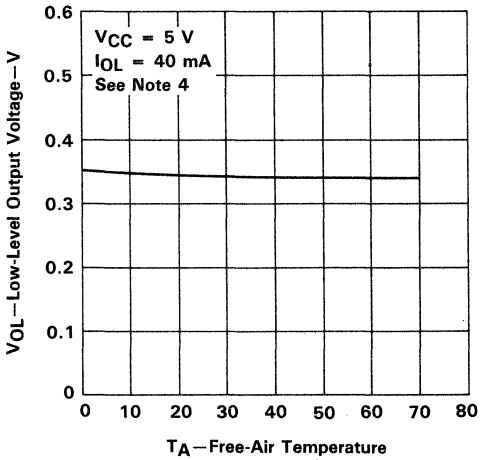


FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

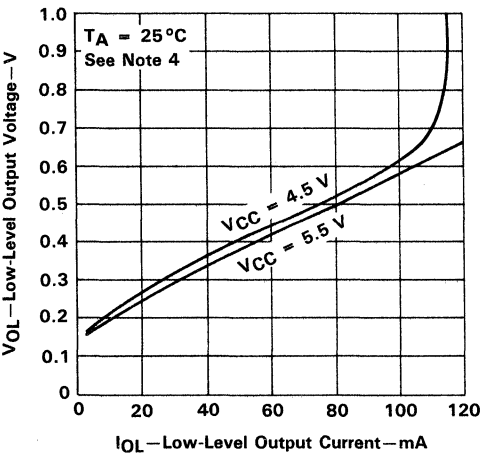


FIGURE 11

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.
4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z inputs.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

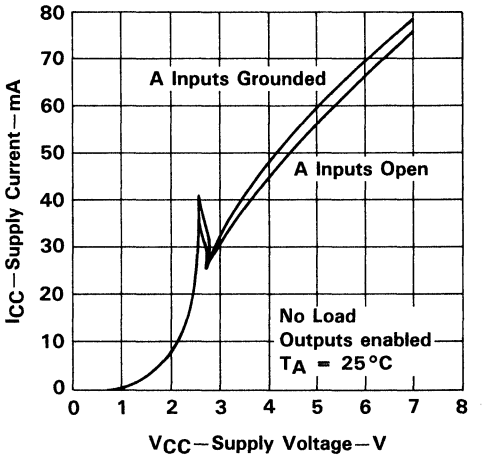


FIGURE 12

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

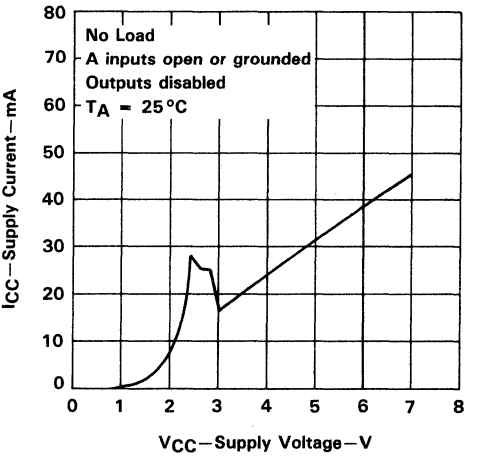


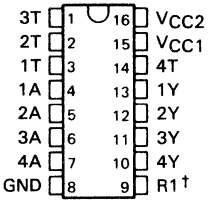
FIGURE 13

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.
4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z inputs.

D899, NOVEMBER 1970—REVISED MAY 1990

- **Satisfies Requirements of EIA Standard RS-232-C**
- **Input Resistance . . . 3 kΩ to 7 kΩ over Full RS-232-C Voltage Range**
- **Input Threshold Adjustable to Meet "Fail-Safe" Requirements Without Using External Components**
- **Built-In Hysteresis for Increased Noise Immunity**
- **Inverting Output Compatible With TTL**
- **Output With Active Pull-Up for Symmetrical Switching Speeds**
- **Standard Supply Voltages . . . 5 V or 12 V**

D, J, OR N PACKAGE
(TOP VIEW)



†For function of R1, see schematic

description

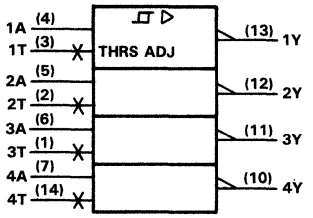
The SN75154 is a monolithic Low-Power Schottky line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA standard RS-232-C. Other applications are for relatively short, single-line, point-to-point data transmission and for level translators. Operation is normally from a single 5-V supply; however, a built-in option allows operation from a 12-V supply without the use of additional components. The output is compatible with most TTL circuits when either supply voltage is used.

In normal operation, the threshold-control terminals are connected to the V_{CC1} terminal, even if power is being supplied via the alternate V_{CC2} terminal. This provides a wide hysteresis loop, which is the difference between the positive-going and negative-going threshold voltages. See typical characteristics. In this mode of operation, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

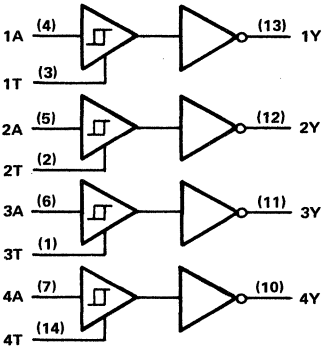
The SN75154 is characterized for operation from 0°C to 70°C.

logic symbol†

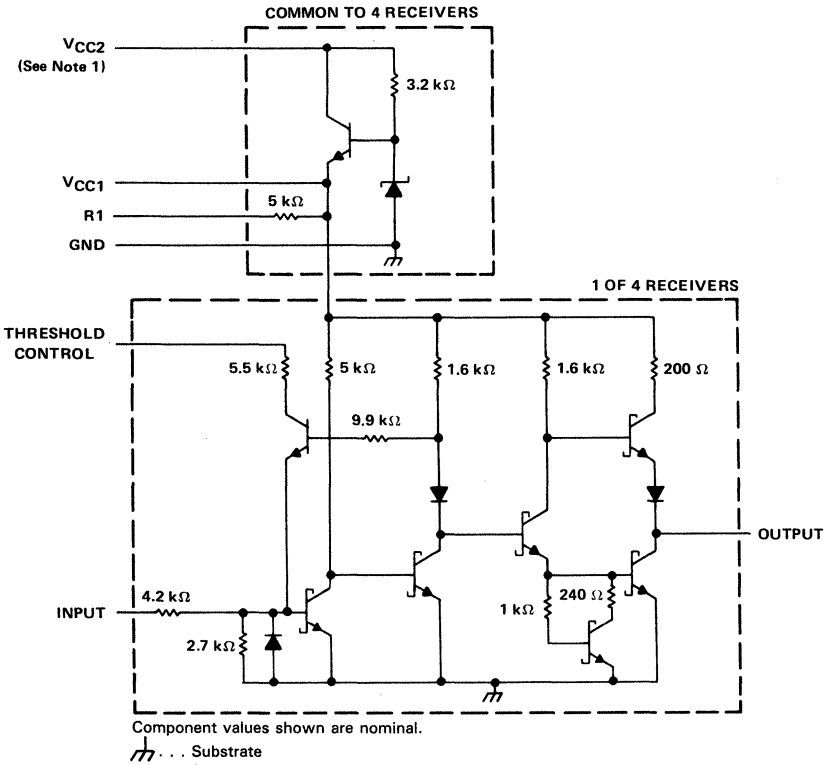


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematic



NOTE 1: When V_{CC1} is used, V_{CC2} may be left open or shorted to V_{CC1}. When V_{CC2} is used, V_{CC1} must be left open or connected to the threshold control pins.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Normal supply voltage, V_{CC1} (see Note 2) . . . . . 7 V
Alternate supply voltage, V_{CC2} . . . . . 14 V
Input voltage . . . . . ±25 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Normal supply voltage, V_{CC1}	4.5	5	5.5	V
Alternate supply voltage, V_{CC2}	10.8	12	13.2	V
High-level input voltage, V_{IH} (see Note 3)	3		15	V
Low-level input voltage, V_{IL} (see Note 3)	−15		−3	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

NOTES: 2. Voltage values are with respect to network ground terminal.
3. The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic and threshold levels only, e.g., when 0 V is the maximum, the minimum limit is a more negative voltage.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{T+}	Positive-going threshold voltage	Normal operation	1		0.8	2.2	3	V
		Fail-safe operation			0.8	2.2	3	
V_{T-}	Negative-going threshold voltage	Normal operation	1		−3	−1.1	0	V
		Fail-safe operation			0.8	1.4	3	
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Normal operation	1		0.8	3.3	6	V
		Fail-safe operation			0	0.8	2.2	
V_{OH}	High-level output voltage		1	I_{OH} = −400 μA	2.4	3.5		V
V_{OL}	Low-level output voltage		1	I_{OL} = 16 mA		0.29	0.4	V
r_i	Input resistance		2	ΔV_I = −25 V to −14 V	3	5	7	kΩ
				ΔV_I = −14 V to −3 V	3	5	7	
				ΔV_I = −3 V to 3 V	3	6	8	
				ΔV_I = 3 V to 14 V	3	5	7	
				ΔV_I = 14 V to 25 V	3	5	7	
$V_{I(open)}$	Open-circuit input voltage		3	I_I = 0	0	0.2	2	V
I_{OS}	Short-circuit output current†		4	V_{CC1} = 5.5 V, V_I = −5 V	−10	−20	−40	mA
I_{CC1}	Supply current from V_{CC1}		5	V_{CC1} = 5.5 V, T_A = 25°C		20	35	mA
I_{CC2}	Supply current from V_{CC2}			V_{CC2} = 13.2 V, T_A = 25°C		23	40	

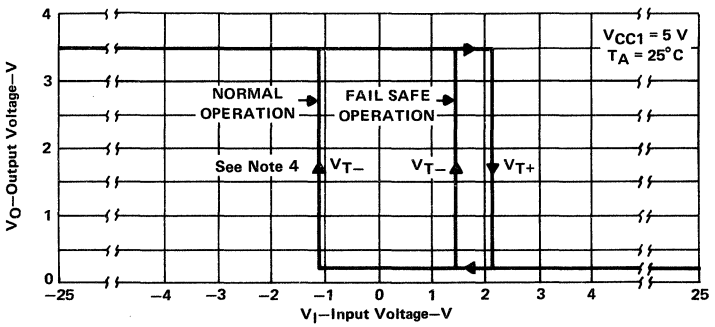
†Not more than one output should be shorted at a time.
‡All typical values are at V_{CC1} = 5 V, T_A = 25°C.

switching characteristics, V_{CC1} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	6	C_L = 50 pF, R_L = 390 Ω		11		ns
t_{PHL}	Propagation delay time, high-to-low-level output				8		ns
t_{TLH}	Transition time, low-to-high-level output				7		ns
t_{THL}	Transition time, high-to-low-level output				2.2		ns

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs INPUT VOLTAGE



NOTE 4: For normal operation, the threshold controls are connectd to V_{CC1}. For fail-safe operation, the threshold controls are open.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

TEST TABLE

TEST	MEASURE	A	T	Y	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open-circuit input	V_{OH}	Open	Open	I_{OH}	4.5 V	Open
(fail safe)	V_{OH}	Open	Open	I_{OH}	Open	10.8 V
V_{T+} min,	V_{OH}	0.8 V	Open	I_{OH}	5.5 V	Open
V_{T-} min (fail safe)	V_{OH}	0.8 V	Open	I_{OH}	Open	13.2 V
V_{T+} min (normal)	V_{OH}	Note A	Pin 15	I_{OH}	5.5 V and T	Open
	V_{OH}	Note A	Pin 15	I_{OH}	T	13.2 V
V_{IL} max,	V_{OH}	−3 V	Pin 15	I_{OH}	5.5 V and T	Open
V_{T-} min (normal)	V_{OH}	−3 V	Pin 15	I_{OH}	T	13.2 V
V_{IH} min, V_{T+} max,	V_{OL}	3 V	Open	I_{OL}	4.5 V	Open
V_{T-} max (fail safe)	V_{OL}	3 V	Open	I_{OL}	Open	10.8 V
V_{IH} min, V_{T+} max	V_{OL}	3 V	Pin 15	I_{OL}	4.5 V and T	Open
(normal)	V_{OL}	3 V	Pin 15	I_{OL}	T	10.8 V
V_{T-} max (normal)	V_{OL}	Note B	Pin 15	I_{OL}	5.5 V and T	Open
	V_{OL}	Note B	Pin 15	I_{OL}	T	13.2 V

NOTES: A. Momentarily apply −5 V, then 0.8 V.
B. Momentarily apply 5 V, then ground.

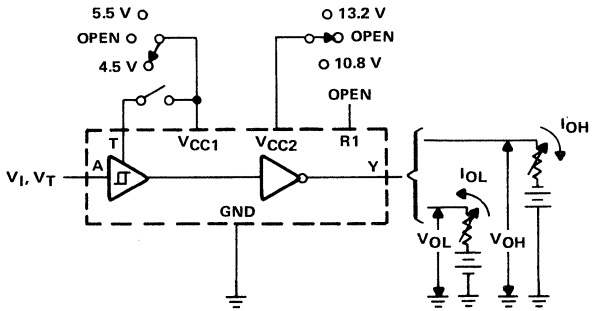
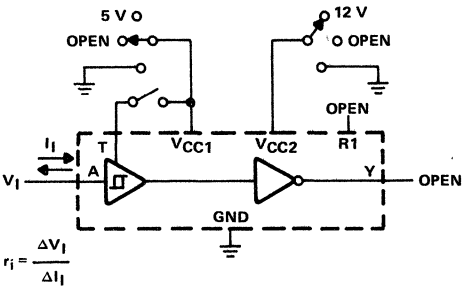


FIGURE 1. V_{IH}, V_{IL}, V_{T+}, V_{T-}, V_{OH}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

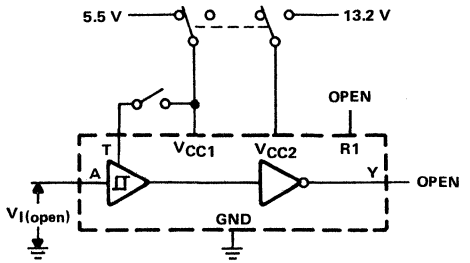
d-c test circuits† (continued)



TEST TABLE

T	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open	5 V	Open
Open	GND	Open
Open	Open	Open
Pin 15	T and 5 V	Open
GND	GND	Open
Open	Open	12 V
Open	Open	GND
Pin 15	T	12 V
Pin 15	T	GND
Pin 15	T	Open

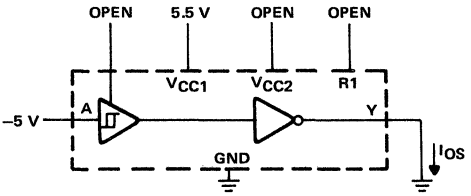
FIGURE 2. r_i



TEST TABLE

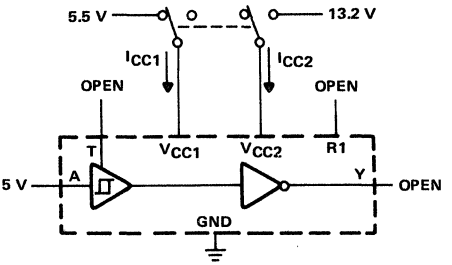
T	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open	5.5 V	Open
Pin 15	5.5 V	Open
Open	Open	13.2 V
Pin 15	T	13.2 V

FIGURE 3. $V_{I(open)}$



Each output is tested separately.

FIGURE 4. I_{OS}



All four line receivers are tested simultaneously.

FIGURE 5. I_{CC}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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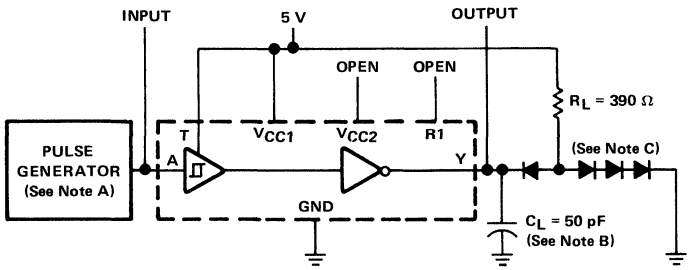
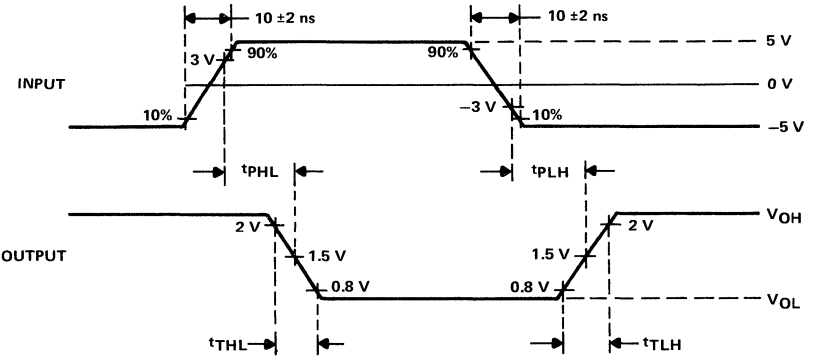
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

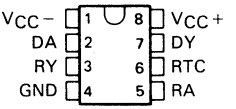
NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, $t_W \leq$ 200 ns, duty cycle ≤ 20%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 6. SWITCHING TIMES

D2951, JULY 1986—REVISED AUGUST 1989

- **Meets EIA Standard RS-232-C**
- **10-mA Current Limited Output**
- **Wide Range of Supply Voltage . . . V_{CC} = 4.5 V to 15 V**
- **Low Power . . . 130 mW**
- **Built-In 5-V Regulator**
- **Response Control Provides:**
  Input Threshold Shifting
  Input Noise Filtering
- **Power-Off Output Resistance . . . 300 Ω Typ**
- **Driver Input TTL Compatible**

D, JG, OR P PACKAGE
(TOP VIEW)

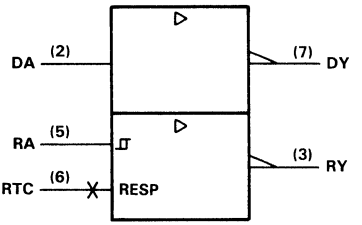


description

The SN75155 is a monolithic line driver and receiver that is designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA standard RS-232-C. A Response Control input is provided for the receiver. A resistor or a resistor and a bias voltage can be connected between the response control input and ground to provide noise filtering. The driver used is similar to the SN75188. The receiver used is similar to the SN75189A.

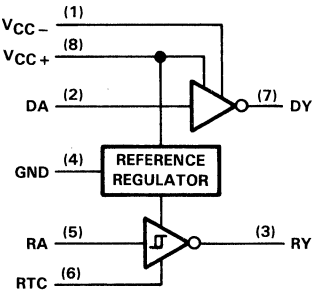
The SN75155 is characterized for operation from 0°C to 70°C.

logic symbol†

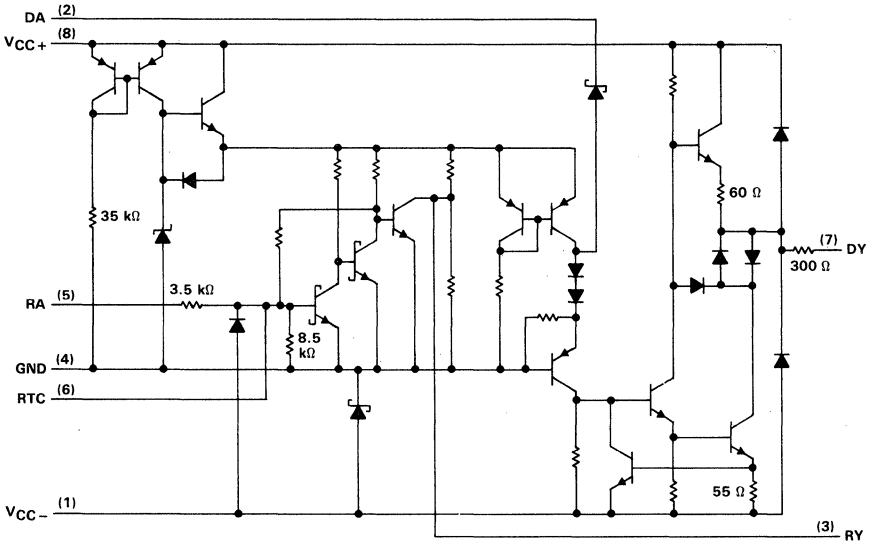


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

logic diagram



schematic



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −15 V
Input voltage range: Driver . . . . . −15 V to 15 V
Receiver . . . . . −30 V to 30 V
Output voltage range (Driver) . . . . . −15 V to 15 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

OTE: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE†	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
JG	825 mW	6.6 mW/°C	528 mW
P	1000 mW	8.0 mW/°C	640 mW

†In the JG package, SN75155 chips are glass mounted.

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4.5	12	15	V
Supply voltage, V_{CC-}	−4.5	−12	−15	V
Input voltage, driver, $V_{I(D)}$			±15	V
Input voltage, receiver, $V_{I(R)}$	−25		25	V
High-level input voltage, driver, V_{IH}	2			V
Low-level input voltage, driver, V_{IL}			0.8	V
Response control current			±5.5	mA
Output current, receiver, $I_{O(R)}$			24	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

total device

PARAMETERS		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
I_{CCH+}	High-level supply current	V_{CC+} = 5 V,	V_{CC-} = −5 V,	$V_{I(D)}$ = 2 V,		6.3	8.1	mA
		V_{CC+} = 9 V,	V_{CC-} = −9 V,	$V_{I(R)}$ = 2.3 V,		9.1	11.9	
		V_{CC+} = 12 V,	V_{CC-} = −12 V,	Output open		10.4	14	
I_{CCL+}	Low-level supply current	V_{CC+} = 5 V,	V_{CC-} = −5 V,	$V_{I(D)}$ = 0.8 V,		2.5	3.4	mA
		V_{CC+} = 9 V,	V_{CC-} = −9 V,	$V_{I(R)}$ = 0.6 V,		3.7	5.1	
		V_{CC+} = 12 V,	V_{CC-} = −12 V,	Output open		4.1	5.6	
I_{CC+}	Supply current	V_{CC+} = 5 V,	V_{CC-} = 0,	$V_{I(R)}$ = 2.3 V,		4.8	6.4	mA
		V_{CC+} = 9 V,	V_{CC-} = 0,	$V_{I(D)}$ = 0		6.7	9.1	
I_{CCH-}	High-level supply current	V_{CC+} = 5 V,	V_{CC-} = −5 V,	$V_{I(D)}$ = 2 V,		−2.4	−3.1	mA
		V_{CC+} = 9 V,	V_{CC-} = −9 V,	$V_{I(R)}$ = 2.3 V,		−3.9	−4.9	
		V_{CC+} = 12 V,	V_{CC-} = −12 V,	Output open		−4.8	−6.1	
I_{CCL-}	Low-level supply current	V_{CC+} = 5 V,	V_{CC-} = −5 V,	$V_{I(D)}$ = 0.8 V,		−0.2	−0.35	mA
		V_{CC+} = 9 V,	V_{CC-} = −9 V,	$V_{I(R)}$ = 0.6 V,		−0.25	−0.4	
		V_{CC+} = 12 V,	V_{CC-} = −12 V,	Output open		−0.27	−0.45	

†All typical values are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 12 V, V_{CC-} = −12 V (unless otherwise noted)

driver section

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ	V_{CC+} = 5 V, V_{CC-} = −5 V	3.2	3.7		V
			V_{CC+} = 9 V, V_{CC-} = −9 V	6.5	7.2		
			V_{CC+} = 12 V, V_{CC-} = −12 V	8.9	9.8		
V_{OL}	Low-Level output voltage (see Note 2)	V_{IH} = 2 V, R_L = 3 kΩ	V_{CC+} = 5 V, V_{CC-} = −5 V		−3.6	−3.2	V
			V_{CC+} = 9 V, V_{CC-} = −9 V		−7.1	−6.4	
			V_{CC+} = 12 V, V_{CC-} = −12 V		−9.7	−8.8	
I_{IH}	High-level input current	V_I = 7 V				5	μA
I_{IL}	Low-level input current	V_I = 0			−0.73	−1.2	mA
I_{OSH}	High-level short-circuit output current	V_I = 0.8 V, V_O = 0		−7	−12	−14.5	mA
I_{OSL}	Low-level short-circuit output current	V_I = 2 V, V_O = 0		6.5	11.5	15	mA
R_O	Output resistance with power off	V_O = −2 V to 2 V			300		Ω

receiver section (see Figure 1)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage			1.2	1.9	2.3	V
V_{T-}	Negative-going threshold voltage			0.6	0.95	1.2	V
V_{hys}	Hysteresis			0.6			V
V_{OH}	High-level output voltage	V_I = 0.6 V, I_{OH} = 10 μA	V_{CC+} = 5 V, V_{CC-} = −5 V	3.7	4.1	4.5	V
			V_{CC+} = 12 V, V_{CC-} = −12 V	4.4	4.7	5.2	
		V_I = 0.6 V, I_{OH} = 0.4 mA	V_{CC+} = 5 V, V_{CC-} = −5 V	3.1	3.4	3.8	
			V_{CC+} = 12 V, V_{CC-} = −12 V	3.6	4	4.5	
V_{OL}	Low-level output voltage	V_I = 2.3 V, I_{OL} = 24 mA			0.2	0.3	V
I_{IH}	High-level input current	V_I = 25 V		3.6	6.7	10	mA
		V_I = 3 V		0.43	0.67	1	mA
I_{IL}	Low-level input current	V_I = −25 V		−3.6	−6.7	−10	mA
		V_I = −3 V		−0.43	−0.67	−1	mA
I_{OS}	Short-circuit output current	V_I = 0.6 V			−2.8	−3.7	mA

†All typical values are at T_A = 25°C.

NOTE 2: The algebraic limit system, in which the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic voltage levels only, e.g., if −8.8 V is the maximum, the typical value is a more negative value.

switching characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, C_L = 50 pF (unless otherwise noted)

driver section (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 3 kΩ		250	480	ns
t_{PHL}	Propagation delay time high-to-low-level output			80	150	
t_r	Output rise time	R_L = 3 kΩ		67	180	ns
		R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF		2.4	3	μs
t_f	Output fall time	R_L = 3 kΩ		48	160	ns
		R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF		1.9	3	μs

receiver section (see Figure 3)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 400 Ω		175	245	ns
t_{PHL}	Propagation delay time, high-to-low-level output			37	100	
t_r	Output rise time	R_L = 400 Ω		255	360	ns
t_f	Output fall time	R_L = 400 Ω		23	50	ns

†All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

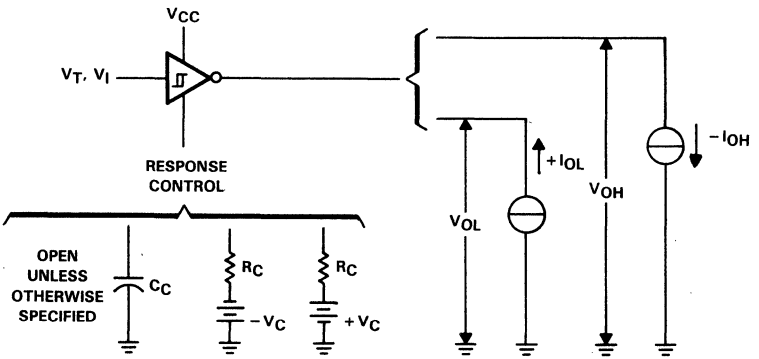
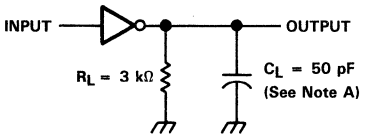
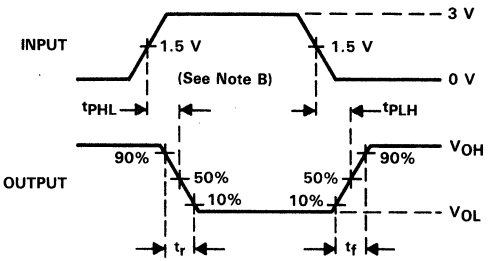


FIGURE 1. RECEIVER SECTION TEST CIRCUIT (V_{T+}, V_{T-}, V_{OH}, V_{OL})

PARAMETER MEASUREMENT INFORMATION



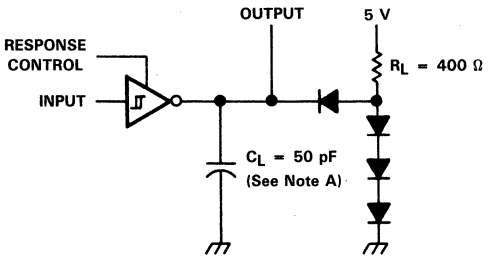
TEST CIRCUIT



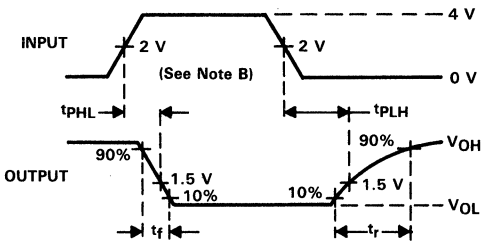
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input waveform is supplied by a generator with the following characteristics: $Z_{out} \approx 50\ \Omega$, $t_w = 1\ \mu s$, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

FIGURE 2. DRIVER SECTION SWITCHING TEST CIRCUIT AND VOLTAGE WAVEFORMS



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input waveform is supplied by a generator with the following characteristics: $Z_{out} \approx 50\ \Omega$, $t_w = 1\ \mu s$, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

FIGURE 3. RECEIVER SECTION SWITCHING TEST CIRCUIT AND VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS (DRIVER)

VOLTAGE TRANSFER CHARACTERISTICS

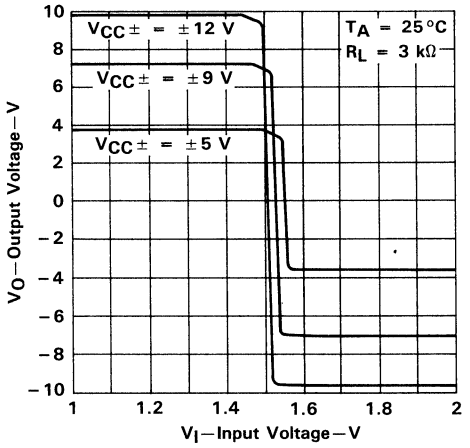


FIGURE 4

OUTPUT CURRENT vs OUTPUT VOLTAGE

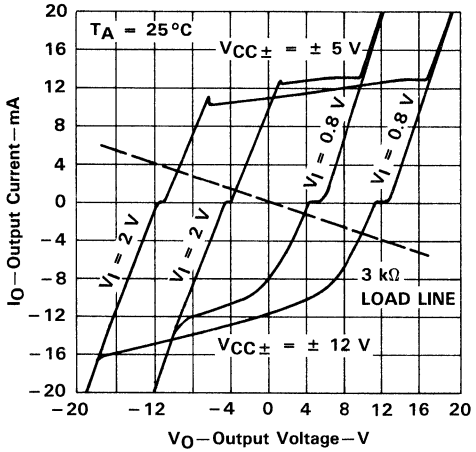


FIGURE 5

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

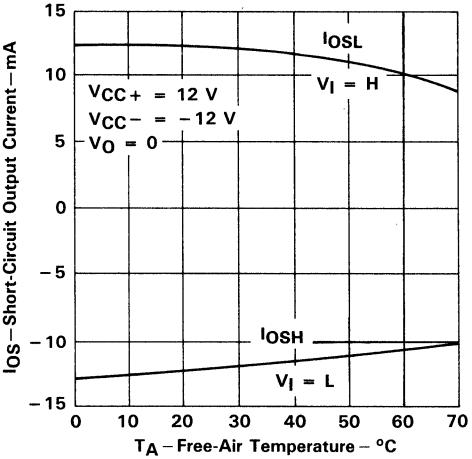


FIGURE 6

SLEW RATE vs LOAD CAPACITANCE

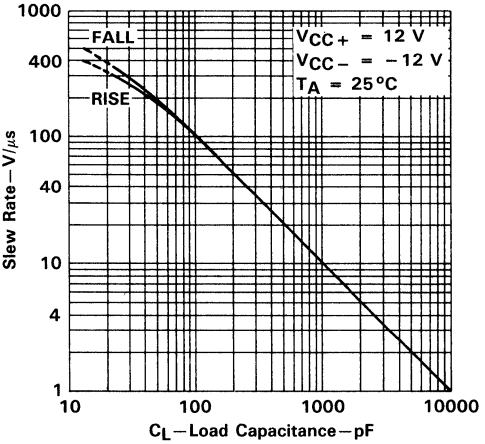


FIGURE 7

TYPICAL CHARACTERISTICS (RECEIVER)

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

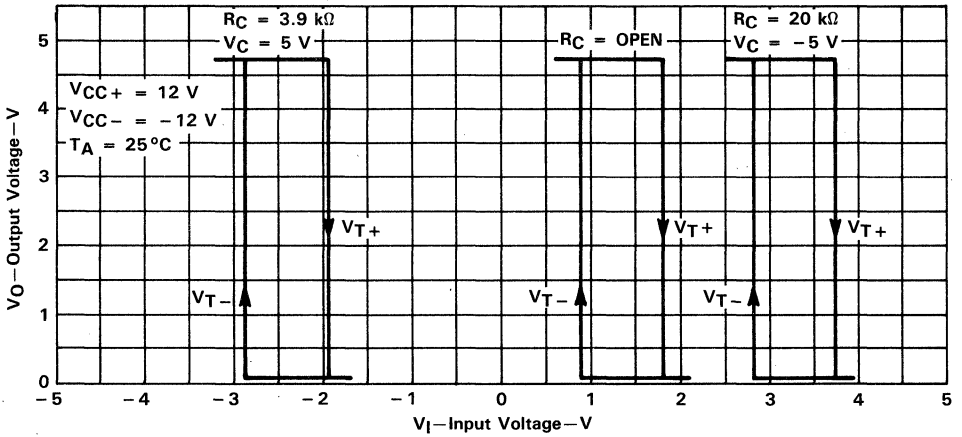


FIGURE 8

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

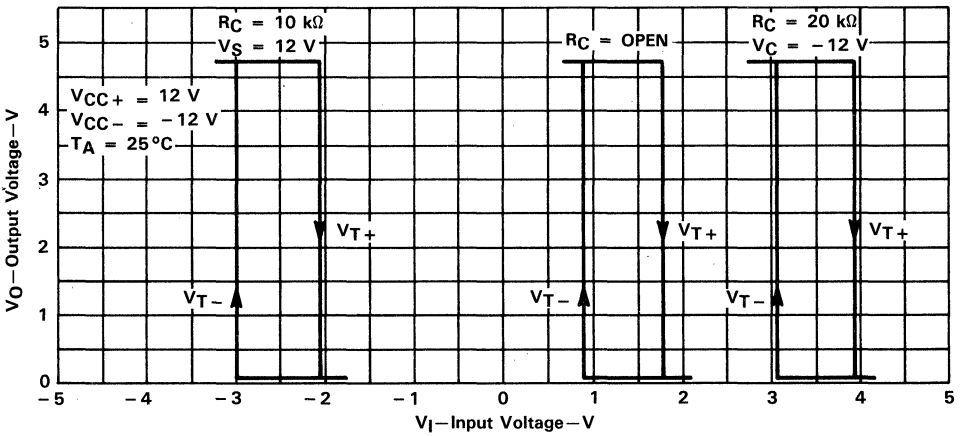


FIGURE 9

TYPICAL CHARACTERISTICS (RECEIVER)

INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

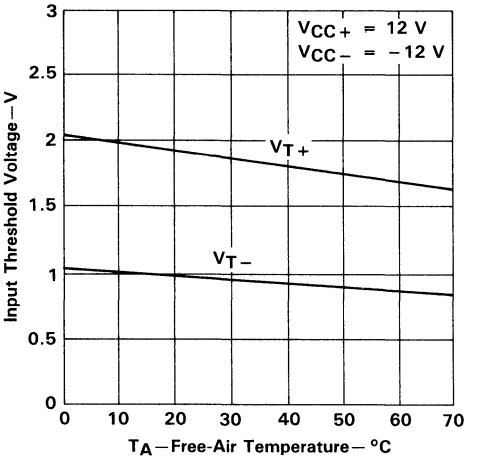


FIGURE 10

INPUT CURRENT
vs
INPUT VOLTAGE

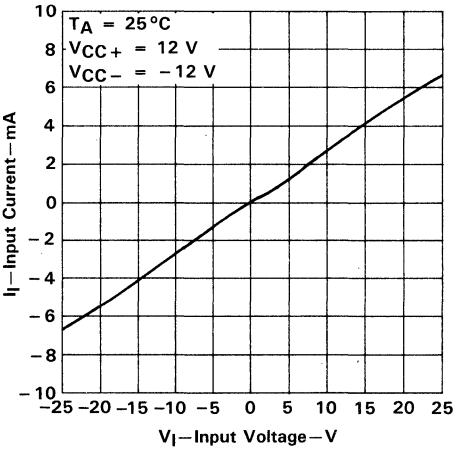


FIGURE 11

NOISE REJECTION

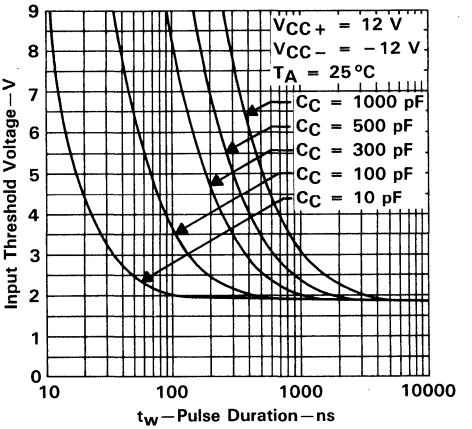


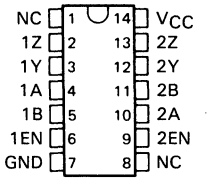
FIGURE 12

SN75159
DUAL DIFFERENTIAL LINE DRIVER WITH 3-STATE OUTPUTS

D2325, JANUARY 1977—REVISED SEPTEMBER 1986

- **Meets EIA Standard RS-422-A**
- **Single 5-V Supply**
- **Balanced Line Operation**
- **TTL-Compatible**
- **High-Impedance Output State for Party-Line Applications**
- **High-Current Active-Pull-Up Outputs**
- **Short-Circuit Protection**
- **Dual Channels**
- **Clamp Diodes at Inputs**

D, J, OR N PACKAGE
(TOP VIEW)



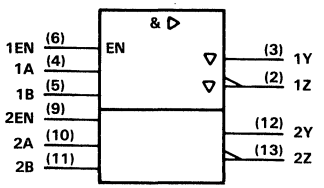
NC—No internal connection

description

The SN75159 dual differential line driver with three-state outputs is designed to provide all the features of the SN75158 line driver with the added feature of driver output controls. There is an individual control for each driver. When the output control is low, the associated outputs are in a high-impedance state and the outputs can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

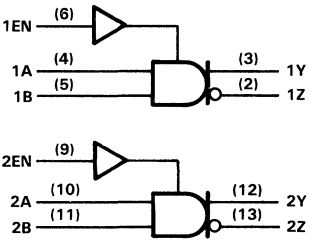
The SN75159 is characterized for operation from 0°C to 70°C.

logic symbol†

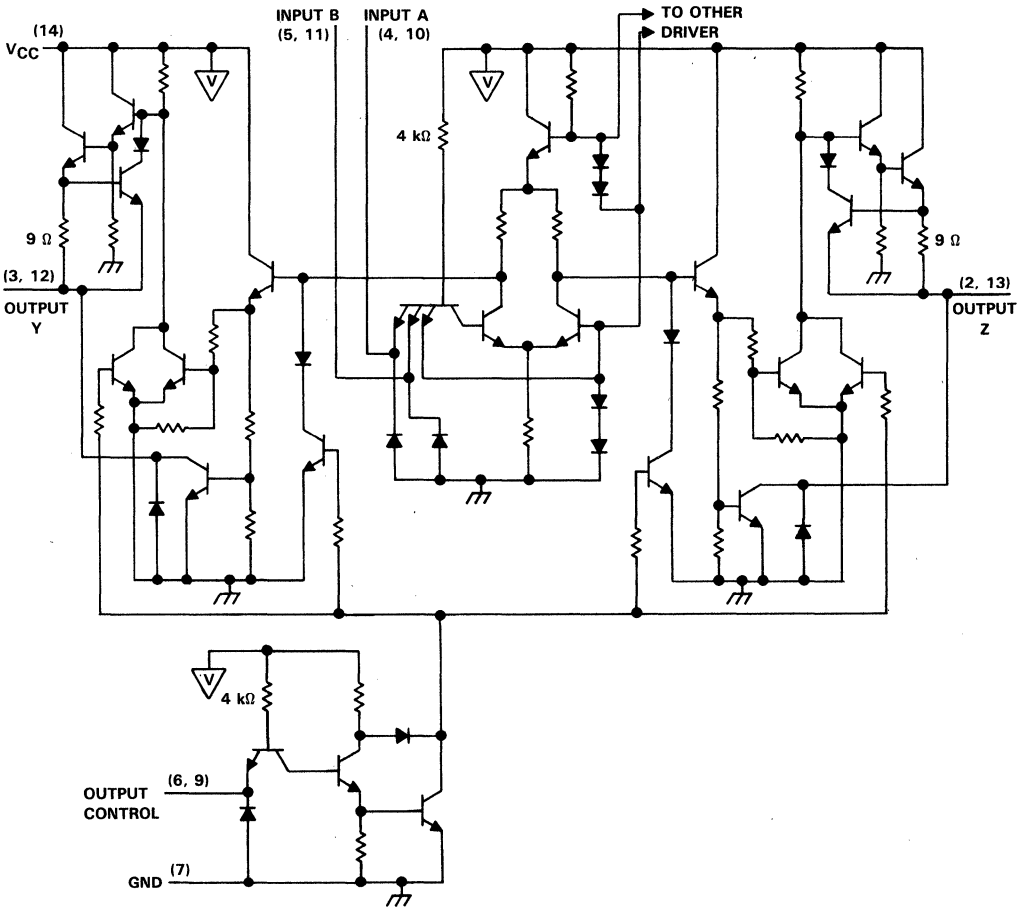


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each driver)



▽ . . . V_{CC} bus

Resistor values shown are nominal.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state voltage applied to open-collector outputs . . . . . 12 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
D package . . . . . 950 mW
J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values except differential output voltage V_{OD} are with respect to the network ground terminal. V_{OD} is at the Y output with respect to the Z output.
2. For operation above 25°C free-air temperature, derate the D package to 608 mW at 70°C at the rate of 7.6 mW/°C, the J package to 656 mW at 70°C at the rate of 8.2 mW/°C, and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75159 chips are glass mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output voltage, I_{OH}			−40	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −12 mA				−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V, V_{IH} = 2 V, I_{OH} = −40 mA			2.4	3.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V, V_{IH} = 2 V, I_{OL} = 40 mA				0.25	0.4	V
V_{OK}	Output clamp voltage	V_{CC} = 5.25 V, I_O = −40 mA				−1.1	−1.5	V
V_O	Output voltage	V_{CC} = 4.75 V to 5.25 V, I_O = 0			0		6	V
$\|V_{OD1}\|$	Differential output voltage	V_{CC} = 5.25 V, I_O = 0				3.5	$2V_{OD2}$	V
$\|V_{OD2}\|$	Differential output voltage	V_{CC} = 4.75 V			2	3.0		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡	V_{CC} = 4.75 V	R_L = 100 Ω, See Figure 1			±0.02	±0.4	V
V_{OC}	Common-mode output voltage§	V_{CC} = 5.25 V	R_L = 100 Ω, See Figure 1			1.8	3	V
		V_{CC} = 4.75 V	R_L = 100 Ω, See Figure 1			1.5	3	
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡	V_{CC} = 4.75 V to 5.25 V	R_L = 100 Ω, See Figure 1			±0.01	±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			0.1	100	μA
			V_O = −0.25 V			−0.1	−100	
			V_O = −0.25 V to 6 V				±100	
I_{OZ}	Off-state (high impedance-state) output current	V_{CC} = 5.25 V, Output controls at 0.8 V	T_A = 25°C,	V_O = 0 to V_{CC}			±10	μA
			T_A = 70°C	V_O = 0			−20	
				V_O = 0.4 V			±20	
				V_O = 2.4 V			±20	
				V_O = V_{CC}			20	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V, V_I = 5.5 V					1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.4 V					40	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.4 V				−1	−1.6	mA
I_{OS}	Short-circuit output current¶	V_{CC} = 5.25 V			−40	−90	−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = 5.25 V, Inputs grounded, T_A = 25°C	No load,			47	65	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C except for V_{OC}, for which V_{CC} is as stated under test conditions.
‡ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitudes of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§ In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
¶ Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics over operating free-air temperature range, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 2, Termination A		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			11	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 2, Termination B		13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	15	ns
t_{TLH}	Transition time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 2, Termination A		4	20	ns
t_{THL}	Transition time, high-to-low-level output			4	20	ns
t_{PZH}	Output enable time to high level	C_L = 30 pF, R_L = 180 Ω, See Figure 3		7	20	ns
t_{PZL}	Output enable time to low level	C_L = 30 pF, R_L = 250 Ω, See Figure 4		14	40	ns
t_{PHZ}	Output disable time from high level	C_L = 30 pF, R_L = 180 Ω, See Figure 3		10	30	ns
t_{PLZ}	Output disable time from low level	C_L = 30 pF, R_L = 250 Ω, See Figure 4		17	35	ns
	Overshoot factor	R_L = 100 Ω, See Figure 2, Termination C			10	%

† All typical values are at T_A = 25°C.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A
V_O	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o
$\|V_{OD2}\|$	V_t
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$

PARAMETER MEASUREMENT INFORMATION

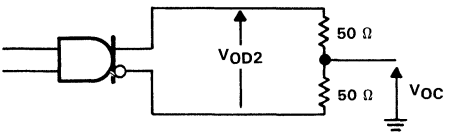
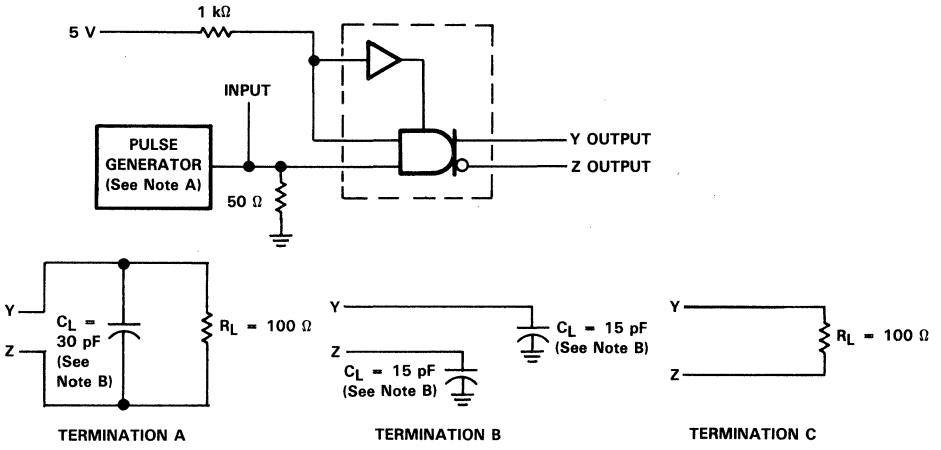
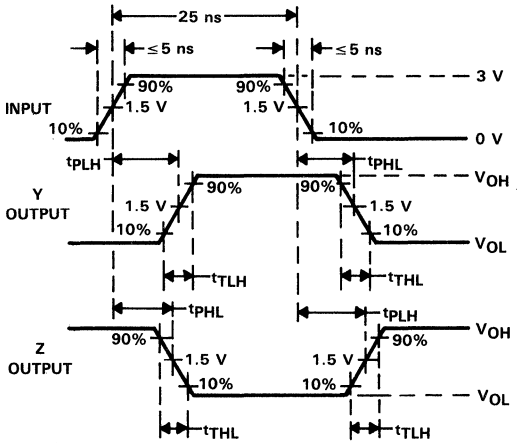


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES

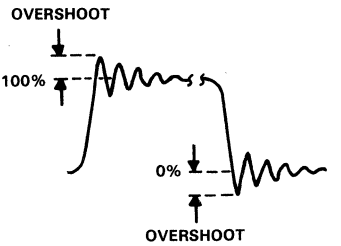
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUITS



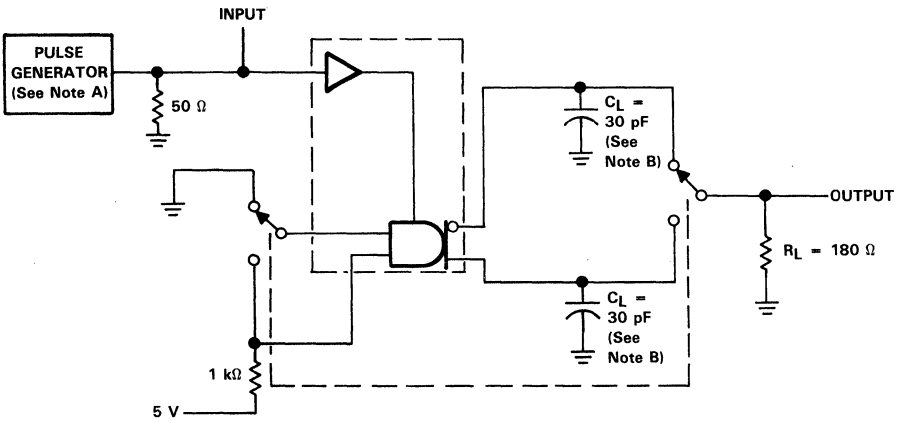
VOLTAGE WAVEFORMS



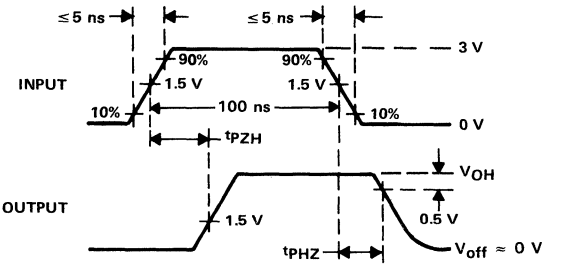
NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, PRR ≤ 10 MHz.
B. C_L includes probe and jig capacitance.

FIGURE 2. t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, AND OVERSHOOT FACTOR

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

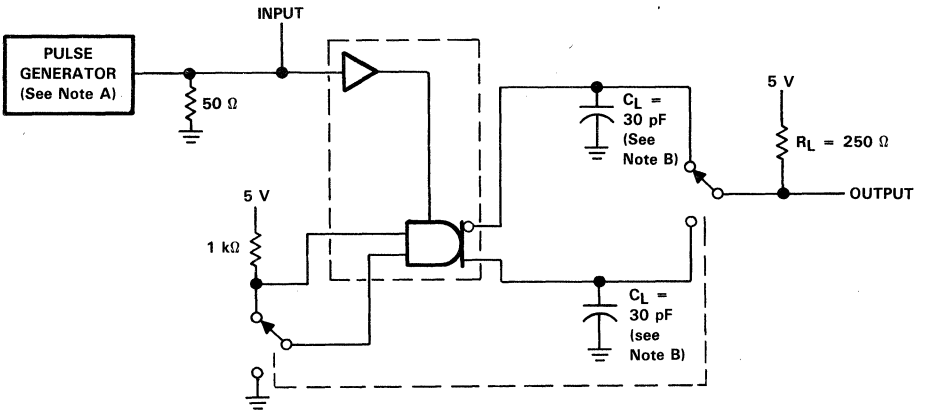


VOLTAGE WAVEFORMS

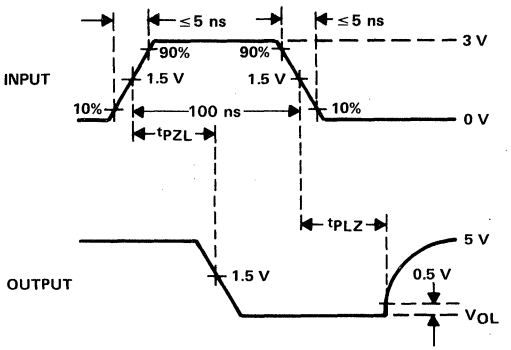
NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

FIGURE 3. t_{PZH} AND t_{PHZ}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, PRR≤ 500 kHz.
C. C_L includes probe and jig capacitance.

FIGURE 4. t_{PZL} AND t_{PLZ}

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

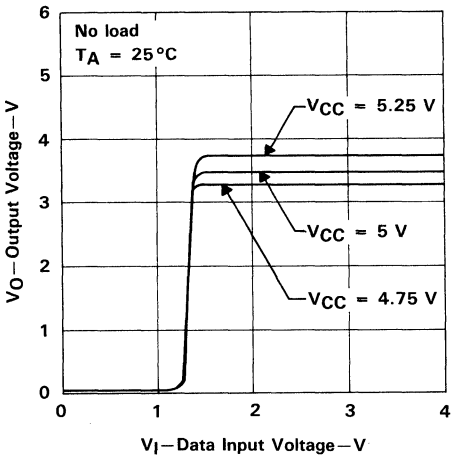


FIGURE 5

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

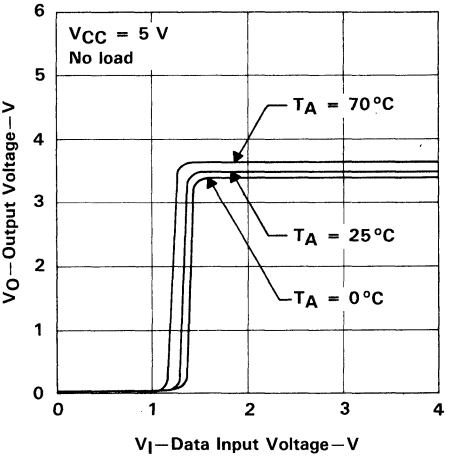


FIGURE 6

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

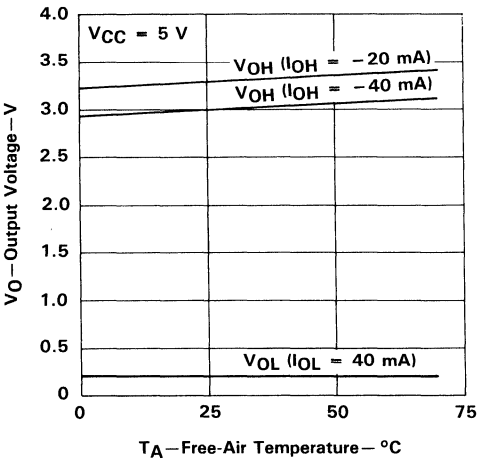


FIGURE 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

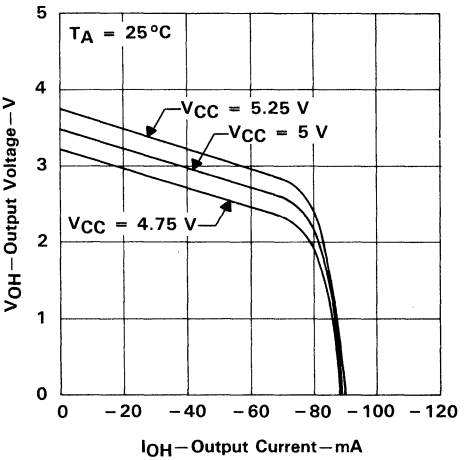


FIGURE 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

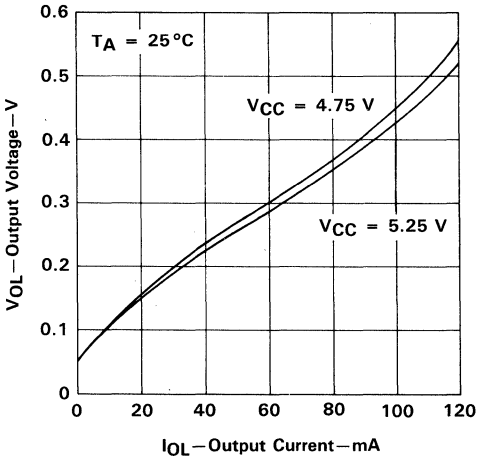


FIGURE 9

SUPPLY CURRENT
(BOTH DRIVERS)
vs
SUPPLY VOLTAGE

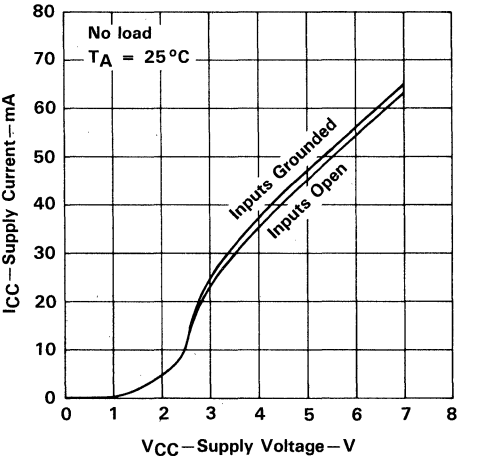


FIGURE 10

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREE-AIR TEMPERATURE

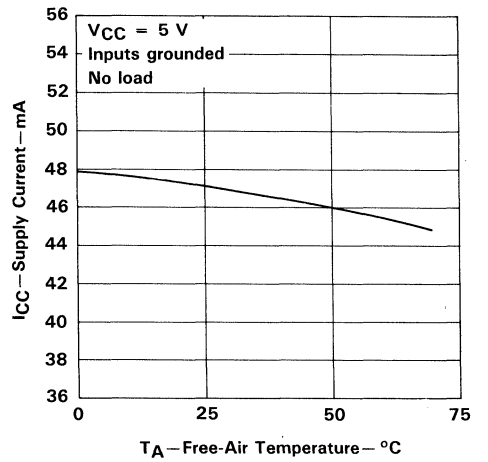


FIGURE 11

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREQUENCY

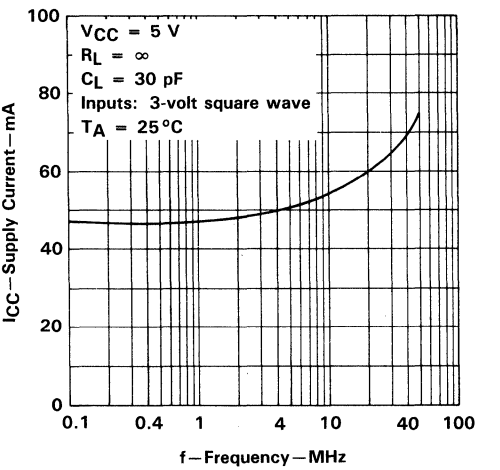


FIGURE 12

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIMES
FROM DATA INPUTS
vs
FREE-AIR TEMPERATURE

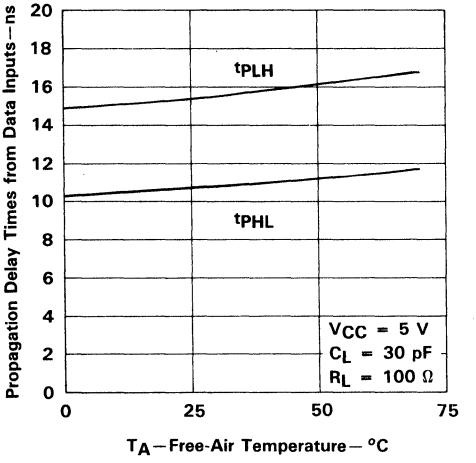


FIGURE 13

OUTPUT ENABLE AND DISABLE TIMES
vs
FREE-AIR TEMPERATURE

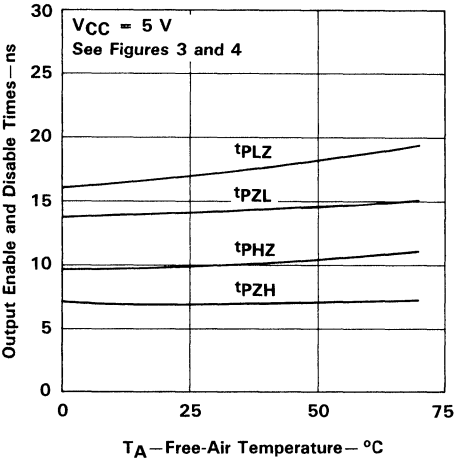
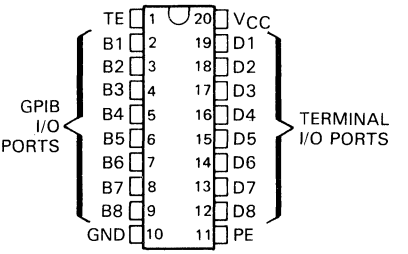


FIGURE 14

MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- Power-Up/Power-Down Protection (Glitch-Free)
- High-Speed, Low-Power Schottky Circuitry
- Low-Power Dissipation . . . 72 mW Max Per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)

DW, J, OR N PACKAGE
(TOP VIEW)



description

The SN75160B 8-channel general-purpose interface bus transceiver is a monolithic, high-speed, low-power Schottky device designed for two-way data communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the passive-pullup or 3-state mode. If Talk Enable (TE) is high, these ports have the characteristics of passive-pullup outputs when Pullup Enable (PE) is low, and of 3-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. The driver outputs are designed to handle loads up to 48 mA of sink current.

Output glitches during power-up and power-down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when V_{CC} = 0. When combined with the SN75161B or SN75162B management bus transceivers, the pair provides the complete 16-wire interface for the IEEE 488 bus.

The SN75160B is characterized for operation from 0°C to 70°C.

FUNCTION TABLES

EACH DRIVER

INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z†
X	L	X	Z†

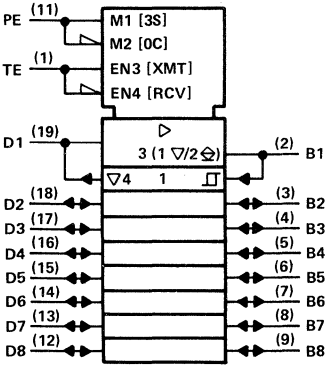
EACH RECEIVER

INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

H = high level, L = low level, X = irrelevant, Z = High-impedance state.

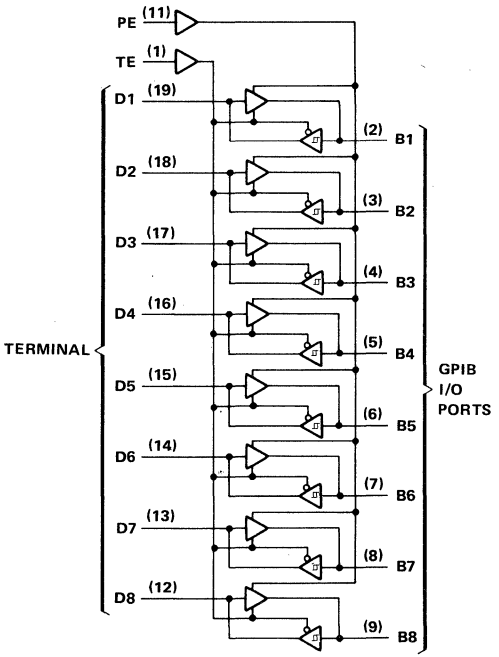
† This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and ground.

logic symbol†



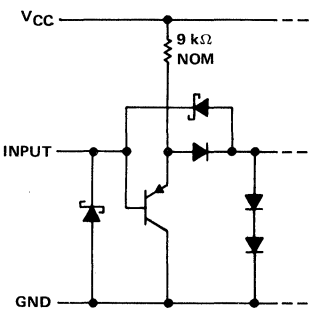
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs.
⏚ Designates passive-pullup outputs.

logic diagram (positive logic)

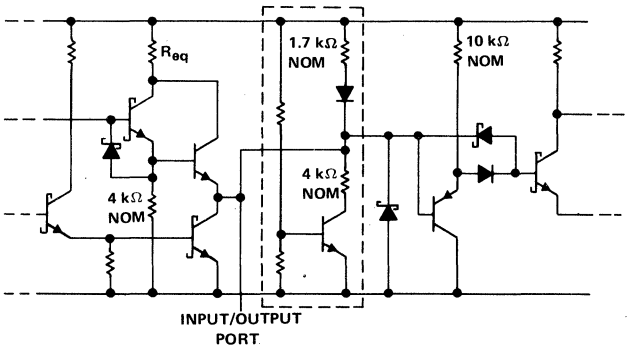


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total power dissipation (see Note 2) . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. In the J package, SN75160B chips are alloy mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
J	1375 mW	11.0 mW/°C	880 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pull-ups active			−5.2	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4	0.65		V
V_{OH}	High-level output voltage	Terminal	I_{OH} = −800 μA,	TE at 0.8 V	2.7	3.5		V
		Bus	I_{OH} = −5.2 mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	TE at 2 V		0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current	Terminal	V_I = 0.5 V			−10	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 to 2.5 V			−40	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load	Receivers low and enabled		70	90	mA
				Drivers low and enabled		85	110	
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0, f = 1 MHz	$V_{I/O}$ = 0 to 2 V,		30		pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					15	22	
t_{PZH}	Output enable time to high level	TE	Bus	See Figure 3		25	35	ns
t_{PHZ}	Output disable time from high level					13	22	
t_{PZL}	Output enable time to low level					22	35	
t_{PLZ}	Output disable time from low level					22	32	
t_{PZH}	Output enable time to high level	TE	Terminal	See Figure 4		20	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level					23	32	
t_{PLZ}	Output disable time from low level					19	30	
t_{en}	Output pull-up enable time	PE	Bus	See Figure 5		15	22	ns
t_{dis}	Output pull-up disable time					13	20	

PARAMETER MEASUREMENT INFORMATION

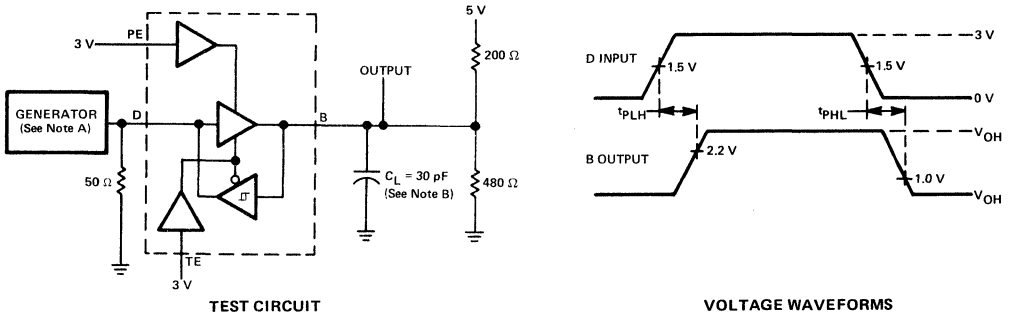


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

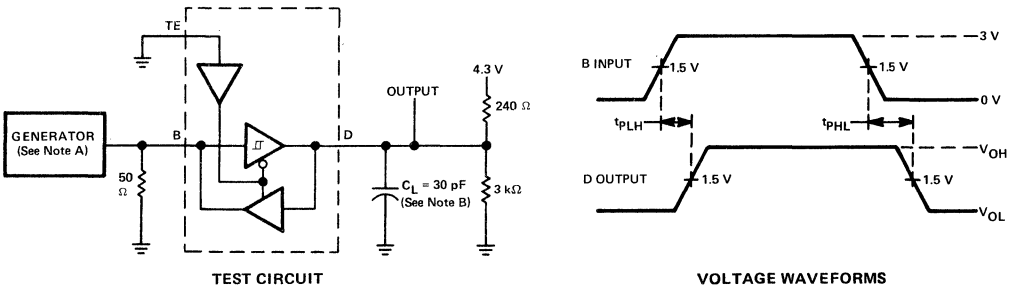


FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

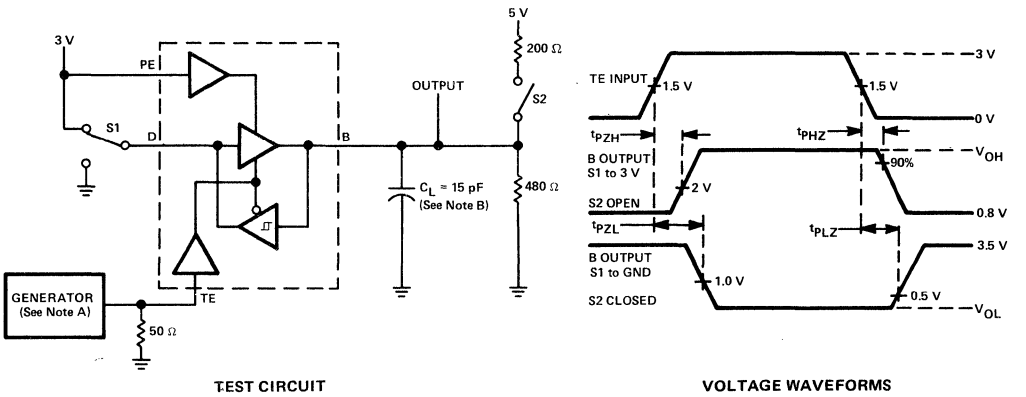


FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

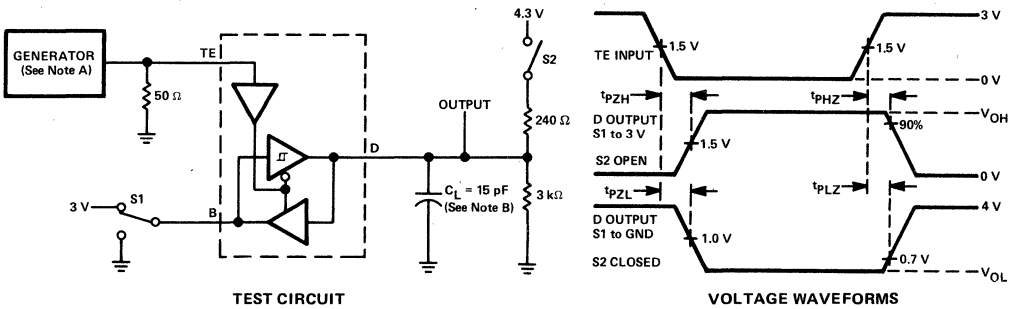


FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES

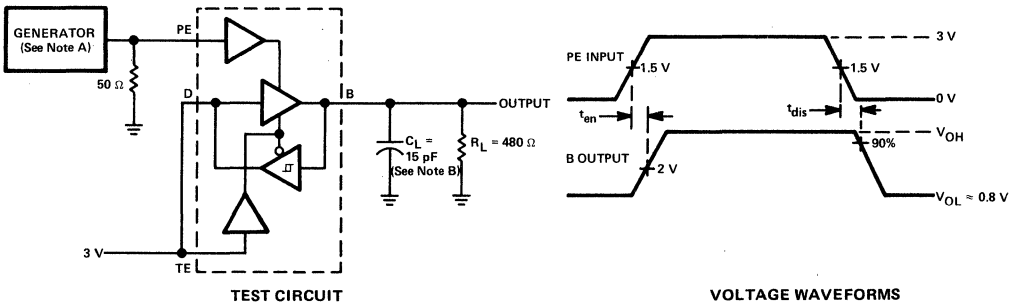


FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

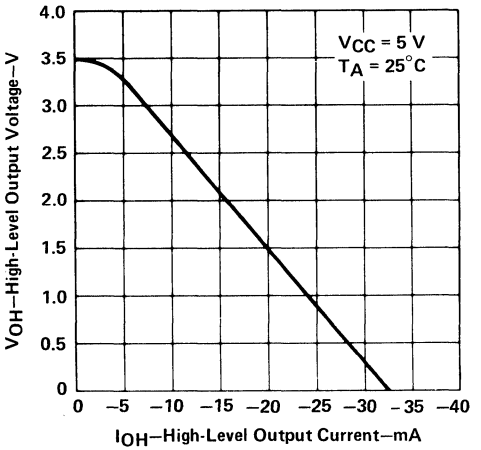


FIGURE 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

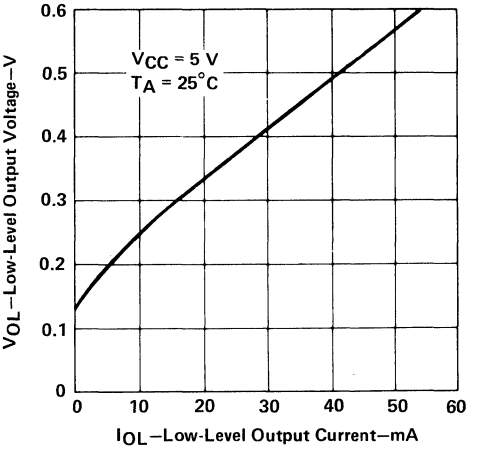


FIGURE 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

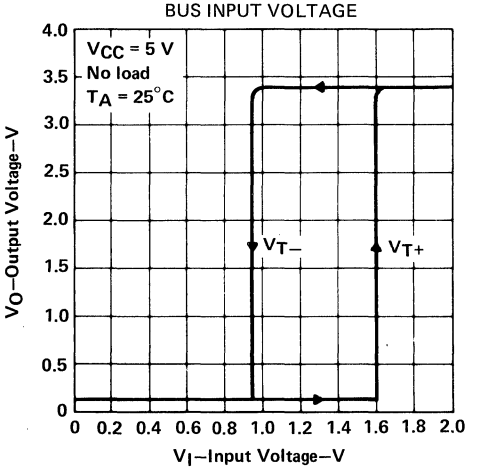


FIGURE 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

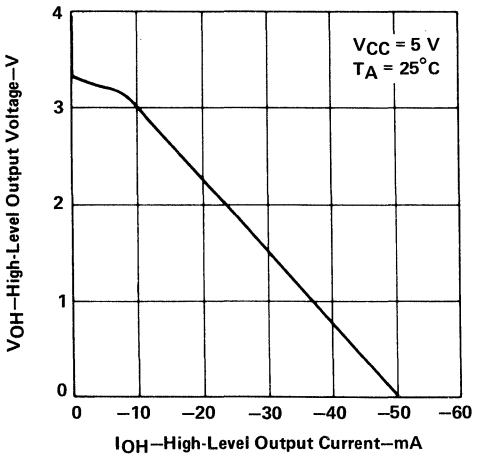


FIGURE 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

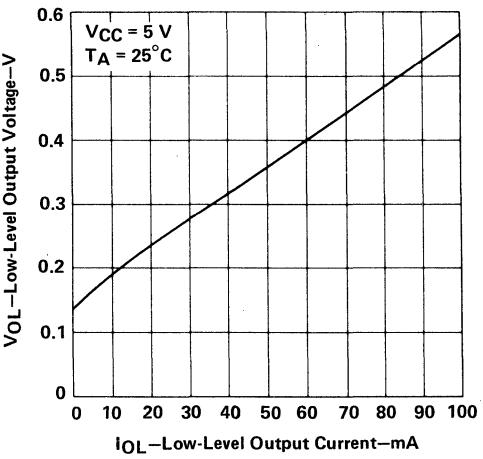


FIGURE 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

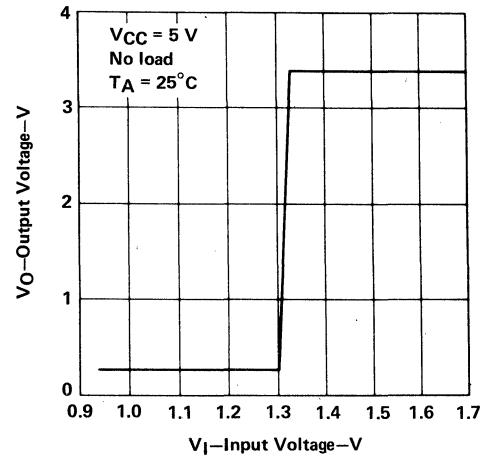


FIGURE 11

BUS CURRENT
vs
BUS VOLTAGE

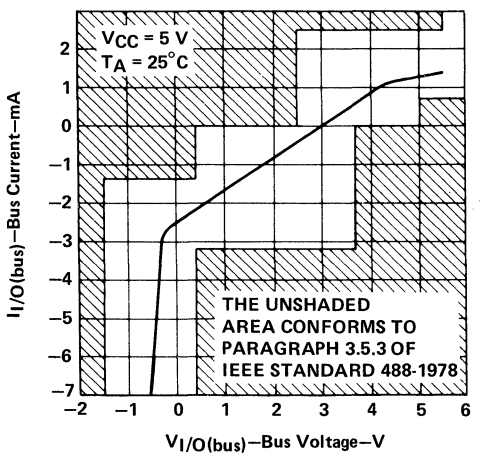


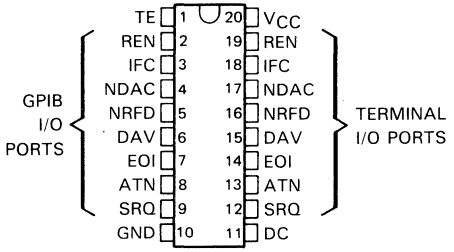
FIGURE 12

D2618, OCTOBER 1980—REVISED OCTOBER 1985

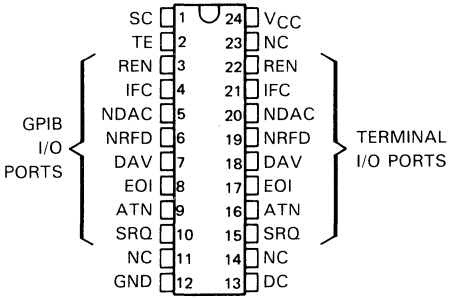
MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- Power-Up/Power-Down Protection (Glitch-Free)
- Designed to Implement Control Bus Interface
- SN75161B Designed for Single Controller
- SN75162B Designed for Multi-Controllers
- High-Speed, Low-Power Schottky Circuitry
- Low-Power Dissipation . . . 72 mW Max Per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)

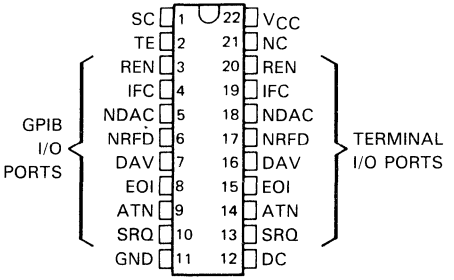
SN75161B . . . DW, J, OR N PACKAGE
(TOP VIEW)



SN75162B . . . DW PACKAGE
(TOP VIEW)



SN75162B . . . N PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN75161B and SN75162B eight-channel general-purpose interface bus transceivers are monolithic, high-speed, low-power Schottky devices designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a single- or multiple-controller instrumentation system. When combined with the SN75160B octal bus transceiver, the SN75161B or SN75162B provides the complete 16-wire interface for the IEEE 488 bus.

The SN75161B and SN75162B each features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. A power up/down disable circuit is included on all bus and receiver outputs. This provides glitch-free operation during V_{CC} power-up and power-down. The direction of data through these driver-receiver pairs is determined by the DC, TE, and SC (on SN75162B) enable signals. The SC input on the SN75162B allows the REN and IFC transceivers to be controlled independently.

description (continued)

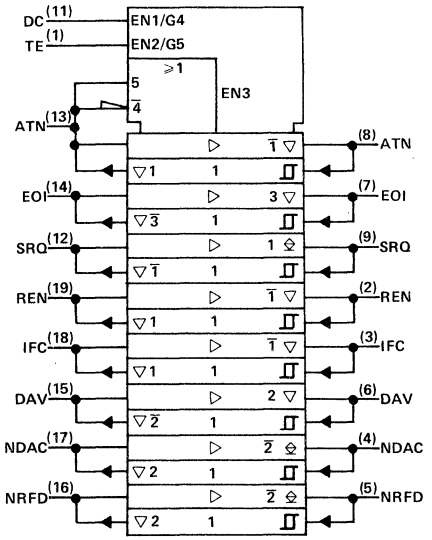
The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when supply voltage V_{CC} is 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features p-n-p transistor inputs for high input impedance and hysteresis of 400 mV for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

The SN75161B and SN75162B are characterized for operation from 0°C to 70°C.

CHANNEL IDENTIFICATION TABLE

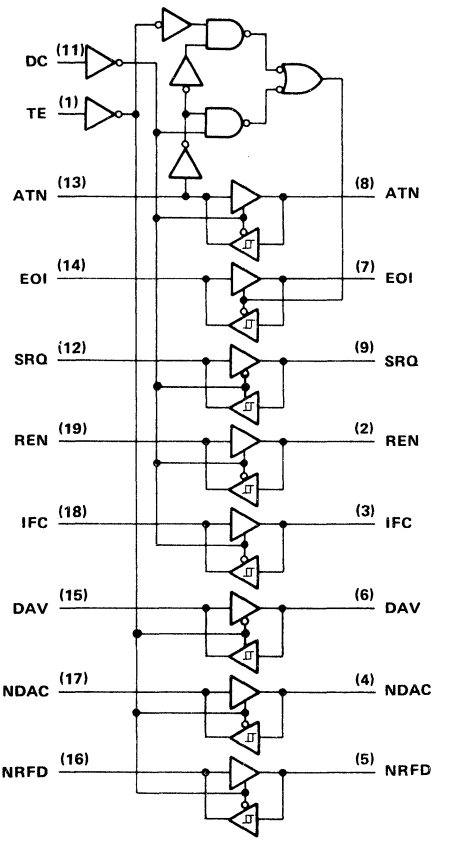
NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
SC	System Control (SN75162B only)	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End or Identify	
DAV	Data Valid	Data Transfer
NDAC	Not Data Accepted	
NRFD	Not Ready for Data	

SN75161B logic symbol†

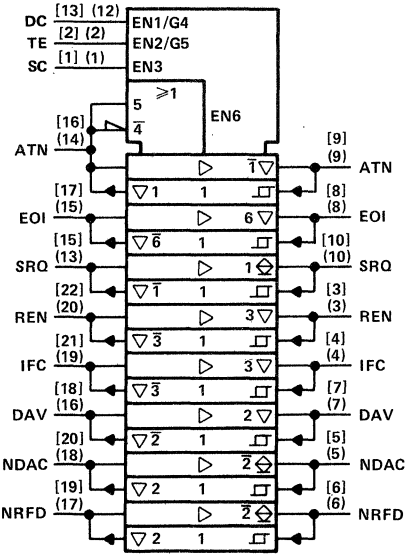


† This symbol is in accordance with IEEE Std 91-1984 and IEC publication 617-12.
▽designates 3-state output, ⏀designates passive-pullup outputs.

SN75161B logic diagram (positive logic)

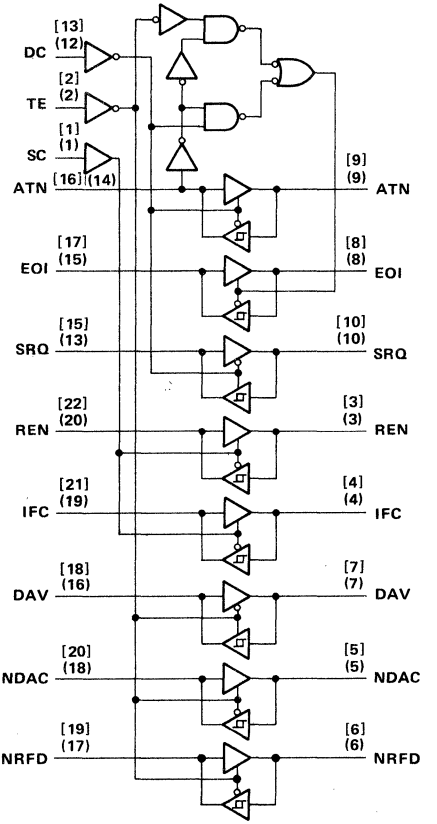


SN75162B logic symbol†



† This symbol is in accordance with IEEE Std 91-1984 and IEC publication 617-12.
▽designates 3-state output, ⏀designates passive-pullup outputs.

SN75162B logic diagram (positive logic)



[ ] Denotes pin numbers for DW package.
( ) Denotes pin numbers for N package.

SN75161B
RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS			BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
			(Controlled by DC)					(Controlled by TE)		
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

SN75162B
RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS				BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
				(Controlled by DC)		(Controlled by SC)			(Controlled by TE)		
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

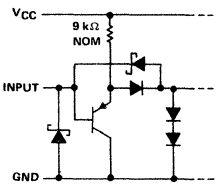
H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

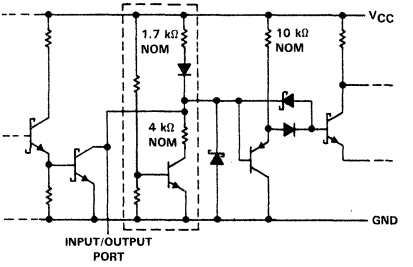
† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

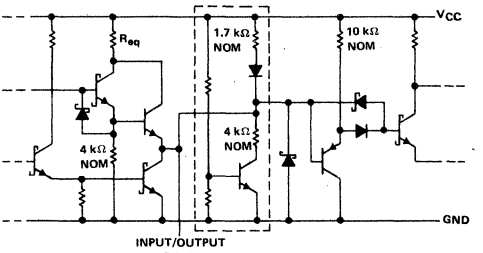


TYPICAL OF SRQ, NDAC, and NRFD GPIB I/O PORT



Circuit inside dashed lines is on the driver outputs only.

TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, and NRFD GPIB I/O PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Low-level driver output current	100 mA
Continuous total power dissipation (see Note 2)	See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: J package	300°C
Lead temperature 1,6 mm (1/16) inch from the case for 10 seconds: DW or N package	260°C

NOTES 1. All voltage values are with respect to network ground terminal.
2. In the J package, SN75161B chips are alloy mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW (20 Pin)	1125 mW	9.0 mW/°C	720 mW
DW (24 Pin)	1350 mW	10.8 mW/°C	864 mW
J	1375 mW	11.0 mW/°C	880 mW
N (20 Pin)	1150 mW	9.2 mW/°C	736 mW
N (22 Pin)	1700 mW	13.6 mW/°C	1088 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with 3-state outputs			−5.2	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = −800 μA		2.7	3.5		V
		Bus	I_{OH} = −5.2 mA		2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA			0.3	0.5	V
		Bus	I_{OL} = 48 mA			0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal and control inputs	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current		V_I = 0.5 V			−10	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 to 2.5 V			−40	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load,	TE, DC, and SC low			110	mA
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{OH} applies for 3-state outputs only.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus (SRQ, NDAC NRFD)	C_L = 30 pF, See Figure 1		29	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					15	22	
t_{PZH}	Output enable time to high level	TE, DC, or SC	BUS (ATTN, EOI, REN, IFC, and DAV)	See Figure 3			60	ns
t_{PHZ}	Output disable time from high level						45	
t_{PZL}	Output enable time to low level						60	
t_{PLZ}	Output disable time from low level						55	
t_{PZH}	Output enable time to high level	TE, DC, or SC	Terminal	See Figure 4			55	ns
t_{PHZ}	Output disable time from high level						50	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						55	

PARAMETER MEASUREMENT INFORMATION

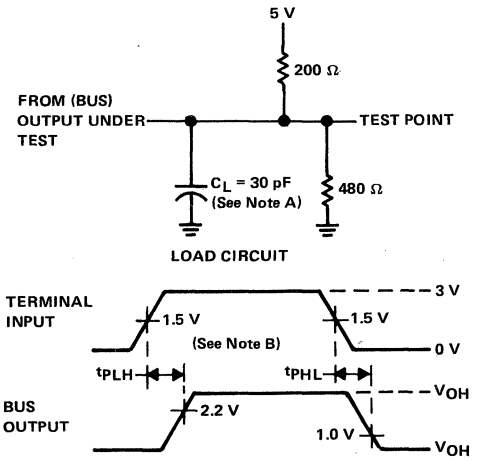


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

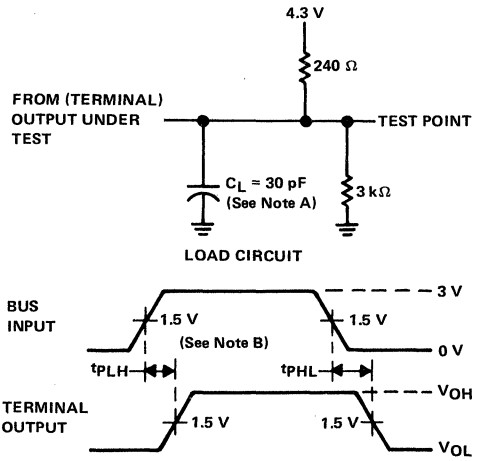
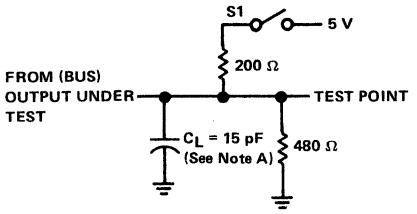


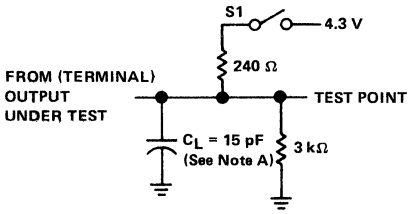
FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_O = 50 Ω.

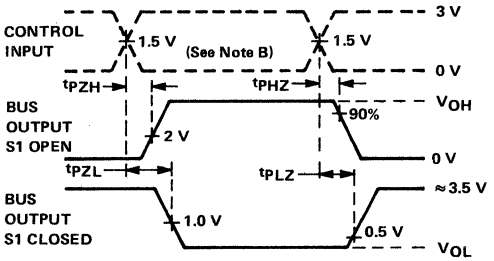
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

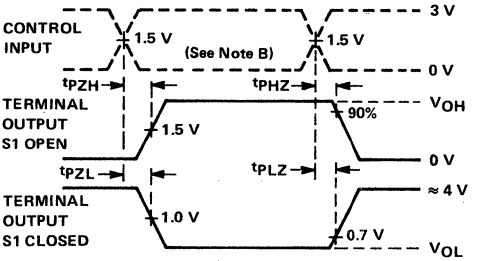


LOAD CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3. BUS ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS

FIGURE 4. TERMINAL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_O = 50 Ω.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

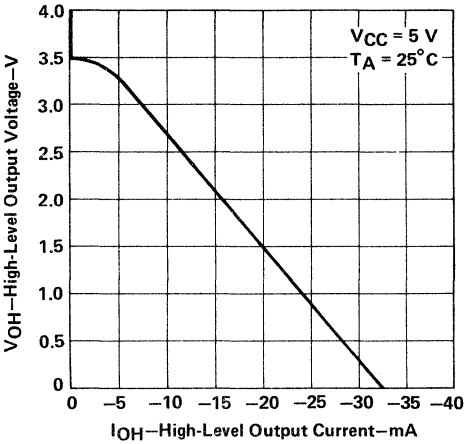


FIGURE 5

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

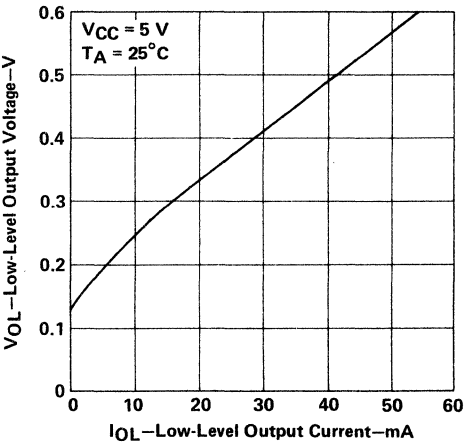


FIGURE 6

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

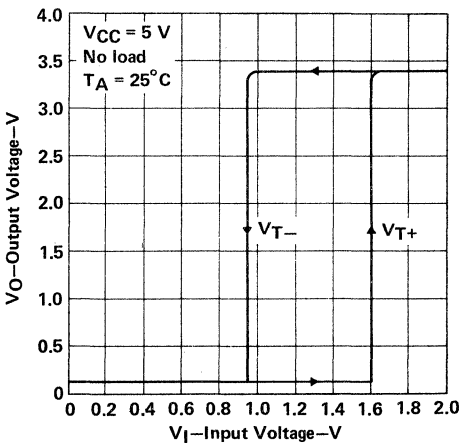


FIGURE 7

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

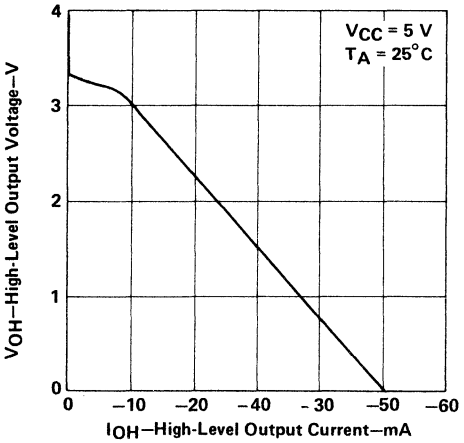


FIGURE 8

BUS-LOW LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

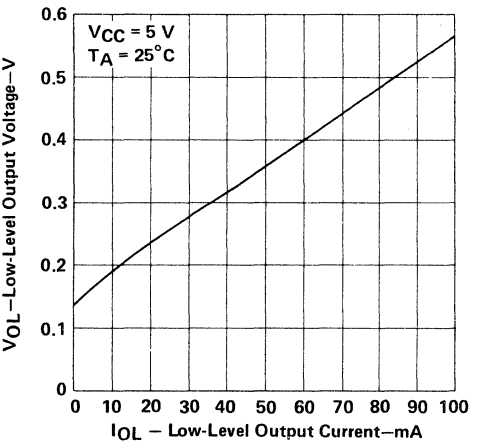


FIGURE 9

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

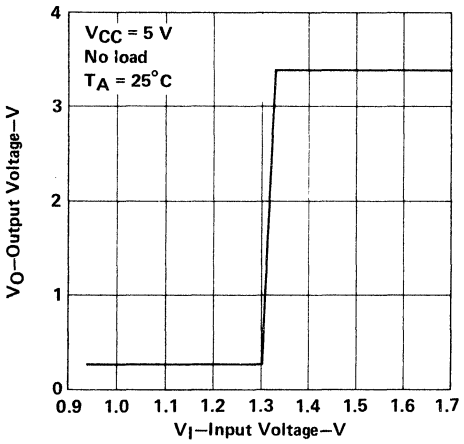


FIGURE 10

BUS CURRENT
vs
BUS VOLTAGE

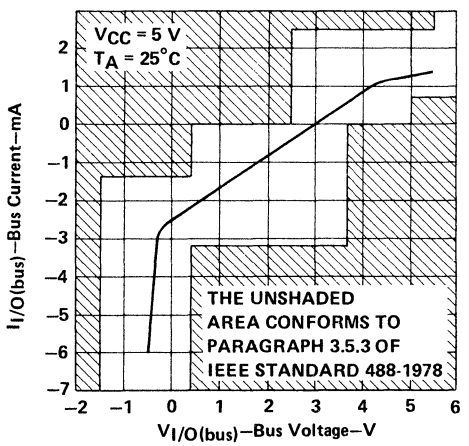
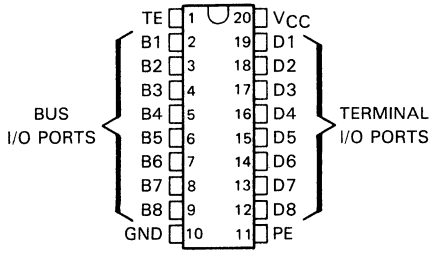


FIGURE 11

D2611, OCTOBER 1985

- **8-Channel Bidirectional Transceivers**
- **Power-Up/Power-Down Protection (Glitch-Free)**
- **High-Speed Low-Power Schottky Circuitry**
- **Low Power Dissipation . . . 66 mW Max Per Channel**
- **High-Impedance P-N-P Inputs**
- **Receiver Hysteresis . . . 650 mV Typ**
- **Open-Collector Driver Output Option**
- **No Loading of Bus When Device Is Powered Down (V_{CC} = 0)**

DW, J, OR N PACKAGE
(TOP VIEW)



description

The SN75163B octal general-purpose interface bus transceiver is a monolithic, high-speed, low-power Schottky device. It is designed for two-way data communications over single-ended transmission lines. The transceiver features driver outputs that can be operated in either the open-collector or 3-state modes. If Talk Enable (TE) is high, these outputs have the characteristics of open-collector outputs when Pullup Enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places the outputs in the high-impedance state. The driver outputs are designed to handle loads of up to 48 mA of sink current. Each receiver features p-n-p transistor inputs for high input impedance and 400 mV of hysteresis for increased noise immunity.

Output glitches during power-up and power-down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when V_{CC} = 0.

The SN75163B is characterized for operation from 0°C to 70°C.

FUNCTION TABLES

EACH DRIVER

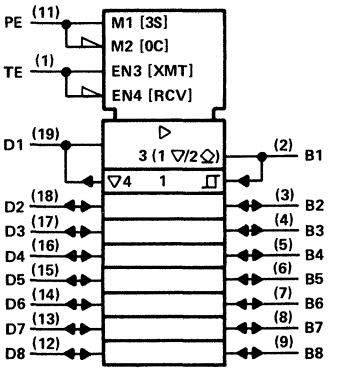
INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	H	L
H	X	L	Z
L	H	L	L
X	L	X	Z

EACH RECEIVER

INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

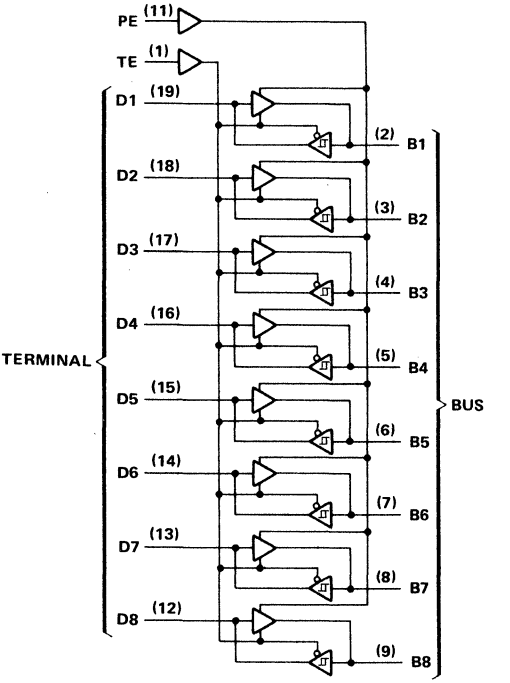
H = high level, L = low level, X = irrelevant, Z = high-impedance state.

logic symbol†



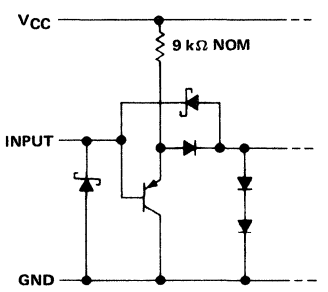
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs.
◇ Designates open-collector outputs.

logic diagram (positive logic)

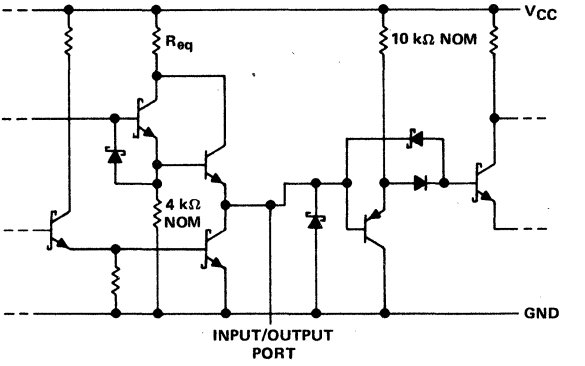


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total power dissipation (see Note 2) . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. In the J package, SN75163B chips are alloy mounted.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
J	1375 mW	11.0 mW/°C	880 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			−10	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature range, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)‡	Bus			0.4	0.65		V
V_{OH}	High level output voltage	Terminal	I_{OH} = −800 μA,	TE at 0.8 V	2.7	3.5		V
		Bus	I_{OH} = −10 mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	PE and TE at 2 V		0.4	0.5	
I_{OH}	High-level output current (open-collector mode)	Bus	V_O = 5.5 V, D and TE at 2 V	PE at 0.8 V,			100	μA
I_{OZ}	Off-state output current (3-state mode)	Bus	PE at 2 V, TE at 0.8 V	V_O = 2.7 V			20	μA
				V_O = 0.4 V			−20	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current	Terminal	V_I = 0.5 V			−10	−100	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load	Receivers low and enabled			80	mA
				Drivers low and enabled			100	
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V or 0, f = 1 MHz	$V_{I/O}$ = 0 to 2 V,		30		pF

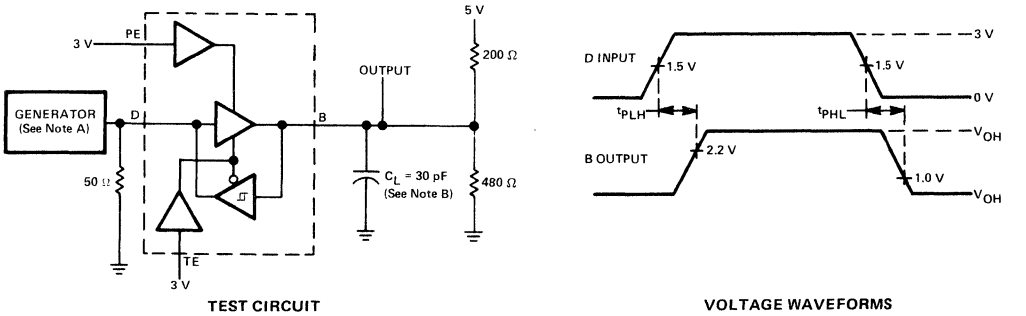
†All typical values are at V_{CC} = 5, T_A = 25°C.

‡Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

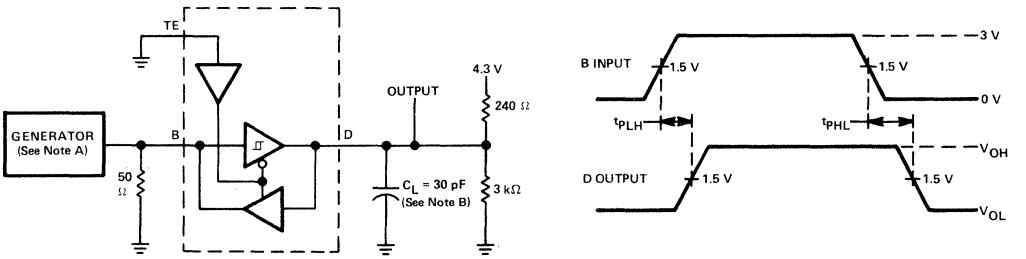
PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					15	22	
t_{PZH}	Output enable time to high level	TE	Bus	See Figure 3		25	35	ns
t_{PHZ}	Output disable time from high level					13	22	
t_{PZL}	Output enable time to low level					22	35	
t_{PLZ}	Output disable time from low level					22	32	
t_{PZH}	Output enable time to high level	TE	Terminal	See Figure 4		20	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level					23	32	
t_{PLZ}	Output disable time from low level					19	30	
t_{en}	Output pull-up enable time	PE	Terminal	See Figure 5		15	22	ns
t_{dis}	Output pull-up disable time					13	20	

PARAMETER MEASUREMENT INFORMATION



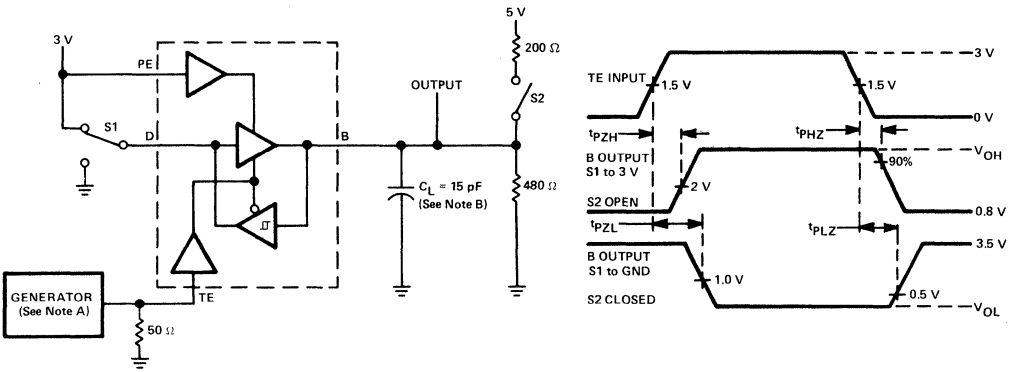
TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

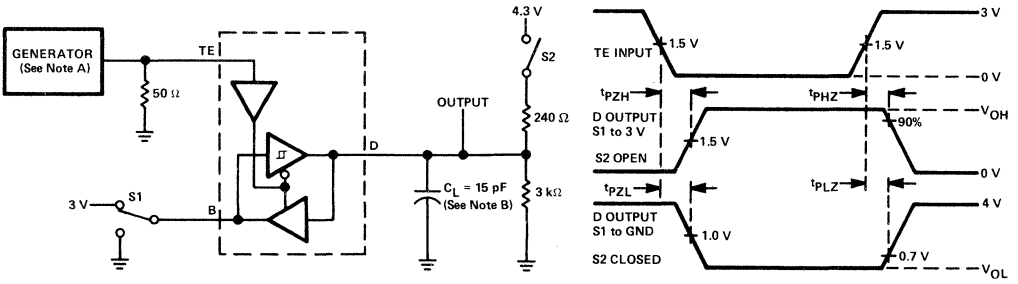


TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

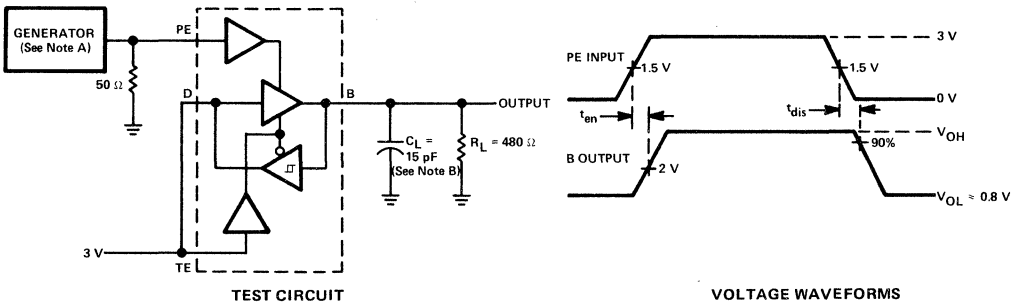
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ ns, Z_o = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

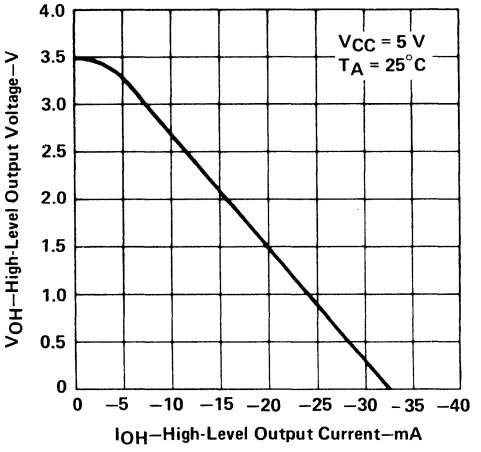


FIGURE 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

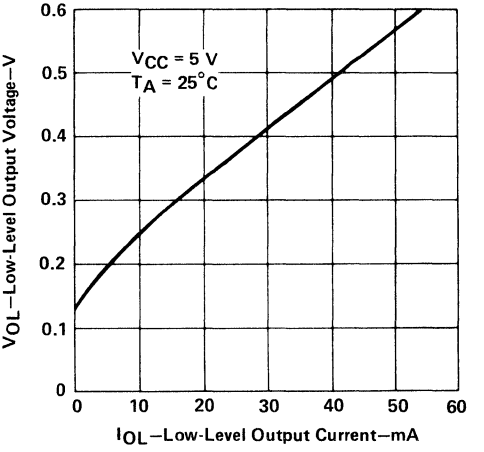


FIGURE 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

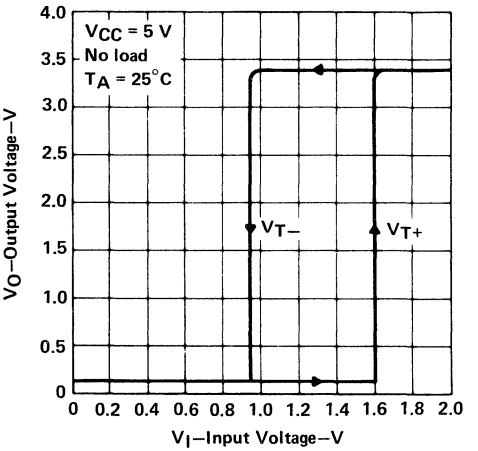


FIGURE 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

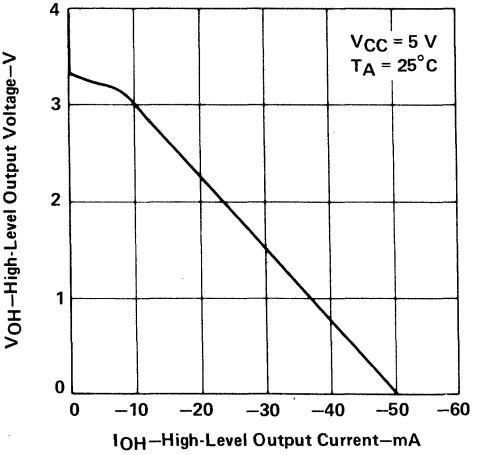


FIGURE 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

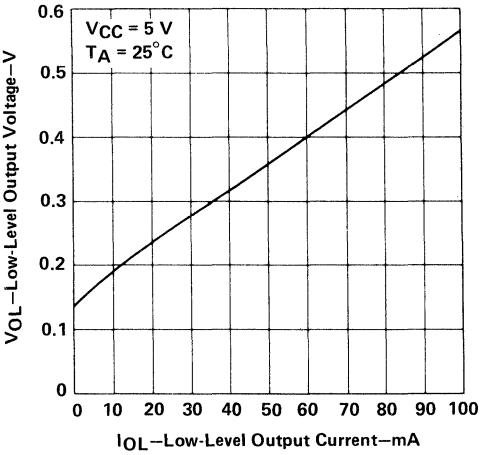


FIGURE 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

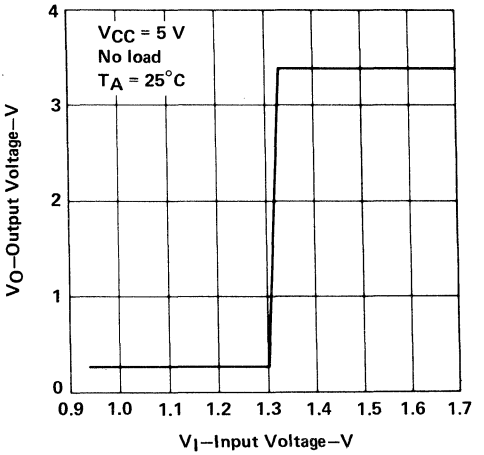
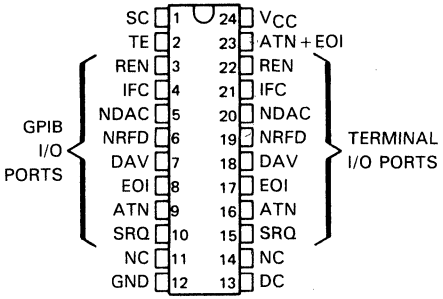


FIGURE 11

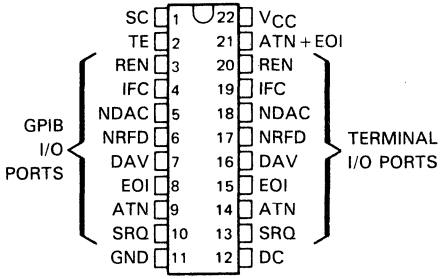
D2908, OCTOBER 1985

- 8-Channel Bidirectional Transceiver
- Power-Up/Power-Down Protection (Glitch-Free)
- ATN + EOI (OR Function) Output to Simplify Board Layout
- Designed to Implement Control Bus Interface for Multi-Controllers
- Low-Power Dissipation . . . 72 mW Max Per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device is Powered Down (V_{CC} = 0)

DW SMALL OUTLINE PACKAGE
(TOP VIEW)



N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection.

description

The SN75164B eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, low-power Schottky device designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a multiple-controller instrumentation system. When combined with the SN75160B octal bus transceiver, the SN75164B provides the complete 16-wire interface for the IEEE 488 bus.

The SN75164B features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. All outputs are disabled (at a high-impedance state) during V_{CC} power-up and power-down transitions for glitch-free operation. The direction of data flow through these driver-receiver pairs is determined by the DC, TE, and SC enable signals. The SN75164B is identical to the SN75162B with the addition of an OR gate to help simplify board layouts in several popular applications. The ATN and EOI signals are ORed to pin 21, which is a standard totem-pole output.

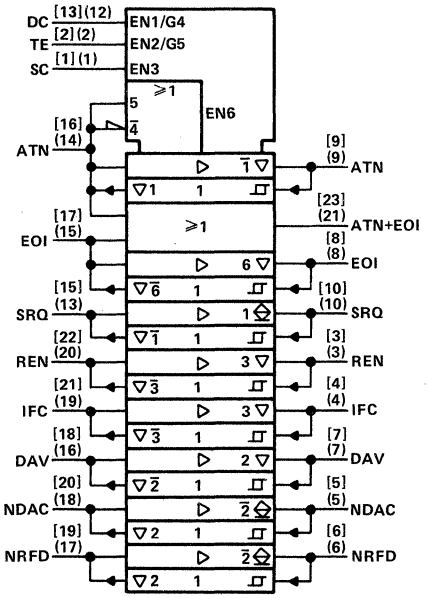
CHANNEL IDENTIFICATION TABLE

NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
SC	System Control	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End or Identify	
ATN + EOI	ATN logical OR EOI	Logic
DAV	Data Valid	Data Transfer
NDAC	Not Data Accepted	
NRFD	Not Ready for Data	

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when supply voltage V_{CC} is 0. The drivers are designed to handle loads up to 48 milliamperes of sink current. Each receiver features p-n-p transistor inputs for high input impedance and a guaranteed hysteresis of 400 millivolts for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

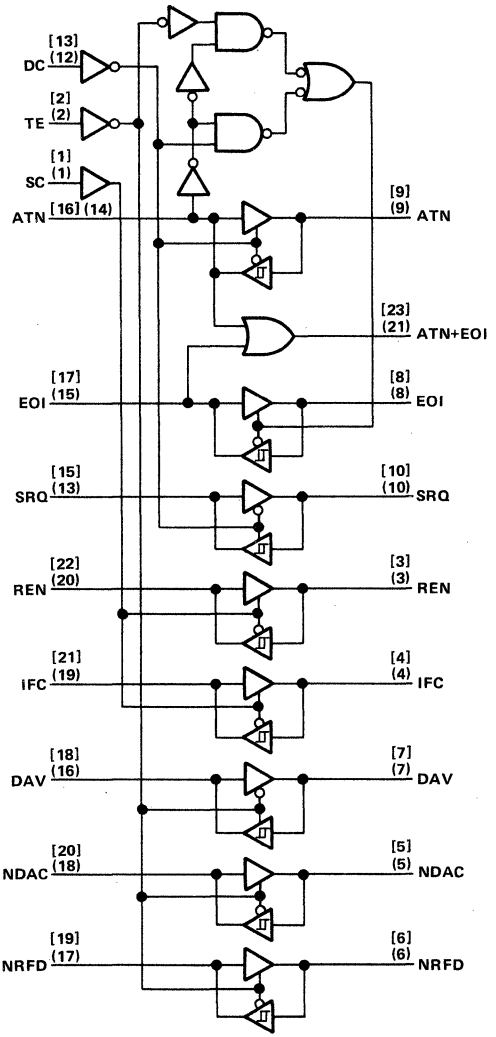
The SN75164B is manufactured in a 22-pin dual-in-line and 24-pin Small Outline package. The SN75164B is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



[ ] Denotes pin numbers for DW package.
( ) Denotes pin numbers for N package.

RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS				BUS-MANAGEMENT CHANNELS				DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN† (Controlled by DC)	SRQ (Controlled by DC)	REN (Controlled by SC)	IFC (Controlled by SC)	EOI	DAV (Controlled by TE)	NDAC (Controlled by TE)	NRFD (Controlled by TE)
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

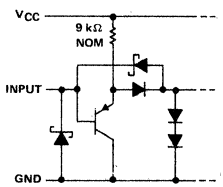
† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

ATN + EOI FUNCTION TABLE

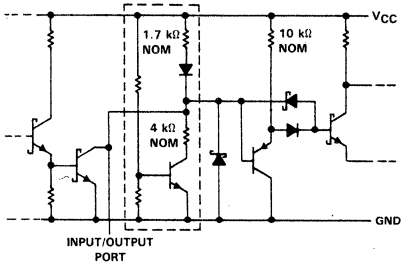
INPUTS		OUTPUT
ATN	EOI	ATN + EOI
H	X	H
X	H	H
L	L	L

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

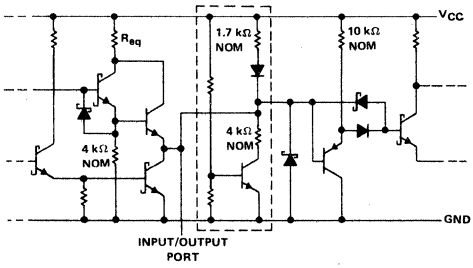


TYPICAL OF SRQ, NDAC, and NRFD GPIB I/O PORT



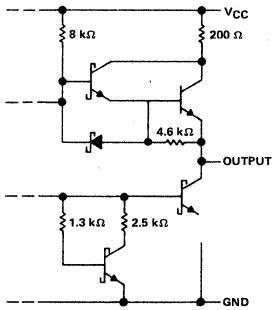
Circuit inside dashed lines is on GPIB I/O ports only.

TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, and NRFD GPIB I/O PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on GPIB I/O ports only.

ATN+EOI OUTPUT



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
DW package . . . . . 1350 mW
N package . . . . . 1700 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 10 seconds: DW or N package . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the DW package at the rate of 10.8 mW/°C, the N package at the rate of 13.6 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with 3-state outputs			−5.2	mA
	Terminal ports			−800	μA
	ATN + EOI			−400	
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
	ATN + EOI			4	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA				−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4			V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = −800 μA		2.7			V
		Bus	I_{OH} = −5.2 mA		2.5			
		ATN + EOI	I_{OH} = −400 μA		2.7			
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA				0.5	V
		Bus	I_{OL} = 48 mA				0.5	
		ATN + EOI	I_{OL} = 4 mA				0.4	
I_I	Input current at maximum input voltage	Terminal§	V_I = 5.5 V				100	μA
		ATN, EOI	V_I = 5.5 V				200	
I_{IH}	High-level input current	Terminal, control	V_I = 2.7 V				20	μA
		ATN, EOI	V_I = 2.7 V				40	
I_{IL}	Low-level input current	Terminal, control	V_I = 0.5 V				−100	μA
		ATN, EOI	V_I = 0.5 V				−500	
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5		3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 V to 2.5 V			−40	μA
I_{OS}	Short-circuit output current	Terminal			−15		−75	mA
		Bus			−25		−125	
		ATN + EOI			−10		−100	
I_{CC}	Supply current		No load, TE, DC, and SC low				120	mA
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0 V, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{OH} applies for three-state outputs only.
§ Except ATN and EOI terminal pins.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus (SRQ, NDAC NRFD)	C_L = 30 pF, See Figure 1		29	35	ns
t_{PLH}	Propagation delay time low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					15	22	
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal ATN or Terminal EOI	ATN+EOI	See Figure 3		14		ns
t_{PHL}	Propagation delay time, high-to-low-level output	Terminal ATN or Terminal EOI	ATN+EOI	See Figure 3		14		ns
t_{PZH}	Output enable time to high level	TE, DC, or SC	BUS (ATTN, EOI, REN, IFC, and DAV)	See Figure 4			60	ns
t_{PHZ}	Output disable time from high level						45	
t_{PZL}	Output enable time to low level						60	
t_{PLZ}	Output disable time from low level						55	
t_{PZH}	Output enable time to high level	TE, DC, or SC	Terminal	See Figure 5			55	ns
t_{PHZ}	Output disable time from high level						50	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						55	

PARAMETER MEASUREMENT INFORMATION

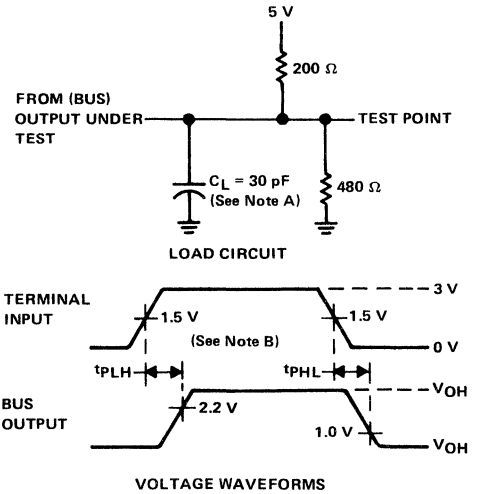


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

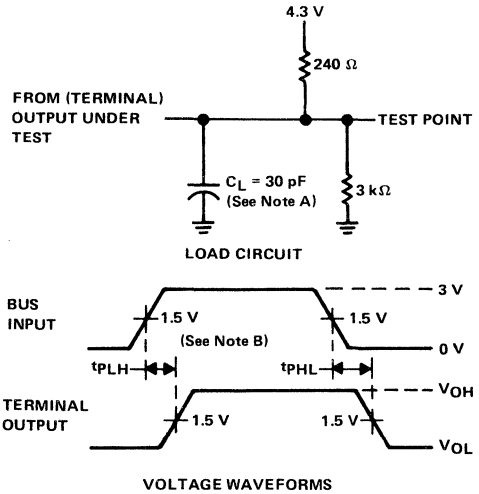
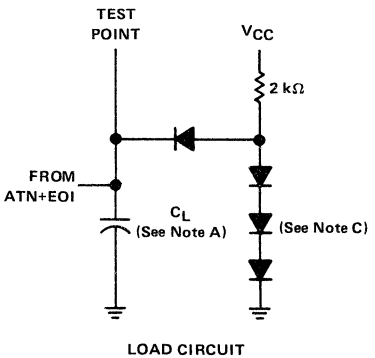


FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES



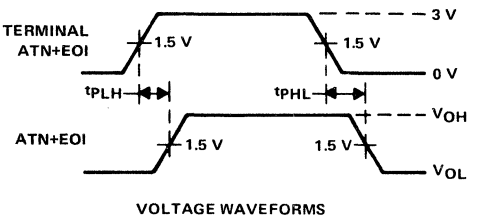
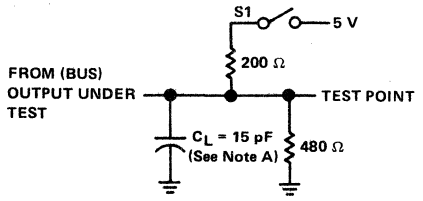


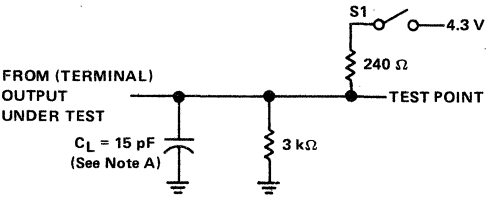
FIGURE 3. ATN + EOI PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.
C. All diodes are 1N916 or 1N3064.

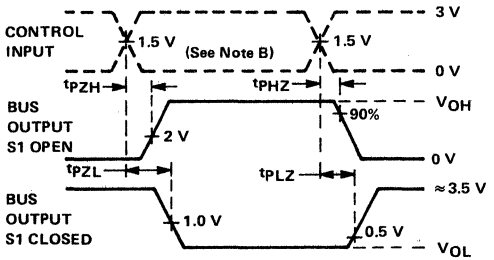
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

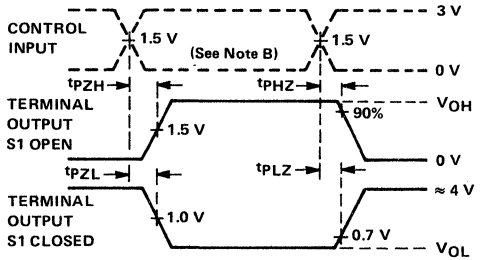


LOAD CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4. BUS ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS

FIGURE 5. TERMINAL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

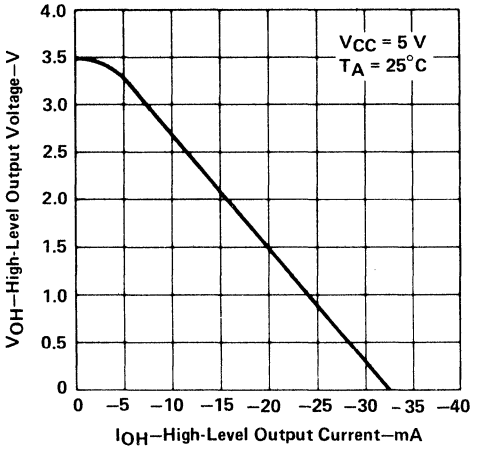


FIGURE 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

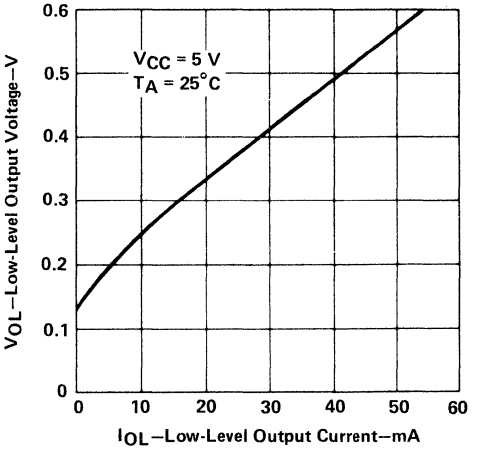


FIGURE 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

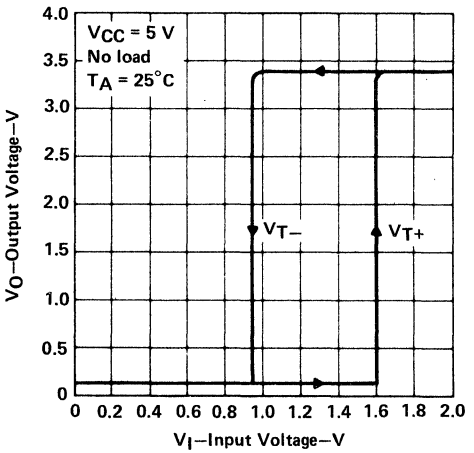


FIGURE 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

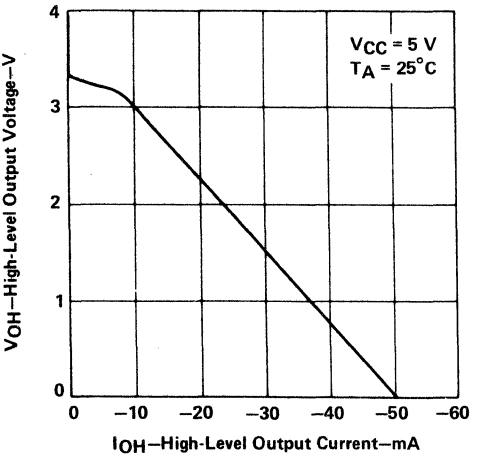


FIGURE 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

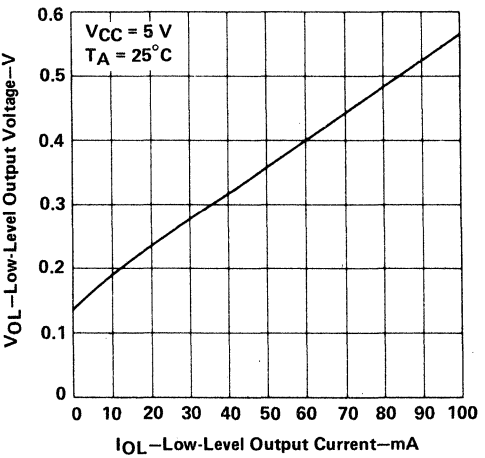


FIGURE 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

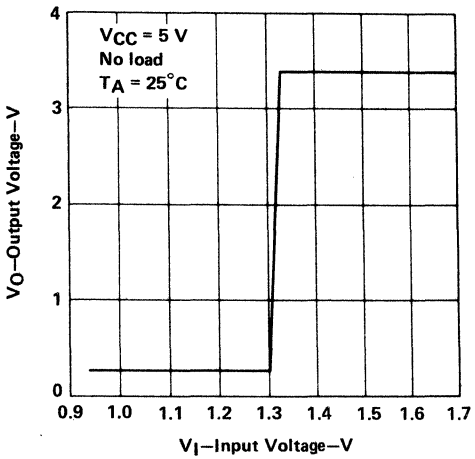


FIGURE 11

BUS CURRENT
vs
BUS VOLTAGE

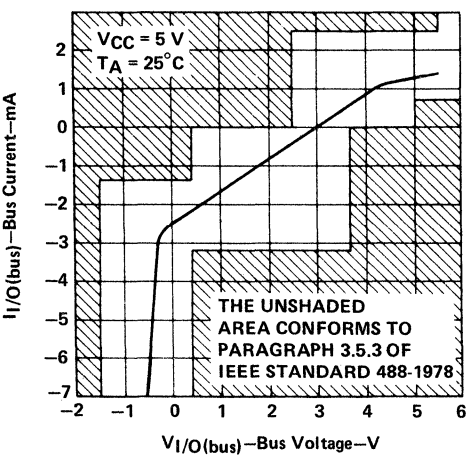
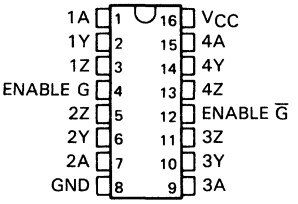


FIGURE 12

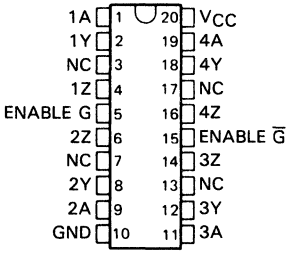
D2596, OCTOBER 1980—REVISED APRIL 1988

- **Meets EIA Standards RS-422-A and RS-485**
- **Meets CCITT Recommendations V.11 and X.27**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Output Voltage Range of −7 V to 12 V**
- **Active-High and Active-Low Enables**
- **Thermal Shutdown Protection**
- **Positive- and Negative-Current Limiting**
- **Operates from Single 5-V Supply**
- **Low Power Requirements**
- **Functionally Interchangeable with AM26LS31**

J OR N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC—No internal connection

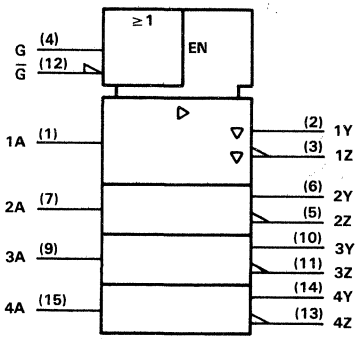
description

The SN75172 is a monolithic quadruple differential line driver with three-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. The device is optimized for balanced multipoint bus transmission at rates of up to 4 megabaud. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

The SN75172 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

The SN75172 is characterized for operation from 0°C to 70°C.

logic symbol†



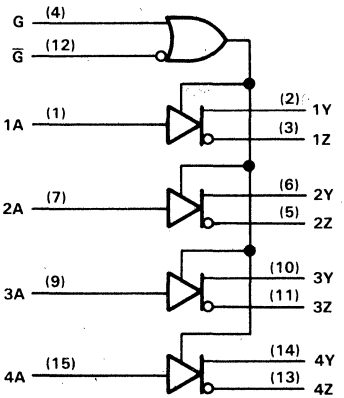
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages.

FUNCTION TABLE
(EACH DRIVER)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level
L = low level
X = irrelevant
Z = high impedance (off)

logic diagram (positive logic)



TEXAS INSTRUMENTS
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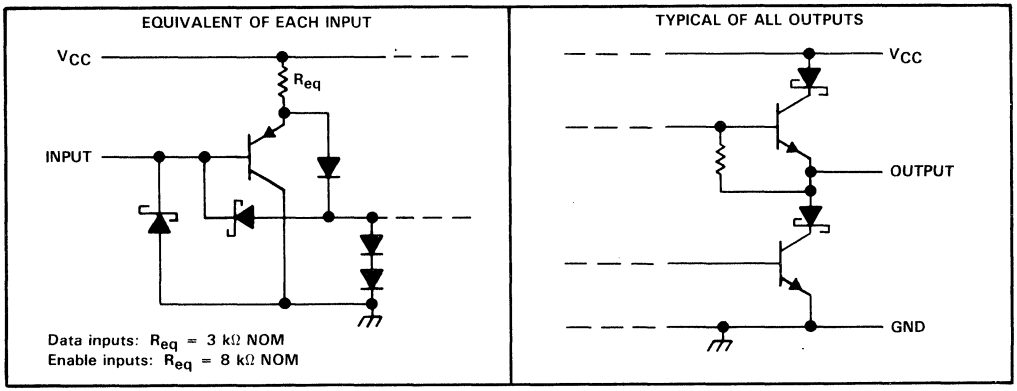
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}			−7 to 12	V
High-level output current, I_{OH}			−60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1		½ V_{OD1}			
				2			V
		R_L = 54 Ω, See Figure 1		1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 2		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡	R_L = 54 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage§					+3 −1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡					±0.2	V
I_O	Output current with power off	V_{CC} = 0, V_O = −7 V to 12 V				±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_I = 0.5 V				−360	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−180	mA
		V_O = V_{CC}				180	
		V_O = 12 V				500	
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		38	60	mA
			Outputs disabled		18	40	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§ In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
NOTE 2: See EIA Standard RS-485 Figure 3-5, Test Termination Measurement 2.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - V_{os}\|$	$\|V_{os} - V_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

switching characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω, See Figure 2		45	65	ns
t_{TD}	Differential-output transition time			80	120	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See Figure 3		80	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See Figure 4		45	80	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, See Figure 3		78	115	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See Figure 4		18	30	ns

PARAMETER MEASUREMENT INFORMATION

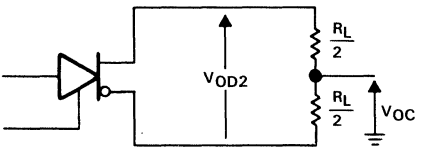


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES

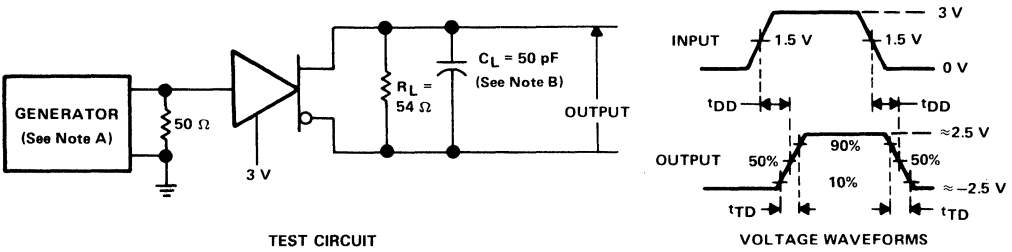


FIGURE 2. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

PARAMETER MEASUREMENT INFORMATION

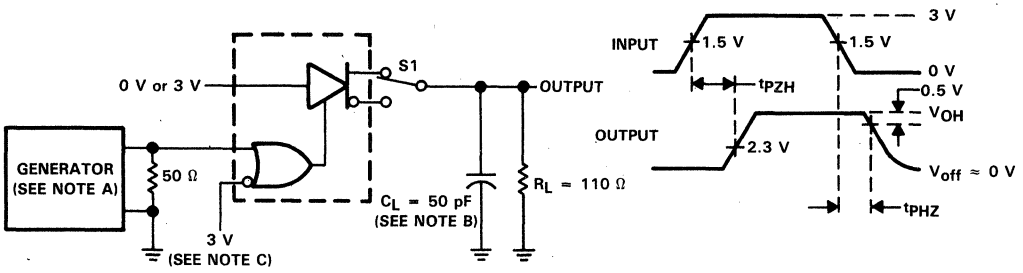


FIGURE 3. t_{PZH} AND t_{PHZ}

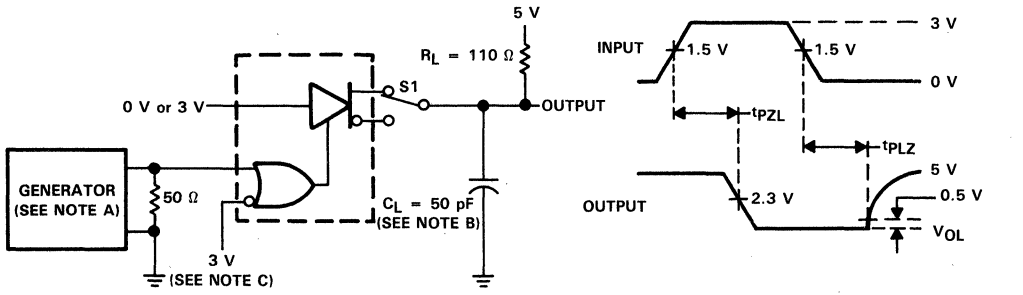


FIGURE 4. t_{PZL} AND t_{PLZ}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_f \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_{out} = 50\ \Omega$.
B. C_L include probe and jig capacitance.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

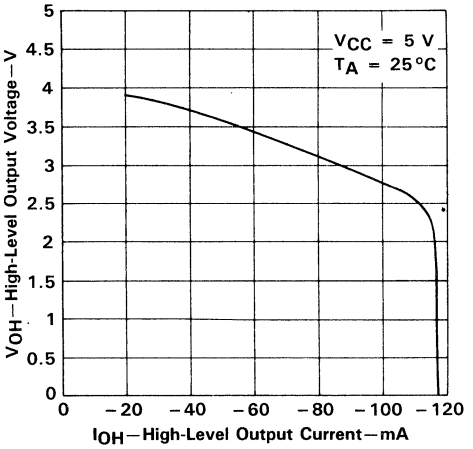


FIGURE 5

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

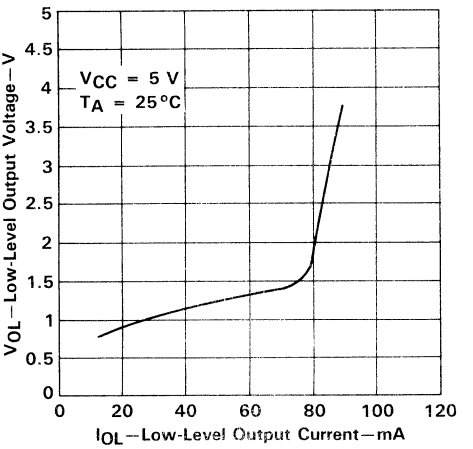


FIGURE 6

DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

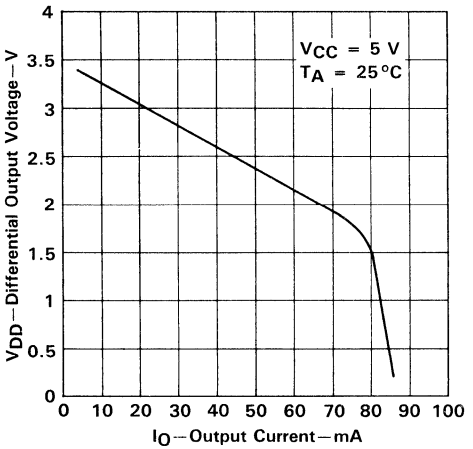


FIGURE 7

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

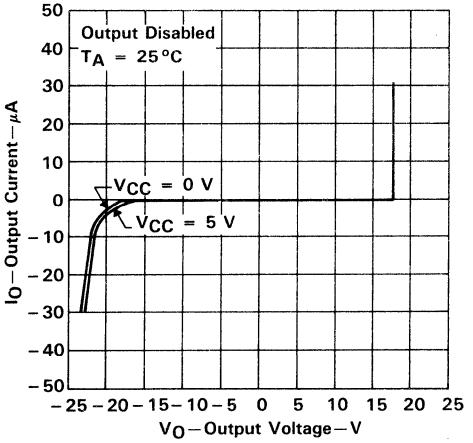


FIGURE 8

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

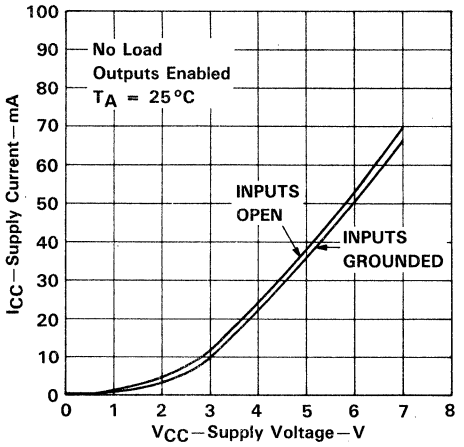


FIGURE 9

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

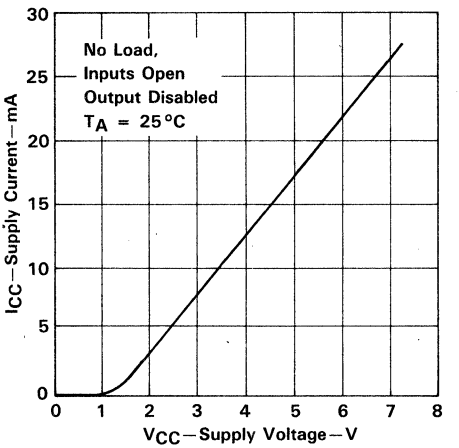
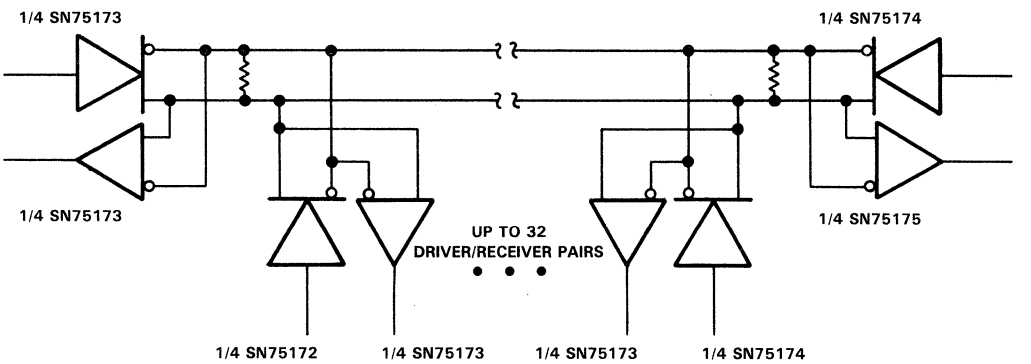


FIGURE 10

TYPICAL APPLICATION



NOTE A: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 11

D2600, OCTOBER 1980—REVISED JULY 1990

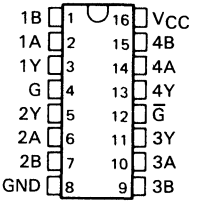
- **Meets EIA Standards RS-422-A, RS-423-A, and RS-485**
- **Meets CCITT Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Input Voltage Range . . . −12 to 12 V**
- **Input Sensitivity . . . ±200 mV**
- **Input Hysteresis . . . 50 mV Typ**
- **High Input Impedance . . . 12 kΩ Min**
- **Operates from Single 5-V Supply**
- **Low Power Requirements**
- **Plug-In Replacement for AM26LS32**

description

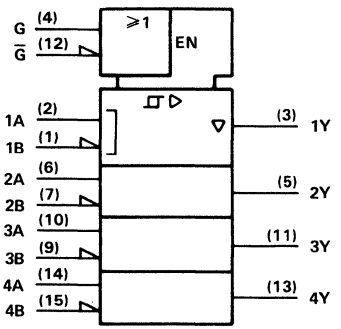
The SN75173 is a monolithic quadruple differential line receiver with 3-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A, RS-423-A, and RS-485 and several CCITT recommendations. The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. The four receivers share two ORed enable inputs, one active when high, the other active when low. The device features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of −12 to 12 V. Fail safe design ensures that if the inputs are open circuited, the outputs will always be high. The SN75173 is designed for optimum performance when used with the SN75172 or SN75174 quadruple differential line drivers.

The SN75173 is characterized for operation from 0°C to 70°C.

D, J, OR N PACKAGE
(TOP VIEW)

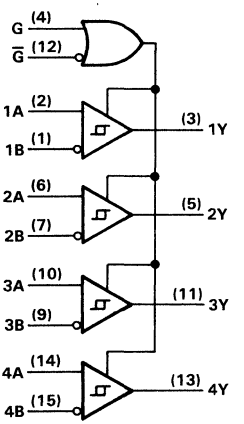


logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

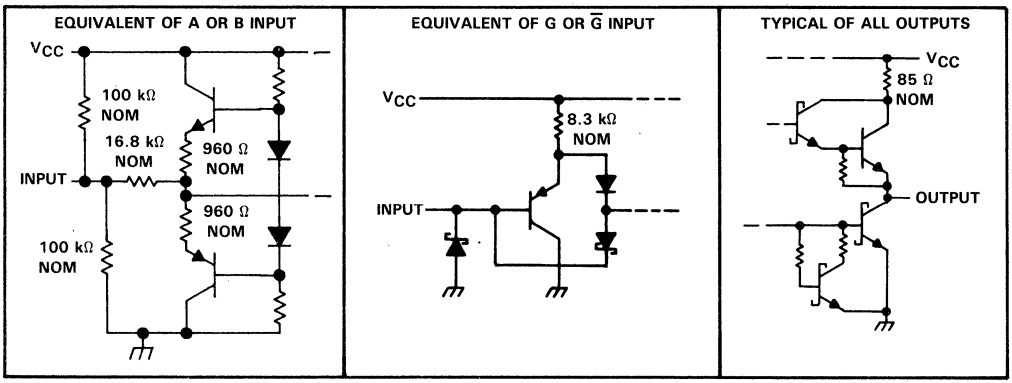


FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL A–B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V $< V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z

H = high level
L = low level
X = irrelevant
? = indeterminate
Z = high impedance (off)

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, A or B inputs . . . . . ±25 V
Differential input voltage (see Note 2) . . . . . ±25 V
Enable input voltage . . . . . 7 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
D package . . . . . 950 mW
J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the D package to 608 mW at 70°C at the rate of 7.6 mW/°C, the J package to 656 mW at 70°C at the rate of 8.2 mW/°C, and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75173 chips are glass mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±12	V
Differential input voltage, V_{ID}			±12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

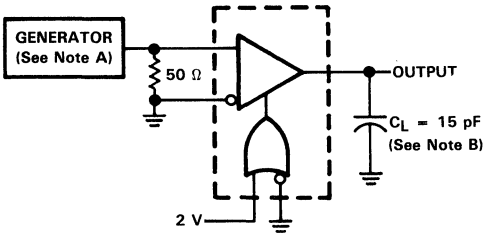
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 16 mA	−0.2‡			V
V_{hys}	Hysteresis§				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −400 μA	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input at 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current¶			−15		−85	mA
I_{CC}	Supply current	Outputs disabled				70	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for threshold voltage levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
¶Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
NOTE 4: Refer to EIA Standard RS-422-A and RS-423-A for exact conditions.

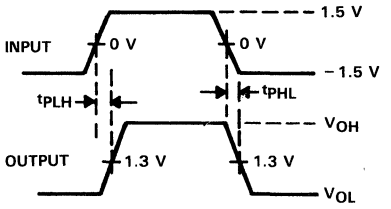
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF,			20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	See Figure 1			22	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 2		17	22	ns
t_{PZL}	Output enable time to low level	C_L = 15 pF,	See Figure 3		20	25	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF,	See Figure 2		21	30	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF,	See Figure 3		30	40	ns

PARAMETER MEASUREMENT INFORMATION

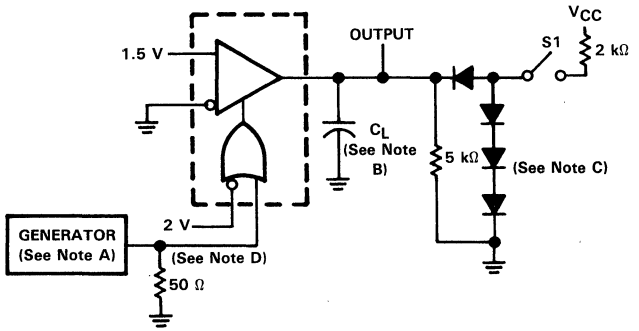


TEST CIRCUIT

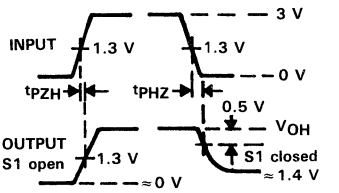


VOLTAGE WAVEFORMS

FIGURE 1. t_{PLH}, t_{PHL}



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2. t_{PHZ}, t_{PZH}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

PARAMETER MEASUREMENT INFORMATION

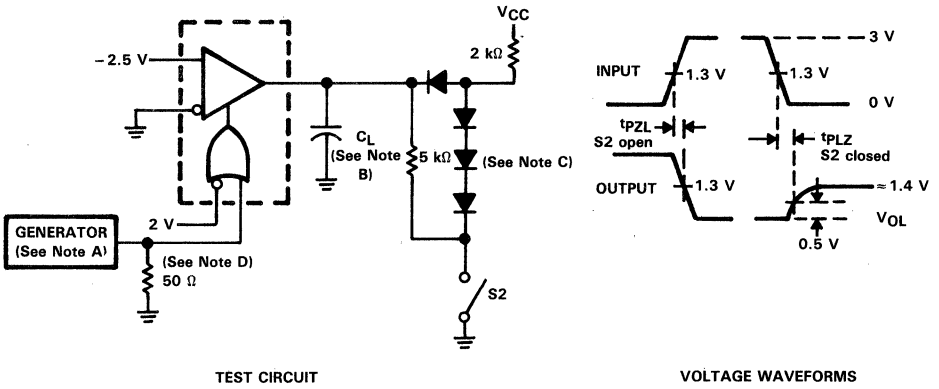


FIGURE 3. t_{PZL}, t_{PLZ}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

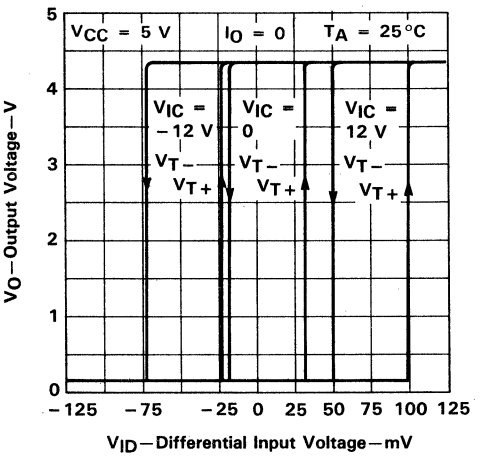


FIGURE 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

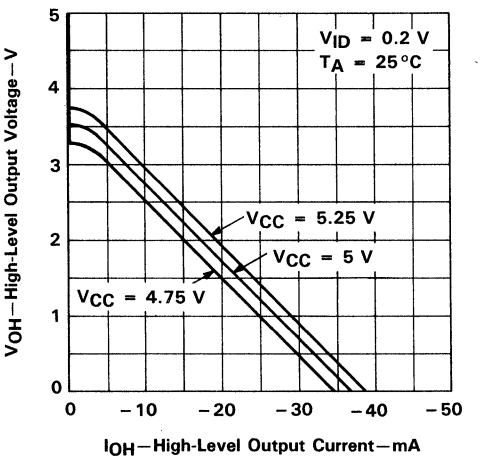


FIGURE 5

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

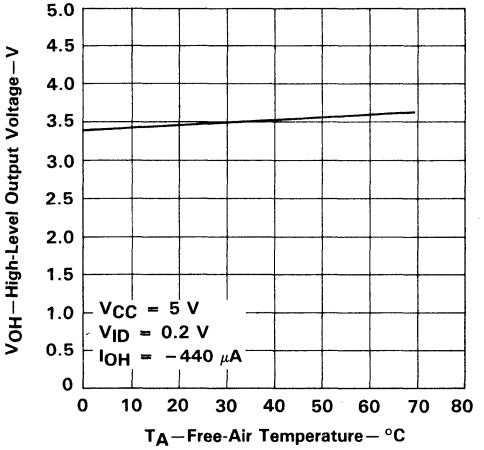


FIGURE 6

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

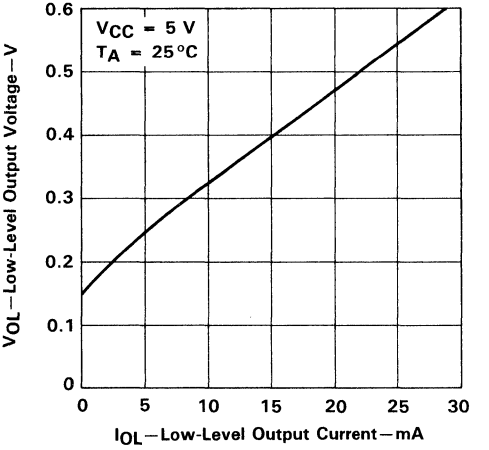


FIGURE 7

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

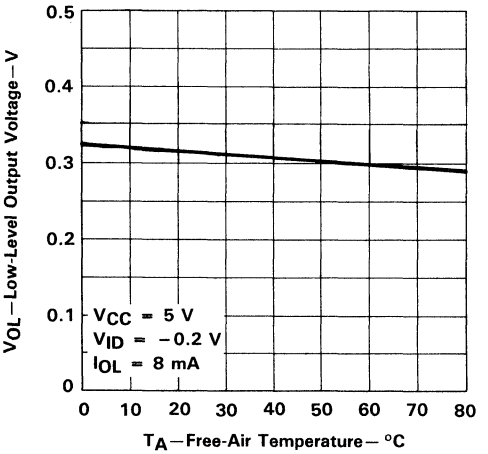


FIGURE 8

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

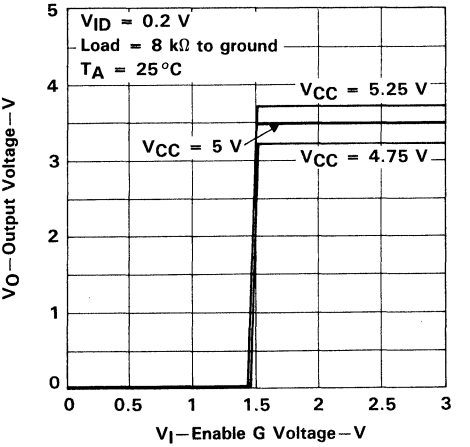


FIGURE 9

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

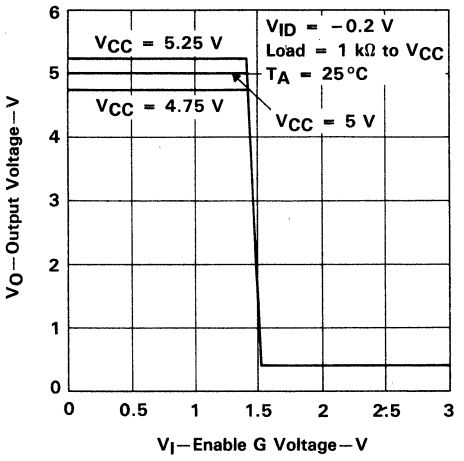


FIGURE 10

INPUT CURRENT
vs
INPUT VOLTAGE

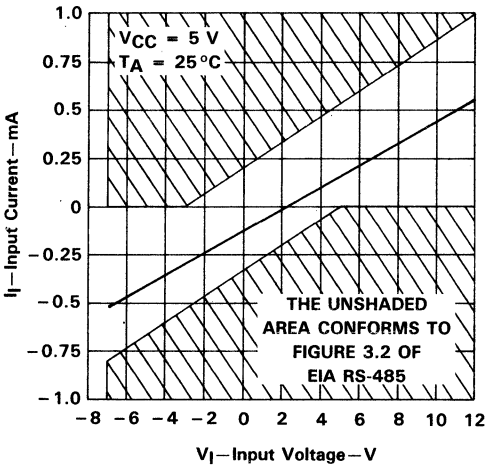
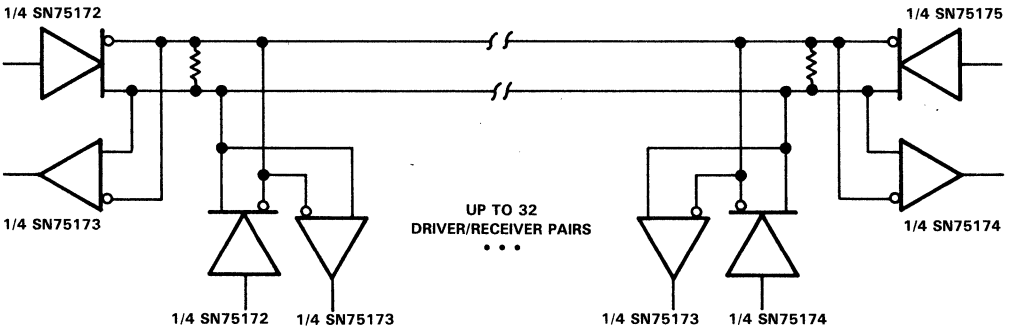


FIGURE 11

TYPICAL APPLICATION



NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

D2601, OCTOBER 1980—REVISED MAY 1988

- **Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Output Voltage Range of −7 V to 12 V**
- **Active-High Enable**
- **Thermal Shutdown Protection**
- **Positive- and Negative-Current Limiting**
- **Operates from Single 5-V Supply**
- **Low Power Requirements**
- **Functionally Interchangeable with MC3487**

description

The SN75174 is a monolithic quadruple differential line driver with three-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. The device is optimized for balanced multipoint bus transmission at rates up to 4 megabaud. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

The SN75174 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

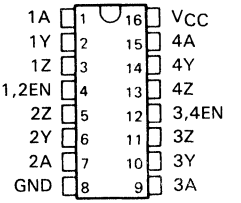
The SN75174 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH DRIVER)

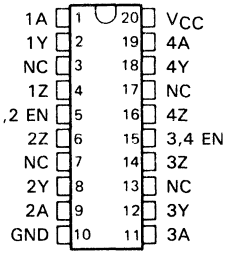
INPUT	ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = TTL high level, X = irrelevant,
L = TTL low level, Z = High impedance (off)

J OR N PACKAGE
(TOP VIEW)

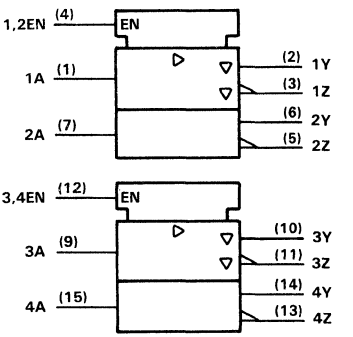


DW PACKAGE
(TOP VIEW)



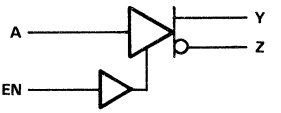
NC—No internal connection

logic symbol†

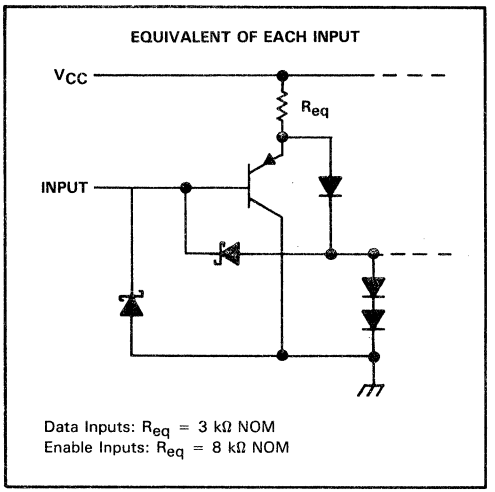


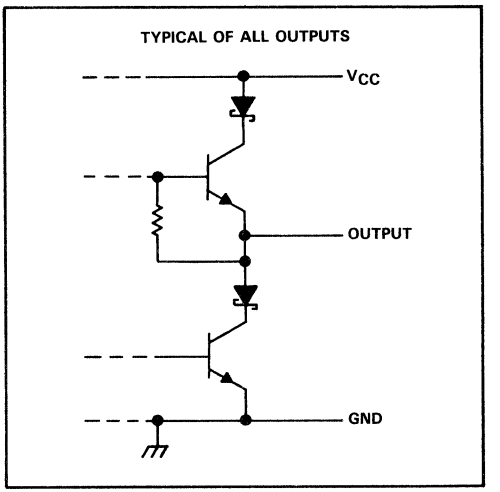
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each driver (positive logic)



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-Level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}			−7 to 12	V
High-level output curent, I_{OH}			−60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, I_{OH} = −33 mA	V_{IL} = 0.8 V,		3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, I_{OL} = 33 mA	V_{IL} = 0.8 V,		1.1		V
V_O	Output voltage	I_O = 0		0		6	V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0		1.5		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	½ V_{OD1}			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 2		1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage‡	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common mode output voltage					+3 −1	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common mode output voltage‡					±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = −7 V to 12 V			±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_I = 0.5 V				−360	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = V_{CC}				180	
		V_O = 12 V				500	
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		38	60	mA
			Oututs disabled		18	40	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
NOTE 2: See EIA Standard RS-485 Figure 3.5, Test Termination Measurement 2.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω, See Figure 2		45	65	ns
t_{TD}	Differential-output transition time			80	120	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See Figure 3		80	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See Figure 4		55	80	ns
t_{PHZ}	Outut disable time from high level	R_L = 110 Ω, See Figure 3		75	115	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See Figure 4		18	30	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

PARAMETER MEASUREMENT INFORMATION

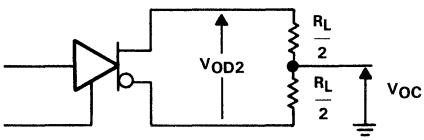
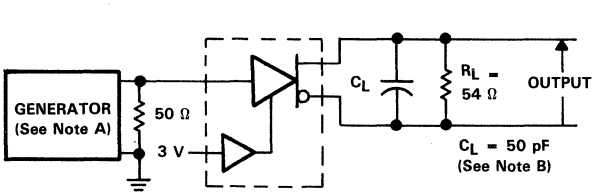
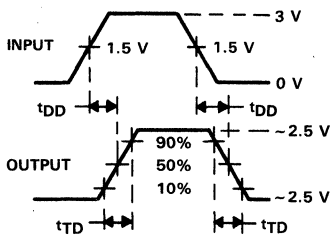


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



TEST CIRCUIT

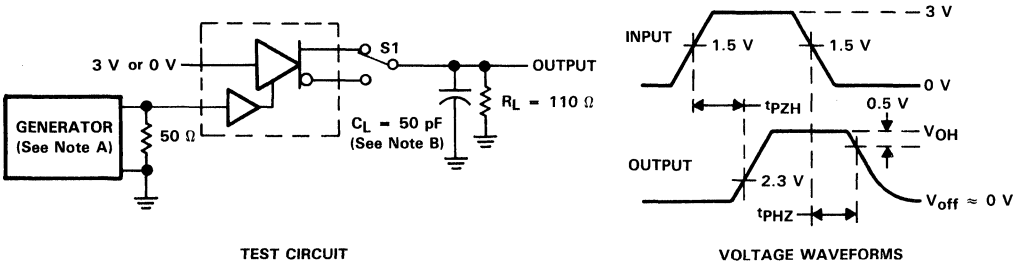


VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

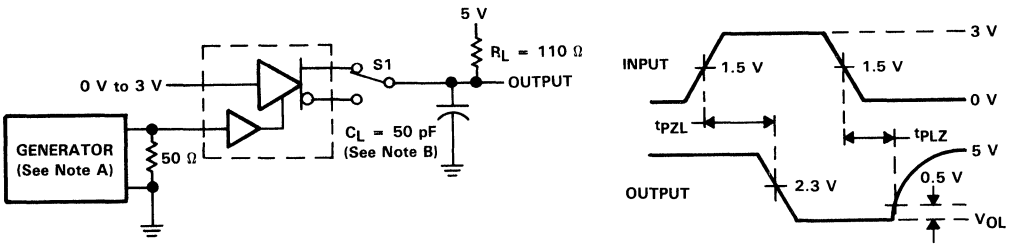
FIGURE 2. DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 3. t_{PZH} AND t_{PHZ}



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 4. t_{PZL} AND t_{PLZ}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

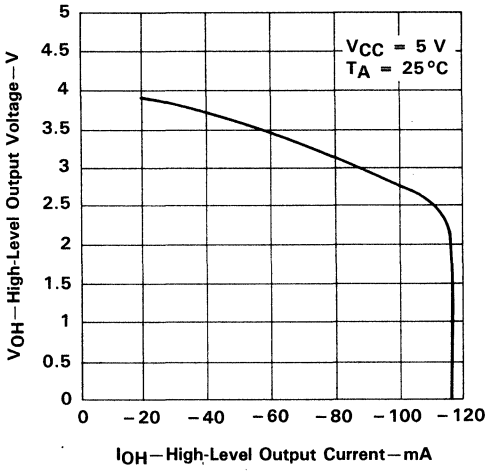


FIGURE 5

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

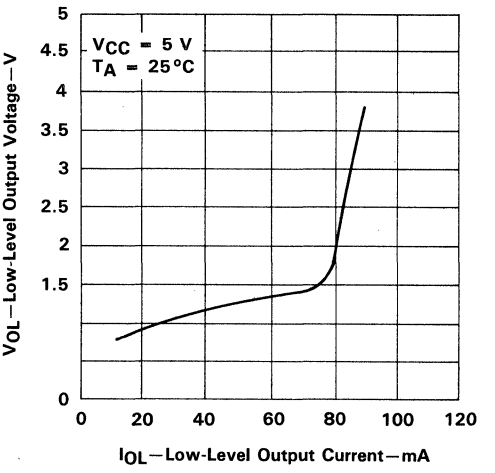


FIGURE 6

DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

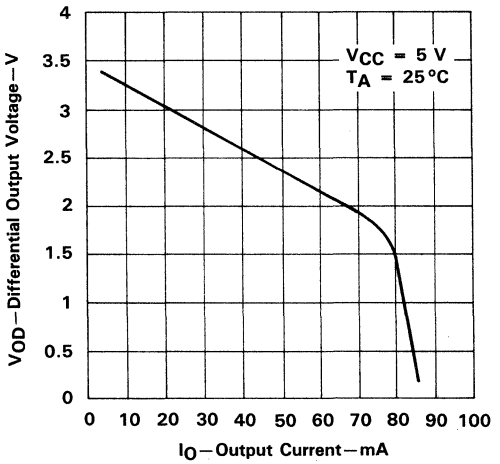


FIGURE 7

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

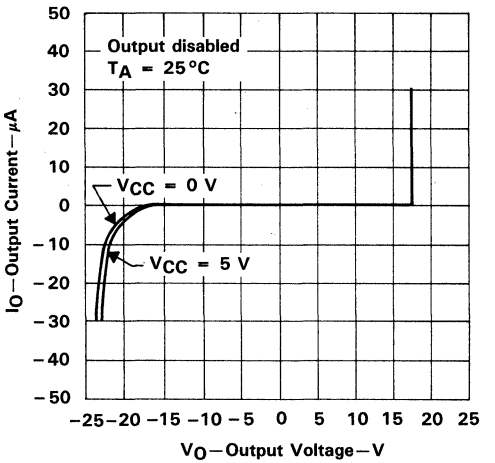


FIGURE 8

TYPICAL CHARACTERISTICS

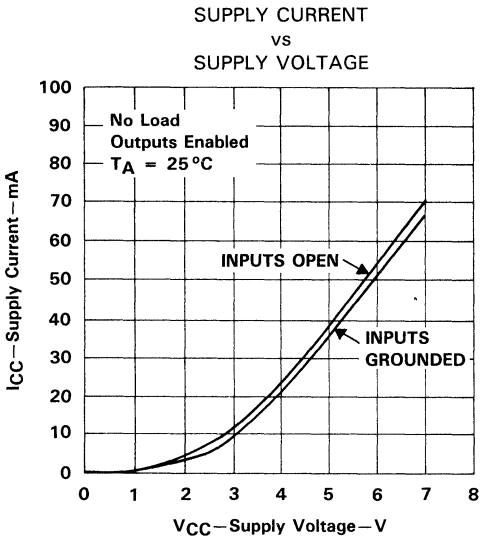


FIGURE 9

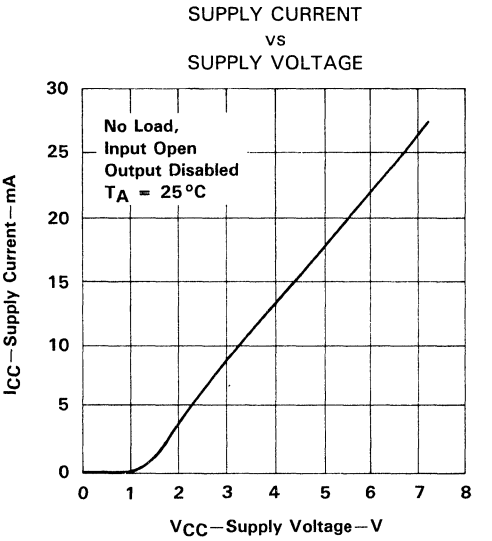
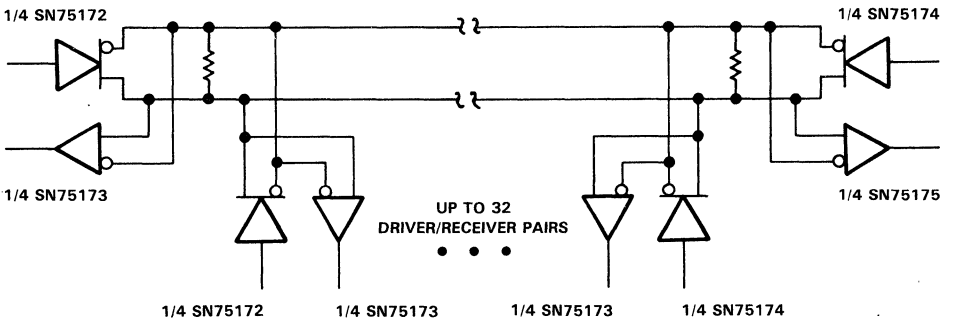


FIGURE 10

TYPICAL APPLICATION



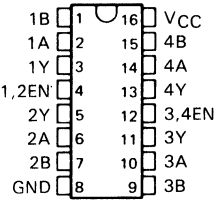
NOTE: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 11

D2602, OCTOBER 1980—REVISED SEPTEMBER 1989

- **Meets EIA Standards RS-422-A, RS-423-A, and RS-485**
- **Meets CCITT Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Input Voltage Range −12 V to 12 V**
- **Input Sensitivity . . . ±200 mV**
- **Input Hysteresis . . . 50 mV Typ**
- **High Input Impedance . . . 12 kΩ Min**
- **Operates from Single 5-V Supply**
- **Low Power Requirements**
- **Plug-in Replacement for MC3486**

D, J, OR N PACKAGE
(TOP VIEW)



description

The SN75175 is a monolithic quadruple differential line receiver with 3-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A, RS-423-A, and RS-485 and several CCITT recommendations. The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. Each of the two pairs of receivers has a common active-high enable.

The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of ±12 V. The SN75175 is designed for optimum performance when used with the SN75172 or SN75174 quadruple differential line drivers.

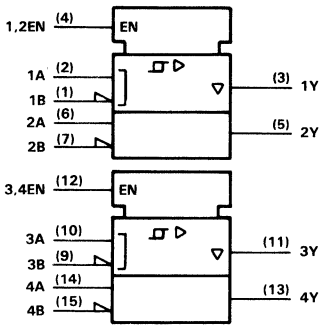
The SN75175 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUTS A − B	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \geq -0.2$ V	H	L
X	L	Z

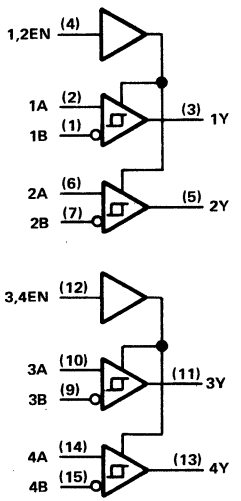
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbol†

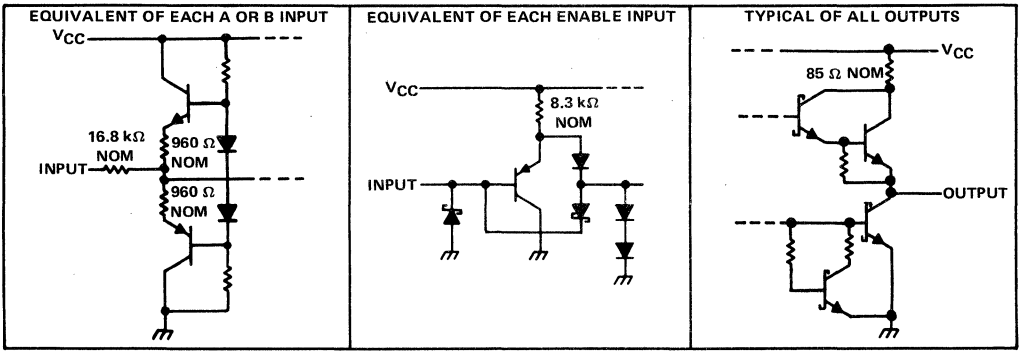


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, A or B inputs . . . . . ±25 V
Differential input voltage (see Note 2) . . . . . ±25 V
Enable input voltage . . . . . 7 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
D package . . . . . 950 mW
J package . . . . . 1025 mW
N Package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . −300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . −260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the D package to 608 mW at 70°C at the rate of 7.6 mW/°C, the J package to 656 mW at 70°C at the rate of 8.2 mW/°C, and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75175 chips are glass mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±12	V
Differential input voltage, V_{ID}			±12	V
High-level enable input voltage, V_{IH}	2			V
Low-level enable input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V, I_O = −0.4 mA				0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V, I_O = 16 mA		−0.2‡			V
V_{hys}	Hysteresis§				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = −400 μA, See Figure 1		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 1	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input at 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current¶			−15		−85	mA
I_{CC}	Supply current	Outputs disabled				70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.
§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
¶ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
NOTE 4: Refer to EIA standards RS-422-A, RS-423-A, and RS-485 for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 2		22	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			25	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 3		13	30	ns
t_{PZL}	Output enable time to low level			19	30	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF, See Figure 3		26	35	ns
t_{PLZ}	Output disable time from low level			25	35	ns

PARAMETER MEASUREMENT INFORMATION

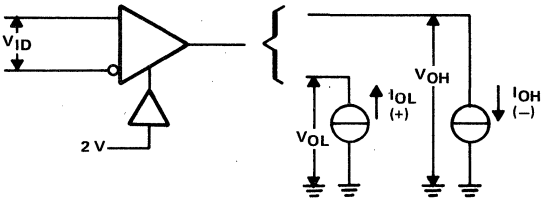


FIGURE 1. V_{OH}, V_{OL}

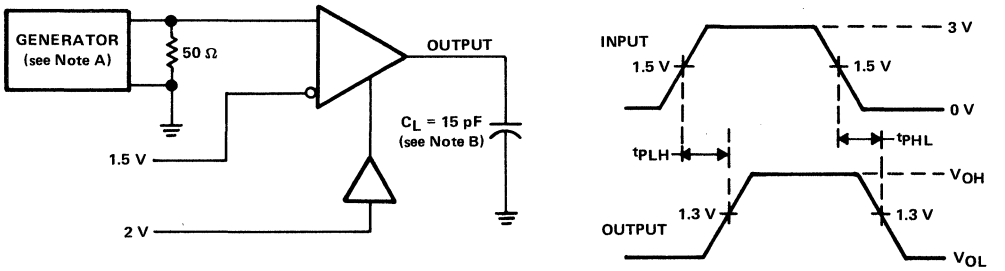
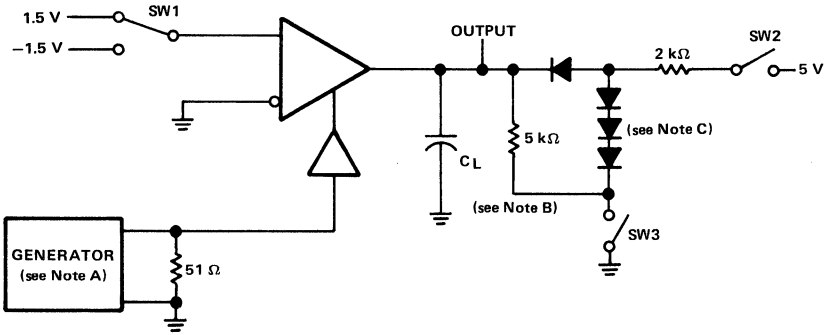


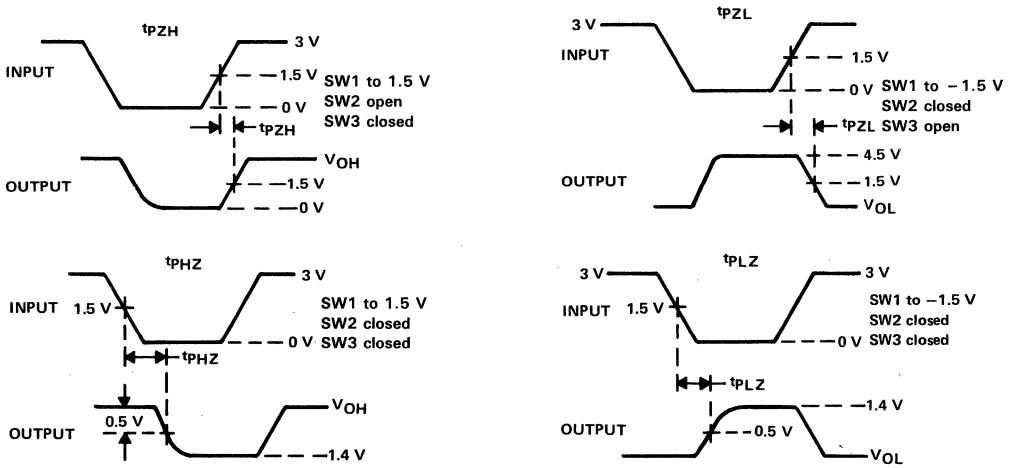
FIGURE 2. PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and stray capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3. ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_f ≤ 6 ns, t_r ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or equivalent.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

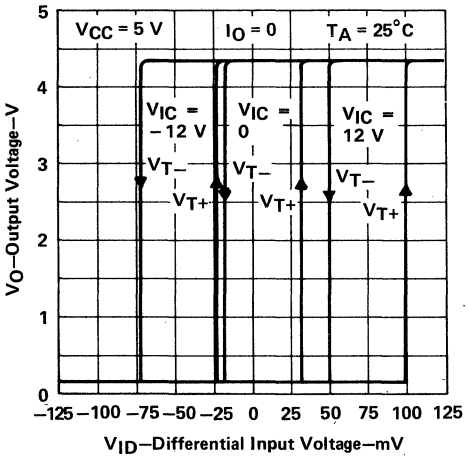


FIGURE 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

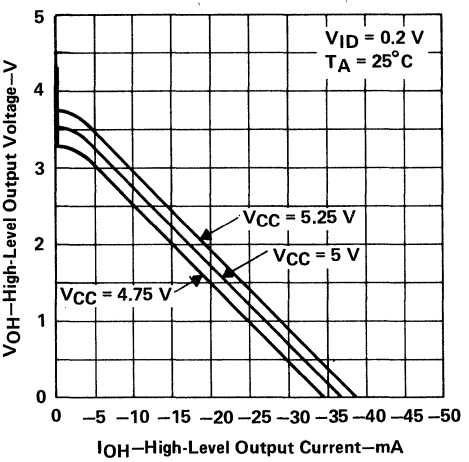


FIGURE 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

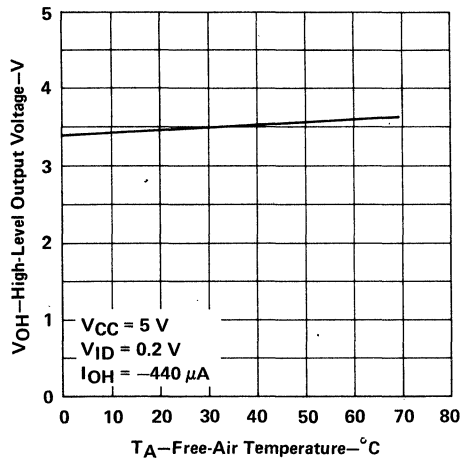


FIGURE 6

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

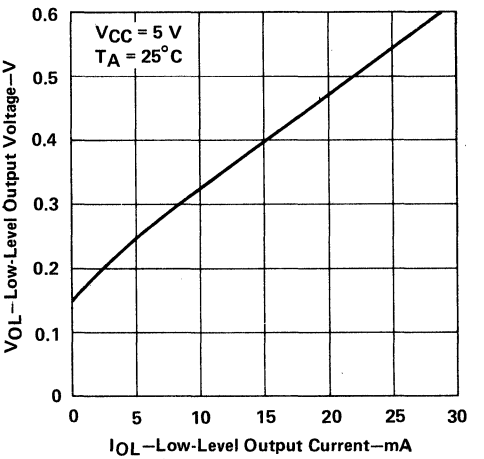


FIGURE 7

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

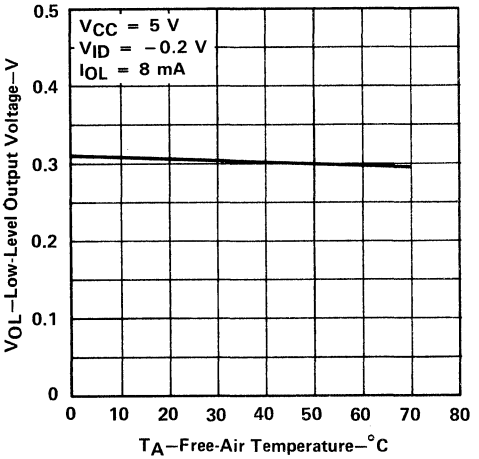


FIGURE 8

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

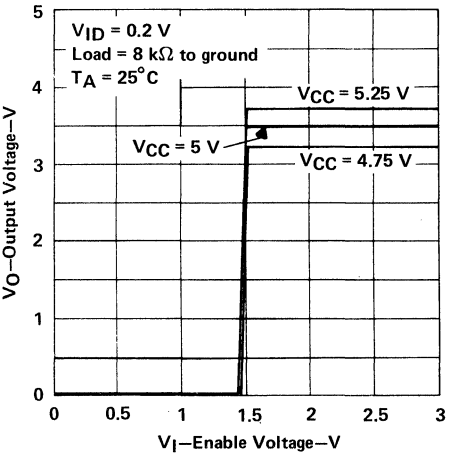


FIGURE 9

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

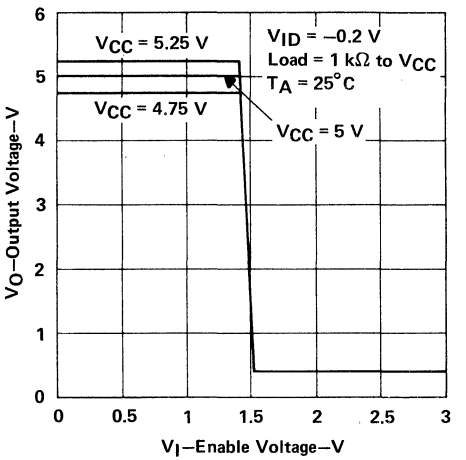


FIGURE 10

SUPPLY CURRENT
(ALL RECEIVERS)
vs
SUPPLY VOLTAGE

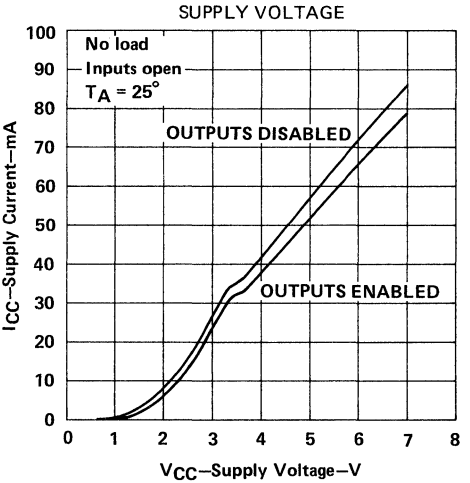


FIGURE 11

TYPICAL CHARACTERISTICS

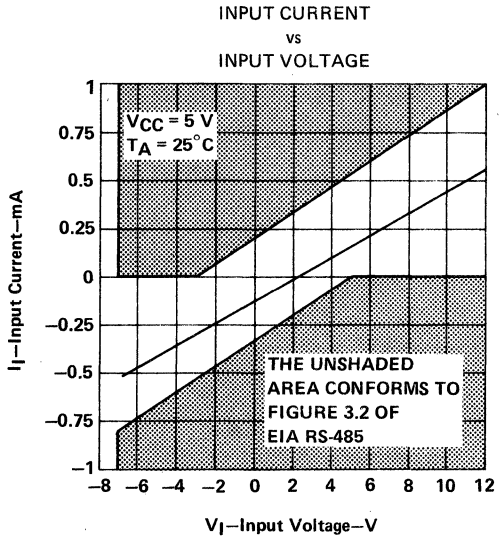


FIGURE 12

TYPICAL APPLICATION

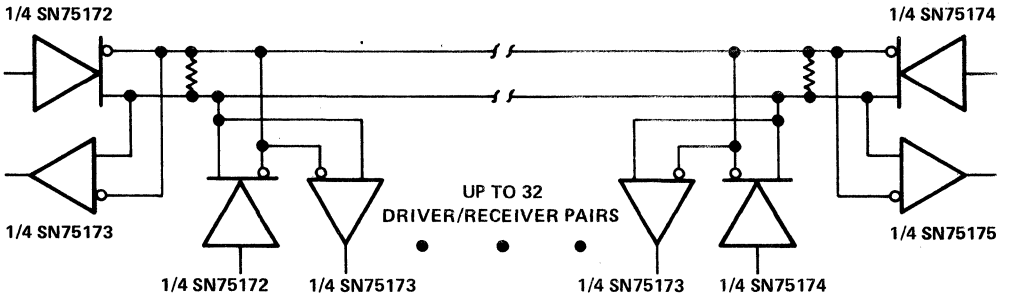


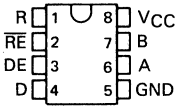
FIGURE 13

NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

D2619, JUNE 1984—REVISED AUGUST 1989

- Bidirectional Transceiver
- Meets EIA Standards RS-422A and CCITT Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability. . . ±60 mA Max
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-V Supply
- Low Power Requirements

D OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



FUNCTION TABLE (DRIVER)

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A − B	$\overline{RE}$	R
$V_{ID} \geq 0.2$ V	L	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

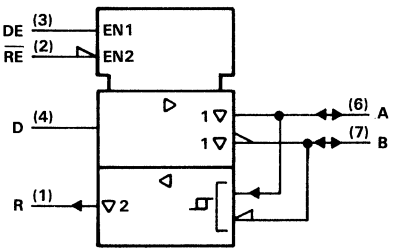
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

description

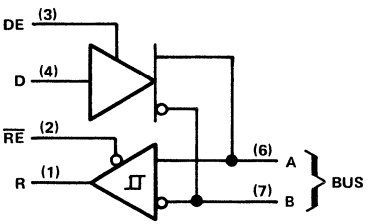
The SN75176A differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meets EIA Standard RS-422A and CCITT Recommendations V.11 and X.27.

The SN75176A combines a 3-state differential line driver and a differential-input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

logic symbol



logic diagram (positive logic)

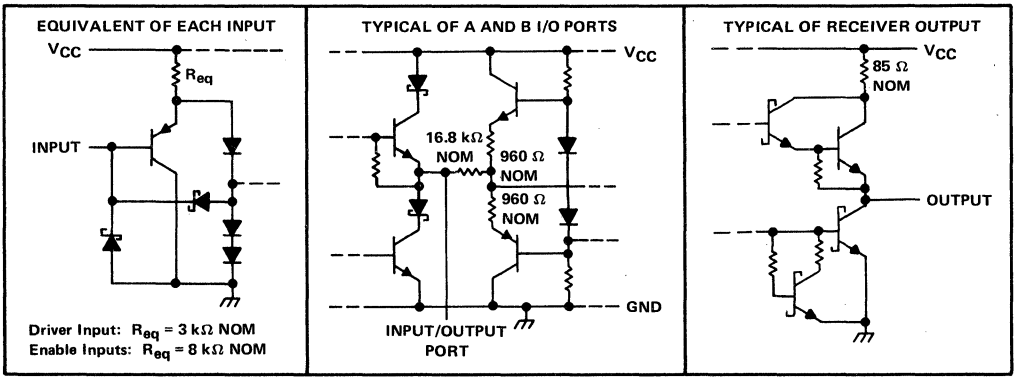


description (continued)

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN75176A can be used in transmission line applications employing the SN75172 and SN75174 quadruple differential line drivers and the SN75173 and SN75175 quadruple differential line receivers.

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage at any bus terminal . . . . . −10 V to 15 V
Enable input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
D package . . . . . 725 mW
P package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the D package to 464 mW at 70°C at the rate of 5.8 mW/°C and derate the P package to 640 mW at 70°C at the rate of 8.0 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common-mode), V_I or V_{IC}		−7		12	V
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 3)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

NOTE 3: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, I_{OH} = −33 mA	V_{IL} = 0.8 V,		3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, I_{OL} = 33 mA	V_{IL} = 0.8 V,		1.1		V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0				2 V_{OD2}	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω,	See Figure 1	2	2.7		V
		R_L = 54 Ω,	See Figure 1	1.5	2.4		
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡					±0.2	V
V_{OC}	Common-mode output voltage§	R_L = 54 Ω or 100 Ω,	See Figure 1			3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡					±0.2	V
I_O	Output current	Output disabled, See Note 4	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = V_{CC}				250	
		V_O = 12 V				500	
I_{CC}	Supply current (total package)	No load	Outputs enabled		35	50	mA
			Outputs disabled		26	40	

†All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡$\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
§In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-422A for exact conditions.

driver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 60 Ω,	See Figure 3		40	60	ns
t_{TD}	Differential-output transition time				65	95	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		55	90	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		30	50	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4		85	130	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5		20	40	ns

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
$V_{T+} - V_{T-}$	Hysteresis§				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		35	50	mA
			Outputs disabled		26	40	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-422A for exact conditions.

receiver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V,			21	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	See Figure 6		23	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 7		10	30	ns
t_{PZL}	Output enable time to low level				12	30	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 7		20	35	ns
t_{PLZ}	Output disable time from low level				17	35	ns

PARAMETER MEASUREMENT INFORMATION

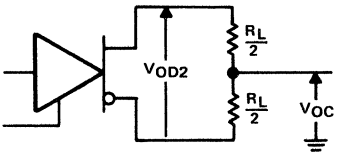


FIGURE 1. DRIVER V_{OD} AND V_{OC}

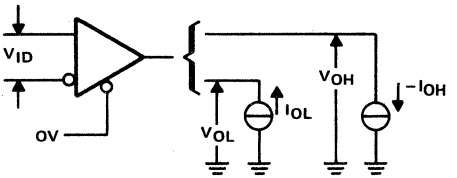
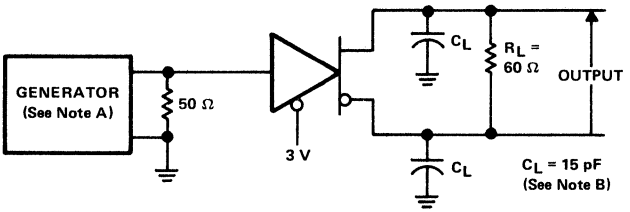
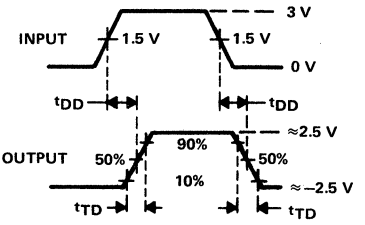


FIGURE 2. RECEIVER V_{OH} AND V_{OL}

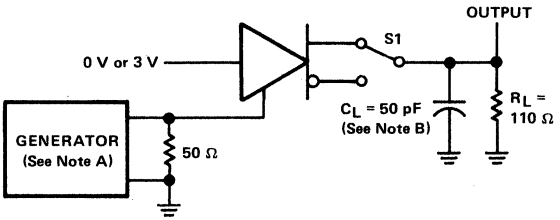


TEST CIRCUIT

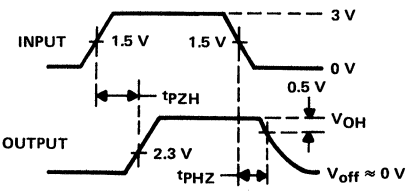


VOLTAGE WAVEFORMS

FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

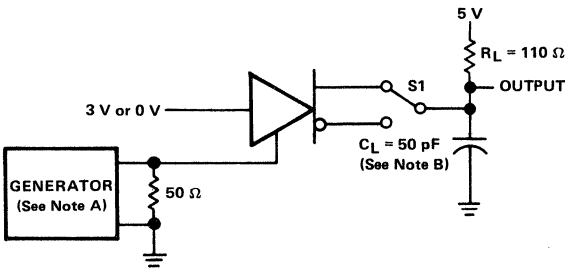


TEST CIRCUIT

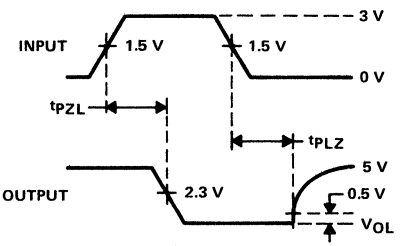


VOLTAGE WAVEFORMS

FIGURE 4. DRIVER ENABLE AND DISABLE TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

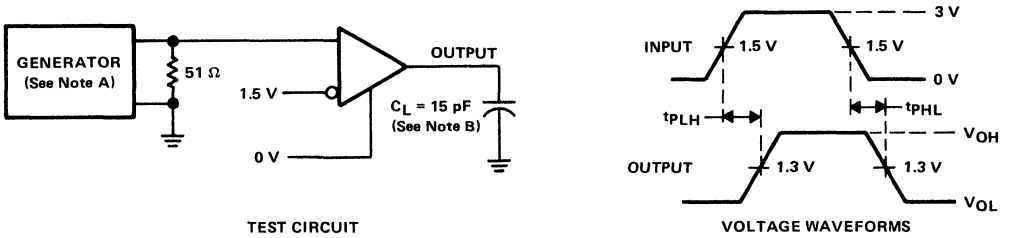


FIGURE 6. RECEIVER PROPAGATION DELAY TIMES

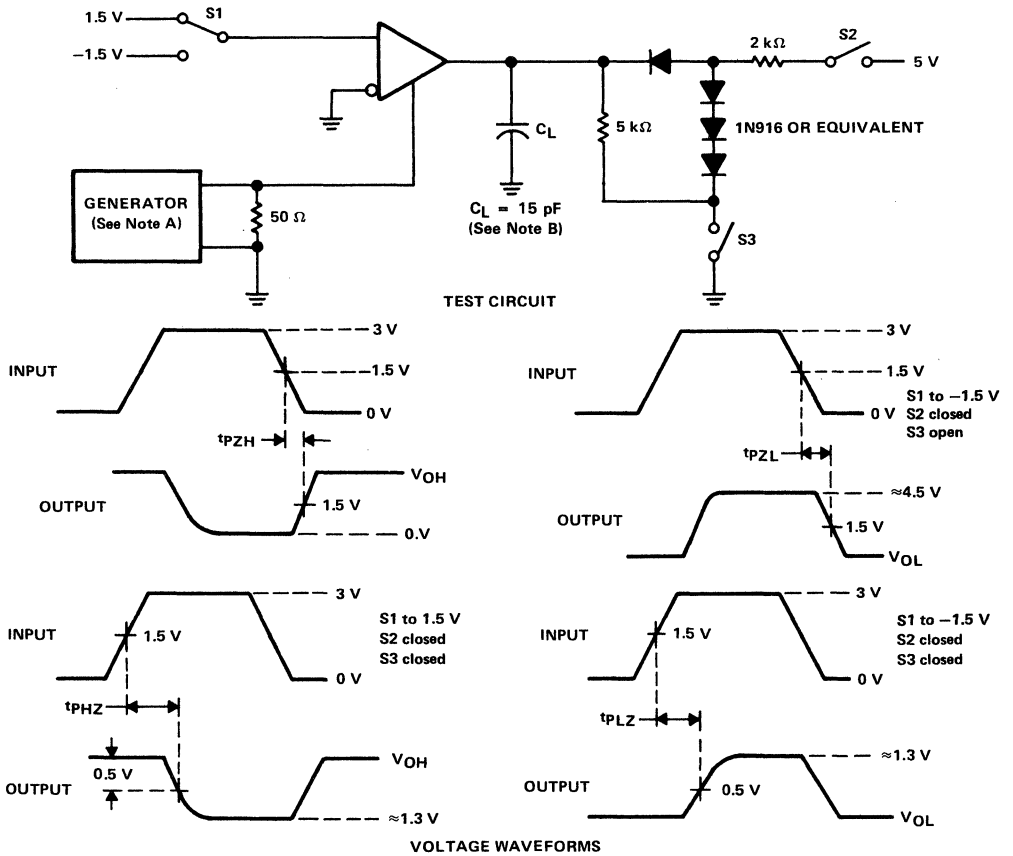


FIGURE 7. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_{out} = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

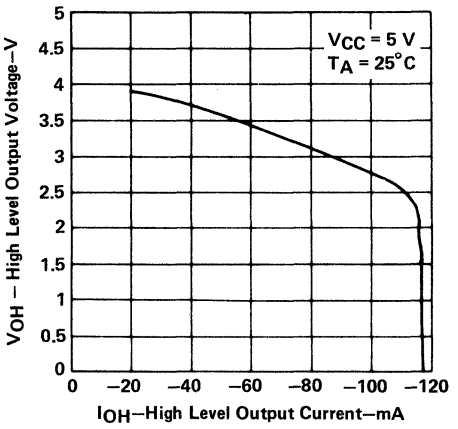


FIGURE 8

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

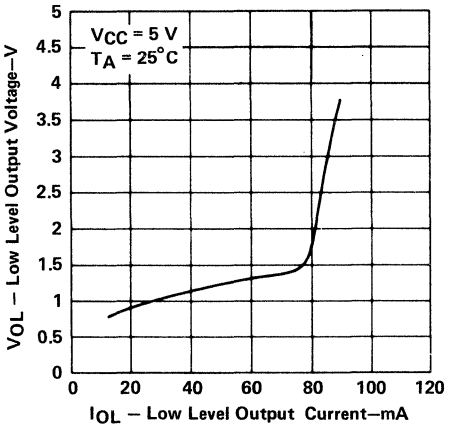


FIGURE 9

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

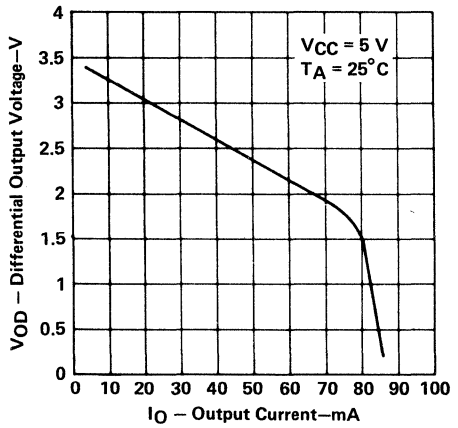


FIGURE 10

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

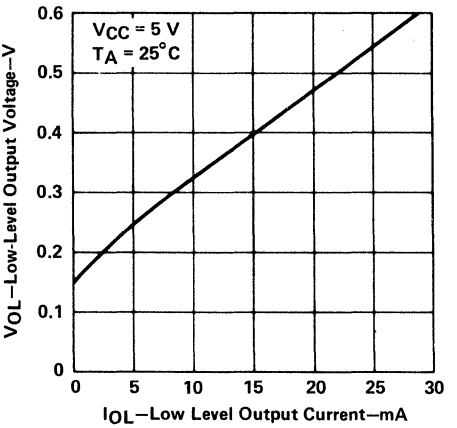


FIGURE 11

TYPICAL CHARACTERISTICS

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

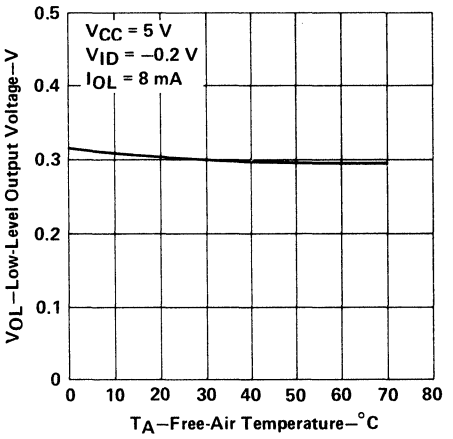


FIGURE 12

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

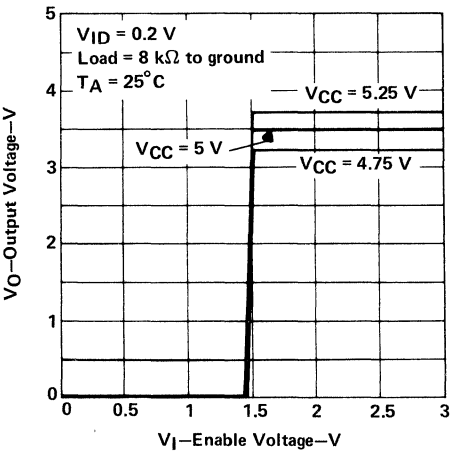


FIGURE 13

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

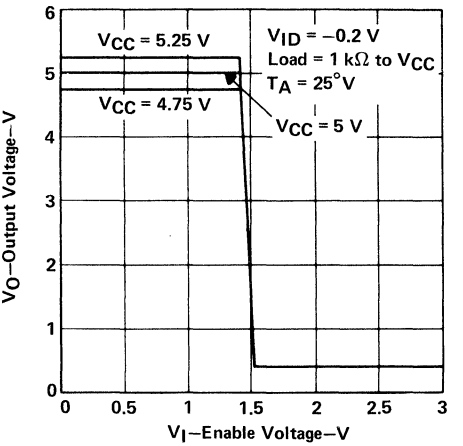
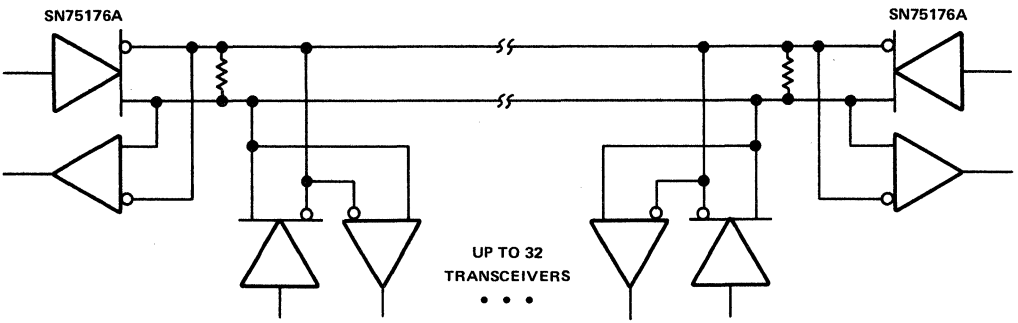


FIGURE 14

TYPICAL APPLICATION



NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

TEXAS INSTRUMENTS
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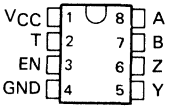
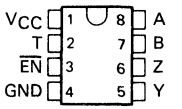
D2606, JULY 1985—REVISED JANUARY 1990

- Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Bus Voltage Range . . . −7 V to 12 V
- Positive and Negative Current Limiting
- Driver Output Capability . . . 60 mA Max
- Driver Thermal Shutdown Protection
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-V Supply
- Low Power Requirements

SN75177B . . . D, JG, OR P PACKAGE
(TOP VIEW)



SN75178B . . . JG OR P PACKAGE
(TOP VIEW)



SN75177B FUNCTION TABLE

DIFFERENTIAL INPUTS A−B	ENABLE EN	OUTPUTS T	Y	Z
$V_{ID} \geq 0.2$ V	H	H	H	L
-0.2 V $< V_{ID} < 0.2$ V	H	?	?	?
$V_{ID} \leq 0.2$ V	H	L	L	H
X	L	Z	Z	Z

SN75178B FUNCTION TABLE

DIFFERENTIAL INPUTS A−B	ENABLE $\overline{EN}$	OUTPUTS T	Y	Z
$V_{ID} \geq 0.2$ V	L	H	H	L
-0.2 V $< V_{ID} < 0.2$ V	L	?	?	?
$V_{ID} \leq 0.2$ V	L	L	L	H
X	H	Z	Z	Z

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = impedance (off)

description

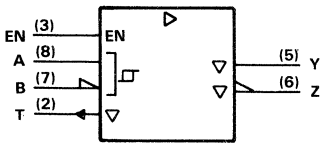
The SN75177B and SN75178B differential bus repeaters are monolithic integrated devices each designed for one-way data communication on multipoint bus transmission lines. These devices are designed for balanced transmission bus line applications and meet EIA Standard RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. Each device is designed to improve the performance of the data communication over long bus lines. The SN75177B and SN75178B are identical except for the complementary enable inputs, which allow the devices to be used in pairs for bidirectional communication.

The SN75177B and SN75178B feature positive- and negative-current limiting 3-state outputs for the receiver and driver. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of −7 V to 12 V. The driver features thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The driver is designed to drive current loads up to 60 mA maximum.

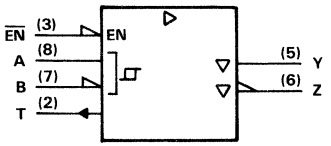
The SN75177B and SN75178B are designed for optimum performance when used on transmission buses employing the SN75172 and SN75174 differential line drivers, SN75173 and SN75175 differential line receivers, or SN75176B bus transceiver.

logic symbols†

SN75177B



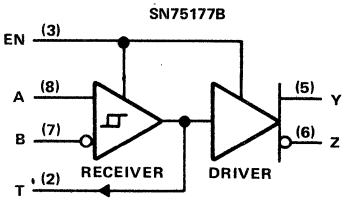
SN75178B



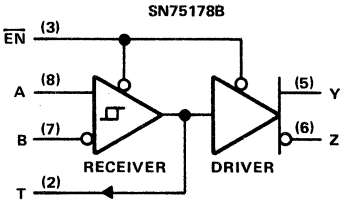
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

SN75177B

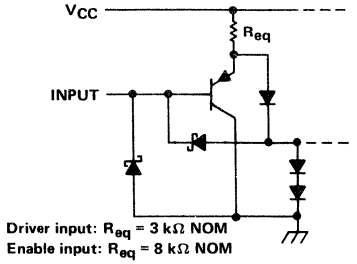


SN75178B

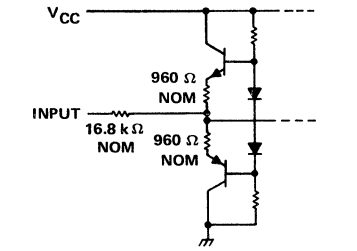


schematics of inputs and outputs

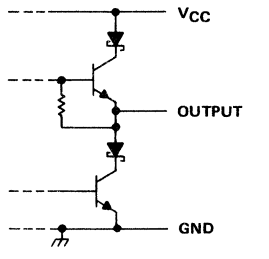
EQUIVALENT OF DRIVER OR ENABLE INPUT



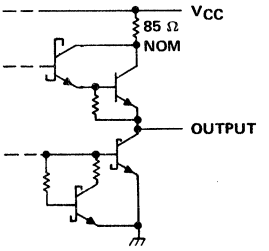
EQUIVALENT OF EACH RECEIVER INPUT



TYPICAL OF ALL DRIVER OUTPUTS



TYPICAL OF ALL RECEIVER OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage range at any bus terminal . . . . . −10 V to 15 V
Differential input voltage (see Note 2) . . . . . ±25 V
Enable input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
D package . . . . . 725 mW
JG package . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the D package to 464 mW at 70°C at the rate of 5.8 mW/°C, the JG package to 528 mW at 70°C at the rate of 6.6 mW/°C and the P package to 640 mW at 70°C at the rate of 8.0 mW/°C. In the JG package, SN75177B and SN75178B chips are glass mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	EN or $\overline{EN}$	2			V
Low-level linput voltage, V_{IL}	EN or $\overline{EN}$			0.8	V
Common-mode input voltage, V_{IC}		−7†		12	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

†The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1		½V_{OD1}			V
				2			
		R_L = 54 Ω, See Figure 1		1.5	2.5	5	V
$\|V_{OD3}\|$	Differential output voltage	See Note 4		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡	R_L = 54 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage					3	V
						−1	
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡					±0.2	V
I_O	Output current	V_{CC} = 0, V_O = −7 V to 12 V				±100	μA
I_{OZ}	High-impedance-stage output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current (total package)	No load	Outputs enabled		57	70	mA
			Outputs disabled		26	35	

†All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡$\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
NOTE 4: See EIA Standard RS-485 from Figure 3.5, Test Termination Measurement 2.

driver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω, See Figure 3		15	22	ns
t_{TD}	Differential-output transition time			20	30	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See Figure 4		85	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See Figure 5		40	60	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, See Figure 4		150	250	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See Figure 5		20	30	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test termination Measurement 2)
$\Delta\|V_{OD}\|$	$\|\ \|V_t\| - \|\overline{V}_t\|\ \|$	$\|\ \|V_t\| - \|\overline{V}_t\|\ \|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|\ V_{os} - \overline{V}_{os}\ \|$	$\|\ V_{os} - \overline{V}_{os}\ \|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis§				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				20	μA
						−400	
I_I	Line input current	Other input at 0 V, See Note 5	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−200	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		57	70	mA
			Outputs disabled		26	35	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 12.
NOTE 5: Refer to EIA Standard RS-422 for exact conditions.

receiver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V,			19	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	See Figure 6		30	40	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 7		10	20	ns
t_{PZL}	Output enable time to low level				12	20	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 8		25	35	ns
t_{PLZ}	Output disable time from low level				17	25	ns

PARAMETER MEASUREMENT INFORMATION

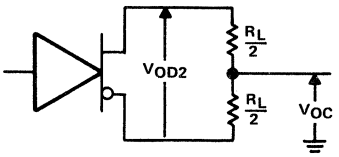


FIGURE 1. DRIVER V_{OD} AND V_{OC}

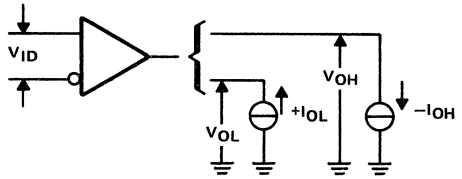


FIGURE 2. RECEIVER V_{OH} AND V_{OL}

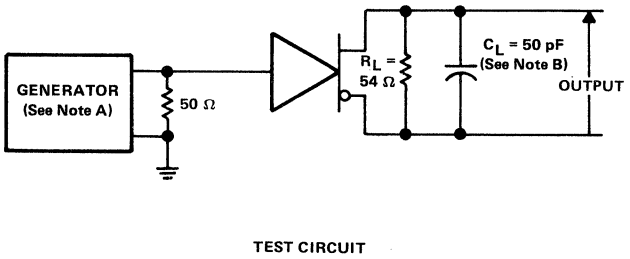


FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

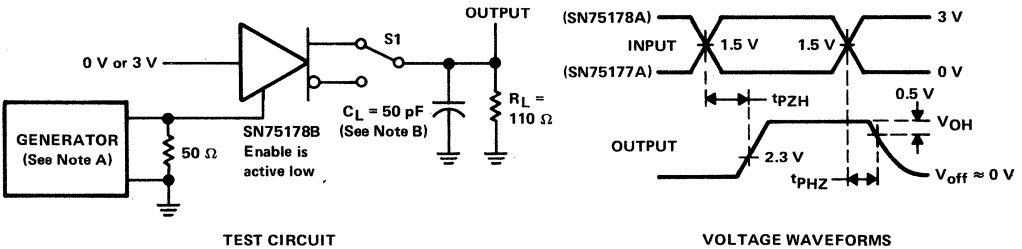
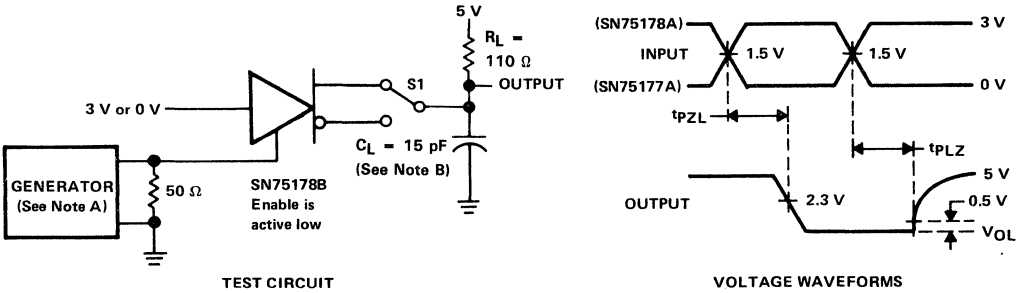


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES (t_{PZH}, t_{PHZ})

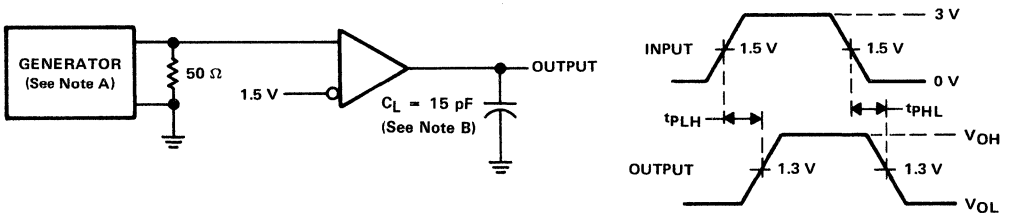
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 5. DRIVER ENABLE AND DISABLE TIMES (t_{PZL}, t_{PLZ})

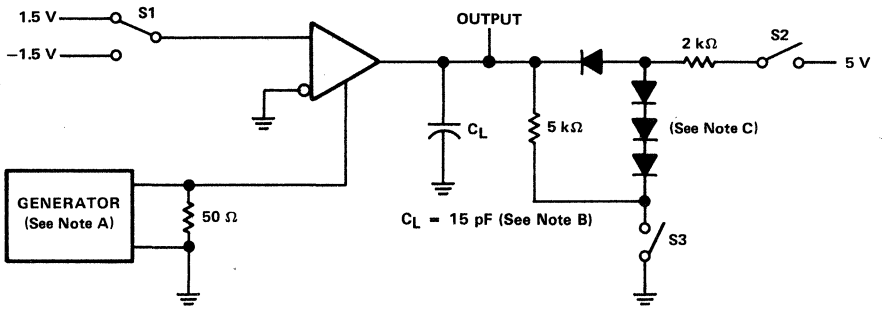


TEST CIRCUIT VOLTAGE WAVEFORMS

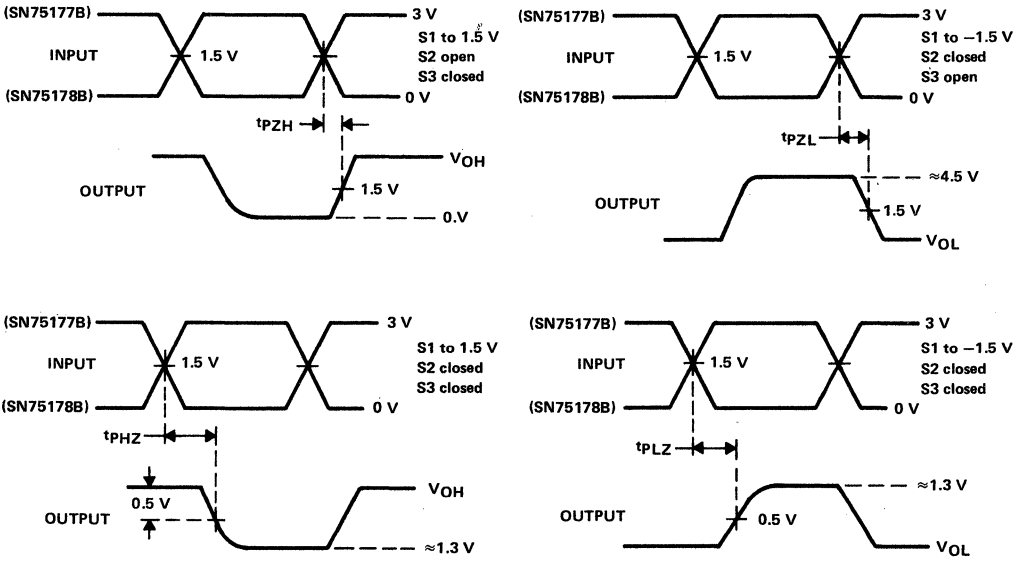
FIGURE 6. RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≈ 50%, $t_r = t_f = 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

FIGURE 7. RECEIVER ENABLE AND DISABLE TIMES

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

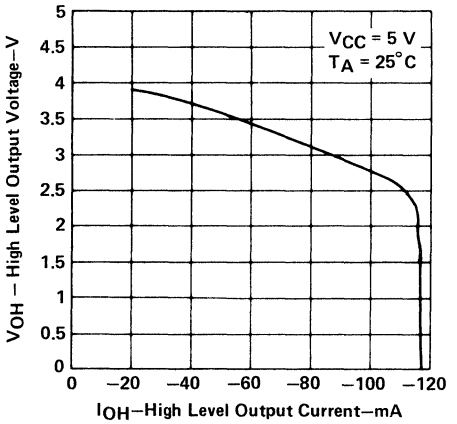


FIGURE 8

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

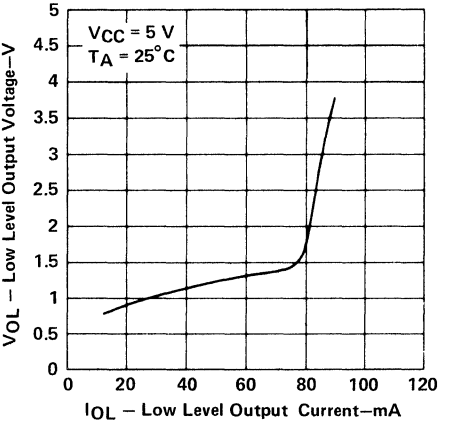


FIGURE 9

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

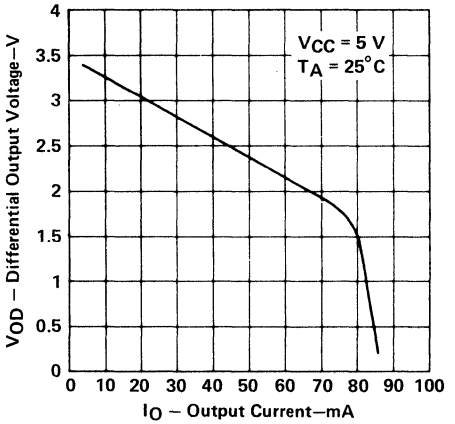


FIGURE 10

RECEIVER OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

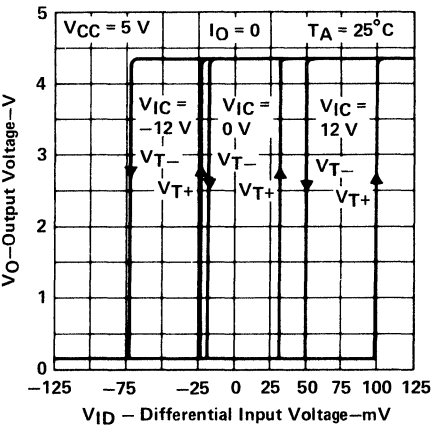


FIGURE 11

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

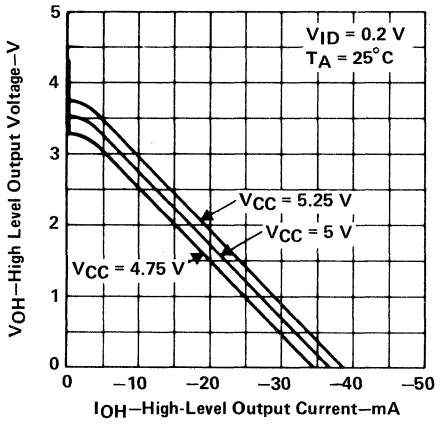


FIGURE 12

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

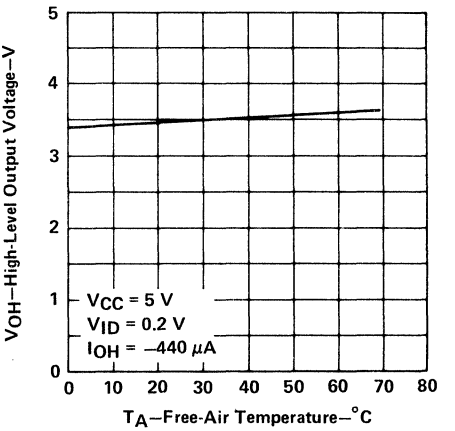


FIGURE 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

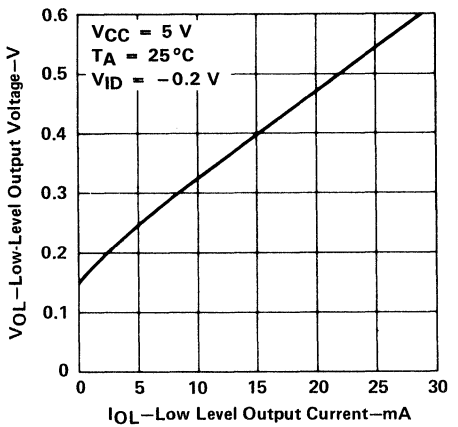


FIGURE 14

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

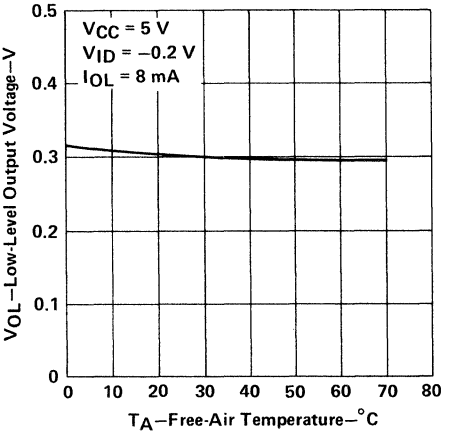
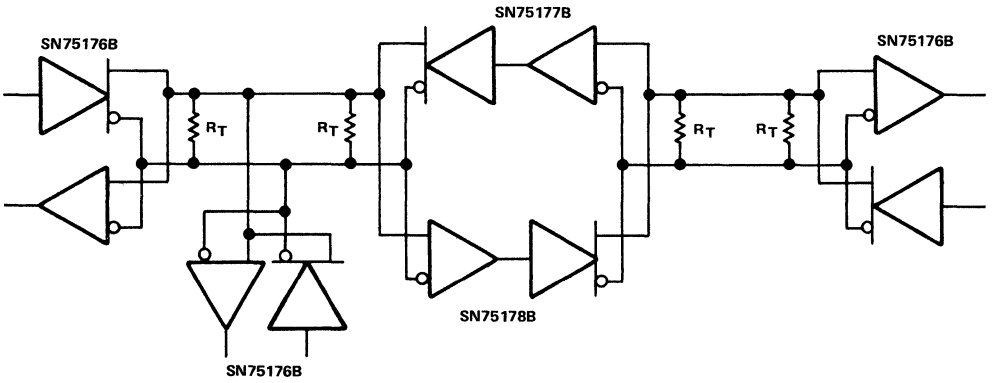


FIGURE 15

APPLICATION INFORMATION



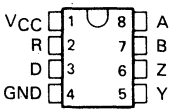
NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 16. TYPICAL APPLICATION CIRCUIT

D2845, OCTOBER 1985—REVISED AUGUST 1989

- Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27
- Bus Voltage Range . . . −7 V to 12 V
- Positive and Negative Current Limiting
- Driver Output Capability . . . 60 mA Max
- Driver Thermal Shutdown Protection
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-V Supply
- Low Power Requirements

D, JG, OR P PACKAGE
(TOP VIEW)



FUNCTION TABLE (DRIVER)

INPUT	OUTPUTS	
D	Y	Z
H	H	L
L	L	H

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS	OUTPUT
A − B	R
$V_{ID} \geq 0.2$ V	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	?
$V_{ID} \leq -0.2$ V	L

H = high level, L = low level, ? = indeterminate

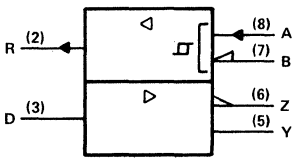
description

The SN75179B driver and bus receiver circuit is a monolithic integrated device designed for balanced transmission line applications and meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. It is designed to improve the performance of full-duplex data communications over long bus lines.

The SN75179B driver outputs provide limiting for both positive and negative currents. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of −12 V to 12 V. The driver provides thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The device is designed to drive current loads of up to 60 mA maximum.

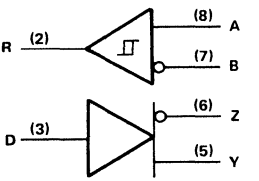
The SN75179B is characterized for operation from 0°C to 70°C.

logic symbol†

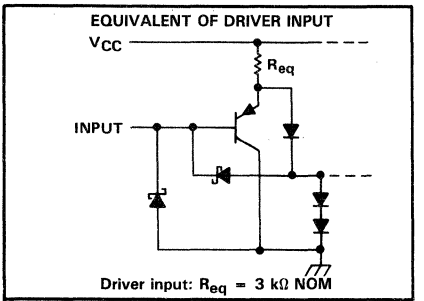


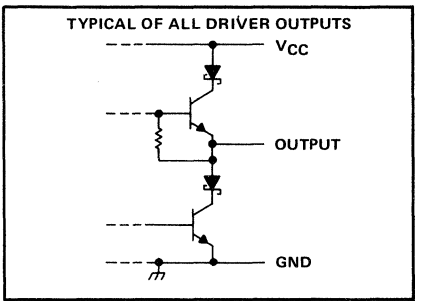
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

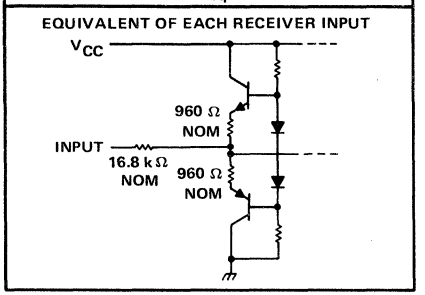
logic diagram

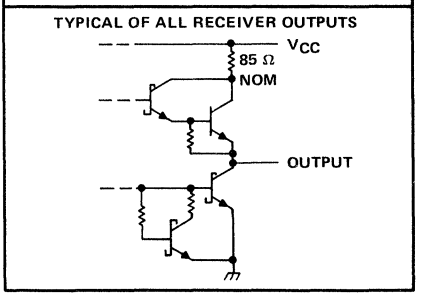


schematics of inputs and outputs









absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage at any bus terminal . . . . . −10 V to 15 V
Differential input voltage (see Note 2) . . . . . ±25 V
Continuous total dissipation at (or below 25 °C free-air temperature (see Note 3):
D package . . . . . 725 mW
JG package . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260 °C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300 °C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25 °C free-air temperature, derate the D package to 464 mW at 70 °C at the rate of 5.8 mW/°C , the JG package to 528 mW at 70 °C at the rate of 6.6 mW/ °C and the P package to 640 mW at 70 °C at the rate of 8.0 mW/ °C..
In the JG package SN75179B, chips are glass mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	Driver	2			V
Low-level input voltage, V_{IL}	Driver			0.8	V
Common-mode input voltage, V_{IC}		−7†		12	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

† The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω,	See Figure 1	$\frac{1}{2}V_{OD1}$			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
$\|V_{OD3}\|$	Differential output voltage	See Note 4		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§					±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω,	See Figure 1			+3 −1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	V_{CC} = 0,	V_O = −7 V to 12 V			±100	μA
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−200	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = V_{CC} or 12 V				250	
I_{CC}	Supply current (total package)	No load			57	70	mA

‡All typical values are at V_{CC} = 5 V and T_A = 25°C.
§$\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
NOTE 4: See EIA Standard RS-485, Figure 3.5, Test Termination Measurement 2.

driver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω,	See Figure 3		15	22	ns
t_{TD}	Differential-output transition time				20	30	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1}\rvert$	V_o	V_o
$\lvert V_{OD2}\rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3}\rvert$		V_t (Test termination Measurement 2)
$\Delta\lvert V_{OD}\rvert$	$\lvert\,\lvert V_t\rvert - \lvert\overline{V}_t\rvert\,\rvert$	$\lvert\,\lvert V_t\rvert - \lvert\overline{V}_t\rvert\,\rvert$
V_{OC}	$\lvert V_{os}\rvert$	$\lvert V_{os}\rvert$
$\Delta\lvert V_{OC}\rvert$	$\lvert V_{os} - \overline{V}_{os}\rvert$	$\lvert V_{os} - \overline{V}_{os}\rvert$
I_{OS}	$\lvert I_{sa}\rvert$, $\lvert I_{sb}\rvert$	
I_O	$\lvert I_{xa}\rvert$, $\lvert I_{xb}\rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis§				50		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_I	Line input current	Other input at 0 V, See Note 5	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
r_i	Input resistance			12			kΩ
i_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load			57	70	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.
NOTE 5: Refer to EIA Standard RS-422-A for exact conditions.

receiver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF, See Figure 4		19	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			30	40	ns

PARAMETER MEASUREMENT INFORMATION

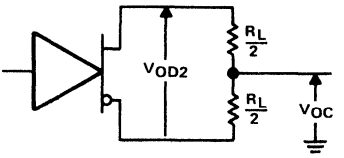


FIGURE 1. DRIVER V_{OD} AND V_{OC}

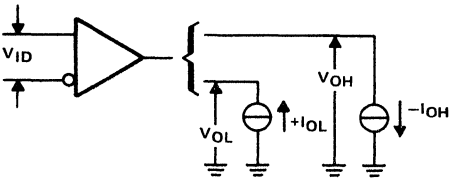
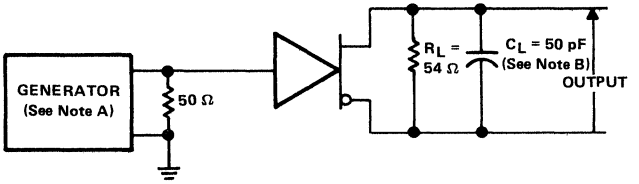
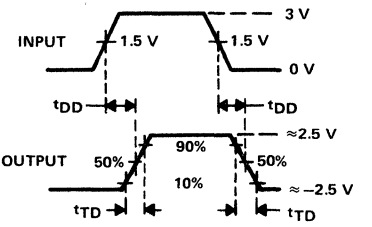


FIGURE 2. RECEIVER V_{OH} AND V_{OL}

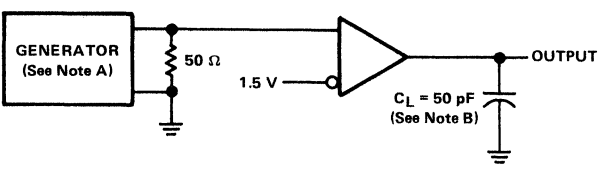


TEST CIRCUIT

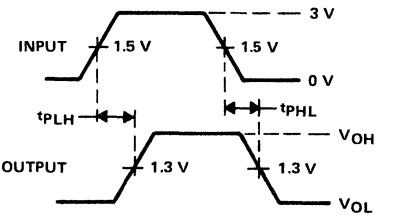


VOLTAGE WAVEFORMS

FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4. RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

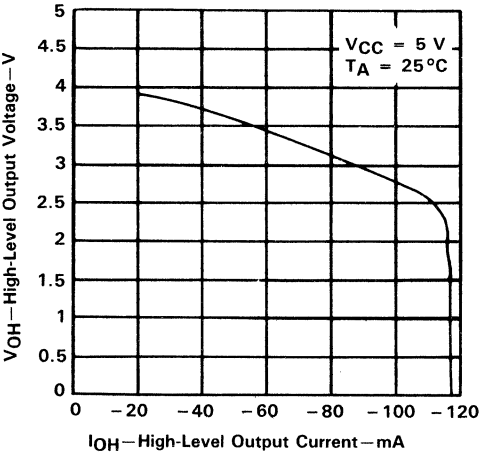


FIGURE 5

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

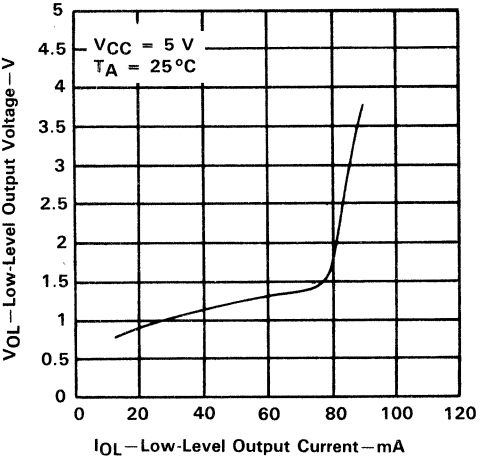


FIGURE 6

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

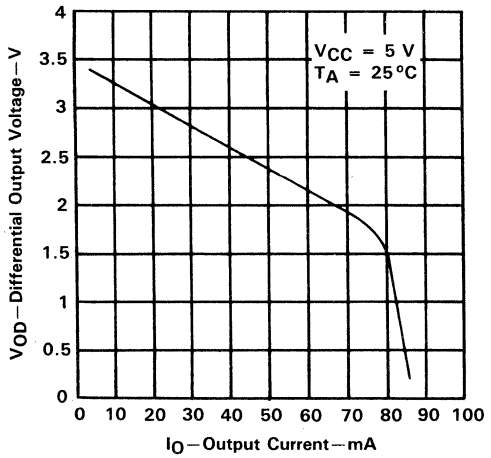


FIGURE 7

RECEIVER OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

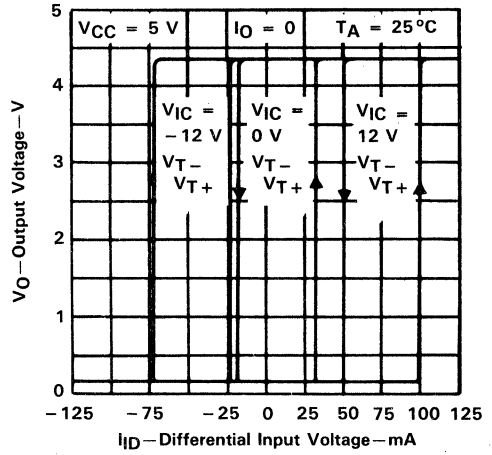


FIGURE 8

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

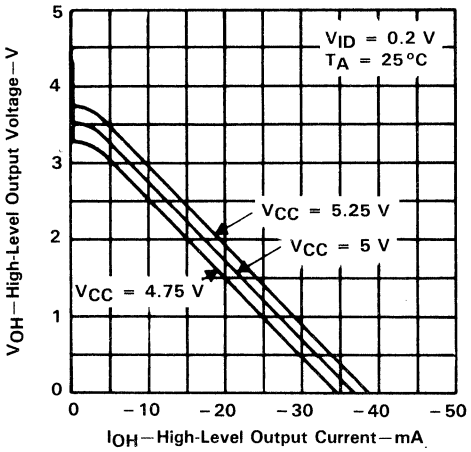


FIGURE 9

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

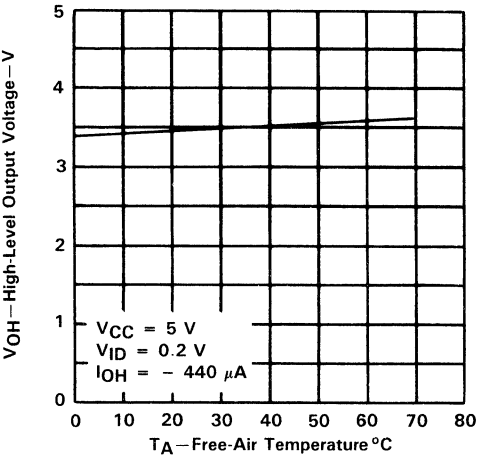


FIGURE 10

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

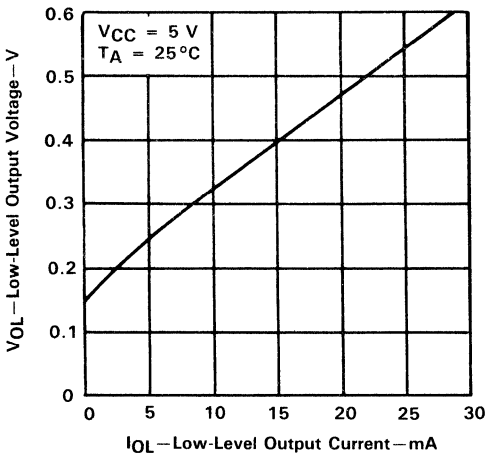


FIGURE 11

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

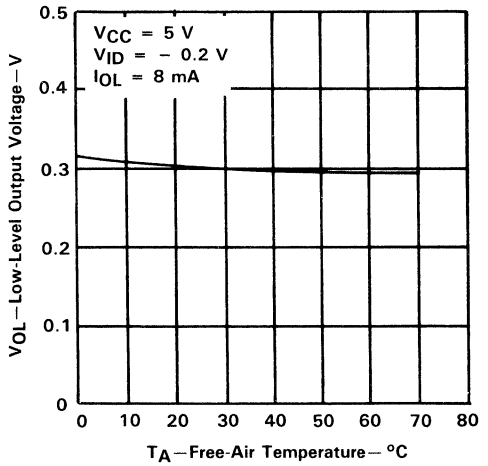
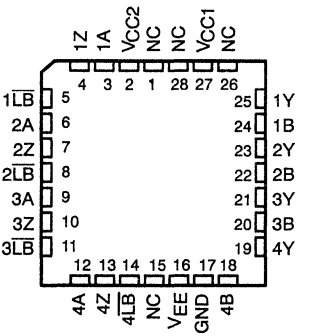


FIGURE 12

D3389, FEBRUARY 1990

- **Meets Standards RS-232-C, EIA-232-D, and CCITT V.28**
- **Four Independent Drivers and Receivers**
- **Loopback Mode Functionally Self-Tests Drivers and Receivers Without Disconnection From Line**
- **Driver Slew Rate Limited to 30 V/μs Max**
- **Built-in Receiver 1-μs Noise Filter**
- **Internal Thermal Overload Protection**
- **EIA-232-D Inputs and Outputs Withstand ± 30V**
- **Low Supply Current . . . 2.5 mA Typ**
- **ESD Protection Exceeds 2000 V Per MIL-STD-833C Method 3015**

FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN75186 is a low-power bipolar device containing four driver/receiver pairs designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). Additionally, the SN75186 has a loopback mode that may be used by a data communication system to perform a functional self test on each driver/receiver pair, removing the need to locally disconnect cables and install a loopback connector. Flexibility of control is ensured by each driver/receiver pair having its own loopback control input. The SN75186 is designed to conform to standards RS-232-C, its revision ANSI/EIA-232-D-1986, and CCITT V.28.

The maximum slew rate is limited to 30 V/μs at the driver outputs and drives a capacitive load of 2500 pF at 20 kBaud. The receivers have input filters that disregard input noise pulses shorter than 1 μs. The SN75186 is a robust device capable of withstanding ± 30 V at driver outputs and at receiver inputs whether powered or unpowered. This device has an internal ESD protection rated at 2 kV to prevent functional failures.

The SN75186 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH RECEIVER)

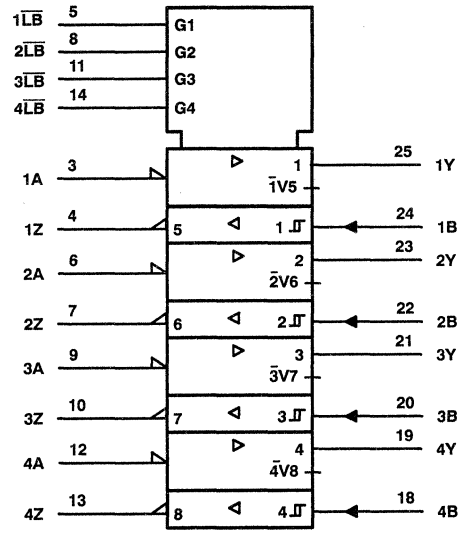
LOOPBACK	INPUTS		OUTPUT
$\overline{LB}$	A	B†	Z
H	X	H	L
H	X	L	H
L	L	X	L
L	H	X	H

FUNCTION TABLE (EACH DRIVER)

LOOPBACK	INPUT	OUTPUT
$\overline{LB}$	A	Y†
H	H	L
H	L	H
L	X	L

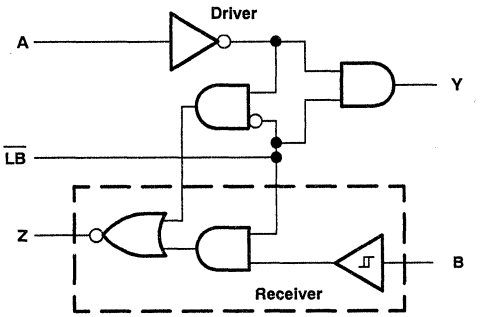
† Voltages are RS-232-C, EIA-232-D, and V.28 levels
H = high level, L = low level, X = irrelevant

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

logic diagram, each driver/receiver pair (positive logic)



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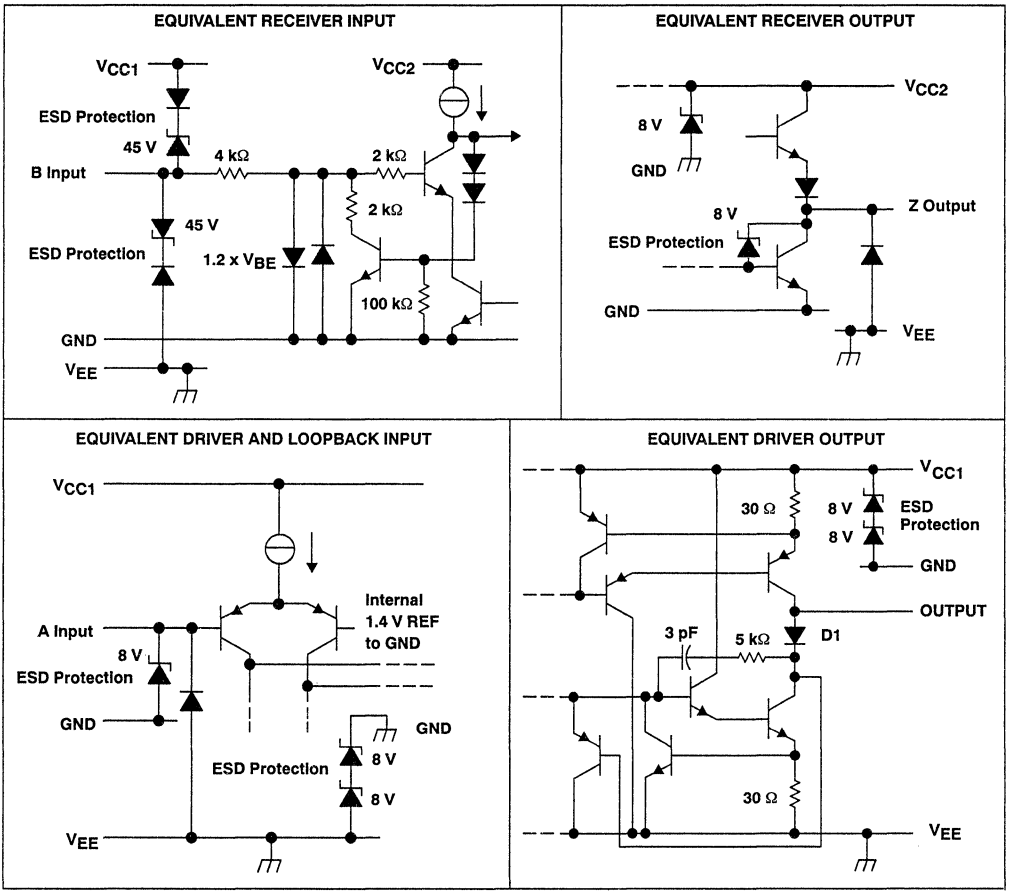
schematics of inputs and outputs



All component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) ..... 15 V
Supply voltage, V_{CC2} ..... 7 V
Supply voltage, V_{EE} ..... −15 V
Receiver input voltage range ..... −30 V to 30 V
Driver input voltage range ..... (V_{EE} + 2 V) to V_{CC1} V
Loopback input voltage range ..... 0 V to 7 V
Driver output voltage range ..... −30 V to 30 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 1400 mW
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 10 seconds ..... 260°C

NOTES: 1. All voltages are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly to 896 mW at 70°C at the rate of 11.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	13.2	V
Supply voltage, V_{CC2}		4.5	5	5.5	V
Supply voltage, V_{EE}		−10.8	−12	−13.2	V
Input voltage, V_I	Driver and loopback	0		V_{CC2}	V
Input voltage, V_I (see Note 3)	Receiver			± 30	V
High-level input voltage, V_{IH}	Driver and loopback	2			V
Low-level input voltage, V_{IL}	Driver and loopback			0.8	V
Output voltage, V_O, powered on or off	Driver			± 30	V
High-level output current, I_{OH}	Receiver			−4	mA
Low-level output current, I_{OL}	Receiver			4	mA
Operating free-air temperature, T_A		0		70	°C

NOTE 3: If all receiver inputs are held at ± 30 V, the thermal dissipation limit of the package may be exceeded. The thermal shutdown may not protect the device, as this dissipation occurs in the receiver input resistors.

DRIVER SECTION

driver electrical characteristics over full recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	R_L = 3 kΩ,	V_{IL} = 0.8 V,	See Figure 1	7			V
V_{OL}	Low-level output voltage‡	R_L = 3 kΩ,	V_{IH} = 2 V,	See Figure 1			–7	V
$V_{OH(LB)}$	High-level output voltage in loopback mode‡§¶	R_L = 3 kΩ,	$\overline{LB}$ at 0.8 V,	V_{IL} = 0.8 V			–7	V
I_{IH}	High-level input current (driver and loopback inputs)#	V_I = 5 V,	See Figure 2				100	μA
I_{IL}	Low-level input current (driver and loopback inputs)#	V_I = 0,	See Figure 2				– 100	μA
$I_{OS(H)}$	High-level short-circuit output current	V_I = 0.8 V, V_O = 0, See Note 4 and Figure 1			– 10	– 20	– 35	mA
$I_{OS(L)}$	Low-level short-circuit output current	V_I = 2 V, V_O = 0, See Note 4 and Figure 1			10	20	35	mA
I_{CC1}	Supply current from V_{CC1}	No load				2.5	4	mA
$I_{CC1(LB)}$	Supply current from V_{CC1} with loopback on	No load,	$\overline{LB}$ at 0.8 V				10	mA
I_{EE}	Supply current from V_{EE}	No load				–2.5	–4	mA
$I_{EE(LB)}$	Supply current from V_{EE} with loopback on	No load,	$\overline{LB}$ at 0.8 V				–10	mA
I_{CC2}	Supply current from V_{CC2}	No load,	V_I = 0,	See Note 6		–10	–100	μA
$I_{CC2(LB)}$	Supply current from V_{CC2} with loopback on	No load, $\overline{LB}$ at 0.8 V, V_I = 0, See Note 6				– 10	– 100	μA
r_o	Output resistance	$V_{CC1} = V_{EE} = V_{CC2}$ = 0, V_O = – 2 V to 2 V,		See Note 5	0.3	5		kΩ

† All typical values are at T_A = 25°C.
‡ The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.
§ This is the most positive level that the driver output will rise to when the device is in the loopback mode and the driver input is at a low level.
¶ The loopback mode should be entered only when the driver output is in the low (marking) state.
# Unused driver inputs should be tied to 0 V or V_{CC2}; unused loopback inputs should be tied to V_{CC2}.

NOTES: 4. Minimum $I_{OS(H)}$ and $I_{OS(L)}$ are specified at V_O = 0 as this more accurately describes the output current needed to dynamically drive capacitive lines. A minimum of ±10 mA is sufficient to drive 2500 pF in parallel with 3 kΩ at a slew rate of 4 V/μs (in accordance with EIA-232-D and V.28).
5. Test conditions are those specified by EIA-232-D.
6. Without a load and V_I = 0, the worst case conditions, V_{CC2} pin sources a small current originating from V_{CC1} giving I_{CC2} supply current a negative sign. When a receiver has an output load, V_{CC2} sinks static and dynamic supply currents to meet load requirements.

driver switching characteristics over full recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3		0.6	5	μs
t_{PHL}	Propagation delay time, high-to-low-level output			0.8	5	μs
t_{skew}	$\lvert t_{PLH} - t_{PHL} \rvert$	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF to 2500 pF		0.2	1	μs
SR	Output slew rate	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF to 2500 pF	4		30	V/μs
$t_{pd(ILB)}$	Propagation delay time going into loopback mode‡	R_L = 3 kΩ to 7 kΩ, See Note 7, See Figure 7		3	50	μs
$t_{pd(OLB)}$	Propagation delay time going out of loopback mode§	R_L = 3 kΩ to 7 kΩ, See Note 7, See Figure 7		3	50	μs
$t_{pd(LB)}$	Propagation delay time in loopback mode¶	R_L = 3 kΩ to 7 kΩ, See Note 7, See Figure 8		3	15	μs
t_{skew}	Skew time in loopback mode	R_L = 3 kΩ to 7 kΩ, See Note 7		4	10	μs

† All typical values are at T_A = 25°C.
‡ This is the delay between entering the loopback mode and when the data on the receiver output becomes valid.
§ This is the worst-case (rising or falling edges) total propagation delay between driver input and receiver output when in the loopback mode.
¶ This is the magnitude of the difference between the propagation delay time of the rising and falling edges of $t_{pd(LB)}$.
NOTE 7: Skew time is the magnitude of the difference between t_{PHL} and t_{PLH} and is measured with a 0 to 3-V input pulse.

RECEIVER SECTION

receiver electrical characteristics over full recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	See Figure 5		1.3	2	2.5	V
V_{T-}	Negative-going threshold voltage	See Figure 5		0.5	1	1.7	V
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)			0.5	1	1.5	V
V_{OH}	High-level output voltage	V_I = –3 V or inputs open,	I_{OH} = –20 μA	3.5			V
		See Note 8 and Figure 5,	I_{OH} = –4 mA	2.4			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 5	V_I = 3 V,			0.4	V
$I_{OS(H)}$	Short-circuit output current at high-level	V_{OH} = 0,	See Figure 4		–20	–60	mA
$I_{OS(L)}$	Short-circuit output current at low-level	V_{OL} = V_{CC2},	See Figure 4		20	60	mA
r_{in}	Input resistance	$\lvert V_I \rvert \le 25$ V		3			kΩ
		$\lvert V_I \rvert$ = 3 V to 25 V				7	

NOTE 8: If the inputs are left unconnected, the receiver interprets this as a low input and the receiver outputs will remain in the high state.

receiver switching characteristics over full recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	See Figure 6			2	6	μs
t_{PHL}	Propagation delay time, high-to-low-level output				2	6	μs
t_{TLH}	Transition time, low-to-high level output‡	C_L = 50 pF,	See Figure 6		200	300	ns
t_{THL}	Transition time, high-to-low level output‡				50	300	ns
t_{skew}	$\lvert t_{PLH} - t_{PHL} \rvert$				0.1	1	μs
t_{wN}	Maximum pulse duration assumed to be noise§	Pulse amplitude = 5 V		1	2	4	μs

† All typical values are at T_A = 25°C.

‡ Transition times are measured between 10% and 90% points on output waveform.

§ The receiver will ignore any positive- or negative-going pulse whose duration is less than the minimum value of t_w and accept any positive- or negative-going pulse whose duration is greater than the maximum value of t_w.

PARAMETER MEASUREMENT INFORMATION

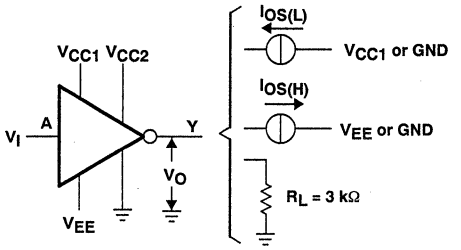


Figure 1. Driver Test Circuit, V_{OH}, V_{OL}, $I_{OS(L)}$, $I_{OS(H)}$

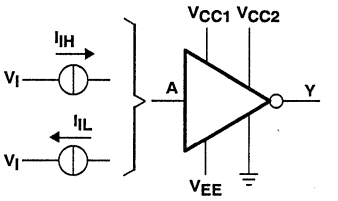
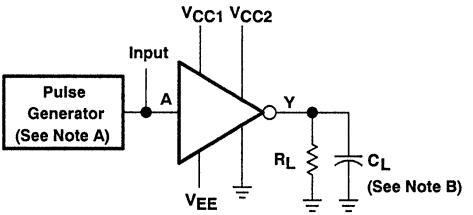
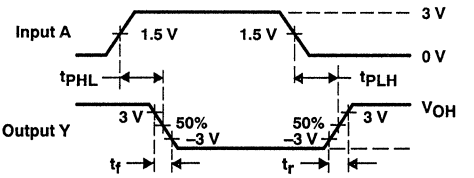


Figure 2. Driver and Loopback Test Circuit, I_{IL}, I_{IH}



DRIVER TEST CIRCUIT



DRIVER VOLTAGE WAVEFORMS
(See Note C)

Figure 3. Driver Propagation Time and Slew Rate

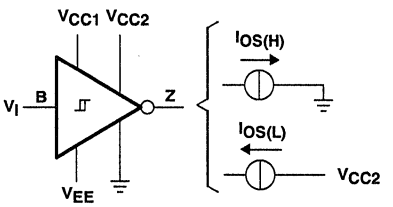


Figure 4. Receiver Test Circuit, $I_{OS(H)}$, $I_{OS(L)}$

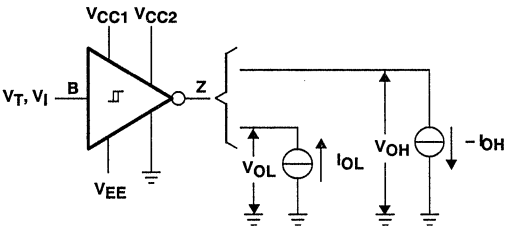


Figure 5. Receiver Test Circuit, V_T, V_{OL}, V_{OH}

NOTES: A. The pulse generator has the following characteristics: t_w = 25 µs, PRR = 20 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. Slew rate $= \frac{6\ V}{t_r \text{ or } t_f}$.

PARAMETER MEASUREMENT INFORMATION

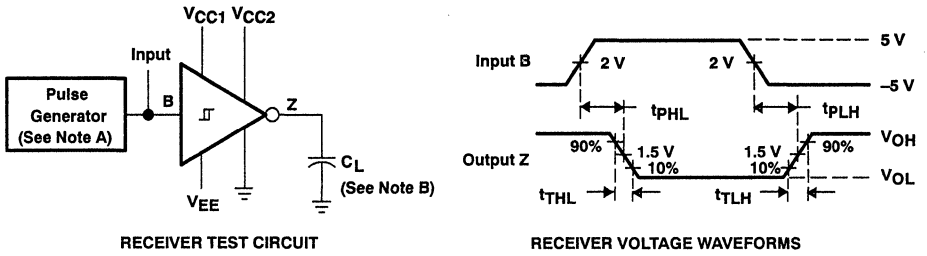


Figure 6. Receiver Propagation and Transition Times

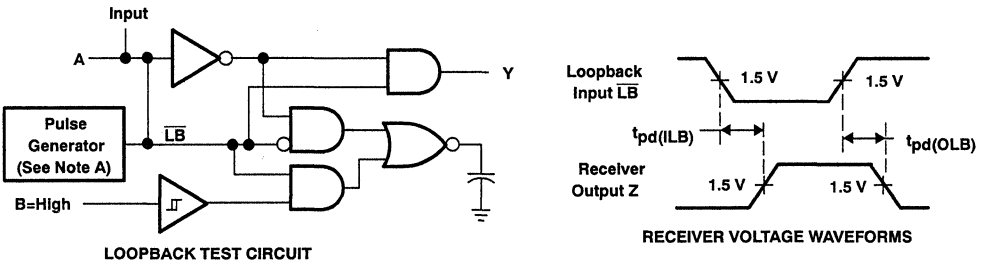


Figure 7. Loopback Entry and Exit Propagation Times

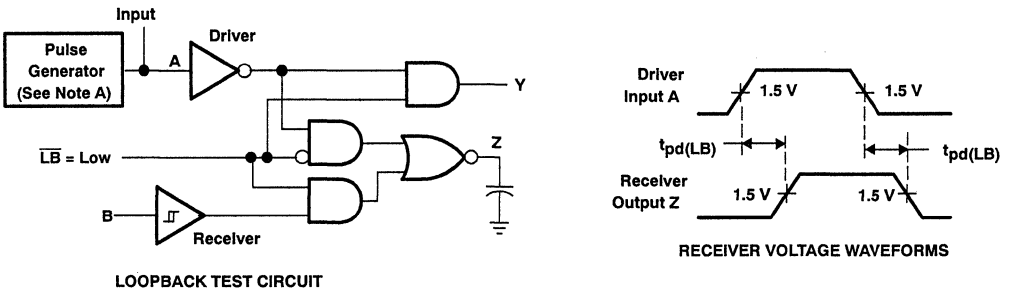


Figure 8. Loop Propagation Times in Loopback Mode

NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PRINCIPLES OF OPERATION

In normal operation, the SN75186 acts as four independent drivers and receivers; the loopback mode is held off by keeping logic inputs $\overline{LB}$ high. Taking a particular $\overline{LB}$ input low activates the loopback mode in the corresponding driver/receiver pair. This causes the output from that driver to be fed back to the input of its receiver through dedicated internal loopback circuitry. Data from the receiver output can then be compared, by a communication system, with the data transmitted to the driver to determine if the functional operation of the driver and receiver together is correct.

In the loopback mode, external data at the input of the receiver is ignored and the driver does not transmit data onto the line. Extraneous data is prevented internally from being sent by the driver in the loopback mode by clamping its output to a level below the maximum interface voltage, – 5 V, ot the EIA-232-D marking state. Below this marking level, a reduced 1.5-V output amplitude is used at the driver output. This signal is detected by an on-chip loopback comparator and fed to the input stage of the receiver to complete the loop.

Line faults external to the SN75186 are detected in addition to device failures. These line faults include short circuits to ground and to external supply voltages that are greater than (V_{EE} + 7 V) and less than V_{EE} typically. For example, with V_{EE} = –12 V, line short circuits to voltages greater than –5 V and less than –12 V will be detected. The loopback mode should be entered only when the driver output is low, that is, the marking condition of EIA-232-D. It is recommended that loopback not be entered when the driver output is in a high state as this may cause a low-level, nondamaging oscillation at the driver output.

When in the loopback mode, approximately 95% of the SN75186 circuit is functionally checked. There exists some low probability of fault mechanisms in circuitry not checked in the loopback mode. To reduce the chances of undetected failure, the unchecked circuitry has been designed to be more robust than that within the loopback test loop. The areas where special attention has been paid are the receiver input potential divider and resistors, the driver output blocking diode (D1), and parts of the driver clamp circuit.

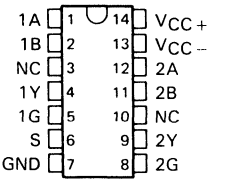
Protection of the SN75186 is achieved by means of driver output current limits and a thermal trip. Although this device will withstand ±30 V at its receiver input, package thermal dissipation limitations have to be taken into consideration if more than one receiver is connected simultaneously. This is due to the possible dissipation in the 3-kΩ minimum input resistors, which is not under the control of the thermal trip. Although the supply current is higher in the loopback mode than in normal operation, the total power dissipation is not sufficient under normal worst-case conditions (of receiver input V_I = 15 V + 10%, receiver output voltage = 2.4 V at 4 mA, driver load of 3 kΩ) to cause the thermal limiting circuitry to trip.

If the SN75186 goes into thermal trip, the output of the driver goes to a high-impedance state and the receiver output is held in a logic-high marking state. Both driver and receiver outputs maintain a marking state for the following circuit and do not allow indeterminate conditions to exist.

The standards specify a minimum driver output resistance to ground of 300 Ω when the device is powered off. To fully comply with EIA-232-D power-off fault conditions, many drivers need diodes in series with each supply voltage to prevent reverse current flow and driver damage. The SN75186 overcomes this need by providing a high-impedance driver output of typically 5 kΩ under power-off conditions through the use of the equivalent of these series diodes in the driver output circuit.

- **Plug-in Replacement for SN75107A and SN75107B with Improved Characteristics**
- **±10 mV Input Sensitivity**
- **TTL Compatible**
- **Standard Supply Voltages . . . ±5 V**
- **Differential Input Common-Mode Voltage Range of ±3 V**
- **Strobe Inputs for Channel Selection**
- **'207 and '207B Have Totem-Pole Outputs**
- **"B" Version Has Diode-Protected Input Stage for Power-Off Condition**
- **Sense Amplifier for MOS Memories**
- **Dual Comparator**
- **High-Sensitivity Line Receiver**

D OR N PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 10$ mV	X	X	H
-10 mV $< V_{ID} <$ 10 mV	X	L	H
	L	X	H
	H	H	Indeterminate
$V_{ID} \leq -10$ mV	X	L	H
	L	X	H
	H	H	L

H = high level, L = low level, X = irrelevant

description

The SN75207 and SN75207B are pin-for-pin replacements for the SN75107A and SN75107B respectively. The improved input sensitivity makes them more suitable for MOS memory sense amplifiers and can result in faster memory cycles. Improved sensitivity also makes them more useful in line receiver applications by allowing use of longer transmission line lengths. The '207 and '207B each features a TTL-compatible active-pull-up output.

The essential difference between the unsuffixed and "B" version can be seen in the schematics. Input-protection diodes are in series with the collectors of the differential-input transistors of the "B" version. These diodes are useful in certain "party-line" systems that may have multiple V_{CC+} power supplies and may be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:

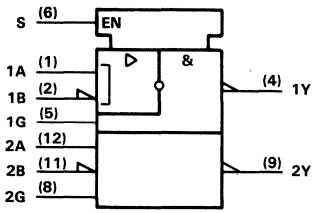
UNSUFFIXED VERSION

"B" VERSION

This would be a problem in specific systems that might possibly have the transmission lines biased to some potential greater than 1.4 V.

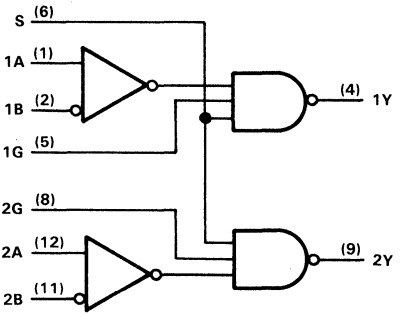
These devices are characterized for operation from 0 °C to 70 °C and are available in plastic small outline (D) package or plastic dual-in-line (N) package.

logic symbol†

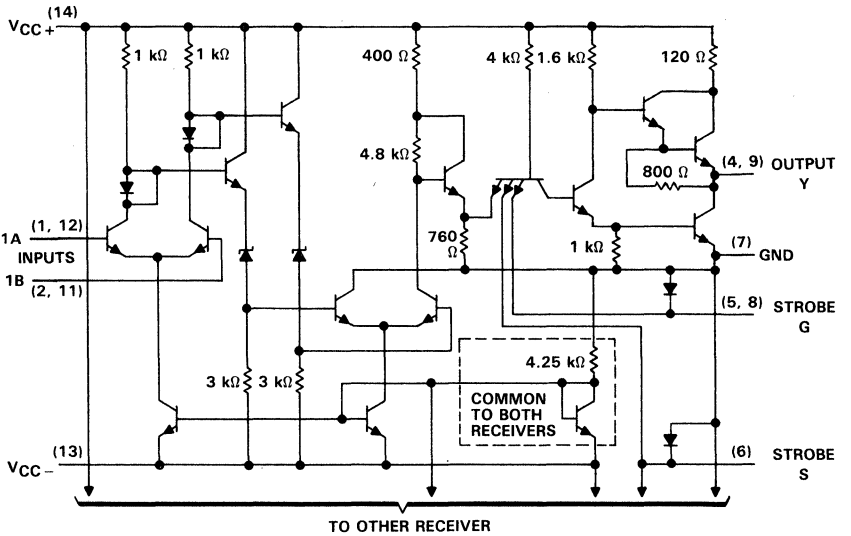


†This symbol is in accordance with ANSI/EEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each receiver)



NOTE: Resistor values shown are nominal.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

design characteristics

The '207 and '207B line receivers/sense amplifiers are TTL-compatible dual circuits intended for use in high-speed data-transmission systems or MOS memory systems. They are designed to detect low-level differential signals in the presence of common-mode noise and variations of temperature and supplies. The dc specifications reflect worst case conditions of temperature, supply voltages, and input voltages.

The input common-mode voltage range is ±3 V. This is adequate for application in most systems. In systems with requirements for greater common-mode voltage range, input attenuators may be used to decrease the noise to an acceptable level at the receiver-input terminals.

The circuits feature individual strobe inputs for each channel and a strobe input common to both channels for logic versatility. The strobe inputs are tested to assure 400 mV of dc noise margin when interfaced with Series 54/74 TTL.

The circuits feature high input impedance and low input currents, which induce very little loading on the transmission line. This makes these devices especially useful in party-line systems. The excellent input sensitivity (3 mV typical) is particularly important when data is to be detected at the end of a long transmission line and the amplitude of the data has deteriorated due to cable losses. The circuits are designed to detect input signals of 10 mV (or greater) amplitude and convert the polarity of the signal into appropriate TTL-compatible output logic levels.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 7 V
Supply voltage, V_{CC-} . . . . . −7 V
Differential input voltage (see Note 2) . . . . . ±6 V
Common-mode input voltage (see Note 3) . . . . . ±5 V
Strobe input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature: (see Note 4)
  D package . . . . . 950 mW
  N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to ground terminal.
2. Differential input voltage values are at the noninverting (A) terminal with respect to the inverting (B) terminal.
3. Common-mode input voltage is the average of the voltages at the A and B inputs.
4. For operation above 25°C free-air temperature, derate linearly to 608 mW at 70°C at the rate of 7.6 mW/°C for the D package and 736 mW at 70°C at the rate of 9.2 mW/°C for the N package.

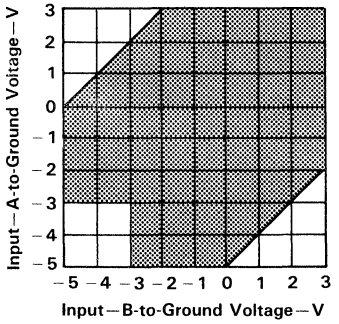
recommended operating conditions (see Note 5)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4.75	5	5.25	V
Supply voltage, V_{CC-}	−4.75	−5	−5.25	V
High-level differential input voltage V_{IDH} (see Note 6)	0.01		5	V
Low-level differential input voltage, V_{IDL}	−5†		−0.01	V
Common-mode input voltage, V_{IC} (see Notes 6 and 7)	−3†		3	V
Input voltage, any differential input to ground (see Note 6)	−5†		3	V
High-level input voltage at strobe inputs, $V_{IH(S)}$	2		5.5	V
Low-level input voltage at strobe inputs, $V_{IL(S)}$	0		0.8	V
Low-level output current, I_{OL}			−16	mA
Operating free-air temperature, T_A	0		70	°C

† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

NOTES: 5. When using only one channel of the line receiver, the strobe G of the unused channel should be grounded and at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 V and 3 V.
6. The recommended combinations of input voltages fall within the shaded area of the figure shown.
7. The common-mode voltage may be as low as −4 V provided that the more positive of the two inputs is not more negative than −3 V.

RECOMMENDED COMBINATIONS
OF INPUT VOLTAGES



electrical characteristics over recommended free-air temperature range (unless otherwise noted)

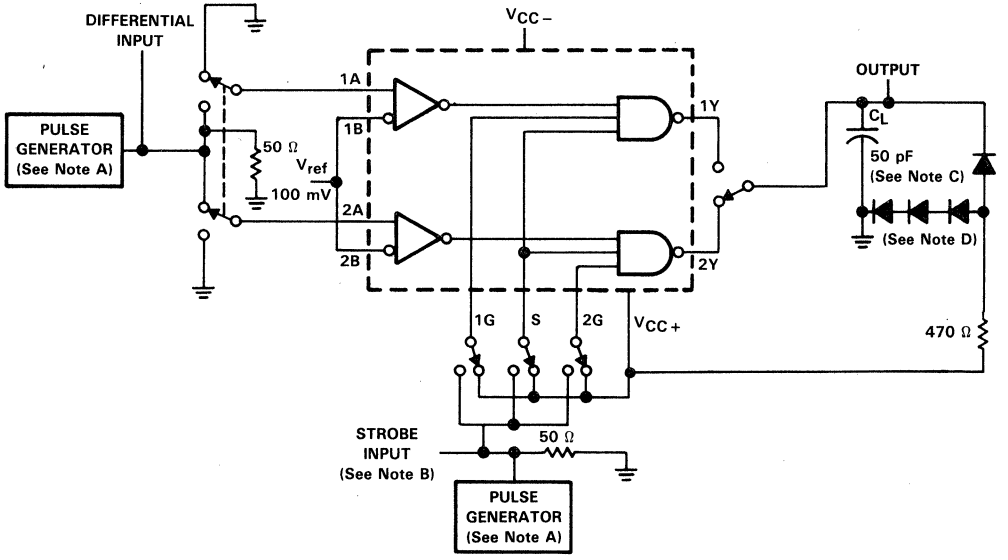
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{IH}	High-level input current	'207	$V_{CC\pm}$ = ±5.25 V	V_{ID} = 5 V		30	75	μA
		'207B		V_{ID} = −5 V		30	75	
I_{IL}	Low-level input current	'207	$V_{CC\pm}$ = ±5.25 V	V_{ID} = −5 V			−10	μA
		'207B		V_{ID} = 5 V			−10	
I_{IH}	High-level input current into 1G or 2G		$V_{CC\pm}$ = ±5.25 V, $V_{IH(S)}$ = 2.4 V				40	μA
			$V_{CC\pm}$ = ±5.25 V, $V_{IH(S)}$ = ±5.25 V				1	mA
I_{IL}	Low-level input current into 1G or 2G		$V_{CC\pm}$ = ±5.25 V, $V_{IL(S)}$ = 0.4 V				−1.6	mA
I_{IH}	High-level input current into S		$V_{CC\pm}$ = ±5.25 V, $V_{IH(S)}$ = 2.4 V				80	μA
			$V_{CC\pm}$ = ±5.25 V, $V_{IH(S)}$ = ±5.25 V				2	mA
I_{IL}	Low-level input current into S		$V_{CC\pm}$ = ±5.25 V, $V_{IL(S)}$ = 0.4 V				−3.2	mA
V_{OH}	High-level output voltage		$V_{CC\pm}$ = ±4.75 V, $V_{IL(S)}$ = 0.8 V, V_{IDH} = 10 mV, I_{OH} = −400 μA, V_{IC} = −3 V to 3 V		2.4			V
V_{OL}	Low-level output voltage		$V_{CC\pm}$ = ±4.75 V, $V_{IH(S)}$ = 2 V, V_{IDL} = −10 mV, I_{OL} = 16 mA, V_{IC} = −3 V to 3 V				0.4	V
I_{OH}	High-level output current		$V_{CC\pm}$ = ±4.75 V, V_{OH} = ±5.25 V					μA
I_{OS}	Short-circuit output current‡		$V_{CC\pm}$ = ±5.25 V		−18		−70	mA
I_{CCH+}	Supply current from V_{CC+}, outputs high		$V_{CC\pm}$ = ±5.25 V, T_A = 25°C			18	30	mA
I_{CCH-}	Supply current from V_{CC-}, outputs high		$V_{CC\pm}$ = ±5.25 V, T_A = 25°C			−8.4	−15	mA

†All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time.

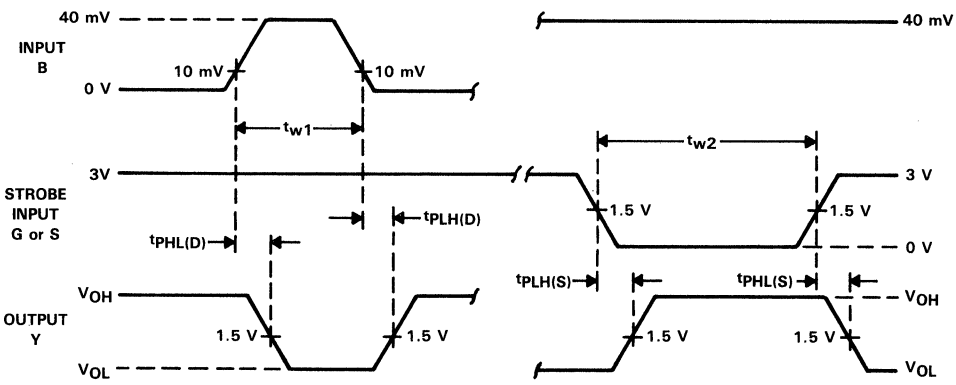
switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low-to-high-level output, from differential inputs A and B	R_L = 470 Ω, C_L = 50 pF, See Figure 1		35	ns
$t_{PHL(D)}$	Propagation delay time, high-to-low-level output, from differential inputs A and B			20	ns
$t_{PLH(S)}$	Propagation delay time, low-to-high-level output, from strobe input G or S			17	ns
$t_{PHL(S)}$	Propagation delay time, high-to-low-level output, from strobe input G or S			17	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r \leq 5$ ns, $t_f \leq 5$ ns, t_{w1} = 500 ns with PRR = 1 MHz, t_{w2} = 1 μs with PRR = 500 kHz.
B. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916.

FIGURE 1. PROPAGATION DELAY TIMES

TEXAS INSTRUMENTS
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TYPICAL APPLICATION DATA

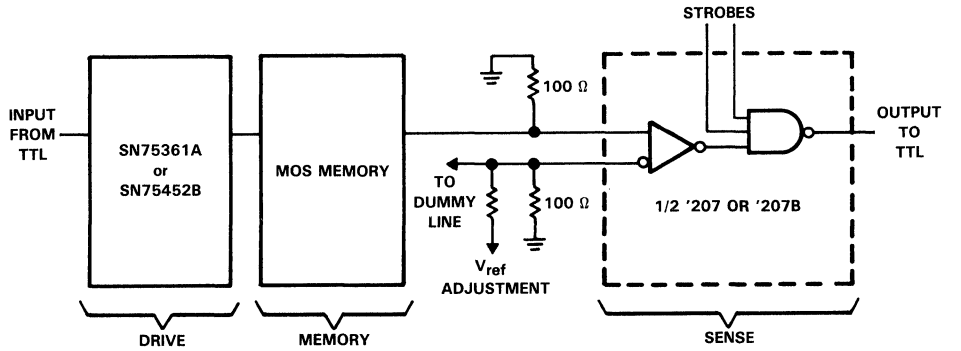
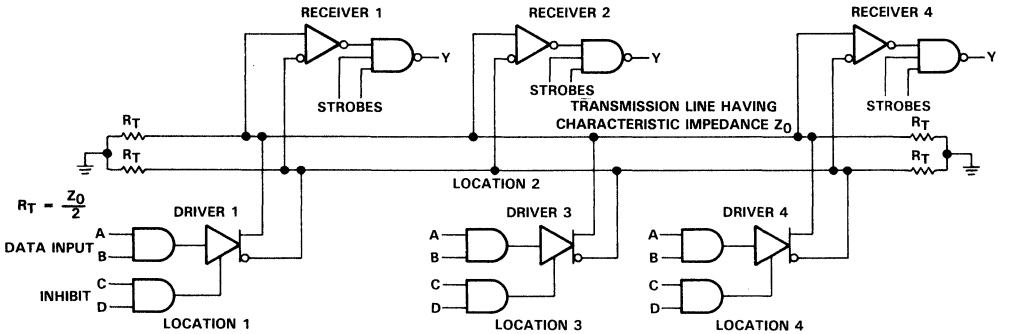


FIGURE 2. MOS MEMORY SENSE AMPLIFIER



Receivers are '207 or '207B; drivers are SN55109A, SN75109A, SN55110A, SN75110A, or SN75112.

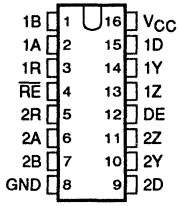
FIGURE 3. DATA-BUS OR PARTY-LINE SYSTEM

PRECAUTIONS: When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 V and 3 V, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers. Strobe G of the unused channel should be grounded.

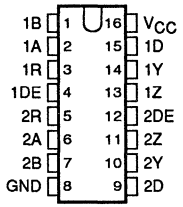
D3381, MARCH 1990

- **Meets EIA Standards RS-422-A, RS485**
- **Meets CCITT Recommendations V.10, V.11, X.26, X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **Driver Common-Mode Output Voltage Range of −7 V to 12 V**
- **Driver Positive- and Negative-Current Limiting**
- **Thermal Shutdown Protection**
- **Driver 3-State Outputs Active-High Enable**
- **Receiver Common-Mode Input Voltage Range of −12 V to 12 V**
- **Receiver Input Sensitivity ... ±200 mV**
- **Receiver Hysteresis ... 50 mV Typ**
- **Receiver High-Input-Impedance ... 12 kΩ Min**
- **Receiver 3-State Outputs Active-Low Enable for SN751177 Only**
- **Operates from Single 5-V Supply**

SN751177
N PACKAGE
(TOP VIEW)



SN751178
N PACKAGE
(TOP VIEW)



description

The SN751177 and SN751178 dual differential drivers and receivers are monolithic integrated circuits that are designed for balanced multipoint bus transmission at rates up to 10 M bits per second. They are designed to improve the performance of full-duplex data communications over long bus lines and meet EIA standards RS-422-A, RS-485 and several CCITT recommendations.

The SN751177 and SN751178 driver outputs provide limiting for both positive and negative currents and thermal shutdown protection from line fault conditions on the transmission bus line.

The receiver features high input impedance of 12 kΩ, an input sensitivity of ±200 mV over a common-mode input voltage range of −12 V to 12 V and typical input hysteresis of 50 mV. Fail-safe design ensures that if the receiver inputs are open, the receiver outputs will always be high.

The SN751177 and SN751178 are characterized for operation from −20°C to 85°C.

SN751177, SN751178
FUNCTION TABLE OF EACH DRIVER

INPUT	ENABLE	OUTPUT	
D	DE	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

SN751177
FUNCTION TABLE OF EACH RECEIVER

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A − B	$\overline{RE}$	R
$V_{ID} \geq 0.2$ V	L	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

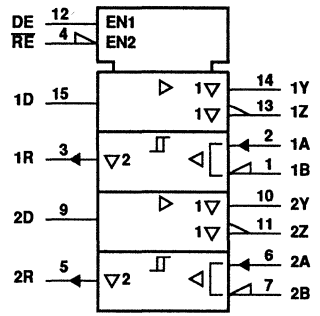
SN751178
FUNCTION TABLE OF EACH RECEIVER

DIFFERENTIAL INPUTS	OUTPUT
A − B	R
$V_{ID} \geq 0.2$ V	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	?
$V_{ID} \leq -0.2$ V	L

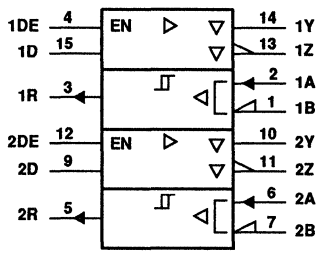
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbols†

SN751177



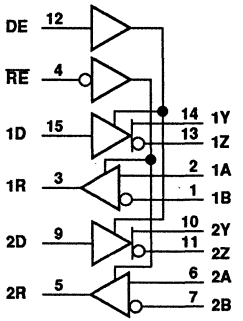
SN751178



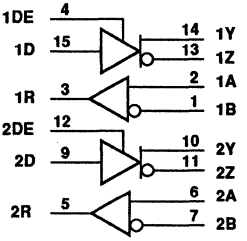
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

logic diagrams (positive logic)

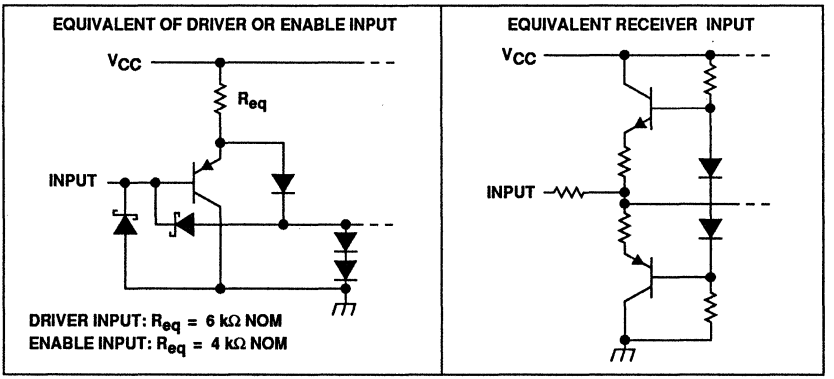
SN751177



SN751178

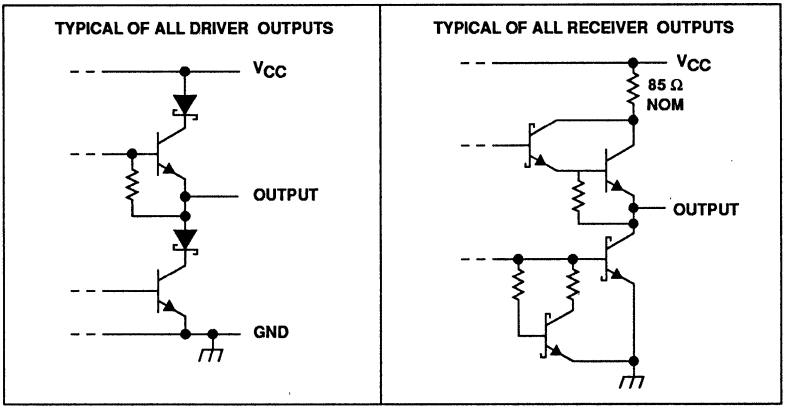


schematics of inputs



All resistor values are nominal.

schematics of outputs



All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, DE, $\overline{RE}$, and D inputs . . . . . 7 V
Input voltage range, receiver A or B inputs . . . . . −25 V to 25 V
Receiver differential input voltage range (see Note 2) . . . . . −25 V to 25 V
Output voltage range,Driver . . . . . −10 V to 15 V
Receiver low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 1150 mW
Operating free-air temperature range, T_A . . . . . −20°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values,except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.
3. For operation above 25°C free-air temperature, derate to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	DE, $\overline{RE}$, and D inputs	2			V
Low-level input voltage, V_{IL}				0.8	V
Common-mode output voltage, V_{OC} (see Note 4)	Driver	−7		12	V
High-level output current, I_{OH}				−60	mA
Low-level output current, I_{OL}				60	mA
Common-mode input voltage, V_{IC}	Receiver			±12	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}				−400	μA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A		−20		85	°C

NOTE 4: The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

DRIVER SECTIONS

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −33 mA			3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = 33 mA			1.1		V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1		2			V
				1/2 V_{OD1}			
		R_L = 54 Ω, See Figure 1		1.5		5	
V_{OD3}	Differential output voltage	See Note 5		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage (see Note 6)	R_L = 54 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage (see Note 4)			−1		3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage (see Note 6)					±0.2	V
I_O	Output current with power off	V_{CC} = 0, V_O = −7 V to 12 V				±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level input current	V_{IL} = 0.4 V				−100	mA
I_{OS}	Short-circuit output current (see Note 7)	V_O = −7 V				−250	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current	No load	outputs enabled		80	110	μA
			outputs disabled		50	80	

†All typical values are at V_{CC} = 5 V and T_A = 25°C

NOTES: 4. The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.
5. See EIA Standard RS-485 Figure 3.5, Test Termination Measurement 2.
6. $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
7. Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

driver switching characteristics at V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DD}	Differential output delay time	R_L = 54 Ω, C_L = 50 pF, See Figure 3		20	25	ns
t_{TD}	Differential output transition time			27	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 27 Ω, C_L = 50 pF, See Figure 4		20	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			20	25	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, C_L = 50 pF, See Figure 5		80	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, C_L = 50 pF, See Figure 6		40	60	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, C_L = 50 pF, See Figure 5		90	120	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, C_L = 50 pF, See Figure 6		30	45	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422A	RS-485
$\|V_{OD1}\|$	V_O	V_O
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test termination measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{OS}\|$	$\|V_{OS}\|$
$\Delta\|V_{OC}\|$	$\|V_{OS} - \overline{V}_{OS}\|$	$\|V_{OS} - \overline{V}_{OS}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTIONS

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential input high threshold voltage		V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential input low threshold voltage (see Note 4)		V_O = 0.5 V,	I_O = 16 mA	−0.2			V
V_{hys}	Input hysteresis (see Note 8)					50		mV
V_{IK}	Enable clamp voltage	SN751177	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = −400 μA	2.7			V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV	I_{OL} = 8 mA			0.45	V
				I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	SN751177	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current (see Note 9)		Other input at 0 V	V_I = 12 V			1	mA
				V_I = −7 V			−0.8	
I_{IH}	High-level enable input current	SN751177	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable input current	SN751177	V_{IL} = 0.4 V				−100	μA
I_{OS}	Short-circuit output current (see Note 7)				−15		−85	mA
I_{CC}	Supply current		No load,	outputs enabled		80	110	mA
r_i	Input resistance				12			kΩ

†All typical values are at V_{CC} = 5 V and T_A = 25°C

NOTES: 4. The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

7. Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
8. Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.
9. Refer to EIA standards RS-422-A, RS-423-A, RS-485-A for exact conditions.

receiver switching characteristics at V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		V_{ID} = −1.5 V to 1.5 V,			20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output		C_L = 15 pF,	See Figure 7		22	35	ns
t_{PZH}	Output enable time to high level	SN751177	C_L = 15 pF,	See Figure 8		17	25	ns
t_{PZL}	Output enable time to low level					20	27	ns
t_{PHZ}	Output disable time from high level					25	40	ns
t_{PLZ}	Output disable time from low level					30	40	ns

PARAMETER MEASUREMENT INFORMATION

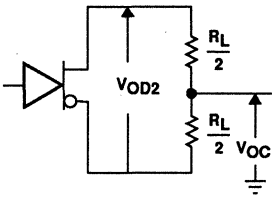


FIGURE 1. DRIVER TEST CIRCUIT, V_{OD} AND V_{OC}

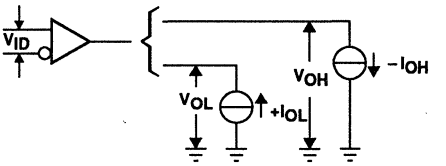
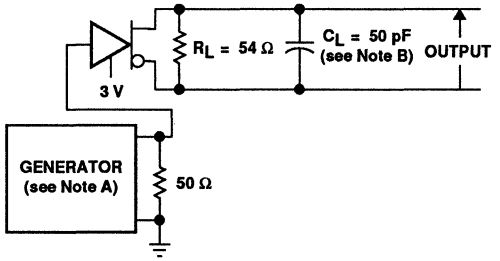
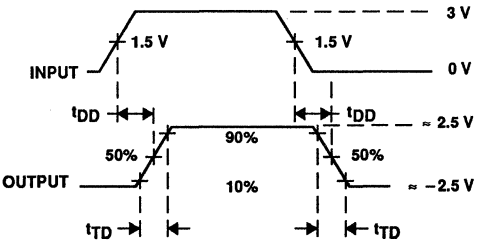


FIGURE 2. RECEIVER TEST CIRCUIT, V_{OH} AND V_{OL}

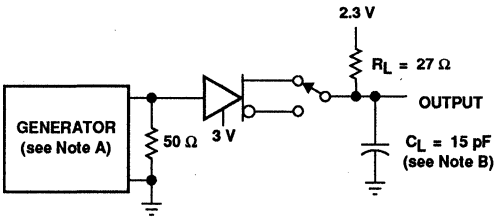


(a) DRIVER TEST CIRCUIT

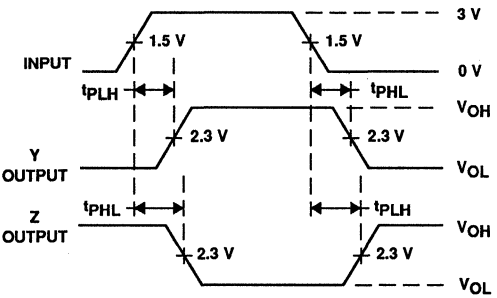


(b) DRIVER VOLTAGE WAVEFORMS

FIGURE 3. DRIVER DIFFERENTIAL OUTPUT DELAY AND TRANSITION TIMES



(a) DRIVER TEST CIRCUIT

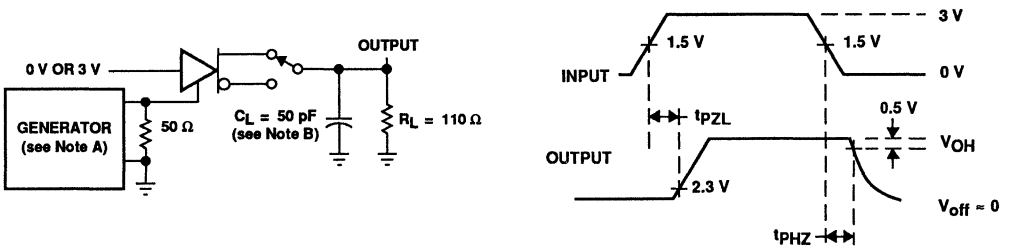


(b) DRIVER VOLTAGE WAVEFORMS

FIGURE 4. DRIVER PROPAGATION DELAY TIMES

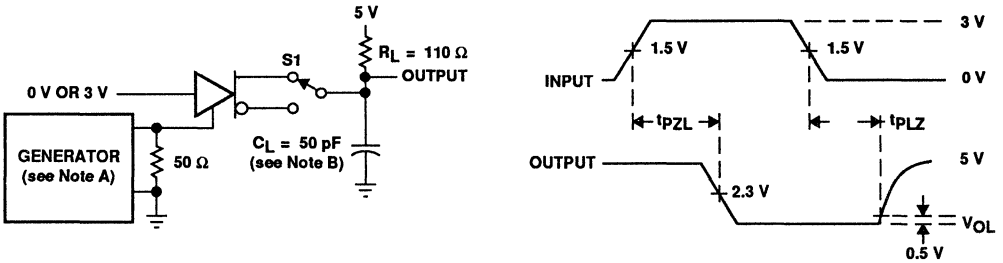
NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns..
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



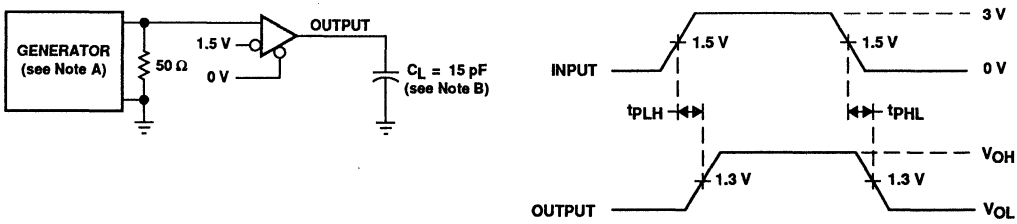
(a) DRIVER TEST CIRCUIT (b) DRIVER VOLTAGE WAVEFORMS

FIGURE 5. DRIVER ENABLE AND DISABLE TIMES



(a) DRIVER TEST CIRCUIT (b) DRIVER VOLTAGE WAVEFORMS

FIGURE 6. DRIVER ENABLE AND DISABLE TIMES

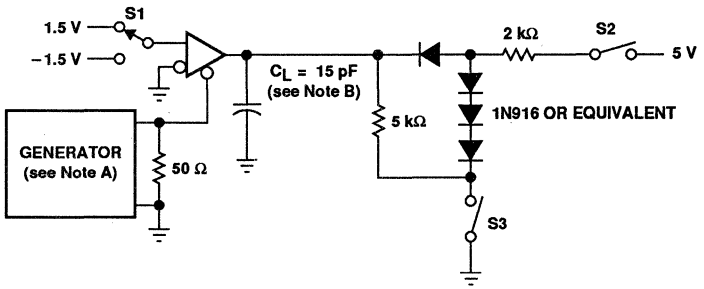


(a) RECEIVER TEST CIRCUIT (b) RECEIVER VOLTAGE WAVEFORMS

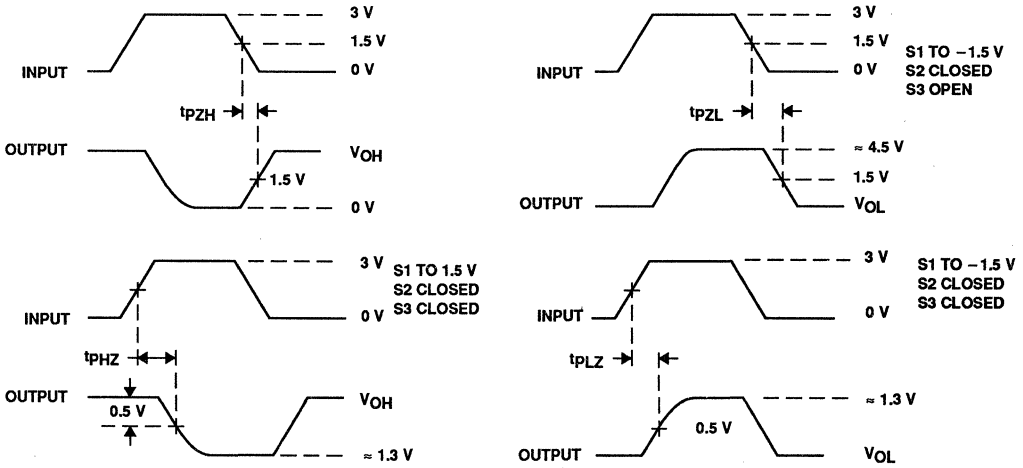
FIGURE 7. RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns..
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



(a) RECEIVER TEST CIRCUIT



(b) RECEIVER VOLTAGE WAVEFORMS

FIGURE 8. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns..
B. C_L includes probe and jig capacitance.

D3494, MAY 1990

- **Meets IBM 360/370 Input/Output Interface Specification for 4.5 Mb/s Operation**
- **Single 5-V Supply**
- **Uncommitted Emitter-Follower Output Structure for Party-Line Operation**
- **Driver Output Short-Circuit Protection**
- **Driver Input/Receiver Output Compatible with TTL**
- **Receiver Input Resistance . . . 7.4 kΩ to 20 kΩ**
- **Ratio Specification for Propagation Delay Time, Low-to-High/High-to-Low**

description

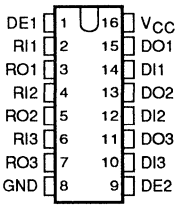
The SN751730 triple line driver/receiver is specifically designed to meet the input/output interface specifications for IBM System 360/370. It is also compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower driver outputs of the SN751730 will drive terminated lines such as coaxial cable or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 2.5 V.

An open line will affect the receiver input as would a low-level input voltage.

All the driver inputs and receiver outputs are in conventional TTL configuration and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line, by pulling either DE1 or DE2 to a low level.

D OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE OF EACH DRIVER

INPUTS			OUTPUT
DI	DE1	DE2	DO
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

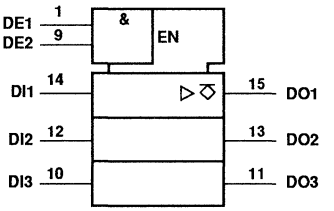
FUNCTION TABLE OF EACH RECEIVER

INPUT	OUTPUT
RI	RO
L	H
H	L
OPEN	H

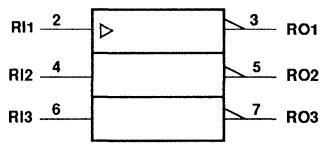
H = high level, L = low level,
X = irrelevant

logic symbols†

DRIVER



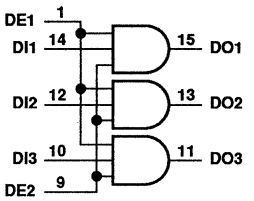
RECEIVER



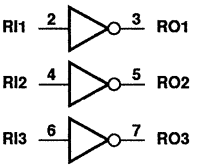
†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

DRIVER

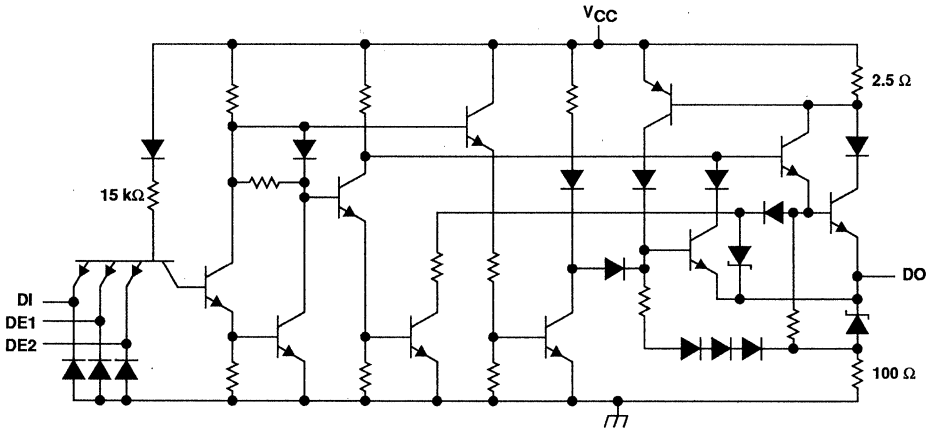


RECEIVER

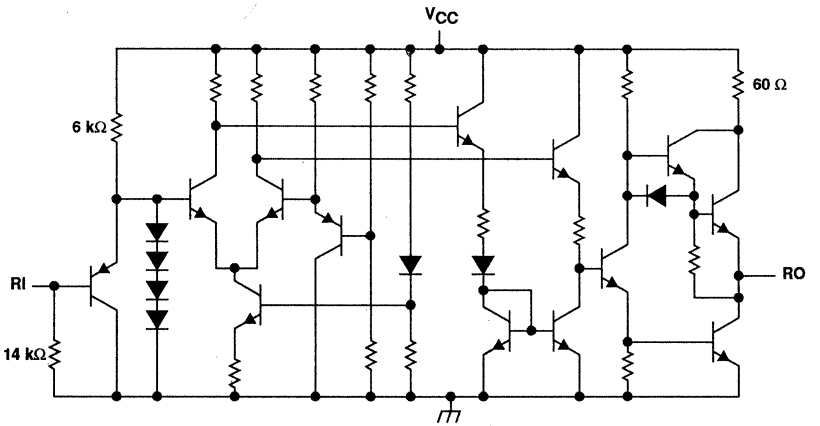


equivalent schematics of driver and receiver

DRIVER



RECEIVER



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage range, V_I: Driver . . . . . −0.5 V to 7 V
Receiver . . . . . −0.5 V to 7 V
Output voltage range, V_O Driver . . . . . −0.5 V to 7 V
Enable input voltage range . . . . . −0.5 V to 7 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	Driver, Enable	2			V
	Receiver	1.55			
Low-level input voltage, V_{IL}	Driver, Enable			0.8	V
	Receiver			1.15	
Operating free-air temperature, T_A		0		70	°C

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V,	I_{IL} = −18 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = 4.75 V, I_{OH} = 59.3 mA,	V_{IH} = 2 V, T_A = 25°C	3.11			V
			V_{CC} = 5.25 V, I_{OH} = 78.1 mA	V_{IH} = 2 V,			4.10	
			V_{CC} = 4.75 V, R_L = 51.4 Ω	V_{IH} = 2 V,	3.05			
			V_{CC} = 5.25 V, R_L = 56.9 Ω	V_{IH} = 2 V,			4.20	
V_{ODH}	Differential high-level output voltage		R_L = 46.3 Ω or 56.9 Ω				0.50	V
V_{OL}	Low-level output voltage		V_{CC} = 5.25 V, V_{IL} = 0.8 V, V_{IH} = 4.5 V	I_{OL} = −0.24 mA			0.15	V
				R_L = 56.9 Ω			0.5	
I_{IH}	High-level input current	DI	V_{CC} = 5.25 V,	V_{IH} = 2.7 V			20	μA
		DE					60	
I_{IL}	Low-level input current	DI	V_{CC} = 5.25 V,	V_{IL} = 0.4 V			−400	μA
		DE					−1200	
I_{OH}	High-level output current		V_{CC} = 4.75 V, V_{OH} = 5 V	V_{IL} = 0			100	μA
				V_{IH} = 4.5 V			100	
I_{OS}	Short-circuit output current		V_{CC} = 5.25 V,	V_{IH} = 4.5 V	−30			mA
I_{CCH}	Supply current (total package)		V_{CC} = 5.25 V, No load	$V_{I(D)}$ = 4.5 V, $V_{I(R)}$ = 0			47	mA
I_{CCL}				$V_{I(D)}$ = 0, $V_{I(R)}$ = 4.5 V			80	

driver switching characteristics, V_{CC} = 5 V ±5%, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low to high level output	R_L = 47.5 Ω,	See Figure 1	6.5	12	18.5	ns
t_{PHL}	Propagation delay time, high to low level output			6.5	12	18.5	ns
Δt_{PD}	Differential propagation delay time†					10	ns
t_r	Output rise time	V_{CC} = 5 V, R_L = 47.5 Ω, See Figure 1	V_O = 0.15 to 3.05 V, C_L = 10.2 pF,	5	10		ns
t_f	Output fall time			5	13		ns
SR	Slew rate	V_O = 1 to 3 V average, R_L = 47.5 Ω, C_L = 10.2 pF,	See Figure 1			0.65	V/ns

†$\Delta t_{PD} = |t_{PLH} - t_{PHL}|$

receiver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, I_{OH} = −400 µA	V_I = 1.15 V,	2.7			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 1.55 V	I_{OL} = 8 mA			0.5	V
			I_{OL} = 4 mA			0.4	
r_i	Input resistance	V_{CC} = 0,	V_I = 0.15 to 3.9 V	7.4		20	kΩ
I_{IH}	High-level input current	V_{CC} = 4.75 V,	V_{IH} = 3.11 V			0.42	mA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_{IL} = 0.15 V	−0.24		0.04	mA
I_{OS}	Short-circuit output current, See Note 2	V_{CC} = 5.25 V,	V_{IL} = 0	−20		−100	mA
I_{CCH}	Supply current (total package)	V_{CC} = 5.25 V, No load	$V_{I(D)}$ = 4.5 V, $V_{I(R)}$ = 0			47	mA
I_{CCL}			$V_{I(D)}$ = 0, $V_{I(R)}$ = 4.5 V			80	

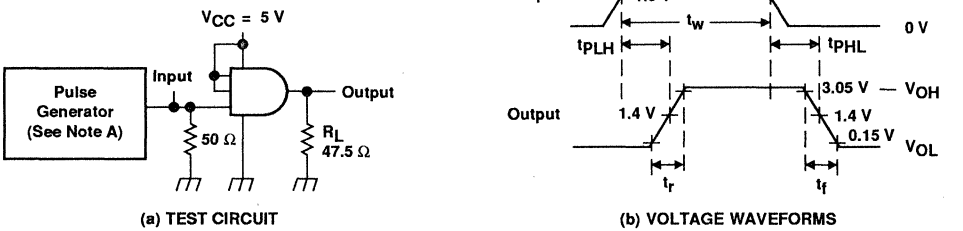
NOTE 2: Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

receiver switching characteristics, V_{CC} = 5 V ±5%, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low to high level output	R_L = 2 kΩ, See Figure 2	C_L = 15 pF	7.5	12	19.5	ns
t_{PHL}	Propagation delay time, high to low level output			7.5	12	19.5	ns
Δt_{PD}	Differential propagation delay time†					10	ns

†$\Delta t_{PD} = |t_{PLH} - t_{PHL}|$

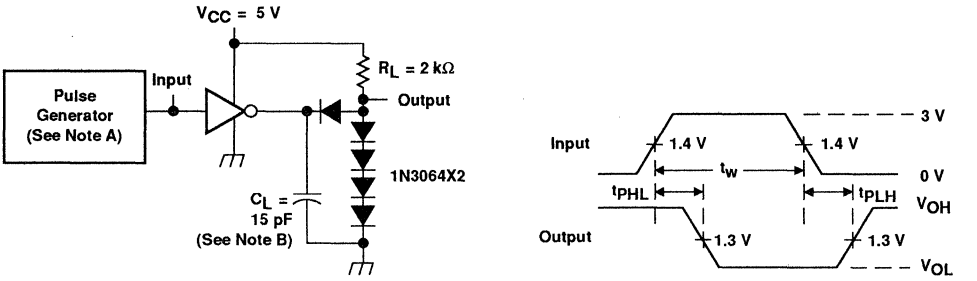
PARAMETER MEASUREMENT INFORMATION



(a) TEST CIRCUIT (b) VOLTAGE WAVEFORMS

NOTE A: The pulse generator has the following characteristics: $z_o \approx 50\ \Omega$, $t_w \leq 500$ ns, PRR ≤ 1 MHz, $t_f \leq 6$ ns, $t_r \leq 15$ ns

Figure 1. Driver Switching Times



(a) TEST CIRCUIT (b) VOLTAGE WAVEFORMS

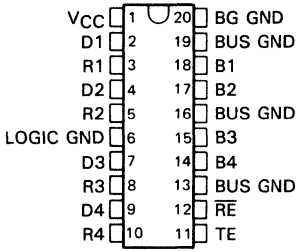
NOTES: A. The pulse generator has the following characteristics: $z_o \approx 50\ \Omega$, $t_w \leq 500$ ns, PRR ≤ 1 MHz, $t_f \leq 10$ ns, $t_r \leq 10$ ns.
B. C_L includes probe and jig capacitance.

Figure 2. Receiver Switching Times

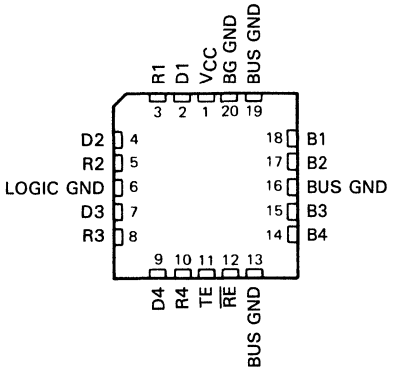
D3077, JANUARY 1988—REVISED SEPTEMBER 1989

- **High-Speed Quad Transceiver**
- **Fully Compatible with IEEE Std 896.1—1987 Futurebus Requirements**
- **Drives Load Impedances as Low as 10 Ω**
- **High-Speed Advanced Low-Power Schottky Circuits**
- **Low Power Dissipation . . . 81 mW Max per Channel**
- **High-Impedance P-N-P Inputs**
- **BTL™ Logic Level 1-V Bus Swing Reduces Power Consumption**
- **Low Bus-Port Capacitance**
- **Power-Up/Power-Down Protection (Glitch-Free)**
- **Open-Collector Driver Outputs Allows Wired-OR Connections**
- **Multiple Bus Channel Ground Returns to Reduce Channel Noise Interference**
- **Designed to Be a Faster, Lower Power Functional Equivalent of National DS3893**

N PACKAGE
(TOP VIEW)



FN CHIP CARRIER PACKAGE
(TOP VIEW)



description

The SN75ALS053 is a four-channel, monolithic, high-speed, advanced low-power Schottky device designed for two-way data communication in a densely populated backplane. The SN75ALS053 has independent driver input (Dn) and receiver output (Rn) pins and separate driver and receiver disables. This transceiver is designed for use in high-speed bus systems and is similar to the SN75ALS057 transceiver except that the trapezoidal feature has been eliminated to speed up the propagation delays.

These transceivers feature open-collector driver outputs, each with a series Schottky diode to reduce capacitive loading to the bus. By using a 2-V pullup on the bus, the output signal swing will be approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs are capable of driving an equivalent dc load of as low as 10 Ω.

The receivers have a precision threshold set by an internal bandgap reference to give accurate input thresholds over V_{CC} and temperature variations.

These transceivers are compatible with Backplane Transceiver Logic (BTL™) technology at significantly reduced power dissipation per channel.

The SN75ALS053 is characterized for operation from 0°C to 70°C.

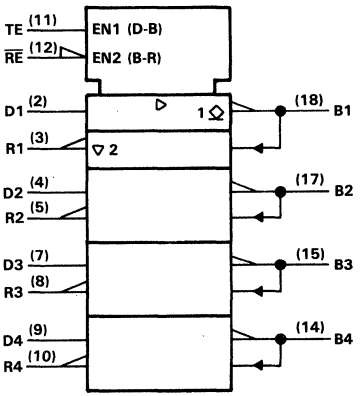
BTL is a trademark of National Semiconductor Corporation.

FUNCTION TABLE
TRANSMIT/RECEIVE

CONTROLS		CHANNELS	
TE	$\overline{RE}$	D → B	B → R
L	L	D	R
L	H	D	D
H	L	T	R
H	H	T	D

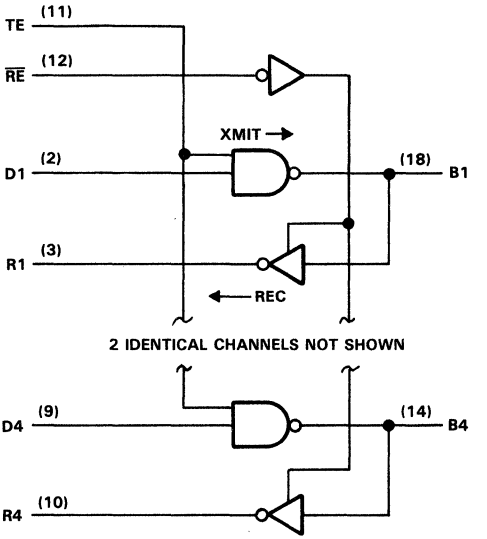
H = high level, L = low level, R = receive, T = transmit, D = disable
Direction of data transmission is from Dn to Bn, direction of data reception is from Bn to Rn.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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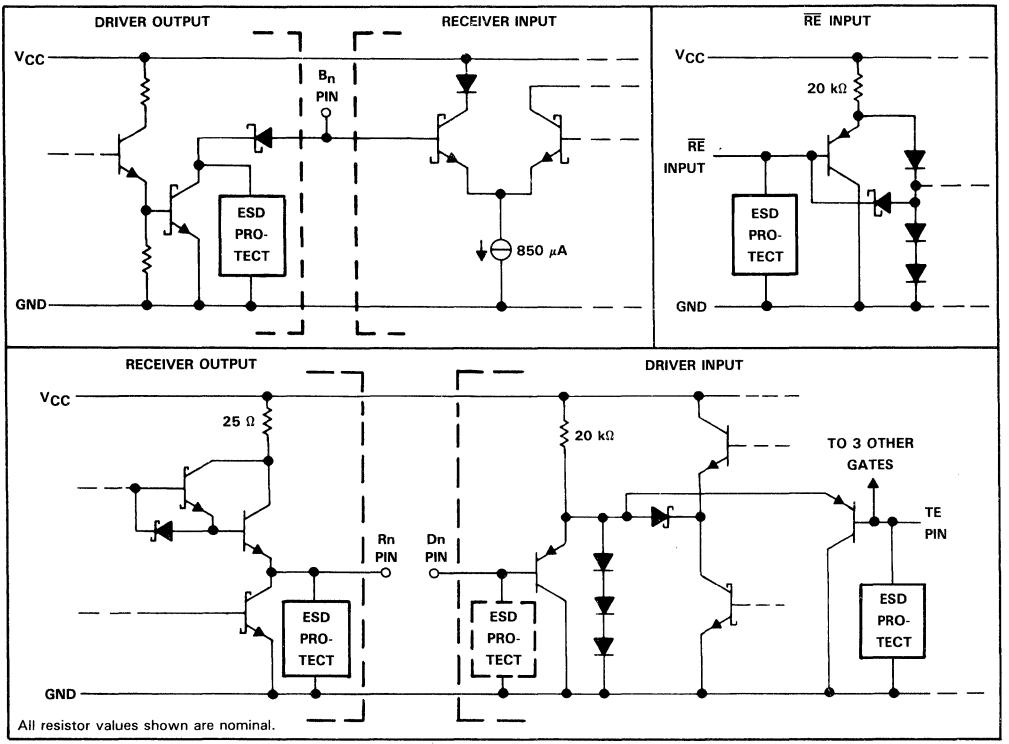
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	6 V
Control input voltage	5.5 V
Driver input voltage	5.5 V
Driver output voltage	2.5 V
Receiver input voltage	2.5 V
Receiver output voltage	5.5 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: N package	260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
FN	1400 mW	11.2 mW/°C	896 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level driver and control input voltage, V_{IH}	2			V
Low-level driver and control input voltage, V_{IL}			0.8	V
Bus termination voltage	1.9		2.1	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage at Dn, DE, or $\overline{RE}$		$I_I = -18$ mA			−1.5	V
V_T	Receiver input threshold at Bn			1.426		1.674	V
V_{OH}	High-level output voltage at Rn		Bn at 1.2 V, $\overline{RE}$ at 0.8 V, $I_{OH} = -1$ mA	2.5			V
V_{OL}	Low-level output voltage	Rn	Bn at 2 V, $\overline{RE}$ at 0.8 V, $I_{OL} = 20$ mA			0.5	V
		Bn	Dn at 2.4 V, TE at 2.4 V, $V_L = 2$ V, $R_L = 10\ \Omega$, See Figure 1	0.75		1.2	
I_{IH}	High-level input current	Dn, TE or $\overline{RE}$	$V_I = V_{CC}$			40	μA
		Bn	$V_I = 2$ V, $V_{CC} = 0$ or 5.25 V, Dn at 0.8 V, TE at 0.8 V,			100	
I_{IL}	Low-level input current at Dn, TE or $\overline{RE}$		$V_I = 0.4$ V			−400	μA
I_{OS}	Short-circuit output current at Rn		Rn at 0 V, Bn at 1.2 V, $\overline{RE}$ at 0.8 V	−70		−200	mA
I_{CC}	Supply current					65	mA
$C_{o(B)}$	Driver output capacitance		$V_{CC} = 5$ V, $T_A = 25°C$		6.5		pF

switching characteristics over recommended ranges of operating free-air temperature and V_{CC} (unless otherwise noted)

driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Dn	Bn	TE at 3 V, V_L = 2 V, See Figure 2	2	7	ns
t_{PHL}	Propagation delay time high-to-low-level output				2	7	
t_{PLH}	Propagation delay time, low-to-high-level output	Dn	Bn	Dn at 3 V, V_L = 2 V, See Figure 2	2	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output				2	7	
t_{TLH}	Transition time, low-to-high-level output	Dn	Bn	TE at 3 V, V_L = 2 V, See Figure 2	0.5	5	ns
t_{THL}	Transition time, high-to-low-level output				0.5	5	
	Skew between driver channels†	Dn	Bn	TE at 3 V, V_L = 2 V		1	ns

receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Bn	Rn	$\overline{RE}$ at 0.3 V, TE at 0.3 V, See Figure 3	2	8	ns
t_{PHL}	Propagation delay time, high-to-low-level output				2	8	
t_{PLZ}	Output disable time from low level	$\overline{RE}$	Rn	Bn at 2 V, TE at 0.3 V, V_L = 5 V, C_L = 5 pF, R_{L1} = 500 Ω, See Figure 4		6	ns
t_{PZL}	Output enable time to low level	$\overline{RE}$	Rn	Bn at 2 V, TE at 0.3 V, V_L = 5 V, C_L = 5 pF, R_{L1} = 500 Ω, See Figure 4		12	ns
t_{PHZ}	Output disable time from high level	$\overline{RE}$	Rn	Bn at 1 V, TE at 0.3 V, V_L = 0, C_L = 5 pF, R_{L1} = 500 Ω, See Figure 4		6	ns
t_{PZH}	Output enable time to high level	$\overline{RE}$	Rn	Bn at 1 V, TE at 0.3 V, V_L = 0, C_L = 5 pF, R_{L1} = 500 Ω, See Figure 4		12	ns
	Skew between receiver channels†	Bn	Rn	$\overline{RE}$ at 0.3 V, TE at 0.3 V		1	ns

†Skew is the difference between the propagation delay time (t_{PLH} or t_{PHL}) of one receiver channel and that same propagation delay time of any other receiver channel. It applies for both t_{PLH} and t_{PHL}.

PARAMETER MEASUREMENT INFORMATION

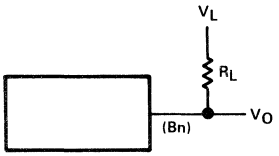
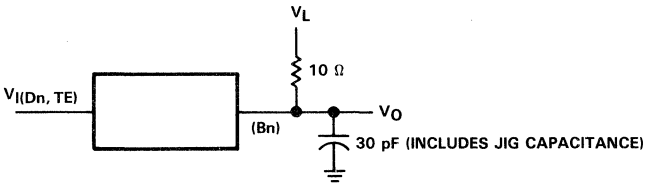
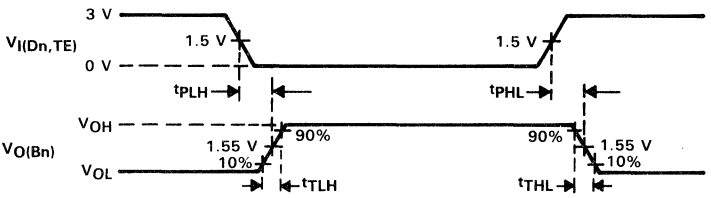


FIGURE 1. DRIVER LOW-LEVEL-OUTPUT-VOLTAGE TEST CIRCUIT



TEST CIRCUIT

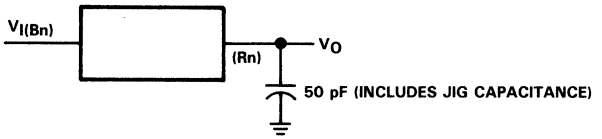


VOLTAGE WAVEFORMS

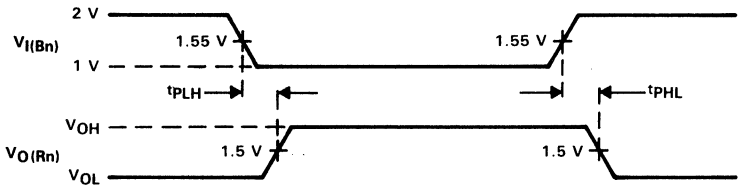
NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 2. DRIVER PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



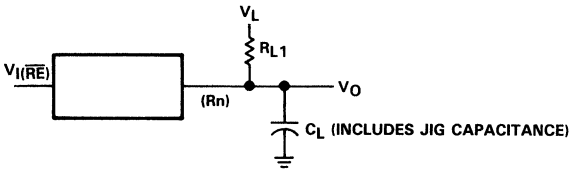
TEST CIRCUIT



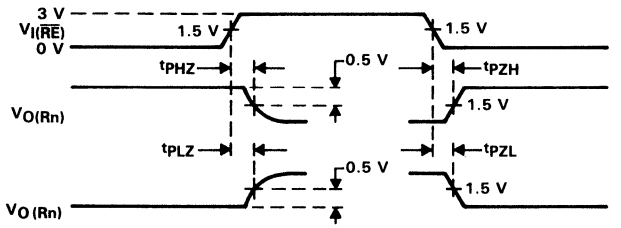
VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \leq 10$ ns from 10% to 90%

FIGURE 3. RECEIVER PROPAGATION DELAY TIMES



TEST CIRCUIT



VOLTAGE WAVEVORMS

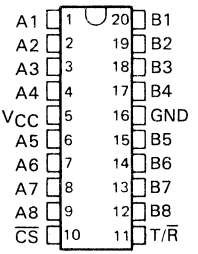
NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 4. PROPAGATION DELAY FROM $\overline{RE}$ TO Rn

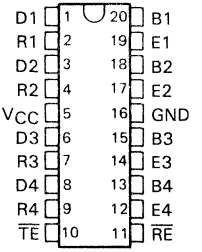
D3025, AUGUST 1987—REVISED JUNE 1990

- **SN75ALS056 Is an Octal Transceiver**
- **SN75ALS057 Is a Quad Transceiver**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Low Power Dissipation . . . 52.5 mW/Channel Max**
- **High-Impedance P-N-P Inputs**
- **Logic Level 1-V Bus Swing Reduces Power Consumption**
- **Trapezoidal Bus Output Waveform Reduces Noise Coupling to Adjacent Lines**
- **Power-Up/Down Protection (Glitch Free)**
- **Open-Collector Driver Outputs Allow Wired-OR Connections**
- **Designed to Be a Faster, Lower Power Functional Equivalent of National DS3896, DS3897**

SN75ALS056
DW OR N PACKAGE
(TOP VIEW)



SN75ALS057
DW OR N PACKAGE
(TOP VIEW)



description

The SN75ALS056 is an 8-channel, monolithic, high-speed, advanced low-power Schottky device designed for 2-way data communication in a densely populated backplane. The SN75ALS057 is a 4-channel version with independent driver input (Dn) and receiver output (Rn) pins and a separate driver disable for each driver (En).

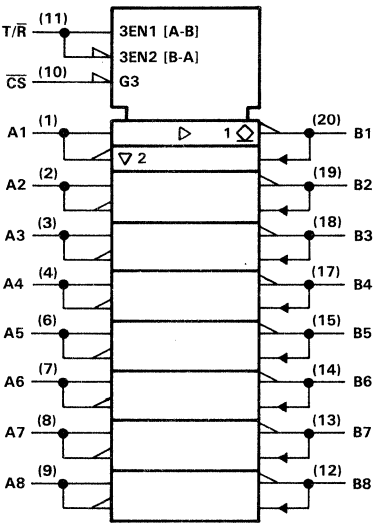
These transceivers feature open-collector driver outputs with a series Schottky diode to reduce capacitive loading to the bus. By using a 2-V pull-up termination on the bus, the output signal swing will be approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs generate trapezoidal waveforms that reduce crosstalk between channels. The drivers are capable of driving an equivalent dc load as low as 18.5 Ω.

The receivers have internal low-pass filters to further improve noise immunity.

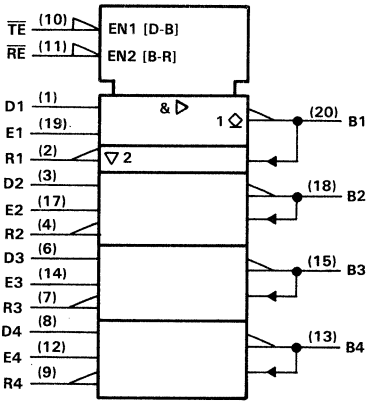
The SN75ALS056 and SN75ALS057 are characterized for operation from 0°C to 70°C.

logic symbols†

SN75ALS056

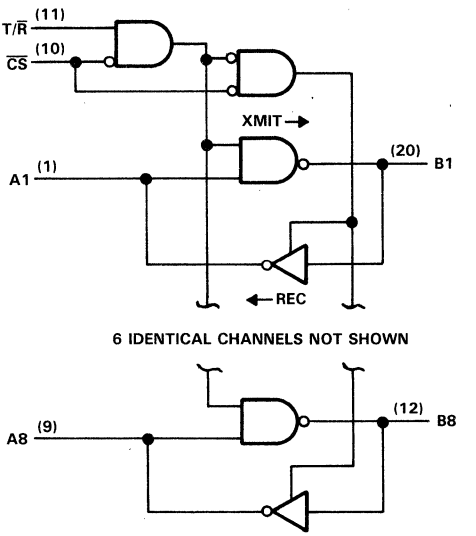


SN75ALS057

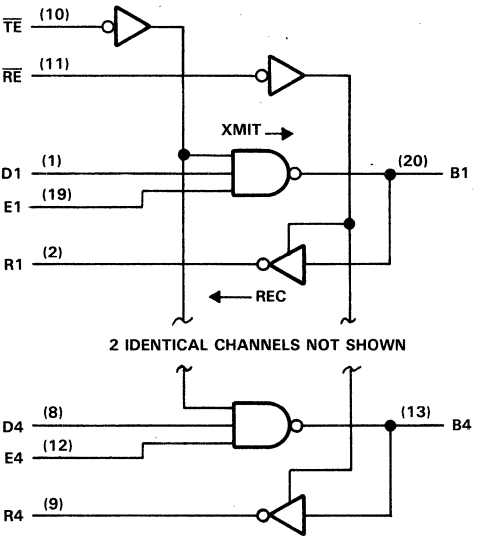


logic diagrams (positive logic)

SN75ALS056



SN75ALS057



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN75ALS056
FUNCTION TABLE
TRANSMIT/RECEIVE

CONTROLS		CHANNELS
$\overline{CS}$	T/$\overline{R}$	A ↔ B
L	H	T (A → B)
L	L	R (B → A)
H	X	D

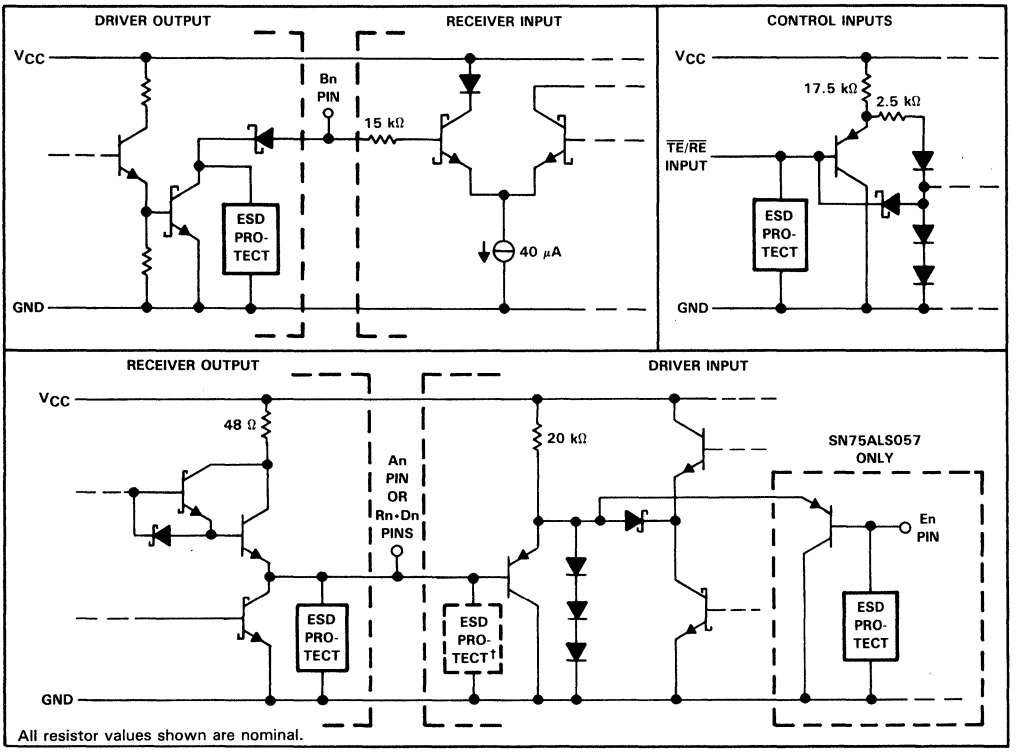
SN75ALS057
FUNCTION TABLE
TRANSMIT/RECEIVE

CONTROLS			CHANNELS	
$\overline{TE}$	$\overline{RE}$	En	D → B	B → R
L	L	L	D	R
L	L	H	T	R
L	H	L	D	D
L	H	H	T	D
H	L	X	D	R
H	H	X	D	D

H = high level, L = low level, R = receive, T = transmit, D = disable, X = irrelevant

Direction of data transmission is from An to Bn for the SN75ALS056 and from Dn to Bn for the SN75ALS057. Direction of data reception is from Bn to An for the SN75ALS056 and from Bn to Rn for the SN75ALS057. Data transfer is inverting in both directions.

schematics of inputs and outputs



†Additional ESD protection is on the SN75ALS057 only, which has separate receiver output and driver input pins.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6 V
Control input voltage . . . . . 5.5 V
Driver input voltage . . . . . 5.5 V
Driver output voltage . . . . . 2.5 V
Receiver input voltage . . . . . 2.5 V
Receiver output voltage . . . . . 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level driver and control input voltage, V_{IH}	2			V
Low-level driver and control input voltage, V_{IL}			0.8	V
Bus termination voltage	1.9		2.1	V
Operating free-air temperature, T_A	0		70	°C

SN75ALS056 electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage at An, T/$\overline{R}$, or $\overline{CS}$		I_I = −18 mA			−1.5	V
V_T	Receiver input threshold at Bn			1.426		1.674	mV
V_{OH}	High-level output voltage at An		Bn at 1.2 V, $\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V, I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage	An	Bn at 2 V, $\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V, I_{OL} = 16 mA			0.5	V
		Bn	An at 2 V, $\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 2 V, V_L = 2 V, R_L = 18.5 Ω, See Figure 1	0.75		1.2	
I_{IH}	High-level input current	An, T/$\overline{R}$, or $\overline{CS}$	V_I = V_{CC}			40	μA
		Bn	V_I = 2 V, V_{CC} = 0 or 5.25 V, An at 0.8 V, T/$\overline{R}$ at 0.8 V			100	
I_{IL}	Low-level input current at An, T/$\overline{R}$, or $\overline{CS}$		V_I = 0.4 V			−400	μA
I_{OS}	Short-circuit output current at An		An at 0 V, Bn at 1.2 V, $\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V	−40		−120	mA
I_{CC}	Supply current					75	mA
$C_{o(B)}$	Driver output capacitance				4.5		pF

SN75ALS057 electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage at Dn, En, $\overline{TE}$, or $\overline{RE}$		I_I = −18 mA			−1.5	V
V_T	Receiver input threshold at Bn			1426		1674	mV
V_{OH}	High-level output voltage at Rn		Bn at 1.2 V, $\overline{RE}$ at 0.8 V, I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage	Rn	Bn at 2 V, $\overline{RE}$ at 0.8 V, I_{OL} = 16 mA			0.5	V
		Bn	Dn at 2 V, En at 2 V, $\overline{TE}$ at 0.8 V, V_L = 2 V, R_L = 18.5 Ω, See Figure 1	0.75		1.2	
I_{IH}	High-level input current	Dn, En, $\overline{TE}$, or $\overline{RE}$	V_I = V_{CC}			40	μA
		Bn	V_I = 2 V, V_{CC} = 0 or 5.25 V, Dn at 0.8 V, En at 0.8 V, $\overline{TE}$ at 0.8 V			100	
I_{IL}	Low-level input current at Dn, En, $\overline{TE}$, or $\overline{RE}$		V_I = 0.4 V			−400	μA
I_{OS}	Short-circuit output current at Rn		Rn at 0, Bn at 1.2 V, $\overline{RE}$ at 0.8 V	−40		−120	mA
I_{CC}	Supply current					40	mA
$C_{o(B)}$	Driver output capacitance				4.5		pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of operating free-air temperature and V_{CC} (unless otherwise noted)

driver

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	An	Bn	$\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 2 V, V_L = 2 V, See Figure 2			19	ns
t_{PHL} Propagation delay time, high-to-low-level output						18	
t_{PLH} Propagation delay time, low-to-high-level output	$\overline{CS}$	Bn	An and T/$\overline{R}$ at 2 V, V_L = 2 V, See Figure 2			24	ns
t_{PHL} Propagation delay time, high-to-low-level output						20	
t_{PLH} Propagation delay time, low-to-high-level output	T/$\overline{R}$	Bn	$V_{I(An, Bn)}$ = 5 V, $\overline{CS}$ at 0.8 V, R_{L2} not connected, C_L = 30 pF, R_{L1} = 18 Ω, See Figure 3			25	ns
t_{PHL} Propagation delay time, high-to-low-level output						35	
t_{TLH} Transition time, low-to-high-level output	An	Bn	$\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 2 V, V_L = 2 V, See Figure 2	1	3	11	ns
t_{THL} Transition time, high-to-low-level output				1	3	6	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of operating free-air temperature and V_{CC} (unless otherwise noted)

receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Bn	An	$\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V, See Figure 4		18	ns
t_{PHL}	Propagation delay time, high-to-low-level output					18	
t_{PLZ}	Output disable time from low level	$\overline{CS}$	An	Bn at 2 V, T/$\overline{R}$ at 0.8 V, C_L = 5 pF, V_L = 5 V, R_{L1} = 390 Ω, R_{L2} not connected, See Figure 5		18	ns
t_{PZL}	Output enable time to low level	$\overline{CS}$	An	Bn at 2 V, T/$\overline{R}$ at 0.8 V, C_L = 30 pF, V_L = 5 V, R_{L1} = 390 Ω, R_{L2} = 1.6 kΩ, See Figure 5		15	ns
t_{PHZ}	Output disable time from high level	$\overline{CS}$	An	Bn at 0.8 V, T/$\overline{R}$ at 0.8 V, C_L = 5 pF, V_L = 0, R_{L1} = 390 Ω, R_{L2} not connected, See Figure 5		8	ns
t_{PZH}	Output enable time to high level	$\overline{CS}$	An	Bn at 0.8 V, T/$\overline{R}$ at 0.8 V, C_L = 30 pF, V_L = 0, R_{L1} not connected, R_{L2} = 1.6 kΩ, See Figure 5		17	ns
t_{PLZ}	Output disable time from low level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(An,Bn)}$ = 2 V, V_L = 5 V, R_{L1} = 390 Ω, R_{L2} not connected, C_L = 5 pF, See Figure 3		20	ns
t_{PZL}	Output enable time to low level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(An,Bn)}$ = 2 V, V_L = 5 V, R_{L1} = 390 Ω, R_{L2} = 1.6 kΩ, C_L = 30 pF, See Figure 3		40	ns
t_{PHZ}	Output disable time from high level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(An,Bn)}$ = 0, V_L = 0, R_{L1} = 390 Ω, R_{L2} not connected, C_L = 5 pF, See Figure 3		17	ns
t_{PZH}	Output enable time to high level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(An,Bn)}$ = 0, V_L = 0, R_{L1} not connected, R_{L2} = 1.6 kΩ, C_L = 30 pF, See Figure 3		15	ns
$t_{w(NR)}$	Receiver noise rejection pulse duration	Bn	An or Rn	$\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V, See Figure 6	3		ns

switching characteristics over recommended ranges of operating free-air temperature and V_{CC} (unless otherwise noted)

driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Dn or En	Bn	$\overline{TE}$ at 0.8 V, $\overline{RE}$ at 2 V, V_L = 2 V, See Figure 2			19	ns
t_{PHL}	Propagation delay time, high-to-low-level output						18	
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{TE}$	Bn	Dn, En, $\overline{RE}$ at 2 V, V_L = 2 V, R_{L1} = 18 Ω, See Figure 2			24	ns
t_{PHL}	Propagation delay time, high-to-low-level output						20	
t_{TLH}	Transition time, low-to-high-level output	Dn or En	Bn	$\overline{RE}$ at 2 V, V_L = 2 V, $\overline{TE}$ at 0.8 V, See Figure 2	1	3	11	ns
t_{THL}	Transition time, high-to-low-level output				1	3	6	

receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Bn	Rn	$\overline{RE}$ at 0.8 V, $\overline{TE}$ at 2 V, See Figure 4		18	ns
t_{PHL}	Propagation delay time, high-to-low-level output					18	
t_{PLZ}	Output disable time from low level	$\overline{RE}$	Rn	Bn at 2 V, $\overline{TE}$ at 2 V, V_L = 5 V, C_L = 5 pF, R_{L1} = 390 Ω, R_{L2} not connected, See Figure 5		18	ns
t_{PZL}	Output enable time to low level	$\overline{RE}$	Rn	Bn at 2 V, $\overline{TE}$ at 2 V, V_L = 5 V, C_L = 30 pF, R_{L1} = 390 Ω, R_{L2} 1.6 kΩ, See Figure 5		15	ns
t_{PHZ}	Output disable time from high level	$\overline{RE}$	Rn	Bn at 0.8 V, $\overline{TE}$ at 2 V, V_L = 0, C_L = 5 pF, R_{L1} = 390 Ω, R_{L2} not connected, See Figure 5		17	ns
t_{PZH}	Output enable time to high level	$\overline{RE}$	Rn	Bn at 0.8 V, $\overline{TE}$ at 2 V, V_L = 0, C_L = 30 pF, R_{L1} not connected, R_{L2} = 1.6 kΩ, See Figure 5		17	ns
$t_{w(NR)}$	Receiver noise rejection pulse duration	Bn	Cn	$\overline{TE}$ at 2.0 V, $\overline{RE}$ at 0.8 V, See Figure 6	3		ns

driver plus receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Dn	Rn	$\overline{RE}$ at 0.8 V, $\overline{TE}$ at 0.8 V, See Figure 7		40	ns
t_{PHL}	Propagation delay time, high-to-low-level output					40	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

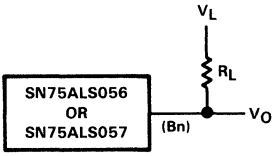
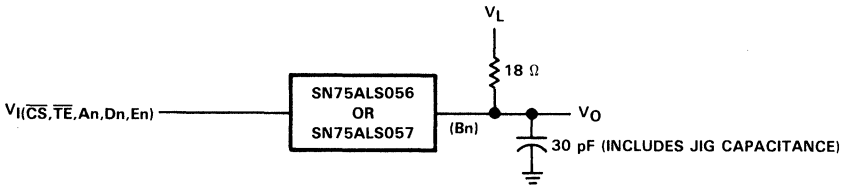
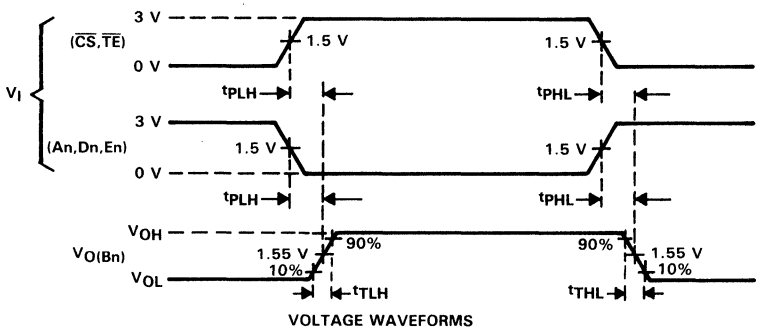


FIGURE 1. DRIVER LOW-LEVEL-OUTPUT-VOLTAGE TEST CIRCUIT



TEST CIRCUIT

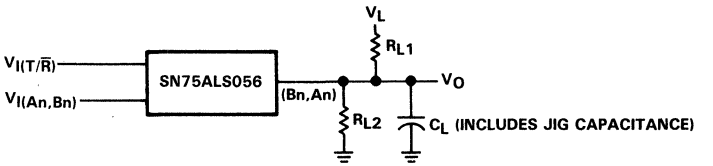


VOLTAGE WAVEFORMS

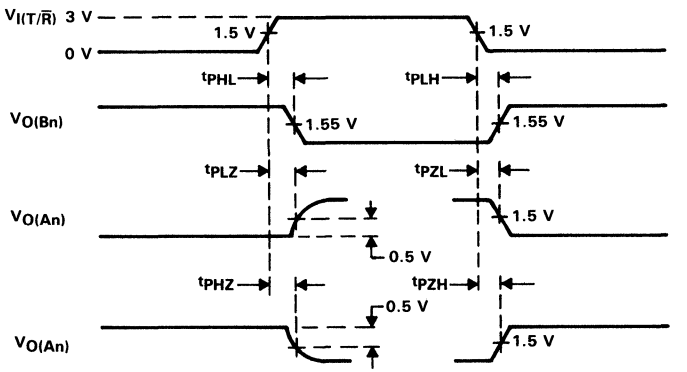
NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 2. DRIVER PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



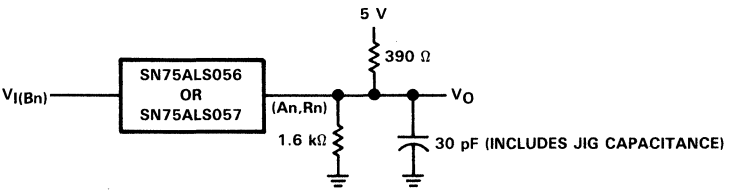
TEST CIRCUIT



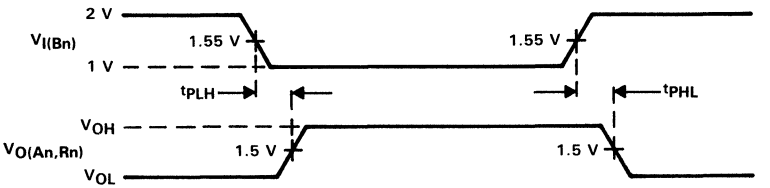
VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 3. PROPAGATION DELAY FROM T/$\overline{R}$ TO An OR Bn



TEST CIRCUIT

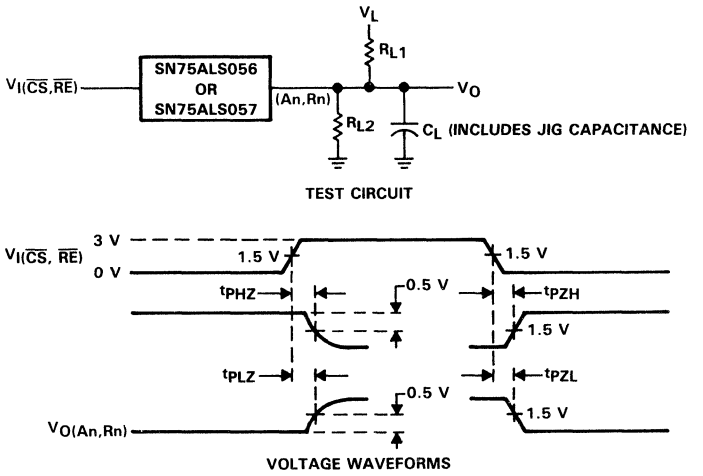


VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \leq 10$ ns from 10% to 90%

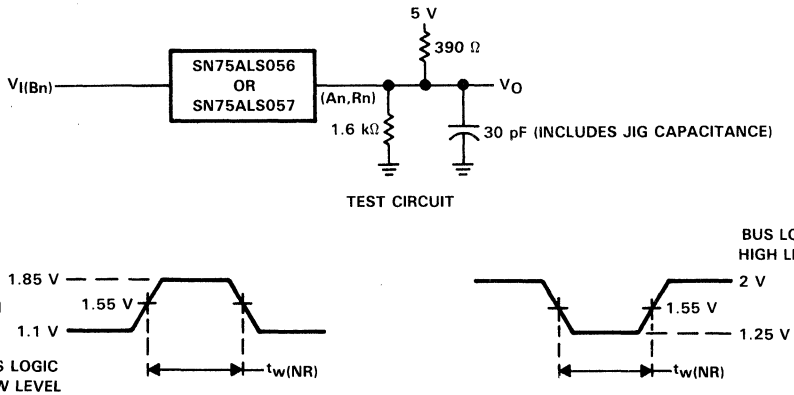
FIGURE 4. RECEIVER PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

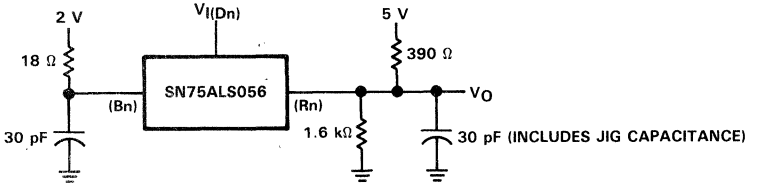
FIGURE 5. PROPAGATION DELAY FROM $\overline{CS}$ TO An OR $\overline{RE}$ TO Rn



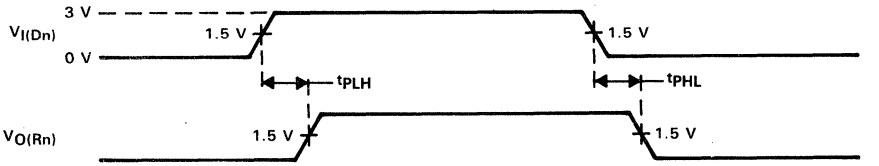
NOTE: $t_r = t_f \leq 2$ ns from 10% to 90%

FIGURE 6. RECEIVER NOISE IMMUNITY

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

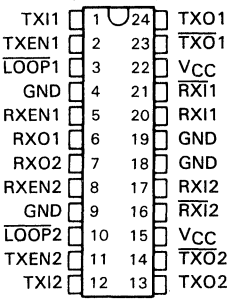
NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 7. DRIVER PLUS RECEIVER DELAY TIMES

D3279, APRIL 1989

- **Compatible with IOS 8802.3:1989 and ANSI/IEEE Std 802.3-1988**
- **Interdevice Loop-Back Paths for System Testing**
- **Squelch Function Implemented on the Receiver Inputs**
- **Drivers Will Drive a Balanced 78-Ω Load**
- **Transformer Coupling Not Required in System**
- **Power-Up/Power-Down Protection (Glitch-Free)**
- **Isolated Ground Pins for Reduced Noise Coupling**
- **Fault-Condition Protection Built into the Device**
- **Driver Inputs Are Level-Shifted ECL Compatible**

NT
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The SN75ALS085 is a monolithic, high-speed, advanced low-power Schottky, dual-channel driver/receiver device designed for use in the AUI of ANSI/IEEE Std 802.3-1988. The two drivers on the device will drive a 78-Ω balanced, terminated twisted-pair transmission line up to a maximum length of 50 meters. In the off (idle) state, the drivers will maintain minimal differential output voltage on the twisted-pair line and, at the same time, remain within the required output common-mode range.

With the driver enable (TXEN) high, upon receiving the first falling edge into the driver input, the differential outputs will rise to full-amplitude output levels within 25 ns. The output amplitude will be maintained for the remainder of the packet. After the last positive packet edge transmitted into the driver, the driver will maintain a minimum of 70% of full differential output for a minimum of 200 ns, then decay down to a minimum level for the reset (idle) condition within 8 μs. Disabling the driver by taking the driver enable low will also force the output into the idle condition after the normal 8-μs timeout. While operating, the driver is able to withstand a set of fault conditions and not suffer damage due to the faults being applied. The drivers will power up in the idle state to ensure that no activity is placed on the twisted-pair cable that could be interpreted as network traffic.

The line receiver squelch function interfaces to a differential twisted-pair line terminated external to the device. The receiver squelch circuit allows differential receive signals to pass through as long as the input amplitude and pulse duration are greater than the minimum squelch threshold. This assures a good signal-to-noise ratio while the data path is active and prevents system noise from causing false data transitions during line shut down and line-idle conditions. The RXO outputs default to a high level and the RXEN outputs default to a low level while the squelch function is blocking the data path through the receiver (idle). The line receiver squelch will become active within 50 ns when the input squelch threshold is exceeded. The RXEN pin will be driven high while the squelch circuit is allowing data to pass through the receiver. The receiver squelch circuit will also withstand a set of fault conditions while operating without causing permanent damage to the device.

The purpose of the loop functions is to provide a means by which system data path verification can be done to isolate faulty interfaces and assist in network diagnosis. The LOOP pins are TTL compatible and must be held high for normal operation. When $\overline{\text{LOOP}}$1 is taken low, the output of driver 1 (TXO1) immediately goes into the idle state. Also, the input to receiver 1 is ignored and a path from TXI1 to RXO1 is established. When $\overline{\text{LOOP}}$1 is taken back high, driver 1 and receiver 1 revert back to their normal operation. When $\overline{\text{LOOP}}$2 is taken low, a similar data path is established between TXI1 and RXO2. TXEN1 must be high for the loop functions to operate and TXEN1 can be used to gate the loop function if desired. During loop operation, the respective receiver enable output (RXEN) will reflect the status of TXEN1.

RECEIVER FUNCTION TABLE
$\overline{\text{LOOP}}$ = H

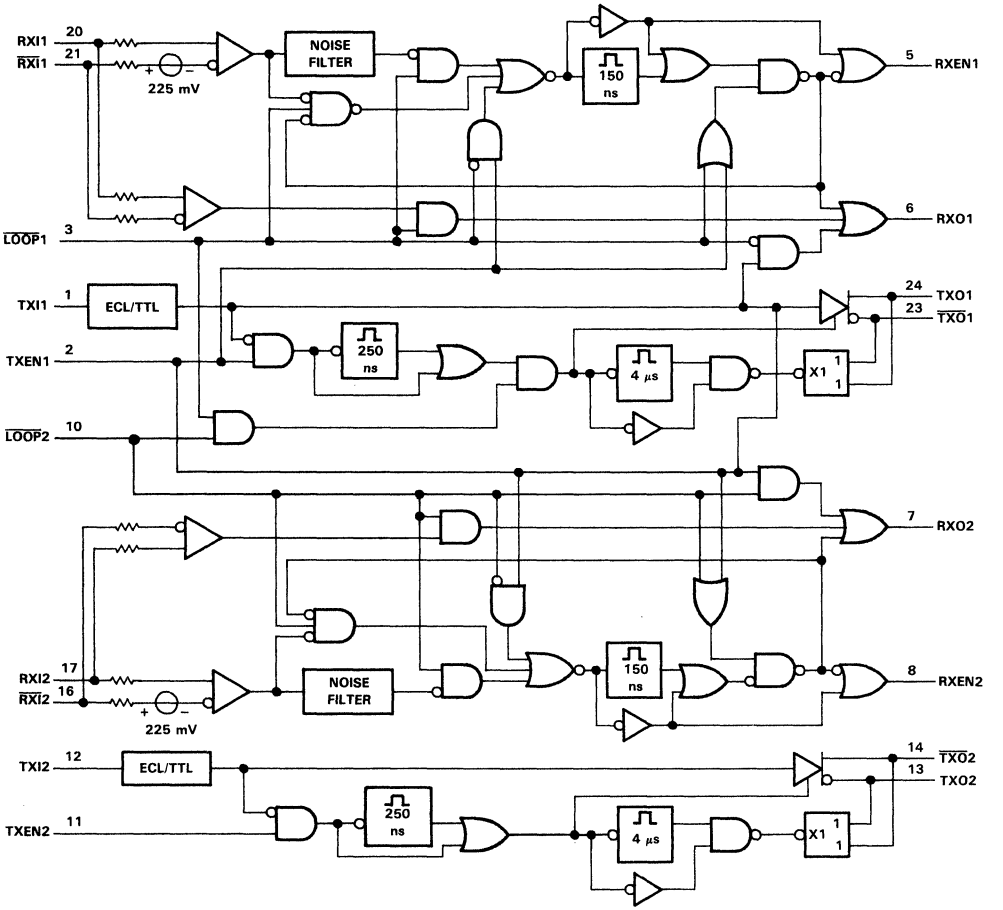
		OUTPUTS	
RXI	PREVIOUS RXEN	RXEN	RXO
V_{ID} = 1315 mV to −175 mV, t_w < 25 ns	L	L	H
V_{ID} = −275 mV to −1315 mV, t_w > 50 ns	X	H	L
V_{ID} = 318 mV to 1315 mV, t_w < 130 ns	H	H	H
V_{ID} = 318 mV to 1315 mV, t_w > 175 ns	X	L	H

DRIVER FUNCTION TABLE
$\overline{\text{LOOP}}$ = H

TXI	TXEN	PREVIOUS TXO	OUTPUT TXO
L	L	IDLE	IDLE
H	L	IDLE	IDLE
↓	H	IDLE	L
L	H	ACTIVE	L
H < 200 ns	H	ACTIVE	H
H > 8 μs	H	ACTIVE	IDLE
L	L > 8 μs	ACTIVE	IDLE
H < 200 ns	L > 8 μs	ACTIVE	IDLE
H < 200 ns	L < 200 ns	ACTIVE	H
H > 8 μs	L < 200 ns	ACTIVE	IDLE
L	L < 200 ns	ACTIVE	L

H = $V_I \geq V_T$ max, L = $V_I \leq V_T$ min

logic diagram (positive logic)



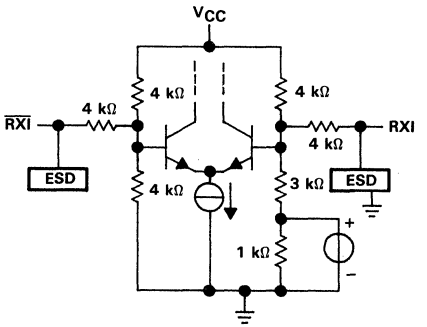
LOOP FUNCTION TABLE

INPUTS						OUTPUTS				
$\overline{LOOP}$1	$\overline{LOOP}$2	TXI1	TXEN1	RXI1	RXI2	RXO1	RXO2	RXEN1	RXEN2	TXO1
L	L	L	H	X	X	L	L	H	H	IDLE
L	L	H	H	X	X	H	H	H	H	IDLE
L	L	X	L	X	X	H	H	L	L	IDLE
L	H	L	H	X	NORMAL	L	NORMAL	H	NORMAL	IDLE
L	H	H	H	X	NORMAL	H	NORMAL	H	NORMAL	IDLE
L	H	X	L	X	NORMAL	H	NORMAL	L	NORMAL	IDLE
H	L	L	H	NORMAL	X	NORMAL	L	NORMAL	H	IDLE
H	L	H	H	NORMAL	X	NORMAL	H	NORMAL	H	IDLE
H	L	X	L	NORMAL	X	NORMAL	H	NORMAL	L	IDLE
H	H	NORMAL	NORMAL	NORMAL	NORMAL	NORMAL	NORMAL	NORMAL	NORMAL	NORMAL

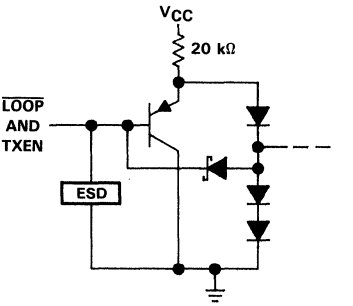
H = high level, L = low level, X = don't care

schematics of inputs and outputs

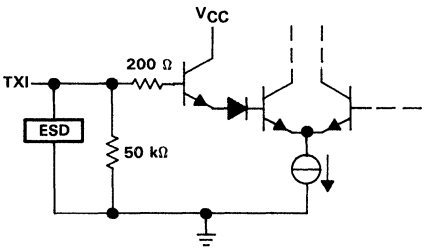
RXI AND RXI INPUTS



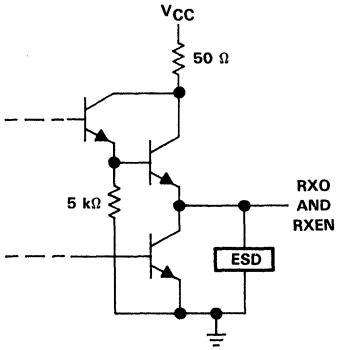
LOOP AND TXEN INPUTS



TXI INPUTS



RXO AND RXEN OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6 V
TXI and $\overline{LOOP}$ input voltage . . . . . 5.5 V
TXO and $\overline{TXO}$ output voltage . . . . . 16 V
RXI and $\overline{RXI}$ input voltage . . . . . 16 V
RXO and RXEN output voltage . . . . . 5.5 V
Continuous total power dissipation at (or below) 25°C (see Note 2) . . . . . 1250 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly to 800 mW at 70°C at the rate of 10 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode voltage at RXI inputs, V_{IC}	1		4.2	V
Differential voltage between RXI inputs, V_{ID}	±318		±1315	mV
High-level input voltage, $\overline{LOOP}$ and TXEN, V_{IH}	2			V
Low-level input voltage, $\overline{LOOP}$ and TXEN, V_{IL}			0.8	V
High-level output current, RXO and RXEN, I_{OH}			−0.4	mA
Low-level output voltage, RXO and RXEN, I_{OL}			16	mA
Setup time, Driver mode, TXEN high before TXI↓, t_{su1} (see Figure 8)	10			ns
Setup time, Loop mode, $\overline{LOOP}$ low before TXEN↑, t_{su2} (see Figure 10)	15			ns
Setup time, Loop mode, TXEN high before TXI↓, t_{su3} (see Figure 10)	10			ns
Hold time, Loop mode, TXEN high after TXI↑, t_{h1} (see Figure 9)	10			ns
Hold time, Loop mode, $\overline{LOOP}$ low after TXEN↓, th_2 (see Figure 9)	15			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{IK}	Clamp voltage at all inputs		I_I = −18 mA			−1.5	V
V_T	Driver input (TXI) threshold voltage		T_A = 0°C	V_{CC} = 4.75 V	3.202	3.752	V
				V_{CC} = 5 V	3.389	3.998	
				V_{CC} = 5.25 V	3.577	4.244	
			T_A = 25°C	V_{CC} = 4.75 V	3.213	3.797	V
				V_{CC} = 5 V	3.400	4.043	
				V_{CC} = 5.25 V	3.588	4.289	
			T_A = 70°C	V_{CC} = 4.75 V	3.239	3.849	V
				V_{CC} = 5 V	3.426	4.095	
				V_{CC} = 5.25 V	3.614	4.341	
V_{IDT}	Receiver differential input threshold voltage					−275	mV
V_{OC}	Driver output (TXO) common-mode voltage	Idle	TXEN at 0.8 V, $\overline{LOOP}$1 at 2 V, $\overline{LOOP}$2 at 2 V, See Figure 1		1	4.2	V
		Active	TXEN at 2 V, $\overline{LOOP}$1 at 2 V, $\overline{LOOP}$2 at 2 V, TXI at 3.2 V, See Figure 1		1	4.2	
		Active	TXEN at 2 V, $\overline{LOOP}$1 at 2 V, $\overline{LOOP}$2 at 2 V, TXI at 4.4 V, See Figure 1		1	4.2	
V_{OD}	Driver output (TXO) differential voltage	Idle	TXEN at 0.8 V, $\overline{LOOP}$1 at 2 V, $\overline{LOOP}$2 at 2 V, See Figure 1			±40	mV
		Active	TXEN at 2 V, $\overline{LOOP}$1 at 2 V, $\overline{LOOP}$2 at 2 V, TXI at 3.2 V, See Figure 1		−600	−1315	
		Active	TXEN at 2 V, $\overline{LOOP}$1 at 2 V, $\overline{LOOP}$2 at 2 V, TXI at 4.4 V, See Figure 1		600	1315	
V_{OH}	High-level output voltage	RXO, RXEN	I_{OH} = −0.4 mA		2.4		V
V_{OL}	Low-level output voltage	RXO, RXEN	I_{OL} = 16 mA			0.5	V
I_{IH}	High-level input current	TXEN, $\overline{LOOP}$	V_I = 2 V			20	μA
		TXI	V_I = 4.5 V			400	
		$\overline{RXI}$, RXI	V_{ID} = −0.5 V, V_{IC} = 1 V to 4.2 V			1000	
I_{IL}	Low-level input current	TXEN, $\overline{LOOP}$	V_I = 0.8 V			−200	μA
		TXI	V_I = 3.1 V			100	
			V_I = 0.3 V		4	10	
		$\overline{RXI}$, RXI	V_{ID} = 0.5 V, V_{IC} = 1 V to 4.2 V			1000	
I_{OD}	Driver differential output current	Idle	TXEN at 0.8 V, $\overline{LOOP}$1 at 2 V, $\overline{LOOP}$2 at 2 V, See Figure 2			±4	mA
I_{OS}	Short-circuit output current†	RXO, RXEN	V_O at 0 V, $\overline{RXI}$ at 3 V, RXI at 2 V		−40	−150	mA
I_{CC}	Supply current		$\overline{LOOP}$ at 2 V, TXEN at 2 V, TXI at 4.5 V, Outputs open			225	mA

†Not more than one output should be shorted at a time, and the duration of the test should not exceed 1 second.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS†	MIN	MAX	UNIT
Driver fault condition current	TXO shorted to $\overline{\text{TXO}}$, Current measured in short		150	mA
	TXO at 0 V, $\overline{\text{TXO}}$ is open, Current measured at TXO		150	
	TXO is open, $\overline{\text{TXO}}$ at 0, Current measured at $\overline{\text{TXO}}$		150	
	TXO at 0 V, $\overline{\text{TXO}}$ at 0 V, Current measured at TXO and $\overline{\text{TXO}}$		150	
	TXO at 16 V, $\overline{\text{TXO}}$ is open, Current measured at TXO		150	
	TXO is open, $\overline{\text{TXO}}$ at 16 V, Current measured at TXO		150	
	TXO at 16 V, $\overline{\text{TXO}}$ at 16 V, Current measured at TXO and $\overline{\text{TXO}}$		150	
Receiver fault condition current	RXI shorted to $\overline{\text{RXI}}$, Current measured in short		10	mA
	RXI at 0 V, $\overline{\text{RXI}}$ is open, Current measured at RXI		3	
	RXI is open, $\overline{\text{RXI}}$ at 0 V, Current measured at RXI		3	
	RXI at 0 V, $\overline{\text{RXI}}$ at 0 V, Current measured at RXI and $\overline{\text{RXI}}$		3	
	RXI at 16 V, $\overline{\text{RXI}}$ at open, Current measured at RXI		10	
	RXI at open, $\overline{\text{RXI}}$ at 16 V, Current measured at $\overline{\text{RXI}}$		10	
	RXI at 16 V, $\overline{\text{RXI}}$ at 16 V, Current measured at RXI and $\overline{\text{RXI}}$		10	

†Fault conditions should be measured on only one channel at a time.

switching characteristics over recommended ranges of operating free-air temperature and V_{CC} (unless otherwise noted)

driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	TXI	TXO, $\overline{TXO}$	TXEN at 2 V, See Figure 3		15	ns
t_{PHL}	Propagation delay time, high-to-low level output	TXI	TXO, $\overline{TXO}$	TXEN at 2 V, See Figure 3		15	ns
t_{PIL}	Propagation delay time, idle-to-low level output	TXI	TXO, $\overline{TXO}$	TXEN at 2 V, See Figure 4		25	ns
t_{PIL}	Propagation delay time, idle-to-low level output	TXEN	TXO, $\overline{TXO}$	TXI at 3.2 V, See Figure 5		25	ns
t_{PH70}	Propagation delay time, high-to-70% level output	TXI	TXO, $\overline{TXO}$	TXEN at 2 V, See Figure 6	200		ns
		TXEN	TXO, $\overline{TXO}$	TXI at 4.4 V, See Figure 7	200		
t_{PHI}	Propagation delay time, high-to-idle output	TXI	TXO, $\overline{TXO}$	TXEN at 2 V, See Figure 6	200	8000	ns
		TXEN	TXO, $\overline{TXO}$	TXI at 4.4 V, See Figure 7	200	8000	
V_U	Driver output differential undershoot	TXI	TXO, $\overline{TXO}$	TXEN at 2 V, See Figure 6		−100	mV
t_{skew}	Driver caused signal skew ($t_{PLH} - t_{PHL}$)	TXI	TXO, $\overline{TXO}$	TXEN at 2 V, See Figure 3		±3	ns
t_r	Rise time, TXO, $\overline{TXO}$			TXEN at 2 V, See Figure 3	1	5	ns
t_f	Fall time, TXO, $\overline{TXO}$			TXEN at 2 V, See Figure 3	1	5	ns

receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	$\overline{RXI}$, RXI	RXO	V_{IC} = 1 V to 4.2 V, See Figure 11		15	ns
t_{PHL}	Progagation delay time, high-to-low level output	$\overline{RXI}$, RXI	RXO	V_{IC} = 1 V to 4.2 V, See Figure 11		15	ns
t_{PLH}	Start-up delay time, low-to-high level output	$\overline{RXI}$, RXI	RXEN	V_{IC} = 1 V to 4.2 V, V_{ID} = −500 mV, See Figure 13		50	ns
t_{PHL}	Shutdown delay time, high-to-low level output	$\overline{RXI}$, RXI	RXEN	V_{IC} = 1 V to 4.2 V, V_{ID} = 500 mV, See Figure 13	130	175	ns
t_{skew}	Receiver caused signal skew ($t_{PLH} - t_{PHL}$)	$\overline{RXI}$, RXI	RXO	V_{IC} = 1 V to 4.2 V, V_{ID} = 500 mV, See Figure 11		±3	ns
t_w	Pulse duration at $\overline{RXI}$ and RXI (to not activate squelch)			V_{IC} = 1 V to 4.2 V, V_{ID} = −175 mV, See Figure 12	25		ns
t_w	Pulse duration at $\overline{RXI}$ and RXI (to activate squelch)			V_{IC} = 1 V to 4.2 V, V_{ID} = −275 mV, See Figure 12		50	ns
t_{r1}	Rise time, RXO			V_{IC} = 1 V to 4.2 V, V_{ID} = ±500 mV, See Figure 11	1	8	ns
t_{r2}	Rise time, RXEN			V_{IC} = 1 V to 4.2 V, V_{ID} = ±500 mV, See Figure 13	1	8	ns
t_{f1}	Fall time, RXO			V_{IC} = 1 V to 4.2 V, V_{ID} = ±500 mV, See Figure 11	1	8	ns
t_{f2}	Fall time, RXEN			V_{IC} = 2.5 V, V_{ID} = ±500 mV, See Figure 13	1	8	ns
t_{valid}	RXO valid after RXEN high			See Figure 11	−10	15	ns

switching characteristics over recommended ranges of operating free-air temperature and V_{CC} (unless otherwise noted)

loop

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	TXI	RXO	LOOP at 0.8 V, TXEN at 2 V, See Figure 14		30	ns
t_{PHL}	Propagation delay time, high-to-low level output	TXI	RXO	LOOP at 0.8 V, TXEN at 2 V, See Figure 14		30	ns
t_{PLH}	Propagation delay time, low-to-high level output	TXEN	RXEN	LOOP at 0.8 V, See Figure 15		50	ns
t_{PHL}	Propagation delay time, high-to-low level output	TXEN	RXEN	LOOP at 0.8 V, See Figure 15		50	ns

PARAMETER MEASUREMENT INFORMATION

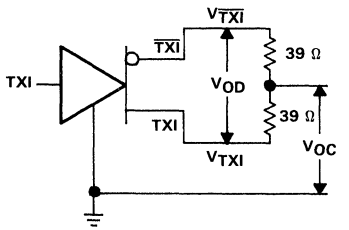


FIGURE 1

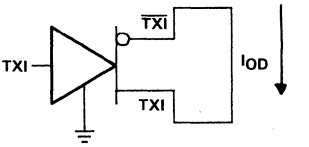
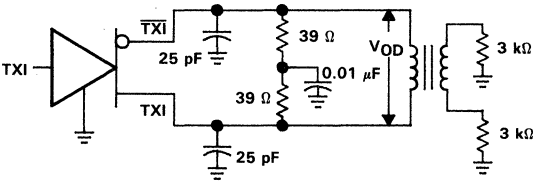
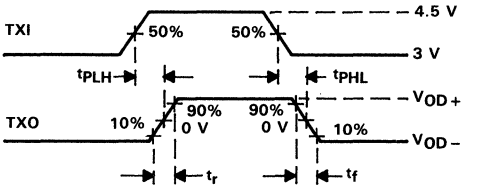


FIGURE 2

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



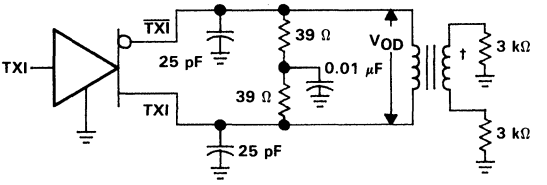
VOLTAGE WAVEFORMS

TRANSFORMER SPECIFICATIONS

Turns Ratio	1:1
Magnetizing Inductance	26 to 30 μH
Winding Resistance	0.6 Ω Max
Rise Time 10% to 90%	5 ns Max
Interwinding Capacitance	25 pF
Leakage Inductance	0.25 μH Max
Inductive Q	1250 Min

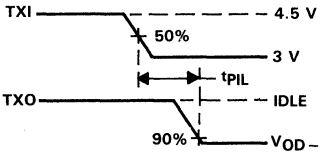
FIGURE 3

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

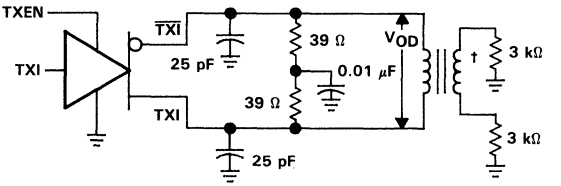
†See Figure 3



VOLTAGE WAVEFORMS

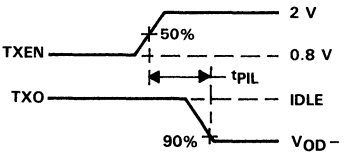
NOTE: Input $t_r \leq 5$ ns from 10% to 90%; $t_f \leq 5$ ns from 90% to 10%

FIGURE 4



TEST CIRCUIT

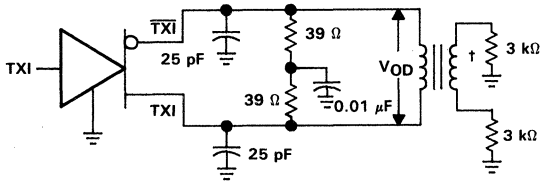
†See Figure 3



VOLTAGE WAVEFORMS

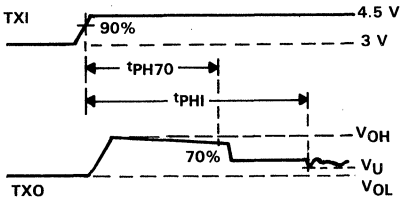
FIGURE 5

PARAMETER MEASUREMENT INFORMATION



†See Figure 3

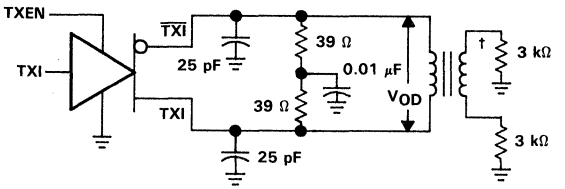
TEST CIRCUIT



VOLTAGE WAVEFORMS

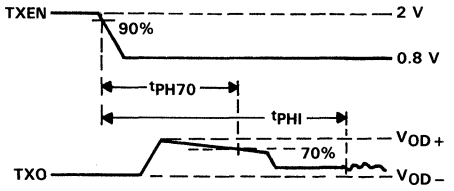
NOTE: Input $t_r \leq 5$ ns from 10% to 90%; $t_f \leq 5$ ns from 90% to 10%

FIGURE 6



†See Figure 3

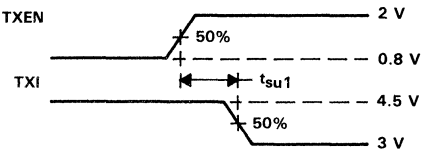
TEST CIRCUIT



VOLTAGE WAVEFORMS

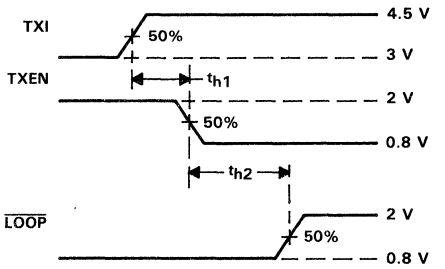
FIGURE 7

PARAMETER MEASUREMENT INFORMATION



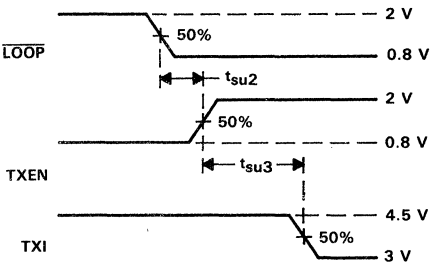
NOTE: Input $t_r \leq 5$ ns from 10% to 90%; $t_f \leq 5$ ns from 90% to 10%

FIGURE 8



NOTE: Input $t_r \leq 5$ ns from 10% to 90%; $t_f \leq 5$ ns from 90% to 10%

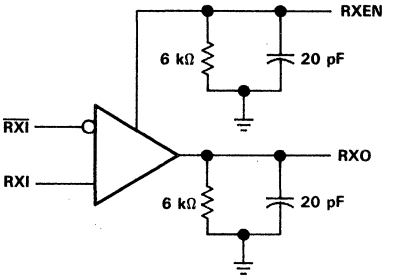
FIGURE 9



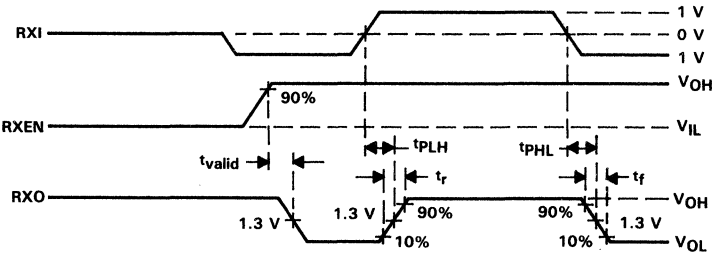
NOTE: Input $t_r \leq 5$ ns from 10% to 90%; $t_f \leq 5$ ns from 90% to 10%

FIGURE 10

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

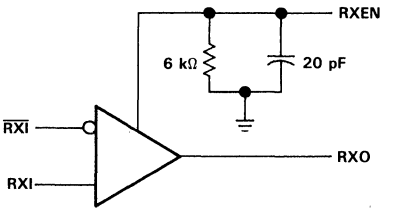


VOLTAGE WAVEFORMS

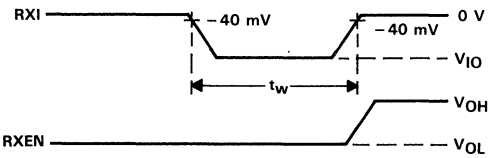
NOTE: Input $t_r \leq 5$ ns from 10% to 90%; $t_f \leq 5$ ns from 90% to 10%

FIGURE 11

PARAMETER MEASUREMENT INFORMATION

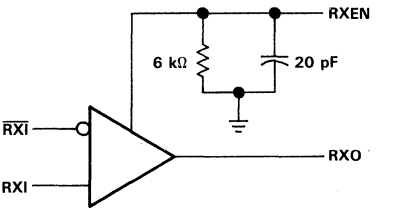


TEST CIRCUIT

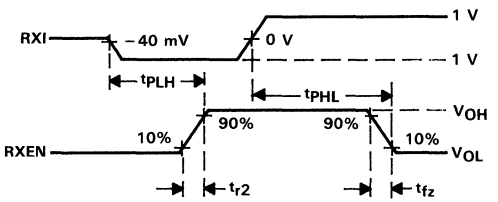


VOLTAGE WAVEFORMS

FIGURE 12



TEST CIRCUIT

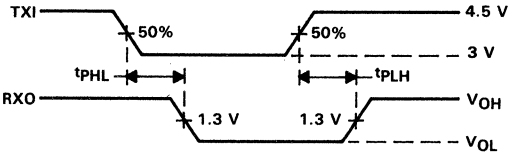


VOLTAGE WAVEFORMS

NOTE: Input $t_r \leq 5$ ns from 10% to 90%; $t_f \leq 5$ ns from 90% to 10%

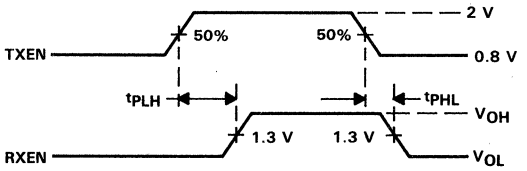
FIGURE 13

PARAMETER MEASUREMENT INFORMATION



NOTE: Input $t_r \leq 5$ ns from 10% to 90%; $t_f \leq 5$ ns from 90% to 10%

FIGURE 14



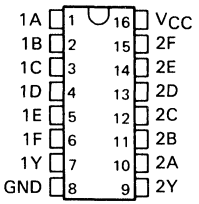
NOTE: Input $t_r \leq 5$ ns from 10% to 90%; $t_f \leq 5$ ns from 90% to 10%

FIGURE 15

D1334, SEPTEMBER 1987—REVISED AUGUST 1989

- **Permits Digital Data Transmission over Coaxial Cable, Strip Line, or Twisted Pair**
- **Operates with 50-Ω to 500-Ω Transmission Lines**
- **TTL-Compatible with 5-V Supply**
- **2.4-V Output at I_{OH} = −75 mA**
- **Uncommitted Emitter-Follower Output Structure for Party-Line Operation**
- **IMPACT™ Low-Power Schottky Technology**
- **Improved Replacement for the SN75121 and Signetics 8T13**
- **Glitchless Power-Up/Power-Down**
- **Short-Circuit Protection**
- **AND-OR Logic Configuration**
- **High Speed . . . Maximum Propagation Delay Time of 14 ns at C_L = 15 pF**

D OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All other input combinations						L

H = high level
L = low level
X = irrelevant

description

The SN75ALS121 dual line driver is designed for digital data transmission over lines having impedances from 50 to 500 Ω. It is compatible with standard TTL logic and supply voltage levels.

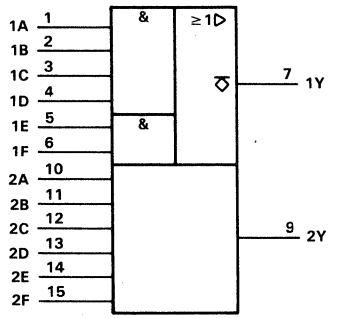
The low-impedance emitter-follower outputs drive terminated lines such as coaxial cable, strip line, or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 1.5 volts. All inputs are in conventional TTL configuration. Gating can be used during power-up and power-down sequences to ensure that no noise is introduced on the line.

The SN75ALS121 employs the IMPACT™ process to achieve fast switching speeds, low power dissipation, and reduced input current requirements.

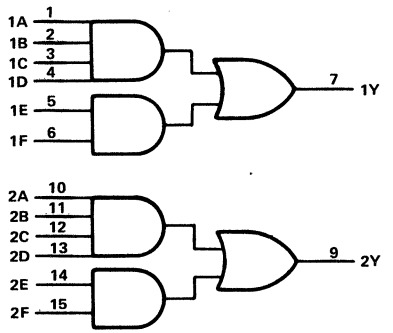
The SN75ALS121 is characterized for operation from 0°C to 70°C.

IMPACT is a trademark of Texas Instruments Incorporated

logic symbol†

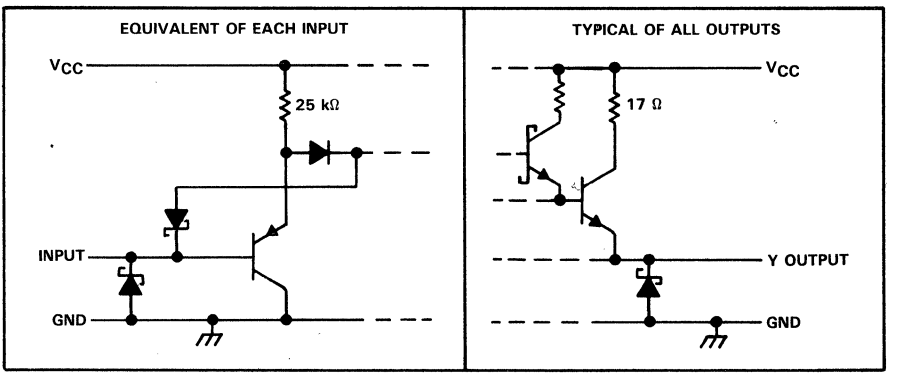


logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6 V
Input voltage . . . . . 6 V
Output voltage . . . . . 6 V
Continuous total dissipation at (or below) 25°C free air temperature (see Note 2):
D package . . . . . 950 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the D package linearly to 608 mW at 70°C at the rate of 7.6 mW/°C and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−75	mA
Operating free-air temperature range, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 5 V,	I_I = −12 mA				−1.5	V
$V_{(BR)I}$	Input breakdown voltage	V_{CC} = 5 V,	I_I = 10 mA		5.5			V
V_{OH}	High-level output voltage	V_{IH} = 2 V,	I_{OH} = −75 mA,	See Note 3	2.4	3.2		V
I_{OH}	High-level output current	V_{CC} = 5 V, T_A = 25°C,	V_{IH} = 4.5 V, See Note 3	V_{OH} = 2 V,	−100	−200	−250	mA
I_{OL}	Low-level output current	V_{IL} = 0.8 V,	V_{OL} = 0.4 V,	See Note 3			−800	μA
$I_{O(off)}$	Off-state output current	V_{CC} = 3 V,	V_O = 3 V				500	μA
I_{IH}	High-level input current	V_I = 4.5 V					40	μA
I_{IL}	Low-level input current	V_I = 0.4 V					−250	μA
I_{OS}	Short-circuit output current	V_{CC} = 5 V				−5	−30	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	All inputs at 2 V,	No load		9	14	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	All inputs at 0.8 V,	No load		13	30	mA

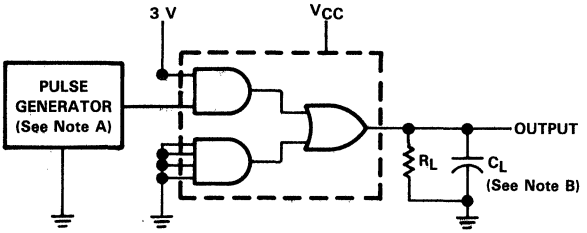
† All typical values are at V_{CC} = 5 V and T_A = 25°C.
NOTE 3: The output voltage and current limits are ensured for any appropriate combination of high and low inputs specified by the function table for the desired output.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

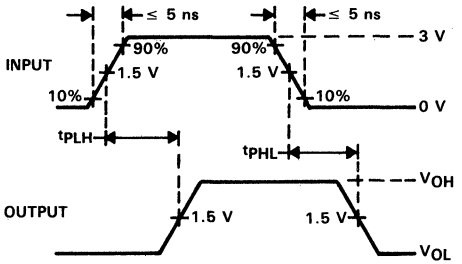
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 37 Ω, C_L = 15 pF, See Figure 1		6	14	ns
t_{PHL}	Propagation delay time, high-to-low-level output			4	14	ns
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 37 Ω, C_L = 1000 pF, See Figure 1		18	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			29	50	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, t_w = 200 ns, duty cycle = 50%.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

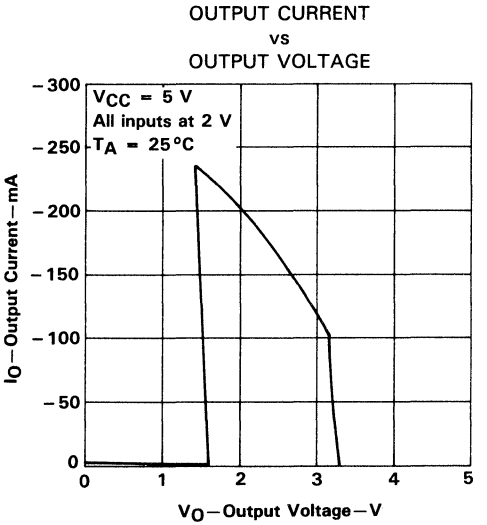
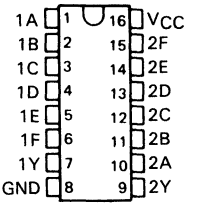


FIGURE 2

D1332, SEPTEMBER 1987—REVISED AUGUST 1989

- **Meets IBM 360 Input Interface Specifications**
- **Permits Digital Data Transmission over Coaxial Cable, Strip Line, or Twisted Pair**
- **TTL-Compatible with 5-V Supply**
- **3.11-V Output at I_{OH} = −59.3 mA**
- **Uncommitted Emitter-Follower Output Structure for Party-Line Operation**
- **IMPACT™ Low-Power Schottky Technology**
- **Improved Replacement for the SN75123 and Signetics 8T13**
- **Glitchless Power-Up/Power-Down**
- **Short-Circuit Protection**
- **AND-OR Logic Configuration**
- **High Speed . . . Maximum Propagation Delay Time of 14 ns at C_L = 15 pF**

D OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All other input combinations						L

H = high level L = low level X = irrelevant

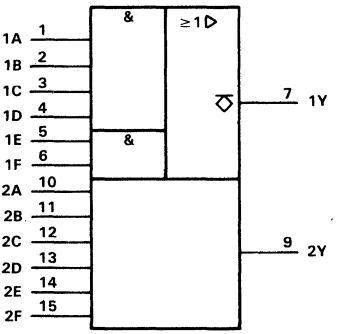
description

The SN75ALS123 dual line driver is specifically designed to meet the input interface specifications for the IBM System 360. It is compatible with standard TTL logic and supply voltage levels. The low-impedance, emitter-follower outputs drive terminated lines such as coaxial cable, strip line, or twisted pair. The uncommitted output allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 1.5 V. All inputs are in conventional TTL configuration. Gating can be used during power-up and power-down sequences to ensure that no noise is introduced on the line.

The SN75ALS123 employs the IMPACT™ process to achieve fast switching speeds, low power dissipation, and reduced input current requirements.

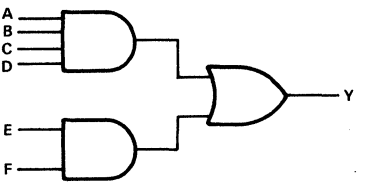
The SN75ALS123 is characterized for operation from 0°C to 70°C.

logic symbol†



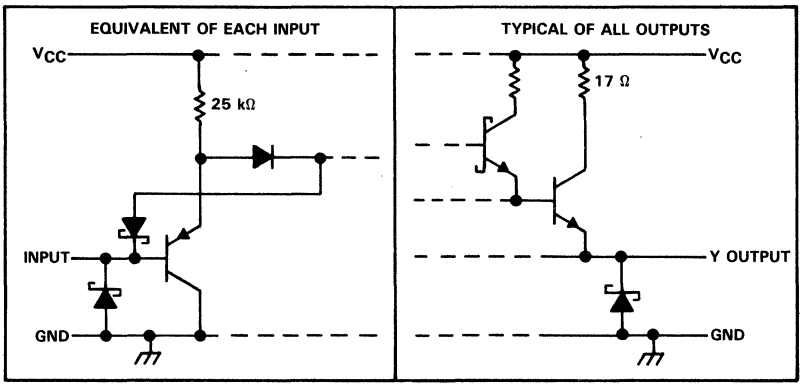
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each driver (positive logic)



IMPACT is a trademark of Texas Instruments Incorporated.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Output voltage . . . . . 6 V
Continuous total dissipation at (or below) 25°C free air temperature (see Note 2):
D package . . . . . 950 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the D package to 608 mW at 70°C at the rate of 7.6 mW/°C and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−100	mA
Operating free-air temperature range, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 5 V,	I_I = −12 mA				−1.5	V
$V_{(BR)I}$	Input breakdown voltage	V_{CC} = 5 V,	I_I = 10 mA		5.5			V
V_{OH}	High-level output voltage	V_{CC} = 5 V, See Note 3	V_{IH} = 2 V,	I_{OH} = −59.3 mA,	2.9			V
		V_{CC} = 5 V, T_A = 25°C,	V_{IH} = 2 V, See Note 3	I_{OH} = −59.3 mA,	3.11	3.3		
V_{OL}	Low-level output voltage	V_{IL} = 0.8 V,	I_{OL} = −240 μA,	See Note 2			0.15	V
I_{OH}	High-level output current	V_{CC} = 5 V, T_A = 25°C,	V_{IH} = 4.5 V, See Note 3	V_{OH} = 2 V,	−100	−200	−250	mA
$I_{O(off)}$	Off-state output current	V_{CC} = 0,	V_O = 3 V				40	μA
I_{IH}	High-level input current	V_I = 4.5 V					40	μA
I_{IL}	Low-level input current	V_I = 0.4 V					−250	μA
I_{OS}	Short-circuit output current	V_{CC} = 5 V				−5	−30	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	All inputs at 2 V,	No load		9	14	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	All inputs at 0.8 V,	No load		13	30	mA

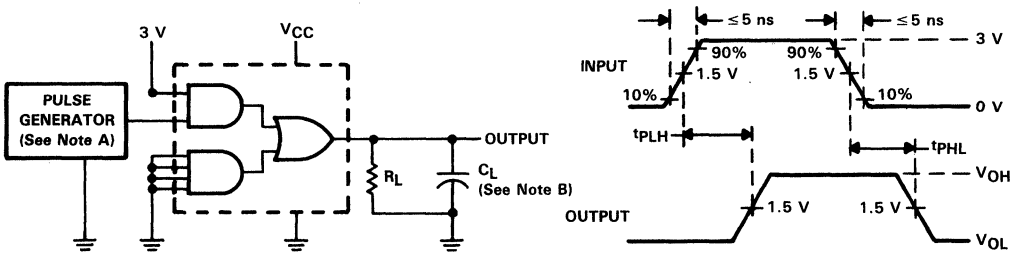
NOTE 3. The output voltage and current limits are ensured for any appropriate combination of high and low inputs specified by the function table for the desired output.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 50 Ω, C_L = 15 pF, See Figure 1		4	14	ns
t_{PHL}	Propagation delay time, high-to-low-level output			5	14	ns
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 50 Ω, C_L = 100 pF, See Figure 1		8	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			8	20	ns

†All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 1. SWITCHING TIMES

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, t_W = 200 ns, duty cycle = 50%.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

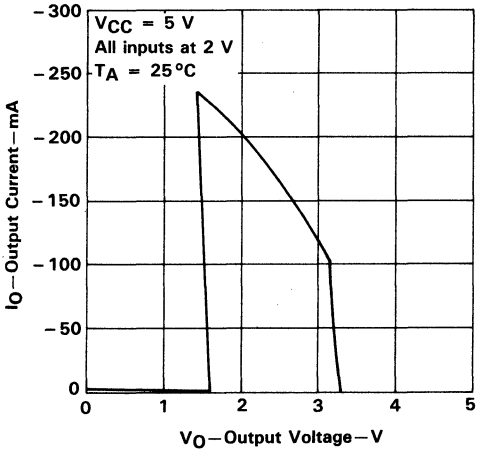


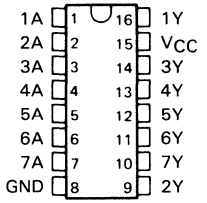
FIGURE 2

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

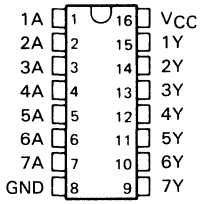
D2239, APRIL 1987—REVISED AUGUST 1989

- Meets IBM 360/370 I/O Specification
- Input Resistance . . . 7 kΩ to 20 kΩ
- Output Compatible with TTL
- IMPACT™ Low-Power Schottky Technology
- Operates from Single 5-V Supply
- High Speed . . . Low Propagation Delay
- Ratio Specification for Propagation Delay Time, Low-to-High/High-to-Low
- Glitch-Free Power-Up and Power-Down
- Seven Channels in One 16-Pin Package
- Standard V_{CC} and Ground Positioning on SN75ALS127

SN75ALS125 . . . D, J, OR N PACKAGE
(TOP VIEW)



SN75ALS127 . . . D, J, OR N PACKAGE
(TOP VIEW)



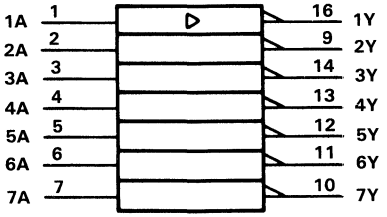
description

The SN75ALS125 and SN75ALS127 are monolithic seven-channel line receivers designed to satisfy the requirements of the IBM System 360/370 input/output interface specifications. Employing the IMPACT™ process allows low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs.

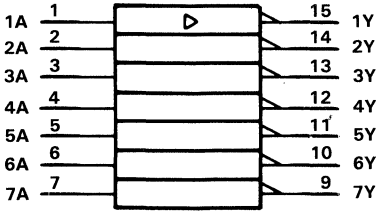
The SN75ALS125 and SN75ALS127 are characterized for operation from 0°C to 70°C.

logic symbols†

SN75ALS125



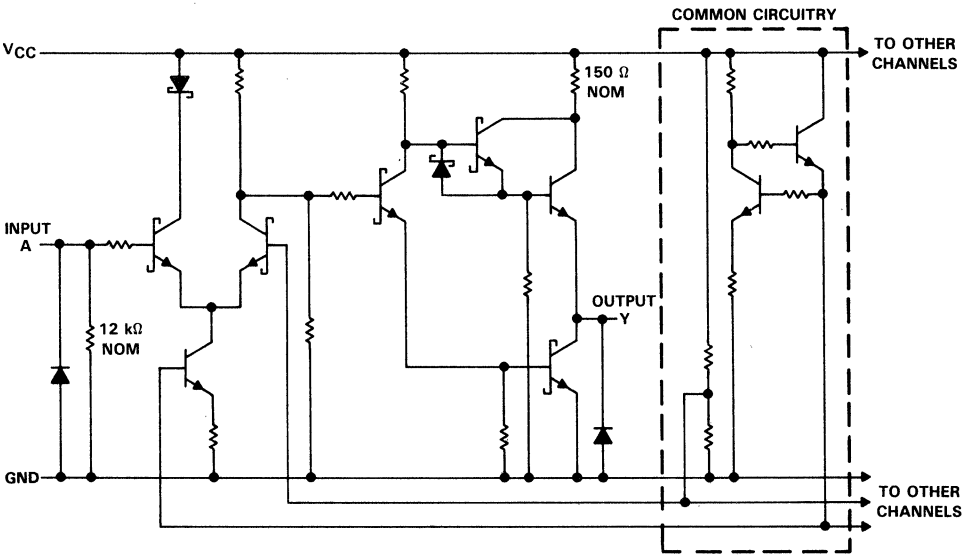
SN75ALS127



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

IMPACT is a trademark of Texas Instruments Incorporated

schematic (each receiver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage range . . . . . −0.15 V to 7 V
Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2):
D package . . . . . 950 mW
J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260 °C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25 °C free-air temperature, derate the D package to 608 mW at 70 °C at the rate of 7.6 mW/ °C, the J package to 656 mW/ °C at 70 °C at the rate of 8.2 mW/ °C, and the N package to 736 mW at 70 °C at the rate of 9.2 mW/ °C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH}	1.7			V
Low-level input voltage, V_{IL}			0.7	V
High-level output current, I_{OH}			−0.4	V
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

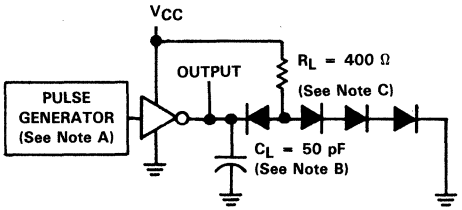
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V, V_{IL} = 0.7 V, I_{OH} = −0.4 mA	2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V, V_{IH} = 1.7 V, I_{OL} = 16 mA		0.4	0.5	V
I_{IH}	High-level input current	V_{CC} = 5.5 V, V_I = 3.11 V		0.3	0.42	mA
I_{IL}	Low-level input current	V_{CC} = 5.5 V, V_I = 0.15 V			30	μA
I_{OS}	Short-circuit output current‡	V_{CC} = 5.5 V, V_O = 0	−18		−60	mA
r_i	Input resistance	V_{CC} = 4.5 V, 0, or open, ΔV_I = 0.15 V to 4.15 V	7		20	kΩ
I_{CC}	Supply current	V_{CC} = 5.5 V, I_{OH} = −0.4 mA, All inputs at 0.7 V		15	25	mA
		V_{CC} = 5.5 V, I_{OL} = 16 mA, All inputs at 4 V		28	47	mA

switching characteristics over recommended operating temperature range (unless otherwise noted), V_{CC} = 5 V

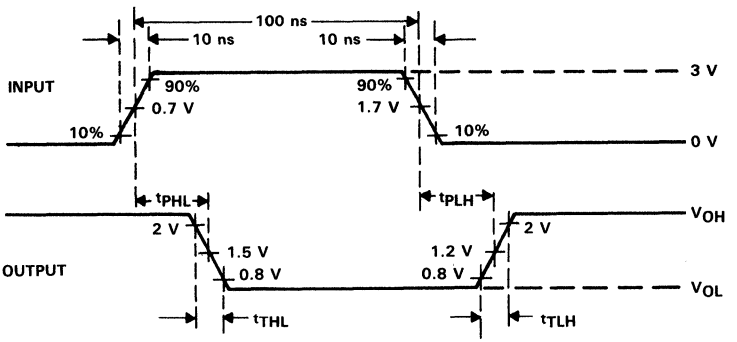
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 400 Ω, C_L = 50 pF, See Figure 1	7	14	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	18	30	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times		0.5	0.8	1.3	
t_{TLH}	Transition time, low-to-high-level output		1	7	12	ns
t_{THL}	Transition time, high-to-low-level output		1	3	12	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$, PRR $\leq$ 5 MHz.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

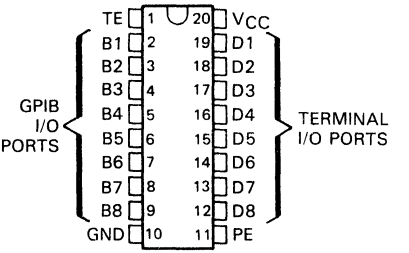
FIGURE 1

D2525, JUNE 1986—REVISED AUGUST 1989

MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

DW, J, OR N PACKAGE
(TOP VIEW)



description

The SN75ALS160 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky device designed for two-way data communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the passive-pullup or three-state mode. If Talk Enable (TE) is high, these ports have the characteristics of passive-pullup outputs when Pullup Enable (PE) is low, and of three-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. The driver outputs are designed to handle loads up to 48 milliamperes of sink current.

An active turn-off feature has been incorporated into the bus-terminating resistors so that the device exhibits a high impedance to the bus when V_{CC} = 0. When combined with the SN75ALS161 or SN75ALS162 management bus transceiver, the pair provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS160 is manufactured in a 20-pin package and is characterized for operation from 0°C to 70°C.

FUNCTION TABLES

EACH DRIVER

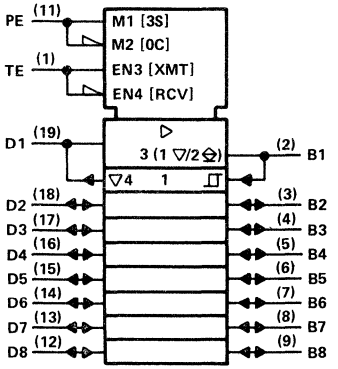
INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z†
X	L	X	Z†

EACH RECEIVER

INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

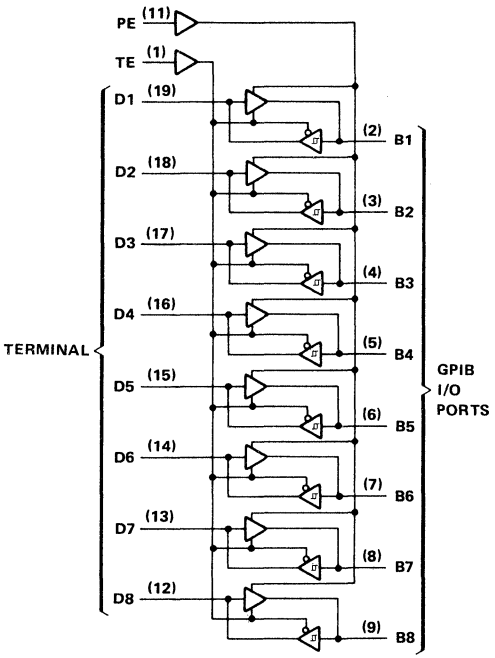
H = high level, L = low level, X = irrelevant,
Z = high-impedance state.
† This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and ground.

logic symbol†



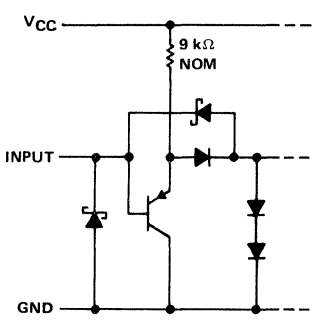
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs.
◈ Designates passive-pullup outputs.

logic diagram (positive logic)

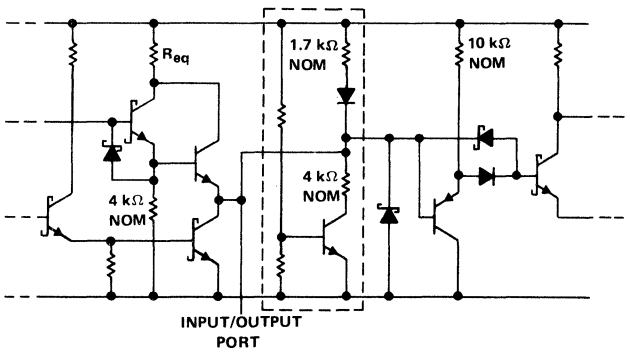


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
DW package . . . . . 1025 mW
J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the DW and J packages to 656 mW at 70°C at the rate of 8.2 mW/°C and derate the N package to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			−5.2	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = −800 μA,	TE at 0.8 V	2.7	3.5		V
		Bus	I_{OH} = −5.2 mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	TE at 2 V		0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal,	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current	PE, or TE	V_I = 0.5 V			−10	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			2.5	
							−3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 to 2.5 V			40	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load	Terminal outputs low and enabled		42	65	mA
				Bus outputs low and enabled		52	80	
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{OH} applies to 3-state outputs only.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), V_{CC} = 5 V

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		7	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					8	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		7	14	ns
t_{PHL}	Propagation delay time, high-to-low-level output					9	14	
t_{PZH}	Output enable time to high level	TE	Bus	C_L = 15 pF, See Figure 3		19	30	ns
t_{PHZ}	Output disable time from high level					5	12	
t_{PZL}	Output enable time to low level					16	35	
t_{PLZ}	Output disable time from low level					9	20	
t_{PZH}	Output enable time to high level	TE	Terminal	C_L = 15 pF, See Figure 4		13	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level					12	20	
t_{PLZ}	Output disable time from low level					11	20	
t_{en}	Output pull-up enable time	PE	Bus	C_L = 15 pF, See Figure 5		11	22	ns
t_{dis}	Output pull-up disable time					6	12	

†Typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

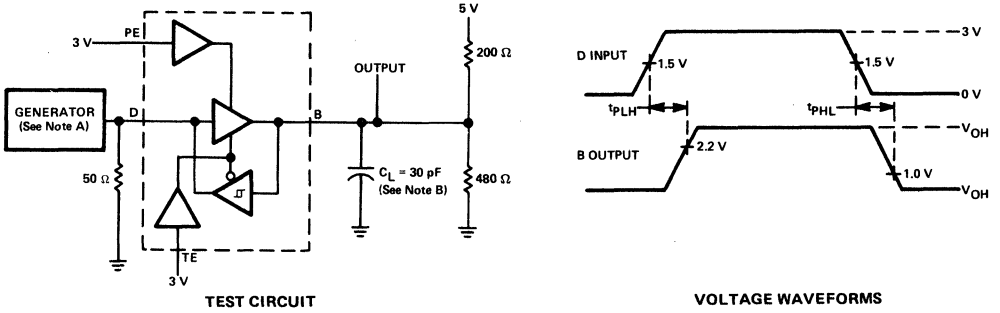


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

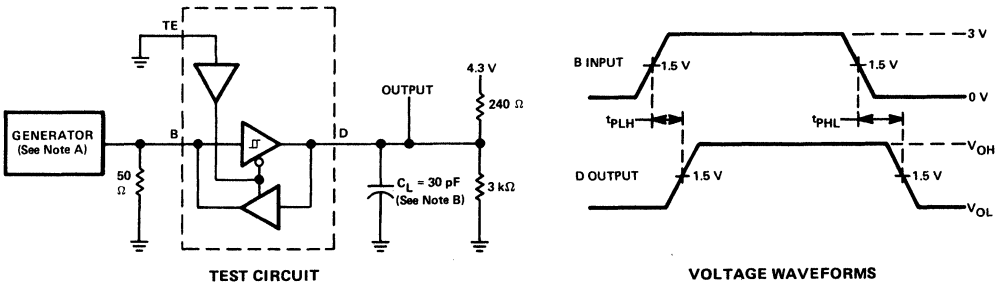


FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

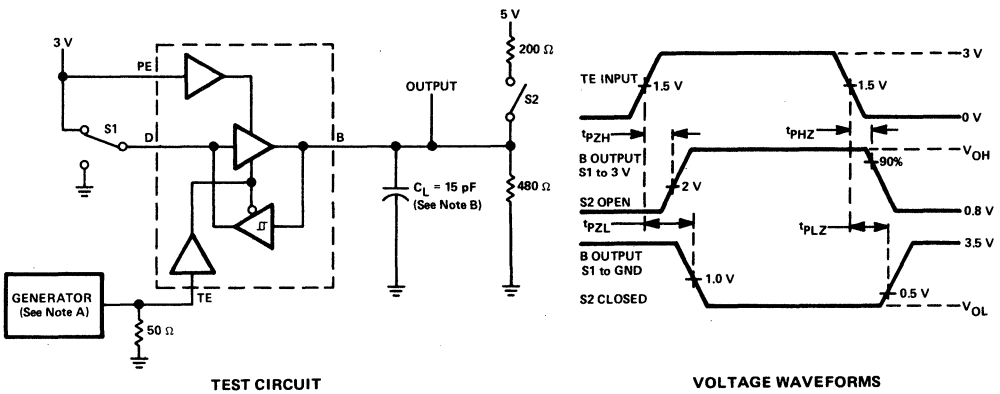


FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

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PARAMETER MEASUREMENT INFORMATION

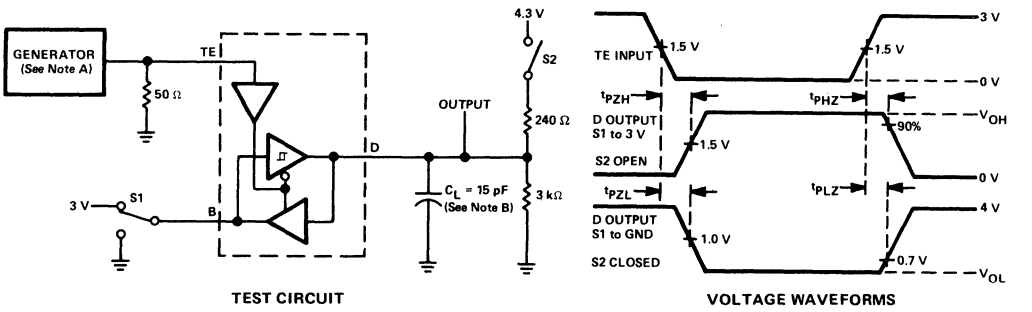


FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES

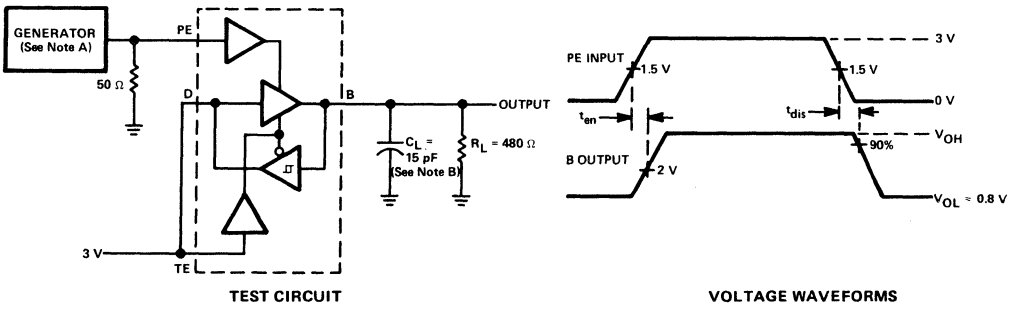


FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

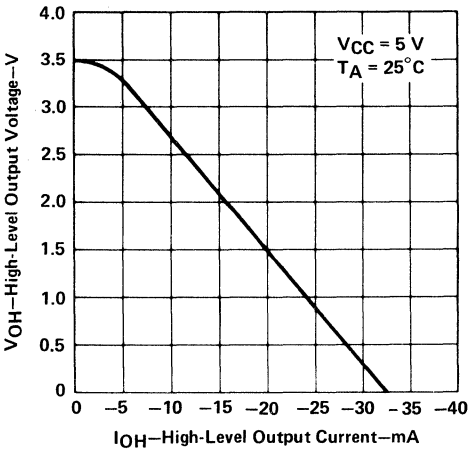


FIGURE 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

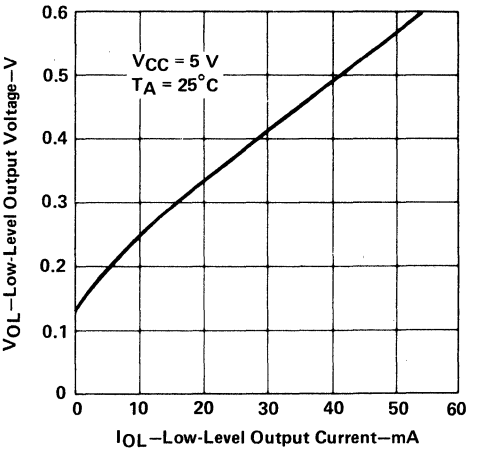


FIGURE 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

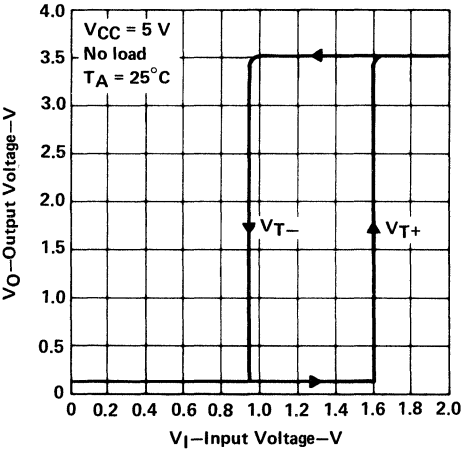


FIGURE 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

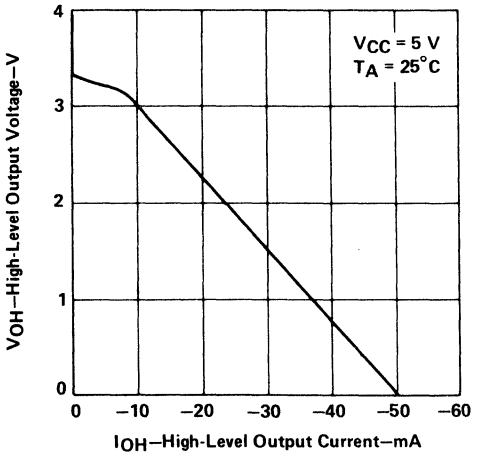


FIGURE 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

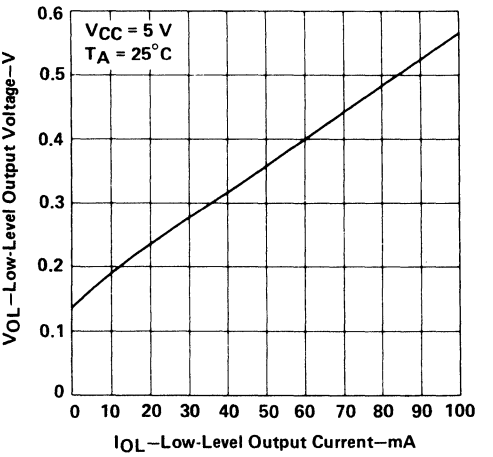


FIGURE 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

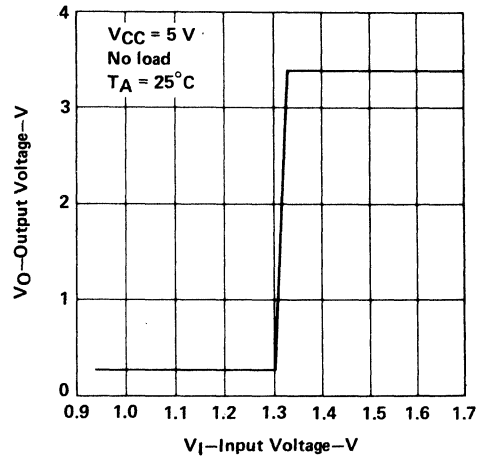


FIGURE 11

BUS CURRENT
vs
BUS VOLTAGE

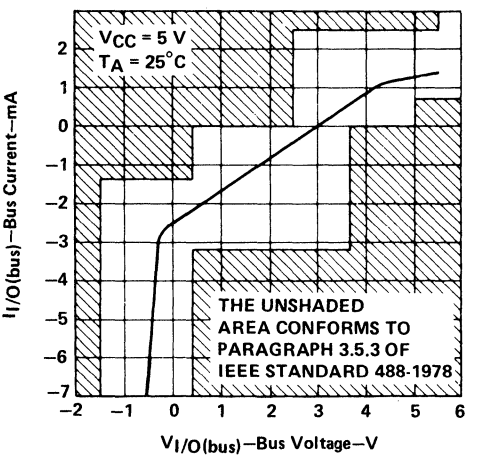


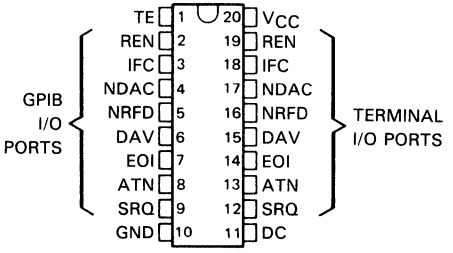
FIGURE 12

D2618, JUNE 1986—REVISED AUGUST 1989

MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- Designed to Implement Control Bus Interface
- Designed for Single Controller
- High-Speed Advanced Low-Power Schottky Circuitry
- Low-Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

DW, J, OR N PACKAGE
(TOP VIEW)



CHANNEL IDENTIFICATION TABLE

NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End or Identify	
DAV	Data Valid	Data Transfer
NDAC	Not Data Accepted	
NRFD	Not Ready for Data	

description

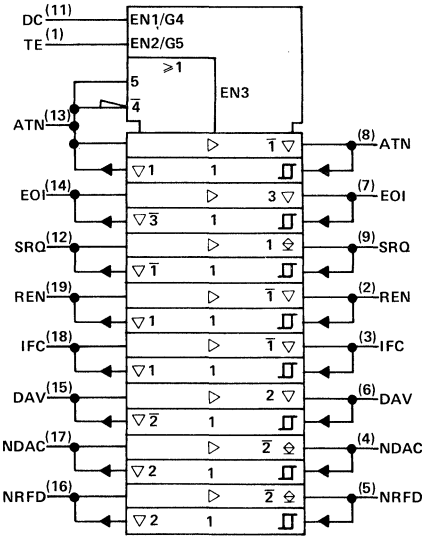
The SN75ALS161 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky process device designed to provide the bus-management and data-transfer signals between operating units of a single controller instrumentation system. When combined with the SN75ALS160 octal bus transceiver, the SN75ALS161 provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS161 features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the DC and TE enable signals.

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when V_{CC} = 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features p-n-p transistor inputs for high input impedance and hysteresis of 400 mV minimum for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

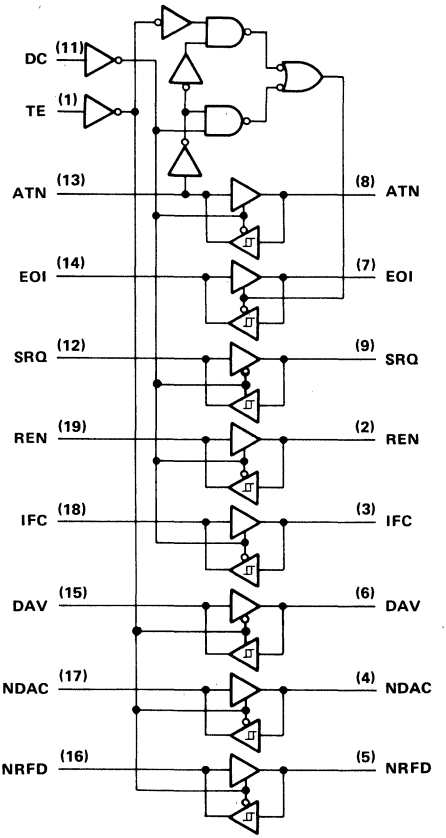
The SN75ALS161 is manufactured in a 20-pin package and is characterized for operation from 0 °C to 70 °C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs.
⏀ Designates passive-pullup outputs.

logic diagram (positive logic)



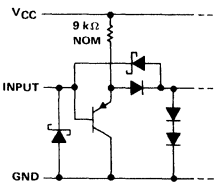
RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS			BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
DC	TE	ATN‡	ATN‡	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
			(Controlled by DC)					(Controlled by TE)		
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

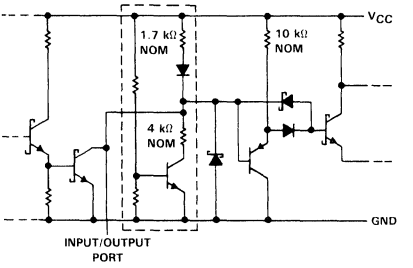
H = high level, L = low level, R = receive, T = transmit, X = irrelevant
Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.
‡ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

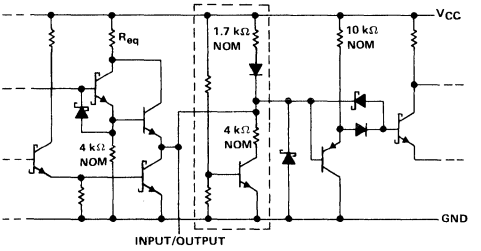


TYPICAL OF SRQ, NDAC, and NRFD GPIB I/O PORT



Circuit inside dashed lines is on the driver outputs only.

TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, and NRFD GPIB I/O PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
- DW package . . . . . 1025 mW
- J package . . . . . 1025 mW
- N package . . . . . 1150 mW

Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the DW and J packages to 656 mW at 70°C at the rate of 8.2 mW/°C, and derate the N package to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			−5.2	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = −800 μA		2.7	3.5		V
		Bus	I_{OH} = −5.2 mA		2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA			0.3	0.5	V
		Bus	I_{OL} = 48 mA			0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal and control inputs	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current		V_I = 0.5 V			−10	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 to 2.5 V			40	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load, TE and DC low			55	75	mA
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{OH} applies to 3-state outputs only.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), V_{CC} = 5 V

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					12	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		5	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output					7	14	
t_{PZH}	Output enable time to high level	TE or DC	BUS (ATTN, EOI, REN, IFC, and DAV)	C_L = 15 pF, See Figure 3			30	ns
t_{PHZ}	Output disable time from high level						20	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						20	
t_{PZH}	Output enable time to high level	TE or DC	Terminal	C_L = 15 pF, See Figure 4			30	ns
t_{PHZ}	Output disable time from high level						25	
t_{PZL}	Output enable time to low level						30	
t_{PLZ}	Output disable time from low level						25	

†All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

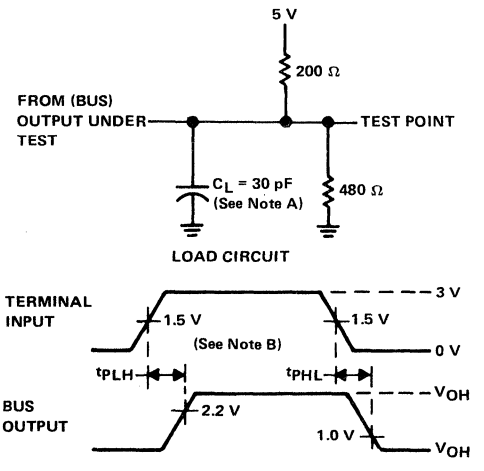


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

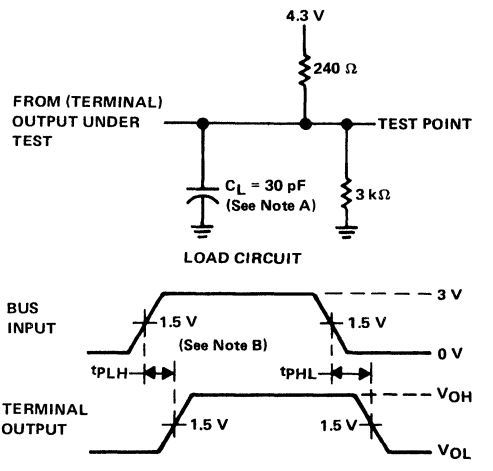
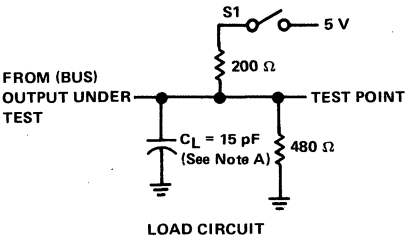


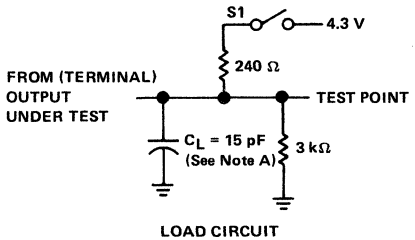
FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.

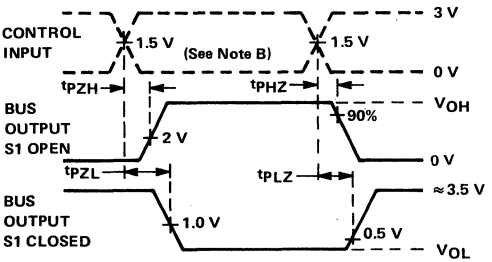
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

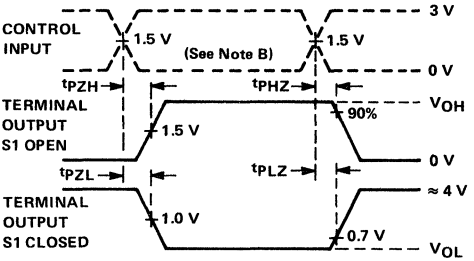


LOAD CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3. BUS ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS

FIGURE 4. TERMINAL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

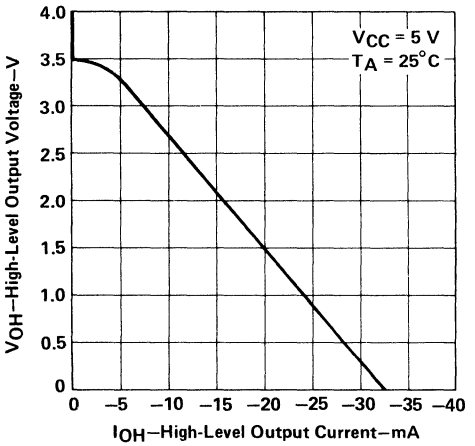


FIGURE 5

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

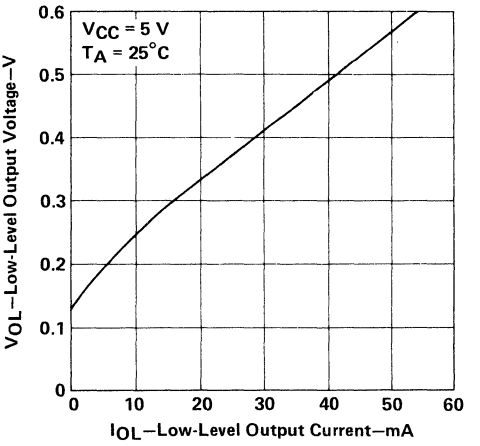


FIGURE 6

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

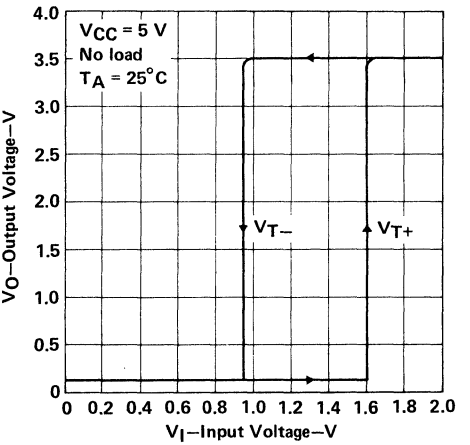


FIGURE 7

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

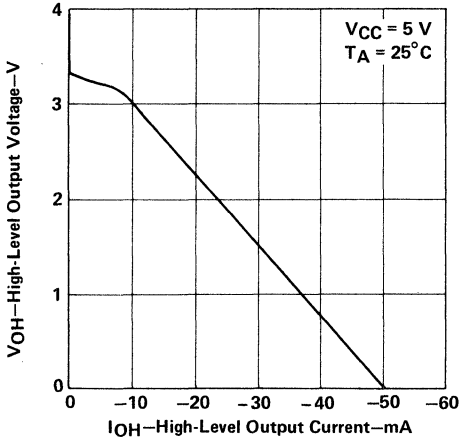


FIGURE 8

BUS-LOW LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

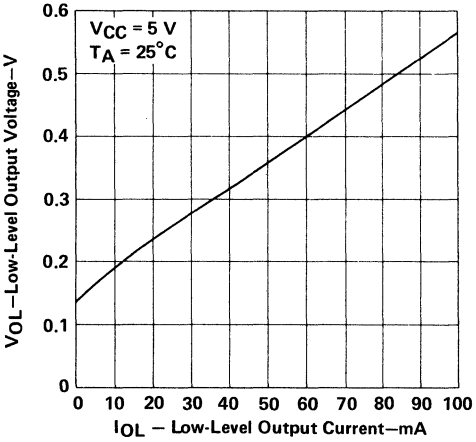


FIGURE 9

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

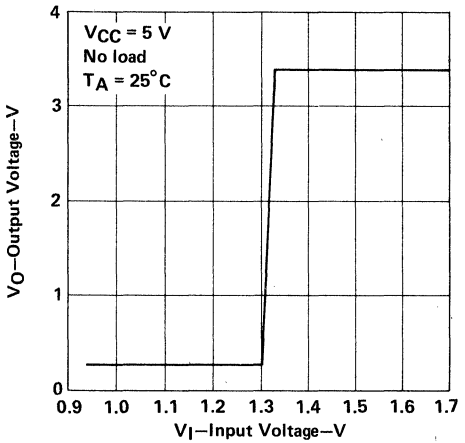


FIGURE 10

BUS CURRENT
vs
BUS VOLTAGE

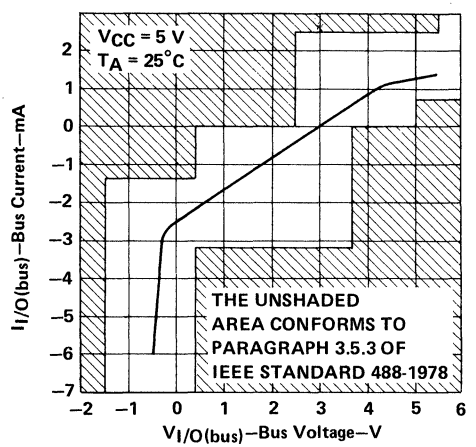


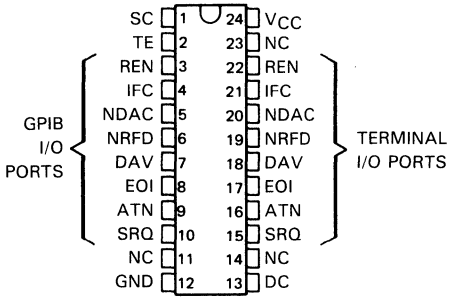
FIGURE 11

D2618, JUNE 1986—REVISED AUGUST 1989

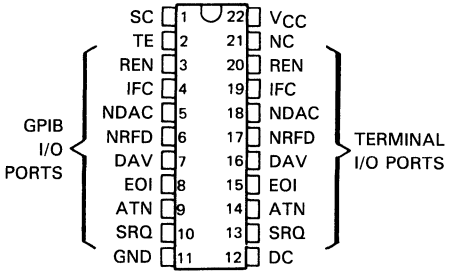
MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- Designed to Implement Control Bus Interface
- Designed for Multicontrollers
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

DW PACKAGE
(TOP VIEW)



N PACKAGE
(TOP VIEW)



NC—No internal connection.

description

The SN75ALS162 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky process device designed to provide the bus-management and data-transfer signals between operating units of a multiple-controller instrumentation system. When combined with the SN75ALS160 octal bus transceiver, the SN75ALS162 provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS162 features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the DC, TE, and SC enable signals. The SC input allows the REN and IFC transceivers to be controlled independently.

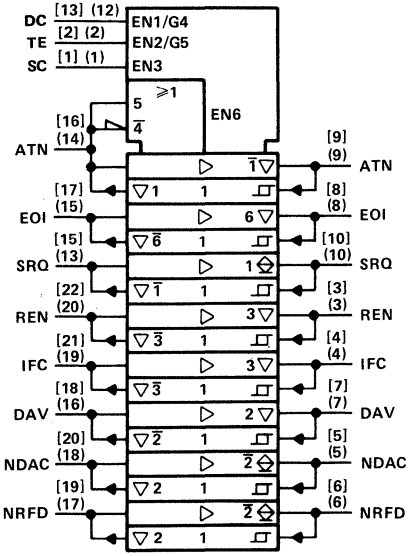
The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when V_{CC} = 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features p-n-p transistor inputs for high input impedance and hysteresis of 400 mV minimum for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

The SN75ALS162 is manufactured in a 22-pin dual-in-line N package and in 24-pin DW package, and is characterized for operation from 0°C to 70°C.

CHANNEL IDENTIFICATION TABLE

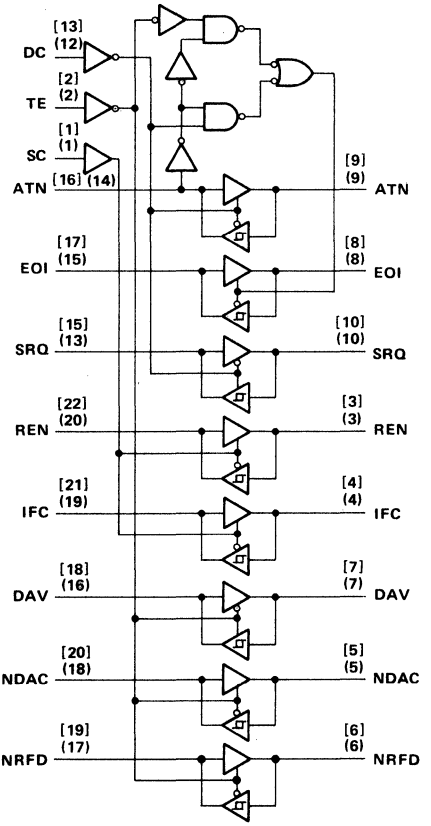
NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
SC	System Control	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End or Identify	
DAV	Data Valid	Data Transfer
NDAC	Not Data Accepted	
NRFD	Not Ready for Data	

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs.
⏀ Designates passive-pullup outputs.

logic diagram (positive logic)



[ ] Denotes pin numbers for DW package.
( ) Denotes pin numbers for N package.

RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS				BUS-MANAGEMENT CHANNELS				DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN† (Controlled by DC)	SRQ (Controlled by DC)	REN (Controlled by SC)	IFC (Controlled by SC)	EOI	DAV (Controlled by TE)	NDAC (Controlled by TE)	NRFD (Controlled by TE)
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

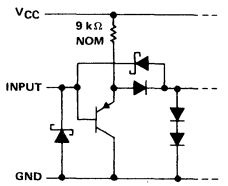
H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

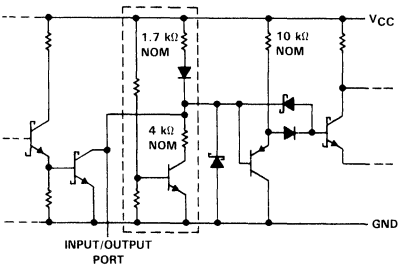
†ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

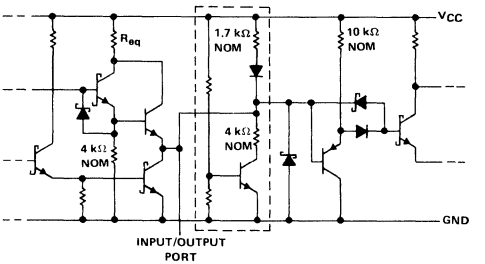


TYPICAL OF SRQ, NDAC, and NRFD GPIB I/O PORT



Circuit inside dashed lines is on the driver outputs only.

TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, and NRFD GPIB I/O PORTS



Driver output R_{eq} = 30 Ω NOM

Receiver output R_{eq} = 110 Ω NOM

Circuit inside dashed lines is on the driver outputs only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
DW package . . . . . 1350 mW
N package . . . . . 1700 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the DW package to 864 mW at 70°C at the rate of 10.8 mW/°C, and derate the N package to 1088 mW at 70°C at the rate of 13.6 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with 3-state outputs			−5.2	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = −800 μA		2.7	3.5		V
		Bus	I_{OH} = −5.2 mA		2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA			0.3	0.5	V
		Bus	I_{OL} = 48 mA			0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal and control inputs	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current		V_I = 0.5 V			−10	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 to 2.5 V			−40	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load,	TE, DC, and SC low		55	75	mA
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡V_{OH} applies for 3-state outputs only.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), V_{CC} = 5 V

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					12	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		5	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output					7	14	
t_{PZH}	Output enable time to high level	TE, DC, or SC	BUS (ATTN, EOI, REN, IFC, and DAV)	C_L = 15 pF, See Figure 3			30	ns
t_{PHZ}	Output disable time from high level						20	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						20	
t_{PZH}	Output enable time to high level	TE, DC, or SC	Terminal	C_L = 15 pF, See Figure 4			30	ns
t_{PHZ}	Output disable time from high level						25	
t_{PZL}	Output enable time to low level						30	
t_{PLZ}	Output disable time from low level						25	

†All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

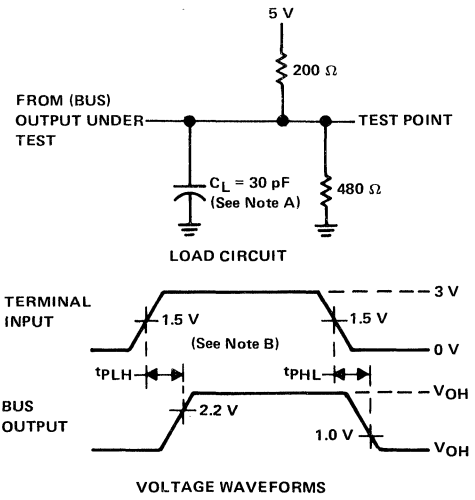


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

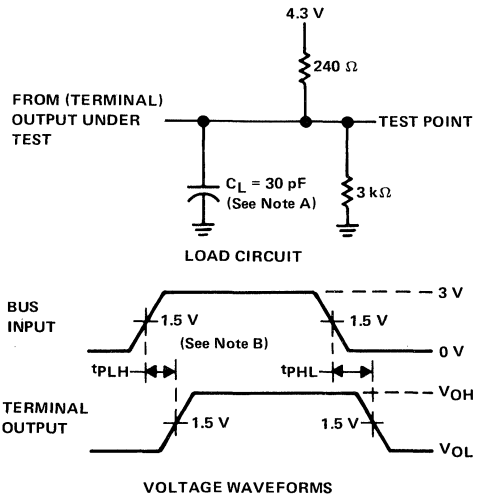
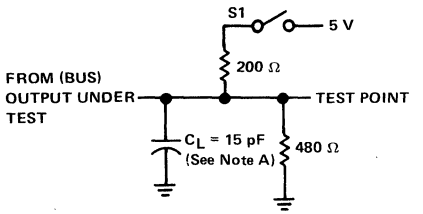


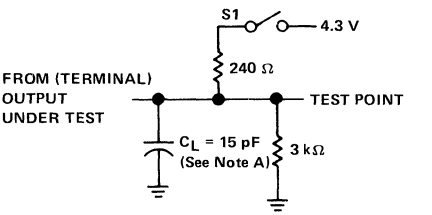
FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.

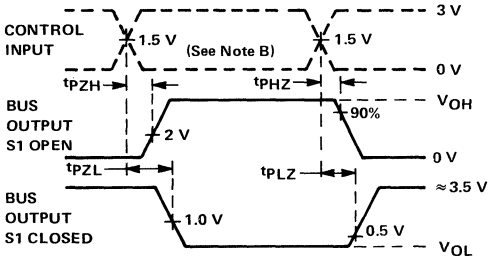
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

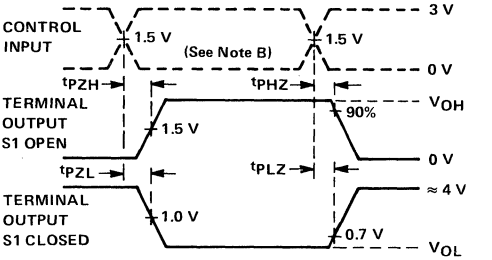


LOAD CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3. BUS ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS

FIGURE 4. TERMINAL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

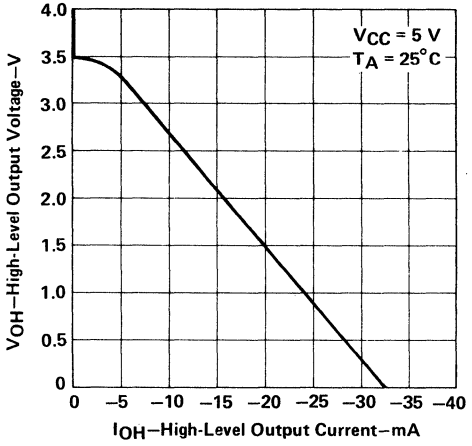


FIGURE 5

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

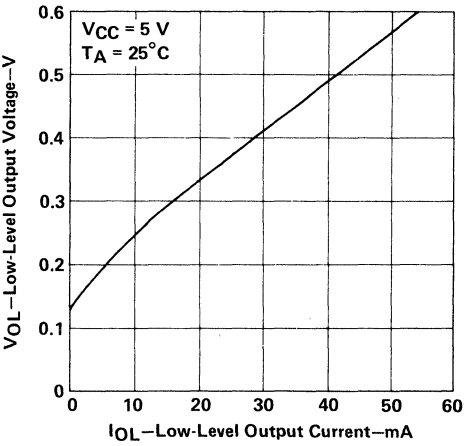


FIGURE 6

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

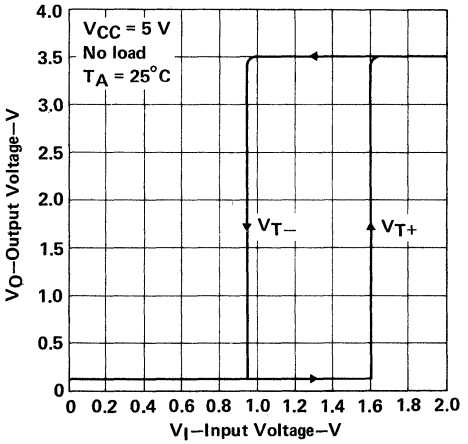


FIGURE 7

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

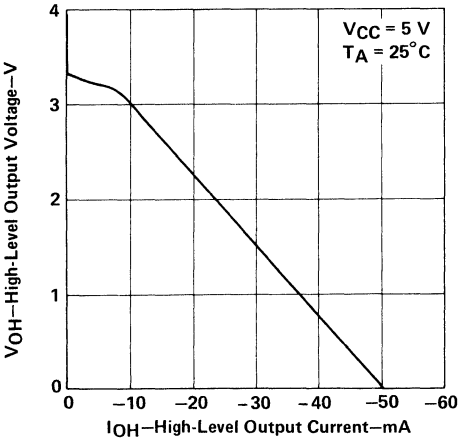


FIGURE 8

BUS-LOW LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

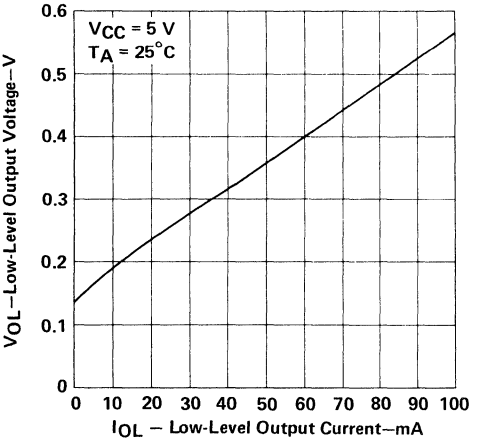


FIGURE 9

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

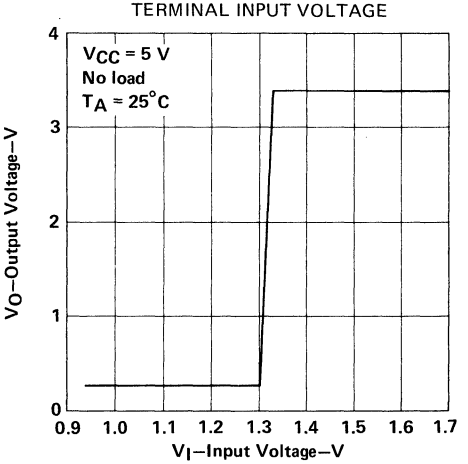


FIGURE 10

BUS CURRENT
vs
BUS VOLTAGE

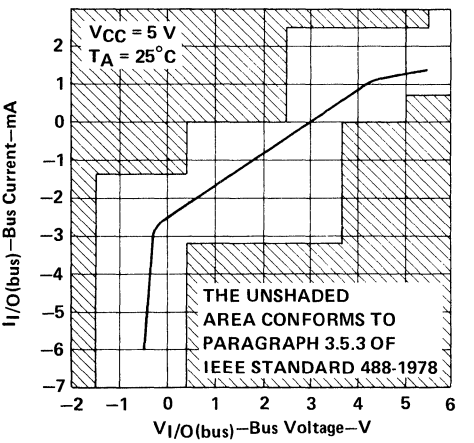
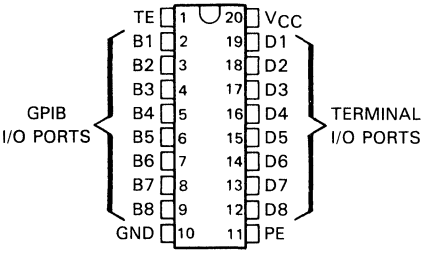


FIGURE 11

D2611, JUNE 1986—REVISED SEPTEMBER 1989

- **8-Channel Bidirectional Transceivers**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Low Power Dissipation . . . 46 mW Max per Channel**
- **Fast Propagation Times . . . 20 ns Max**
- **High-Impedance P-N-P Inputs**
- **Receiver Hysteresis . . . 650 mV Typ**
- **Open-Collector Driver Output Option**
- **No Loading of Bus When Device Is Powered Down (V_{CC} = 0)**
- **Power-Up/Power-Down Protection (Glitch-Free)**

DW, J, OR N PACKAGE
(TOP VIEW)



description

The SN75ALS163 octal general-purpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky device. It is designed for two-way data communications over single-ended transmission lines. The transceiver features driver outputs that can be operated in either the open-collector or 3-state mode. If Talk Enable (TE) is high, these outputs have the characteristics of open-collector outputs when Pullup Enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places the outputs in the high-impedance state. The driver outputs are designed to handle loads of up to 48 mA of sink current. Each receiver features p-n-p transistor inputs for high input impedance and 400 mV minimum of hysteresis for increased noise immunity.

Output glitches during power-up and power-down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when V_{CC} = 0.

The SN75ALS163 is characterized for operation from 0°C to 70°C.

FUNCTION TABLES

EACH DRIVER

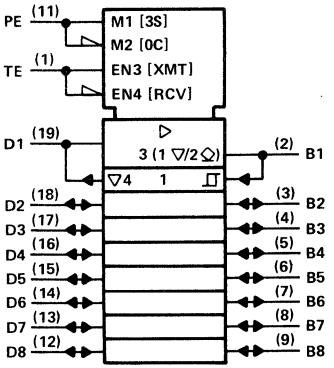
INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z
X	L	X	Z

EACH RECEIVER

INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

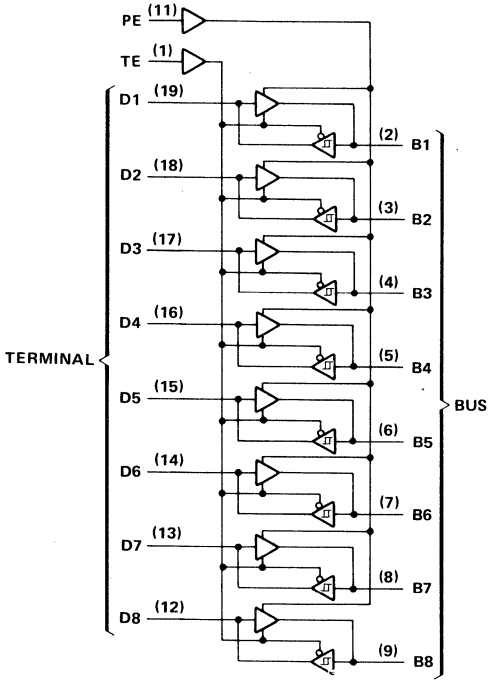
H = high level, L = low level, X = irrelevant, Z = High-impedance state.

logic symbol†



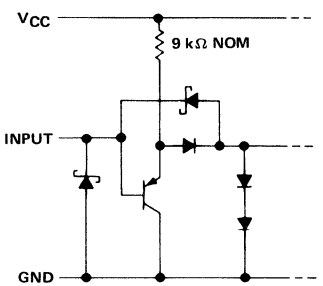
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs.
◇ Designates open-collector outputs.

logic diagram (positive logic)

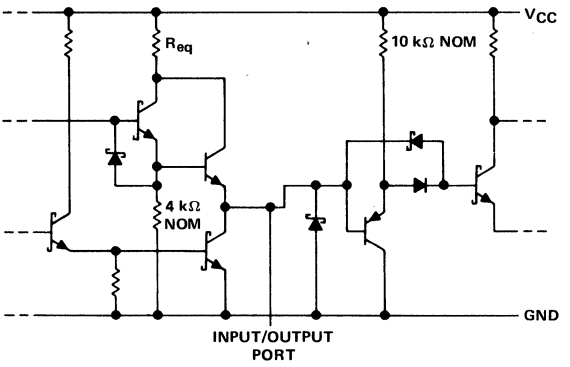


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package . . . . 260°C

NOTE: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			−5.2	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature range, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = −800 μA,	TE at 0.8 V	2.7	3.5		V
		Bus	I_{OH} = −5.2 mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	TE at 2 V		0.35	0.5	
I_{OH}	High-level output current (open-collector mode)	Bus	V_O = 5.5 V, D and TE at 2 V	PE at 0.8 V,			100	μA
I_{OZ}	Off-state output current (3-state mode)	Bus	PE at 2 V, TE at 0.8 V	V_O = 2.7 V			20	μA
				V_O = 0.5 V			−100	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal,	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current	PE, or TE	V_I = 0.5 V			−10	−100	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load	Terminal outputs low and enabled		42	65	mA
				Bus outputs low and enabled		52	80	
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V or 0, f = 1 MHz	$V_{I/O}$ = 0 to 2 V,		30		pF

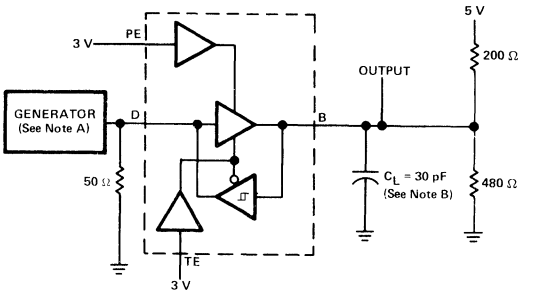
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), V_{CC} = 5 V

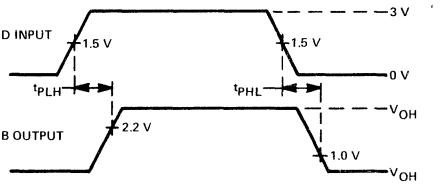
PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP§	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		7	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					8	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		7	14	ns
t_{PHL}	Propagation delay time, high-to-low-level output					9	14	
t_{PZH}	Output enable time to high level	TE	Bus	C_L = 15 pF, See Figure 3		19	30	ns
t_{PHZ}	Output disable time from high level					5	12	
t_{PZL}	Output enable time to low level					16	35	
t_{PLZ}	Output disable time from low level					9	20	
t_{PZH}	Output enable time to high level	TE	Terminal	C_L = 15 pF, See Figure 4		13	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level					12	20	
t_{PLZ}	Output disable time from low level					11	20	
t_{en}	Output pull-up enable time	PE	Bus	C_L = 15 pF, See Figure 5		11	22	ns
t_{dis}	Output pull-up disable time					6	12	

§All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

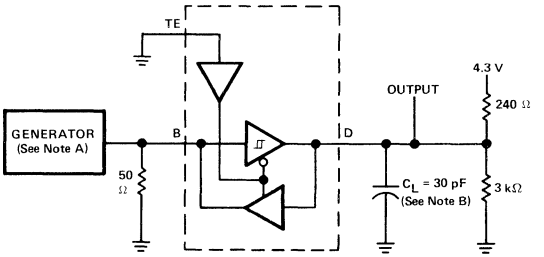


TEST CIRCUIT

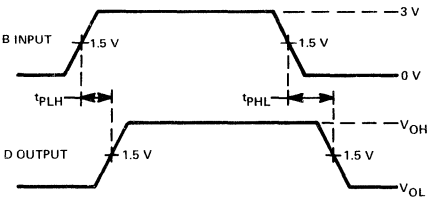


VOLTAGE WAVEFORMS

FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

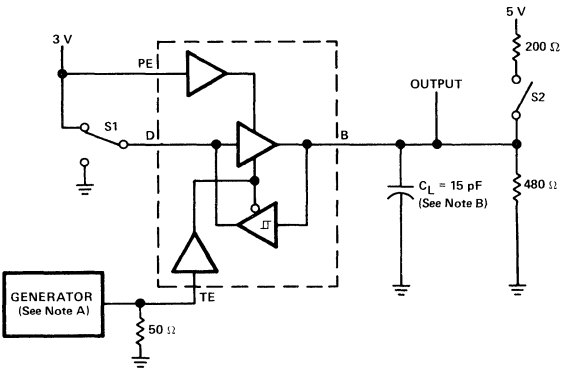


TEST CIRCUIT

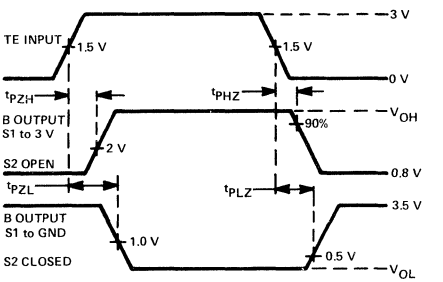


VOLTAGE WAVEFORMS

FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

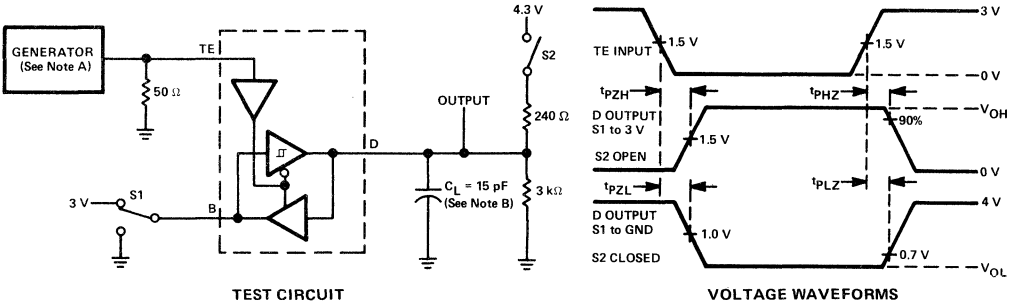


FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES

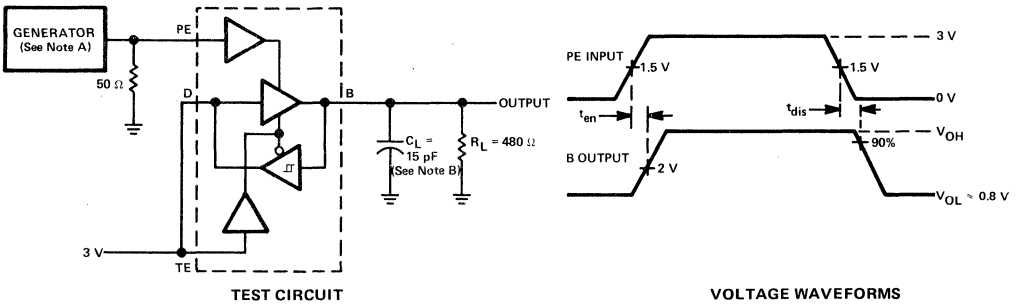


FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

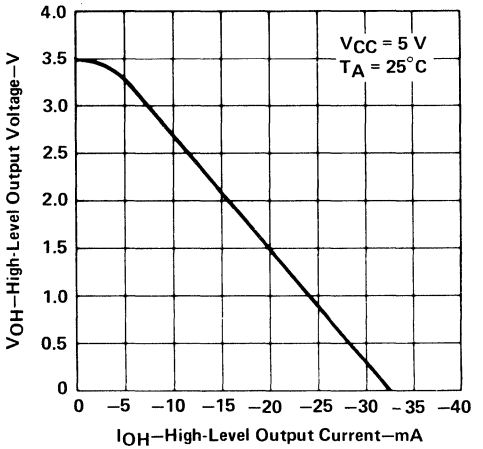


FIGURE 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

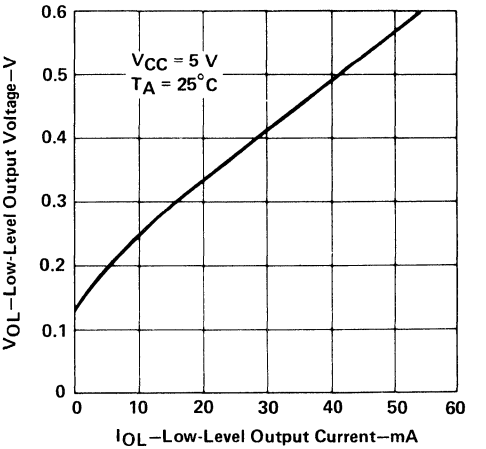


FIGURE 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

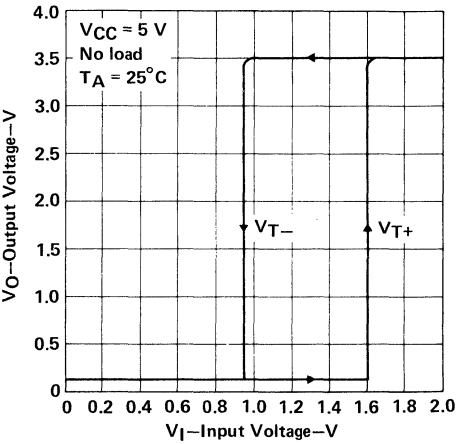


FIGURE 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

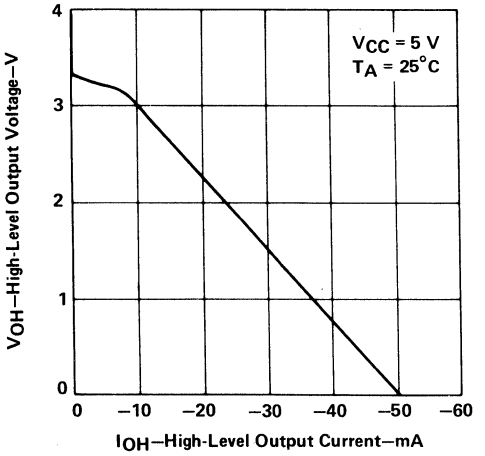


FIGURE 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

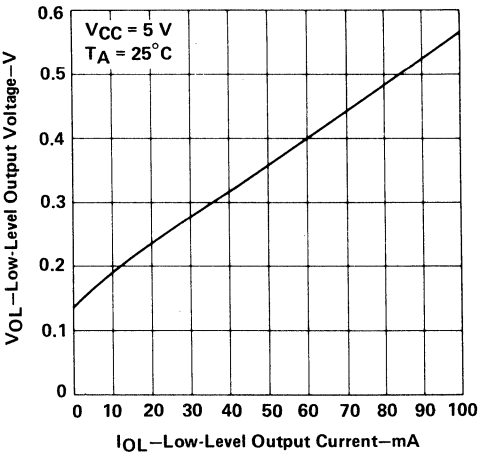


FIGURE 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

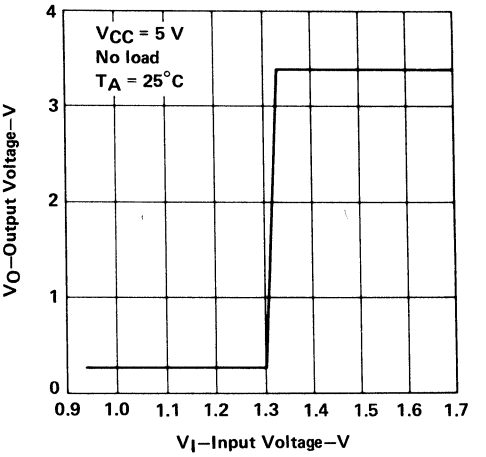
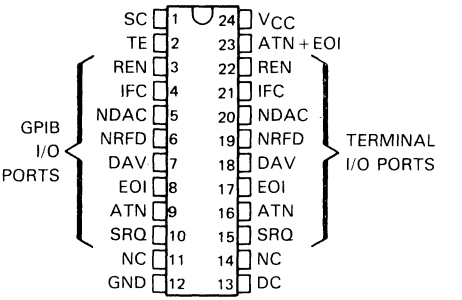


FIGURE 11

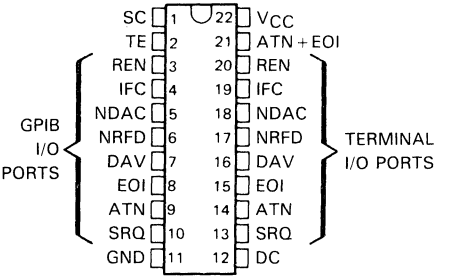
D2908, JUNE 1986—REVISED AUGUST 1989

- 8-Channel Bidirectional Transceiver
- Designed to Implement Control Bus Interface
- Designed for Multicontrollers
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

DW PACKAGE
(TOP VIEW)



N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection.

description

The SN75ALS164 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky device designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a multiple-controller instrumentation system. When combined with the SN75ALS160 octal bus transceiver, the SN75ALS164 provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS164 features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. All outputs are disabled (at a high-impedance state) during V_{CC} power-up and power-down transitions for glitch-free operation. The direction of data flow through these driver-receiver pairs is determined by the DC, TE, and SC enable signals. The SN75ALS164 is identical to the SN75ALS162 with the addition of an OR gate to help simplify board layouts in several popular applications. The ATN and EOI signals are ORed to pin 21, which is a standard totem-pole output.

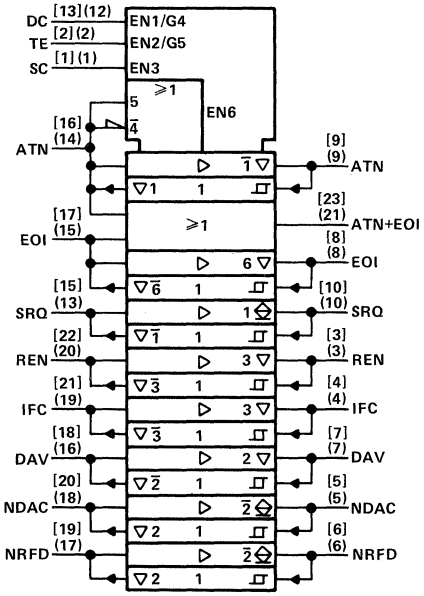
CHANNEL IDENTIFICATION TABLE

NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
SC	System Control	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End or Identify	
ATN + EOI	ATN logical OR EOI	Logic
DAV	Data Valid	Data Transfer
NDAC	Not Data Accepted	
NRFD	Not Ready for Data	

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when supply voltage V_{CC} is 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features p-n-p transistor inputs for high input impedance and hysteresis of 400 mV minimum for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

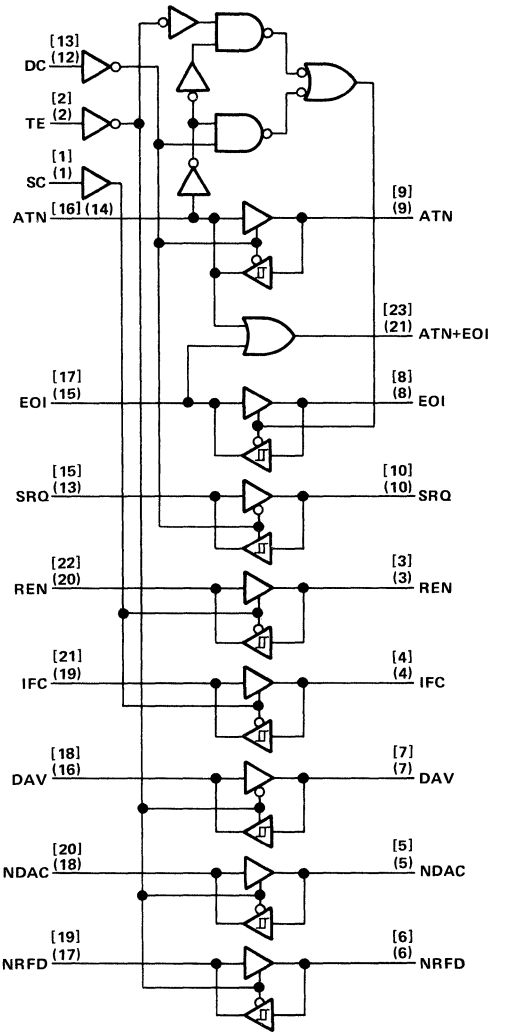
The SN75ALS164 is manufactured in a 22-pin dual-in-line N package and in 24-pin DW package, and is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽Designates 3-state outputs.
⏀ Designates passive-pullup outputs.

logic diagram (positive logic)



[ ] Denotes pin numbers for DW package.
( ) Denotes pin numbers for N package.

RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS				BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN† (Controlled by DC)	SRQ (Controlled by DC)	REN (Controlled by SC)	IFC (Controlled by SC)	EOI	DAV (Controlled by TE)	NDAC (Controlled by TE)	NRFD (Controlled by TE)
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

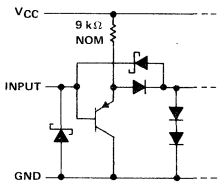
H = high level, L = low level, R = receive, T = transmit, X = irrelevant
Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.
†ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

ATN + EOI FUNCTION TABLE

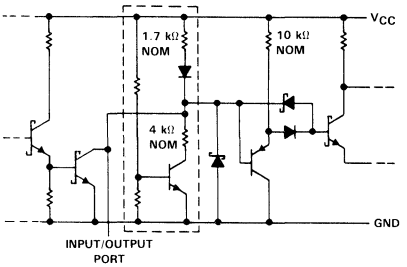
INPUTS		OUTPUT
ATN	EOI	ATN + EOI
H	X	H
X	H	H
L	L	L

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

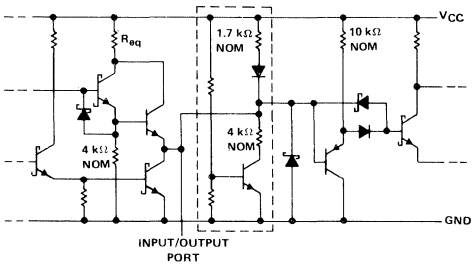


TYPICAL OF SRQ, NDAC, and NRFD GPIB I/O PORT



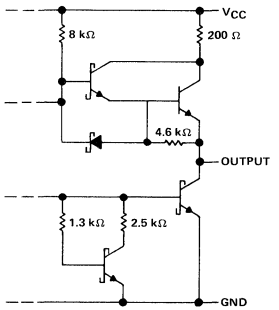
Circuit inside dashed lines is on GPIB I/O ports only.

TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, and NRFD GPIB I/O PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on GPIB I/O ports only.

ATN+EOI OUTPUT



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
DW package . . . . . 1350 mW
N package . . . . . 1700 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 10 seconds: DW or N package . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the DW package to 864 mW at 70°C at the rate of 10.8 mW/°C, and derate the N package to 1088 mW at 70°C at the rate of 13.6 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with 3-state outputs			−5.2	mA
	Terminal ports			−800	μA
	ATN + EOI			−400	
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
	ATN + EOI			4	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = −800 μA		2.7	3.5		V
		Bus	I_{OH} = −5.2 mA		2.5	3.3		
		ATN + EOI	I_{OH} = −400 μA		2.7			
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA			0.3	0.5	V
		Bus	I_{OL} = 48 mA			0.35	0.5	
		ATN + EOI	I_{OL} = 4 mA				0.4	
I_I	Input current at maximum input voltage	Terminal§	V_I = 5.5 V			0.2	100	μA
		ATN, EOI	V_I = 5.5 V				200	
I_{IH}	High-level input current	Terminal control	V_I = 2.7 V			0.1	20	μA
		ATN, EOI	V_I = 2.7 V				40	
I_{IL}	Low-level input current	Terminal control	V_I = 0.5 V			−10	−100	μA
		ATN, EOI	V_I = 0.5 V				−500	
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 to 2.5 V			−40	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
		ATN + EOI			−10		−100	
I_{CC}	Supply current		No load, TE, DC, and SC low			55	75	mA
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{OH} applies for 3-state outputs only.
§ Except ATN and EOI terminal pins.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), V_{CC} = 5 V

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					12	20	
t_{PLH}	Propagation delay time low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		5	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output					7	14	
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal ATN or Terminal EOI	ATN+EOI	C_L = 15 pF, See Figure 3		3.5	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output	Terminal ATN or Terminal EOI	ATN+EOI	C_L = 15 pF, See Figure 3		7	15	ns
t_{PZH}	Output enable time to high level	TE, DC, or SC	BUS (ATTN, EOI, REN, IFC, and DAV)	C_L = 15 pF, See Figure 4			30	ns
t_{PHZ}	Output disable time from high level						20	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						20	
t_{PZH}	Output enable time to high level	TE, DC, or SC	Terminal	C_L = 15 pF, See Figure 5			30	ns
t_{PHZ}	Output disable time from high level						25	
t_{PZL}	Output enable time to low level						30	
t_{PLZ}	Output disable time from low level						25	

PARAMETER MEASUREMENT INFORMATION

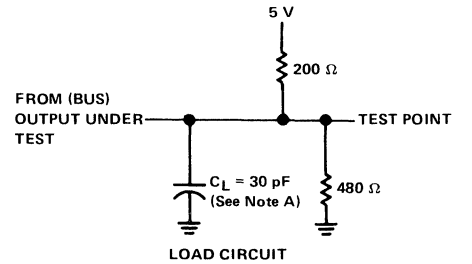


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

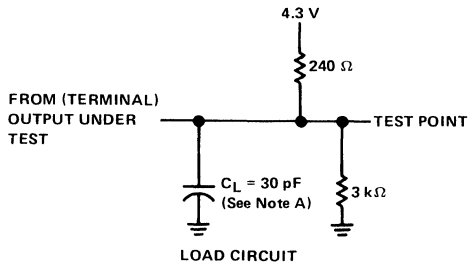
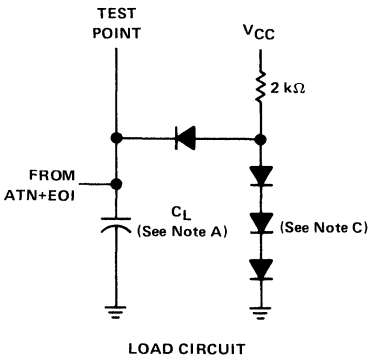


FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES



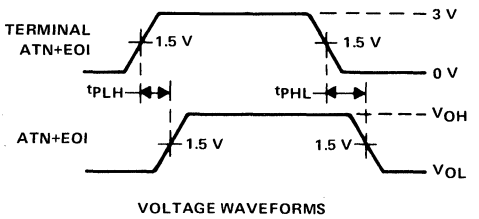
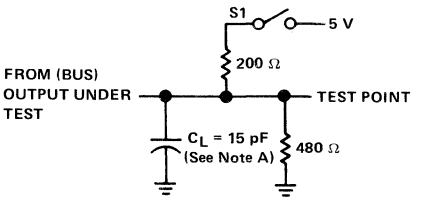


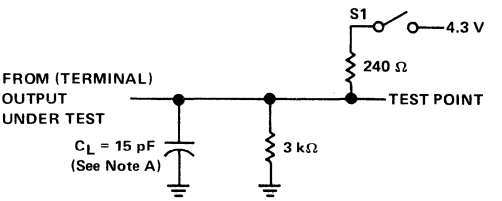
FIGURE 3. ATN + EOI PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.
C. All diodes are 1N916 or 1N3064.

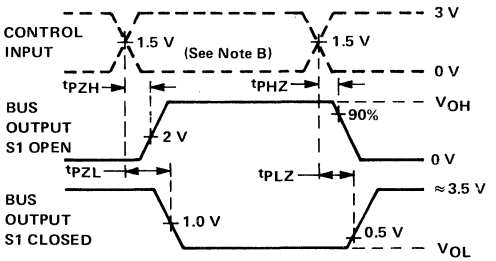
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

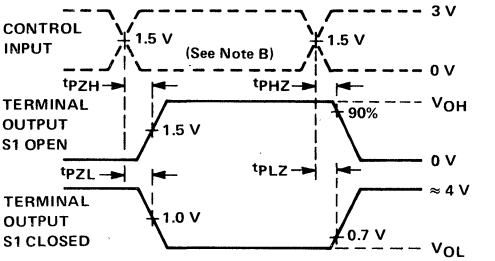


LOAD CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4. BUS ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS

FIGURE 5. TERMINAL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤6 ns, t_f ≤6 ns, Z_{out} = 50 Ω.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

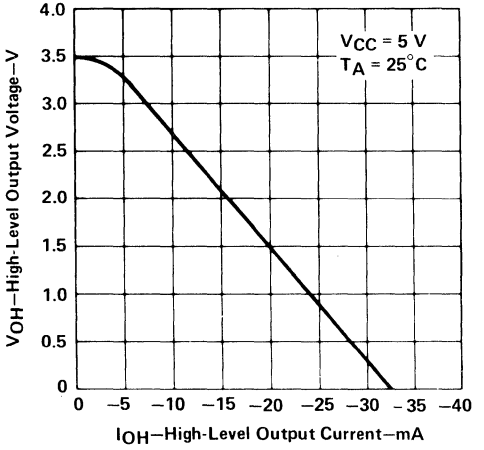


FIGURE 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

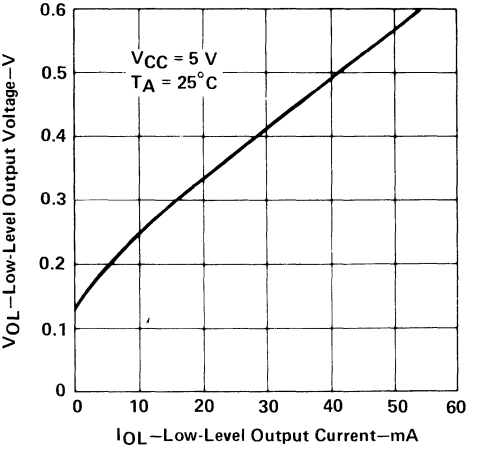


FIGURE 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

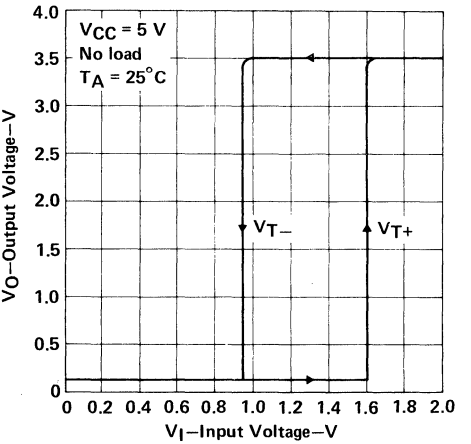


FIGURE 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

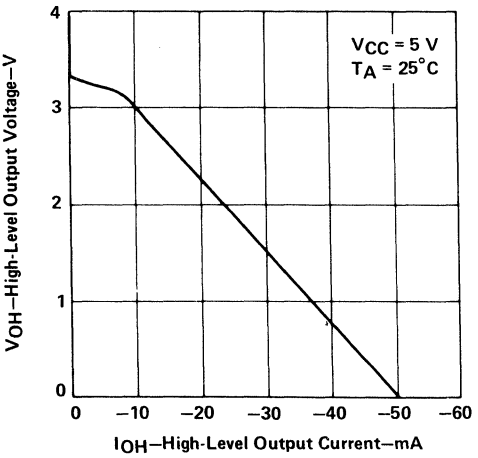


FIGURE 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

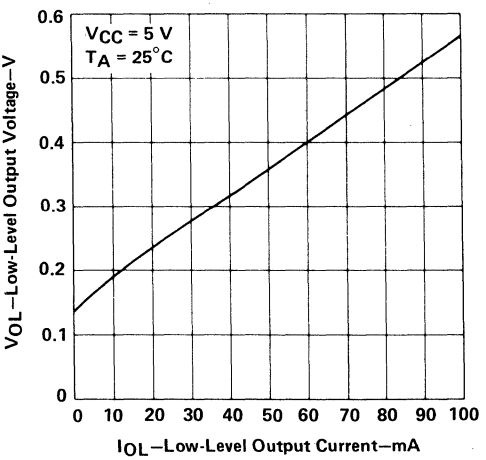


FIGURE 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

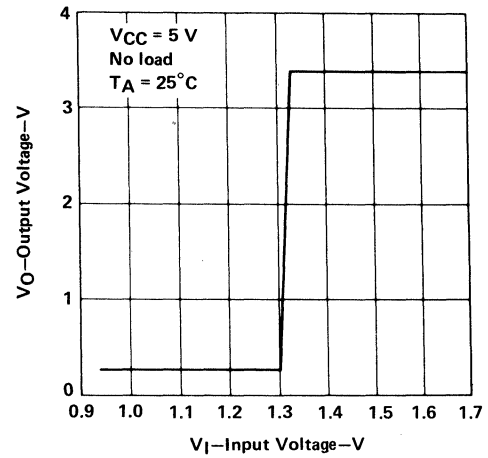


FIGURE 11

BUS CURRENT
vs
BUS VOLTAGE

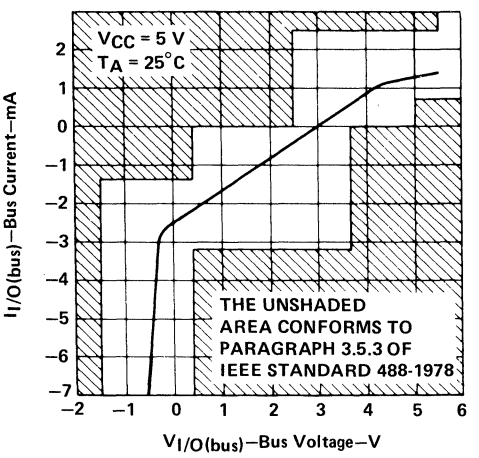


FIGURE 12

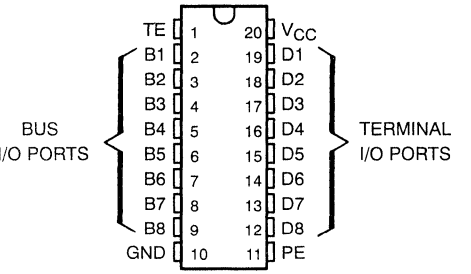
SN75ALS165
OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

D3011, JUNE 1986—REVISED AUGUST 1989

MEETS IEEE STANDARD 488-1978 (GPIB)

- **8-Channel Bidirectional Transceiver**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Low Power Dissipation . . . 46 mW Max per Channel**
- **Fast Propagation Times . . . 20 ns Max**
- **High-Impedance P-N-P Inputs**
- **Receiver Hysteresis . . . 650 mV Typ**
- **No Loading of Bus When Device Is Powered Down (V_{CC} = 0)**
- **Power-Up/Power-Down Protection (Glitch-Free)**
- **Driver and Receiver Can Be Disabled Simultaneously**

DW OR N PACKAGE
(TOP VIEW)



description

The SN75ALS165 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky device designed for two-way data communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the passive-pullup or 3-state mode. If Talk Enable (TE) is high, these ports have the characteristics of passive-pullup outputs when Pullup Enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. Taking TE and PE low places both the drivers and receivers in the high-impedance state. The driver outputs are designed to handle loads up to 48 mA of sink current.

FUNCTION TABLES

EACH DRIVER

INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z†
X	L	X	Z†

EACH RECEIVER

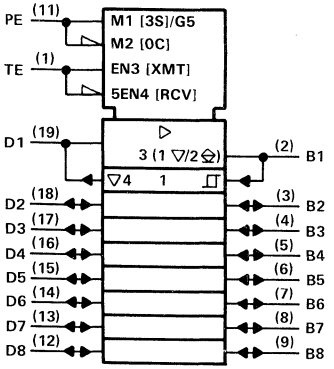
INPUTS			OUTPUT
B	TE	PE	D
L	L	H	L
H	L	H	H
X	H	X	Z
X	X	L	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance state
† This is the high impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and ground.

An active turn-off feature is incorporated into the bus-terminating resistors so that the device exhibits a high impedance to the bus when V_{CC} = 0. When combined with the SN75ALS161 or SN75ALS162 management bus transceiver, the pair provides the complete 16-wire interface for the IEEE 488 bus.

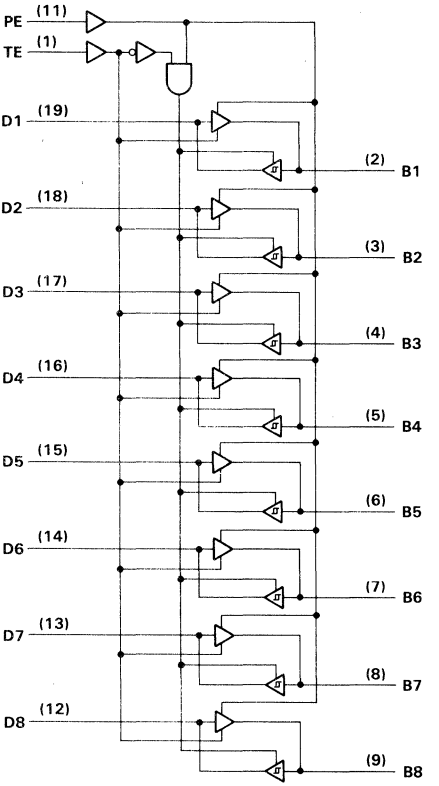
The SN75ALS165 is manufactured in a 20-pin package and is characterized for operation from 0°C to 70°C.

logic symbol†



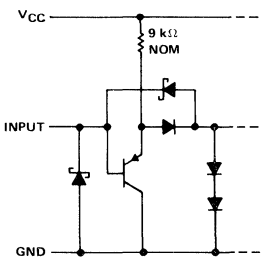
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs
◇ Designates passive-pullup outputs

logic diagram (positive logic)

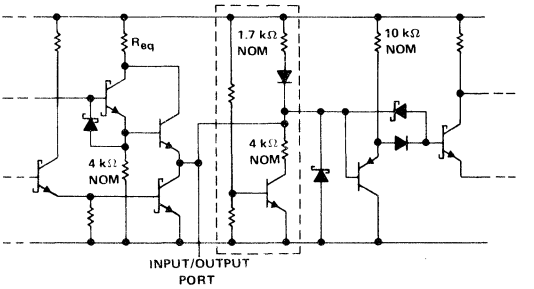


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage ..... 5.5 V
Low-level driver output current ..... 100 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			−5.2	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = −800 μA,	TE at 0.8 V	2.7	3.5		V
		Bus	I_{OH} = −5.2 mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	TE at 2 V		0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal and control inputs	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current		V_I = 0.5 V			−10	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0 ,	$V_{I(bus)}$ = 0 to 2.5 V			40	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load	Terminal outputs low and enabled		42	65	mA
				Bus outputs low and enabled		52	80	
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0, f = 1 MHz	$V_{I/O}$ = 0 to 2 V,		30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ V_{OH} applies for 3-state outputs only.

TEXAS INSTRUMENTS
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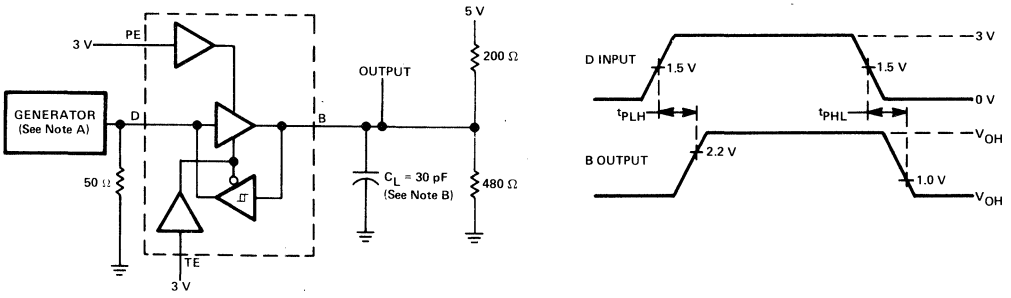
switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), V_{CC} = 5 V

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		7	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					8	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		7	14	ns
t_{PHL}	Propagation delay time, high-to-low-level output					9	14	
t_{PZH}	Output enable time to high level	TE	Bus	C_L = 15 pF, See Figure 3		19	30	ns
t_{PHZ}	Output disable time from high level					5	12	
t_{PZL}	Output enable time to low level					16	35	
t_{PLZ}	Output disable time from low level					9	20	
t_{PZH}	Output enable time to high level	TE	Terminal	C_L = 15 pF, See Figure 4		13	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level					12	20	
t_{PLZ}	Output disable time from low level					11	20	
t_{en}	Output pull-up enable time	PE	Terminal	C_L = 15 pF, See Figure 5		11	22	ns
t_{dis}	Output pull-up disable time					6	12	

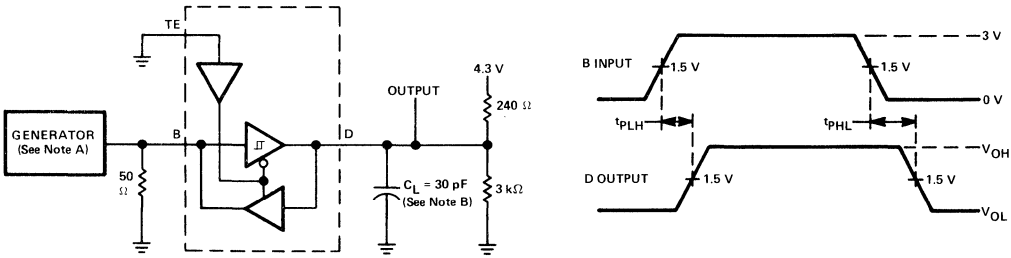
† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

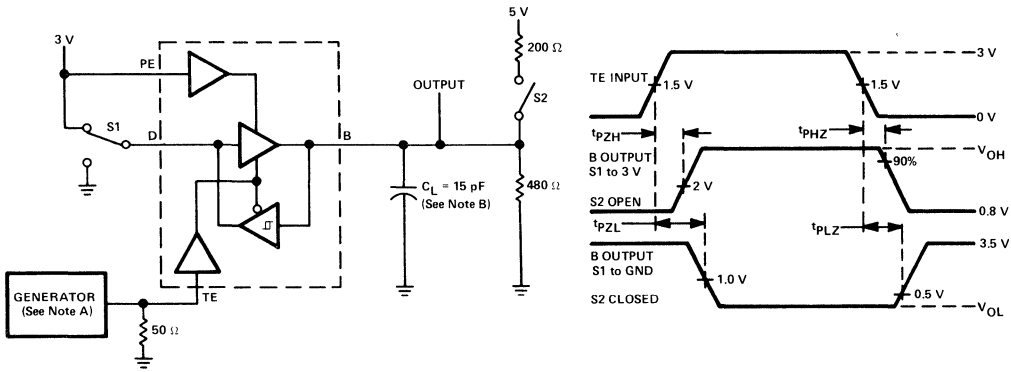
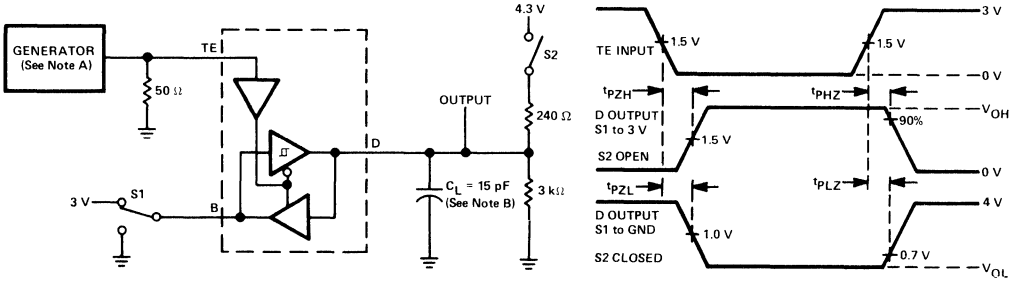


FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.

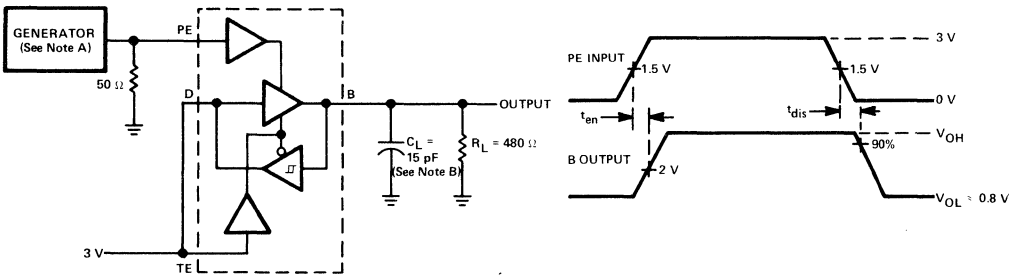
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

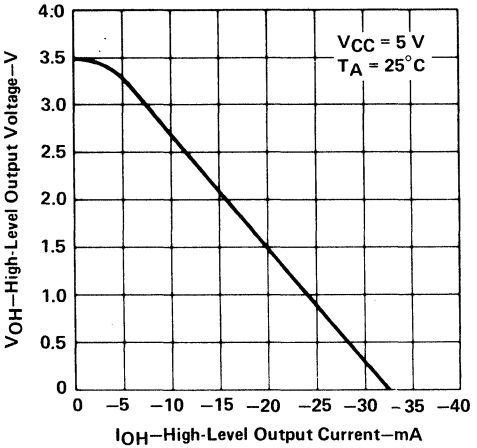


FIGURE 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

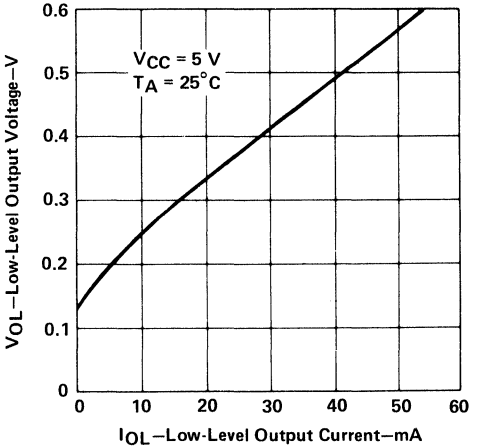


FIGURE 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

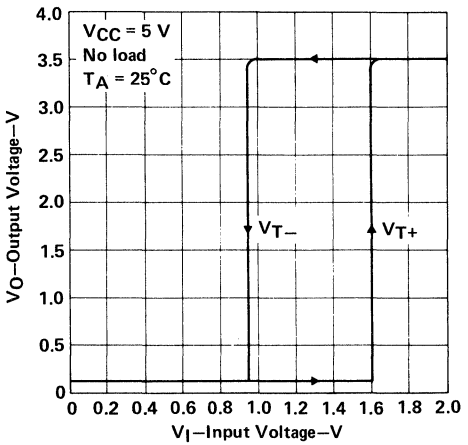


FIGURE 8

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

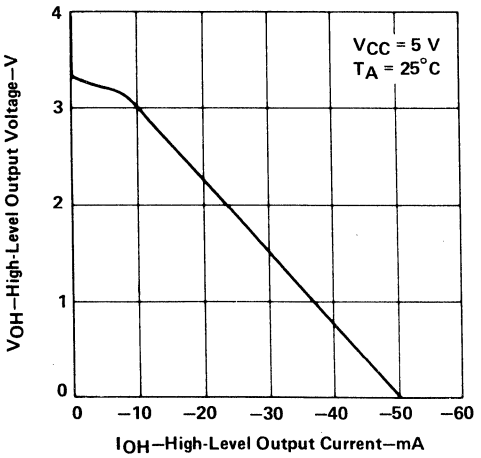


FIGURE 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

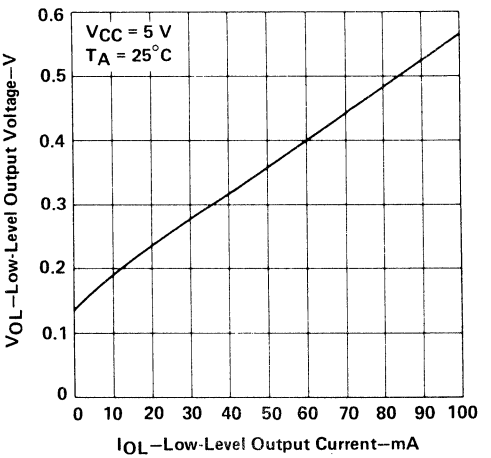


FIGURE 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

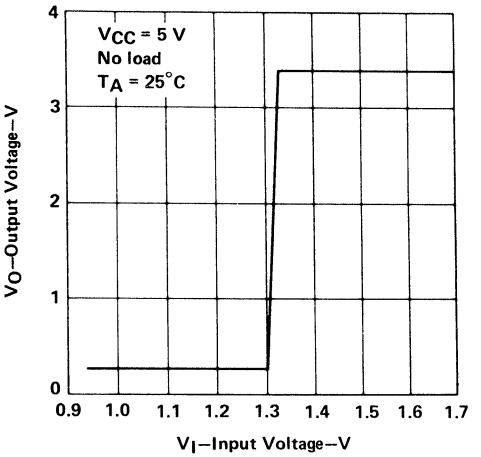
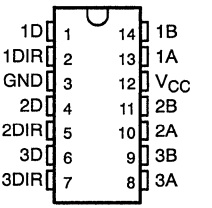


FIGURE 11

D3040, AUGUST 1987–REVISED MAY 1990

- Three Bidirectional Transceivers
- Driver Meets EIA Standards RS-422A and RS-485 and CCITT Recommendations V.11 and X.27 and ANSI Standard X3.131-1986
- High-Speed Advanced Low-Power Schottky Circuitry
- Designed for 25-MBaud Operation in Both Serial and Parallel Applications
- Low Skew . . . 6 ns Max
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Low Supply Current Requirements 90 mA Max
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capacity . . . ± 60 mA
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedances . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ± 300 mV Max
- Receiver Input Hysteresis . . . 60 mV Typ
- Operates from a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection
- Features Independent Direction Controls for Each Channel

J PACKAGE
(TOP VIEW)



Function Table
(each driver)

INPUT D	DIR	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

Function Table
(each receiver)

DIFFERENTIAL INPUTS A – B	DIR	OUTPUT R
$V_{ID} \geq 0.3$ V	L	H
-0.3 V $< V_{ID} < 0.3$ V	L	?
$V_{ID} \leq -0.3$ V	L	L
X	H	Z

H = high level, L = low level, ? = indeterminate;
X = irrelevant, Z = high impedance (off)

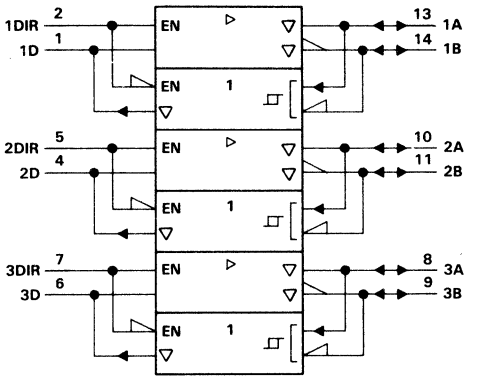
description

The SN75ALS170 triple differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and the driver meets EIA Standards RS-422-A and RS-485 and CCITT recommendations V.11 and X.27 and ANSI Standard X3.131-1986.

The SN75ALS170 operates from a single 5-V power supply. The drivers and receivers have active-high and active-low enables, respectively, which are internally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or $V_{CC} = 0$. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

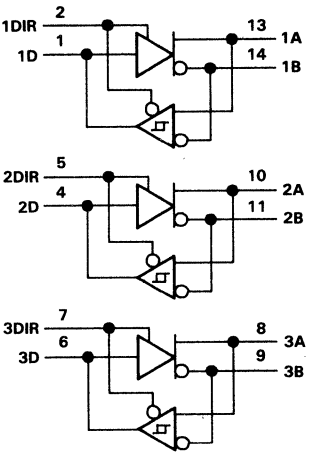
The SN75ALS170 is characterized for operation from 0°C to 70°C.

logic symbol†

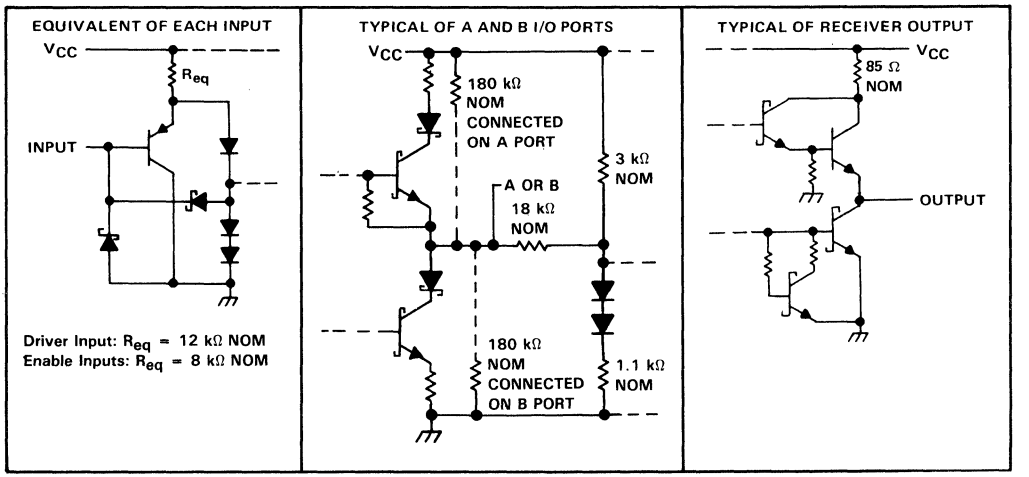


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage at any bus terminal . . . . . −10 V to 15 V
Enable input voltage . . . . . 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds . . . . . 300°C

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
J	1025 mW	8.2 mW/°C	656 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DIR	2			V
Low-level input voltage, V_{IL}	D, DIR			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −55 mA	2.7			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 55 mA			1.7	V
$\lvert V_{OD1} \rvert$	Differential output voltage	I_O = 0		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	1/2 V_{OD1}			
				2			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	V_{test} = −7 V to 12 V,	See Figure 2	1.5		5	V
$\Delta \lvert V_{OD} \rvert$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					+3	V
						−1	
$\Delta \lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Output disabled, See Note 3	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current¶	V_O = −7 V				−250	mA
		V_O = 0				−150	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current	No load	Outputs enabled		69	90	mA
			Outputs disabled		57	78	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ $\Delta \lvert V_{OD} \rvert$ and $\Delta \lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
¶ Duration of the short-circuit current should not exceed one second.
NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

driver switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω, See Figure 3	C_L = 50 pF,	3	8	13	ns
		R_{L1} = R_{L3} = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 6	3	8	13	
	Skew ($\lvert t_{DDH} - t_{DDL} \rvert$)	R_L = 54 Ω, See Figure 3	C_L = 50 pF,		1	6	ns
		R_{L1} = R_{L3} = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 6		1	6	
t_{TD}	Differential-output transition time	R_L = 54 Ω, See Figure 3	C_L = 50 pF,	3	8	13	ns
		R_{L1} = R_{L3} = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 6	3	8	13	
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		30	50	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		30	50	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4	3	8	13	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5	3	8	13	ns
t_{PDE}	Differential-output enable time	R_{L1} = R_{L3} = 165 Ω,	R_{L2} = 75 Ω,	8	30	45	ns
t_{PDZ}	Differential-output disable time	C_L = 60 pF,	See Figure 7	5	10	15	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$		V_t (Test Termination Measurement 2)
V_{test}		V_{tst}
$\Delta \lvert V_{OD} \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.3	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.3‡			V
V_{hys}	Hysteresis§				60		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 300 mV, See Figure 8	I_{OH} = −400 µA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −300 mV, See Figure 8	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 2.4 V				20	µA
		V_O = 0.4 V				−400	
I_I	Line input current	Other input = 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	µA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	µA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 300 mV,	V_O = 0	−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		69	90	mA
			Outputs disabled		57	78	

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.

NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, See Figure 9	C_L = 15 pF,	9	14	19	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	14	19	ns
	Skew ($\lvert t_{PLH} - t_{PHL} \rvert$)				2	6	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 10		7	14	ns
t_{PZL}	Output enable time to low level				7	14	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 10		20	35	ns
t_{PLZ}	Output disable time from low level				8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

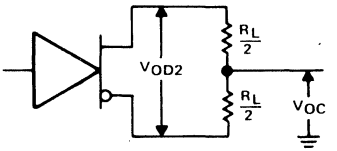


FIGURE 1. DRIVER V_{OD} AND V_{OC}

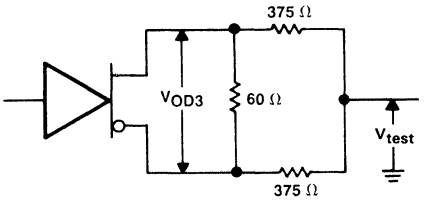


FIGURE 2. DRIVER V_{OD3}

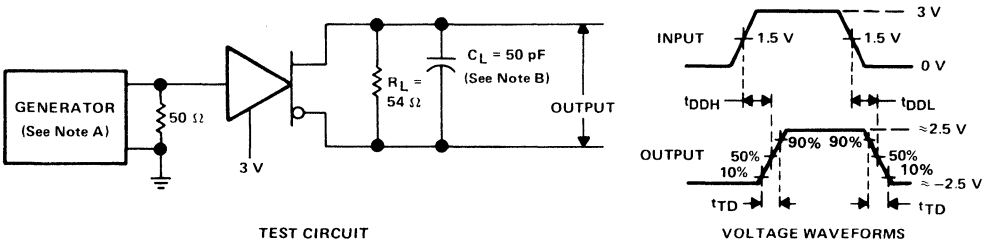


FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

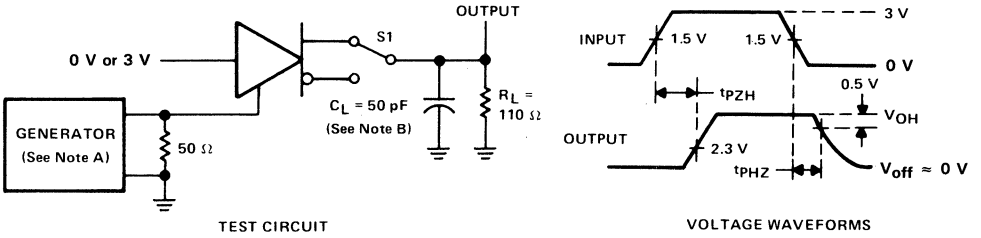


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

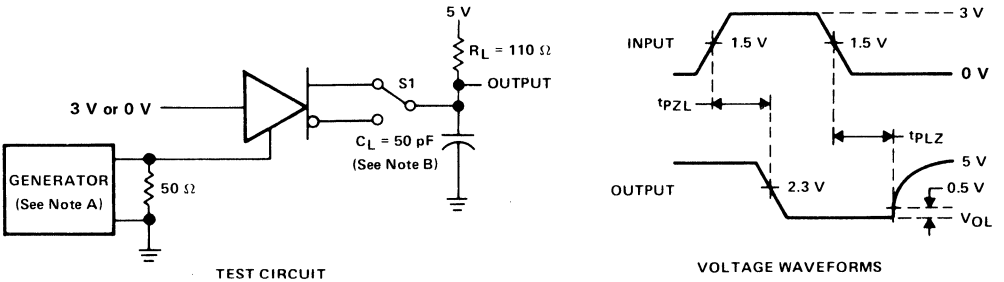


FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

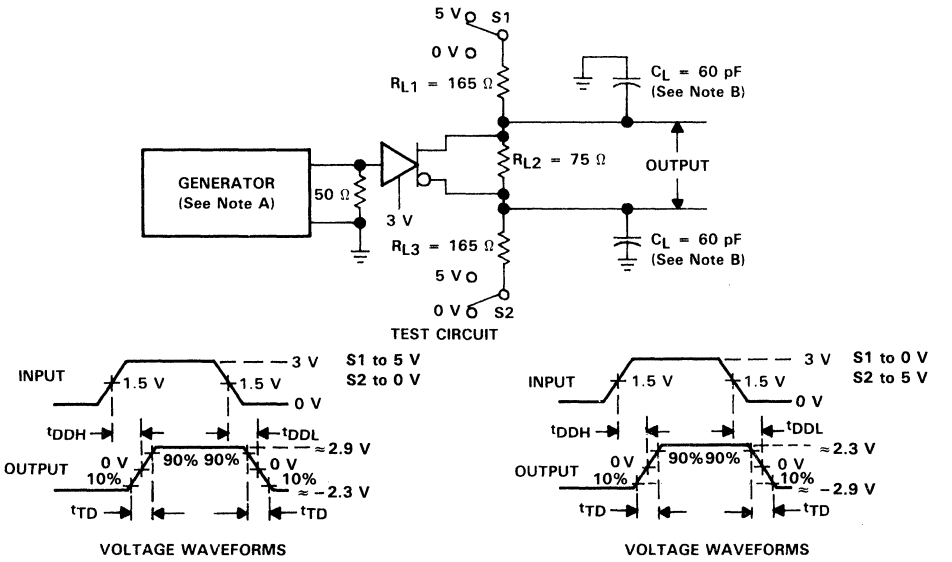
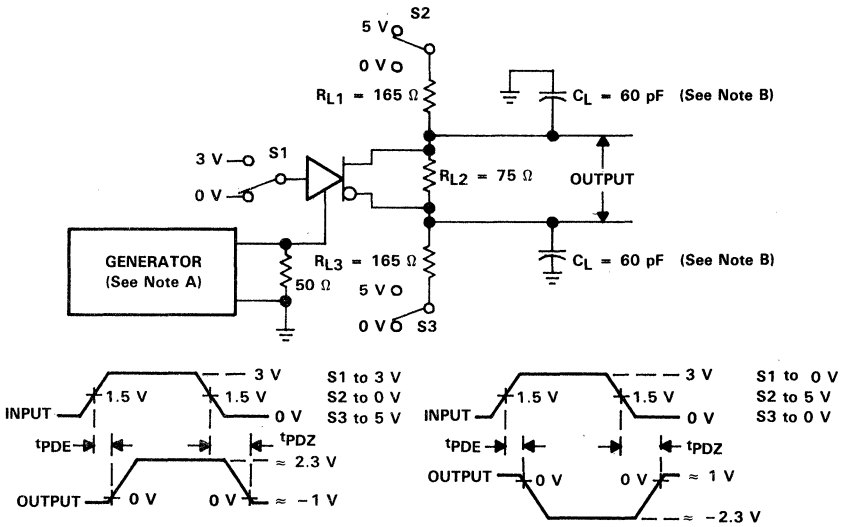


FIGURE 6. DRIVER DELAY AND TRANSITION TIMES WITH DOUBLE-DIFFERENTIAL-SCSI TERMINATION FOR THE LOAD

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 7. DRIVER DIFFERENTIAL-ENABLE AND DISABLE TIMES WITH A DOUBLE-SCSI TERMINATION

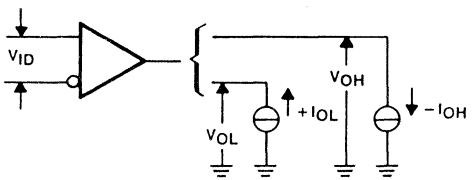


FIGURE 8. RECEIVER V_{OH} AND V_{OL}

TEXAS INSTRUMENTS
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PARAMETER MEASUREMENT INFORMATION

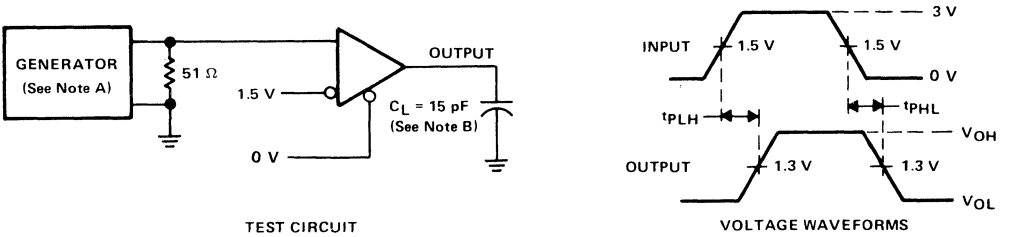

FIGURE 9. RECEIVER PROPAGATION DELAY TIMES

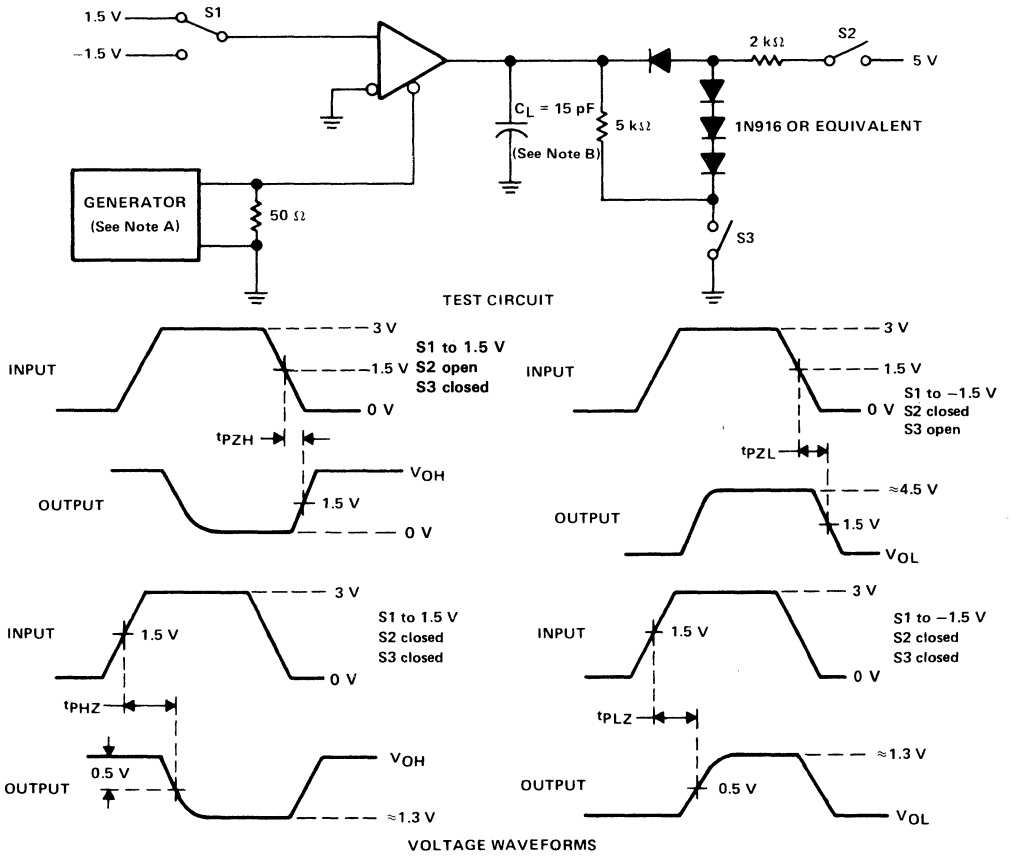

FIGURE 10. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_o = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

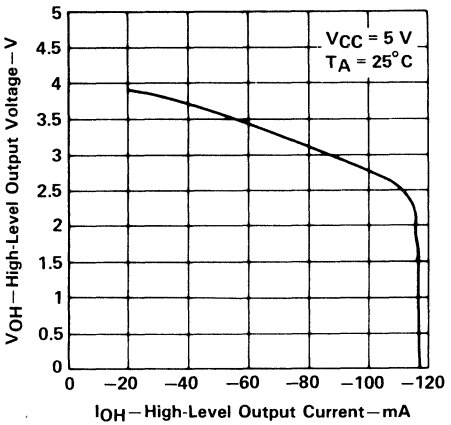

FIGURE 11

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

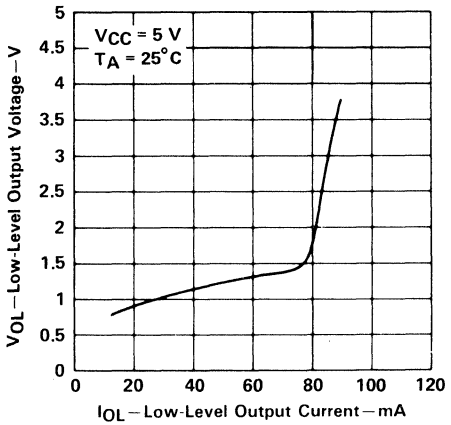

FIGURE 12

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

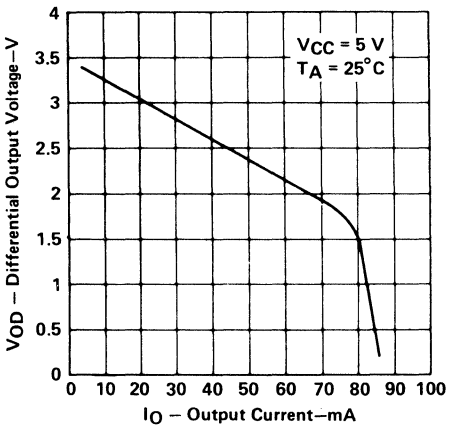

FIGURE 13

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

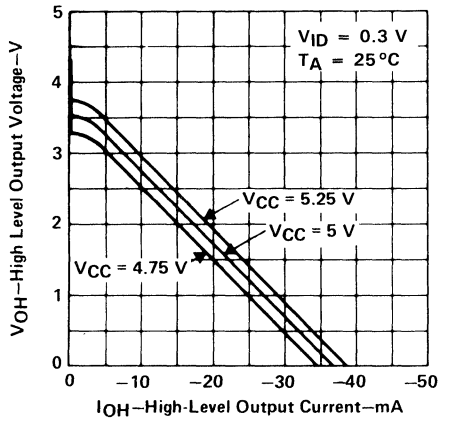


FIGURE 14

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

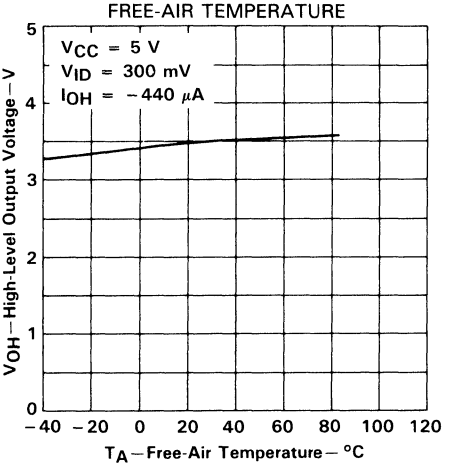


FIGURE 15

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

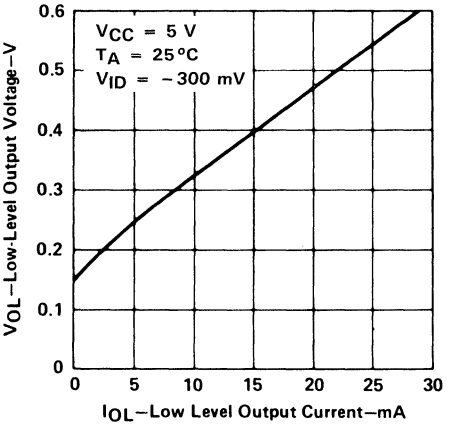


FIGURE 16

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

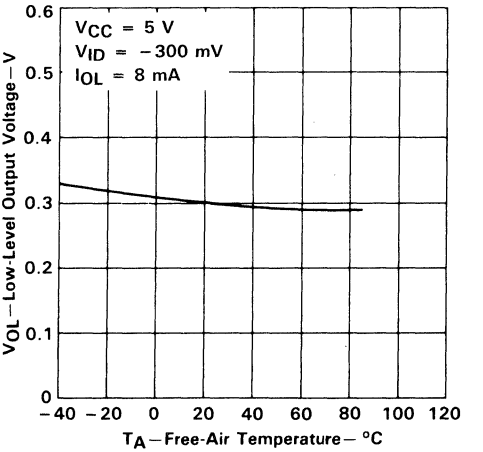


FIGURE 17

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

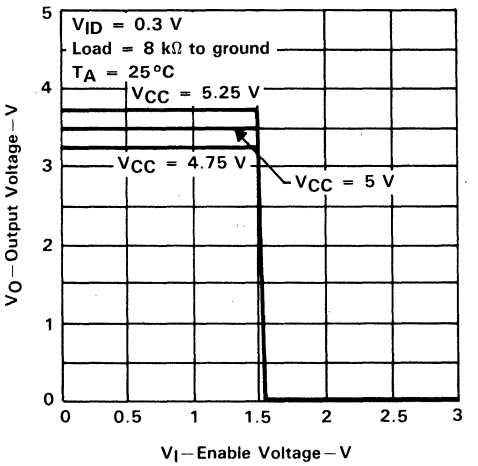


FIGURE 18

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

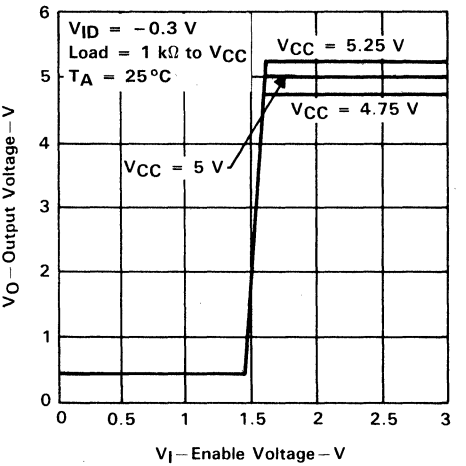


FIGURE 19

APPLICATION INFORMATION

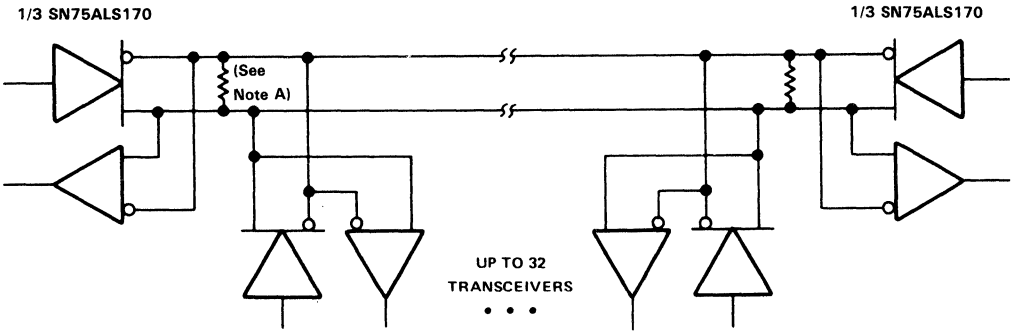


FIGURE 20. TYPICAL APPLICATION CIRCUIT

NOTE A: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

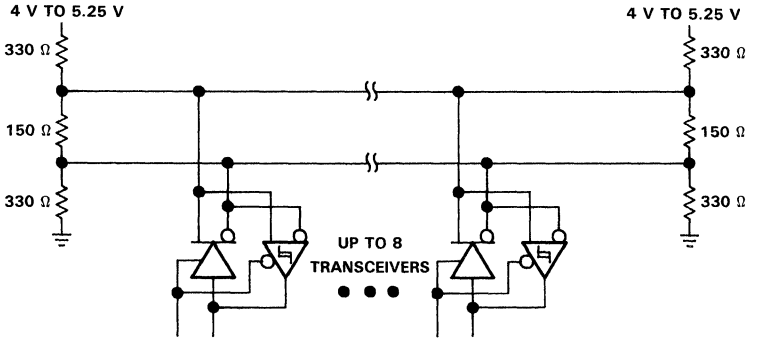


FIGURE 21. TYPICAL DIFFERENTIAL SCSI APPLICATION CIRCUIT

APPLICATION INFORMATION

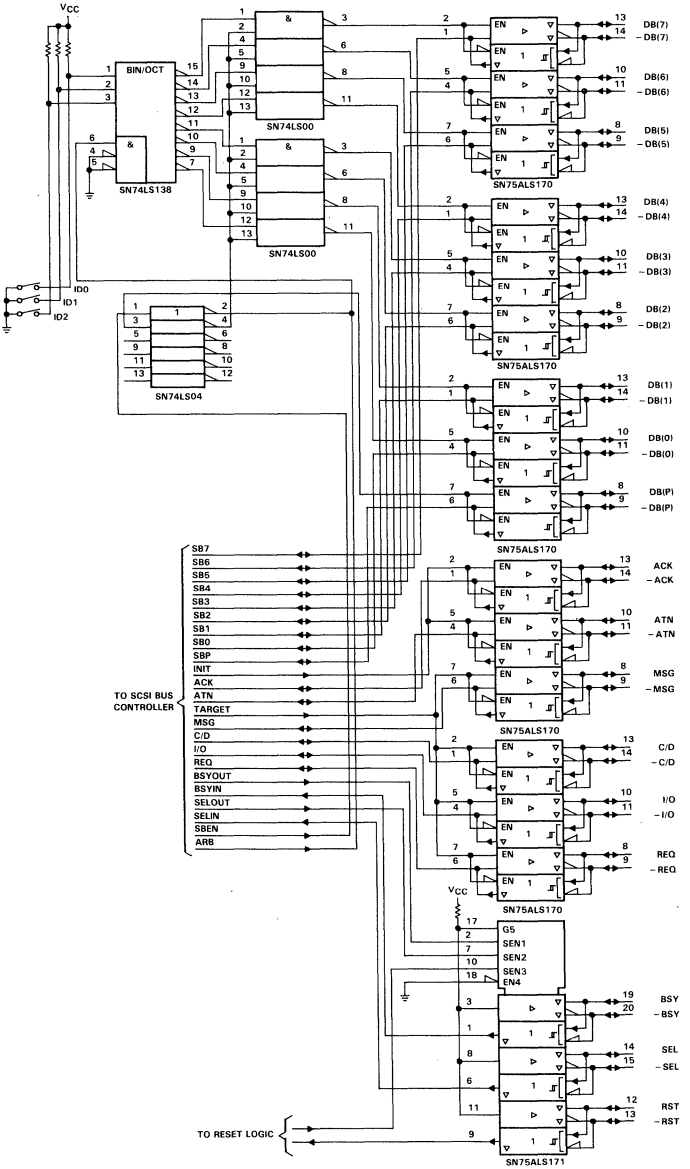
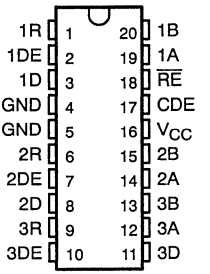


FIGURE 22. TYPICAL DIFFERENTIAL SCSI BUS INTERFACE IMPLEMENTATION

D3041, AUGUST 1987–REVISED MAY 1990

- Three Bidirectional Transceivers
- Driver Meets EIA Standards RS-422A and RS-485 and CCITT Recommendations V.11 and X.27 and ANSI Standard X3.131-1986
- High-Speed Advanced Low-Power Schottky Circuitry
- Designed for 25-MBaud Operation in Both Serial and Parallel Applications
- Low Skew . . . 6 ns Max
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Features Independent Driver Enables and Combined Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltages Ranges
- Driver Output Capacity . . . ± 60 mA
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedances . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ± 300 mV Max
- Receiver Input Hysteresis . . . 60 mV Typ
- Operates from a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection
- Low Supply Current Requirements
  90 mA Max

J PACKAGE
(TOP VIEW)



FUNCTION TABLE (EACH DRIVER)

INPUT	ENABLE		OUTPUTS	
D	DE	CDE	A	B
H	H	H	H	L
L	H	H	L	H
X	L	X	Z	Z
X	X	L	Z	Z

FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A – B	$\overline{RE}$	R
$V_{ID} \geq 0.3$ V	L	H
-0.3 V $< V_{ID} < 0.3$ V	L	?
$V_{ID} \leq -0.3$ V	L	L
X	H	Z

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

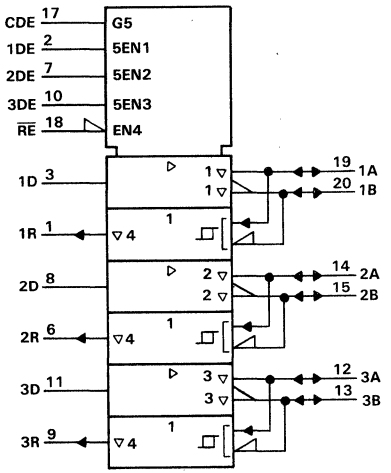
description

The SN75ALS171 triple differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and the driver meets EIA Standards RS-422-A and RS-485 and CCITT recommendations V.11 and X.27 and ANSI Standard X3.131-1986.

The SN75ALS171 operates from a single 5-V power supply. The drivers and receivers have individual active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential output and the receiver differential input pairs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} is at 0 V. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

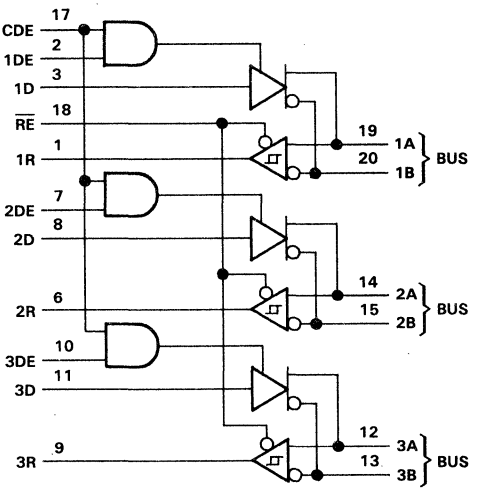
The SN75ALS171 is characterized for operation from 0°C to 70°C.

logic symbol†

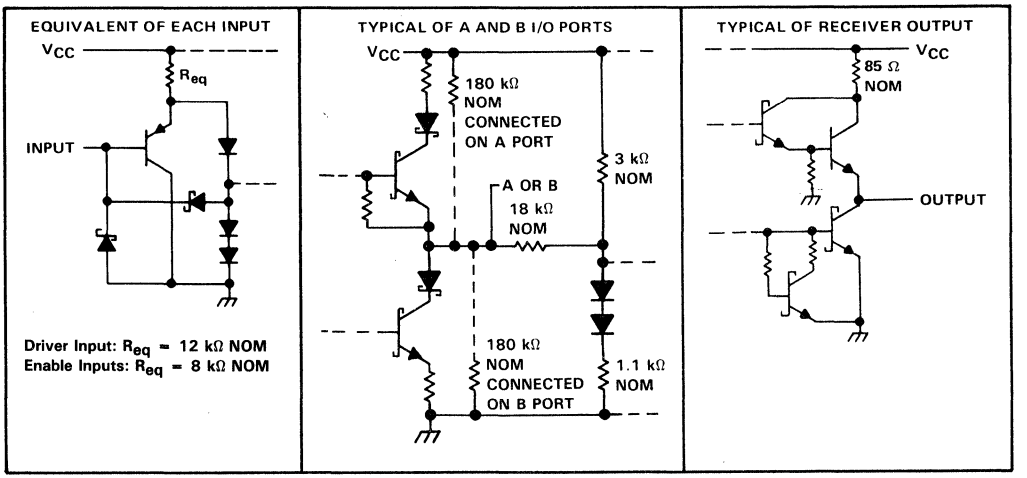


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage at any bus terminal . . . . . −10 V to 15 V
Enable input voltage . . . . . 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds . . . . . 300°C

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
J	1025 mW	8.2 mW/°C	656 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}		−7		12	V
High-level input voltage, V_{IH}	D, CDE, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, CDE, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, TA		0		70	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −55 mA	2.7			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 55 mA			1.7	V
$\lvert V_{OD1} \rvert$	Differential output voltage	I_O = 0		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	1/2 V_{OD1}			
				2			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	V_{test} = −7 V to 12 V,	See Figure 2	1.5		5	V
$\Delta \lvert V_{OD} \rvert$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					+3	V
						−1	
$\Delta \lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Output disabled,	V_O = 12 V			1	mA
		See Note 3	V_O = −7 V			−0.8	
I_{IH}	High-level enable-input current	D and DE	V_{IH} = 2.7 V			20	µA
		CDE				60	
I_{IL}	Low-level enable-input current	D and DE	V_{IL} = 0.4 V			−100	µA
		CDE				−900	
I_{OS}	Short-circuit output current¶	V_O = −7 V				−250	mA
		V_O = 0				−150	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current	No load	Outputs enabled		69	90	mA
			Outputs disabled		57	78	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ $\Delta \lvert V_{OD} \rvert$ and $\Delta \lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
¶ Duration of the short-circuit current should not exceed one second.
NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

driver switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω, See Figure 3	C_L = 50 pF,	3	8	13	ns
		R_{L1} = R_{L3} = 165 Ω, C_L = 60 pF, See Figure 6	R_{L2} = 75 Ω, V_{TERM} = 5 V,	3	8	13	ns
	Skew ($\lvert t_{DDH} - t_{DDL} \rvert$)	R_L = 54 Ω, See Figure 3	C_L = 50 pF,		1	6	ns
		R_{L1} = R_{L3} = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 6		1	6	ns
t_{TD}	Differential-output transition time	R_L = 54 Ω, See Figure 3	C_L = 50 pF,	3	8	13	ns
		R_{L1} = R_{L3} = 165 Ω, C_L = 60 pF, See Figure 6	R_{L2} = 75 Ω, V_{TERM} = 5 V,	3	8	13	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		30	50	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		30	50	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4	3	8	13	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5	3	8	13	ns
t_{PDE}	Differential-output enable time	R_{L1} = R_{L3} = 165 Ω,	R_{L2} = 75 Ω,	8	30	45	ns
t_{PDZ}	Differential-output disable time	C_L = 60 pF,	See Figure 7	5	10	15	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$		V_t (Test Termination Measurement 2)
V_{test}		V_{tst}
$\Delta \lvert V_{OD} \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.3	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.3‡			V
V_{hys}	Hysteresis§				60		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 300 mV, See Figure 8	I_{OH} = −400 µA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = − 300 mV, See Figure 8	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	µA
I_I	Line input current	Other input = 0 V,	V_I = 12 V			1	mA
		See Note 4	V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				60	µA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−300	µA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 300 mV,	V_O = 0	−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		69	90	mA
			Outputs disabled		57	78	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.
NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, See Figure 9	C_L = 15 pF,	9	14	19	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	14	19	ns
	Skew ($\lvert t_{PLH} - t_{PHL} \rvert$)				2	6	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 10		7	14	ns
t_{PZL}	Output enable time to low level				7	14	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 10		20	35	ns
t_{PLZ}	Output disable time from low level				8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

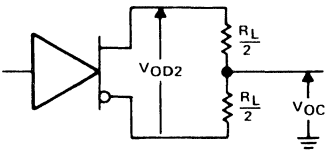


FIGURE 1. DRIVER V_{OD} AND V_{OC}

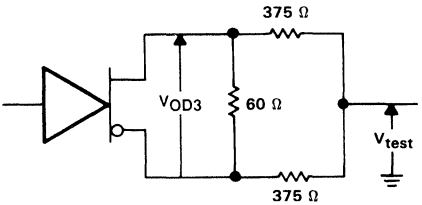


FIGURE 2. DRIVER V_{OD3}

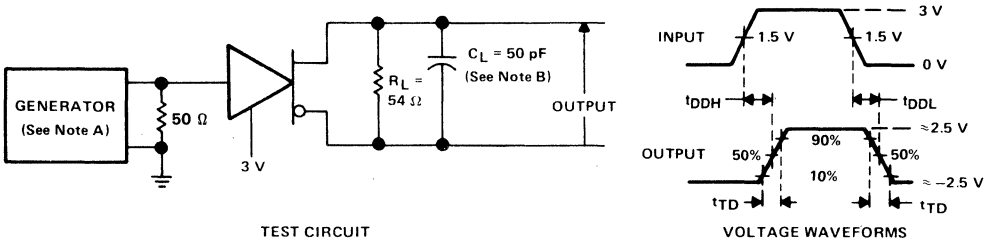


FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_o = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

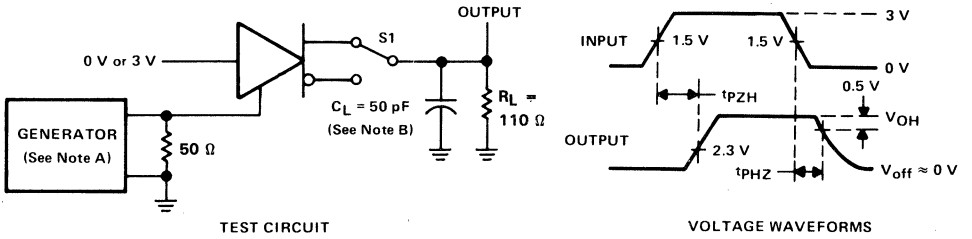


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

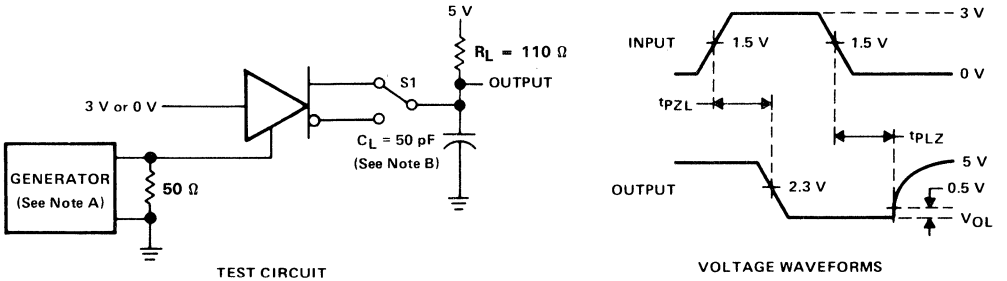


FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

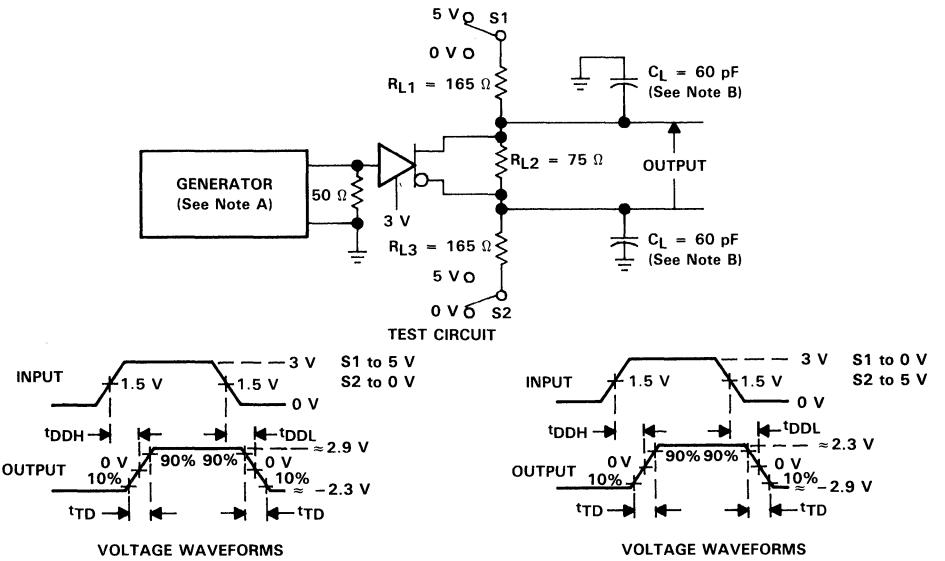


FIGURE 6. DRIVER DELAY AND TRANSITION TIMES WITH DOUBLE-DIFFERENTIAL-SCSI TERMINATION FOR THE LOAD

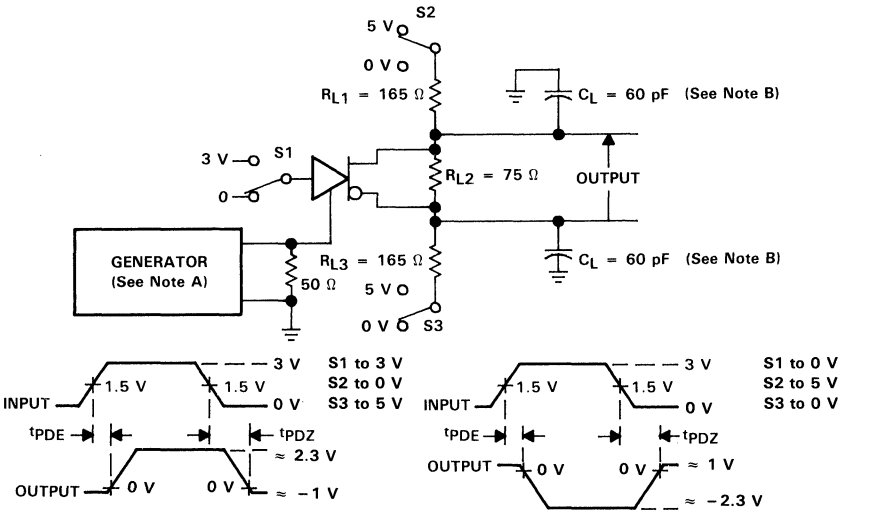


FIGURE 7. DRIVER DIFFERENTIAL-ENABLE AND DISABLE TIMES WITH A DOUBLE-SCSI TERMINATION

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

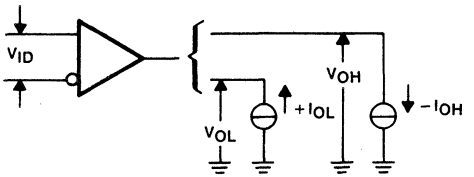


FIGURE 8. RECEIVER V_{OH} AND V_{OL}

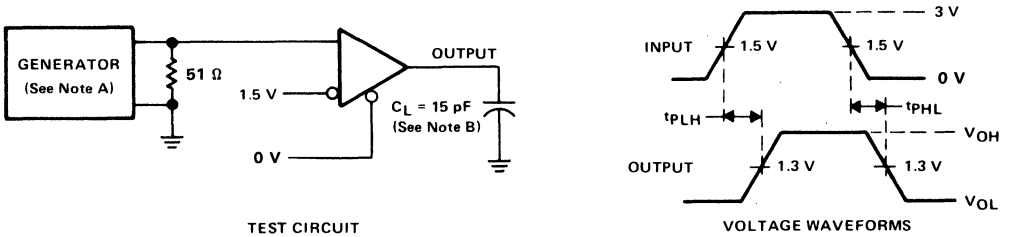


FIGURE 9. RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

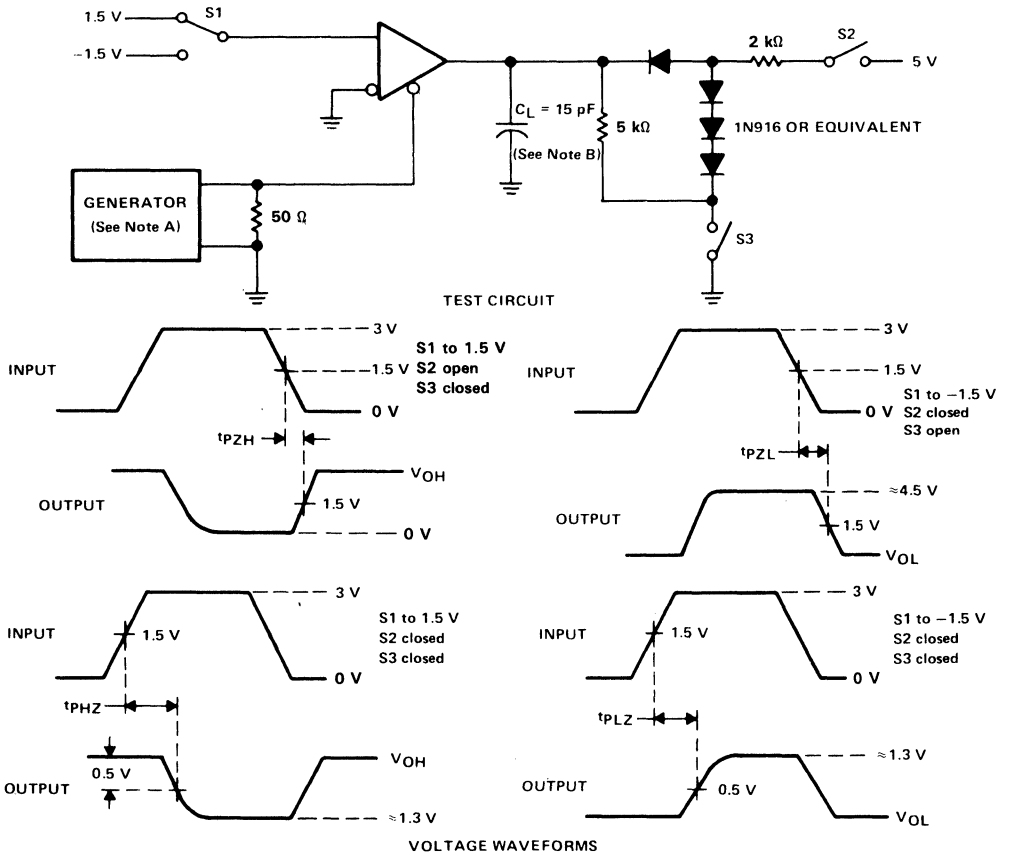


FIGURE 10. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

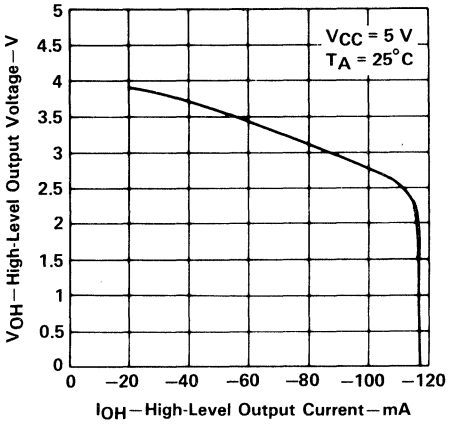


FIGURE 11

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

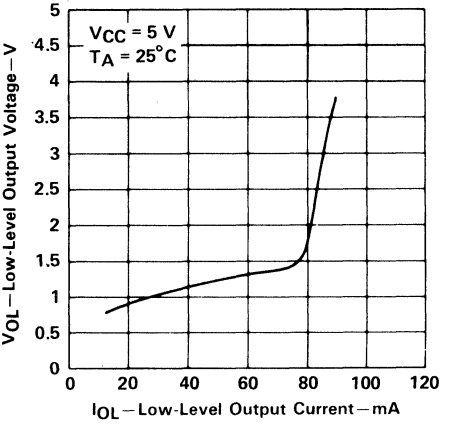


FIGURE 12

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

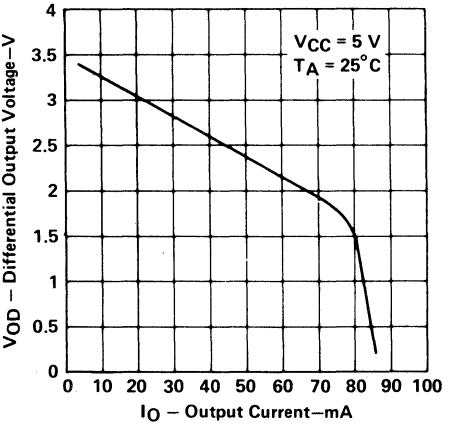


FIGURE 13

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

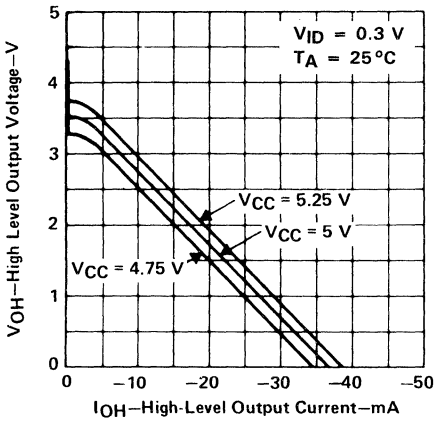


FIGURE 14

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

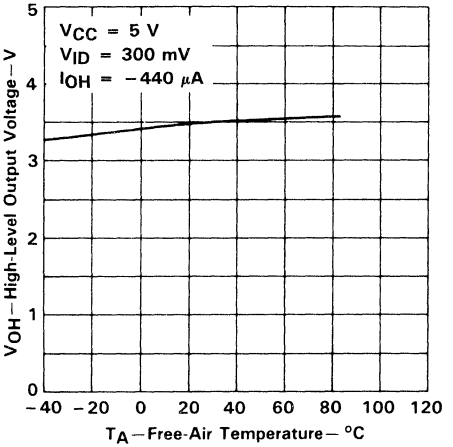


FIGURE 15

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

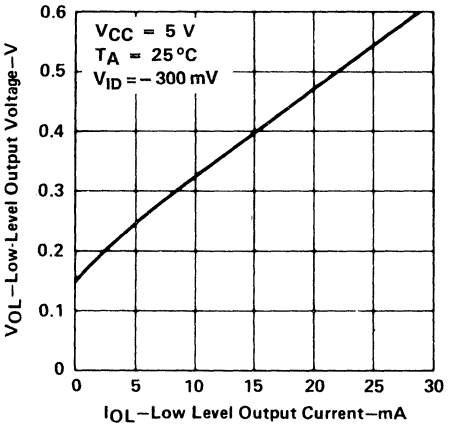


FIGURE 16

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

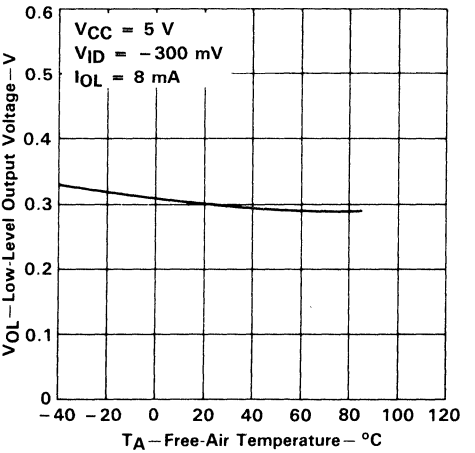


FIGURE 17

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

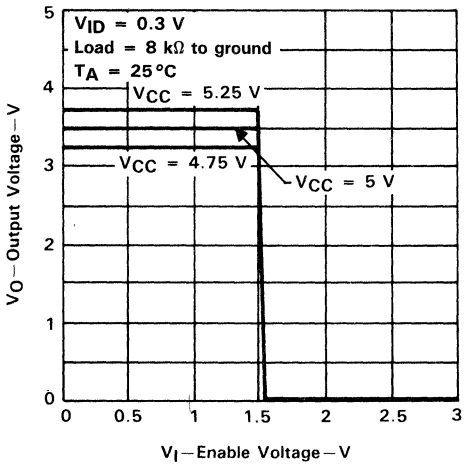


FIGURE 18

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

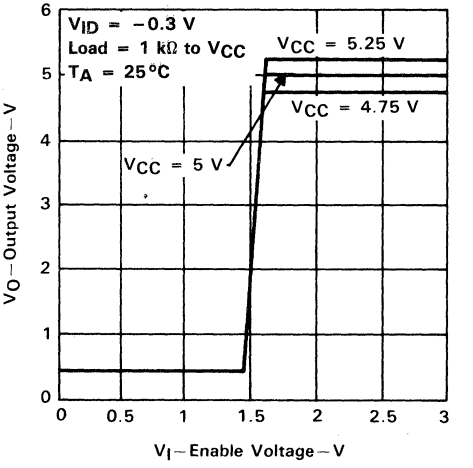
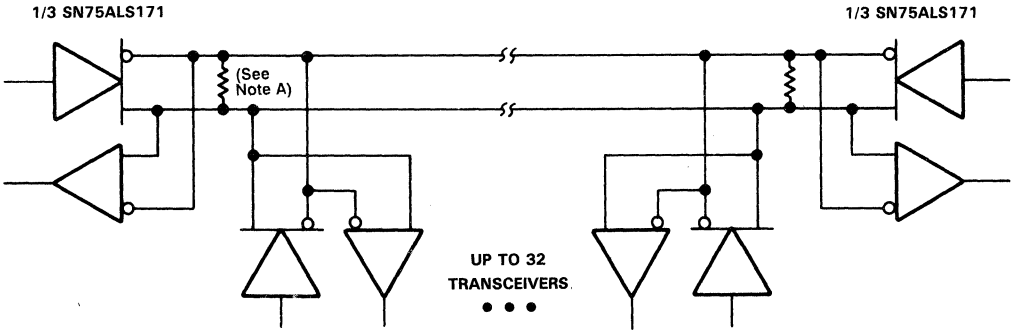


FIGURE 19

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 20. TYPICAL APPLICATION CIRCUIT

APPLICATION INFORMATION

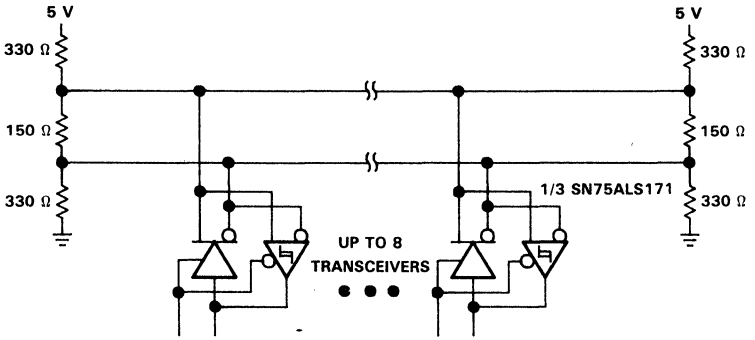


FIGURE 21. TYPICAL DIFFERENTIAL SCSI APPLICATION CIRCUIT

APPLICATION INFORMATION

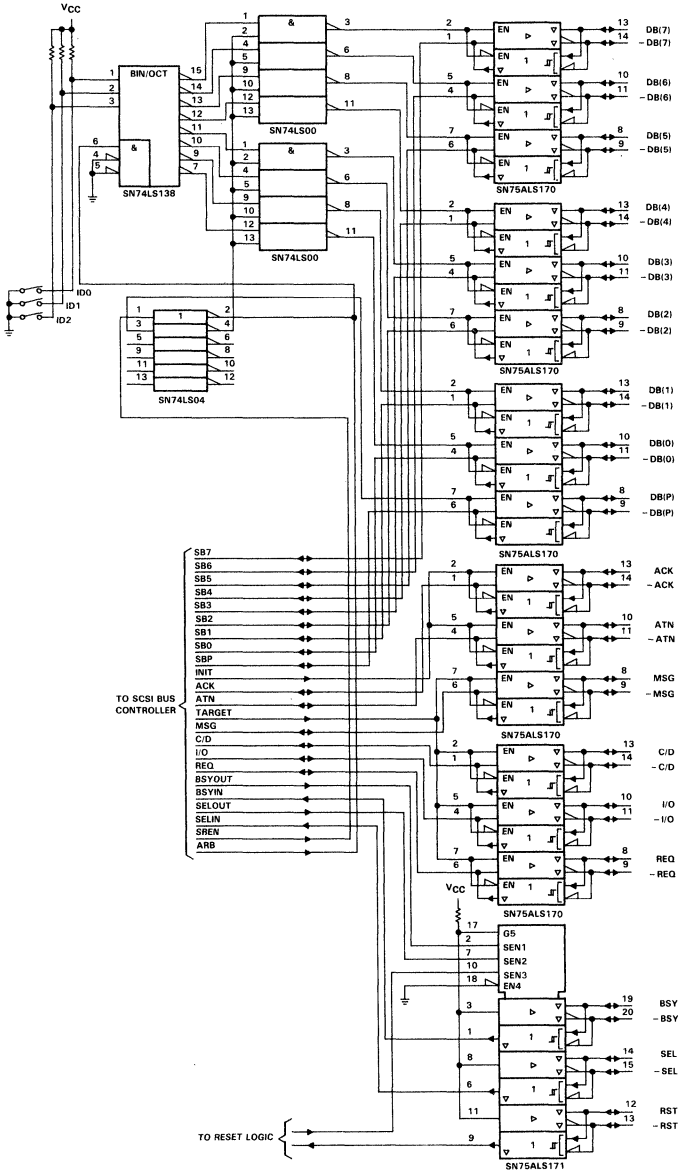


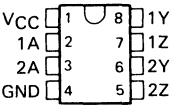
FIGURE 22. TYPICAL DIFFERENTIAL SCSI BUS INTERFACE IMPLEMENTATION

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D3068, DECEMBER 1987—REVISED AUGUST 1989

- **Meets EIA Standard RS-422-A**
- **High Speed, Low-Power ALS Design**
- **TTL-and CMOS-Input Compatibility**
- **Single 5-V Supply Operation**
- **Output Short-Circuit Protection**
- **Improved Replacement for the UA9638**

D OR P PACKAGE
(TOP VIEW)



description

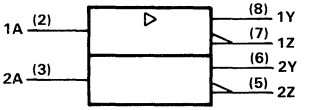
The SN75ALS191 is a dual high-speed differential line driver designed to meet EIA Standard RS-422-A. The inputs are TTL- and CMOS-compatible and have input clamp diodes. Schottky-diode-clamped transistors are used to minimize propagation delay time. This device operates from a single 5-volt power supply and is supplied in 8-pin packages.

The SN75ALS191 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH DRIVER)

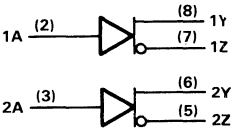
INPUT	OUTPUTS	
A	Y	Z
H	H	L
L	L	H

logic symbol†

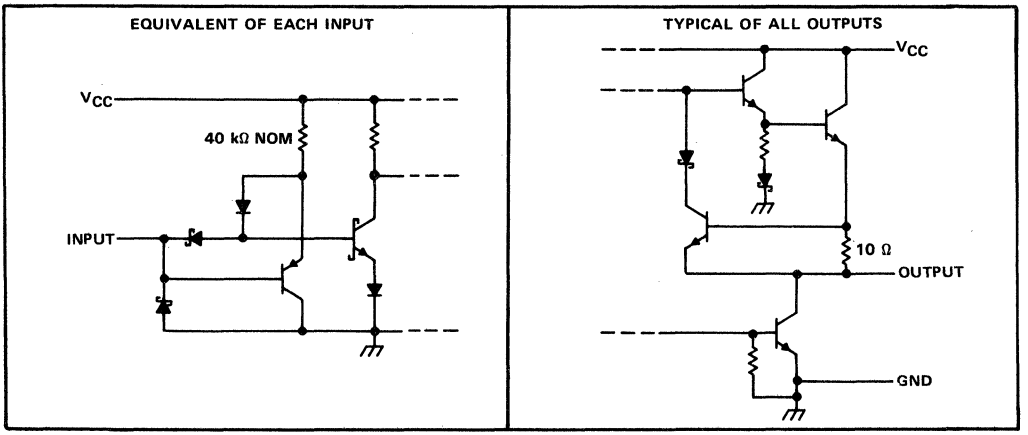


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values except differential output voltage V_{OD} are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−50	mA
Low-level output current, I_{OL}			50	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −18 mA			−1	−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −10 mA	2.5	3.3		V
			I_{OH} = −40 mA	2			
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 40 mA				0.5	V
$\lvert V_{OD1} \rvert$	Differential output voltage	V_{CC} = 5.25 V, I_O = 0				$2V_{OD2}$	V
$\lvert V_{OD2} \rvert$	Differential output voltage	V_{CC} = 4.75 V to 5.25 V, R_L = 100 Ω, See Figure 1		2			V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of‡ differential output voltage					±0.4	V
V_{OC}	Common-mode output voltage§					3	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of‡ common-mode output voltage					±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V		0.1	100	μA
			V_O = −0.25 V		−0.1	−100	
			V_O = −0.25 V to 6 V			±100	
I_I	Input current	V_{CC} = 5.25 V, V_I = 5.5 V				50	μA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.7 V				25	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.5 V				−200	μA
I_{OS}	Short-circuit output current¶	V_{CC} = 5.25 V, V_O = 0		−50		−150	mA
I_{CC}	Supply current (all drivers)	V_{CC} = 5.25 V, No load,	All inputs at 0 V		32	40	mA

†All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡$\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
¶Only one output at a time should be shorted and duration of the short-circuit should not exceed one second.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), V_{CC} = 5 V

PARAMETER		TEST CONDITION	MIN	TYP#	MAX	UNIT
t_{DD}	Differential-output delay time	C_L = 15 pF, R_L = 100 Ω, See Figure 2		3.5	7	ns
t_{TD}	Differential-output transition time			3.5	7	ns
	Skew			1.5	4	ns

Typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

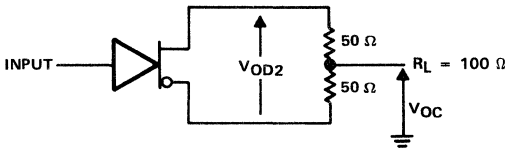
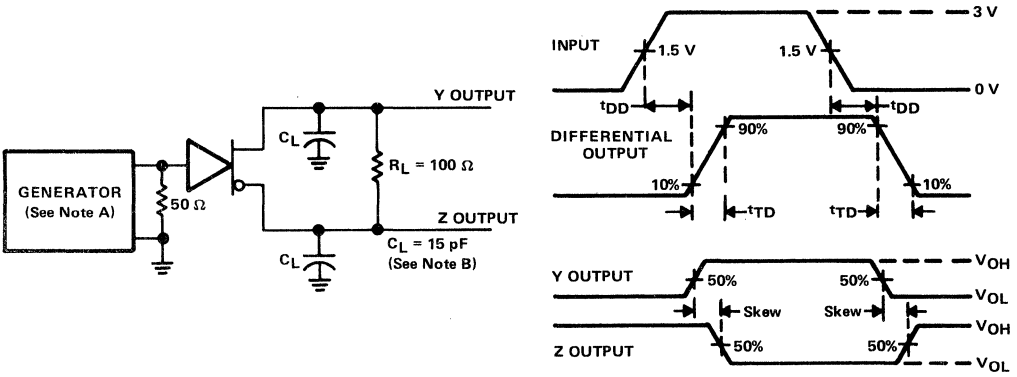


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



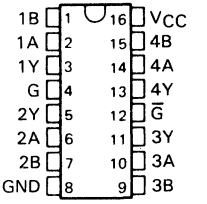
TEST CIRCUITS **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse generator has the following characteristics: Z_{OUT} = 50 Ω, PRR ≤ 500 kHz, t_w = 100 ns, t_r = ≤ 5 ns.
B. C_L includes probe and jig capacitance.

FIGURE 2. SWITCHING TIMES

- **Meets EIA Standards RS-422-A and RS-423-A**
- **Meets CCITT Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Input Voltage Range . . . −7 V to 7 V**
- **Input Sensitivity . . . ±200 mV**
- **Input Hysteresis . . . 120 mV Typ**
- **High Input Impedance . . . 12 kΩ Min**
- **Operates from Single 5-V Supply**
- **Low I_{CC} Requirements: I_{CC} . . . 35 mA Max**
- **Improved Speed and Power Consumption Compared to AM26LS32A**

J PACKAGE
(TOP VIEW)



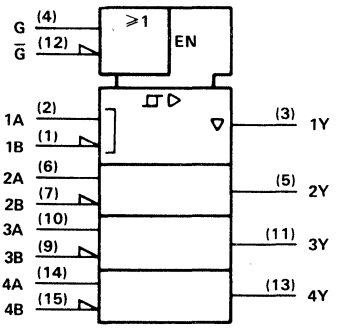
description

The SN75ALS193 is a monolithic quadruple line receiver with 3-state outputs designed using Advanced Low-Power Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication. This, in turn, provides significantly less power requirements and permits much higher data throughput than other designs. The device meets the specifications of EIA Standards RS-422-A and RS-423-A. It features 3-state outputs that permit direct connection to a bus-organized system with a Fail-Safe design that ensures the outputs will always be high if the inputs are open.

The device is optimized for balanced multipoint bus transmission at rates up to 20 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ±200 mV over a common-mode input voltage range of −7 to 7 V. It also features active-high and active-low enable functions that are common to the four channels. The SN75ALS193 is designed for optimum performance when used with the SN75ALS192 quadruple differential line driver.

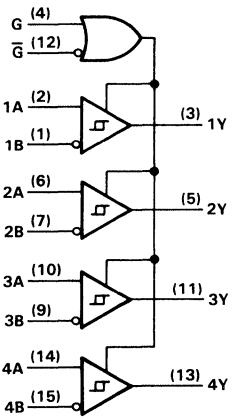
The SN75ALS193 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

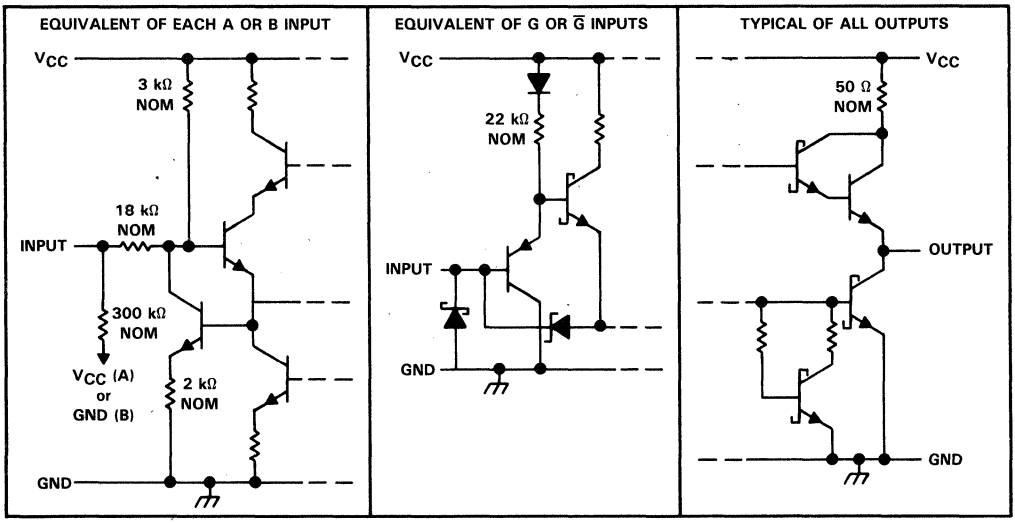


FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL A–B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V $< V_{ID} <$ 0.2 V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z

H = high level
L = low level
X = irrelevant
? = indeterminate
Z = high impedance (off)

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, A or B inputs . . . . . ±15 V
Differential input voltage (see Note 2) . . . . . ±15 V
Enable input voltage . . . . . 7 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 1025 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds . . . . . 300°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the J package to 656 mW at 70°C at the rate of 8.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Differential input voltage, V_{ID}			±12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended range of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage					200	mV
V_{T-}	Negative-going threshold voltage			−200‡			mV
V_{hys}	Hysteresis§				120		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 1	I_{OH} = −400 μA,	2.7	3.6		V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 1	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_{CC} = 5.25 V	V_O = 2.4 V			20	μA
			V_O = 0.4 V			−20	
I_I	Line input current	Other input at 0 V, See Note 4	V_I = 15 V		0.7	1.2	mA
			V_I = −15 V		−1.0	−1.7	
I_{IH}	High-level enable-input current		V_{IH} = 2.7 V			20	μA
			V_{IH} = 5.25 V			100	
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
	Input resistance			12	18		kΩ
I_{OS}	Short-circuit output current	V_{ID} = 3 V, See Note 5	V_O = 0,	−15	−78	−130	mA
I_{CC}	Supply current	Outputs disabled			22	35	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
NOTES: 4. Refer to EIA Standard RS-422-A and RS-423-A for exact conditions.
5. Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −2.5 V to 2.5 V, C_L = 15 pF, See Figure 2			15	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output				15	22	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PZL}	Output enable time to low level	C_L = 15 pF,	See Figure 3		11	25	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF,	See Figure 3		13	25	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF,	See Figure 3		15	22	ns

PARAMETER MEASUREMENT INFORMATION

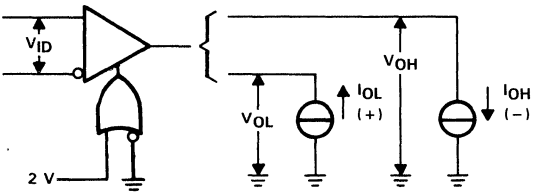
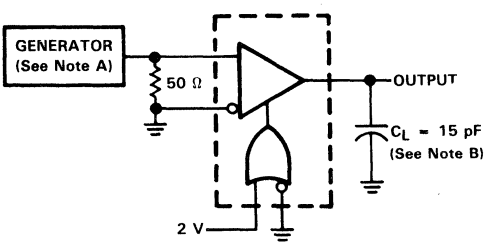
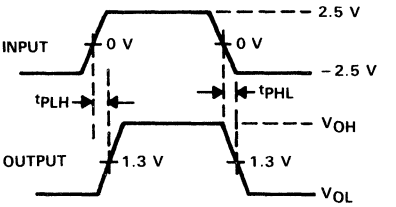


FIGURE 1. V_{OH}, V_{OL}



TEST CIRCUIT

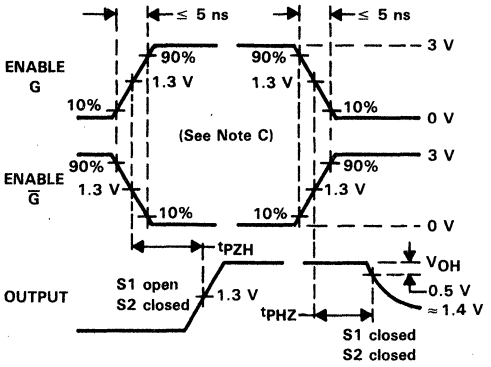


VOLTAGE WAVEFORMS

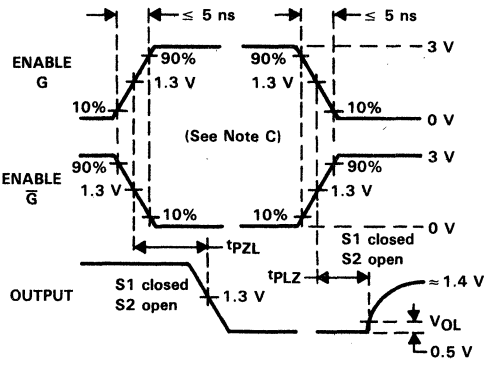
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_{out} = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

FIGURE 2. t_{PLH}, t_{PHL}

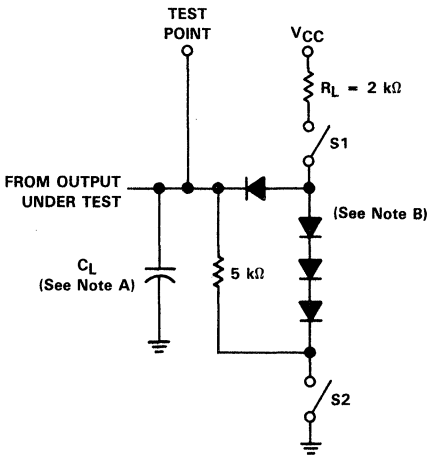
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS FOR t_{PHZ}, t_{PZH}



VOLTAGE WAVEFORMS FOR t_{PLZ}, t_{PZL}



LOAD CIRCUIT

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

FIGURE 3. t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL}

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

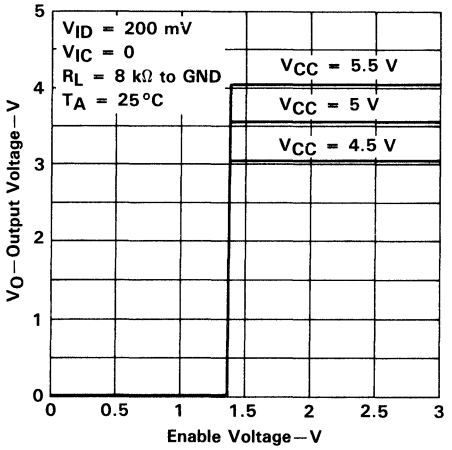


FIGURE 4

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

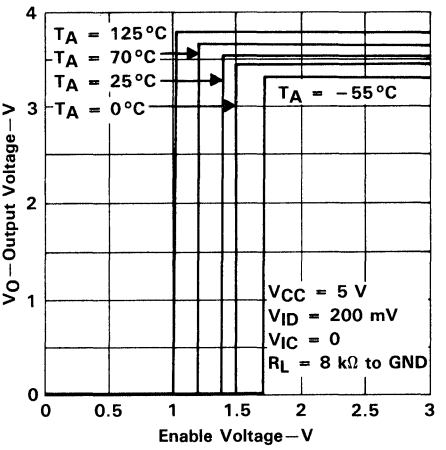


FIGURE 5

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

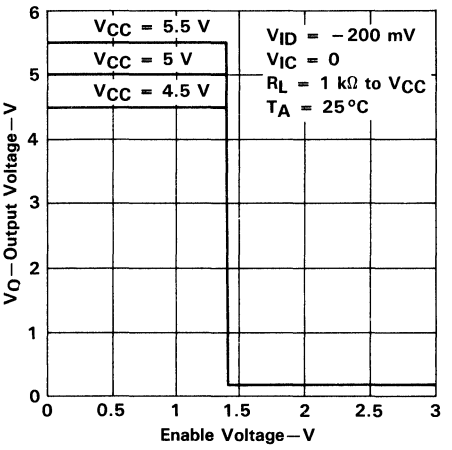


FIGURE 6

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

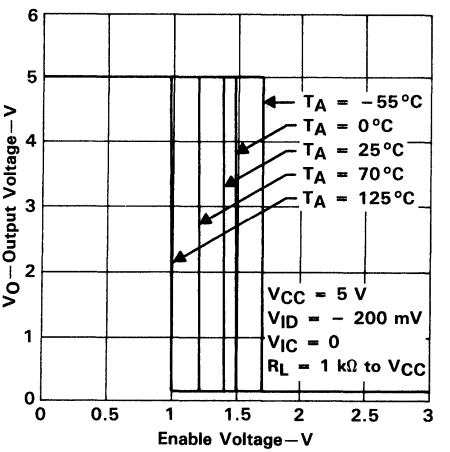


FIGURE 7

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

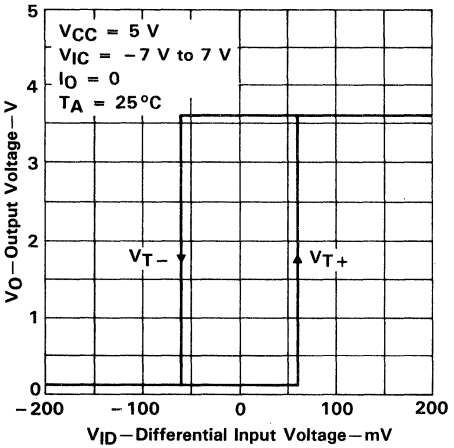


FIGURE 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

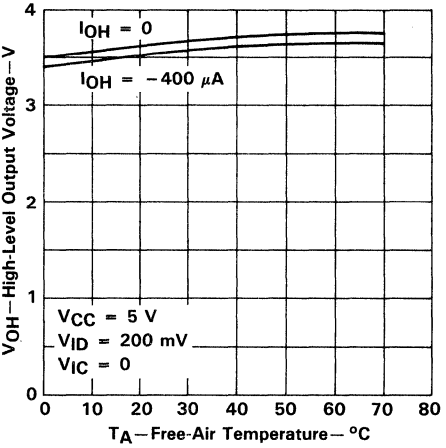


FIGURE 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

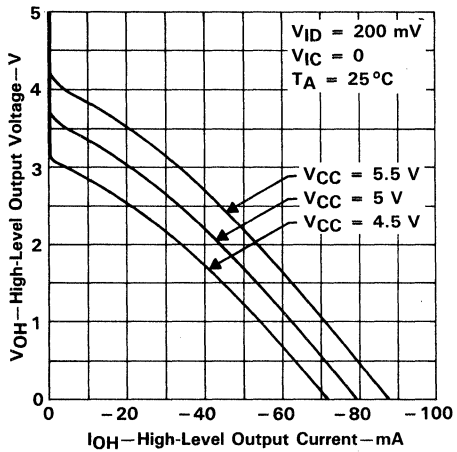


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

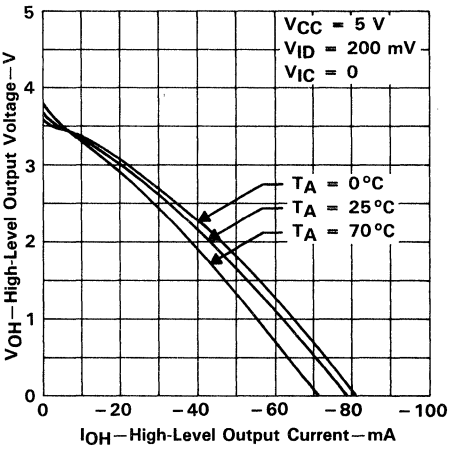


FIGURE 11

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

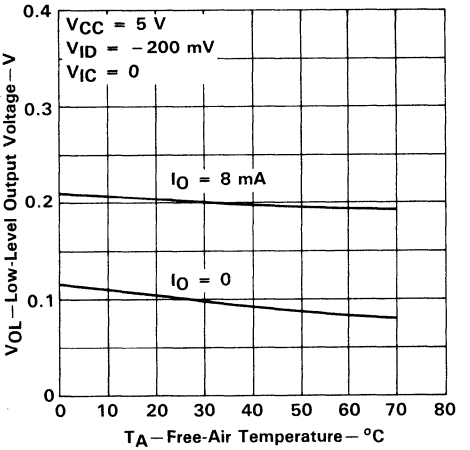


FIGURE 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

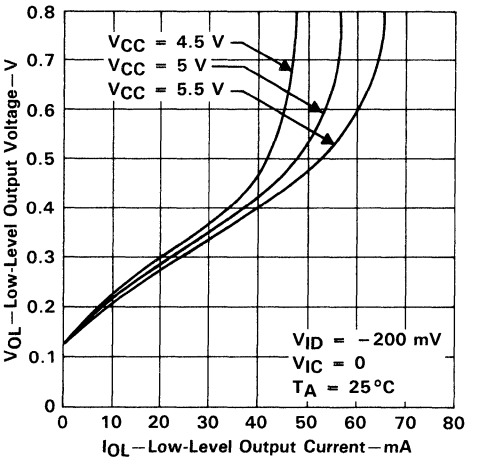


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

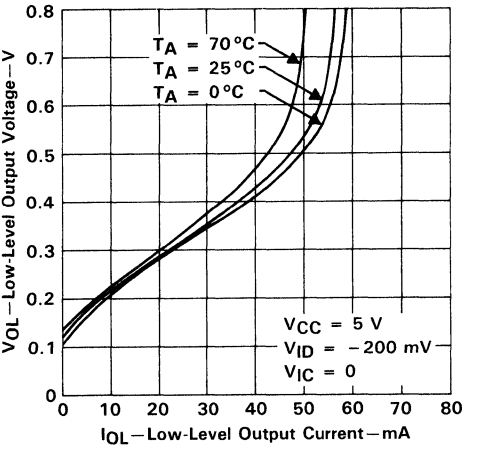


FIGURE 14

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

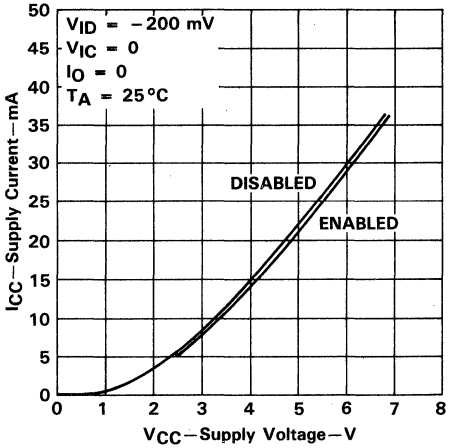


FIGURE 15

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

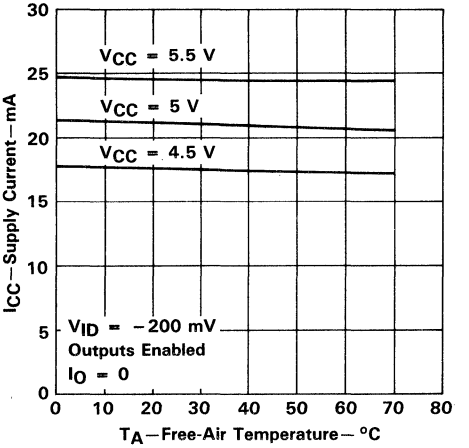


FIGURE 16

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

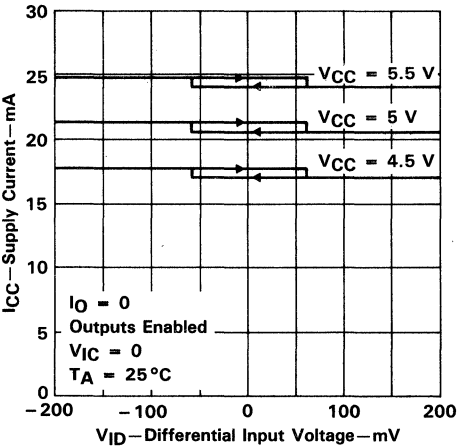


FIGURE 17

SUPPLY CURRENT
vs
FREQUENCY

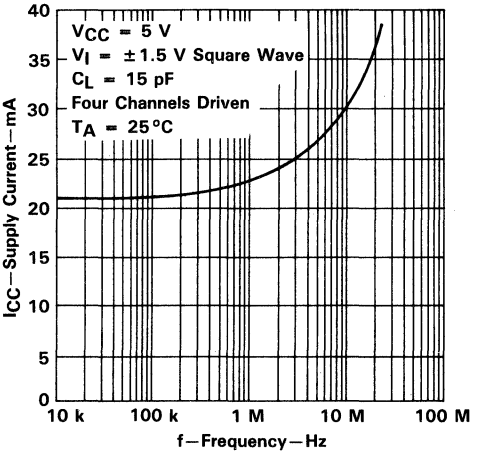


FIGURE 18

TYPICAL CHARACTERISTICS

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

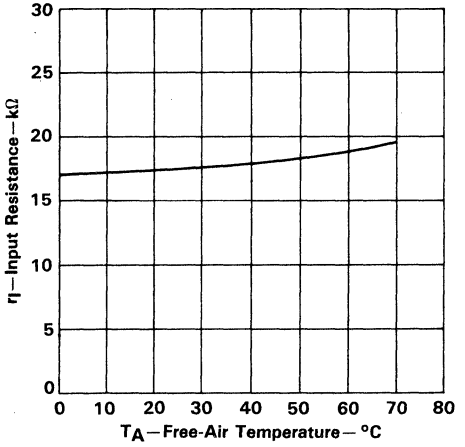


FIGURE 19

INPUT CURRENT
vs
INPUT VOLTAGE

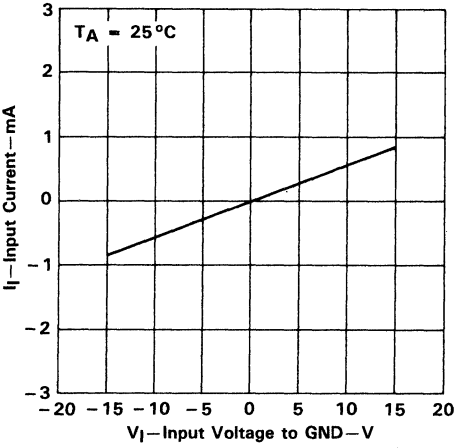


FIGURE 20

SWITCHING CHARACTERISTICS
vs
FREE-AIR TEMPERATURE

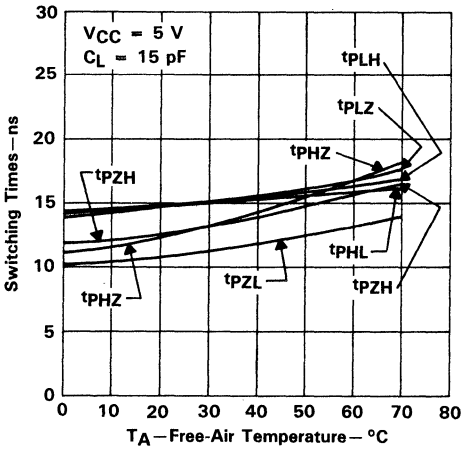


FIGURE 21

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

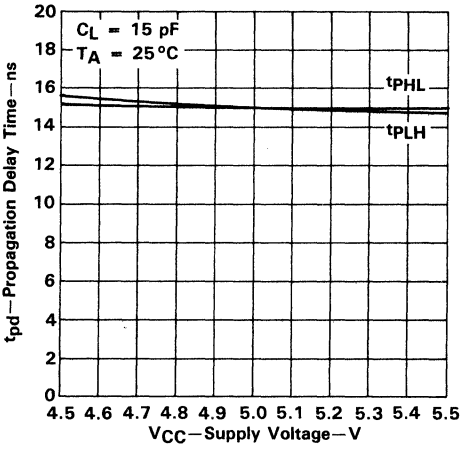
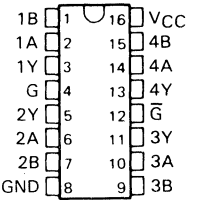


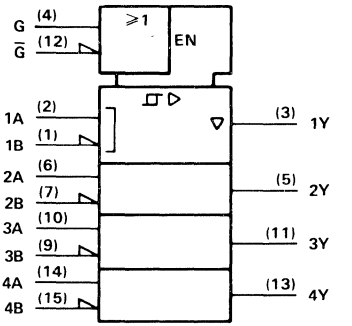
FIGURE 22

- **Meets CCITT Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Input Voltage Range . . . −7 V to 7 V**
- **Input Sensitivity . . . ±300 mV**
- **Input Hysteresis . . . 120 mV Typ**
- **High Input Impedance . . . 12 kΩ Min**
- **Operates from Single 5-V Supply**
- **Low I_{CC} Requirements: I_{CC} . . . 35 mA Max**
- **Improved Speed and Power Consumption Compared to AM26LS32A**

D OR N PACKAGE
(TOP VIEW)

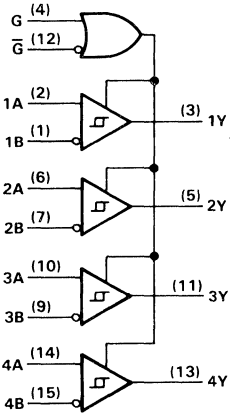


logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



description

The SN75ALS197 is a monolithic quadruple line receiver with three-state outputs designed using Advanced Low-Power Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication. This, in turn, provides significantly less power requirements and permits much higher data throughput than other designs. The device meets the specifications of CCITT Recommendations V.10, V.11, X.26, and X.27. It features three-state outputs that permit direct connection to a bus-organized system with a Fail-Safe design that ensures the outputs will always be high if the inputs are open.

The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ±300 mV over a common-mode input voltage range of −7 V to 7 V. It also features active-high and active-low enable functions that are common to the four channels. The SN75ALS197 is designed for optimum performance when used with the SN75ALS192 quadruple differential line driver.

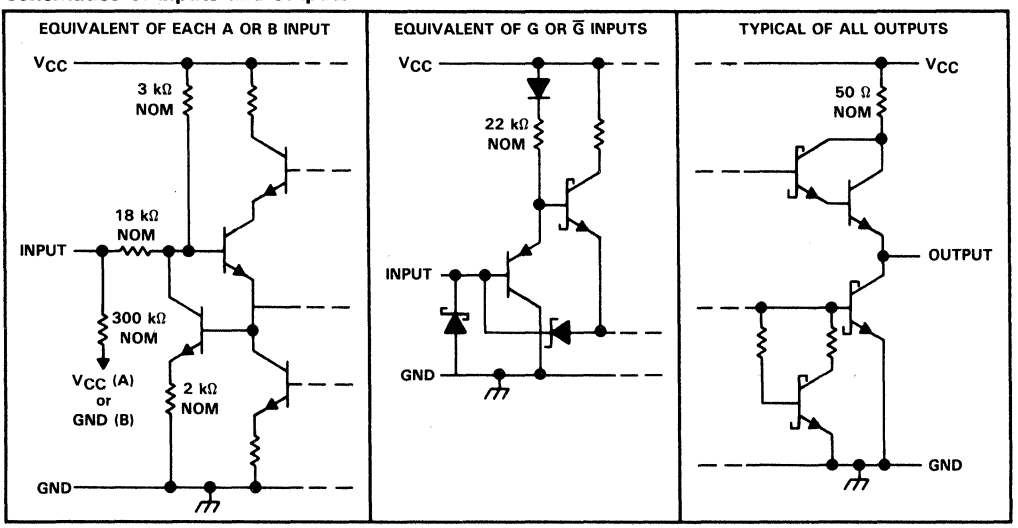
The SN75ALS197 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL A–B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.3$ V	H	X	H
	X	L	H
-0.3 V $< V_{ID} <$ 0.3 V	H	X	?
	X	L	?
$V_{ID} \leq -0.3$ V	H	X	L
	X	L	L
X	L	H	Z

H = high level
L = low level
X = irrelevant
? = indeterminate
Z = high-impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, A or B inputs . . . . . ±15 V
Differential input voltage (see Note 2) . . . . . ±15 V
Enable input voltage . . . . . 7 V
Low-level output current . . . . . 50 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Differential input voltage, V_{ID}			±12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended range of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage					300	mV
V_{T-}	Negative-going threshold voltage			−300‡			mV
V_{hys}	Hysteresis§				120		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 300 mV,	I_{OH} = −400 μA	2.7	3.6		V
V_{OL}	Low-level output voltage	V_{ID} = −300 mV	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_{CC} = 5.25 V	V_O = 2.4 V			20	μA
			V_O = 0.4 V			−20	
I_I	Line input current	Other input at 0 V, See Note 3	V_I = 15 V		0.7	1.2	mA
			V_I = −15 V		−1.0	−1.7	
I_{IH}	High-level enable-input current		V_{IH} = 2.7 V			20	μA
			V_{IH} = 5.25 V			100	
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
	Input resistance			12	18		kΩ
I_{OS}	Short-circuit output current	V_{ID} = 3 V, See Note 4	V_O = 0,	−15	−78	−130	mA
I_{CC}	Supply current	Outputs disabled			22	35	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.
NOTES: 3. Refer to CCITT Recommendation V.10 and V.11 for exact conditions.
4. Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −2.5 V to 2.5 V, C_L = 15 pF, See Figure 2			15	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output				15	22	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PZL}	Output enable time to low level				11	25	
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PLZ}	Output disable time from low level				15	22	

PARAMETER MEASUREMENT INFORMATION

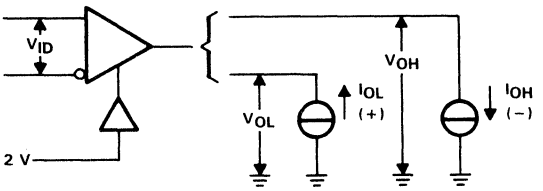
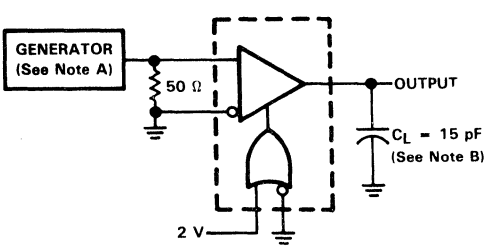
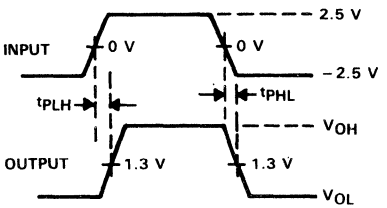


FIGURE 1. V_{OH}, V_{OL}



TEST CIRCUIT

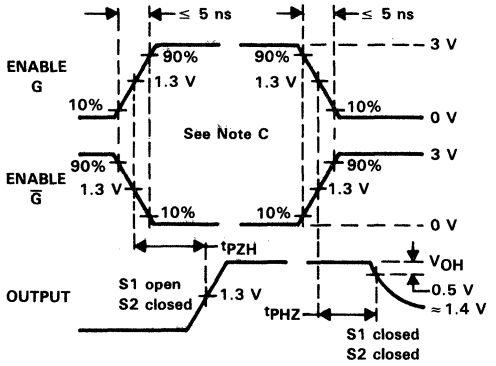


VOLTAGE WAVEFORMS

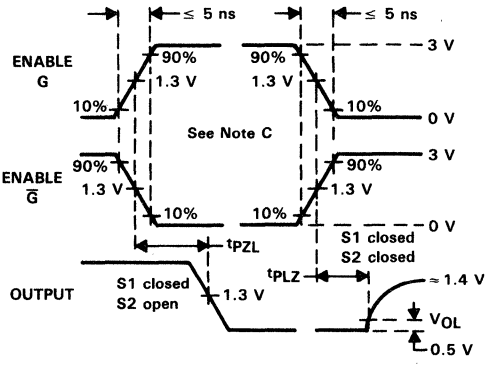
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_{out} = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

FIGURE 2. t_{PLH}, t_{PHL}

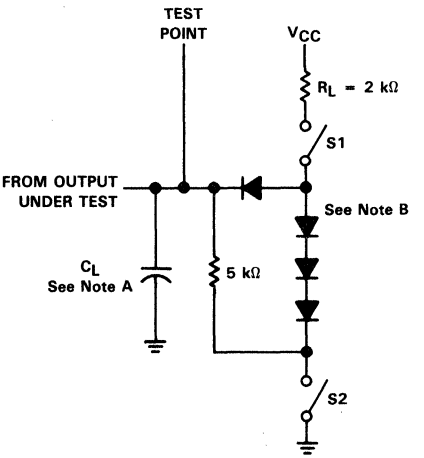
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS FOR t_{PHZ}, t_{PZH}



VOLTAGE WAVEFORMS FOR t_{PLZ}, t_{PZL}



LOAD CIRCUIT

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

FIGURE 3. t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL}

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

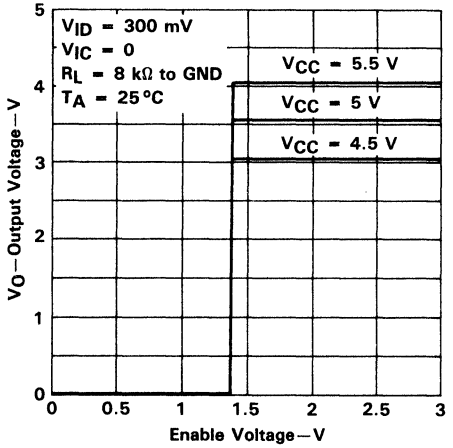


FIGURE 4

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

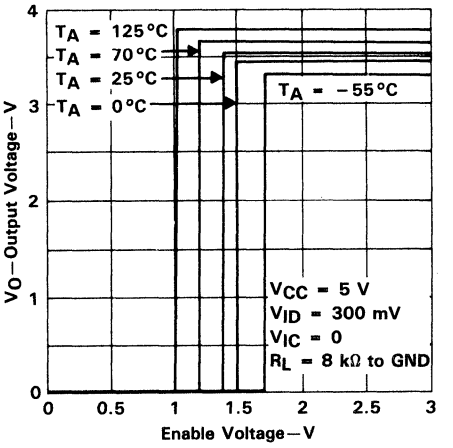


FIGURE 5

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

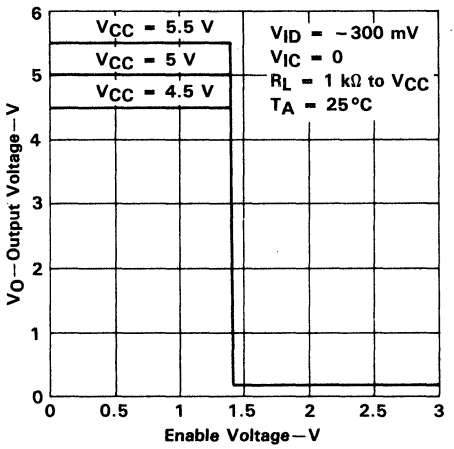


FIGURE 6

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

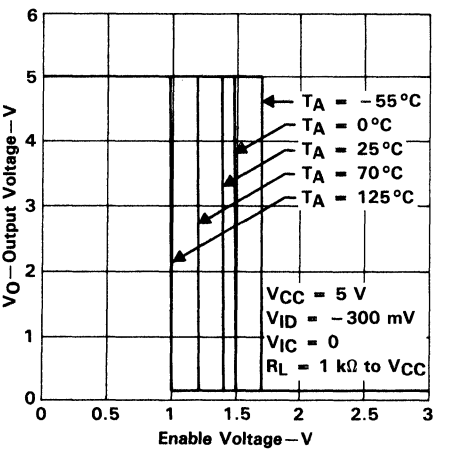


FIGURE 7

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

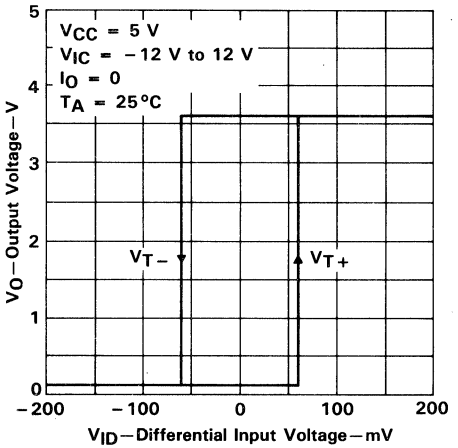


FIGURE 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

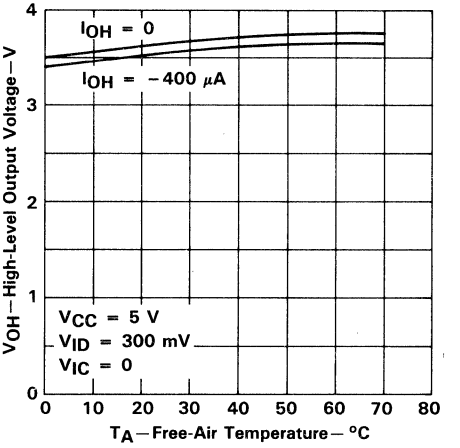


FIGURE 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

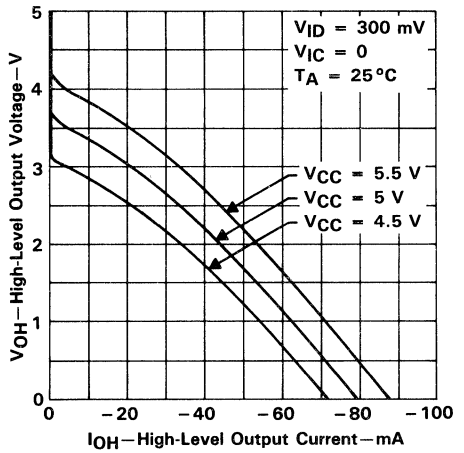


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

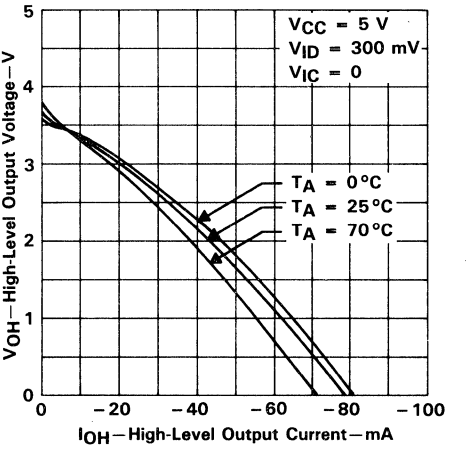


FIGURE 11

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

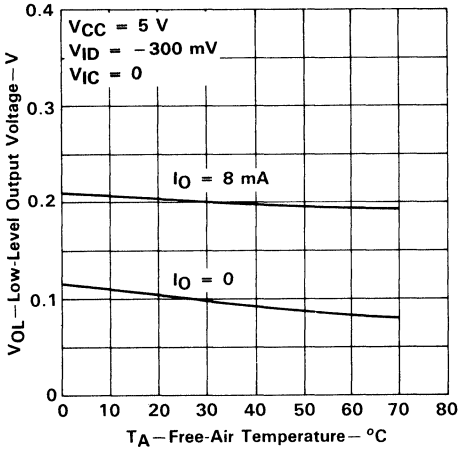


FIGURE 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

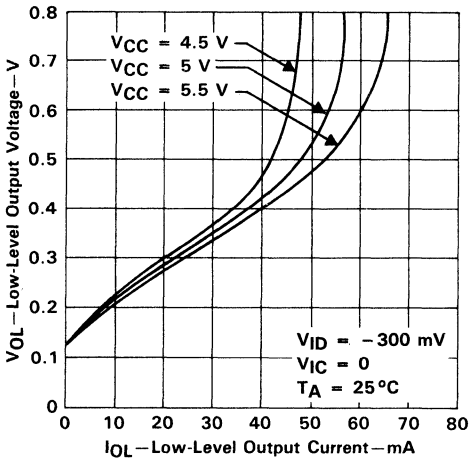


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

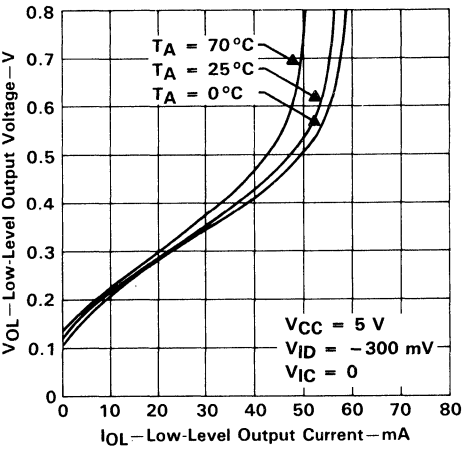


FIGURE 14

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

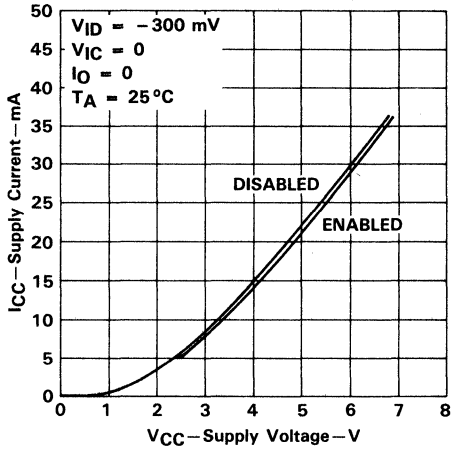


FIGURE 15

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

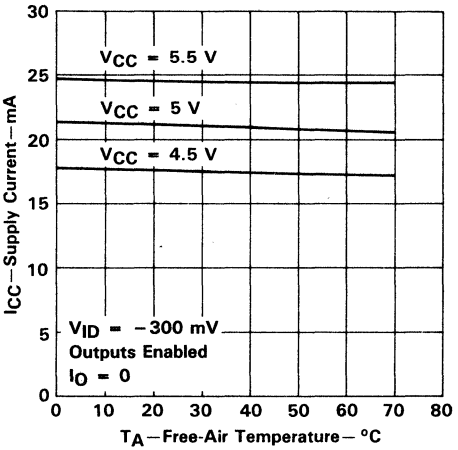


FIGURE 16

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

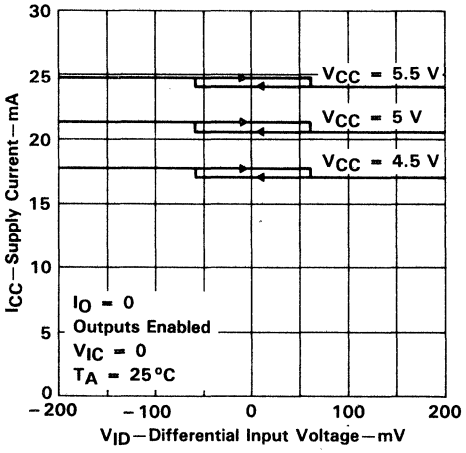


FIGURE 17

SUPPLY CURRENT
vs
FREQUENCY

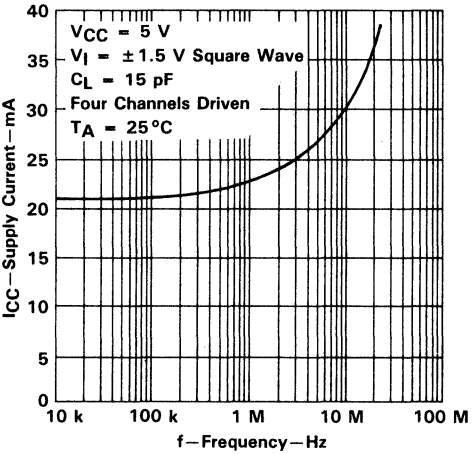


FIGURE 18

TYPICAL CHARACTERISTICS

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

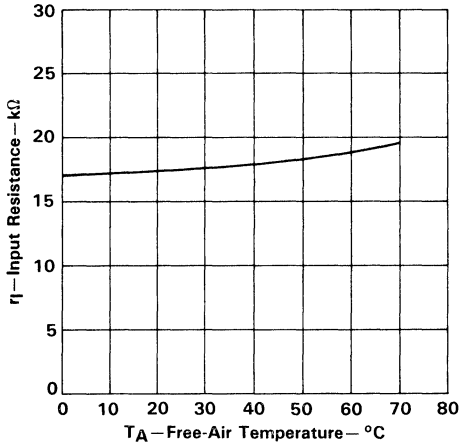


FIGURE 19

INPUT CURRENT
vs
INPUT VOLTAGE

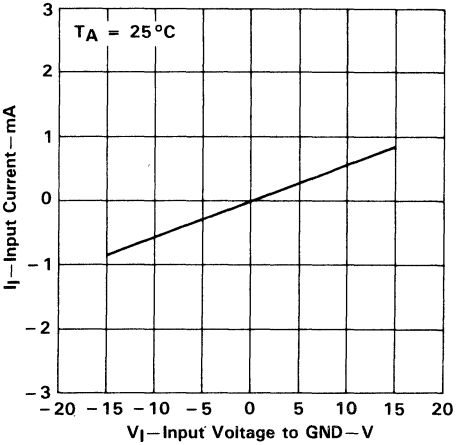


FIGURE 20

SWITCHING CHARACTERISTICS
vs
FREE-AIR TEMPERATURE

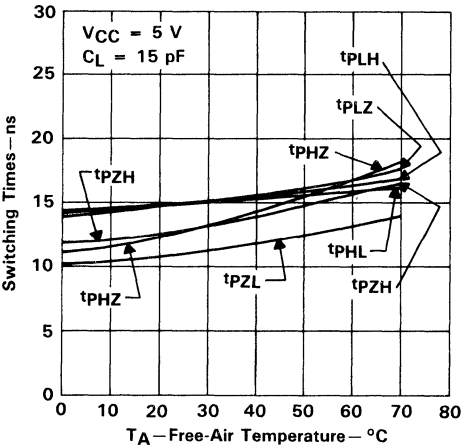


FIGURE 21

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

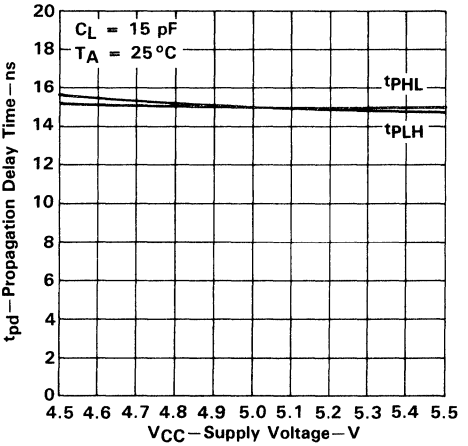


FIGURE 22

- **Meets CCITT Recommendations V.10, V.11, X.26, and X.27**
- **−7 V to 7 V Common-Mode Range with 300-mV Sensitivity**
- **3-State TTL-Compatible Outputs**
- **High Input Impedance . . . 12 kΩ Min**
- **Input Hysteresis . . . 120 mV Typ**
- **Single 5-V Supply Operation**
- **Low Supply Current Requirement . . . 35 mA Max**
- **Improved Speed and Power Consumption Compared to MC3486**

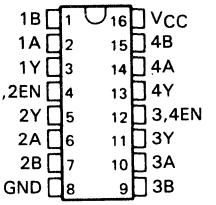
description

The SN75ALS199 is a monolithic quadruple line receiver with three-state outputs designed using Advanced Low-Power Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication, providing significantly less power consumption and permitting much higher data throughput than other designs. The device meets the specifications of CCITT Recommendations V.10, V.11, X.26 and X.27.

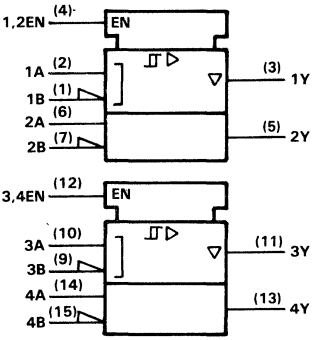
The SN75ALS199 features three-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open. The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ±300 mV over a common-mode input voltage range of ±7 V. It also features an active-high enable function for each of two receiver pairs. The SN75ALS199 is designed for optimum performance when used with the SN75ALS194 quadruple differential line driver.

The SN75ALS199 is characterized for operation from 0°C to 70°C.

D OR N PACKAGE
(TOP VIEW)

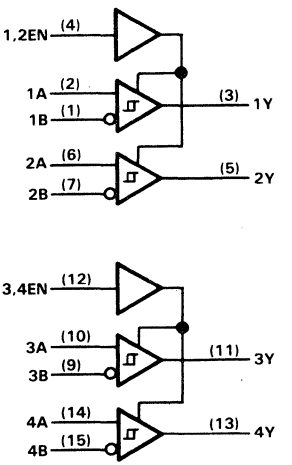


logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram

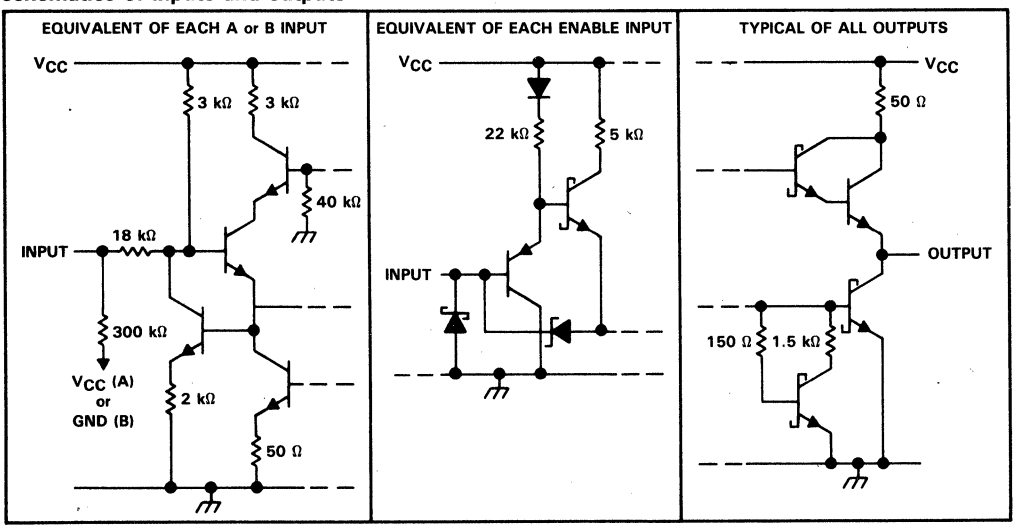


FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL A–B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.3$ V	H	X	H
	X	L	H
-0.3 V $< V_{ID} < 0.3$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.3$ V	H	X	L
	X	L	L
X	L	H	Z

H = high level
L = low level
X = irrelevant
? = indeterminate
Z = high-impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, A or B inputs, V_I . . . . . ±15 V
Differential input voltage (see Note 2) . . . . . ±15 V
Enable input voltage . . . . . 7 V
Low-level output current . . . . . 50 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Differential input voltage, V_{ID}			±12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage					300	mV
V_{T-}	Negative-going threshold voltage			−300‡			mV
V_{hys}	Hysteresis§				120		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 300 mV,	I_{OH} = −400 μA	2.7	3.6		V
V_{OL}	Low-level output voltage	V_{ID} = −300 mV	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance state output current	V_{IL} = 0.8 V, V_O = 2.7 V	V_{ID} = −3 V,			20	μA
		V_{IL} = 0.8 V, V_O = 0.5 V	V_{ID} = 3 V,			−20	
I_I	Line input current	Other input at 0 V, See Note 3	V_I = 15 V		0.7	1.2	mA
			V_I = −15 V		−1.0	−1.7	
I_{IH}	High-level enable-input current		V_{IH} = 2.7 V			20	μA
			V_{IH} = 5.25 V			100	
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
	Input resistance			12	18		kΩ
I_{OS}	Short-circuit output current	V_{ID} = 3 V, See Note 4	V_O = 0,	−15	−78	−130	mA
I_{CC}	Supply current	Outputs disabled			22	35	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.
NOTES: 3. Refer to CCITT Recommendations V.10 and V.11 for exact conditions.
4. Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = 0 V to 3 V, See Figure 2	C_L = 15 pF,		15	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output				15	22	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PZL}	Output enable time to low level				11	25	
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PLZ}	Output disable time from low level				15	22	

PARAMETER MEASUREMENT INFORMATION

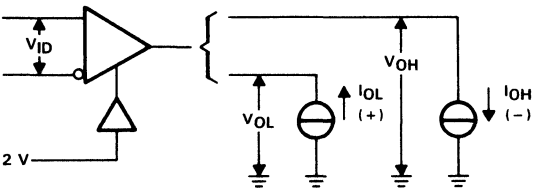
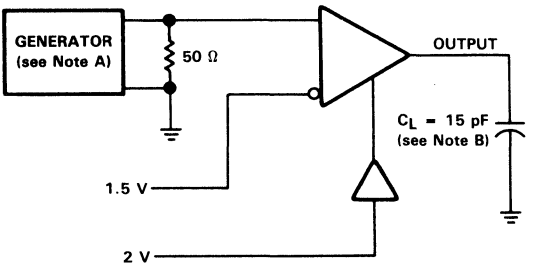
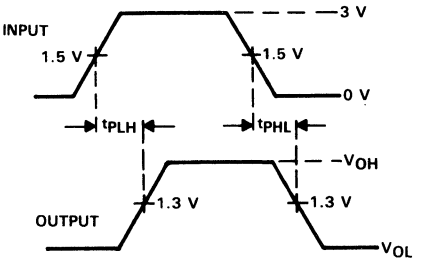


FIGURE 1. V_{OH}, V_{OL}



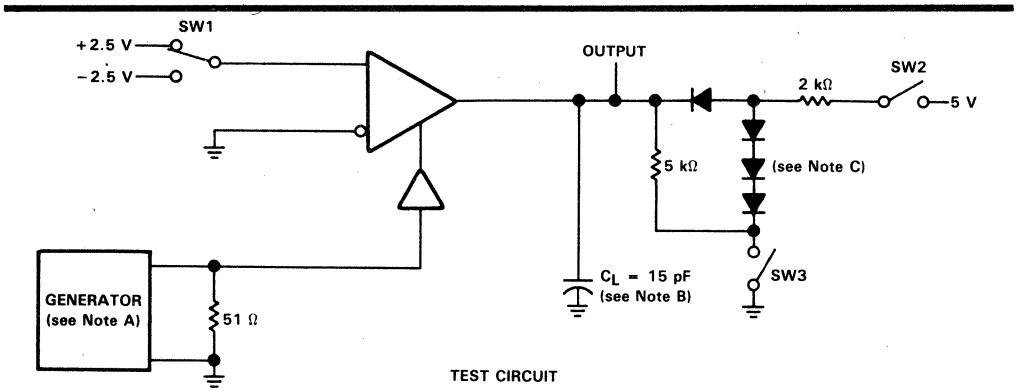
TEST CIRCUIT



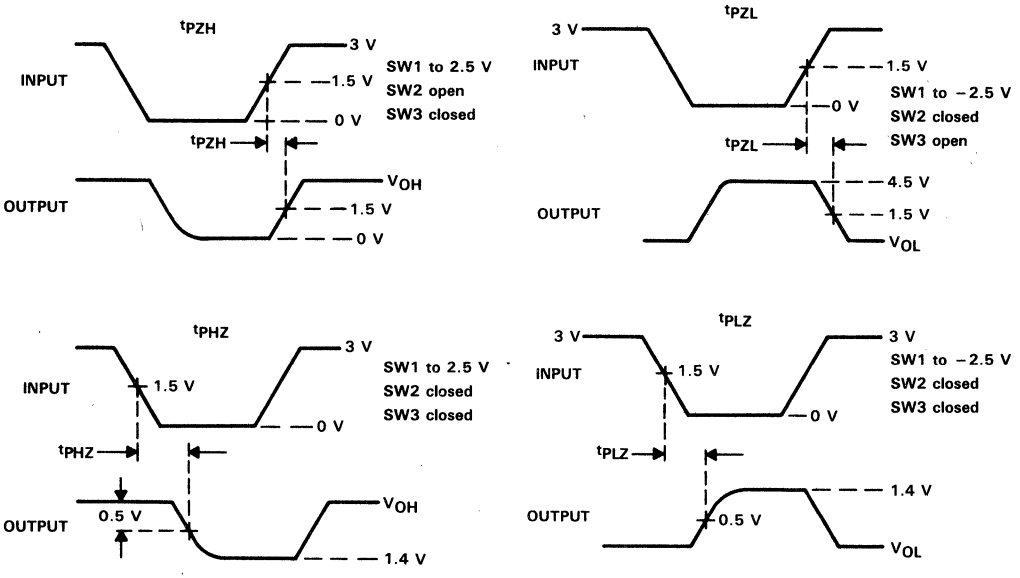
VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_{out} = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

FIGURE 2. PROPAGATION DELAY TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_{out} = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

FIGURE 3. ENABLE AND DISABLE TIMES

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

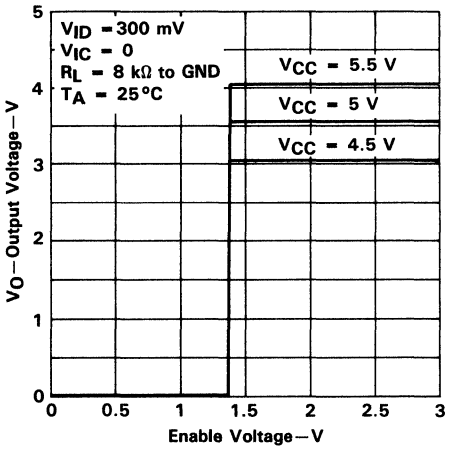


FIGURE 4

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

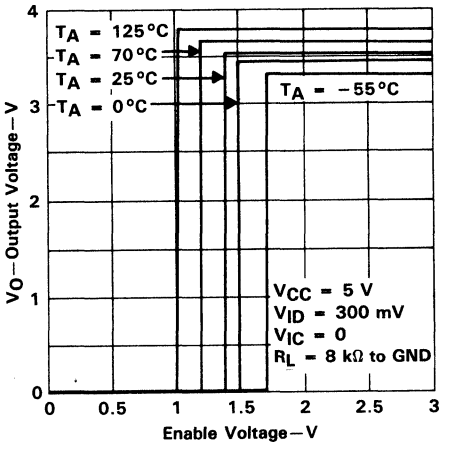


FIGURE 5

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

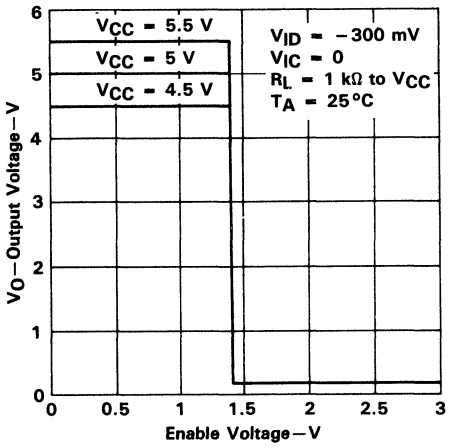


FIGURE 6

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

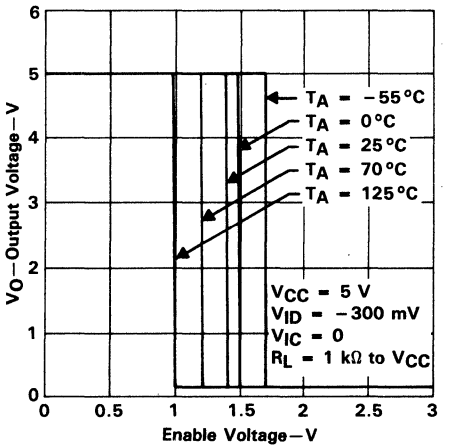


FIGURE 7

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

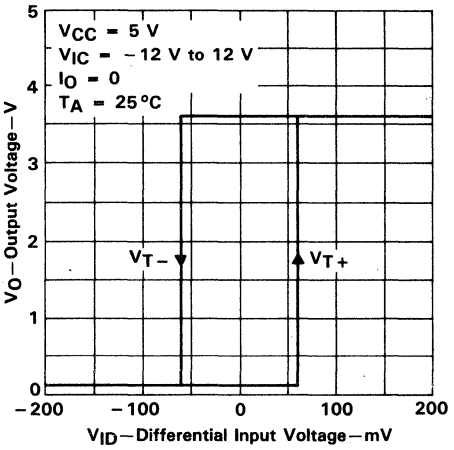


FIGURE 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

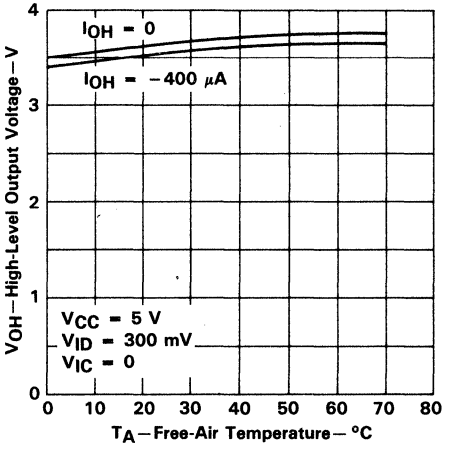


FIGURE 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

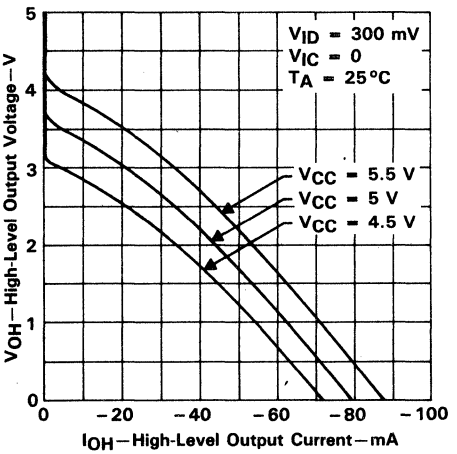


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

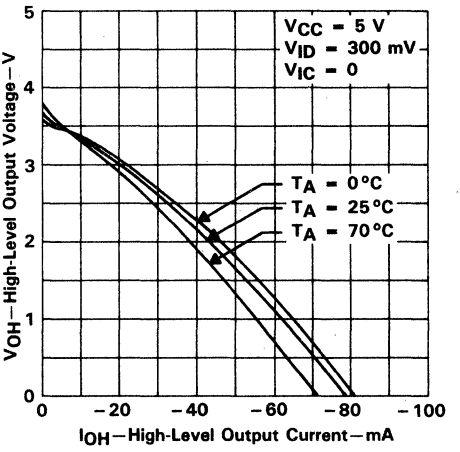


FIGURE 11

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

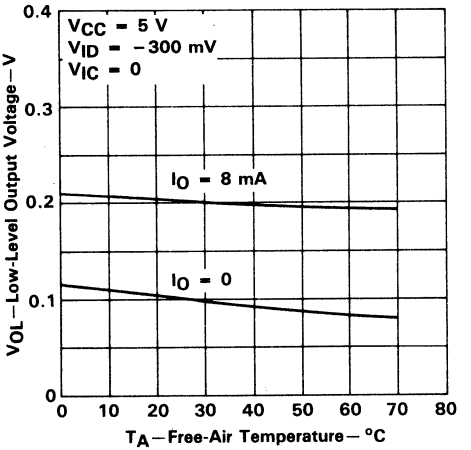


FIGURE 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

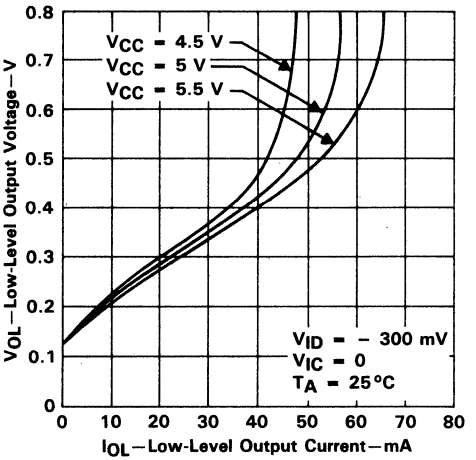


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

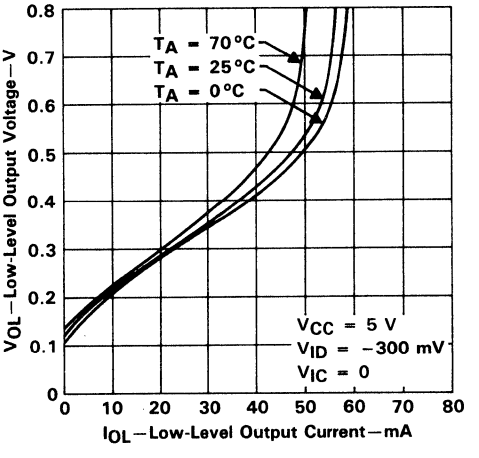


FIGURE 14

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

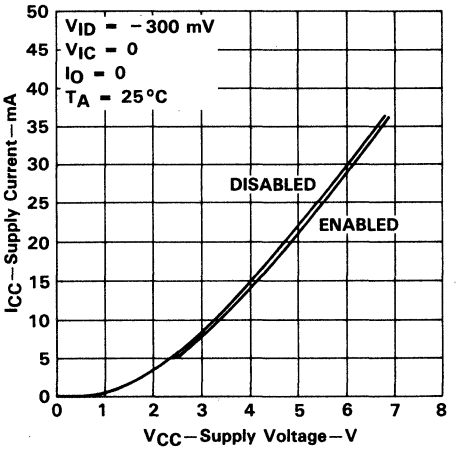


FIGURE 15

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

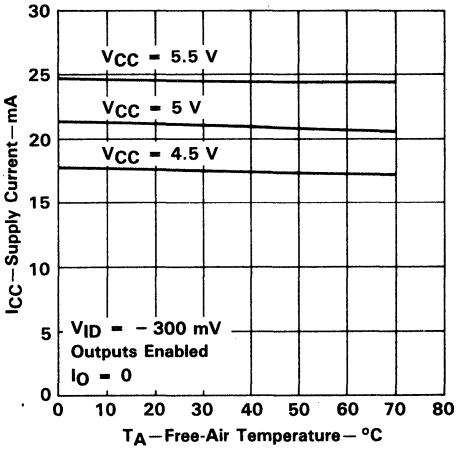


FIGURE 16

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

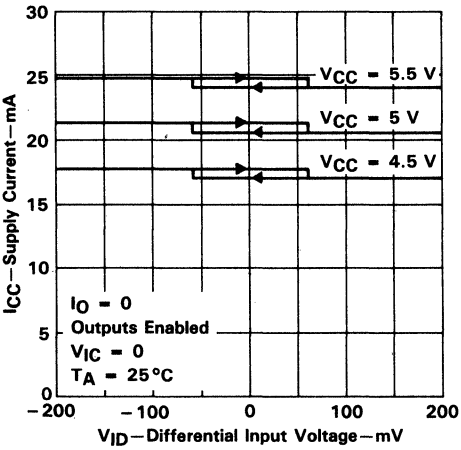


FIGURE 17

SUPPLY CURRENT
vs
FREQUENCY

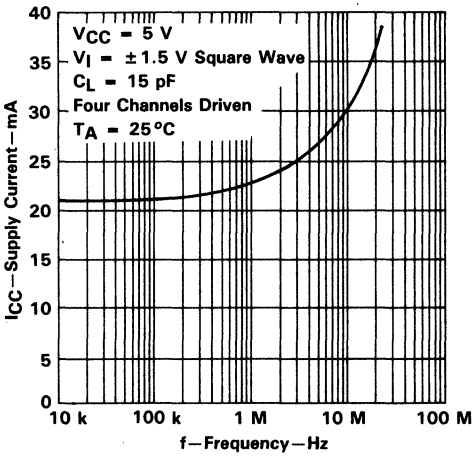


FIGURE 18

TYPICAL CHARACTERISTICS

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

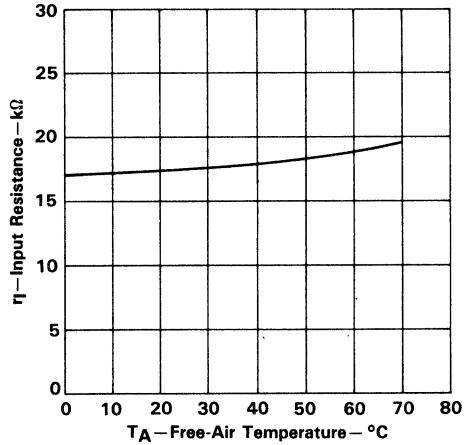


FIGURE 19

INPUT CURRENT
vs
INPUT VOLTAGE

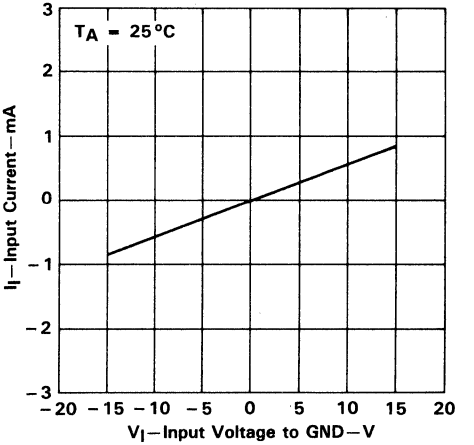


FIGURE 20

SWITCHING CHARACTERISTICS
vs
FREE-AIR TEMPERATURE

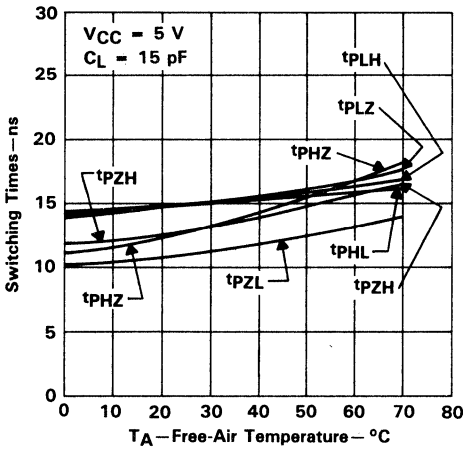


FIGURE 21

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

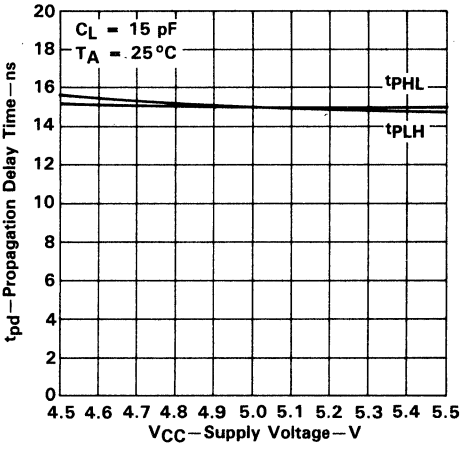
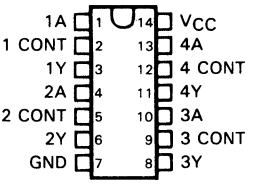


FIGURE 22

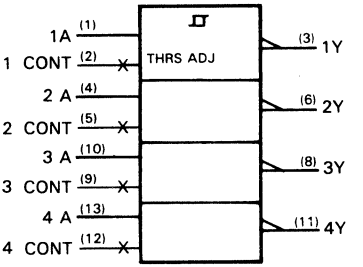
D3144, OCTOBER 1988—REVISED JULY 1990

- **Meets Standard EIA-232-D (Revision of RS-232-C)**
- **Low Supply Current . . . 420 μA Typ**
- **Preset On-Chip Input Noise Filter**
- **Built-in Input Hysteresis**
- **Response and Threshold Control Inputs**
- **Push-Pull Outputs**
- **ESD Protection Exceeds 1000 V Per MIL-STD-883C, Method 3015**
- **Functionally Interchangeable and Pin Compatible with Texas Instruments SN75189/SN75189A, Motorola MC1489/MC489A, and National Semiconductor DS14C88A**

D, DB, OR N PACKAGE
(TOP VIEW)

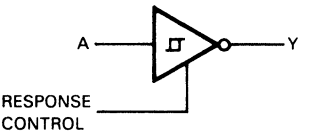


logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (each receiver)



description

The SN65C189, SN65C189A, SN75C189, and SN75C189A are low-power bipolar quadruple line receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). These devices have been designed to conform with Standard ANSI/EIA-232-D-1986, which supersedes RS-232-C.

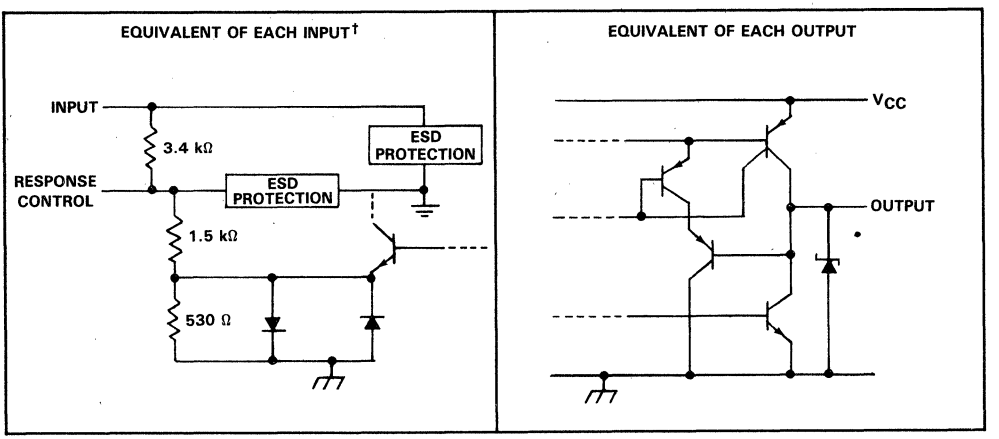
The SN65C189 and SN75C189 have a 0.25 V typical hysteresis compared with 1 V for the SN65C189A and SN75C189A. Each receiver has provision for adjustment of the overall input threshold levels. This is achieved by choosing external series resistors and voltages to provide bias levels for the response control pins. The output is in the high logic state if the input is left open circuited or shorted to ground.

These devices have an on-chip filter that rejects input pulses of shorter than 1-μs minimum duration. An external capacitor may be connected from the control pins to ground to provide further input noise filtering for each receiver.

The SN65C189, SN75C189, SN65C189A, and SN75C189A have been designed using low-power techniques in a bipolar technology. In most applications, these receivers will interface to single inputs of peripheral devices such as UARTs, ACEs, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN65C189, SN75C189, SN65C189A, and SN75C189A outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS or 74F logic families.

The SN65C189 and SN65C189A are characterized for operation from −40°C to 85°C. The SN75C189 and SN75C189A are characterized for operation from 0°C to 70°C.

schematic of inputs and outputs



†All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage range . . . . . −30 V to 30 V
Output voltage range . . . . . −0.3 V to V_{CC} + 0.3 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN65C189, SN65C189A . . . . . −40°C to 85°C
SN75C189, SN75C189A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW
DB	525 mW	4.2 mW/°C	273 mW
N	1150 mW	9.2 mW/°C	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	6	V
Input voltage, V_I (see Note 2)		−25		25	V
High-level output current, I_{OH}				−3.2	mA
Low-level output current, I_{OL}				3.2	mA
Response control current				±1	mA
Operating free-air temperature, T_A	SN65C189, SN65C189A	−40		85	°C
	SN75C189, SN75C189A	0		70	

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if −10 V is a maximum, the typical value is a more negative voltage.

electrical characteristics over recommended free-air temperature range, V_{CC} = 5 V ±10% (unless otherwise noted) (See Note 3)

PARAMETERS			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold level	SN75C189	See Figure 1		1		1.5	V
		SN75C189A			1.6		2.25	
V_{T-}	Negative-going threshold level	SN75C189	See Figure 1		0.75		1.25	V
		SN75C189A			0.75	1	1.25	
V_{hys}	Input hysteresis	SN75C189	See Figure 1		0.15	0.33		V
		SN75C189A			0.65	0.97		
V_{OH}	High-level output voltage		V_{CC} = 4.5 V to 6 V, I_{OH} = −20 μA	V_I = 0.75 V,	3.5			V
			V_I = 0.75 V,	I_{OH} = −3.2 mA	2.5			
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V to 6 V, I_{OL} = 3.2 mA	V_I = 3 V,			0.4	V
I_{IH}	High-level input current		See Figure 2	V_I = 25 V	3.6		8.3	mA
				V_I = 3 V	0.43		1	
I_{IL}	Low-level input current		See Figure 2	V_I = −25 V	−3.6		−8.3	mA
				V_I = −3 V	−0.43		−1	
I_{OS}	Short-circuit output current		See Figure 3				−35	mA
I_{CC}	Supply current		V_I = 5 V, No load, See Figure 2			420	700	μA

†All typical values are at T_A = 25°C.
NOTE 3: All characteristics are measured with response control terminal open.

switching characteristics at T_A = 25°C, V_{CC} = 5 V ±10%

PARAMETERS		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF,	See Figure 4			6	μs
t_{PHL}	Propagation delay time high-to-low-level output	C_L = 50 pF,	See Figure 4			6	μs
t_{TLH}	Transition time, high-to-low-level output‡	C_L = 50 pF,	See Figure 4			500	ns
t_{THL}	Transition time, high-to-low-level output‡	C_L = 50 pF,	See Figure 4			300	ns
$t_{w(N)}$	Duration of longest pulse rejected as noise§	C_L = 50 pF,	See Figure 4	1		6	μs

‡Measured between 10% and 90% points of output waveform.
§The intent of this specification is that any input pulse of less than 1 μs will have no effect on the output, and any pulse duration of greater than 6 μs will cause the output to change state twice. Reaction to a pulse duration between 1 μs and 6 μs is uncertain.

PARAMETER MEASUREMENT INFORMATION†

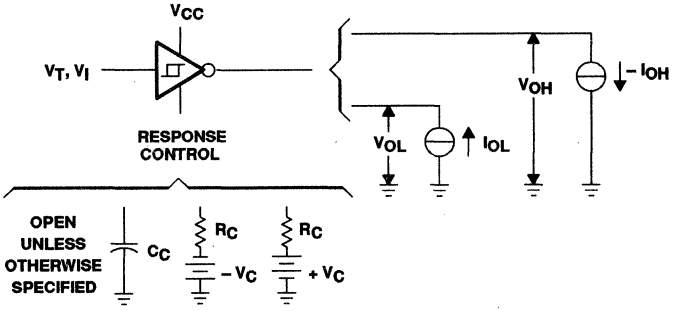
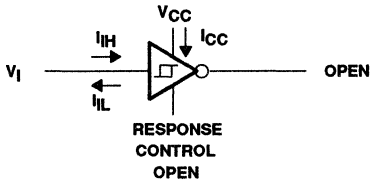


FIGURE 1. V_{T+}, V_{T-}, V_{OH}, V_{OL}



I_{CC} is tested for all four receivers simultaneously

FIGURE 2. I_{IH}, I_{IL}, I_{CC}

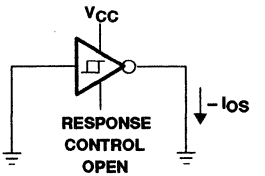
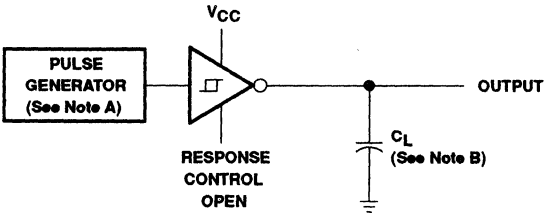


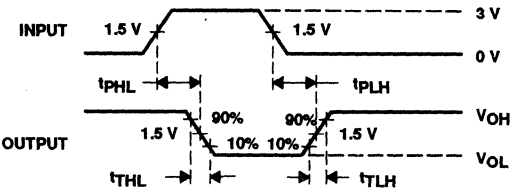
FIGURE 3. I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, t_W = 25 μs.
B. C_L includes probe and jig capacitances.

FIGURE 4. SWITCHING TIMES

TYPICAL CHARACTERISTICS

SN75C189
POSITIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

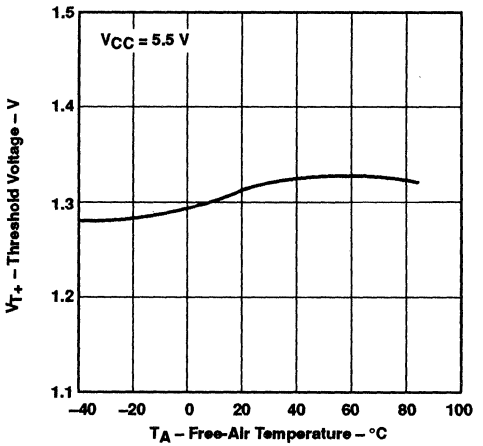


FIGURE 5

SN75C189A
POSITIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

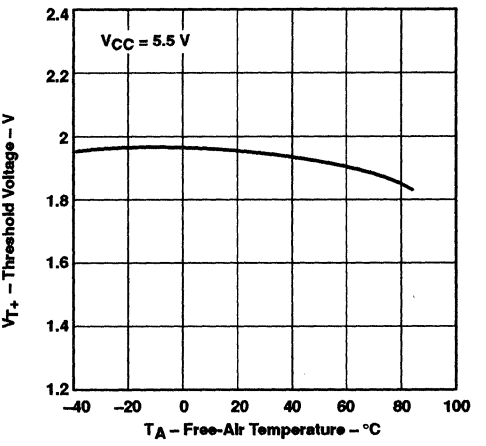


FIGURE 6

SN75C189
NEGATIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

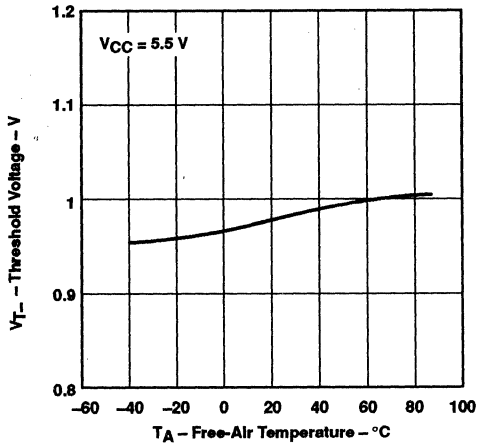


FIGURE 7

SN75C189A
NEGATIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

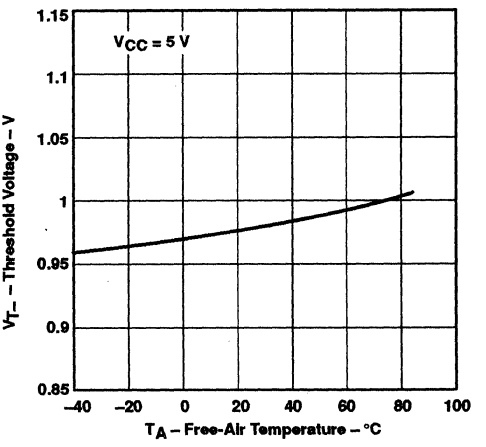


FIGURE 8

TYPICAL CHARACTERISTICS

SN75C189
INPUT HYSTERESIS
vs
FREE-AIR TEMPERATURE

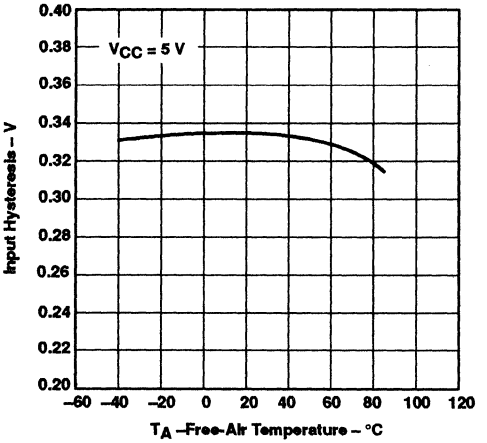


FIGURE 9

SN75C189A
INPUT HYSTERESIS
vs
FREE-AIR TEMPERATURE

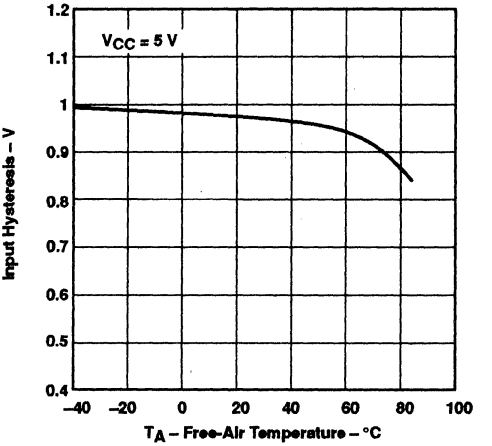


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

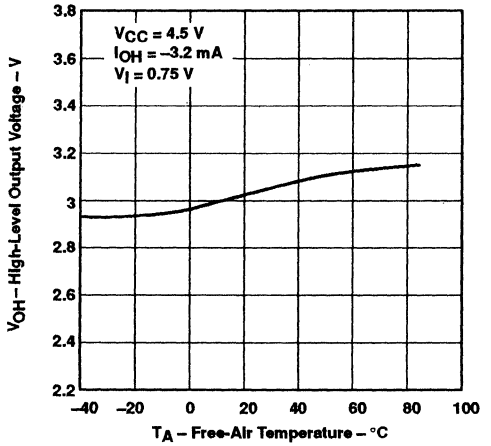


FIGURE 11

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

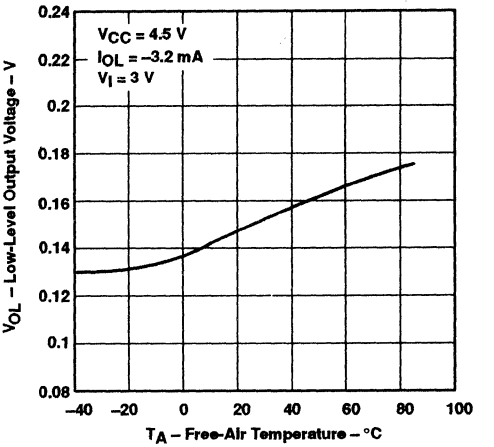


FIGURE 12

TYPICAL CHARACTERISTICS

SN75C189
HIGH-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE

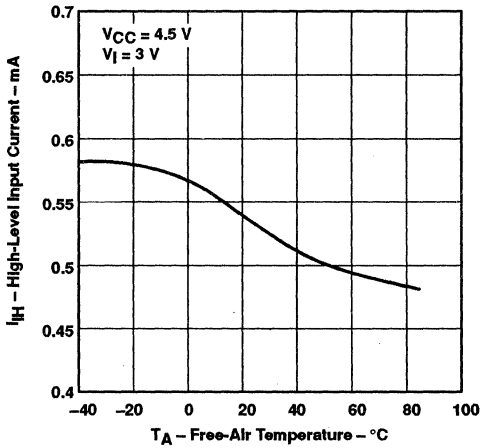


FIGURE 13

SN75C189A
HIGH-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE

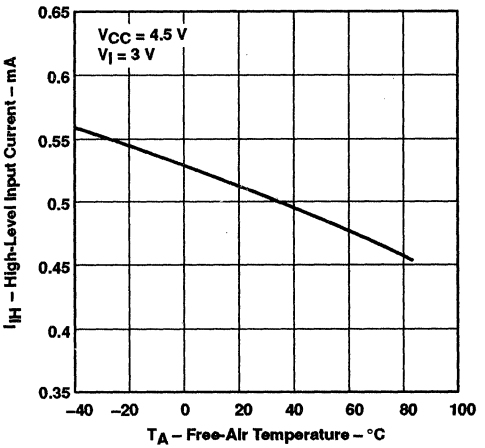


FIGURE 14

SN75C189
LOW-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE

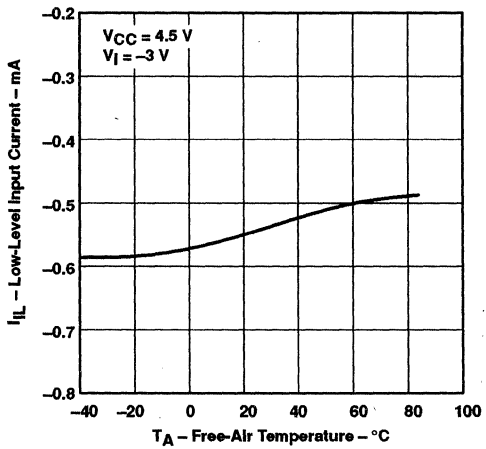


FIGURE 15

SN75C189A
LOW-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE

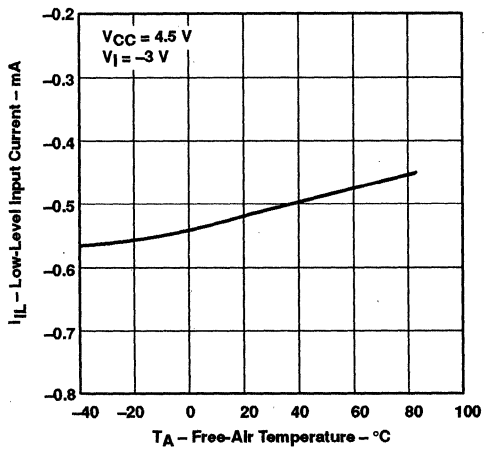


FIGURE 16

TYPICAL CHARACTERISTICS

HIGH-LEVEL SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

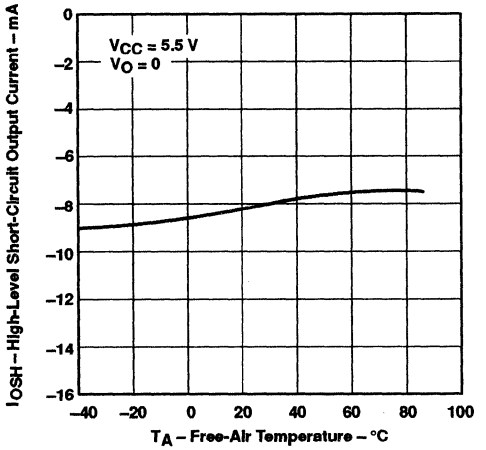


FIGURE 17

LOW-LEVEL SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

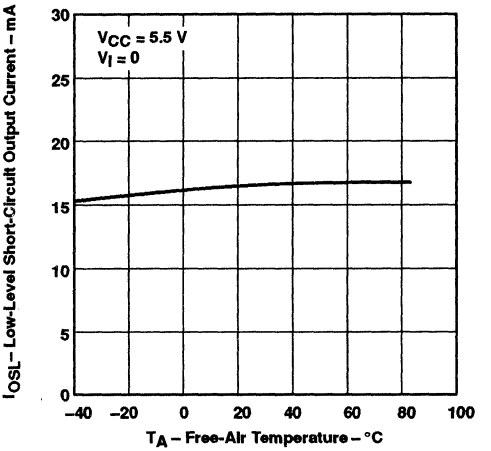


FIGURE 18

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

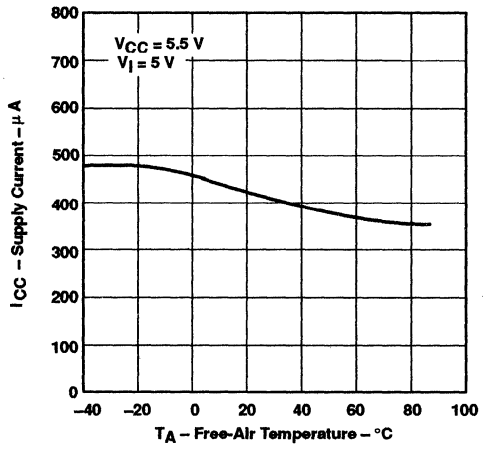


FIGURE 19

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

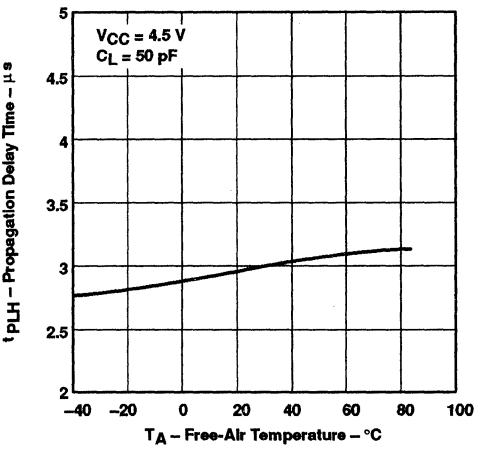


FIGURE 20

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME, HIGH-TO-LOW-LEVEL OUTPUT vs FREE-AIR TEMPERATURE

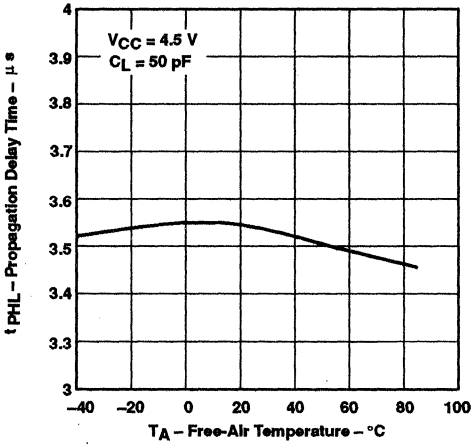


FIGURE 21

TRANSITION TIME, LOW-TO-HIGH-LEVEL vs FREE-AIR TEMPERATURE

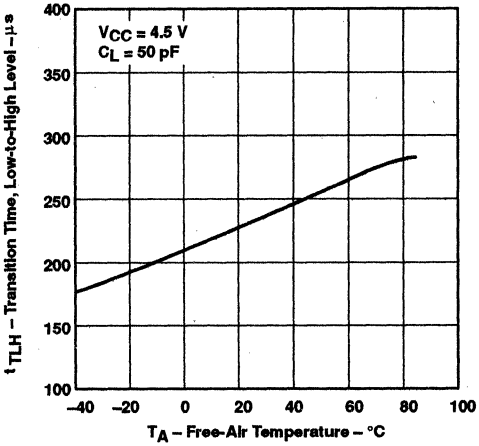


FIGURE 22

TRANSITION TIME, HIGH-TO-LOW-LEVEL vs FREE-AIR TEMPERATURE

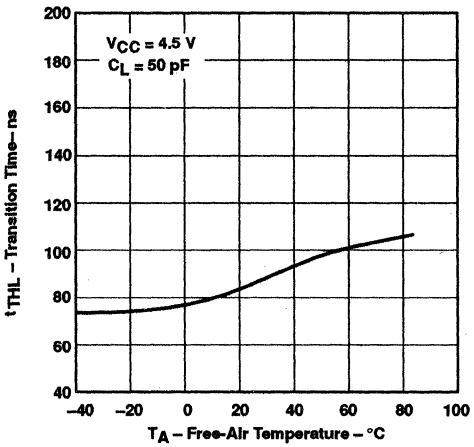


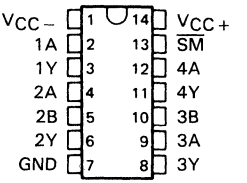
FIGURE 23

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D3472, JULY 1990

- Meets EIA-232-D (Revision of RS-232-C)
- Very Low Supply Current . . . 115 μA Typ
- Sleep Mode:
  3-State Outputs in High-Impedance State
  Ultra Low Supply Current . . . 17 μA Typ
- Improved Functional Replacement for:
  SN75188
  Motorola MC1488
  National Semiconductor DS14C88 and DS1488
- CMOS- and TTL-Compatible Data Inputs
- On-Chip Slew-Rate Limit . . . 30 V/μs
- Output Current Limit . . . 10 mA Typ
- Wide Supply Voltage Range . . . ±4.5 V to ±15 V
- ESD-Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015.2

D, DB, OR N PACKAGE
(TOP VIEW)



description

The SN65C198 and SN75C198 are monolithic low-power BI-MOS quadruple line drivers designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE) in conformance with the specifications of ANSI/EIA-232-D-1986.

The Sleep Mode input $\overline{SM}$ can be used to switch the outputs to high impedance, which avoids the transmission of corrupted data during power up and allows significant system power savings during data-off periods.

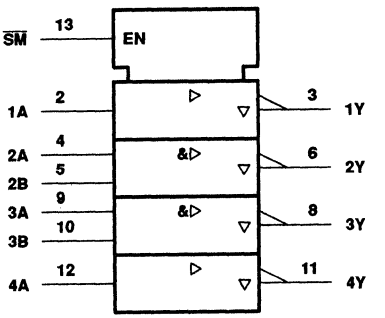
The SN65C198 is characterized for operation from −40°C to 85°C. The SN75C198 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{SM}$	A	B	Y
H	H	H	L
H	L	X	H
H	X	L	H
L	X	X	Z

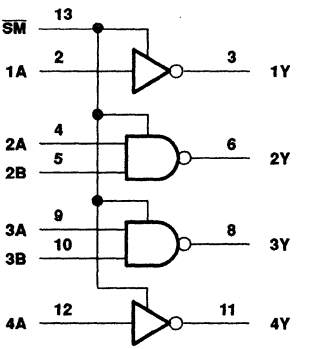
H = high level, L = low level,
X = irrelevant,
Z = high-impedance

logic symbol†

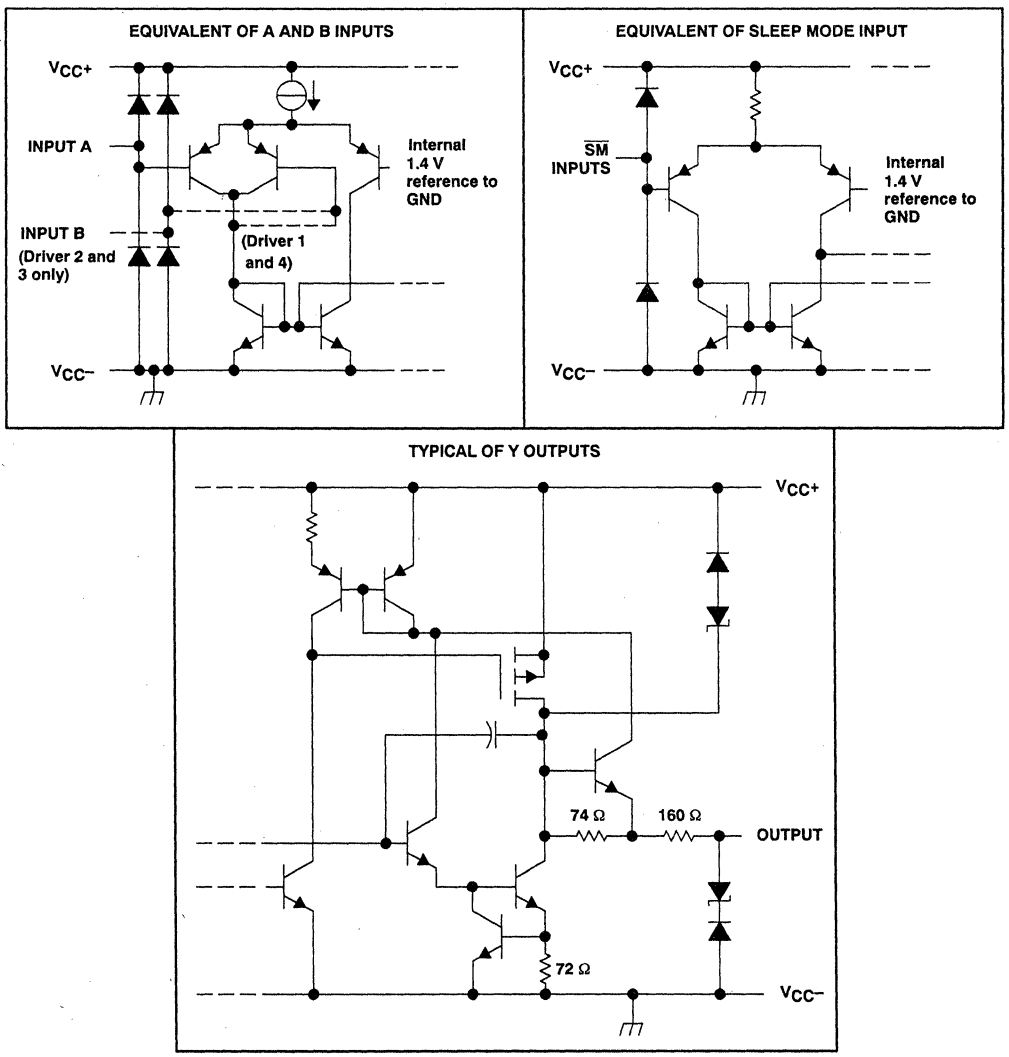


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC-} . . . . . −15 V
Input voltage range . . . . . −15 V to 15 V
Output voltage range . . . . . V_{CC-} −6 V to V_{CC+} + 6 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN65C198 . . . . . −40°C to 85°C
SN75C198 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW
DB	525 mW	4.2 mW/°C	273 mW
N	1150 mW	9.2 mW/°C	598 mW

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}			4.5	12	15	V
Supply voltage, V_{CC-}			−4.5	−12	−15	V
Input voltage, V_I (see Note 2)			V_{CC-} +2		V_{CC+}	V
High-level input voltage, V_{IH}			2			V
Low-level input voltage, V_{IL}	A and B inputs				0.8	V
	$\overline{SM}$ input				0.6	
Operating free-air temperature, T_A		SN65C198	−40		85	°C
		SN75C198	0		70	

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if −10 V is a maximum, the typical value is a more negative voltage.

electrical characteristics over recommended free-air temperature range, $V_{CC\pm}$ = ±12 V, $\overline{SM}$ at 2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 KΩ	$V_{CC\pm}$ = ±5 V	4			V
			$V_{CC\pm}$ = ±12 V	10			
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 2 V, R_L = 3 kΩ	$V_{CC\pm}$ = ±5V			−4	V
			$V_{CC\pm}$ = ±12V			−10	
I_{IH}	High-level input current	V_I = 5 V				10	μA
I_{IL}	Low-level input current	V_I = 0				−10	μA
I_{OZ}	High-impedance state output current	$\overline{SM}$ at 0.6 V	V_O = 12 V, $V_{CC\pm}$ = ±12 V			100	μA
			V_O = −12 V, $V_{CC\pm}$ = ±12 V			−100	
I_{OSH}	High-level short-circuit output current‡	V_I = 0.8 V,	V_O = 0 or V_{CC-}	−4.5	−10	−19.5	mA
I_{OSL}	Low-level short-circuit output current‡	V_I = 2 V,	V_O = 0 or V_{CC+}	4.5	10	19.5	mA
r_o	Output resistance with power off	$V_{CC\pm}$ = 0,	V_O = −2 V to 2 V	300			Ω
I_{CC+}	Supply current from V_{CC+}	A and B inputs at 0.8 V or 2 V, no load	$V_{CC\pm}$ = ±5 V		90	160	μA
			$V_{CC\pm}$ = ±12 V		95	160	
		A and B inputs at 0.8 V or 2 V, R_L = 3 kΩ, $\overline{SM}$ at 0.6 V	$V_{CC\pm}$ = ±5 V		17	40	
			$V_{CC\pm}$ = ±12 V		17	40	
I_{CC-}	Supply current from V_{CC-}	A and B inputs at 0.8 V or 2 V, no load	$V_{CC\pm}$ = ±5 V		−90	−160	μA
			$V_{CC\pm}$ = ±12 V		−95	−160	
		A and B inputs at 0.8 V or 2 V, R_L = 3 kΩ, $\overline{SM}$ at 0.6 V	$V_{CC\pm}$ = ±5 V		−17	−40	
			$V_{CC\pm}$ = ±12 V		−17	−40	

†All typical values are at T_A = 25°C.
‡Not more than one output should be shorted at a time.
NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if −10 V is a maximum, the typical value is a more negative voltage.

switching characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output§	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 1			3	μs
t_{PHL}	Propagation delay time, high-to-low-level output§				3.5	μs
t_{TLH}	Transition time, low-to-high-level output¶		0.53	1	3.2	μs
t_{THL}	Transition time, high-to-low-level output¶		0.53	1	3.2	μs
t_{TLH}	Transition time, low-to-high-level output#	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 2		1.5		μs
t_{THL}	Transition time, high-to-low-level output#			1.5		μs
t_{PZH}	Output enable time to high level	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3			50	μs
t_{PHZ}	Output disable time from high level				10	μs
t_{PZL}	Output enable time to low level	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 4			15	μs
t_{PLZ}	Output disable time from low level				10	μs
SR	Output slew rate#	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF	6	15	30	V/μs

†All typical values are at T_A = 25°C.
§t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate and are measured at the 50% points.
¶Measured between 10% and 90% points of output waveform.
#Measured between 3-V and −3-V points of output waveform.

PARAMETER MEASUREMENT INFORMATION

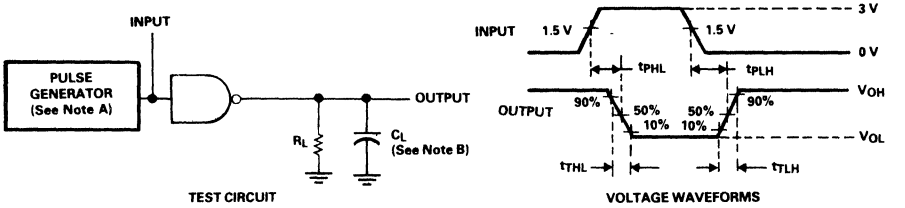


FIGURE 1. PROPAGATION AND TRANSITION TIMES

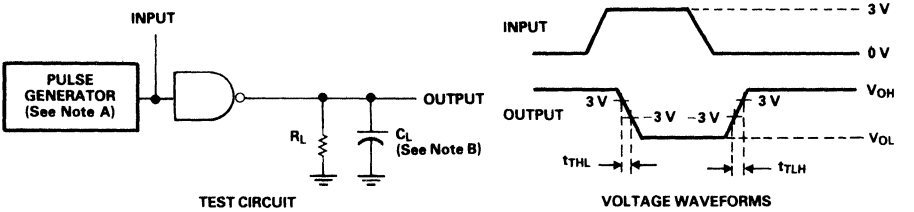


FIGURE 2. PROPAGATION AND TRANSITION TIMES

NOTE: A. The pulse generator has the following characteristics: t_W = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, t_r = t_f ≤ 50 ns.
B. C_L includes probe and jig capacitance.

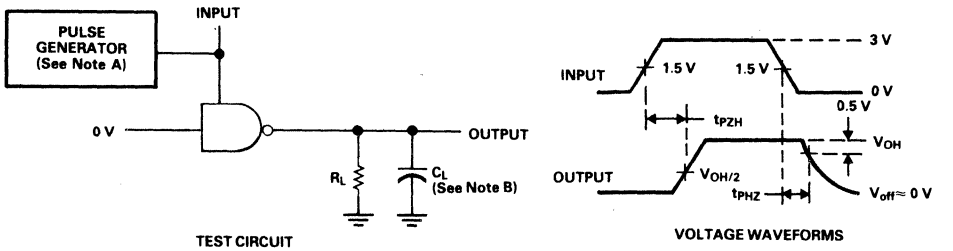


FIGURE 3. DRIVER ENABLE AND DISABLE TIMES

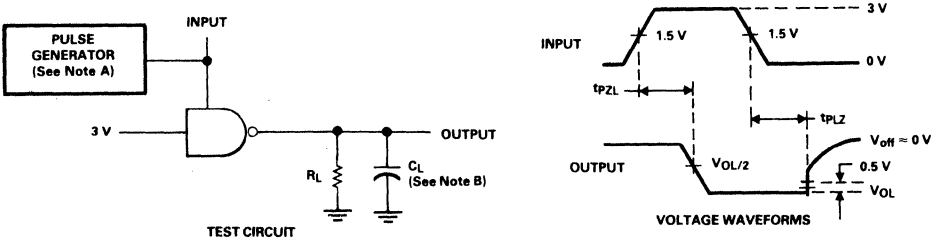


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

NOTE: A. The pulse generator has the following characteristics: t_W = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, t_r = t_f ≤ 50 ns.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

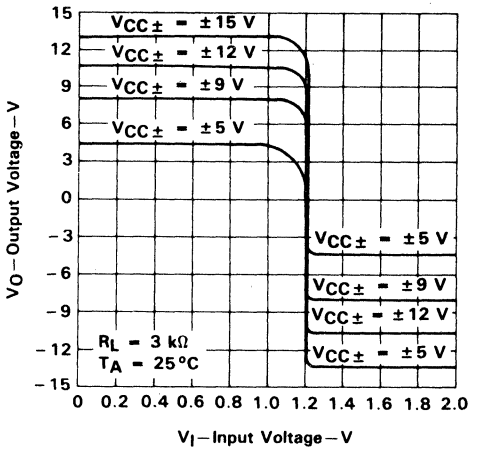


FIGURE 2

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

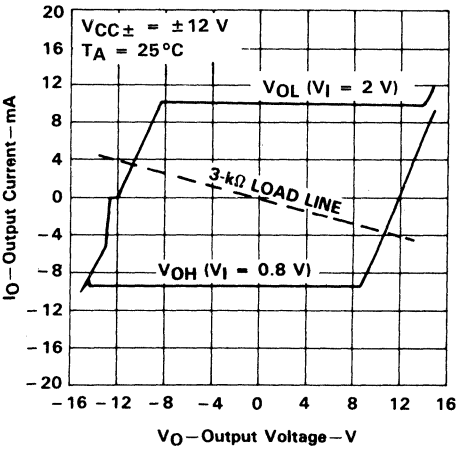


FIGURE 3

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

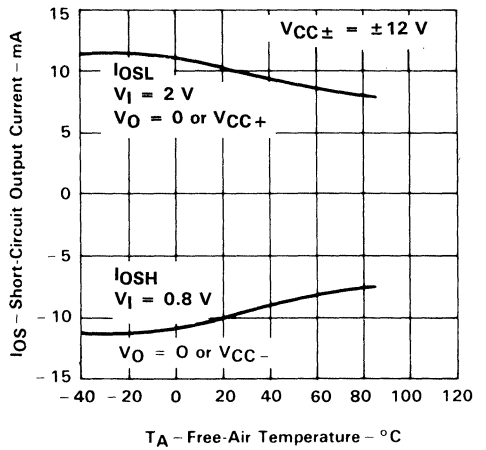


FIGURE 4

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

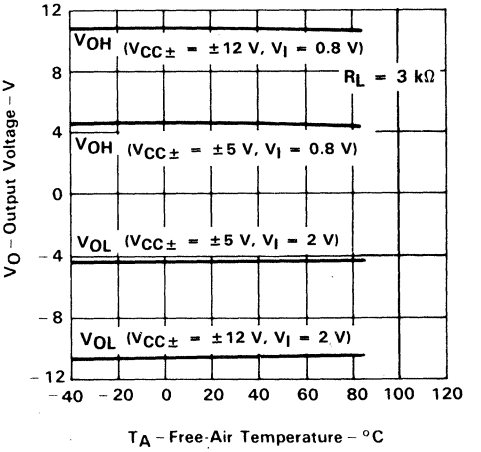


FIGURE 5

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

INPUT CURRENT
vs
FREE-AIR TEMPERATURE

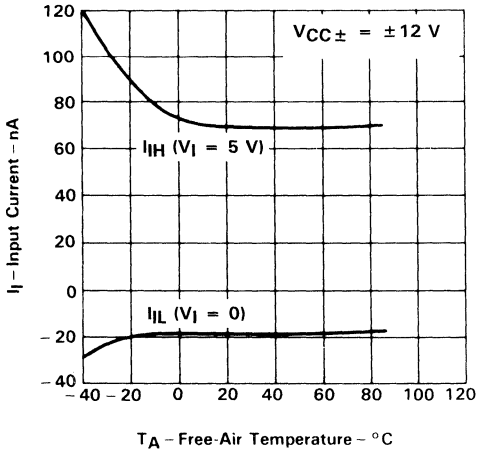


FIGURE 6

POWER-OFF OUTPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

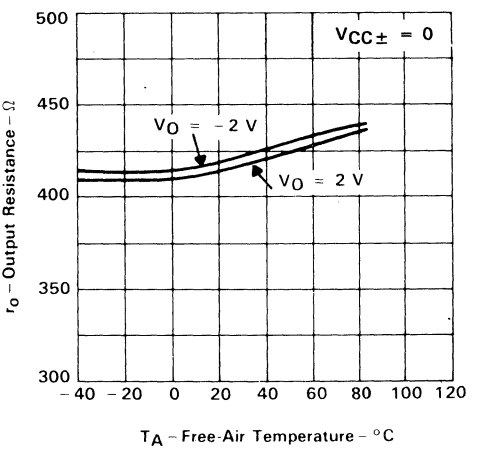


FIGURE 7

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

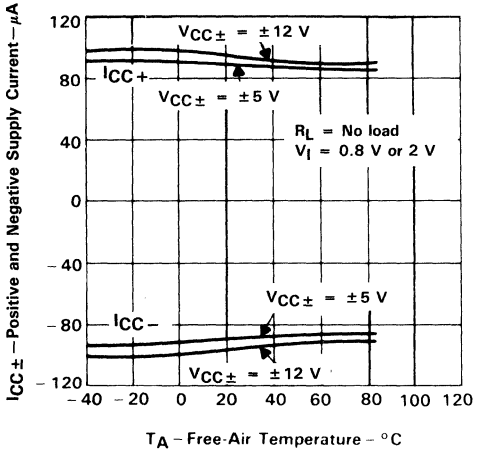


FIGURE 8

OUTPUT SLEW RATE
vs
FREE-AIR TEMPERATURE

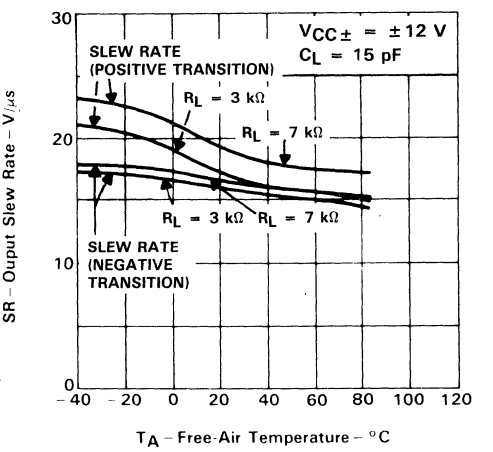


FIGURE 9

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

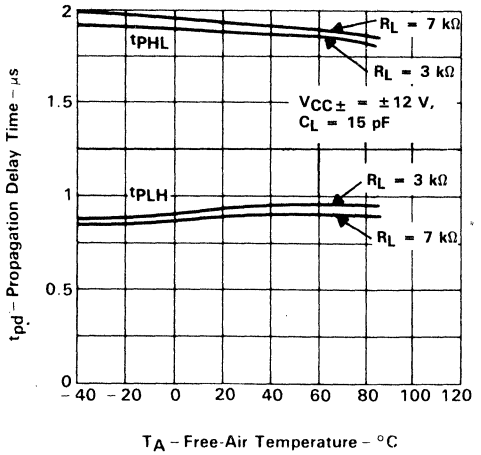


FIGURE 10

OUTPUT TRANSITION TIME
vs
FREE-AIR TEMPERATURE

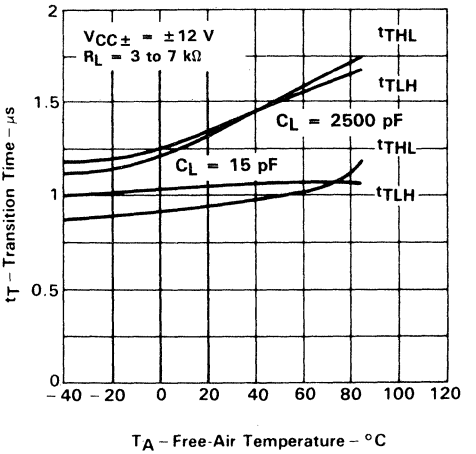


FIGURE 11

OUTPUT ENABLE TIME TO HIGH LEVEL
vs
FREE-AIR TEMPERATURE

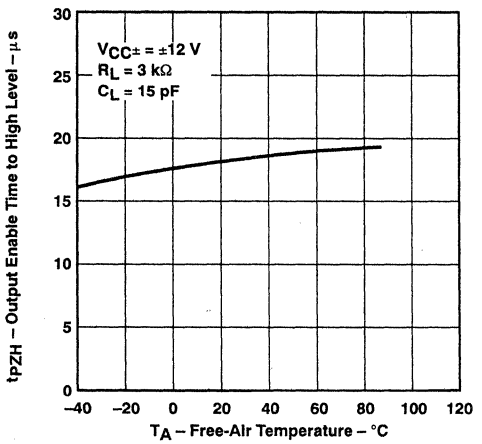


FIGURE 12

OUTPUT DISABLE TIME FROM HIGH LEVEL
vs
FREE-AIR TEMPERATURE

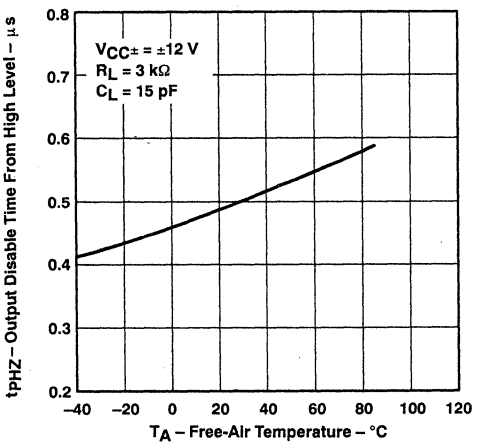


FIGURE 13

TYPICAL CHARACTERISTICS

OUTPUT ENABLE TIME TO LOW LEVEL
vs
FREE-AIR TEMPERATURE

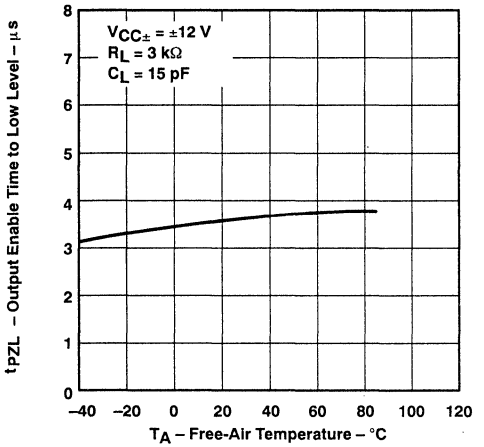


FIGURE 14

OUTPUT DISABLE TIME FROM LOW LEVEL
vs
FREE-AIR TEMPERATURE

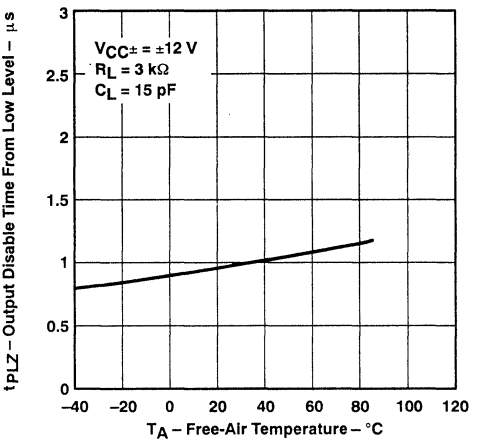
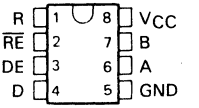


FIGURE 15

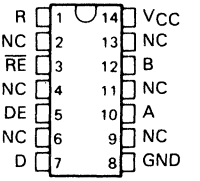
D3272, MARCH 1989

- Bidirectional Transceiver
- Suitable for Most EIA Standards RS-422-A and RS-485 Applications
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability . . . ±60 mA Max
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-V Supply
- Low Power Requirements

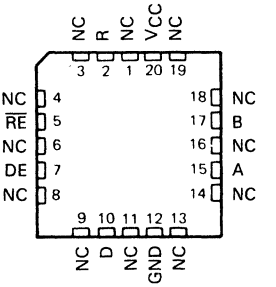
JG PACKAGE
(TOP VIEW)



W PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN95176B differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. These transceivers are suitable for most RS-422-A and RS-485 applications to the extent of the specified data sheet characteristics and operating conditions.

The SN95176B combines a 3-state differential line driver and a differential input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

FUNCTION TABLE (DRIVER)

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A – B	$\overline{RE}$	R
$V_{ID} \geq 0.2$ V	L	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

TEXAS INSTRUMENTS
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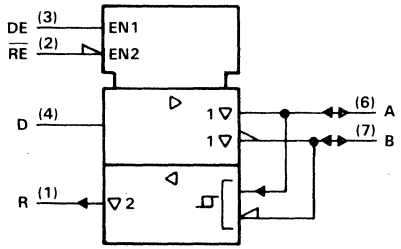
description (continued)

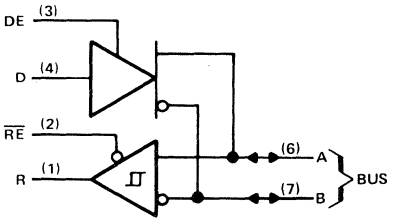
The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN95176B is characterized for operation from −40°C to 110°C.

logic symbol†

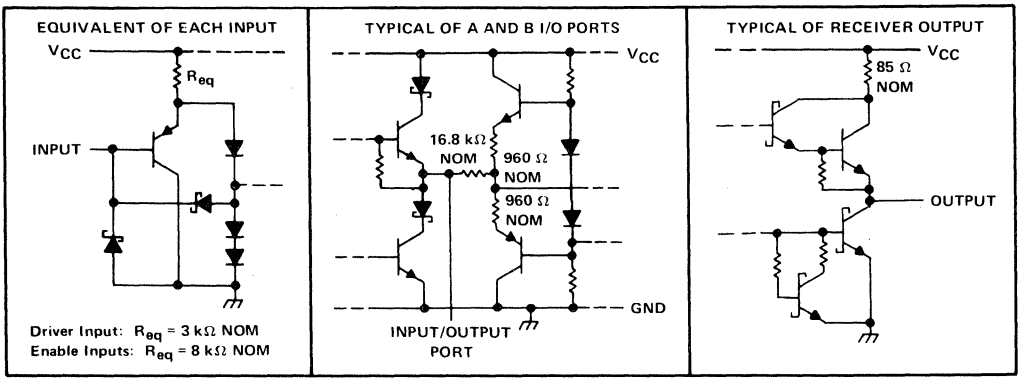


logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JG package.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage at any bus terminal . . . . . −10 V to 15 V
Enable input voltage . . . . . 5.5 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . −40°C to 110°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: JG or W package . . . . 300°C

NOTE 1: All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 110°C POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	440 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	336 mW
W	1000 mW	8.0 mW/°C	640 mW	520 mW	320 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		−40		110	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω,	See Figure 1	2			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 3			4		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§	R_L = 54 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Outputs disabled, See Note 4	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = 0				−150	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	70	mA
			Outputs disabled		26	35	

†The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡All typical values are at V_{CC} = 5 V and T_A = 25°C.
§$\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

NOTES: 3. See EIA Standard RS-485 Figure 3.5, Test Termination Measurement 2.
4. This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

driver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 54 Ω,	See Figure 3		15	22	ns
t_{TD}	Differential-output transition time				20	30	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		85	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		40	60	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4		150	250	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5		20	30	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis§				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 5	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance	V_I = 12 V		12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	70	mA
			Outputs disabled		26	35	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
NOTE 5: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

receiver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = 0 to 3 V,			21	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	See Figure 6		23	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 7		10	20	ns
t_{PZL}	Output enable time to low level				12	20	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 7		20	35	ns
t_{PLZ}	Output disable time from low level				17	25	ns

PARAMETER MEASUREMENT INFORMATION

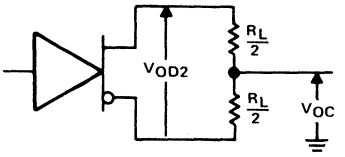


FIGURE 1. DRIVER V_{OD} AND V_{OC}

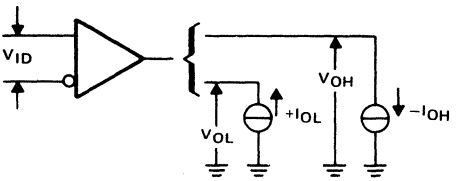
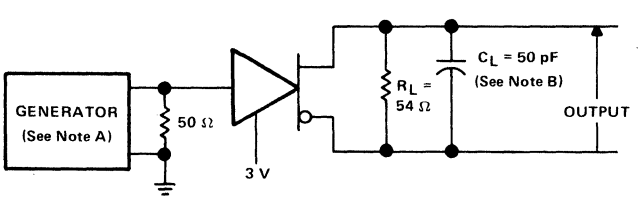
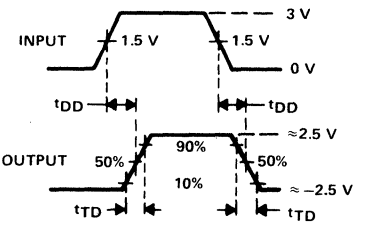


FIGURE 2. RECEIVER V_{OH} AND V_{OL}

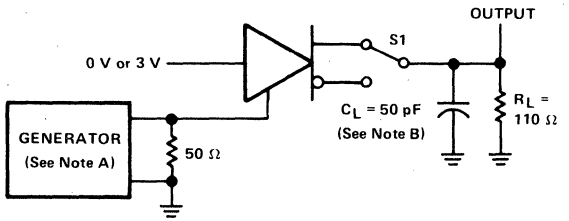


TEST CIRCUIT

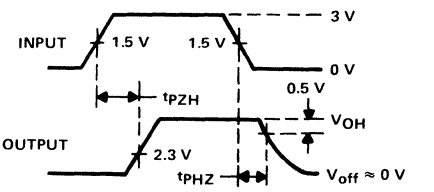


VOLTAGE WAVEFORMS

FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

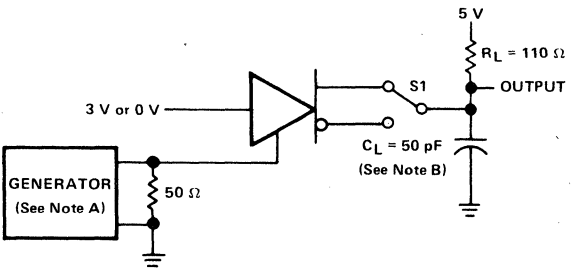


TEST CIRCUIT

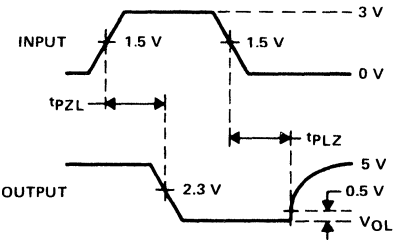


VOLTAGE WAVEFORMS

FIGURE 4. DRIVER ENABLE AND DISABLE TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 5 ns, Z_o = 50 Ω.
B. C_L includes probe and jig capacitance.
C. Equivalent test circuits may be substituted for actual testing.

PARAMETER MEASUREMENT INFORMATION

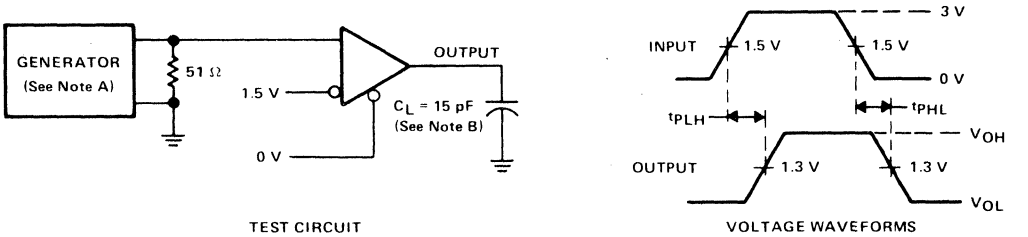


FIGURE 6. RECEIVER PROPAGATION DELAY TIMES

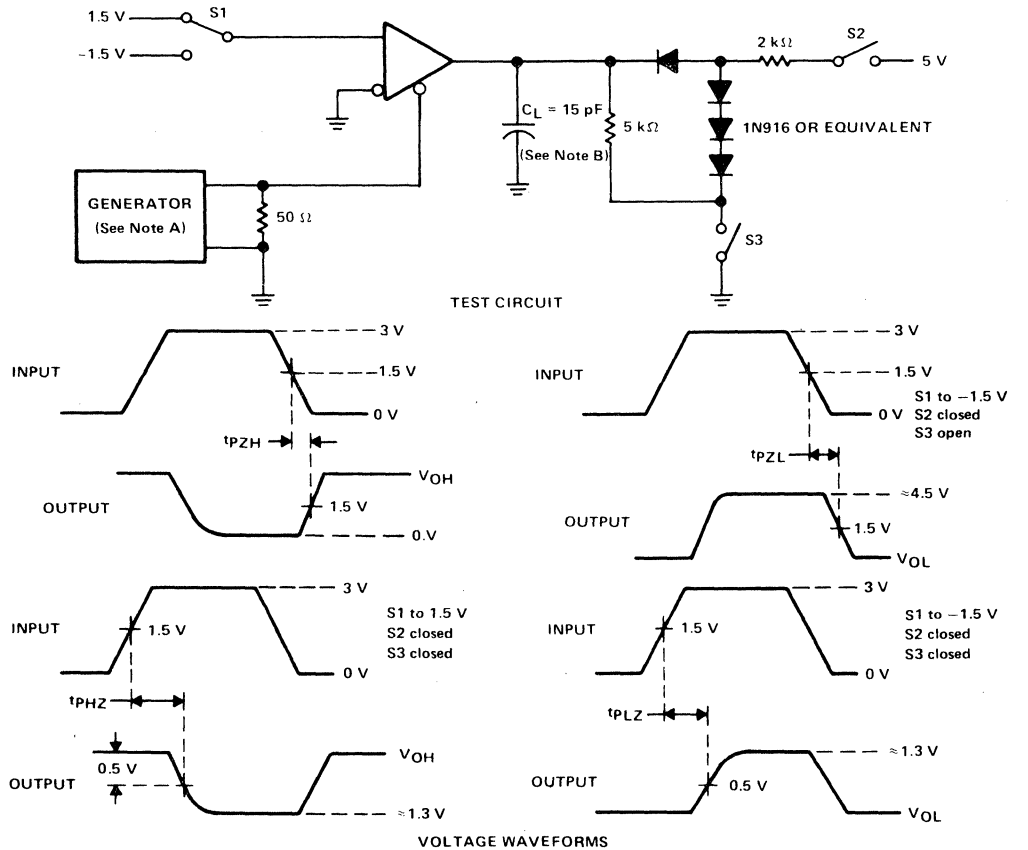


FIGURE 7. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. Equivalent test circuits may be substituted for actual testing.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

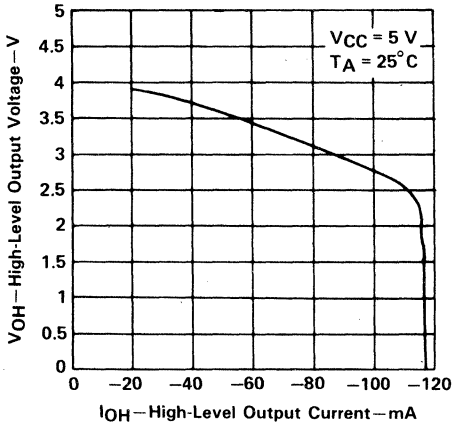


FIGURE 8

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

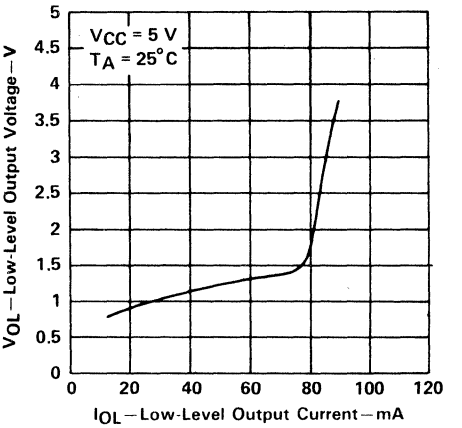


FIGURE 9

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

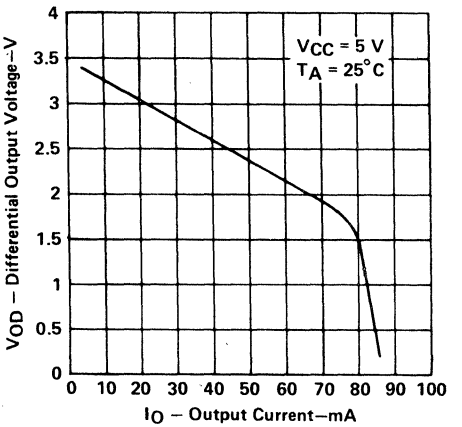


FIGURE 10

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

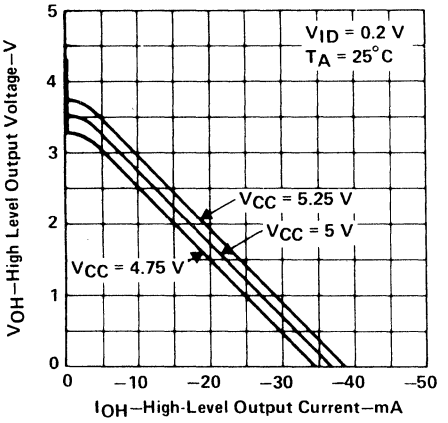


FIGURE 11

RECEIVER HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

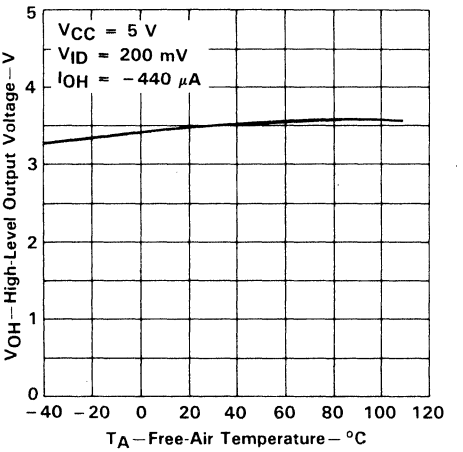


FIGURE 12

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

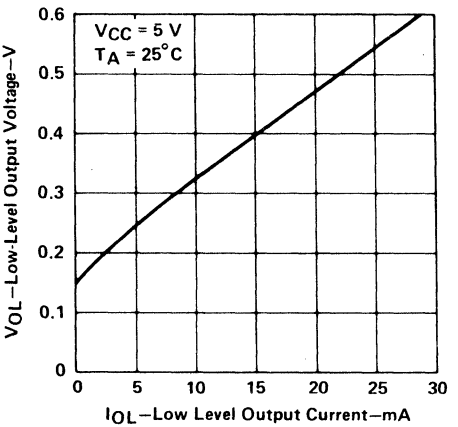


FIGURE 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

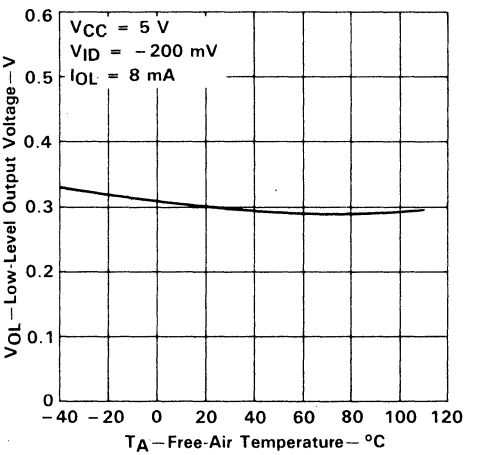


FIGURE 14

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

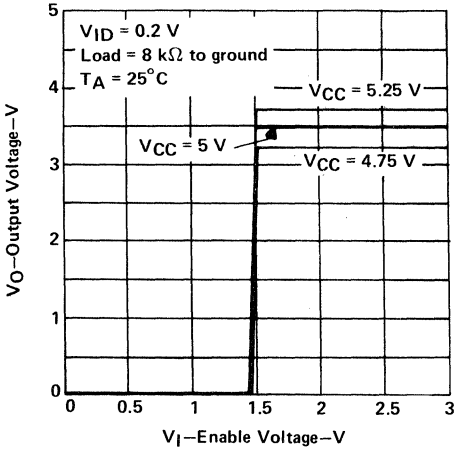


FIGURE 15

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

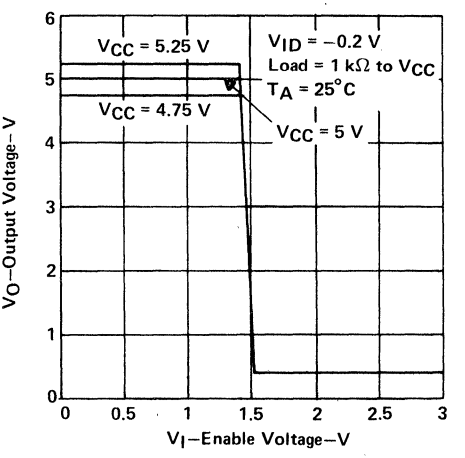
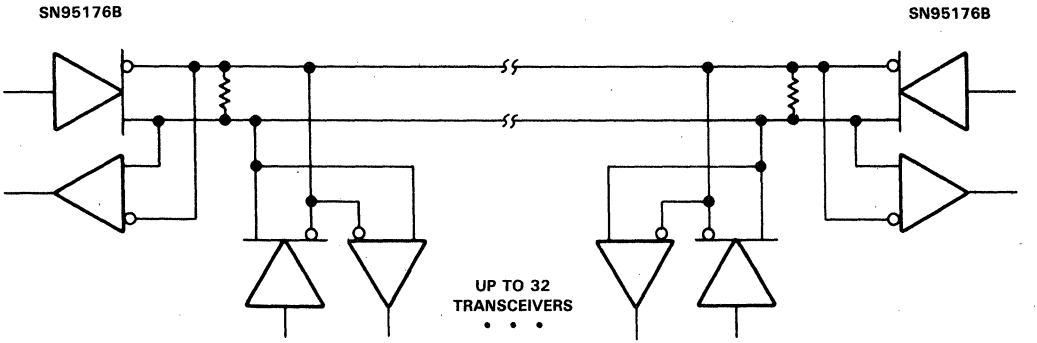


FIGURE 16

APPLICATION INFORMATION



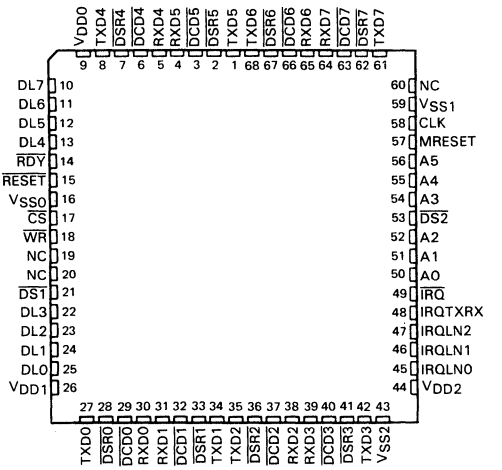
NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 17. TYPICAL APPLICATION CIRCUIT

D2941, APRIL 1986—REVISED JULY 1990

- **Eight Independent Full-Duplex Serial Data Lines**
- **Programmable Baud Rates Individually Selectable for the Transmitter/Receiver of Each Line (50 to 19,200 Baud)**
- **Summary Registers Allow a Single Read to Detect a Data Set Change or to Determine the Cause of an Interrupt on Any Line**
- **Triple Buffers for Each Receiver**
- **Device Scanner Mechanism Reports Interrupt Requests Due to Transmitter/Receiver Interrupts**
- **Independently Programmable Lines for Interrupt-Driven Operation**
- **Modem Status Change Detection for Data Set Ready (DSR) and Data Carrier Detect (DCD) Signals**
- **Programmable Interrupts for Modem Status Changes**
- **Synchronizes Critical Read-Only Registers**
- **Replaces Eight Signetics 2661 UARTs**
- **Direct Second Source to DEC DC349 (78808)**

FN, HA, OR HB PACKAGE
(TOP VIEW—LID UP FOR HA OR HB)



NC—No internal connection

PACKAGE DESIGNATIONS

DESCRIPTION	TI	DEC
Cerquad Gull-Wing	HA	GA
Cerquad Straight	HB	FA
Plastic PLCC	FN	

description

The TCM78808 octal asynchronous receiver/transmitter is designed for the new generations of asynchronous serial communications and for microcomputer systems. The device performs the basic operations necessary for simultaneous reception and transmission of asynchronous messages on eight independent lines.

On-chip baud rate generation allows the designer to select and program any one of 16 rates between 50 and 19,200 baud. Baud rates are selectable for each receiver and transmitter. A built-in scanning mechanism provides an alternative to the customary polling of status registers.

The TCM78808 functions as a serial-to-parallel, parallel-to-serial converter/controller. It can be programmed by a microprocessor to provide different characteristics for each of its eight serial data lines (stop bits, parity, character length, baud rates, etc.). Each individual serial line functions as a one-line UART-type device.

An integral interrupt scanner checks for device interrupt conditions on the eight lines of the TCM78808. Its scanning algorithm is designed to give priority to receivers over transmitters. The scanner can also be programmed to check for interrupts due to changes in modem control signals (DSR and DCD).

The TCM78808 contains two types of programmable registers: line specific and summary. The six line-specific registers provide independent control of each of the eight serial lines. Two summary registers consolidate information about the current state of all eight lines and allow programs to service device interrupts quickly and efficiently.

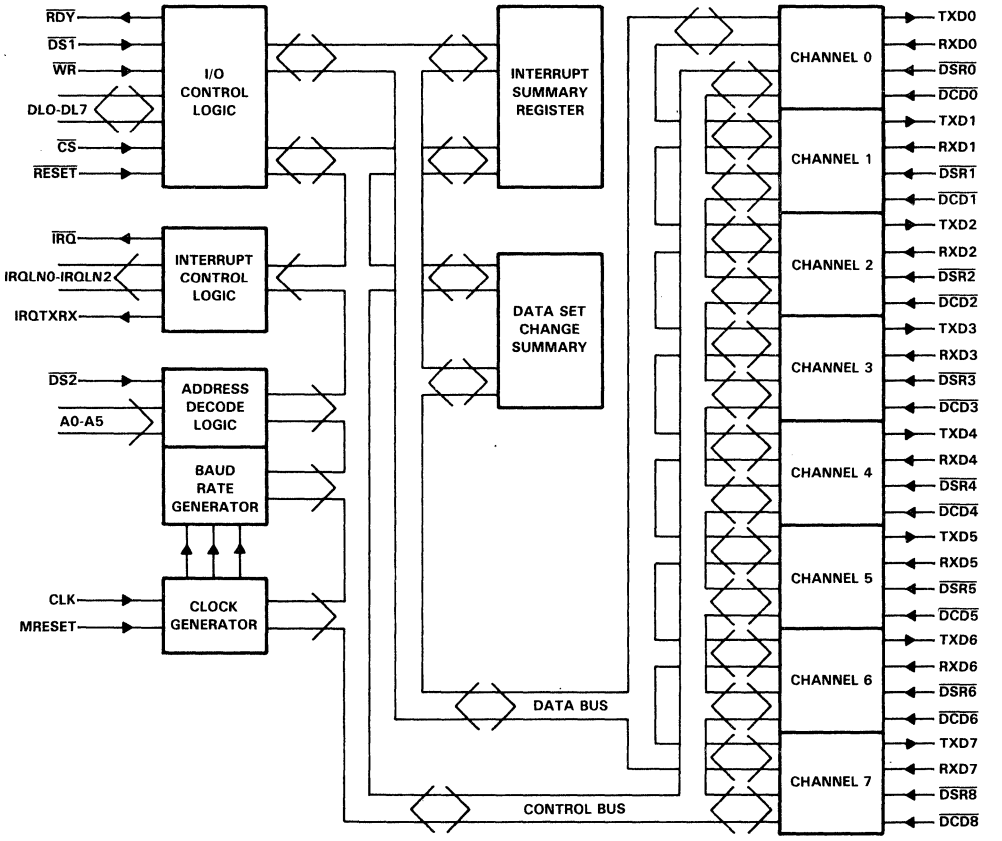
Each of the eight serial data lines in the TCM78808 has a set of line-specific registers for buffering data into and out of the line and for external control of line characteristics. The receiver buffer register comprises a character assembly register plus a two-entry, first-in first-out (FIFO) buffer. The transmitter holding register provides similar functions on the output side. Information about the current state of the given line is contained in the (read-only) status register. Two mode registers control communications parameters. One mode register handles stop bits, parity, character length, and modem control interrupt enable (MCIE). The second mode register sets the incoming and outgoing baud rates. The command register controls various other functions of the given line.

The TCM78808 has a pair of summary registers that provide the current status of all eight serial data lines. This makes it possible to determine that line status has changed with a single read operation. The (read-only) interrupt summary register indicates that an interrupt has occurred and contains both the line number that generated the interrupt and the corresponding direction of flow (transmitter or receiver). With both MCIEs set and receiver interrupt enabled, the interrupt summary register will respond to changes in $\overline{\text{DSR}}$ or $\overline{\text{DCD}}$. The data-set-change summary register monitors changes in $\overline{\text{DSR}}$ or $\overline{\text{DCD}}$ on a line-by-line basis and indicates whether a modem status change has occurred on each data line subsequent to the last time the corresponding bit was cleared.

The TCM78808 is characterized for operation from 0°C to 70°C.

SIGNAL	DESCRIPTION
A0 THRU A5	Address bits 0 through 5 select the internal registers in the TCM78808.
CLK	Clock input for timing
$\overline{\text{CS}}$	Chip Select. When low, activates the TCM78808 to receive and transmit data over data lines DL0 through DL7.
$\overline{\text{DCD0}}$ THRU $\overline{\text{DCD7}}$	Data-Set Carrier Detect inputs monitor data-set carrier detect signals from modems.
DL0 THRU DL7	Data Lines 0 through 7 receive and transmit the parallel data.
$\overline{\text{DS1}}$, $\overline{\text{DS2}}$	Data Strobes 1 and 2 receive timing information for data transfers. The $\overline{\text{DS1}}$ and $\overline{\text{DS2}}$ inputs must be connected together.
$\overline{\text{DSR0}}$ THRU $\overline{\text{DSR7}}$	Data Set Ready inputs monitor data-set-ready signals from modems.
$\overline{\text{IRQ}}$	Interrupt Request output requests a processor interrupt.
IRQLN0 THRU IRQLN2	Interrupt Request Line number outputs indicate the line number of the originating interrupt request.
IRQTXRX	Interrupt Request Transmit/Receive output indicates whether an interrupt request is for transmitting or receiving data.
MRESET	Manufacturing Reset. For manufacturing use
$\overline{\text{RDY}}$	Ready output indicates when the TCM78808 is ready to participate in data-transfer cycles.
$\overline{\text{RESET}}$	Reset input initializes the internal logic.
RXD0 THRU RXD7	Receive Data inputs accept asynchronous bit-serial data input streams.
TXD0 THRU TXD7	Transmit Data output provides asynchronous bit-serial data output streams.
V_{DD0} THRU V_{DD2}	5-V nominal power supply
V_{SS0} THRU V_{SS2}	Ground reference
$\overline{\text{WR}}$	Write input specifies direction of data transfer on the DL0 through DL7 lines.

functional block diagram



absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{DD} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . −5 V to 7 V
Input current, I_I . . . . . −30 mA to 5 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range: HA or HB package . . . . . −65°C to 150°C
FN package . . . . . 0°C to 125°C

NOTE 1: All voltage values are with respect to V_{SS1} and V_{SS2}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5.25 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 4.75 V, I_{OH} for DL0 thru DL7 = −3.5 mA, I_{OH} for all other (except $\overline{IRQ}$ and $\overline{RDY}$) = −2 mA	2.4		V
V_{OL}	Low-level output voltage		V_{DD} = 4.75 V, I_{OL} for DL0 thru DL7 = 5.5 mA, I_{OL} for all other = 3.5 mA		0.4	V
I_{IH}	High-level input current		V_I = 5.25 V		10	μA
I_{IL}	Low-level input current		V_I = 0		−10	μA
I_{OS}†	Short-circuit output current	DL0-DL7	V_{DD} = 5.25 V	−50	−180	mA
		All other outputs except $\overline{IRQ}$ and $\overline{RDY}$		−30	−110	
I_{OZH}‡	Off-state output current, high-level voltage applied		V_O = 2.4 V		−10	μA
I_{OZL}‡	Off-state output current, low-level voltage applied		V_O = 0.4 V		10	μA
I_{DD}	Supply current		V_{DD} = 5 V, T_A = 25°C		200	mA
C_i	Input capacitance				4	pF
C_{io}§	Input/output capacitance				5	pF

† Not more than one output should be short circuited at a time, and the duration of the short should not exceed 1 second.
‡ All 3-state output drivers are wired in an I/O configuration. The parameters include the driver and receiver input currents.
§ This parameter includes the capacitive loads of the output driver and the receiver input.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

bus read and write timing requirements (see Figures 3 and 4)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{w1}	Pulse duration, $\overline{DS1}$/$\overline{DS2}$ low	$\overline{WR}$ high	0.18	10	μs
t_{w2}	Pulse duration, $\overline{DS1}$/$\overline{DS2}$ high		450		ns
t_{w3}	Pulse duration, $\overline{DS1}$/$\overline{DS2}$ low	$\overline{WR}$ low	0.13	10	μs
t_{su1}	Setup time, A5-A0 valid before $\overline{DS1}$ and $\overline{DS2}$ low		30		ns
t_{su2}	Setup time, $\overline{WR}$ high before $\overline{DS1}$ and $\overline{DS2}$ low		30		ns
t_{su3}	Setup time, $\overline{CS}$ low before $\overline{DS1}$ and $\overline{DS2}$ low		30		ns
t_{su4}	Setup time, DL7-DL0 valid before $\overline{DS1}$ and $\overline{DS2}$ low		130		ns
t_{h1}	Hold time, A5-A0 valid after $\overline{DS1}$ and $\overline{DS2}$ high		10		ns
t_{h2}	Hold time, $\overline{WR}$ high or low after $\overline{DS1}$ and $\overline{DS2}$ high		10		ns
t_{h3}	Hold time, $\overline{CS}$ low after $\overline{DS1}$ and $\overline{DS2}$ high		10		ns
t_{h4}	Hold time, DL7-DL0 valid after $\overline{DS1}$ and $\overline{DS2}$ high		30		ns
t_v	Valid time, DL7-DL0 after $\overline{DS1}$ and $\overline{DS2}$ high		0		ns

write switching characteristics (see Figures 3 and 4)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{en}	Enable time	C_L = 150 pF		165	ns
t_{dis}	Disable time	C_L = 50 pF		50	ns
		C_L = 100 pF		60	
		C_L = 150 pF		65	
t_{pd1}	Propagation delay time, from $\overline{CS}$ low to $\overline{RDY}$ low	C_L = 50 pF		90	ns
t_{pd2}†	Propagation delay time, from $\overline{CS}$ high to $\overline{RDY}$ high	C_L = 50 pF		210	ns
t_{pd3}	Propagation delay time, from $\overline{DS1}$ and $\overline{DS2}$ low to DL7-DL0 valid	C_L = 150 pF		165	ns
t_{pd4}†	Propagation delay time, from $\overline{DS1}$ and $\overline{DS2}$ low to $\overline{IRQ}$ high	C_L = 50 pF		635	ns

†Total rise time is dependent upon internal delay plus the pull-up delay introduced by the external resistor being used. Parameter t_{pd2} is calculated from t_{pd2} = 75 ns + R_{CL}, and t_{pd4} is calculated from t_{pd4} = 500 ns + R_{CL} where R = value of the resistor that connects to C_L in Figure 1.

write timing requirements (see Figure 5)

		TEST CONDITIONS	MIN	MAX	UNIT
f_{clock}	Clock frequency		4.9152		MHz
t_{w4}	Pulse duration, clock high or low		95		ns
t_{w5}	Pulse duration, $\overline{RESET}$ low		1		μs
t_{w6}	Pulse duration, DCD7-DCD0 and $\overline{DSR7}$-$\overline{DSR0}$ high or low		1		μs
t_{w7}	Pulse duration, TXD7-TXD0 high or low		250		ns
t_{su5}	Setup time, $\overline{DS1}$ and $\overline{DS2}$ high before $\overline{RESET}$ high		900		ns
t_{su6}	Setup time, MRESET high before $\overline{RESET}$ low		250		ns
t_{h5}	Hold time, $\overline{DS1}$ and $\overline{DS2}$ high after $\overline{RESET}$ high		1		μs
t_{h6}	Hold time, MRESET high after $\overline{RESET}$ high		250		ns
t_{d1}	Delay time, IRQLN2-IRQLN0 and IRQTXRX valid to $\overline{IRQ}$ low	C_L = 50 pF	100		ns
t_{d2}	Hold time, IRQLN2-IRQLN0 and IRQTXRX valid after $\overline{IRQ}$ high	C_L = 50 pF	100		ns

PARAMETER MEASUREMENT INFORMATION

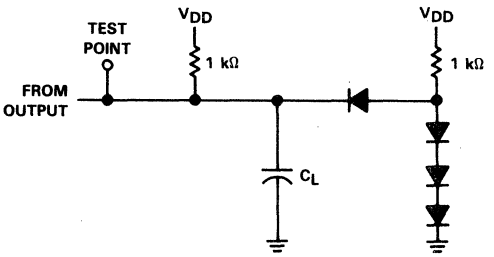


FIGURE 1. STANDARD OUTPUT LOAD CIRCUIT

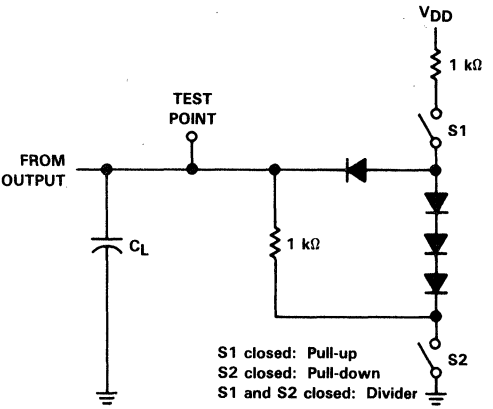


FIGURE 2. 3-STATE OUTPUT LOAD CIRCUIT

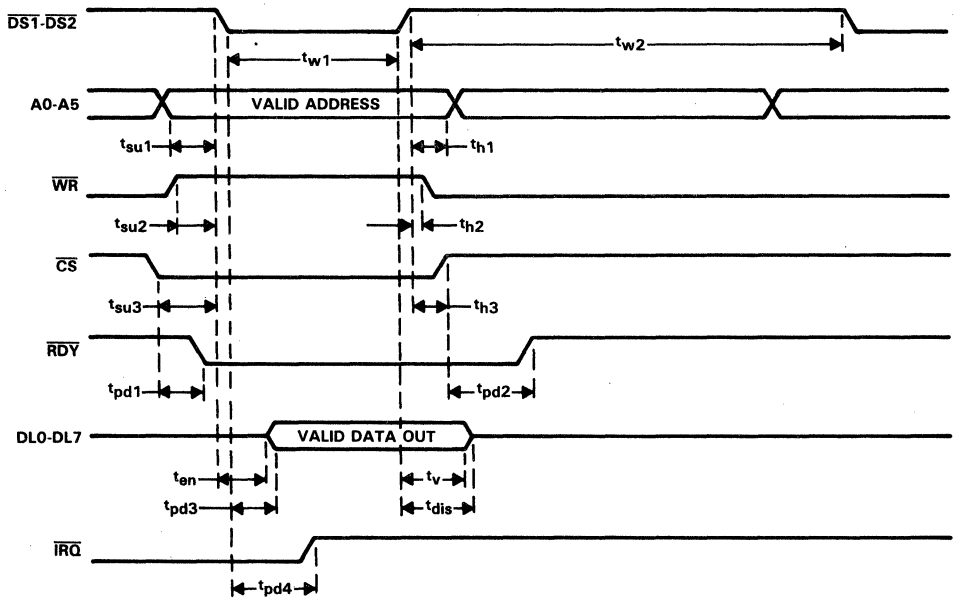


FIGURE 3. BUS READ CYCLE TIMING WAVEFORMS

PARAMETER MEASUREMENT INFORMATION

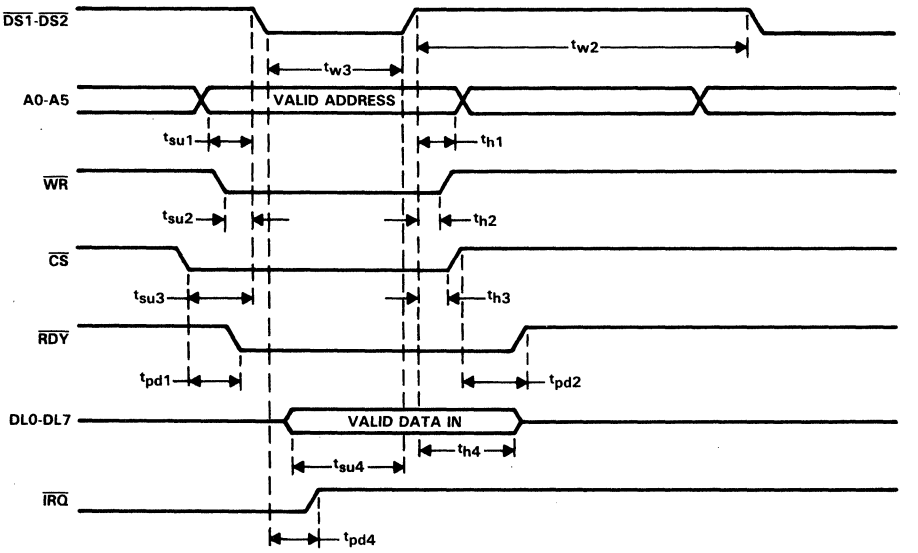


FIGURE 4. BUS WRITE CYCLE TIMING WAVEFORMS

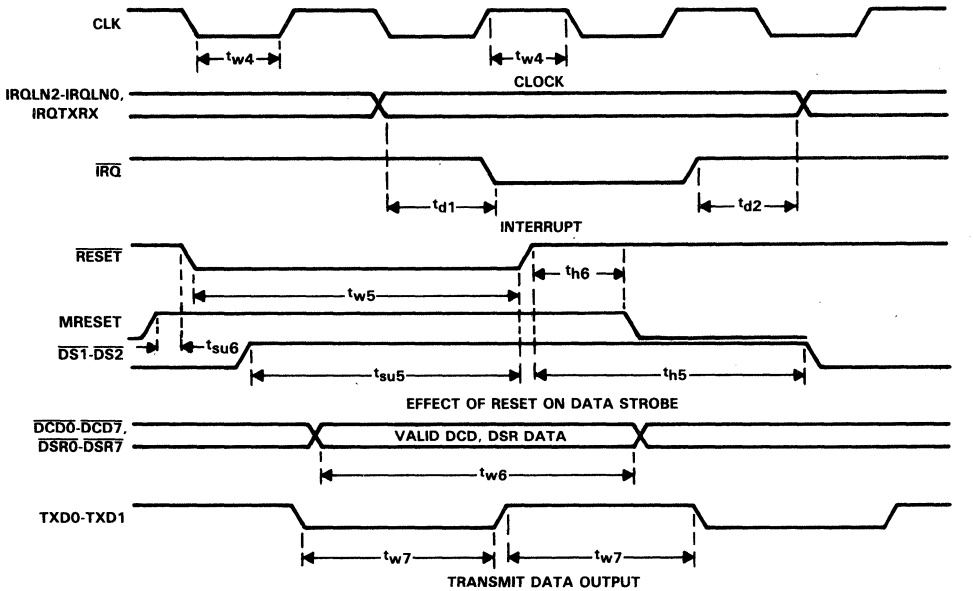
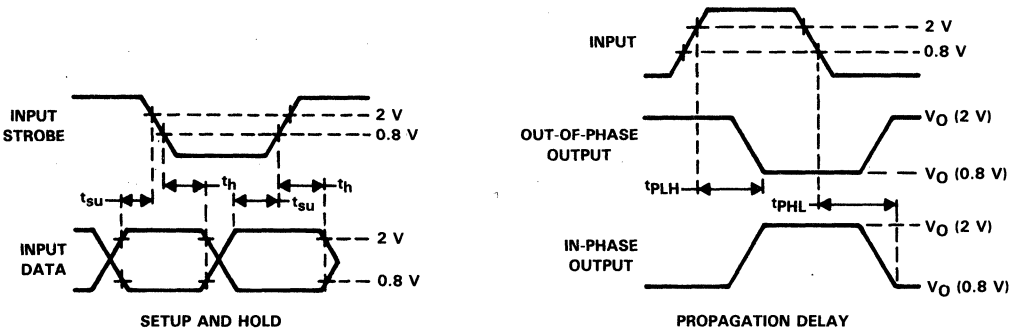


FIGURE 5. MISCELLANEOUS SIGNAL TIMING

PARAMETER MEASUREMENT INFORMATION



NOTE: $t_{pd} = t_{PLH}$ or t_{PHL}

FIGURE 6. VOLTAGE WAVEFORMS

PRINCIPLES OF OPERATION

electrical operation

data and address

data lines (DL7 through DL0)

These lines are used for the parallel transmission and reception of data between the CPU and the TCM78808. The receivers are activated by the data strobe ($\overline{DS1}$, $\overline{DS2}$) signal. The output drivers are active only when the chip select ($\overline{CS}$) signal is low (active), the data strobe ($\overline{DS1}$, $\overline{DS2}$) signal goes low (active), and the write ($\overline{WR}$) signal is high (inactive). The drivers will become inactive (high impedance) within 50 ns when one or more of the following occurs: the chip select ($\overline{CS}$) signal goes high, the data strobe ($\overline{DS1}$, $\overline{DS2}$) goes high, or the write ($\overline{WR}$) signal goes low.

address lines (A5 through A0)

These lines select which internal register is accessible through the data I/O lines (DL7 through DL0) when the data strobe ($\overline{DS1}$, $\overline{DS2}$) and chip select ($\overline{CS}$) signals are low. Table 1 lists the addresses corresponding to each register. The receiver buffer and transmitter holding register for each line have the same address. When the ($\overline{WR}$) signal is high, the address accesses the receiver buffer register. When $\overline{WR}$ is low, it accesses the transmitter holding register.

PRINCIPLES OF OPERATION

TABLE 1. TCM78808 REGISTERS ADDRESS SELECTION

ADDRESS LINE†						READ/ WRITE	REGISTER
A5	A4	A3	A2	A1	A0		
L	L	L	L	L	L	Read	Line 0 Receiver Buffer
L	L	L	L	L	L	Write	Line 0 Transmitter Holding
L	L	L	L	L	H	Read	Line 0 Status
L	L	L	L	H	L	Read/Write	Line 0 Mode Registers 1 and 2
L	L	L	L	H	H	Read/Write	Line 0 Command
L	L	H	L	L	L	Read	Line 1 Receiver Buffer
L	L	H	L	L	L	Write	Line 1 Transmitter Holding
L	L	H	L	L	H	Read	Line 1 Status
L	L	H	L	H	L	Read/Write	Line 1 Mode Registers 1 and 2
L	L	H	L	H	H	Read/Write	Line 1 Command
L	H	L	L	L	L	Read	Line 2 Receiver Buffer
L	H	L	L	L	L	Write	Line 2 Transmitter Holding
L	H	L	L	L	H	Read	Line 2 Status
L	H	L	L	H	L	Read/Write	Line 2 Mode Registers 1 and 2
L	H	L	L	H	H	Read/Write	Line 2 Command
L	H	H	L	L	L	Read	Line 3 Receiver Buffer
L	H	H	L	L	L	Write	Line 3 Transmitter Holding
L	H	H	L	L	H	Read	Line 3 Status
L	H	H	L	H	L	Read/Write	Line 3 Mode Registers 1 and 2
L	H	H	L	H	H	Read/Write	Line 3 Command
H	L	L	L	L	L	Read	Line 4 Receiver Buffer
H	L	L	L	L	L	Write	Line 4 Transmitter Holding
H	L	L	L	L	H	Read	Line 4 Status
H	L	L	L	H	L	Read/Write	Line 4 Mode Registers 1 and 2
H	L	L	L	H	H	Read/Write	Line 4 Command
H	L	H	L	L	L	Read	Line 5 Receiver Buffer
H	L	H	L	L	L	Write	Line 5 Transmitter Holding
H	L	H	L	L	H	Read	Line 5 Status
H	L	H	L	H	L	Read/Write	Line 5 Mode Registers 1 and 2
H	L	H	L	H	H	Read/Write	Line 5 Command
H	H	L	L	L	L	Read	Line 6 Receiver Buffer
H	H	L	L	L	L	Write	Line 6 Transmitter Holding
H	H	L	L	L	H	Read	Line 6 Status
H	H	L	L	H	L	Read/Write	Line 6 Mode Registers 1 and 2
H	H	L	L	H	H	Read/Write	Line 6 Command
H	H	H	L	L	L	Read	Line 7 Receiver Buffer
H	H	H	L	L	L	Write	Line 7 Transmitter Holding
H	H	H	L	L	H	Read	Line 7 Status
H	H	H	L	H	L	Read/Write	Line 7 Mode Registers 1 and 2
H	H	H	L	H	H	Read/Write	Line 7 Command
X	X	X	H	L	L	Read	Interrupt Summary
X	X	X	H	L	H	Read	Data Set Change Summary

†X = Either L or H

PRINCIPLES OF OPERATION

bus transaction control

chip select ($\overline{CS}$)

This signal, when low, permits data transfers through the DL7 through DL0 lines to or from the internal registers. Data transfer is controlled by the data strobe ($\overline{DS1}$, $\overline{DS2}$) signal and the write ($\overline{WR}$) signal.

data strobe ($\overline{DS1}$, $\overline{DS2}$)

The data strobe inputs ($\overline{DS1}$ and $\overline{DS2}$) must be connected together. This input receives timing information for data transfers. During a write cycle, the CPU activates the data strobe signal when valid output data is available and deactivates the data strobe signal before the data is removed. During a read cycle, the CPU activates the data strobe signal, and the TCM78808 transfers the valid data.

When the data strobe signal is high, the DL7 through DL0 lines are in a high-impedance state.

write ($\overline{WR}$)

The write ($\overline{WR}$) signal specifies the direction of data transfer on the DL7 through DL0 pins by controlling the direction of their transceivers. If the $\overline{WR}$ signal is low during a data transfer (with the $\overline{CS}$, $\overline{DS1}$, and $\overline{DS2}$ signals also low), the TCM78808 receives data from DL7 through DL0. If the $\overline{WR}$ signal is high during a write data transfer, the TCM78808 drives data onto the DL7 through DL0 lines.

interrupt request ($\overline{IRQ}$)

The $\overline{IRQ}$ output is an active-low, open-drain output. The integral interrupt scanner drives the $\overline{IRQ}$ signal low when it has detected an interrupt condition on one of the eight serial data lines.

interrupt request transmit/receive (IRQTxRx)

This signal indicates when the interrupt scanner stops and activates $\overline{IRQ}$ because of a transmitter interrupt condition (IRQTxRx = H) or because of a receiver interrupt condition (IRQTxRx = L). The signal is valid only while the $\overline{IRQ}$ signal is low. The state of IRQTxRx signal also appears as bit 0 of the interrupt summary register.

interrupt request line number (IRQLN2 through IRQLN0)

These lines indicate the line number at which the TCM78808 interrupt scanner stopped and activated the interrupt request ($\overline{IRQ}$) signal. The number on these lines is valid only while the $\overline{IRQ}$ signal is low. Line IRQLN2 is the high-order bit, and the IRQLN0 line is the low-order bit.

The state of these signals also appears as bits in the interrupt summary register: IRQLN2 as bit 3, IRQLN1 as bit 2, and IRQLN0 as bit 1. Table 2 shows the line numbers corresponding to settings of IRQLN2 through IRQLN0.

PRINCIPLES OF OPERATION

TABLE 2. TCM78808 INTERRUPT REQUEST LINE INDICATIONS

IRQLN2	IRQLN1	IRQLN0	INTERRUPT REQUEST LINE NUMBER
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

serial data

transmit data (TXD7 through TXD0)

These outputs transmit the asynchronous bit-serial data streams. They remain at a high level when no data is being transmitted and at a low level when the TxBRK bit in the command register of the associated line is set.

receive data (RXD7 through RXD0)

These lines accept asynchronous bit-serial data streams. The input signals must remain at the high level for at least one-half bit time before a high-to-low transition is recognized. A high-to-low transition is required to signal the beginning of a start bit and initiate data reception.

modem signals

data set ready ($\overline{DSR7}$ through $\overline{DSR0}$)

These eight inputs, one for each serial data line on the TCM78808, are typically connected via intervening level converters to the data set ready outputs of modems. A TTL low at a $\overline{DSR}$ pin causes the $\overline{DSR}$ bit (bit 7) in the status register of the corresponding line to be activated. A TTL high at a $\overline{DSR}$ pin causes the $\overline{DSR}$ bit in the status register of the corresponding line to be inactive. A change of this input from high to low or low to high causes the activation of the data set change (DSCHNG) bit that corresponds to this line in the data set change summary register. Changes from one level to the other and back again that occur within 1 μs may not be detected.

carrier detect ($\overline{DCD7}$ through $\overline{DCD0}$)

These eight inputs, one for each serial data line of the TCM78808, are typically connected through intervening level converters to the received-line-signal-detect (also called carrier-detect) outputs of modems. A TTL low at a $\overline{DCD}$ input causes the $\overline{DCD}$ bit of the corresponding line status register to be deactivated. A change of this input from high to low or low to high causes the activation of the data-set-change (DSCHNG) bit that corresponds to this line in the data-set-change summary register. Changes from one level to the other and back again that occur within 1 μs may not be detected.

PRINCIPLES OF OPERATION

general control signals

ready ($\overline{RDY}$)

The $\overline{RDY}$ output is an open-drain output. Upon detecting a negative transition of $\overline{CS}$, the TCM78808 activates the $\overline{RDY}$ signal to indicate readiness to take part in data transfer cycles. The $\overline{RDY}$ signal deactivates on the trailing edge of $\overline{CS}$.

reset ($\overline{RESET}$)

When the $\overline{RESET}$ input goes low, the TxD7 through TxD0 lines are low, and all internal status bits listed in the Architecture Summary paragraph are cleared.

manufacturing reset (MRESET)

This signal is for manufacturing use only. The input should be connected to ground for normal operation.

clock signals

clock input (CLK)

All baud rates and internal clocks are derived from this input. Normal operating frequency is 4.9152 MHz ±0.1%, and duty cycle is 50 ±5%.

architecture summary

line-specific registers

Each of the eight serial data lines has a set of registers for buffering data into and out of the line and for external control of the line characteristics. These registers are selected for access by setting the appropriate address on lines A5 through A0. Lines A5 through A3 select one of the eight data lines . Lines A2 through A0 select the specific register for that line. Refer to Table 1 for the register address assignments.

receiver buffer register

Each line receiver consists of a character-assembly register and a two-entry FIFO that is the receiver buffer register. When the RxEN bit in a line command register is set, received characters are moved automatically into the line receiver buffer as soon as they have been deserialized from the associated communications line. When there are characters in this FIFO, the RxRDY bit is set in the status register for the line.

The activation of the RxRDY signal for a line that already has the RxIE bit of its command register set causes the interrupt scanner logic to stop and generate an interrupt condition (the $\overline{IRQ}$ signal is low). When the receiver buffer is read, the interrupt condition is cleared (the $\overline{IRQ}$ signal is high), and the interrupt scanner resumes operation.

If there is another entry in a line FIFO, the RxRDY bit remains active. When the interrupt scanner reaches this line again, the activation of RxRDY causes the scanner to halt and generate another interrupt ($\overline{IRQ}$ goes low).

The $\overline{RESET}$ signal clears the RxEN bit and initializes the receiver logic. The RxRDY flag is cleared, and the receiver buffer register outputs become undefined. Any data in the FIFO at that time is lost.

PRINCIPLES OF OPERATION

transmitter holding register

Each line has a transmitter holding register that can be written to. When the TxEN bit in the line command register is set and the serialization logic becomes idle, characters are automatically moved from the output of this register into the transmitter serialization logic.

When this register is empty, the TxRDY bit in the line status register is set. If the transmitter interrupt enable (TxIE) bit in the line command register is also set, the interrupt scanner logic halts and generates an interrupt condition. If a character is then loaded into the register, the interrupt is cleared, and the scanner resumes operation.

The $\overline{\text{RESET}}$ signal also initializes the transmitter logic. The TxRDY flag is cleared, and the transmitter holding register contents are lost. The transmitter enable (TxEN) bit in the line command register is also cleared by $\overline{\text{RESET}}$. Software clearing of TxEN alone produces results different from the full $\overline{\text{RESET}}$ in that the transmitter holding register contents are not lost. They are transmitted when TxEN is set again.

status register

Each line has a read-only status register that provides information about the current state of the given line. This register indicates the readiness of a line for transmission or reception of data and flags error conditions in its bit fields. Figure 7 shows the format of the status register. Table 3 lists the flag bits in each register.

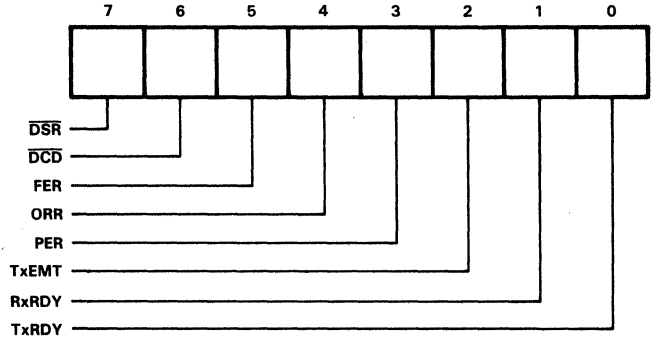


FIGURE 7. TCM78808 STATUS REGISTERS (LINE 0 THROUGH 6) FORMAT

PRINCIPLES OF OPERATION

TABLE 3. TCM78808 STATUS REGISTERS (LINES 0 THROUGH 7) DESCRIPTION

BIT	DESCRIPTION
7	DSR (Data Set Ready). This bit is the inverted state of the $\overline{DSR}$ line.
6	DCD (Data Set Carrier Detect). This bit is the inverted state of the $\overline{DCD}$ line.
5	FER (Frame Error). Set when the received character currently displayed in the receiver buffer register was not framed by a stop bit. Only the first stop bit is checked to determine that a framing error exists. Subsequent reading of the receiver buffer register that indicates all zeros (including the parity bit, if any) can be interpreted as a Break condition. This bit is cleared by clearing RxEN (bit 2) of the command register, by $\overline{RESET}$, or by setting the reset error RERR (bit 4) of the command register.
4	ORR (Overrun error). Set when the character in the receiver buffer was not read before another character was received. Cleared by clearing RxEN (bit 2) of the command register, by $\overline{RESET}$, or by setting reset error RERR (bit 4) of the command register.
3	PER (Parity Error). If parity is enabled and this bit is set, the received character in the receiver buffer register has an incorrect parity bit. This bit is cleared by clearing RxEN (bit 2) of the command register, by $\overline{RESET}$, by setting reset error RERR (bit 2) of the command register, or by reading the current character in the receiver buffer register.
2	TxEMT (Transmitter Empty). Set when the transmitter serialization logic for the associated line has completed transmission of a character, and no new character has been loaded into the transmission holding register. Cleared by loading the transmitter holding register, by clearing TxEN(0) of the command register, or by $\overline{RESET}$.
1	RxRDY (Receiver Buffer Ready). When set, a character has been loaded into the FIFO buffer from the deserialization logic. Cleared by reading the receiver buffer register, by clearing RxEN (bit 2) in the command register, or by $\overline{RESET}$.
0	TxRDY (Transmitter Holding Register Ready). When set, this bit indicates that the transmitter holding register is empty. Cleared when the program has loaded a character into the transmitter holding register, when the transmitter for this line is disabled by clearing TxEN (bit 0) in the command register, or $\overline{RESET}$. This bit is initially set when the transmitter logic is enabled by the setting of the TxEN (bit 0) and the transmitter holding register is empty. This bit is not set when the automatic echo or remote loopback modes are programmed. Data can be overwritten if a consecutive write is performed while TxRDY is cleared.

mode registers 1 and 2

These read/write registers control the attributes (including parity, character length, and line speed) of the communications line.

Each of the eight communications lines has two of these registers, both accessed by the same address on A5 through A0. Successive access operations (either read or write, in any combination) alternate between the two registers at that address by use of an internal pointer. The first operation addresses mode register 1. The pointer is reset to point to mode register 1 by $\overline{RESET}$ or by a read of the command register for this line. These registers should not be accessed by bit-oriented instructions that do read/modify/write cycles such as the PDP-11 BIS, BIC, and BIT instructions.

Figure 8 shows the format of mode registers 1, and Table 4 describes the function of the register information.

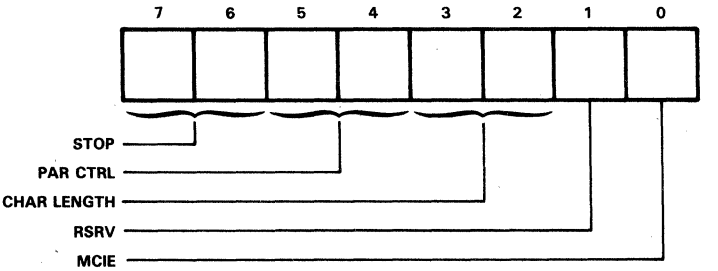


FIGURE 8. TCM78808 MODE REGISTERS 1 (LINE 0-6) FORMAT

PRINCIPLES OF OPERATION

TABLE 4. TCM78808 MODE REGISTERS 1 (LINES 0 THROUGH 6) DESCRIPTION

BIT	DESCRIPTION
7,6	STOP. These bits determine the number of stop bits that are appended to the transmitted characters as follows. These bits are cleared by $\overline{\text{RESET}}$. Bit 7 / Bit 6 / Stop Bits L / L / Invalid L / H / 1.0 H / L / 1.5 H / H / 2.0
5,4	PAR CTRL (Parity control). These bits determine parity as follows and are cleared by $\overline{\text{RESET}}$. (X = either H or L) Bit 5 / Bit 4 / Parity Type H / H / Even L / H / Odd X / L / Disabled
3,2	CHAR LENGTH (Character length). These bits determine the length (excluding start bit, parity, and stop bits) of the characters received and sent. Received characters of less than 8 bits are "right aligned" in the receiver buffer with unused high-order bits equal to zero. Parity bits are not shown in the receiver buffer. The character length bits are cleared by $\overline{\text{RESET}}$. The character length bits are defined as follows: Bit 3 / Bit 2 / Bit Length L / L / 5 L / H / 6 H / L / 7 H / H / 8
1	RSRV. Reserved and cleared by $\overline{\text{RESET}}$.
0	MCIE (Modem control interrupt enable). When set and RxIE (bit 5) of the command register is set, the modem control interrupts are enabled. Refer to the interrupt Scanner and Interrupt Handling information. Cleared by $\overline{\text{RESET}}$.

Figure 9 shows the format of mode registers 2, and Table 5 indicates the baud rate selections of the register. Bits 7 through 4 of mode register 2 control the transmitter baud rate, and bits 3 through 0 control the receiver baud rate. These registers are cleared by $\overline{\text{RESET}}$.

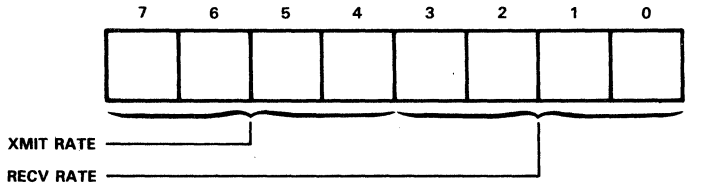


FIGURE 9. TCM78808 MODE REGISTERS 2 (LINE 0 THROUGH 6) FORMAT

PRINCIPLES OF OPERATION

TABLE 5. TCM78808 MODE REGISTERS 2 (LINES 0 THROUGH 6) DESCRIPTION

BIT	DESCRIPTION
7-0	XMIT RATE/RECV RATE (Transmitter/Receiver Rate). Selects the baud rate of the transmitter (bits 7 through 4) and receiver (bits 3 through 0) as follows:

Transmitter Bits				Receiver Bits				Nominal	Actual	Error†
7	6	5	4	3	2	1	0	Rate	Rate	(percent)
L	L	L	L	L	L	L	L	50	same	–
L	L	L	H	L	L	L	H	75	same	–
L	L	H	L	L	L	H	L	110	109.09	0.826
L	L	H	H	L	L	H	H	134.5	133.33	0.867
L	H	L	L	L	H	L	L	150	same	–
L	H	L	H	L	H	L	H	300	same	–
L	H	H	L	L	H	H	L	600	same	–
L	H	H	H	L	H	H	H	1200	same	–
H	L	L	L	H	L	L	L	1800	1745.45	3.03
H	L	L	H	H	L	L	H	2000	2021.05	1.05
H	L	H	L	H	L	H	L	2400	same	–
H	L	H	H	H	L	H	H	3600	3490.91	3.03
H	H	L	L	H	H	L	L	4800	same	–
H	H	L	H	H	H	L	H	7200	6981.81	3.03
H	H	H	L	H	H	H	L	9600	same	–
H	H	H	H	H	H	H	H	19200	same	–

† The frequency of the clock input (CLK) is 4.9152 MHz. The clock input may vary by 0.1%. This variance results in an error that must be added to the error listed in the error column.

command register

These read/write registers control various functions on the selected line. Figure 10 shows the format of the command registers, and Table 6 describes the function of the register information.

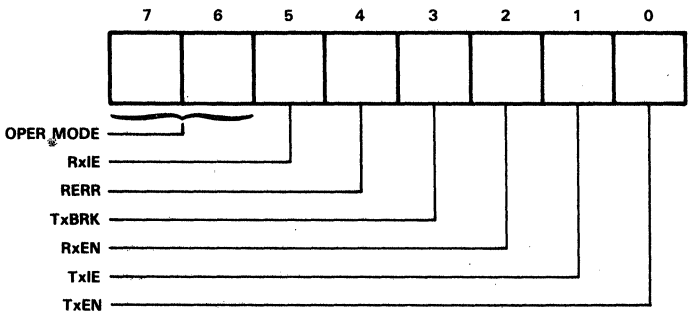


FIGURE 10. TCM78808 COMMAND REGISTERS (LINE 0 THROUGH 6) FORMAT

PRINCIPLES OF OPERATION

TABLE 6. TCM78808 COMMAND REGISTERS (LINES 0 THROUGH 7) DESCRIPTION

BIT	DESCRIPTION
7,6	OPER MODE (Operation Mode). These bits control the operating mode of the channel as follows. These bits are cleared by $\overline{\text{RESET}}$. Bit 7 / Bit 6 / Operating Mode L / L / Normal operation L / H / Automatic echo H / L / Local loopback H / H / Remote loopback
5	RxIE (Receiver Interrupt Enable). When set, the RxRDY flag (bit 1) of the status register for this line will generate an interrupt.
4	RERR (Reset Error). When set, this bit clears the framing error, overrun error, and parity error of the status register associated with this line. This bit is cleared by $\overline{\text{RESET}}$. It is not self-clearing.
3	TxBRK (Transmit Break). When set, this bit forces the appropriate TxD7-TxD0 line to the spacing state at the conclusion of the character presently being transmitted. When the program clears this bit, normal operation is restored, and any character pending in the transmitter holding register is moved into the serialization logic and transmitted. The minimum break length obtainable is twice the character length plus 1 bit time. The maximum break length depends on the amount of time between the program setting and clearing this bit, but is an integral number of bit times. This bit is cleared by $\overline{\text{RESET}}$.
2	RxEN (Receiver Enable). When set, this bit enables the receiver logic. When cleared, it stops the assembling of the received character, clears all receiver error bits and the RxRDY (bit 1) of the status register, clears any receiver interrupt conditions associated with this line, and initializes all receiver logic. This bit is cleared by $\overline{\text{RESET}}$.
1	TxIE (Transmit Interrupt Enable). When set, the state of the associated TxRDY flag (bit 0) of the status register is made available to the interrupt scanner logic. When the interrupt scanner logic scans this line, it determines if the TxRDY flag is set and, if so, generates an interrupt.
0	TxEN (Transmitter Enable). When set, this bit enables the transmitter logic. When cleared, it inhibits the serialization of the characters that follow, but the serialization of the current character is completed. It also clears the TxRDY flag (bit 0) of the status register, clears any transmitter interrupt conditions associated with the transmitter holding register, and initializes all transmitter logic except that associated with the transmitter holding register. The character in the transmitter holding register is retained so that XON/XOFF situations can be properly processed. This bit is cleared by $\overline{\text{RESET}}$.

Bits 5 through 0 enable the line receiver and transmitter, enable handling of interrupts, initiate the transmission of break characters, and reset error bits for the line. Refer to the "Interrupt Scanner and Interrupt Handling" paragraphs for detailed interrupt information. Bits 7 and 6 control the operating mode of the line. The four modes that can be set are normal operation, automatic echo, local loopback, and remote loopback.

normal operation

The serial data received is assembled in the receiver logic and transferred in parallel to the receiver buffer register. The RxEN bit must be set. Data to be transmitted is loaded in parallel into the transmitter holding register, then automatically transferred into the transmitter logic and serialized for transmission. The TxEN bit must be set.

automatic echo

The serial data received is assembled into parallel form in the receiver logic (the RxEN bit must be set) and transferred to the receiver buffer register. Arriving serial data is also routed to the line's TxDn pin for serial output. TxEN is ignored, and the transmitter logic is disabled. TxRDY flags and TxEMT indications are cleared. No transmitter interrupts are generated.

PRINCIPLES OF OPERATION

local loopback

The serial data from the RxDn input is ignored, and the receiver serial input receives data from the transmitter serial output. That data is assembled into parallel form in the receiver logic (the RxEN bit must be set) and transferred to the receiver buffer register where it can be read by the program. Data to be transmitted to the receiver is loaded in parallel form into the transmitter holding register from which it is automatically moved into the transmitter logic and serialized for transmission. The TxEN bit must be set. The transmission goes only to the receiver serial input; the TxDn output is held high. As in normal operation, transmission and reception baud rates are controlled by the transmitter speed and receiver speed entries in mode register 2.

remote loopback

The serial data received on the RxDn line is returned to the TxDn line without further action. No data is received or transmitted. The RxRDY, TxRDY, and TxEMT flags are disabled. The TxEN and RxEN bits of the command register are held cleared, causing the transmitter and receiver logic to be disabled.

summary registers

The TCM78808 contains two registers that summarize the current status of all eight serial data lines, making it possible to determine that a line status has changed with a a single read operation. These registers are selected for access by setting the appropriate address on inputs A2 through A0. Because the registers are shared by eight serial lines, the line-selection bits A5 through A3 are ignored when these registers are accessed. Refer to "Interrupt Scanner and Interrupt Handling" for detailed interrupt information.

interrupt summary register

This read-only register indicates that a transmitter or receiver interrupt condition has occurred and indicates the line number that generated the interrupt. Figure 11 shows the format of the interrupt summary register, and Table 7 describes register information.

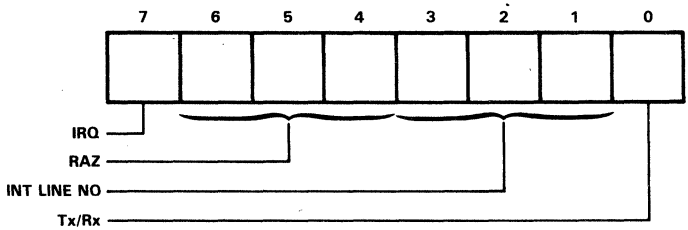


FIGURE 11. TCM78808 INTERRUPT SUMMARY REGISTER FORMAT

PRINCIPLES OF OPERATION

TABLE 7. TCM78808 INTERRUPT SUMMARY REGISTER DESCRIPTION

BIT	DESCRIPTION
7	IRQ (Interrupt Request). When set, this bit indicates that the interrupt scanner has found an interrupting condition among the eight serial lines of the TCM78808. These conditions also result in activating the IRQ signal.
6,5,4	RAZ (Read as Zero). Not used
3,2,1†	INT LINE NO (Interrupting Line Number). These bits indicate the line number upon which an interrupting condition was found. These bits correspond to the IRQLN2-IRQLNO signals: bit 3 = IRQLN2, bit 2 = IRQLN1, and bit 1 = IRQLNO. See Table 2.
0†	Tx/Rx (Transmit/Receive). This bit indicates whether the interrupting condition was caused by a transmitter (Tx/Rx = 1) or a receiver (Tx/Rx = 0). This bit corresponds to the IRQTxRx signal of the TCM78808 and is set when IRQTxRx is set.

† Bits 3-0 above represent the outputs of a free-running counter and are valid only when bit 7 is set.

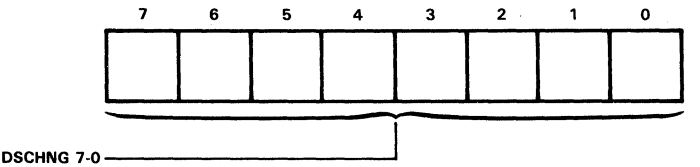


FIGURE 12. TCM78808 DATA SET CHANGE SUMMARY REGISTER FORM

When the MCIE bit in a line mode register 1 is set and RxIE is also set, the modem control interrupts are enabled for that line. If DSCHNG for that line is then set, the interrupt scanner will halt and generate an interrupt. The data set change summary register bits are cleared by writing a high into the bit position. A program that uses this register should read and save a copy of its contents. The copy can then be written back to the register to clear the bits that were set. The system interrupts should be disabled, and writeback should directly follow the read operation.

The $\overline{\text{RESET}}$ signal disables and initializes the data set change logic. When the $\overline{\text{RESET}}$ signal is high, future changes in $\overline{\text{DSR}}$ and $\overline{\text{DCD}}$ are reported as they occur.

interrupt scanner and interrupt handling

The interrupt scanner is a 4-bit counter that sequentially checks lines 0 through 7 for a receiver interrupt (counter positions 0 through 7) and then checks the lines in the same order for a transmitter interrupt (counter positions 8 through 15). If the scanner detects an interrupt condition, it stops, and the $\overline{\text{IRQ}}$ signal goes low. An interrupt must be serviced by software, or no other interrupt request can be posted.

The scanner determines that a line has a receiver interrupt if the line receiver buffer is ready and receiver interrupts are enabled for that line (RxRDY and RxIE = H) or if either of the line modem status signals has changed state and both receiver and modem control interrupts are enabled for that line (DSCHNG, RxIE, and MCIE all high).

The scanner determines that a line has a transmitter interrupt if the line's transmitter holding the register is empty and transmitter interrupts are enabled for that line (TxRDY and TxIE both high).

PRINCIPLES OF OPERATION

When the scanner detects an interrupt, it reports the line number on the IRQ2-IRQ0 lines. The IRQTxRx signal is high for a transmitter interrupt and is low for a receiver interrupt. The appropriate bits are also updated in the interrupt summary register. The $\overline{IRQ}$ line goes high, and the scanner is restarted for each of the following three types of interrupt conditions:

1. Reading the receiver buffer or resetting the RxIE bit of the interrupting line for the first type of receiver interrupt previously described.
2. Resetting the MCIE, RxIE, or DSCHNG bit of the interrupting line for the second type of receiver interrupt previously described.
3. Loading the transmitter holding register or resetting the TxIE bit of the interrupting line for transmitter interrupts.

If the scanner was originally stopped by a receiver interrupt condition, the scanner resumes sequential operation from where it stopped, thus providing receivers with equal priority. If the scanner was stopped by a transmitter condition, the scanner restarts from position 0 (line receiver), thus giving receivers priority over transmitters.

edge-triggered and level-triggered interrupt systems

If the interrupt system of the TCM78808 is used only for generating interrupts for the RxRDY and/or TxRDY flags, the $\overline{IRQ}$ line can be connected to a processor having either edge-triggered or level-triggered interrupt capability. If the modem control interrupts are being used (MCIE in mode register 1 = 1), the $\overline{IRQ}$ line can be connected only to a processor that uses level-triggered interrupts.

modem handling

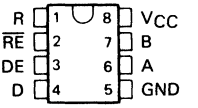
The TxEMT (transmitter empty) bit of the status register is typically used to indicate when a program can disable the transmission medium, as when deactivating the request-to-send line of a modem. A typical program will load the last character for transmission and then monitor the TxEMT bit of the status register.

The setting of the TxEMT bit to indicate that transmission is complete may occur a substantial time after the loading of the last character. After the last character is loaded, one character is in the transmitter holding register, and one character is in the serialization logic. Therefore, it will be two character times before the transmission process is completed. Waiting for the TxRDY signal to be set before monitoring the TxEMT status shortens this by one character time because the TxRDY status bit indicates that there are no characters in the transmitter holding register. The times involved are calculated by taking the reciprocal of the baud rate being used, multiplying by the number of bits per character [a start bit - 5, 6, 7, or 8 data bits (plus parity bit if enabled) and 1, 1.5, or 2 stop bits], and multiplying by either two characters or one depending on when TxEMT monitoring begins.

D3408, NOVEMBER 1988 – REVISED JANUARY 1990

- Bidirectional Transceiver
- Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27
- High-Speed Advanced Low-Power Schottky Circuitry
- Designed for 25-MBaud Operation in Both Serial and Parallel Applications
- Low Skew . . . 8 ns Max
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Low Supply Current Requirements 30 mA Max
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capacity . . . ±60 mA
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedances . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV Max
- Receiver Input Hysteresis . . . 70 mV Typ
- Fail Safe . . . High Receiver Output with Inputs Open
- Operates from a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection
- Interchangeable with National DS3695

D OR P PACKAGE
(TOP VIEW)



FUNCTION TABLE (DRIVER)

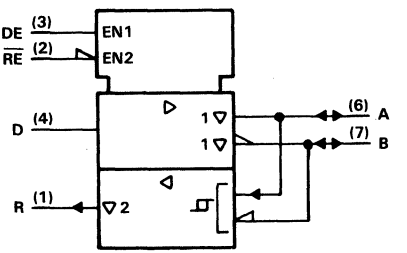
INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A – B	$\overline{RE}$	R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Inputs Open	L	H

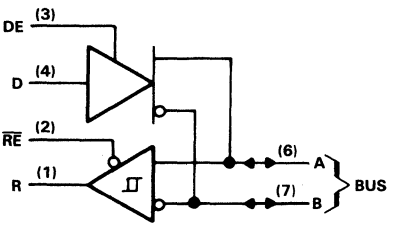
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



description

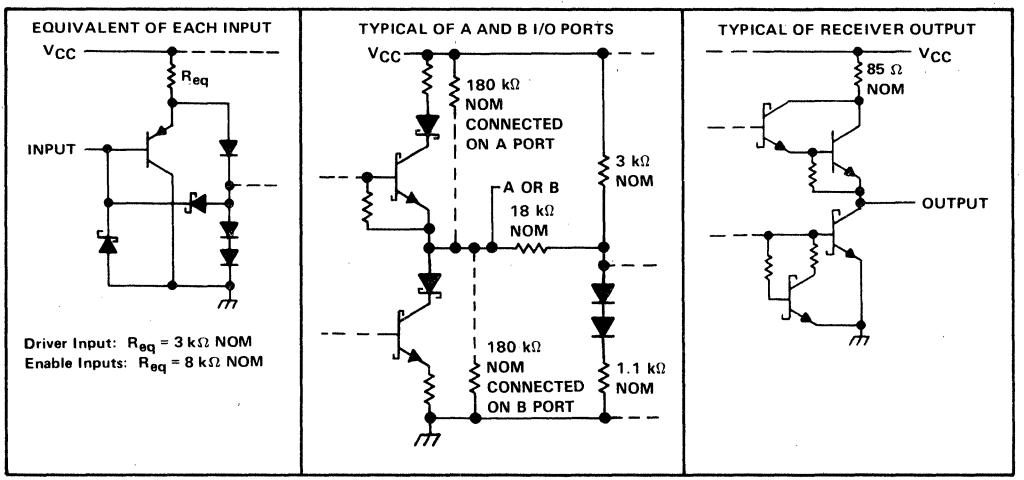
The TL3695 Differential Bus Transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meets EIA Standards RS-422-A and RS-485 and CCITT recommendations V.11 and X.27.

The TL3695 combines a 3-state differential line driver and a differential input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs

and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. This port features wide positive and negative common-mode voltage ranges making the device suitable for party line applications.

The TL3695 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Enable input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	I_O = 0		1.5		5	V
$\lvert V_{OD2} \rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	1/2 V_{OD1}			
				2			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	V_{test} = −7 V to 12 V,	See Figure 2	1.5		5	V
$\Delta \lvert V_{OD} \rvert$	Change in magnitude of differential output voltage§	R_L = 54 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3	V
$\Delta \lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Output disabled, See Note 3	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				−200	µA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = 0				−150	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current	No load	Outputs enabled		23	50	mA
			Outputs disabled		19	35	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ $\Delta \lvert V_{OD} \rvert$ and $\Delta \lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

driver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
t_{DD}	Differential-output delay time	$C_{L1} = C_{L2} = 100$ pF,	$R_L = 60\ \Omega$,	See Figure 3		8	22	ns
	Skew ($\lvert t_{DDH} - t_{DDL} \rvert$)					1	8	ns
t_{TD}	Differential output transition time					8	18	ns
t_{PZH}	Output enable time to high level	$C_L = 100$ pF,	$R_L = 500\ \Omega$,	See Figure 4			50	ns
t_{PZL}	Output enable time to low level	$C_L = 100$ pF,	$R_L = 500\ \Omega$,	See Figure 5			50	ns
t_{PHZ}	Output disable time from high level	$C_L = 15$ pF,	$R_L = 500\ \Omega$,	See Figure 4		8	30	ns
t_{PLZ}	Output disable time from low level	$C_L = 15$ pF,	$R_L = 500\ \Omega$,	See Figure 5		8	30	ns

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o	V_o
$\lvert V_{OD2} \rvert$	V_t ($R_L = 100\ \Omega$)	V_t ($R_L = 54\ \Omega$)
$\lvert V_{OD3} \rvert$		V_t (Test Termination Measurement 2)
V_{test}		V_{tst}
$\Delta \lvert V_{OD} \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis§	V_{OC} = 0			70		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV or Inputs open I_{OH} = −400 µA,	See Figure 6	2.4			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 16 mA			0.5	V
		See Figure 6	I_{OL} = 8 mA			0.45	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	µA
I_I	Line input current	Other input = 0 V,	V_I = 12 V			1	mA
		See Note 4	V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	µA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	µA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current	V_O = 0		−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		23	50	mA
			Outputs disabled		19	35	

NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V,	C_L = 15 pF,		14	37	ns
t_{PHL}	Propagation delay time, high-to-low-level output	See Figure 7			14	37	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 8		7	20	ns
t_{PZL}	Output enable time to low level				7	20	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 8		7	16	ns
t_{PLZ}	Output disable time from low level				8	16	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

PARAMETER MEASUREMENT INFORMATION

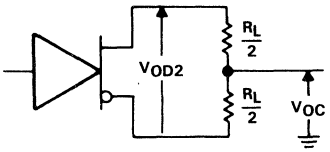


FIGURE 1. DRIVER V_{OD} AND V_{OC}

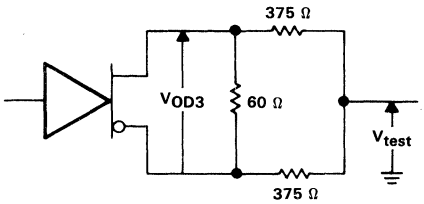
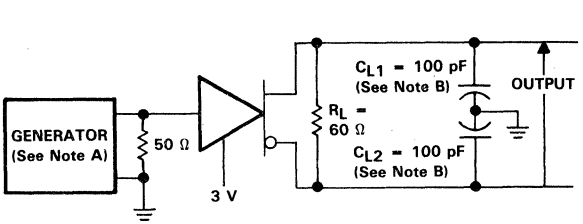
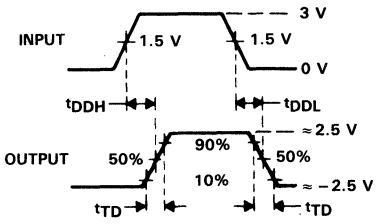


FIGURE 2. DRIVER V_{OD3}



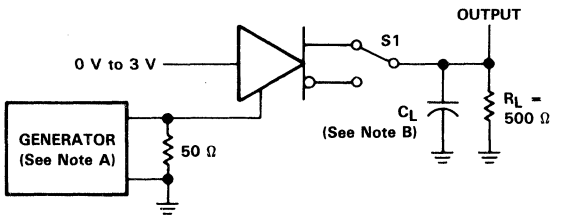
TEST CIRCUIT



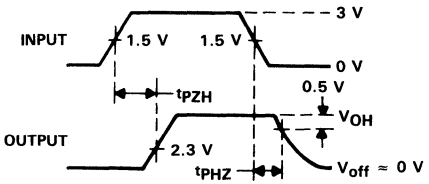
VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES



TEST CIRCUIT

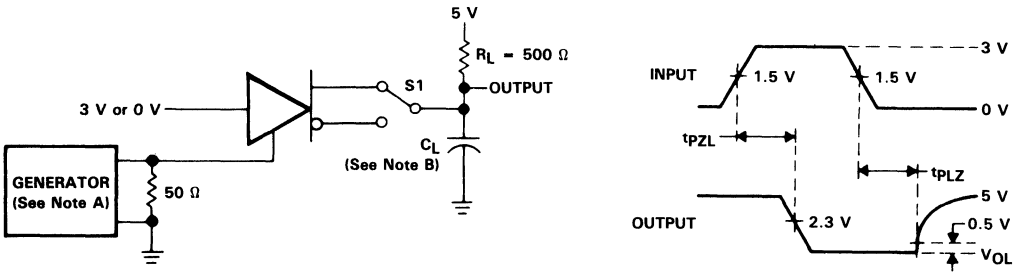


VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance. (See switching characteristics — test conditions)

FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance. (See switching characteristics — test conditions)

FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

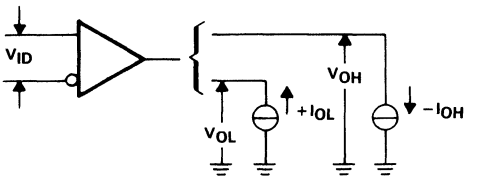
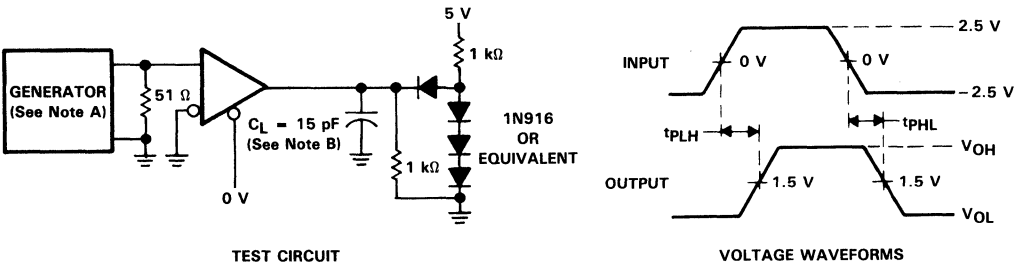


FIGURE 6. RECEIVER V_{OH} AND V_{OL}

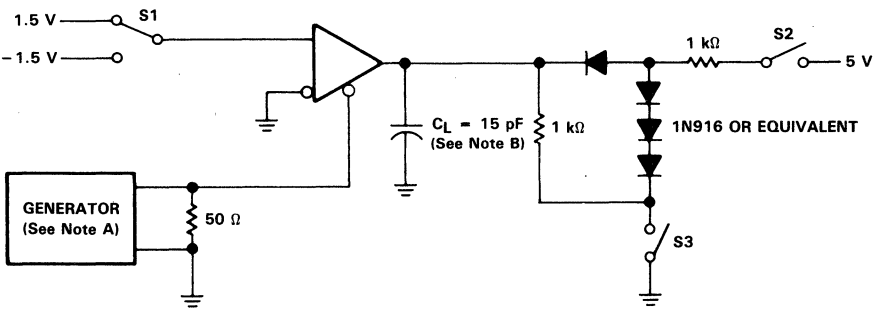


TEST CIRCUIT VOLTAGE WAVEFORMS

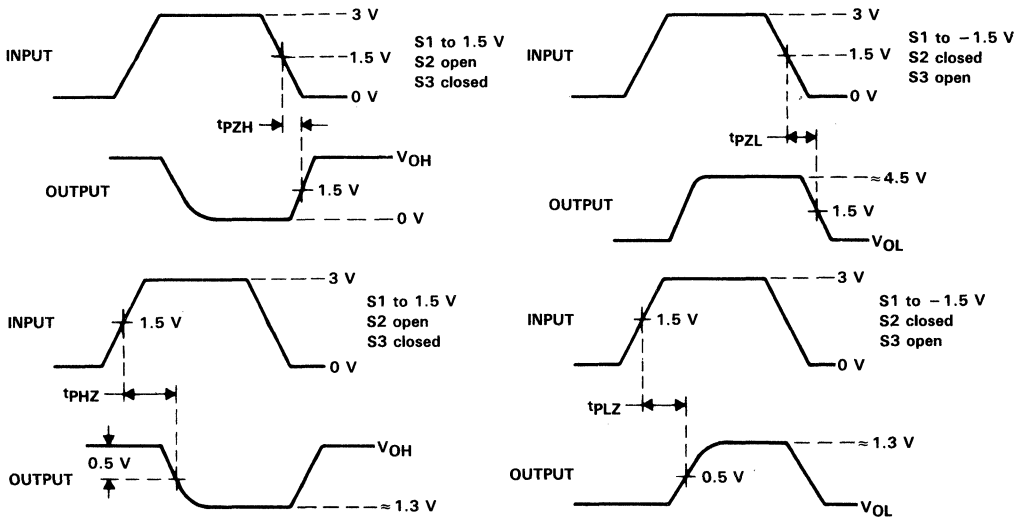
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 7. RECEIVER PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 8. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

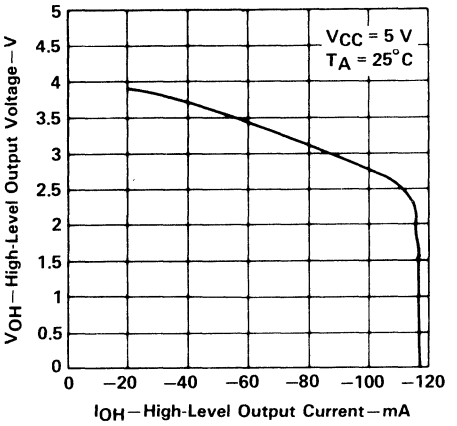


FIGURE 9

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

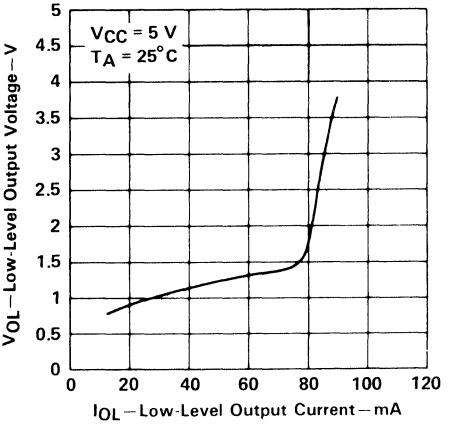


FIGURE 10

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

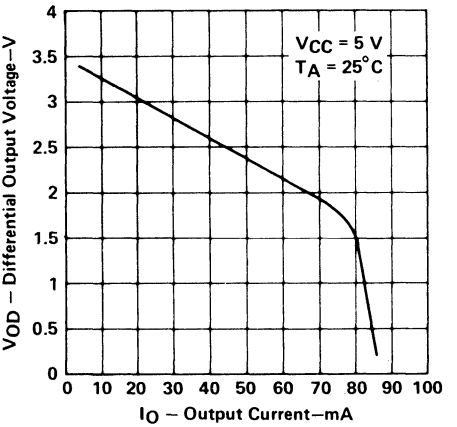


FIGURE 11

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

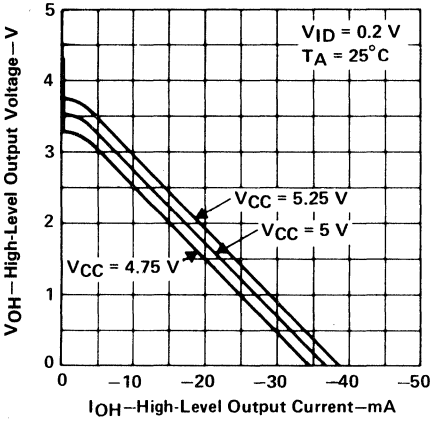


FIGURE 12

RECEIVER HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

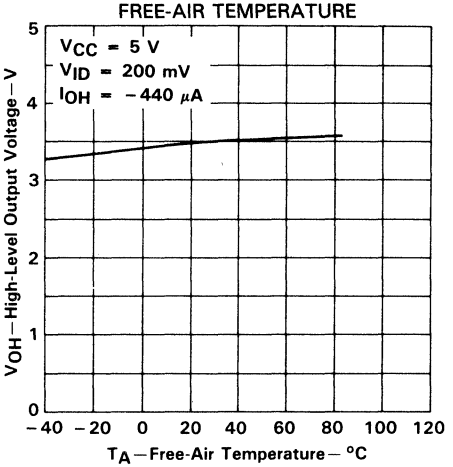


FIGURE 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

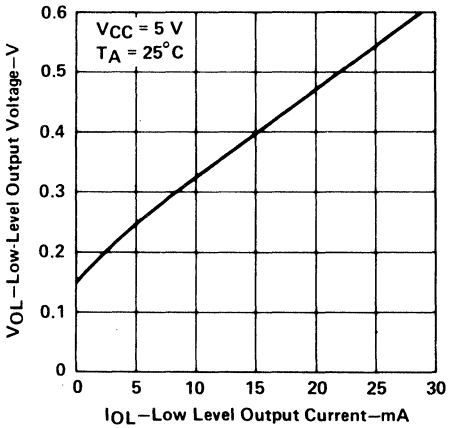


FIGURE 14

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

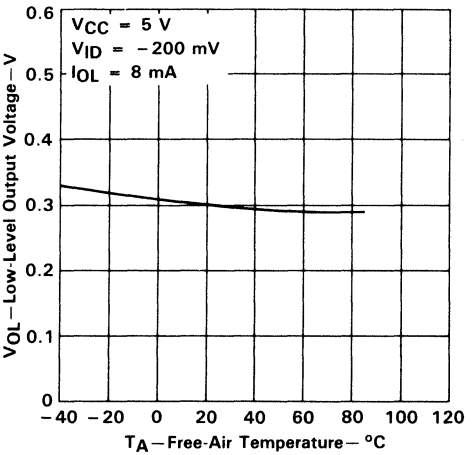


FIGURE 15

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

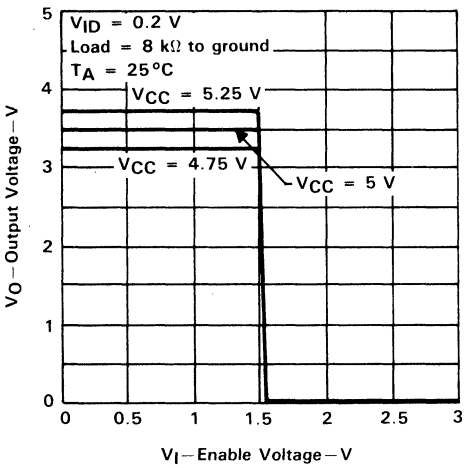


FIGURE 16

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

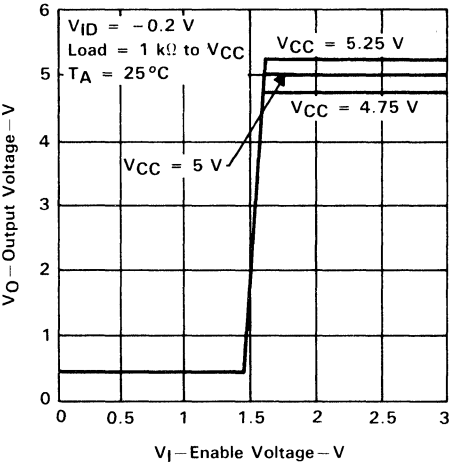
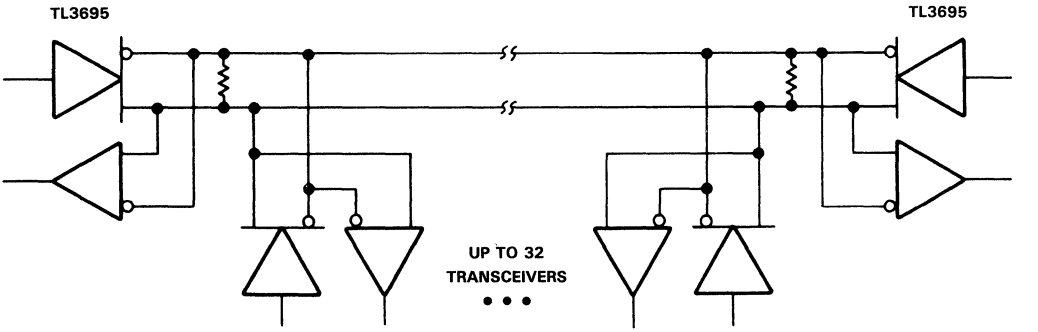


FIGURE 17

APPLICATION INFORMATION



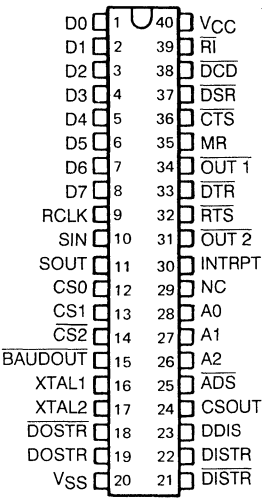
NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 18. TYPICAL APPLICATION CIRCUIT

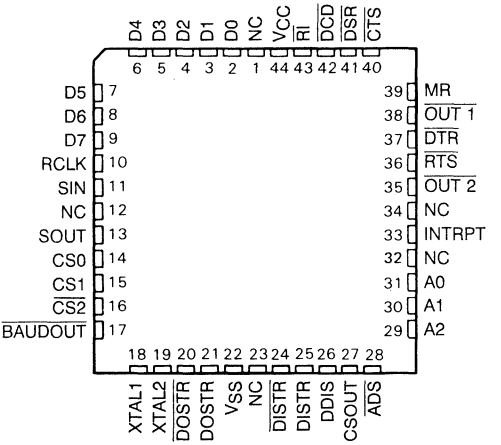
D3096, MARCH 1988 – REVISED APRIL 1989

- **Programmable Baud Rate Generator Allows Division of Any Input Reference Clock by 1 to ($2^{16}-1$) and Generates an Internal 16 X Clock**
- **Full Double Buffering Eliminates the Need for Precise Synchronization**
- **Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or from the Serial Data Stream**
- **Independent Receiver Clock Input**
- **Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts**
- **Fully Programmable Serial Interface Characteristics:**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even-, Odd-, or No-Parity Bit Generation and Detection**
  - **1-, 1 1/2-, or 2-Stop Bit Generation**
  - **Baud Generation (DC to 256 Kilobits per Second)**
- **False Start Bit Detection**
- **Complete Status Reporting Capabilities**
- **Three-State TTL Drive Capabilities for Bidirectional Data Bus and Control Bus**
- **Line Break Generation and Detection**
- **Internal Diagnostic Capabilities:**
  - **Loopback Controls for Communications Link Fault Isolation**
  - **Break, Parity, Overrun, Framing Error Simulation**
- **Full Prioritized Interrupt System Controls**
- **Modem Control Functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, and $\overline{DCD}$)**
- **Easily Interfaces to Most Popular Microprocessors**
- **Faster Plug-In Replacement for National Semiconductor NS16C450**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

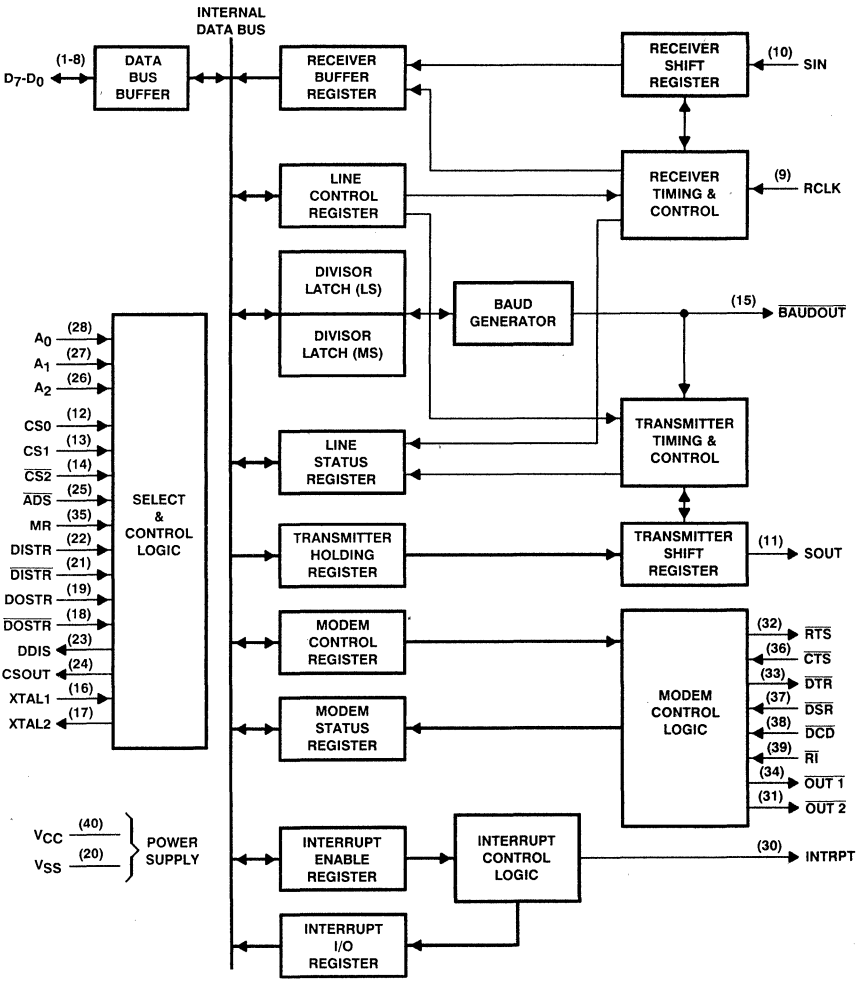
The TL16C450 is a CMOS version of an Asynchronous Communications Element (ACE). It typically functions in a microcomputer system as a serial input/output interface.

The TL16C450 performs serial-to-parallel conversion on data received from a peripheral device or modem and parallel-to-serial conversion on data received from its CPU. The CPU can read and report on the status of

the ACE at any point in the ACE's operation. Reported status information includes: the type of transfer operation in progress, the status of the operation, and any error conditions encountered.

The TL16C450 ACE includes a programmable, on-board, baud rate generator. This generator is capable of dividing a reference clock input by divisors from 1 to ($2^{16}-1$) and producing a 16 X clock for driving the internal transmitter logic. Provisions are also included to use this 16 X clock to drive the receiver logic. Also included in the ACE is a complete modem control capability and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

block diagram



Pin numbers shown are for the N package.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

PIN NAME	PIN NO.†	I/O	DESCRIPTION
A0 A1 A2	28 [31] 27 [30] 26 [29]	I	Register Select. Three inputs used during read and write operations to select the ACE register to read from or write to. Refer to Table 1 for register addresses, also refer to the Address Strobe ($\overline{ADS}$) signal description.
$\overline{ADS}$	25 [28]	I	Address Strobe. When $\overline{ADS}$ is active (low), the Register Select signals (A0, A1, and A2) and Chip Select signals (CS0, CS1, $\overline{CS2}$) drive the internal select logic directly; when high, the Register Select and Chip Select signals are held in the state they were in when the low-to-high transition of $\overline{ADS}$ occurred.
$\overline{BAUDOUT}$	15 [17]	O	Baud Out. 16 X clock signal for the transmitter section of the ACE. The clock rate is established by the reference oscillator frequency divided by a divisor specified by the Baud Generator Divisor Latches. $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input.
CS0 CS1 $\overline{CS2}$	12 [14] 13 [15] 14 [16]	I	Chip Select. When active (high and low, respectively), these three inputs select the ACE. Refer to the $\overline{ADS}$ (Address Strobe) signal description.
CSOUT	24 [27]	O	Chip Select Out. When CSOUT is high, it indicates that the ACE has been selected by the Chip Select inputs (CS0, CS1, and $\overline{CS2}$). CSOUT is low when the chip is deselected.
$\overline{CTS}$	36 [40]	I	Clear To Send. $\overline{CTS}$ is a modem status signal whose condition can be checked by reading bit 4 (CTS) of the Modem Status Register. Bit 0 (DCTS) of the Modem Status Register indicates that this signal has changed state since the last read from the Modem Status Register. If the Modem Status Interrupt is enabled when $\overline{CTS}$ changes state, an interrupt is generated.
D0 D1 D2 D3 D4 D5 D6 D7	1 [2] 2 [3] 3 [4] 4 [5] 5 [6] 6 [7] 7 [8] 8 [9]	I/O	Data Bus. Eight 3-state data lines provide a bidirectional path for data, control, and status information between the ACE and the CPU.
$\overline{DCD}$	38 [42]	I	Data Carrier Detect. $\overline{DCD}$ is a modem status signal whose condition can be checked by reading bit 7 (DCD) of the Modem Status Register. Bit 3 (DDCD) of the Modem Status Register indicates that this signal has changed state since the last read from the Modem Status Register. If the Modem Status Interrupt is enabled when the $\overline{DCD}$ changes state, an interrupt is generated.
DDIS	23 [26]	O	Driver Disable. This output is active (high) when the CPU is not reading data. When active, this output can be used to disable an external transceiver.
DISTR $\overline{DISTR}$	22 [25] 21 [24]	I	Data Input Strobes. When either input is active (high or low, respectively) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register. Only one of these inputs is required for the transfer of data during a read operation; the other input should be tied in its inactive state (i.e., DISTR tied low or $\overline{DISTR}$ tied high).
DOSTR $\overline{DOSTR}$	19 [21] 18 [20]	I	Data Output Strobes. When either input is active (high or low, respectively), while the ACE is selected, the CPU is allowed to write control words or data into a selected ACE register. Only one of these inputs is required to transfer data during a write operation; the other input should be tied in its inactive state (i.e., DOSTR tied low or $\overline{DOSTR}$ tied high).
$\overline{DSR}$	37 [41]	I	Data Set Ready. $\overline{DSR}$ is a modem status signal whose condition can be checked by reading bit 5 (DSR) of the Modem Status Register. Bit 1 (DDSR) of the Modem Status Register indicates that this signal has changed state since the last read from the Modem Status Register. If the modem status interrupt is enabled when the $\overline{DSR}$ changes state, an interrupt is generated.
$\overline{DTR}$	33 [37]	O	Data Terminal Ready. When active (low), $\overline{DTR}$ informs a modem or data set that the ACE is ready to establish communication. $\overline{DTR}$ is placed in the active state by setting the DTR bit of the Modem Control Register to a high level. $\overline{DTR}$ is placed in the inactive state either as a result of a Master Reset or during loop mode operation or resetting bit 0 (DTR) of the Modem Control Register.
INTRPT	30 [33]	O	Interrupt. When active (high), INTRPT informs the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are; a receiver error, received data is available, the transmitter holding register is empty, and an enabled modem status interrupt. The INTRPT output is reset (inactivated) either when the interrupt is serviced or as a result of a Master Reset.

† Pin numbers shown in brackets are for the FN package.

PIN NAME	PIN NO.†	I/O	DESCRIPTION
MR	35 [39]	I	Master Reset. When active (high), MR clears most ACE registers and sets the state of various output signals. Refer to Table 2, ACE Reset Functions.
$\overline{OUT\ 1}$ $\overline{OUT\ 2}$	34 [38] 31 [35]	O	Outputs 1 and 2. User-designated output pins that are set to their active states by setting their respective Modem Control Register bits (OUT 1 and OUT 2) high. $\overline{OUT\ 1}$ and $\overline{OUT\ 2}$ are set to their inactive (high) states as a result of Master Reset or during loop mode operations or by resetting bit 2 (OUT 1) or bit 3 (OUT 2) of the MCR.
RCLK	9 [10]	I	Receiver Clock. The 16 X baud rate clock for the receiver section of the ACE.
$\overline{RI}$	39 [43]	I	Ring Indicator. $\overline{RI}$ is a modem status signal whose condition can be checked by reading bit 6 (RI) of the Modem Status Register. Bit 2 (TERI) of the Modem Status Register indicates that the $\overline{RI}$ input has transitioned from a low to a high state since the last read from the Modem Status Register. If the Modem Status Interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{RTS}$	32 [36]	O	Request to Send. When active, informs the modem or data set that the ACE is ready to transmit data. $\overline{RTS}$ is set to its active state by setting the RTS Modem Control Register bit and is set to its inactive (high) state either as a result of a Master Reset or during loop mode operations or by resetting bit 1 (RTS) of the MCR.
SIN	10 [11]	I	Serial Input. Serial data input from a connected communications device.
SOUT	11 [13]	O	Serial Output. Composite serial data output to a connected communication device. SOUT is set to the Marking (logic 1) state as a result of Master Reset.
V_{CC}	40 [44]		5-V Supply Voltage
V_{SS}	20 [22]		Supply Common
XTAL1 XTAL2	16 [18] 17 [19]	I/O	External Clock. Connects the ACE to the main timing reference (clock or crystal).

† Pin numbers shown in brackets are for the FN package.

absolute maximum ratings over free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range at any input, V_I . . . . . −0.5 V to 7 V
Output voltage range, V_O . . . . . −0.5 V to 7 V
Continuous total dissipation at (or below) 70°C free-air temperature:
FN package . . . . . 1100 mW
N package . . . . . 800 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}‡	High-level output voltage	I_{OH} = −1 mA	2.4			V
V_{OL}‡	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
I_{lkg}	Input leakage current	V_{CC} = 5.25 V, V_{SS} = 0, V_I = 0 to 5.25 V, All other pins floating			±10	μA
I_{OZ}	High-impedance output current	V_{CC} = 5.25 V, V_{SS} = 0, V_O = 0 V to 5.25 V, chip selected, write mode or, chip deselected			±20	μA
I_{CC}	Supply current	V_{CC} = 5.25 V, T_A = 25°C, SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V, All other inputs at 0.8 V, XTAL1 at 4 MHz, No load on outputs. Baud rate = 50 kilobits per second			10	mA
C_{XTAL1}	Clock input capacitance	V_{CC} = 0, V_{SS} = 0, f = 1 MHz, T_A = 25°C, All other pins grounded		15	20	pF
C_{XTAL2}	Clock output capacitance			20	30	pF
C_i	Input capacitance			6	10	pF
C_o	Output capacitance			10	20	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ These parameters apply for all outputs except XTAL2.

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	MIN	MAX	UNIT
t_{cR}	Cycle time, read (t_{w7} + t_{d8} + t_{d9})		175		ns
t_{cW}	Cycle time, write (t_{w6} + t_{d5} + t_{d6})		175		ns
t_{w5}	Pulse duration, address strobe low	2, 3	15		ns
t_{w6}	Pulse duration, write strobe	2	80		ns
t_{w7}	Pulse duration, read strobe	3	80		ns
t_{wMR}	Pulse duration, master reset		1000		ns
t_{su1}	Setup time, address	2,3	15		ns
t_{su2}	Setup time, chip select	2,3	15		ns
t_{su3}	Setup time, data	2	15		ns
t_{h1}	Hold time, address	2,3	0		ns
t_{h2}	Hold time, chip select	2,3	0		ns
t_{h3}	Hold time, write to chip select	2	20		ns
t_{h4}	Hold time, write to address	2	20		ns
t_{h5}	Hold time, data	2	15		ns
t_{h6}	Hold time, read to chip select	3	20		ns
t_{h7}	Hold time, read to address	3	20		ns
t_{d4}§	Delay time, select to write	2	15		ns
t_{d5}§	Delay time, address to write	2	15		ns
t_{d6}	Delay time, write cycle	2	80		ns
t_{d7}§	Delay time, chip select to read	3	15		ns
t_{d8}§	Delay time, address to read	3	15		ns
t_{d9}	Delay time, read cycle	3	80		ns

§ Only applies when ADS is low.

system switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w1}	Pulse duration, clock high	1	f = 9 MHz maximum	50		ns
t_{w2}	Pulse duration, clock low	1	f = 9 MHz maximum	50		ns
t_{d3}	Delay time, select to CS output	2,3	C_L = 100 pF		70	ns
t_{d10}	Delay time, read to data	3	C_L = 100 pF		60	ns
t_{d11}	Delay time, read to floating data	3	C_L = 100 pF	0	60	ns
$t_{dis(R)}$	Read to driver disable	3	C_L = 100 pF		60	ns

baud generator switching requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w3}	Pulse duration, $\overline{\text{BAUDOUT}}$ low	1	f = 6.25 MHz, CLK ÷ 1, C_L = 100 pF	80		ns
t_{w4}	Pulse duration, $\overline{\text{BAUDOUT}}$ high	1	f = 6.25 MHz, CLK ÷ 1, C_L = 100 pF	80		ns
t_{d1}	Delay time, $\overline{\text{BAUDOUT}}$ low to high	1	C_L = 100 pF		125	ns
t_{d2}	Delay time, $\overline{\text{BAUDOUT}}$ high to low	1	C_L = 100 pF		125	ns

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d12}	Delay time, RCLK to sample	4			100	ns
t_{d13}	Delay time, stop to set interrupt	4		1	1	RCLK cycles
t_{d14}	Delay time, read RBR/LSR to reset interrupt	4	C_L = 100 pF		140	ns

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d15}	Delay time, initial write THR to transmit start	5		8	24	baudout cycles
t_{d16}	Delay time, stop to interrupt	5		8	8	baudout cycles
t_{d17}	Delay time, write THR to reset interrupt	5	C_L = 100 pF		140	ns
t_{d18}	Delay time, initial write to interrupt (THRE)	5		16	32	baudout cycles
t_{d19}	Delay time, read IIR to reset interrupt (THRE)	5	C_L = 100 pF		140	ns

modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d20}	Delay time, write MCR to output	6	C_L = 100 pF		100	ns
t_{d21}	Delay time, modem input to set interrupt	6	C_L = 100 pF		170	ns
t_{d22}	Delay time, read MSR to reset interrupt	6	C_L = 100 pF		140	ns

PARAMETER MEASUREMENT INFORMATION

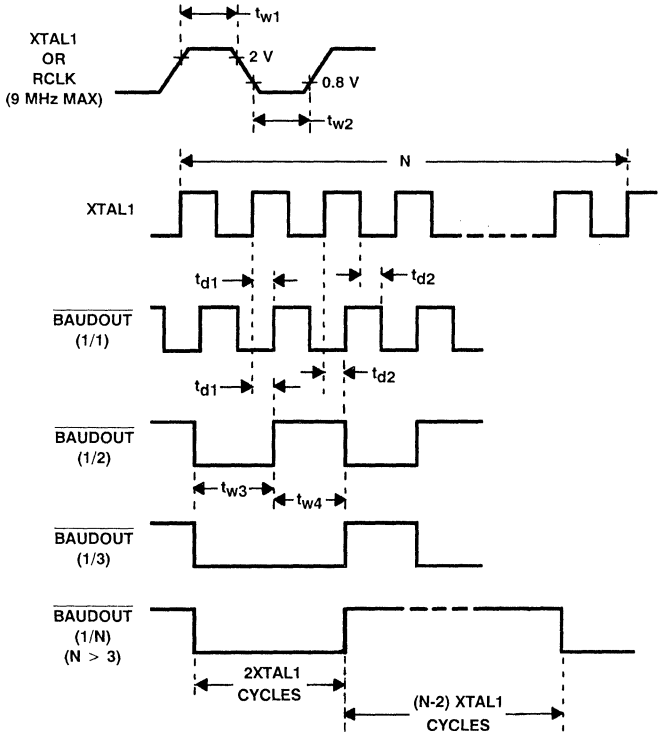
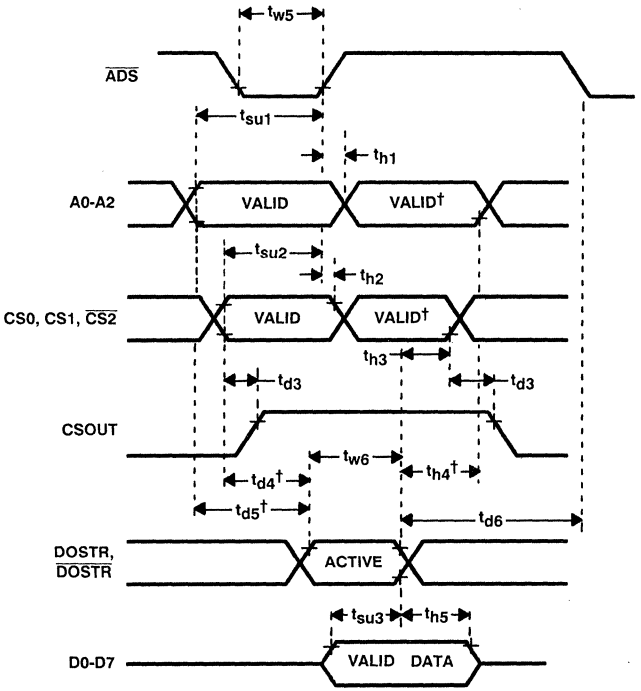


FIGURE 1. BAUD GENERATOR TIMING

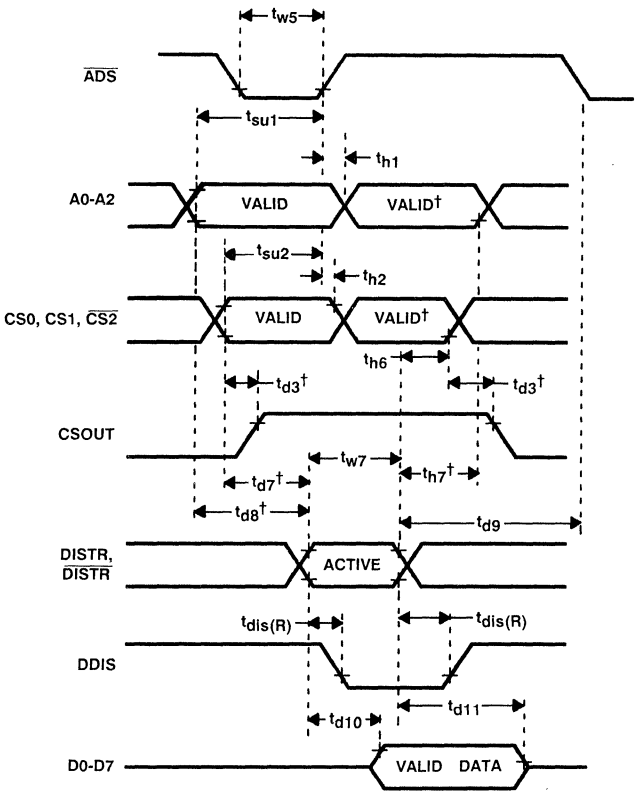
PARAMETER MEASUREMENT INFORMATION



† Applicable only when $\overline{ADS}$ is tied low.

FIGURE 2. WRITE CYCLE TIMING

PARAMETER MEASUREMENT INFORMATION



† Applicable only when ADS is tied low.

FIGURE 3. READ CYCLE TIMING

PARAMETER MEASUREMENT INFORMATION

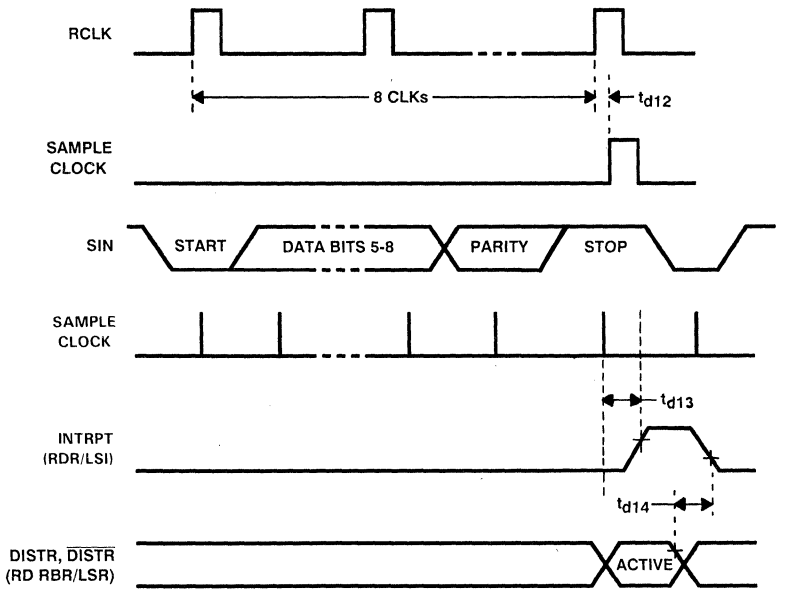


FIGURE 4. RECEIVER TIMING

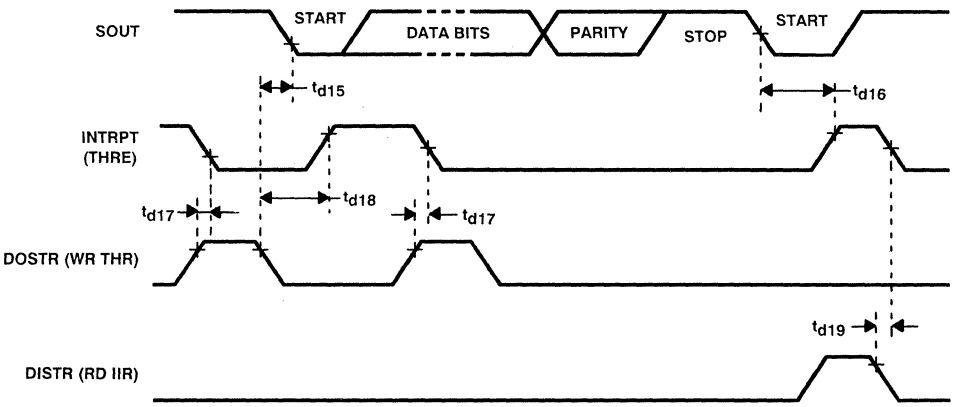


FIGURE 5. TRANSMITTER TIMING

PARAMETER MEASUREMENT INFORMATION

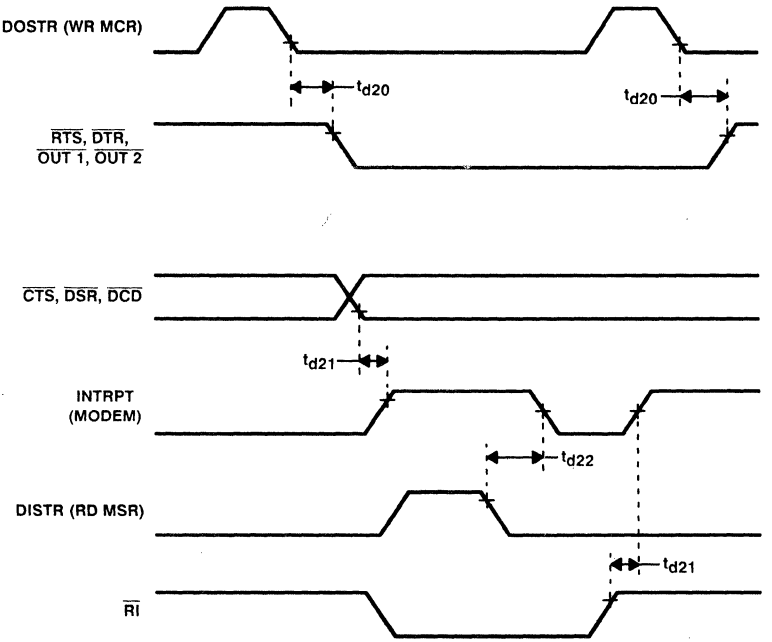


FIGURE 6. MODEM CONTROL TIMING

TYPICAL APPLICATION DATA

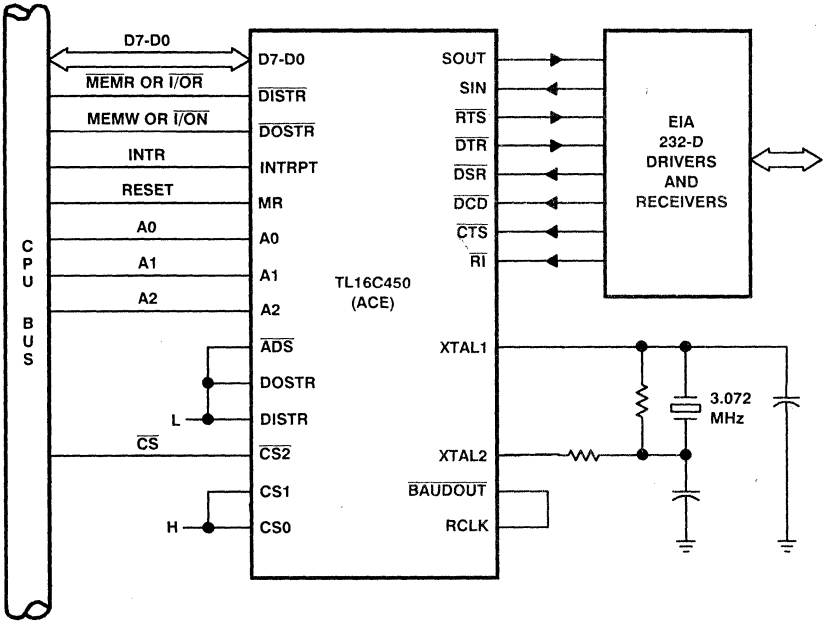


FIGURE 7. BASIC TL16C450 CONFIGURATION

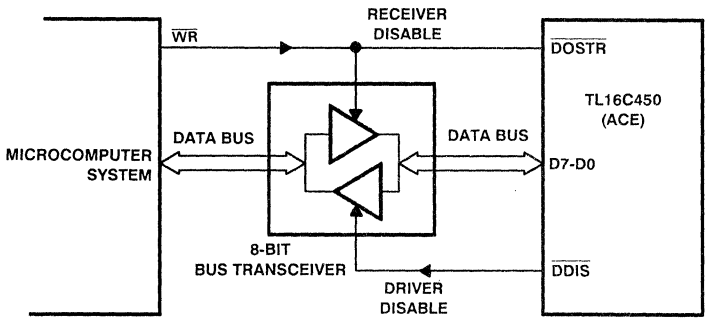


FIGURE 8. TYPICAL INTERFACE FOR A HIGH-CAPACITY DATA BUS

TYPICAL APPLICATION DATA

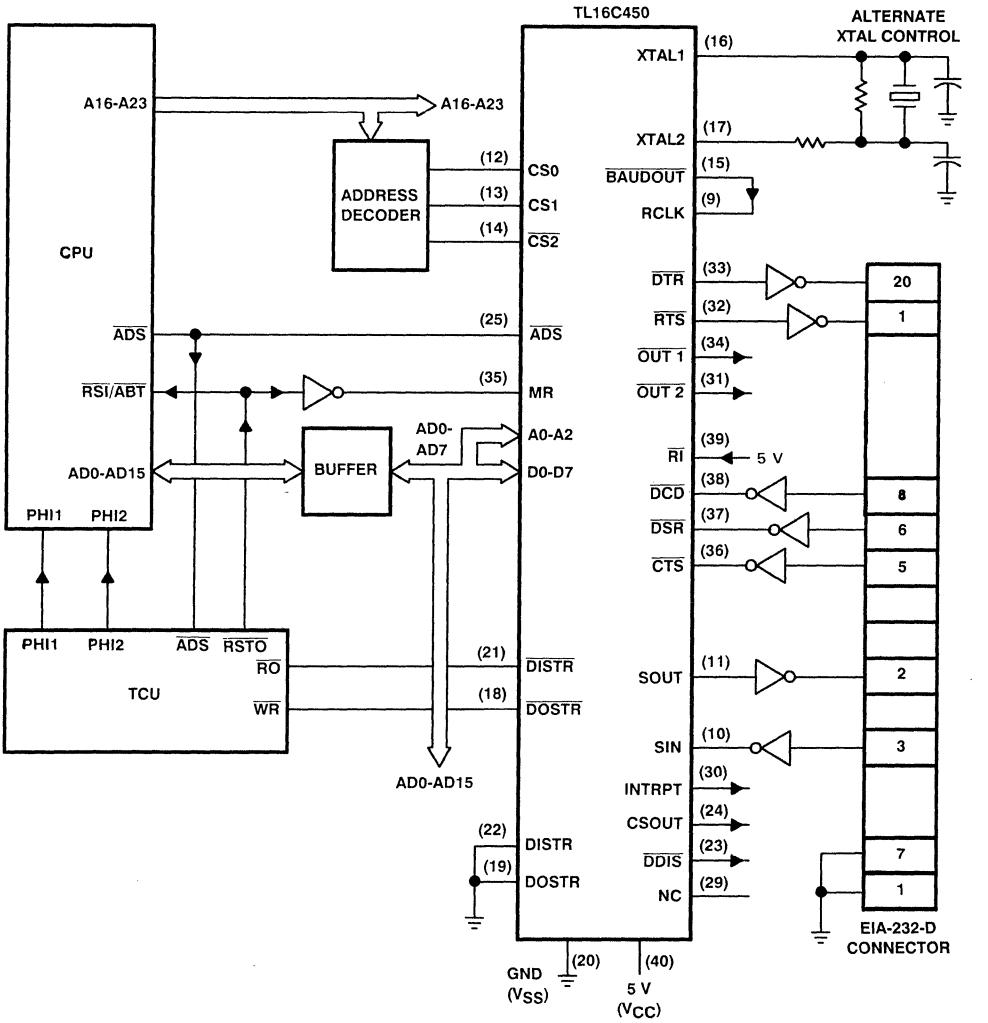


FIGURE 9. TYPICAL TL16C450 CONNECTION TO A CPU

PRINCIPLES OF OPERATION

TABLE 1. REGISTER SELECTION

DLAB†	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding register (write)
0	L	L	H	Interrupt enable
X	L	H	L	Interrupt identification (read only)
X	L	H	H	Line control
X	H	L	L	Modem control
X	H	L	H	Line status
X	H	H	L	Modem status
X	H	H	H	Scratch
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor Latch (MSB)

† The Divisor Latch Access Bit (DLAB) is the most significant bit of the Line Control Register. The DLAB signal is controlled by writing to this bit location (see Table 3).

TABLE 2. ACE RESET FUNCTIONS

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is high, bits 1 and 2 are low, and bits 3-7 are permanently low
Line Control Register	Master Reset	All bits low
Modem Control Register	Master Reset	All bits low
Line Status Register	Master Reset	Bits 5 and 6 are high, all other bits are low
Modem Status Register	Master Reset	Bits 0-3 are low, bits 4-7 are input signals
SOUT	Master Reset	High
INTRPT (Receiver Error Flag)	Read LSR/MR	Low
INTRPT (Received Data Available)	Read RBR/MR	Low
INTRPT (Transmitter Holding Register Empty)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{\text{OUT 2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{OUT 1}}$	Master Reset	High
Scratch Register	Master Reset	No effect
Divisor Latch (LSB and MSB) Registers	Master Reset	No effect
Receiver Buffer Register	Master Reset	No effect
Transmitter Holding Register	Master Reset	No effect

PRINCIPLES OF OPERATION

accessible registers

The system programmer, via the CPU, has access to and control over any of the ACE registers that are summarized in Table 3. These registers are used to control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

TABLE 3. SUMMARY OF ACCESSIBLE REGISTERS

Bit No.	REGISTER ADDRESS										
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	3	4	5	6	7	0 DLAB=1	1 DLAB=1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LSB)	Latch (MSB)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12	
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Cata Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

* Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

PRINCIPLES OF OPERATION

receiver buffer register (RBR)

The ACE's receiver section consists of a Receiver Shift Register and a Receiver Buffer Register. Timing is supplied by the 16 X Receiver Clock (RCLK). Receiver section control is a function of the ACE's Line Control Register.

The ACE's Receiver Shift Register receives serial data from the Serial Input (SIN) pin. The Receiver Shift Register then converts the data to a parallel form and loads it into the Receiver Buffer Register. When a character is placed in the Receiver Buffer Register and the Received Data Available interrupt is enabled, an interrupt is generated. This interrupt is cleared when the data is read out of the Receiver Buffer Register.

transmitter holding register (THR)

The ACE's transmitter section consists of a Transmitter Holding Register and a Transmitter Shift Register. Timing is supplied by the Baud Out ($\overline{\text{BAUDOUT}}$) clock signal. Transmitter section control is a function of the ACE's Line Control Register.

The ACE Transmitter Holding Register receives data off the Internal Data Bus and, when the shift register is idle, moves it into the Transmitter Shift Register. The Transmitter Shift Register serializes the data and outputs it at the Serial Output (SOUT). If the Transmitter Holding Register is empty and the Transmitter Holding Register Empty (THRE) interrupt is enabled, an interrupt is generated. This interrupt is cleared when a character is loaded into the register.

interrupt enable register (IER)

The Interrupt Enable Register enables each of the four types of interrupts (refer to Table 4) and the INTRPT output signal in response to an interrupt generation. The Interrupt Enable Register can also be used to disable the interrupt system by setting bits 0 through 3 to logic 0. The contents of this register are summarized in Table 3 and are described below.

Bit 0. This bit, when set to logic 1, enables the Received Data Available interrupt.

Bit 1. This bit, when set to logic 1, enables the Transmitter Holding Register Empty interrupt.

Bit 2. This bit, when set to logic 1, enables the Receiver Line Status interrupt.

Bit 3. This bit, when set to logic 1, enables the Modem Status interrupt.

Bits 4 thru 7. Bits 4 through 7 in the Interrupt Enable Register are not used and are always set to logic 0.

PRINCIPLES OF OPERATION

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most microprocessors.

The ACE provides four prioritized levels of interrupts:

Priority 1 – Receiver line status (highest priority)
Priority 2 – Receiver data ready
Priority 3 – Transmitter holding register empty
Priority 4 – Modem status (lowest priority)

When an interrupt is generated, the Interrupt Identification Register indicates that an interrupt is pending and the type of that interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 4.

Bit 0. This bit can be used either in a hardwire-prioritized, or polled interrupt system. If this bit is a logic 0, an interrupt is pending. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2. These two bits are used to identify the highest priority interrupt pending, as indicated in Table 4.

Bits 3 thru 7. Bits 3 through 7 in the Interrupt Identification Register are not used and are always set at logic 0.

TABLE 4. INTERRUPT CONTROL FUNCTIONS

INTERRUPT IDENTIFICATION REGISTER			PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 2	BIT 1	BIT 0				
0	0	1	None	None	None	–
1	1	0	1	Receiver line status	Overrun error, parity error, framing error or break interrupt	Reading the Line Status register
1	0	0	2	Received data available	Receiver data available	Reading the Receiver buffer Buffer register
0	1	0	3	Transmitter Holding register empty	Transmitter Holding register empty	Reading the Interrupt Identification register (if source of interrupt) or writing into the Transmitter Holding register
0	0	0	4	Modem status	Clear to Send, Data Set Ready, Ring Indicator, or Data Carrier Detect	Reading the Modem Status register

PRINCIPLES OF OPERATION

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the Line Control register. In addition, the programmer is able to retrieve, inspect, and modify the contents of the Line Control register; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and are described below.

Bits 0 and 1. These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2. This bit specifies either one, one and one-half, or two Stop bits in each transmitted character. If bit 2 is a logic 0, one Stop bit is generated in the data. If bit 2 is a logic 1, the number of Stop bits generated is dependent on the word length selected with bits 0 and 1. The Receiver checks the first Stop bit only, regardless of the number of Stop bits selected. The number of Stop bits generated, in relation to word length and bit 2, is shown in the following.

Bit 2	Word Length Selected by Bits 1 and 2	Number of Stop Bits Generated
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

Bit 3. This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, if bit 3 is a logic 1, parity is checked. When bit 3 is a logic 0, no parity is generated or checked.

Bit 4. Bit 4 is the Even Parity Select bit. When parity is enabled by bit 3: a logic 1 in bit 4 produces Even Parity (an even number of logic is in the data and parity bits) and a logic 0 in bit 4 produces Odd Parity (an odd number of logic 1s).

Bit 5. This is the Stick parity bit. When bits 3, 4, and 5 are logic 1s, the Parity bit is transmitted and checked as a logic 0. When bits 3 and 5 are logic 1s and bit 4 is a logic 0, the Parity bit is transmitted and checked as a logic 1.

Bit 6. This bit is the Break Control bit. Bit 6 is set to a logic 1 to force a break condition, i.e, a condition where the Serial Output (SOUT) pin is forced to the spacing (logic 0) state. When bit 6 is set to a logic 0, the break condition is disabled. The break condition has no effect on the transmitter logic, it only effects the serial output.

Bit 7. This bit is the Divisor Latch Access bit (DLAB). Bit 7 must be set to a logic 1 to access the Divisor Latches of the Baud Generator during a read or write. Bit 7 must be set to a logic 0 during a read or write to access the Receiver Buffer, the Transmitter Holding register, or the Interrupt Enable register.

modem control register (MCR)

The Modem Control register is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described below.

Bit 0. Bit 0 (DTR) controls the Data Terminal Ready ($\overline{DTR}$) output. Setting this bit to a logic 1 forces the $\overline{DTR}$ output to its active state (low). When bit 0 is set to a logic 0, $\overline{DTR}$ goes high.

Bit 1. Bit 1 (RTS) controls the Request to Send ($\overline{RTS}$) output in a manner identical to Bit 0's control over the $\overline{DTR}$ output.

Bit 2. Bit 2 (OUT 1) controls the Output 1 ($\overline{OUT\ 1}$) signal, a user designated output signal, in a manner identical to Bit 0's control over the $\overline{DTR}$ output.

Bit 3. Bit 3 (OUT 2) controls the Output 2 ($\overline{OUT\ 2}$) signal, a user designated output signal, in a manner identical to Bit 0's control over the $\overline{DTR}$ output.

Bit 4. Bit 4 provides a local loopback feature for diagnostic testing of the ACE. When this bit is set to a logic high, the following occurs:

1. The transmitter Serial Output (SOUT) is set high.
2. The receiver Serial Input (SIN) is disconnected.
3. The output of the Transmitter Shift register is looped back into the Receiver Shift register input.
4. The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected.
5. The four modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four modem control inputs.
6. The four modem control output pins are forced to their inactive states (high).

In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit- and receive-data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational but the modem control interrupt's sources are now the lower four bits of the Modem Control register instead of the four modem control inputs. All interrupts are still controlled by the Interrupt Enable register.

Bit 5 through 7. These bits are set to logic 0.

line status register (LSR)†

The Line Status Register provides information to the CPU concerning the status of data transfers. The contents of this register are summarized in Table 3 and are described below.

Bit 0. Bit 0 is the Data Ready (DR) indicator for the receiver. This bit is set to a logic 1 condition whenever a complete incoming character has been received and transferred into the Receiver Buffer register and is reset to logic 0 by reading the Receiver Buffer Register.

Bit 1‡. Bit 1 is the Overrun Error (OE) indicator. When this bit is set to logic 1, it indicates that before the character in the Receiver Buffer register was read, it was overwritten by the next character transferred into the register. The OE indicator is reset every time the CPU reads the contents of the Line Status register.

Bit 2‡. Bit 2 is the Parity Error (PE) indicator. When this bit is set to logic 1, it indicates that the parity of the received data character does not match the parity selected in the Line Control Register (bit 4). The PE bit is reset every time the CPU reads the contents of the Line Status register.

Bit 3‡. Bit 3 is the Framing Error (FE) indicator. When this bit is set to logic 1, it indicates that the received character did not have a valid (logic 1) Stop bit. The FE bit is reset every time the CPU reads the contents of the Line Status register.

† The Line Status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.

‡ Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt.

Bit 4‡. Bit 4 is the Break Interrupt (BI) indicator. When this bit is set to logic 1, it indicates that the received data input was held in the logic 0 state for longer than a full-word transmission time. A "full-word transmission time" is defined as the total time of the Start, Data, Parity, and Stop bits. The BI bit is reset every time the CPU reads the contents of the Line Status register.

Bit 5. Bit 5 is the Transmitter Holding Register Empty (THRE) indicator. This bit is set to a logic 1 condition when the Transmitter Holding Register is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when the THRE bit is a logic 1, then an interrupt is generated. THRE is set to a logic 1 when the contents of the Transmitter Holding Register are transferred to the transmitted Shift Register. This bit is reset to logic 0 concurrent with the loading of the Transmitter Holding Register by the CPU.

Bit 6. Bit 6 is the Transmitter Empty (TEMT) indicator. This bit is set to a logic 1 when the Transmitter Holding register and the Transmitter Shift register are both empty. When either the Transmitter Holding register or the Transmitter Shift register contains a data character, the TEMT bit is reset to logic 0.

Bit 7. This bit is always reset to logic 0.

‡ Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt.

modem status register (MSR)

The Modem Status register is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provides change information; when a control input from the modem changes state the appropriate bit is set to logic 1. All four bits are reset to logic 0 when the CPU reads the Modem Status register. The contents of this register are summarized in Table 3 and are described below.

Bit 0. Bit 0 is the Delta Clear to Send (DCTS) indicator. This bit indicates that the $\overline{CTS}$ input has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the Modem Status Interrrupt is enabled, a Modem Status Interrupt is generated.

Bit 1. Bit 1 is the Delta Data Set Ready (DDSR) indicator. This bit indicates that the $\overline{DSR}$ input has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the Modem Status Interrrupt is enabled, a Modem Status Interrupt is generated.

Bit 2. Bit 2 is the Trailing Edge of Ring Indicator (TERI) detector. This bit indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state. When this bit is a logic 1 and the Modem Status Interrrupt is enabled, a Modem Status Interrupt is generated.

Bit 3. Bit 3 is the Delta Data Carrier Detect (DDCD) indicator. This bit indicates that the $\overline{DCD}$ input to the chip has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the Modem Status Interrrupt is enabled, a Modem Status Interrupt is generated.

Bit 4. Bit 4 is the complement of the Clear to Send ($\overline{CTS}$) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control register bit 1 (RTS).

Bit 5. Bit 5 is the complement of the Data Set Ready ($\overline{DSR}$) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control register bit 0 (DTR).

Bit 6. Bit 6 is the complement of the Ring Indicator ($\overline{RI}$) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control registers bit 2 (OUT 1).

Bit 7. Bit 7 is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control registers bit 3 (OUT 2).

scratch register (SCR)

The Scratch register is an 8-bit register that is intended for the programmer's use as a "scratchpad," in the sense that it will temporarily hold the programmer's data without affecting any other ACE operation.

programmable baud generator

The ACE contains a programmable Baud Generator that takes a clock input in the range between DC and 9 MHz and divides it by a divisor in the range between 1 and $2^{16}-1$. The output frequency of the Baud Generator is sixteen times (16 X) the baud rate. The formula for the divisor is:

divisor # = XTAL1 frequency input ÷ (desired baud rate X 16)

Two 8-bit registers, called Divisor Latches, are used to store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization of the ACE in order to ensure desired operation of the Baud Generator. When either of the Divisor Latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

Tables 5 and 6, which follow, illustrate the use of the Baud Generator with crystal frequencies of 1.8432 MHz and 3.072 MHz, respectively. For baud rates of 38.4 kilobits per second and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency.

Refer to Figure 10 for examples of typical clock circuits.

PRINCIPLES OF OPERATION

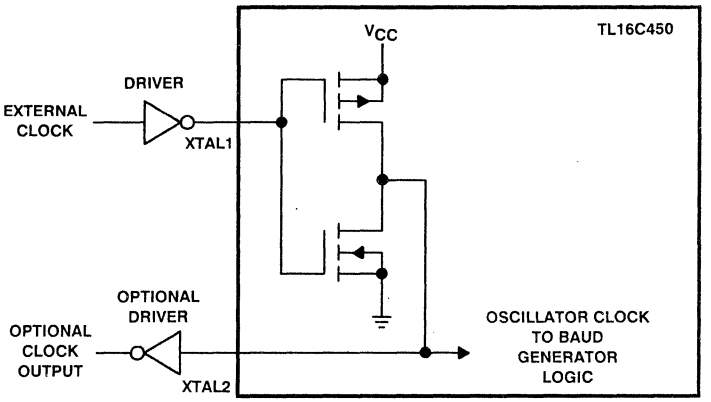
TABLE 5. BAUD RATES USING A 1.8432-MHz CRYSTAL

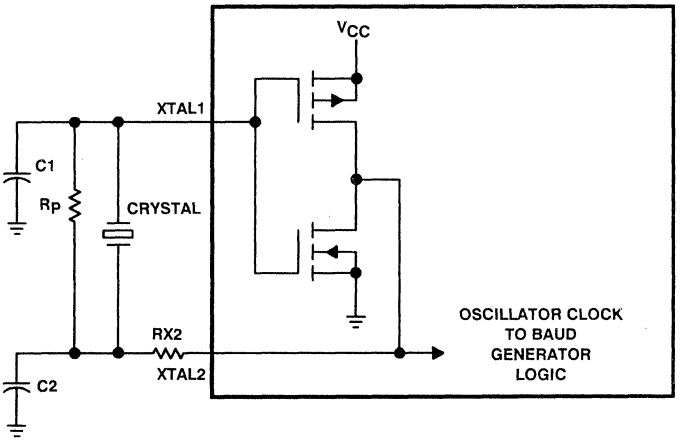
DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	2.86

TABLE 6. BAUD RATES USING A 3.072-MHz CRYSTAL

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	
75	2560	
110	1745	0.026
134.5	1428	0.034
150	1280	
300	640	
600	320	
1200	160	
1800	107	0.312
2000	96	
2400	80	
3600	53	0.628
4800	40	
7200	27	1.23
9600	20	
19200	10	
38400	5	

PRINCIPLES OF OPERATION





TYPICAL CRYSTAL OSCILLATOR NETWORK

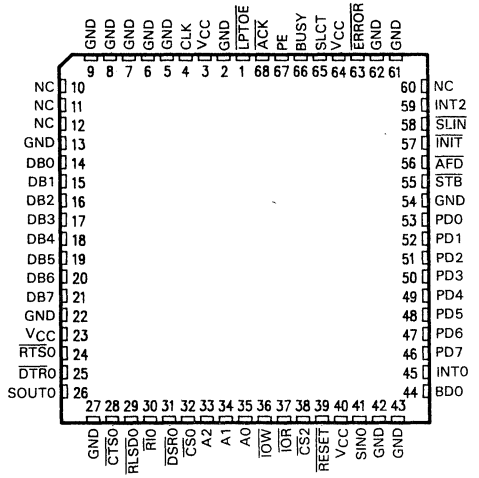
CRYSTAL	R_P	R_{X2}	C_1	C_2
3.1 MHz	1 MΩ	1.5 kΩ	10-30 pF	40-60 pF
1.8 MHz	1 MΩ	1.5 kΩ	10-30 pF	40-60 pF

FIGURE 10. TYPICAL CLOCK CIRCUITS

D3284, MAY 1989—REVISED JANUARY 1990

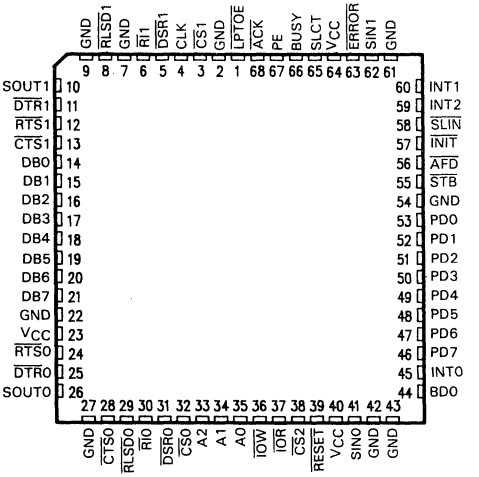
- **Integrates Most Communications Card Functions From the IBM PC/AT or Compatibles with Single-/ or Dual-Channel Serial Ports**
- **TL16C451 Consists of One TL16C450 Plus Centronix Printer Interface**
- **TL16C452 Consists of Two TL16C450s Plus Centronix Printer Interface**
- **Fully Programmable Serial Interface Characteristics:**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even-, Odd-, or No-Parity Bit Generation and Detection**
  - **1-, 1 1/2-, or 2 Stop-Bit Generation**
  - **Programmable Baud Rate (DC to 256 Kilobits per Second)**
- **Fully Double Buffered for Reliable Asynchronous Operation**

TL16C451 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

TL16C452 . . . FN PACKAGE
(TOP VIEW)

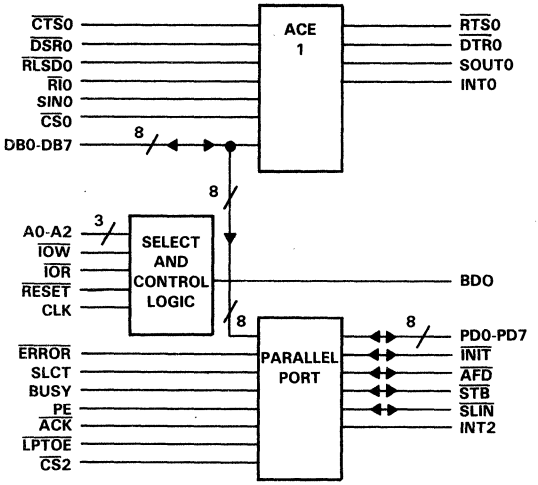


description

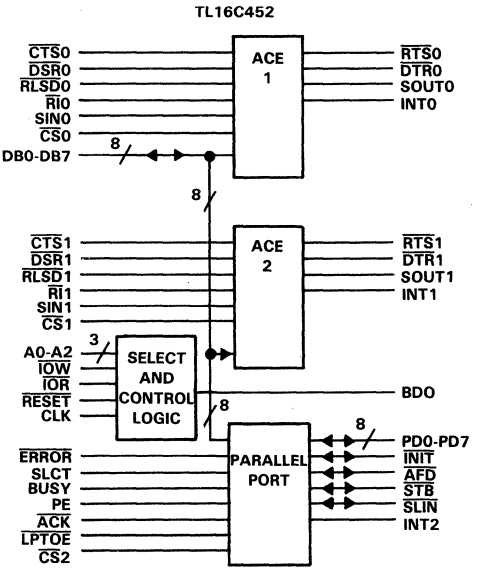
The TL16C451 and TL16C452 provide single- and dual-channel (respectively) serial interfaces along with a single Centronix parallel-port interface. The serial interfaces provide a serial-to-parallel conversion for data received from a peripheral device or modem and a parallel-to-serial conversion for data transmitted by a computer CPU. The parallel interface provides a bidirectional parallel data port that fully conforms to the requirements for a Centronix-type printer. A computer CPU can read the status of the asynchronous-communications-element (ACE) interfaces at any point in the operation. The status includes the state of the modem signals ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) and any changes to these signals that have occurred since the last time they were read, the state of the transmitter and receiver including errors detected on received data, and printer status. The TL16C451 and TL16C452 provide control for modem signals ($\overline{RTS}$ and $\overline{DTR}$), interrupt enables, baud-rate programming, and parallel-port control signals.

functional block diagrams

TL16C451



TL16C452



PIN NAME†	PIN NO.	I/O	DESCRIPTION
A0 A1 A2	35 34 33	I	Register Select. Three inputs used during read and write operations to select the register to read from or write to. Refer to Table 1 for register addresses, also refer to the chip select signals ($\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$).
$\overline{ACK}$	68	I	Line Printer Acknowledge. This input goes low to indicate a successful data transfer has taken place. It generates a printer-port interrupt during its positive transition.
$\overline{AFD}$	56	I/O	Line Printer Autofeed. This open-drain line provides the line printer with a low signal when continuous-form paper is to be autofed to the printer. An internal pullup is provided.
BDO	44	O	Bus Buffer Output. This output is active (high) when the CPU is reading data. When active, this output can be used to disable an external transceiver.
BUSY	66	I	Line Printer Busy. This is an input line from the line printer that goes high when the line printer is not ready to accept data.
CLK	4	I/O	External Clock. Connects the ACE to the main timing reference.
$\overline{CS0}$ $\overline{CS1}$ [V_{CC}] $\overline{CS2}$	32 3 38	I	Chip Selects. Each chip select enables read and write operations to its respective channel. $\overline{CS0}$ and $\overline{CS1}$ select serial channels 0 and 1, respectively, and $\overline{CS2}$ selects the parallel port.
$\overline{CTS0}$ $\overline{CTS1}$ [GND]	28 13	I	Clear To Send. $\overline{CTS}$ is an active-low modem status signal whose state can be checked by reading bit 4 (CTS) of the Modem Status Register. Bit 0 (DCTS) of the Modem Status Register indicates that this signal has changed state since the last read from the Modem Status Register. If the Modem Status Interrupt is enabled when $\overline{CTS}$ changes state, an interrupt is generated.
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	14 15 16 17 18 19 20 21	I/O	Data Bus. Eight 3-state data lines provide a bidirectional path for data, control, and status information between the TL16C451/TL16C452 and the CPU. DB0 is the least significant bit (LSB).
$\overline{DSR0}$ $\overline{DSR1}$ [GND]	31 5	I	Data Set Ready. $\overline{DSR}$ is an active-low modem status signal whose state can be checked by reading bit 5 (DSR) of the Modem Status Register. Bit 1 (DDSR) of the Modem Status Register indicates that this signal has changed state since the last read from the Modem Status Register. If the modem status interrupt is enabled when the $\overline{DSR}$ changes state, an interrupt is generated.
$\overline{DTR0}$ $\overline{DTR1}$ [NC]	25 11	O	Data Terminal Ready. When active (low), $\overline{DTR}$ informs a modem or data set that the ACE is ready to establish communication. $\overline{DTR}$ is placed in the active state by setting the DTR bit of the Modem Control Register to a high level. $\overline{DTR}$ is placed in the inactive state either as a result of a reset or during loop mode operation or resetting bit 0 (DTR) of the Modem Control Register.
$\overline{ERROR}$	63	I	Line Printer Error. This is an input line from the line printer. The line printer reports an error by holding this line low during the error conditon.
$\overline{INIT}$	57	I/O	Line Printer Initialize. This open-drain line provides the line printer with a signal that allows the line printer initialization routine to be started. An internal pullup is provided.
INT0 INT1 [NC]	45 60	O	Interrupt. INTn is an active-high 3-state output that is enabled by bit 3 of the MCR. When active , INTn informs the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are; a receiver error, received data is available, the transmitter holding register is empty, and an enabled modem status interrupt. The INTn output is reset (low) either when the interrupt is serviced or as a result of a reset.
INT2	59	O	Printer Port Interrupt. This signal is an active-high 3-state output generated by the positive transition of $\overline{ACK}$. It is enabled by bit 4 of the Write Control Register.
$\overline{IOR}$	37	I	Data Read Strobe. When $\overline{IOR}$ input is active (low) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register.
$\overline{IOW}$	36	I	Data Write Strobe. When $\overline{IOW}$ input is active (low) while the ACE is selected, the CPU is allowed to write control words or data into a selected ACE register.

† Names shown in brackets are for the TL16C451.

PIN NAME†	PIN NO.	I/O	DESCRIPTION
$\overline{\text{LPTOE}}$	1	I	Parallel Data Output Enable. When low, this signal enables the Write Data Register to the PD0-PD7 lines. A high puts the PD0-PD7 lines in the high-impedance state allowing them to be used as inputs. $\overline{\text{LPTOE}}$ is usually tied low for line printer operation.
PD0-PD7	53-46	I/O	Parallel Data Bits (0-7). These eight lines provide a byte-wide input or output port to the system. The eight lines are held in a high-impedance state when $\overline{\text{LPTOE}}$ is high.
PE	67	I	Line Printer Paper Empty. This is an input line from the line printer that goes high when the printer runs out of paper.
$\overline{\text{RESET}}$	39	I	Reset. When active (low), $\overline{\text{RESET}}$ clears most ACE registers and sets the state of various output signals. Refer to Table 2, ACE Reset Functions.
$\overline{\text{RI}}$0 $\overline{\text{RI}}$1 [GND]	30 6	I	Ring Indicator. $\overline{\text{RI}}$ is an active-low modem status signal whose state can be checked by reading bit 6 (RI) of the Modem Status Register. Bit 2 (TERI) of the Modem Status Register indicates that the $\overline{\text{RI}}$ input has transitioned from a low to a high state since the last read from the Modem Status Register. If the Modem Status Interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{\text{RLSD}}$0 $\overline{\text{RLSD}}$1 [GND]	29 8	I	Receive Line Signal Detect. $\overline{\text{RLSD}}$0 is an active-low modem status signal whose state can be checked by reading bit 7 of the Modem Status Register. Bit 3 (DRLSD) of the Modem Status Register indicates that this signal has changed state since the last read from the Modem Status Register. If the Modem Status Interrupt is enabled when $\overline{\text{RLSD}}$0 changes state, an interrupt is generated. This bit is low when a data carrier is detected.
$\overline{\text{RTS}}$0 $\overline{\text{RTS}}$1 [NC]	24 12	O	Request To Send. When active (low), this signal informs the modem or data set that the ACE is ready to transmit data. $\overline{\text{RTS}}$ is set to its active state by setting the RTS Modem Control Register bit and is set to its inactive (high) state either as a result of a reset or during loop mode operations or by resetting bit 1 (RTS) of the modem control register.
SIN0 SIN1 [GND]	41 62	I	Serial Input. Serial data input from a connected communications device.
SLCT	65	I	Line Printer Selected. This is an input line from the line printer that goes high when the line printer has been selected.
$\overline{\text{SLIN}}$	58	I/O	Line Printer Select. This open-drain line selects the printer when it is active (low). An internal pullup is provided.
SOUT0 SOUT1 [NC]	26 10	O	Serial Output. Composite serial data output to a connected communication device. SOUT is set to the Marking (logic 1) state as a result of reset.
$\overline{\text{STB}}$	55	I/O	Line Printer Strobe. This open-drain line provides communication synchronization between the TL16C451/TL16C452 and the line printer. When it is active (low), it provides the line printer with a signal to latch the data currently on the parallel port. An internal pullup is provided.
V_{CC}	23,40, 64		5-V Supply Voltage
GND	2,7,9, 22,27, 42,43, 54,61		Supply Common

† Names shown in brackets are for the TL16C451.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range at any input, V_I . . . . . −0.5 V to 7 V
Output voltage range, V_O . . . . . −0.5 V to 7 V
Continuous total power dissipation . . . . . 1100 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −0.4 mA on DB0-DB7	2.4			V
		I_{OH} = −2 mA to 4 mA on PD0-PD7				
		I_{OH} = −0.2 mA on $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$				
		I_{OH} = −0.2 mA on all other outputs				
V_{OL}	Low-level output voltage	I_{OL} = 4 mA on DB0-DB7			0.4	V
		I_{OL} = 12 mA on PD0-PD7				
		I_{OL} = 10 mA on $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ (see Note 2)				
		I_{OL} = 2 mA on all other outputs				
I_{lkg}	Input leakage current	V_{CC} = 5.25 V, V_{SS} = 0, V_I = 0 to 5.25 V, All other pins floating			±10	µA
I_{OZ}	High-impedance output current	V_{CC} = 5.25 V, V_{SS} = 0, V_O = 0 to 5.25 V, Chip selected and write mode, or chip deselected			±20	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, T_A = 25°C, SIN, $\overline{DSR}$, $\overline{RLSD}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V, All other inputs at 0.8 V, XTAL1 at 4 MHz, No load on outputs. Baud rate = 50 kilobits per second			10	mA
C_{XTAL1}	Clock input capacitance	V_{CC} = 0, V_{SS} = 0, f = 1 MHz, T_A = 25°C, All other pins grounded		15	20	pF
C_{XTAL2}	Clock output capacitance			20	30	pF
C_i	Input capacitance			6	10	pF
C_o	Output capacitance			10	20	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ are open-collector output pins that each have an internal pullup to V_{CC}. This will generate a maximum of 2 mA of internal I_{OL} per pin. In addition to this internal current, each pin will sink at least 10 mA while maintaining the V_{OL} specification of 0.4 V Max.

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	FIGURE	MIN	MAX	UNIT
t_{cR}	Cycle time, read ($t_{w7} + t_{d8} + t_{d9}$)		175		ns
t_{cW}	Cycle time, write ($t_{w6} + t_{d5} + t_{d6}$)		175		ns
t_{w1}	Pulse duration, clock high	1	50		ns
t_{w2}	Pulse duration, clock low	1	50		ns
t_{w5}	Pulse duration, write strobe	2	80		ns
t_{w6}	Pulse duration, read strobe	3	80		ns
t_{wRST}	Pulse duration, reset		1000		ns
t_{su1}	Setup time, address	2,3	15		ns
t_{su2}	Setup time, chip select	2,3	15		ns
t_{su3}	Setup time, data	2	15		ns
t_{h1}	Hold time, address	2,3	20		ns
t_{h2}	Hold time, chip select	2,3	20		ns
t_{h3}	Hold time, data	2	15		ns
t_{d3}	Delay time, write cycle	2	80		ns
t_{d4}	Delay time, read cycle	3	80		ns

system switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d5}	Delay time, read to data	3	C_L = 100 pF		60	ns
t_{d6}	Delay time, read to floating data	3	C_L = 100 pF	0	60	ns
$t_{dis(R)}$	Read to driver disable	3	C_L = 100 pF		60	ns

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d7}	Delay time, RCLK to sample	4			100	ns
t_{d8}	Delay time, stop to set interrupt	4		1	1	RCLK cycles
t_{d9}	Delay time, read RBR/LSR to reset interrupt	4	C_L = 100 pF		140	ns

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d10}	Delay time, initial write THR to transmit start	5		8	24	baudout cycles
t_{d11}	Delay time, stop to interrupt	5		8	8	baudout cycles
t_{d12}	Delay time, write THR to reset interrupt	5	C_L = 100 pF		140	ns
t_{d13}	Delay time, initial write to interrupt (THRE)	5		16	32	baudout cycles
t_{d14}	Delay time, read IIR to reset interrupt (THRE)	5	C_L = 100 pF		140	ns

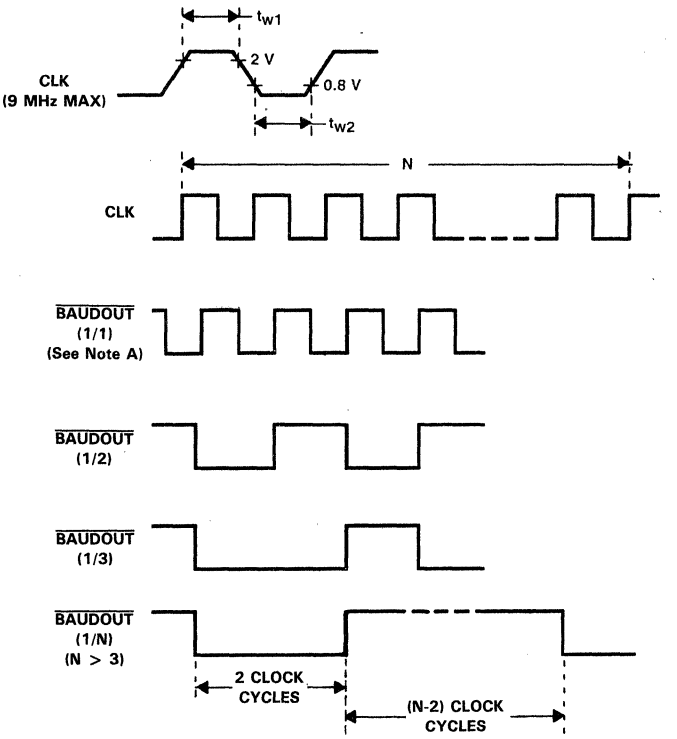
modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d15}	Delay time, write MCR to output	6	C_L = 100 pF		100	ns
t_{d16}	Delay time, modem input to set interrupt	6	C_L = 100 pF		170	ns
t_{d17}	Delay time, read MSR to reset interrupt	6	C_L = 100 pF		140	ns

parallel port switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d18}	Delay time, write parallel port control to output	7	C_L = 100 pF		60	ns
t_{d19}	Delay time, write parallel port data to output	7	C_L = 100 pF		60	ns
t_{d20}	Delay time, output enable to data	7	C_L = 100 pF		60	ns
t_{d21}	Delay time, $\overline{ACK}$ to INT2	7	C_L = 100 pF		100	ns

PARAMETER MEASUREMENT INFORMATION



NOTE A: $\overline{\text{BAUDOUT}}$ is an internally generated signal used in the receiver and transmitter circuits to synchronize data.

FIGURE 1. BAUD GENERATOR TIMING

PARAMETER MEASUREMENT INFORMATION

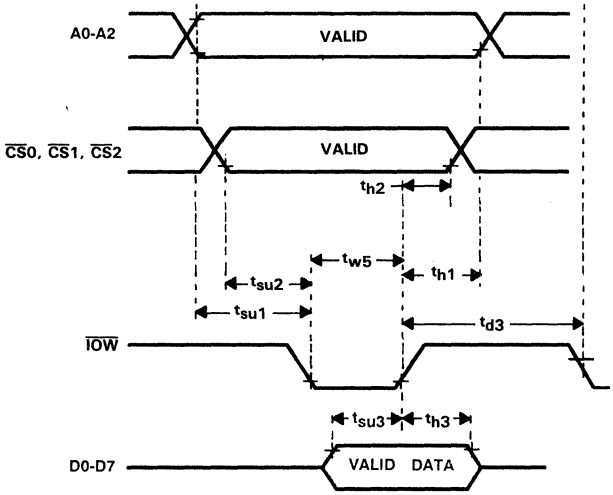


FIGURE 2. WRITE CYCLE TIMING

PARAMETER MEASUREMENT INFORMATION

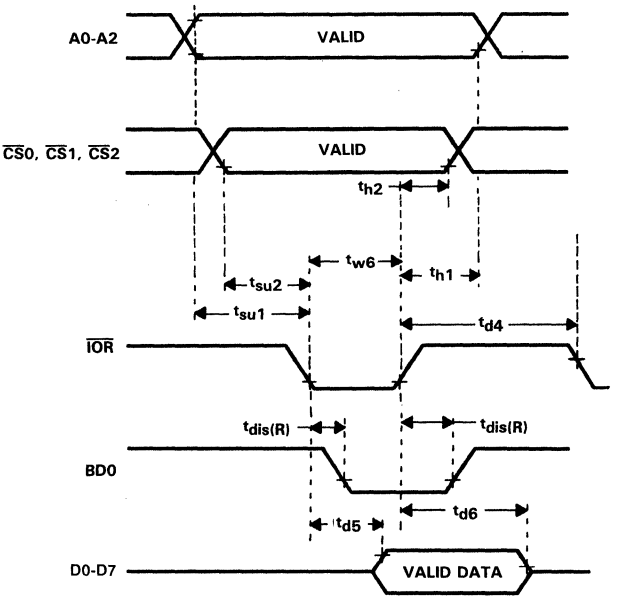


FIGURE 3. READ CYCLE TIMING

PARAMETER MEASUREMENT INFORMATION

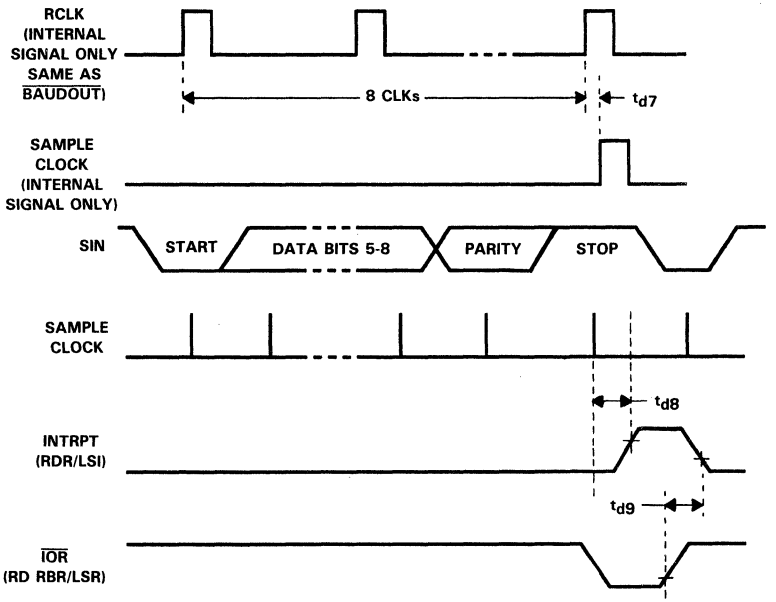


FIGURE 4. RECEIVER TIMING

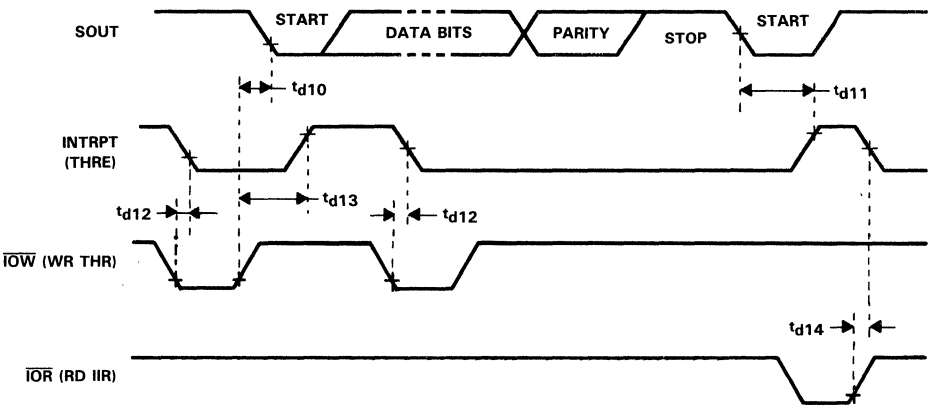


FIGURE 5. TRANSMITTER TIMING

PARAMETER MEASUREMENT INFORMATION

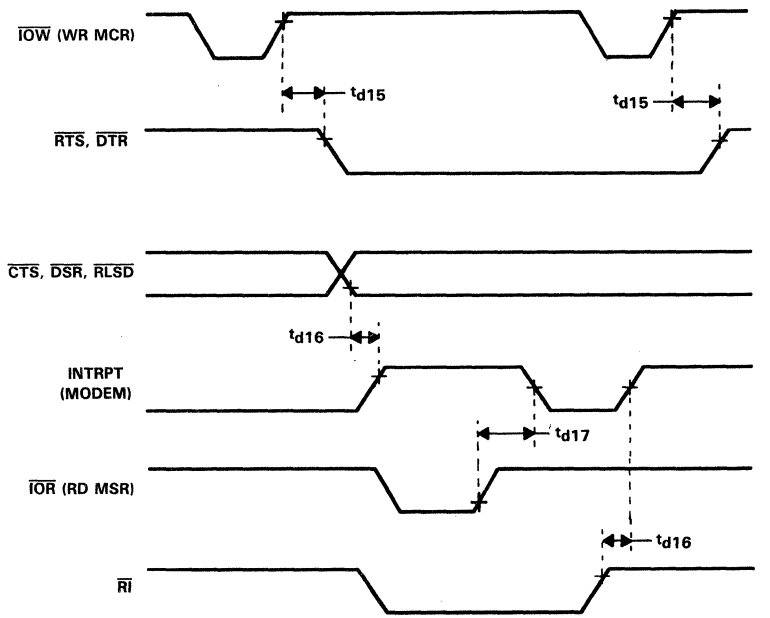


FIGURE 6. MODEM CONTROL TIMING

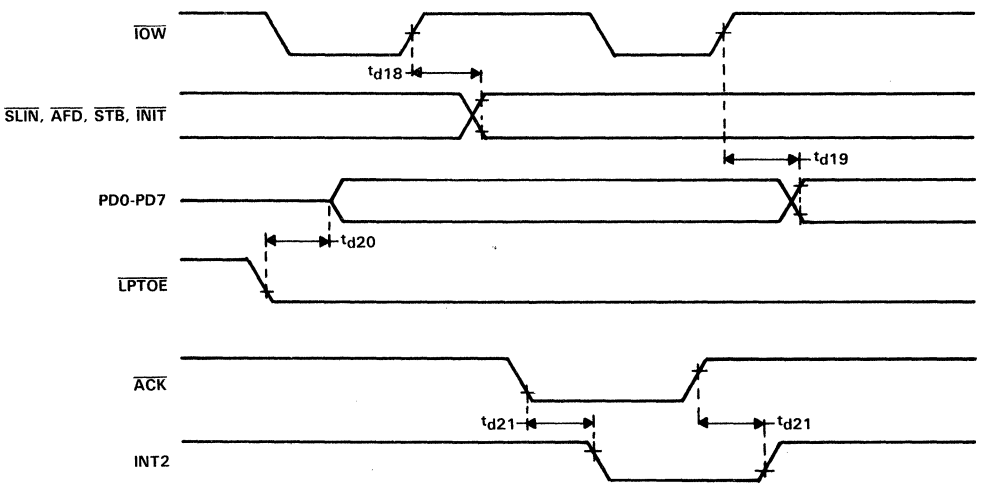


FIGURE 7. PARALLEL PORT TIMING

APPLICATION INFORMATION

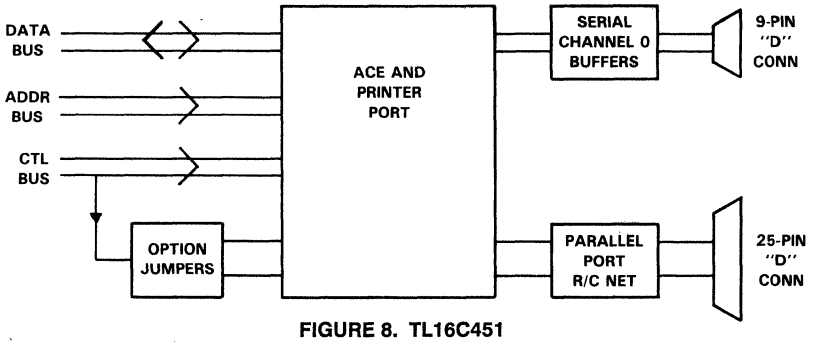


FIGURE 8. TL16C451

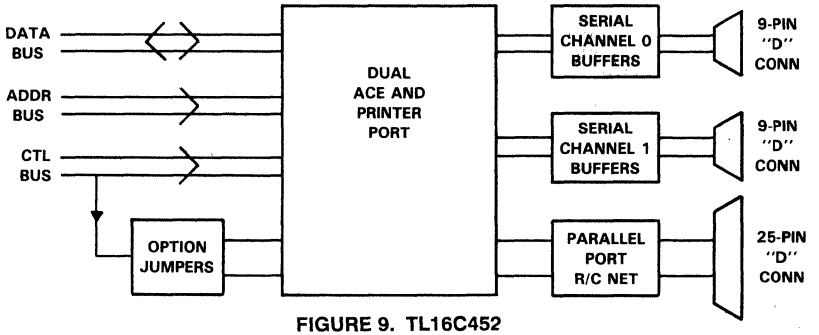


FIGURE 9. TL16C452

PRINCIPLES OF OPERATION

TABLE 1. REGISTER SELECTION

DLAB†	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding register (write)
0	L	L	H	Interrupt enable
X	L	H	L	Interrupt identification (read only)
X	L	H	H	Line control
X	H	L	L	Modem control
X	H	L	H	Line status
X	H	H	L	Modem status
X	H	H	H	Scratch
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor Latch (MSB)

† The Divisor Latch Access Bit (DLAB) is the most significant bit of the Line Control Register. The DLAB signal is controlled by writing to this bit location (see Table 3).

TABLE 2. ACE RESET FUNCTIONS

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	$\overline{\text{Reset}}$	All bits low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	$\overline{\text{Reset}}$	Bit 0 is high, bits 1 and 2 are low, and bits 3-7 are permanently low
Line Control Register	$\overline{\text{Reset}}$	All bits low
Modem Control Register	$\overline{\text{Reset}}$	All bits low
Line Status Register	$\overline{\text{Reset}}$	Bits 5 and 6 are high, all other bits are low
Modem Status Register	$\overline{\text{Reset}}$	Bits 0-3 are low, bits 4-7 are input signals
SOUT	$\overline{\text{Reset}}$	High
INTRPT (Receiver Error Flag)	Read LSR/$\overline{\text{Reset}}$	Low
INTRPT (Received Data Available)	Read RBR/$\overline{\text{Reset}}$	Low
INTRPT (Transmitter Holding Register Empty)	Read IIR/Write THR/$\overline{\text{Reset}}$	Low
INTRPT (Modem Status Changes)	Read MSR/$\overline{\text{Reset}}$	Low
$\overline{\text{OUT 2}}$ (interrupt enable)	$\overline{\text{Reset}}$	High
$\overline{\text{RTS}}$	$\overline{\text{Reset}}$	High
$\overline{\text{DTR}}$	$\overline{\text{Reset}}$	High
$\overline{\text{OUT 1}}$	$\overline{\text{Reset}}$	High
Scratch Register	$\overline{\text{Reset}}$	No effect
Divisor Latch (LSB and MSB) Registers	$\overline{\text{Reset}}$	No effect
Receiver Buffer Registers	$\overline{\text{Reset}}$	No effect
Transmitter Holding Registers	$\overline{\text{Reset}}$	No effect

PRINCIPLES OF OPERATION

accessible registers

The system programmer, via the CPU, has access to and control over any of the ACE registers that are summarized in Table 3. These registers are used to control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

TABLE 3. SUMMARY OF ACCESSIBLE REGISTERS

Bit No.	REGISTER ADDRESS										
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	Line Control Register	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LSB)	Latch (MSB)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2 (Interrupt Enable)	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Receive Line Signal Detect (RLSD)	Bit 7	Bit 7	Bit 15

* Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

PRINCIPLES OF OPERATION

receiver buffer register (RBR)

The ACE's receiver section consists of a Receiver Shift Register and a Receiver Buffer Register. Timing is supplied by the 16 X Receiver Clock (RCLK). Receiver section control is a function of the ACE's Line Control Register.

The ACE's Receiver Shift Register receives serial data from the Serial Input (SIN) pin. The Receiver Shift Register then converts the data to a parallel form and loads it into the Receiver Buffer Register. When a character is placed in the Receiver Buffer Register and the Received Data Available interrupt is enabled, an interrupt is generated. This interrupt is cleared when the data is read out of the Receiver Buffer Register.

transmitter holding register (THR)

The ACE's transmitter section consists of a Transmitter Holding Register and a Transmitter Shift Register. Timing is supplied by the Baud Out ($\overline{\text{BAUDOUT}}$) clock signal. Transmitter section control is a function of the ACE's Line Control Register.

The ACE Transmitter Holding Register receives data off the Internal Data Bus and, when the shift register is idle, moves it into the Transmitter Shift Register. The Transmitter Shift Register serializes the data and outputs it at the Serial Output (SOUT). If the Transmitter Holding Register is empty and the Transmitter Holding Register Empty (THRE) interrupt is enabled, an interrupt is generated. This interrupt is cleared when a character is loaded into the register.

interrupt enable register (IER)

The Interrupt Enable Register enables each of the four types of interrupts (refer to Table 4) and the INTRPT output signal in response to an interrupt generation. The Interrupt Enable Register can also be used to disable the interrupt system by setting bits 0 through 3 to logic 0. The contents of this register are summarized in Table 3 and are described below.

Bit 0. This bit, when set to logic 1, enables the Received Data Available interrupt.

Bit 1. This bit, when set to logic 1, enables the Transmitter Holding Register Empty interrupt.

Bit 2. This bit, when set to logic 1, enables the Receiver Line Status interrupt.

Bit 3. This bit, when set to logic 1, enables the Modem Status interrupt.

Bits 4 thru 7. Bits 4 through 7 in the Interrupt Enable Register are not used and are always set to logic 0.

PRINCIPLES OF OPERATION

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most microprocessors.

The ACE provides four prioritized levels of interrupts:

Priority 1 – Receiver line status (highest priority)
Priority 2 – Receiver data ready
Priority 3 – Transmitter holding register empty
Priority 4 – Modem status (lowest priority)

When an interrupt is generated, the Interrupt Identification Register indicates that an interrupt is pending and the type of that interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 4.

Bit 0. This bit can be used either in a hardwire-prioritized, or polled interrupt system. If this bit is a logic 0, an interrupt is pending. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2. These two bits are used to identify the highest priority interrupt pending, as indicated in Table 4.

Bits 3 thru 7. Bits 3 through 7 in the Interrupt Identification Register are not used and are always set at logic 0.

TABLE 4. INTERRUPT CONTROL FUNCTIONS

INTERRUPT IDENTIFICATION REGISTER			PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 2	BIT 1	BIT 0				
0	0	1	None	None	None	–
1	1	0	1	Receiver line status	Overrun error, parity error, framing error or break interrupt	Reading the Line Status register
1	0	0	2	Received data available	Receiver data available	Reading the Receiver buffer Buffer register
0	1	0	3	Transmitter Holding register empty	Transmitter Holding register empty	Reading the Interrupt Identification register (if source of interrupt) or writing into the Transmitter Holding register
0	0	0	4	Modem status	Clear to Send, Data Set Ready, Ring Indicator, or Receive Line Signal Detect	Reading the Modem Status register

PRINCIPLES OF OPERATION

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the Line Control register. In addition, the programmer is able to retrieve, inspect, and modify the contents of the Line Control register; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and are described below.

Bits 0 and 1. These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2. This bit specifies either one, one and one-half, or two Stop bits in each transmitted character. If bit 2 is a logic 0, one Stop bit is generated in the data. If bit 2 is a logic 1, the number of Stop bits generated is dependent on the word length selected with bits 0 and 1. The number of Stop bits generated, in relation to word length and bit 2, is as follows:

Bit 2	Word Length Selected by Bits 1 and 2	Number of Stop Bits Generated
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

Bit 3. This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, if bit 3 is a logic 1, parity is checked. When bit 3 is a logic 0, no parity is generated or checked.

Bit 4. Bit 4 is the Even Parity Select bit. When parity is enabled by bit 3: a logic 1 in bit 4 produces Even Parity (an even number of logic is in the data and parity bits) and a logic 0 in bit 4 produces Odd Parity (an odd number of logic 1s).

Bit 5. This is the Stick parity bit. When bits 3, 4, and 5 are logic 1s, the Parity bit is transmitted and checked as a logic 0. When bits 3 and 5 are logic 1s and bit 4 is a logic 0, the Parity bit is transmitted and checked as a logic 1.

Bit 6. This bit is the Break Control bit. Bit 6 is set to a logic 1 to force a break condition, i.e, a condition where the Serial Output (SOUT) pin is forced to the spacing (logic 0) state. When bit 6 is set to a logic 0, the break condition is disabled. The break condition has no effect on the transmitter logic, it only effects the serial output.

Bit 7. This bit is the Divisor Latch Access bit (DLAB). Bit 7 must be set to a logic 1 to access the Divisor Latches of the Baud Generator during a read or write. Bit 7 must be set to a logic 0 during a read or write to access the Receiver Buffer, the Transmitter Holding register, or the Interrupt Enable register.

modem control register (MCR)

The Modem Control register is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described below.

Bit 0. Bit 0 (DTR) controls the Data Terminal Ready ($\overline{DTR}$) output. Setting this bit to a logic 1 forces the $\overline{DTR}$ output to its active state (low). When bit 0 is set to a logic 0, $\overline{DTR}$ goes high.

Bit 1. Bit 1 (RTS) controls the Request to Send ($\overline{RTS}$) output in a manner identical to Bit 0's control over the $\overline{DTR}$ output.

Bit 2. Bit 2 (OUT 1) is a reserved location used only in the loopback mode.

Bit 3. Bit 3 (OUT 2) controls the output enable for the interrupt signal. When set to a logic 1, the interrupt is enabled. When bit 3 is set to a logic 0, the interrupt is disabled.

Bit 4. Bit 4 provides a local loopback feature for diagnostic testing of the ACE. When this bit is set to a logic high, the following occurs:

1. The transmitter Serial Output (SOUT) is set high.
2. The receiver Serial Input (SIN) is disconnected.
3. The output of the Transmitter Shift register is looped back into the Receiver Shift register input.
4. The four modem status inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected.
5. The modem control register bits (DTR, RTS, OUT1, and OUT2) are connected to the modem status register bits (DSR, CTS, RI, and RLSD), respectively.
6. The four modem control output pins are forced to their inactive states (high).

In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit- and receive-data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational but the modem control interrupt's sources are now the lower four bits of the Modem Control register instead of the four modem control inputs. All interrupts are still controlled by the Interrupt Enable register.

Bit 5 through 7. These bits are set to logic 0.

line status register (LSR)†

The Line Status Register provides information to the CPU concerning the status of data transfers. The contents of this register are summarized in Table 3 and are described below.

Bit 0. Bit 0 is the Data Ready (DR) indicator for the receiver. This bit is set to a logic 1 condition whenever a complete incoming character has been received and transferred into the Receiver Buffer register and is reset to logic 0 by reading the Receiver Buffer Register.

Bit 1‡. Bit 1 is the Overrun Error (OE) indicator. When this bit is set to logic 1, it indicates that before the character in the Receiver Buffer register was read, it was overwritten by the next character transferred into the register. The OE indicator is reset every time the CPU reads the contents of the Line Status register.

Bit 2‡. Bit 2 is the Parity Error (PE) indicator. When this bit is set to logic 1, it indicates that the parity of the received data character does not match the parity selected in the Line Control Register (bit 4). The PE bit is reset every time the CPU reads the contents of the Line Status register.

Bit 3‡. Bit 3 is the Framing Error (FE) indicator. When this bit is set to logic 1, it indicates that the received character did not have a valid (logic 1) Stop bit. The FE bit is reset every time the CPU reads the contents of the Line Status register.

† The Line Status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.
‡ Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt.

Bit 4‡. Bit 4 is the Break Interrupt (BI) indicator. When this bit is set to logic 1, it indicates that the received data input was held in the logic 0 state for longer than a full-word transmission time. A "full-word transmission time" is defined as the total time of the Start, Data, Parity, and Stop bits. The BI bit is reset every time the CPU reads the contents of the Line Status register.

Bit 5. Bit 5 is the Transmitter Holding Register Empty (THRE) indicator. This bit is set to a logic 1 condition when the Transmitter Holding Register is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when the THRE bit is a logic 1, then an interrupt is generated. THRE is set to a logic 1 when the contents of the Transmitter Holding Register are transferred to the transmitted Shift Register. This bit is reset to logic 0 concurrent with the loading of the Transmitter Holding Register by the CPU.

Bit 6. Bit 6 is the Transmitter Empty (TEMT) indicator. This bit is set to a logic 1 when the Transmitter Holding register and the Transmitter Shift register are both empty. When either the Transmitter Holding register or the Transmitter Shift register contains a data character, the TEMT bit is reset to logic 0.

Bit 7. This bit is always reset to logic 0.

‡ Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt.

modem status register (MSR)

The Modem Status register is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provides change information; when a control input from the modem changes state the appropriate bit is set to logic 1. All four bits are reset to logic 0 when the CPU reads the Modem Status register. The contents of this register are summarized in Table 3 and are described below.

Bit 0. Bit 0 is the Delta Clear to Send (DCTS) indicator. This bit indicates that the $\overline{CTS}$ input has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the Modem Status Interrrupt is enabled, a Modem Status Interrupt is generated.

Bit 1. Bit 1 is the Delta Data Set Ready (DDSR) indicator. This bit indicates that the $\overline{DSR}$ input has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the Modem Status Interrrupt is enabled, a Modem Status Interrupt is generated.

Bit 2. Bit 2 is the Trailing Edge of Ring Indicator (TERI) detector. This bit indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state. When this bit is a logic 1 and the Modem Status Interrrupt is enabled, a Modem Status Interrupt is generated.

Bit 3. Bit 3 is the Delta Receive Line Signal Detect (DRLSD) indicator. This bit indicates that the $\overline{RLSD}$ input to the chip has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the Modem Status Interrrupt is enabled, a Modem Status Interrupt is generated.

Bit 4. Bit 4 is the complement of the Clear to Send ($\overline{CTS}$) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control register bit 1 (RTS).

Bit 5. Bit 5 is the complement of the Data Set Ready ($\overline{DSR}$) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control register bit 0 (DTR).

Bit 6. Bit 6 is the complement of the Ring Indicator ($\overline{RI}$) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control registers bit 2 (OUT 1).

Bit 7. Bit 7 is the complement of the Receive Line Signal Detect ($\overline{RLSD}$) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control registers bit 3 (OUT 2).

scratch register (SCR)

The Scratch register is an 8-bit register that is intended for the programmer's use as a "scratchpad," in the sense that it will temporarily hold the programmer's data without affecting any other ACE operation.

programmable baud generator

The ACE contains a programmable Baud Generator that takes a clock input in the range between dc and 9 MHz and divides it by a divisor in the range between 1 and $2^{16}-1$. The output frequency of the Baud Generator is sixteen times (16 X) the baud rate. The formula for the divisor is:

$$\text{divisor } \# = \text{CLK frequency input} \div (\text{desired baud rate X } 16)$$

Two 8-bit registers, called Divisor Latches, are used to store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization of the ACE in order to ensure desired operation of the Baud Generator. When either of the Divisor Latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load. For baud rates of 38.4 kilobits per second and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency.

interrupt control logic

The interrupt control logic is shown in Figure 9.

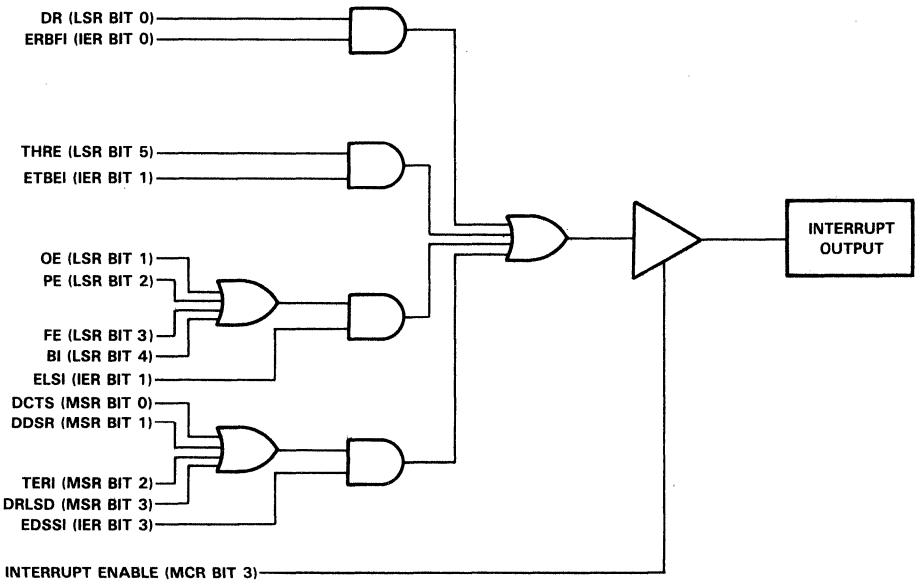


FIGURE 9. INTERRUPT CONTROL LOGIC

parallel port registers

The parallel port registers interface either device to a Centronix-style printer. When Chip Select 2 ($\overline{CS2}$) is low, the parallel port is selected. Tables 5 and 6 show the registers associated with this parallel port. The read or write function of the register is controlled by the state or the read ($\overline{IOR}$) and write ($\overline{IOW}$) pin as shown. The Read Data Register allows the microprocessor to read the information on the parallel bus.

The Read Status Register allows the microprocessor to read the status of the printer in the five most significant bits. The status bits are Printer Busy ($\overline{BUSY}$), Acknowledge ($\overline{ACK}$) which is a handshake function, Paper Empty (PE), Printer Selected (SLCT), and Error ($\overline{ERROR}$). The Read Control Register allows the state of the control lines to be read. The Write Control Register sets the state of the control lines, which are Interrupt Enable (IRQ ENB), Select In (SLIN), Initialize the Printer ($\overline{INIT}$), Autofeed the Paper (AFD), and Strobe (STB), which informs the printer of the presence of a valid byte on the parallel bus. These signals are set to 0 when a reset occurs. The Write Data Register allows the microprocessor to write a byte to the parallel bus. The parallel port is completely compatible with the parallel port implementation used in the IBM Serial/Parallel Adaptor.

TABLE 5. PARALLEL PORT REGISTERS

REGISTER	REGISTER BITS							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Read Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	$\overline{BUSY}$	$\overline{ACK}$	PE	SLCT	$\overline{ERROR}$	1	1	1
Read Control	1	1	1	IRQ ENB	SLIN	$\overline{INIT}$	AFD	STB
Write Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	1	1	1	IRQ ENB	SLIN	$\overline{INIT}$	AFD	STB

TABLE 6. PARALLEL PORT REGISTER SELECT

CONTROL PINS					REGISTER SELECTED
$\overline{IOR}$	$\overline{IOW}$	$\overline{CS2}$	A1	A0	
L	H	L	L	L	Read Data
L	H	L	L	H	Read Status
L	H	L	H	L	Read Control
L	H	L	H	H	Invalid
H	L	L	L	L	Write Data
H	L	L	L	H	Invalid
H	L	L	H	L	Write Control
H	L	L	H	H	Invalid

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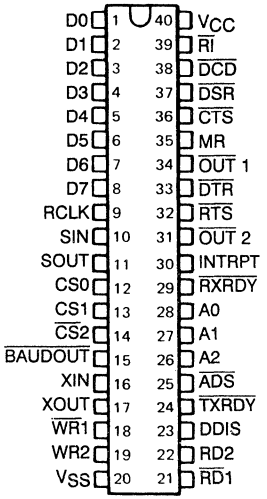
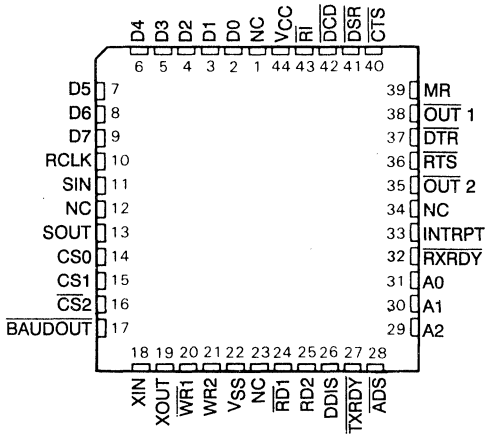
- Capable of Running with All Existing TL16C450 Software
- After Reset, All Registers Are Identical to the TL16C450 Register Set
- In the FIFO Mode, Transmitter and Receiver Are Each Buffered with 16-Byte FIFOs to Reduce the Number of Interrupts to the CPU
- In the TL16C450 Mode, Holding and Shift Registers Eliminate the Need for Precise Synchronization Between the CPU and Serial Data
- Programmable Baud Rate Generator Allows Division of Any Input Reference Clock by 1 to ($2^{16}-1$) and Generates an Internal 16 X Clock
- Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or from the Serial Data Stream
- Independent Receiver Clock Input
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Fully Programmable Serial Interface Characteristics:
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even-, Odd-, or No-Parity Bit Generation and Detection
  - 1-, 1 1/2-, or 2-Stop Bit Generation
  - Baud Generation (DC to 256 Kilobits per Second)
- False-Start Bit Detection
- Complete Status Reporting Capabilities
- 3-State TTL Drive Capabilities for Bidirectional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities:
  - Loopback Controls for Communications Link Fault Isolation
  - Break, Parity, Overrun, Framing Error Simulation
- Full Prioritized Interrupt System Controls
- Modem Control Functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, and $\overline{DCD}$)
- Faster Plug-In Replacement for National Semiconductor NS16550A

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL16C550A is a functional upgrade of the TL16C450 Asynchronous Communications Element (ACE). Functionally identical to the TL16C450 on powerup (Character Mode†), the TL16C550A can be placed in an alternate mode (FIFO) to relieve the CPU of excessive software overhead.

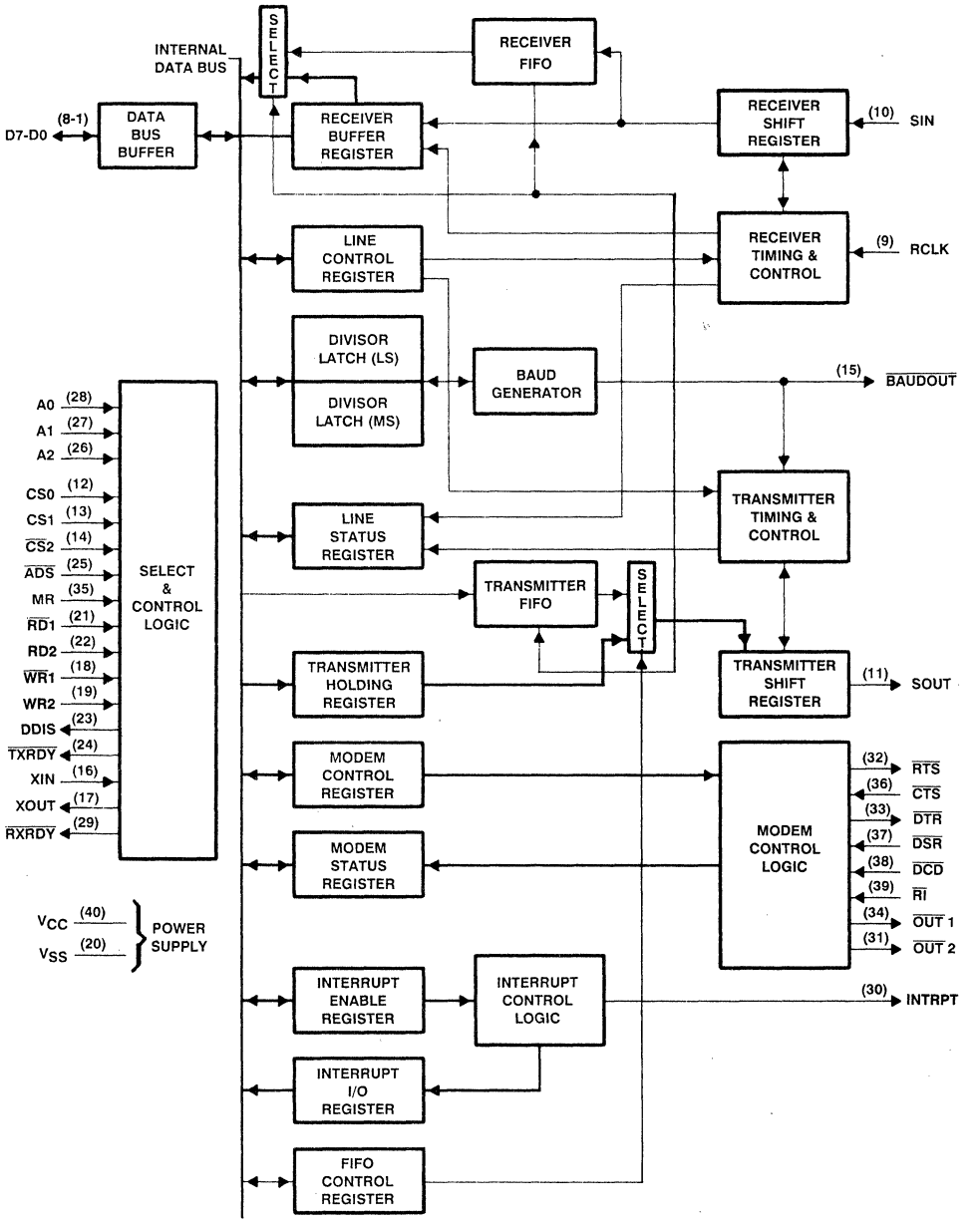
In this mode, internal FIFOs are activated allowing 16 bytes (plus 3 bits or error data per byte in the receiver FIFO) to be stored in both receive and transmit modes. To minimize system overhead and maximize system efficiency, all logic is on the chip. Two of the TL16C450 pin functions (pins 24 and 29 on the N package and pins 27 and 32 on the FN package) have been changed to allow signalling of DMA transfers.

The TL16C550A performs serial-to-parallel conversion on data received from a peripheral device or modem and parallel-to-serial conversion on data received from its CPU. The CPU can read and report on the status of the ACE at any point in the ACE's operation. Reported status information includes: the type of transfer operation in progress, the status of the operation, and any error conditions encountered.

The TL16C550A ACE includes a programmable, on-board, baud rate generator. This generator is capable of dividing a reference clock input by divisors from 1 to $(2^{16} - 1)$ and producing a 16 X clock for driving the internal transmitter logic. Provisions are also included to use this 16 X clock to drive the receiver logic. Also included in the ACE is a complete modem control capability and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

† The TL16C550A can also be reset to the TL16C450 mode under software control.

block diagram



Pin numbers shown are for the N package.

PIN NAME	PIN NO.†	I/O	DESCRIPTION
A0 A1 A2	28 [31] 27 [30] 26 [29]	I	Register Select. Three inputs used during read and write operations to select the ACE register to read from or write to. Refer to Table 1 for register addresses, also refer to the Address Strobe ($\overline{ADS}$) signal description.
$\overline{ADS}$	25 [28]	I	Address Strobe. When $\overline{ADS}$ is active (low), the Register Select signals (A0, A1, and A2) and Chip Select signals (CS0, CS1, $\overline{CS2}$) drive the internal select logic directly; when high, the Register Select and Chip Select signals are held in the state they were in when the low-to-high transition of $\overline{ADS}$ occurred.
$\overline{BAUDOUT}$	15 [17]	O	Baud Out. 16 X clock signal for the transmitter section of the ACE. The clock rate is established by the reference oscillator frequency divided by a divisor specified by the Baud Generator Divisor Latches. $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input.
CS0 CS1 $\overline{CS2}$	12 [14] 13 [15] 14 [16]	I	Chip Select. When active (high, high, and low, respectively), these three inputs select the ACE. If any of these inputs are inactive, the ACE remains inactive. Refer to the $\overline{ADS}$ (Address Strobe) signal description.
$\overline{CTS}$	36 [40]	I	Clear To Send. $\overline{CTS}$ is a modem status signal whose condition can be checked by reading bit 4 (CTS) of the Modem Status Register. Bit 0 (DCTS) of the Modem Status Register indicates that this signal has changed state since the last read from the Modem Status Register. If the Modem Status Interrupt is enabled when $\overline{CTS}$ changes state, an interrupt is generated.
D0 D1 D2 D3 D4 D5 D6 D7	1 [2] 2 [3] 3 [4] 4 [5] 5 [6] 6 [7] 7 [8] 8 [9]	I/O	Data Bus. Eight 3-state data lines provide a bidirectional path for data, control, and status information between the ACE and the CPU.
$\overline{DCD}$	38 [42]	I	Data Carrier Detect. $\overline{DCD}$ is a modem status signal whose condition can be checked by reading bit 7 (DCD) of the Modem Status Register. Bit 3 (DDCD) of the Modem Status Register indicates that this signal has changed state since the last read from the Modem Status Register. If the Modem Status Interrupt is enabled when the $\overline{DCD}$ changes state, and interrupt is generated.
DDIS	23 [26]	O	Driver Disable. This output is active (high) when the CPU is not reading data. When active, this output can be used to disable an external transceiver.
$\overline{DSR}$	37 [41]	I	Data Set Ready. $\overline{DSR}$ is a modem status signal whose condition can be checked by reading bit 5 (DSR) of the Modem Status Register. Bit 1 (DDSR) of the Modem Status Register indicates that this signal has changed state since the last read from the Modem Status Register. If the modem status interrupt is enabled when the $\overline{DSR}$ changes state, an interrupt is generated.
$\overline{DTR}$	33 [37]	O	Data Terminal Ready. When active (low), $\overline{DTR}$ informs a modem or data set that the ACE is ready to establish communication. $\overline{DTR}$ is placed in the active state by setting the DTR bit of the Modem Control Register to a high level. $\overline{DTR}$ is placed in the inactive state either as a result of a Master Reset or during loop mode operation or resetting bit 0 (DTR) of the Modem Control Register.
INTRPT	30 [33]	O	Interrupt. When active (high), INTRPT informs the CPU that the ACE has a interrupt to be serviced. Four conditions that cause an interrupt to be issued are; a receiver error, received data is available or timeout (FIFO mode only), the transmitter holding register is empty, and an enabled modem status interrupt. The INTRPT output is reset (deactivated) either when the interrupt is serviced or as a result of a Master Reset.
MR	35 [39]	I	Master Reset. When active (high), MR clears most ACE registers and sets the state of various output signals. Refer to Table 2, ACE Reset Functions.
$\overline{OUT1}$ $\overline{OUT2}$	34 [38] 31 [35]	O	Outputs 1 and 2. User-designated output pins that are set to their active states by setting their respective Modem Control Register bits (OUT 1 and OUT 2) high. $\overline{OUT}$ 1 and $\overline{OUT}$ 2 are set to their inactive (high) states as a result of Master Reset or during loop mode operations or by resetting bit 2 (OUT 1) or bit 3 (OUT 2) of the MCR.
RCLK	9 [10]	I	Receiver Clock. The 16 X baud rate clock for the receiver section of the ACE.
$\overline{RD1}$ RD2	21 [24] 22 [25]	I	Read inputs. When either input is active (high or low, respectively) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register. Only one of these inputs is required for the transfer of data during a read operation; the other input should be tied in its inactive state (i.e., RD2 tied low or $\overline{RD1}$ tied high).

† Pin numbers shown in brackets are for the FN package.

PIN NAME	PIN NO.†	I/O	DESCRIPTION
$\overline{RI}$	39 [43]	I	Ring indicator. $\overline{RI}$ is a modem status signal whose condition can be checked by reading bit 6 (RI) of the Modem Status Register. Bit 2 (TERI) of the Modem Status Register indicates that the $\overline{RI}$ input has transitioned from a low to a high state since the last read from the Modem Status Register. If the Modem Status Interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{RTS}$	32 [36]	O	Request to Send. When active, informs the modem or data set that the ACE is ready to transmit data. $\overline{RTS}$ is set to its active state by setting the RTS Modem Control Register bit and is set to its inactive (high) state either as a result of a Master Reset or during loop-mode operations or by resetting bit 1 (RTS) of the MCR.
$\overline{RXRDY}$	29 [32]	O	Receiver Ready Output. Receiver DMA signalling is available with this pin. When operating in the FIFO mode, one of two types of DMA signalling can be selected via FCR3. When operating in the TL16V450 mode, only DMA Mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the receiver FIFO has been emptied. In DMA Mode 0 (FCRO = 0 or FCRO = 1, FCR3 = 0), if there is at least 1 character in the receiver FIFO or receiver holding register, $\overline{RXRDY}$ will be active (low). When RXRDY has been active but there are no characters in the FIFO or holding register, $\overline{RXRDY}$ will go inactive (high). In DMA Mode 1 (FCRO = 1, FCR3 = 1), when the trigger level or the timeout has been reached, $\overline{RXRDY}$ will go active (low); when it has been active but there are no more characters in the FIFO or holding register, it will go inactive (high).
SIN	10 [11]	I	Serial Input. Serial data input from a connected communications device.
SOUT	11 [13]	O	Serial Output. Composite serial data output to a connected communication device. SOUT is set to the Marking (logic 1) state as a result of Master Reset.
$\overline{TXRDY}$	24 [27]	O	Transmitter Ready Output. Transmitter DMA signalling is available with this pin. When operating in the FIFO mode, one of two types of DMA signalling can be selected via FCR3. When operating in the TL16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the transmit FIFO has been filled.
V_{CC}	40 [44]		5-V Supply Voltage
V_{SS}	20 [22]		Supply Common
$\overline{WR1}$ WR2	18 [20] 19 [21]	I	Write Inputs. When either input is active (high or low, respectively), while the ACE is selected, the CPU is allowed to write control words or data into a selected ACE register. Only one of these inputs if required to transfer data during a write operation; the other input should be tied in its inactive state (i.e., WR2 tied low or $\overline{WR1}$ tied high).
XIN XOUT	16 [18] 17 [19]	I/O	External Clock. Connects the ACE to the main timing reference (clock or crystal).

† Pin numbers shown in brackets are for the FN package.

absolute maximum ratings over free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... – 0.5 V to 7 V
Input voltage range at any input, V_I ..... – 0.5 V to 7 V
Output voltlage range, V_O ..... – 0.5 V to 7 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Case temperature for 10 seconds: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package ..... 260°C

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	– 0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}‡	High-level output voltage	I_{OH} = −1 mA	2.4			V
V_{OL}‡	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
I_{lkg}	Input leakage current	V_{CC} = 5.25 V, V_{SS} = 0, V_I = 0 to 5.25 V, All other pins floating			±10	µA
I_{OZ}	High-impedance output current	V_{CC} = 5.25 V, V_{SS} = 0, V_O = 0 to 5.25 V, Chip selected in Write mode or Chip deselected			±20	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, T_A = 25°C, SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V, All other inputs at 0.8 V, XTAL1 at 4 MHz, No load on outputs, Baud rate = 50 kilobits per second			10	mA
C_{XIN}	Clock input capacitance	V_{CC} = 0, V_{SS} = 0, All other pins grounded, f = 1 MHz, T_A = 25°C		15	20	pF
C_{XOUT}	Clock output capacitance			20	30	pF
C_i	Input capacitance			6	10	pF
C_o	Output capacitance			10	20	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ These parameters apply for all outputs except XOUT.

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	FIGURE	MIN	MAX	UNIT
t_{cR}	Cycle time, read ($t_{w7} + t_{d8} + t_{d9}$)	RC		175		ns
t_{cW}	Cycle time, write ($t_{w6} + t_{d5} + t_{d6}$)	WC		175		ns
t_{w5}	Pulse duration, address strobe low	t_{ADS}	2,3	15		ns
t_{w6}	Pulse duration, write strobe	t_{WR}	2	80		ns
t_{w7}	Pulse duration, read strobe	t_{RD}	3	80		ns
t_{w8}	Pulse duration, master reset	t_{MR}		1		µs
t_{su1}	Setup time, address	t_{AS}	2,3	15		ns
t_{su2}	Setup time, chip select	t_{CS}	2,3	15		ns
t_{su3}	Setup time, data	t_{DS}	2	15		ns
t_{h1}	Hold time, address	t_{AH}	2,3	0		ns
t_{h2}	Hold time, chip select	t_{CH}	2,3	0		ns
t_{h3}	Hold time, write to chip select	t_{WCS}	2	20		ns
t_{h4}	Hold time, write to address	t_{WA}	2	20		ns
t_{h5}	Hold time, data	t_{DH}	2	15		ns
t_{h6}	Hold time, read to chip select	t_{RCS}	3	20		ns
t_{h7}	Hold time, read to address	t_{RA}	3	20		ns
t_{d4}§	Delay time, select to write	t_{CSW}	2	15		ns
t_{d5}§	Delay time, address to write	t_{AW}	2	15		ns
t_{d6}	Delay time, write cycle	t_{WC}	2	80		ns
t_{d7}§	Delay time, chip select to read	t_{CSR}	3	15		ns
t_{d8}§	Delay time, address to read	t_{AR}	3	15		ns
t_{d9}	Delay time, read cycle	t_{RC}	3	80		ns

§ Only applies when ADS is low.

system switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 2)

	PARAMETER	ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w1}	Pulse duration, clock high	t_{XH}	1	f = 9 MHz maximum	50		ns
t_{w2}	Pulse duration, clock low	t_{XL}	1	f = 9 MHz maximum	50		ns
t_{d10}	Delay time, read to data	t_{RVD}	3	C_L = 100 pF		60	ns
t_{d11}	Delay time, read to floating data	t_{HZ}	3	C_L = 100 pF	0	60	ns
$t_{dis(R)}$	Read to driver disable	t_{RDD}	3	C_L = 100 pF		60	ns

baud generator switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w3}	Pulse duration, $\overline{\text{BAUDOUT}}$ low	t_{LW}	1	f = 9 MHz, CLK ÷ 2, C_L = 100 pF	80		ns
t_{w4}	Pulse duration, $\overline{\text{BAUDOUT}}$ high	t_{HW}	1	f = 9 MHz, CLK ÷ 2, C_L = 100 pF	100		ns
t_{d1}	Delay time, $\overline{\text{BAUDOUT}}$ low to high	t_{BLD}	1	C_L = 100 pF		125	ns
t_{d2}	Delay time, $\overline{\text{BAUDOUT}}$ high to low	t_{BHD}	1	C_L = 100 pF		125	ns

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 3)

	PARAMETER	ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d12}	Delay time, RCLK to sample	t_{SCD}	4			100	ns
t_{d13}	Delay time, stop to set interrupt or read RBR to LSI interrupt	t_{SINT}	4,5,6,7,8			1	RCLK cycles
t_{d14}	Delay time, read RBR/LSR to reset interrupt	t_{RINT}	4,5,6,7,8	C_L = 100 pF		150	ns

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d15}	Delay time, initial write to transmit start	t_{IRS}	9		8	24	baudout cycles
t_{d16}	Delay time, stop to interrupt	t_{STI}	9		8	8	baudout cycles
t_{d17}	Delay time, write THR to reset interrupt	t_{HR}	9	C_L = 100 pF		140	ns
t_{d18}	Delay time, initial write to interrupt (THRE)	t_{SI}	9		16	32	baudout cycles
t_{d19}	Delay time, read IIR to reset interrupt (THRE)	t_{IR}	9	C_L = 100 pF		140	ns
t_{d20}	Delay time, write to TXRDY inactive	t_{WXI}	10,11	C_L = 100 pF		195	ns
t_{d21}	Delay time, start to TXRDY active	t_{SXA}	10,11	C_L = 100 pF		8	baudout cycles

modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d22}	Delay time, write MCR to output	t_{MDO}	12	C_L = 100 pF		100	ns
t_{d23}	Delay time, modem interrupt to set interrupt	t_{SIM}	12	C_L = 100 pF		170	ns
t_{d24}	Delay time, read MSR to reset interrupt	t_{RIM}	12	C_L = 100 pF		140	ns

NOTES: 2. Charge and discharge time is determined by V_{OL}, V_{OH}, and external loading.
3. In FIFO mode RC = 425 ns (minimum) between reads of the receiver FIFO and the status registers (interrupt identification register or line status register).

PARAMETER MEASUREMENT INFORMATION

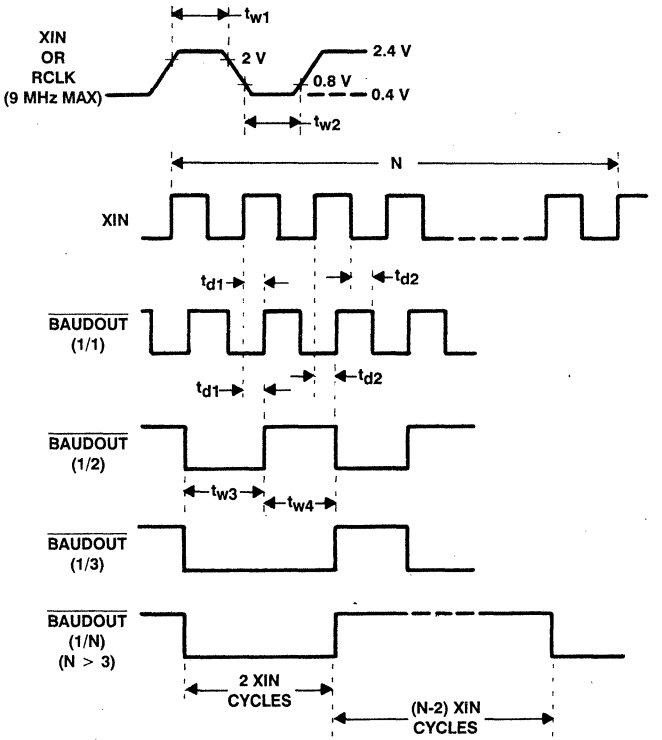
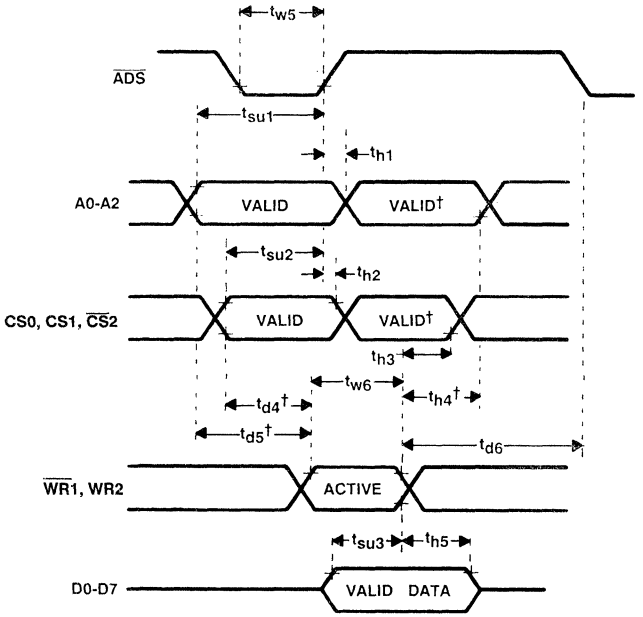


FIGURE 1. BAUD GENERATOR TIMING

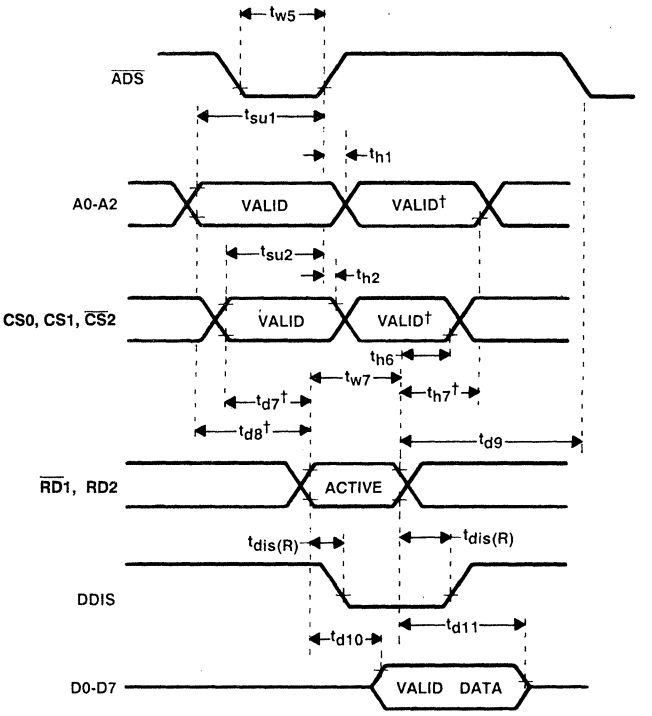
PARAMETER MEASUREMENT INFORMATION



† Applicable only when ADS is tied low.

FIGURE 2. WRITE CYCLE TIMING

PARAMETER MEASUREMENT INFORMATION



† Applicable only when ADS is tied low.

FIGURE 3. READ CYCLE TIMING

PARAMETER MEASUREMENT INFORMATION

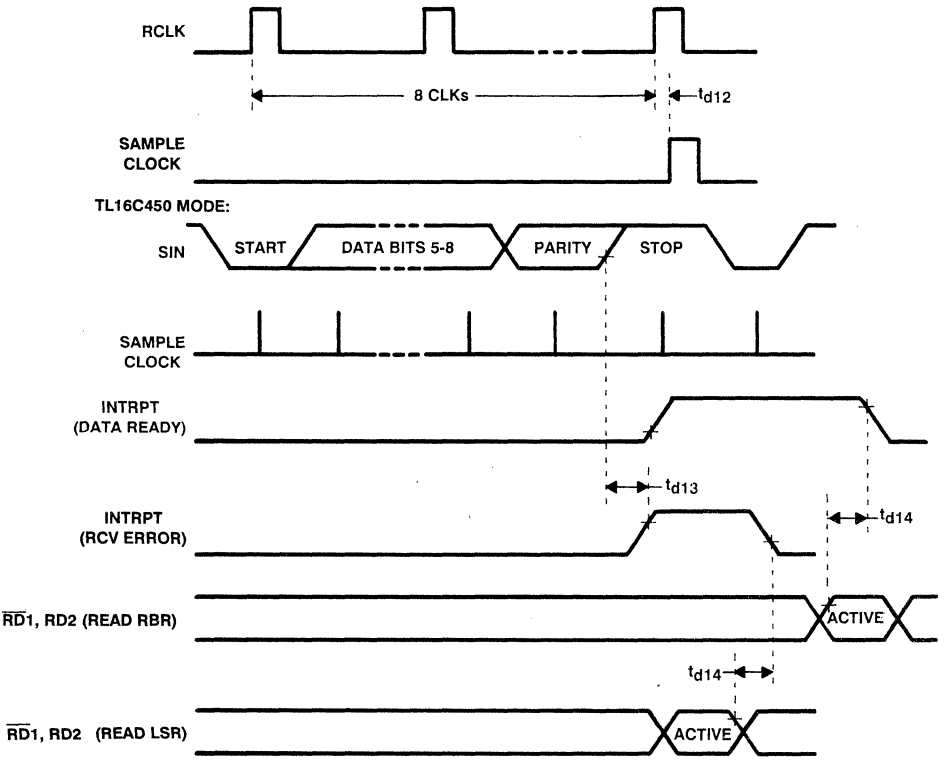


FIGURE 4. RECEIVER TIMING

PARAMETER MEASUREMENT INFORMATION

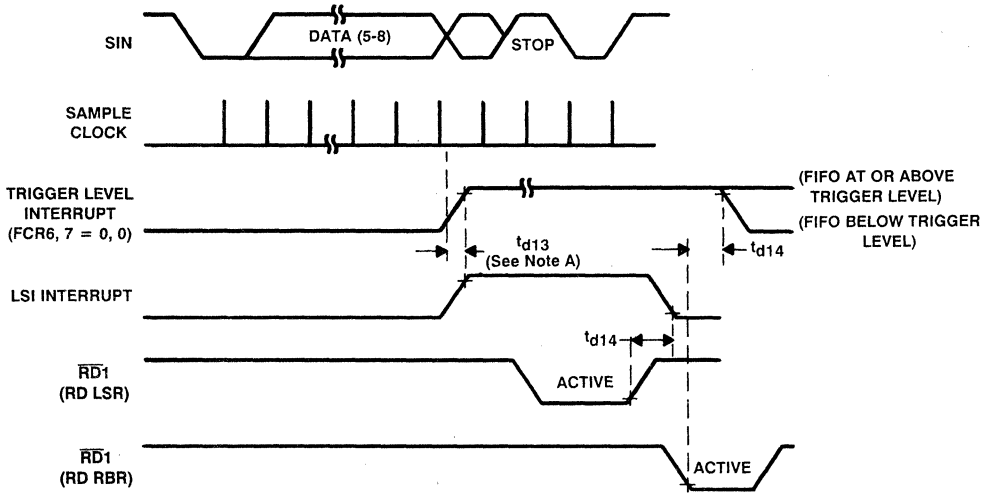


FIGURE 5. RECEIVER FIFO FIRST BYTE (SETS DR BIT)

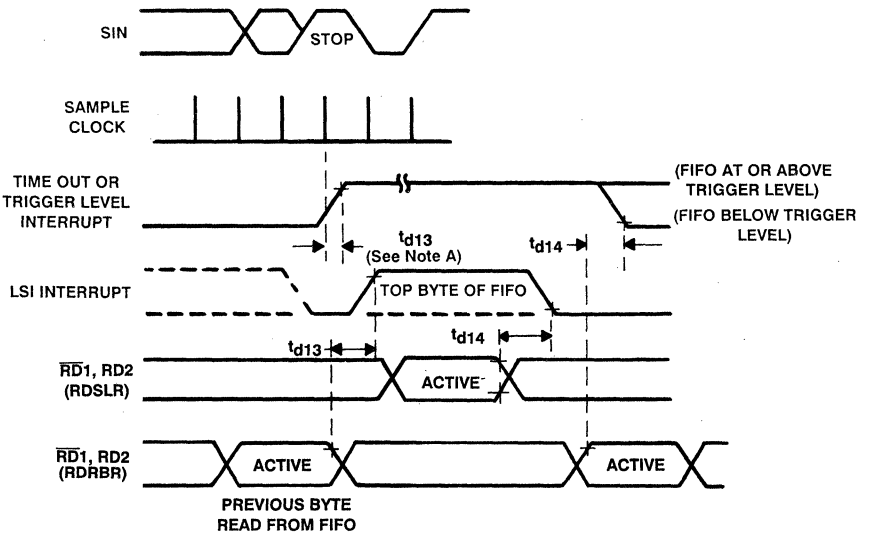
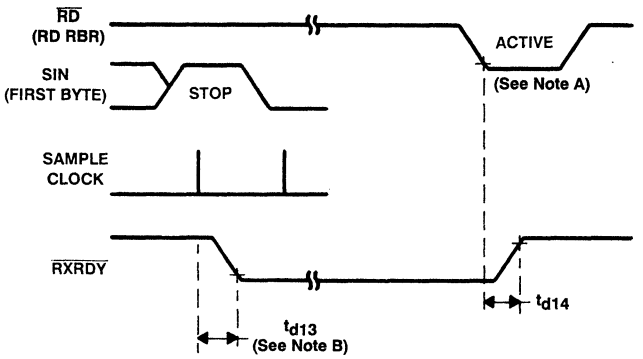


FIGURE 6. RECEIVER FIFO BYTES OTHER THAN THE FIRST BYTE (DR INTERNAL BIT ALREADY SET)

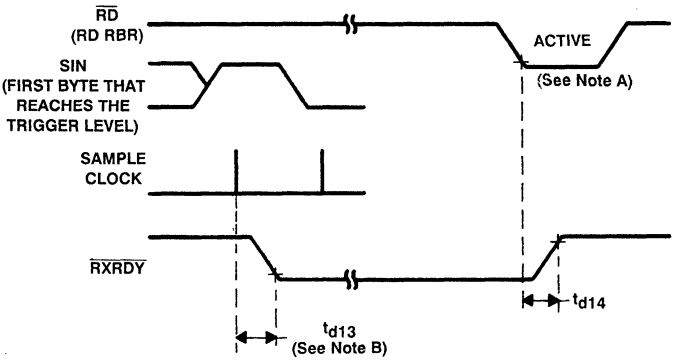
NOTE A: For a timeout interrupt, t_{d13} = 8 RCLKs.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This is the reading of the last byte in the FIFO.
B. For a timeout interrupt, t_{d13} = 8 RCLKs.

FIGURE 7. RECEIVER READY (PIN 29), FCR0 = 0 OR FCR0 = 1 AND FCR3 = 0 (MODE 0)



NOTES: A. This is the reading of the last byte in the FIFO.
B. For a timeout interrupt, t_{d13} = 8 RCLKs.

FIGURE 8. RECEIVER READY (PIN 29) FCR = 1 AND FCR3 = 1 (MODE 1)

PARAMETER MEASUREMENT INFORMATION

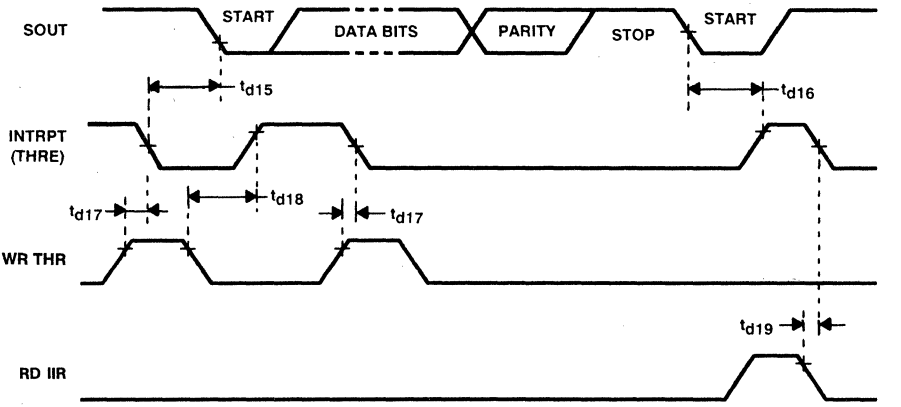


FIGURE 9. TRANSMITTER TIMING

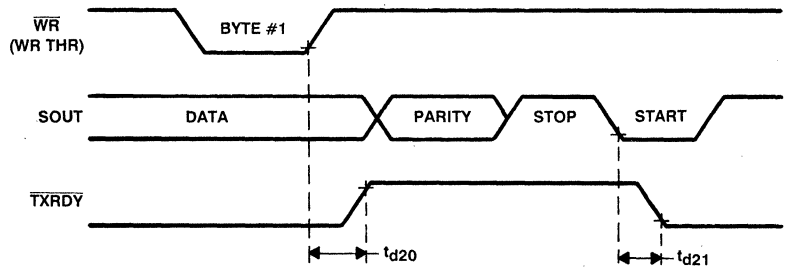


FIGURE 10. TRANSMITTER READY (PIN 24), FCR0 = 0 OR FCR0 = 1 AND FCR3 = 0 (MODE 0)

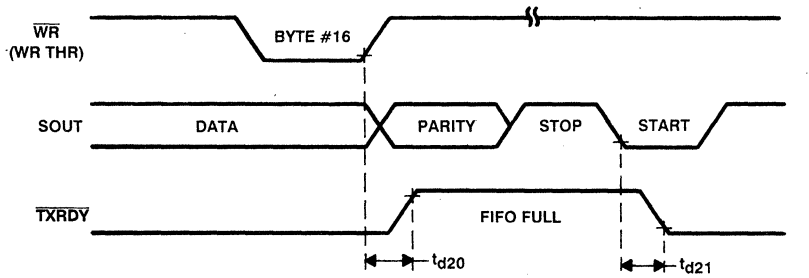


FIGURE 11. TRANSMITTER READY (PIN 24) FCR0 = 1 AND FRCR3 = 1 (MODE 1)

PARAMETER MEASUREMENT INFORMATION

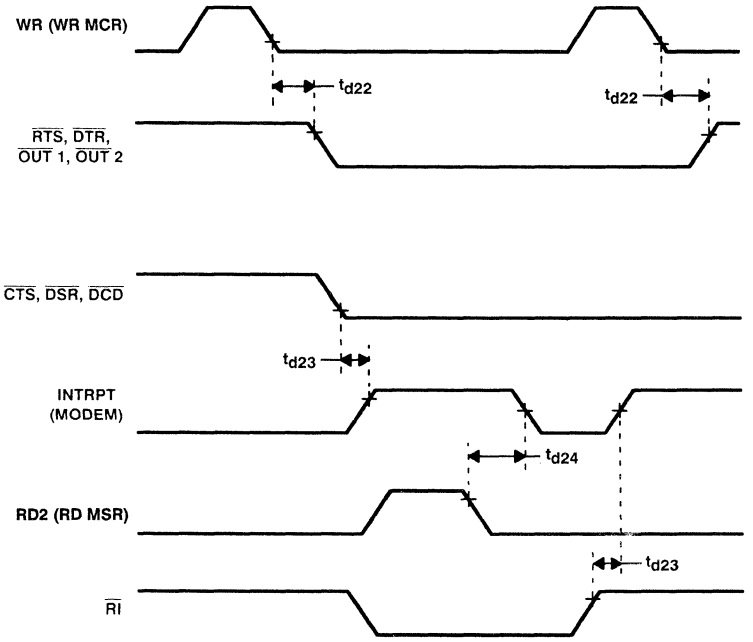


FIGURE 12. MODEM CONTROL TIMING

APPLICATION INFORMATION

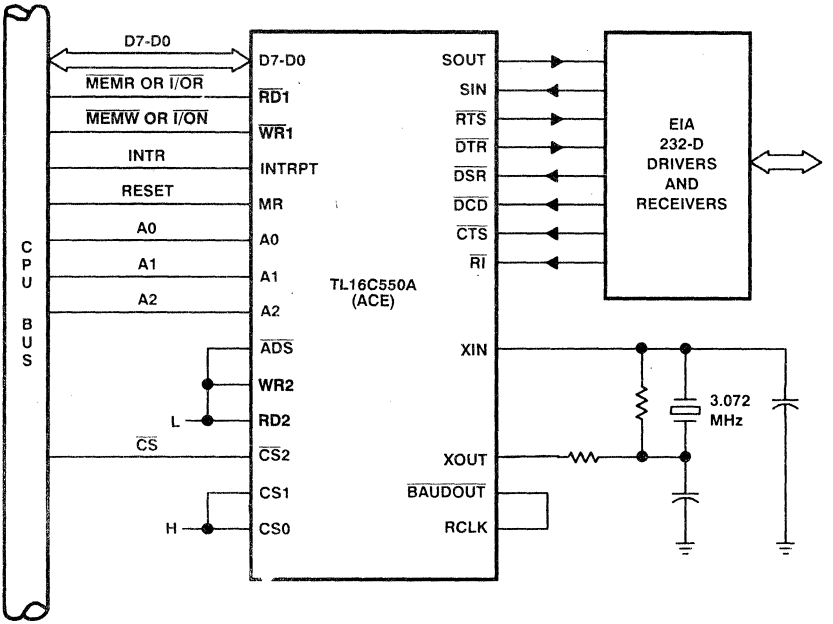


FIGURE 13. BASIC TL16C550A CONFIGURATION

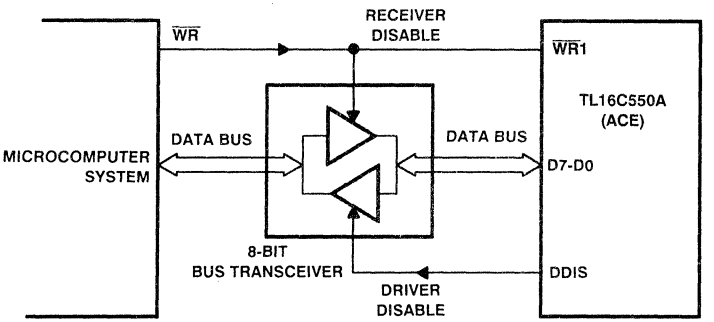


FIGURE 14. TYPICAL INTERFACE FOR A HIGH-CAPACITY DATA BUS

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APPLICATION INFORMATION

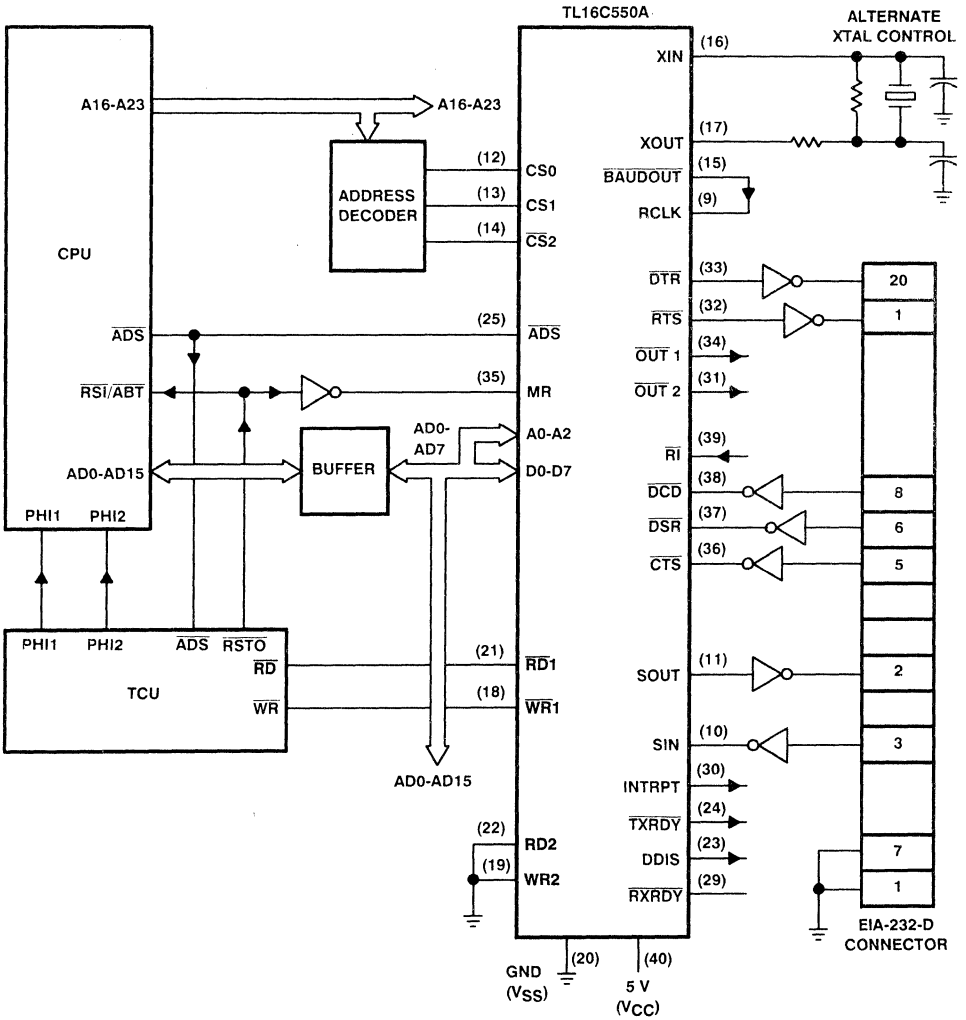


FIGURE 15. TYPICAL TL16C550A CONNECTION TO A CPU

PRINCIPLES OF OPERATION

TABLE 1. REGISTER SELECTION

DLAB†	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding register (write)
0	L	L	H	Interrupt enable
X	L	H	L	Interrupt identification (read only)
X	L	H	L	FIFO control (write)
X	L	H	H	Line control
X	H	L	L	Modem control
X	H	L	H	Line status
X	H	H	L	Modem status
X	H	H	H	Scratch
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor Latch (MSB)

† The Divisor Latch Access Bit (DLAB) is the most significant bit of the Line Control Register. The DLAB signal is controlled by writing to this bit location (see Table 3).

TABLE 2. ACE RESET FUNCTIONS

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is high, bits 1-3 are low, and bits 4-7 are permanently low
FIFO Control Register	Master Reset	All bits low
Line Control Register	Master Reset	All bits low
Modem Control Register	Master Reset	All bits low (5-7 permanent)
Line Status Register	Master Reset	Bits 5 and 6 are high, all other bits are low
Modem Status Register	Master Reset	Bits 0-3 are low, bits 4-7 are input signals
SOUT	Master Reset	High
INTRPT (Receiver Error Flag)	Read LSR/MR	Low
INTRPT (Received Data Available)	Read RBR/MR	Low
INTRPT (Transmitter Holding Register Empty)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{OUT}$ 2	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT}$ 1	Master Reset	High
Scratch Register	Master Reset	No effect
Divisor Latch (LSB and MSB) Registers	Master Reset	No effect
Receiver Buffer Registers	Master Reset	No effect
Transmitter Holding Registers	Master Reset	No effect
RCVR FIFO	MR/FCR1·FCR0/ ΔFCR0	All bits low
XMIT FIFO	MR/FCR2·FCR0/ ΔFCR0	All bits low

PRINCIPLES OF OPERATION

accessible registers

The system programmer, via the CPU, has access to and control over any of the ACE registers that are summarized in Table 3. These registers are used to control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

TABLE 3. SUMMARY OF ACCESSIBLE REGISTERS

Bit No.	REGISTER ADDRESS											
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LSB)	Latch (MSB)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR[#]	MSR	SCR	DLL	DLM
0	Data Bit 0†	Data Bit 0	Enable Received Data Available Interrupt (ERBI)	"0" if Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (ΔCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Receiver FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (ΔDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Transmitter FIFO Reset	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit (2) (Note 4)	DMA Mode Select	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (ΔDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled (Note 4)	Receiver Trigger (LSB)	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled (Note 4)	Receiver Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO (Note 4)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

† Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
NOTE 4: These bits are always 0 in the TL16C450 mode.

PRINCIPLES OF OPERATION

receiver buffer register (RBR)

The ACE's receiver section consists of a Receiver Shift Register (RSR) and a Receiver Buffer Register (RBR). The RBR is actually a 16-byte FIFO. Timing is supplied by the 16 X Receiver Clock (RCLK). Receiver section control is a function of the ACE's Line Control Register.

The ACE's RSR receives serial data from the Serial Input (SIN) pin. The RSR then deserializes the data and moves it into the RBR FIFO. In the TL16C450 mode, when a character is placed in the Receiver Buffer Register and the Received Data Available interrupt is enabled, an interrupt is generated. This interrupt is cleared when the data is read out of the Receiver Buffer Register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO Control Register.

transmitter holding register (THR)

The ACE's transmitter section consists of a Transmitter Holding Register (THR) and a Transmitter Shift Register (TSR). The THR is actually a 16-byte FIFO. Timing is supplied by the Baud Out ($\overline{\text{BAUDOUT}}$) clock signal. Transmitter section control is a function of the ACE's Line Control Register.

The ACE THR receives data off the Internal Data Bus and, when the shift register is idle, moves it into the TSR. The TSR serializes the data and outputs it at the Serial Output (SOUT). In the TL16C450 mode, if the THR is empty and the Transmitter Holding Register Empty (THRE) interrupt is enabled, an interrupt is generated. This interrupt is cleared when a character is loaded into the register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

interrupt enable register (IER)

The Interrupt Enable Register enables each of the five types of interrupts (refer to Table 4) and the INTRPT output signal in response to an interrupt generation. The Interrupt Enable Register can also be used to disable the interrupt system by setting bits 0 through 3 to logic 0. The contents of this register are summarized in Table 3 and are described below.

Bit 0. This bit, when set to logic 1, enables the Received Data Available interrupt.

Bit 1. This bit, when set to logic 1, enables the Transmitter Holding Register Empty interrupt.

Bit 2. This bit, when set to logic 1, enables the Receiver Line Status interrupt.

Bit 3. This bit, when set to logic 1, enables the Modem Status interrupt.

Bits 4 thru 7. Bits 4 through 7 in the Interrupt Enable Register are not used and are always set to logic 0.

FIFO control register

The FIFO control register (FCR) is a write-only register at the same location as the IIR, which is a read-only register. The FCR is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signalling.

Bit 0. FCR0, when set to logic 1, enables the transmit and receive FIFOs. This bit must be a 1 when other FCR bits are written to or they will not be programmed. Changing this bit clears the FIFOs.

Bit 1. FCR1, when set to logic 1, clears all bytes in the receiver FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self clearing.

Bit 2. FCR2, when set to logic 1, clears all bytes in the transmit FIFO and resets its counter to 0. The shift register is not cleared. The 1 that is written to this bit position is self clearing.

Bit 3. If FCR0 is a 1, setting FCR3 to a 1 causes the $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ to change from mode 0 to mode 1.

PRINCIPLES OF OPERATION

Bits 4 and 5. FCR4 and FCR5 are reserved for future use.

Bits 6 and 7. FCR6 and FCR7 are used to set the trigger level for the receiver FIFO interrupt.

BIT 7	BIT 6	RECEIVER FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most popular microprocessors.

The ACE provides four prioritized levels of interrupts:

Priority 1 – Receiver line status (highest priority)
Priority 2 – Receiver data ready or Receiver character timeout
Priority 3 – Transmitter holding register empty
Priority 4 – Modem status (lowest priority)

When an interrupt is generated, the Interrupt Identification Register indicates that an interrupt is pending and the type of that interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 4. Detail on each bit are as follows:

Bit 0. This bit can be used either in a hardwire-prioritized, or polled interrupt system. If this bit is a logic 0, an interrupt is pending. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2. These two bits are used to identify the highest priority interrupt pending, as indicated in Table 4.

Bit 3. This bit is always 0 in the TL16C450 mode. In FIFO mode, this bit is set with bit 2 to indicate that a timeout interrupt is pending.

Bits 4 thru 5. These two bits are not used and are always set at logic 0.

Bits 6 and 7. These two bits are always 0 in the TL16C450 mode. They are set when bit 0 of the FIFO Control Register is equal to 1.

PRINCIPLES OF OPERATION

TABLE 4. INTERRUPT CONTROL FUNCTIONS

INTERRUPT IDENTIFICATION REGISTER				PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 3	BIT 2	BIT 1	BIT 0				
0	0	0	1	None	None	None	–
0	1	1	0	1	Receiver line status	Overrun error, parity error, framing error,or break interrrupt	Reading the Line Status register
1	1	0	0	2	Received data available	Receiver data available in the TL16C450 mode or trigger level reached in the FIFO mode.	Reading the Receiver buffer Buffer register
1	1	0	0	2	Character timeout indication	No characters have been removed from or input to the receiver FIFO during the last four character times and there is at least one character in it during this time	Reading the Receiver Buffer Register
0	0	1	0	3	Transmitter Holding register empty	Transmitter Holding register empty	Reading the Interrupt Identification register (if source of interrupt) or writing into the Transmitter Holding register
0	0	0	0	4	Modem status	Clear to Send, Data Set Ready, Ring Indicator, or Data Carrier Detect	Reading the Modem Status register

PRINCIPLES OF OPERATION

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the Line Control register. In addition, the programmer is able to retrieve, inspect, and modify the contents of the Line Control register; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and are described below.

Bits 0 and 1. These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2. This bit specifies either one, one and one-half, or two Stop bits in each transmitted character. If bit 2 is a logic 0, one Stop bit is generated in the data. If bit 2 is a logic 1, the number of Stop bits generated is dependent on the word length selected with bits 0 and 1. The receive clocks the first stop bit only, regardless of the number of stop bits selected. The number of Stop bits generated, in relation to word length and bit 2, is shown in the following.

Bit 2	Word Length Selected by Bits 1 and 2	Number of Stop Bits Generated
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

Bit 3. This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, if bit 3 is a logic 1, parity is checked. When bit 3 is a logic 0, no parity is generated or checked.

Bit 4. Bit 4 is the Even Parity Select bit. When parity is enabled by bit 3: a logic 1 in bit 4 produces Even Parity (an even number of logic 1s in the data and parity bits) and a logic 0 in bit 4 produces Odd Parity (an odd number of logic 1s).

Bit 5. This is the Stick parity bit. When bits 3, 4, and 5 are logic 1s, the Parity bit is transmitted and checked as a logic 0. When bits 3 and 5 are logic 1s and bit 4 is a logic 0, the Parity bit is transmitted and checked as a logic 1. If bit 5 is a logic 0, stick parity is disabled.

Bit 6. This bit is the Break Control bit. Bit 6 is set to a logic 1 to force a break condition, i.e, a condition where the Serial Output (SOUT) pin is forced to the spacing (logic 0) state. When bit 6 is set to a logic 0, the break condition is disabled. The break condition has no effect on the transmitter logic; it only effects the serial output.

Bit 7. This bit is the Divisor Latch Access bit (DLAB). Bit 7 must be set to a logic 1 to access the Divisor Latches of the Baud Generator during a read or write. Bit 7 must be set to a logic 0 during a read or write to access the Receiver Buffer, the Transmitter Holding register, or the Interrupt Enable register.

modem control register (MCR)

The Modem Control register is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described below.

Bit 0. Bit 0 (DTR) controls the Data Terminal Ready ($\overline{DTR}$) output. Setting this bit to a logic 1 forces the $\overline{DTR}$ output to its low state. When bit 0 is set to a logic 0, $\overline{DTR}$ goes high.

Bit 1. Bit 1 (RTS) controls the Request to Send ($\overline{RTS}$) output in a manner identical to Bit 0's control over the $\overline{DTR}$ output.

Bit 2. Bit 2 (OUT 1) controls the Output 1 ($\overline{OUT}$ 1) signal, a user-designated output signal, in a manner identical to Bit 0's control over the $\overline{DTR}$ output.

Bit 3. Bit 3 (OUT 2) controls the Output 2 ($\overline{OUT}$ 2) signal, a user-designated output signal, in a manner identical to Bit 0's control over the $\overline{DTR}$ output.

Bit 4. Bit 4 provides a local loopback feature for diagnostic testing of the ACE. When this bit is set to a logic high, the following occurs:

1. The transmitter Serial Output (SOUT) is set high.
2. The receiver Serial Input (SIN) is disconnected.
3. The output of the Transmitter Shift register is looped back into the Receiver Shift register input.
4. The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected.
5. The four modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT}$ 1, and $\overline{OUT}$ 2) are internally connected to the four modem control inputs.
6. The four modem control output pins are forced to their inactive states (high).

In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit- and receive-data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational but the modem control interrupt's sources are now the lower four bits of the Modem Control register instead of the four modem control inputs. All interrupts are still controlled by the Interrupt Enable register.

Bit 5 through 7. These bits are permanently set to logic 0.

line status register (LSR)†

The Line Status Register provides information to the CPU concerning the status of data transfers. The contents of this register are described below and summarized in Table 3.

Bit 0. Bit 0 is the Data Ready (DR) indicator for the receiver. This bit is set to a logic 1 condition whenever a complete incoming character has been received and transferred into the Receiver Buffer register or the FIFO and is reset to logic 0 by reading all of the data in the Receiver Buffer Register or the FIFO.

Bit 1‡. Bit 1 is the Overrun Error (OE) indicator. When this bit is set to logic 1, it indicates that before the character in the Receiver Buffer register was read, it was overwritten by the next character transferred into the register. The OE indicator is reset every time the CPU reads the contents of the Line Status register. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but is not transferred to the FIFO.

Bit 2‡. Bit 2 is the Parity Error (PE) indicator. When this bit is set to logic 1, it indicates that the parity of the received data character does not match the parity selected in the Line Control Register (bit 4). The PE bit is reset every time the CPU reads the contents of the Line Status register. In the FIFO mode, this error is

† The Line Status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.
‡ Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt.

associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 3‡. Bit 3 is the Framing Error (FE) indicator. When this bit is set to logic 1, it indicates that the received character did not have a valid (logic 1) Stop bit. The FE bit is reset every time the CPU reads the contents of the Line Status register. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. The ACE will try to resynchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit. The ACE then samples this start bit twice and then accepts the input data.

Bit 4‡. Bit 4 is the Break Interrupt (BI) indicator. When this bit is set to logic 1, it indicates that the received data input was held in the logic 0 state for longer than a full-word transmission time. A "full-word transmission time" is defined as the total time of the Start, Data, Parity, and Stop bits. The BI bit is reset every time the CPU reads the contents of the Line Status register. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs, only one 0 character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.

Bit 5. Bit 5 is the Transmitter Holding Register Empty (THRE) indicator. This bit is set to logic 1 when the Transmitter Holding Register is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when the THRE bit is a logic 1, then an interrupt is generated. THRE is set to a logic 1 when the contents of the Transmitter Holding Register are transferred to the transmitted Shift Register. This bit is reset to logic 0 concurrent with the loading of the Transmitter Holding Register by the CPU. In the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.

Bit 6. Bit 6 is the Transmitter Empty (TEMT) indicator. This bit is set to a logic 1 when the Transmitter Holding register and the Transmitter Shift register are both empty. When either the Transmitter Holding register or the Transmitter Shift register contains a data character, the TEMT bit is reset to logic 0. In the FIFO mode, this bit is set to a 1 when the transmitter FIFO and shift register are both empty.

Bit 7. In the TL16C550A, this bit is always reset to logic 0. In the TL16C450 mode, this bit is always a 0. In the FIFO mode, LSR7 is set when there is at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO.

‡ Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt.

modem status register (MSR)

The Modem Status register is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provides change information; when a control input from the modem changes state, the appropriate bit is set to logic 1. All four bits are reset to logic 0 when the CPU reads the Modem Status register. The contents of this register are summarized in Table 3 and are described below.

Bit 0. Bit 0 is the change in Clear to Send (DCTS) indicator. This bit indicates that the $\overline{CTS}$ input has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the Modem Status Interrupt is enabled, a Modem Status Interrupt is generated.

Bit 1. Bit 1 is the change in Data Set Ready (DDSR) indicator. This bit indicates that the $\overline{DSR}$ input has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the Modem Status Interrupt is enabled, a Modem Status Interrupt is generated.

Bit 2. Bit 2 is the Trailing Edge of Ring Indicator (TERI) detector. This bit indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state. When this bit is a logic 1 and the Modem Status Interrupt is enabled, a Modem Status Interrupt is generated.

Bit 3. Bit 3 is the change in Data Carrier Detect (DDCD) indicator. This bit indicates that the $\overline{DCD}$ input to the chip has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the Modem Status Interrupt is enabled, a Modem Status Interrupt is generated.

Bit 4. Bit 4 is the compliment of the Clear to Send ($\overline{CTS}$) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control register bit 1 (RTS).

Bit 5. Bit 5 is the compliment of the Data Set Ready ($\overline{DSR}$) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control register bit 0 (DTR).

Bit 6. Bit 6 is the compliment of the Ring Indicator ($\overline{RI}$) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control registers bit 2 (OUT 1).

Bit 7. Bit 7 is the compliment of the Data Carrier Detect ($\overline{DCD}$) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control registers bit 3 (OUT 2).

scratch register (SCR)

The Scratch register is an 8-bit register that is intended for the programmer's use as a "scratchpad," in the sense that it will temporarily hold the programmer's data without affecting any other ACE operation.

programmable baud generator

The ACE contains a programmable baud generator that takes a clock input in the range between dc and 8 MHz and divides it by a divisor in the range between 1 and $2^{16}-1$. The output frequency of the baud generator is sixteen times (16 X) the baud rate. The formula for the divisor is:

$$\text{divisor \#} = \text{XIN frequency input} \div (\text{desired baud rate X } 16)$$

Two 8-bit registers, called divisor latches, are used to store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the ACE in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

Tables 5 and 6, which follow, illustrate the use of the baud generator with crystal frequencies of 1.8432 MHz and 3.072 MHz, respectively. For baud rates of 38.4 kilobits per second and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency.

Refer to Figure 10 for examples of typical clock circuits.

FIFO interrupt-mode operation

When the receiver FIFO and receiver interrupts are enabled (FCR0 = 1, IER0 = 1) receiver interrupts will occur as follows:

1. The Receive Data Available interrupt will be issued to the microprocessor when the FIFO has reached its programmed trigger level. It will be cleared as soon as the FIFO drops below its programmed trigger level.
2. The IIR Receive Data Available indication also occurs when the FIFO trigger level is reached, and, like the interrupt, it is cleared when the FIFO drops below the trigger level.
3. The Receiver Line Status interrupt (IIR = 06), as before, has higher priority than the Received Data Available (IIR = 04) interrupt.
4. The data ready bit (LSR0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

When receiver FIFO and receiver interrupts are enabled, receiver FIFO timeout interrupts will occur as follows:

1. FIFO timeout interrupt will occur if the following conditions exist:
   a. At least one character is in the FIFO.
   b. The most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed, the second one is included in this time delay).

c. The most recent microprocessor read of the FIFO was longer than 4 continuous character times ago.

This will cause a maximum character received to interrupt issued delay of 160 ms at 300 baud with a 12-bit character.

2. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).
3. When a timeout interrupt has occurred, it is cleared and the timer reset when the microprocessor reads one character from the receiver FIFO.
4. When a timeout interrupt has not occurred, the timeout timer is reset after a new character is received or after the microprocessor reads the receiver FIFO.

When the transmit FIFO and transmitter interrupts are enabled (FCR0 = 1, IER1 = 1), transmit interrupts will occur as follows:

1. The Transmitter Holding Register interrupt (02) occurs when the transmit FIFO is empty. It is cleared as soon as the Transmitter Holding Register is written to (1 to 16 characters may be written to the transmit FIFO while servicing this interrupt) or the IIR is read.
2. The Transmit FIFO Empty indications will be delayed 1 character time minus the last stop bit time when the following occurs: THRE = 1 and there have not been at least two bytes at the same time in the transmit FIFO since the last THRE = 1. The first transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and receiver FIFO trigger level interrupts have the same priority as the current Received Data Available interrupt; Transmit FIFO Empty has the same priority as the current Transmitter Holding Register Empty interrupt.

FIFO polled-mode operation

With FCR0 = 1, resetting IER0, IER1, IER2, IER3, or all four to 0 puts the ACE in the FIFO Polled Mode of operation. Since the receiver and transmitter are controlled separately, either one or both can be in the polled mode of operation.

In this mode, the user program will check receiver and transmitter status via the LSR. As stated previously:

1. LSR0 will be set as long as there is one byte in the receiver FIFO.
2. LSR1 through LSR4 will specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since IER2 = 0.
3. LSR5 will indicate when the transmit FIFO is empty.
4. LSR6 will indicate that both the transmit FIFO and shift registers are empty.
5. LSR7 will indicate whether there are any errors in the receiver FIFO.

There is no trigger level reached or timeout conditions indicated in the FIFO Polled Mode. However, the receiver and transmit FIFOs are still fully capable of holding characters.

PRINCIPLES OF OPERATION

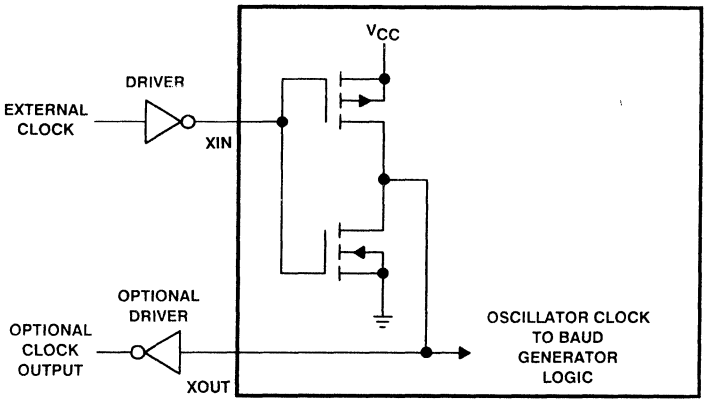
TABLE 5. BAUD RATES USING A 1.8432-MHz CRYSTAL

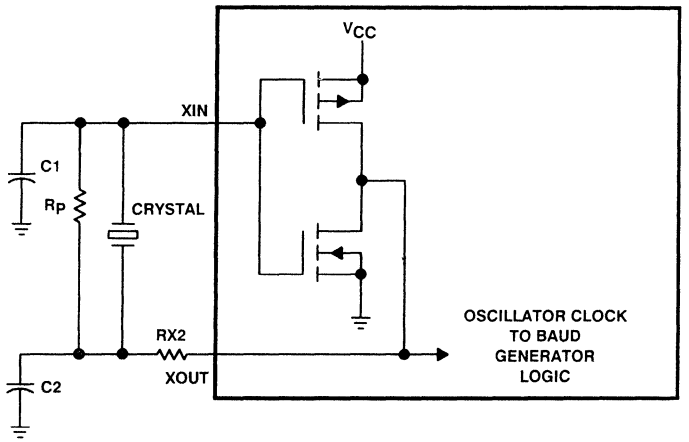
DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	2.86

TABLE 6. BAUD RATES USING A 3.072-MHz CRYSTAL

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	
75	2560	
110	1745	0.026
134.5	1428	0.034
150	1280	
300	640	
600	320	
1200	160	
1800	107	0.312
2000	96	
2400	80	
3600	53	0.628
4800	40	
7200	27	1.23
9600	20	
19200	10	
38400	5	

PRINCIPLES OF OPERATION





TYPICAL CRYSTAL OSCILLATOR NETWORK

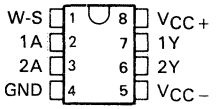
CRYSTAL	RP	RX2	C1	C2
3.1 MHz	1 MΩ	1.5 kΩ	10-30 pF	40-60 pF
1.8 MHz	1 MΩ	1.5 kΩ	10-30 pF	40-60 pF

FIGURE 16. TYPICAL CLOCK CIRCUITS

D2608, OCTOBER 1980—REVISED SEPTEMBER 1986

- **Meets EIA Standards RS-423-A and RS-232-C and Federal Standard 1030**
- **Slew Rate Control**
- **Output Short-Circuit-Current Limiting**
- **Wide Supply Voltage Range**
- **8-Pin Package**
- **Designed to Be Interchangeable With Fairchild 9636A**

D, JG, OR P PACKAGE
(TOP VIEW)

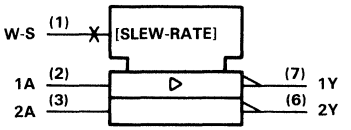


description

The uA9636AC is a dual single-ended line driver designed to meet EIA Standards RS-423-A and RS-232-C and Federal Standard 1030. The slew rates of both amplifiers are controlled by a single external resistor, R_{WS}, connected between the wave-shape-control terminal and ground. Output current limiting is provided. Inputs are compatible with TTL and CMOS and are diode-protected against negative transients. This device operates from ±12 V and is supplied in an 8-pin package.

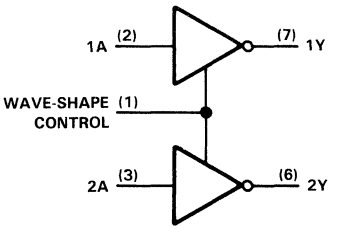
The uA9636AC is characterized for operation from 0°C to 70°C.

logic symbol†

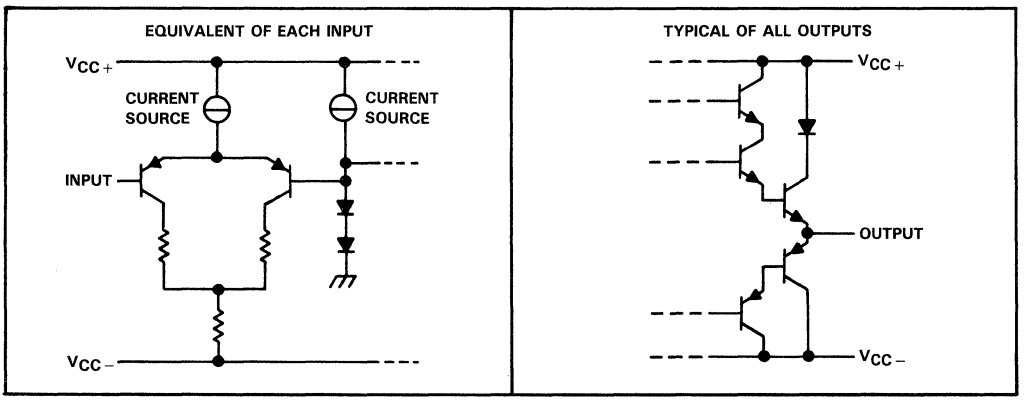


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Positive supply voltage range, V_{CC+} (see Note 1) . . . . . V_{CC-} to 15 V
Negative supply voltage range, V_{CC-} . . . . . 0.5 V to −15 V
Output voltage . . . . . ±15 V
Output current . . . . . ±150 mA
Continuous total power dissipation (see Note 2) . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P packages . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. In the JG package, uA9636AC chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW
JG	825 mW	6.6 mW/°C	528 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Positive supply voltage, V_{CC+}	10.8	12	13.2	V
Negative supply voltage, V_{CC-}	−10.8	−12	−13.2	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Wave-shaping resistor, R_{WS}	10		1000	kΩ
Operating free-air temperature, T_A	0		70	°C

TEXAS INSTRUMENTS
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electrical characteristics over recommended range of free-air temperature, supply voltage, and wave-shaping resistance (unless otherwise noted)

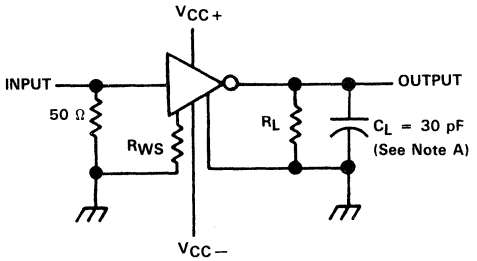
PARAMETER		TEST CONDITIONS		MIN	TYP† (See Note 3)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −15 mA			−1.1	−1.5	V
V_{OH}	High-level output voltage	V_I = 0.8 V	R_L = ∞	5	5.6	6	V
			R_L = 3 kΩ to ground	5	5.6	6	
			R_L = 450 Ω to ground	4	5.4	6	
V_{OL}	Low-level output voltage	V_I = 2 V	R_L = ∞	−6	−5.7	−5	V
			R_L = 3 kΩ to ground	−6	−5.6	−5	
			R_L = 450 Ω to ground	−6	−5.4	−4	
I_{IH}	High-level input current	V_I = 2.4 V				10	μA
		V_I = 5.5 V				100	
I_{IL}	Low-level input current	V_I = 0.4 V			−20	−80	μA
I_O	Output current (power off)	$V_{CC\pm}$ = 0,	V_O = ±6 V			±100	μA
I_{OS}	Short-circuit output current‡	V_I = 2 V		15	25	150	mA
		V_I = 0		−15	−40	−150	
r_o	Output resistance	R_L = 450 Ω			25	50	Ω
I_{CC+}	Positive supply current	V_{CC} = ±12 V, R_{WS} = 100 kΩ,	V_I = 0, Output open		13	18	mA
I_{CC-}	Negative supply current	V_{CC} = ±12 V, R_{WS} = 100 kΩ,	V_I = 0, Output open		−13	−18	mA

†All typical values are at V_{CC} ±12 V, T_A = 25°C.
‡Not more than one output should be shorted to ground at a time.
NOTE 3: The algebraic convention, in which the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for logic voltage levels, e.g., when −5 V is the maximum, the minimum is a more-negative voltage.

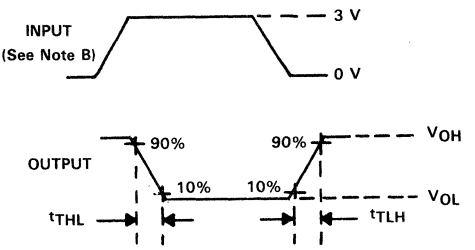
switching characteristics, $V_{CC\pm}$ = 12 V, T_A = 25°C, see Figure 1

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{TLH}	Transition time, low-to-high-level output	R_L = 450 Ω, C_L = 30 pF	R_{WS} = 10 kΩ	0.8	1.1	1.4	μs
			R_{WS} = 100 kΩ	8	11	14	
			R_{WS} = 500 kΩ	40	55	70	
			R_{WS} = 1 MΩ	80	110	140	
t_{THL}	Transition time, high-to-low-level output	R_L = 450 Ω, C_L = 30 pF	R_{WS} = 10 kΩ	0.8	1.1	1.4	μs
			R_{WS} = 100 kΩ	8	11	14	
			R_{WS} = 500 kΩ	40	55	70	
			R_{WS} = 1 mΩ	80	110	140	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50\ \Omega$, PRR ≤ 1 kHz, duty cycle = 50%.

FIGURE 1. TRANSITION TIMES

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

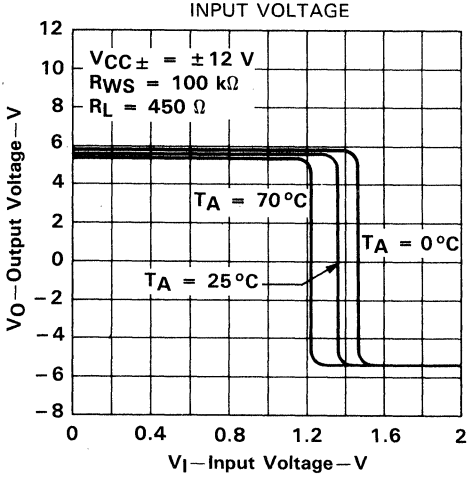


FIGURE 2

INPUT CURRENT
vs
INPUT VOLTAGE

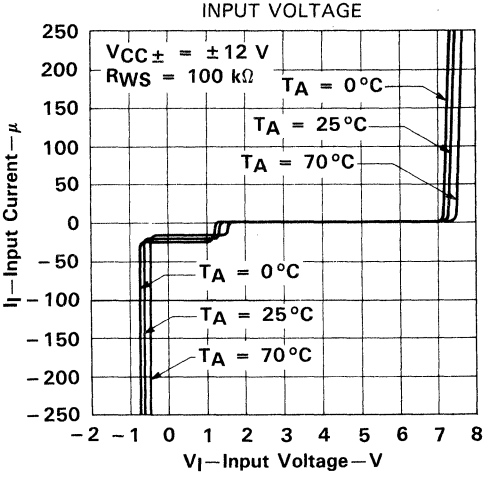


FIGURE 3

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TYPICAL CHARACTERISTICS

OUTPUT CURRENT
vs
OUTPUT VOLTAGE
(POWER ON)

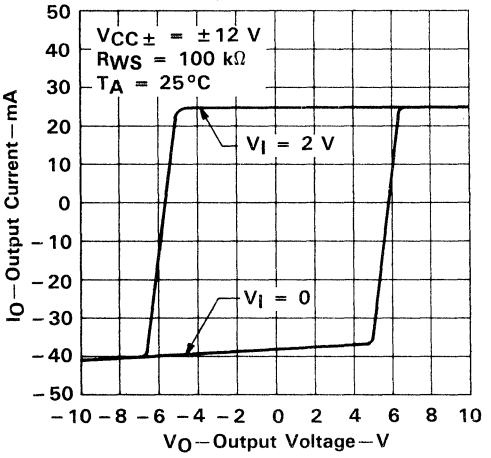

FIGURE 4

OUTPUT CURRENT
vs
OUTPUT VOLTAGE
(POWER OFF)

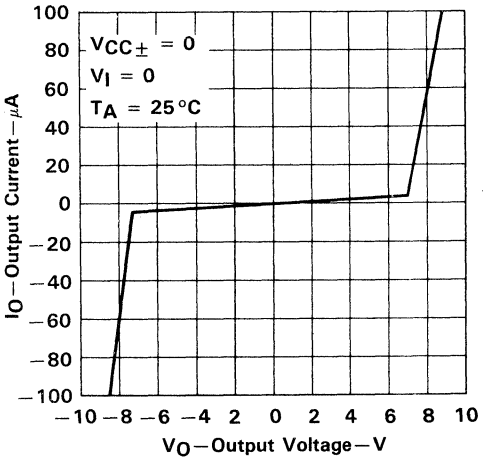

FIGURE 5

TRANSITION TIMES
vs
WAVESHAPING RESISTANCE

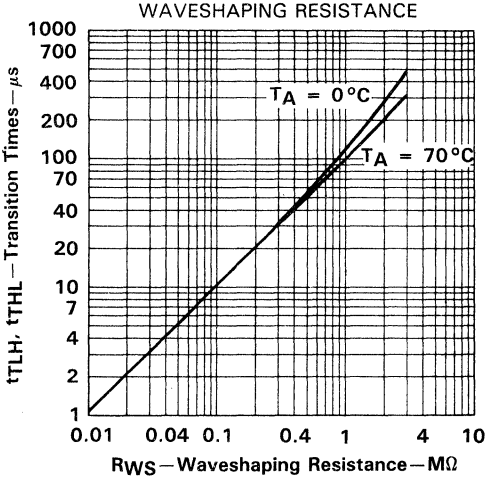

FIGURE 6

APPLICATION INFORMATION

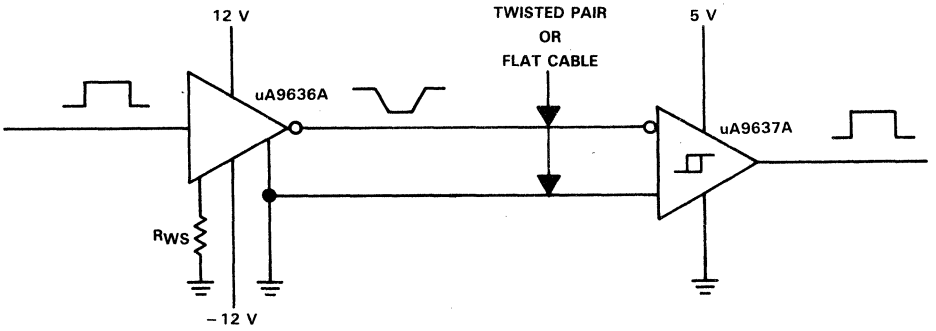

FIGURE 7. RS-423-A SYSTEM APPLICATION

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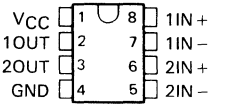
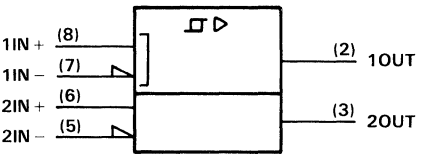
D2609, SEPTEMBER 1980—REVISED NOVEMBER 1986

- Meets EIA Standards RS-422-A and RS-423-A
- Meets Federal Standards 1020 and 1030
- Operates from Single 5-V Power Supply
- Wide Common-Mode Voltage Range
- High Input Impedance
- TTL-Compatible Outputs
- High-Speed Schottky Circuitry
- 8-Pin Dual-In-Line and "Small Outline" Packages
- Similar to SN75157 except for Corner V_{CC} and Ground Pin Positions
- Designed to Be Interchangeable with Fairchild μA9637A

uA9637M . . . JG PACKAGE
uA9637C . . . D, JG, OR P PACKAGE
(TOP VIEW)

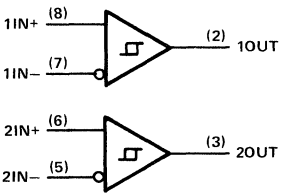


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram

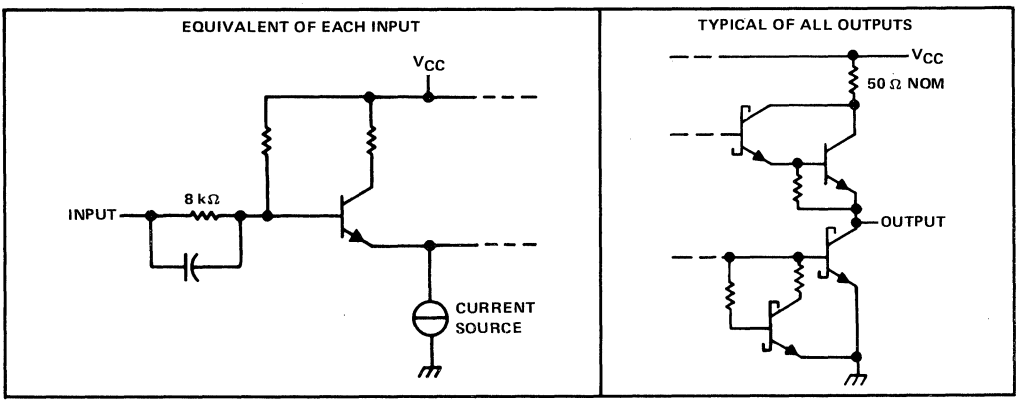


description

The uA9637AC is a dual differential line receiver designed to meet EIA standards RS-422-A and RS-423-A and Federal Standards 1020 and 1030. It utilizes Schottky circuitry and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. This device operates from a single 5-volt power supply and is supplied in an 8-pin dual-in-line package and small outline package.

The uA9637AM is characterized over the full military temperature range of −55°C to 125°C. The uA9637AC is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage . . . . . ±15 V
Differential input voltage (see Note 2) . . . . . ±15 V
Output voltage (see Note 1) . . . . . −0.5 V to 5.5 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
D package . . . . . 725 mW
JG package: uA9637AM . . . . . 1050 mW
uA9637AC . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature range: uA9637AM . . . . . −55°C to 125°C
uA9637AC . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate linearly at the following rates: 5.8 mW/°C for the D package, 8.4 mW/°C for uA9637AM in the JG package, 6.6 mW/°C for uA9637AC in the JG package, and 8.0 mW/°C for the P package.

recommended operating conditions

	uA9637AM			uA9637AC			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7			±7	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

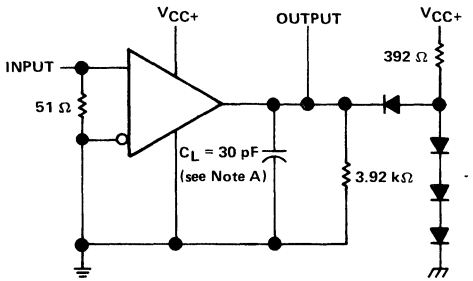
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
				See Note 4			
V_T	Threshold voltage (V_{T+} and V_{T-})	See Note 5		−0.2		0.2	V
				−0.4		0.4	
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				70		mV
V_{OH}	High-level output voltage	V_{ID} = 0.2 V,	I_O = −1 mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2 V,	I_O = 20 mA		0.35	0.5	V
I_I	Input current	V_{CC} = 0 to 5.5 V, See Note 6	V_I = 10 V		1.1	3.25	mA
			V_I = −10 V		−1.6	−3.25	
I_{OS}	Short-circuit output current‡	V_O = 0,	V_{ID} = 0.2 V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5 V,	No load		35	50	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTES: 4. The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
5. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
6. The input not under test is grounded.

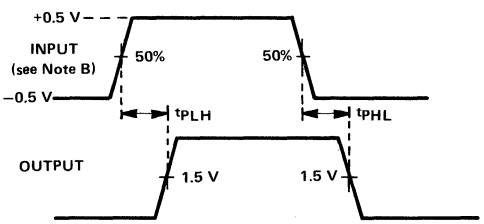
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 1		15	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			13	25	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORM

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 5 MHz, duty cycle = 50%.

FIGURE 1. TRANSITION TIMES

TYPICAL CHARACTERISTICS

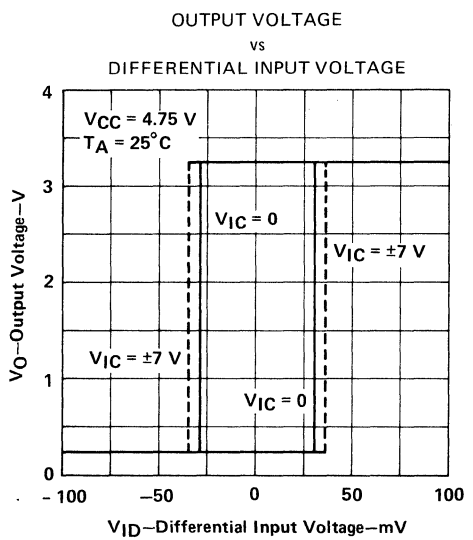


FIGURE 2

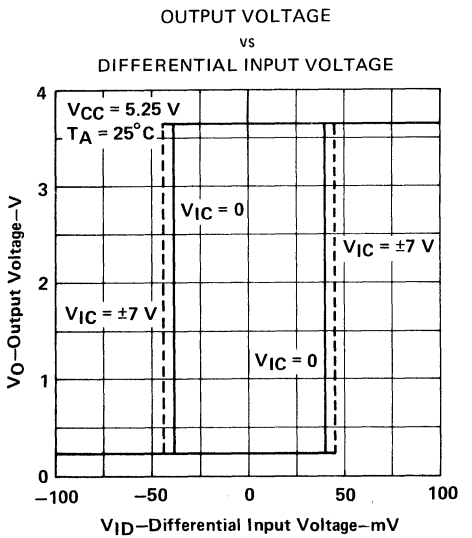


FIGURE 3

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

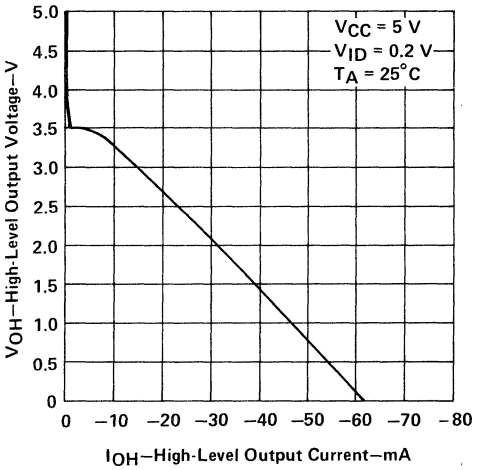


FIGURE 4

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

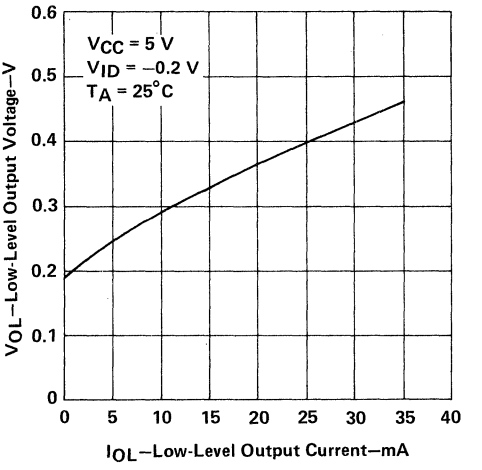


FIGURE 5

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

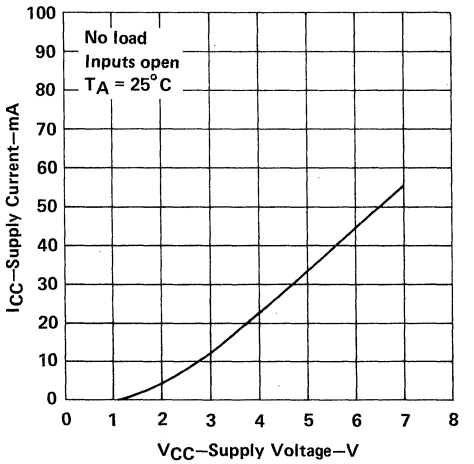


FIGURE 6

TYPICAL APPLICATION DATA

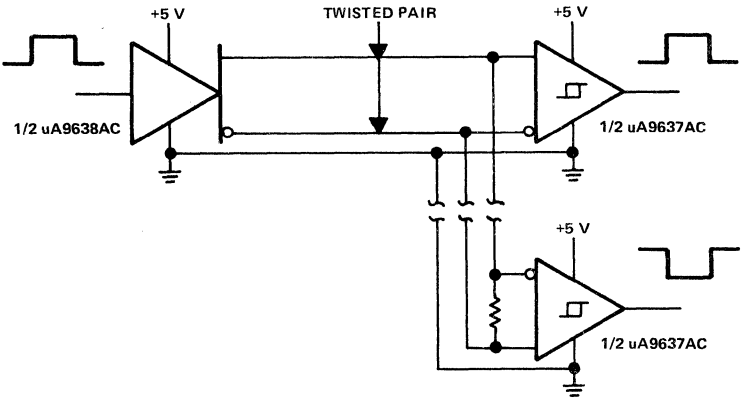
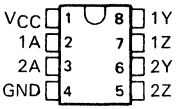


FIGURE 7. RS-422-A SYSTEM APPLICATIONS

D2612, OCTOBER 1980—REVISED SEPTEMBER 1986

- **Meets EIA Standard RS-422-A**
- **Operates From a Single 5-V Supply**
- **TTL-and CMOS-Input Compatibility**
- **Output Short-Circuit Protection**
- **Schottky Circuitry**
- **Designed to Be Interchangeable With Fairchild 9638**

D, JG, OR P PACKAGE
(TOP VIEW)

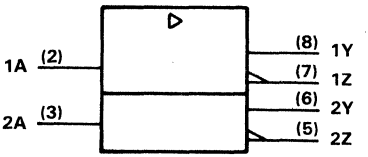


description

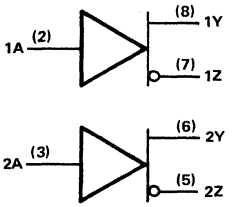
The uA9638C is a dual high-speed differential line driver designed to meet EIA Standard RS-422-A. The inputs are TTL- and CMOS-compatible and have input clamp diodes. Schottky-diode-clamped transistors are used to minimize propagation delay time. This device operates from a single 5-V power supply and is supplied in an 8-pin package.

The uA9638C is characterized for operation from 0°C to 70°C.

logic symbol†



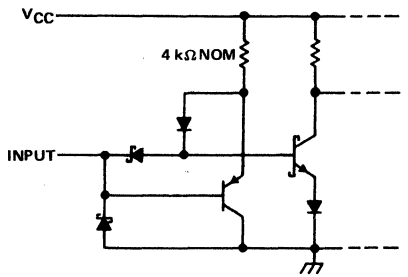
logic diagram



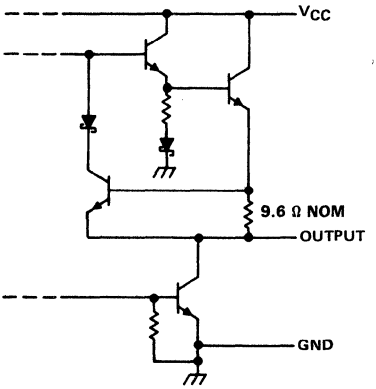
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range . . . . . −0.5 V to 7 V
Continuous total power dissipation (see Note 2) . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from 10 seconds: D and P package . . . . . 260°C

NOTES: 1. Voltage values except differential output voltages are with respect to network ground terminal.
2. In the JG package, uA9638C chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW
JG	825 mW	6.6 mW/°C	528 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−50	mA
Low-level output current, I_{OL}			50	mA
Operating free-air temperature, T_A	0		70	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −18 mA			−1	−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −10 mA	2.5	3.5		V
			I_{OH} = −40 mA	2			
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 40 mA				0.5	V
$\lvert V_{OD1} \rvert$	Differential output voltage	V_{CC} = 5.25 V, I_O = 0				$2V_{OD2}$	V
$\lvert V_{OD2} \rvert$	Differential output voltage	V_{CC} = 4.75 V to 5.25 V, R_L = 100 Ω, See Figure 1		2			V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of‡ differential output voltage					±0.4	V
V_{OC}	Common-mode output voltage§					3	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of‡ common-mode output voltage					±0.4	V
I_O	Output current with power off	V_{CC} = 0,	V_O = 6 V		0.1	100	µA
			V_O = −0.25 V		−0.1	−100	
			V_O = −0.25 V to 6 V			±100	
I_I	Input current	V_{CC} = 5.25 V, V_I = 5.5 V				50	µA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.7 V				25	µA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.5 V				−200	µA
I_{OS}	Short-circuit output current¶	V_{CC} = 5.25 V, V_O = 0		−50		−150	mA
I_{CC}	Supply current (all drivers)	V_{CC} = 5.25 V, No load,	All inputs at 0 V		45	65	mA

†All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡$\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
¶Only one output at a time should be shorted and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	C_L = 15 pF, R_L = 100 Ω, See Figure 2		10	15	ns
t_{TD}	Differential-output transition time			10	15	ns
	Skew			1		ns

PARAMETER MEASUREMENT INFORMATION

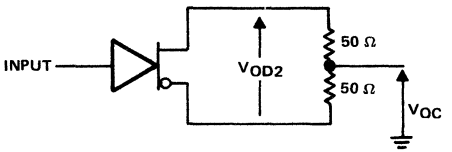
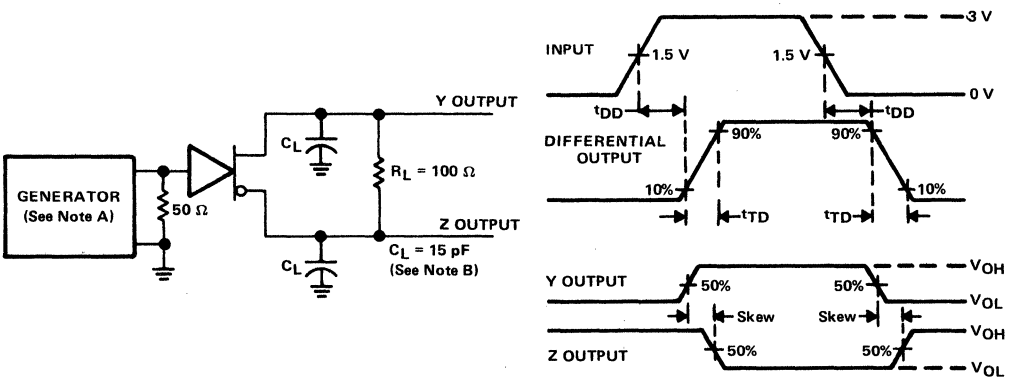


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



TEST CIRCUITS VOLTAGE WAVEFORMS

NOTES: A. The input pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_W = 100 ns, t_r = ≤ 5 ns.
B. C_L includes probe and jig capacitance.

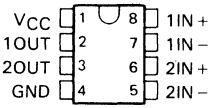
FIGURE 2. SWITCHING TIMES

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

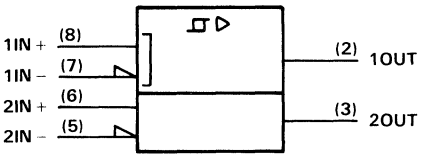
D3009, OCTOBER 1986

- Meets EIA Standards RS-422-A and RS-423-A
- Meets Federal Standards 1020 and 1030
- Operates from Single 5-V Power Supply
- Wide Common-Mode Voltage Range
- High Input Impedance
- TTL-Compatible Outputs
- High-Speed Schottky Circuitry
- 8-Pin Dual-In-Line and "Small Outline" Packages
- Designed to be Interchangeable with Fairchild μA9639AC

D, JG, OR P PACKAGE
(TOP VIEW)

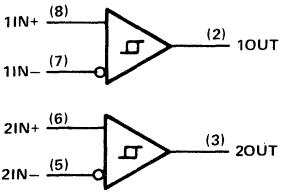


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



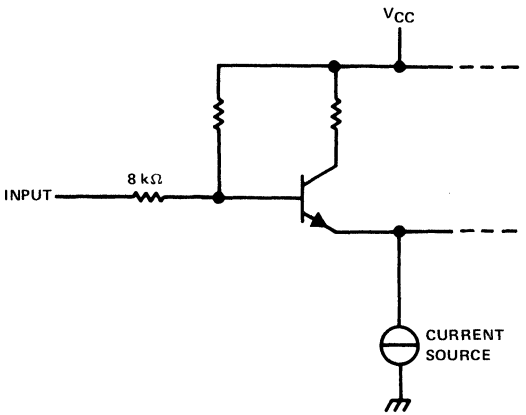
description

The uA9639C is a dual differential line receiver designed to meet EIA standards RS-422-A and RS-423-A and Federal Standards 1020 and 1030. It utilizes Schottky circuitry and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. This device operates from a single 5-volt power supply and is supplied in an 8-pin dual-in-line package and "small outline" package.

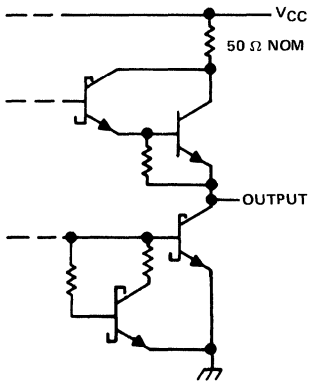
The uA9639C is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage . . . . . ±15 V
Differential input voltage (see Note 2) . . . . . ±15 V
Output voltage (see Note 1) . . . . . −0.5 V to 5.5 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
D package . . . . . 725 mW
JG package . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package . . . . . 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the D package to 464 mW at 70°C at the rate of 5.8 mW/°C, the JG package to 528 mW at 70°C at the rate of 6.6 mW/°C, and the P package to 640 mW at 70°C at the rate of 8.0 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Operating free-air temperature T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

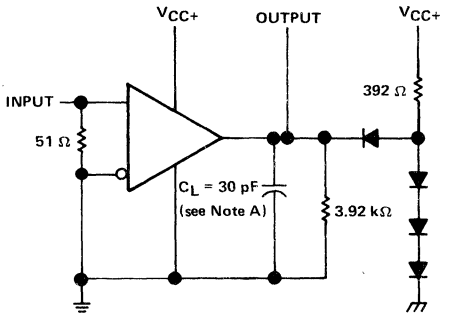
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
					See Note 4		
V_T	Threshold voltage (V_{T+} and V_{T-})			−0.2		0.2	V
		See Note 5		−0.4		0.4	
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				70		mV
V_{OH}	High-level output voltage	V_{ID} = 0.2 V,	I_O = −1 mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2 V,	I_O = 20 mA		0.35	0.5	V
I_I	Input current	V_{CC} = 0 to 5.5 V,	V_I = 10 V		1.1	3.25	mA
		See Note 6	V_I = −10 V		−1.6	−3.25	
I_{OS}	Short-circuit output current‡	V_O = 0,	V_{ID} = 0.2 V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5 V,	No load		35	50	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTES: 4. The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
5. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
6. The input not under test is grounded.

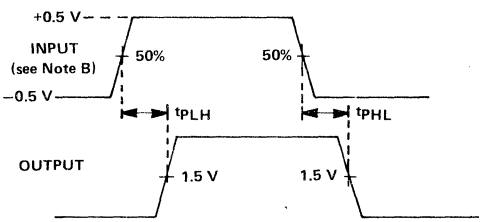
switching characteristics, V_{CC} = 5 V, T_A = 0°C to 70°C

PARAMETER		TEST CONDITION	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 1		85	ns
t_{PHL}	Propagation delay time, high-to-low-level output			85	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORM

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 5 MHz, duty cycle = 50%.

FIGURE 1. TRANSITION TIMES

TYPICAL CHARACTERISTICS

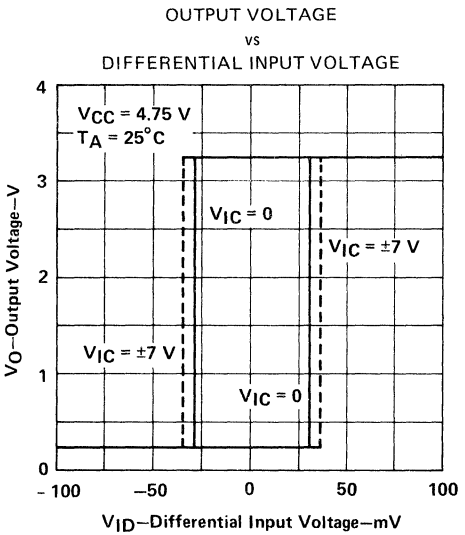


FIGURE 2

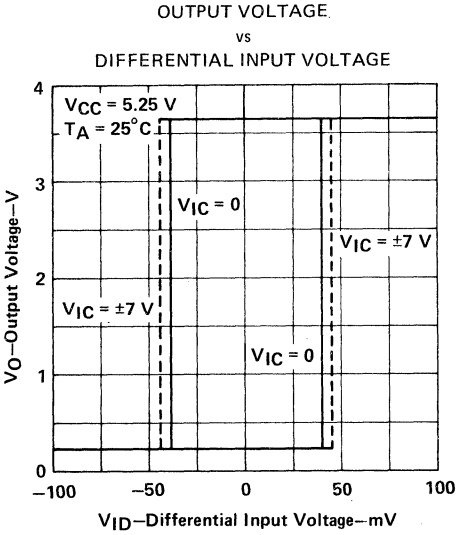


FIGURE 3

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

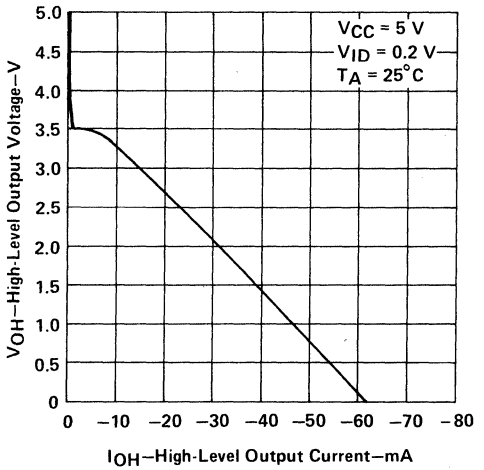


FIGURE 4

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

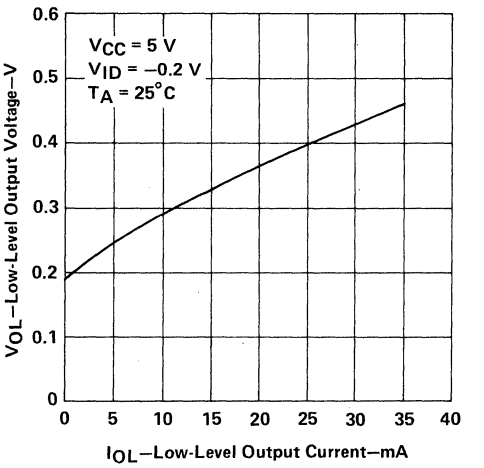


FIGURE 5

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

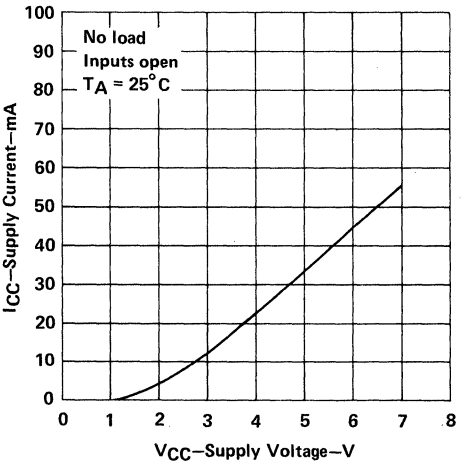


FIGURE 6

TYPICAL APPLICATION DATA

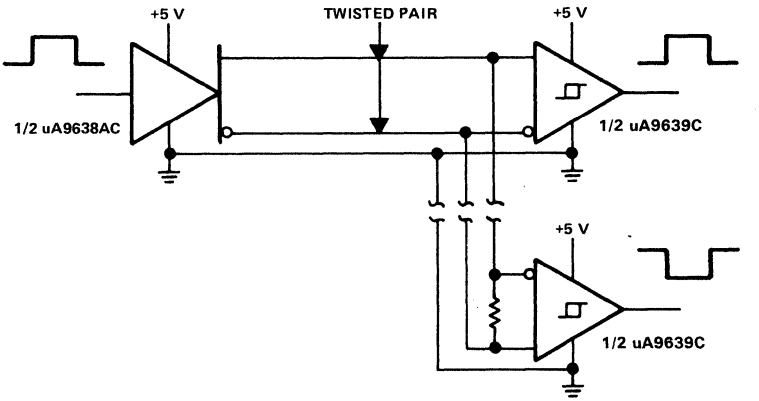


FIGURE 7. RS-422-A SYSTEM APPLICATIONS

D2471, DECEMBER 1984—REVISED MAY 1990

- **Controls 32 Electrodes**
- **100-V Totem-Pole Outputs**
- **Low Stand-by Power Consumption**
- **All Outputs Contain Sink and Source Clamp Diodes**
- **15 mA Steady-State Output Current**
- **Rugged DMOS Outputs**
- **CMOS Inputs**
- **Dependable Texas Instruments Quality and Reliability**
- **Direct Replacement for SN55500D**

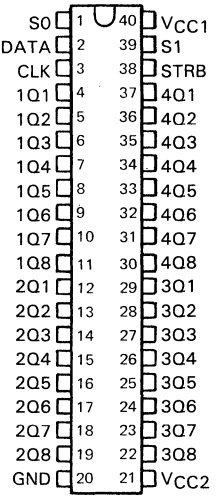
description

The SN55500E is a monolithic BIDFET† integrated circuit designed to perform the line select operation of a matrix-addressable display. The device inputs are diode-clamped CMOS inputs.

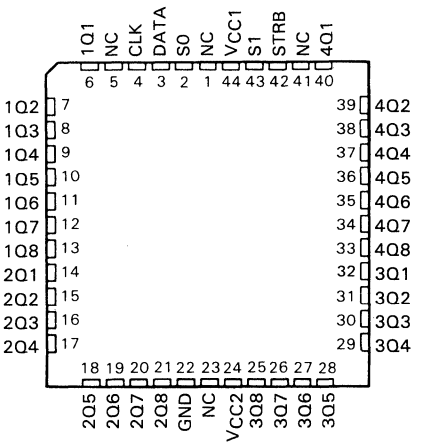
The outputs of the driver are normally low and can be selectively switched high when the strobe input is low. Selection of the outputs is achieved through the data, S0, and S1 inputs. The 8-bit data stored internally in the serial register is inverted and sent to one of four output sections by the 2-line to 4-line decoder. All other outputs remain low. Internal circuits provide a high-current pulse to the level-shifting circuit during positive output transitions. When the output transition is complete, the low steady-state current reduces the circuits standby power consumption. All outputs contain clamp diodes to the V_{CC2} and GND supply inputs.

The SN55500E is characterized for operation over the full military temperature range of −55°C to 125°C.

JD PACKAGE
(TOP VIEW)



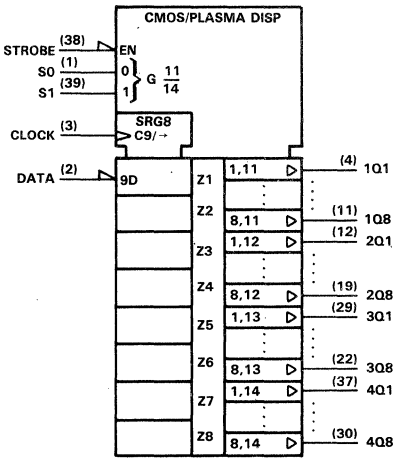
FD PACKAGE
(TOP VIEW)



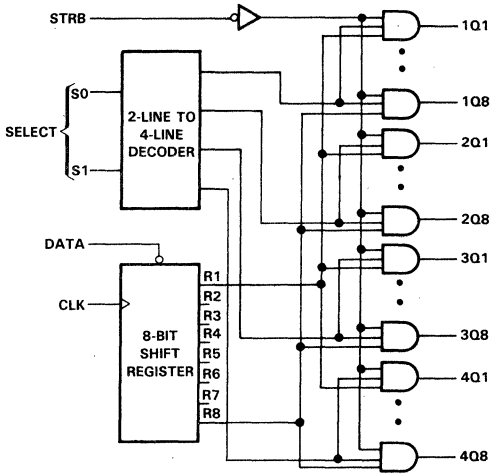
NC—No internal connection

† BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

logic symbol†



functional block diagram (positive logic)



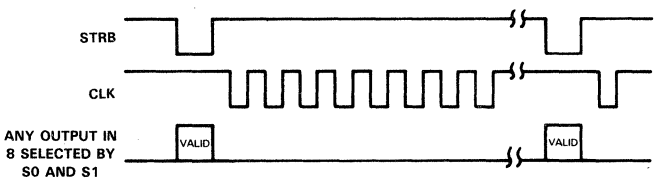
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JD package.

FUNCTION TABLE

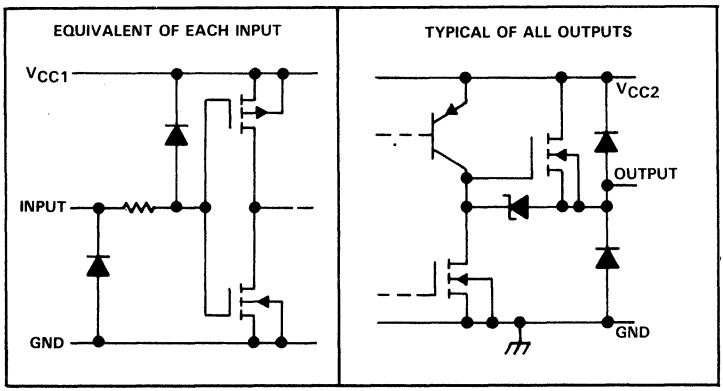
FUNCTION	INPUTS					OUTPUTS						
	DATA	CLK	SELECT		STRB	SHIFT REGISTER			1Q1 ... 1Q8	2Q1 ... 2Q8	3Q1 ... 3Q8	4Q1 ... 4Q8
			S1	S0		R1	R2	R3 ... R8				
LOAD	H	↑	X	X	H	L	$R1_n$	$R2_n$ ... $R7_n$	L ... L	L ... L	L ... L	L ... L
	L	↑	X	X	H	H	$R1_n$	$R2_n$ ... $R7_n$	L ... L	L ... L	L ... L	L ... L
STROBE	X	X	X	X	H	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	L ... L	L ... L	L ... L	L ... L
	X	H	L	L	L	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	R1 ... R8	L ... L	L ... L	L ... L
	X	H	L	H	L	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	L ... L	R1 ... R8	L ... L	L ... L
	X	H	H	L	L	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	L ... L	L ... L	R1 ... R8	L ... L
	X	H	H	H	L	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	L ... L	L ... L	L ... L	R1 ... R8

H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
R1 . . . R8 = levels currently at internal outputs of shift registers one through eight, respectively.
$R1_n$ . . . $R8_n$ = levels at outputs R1 through R8 respectively, before the most recent ↑ transition of the clock.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 13.8 V
Supply voltage, V_{CC2} . . . . . 100 V
Input voltage . . . . . V_{CC1} +0.3 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1825 mW
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FD package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JD package . . . . . 300°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, see Dissipation Rating Table.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
FD	1825 mW	14.6 mW/°C	25°C
JD	1825 mW	22 mW/°C	67°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	13.2	V
Supply voltage, V_{CC2}		0		100	V
High-level input voltage, V_{IH}, as a percentage of V_{CC1}		75%			
Low-level input voltage, V_{IL}, as a percentage of V_{CC1}				25%	
High-level output clamp current				20	mA
Low-level output clamp current				−20	mA
Clock frequency, f_{clock} (see Figure 2)		0		8	MHz
Duration of high or low clock pulse, t_w		62			ns
Setup time, t_{su}	Data inputs before clock↑	20			ns
	Select inputs before strobe↓	50			
Hold time, t_h	Data inputs after clock↑ (see Note 3)	50			ns
	Strobe input high after clock↑	50			
	Select inputs after strobe↑	50			
Operating free-air temperature, T_A		−55			°C
Operating case temperature, T_C				125	°C

NOTE 3: For operation above 25°C junction temperature, refer to Figure 2.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

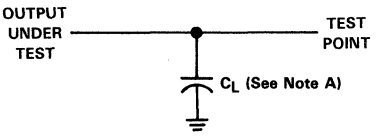
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC1} = 12 V,	I_I = −12 mA		−1	−1.5	V
V_{OH}	High-level output voltage	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OH} = −1 mA	94	97.5		V
			I_{OH} = −10 mA	92	94.5		
			I_{OH} = −15 mA	90	93.5		
V_{OL}	Low-level output voltage	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OL} = 1 mA		0.85	2	V
			I_{OL} = 10 mA		2	4	
			I_{OL} = 15 mA		2.75	5	
V_{OK}	Output clamp voltage	V_{CC2} = 0	I_O = 20 mA		1	2.5	V
			I_O = −20 mA		−1.2	−2.5	
I_{IH}	High-level input current	V_{CC1} = 13.2 V,	V_I = V_{IH} min			1	μA
I_{IL}	Low-level input current	V_{CC1} = 13.2 V,	V_I = V_{IL} max			−1	μA
I_{CC1}	Supply current	V_{CC1} = 13.2 V,	V_{CC2} = 100 V		0.05	1	mA
I_{CC2}	Supply current	V_{CC2} = 100 V			1	5	mA

†All typical values are at V_{CC} = 12 V, T_A = 25°C.

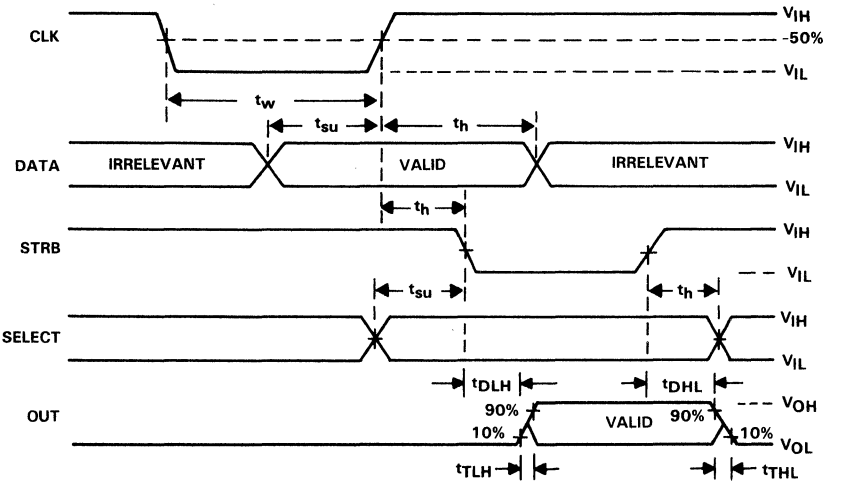
switching characteristics, V_{CC1} = 12 V, V_{CC2} = 100 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output from strobe input	C_L = 30 pF, See Figure 1		250	ns
t_{DLH}	Delay time, low-to-high-level output from strobe input			450	ns
t_{THL}	Transition time, high-to-low-level output			200	ns
t_{TLH}	Transition time, low-to-high-level output			300	ns

PARAMETER MEASUREMENT INFORMATION



LOAD TEST CIRCUIT

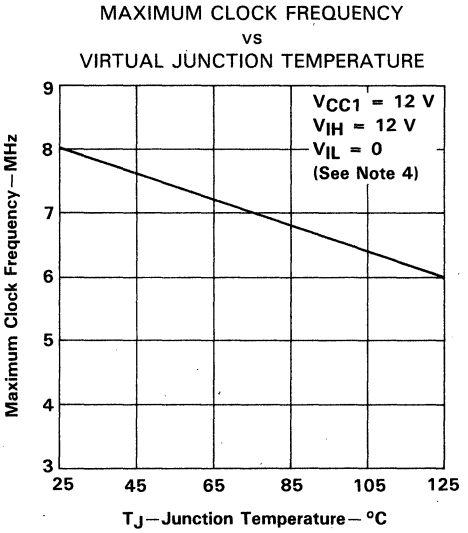


VOLTAGE WAVEFORMS

NOTE A. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS



NOTE 4: This curve assumes a symmetrical clock pulse.

FIGURE 2

THERMAL INFORMATION

junction temperature formula

$$T_J = T_A + P_D R_{\theta JA}$$
$$T_J = T_C + P_D R_{\theta JC}$$

where

T_J = virtual junction temperature
T_A = free-air temperature
P_D = average device power dissipation
R_θ = thermal resistance (junction-to-air, $R_{\theta JA}$, or junction-to-case, $R_{\theta JC}$)

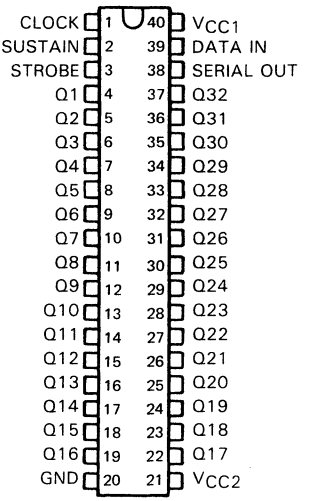
PACKAGE TYPE	$R_{\theta JA}$	$R_{\theta JC}$
FD 44-pin ceramic	68 °C/W	20 °C/W
JD 40-pin ceramic	45 °C/W	12 °C/W

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D2472, APRIL 1986—REVISED DECEMBER 1989

- **Controls 32 Electrodes**
- **100-V Totem-Pole Outputs**
- **Low Stand-by Power Consumption**
- **All Outputs Contain Sink and Source Clamp Diodes**
- **15-mA Steady-State Output Current**
- **Rugged DMOS Outputs**
- **CMOS Inputs**
- **Direct Replacement for SN55501C, SN55501D**

J PACKAGE
(TOP VIEW)



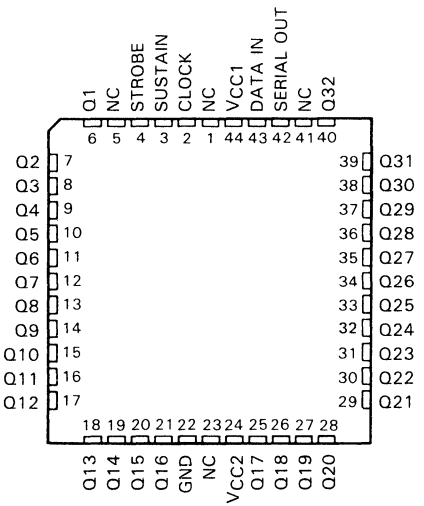
description

The SN55501E is a monolithic BIDFET† integrated circuit designed to provide the serial-to-parallel conversion and level translation of data in a matrix-addressable display. This device has diode-clamped CMOS inputs.

The Q outputs of these drivers are normally high and can be switched either selectively or together. Any output whose associated register bit (in the internal 32-bit serial register) contains a low will switch low when STROBE is low if SUSTAIN is high. All other outputs remain high. When SUSTAIN is switched low, all outputs switch low independently of the data or strobe inputs. This feature can be used to generate a portion of the SUSTAIN pulse required in the operation of an ac plasma display. The internal level-shift circuits provide additional drive during the times that the outputs switch high to facilitate fast rise times while maintaining low stand-by power consumption. All outputs contain clamp diodes to the V_{CC2} and GND supply inputs.

The SN55501E is characterized for operation over the full military temperature range of −55°C to 125°C.

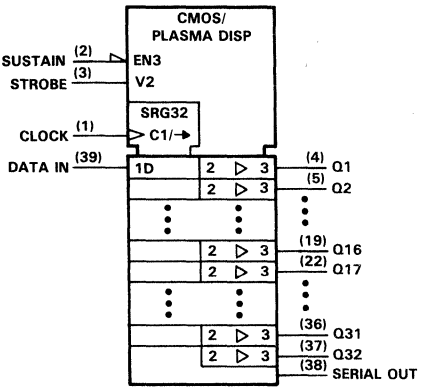
FD OR FJ PACKAGE
(TOP VIEW)



NC—No internal connection

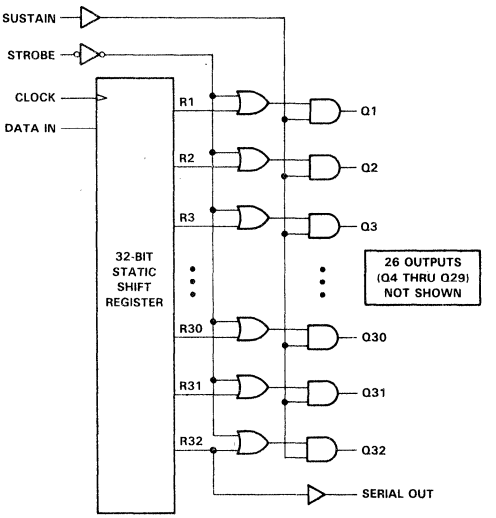
†BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J package.

functional block diagram (positive logic)

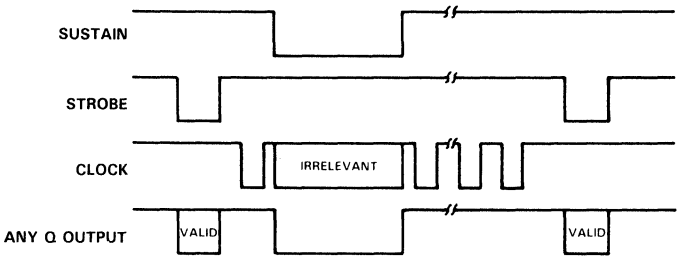


FUNCTION TABLE

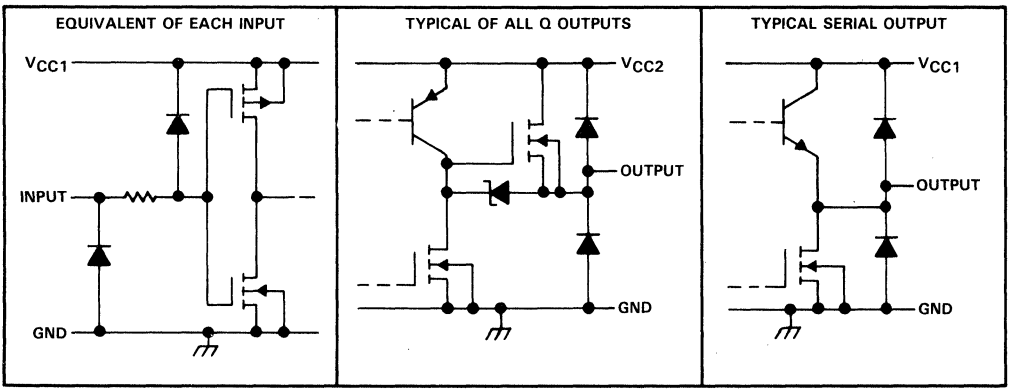
FUNCTION	INPUTS				OUTPUTS						
	DATA	CLOCK	STROBE	SUSTAIN	SHIFT REGISTER R1	SHIFT REGISTER R2	SHIFT REGISTER R3...R32	SERIAL DATA	Q1	Q2	Q3....Q32
LOAD	H	↑	H	H	H	$R1_n$	$R2_n$...$R31_n$	$R32_n$	H	H	H....H
	L	↑	H	H	L	$R1_n$	$R2_n$...$R31_n$	$R32_n$	H	H	H....H
STROBE	X	X	H	H	$R1_n$	$R2_n$	$R3_n$...$R32_n$	$R32_n$	H	H	H....H
	X	H	L	H	$R1_n$	$R2_n$	$R3_n$...$R32_n$	$R32_n$	R1	R2	R3 ....R32
SUSTAIN	X	X	X	L	$R1_n$	$R2_n$	$R3_n$...$R32_n$	$R32_n$	L	L	L L

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
R1...R32 = levels currently at internal outputs of shift registers one through thirty-two, respectively.
$R1_n$...$R32_n$ = levels at shift-register outputs R1 through R32 respectively, before the most recent ↑ transition at the CLOCK input.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 100 V
Input voltage . . . . . V_{CC1} + 0.3 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FD or FJ package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 125°C$ POWER RATING
FD or FJ	1825 mW	14.6 mW/°C	25°C	365 mW
J	1825 mW	22.0 mW/°C	67°C	550 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	13.2	V
Supply voltage, V_{CC2}		0		100	V
High-level input voltage, V_{IH}		0.75 V_{CC1}			
Low-level input voltage, V_{IL}				0.25 V_{CC1}	
Peak high-level Q output current, I_{OH}				−20	mA
Peak low-level Q output current, I_{OL}				20	mA
High-level Q output clamp current, I_{OKH}				20	mA
Low-level Q output clamp current, I_{OKL}				−20	mA
Clock frequency, f_{clock}, at or below, 25°C junction temperature (see Note 2)		0		8	MHz
Duration of high or low clock pulse, t_w		62			ns
Setup time, t_{su}	Data inputs before CLOCK↑	20			ns
Hold time, t_h	Data hold time after CLOCK↑	50			ns
	STROBE high after CLOCK↑	150			
	STROBE high after SUSTAIN↑	250			
Operating free-air temperature, T_A		−55		125	°C
Operating case temperature, T_C				125	

NOTE 2: See Figure 3 for maximum clock frequency when devices are operated in cascade or for operation above T_J = 25°C.

electrical characteristics over recommended operating temperature range

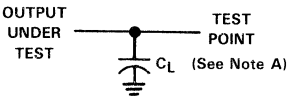
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		V_{CC1} = 12 V,	I_I = 12 mA		−1	−1.5	V
V_{OH}	High-level output voltage	Q outputs	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OH} = −1 mA	94	97.5		V
				I_{OH} = −10 mA	92	94.5		
				I_{OH} = −15 mA	90	93.5		
		SERIAL OUT	V_{CC1} = 10.8 V,	I_{OH} = −100 μA	9	10		
V_{OL}	Low-level output voltage	Q outputs	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OL} = 1 mA		0.85	2	V
				I_{OL} = 10 mA		2	4	
				I_{OL} = 15 mA		2.75	5	
		SERIAL OUT	V_{CC1} = 10.8 V,	I_{OL} = 100 μA		0.1	1	
V_{OK}	Output clamp voltage	Q outputs	V_{CC2} = 0	I_{OK} = 20 mA		1	2.5	V
				I_{OK} = −20 mA		−1.2	−2.5	
I_{IH}	High-level input current		V_{CC1} = 13.2 V, V_{CC2} = 100 V	V_{IH} = V_{IH}min,			1	μA
I_{IL}	Low-level input current		V_{CC1} = 13.2 V, V_{CC2} = 100 V	V_{IL} = V_{IL}max,			−1	μA
I_{CC1}	Supply current from V_{CC1}		V_{CC1} = 13.2 V,	V_{CC2} = 100 V‡		0.05	1	mA
I_{CC2}	Supply current from V_{CC2}		V_{CC1} = 13.2 V, V_{CC2} = 100 V	Outputs low		0.1	1	mA
				Outputs high		1	5	

†Typical values are at V_{CC1} = 12 V, T_A = 25°C.
‡Measure with inputs at V_{CC1} and again with inputs at GND.

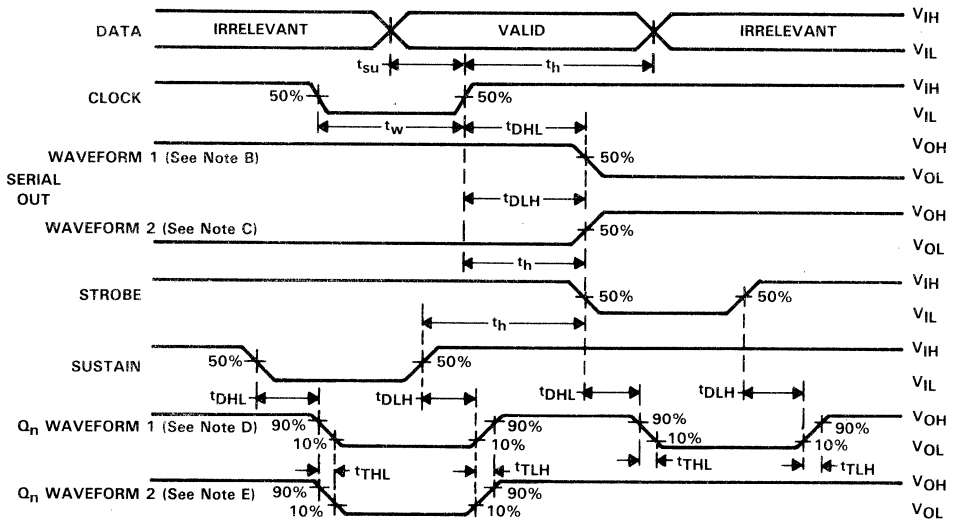
switching characteristics, V_{CC1} = 12 V, V_{CC2} = 100 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level outputs	STROBE to Q outputs	C_L = 30 pF			250	ns
		SUSTAIN to Q outputs	C_L = 30 pF			250	
		CLOCK to SERIAL OUT	C_L = 20 pF			147	
t_{DLH}	Delay time, low-to-high-level outputs	STROBE to Q outputs	C_L = 30 pF			450	ns
		SUSTAIN to Q outputs	C_L = 30 pF			450	
		CLOCK to SERIAL OUT	C_L = 20 pF			147	
t_{THL}	Transition time, high-to-low-level Q output		C_L = 30 pF			200	ns
t_{TLH}	Transition time, low-to-high-level Q output		C_L = 30 pF			300	ns

PARAMETER MEASUREMENT INFORMATION



LOAD TEST CIRCUIT



NOTES: A. C_L includes probe and jig capacitance.
B. Serial out waveform for internal conditions such that a low is registered in R32.
C. Serial out waveform for internal conditions such that a high is registered in R32.
D. Q_n output with a low stored in associated register R_n.
E. Q_n output with a high stored in associated register R_n.

VOLTAGE WAVEFORMS

FIGURE 1. SWITCHING CHARACTERISTICS

RECOMMENDED OPERATING CONDITIONS

MAXIMUM CLOCK FREQUENCY
vs
JUNCTION TEMPERATURE

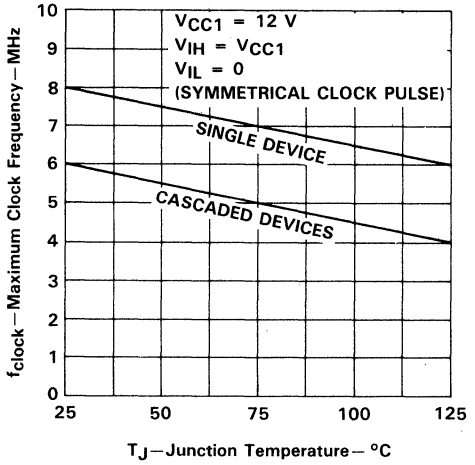


FIGURE 2

INPUT VOLTAGE LOGIC LEVEL LIMITS
vs
V_{CC1} SUPPLY VOLTAGE

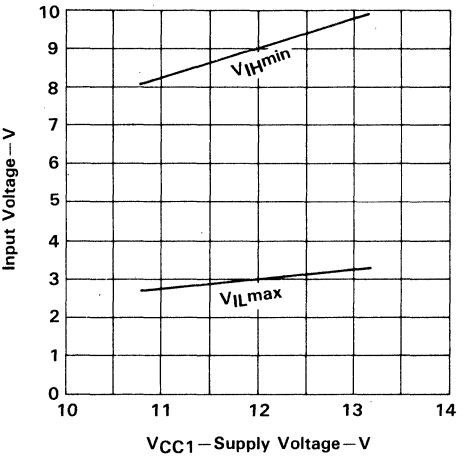


FIGURE 3

THERMAL CHARACTERISTICS

junction temperature formula

$$T_J = T_A + P_D R_\theta$$

where

T_J = virtual junction temperature
T_A = free-air temperature
P_D = average device power dissipation
R_θ = thermal resistance (junction-to-air, $R_{\theta JA}$, or junction-to-case, $R_{\theta JC}$)

PACKAGE	$R_{\theta JA}$	$R_{\theta JC}$
FD or FJ	68°C/W	20°C/W
J	45°C/W	12°C/W

D2743, APRIL 1986

- **Each Device Drives 32 Electrodes**
- **High-Voltage Open-Drain DMOS Outputs**
- **50-mA Output Current Capability**
- **CMOS-Compatible Inputs**
- **Very Low Steady-State Power Consumption**

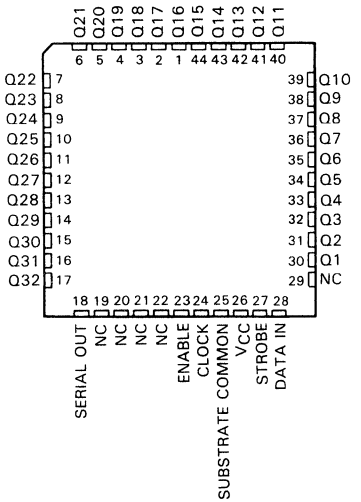
description

The SN55551 and SN55552 are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS-compatible and all outputs are high-voltage open-drain DMOS transistors. The SN55552 output sequence has been reversed from the SN55551 for ease in printed circuit board layout.

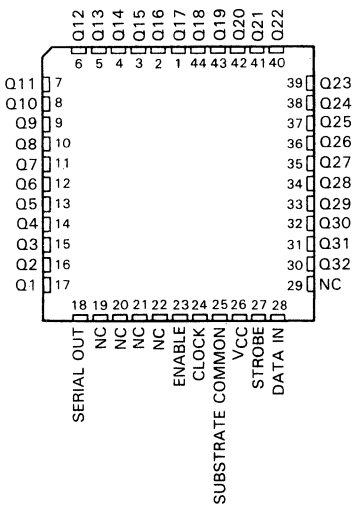
The devices consist of a 32-bit shift register, 32 AND gates, and 32 output OR gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to the Substrate Common terminal. Serial data is entered into the shift register on the high-to-low transition of the clock input. A high Enable input allows those outputs with a high in their associated register to be turned on causing the corresponding row to be connected to the composite row drive signal. When the Strobe input is low, all output transistors are turned on. The Serial Data output from the shift register may be used to cascade additional devices. This output is not affected by the Enable or Strobe inputs.

The SN55551 and SN55552 are characterized for operation over the full military temperature range of −55°C to 125°C.

SN55551 . . . FD PACKAGE
(TOP VIEW)



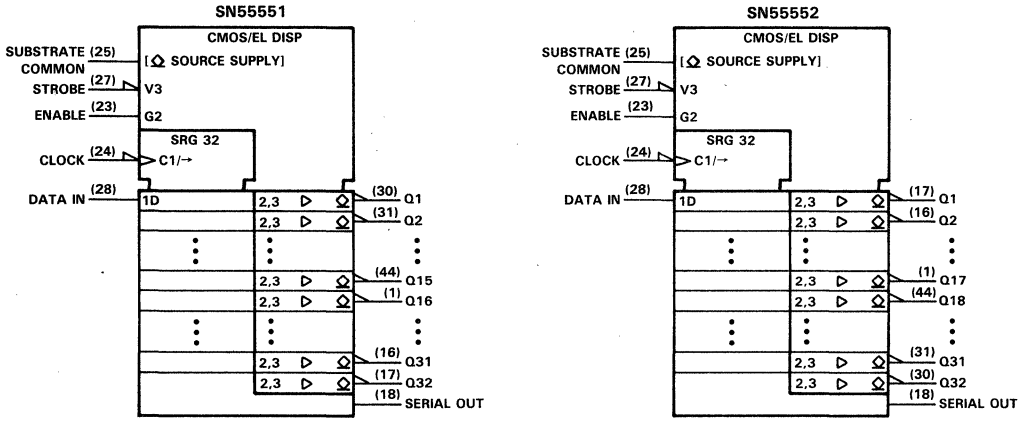
SN55552 . . . FD PACKAGE
(TOP VIEW)



NC—No internal connection

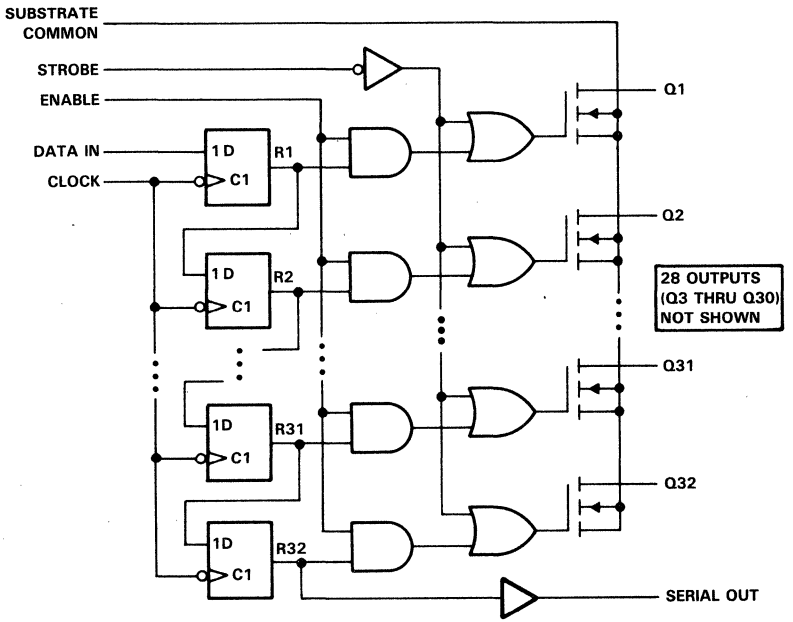
†BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. The symbol ◇ here indicates an n-channel open-drain output.

logic diagram (positive logic)

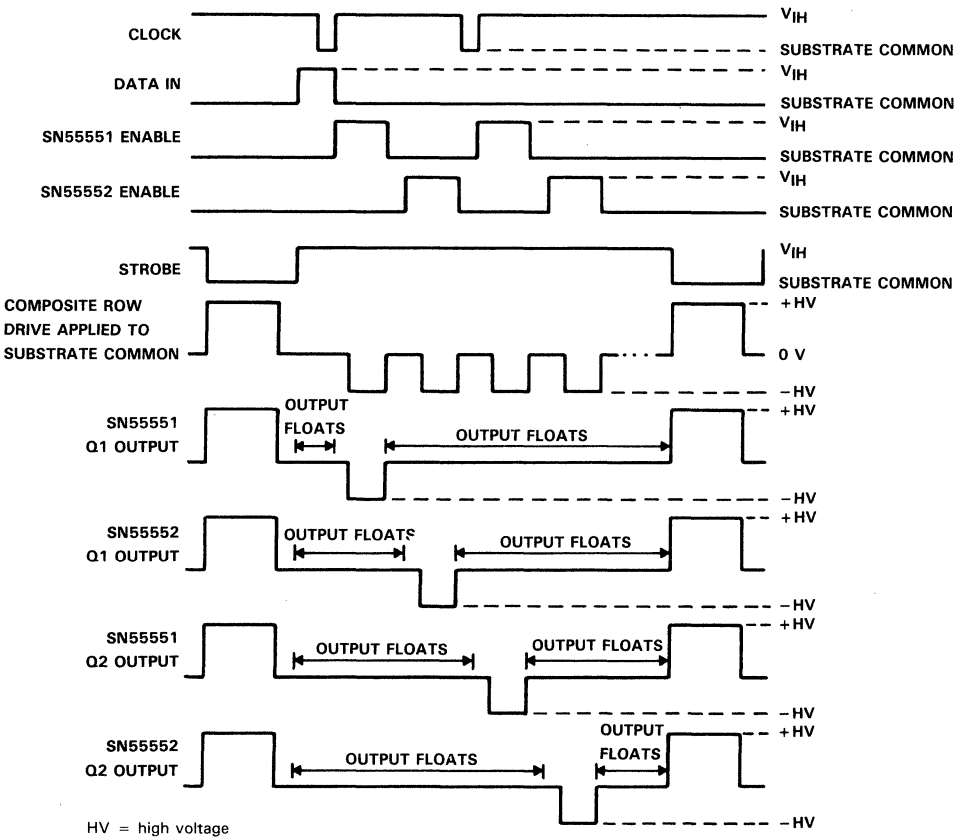


FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R32	OUTPUTS	
	CLOCK	ENABLE	STROBE		SERIAL	Q1 THRU Q32
LOAD	↓	X	X	Load and Shift†	R32	Determined by Enable and Strobe
	No. ↓	X	X	No Change	R32	Determined by Enable and Strobe
ENABLE	X	L	H	As determined above	R32	All Q outputs off
	X	H	H	As determined above	R32	Determined by R1 through R32
STROBE	X	X	L	As determined above	R32	All Q outputs on

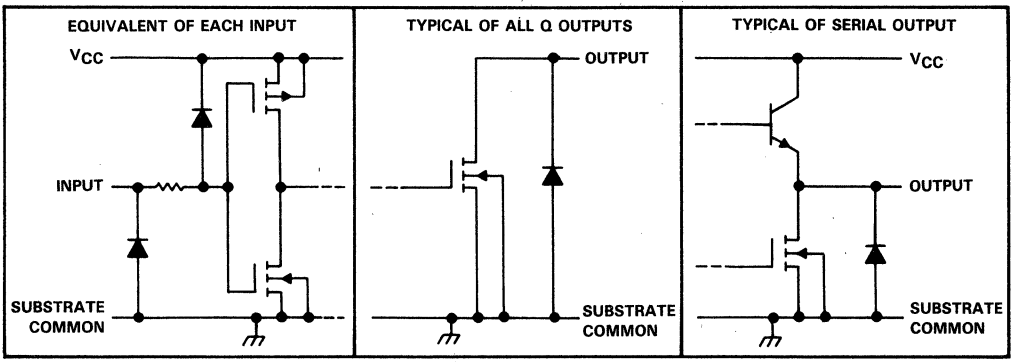
H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition.
†Register R32 takes on the state of R31, R31 takes on the state of R30,. . .R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



NOTE: During operation Clock, Data In, Enable, and Strobe are referenced to the Composite Row Drive signal received at the Substrate Common pin of the device.

schematic of inputs and outputs



absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Q off-state output voltage, $V_{O(off)}$ . . . . . 225 V
Input voltage . . . . . V_{CC} + 0.3 V
Substrate common terminal current (see Note 2) . . . . . 1.5 A
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 1825 mW
Minimum operating free-air temperature . . . . . −55°C
Operating case temperature . . . . . 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to substrate common terminal.
2. Duty cycle is limited by package dissipation.
3. For operation above 25°C free-air temperature, derate linearly at the rate of 14.6 mW/°C.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			10.8	12	15	V
$V_{O(off)}$	Off-state Q output voltage			0		200	V
V_{IH}	High-level input voltage			0.75V_{CC}		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			−0.3		0.25V_{CC}	V
$I_{O(on)}$	On-state Q output current	V_{DD} = 80 V, Duty cycle ≤ 1%	V_{CC} = 10.8 V, T_C = 25°C			50	mA
			V_{CC} = 15 V, T_C = 25°C			80	
f_{clock}	Clock frequency, T_A = 25°C					6.25	MHz
t_w	Clock pulse duration, high or low, T_A = 25°C			80			ns
t_{su}	Setup time, data valid before clock↓, T_A = 25°C			20			ns
t_h	Hold time, data valid after clock↓, T_A = 25°C			110			ns
T_A	Operating free-air temperature			−55			°C
T_C	Operating case temperature					125	°C

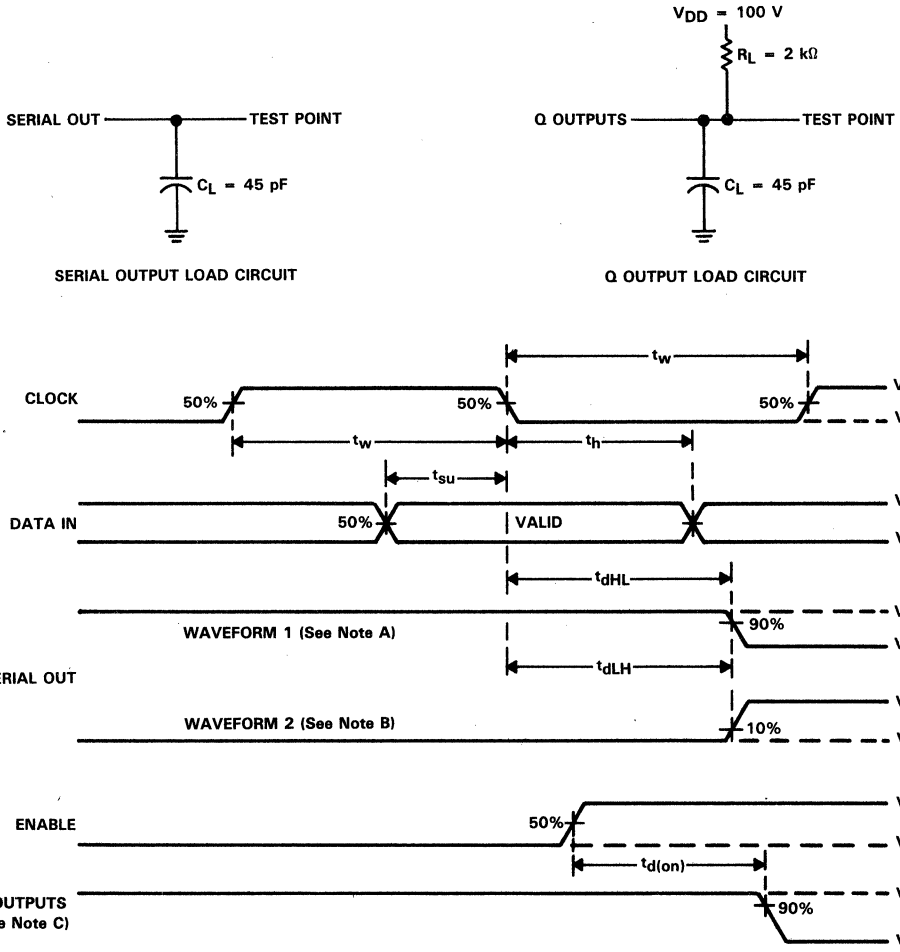
electrical characteristics over recommended operating temperature range, V_{CC} = 12 V, substrate common at 0 V

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Serial outputs	I_O = −100 μA	10		V
V_{OL}	Low-level output voltage	Q outputs	I_O = 50 mA		50	V
		Serial output	I_O = 100 μA		1.5	
I_{IH}	High-level input current		V_I = 12 V		5	μA
I_{IL}	Low-level input current		V_I = 0		−5	μA
$I_{O(off)}$	Off-state Q output current		V_O = 200 V		50	μA
I_{CC}	Supply current				500	μA

switching characteristics, V_{CC} = 12 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{dLH}	Delay time, clock↓ to serial↓	C_L = 45 pF to common, See Figure 1		200	ns
t_{dHL}	Delay time, clock↓ to serial↑			200	ns
t_{dHL}	Delay time, enable to Q output↓	V_{DD} = 100 V, R_L = 2 kΩ, C_L = 45 pF to common, See Figure 1		500	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Waveform 1 is for internal conditions such that a low is clocked into R32.
B. Waveform 2 is for internal conditions such that a high is clocked into R32.
C. To measure $t_{d(on)}$, a high is stored in the associated register.

FIGURE 1. SWITCHING CHARACTERISTICS

RECOMMENDED OPERATING CONDITIONS

MAXIMUM ON-STATE Q OUTPUT CURRENT
vs
SUPPLY VOLTAGE

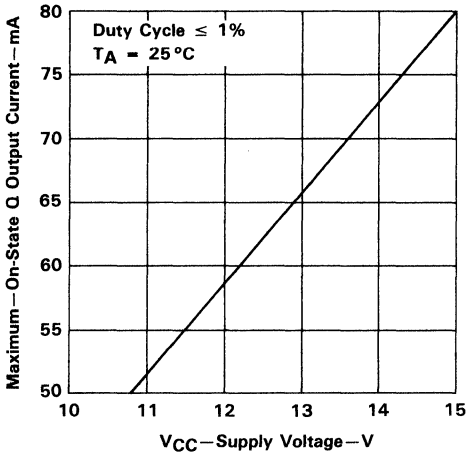


FIGURE 2

TYPICAL CHARACTERISTICS

OUTPUT CHARACTERISTICS SHOWING
SAFE OPERATION AREA (SOA)

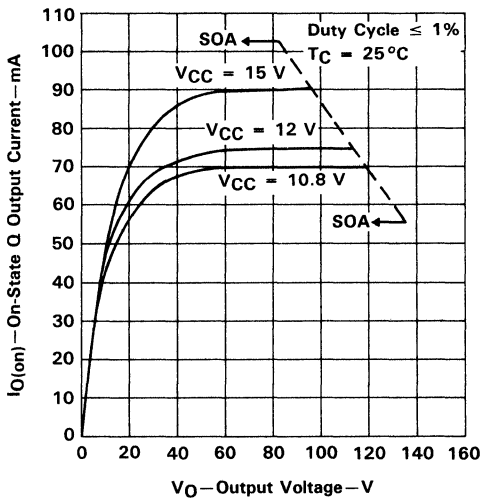


FIGURE 3

OUTPUT SATURATION CURRENT
vs
JUNCTION TEMPERATURE

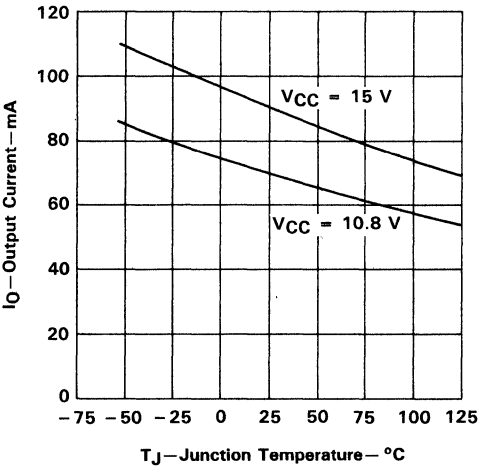


FIGURE 4

D2744, APRIL 1986

- **Each Device Drives 32 Electrodes**
- **60-V Output Voltage Swing Capability**
- **15-mA Output Source and Sink Current Capability**
- **High-Speed Serially-Shifted Data Input**
- **Totem-Pole Outputs**
- **Latches on All Driver Outputs**

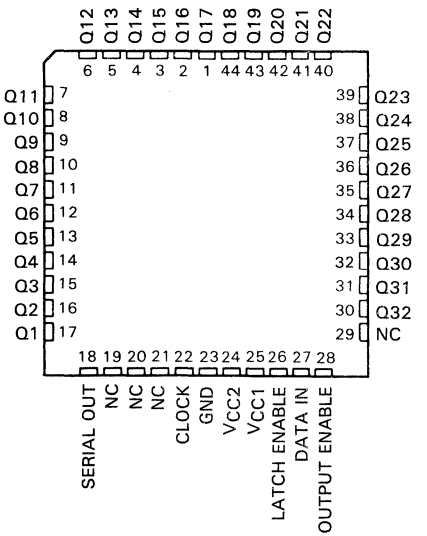
description

The SN55553 and SN55554 are monolithic BIDFET† integrated circuits designed to drive the column electrodes of an electroluminescent display. The SN55554 output sequence has been reversed from the SN55553 for ease in printed circuit board layout.

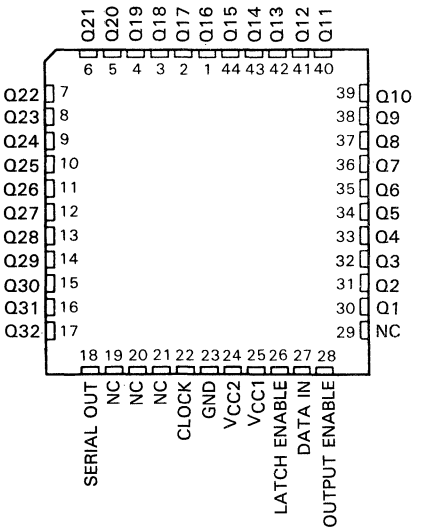
The devices consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of the clock input. When high, the Latch Enable input transfers the shift register contents to the outputs of the 32 latches. When Output Enable is high, all Q outputs are enabled. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the Latch Enable or Output Enable inputs.

The SN55553 and SN55554 are characterized for operation over the full military temperature range of −55°C to 125°C.

SN55553 . . . FD PACKAGE
(TOP VIEW)



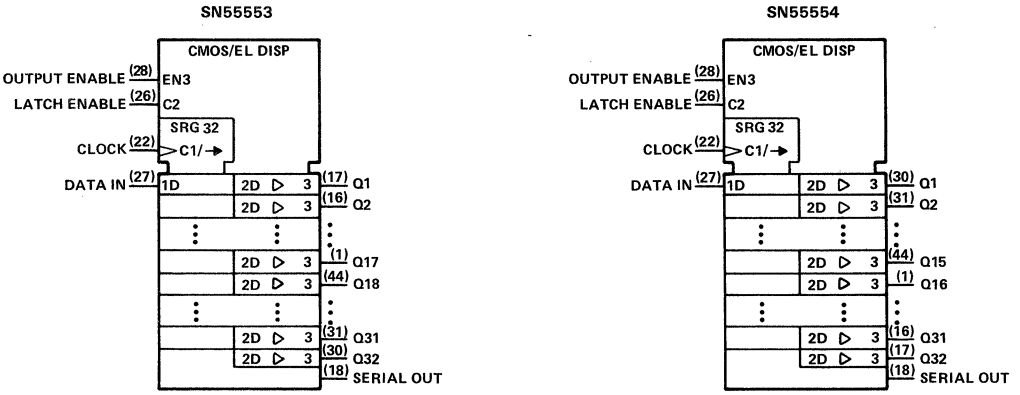
SN55554 . . . FD PACKAGE
(TOP VIEW)



NC—No internal connection

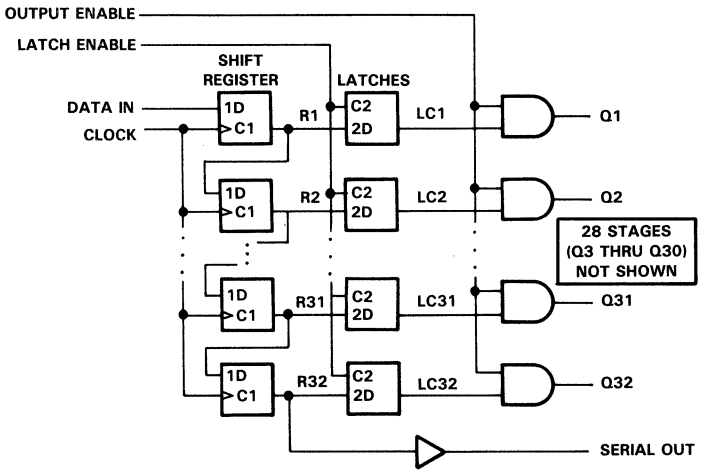
†BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

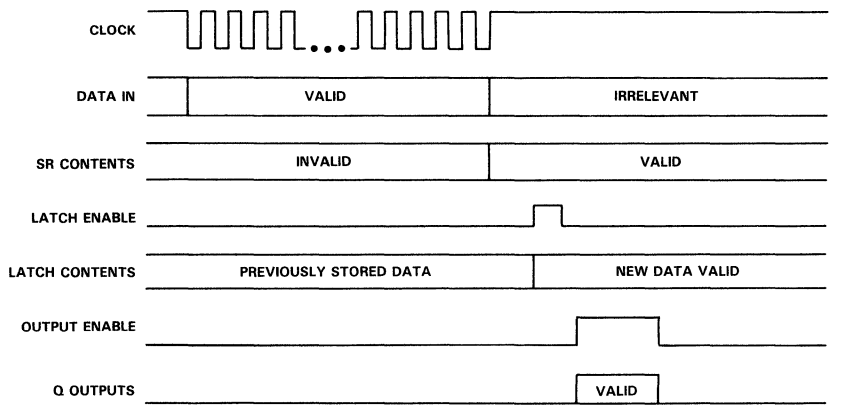


FUNCTION TABLE

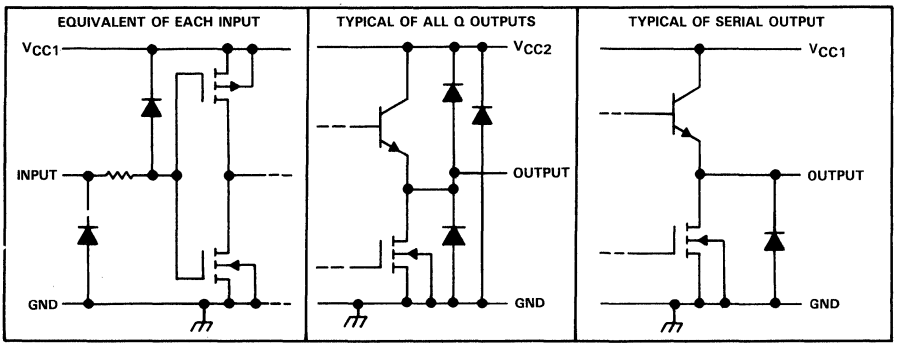
FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R32	LATCHES LC1 THRU LC32	OUTPUTS	
	CLOCK	LATCH ENABLE	OUTPUT ENABLE			SERIAL	Q1 THRU Q32
LOAD	↑	X	X	Load and shift†	Determined by	R32	Determined by
	No↑	X	X	No change	Latch Enable‡	R32	Output Enable
LATCH	X	L	X	As determined above	Stored data	R32	Determined by
	X	H	X	As determined above	New data	R32	Output Enable
OUTPUT ENABLE	X	X	L	As determined above	Determined by	R32	All L
	X	X	H	As determined above	Latch Enable‡	R32	LC1 thru LC32, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
†R32 and the serial output take on the state of R31, R31 takes on the state of R30,. . .R2 takes on the state of R1, and R1 takes on the state of the data input.
‡New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.

typical operating sequence



schematic of inputs and outputs



absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC2} . . . . . 70 V
Input voltage . . . . . V_{CC1} + 0.3 V
Ground current . . . . . 700 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1825 mW
Minimum operating free-air temperature . . . . . −55°C
Operating case temperature . . . . . 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 14.6 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage	10.8	12	13.2	V
V_{CC2}	Supply voltage	0		60	V
V_{IH}	High-level input voltage	$0.75V_{CC}$		$V_{CC}+0.3$	V
V_{IL}	Low-level input voltage	−0.3		$0.25V_{CC}$	
I_{OH}	High-level output current	−15			mA
I_{OL}	Low-level output current	15			mA
I_{OK}	Peak output clamp diode current			±20	mA
f_{clock}	Clock frequency, T_A = 25°C			6.25	MHz
$t_{w(CLK)}$	Clock pulse duration, high or low, T_A = 25°C	80			ns
$t_{w(LE)}$	Latch enable pulse duration, T_A = 25°C	80			
t_{su}	Setup time, data valid before clock↑, T_A = 25°C	20			ns
t_h	Hold time, data valid after clock ↑, T_A = 25°C	110			ns
T_A	Operating free-air temperature	−55			
T_C	Operating case temperature			125	

electrical characteristics over recommended operating temperature range, V_{CC1} = 12 V, V_{CC2} = 60 V

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_O = −15 mA	55		V
		Serial output	I_O = −100 μA	10		
V_{OL}	Low-level output voltage	Q outputs	I_O = 15 mA		10	V
		Serial output	I_O = 100 μA		1.5	
I_{IH}	High-level input current (see Note 3)		V_I = 12 V		5	μA
I_{IL}	Low-level input current (see Note 3)		V_I = 0		−5	μA
I_{CC1}	Supply current, V_{CC1}				7	mA
I_{CC2}	Supply current, V_{CC2}		Outputs high		20	mA
			Outputs low		2	

NOTE 3: I_{IH} and I_{IL} parameter performances are independent of V_{CC2} and need not be 60 V for this test.

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switching characteristics, V_{CC1} = 12 V, V_{CC2} = 60 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{dLH}	Delay time, clock↑ to serial↑	C_L = 45 pF to ground, See Figures 1 and 2		200	ns
t_{dHL}	Delay time, clock↑ to serial↓			200	ns
t_{dLH}	Delay time, LE to Q output↑	C_L = 45 pF to ground, See Figures 1 and 3		1000	ns
t_{dHL}	Delay time, LE to Q output↓			500	ns

PARAMETER MEASUREMENT INFORMATION

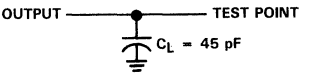


FIGURE 1. OUTPUT LOAD CIRCUIT

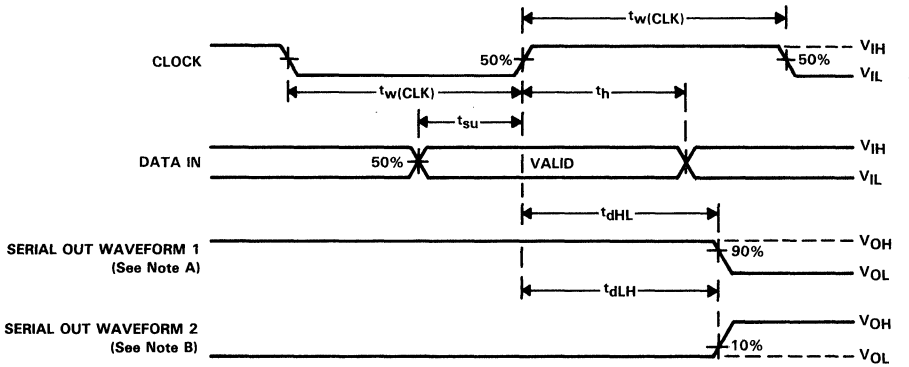


FIGURE 2. VOLTAGE WAVEFORMS FOR SERIAL OUTPUT

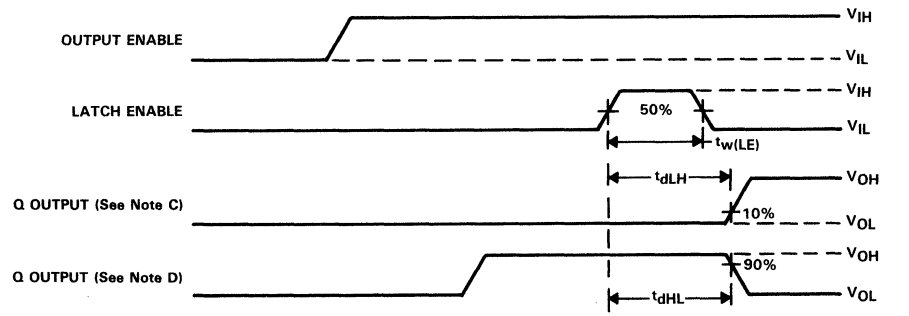


FIGURE 3. VOLTAGE WAVEFORMS FOR Q OUTPUTS

NOTES: A. Waveform 1 is for internal conditions such that a low is clocked into R32.
B. Waveform 2 is for internal conditions such that a high is clocked into R32.
C. To measure t_{dLH}, initially a low is stored in the latch and a high is stored in the shift register.
D. To measure t_{dHL}, initially a high is stored in the latch and a low is stored in the shift register.

D3313, OCTOBER 1989

- **Each Device Drives 34 Electrodes**
- **Selectable Open-Source or Open-Drain Output**
- **Outputs Rated at 225 V**
- **Output Current Capability: −90 mA to 150 mA**
- **CMOS-Compatible Inputs**
- **Very Low Steady-State Power Consumption**

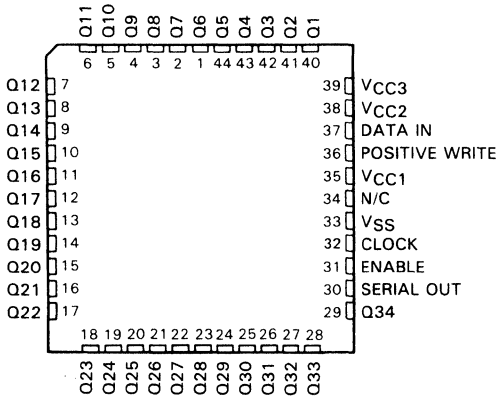
description

The SN55563A and SN55564A are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS compatible. If the Positive Write input is high, the Q outputs act like open-source outputs and output data is not inverted with respect to input data. If the Positive Write input is low, the Q outputs act like open-drain outputs and output data is inverted with respect to input data. The SN55564A output sequence has been reversed from the SN55563A for ease in printed circuit board layout.

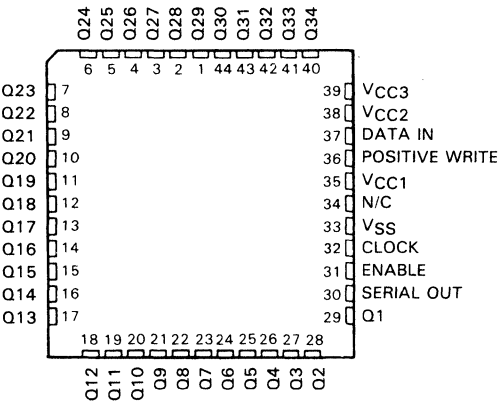
Typically, composite V_{CC2}, V_{CC3}, and V_{SS} signals are externally generated by a high-voltage switching circuit. Serial data is entered into the shift register on the high-to-low transition of the clock input. A high Enable input allows those outputs with a high in their associated register to be turned on, causing the corresponding row to be connected to V_{CC2} when Positive Write is high or to V_{SS} when Positive Write is low. V_{CC3} may be tied to V_{CC2} or held 5 to 15 V above V_{CC2} for better V_{OH} characteristics. The Serial Output from the shift register may be used to cascade additional devices. This output is not affected by the Enable or Positive Write inputs.

The SN55563A and SN55564A are characterized for operation over the full military operating temperature range of −55°C to 125°C.

SN55563A . . . FJ PACKAGE
(TOP VIEW)



SN55564A . . . FJ PACKAGE
(TOP VIEW)



NC—No internal connection

†BIDFET-Bipolar, double-diffused, N-channel and P-channel MOS transistors on the same chip — Patented Process

LOAD FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R34	OUTPUTS	
	CLOCK	ENABLE	POSITIVE WRITE		SERIAL	Q1 THRU Q34
LOAD	↓	X	X	Load and Shift†	R34	Determined by Enable and Positive Write
	No↓	X	X	No Change	R34	Determined by Enable and Positive Write

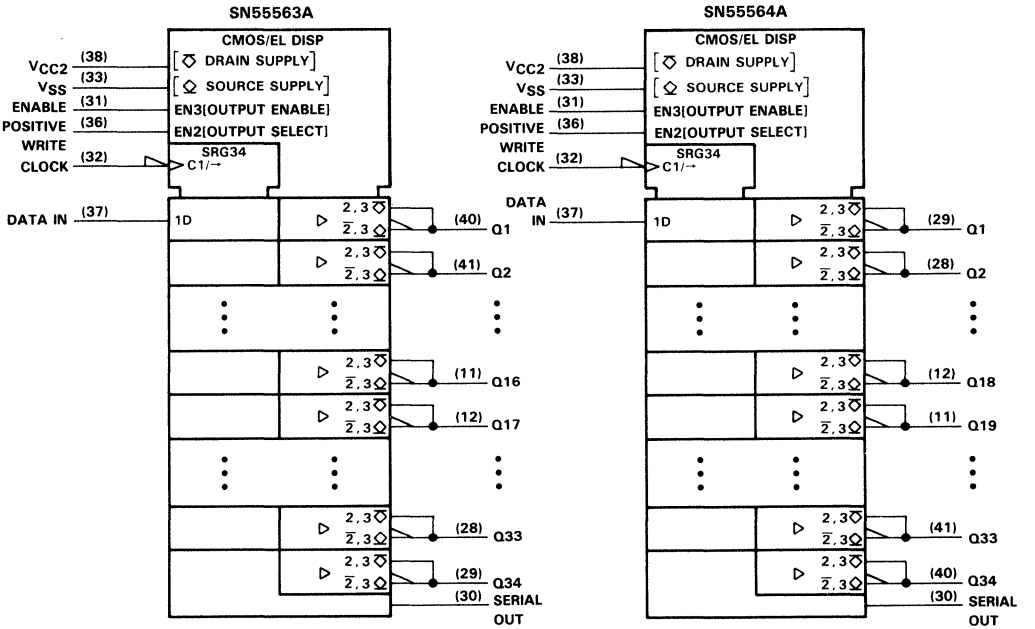
†Register R34 takes on the state of R33, R33 takes on the state of R32, . . . R2 takes on the state of R1, R1 takes on the state of the data input.

OUTPUT CONTROL FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTER CONTENTS Rn FOR R1 THRU R34 (Determined Above)	OUTPUTS	
	CLOCK	ENABLE	POSITIVE WRITE		SERIAL	Q1 THRU Q34
OUTPUT CONTROL	X	L	X	X	R34	High-Impedance
	X	H	H	H	R34	H
	X	H	L	H	R34	L
	X	X	X	L	R34	High-Impedance

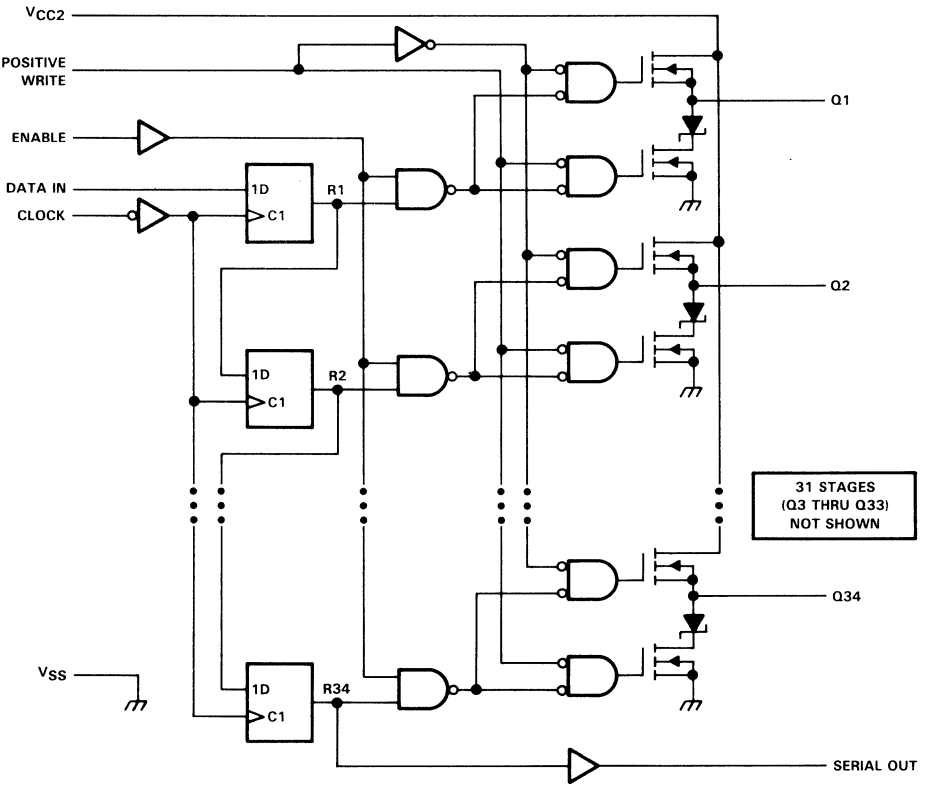
H = high, L = low, X = irrelevant, ↓ = high-to-low transition

logic symbols‡

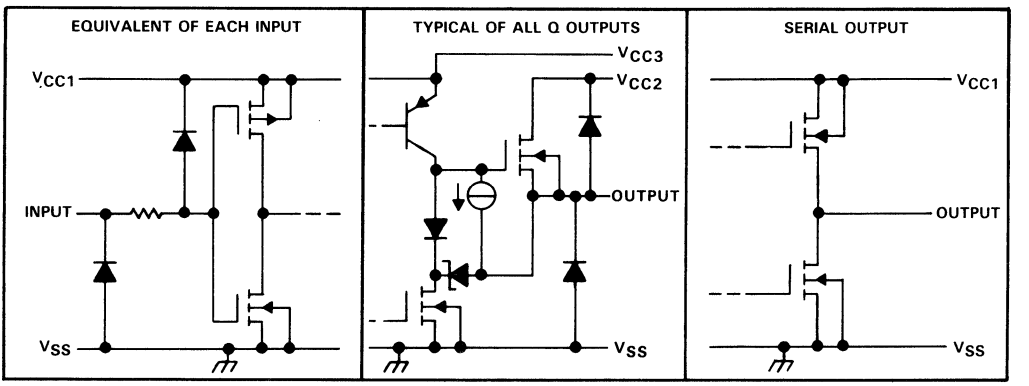


‡These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

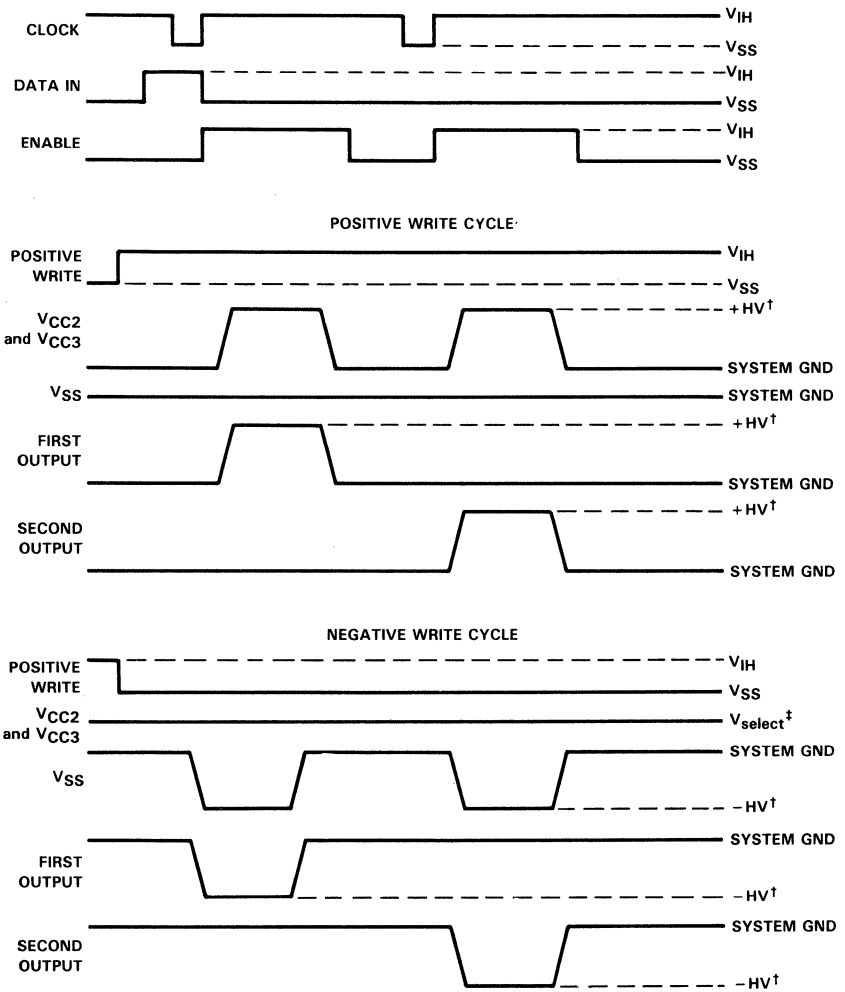
logic diagram (positive logic)



schematics of inputs and outputs



typical operating sequence



†HV = high voltage
‡V_{select} is a voltage level between V_{CC2} of the column driver and V_{SS}.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperture range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 230 V
Supply voltage, V_{CC3} . . . . . 230 V
Supply voltage, V_{SS} . . . . . −230 V
Input voltage . . . . . −0.3 V to V_{CC1} + 0.3 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1825 mW
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to V_{SS}.
2. For operation above 25°C free-air temperature, derate 365 mW at 125°C at the rate of 14.6 mW/°C.

recommended operating conditions (see Figure 1 and Figure 2)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	10.8	12	13.2	V
Supply voltage, V_{CC2}	$V_{CC3}-15$		V_{CC3}	V
Supply voltage, V_{CC3}	0		225	V
Supply voltage, V_{SS}	0		−225	V
High-level input voltage, V_{IH}	$0.75V_{CC1}$		$V_{CC1}+0.3$	V
Low-level input voltage, V_{IL}†	−0.3		$0.25V_{CC1}$	V
High-level output current, I_{OH}			−90	mA
Low-level output current, I_{OL}			150	mA
Output clamp current, I_{OK}			±150	mA
Clock frequency, f_{clock}			1	MHz
Pulse duration, Clock high or low, t_{wCLK}	125			ns
Setup time, data high or low before clock↓, t_{su1}	100			ns
Setup time, Clock low before V_{CC2}↑ or V_{SS}↓, t_{su2}	300‡			ns
Setup time, Enable high before V_{CC2}↑ or V_{SS}↓, t_{su3}	300‡			ns
Setup time, Positive Write high or low before V_{CC2}↑ or V_{SS}↓, t_{su4}	300‡			ns
Hold time, data high or low after clock↓, t_{h1}	100			ns
Hold time, Clock high after V_{CC2}↓ or V_{SS}↑, t_{h2}	300‡			ns
Hold time, Enable high after V_{CC2}↓ or V_{SS}↑, t_{h3}	0‡			ns
Hold time, Positive Write after V_{CC2}↓ or V_{SS}↑, t_{h4}	0‡			ns
Hold time, Enable low between successive V_{CC2}↑, t_{h5}	12‡			μs
Hold time, Enable low between successive V_{SS}↓, t_{h6}	300‡			ns
Operating free-air temperature, T_A	−55		125	°C

†The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
‡These minimum recommendations are not tested during manufacturing. Performance is dependent on application voltage and temperature and must be validated by the user.

electrical characteristics over recommended operating ranges of V_{CC1} and free-air temperature range, V_{CC2} = 225 V, V_{CC3} = 225 V, V_{SS} = 0 (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$I_{O(off)}$	Off-state Q output current		V_O = 225 V		150	μA
			V_O = 0		−150	
V_{OH}	High-level output voltage	Q outputs	I_O = −70 mA, V_{CC1} = 12 V	V_{CC2} − 40		V
			I_O = −90 mA, V_{CC1} = 12 V	V_{CC2} − 45		
		Serial Out	I_O = −100 μA, V_{CC1} = 12 V	10.5		
V_{OL}	Low-level output voltage	Q outputs	I_O = 150 mA		30	V
		Serial Out	I_O = 100 μA		1	
I_{IH}	High-level input current		V_{IH} = V_{CC1}		100	μA
I_{IL}	Low-level input current		V_{IL} = 0		−100	μA
I_{CC1}	Supply current from V_{CC1}		One Q output high		4	mA
			All Q outputs low or high impedance		2	
I_{CC3}	Supply current from V_{CC3}‡		One Q output high, V_{CC1} = 12 V		10	mA
			All Q outputs low or high impedance, V_{CC1} = 12 V		200	μA

switching characteristics over recommended operating range of V_{CC1}, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level serial output from clock	C_L = 50 pF to V_{SS}, See Figures 3 and 4		400	ns
t_{PHL}	Propagation delay time, high-to-low level serial output from clock			400	ns

‡I_{CC3} is measured with V_{CC2} and V_{CC3} shorted together.

PARAMETER MEASUREMENT INFORMATION

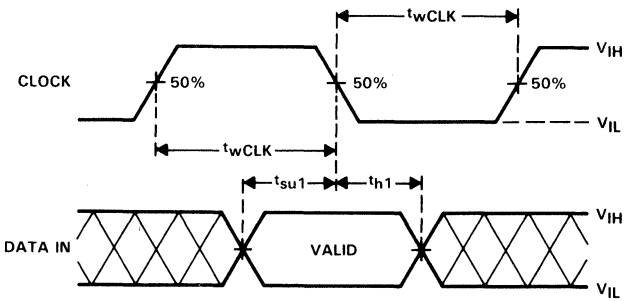


FIGURE 1. INPUT TIMING VOLTAGE WAVEFORMS

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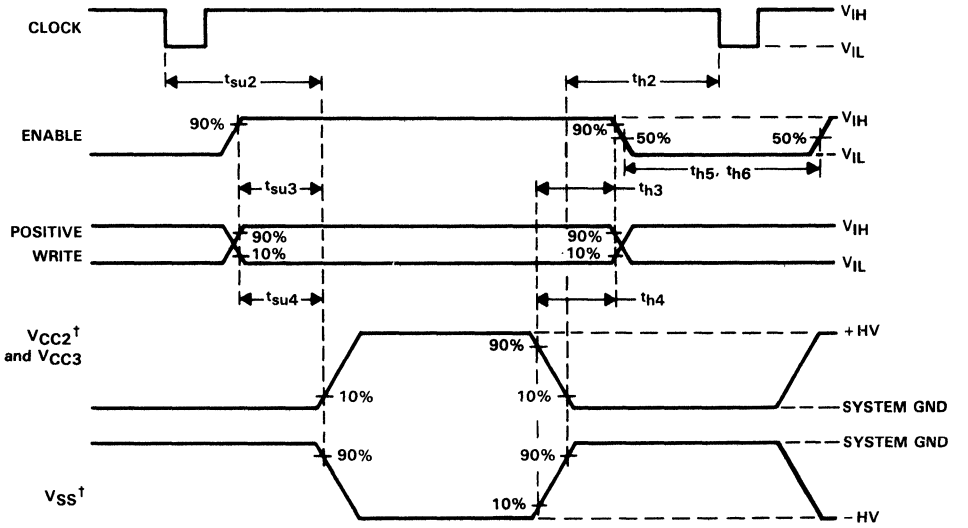
PARAMETER MEASUREMENT INFORMATION



†Timing waveforms are with respect to V_{CC2} or V_{SS}, as appropriate.

FIGURE 2. CONTROL INPUT TIMING VOLTAGE WAVEFORMS

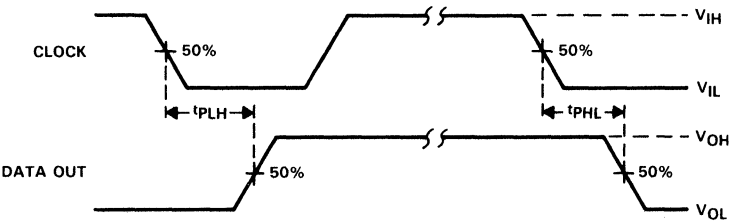
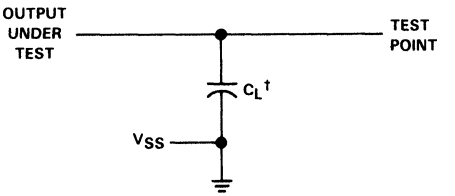


FIGURE 3. VOLTAGE WAVEFORMS FOR PROPAGATION DELAY TIMES, CLOCK TO DATA OUT



†C_L includes probe and jig capacitance.

FIGURE 4. LOAD CIRCUIT

D2471, DECEMBER 1985—REVISED JULY 1989

- **Controls 32 Electrodes**
- **100-V Totem-Pole Outputs**
- **Low Stand-by Power Consumption**
- **All Outputs Contain Sink and Source Clamp Diodes**
- **15-mA Steady-State Output Current**
- **Rugged DMOS Outputs**
- **CMOS Inputs**
- **Direct Replacement for SN75500A**

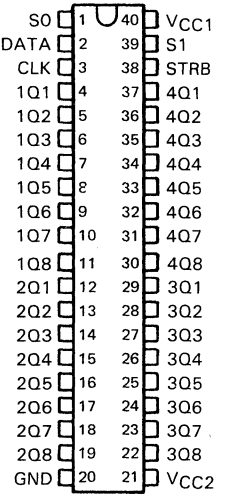
description

The SN65500E and SN75500E are monolithic BIDFET† integrated circuits designed to perform the line select operation of a matrix-addressable display. The device inputs are diode-clamped CMOS inputs.

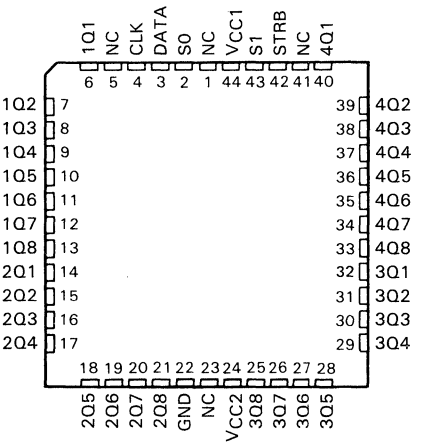
The outputs of these drivers are normally low and can be selectively switched high when the strobe input is low. Selection of the outputs is achieved through the data, S0, and S1 inputs. The 8-bit data stored internally in the serial register is inverted and sent to one of four output sections by the 2-line to 4-line decoder. All other outputs remain low. Internal circuits provide a high-current pulse to the level-shifting circuit during positive output transitions. When the output transition is complete, the low steady-state current reduces the circuit's standby power consumption. All outputs contain clamp diodes to the V_{CC2} and GND supply inputs.

The SN65500E is characterized for operation from −40°C to 85°C. The SN75500E is characterized for operation from 0°C to 70°C.

N PACKAGE
(TOP VIEW)



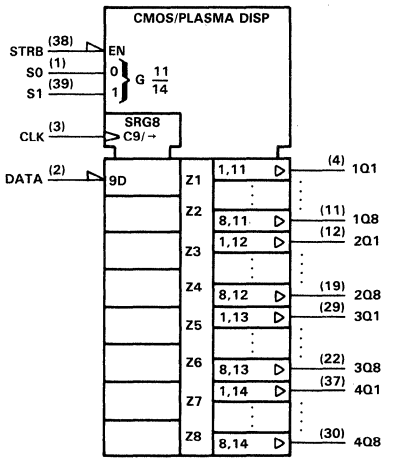
FN PACKAGE
(TOP VIEW)



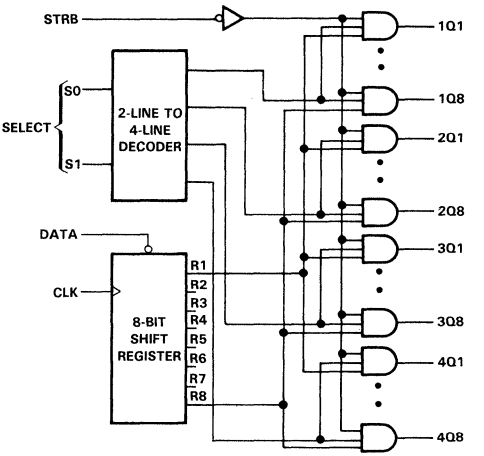
NC—No internal connection

†BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

logic symbol†



functional block diagram (positive logic)



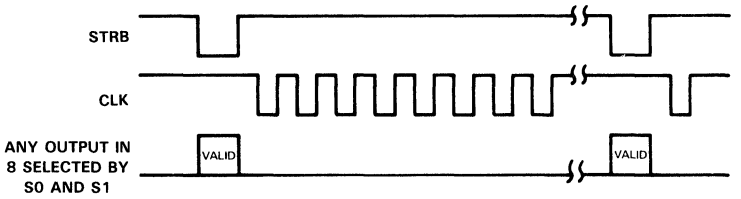
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

FUNCTION TABLE

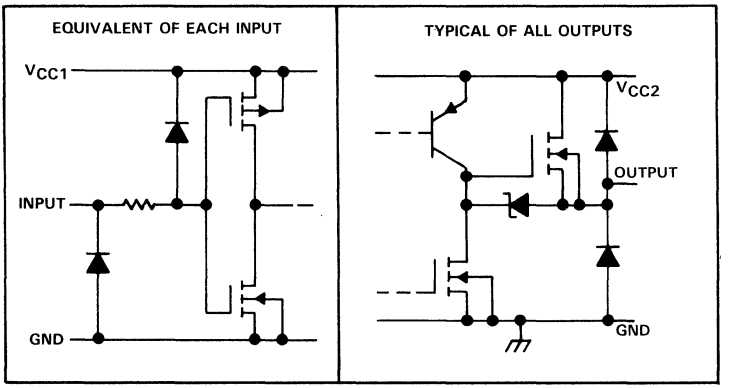
FUNCTION	INPUTS					OUTPUTS							
	DATA	CLK	SELECT		STRB	SHIFT REGISTER			1Q1 ... 1Q8	2Q1 ... 2Q8	3Q1 ... 3Q8	4Q1 ... 4Q8
			S1	S0		R1	R2	R3 ... R8				
LOAD	H	↑	X	X	H	L	$R1_n$	$R2_n$ ... $R7_n$	L ... L	L ... L	L ... L	L ... L
	L	↑	X	X	H	H	$R1_n$	$R2_n$ ... $R7_n$	L ... L	L ... L	L ... L	L ... L
STROBE	X	X	X	X	H	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	L ... L	L ... L	L ... L	L ... L
	X	H	L	L	L	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	R1 ... R8	L ... L	L ... L	L ... L
	X	H	L	H	L	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	L ... L	R1 ... R8	L ... L	L ... L
	X	H	H	L	L	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	L ... L	L ... L	R1 ... R8	L ... L
	X	H	H	H	L	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	L ... L	L ... L	L ... L	R1 ... R8

H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
R1 . . . R8 = levels currently at internal outputs of shift registers one through eight, respectively.
$R1_n$ . . . $R8_n$ = levels at shift-register outputs R1 through R8, respectively, before the most recent ↑ transition of the clock.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 100 V
Input voltage . . . . . V_{CC1} + 0.3 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN65500E . . . . . −40°C to 85°C
SN75500E . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C
Case temperature for 10 seconds: FN package . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1775 mW	14.2 mW/°C	1136 mW	923 mW
N	1275 mW	10.2 mW/°C	816 mW	663 mW

recommended operating conditions

		SN65500E			SN75500E			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC1}		10.8	12	13.2	10.8	12	13.2	V
Supply voltage, V_{CC2}		0		100	0		100	V
High-level input voltage, V_{IH}, as a percentage of V_{CC1}		75%			75%			
Low-level input voltage, V_{IL}, as a percentage of V_{CC1}				25%			25%	
High-level output clamp current				20			20	mA
Low-level output clamp current				−20			−20	mA
Clock frequency, f_{clock} (see Figure 2)		0		8	0		8	MHz
Duration of high or low clock pulse, t_w		62			62			ns
Setup time, t_{su}	Data inputs before clock↑	20			20			ns
	Select inputs before strobe↓	50			50			
Hold time, t_h	Data inputs after clock↑ (see Note 2)	50			50			ns
	Strobe input high after clock↑	50			50			
	Select inputs after strobe↑	50			50			
Operating free-air temperature, T_A		−40		85	0		70	°C

NOTE 2: For operation above 25°C junction temperature, refer to Figure 2.

electrical characteristics over recommended operating free-air temperature range

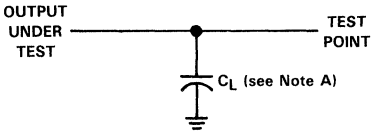
PARAMETER		TEST CONDITIONS		SN65500E			SN75500E			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	Input clamp voltage	V_{CC1} = 12 V,	I_I = −12 mA		−1	−1.5		−1	−1.5	V
V_{OH}	High-level output voltage	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OH} = −1 mA	94	97.5		95	97.5		V
			I_{OH} = −10 mA	92	94.5		93	94.5		
			I_{OH} = −15 mA	90	93.5		91	93.5		
V_{OL}	Low-level output voltage	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OL} = 1 mA		0.85	2		0.85	2	V
			I_{OL} = 10 mA		2	4		2	4	
			I_{OL} = 15 mA		2.75	5		2.75	5	
V_{OK}	Output clamp voltage	V_{CC2} = 0	I_O = 20 mA		1	2.5		1	2.5	V
			I_O = −20 mA		−1.2	−2.5		−1.2	−2.5	
I_{IH}	High-level input current	V_{CC1} = 13.2 V,	V_I = V_{IH} min			1			1	μA
I_{IL}	Low-level input current	V_{CC1} = 13.2 V,	V_I = V_{IL} max			−1			−1	μA
I_{CC1}	Supply current	V_{CC1} = 13.2 V,	V_{CC2} = 100 V		0.05	1		0.05	1	mA
I_{CC2}	Supply current	V_{CC2} = 100 V			1	5		1	3	mA

†All typical values are at V_{CC1} = 12 V, T_A = 25°C.

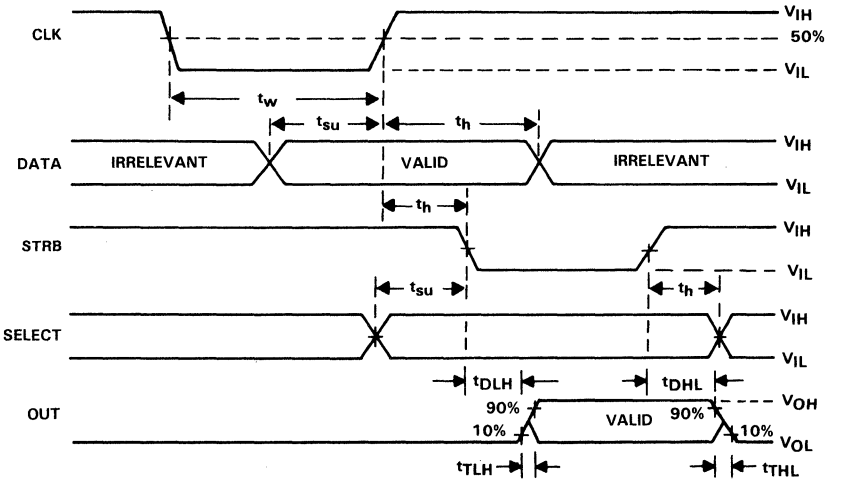
switching characteristics, V_{CC1} = 12 V, V_{CC2} = 100 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output from strobe input	C_L = 30 pF, See Figure 1		250	ns
t_{DLH}	Delay time, low-to-high-level output from strobe input			450	ns
t_{THL}	Transition time, high-to-low-level output			200	ns
t_{TLH}	Transition time, low-to-high-level output			300	ns

PARAMETER MEASUREMENT INFORMATION



LOAD TEST CIRCUIT



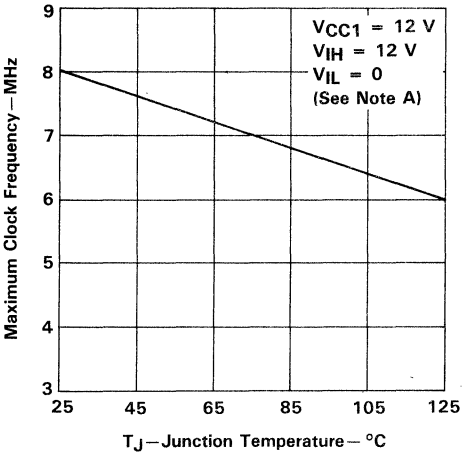
VOLTAGE WAVEFORMS

NOTE A. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

MAXIMUM CLOCK FREQUENCY
vs
VIRTUAL JUNCTION TEMPERATURE



NOTE A: This curve assumes a symmetrical clock pulse.

FIGURE 2

THERMAL INFORMATION

junction temperature formula

$$T_J = T_A + P_D R_{\theta JA}$$
$$T_J = T_C + P_D R_{\theta JC}$$

where

T_J = virtual junction temperature
T_A = free-air temperature
P_D = average device power dissipation
R_θ = thermal resistance (junction-to-air, $R_{\theta JA}$, or junction-to-case, $R_{\theta JC}$)

PACKAGE TYPE	$R_{\theta JA}$	$R_{\theta JC}$
FN 44-pin plastic	70°C/W	22°C/W
N 40-pin plastic	97°C/W	27°C/W

D2472, MARCH 1983—REVISED OCTOBER 1989

- **Controls 32 Electrodes**
- **100-V Totem-Pole Outputs**
- **Low Standby Power Consumption**
- **All Outputs Contain Sink and Source Clamp Diodes**
- **15-mA Steady-State Output Current**
- **Rugged DMOS Outputs**
- **CMOS Inputs**
- **Direct Replacement for SN75501C**

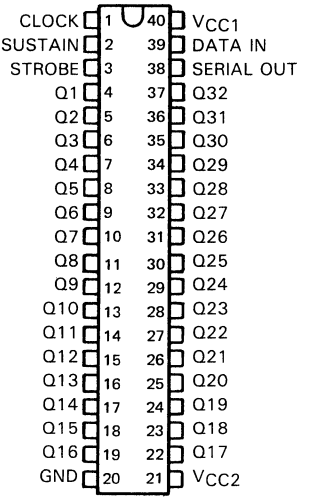
description

The SN65501E and SN75501E are monolithic BIDFET† integrated circuits designed to provide the serial-to-parallel conversion and level translation of data in a matrix-addressable display. The device inputs are diode-clamped CMOS inputs.

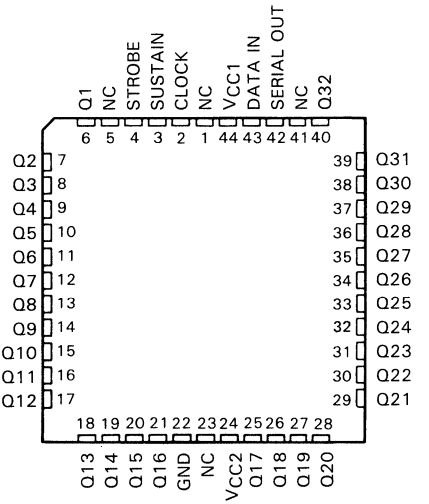
The Q outputs of these drivers are normally high and can be switched either selectively or together. Any output whose associated register bit (in the internal 32-bit serial register) contains a low will switch low when STROBE is low if SUSTAIN is high. All other outputs remain high. When SUSTAIN is low, all outputs switch low independently of the data or strobe inputs. This feature can be used to generate a portion of the sustain pulse required in the operation of an ac plasma display. The internal level-shift circuits provide additional drive during the times that the outputs switch high to facilitate fast rise times while maintaining low standby power consumption. All outputs contain clamp diodes to the V_{CC2} and GND supply inputs.

The SN65501E is characterized for operation over the temperature range of −40°C to 85°C. The SN75501E is characterized for operation over the temperature range of 0°C to 70°C.

N PACKAGE
(TOP VIEW)



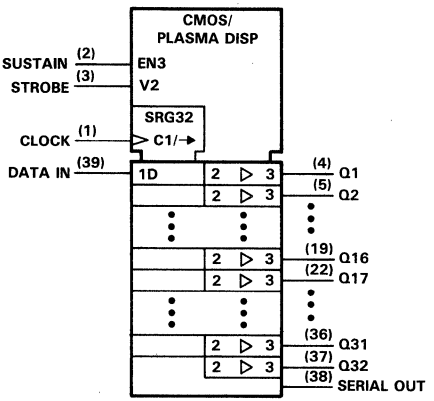
FN PACKAGE
(TOP VIEW)



NC—No internal connection

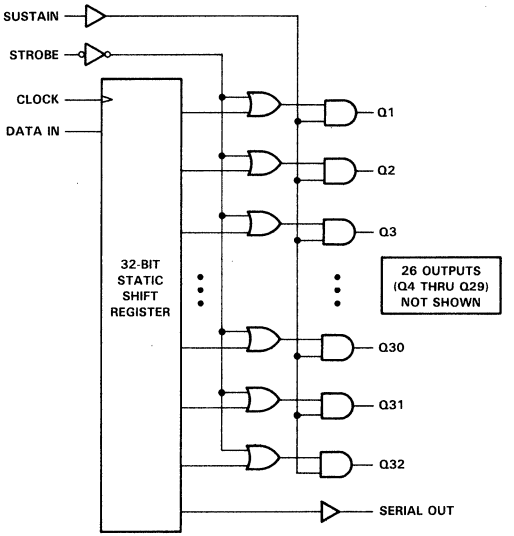
† BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

functional block diagram (positive logic)

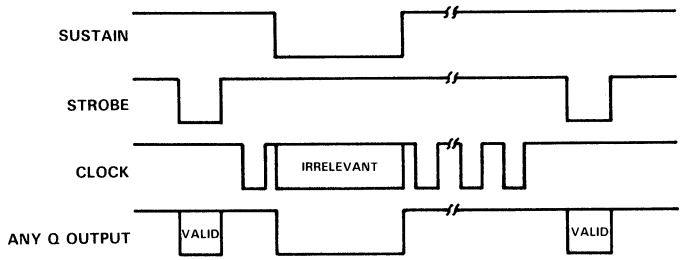


FUNCTION TABLE

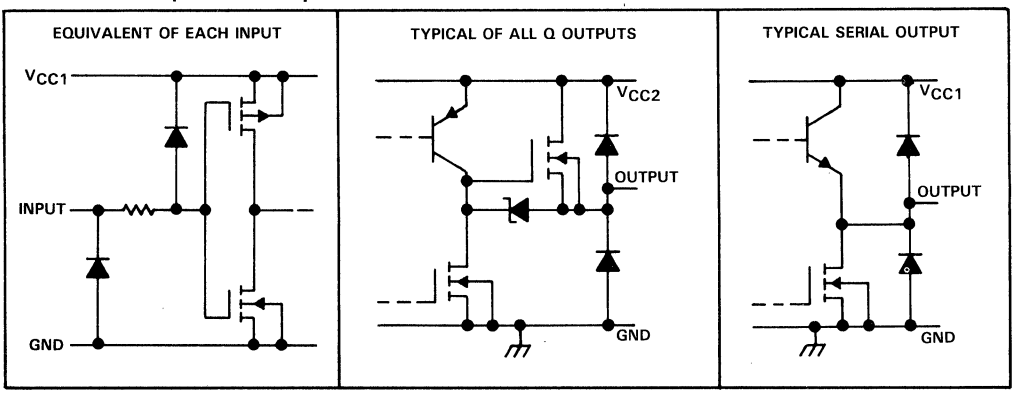
FUNCTION	INPUTS				OUTPUTS						
	DATA	CLOCK	STROBE	SUSTAIN	SHIFT REGISTER R1	SHIFT REGISTER R2	SHIFT REGISTER R3 . . . R32	SERIAL DATA	Q1	Q2	Q3 . . . Q32
LOAD	H	↑	H	H	H	$R1_n$	$R2_n$ . . . $R31_n$	$R32_n$	H	H	H . . . H
	L	↑	H	H	L	$R1_n$	$R2_n$ . . . $R31_n$	$R32_n$	H	H	H . . . H
STROBE	X	X	H	H	$R1_n$	$R2_n$	$R3_n$ . . . $R32_n$	$R32_n$	H	H	H . . . H
	X	H	L	H	$R1_n$	$R2_n$	$R3_n$ . . . $R32_n$	$R32_n$	R1	R2	R3 . . . R32
SUSTAIN	X	X	X	L	$R1_n$	$R2_n$	$R3_n$ . . . $R32_n$	$R32_n$	L	L	L . . . L

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
R1 . . . R32 = levels currently at internal outputs of shift registers one through thirty-two, respectively.
$R1_n$ . . . $R32_n$ = levels at shift-register outputs R1 through R32 respectively, before the most recent ↑ transition at the CLOCK input.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 100 V
Input voltage . . . . . V_{CC1} to 0.3 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65501E . . . . . −40°C to 85°C
SN75501E . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1775 mW	14.2 mW/°C	1136 mW	923 mW
N	1275 mW	10.2 mW/°C	816 mW	663 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	13.2	V
Supply voltage, V_{CC2}		0		100	V
High-level input voltage, V_{IH}		0.75 V_{CC1}			V
Low-level input voltage, V_{IL}				0.25 V_{CC1}	V
High-level Q output clamp current, I_{OKH}				20	mA
Low-level Q output clamp current, I_{OKL}				−20	mA
Clock frequency, f_{clock}, at or below, 25°C junction temperature (see Note 2)		0		8	MHz
Duration of high or low clock pulse, t_w		62			ns
Setup time, t_{su}	Data inputs before CLOCK↑	20			ns
	Data inputs after CLOCK↑	50			
Hold time, t_h	STROBE high after CLOCK↑	150			ns
	STROBE high after SUSTAIN↑	250			
Operating free-air temperature, T_A	SN65501E	−40		85	°C
	SN75501E	0		70	

NOTE 2: See Figure 3 for maximum clock frequency when devices are operated in cascade or for operation above T_J = 25°C.

electrical characteristics over recommended operating free-air temperature range

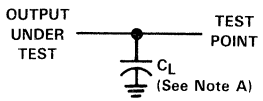
PARAMETER			TEST CONDITIONS		SN65501E			SN75501E			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	Input clamp voltage		V_{CC1} = 12 V,	I_I = 12 mA		−1	−1.5		−1	−1.5	V
V_{OH}	High-level output voltage	Q outputs	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OH} = −1 mA	94	97.5		95	97.5		V
				I_{OH} = −10 mA	92	94.5		93	94.5		
				I_{OH} = −15 mA	90	93.5		91	93.5		
		SERIAL OUT	V_{CC1} = 10.8 V,	I_{OH} = −100 μA	9	10		9	10		
V_{OL}	Low-level output voltage	Q outputs	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OL} = 1 mA		0.85	2		0.85	2	V
				I_{OL} = 10 mA		2	4		2	4	
				I_{OL} = 15 mA		2.75	5		2.75	5	
		SERIAL OUT	V_{CC1} = 10.8 V,	I_{OL} = 100 μA		0.1	1		0.1	1	
V_{OK}	Output clamp voltage	Q output	V_{CC2} = 0	I_{OK} = 20 mA		1	2.5		1	2.5	V
				I_{OK} = −20 mA		−1.2	−2.5		−1.2	−2.5	
I_{IH}	High-level input current		V_{CC1} = 13.2 V, V_{CC2} = 100 V	V_{IH} = V_{IH}min,			1			1	μA
I_{IL}	Low-level input current		V_{CC1} = 13.2 V, V_{CC2} = 100 V	V_{IL} = V_{IL}max,			−1			−1	μA
I_{CC1}	Supply current from V_{CC1}		V_{CC1} = 13.2 V, V_{CC2} = 100 V			0.05	1		0.05	1	mA
I_{CC2}	Supply current from V_{CC2}		V_{CC2} = 100 V			1	5		1	3	mA

† Typical values are at V_{CC1} = 12 V, T_A = 25°C.

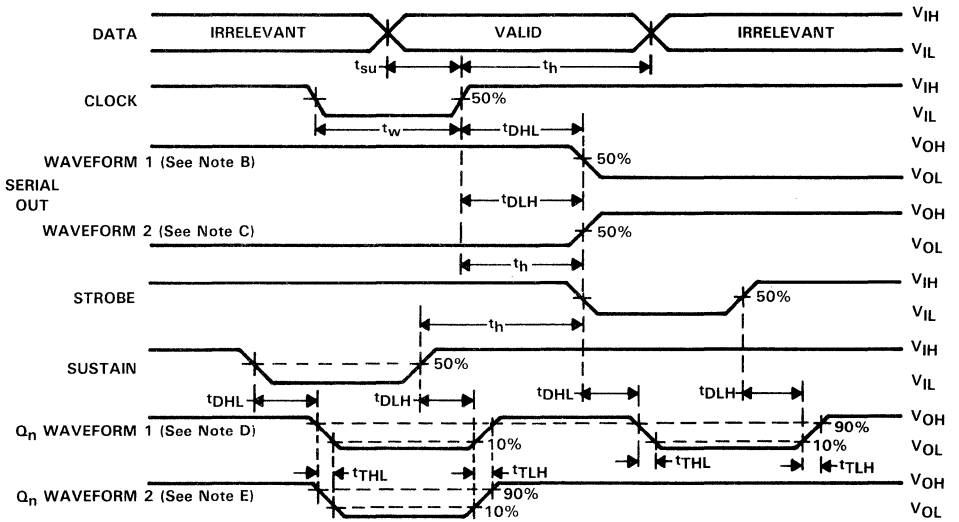
switching characteristics, V_{CC1} = 12 V, V_{CC2} = 100 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level outputs	STROBE to Q outputs	C_L = 30 pF			250	ns
		SUSTAIN to Q outputs	C_L = 30 pF			250	
		CLOCK to SERIAL OUT	C_L = 20 pF			147	
t_{DLH}	Delay time, low-to-high-level outputs	STROBE to Q outputs	C_L = 30 pF			450	ns
		SUSTAIN to Q outputs	C_L = 30 pF			450	
		CLOCK to SERIAL OUT	C_L = 20 pF			147	
t_{THL}	Transition time, high-to-low-level Q output		C_L = 30 pF			200	ns
t_{TLH}	Transition time, low-to-high-level Q output		C_L = 30 pF			300	ns

PARAMETER MEASUREMENT INFORMATION



LOAD TEST CIRCUIT



NOTES: A. C_L includes probe and jig capacitance.
B. Serial out waveform for internal conditions such that a low is registered in R32.
C. Serial out waveform for internal conditions such that a high is registered in R32.
D. Q_n output with a low stored in associated register R_n.
E. Q_n output with a high stored in associated register R_n.

VOLTAGE WAVEFORMS

FIGURE 1. SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

MAXIMUM CLOCK FREQUENCY
vs
JUNCTION TEMPERATURE

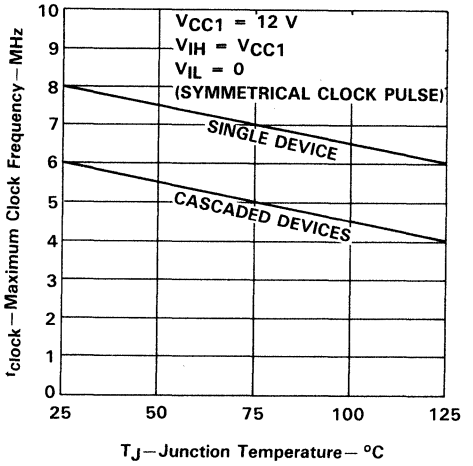


FIGURE 2

INPUT VOLTAGE LOGIC LEVEL LIMITS
vs
V_{CC1} SUPPLY VOLTAGE

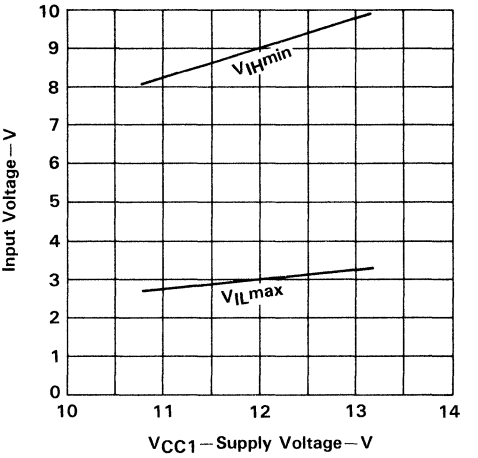


FIGURE 3

THERMAL CHARACTERISTICS

junction temperature formula

$$T_J = T_A + P_D R_\theta$$

where

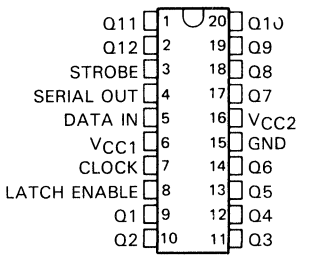
T_J = virtual junction temperature
T_A = free-air temperature
P_D = average device power dissipation
R_θ = thermal resistance (junction-to-air, $R_{\theta JA}$, or junction-to-case, $R_{\theta JC}$)

PACKAGE	$R_{\theta JA}$	$R_{\theta JC}$
FN	70°C/W	22°C/W
N	100°C/W	27°C/W

D2654, DECEMBER 1985—REVISED OCTOBER 1989

- **Each Device Drives 12 Lines**
- **60-V Output Voltage Swing Capability**
- **25-mA Output Source Current Capability**
- **High-Speed Serially-Shifted Data Input**
- **TTL-Compatible Inputs**
- **Latches on All Driver Outputs**

DW OR N PACKAGE
(TOP VIEW)



description

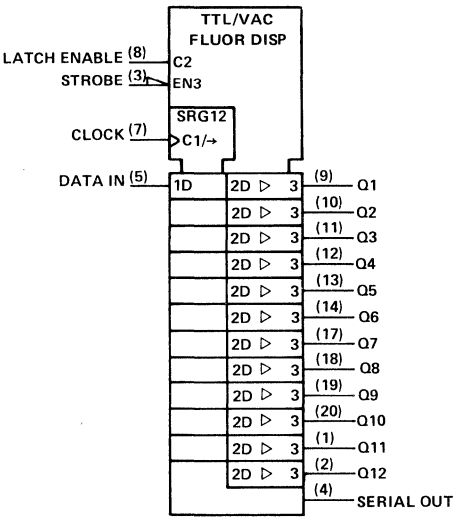
The SN65512B and SN75512B are monolithic BIDFET† integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display.

All device inputs are diode-clamped p-n-p inputs and will assume a high logic level when open-circuited. The nominal input threshold is 1.5 V. Outputs are totem-pole structures formed by an n-p-n emitter follower and double-diffused MOS (DMOS) transistors.

The device consists of a 12-bit shift register, 12 latches, and 12 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. When high, LATCH ENABLE transfers the shift register contents to the outputs of the 12 latches. The active-low STROBE input enables all Q outputs. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by LATCH ENABLE or STROBE.

The SN65512B is characterized for operation from −40°C to 85°C. The SN75512B is characterized for operation from 0°C to 70°C.

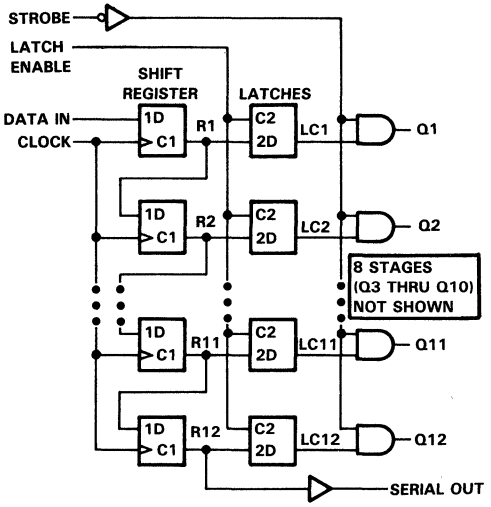
logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

† BIDFET —Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

logic diagram (positive logic)

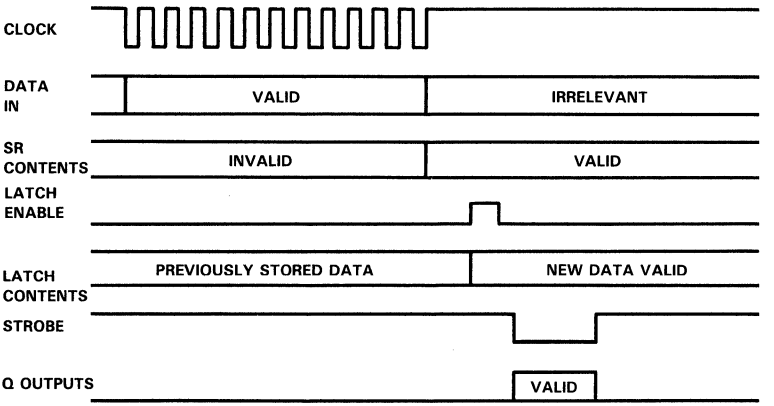


FUNCTION TABLE

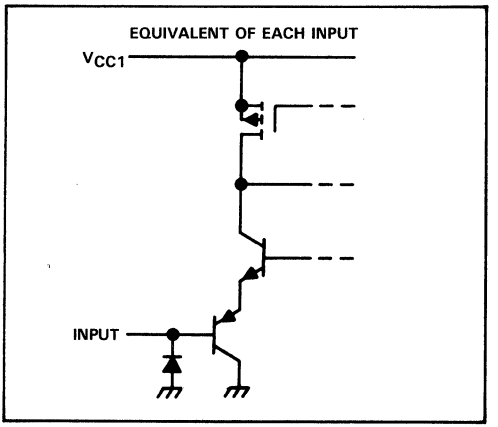
FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R12	LATCHES LC1 THRU LC12	OUTPUTS	
	CLOCK	LATCH ENABLE	STROBE			SERIAL	Q1 THRU Q12
LOAD	↑	X	X	Load and shift†	Determined by LATCH ENABLE‡	R12	Determined by STROBE
	No↑	X	X	No change	Determined by LATCH ENABLE‡	R12	Determined by STROBE
LATCH	X	L	X	As determined above	Stored data	R12	Determined by STROBE
	X	H	X		New data	R12	Determined by STROBE
STROBE	X	X	H	As determined above	Determined by LATCH ENABLE‡	R12	All L
	X	X	L		Determined by LATCH ENABLE‡	R12	LC1 thru LC12, respectively

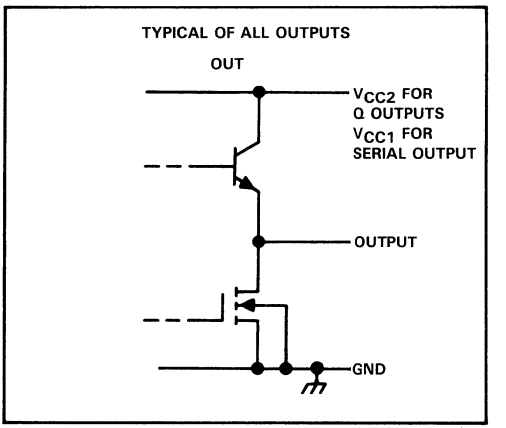
H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
† R12 takes on the state of R11, R11 takes on the state of R10, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.
‡ New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 70 V
Input voltage . . . . . V_{CC1}
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN65512B . . . . . −40°C to 85°C
SN75512B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		SN65512B		SN75512B		UNIT
		MIN	MAX	MIN	MAX	
Supply voltage, V_{CC1}		5	15	5	15	V
Supply voltage, V_{CC2}		0	60	0	60	V
High-level input voltage, V_{IH}		2		2		V
Low-level input voltage, V_{IL}			0.8		0.8	V
High-level output current, I_{OH}			−25		−25	mA
Low-level output current, I_{OL}	V_{CC1} = 10 V		5		5	mA
Clock frequency, f_{clock}	V_{CC1} = 15 V, T_A = 25°C	0	4	0	4	MHz
	V_{CC1} = 5 V, T_A = 25°C	0	1	0	1	
Pulse duration, CLOCK high or low, t_w	V_{CC1} = 15 V, T_A = 25°C	100		100		ns
	V_{CC1} = 5 V, T_A = 25°C	500		500		
Setup time, DATA IN before CLOCK↑, t_{su} (see Figure 1)	V_{CC1} = 15 V, T_A = 25°C	100		100		ns
	V_{CC1} = 5 V, T_A = 25°C	250		250		
Hold time, DATA IN after CLOCK↑, t_h (see Figure 1)	V_{CC1} = 15 V, T_A = 25°C	50		50		ns
	V_{CC1} = 5 V, T_A = 25°C	250		250		
Operating free-air temperature, T_A		−40	85	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	Q outputs	I_{OH} = −25 mA		57.5	58		V
		Serial output	I_{OH} = −200 μA, V_{CC1} = 10 V		9	9.5		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 5 mA, V_{CC1} = 10 V			2.6	5	V
		Serial output	I_{OL} = 200 μA, V_{CC1} = 10 V			0.05	0.2	
I_{IH}	High-level input current		V_{CC1} = 15 V, V_I = 5 V			0.01	1	μA
I_{IL}	Low-level input current		V_{CC1} = 15 V, V_I = 0.8 V			−25	−150	μA
I_{CC1}	Supply current from V_{CC1}		V_{CC1} = 15 V	V_I = 5 V		80	500	μA
				V_I = 0.8 V		2	6	mA
I_{CC2}	Supply current from V_{CC2}		V_{CC1} = 15 V	All outputs high		10	100	μA
				STROBE at 2 V		0.8	3	mA

†All typical values are at V_{CC1} = 10 V, T_A = 25°C.

switching characteristics, V_{CC1} = 10 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output	C_L = 30 pF, See Figure 2		300	ns
t_{DLH}	Delay time, low-to-high-level output			300	ns
t_{THL}	Transition time, high-to-low-level output			500	ns
t_{TLH}	Transition time, low-to-high-level output			500	ns

PARAMETER MEASUREMENT INFORMATION

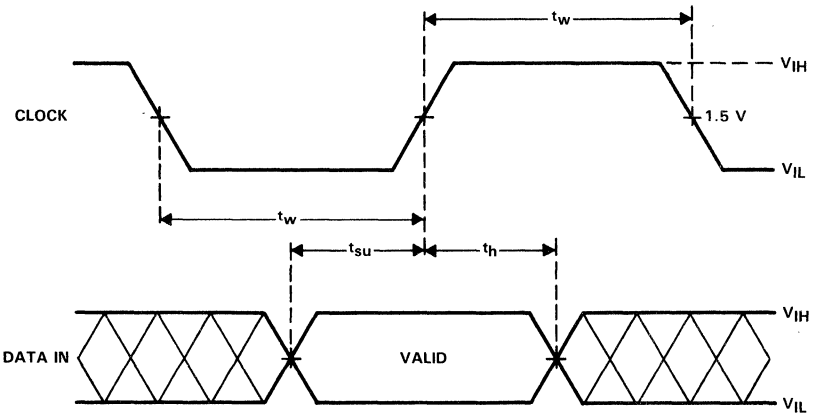


FIGURE 1. INPUT TIMING VOLTAGE WAVEFORMS

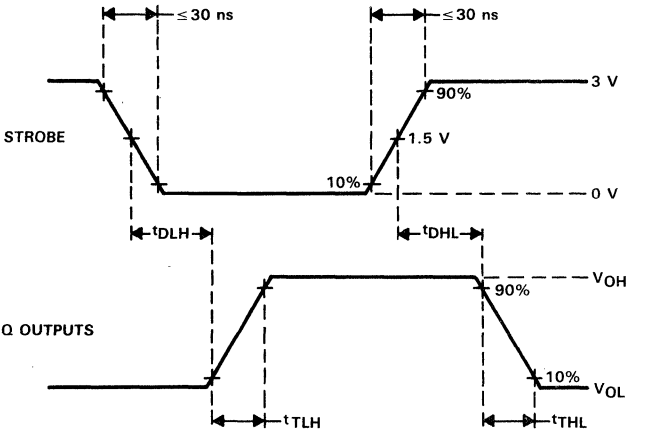


FIGURE 2. SWITCHING-TIME VOLTAGE WAVEFORMS

D2720, MARCH 1983—REVISED MAY 1990

- **Each Device Drives 32 Lines**
- **60-V Output Voltage Swing Capability**
- **25-mA Output Source Current Capability**
- **High-Speed Serially Shifted Data Input**
- **Latches on All Driver Outputs**

description

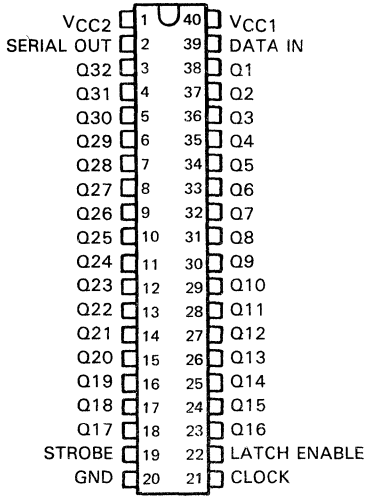
The SN65518 and SN75518 are monolithic BIDFET† integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display.

The devices each consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. While LATCH ENABLE is high, parallel data is transferred to the output buffers through a 32-bit latch. Data present in the latch during the high-to-low transition of LATCH ENABLE is latched. When STROBE is low, all Q outputs are enabled. When STROBE is high, all Q outputs are low.

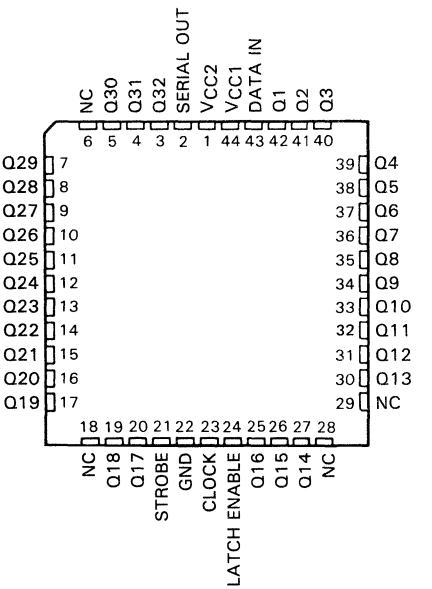
Serial data output from the shift register may be used to cascade additional devices. This output is not affected by LATCH ENABLE or STROBE.

The SN65518 is characterized for operation from −40°C to 85°C and the SN75518 is characterized for operation from 0°C to 70°C.

N PACKAGE
(TOP VIEW)



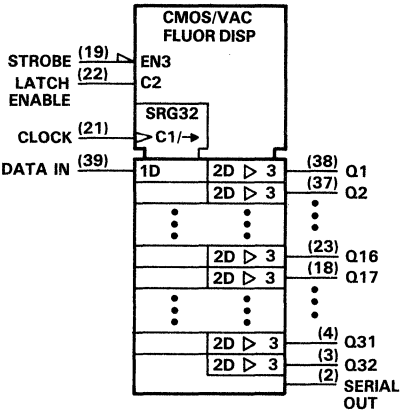
FN PACKAGE
(TOP VIEW)



†BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip—patented process.

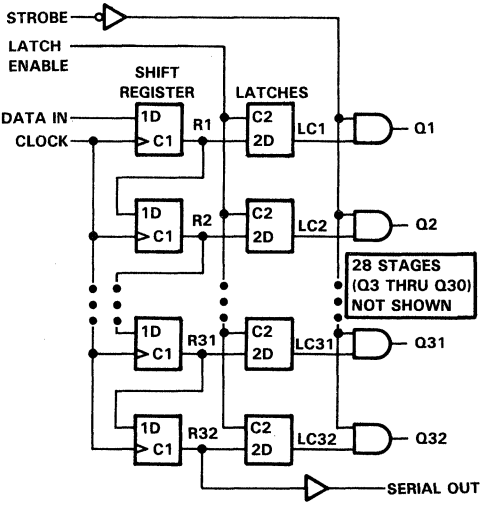
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

logic diagram (positive logic)

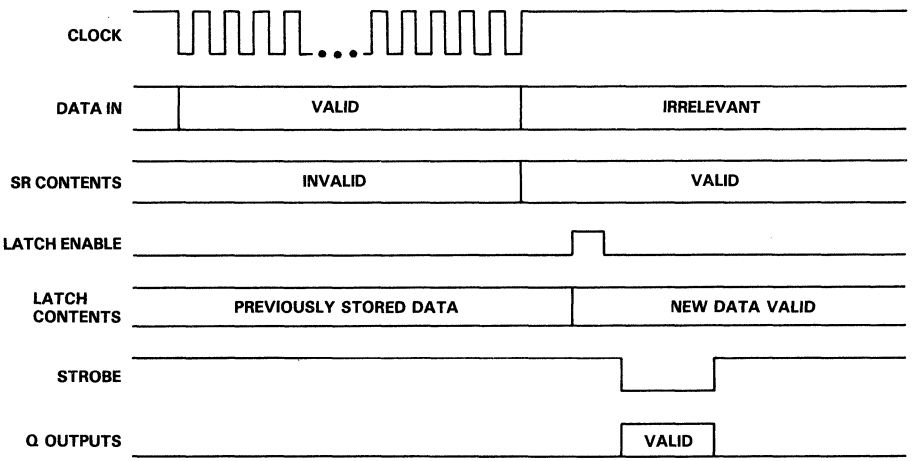


FUNCTION TABLE

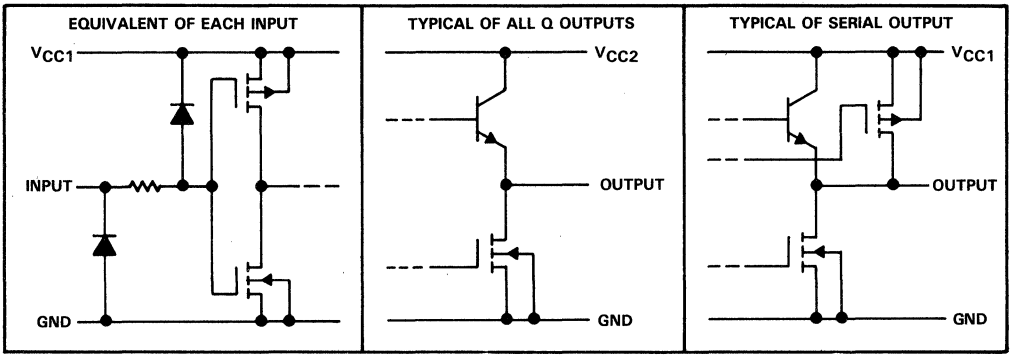
FUNCTION	CONTROL INPUTS			SHIFT REGISTERS	LATCHES	OUTPUTS	
	CLOCK	LATCH ENABLE	STROBE	R1 THRU R32	LC1 THRU LC32	SERIAL	Q1 THRU Q32
LOAD	↑	X	X	Load and shift†	Determined by	R32	Determined by STROBE
	Not↑	X	X	No change	LATCH ENABLE‡		
LATCH	X	L	X	As determined	Stored data	R32	Determined by STROBE
	X	H	X	above	New Data		
STROBE	X	X	H	As determined	Determined by	R32	All L
	X	X	L	above	LATCH ENABLE‡		LC1 thru LC32, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
†R32 and the serial output take on the state of R31, R31 takes on the state of R30, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.
‡New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 70 V
Input voltage, V_I . . . . . V_{CC1}
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65518 . . . . . −40°C to 85°C
SN75518 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1700 mW	13.6 mW/°C	1088 mW	884 mW
N	1250 mW	10.0 mW/°C	800 mW	650 mW

recommended operating conditions, T_A = 25°C (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{CC1}		4.5	15	V
Supply voltage, V_{CC2}		0	60	V
High-level input voltage, V_{IH} (see Figure 1)	V_{CC1} = 4.5 V	3.5		V
	V_{CC1} = 15 V	12		
Low-level input voltage, V_{IL} (see Figure 1)		−0.3	0.8	V
High-level output current, I_{OH}			−25	mA
Low-level output current, I_{OL}			2	mA
Clock frequency, f_{clock} (see Figure 2)	V_{CC1} = 10 V to 15 V	0	5	MHz
	V_{CC1} = 4.5 V	0	1	
Pulse duration, CLOCK high, $t_{w(CKH)}$	V_{CC1} = 10 V to 15 V	100		ns
	V_{CC1} = 4.5 V	500		
Pulse duration, CLOCK low, $t_{w(CKL)}$	V_{CC1} = 10 V to 15 V	100		ns
	V_{CC1} = 4.5 V	500		
Setup time, DATA IN before CLOCK↑, t_{su}	V_{CC1} = 10 V to 15 V	75		ns
	V_{CC1} = 4.5 V	150		
Hold time, DATA IN after CLOCK↑, t_h	V_{CC1} = 10 V to 15 V	75		ns
	V_{CC1} = 4.5 V	150		
Operating free-air temperature, T_A	SN65518	−40	85	°C
	SN75518	0	70	

electrical characteristics over recommended ranges of operating free-air temperature and V_{CC1} (unless otherwise noted), V_{CC2} = 60 V

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	Q outputs	I_{OH} = −25 mA	57.5	58		V
		SERIAL OUT	V_{CC1} = 5 V, I_{OH} = −20 μA	4.5	4.9	5	
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 1 mA			5	V
		SERIAL OUT	I_{OL} = 20 μA		0.06	0.8	
I_{IH}	High-level input current		V_{CC1} = 15 V, V_I = 15 V		0.1	1	μA
I_{IL}	Low-level input current		V_{CC1} = 15 V, V_I = 0 V		−0.1	−1	μA
I_{CC1}	Supply current		V_{CC1} = 4.5 V		1.8	4	mA
			V_{CC1} = 15 V		2	5	
I_{CC2}	Supply current	SN65518	Outputs high, T_A = −40°C			12	mA
		SN65518, SN75518	Outputs high, T_A = 0°C to MAX		7	10	
			Outputs low		0.01	0.5	

†All typical values are at T_A = 25°C.

switching characteristics, V_{CC2} = 60 V, C_L = 50 pF, T_A = 25°C (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	MAX	UNIT
t_d	Delay time, CLOCK to DATA OUT		V_{CC1} = 4.5 V	C_L = 15 pF, See Figure 4		600	ns
			V_{CC1} = 15 V			150	
t_{DHL}	Delay time, high-to-low-level Q output	from LATCH ENABLE	V_{CC1} = 4.5 V	See Figure 5		1.5	µs
		from STROBE		See Figure 6		1	
		from LATCH ENABLE	V_{CC1} = 15 V	See Figure 5		0.5	
		from STROBE		See Figure 6		0.5	
t_{DLH}	Delay time, low-to-high-level Q output	from LATCH ENABLE	V_{CC1} = 4.5 V	See Figure 5		1.5	µs
		from STROBE		See Figure 6		1	
		from LATCH ENABLE	V_{CC1} = 15 V	See Figure 5		0.25	
		from STROBE		See Figure 6		0.25	
t_{THL}	Transition time, high-to-low-level Q output		V_{CC1} = 4.5 V	See Figure 6		3	µs
			V_{CC1} = 15 V			1.5	
t_{TLH}	Transition time, low-to-high-level Q output		V_{CC1} = 4.5 V	See Figure 6		2.5	µs
			V_{CC1} = 15 V			0.75	

RECOMMENDED OPERATING CONDITIONS

INPUT VOLTAGE LOGIC-LEVEL LIMITS
vs
SUPPLY VOLTAGE V_{CC1}

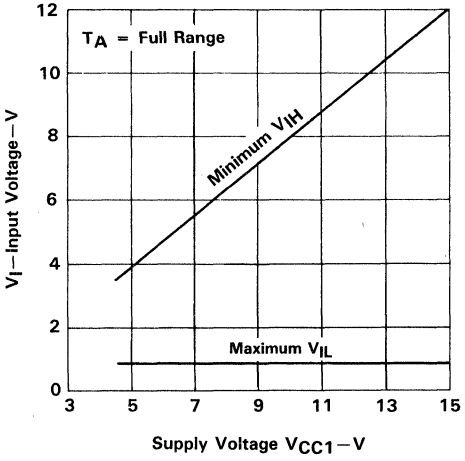


FIGURE 1

MAXIMUM INPUT DATA RATE
vs
SUPPLY VOLTAGE V_{CC1}

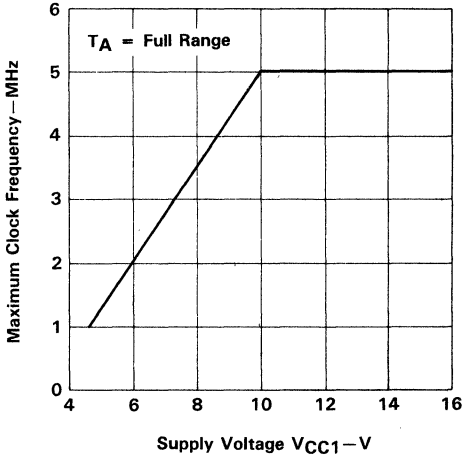


FIGURE 2

PARAMETER MEASUREMENT INFORMATION†

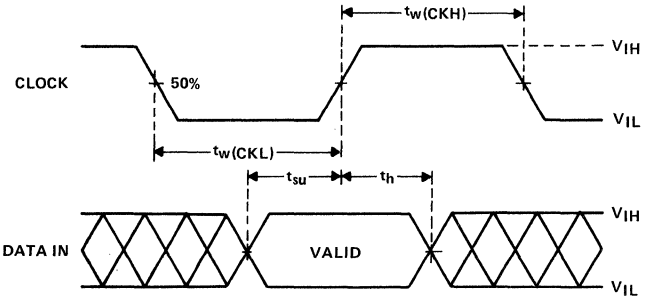


FIGURE 3. INPUT TIMING VOLTAGE WAVEFORMS

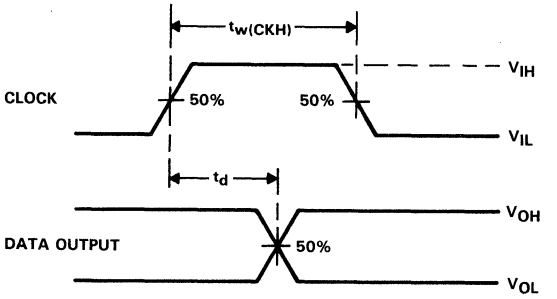


FIGURE 4. DATA OUTPUT SWITCHING TIMES

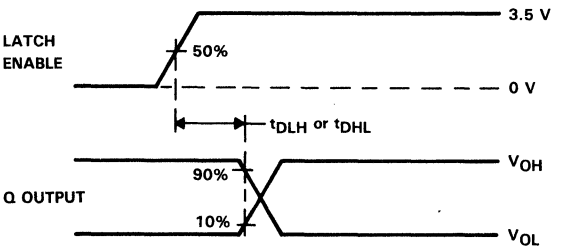


FIGURE 5. Q OUTPUT SWITCHING TIMES

†For testing purposes, all input pulses have maximum rise and fall times of 30 ns.

PARAMETER MEASUREMENT INFORMATION†

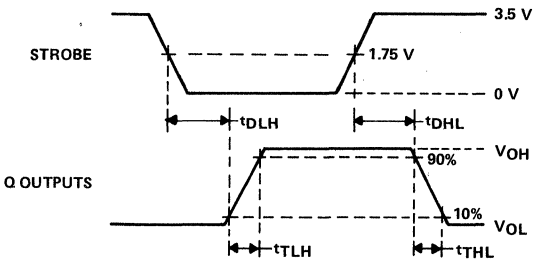


FIGURE 6. SWITCHING-TIME VOLTAGE WAVEFORMS

†For testing purposes, all input pulses have maximum rise and fall times of 30 ns.

D2743, MARCH 1983—REVISED OCTOBER 1989

- **Each Device Drives 32 Electrodes**
- **High-Voltage Open-Drain DMOS Outputs**
- **50-mA Output Current Capability**
- **CMOS-Compatible Inputs**
- **Very Low Steady-State Power Consumption**

description

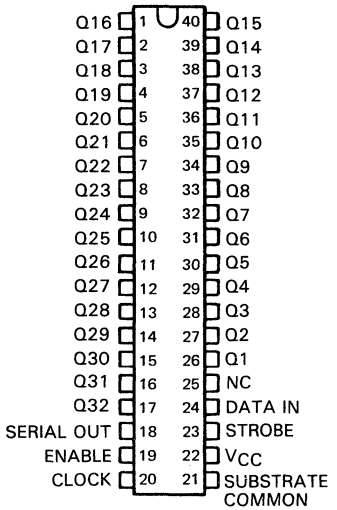
The SN65551, SN65552, SN75551, and SN75552 are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS-compatible and all outputs are high-voltage open-drain DMOS transistors. The SN75552 output sequence is reversed from the SN75551 for ease in printed circuit board layout.

The devices consist of a 32-bit shift register, 32 AND gates, and 32 output OR gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to the SUBSTRATE COMMON terminal. Serial data is entered into the shift register on the high-to-low transition of CLOCK. A high at the ENABLE input allows those outputs with a high in their associated register to be turned on causing the corresponding row to be connected to the composite row drive signal. When STROBE is low, all output transistors are turned on. The Serial Data output (SERIAL OUT) from the shift register may be used to cascade additional devices. This output is not affected by the ENABLE or STROBE inputs.

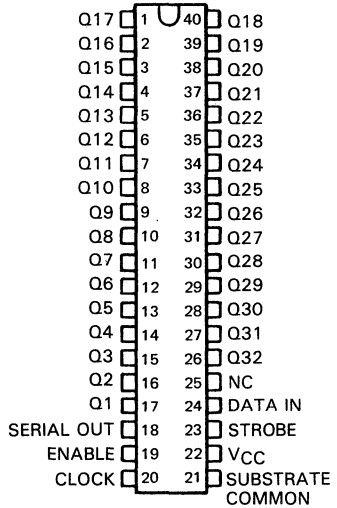
The SN65551 and SN65552 are characterized for operation from −40°C to 85°C. The SN75551 and SN75552 are characterized for operation from 0°C to 70°C.

N
DUAL-IN-LINE-PACKAGES
(TOP VIEW)

SN65551, SN75551



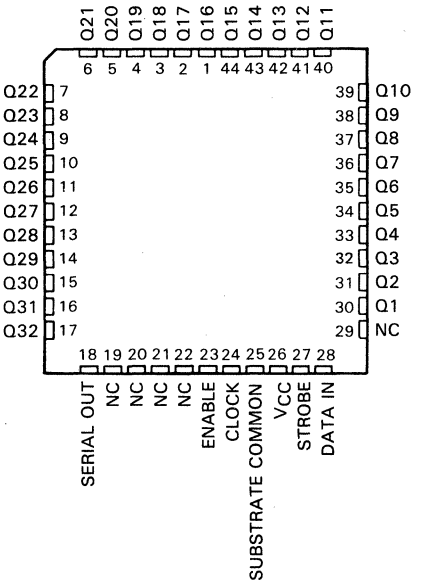
SN65552, SN75552



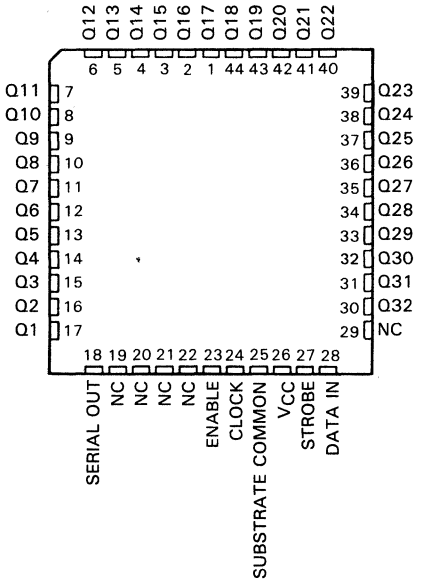
NC—No internal connection

† BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

SN65551, SN75551 . . . FN PACKAGE
(TOP VIEW)



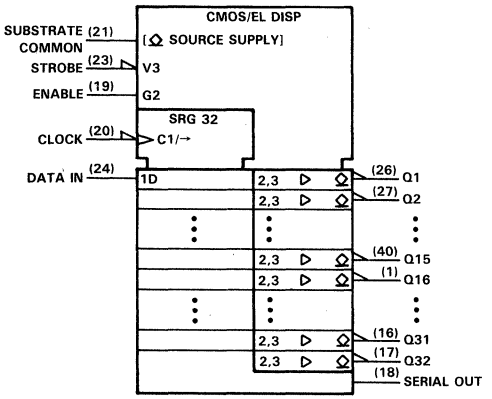
SN65552, SN75552 . . . FN PACKAGE
(TOP VIEW)



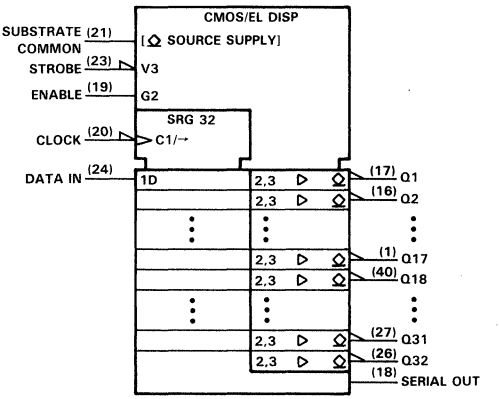
NC—No internal connection

logic symbols†

SN65551, SN75551

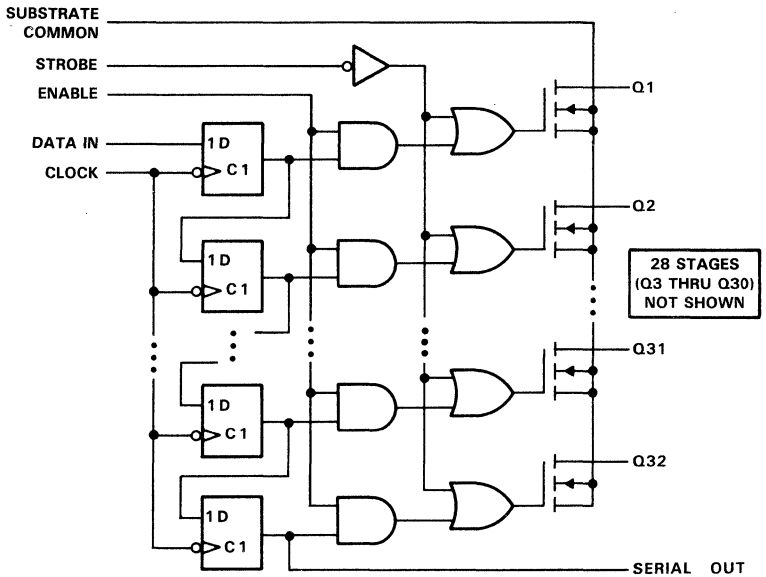


SN65552, SN75552



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. The symbol ◇ here indicates an n-channel open-drain output.
Pin numbers shown are for the N package.

logic diagram (positive logic)

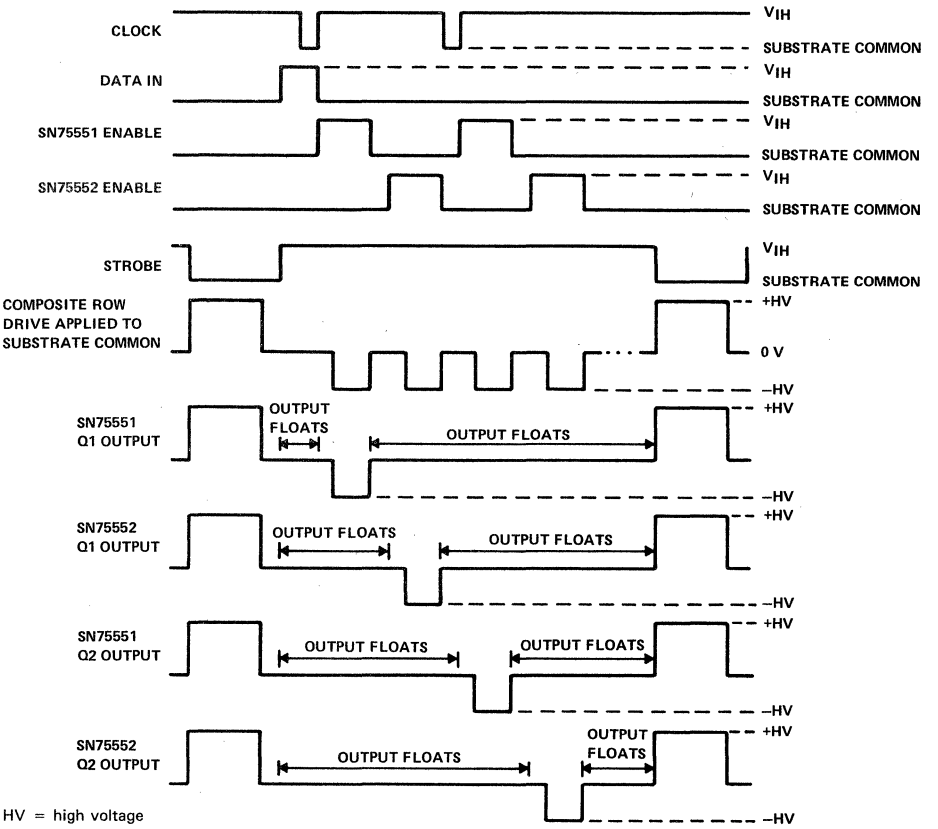


FUNCTION TABLE

FUNCTIONS	CONTROL INPUTS			SHIFT REGISTERS	OUTPUTS	
	CLOCK	ENABLE	STROBE	R1 THRU R32	SERIAL	Q1 THRU Q32
LOAD	↓	X	X	Load and Shift†	R32	Determined by ENABLE and STROBE
	No ↓	X	X	No Change	R32	Determined by ENABLE and STROBE
ENABLE	X	L	H	As determined above	R32	All Q outputs off
	X	H	H	As determined above	R32	Determined by R1 through R32
STROBE	X	X	L	As determined above	R32	All Q outputs on

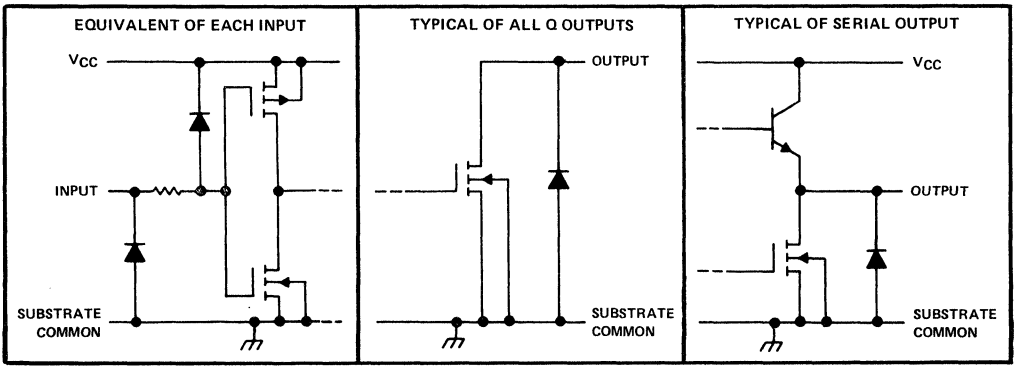
H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition.
†Register R32 takes on the state of R31, R31 takes on the state of R30,. . .R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



NOTE: During operation CLOCK, DATA IN, ENABLE, and STROBE are referenced to the Composite Row Drive signal received at the SUBSTRATE COMMON pin of the device.

schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Off-state Q output voltage, $V_{O(off)}$ . . . . . 225 V
Input voltage . . . . . $V_{CC}+0.3$ V
Substrate common terminal current (see Note 2) . . . . . 1.5 A
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN65551, SN65552 . . . . . −40°C to 85°C
SN75551, SN75552 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values are with respect to SUBSTRATE COMMON terminal.
2. Duty cycle is limited by package dissipation.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1700 mW	13.6 mW/°C	1088 mW	884 mW
N	1250 mW	10.0 mW/°C	800 mW	650 mW

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			10.8	12	15	V
V_{IH}	High-level input voltage (see Figure 1)		V_{CC} = 10.8 V	8.1		11.1	V
			V_{CC} = 15 V	11.25		15.3	
V_{IL}	Low-level input voltage (see Figure 1)		V_{CC} = 10.8 V	−0.3		2.7	V
			V_{CC} = 15 V	−0.3		3.75	
$V_{O(off)}$	Off-state Q output voltage			0		200	V
$I_{O(on)}$	On-state output current, duty cycle ≤ 1%, (see Figures 2, 3, and 4)		V_{CC} = 10.8 V, T_A = 25°C			50	mA
			V_{CC} = 15 V, T_A = 25°C			80	
I_{OK}	Output clamp current					−45	mA
f_{clock}	Clock frequency			0		4	MHz
t_w	Pulse duration, CLOCK high or low			125			ns
t_{su}	Setup time, DATA IN before CLOCK (see Figure 5)			50			ns
t_h	Hold time, DATA IN after CLOCK (see Figure 5)			100			ns
T_A	Operating free-air temperature	SN65551, SN65552		−40		85	°C
		SN75551, SN75552		0		70	

electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$I_{O(off)}$	Off-state Q output current		V_O = 200 V		10	μA
V_{OH}	High-level output voltage	Serial outputs	I_O = −100 μA	V_{CC}−1.5		V
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 50 mA, See Figure 3		30	V
		Serial output	I_{OL} = 100 μA		1	
I_{IH}	High-level input current		V_I @ V_{CC}		1	μA
I_{IL}	Low-level input current		V_I = 0		−1	μA
I_{CC}	Supply current from V_{CC}				250	μA

switching characteristics, V_{CC} = 12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level SERIAL OUTPUT from CLOCK	C_L = 20 pF to ground, See Figure 6		200	ns
t_{PLH}	Propagation delay time, low-to-high level SERIAL OUTPUT from CLOCK			200	ns
$t_{d(on)}$	Turn-on delay time, Q outputs from ENABLE	I_{OL} = 50 mA, STROBE at V_{CC}, R_L = 1.4 kΩ to 100 V, See Figure 7		500	ns

RECOMMENDED OPERATING CONDITIONS

INPUT VOLTAGE LOGIC-LEVEL LIMITS
vs
SUPPLY VOLTAGE

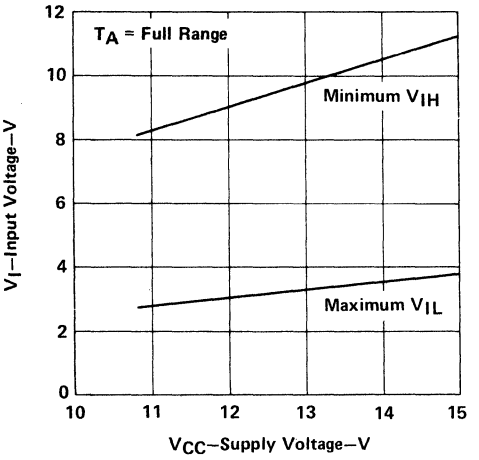


FIGURE 1

MAXIMUM ON-STATE Q OUTPUT CURRENT
vs
SUPPLY VOLTAGE

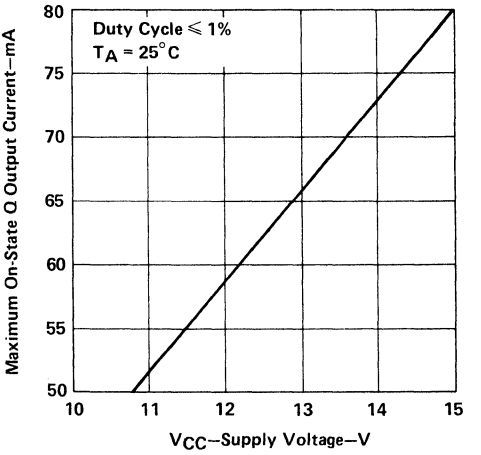
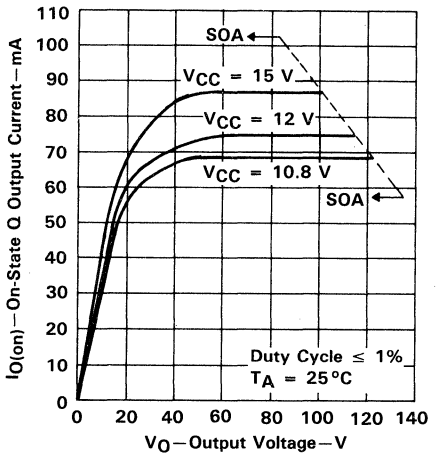


FIGURE 2

TYPICAL CHARACTERISTICS

ON-STATE Q OUTPUT CURRENT
vs
OUTPUT VOLTAGE



SOA = Safe Operating Area

FIGURE 3

OUTPUT SATURATION CURRENT
vs
FREE-AIR TEMPERATURE†

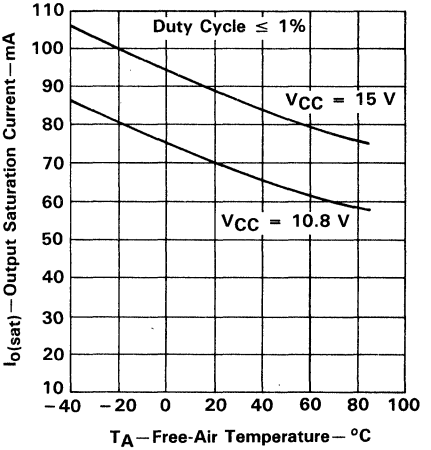


FIGURE 4

† Data for temperatures below 0°C and above 70°C apply only for SN65551 and SN65552.

PARAMETER MEASUREMENT INFORMATION

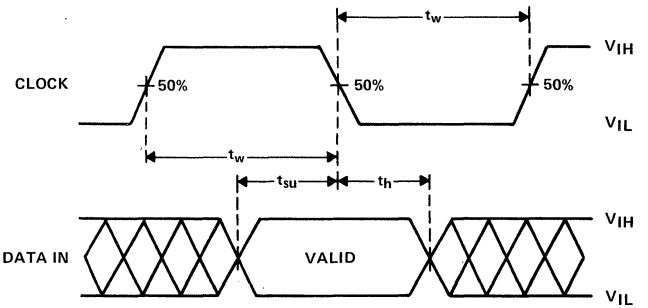


FIGURE 5. INPUT TIMING VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION

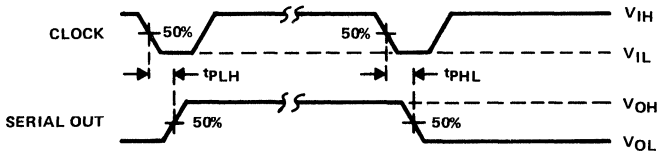


FIGURE 6. VOLTAGE WAVEFORMS, SERIAL OUTPUT

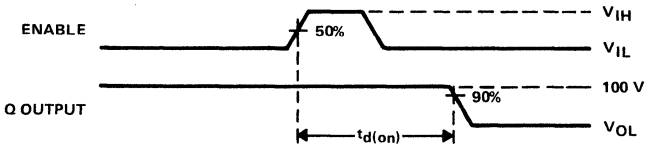


FIGURE 7. VOLTAGE WAVEFORMS, Q OUTPUT

D2744, MARCH 1983—REVISED DECEMBER 1989

- **Each Device Drives 32 Electrodes**
- **60-V Output Voltage Swing Capability**
- **15-mA Output Source and Sink Current Capability**
- **High-Speed Serially-Shifted Data Input**
- **Totem-Pole Outputs**
- **Latches on All Driver Outputs**

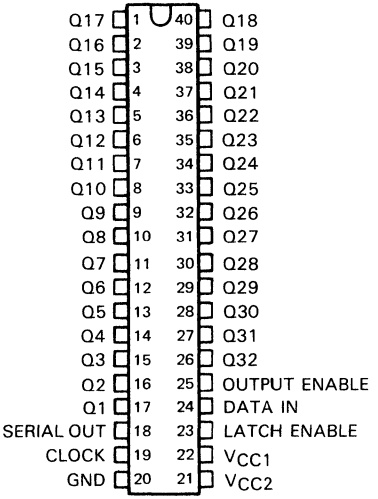
description

The SN65553, SN65554, SN75553, and SN75554 are monolithic BIDFET† integrated circuits designed to drive the column electrodes of an electroluminescent display. The SN65554 and SN75554 output sequence is reversed from the SN65553 and SN75553 for ease in printed circuit board layout.

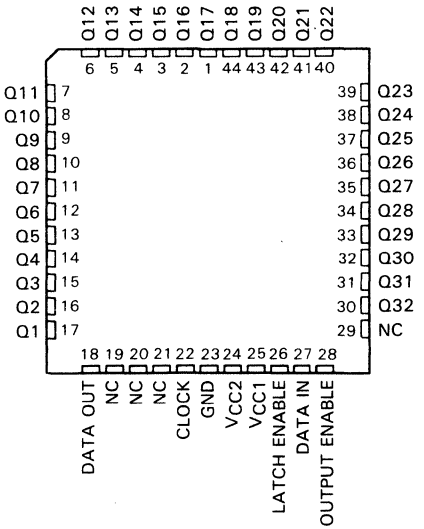
The devices consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. When high, LATCH ENABLE transfers the shift register contents to the outputs of the 32 latches. When OUTPUT ENABLE is high, all Q outputs are enabled. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by LATCH ENABLE or OUTPUT ENABLE.

The SN65553 and SN65554 are characterized for operation from −40°C to 85°C. The SN75553 and SN75554 are characterized for operation from 0°C to 70°C.

N PACKAGE
(TOP VIEW)
SN65553, SN75553



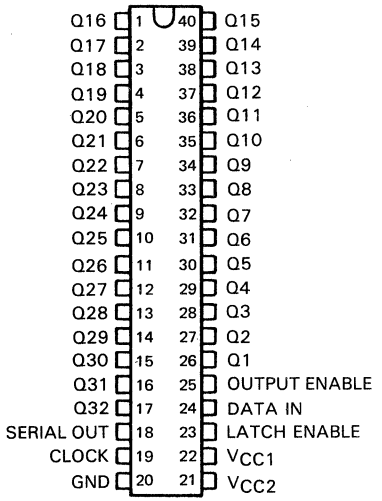
FN PACKAGE
(TOP VIEW)
SN65553, SN75553



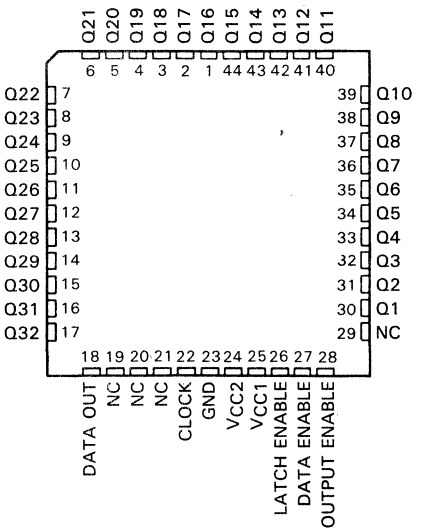
NC—No internal connection

†BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

N PACKAGE
(TOP VIEW)
SN65554, SN75554



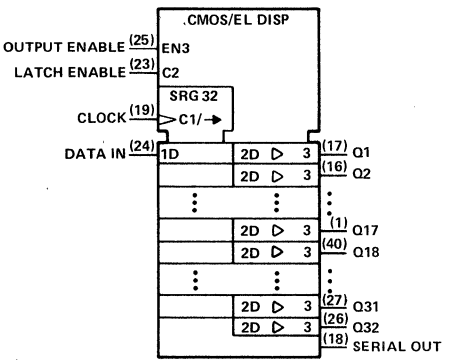
FN PACKAGE
(TOP VIEW)
SN65554, SN75554



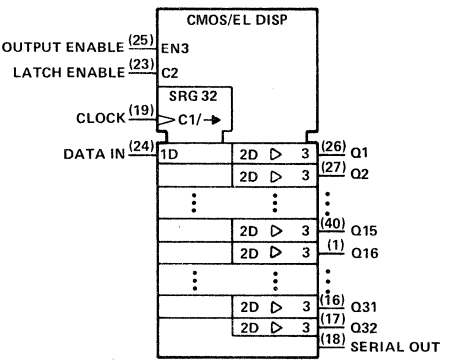
NC—No internal connection

logic symbols†

SN65553, SN75553

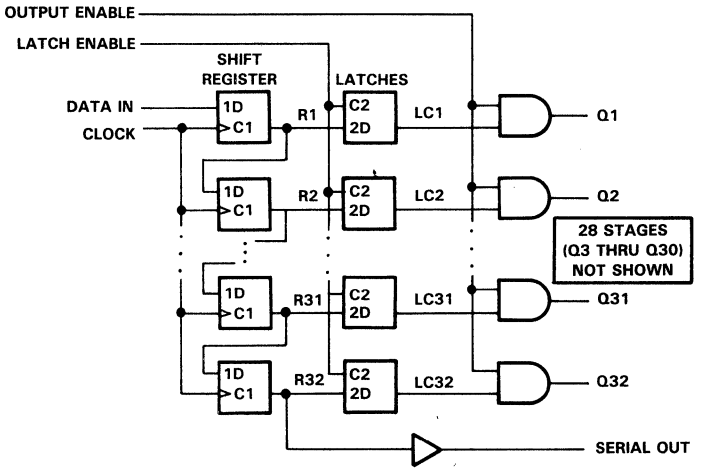


SN65554, SN75554



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for N packages.

logic diagram (positive logic)



FUNCTION TABLE

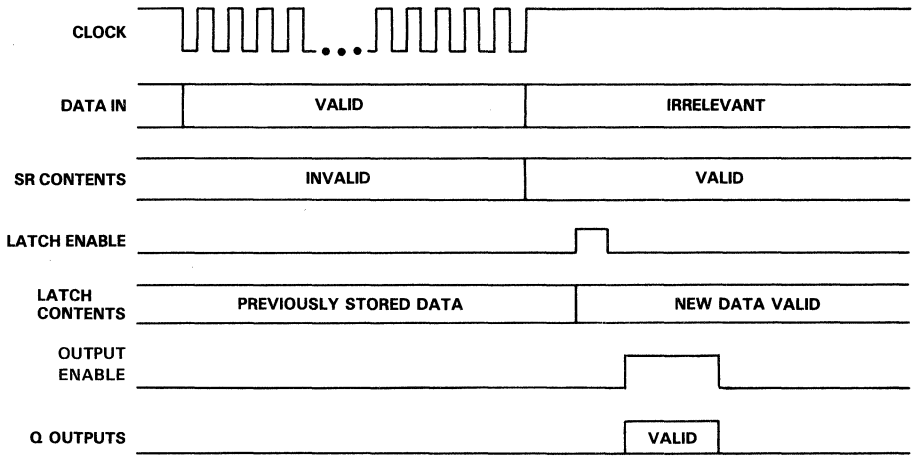
FUNCTION	CONTROL INPUTS			SHIFT REGISTER	LATCHES	OUTPUTS	
	CLOCK	LATCH ENABLE	OUTPUT ENABLE	R1 THRU R32	LC1 THRU LC32	SERIAL	Q1 THRU Q22
LOAD	↑	X	X	Load and shift†	Determined by	R32	Determined by
	No↑	X	X	No change	LATCH ENABLE‡	R32	OUTPUT ENABLE
LATCH	X	L	X	As determined	Stored data	R32	Determined by
	X	H	X	above	New data	R32	OUTPUT ENABLE
OUTPUT	X	X	L	As determined	Determined by	R32	All L
ENABLE	X	X	H	above	LATCH ENABLE‡	R32	LC1 thru LC32, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.

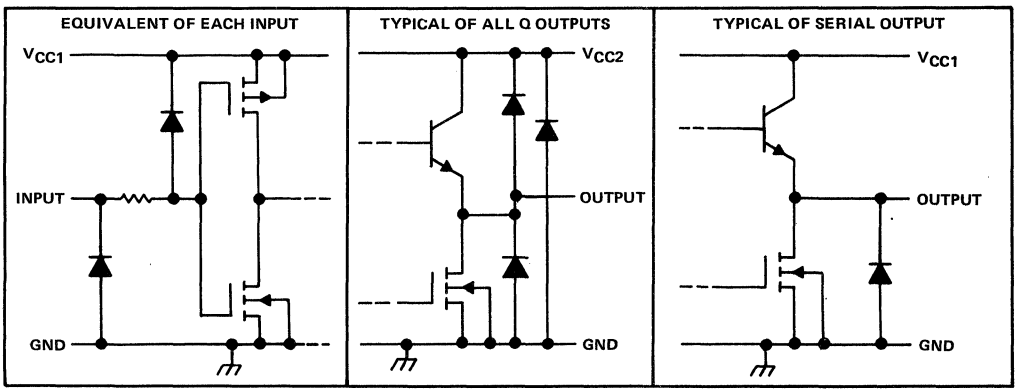
†R32 and the serial output take on the state of R31, R31 takes on the state of R30, . . .R2 takes on the state of R1, and R1 takes on the state of the data input.

‡New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematic of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC2} . . . . . 70 V
Input voltage . . . . . V_{CC1} + 0.3 V
Ground current . . . . . 700 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN65553, SN65554 . . . . . −40°C to 85°C
SN75553, SN75554 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1700 mW	13.6 mW/°C	1088 mW	884 mW
N	1250 mW	10.0 mW/°C	800 mW	650 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	15	V
Supply voltage, V_{CC2}		0		60	V
High-level input voltage, V_{IH} (see Figure 1)	V_{CC1} = 10.8 V	8.1		11.1	V
	V_{CC1} = 15 V	11.25		15.3	
Low-level input voltage, V_{IL} (see Figure 1)	V_{CC1} = 10.8 V	−0.3		2.7	V
	V_{CC1} = 15 V	−0.3		3.75	
High-level output current, I_{OH}		−15			mA
Low-level output current, I_{OL}		15			mA
Output clamp current, I_{OK}				20	mA
Clock frequency, f_{clock}		0		6.25	MHz
Pulse duration, CLOCK high or low, $t_{w(CLK)}$ (see Figure 2)		80			ns
Pulse duration, LATCH ENABLE, $t_{w(LE)}$ (see Figure 4)		80			ns
Data setup time before CLOCK ↑, t_{su} (see Figure 2)		20			ns
Data hold time after CLOCK ↑, t_h (see Figure 2)		80			ns
Operating free-air temperature, T_A	SN65553, SN65554	−40		85	°C
	SN75553, SN75554	0		70	

electrical characteristics over recommended ranges of V_{CC1} and operating free-air temperature, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_O = −15 mA	57		V
		SERIAL OUT	I_O = −100 μA	V_{CC1}−1.5		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 15 mA		8	V
		SERIAL OUT	I_{OL} = 100 μA		1	
I_{IH}	High-level input current		$V_I = V_{CC1}$		1	μA
I_{IL}	Low-level input current		V_I = 0		−1	μA
I_{CC1}	Supply current from V_{CC1}				5	mA
I_{CC2}	Supply current from V_{CC2}	SN65553, SN65554			12	mA
		SN75553, SN75554			10	

switching characteristics, V_{CC1} = 12 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level SERIAL OUT from CLOCK	C_L = 20 pF to ground, See Figure 3		140	ns
t_{PLH}	Propagation delay time, low-to-high-level SERIAL OUT from CLOCK			140	ns
t_{DHL}	Delay time, high-to-low-level Q output from LATCH ENABLE	C_L = 20 pF to ground, See Figure 4		500	ns
t_{DLH}	Delay time, low-to-high-level Q output from LATCH ENABLE	C_L = 20 pF to ground, See Figure 4		1	μs

RECOMMENDED OPERATION CONDITIONS

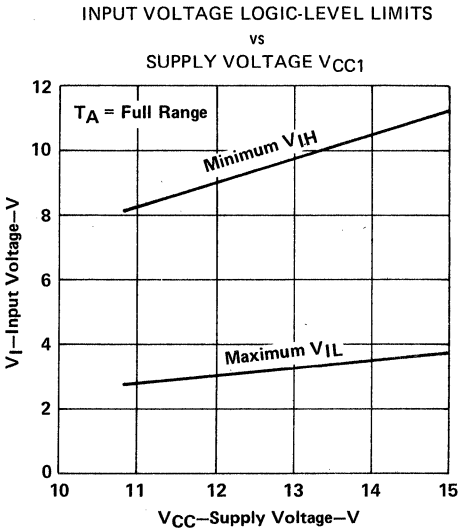


FIGURE 1

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

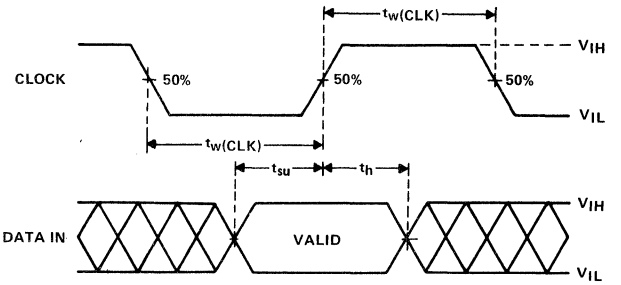


FIGURE 2. INPUT TIMING VOLTAGE WAVEFORMS

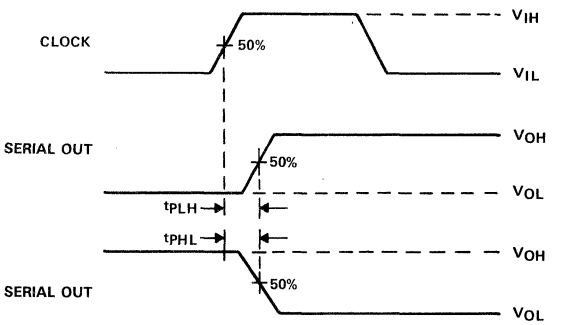


FIGURE 3. VOLTAGE WAVEFORMS FOR PROPAGATION DELAY CLOCK TO SERIAL OUTPUT

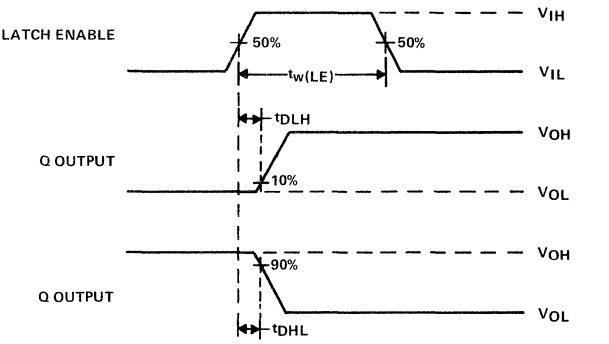


FIGURE 4. VOLTAGE WAVEFORMS FOR DELAY TIMES, LATCH ENABLE TO Q OUTPUTS

D2744, APRIL 1985—REVISED JULY 1990

- **Each Device Drives 32 Electrodes**
- **90-V Output Voltage Swing Capability Using Ramped Supply**
- **15-mA Output Source and Sink Current Capability**
- **High-Speed Serially-Shifted Data Input**
- **Totem-Pole Outputs**
- **Latches on All Driver Outputs**

description

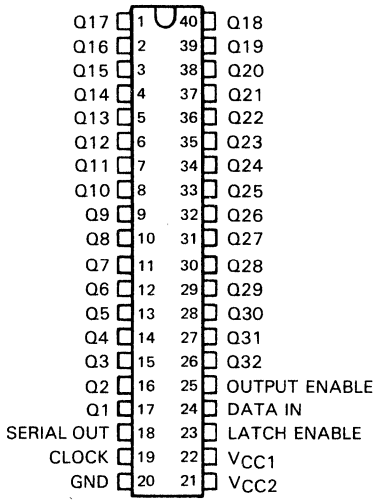
The SN65555, SN75555, SN65556, and SN75556 are monolithic BIDFET† integrated circuits designed to drive the column electrodes of an electro-luminescent display. The SN65556 and SN75556 output sequence is reversed from the SN65555 and SN75555 for ease in printed circuit board layout.

The devices consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. When high, LATCH ENABLE transfers the shift register contents to the outputs of the 32 latches. When OUTPUT ENABLE is high, all Q outputs are enabled. Data must be loaded into the latches and OUTPUT ENABLE must be high before supply voltage V_{CC2} is ramped up.

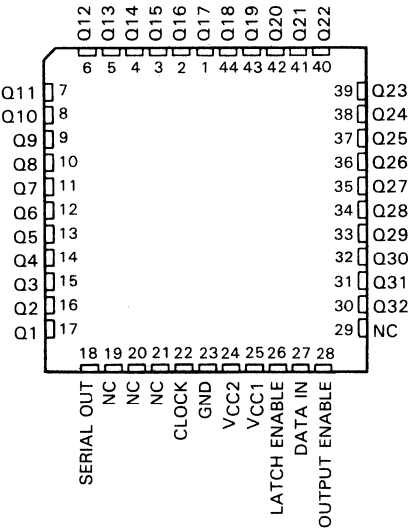
Serial data output from the shift register may be used to cascade shift registers. This output is not affected by LATCH ENABLE or OUTPUT ENABLE.

The SN65555 and SN65556 are characterized for operation from −40°C to 85°C. The SN75555 and SN75556 are characterized for operation from 0°C to 70°C.

SN65555, SN75555
N PACKAGE
(TOP VIEW)



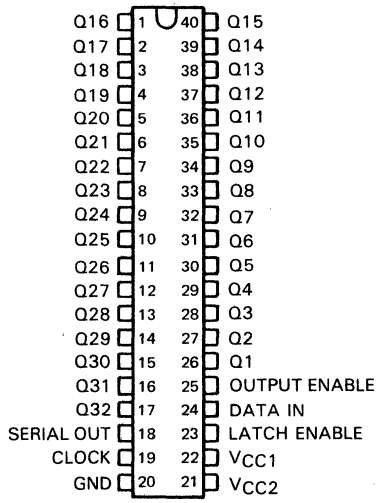
SN65555, SN75555
FN PACKAGE
(TOP VIEW)



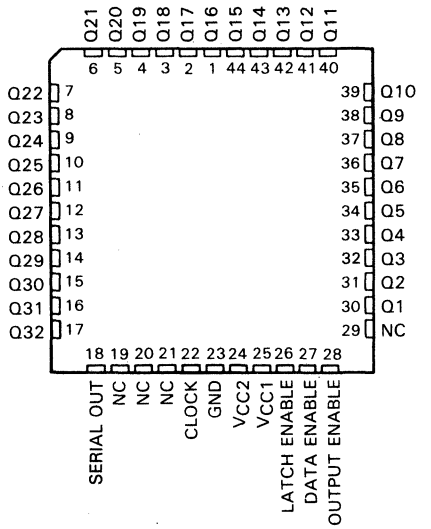
NC—No internal connection

†BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

SN65556, SN75556
N PACKAGE
(TOP VIEW)



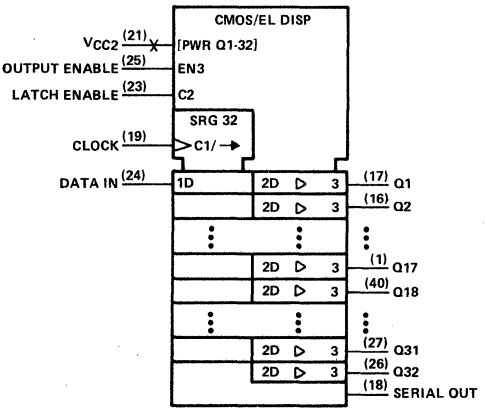
SN65556, SN75556
FN PACKAGE
(TOP VIEW)



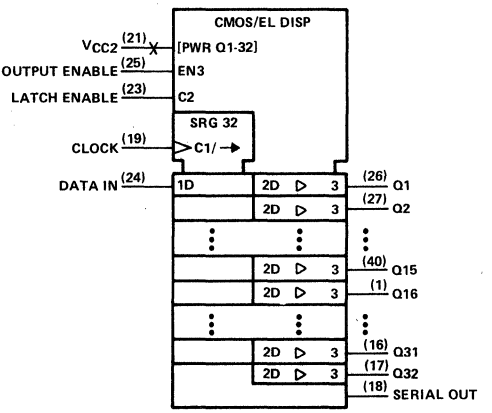
NC—No internal connection

logic symbols†

SN65555, SN75555

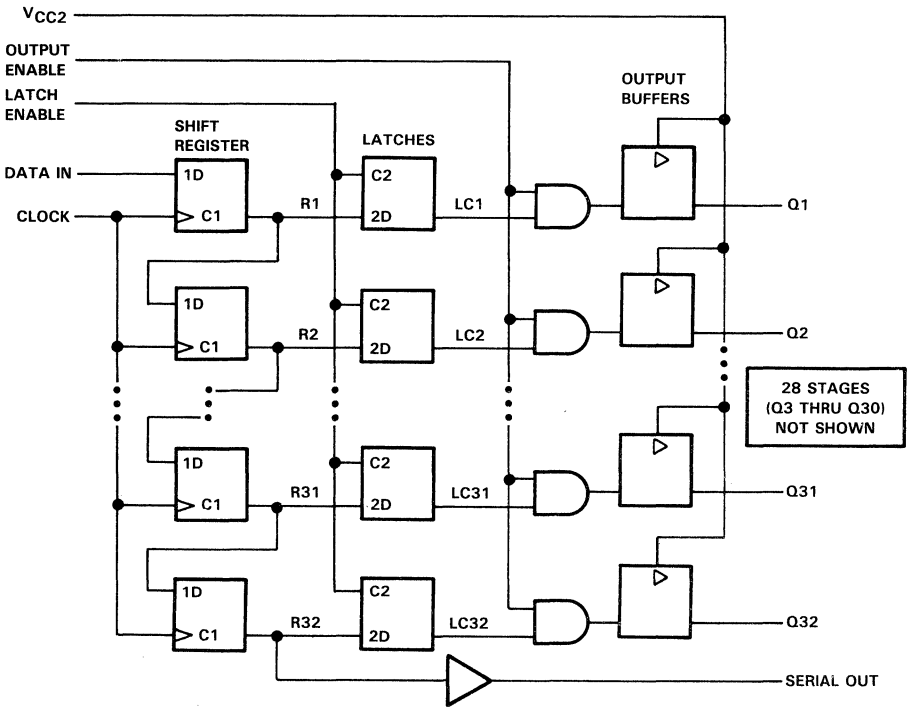


SN65556, SN75556



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for N packages.

logic diagram (positive logic)

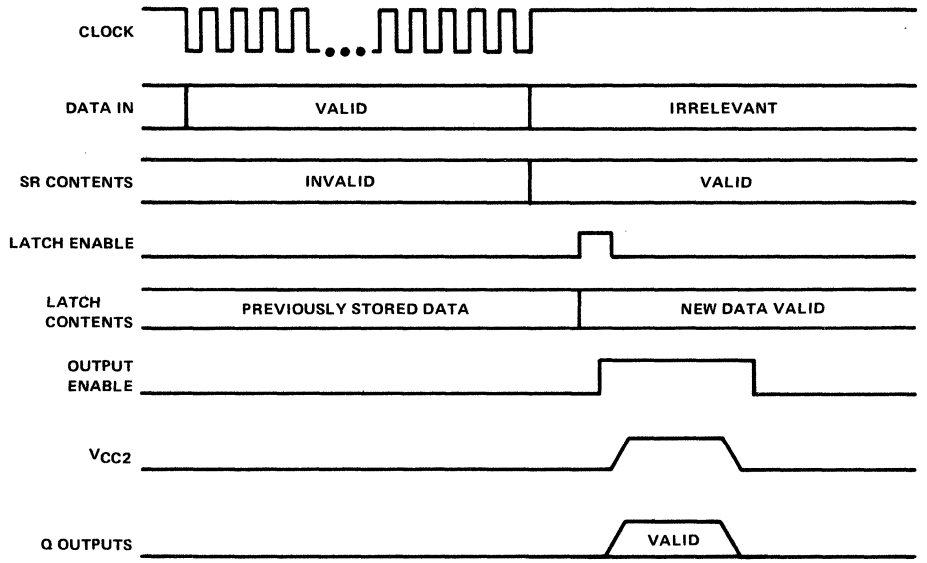


FUNCTION TABLE

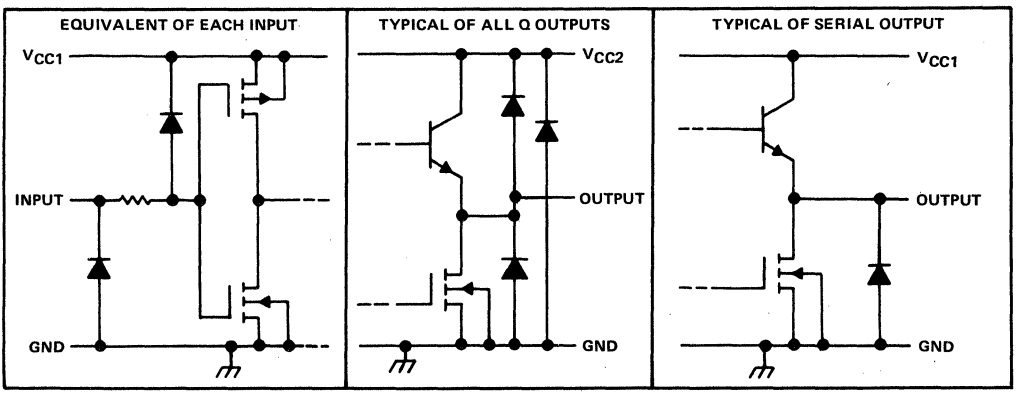
FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R32	LATCHES LC1 THRU LC32	OUTPUTS	
	CLOCK	LATCH ENABLE	OUTPUT ENABLE			SERIAL	Q1 THRU Q32
LOAD	↑	X	X	Load and shift†	Determined by LATCH ENABLE‡	R32	Determined by OUTPUT ENABLE
	No↑	X	X	No change		R32	
LATCH	X	L	X	As determined above	Stored data	R32	Determined by OUTPUT ENABLE
	X	H	X		New data	R32	
OUTPUT ENABLE	X	X	L	As determined above	Determined by LATCH ENABLE‡	R32	All L
	X	X	H			R32	LC1 thru LC32, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
†R32 and the serial output take on the state of R31, R31 takes on the state of R30,. . .R2 takes on the state of R1, and R1 takes on the state of the data input.
‡New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematic of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC2} (see Note 2) . . . . . 90 V
Input voltage . . . . . V_{CC1} + 0.3 V
Ground current . . . . . 700 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN65555, SN65556 . . . . . −40°C to 85°C
SN75555, SN75556 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. These devices have been designed to be used in applications in which the high-voltage supply, V_{CC2}, is switched to ground before changing the state of the outputs.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1700 mW	13.6 mW/°C	1088 mW	884 mW
N	1250 mW	10.0 mW/°C	800 mW	650 mW

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage		10.8	12	15	V
V_{CC2}	Supply voltage		0		80	V
V_{IH}	High-level input voltage (see Figure 1)	V_{CC1} = 10.8 V	8.1		11.1	V
		V_{CC1} = 15 V	11.25		15.3	
V_{IL}	Low-level input voltage (see Figure 1)	V_{CC1} = 10.8 V	−0.3†		2.7	V
		V_{CC1} = 15 V	−0.3†		3.75	
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current				15	mA
I_{OK}	Output clamp current				20	mA
f_{clock}	Clock frequency		0		6.25	MHz
$t_{w(CLK)}$	Pulse duration, CLOCK high or low (see Figure 2)		80			ns
$t_{w(LE)}$	Pulse duration, LATCH ENABLE		80			ns
t_{su}	Setup time	DATA IN before CLOCK↑ (see Figure 2)	20			ns
		OUTPUT ENABLE before V_{CC2}↑ (see Figure 4)	500			
t_h	Hold time	DATA IN after CLOCK↑ (see Figure 2)	80			ns
		OUTPUT ENABLE after V_{CC2}↑ (see Figure 4)	100			
dv/dt	Rate of rise for V_{CC2}				80	V/μs
T_A	Operating free-air temperature	SN65555, SN65556	−40		85	°C
		SN75555, SN75556	0		70	

†The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over recommended operating free-air temperature range, V_{CC1} = 12 V, V_{CC2} = 80 V

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_O = −15 mA	77		V
		SERIAL OUT	I_O = −100 μA	10.5		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 15 mA		8	V
		SERIAL OUT	I_{OL} = 100 μA		1	
I_{IH}	High-level input current		V_I = 12 V		1	μA
I_{IL}	Low-level input current		V_I = 0		−1	μA
I_{CC1}	Supply current from V_{CC1}				2	mA
I_{CC2}	Supply current from V_{CC2}				5	mA

switching characteristics, V_{CC1} = 12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level SERIAL OUT from CLOCK	C_L = 20 pF to ground, V_{CC2} = 0, See Figure 3		140	ns
t_{PLH}	Propagation delay time, low-to-high-level SERIAL OUT from CLOCK			140	ns
t_d	Delay time, V_{CC2} to Q outputs	dv/dt = 80 V/μs, See Figure 4		100	ns

RECOMMENDED OPERATION CONDITIONS

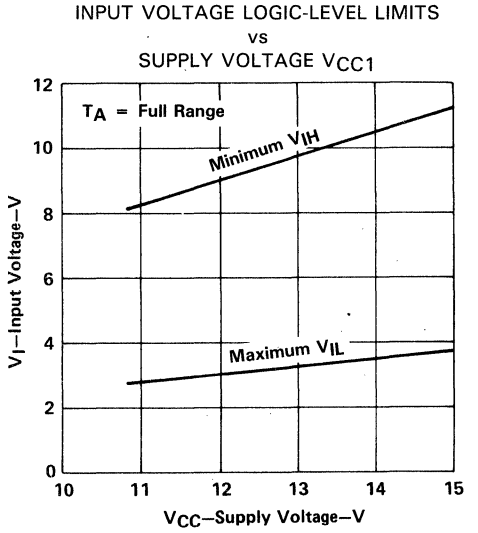


FIGURE 1

PARAMETER MEASUREMENT INFORMATION

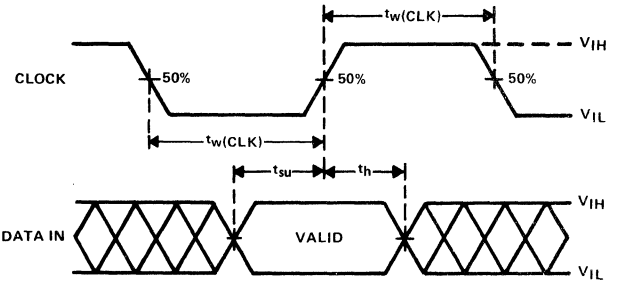


FIGURE 2. INPUT TIMING VOLTAGE WAVEFORMS

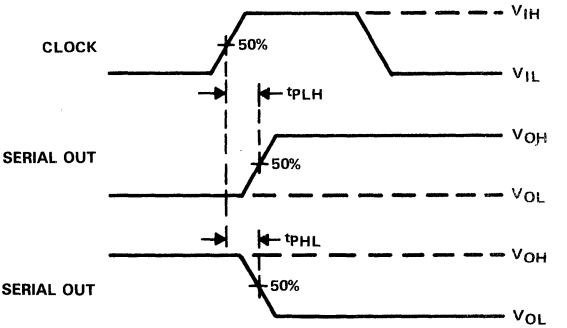


FIGURE 3. VOLTAGE WAVEFORMS FOR PROPAGATION DELAY CLOCK TO SERIAL OUTPUT

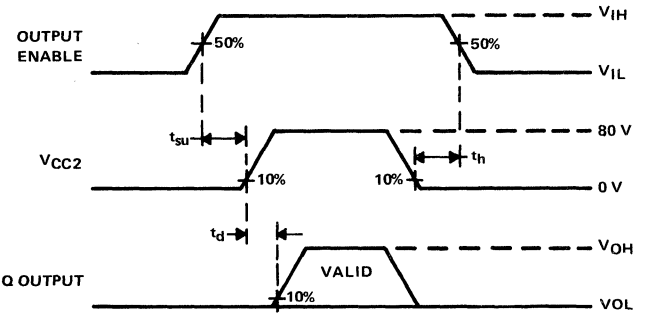


FIGURE 4. VOLTAGE WAVEFORMS FOR DELAY TIMES, V_{CC2} TO Q OUTPUTS

D2999, DECEMBER 1985—REVISED OCTOBER 1989

- **Each Device Drives 32 Electrodes**
- **High-Voltage Open-Collector N-P-N Outputs Using Ramped Supply**
- **300-mA Output Current Capability**
- **CMOS-Compatible Inputs**
- **Very Low Steady-State Power Consumption**

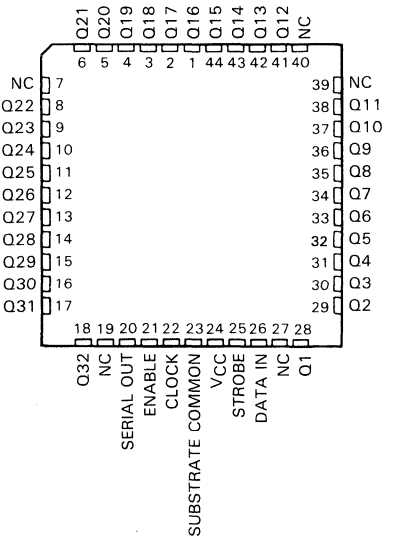
description

These devices are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS-compatible and all outputs are high-voltage open-collector n-p-n transistors. The SN65558 and SN75558 output sequences are reversed from the SN65557 and SN75557 for ease in printed circuit board layout.

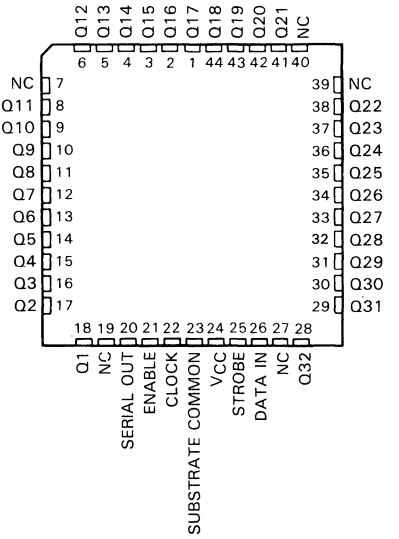
The devices consist of a 32-bit shift register, 32 AND gates, and 32 output OR gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to the SUBSTRATE COMMON terminal. Serial data is entered into the shift register on the high-to-low transition of the clock input. A high ENABLE allows those outputs with a high in their associated register to be turned on causing the corresponding row to be connected to the composite row drive signal. When STROBE is low, all output transistors are turned on. The Serial Data output (SERIAL OUT) from the shift register may be used to cascade additional devices. This output is not affected by the ENABLE or STROBE inputs.

The SN65557 and SN65558 are characterized for operation from −40°C to 85°C. The SN75557 and SN75558 are characterized for operation from 0°C to 70°C.

SN65557, SN75557 . . . FN PACKAGE
(TOP VIEW)



SN65558, SN75558 . . . FN PACKAGE
(TOP VIEW)

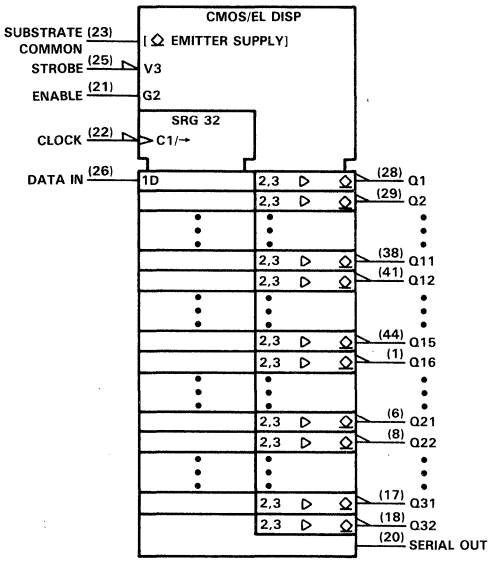


NC—No internal connection

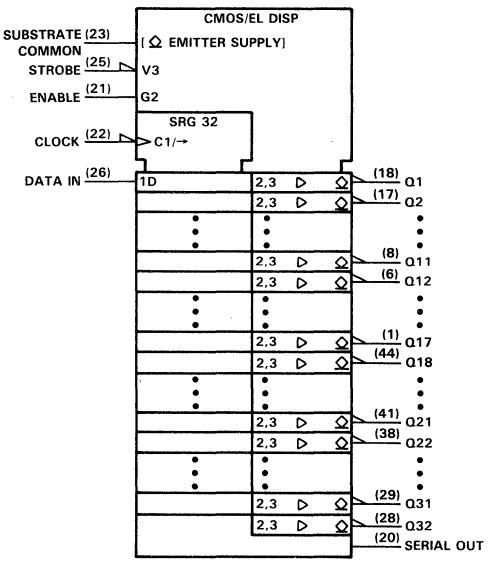
† BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process

logic symbols†

SN65557, SN75557

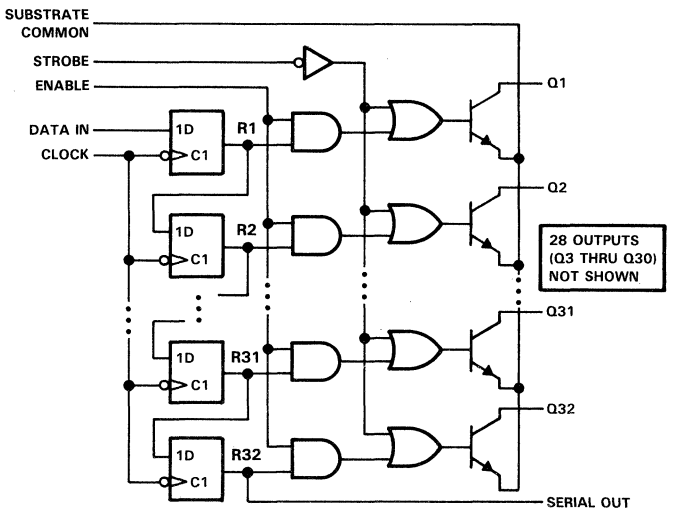


SN65558, SN75558



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

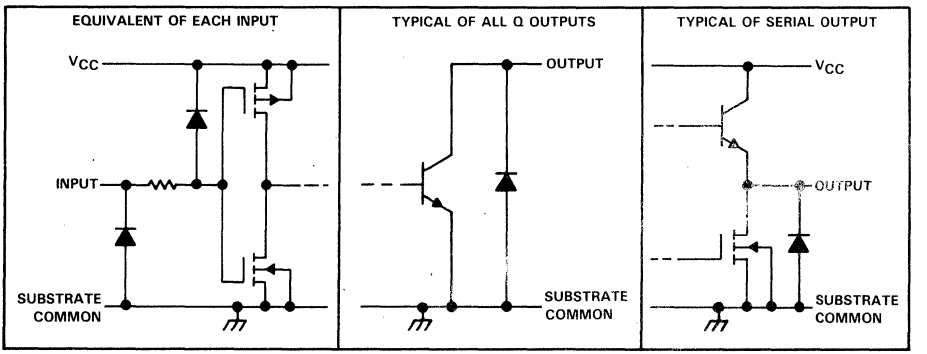


FUNCTION TABLE

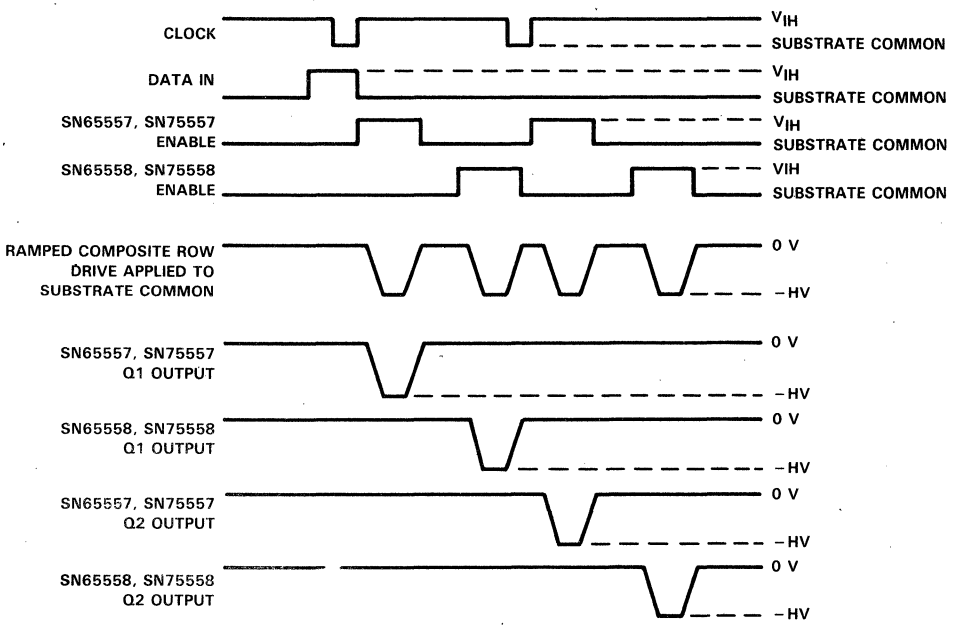
FUNCTION	CONTROL INPUTS			SHIFT REGISTERS	OUTPUTS	
	CLOCK	ENABLE	STROBE	R1 THRU R32	SERIAL	Q1 THRU Q32
LOAD	↓	X	X	Load and Shift†	R32	Determined by ENABLE and STROBE
	No ↓	X	X	No Change	R32	Determined by ENABLE and STROBE
ENABLE	X	L	H	As determined above	R32	All Q outputs off
	X	H	H	As determined above	R32	Determined by R1 through R32
STROBE	X	X	L	As determined above	R32	All Q outputs on

H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition.
†Register R32 takes on the state of R31, R31 takes on the state of R30, . . .R2 takes on the state of R1, and R1 takes on the state of the data input.

schematics of inputs and outputs



typical operating sequence



HV = High voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Off-state output voltage, $V_{O(off)}$ (see Note 2) . . . . . 110 V
Input voltage . . . . . $V_{CC}+0.3$ V
Substrate common terminal current (see Note 3) . . . . . 750 mA
Continuous total power dissipation at (or below)
25°C free-air temperature (see Note 4) . . . . . 1700 mW
Operating free-air temperature range: SN65557, SN65558 . . . . . −40°C to 85°C
SN75557, SN75558 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to SUBSTRATE COMMON terminal.
2. Data must be clocked into the shift register and Q outputs enabled prior to ramping SUBSTRATE COMMON to −HV (see typical operating sequence).
3. Duty cycle is limited by package dissipation.
4. For operation above 25°C free-air temperature, derate linearly to 1088 mW at 70°C, and 884 mW at 85°C at the rate of 13.6 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		10.8	12	15	V
High-level input voltage, V_{IH} (see Figure 1)	V_{CC} = 10.8 V	8.1		11.1	V
	V_{CC} = 15 V	11.25		15.3	
Low-level input voltage, V_{IL} (see Figure 1)	V_{CC} = 10.8 V	−0.3		2.7	V
	V_{CC} = 15 V	−0.3		3.75	
Off-state Q output voltage, $V_{O(off)}$		−0.3		100	V
On-state Q output current, $I_{O(on)}$, duty cycle ≤ 1%, V_{CC} = 15 V				300	mA
Rate of rise for SUBSTRATE COMMON, dV/dt (see Figure 4)				100	V/μs
Clock frequency, f_{clock}		0		4	MHz
Pulse duration, CLOCK high or low, t_w		125			ns
Setup time, t_{su}	DATA IN before CLOCK↓ (see Figure 2)	50			ns
	ENABLE before SUBSTRATE COMMON ↓ (see Figure 4)	500			
Hold time, t_h, DATA IN after CLOCK↓ (see Figure 2)		100			ns
Operating free-air temperature, T_A	SN65557, SN65558	−40		85	°C
	SN75557, SN75558	0		70	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 12 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN65557 SN65558		SN75557 SN75558		UNIT
				MIN	MAX	MIN	MAX	
$I_{O(off)}$	Off-state Q output current		V_O = 100 V		20		10	μA
V_{OH}	High-level output voltage	Serial outputs	I_O = −100 μA	10.5		10.5		V
V_{VOL}	Low-level output voltage	Q outputs	I_{OL} = 300 mA		20		10	V
		Serial output	I_{OL} = 100 μA		1		1	
I_{IH}	High-level input current		V_I = 12 V		1		1	μA
I_{IL}	Low-level input current		V_I = 0		−1		−1	μA
I_{CC}	Supply current from V_{CC}				250		250	μA

switching characteristics, V_{CC} = 12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level SERIAL OUTPUT from CLOCK	C_L = 20 pF to SUBSTRATE COMMON (see Figure 3)		200	ns
t_{PLH}	Propagation delay time, low-to-high-level SERIAL OUTPUT from CLOCK			200	ns
$t_{d(on)}$	Turn-on delay time, Q outputs from ENABLE	dV/dt = 100 V/μs, STROBE at V_{CC}, R_L = 2 kΩ to 60 V (see Figure 4)		500	ns

RECOMMENDED OPERATING CONDITIONS

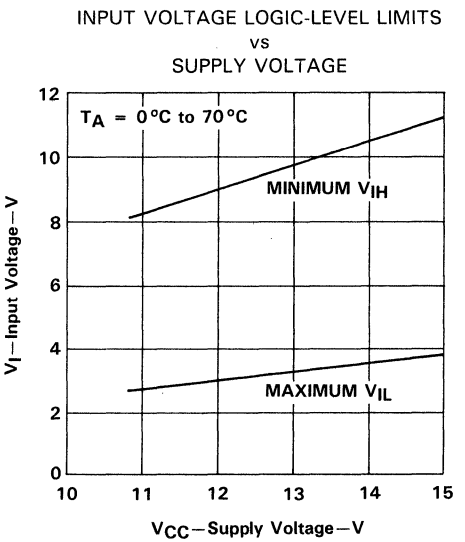


FIGURE 1

TEXAS INSTRUMENTS
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PARAMETER MEASUREMENT INFORMATION

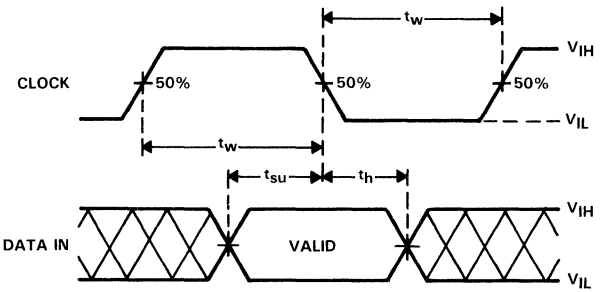


FIGURE 2. INPUT TIMING VOLTAGE WAVEFORMS

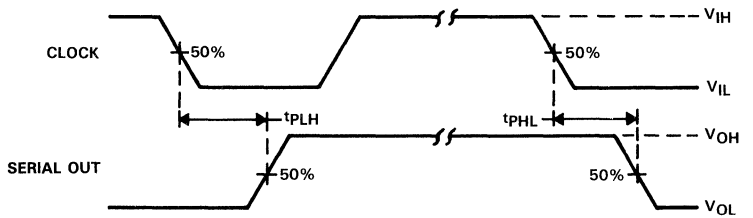


FIGURE 3. VOLTAGE WAVEFORMS FOR PROPAGATION DELAY TIMES, CLOCK TO DATA OUT

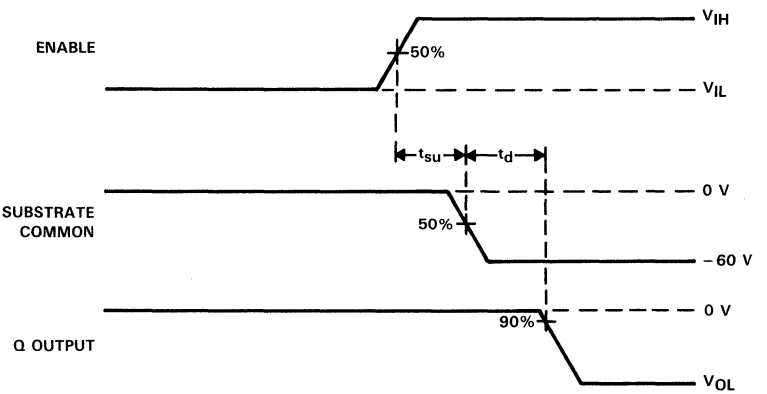


FIGURE 4. VOLTAGE WAVEFORMS FOR TURN ON DELAY TIME, SUBSTRATE COMMON TO Q OUTPUT

TYPICAL CHARACTERISTICS

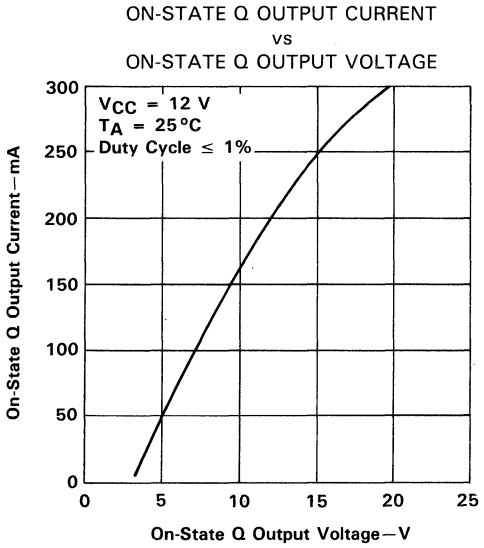
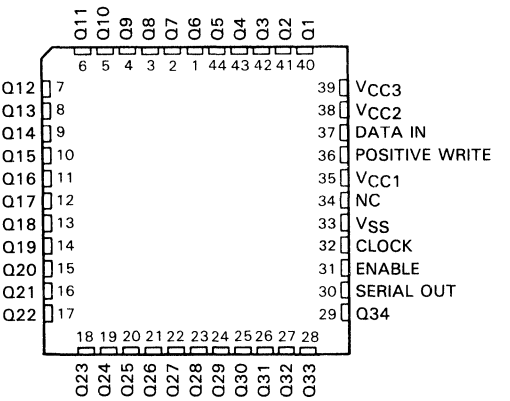


FIGURE 5

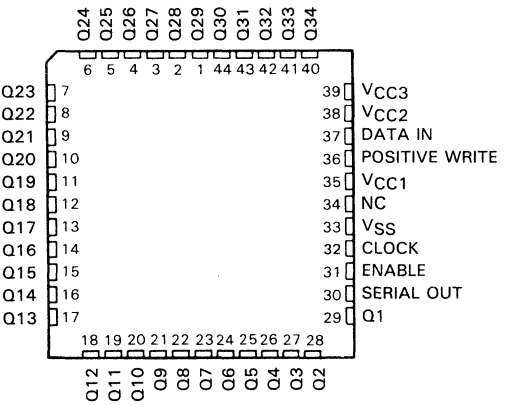
D3223, MAY 1986—REVISED DECEMBER 1989

- **Each Device Drives 34 Electrodes**
- **Selectable Open-Source or Open-Drain Output**
- **Outputs Rated at 240 V**
- **Output Current Capability:**
  – 150 mA to 100 mA (SN65')
  – 150 mA to 120 mA (SN75')
- **CMOS-Compatible Inputs**
- **Very Low Steady-State Power Consumption**

SN65563A, SN75563A . . . FN PACKAGE
(TOP VIEW)



SN65564A, SN75564A . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN65563A, SN65564A, SN75563A, and SN75564A are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS compatible. If POSITIVE WRITE is high, the Q outputs act like open-source outputs and output data is not inverted with respect to input data. If POSITIVE WRITE is low, the Q outputs act like open-drain outputs and output data is inverted with respect to input data. The SN65564A and SN75564A output sequences are reversed from the SN65563A and SN75563A for ease in printed circuit board layout.

Typically, composite V_{CC2}, V_{CC3}, and ground signals are externally generated by a high-voltage switching circuit. Serial data is entered into the shift register on the high-to-low transition of CLOCK. A high at the ENABLE input allows those outputs with a high in their associated register to be turned on, causing the corresponding row to be connected to V_{CC2} when POSITIVE WRITE is high or to ground when POSITIVE WRITE is low. V_{CC3} may be tied to V_{CC2} or held 5 V to 15 V above V_{CC2} for better V_{OH} characteristics. SERIAL OUTPUT from the shift register may be used to cascade additional devices. This output is not affected by the ENABLE or POSITIVE WRITE inputs.

The SN65563A and SN65564A are characterized for operation over the full automotive operating temperature range of −40°C to 85°C. The SN75563A and SN75564A are characterized for operation from 0°C to 70°C.

†BIDFET-Bipolar, double-diffused, N-channel and P-channel MOS transistors on the same chip — Patented Process

LOAD FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R34	OUTPUTS	
	CLOCK	ENABLE	POSITIVE WRITE		SERIAL	Q1 THRU Q34
LOAD	↓	X	X	Load and Shift†	R34	Determined by ENABLE and POSITIVE WRITE
	No↓	X	X	No Change	R34	Determined by ENABLE and POSITIVE WRITE

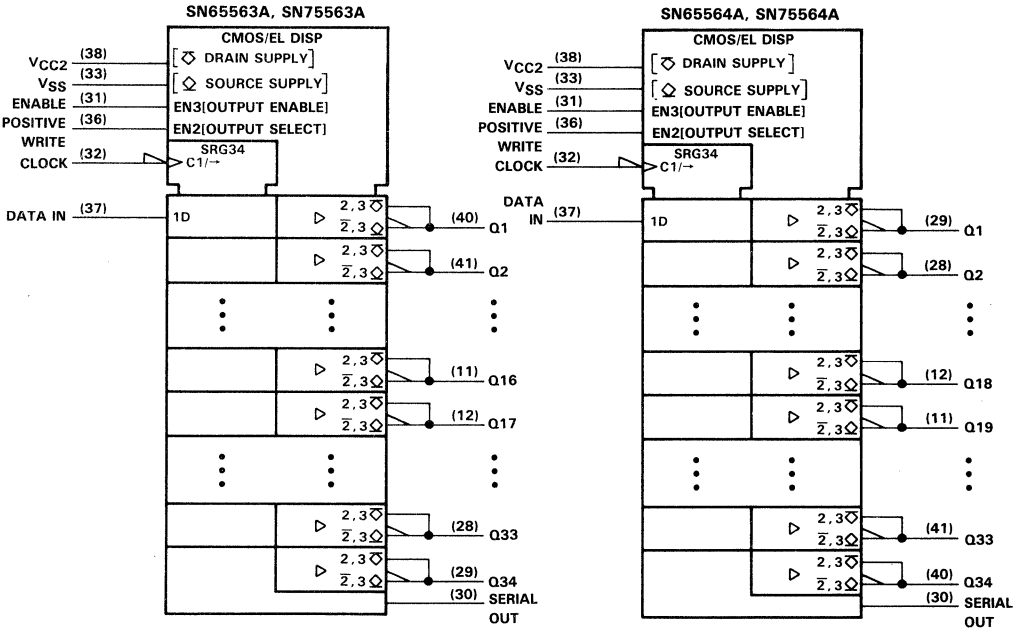
†Register R34 takes on the state of R33, R33 takes on the state of R32, . . . R2 takes on the state of R1, R1 takes on the state of the data input.

OUTPUT CONTROL FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTER CONTENTS Rn FOR R1 THRU R34 (Determined Above)	OUTPUTS	
	CLOCK	ENABLE	POSITIVE WRITE		SERIAL	Q1 THRU Q34
OUTPUT CONTROL	X	L	X	X	R34	High-Impedance
	X	H	H	H	R34	H
	X	H	L	H	R34	L
	X	X	X	L	R34	High-Impedance

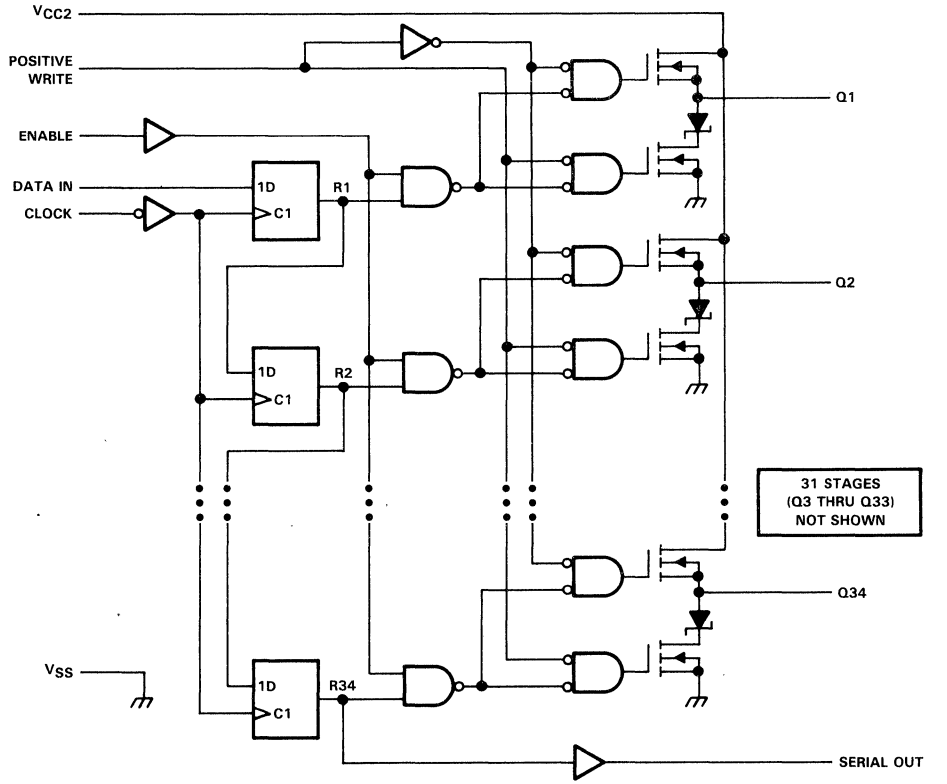
H = high, L = low, X = irrelevant, ↓ = high-to-low transition

schematics of inputs and outputs

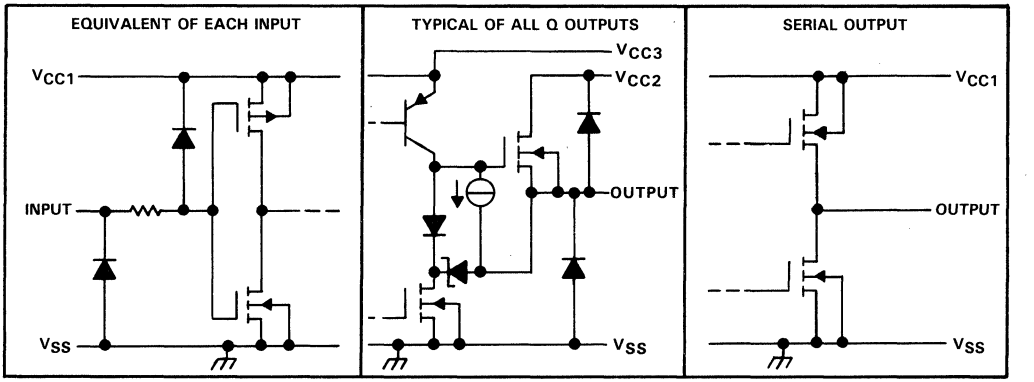


‡These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

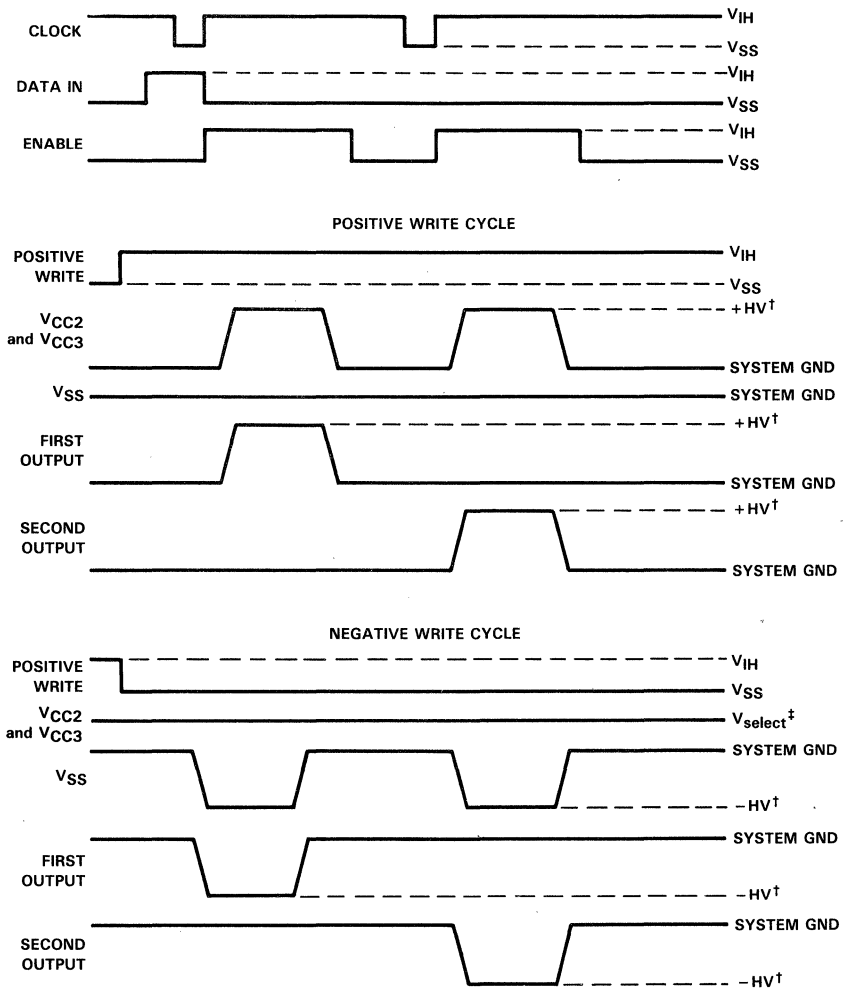
logic diagram (positive logic)



schematics of inputs and outputs



typical operating sequence



†HV = high voltage
‡During the negative write cycle, the V_{CC2} and V_{CC3} supplies are in a high-impedance state.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperture range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 240 V
Supply voltage, V_{CC3} . . . . . 240 V
Supply voltage, V_{SS} . . . . . −240 V
Input voltage . . . . . −0.3 V to V_{CC1} + 0.3 V
Continuous total power dissipation at (or below) 25 °C free-air temperature (see Note 2) . . . . . 1700 mW
Operating free-air temperature range: SN65563A, SN65564A . . . . . −40 °C to 85 °C
SN75563A, SN75564A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −40 °C to 125 °C
Case temperature for 10 seconds . . . . . 260 °C

NOTES: 1. Voltage values are with respect to V_{SS}.
2. For operation above 25 °C free-air temperature, derate to 1088 mW at 70 °C or 884 mW at 85 °C at the rate of 13.6 mW/ °C.

recommended operating conditions (see Note 1, Figure 1, and Figure 2)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		7.5	12	13.2	V
Supply voltage, V_{CC2}		$V_{CC3}-15$		V_{CC3}	V
Supply voltage, V_{CC3}		0		235	V
Supply voltage, V_{SS}		0		−235	V
High-level input voltage, V_{IH}		$0.75V_{CC1}$		$V_{CC1}+0.3$	V
Low-level input voltage, V_{IL}†		−0.3		$0.25V_{CC1}$	V
High-level output current, I_{OH}	SN65563A, SN65564A			−100	mA
	SN75563A, SN75564A			−120	
Low-level output current, I_{OL}				150	mA
Output clamp current, I_{OK}				±150	mA
Clock frequency, f_{clock}				4	MHz
Pulse duration, CLOCK high or low, t_{wCLK}		125			ns
Setup time, DATA IN high or low before CLOCK↓, t_{su1}		100			ns
Setup time, CLOCK low before V_{CC2}↑ or V_{SS}↓, t_{su2}		300			ns
Setup time, ENABLE high before V_{CC2}↑ or V_{SS}↓, t_{su3}		300			ns
Setup time, POSITIVE WRITE high or low before V_{CC2}↑ or V_{SS}↓, t_{su4}		300			ns
Hold time, DATA IN high or low after CLOCK↓, t_{h1}		100			ns
Hold time, CLOCK high after V_{CC2}↓ or V_{SS}↑, t_{h2}		300			ns
Hold time, ENABLE high after V_{CC2}↓ or V_{SS}↑, t_{h3}		0			ns
Hold time, POSITIVE WRITE after V_{CC2}↓ or V_{SS}↑, t_{h4}		0			ns
Hold time, ENABLE low between successive V_{CC2}↑, t_{h5}	SN65563A, SN65564A	12			μs
	SN75563A, SN75564A	10			
Hold time, ENABLE low between successive V_{SS}↓, t_{h6}		300			ns
Operating free-air temperature, T_A	SN65563A, SN65564A	−40		85	°C
	SN75563A, SN75564A	0		70	

†The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating ranges of V_{CC1} and free-air temperature range, V_{CC2} = 235 V, V_{CC3} = 235 V, V_{SS} = 0 (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$I_{O(off)}$	Off-state Q output current		V_O = 235 V		50	μA
			V_O = 0		−50	
V_{OH}	High-level output voltage	Q outputs	I_O = −70 mA	V_{CC2} − 30		V
		SERIAL OUT	I_O = −100 μA, V_{CC1} = 12 V	10.5		
V_{OL}	Low-level output voltage	Q outputs	I_O = 150 mA		30	V
		SERIAL OUT	I_O = 100 μA		1	
I_{IH}	High-level input current		V_{IH} = V_{CC1}		100	μA
I_{IL}	Low-level input current		V_{IL} = 0		−100	μA
I_{CC1}	Supply current from V_{CC1}		One Q output high		4	mA
			All Q outputs low or high impedance		2	
I_{CC3}	Supply current from V_{CC3}		One Q output high		10	mA
			All Q outputs low or high impedance		200	μA

switching characteristics operating range of V_{CC1}, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level serial output from clock	C_L = 50 pF to V_{SS}, See Figures 3 and 4		400	ns
t_{PHL}	Propagation delay time, high-to-low level serial output from clock			400	ns

PARAMETER MEASUREMENT INFORMATION

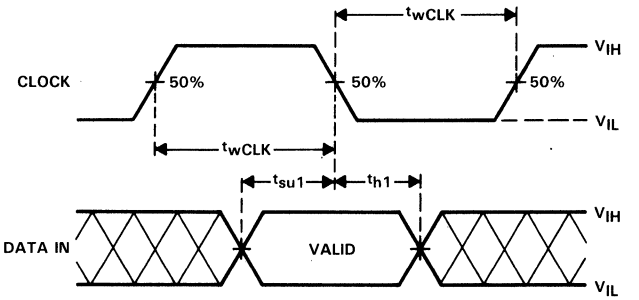
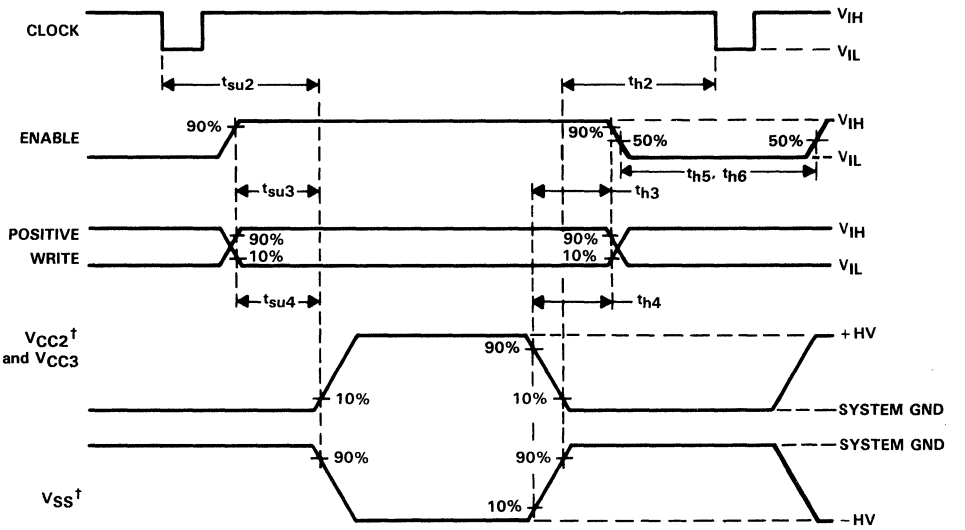


FIGURE 1. INPUT TIMING VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION



†Timing waveforms are with respect to V_{CC2} or V_{SS}, as appropriate.

FIGURE 2. CONTROL INPUT TIMING VOLTAGE WAVEFORMS

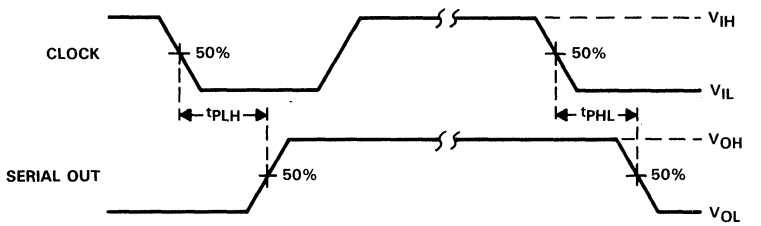


FIGURE 3. VOLTAGE WAVEFORMS FOR PROPAGATION DELAY TIMES, CLOCK TO DATA OUT

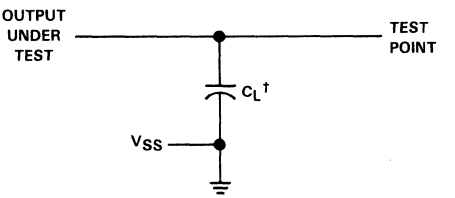


FIGURE 4. LOAD CIRCUIT

†C_L includes probe and jig capacitance.

D3005, DECEMBER 1986—REVISED JULY 1989

- **Each Device Drives 32 Lines**
- **180-V Open-Drain Parallel Outputs**
- **220-mA Parallel Output Sink Current Capability**
- **CMOS-Compatible Inputs**
- **Strobe Input Provided**
- **Serial Data Output for Cascade Operation**
- **Inputs Have Built-in Electrostatic Discharge Protection**

description

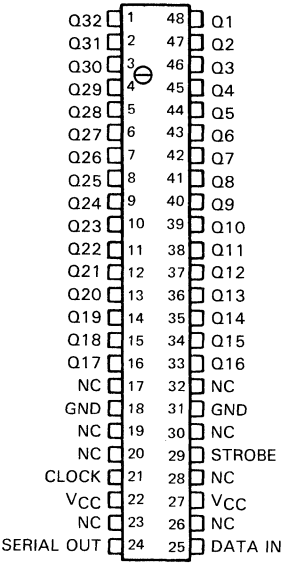
The SN751506 and the SN751516 are monolithic integrated circuits designed to drive the scan lines of a dc plasma panel display. The SN751516 pin sequence is reversed from the SN751506 for ease in printed circuit board layout.

Each device consists of a 32-bit shift register and 32 OR gates. Serial data is entered into the shift register on the high-to-low transition of the clock input. When STROBE is low, all Q outputs are in the off-state. Outputs are open-drain JFET transistors with a breakdown voltage in excess of 180 V. The outputs have a 220-mA sink current capability in the on state. Only one Q output should be allowed to be in the on state at a time.

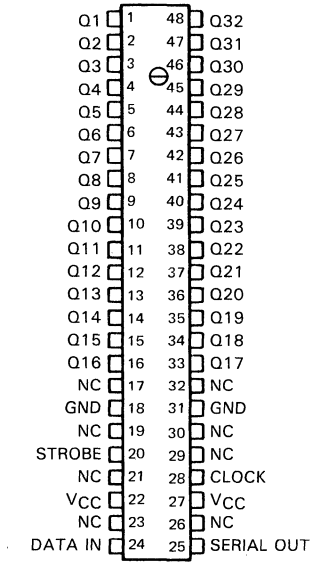
Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the strobe input. All inputs are CMOS compatible with ESD protection built in.

The SN751506 and SN751516 are characterized for operation from 0°C to 70°C.

SN751506 . . . FT PACKAGE
(TOP VIEW)

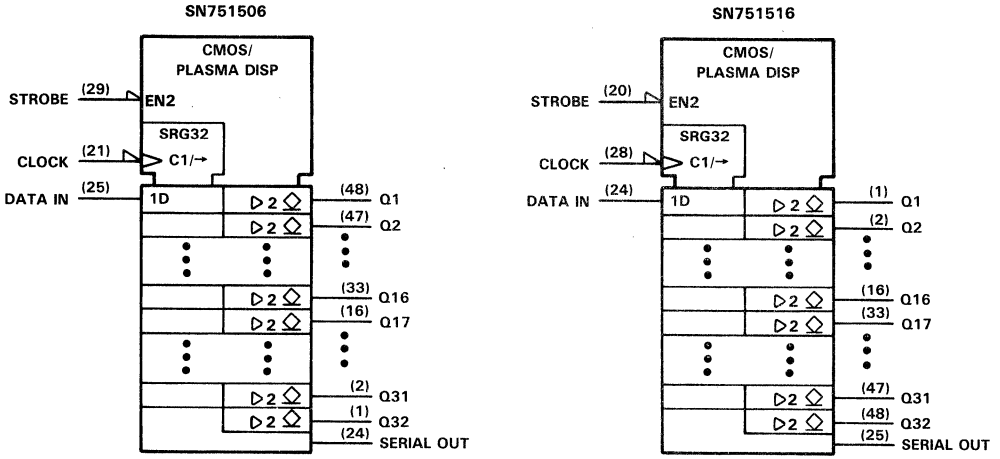


SN751516 . . . FT PACKAGE
(TOP VIEW)



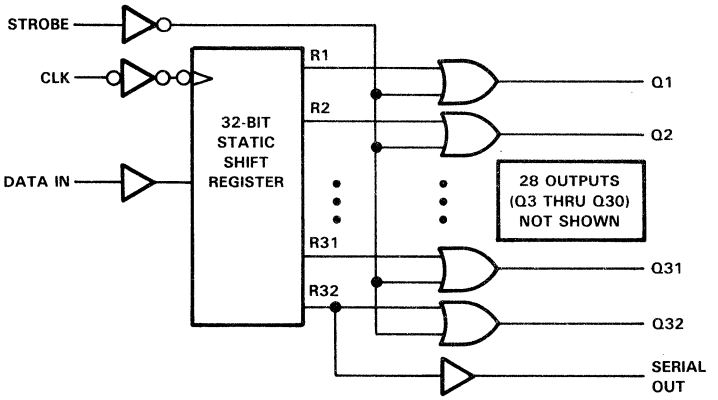
NC—No internal connection

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

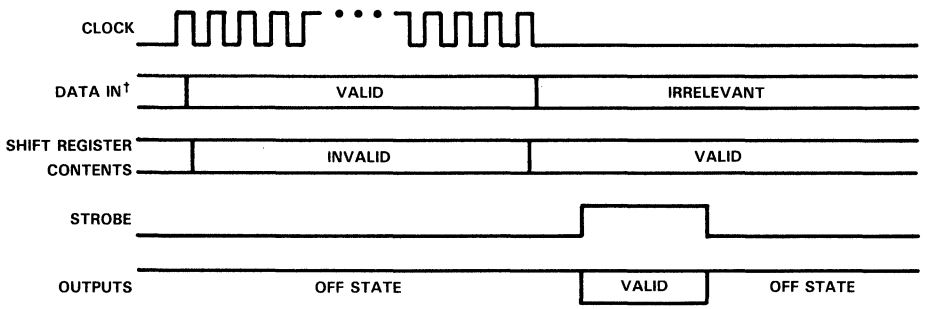


FUNCTION TABLE

FUNCTION	CONTROL INPUTS		SHIFT REGISTERS	OUTPUTS	
	CLOCK	STROBE	R1 THRU R32	SERIAL	Q1 THRU Q32
LOAD	↓	X	Load and shift‡	R32	Determined by STROBE
	No↓	X	No change	R32	
STROBE	X	L	As determined above	R32	All high impedance
	X	H		R32	R1 thru R32

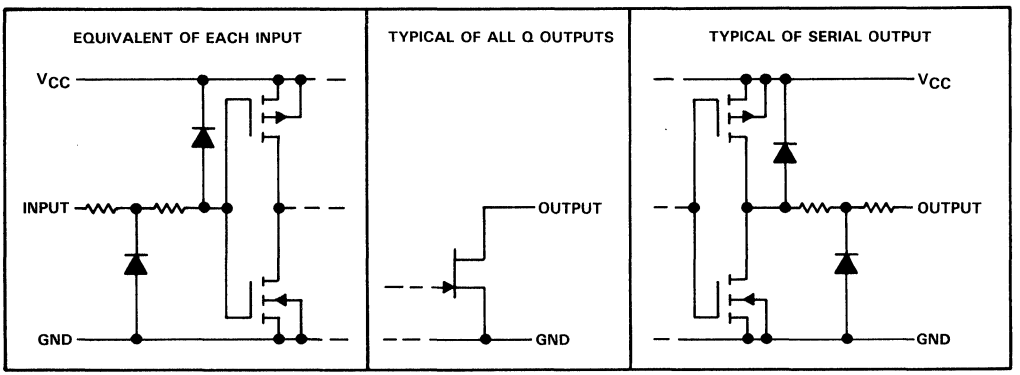
H = high level, L = low level, X = irrelevant, ↓ = high to low transition.
‡ R32 takes on the state of R31, R31 takes on the state of R30, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



†Only 1 bit in 32 should be low in the input data.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.4 V to 7 V
On-state Q output voltage, V_O . . . . . −0.4 V to 125 V
Off-state Q output voltage, V_O . . . . . −0.4 V to 180 V
Input voltage . . . . . −0.4 V to V_{CC}+0.4 V
Serial output voltage . . . . . −0.4 V to V_{CC}+0.4 V
Q output on-state time duration (see Note 2) . . . . . 100 μs
Q output duty cycle (see Note 2) 1/200
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 1025 mW
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to GND.
2. Only one Q output should be on at a time.
3. For operation above 25°C free-air temperature, derate linearly to 656 mW at 70°C at the rate of 8.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4	5	6	V
Peak on-state Q output voltage, $V_{O(on)}$				110	V
High-level input voltage, V_{IH}	V_{CC} = 4 V	3.2			V
	V_{CC} = 6 V	4.8			
Low-level input voltage, V_{IL}	V_{CC} = 4 V			0.8	V
	V_{CC} = 6 V			1.2	
Output current, I_O (T_A = 25°C)				220	mA
Clock frequency, f_{clock}				200	kHz
Pulse duration, CLOCK high or low, t_{wCLK}		1.5†			μs
Pulse duration, DATA, t_{wD}		5			μs
Pulse duration, STROBE, t_{wSTRB}		2			μs
Setup time, DATA IN before CLOCK↓, t_{su}		1			μs
Hold time, DATA IN after CLOCK↓, t_h		1.2			μs
Operating free-air temperature, T_A		0		70	°C

† The minimum clock period is 5 μs.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	SERIAL OUT	I_{OH} = −0.1 mA	4.5			V
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 180 mA		6	10	V
		SERIAL OUT	I_{OL} = 0.1 mA			0.5	
$I_{O(off)}$	Off-state output current	Q outputs	V_{OH} = 110 V			1	μA
I_{OL}	Low-level output current	Q outputs	V_{OL} = 16 V	220			mA
I_{IH}	High-level input current		V_I = V_{CC}			1	μA
I_{IL}	Low-level input current		V_I = 0			−1	μA
C_i	Input capacitance					15	pF
I_{CC}	Supply current		All Q outputs off			1	mA
			One Q output on		20	40	

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, CLOCK to SERIAL OUT	C_L = 15 pF		0.2	0.5	μs
t_{DHL}	Delay time, high-to-low-level Q output from STROBE or CLOCK inputs	C_L = 150 pF, R_L = 470 Ω, See Figures 2 and 3		0.2‡	0.6	μs
t_{DLH}	Delay time, low-to-high-level Q output from STROBE or CLOCK inputs			0.35‡	1	μs
t_{THL}	Transition time, high-to-low-level Q output			0.1	0.3	μs
t_{TLH}	Transition time, low-to-high-level Q output			0.35	1	μs

‡ Typical values are for clock inputs. Typical from strobe inputs will be less.

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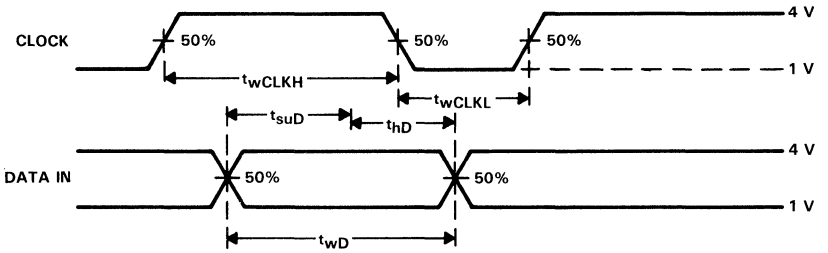


FIGURE 1. INPUT TIMING VOLTAGE WAVEFORMS

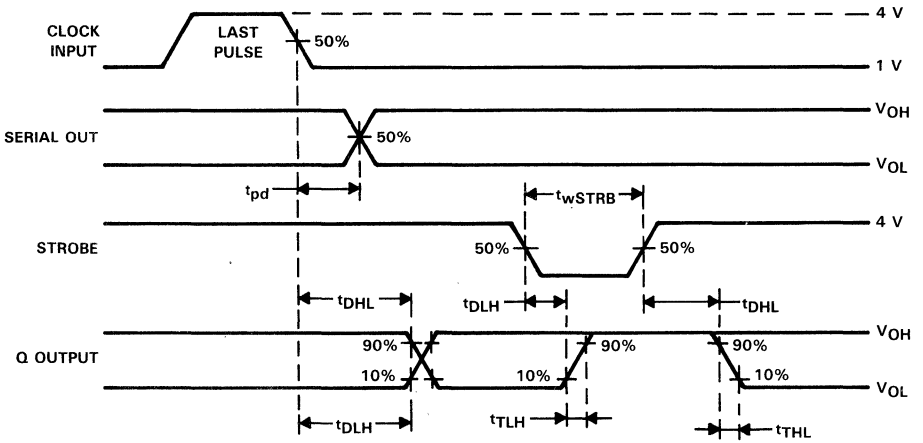
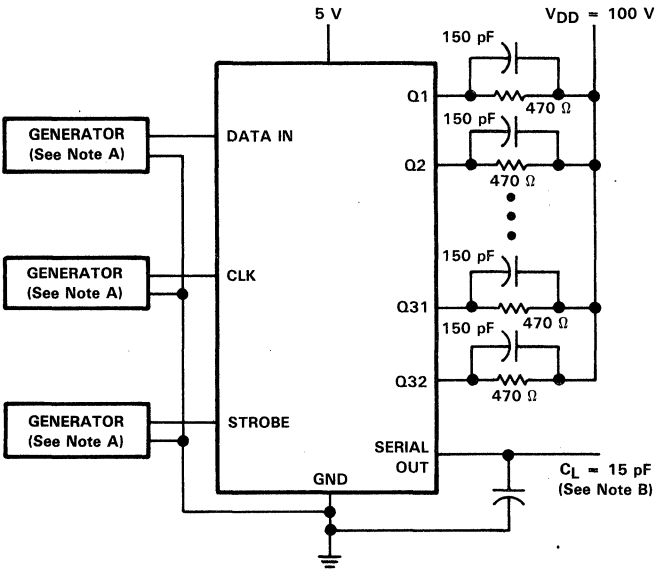


FIGURE 2. SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input pulses are supplied by generators having the following characteristics: t_w = 1.25 μs, PRR ≤ 200 kHz, t_r ≤ 30 ns, t_f ≤ 30 ns, Z_o = 50 Ω.

B. C_L includes probe and jig capacitance.

FIGURE 3. TEST CIRCUIT

TYPICAL CHARACTERISTICS

LOW-LEVEL Q OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

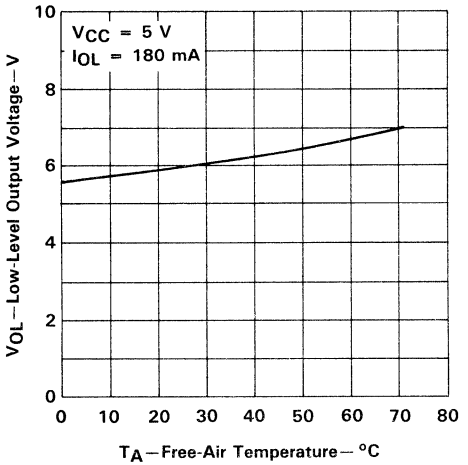


FIGURE 4

LOW-LEVEL Q OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

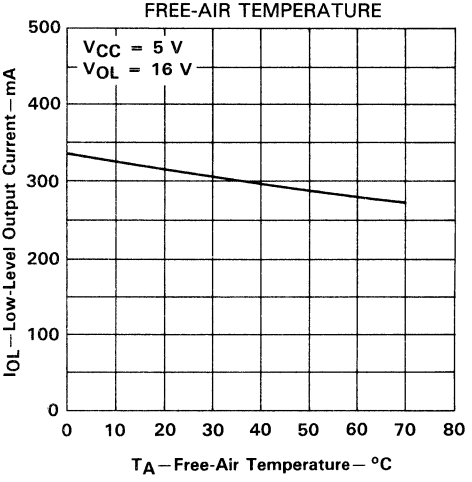


FIGURE 5

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

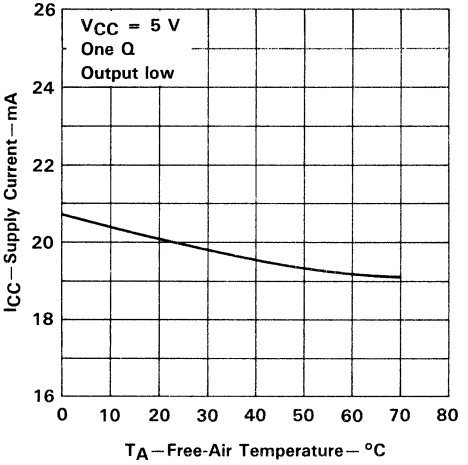


FIGURE 6

PROPAGATION DELAY TIME,
CLOCK TO SERIAL OUTPUT
vs
FREE-AIR TEMPERATURE

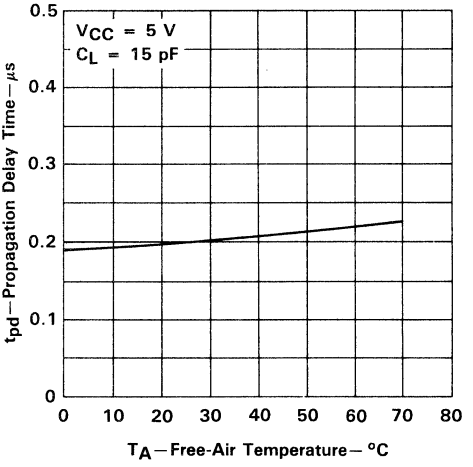


FIGURE 7

TYPICAL CHARACTERISTICS

DELAY TIME,
HIGH-TO-LOW-LEVEL Q OUTPUT
vs
FREE-AIR TEMPERATURE

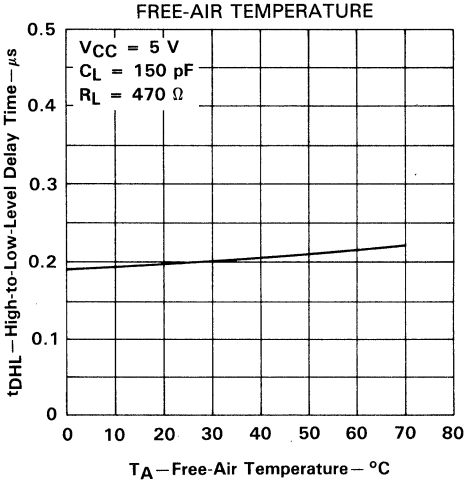


FIGURE 8

DELAY TIME,
LOW-TO-HIGH-LEVEL Q OUTPUT
vs
FREE-AIR TEMPERATURE

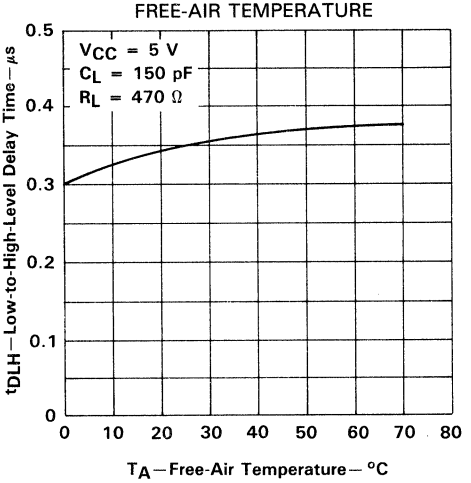


FIGURE 9

TRANSITION TIME,
HIGH-TO-LOW-LEVEL Q OUTPUT
vs
FREE-AIR TEMPERATURE

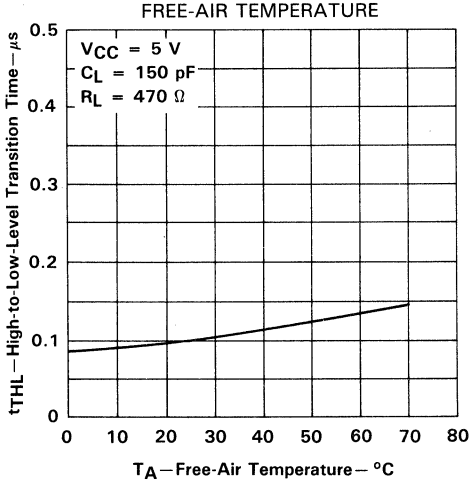


FIGURE 10

TRANSITION TIME,
LOW-TO-HIGH-LEVEL Q OUTPUT
vs
FREE-AIR TEMPERATURE

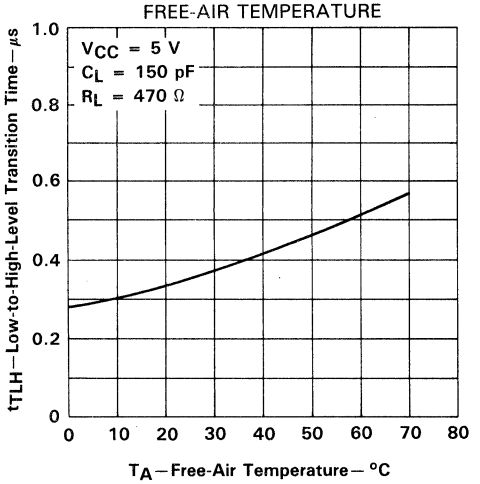


FIGURE 11

D2984, JANUARY 1987—REVISED NOVEMBER 1989

- **Each Device Drives 32 Lines**
- **−120-V P-N-P Open-Collector Parallel Outputs**
- **High-Speed Serially Shifted Data Inputs**
- **CMOS-Compatible Inputs**
- **Strobe and Sustain Inputs Provided**
- **Serial Data Output for Cascade Operation**

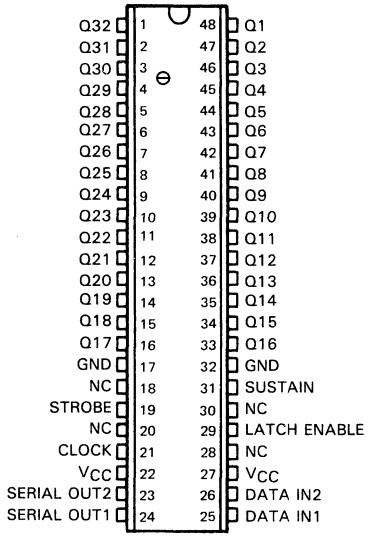
description

The SN751508 and SN751518 are monolithic integrated circuits designed to drive the data lines of a dc plasma panel display. The SN751518 pin sequence is reversed from the SN751508 for ease in printed circuit board layout.

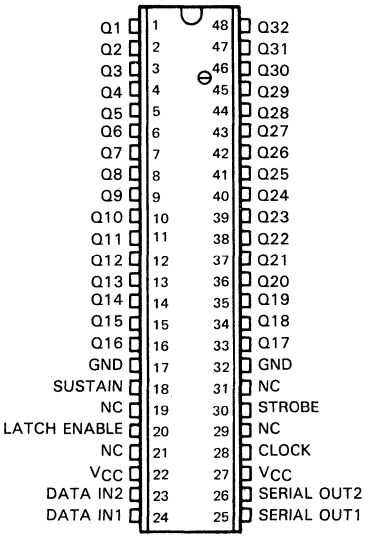
Each device consists of two 16-bit shift registers, 32 latches, 32 OR gates, and 32 P-N-P open-collector output AND gates. Typically, a 32-bit data string is split into two 16-bit data strings externally and then entered in parallel into the shift registers on the high-to-low transition of the clock signal. A high LATCH ENABLE transfers the data from the shift registers to the inputs of 32 OR gates through the latches. Data present in the latch during the high-to-low transition of LATCH ENABLE is stored. When STROBE is high, the latch is masked and a high will be placed on the data input of the output AND gates. When STROBE is low, and SUSTAIN is high, data from the latches is reflected at the outputs. When low, SUSTAIN will force all outputs to their off state. Drivers may be cascaded via the serial data outputs of the static shift registers. These outputs are not affected by LATCH ENABLE, STROBE, or SUSTAIN.

The SN751508 and the SN751518 are characterized from 0°C to 70°C.

SN751508 . . . FT PACKAGE
(TOP VIEW)



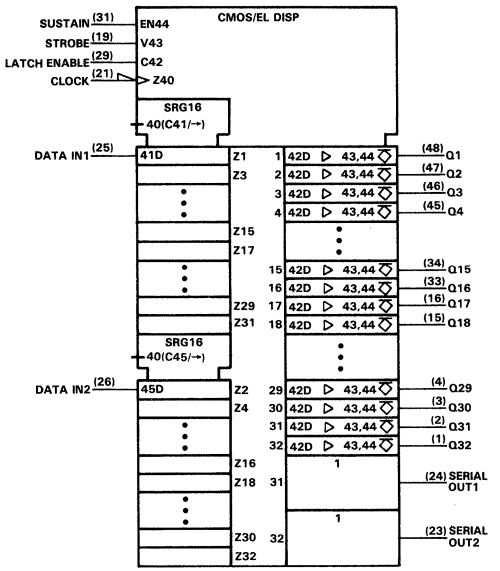
SN751518 . . . FT PACKAGE
(TOP VIEW)



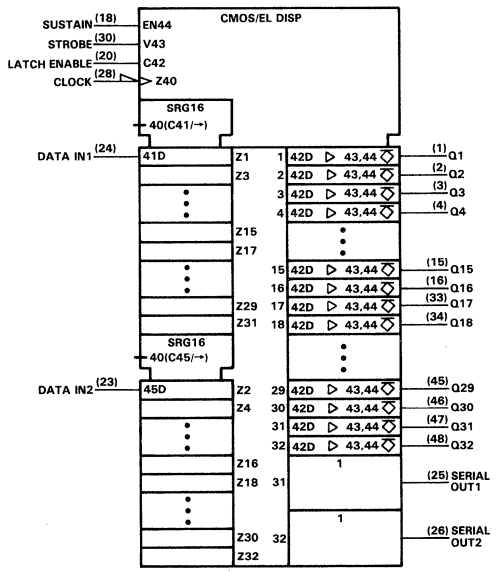
NC—No internal connection

logic symbols†

SN751508

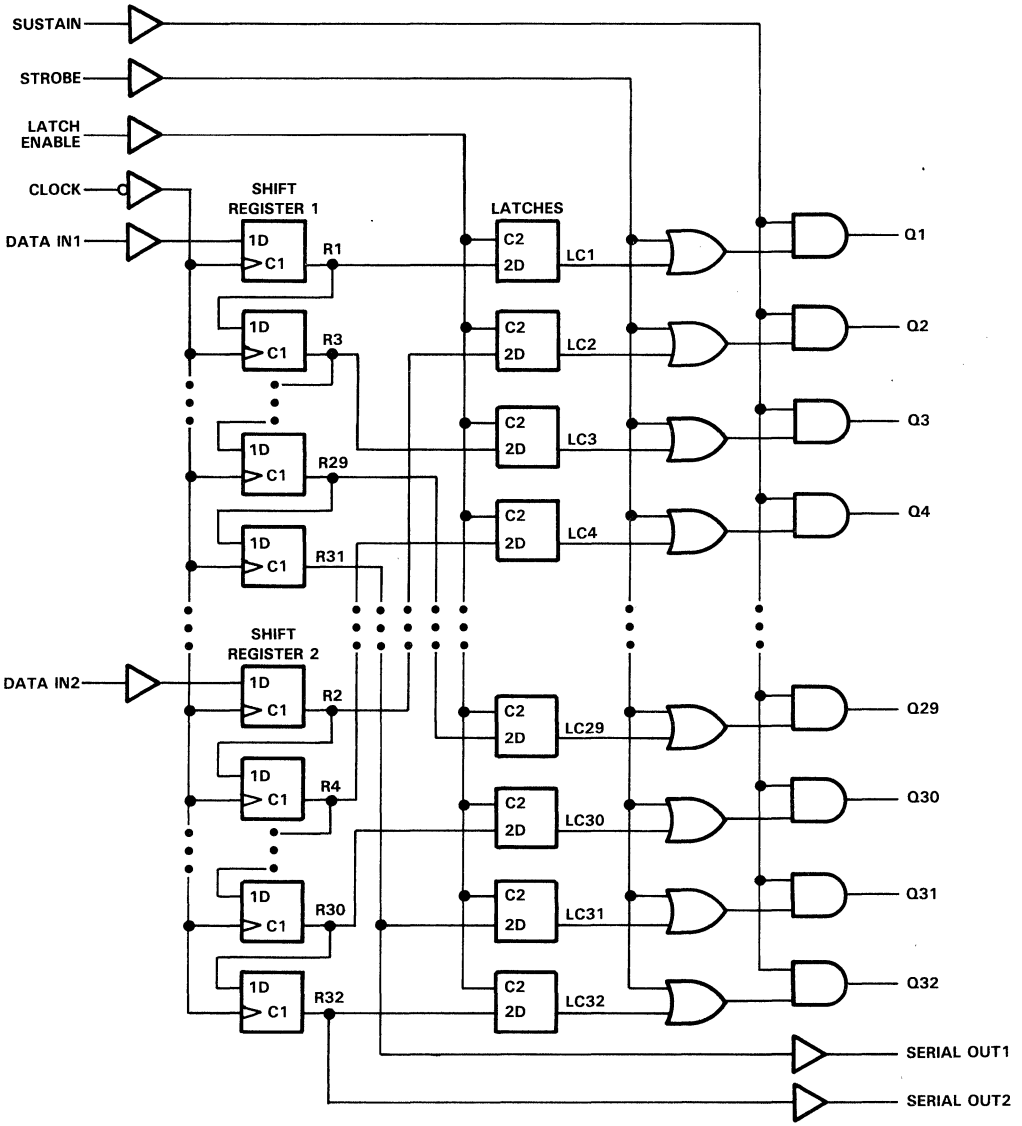


SN751518



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



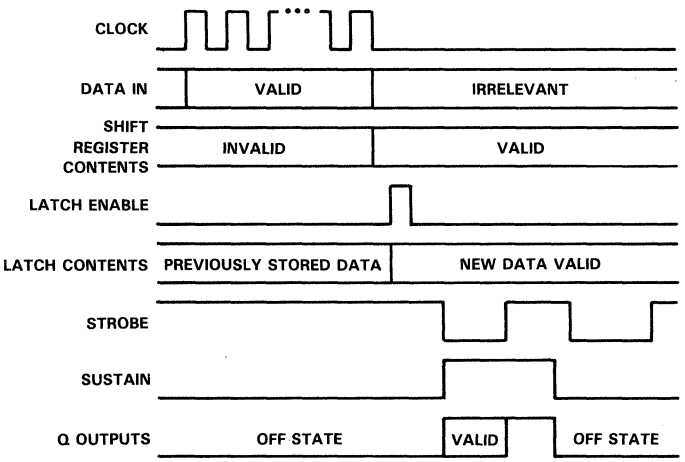
FUNCTION	CONTROL INPUTS				SHIFT REGISTERS R1 THRU R32	LATCHES LC1 THRU LC32	OUTPUTS		
	CLOCK	LATCH ENABLE	STROBE	SUSTAIN			SERIAL SO1	SERIAL SO2	Q1 THRU Q32
LOAD	↓	X	X	X	Load and shift†	Determined by	R31	R32	Determined by
	No ↓	X	X	X	No change	LATCH ENABLE‡			SUSTAIN and STROBE
LATCH ENABLE	X	L	X	X	As determined	Stored data	R31	R32	Determined by
	X	H	X	X	above	New data			SUSTAIN and STROBE
STROBE	X	X	L	H	As determined	Determined by	R31	R32	LC1 thru LC32
	X	X	H	H	above	LATCH ENABLE‡			All on (high)
SUSTAIN	X	X	X	L	As determined above	Determined by LATCH ENABLE‡	R31	R32	All off

H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition

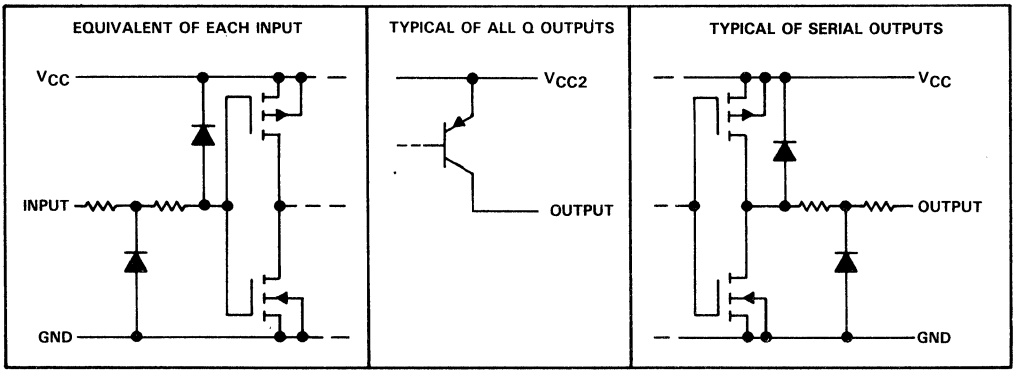
† Each even-numbered shift register stage takes on the state of the next-lower even-numbered stage, and likewise each odd-numbered shift register stage takes on the state of the next-lower odd-numbered stage; i.e., R32 takes on the state of R30, R30 takes on the state of R28, . . . R4 takes on the state of R2, R2 takes on the state of Data In2, R31 takes on the state of R29, R29 takes on the state of R27, . . . R3 takes on the state of R1, and R1 takes on the state on Data In1.

‡ New data enters the latches while LATCH ENABLE is high. This data is stored while LATCH ENABLE is low.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.4 to 7 V
On-state Q output voltage, V_O . . . . . −120 V to V_{CC} +0.4 V
Input voltage . . . . . −0.4 V to V_{CC} +0.4 V
Serial output voltage . . . . . −0.4 V to V_{CC} +0.4 V
Continuous total power dissipation at (or below) 25 °C free-air temperature (see Note 2) . . . . . 1025 mW
Operating free-air temperature range, T_A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260 °C

NOTES: 1. Voltages values are with respect to GND.
2. For operation above 25 °C free-air temperature, derate linearly to 656 mW at 70 °C at the rate of 8.2 mW/°C.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			4.5	5	5.5	V
Output voltage, V_O					−75	V
High-level input voltage, V_{IH}		V_{CC} = 4.5 V	3.6			V
		V_{CC} = 5.5 V	4.4			
Low-level input voltage, V_{IL}		V_{CC} = 4.5 V			0.9	V
		V_{CC} = 5.5 V			1	
Output current, I_O (T_A = 25°C)					−1.2	mA
Clock frequency, f_{clock}					5	MHz
Pulse duration, t_w (see Figure 1)	CLOCK		75			ns
	DATA IN		160			
	LATCH ENABLE		90			
	STROBE		2			μs
	SUSTAIN		2			
Setup time, t_{su} (see Figure 1)	DATA IN before CLOCK↓		20			ns
	CLOCK low before LATCH ENABLE↑		50			
	LATCH ENABLE low before CLOCK↓		0			
	LATCH ENABLE high before STROBE↓		0			
	LATCH ENABLE high before SUSTAIN↑		0			
Hold time, DATA IN after CLOCK↓, t_h (see Figure 1)			50			μs
Operating free-air temperature, T_A			0		70	°C

electrical characteristics, V_{CC} = 5 V, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH} High-level output voltage	Q outputs		I_{OH} = −0.5 mA		4	4.5		V
	Serial Outputs	V_{CC} = 5.5 V	I_{OH} = −100 μA		4.3	4.6		
			I_{OH} = −20 μA		4.4			
		V_{CC} = 4.5 V	I_{OH} = −100 μA		3.4	3.6		
			I_{OH} = −20 μA		3.6			
V_{OL} Low-level output voltage	Serial Outputs	V_{CC} = 5.5 V	I_{OL} = 100 μA			0.9	1.2	V
			I_{OL} = 20 μA				1.1	
		V_{CC} = 4.5 V	I_{OL} = 100 μA			0.9	1.1	
			I_{OL} = 20 μA				0.9	
I_{OH} High-level Q output current			T_A = 25°C,	V_O = 3 V	−1.2			mA
I_{OL} Low-level Q output current			T_A = 25°C,	V_O = −75 V			−500	μA
I_{IH} High-level input current			T_A = 25°C,	V_I = V_{CC}			1	μA
I_{IL} Low-level input current			T_A = 25°C,	V_I = 0			−1	μA
I_{CC} Supply current			All Q outputs high,	V_{CC} = 5.5 V		17	25	mA
			All Q outputs low				3	
C_i Input capacitance							15	pF

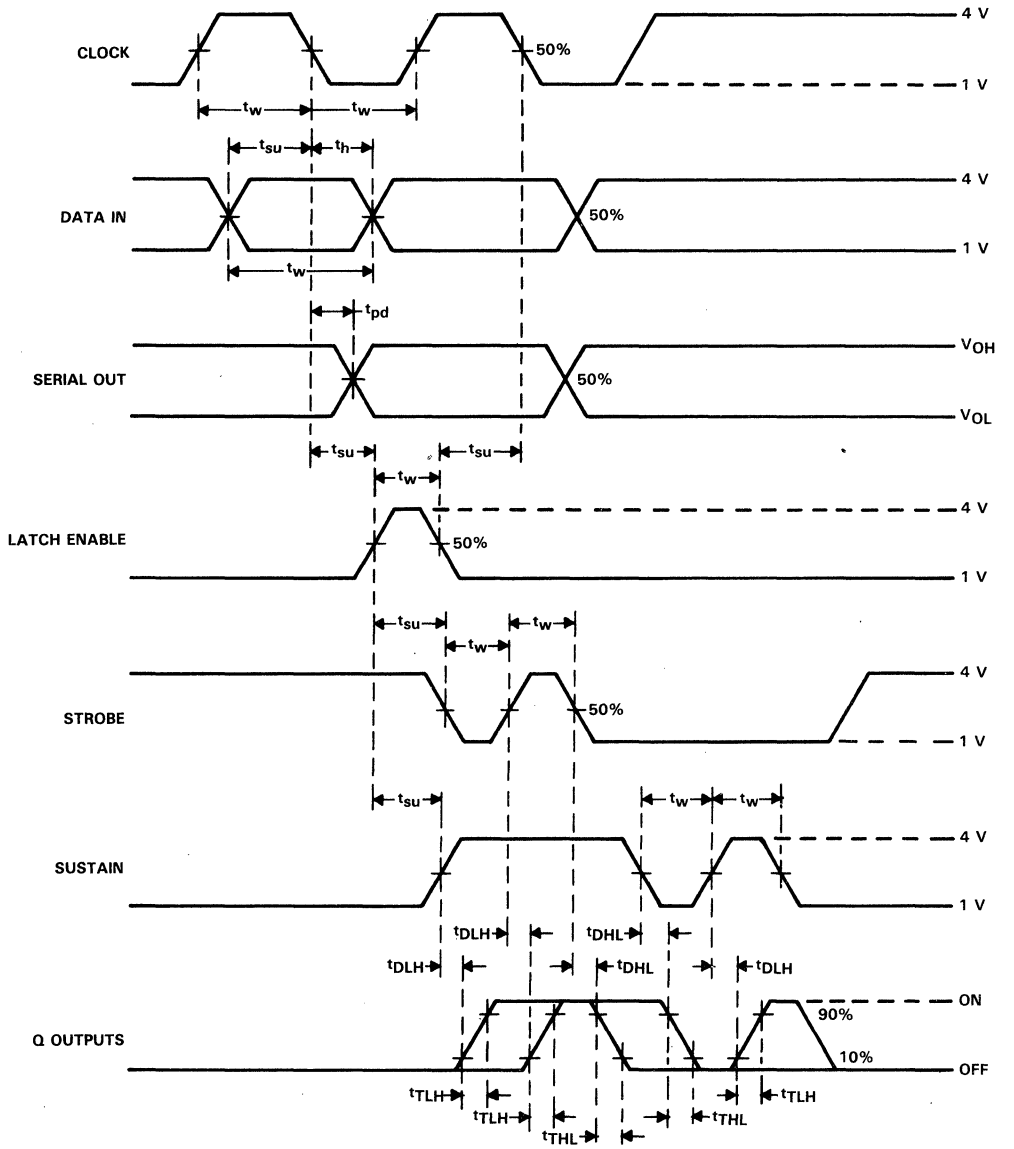
†All typical values are at T_A = 25°C.

switching characteristics V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, CLOCK to Serial Outputs	C_L = 15 pF		100	150	ns
t_{DLH}	Delay time, low-to-high-level Q output from SUSTAIN or STROBE	C_L = 15 pF, R_L = 91 kΩ, See Figures 1 and 2		0.3‡	1	μs
t_{DHL}	Delay time, high-to-low-level Q output from SUSTAIN or STROBE			1‡	2.5	μs
t_{TLH}	Transition time, low-to-high-level Q output			2	5	μs
t_{THL}	Transition time, high-to-low-level Q output			11	18	μs

‡Typical values for delay times are measured from the SUSTAIN input.

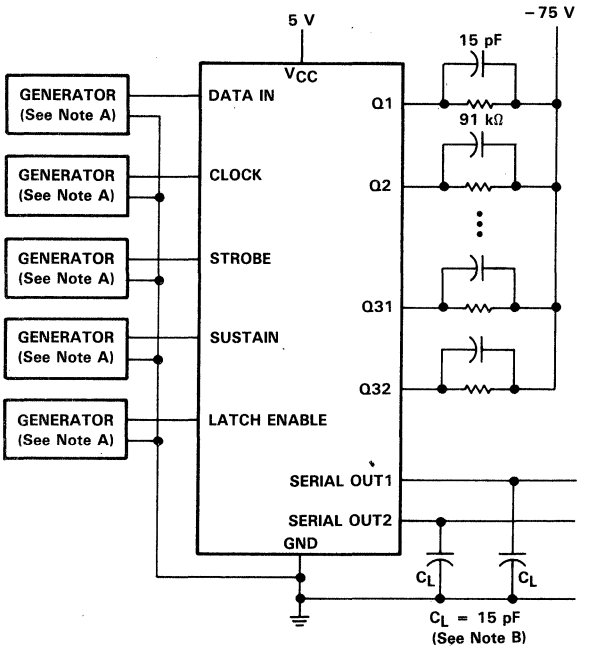
PARAMETER MEASUREMENT INFORMATION



NOTE: Input t_r and t_f are less than or equal to 10 ns.

FIGURE 1. INPUT TIMING AND SWITCHING TIME VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

NOTES: A. Input pulses are supplied by generators having the following characteristics: t_w = 100 ns, PRR ≤ 5 MHz, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_o = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 2

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

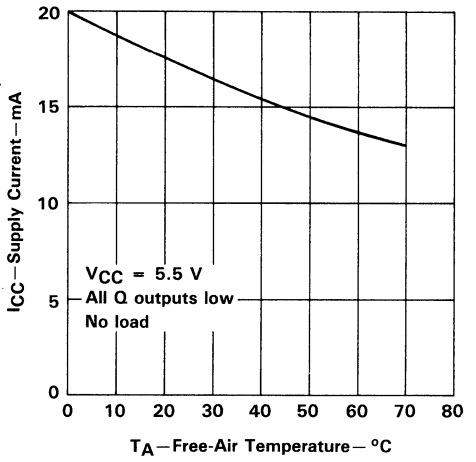


FIGURE 3

DELAY TIME, CLOCK TO SERIAL OUTPUT
vs
FREE-AIR TEMPERATURE

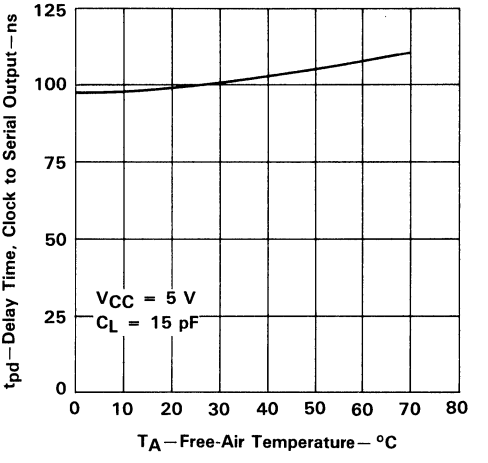


FIGURE 4

DELAY TIME, SUSTAIN INPUT TO Q OUTPUT,
LOW TO HIGH
vs
FREE-AIR TEMPERATURE

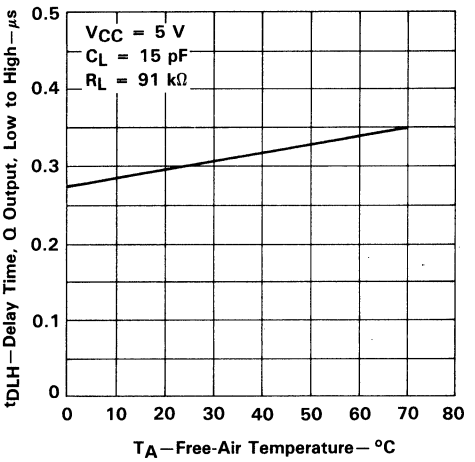


FIGURE 5

DELAY TIME, SUSTAIN INPUT TO Q OUTPUT,
HIGH TO LOW
vs
FREE-AIR TEMPERATURE

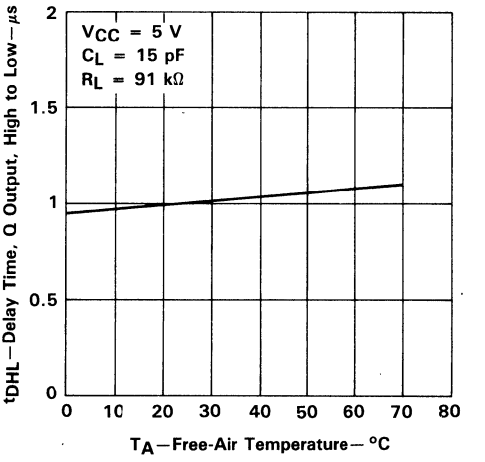


FIGURE 6

TYPICAL CHARACTERISTICS

TRANSITION TIME, Q OUTPUT, LOW TO HIGH vs FREE-AIR TEMPERATURE

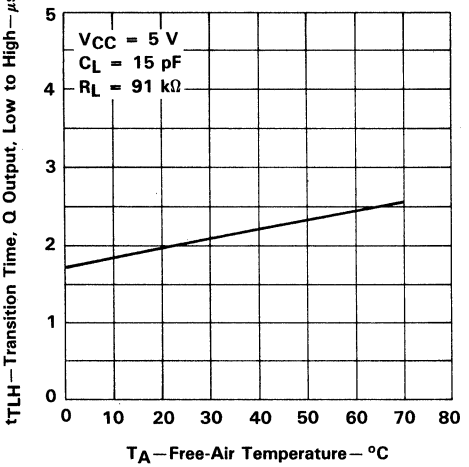


FIGURE 7

TRANSITION TIME, Q OUTPUT, HIGH TO LOW vs FREE-AIR TEMPERATURE

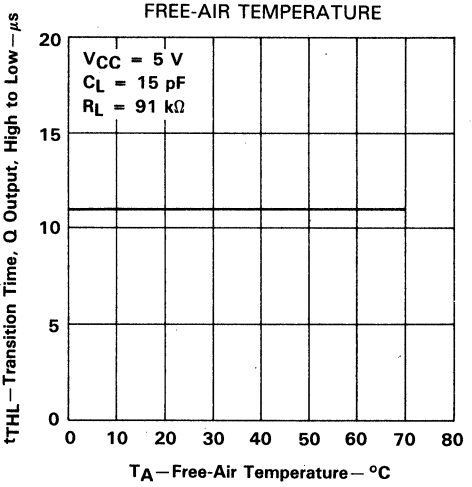


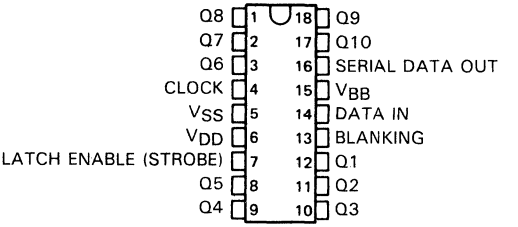
FIGURE 8

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

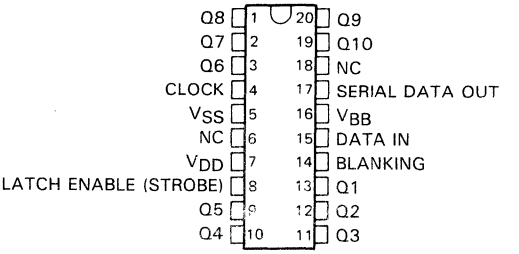
D2715, DECEMBER 1984—REVISED OCTOBER 1989

- **Each Device Drives 10 Lines**
- **60-V Output Voltage Rating**
- **40-mA Output Source Current**
- **High-Speed Serially-Shifted Data Input**
- **CMOS-Compatible Inputs**
- **Latches on All Driver Outputs**
- **Improved Direct Replacement for UCN4810A and TL4810A**

N PACKAGE
(TOP VIEW)



DW
SMALL OUTLINE PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TL4810BI and TL4810B are monolithic BIDFET† integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). These devices feature a serial data output to cascade additional devices for large display arrays.

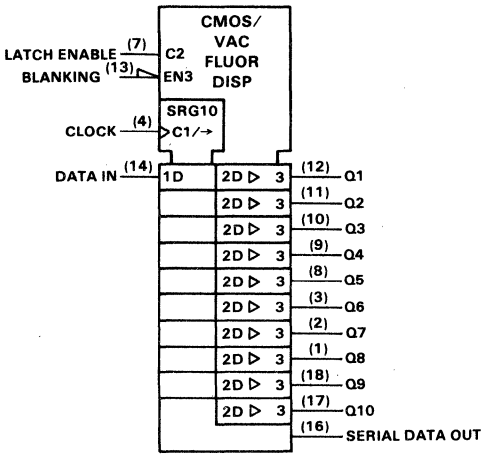
A 10-bit data word is serially loaded into the shift register on the positive-going transitions of the clock. Parallel data is transferred to the output buffers through a 10-bit D-type latch while LATCH ENABLE is high and is latched when LATCH ENABLE is low. When BLANKING is high, all outputs are low.

Outputs are totem-pole structures formed by n-p-n emitter-follower and double-diffused MOS (DMOS) transistors with output voltage ratings of 70 V and 40 mA source-current capability. All inputs are compatible with CMOS and TTL levels, but each requires the addition of a pull-up resistor to V_{DD} when driven by TTL logic.

The TL4810BI is characterized for operation from −40°C to 85°C. The TL4810B is characterized for operation from 0°C to 70°C.

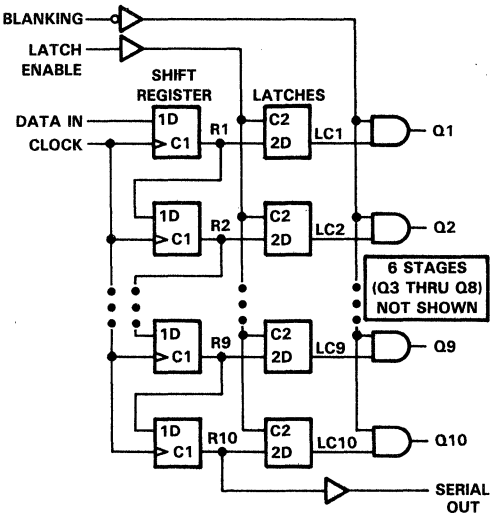
† BIDFET—Bipolar, Double-Diffused, N-Channel and P-Channel MOS transistors on same chip—patented process.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

logic diagram (positive logic)

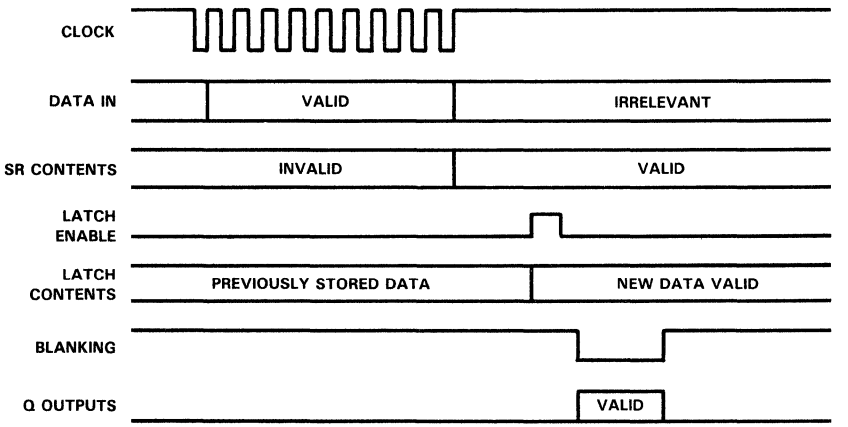


FUNCTION TABLE

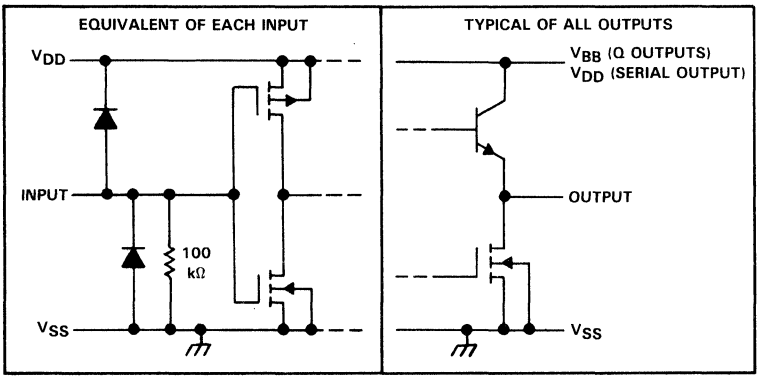
FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R10‡	LATCHES LC1 THRU LC10	OUTPUTS	
	CLOCK	LATCH ENABLE	BLANKING			SERIAL	Q1 THRU Q10
LOAD	↑	X	X	Load and shift‡	Determined by	R10	Determined by BLANKING
	No↑	X	X	No change	LATCH ENABLE§		
LATCH	X	L	X	As determined above	Stored data	R10	Determined by BLANKING
	X	H	X		New data		
BLANK	X	X	H	As determined above	Determined by	R10	All L
	X	X	L		LATCH ENABLE§		LC1 thru LC10 respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
‡ Register R10 takes on the state of R9, R9 takes on the state of R8 . . . R2 takes on the state of R1, and R1 takes on the state of the data input.
§ New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Driver supply voltage, V_{BB} . . . . . 70 V
Output voltage . . . . . 70 V
Input voltage . . . . . −0.3 V to V_{DD} + 0.3 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TL4810BI . . . . . −40°C to 85°C
TL4810B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to V_{SS}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

PARAMETER		TL4810BI			TL4810B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4.75		15.75	4.75		15.75	V
Supply voltage, V_{BB}		5		60	5		60	V
Supply voltage, V_{SS}			0			0		V
High-level input voltage, V_{IH}	for V_{DD} = 5 V	3.5		5.3	3.5		5.3	V
	for V_{DD} = 15 V	13.5		15.3	13.5		15.3	
Low-level input voltage, V_{IL}		−0.3†		0.8	−0.3†		0.8	V
Continuous high-level output current, I_{OH}				−25			−25	mA
Operating free-air temperature, T_A		−40		85	0		70	°C

† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltages only.

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V to 15 V, V_{BB} = 60 V, V_{SS} = 0 (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TL4810BI			TL4810B			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH}	High-level output voltage	Q outputs	I_{OH} = −25 mA		57.5	58		57.5	58		V
		Serial output	V_{DD} = 5 V,	I_{OH} = −100 μA	4	4.5		4	4.5		
			V_{DD} = 15 V,	I_{OH} = −100 μA	14	14.7		14	14.7		
V_{OL}	Low-level output voltage	Q outputs	I_{OH} = 1 μA,	BLANKING at V_{DD}		0.5	1		0.5	1	V
		Serial output	V_{DD} = 5 V,	I_{OL} = 100 μA		0.05	0.1		0.05	0.1	
			V_{DD} = 15 V,	I_{OL} = 100 μA		0.02	0.1		0.02	0.1	
I_{OL}	Low-level Q output current (pull-down current)		V_O = 60 V, T_A = MIN to 70°C	BLANKING at V_{DD},	2.5	3.7		2.5	3.7		mA
			V_O = 60 V, T_A = 85°C	BLANKING at V_{DD},	2						
$I_{O(off)}$	Off-state output current		V_O = 0, T_A = MAX	BLANKING at V_{DD},		−1	−15		−1	−15	μA
I_H	High-level input current		V_I = V_{DD}			30	50		30	50	μA
I_{BB}	Supply current from V_{BB}		All outputs low			0.5	1		0.5	1	mA
			All outputs high, T_A = 0°C to MAX			2.7	4		2.7	4	
			All outputs high, T_A = −40°C				5				
I_{DD}	Supply current from V_{DD}		All inputs at 0 V,	V_{DD} = 5 V		10	50		10	50	μA
			One Q output high	V_{DD} = 15 V		10	100		10	100	
			All inputs at 0 V,	V_{DD} = 5 V		10	50		10	50	
			All outputs low	V_{DD} = 15 V		10	100		10	100	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C, except for I_O.

timing requirements over recommended operating free-air temperature range

PARAMETER		V_{DD} = 5 V		V_{DD} = 15 V		UNIT
		MIN	MAX	MIN	MAX	
$t_{w(CKH)}$	Pulse duration, CLOCK high	250		50		ns
$t_{w(LEH)}$	Pulse duration, LATCH ENABLE high	250		50		ns
$t_{su(D)}$	Setup time, DATA IN before CLOCK↑	125		25		ns
$t_{h(D)}$	Hold time, DATA IN after CLOCK↑	125		25		ns
$t_{CKH-LEH}$	Delay time, CLOCK↑ to LATCH ENABLE high	125		25		ns

switching characteristics, V_{BB} = 60 V, T_A = 25°C

PARAMETER			MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, LATCH ENABLE to output	V_{DD} = 5 V		1		μs
		V_{DD} = 15 V		0.5		

PARAMETER MEASUREMENT INFORMATION

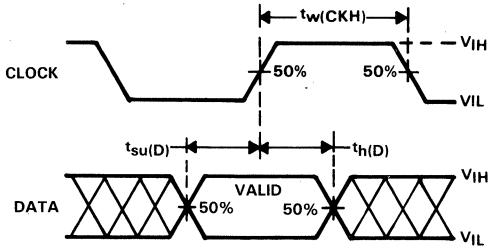


FIGURE 1. INPUT TIMING

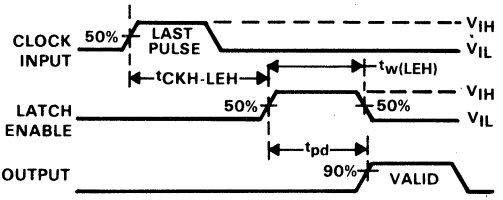


FIGURE 2. OUTPUT SWITCHING TIMES

THERMAL INFORMATION

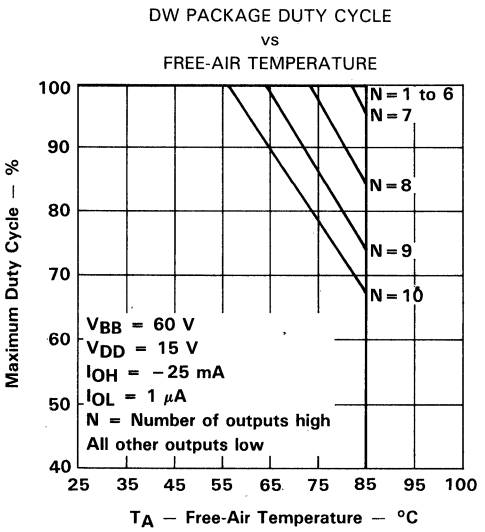


FIGURE 3

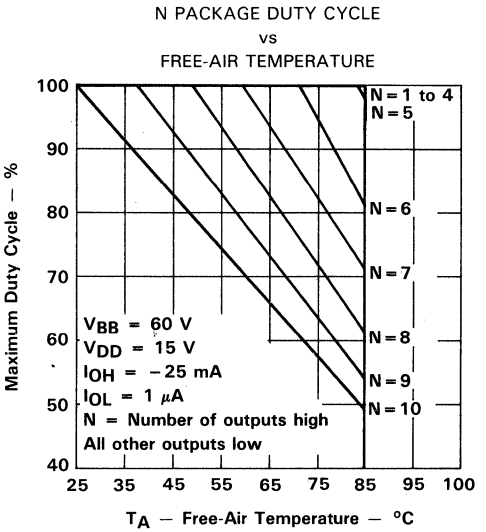
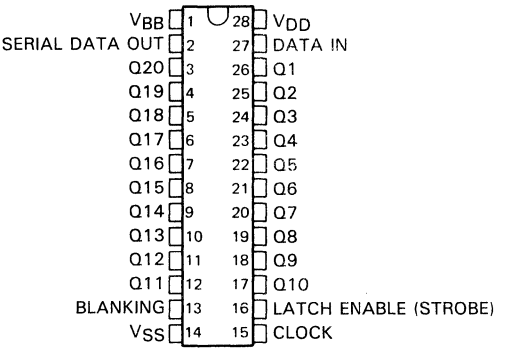


FIGURE 4

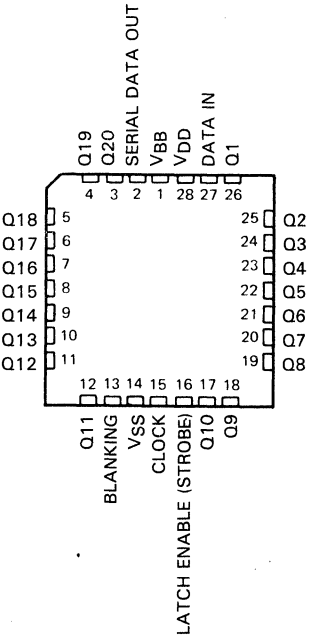
D2914, OCTOBER 1985—REVISED OCTOBER 1989

- **Drives Up to 20 Lines**
- **70-V Output Voltage Swing Capability**
- **40-mA Output Source Current Capability**
- **High-Speed Serially-Shifted Data Input**
- **CMOS-Compatible Inputs**
- **Direct Replacement for Sprague UCN5812A**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TLC5812I and TLC5812 are monolithic BIDFET† integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). Each device features a serial data output to cascade additional devices for large display arrays.

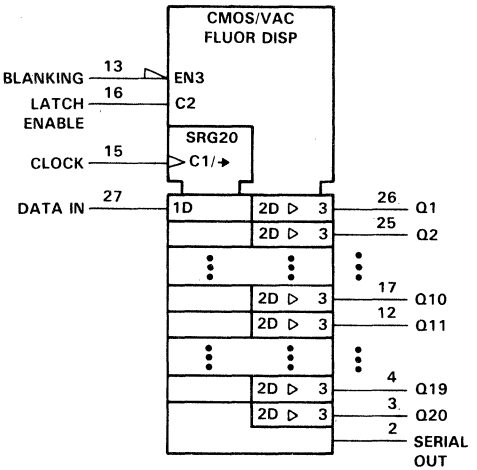
A 20-bit data word is serially loaded into the shift register on the low-to-high transition of CLOCK. Parallel data is transferred to the output buffers through a 20-bit D-type latch while LATCH ENABLE is high and is latched when LATCH ENABLE is low. When BLANKING is high, all outputs are low.

The outputs are totem-pole structures formed by n-p-n emitter-follower and double-diffused MOS (DMOS) transistors with output voltage ratings of 70 V and a source-current capability of 40 mA. All inputs are CMOS compatible.

The TLC5812I is characterized for operation from −40°C to 85°C. The TLC5812 is characterized for operation from 0°C to 70°C.

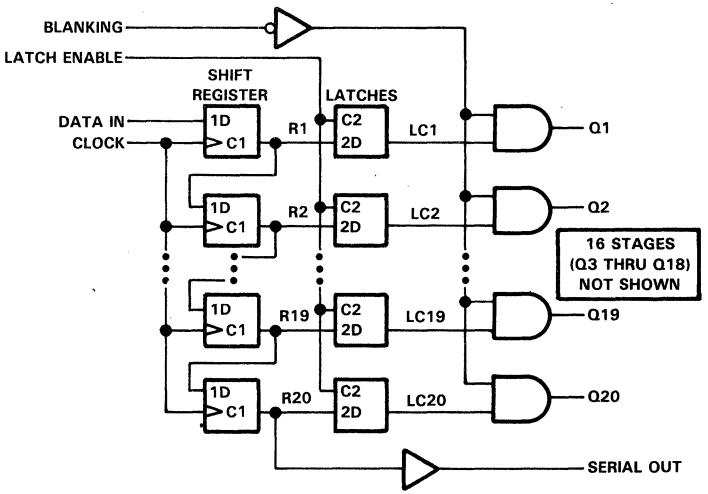
† BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on the same chip — patented process.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

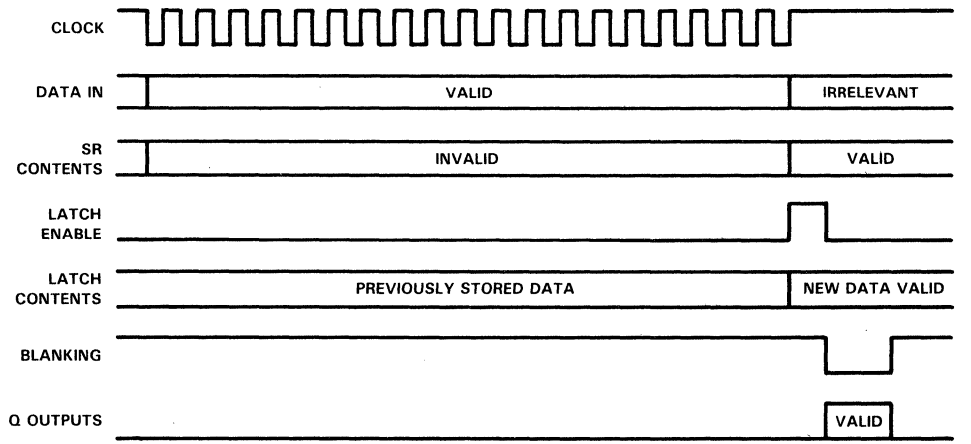


FUNCTION TABLE

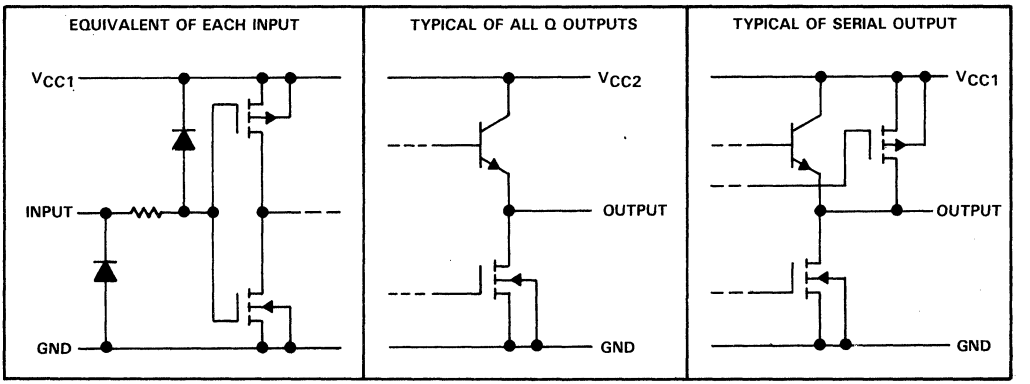
FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R20	LATCHES LC1 THRU LC20	OUTPUTS	
	CLOCK	LATCH ENABLE	BLANKING			SERIAL	Q1 THRU Q20
LOAD	↑	X	X	Load and shift†	Determined by	R20	Determined by BLANKING
	Not↑	X	X	No change	LATCH ENABLE‡	R20	
LATCH	X	L	X	As determined above	Stored data	R20	Determined by BLANKING
	X	H	X		New data	R20	
BLANK	X	X	H	As determined above	Determined by	R20	All L
	X	X	L		LATCH ENABLE‡	R20	LC1 thru LC20, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
†R20 takes on the state of R19, R19 takes on the state of R18, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.
‡New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 15 V
Supply voltage, V_{BB} . . . . . 70 V
Output voltage, V_O . . . . . 70 V
Input voltage, V_I . . . . . −0.3 V to V_{DD} +0.3 V
Output current, I_O . . . . . −40 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TL5812I . . . . . −40°C to 85°C
TL5812 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1. All voltage values are with respect to V_{SS}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1400 mW	11.2 mW/°C	896 mW	728 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions.

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5		15	V
Supply voltage, V_{BB}		0		60	V
Supply voltage, V_{SS}			0		V
High-level input voltage, V_{IH}		$V_{DD}-1.5$		$V_{DD}+0.3$	V
Low-level input voltage, V_{IL}		−0.3†		0.8	V
High-level output current, I_{OH}				−40	mA
Operating free-air temperature, T_A	TL5812I	−40		85	°C
	TL5812	0		70	

†The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over operating free-air temperature range, V_{DD} = 5 V to 15 V, V_{BB} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output	Q outputs	I_{OH} = −25 mA		57.5	58.2		V
		Serial outputs	V_{DD} = 5 V,	I_{OH} = −20 μA	4.5	4.9		
			V_{DD} = 15 V,	I_{OH} = −20 μA	14.5	14.9		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 1 mA,	BLANKING at V_{DD}		0.7	1.5	V
		Serial outputs	V_{DD} = 5 V,	I_{OL} = 20 μA		0.06	0.3	
			V_{DD} = 15 V,	I_{OL} = 20 μA		0.03	0.3	
I_{IH}	High-level input current		$V_I = V_{DD}$			0.3	1	μA
I_{IL}	Low-level input current		V_I = 0			−0.3	−1	μA
I_{OL}	Low-level output current (pull down current)		V_O = 60 V,	BLANKING at V_{DD}	2.5	3.2		μA
$I_{O(off)}$	Off-state output current		V_O = 0,	BLANKING at V_{DD}		< −1	−15	μA
I_{BB}	Supply current from V_{BB}		Outputs high			3.5	8	mA
			Outputs low			0.02	0.5	
I_{DD}	Supply current from V_{DD}		V_{DD} = 5 V			1.5	3	mA
			V_{DD} = 15 V			1.7	4	

‡All typical characteristics are at T_A = 25°C.

timing requirements over operating free-air temperature range

PARAMETER			MIN	MAX	UNIT
t_{wCKH}	Pulse duration, CLOCK high	V_{DD} = 5 V	500		ns
		V_{DD} = 15 V	100		
t_{wLEH}	Pulse duration, LATCH ENABLE high	V_{DD} = 5 V	500		ns
		V_{DD} = 15 V	100		
t_{suD}	Setup time, data before CLOCK↑	V_{DD} = 5 V	150		ns
		V_{DD} = 15 V	75		
t_{hD}	Hold time, data after CLOCK↑	V_{DD} = 5 V	150		ns
		V_{DD} = 15 V	75		
$t_{CKH-LEH}$	Delay time, CLOCK↑ to LATCH ENABLE high	V_{DD} = 5 V	150		ns
		V_{DD} = 15 V	75		

switching characteristics, V_{BB} = 60 V, T_A = 25°C

PARAMETER			MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, LATCH ENABLE to output	V_{DD} = 5 V		2.2		μs
		V_{DD} = 15 V		0.8		

PARAMETER MEASUREMENT INFORMATION

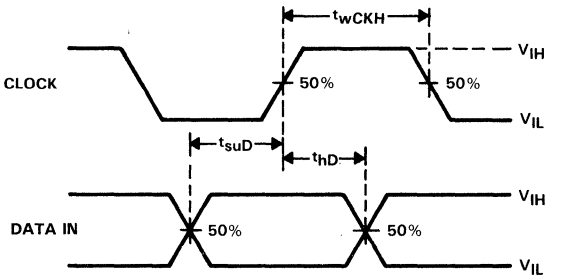


FIGURE 1. INPUT TIMING

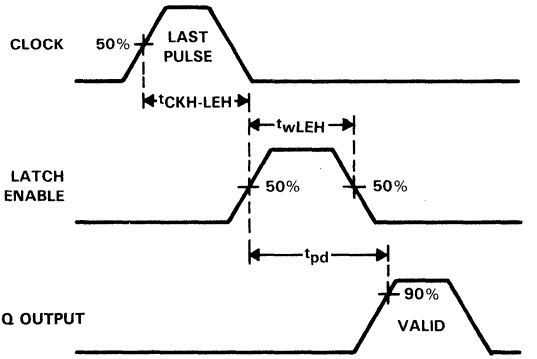


FIGURE 2. OUTPUT SWITCHING TIMES

THERMAL INFORMATION

DUTY CYCLE
vs
FREE-AIR TEMPERATURE

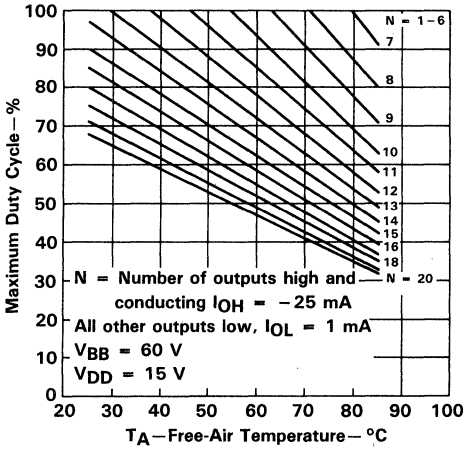
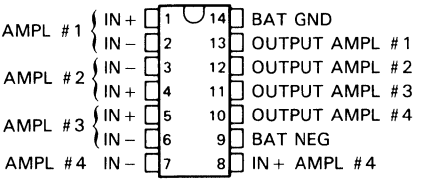


FIGURE 3

D2758, MARCH 1986—REVISED MARCH 1990

- **Designed for −52-V Battery Operation**
- **50-mA Output Current Capability**
- **Input Compatible with TTL and CMOS**
- **High Common-Mode Input Voltage Range**
- **Very Low Input Current**
- **Fail-Safe Disconnect Feature**
- **Built-In Output Clamp Diode**
- **Direct Replacement for National DS3680 and Fairchild μA3680**

D OR N PACKAGE
(TOP VIEW)

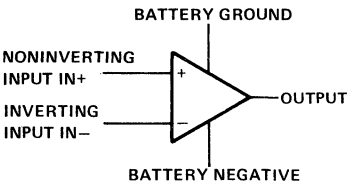


description

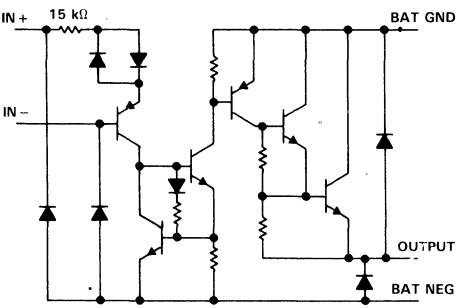
The DS3680I telephone relay driver is a monolithic integrated circuit designed to interface −48-V relay systems to TTL or other systems in telephone applications. It is capable of sourcing up to 50 mA from standard −52-V battery power. To reduce the effects of noise and IR drop between logic ground and battery ground, these drivers are designed to operate with a common-mode input range of ±20 V referenced to battery ground. The common-mode input voltages for the four drivers can be different, so a wide range of input elements can be accommodated. The high-impedance inputs are compatible with positive TTL and CMOS levels or negative logic levels. A clamp network is included in the driver outputs to limit high-voltage transients generated by the relay coil during switching. The complementary inputs ensure that the driver output will be "off" as a fail-safe condition when either output is open.

The DS3680I is characterized for operation from −40°C to 85°C.

symbol (each driver)



schematic diagram (each driver)



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range at BAT NEG, V_{B-} (see Note 1) . . . . . −70 V to 0.5 V
Input voltage range with respect to BAT GND . . . . . −70 V to 20 V
Input voltage range with respect to BAT NEG . . . . . −0.5 V to 70 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±20 V
Output current: resistive load . . . . . −100 mA
inductive load . . . . . −50 mA
Inductive output load . . . . . 5 H
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltages are with respect to the BAT GND terminal unless otherwise specified.
2. Differential input voltages are at the noninverting input terminal IN+ with respect to the inverting input terminal IN−.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{B-}	−10	−60	V
Input voltage, either input	−20†	20	V
High-level differential input voltage, V_{IDH}	2	20	V
Low-level differential input voltage, V_{IDL}	−20†	0.8	V
Operating free-air temperature, T_A	−40	85	°C

†The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for input voltage levels.

electrical characteristics over recommended operating free-air temperature range, V_{B-} = −52 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
I_{IH}	High-level input current (into IN+)	V_{ID} = 2 V			40	100	μA
		V_{ID} = 7 V			375	1000	
I_{IL}	Low-level input current (into IN+)	V_{ID} = 0.4 V			0.01	5	μA
		V_{ID} = −7 V			−1	−100	
$V_{O(on)}$	On-state output voltage	I_O = −50 mA,	V_{ID} = 2 V		−1.6	−2.1	V
$I_{O(off)}$	Off-state output current	$V_O = V_{B-}$	V_{ID} = 0.8 V		−2	−100	μA
			Inputs open		−2	−100	
I_R	Clamp diode reverse current	V_O = 0			2	100	μA
V_{OK}	Output clamp voltage	I_O = 50 mA			0.9	1.2	V
		I_O = −50 mA,	V_{B-} = 0		−0.9	−1.2	
$I_{B(on)}$	On-state battery current	All drivers on			−2	−4.4	mA
$I_{B(off)}$	Off-state battery current	All drivers off			−1	−100	μA

‡All typical values are at T_A = 25°C.

switching characteristics V_{B-} = −52 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{on}	Turn-on time	V_{ID} = 3-V pulse,	R_L = 1 kΩ,		1	10	μs
t_{off}	Turn-off time	L = 1 H,	See Figure 2		1	10	μs

PARAMETER MEASUREMENT INFORMATION

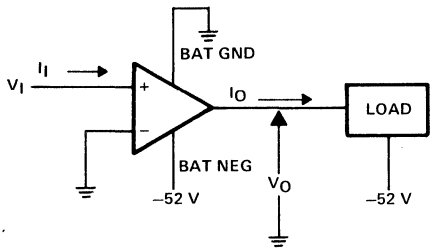
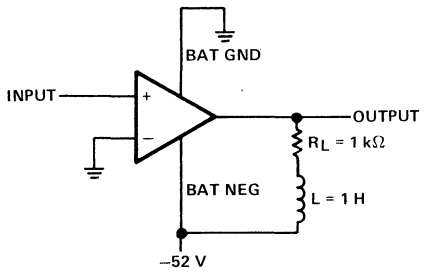
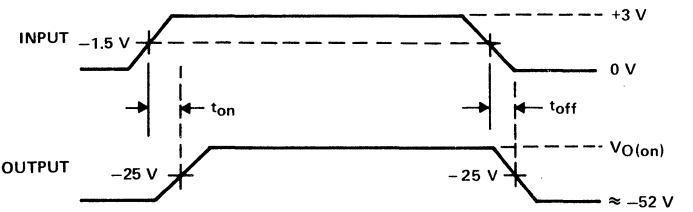


FIGURE 1. GENERALIZED TEST CIRCUIT, EACH DRIVER



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2. SWITCHING CHARACTERISTICS, EACH DRIVER

APPLICATION INFORMATION

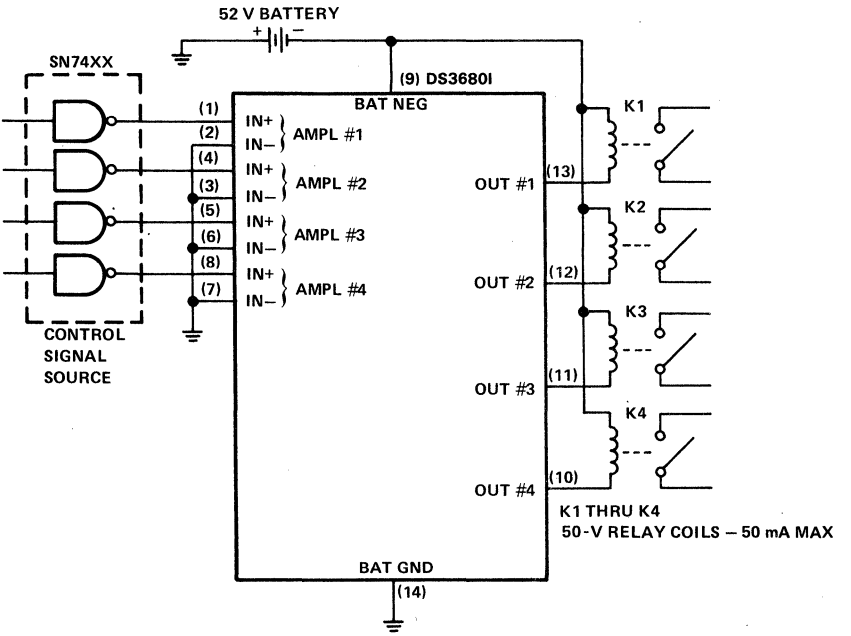
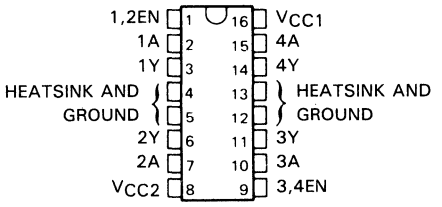


FIGURE 3. RELAY DRIVER

D2942, SEPTEMBER 1986–REVISED MAY 1990

- **1-A Output Current Capability Per Driver**
- **Pulsed Current 2-A Driver**
- **Wide Supply Voltage Range: 4.5 V to 36 V**
- **Separate Input-Logic Supply**
- **NE Package Designed for Heat Sinking**
- **Thermal Shutdown**
- **Internal ESD Protection**
- **High-Noise-Immunity Inputs**
- **Functional Replacement for SGS L293**

NE PACKAGE
(TOP VIEW)



FUNCTION TABLE
(EACH DRIVER)

INPUTS†		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

H = high-level
L = low-level
X = irrelevant
Z = high-impedance (off)

†In the thermal shutdown mode, the output is in the high-impedance state regardless of the input levels.

description

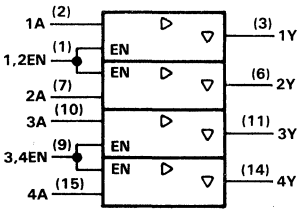
The L293 is a quadruple high-current half-H driver designed to provide bidirectional drive currents of up to one ampere at voltages from 4.5 V to 36 V. It is designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

All inputs are TTL-compatible. Each output is a complete totem-pole drive circuit with a Darlington transistor sink and a psuedo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs are active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

External high-speed output clamp diodes should be used for inductive transient suppression. A V_{CC1} terminal , separate from V_{CC2}, is provided for the logic inputs to minimize device power dissipation.

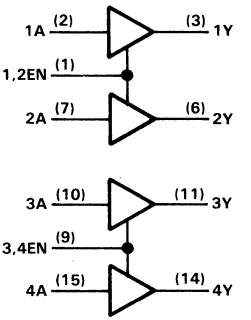
The L293 is designed for operation from 0°C to 70°C.

logic symbol‡

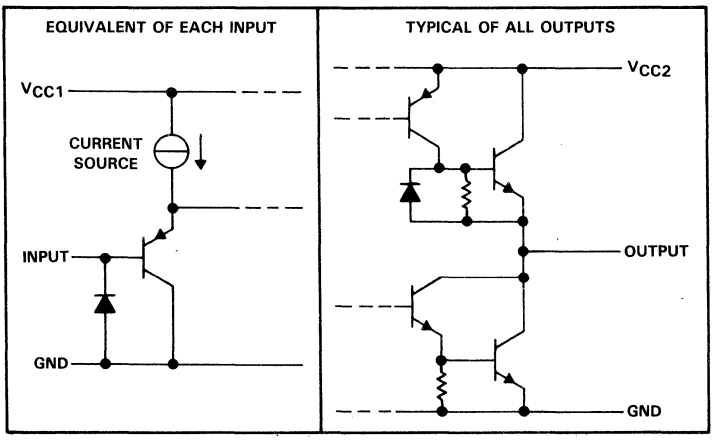


‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage, V_{CC1} (see Note 1) . . . . . 36 V
Output supply voltage, V_{CC2} . . . . . 36 V
Input voltage . . . . . 7 V
Output voltage range . . . . . −3 V to V_{CC2} +3 V
Peak output current (nonrepetitive, t ≤ 5 ms) . . . . . ±2 A
Continuous output current . . . . . ±1 A
Continuous total dissipation at (or below) 25 °C free-air temperature (see Notes 2 and 3) . . . . . 2075 mW
Continuous total dissipation at 80 °C case temperature (see Note 3) . . . . . 5000 mW
Operating case or virtual junction temperature range . . . . . −40 °C to 150 °C
Storage temperature range . . . . . −65 °C to 150 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260 °C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25 °C free-air temperature, derate linearly at the rate of 16.6 mW/°C.
3. For operation above 25 °C case temperature, derate linearly at the rate of 71.4 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	MAX	UNIT
Logic supply voltage, V_{CC1}		4.5	7	V
Output supply voltage, V_{CC2}			36	V
High-level input voltage, V_{IH}	$V_{CC1} \leq 7$ V	2.3		V
	$V_{CC1} \geq 7$ V	2.3	7	
Low-level input voltage, V_{IL}		−0.3†	1.5	V
Operating free-air temperature, T_A		0	70	°C

†The algebraic convention, in which the least positive (most negative) designated minimum, is used in this data sheet for logic voltage levels.

TEXAS INSTRUMENTS
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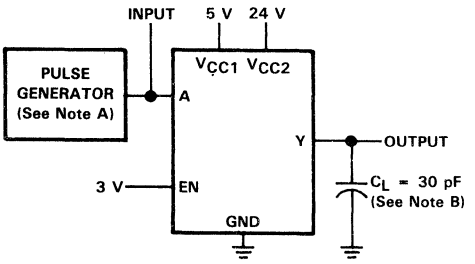
electrical characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −1 A		V_{CC2}−1.8	V_{CC2}−1.4		V
V_{OL}	Low-level output voltage		I_{OL} = 1 A			1.2	1.8	V
I_{IH}	High-level input current	A	V_I = 7 V			0.2	100	μA
		EN				0.2	±10	
I_{IL}	Low-level input current	A	V_I = 0			−3	−10	μA
		EN				−2	−100	
I_{CC1}	Logic supply current		I_O = 0	All outputs at high level		13	22	mA
				All outputs at low level		35	60	
				All outputs at high impedance		8	24	
I_{CC2}	Output supply current		I_O = 0	All outputs at high level		14	24	mA
				All outputs at low level		2	6	
				All outputs at high impedance		2	4	

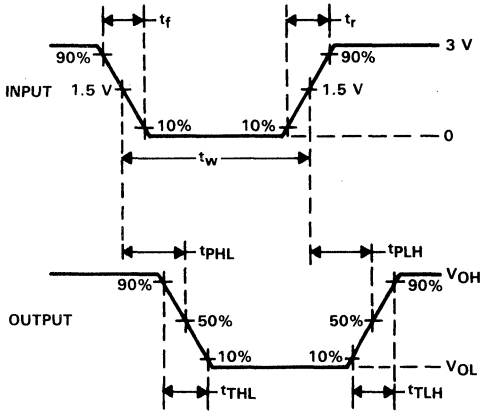
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from A input	C_L = 30 pF, See Figure 1		800		ns
t_{PHL}	Propagation delay time, high-to-low-level output from A input			400		ns
t_{TLH}	Transition time, low-to-high-level output			300		ns
t_{THL}	Transition time, high-to-low-level output			300		ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, t_w = 10 μs, PRR = 5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES

APPLICATION INFORMATION

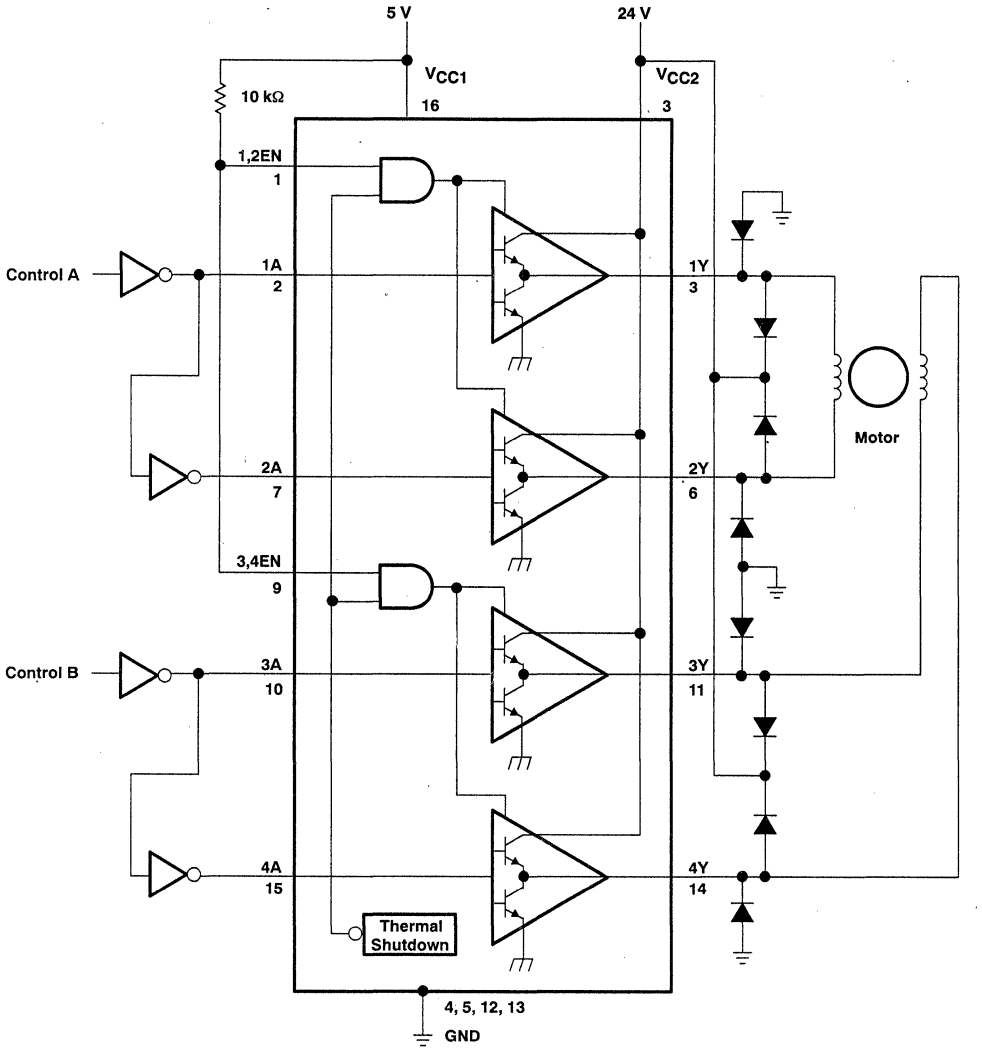


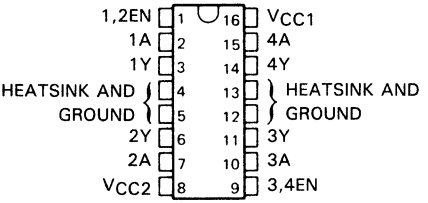
Figure 2. Two-Phase Motor Driver

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D3511, SEPTEMBER 1986—REVISED MAY 1990

- **600-mA Output Current Capability Per Driver**
- **Pulsed Current 1.2-A Per Driver**
- **Output Clamp Diodes for Inductive Transient Suppression**
- **Wide Supply Voltage Range: 4.5 V to 36 V**
- **Separate Input-Logic Supply**
- **Thermal Shutdown**
- **Internal ESD Protection**
- **High-Noise-Immunity Inputs**
- **Functional Replacement for SGS L293D**

NE PACKAGE
(TOP VIEW)



FUNCTION TABLE
(EACH DRIVER)

INPUTS†		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

H = high-level
L = low-level
X = irrelevant
Z = high-impedance (off)

†In the thermal shutdown mode, the output is in the high-impedance state regardless of the input levels.

description

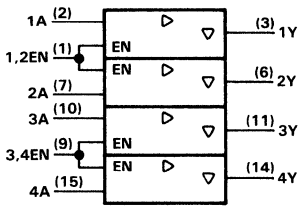
The L293D is a quadruple high-current half-H driver designed to provide bidirectional drive currents of up to 600 mA at voltages from 4.5 V to 36 V. It is designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

All inputs are TTL-compatible. Each output is a complete totem-pole drive circuit with a Darlington transistor sink and a psuedo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high,the associated drivers are enabled and their outputs are active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

A V_{CC1} terminal, separate from V_{CC2}, is provided for the logic inputs to minimize device power dissipation.

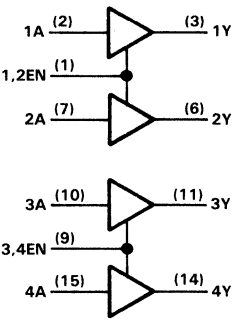
The L293D is designed for operation from 0°C to 70°C.

logic symbol‡

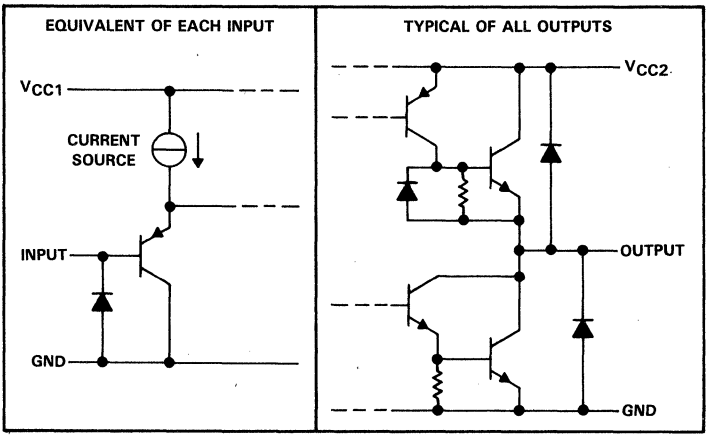


‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage, V_{CC1} (see Note 1) . . . . . 36 V
Output supply voltage, V_{CC2} . . . . . 36 V
Input voltage . . . . . 7 V
Output voltage range . . . . . −3 V to V_{CC2}+3 V
Peak output current (nonrepetitive, t ≤ 100 μs) . . . . . ±1.2 A
Continuous output current . . . . . ±600 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Notes 2 and 3) . . . . . 2075 mW
Continuous total dissipation at 80°C case temperature (see Note 3) . . . . . 5000 mW
Operating case or virtual junction temperature range . . . . . −40°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C.
3. For operation above 25°C case temperature, derate linearly at the rate of 71.4 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	MAX	UNIT
Logic supply voltage, V_{CC1}		4.5	7	V
Output supply voltage, V_{CC2}		V_{CC1}	36	V
High-level input voltage, V_{IH}	V_{CC1} ≤ 7 V	2.3	V_{CC1}	V
	V_{CC1} ≥ 7 V	2.3	7	
Low-level input voltage, V_{IL}		−0.3†	1.5	V
Operating free-air temperature, T_A		0	70	°C

†The algebraic convention, in which the least positive (most negative) designated minimum, is used in this data sheet for logic voltage levels.

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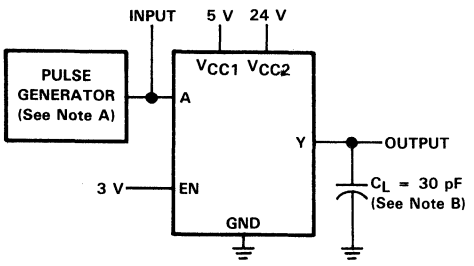
electrical characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −0.6 A		V_{CC2}−1.8	V_{CC2}−1.4		V
V_{OL}	Low-level output voltage		I_{OL} = 0.6 A			1.2	1.8	V
V_{OKH}	High-level output clamp voltage		I_{OK} = 0.6 A			V_{CC2}+1.3		V
V_{OKL}	Low-level output clamp voltage		I_{OK} = −0.6 A			1.3		V
I_{IH}	High-level input current	A	V_I = 7 V			0.2	100	μA
		EN				0.2	±10	
I_{IL}	Low-level input current	A	V_I = 0			−3	−10	μA
		EN				−2	−100	
I_{CC1}	Logic supply current		I_O = 0	All outputs at high level		13	22	mA
				All outputs at low level		35	60	
				All outputs at high impedance		8	24	
I_{CC2}	Output supply current		I_O = 0	All outputs at high level		14	24	mA
				All outputs at low level		2	6	
				All outputs at high impedance		2	4	

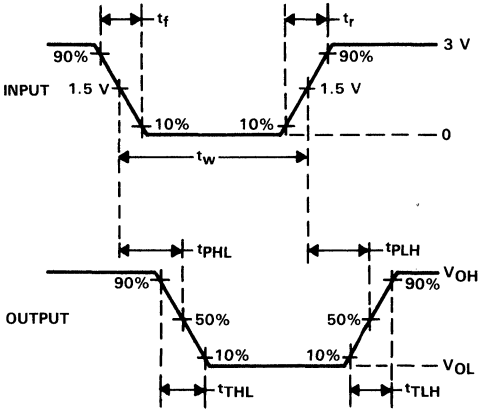
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from A input	C_L = 30 pF, See Figure 1		800		ns
t_{PHL}	Propagation delay time, high-to-low-level output from A input			400		ns
t_{TLH}	Transition time, low-to-high-level output			300		ns
t_{THL}	Transition time, high-to-low-level output			300		ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, t_w = 10 μs, PRR = 5 kHz, Z_o = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES

APPLICATION INFORMATION

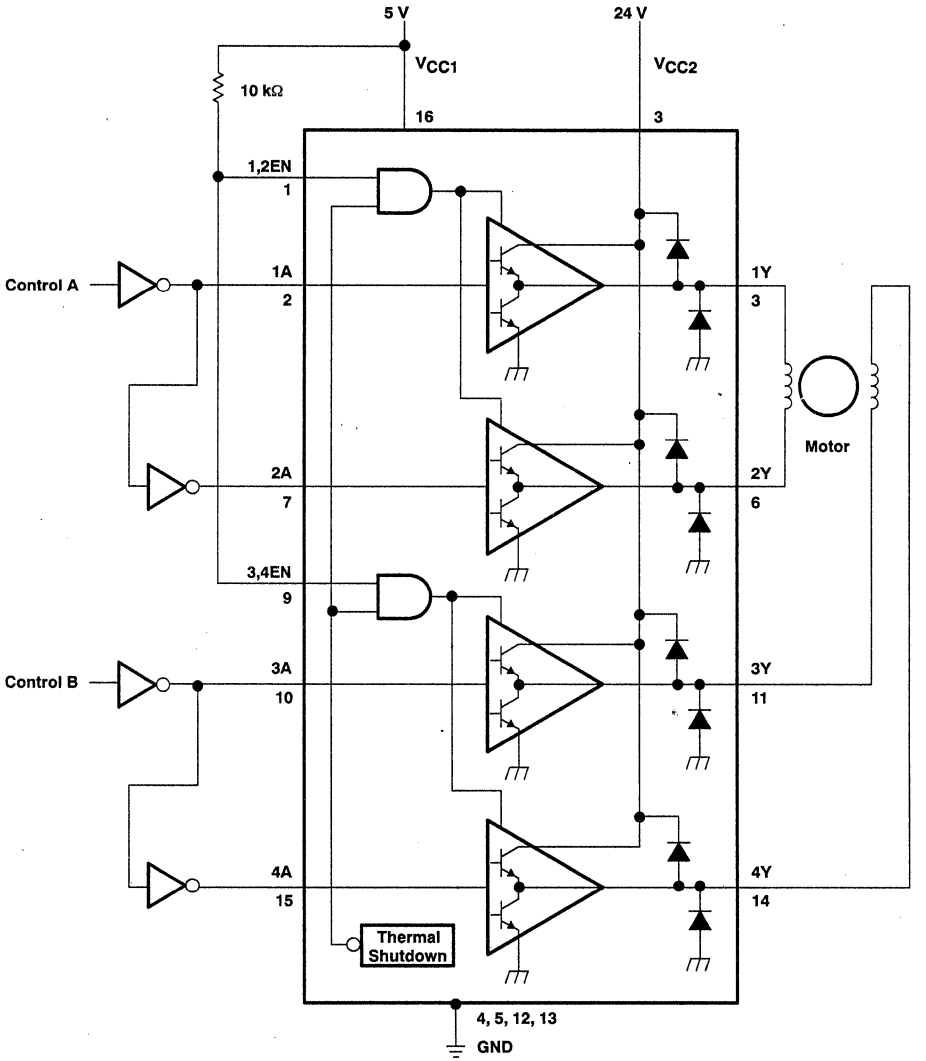


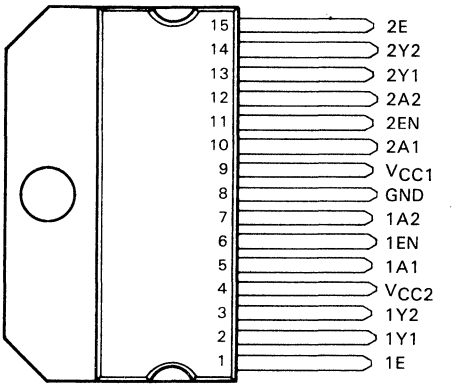
Figure 2. Two-Phase Motor Driver

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D2942, OCTOBER 1986—REVISED JUNE 1990

- **2-A Output Current Capability per Full-H Driver**
- **Wide Range of Output Supply Voltage . . . 5 V to 46 V**
- **Separate Input-Logic Supply Voltage**
- **Thermal Shutdown**
- **Internal Electrostatic Discharge Protection**
- **High Noise Immunity**
- **Functional Replacement for SGS L298**

KV PACKAGE
(TOP VIEW)



The tab is electrically connected to pin 8.

description

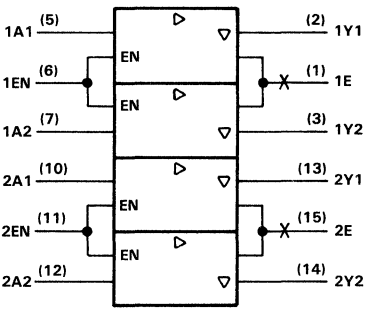
The L298 is a dual high-current full-H driver designed to provide bidirectional drive currents of up to two amperes at voltages from 5 V to 46 V. It is designed to drive inductive loads such as relays, solenoids, dc motors, stepping motors, and other high-current or high-voltage loads in positive-supply applications. All inputs are TTL compatible. Each output (Y) is a complete totem-pole drive with a Darlington transistor sink and a psuedo-Darlington source. Each full-H driver is enabled separately. Outputs 1Y1 and 1Y2 are enabled by 1EN and outputs 2Y1 and 2Y2 are enabled by 2EN. When an EN input is high, the associated channels are active. When an EN input is low, the associated channels are off (i.e., in the high-impedance state).

Each half of the device forms a full-H reversible driver suitable for solenoid or motor applications. The current in each full-H driver can be monitored by connecting a resistor between the sense output terminal 1E and ground and another resistor between sense output terminal 2E and ground.

External high-speed output-clamp diodes should be used for inductive transient suppression. To minimize device power dissipation, a V_{CC1} supply voltage, separate from V_{CC2}, is provided for the logic inputs.

The L298 is designed for operation from 0°C to 70°C.

logic symbol†



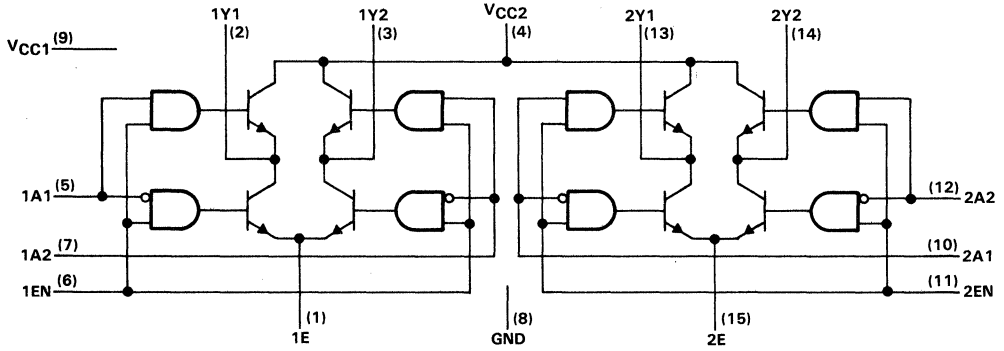
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(EACH CHANNEL)

INPUTS‡		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

‡ In the thermal shutdown mode, the outputs are in the high-impedance state regardless of the input levels.
H = high-level
L = low-level
X = irrelevant
Z = high-impedance (off)

logic diagram (positive logic)



absolute maximum ratings over operating temperature range (unless otherwise noted)

Logic supply voltage, V_{CC1}, (see Note 1) . . . . . 7 V
Output supply voltage, V_{CC2} . . . . . 50 V
Input voltage range at A or EN, V_I . . . . . −0.3 to 7 V
Output voltage range, V_O . . . . . −2 V to V_{CC2}+2 V
Emitter terminal (1E and 2E) voltage range . . . . . −0.5 to 2.3 V
Emitter terminal (1E and 2E) voltage (nonrepetitive, $t_w \leq 50\ \mu s$) . . . . . −1 V
Peak output current, I_{OM}, (nonrepetitive, $t_w \leq 0.1$ ms) . . . . . ±3 A
(repetitive, $t_w \leq 10$ ms, duty cycle ≤ 80%) . . . . . ±2.5 A
Continuous output current, I_O . . . . . ±2 A
Peak combined output current for each full-H driver (see Note 2)
(nonrepetitive, $t_w \leq 0.1$ ms) . . . . . ±3 A
(repetitive, $t_w \leq 10$ ms, duty cycle ≤ 80%) . . . . . ±2.5 A
Continuous combined output current for each full-H driver (see Note 2) . . . . . 3.575 W
Continuous dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 3.575 W
Continuous dissipation at (or below) 75°C case temperature (see Note 3) . . . . . 25 W
Operating free-air, case, or virtual junction temperature range . . . . . −40°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal, unless otherwise noted.
2. Combined output current applies to each of the two full-H drivers individually. This current is the sum of the currents at outputs 1Y1 and 1Y2 for full-H driver 1 and the sum of the currents at outputs 2Y1 and 2Y2 for full-H driver 2. The full-H drivers may carry the rated combined current simultaneously.
3. For operation above 25°C free-air temperature, derate linearly at the rate of 28.6 mW/°C. For operation above 75°C case temperature, derate linearly at the rate of 333 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	MAX	UNIT
Logic supply voltage, V_{CC1}		4.5	7	V
Output supply voltage, V_{CC2}		5	46	V
Emitter terminal (1E or 2E) voltage, V_E (see Note 4)		−0.5†	2	V
			$V_{CC1}-3.5$	
			$V_{CC2}-4$	
High-level input voltage, V_{IH} (see Note 4)	A	2.3	V_{CC1}	V
			$V_{CC2}-2.5$	
	EN	2.3	7	
			V_{CC1}	
Low-level input voltage at A or EN, V_{IL}		−0.3†	1.5	V
Output current, I_O			±2	A
Commutation frequency, f_c			40	kHz
Operating free-air temperature, T_A		0	70	°C

†The algebraic convention, in which the least positive (most negative) designated minimum, is used in this data sheet for emitter terminal voltage and logic voltage levels.

NOTE 4: For optimum device performance, the maximum recommended voltage at any A input is 2.5 V lower then V_{CC2}, the maximum recommended voltage at any EN input is V_{CC1}, and the maximum recommended voltage at any emitter terminal is 3.5 V lower than V_{CC1} and 4 V lower than V_{CC2}.

electrical characteristics, V_{CC1} = 5 V, V_{CC2} = 42 V, V_E = 0, T_J = 25°C (unless otherwise noted)

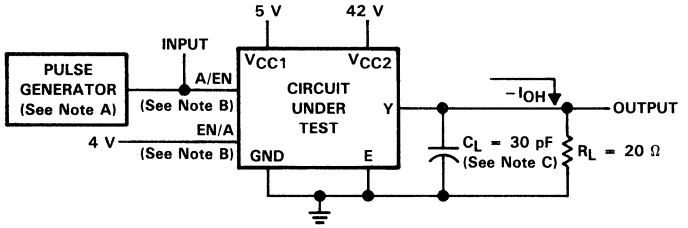
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −1 A		$V_{CC2}-1.8$	$V_{CC2}-1.2$		V
			I_{OH} = −2 A		$V_{CC2}-2.8$	$V_{CC2}-1.8$		
V_{OL}	Low-level output voltage		I_{OL} = 1 A			$V_E+1.2$	$V_E+1.8$	V
			I_{OL} = 2 A			$V_E+1.7$	$V_E+2.6$	
V_{drop}	Total source plus sink output voltage drop		I_{OH} = −1 A, I_{OL} = 1 A	See Note 5		2.4	3.4	V
			I_{OH} = −2 A, I_{OL} = 2 A			3.5	5.2	
I_{IH}	High-level input current	A	$V_I = V_{IH}$			30	100	μA
		EN	$V_I = V_{IH} \le V_{CC1}-0.6$ V			30	100	
I_{IL}	Low-level input current		V_I = 0 to 1.5 V				−10	μA
I_{CC1}	Logic supply current		I_O = 0	All outputs at high level		7	12	mA
				All outputs at low level		24	32	
				All outputs at high impedance		4	6	
I_{CC2}	Output supply current		I_O = 0	All outputs at high level		38	50	mA
				All outputs at low level		13	20	
				All outputs at high impedance			2	

NOTE 5. The V_{drop} specification applies for I_{OH} and I_{OL} applied simultaneously to different output channels.
$V_{drop} = V_{CC2} - V_{OH} + V_{OL} - V_E$

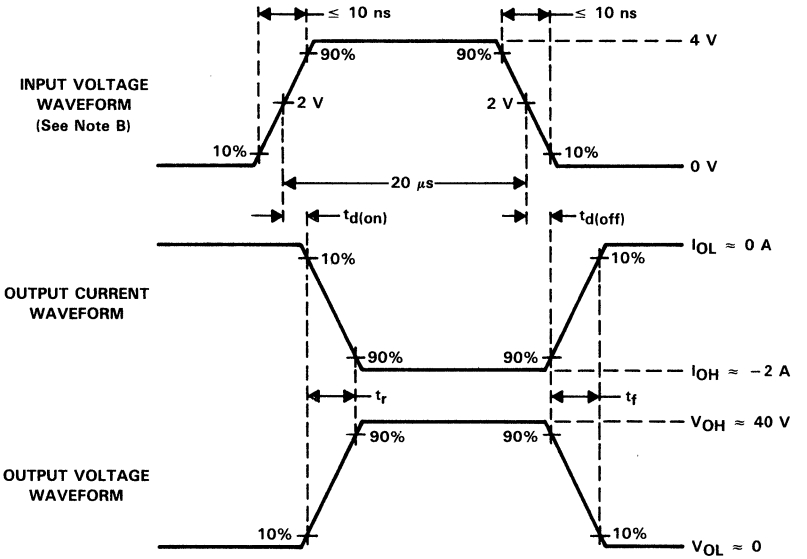
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 42 V, V_E = 0, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Source current turn-on delay time from A input	C_L = 30 pF, See Figure 1		2.5		μs
$t_{d(off)}$	Source current turn-off delay time from A input			1.7		μs
t_r	Source current rise time (turning on)			0.4		μs
t_f	Source current fall time (turning off)			0.2		μs
$t_{d(on)}$	Source current turn-on delay time from EN input			2.5		μs
$t_{d(off)}$	Source current turn-off delay time from EN input			1.7		μs
$t_{d(on)}$	Sink current turn-on delay time from A input	C_L = 30 pF, See Figure 2		1.5		μs
$t_{d(off)}$	Sink current turn-off delay time from A input			0.7		μs
t_r	Sink current rise time (turning on)			0.2		μs
t_f	Sink current fall time (turning off)			0.2		μs
$t_{d(on)}$	Sink current turn-on delay time from EN input			1.5		μs
$t_{d(off)}$	Sink current turn-off delay time from EN input			0.7		μs

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

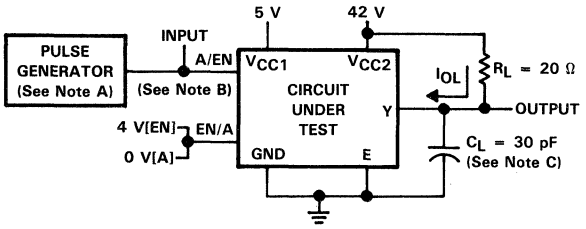


VOLTAGE AND CURRENT WAVEFORMS

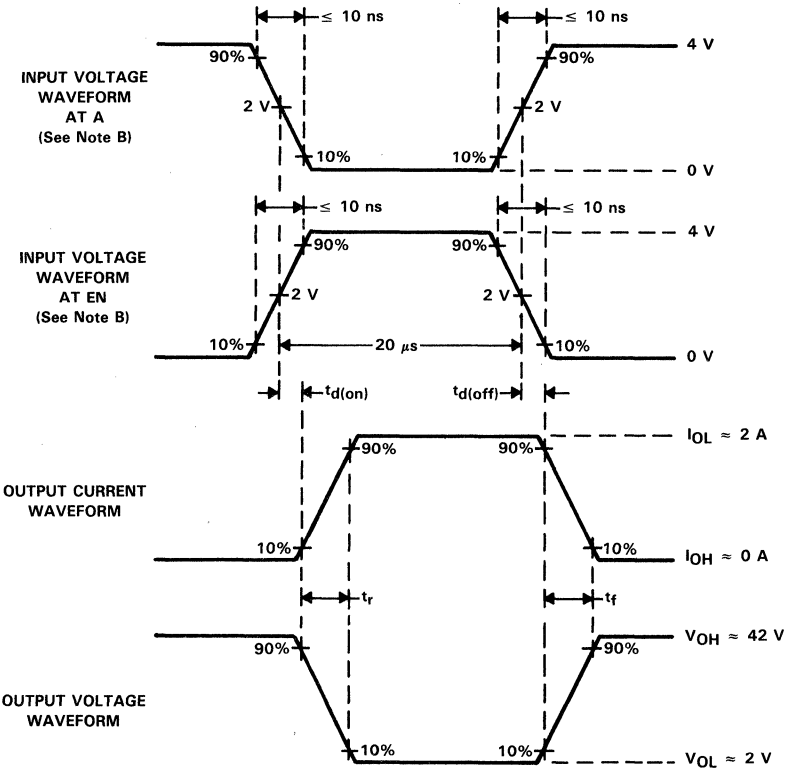
NOTES: A. The pulse generator has the following characteristics: PRR = 2 kHz, Z_O = 50 Ω.
B. EN is at 4 V if A is used as the switching input. A is at 4 V if EN is the switching input.
C. C_L includes probe and jig capacitance.

FIGURE 1. SOURCE CURRENT SWITCHING TIMES FROM DATA AND ENABLE INPUTS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 2 kHz, Z_O = 50 Ω.
B. EN is at 4 V if A is used as the switching input. A is at 0 V if EN is the switching input.
C. C_L includes probe and jig capacitance.

FIGURE 2. SINK CURRENT SWITCHING TIMES FROM DATA AND ENABLE INPUTS

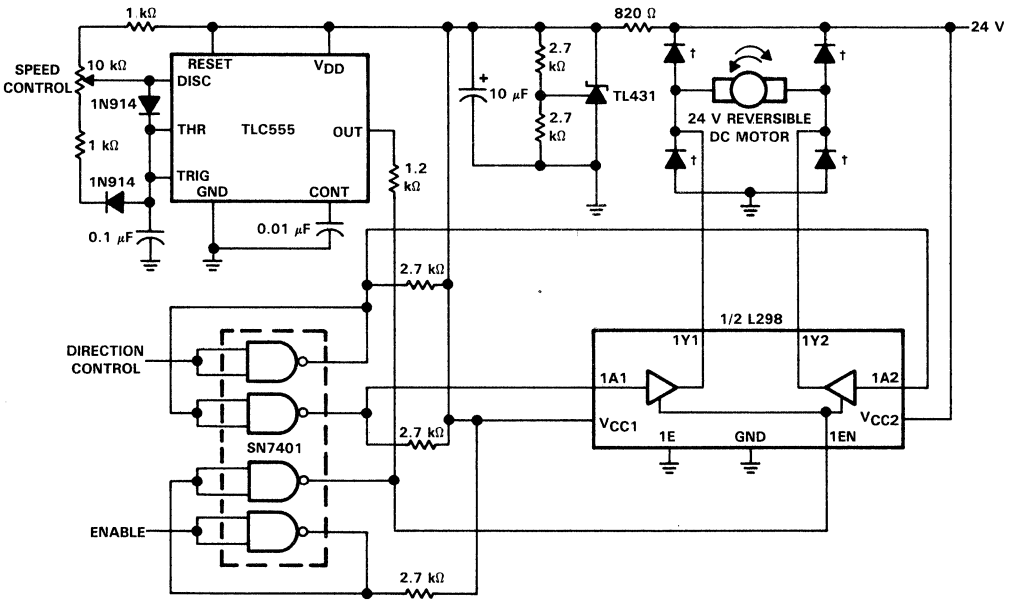
APPLICATION INFORMATION

This circuit shows one half of an L298 used to provide full-H bridge drive for a 24-V 2-A dc motor. Speed control is achieved with a TLC555 timer. This provides variable duty cycle pulses to the EN input of the L298. In this configuration, the operating frequency is approximately 1.2 kHz. The duty cycle is adjustable from 10% to 90% to provide a wide range of motor speeds. The motor direction is determined by the logic level at the direction control input. The circuit may be enabled or disabled by the logic level at the EN input. A 5-V supply for the logic and timer circuit is provided by a TL431 shunt regulator. For circuit operation, refer to the function table.

FUNCTION TABLE

ENABLE	DIRECTION CONTROL	1Y1	1Y2
H	H	source	sink
H	L	sink	source
L	X	disabled	disabled

X = don't care H = high level L = low level



†Diodes are 1N4934 or equivalent.

FIGURE 3. L298 AS BIDIRECTIONAL DC MOTOR DRIVER

PERIPHERAL DRIVERS FOR HIGH-CURRENT SWITCHING AT VERY HIGH SPEEDS

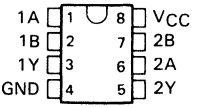
- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 20 V (After Conducting 300 mA)
- High-Speed Switching
- Circuit Flexibility for Varied Applications
- TTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Plastic DIP (P) with Copper Lead Frame Provides Cooler Operation and Improved Reliability
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

SUMMARY OF SERIES 55451B/75451B

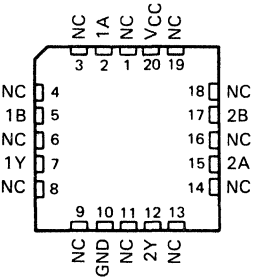
DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN55451B	AND†	FK,JG
SN55452B	NAND	FK,JG
SN55453B	OR	FK,JG
SN55454B	NOR	FK,JG
SN75451B	AND	D,P
SN75452B	NAND	D,P
SN75453B	OR	D,P
SN75454B	NOR	D,P

†With output transistor base connected externally to output of gate.

SN55451B, SN55452B,
SN55453B, SN55454B . . . JG PACKAGE
SN75451B, SN75452B,
SN75453B, SN75454B . . . D OR P PACKAGE
(TOP VIEW)



SN55451B, SN55452B,
SN55453B, SN55454B, . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

Series SN55451B/75451B dual peripheral drivers are a family of versatile devices designed for use in systems that employ TTL logic. This family is functionally interchangeable with and replaces the SN75450 family and the SN75450A family devices manufactured previously. The speed of the SN55451B/SN75451B family is equal to that of the SN75450 family, and the parts are designed to ensure freedom from latch-up. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN55451B/SN75451B, SN55452B/SN75452B, SN55453B/SN75453B, and SN55454B/SN75454B are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic), with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

Series SN55451B drivers are characterized for operation over the full military range of −55°C to 125°C. Series SN75451B drivers are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55451B SN55452B SN55453B SN55454B	SN75451B SN75452B SN75453B SN75454B	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage		5.5	5.5	V
Interemitter voltage (see Note 2)		5.5	5.5	V
Off-state output voltage		30	30	V
Continuous collector or output current (see Note 4)		400	400	mA
Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 4)		500	500	mA
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range, T_A		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300		°C
Lead temperature 1,6 mm (1,16 inch) from case for 10 seconds	D or P package		260	°C

NOTES: 1. Voltage values are with respect to the network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

DISSIPATION RATING TABLE

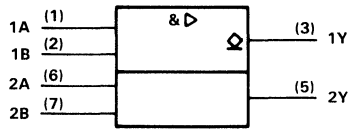
PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	—

recommended operating conditions

	SERIES 55451B			SERIES 75451B			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
Operating free-air temperature, T_A	−55		125	0		70	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

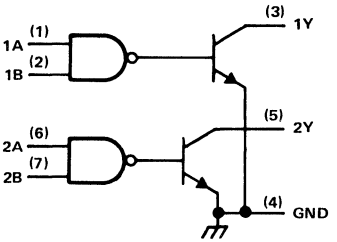
FUNCTION TABLE (EACH DRIVER)

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

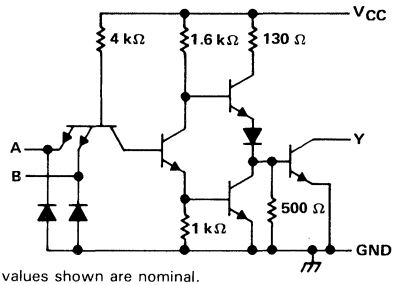
positive logic: $Y = AB$ or $\overline{\overline{A}+\overline{B}}$

Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

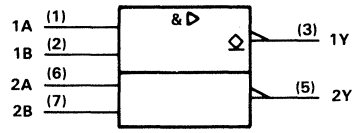
PARAMETER		TEST CONDITIONS‡	SN55451B MIN	SN55451B TYP§	SN55451B MAX	SN75451B MIN	SN75451B TYP§	SN75451B MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{OH} = 30 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		7	11		7	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		52	65		52	65	mA

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

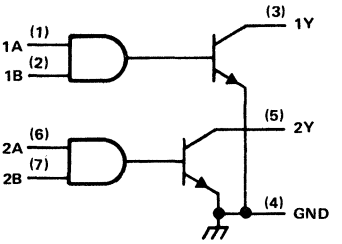
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		18	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output				18	25	ns
t_{TLH}	Transition time, low-to-high-level output				5	8	ns
t_{THL}	Transition time, high-to-low-level output				7	12	ns
V_{OH}	High-level output voltage after switching	SN55451B	V_S = 20 V, $I_O \approx$ 300 mA, See Figure 2		V_S−6.5		mV
		SN75451B			V_S−6.5		

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

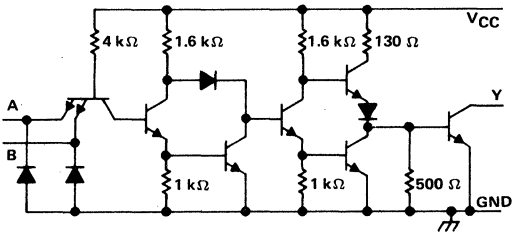


FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

positive logic:
$Y = \overline{AB}$ or $\overline{A} + \overline{B}$

schematic (each driver)



Pin numbers shown are for D, JG, and P packages.

Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

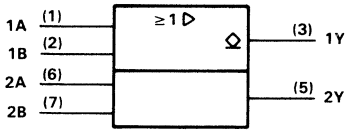
PARAMETER		TEST CONDITIONS‡		SN55452B			SN75452B			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 30 V	V_{IL} = 0.8 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 100 mA	V_{IH} = MIN		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, I_{OL} = 300 mA	V_{IH} = MIN,		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V		−1.1	−1.6		−1.1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX,	V_I = 0		11	14		11	14	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX,	V_I = 5 V		56	71		56	71	mA

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		26	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				24	35	ns
t_{TLH}	Transition time, low-to-high-level output				5	8	ns
t_{THL}	Transition time, high-to-low-level output				7	12	ns
V_{OH}	High-level output voltage after switching	SN55452B	V_S = 20 V, $I_O \approx$ 300 mA, See Figure 2		V_S−6.5		mV
		SN75452B			V_S−6.5		

logic symbol†



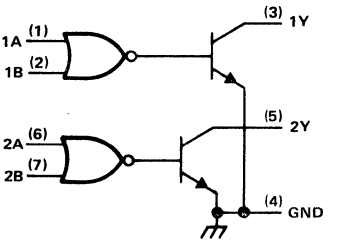
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE (EACH DRIVER)

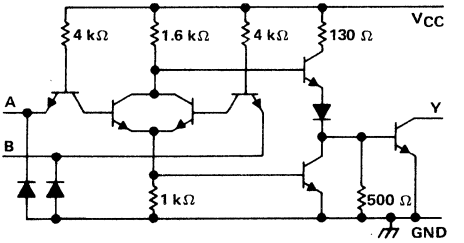
A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

positive logic:
$Y = A + B$ or $\overline{\overline{A}\,\overline{B}}$

logic diagram (positive logic)



schematic (each driver)



Pin numbers shown are for D, JG, and P packages.

Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

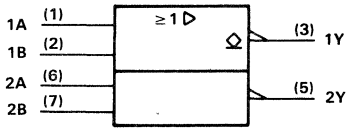
PARAMETER		TEST CONDITIONS‡		SN55453B			SN75453B			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 30 V	V_{IH} = MIN,			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 100 mA	V_{IL} = 0.8 V,		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, I_{OL} = 300 mA	V_{IL} = 0.8 V,		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX,	V_I = 5 V		8	11		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX,	V_I = 0		54	68		54	68	mA

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

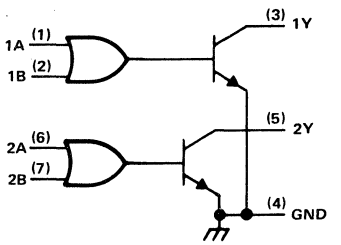
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		18	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output				16	25	ns
t_{TLH}	Transition time, low-to-high-level output				5	8	ns
t_{THL}	Transition time, high-to-low-level output				7	12	ns
V_{OH}	High-level output voltage after switching	SN55453B	V_S = 20 V, $I_O \approx$ 300 mA, See Figure 2	V_S−6.5			mV
		SN75453B		V_S−6.5			

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

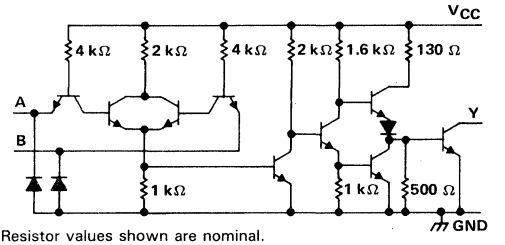


FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

positive logic:
$Y = \overline{A+B}$ or $\overline{AB}$

schematic (each driver)



Pin numbers shown are for D, JG, and P packages.

Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

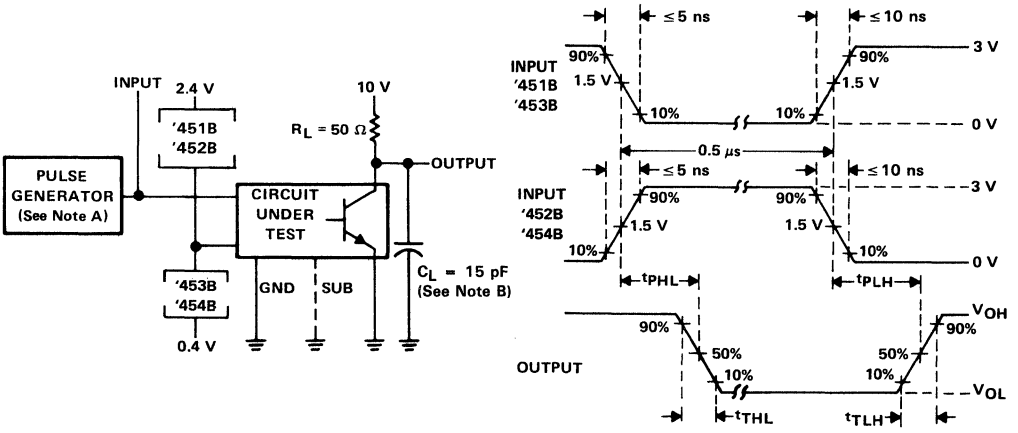
PARAMETER		TEST CONDITIONS‡		SN55454B			SN75454B			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 30 V	V_{IL} = 0.8 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 100 mA	V_{IH} = MIN		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, I_{OL} = 300 mA	V_{IH} = MIN,		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX,	V_I = 0		13	17		13	17	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX,	V_I = 5 V		61	79		61	79	mA

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		27	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				24	35	ns
t_{TLH}	Transition time, low-to-high-level output				5	8	ns
t_{THL}	Transition time, high-to-low-level output				7	12	ns
V_{OH}	High-level output voltage after switching	SN55454B	V_S = 20 V, $I_O \approx$ 300 mA, See Figure 2		V_S−6.5		mV
		SN75454B		V_S−6.5			

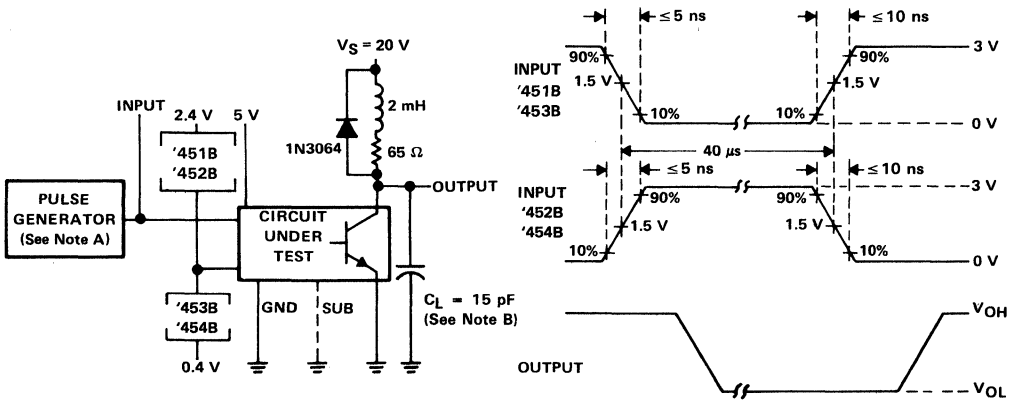
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES OF COMPLETE DRIVERS



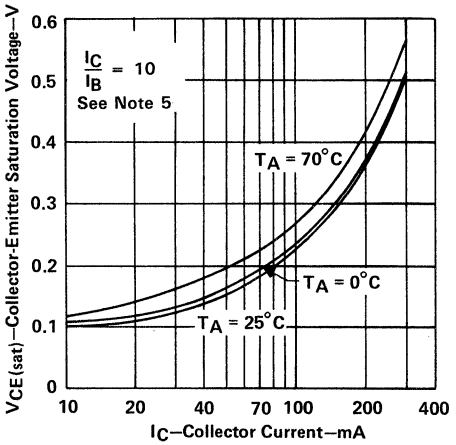
TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 2. LATCH-UP TEST OF COMPLETE DRIVERS

TYPICAL CHARACTERISTICS

TRANSISTOR
COLLECTOR-EMITTER SATURATION VOLTAGE
vs
COLLECTOR CURRENT



NOTE 5: These parameters must be measured using pulse techniques, t_w = 300 μs, duty cycle $\leq$2%.

FIGURE 3

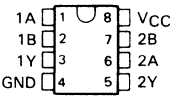
PERIPHERAL DRIVERS FOR HIGH-VOLTAGE, HIGH-CURRENT DRIVER APPLICATIONS

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 30 V (After Conducting 300 mA)
- Medium-Speed Switching
- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Plastic DIP (P) with Copper Lead Frame for Cooler Operation and Improved Reliability
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

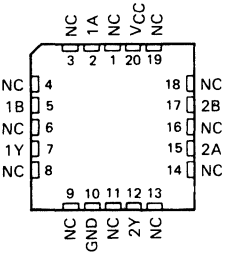
SUMMARY OF SERIES 55461/75461

DEVICE	LOGIC	PACKAGES
SN55461	AND	FK,JG
SN55462	NAND	FK,JG
SN55463	OR	FK,JG
SN55464	NOR	FK,JG
SN75461	AND	D,P
SN75462	NAND	D,P
SN75463	OR	D,P

SN55461, SN55462,
SN55463, SN55464 . . . JG PACKAGE
SN75461, SN75462,
SN75463 . . . D OR P PACKAGE
(TOP VIEW)



SN55461, SN55462,
SN55463, SN55464, . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These dual peripheral drivers are functionally interchangeable with SN55451B through SN55454B and SN75451B through SN75453B peripheral drivers, but are designed for use in systems that require higher breakdown voltages than those devices can provide at the expense of slightly slower switching speeds. Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN55461/SN75461, SN55462/SN75462, SN55463/SN75463, and SN55464 are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic), with the output of the gates internally connected to the bases of the n-p-n output transistors.

Series SN55461 drivers are characterized for operation over the full military temperature range of −55°C to 125°C; Series SN75461 drivers are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55461 SN55462 SN55463 SN55464	SN75461 SN75462 SN75463	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage		5.5	5.5	V
Interemitter voltage (see Note 2)		5.5	5.5	V
Off-state output voltage		35	35	V
Continuous collector or output current (see Note 3)		400	400	mA
Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 3)		500	500	mA
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range, T_A		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

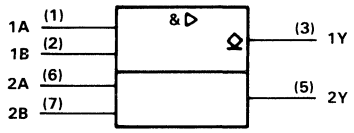
DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	–
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	–

recommended operating conditions

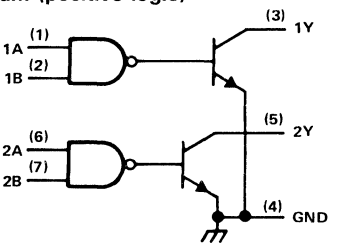
	SN55461 THRU SN55464			SN75461 THRU SN75463			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
Operating free-air temperature, T_A	−55		125	0		70	°C

logic symbol†



† This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)

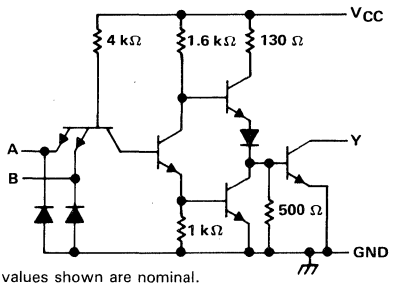


FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

positive logic:
$Y = AB$ or $\overline{\overline{A} + \overline{B}}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

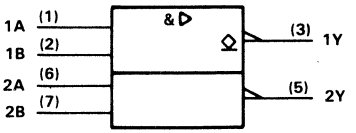
PARAMETER		TEST CONDITIONS†	SN55461			SN75461			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{OH} = 35 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		8	11		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		56	76		56	76	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditons.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

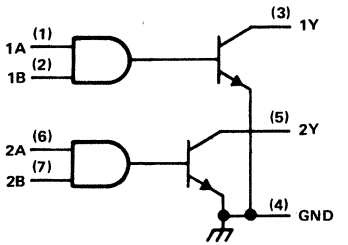
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		$I_O \approx$ 200 mA, R_L = 50 Ω,	C_L = 15 pF, See Figure 1		30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output					25	40	ns
t_{TLH}	Transition time, low-to-high-level output					8	20	ns
t_{THL}	Transition time, high-to-low-level output					10	20	ns
V_{OH}	High-level output voltage after switching	SN55461	V_S = 30 V, See Figure 2	$I_O \approx$ 300 mA,	V_S−10			mV
		SN75461			V_S−10			

logic symbol†



† This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)

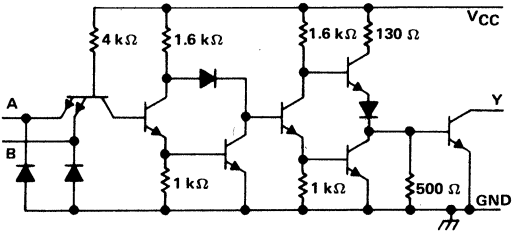


FUNCTION TABLE (EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

positive logic:
$Y = \overline{AB}$ or $\overline{A} + \overline{B}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

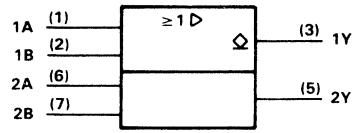
PARAMETER		TEST CONDITIONS†	SN55462			SN75462			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 35 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IH} = MIN, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1.1	−1.6		−1.1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 0		13	17		13	17	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 5 V		61	76		61	76	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

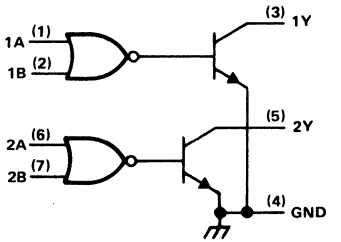
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		45	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output				30	50	ns
t_{TLH}	Transition time, low-to-high-level output				13	25	ns
t_{THL}	Transition time, high-to-low-level output				10	20	ns
V_{OH}	High-level output voltage after switching	SN55462	V_S = 30 V, $I_O \approx$ 300 mA, See Figure 2		V_S−10		mV
		SN75462			V_S−10		

logic symbol†



†This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)

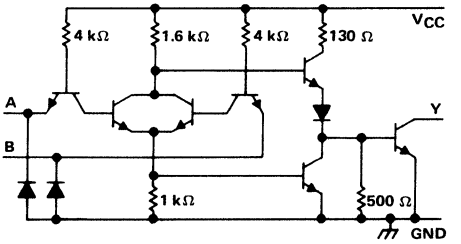


FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

positive logic:
$Y = A + B$ or $\overline{\overline{A}\,\overline{B}}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

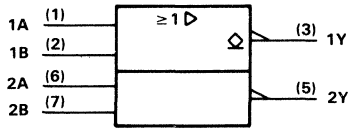
PARAMETER		TEST CONDITIONS†	SN55463			SN75463			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{OH} = 35 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		8	11		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		58	76		58	76	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output				25	40	ns
t_{TLH}	Transition time, low-to-high-level output				8	25	ns
t_{THL}	Transition time, high-to-low-level output				10	25	ns
V_{OH}	High-level output voltage after switching	SN55463	V_S = 30 V, $I_O \approx$ 300 mA, See Figure 2		V_S−10		mV
		SN75463		V_S−10			

logic symbol†



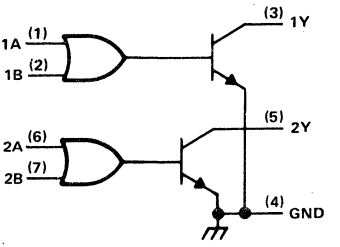
† This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JG package.

FUNCTION TABLE (EACH DRIVER)

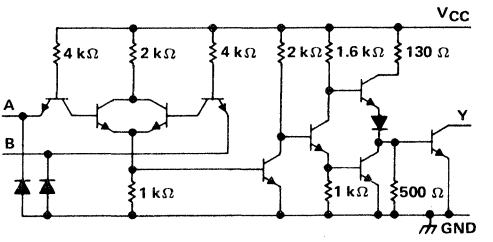
A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

positive logic:
$Y = \overline{A+B}$ or $\overline{A}\,\overline{B}$

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

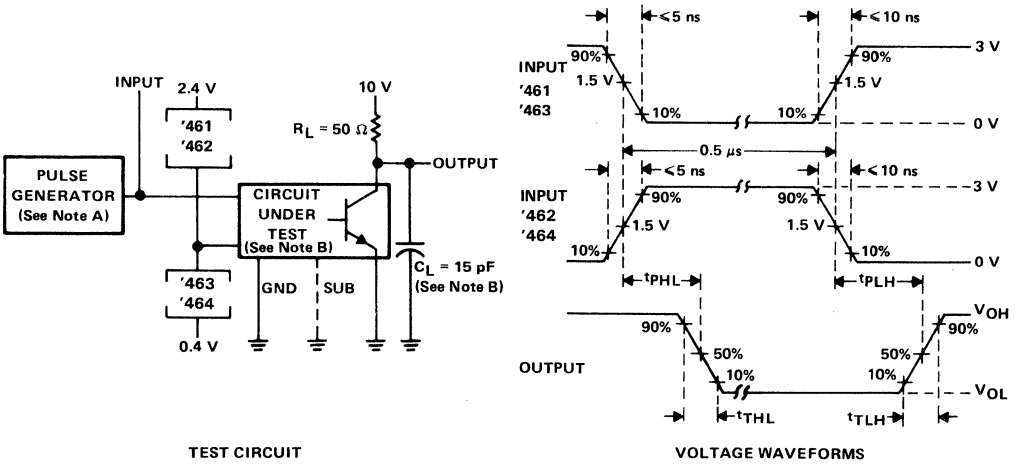
PARAMETER		TEST CONDITIONS†	SN55464 MIN	SN55464 TYP‡	SN55464 MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 35 V			300	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = 100 mA		0.25	0.5	V
		V_{CC} = MIN, V_{IH} = MIN, I_{OL} = 300 mA		0.5	0.8	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 0		14	19	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 5 V		67	85	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		40	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output				30	50	ns
t_{TLH}	Transition time, low-to-high-level output				8	20	ns
t_{THL}	Transition time, high-to-low-level output				10	20	ns
V_{OH}	High-level output voltage after switching	SN55464	V_S = 30 V, $I_O \approx$ 300 mA, See Figure 2		V_S−10		mV
		SN75464		V_S−10			

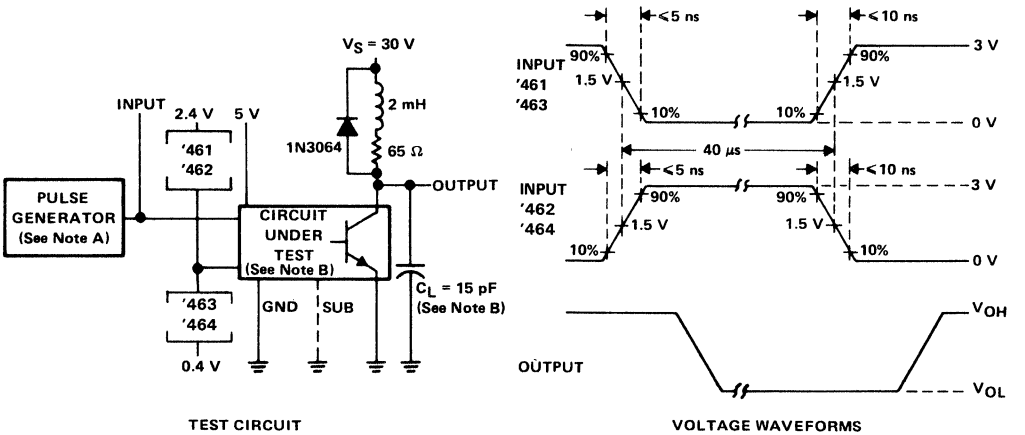
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHZ, Z_{out} ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

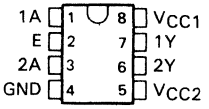
NOTES: A. The pulse generator has the following characteristics: PRR ≤ 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 2. LATCH-UP TEST

D3004, JULY 1986

- **Dual Circuits Capable of Driving High-Capacitance Loads at High Speeds**
- **Output Supply Voltage Range Up to 24 V**
- **Low Standby Power Dissipation**

D OR P PACKAGE
(TOP VIEW)

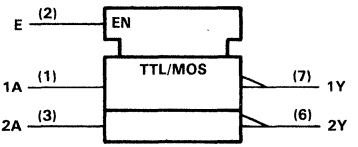


description

The SN75372 is a dual NAND gate interface circuit designed to drive power MOSFETs from TTL inputs. It provides high current and voltage levels necessary to drive large capacitive loads at high speeds. The device operates from a V_{CC1} of 5 V and a V_{CC2} of up to 24 V.

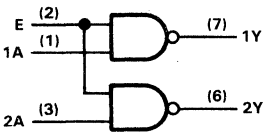
The SN75372 is characterized for operation from 0°C to 70°C.

logic symbol†

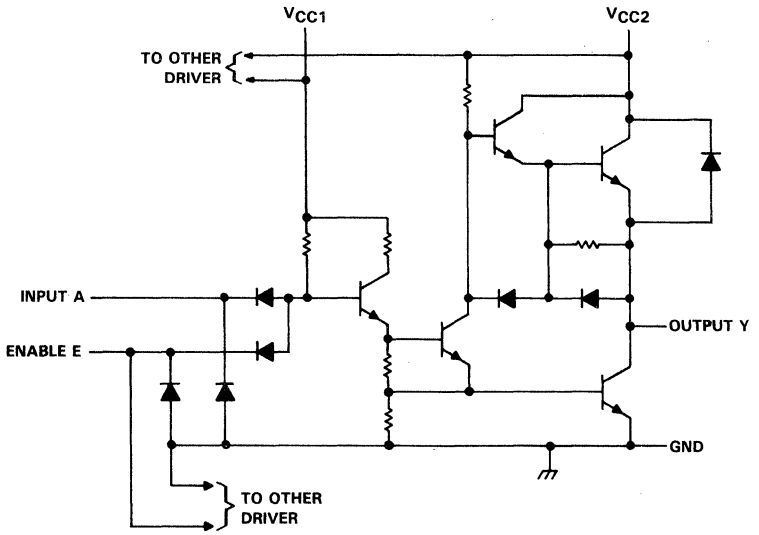


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1) . . . . . −0.5 V to 7 V
Supply voltage range of V_{CC2} . . . . . −0.5 V to 25 V
Input voltage . . . . . 5.5 V
Peak output current (t_w < 10 ms, duty cycle < 50%): Sink . . . . . 500 mA
Source . . . . . 500 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	20	24	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−10	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating free-air temperature (unless otherwise noted)

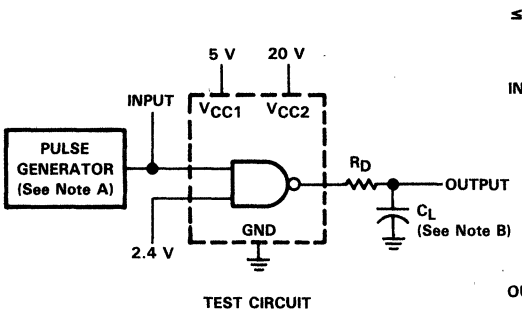
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{IL} = 0.8 V,	I_{OH} = −50 μA	V_{CC2}−1.3	V_{CC2}−0.8		V
			V_{IL} = 0.8 V,	I_{OH} = −10 mA	V_{CC2}−2.5	V_{CC2}−1.8		
V_{OL}	Low-level output voltage		V_{IH} = 2 V,	I_{OL} = 10 mA		0.15	0.3	V
			V_{CC2} = 15 V to 24 V, I_{OL} = 40 mA	V_{IH} = 2 V,		0.25	0.5	
V_F	Output clamp diode forward voltage		V_I = 0,	I_F = 20 mA			1.5	V
I_I	Input current at maximum input voltage		V_I = 5.5 V				1	mA
I_{IH}	High-level input current	Any A	V_I = 2.4 V				40	μA
		Any E					80	
I_{IL}	Low-level input current	Any A	V_I = 0.4 V			−1	−1.6	mA
		Any E				−2	−3.2	
$I_{CC1(H)}$	Supply current from V_{CC1}, both outputs high		V_{CC1} = 5.25 V, All inputs at 0 V,	V_{CC2} = 24 V, No load		2	4	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, both outputs high						0.5	mA
$I_{CC1(L)}$	Supply current from V_{CC1}, both outputs low		V_{CC1} = 5.25 V, All inputs at 5 V,	V_{CC2} = 24 V, No load		16	24	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, both outputs low					7	13	mA
$I_{CC2(S)}$	Supply current from V_{CC2}, standby condition		V_{CC1} = 0, All inputs at 5 V,	V_{CC2} = 24 V, No load			0.5	mA

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 20 V, and T_A = 25°C.

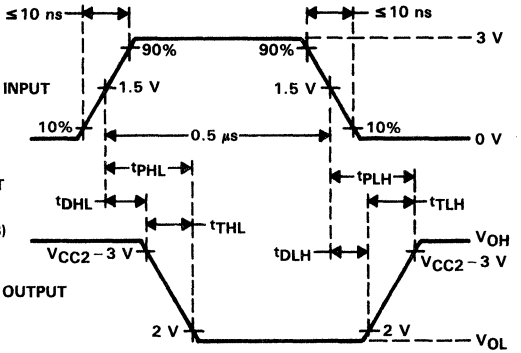
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 20 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 390 pF, R_D = 10 Ω, See Figure 1		20	35	ns
t_{DHL}	Delay time, high-to-low-level output			10	20	ns
t_{TLH}	Transition time, low-to-high-level output			20	30	ns
t_{THL}	Transition time, high-to-low-level output			20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output		10	40	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	30	50	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

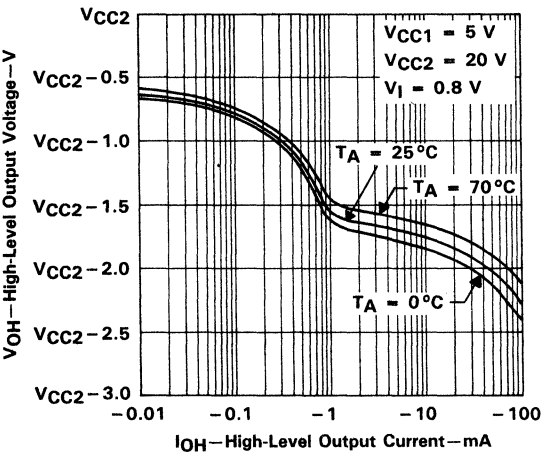


FIGURE 2

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

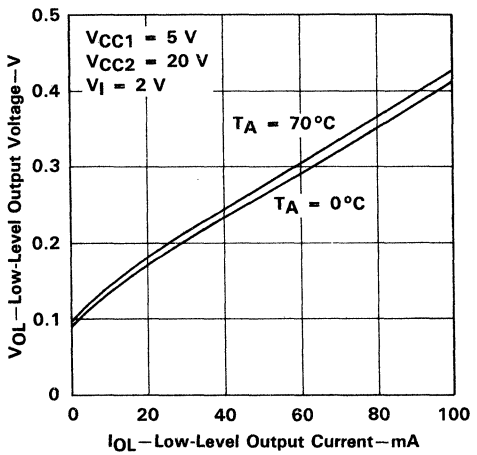


FIGURE 3

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

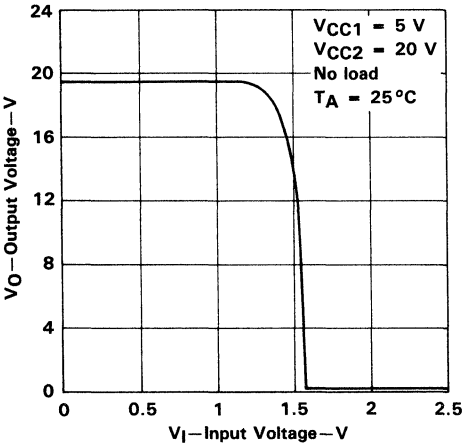


FIGURE 4

POWER DISSIPATION (BOTH DRIVERS)
vs
FREQUENCY

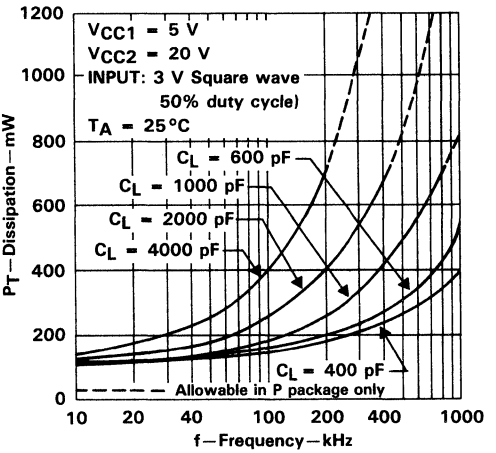


FIGURE 5

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

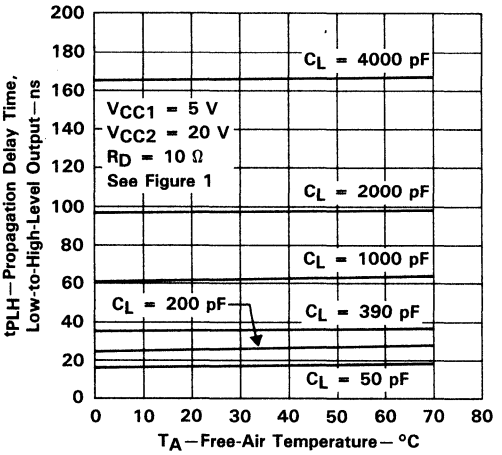


FIGURE 6

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

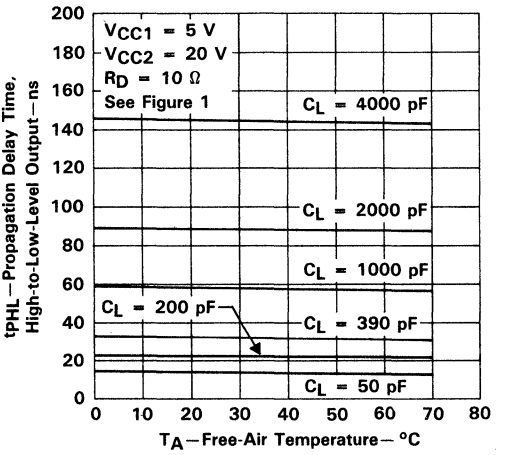


FIGURE 7

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

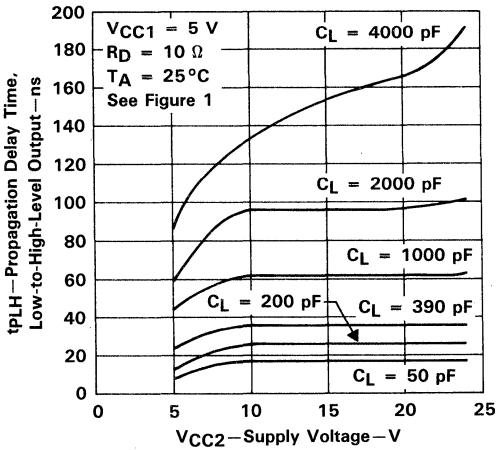


FIGURE 8

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

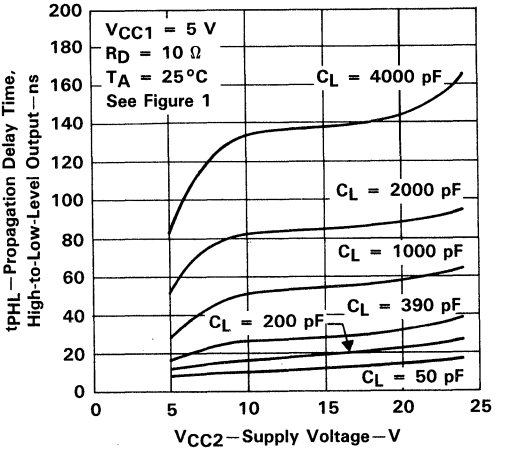


FIGURE 9

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
LOAD CAPACITANCE

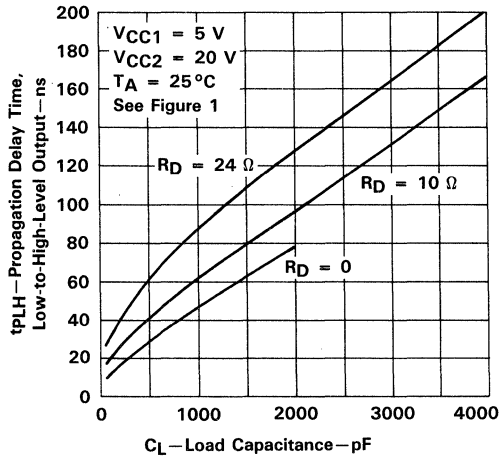


FIGURE 10

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
LOAD CAPACITANCE

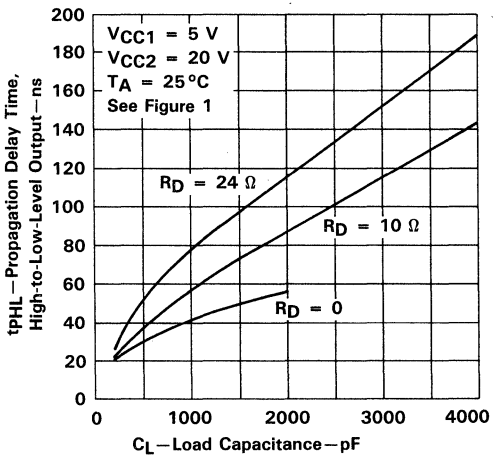


FIGURE 11

NOTE: For R_D = 0, operation with C_L > 2000 pF violates absolute maximum current rating.

APPLICATIONS INFORMATION

driving power MOSFETs

The drive requirements of power MOSFETs are much lower than comparable bipolar power transistors. The input impedance of a FET consists of a reverse biased PN junction that can be described as a large capacitance in parallel with a very high resistance. For this reason, the commonly used open-collector driver with a pull-up resistor is not satisfactory for high-speed applications. In Figure 12(a), an IRF151 power MOSFET switching an inductive load is driven by an open-collector transistor driver with a 470-Ω pull-up resistor. The input capacitance (C_{iss}) specification for an IRF151 is 4000 pF maximum. The resulting long turn-on time due to the combination of C_{iss} and the pull-up resistor is shown in Figure 12(b).

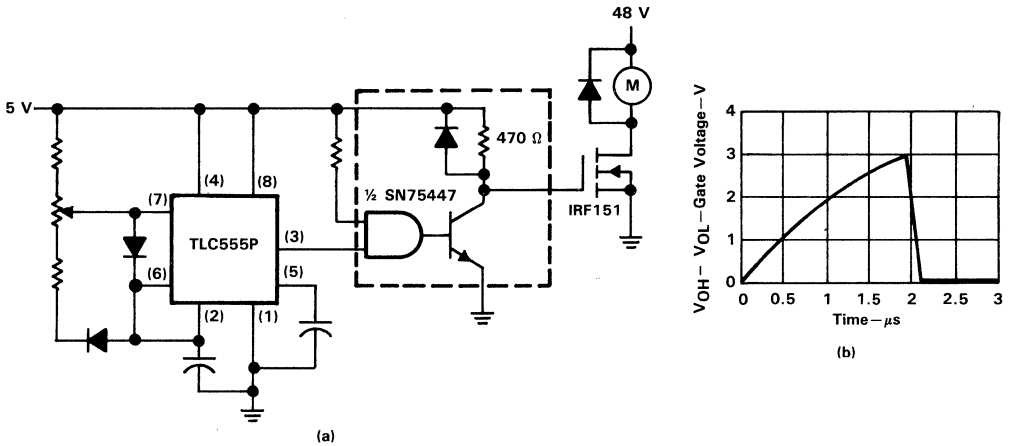


FIGURE 12. POWER MOSFET DRIVE USING SN75447

APPLICATIONS INFORMATION

A faster, more efficient drive circuit uses an active pull-up as well as an active pull-down output configuration, referred to as a totem-pole output. The SN75372 driver provides the high speed, totem-pole drive desired in an application of this type, see Figure 13(a). The resulting faster switching speeds are shown in Figure 13(b).

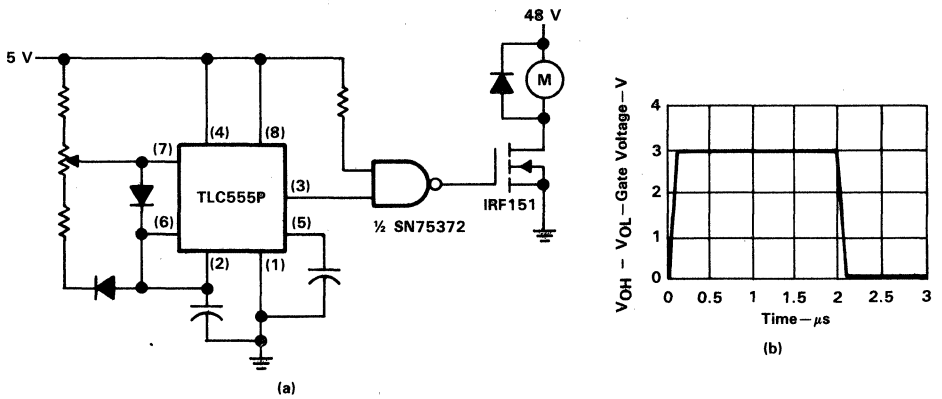


FIGURE 13. POWER MOSFET DRIVE USING SN75372

Power MOSFET drivers must be capable of supplying high peak currents to achieve fast switching speeds as shown by the equation

$$I_{pk} = \frac{VC}{t_r}$$

where C is the capacitive load, and t_r is the desired rise time. V is the voltage that the capacitance is charged to. In the circuit shown in Figure 13(a), V is found by the equation

$$V = V_{OH} - V_{OL}$$

Peak current required to maintain a rise time of 100 ns in the circuit of Figure 13(a) is

$$I_{PK} = \frac{(3\text{-}0)4(10-9)}{100(10-9)} = 120 \text{ mA}$$

Circuit capacitance can be ignored because it is very small compared to the input capacitance of the IRF151. With a V_{CC} of 5 V, and assuming worst-cast conditions, the gate drive voltage is 3 V.

For applications in which the full voltage of V_{CC2} must be supplied to the MOSFET gate, the SN75374 QUAD MOSFET driver should be used.

THERMAL INFORMATION

power dissipation precautions

Significant power may be dissipated in the SN75372 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. Figure 5 shows the power dissipated in a typical SN75372 as a function of load capacitance and frequency. Average power dissipated by this driver is derived from the equation

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are

$$P_{DC(AV)} = \frac{P_H t_H + P_L t_L}{T}$$

$$P_{C(AV)} \approx C V_C^2 f$$

$$P_{S(AV)} = \frac{p_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

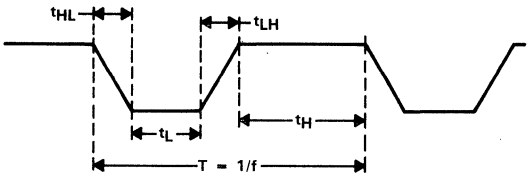


FIGURE 14. OUTPUT VOLTAGE WAVEFORM

where the times are as defined in Figure 14.

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation, C is the load capacitance. V_C is the voltage across the load capacitance during the charge cycle shown by the equation

$$V_C = V_{OH} - V_{OL}$$

$P_{S(AV)}$ may be ignored for power calculations at low frequencies.

THERMAL INFORMATION

In the following power calculation, both channels are operating under identical conditions: V_{OH} = 19.2 V and V_{OL} = 0.15 V with V_{CC1} = 5 V, V_{CC2} = 20 V, V_C = 19.05 V, C = 1000 pF, and the duty cycle = 60%. At 0.5 MHz, $P_{S(AV)}$ is negligible and can be ignored. When the output voltage is high, I_{CC2} is negligible and can be ignored.

On a per-channel basis using data sheet values

$$P_{DC(AV)} = \left[(5\text{ V})\left(\frac{2\text{ mA}}{2}\right) + (20\text{ V})\left(\frac{0\text{ mA}}{2}\right)\right](0.6) + \left[(5\text{ V})\left(\frac{16\text{ mA}}{2}\right) + (20\text{ V})\left(\frac{7\text{ mA}}{2}\right)\right](0.4)$$

$P_{DC(AV}$ = 47 mW per channel

Power during the charging time of the load capacitance is

$P_{C(AV)}$ = (1000 pF) (19.05 V)^2 (0.5 MHz) = 182 mW per channel

Total power for each driver is

$P_{T(AV)}$ = 47 mW + 182 mW = 229 mW

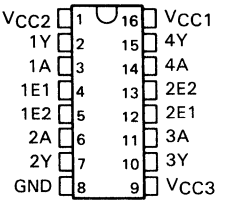
and total package power is

$P_{T(AV)}$ = (229) (2) = 458 mW.

D3004, SEPTEMBER 1986

- **Quadruple Circuits Capable of Driving High-Capacitance Loads at High Speeds**
- **Output Supply Voltage Range from 5 V to 24 V**
- **Low Standby Power Dissipation**
- **V_{CC3} Supply Maximizes Output Source Voltage**

D OR N PACKAGE
(TOP VIEW)



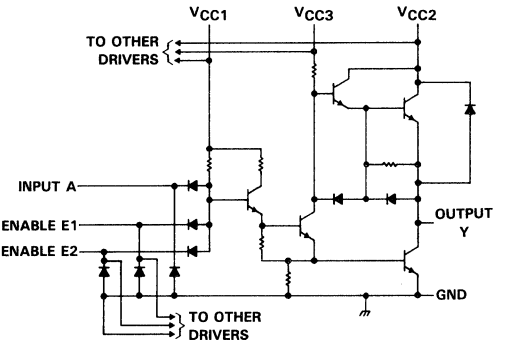
description

The SN75374 is a quadruple NAND interface circuit designed to drive power MOSFETs from TTL inputs. It provides the high current and voltage necessary to drive large capacitive loads at high speeds.

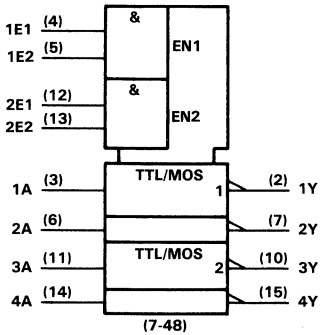
The outputs can be switched very close to the V_{CC2} supply rail when V_{CC3} is about 3 V higher than V_{CC2}. The V_{CC3} pin can also be tied directly to V_{CC2} when the source voltage requirements are lower.

The SN75374 is characterized for operation from 0°C to 70°C.

schematic (each driver)

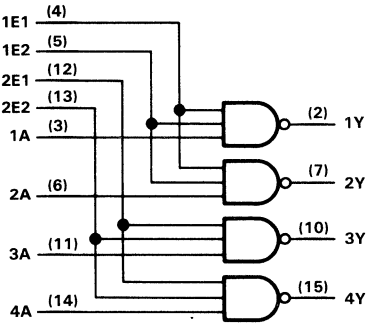


logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1}, (see Note 1) . . . . . −0.5 V to 7 V
Supply voltage range of V_{CC2} . . . . . −0.5 V to 25 V
Supply voltage range of V_{CC3} . . . . . −0.5 V to 30 V
Input voltage . . . . . 5.5 V
Peak output current (t_w < 10 ms, duty cycle < 50%): Sink . . . . . 500 mA
Source . . . . . 500 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	20	24	V
Supply voltage, V_{CC3}	V_{CC2}	24	28	V
Voltage difference between supply voltages: $V_{CC3} - V_{CC2}$	0	4	10	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−10	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, V_{CC3}, and operating free-air temperature (unless otherwise noted)

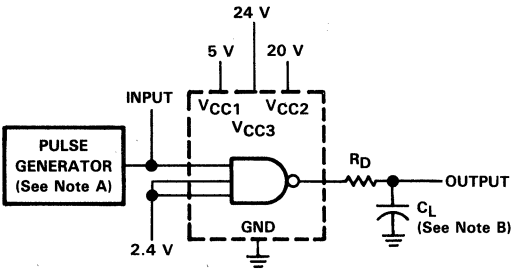
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC3} = V_{CC2}+3 V,	V_{IL} = 0.8 V, I_{OH} = −100 μA	V_{CC2}−0.3	V_{CC2}−0.1		V
			V_{CC3} = V_{CC2}+3 V,	V_{IL} = 0.8 V, I_{OH} = −10 mA	V_{CC2}−1.3	V_{CC2}−0.9		
			V_{CC3} = V_{CC2},	V_{IL} = 0.8 V, I_{OH} = −50 μA	V_{CC2}−1	V_{CC2}−0.7		
			V_{CC3} = V_{CC2},	V_{IL} = 0.8 V, I_{OH} = −10 mA	V_{CC2}−2.5	V_{CC2}−1.8		
V_{OL}	Low-level output voltage		V_{IH} = 2 V,	I_{OL} = 10 mA		0.15	0.3	V
			V_{CC2} = 15 V to 28 V,	V_{IH} = 2 V, I_{OL} = 40 mA		0.25	0.5	
V_F	Output clamp diode forward voltage		V_I = 0,	I_F = 20 mA			1.5	V
I_I	Input current at maximum input voltage		V_I = 5.5 V				1	mA
I_{IH}	High-level input current	Any A	V_I = 2.4 V				40	μA
		Any E					80	
I_{IL}	Low-level input current	Any A	V_I = 0.4 V			−1	−1.6	mA
		Any E				−2	−3.2	
$I_{CC1(H)}$	Supply current from V_{CC1}, all outputs high		V_{CC1} = 5.25 V, No load	V_{CC2} = 24 V, V_{CC3} = 28 V, All inputs at 0 V,		4	8	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high					−2.2	0.25	
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high					2.2	3.5	
$I_{CC1(L)}$	Supply current from V_{CC1}, all outputs low		V_{CC1} = 5.25 V, No load	V_{CC2} = 24 V, V_{CC3} = 28 V, All inputs at 5 V,		31	47	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, all outputs low						2	
$I_{CC3(L)}$	Supply current from V_{CC3}, all outputs low					16	27	
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high		V_{CC1} = 5.25 V, No load	V_{CC2} = 24 V, V_{CC3} = 24 V, All inputs at 0 V,			0.25	mA
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high						0.5	
$I_{CC2(S)}$	Supply current from V_{CC2}, standby condition		V_{CC1} = 0, No load	V_{CC2} = 24 V, V_{CC3} = 24 V, All inputs at 0 V,			0.25	mA
$I_{CC3(S)}$	Supply current from V_{CC3}, standby condition						0.5	

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, and T_A = 25°C except for V_{OH} for which V_{CC2} and V_{CC3} are as stated under test conditions.

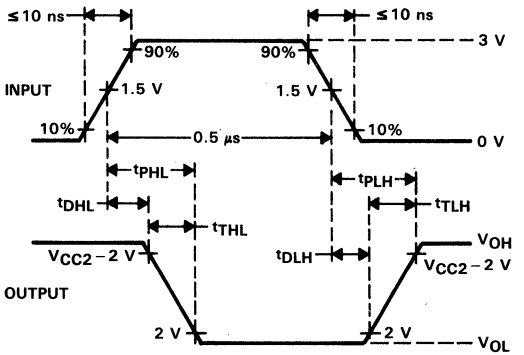
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 200 pF, R_D = 24 Ω, See Figure 1		20	30	ns
t_{DHL}	Delay time, high-to-low-level output			10	20	ns
t_{TLH}	Transition time, low-to-high-level output			20	30	ns
t_{THL}	Transition time, high-to-low-level output			20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output		10	40	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	30	50	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

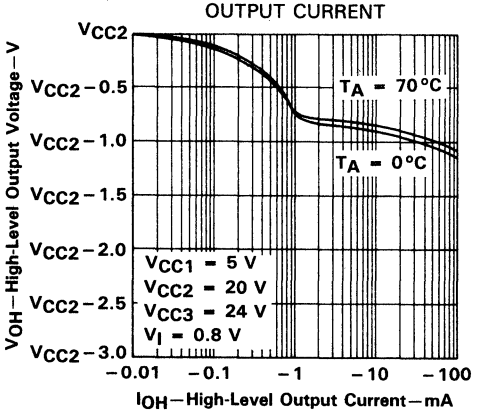


FIGURE 2

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

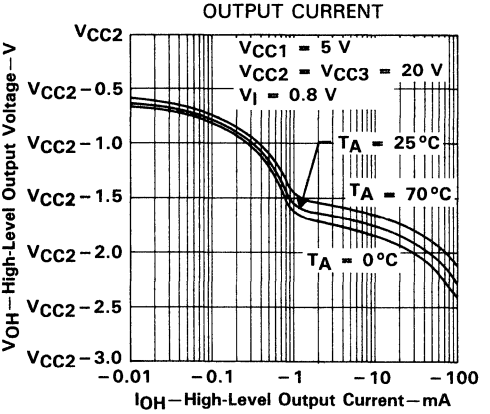


FIGURE 3

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

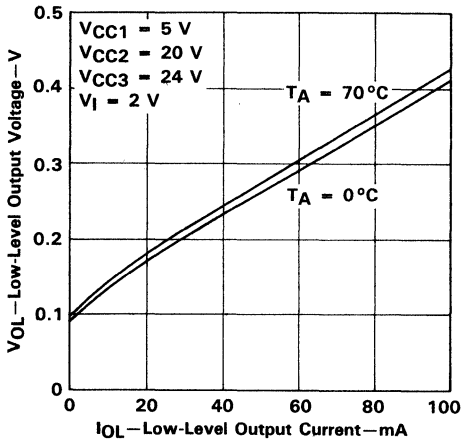


FIGURE 4

VOLTAGE TRANSFER CHARACTERISTICS

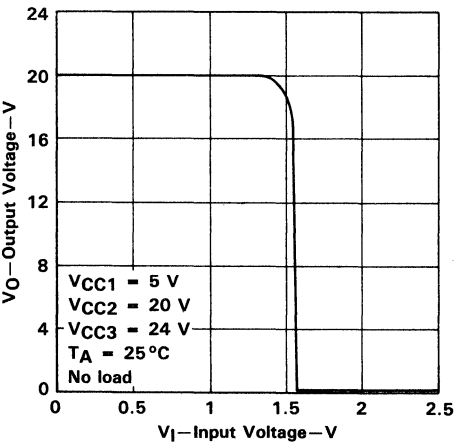


FIGURE 5

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

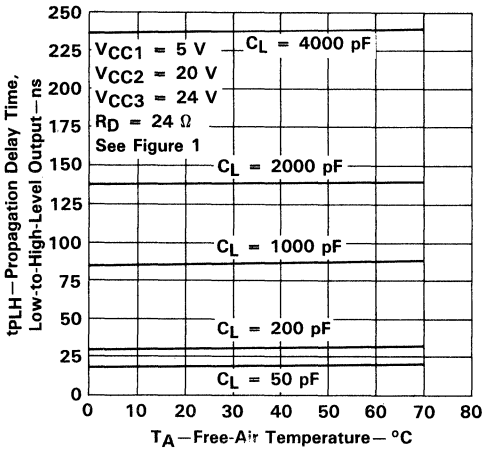


FIGURE 6

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
T_A-FREE-AIR TEMPERATURE

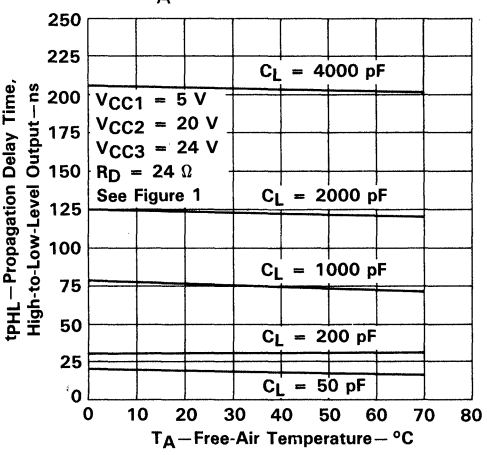


FIGURE 7

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

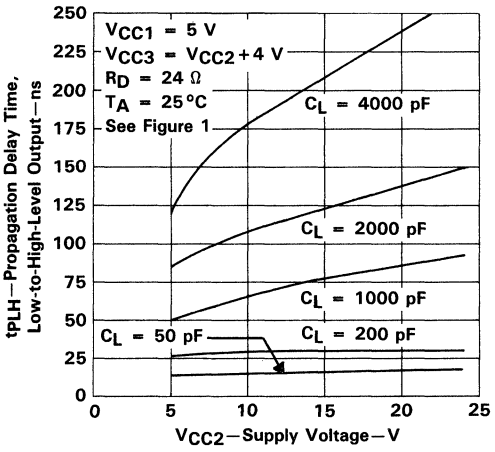


FIGURE 8

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

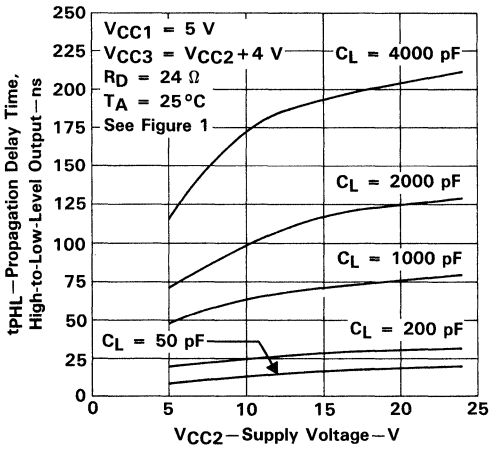


FIGURE 9

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
LOAD CAPACITANCE

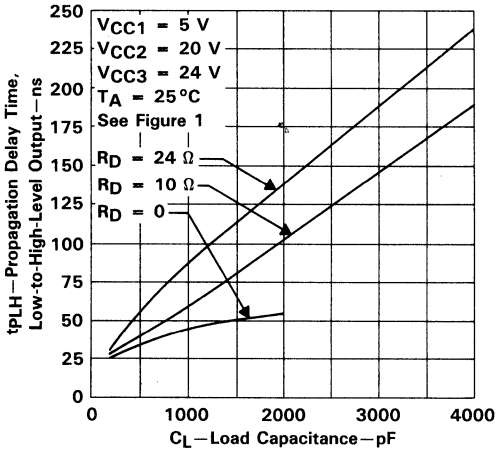


FIGURE 10

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
LOAD CAPACITANCE

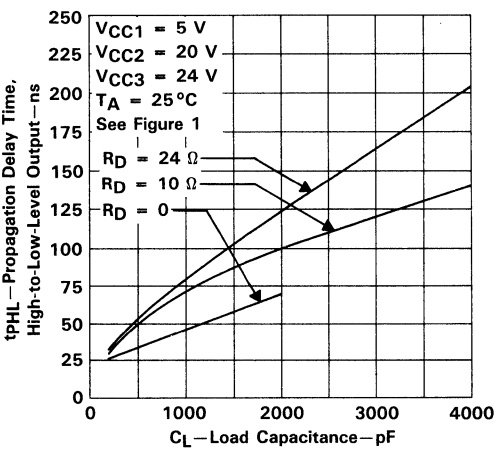


FIGURE 11

POWER DISSIPATION (ALL DRIVERS)
vs
FREQUENCY

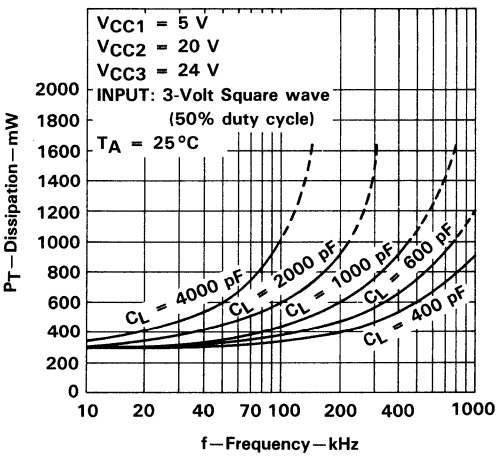


FIGURE 12

NOTE: For R_D = 0, operation with C_L > 2000 pF violates absolute maximum current rating.

APPLICATIONS INFORMATION

driving power MOSFETs

The drive requirements of power MOSFETs are much lower than comparable bipolar power transistors. The input impedance of a FET consists of a reverse biased PN junction that can be described as a large capacitance in parallel with a very high resistance. For this reason, the commonly used open-collector driver with a pull-up resistor is not satisfactory for high-speed applications. In Figure 13(a), an IRF151 power MOSFET switching an inductive load is driven by an open-collector transistor driver with a 470-Ω pull-up resistor. The input capacitance (C_{iss}) specification for an IRF151 is 4000 pF maximum. The resulting long turn-on time due to the product of input capacitance and the pull-up resistor is shown in Figure 13(b).

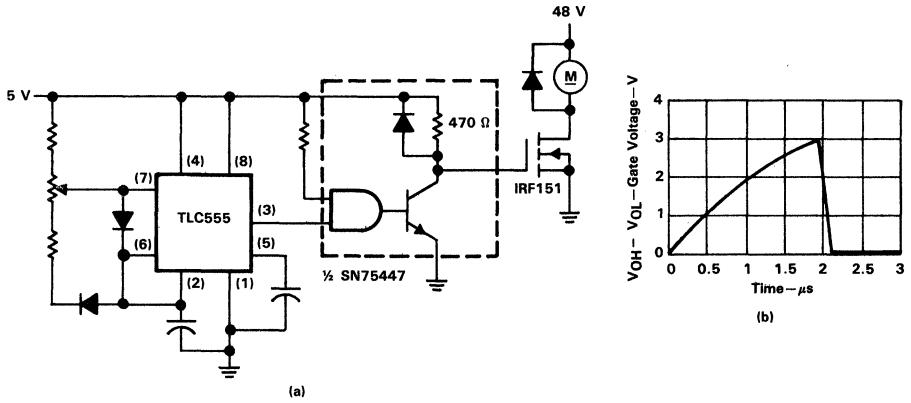


FIGURE 13. POWER MOSFET DRIVE USING SN75447

A faster, more efficient drive circuit uses an active pull-up as well as an active pull-down output configuration, referred to as a totem-pole output. The SN75374 driver provides the high-speed totem-pole drive desired in an application of this type, see Figure 14(a). The resulting faster switching speeds are shown in Figure 14(b).

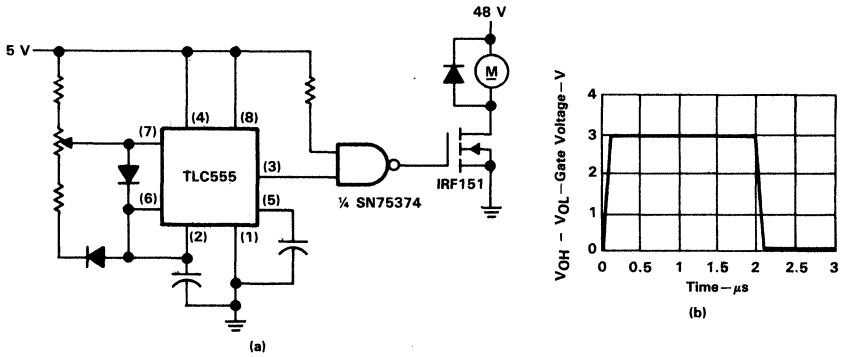


FIGURE 14. POWER MOSFET DRIVE USING SN75374

APPLICATIONS INFORMATION

Power MOSFET drivers must be capable of supplying high peak currents to achieve fast switching speeds as shown by the equation

$$I_{pk} = \frac{VC}{t_r}$$

where C is the capacitive load, and t_r is the desired rise time. V is the voltage that the capacitance is charged to. In the circuit shown in Figure 14(a), V is found by the equation

$$V = V_{OH} - V_{OL}$$

Peak current required to maintain a rise time of 100 ns in the circuit of Figure 14(a) is

$$I_{PK} = \frac{(3\text{-}0)4(10-9)}{100(10-9)} = 120 \text{ mA}$$

Circuit capacitance can be ignored because it is very small compared to the input capacitance of the IRF151. With a V_{CC} of 5 V, and assuming worst-case conditions, the gate drive voltage is 3 V.

For applications in which the full voltage of V_{CC2} must be supplied to the MOSFET gate, V_{CC3} should be at least 3 V higher than V_{CC2}.

THERMAL INFORMATION

power dissipation precautions

Significant power may be dissipated in the SN75374 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. Figure 12 shows the power dissipated in a typical SN75374 as a function of frequency and load capacitance. Average power dissipated by this driver is derived from the equation

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are

$$P_{DC(AV)} = \frac{P_H t_H + P_L t_L}{T}$$

$$P_{C(AV)} \approx C\, V^2_C\, f$$

$$P_{S(AV)} = \frac{p_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

where the times are as defined in Figure 15.

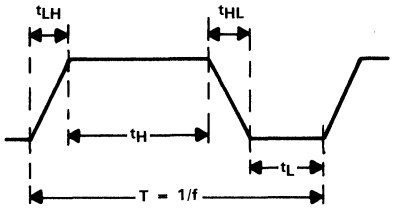


FIGURE 15. OUTPUT VOLTAGE WAVEFORM

THERMAL INFORMATION

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation, C is the load capacitance. V_C is the voltage across the load capacitance during the charge cycle shown by the equation

$$V_C = V_{OH} - V_{OL}$$

$P_{S(AV)}$ may be ignored for power calculations at low frequencies.

In the following power calculation, all four channels are operating under identical conditions: f = 0.2 MHz, V_{OH} = 19.9 V and V_{OL} = 0.15 V with V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, V_C = 19.75 V, C = 1000 pF, and the duty cycle = 60%. At 0.2 MHz for C_L < 2000 pF, $P_{S(AV)}$ is negligible and can be ignored. When the output voltage is low, I_{CC2} is negligible and can be ignored.

On a per-channel basis using data sheet values

$$P_{DC(AV)} = \left[(5\text{ V})\left(\frac{4\text{ mA}}{4}\right) + (20\text{ V})\left(\frac{-2.2\text{ mA}}{4}\right) + (24\text{ V})\left(\frac{2.2\text{ mA}}{4}\right)\right](0.6) + \left[(5\text{ V})\left(\frac{31\text{ mA}}{4}\right) + (20\text{ V})\left(\frac{0\text{ mA}}{4}\right) + (24\text{ V})\left(\frac{16\text{ mA}}{4}\right)\right](0.4)$$

$P_{DC(AV}$ = 58.2 mW per channel

Power during the charging time of the load capacitance is

$P_{C(AV)}$ = (1000 pF) (19.75 V)^2 (0.2 MHz) = 78 mW per channel

Total power for each driver is

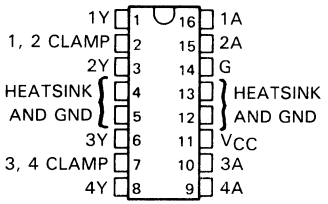
$P_{T(AV)}$ = 58.2 mW + 78 mW = 136.2 mW

The total package power is

$P_{T(AV)}$ = (136.2) (4) = 544.8 mW

- **Saturating Outputs With Low On Resistance**
- **Very Low Standby Power . . . 53 mW Max**
- **High-Impedance MOS- or TTL-Compatible Inputs**
- **Standard 5-V Supply Voltage**
- **No Output Glitch During Power-Up or Power-Down**
- **Output Clamp Diodes for Transient Suppression**
- **2-W Power Package . . . 60°C/W $R_{\theta JA}$**
- **600-mA Output Current**
- **35-V Switching Voltage**

NE DUAL-IN-LINE PACKAGE
(TOP VIEW)



FUNCTION TABLE
(EACH NAND DRIVER)

INPUTS		OUTPUT
A	G	Y
L	X	H
X	L	H
H	H	L

H = high level, L = low level
X = irrelevant

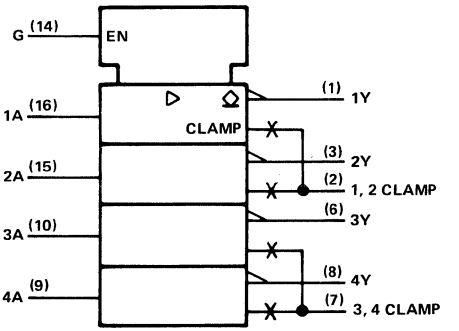
description

The SN75435 quadruple peripheral driver is designed for use in systems requiring high current, high voltage, and high load power. It features four inverting open-collector drivers with a common enable input that, when taken low, disables all four outputs. Each driver is protected against load shorts with its own latching over-current shutdown circuitry, which will turn the output off when a load short is detected. A short on one load will not affect operation of the other three drivers. The latch for the shutdown will hold the output off until the input or enable pin is taken low and then high again. A delay circuit is incorporated in the over-current shutdown to allow load capacitance of up to 5 nF at 35 V.

Applications include relay drivers, lamp drivers, solenoid drivers, motor drivers, LED drivers, line drivers, logic buffers, hammer drivers, and memory drivers.

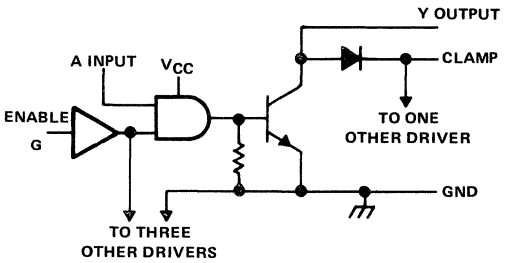
The SN75435 is characterized for operation from 0°C to 70°C.

logic symbol†

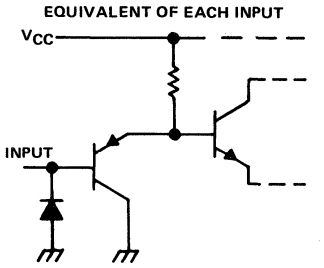


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of inputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Output supply voltage . . . . . 70 V
Output diode clamp current . . . . . 1 A
Continuous total power dissipation
at (or below) 25°C free-air temperature (see Note 2) . . . . . 2075 mW
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Output voltage			35	V
Output current			600	mA
Load capacitance (See Figure 3)			35	nF
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range

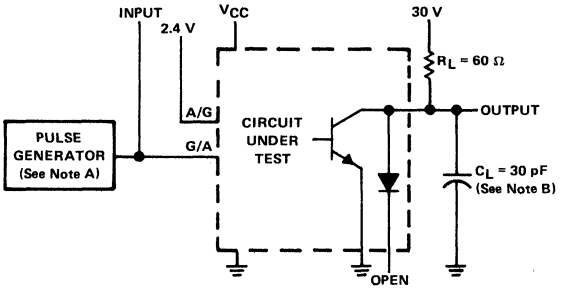
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = −12 mA		−0.9	−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 70 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V	I_{OL} = 300 mA		0.25	0.5	V
			I_{OL} = 600 mA		0.55	1	
V_R	Output clamp diode reverse voltage	V_{CC} = 4.75 V,	I_R = 100 μA	70	100		V
V_F	Output clamp diode forward voltage	I_F = 600 mA			1.2	1.6	V
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 5.25 V		0.01	10	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.8 V		−0.5	−10	μA
	Over-current shutdown current	V_{CC} = 4.75 V to 5.25 V		650	850		mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	V_I = 0		6	10	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	V_I = 5 V		55	75	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

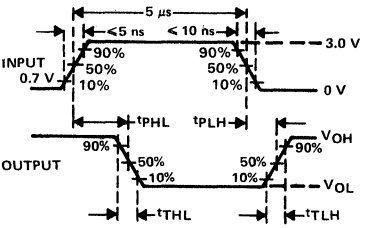
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propogation delay time, low-to-high-level output	C_L = 30 pF, R_L = 60 Ω, See Figure 1		750		ns
t_{PHL}	Propagation delay time, high-to-low-level output			750		ns
t_{TLH}	Transition time, low-to-high-level output			200		ns
t_{THL}	Transition time, high-to-low-level output			200		ns
V_{OH}	High-level output voltage after switching	See Figure 2	V_S – 10			mV

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

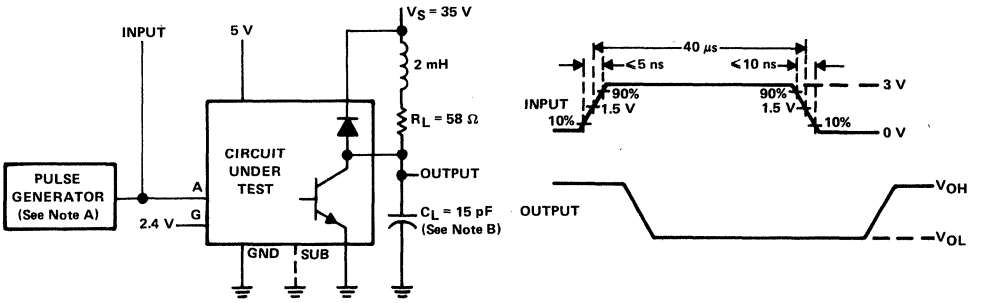


VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. C_L include probe and jig capacitance.

FIGURE 2. LATCH-UP TEST

RECOMMENDED OPERATING CONDITIONS

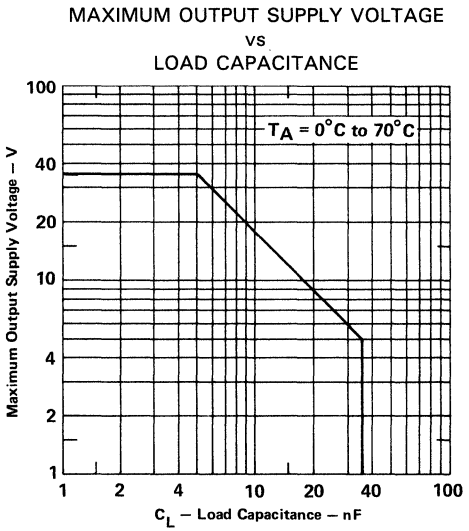
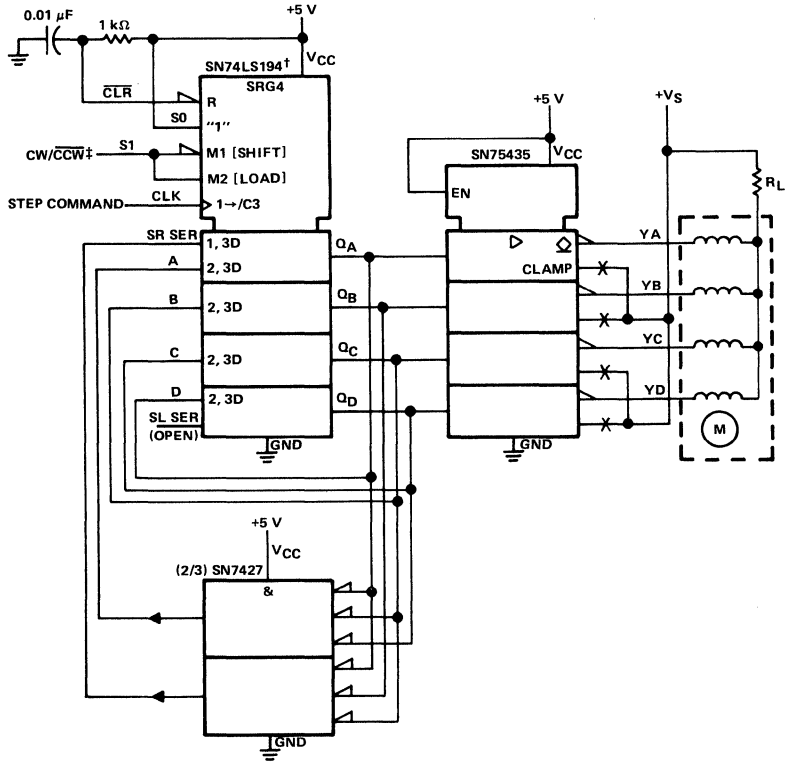
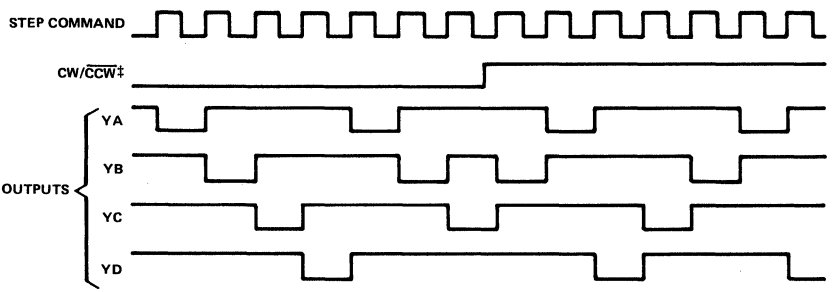


FIGURE 3

APPLICATION INFORMATION



4-WINDING STEPPER MOTOR CONTROL CIRCUIT



TIMING DIAGRAM FOR MOTOR CONTROL CIRCUIT

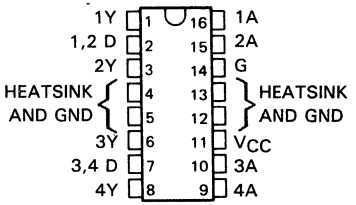
†The SN74LS194 is a universal shift register with both shift-right and shift-left capability. In this application S0 (pin 9) is wired high and only the shift-right and parallel-load modes are utilized. The logic symbol shown above has been simplified to show only the utilized modes.

‡This signal is CW/$\overline{\text{CCW}}$ or $\overline{\text{CW}}$/CCW depending on motor winding.

D2806, DECEMBER 1986

- **Saturating Outputs With Low On-State Resistance**
- **High-Impedance Inputs Compatible With CMOS, MOS, and TTL Levels**
- **Very Low Standby Power . . . 21 mW Maximum**
- **High-Voltage Outputs . . . 70 V Min**
- **No Output Glitch During Power Up or Power Down**
- **No Latch-Up Within Recommended Operating Conditions**
- **Output Clamp Diodes for Transient Suppression**
- **2-W Power Package**

NE PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each NAND driver)

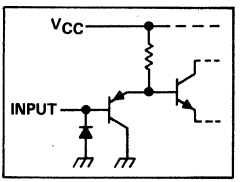
INPUTS A	INPUTS G	OUTPUT Y
H	H	L
L	X	H
X	L	H

H = high level,
L = low level,
X = irrelevant

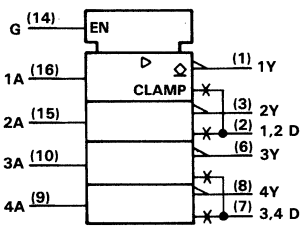
description

The SN75436, SN75437A, and SN75438 quadruple peripheral drivers are designed for use in systems requiring high current, high voltage, and high load power. Each device features four inverting open-collector outputs with a common enable input that, when taken low, disables all four outputs. The envelope of I-V characteristics exceeds the specifications sufficiently to avoid high-current latch-up. Applications include driving relays, lamps, solenoids, motors, LEDs, transmission lines, hammers, and other high-power-demand devices.

equivalent schematic of each input

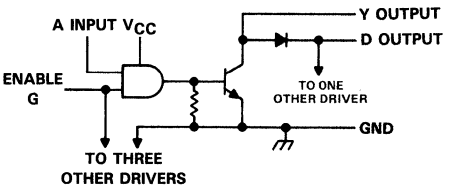


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic, each driver)



SELECTION GUIDE

FEATURE	SN75436	SN75437A	SN75438	UNIT
Maximum recommended output current	0.5	0.5	1	A
Maximum V_{OL} at maximum I_{OL}	0.5	0.5	1	V
Maximum recommended output supply voltage in an inductive switching circuit, V_S	50	35	35	V

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 30 V
Output current: SN75436, SN75437A (see Note 1) . . . . . 0.75 A
SN75438 . . . . . 1.25 A
Output clamp diode current . . . . . 1.25 A
Output voltage (off-state) . . . . . 70 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 2075 mW
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16-inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All four sections of these circuits may conduct rated current simultaneously; however, power dissipation average over a short time interval must fall within the continuous dissipation ratings.
2. For operation above 25°C free-air temperature, derate linearly to 1328 mW at 70°C at the rate of 16.6 mW/°C.

recommended operating conditions

PARAMETER	SN75436			SN75437A			SN75438			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
Output current, I_{OL}			0.5			0.5			1	A
Output supply voltage in inductive switching circuit (see Figure 2), V_S			50			35			35	V
High-level input voltage, V_{IH}	2			2			2			V
Low-level input voltage, V_{IL}			0.8			0.8			0.8	V
Operating free-air temperature, T_A	0		70	0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

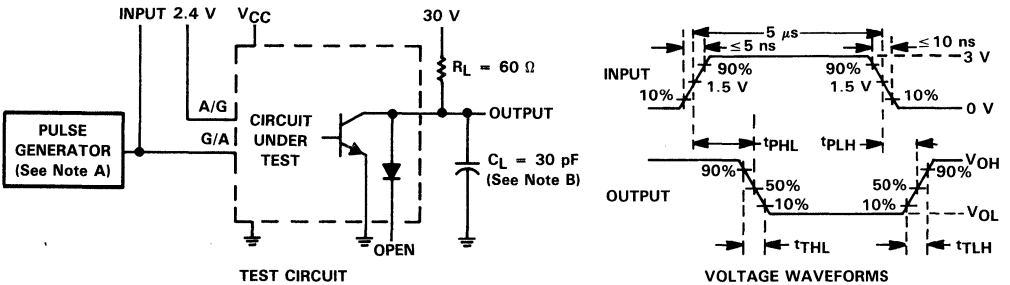
PARAMETER		TEST CONDITIONS		SN75436 SN75437A			SN75438			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	Input clamp	V_{CC} = 4.75 V,	I_I = −12 mA		−0.9	−1.5		−0.9	−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 70 V		1	100		1	100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V	I_{OL} = 250 mA		0.14	0.25		0.14	0.25	V
			I_{OL} = 500 mA		0.28	0.5		0.28	0.5	
			I_{OL} = 750 mA					0.42	0.75	
			I_{OL} = 1 A					0.60	1	
$V_{R(K)}$	Output clamp diode reverse voltage	V_{CC} = 4.75 V,	I_R = 100 μA	70	100		70	100		V
$V_{F(K)}$	Output clamp diode forward voltage	I_F = 500 mA			1	1.6		1	1.6	V
		I_F = 1 A						1.2	2	
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 5.25 V		0.1	10		0.1	10	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.8 V		−0.25	−10		−0.25	−10	μA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	V_I = 0		1	4		1	4	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	V_I = 5 V		45	65		45	65	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

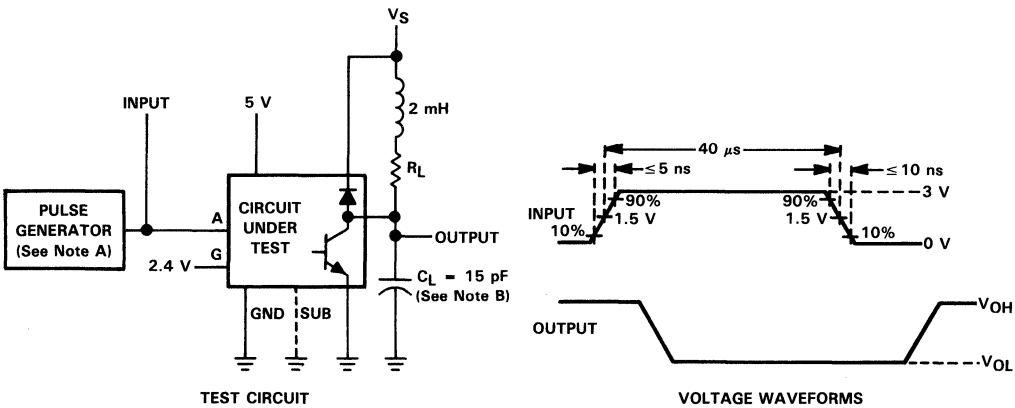
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		C_L = 30 pF, See Figure 1	R_L = 60 Ω,		1950	5000	ns
t_{PHL}	Propagation delay time, high-to-low-level output					150	500	ns
t_{TLH}	Transition time, low-to-high-level output					40		ns
t_{THL}	Transition time, high-to-low-level output					36		ns
V_{OH}	High-level output voltage, after switching	SN75436	V_S = 50 V, R_L = 100 Ω,	I_O ≈ 500 mA, See Figure 2	V_S − 10			mV
		SN75437A	V_S = 35 V, R_L = 70 Ω,	I_O ≈ 500 mA, See Figure 2	V_S − 10			mV
		SN75438	V_S = 35 V, R_L = 35 Ω,	I_O ≈ 1 A, See Figure 2	V_S − 10			mV

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS



NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 2. LATCH-UP TEST

PARAMETER MEASUREMENT INFORMATION

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

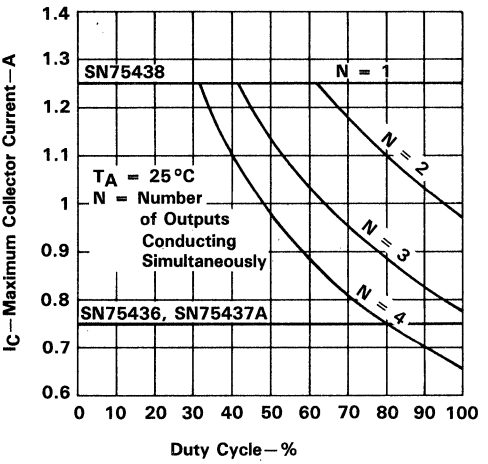


FIGURE 3

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

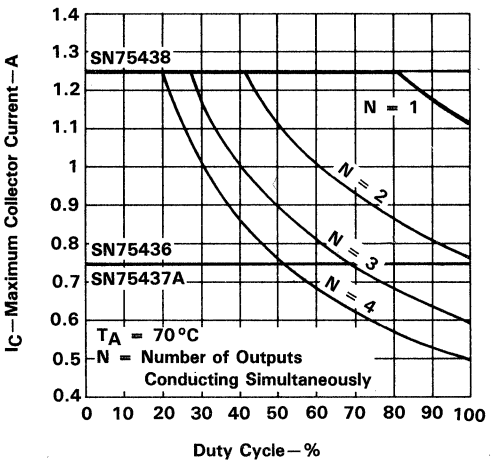


FIGURE 4

APPLICATION INFORMATION

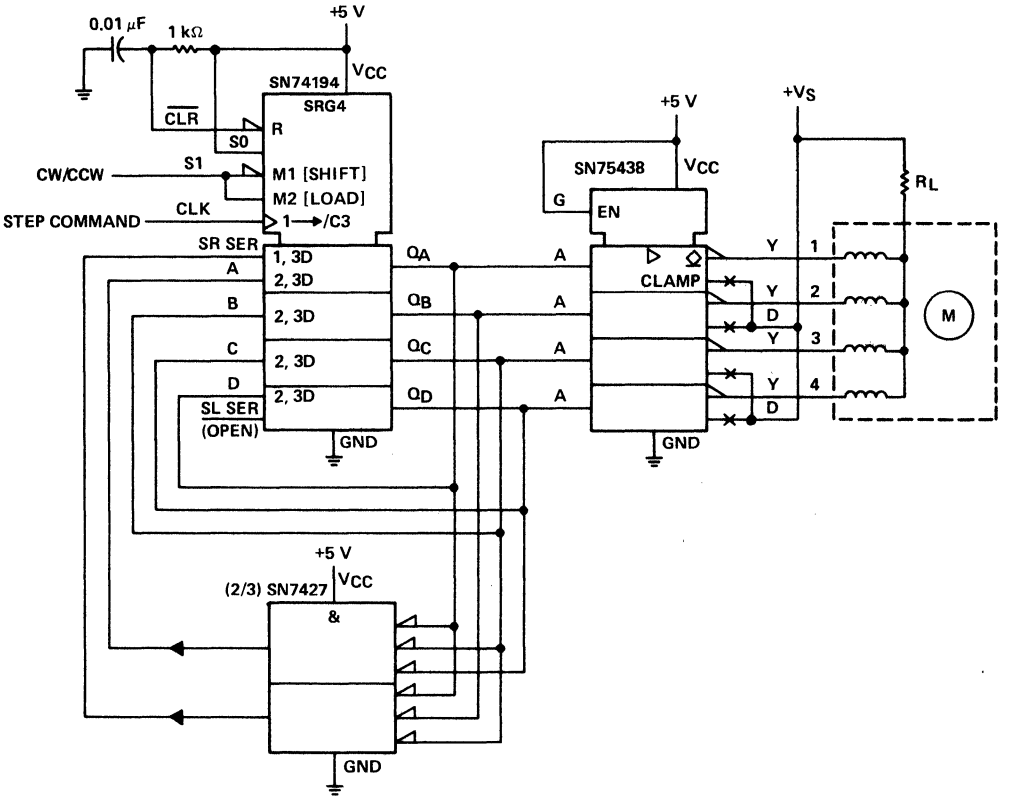


FIGURE 5. 4-WINDING STEPPER MOTOR CONTROL CIRCUIT

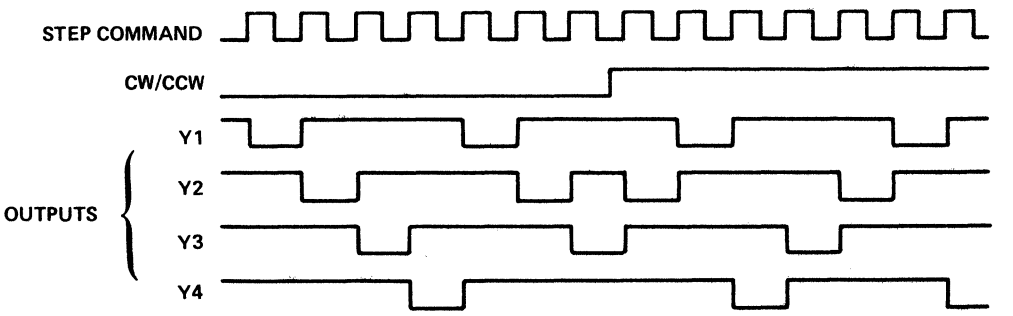
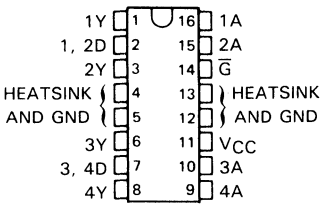


FIGURE 6. TIMING DIAGRAM

D3116, MAY 1988 – REVISED NOVEMBER 1989

- **1.3-A Current Capability Each Channel**
- **Saturating Outputs With Low On-State Resistance**
- **Two Inverting and Two Noninverting Driver Channels With Common Active-Low Enable Input**
- **Key Application Is as a Complete Full-Step 4-Phase DC Stepper Motor Driver Using Only Three Directly Connected Logic Control Signal Lines From Standard Microprocessors**
- **High-Impedance Inputs Compatible With TTL or CMOS Levels**
- **Very Low Standby Power . . . 10 mW Typ**
- **50-V Noninductive Switching Voltage Capability**
- **40-V Inductive Switching Voltage Capability**
- **Output Clamp Diodes for Inductive Transient Protection**
- **2-W Power Package**

NE PACKAGE
(TOP VIEW)



FUNCTION TABLES

(Each Channel 1 or Channel 4 Driver)

INPUTS		OUTPUT
A	$\overline{G}$	Y
H	L	L
L	X	H
X	H	H

(Each Channel 2 or Channel 3 Driver)

INPUTS		OUTPUT
A	$\overline{G}$	Y
L	L	L
H	X	H
X	H	H

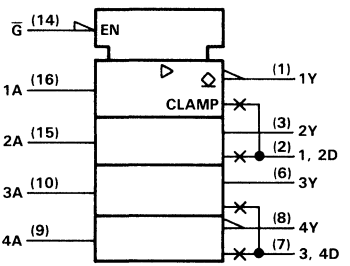
H = high level
L = low level
X = irrelevant

description

The SN75439 quadruple peripheral driver is designed for use in systems requiring high current, high voltage, and high load power. The device features two inverting and two noninverting open-collector outputs with a common-enable input that, when taken high, disables all four outputs. By pairing each inverting channel with a corresponding noninverting channel (such as channel 1 paired with channel 2 and channel 3 paired with channel 4), the device may be used as a complete full-step 4-phase dc stepper motor driver using only two input logic control signals plus the enable signal, as shown in Figure 3. Other applications include driving relays, lamps, solenoids, motors, LEDs, transmission lines, hammers, and other high-power-demand loads.

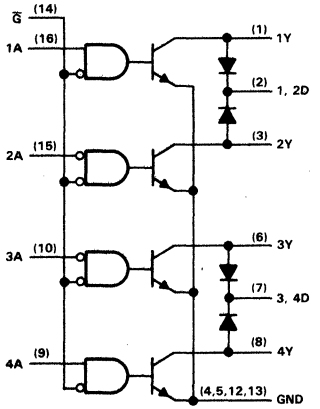
The SN75439 is characterized for operation from 0°C to 70°C.

logic symbol†

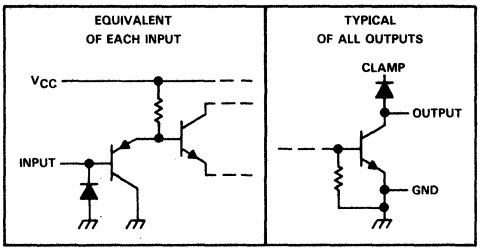


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 7 V
Input voltage, V_I . . . . . 7 V
Output voltage range, V_O . . . . . −0.3 V to 52 V
Output voltage, V_O (inductive load) . . . . . 43 V
Output clamp-diode terminal voltage range, V_{OK} . . . . . −0.3 V to 52 V
Input current, I_I . . . . . −15 mA
Peak sink output current, I_{OM} (nonrepetitive, $t_w \leq 0.1$ ms) (see Note 2) . . . . . 1.5 A
(repetitive, $t_w \leq 10$ ms, duty cycle $\leq 50\%$) . . . . . 1.4 A
Continuous sink output current, I_O (see Note 2) . . . . . 1.3 A
Peak output clamp diode current, I_{OKM} (nonrepetitive, $t_w \leq 0.1$ ms) (see Note 2) . . . . . 1.5 A
(repetitive, $t_w \leq 10$ ms, duty cycle $\leq 50\%$) . . . . . 1.3 A
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 2075 mW
Continuous total dissipation at (or below) 65°C case temperature (see Note 3) . . . . . 5000 mW
Operating case or virtual junction temperature range . . . . . −55°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal (unless otherwise specified).
2. All four channels of this device may conduct rated current simultaneously; however, power dissipation average over a short time interval must fall within the continuous dissipation range.
3. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C. For operation above 65°C case temperature, derate linearly at the rate of 59 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Output supply voltage in inductive switching circuit, V_S (see Figure 2)			40	V
High-level input voltage, V_{IH}	2		5.25	V
Low-level input voltage, V_{IL}	−0.3†		0.8	V
Low-level output current, I_{OL}			1.3	A
Operating free-air temperature, T_A	0	25	70	°C

† The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltages (unless otherwise noted)

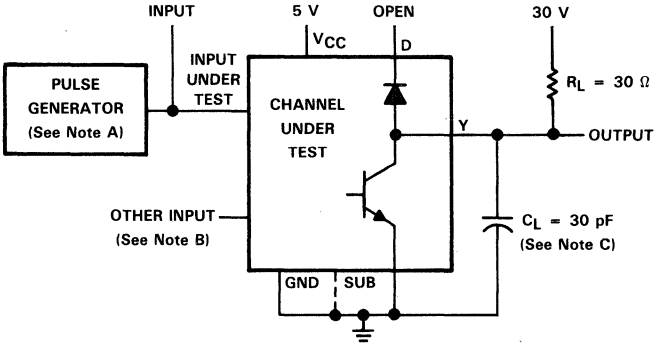
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −12 mA			−0.9	−1.5	V
V_{OL}	Low-level output voltage	I_{OL} = 0.5 A	See Note 4		0.2	0.35	V
		I_{OL} = 1 A			0.4	0.7	
		I_{OL} = 1.3 A			0.5	0.9	
$V_{F(K)}$	Output clamp diode forward voltage	I_F = 0.5 A	See Note 4		1.1	1.9	V
		I_F = 1 A			1.3	2.2	
		I_F = 1.3 A			1.4	2.4	
I_{OH}	High-level output current	V_{OH} = 50 V,	V_{OK} = 50 V			100	µA
I_{IH}	High-level input current	$V_I = V_{IH}$				10	µA
I_{IL}	Low-level input current	V_I = 0 to 0.8 V				−10	µA
$I_{R(K)}$	Output clamp-diode reverse current (at Y output)	V_R = 50 V,	V_O = 0			100	µA
I_{CC}	Supply current	All outputs at high level (off)			2	8	mA
		All outputs at low level (on)			140	200	
		Two outputs at high level (off) and two outputs at low level (on)			70	110	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 4: These parameters must be measured using pulse techniques, t_w = 1 ms, duty cycle ≤ 10%.

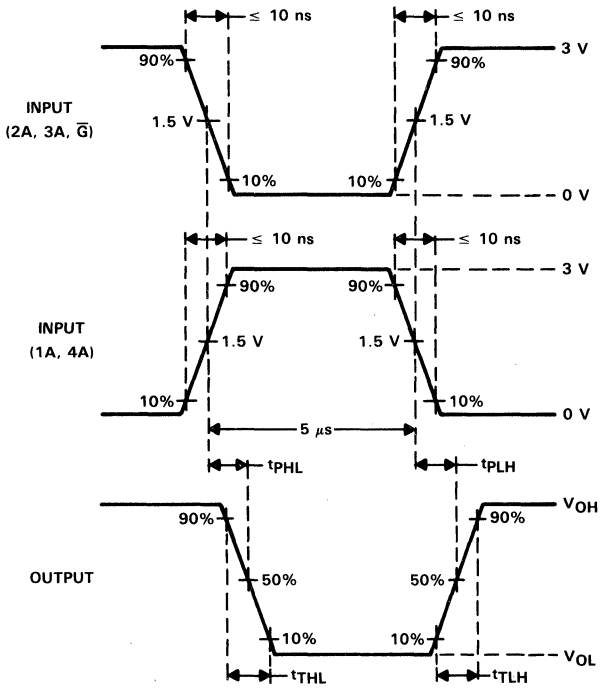
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_{OL}≈1 A, R_L = 30 Ω,	C_L = 30 pF, See Figure 1		1500		ns
t_{PHL}	Propagation delay time, high-to-low-level output				100		ns
t_{TLH}	Transition time, low-to-high-level output				170		ns
t_{THL}	Transition time, high-to-low-level output				50		ns
V_{OH}	High-level output voltage (after switching inductive load)	V_S = 40 V, R_L = 31 Ω,	I_O≈1.3 A, See Figure 2	V_S−100			mV

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

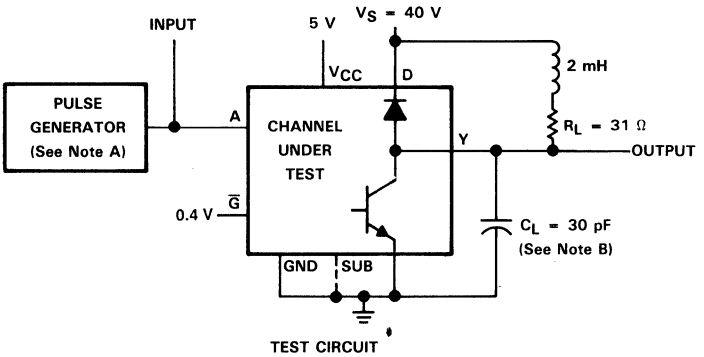


VOLTAGE WAVEFORMS

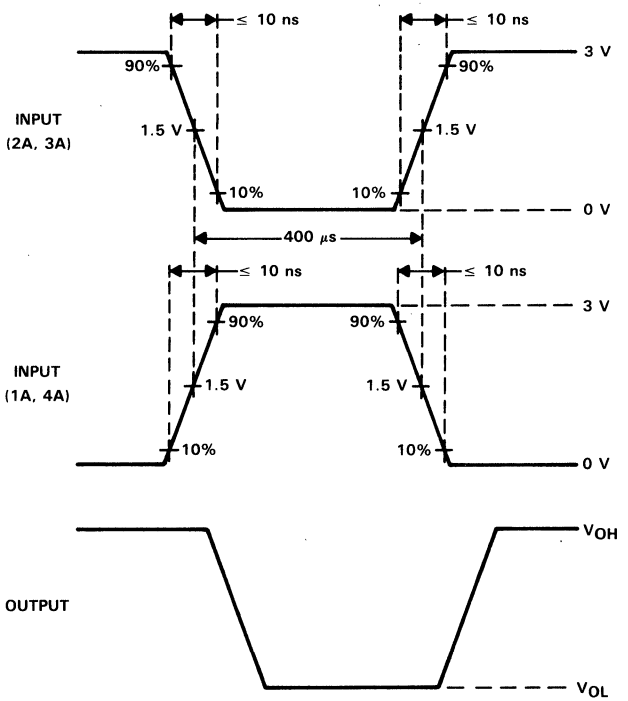
NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, Z_O = 50 Ω.
B. Enable input $\overline{G}$ is at 0 V if input A is used as the switching input. When $\overline{G}$ is used as the switching input, the corresponding A input is at 0 V if testing channel 2 or channel 3 or at 3 V if testing channel 1 or channel 4.
C. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 2. OUTPUT LATCH-UP TEST

APPLICATION INFORMATION

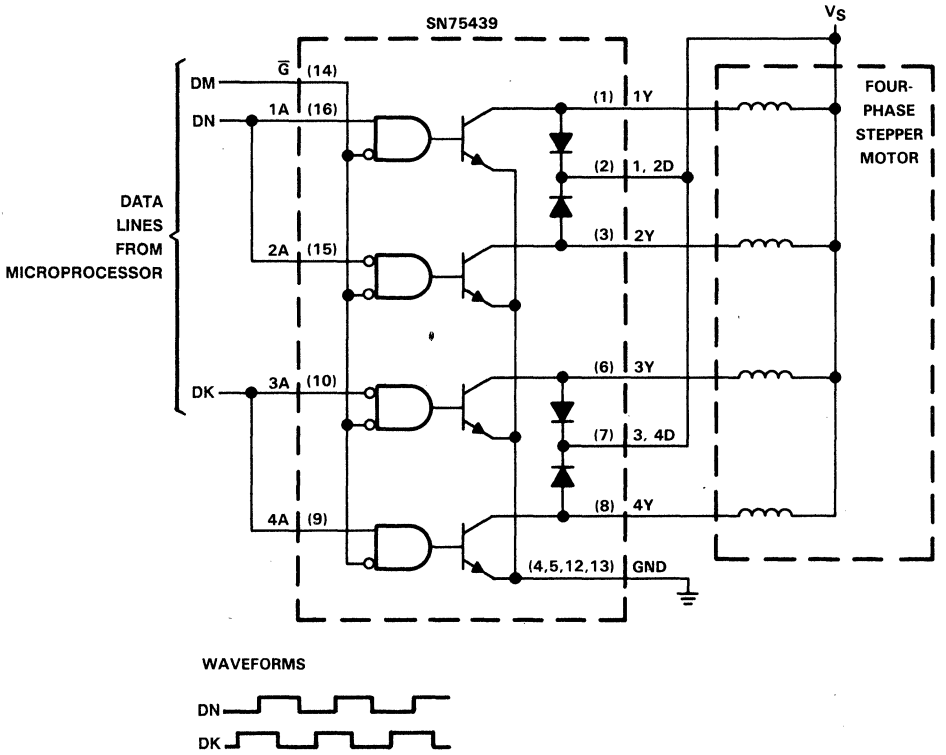


FIGURE 3. FULL-STEP FOUR-PHASE STEPPER MOTOR DRIVER

D2481, DECEMBER 1978—REVISED DECEMBER 1989

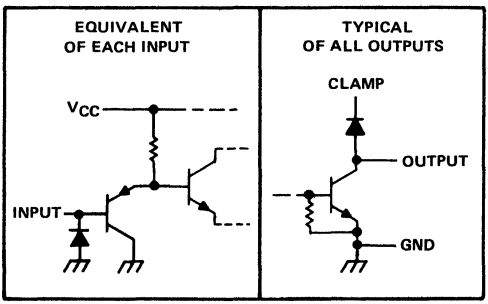
- **Very Low Power Requirements**
- **Very Low Input Current**
- **Characterized for Use to 350 mA**
- **No Output Latch-Up at 50 V (After Conducting 300 mA)**
- **High-Voltage Outputs (70 V Min)**
- **Output Clamp Diodes for Transient Suppression (350 mA, 70 V)**
- **TTL- or MOS-Compatible Diode-Clamped Inputs**
- **Standard Supply Voltage**
- **Suitable for Hammer-Driver Applications**

description

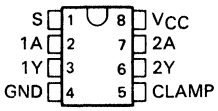
Series SN75446 dual peripheral drivers are designed for use in systems that require high current, high voltage, and fast switching times. The SN75446, SN75447, SN75448, and SN75449 provide AND, NAND, OR, and NOR drivers, respectively. These devices have diode-clamped inputs as well as high-current, high-voltage inductive-clamp diodes on the outputs.

Series SN75446 drivers are characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



D OR P PACKAGE
(TOP VIEW)



FUNCTION TABLES

SN75446
(EACH AND DRIVER)

INPUTS		OUTPUT
A	S	Y
H	H	H
L	X	L
X	L	L

SN75447
(EACH NAND DRIVER)

INPUTS		OUTPUT
A	S	Y
H	H	L
L	X	H
X	L	H

SN75448
(EACH OR DRIVER)

INPUTS		OUTPUT
A	S	Y
H	X	H
X	H	H
L	L	L

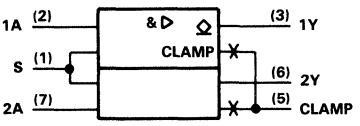
SN75449
(EACH NOR DRIVER)

INPUTS		OUTPUT
A	S	Y
H	X	L
X	H	L
L	L	H

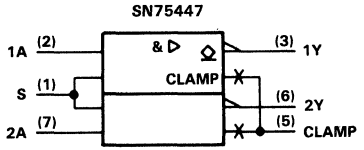
H = high level
L = low level
X = irrelevant

logic symbols†

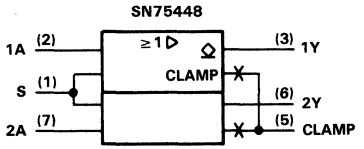
SN75446



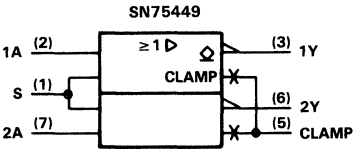
SN75447



SN75448



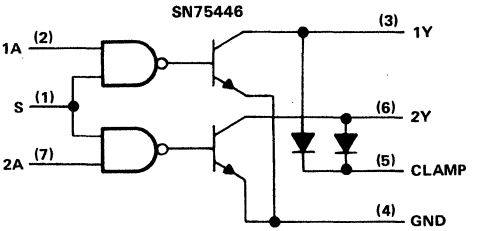
SN75449



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

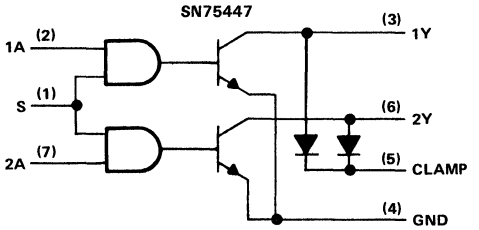
logic diagrams (positive logic)

SN75446



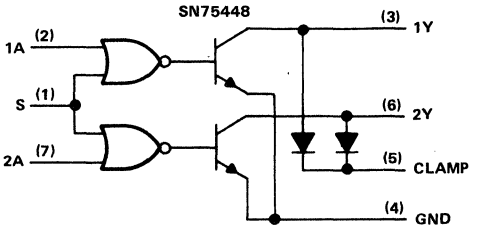
positive logic: $Y = AS$ or $\overline{\overline{A}+\overline{S}}$

SN75447



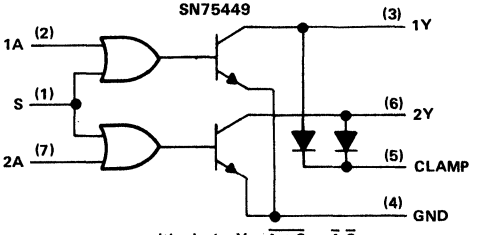
positive logic: $Y = \overline{AS}$ or $\overline{A} + \overline{S}$

SN75448



positive logic: $Y = A + S$ or $\overline{\overline{A}\,\overline{S}}$

SN75449



positive logic: $Y = \overline{A} + \overline{S}$ or $\overline{A}\,\overline{S}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Output current (see Note 2) . . . . . 400 mA
Output clamp diode current . . . . . 400 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

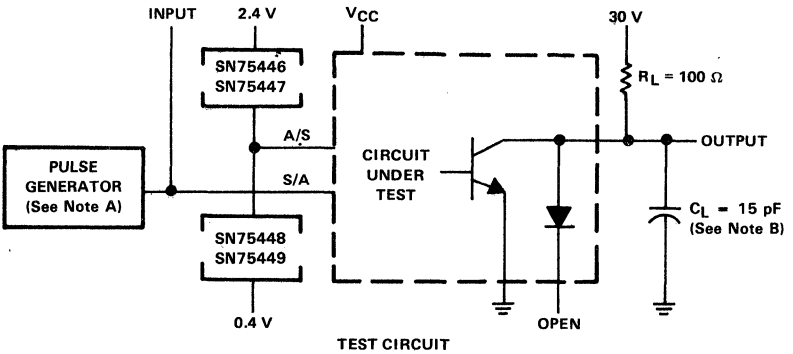
electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		$I_I = -12$ mA			−0.9	−1.5	V
I_{OH}	High-level output current		$V_{CC} = 4.75$ V, $V_{IL} = 0.8$ V,	$V_{IH} = 2$ V, $V_{OH} = 70$ V		1	100	μA
V_{OL}	Low-level output voltage		$V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V	$I_{OL} = 100$ mA		0.10	0.3	V
				$I_{OL} = 200$ mA		0.22	0.45	
				$I_{OL} = 300$ mA		0.45	0.65	
				$I_{OL} = 350$ mA		0.55	0.75	
$V_{(BR)O}$	Output breakdown voltage		$V_{CC} = 4.75$ V,	$I_{OH} = 100$ μA	70	100		V
$V_{R(K)}$	Output clamp diode reverse voltage		$V_{CC} = 4.75$ V,	$I_R = 100$ μA	70	100		V
$V_{F(K)}$	Output clamp diode forward voltage		$V_{CC} = 4.75$ V,	$I_F = 350$ mA	0.6	1.2	1.6	V
I_{IH}	High-level input current		$V_{CC} = 5.25$ V,	$V_I = 5.25$ V		0.01	10	μA
I_{IL}	Low-level input current	A input	$V_{CC} = 5.25$ V,	$V_I = 0.8$ V		−0.5	−10	μA
		Strobe S				−1	−20	
I_{CCH}	Supply current, outputs high	SN75446	$V_{CC} = 5.25$ V	$V_I = 5$ V		11	18	mA
		SN75447		$V_I = 0$		11	18	
		SN75448		$V_I = 5$ V		18	25	
		SN75449		$V_I = 0$		18	25	
I_{CCL}	Supply current, outputs low	SN75446	$V_{CC} = 5.25$ V	$V_I = 0$		11	18	mA
		SN75447		$V_I = 5$ V		11	18	
		SN75448		$V_I = 0$		18	25	
		SN75449		$V_I = 5$ V		18	25	

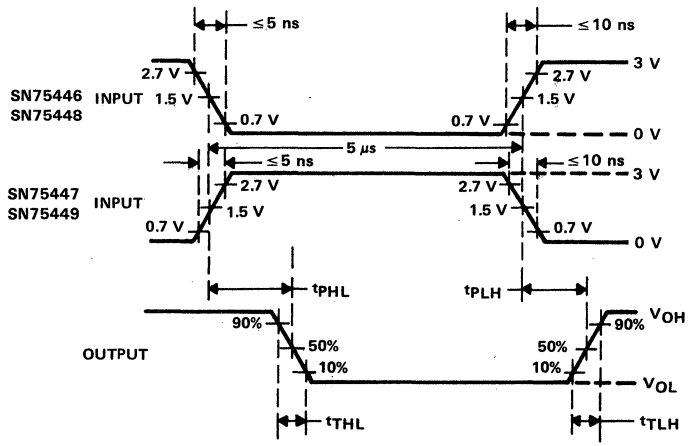
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 100 Ω, See Figure 1		300	750	ns
t_{PHL}	Propagation delay time, high-to-low-level output			200	500	ns
t_{TLH}	Transition time, low-to-high-level output			50	100	ns
t_{THL}	Transition time, high-to-low-level output			50	100	ns
V_{OH}	High-level output voltage after switching	V_S = 55 V, I_O ≈300 mA, See Figure 2	V_S−0.018			V

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

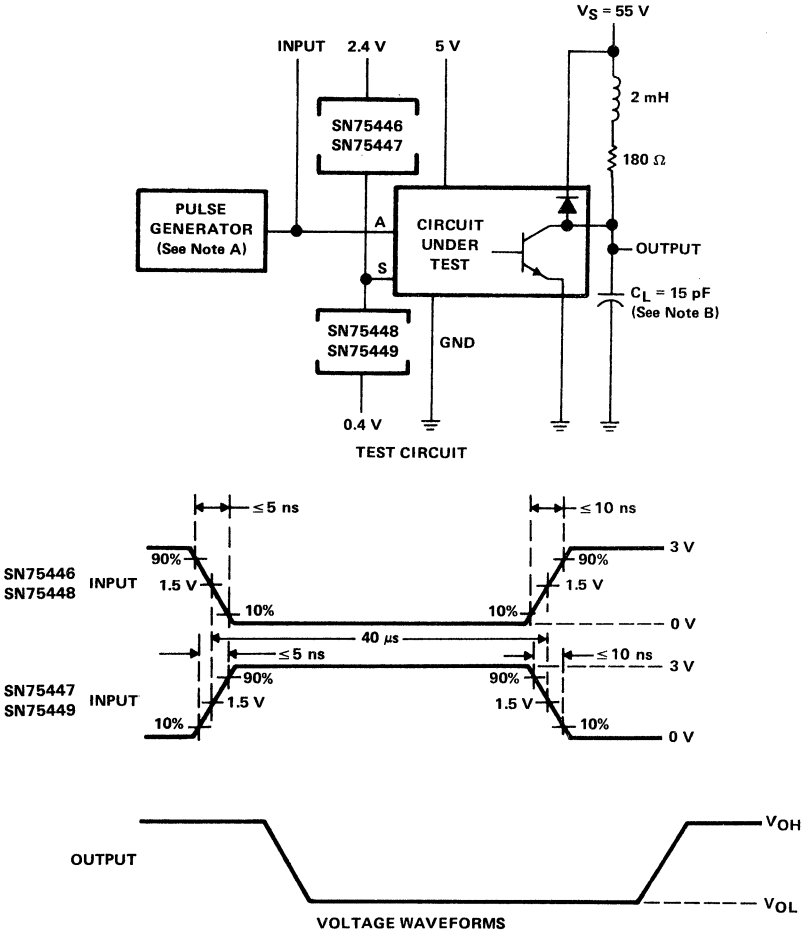


VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

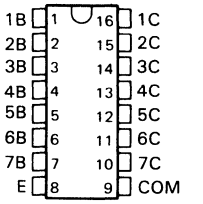
FIGURE 2. LATCH-UP TEST

D2625, DECEMBER 1976—REVISED SEPTEMBER 1986

HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- **500-mA Rated Collector Current (Single Output)**
- **High-Voltage Outputs . . . 100 V**
- **Output Clamp Diodes**
- **Inputs Compatible with Various Types of Logic**
- **Relay Driver Applications**
- **Higher-Voltage Versions of ULN2005A, ULN2001A, ULN2002A, ULN2003A, and ULN2004A, Respectively, for Commercial Temperature Range**

D OR N PACKAGE
(TOP VIEW)

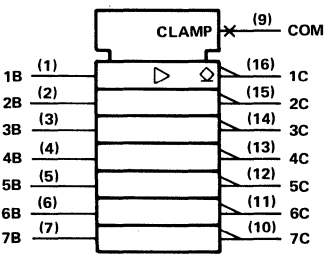


description

The SN75465, SN75466, SN75467, SN75468, and SN75469 are monolithic high-voltage, high-current Darlington transistor arrays. Each consists of seven n-p-n Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

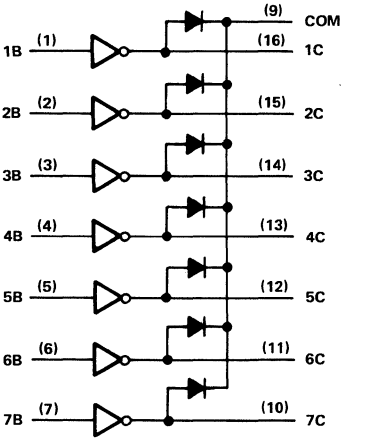
The SN75465 has a 1050-Ω series base resistor and is especially designed for use with TTL where higher current is required and loading of the driving source is not a concern. The SN75466 is a general-purpose array and may be used with TTL, P-MOS, CMOS, and other MOS technologies. The SN75467 is specifically designed for use with 14- to 25-V P-MOS devices and each input has a zener diode and resistor in series to limit the input current to a safe limit. The SN75468 has a 2700-Ω series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS. The SN75469 has a 10.5-kΩ series base resistor to allow its operation directly from CMOS or P-MOS that use supply voltages of 6 to 15 V. The required input current is below that of the SN75468 and the required voltage is less than that required by the SN75467.

logic symbol†

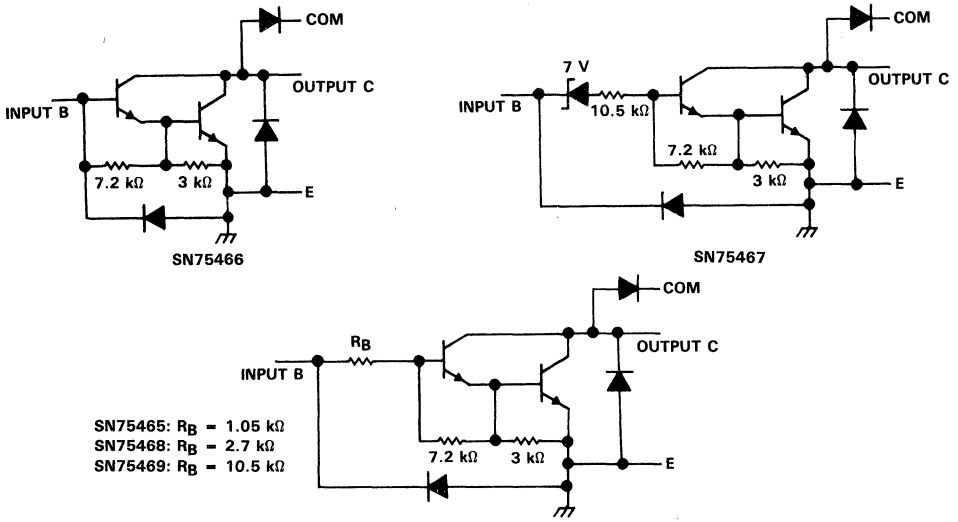


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics (each Darlington pair)



All resistor values shown are nominal.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-emitter voltage	100 V
Input voltage (see Note 1): SN75465	15 V
SN75467, SN75468, SN75469	30 V
Peak collector current (see Figures 14 and 15)	500 mA
Output clamp diode current	500 mA
Total emitter-terminal current	−2.5 A
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: All voltage values are with respect to the emitter/substrate terminal, E, unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS			SN75465			UNIT
						MIN	TYP	MAX	
I_{CEX}	Collector cutoff current	1	$V_{CE}=100$ V,	$I_I=0$				50	μA
			$V_{CE}=100$ V,	$I_I=0$,	$T_A=70°C$			100	
$I_{I(off)}$	Off-state input current	3	$V_{CE}=100$ V,	$I_C=500$ μA,	$T_A=70°C$	50	65		μA
I_I	Input current	4	$V_I=3$ V				1.5	2.4	mA
$V_{I(on)}$	On-state input voltage	5	$V_{CE}=2$ V,	$I_C=350$ mA				2.4	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	6	$I_I=250$ μA,	$I_C=100$ mA			0.9	1.1	V
			$I_I=350$ μA,	$I_C=200$ mA			1	1.3	
			$I_I=500$ μA,	$I_C=350$ mA			1.2	1.6	
I_R	Clamp diode reverse current	7	$V_R=100$ V					50	μA
			$V_R=100$ V,	$T_A=70°C$				100	
V_F	Clamp diode forward voltage	8	$I_F=350$ mA				1.7	2	V
C_i	Input capacitance		$V_I=0$,	$f=1$ MHz			15	25	pF

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS			SN75466			SN75467			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
I_{CEX}	Collector cutoff current	1	$V_{CE}=100$ V,	$I_I=0$				50			50	μA
			$V_{CE}=100$ V,	$I_I=0$				100			100	
		2	$T_A=70°C$	$V_I=6$ V				500			500	
$I_{I(off)}$	Off-state input current	3	$V_{CE}=50$ V, $T_A=70°C$	$I_C=500$ μA,		50	65		50	65		μA
I_I	Input current	4	$V_I=17$ V							0.82	1.25	mA
h_{FE}	Static forward current transfer ratio	6	$V_{CE}=2$ V,	$I_C=350$ mA		1000						
$V_{I(on)}$	On-state input voltage	5	$V_{CE}=2$ V,	$I_C=300$ mA							13	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	6	$I_I=250$ μA,	$I_C=100$ mA			0.9	1.1		0.9	1.1	V
			$I_I=350$ μA,	$I_C=200$ mA			1	1.3		1	1.3	
			$I_I=500$ μA,	$I_C=350$ mA			1.2	1.6		1.2	1.6	
I_R	Clamp diode forward voltage	7	$V_R=100$ V					50			50	μA
			$V_R=100$ V,	$T_A=70°C$				100			100	
V_F	Clamp diode forward voltage	8	$I_F=350$ mA				1.7	2		1.7	2	V
C_i	Input capacitance		$V_I=0$,	$f=1$ MHz			15	25		15	25	pF

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		SN75468			SN75469			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CEX}	Collector cutoff current	1	V_{CE} = 100 V,	I_I = 0			50			50	μA
			V_{CE} = 100 V,	I_I = 0			100			100	
		2	T_A = 70°C	V_I = 1 V						500	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 μA,	50	65		50	65		μA
I_I	Input current	4	V_I = 3.85 V			0.93	1.35				mA
			V_I = 5 V						0.35	0.5	
			V_I = 12 V						1	1.45	
$V_{I(on)}$	On-state input voltage	5	V_{CE} = 2 V	I_C = 125 mA						5	V
				I_C = 200 mA			2.4			6	
				I_C = 250 mA			2.7				
				I_C = 275 mA						7	
				I_C = 300 mA			3				
				I_C = 350 mA						8	
$V_{CE(sat)}$	Collector-emitter saturation voltage	6	I_I = 250 μA,	I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 μA,	I_C = 200 mA		1	1.3		1	1.3	
			I_I = 500 μA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
I_R	Clamp diode reverse current	7	V_R = 100 V				50			50	μA
			V_R = 100 V,	T_A = 70°C			100			100	
V_F	Clamp diode forward voltage	8	I_F = 350 mA			1.7	2		1.7	2	V
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_S = 50 V,	R_L = 163 Ω,		0.25	1	μs
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	See Figure 9		0.25	1	μs
V_{OH}	High-level output voltage after switching	V_S = 50 V, See Figure 10	I_O ≈ 300 mA,	V_S − 20			mV

PARAMETER MEASUREMENT INFORMATION

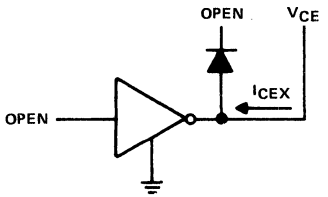


FIGURE 1. I_{CEX}

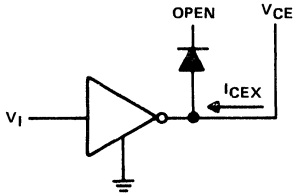


FIGURE 2. I_{CEX}

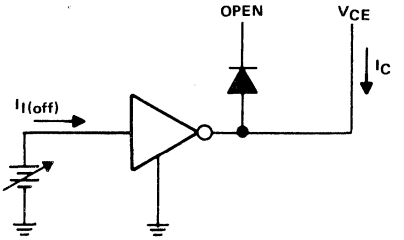


FIGURE 3. $I_{I(off)}$

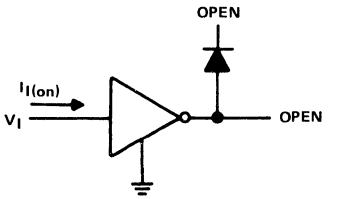


FIGURE 4. I_I

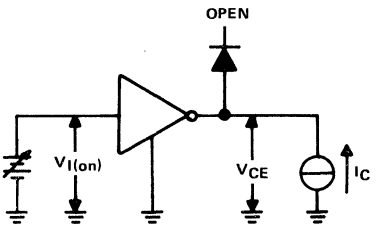
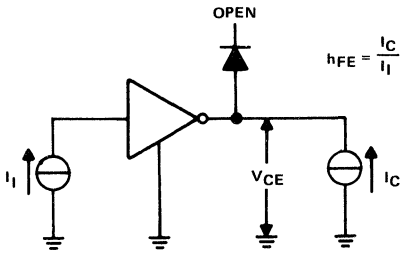


FIGURE 5. $V_{I(on)}$



NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE}.

FIGURE 6. h_{FE}, $V_{CE(sat)}$

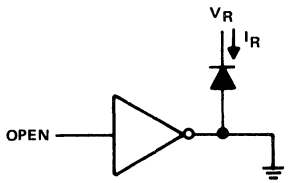


FIGURE 7. I_R

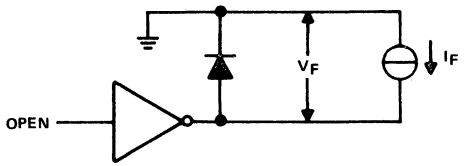
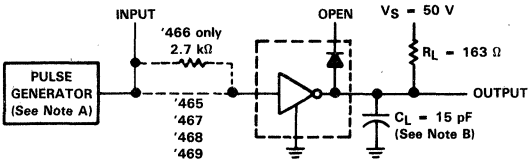
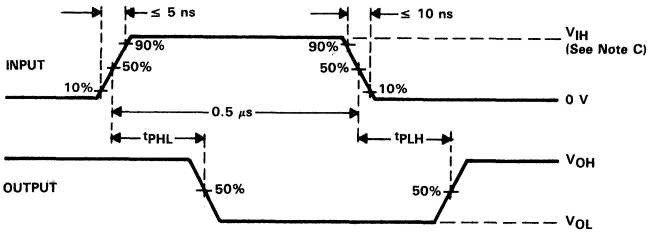


FIGURE 8. V_F

PARAMETER MEASUREMENT INFORMATION



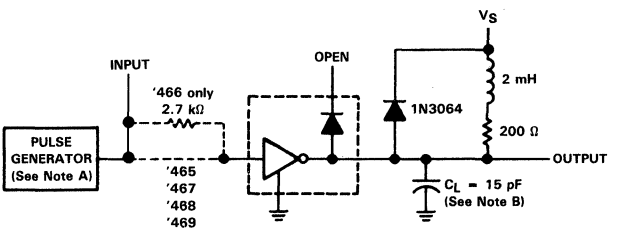
TEST CIRCUIT



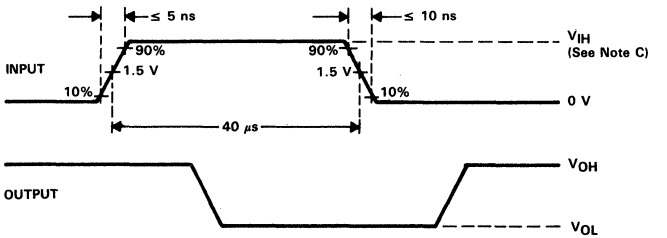
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. For testing the '465, '466, and '468, V_{IH} = 3 V; for the '467, V_{IH} = 13 V; for the '469, V_{IH} = 8 V.

FIGURE 9. PROPAGATION DELAY TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. For testing the '465, '466, and '468, V_{IH} = 3 V; for the '467, V_{IH} = 13 V; for the '469, V_{IH} = 8 V.

FIGURE 10. LATCH-UP TEST

TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (ONE DARLINGTON)

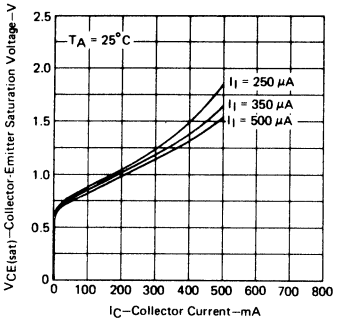


FIGURE 11

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (TWO DARLINGTONS PARALLELED)

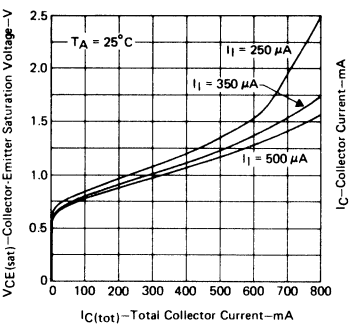


FIGURE 12

COLLECTOR CURRENT vs INPUT CURRENT

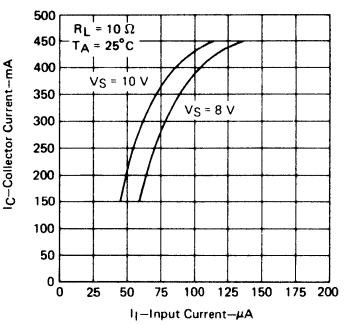


FIGURE 13

THERMAL INFORMATION

D PACKAGE MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE

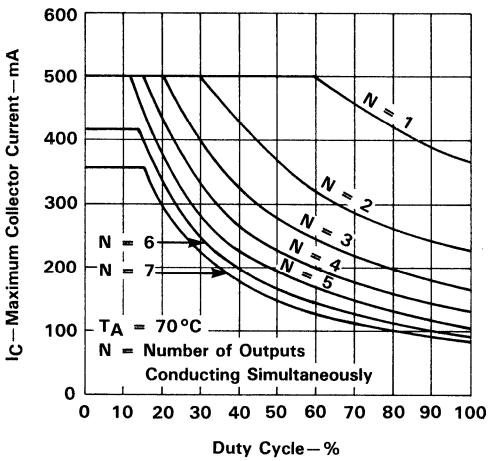


FIGURE 14

N PACKAGE MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE

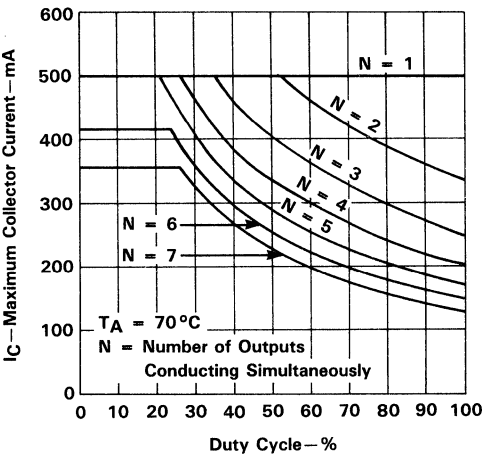
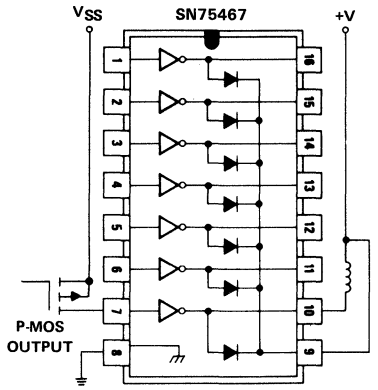
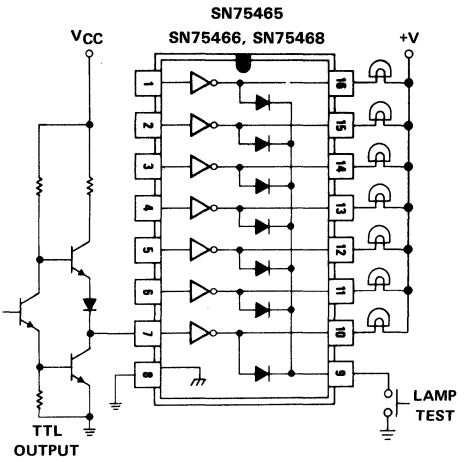


FIGURE 15

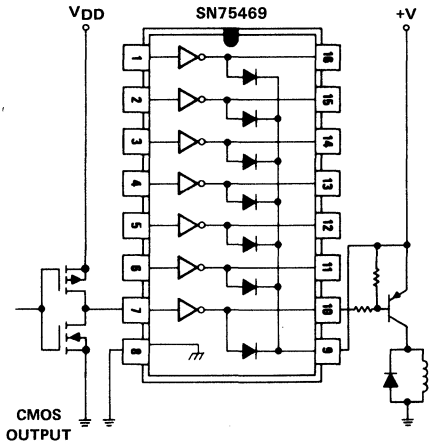
TYPICAL APPLICATION DATA



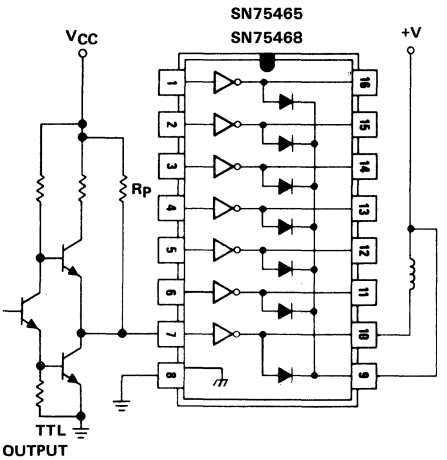
P-MOS TO LOAD



TTL TO LOAD



BUFFER FOR
HIGHER CURRENT LOADS



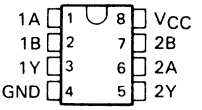
USE OF PULL-UP RESISTORS
TO INCREASE DRIVE CURRENT

D2130, DECEMBER 1976—REVISED MAY 1990

PERIPHERAL DRIVERS FOR HIGH-VOLTAGE, HIGH-CURRENT DRIVER APPLICATIONS

- **Characterized for Use to 300 mA**
- **High-Voltage Outputs**
- **No Output Latch-Up at 55 V (After Conducting 300 mA)**
- **Medium-Speed Switching**
- **Circuit Flexibility for Varied Applications and Choice of Logic Function**
- **TTL-Compatible Diode-Clamped Inputs**
- **Standard Supply Voltages**
- **Plastic DIP (P) with Copper Lead Frame Provides Cooler Operation and Improved Reliability**

D OR P PACKAGE
(TOP VIEW)



SUMMARY OF SERIES SN75471

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN75471	AND	D,P
SN75472	NAND	D,P
SN75473	OR	D,P

description

Series SN75471 dual peripheral drivers are functionally interchangeable with Series SN75451B and Series SN75461 peripheral drivers, but are designed for use in systems that require higher breakdown voltages than either of those series can provide at the expense of slightly slower switching speeds than Series 75451B (limits are the same as Series SN75461). Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN75471, SN75472, and SN75473 are dual peripheral AND, NAND, and OR drivers, respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

Series SN75471 drivers are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Off-state output voltage . . . . . 70 V
Continuous collector or output current (see Note 3) . . . . . 400 mA
Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 3) . . . . . 500 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to the network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

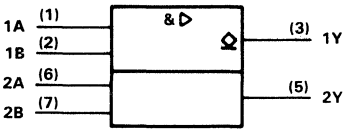
DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

logic symbol†



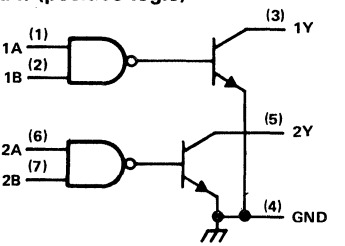
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(EACH DRIVER)

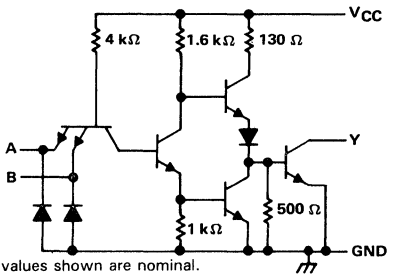
A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

positive logic: $Y = AB$ or $\overline{\overline{A}+\overline{B}}$

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

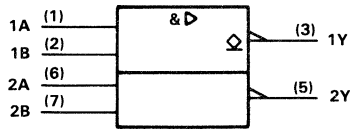
PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −12 mA		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{OH} = 70 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.4	V
		V_{CC} = 4.75 V, V_{IL} = 0.8 V I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V, V_I = 5 V		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V, V_I = 0		56	76	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output			25	40	ns
t_{TLH}	Transition time, low-to-high-level output			8	20	ns
t_{THL}	Transition time, high-to-low-level output			10	20	ns
V_{OH}	High-level output voltage after switching	V_S = 55 V, $I_O \approx$ 300 mA, See Figure 2	V_S−18			mV

logic symbol†



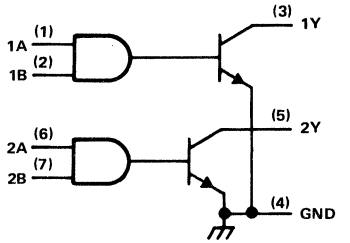
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(EACH DRIVER)

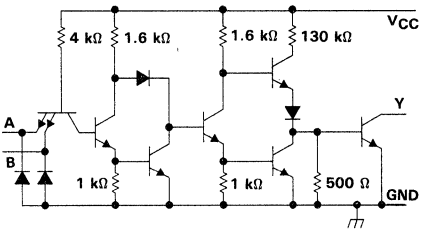
A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

positive logic:
$Y = \overline{AB}$ or $\overline{A}+\overline{B}$

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −12 mA		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{OH} = 70 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.4	V
		V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V, V_I = 5 V		13	17	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V, V_I = 0		61	76	mA

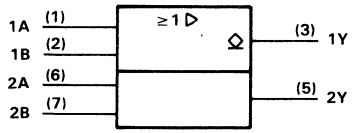
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		45	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output			30	50	ns
t_{TLH}	Transition time, low-to-high-level output			13	25	ns
t_{THL}	Transition time, high-to-low-level output			10	20	ns
V_{OH}	High-level output voltage after switching	V_S = 55 V, $I_O \approx$ 300 mA, See Figure 2	V_S−18			mV

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic symbol†



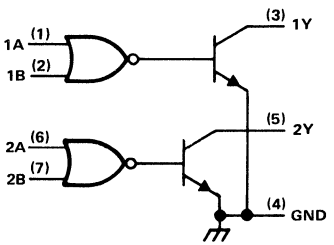
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(EACH DRIVER)

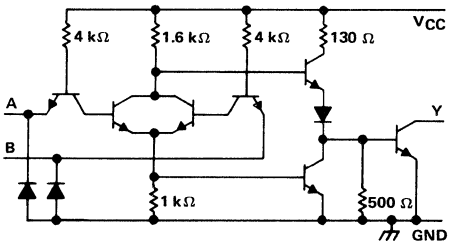
A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

positive logic:
$Y = A + B$ or $\overline{\overline{A}\,\overline{B}}$

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

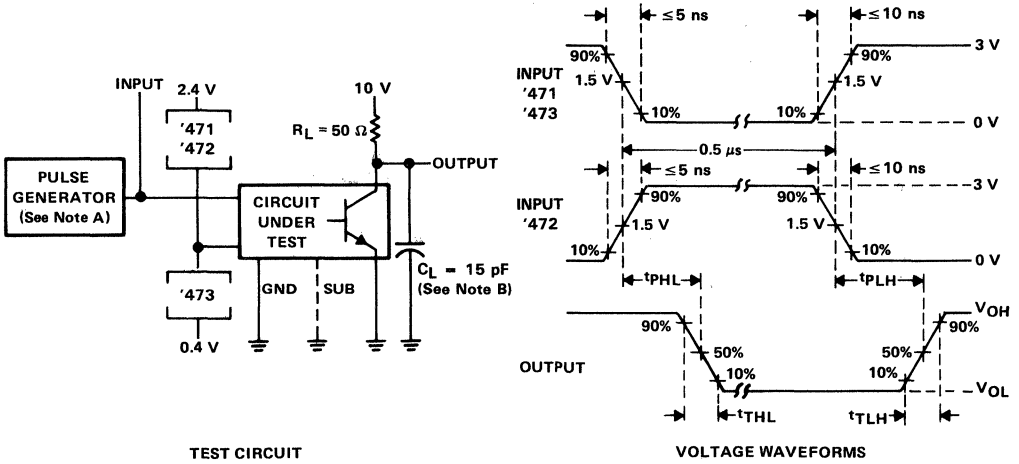
PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −12 mA		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{OH} = 70 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.4	V
		V_{CC} = 4.75 V, V_{IL} = 0.8 V I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V, V_I = 5 V		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V, V_I = 0		58	76	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output			25	40	ns
t_{TLH}	Transition time, low-to-high-level output			8	25	ns
t_{THL}	Transition time, high-to-low-level output			10	25	ns
I_{OH}	High-level output voltage after switching	V_S = 55 V, $I_O \approx$ 300 mA, See Figure 2	V_S−18			mV

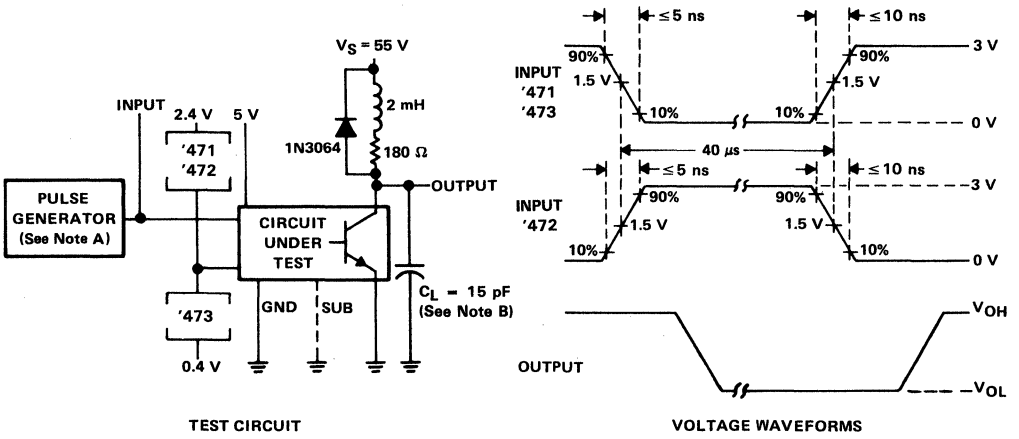
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 12.5 kHz, Z_O ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 2. LATCH-UP TEST

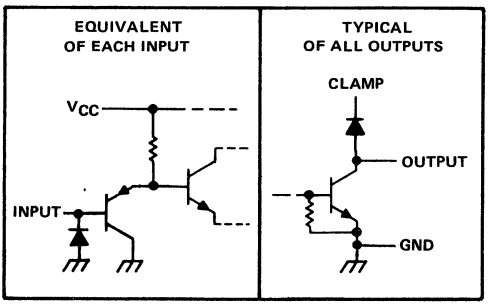
D2284, DECEMBER 1976—REVISED DECEMBER 1989

- **Characterized for Use to 300 mA**
- **No Output Latch-Up at 55 V (After Conducting 300 mA)**
- **High-Voltage Outputs (100 V Typical)**
- **Output Clamp Diodes for Transient Suppression (300 mA, 70 V)**
- **TTL- or MOS-Compatible Diode-Clamped Inputs**
- **P-N-P Inputs Reduce Input Current**
- **Standard Supply Voltage**
- **Suitable for Hammer-Driver Applications**
- **Plastic DIP (P) with Copper Lead Frame Provides Cooler Operation and Improved Reliability**

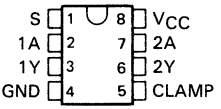
description

Series SN75476 dual peripheral drivers are designed for use in systems that require high current, high voltage, and fast switching times. The SN75476, SN75477, SN75478, and SN75479 provide AND, NAND, OR, and NOR drivers, respectively. These devices have diode-clamped inputs as well as high-current, high-voltage clamp diodes on the outputs for inductive transient protection.

The SN75476, SN75477, SN75478, and SN75479 drivers are characterized for operation from 0°C to 70°C.



D OR P PACKAGE
(TOP VIEW)



FUNCTION TABLES

SN75476
(EACH AND DRIVER)

INPUTS		OUTPUT
A	S	Y
H	H	H
L	X	L
X	L	L

SN75477
(EACH NAND DRIVER)

INPUTS		OUTPUT
A	S	Y
H	H	L
L	X	H
X	L	H

SN75478
(EACH OR DRIVER)

INPUTS		OUTPUT
A	S	Y
H	X	H
X	H	H
L	L	L

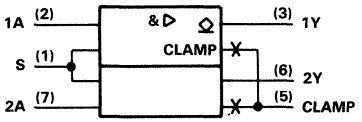
SN75479
(EACH NOR DRIVER)

INPUTS		OUTPUT
A	S	Y
H	X	L
X	H	L
L	L	H

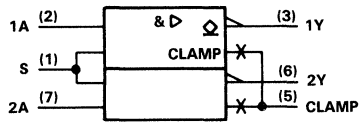
H = high level
L = low level
X = irrelevant

logic symbols†

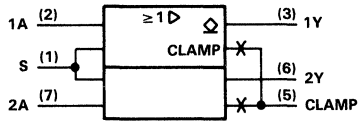
SN75476



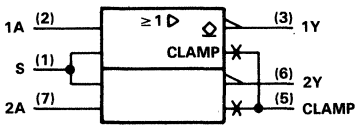
SN75477



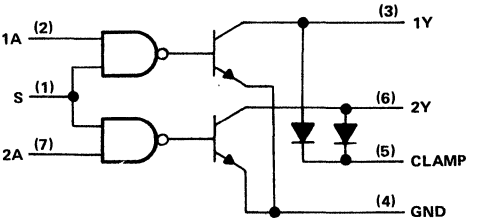
SN75478



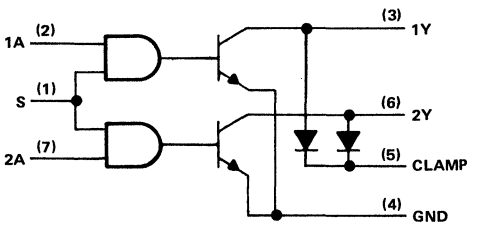
SN75479



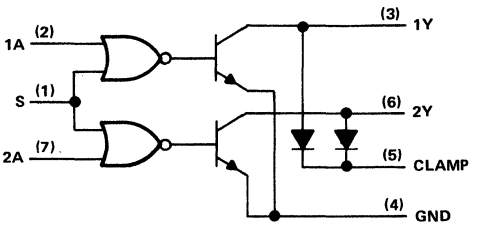
logic diagrams (positive logic)



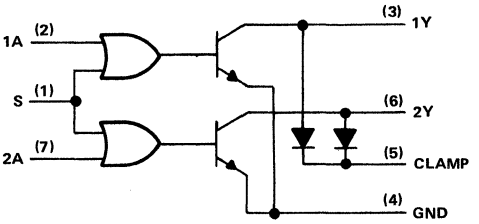
positive logic: $Y = AS$ or $\overline{\overline{A}+\overline{S}}$



positive logic: $Y = \overline{A\overline{S}}$ or $\overline{A} + \overline{S}$



positive logic: $Y = A + S$ or $\overline{\overline{A}\,\overline{S}}$



positive logic: $Y = \overline{A + S}$ or $\overline{A}\,\overline{S}$

† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous output current (see Note 2) . . . . . 400 mA
Peak output current: $t_w \leq 10$ ms, duty cycle $\leq 50\%$ . . . . . 500 mA
$t_w \leq 30$ ns, duty cycle $\leq 0.002\%$ . . . . . 3 A
Output clamp diode current . . . . . 400 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range

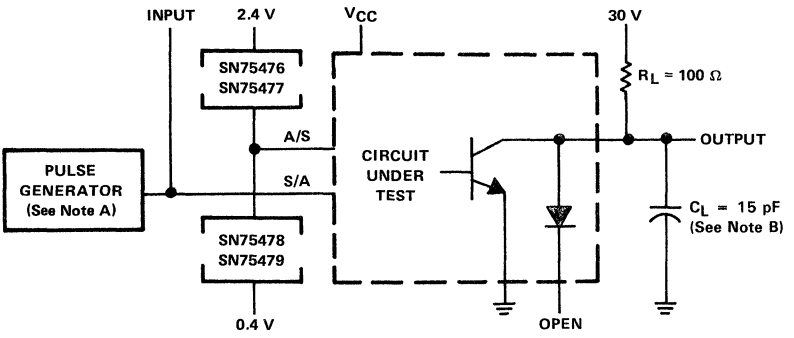
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		$I_I = -12$ mA			−0.95	−1.5	V
I_{OH}	High-level output current		$V_{CC} = 4.5$ V, $V_{IL} = 0.8$ V,	$V_{IH} = 2$ V, $V_{OH} = 70$ V		1	100	μA
V_{OL}	Low-level output voltage		$V_{CC} = 4.5$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V	$I_{OL} = 100$ mA		0.16	0.3	V
				$I_{OL} = 175$ mA		0.22	0.5	
				$I_{OL} = 300$ mA		0.33	0.6	
$V_{(BR)O}$	Output breakdown voltage		$V_{CC} = 4.5$ V,	$I_{OH} = 100$ μA	70	100		V
$V_{R(K)}$	Output clamp diode reverse voltage		$V_{CC} = 4.5$ V,	$I_R = 100$ μA	70	100		V
$V_{F(K)}$	Output clamp diode forward voltage		$V_{CC} = 4.5$ V,	$I_F = 300$ mA	0.8	1.15	1.6	V
I_{IH}	High-level input current		$V_{CC} = 5.5$ V,	$V_I = 5.5$ V		0.01	10	μA
I_{IL}	Low-level input current	A input	$V_{CC} = 5.5$ V,	$V_I = 0.8$ V		−80	−110	μA
		Strobe S				−160	−220	
I_{CCH}	Supply current, outputs high	SN75476	$V_{CC} = 5.5$ V	$V_I = 5$ V		10	17	mA
		SN75477		$V_I = 0$		10	17	
		SN75478		$V_I = 5$ V		10	17	
		SN75479		$V_I = 0$		10	17	
I_{CCL}	Supply current, outputs low	SN75476	$V_{CC} = 5.5$ V	$V_I = 0$		54	75	mA
		SN75477		$V_I = 5$ V		54	75	
		SN75478		$V_I = 0$		54	75	
		SN75479		$V_I = 5$ V		54	75	

†All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

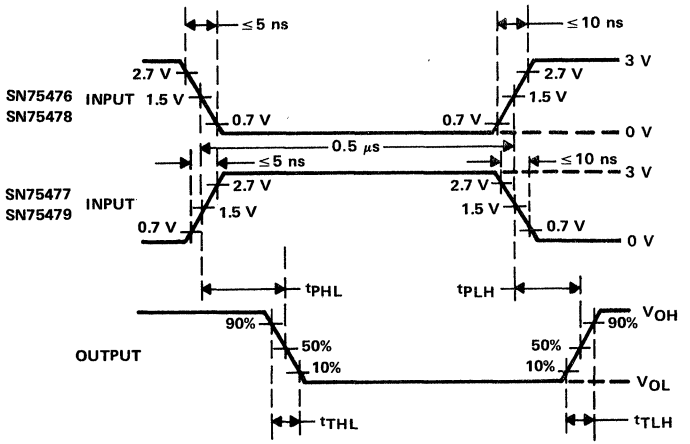
switching characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 100 Ω, See Figure 1		200	350	ns
t_{PHL}	Propagation delay time, high-to-low-level output			200	350	ns
t_{TLH}	Transition time, low-to-high-level output			50	125	ns
t_{THL}	Transition time, high-to-low-level output			90	125	ns
V_{OH}	High-level output voltage after switching	V_S = 55 V, I_O ≈300 mA, See Figure 2	V_S−18			mV

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

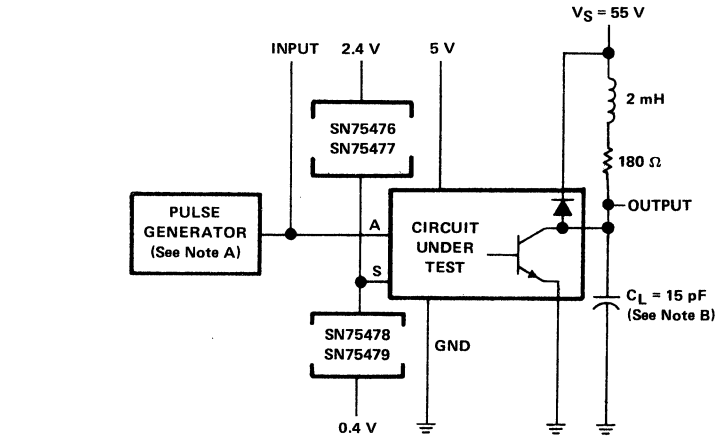


VOLTAGE WAVEFORMS

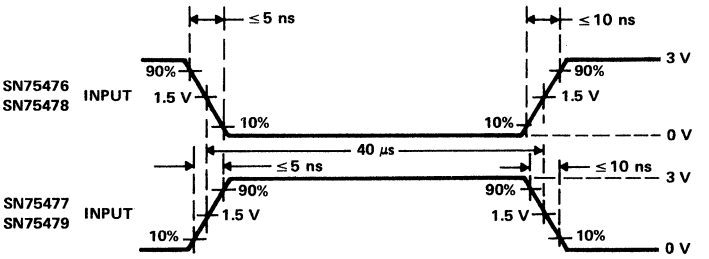
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

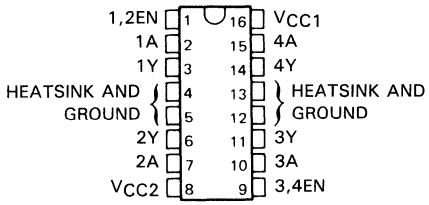
NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 2. LATCH-UP TEST

D2942, NOVEMBER 1986—REVISED MAY 1990

- 1-A Output Current Capability Per Driver
- Output Clamp Diodes for Inductive Transient Suppression
- Applications Include Half-H and Full-H Solenoid Drivers and Motor Drivers
- Designed for Positive-Supply Applications
- Wide Supply Voltage Range: 4.5 V to 36 V
- TTL- and CMOS-Compatible High-Impedance Diode-Clamped Inputs
- Separate Input-Logic Supply
- Thermal Shutdown
- Internal ESD Protection
- Input Hysteresis Improves Noise Immunity
- Three-State Outputs
- Minimized Power Dissipation
- Sink/Source Interlock Circuitry Prevents Simultaneous Conduction
- No Output "Glitch" During Power-Up or Power-Down
- Improved Functional Replacement for the SGS L293D

NE PACKAGE
(TOP VIEW)



FUNCTION TABLE
(EACH DRIVER)

INPUTS†		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

H = high-level
L = low-level
X = irrelevant
Z = high-impedance (off)
† In the thermal shutdown mode, the output is in high-impedance state regardless of the input levels.

description

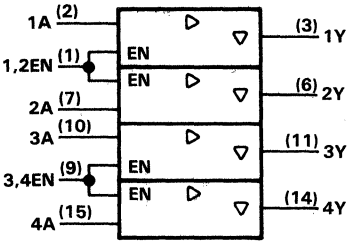
The SN754410 is a quadruple high-current half-H driver designed to provide bidirectional drive currents of up to one ampere at voltages from 4.5 V to 36 V. It is designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

All inputs are compatible with TTL and low-level CMOS logic. Each output (Y) is a complete totem-pole driver with a Darlington transistor sink and a psuedo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs become active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

A separate supply voltage (V_{CC1}) is provided for the logic input circuits to minimize device power dissipation. Supply voltage (V_{CC2}) is used for the output circuits.

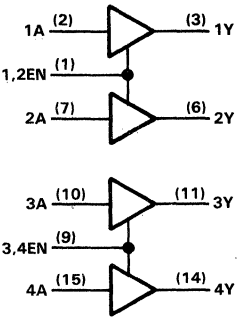
The SN754410 is designed for operation from −40°C to 85°C.

logic symbol†

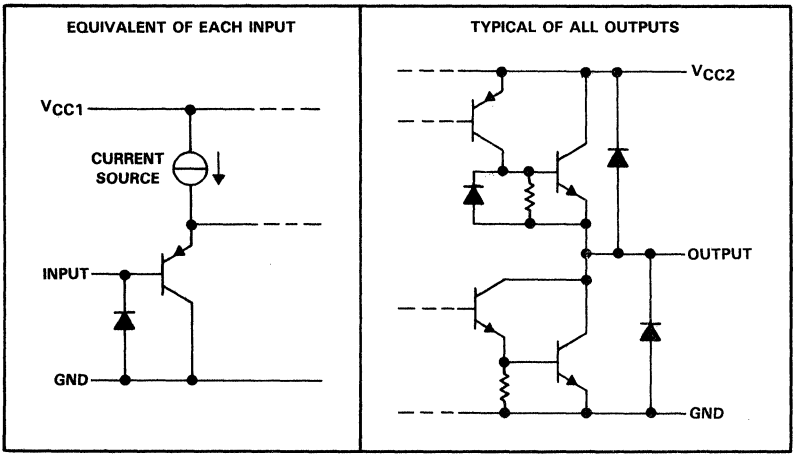


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage range, V_{CC1} (see Note 1) . . . . . −0.5 V to 36 V
Output supply voltage range, V_{CC2} . . . . . −0.5 V to 36 V
Input voltage . . . . . 36 V
Output voltage range, V_O . . . . . −3 V to V_{CC2}+3 V
Peak output current (nonrepetitive, $t_w \leq 5$ ms), I_{PK} . . . . . ±2 A
Continuous output current, I_O . . . . . ±1.1 A
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 2075 mW
Operating free-air temperature range . . . . . −40°C to 85°C
Operating case or virtual junction temperature range . . . . . −40°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC1}	4.5	5.5	V
Output supply voltage, V_{CC2}	4.5	36	V
High-level input voltage, V_{IH}	2	5.5	V
Low-level input voltage, V_{IL}	−0.3†	0.8	V
Operating virtual junction temperature, T_J	−40	125	°C
Operating free-air temperature, T_A	−40	85	°C

† The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating virtual junction temperature (unless otherwise noted)

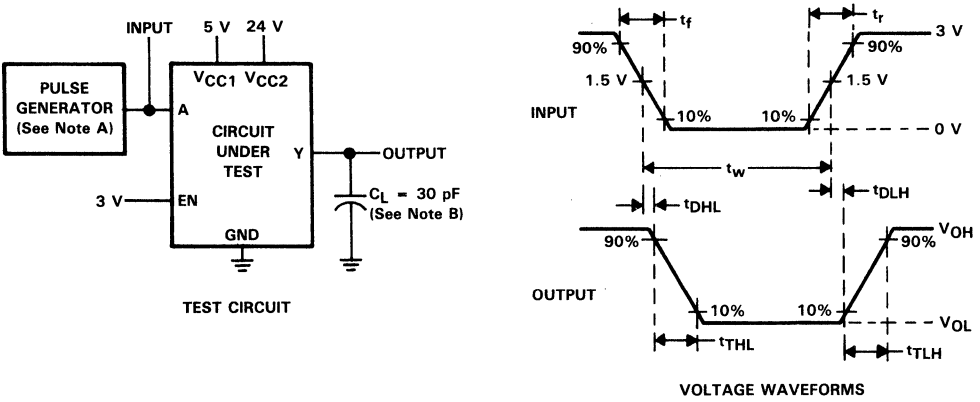
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −12 mA			−0.9	−1.5	V
V_{OH}	High-level output voltage	I_{OH} = −0.5 A		V_{CC2}−1.5	V_{CC2}−1.1		V
		I_{OH} = −1 A		V_{CC2}−2			
		I_{OH} = −1 A, T_J = 25°C		V_{CC2}−1.8	V_{CC2}−1.4		
V_{OL}	Low-level output voltage	I_{OL} = 0.5 A			1	1.4	V
		I_{OL} = 1 A				2	
		I_{OL} = 1 A, T_J = 25°C			1.2	1.8	
V_{OKH}	High-level output clamp voltage	I_{OK} = 0.5 A			V_{CC2}+1.4	V_{CC2}+2	
		I_{OK} = 1 A			V_{CC2}+1.9	V_{CC2}+2.5	
V_{OKL}	Low-level output clamp voltage	I_{OK} = −0.5 A			−1.1	−2	V
		I_{OK} = −1 A			−1.3	−2.5	
I_{OZ}	Off-state (high-impedance state) output current	V_O = V_{CC2}				500	μA
		V_O = 0				−500	
I_{IH}	High-level input current	V_I = 5.5 V					μA
I_{IL}	Low-level input current	V_I = 0				−10	μA
I_{CC1}	Logic supply current	I_O = 0	All outputs at high level			38	mA
			All outputs at low level			70	
			All outputs at high impedance			25	
I_{CC2}	Output supply current	I_O = 0	All outputs at high level			33	mA
			All outputs at low level			20	
			All outputs at high impedance			5	

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C.

switching characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

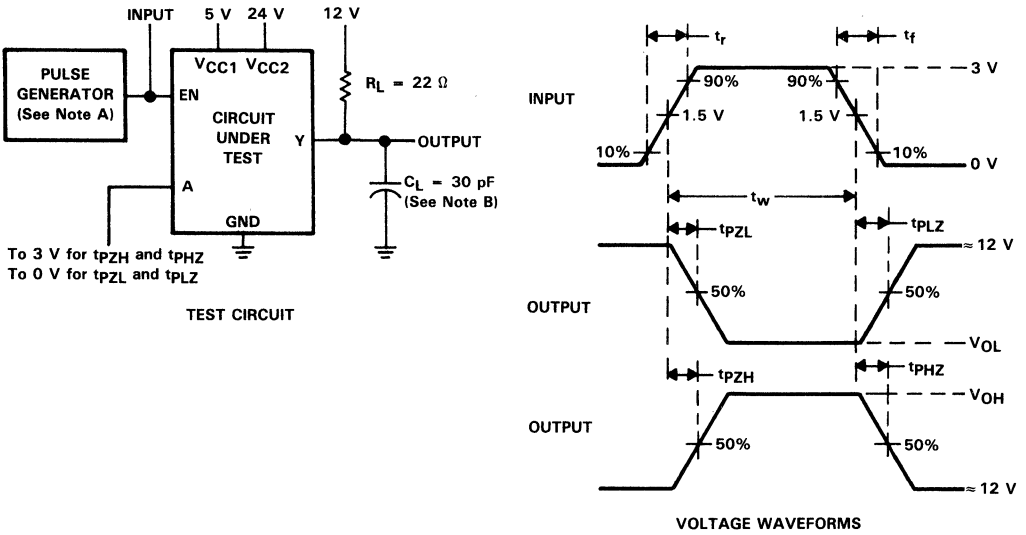
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output from A input	C_L = 30 pF, See Figure 1		800		ns
t_{DHL}	Delay time, high-to-low-level output from A input			400		ns
t_{TLH}	Transition time, low-to-high-level output			300		ns
t_{THL}	Transition time, high-to-low-level output			300		ns
t_{PZH}	Enable time to the high level	C_L = 30 pF, See Figure 2		700		ns
t_{PZL}	Enable time to the low level			400		ns
t_{PHZ}	Disable time from the high level			900		ns
t_{PLZ}	Disable time from the low level			600		ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 10\ \mu s$, PRR = 5 kHz, $Z_o = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES FROM DATA INPUTS



NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 10\ \mu s$, PRR = 5 kHz, $Z_o = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 2. SWITCHING TIMES FROM ENABLE INPUTS

APPLICATION INFORMATION

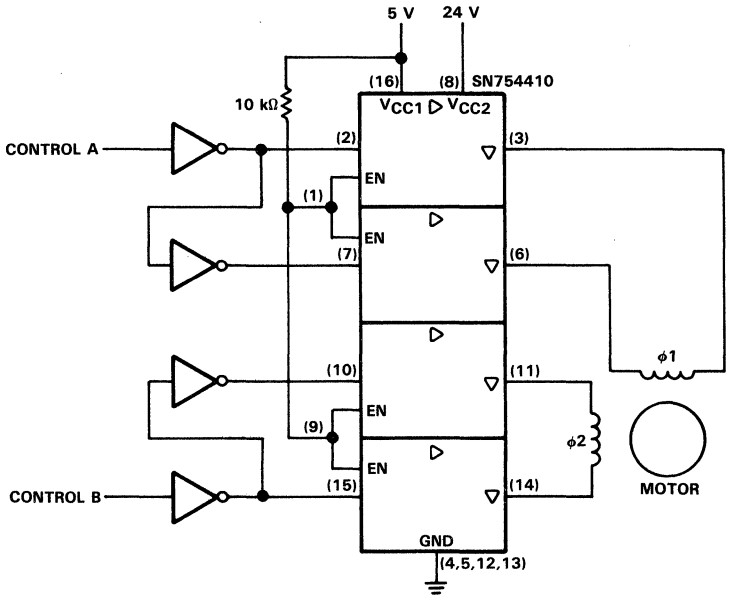
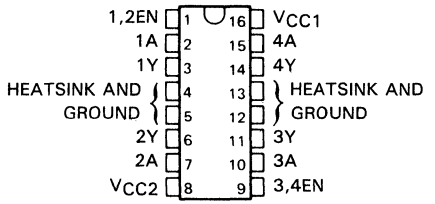


FIGURE 3. TWO-PHASE MOTOR DRIVER

D2942, NOVEMBER 1986—REVISED MAY 1990

- 1-A Output Current Capability Per Driver
- Applications Include Half-H and Full-H Solenoid Drivers and Motor Drivers
- Designed for Positive-Supply Applications
- Wide Supply Voltage Range: 4.5 V to 36 V
- TTL- and CMOS-Compatible High-Impedance Diode-Clamped Inputs
- Separate Input-Logic Supply
- Thermal Shutdown
- Internal ESD Protection
- Input Hysteresis Improves Noise Immunity
- Three-State Outputs
- Minimized Power Dissipation
- Sink/Source Interlock Circuitry Prevents Simultaneous Conduction
- No Output "Glitch" During Power-Up or Power-Down
- Improved Functional Replacement for the SGS L293

NE PACKAGE
(TOP VIEW)



FUNCTION TABLE
(EACH DRIVER)

INPUTS†		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

H = high-level
L = low-level
X = irrelevant
Z = high-impedance (off)
† In the thermal shutdown mode, the output is in the high-impedance state regardless of the input levels.

description

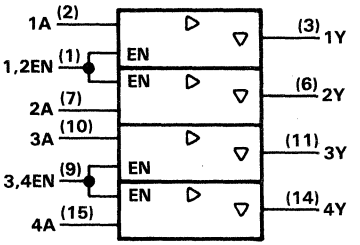
The SN754411 is a quadruple high-current half-H driver designed to provide bidirectional drive currents of up to one ampere at voltages from 4.5 V to 36 V. It is designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

All inputs are compatible with TTL and low-level CMOS logic. Each output (Y) is a complete totem-pole driver with a Darlington transistor sink and a psuedo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs become active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

External high-speed output clamp diodes should be used for inductive-transient suppression. A separate supply voltage (V_{CC1}) is provided for the logic input circuits to minimize device power dissipation. Supply voltage (V_{CC2}) is used for the output circuits.

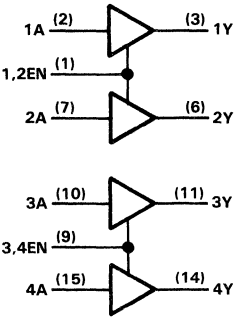
The SN754411 is designed for operation from −40°C to 85°C.

logic symbol†

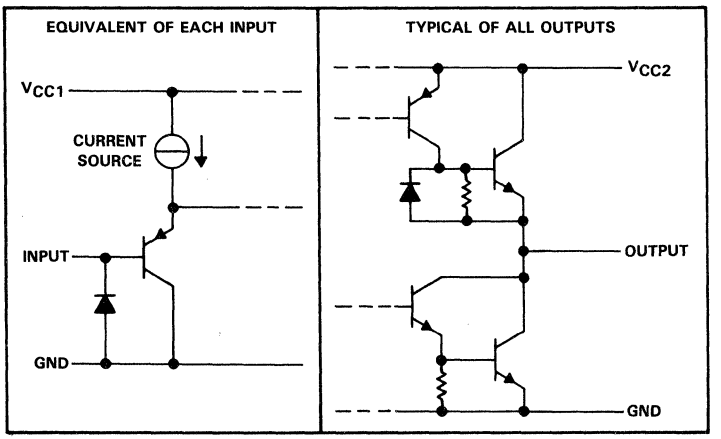


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage range, V_{CC1} (see Note 1) . . . . . −0.5 V to 36 V
Output supply voltage range, V_{CC2} . . . . . −0.5 V to 36 V
Input voltage . . . . . 36 V
Output voltage range, V_O . . . . . −3 V to V_{CC2} + 3 V
Peak output current (nonrepetitive, $t_w \leq 5$ ms), I_{PK} . . . . . ±2 A
Continuous output current, I_O . . . . . ±1.1 A
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 2075 mW
Operating free-air temperature range . . . . . −40°C to 85°C
Operating case or virtual junction temperature range . . . . . −40°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC1}	4.5	5.5	V
Output supply voltage, V_{CC2}	4.5	36	V
High-level input voltage, V_{IH}	2	5.5	V
Low-level input voltage, V_{IL}	−0.3†	0.8	V
Operating virtual junction temperature, T_J	−40	125	°C
Operating free-air temperature, T_A	−40	85	°C

† The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating virtual junction temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −12 mA			−0.9	−1.5	V
V_{OH}	High-level output voltage	I_{OH} = −0.5 A		V_{CC2}−1.5	V_{CC2}−1.1		V
		I_{OH} = −1 A		V_{CC2}−2			
		I_{OH} = −1 A, T_J = 25°C		V_{CC2}−1.8	V_{CC2}−1.4		
V_{OL}	Low-level output voltage	I_{OL} = 0.5 A			1	1.4	V
		I_{OL} = 1 A				2	
		I_{OL} = 1 A, T_J = 25°C			1.2	1.8	
I_{OZ}	Off-state (high-impedance state) output current	V_O = V_{CC2}				500	μA
		V_O = 0				−500	
I_{IH}	High-level input current	V_I = 5.5 V				10	μA
I_{IL}	Low-level input current	V_I = 0				−10	μA
I_{CC1}	Logic supply current	I_O = 0	All outputs at high level			38	mA
			All outputs at low level			70	
			All outputs at high impedance			25	
I_{CC2}	Output supply current	I_O = 0	All outputs at high level			33	mA
			All outputs at low level			20	
			All outputs at high impedance			5	

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C.

switching characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output from A input	C_L = 30 pF, See Figure 1		800		ns
t_{DHL}	Delay time, high-to-low-level output from A input			400		ns
t_{TLH}	Transition time, low-to-high-level output			300		ns
t_{THL}	Transition time, high-to-low-level output			300		ns
t_{PZH}	Enable time to the high level	C_L = 30 pF, See Figure 2		700		ns
t_{PZL}	Enable time to the low level			400		ns
t_{PHZ}	Disable time from the high level			900		ns
t_{PLZ}	Disable time from the low level			600		ns

TEXAS INSTRUMENTS
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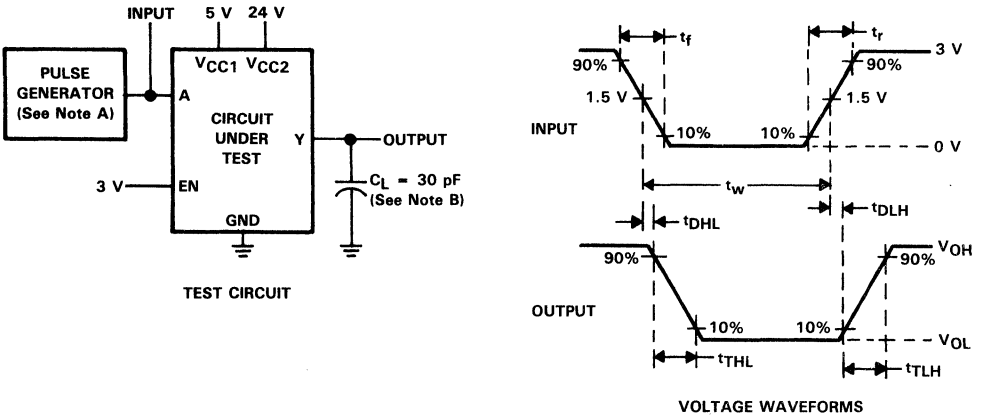
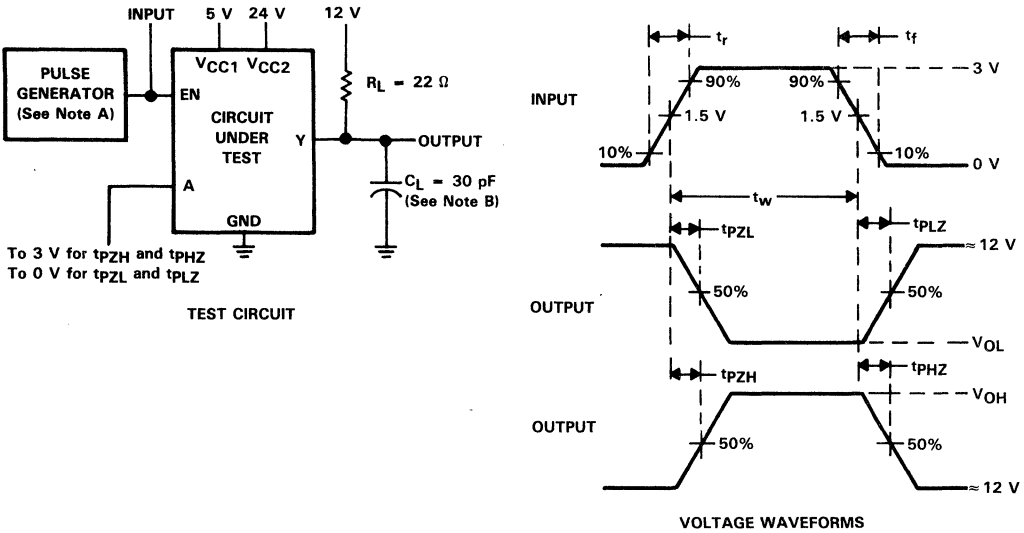
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 10\ \mu s$, PRR = 5 kHz, $Z_o = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES FROM DATA INPUTS



NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 10\ \mu s$, PRR = 5 kHz, $Z_o = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 2. SWITCHING TIMES FROM ENABLE INPUTS

APPLICATION INFORMATION

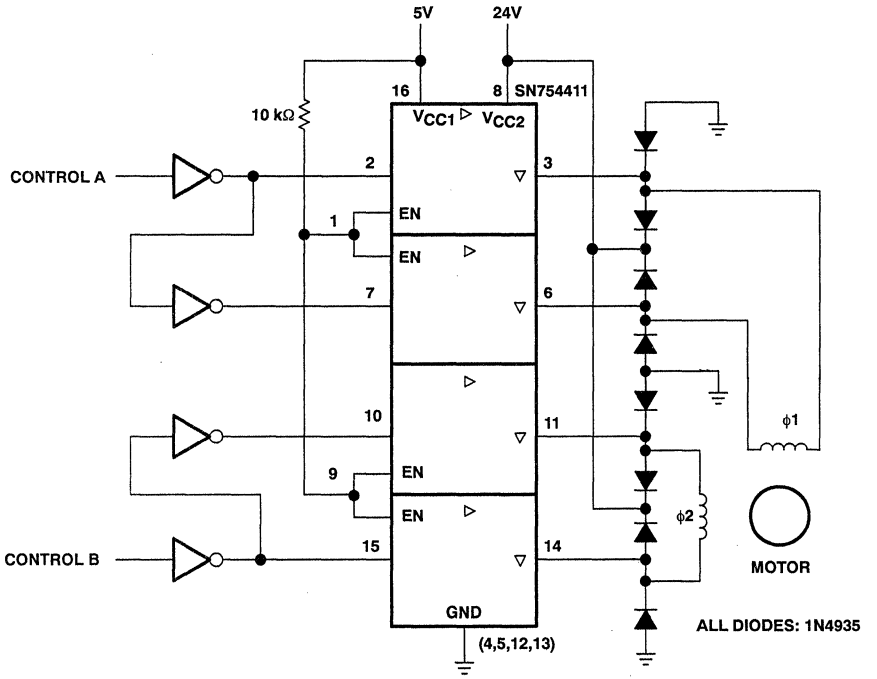
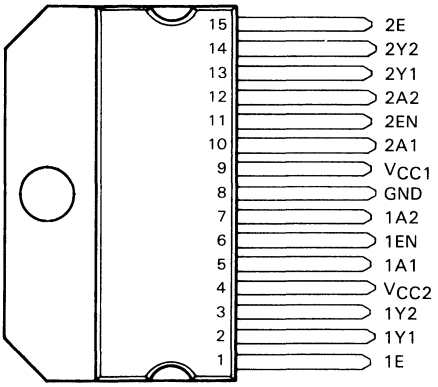


FIGURE 3. TWO-PHASE MOTOR DRIVER

D2942, JUNE 1987—REVISED JANUARY 1990

- **Formerly TLP298**
- **2-A Output Current Capability per Full-H Driver**
- **Applications Include Half-H and Full-H Solenoid Drivers and Motor Drivers**
- **Wide Range of Output Supply Voltage . . . 5 V to 46 V**
- **Separate Input-Logic Supply Voltage**
- **Thermal Shutdown**
- **Internal Electrostatic Discharge Protection**
- **High Noise Immunity**
- **Three-State Outputs**
- **Minimized Power Dissipation**
- **Sink/Source Interlock Circuitry Prevents Simultaneous Conduction**
- **Improved Functional Replacement for the SGS L298**

KV PACKAGE
(TOP VIEW)



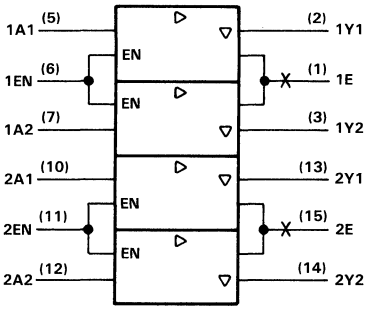
The tab is electrically connected to pin 8.

description

The TPIC0298 is a dual high-current full-H driver designed to provide bidirectional drive currents of up to two amperes at voltages from 5 V to 46 V. It is designed to drive inductive loads such as relays, solenoids, dc motors, stepping motors, and other high-current or high-voltage loads in positive-supply applications. All inputs are TTL compatible. Each output (Y) is a complete totem-pole drive with a Darlington transistor sink and a psuedo-Darlington source. Each full-H driver is enabled separately. Outputs 1Y1 and 1Y2 are enabled by 1EN and outputs 2Y1 and 2Y2 are enabled by 2EN. When an EN input is high, the associated channels are active. When an EN input is low, the associated channels are off (i.e., in the high-impedance state).

Each half of the device forms a full-H reversible driver suitable for solenoid or motor applications. The current in each full-H driver can be monitored by connecting a resistor between the sense output terminal 1E and ground and another resistor between sense output terminal 2E and ground.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(EACH CHANNEL)

INPUTS		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

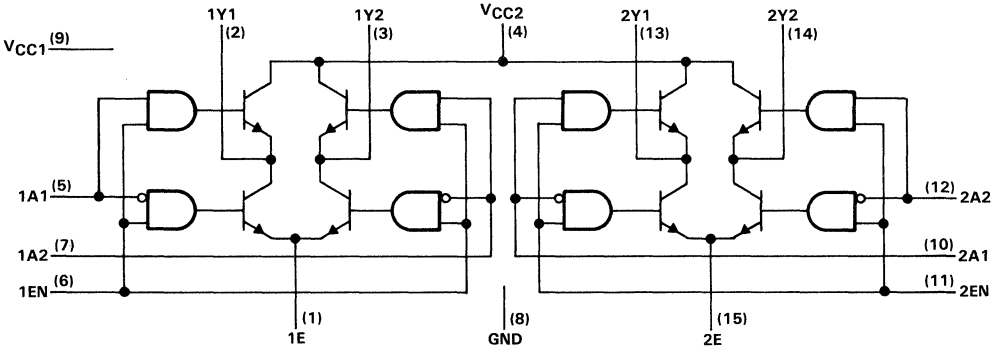
H = high-level
L = low-level
X = irrelevant
Z = high-impedance (off)

description (continued)

External high-speed output-clamp diodes should be used for inductive transient suppression. To minimize device power dissipation, a V_{CC1} supply voltage, separate from V_{CC2}, is provided for the logic inputs.

The TPIC0298 is designed for operation from 0°C to 70°C.

logic diagram (positive logic)



absolute maximum ratings over operating temperature range (unless otherwise noted)

Logic supply voltage range, V_{CC1}, (see Note 1) . . . . . −0.3 V to 7 V
Output supply voltage range, V_{CC2} . . . . . −0.3 V to 50 V
Input voltage range at A or EN, V_I (see Note 2) . . . . . −1.6 V to 7 V
Output voltage range, V_O . . . . . −2 V to V_{CC2}+2 V
Emitter terminal (1E and 2E) voltage range, V_E . . . . . −0.5 V to 2.3 V
Emitter terminal (1E and 2E) voltage (nonrepetitive, $t_w \leq 50\ \mu s$) . . . . . −1 V
Input current at A or EN, I_I . . . . . −15 mA
Peak output current, I_{OM}, (nonrepetitive, $t_w \leq 0.1$ ms) . . . . . ±3 A
(repetitive, $t_w \leq 10$ ms, duty cycle ≤ 80%) . . . . . ±2.5 A
Continuous output current, I_O . . . . . ±2 A
Peak combined output current for each full-H driver (see Note 3)
(nonrepetitive, $t_w \leq 0.1$ ms) . . . . . ±3 A
(repetitive, $t_w \leq 10$ ms, duty cycle ≤ 80%) . . . . . ±2.5 A
Continuous combined output current for each full-H driver (see Note 3) . . . . . ±2 A
Continuous dissipation at (or below) 25°C free-air temperature (see Note 4) . . . . . 3.575 W
Continuous dissipation at (or below) 75°C case temperature (see Note 4) . . . . . 25 W
Operating free-air, case, or virtual junction temperature range . . . . . −40°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal, unless otherwise noted.
2. The maximum current limitation at this terminal generally occurs at a voltage of lower magnitude than the voltage limit, Neither the maximum current nor the maximum voltage for this terminal should be exceeded.
3. Combined output current applies to each of the two full-H drivers individually. This current is the sum of the currents at outputs 1Y1 and 1Y2 for full-H driver 1 and the sum of the currents at outputs 2Y1 and 2Y2 for full-H driver 2. The full-H drivers may carry the rated combined current simultaneously.
4. For operation above 25°C free-air temperature, derate linearly at the rate of 28.6 mW/°C. For operation above 75°C case temperature, derate linearly at the rate of 333 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	MAX	UNIT
Logic supply voltage, V_{CC1}		4.5	7	V
Output supply voltage, V_{CC2}		5	46	V
Emitter terminal (1E or 2E) voltage, V_E (see Note 5)		−0.5†	2	V
			$V_{CC1}-3.5$	
			$V_{CC2}-4$	
High-level input voltage, V_{IH} (see Note 5)	A	2.3	V_{CC1}	V
			$V_{CC2}-2.5$	
	EN	2.3	7	
			V_{CC1}	
Low-level input voltage at A or EN, V_{IL}		−0.3†	1.5	V
Output current, I_O			±2	A
Commutation frequency, f_c			40	kHz
Operating free-air temperature, T_A		0	70	°C

† The algebraic convention, in which the least positive (most negative) designated minimum, is used in this data sheet for emitter terminal voltage and logic voltage levels.

NOTE 5: For optimum device performance, the maximum recommended voltage at any A input is 2.5 V lower than V_{CC2}, the maximum recommended voltage at any EN input is V_{CC1}, and the maximum recommended voltage at any emitter terminal is 3.5 V lower than V_{CC1} and 4 V lower than V_{CC2}.

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and V_E, T_J = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA				−0.9	−1.5	V
V_{OH}	High-level output voltage		I_{OH} = −1 A			V_{CC2}−1.8	V_{CC2}−1.2		V
			I_{OH} = −2 A			V_{CC2}−2.8	V_{CC2}−1.8		
V_{OL}	Low-level output voltage		I_{OL} = 1 A				V_E+1.2	V_E+1.8	V
			I_{OL} = 2 A				V_E+1.7	V_E+2.6	
V_{drop}	Total source plus sink output voltage drop		I_{OH} = −1 A, I_{OL} = 1 A	See Note 6			2.4	3.4	V
			I_{OH} = −2 A, I_{OL} = 2 A				3.5	5.2	
I_{OZH}	Off-state (high-impedance state) output current, high-level voltage applied		V_O = V_{CC2}					500	μA
I_{OZL}	Off-state (high-impedance state) output current, low-level voltage applied		V_O = 0 V, V_E = 0 V					−500	μA
I_{IH}	High-level input current	A	V_I = V_{IH}	EN = H			20	100	μA
				EN = L				10	
		EN	V_I = V_{IH} ≤ V_{CC1}−0.6 V				6	100	
I_{IL}	Low-level input current		V_I = 0 V to 1.5 V					−10	μA
I_{CC1}	Logic supply current		I_O = 0	All outputs at high level			7	12	mA
				All outputs at low level			20	32	
				All outputs at high impedance			4	6	
I_{CC2}	Output supply current		I_O = 0	All outputs at high level			25	50	mA
				All outputs at low level			6	20	
				All outputs at high impedance				2	

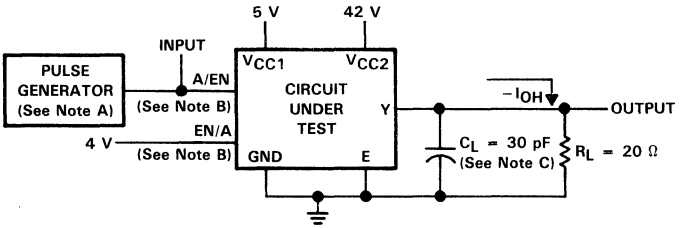
† All typical values are at V_{CC1} = 5 V, V_{CC2} = 42 V, V_E = 0 V, T_J = 25°C (unless otherwise noted).

NOTE 6: The V_{drop} specification applies for I_{OH} and I_{OL} applied simultaneously to different output channels.
V_{drop} = V_{CC2} − V_{OH} + V_{OL} − V_E.

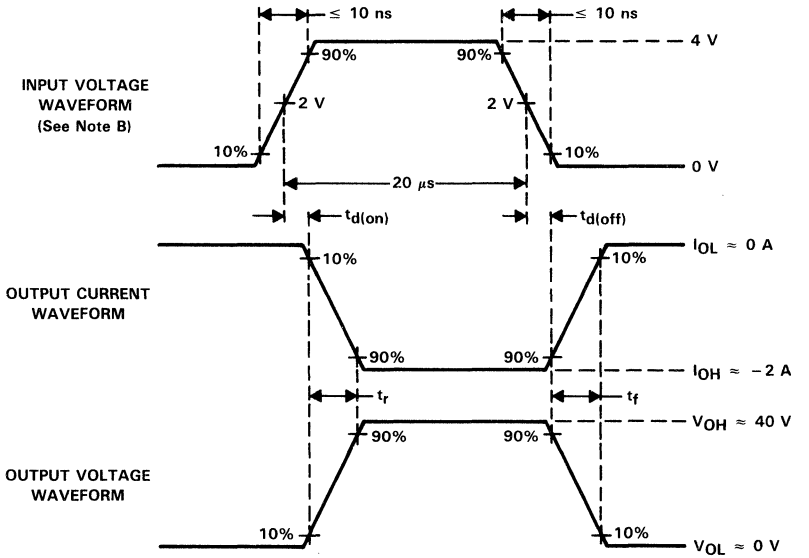
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 42 V, V_E = 0, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Source current turn-on delay time from A input	C_L = 30 pF, See Figure 1		0.6		μs
$t_{d(off)}$	Source current turn-off delay time from A input			0.8		μs
t_r	Source current rise time (turning on)			0.8		μs
t_f	Source current fall time (turning off)			0.2		μs
$t_{d(on)}$	Source current turn-on delay time from EN input			0.5		μs
$t_{d(off)}$	Source current turn-off delay time from EN input			2.5		μs
$t_{d(on)}$	Sink current turn-on delay time from A input	C_L = 30 pF, See Figure 2		1.3		μs
$t_{d(off)}$	Sink current turn-off delay time from A input			0.5		μs
t_r	Sink current rise time (turning on)			0.2		μs
t_f	Sink current fall time (turning off)			0.2		μs
$t_{d(on)}$	Sink current turn-on delay time from EN input			0.3		μs
$t_{d(off)}$	Sink current turn-off delay time from EN input			1		μs

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

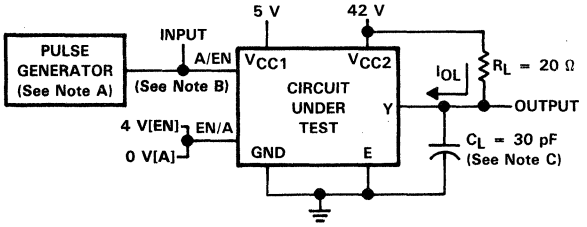


VOLTAGE AND CURRENT WAVEFORMS

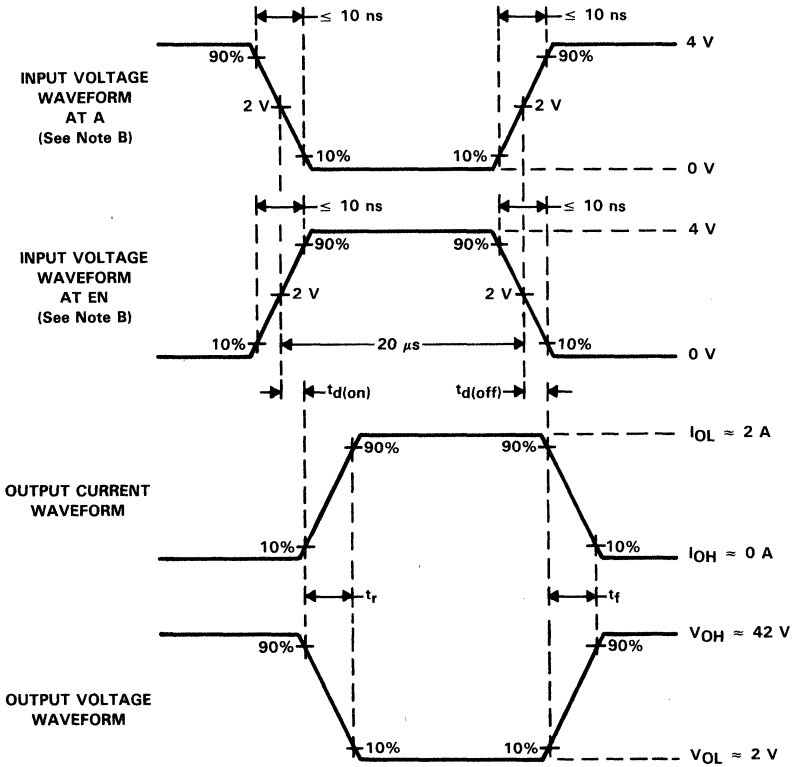
NOTES: A. The pulse generator has the following characteristics: PRR = 2 kHz, Z_O = 50 Ω.
B. EN is at 4 V if A is used as the switching input. A is at 4 V if EN is the switching input.
C. C_L includes probe and jig capacitance.

FIGURE 1. SOURCE CURRENT SWITCHING TIMES FROM DATA AND ENABLE INPUTS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 2 kHz, Z_O = 50 Ω.
B. EN is at 4 V if A is used as the switching input. A is at 0 V if EN is the switching input.
C. C_L includes probe and jig capacitance.

FIGURE 2. SINK CURRENT SWITCHING TIMES FROM DATA AND ENABLE INPUTS

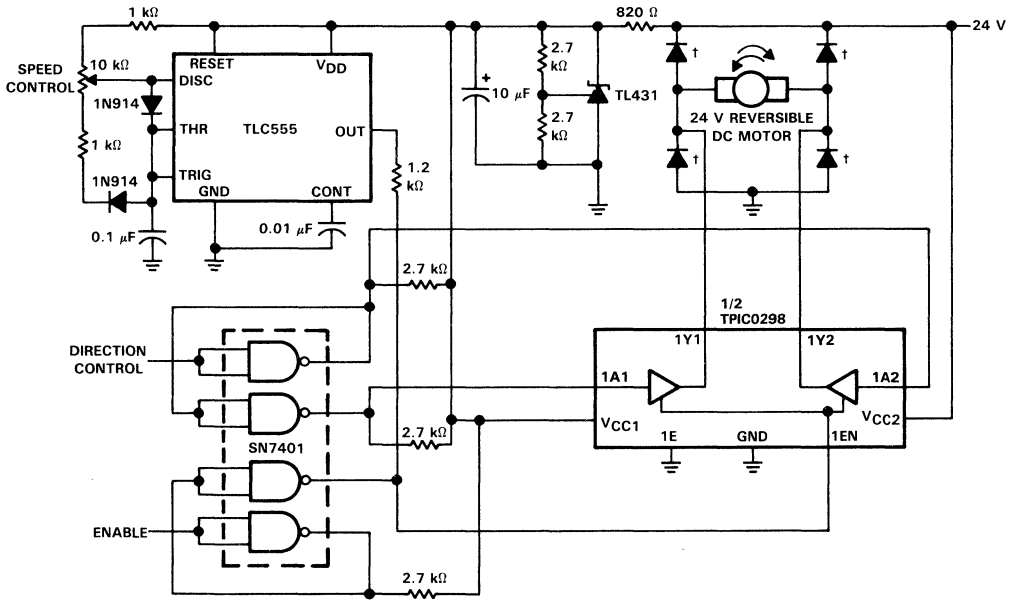
TYPICAL APPLICATION DATA

This circuit shows one half of a TPIC0298 used to provide full-H bridge drive for a 24-V 2-A dc motor. Speed control is achieved with a TLC555 timer. This provides variable duty cycle pulses to the EN input of the TPIC0298. In this configuration, the operating frequency is approximately 1.2 kHz. The duty cycle is adjustable from 10% to 90% to provide a wide range of motor speeds. The motor direction is determined by the logic level at the direction control input. The circuit may be enabled or disabled by the logic level at the EN input. A 5-V supply for the logic and timer circuit is provided by a TL431 short regulator. For circuit operation, refer to the function table.

FUNCTION TABLE

ENABLE	DIRECTION CONTROL	1Y1	1Y2
H	H	source	sink
H	L	sink	source
L	X	disabled	disabled

X = don't care H = high level L = low level



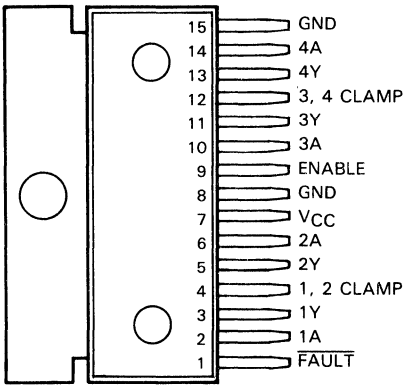
†Diodes are 1N4934 or equivalent.

FIGURE 3. TPIC0298 AS BIDIRECTIONAL DC MOTOR DRIVER

D3299, AUGUST 1989 – REVISED NOVEMBER 1989

- **1-A Current Capability Per Channel**
- **45-V Inductive Switching Voltage Capability**
- **Current Sink Inputs Compatible with TTL or CMOS Devices**
- **Output Clamp Diodes for Inductive Transient Protection**
- **Independent Thermal Shutdown Protection**
- **Overvoltage Shutdown Protection**
- **Independent Channel Current Limit**
- **Error Sensing**
- **Extended Temperature Range of −40°C to 125°C**

KN SINGLE-IN-LINE PACKAGE
(TOP VIEW)



The tab is electrically connected to the GND pins.

description

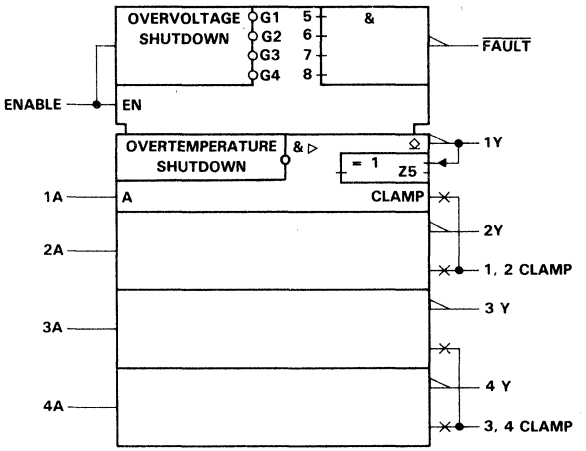
The TPIC2404 is a monolithic high-voltage high-current quadruple low-side switch especially designed for driving from low-level logic to peripheral loads such as relays, solenoids, motors, lamps, and other high-voltage high-current loads. The high-efficiency power switch is optimized for applications where a very rugged power switch is required. The device will tolerate power supply transients and reverse battery conditions up to 13 V.

The TPIC2404 features four inverting open-collector outputs controlled by a common-enable input. When ENABLE is low, the outputs are disabled. An error sensing circuit monitors load and device faults. When an error is sensed, the $\overline{\text{FAULT}}$ output goes to a low state. In addition, the device features on-board V_{CC} overvoltage and thermal overload protection circuits, and the outputs are current-limit protected.

FUNCTION TABLE

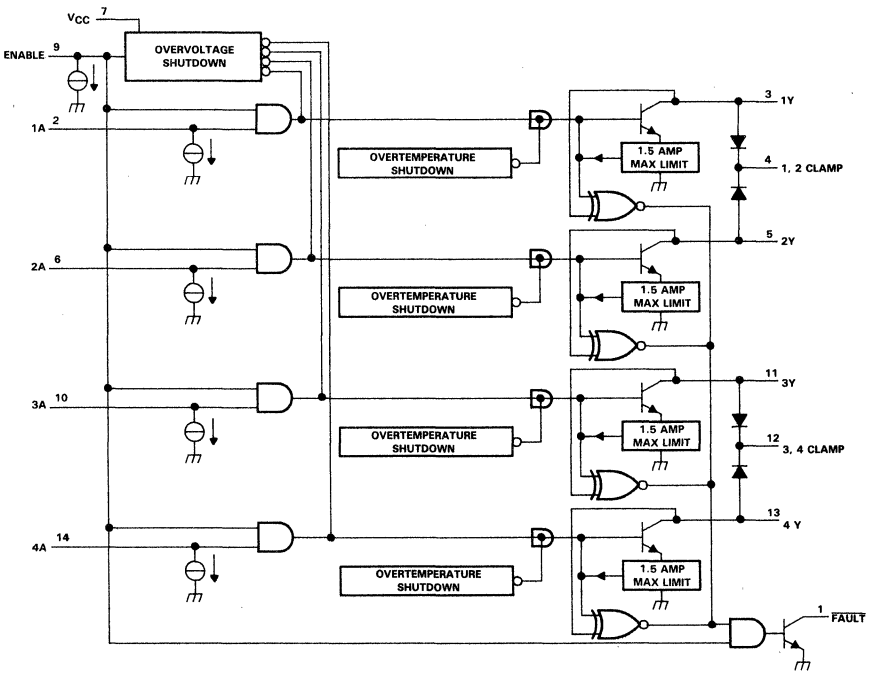
	ENABLE	A	Y	$\overline{\text{FAULT}}$
Normal operation	H H L	H L X	L H H	H H H
Open load	H	L	L	L
Short to GND				
Overvoltage shutdown	H	X	H	L
Thermal shutdown				
Short to V_{CC}	H	H	H	L

logic symbol†



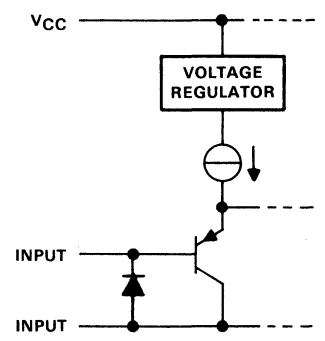
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

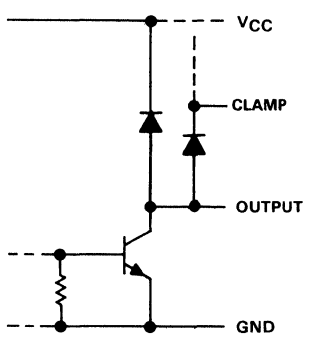


schematics of inputs and outputs

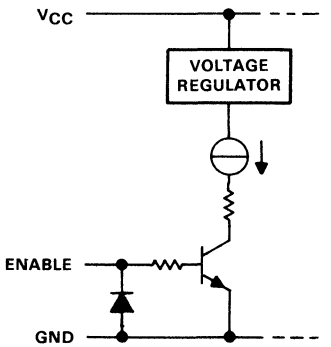
EQUIVALENT OF EACH A INPUT



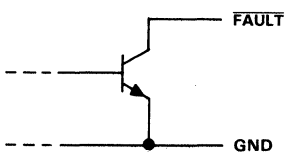
EQUIVALENT OF EACH Y OUTPUT



EQUIVALENT OF ENABLE INPUT



EQUIVALENT OF $\overline{\text{FAULT}}$ OUTPUT



absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . −13 V to 24 V
Input voltage range, V_I . . . . . −0.6 V to 7 V
Output voltage range, V_O . . . . . −0.6 V to 45 V
Output sustaining voltage, $V_{O(sust)}$ . . . . . 45 V
Continuous output sink current (repetitive, t_w < 8 ms), I_{OL} (see Note 2) . . . . . 1.5 A
Output clamp-diode voltage, V_{OK} . . . . . 45 V
Continuous total dissipation at (or below) 25°C case temperature (see Note 3) . . . . . 50 W
Operating case or virtual junction temperature range . . . . . −55°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 s . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. Output sink current is limited by the overcurrent limit.
3. For operation above 25°C free-air or case temperature refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below rated dissipation.

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

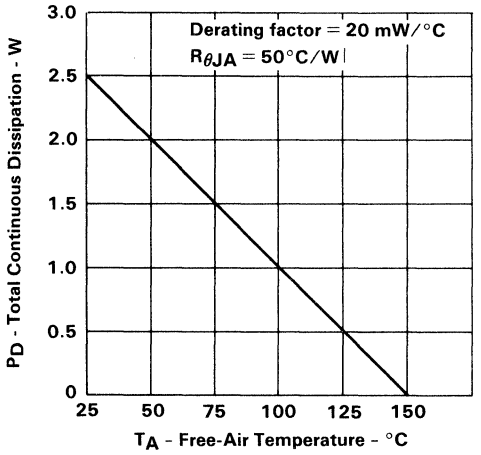


FIGURE 1

CASE TEMPERATURE
DISSIPATION DERATING CURVE

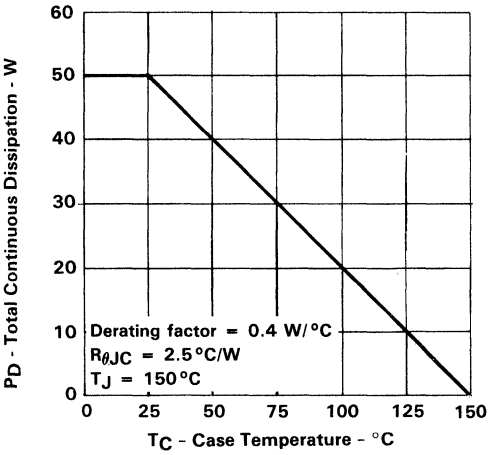


FIGURE 2

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	9	12	16	V
High-level input voltage, V_{IH}	2		5.5	V
Low-level input voltage, V_{IL}	−0.3†		0.8	V
Peak output voltage from external inductive kickback			45	V
Continuous output sink current			1	A
Fault output sink current			75	μA
Operating free-air temperature, T_A	−40		125	°C

† The algebraic convention in which the least positive (most negative) value is designated minimum is used in this data sheet for logic voltage levels.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltages (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$I_{O(off)}$	Off-state output current		V_O = 12 V, ENABLE low		15	100	μA
			V_O = 45 V, ENABLE high		0.6	2	mA
			V_O = 12 V, ENABLE high	200	400	600	μA
I_{IL}	Low-level input current		V_I = 0 to 0.8 V	−10	25	40	μA
I_{IH}	High-level input current	A inputs		10	25	60	μA
		ENABLE			0.2	1	mA
V_{OL}	Low-level output voltage		I_{OL} = 100 mA		0.1	0.15	V
			I_{OL} = 500 mA		0.3	0.55	
			I_{OL} = 1 A		0.8	1.3	
			$\overline{FAULT}$ output, I_{OL} = 30 μA		0.2	0.4	
I_{OL}	Low-level output current		$\overline{FAULT}$ output, V_{OL} = 1 V to 5.5 V	50	90	125	μA
$I_{R(K)}$	Clamp diode reverse current		V_r = 50 V, V_O = 0			100	μA
$V_{F(K)}$	Clamp diode forward voltage		I_f = 1 A			2	V
			I_f = 1.5 A			2.5	
I_{CC}	Supply current		Outputs off, ENABLE low			0.25	mA
			Outputs on, T_A = −40°C			120	
			Outputs on, T_A = 25° C to 125°C			100	

operating characteristics over recommended operating free-air temperature and supply voltages (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
High-level output sense voltage threshold				7	V
Low-level output sense voltage threshold		3			V
Overcurrent limiting	T_A = −40°C			1.85	A
	T_A = 25°C to 125°C		1.2	1.5	
V_{CC} Overvoltage shutdown		25.5		31	V
V_{hys} Overvoltages shutdown hysteresis			0.25		V
Thermal shutdown			155		°C
Thermal shutdown hysteresis			15		°C
Turn-on time			8		μs
Turn-off time			8		μs

‡ All typical values are at V_{CC} = 12 V, T_A = 25 °C.

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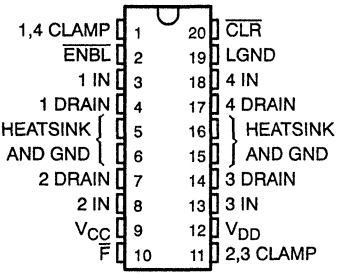
- **Output Voltage up to 60 V**
- **4 Output Channels of 700-mA Nominal Current Per Channel**
- **Pulsed Current 3 A Per Channel**
- **Low $r_{DS(on)}$ . . . 0.5 Ω Typ**
- **Avalanche Energy . . . 50 mJ**
- **Thermal Shutdown Protection with Fault (Overtemperature) Output**
- **NE Package Designed for Heat Sinking**
- **Integral Output Clamp Diodes**
- **Input Transparent Latches for Data Storage**
- **Asynchronous Clear to Turn Off All Outputs**
- **Output Parallel Capability for Increased Current Drive up to 12-A Total Pulsed Load Current**

NE PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each channel)

FUNCTION	INPUTS			OUTPUT	FAULT
	$\overline{ENBL}$	$\overline{CLR}$	IN	Y	$\overline{F}$
NORMAL OPERATION	X	L	X	H	H
	L	H	L	H	H
	L	H	H	L	H
	H	H	X	Q_0	H
THERMAL SHUTDOWN	X	X	X	H	L

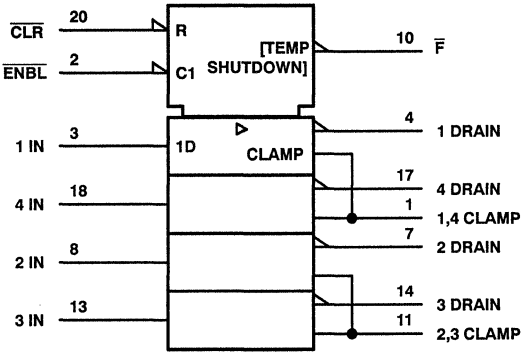
H = high-level, L = low-level, X = irrelevant

description

The TPIC2406 is a monolithic, high-voltage, high-current, quadruple power driver designed for use in systems that require high load power. The device contains built-in high-speed output clamp diodes for inductive transient protection. Power driver applications include lamps, relays, solenoids, and dc stepping motors.

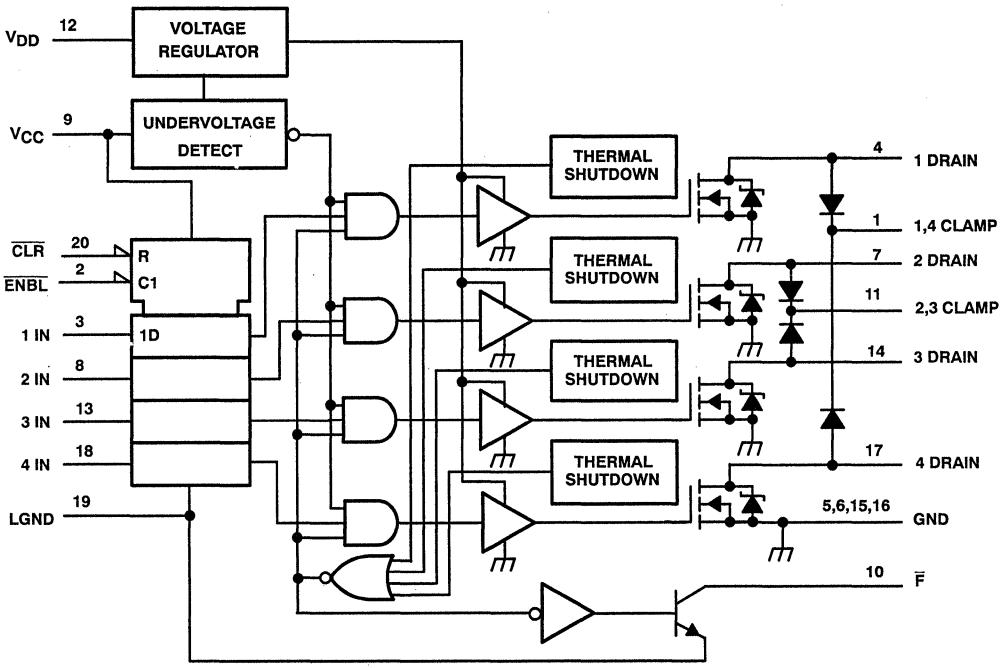
Each device features four inverting open-drain outputs each controlled by an input storage latch with common clear and enable controls. All inputs accept standard TTL- and CMOS-logic levels. The $\overline{CLR}$ function is asynchronous and turns all four outputs off regardless of data inputs. Taking $\overline{ENBL}$ low puts the input latch into a transparent mode, allowing the data inputs to affect the output. In this state, all four outputs will be held off while $\overline{CLR}$ is low, but will return to the stages on the data inputs when $\overline{CLR}$ goes high. When $\overline{ENBL}$ is taken high, the latch is put into a storage mode and the last state of the data inputs is held in the latches. If the $\overline{CLR}$ input is taken low, the data in the latches is cleared, turning all outputs off. If $\overline{CLR}$ is taken high again, $\overline{ENBL}$ must be cycled low to read new data into the latch.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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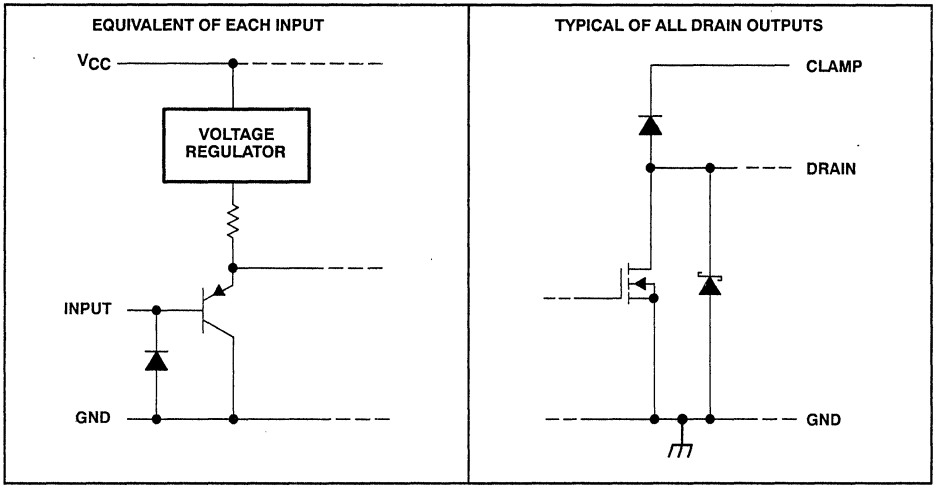
schematics of inputs and outputs



absolute maximum ratings over – 40°C to 125°C case temperature range (unless otherwise noted)

Logic supply voltage, V_{CC} (see Note 1) ..... 7 V
Power MOSFET driver supply voltage, V_{DD} ..... 60 V
Logic input voltage, V_I ..... 7 V
Power MOSFET drain-source voltage, V_{DS} ..... 60 V
$\overline{F}$ output voltage ..... 7 V
Clamp diode voltage ..... 60 V
Continuous source-drain diode anode current ..... 1.25 A
Pulsed source-drain diode anode current ..... 6 A
Pulsed drain current, each output, all outputs on, $I_{D1} = I_{D2} = I_{D3} = I_{D4}$,
$T_A = 25°C$ (see Note 2 and Figures 5 through 8) ..... 3 A
Continuous drain current, each output, all outputs on, $I_{D1} = I_{D2} = I_{D3} = I_{D4}$, $T_A = 25°C$ ..... 770 mA
Peak drain current, single output, I_{DM}, $T_A = 25°C$ (see Note 3) ..... 12.5 A
Single-pulse avalanche energy, E_{AS} ..... 50 mJ
Continuous total dissipation at or below 25°C free-air temperature (see Note 4) ..... 2.5 W
Continuous total dissipation at or below 100°C case temperature (see Note 4) ..... 6 W
Operating junction temperature range, T_J ..... – 40°C to 150°C
Storage temperature range ..... – 40°C to 150°C
Lead temperature ..... 260°C

NOTES: 1. All voltage values are with respect to the five ground (GND and LGND) terminals connected together.
2. Pulse duration = 10 ms, duty cycle = 6%.
3. Pulse duration ≤ 100 μs, duty cycle ≤ 2%.
4. For operation above 25°C free-air temperature, derate linearly at the rate of 20 mW/°C. For operation above 100°C case temperature, derate linearly at the rate of 120 mW/°C. To avoid exceeding the design maximum junction temperature, these ratings should not be exceeded. Due to variations in individual devices, electrical characteristics, and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Logic supply voltage, V_{CC}		4.5		5.5	V
Output supply voltage, V_{DD}		10		35	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.6	V
Setup time, t_{su}, data before $\overline{ENBL}$ ↑ (see Figure 1)		100			ns
Hold time, t_h, data after $\overline{ENBL}$ ↑ (see Figure 1)		100			ns
Pulse duration, t_w (see Figure 1)	$\overline{ENBL}$ low	300			ns
	$\overline{CLR}$ low				
Operating case temperature, T_C		−40		125	°C

electrical characteristics, V_{CC} = 5 V, V_{DD} = 14 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA		60			V
$V_{F(K)}$	Clamp diode forward voltage	I_F = 1.25 A,	See Notes 5 and 6			1.6	V
V_{SD}	Source-drain diode forward voltage	I_S = 1.25 A,	See Notes 5 and 6			1.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OL}	$\overline{F}$ low-level output voltage	I_{OL} = 4 mA			0.4		V
I_{IH}	High-level input current	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_I = 0.4 V			0.1	mA
I_{CC}	Logic supply current	I_O = 0,	All outputs off			10	mA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, T_C = 85°C,	$I_N = I_D$, See Notes 5, 6, and 7		700		mA
I_{DD}	Output supply current	I_O = 0,	All outputs off			6	mA
$I_{R(K)}$	Clamp-diode reverse current	V_{DS} = 55 V,	V_O = 0			1	μA
		V_{DS} = 55 V,	V_O = 0, T_C = 125°C			10	
I_{DSX}	Off-state drain current	V_R = 55 V				1	μA
		V_R = 55 V,	T_C = 125°C			10	
$I_{O(\overline{F})}$	High-level fault leakage current	V_{OH} = 5.5 V				1	μA
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 1.25 A	See Notes 5 and 6		0.5	0.6	Ω
		I_D = 1.25 A, T_C = 125°C			0.8	1	
		I_D = 3 A			0.55	0.65	

NOTES: 5. Technique should limit $T_j - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at 85°C at case temperature.

switching characteristics, V_{CC} = 5 V, V_{DD} = 24 V, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level drain output from clock	C_L = 30 pF,	See Figure 1		450		ns
t_{PHL}	Propagation delay time, high-to-low-level drain output from clock				550		ns
t_{TLH}	Transition time, low-to-high-level of source-drain output				35		ns
t_{THL}	Transition time, high-to-low-level of source-drain output				30		ns
t_{DLH}	Delay time, low-to-high-level drain output from input	C_L = 30 pF, $I_D = I_N$ = 700 mA	See Figure 2,		380		ns
t_{DHL}	Delay time, high-to-low-level drain output from input				380		ns
t_{RLH}	Rise time, low-to-high-level of source-drain output				35		ns
t_{FHL}	Fall time, high-to-low-level of source-drain output				70		ns
t_a	Reverse-recovery-current rise time	I_F = 3 A, See Notes 5 and 6,	di/dt = 100 A/μs, See Figure 3		45		ns

NOTES: 5. Technique should limit $T_j - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

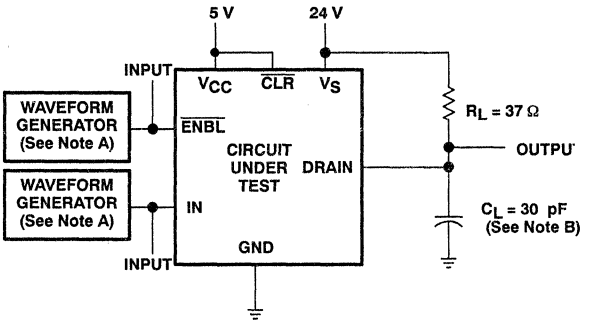
thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance	All four outputs with equal power			8.33	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance				50	°C/W

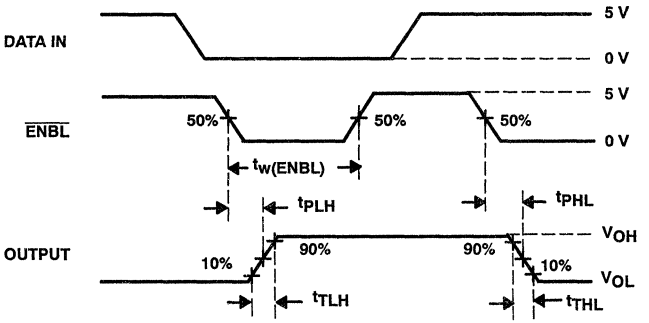
operating characteristics over – 40°C to 125°C case temperature range

PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Undervoltage shutdown	3		4.5	V
	Thermal shutdown temperature		155		°C
	Thermal shutdown hysteresis		15		°C

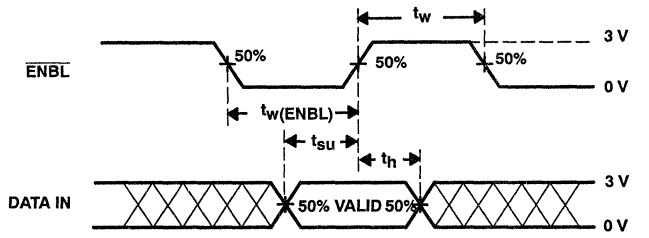
PARAMETER MEASUREMENT INFORMATION



(a) TEST CIRCUIT



(b) SWITCHING TIMES FROM ENABLE INPUT

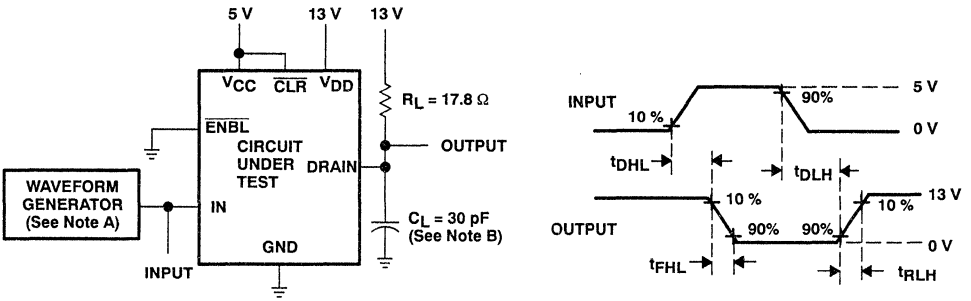


(c) INPUT SETUP AND HOLD WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, PRR = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_w = 5$ ms, PRR = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 2. SWITCHING TIMES

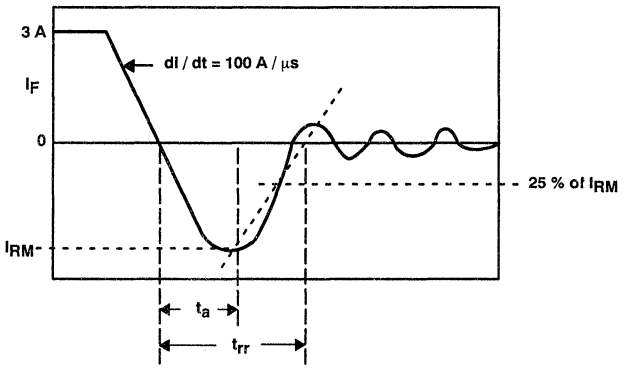
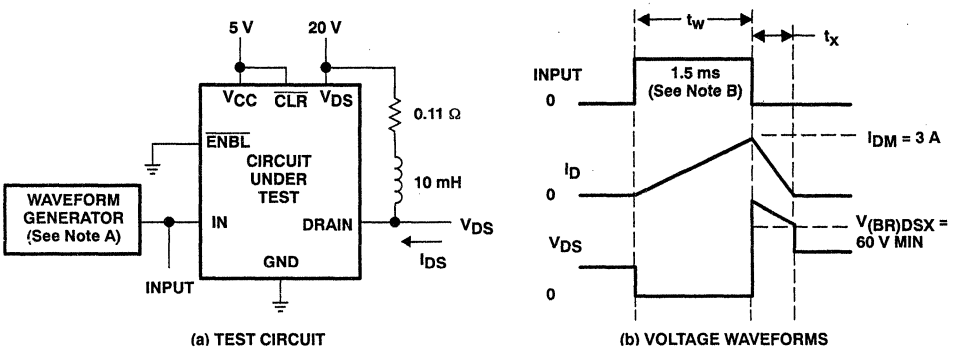


FIGURE 3. REVERSE-RECOVERY-CURRENT WAVEFORMS OF SOURCE-DRAIN DIODE

PARAMETER MEASUREMENT INFORMATION



(a) TEST CIRCUIT

(b) VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 1$ ms, PRR = 5 kHz, $Z_O = 50\ \Omega$.

B. Input pulse duration is increased until peak current $I_{DM} = 3$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{DM} \times V_{(BR)DSX} \times t_x}{2} = 50$ mJ min.

FIGURE 4. SINGLE-PULSE AVALANCHE ENERGY TEST CIRCUIT AND WAVEFORMS

MAXIMUM RATINGS

MAXIMUM DRAIN CURRENT
vs
DUTY CYCLE

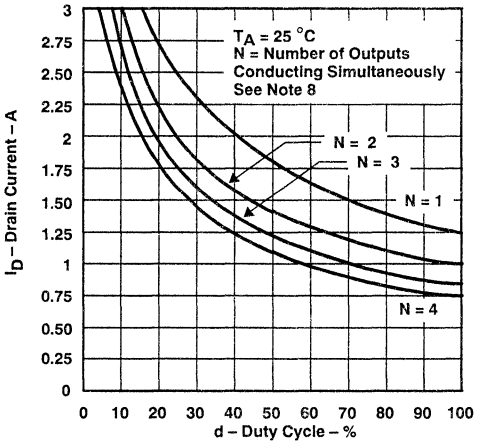


FIGURE 5

MAXIMUM DRAIN CURRENT
vs
DUTY CYCLE

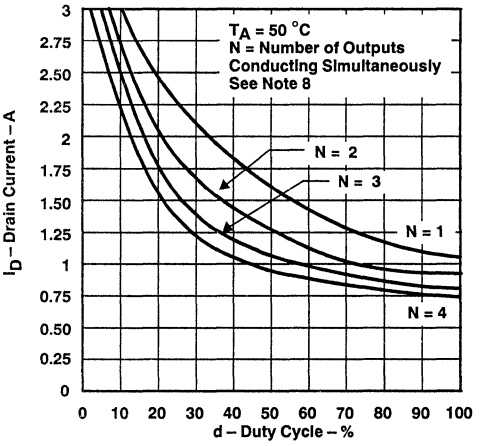


FIGURE 6

MAXIMUM DRAIN CURRENT
vs
DUTY CYCLE

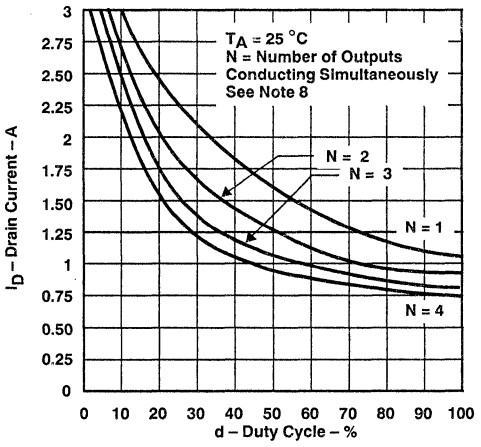


FIGURE 7

MAXIMUM DRAIN CURRENT
vs
PULSE DURATION

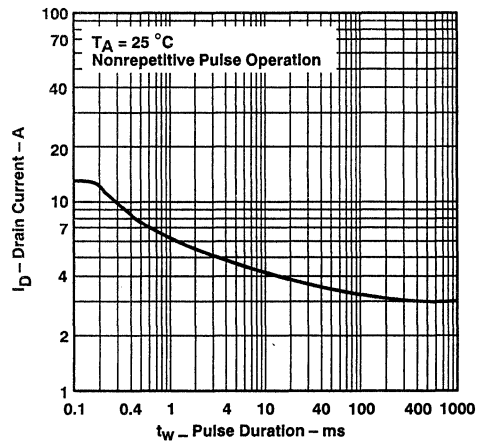
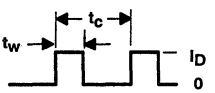


FIGURE 8

NOTE 8: For Figures 5, 6, and 7, $d = \frac{t_W}{t_C} = \frac{10\ ms}{t_C}$. Where t_W and t_C are defined by the following:



MAXIMUM RATINGS

MAXIMUM CONTINUOUS
DRAIN CURRENT
vs
FREE-AIR TEMPERATURE

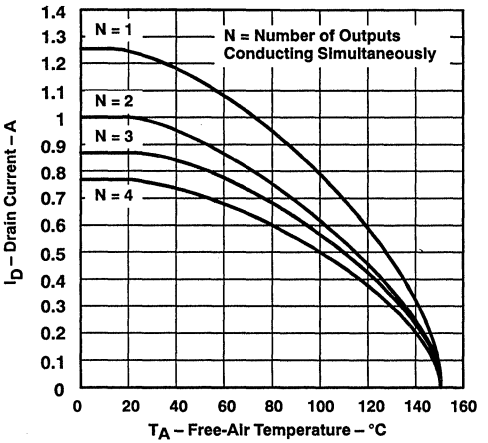


FIGURE 9

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

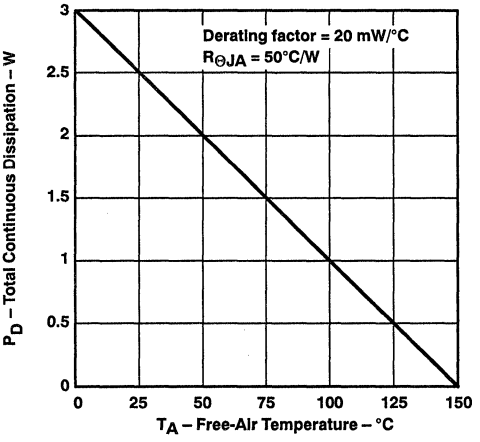


FIGURE 10

TRANSIENT THERMAL IMPEDANCE
vs
ON TIME

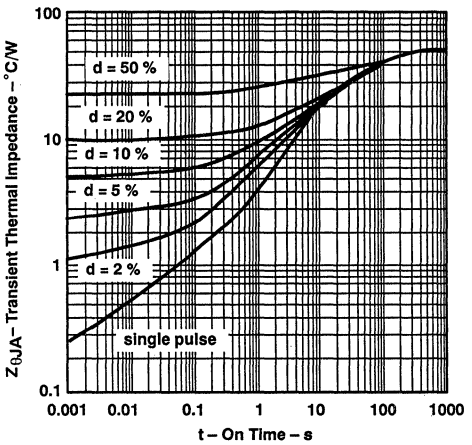


FIGURE 11

The single-pulse curve in Figure 11 represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta JA} = \left| \frac{t_w}{t_c} \right| R_{\theta JA} + \left| 1 - \frac{t_w}{t_c} \right| Z_{\theta(t_w + t_c)} + Z_{\theta(t_w)} - Z_{\theta(t_c)}$$

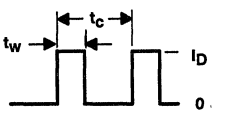
Where:

$Z_{\theta(t_w)}$ = the single-pulse thermal impedance for t = t_w seconds

$Z_{\theta(t_c)}$ = the single-pulse thermal impedance for t = t_c seconds

$Z_{\theta(t_w + t_c)}$ = the single-pulse thermal impedance for t = $t_w + t_c$ seconds

d = t_w/t_c



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TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-RESISTANCE vs DRAIN CURRENT

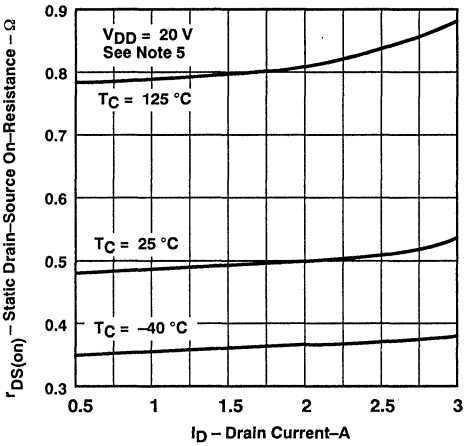


FIGURE 12

STATIC DRAIN-SOURCE ON-RESISTANCE vs POWER MOSFET DRIVER SUPPLY VOLTAGE

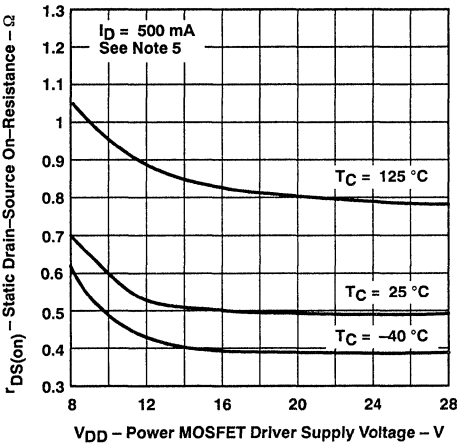


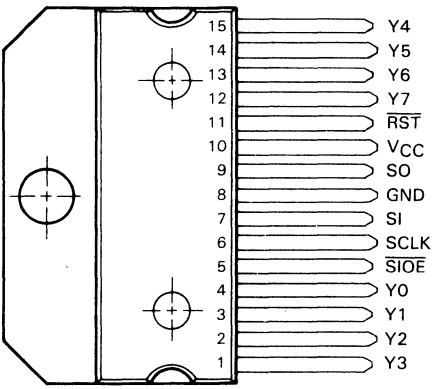
FIGURE 13

NOTE 5: Technique should limit $T_j - T_C$ to 10°C maximum.

D3282, AUGUST 1989 – REVISED JUNE 1990

- **8-Bit Serial-In Parallel-Out Driver**
- **1-A Output Current Capability per Channel or 8-A Total Current**
- **Over-Current Limiting and Out-of-Saturation Voltage Protection on Driver Outputs**
- **Contains Eight Open-Collector Saturating Sink Outputs with Low On-State Voltage**
- **High-Impedance Inputs with Hysteresis are Compatible with TTL or CMOS Levels**
- **Very Low Standby Power . . . 20 mW Typical**
- **Status of Output Drivers May Be Monitored at Serial Output**
- **3-State Serial Output Permits Serial Cascading or Wire-AND Device Connections**
- **25-V Transient Clamping with Inductive Switching on Outputs, 40-mJ Rating per Driver Output**

KV PLASTIC PACKAGE
(TOP VIEW)



The tab is electrically connected to pin 8.

description

The TPIC2801 is a monolithic BIDFET† integrated circuit that is designed to sink currents up to 1 A at 30 V simultaneously at each of eight driver outputs under serial input data control. Status of the individual driver outputs is available in serial data format. The driver outputs have overcurrent limiting and out-of-saturation voltage protection features. Applications include driving solenoids, relays, dc motors, lamps, and other medium-current or high-voltage loads.

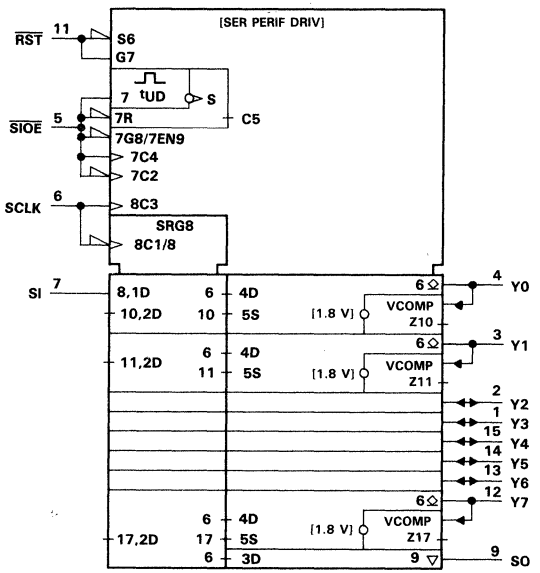
The device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit parallel latch, which independently controls each of the eight Y-output drivers.

Data is entered into the device serially via the serial input (SI) and goes directly into the lowest bit (0) of the shift register. Using proper timing signals, the input data is passed to the corresponding output latch and output driver. A logic high bit at SI_n turns the corresponding output driver (Y_n) off. A logic low bit at SI turns the corresponding output driver on. Serial data is transferred into SI on the high-to-low transition of serial clock (SCLK) input in 8-bit bytes with data for Y7 output (MSB) first and data for Y0 output (LSB) last. Both SI and SCLK are active when serial input-output enable ($\overline{SIOE}$) input is low and are disabled when $\overline{SIOE}$ is high.

Each driver output is monitored by a voltage comparator that compares the Y-output voltage level with an internal out-of-saturation threshold voltage reference level. The logic state of the comparator output is dependent upon whether the Y output is greater or smaller than the reference voltage level. An activated driver output will be unlatched and turned off when the output voltage exceeds the out-of-saturation threshold voltage level except when the internal unlatch enable is low and disabled. The high-to-low transition of $\overline{SIOE}$ transfers the logic state of the comparator output to the shift register.

† BIDFET – Bipolardouble-diffused, N-channel and P-channel MOS transistors on same chip – patented process.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

TEXAS INSTRUMENTS
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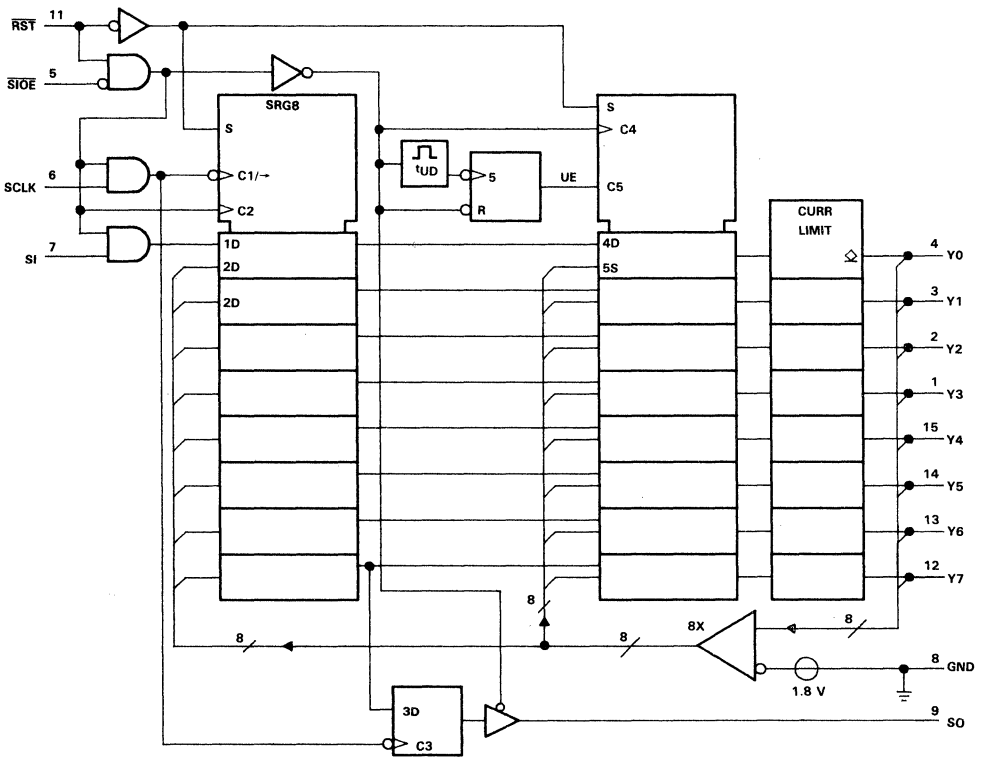
logic diagram (positive logic)



PIN NAME	PIN NO.	I/O	DESCRIPTION
GND	8		Ground. Common return for entire chip. The current out of this pin is potentially as high as 4 A if all outputs are on. This ground is used for both logic and power circuits
$\overline{RST}$	11	I	Reset. An asynchronous reset is provided for the shift register and the parallel latches. This pin is active when low and has no internal pullup. When active, it causes the power outputs to turn off. A power-on clear can be implemented using an RC network to V_{CC}.
$\overline{SCLK}$	6	I	Serial Clock. This pin clocks the shift register. The serial output (SO) will change state on the rising edge of this clock and serial input (SI) data will be accepted on the falling edge.
SI	7	I	Serial Input. This pin is the serial data input. A high on this pin will program a particular output to be off and a low will turn it on.
$\overline{SIOE}$	5	I	Serial Input-Output Enable. Data is transferred from the shift registers to the power outputs on the rising edge of this signal. The falling edge of this signal parallel loads the output voltage sense bits from the power output stages into the shift register. The output driver for the serial output (SO) pin is enabled when this pin is low, provided $\overline{RST}$ is high.
SO	9	O	Serial Output. This pin is the serial 3-state output from the shift register and is in a high-impedance state when $\overline{SIOE}$ is high or $\overline{RST}$ is low. A high for a data bit on this pin indicates that the corresponding power output (Y_n) is high. This could mean that the output was programmed to be off the last time a byte was input to the device or that the output faulted and was latched off by the output voltage sense indicator. A low on this pin for a data bit indicates that the corresponding power output (Y_n) is low (an "on" output stage or open-circuit condition).
V_{CC}	10		5-V supply voltage
Y0	4	O	Power Outputs. The outputs are provided with current limiting and voltage sense for fault indication and protection. The nominal load current for these outputs is 500 mA, but the current limiting is set to a minimum of 1.2 A. The active-low outputs also have voltage clamps set at about 35 V for recirculation of inductive load current. Internal 90-kΩ pull-down resistors are provided at each output. These resistors hold the output low during an open-circuit condition.
Y1	3		
Y2	2		
Y3	1		
Y4	15		
Y5	14		
Y6	13		
Y7	12		

PRINCIPLES OF OPERATION

timing data transfer

Figure 1 shows the overall 8-bit data-byte transfer to and from the TPIC2801 interface bus. The logic state of the eight output drivers, Y0 through Y7, is latched into the shift register at time t_0 on the high-to-low transition of $\overline{SIOE}$. Therefore, the SO output data (DY0, DY1 . . .) represents the conditions at the Y-driver outputs at time t_0. The data at SO output is updated on the low-to-high transition of SCLK.

Input data present at the SI input is clocked into the shift register on the high-to-low transition of SCLK. As shown in Figure 1 on the SI input, input data DI7 is clocked in at time t_1, DI6 is clocked in at time t_2, etc. Eight SCLK pulses are used to serially load the eight bits of new data into the device. After all the new data is serially loaded, the low-to-high transition of $\overline{SIOE}$ parallel loads the new data to the eight driver output latches, which in turn directly control the eight Y-driver outputs.

An unlimited amount of data can be shifted through the shift register (into the SI and out the SO) and this allows other devices to be cascaded in a daisy chain with the TPIC2801. Once the last data bit has been shifted into the TPIC2801, the $\overline{SIOE}$ input should be pulled high. The clock (SCLK) input should be low at both transitions of the $\overline{SIOE}$ input to avoid any false clocking of the shift register. The SCLK input is gated by the $\overline{SIOE}$ input, so the SCLK input is ignored whenever the $\overline{SIOE}$ is high. At the rising edge of the $\overline{SIOE}$ input, the shift register data is latched into the parallel latch and the output stages will be actuated by the new data. An internal 100-µs delay timer is also started on this rising edge. During the time delay, the outputs will be protected only by the analog current-limiting circuits, since the resetting of the parallel latches by fault conditions will be inhibited during this time period. This allows the device to overcome any high switching currents that can flow during turn-on. Once the delay has ended, the output voltages are sensed by the comparators and any output voltages higher than nominally 1.8 V are latched off.

PRINCIPLES OF OPERATION

fault-conditions check

Open-circuit conditions on any output can be monitored or checked by programming that output off. After a short delay (microseconds), another control byte can be clocked into the the device. If the diagnostic bit for that output comes back as a low, it indicates that the output is low and open circuited. A current overload condition can be detected by programming an output on. After waiting an appropriate length of time, another byte should be clocked into the TPIC2801. The diagnostic bit clocked back from the TPIC2801 in the subsequent data transfer should indicate a low output. If a high returns, a current overload is indicated. A quick overall check can be done by clocking in a test control byte. After a sufficient time delay, another control byte (same byte can be used) is clocked in. The diagnostic data is exclusive ORed with the original control byte. If a fault condition exists, a high will result.

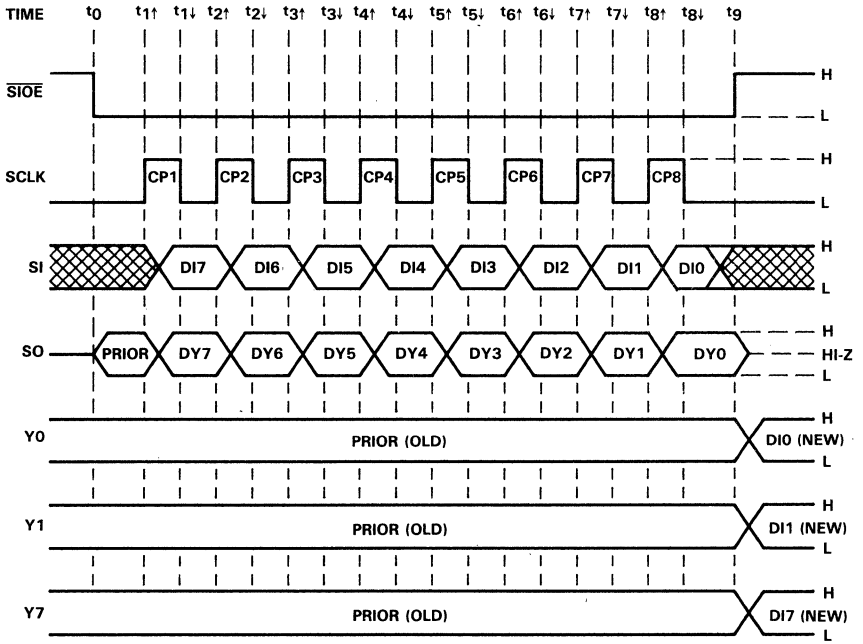
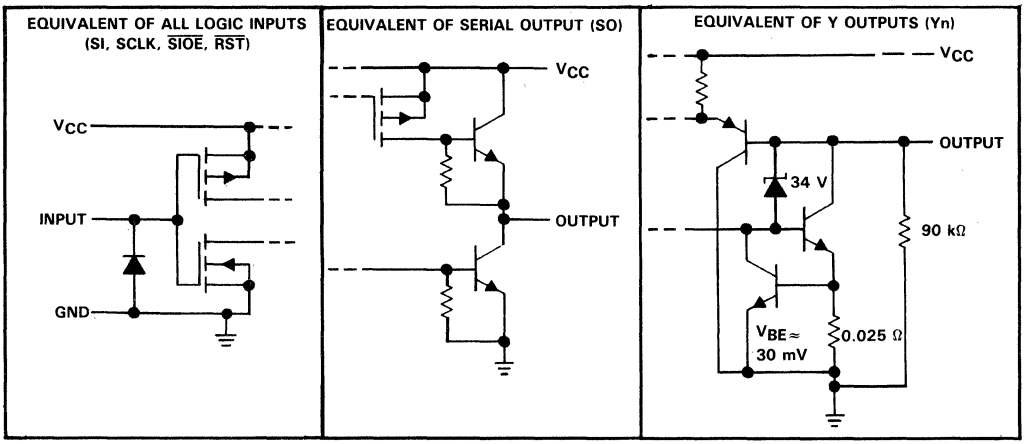


FIGURE 1. DATA-BYTE TRANSFER TIMING

schematics of inputs and outputs



All resistor and voltage values shown are nominal.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1)	−0.3 V to 7 V
Input voltage, V_I	7 V
Output voltage range at SO	−0.3 V to 7 V
Input current, I_I	−15 mA
Peak output sink current at Y, I_O repetitive, t_W = 10 ms, duty cycle = 50%, see Notes 2 and 3	Internally Limited
Continuous output current at Y, I_O (see Note 3)	1 A
Peak current through GND terminal:	
Nonrepetitive t_W = 0.2 ms	−8A
Repetitive, t_W = 10 ms, duty cycle = 50%	−6 A
Continuous current through GND terminal	−4.5 A
Output clamp energy, E_{OK} (after turning off $I_{O(on)}$ = 0.5 A)	40 mJ
Continuous dissipation at (or below) 25°C free-air temperature (see Note 4)	3.575 W
Continuous dissipation at (or below) 75°C case temperature (see Note 4)	25 W
Operating case or virtual-junction temperature range	−55°C to 150°C
Storage temperature range	− 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. Each Y output is individually current limited with a typical over-current limit of about 1.4 A.
3. Multiple Y outputs of this device may conduct rated current simultaneously; however, power dissipation (average) over a short time interval must fall within the continuous dissipation range and the GND current must fall within the GND-terminal current range.
4. For operation above 25°C free-air temperature, derate linearly at the rate of 28.6 mW/°C. For operation above 75°C case temperature, derate lineraly at the rate of 333 mW/°C. To avoid exceeding the maximum virtual-junction temperature, these ratings must not be exceeded.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	0.7 V_{CC}		5.25	V
Low-level input voltage, V_{IL}	−0.3		0.2 V_{CC}	V
Output voltage, $V_{O(off)}$			30	V
Continuous output current, $I_{O(on)}$			1	A
Operating case temperature, T_C	−40	25	105	°C

timing requirements (see Figure 2)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
f_{SCLK}	Clock frequency				0	500	kHz
t_{wSCLKH}	Pulse duration, SCLK high				840		ns
t_{wSCLKL}	Pulse duration, SCLK low				840		ns
t_{wRST}	Pulse duration, $\overline{RST}$ low				1000		ns
t_{su1}	Setup time	$\overline{SIOE}$↓	SCLK↑		1000		ns
t_{su2}	Setup time	SCLK↓	$\overline{SIOE}$↑		1000		ns
t_{su3}	Setup time	SI	SCLK↓		500		ns
t_{h1}	Hold time	SCLK↓	SI		500		ns
t_r	Rise time (SCLK, SI, $\overline{SIOE}$)					2	µs
t_f	Fall time (SCLK, SI, $\overline{SIOE}$)					2	µs

electrical characateristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted)

driver array outputs (Y0 to Y7)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OK}	Output clamp voltage	I_O = 0.5 A, output programmed off and current shunted to ground		30	36	40	V
$I_{O(off)}$	Off-state output current	V_O = 24 V with output programmed off				1	mA
$I_{O(CL)}$	Output current limit	V_O = 3 V with output programmed on		1.05	1.4		A
$V_{O(on)}$	On-state output voltage	With output programmed on	I_{OL} = 0.5 A		0.4	0.5	V
			I_{OL} = 0.75 A		0.6	1	V
			I_{OL} = 1 A, During unlatch disable		0.8	1.5	V
V_{TOS}	Out of saturation threshold voltage	With output programmed on and an over-current fault condition		1.6	1.8	2	V

shift register (Inputs SI, $\overline{SIOE}$, SCLK, and $\overline{RST}$)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{T+}	Positive-going threshold voltage			0.7 V_{CC}	V
V_{T-}	Negative-going threshold voltage		0.2 V_{CC}		V
V_{hys}	Hysteresis voltage ($V_{T+} - V_{T-}$)		0.85	2.25	V
I_I	Input current	V_I = 0 to V_{CC}		±10	µA
C_i	Inpout capacitance	V_I = 0 to V_{CC}		20	pF

† All typical values are at V_{CC} = 5 V, T_J = 25°C.

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted)

shift register (output SO)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OL}	Low-level output voltage	I_O = 1.6 mA			0.2	0.4	V
V_{OH}	High-level output voltage	I_O = −0.8 mA		V_{CC} −1.3			V
I_O	Output current	V_O = 0 to V_{CC}, $\overline{SIOE}$ input high				±10	µA
I_{CC}	Supply current	All outputs on, I_O = 0.5 A at all outputs	T_J = 105°C			150	mA
			T_J = 25°C			200	
			T_J = −40°C			250	
I_{CC}	Supply current	All outputs off	T_J = 25°C		4	10	mA
C_O	Output capacitance	V_O = 0 to V_{CC}, $\overline{SIOE}$ input high				20	pF

† All typical values are at V_{CC} = 5 V, T_J = 25°C.

thermal characteristics

PARAMETER		MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case temperature		3	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient temperature		35	°C/W

switching characteristics over recommended ranges of supply voltage and operating case temperatures (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS		MIN	MAX	UNIT
t_{en}	Enable time	$\overline{SIOE}$↓	SO	C_L = 20 pF, See Figure 3	R_L = 2 kΩ,		1000	ns
t_{dis}	Disable time	$\overline{SIOE}$↑	SO	C_L = 20 pF, See Figure 3	R_L = 2 kΩ,		1000	ns
t_{d1}	Delay time, valid data	SCLK↑	SO	C_L = 200 pF,	See Figure 4		740	ns
t_{d2}	Delay time, unlatch disable	$\overline{SIOE}$↑	Y_n	C_L = 20 pF, See Figure 5	R_L = 5 Ω,	75	250	µs
$t_{r(so)}$	Rise time, SO			C_L = 200 pF,	See Figure 4		150	ns
$t_{f(so)}$	Fall time, SO			C_L = 200 pF,	See Figure 4		150	ns
$t_{d(on)}$	Delay time, turn-on	$\overline{SIOE}$↑	Y_n	I_{OL} = 500 mA, R_L = 28 Ω,	C_L = 20 pF, See Figure 6		10	µs
$t_{d(off)}$	Delay time, turn-off	$\overline{SIOE}$↑	Y_n	I_{OL} = 500 mA, R_L = 28 Ω,	C_L = 20 pF, See Figure 6		10	µs
t_v	Valid time, SO output data remains valid after SCLK high	SCLK↑	SO	C_L = 200 pF,	See Figure 4	0		ns

PARAMETER MEASUREMENT INFORMATION

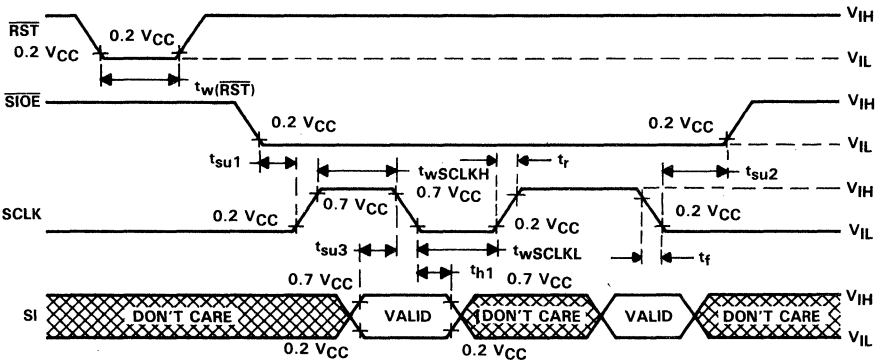
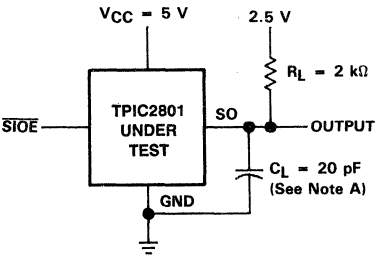
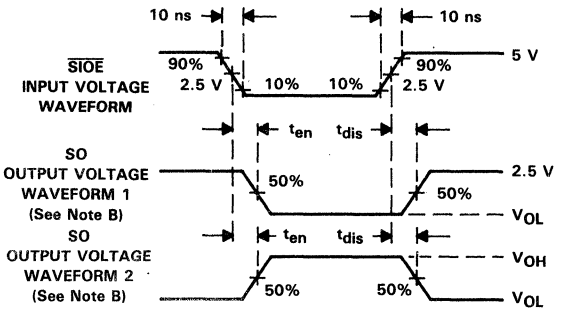


FIGURE 2. INPUT TIMING WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



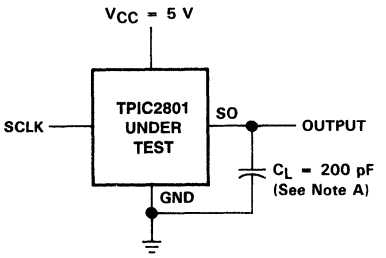
TEST CIRCUIT FOR ENABLE AND DISABLE TIMES



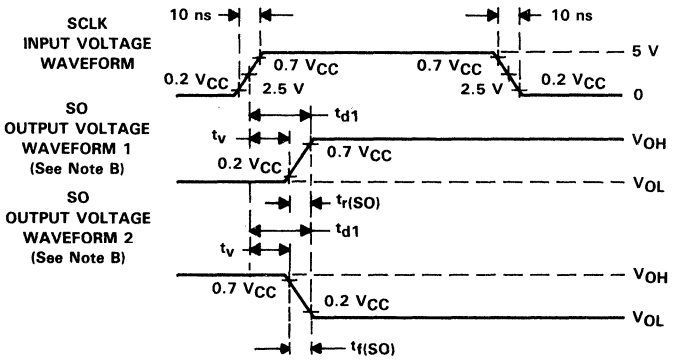
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control when $\overline{SIOE}$ is high. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control when $\overline{SIOE}$ is high.

FIGURE 3. VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES

PARAMETER MEASUREMENT INFORMATION



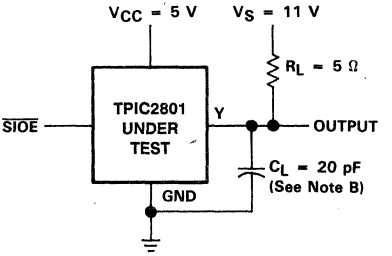
TEST CIRCUIT FOR VALID DATA
DELAY TIME t_{d1} AND VALID TIME t_v



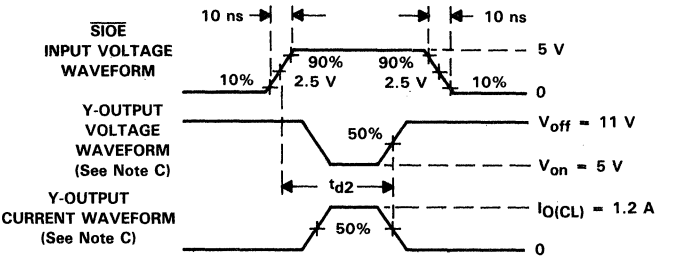
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the low-to-high transition of SCLK causes the SO output to switch from low to high. Waveform 2 is for an output with internal conditions such that the low-to-high transition of SCLK causes the SO output to switch from high to low.

FIGURE 4. VOLTAGE WAVEFORMS FOR DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



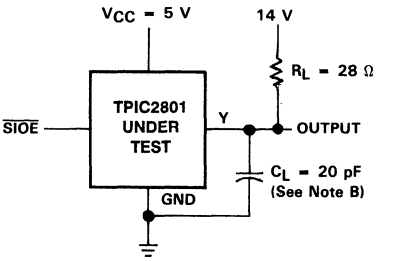
TEST CIRCUIT FOR UNLATCH DISABLE
DELAY TIME t_{d2}
(See Note A)



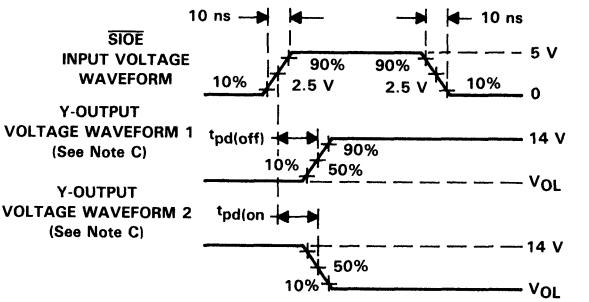
NOTES: A. t_{d2} = delay until Y-output current goes off under fault condition.
B. C_L includes probe and jig capacitance.
C. Output voltage and current waveforms are for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from being off to being on.
D. Load voltage V_S and load resistance R_L are selected such that on-state voltage at the Y output under test, V_{on} is greater than the maximum out-of-saturation threshold voltage, V_{TOS}. Thus, $V_{OL} = V_{on} > V_{TOS(max)} = 1.98$ V.

FIGURE 5. VOLTAGE AND CURRENT WAVEFORMS FOR UNLATCH DISABLE DELAY

PARAMETER MEASUREMENT INFORMATION



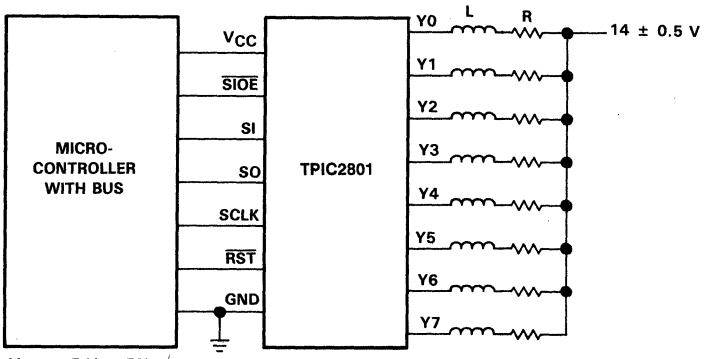
TEST CIRCUIT FOR TURN-OFF $t_{d(off)}$
AND TURN-ON $t_{d(on)}$ DELAY TIMES
(See Note A)



NOTES: A. $t_{d(off)} = t_{PLH}$, $t_{d(on)} = t_{PHL}$.
B. C_L includes probe and jig capacitance.
C. Waveform 1 is for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from on to off. Waveform 2 is for an output with internal conditions such the low-to-high transition of $\overline{SIOE}$ causes the output to switch from off to on.

FIGURE 6. VOLTAGE WAVEFORMS FOR TURN-OFF AND TURN-ON DELAY TIMES

TYPICAL APPLICATION DATA



V_{CC} = 5 V ± 5%
R = 30 Ω ± 5%
L = 10 mH ± 10%
8 LOADS UP TO 0.5 A EACH

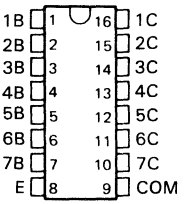
FIGURE 7. MICROCONTROLLER DRIVING EIGHT LOADS USING A TPIC2801 FOR LOAD INTERFACE

D2624, DECEMBER 1976—REVISED SEPTEMBER 1986

HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- **500-mA Rated Collector Current (Single Output)**
- **High-Voltage Outputs . . . 50 V**
- **Output Clamp Diodes**
- **Inputs Compatible With Various Types of Logic**
- **Relay Driver Applications**
- **Designed to Be Interchangeable With Sprague ULN2001A Series**

D OR N PACKAGE
(TOP VIEW)

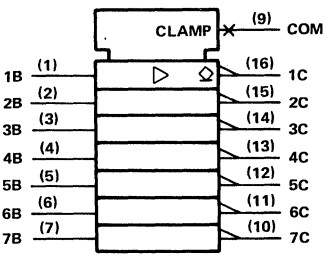


description

The ULN2001A, ULN2002A, ULN2003A, ULN2004A, and ULN2005A are monolithic high-voltage, high-current Darlington transistor arrays. Each consists of seven n-p-n Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. For 100-V (otherwise interchangeable) versions, see the SN75465 through SN75469.

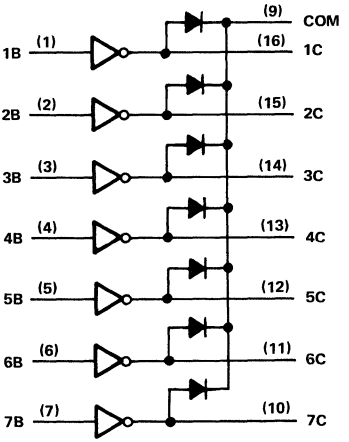
The ULN2001A is a general-purpose array and may be used with TTL, P-MOS, CMOS, and other MOS technologies. The ULN2002A is specifically designed for use with 14- to 25-V P-MOS devices. Each input of this device has a zener diode and resistor in series to control the input current to a safe limit. The ULN2003A has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices. The ULN2004A has a 10.5-kΩ series base resistor to allow its operation directly from CMOS or P-MOS devices that use supply voltages of 6 to 15 V. The required input current of the ULN2004A is below that of the ULN2003A, and the required voltage is less than that required by the ULN2002A. The ULN2005A has a 1050-Ω series base resistor and is specifically designed for use with TTL devices where higher output current is required and loading of the driving source is not a concern.

logic symbol†

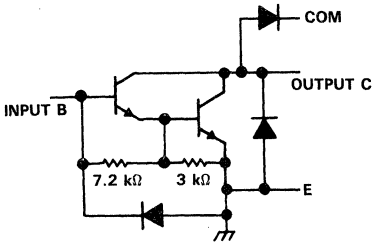


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

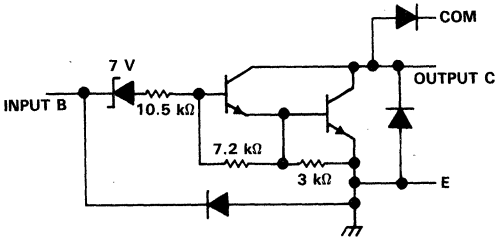
logic diagram



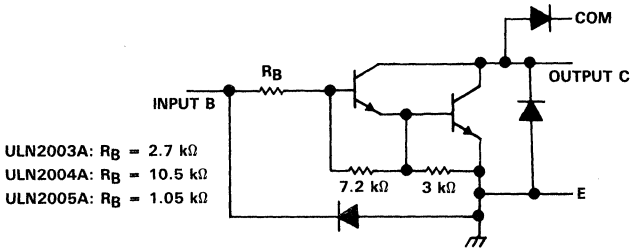
schematics (each Darlington pair)



ULN2001A



ULN2002A



ULN2003A, ULN2004A, ULN2005A

All resistor values shown are nominal.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-emitter voltage	50 V
Input voltage (see Note 1): ULN2002A, ULN2003A, ULN2004A	30 V
ULN2005A	15 V
Peak collector current (see Figures 14 and 15)	500 mA
Output clamp diode current	500 mA
Total emitter-terminal current	−2.5 A
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range	−20°C to 85°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: All voltage values are with respect to the emitter/substrate terminal, E, unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2001A			ULN2002A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V,	I_I = 0			50			50	μA
			V_{CE} = 50 V,	I_I = 0			100			100	
		2	T_A = 70°C	V_I = 6 V						500	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 μA,	50	65		50	65		μA
I_I	Input current	4	V_I = 17 V						0.82	1.25	mA
h_{FE}	Static forward current transfer ratio	5	V_{CE} = 2 V,	I_C = 350 mA	1000						
$V_{I(on)}$	On-state input voltage	6	V_{CE} = 2 V,	I_C = 300 mA						13	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 250 μA,	I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 μA,	I_C = 200 mA		1	1.3		1	1.3	
			I_I = 500 μA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
I_R	Clamp diode reverse current	7	V_R = 50 V				50			50	μA
			V_R = 50 V,	T_A = 70°C			100			100	
V_F	Clamp diode forward voltage	8	I_F = 350 mA			1.7	2		1.7	2	V
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2003A			ULN2004A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V,	I_I = 0			50			50	μA
			V_{CE} = 50 V,	I_I = 0			100			100	
		2	T_A = 70°C	V_I = 1 V						500	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 μA,	50	65		50	65		μA
I_I	Input current	4	V_I = 3.85 V			0.93	1.35				mA
			V_I = 5 V						0.35	0.5	
			V_I = 12 V						1	1.45	
$V_{I(on)}$	On-state input voltage	6	V_{CE} = 2 V	I_C = 125 mA						5	V
				I_C = 200 mA			2.4			6	
				I_C = 250 mA			2.7				
				I_C = 275 mA						7	
				I_C = 300 mA			3				
				I_C = 350 mA						8	
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 250 μA,	I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 μA,	I_C = 200 mA		1	1.3		1	1.3	
			I_I = 500 μA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
I_R	Clamp diode reverse current	7	V_R = 50 V				50			50	μA
			V_R = 50 V,	T_A = 70°C			100			100	
V_F	Clamp diode forward voltage	8	I_F = 350 mA			1.7	2		1.7	2	V
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	ULN2005A			UNIT
				MIN	TYP	MAX	
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V, I_I = 0			50	μA
			V_{CE} = 50 V, I_I = 0, T_A = 70°C			100	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, I_C = 500 μA, T_A = 70°C	50	65		μA
I_I	Input current	4	V_I = 3 V		1.5	2.4	mA
$V_{I(on)}$	On-state input voltage	6	V_{CE} = 2 V, I_C = 350 mA			2.4	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 250 μA, I_C = 100 mA		0.9	1.1	V
			I_I = 350 μA, I_C = 200 mA		1	1.3	
			I_I = 500 μA, I_C = 350 mA		1.2	1.6	
I_R	Clamp diode reverse current	7	V_R = 50 V			50	μA
			V_R = 50 V, T_A = 70°C			100	
V_F	Clamp diode forward voltage	8	I_F = 350 mA		1.7	2	V
C_i	Input capacitance		V_I = 0, f = 1 MHz		15	25	pF

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 9		0.25	1	μs
t_{PHL}	Propagation delay time, high-to-low-level output			0.25	1	μs
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O ≈ 300 mA, See Figure 10	V_S – 20			mV

PARAMETER MEASUREMENT INFORMATION

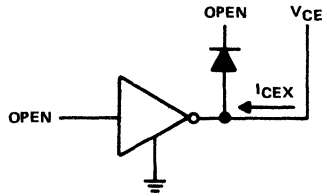


FIGURE 1. I_{CEX}

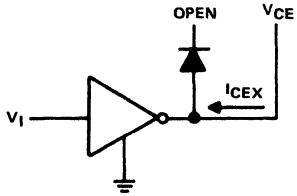


FIGURE 2. I_{CEX}

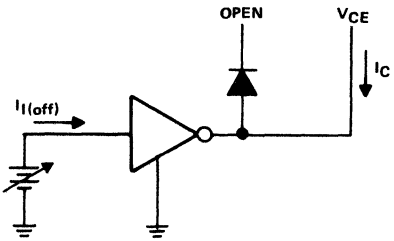


FIGURE 3. $I_{I(off)}$

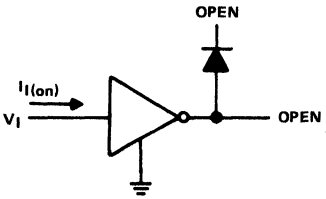
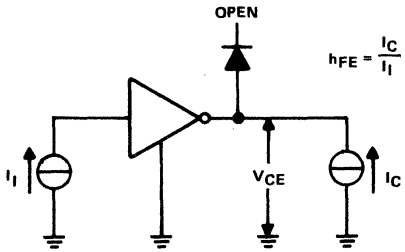


FIGURE 4. I_I



NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE}.

FIGURE 5. h_{FE}, $V_{CE(sat)}$

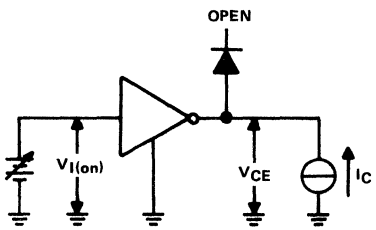


FIGURE 6. $V_{I(on)}$

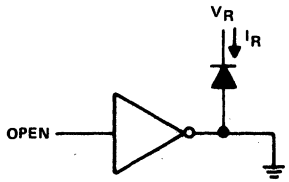


FIGURE 7. I_R

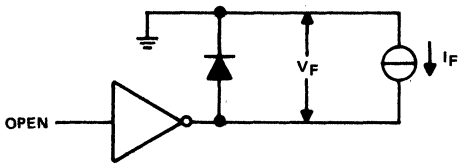
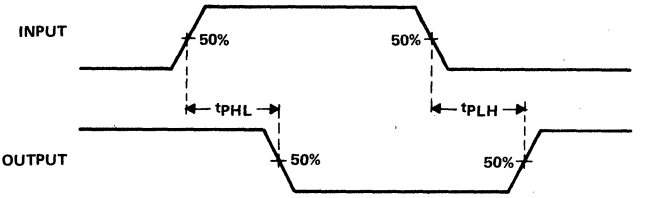


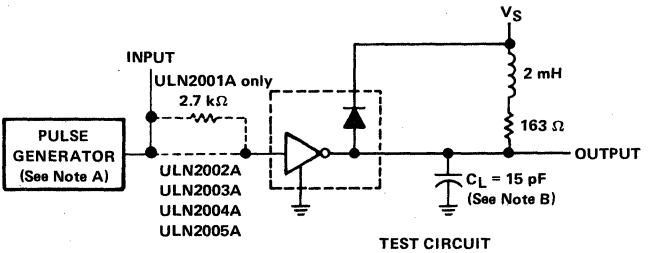
FIGURE 8. V_F

PARAMETER MEASUREMENT INFORMATION

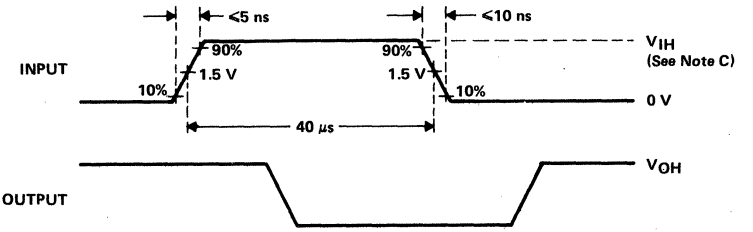


VOLTAGE WAVEFORMS

FIGURE 9. PROPAGATION DELAY TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. For testing the ULN2001A, ULN2003A, and the ULN2005A, V_{IH} = 3 V; for the ULN2002A, V_{IH} = 13 V; for the ULN2004A, V_{IH} = 8 V.

FIGURE 10. LATCH-UP TEST

TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (ONE DARLINGTON)

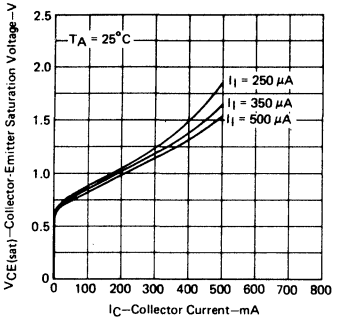


FIGURE 11

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (TWO DARLINGTONS PARALLELED)

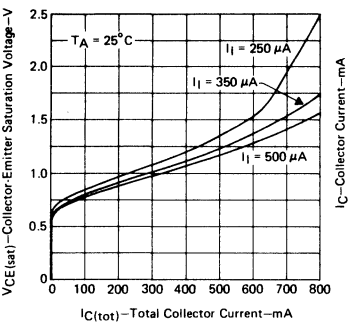


FIGURE 12

COLLECTOR CURRENT vs INPUT CURRENT

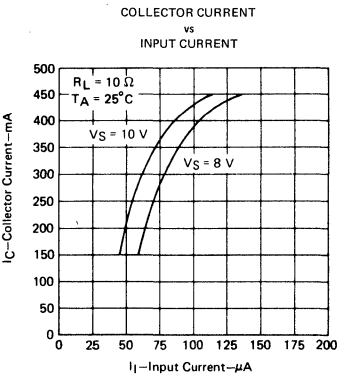


FIGURE 13

THERMAL INFORMATION

D PACKAGE MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE

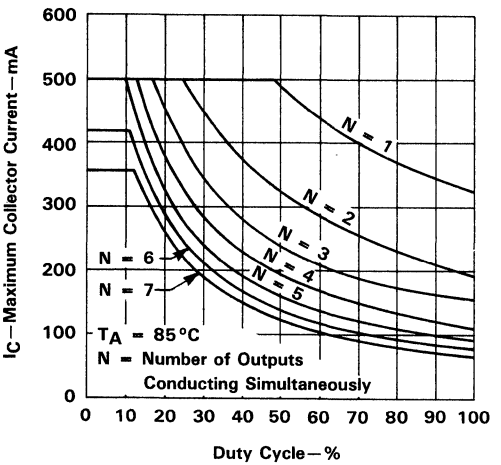


FIGURE 14

N PACKAGE MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE

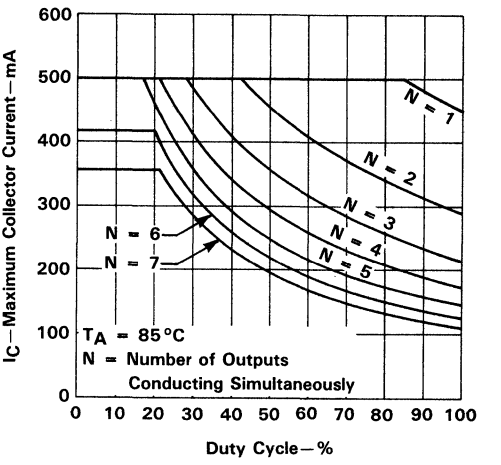
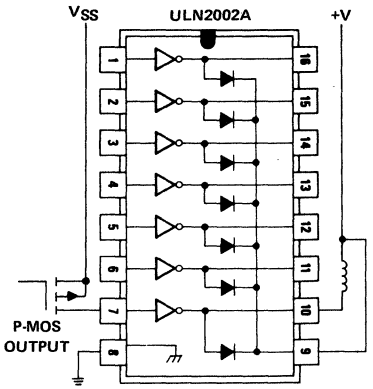
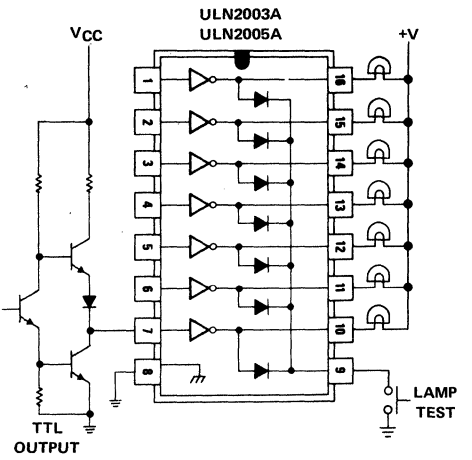


FIGURE 15

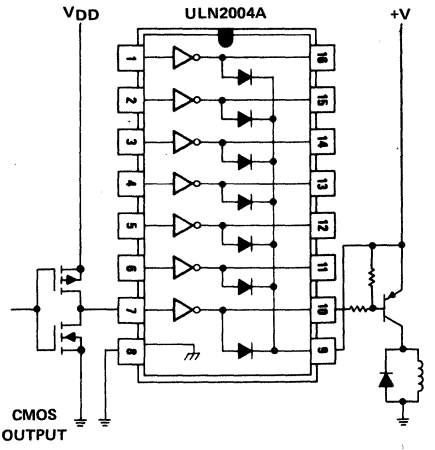
APPLICATION INFORMATION



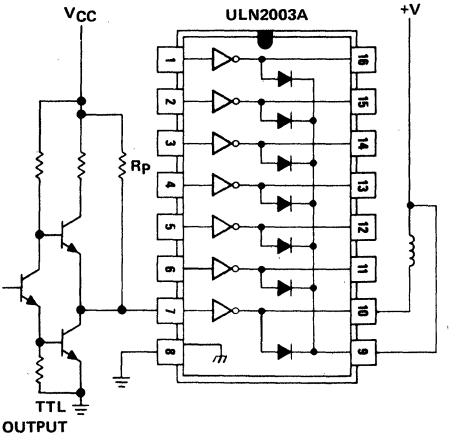
P-MOS TO LOAD



TTL TO LOAD



BUFFER FOR
HIGHER CURRENT LOADS

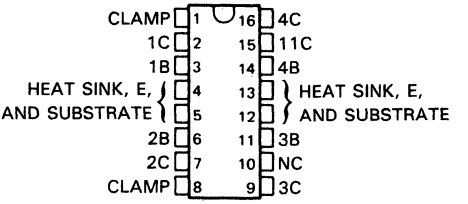


USE OF PULL-UP RESISTORS
TO INCREASE DRIVE CURRENT

D2528, DECEMBER 1979—REVISED SEPTEMBER 1986

- **Output Collector Current . . . 1.5 A Max**
- **2-W Dissipation Rating**
- **High Output-Voltage Capability**
- **Outputs Diode-Clamped for Inductive Loads**
- **Common-Emitter Circuit for Current Sink**
- **ULN2064 and ULN2065 Have TTL Compatible Inputs**
- **ULN2066 and ULN2067 Have CMOS- and PMOS-Compatible Inputs**
- **Designed for Interchangeability With Sprague ULN2064 thru ULN2067, Respectively**

NE PACKAGE
(TOP VIEW)



NC—No internal connection

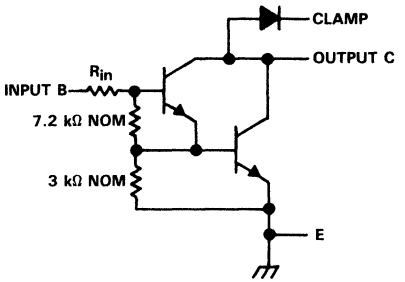
description

The ULN2064, ULN2065, ULN2066, and ULN2067 are monolithic high-voltage, high-current darlington transistor switches. Each comprises four n-p-n darlington pairs. All units feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. Outputs and inputs may each be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. These common-emitter circuits are designed to operate as current sinks to the load.

The ULN2064 and ULN2065 are intended for use with TTL and 5-V MOS logic. The ULN2066 and ULN2067 are intended for use with PMOS and higher-voltage CMOS logic.

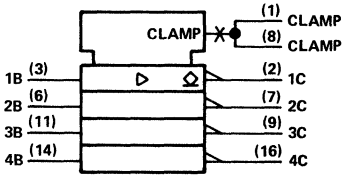
The ULN2064, ULN2065, ULN2066, and ULN2067 are characterized for operation from −20°C to 85°C.

schematic (each darlington pair)



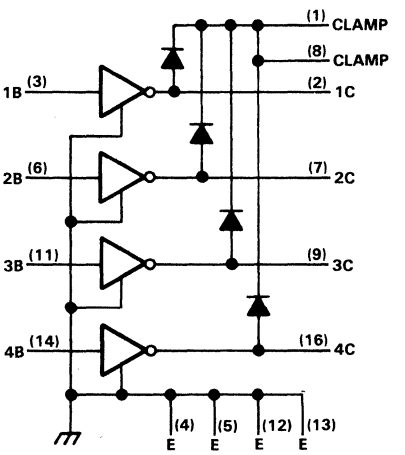
ULN2064, ULN2065: R_{in} = 350 Ω NOM
ULN2066, ULN2067: R_{in} = 3 kΩ NOM

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



absolute maximum ratings at 25°C free-air temperature for each switch (unless otherwise noted)

	ULN2064	ULN2065	ULN2066	ULN2067	UNIT
Collector-emitter voltage	50	80	50	80	V
Input voltage (see Note 1)	15	15	30	30	V
Peak collector current (see Figures 12, 13, and 14)	1.5	1.5	1.5	1.5	A
Input current	25	25	25	25	mA
Total power dissipation at (or below) 25°C free-air temperature (see Note 2)	2075	2075	2075	2075	mW
Operating free-air temperature range	−20 to 85	−20 to 85	−20 to 85	−20 to 85	°C
Storage temperature range	−55 to 150	−55 to 150	−55 to 150	−55 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds	260	260	260	260	°C

NOTES: 1. All voltage values (unless otherwise noted) are with respect to the emitter/substrate terminal E.
2. For operation above 25°C free-air temperature, derate total power linearly to 1079 mW at 85°C at the rate of 16.6 mW/°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	ULN2064 MIN	ULN2064 MAX	ULN2065 MIN	ULN2065 MAX	ULN2066 MIN	ULN2066 MAX	ULN2067 MIN	ULN2067 MAX	UNIT
$V_{CEX(sus)}$	Collector sustaining voltage	1	V_I = 0.4 V, I_C = 100 mA	35		50		35		50		V
I_{CEX}	Collector output cutoff current	2	V_{CE} = 50 V		100				100			μA
			V_{CE} = 50 V, T_A = 70°C		500				500			
			V_{CE} = 80 V				100				100	
			V_{CE} = 80 V, T_A = 70°C				500				500	
$I_{I(on)}$	On-state input current	3	V_I = 2.4 V	1.4	4.3	1.4	4.3					mA
			V_I = 3.75 V	3.3	9.6	3.3	9.6					
			V_I = 5 V					0.6	1.8	0.6	1.8	
			V_I = 12 V					1.7	5.2	1.7	5.2	
$V_{I(on)}$	On-state input voltage	4	V_{CE} = 2 V, I_C = 1 A		2		2		6.5		6.5	V
			V_{CE} = 2 V, I_C = 1.5 A, See Note 3		2.5		2.5		10		10	
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 625 μA, I_C = 500 mA		1.1		1.1		1.1		1.1	V
			I_I = 935 μA, I_C = 750 mA		1.2		1.2		1.2		1.2	
			I_I = 1.25 mA, I_C = 1 A		1.3		1.3		1.3		1.3	
			I_I = 2 mA, I_C = 1.25 A, See Note 3		1.4				1.4			
			I_I = 2.25 mA, I_C = 1.5 A, See Note 3				1.5				1.5	
I_R	Clamp-diode reverse current	6	V_R = 50 V		50				50			μA
			V_R = 50 V, T_A = 70°C		100				100			
			V_R = 80 V				50				50	
			V_R = 80 V, T_A = 70°C				100				100	
V_F	Clamp-diode forward voltage	7	I_F = 1 A		1.75		1.75		1.75		1.75	V
			I_F = 1.5 A, See Note 3		2		2		2		2	

NOTE 3: These parameters must be measured on one output at a time using pulse techniques, t_w = 10 ms, duty cycle ≤ 10%.

switching characteristics at 25°C free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 8			1	μs
t_{PHL}	Propagation delay time, high-to-low-level output				1.5	μs

PARAMETER MEASUREMENT INFORMATION

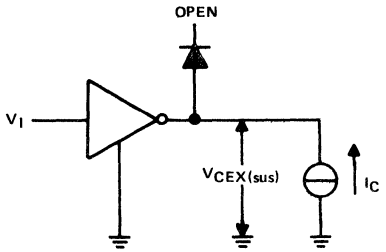


FIGURE 1. $V_{CEX(sus)}$

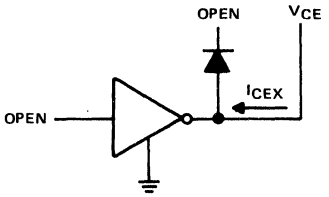


FIGURE 2. I_{CEX}

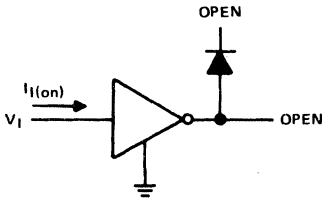


FIGURE 3. $I_{I(on)}$

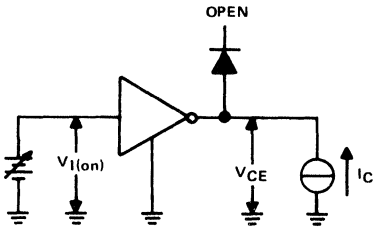


FIGURE 4. $V_{I(on)}$

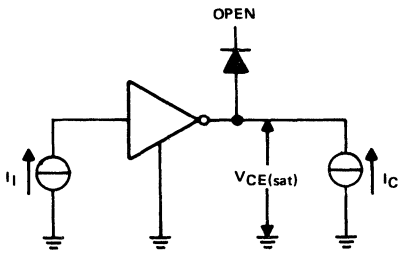


FIGURE 5. $V_{CE(sat)}$

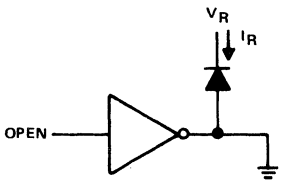


FIGURE 6. I_R

PARAMETER MEASUREMENT INFORMATION

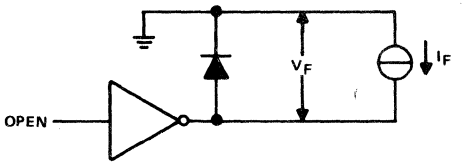
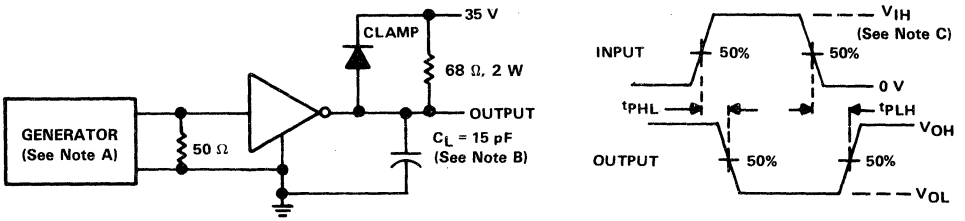


FIGURE 7. V_F



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, Z_O = 50 Ω.
B. C_L includes all probe and stray capacitance.
C. V_{IH} = 2.5 V for ULN2064 and ULN2065. V_{IH} = 10 V for ULN2065 and ULN2067.

FIGURE 8. SWITCHING TIMES

ELECTRICAL CHARACTERISTICS

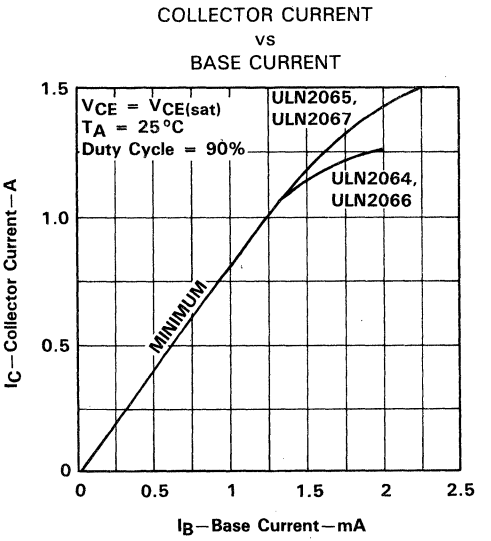


FIGURE 9

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

THERMAL INFORMATION

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

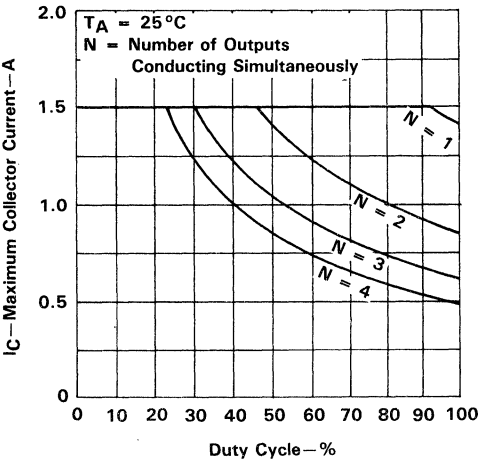


FIGURE 10

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

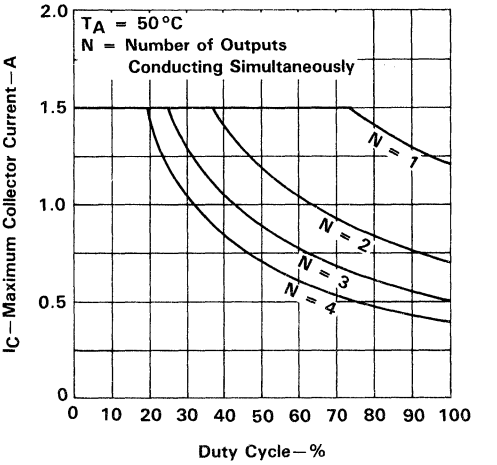


FIGURE 11

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

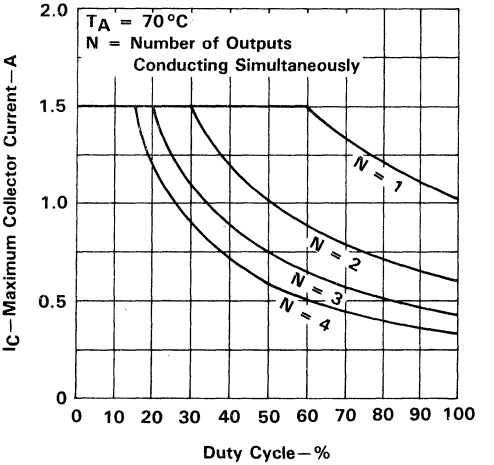


FIGURE 12

APPLICATION INFORMATION

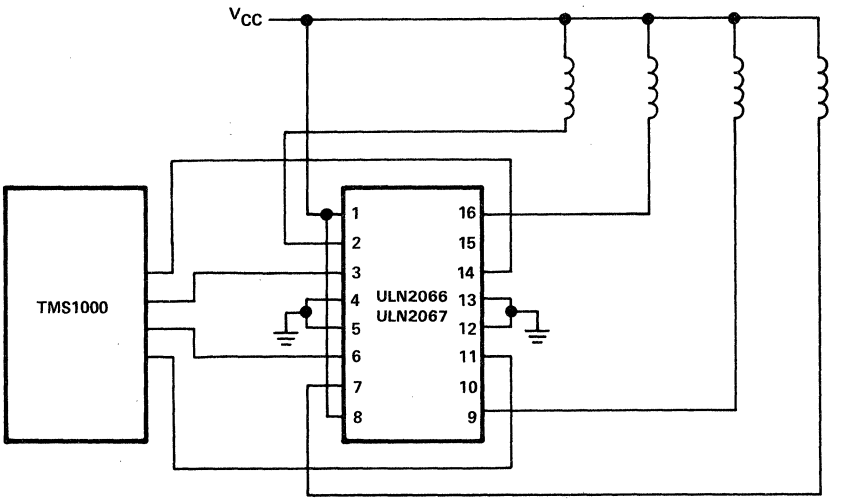
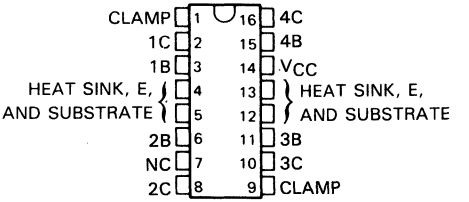


FIGURE 13. RELAY DRIVER INTERFACE

D2579, MAY 1980—REVISED SEPTEMBER 1986

- **Output Collector Current . . . 1.5 A Max**
- **2-W Dissipation Rating**
- **High Output-Voltage Capability**
- **Preamp for High Current Gain**
- **Outputs Diode-Clamped for Inductive Loads**
- **Common-Emitter Circuit for Current Sink**
- **Inputs Compatible With TTL and 5-V CMOS**
- **Designed for Interchangeability With Sprague ULN2068 and ULN2069**

NE PACKAGE
(TOP VIEW)



NC—No internal connection

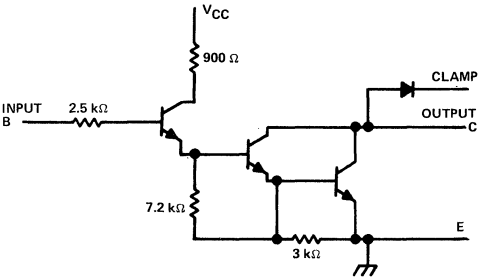
description

The ULN2068 and ULN2069 are monolithic integrated circuits each consisting of four high-voltage, high-current n-p-n cascaded transistor switches. Each switch includes a first stage compatible with both TTL and 5-V CMOS signal levels. The second and third stages form uncommitted-collector outputs with common-cathode clamp diodes for switching inductive loads.

The ULN2068 and ULN2069 can sink up to 1.5 A per switch. Applications include logic buffers, MOS drivers, memory drivers, line drivers, relay drivers, hammer drivers, lamp drivers, and display drivers (LED and gas discharge).

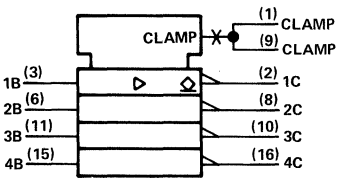
The ULN2068 and ULN2069 are characterized for operation from −20°C to 85°C.

schematic (each switch)



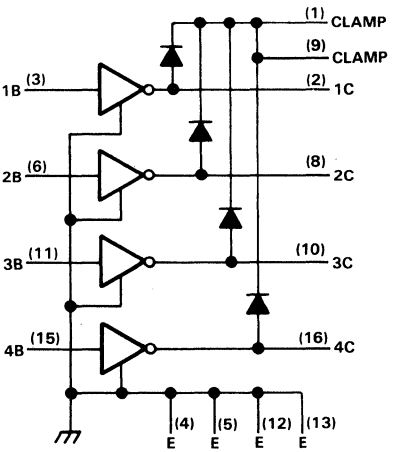
Resistor values shown are nominal.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings at 25°C free-air temperature for each switch (unless otherwise noted)

	ULN2068	ULN2069	UNIT
Collector-emitter voltage	50	80	V
Supply voltage, V_{CC} (see Note 1)	10	10	V
Input voltage	15	15	V
Peak collector current (see Figures 10, 11, and 12)	1.5	1.5	A
Total power dissipation at (or below) 25°C free-air temperature (see Note 2)	2075	2075	mW
Operating free-air temperature range	−20 to 85	−20 to 85	°C
Storage temperature range	−55 to 150	−55 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds	260	260	°C

NOTES: 1. All voltage values (unless otherwise noted) are with respect to the emitter/substrate terminal E.
2. For operation above 25°C free-air temperature, derate total power linearly to 1079 mW at 85°C at the rate of 16.6 mW/°C.

electrical characteristics at 25°C free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	ULN2068 MIN	ULN2068 MAX	ULN2069 MIN	ULN2069 MAX	UNIT
$V_{CEX(sus)}$	Collector sustaining voltage	1	V_I = 0.4 V, I_C = 100 mA	35		50		V
I_{CEX}	Collector output cutoff current	2	V_{CE} = 50 V		100			μA
			V_{CE} = 50 V, T_A = 70°C		500			
			V_{CE} = 80 V				100	
			V_{CE} = 80 V, T_A = 70°C				500	
$I_{I(on)}$	On-state input current	3	V_I = 2.4 V		250		250	μA
			V_I = 3.75 V		1000		1000	
$V_{I(on)}$	On-state input voltage	4	V_{CE} = 2 V, I_C = 1.5 A, See Note 3		2.4		2.4	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	V_I = 2.4 V, I_C = 500 mA		1.1		1.1	V
			V_I = 2.4 V, I_C = 750 mA		1.2		1.2	
			V_I = 2.4 V, I_C = 1 A		1.3		1.3	
			V_I = 2.4 V, I_C = 1.25 A, See Note 3		1.4			
			V_I = 2.4 V, I_C = 1.5 A, See Note 3				1.5	
I_R	Clamp-diode reverse current	6	V_R = 50 V		50			μA
			V_R = 50 V, T_A = 70°C		100			
			V_R = 80 V				50	
			V_R = 80 V, T_A = 70°C				100	
V_F	Clamp-diode forward voltage	7	I_F = 1 A		1.75		1.75	V
			I_F = 1.5 V, See Note 3		2		2	
I_{CC}	Supply current (only one switch conducting)	8	V_I = 2.4 V, I_C = 500 mA		6		6	mA

NOTE 3: These parameters must be measured on one output at a time using pulse techniques, t_w = 10 ms, duty cycle ≤ 10%.

switching characteristics at 25°C free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 9			1	μs
t_{PHL}	Propagation delay time, high-to-low-level output				1.5	μs

PARAMETER MEASUREMENT INFORMATION

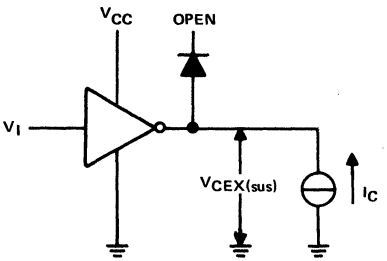


FIGURE 1. $V_{CEX(sus)}$

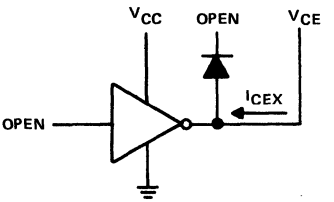


FIGURE 2. I_{CEX}

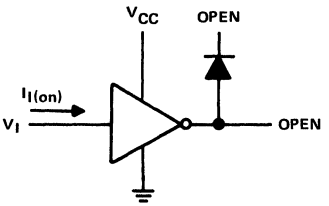


FIGURE 3. $I_{I(on)}$

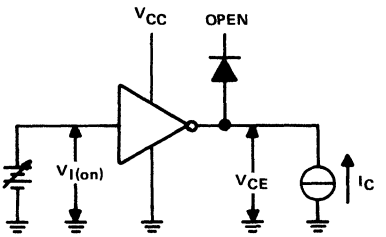


FIGURE 4. $V_{I(on)}$

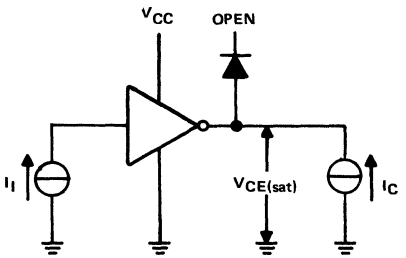


FIGURE 5. $V_{CE(sat)}$

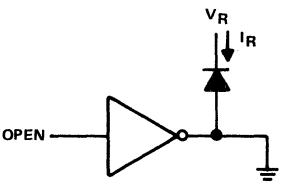


FIGURE 6. I_R

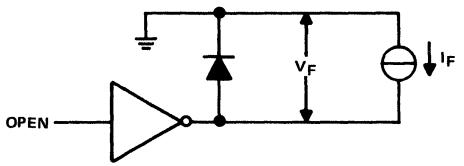


FIGURE 7. V_F

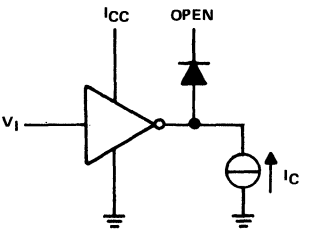
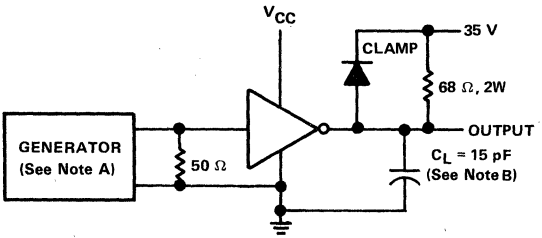
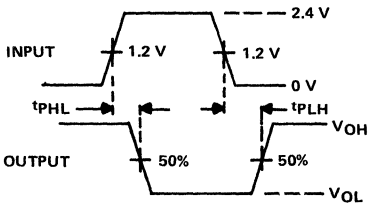


FIGURE 8. I_{CC}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, Z_O = 50 Ω.
B. C_L includes all probe and stray capacitance.

FIGURE 9. SWITCHING TIMES

THERMAL INFORMATION

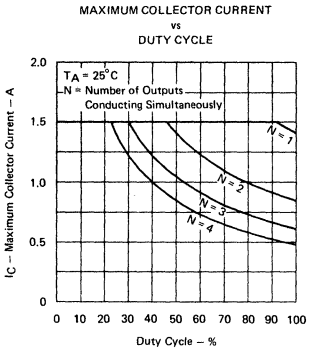


FIGURE 10

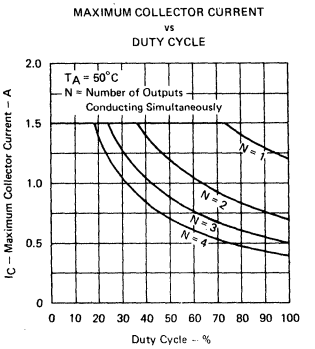


FIGURE 11

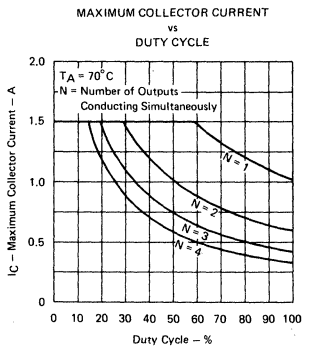


FIGURE 12

APPLICATION INFORMATION

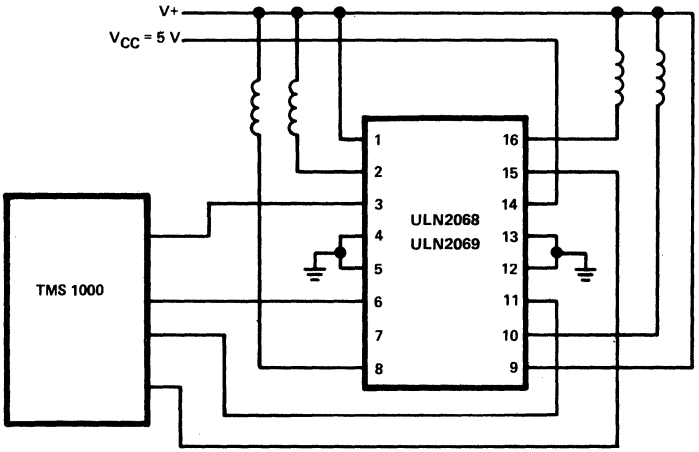
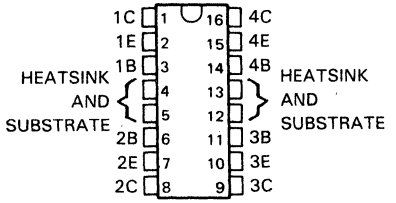


FIGURE 13. RELAY DRIVER INTERFACE

D2580, MAY 1980—REVISED SEPTEMBER 1986

- **Output Collector Current . . . 1.5 A Max**
- **2-W Dissipation Rating**
- **High Output-Voltage Capability**
- **Output Sink- or Source-Current Capabilities**
- **Input Compatible with TTL or 5-V CMOS**
- **Designed for Interchangeability with Sprague ULN2074 and ULN2075**

NE PACKAGE
(TOP VIEW)



description

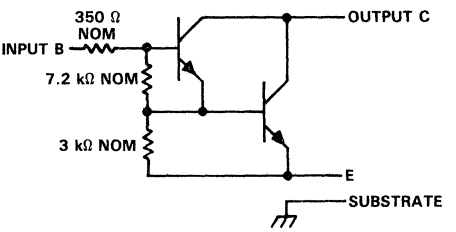
The ULN2074 and ULN2075 are monolithic, quadruple, high-voltage, high-current n-p-n darlington-transistor amplifier devices. They feature high-voltage outputs with collector-current ratings of 1.5 A for each Darlington pair.

The ULN2074 and ULN2075 are unique general-purpose devices, each featuring uncommitted collectors and emitters to allow for either sinking or sourcing the output current. These devices offer the system designer the flexibility of tailoring the circuit to the application. Typical applications include logic buffers, relay drivers, lamp drivers, and hammer drivers.

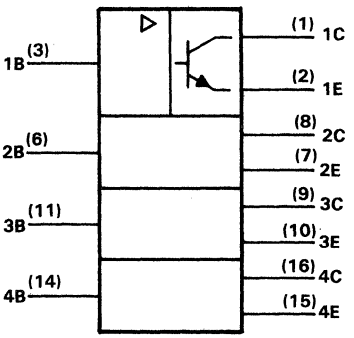
For proper operation, the substrate must be connected to the most negative voltage.

The ULN2074 and ULN2075 are characterized for operation from −20°C to 85°C.

schematic (each switch)



logic symbol†



‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings at 25°C free-air temperature for each switch (unless otherwise noted)

	ULN2074	ULN2075	UNIT
Collector-emitter voltage	50	80	V
Input voltage with respect to substrate	30	60	V
Peak collector current (see Figures 9, 10, and 11)	1.5	1.5	A
Input current	25	25	mA
Total power dissipation at (or below) 25°C free-air temperature (see Note 1)	2075	2075	mW
Operating free-air temperature range	−20 to 85	−20 to 85	°C
Storage temperature range	−55 to 150	−55 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds	260	260	°C

NOTE 1: For operation above 25°C free-air temperature, derate total power linearly to 1079 mW at 85°C at the rate of 16.6 mW/°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	ULN2074		ULN2075		UNIT
				MIN	MAX	MIN	MAX	
$V_{CEX(sus)}$	Collector sustaining voltage	1	V_I = 0.4 V, I_C = 100 mA	35		50		V
I_{CEX}	Collector output cutoff current	2	V_{CE} = 50 V		100			μA
			V_{CE} = 50 V, T_A = 70°C		500			
			V_{CE} = 80 V				100	
			V_{CE} = 80 V, T_A = 70°C				500	
$I_{I(on)}$	On-state input current	3	V_I = 2.4 V	2	4.3	2	4.3	mA
			V_I = 3.75 V	4.5	9.6	4.5	9.6	
$V_{I(on)}$	On-state input voltage	4	V_{CE} = 2 V, I_C = 1 A		2		2	V
			V_{CE} = 2 V, I_C = 1.5 A, See Note 2		2.5		2.5	
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 625 μA, I_C = 500 mA		1.1		1.1	V
			I_I = 935 μA, I_C = 750 mA		1.2		1.2	
			I_I = 1.25 mA, I_C = 1 A		1.3		1.3	
			I_I = 2 mA, I_C = 1.25 A, See Note 2		1.4			
			I_I = 2.25 mA, I_C = 1.5 A, See Note 2				1.5	

NOTE 2: These parameters must be measured on one output at a time using pulse techniques, t_W = 10 ms, duty cycle ≤ 10%.

switching characteristics at 25°C free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 6			1	μs
t_{PHL}	Propagation delay time, high-to-low-level output				1.5	μs

PARAMETER MEASUREMENT INFORMATION

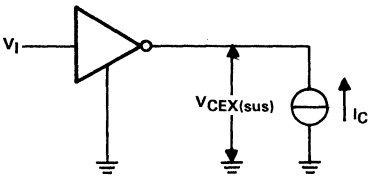


FIGURE 1. $V_{CEX(sus)}$

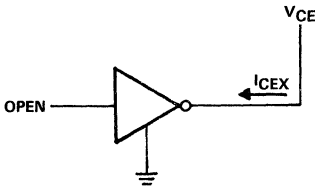


FIGURE 2. I_{CEX}

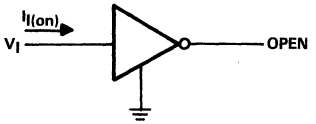


FIGURE 3. $I_{I(on)}$

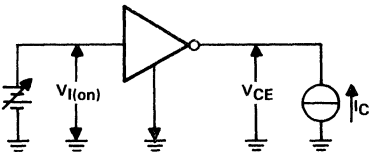


FIGURE 4. $V_{I(on)}$

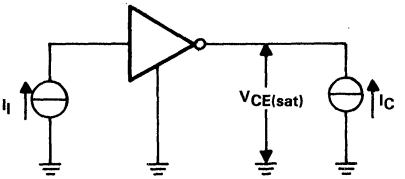
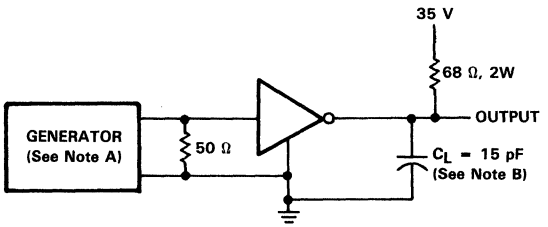
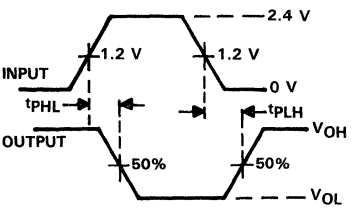


FIGURE 5. $V_{CE(sat)}$



TEST CIRCUITS



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, Z_O = 50 Ω.
B. C_L includes all probe and stray capacitance.

FIGURE 6. SWITCHING CHARACTERISTICS

ELECTRICAL CHARACTERISTICS

INPUT CURRENT
vs
INPUT VOLTAGE

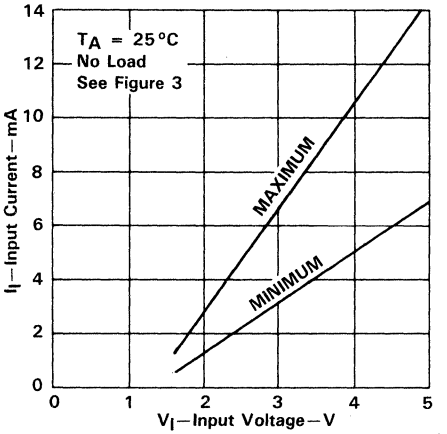


FIGURE 7

COLLECTOR CURRENT
vs
BASE CURRENT

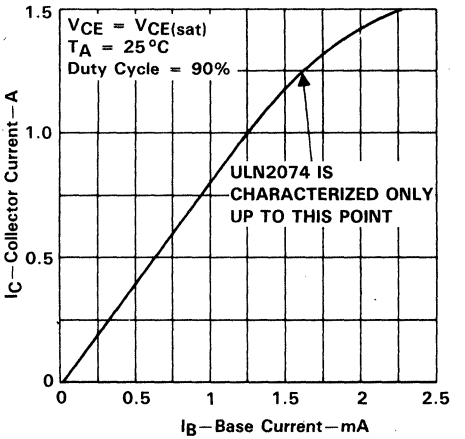


FIGURE 8

THERMAL INFORMATION

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

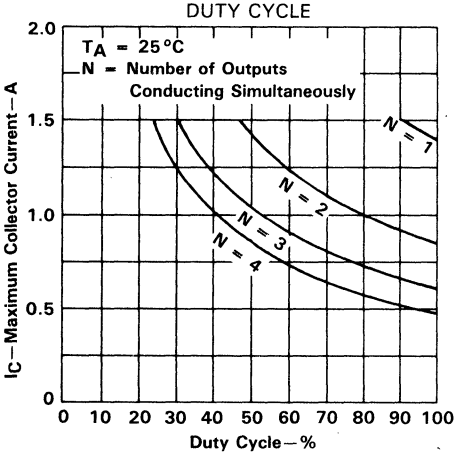


FIGURE 9

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

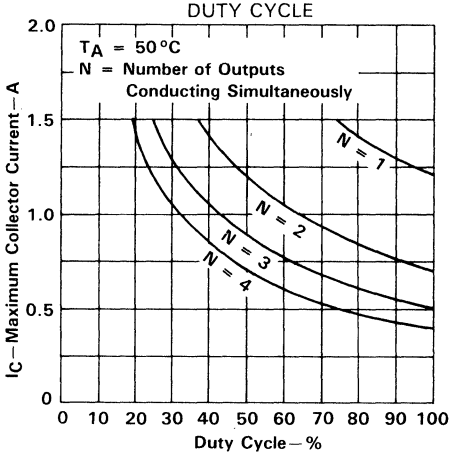


FIGURE 10

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

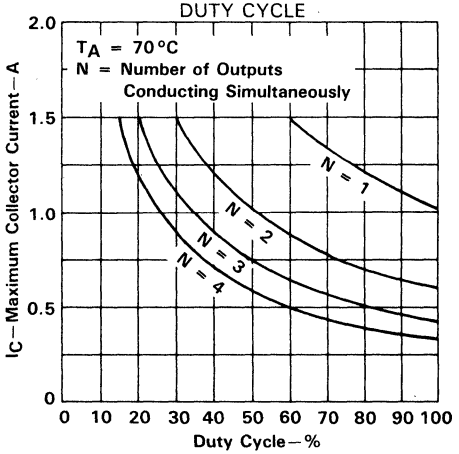


FIGURE 11

APPLICATION INFORMATION

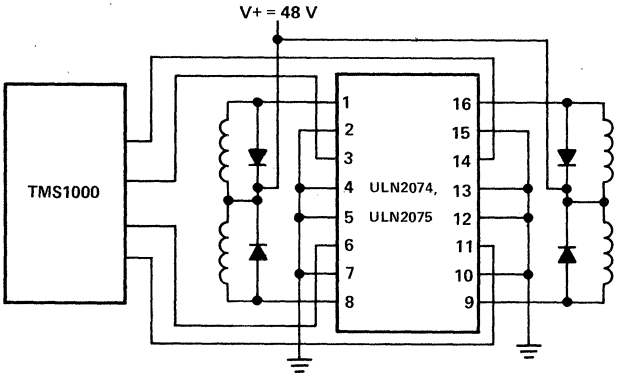


FIGURE 12. RELAY DRIVER INTERFACE WITH EXTERNAL CLAMP DIODES

Contents

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as explained in the following example.

EXAMPLE: SN 75189 N -00

Prefix

MUST CONTAIN TWO, THREE, OR FOUR LETTERS

SN . . . TI Special Functions or Interface Products
TCM . . . . . TI Telecommunication Products
TL . . . . . TI Linear Products
TPIC . . . . . TI Intelligent Power Products

STANDARD SECOND-SOURCE PREFIXES

AM, DP, or DS . . . . . National
LT . . . . . Linear Technology
MAX . . . . . Maxim Integrated Products
MC . . . . . Motorola
N8T . . . . . Signetics
uA . . . . . Fairchild/National

Unique Circuit Description

MUST CONTAIN THREE TO EIGHT CHARACTERS
(From Individual Data Sheets)

Examples: 232 75160B
3695 75C1154
75115 75ALS180

Package

MUST CONTAIN ONE OR TWO LETTERS

D, DB, DW, FD, FK, FN, FT, HA, HB, J, JD, JG, KN, KV, N, NE, NT, P, W
(From Pin-Connection Diagrams on Individual Data Sheet)

Instructions (Dash No.)

MUST CONTAIN TWO NUMBERS

-00 No special instructions
-10 Solder-dipped leads (N, NE, and NT packages only)

Circuits are shipped in one of the carriers below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier.

Dual-In-Line (D, DB, DW, J, JD, JG, N, NE, NT, P)
— Slide Magazines
— A-Channel Plastic Tubing
— Sectioned Cardboard Box
— Individual Cardboard Box

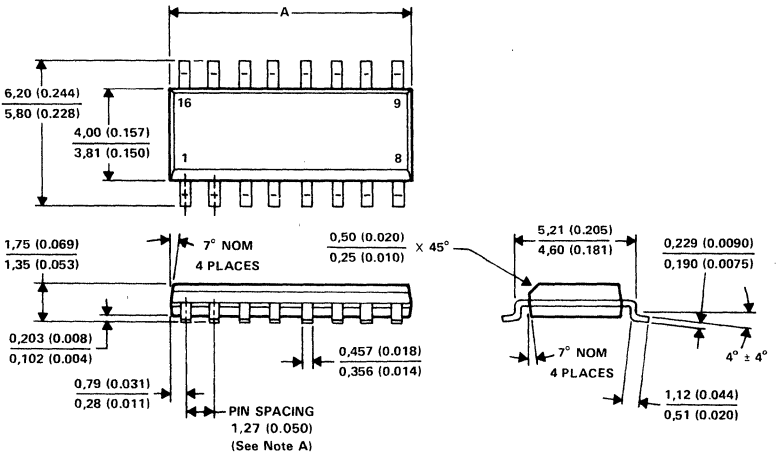
Chip Carrier (FD, FK, FN, FT)
— Anti-Static Plastic Tubing
Flat (HA, HB, W)
— Wells Carrier

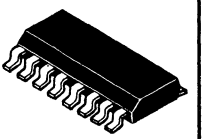
Power Tab (KN, KV)
— Sleeves

D008, D014, and D016 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D008, D014, and D016
(16-pin package used for illustration)





DIM \ PINS	8	14	16
A MIN	4,80 (0.189)	8,55 (0.337)	9,80 (0.386)
A MAX	5,00 (0.197)	8,74 (0.344)	10,00 (0.394)

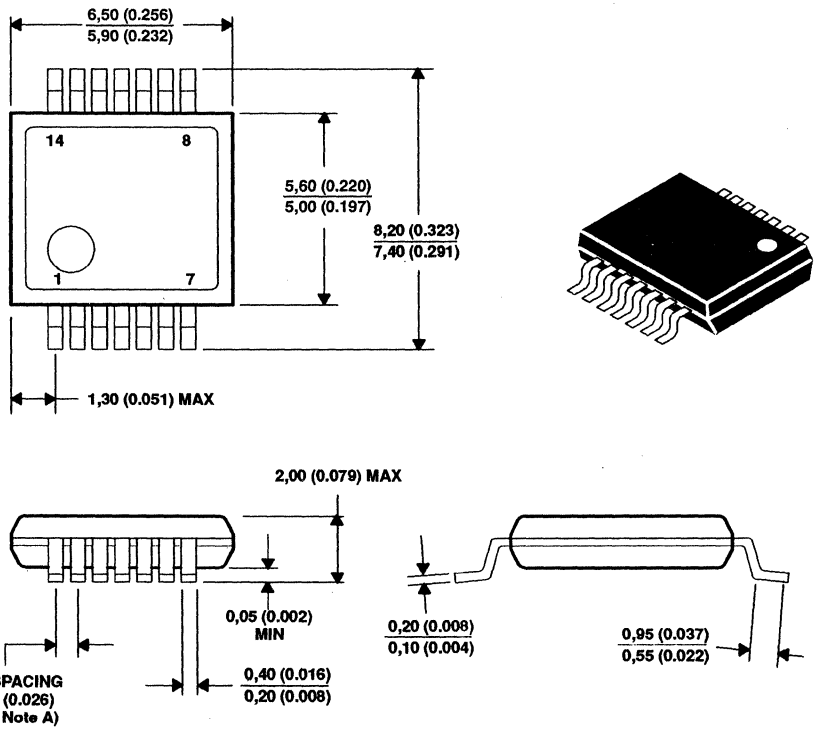
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

DB014 "shrunk small outline" package

This "shrunk small outline" package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DB014



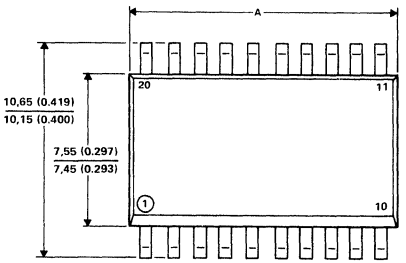
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

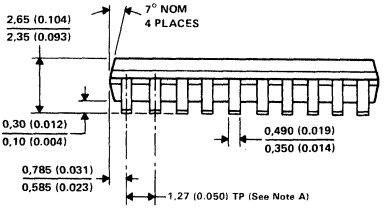
NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

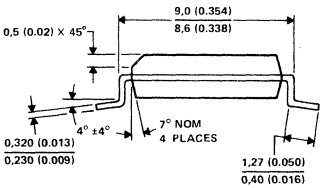
DW016, DW020, DW024, and DW028 plastic "small outline" packages

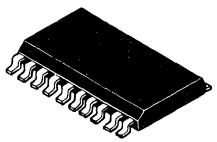
Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DW016, DW020, DW024, and DW028
(20-pin package used for illustration)









DIM \ PINS	16	20	244	28†
A MIN	10,16 (0.400)	12,70 (0.500)	15,29 (0.602)	17,68 (0.696)
A MAX	10,36 (0.408)	12,90 (0.508)	15,49 (0.610)	17,88 (0.704)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

†The 28-pin package drawing is presently classified as Advance Information.

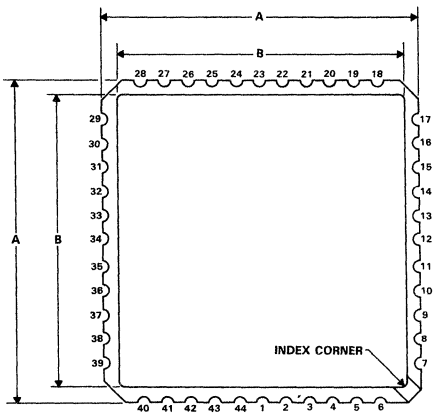
NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

FD020, FD028, FD044, FD052, FD068, FD084, and FK020, FK028, FK044, FK052, FK068, FK084 leadless ceramic chip carrier packages

Each of these hermetically sealed chip charrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder leads on 1,27 (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC standards, 1, 2, and 11.

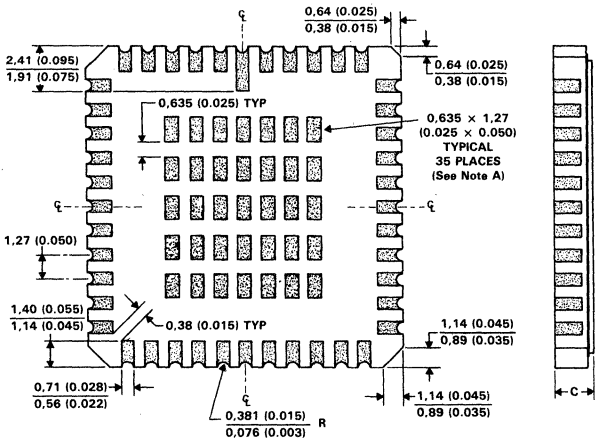
FD020, FD028, FD044, FD052, FD068, FD084,
FK020, FK028, FK044, FK052, FK068, FK084



CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MAX	C MIN	C MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	9,09 (0.358)	1,63 (0.064)	2,03 (0.080)
MS004CC	28	11,23 (0.422)	11,63 (0.458)	11,63 (0.458)	1,63 (0.064)	2,03 (0.080)
MS004CD	44	16,26 (0.640)	16,76 (0.660)	14,22 (0.560)	1,75 (0.069)	3,05 (0.120)
MS004CE	52	18,78 (0.739)	19,33 (0.761)	14,22 (0.560)	2,08 (0.082)	3,05 (0.120)
MS004CF	68	28,83 (0.938)	24,43 (0.962)	21,89 (0.862)	2,08 (0.082)	3,05 (0.120)
MS004CG	84	28,83 (1.135)	29,59 (1.165)	27,05 (1.065)	2,08 (0.082)	3,05 (0.120)

*All dimensions and notes for the specified JEDEC outline apply to the FK package.



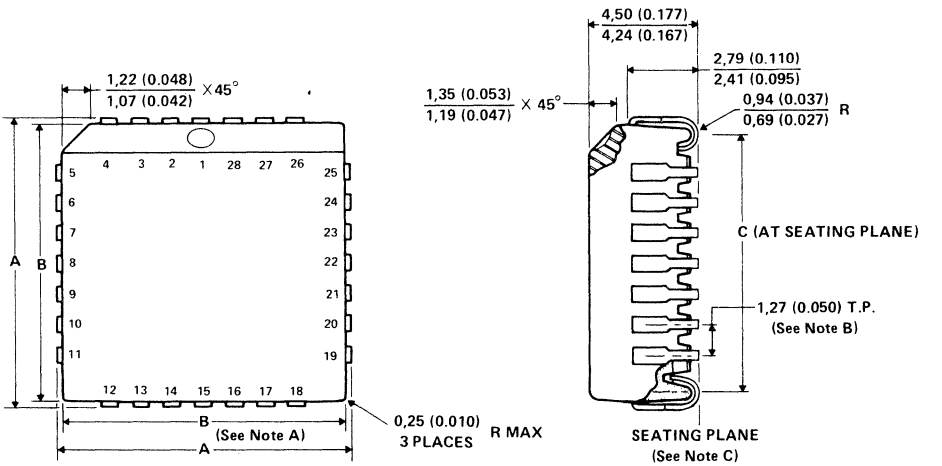
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: The checkerboard pattern is aligned vertically with the contact pads and is symmetrical horizontally as shown; it is applicable to some 44-terminal packages only.

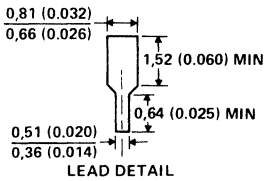
FN020, FN028, FN044, FN068, and FN084 plastic chip carrier packages

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN020, FN028, FN044, FN068, and FN084
(28-terminal package used for illustration)



NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
20	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,87 (0.310)	8,38 (0.330)
28	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,41 (0.410)	10,92 (0.430)
44	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,49 (0.610)	16,00 (0.630)
68	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.956)	23,11 (0.910)	23,62 (0.930)
84	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.158)	27,69 (1.090)	28,70 (1.130)



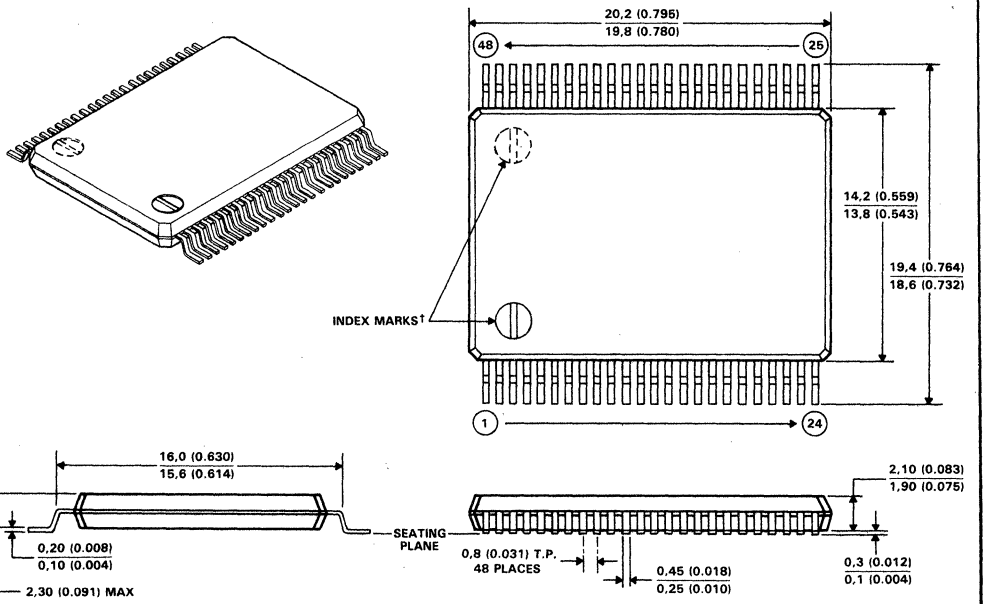
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by dimension B.
B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.
C. The lead contact points are planar within 0,10 (0.004).

FT048

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

FT048



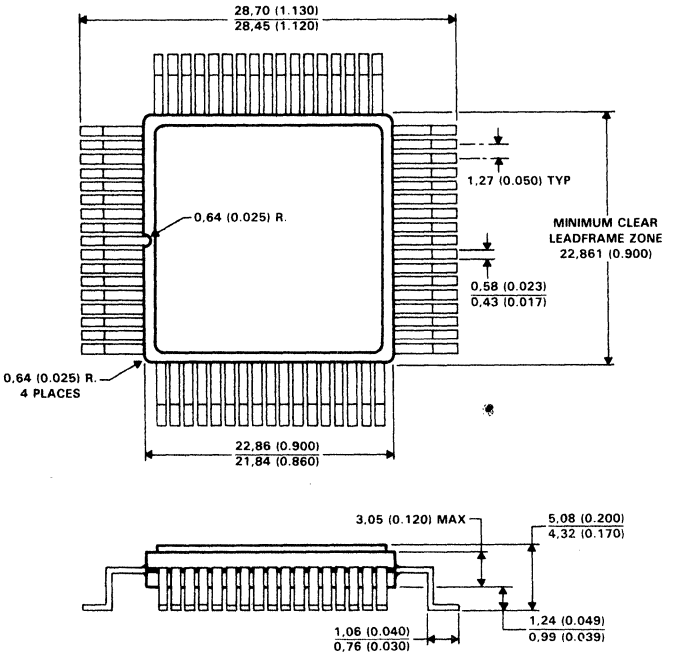
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† There are two versions of the 48-lead FT package that differ in the position of the index mark in the top view. In one version, the mark is near lead 3, in the other version, it is near lead 46. Consult the individual data sheet to see which applies for a particular device type.

HA068 quadriform flat package

The 68-pin HA package is housed in a quadriform flat package. It is hermetically sealed with 0.05-inch-lead spacing configured with gull-wing bent leads for surface mounting capability.

HA068

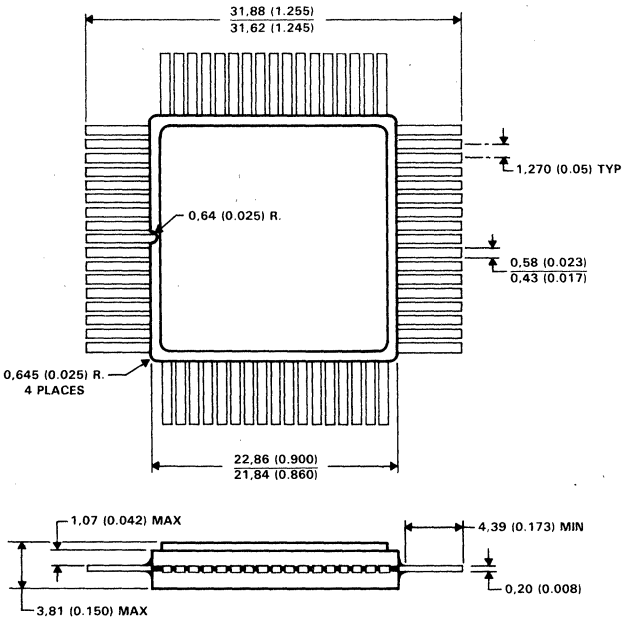


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

HB068 quadriform flat package

The 68-pin HB package is housed in a quadriform flat package. It is hermetically sealed with 0.05-inch-lead spacing configured with straight leads for surface mounting capability.

HB068



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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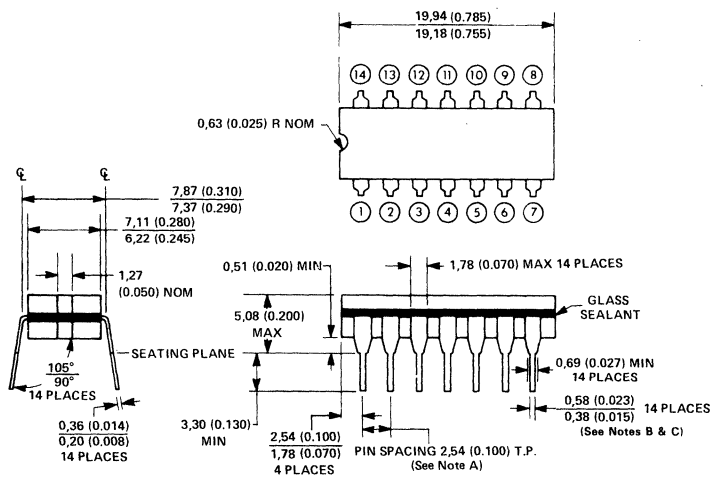
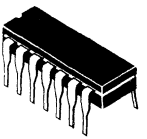
J014 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

J014





Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

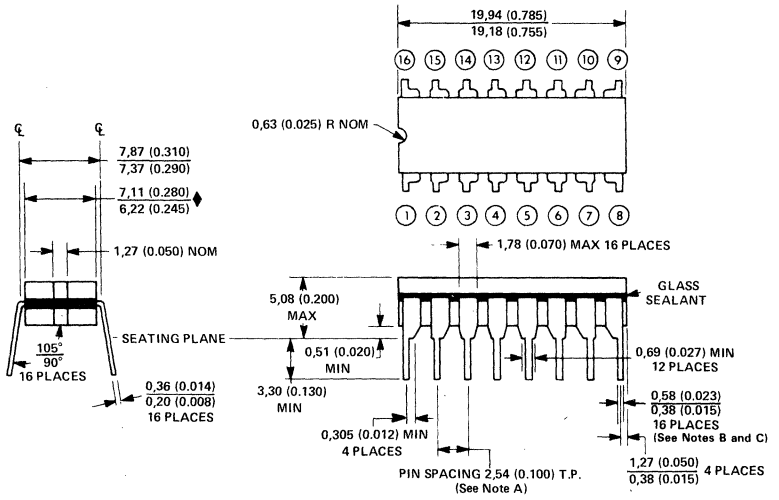
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

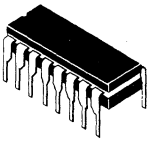
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

J016 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

J016





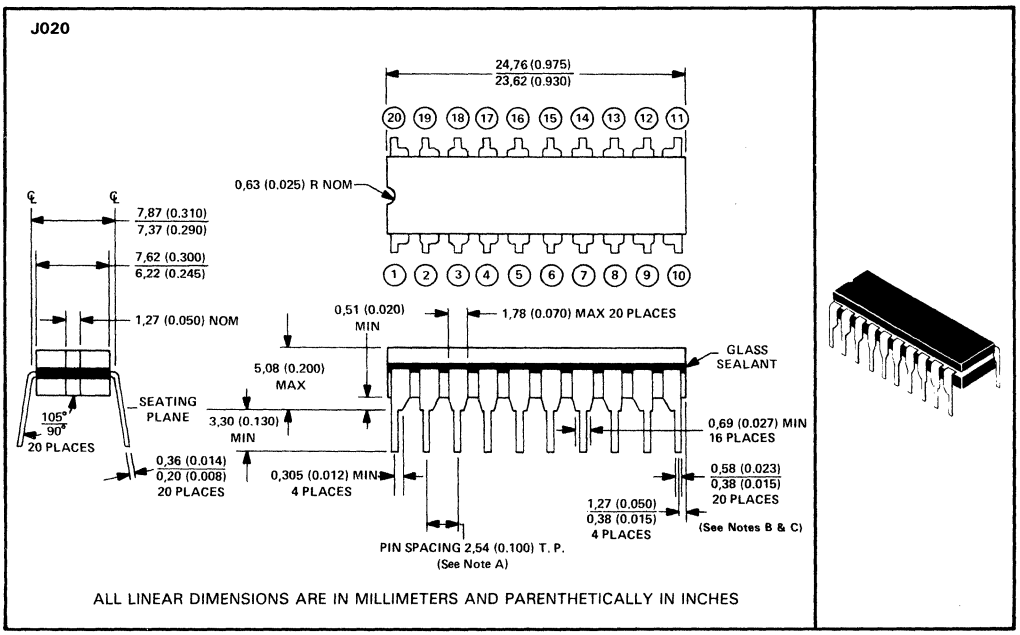
♦ For memories of 64 bits and up, a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, and complex HCMOS parts, this maximum is 7,62 (0.300). All other dimensions apply without modification.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

J020 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

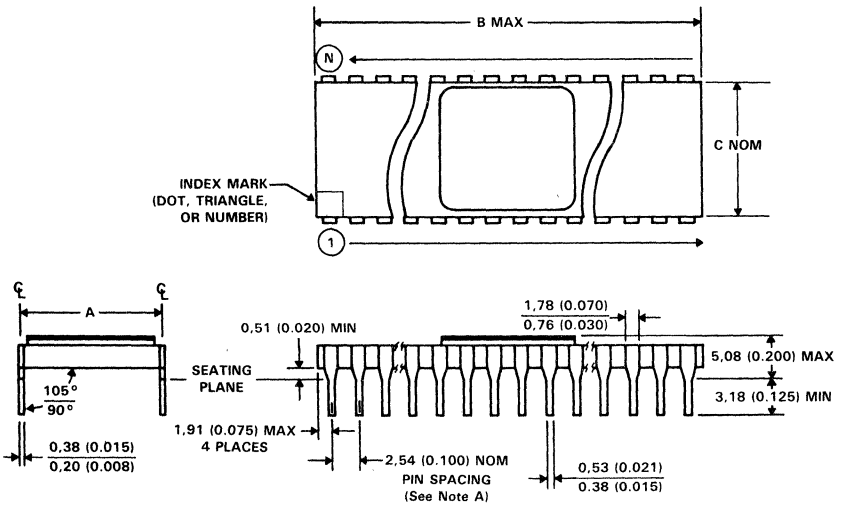


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

JD ceramic side-braze dual-in-line packages

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.

JD CERAMIC—SIDE-BRAZE



DIM \ PINS (N)	16	18	20	22	24
A +0,51 (+0.020) −0,25 (−0.010)	7,62 (0.300)	7,62 (0.300)	7,62 (0.300)	10,16 (0.400)	7,62 (0.300)
B (MAX)	20,57 (0.810)	23,11 (0.910)	25,65 (1.010)	27,94 (1.100)	30,86 (1.215)
C (NOM)	7,37 (0.290)	7,37 (0.290)	7,37 (0.290)	9,91 (0.390)	7,37 (0.290)

DIM \ PINS (N)	24	28	40	48	52	64
A +0,51 (+0.020) −0,25 (−0.010)	15,24 (0,600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	22,86 (0.900)
B (MAX)	31,8 (1.250)	36,8 (1,450)	52,1 (2.050)	62,2 (2.450)	67,3 (2.650)	82,6 (3.250)
C (NOM)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	22,6 (0.890)

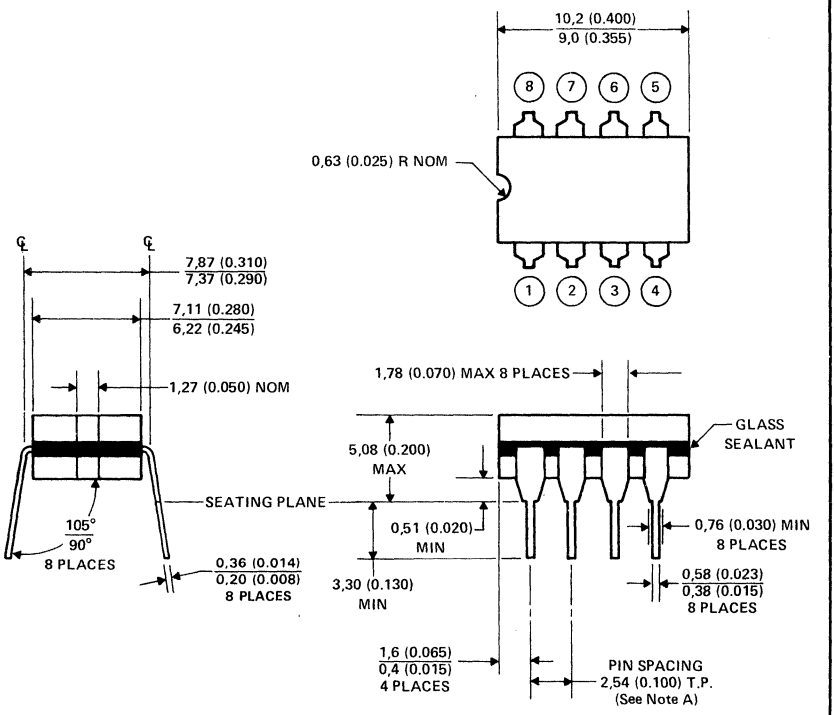
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

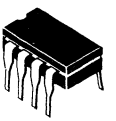
JG008 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and an 8-pin lead frame. The package is intended for insertion in mounting-hole rows 7,62 (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering.

JG008



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

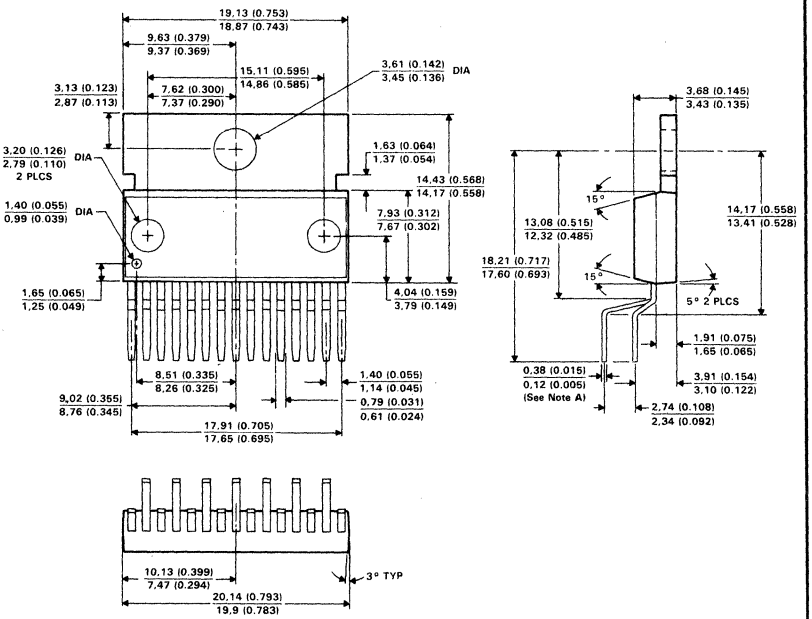


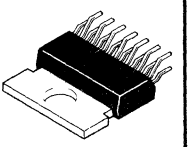
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

KN015 plastic flange-mount package

This package comprises a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.

KN015





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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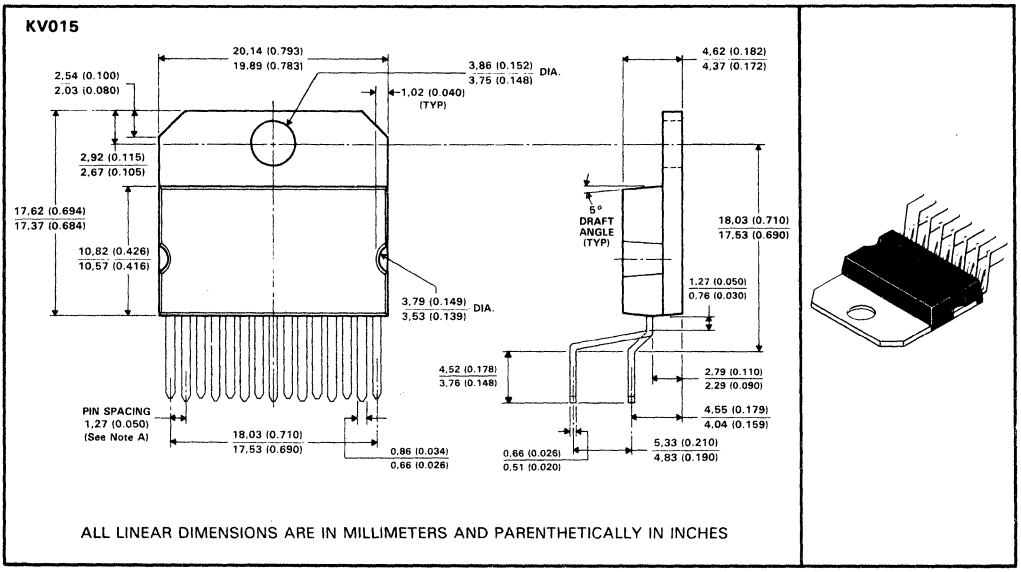
KV015 plastic package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.

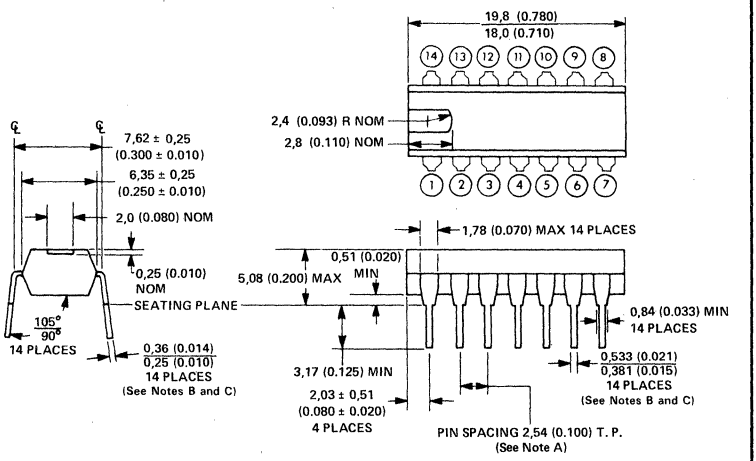


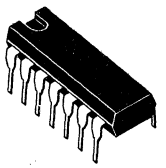
NOTE A: Leads are within 0,36 (0.014) radius of true position (T.P.) at maximum material conditions.

N014 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N014





Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

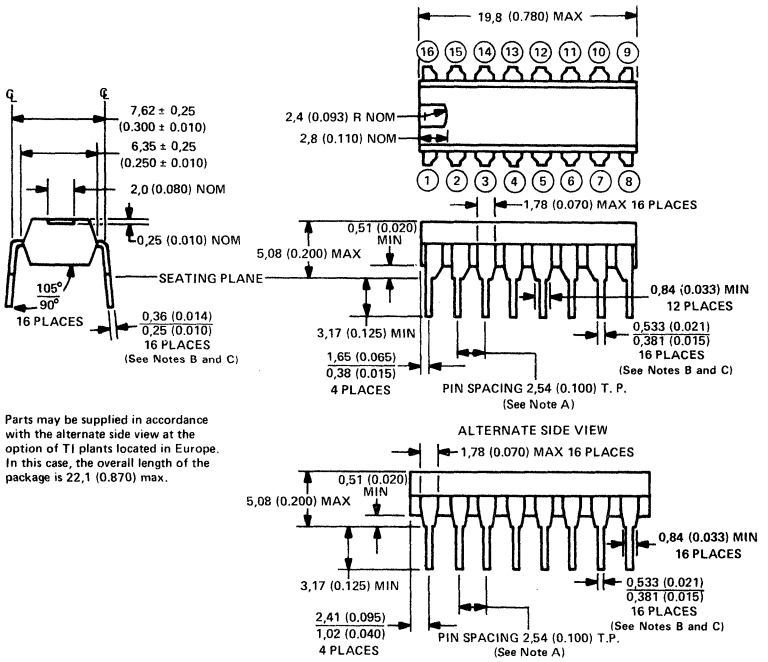
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

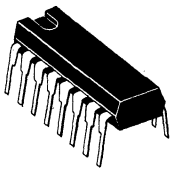
N016 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N016



Parts may be supplied in accordance with the alternate side view at the option of TI plants located in Europe. In this case, the overall length of the package is 22,1 (0.870) max.



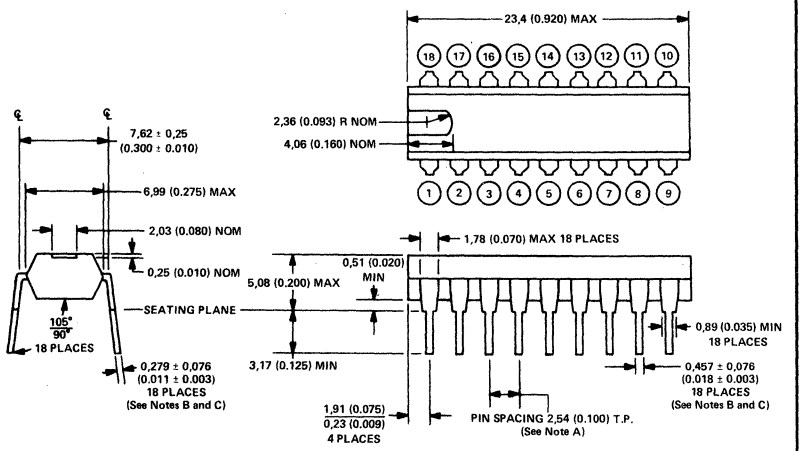
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

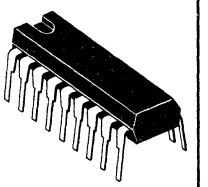
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N018 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N018





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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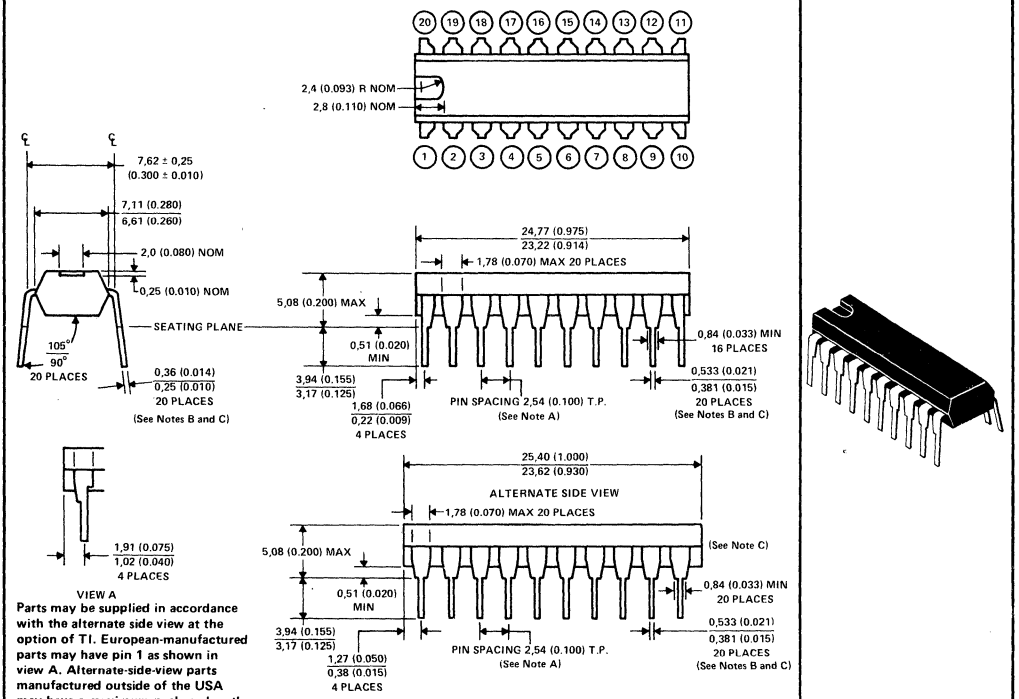
N020 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N020



Parts may be supplied in accordance with the alternate side view at the option of TI. European-manufactured parts may have pin 1 as shown in view A. Alternate-side-view parts manufactured outside of the USA may have a maximum package length of 26,7 (1.050).

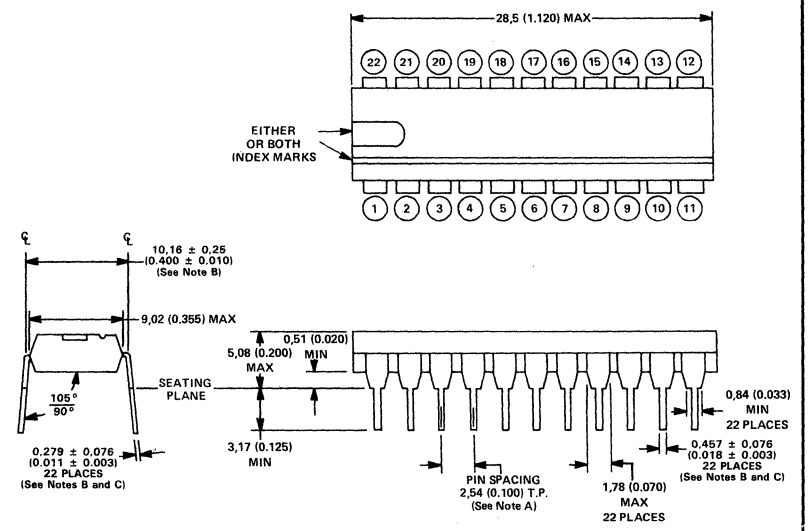
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

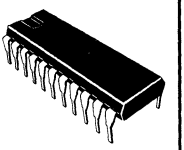
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N022 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 10,16 (0.400) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N022





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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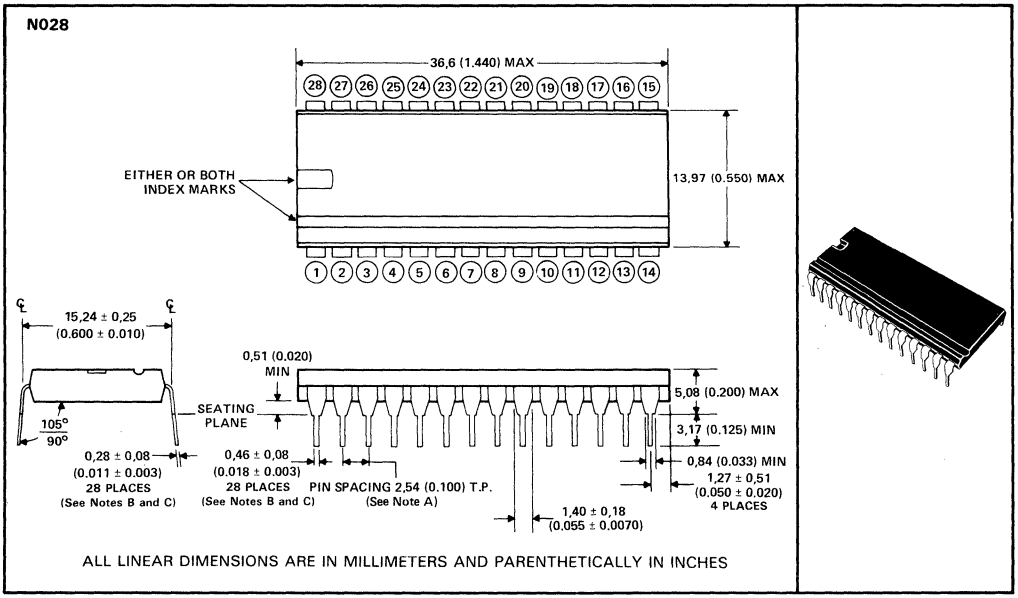
N028 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

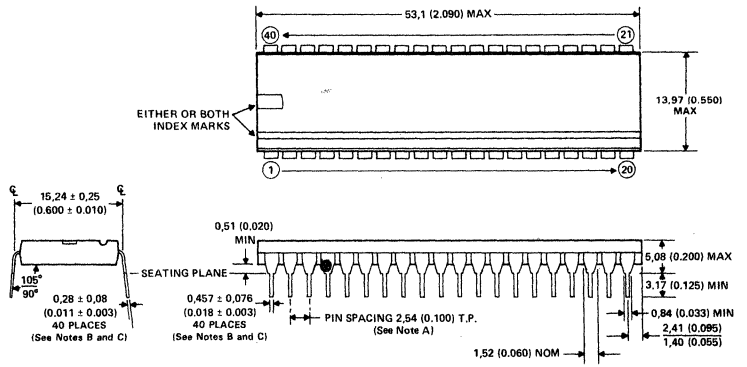


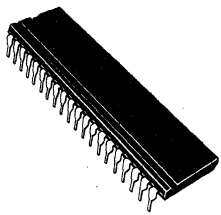
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N040 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N040





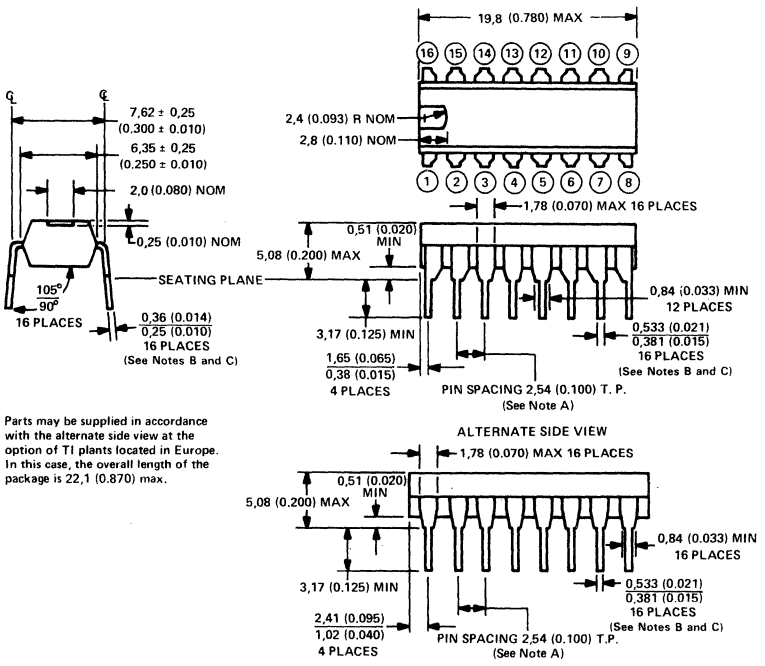
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

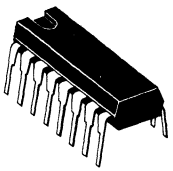
NE016 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a 16-pin lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. For better heat dissipation there are internal tabs connecting the two central leads on each side of the 16-pin package. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NE016



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

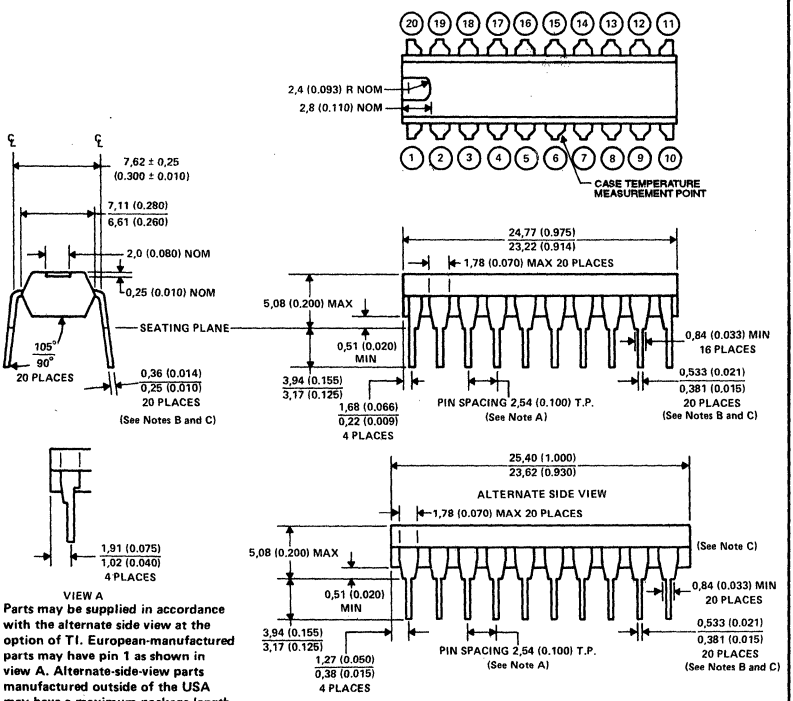


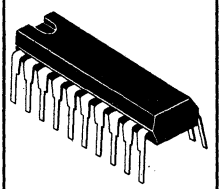
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NE020 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. For better heat dissipation there are internal tabs connecting the two central leads on each side of the 20-pin package. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NE020





Parts may be supplied in accordance with the alternate side view at the option of TI. European-manufactured parts may have pin 1 as shown in view A. Alternate-side-view parts manufactured outside of the USA may have a maximum package length of 26,7 (1.050).

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

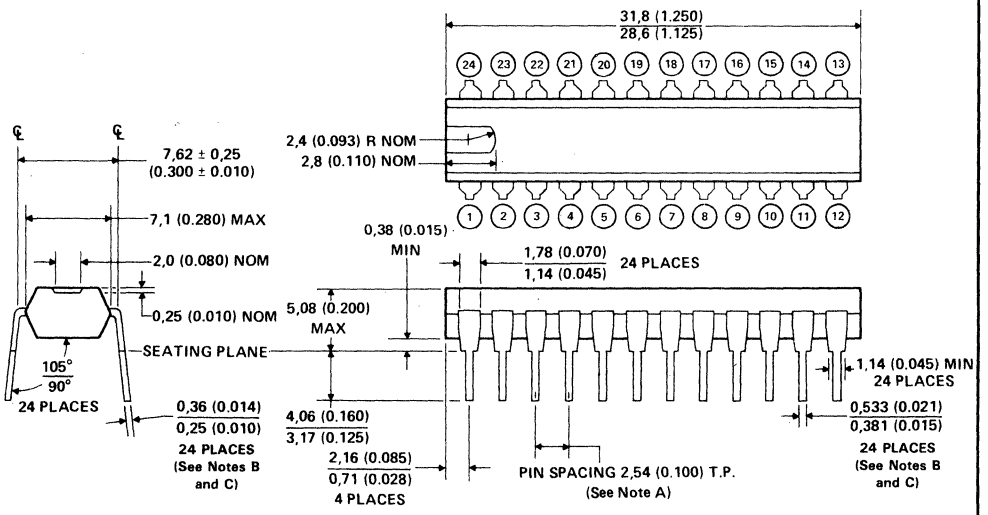
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NT024 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

NT024



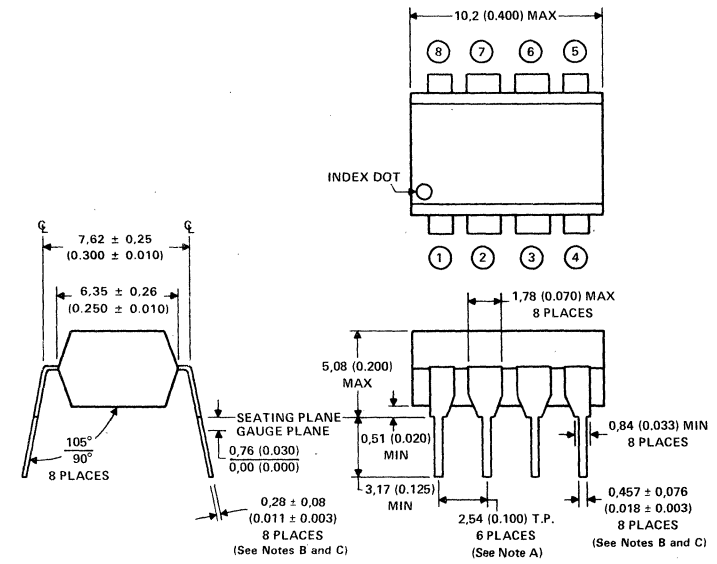
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

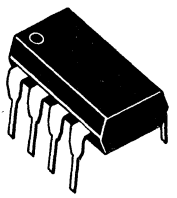
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

P008 dual-in-line plastic package

This package consists of a circuit mounted on an 8-pin lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers (See Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-plated leads require no additional cleaning or processing when used in soldered assembly.

P008



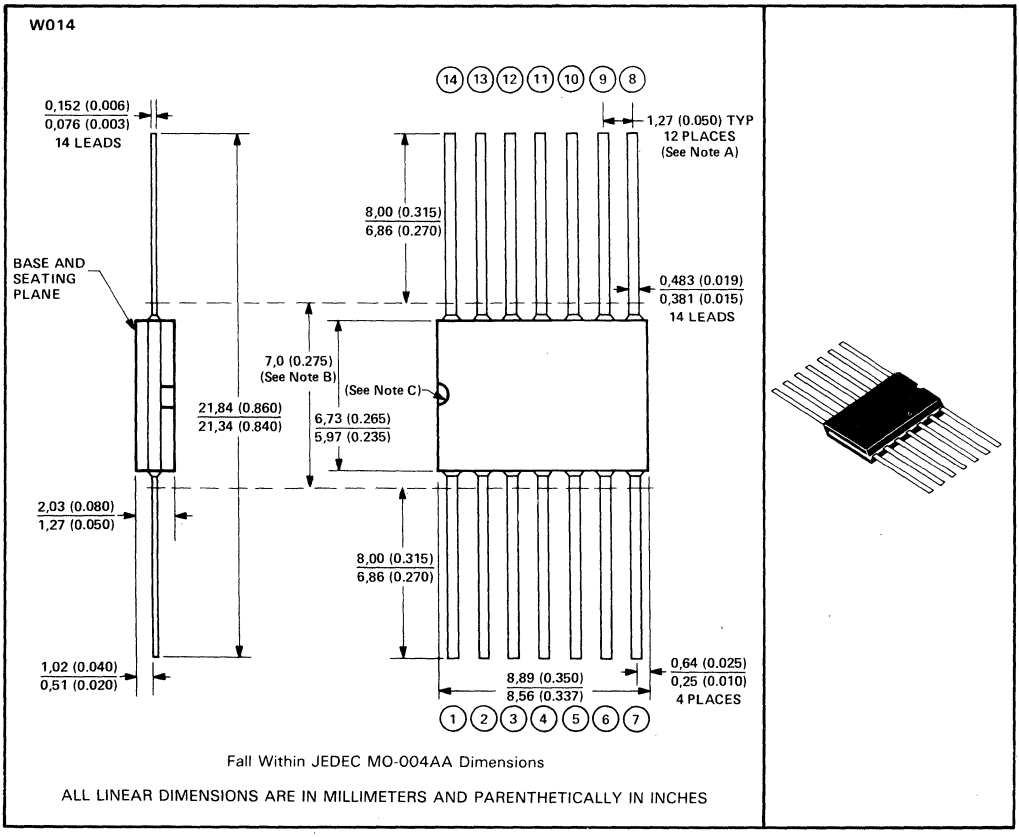


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

W014 ceramic flat package

This hermetically sealed flat package consists of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condition.
B. This dimension determines a zone within which all body and lead irregularities lie.
C. Index point is provided on cap for terminal identification only.

Explanation of Logic Symbols

by F.A. Mann

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List of Illustrations

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IEEE Standards may be purchased from:

Institute of Electrical and Electronics Engineers, Inc.
IEEE Standards Office
345 East 47th Street
New York, N.Y. 10017

International Electrotechnical Commission (IEC) publications may be purchased from:

American National Standards Institute, Inc.
1430 Broadway
New York, N.Y. 10018

1 Introduction

The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be explained in Section 4.

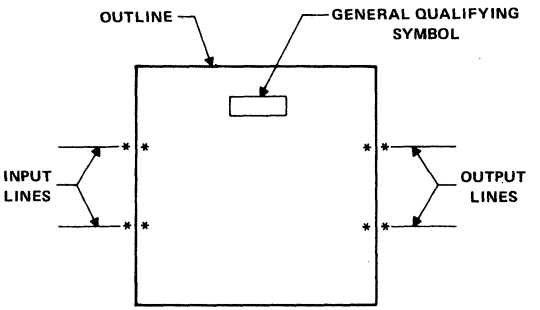
The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

Internationally, Working Group 2 of IEC Technical Committee TC-3 has prepared a new document (Publication 617-12) that consolidates the original work started in the mid 1960's and published in 1972 (Publication 117-15) and the amendments and supplements that have followed. Similarly for the USA, IEEE Committee SCC 11.9 has revised the publication IEEE Std 91/ANSI Y32.14. Now numbered simply ANSI/IEEE Std 91-1984, the IEEE standard contains all of the IEC work that has been approved, and also a small amount of material still under international consideration. Texas Instruments is participating in the work of both organizations and this document introduces new logic symbols in accordance with the new standards. When changes are made as the standards develop, future editions will take those changes into account.

The following explanation of the new symbolic language is necessarily brief and greatly condensed from what the standards publications now contain. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in this data book and is somewhat briefer than the explanation that appears in several of TI's data books on digital logic. However, it includes a new section (6.0) that explains several symbols for actual devices in detail. This has proven to be a powerful learning aid.

2 Symbol Composition

A symbol comprises an outline or a combination of outlines together with one or more qualifying symbols. The shape of the symbols is not significant. As shown in Figure 1, general qualifying symbols are used to tell exactly what logical operation is performed by the elements. Table 1 shows general qualifying symbols defined in the new standards. Input lines are placed on the left and output lines are placed on the right. When an exception is made to that convention, the direction of signal flow is indicated by an arrow as shown in Figure 9.



*Possible positions for qualifying symbols relating to inputs and outputs

Figure 1. Symbol Composition

3 Qualifying Symbols

3.1 General Qualifying Symbols

Table 1 shows general qualifying symbols defined by ANSI/IEEE Standard 91. These characters are placed near the top center or the geometric center of a symbol or symbol element to define the basic function of the device represented by the symbol or of the element.

X/Y is the general qualifying symbol for identifying coders, code converters, and level converters. X and Y may be used in their own right to stand for some code or either or both may be replaced by some other indication of the code or level such as BCD or TTL. As might be expected, interface circuits make frequent use of this set of qualifying symbols.

Table 1. General Qualifying Symbols

SYMBOL	DESCRIPTION
&	AND gate or function
≥1	OR gate or function. The symbol was chosen to indicate that at least one active input is needed to activate the output.
=1	Exclusive OR. One and only one input must be active to activate the output.
1	A simple 1-input gate or element
▷ or ◁	A buffer or element with more than usual output capability (symbol is oriented in the direction of signal flow).
⎍	Schmitt trigger; element with hysteresis
X/Y	Coder, code converter, level converter
	The following are examples of subsets of this general class of qualifying symbol used in this book.
	BCD/7-SEG — BCD to 7-segment display driver
	TTL/MOS — TTL to MOS level converter
	CMOS/PLASMA DISP — Plasma-display driver with CMOS-compatible inputs
	MOS/LED — Light-emitting-diode driver with MOS-compatible inputs
	CMOS/VAC FLUOR DISP — Vacuum-fluorescent display driver with CMOS-compatible inputs
	CMOS/EL DISP — Electroluminescent display driver with CMOS-compatible inputs
	TTL/GAS DISCH DISPLAY — Gas-discharge display driver with TTL-compatible inputs
SRGm	Shift register. m = number of bits.

3.2 Qualifying Symbols for Inputs and Outputs

Qualifying symbols for inputs and outputs are shown in Table 2 and many will be familiar to most users, a likely exception being the logic polarity symbol for directly indicating active-low inputs and outputs. The older logic negation indicator means that the external 0 state produces the internal 1 state. The internal 1 state means the active state. Logic negation may be used in pure logic diagrams; in order to tie the external 1 and 0 logic states to the levels H (high) and L (low), a statement of whether positive logic (1 = H, 0 = L) or negative logic (1 = L, 0 = H) is being used is required or must be assumed. Logic polarity indicators eliminate the need for calling out the logic convention and are used in this data book in the symbology for actual devices. The presence of the triangle polarity indicator indicates that the L logic level will produce the internal 1 state (the active state) or that, in the case of an output, the internal 1 state will produce the external L level. Note how the active direction of transition for a dynamic input is indicated in positive logic, negative logic, and with polarity indication.

When nonstandardized information is shown inside an outline, it is usually enclosed in square brackets [like these]. The square brackets are omitted when associated with a nonlogic input, which is indicated by an X superimposed on the connection line outside the symbol.

Table 2. Qualifying Symbols for Inputs and Outputs


Logic negation at input. External 0 produces internal 1.


Logic negation at output. Internal 1 produces external 0.


Active-low input. Equivalent to  in positive logic

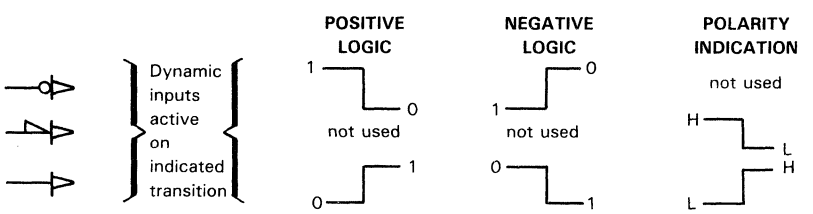

Active-low output. Equivalent to  in positive logic


Active-low input in the case of right-to-left signal flow


Active-low output in the case of right-to-left signal flow


Signal flow from right to left. If not otherwise indicated, signal flow is from left to right.


Bidirectional signal flow




Nonlogic connection. A label inside the symbol will usually define the nature of this pin.


Input for analog signals (on a digital symbol) (see Figure 11)


Input for digital signals (on an analog symbol) (see Figure 11)

3.3 Symbols Inside the Outline

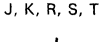
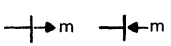
Table 3 shows some symbols used inside the outline. Note particularly that open-collector (open-drain), open-emitter (open-source), and three-state outputs have distinctive symbols. Also note that an EN input affects all of the outputs of the element and has no effect on inputs. An EN input affects all the external outputs of the element in which it is placed, plus the external outputs of any elements shown to be influenced by that element. It has no effect on inputs. When an enable input affects only certain outputs, affects outputs located outside the indicated influence of the element in which the enable input is placed, and/or affects one or more inputs, a form of dependency notation will indicate this (see 4.9). The effects of the EN input on the various types of outputs are shown.

It is particularly important to note that a D input is always the data input of a storage element. At its internal 1 state, the D input sets the storage element to its 1 state, and at its internal 0 state it resets the storage element to its 0 state.

The binary grouping symbol will be explained more fully in Section 6.11. Binary-weighted inputs are arranged in order and the binary weights of the least significant and the most significant lines are indicated by numbers. In this document weights of input and output lines will be represented by powers of two usually only when the binary grouping symbol is used, otherwise decimal numbers will be used. The grouped inputs generate an internal number on which a mathematical function can be performed or that can be an identifying number for dependency notation. This number is the sum of the weights ($1, 2, 4 \ldots 2^n$) of those input standing at their 1 states. A frequent use is in addresses for memories.

Reversed in direction, the binary grouping symbol can be used with outputs. The concept is analogous to that for the inputs and the weighted outputs will indicate the internal number assumed to be developed within the circuit.

Table 3. Symbols Inside the Outline

	Bithreshold input (input with hysteresis)
	N-P-N open-collector or similar output that can supply a relatively low-impedance L level when not turned off. Requires external pull-up. Capable of positive-logic wired-AND connection.
	Passive-pull-up output is similar to N-P-N open-collector output but is supplemented with a built-in passive pull-up.
	N-P-N open-emitter or similar output that can supply a relatively low-impedance H level when not turned off. Requires external pull-down. Capable of positive-logic wired-OR connection.
	Passive-pull-down output is similar to N-P-N open-emitter output but is supplemented with a built-in passive pull-down.
	3-state output
	Output with more than usual output capability (symbol is oriented in the direction of signal flow).
	Enable input When at its internal 1-state, all outputs are enabled. When at its internal 0-state, open-collector, open-emitter outputs, and three-state outputs at external high-impedance state, and all other outputs (i.e., totem-poles) are at the internal 0-state.
J, K, R, S, T	Usual meanings associated with flip-flops (e.g., R = reset, T = toggle)
	Data input to a storage element equivalent to: 
	Shift right (left) inputs, m = 1, 2, 3, etc. If m = 1, it is usually not shown.
	Binary grouping. m is highest power of 2. Produces a number equal to the sum of the weights of the active inputs
	Input line grouping . . . indicates two or more terminals used to implement a single logic input. e.g., differential inputs.

3.4 Combinations of Outlines and Internal Connections

When a circuit has one or more inputs that are common to more than one element of the circuit, the common-control block may be used. This is the only distinctively shaped outline used in the IEC system. Figure 2 shows that unless otherwise qualified by dependency notation, an input to the common-control block is an input to each of the elements below the common-control block.

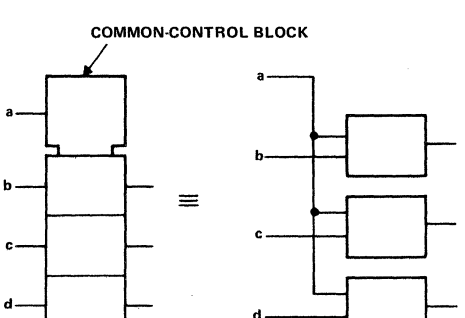


Figure 2. Common-Control Block

The outlines of elements may be embedded within one another or abutted to form complex elements, in which case the following rules apply. There is no logic connection between elements when the line common to their outlines is in the direction of signal flow. There is at least one logic connection when the line common to two outlines is perpendicular to the direction of signal flow. If no indications are shown on either side of the common line, it is assumed that there is only one logic connection. If more than one internal connection exists between adjacent elements, the number of connections will be clarified by the use of one or more of the internal connection symbols from Table 4 and/or appropriate qualifying symbols or dependency notation.

Table 4. Symbols for Internal Connections

	Internal connection. 1 state on left produces 1 state on right.
	Negated internal connection. 1 state on left produces 0 state on right.
	Dynamic internal connection. Transition from 0 to 1 on left produces transitory 1 state on right.
	Dynamic internal connection. Transition from 1 to 0 on left produces transitory 1 state on right.

Table 4 shows symbols that are used to represent internal connection with specific characteristics. The first is a simple noninverting connection, the second is inverting, the third is dynamic. As with this symbol and an external input line, the transition from 0 to 1 on the left produces a momentary 1-state on the right. The fourth symbol is similar except that the active transition on the left is from 1 to 0.

Only logic states, not levels, exist inside symbols. The negation symbol ( ) is used internally even when direct polarity indication ( ) is used externally.

In an array of elements, if the same general qualifying symbol and the same qualifying symbols associated with inputs and outputs would appear inside each of the elements of the array, these qualifying symbols are usually shown only in the first element. This is done to reduce clutter and to save time in recognition. Similarly, large identical elements that are subdivided into smaller elements may each be represented by an unsubdivided outline. The SN75163B symbol (see 6.5) illustrates this principle.

4 Dependency Notation

Some readers will find it more to their liking to skip this section and proceed to the explanation of the symbols for a few actual devices in 6.0. Reference will be made there to various parts of this section as it is needed. If this procedure is followed, it is recommended that 5.0 be read after 6.0 and then all of 4.0 be reread.

4.1 General Explanation

Dependency notation is the powerful tool that sets the IEC symbols apart from previous systems and makes compact, meaningful, symbols possible. It provides the means of denoting the relationship between inputs, outputs, or inputs and outputs without actually showing all the elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function.

In the convention for the dependency notation, use will be made of the terms "affecting" and "affected." In cases where it is not evident which inputs must be considered as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the choice may be made in any convenient way.

So far, eleven types of dependency have been defined but only the eight used in this book are explained. They are listed below in the order in which they are presented and are summarized in Table 5 following 4.10.2.

Section	Dependency Type or Other Subject
4.2	G, AND
4.3	General Rules for Dependency Notation
4.4	V, OR
4.5	N, Negate (Exclusive-OR)
4.6	Z, Interconnection
4.7	X, Transmission
4.8	C, Control
4.9	EN, Enable
4.10	M, Mode

4.2 G (AND) Dependency

A common relationship between two signals is to have them ANDed together. This has traditionally been shown by explicitly drawing an AND gate with the signals connected to the inputs of the gate. The 1972 IEC publication and the 1973 IEEE/ANSI standard showed several ways to show this AND relationship using dependency notation. While ten other forms of dependency have since been defined, the ways to invoke AND dependency are now reduced to one.

In Figure 3 input **b** is ANDed with input **a** and the complement of **b** is ANDed with **c**. The letter G has been chosen to indicate AND relationships and is placed at input **b**, inside the symbol. A number considered appropriate by the symbol designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input **c**.

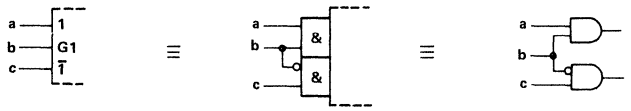


Figure 3. G Dependency Between Inputs

In Figure 4, output **b** affects input **a** with an AND relationship. The lower example shows that it is the internal logic state of **b**, unaffected by the negation sign, that is ANDed. Figure 5 shows input **a** to be ANDed with a dynamic input **b**.

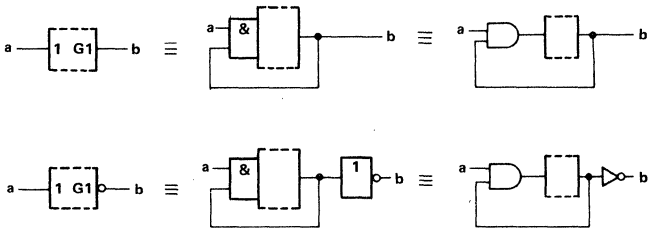


Figure 4. G Dependency Between Outputs and Inputs

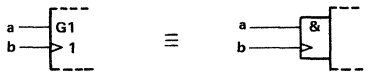


Figure 5. G Dependency with a Dynamic Input

The rules for G dependency can be summarized thus:

When a G*m* input or output (*m* is a number) stands at its internal 1 state, all inputs and outputs affected by G*m* stand at their normally defined internal logic states. When the G*m* input or output stands at its 0 state, all inputs and outputs affected by G*m* stand at their internal 0 states.

4.3 Conventions for the Application of Dependency Notation in General

The rules for applying dependency relationships in general follow the same pattern as was illustrated for G dependency.

Application of dependency notation is accomplished by:

1. Labeling the input (or output) *affecting* other inputs or outputs with the letter symbol indicating the relationship involved (e.g., G for AND) followed by an identifying number, appropriately chosen, and
2. Labeling each input or output *affected* by that affecting input (or output) with that same number.

If it is the complement of the internal logic state of the affecting input or output that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs (Figure 3).

If two affecting inputs or outputs have the same letter and same identifying number, they stand in an OR relationship to each other (Figure 6).

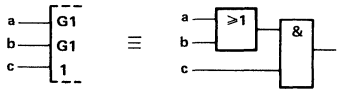


Figure 6. ORed Affecting Inputs

If the affected input or output requires a label to denote its function (e.g., "D"), this label will be *prefixed* by the identifying number of the affecting input (Figure 12).

If an input or output is affected by more than one affecting input, the identifying numbers of each of the affecting inputs will appear in the label of the affected one, separated by commas. The normal reading order of these numbers is the same as the sequence of the affecting relationships (Figure 12).

4.4 V (OR) Dependency

The symbol denoting OR dependency is the letter V (Figure 7).

When a V*m* input or output stands at its internal 1 state, all inputs and outputs affected by V*m* stand at their internal 1 states. When the V*m* input or output stands at its internal 0 state, all inputs and outputs affected by V*m* stand at their normally defined internal logic states.

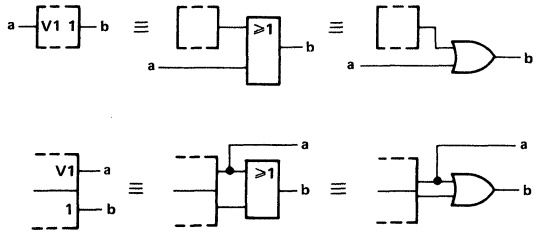


Figure 7. V (OR) Dependency

4.5 N (Negate) (Exclusive-OR) Dependency

The symbol denoting negate dependency is the letter N (Figure 8). Each input or output affected by an N*m* input or output stands in an Exclusive-OR relationship with the N*m* input or output.

When an N*m* input or output stands at its internal 1 state, the internal logic state of each input and each output affected by N*m* is the complement of what it would otherwise be. When an N*m* input or output stands at its internal 0 state, all inputs and outputs affected by N*m* stand at their normally defined internal logic states.

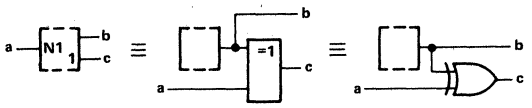


Figure 8. N (Negate) (Exclusive-OR) Dependency

4.6 Z (Interconnection) Dependency

The symbol denoting interconnection dependency is the letter Z.

Interconnection dependency is used to indicate the existence of internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

The internal logic state of an input or output affected by a Z*m* input or output will be the same as the internal logic state of the Z*m* input or output, unless modified by additional dependency notation (Figure 9).

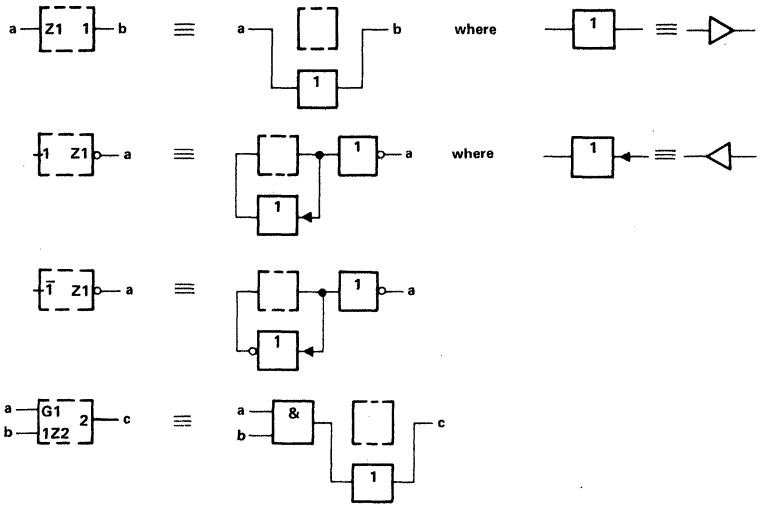


Figure 9. Z (Interconnection) Dependency

4.7 X (Transmission) Dependency

The symbol denoting transmission dependency is the letter X.

Transmission dependency is used to indicate controlled bidirectional connections between affected input/output ports (Figure 10).

When an X*m* input or output stands at its internal 1 state, all input-output ports affected by this X*m* input or output are bidirectionally connected together and stand at the same internal logic state or analog signal level. When an X*m* input or output stands at its internal 0 state, the connection associated with this set of dependency notation does not exist.

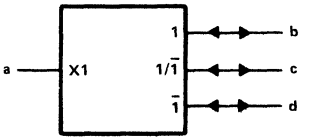


Figure 10. X (Transmission) Dependency

Although the transmission paths represented by X dependency are inherently bidirectional, use is not always made of this property. This is analogous to a piece of wire, which may be constrained to carry current in only one direction. If this is the case in a particular application, then the directional arrows shown in Figures 10 and 11 would be omitted.

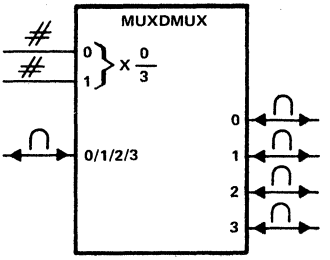


Figure 11. Analog Data Selector (Multiplexer/Demultiplexer)

4.8 C (Control) Dependency

The symbol denoting control dependency is the letter C.

Control inputs are usually used to enable or disable the data (D, J, K, R, or S) inputs of storage elements. They may take on their internal 1 states (be active) either statically or dynamically. In the latter case the dynamic input symbol is used as shown in the second example of Figure 12.

When a C*m* input or output stands at its internal 1 state, the inputs affected by C*m* have their normally defined effect on the function of the element, i.e., these inputs are enabled. When a C*m* input or output stands at its internal 0 state, the inputs affected by C*m* are disabled and have no effect on the function of the element.

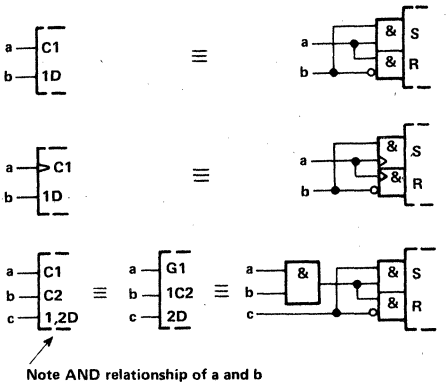


Figure 12. C (Control) Dependency

4.9 EN (Enable) Dependency

The symbol denoting enable dependency is the combination of letters EN.

An EN*m* input has the same effect on outputs as an EN input, see 3.3, but it affects only those outputs labeled with the identifying number *m*. It also affects those inputs labeled with the identifying number *m*. By contrast, an EN input affects all outputs and no inputs. The effect of an EN*m* input on an affected input is identical to that of a C*m* input (Figure 13).

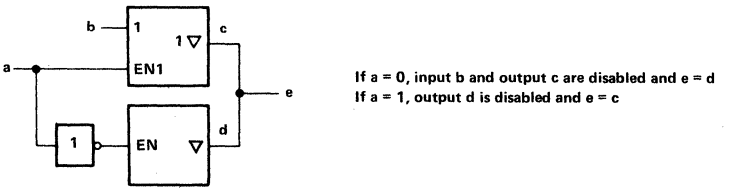


Figure 13. EN (Enable) Dependency

When an EN*m* input stands at its internal 1 state, the inputs affected by EN*m* have their normally defined effect on the function of the element and the outputs affected by this input stand at their normally defined internal logic states, i.e., these inputs and outputs are enabled.

When an EN*m* input stands at its internal 0 state, the inputs affected by EN*m* are disabled and have no effect on the function of the element, and the outputs affected by EN*m* are also disabled. Open-collector outputs are turned off, three-state outputs stand at their high-impedance state, and all other outputs (e.g., totem-pole outputs) stand at their internal 0 states.

4.10 M (MODE) Dependency

The symbol denoting mode dependency is the letter M.

Mode dependency is used to indicate that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

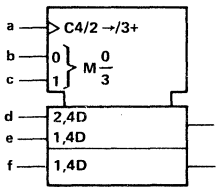
If an input or output has the same effect in different modes of operation, the identifying numbers of the relevant affecting M*m* inputs will appear in the label of that affected input or output between parentheses and separated by solidi, e.g., (1/2)CT=0 ≡ 1CT=0/2CT=0 where 1 and 2 refer to M1 and M2.

4.10.1 M Dependency Affecting Inputs

M dependency affects inputs the same as C dependency. When an M*m* input or M*m* output stands at its internal 1 state, the inputs affected by this M*m* input or M*m* output have their normally defined effect on the function of the element, i.e., the inputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, the inputs affected by this M*m* input or M*m* output have no effect on the function of the element. When an affected input has several sets of labels separated by solidi (e.g., C4/2→/3+), any set in which the identifying number of the M*m* input or M*m* output appears has no effect and is to be ignored. This represents disabling of some of the functions of a multifunction input.

The circuit in Figure 14 has two inputs, **b** and **c**, that control which one of four modes (0, 1, 2, or 3) will exist at any time. Inputs **d**, **e**, and **f** are D inputs subject to dynamic control (clocking) by the **a** input. The numbers 1 and 2 are in the series chosen to indicate the modes so inputs **e** and **f** are only enabled in mode 1 (for parallel loading) and input **d** is only enabled in mode 2 (for serial loading). Note that input **a** has three functions. It is the clock for entering data. In mode 2, it causes right shifting of data, which means a shift away from the control block. In mode 3, it causes the contents of the register to be incremented by one count.



Note that all operations are synchronous.

In MODE 0 (b = 0, c = 0), the outputs remain at their existing states as none of the inputs has an effect.

In MODE 1 (b = 1, c = 0), parallel loading takes place thru inputs e and f.

In MODE 2 (b = 0, c = 1), shifting down and serial loading thru input d take place.

In MODE 3 (b = c = 1), counting up by increment of 1 per clock pulse takes place.

Figure 14. M (Mode) Dependency Affecting Inputs

4.10.2 M Dependency Affecting Outputs

When an M*m* input or M*m* output stands at its internal 1 state, the affected outputs stand at their normally defined internal logic states, i.e., the outputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, at each affected output any set of labels containing the identifying number of that M*m* input or M*m* output has no effect and is to be ignored. When an output has several different sets of labels separated by solidi (e.g., 2,4/3,5), only those sets in which the identifying number of this M*m* input or M*m* output appears are to be ignored.

Figure 15 shows a symbol for a device whose output can behave like either a 3-state output or an open-collector output depending on the signal applied to input **a**. Mode 1 exists when input **a** stands at its internal 1 state and, in that case, the three-state symbol applies and the open-element symbol has no effect. When **a** = 0, mode 1 does not exist so the three-state symbol has no effect and the open-element symbol applies.

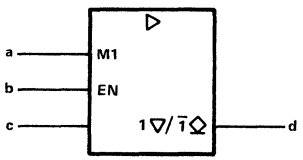


Figure 15. Type of Output Determined by Mode

Table 5. Summary of Dependency Notation

TYPE OF DEPENDENCY	LETTER SYMBOL*	AFFECTING INPUT AT ITS 1-STATE	AFFECTING INPUT AT ITS 0-STATE
Control	C	Permits action	Prevents action
Enable	EN	Permits action	Prevents action of inputs ◇ outputs turned off ▽ outputs at external high impedance Other outputs at internal 0 state
AND	G	Permits action	Imposes 0 state
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Negate (Ex-NOR)	N	Complements state	No effect
OR	V	Imposes 1 state	Permits action
Transmission	X	Bidirectional connection exists	Bidirectional connection does not exist
Interconnection	Z	Imposes 1 state	Imposes 0 state

* These letter symbols appear at the AFFECTING input (or output) and are followed by a number. Each input (or output) AFFECTED by that input is labeled with that same number.

5 Bistable Elements

The dynamic input symbol and dependency notation provide the tools to identify different types of bistable elements and make synchronous and asynchronous inputs easily recognizable (Figure 16).

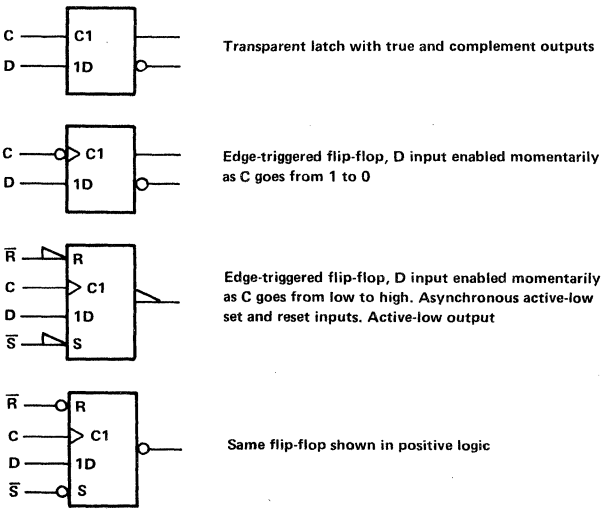


Figure 16. Latches and Flip-Flops

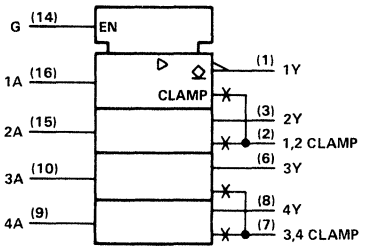
Transparent latches have a level-operated control input. The D input is active as long as the C input is at its internal 1 state. The outputs respond immediately. Edge-triggered elements accept data from D, J, K, R, or S inputs on the active transition of C.

Notice that synchronous inputs can be readily recognized by their dependency labels (a number preceding the functional label, 1D in these examples) compared to the asynchronous inputs (S and R), which are not dependent on the C inputs. Of course if the set and reset inputs were dependent on the C inputs, their labels would be similarly modified (e.g., 1S, 1R).

6 Examples of Actual Device Symbols

The symbols explained in this section include some of the most complex in this book. These were chosen, not to discourage the reader, but to illustrate the amount of information that can be conveyed. It is likely that if one reads these explanations and follows them reasonably well, most of the other symbols will seem simple indeed. The explanations are intended to be independent of each other so they may seem somewhat repetitious. However each illustrates new principles. They are arranged more or less in the order of complexity.

6.1 SN75437A Quadruple Peripheral Driver

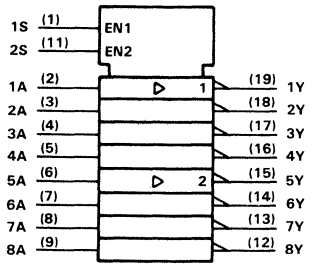


There are four identical sections. The symbology is complete for the first element; the absence of any symbology for the other elements indicates they are identical. The top two elements share a common output clamp, pin 2. This is shown to be a nonlogic connection by the superimposed X on the line. The function for this type of connection is indicated briefly and not necessarily exactly by a small amount of text within the symbol. The bottom two elements likewise share a common clamp.

Each element is shown to be an inverter with amplification (indicated by ▷). Taking TTL as a reference, this means that either the input is sensitive to lower level signals, or the output has greater drive capability than usual. The latter applies in this case. The output is shown by ◇ to be open collector.

All the outputs share a common EN input, pin 14. See Figure 2 for an explanation of the common control block. When EN = 0 (pin 14 is low), the outputs, being open-collector types, are turned off and would be pulled high by an external pullup resistor.

6.2 SN75128 8-Channel Line Receiver

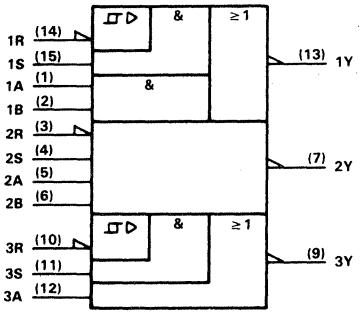


There are eight identical sections. The symbology is complete for the first element; the absence of any symbology for the next three elements indicates they are identical. Likewise the symbology is complete for the fifth element; the absence of any symbology for the next three elements indicates they are identical to the fifth.

Each element is shown to be an inverter with amplification (indicated by ▷). Taking TTL as a reference, this means that either the input is sensitive to lower level signals, or the output has greater drive capability than usual. The former applies in this case. Since neither the symbol for open-collector (◇) or 3-state (▽) outputs is shown, the outputs are of the totem-pole type.

The top four outputs are shown to be affected by affecting input number 1, which is EN1, meaning they will be enabled if EN1 = 1 (pin 1 is high). See 4.9 for an explanation of EN dependency. If pin 1 is low, EN1 = 0 and the affected outputs will go to their inactive (high) levels. Similarly, the lower four outputs are controlled by pin 11.

6.3 SN75122 Triple Line Receivers

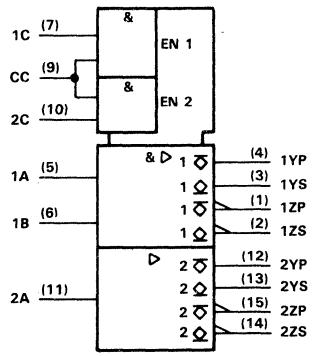


There are two identical sections. The symbology is complete for the first section; the absence of any symbology for the next section indicates it is identical. Likewise the symbology is complete for the third section, which is similar, but not identical, to the first and second.

The top section may be considered to be an OR element (≥1) with two embedded ANDs (&), one of which has an active-low amplified input (▷) with hysteresis (⊓), pin 14. This is ANDed with pin 15 and the result is ORed with the AND of pins 1 and 2. The output of the OR, pin 13, is active-low.

The third section is identical to the first except that pin 12 has no input ANDed with it. Since neither the symbol for open-collector (◇) or 3-state (▽) outputs is shown, the outputs are of the totem-pole type.

6.4 SN75113 Differential Line Drivers with Split 3-State Outputs

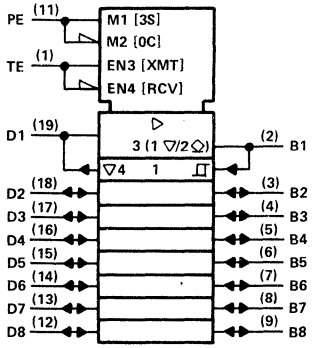


There are two similar elements in the array. The first is a 2-input AND element (indicated by &); the second has only a single input. Both elements are shown to have special amplification (indicated by ▷). Taking TTL as a reference, this means that either the input is sensitive to lower level signals, or the output has greater drive capability than usual. The latter applies in this case.

Each element has four outputs. Pins 4 and 3 are a pair consisting of one open-emitter output (▽) and one open-collector output (◇). Relative to the AND function, both are active high. Pins 1 and 2 are a similar pair but relative to the AND function, both are active low. All outputs of a single, unsubdivided element always have identical internal logic states determined by the function of the element except when otherwise indicated by an associated symbol or label inside the element. Here there is no such contrary indication. All four outputs are shown to be affected by affecting input number 1, which is EN1, meaning they will all be enabled if EN1 = 1. See 4.9 for an explanation of EN dependency. If EN1 = 0, all the affected outputs will be turned off. EN1 is the output of an AND gate (indicated by &) whose active-high inputs are pins 7 and 9. Both pins 7 and 9 must be high to enable the outputs of the top element. Assuming they are enabled and that pins 5 and 6 are both high, the internal state of all four outputs will be a 1. Pins 4 and 3 will both be high, pins 1 and 2 will both be low. The part is designed so that pins 3 and 4 may be connected together creating an active-high 3-state output. Likewise pins 1 and 2 may be connected together to create an active-low 3-state output.

All that has been said about the first element regarding its outputs and their enable inputs also applies to the second element. Pins 9 and 10 are the enable inputs in this case.

6.5 SN75163B Octal General-Purpose Interface Bus Transceiver



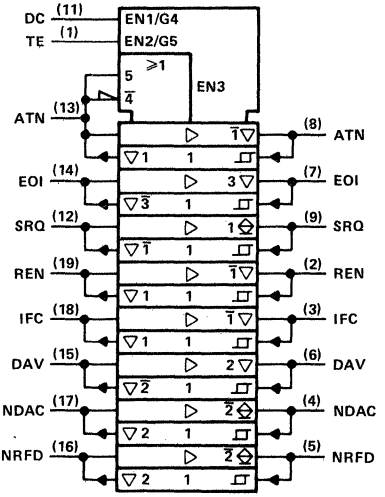
There are eight I/O ports on each side, pins 2 through 9 and 12 through 19. There are eight identical channels. The symbology is complete for the first channel; the absence of any symbology for the other channels indicates they are identical. The eight bidirectional channels each have amplification from left to right, that is, the outputs on the right have increased drive capability (indicated by ▷), and the inputs on the right all have hysteresis (indicated by ⊓).

The outputs on the left are shown to be 3-state outputs by the ▽. They are also shown to be affected by affecting input number 4, which is EN4, meaning they will be enabled if EN4 = 1 (pin 1 is low). See 4.9 for an explanation of EN dependency. If EN4 = 0 (pin 1 is high), the affected outputs will go to their high-impedance (off) states.

The labeling at pin 2, which applies to all the outputs on the right, is unusual because the outputs themselves have an unusual feature. The label includes both the symbol for a 3-state output (▽) and for an open-collector output (◇), separated by a slash indicating that these are alternatives.

The symbol for the 3-state output is shown to be affected by affecting input number 1, which is M1, meaning the ▽ label is valid when M1 = 1 (pin 11 is high), but is to be ignored when M1 = 0 (pin 11 is low). See 4.10 for an explanation of M (mode) dependency. Likewise the symbol for the open-collector output is shown to be affected by affecting input number 2, which is M2, meaning the ◇ label is valid when M2 = 1 (pin 11 is low), but is to be ignored when M2 = 0 (pin 11 is high). These labels are enclosed in parentheses (used as in algebra); the numeral 3 indicates that in either case the output is affected by EN3. Thus the right-hand outputs will be off if pin 1 is low. It can now be seen that pin 1 is the direction control and pin 11 is used to determine whether the outputs are of the 3-state or open-collector variety.

6.6 SN75161B Octal IEEE Std 488 Interface Bus Transceiver



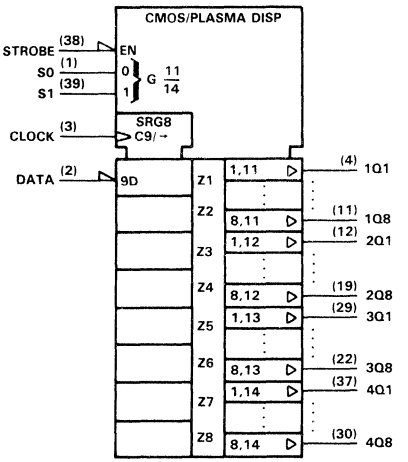
There are eight I/O ports on each side, pins 2 through 9 and 12 through 19. Pin 13 is not only an I/O port; the line running into the common-control block (see Figure 2) indicates that it also has control functions. Pins 1 and 11 are also controls. The eight bidirectional channels each have amplification from left to right, that is, the outputs on the right have increased drive capability (indicated by ▷), and the inputs on the right all have hysteresis (indicated by ⊓). All of the outputs are shown to be of the 3-state type by the ▽ symbol except for the outputs at pins 9, 4, and 5, which are shown to have passive pullups by the ◇ symbol.

Starting with a typical I/O port, pin 18, the output portion is identified by an arrow indicating right-to-left signal flow and the three-state output symbol (▽). This output is shown to be affected by affecting input number 1, which is EN1, meaning it will be enabled as an output if EN1 = 1 (pin 11 is high). See 4.9 for an explanation of EN dependency. If pin 11 is low, EN1 = 0 and the output at pin 18 will be in its high-impedance (off) state. This also applies to the 3-state outputs at pins 13 and 19 and to the passive-pullup output at pin 9. On the other hand, the outputs at pins 8, 2, 3, and 12 all are affected by the complement of EN1. This is indicated by the bar over the 1 at each of those outputs. They are enabled only when pin 11 is low. Thus one function of pin 11 is to serve as direction control for the first, third, fourth, and fifth channels.

Similarly it can be seen that pin 1 serves as direction control for the sixth, seventh, and eighth channels. If pin 1 is high, transmission will be from left to right in the sixth channel, right to left in the seventh and eighth. These transmissions are reversed if pin 1 is low.

The direction control for the second channel, EN3, is more complex. EN3 is the output of an OR (≥1) function. One of the inputs to this OR is the active-high signal on pin 13. This signal is shown to be affected at the input to the OR gate by affecting input number 5, which is G5, meaning that pin 13 is ANDed with pin 1 before entering the OR gate. See 4.2 for an explanation of G (AND) dependency. The other input to the OR is the active-low signal on pin 13. This signal is ANDed with the complement of pin 11 before entering the OR gate. This is indicated by the G4 at pin 1 and the 4 with a bar over it at pin 13. Thus for EN3 to stand at the 1 state, which would enable transmission from pin 14 to pin 7, both pins 13 and 1 must be high or both pins 13 and 11 must be low.

6.7 SN75500E AC Plasma Display Driver with CMOS-Compatible Inputs



The heart of this device and its symbol is an 8-bit shift register. It has a single D input, pin 2, which is shown to be affected by affecting input number 9, which is C9, meaning it will be enabled if C9 = 1. See 4.8 for an explanation of C dependency and 5.0 for a discussion of bistable elements. Since the C input is dynamic, the storage elements are edge-triggered flip-flops. While C9 = 1, which in this case will occur on the transition of pin 3 from low to high, the state of the D input will be stored. Pin 2 is shown to be active low so to store a 1, pin 2 must be low.

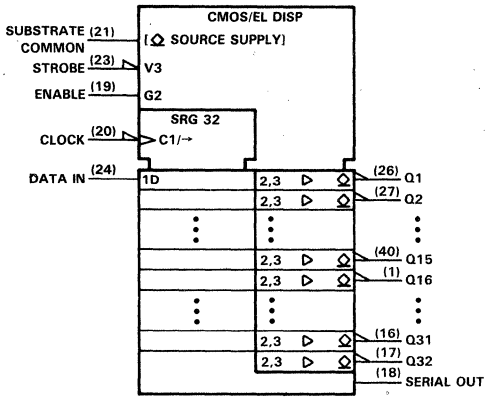
In addition to controlling the D input, pin 3 is shown by /→ to have an additional function. As pin 3 goes from low to high, data stored in the shift register is shifted one position. The right-pointing arrow means that the data is shifted away from the control block (down).

On the right side of the symbol an abbreviation technique has been used that is practical only when the internal labels and the pin numbers are both consecutive. Thus it should be clear that the input of the element whose output is pin 5 is affected by affecting input number 2, just as the input of the element whose output is pin 4 is affected by affecting input number 1. Affecting inputs 1 through 8 are Z inputs (Z1 through Z8), which means their signals are tranferred directly to the output elements. See 4.6 for an explanation of Z dependency.

The inputs of the 32 implicitly shown output elements are also shown to be affected by affecting inputs numbers 11, 12, 13, and 14 in four blocks of eight each. These inputs will be found in the common control block preceded by a letter G and a brace. The brace is called the binary grouping symbol. It is equivalent to a decoder with outputs in this case driving four G inputs (G11, G12, G13, and G14). The weights of the inputs to the coder are shown to be 2^0 and 2^1 for pins 1 and 39, respectively. The decoder has four outputs corresponding to the four possible sums of the weights of the activated decoder inputs. If pins 1 and 39 are both low, the sum of the weights = 0 and G11 = 1. If pin 1 is low while pin 39 is high, the sum = 2 and G13 = 1 and so forth. G indicates AND dependency, see 4.2. Only one of the four affecting G inputs at a time can take on the 1 state. The block of eight output elements affected by that G input are enabled; the 0 state is imposed on the other 24 output elements and externally those output pins are low.

Because of their high-current, high-voltage characteristics, the outputs are labeled with the amplification symbol ▷. All the outputs share a common EN input, pin 38. See Figure 2 for an explanation of the common control block. When EN = 0 (pin 38 is high), the outputs take on their internal 0 states. Being active high, that means they are forced low.

6.8 SN75551 Electroluminescent Row Driver with CMOS-Compatible Inputs



The heart of this device and its symbol is a 32-bit shift register. It has a single D input, pin 24, which is shown to be affected by affecting input number 1, which is C1, meaning it will be enabled if C1 = 1. See 4.8 for an explanation of C dependency and 5.0 for a discussion of bistable elements. Since the C input is dynamic, the storage elements are edge-triggered flip-flops. While C1 = 1, which in this case will occur on the transition of pin 20 from high to low, the state of the D input will be stored. Pin 24 is shown to be active high so to store a 1, pin 24 must be high.

In addition to controlling the D input, pin 20 is shown by /→ to have an additional function. As pin 20 goes from high to low, data stored in the shift register is shifted one position. The right-pointing arrow means that the data is shifted away from the control block (down). The internal inputs of the output buffers are all shown to be affected by affecting inputs 2 and 3. Affecting input 2 is G2, meaning that pin 19 is ANDed with each of the internal register outputs, which are the buffer inputs. If pin 19 is high, the affected buffer inputs are enabled. If pin 19 is low, the 0 state is imposed on the affected buffer inputs. See 4.2 for an explanation of G (AND) dependency. Affecting input 3 is V3, meaning that pin 23 (active low) is ORed with each of the internal register outputs. If pin 23 is high, V3 = 0 and the affected buffer inputs are enabled. If pin 23 is low, V3 = 1 and the 1 state is imposed on the affected buffer inputs. See 4.4 for an explanation of V (OR) dependency. The effect of V3 is taken into account after that of G2 because of the order in which the labels appear. This means that the imposition of the 1 state on the internal buffer inputs by pin 23 would take precedence over the imposition of the 0 state by pin 19 in case both inputs were active. Pin 18 is shown to be an output directly from the thirty-second stage of the shift register. Pins 19 and 23 do not affect this output.

An abbreviation technique has been used for the shift register elements and associated the output lines. This technique is practical only when the pin numbers and pin names are both consecutive.

The symbol ◇ designates an n-p-n open-collector or similar output. In this device, the outputs are actually open-drain n-channel field-effect transistors. Instead of being grounded, the sources of these transistors are all connected to pin 21. This pin is used as an input to control the output voltage.

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