Data Book

Data Acquisition Circuits
Data Conversion and DSP Analog Interface

1995

TEXAS INSTRUMENTS

Data Acquisition Circuits

Data Conversion and DSP Analog Interface

Data Book

1995

Mixed-Signal Products

Data Acquisition Circuits Data Book

Data Conversion and DSP Analog Interface

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INTRODUCTION

Texas Instruments offers an extensive line of industry-standard integrated circuits designed to provide highly reliable circuits for peripheral support applications of microprocessor-based systems, DSP (digital signal processing) related analog interfaces, video interfaces, video and high-speed converters, digitizing requirements that demand ADC and DAC conversion, and general-purpose functions.

TI data acquisition system circuits represent technologies from traditional bipolar through LinCMOS™, Advanced LinCMOS™, and LinEPIC™ processes. The LinCMOS™ and Advanced LinCMOS™ technologies feature improvements in resolution, power consumption, and temperature stability. LinEPIC™ has both improved conversion speed and reduced power consumption.

This data book provides information on the following types of products:

- Dual-Slope Analog-to-Digital Converters (ADC)
- Successive-Approximation Semi-Flash, and Flash ADC Converters
- Current Multiplying and Video DAC Converters
- High-Speed Converters for Control Applications
- Color Palette Chips for Computer Graphics
- Analog Interface Circuits for DSP Interface
- Switched-Capacitor Filter ICs
- Other General-Purpose Functions

These products cover the requirements of PC and workstation multimedia applications such as audio, graphics, communication applications, modems and cellular phones, video capture and image processing, industrial control and disk-drive servo-loop control, automotive,f electronic instrumentation, consumer, digital audio and any DSP or microprocessor-based system. New surface-mount packages include both ceramic and plastic chip carriers, and the small-outline plastic packages that optimize board density with minimum impact on power-dissipation capability. The equipment with handlers and test equipment. In addition, specifications and programs are continuously updated. Quality and performance are monitored throughout all phases of manufacturing.

Included are those new products added to this volume as indicated by a dagger(†). The selection guide includes a functional description of each device by providing key parametric information and packaging options. Ordering information and mechanical data are in the last section of the book.

Complete technical data for all TI semiconductor products are available from your nearest TI Field Sales Office, local authorized TI distributor, or by writing directly to:

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We sincerely believe the new 1995 Data Acquisition Circuits Data Book will be a significant addition to your technical literature from Texas Instruments.

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†Product Preview

†Product Preview

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RESOLUTION	DEVICE	CONVERSION TIME (µs)	SAMPLING RATE (KSPS)	NUMBER OF CHANNELS	INTERNAL REFERENCE	SUPPLY VOLTAGE	PARALLEL OUTPUT	INTERNAL CLOCK	SHUTDOWN	POWER (mW max)	PACKAGE	NUMBER OF TERMINALS	COMMENTS
16/18	TLC320AD57		48, 44.1, 32	2	X	5		X	X	200	DW	28	Dual sigma-delta. SNR of 97 dB
12	TLC2543	10	66	11		5		X	X	12	DW, FN, N	20	Low cost, high resolution
	TLV2543‡	10	66	11		3.3		X	X	8	DW, FN, N	20	3 V version TLC2543
	TLC1225/1125	12	83	1		±5	X			85	N, FN	28	Uni or bipolar with self-calibration
10	TLC1550/1551	6	164	1		5	X	X		40	FN, NW	24	DSP front end with 3-state outputs
	TLC1549	21	38	1		5		X		12	D, FK, JG, P	8	Plug in upgrade for TLC549
	TLV1549	21	38	1		3.3		X		8	D, FK, JG, P	8	3 V version TLC1549
	TLC1543	21	38	11		5		X		12	DW, FN, N	20	Plus in upgrade for TLC543
	TLV1543	21	38	11		3.3		X		8	DW, FK, J, N	20	3 V version TLC1543
	TLC1541	21	32	11		5				12	DW, J, N, FK, FN	20	±1 LSB total error
	TLC1540	21	32	11		5				12	DW, J, N, FK, FN	20	±0.5 LSB total error
8	TLC5510		20,000	1		5	X			90	NS	24	Replaces Sony CXD1175
	TLV5510‡		20,000	1		3	X			60	NS	24	3 V version of TLC5510
	TLC5733‡		20,000	3		5	X			375	QFP	64	Triple ADC with clamp
	TLC5540‡‡		40,000	1		5	X			120	NS	24	High speed ADC
	TLC0820A	1.2	392	1		5	X	X		75	DW, F, NFK, N	20	Replaces AD7820 and ADC0820
	TLC0838‡	20		8		5				12	FN, N	20	Replaces ADC0838
	TLC540	9	75	11		5				12	SW, N, FN	20	Replaces ADC0811 and MC145040
	TLC541	17	40	11		5				12	DW, N, FN	20	Compatible with TLC1540 pinout
	TLC542	20	25	11		5		X		10	FN, N, DW	20	Replaces MC145041
	TLC545	9	76	19		5				12	FN, N	28	uP compatible
	TLC546	17	40	19		5				12	FN, N	28	uP compatible
	TLC548	17	45.5	1		5		X		12	D, P	8	uP compatible
	TLC549	17	40	1		5		X		12	D, P	8	uP compatible

† Budgetary pricing for 0°C to 70°C
‡ Indicates product preview

ANALOG-TO-DIGITAL CONVERTER SELECTION GUIDE

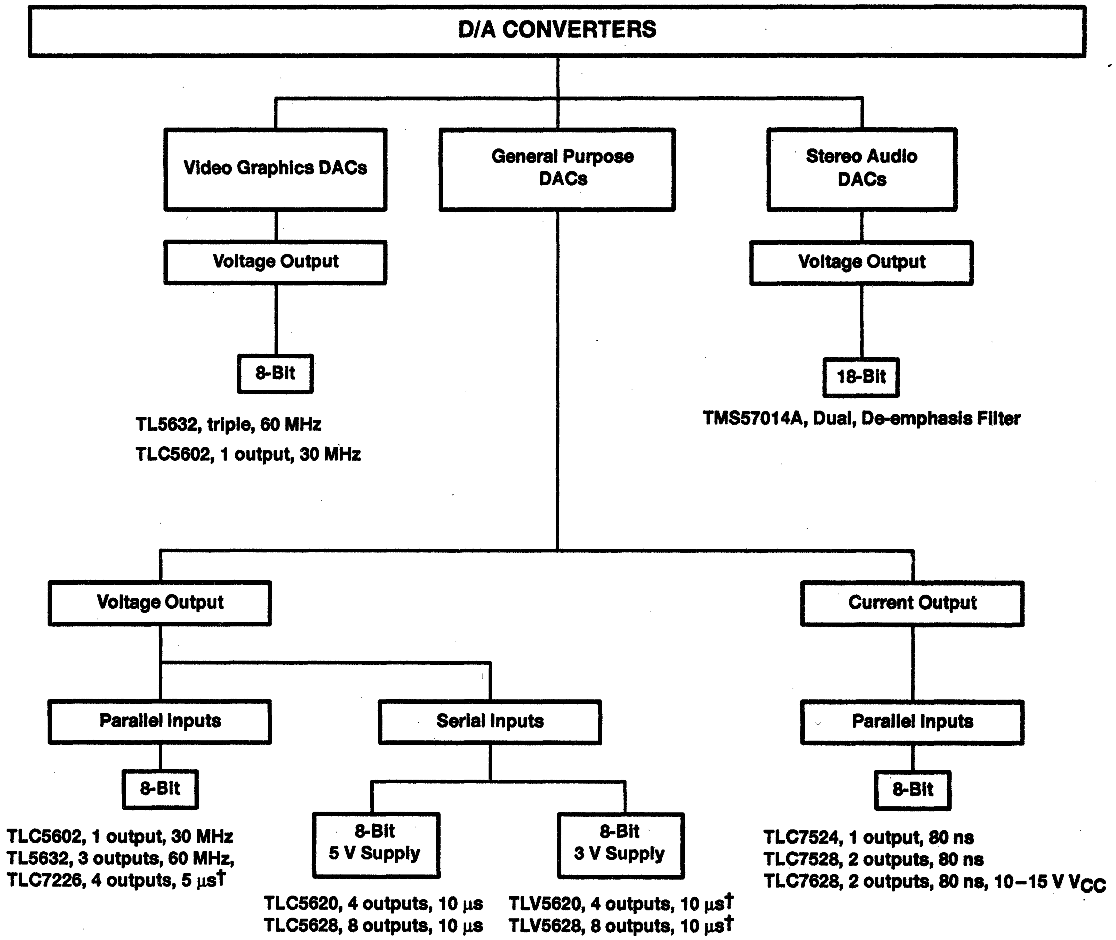
GENERAL PURPOSE A/D CONVERTERS

- $f_S >= 1$ MSPS, $t_{conv} <= 1\ \mu s$
  - 5 V Supply
    - 6-Bit
      - TL5501, 20 MSPS
    - 8-Bit
      - TLC5510, 20 MSPS
      - TLC5733†, 20 MSPS, triple ADC, with clamp
      - TLC5540†, 40 MSPS
  - 3 V Supply
    - 8-Bit
      - TLV5510†, 20 MSPS
- 100 KSPS < f_S < 1 MSPS, $1\ \mu s < t_{conv} < 10\ \mu s$
  - 5 V Supply
    - 8-Bit
      - TLC0820, 392 KSPS
    - 10-Bit
      - TLC1550, 164 KSPS
- f_S < 100 KSPS, $t_{conv} < 10\ \mu s$
  - 5 V Supply
    - 8-Bit
      - TLC0832, 2 inputs,† 30 KSPS
      - TLC0834, 4 inputs,† 30 KSPS
      - TLC0838, 8 inputs,† 30 KSPS
      - TLC540, 11 inputs, 75 KSPS
      - TLC541, 11 inputs, 40 KSPS
      - TLC542, 11 inputs, 25 KSPS
      - TLC545, 19 inputs, 76 KSPS
      - TLC546, 19 inputs, 40 KSPS
      - TLC548, 45.5 KSPS
      - TLC549, 40 KSPS
    - 10-Bit
      - TLC1549, 38 KSPS, internal clock
      - TLC1543, 11 inputs, 38 KSPS
      - TLC1541, 11 inputs, 32 KSPS
      - TLC1540, 11 inputs, 32 KSPS
    - 12-Bit
      - TLC2543, 11 input, 10 μs, Sleep
      - TLC1225, 83 KSPS, self-calibrate
    - 18-Bit
      - TLC320AD57, stereo, Sigma Delta
  - 3 V Supply
    - 10-Bit
      - TLV1549, 38 KSPS
      - TLV1543, 11 inputs, 38 KSPS
    - 12-Bit
      - TLV2543†, 11 inputs, 66 KSPS, Sleep

† Indicates product preview status at time of print.

RESOLUTION	DEVICE	BUS INTERFACE	OUTPUT (I OR V)	NO. OF DACs	REFERENCE†	SETTLING TIME	SUPPLY VOLTAGE (V)	LINEARITY (LSB)	CONVERSION RATE	POWER (mW max)	PACKAGE	NO. OF PINS	COMMENTS
16/18	TMS57014A	Serial	PWM	2	N/A		5		32, 37.8, 44.1 and 48 kHz	350	DWB	28	Dual audio sigma-delta DAC with interpolation filter and digital volume control
8	TLC7524	8, µP	I	1	Ext, M	100 ns	5–15	±0.5		5	D,N,FN	16	Popular low cost MDAC with latch for DSP and µp's
	TLC7528	8, µP	I	2	Ext, M	100 ns	5–15	±0.5		5	DW,N, FN	20	Dual version of TLC7524
	TLC7628	8, µP	I	2	Ext, M	100 ns	10–15	±0.5		20	DW,N, FN	20	Dual MDAC with TTL-compatible inputs
	TLC7225‡	8, µP	V	4	Ext	5 µs		±0.5					Separate reference for each DAC
	TLC7226‡	8, µP	V	8	Ext	5 µs		±0.5		195	DW,N, FN	20	Replaces AD7226
	TLC5620	Serial	V	4	Ext	10 µs	5	±1		10	N,D	14	Low power quad DAC with programmable x1 or x2 output.
	TLC5628	Serial	V	8	Ext	10 µs	5	±1		10	N,DW	16	Low power, octal DAC with programmable x1 or x2 output.
	TLV5620‡	Serial	V	4	Ext	10 µs	3	±1		10	N,D	14	3 V version of TLC5620
	TLV5628‡	Serial	V	8	Ext	10 µs	3	±1		10	N,D	16	3 V version of TLV5628
	TLC5602	8	V	1	Ext	30 ns	5	±0.5	30 MHz	80	N,DW	18	Low power video DAC
	TL5632	8 by 3	V	3	Int		5	±0.5	60 MHz	350	FR	44	Triple video DAC with internal reference.

† Ext, M – external reference, multiplying; PWM – Pulse width modulated
‡ Indicates product preview



† Indicates product preview status at time of print.

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Replacements are based on similarity of electrical and mechanical characteristics shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, compare the specifications of the substitute device with the specifications of the original.

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Manufacturers are arranged in alphabetical order.

ANALOG DEVICES	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT
AD573		TLC1550INW
		TLC1550IFN
		TLC1551INW
		TLC1551IFN
AD7524AD	AD7524AN	TLC7524IN
AD7524JN	AD7524JN	TLC7524CN
AD7528BQ	AD7528BN	TLC7528IN
AD7528KN	AD7528KN	TLC7528CN
AD7820K/B/T	TLC0820A	
AD7820L/C/U		
AD7820	TLC0820	
AD7890		TLC2543IN
		TLC2543IDW
		TLV2543IN (3V)
		TLV2543IDW
ADC82AG		
AD82AM		TLC0820AIN
AD1878		TLC320AD57
AD9048		TLC5540INS
ADC-EK12DC		TLC7135CN
		TLC7135CFN
		ICL7135CN
		ICL7135CFN
ADC-EK12DR		TLC7135CN
		TLC7135CFN
		ICL7135CN
		ICL7135CFN
PM7524FQ		TLC7524IN, AD7524AN
PM7524FP		TLC7524CN, AD7524JN
PM7528		TLC7528, AD7528

BROOKTREE	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT
Bt101, 102, 253		TL5632CFR

CRYSTAL	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT
5336, 5339		TLC320AD57

FUJITSU	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT
MB40576	TL5501	
MB40578	TLC5502	TLV5510 (3 V)
MB40778	TLC5602	

HARRIS	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT
HI1175		TLV5510INS (3 V)

LINEAR TECHNOLOGY	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT
LTC1091		TLC1549IN
		TLC1549IDW
LTC1092/93/94		TLC1542IN
		TLC1543IN
		TLC1542IDW
		TLC1543IDN
LTC1291/92/93/94		TLC2543IDW

MAXIM	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT
MAX17x Family		TLC2543IN
		TLC2543IDW
		TLC2543IFN
		TLC2543 (3V)
MAX509		TLC5620
MAX529		TLC5628

MICRO NETWORKS	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT
MN5100/5101		TLC0820ACN
MN5120/5130/5140		TLC0820ACN

MICRO POWER SYSTEMS	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT
MP7138AN		TLC7135CN
		TLC7135CFN
		ICL7135CN
		ICL7135CFN

MOTOROLA	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT
MC14433P		TLC7135CN
		TLC7135CFN
		ICL7135CN
		ICL7135CFN
MC14444P		TLC546IN
MC145040FN	TLC541MFN	TLC540MFN
MC145040L	TLC541MJ	TLC540MJ
MC145040P	TLC541MN	TLC540MN
MC145041P1	TLC542IN	
MC14051		TLC1543IN
		TLC1542IN
		TLC1543IDW
		TLC1542IDW

NATIONAL	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT
ADC0811BCJ	TLC541IN	TLC540IN
ADC0811BCN	TLC541IFN	TLC540IFN
ADC0811BJ	TLC541MJ	TLC540MJ
ADC0811CCJ	TLC541IN	TLC540IN
ADC0811CCN	TLC541IN	TLC540IN
ADC0811CCV	TLC541IFN	TLC540IFN
ADC0811CJ	TLC541MJ	TLC540MJ
ADC0820BCD	TLC0820BIN	
ADC0820BCN	TLC0820BCN	
ADC0820BD	TLC0820BMJ	
ADC0820CCD	TLC0820AIN	
ADC0820CCN	TLC0820ACN	
ADC0820CD	TLC0820AMJ	
ADC0830BCN		TLC546IN
ADC0830CCN		TLC546IN
ADC0831BCJ	TLC0831BIP	TLC549IN
ADC0831BCN	TLC0831BIP	TLC549IN
ADC0831CCJ	TLC0831AIP	TLC549IN
ADC0831CCN	TLC0831ACP	TLC549IN
ADC0832BCJ	TLC0832BIP	
ADC0832BCN	TLC0832BCP	
ADC0832CCJ	TLC0832AIP	
ADC0832CCN	TLC0832ACP	
ADC0834BCJ		TLC0834BIN
ADC0834BCN		TLC0834BCN
ADC0834CCJ		TLC0834AIN
ADC0834CCN		TLC0834ACN
ADC0838BCJ		TLC0838BIN
ADC0838BCN		TLC0838BCN
ADC0838CCJ		TLC0838AIN

NATIONAL (Continued)	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT
ADC0838CCN		TLC0838ACN
ADC1001CCJ		TLC1541IN
ADC1005BCJ		TLC1541IN
ADC1005CCJ		TLC1541IN
ADC1225		TLC1225
ADC3511CCN		TLC7135CN ICL7135CN
ADC3711CCN		TLC7135CN TLC7135CFN ICL7135CN ICL7135CFN
MF4-50	TLC04/MF4A-50	
MF4-100	TLC14/MF4A-100	

PHILLIPS	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT
NE5036FE/N/D		TLC549CN/CD
NE5037F/N/D		TLC549CN/CD
TDA8703		TLC5540INS
TDA8707		TLC5733IPM

SILICONIX	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT
LD110CJ		TLC7135N ICL7135CN
LD111ACJ		TLC7135CN ICL7135CN
LD120CJ		TLC7135CN ICL7135CN
LD121ACJ		TLC7135CN ICL7135CN
Si7135CJ	TLC7135CN ICL7135CN	

SONY	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT
CXD1175		TLC5510INS TLV5510INC (3V)
CXD1179		TLC5540INS

TELEDYNE	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT
TSC7135CPI	TLC7135CN ICL7135CN	
TSC8701		TLC1541IN
TSC8704		TLC1541IN
TSC14433CN		TLC7135CN ICL7135CN

Analog-to-Digital Converters

ADC0803	ADC0832	TL502	TLC5502-5
ADC0804	ADC0834	TL503	TLC5503-2
ADC0805	ADC0838	TL505	TLC5503-5
ADC0808	TLC532/3	TL507	TL5501
ADC0809	TL500	ADC0820†	
ADC0831	TL501	TLC5502-2	

† Retaining the TLC0820A

Analog Interface Circuits

TLC32071
TLC32042

Analog Switches‡

TL181	TL191	TL607	TLC4066
TL185	TL601	TL610	
TL188	TL604	TLC4016	

‡ All analog switches and multiplexers in the data book are discontinued.

Filters

MF10A
MF10C
TLC10
TLC20

TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS

INTRODUCTION

These terms, definitions, and letter symbols are in accordance with those currently approved by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

1. GENERAL TERMS

Analog-to-Digital Converter (ADC)

A converter that uniquely represents all analog input values within a specified total input range by a limited number of digital output codes, each of which exclusively represents a fractional part of the total analog input range (see Figure 1).

NOTE: This quantization procedure introduces inherent errors of one-half LSB (least significant bit) in the representation since, within this fractional range, only one analog value can be represented free of error by a single digital output code.

CONVERSION CODE

RANGE OF ANALOG INPUT VALUES	DIGITAL OUTPUT CODE
4.5 • 5.5	0 ... 101
3.5 • 4.5	0 ... 100
2.5 • 3.5	0 ... 011
1.5 • 2.5	0 ... 010
0.5 • 1.5	0 ... 001
0 • 0.5	0 ... 000

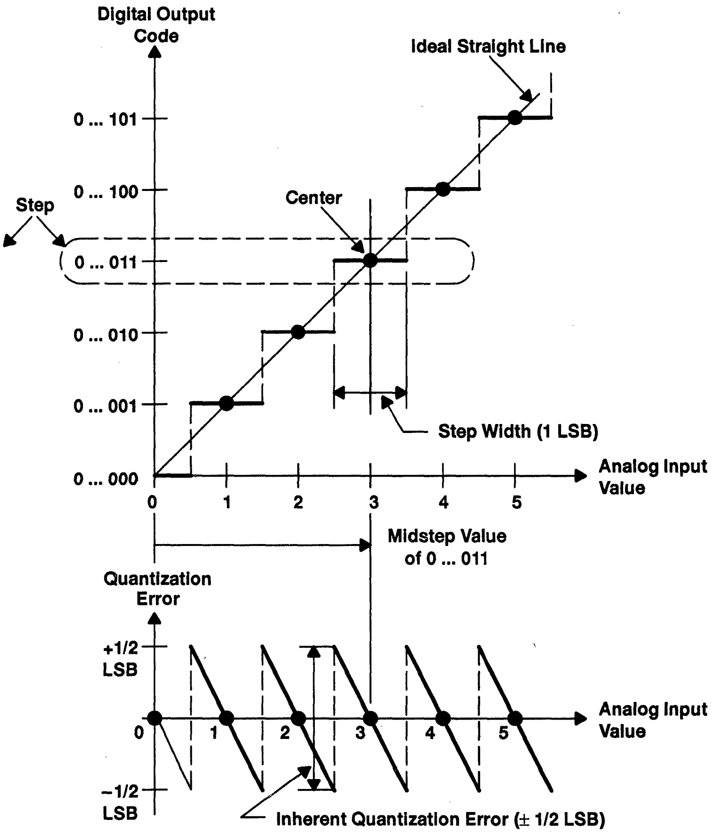


Figure 1. Elements of Transfer Diagram for an Ideal Linear ADC

Analog-to-Digital Processor

An integrated circuit providing the analog part of an ADC; provision of external timing, counting, and arithmetic operations is necessary for implementing a full analog-to-digital converter.

Companding DAC

A DAC whose transfer function complies with a compression or expansion law.

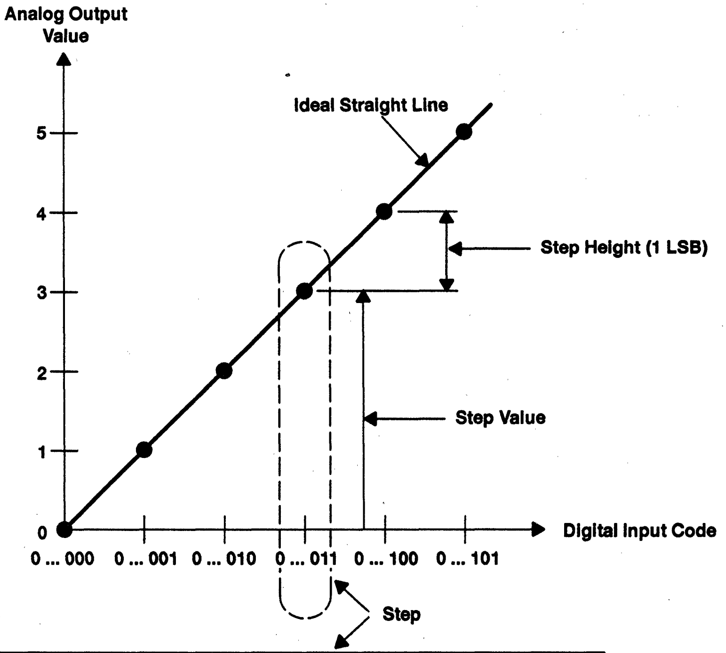
NOTE 1: The corresponding ADC normally consists of such a companding DAC and additional external circuitry.

NOTE 2: The compression or expansion law is usually a logarithmic function, e.g., A-law or μ-law.

Conversion Code (of an ADC or a DAC)

The set of correlations between each of the fractional parts of the total analog input range or each of the digital input codes, respectively, and the corresponding digital output codes or analog output values, respectively (see Figures 1 and 2).

NOTE: Examples of output code formats are straight binary, 2's complement, and binary-coded decimal.



CONVERSION CODE

Digital Input Code	0 ... 000	0 ... 001	0 ... 010	0 ... 011	0 ... 100	0 ... 101
Analog Output Value	0	1	2	3	4	5

Figure 2. Elements of Transfer Diagram for an Ideal Linear DAC

Digital-to-Analog Converter (DAC)

A converter that represents a limited number of different digital input codes by a corresponding number of discrete analog output values (see Figure 2)

NOTE: Examples of input code formats are straight binary, 2's complement, and binary-coded decimal.

Full Scale (of a unipolar ADC or DAC)

A term used to refer a characteristic to that step within the transfer diagram whose nominal midstep value or nominal step value has the highest absolute value [see Figure 3(a) for a linear unipolar ADC].

NOTE 1: The subscript for the letter symbol of a characteristic at full scale is FS.

NOTE 2: In place of a letter symbol, the abbreviation FS is in common use.

Full Scale, Negative (of a bipolar ADC or DAC) [see Figures 3(b) and 3(c)]

A term used to refer a characteristic to the negative end of the transfer diagram, that is, to the step whose nominal midstep value or nominal step value has the most-negative value.

NOTE 1: The subscript for the letter symbol of a characteristic at negative full scale is FS– (V_{FS-}, I_{FS-}).

NOTE 2: In place of a letter symbol, the abbreviation FS– is in common use.

Full Scale, Positive (of a bipolar ADC or DAC) [see Figure 3(b) and 3(c)]

A term used to refer a characteristic to the positive end of the transfer diagram, that is, to the step whose nominal midstep value or nominal step value has the most-positive value.

NOTE 1: The subscript for the letter symbol of a characteristic at positive full scale is FS+ (V_{FS+}, I_{FS+})

NOTE 2: In place of a letter symbol, the abbreviation FS+ is in common use.

Full-Scale Range, Nominal (of a linear ADC or DAC) (V_{FSRnom}, I_{FSRnom}) (see Figure 3)

The total range in analog values that can be coded with uniform accuracy by the total number of steps with this number rounded to the next higher power of 2.

NOTE: In place of the letter symbols, the abbreviation FSR(nom) can be used.

Example: Using a straight binary n-bit code format, it follows:
– for an ADC: FSR(nom) = $2^n \times$ (nominal value of step width)
– for a DAC: FSR(nom) = $2^n \times$ (nominal value of step height)

Full-Scale Value, Nominal (V_{FSnom}, I_{FSnom})

A value derived from the nominal full-scale range:
– for a unipolar converter: $V_{FSnom} = V_{FSRnom}$
– for a bipolar converter: $V_{FSnom} = 1/2\ V_{FSRnom}$ (see Figure 3)

NOTE 1: In a few data sheets, this analog value is used as a reference value for adjustment procedures or as a rounded value for the full-scale range(s).

NOTE 2: In place of letter symbols, the abbreviation FS(nom) is in common use.

Full-Scale Range, (Practical) (of a linear ADC or DAC) (V_{FSR}, I_{FSR}) (V_{FSRpr}, I_{FSRpr}) (see Figure 3)

The total range of analog values that correspond to the ideal straight line.

NOTE 1: The qualifying adjective practical can usually be deleted from this term provided that, in a very few critical cases, the term nominal full-scale range is not also shortened in the same way. This permits use of the shorter letter symbols or abbreviations (see Note 2).

NOTE 2: In place of the letter symbols, the abbreviations FSR and FSR(pr) are in common use.

NOTE 3: The (practical) full-scale range has only a nominal value because it is defined by the end points of the ideal straight line.

Example: Using a straight binary n-bit code format, it follows:
– for an ADC: FSR = $(2^n - 1) \times$ (nominal value of step width)
– for a DAC: FSR = $(2^n - 1) \times$ (nominal value of step height)

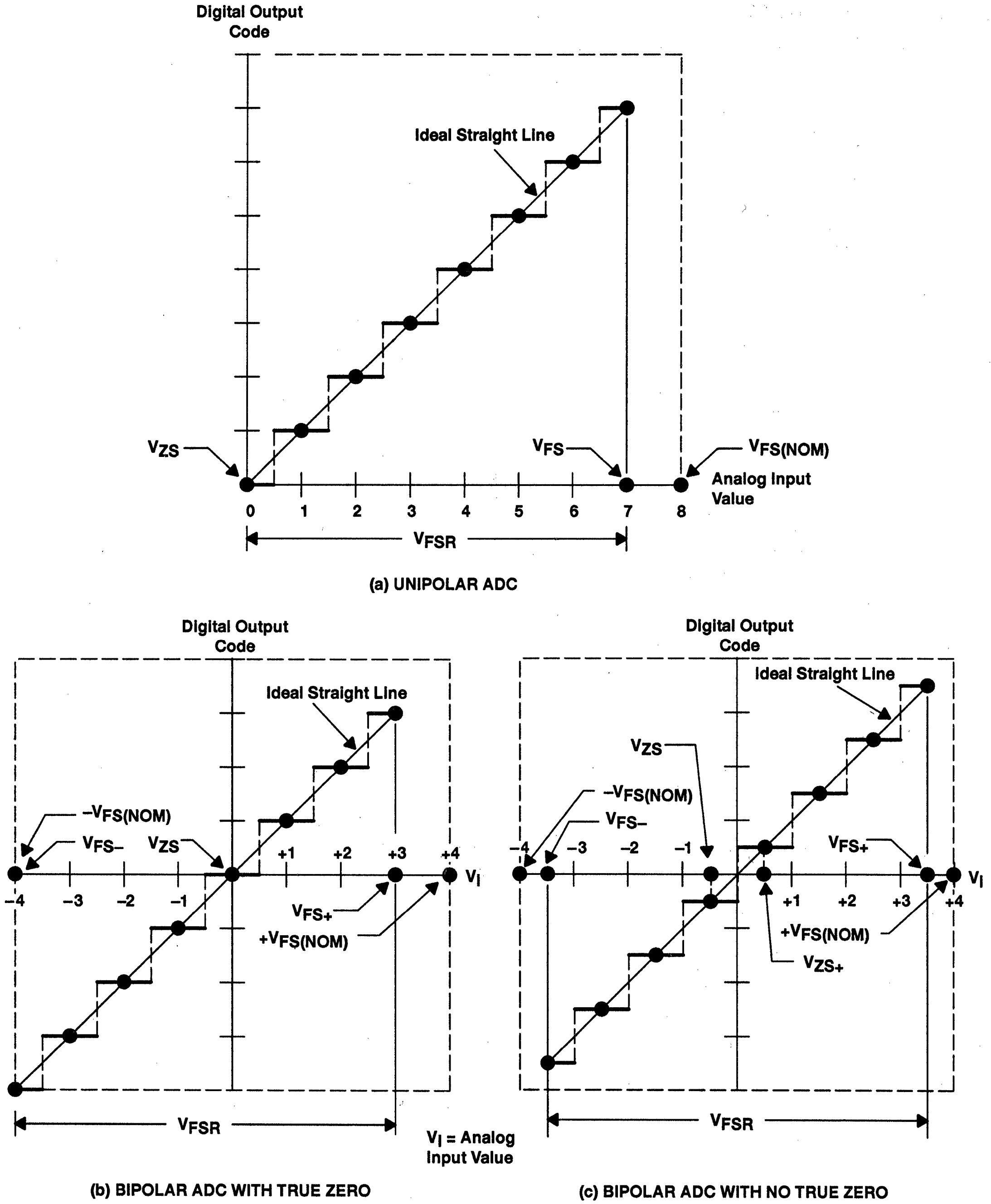


Figure 3. Ideal Straight Line, Full-Scale Value and Zero-Scale Value (Shown for Ideal Linear ADCs)

Gain Point (of an adjustable ADC or DAC)

The point in the transfer diagram corresponding to the midstep value (for an ADC) or the step value (for a DAC) of the step for which gain error is specified (usually full scale), and in reference to which the gain adjustment is performed (see Figures 4 and 5).

NOTE: Gain adjustment causes only a change of the slope of the transfer diagram, without changing the offset error.

Ideal Straight Line (of a linear ADC or DAC)

In the transfer diagram, a straight line between the specified points for the most-positive (least-negative) and most-negative (least-positive) nominal midstep values or nominal step values, respectively (see Figures 1, 2, and 3).

NOTE: The ideal straight line passes through all the points for nominal midstep values or nominal step values, respectively.

Linear ADC

An ADC having steps ideally of equal width excluding the steps at the two ends of the total range of analog input values.

NOTE: Ideally, the width of each end steps is one half of the width of any other step (see Figure 1).

Linear DAC

A DAC having steps ideally of equal height (see Figure 2).

LSB, Abbreviation

The abbreviation for Least Significant Bit, that is, for the bit that has the lowest positional weight in a natural binary numeral.

Example: In the natural binary numeral 1010, the rightmost bit 0 is the LSB.

LSB, Unit Symbol (for linear converters only)

The unit symbol for the magnitude of the analog resolution of a linear converter, which serves as a reference unit to express the magnitude of other analog quantities of that same converter, especially of analog errors, as multiples or submultiples of the magnitude of the analog resolution.

Example: 1/2 LSB means an analog quantity equal to 0.5 times the analog resolution.

NOTE: The unit symbol LSB refers to the fact that, for a natural binary code, the analog resolution corresponds to the nominal positional weight attributed to the least significant bit of the binary numeral.

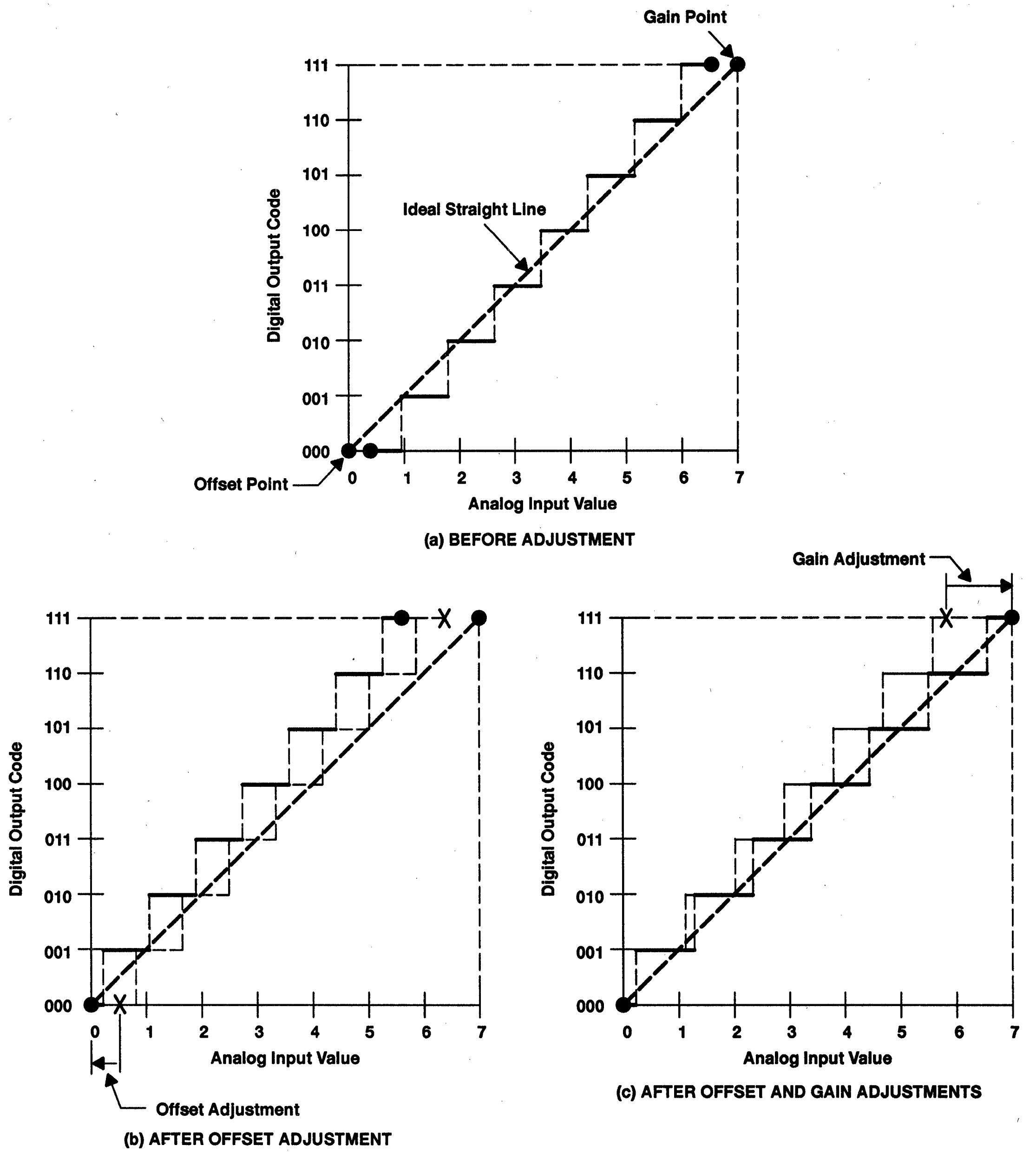
In this case, the identity:
1 LSB = analog resolution
leads, for an n-bit resolution, to:

$$1\ \text{LSB} = \frac{\text{FSR}}{2^n - 1} = \frac{\text{FSR(nom)}}{2^n}$$

Midstep Value (of an ADC)

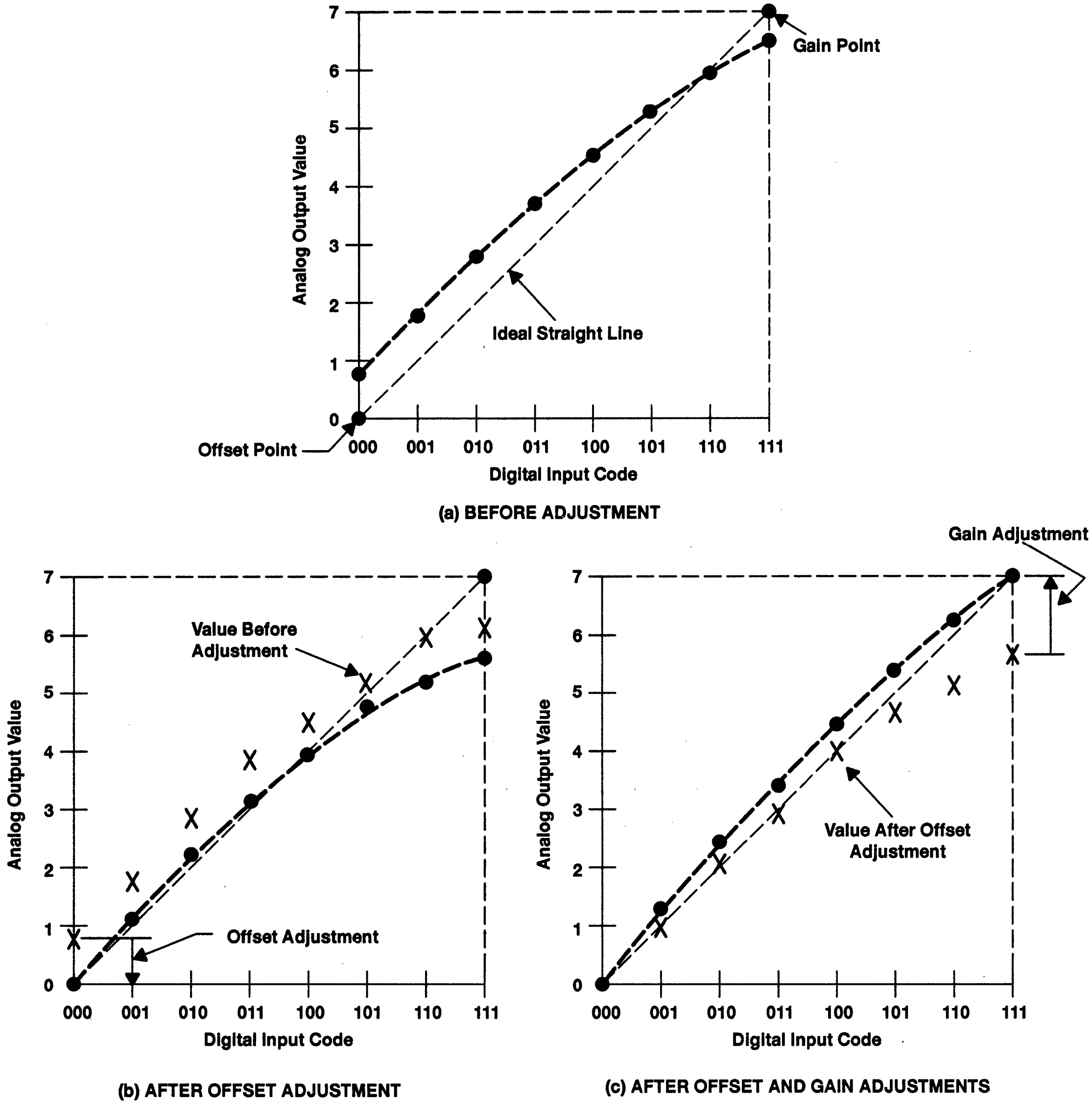
The analog value for the center of the step excluding the steps at the two ends of the total range of analog input values.

NOTE: For the end steps, the midstep value is defined as the analog value that results when the analog value for the transition to the adjacent step is reduced or enlarged, as appropriate, by half the nominal value of the step width (see Figure 1).



NOTE A: In the above examples, the offset point is referred to the step with the digital code 000, and the gain point is referred to the step with the digital code 111.

Figure 4. Adjustment in Offset Point and Gain Point for an ADC



NOTE A: In the above examples, the offset point is referred to the step with the digital code 000, and the gain point is referred to the step with the digital code 111.

Figure 5. Adjustment in Offset and Gain Point for a DAC

Midstep Value, Nominal (of an ADC)

A specified analog value within a step that is ideally represented free of error by the corresponding digital output code (see Figure 1).

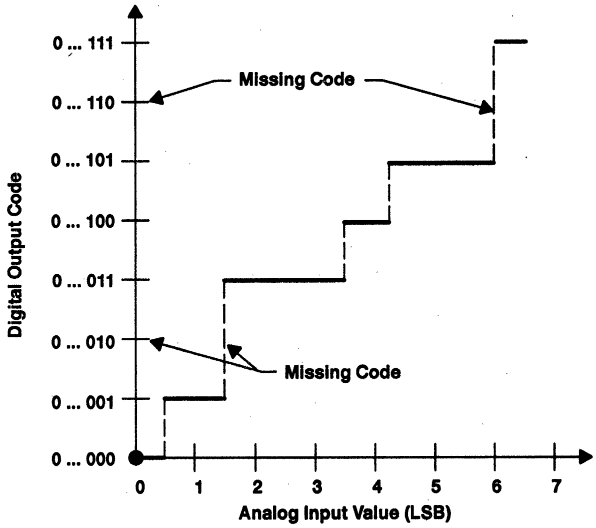


Figure 6. Missing Code for an ADC

Missing Code (of an ADC)

An intermediate code that is absent when the changing analog input to an ADC causes a multiple code change in the digital output (see Figure 6).

Monotonicity (of an ADC or a DAC)

A property of the transfer function that ensures the consistent increase or decrease of the analog output of a DAC or the digital output of an ADC in response to a consistent increase or decrease of the digital or analog input, respectively (Figure 7 illustrates nonmonotonic conversion).

NOTE: An intermediate increment with the value of zero does not invalidate monotonicity.

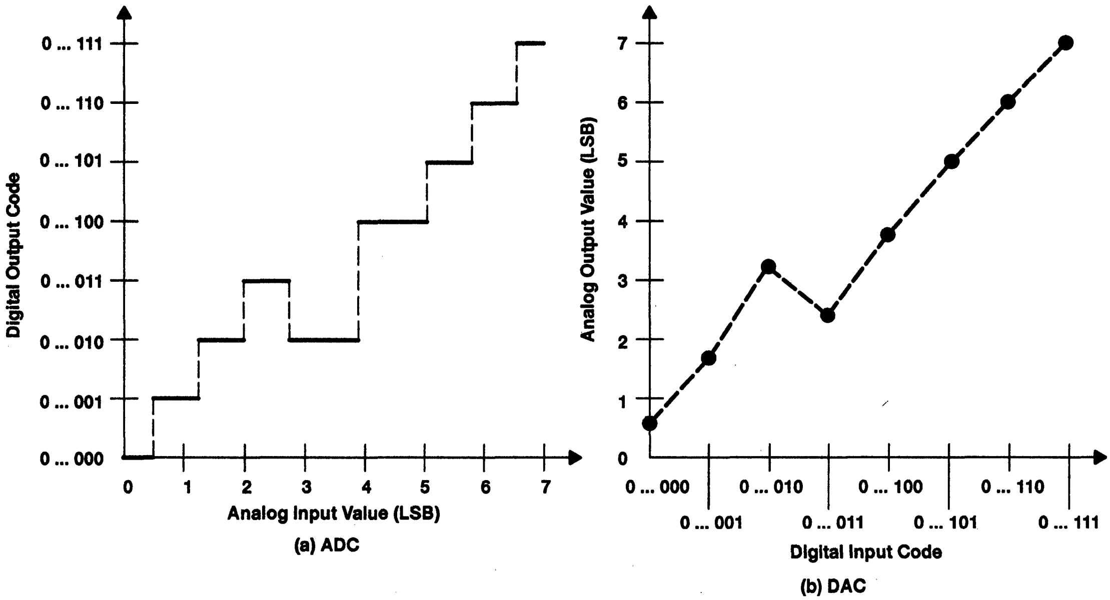


Figure 7. Nonmonotonic Conversion of an ADC or DAC

Multiplying DAC

A DAC having at least two inputs, at least one of which is digital, and whose analog output value is proportional to the product of the inputs.

Nonlinear ADC or DAC

An ADC or a DAC with a specified nonlinear transfer function between the nominal midstep values or nominal step values, respectively, and the corresponding step widths or step heights, respectively.

NOTE: The function may be continuously nonlinear or piece-wise linear.

Offset Point (of an adjustable ADC or DAC)

The point in the transfer diagram corresponding to the midstep value (for an ADC) or the step value (for a DAC) of the step about which the transfer diagram rotates when gain is adjusted (see Figures 4 and 5).

NOTE: Offset adjustment must be performed with respect to this point so that it causes only a parallel displacement of the transfer diagram, without changing its slope.

Resolution (general term)

NOTE 1: Resolution as a capability can be expressed in different forms: (see resolution, analog, resolution, numerical, and resolution, relative).

NOTE 2: Resolution is a design parameter and therefore has only a nominal value.

NOTE 3: The terms for these different forms may all be shortened to resolution if no ambiguity is likely to occur (for example, when the dimension of the term is also given).

Resolution (of an ADC)

The degree to which nearly equal values of the analog input quantity can be discriminated.

Resolution (of a DAC)

The degree to which nearly equal values of the analog output quantity can be produced.

Resolution, Analog (of a linear or nonlinear ADC or DAC)

For an ADC: The nominal value of the step width.
For a DAC: The nominal value of the step height.

NOTE: For a linear ADC or DAC, the constant magnitude of the analog resolution is often used as the reference unit LSB.

Resolution, Numerical

The number (n) of digits in the chosen numbering system necessary to express the total number of steps.

NOTE 1: The numbering system is normally a binary or a decimal system.

NOTE 2: In the binary-coded-decimal numbering system, the term 1/2 digit refers to an additional decimal digit with the highest positional value, but limited to the decimal figures 0 or 1 as it is represented by only a single bit. This additional digit serves to double the range of values covered by the other n digits.

Resolution, Relative (of a Linear ADC or DAC)

The ratio of the analog resolution to the full-scale range (practical or nominal).

NOTE: This ratio is normally expressed as a percentage of the full-scale range [% of FSR, % of FSR(nom)]. For high resolutions (high value of n), it is of little importance whether this ratio refers to the practical or nominal full-scale range.

Step (of an analog-to-digital or digital-to-analog conversion)

In the conversion code: Any of the individual correlations.

In the transfer diagram: Any part of the diagram equating to an individual correlation.

For an ADC, a step represents both a fractional range of analog input values and the corresponding digital output code (see Figure 1).

For a DAC, a step represents both a digital input code and the corresponding discrete analog output value (see Figure 2).

Step Height (Step Size) (of a DAC)

The absolute value of the difference in step value between two adjacent steps in the transfer diagram. (see Figure 2).

NOTE: For companding DACs, the term step size is in general use.

Step Value (of a DAC)

The value of the analog output representing a digital input code (see Figure 2).

Step Value, Nominal (of a DAC)

A specified step value that represents free of error the corresponding digital input code (see Figure 2).

Step Width (of an ADC)

The absolute value of the difference between the two ends of the range of analog values corresponding to one step (see Figure 1).

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Temperature Coefficients of Analog Characteristics (α)

NOTE 1: The letter symbol for the temperature coefficient of an analog characteristic consists of the letter symbol α with a subscript referring to the relevant characteristic.

Example: Temperature coefficient of the gain error: α_{EG}

NOTE 2: Temperature coefficients are usually specified in parts per million (relative to the full-scale value) per degrees Celsius, that is, in ppm/°C.

Zero Scale (of an ADC or a DAC with true zero) [see Figures 3(a) and 3(b)]

A term used to refer a characteristic to the step whose nominal midstep value or nominal step value equals zero.

NOTE 1: The subscript for the letter symbol of a characteristic at zero scale is ZS.

NOTE 2: In place of a letter symbol, the abbreviation ZS is in common use.

Zero Scale, Negative (of an ADC or a DAC with no true zero) [see Figure 3(c)]

A term used to refer a characteristic to the negative step closest to analog zero.

NOTE 1: The subscript for the letter symbol of a characteristic at negative zero scale is ZS– (V_{ZS-}, I_{ZS-}).

NOTE 2: In place of a letter symbol, the abbreviation ZS– is in common use.

Zero Scale, Positive (of an ADC or a DAC with no true zero) [see Figure 3(c)]

A term used to refer a characteristic to the positive step closest to analog zero.

NOTE 1: The subscript for the letter symbol of a characteristic at positive zero scale is ZS+ (V_{ZS+}, I_{ZS+}).

NOTE 2: In place of a letter symbol, the abbreviation ZS+ is in common use.

2. STATIC PERFORMANCE

Accuracy (see Errors, Part 4)

Asymmetry, Full-Scale (of a DAC with a bipolar analog range) (ΔI_{FSS}, ΔV_{FSS})

The difference between the absolute values of the two full-scale analog values.

Compliance, Current (of a DAC) ($I_{O(op)}$)

The permissible range of output current within which the specifications are valid.

Compliance, Voltage (of a DAC) ($V_{O(op)}$)

The permissible range of output voltage within which the specifications are valid.

Error (see Part 4)

Supply Voltage Sensitivity, (of a DAC) (k_{SVS})

The change in full scale output current (or voltage) caused by a change in supply voltage.

NOTE: This sensitivity is usually expressed as the ratio of the percent change of full-scale current (or voltage) to the percent change of supply voltage.

3. DYNAMIC PERFORMANCE

Conversion Rate (of an externally controlled ADC) (f_c)

The number of conversions per unit time.

NOTE 1: The maximum conversion rate should be specified for full resolution.

NOTE 2: The conversion rate is usually expressed as the number of conversions per second.

NOTE 3: Due to additionally needed settling or recovery times, the maximum specified conversion rate is smaller than the reciprocal of the worst-case conversion time.

Conversion Time (of an ADC) (t_c)

The time elapsed between the command to perform a conversion and the appearance at the converter output of the complete digital representation of the analog input value.

Delay Time, (Digital) (of a linear or a multiplying DAC) (t_d, t_{dd})

The time interval between the instant when the digital input changes and the instant when the analog output passes a specified value that is close to its initial value, ignoring glitches (see Figure 8).

NOTE : For a multiplying DAC, the full term and the additional subscript d must be used to distinguish between the digital and the delay time.

Delay Time, Reference (of a multiplying DAC) (t_{dr})

The time interval between the instant when a step change of the reference voltage occurs and the instant when the analog output passes a specified value that is close to its initial value.

Feedthrough Capacitance (C_F)

The value of the capacitance for a specified value of R in an equivalent circuit for the calculation of the feedthrough error.

NOTE: The equivalent circuit consists of a high-pass R-C filter between the reference input and the analog output.

Feedthrough Error (see Part 4)

Glitch (of a DAC)

A short, undesirable transient in the analog output occurring following a code change at the digital input (see Figure 8).

Glitch Area (of a DAC)

The time integral of the analog value of the glitch transient.

NOTE 1: Usually, the maximum specified glitch area refers to a specified worst-case code change.

NOTE 2: Instead of a letter symbol, the abbreviation GA is in use.

Glitch Energy (of a DAC)

The time integral of the electrical power of the glitch transient.

NOTE 1: Usually, the maximum specified glitch energy refers to a specified worst-case code change.

NOTE 2: Instead of a letter symbol, the abbreviation GE is in use.

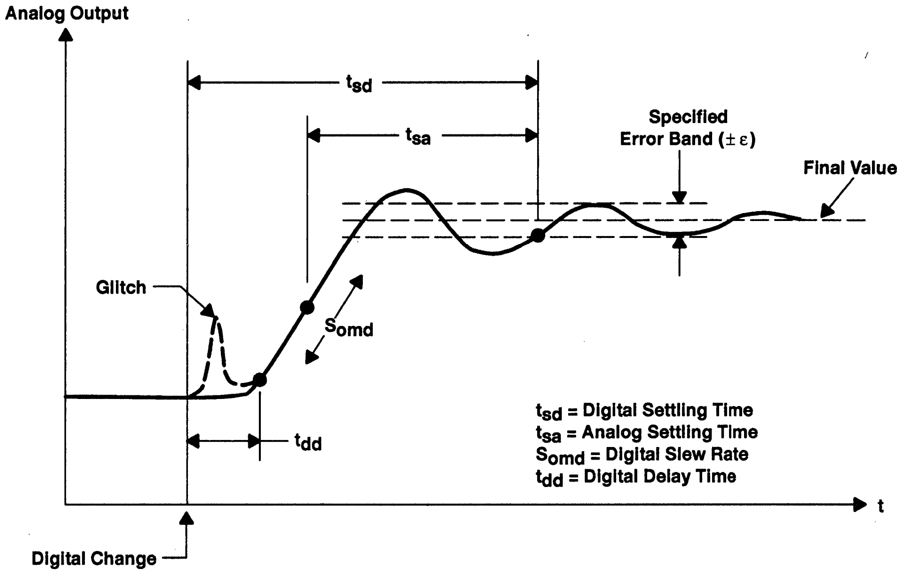


Figure 8. Output Characteristics of a Linear or a Multiplying DAC for a Step Change in the Digital Input Code

Pedestal (Error) (E_p) (see Part 4)

Ramp Delay, Steady-state (of a multiplying DAC) ($t_{d(ramp)}$)

The time separation between the actual curve of the analog output and the theoretical curve (with no delay) for a ramp in reference voltage, after the settling time to steady-state ramp has elapsed (see Figure 9).

Settling Time, Analog (of a DAC) (t_{sa})

The time interval between the instant when the analog output passes a specified value and the instant when the analog output enters for the last time a specified error band about its final value (see Figures 8 and 10).

Settling Time, (Digital) (of a linear or a multiplying DAC) (t_s, t_{sd})

The time interval between the instant when the digital input changes and the instant when the analog output value enters for the last time a specified error band about its final value (see Figure 8).

NOTE: For a multiplying DAC, the full term and the additional subscript d must be used to distinguish between the digital and the settling time.

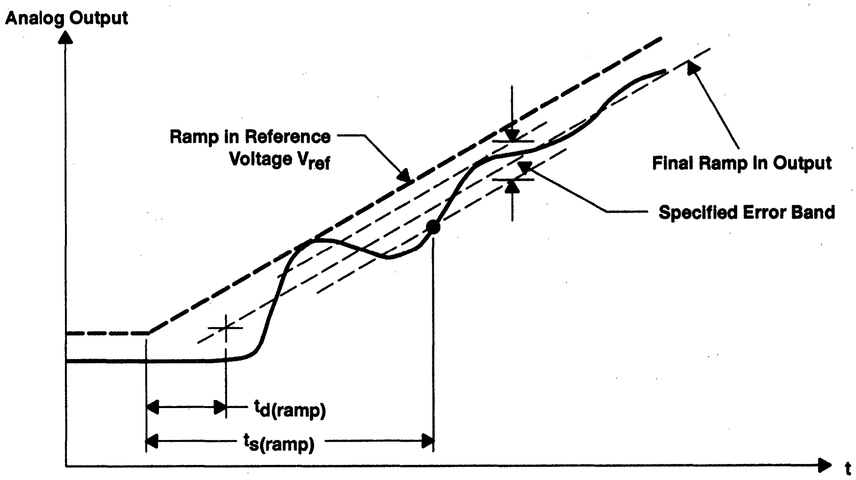
Settling Time, Reference (of a multiplying DAC) (t_{sr})

The time interval between the instant when a step change of the reference voltage occurs and the instant when the analog output enters for the last time a specified error band about its final value (see Figure 10).

NOTE: Specifications for the reference settling time are usually given for the highest allowed step change in reference voltage.

Settling Time to Steady-State Ramp (of a multiplying DAC) ($t_{s(ramp)}$)

The time interval between the instant a ramp in the reference voltage starts and the instant when the analog output value enters for the last time a specified error band about the final ramp in the output (see Figure 9).



$t_{s(ramp)}$ = Settling Time to Steady-State Ramp Delay
$t_{d(ramp)}$ = Steady-State Ramp Delay

Figure 9. Output Characteristics for a Ramp in Reference Voltage of a Multiplying DAC

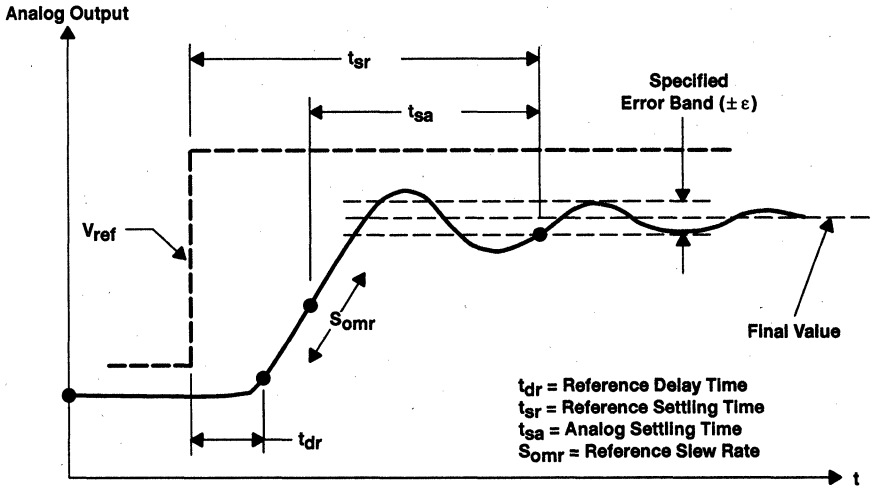


Figure 10. Output Characteristics for a Step Change in Reference Voltage of a Multiplying DAC

Skewing Time, Internal (of a DAC)

The difference in internal delay between the individual output transitions for a given change of digital input.

NOTE: The internal (and external) skew has a major influence on the settling time for critical changes in the digital input, for example, for a 1-LSB change from 011 . . . 111 to 100 . . . 000, and is an important source of commutation noise.

Slew Rate, (Digital) (of a linear or a multiplying DAC) (S_{OM}, S_{OMD})

The maximum rate of change of the analog output value when a change of the digital input code causes a large step change of the analog output value (see Figure 8).

NOTE 1: For a multiplying DAC, the full term and the additional subscript D must be used to distinguish between the digital and the slew rate.

NOTE 2: The abbreviations SR and SR(dig) are also used.

Slew Rate, Reference (of a multiplying DAC) (S_{OMR})

The maximum rate of change of the analog output following a large step change of the reference voltage (see Figure 10).

NOTE: The abbreviation SR(ref) is also used.

4. ERRORS, ACCURACY

The definitions in this section describe the errors as the difference between the actual value and the nominal value of the analog quantity. As such they may be expressed in conventional units (for example, millivolts) or as multiples or submultiples of 1 LSB. An error can also be expressed as a relative value, for example, in % of FSR. In this case, it is common practice to use the same term as for the analog value.

Absolute Accuracy Error

Synonym for total error.

Feedthrough Error (of a multiplying DAC) (E_F)

An error in analog output due to variation in the reference voltage that appears as an offset error and is proportional to frequency and amplitude of the reference signal.

NOTE 1: The specification for the feedthrough error is given for the digital input for which the offset error is specified, and for a reference signal of specified frequency and amplitude.

NOTE 2: This error may also be expressed as a peak-to-peak analog value.

Full-Scale Error (of a linear ADC or DAC) (E_{FS})

The difference between the actual midstep value or step value and the nominal midstep value or step value, respectively, at specified full scale.

NOTE: Normally, this error specification is applied to converters that have no arrangement for an external adjustment of offset error and gain error.

Gain Error (of a linear ADC or DAC) (E_G)

For an ADC: The difference between the actual midstep value and the nominal midstep value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero [see Figure 11(a)].

For a DAC: The difference between the actual step value and the nominal step value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero [see Figure 11(b)].

NOTE: See Notes 1 and 2 under Offset Error.

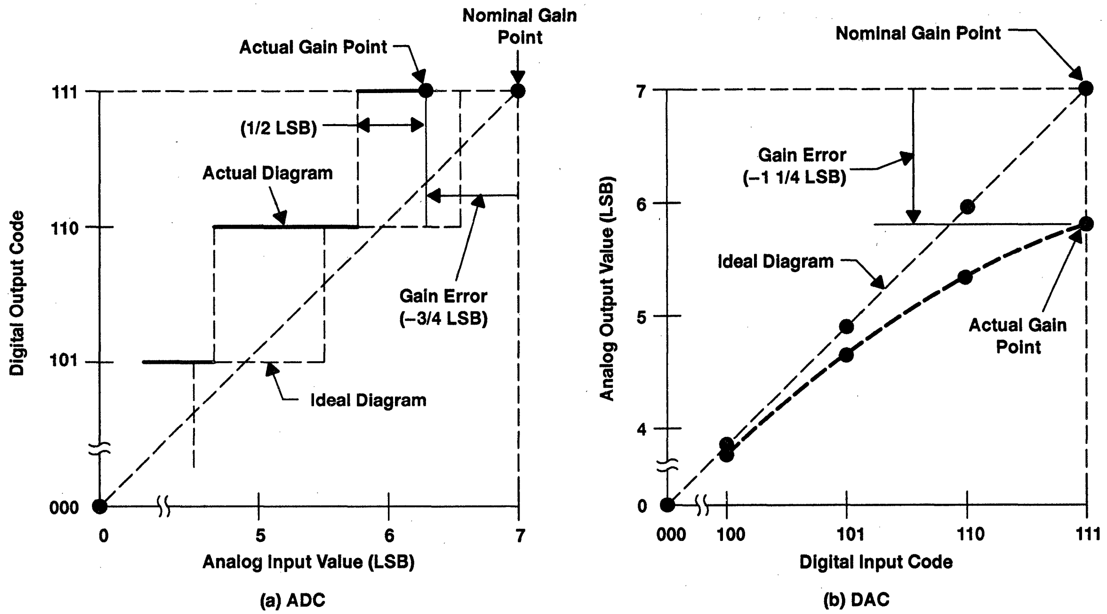


Figure 11. Gain Error of a Linear 3-Bit Natural Binary Code Converter (Specified at Step 111), After Correction of the Offset Error

Instability, Long-Term (Accuracy) ($\Delta E_{(\Delta t)}$, $\Delta E_{(t)}$)

The additional error caused by the aging of the components and specified for a longer period in time.

Linearity Error, Best-Straight-Line (of a linear and adjustable ADC) ($E_{L(adj)}$)

The difference between the actual analog value at the transition between any two adjacent steps and its ideal value after offset error and gain error have been adjusted to minimize the magnitude of the extreme values of this difference [see Figure 12(a)].

NOTE 1: The inherent quantization error is not included in the best-straight-line linearity error of an ADC. The ideal value for the transition corresponds to the nominal midstep value ±1/2 LSB.

NOTE 2: For a uniformly curved transfer diagram, the extreme values will be very close to half of the magnitude of the end-point linearity error [see Figure 12(a)].

Linearity Error, Best-Straight-Line (of a linear and adjustable DAC) ($E_{L(adj)}$)

The difference between the actual step value and the nominal step value after offset error and gain error have been adjusted to minimize the magnitude of the extreme values of this difference [see Figure 12(b)].

NOTE: For a uniformly curved transfer diagram, the extreme values will be very close to half of the magnitude of the end-point linearity error [see Figure 12(b)].

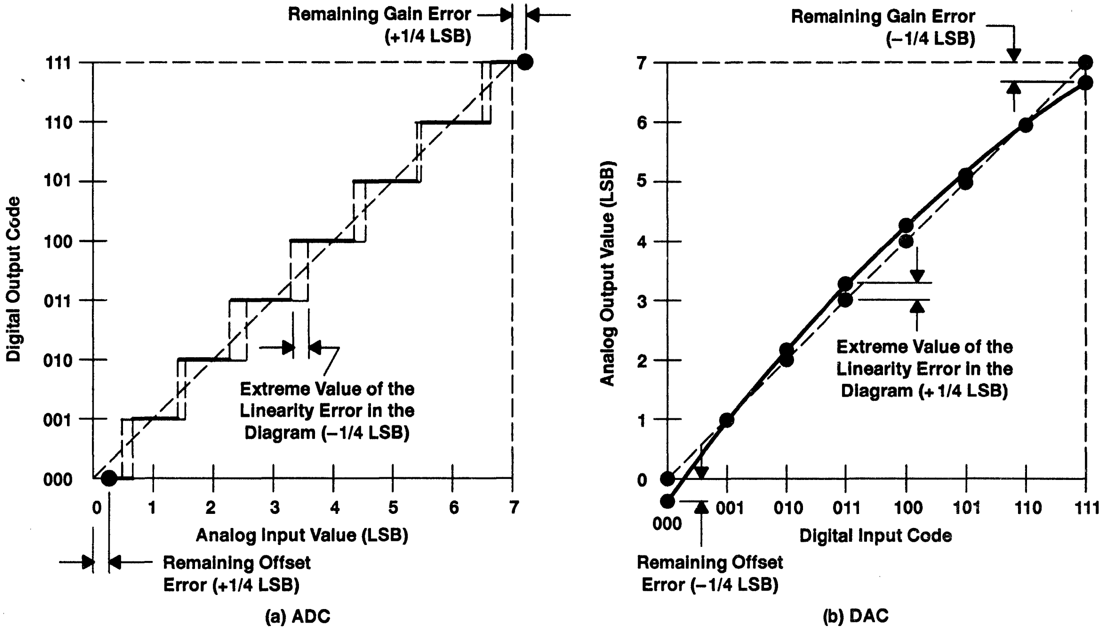


Figure 12. Best-Straight-Line Linearity Error of a Linear 3-Bit Natural Binary-Coded Converter (Values Between ±1/4 LSB)

Linearity Error, Differential (of a linear ADC or DAC) (E_D)

The difference between the actual step width or step height and the ideal value (1 LSB) (see Figure 13).

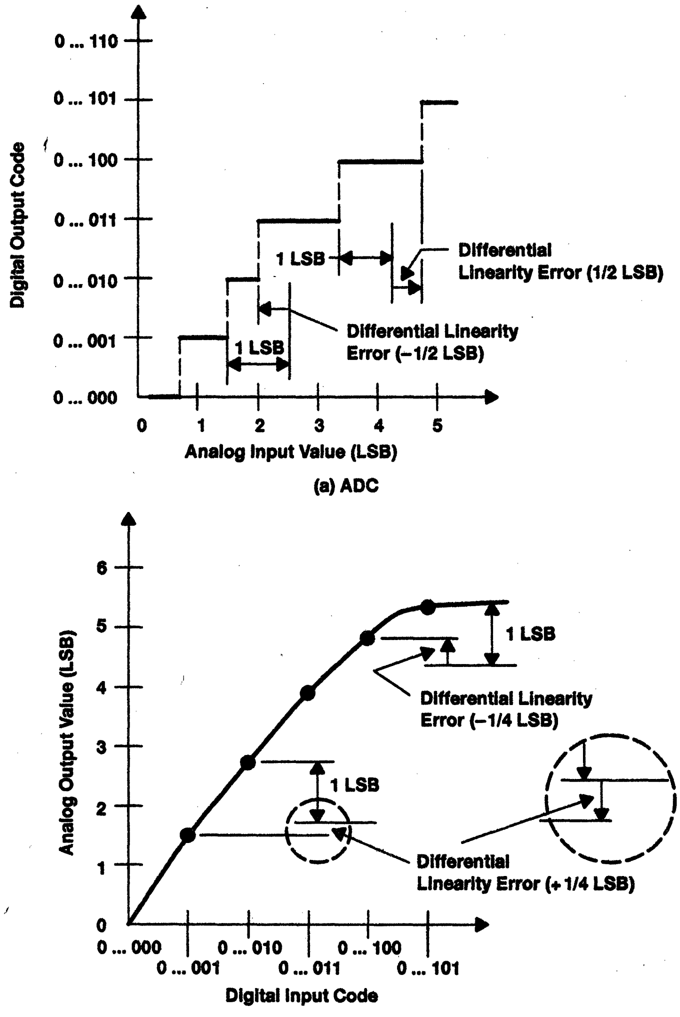
NOTE: A differential linearity error greater than 1 LSB can lead to missing codes in an ADC or to nonmonotonicity of an ADC or a DAC (see Figures 6 and 7).

Linearity Error, End-Point (of a linear and adjustable ADC) (E_L)

The difference between the actual analog value at the transition between any two adjacent steps and its ideal value after offset error and gain error have been adjusted to zero [see Figure 14(a)].

NOTE 1: The short term linearity error is in common use and is sufficient if no ambiguity with the best-straight-line linearity error is likely to occur.

NOTE 2: The inherent quantization error is not included in the linearity error of an ADC. The ideal value for the transition corresponds to the nominal midstep value ±1/2 LSB.



(a) ADC

(b) DAC

Figure 13. Differential Linearity Error of a Linear ADC or DAC

Linearity Error, End-Point (of a linear and adjustable DAC) (E_L)

The difference between the actual step value and the nominal step value after offset error and gain error have been adjusted to zero [see Figure 14(b)].

NOTE : The short term linearity error is in common use and is sufficient if no ambiguity with the best-straight-line linearity error is likely to occur.

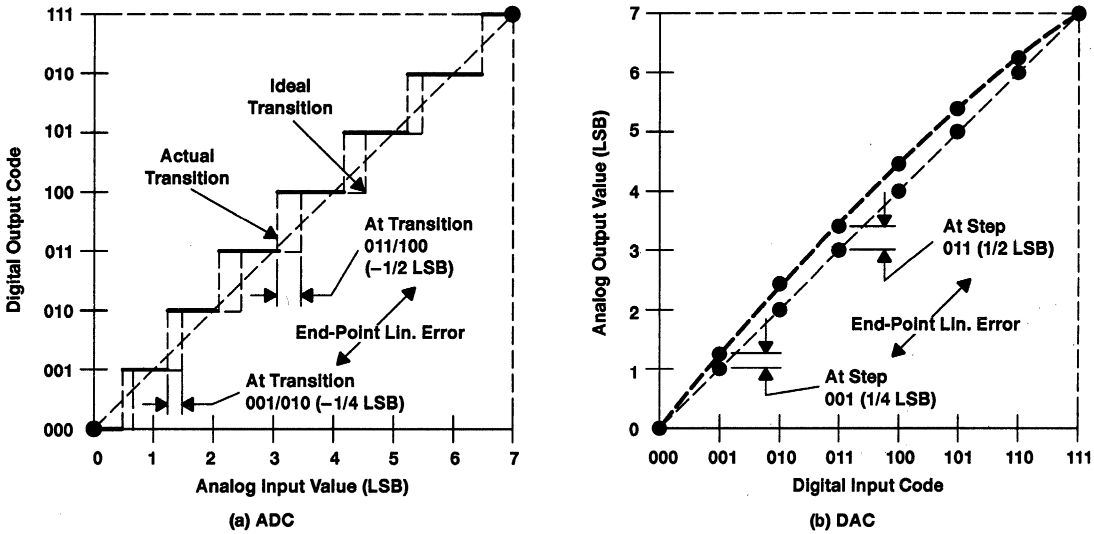


Figure 14. End-Point Linearity Error of a Linear 3-Bit Natural Binary-Coded ADC or DAC (Offset Error and Gain Error are Adjusted to the Value Zero)

Offset Error (of a linear ADC or DAC) (E_O)

For an ADC: The difference between the actual midstep value and the nominal midstep value at the offset point [see Figure 15(a)].

For a DAC: The difference between the actual step value and the nominal step value at the offset point [see Figure 15(b)].

NOTE 1: Usually, the specified steps for the specification of offset error and gain error are the steps at the ends of the practical full-scale range. For an ADC, the midstep value of these steps is defined as the value for a point 1/2 LSB apart from the adjacent transition (see Figures 11 and 15).

NOTE 2: The terms offset error and gain error should be used only for error that can be adjusted to zero. Otherwise, the terms zero-scale error and full-scale error should be used.

Pedestal (Error) (E_P)

A dynamic offset produced in the commutation process.

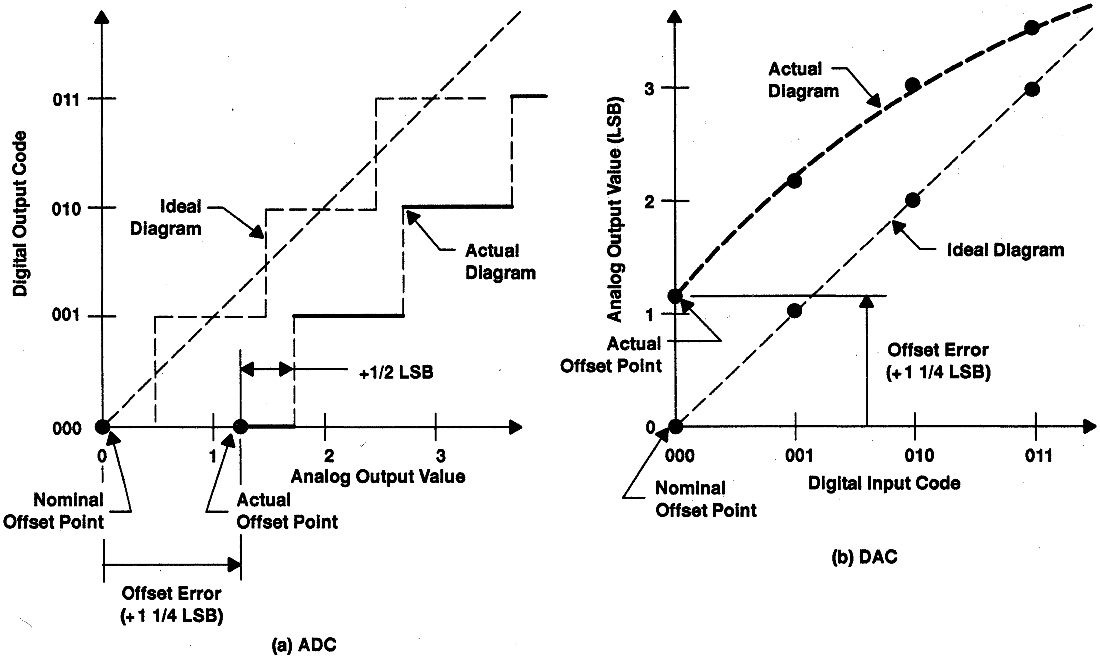


Figure 15. Offset Error of a Linear 3-Bit Natural Binary Code Converter (Specified at Step 000)

Quantization Error, Inherent (of an ideal ADC)

Within a step, the maximum (positive or negative) possible deviation of the actual analog input value from the nominal midstep value.

NOTE 1: This error follows necessarily from the quantization procedure. For a linear ADC, its value equals ±1/2 LSB (see Figure 1).

NOTE 2: The term resolution error for the inherent quantization error is deprecated, because resolution as a design parameter has only a nominal value.

Rollover Error (of an ADC with decimal output and auto-polarity) (E_{RO})

The difference in output readings with the analog input switched between positive and negative values of the same magnitude (close to full scale).

Total Error (of a linear ADC) (E_T)

The maximum difference (positive or negative) between an analog value and the nominal midstep value within any step [see Figure 16(a)].

NOTE 1: If this error is expressed as a relative value, the term relative accuracy error should be used instead of absolute accuracy error.

NOTE 2: This error includes contributions from offset error, gain error, linearity error, and the inherent quantization error.

Total Error (of a linear DAC) (E_T)

The difference (positive or negative) between the actual step value and the nominal step value for any step [see Figure 16(b)].

NOTE 1: If this error is expressed as a relative value, the term relative accuracy error should be used instead of absolute accuracy error.

NOTE 2: This error includes contributions from offset error, gain error, and linearity error.

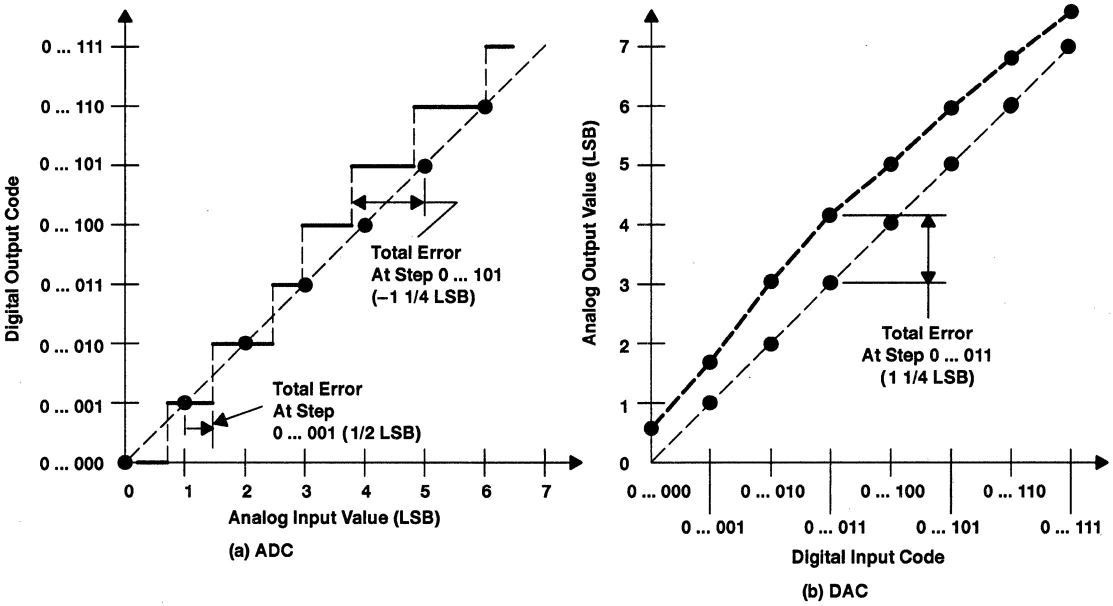


Figure 16. Absolute Accuracy Error, Total Error of a Linear ADC or DAC

Zero-Scale Error (of a linear ADC or DAC) (E_{ZS})

The difference between the actual midstep value or step value and the nominal midstep value or step value, respectively, at specified zero scale.

NOTE: Normally, this error specification is applied to converters that have no arrangement for an external adjustment of offset error and gain error.

5. Dynamic and Sigma-Delta Definitions

Resolution

The number of different output codes possible. Expressed as N, where 2^N is the number of available output codes.

Dynamic Range

The ratio of the largest allowable input signal to the noise floor.

Total Harmonic Distortion

The ratio of the rms sum of all harmonics to the rms value of the largest allowable input signal. Units in dB's.

Signal to Intermodulation Distortion

The ratio of the rms sum of two input signals to the rms sum of all discernible intermodulation and harmonic distortion products.

Linearity Error

The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. Zero-scale is a point 1/2 LSB below the first code transition and full-scale is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in %FS.

Differential Nonlinearity

The deviation of a code's width from the ideal width in LSB's.

Positive Full Scale Error

The deviation of the last code transition from the ideal, (V_{ref} – 1.5 LSB).

Positive Full Scale Drift

The drift in effective, positive, full-scale input voltage with temperature.

Negative Full Scale Error

The deviation of the first code transition from the ideal, ($-V_{ref}$ + 0.5 LSB).

Negative Full Scale Drift

The drift in effective, negative, full-scale input voltage with temperature.

Bipolar Offset

The deviation of the midscale transition from the ideal. The ideal is defined as the middle transition lying on a straight line between actual positive full-scale and actual negative full-scale.

Bipolar Offset Drift

The drift in the bipolar offset error with temperature.

Absolute Group Delay

The delay through the filter section of the part.

Passband Frequency

The upper –3 dB frequency.

ICL7135C, TLC7135C
4 1/2-DIGIT PRECISION
ANALOG-TO-DIGITAL CONVERTERS

SLAS074A – DECEMBER 1986 – REVISED MAY 1995

- **Zero Reading for 0-V Input**
- **Precision Null Detection With True Polarity at Zero**
- **1-pA Typical Input Current**
- **True Differential Input**
- **Multiplexed Binary-Coded-Decimal (BCD) Output**
- **Low Rollover Error: ± 1 Count Max**
- **Control Signals Allow Interfacing With UARTs or Microprocessors**
- **Autoranging Capability With Over-and Under-Range Signals**
- **TTL-Compatible Outputs**
- **Direct Replacement for Teledyne TSC7135, Intersil ICL7135, Maxim ICL7135, and Siliconix SI7135**
- **CMOS Technology**

N PACKAGE
(TOP VIEW)

V_{CC-}	1	28	UNDER RANGE
REF	2	27	OVER RANGE
ANLG COMMON	3	26	$\overline{\text{STROBE}}$
INT OUT	4	25	RUN/$\overline{\text{HOLD}}$
AUTO ZERO	5	24	DGTL GND
BUFF OUT	6	23	POLARITY
C_{ref-}	7	22	CLK
C_{ref+}	8	21	BUSY
IN–	9	20	D1
IN+	10	19	D2
V_{CC+}	11	18	D3
D5	12	17	D4
B1	13	16	B8
B2	14	15	B4

description

The ICL7135C and TLC7135C converters are manufactured with Texas Instruments highly efficient CMOS technology. This 4 1/2-digit, dual-slope-integrating, analog-to-digital converter (DAC) is designed to provide interfaces to both a microprocessor and a visual display. The digit-drive outputs D1 through D4 and multiplexed binary-coded-decimal outputs B1, B2, B4, and B8 provide an interface for LED or LCD decoder/drivers as well as microprocessors.

The ICL7135C and TLC7135C offer 50-ppm (one part in 20,000) resolution with a maximum linearity error of one count. The zero error is less than 10 µV and zero drift is less than 0.5 µV/°C. Source-impedance errors are minimized by low input current (less than 10 pA). Rollover error is limited to ± 1 count.

The BUSY, $\overline{\text{STROBE}}$, RUN/$\overline{\text{HOLD}}$, OVER RANGE, and UNDER RANGE control signals support microprocessor-based measurement systems. The control signals also can support remote data acquisition systems with data transfer through universal asynchronous receiver transmitters (UARTs).

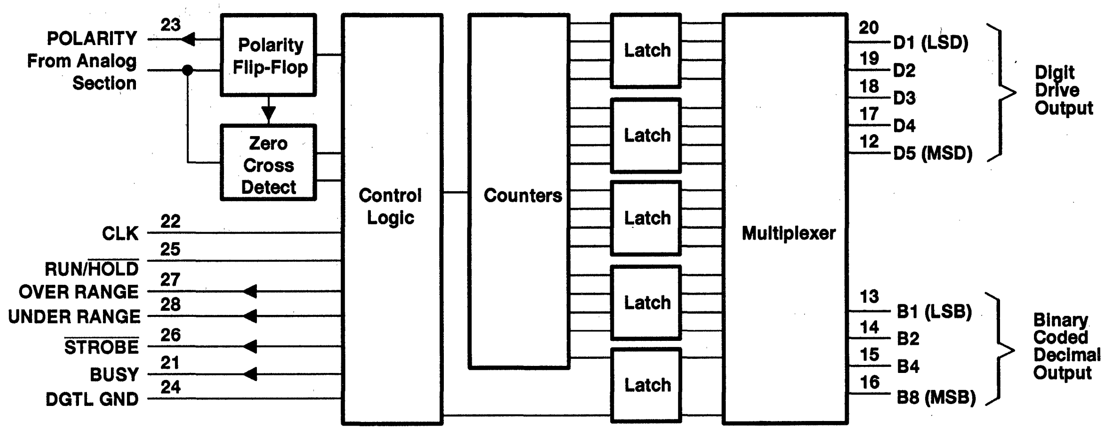
The ICL7135C and TLC7135C are characterized for operation from 0°C to 70°C.

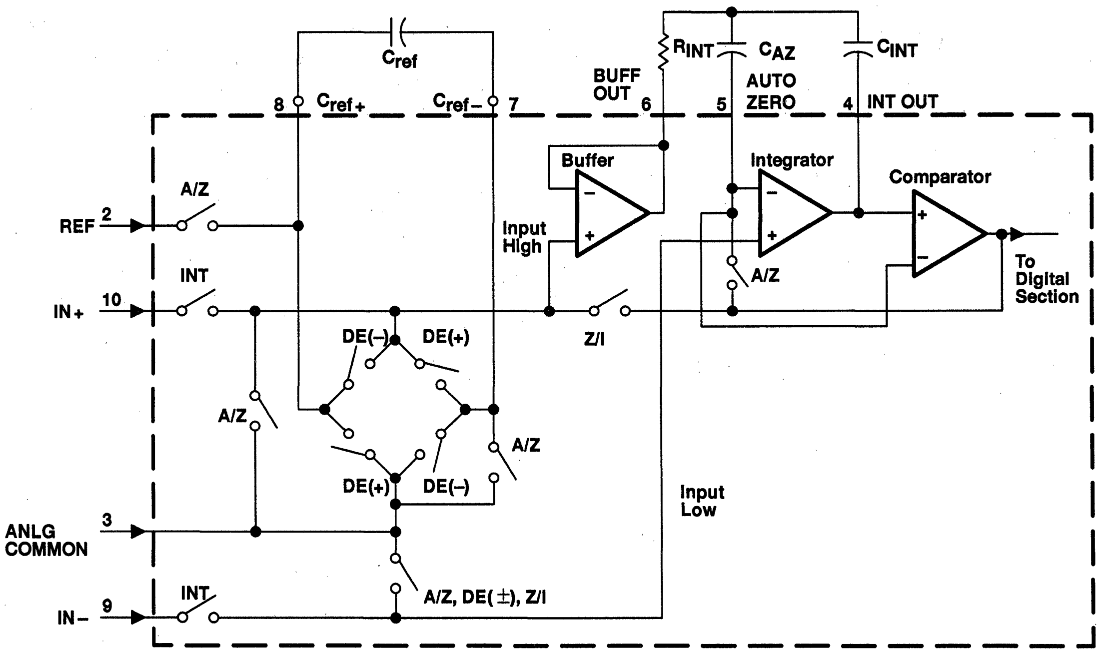
AVAILABLE OPTIONS

T_A	PACKAGE PLASTIC DIP (N)
0°C to 70°C	ICL7135CN
	TLC7135CN

Caution. These devices have limited built-in protection. The leads should be shorted together or the device placed in conductive foam during storage or handliing to prevent electrostatic damage to the MOS gates.

functional block diagram





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{CC+} with respect to V_{CC-}) .... 15 V
Analog input voltage (IN– or IN+) .... V_{CC-} to V_{CC+}
Reference voltage range .... V_{CC-} to V_{CC+}
Clock input voltage range .... 0 V to V_{CC+}
Operating free-air temperature range, T_A .... 0°C to 70°C
Storage temperature range, T_{stg} .... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4	5	6	V
Supply voltage, V_{CC-}	–3	–5	–8	V
Reference voltage, V_{ref}		1		V
High-level input voltage, CLK, RUN/$\overline{HOLD}$, V_{IH}	2.8			V
Low-level input voltage, CLK, RUN/$\overline{HOLD}$, V_{IL}			0.8	V
Differential input voltage, V_{ID}	V_{CC-} +1		V_{CC+} –0.5	V
Maximum operating frequency, f_{clock} (see Note 1)	1.2	2		MHz
Operating free-air temperature range, T_A	0		70	°C

NOTE 1: Clock frequency range extends down to 0 Hz.

electrical characteristics, V_{CC+} = 5 V, V_{CC-} = 5 V, V_{ref} = 1 V, f_{clock} = 120 kHz, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	D1-D5,B1,B2,B4,B8	I_O = –1 mA		2.4		5	V
		Other outputs	I_O = –10 µA		4.9		5	
V_{OL}	Low-level output voltage		I_O = 1.6 mA				0.4	V
$V_{ON(PP)}$	Peak-to-peak output noise voltage (see Note 2)		V_{ID} = 0,	Full scale = 2 V		15		µV
α_{VO}	Zero-reading temperature coefficient of output voltage		V_{ID} = 0,	0°C ≤ T_A ≤ 70°C		0.5	2	µV/°C
I_{IH}	High-level input current		V_I = 5 V,	0°C ≤ T_A ≤ 70°C		0.1	10	µA
I_{IL}	Low-level input current		V_I = 0 V,	0°C ≤ T_A ≤ 70°C		–0.02	–0.1	mA
I_I	Input leakage current, IN– and IN+		V_{ID} = 0	T_A = 25°C		1	10	pA
				0°C ≤ T_A ≤ 70°C			250	
I_{CC+}	Positive supply current		f_{clock} = 0	T_A = 25°C		1	2	mA
				0°C ≤ T_A ≤ 70°C			3	
I_{CC-}	Negative supply current		f_{clock} = 0	T_A = 25°C		–0.8	–2	mA
				0°C ≤ T_A ≤ 70°C			–3	
C_{pd}	Power dissipation capacitance		See Note 3			40		pF

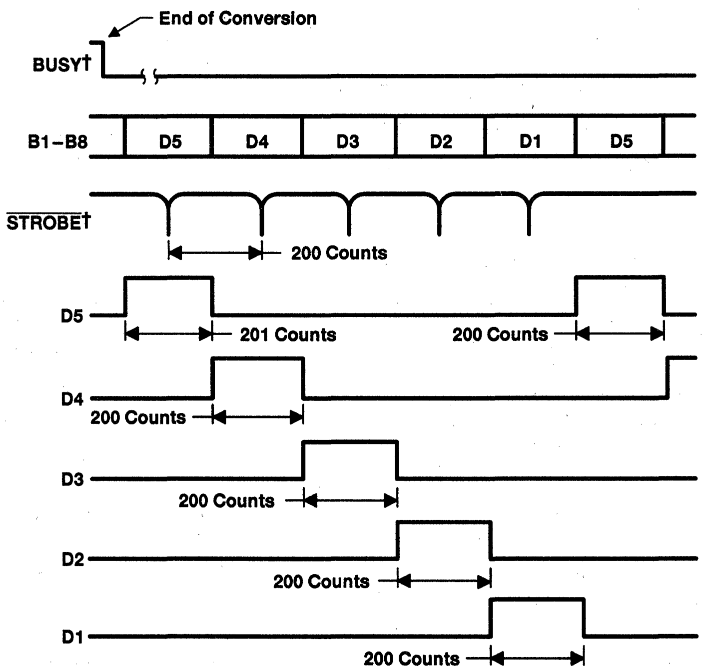
NOTES: 2. This is the peak-to-peak value that is not exceeded 95% of the time.
3. Factor-relating clock frequency to increase in supply current. At V_{CC+} = 5 V, $I_{CC+} = I_{CC+}(f_{clock} = 0) + C_{pd} \times 5\text{ V} \times f_{clock}$

operating characteristics, V_{CC+} = 5 V, V_{CC-} = 5 V, V_{ref} = 1 V, f_{clock} = 120 kHz, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
α_{FS}	Full-scale temperature coefficient (see Note 4)	V_{ID} = 2 V, 0°C ≤ T_A ≤ 70°C			5	ppm/°C
E_L	Linearity error	−2 V ≤ V_{ID} ≤ 2 V		0.5		count
E_D	Differential linearity error (see Note 5)	−2 V ≤ V_{ID} ≤ 2 V		0.01		LSB
E_{FS}	± Full-scale symmetry error (rollover error) (see Note 6)	V_{ID} = ±2 V		0.5	1	count
	Display reading with 0-V input	V_{ID} = 0, 0°C ≤ T_A ≤ 70°C	−0.0000	±0.0000	0.0000	Digital Reading
	Display reading in ratiometric operation	V_{ID} = V_{ref}, T_A = 25°C	0.9998	0.9999	1.0000	Digital Reading
		0°C ≤ T_A ≤ 70°C	0.9995	0.9999	1.0005	

NOTES: 4. This parameter is measured with an external reference having a temperature coefficient of less than 0.01 ppm/°C.
5. The magnitude of the difference between the worst case step of adjacent counts and the ideal step.
6. Rollover error is the difference between the absolute values of the conversion for 2 V and −2 V.

timing diagrams



† Delay between BUSY going low and the first $\overline{\text{STROBE}}$ pulse is dependent upon the analog input.

Figure 1

timing diagrams (continued)

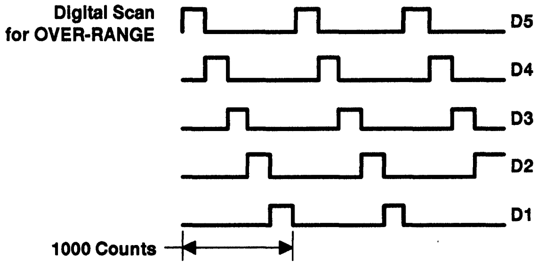


Figure 2

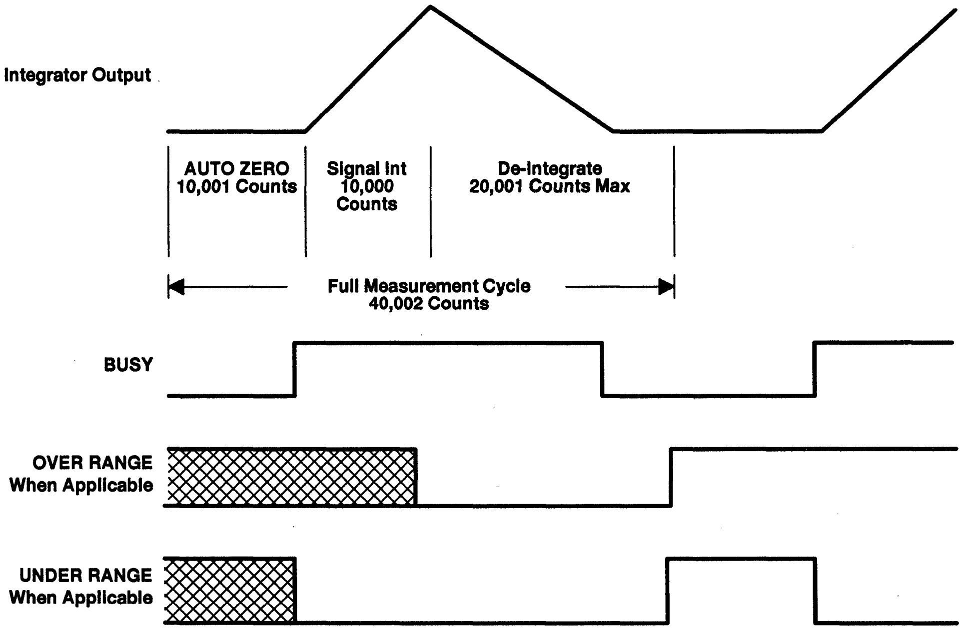
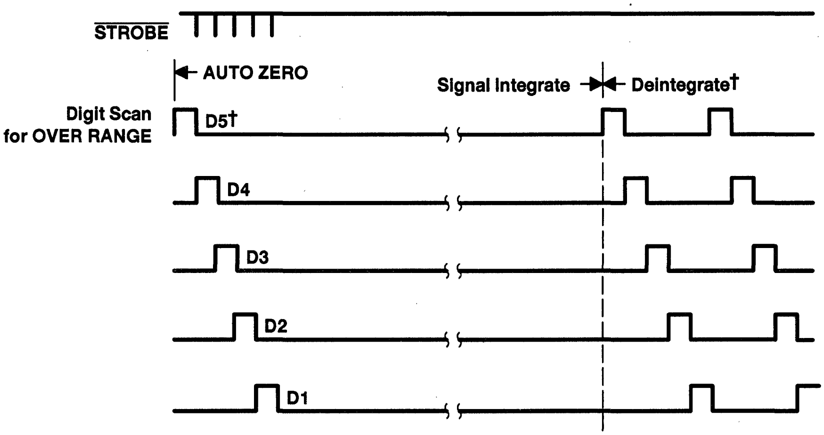


Figure 3

timing diagrams (continued)



† First D5 of AUTO ZERO and deintegrate is one count longer.

Figure 4

PRINCIPLES OF OPERATION

A measurement cycle for the ICL7135C and TLC7135C consists of the following four phases.

1. Auto-Zero Phase. The internal IN+ and IN– inputs are disconnected from the terminals and internally connected to ANLG COMMON. The reference capacitor is charged to the reference voltage. The system is configured in a closed loop and the auto-zero capacitor is charged to compensate for offset voltages in the buffer amplifier, integrator, and comparator. The auto-zero accuracy is limited only by the system noise, and the overall offset, as referred to the input, is less than 10 μV.
2. Signal Integrate Phase. The auto-zero loop is opened and the internal IN+ and IN– inputs are connected to the external terminals. The differential voltage between these inputs is integrated for a fixed period of time. When the input signal has no return with respect to the converter power supply, IN– can be tied to ANLG COMMON to establish the correct common-mode voltage. Upon completion of this phase, the polarity of the input signal is recorded.
3. deintegrate Phase. The reference is used to perform the deintegrate task. The internal IN- is internally connected to ANLG COMMON and IN+ is connected across the previously charged reference capacitor. The recorded polarity of the input signal ensures that the capacitor is connected with the correct polarity so that the integrator output polarity returns to zero. The time required for the output to return to zero is proportional to the amplitude of the input signal. The return time is displayed as a digital reading and is determined by the equation 10,000 × (V_{ID}/V_{ref}). The maximum or full-scale conversion occurs when V_{ID} is two times V_{ref}.
4. Zero Integrator Phase. The internal IN– is connected to ANLG COMMON. The system is configured in a closed loop to cause the integrator output to return to zero. Typically, this phase requires 100 to 200 clock pulses. However, after an over-range conversion, 6200 pulses are required.

PRINCIPLES OF OPERATION

description of analog circuits

input signal range

The common mode range of the input amplifier extends from 1 V above the negative supply to 1 V below the positive supply. Within this range, the common-mode rejection ratio (CMRR) is typically 86 dB. Both differential and common-mode voltages cause the integrator output to swing. Therefore, care must be exercised to ensure that the integrator output does not become saturated.

analog common

Analog common (ANLG COMMON) is connected to the internal IN– during the auto-zero, deintegrate, and zero integrator phases. When IN– is connected to a voltage that is different than analog common during the signal integrate phase, the resulting common-mode voltage is rejected by the amplifier. However, in most applications, IN– is set at a known fixed voltage (i.e., power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. Removing the common-mode voltage in this manner slightly increases conversion accuracy.

reference

The reference voltage is positive with respect to analog common. The accuracy of the conversion result is dependent upon the quality of the reference. Therefore, to obtain a high accuracy conversion, a high quality reference should be used.

description of digital circuits

RUN/$\overline{\text{HOLD}}$ input

When RUN/$\overline{\text{HOLD}}$ is high or open, the device continuously performs measurement cycles every 40,002 clock pulses. When this input is taken low, the integrated circuit continues to perform the ongoing measurement cycle and then hold the conversion reading for as long as the terminal is held low. When the terminal is held low after completion of a measurement cycle, a short positive pulse (greater than 300 ns) initiates a new measurement cycle. When this positive pulse occurs before the completion of a measurement cycle, it will not be recognized. The first $\overline{\text{STROBE}}$ pulse, which occurs 101 counts after the end of a measurement cycle, is an indication of the completion of a me asurement cycle. Thus, the positive pulse could be used to trigger the start of a new measurement after the first $\overline{\text{STROBE}}$ pulse.

$\overline{\text{STROBE}}$ input

Negative going pulses from this input transfer the BCD conversion data to external latches, UARTs, or microprocessors. At the end of the measurement cycle, $\overline{\text{STROBE}}$ goes high and remains high for 201 counts. The most significant digit (MSD) BCD bits are placed on the BCD terminals. After the first 101 counts, halfway through the duration of output D1–D5 going high, the $\overline{\text{STROBE}}$ terminal goes low for 1/2 clock pulse width. The placement of the $\overline{\text{STROBE}}$ pulse at the midpoint of the D5 high pulse allows the information to be latched into an external device on either a low-level or an edge. Such placement of the $\overline{\text{STROBE}}$ pulse also ensures that the BCD bits for the second MSD are not yet competing for the BCD lines and latching of the correct bits is ensured. The above process is repeated for the second MSD and the D4 output. Similarly, the process is repeated through the least significant digit (LSD). Subsequently, inputs D5 through D1 and the BCD lines continue scanning without the inclusion of $\overline{\text{STROBE}}$ pulses. This subsequent continuous scanning causes the conversion results to be continuously displayed. Such subsequent scanning does not occur when an over-range condition occurs.

PRINCIPLES OF OPERATION

BUSY output

The BUSY output goes high at the beginning of the signal integrate phase. BUSY remains high until the first clock pulse after zero crossing or at the end of the measurement cycle when an over-range condition occurs. It is possible to use the BUSY terminal to serially transmit the conversion result. Serial transmission can be accomplished by ANDing the BUSY and CLOCK signals and transmitting the ANDed output. The transmitted output consists of 10,001 clock pulses, which occur during the signal integrate phase, and the number of clock pulses that occur during the deintegrate phase. The conversion result can be obtained by subtracting 10,001 from the total number of clock pulses.

OVER-RANGE output

When an over-range condition occurs, this terminal goes high after the BUSY signal goes low at the end of the measurement cycle. As previously noted, the BUSY signal remains high until the end of the measurement cycle when an over-range condition occurs. The OVER RANGE output goes high at the end of BUSY and goes low at the beginning of the deintegrate phase in the next measurement cycle.

UNDER-RANGE output

At the end of the BUSY signal, this terminal goes high when the conversion result is less than or equal to 9% (count of 1800) of the full-scale range. The UNDER RANGE output is brought low at the beginning of the signal integrate phase of the next measurement cycle.

POLARITY output

The POLARITY output is high for a positive input signal and updates at the beginning of each deintegrate phase. The polarity output is valid for all inputs including ±0 and OVER RANGE signals.

digit-drive (D1, D2, D4 and D5) outputs

Each digit-drive output (D1 through D5) sequentially goes high for 200 clock pulses. This sequential process is continuous unless an over-range occurs. When an over-range occurs, all of the digit-drive outputs are blanked from the end of the strobe sequence until the beginning of the deintegrate phase (when the sequential digit-drive activation begins again). The blanking activity during an over-range condition can cause the display to flash and indicate the over-range condition.

BCD outputs

The BCD bits (B1, B2, B4 and B8) for a given digit are sequentially activated on these outputs. Simultaneously, the appropriate digit-drive line for the given digit is activated.

system aspects

integrating resistor

The value of the integrating resistor (R_{INT}) is determined by the full-scale input voltage and the output current of the integrating amplifier. The integrating amplifier can supply 20 µA of current with negligible nonlinearity. The equation for determining the value of this resistor is:

$$R_{INT} = \frac{\text{Full Scale Voltage}}{I_{INT}}$$

Integrating amplifier current, I_{INT}, from 5 to 40 µA yields good results. However, the nominal and recommended current is 20 µA.

PRINCIPLES OF OPERATION

integrating capacitor

The product of the integrating resistor and capacitor should be selected to give the maximum voltage swing without causing the integrating amplifier output to saturate and get too close to the power supply voltages. When the amplifier output is within 0.3 V of either supply, saturation occurs. With ±5-V supplies and ANLG COMMON connected to ground, the designer should design for a ±3.5-V to ±4-V integrating amplifier swing. A nominal capacitor value is 0.47 μF. The equation for determining the value of the integrating capacitor (C_{INT}) is:

$$C_{INT} = \frac{10,000 \times \text{Clock Period} \times I_{INT}}{\text{Integrator Output Voltage Swing}}$$

Where:

I_{INT} is nominally 20 μA.

Capacitors with large tolerances and high dielectric absorption can induce conversion inaccuracies. A capacitor that is too small could cause the integrating amplifier to saturate. High dielectric absorption causes the effective capacitor value to be different during the signal integrate and deintegrate phases. Polypropylene capacitors have very low dielectric absorption. Polystyrene and polycarbonate capacitors have higher dielectric absorption, but also work well.

auto-zero and reference capacitor

Large capacitors tend to reduce noise in the system. Dielectric absorption is unimportant except during power up or overload recovery. Typical values are 1 μF.

reference voltage

For high-accuracy absolute measurements, a high quality reference should be used.

rollover resistor and diode

The ICL7135C and TLC7135C have a small rollover error; however, it can be corrected. The correction is to connect the cathode of any silicon diode to INT OUT and the anode to a resistor. The other end of the resistor is connected to ANLG COMMON or ground. For the recommended operating conditions, the resistor value is 100 kΩ. This value may be changed to correct any rollover error that has not been corrected. In many noncritical applications the resistor and diode are not needed.

maximum clock frequency

For most dual-slope A/D converters, the maximum conversion rate is limited by the frequency response of the comparator. In this circuit, the comparator follows the integrator ramp with a 3-μs delay. Therefore, with a 160-kHz clock frequency (6-μs period), half of the first reference integrate clock period is lost in delay. Hence, the meter reading changes from 0 to 1 with a 50-μV input, 1 to 2 with a 150-μV input, 2 to 3 with a 250-μV input, etc. This transition at midpoint is desirable; however, when the clock frequency is increased appreciably above 160 kHz, the instrument flashes 1 on noise peaks even when the input is shorted. The above transition points assume a 2-V input range is equivalent to 20,000 clock cycles.

When the input signal is always of one polarity, comparator delay need not be a limitation. Clock rates of 1 MHz are possible since nonlinearity and noise do not increase substantially with frequency. For a fixed clock frequency, the extra count or counts caused by comparator delay are a constant and can be subtracted out digitally.

PRINCIPLES OF OPERATION

maximum clock frequency (continued)

For signals with both polarities, the clock frequency can be extended above 160 kHz without error by using a low value resistor in series with the integrating capacitor. This resistor causes the integrator to jump slightly towards the zero-crossing level at the beginning of the deintegrate phase, and thus compensates for the comparator delay. This series resistor should be 10 Ω to 50 Ω. This approach allows clock frequencies up to 480 kHz.

minimum clock frequency

The minimum clock frequency limitations result from capacitor leakage from the auto-zero and reference capacitors. Measurement cycles as high as 10 μs are not influenced by leakage error.

rejection of 50-Hz or 60-Hz pickup

To maximize the rejection of 50-Hz or 60-Hz pickup, the clock frequency should be chosen so that an integral multiple of 50-Hz or 60-Hz periods occur during the signal integrate phase. To achieve rejection of these signals, some clock frequencies that can be used are:

50 Hz: 250, 166.66, 125, 100 kHz, etc.
60 Hz: 300, 200, 150, 120, 100, 40, 33.33 kHz, etc.

zero-crossing flip-flop

This flip-flop interrogates the comparator's zero-crossing status. The interrogation is performed after the previous clock cycle and the positive half of the ongoing clock cycle has occurred, so any comparator transients that result from the clock pulses do not affect the detection of a zero-crossing. This procedure delays the zero-crossing detection by one clock cycle. To eliminate the inaccuracy, which is caused by this delay, the counter is disabled for one clock cycle at the beginning of the deintegrate phase. Therefore, when the zero-crossing is detected one clock cycle later than the zero-crossing actually occurs, the correct number of counts is displayed.

noise

The peak-to-peak noise around zero is approximately 15 μV (peak-to-peak value not exceeded 95% of the time). Near full scale, this value increases to approximately 30 μV. Much of the noise originates in the auto-zero loop, and is proportional to the ratio of the input signal to the reference.

analog and digital grounds

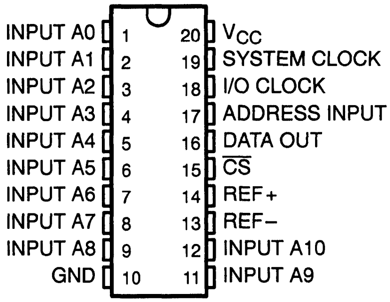
For high-accuracy applications, ground loops must be avoided. Return currents from digital circuits must not be sent to the analog ground line.

power supplies

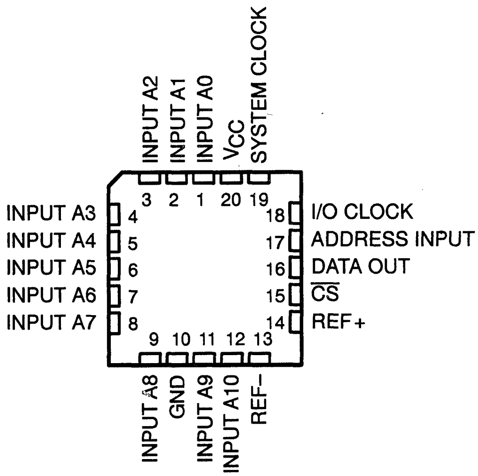
The ICL7135C and TLC7135C are designed to work with ±5-V power supplies. However, 5-V operation is possible when the input signal does not vary more than ±1.5 V from midsupply.

- **8-Bit Resolution A/D Converter**
- **Microprocessor Peripheral or Stand-Alone Operation**
- **On-Chip 12-Channel Analog Multiplexer**
- **Built-in Self-Test Mode**
- **Software-Controllable Sample and Hold**
- **Total Unadjusted Error . . . ±0.5 LSB Max**
- **TLC541 is Direct Replacement for Motorola MC145040 and National Semiconductor ADC0811. TLC540 is Capable of Higher Speed**
- **Pinout and Control Signals Compatible with TLC1540 Family of 10-Bit A/D Converters**
- **CMOS Technology**

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



PARAMETER	TLC540	TLC541
Channel Acquisition Sample Time	2 µs	3.6 µs
Conversion Time (Max)	9 µs	17 µs
Samples per Second (Max)	75 x 10^3	40 x 10^3
Power Dissipation (Max)	12.5 mW	12.5 mW

description

The TLC540 and TLC541 are CMOS A/D converters built around an 8-bit switched-capacitor successive-approximation A/D converters. They are designed for serial interface to a microprocessor or peripheral via a 3-state output with up to four control inputs, including independent SYSTEM CLOCK, I/O CLOCK, chip select ($\overline{CS}$), and ADDRESS INPUT. A 4-MHz system clock for the TLC540 and a 2.1-MHz system clock for the TLC541 with a design that includes simultaneous read/write operation allow high-speed data transfers and sample rates of up to 75,180 samples per second for the TLC540 and 40,000 samples per second for the TLC541. In addition to the high-speed converter and versatile control logic, there is an on-chip 12-channel analog multiplexer that can be used to sample any one of 11 inputs or an internal self-test voltage, and a sample-and-hold that can operate automatically or under microprocessor control. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

AVAILABLE OPTIONS

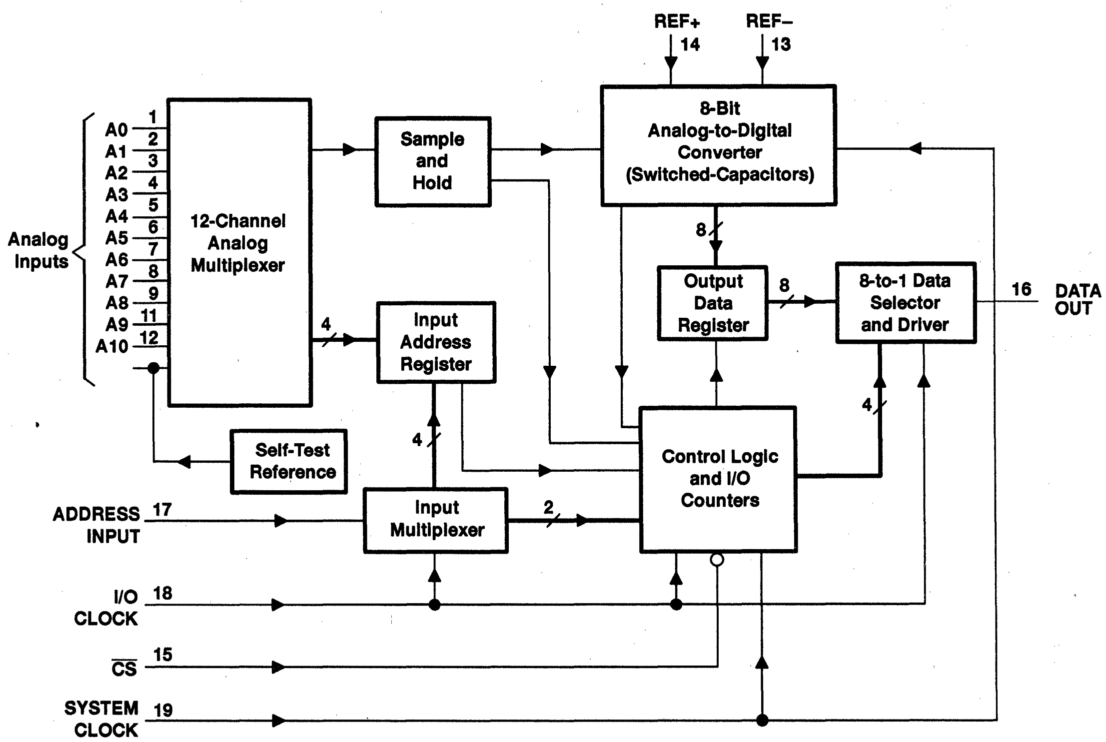
T_A	PACKAGE		
	SO PLASTIC DIP (DW)	PLASTIC DIP (N)	CHIP CARRIER (FN)
−40°C to 85°C	TLC540IDW TLC541IDW	TLC540IN TLC541IN	TLC540IFN TLC541IFN

description (continued)

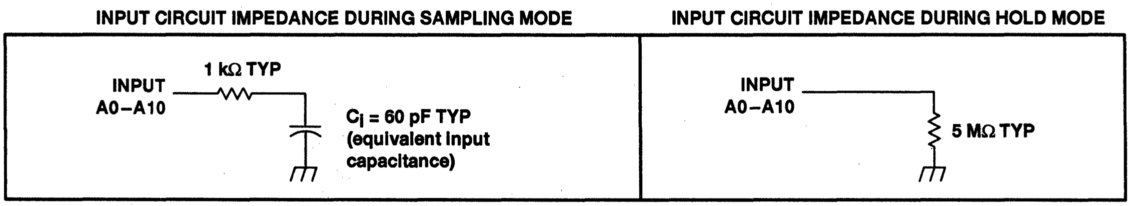
The converters incorporated in the TLC540 and TLC541 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A switched-capacitor design allows low-error (±0.5 LSB) conversion in 9 µs for the TLC540 and 17 µs for the TLC541 over the full operating temperature range.

The TLC540I and TLC541I are characterized for operation from −40°C to 85°C.

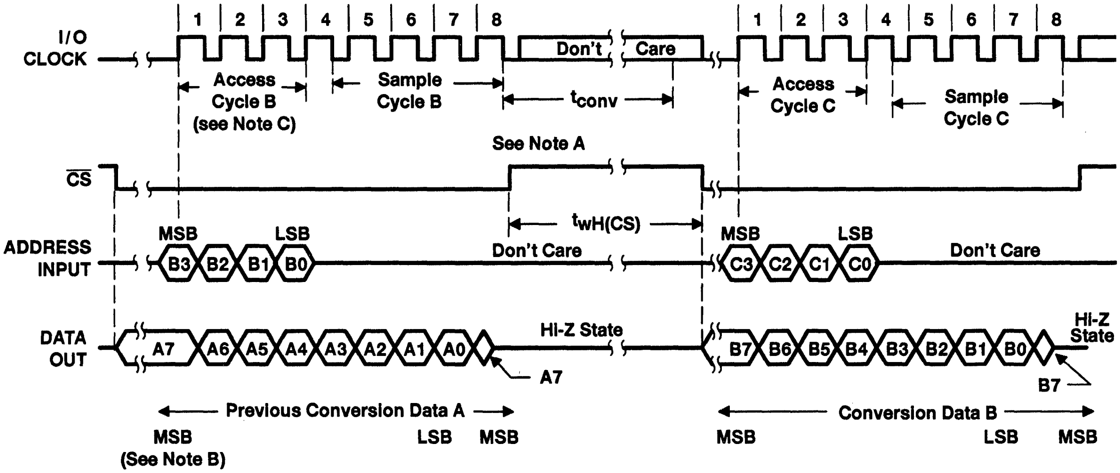
functional block diagram



typical equivalent inputs



operating sequence



NOTES: A. The conversion cycle, which requires 36 system clock periods, is initiated on the 8th falling edge of I/O CLOCK after $\overline{CS}$ goes low for the channel whose address exists in memory at that time. If $\overline{CS}$ is kept low during conversion, I/O CLOCK must remain low for at least 36 system clock cycles to allow conversion to be completed.

B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6–A0) will be clocked out on the first seven I/O CLOCK falling edges.

C. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for three system clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range, V_I (any input)	–0.3 V to V_{CC} +0.3 V
Output voltage range, V_O	–0.3 V to V_{CC} +0.3 V
Peak input current range (any input)	±10 mA
Peak total input current (all inputs)	±30 mA
Operating free-air temperature range, T_A: TLC540I, TLC541I	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to digital ground with REF– and GND wired together (unless otherwise noted).

recommended operating conditions

			TLC540			TLC541			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)			2.5	V_{CC}	$V_{CC}+0.1$	2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{ref-} (see Note 2)			−0.1	0	2.5	− 0.1	0	2.5	V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)			1	V_{CC}	$V_{CC}+0.2$	1	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)			0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH}			2			2			V
Low-level control input voltage, V_{IL}					0.8			0.8	V
Setup time, address bits at data input before I/O CLOCK↑, $t_{su(A)}$			200			400			ns
Hold time, address bits after I/O CLOCK↑, $t_{h(A)}$			0			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3)			3			3			System clock cycles
$\overline{CS}$ high during conversion, $t_{wH(CS)}$			36			36			System clock cycles
I/O CLOCK frequency, $f_{clock(I/O)}$			0		2.048	0		1.1	MHz
Pulse duration, SYSTEM CLOCK frequency, $f_{clock(SYS)}$			$f_{clock(I/O)}$		4	$f_{clock(I/O)}$		2.1	MHz
Pulse duration, SYSTEM CLOCK high, $t_{wH(SYS)}$			110			210			MHz
Pulse duration, SYSTEM CLOCK low, $t_{wL(SYS)}$			100			190			MHz
Pulse duration, I/O clock high, $t_{wH(I/O)}$			200			404			ns
Pulse duration, I/O clock low, $t_{wL(I/O)}$			200			404			ns
Clock transition time (see Note 4)	System	$f_{clock(SYS)} \leq 1048$ kHz			30			30	ns
		$f_{clock(SYS)} > 1048$ kHz			20			20	
	I/O	$f_{clock(I/O)} \leq 525$ kHz			100			100	
		$f_{clock(I/O)} > 525$ kHz			40			40	
Operating free-air temperature, T_A		TLC540I, TLC541I	−40		85	−40		85	°C

NOTES: 2. Analog input voltages greater than that applied to REF + convert as all "1"s (11111111), while input voltages less than that applied to REF− convert as all "0"s (00000000). For proper operation, REF+ voltage must be at least 1 V higher than REF− voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.

3. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for three SYSTEM CLOCK cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum chip select setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating temperature range, $V_{CC} = V_{ref+} = 4.75$ V to 5.5 V, $f_{clock(I/O)} = 2.048$ MHz for TLC540 or $f_{clock(I/O)} = 1.1$ MHz for TLC541 (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage, DATA OUT		$V_{CC} = 4.75$ V, $I_{OH} = 360\ \mu A$	2.4			V
V_{OL}	Low-level output voltage		$V_{CC} = 4.75$ V, $I_{OL} = 1.6$ mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		$V_O = V_{CC}$, $\overline{CS}$ at V_{CC}			10	μA
			$V_O = 0$, $\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		$V_I = V_{CC}$		0.005	2.5	μA
I_{IL}	Low-level input current		$V_I = 0$		−0.005	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V		1.2	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V		0.4	1	μA
			Selected channel at 0 V, Unselected channel at V_{CC}		−0.4	−1	
$I_{CC} + I_{ref}$	Supply and reference current		$V_{ref+} = V_{CC}$, $\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs			7	55	pF
		Control inputs			5	15	

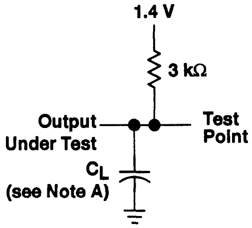
† All typical values are at $T_A = 25°C$.

operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+} - 4.75$ V to 5.5 V, $f_{clock(I/O)}$ = 2.048 MHz for TLC540 or 1.1 MHz for TLC541, $f_{clock(SYS)}$ = 4 MHz for TLC540 or 2.1 MHz for TLC541

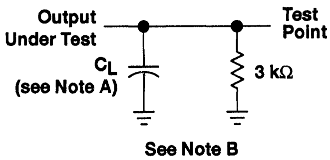
	PARAMETER	TEST CONDITIONS	TLC540		TLC541		UNIT
			MIN	MAX	MIN	MAX	
E_L	Linearity error	See Note 5		±0.5		±0.5	LSB
E_{ZS}	Zero–scale error	See Notes 2 and 6		±0.5		±0.5	LSB
E_{FS}	Full-scale error	See Notes 2 and 6		±0.5		±0.5	LSB
	Total unadjusted error	See Note 7		±0.5		±0.5	LSB
	Self-test output code	Input A11 address = 1011, (see Note 8)	01111101 (125)	10000011 (131)	01111101 (125)	10000011 (131)	
t_{conv}	Conversion time	See Operating Sequence		9		17	µs
	Total access and conversion time	See Operating Sequence		13.3		25	µs
t_a	Channel acquisition time (sample cycle)	See Operating Sequence		4		4	I/O clock cylces
t_v	Time output data remains valid after I/O CLOCK↓		10		10		ns
t_d	Delay time, I/O CLOCK↓ to data output valid	See Parameter Measurement Information		300		400	ns
t_{en}	Output enable time			150		150	ns
t_{dis}	Output disable time			150		150	ns
$t_{r(bus)}$	Data bus rise time			300		300	ns
$t_{f(bus)}$	Data bus fall time			300		300	ns

NOTES: 2. Analog input voltages greater than that applied to REF+ convert to all "1"s (11111111) while input voltages less than that applied to REF– convert to all "0"s (00000000). For proper operation, REF+ voltage must be at least 1 V higher than REF– voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.
5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero-scale error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
7. Total unadjusted error is the sum of linearity, zero-scale, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic.

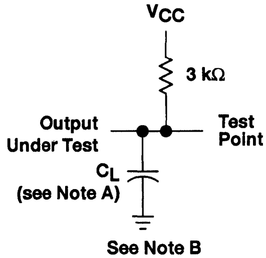
PARAMETER MEASUREMENT INFORMATION



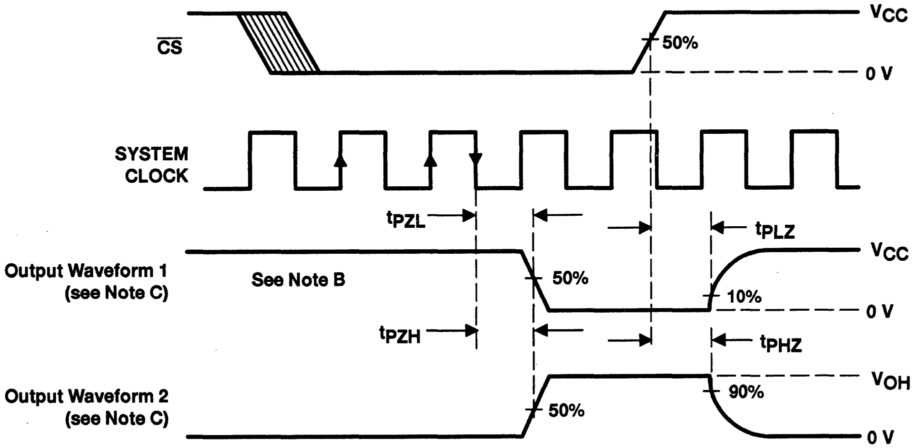
LOAD CIRCUIT FOR
t_d, t_r, AND t_f



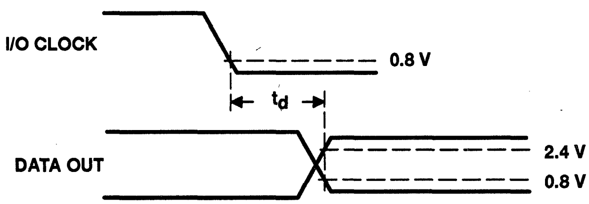
LOAD CIRCUIT FOR
t_{PZH} AND t_{PHZ}



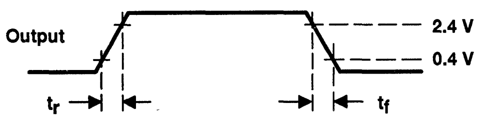
LOAD CIRCUIT FOR
t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS FOR DELAY TIME



VOLTAGE WAVEFORMS FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF for TLC540 and 100 pF for TLC541.
B. t_{en} = t_{PZH} or t_{PZL}, t_{dis} = t_{PHZ} or t_{PLZ}.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

APPLICATIONS INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 1, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S\left(1 - e^{-t_c/R_tC_i}\right) \tag{1}$$

where

$R_t = R_s + r_i$

The final voltage to 1/2 LSB is given by

$$V_C\,(1/2\ \text{LSB}) = V_S - (V_S/512) \tag{2}$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - \left(V_S/512\right) = V_S\left(1 - e^{-t_c/R_tC_i}\right) \tag{3}$$

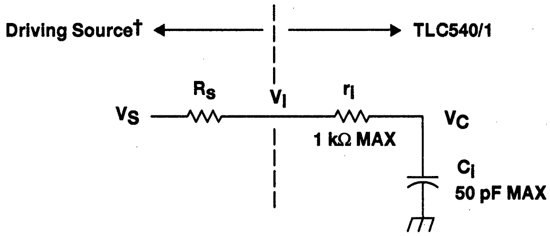
and

$$t_c\,(1/2\ \text{LSB}) = R_t \times C_i \times \ln(512) \tag{4}$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c\,(1/2\ \text{LSB}) = (R_s + 1\ \text{k}\Omega) \times 60\ \text{pF} \times \ln(512) \tag{5}$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at INPUT A0–A10
V_S = External Driving Source Voltage
R_s = Source Resistance
r_I = Input Resistance
C_I = Equivalent Input Capacitance

† Driving source requirements:
- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_s must be real at the input frequency.

Figure 1. Equivalent Input Circuit Including the Driving Source

PRINCIPLES OF OPERATION

The TLC540 and TLC541 are each complete data acquisition systems on a single chip. They include such functions as analog multiplexer, sample and hold, 8-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs [two clocks, chip select ($\overline{CS}$), and address]. These control inputs and a TTL-compatible 3-state output are intended for serial communications with a microprocessor or microcomputer. With judicious interface timing, with TLC540 a conversion can be completed in 9 μs, while complete input-conversion-output cycles can be repeated every 13 μs. With TLC541 a conversion can be completed in 17 μs, while complete input-conversion-output cycles are repeated every 25 μs. Furthermore, this fast conversion can be executed on any of 11 inputs or its built-in self-test and in any order desired by the controlling processor.

The system and I/O clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to SYSTEM CLOCK, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using I/O CLOCK. SYSTEM CLOCK will drive the conversion crunching circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, DATA OUT is in a 3-state condition and ADDRESS INPUT and I/O CLOCK are disabled. This feature allows each of these terminals, with the exception of $\overline{CS}$, to share a control logic point with their counterpart terminals on additional A/D devices when additional TLC540/541 devices are used. In this way, the above feature serves to minimize the required control logic terminals when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for two rising edges and then a falling edge of SYSTEM CLOCK after a low $\overline{CS}$ transition, before the low transition is recognized. This technique is used to protect the device against noise when the device is used in a noisy environment. The MSB of the previous conversion result automatically appears on DATA OUT.
2. A new positive-logic multiplexer address is shifted in on the first four rising edges of I/O CLOCK. The MSB of the address is shifted in first. The negative edges of these four I/O clock pulses shift out the second, third, fourth, and fifth most significant bits of the previous conversion result. The on-chip sample and hold begins sampling the newly addressed analog input after the fourth falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Three clock cycles are then applied to I/O CLOCK and the sixth, seventh, and eighth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final eighth clock cycle is applied to I/O CLOCK. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 36 system clock cycles. After this final I/O clock cycle, $\overline{CS}$ must go high or the I/O CLOCK must remain low for at least 36 system clock cycles to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on I/O CLOCK. If glitches occur on I/O CLOCK, the I/O sequence between the microprocessor/controller and the device loses synchronization. Also, if $\overline{CS}$ is taken high, it must remain high until the end of the conversion. Otherwise, a valid falling edge of $\overline{CS}$ causes a reset condition, which aborts the conversion in progress.

A new conversion can be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 system clock cycles occur. Such action yields the conversion result of the previous conversion and not the ongoing conversion.

PRINCIPLES OF OPERATION

It is possible to connect SYSTEM CLOCK and I/O clock together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

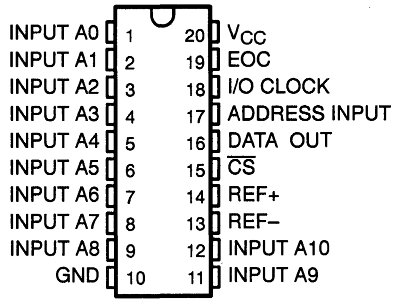
1. The first two clocks are required for this device to recognize $\overline{\text{CS}}$ is at a valid low level when the common clock signal is used as an I/O CLOCK. When $\overline{\text{CS}}$ is recognized by the device to be at a high level, the common clock signal is used for the conversion clock also.
2. A low $\overline{\text{CS}}$ must be recognized before the I/O CLOCK can shift in an analog channel address. The device recognizes a $\overline{\text{CS}}$ transition when the SYSTEM CLOCK terminal receives two positive edges and then a negative edge. For this reason, after a $\overline{\text{CS}}$ negative edge, the first two clock cycles do not shift in the address. Also, upon shifting in the address, $\overline{\text{CS}}$ must be raised after the eighth valid (10 total) I/O CLOCK. Otherwise, additional common clock cycles are recognized as I/O CLOCKS and will shift in an erroneous address.

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device accommodates these applications. Although the on-chip sample and hold begins sampling upon the negative edge of the fourth valid I/O clock cycle, the hold function is not initiated until the negative edge of the eighth valid I/O clock cycle. Thus, the control circuitry can leave the I/O clock signal in its high state during the eighth valid I/O clock cycle until the moment at which the analog signal must be converted. The TLC540/TLC541 continues sampling the analog input until the eighth falling edge of the I/O clock. The control circuitry or software then immediately lowers the I/O clock signal and holds the analog signal at the desired point in time and start conversion.

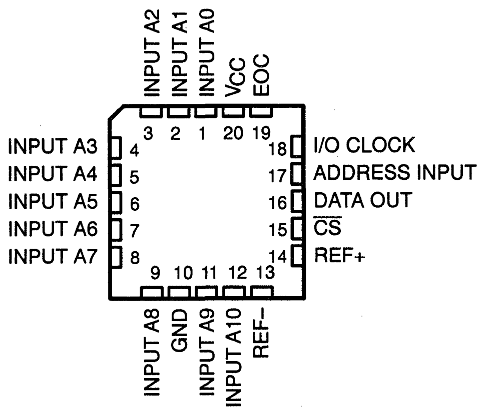
Detailed information on interfacing to most popular microprocessors is readily available from the factory.

- **8-Bit Resolution A/D Converter**
- **Microprocessor Peripheral or Stand-Alone Operation**
- **On-Chip 12-Channel Analog Multiplexer**
- **Built-in Self-Test Mode**
- **Software-Controllable Sample and Hold**
- **Total Unadjusted Error . . . ±0.5 LSB Max**
- **Direct Replacement for Motorola MC145041**
- **On-Board System Clock**
- **End-of-Conversion (EOC) Output**
- **Pinout and Control Signals Compatible With the TLC1542/3 10-Bit A/D Converters**
- **CMOS Technology**

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



PARAMETER	VALUE
Channel Acquisition/Sample Time	16 µs
Conversion Time (Max)	20 µs
Samples per Second (Max)	25×10^3
Power Dissipation (Max)	10 mW

description

The TLC542 is a CMOS converter built around an 8-bit switched-capacitor successive-approximation analog-to-digital converter. The device is designed for serial interface to a microprocessor or peripheral via a 3-state output with three inputs [including I/O CLOCK, $\overline{CS}$ (chip select), and ADDRESS INPUT]. The TLC542 allows high-speed data transfers and sample rates of up to 40,000 samples per second. In addition to the high-speed converter and versatile control logic, an on-chip 12-channel analog multiplexer can sample any one of 11 inputs or an internal "self-test" voltage, and the sample and hold is started under microprocessor control. At the end of conversion, the end-of-conversion (EOC) output pin goes high to indicate that conversion is complete. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

AVAILABLE OPTIONS

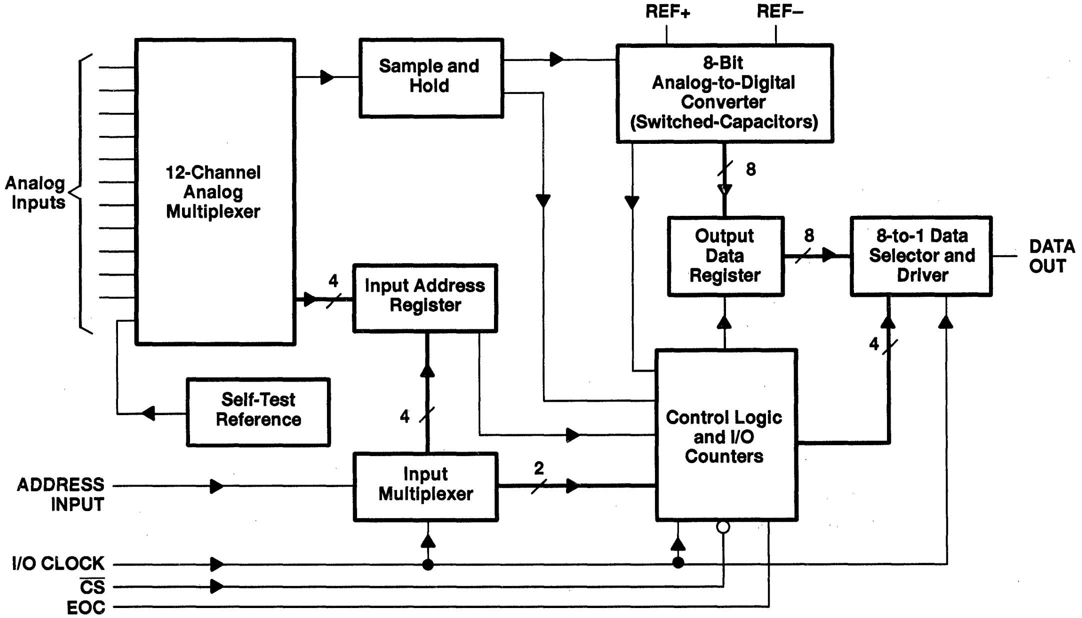
T_A	PACKAGE		
	CHIP CARRIER (FN)	PLASTIC DIP (N)	SMALL OUTLINE (DW)
0°C to 70°C	TLC542CFN	TLC542CN	TLC542CDW
–40°C to 85°C	TLC542IFN	TLC542IN	TLC542IDW

description (continued)

The converter incorporated in the TLC542 features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noises. A switched-capacitor design allows low-error (±0.5 LSB) conversion in 20 µs over the full operating temperature range.

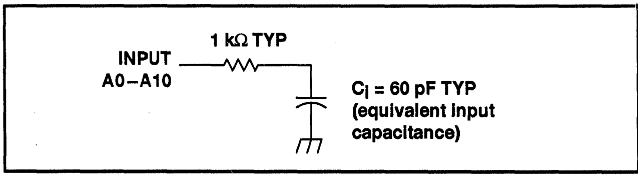
The TLC542C is characterized for operation from 0°C to 70°C and the TLC542I is characterized for operation from −40°C to 85°C.

functional block diagram

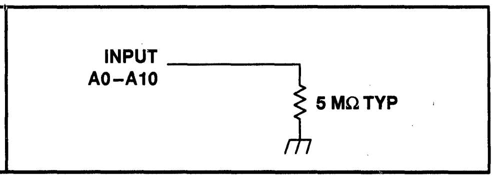


typical equivalent inputs

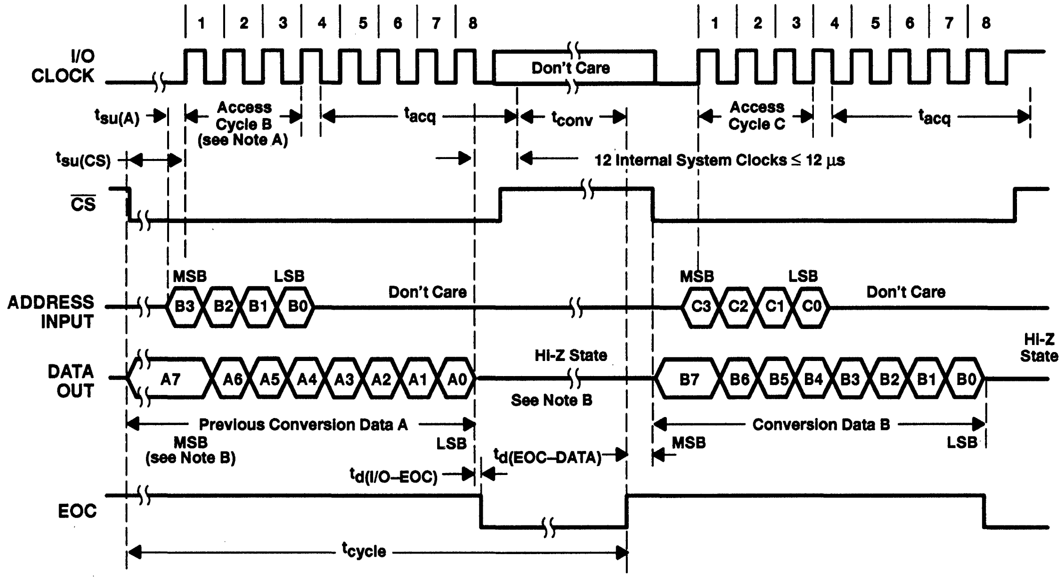
INPUT CIRCUIT IMPEDANCE DURING SAMPLING MODE



INPUT CIRCUIT IMPEDANCE DURING HOLD MODE



operating sequence



NOTES: A. To minimize errors caused by noise at the chip select input, the internal circuitry waits for two rising edges and one falling edge of the internal system clock after $\overline{CS}$↓ before responding to control input signals. The $\overline{CS}$ setup time is given by the $t_{su(CS)}$ specifications. Therefore, no attempt should be made to clock-in an address until the minimum chip select setup time has elapsed.

B. The output is 3-stated on $\overline{CS}$ going high or on the negative edge of the eighth I/O clock.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)		6.5 V
Input voltage range (any input)		−0.3 V to V_{CC} + 0.3 V
Output voltage range		−0.3 V to V_{CC} + 0.3 V
Peak input current range (any input)		±20 mA
Peak total input current (all inputs)		±30 mA
Operating free-air temperature range:	TLC542C	0°C to 70°C
	TLC542I	−40°C to 85°C
Storage temperature range		−65°C to 150°C
Case temperature for 10 seconds: FN package		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package		260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to digital ground with REF– and GND wired together (unless otherwise noted).

recommended operating conditions, V_{CC} = 4.75 to 5.5 V

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)		V_{ref-}	V_{CC}	V_{CC} + 0.1	V
Negative reference voltage, V_{ref-} (see Note 2)		−0.1	0	V_{ref+}	V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)		1	V_{CC}	V_{CC} + 0.2	V
Analog input voltage (see Note 3)		0		V_{CC}	V
High-level control input voltage, V_{IH}		2			V
Low-level control input voltage, V_{IL}				0.8	V
Setup time, address bits at data input before I/O CLOCK↑, $t_{su(A)}$		400			ns
Hold time, address bits after I/O CLOCK↑, $t_{h(A)}$		0			ns
Hold time, $\overline{CS}$ low after 8th I/O CLOCK↑, $t_{h(CS)}$		0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 4)		3.8			µs
Input/output clock frequency, $f_{clock(I/O)}$		0	1.1		MHz
Input/output clock high, $t_{wH(I/O)}$		404			ns
Input/output clock low, $t_{wL(I/O)}$		404			ns
I/O CLOCK transition time, t_t (see Note 3)	$f_{clock(I/O)} \le 525$ kHz			100	ns
	$f_{clock(I/O)} > 525$ kHz			40	
Operating free-air temperature, T_A	TLC542C	0		70	°C
	TLC542I	−40		85	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (11111111), while input voltages less than that applied to REF− convert as all zeros (00000000). For proper operation, REF+ must be at least 1 V higher than REF−. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.

3. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

4. To minimize errors caused by noise at the chip select input, the internal circuitry waits for two rising edges and one falling edge of the internal system clock after $\overline{CS}$ ↓ before responding to control input signals. The $\overline{CS}$ setup time is given by the $t_{su(CS)}$ specifications. Therefore, no attempt should be made to clock-in address data until the minimum chip select setup time has elapsed.

electrical characteristics over recommended operating temperature range, $V_{CC} = V_{ref+}$ = 4.75 V to 5.5 V, $f_{clock(I/O)}$ = 1.1 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (DATA OUT)		V_{CC} = 4.75 V,	I_{OH} = −360 µA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 1.6 mA			0.4	V
	Off-state (high-impedance state) output current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}			10	µA
			V_O = 0,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		$V_I = V_{CC}$			0.005	2	µA
I_{IL}	Low-level input current		V_I = 0			−0.005	−2.5	µA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.2	2	mA
	Selected channel leakage current		Selected at V_{CC}, Unselected channel at 0 V	0°C to 70 °C			0.4	µA
				– 40°C to 85°C			−0.4	
I_{ref}	Maximum static analog reference current into REF+		$V_{ref+} = V_{CC}$,	V_{ref-} = GND			10	µA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

† All typical values are at T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 4.75 to 5.5 V, $f_{clock(I/O)}$ = 1 MHZ

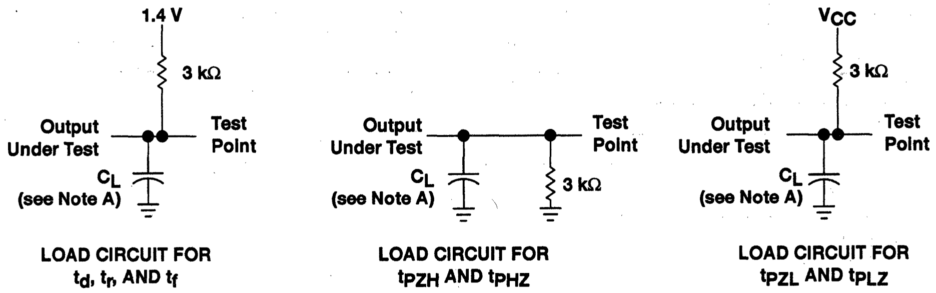
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error (see Note 5)				±0.5	LSB
E_{ZS}	Zero-scale error (see Note 6)	See Note 2			±0.5	LSB
E_{FS}	Full-scale error (see Note 6)	See Note 2			±0.5	LSB
	Total unadjusted error (see Note 7)				±0.5	LSB
	Self-test output code	Input A11 address = 1011, See Note 8	01111101 (126)	128	10000011 (130)	
t_{conv}	Conversion time	See operating sequence			20	µs
t_{cycle}	Total access and conversion cycle time	See operating sequence			40	µs
t_{acq}	Channel acquisition time (sample cycle)	See operating sequence			16	µs
t_v	Time ouput data remains valid after I/O CLK↓	See Figure 5	10			ns
$t_{d(IO-DATA)}$	Delay time, I/O CLK↓ to data output valid	See Figure 5			400	ns
$t_{d(IO-EOC)}$	Delay time, 8th I/O CLK↓ to EOC↓	See Figure 6			500	ns
$t_{d(EOC-DATA)}$	Delay time, EOC↑ to data out (MSB)	See Figure 7			400	ns
t_{PZH}, t_{PZL}	Delay time, CS↓ to data out (MSB)	See Figure 2			3.4	µs
t_{PHZ}, t_{PLZ}	Delay time, CS↑ to data out (MSB)	See Figure 2			150	ns
$t_{r(EOC)}$	Rise time	See Figure 7			100	ns
$t_{f(EOC)}$	Fall time	See Figure 6			100	ns
$t_{r(bus)}$	Data bus rise time	See Figure 5			300	ns
$t_{f(bus)}$	Data bus fall time	See Figure 5			300	ns

† All typical values are at T_A = 25°C

NOTES: 2. Analog input voltages greater than that applied to REF+ convert to all ones (11111111), while input voltages less than that applied to REF− convert to all zeros (00000000). For proper operation, REF+ must be at least 1 V higher than REF−. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.

5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero-scale Error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
7. Total unadjusted error is the sum of linearity, zero-scale, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic. The A11 analog input signal is internally generated and is used for test purposes.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L = 50 pF

Figure 1. Load Circuits

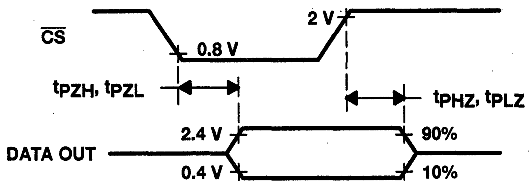


Figure 2. $\overline{CS}$ to Data Output Timing

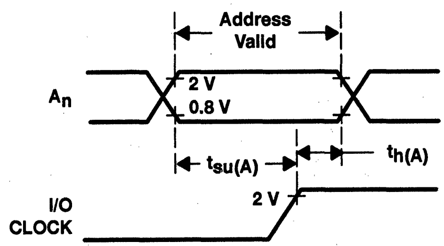


Figure 3. Address Timing

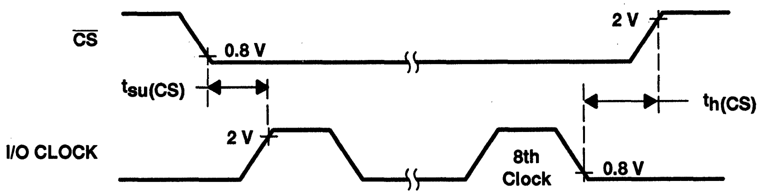


Figure 4. Figure 4. $\overline{CS}$ to I/O CLOCK Timing

PARAMETER MEASUREMENT INFORMATION

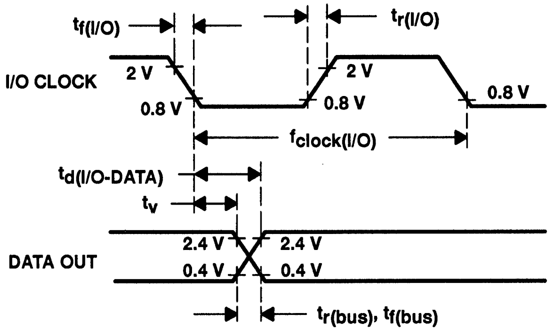


Figure 5. Data Output Timing

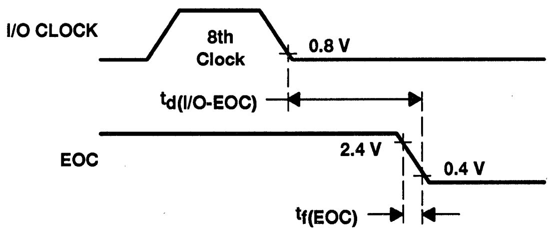


Figure 6. EOC Timing

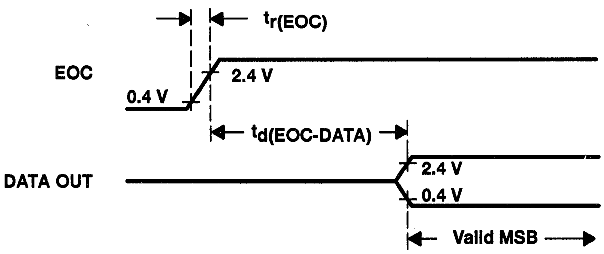


Figure 7. Data Output to EOC Timing

APPLICATIONS INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 8, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c/R_tC_i}\right) \tag{1}$$

where

$$R_t = R_s + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C\ (1/2\ \text{LSB}) = V_S - (V_S/512) \tag{2}$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S/512) = V_S \left(1 - e^{-t_c/R_tC_i}\right) \tag{3}$$

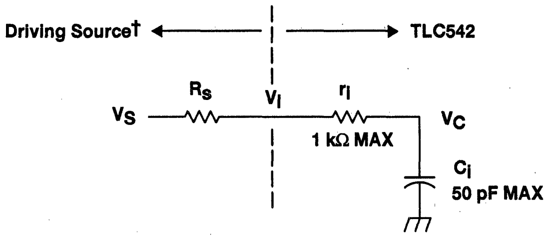
and

$$t_c\ (1/2\ \text{LSB}) = R_t \times C_i \times \ln(512) \tag{4}$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c\ (1/2\ \text{LSB}) = (R_s + 1\ \text{k}\Omega) \times 60\ \text{pF} \times \ln(512) \tag{5}$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at INPUT A0–A10
V_S = External Driving Source Voltage
R_s = Source Resistance
r_i = Input Resistance
C_i = Input Capacitance

† Driving source requirements:
- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_s must be real at the input frequency.

Figure 8. Equivalent Input Circuit Including the Driving Source

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PRINCIPLES OF OPERATION

The TLC542 is a complete data acquisition system on a single chip. The device includes such functions as analog multiplexer, sample and hold, 8-bit A/D converter, data and control registers, and control logic. Three control inputs (I/O CLOCK, $\overline{CS}$ (chip select), and ADDRESS INPUT) are included for flexibility and access speed. These control inputs and a TTL-compatible 3-state output are intended for serial communications with a microprocessor or microcomputer. With judicious interface timing, the TLC542 can complete a conversion in 20 µs, while complete input-conversion-output cycles can be repeated every 40 µs. Futhermore, this fast conversion can be executed on any of 11 inputs or its built-in self-test and in any order desired by the controlling processor.

When $\overline{CS}$ is high, the DATA OUT terminal is in a 3-state condition, and the ADDRESS INPUT and I/O CLOCK terminals are disabled. When additional TLC542 devices are used, this feature allows each of these termminals, with the exception of the $\overline{CS}$ terminal, to share a control logic point with their counterpart terminals on additional A/D devices. Thus, this feature minimizes the control logic terminals required when using multiple A/D devices.

The control sequence is designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is as follows:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the internal system clock before recognizing the low $\overline{CS}$ transition. The MSB of the result of the previous conversion automatically appears on the DATA OUT terminal.
2. On the first four rising edges of the I/O CLOCK, a new positive-logic multiplexer address is shifted in, with the MSB of this address shifted first. The negative edges of these four I/O CLOCK pulses shift out the second, third, fourth, and fifth most significant bits of the result of the previous conversion. The on-chip sample and hold begins sampling the newly addressed analog input after the fourth falling edge of the I/O CLOCK. The sampling operation basically involves charging the internal capacitors to the level of the analog input voltage.
3. Three clock cycles are applied to the I/O CLOCK terminal and the sixth, seventh, and eighth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final eighth clock cycle is applied to the I/O CLOCK terminal. The falling edge of this clock cycle initiates a 12-system clock (≈ 12 µs) additional sampling period while the output is in the high-impedance state. Conversion is then performed during the next 20 µs. After this final I/O CLOCK cycle, $\overline{CS}$ must go high or the I/O CLOCK must remain low for at least 20 µs to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. If $\overline{CS}$ is taken high, it must remain high until the end of conversion. Otherwise, a valid falling edge of $\overline{CS}$ causes a reset condition, which aborts the conversion process.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 20-µs conversion time has elapsed. Such action yields the conversion result of the previous conversion and not the ongoing conversion.

The end-of-conversion (EOC) output goes low on the negative edge of the eighth I/O CLOCK. The subsequent low-to-high transition of EOC indicates the A/D conversion is complete and the conversion is ready for transfer.

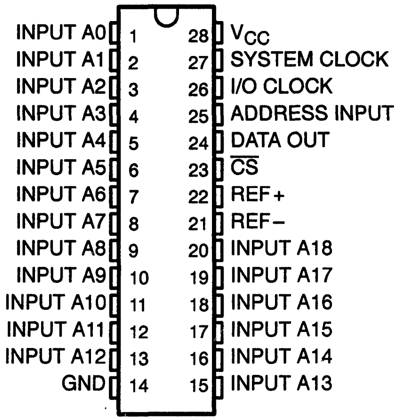
TLC545C, TLC545I, TLC546C, TLC546I
8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 19 INPUTS

SLAS066A – DECEMBER 1985 – REVISED MARCH 1995

- **8-Bit Resolution A/D Converter**
- **Microprocessor Peripheral or Stand-Alone Operation**
- **On-Chip 20-Channel Analog Multiplexer**
- **Built-in Self-Test Mode**
- **Software-Controllable Sample and Hold**
- **Total Unadjusted Error . . . ±0.5 LSB Max**
- **Timing and Control Signals Compatible With 8-Bit TLC540 and 10-Bit TLC1540 A/D Converter Families**
- **CMOS Technology**

PARAMETER	TL545	TL546
Channel Acquisition Time	1.5 μs	2.7 μs
Conversion Time (Max)	9 μs	17 μs
Sampling Rate (Max)	76×10^3	40×10^3
Power Dissipation (Max)	15 mW	15 mW

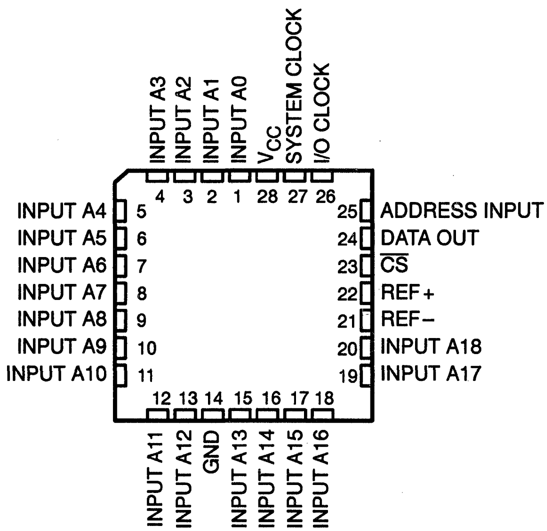
N or DW PACKAGE (TOP VIEW)



description

The TLC545 and TLC546 are CMOS analog-to-digital converters built around an 8-bit switched capacitor successive-approximation analog-to-digital converter. They are designed for serial interface to a microprocessor or peripheral via a 3-state output with up to four control inputs including independent SYSTEM CLOCK, I/O CLOCK, chip select ($\overline{CS}$), and ADDRESS INPUT. A 4-MHz system clock for the TLC545 and a 2.1-MHz system clock for the TLC546 with a design that includes simultaneous read/write operation allowing high-speed data transfers and sample rates of up to 76,923 samples per second for the TLC545, and 40,000 samples per second for the TLC546.

FN PACKAGE (TOP VIEW)



AVAILABLE OPTIONS

T_A	PACKAGE		
	CHIP CARRIER (FN)	PLASTIC DIP (N)	SMALL OUTLINE (DW)
0°C to 70°C	TLC545CFN TLC546CFN	TLC545CN TLC546CN	TLC545CDW TLC546CDW
−40°C to 85°C	TLC545IFN TLC546IFN	TLC545IN TLC546IN	TLC545IDW TLC546IDW

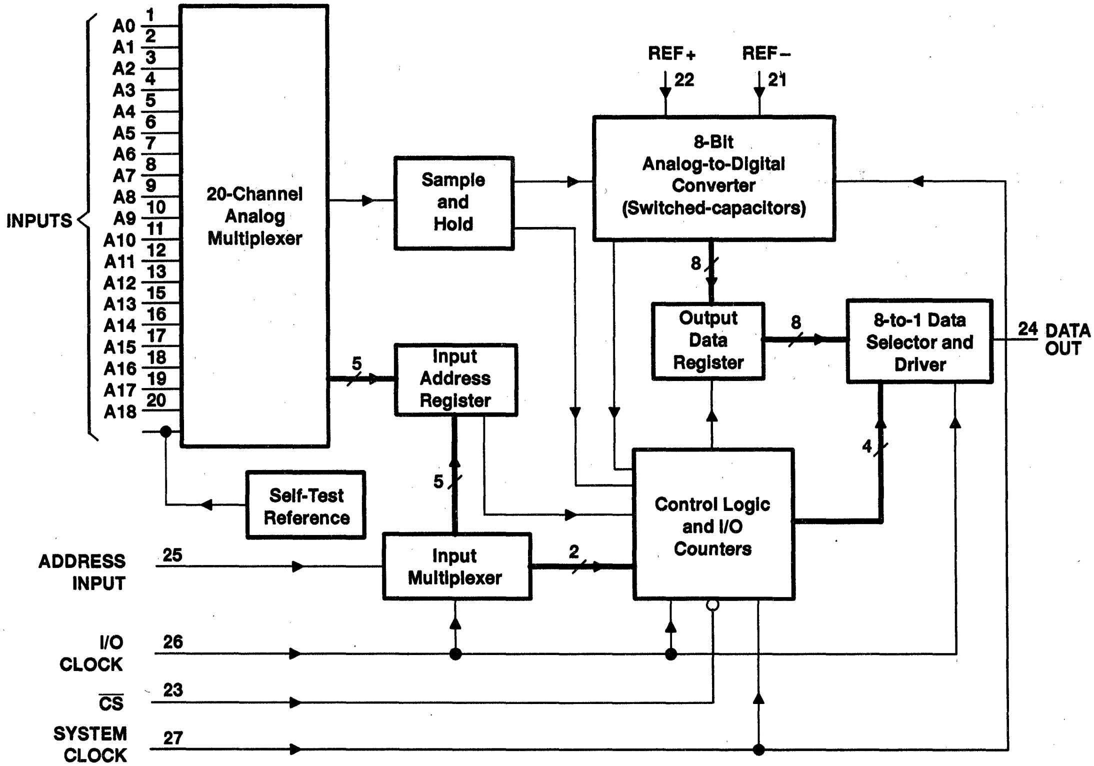
description (continued)

In addition to the high-speed converter and versatile control logic, there is an on-chip 20-channel analog multiplexer that can be used to sample any one of 19 inputs or an internal self-test voltage, and a sample-and-hold that can operate automatically or under microprocessor control.

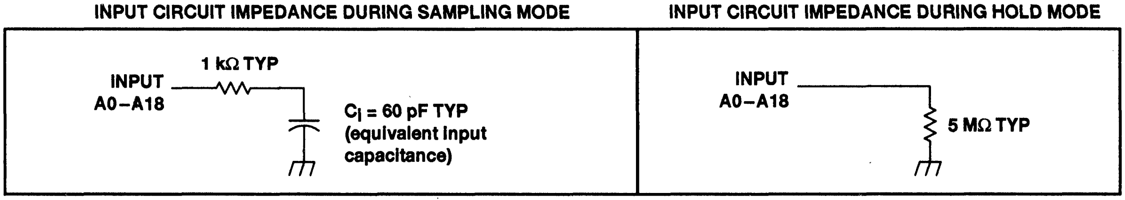
The converters incorporated in the TLC545 and TLC546 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A totally switched capacitor design allows low-error (±0.5 LSB) conversion in 9 μs for the TLC545, and 17 μs for the TLC546, over the full operating temperature range. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The TLC545C and the TLC546C are characterized for operation from 0°C to 70°C. The TLC545I and the TLC546I are characterized for operation from −40°C to 85°C.

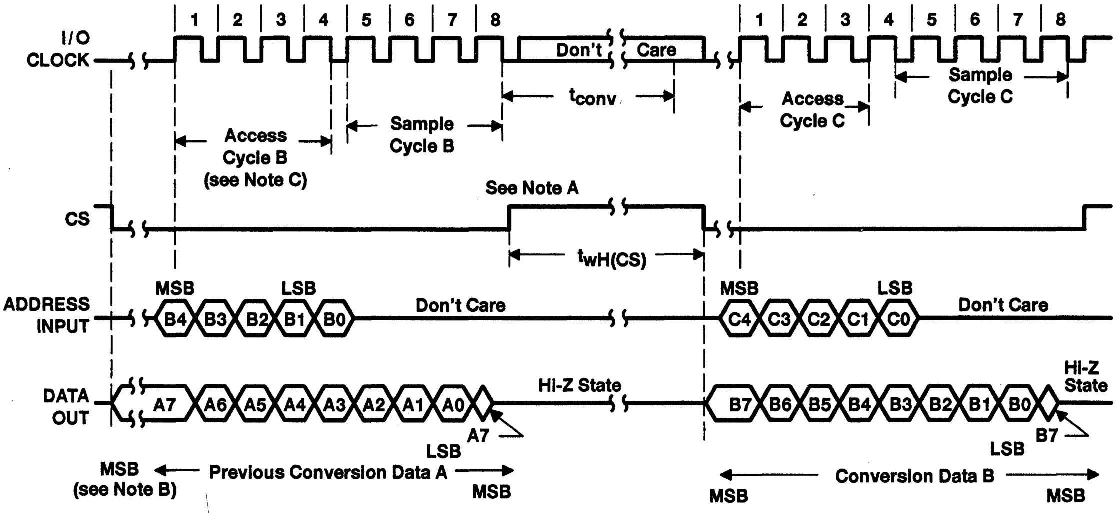
functional block diagram



typical equivalent inputs



operating sequence



NOTES: A. The conversion cycle, which requires 36 system clock periods, is initiated with the eighth I/O CLOCK↓ after $\overline{CS}$↓ for the channel whose address exists in memory at that time.

B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6–A0) will be clocked out on the first seven I/O CLOCK falling edges.

C. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for three system clock cycles (or less) after a chip select transition before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range, V_I (any input)	−0.3 V to V_{CC} +0.3 V
Output voltage range, V_O	−0.3 V to V_{CC} +0.3 V
Peak input current range (any input)	±10 mA
Peak total input current (all inputs)	±30 mA
Operating free-air temperature range, T_A: TLC545C, TLC546C	0°C to 70°C
TLC545I, TLC546I	−40°C to 85°C
Storage temperature range, T_{stg}	−65°C to 150°C
Case temperature for 10 seconds, T_C: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N or DW package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

			TLC545			TLC546			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)			0	V_{CC}	V_{CC} +0.1	0	V_{CC}	V_{CC} +0.1	V
Negative reference voltage, V_{ref-} (see Note 3)			−0.1	0	V_{CC}	−0.1	0	V_{CC}	V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 3)			0	V_{CC}	V_{CC} +0.2	0	V_{CC}	V_{CC} +0.2	V
Analog input voltage (see Note 3)			0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH}			2			2			V
Low-level control input voltage, V_{IL}					0.8			0.8	V
Setup time, address bits at data input before I/O CLOCK↑, $t_{su(A)}$			200			400			ns
Address hold time, t_h			0			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 2)			3			3			System clock cycles
I/O CLOCK frequency, $f_{clock(I/O)}$			0		2.048	0		1.1	MHz
SYSTEM CLOCK frequency, $f_{clock(SYS)}$			$f_{clock(I/O)}$		4	$f_{clock(I/O)}$		2.1	MHz
Pulse duration, $\overline{CS}$ high during conversion, $t_{wH(CS)}$			36			36			System clock cycles
Pulse duration, SYSTEM CLOCK high, $t_{wH(SYS)}$			110			210			ns
Pulse duration, SYSTEM CLOCK low, $t_{wL(SYS)}$			100			190			ns
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$			200			404			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$			200			404			ns
Clock transition time (see Note 4)	System	$f_{clock(SYS)} \le 1048$ kHz			30			30	ns
		$f_{clock(SYS)} > 1048$ kHz			20			20	
	I/O	$f_{clock(I/O)} \le 525$ kHz			100			100	ns
		$f_{clock(I/O)} > 525$ kHz			40			40	
Operating free-air temperature, T_A		TLC545C, TLC546C	0		70	0		70	°C
		TLC545I, TLC546I	−40		85	−40		85	

NOTES: 2. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for three system clock cycles (or less) after a chip select falling edge or rising edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip select setup time has elapsed.

3. Analog input voltages greater than that applied to REF+ convert as all "1"s (11111111), while input voltages less than that applied to REF– convert as all "0"s (00000000). As the differential reference voltage decreases below 4.75 V, the total unadjusted error tends to increase.

4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating temperature range, $V_{CC} = V_{ref+}$ = 4.75 V to 5.5 V, $f_{clock(I/O)}$ = 2.048 MHz for TLC545 or $f_{clock(I/O)}$ = 1.1 MHz for TLC546 (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (DATA OUT)		V_{CC} = 4.75 V,	I_{OH} = −360 µA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 3.2 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) ouput current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}			10	µA
			V_O = 0,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		$V_I = V_{CC}$			0.005	2.5	µA
I_{IL}	Low-level input current		V_I = 0			−0.005	−2.5	µA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.2	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V			0.4	1	µA
			Selected channel at 0 V, Unselected channel at V_{CC}			−0.4	−1	
$I_{CC} + I_{ref}$	Supply and reference current		$V_{ref+} = V_{CC}$,	$\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

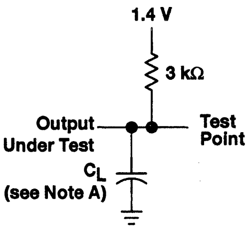
† All typical values are at T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 4.75 V to 5.5 V, $f_{clock(I/O)}$ = 2.048 MHz for TLC545 or 1.1 MHz for TLC546, $f_{clock(SYS)}$ = 4 MHz for TLC545 or 2.1 MHz for TLC546

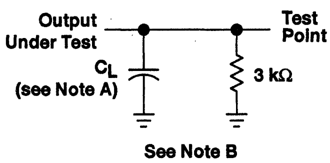
PARAMETER		TEST CONDITIONS	TLC545			TLC546			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
E_L	Linearity error	See Note 5			±0.5			±0.5	LSB
E_{ZS}	Zero-scale error	See Note 6			±0.5			±0.5	LSB
E_{FS}	Full-scale error	See Note 6			±0.5			±0.5	LSB
	Total unadjusted error	See Note 7			±0.5			±0.5	LSB
	Self-test output code	INPUT A19 address = 10011 (see Note 8)	01111101 (125)		10000011 (131)	01111101 (125)		10000011 (131)	
t_{conv}	Conversion time	See Operating Sequence			9			17	µs
	Total access and conversion time	See Operating Sequence			13			25	µs
t_{acq}	Channel acquisition time (sample cycle)	See Operating Sequence			3			3	I/O clock cycles
t_v	Time output data remains valid after I/O CLOCK↓		10			10			ns
t_d	Delay time, I/O CLOCK to DATA OUT valid	See Parameter Measurement Information			300			400	ns
t_{en}	Output enable time				150			150	ns
t_{dis}	Output disable time				150			150	ns
$t_{r(bus)}$	Data bus rise time				300			300	ns
$t_{f(bus)}$	Data bus fall time				300			300	ns

NOTES: 5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero-scale error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
7. Total unadjusted error is the sum of linearity, zero-scale, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic. The INPUT A19 analog input signal is internally generated and is used for test purposes.

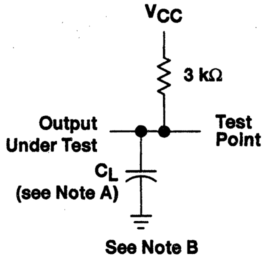
PARAMETER MEASUREMENT INFORMATION



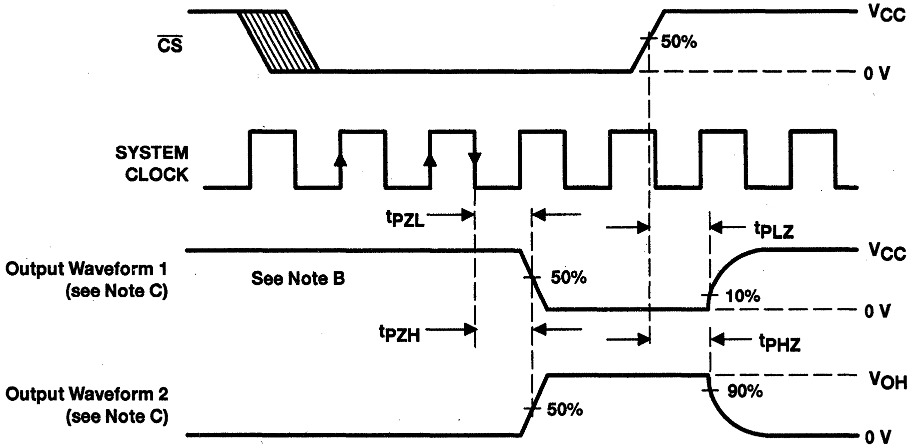
LOAD CIRCUIT FOR t_d, t_r, AND t_f



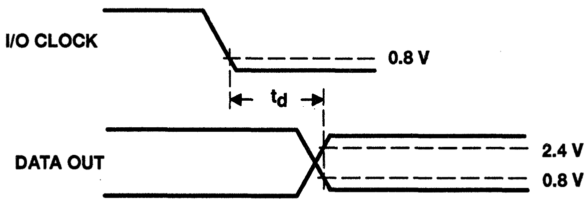
LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}



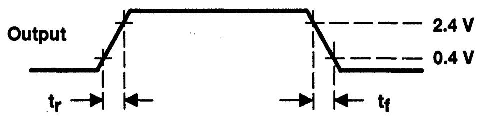
LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS FOR DELAY TIME



VOLTAGE WAVEFORMS FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF for TLC545 and 100 pF for TLC546
B. $t_{en} = t_{PZH}$ or t_{PZL}, $t_{dis} = t_{PHZ}$ or t_{PLZ}
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

simplified analog input analysis

Using the equivalent circuit in Figure 1, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c/R_tC_i}\right) \tag{1}$$

where

$$R_t = R_s + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C\ (1/2\ \text{LSB}) = V_S - (V_S/512) \tag{2}$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S/512) = V_S \left(1 - e^{-t_c/R_tC_i}\right) \tag{3}$$

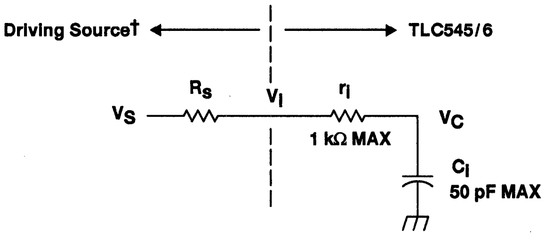
and

$$t_c\ (1/2\ \text{LSB}) = R_t \times C_i \times \ln(512) \tag{4}$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c\ (1/2\ \text{LSB}) = (R_s + 1\ \text{k}\Omega) \times 60\ \text{pF} \times \ln(512) \tag{5}$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at INPUT A0–A18
V_S = External Driving Source Voltage
R_s = Source Resistance
r_i = Input Resistance
C_i = Input Capacitance

† Driving source requirements:
- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_s must be real at the input frequency.

Figure 1. Equivalent Input Circuit Including the Driving Source

PRINCIPLES OF OPERATION

The TLC545 and TLC546 are both complete data acquisition systems on single chips. Each includes such functions as system clock, sample and hold, 8-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs; $\overline{\text{CS}}$, ADDRESS INPUT, I/O CLOCK, and SYSTEM CLOCK. These control inputs and a TTL-compatible 3-state output facilitate serial communications with a microprocessor or microcomputer. The TLC545 and TLC546 can complete conversions in a maximum of 9 and 17 μs respectively, while complete input-conversion-output cycles can be repeated at a maximum of 13 and 25 μs, respectively.

The system clock and I/O clock are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to the SYSTEM CLOCK input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using the I/O CLOCK. SYSTEM CLOCK will drive the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{\text{CS}}$ is high, DATA OUT is in a high-impedance condition, and ADDRESS INPUT and I/O CLOCK are disabled. This feature allows each of these terminals, with the exception of $\overline{\text{CS}}$, to share a control logic point with their counterpart terminals on additional A/D devices when additional TLC545/TLC546 devices are used. Thus, the above feature serves to minimize the required control logic terminals when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{\text{CS}}$ is brought low. To minimize errors caused by noise at $\overline{\text{CS}}$, the internal circuitry waits for two rising edges and then a falling edge of the SYSTEM CLOCK after a $\overline{\text{CS}}$ transition before the transition is recognized. The MSB of the previous conversion result automatically appears on DATA OUT.
2. A new positive-logic multiplexer address is shifted in on the first five rising edges of I/O CLOCK. The MSB of the address is shifted in first. The negative edges of these five I/O clocks shift out the second, third, fourth, fifth, and sixth most significant bits of the previous conversion result. The on-chip sample and hold begins sampling the newly addressed analog input after the fifth falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Two clock cycles are then applied to I/O CLOCK and the seventh and eighth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final eighth clock cycle is applied to I/O CLOCK. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 36 system clock cycles. After this final I/O clock cycle, $\overline{\text{CS}}$ must go high or the I/O CLOCK must remain low for at least 36 system clock cycles to allow for the conversion function.

$\overline{\text{CS}}$ can be kept low during periods of multiple conversion. When keeping $\overline{\text{CS}}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O CLOCK line. If glitches occur on the I/O CLOCK line, the I/O sequence between the microprocessor/controller and the device loses synchronization. Also, if $\overline{\text{CS}}$ is taken high, it must remain high until the end of conversion. Otherwise, a valid falling edge of $\overline{\text{CS}}$ causes a reset condition, which aborts the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 system clock cycles occur. Such action yields the conversion result of the previous conversion and not the ongoing conversion.

PRINCIPLES OF OPERATION

It is possible to connect SYSTEM CLOCK and I/O CLOCK together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

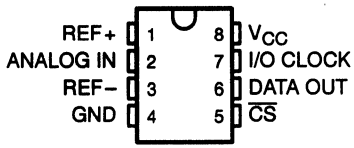
1. The first two clocks are required for this device to recognize $\overline{CS}$ is at a valid low level when the common clock signal is used as an I/O CLOCK. When $\overline{CS}$ is recognized by the device to be at a high level, the common clock signal is used for the conversion clock also.
2. A low $\overline{CS}$ must be recognized before the I/O CLOCK can shift in an analog channel address. The device recognizes a $\overline{CS}$ transition when the SYSTEM CLOCK terminal receives two positive edges and then a negative edge. For this reason, after a $\overline{CS}$ negative edge, the first two clock cycles do not shift in the address. Also, upon shifting in the address, $\overline{CS}$ must be raised after the eighth valid (10 total) I/O CLOCK. Otherwise, additional common clock cycles are recognized as I/O CLOCKS and shift in an erroneous address.

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device accommodates these applications. Although the on-chip sample and hold begins sampling upon the negative edge of the fourth valid I/O clock cycle, the hold function is not initiated until the negative edge of the eighth valid I/O clock cycle. Thus, the control circuitry can leave the I/O clock signal in its high state during the eighth valid I/O clock cycle, until the moment at which the analog signal must be converted. The TLC545/546 continues sampling the analog input until the eighth valid falling edge of the I/O clock. The control circuitry or software must then immediately lower the I/O clock signal to initiate the hold function at the desired point in time and to start conversion.

Detailed information on interfacing to most popular microprocesors is readily available from the factory.

- **Microprocessor Peripheral or Stand-Alone Operation**
- **8-Bit Resolution A/D Converter**
- **Differential Reference Input Voltages**
- **Conversion Time . . . 17 μs Max**
- **Total Access and Conversion Cycles Per Second**
  - **TLC548 . . . up to 45,500**
  - **TLC549 . . . up to 40,000**
- **On-Chip Software-Controllable Sample-and-Hold**
- **Total Unadjusted Error . . . ±0.5 LSB Max**
- **4-MHz Typical Internal System Clock**
- **Wide Supply Range . . . 3 V to 6 V**
- **Low Power Consumption . . . 15 mW Max**
- **Ideal for Cost-Effective, High-Performance Applications Including Battery-Operated Portable Instrumentation**
- **Pinout and Control Signals Compatible With the TLC540 and TLC545 8-Bit A/D Converters and with the TLC1540 10-Bit A/D Converter**
- **CMOS Technology**

D OR P PACKAGE
(TOP VIEW)



description

The TLC548 and TLC549 are CMOS analog-to-digital converter integrated circuits built around an 8-bit switched-capacitor successive-approximation ADC. They are designed for serial interface with a microprocessor or peripheral through a 3-state data output and an analog input. The TLC548 and TLC549 use only the input/output clock (I/O CLOCK) input along with the chip select ($\overline{CS}$) input for data control. The maximum I/O CLOCK input frequency of the TLC548 is 2.048 MHz, and the I/O CLOCK input frequency of the TLC549 is specified up to 1.1 MHz. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

Operation of the TLC548 and the TLC549 is very similar to that of the more complex TLC540 and TLC541 devices; however, the TLC548 and TLC549 provide an on-chip system clock that operates typically at 4 MHz and requires no external components. The on-chip system clock allows internal device operation to proceed independently of serial input/output data timing and permits manipulation of the TLC548 and TLC549 as desired for a wide range of software and hardware requirements. The I/O CLOCK together with the internal system clock allow high-speed data transfer and conversion rates of 45,500 conversions per second for the TLC548, and 40,000 conversions per second for the TLC549.

AVAILABLE OPTIONS

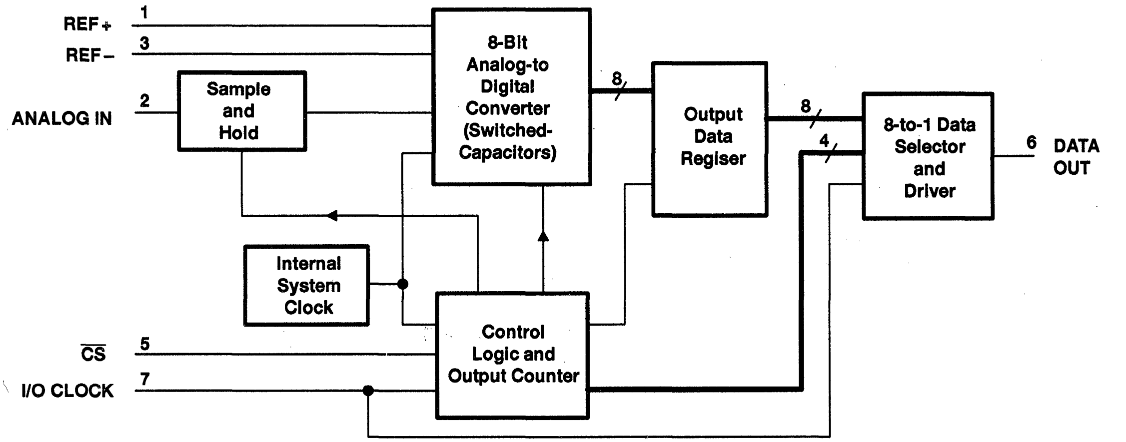
T_A	PACKAGE	
	SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	TLC548CD TLC549CD	TLC548CP TLC549CP
−40°C to 85°C	TLC548ID TLC549ID	TLC548IP TLC549IP

description (Continued)

Additional TLC548 and TLC549 features include versatile control logic, an on-chip sample-and-hold circuit that can operate automatically or under microprocessor control, and a high-speed converter with differential high-impedance reference voltage inputs that ease ratiometric conversion, scaling, and circuit isolation from logic and supply noises. Design of the totally switched-capacitor successive-approximation converter circuit allows conversion with a maximum total error of ±0.5 least significant bit (LSB) in less than 17 µs.

The TLC548C and TLC549C are characterized for operation from 0°C to 70°C. The TLC548I and TLC549I are characterized for operation from −40°C to 85°C.

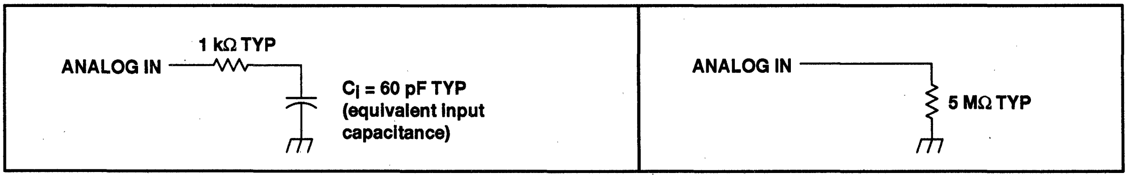
functional block diagram



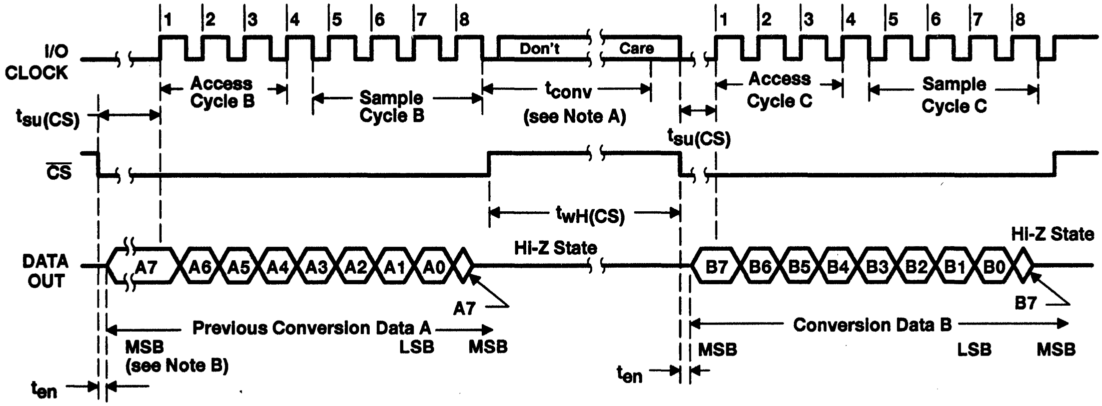
typical equivalent inputs

INPUT CIRCUIT IMPEDANCE DURING SAMPLING MODE

INPUT CIRCUIT IMPEDANCE DURING HOLD MODE



operating sequence



NOTES: A. The conversion cycle, which requires 36 internal system clock periods (17 µs maximum), is initiated with the eighth I/O clock pulse trailing edge after $\overline{CS}$ goes low for the channel whose address exists in memory at the time.

B. The most significant bit (A7) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6–A0) will be clocked out on the first seven I/O clock falling edges. B7–B0 will follow in the same manner.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) .... 6.5 V
Input voltage range at any input .... –0.3 V to V_{CC} + 0.3 V
Output voltage range .... –0.3 V to V_{CC} + 0.3 V
Peak input current range (any input) .... ±10 mA
Peak total input current range (all inputs) .... ±30 mA
Operating free-air temperature range, T_A (see Note 2): TLC548C, TLC549C .... 0°C to 70°C
TLC548I, TLC549I .... –40°C to 85°C
Storage temperature range, T_{stg} .... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal with the REF– and GND terminals connected together, unless otherwise noted.

2. The D package is not recommended below –40°C.

recommended operating conditions

		TLC548			TLC549			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		3	5	6	3	5	6	V
Positive reference voltage, V_{ref+} (see Note 3)		2.5	V_{CC}	V_{CC}+0.1	2.5	V_{CC}	V_{CC}+0.1	V
Negative reference voltage, V_{ref-} (see Note 3)		−0.1	0	2.5	−0.1	0	2.5	V
Differential reference voltage, V_{ref+}, V_{ref-} (see Note 3)		1	V_{CC}	V_{CC}+0.2	1	V_{CC}	V_{CC}+0.2	V
Analog input voltage (see Note 3)		0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH} (for V_{CC} = 4.75 V to 5.5 V)		2			2			V
Low-level control input voltage, V_{IL} (for V_{CC} = 4.75 V to 5.5 V)				0.8			0.8	V
Input/output clock frequency, $f_{clock(I/O)}$ (for V_{CC} = 4.75 V to 5.5 V)		0		2.048	0		1.1	MHz
Input/output clock high, $t_{wH(I/O)}$ (for V_{CC} = 4.75 V to 5.5 V)		200			404			ns
Input/output clock low, $t_{wL(I/O)}$ (for V_{CC} = 4.75 V to 5.5 V)		200			404			ns
Input/output clock transition time, $t_{t(I/O)}$ (see Note 4) (for V_{CC} = 4.75 V to 5.5 V)				100			100	ns
Duration of $\overline{CS}$ input high state during conversion, $t_{wH(CS)}$ (for V_{CC} = 4.75 V to 5.5 V)		17			17			µs
Setup time, $\overline{CS}$ low before first I/O CLOCK, $t_{su(CS)}$ (for V_{CC} = 4.75 V to 5.5 V) (see Note 5)		1.4			1.4			µs
Operating free-air temperature, T_A	TLC548C, TLC549C	0		70	0		70	°C
	TLC548I, TLC549I	−40		85	−40		85	

NOTES: 3. Analog input voltages greater than that applied to REF+ convert to all ones (11111111), while input voltages less than that applied to REF− convert to all zeros (00000000). For proper operation, the positive reference voltage V_{ref+}, must be at least 1 V greater than the negative reference voltage V_{ref-}. In addition, unadjusted errors may increase as the differential reference voltage $V_{ref+} - V_{ref-}$ falls below 4.75 V.

4. This is the time required for the input/output clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 µs for remote data acquisition applications in which the sensor and the ADC are placed several feet away from the controlling microprocessor.

5. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and one falling edge of internal system clock after $\overline{CS}$↓ before responding to control input signals. This $\overline{CS}$ set-up time is given by the t_{en} and $t_{su(CS)}$ specifications.

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 4.75 V to 5.5 V, $f_{clock(I/O)}$ = 2.048 MHz for TLC548 or 1.1 MHz for TLC549 (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.75 V,	I_{OH} = −360 µA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 3.2 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}			10	µA
			V_O = 0,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current, control inputs		$V_I = V_{CC}$			0.005	2.5	µA
I_{IL}	Low-level input current, control inputs		V_I = 0			−0.005	−2.5	µA
$I_{I(on)}$	Analog channel on-state input current during sample cycle		Analog input at V_{CC}			0.4	1	µA
			Analog input at 0 V			−0.4	−1	
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.8	2.5	mA
$I_{CC} + I_{ref}$	Supply and reference current		$V_{ref+} = V_{CC}$			1.9	3	mA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

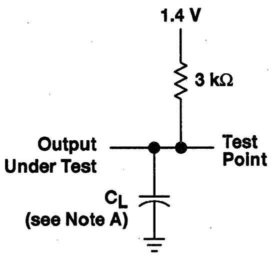
operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 4.75 V to 5.5 V, $f_{clock(I/O)}$ = 2.048 MHz for TLC548 or 1.1 MHz for TLC549 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLC548			TLC549			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
E_L	Linearity error	See Note 6			±0.5			±0.5	LSB
E_{ZS}	Zero-scaleerror	See Note 7			±0.5			±0.5	LSB
E_{FS}	Full-scale error	See Note 7			±0.5			±0.5	LSB
	Total unadjusted error	See Note 8			±0.5			±0.5	LSB
t_{conv}	Conversion time	See Operating Sequence		8	17		12	17	µs
	Total access and conversion time	See Operating Sequence		12	22		19	25	µs
t_a	Channel acquisition time (sample cycle)	See Operating Sequence			4			4	I/O clock cycles
t_v	Time output data remains valid after I/O CLOCK↓		10			10			ns
t_d	Delay time to data output valid	I/O CLOCK↓			2000			400	ns
t_{en}	Output enable time				1.4			1.4	µs
t_{dis}	Output disable time	See Parameter Measurement Information			150			150	ns
$t_{r(bus)}$	Data bus rise time				300			300	ns
$t_{f(bus)}$	Data bus fall time				300			300	ns

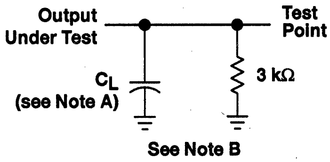
† All typicals are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 6. Linearity error is the deviation from the best straight line through the A/D transfer characteristics.
7. Zero-scale error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
8. Total unadjusted error is the sum of linearity, zero-scale, and full-scale errors.

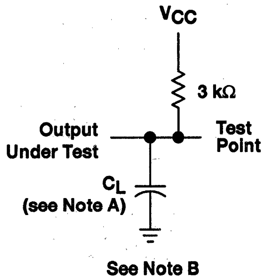
PARAMETER MEASUREMENT INFORMATION



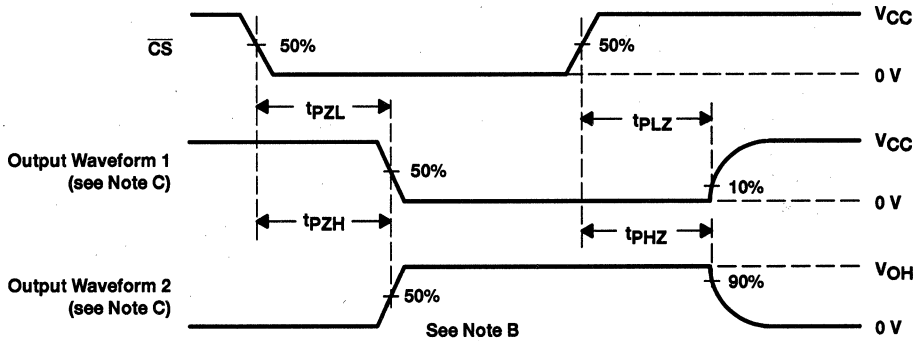
LOAD CIRCUIT FOR
t_d, t_r, AND t_f



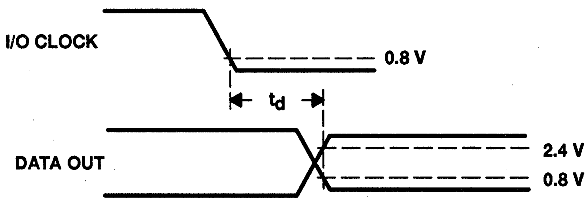
LOAD CIRCUIT FOR
t_{PZH} AND t_{PHZ}



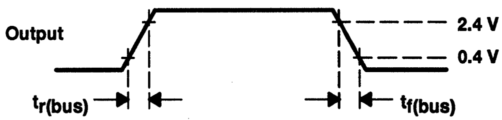
LOAD CIRCUIT FOR
t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS FOR DELAY TIME



VOLTAGE WAVEFORMS FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF for TLC548 and 100 pF for TLC549; C_L includes jig capacitance.
B. $t_{en} = t_{PZH}$ or t_{PZL}, $t_{dis} = t_{PHZ}$ or t_{PLZ}.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

APPLICATIONS INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 1, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S\left(1 - e^{-t_c/R_tC_i}\right) \quad (1)$$

where

$$R_t = R_s + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C\,(1/2\ \text{LSB}) = V_S - (V_S/512) \quad (2)$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S/512) = V_S\left(1 - e^{-t_c/R_tC_i}\right) \quad (3)$$

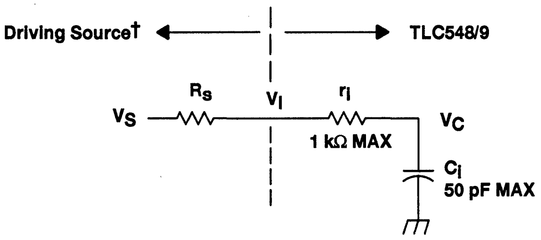
and

$$t_c\,(1/2\ \text{LSB}) = R_t \times C_i \times \ln(512) \quad (4)$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c\,(1/2\ \text{LSB}) = (R_s + 1\ \text{k}\Omega) \times 60\ \text{pF} \times \ln(512) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at ANALOG IN
V_S = External Driving Source Voltage
R_s = Source Resistance
r_i = Input Resistance
C_i = Input Capacitance

† Driving source requirements:
- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_s must be real at the input frequency.

Figure 1. Equivalent Input Circuit Including the Driving Source

PRINCIPLES OF OPERATION

The TLC548 and TLC549 are each complete data acquisition systems on a single chip. Each contains an internal system clock, sample and hold, 8-bit A/D converter, data register, and control logic circuitry. For flexibility and access speed, there are two control inputs: I/O CLOCK and chip select ($\overline{CS}$). These control inputs and a TTL-compatible 3-state output facilitate serial communications with a microprocessor or minicomputer. A conversion can be completed in 17 µs or less, while complete input-conversion-output cycles can be repeated in 22 µs for the TLC548 and in 25 µs for the TLC549.

The internal system clock and I/O CLOCK are used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Due to this independence and the internal generation of the system clock, the control hardware and software need only be concerned with reading the previous conversion result and starting the conversion by using the I/O clock. In this manner, the internal system clock drives the “conversion crunching” circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, DATA OUT is in a high-impedance condition and I/O CLOCK is disabled. This $\overline{CS}$ control function allows I/O CLOCK to share the same control logic point with its counterpart terminal when additional TLC548 and TLC549 devices are used. This also serves to minimize the required control logic terminals when using multiple TLC548 and TLC549 devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for two rising edges and then a falling edge of the internal system clock after a $\overline{CS}\downarrow$ before the transition is recognized. However, upon a $\overline{CS}$ rising edge, DATA OUT will go to a high-impedance state within the t_{dis} specification even though the rest of the integrated circuitry will not recognize the transition until the $t_{su(CS)}$ specification has elapsed. This technique is used to protect the device against noise when used in a noisy environment. The most significant bit (MSB) of the previous conversion result will initially appear on DATA OUT when $\overline{CS}$ goes low.
2. The falling edges of the first four I/O CLOCK cycles shift out the second, third, fourth, and fifth most significant bits of the previous conversion result. The on-chip sample and hold begins sampling the analog input after the fourth high-to-low transition of I/O CLOCK. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Three more I/O CLOCK cycles are then applied to the I/O CLOCK terminal and the sixth, seventh, and eighth conversion bits are shifted out on the falling edges of these clock cycles.
4. The final, (the eighth), clock cycle is applied to I/O CLOCK. The on-chip sample and hold begins the hold function upon the high-to-low transition of this clock cycle. The hold function will continue for the next four internal system clock cycles, after which the holding function terminates and the conversion is performed during the next 32 system clock cycles, giving a total of 36 cycles. After the eighth I/O CLOCK cycle, $\overline{CS}$ must go high or the I/O clock must remain low for at least 36 internal system clock cycles to allow for the completion of the hold and conversion functions. $\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O CLOCK line. If glitches occur on I/O CLOCK, the I/O sequence between the microprocessor/controller and the device will lose synchronization. If $\overline{CS}$ is taken high, it must remain high until the end of conversion. Otherwise, a valid high-to-low transition of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 internal system clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

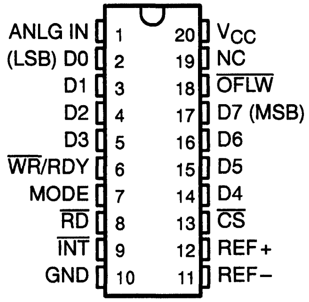
PRINCIPLES OF OPERATION

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device will accommodate these applications. Although the on-chip sample and hold begins sampling upon the high-to-low transition of the fourth I/O CLOCK cycle, the hold function does not begin until the high-to-low transition of the eighth I/O CLOCK cycle, which should occur at the moment when the analog signal must be converted. The TLC548 and TLC549 will continue sampling the analog input until the high-to-low transition of the 8th I/O CLOCK pulse. The control circuitry or software will then immediately lower I/O CLOCK and start the holding function to hold the analog signal at the desired point in time and start conversion.

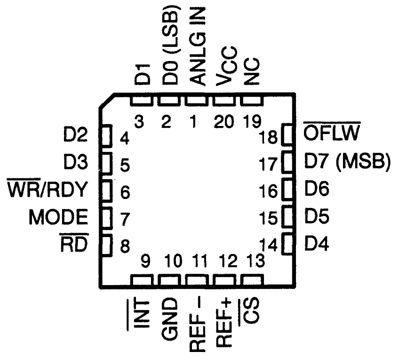
Detailed information on interfacing to the most popular microprocessor is readily available from Texas Instruments.

- **Advanced LinCMOS™ Silicon-Gate Technology**
- **8-Bit Resolution**
- **Differential Reference Inputs**
- **Parallel Microprocessor Interface**
- **Conversion and Access Time Over Temperature Range**
  Read Mode . . . 2.5 μs Max
- **No External Clock or Oscillator Components Required**
- **On-Chip Track and Hold**
- **Single 5-V Supply**
- **TLC0820A Is Direct Replacement for National Semiconductor ADC0820C/CC and Analog Devices AD7820K/B/T**

DB, DW, OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLC0820AC and the TLC0820AI are Advanced LinCMOS™ 8-bit analog-to-digital converters each consisting of two 4-bit flash converters, a 4-bit digital-to-analog converter, a summing (error) amplifier, control logic, and a result latch circuit. The modified flash technique allows low-power integrated circuitry to complete an 8-bit conversion in 1.18 μs over temperature. The on-chip track-and-hold circuit has a 100-ns sample window and allows these devices to convert continuous analog signals having slew rates of up to 100 mV/μs without external sampling components. TTL-compatible 3-state output drivers and two modes of operation allow interfacing to a variety of microprocessors. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

AVAILABLE OPTIONS

T_A	TOTAL UNADJUSTED ERROR	PACKAGE			
		SSOP (DB)	PLASTIC SMALL OUTLINE (DW)	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	±1 LSB	TLC0820ACDB	TLC0820ACDW	TLC0820ACFN	TLC0820ACN
–40°C to 85°C	±1 LSB	TLC0820AIDB	TLC0820AIDW	TLC0820AIFN	TLC0820AIN

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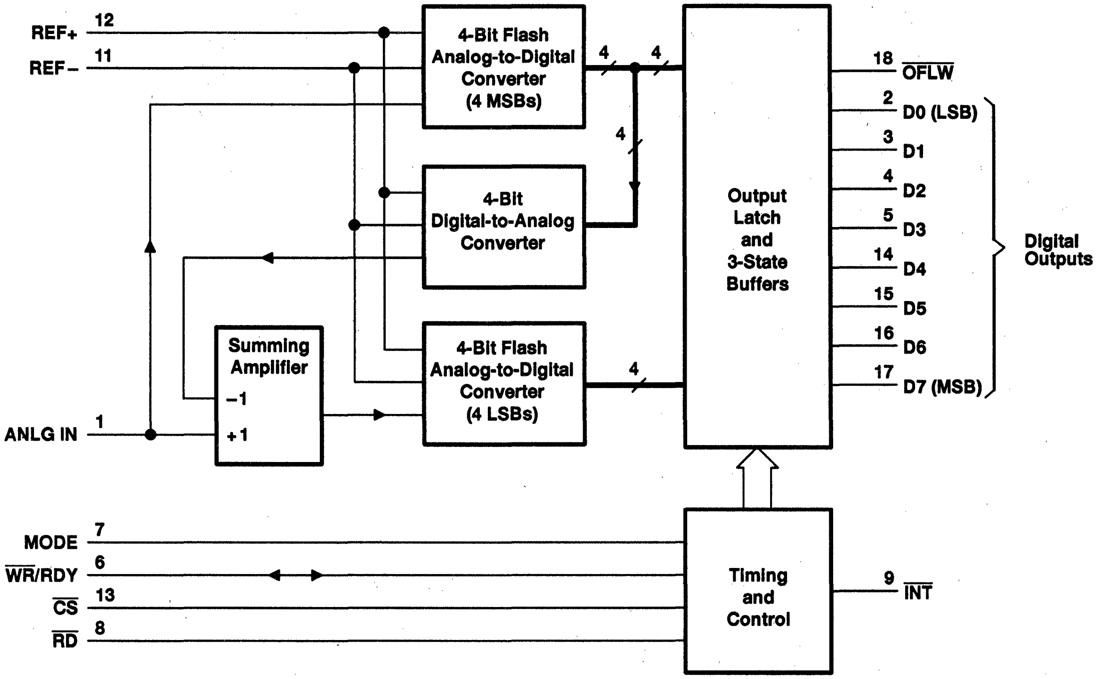
functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ANLG IN	1	I	Analog input
$\overline{CS}$	13	I	Chip select. $\overline{CS}$ must be low in order for $\overline{RD}$ or $\overline{WR}$ to be recognized by the ADC.
D0	2	O	Digital, 3-state output data, bit 1 (LSB)
D1	3	O	Digital, 3-state output data, bit 2
D2	4	O	Digital, 3-state output data, bit 3
D3	5	O	Digital, 3-state output data, bit 4
D4	14	O	Digital, 3-state output data, bit 5
D5	15	O	Digital, 3-state output data, bit 6
D6	16	O	Digital, 3-state output data, bit 7
D7	17	O	Digital, 3-state output data, bit 8 (MSB)
GND	10		Ground
$\overline{INT}$	9	O	Interrupt. In the write-read mode, the interrupt output ($\overline{INT}$) going low indicates that the internal count-down delay time, $t_{d(int)}$, is complete and the data result is in the output latch. The delay time $t_{d(int)}$ is typically 800 ns starting after the rising edge of $\overline{WR}$ (see operating characteristics and Figure 3). If $\overline{RD}$ goes low prior to the end of $t_{d(int)}$, $\overline{INT}$ goes low at the end of $t_{d(RIL)}$ and the conversion results are available sooner (see Figure 2). $\overline{INT}$ is reset by the rising edge of either $\overline{RD}$ or $\overline{CS}$.
MODE	7	I	Mode select. MODE is internally tied to GND through a 50-μA current source, which acts like a pulldown resistor. When MODE is low, the read mode is selected. When MODE is high, the write-read mode is selected.
NC	19		No internal connection
$\overline{OFLW}$	18	O	Overflow. Normally $\overline{OFLW}$ is a logical high. However, if the analog input is higher than V_{ref+}, $\overline{OFLW}$ will be low at the end of conversion. It can be used to cascade two or more devices to improve resolution (9 or 10 bits).
$\overline{RD}$	8	I	Read. In the write-read mode with $\overline{CS}$ low, the 3-state data outputs D0 through D7 are activated when $\overline{RD}$ goes low. $\overline{RD}$ can also be used to increase the conversion speed by reading data prior to the end of the internal count-down delay time. As a result, the data transferred to the output latch is latched after the falling edge of $\overline{RD}$. In the read mode with $\overline{CS}$ low, the conversion starts with $\overline{RD}$ going low. $\overline{RD}$ also enables the 3-state data outputs on completion of the conversion. RDY going into the high-impedance state and $\overline{INT}$ going low indicate completion of the conversion.
REF−	11	I	Reference voltage. REF− is placed on the bottom of the resistor ladder.
REF+	12	I	Reference voltage. REF+ is placed on the top of the resistor ladder.
V_{CC}	20		Power supply voltage
$\overline{WR}$/RDY	6	I/O	Write ready. In the write-read mode with $\overline{CS}$ low, the conversion is started on the falling edge of the $\overline{WR}$ input signal. The result of the conversion is strobed into the output latch after the internal count-down delay time, $t_{d(int)}$, provided that the $\overline{RD}$ input does not go low prior to this time. The delay time $t_{d(int)}$ is approximately 800 ns. In the read mode, RDY (an open-drain output) goes low after the falling edge of $\overline{CS}$ and goes into the high-impedance state when the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) .... 10 V
Input voltage range, all inputs (see Note 1) .... −0.2 V to V_{CC}+0.2 V
Output voltage range, all outputs (see Note 1) .... −0.2 V to V_{CC}+0.2 V
Operating free-air temperature range: TLC0820AC .... 0°C to 70°C
TLC0820AI .... −40°C to 85°C
Storage temperature range .... −65°C to 150°C
Case temperature for 10 seconds: FN package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DB, DW or N package .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to network GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			4.5	5	8	V
Analog input voltage			−0.1		V_{CC}+0.1	V
Positive reference voltage, V_{ref+}			V_{ref-}		V_{CC}	V
Negative reference voltage, V_{ref-}			GND		V_{ref+}	V
High-level input voltage, V_{IH}	V_{CC} = 4.75 V to 5.25 V	$\overline{CS}$, $\overline{WR}$/RDY, $\overline{RD}$	2			V
		MODE	3.5			
Low-level input voltage, V_{IL}	V_{CC} = 4.75 V to 5.25 V	$\overline{CS}$, $\overline{WR}$/RDY, $\overline{RD}$			0.8	V
		MODE			1.5	
Pulse duration, write in write-read mode, $t_{w(W)}$ (see Figures 2, 3, and 4)			0.5		50	μs
Operating free-air temperature, T_A	TLC0820AC		0		70	°C
	TLC0820AI		−40		85	

electrical characteristics at specified operating free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	D0–D7, $\overline{\text{INT}}$, or $\overline{\text{OFLW}}$	V_{CC} = 4.75 V, I_{OH} = –360 µA	Full range	2.4			V
			V_{CC} = 4.75 V, I_{OH} = –10 µA	Full range	4.5			
				25°C	4.6			
V_{OL}	Low-level output voltage	D0–D7, $\overline{\text{OFLW}}$, $\overline{\text{INT}}$, or $\overline{\text{WR}}$/RDY	V_{CC} = 5.25 V, I_{OL} = 1.6 mA	Full range			0.4	V
				25°C			0.34	
I_{IH}	High-level input current	$\overline{\text{CS}}$ or $\overline{\text{RD}}$	V_{IH} = 5 V	Full range		0.005	1	µA
		WR/RDY		Full range			3	
				25°C		0.1	0.3	
		MODE		Full range			200	
				25°C		50	170	
I_{IL}	Low-level input current	$\overline{\text{CS}}$, $\overline{\text{WR}}$/RDY, $\overline{\text{RD}}$, or MODE	V_{IL} = 0	Full range		–0.005	–1	µA
I_{OZ}	Off-state (high-impedance-state) output current	D0–D7 or $\overline{\text{WR}}$/RDY	V_O = 5 V	Full range			3	µA
				25°C		0.1	0.3	
			V_O = 0	Full range			–3	
				25°C		–0.1	–0.3	
I_I	Analog input current		CS at 5 V, V_I = 5 V	Full range			3	µA
				25°C			0.3	
			CS at 5 V, V_I = 0	Full range			–3	
				25°C			–0.3	
I_{OS}	Short-circuit output current	D0–D7, $\overline{\text{OFLW}}$, $\overline{\text{INT}}$, or $\overline{\text{WR}}$/RDY	V_O = 5 V	Full range	7			mA
				25°C	8.4	14		
		D0–D7 or $\overline{\text{OFLW}}$	V_O = 0	Full range	–6			
				25°C	–7.2	–12		
		INT		Full range	–4.5			
				25°C	– 5.3	–9		
R_{ref}	Reference resistance			Full range	1.25		6	kΩ
				25°C	1.4	2.3	5.3	
I_{CC}	Supply current		$\overline{\text{CS}}$, $\overline{\text{WR}}$/RDY, and $\overline{\text{RD}}$ at 0 V	Full range			15	mA
				25°C		7.5	13	
C_i	Input capacitance	D0–D7		Full range		5		pF
		ANLG IN				45		
C_o	Output capacitance	D0–D7		Full range			5	pF

† Full range is as specified in recommended operating conditions.

operating characteristics, V_{CC} = 5 V, V_{ref+} = 5 V, V_{ref-} = 0, t_r = t_f = 20 ns, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
k_{SVS}	Supply-voltage sensitivity	V_{CC} = 5 V ± 5%,	T_A = MIN to MAX		±1/16	±1/4	LSB
	Total unadjusted error‡	MODE at 0 V,	T_A = MIN to MAX			1	LSB
$t_{conv(R)}$	Conversion time, read mode	MODE at 0 V,	See Figure 1		1.6	2.5	µs
$t_{a(R)}$	Access time, $\overline{RD}$↓ to data valid	MODE at 0 V,	See Figure 1		$t_{conv(R)}$ +20	$t_{conv(R)}$ +50	ns
$t_{a(R1)}$	Access time, $\overline{RD}$↓ to data valid	MODE at 5 V, $t_{d(WR)} < t_{d(int)}$, See Figure 2	C_L = 15 pF		190	280	ns
			C_L = 100 pF		210	320	
$t_{a(R2)}$	Access time, $\overline{RD}$↓ to data valid	MODE at 5 V, $t_{d(WR)} > t_{d(int)}$, See Figure 3	C_L = 15 pF		70	120	ns
			C_L = 100 pF		90	150	
$t_{a(INT)}$	Access time, $\overline{INT}$↓ to data valid	MODE at 5 V,	See Figure 4		20	50	ns
t_{dis}	Disable time, $\overline{RD}$↑ to data valid	R_L = 1 kΩ, See Figures 1, 2, 3, and 5	C_L = 10 pF,		70	95	ns
$t_{d(int)}$	Delay time, $\overline{WR}$/RDY↑ to $\overline{INT}$↓	MODE at 5 V, See Figures 2, 3, and 4	C_L = 50 pF,		800	1300	ns
$t_{d(NC)}$	Delay time, to next conversion	See Figures 1, 2, 3, and 4		500			ns
$t_{d(WR)}$	Delay time, $\overline{WR}$/RDY↑ to $\overline{RD}$↓ in write-read mode	See Figure 2		0.4			µs
$t_{d(RDY)}$	Delay time, $\overline{CS}$↓ to $\overline{WR}$/RDY↓	MODE at 0 V, See Figure 1	C_L = 50 pF,		50	100	ns
$t_{d(RIH)}$	Delay time, $\overline{RD}$↑ to $\overline{INT}$↑	C_L = 50 pF,	See Figures 1, 2, and 3		125	225	ns
$t_{d(RIL)}$	Delay time, $\overline{RD}$↓ to $\overline{INT}$↓	MODE at 5 V, See Figure 2	$t_{d(WR)} < t_{d(int)}$,		200	290	ns
$t_{d(WIH)}$	Delay time, $\overline{WR}$/RDY↑ to $\overline{INT}$↑	MODE at 5 V, See Figure 4	C_L = 50 pF,		175	270	ns
	Slew-rate tracking				0.1		V/µs

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ Total unadjusted error includes offset, full-scale, and linearity errors.

PARAMETER MEASUREMENT INFORMATION

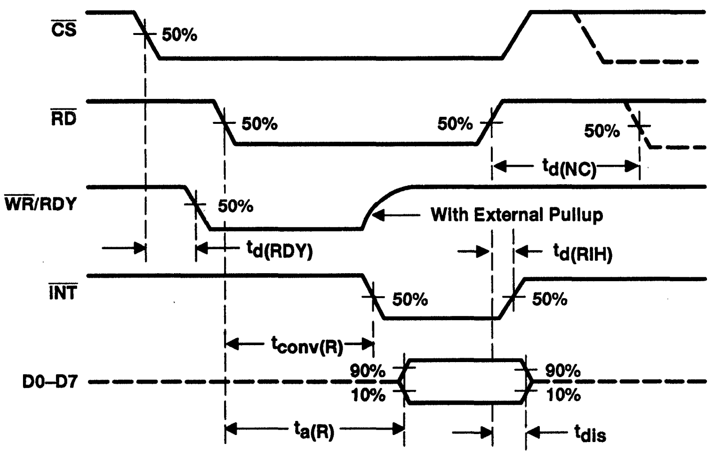


Figure 1. Read-Mode Waveforms (MODE Low)

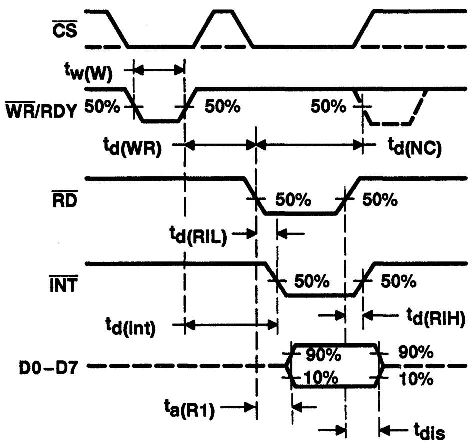


Figure 2. Write-Read-Mode Waveforms [MODE High and $t_{d(WR)} < t_{d(int)}$]

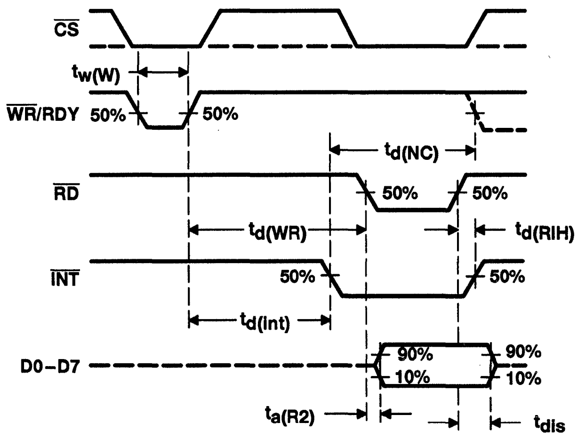


Figure 3. Write-Read-Mode Waveforms [MODE High and $t_{d(WR)} > t_{d(int)}$]

PARAMETER MEASUREMENT INFORMATION

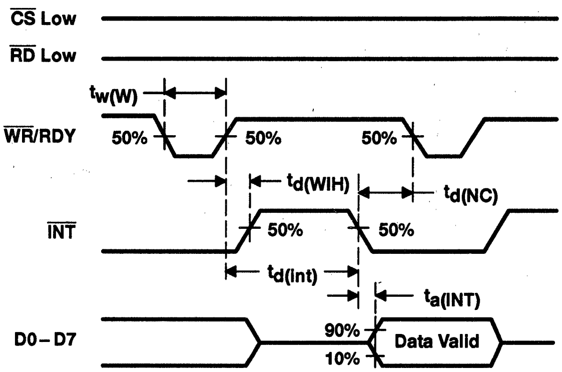


Figure 4. Write-Read-Mode Waveforms (Stand-Alone Operation, MODE High, and RD Low)

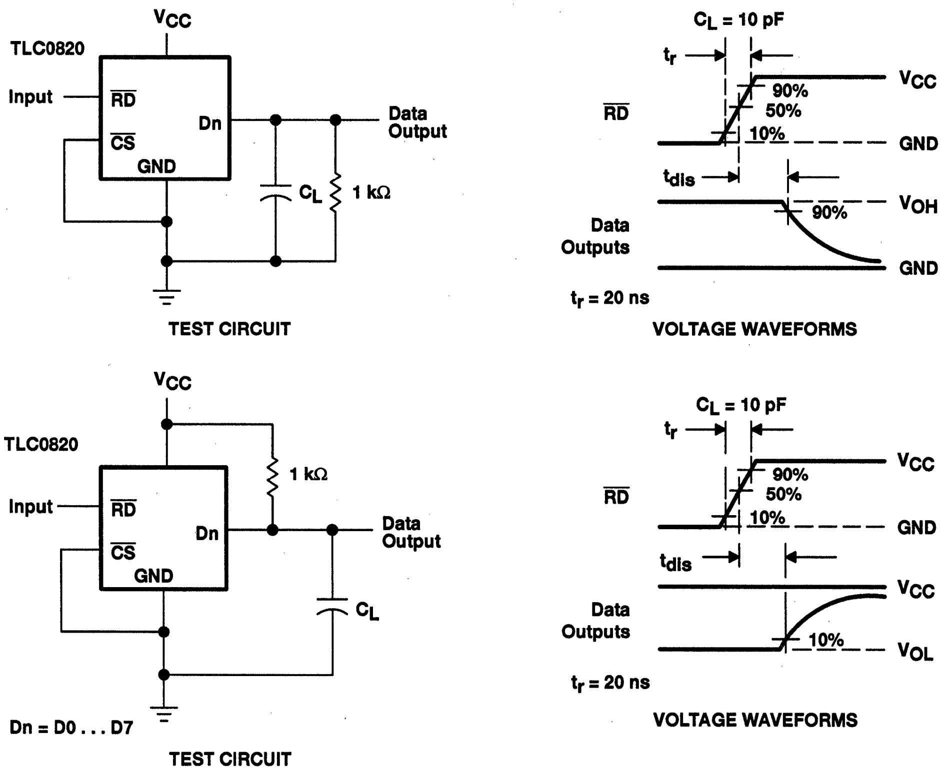


Figure 5. Test Circuit and Voltage Waveforms

PRINCIPLES OF OPERATION

The TLC0820AC and TLC0820AI each employ a combination of sampled-data comparator techniques and flash techniques common to many high-speed converters. Two 4-bit flash analog-to-digital conversions are used to give a full 8-bit output.

The recommended analog input voltage range for conversion is −0.1 V to V_{CC} + 0.1 V. Analog input signals that are less than V_{ref-} + 1/2 LSB or greater than V_{ref+} – 1/2 LSB convert to 00000000 or 11111111, respectively. The reference inputs are fully differential with common-mode limits defined by the supply rails. The reference input values define the full-scale range of the analog input. This allows the gain of the ADC to be varied for ratiometric conversion by changing the V_{ref+} and V_{ref-} voltages.

The device operates in two modes, read (only) and write-read, that are selected by MODE. The converter is set to the read (only) mode when MODE is low. In the read mode, $\overline{WR}$/RDY is used as an output and is referred to as the ready terminal. In this mode, a low on $\overline{WR}$/RDY while $\overline{CS}$ is low indicates that the device is busy. Conversion starts on the falling edge of $\overline{RD}$ and is completed no more than 2.5 µs later when $\overline{INT}$ falls and $\overline{WR}$/RDY returns to the high-impedance state. Data outputs also change from high-impedance to active states at this time. After the data is read, $\overline{RD}$ is taken high, $\overline{INT}$ returns high, and the data outputs return to their high-impedance states.

When MODE is high, the converter is set to the write-read mode and $\overline{WR}$/RDY is referred to as the write terminal. Taking $\overline{CS}$ and $\overline{WR}$/RDY low selects the converter and initiates measurement of the input signal. Approximately 600 ns after $\overline{WR}$/RDY returns high, the conversion is completed. Conversion starts on the rising edge of $\overline{WR}$/RDY in the write-read mode.

The high-order 4-bit flash ADC measures the input by means of 16 comparators operating simultaneously. A high-precision 4-bit DAC then generates a discrete analog voltage from the result of that conversion. After a time delay, a second bank of comparators does a low-order conversion on the analog difference between the input level and the high-order DAC output. The results from each of these conversions enter an 8-bit latch and are output to the 3-state output buffers on the falling edge of $\overline{RD}$.

APPLICATION INFORMATION

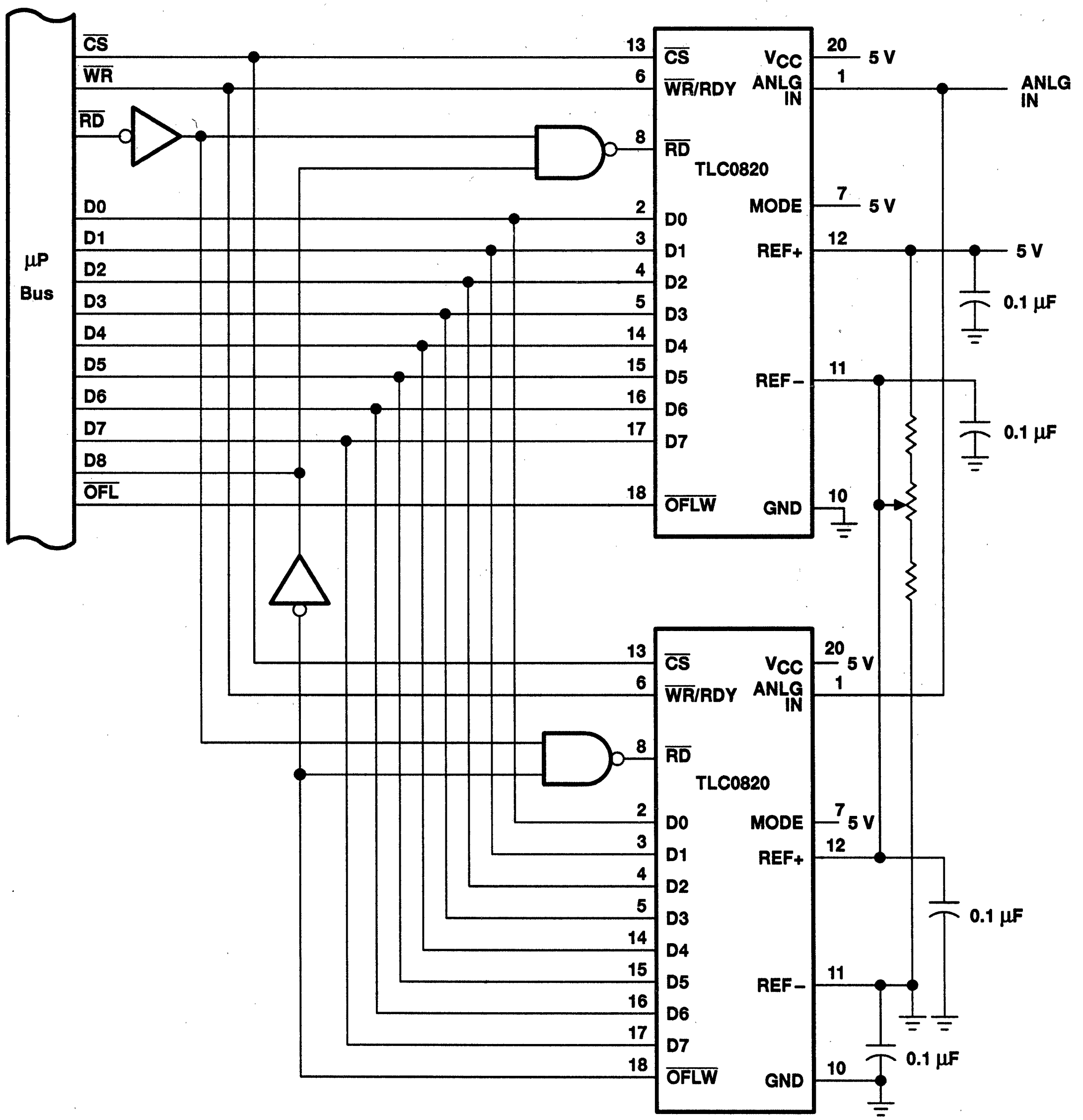
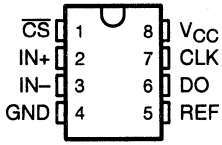


Figure 6. Configuration for 9-Bit Resolution

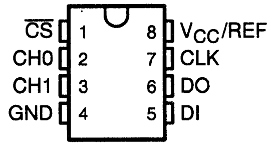
- **8-Bit Resolution**
- **Easy Microprocessor Interface or Stand-Alone Operation**
- **Operates Ratiometrically or With 5-V Reference**
- **Single Channel or Multiplexed Twin Channels With Single-Ended or Differential Input Options**
- **Input Range 0 to 5 V With Single 5-V Supply**
- **Inputs and Outputs Are Compatible With TTL and MOS**
- **Conversion Time of 32 μs at f_{clock} = 250 kHz**
- **Designed to Be Interchangeable With National Semiconductor ADC0831 and ADC0832**

DEVICE	TOTAL UNADJUSTED ERROR	
	A-SUFFIX	B-SUFFIX
TLC0831	± 1 LSB	± 1/2 LSB
TLC0832	± 1 LSB	± 1/2 LSB

TLC0831 . . . D OR P PACKAGE
(TOP VIEW)



TLC0832 . . . D OR P PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

These devices are 8-bit successive-approximation analog-to-digital converters. The TLC0831 has single input channels; the TLC0832 has multiplexed twin input channels. The serial output is configured to interface with standard shift registers or microprocessors. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The TLC0832 multiplexer is software configured for single-ended or differential inputs. The differential analog voltage input allows for common-mode rejection or offset of the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

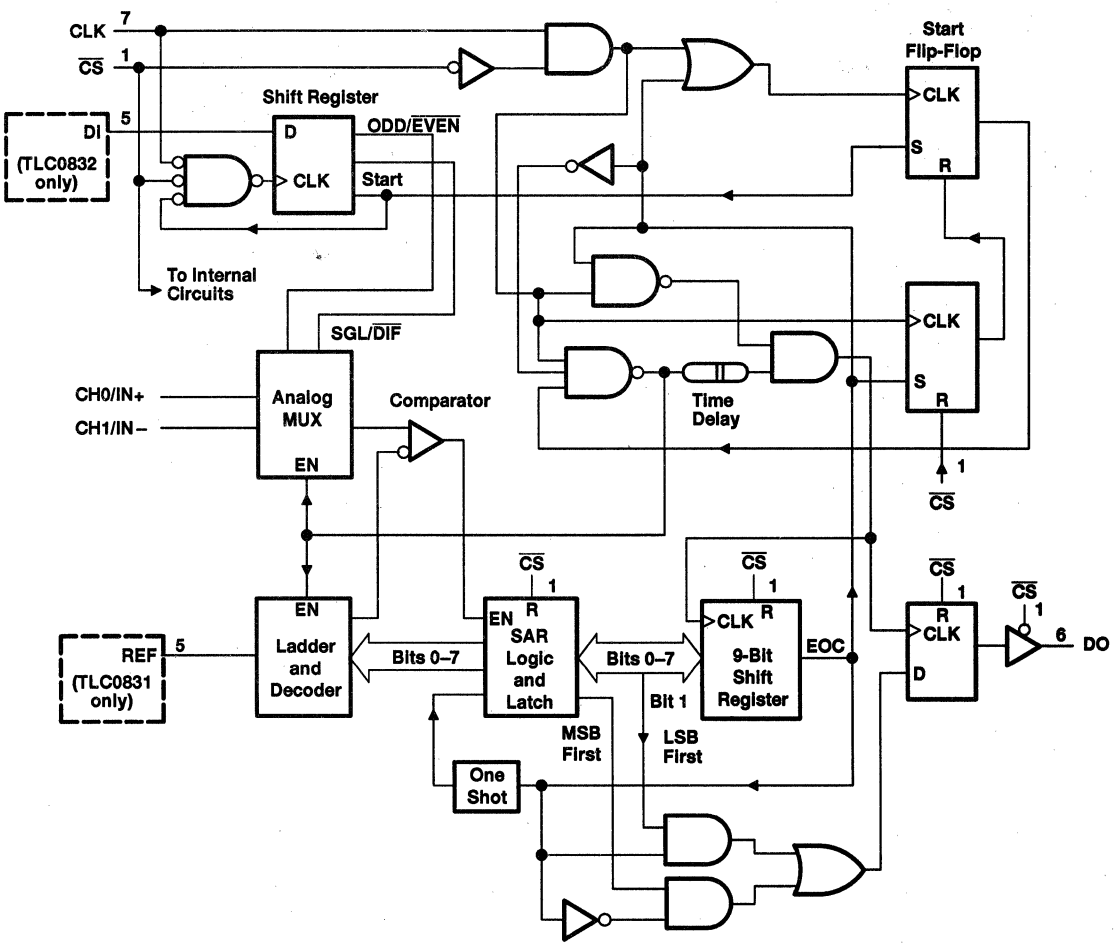
The operation of the TLC0831 and TLC0832 devices is very similar to the more complex TLC0834 and TLC0838 devices. Ratiometric conversion can be attained by setting the REF input equal to the maximum analog input signal value, which gives the highest possible conversion resolution. Typically, REF is set equal to V_{CC} (done internally on the TLC0832). For more detail on the operation of the TLC0831 and TLC0832 devices, refer to the TLC0834/TLC0838 data sheet.

The TLC0831AC, TLC0831BC, TLC0832AC, and TLC0832BC are characterized for operation from 0°C to 70°C. The TLC0831AI, TLC0831BI, TLC0832AI, and TLC0832BI are characterized for operation from −40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGE			
	SMALL OUTLINE (D)		PLASTIC DIP (P)	
0°C to 70°C	TLC0831ACP TLC0831BCP	TLC0832ACP TLC0832BCP	TLC0831ACP TLC0831BCP	TLC0832ACP TLC0832BCP
−40°C to 85°C	TLC0831AIP TLC0831BIP	TLC0832AIP TLC0832BIP	TLC0831AIP TLC0831BIP	TLC0832AIP TLC0832BIP

functional block diagram



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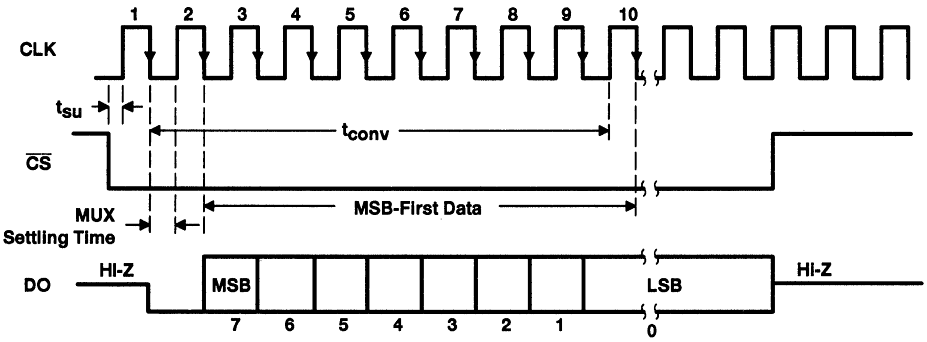
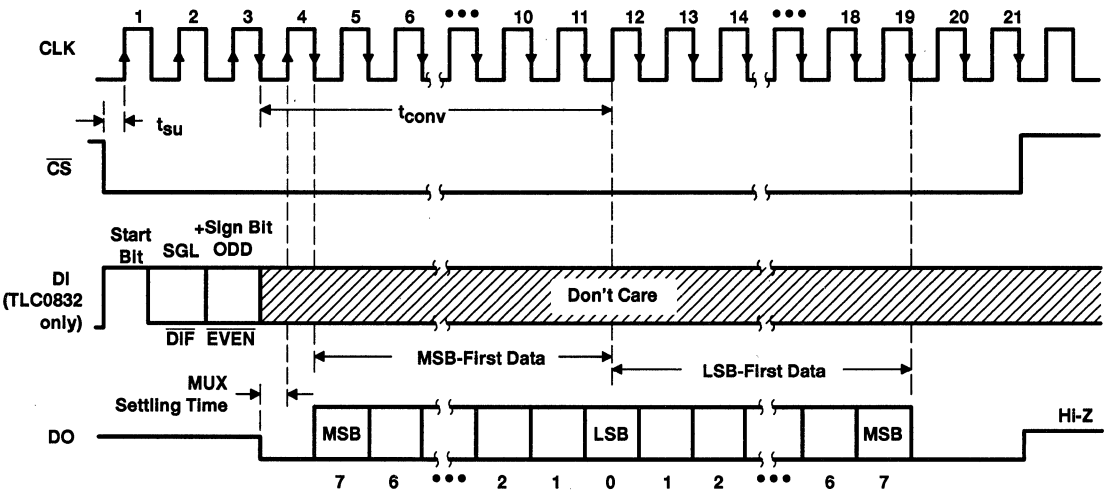
sequence of operation

TLC0831



TLC0832



PRODUCT PREVIEW

TLC0832 MUX-ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS		CHANNEL NUMBER	
SGL/$\overline{DIF}$	ODD/$\overline{EVEN}$	0	1
L	L	+	–
L	H	–	+
H	L	+	2
H	H		+

H = high level, L = low level,
– or + = polarity of selected input

PRODUCT PREVIEW

absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) .... 6.5 V
Input voltage range, V_I: Logic .... −0.3 V to V_{CC} + 0.3 V
Analog .... −0.3 V to V_{CC} + 0.3 V
Input current, I_I .... ±5 mA
Total input current .... ±20 mA
Operating free-air temperature range, T_A: C suffix .... 0°C to 70°C
I suffix .... −40°C to 85°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to the network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	6.3	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Clock frequency, f_{clock}		10		600	kHz
Clock duty cycle (see Note 2)		40%		60%	
Pulse duration, $\overline{CS}$ high, $t_{wH(CS)}$		220			ns
Setup time, $\overline{CS}$ low or TLC0832 data valid before CLK↑, t_{su}		350			ns
Hold time, TLC0832 data valid after CLK↑, t_h		90			ns
Operating free-air temperature, T_A	C suffix	0		70	°C
	I suffix	−40		85	

NOTE 2: The clock-duty-cycle range ensures proper operation at all clock frequencies. If a clock frequency is used outside the recommended duty-cycle range, the minimum pulse duration (high or low) is 1 μs.

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electrical characteristics over recommended range of operating free-air temperature, V_{CC} = 5 V, f_{clock} = 1 MHz (unless otherwise noted)

digital section

PARAMETER		TEST CONDITIONS†		C SUFFIX			I SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH}	High-level output voltage	V_{CC} = 4.75 V,	I_{OH} = −360 µA	2.8			2.4			V
		V_{CC} = 4.75 V,	I_{OH} = −10 µA	4.6			4.5			
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V,	I_{OL} = 1.6 mA	0.34			0.4			V
I_{IH}	High-level input current	V_{IH} = 5 V			0.005	1		0.005	1	µA
I_{IL}	Low-level input current	V_{IL} = 0			−0.005	−1		−0.005	−1	µA
I_{OH}	High-level output (source) current	V_{OH} = V_O,	T_A = 25°C	−6.5	−14		−6.5	−14		mA
I_{OL}	Low-level output (sink) current	V_{OL} = V_{CC},	T_A = 25°C	8	16		8	16		mA
I_{OZ}	High-impedance-state output current (DO)	V_O = 5 V,	T_A = 25°C		0.01	3		0.01	3	µA
		V_O = 0,	T_A = 25°C		−0.01	−3		−0.01	−3	
C_i	Input capacitance				5			5		pF
C_o	Output capacitance				5			5		pF

† All parameters are measured under open-loop conditions with zero common-mode input voltage.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

analog and converter section

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{ICR}	Common-mode input voltage		See Note 3	−0.05 to V_{CC}+0.05			V
$I_{I(stdby)}$	Standby-input current (see Note 4)	On channel	V_I = 5 V			1	µA
		Off channel	V_I = 0			−1	
		On channel	V_I = 0			−1	
		Off channel	V_I = 5 V			1	
$r_{i(REF)}$	Input resistance to REF			1.3	2.4	5.9	kΩ

† All parameters are measured under open-loop conditions with zero common-mode input voltage.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 3. If channel IN– is more positive than channel IN+, the digital output code will be 0000 0000. Connected to each analog input are two on-chip diodes that conduct forward current for analog input voltages one diode drop above V_{CC} .Care must be taken during testing at low V_{CC} levels (4.5 V) because high-level analog input voltage (5 V) can, especially at high temperatures, cause this input diode to conduct and cause errors for analog inputs that are near full scale. As long as the analog voltage does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 to 5-V input voltage range requires a minimum V_{CC} of 4.95 V for all variations of temperature and load.

4. Standby-input currents are currents going into or out of the on or off channels when the A/D converter is not performing conversion and the clock is in a high or low steady-state conditions.

total device

PARAMETER			MIN	TYP‡	MAX	UNIT
I_{CC}	Supply current	TLC0831		1	2.5	mA
		TLC0832		3	5.2	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

PRODUCT PREVIEW

operating characteristics $V_{CC} = V_{ref} = 5$ V, $f_{clock} = 1$ MHz, $t_r = t_f = 20$ ns, $T_A = 25°C$ (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	AI, AC SUFFIX			BI, BC SUFFIX			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
	Supply-voltage variation error		V_{CC} = 4.75 V to 5.25 V		±1/16	±1/4		±1/16	±1/4	LSB
	Total unadjusted error (see Note 5)		V_{ref} = 5 V, T_A = MIN to MAX			±1			±1/2	LSB
	Common-mode error		Differential mode		±1/16	±1/4		±1/16	±1/4	LSB
t_{pd}	Propagation delay time, output data after CLK↑ (see Note 6)	MSB-first data	C_L = 100 pF		650	1500		650	1500	ns
		LSB-first data			250	600		250	600	
t_{dis}	Output disable time, DO after $\overline{CS}$↑		C_L = 10 pF, R_L = 10 kΩ		125	250		125	250	ns
			C_L = 100 pF, R_L = 2 kΩ			500			500	
t_{conv}	Conversion time (multiplexer-addressing time not included)					8			8	clock periods

† All parameters are measured under open-loop conditions with zero common-mode input voltage. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 5. Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.
6. The MSB-first data is output directly from the comparator and therefore requires additional delay to allow for comparator response time. LBS-first data applies only to TLC0832.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

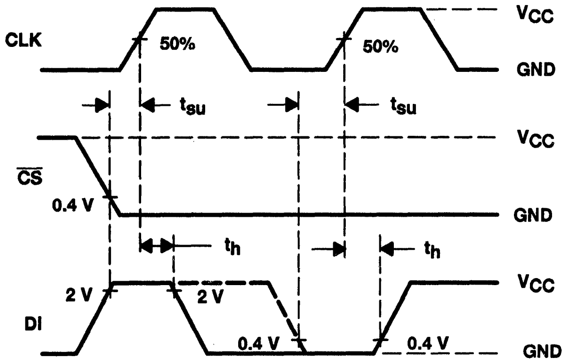


Figure 1. TLC0832 Data-Input Timing

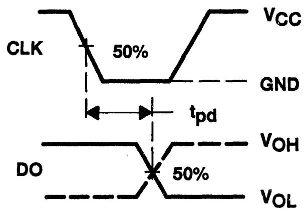
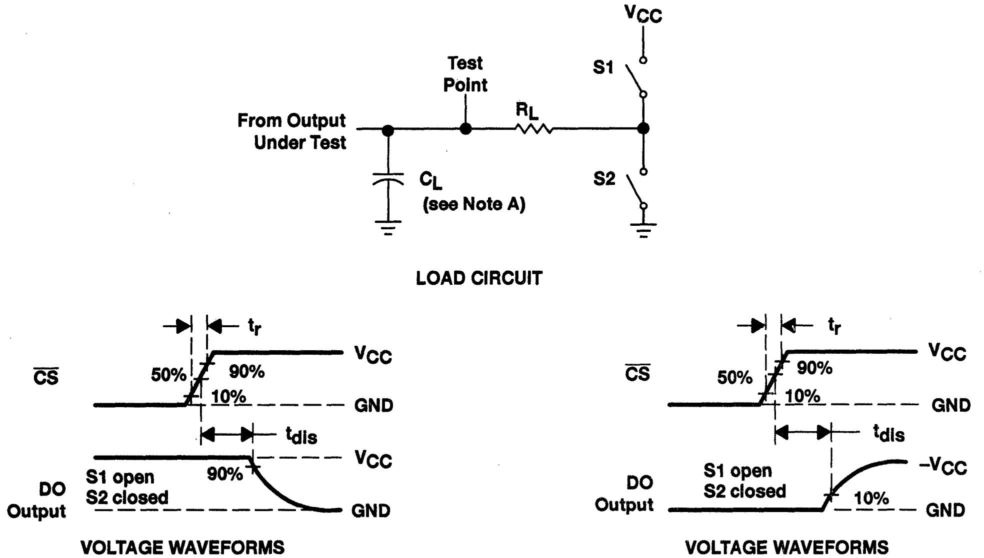


Figure 2. Data-Output Timing



NOTE A: C_L includes probe and jig capacitance.

Figure 3. Output Disable Time Test Circuit and Voltage Waveforms

PRODUCT PREVIEW

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

UNADJUSTED OFFSET ERROR vs REFERENCE VOLTAGE

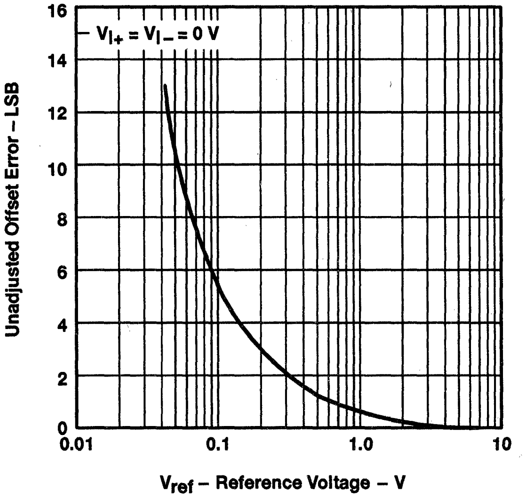


Figure 4

LINEARITY ERROR vs REFERENCE VOLTAGE

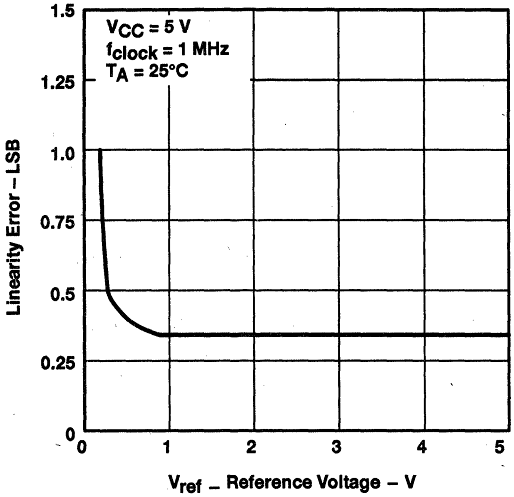


Figure 5

LINEARITY ERROR vs FREE-AIR TEMPERATURE

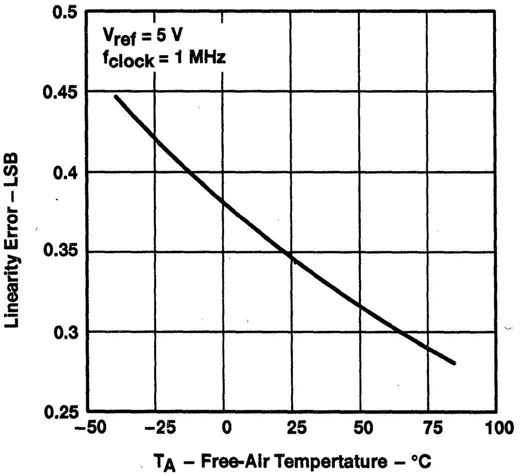


Figure 6

LINEARITY ERROR vs CLOCK FREQUENCY

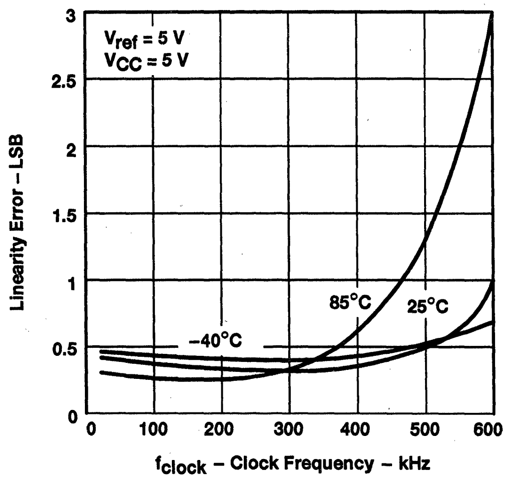


Figure 7

TYPICAL CHARACTERISTICS

TLC0831
SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

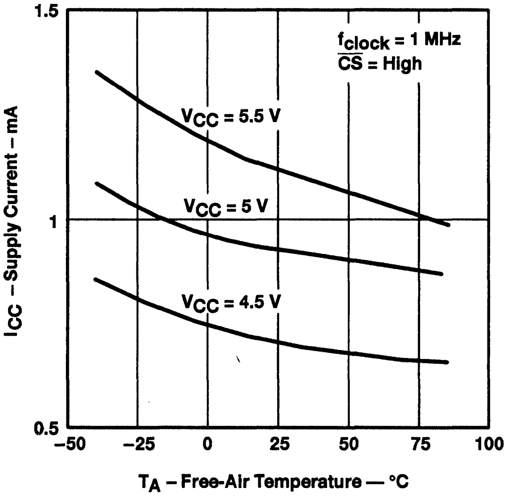


Figure 8

TLC0831
SUPPLY CURRENT
vs
CLOCK FREQUENCY

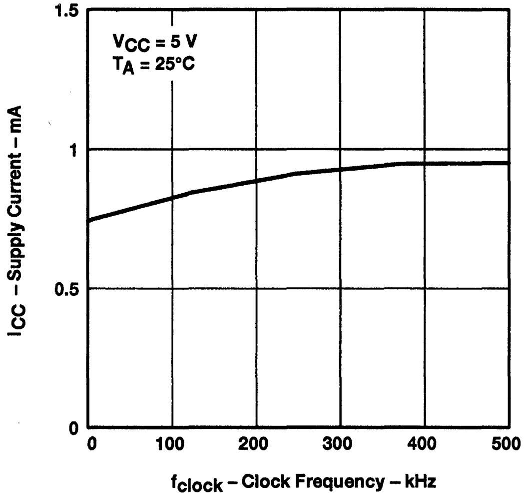


Figure 9

OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

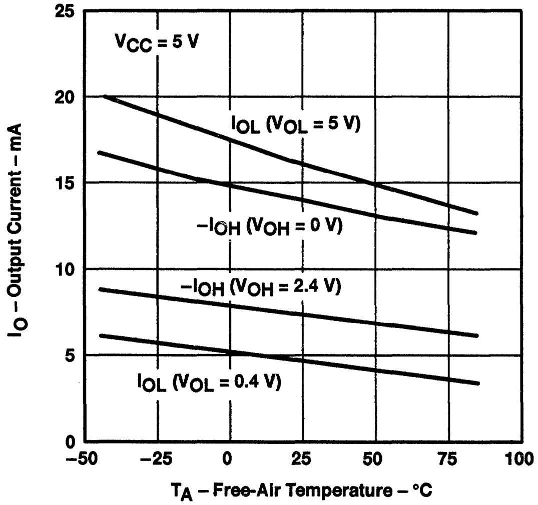


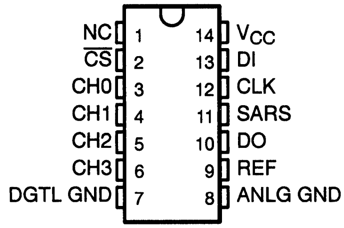
Figure 10

PRODUCT PREVIEW

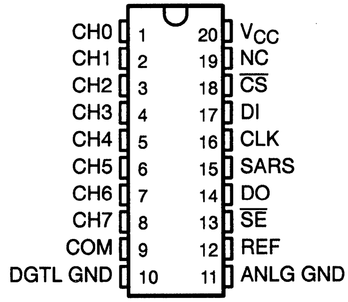
- **8-Bit Resolution**
- **Easy Microprocessor Interface or Stand-Alone Operation**
- **Operates Ratiometrically or With 5-V Reference**
- **4- or 8-Channel Multiplexer Options With Address Logic**
- **Input Range 0 to 5 V With Single 5-V Supply**
- **Remote Operation With Serial Data Link**
- **Inputs and Outputs Are Compatible With TTL and MOS**
- **Conversion Time of 32 μs at f_{CLK} = 250 kHz**
- **Functionally Equivalent to the ADC0834 and ADC0838 Without the Internal Zener Regulator Network**

DEVICE	TOTAL UNADJUSTED ERROR	
	A-SUFFIX	B-SUFFIX
TLC0834	±1 LSB	±1/2 LSB
TLC0838	±1 LSB	±1/2 LSB

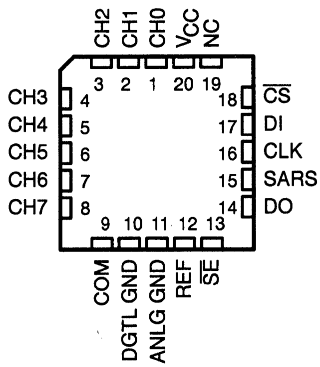
**TLC0834 . . . D OR N PACKAGE
(TOP VIEW)**



**TLC0838 . . . DW OR N PACKAGE
(TOP VIEW)**



**TLC0838 . . . FN PACKAGE
(TOP VIEW)**



description

These devices are 8-bit successive-approximation analog-to-digital converters, each with an input-configurable multichannel multiplexer and serial input/output. The serial input/output is configured to interface with standard shift registers or microprocessors. Detailed information on interfacing with most popular microprocessors is readily available from the factory.

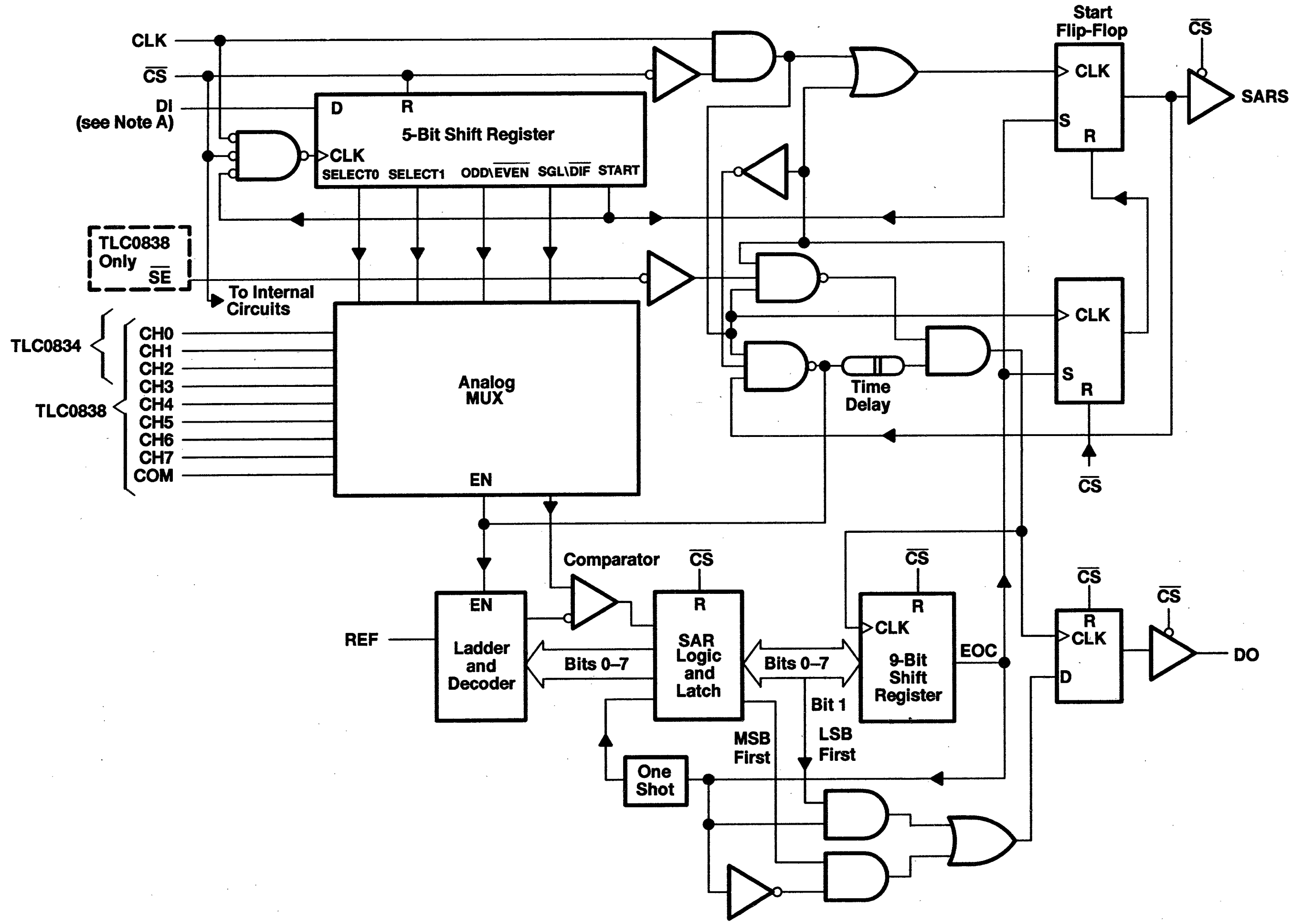
PRODUCT PREVIEW

AVAILABLE OPTIONS

T_A	PACKAGE			
	SMALL OUTLINE (D)	SMALL OUTLINE (DW)	PLASTIC DIP (N)	CHIP CARRIER (FN)
0°C to 70°C	TLC0834ACD TLC0834BCD	TLC0838ACDW TLC0838BCDW	TLC0834ACN TLC0838ACN TLC0834BCN TLC0838BCN	TLC0838ACFN TLC0838BCFN
−40°C to 85°C	TLC0834AID TLC0834BID	TLC0838AIDW TLC0838BIDW	TLC0834AIN TLC0838AIN TLC0834BIN TLC0838BIN	TLC0838AIFN TLC0838BIFN

PRODUCT PREVIEW

functional block diagram



NOTE A: For the TLC0834, DI is input directly to the D input of SELECT1; SELECT0 is forced to a high.

description (continued)

The TLC0834 (4-channel) and TLC0838 (8-channel) multiplexer is software configured for single-ended or differential inputs as well as pseudo-differential input assignments. The differential analog voltage input allows for common-mode rejection or offset of the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

The TLC0834AC, TLC0834BC and TLC0838AC, TLC0838BC are characterized for operation from 0°C to 70°C. The TLC0834AI, TLC0834BI, and TLC0838AI, TLC0838BI are characterized for operation from −40°C to 85°C.

functional description

The TLC0834 and TLC0838 use a sample-data-comparator structure that converts differential analog inputs by a successive-approximation routine. Operation of both devices is similar with the exception of $\overline{SE}$, an analog common input, and multiplexer addressing. The input voltage to be converted is applied to a channel terminal and is compared to ground (single ended), to an adjacent input (differential), or to a common terminal (pseudo differential) that can be an arbitrary voltage. The input terminals are assigned a positive (+) or negative (–) polarity. If the signal input applied to the assigned positive terminal is less than the signal on the negative terminal, the converter output is all zeros.

Channel selection and input configuration are under software control using a serial-data link from the controlling processor. A serial-communication format allows more functions to be included in a converter package with no increase in size. In addition, it eliminates the transmission of low-level analog signals by locating the converter at the analog sensor and communicating serially with the controlling processor. This process returns noise-free digital data to the processor.

A particular input configuration is assigned during the multiplexer-addressing sequence. The multiplexer address is shifted into the converter through the data input (DI) line. The multiplexer address selects the analog inputs to be enabled and determines whether the input is single ended or differential. When the input is differential, the polarity of the channel input is assigned. Differential inputs are assigned to adjacent channel pairs . For example, channel 0 and channel 1 may be selected as a differential pair. These channels cannot act differentially with any other channel. In addition to selecting the differential mode, the polarity may also be selected. Either channel of the channel pair may be designated as the negative or positive input.

The common input on the TLC0838 can be used for a pseudo-differential input. In this mode, the voltage on the common input is considered to be the negative differential input for all channel inputs. This voltage can be any reference potential common to all channel inputs. Each channel input can then be selected as the positive differential input. This feature is useful when all analog circuits are biased to a potential other than ground.

A conversion is initiated by setting $\overline{CS}$ low, which enables all logic circuits. $\overline{CS}$ must be held low for the complete conversion process. A clock input is then received from the processor. On each low-to-high transition of the clock input, the data on DI is clocked into the multiplexer-address shift register. The first logic high on the input is the start bit. A 3- to 4-bit assignment word follows the start bit. On each successive low-to-high transition of the clock input, the start bit and assignment word are shifted through the shift register. When the start bit is shifted into the start location of the multiplexer register, the input channel is selected and conversion starts. The SAR status output (SARS) goes high to indicate that a conversion is in progress, and DI to the multiplexer shift register is disabled the duration of the conversion.

An interval of one clock period is automatically inserted to allow the selected multiplexed channel to settle. DO comes out of the high-impedance state and provides a leading low for this one clock period of multiplexer settling time. The SAR comparator compares successive outputs from the resistive ladder with the incoming analog signal. The comparator output indicates whether the analog input is greater than or less than the resistive-ladder output. As the conversion proceeds, conversion data is simultaneously output from DO, with the most significant bit (MSB) first. After eight clock periods, the conversion is complete and SARS goes low.

PRODUCT PREVIEW

functional description (continued)

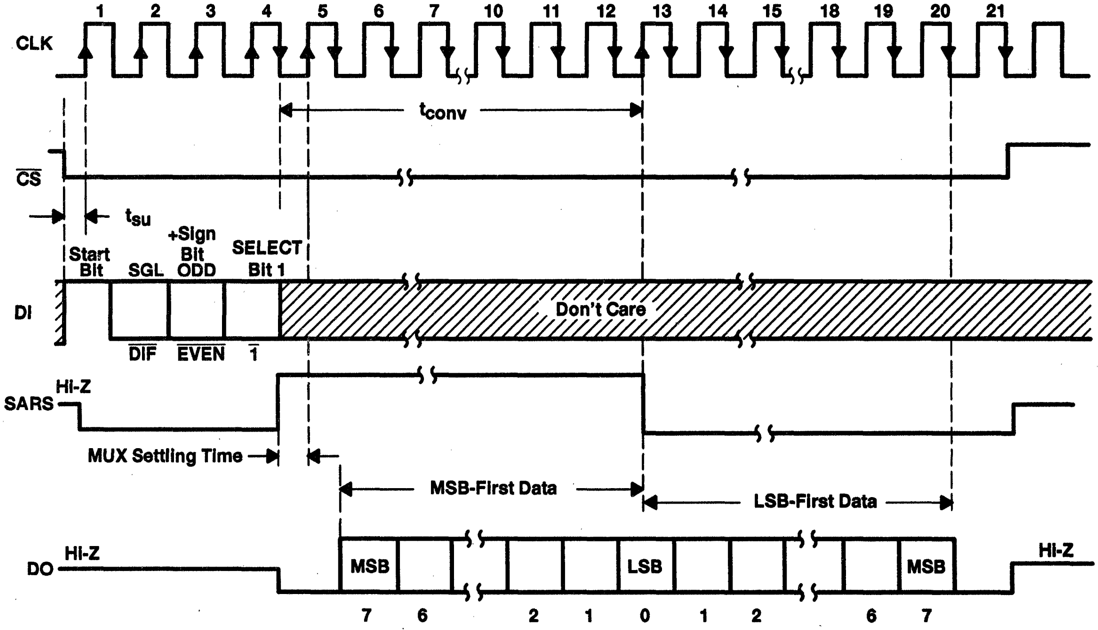
The TLC0834 outputs the least-significant-bit (LSB) first data after the MSB-first data stream. If $\overline{SE}$ is held high on the TLC0838, the value of the LSB remains on the data line. When $\overline{SE}$ is forced low, the data is then clocked out as LSB-first data. (To output LSB first, $\overline{SE}$ must first go low, then the data stored in the 9-bit shift register outputs LSB first.) When $\overline{CS}$ goes high, all internal registers are cleared. At this time, the output circuits go to the high-impedance state. If another conversion is desired, $\overline{CS}$ must make a high-to-low transition followed by address information.

DI and DO can be tied together and controlled by a bidirectional processor I/O bit received on a single wire. This is possible because DI is only examined during the multiplexer-addressing interval and DO is still in the high-impedance state.

Detailed information on interfacing to most popular microprocessors is readily available from the factory.

sequence of operation

TLC0834



PRODUCT PREVIEW

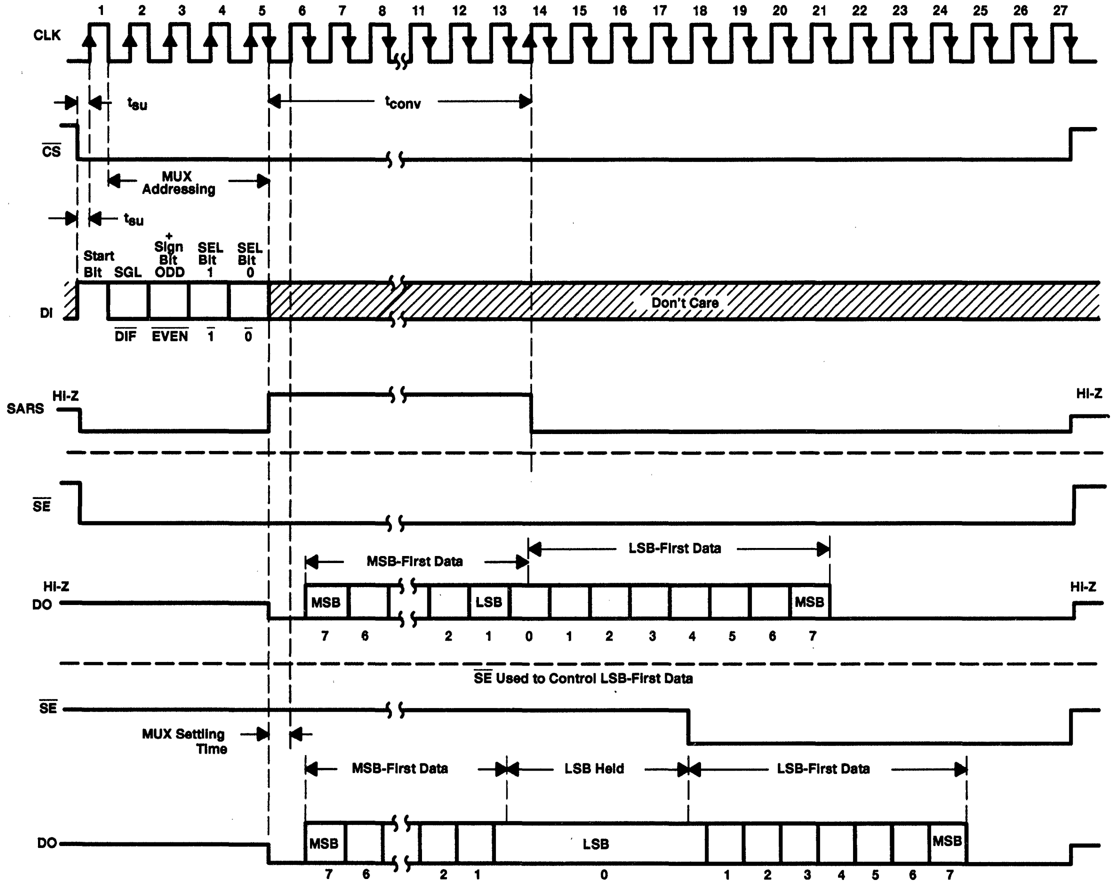
TLC0834 MUX-ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS			CHANNEL NUMBER			
SGL/$\overline{DIF}$	ODD/$\overline{EVEN}$	SELECT BIT 1	0	1	2	3
L	L	L	+	–		
L	L	H			+	–
L	H	L	–	+		
L	H	H			–	+
H	L	L	+			
H	L	H			+	
H	H	L		+		
H	H	H				+

H = high level, L = low level, – or + = polarity of selected input

sequence of operation

TLC0838



PRODUCT PREVIEW

PRODUCT PREVIEW

TLC0838 MUX-ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS				SELECTED CHANNEL NUMBER								
SGL/$\overline{DIF}$	ODD/$\overline{EVEN}$	SELECT		0		1		2		3		COM
		1	0	0	1	2	3	4	5	6	7	
L	L	L	L	+	–							
L	L	L	H			+	–					
L	L	H	L					+	–			
L	L	H	H							+	–	
L	H	L	L	–	+							
L	H	L	H			–	+					
L	H	H	L					–	+			
L	H	H	H							–	+	
H	L	L	L	+								–
H	L	L	H			+						–
H	L	H	L					+				–
H	L	H	H							+		–
H	H	L	L		+							–
H	H	L	H				+					–
H	H	H	L						+			–
H	H	H	H								+	–

H = high level, L = low level, – or + = polarity of selected input

absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) .... 6.5 V
Input voltage range: Logic .... –0.3 V to V_{CC} + 0.3 V
Analog .... –0.3 V to V_{CC}+ 0.3 V
Input current, I_I .... ±5 mA
Total input current .... ±20 mA
Operating free-air temperature range, T_A: C suffix .... 0°C to 70°C
I suffix .... –40°C to 85°C
Storage temperature range, T_{stg} .... –65°C to 150°C
Case temperature for 10 seconds, T_C: FN package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to the network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	6.3	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Clock frequency, f_{clock}		10		600	kHz
Clock duty cycle (see Note 2)		40%		60%	
Pulse duration, $\overline{CS}$ high, $t_{wH(CS)}$		220			ns
Setup time, t_{su}	$\overline{CS}$ low, $\overline{SE}$ low, or data valid before clock↑	350			ns
Hold time, data valid after clock↑, t_h		90			ns
Operating free-air temperature, T_A	C suffix	0		70	°C
	I suffix	−40		85	

NOTE 2: The clock-duty-cycle range ensures proper operation at all clock frequencies. If a clock frequency is used outside the recommended duty-cycle range, the minimum pulse duration (high or low) is 1 µs.

electrical characteristics over recommended range of operating free-air temperature, V_{CC} = 5 V, f_{clock} = 250 kHz (unless otherwise noted)

digital section

PARAMETER		TEST CONDITIONS†	C SUFFIX			I SUFFIX			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, I_{OH} = −360 µA	2.8			2.4			V
		V_{CC} = 4.75 V, I_{OH} = −10 µA	4.6			4.5			
V_{OL}	Low-level output voltage	V_{CC} = 5.25 V, I_{OH} = 1.6 mA			0.34			0.4	V
I_{IH}	High-level input current	V_{IH} = 5 V		0.005	1		0.005	1	µA
I_{IL}	Low-level input current	V_{IL} = 0		−0.005	−1		−0.005	−1	µA
I_{OH}	High-level output (source) current	V_{OH} = 0, T_A = 25°C	−6.5	−14		−6.5	−14		mA
I_{OL}	Low-level output (sink) current	V_{OL} = V_{CC}, T_A = 25°C	8	16		8	16		mA
I_{OZ}	High-impedance-state output current (DO or SARS)	V_O = 5 V, T_A = 25°C		0.01	3		0.01	3	µA
		V_O = 0, T_A = 25°C		−0.01	−3		−0.01	−3	
C_i	Input capacitance						5		pF
C_o	Output capacitance						5		pF

† All parameters are measured under open-loop conditions with zero common-mode input voltage (unless otherwise specified).
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

PRODUCT PREVIEW

analog and converter section

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{ICR}	Common-mode input voltage		See Note 3	−0.05 to V_{CC}+0.05			V
$I_{I(stdby)}$	Standby-input current (see Note 4)	On channel	V_I = 5 V			1	µA
		Off channel	V_I = 0			−1	
		On channel	V_I = 0			−1	
		Off channel	V_I = 5 V			1	
$r_{i(REF)}$	Input resistance to REF			1.3	2.4	5.9	kΩ

total device

PARAMETER		MIN	TYP‡	MAX	UNIT
I_{CC}	Supply current		1	2.5	mA

† All parameters are measured under open-loop conditions with zero common-mode input voltage.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 3. If channel IN− is more positive than channel IN+, the digital output code will be 0000 0000. Connected to each analog input are two on-chip diodes that conduct forward current for analog input voltages one diode drop above V_{CC} .Care must be taken during testing at low V_{CC} levels (4.5 V) because high-level analog input voltage (5 V) can, especially at high temperatures, cause this input diode to conduct and cause errors for analog inputs that are near full scale. As long as the analog voltage does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 to 5-V input voltage range requires a minimum V_{CC} of 4.950 V for all variations of temperature and load.

4. Standby-input currents are currents going into or out of the on or off channels when the A/D converter is not performing conversion and the clock is in a high or low steady-state condition.

PRODUCT PREVIEW

operating characteristics, V_{CC} = 5 V, f_{clock} = 250 kHz, t_r = t_f = 20 ns, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	AI, AC SUFFIX			BI, BC SUFFIX			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
	Supply-voltage variation error		V_{CC} = 4.75 V to 5.25 V		±1/16	±1/4		±1/16	±1/4	LSB
	Total unadjusted error (see Note 5)		V_{ref} = 5 V, T_A = MIN to MAX			±1			±1/2	LSB
	Common-mode error		Differential mode		±1/16	±1/4		±1/16	±1/4	LSB
t_{pd}	Propagation delay time, output data after CLK↓ (see Note 6)	MSB-first data	C_L = 100pF			1500			1500	ns
		LSB-first data				600			600	
t_{dis}	Output disable time, DO or SARS after CS↑		C_L = 10 pF, R_L = 10 kΩ			250			250	ns
			C_L = 100 pF, R_L = 2 kΩ			500			500	
t_{conv}	Conversion time (multiplexer-addressing time not included)					8			8	clock periods

† All parameters are measured under open-loop conditions with zero common-mode input voltage. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 5. Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.
6. The MSB-first data is output directly from the comparator and therefore requires additional delay to allow for comparator response time.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

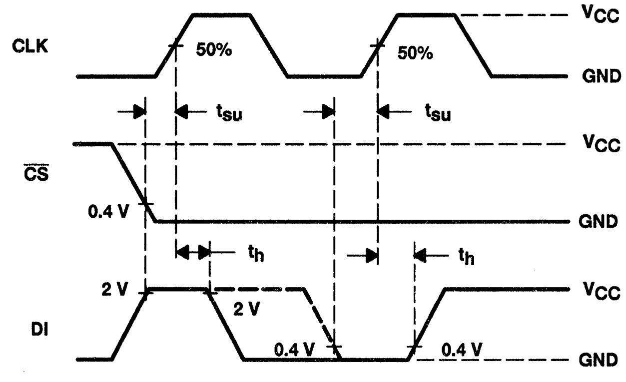


Figure 1. Data-Input Timing

PARAMETER MEASUREMENT INFORMATION

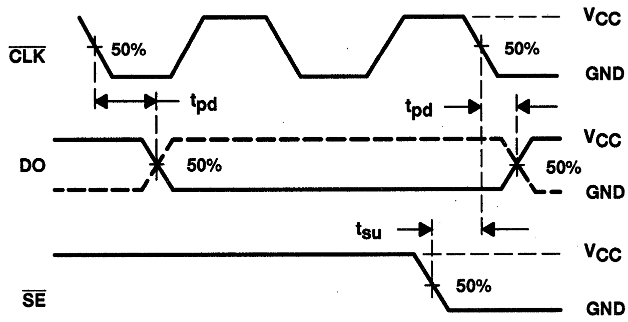
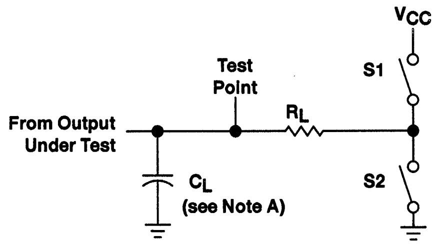
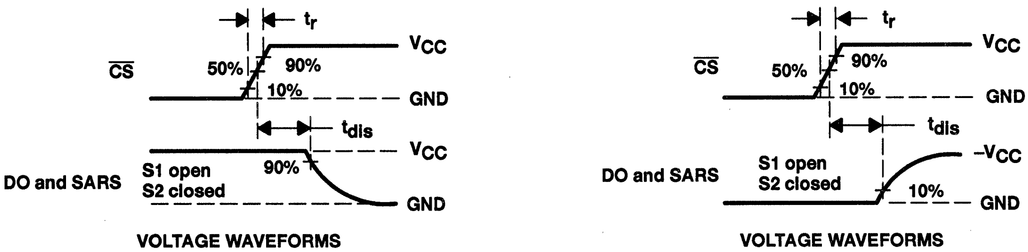


Figure 2. Data-Output Timing





NOTE A: C_L includes probe and jig capacitance.

Figure 3. Output Disable Time Test Circuit and Voltage Waveforms

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

UNADJUSTED OFFSET ERROR vs REFERENCE VOLTAGE

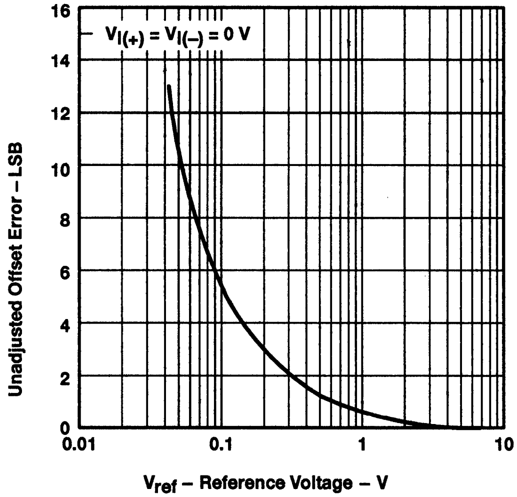


Figure 4

LINEARITY ERROR vs REFERENCE VOLTAGE

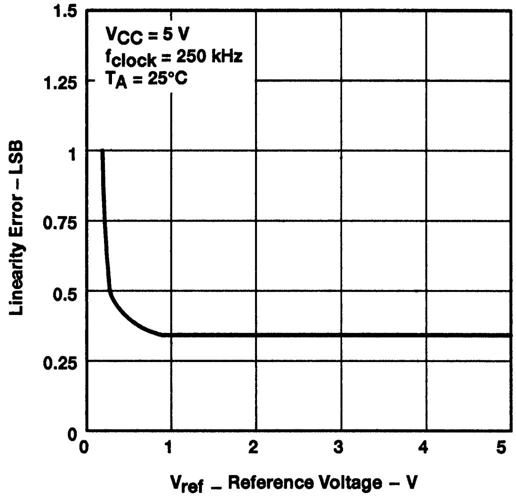


Figure 5

LINEARITY ERROR vs FREE-AIR TEMPERATURE

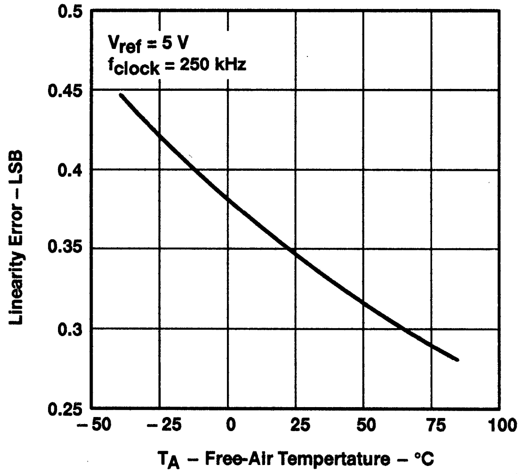


Figure 6

LINEARITY ERROR vs CLOCK FREQUENCY

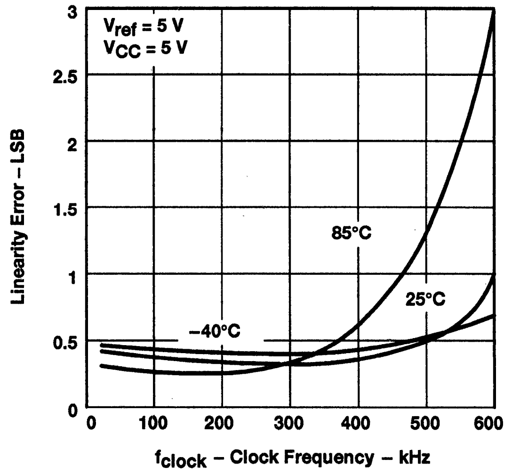


Figure 7

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

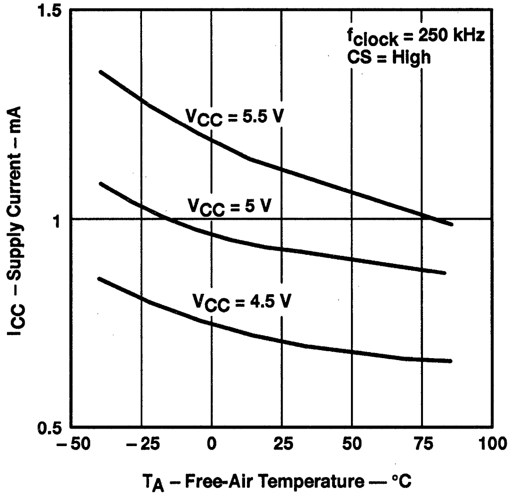


Figure 8

SUPPLY CURRENT vs CLOCK FREQUENCY

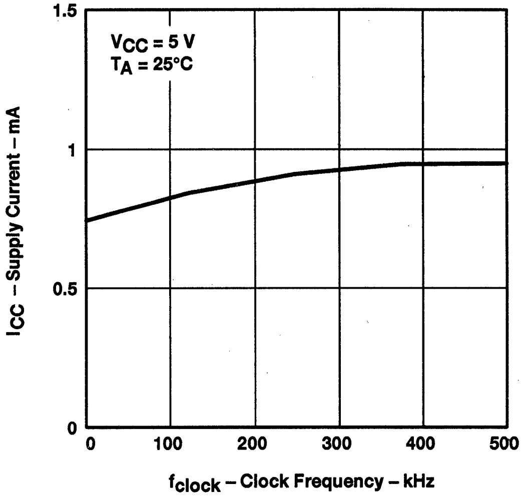


Figure 9

OUTPUT CURRENT vs FREE-AIR TEMPERATURE

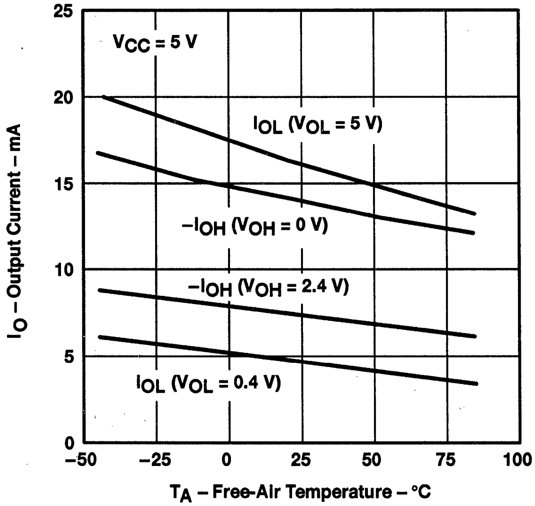


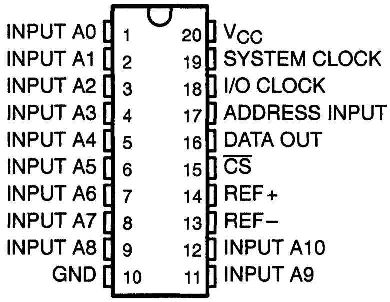
Figure 10

PRODUCT PREVIEW

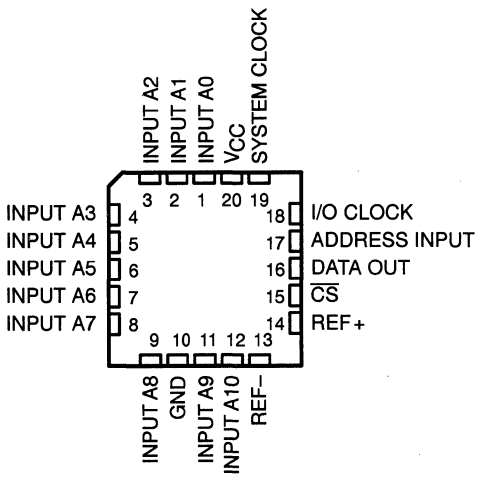
- **10-Bit Resolution A/D Converter**
- **Microprocessor Peripheral or Stand-Alone Operation**
- **On-Chip 12-Channel Analog Multiplexer**
- **Built-In Self-Test Mode**
- **Software-Controllable Sample and Hold**
- **Total Unadjusted Error**
  TLC1540: ±0.5 LSB Max
  TLC1541: ±1 LSB Max
- **Pinout and Control Signals Compatible With TLC540 and TLC549 Families of 8-Bit A/D Converters**
- **CMOS Technology**

PARAMETER	VALUE
Channel Acquisition Sample Time	5.5 µs
Conversion Time (Max)	21 µs
Samples Per Second (Max)	32×10^3
Power Dissipation (Max)	6 mW

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TLC1540 and TLC1541 are CMOS A/D converters built around a 10-bit, switched-capacitor, successive-approximation A/D converter. They are designed for serial interface to a microprocessor or peripheral via a 3-state output with up to four control inputs [including independent SYSTEM CLOCK, I/O CLOCK, chip select ($\overline{CS}$), and ADDRESS INPUT]. A 2.1-MHz system clock for the TLC1540 and TLC1541, with a design that includes simultaneous read/write operation, allows high-speed data transfers and sample rates of up to 32,258 samples per second. In addition to the high-speed converter and versatile control logic, there is an on-chip, 12-channel analog multiplexer that can be used to sample any one of 11 inputs or an internal self-test voltage and a sample and hold that can operate automatically or under microprocessor control. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

AVAILABLE OPTIONS

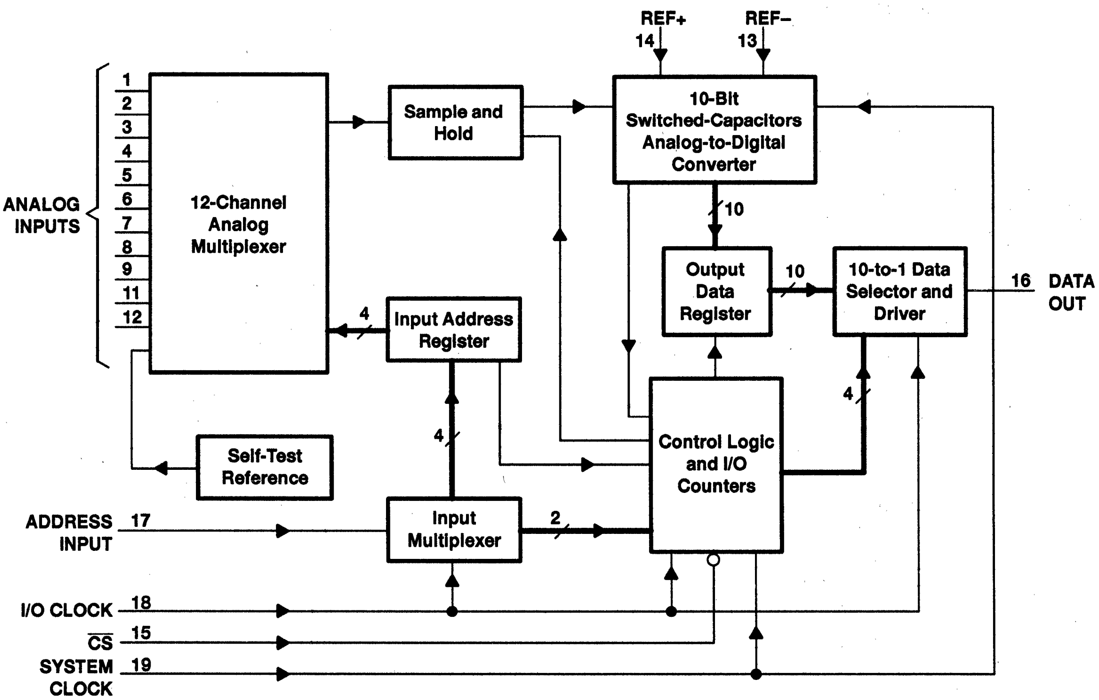
T_A	PACKAGE		
	PLASTIC DIP (DW)	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	TLC1540CDW TLC1541CDW	TLC1540CFN TLC1541CFN	TLC1540CN TLC1541CN

description (continued)

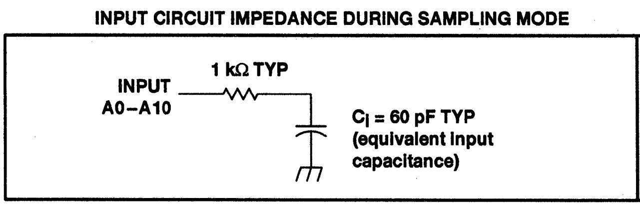
The converters incorporated in the TLC1540 and TLC1541 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A totally switched-capacitor design allows low-error conversion (±0.5 LSB for the TLC1540, ±1 LSB for the TLC1541) in 21 µs over the full operating temperature range.

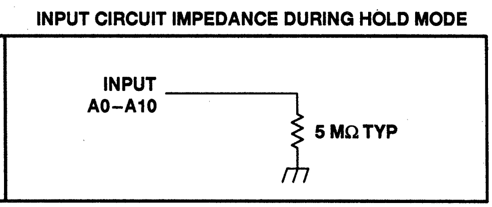
The TLC1540 and the TLC1541 are available in DW, FN, and N packages. The C-suffix versions are characterized for operation from 0°C to 70°C.

functional block diagram

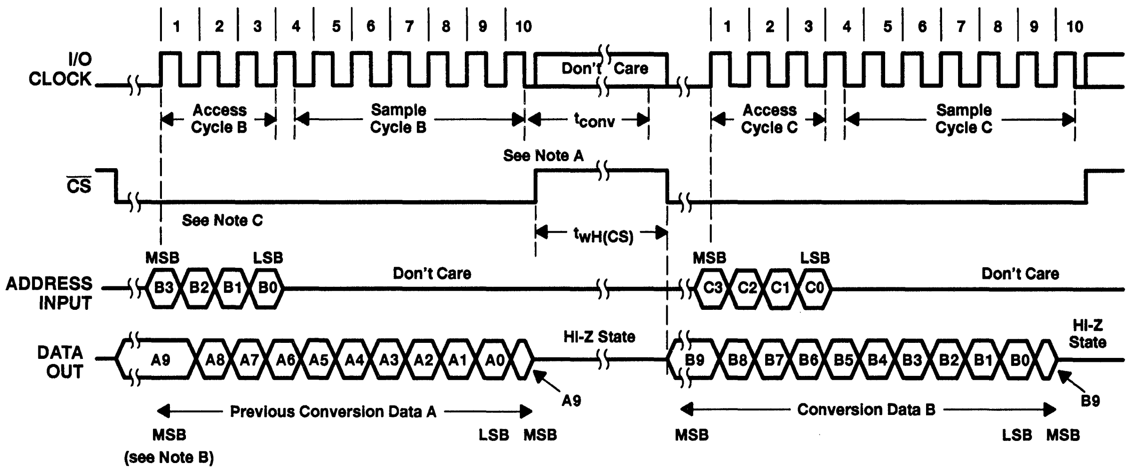


typical equivalent inputs





operating sequence



NOTES: A. The conversion cycle, which requires 44 system clock periods, initiates on the tenth falling edge of the I/O clock after $\overline{CS}$ goes low for the channel whose address exists in memory at that time. If $\overline{CS}$ is kept low during conversion, the I/O clock must remain low for at least 44 system clock cycles to allow the conversion to complete.

B. The most significant bit (MSB) is automatically placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining nine bits (A8–A0) clock out on the first nine I/O clock falling edges.

C. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for three system clock cycles (or less) after a chip-select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time elapses.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . 6.5 V
Input voltage range, V_I (any input) . . . . –0.3 V to V_{CC} + 0.3 V
Output voltage range, V_O . . . . –0.3 V to V_{CC} + 0.3 V
Peak input current (any input) . . . . ±10 mA
Peak total input current (all inputs) . . . . ±30 mA
Operating free-air temperature range, T_A: TLC1540C, TLC1541C . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Case temperature for 10 seconds, T_C: FN package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to digital ground with REF– and GND wired together (unless otherwise noted).

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			4.75	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)			2.5	V_{CC}	V_{CC}+0.1	V
Negative reference voltage, V_{ref-} (see Note 2)			−0.1	0	2.5	V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)			1	V_{CC}	V_{CC}+0.2	V
Analog input voltage (see Note 2)			0		V_{CC}	V
High-level control input voltage, V_{IH}			2			V
Low-level control input voltage, V_{IL}					0.8	V
Input/output clock frequency, $f_{clock(I/O)}$			0		1.1	MHz
System clock frequency, $f_{clock(SYS)}$			$f_{clock(I/O)}$		2.1	MHz
Setup time, address bits before I/O CLOCK↑, $t_{su(A)}$			400			ns
Hold time, address bits after I/O CLOCK↑, $t_{h(A)}$			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3)			3			System clock cycles
Pulse duration, $\overline{CS}$ high during conversion, $t_{wH(CS)}$			44			System clock cycles
Pulse duration, SYSTEM CLOCK high, $t_{wH(SYS)}$			210			ns
Pulse duration, SYSTEM CLOCK low, $t_{wL(SYS)}$			190			ns
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$			404			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$			404			ns
Clock transition time (see Note 4)	System	$f_{clock(SYS)} \le 1048$ kHz			30	ns
		$f_{clock(SYS)} > 1048$ kHz			20	
	I/O	$f_{clock(I/O)} \le 525$ kHz			100	ns
		$f_{clock(I/O)} > 525$ kHz			40	
Operating free-air temperature, T_A			0		70	°C

NOTES: 2. Analog input voltages greater than that applied to REF + convert as all ones (1111111111), while input voltages less than that applied to REF – convert as all zeros (0000000000). For proper operation, REF + voltage must be at least 1 V higher than REF – voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.

3. To minimize errors caused by noise at the chip select input, the internal circuitry waits for three system clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum chip select setup time elapses.

4. The amount of time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating temperature range, $V_{CC} = V_{ref+} = 4.75$ V to 5.5 V (unless otherwise noted), $f_{clock(I/O)} = 1.1$ MHz, $f_{clock(SYS)} = 2.1$ MHz

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (terminal 16)		$V_{CC} = 4.75$ V,	$I_{OH} = 360$ µA	2.4			V
V_{OL}	Low-level output voltage		$V_{CC} = 4.75$ V,	$I_{OL} = 3.2$ mA			0.4	V
I_{OZ}	High-impedance-state output current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}			10	µA
			$V_O = 0$,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		$V_I = V_{CC}$			0.005	2.5	µA
I_{IL}	Low-level input current		$V_I = 0$			−0.005	−2.5	µA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.2	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V			0.4	1	µA
			Selected channel at 0 V, Unselected channel at V_{CC}			−0.4	−1	
$I_{CC} + I_{ref}$	Supply and reference current		$V_{ref+} = V_{CC}$,	$\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

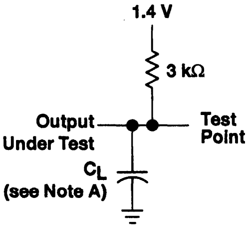
† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

operating characteristics over recommended operating temperature range, $V_{CC} = V_{ref+} = 4.75$ V to 5.5 V, $f_{clock(I/O)} = 1.1$ MHz, $f_{clock(SYS)} = 2.1$ MHz

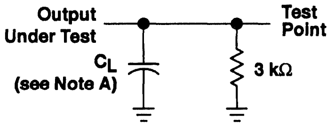
PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
E_L	Linearity error	TLC1540	See Note 5		±0.5	LSB
		TLC1541			±1	
E_{ZS}	Zero-scale error	TLC1540	See Notes 2 and 6		±0.5	LSB
		TLC1541			±1	
E_{FS}	Full-scale error	TLC1540	See Notes 2 and 6		±0.5	LSB
		TLC1541			±1	
E_T	Total unadjusted error	TLC1540	See Note 7		±0.5	LSB
		TLC1541			±1	
	Self-test output code		Input A11 address = 1011 (see Note 8)	0111110100 (500)	1000001100 (524)	
t_{conv}	Conversion time		See Operating Sequence		21	µs
	Total access and conversion time		See Operating Sequence		31	µs
t_{acq}	Channel acquisition time (sample cycle)		See Operating Sequence		6	I/O clock cycles
t_v	Time output data remains valid after I/O CLOCK↓			10		ns
t_d	Delay time, I/O CLOCK↓ to DATA OUT valid		See Parameter Measurement Information		400	ns
t_{en}	Output enable time				150	ns
t_{dis}	Output disable time				150	ns
$t_{r(bus)}$	Data bus rise time				300	ns
$t_{f(bus)}$	Data bus fall time				300	ns

NOTES: 2. Analog input voltages greater than that applied to REF + convert as all ones (1111111111), while input voltages less than that applied to REF – convert as all zeros (0000000000). For proper operation, REF + voltage must be at least 1 V higher than REF – voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.
5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero-scale error is the difference between 0000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.
7. Total unadjusted error includes linearity, zero-scale, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic. The A11 analog input signal is internally generated and used for test purposes.

PARAMETER MEASUREMENT INFORMATION

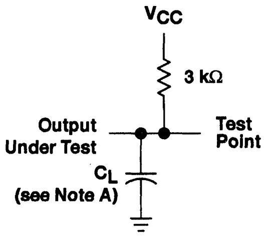


LOAD CIRCUIT FOR t_d, t_r, AND t_f



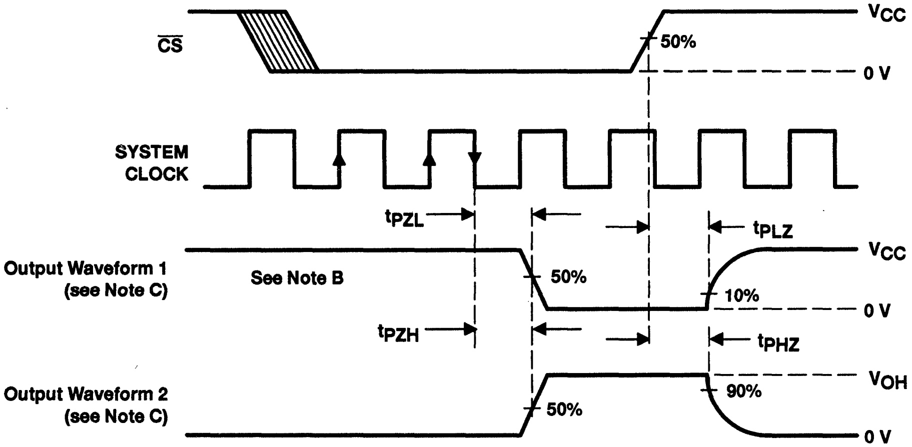
See Note B

LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}

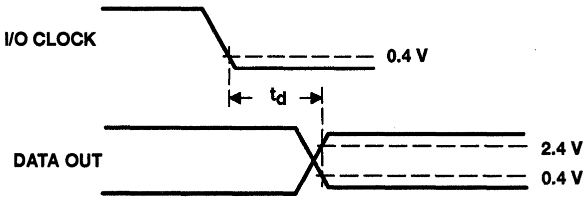


See Note B

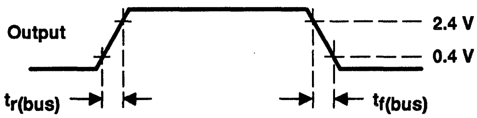
LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS FOR DELAY TIME



VOLTAGE WAVEFORMS FOR RISE AND FALL TIMES

NOTES: A. $C_L = 50$ pF
B. $t_{en} = t_{PZH}$ or t_{PZL} and $t_{dis} = t_{PHZ}$ or t_{PLZ}.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

APPLICATION INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 1, the time required to charge the analog input capacitance from 0 V to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c/R_t C_i}\right) \quad (1)$$

where

$$R_t = R_s + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C\ (1/2\ \text{LSB}) = V_S - (V_S/2048) \quad (2)$$

Equating equation 1 to equation 2 and solving for time (t_c) gives

$$V_S - (V_S/2048) = V_S \left(1 - e^{-t_c/R_t C_i}\right) \quad (3)$$

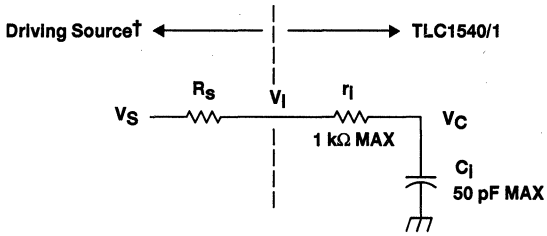
and

$$t_c\ (1/2\ \text{LSB}) = R_t \times C_i \times \ln(2048) \quad (4)$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c\ (1/2\ \text{LSB}) = (R_s + 1\ \text{k}\Omega) \times 60\ \text{pF} \times \ln(2048) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at INPUT A0–A10
V_S = External Driving Source Voltage
R_s = Source Resistance
r_I = Input Resistance
C_I = Input Capacitance

† Driving source requirements:
- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_s must be real at the input frequency.

Figure 1. Equivalent Input Circuit Including the Driving Source

PRINCIPLES OF OPERATION

The TLC1540 and TLC1541 are complete data acquisition systems on single chips. Each includes such functions as sample and hold, 10-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs: chip select ($\overline{CS}$), address input, I/O clock, and system clock. These control inputs and a TTL-compatible, 3-state output are intended for serial communications with a microprocessor or microcomputer. The TLC1540 and TLC1541 can complete conversions in a maximum of 21 µs, while complete input-conversion-output cycles can be repeated at a maximum of 31 µs.

The system and I/O clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to the SYSTEM CLOCK input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using I/O CLOCK. SYSTEM CLOCK will drive the conversion-crunching circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, DATA OUT is in a 3-state condition and ADDRESS INPUT and I/O CLOCK are disabled. This feature allows each of these terminals, with the exception of the $\overline{CS}$ terminal, to share a control logic point with its counterpart terminals on additional A/D devices when using additional TLC1540/1541 devices. In this way, the above feature serves to minimize the required control logic terminals when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of SYSTEM CLOCK after a low $\overline{CS}$ transition before recognizing the low transition. This technique protects the device against noise when the device is used in a noisy environment. The MSB of the previous conversion result automatically appears on DATA OUT.
2. A new positive-logic multiplexer address shifts in on the first four rising edges of I/O CLOCK. The MSB of the address shifts in first. The negative edges of these four I/O clock pulses shift out the second, third, fourth, and fifth most-significant bits of the previous conversion result. The on-chip sample-and-hold begins sampling the newly addressed analog input after the fourth falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Five clock cycles are then applied to the I/O CLOCK, and the sixth, seventh, eighth, ninth, and tenth conversion bits shift out on the negative edges of these clock cycles.
4. The final tenth-clock cycle is applied to the I/O CLOCK. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 44 system clock cycles. After this final I/O clock cycle, $\overline{CS}$ must go high or the I/O CLOCK must remain low for at least 44 system-clock cycles to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on I/O CLOCK. If glitches occur on I/O CLOCK, the I/O sequence between the microprocessor/controller and the device loses synchronization. Also, if $\overline{CS}$ goes high, it must remain high until the end of the conversion. Otherwise, a valid falling edge of $\overline{CS}$ causes a reset condition, which aborts the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 44 system-clock cycles occur. Such action yields the conversion result of the previous conversion and not the ongoing conversion.

PRINCIPLES OF OPERATION

It is possible to connect SYSTEM CLOCK and I/O CLOCK together in special situations in which controlling-circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

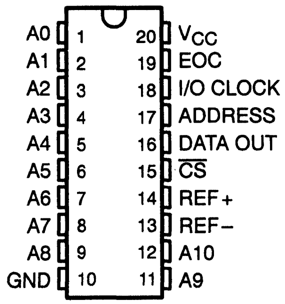
1. This device requires the first two clocks to recognize that $\overline{CS}$ is at a valid low level when the common clock signal is used as an I/O CLOCK. When $\overline{CS}$ is recognized by the device to be at a high level, the common clock signal is used for the conversion clock also.
2. A low $\overline{CS}$ must be recognized before the I/O CLOCK can shift in an analog channel address. The device recognizes a $\overline{CS}$ transition when the SYSTEM CLOCK terminal receives two positive edges and then a negative edge. For this reason, after a $\overline{CS}$ negative edge, the first two clock cycles do not shift in the address. Also, upon shifting in the address, $\overline{CS}$ must be raised after the tenth valid (12 total) I/O CLOCK. Otherwise, additional common-clock cycles are recognized as I/O CLOCK cycles and shift in an erroneous address.

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device accommodates these applications. Although the on-chip sample-and-hold begins sampling upon the negative edge of the fourth valid I/O CLOCK cycle, the hold function does not initiate until the negative edge of the eighth valid I/O CLOCK cycle. Thus, the control circuitry can leave the I/O CLOCK signal in its high state during the tenth valid I/O CLOCK cycle until the moment at which the analog signal must be converted. The TLC1540/TLC1541 continues sampling the analog input until the eighth valid falling edge of the I/O CLOCK. The control circuitry or software then immediately lowers the I/O CLOCK signal and holds the analog signal at the desired point in time and starts the conversion.

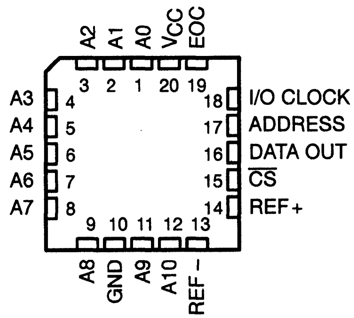
Detailed information on interfacing to most popular microprocessors is readily available from the factory.

- **10-Bit-Resolution A/D Converter**
- **11 Analog Input Channels**
- **Three Built-In Self-Test Modes**
- **Inherent Sample and Hold**
- **Total Unadjusted Error . . . ±1 LSB Max**
- **On-Chip System Clock**
- **End-of-Conversion (EOC) Output**
- **Terminal Compatible With TLC1542**
- **CMOS Technology**

DB, J, DW, OR N PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



description

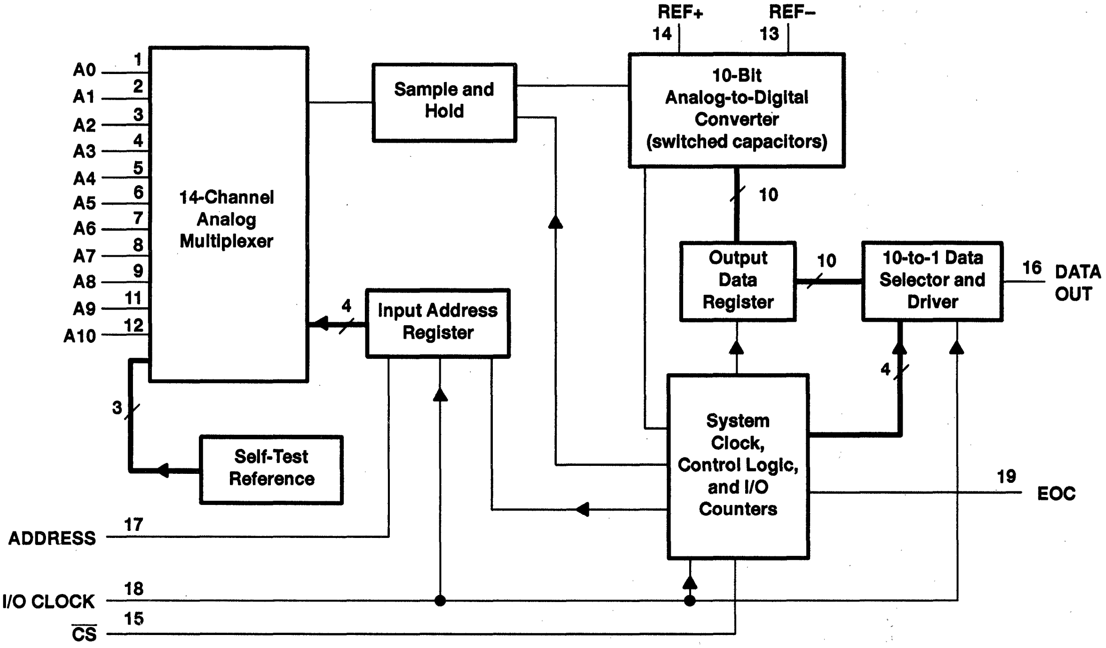
The TLC1543C, TLC1543I, and TLC1543Q are CMOS 10-bit, switched-capacitor, successive-approximation, analog-to-digital converters. These devices have three inputs and a 3-state output [chip select ($\overline{CS}$), input-output clock (I/O CLOCK), address input (ADDRESS), and data output (DATA OUT)] that provide a direct four-wire interface to the serial port of a host processor. These devices allow high-speed data transfers from the host.

In addition to a high-speed A/D converter and versatile control capability, these devices have anon-chip 14-channel multiplexer that can select any one of 11 analog inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of A/D conversion, the end-of-conversion (EOC) output goes high to indicate that conversion is complete. The converter incorporated in the devices features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating free-air temperature range.

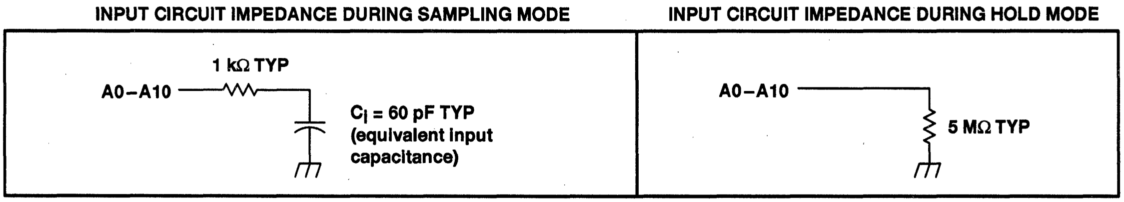
AVAILABLE OPTIONS

T_A	PACKAGE					
	SMALL OUTLINE (DB)	SMALL OUTLINE (DW)	CHIP CARRIER (FN)	PLASTIC DIP (N)	CHIP CARRIER (FK)	CERAMIC DIP (J)
0°C to 70°C		TLC1542CDW	TLC1542CFN	TLC1542CN		
	TLC1543CDB	TLC1543CDW	TLC1543CFN	TLC1543CN		
−40°C to 85°C		TLC1542IDW	TLC1542IFN	TLC1542IN		
		TLC1543IDW	TLC1543IFN	TLC1543IN		
−40°C to 125°C		TLC1542QDW	TLC1542QFN	TLC1542QN		
		TLC1543QDW	TLC1543QFN	TLC1543QN		
−55°C to 125°C					TLC1542MFK	TLC1542MJ

functional block diagram



typical equivalent inputs



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADDRESS	17	I	Serial address input. A 4-bit serial address selects the desired analog input or test voltage that is to be converted next. The address data is presented with the MSB first and is shifted in on the first four rising edges of I/O CLOCK. After the four address bits have been read into the address register, this input is ignored for the remainder of the current conversion period.
A0–A10	1–9, 11, 12	I	Analog signal inputs. The 11 analog inputs are applied to these terminals and are internally multiplexed. The driving source impedance should be less than or equal to 1 kΩ.
$\overline{CS}$	15	I	Chip select. A high-to-low transition on this input resets the internal counters and controls and enables DATA OUT, ADDRESS, and I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock. A low-to-high transition disables ADDRESS and I/O CLOCK within a setup time plus two falling edges of the internal system clock.
DATA OUT	16	O	The 3-state serial output for the A/D conversion result. This output is in the high-impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low. With a valid chip select, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB value of the previous conversion result. The next falling edge of I/O CLOCK drives this output to the logic level corresponding to the next most significant bit, and the remaining bits are shifted out in order with the LSB appearing on the ninth falling edge of I/O CLOCK. On the tenth falling edge of I/O CLOCK, DATA OUT is driven to a low logic level so that serial interface data transfers of more than ten clocks produce zeroes as the unused LSBs.
EOC	19	O	End of conversion. This output goes from a high to a low logic level on the trailing edge of the tenth I/O CLOCK and remains low until the conversion is complete and data are ready for transfer.
GND	10	I	The ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to this terminal.
I/O CLOCK	18	I	Input/output clock. This terminal receives the serial I/O CLOCK input and performs the following four functions: 1) It clocks the four input address bits into the address register on the first four rising edges of the I/O CLOCK with the multiplex address available after the fourth rising edge. 2) On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplex input begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLOCK. 3) It shifts the nine remaining bits of the previous conversion data out on DATA OUT. 4) It transfers control of the conversion to the internal state controller on the falling edge of the tenth clock.
REF+	14	I	The upper reference voltage value (nominally V_{CC}) is applied to this terminal. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to the REF– terminal.
REF–	13	I	The lower reference voltage value (nominally ground) is applied to this terminal.
V_{CC}	20	I	Positive supply voltage

detailed description

With chip select ($\overline{CS}$) inactive (high), the ADDRESS and I/O CLOCK inputs are initially disabled and DATA OUT is in the high-impedance state. When the serial interface takes $\overline{CS}$ active (low), the conversion sequence begins with the enabling of I/O CLOCK and ADDRESS and the removal of DATA OUT from the high-impedance state. The serial interface then provides the 4-bit channel address to ADDRESS and the I/O CLOCK sequence to I/O CLOCK. During this transfer, the serial interface also receives the previous conversion result from DATA OUT. I/O CLOCK receives an input sequence that is between 10 and 16 clocks long from the host serial interface. The first four I/O clocks load the address register with the 4-bit address on ADDRESS, selecting the desired analog channel, and the next six clocks providing the control timing for sampling the analog input.

detailed description (continued)

There are six basic serial-interface timing modes that can be used with the device. These modes are determined by the speed of I/O CLOCK and the operation of $\overline{\text{CS}}$ as shown in Table 1. These modes are (1) a fast mode with a 10-clock transfer and $\overline{\text{CS}}$ inactive (high) between conversion cycles, (2) a fast mode with a 10-clock transfer and $\overline{\text{CS}}$ active (low) continuously, (3) a fast mode with an 11- to 16-clock transfer and $\overline{\text{CS}}$ inactive (high) between conversion cycles, (4) a fast mode with a 16-bit transfer and $\overline{\text{CS}}$ active (low) continuously, (5) a slow mode with an 11- to 16-clock transfer and $\overline{\text{CS}}$ inactive (high) between conversion cycles, and (6) a slow mode with a 16-clock transfer and $\overline{\text{CS}}$ active (low) continuously.

The MSB of the previous conversion appears at DATA OUT on the falling edge of $\overline{\text{CS}}$ in mode 1, mode 3, and mode 5, on the rising edge of EOC in mode 2 and mode 4, and following the sixteenth clock falling edge in mode 6. The remaining nine bits are shifted out on the next nine falling edges of I/O CLOCK. Ten bits of data are transmitted to the host-serial interface through DATA OUT. The number of serial clock pulses used also depends on the mode of operation, but a minimum of ten clock pulses is required for conversion to begin. On the tenth clock falling edge, the EOC output goes low and returns to the high logic level when conversion is complete and the result can be read by the host. Also, on the tenth clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero if the I/O CLOCK transfer is more than ten clocks long.

Table 1 lists the operational modes with respect to the state of $\overline{\text{CS}}$, the number of I/O serial transfer clocks that can be used, and the timing edge on which the MSB of the previous conversion appears at the output.

Table 1. Mode Operation

MODES		$\overline{\text{CS}}$	NO. OF I/O CLOCKS	MSB AT DATA OUT†	TIMING DIAGRAM
Fast Modes	Mode 1	High between conversion cycles	10	$\overline{\text{CS}}$ falling edge	Figure 9
	Mode 2	Low continuously	10	EOC rising edge	Figure 10
	Mode 3	High between conversion cycles	11 to 16‡	$\overline{\text{CS}}$ falling edge	Figure 11
	Mode 4	Low continuously	16‡	EOC rising edge	Figure 12
Slow Modes	Mode 5	High between conversion cycles	11 to 16‡	$\overline{\text{CS}}$ falling edge	Figure 13
	Mode 6	Low continuously	16‡	16th clock falling edge	Figure 14

† These edges also initiate serial-interface communication.
‡ No more than 16 clocks should be used.

fast modes

The device is in a fast mode when the serial I/O CLOCK data transfer is completed before the conversion is completed. With a 10-clock serial transfer, the device can only run in a fast mode since a conversion does not begin until the falling edge of the tenth I/O CLOCK.

mode 1: fast mode, $\overline{\text{CS}}$ inactive (high) between conversion cycles, 10-clock transfer

In this mode, $\overline{\text{CS}}$ is inactive (high) between serial I/O CLOCK transfers and each transfer is ten clocks long. The falling edge of $\overline{\text{CS}}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{\text{CS}}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{\text{CS}}$ disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 2: fast mode, $\overline{\text{CS}}$ active (low) continuously, 10-clock transfer

In this mode, $\overline{\text{CS}}$ is active (low) between serial I/O CLOCK transfers and each transfer is ten clocks long. After the initial conversion cycle, $\overline{\text{CS}}$ is held active (low) for subsequent conversions; the rising edge of EOC then begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previous conversion to appear immediately on this output.

mode 3: fast mode, $\overline{CS}$ inactive (high) between conversion cycles, 11- to 16-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 4: fast mode, $\overline{CS}$ active (low) continuously, 16-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions; the rising edge of EOC then begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previous conversion to appear immediately on this output.

slow modes

In a slow mode, the conversion is completed before the serial I/O CLOCK data transfer is completed. A slow mode requires a minimum 11-clock transfer into I/O CLOCK, and the rising edge of the eleventh clock must occur before the conversion period is complete; otherwise, the device loses synchronization with the host-serial interface and $\overline{CS}$ has to be toggled to initialize the system. The eleventh rising edge of the I/O CLOCK must occur within 9.5 µs after the tenth I/O clock falling edge.

mode 5: slow mode, $\overline{CS}$ inactive (high) between conversion cycles, 11- to 16-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 6: slow mode, $\overline{CS}$ active (low) continuously, 16-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions. The falling edge of the sixteenth I/O CLOCK then begins each sequence by removing DATA OUT from the low state, allowing the MSB of the previous conversion to appear immediately at DATA OUT. The device is then ready for the next 16-clock transfer initiated by the serial interface.

address bits

The 4-bit analog channel-select address for the next conversion cycle is presented to the ADDRESS terminal (MSB first) and is clocked into the address register on the first four leading edges of I/O CLOCK. This address selects one of 14 inputs (11 analog inputs or three internal test inputs).

analog inputs and test modes

The 11 analog inputs and the three internal test inputs are selected by the 14-channel multiplexer according to the input address as shown in Tables 2 and 3. The input multiplexer is a break-before-make type to reduce input-to-input noise injection resulting from channel switching.

Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK, and sampling continues for six I/O CLOCK periods. The sample is held on the falling edge of the tenth I/O CLOCK. The three test inputs are applied to the multiplexer, sampled, and converted in the same manner as the external analog inputs.

analog inputs and test modes (continued)

Table 2. Analog-Channel-Select Address

ANALOG INPUT SELECTED	VALUE SHIFTED INTO ADDRESS INPUT	
	BINARY	HEX
A0	0000	0
A1	0001	1
A2	0010	2
A3	0011	3
A4	0100	4
A5	0101	5
A6	0110	6
A7	0111	7
A8	1000	8
A9	1001	9
A10	1010	A

Table 3. Test-Mode-Select Address

INTERNAL SELF-TEST VOLTAGE SELECTED†	VALUE SHIFTED INTO ADDRESS INPUT		OUTPUT RESULT (HEX)‡
	BINARY	HEX	
$\frac{V_{ref+} - V_{ref-}}{2}$	1011	B	200
V_{ref-}	1100	C	000
V_{ref+}	1101	D	3FF

† V_{ref+} is the voltage applied to the REF+ input, and V_{ref-} is the voltage applied to the REF– input.
‡ The output results shown are the ideal values and vary with the reference stability and with internal offsets.

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF–) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF–. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half V_{CC}), a 0 bit is placed in the output register and the 512-weight capacitor is switched to REF–. If the voltage at the summing node is less than the trip point of the threshold detector, a 1 bit is placed in the register and the 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are counted.

converter and analog input (continued)

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to count and weigh the bits from MSB to LSB.

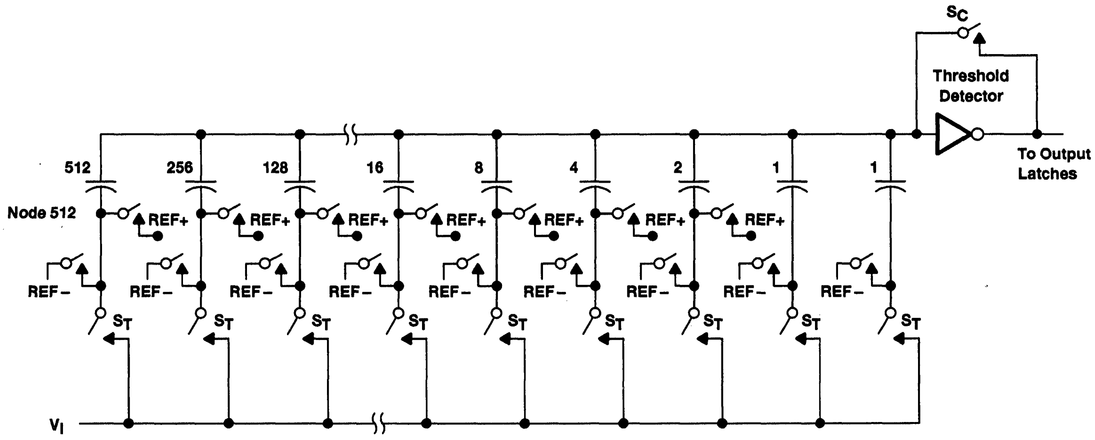


Figure 1. Simplified Model of the Successive-Approximation System

chip-select operation

The trailing edge of $\overline{CS}$ starts all modes of operation, and $\overline{CS}$ can abort a conversion sequence in any mode. A high-to-low transition on $\overline{CS}$ within the specified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the contents of the output data register remain at the previous conversion result). Exercise care to prevent $\overline{CS}$ from being taken low close to completion of conversion because the output data can be corrupted.

reference voltage inputs

There are two reference inputs used with the device: REF+ and REF–. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero reading, respectively. The values of REF+, REF–, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and at zero when the input signal is equal to or lower than REF–.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) .... −0.5 V to 6.5 V
Input voltage range, V_I .... −0.3 V to V_{CC} + 0.3 V
Output voltage range, V_O .... −0.3 V to V_{CC} + 0.3 V
Positive reference voltage, V_{ref+} .... V_{CC} + 0.1 V
Negative reference voltage, V_{ref-} .... −0.1 V
Peak input current (any input) .... ±20 mA
Peak total input current (all inputs) .... ±30 mA
Operating free-air temperature range, T_A: TLC1542C, TLC1543C .... 0°C to 70°C
TLC1542I, TLC1543I .... −40°C to 85°C
TLC1542Q, TLC1543Q .... −40°C to 125°C
TLC1542M .... −55°C to 125°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to digital ground with REF – and GND wired together (unless otherwise noted).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)			V_{CC}		V
Negative reference voltage, V_{ref-} (see Note 2)			0		V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)		2.5	V_{CC}	V_{CC}+0.2	V
Analog input voltage (see Note 2)		0		V_{CC}	V
High-level control input voltage, V_{IH}	V_{CC} = 4.5 V to 5.5 V	2			V
Low-level control input voltage, V_{IL}	V_{CC} = 4.5 V to 5.5 V			0.8	V
Setup time, address bits at data input before I/O CLOCK↑, $t_{su(A)}$		100			ns
Hold time, address bits after I/O CLOCK↑, $t_{h(A)}$		0			ns
Hold time, $\overline{CS}$ low after last I/O CLOCK↓, $t_{h(CS)}$		0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3)		1.425			µs
Clock frequency at I/O CLOCK (see Note 4)		0		2.1	MHz
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$		190			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$		190			ns
Transition time, I/O CLOCK, $t_{t(I/O)}$ (see Note 5 and Figure 6)				1	µs
Transition time, ADDRESS and $\overline{CS}$, $t_{t(CS)}$				10	µs
Operating free-air temperature, T_A	TLC1542C, TLC1543C	0		70	°C
	TLC1542I, TLC1543I	−40		85	°C
	TLC1542Q, TLC1543Q	−40		125	°C
	TLC1542M	−55		125	°C

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF− convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.
3. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}$↓ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.
4. For 11- to 16-bit transfers, after the tenth I/O CLOCK falling edge (≤ 2 V) at least 1 I/O CLOCK rising edge (≥ 2 V) must occur within 9.5 µs.
5. This is the time required for the clock input signal to fall from V_{IH}min to V_{IL}max or to rise from V_{IL}max to V_{IH}min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 µs for remote data-acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+} = 4.5$ V to 5.5 V, I/O CLOCK frequency = 2.1 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.5 V,	I_{OH} = −1.6 mA	2.4			V
			V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −20 μA	V_{CC}−0.1			
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V,	I_{OL} = 1.6 mA			0.4	V
			V_{CC} = 4.5 V to 5.5 V,	I_{OL} = 20 μA			0.1	
I_{OZ}	Off-state (high-impedance-state) output current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}			10	μA
			V_O = 0,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		$V_I = V_{CC}$			0.005	2.5	μA
I_{IL}	Low-level input current		V_I = 0			−0.005	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			0.8	2.5	mA
	Selected channel leakage current TLC1542/TLC1543 C, I, or Q		Selected channel at V_{CC},	Unselected channel at 0 V			1	μA
			Selected channel at 0 V,	Unselected channel at V_{CC}			−1	
	Selected channel leakage current TLC1542M		Selected channel at V_{CC}, T_A = 25°C	Unselected channel at 0 V,			1	μA
			Selected channel at 0 V, T_A = 25°C	Unselected channel at V_{CC},			−1	
			Selected channel at V_{CC},	Unselected channel at 0 V			2.5	
			Selected channel at 0 V,	Unselected channel at V_{CC}			−2.5	
	Maximum static analog reference current into REF+		$V_{ref+} = V_{CC}$,	V_{ref-} = GND			10	μA
C_i	Input capacitance	Analog inputs				7		pF
		Control inputs				5		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+} = 4.5$ V to 5.5 V, I/O CLOCK frequency = 2.1 MHz (unless otherwise noted)

			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error (see Note 6)	TLC1542C, I, or Q				±0.5	LSB
		TLC1543C, I, or Q				±1	LSB
		TLC1542M				±1	LSB
E_{ZS}	Zero-scale error (see Note 7)	TLC1542C, I, or Q	See Note 2			±0.5	LSB
		TLC1543C, I, or Q	See Note 2			±1	LSB
		TLC1542M	See Note 2			±1	LSB
E_{FS}	Full-scale error (see Note 7)	TLC1542C, I, or Q	See Note 2			±0.5	LSB
		TLC1543C, I, or Q	See Note 2			±1	LSB
		TLC1542M	See Note 2			±1	LSB
	Total unadjusted error (see Note 8)	TLC1542C, I, or Q				±1	LSB
		TLC1543C, I, or Q				±1	LSB
		TLC1542M				±1	LSB
	Self-test output code (see Table 3 and Note 9)		ADDRESS = 1011		512		
			ADDRESS = 1100		0		
			ADDRESS = 1101		1023		
t_{conv}	Conversion time		See timing diagrams			21	µs
t_c	total cycle time (access, sample, and conversion)		See timing diagrams and Note 10			21 +10 I/O CLOCK periods	µs
t_{acq}	Channel acquisition time (sample)		See timing diagrams and Note 10			6	I/O CLOCK periods
t_v	Valid time, DATA OUT remains valid after I/O CLOCK↓		See Figure 6	10			ns
$t_{d(I/O-DATA)}$	Delay time, I/O CLOCK↓ to DATA OUT valid		See Figure 6			240	ns
$t_{d(I/O-EOC)}$	Delay time, tenth I/O CLOCK↓ to EOC↓		See Figure 7		70	240	ns
$t_{d(EOC-DATA)}$	Delay time, EOC↑ to DATA OUT (MSB)		See Figure 8			100	ns

† All typical values are at $T_A = 25°C$.

NOTES:
2. Analog input voltages greater than that applied to REF + convert as all ones (1111111111), while input voltages less than that applied to REF – convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.
6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
7. Zero-scale error is the difference between 0000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.
8. Total unadjusted error comprises linearity, zero-scale, and full-scale errors.
9. Both the input address and the output codes are expressed in positive logic.
10. I/O CLOCK period = 1/(I/O CLOCK frequency) (see Figure 6)

operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+} = 4.5$ V to 5.5 V, I/O CLOCK frequency = 2.1 MHz (unless otherwise noted) (continued)

		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PZH}, t_{PZL}	Enable time, $\overline{CS}$↓ to DATA OUT (MSB driven)	See Figure 3			1.3	µs
t_{PHZ}, t_{PLZ}	Disable time, $\overline{CS}$↑ to DATA OUT (high impedance)	See Figure 3			150	ns
$t_{r(EOC)}$	Rise time, EOC	See Figure 8			300	ns
$t_{f(EOC)}$	Fall time, EOC	See Figure 7			300	ns
$t_{r(DATA)}$	Rise time, data bus	See Figure 6			300	ns
$t_{f(DATA)}$	Fall time, data bus	See Figure 6			300	ns
$t_{d(I/O\text{-}CS)}$	Delay time, tenth I/O CLOCK↓ to $\overline{CS}$↓ to abort conversion (see Note 11)				9	µs

† All typical values are at $T_A = 25°C$.

NOTE 11. Any transitions of $\overline{CS}$ are recognized as valid only if the level is maintained for a setup time plus two falling edges of the internal clock (1.425 µs) after the transition.

PARAMETER MEASUREMENT INFORMATION

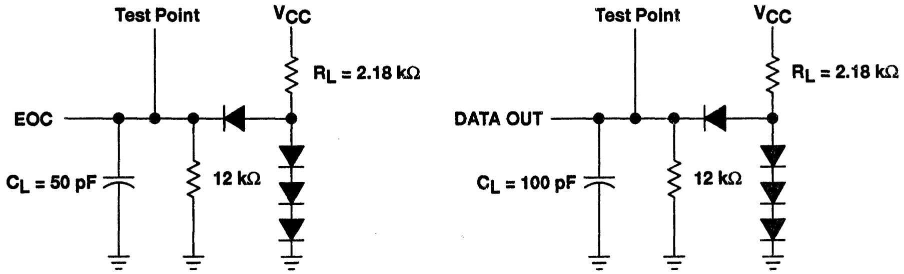


Figure 2. Load Circuits

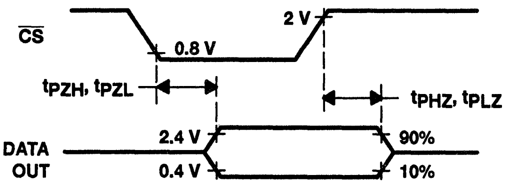


Figure 3. DATA OUT Enable and Disable Voltage Waveforms

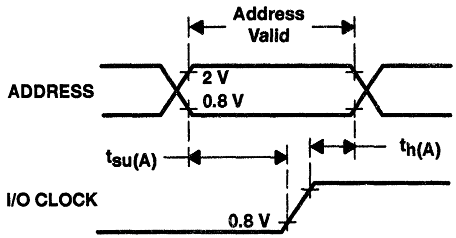


Figure 4. ADDRESS Setup and Hold Time Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

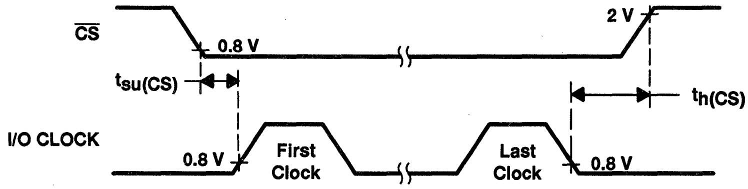


Figure 5. I/O CLOCK Setup and Hold Time Voltage Waveforms

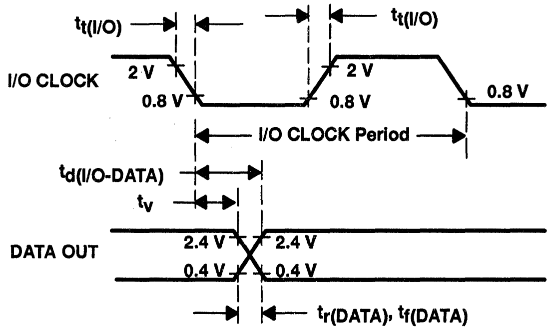


Figure 6. I/O CLOCK and DATA OUT Voltage Waveforms

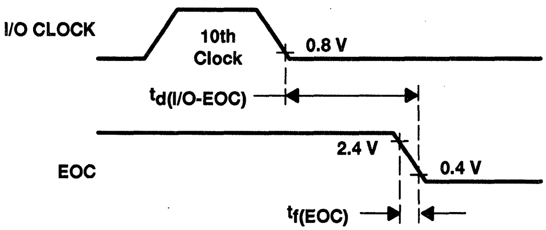


Figure 7. I/O CLOCK and EOC Voltage Waveforms

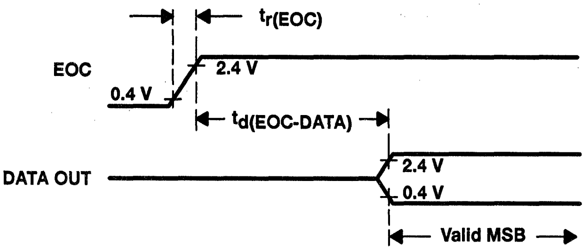


Figure 8. EOC and DATA OUT Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

timing diagrams

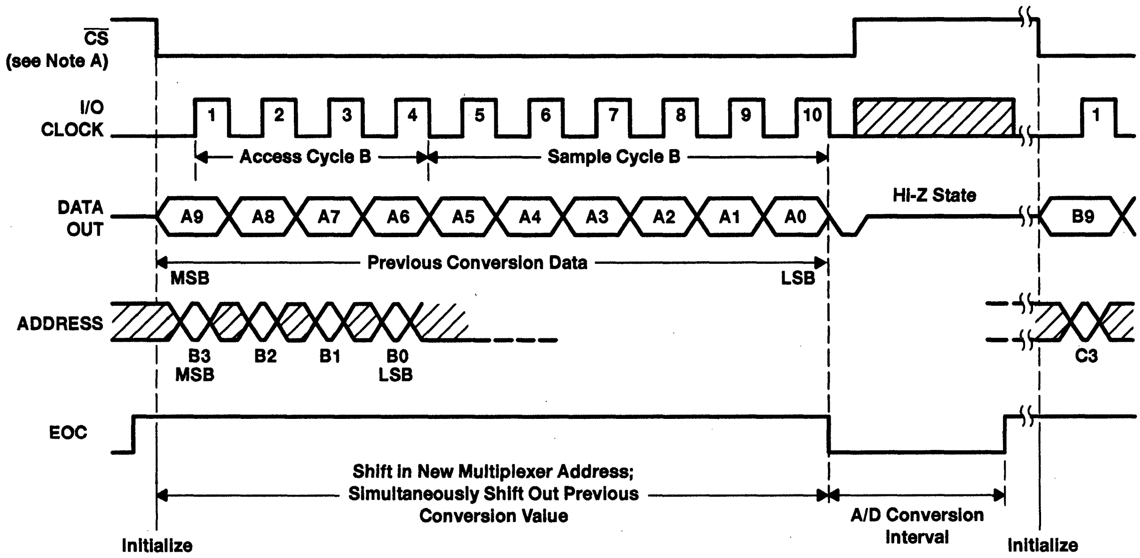


Figure 9. Timing for 10-Clock Transfer Using $\overline{CS}$

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

PARAMETER MEASUREMENT INFORMATION

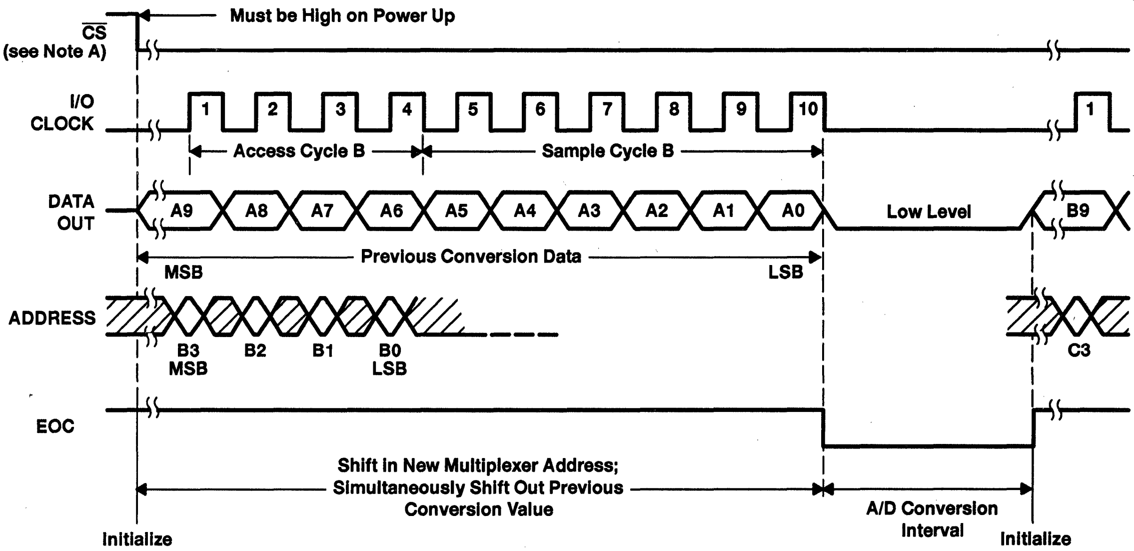


Figure 10. Timing for 10-Clock Transfer Not Using $\overline{CS}$

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

PARAMETER MEASUREMENT INFORMATION

timing diagrams (continued)

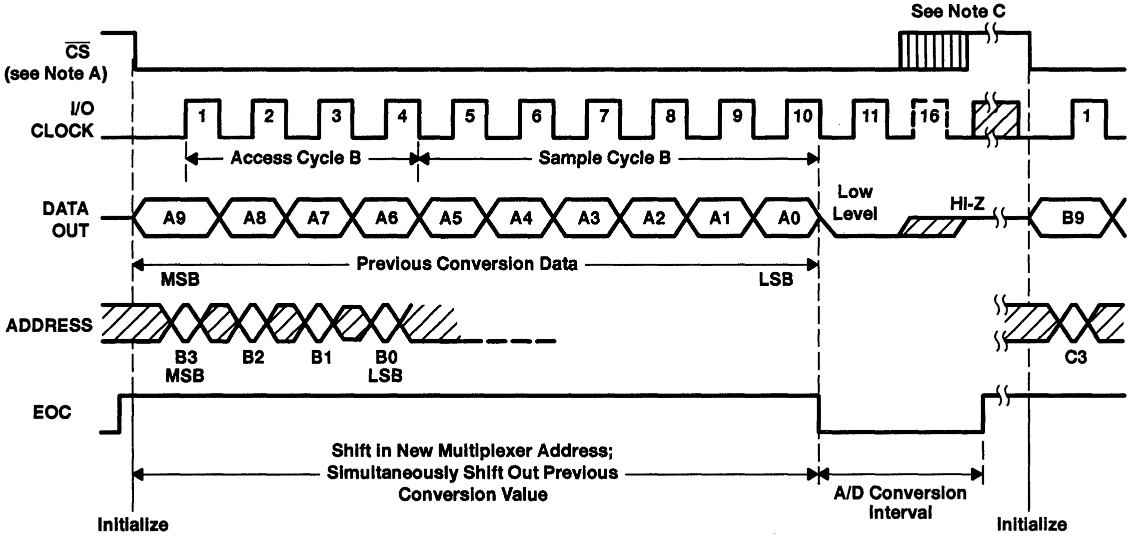


Figure 11. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$ (Serial Transfer Interval Shorter Than Conversion)

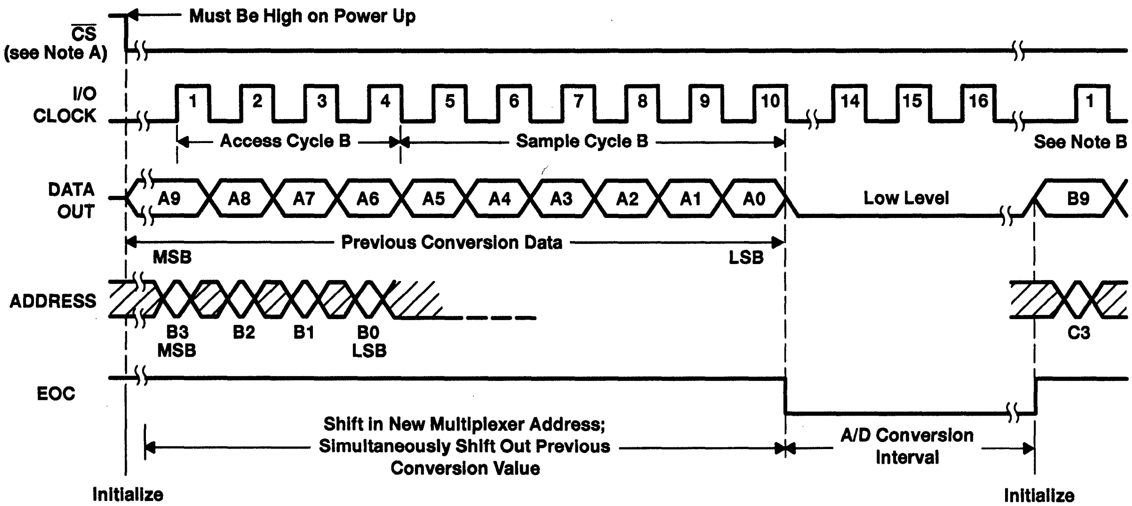
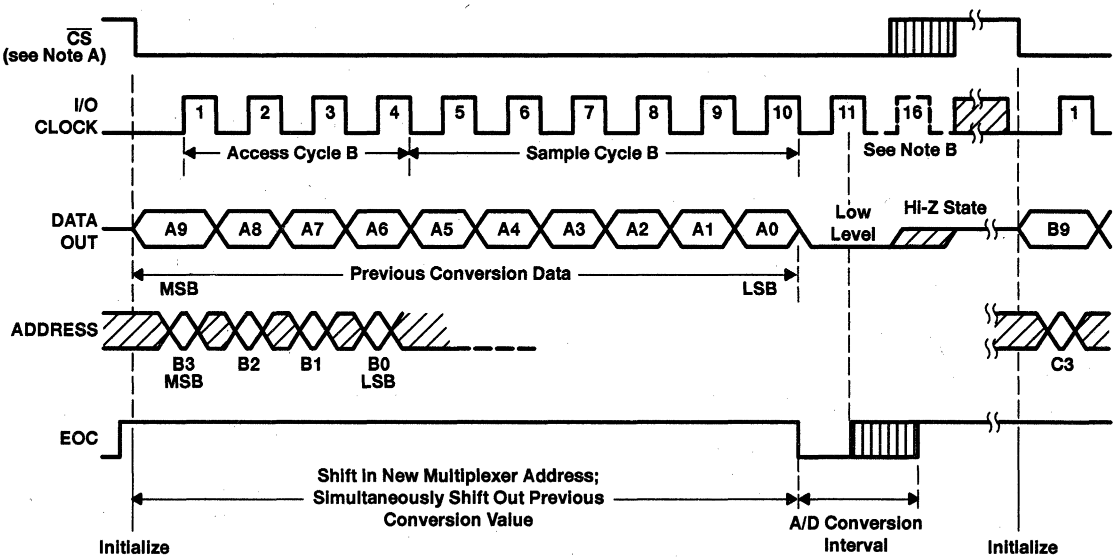


Figure 12. Timing for 16-Clock Transfer Not Using $\overline{CS}$ (Serial Transfer Interval Shorter Than Conversion)

NOTES: A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.
B. The first I/O CLOCK must occur after the rising edge of EOC.
C. A low-to-high transition of $\overline{CS}$ disables ADDRESS and the I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.

PARAMETER MEASUREMENT INFORMATION

timing diagrams (continued)



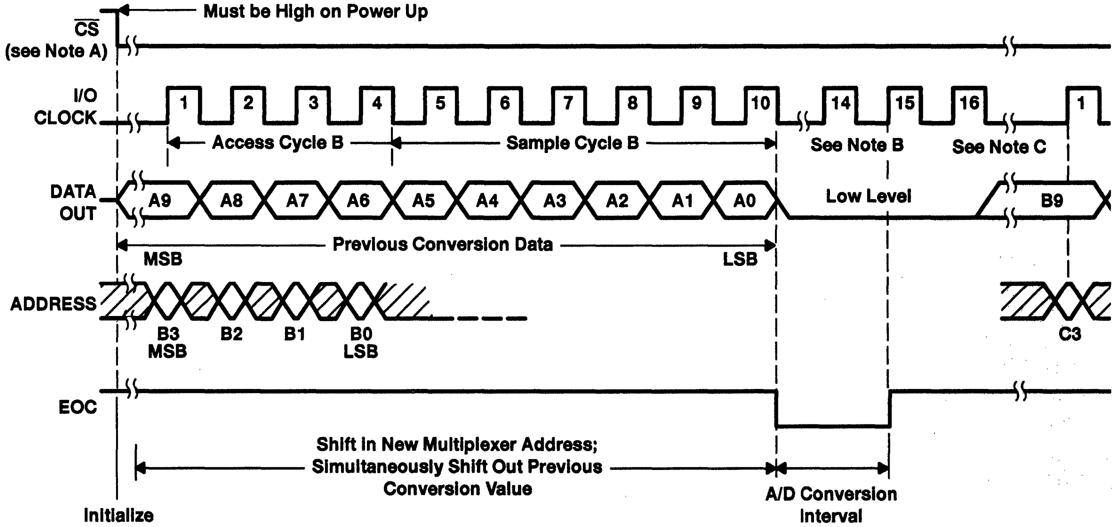
NOTES: A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

B. The 11th rising edge of the I/O CLOCK sequence must occur before the conversion is complete to prevent losing serial interface synchronization.

Figure 13. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$ (Serial Transfer Interval Longer Than Conversion)

PARAMETER MEASUREMENT INFORMATION

timing diagrams (continued)



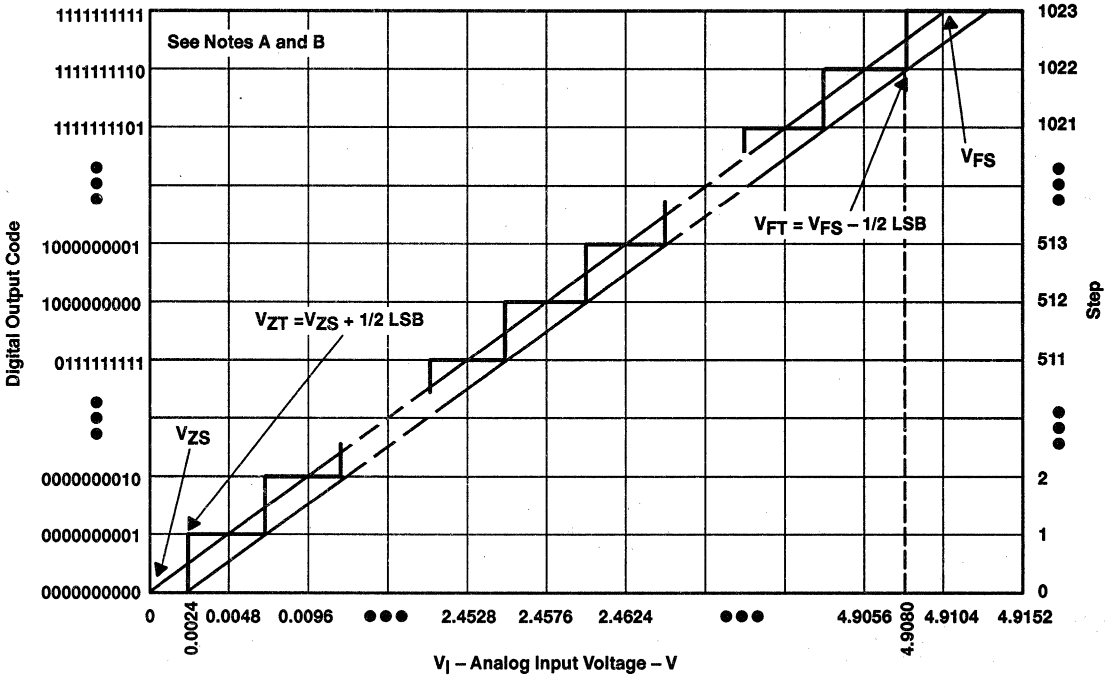
NOTES: A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

B. The 11th rising edge of the I/O CLOCK sequence must occur before the conversion is complete to prevent losing serial interface synchronization.

C. The I/O CLOCK sequence is exactly 16 clock pulses long.

Figure 14. Timing for 16-Clock Transfer Not Using $\overline{CS}$ (Serial Transfer Interval Longer Than Conversion)

APPLICATION INFORMATION



NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0024 V and the transition to full scale (V_{FT}) is 4.908 V. 1 LSB = 4.8 mV.

B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 15. Ideal Conversion Characteristics

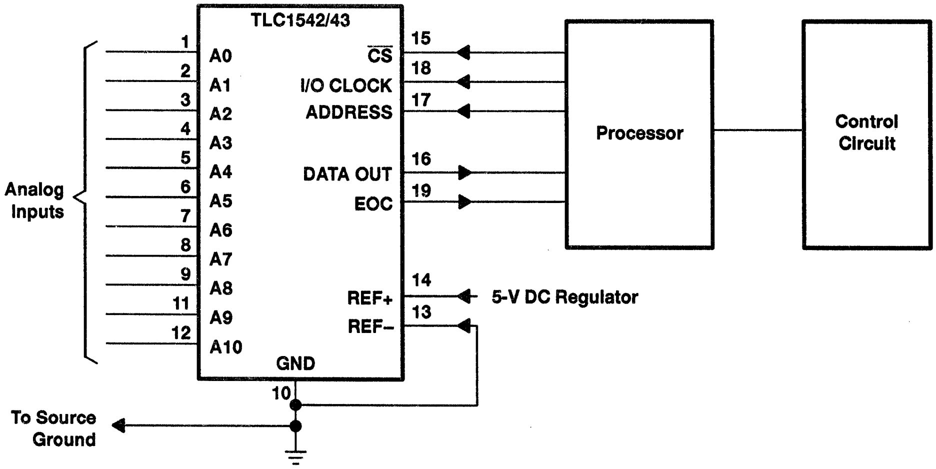


Figure 16. Serial Interface

APPLICATION INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 17, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c/R_t C_i}\right) \tag{1}$$

where

$$R_t = R_s + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C\,(1/2\ \text{LSB}) = V_S - (V_S/2048) \tag{2}$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S/2048) = V_S \left(1 - e^{-t_c/R_t C_i}\right) \tag{3}$$

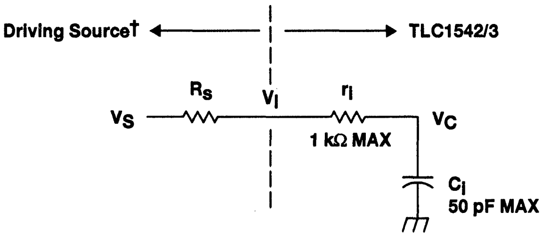
and

$$t_c\,(1/2\ \text{LSB}) = R_t \times C_i \times \ln(2048) \tag{4}$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c\,(1/2\ \text{LSB}) = (R_s + 1\ \text{k}\Omega) \times 60\ \text{pF} \times \ln(2048) \tag{5}$$

This time must be less than the converter sample time shown in the timing diagrams.



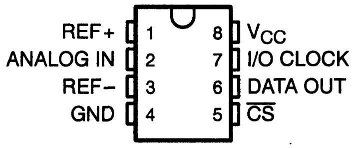
V_I = Input Voltage at A0–A10
V_S = External Driving Source Voltage
R_s = Source Resistance
r_I = Input Resistance
C_I = Equivalent Input Capacitance

† Driving source requirements:
- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_s must be real at the input frequency.

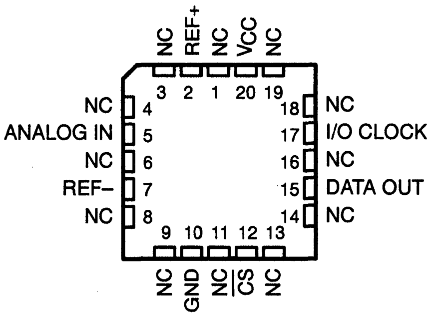
Figure 17. Equivalent Input Circuit Including the Driving Source

- **10-Bit-Resolution A/D Converter**
- **Inherent Sample and Hold**
- **Total Unadjusted Error . . . ±1 LSB Max**
- **On-Chip System Clock**
- **Terminal Compatible With TLC549 and TLV1549**
- **CMOS Technology**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLC1549C, TLC1549I, and TLC1549M are 10-bit, switched-capacitor, successive-approximation analog-to-digital converters. These devices have two digital inputs and a 3-state output [chip select (CS), input-output clock (I/O CLOCK), and data output (DATA OUT)] that provide a three-wire interface to the serial port of a host processor.

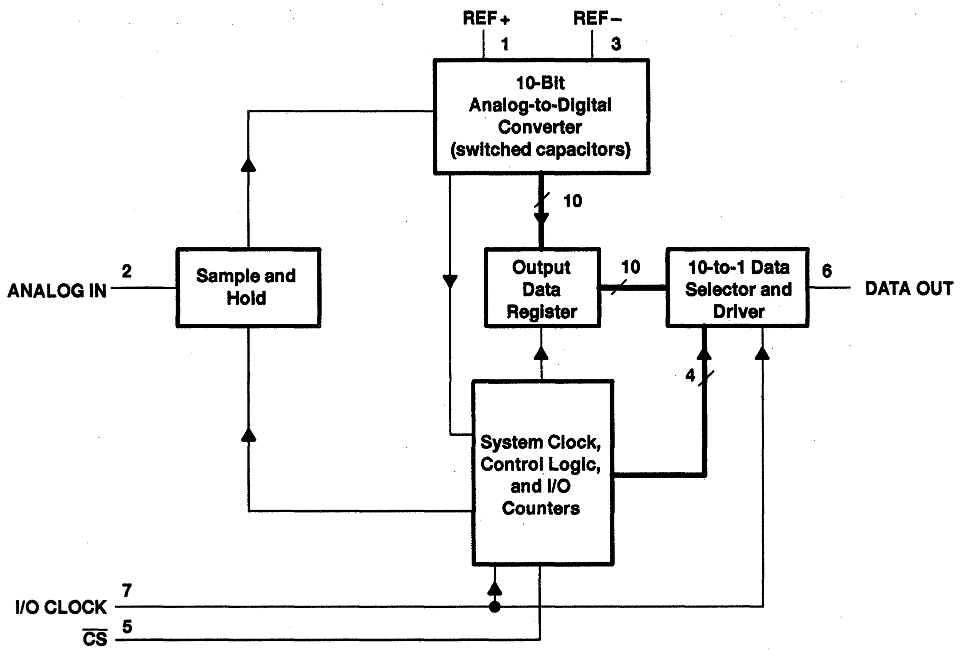
The sample-and-hold function is automatic. The converter incorporated in these devices features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating free-air temperature range.

The TLC1549C is characterized for operation from 0°C to 70°C. The TLC1549I is characterized for operation from −40°C to 85°C. The TLC1549M is characterized for operation over the full military temperature range of −55°C to 125°C.

AVAILABLE OPTIONS

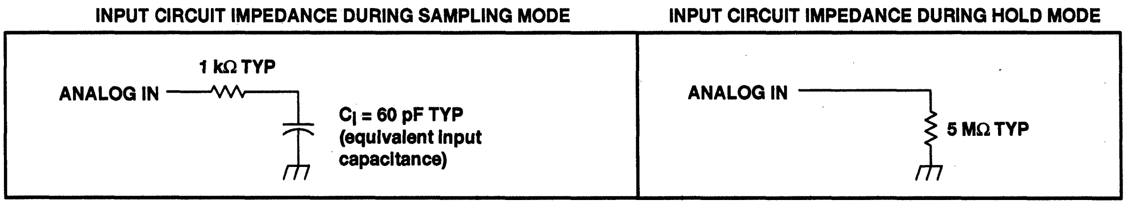
T_A	PACKAGE			
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	TLC1549CD	—	—	TLC1549CP
−40°C to 85°C	TLC1549ID	—	—	TLC1549IP
−55°C to 125°C	—	TLC1549MFK	TLC1549MJG	—

functional block diagram



Terminal numbers shown are for the D, JG, and P packages only.

typical equivalent inputs



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ANALOG IN	2	I	Analog signal input. The driving source impedance should be ≤ 1 kΩ. The external driving source to ANALOG IN should have a current capability ≥ 10 mA.
$\overline{CS}$	5	I	Chip select. A high-to-low transition on $\overline{CS}$ resets the internal counters and controls and enables DATA OUT and I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock. A low-to-high transition disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.
DATA OUT	6	O	This 3-state serial output for the A/D conversion result is in the high-impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low. With a valid chip select, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB value of the previous conversion result. The next falling edge of I/O CLOCK drives DATAOUT to the logic level corresponding to the next most significant bit, and the remaining bits are shifted out in order with the LSB appearing on the ninth falling edge of I/O CLOCK. On the tenth falling edge of I/O CLOCK, DATA OUT is driven to a low logic level so that serial interface data transfers of more than ten clocks produce zeroes as the unused LSBs.
GND	4		The ground return for internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
I/O CLOCK	7	I	Input/output clock. I/O CLOCK receives the serial I/O CLOCK input and performs the following three functions: 1) On the third falling edge of I/O CLOCK, the analog input voltage begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLOCK. 2) It shifts the nine remaining bits of the previous conversion data out on DATA OUT. 3) It transfers control of the conversion to the internal state controller on the falling edge of the tenth clock.
REF+	1	I	The upper reference voltage value (nominally V_{CC}) is applied to REF+. The maximum input voltage range is determined by the difference between the voltage applied to REF+ and the voltage applied to REF–.
REF–	3	I	The lower reference voltage value (nominally ground) is applied to REF–.
V_{CC}	8		Positive supply voltage

detailed description

With chip select ($\overline{CS}$) inactive (high), I/O CLOCK is initially disabled and DATA OUT is in the high-impedance state. When the serial interface takes $\overline{CS}$ active (low), the conversion sequence begins with the enabling of I/O CLOCK and the removal of DATA OUT from the high-impedance state. The serial interface then provides the I/O CLOCK sequence to I/O CLOCK and receives the previous conversion result from DATA OUT. I/O CLOCK receives an input sequence that is between 10 and 16 clocks long from the host serial interface. The first ten I/O clocks provide the control timing for sampling the analog input.

There are six basic serial interface timing modes that can be used with the TLC1549. These modes are determined by the speed of I/O CLOCK and the operation of $\overline{CS}$ as shown in Table 1. These modes are (1) a fast mode with a 10-clock transfer and $\overline{CS}$ inactive (high) between transfers, (2) a fast mode with a 10-clock transfer and $\overline{CS}$ active (low) continuously, (3) a fast mode with an 11- to 16-clock transfer and $\overline{CS}$ inactive (high) between transfers, (4) a fast mode with a 16-bit transfer and $\overline{CS}$ active (low) continuously, (5) a slow mode with an 11- to 16-clock transfer and $\overline{CS}$ inactive (high) between transfers, and (6) a slow mode with a 16-clock transfer and $\overline{CS}$ active (low) continuously.

The MSB of the previous conversion appears on DATA OUT on the falling edge of $\overline{CS}$ in mode 1, mode 3, and mode 5, within 21 µs from the falling edge of the tenth I/O CLOCK in mode 2 and mode 4, and following the sixteenth clock falling edge in mode 6. The remaining nine bits are shifted out on the next nine falling edges of I/O CLOCK. Ten bits of data are transmitted to the host serial interface through DATA OUT. The number of serial clock pulses used also depends on the mode of operation, but a minimum of ten clock pulses is required for conversion to begin. On the tenth clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero if the I/O CLOCK transfer is more than ten clocks long.

detailed description (continued)

Table 1 lists the operational modes with respect to the state of $\overline{CS}$, the number of I/O serial transfer clocks that can be used, and the timing on which the MSB of the previous conversion appears at the output.

Table 1. Mode Operation

MODES		$\overline{CS}$	NO. OF I/O CLOCKS	MSB AT Terminal 6†	TIMING DIAGRAM
Fast Modes	Mode 1	High between conversion cycles	10	$\overline{CS}$ falling edge	Figure 6
	Mode 2	Low continuously	10	Within 21 µs	Figure 7
	Mode 3	High between conversion cycles	11 to 16‡	$\overline{CS}$ falling edge	Figure 8
	Mode 4	Low continuously	16‡	Within 21 µs	Figure 9
Slow Modes	Mode 5	High between conversion cycles	11 to 16‡	$\overline{CS}$ falling edge	Figure 10
	Mode 6	Low continuously	16‡	16th clock falling edge	Figure 11

† This timing also initiates serial interface communication.
‡ No more than 16 clocks should be used.

All the modes require a minimum period of 21 µs after the falling edge of the tenth I/O CLOCK before a new transfer sequence can begin. During a serial I/O CLOCK data transfer, $\overline{CS}$ must be active (low) so that I/O CLOCK is enabled. When $\overline{CS}$ is toggled between data transfers (modes 1, 3, and 5), the transitions at $\overline{CS}$ are recognized as valid only if the level is maintained for a minimum period of 1.425 µs after the transition. If the transfer is more than ten I/O clocks (modes 3, 4, 5, and 6), the rising edge of the eleventh clock must occur within 9.5 µs after the falling edge of the tenth I/O CLOCK; otherwise, the device could lose synchronization with the host serial interface and $\overline{CS}$ has to be toggled to restore proper operation.

fast modes

The TLC1549 is in a fast mode when the serial I/O CLOCK data transfer is completed within 21 µs from the falling edge of the tenth I/O CLOCK. With a ten-clock serial transfer, the device can only run in a fast mode.

mode 1: fast mode, $\overline{CS}$ inactive (high) between transfers, 10-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O CLOCK transfers and each transfer is ten clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 2: fast mode, $\overline{CS}$ active (low) continuously, 10-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O CLOCK transfers and each transfer is ten clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions. Within 21 µs after the falling edge of the tenth I/O CLOCK, the MSB of the previous conversion appears at DATA OUT.

mode 3: fast mode, $\overline{CS}$ inactive (high) between transfers, 11- to 16-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 4: fast mode, $\overline{CS}$ active (low) continuously, 16-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions. Within 21 µs after the falling edge of the tenth I/O CLOCK, the MSB of the previous conversion appears at DATA OUT.

slow modes

In a slow mode, the serial I/O CLOCK data transfer is completed after 21 μs from the falling edge of the tenth I/O CLOCK.

mode 5: slow mode, $\overline{CS}$ inactive (high) between transfers, 11- to 16-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 6: slow mode, $\overline{CS}$ active (low) continuously, 16-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions. The falling edge of the sixteenth I/O CLOCK then begins each sequence by removing DATA OUT from the low state, allowing the MSB of the previous conversion to appear immediately at DATA OUT. The device is then ready for the next-16 clock transfer initiated by the serial interface.

analog input sampling

Sampling of the analog input starts on the falling edge of the third I/O CLOCK, and sampling continues for seven I/O CLOCK periods. The sample is held on the falling edge of the tenth I/O CLOCK.

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF–) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF–. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half V_{CC}), a bit 0 is placed in the output register and the 512-weight capacitor is switched to REF–. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and this 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are determined.

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to determine the bits from MSB to LSB.

converter and analog input (continued)

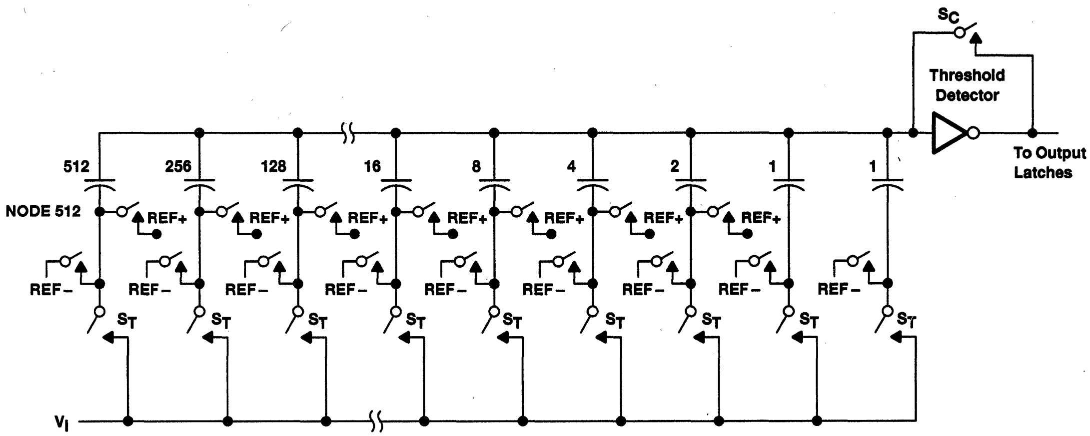


Figure 1. Simplified Model of the Successive-Approximation System

chip-select operation

The trailing edge of $\overline{CS}$ starts all modes of operation, and $\overline{CS}$ can abort a conversion sequence in any mode. A high-to-low transition on $\overline{CS}$ within the specified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the contents of the output data register remain at the previous conversion result). Care should be exercised to prevent $\overline{CS}$ from being taken low close to completion of conversion because the output data may be corrupted.

reference voltage inputs

There are two reference inputs used with the TLC1549: REF+ and REF−. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero reading respectively. The values of REF+, REF−, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and at zero when the input signal is equal to or lower than REF−.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1): TLC1549C, TLC1549I .... −0.5 V to 6.5 V
TLC1549M .... −0.5 V to 6 V
Input voltage range, V_I (any input) .... −0.3 V to V_{CC} + 0.3 V
Output voltage range, V_O .... −0.3 V to V_{CC} + 0.3 V
Positive reference voltage, V_{ref+} .... V_{CC} + 0.1 V
Negative reference voltage, V_{ref-} .... −0.1 V
Peak input current (any input) .... ±20 mA
Peak total input current (all inputs) .... ±30 mA
Operating free-air temperature range, T_A: TLC1549C .... 0°C to 70°C
TLC1549I .... −40°C to 85°C
TLC1549M .... −55°C to 125°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to ground with REF− and GND wired together (unless otherwise noted).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)			V_{CC}		V
Negative reference voltage, V_{ref-} (see Note 2)			0		V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)		2.5	V_{CC}	V_{CC}+0.2	V
Analog input voltage (see Note 2)		0		V_{CC}	V
High-level control input voltage, V_{IH}	V_{CC} = 4.5 V to 5.5 V	2			V
Low-level control input voltage, V_{IL}	V_{CC} = 4.5 V to 5.5 V			0.8	V
Clock frequency at I/O CLOCK (see Note 3)		0		2.1	MHz
Setup time, $\overline{CS}$ low before first I/O CLOCK↑, $t_{su(CS)}$ (see Note 4)		1.425			µs
Hold time, $\overline{CS}$ low after last I/O CLOCK↓, $t_{h(CS)}$		0			ns
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$		190			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$		190			ns
Transition time, I/O CLOCK, $t_{t(I/O)}$ (see Note 5 and Figure 5)				1	µs
Transition time, $\overline{CS}$, $t_{t(CS)}$				10	µs
Operating free-air temperature, T_A	TLC1549C	0		70	°C
	TLC1549I	−40		85	°C
	TLC1549M	−55		125	°C

NOTES: 2. Analog input voltages greater than that applied to REF + convert as all ones (1111111111), while input voltages less than that applied to REF − convert as all zeros (0000000000). The TLC1549 is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.

3. For 11- to 16-bit transfers, after the tenth I/O CLOCK falling edge (≤ 2 V) at least 1 I/O CLOCK rising edge (≥ 2 V) must occur within 9.5 µs.

4. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}$↓ before responding to the I/O CLOCK. No attempt should be made to clock out the data until the minimum $\overline{CS}$ setup time has elapsed.

5. This is the time required for the clock input signal to fall from V_{IH}min to V_{IL}max or to rise from V_{IL}max to V_{IH}min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 µs for remote data-acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+} = 4.5$ V to 5.5 V, I/O CLOCK frequency = 2.1 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		$V_{CC} = 4.5$ V,	$I_{OH} = -1.6$ mA	2.4			V
			$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -20$ µA	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$V_{CC} = 4.5$ V,	$I_{OL} = 1.6$ mA			0.4	V
			$V_{CC} = 4.5$ V to 5.5 V,	$I_{OL} = 20$ µA			0.1	
I_{OZ}	Off-state (high-impedance-state) output current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}			10	µA
			$V_O = 0$,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		$V_I = V_{CC}$			0.005	2.5	µA
I_{IL}	Low-level input current		$V_I = 0$			−0.005	−2.5	µA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			0.8	2.5	mA
	Analog input leakage current		$V_I = V_{CC}$				1	µA
			$V_I = 0$				−1	
	Maximum static analog reference current into REF+		$V_{ref+} = V_{CC}$,	V_{ref-} = GND			10	µA
C_i	Input capacitance	TLC1549C, I (Analog)	During sample cycle			30	55	pF
		TLC1549M (Analog)	During sample cycle			30		
		TLC1549C, I (Control)				5	15	
		TLC1549M (Control)				5		

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 4.5 V to 5.5 V, I/O CLOCK frequency = 2.1 MHz

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
E_L	Linearity error (see Note 6)			±1	LSB
E_{ZS}	Zero-scale error (see Note 7)	See Note 2		±1	LSB
E_{FS}	Full-scale error (see Note 7)	See Note 2		±1	LSB
	Total unadjusted error (see Note 8)			±1	LSB
t_{conv}	Conversion time	See Figures 6–10		21	μs
t_c	Total cycle time (access, sample, and conversion)	See Figures 6–10, See Note 9		21 +10 I/O CLOCK periods	μs
t_v	Valid time, DATA OUT remains valid after I/O CLOCK↓	See Figure 5	10		ns
$t_{d(I/O\text{-}DATA)}$	Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 5		240	ns
t_{PZH}, t_{PZL}	Enable time, $\overline{CS}$↓ to DATA OUT (MSB driven)	See Figure 3		1.3	μs
t_{PHZ}, t_{PLZ}	Disable time, $\overline{CS}$↑ to DATA OUT (high impedance)	See Figure 3		180	ns
$t_{r(bus)}$	Rise time, data bus	See Figure 5		300	ns
$t_{f(bus)}$	Fall time, data bus	See Figure 5		300	ns
$t_{d(I/O\text{-}CS)}$	Delay time, tenth I/O CLOCK↓ to $\overline{CS}$↓ to abort conversion (see Note 10)			9	μs

NOTES: 2. Analog input voltages greater than that applied to REF + convert as all ones (1111111111), while input voltages less than that applied to REF – convert as all zeros (0000000000). The TLC1549 is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.
6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
7. Zero error is the difference between 0000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.
8. Total unadjusted error comprises linearity, zero, and full-scale errors.
9. I/O CLOCK period = 1/(I/O CLOCK frequency). Sampling begins on the falling edge of the third I/O CLOCK, continues for seven I/O CLOCK periods, and ends on the falling edge of the 10th I/O CLOCK (see Figure 5).
10. Any transitions of $\overline{CS}$ are recognized as valid only if the level is maintained for a minimum of a setup time plus two falling edges of the internal clock (1.425 μs) after the transition.

PARAMETER MEASUREMENT INFORMATION

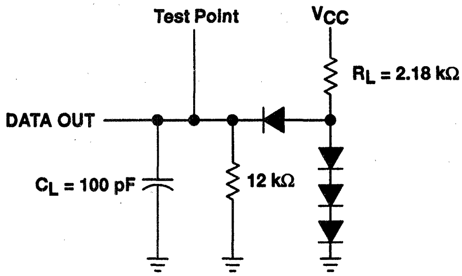


Figure 2. Load Circuit

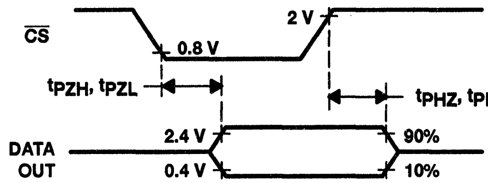


Figure 3. DATA OUT to Hi-Z Voltage Waveforms

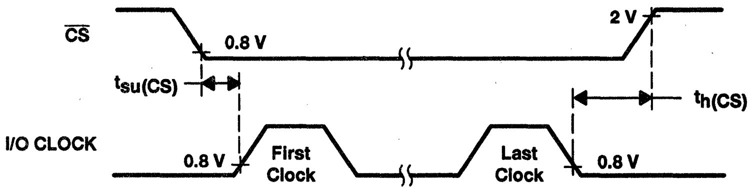


Figure 4. $\overline{CS}$ to I/O CLOCK Voltage Waveforms

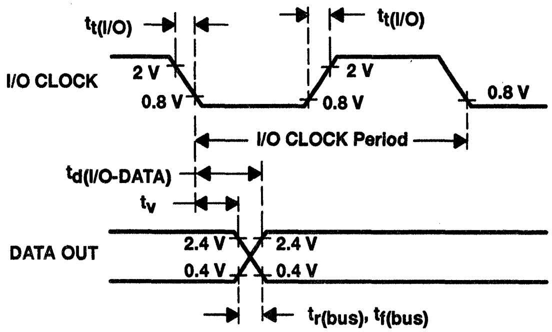


Figure 5. I/O CLOCK and DATA OUT Voltage Waveforms

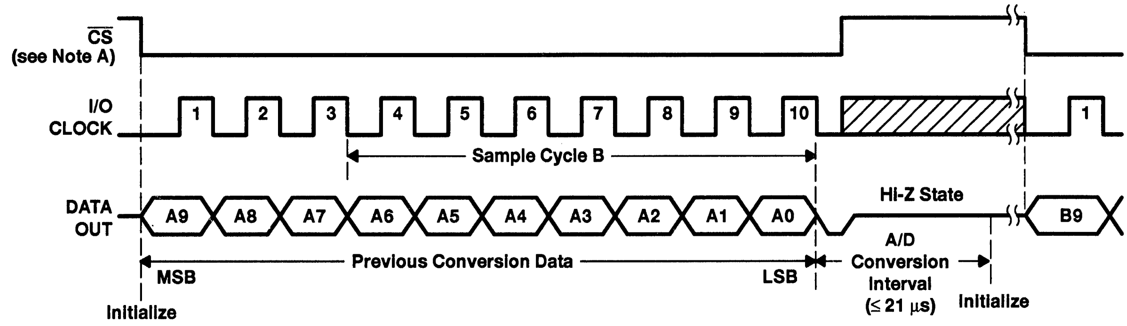


Figure 6. Timing for 10-Clock Transfer Using $\overline{CS}$

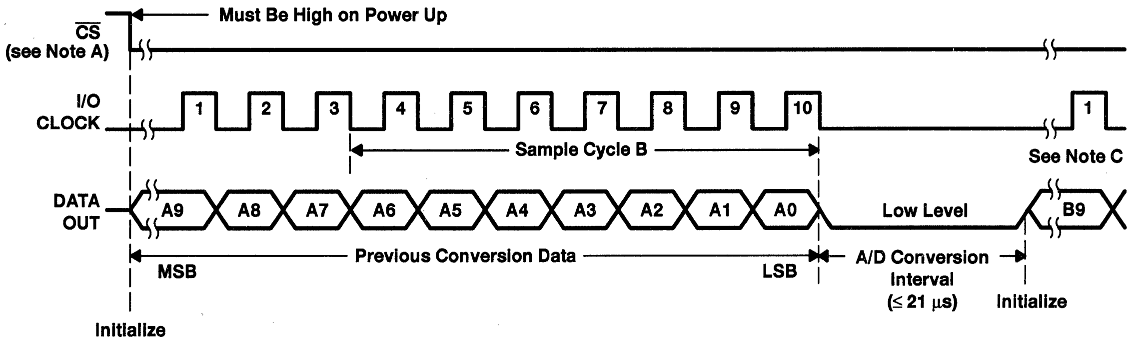


Figure 7. Timing for 10-Clock Transfer Not Using $\overline{CS}$

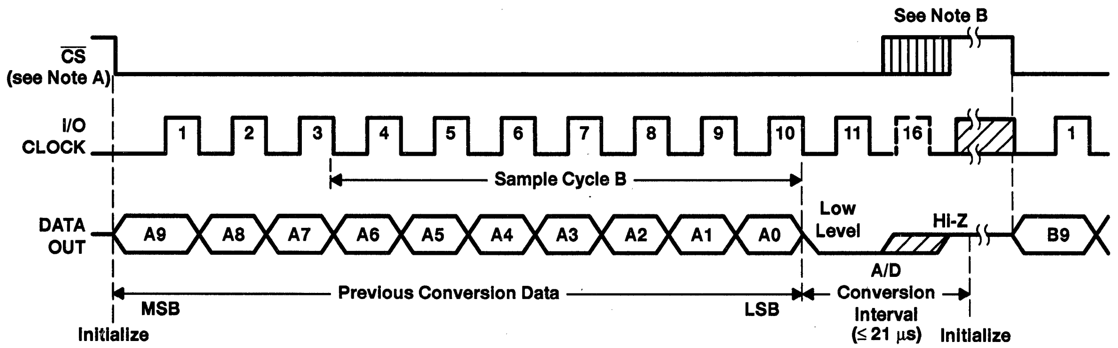


Figure 8. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$ (Serial Transfer Completed Within 21 µs)

NOTES: A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to the I/O CLOCK. No attempt should be made to clock out the data until the minimum $\overline{CS}$ setup time has elapsed.

B. A low-to-high transition of $\overline{CS}$ disables I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.

C. The first I/O CLOCK must occur after the end of the previous conversion.

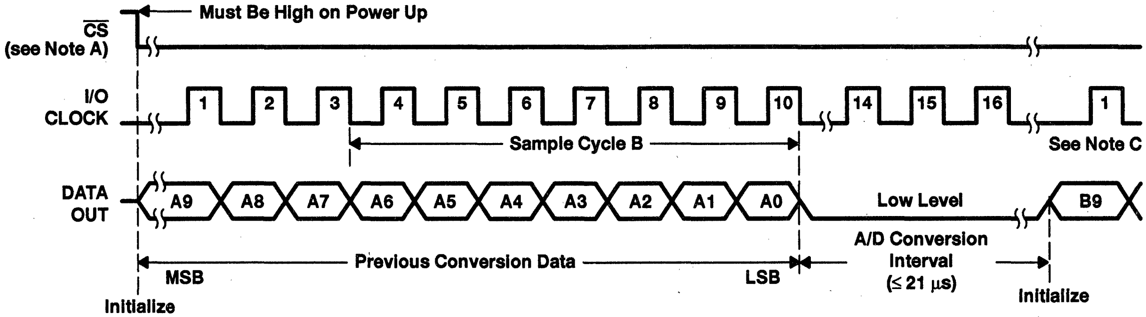


Figure 9. Timing for 16-Clock Transfer Not Using $\overline{CS}$ (Serial Transfer Completed Within 21 μs)

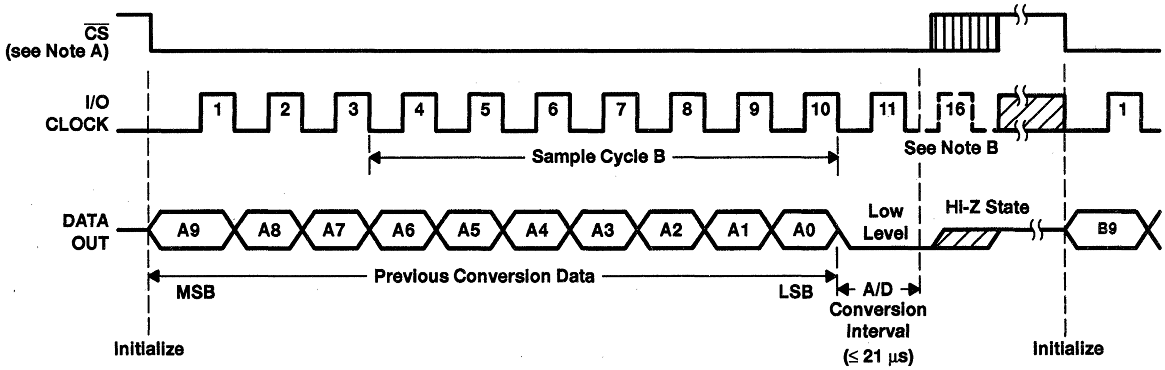


Figure 10. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$ (Serial Transfer Completed After 21 μs)

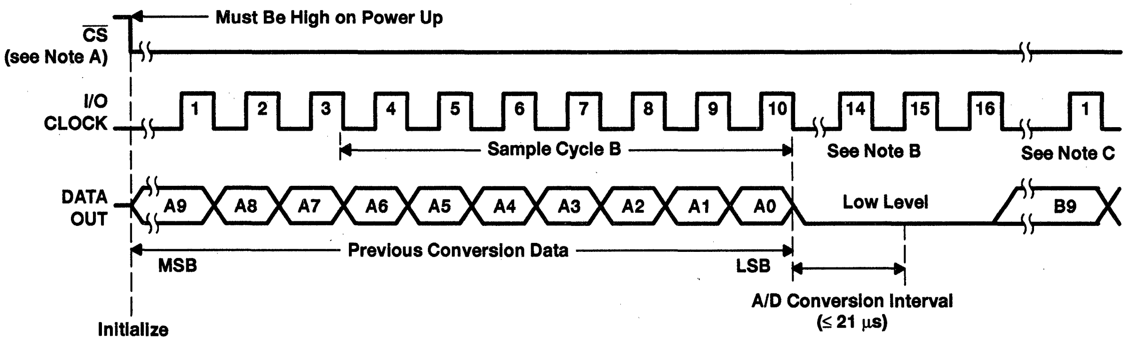


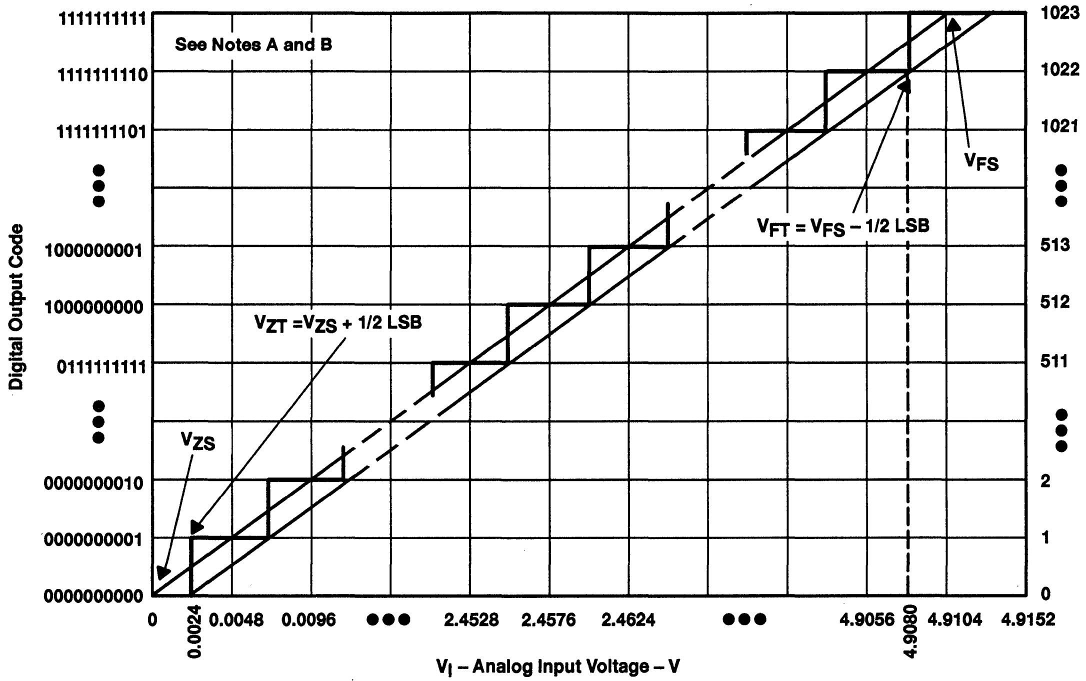
Figure 11. Timing for 16-Clock Transfer Not Using $\overline{CS}$ (Serial Transfer Completed After 21 μs)

NOTES: A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a set up time plus two falling edges of the internal system clock after $\overline{CS}$↓ before responding to the I/O CLOCK. No attempt should be made to clock out the data until the minimum $\overline{CS}$ setup time has elapsed.

B. A low-to-high transition of $\overline{CS}$ disables I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.

C. The first I/O CLOCK must occur after the end of the previous conversion.

APPLICATION INFORMATION



NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0024 V and the transition to full scale (V_{FT}) is 4.908 V. 1 LSB = 4.8 mV.

B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 12. Ideal Conversion Characteristics

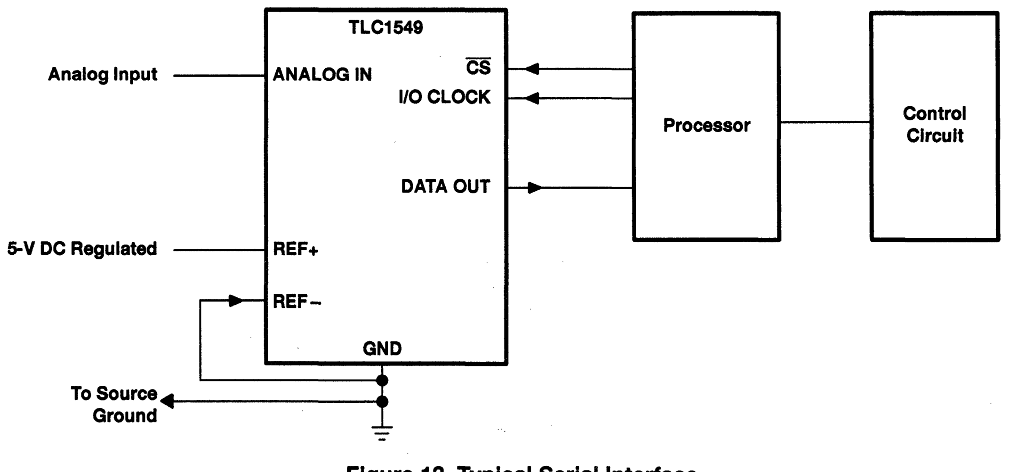


Figure 13. Typical Serial Interface

APPLICATION INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 14, the time required to charge the analog input capacitance from 0 V to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S\left(1 - e^{-t_c/R_tC_i}\right) \tag{1}$$

where

$R_t = R_s + r_i$

The final voltage to 1/2 LSB is given by

$$V_C\ (1/2\ \text{LSB}) = V_S - (V_S/2048) \tag{2}$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - \left(V_S/2048\right) = V_S\left(1 - e^{-t_c/R_tC_i}\right) \tag{3}$$

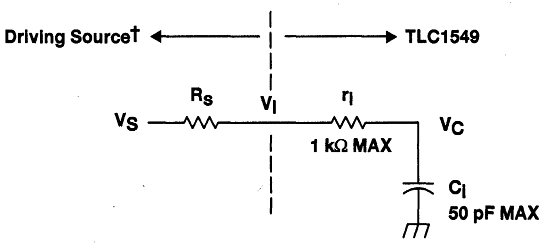
and

$$t_c\ (1/2\ \text{LSB}) = R_t \times C_i \times \ln(2048) \tag{4}$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c\ (1/2\ \text{LSB}) = (R_s + 1\ \text{k}\Omega) \times 60\ \text{pF} \times \ln(2048) \tag{5}$$

This time must be less than the converter sample time shown in the timing diagrams.



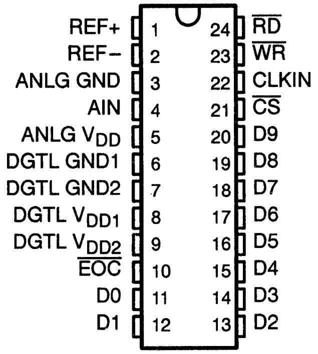
V_I = Input Voltage at ANALOG IN
V_S = External Driving Source Voltage
R_s = Source Resistance
r_I = Input Resistance
C_I = Input Capacitance

† Driving source requirements:
- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_s must be real at the input frequency.

Figure 14. Equivalent Input Circuit Including the Driving Source

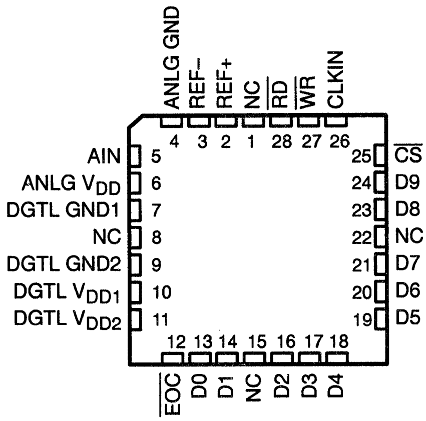
- **Power Dissipation . . . 40 mW Max**
- **Advanced LinEPIC™ Single-Poly Process Provides Close Capacitor Matching for Better Accuracy**
- **Fast Parallel Processing for DSP and μP Interface**
- **Either External or Internal Clock Can Be Used**
- **Conversion Time . . . 6 μs**
- **Total Unadjusted Error . . . ±1 LSB Max**
- **CMOS Technology**

J† OR NW PACKAGE
(TOP VIEW)



† Refer to the mechanical data for the JW package.

FK OR FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLC1550x and TLC1551 are data acquisition analog-to-digital converters (ADCs) using a 10-bit, switched-capacitor, successive-approximation network. A high-speed, 3-state parallel port directly interfaces to a digital signal processor (DSP) or microprocessor (μP) system data bus. D0 through D9 are the digital output terminals with D0 being the least significant bit (LSB). Separate power terminals for the analog and digital portions minimize noise pickup in the supply leads. Additionally, the digital power is divided into two parts to separate the lower current logic from the higher current bus drivers. An external clock can be applied to CLKIN to override the internal system clock if desired.

The TLC1550I and TLC1551I are characterized for operation from −40°C to 85°C. The TLC1550M is characterized over the full military range of −55°C to 125°C.

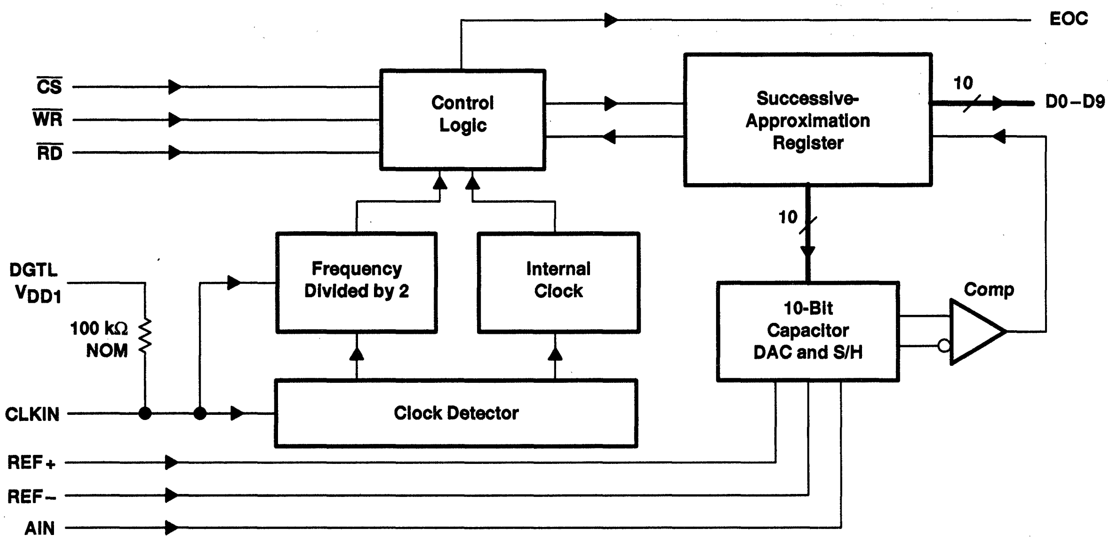
AVAILABLE OPTIONS

T_A	PACKAGE			
	CERAMIC CHIP CARRIER (FK)	PLASTIC CHIP CARRIER (FN)	CERAMIC DIP (J)	PLASTIC DIP (NW)
−40°C to 85°C	–	TLC1550IFN TLC1551IFN	–	TLC1550INW TLC1551INW
−55°C to 125°C	TLC1550MFK	–	TLC1550MJ	–

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground.

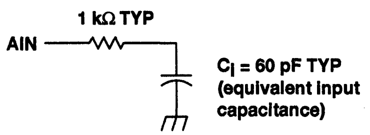
Advanced LinEPIC is a trademark of Texas Instruments Incorporated.

functional block diagram

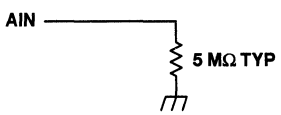


typical equivalent inputs

INPUT CIRCUIT IMPEDANCE DURING SAMPLING MODE



INPUT CIRCUIT IMPEDANCE DURING HOLD MODE



Terminal Functions

TERMINAL NAME	NO.†	NO.‡	DESCRIPTION
ANLG GND	4	3	Analog ground. The reference point for the voltage applied on terminals ANLG V_{DD}, AIN, REF+, and REF–.
AIN	5	4	Analog voltage input. The voltage applied to AIN is converted to the equivalent digital output.
ANLG V_{DD}	6	5	Analog positive power supply voltage. The voltage applied to this terminal is designated V_{DD3}.
CLKIN	26	22	Clock input. CLKIN is used for external clocking instead of using the internal system clock. It usually takes a few microseconds before the internal clock is disabled. To use the internal clock, CLKIN should be tied high or left unconnected.
$\overline{CS}$	25	21	Chip-select. $\overline{CS}$ must be low for $\overline{RD}$ or $\overline{WR}$ to be recognized by the A/D converter.
D0	13	11	Data bus output. D0 is bit 1 (LSB).
D1	14	12	Data bus output. D1 is bit 2.
D2	16	13	Data bus output. D2 is bit 3.
D3	17	14	Data bus output. D3 is bit 4.
D4	18	15	Data bus output. D4 is bit 5.
D5	19	16	Data bus output. D5 is bit 6.
D6	20	17	Data bus output. D6 is bit 7.
D7	21	18	Data bus output. D7 is bit 8.
D8	23	19	Data bus output. D8 is bit 9.
D9	24	20	Data bus output. D9 is bit 10 (MSB).
DGTL GND1	7	6	Digital ground 1. The ground for power supply DGTL V_{DD1} and is the substrate connection.
DGTL GND2	9	7	Digital ground 2. The ground for power supply DGTL V_{DD2}.
DGTL V_{DD1}	10	8	Digital positive power-supply voltage 1. DGTL V_{DD1} supplies the logic. The voltage applied to DGTL V_{DD1} is designated V_{DD1}.
DGTL V_{DD2}	11	9	Digital positive power-supply voltage 2. DGTL V_{DD2} supplies only the higher-current output buffers. The voltage applied to DGTL V_{DD2} is designated V_{DD2}.
$\overline{EOC}$	12	10	End-of-conversion. $\overline{EOC}$ goes low indicating that conversion is complete and the results have been transferred to the output latch. $\overline{EOC}$ can be connected to the µP- or DSP-interrupt terminal or can be continuously polled.
$\overline{RD}$	28	24	Read input. When $\overline{CS}$ is low and $\overline{RD}$ is taken low, the data is placed on the data bus from the output latch. The output latch stores the conversion results at the most recent negative edge of $\overline{EOC}$. The falling edge of $\overline{RD}$ resets $\overline{EOC}$ to a high within the $t_{d(EOC)}$ specifications.
REF+	2	1	Positive voltage-reference input. Any analog input that is greater than or equal to the voltage on REF+ converts to 1111111111. Analog input voltages between REF+ and REF– convert to the appropriate result in a ratiometric manner.
REF–	3	2	Negative voltage reference input. Any analog input that is less than or equal to the voltage on REF– converts to 0000000000.
$\overline{WR}$	27	23	Write input. When $\overline{CS}$ is low, conversion is started on the rising edge of $\overline{WR}$. On this rising edge, the ADC holds the analog input until conversion is completed. Before and after the conversion period, which is given by t_{conv}, the ADC remains in the sampling mode.

† Terminal numbers for FK and FN packages.
‡ Terminal numbers for J and NW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD1}, V_{DD2}, and V_{DD3} (see Note 1)	6.5 V
Input voltage range, V_I (any input)	−0.3 V to V_{DD} + 0.3 V
Output voltage range, V_O	−0.3 V to V_{DD} + 0.3 V
Peak input current (any digital input)	±10 mA
Peak total input current (all inputs)	±30 mA
Operating free-air temperature range, T_A: TLC1550I, TLC1551I	−40°C to 85°C
TLC1550M	−55°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Case temperature for 10 seconds: FK or FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: J or NW package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: V_{DD1} is the voltage measured at DGTL V_{DD1} with respect to DGND1. V_{DD2} is the voltage measured at DGTL V_{DD2} with respect to the DGND2. V_{DD3} is the voltage measured at ANLG V_{DD} with respect to AGND. For these specifications, all ground terminals are tied together (and represent 0 V). When V_{DD1}, V_{DD2}, and V_{DD3} are equal, they are referred to simply as V_{DD}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD1}, V_{DD2}, V_{DD3}		4.75	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)			V_{DD3}		V
Negative reference voltage, V_{ref-} (see Note 2)			0		V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)			0.3	0.3	V
Analog input voltage range		0		V_{DD3}	V
High-level control input voltage, V_{IH}		2			V
Low-level control input voltage, V_{IL}				0.8	V
Input clock frequency, $f_{(CLKIN)}$		0.5		7.8	MHz
Setup time, $\overline{CS}$ low before $\overline{WR}$ or $\overline{RD}$ goes low, $t_{su(CS)}$		0			ns
Hold time, $\overline{CS}$ low after $\overline{WR}$ or $\overline{RD}$ goes high, $t_{h(CS)}$		0			ns
$\overline{WR}$ or $\overline{RD}$ pulse duration, $t_{w(WR)}$		50			ns
Input clock low pulse duration, $t_{wL(CLKIN)}$		40% of period		80% of period	
Operating free-air temperature, T_A	TLC155xI	−40		85	°C
	TLC1550M	−55		125	°C

NOTE 2: Analog input voltages greater than that applied to REF+ convert to all 1s (1111111111), while input voltages less than that applied to REF− convert to all 0s (0000000000). The total unadjusted error may increase as this differential voltage falls below 4.75 V.

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = V_{ref+} = 4.75$ to 5.5 V and $V_{ref-} = 0$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} = 4.75 V,	I_{OH} = −360 μA	2.4			V
V_{OL}	Low-level output voltage	V_{DD} = 4.75 V, I_{OL} = 2.4 mA	T_A = 25°C			0.4	V
			T_A = −55°C to 125°C			0.5	
I_{OZ}	Off-state (high-impedance-state) output current	$V_O = V_{DD}$,	$\overline{CS}$ and $\overline{RD}$ at V_{DD}			10	μA
		V_O = 0,	$\overline{CS}$ and $\overline{RD}$ at V_{DD}			−10	
I_{IH}	High-level input current	$V_I = V_{DD}$			0.005	2.5	μA
I_{IL}	Low-level input current (except CLKIN)	V_I = 0		−2.5	−0.005		μA
I_{IL}	Low-level input current (CLKIN)			−150	−50		μA
I_{OS}	Short-circuit output current	V_O = 5 V,	T_A = 25°C	7	14		mA
		V_O = 0,	T_A = 25°C		−12	−6	
I_{DD}	Operating supply current	$\overline{CS}$ low and $\overline{RD}$ high			2	8	mA
C_i	Input capacitance — Analog inputs	See typical equivalent inputs TLC1550/1I			60	90*	pF
	Input capacitance — Digital inputs				5	15*	

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† All typical values are at V_{DD} = 5 V, T_A = 25°C.

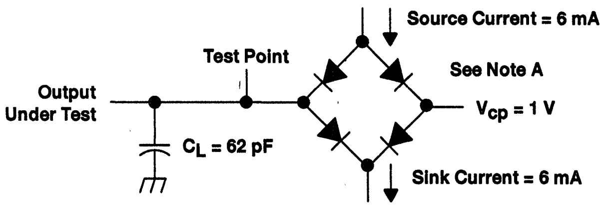
operating characteristics over recommended operating free-air temperature range with internal clock and minimum sampling time of 4 μs, $V_{DD} = V_{ref+} = 5$ V and $V_{ref-} = 0$ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP‡	MAX	UNIT
E_L	Linearity error	TLC1550I	See Note 3	Full range			±0.5	LSB
		TLC1551I		Full range			±1	
		TLC1550M		25°C			±0.5	
				Full range			±1	
E_{ZS}	Zero-scale error	TLC1550I	See Notes 2 and 4	Full range			±0.5	LSB
		TLC1551I		Full range			±1	
		TLC1550M		25°C			±0.5	
				Full range			±1	
E_{FS}	Full-scale error	TLC1550I	See Notes 2 and 4	Full range			±0.5	LSB
		TLC1551I		Full range			±1	
		TLC1550M		25°C			±0.5	
				Full range			±1	
	Total unadjusted error	TLC1550I	See Note 5	Full range			±0.5	LSB
		TLC1551I		Full range			±1	
		TLC1550M		25°C			±1	
t_{conv}	Conversion time		$f_{clock(external)}$ = 4.2 MHz or internal clock				6	μs
$t_{a(D)}$	Data access time after $\overline{RD}$ goes low		See Figure 3				35	ns
$t_{v(D)}$	Data valid time after $\overline{RD}$ goes high				5			ns
$t_{dis(D)}$	Disable time, delay time from $\overline{RD}$ high to high impedance						30	ns
$t_{d(EOC)}$	Delay time, $\overline{RD}$ low to $\overline{EOC}$ high				0	15		ns

† Full range is –40°C to 85°C for the TL155xI devices and –55°C to 125°C for the TLC1550M.
‡ All typical values are at V_{DD} = 5 V, T_A = 25°C.

NOTES: 2. Analog input voltages greater than that applied to REF+ convert to all 1s (1111111111), while input voltages less than that applied to REF– convert to all 0s (0000000000). The total unadjusted error may increase as this differential voltage falls below 4.75 V.
3. Linearity error is the difference between the actual analog value at the transition between any two adjacent steps and its ideal value after zero-scale error and full-scale error have been removed.
4. Zero-scale error is the difference between the actual mid-step value and the nominal mid-step value at specified zero scale. Full-scale error is the difference between the actual mid-step value and the nominal mid-step value at specified full scale.
5. Total unadjusted error is the difference between the actual analog value at the transition between any two adjacent steps and its ideal value. It includes contributions from zero-scale error, full-scale error, and linearity error.

PARAMETER MEASUREMENT INFORMATION



V_{cp} = voltage commutation point for switching between source and sink currents

NOTE A: Equivalent load circuit of the Teradyne A500 tester for timing parameter measurement

Figure 1. Test Load Circuit

APPLICATION INFORMATION

simplified analog input analysis

Using the circuit in Figure 2, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S\left(1-e^{-t_c/R_tC_i}\right) \qquad (1)$$

where

$R_t = R_s + r_i$

The final voltage to 1/2 LSB is given by

$$V_C\ (1/2\ \text{LSB}) = V_S - (V_S/1024) \qquad (2)$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - \left(V_S/512\right) = V_S\left(1-e^{-t_c/R_tC_i}\right) \qquad (3)$$

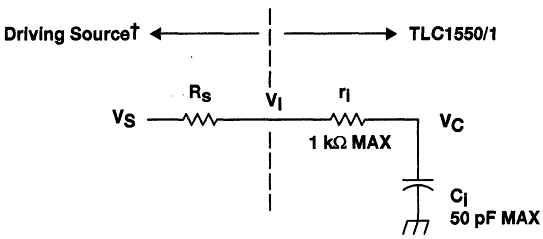
and

$$t_c\ (1/2\ \text{LSB}) = R_t \times C_i \times \ln(1024) \qquad (4)$$

Therefore, with the values given, the time for the analog input signal to settle is

$$t_c\ (1/2\ \text{LSB}) = (R_s + 1\ \text{k}\Omega) \times 60\ \text{pF} \times \ln(1024) \qquad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input voltage at AIN
V_S = External driving source voltage
R_s = Source resistance
r_i = Input resistance
C_I = Input capacitance

† Driving source requirements:
- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_s must be real at the input frequency.

Figure 2. Input Circuit Including the Driving Source

PRINCIPLES OF OPERATION

The operating sequence for complete data acquisition is shown in Figure 3. Processors can address the TLC1550 and TLC1551 as an external memory device by simply connecting the address lines to a decoder and the decoder output to $\overline{CS}$. Like other peripheral devices, the write ($\overline{WR}$) and read ($\overline{RD}$) input signals are valid only when $\overline{CS}$ is low. Once $\overline{CS}$ is low, the on-board system clock permits the conversion to begin with a simple write command and the converted data to be presented to the data bus with a simple read command. The device remains in a sampling (track) mode from the rising edge of $\overline{EOC}$ until conversion begins with the rising edge of $\overline{WR}$, which initiates the hold mode. After the hold mode begins, the clock controls the conversion automatically. When the conversion is complete, the end-of-conversion ($\overline{EOC}$) signal goes low indicating that the digital data has been transferred to the output latch. Lowering $\overline{CS}$ and $\overline{RD}$ then resets $\overline{EOC}$ and transfers the data to the data bus for the processor read cycle.

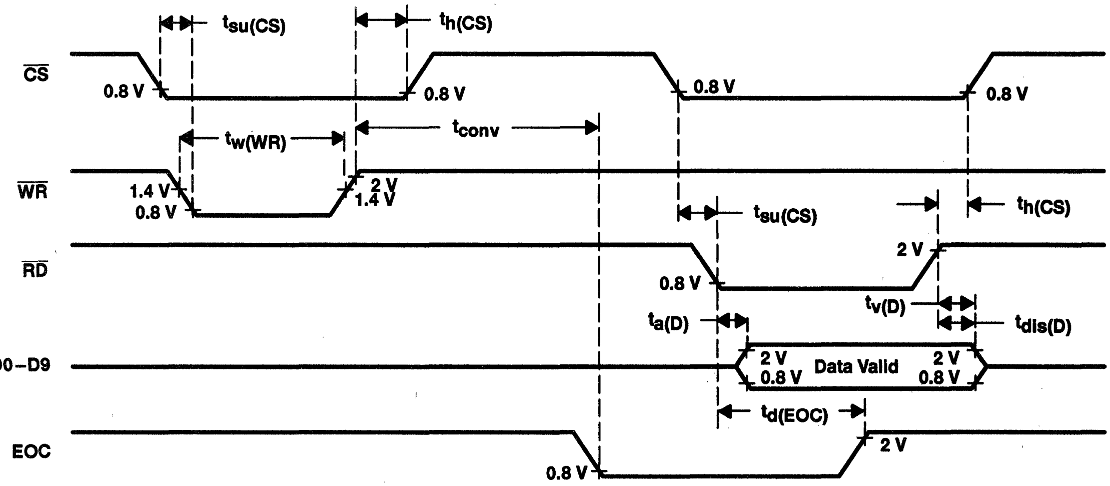
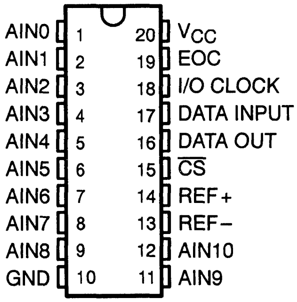


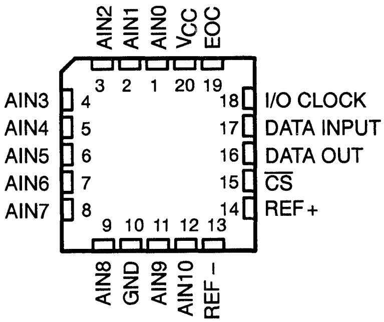
Figure 3. TLC1550 or TLC1551 Operating Sequence

- **12-Bit-Resolution A/D Converter**
- **10-μs Conversion Time Over Operating Temperature**
- **11 Analog Input Channels**
- **3 Built-In Self-Test Modes**
- **Inherent Sample and Hold**
- **Linearity Error . . . ±1 LSB Max**
- **On-Chip System Clock**
- **End-of-Conversion (EOC) Output**
- **Unipolar or Bipolar Output Operation (Signed Binary With Respect to 1/2 the Applied Voltage Reference)**
- **Programmable MSB or LSB First**
- **Programmable Power Down**
- **Programmable Output Data Length**
- **CMOS Technology**
- **Application Report Available†**

DB, DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TLC2543C and TLC2543I are 12-bit, switched-capacitor, successive-approximation, analog-to-digital converters. Each device has three control inputs [chip select ($\overline{CS}$), the input-output clock (I/O CLOCK), and the address input (DATA INPUT)] and is designed for communication with the serial port of a host processor or peripheral through a serial 3-state output. The device allows high-speed data transfers from the host.

In addition to the high-speed converter and versatile control capability, the device has an on-chip 14-channel multiplexer that can select any one of 11 inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of conversion, the end-of-conversion (EOC) output goes high to indicate that conversion is complete. The converter incorporated in the device features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating temperature range.

The TLC2543 is available in the DB, DW, FN, and N packages. The TLC2543C is characterized for operation from 0°C to 70°C, and the TLC2543I is characterized for operation from –40°C to 85°C.

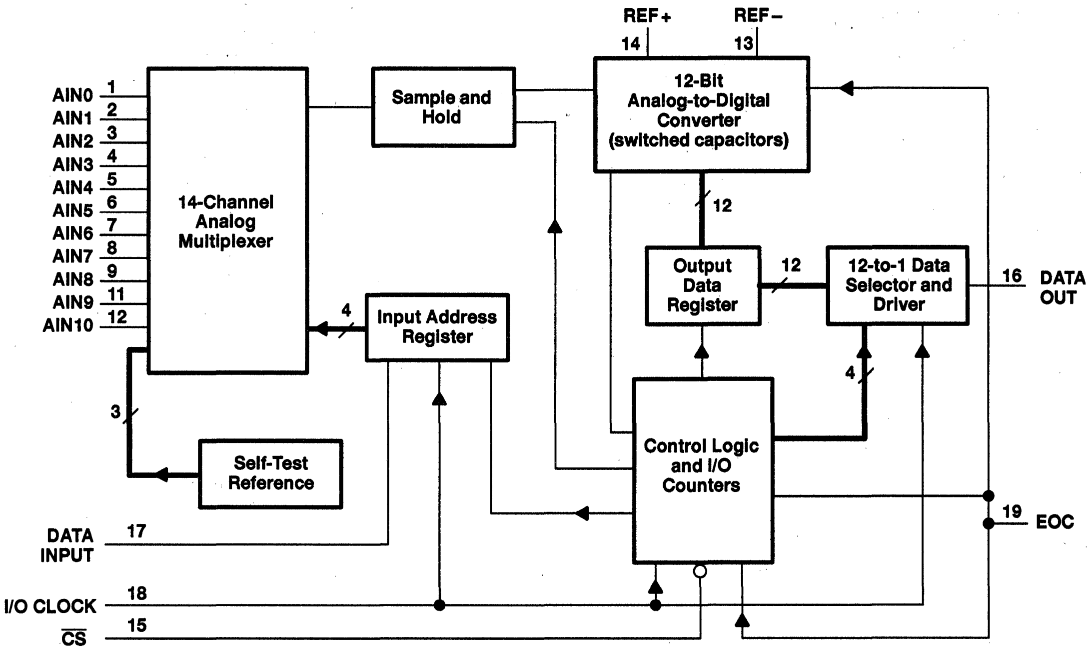
AVAILABLE OPTIONS

T_A	PACKAGE			
	SMALL OUTLINE (DB)‡	SMALL OUTLINE (DW)	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	TLC2543CDB	TLC2543CDW	TLC2543CFN	TLC2543CN
–40°C to 85°C	TLC2543IDB	TLC2543IDW	TLC2543IFN	TLC2543IN

‡ Available in tape and reel and ordered as the TLC2543CDBR or TLC2543IDBR.

† Microcontroller Based Data Acquisition Using the TLC2543 12-bit Serial-Out ADC (SLAA012)

functional block diagram



TEXAS INSTRUMENTS
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Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AIN0 – AIN10	1–9, 11, 12	I	These 11 analog-signal inputs are internally multiplexed. The driving source impedance should be less than or equal to 50 Ω for 4.1-MHz I/O CLOCK operation and capable of slewing the analog input voltage into a capacitance of 60 pF.
$\overline{CS}$	15	I	Chip select. A high-to-low transition on $\overline{CS}$ resets the internal counters and controls and enables DATA OUT, DATA INPUT, and I/O CLOCK. A low-to-high transition disables DATA INPUT and I/O CLOCK within a setup time.
DATA INPUT	17	I	Serial-data input. A 4-bit serial address selects the desired analog input or test voltage to be converted next. The serial data is presented with the MSB first and is shifted in on the first four rising edges of I/O CLOCK. After the four address bits are read into the address register, I/O CLOCK clocks the remaining bits in order.
DATA OUT	16	O	The 3-state serial output for the A/D conversion result. DATA OUT is in the high-impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low. With a valid $\overline{CS}$, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB/LSB value of the previous conversion result. The next falling edge of I/O CLOCK drives DATA OUT to the logic level corresponding to the next MSB/LSB, and the remaining bits are shifted out in order.
EOC	19	O	End of conversion goes from a high to a low logic level after the falling edge of the last I/O CLOCK and remains low until the conversion is complete and data are ready for transfer.
GND	10		The ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
I/O CLOCK	18	I	Input/output clock. I/O CLOCK receives the serial input and performs the following four functions: 1. It clocks the eight input data bits into the input data register on the first eight rising edges of I/O CLOCK with the multiplexer address available after the fourth rising edge. 2. On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplexer input begins charging the capacitor array and continues to do so until the last falling edge of I/O CLOCK. 3. It shifts the 11 remaining bits of the previous conversion data out on DATA OUT. Data changes on the falling edge of I/O CLOCK. 4. It transfers control of the conversion to the internal state controller on the falling edge of the last I/O CLOCK.
REF+	14	I	The upper reference voltage value (nominally V_{CC}) is applied to REF+. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to the REF– terminal.
REF–	13	I	The lower reference voltage value (nominally ground) is applied to REF–.
V_{CC}	20		Positive supply voltage

detailed description

Initially, with chip select ($\overline{CS}$) high, I/O CLOCK and DATA INPUT are disabled and DATA OUT is in the high-impedance state. $\overline{CS}$, going low, begins the conversion sequence by enabling I/O CLOCK and DATA INPUT and removes DATA OUT from the high-impedance state.

The input data is an 8-bit data stream consisting of a 4-bit analog channel address (D7–D4), a 2-bit data length select (D3–D2), an output MSB or LSB first bit (D1), and a unipolar or bipolar output select bit (D0) that are applied to DATA INPUT. The I/O CLOCK sequence applied to the I/O CLOCK terminal transfers this data to the input data register.

During this transfer, the I/O CLOCK sequence also shifts the previous conversion result from the output data register to DATA OUT. I/O CLOCK receives the input sequence of 8, 12, or 16 clocks long depending on the data-length selection in the input data register. Sampling of the analog input begins on the fourth falling edge of the input I/O CLOCK sequence and is held after the last falling edge of the I/O CLOCK sequence. The last falling edge of the I/O CLOCK sequence also takes EOC low and begins the conversion.

converter operation

The operation of the converter is organized as a succession of two distinct cycles: 1) the I/O cycle and 2) the actual conversion cycle. The I/O cycle is defined by the externally provided I/O CLOCK and lasts 8, 12, or 16 clock periods, depending on the selected output data length.

1. I/O cycle

   During the I/O cycle, two operations take place simultaneously.

   a. An 8-bit data stream consisting of address and control information is provided to DATA INPUT. This data is shifted into the device on the rising edge of the first eight I/O CLOCKs. DATA INPUT is ignored after the first eight clocks during 12 or 16 clock I/O transfers.

   b. The data output, with a length of 8, 12, or 16 bits, is provided serially on DATA OUT. If $\overline{CS}$ is held low, the first output data bit occurs on the rising edge of EOC. If $\overline{CS}$ is negated between conversions, the first output data bit occurs on the falling edge of $\overline{CS}$. This data is the result of the previous conversion period, and after the first output data bit, each succeeding bit is clocked out on the falling edge of each succeeding I/O CLOCK.

2. Conversion cycle

   The conversion cycle is transparent to the user, and it is controlled by an internal clock synchronized to I/O CLOCK. During the conversion period, the device performs a successive-approximation conversion on the analog input voltage. The EOC output goes low at the start of the conversion cycle and goes high when conversion is complete and the output data register is latched. A conversion cycle is started only after the I/O cycle is completed, which minimizes the influence of external digital noise on the accuracy of the conversion.

power up and initialization

After power up, $\overline{CS}$ must be taken from high to low to begin an I/O cycle. EOC is initially high, and the input data register is set to all zeroes. The contents of the output data register are random, and the first conversion result should be ignored. To initialize during operation, $\overline{CS}$ is taken high and returned low to begin the next I/O cycle. The first conversion after the device has returned from the power-down state may not read accurately due to internal device settling.

operational terminology

Current (N) I/O cycle	The entire I/O CLOCK sequence that transfers address and control data into the data register and clocks the digital result from the previous conversion from DATA OUT
Current (N) conversion cycle	The conversion cycle starts immediately after the current I/O cycle. The end of the current I/O cycle is the last clock falling edge in the I/O CLOCK sequence. The current conversion result is loaded into the output register when conversion is complete.
Current (N) conversion result	The current conversion result is serially shifted out on the next I/O cycle.
Previous (N−1) conversion cycle	The conversion cycle just prior to the current I/O cycle
Next (N+1) I/O cycle	The I/O period that follows the current conversion cycle

Example: In the 12-bit mode, the result of the current conversion cycle is a 12-bit serial-data stream clocked out during the next I/O cycle. The current I/O cycle must be exactly 12 bits long to maintain synchronization, even if this corrupts the output data from the previous conversion. The current conversion is begun immediately after the twelfth falling edge of the current I/O cycle.

data input

The data input is internally connected to an 8-bit serial-input address and control register. The register defines the operation of the converter and the output data length. The host provides the data word with the MSB first. Each data bit is clocked in on the rising edge of the I/O CLOCK sequence (see Table 1 for the data register format).

data input address bits

The four MSBs (D7 – D4) of the data register are used to address one of the 11 input channels, a reference-test voltage, or the power-down mode. The address bits affect the current conversion, which is the conversion that immediately follows the current I/O cycle. The reference voltage is nominally equal to $V_{ref+} - V_{ref-}$.

data output length

The next two bits (D3 and D2) of the data register select the output data length. The data-length selection is valid for the current I/O cycle (the cycle in which the data is read). The data-length selection, being valid for the current I/O cycle, allows device startup without losing I/O synchronization. A data length of 8, 12, or 16 bits can be selected. Since the converter has 12-bit resolution, a data length of 12 bits is suggested.

With D3 and D2 set to 00 or 10, the device is in the 12-bit data-length mode and the result of the current conversion is output as a 12-bit serial-data stream during the next I/O cycle. The current I/O cycle must be exactly 12 bits long for proper synchronization, even if this means corrupting the output data from a previous conversion. The current conversion is started immediately after the twelfth falling edge of the current I/O cycle.

With bits D3 and D2 set to 11, the 16-bit data-length mode is selected, which allows convenient communication with 16-bit serial interfaces. In the 16-bit mode, the result of the current conversion is output as a 16-bit serial-data stream during the next I/O cycle with the four LSBs always set to 0 (pad bits). The current I/O cycle must be exactly 16 bits long to maintain synchronization even if this means corrupting the output data from the previous conversion. The current conversion is immediately started after the sixteenth falling edge of the current I/O cycle.

With bits D3 and D2 set to 01, the 8-bit data-length mode is selected, which allows fast communication with 8-bit serial interfaces. In the 8-bit mode, the result of the current conversion is output as an 8-bit serial-data stream during the next I/O cycle. The current I/O cycle must be exactly 8 bits long to maintain synchronization, even if this means corrupting the output data from the previous conversion. The four LSBs of the conversion result are truncated and discarded. The current conversion is immediately started after the eighth falling edge of the current I/O cycle.

Since D3 and D2 take effect on the current I/O cycle when the data length is programmed, there can be a conflict with the previous cycle when the data-word length is changed from one cycle to the next. This may occur when the data format is selected to be least significant bit first, since at the time the data length change becomes effective (six rising edges of I/O CLOCK), the previous conversion result has already started shifting out.

In actual operation, if different data lengths are required within an application and the data length is changed between two conversions, no more than one conversion result can be corrupted and only if it is shifted out in LSB first format.

sampling period

During the sampling period, one of the analog inputs is internally connected to the capacitor array of the converter to store the analog input signal. The converter starts sampling the selected input immediately after the four address bits have been clocked into the input data register. Sampling starts on the fourth falling edge of I/O CLOCK. The converter remains in the sampling mode until the eighth, twelfth, or sixteenth falling edge of the I/O CLOCK depending on the data-length selection. After the EOC delay time from the last I/O CLOCK falling edge, the EOC output goes low indicating that the sampling period is over and the conversion period has begun. After EOC goes low, the analog input can be changed without affecting the conversion result. Since the delay from the falling edge of the last I/O CLOCK to EOC low is fixed, time-varying analog input signals can be digitized at a fixed rate without introducing systematic harmonic distortion or noise due to timing uncertainty.

After the 8-bit data stream has been clocked in, DATA INPUT should be held at a fixed digital level until EOC goes high (indicating the conversion is complete) to maximize the sampling accuracy and minimize the influence of external digital noise.

data register, LSB first

D1 in the input data register (LSB first) is used to control the direction of the output binary data transfer. When D1 is set to 0, the conversion result is shifted out MSB first. When set to 1, the data is shifted out LSB first. Selection of MSB first or LSB first always affects the next I/O cycle and not the current I/O cycle. When changing from one data direction to another, the current I/O cycle is never disrupted.

data register, bipolar format

D0 in the input data register (BIP) is used to control the binary data format used to represent the conversion result. When D0 is set to 0, the conversion result is represented as unipolar (unsigned binary) data. Nominally, the conversion result of an input voltage equal to V_{ref-} is a code of all zeros (000 . . . 0), the conversion result of an input voltage equal to V_{ref+} is a code of all ones (111 . . . 1), and the conversion result of $(V_{ref+} + V_{ref-})/2$ is a code of a one followed by zeros (100 . . . 0).

When D0 is set to 1, the conversion result is represented as bipolar (signed binary) data. Nominally, conversion of an input voltage equal to V_{ref-} is a code of a 1 followed by zeros (100 . . . 0), conversion of an input voltage equal to V_{ref+} is a code of a 0 followed by all ones (011 . . . 1), and the conversion of $(V_{ref+} + V_{ref-})/2$ is a code of all zeros (000 . . . 0). The MSB is interpreted as the sign bit. The bipolar data format is related to the unipolar format in that the MSBs are always each other's complement.

Selection of the unipolar or bipolar format always affects the current conversion cycle, and the result is output during the next I/O cycle. When changing between unipolar and bipolar formats, the data output during the current I/O cycle is not affected.

EOC output

The EOC signal indicates the beginning and the end of conversion. In the reset state, EOC is always high. During the sampling period (beginning after the 4th falling edge of the I/O CLOCK sequence), EOC remains high until the internal sampling switch of the converter is safely opened. The opening of the sampling switch occurs after the eighth, twelfth, or sixteenth I/O CLOCK falling edge, depending on the data-length selection in the input data register. After the EOC signal goes low, the analog input signal can be changed without affecting the conversion result.

The EOC signal goes high again after the conversion is completed and the conversion result is latched into the output data register. The rising edge of EOC returns the converter to a reset state and a new I/O cycle begins. On the rising edge of EOC, the first bit of the current conversion result is on DATA OUT if $\overline{CS}$ is low. If $\overline{CS}$ is negated between conversions, the first bit of the current conversion result occurs at DATA OUT on the falling edge of $\overline{CS}$.

data format and pad bits

D3 and D2 of the input data register determine the number of significant bits in the digital output that represent the conversion result. The LSB-first bit determines the direction of the data transfer while the BIP bit determines the arithmetic conversion. The numerical data is always justified toward the MSB in any output format.

The internal conversion result is always 12 bits long. When an 8-bit data transfer is selected, the four LSBs of the internal result are discarded to provide a faster one-byte transfer. When a 12-bit transfer is used, all bits are transferred. When a 16-bit transfer is used, four LSB pad bits are always appended to the internal conversion result. In the LSB-first mode, four leading zeros are output. In the MSB-first mode, the last four bits output are zeros.

When $\overline{CS}$ is held low continuously, the first data bit of the just completed conversion occurs on DATA OUT on the rising edge of EOC. When a new conversion is started after the last falling edge of I/O CLOCK, EOC goes low and the serial output is forced to a logic zero until EOC goes high again.

When $\overline{CS}$ is negated between conversions, the first data bit occurs on DATA OUT on the falling edge of $\overline{CS}$. On each subsequent falling edge of I/O CLOCK after the first data bit appears, the data is changed to the next bit in the serial conversion result until the required number of bits has been output.

chip-select input ($\overline{CS}$)

The chip-select input ($\overline{CS}$) is used to enable and disable the device. During normal operation, $\overline{CS}$ should be low. Although the use of $\overline{CS}$ is not necessary to synchronize a data transfer, it can be brought high between conversions to coordinate the data transfer of several devices sharing the same bus.

When $\overline{CS}$ is brought high, the serial-data output is immediately brought to the high-impedance state, releasing its output data line to other devices that may share it. After an internally generated debounce time, I/O CLOCK is inhibited, thus preventing any further change in the internal state.

When $\overline{CS}$ is subsequently brought low again, the device is reset. $\overline{CS}$ must be held low for an internal debounce time before the reset operation takes effect. After $\overline{CS}$ is debounced low, I/O CLOCK must remain inactive (low) for a minimum time before a new I/O cycle can start.

$\overline{CS}$ can be used to interrupt any ongoing data transfer or any ongoing conversion. If $\overline{CS}$ is debounced low long enough before the end of the current conversion cycle, the previous conversion result is saved in the internal output buffer and shifted out during the next I/O cycle.

power-down features

When a binary address of 1110 is clocked into the input data register during the first four I/O CLOCK cycles, the power-down mode is selected. Power down is activated on the falling edge of the fourth I/O CLOCK pulse.

During power down, all internal circuitry is put in a low-current standby mode. No conversions are performed, and the internal output buffer keeps the previous conversion cycle data results, provided that all digital inputs are held above V_{CC} – 0.5 V or below 0.5 V. The I/O logic remains active so the current I/O cycle must be completed even when the power-down mode is selected. Upon power-on reset and before the first I/O cycle, the converter normally begins in the power-down mode. The device remains in the power-down mode until a valid (other than 1110) input address is clocked in. Upon completion of that I/O cycle, a normal conversion is performed with the results being shifted out during the next I/O cycle.

analog input, test, and power-down mode

The 11 analog inputs, three internal voltages, and power-down mode are selected by the input multiplexer according to the input addresses shown in Tables 2, 3, and 4. The input multiplexer is a break-before-make type to reduce input-to-input noise rejection resulting from channel switching. Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK and continues for the remaining I/O CLOCK pulses. The sample is held on the falling edge of the last I/O CLOCK pulse. The three internal test inputs are applied to the multiplexer, sampled, and converted in the same manner as the external analog inputs. The first conversion after the device has returned from the power-down state may not read accurately due to internal device settling.

Table 1. Input-Register Format

FUNCTION SELECT	INPUT DATA BYTE							
	ADDRESS BITS				L1	L0	LSBF	BIP
	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
Select input channel								
AIN0	0	0	0	0				
AIN1	0	0	0	1				
AIN2	0	0	1	0				
AIN3	0	0	1	1				
AIN4	0	1	0	0				
AIN5	0	1	0	1				
AIN6	0	1	1	0				
AIN7	0	1	1	1				
AIN8	1	0	0	0				
AIN9	1	0	0	1				
AIN10	1	0	1	0				
Select test voltage								
$(V_{ref+} - V_{ref-})/2$	1	0	1	1				
V_{ref-}	1	1	0	0				
V_{ref+}	1	1	0	1				
Software power down	1	1	1	0				
Output data length								
8 bits					0	1		
12 bits					X	0		
16 bits					1	1		
Output data format								
MSB first							0	
LSB first							1	
Unipolar (binary)								0
Bipolar (2s complement)								1

Table 2. Analog-Channel-Select Address

ANALOG INPUT SELECTED	VALUE SHIFTED INTO DATA INPUT	
	BINARY	HEX
AIN0	0000	0
AIN1	0001	1
AIN2	0010	2
AIN3	0011	3
AIN4	0100	4
AIN5	0101	5
AIN6	0110	6
AIN7	0111	7
AIN8	1000	8
AIN9	1001	9
AIN10	1010	A

Table 3. Test-Mode-Select Address

INTERNAL SELF-TEST VOLTAGE SELECTED†	VALUE SHIFTED INTO DATA INPUT		UNIPOLAR OUTPUT RESULT (HEX)‡
	BINARY	HEX	
$\frac{V_{ref+} - V_{ref-}}{2}$	1011	B	200
V_{ref-}	1100	C	000
V_{ref+}	1101	D	3FF

† V_{ref+} is the voltage applied to REF+, and V_{ref-} is the voltage applied to REF–.
‡ The output results shown are the ideal values and may vary with the reference stability and with internal offsets.

Table 4. Power-Down-Select Address

INPUT COMMAND	VALUE SHIFTED INTO DATA INPUT		RESULT
	BINARY	HEX	
Power down	1110	E	$I_{CC} \le 25\ \mu A$

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF–) voltage. In the switching sequence, 12 capacitors are examined separately until all 12 bits are identified and the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 4096). Node 4096 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF–. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half V_{CC}), a bit 0 is placed in the output register and the 4096-weight capacitor is switched to REF–. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and this 4096-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 2048-weight capacitor, the 1024-weight capacitor, and so forth, down the line until all bits are determined. With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to determine the bits from MSB to LSB.

reference voltage inputs

There are two reference inputs used with the device, the voltages applied to the REF+ and REF– terminals. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero-scale reading, respectively. These voltages and the analog input should not exceed the positive supply or be lower than ground consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ terminal voltage and at zero when the input signal is equal to or lower than REF– terminal voltage.

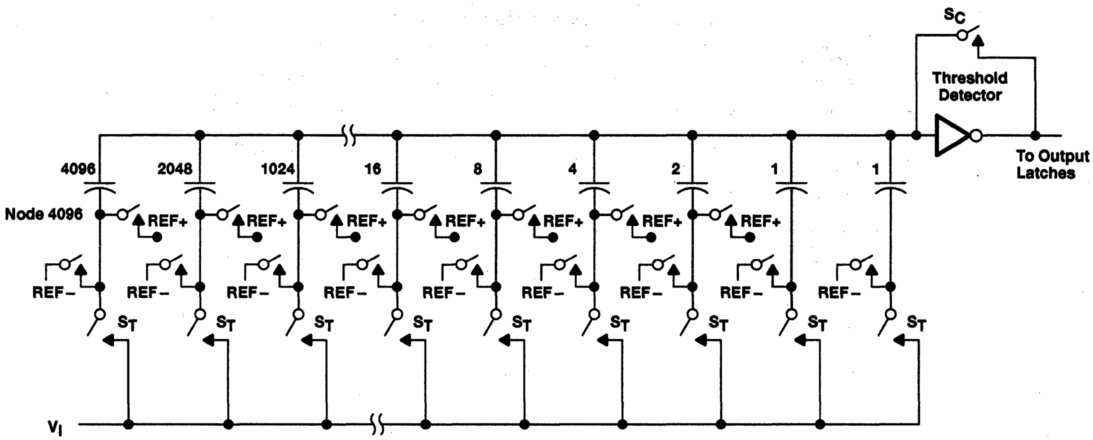


Figure 1. Simplified Model of the Successive-Approximation System

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.5 V to 6.5 V
Input voltage range, V_I (any input)	−0.3 V to V_{CC} + 0.3 V
Output voltage range, V_O	−0.3 V to V_{CC} + 0.3 V
Positive reference voltage, V_{ref+}	V_{CC} + 0.1 V
Negative reference voltage, V_{ref-}	−0.1 V
Peak input current, I_I (any input)	±20 mA
Peak total input current, I_I (all inputs)	±30 mA
Operating free-air temperature range, T_A: TLC2543C	0°C to 70°C
TLC2543I	−40°C to 85°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminal with REF– and GND wired together (unless otherwise noted).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)			V_{CC}		V
Negative reference voltage, V_{ref-} (see Note 2)			0		V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)		2.5	V_{CC}	$V_{CC}+0.1$	V
Analog input voltage (see Note 2)		0		V_{CC}	V
High-level control input voltage, V_{IH}	V_{CC} = 4.5 V to 5.5 V	2			V
Low-level control input voltage, V_{IL}	V_{CC} = 4.5 V to 5.5 V			0.8	V
Clock frequency at I/O CLOCK		0		4.1	MHz
Setup time, address bits at DATA INPUT before I/O CLOCK↑, $t_{su(A)}$ (see Figure 5)		100			ns
Hold time, address bits after I/O CLOCK↑, $t_{h(A)}$ (see Figure 5)		0			ns
Hold time, $\overline{CS}$ low after last I/O CLOCK↓, $t_{h(CS)}$ (see Figure 6)		0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3 and Figure 6)		1.425			µs
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$		120			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$		120			ns
Transition time, I/O CLOCK, $t_{t(I/O)}$ (see Note 4 and Figure 7)				1	µs
Transition time, DATA INPUT and $\overline{CS}$, $t_{t(CS)}$				10	µs
Operating free-air temperature, T_A	TLC2543C	0		70	°C
	TLC2543I	–40		85	°C

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (111111111111), while input voltages less than that applied to REF– convert as all zeros (000000000000).
3. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for a setup time after $\overline{CS}$↓ before responding to control input signals. No attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.
4. This is the time required for the clock input signal to fall from V_{IH}min to V_{IL}max or to rise from V_{IL}max to V_{IH}min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 4.5 V to 5.5 V, I/O CLOCK frequency = 4.1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = –1.6 mA	2.4			V
		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –20 µA	V_{CC}–0.1			
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 1.6 mA			0.4	V
		V_{CC} = 4.5 V to 5.5 V,	I_{OL} = 20 µA			0.1	
I_{OZ}	Off-state (high-impedance-state) output current	$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}		1	2.5	µA
		V_O = 0,	$\overline{CS}$ at V_{CC}		1	–2.5	
I_{IH}	High-level input current	$V_I = V_{CC}$			1	2.5	µA
I_{IL}	Low-level input current	V_I = 0			1	–2.5	µA
I_{CC}	Operating supply current	$\overline{CS}$ at 0 V			1	2.5	mA
$I_{CC(PD)}$	Power-down current	For all digital inputs, $0 \le V_I \le 0.5$ V or $V_I \ge V_{CC} - 0.5$ V			4	25	µA
	Selected channel leakage current	Selected channel at V_{CC}, Unselected channel at 0 V				1	µA
		Selected channel at 0 V, Unselected channel at V_{CC}				–1	
	Maximum static analog reference current into REF+	$V_{ref+} = V_{CC}$,	V_{ref-} = GND		1	2.5	µA
C_i	Input capacitance, Analog inputs				30	60	pF
	Input capacitance, Control inputs				5	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

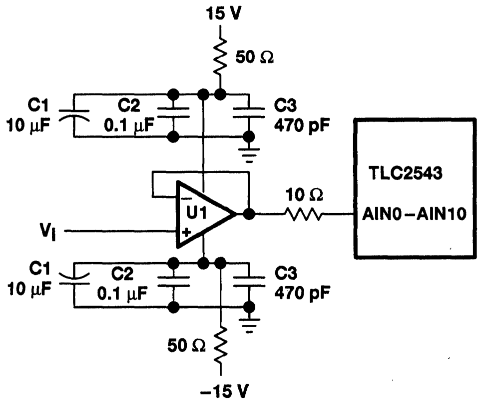
operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 4.5 V to 5.5 V, I/O CLOCK frequency = 4.1 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error (see Note 5)	See Figure 2			±1	LSB
E_D	Differential linearity error	See Figure 2			±1	LSB
E_O	Offset error (see Note 6)	See Note 2 and Figure 2			±1.5	LSB
E_G	Gain error (see Note 6)	See Note 2 and Figure 2			±1	LSB
E_T	Total unadjusted error (see Note 7)				±1.75	LSB
	Self-test output code (see Table 3 and Note 8)	DATA INPUT = 1011		2048		
		DATA INPUT = 1100		0		
		DATA INPUT = 1101		4095		
t_{conv}	Conversion time	See Figures 10–15		8	10	µs
t_c	Total cycle time (access, sample, and conversion)	See Figures 10–15 and Note 9			10 + total I/O CLOCK periods + $t_{d(I/O-EOC)}$	µs
t_{acq}	Channel acquisition time (sample)	See Figures 10–15 and Note 9	4		12	I/O CLOCK periods
t_v	Valid time, DATA OUT remains valid after I/O CLOCK↓	See Figure 7	10			ns
$t_{d(I/O-DATA)}$	Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 7			150	ns
$t_{d(I/O-EOC)}$	Delay time, last I/O CLOCK↓ to EOC↓	See Figure 8		1.5	2.2	µs
$t_{d(EOC-DATA)}$	Delay time, EOC↑ to DATA OUT (MSB/LSB)	See Figure 9			100	ns
t_{PZH}, t_{PZL}	Enable time, $\overline{CS}$↓ to DATA OUT (MSB/LSB driven)	See Figure 4		0.7	1.3	µs
t_{PHZ}, t_{PLZ}	Disable time, $\overline{CS}$↑ to DATA OUT (high impedance)	See Figure 4		70	150	ns
$t_{r(EOC)}$	Rise time, EOC	See Figure 9		15	50	ns
$t_{f(EOC)}$	Fall time, EOC	See Figure 8		15	50	ns
$t_{r(bus)}$	Rise time, data bus	See Figure 7		15	50	ns
$t_{f(bus)}$	Fall time, data bus	See Figure 7		15	50	ns
$t_{d(I/O-CS)}$	Delay time, last I/O CLOCK↓ to $\overline{CS}$↓ to abort conversion (see Note 10)				5	µs

† All typical values are at T_A = 25°C.

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (111111111111), while input voltages less than that applied to REF– convert as all zeros (000000000000).
5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Gain error is the difference between the actual midstep value and the nominal midstep value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. Offset error is the difference between the actual midstep value and the nominal midstep value at the offset point.
7. Total unadjusted error comprises linearity, zero-scale, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic.
9. I/O CLOCK period = 1/(I/O CLOCK frequency) (see Figure 7).
10. Any transitions of $\overline{CS}$ are recognized as valid only if the level is maintained for a setup time. $\overline{CS}$ must be taken low at ≤ 5 µs of the tenth I/O CLOCK falling edge to ensure a conversion is aborted. Between 5 µs and 10 µs, the result is uncertain as to whether the conversion is aborted or the conversion results are valid.

PARAMETER MEASUREMENT INFORMATION



LOCATION	DESCRIPTION	PART NUMBER
U1	OP27	—
C1	10-µF 35-V tantalum capacitor	—
C2	0.1-µF ceramic NPO SMD capacitor	AVX 12105C104KA105 or equivalent
C3	470-pF porcelain Hi-Q SMD capacitor	Johanson 201S420471JG4L or equivalent

Figure 2. Analog Input Buffer to Analog Inputs AIN0 – AIN10

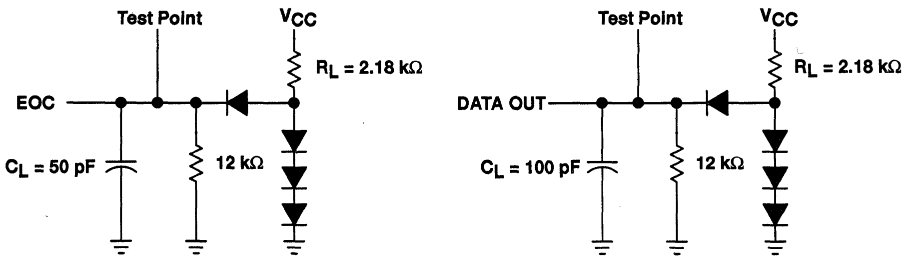


Figure 3. Load Circuits

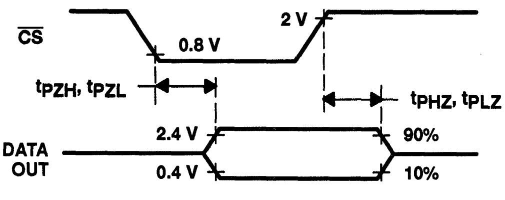


Figure 4. DATA OUT to Hi-Z Voltage Waveforms

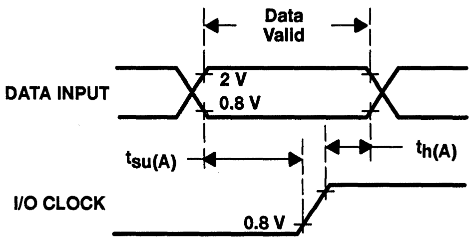


Figure 5. DATA INPUT and I/O CLOCK Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

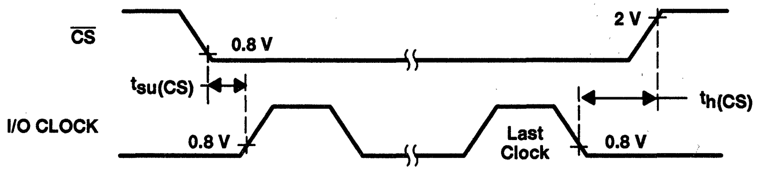


Figure 6. $\overline{CS}$ and I/O CLOCK Voltage Waveforms†

† To ensure full conversion accuracy, it is recommended that no input signal change occurs while a conversion is ongoing.

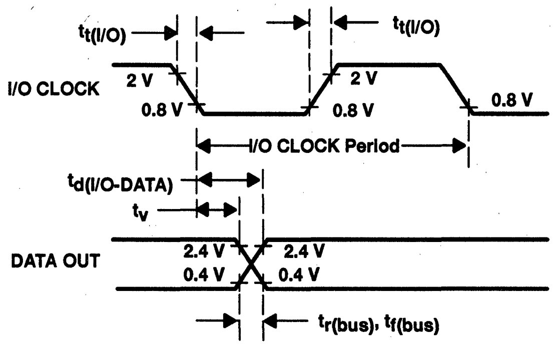


Figure 7. I/O CLOCK and DATA OUT Voltage Waveforms

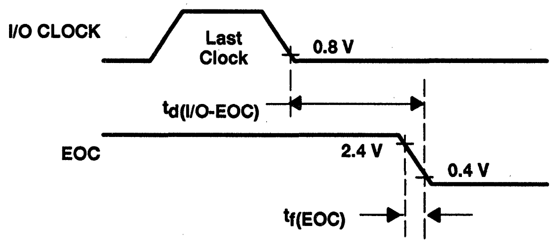


Figure 8. I/O CLOCK and EOC Voltage Waveforms

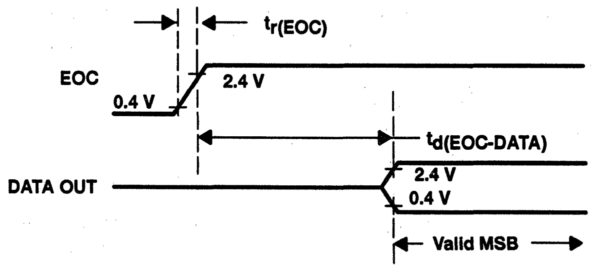


Figure 9. EOC and DATA OUT Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

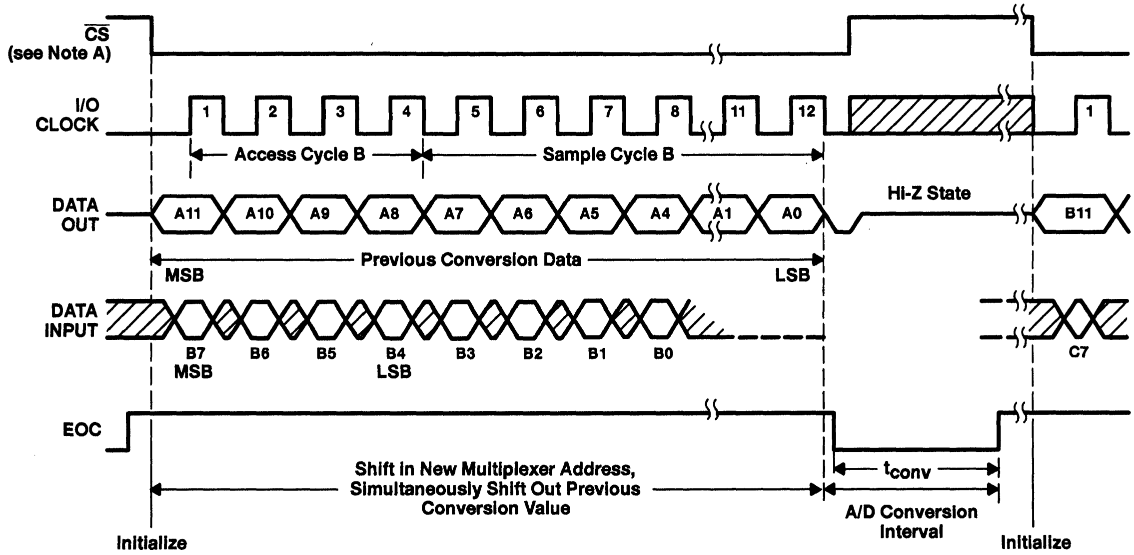


Figure 10. Timing for 12-Clock Transfer Using $\overline{CS}$ With MSB First

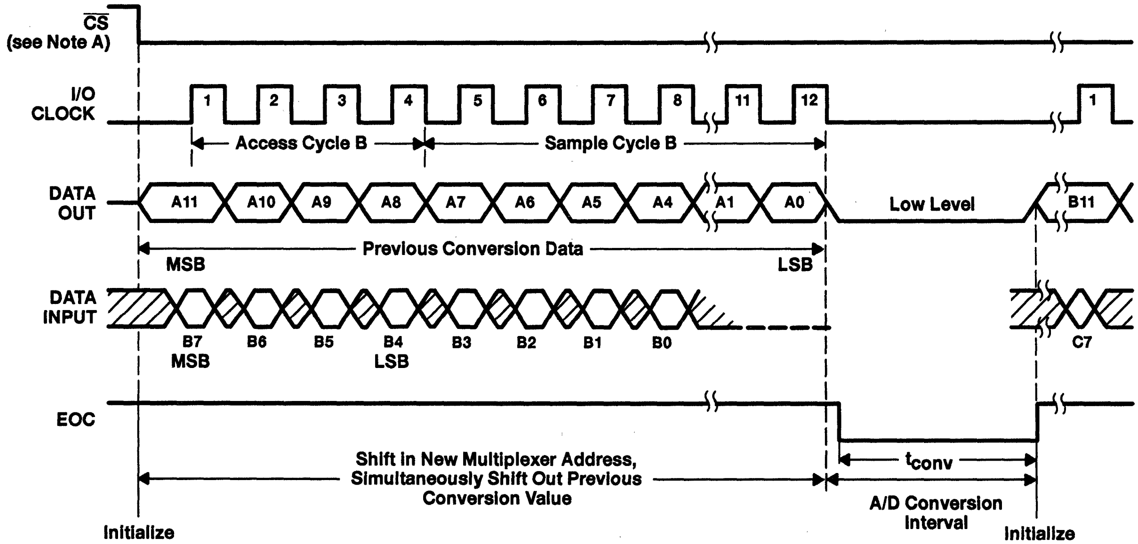


Figure 11. Timing for 12-Clock Transfer Not Using $\overline{CS}$ With MSB First

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

PARAMETER MEASUREMENT INFORMATION

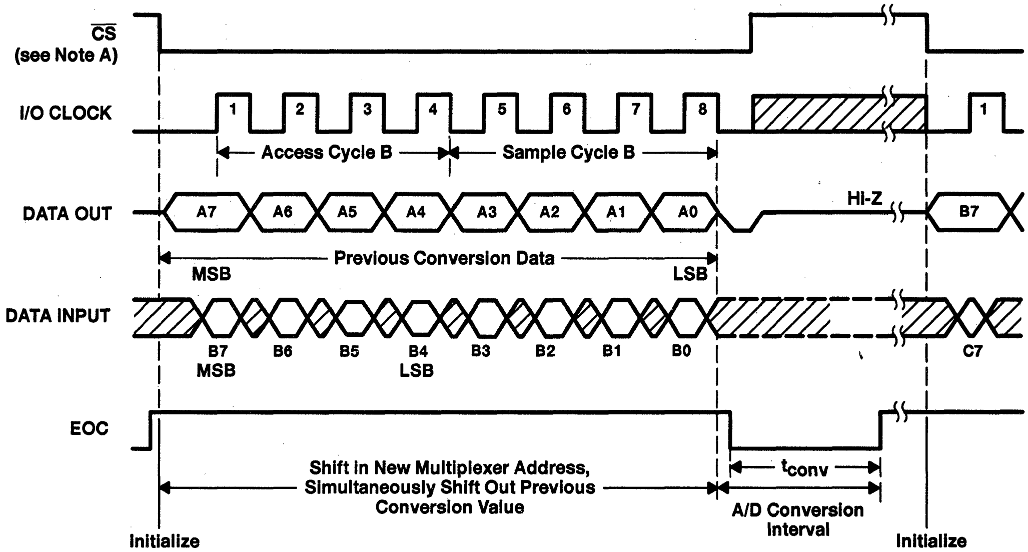


Figure 12. Timing for 8-Clock Transfer Using $\overline{CS}$ With MSB First

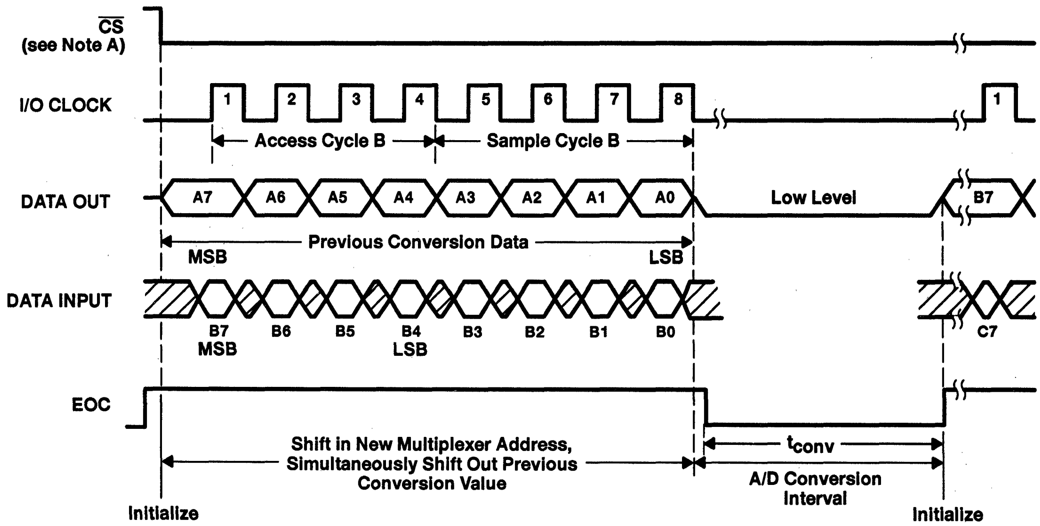


Figure 13. Timing for 8-Clock Transfer Not Using $\overline{CS}$ With MSB First

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

PARAMETER MEASUREMENT INFORMATION

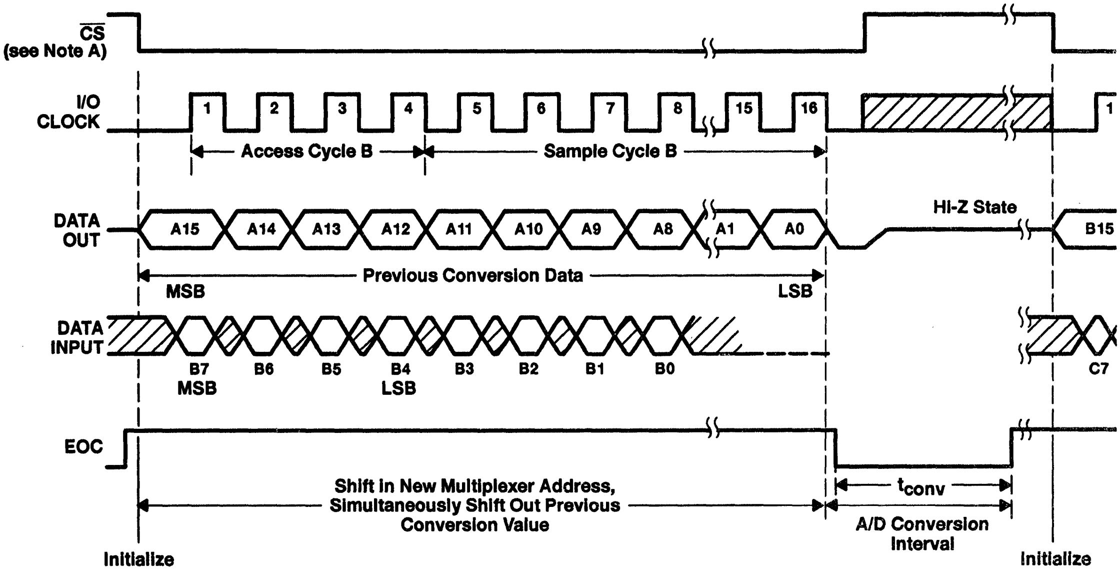


Figure 14. Timing for 16-Clock Transfer Using $\overline{CS}$ With MSB First

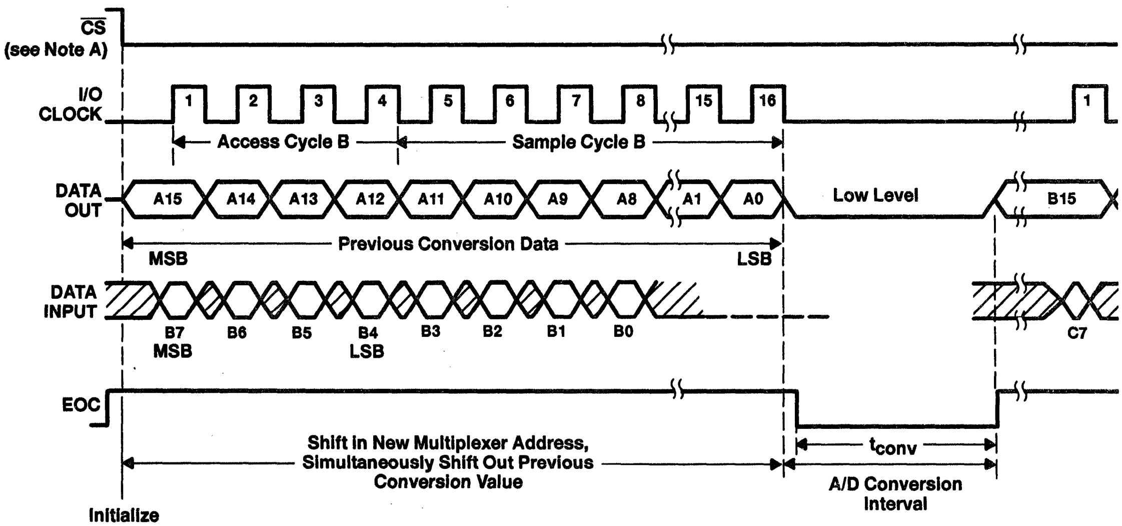
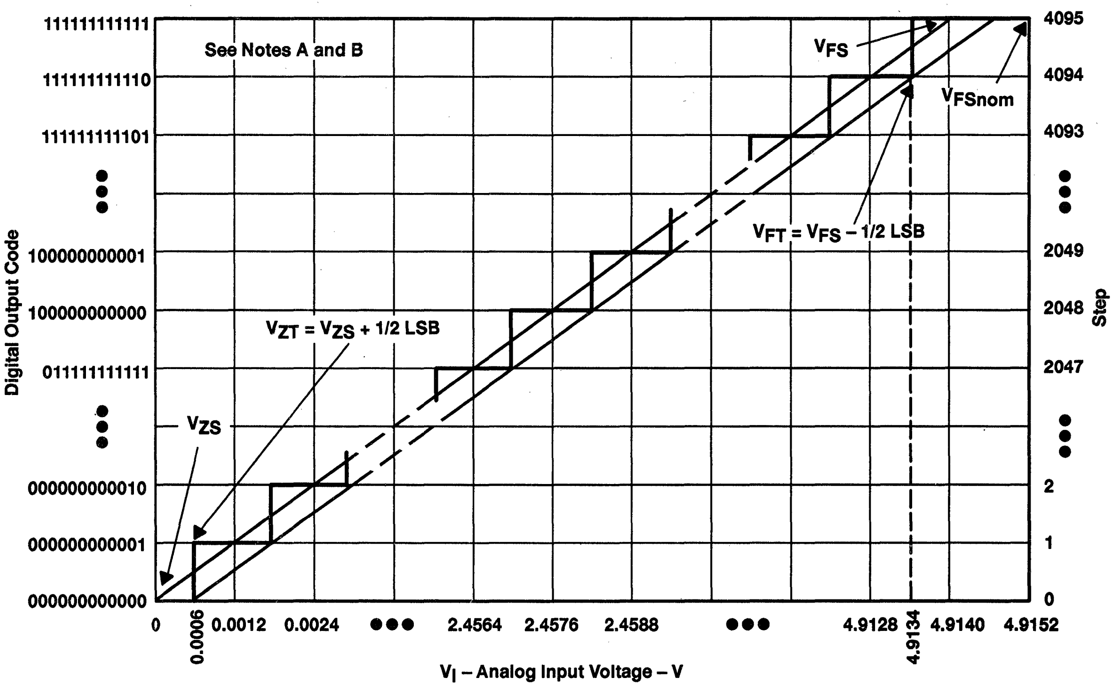


Figure 15. Timing for 16-Clock Transfer Not Using $\overline{CS}$ With MSB First

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}$↓ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

APPLICATION INFORMATION



NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0006 V and the transition to full scale (V_{FT}) is 4.9134 V. 1 LSB = 1.2 mV.

B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 16. Ideal Conversion Characteristics

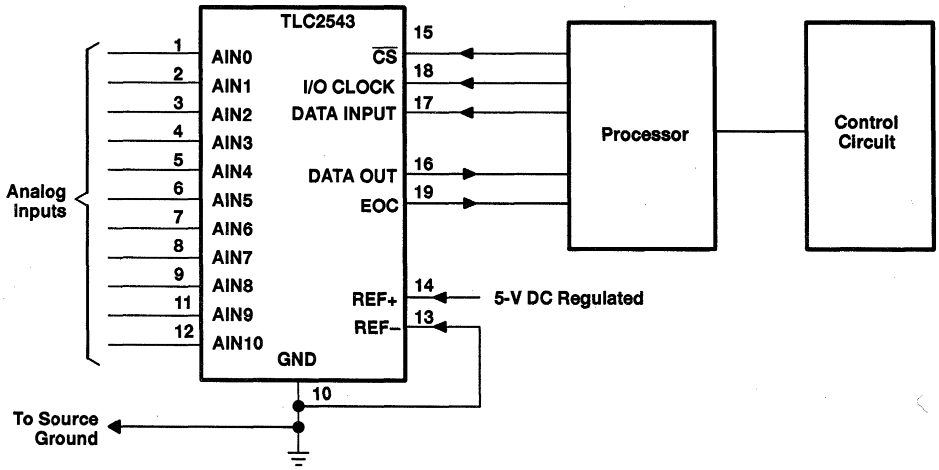


Figure 17. Serial Interface

APPLICATIONS INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 18, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S\left(1 - e^{-t_c/R_tC_i}\right) \qquad (1)$$

where

$$R_t = R_s + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C\ (1/2\ \text{LSB}) = V_S - (V_S/8192) \qquad (2)$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - \left(V_S/58192\right) = V_S\left(1 - e^{-t_c/R_tC_i}\right) \qquad (3)$$

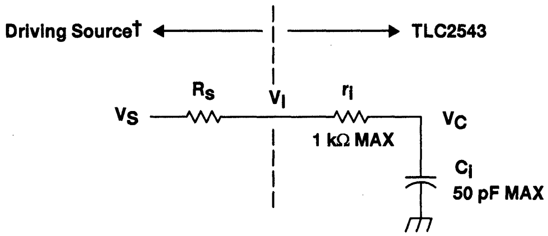
and

$$t_c\ (1/2\ \text{LSB}) = R_t \times C_i \times \ln(8192) \qquad (4)$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c\ (1/2\ \text{LSB}) = (R_s + 1\ \text{k}\Omega) \times 60\ \text{pF} \times \ln(8192) \qquad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at AIN
V_S = External Driving Source Voltage
R_s = Source Resistance
r_i = Input Resistance
C_i = Input Capacitance

† Driving source requirements:
- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_s must be real at the input frequency.

Figure 18. Equivalent Input Circuit Including the Driving Source

SLAS095B – SEPTEMBER 1994 – REVISED FEBRUARY 1995

features

- 8-Bit Resolution
- Linearity Error
  ±0.75 LSB Max (25°C)
  ±1 LSB Max (–20°C to 75°C)
- Differential Linearity Error
  ±0.5 LSB (25°C)
  ±0.75 LSB Max (–20°C to 75°C)
- Maximum Conversion Rate
  20 Mega-Samples per Second
  (MSPS) Min
- 5-V Single-Supply Operation
- Low Power Consumption . . . 90 mW Typ
- Interchangeable With Sony CXD1175

applications

- Digital TV
- Medical Imaging
- Video Conferencing
- High-Speed Data Conversion
- QAM Demodulators

NS PACKAGE†
(TOP VIEW)

Pin name	Pin	Pin	Pin name
$\overline{OE}$	1	24	DGND
DGND	2	23	REFB
D1(LSB)	3	22	REFBS
D2	4	21	AGND
D3	5	20	AGND
D4	6	19	ANALOG IN
D5	7	18	V_{DDA}
D6	8	17	REFT
D7	9	16	REFTS
D8(MSB)	10	15	V_{DDA}
V_{DDD}	11	14	V_{DDA}
CLK	12	13	V_{DDD}

† Available in tape and reel only and ordered as the TLC5510INSLE.

AVAILABLE OPTIONS

T_A	NS PACKAGE (TAPE AND REEL ONLY)
–20°C to 75°C	TLC5510INSLE

description

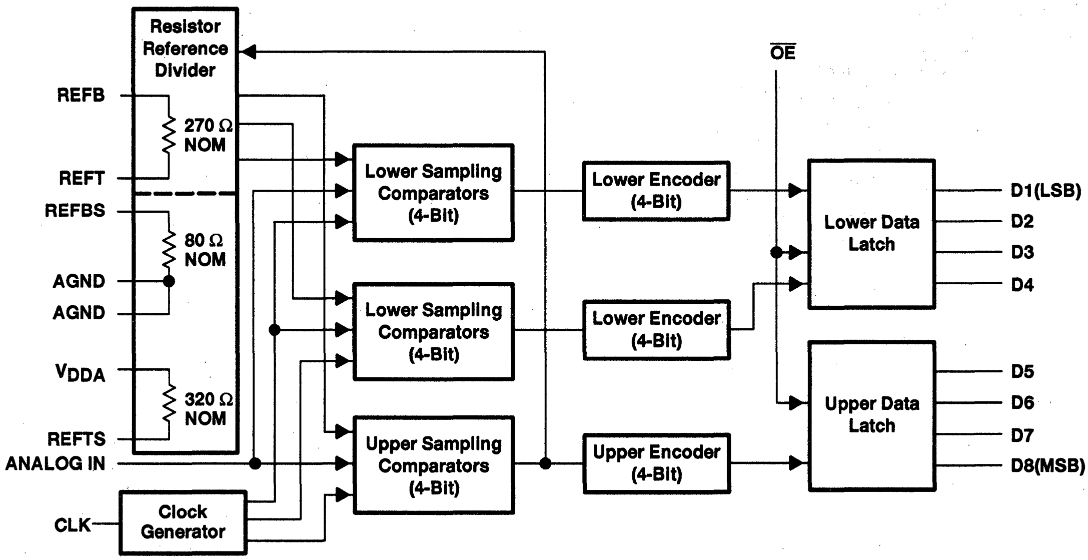
The TLC5510 is a CMOS, 8-bit, 20 MSPS analog-to-digital converter (ADC) that utilizes a semiflash architecture. The TLC5510 operates with a single 5 V supply and consumes only 100 mW of power typically. Also included is an internal sample and hold circuit, parallel outputs with high impedance mode, and internal reference resistors.

The semiflash architecture reduces power consumption and die size compared to flash converters. By implementing the conversion in a 2-step process, the number of comparators is significantly reduced. The latency of the data upon conversion is 2.5 clocks.

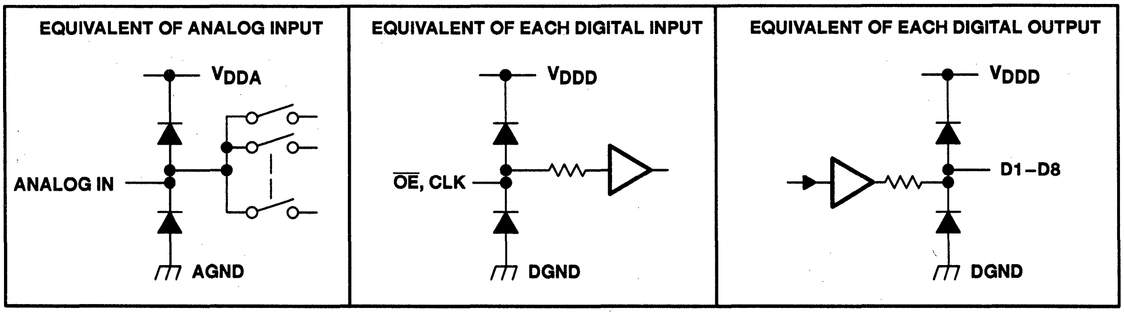
The internal reference resistors can create a standard, 2-V, full-scale conversion range using V_{DDA}. Only external jumpers are required to implement this option. This reduces the need for external references or resistors. Differential linearity is 0.5 LSB at 25°C and a maximum of 0.75 LSB over the full operating temperature range. Dynamic characteristics are specified with a differential gain of 1% and differential phase of 0.7%.

The TLC5510 is characterized for operation from –20°C to 75°C.

functional block diagram



schematics of inputs and outputs



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AGND	20, 21		Analog ground
ANALOG IN	19	I	Analog input
CLK	12	I	Clock in
DGND	2, 24		Digital ground
D1–D8	3–10	O	Digital data out. D1:LSB, D8:MSB
$\overline{OE}$	1	I	Output enable. When $\overline{OE}$ = L, data is enabled. When $\overline{OE}$ = H, D1–D8 is in high impedance state.
V_{DDA}	14, 15, 18		Analog V_{DD}
V_{DDD}	11, 13		Digital V_{DD}
REFB	23	I	Reference voltage in (bottom)
REFBS	22		Reference voltage (bottom). When using the internal voltage divider to generate a nominal 2-V reference, this terminal is shorted to the REFB terminal (see Figure 2).
REFT	17	I	Reference voltage in (top)
REFTS	16		Reference voltage (top). When using the internal voltage divider to generate a nominal 2-V reference, this terminal is shorted to the REFT terminal (see Figure 2).

absolute maximum ratings†

Supply voltage, V_{DDA}, V_{DDD} .... 7 V
Reference voltage input range, $V_{ref(T)}$, $V_{ref(B)}$, $V_{ref(BS)}$, $V_{ref(TS)}$ .... AGND to V_{DDA}
Analog input voltage range, $V_{I(ANLG)}$ .... AGND to V_{DDA}
Digital input voltage range, $V_{I(DGTL)}$ .... DGND to V_{DDD}
Digital output voltage range, $V_{O(DGTL)}$ .... DGND to V_{DDD}
Operating free-air temperature range, T_A .... –20°C to 75°C
Storage temperature range, T_{stg} .... –55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage	V_{DDA}–AGND	4.75	5	5.25	V
	V_{DDD}–AGND	4.75	5	5.25	V
	AGND–DGND	–100	0	100	mV
Reference input voltage (top), $V_{ref(T)}$		$V_{ref(B)}$+2	$V_{ref(B)}$+2	2.7	V
Reference input voltage (bottom), $V_{ref(B)}$		0	0.6	$V_{ref(T)}$–2	V
Analog input voltage range, $V_{I(ANLG)}$ (see Note 1)		$V_{ref(B)}$		$V_{ref(T)}$	V
High-level input voltage, V_{IH}		4			V
Low-level input voltage, V_{IL}				1	V
Pulse duration, clock high, $t_{w(H)}$		25			ns
Pulse duration, clock low, $t_{w(L)}$		25			ns

NOTE 1: REFT – REFB ≥ 2.4 V maximum

electrical characteristics at V_{DD} = 5 V, $V_{ref(T)}$ = 2.5 V, $V_{ref(B)}$ = 0.5 V, f_{conv} = 20 MSPS, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
E_L	Linearity error	f_{conv} = 20 MSPS, V_I = 0.5 V to 2.5 V	T_A = 25°C			±0.4	±0.75	LSB
			T_A = −20°C to 75°C				±1	
E_D	Linearity error, differential		T_A = 25°C			±0.3	±0.5	
			T_A = −20°C to 75°C				±0.75	
	Self bias (1)	Short REFB to REFBS,	Short REFT to REFTS		0.57	0.61	0.65	V
	Self bias (2)				1.9	2.02	2.15	
	Self bias (3)	Short REFB to AGND,	Short REFT to REFTS		2.18	2.29	2.4	
I_{ref}	Reference voltage current	$V_{ref(T)} - V_{ref(B)}$ = 2 V			5.2	7.5	10.5	mA
R_{ref}	Reference voltage resistor	Between REFT and REFB terminals			190	270	350	Ω
C_i	Analog input capacitance	$V_{I(ANLG)}$ = 1.5 V + 0.07 V_{rms}				16		pF
E_{ZS}	Zero-scale error	V_{ref} = REFT − REFB = 2 V			−18	−43	−68	mV
E_{FS}	Full-scale error				−20	0	20	
I_{IH}	High-level input current	V_{DD} = MAX,	$V_{IH} = V_{DD}$				5	μA
I_{IL}	Low-level input current	V_{DD} = MAX,	V_{IL} = 0 V				5	
I_{OH}	High-level output current	$\overline{OE}$ = GND,	V_{DD} = MIN,	$V_{OH} = V_{DD}$−0.5 V	−1.5			mA
I_{OL}	Low-level output current	$\overline{OE}$ = GND,	V_{DD} = MIN,	V_{OL} = 0.4 V	2.5			
I_{OZH}	High-level high-impedance-state output leakage current	$\overline{OE} = V_{DD}$,	V_{DD} = MAX	$V_{OH} = V_{DD}$			16	μA
I_{OZL}	Low-level high-impedance-state output leakage current	$\overline{OE} = V_{DD}$,	V_{DD} = MIN	V_{OL} = 0 V			16	
I_{DD}	Supply current	f_s = 20 MSPS,	National Television System Committee (NTSC) ramp wave input			18	27	mA

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

operating characteristics at V_{DD} = 5 V, V_{RT} = 2.5 V, V_{RB} = 0.5 V, f_s = 20 MSPS, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{conv}	Maximum conversion rate	$V_{I(ANLG)}$ = 0.5 V – 2.5 V, f_I = 1-kHz ramp wave form	20			MSPS
BW	Analog input bandwidth	At – 1 dB		14		MHz
t_{dd}	Digital output delay time	$C_L \le$ 10 pF (see Note 2)		18	30	ns
	Differential gain	NTSC 40 Institute of Radio Engineers (IRE) modulation wave, f_{conv} = 14.3 MSPS		1%		
	Differential phase			0.7		degrees
t_{AJ}	Aperture jitter time			30		ps
$t_{d(s)}$	Sampling delay time			4		ns

NOTE 2: C_L includes probe and jig capacitance

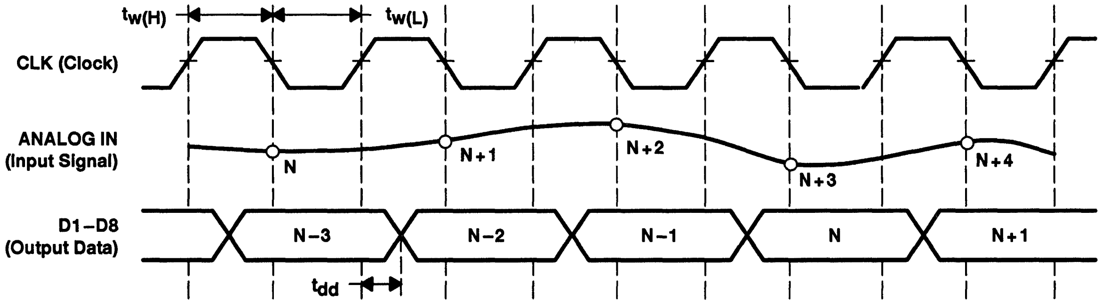


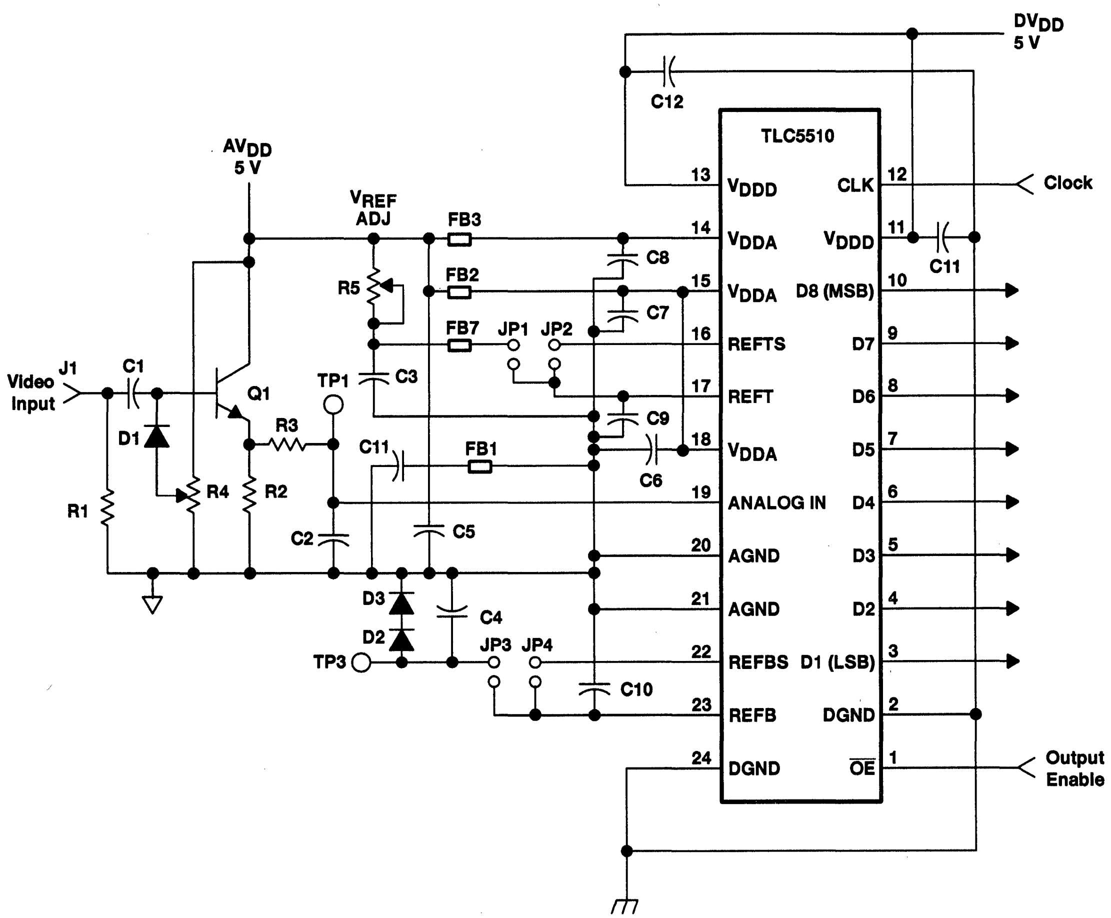
Figure 1. I/O Timing Diagram

APPLICATION INFORMATION

The following notes are design recommendations that should be used with the TLC5510.

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or printed-circuit-board (PCB) techniques should be used throughout the evaluation and production process. Breadboards should be copper clad for bench evaluation.
- Since AGND and DGND are not connected internally, these terminals need to be connected externally. With breadboards, these ground lines should be connected through separate leads with correct supply bypassing. A good method to use is separate twisted-pair cables for the supply lines to minimize noise pickup. An analog and digital ground plane should be used on PCB layouts.
- V_{DDA} to AGND and V_{DDD} to DGND should be decoupled with 1-µF and 0.01-µF capacitors, respectively, and placed as close as possible to the affected device terminals. A ceramic-chip capacitor is recommended for the 0.01-µF capacitor. Care should be exercised to ensure a solid noise-free ground connection for the analog and digital grounds.
- V_{DDA}, AGND, and ANALOG IN terminals should be shielded from the higher frequency terminals, CLK and D0–D7. When possible, AGND traces should be placed on both sides of the ANALOG IN traces on the PCB for shielding.
- In testing or application of the device, the resistance of the driving source connected to the analog input should be 10 Ω or less within the analog frequency range of interest.

APPLICATION INFORMATION



LOCATION	DESCRIPTION
C1, C3–C4, C6–C12	0.1-µF Capacitor
C2	10-pF Capacitor
C5	47-µF Capacitor
FB1, FB2, FB3, FB7	Ferrite Bead
Q1	2N3414 or equivalent
R1, R3	75-Ω resistor
R2	500-Ω resistor
R4	10-kΩ resistor, clamp voltage adjust
R5	300-Ω resistor, reference-voltage fine adjust

Figure 2. Application and Test Schematic

NOTE A: JP1, JP2, JP3, and JP4 allow adjustment of the reference voltage by R5 using temperature-compensating diodes D2, D3.

PRINCIPLES OF OPERATION

functional description

The TLC5510 is a semiflash ADC featuring two lower comparator blocks of four bits each.

As shown in Figure 3, input voltage $V_I(1)$ is sampled with the falling edge of CLK1 to the upper comparators block and the lower comparators block(A), S(1). The upper comparators block finalizes the upper data UD(1) with the rising edge of CLK2, and simultaneously, the lower reference voltage generates the voltage RV(1) corresponding to the upper data. The lower comparators block (A) finalizes the lower data LD(1) with the rising edge of CLK3. UD(1) and LD(1) are combined and output as OUT(1) with the rising edge of CLK4. According to the above internal operation described, output data is delayed 2.5 clocks from the analog input voltage sampling point.

Input voltage $V_I(2)$ is sampled with the falling edge of CLK2. UD(2) is finalized with the rising edge of CLK3, and LD(2) is finalized with the rising edge of CLK4 at the lower comparators block(B). OUT(2) is output with the rising edge of CLK5.

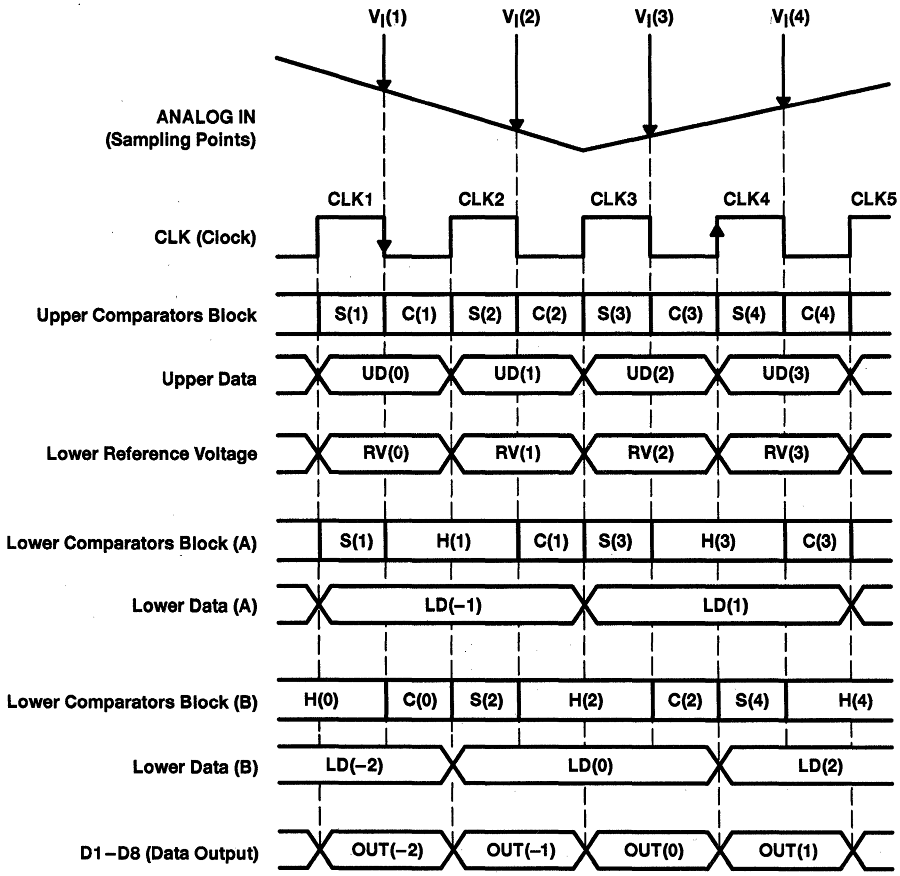


Figure 3. Internal Functional Timing Diagram

PRINCIPLES OF OPERATION

internal referencing

Three internal resistors are provided so that the device can generate an internal reference voltage. These resistors are brought out on terminals V_{DDA}, REFTS, REFT, REFB, REFBS, and AGND.

To use the internally generated reference voltage, terminal connections should be made as shown in Figure 4. This connection provides the standard video 2-V reference for the nominal digital output.

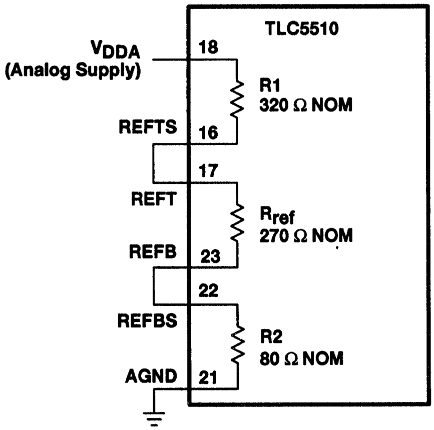


Figure 4. External Connections for Using the Internal-Reference Resistor Divider

functional operation

The TLC5510 functions as shown in Table 1.

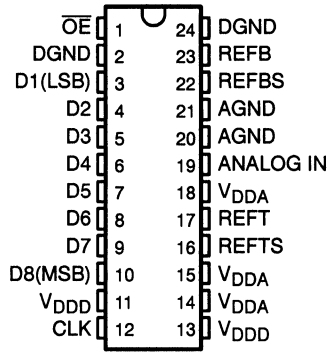
Table 1. Functional Operation

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE MSB							LSB
$V_{ref(T)}$	0	1	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	127	1	0	0	0	0	0	0	0
•	128	0	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
$V_{ref(B)}$	255	0	0	0	0	0	0	0	0

features

- 8-Bit Resolution
- Linearity Error
  - ±0.75 LSB Max (25°C)
  - ±1 LSB Max (–20°C to 75°C)
- Differential Linearity Error
  - ±0.5 LSB (25°C)
  - ±0.75 LSB Max (–20°C to 75°C)
- Maximum Conversion Rate of 40 Mega-Samples per Second (MSPS) Min
- Internal Sample and Hold
- 5-V Single-Supply Operation
- Low Power Consumption . . . 100 mW Typ
- Analog Input Bandwidth . . . >75 MHz Typ

NS PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_A	NS PACKAGE
–20°C to 75°C	TLC5540INS

applications

- Quadrature Phase Shift Keying (QPSK) Demodulators
- Medical Imaging
- Charge-Coupled Device (CCD) Scanners
- Video Conferencing
- Digital Set-Top Box
- Digital Down Converters
- High-Speed Signal Processing

description

The TLC5540 is a CMOS, 8-bit, 40 MSPS analog-to-digital converter (ADC) that utilizes a semiflash architecture. The TLC5540 operates with a single 5 V supply and consumes only 100 mW of power typically. Also included is an internal sample and hold circuit, parallel outputs with high impedance mode and internal reference resistors.

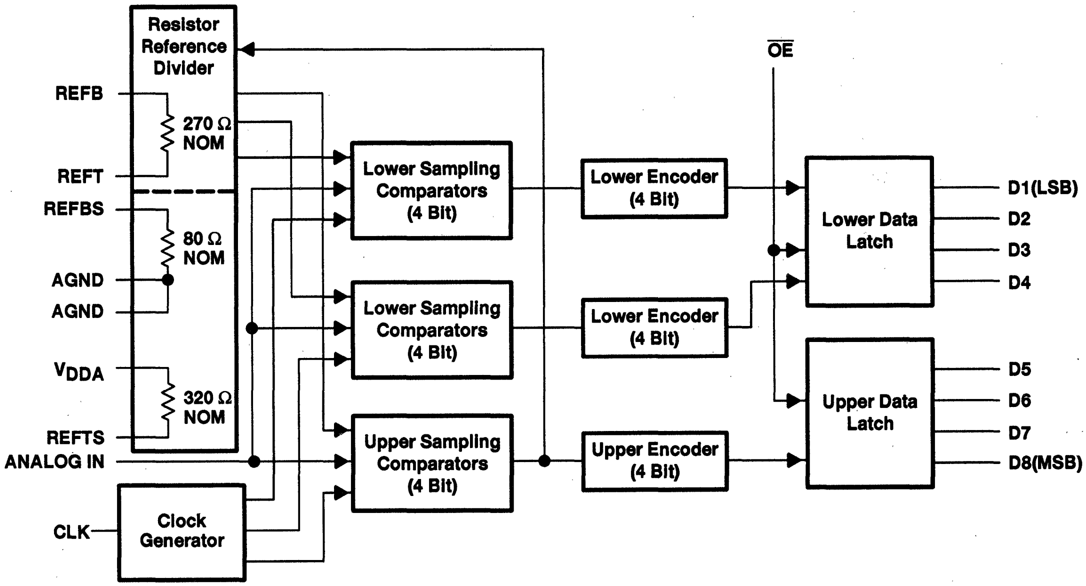
The TLC5540 has a wide analog-input bandwidth typically greater than 75 MHz. This feature allows use of the ADC in undersampling applications such as digital down converters and allows the elimination of expensive RF components.

The semiflash architecture reduces power consumption and die size compared to flash converters. The conversion is implemented in a 2-step process which significantly reduces the number of comparators. The latency of the data upon conversion is 2.5 clocks.

The internal reference resistors can create a standard 2-V full-scale conversion range using V_{DDA}. Only external jumpers are required to implement this option, thereby reducing the need for external references or resistors. The TLC5540 is characterized for operation from –20°C to 75°C. Differential linearity is ±0.5 LSB at 25°C and a maximum of ±0.75 LSB over the full operating temperature range. Dynamic characteristics are specified with a differential gain of 1% and differential phase of 0.7%.

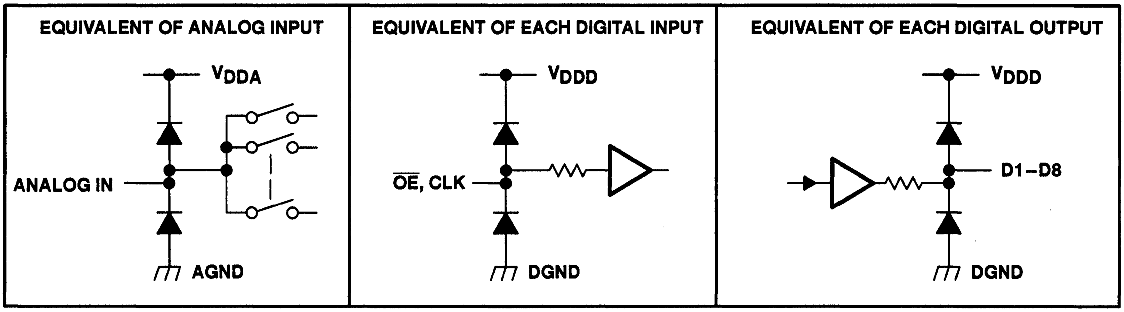
PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

schematics of inputs and outputs



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	20, 21		Analog ground
ANALOG IN	19	I	Analog input
CLK	12	I	Clock input
DGND	2, 24		Digital ground
D1–D8	3–10	O	Digital data out. D1:LSB, D8:MSB
$\overline{OE}$	1	I	Output enable. When $\overline{OE}$ = L, data is enabled. When $\overline{OE}$ = H, D1–D8 is high impedance.
V_{DDA}	14, 15, 18		Analog V_{DD}
V_{DDD}	11, 13		Digital V_{DD}
REFB	23	I	Reference voltage in (bottom)
REFBS	22		Reference voltage (bottom). When using the internal voltage divider to generate a nominal 2-V reference, this terminal is shorted to the REFB terminal and the REFTS terminal is shorted to the REFT terminal (see Figure 3).
REFT	17	I	Reference voltage in (top)
REFTS	16		Reference voltage (top). When using the internal voltage divider to generate a nominal 2-V reference, this terminal is shorted to the REFT terminal and the REFBS terminal is shorted to the REFB terminal (see Figure 3).

PRODUCT PREVIEW

absolute maximum ratings†

Supply voltage, V_{DDA}, V_{DDD} .... 7 V
Reference voltage input range, $V_{ref(T)}$, $V_{ref(B)}$, $V_{ref(BS)}$, $V_{ref(TS)}$ .... AGND to V_{DDA}
Analog input voltage range, $V_{I(ANLG)}$ .... AGND to V_{DDA}
Digital input voltage range, $V_{I(DGTL)}$ .... DGND to V_{DDD}
Digital output voltage range, $V_{O(DGTL)}$ .... DGND to V_{DDD}
Operating free-air temperature range, T_A .... –20°C to 75°C
Storage temperature range, T_{stg} .... –55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage	V_{DDA}–AGND	4.75	5	5.25	V
	V_{DDD}–AGND	4.75	5	5.25	V
	AGND–DGND	–100	0	100	mV
Reference input voltage (top), $V_{ref(T)}$		$V_{ref(B)}$+2	$V_{ref(B)}$+2	2.7	V
Reference input voltage (bottom), $V_{ref(B)}$		0	0.6	$V_{ref(T)}$–2	V
Analog input voltage range, $V_{I(ANLG)}$ (see Note 1)		$V_{ref(B)}$		$V_{ref(T)}$	V
High-level input voltage, V_{IH}		4			V
Low-level input voltage, V_{IL}				1	V
Pulse duration, clock high, $t_{w(H)}$		25			ns
Pulse duration, clock low, $t_{w(L)}$		25			ns

NOTE 1: REFT – REFB ≥ 2.4 V maximum

electrical characteristics at V_{DD} = 5 V, $V_{ref(T)}$ = 2.5 V, $V_{ref(B)}$ = 0.5 V, $f_{(sampling)}$ = 40 MSPS, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
E_L	Linearity error	$f_{(sampling)}$ = 40 MSPS, V_I = 0.5 V to 2.5 V	T_A = 25°C		±0.4	±0.75	LSB
			T_A = –20°C to 75°C			±1	LSB
E_D	Linearity error, differential		T_A = 25°C		±0.3	±0.5	LSB
			T_A = –20°C to 75°C			±0.75	LSB
	Self bias (1)	Short REFB to REFBS,	Short REFT to REFTS	0.57	0.61	0.65	V
	Self bias (2)			1.9	2.02	2.15	V
	Self bias (3)	Short REFB to AGND,	Short REFT to REFTS	2.18	2.29	2.4	V
I_{ref}	Reference-voltage current	$V_{ref(T)} - V_{ref(B)}$ = 2 V		5.2	7.5	10.5	mA
R_{ref}	Reference-voltage resistor	Between REFT and REFB terminals		190	270	350	Ω
C_i	Analog-input capacitance	$V_{I(ANLG)}$ = 1.5 V + 0.07 V_{rms}			16		pF
E_{ZS}	Zero-scale error	V_{ref} = REFT – REFB = 2 V		–18	–43	–68	mV
E_{FS}	Full-scale error			–20	0	20	mV
I_{IH}	High-level input current	V_{DD} = MAX,	$V_{IH} = V_{DD}$			5	µA
I_{IL}	Low-level input current	V_{DD} = MAX,	V_{IL} = 0			5	µA
I_{OH}	High-level output current	$\overline{OE}$ = GND,	V_{DD} = MIN, $V_{OH} = V_{DD}$–0.5 V	–1.5			mA
I_{OL}	Low-level output current	$\overline{OE}$ = GND,	V_{DD} = MIN, V_{OL} = 0.4 V	2.5			mA
I_{OZH}	High-level high-impedance-state output leakage current	$\overline{OE} = V_{DD}$,	V_{DD} = MAX $V_{OH} = V_{DD}$			16	µA
I_{OZL}	Low-level high-impedance-state output leakage current	$\overline{OE} = V_{DD}$,	V_{DD} = MIN V_{OL} = 0			16	µA
I_{DD}	Supply current	$f_{(sampling)}$ = 40 MSPS,	National Television System Committee (NTSC) ramp wave input		20	30	mA

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

operating characteristics at V_{DD} = 5 V, V_{RT} = 2.5 V, V_{RB} = 0.5 V, $f_{(sampling)}$ = 40 MSPS, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(sampling)}$	Maximum conversion rate	$V_{I(ANLG)}$ = 0.5 V – 2.5 V, f_I = 1-kHz ramp wave form	40			MSPS
BW	Analog-input bandwidth	At – 3 dB		>75		MHz
t_{pd}	Digital-output delay time	$C_L \le 10$ pF (see Note 2)		18	30	ns
	Differential gain	NTSC 40 Institute Radio Engineers (IRE) modulation wave, f_{conv} = 14.3 MSPS		1%		
	Differential phase			0.7		degrees
t_{AJ}	Aperture jitter time			30		ps
$t_{d(s)}$	Sampling delay time			4		ns

NOTE 2: C_L includes probe and jig capacitance

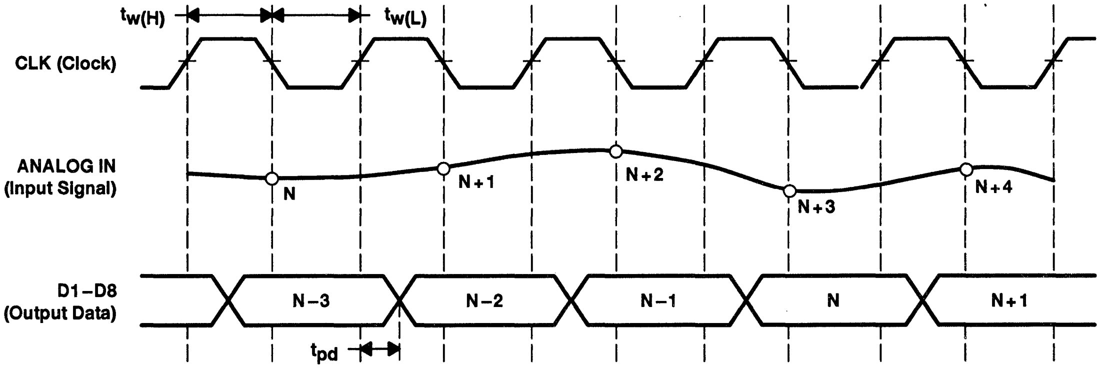


Figure 1. I/O Timing Diagram

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

functional description

The TLC5540 is a semiflash, analog-to-digital converter featuring two lower comparator blocks of four bits each.

As shown in Figure 2, input voltage $V_I(1)$ is sampled with the falling edge of CLK1 to the upper comparators block and the lower comparators block(A), S(1). The upper comparators block finalizes the upper data UD(1) with the rising edge of CLK2, and simultaneously, the lower reference voltage generates the voltage RV(1) corresponding to the upper data. The lower comparators block (A) finalizes the lower data LD(1) with the rising edge of CLK3. UD(1) and LD(1) are combined and output as OUT(1) with the rising edge of CLK4. According to the above internal operation described, output data is delayed 2.5 clocks from the analog input voltage sampling point.

Input voltage $V_I(2)$ is sampled with the falling edge of CLK2. UD(2) is finalized with the rising edge of CLK3, and LD(2) is finalized with the rising edge of CLK4 at the lower comparators block(B). OUT(2) is output with the rising edge of CLK5.

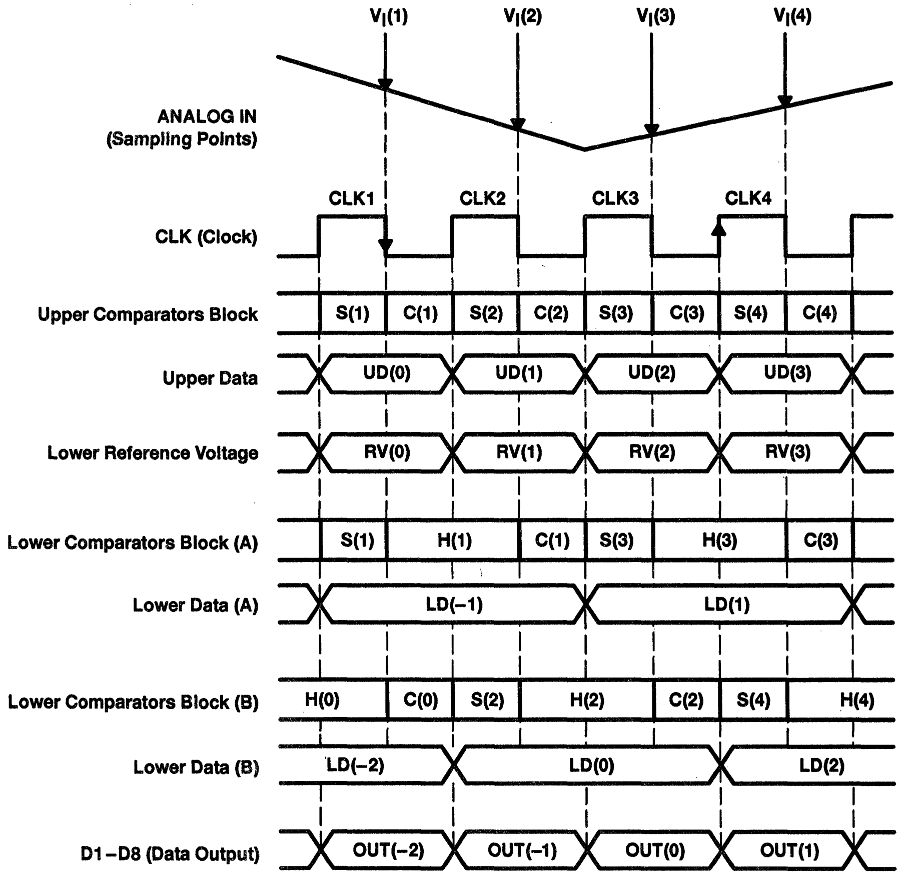


Figure 2. Internal Functional Timing Diagram

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

internal referencing

Three internal resistors allow the device to generate an internal reference voltage. These resistors are brought out on terminals V_{DDA}, REFTS, REFT, REFB, REFBS, and AGND.

To use the internally-generated reference voltage, terminal connections should be made as shown in Figure 3. This connection provides the standard video 2-V reference for the nominal digital output.

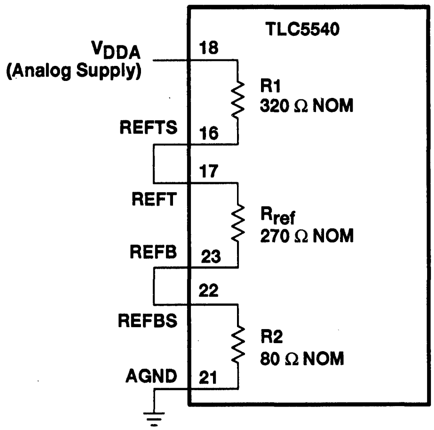


Figure 3. External Connections for Using the Internal Reference Resistor Divider

functional operation

Table 1 shows the TLC5540 functions.

Table 1. Functional Operation

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE MSB							LSB
$V_{ref(T)}$	0	1	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	127	1	0	0	0	0	0	0	0
•	128	0	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
$V_{ref(B)}$	255	0	0	0	0	0	0	0	0

PRODUCT PREVIEW

APPLICATION INFORMATION

The following notes are design recommendations that should be used with the TLC5540.

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or printed-circuit-board (PCB) techniques should be used throughout the evaluation and production process. Breadboards should be copper clad for bench evaluation.
- Since AGND and DGND are not connected internally, these terminals need to be connected externally. With breadboards, these ground lines should be connected through separate leads with correct supply bypassing. Separate twisted-pair cables are a good method to use for the supply lines to minimize noise pickup. An analog and digital ground plane should be used on PCB layouts.
- V_{DDA} to AGND and V_{DDD} to DGND should be decoupled with 1-µF and 0.01-µF capacitors, respectively, placed as close as possible to the appropriate device terminals. A ceramic-chip capacitor is recommended for the 0.01-µF capacitor. Care should be exercised to ensure a solid noise-free ground connection for the analog and digital grounds.
- V_{DDA}, AGND, and ANALOG IN terminals should be shielded from the higher frequency terminals, CLK and D0–D7. If possible, AGND traces should be placed on both sides of the ANALOG IN traces on the PCB for shielding.
- In testing or application of the device, the resistance of the driving source connected to the analog input should be 10 Ω or less within the analog frequency range of interest.

PRODUCT PREVIEW

TLC5733
20 MSPS 3-CHANNEL ANALOG-TO-DIGITAL CONVERTER WITH HIGH-PRECISION CLAMP

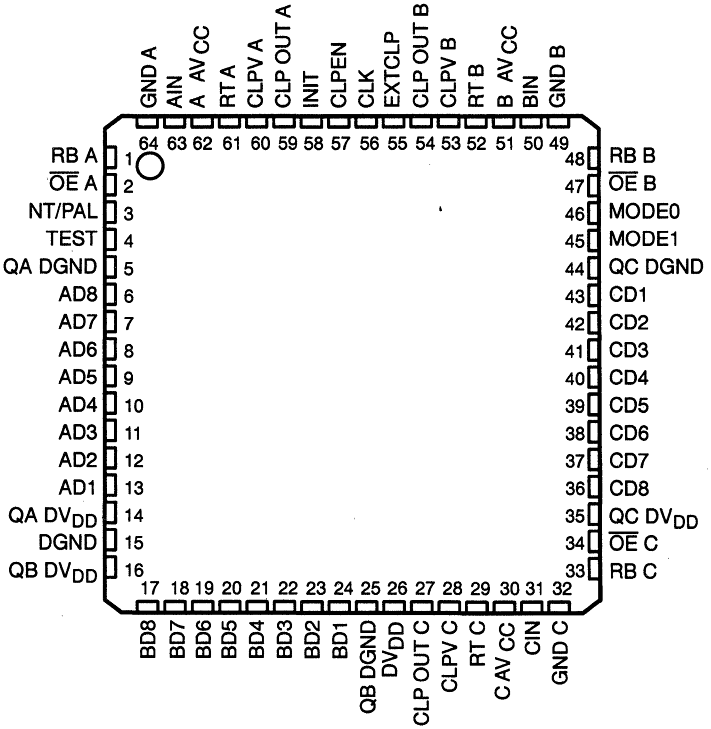
SLAS104 – JULY 1995

- 3-Channel CMOS ADC
- 8-Bit Resolution
- Differential Linearity Error . . . ±0.5 LSB Max
- Linearity Error . . . ±0.75 LSB Max
- Maximum Conversion Rate 20 Mega-Samples per Second (MSPS) Min
- Analog Input Voltage Range 2 $V_{(PP)}$ (Min)
- 64-Pin Shrink QFP Package
- Analog Input Bandwidth . . . >14 MHz
- Suitable for YUV or RGB Applications
- Digital Clamp Optimized for NTSC or PAL YUV Component
- High Precision Clamp . . . ±1 LSB
- Automatic Clamp Pulse Generator
- Output Data Format Multiplexer
- 5-V Single-Supply Operation
- Low Power Consumption

description

The TLC5733 is a three-channel 8-bit semiflash analog-to-digital converter (ADC) that operates from a single 5-V power supply. It converts a wide-band analog signal (such as a video signal) to digital data at sampling rates up to 20 MSPS minimum. The TLC5733 contains a feed-back type high-precision clamp circuit for each ADC channel for video (YUV) applications and a clamp pulse generator that detects COMPOSITE SYNC† pulses automatically. A clamp pulse can also be supplied externally. The output data format multiplexer selects a ratio of Y:U:V of 4:4:4, 4:1:1, or 4:2:2. For RGB applications, the 4:4:4 output format without clamp function can be used. The TLC5733 is characterized for operation from −20°C to 75°C.

PM PACKAGE
(TOP VIEW)

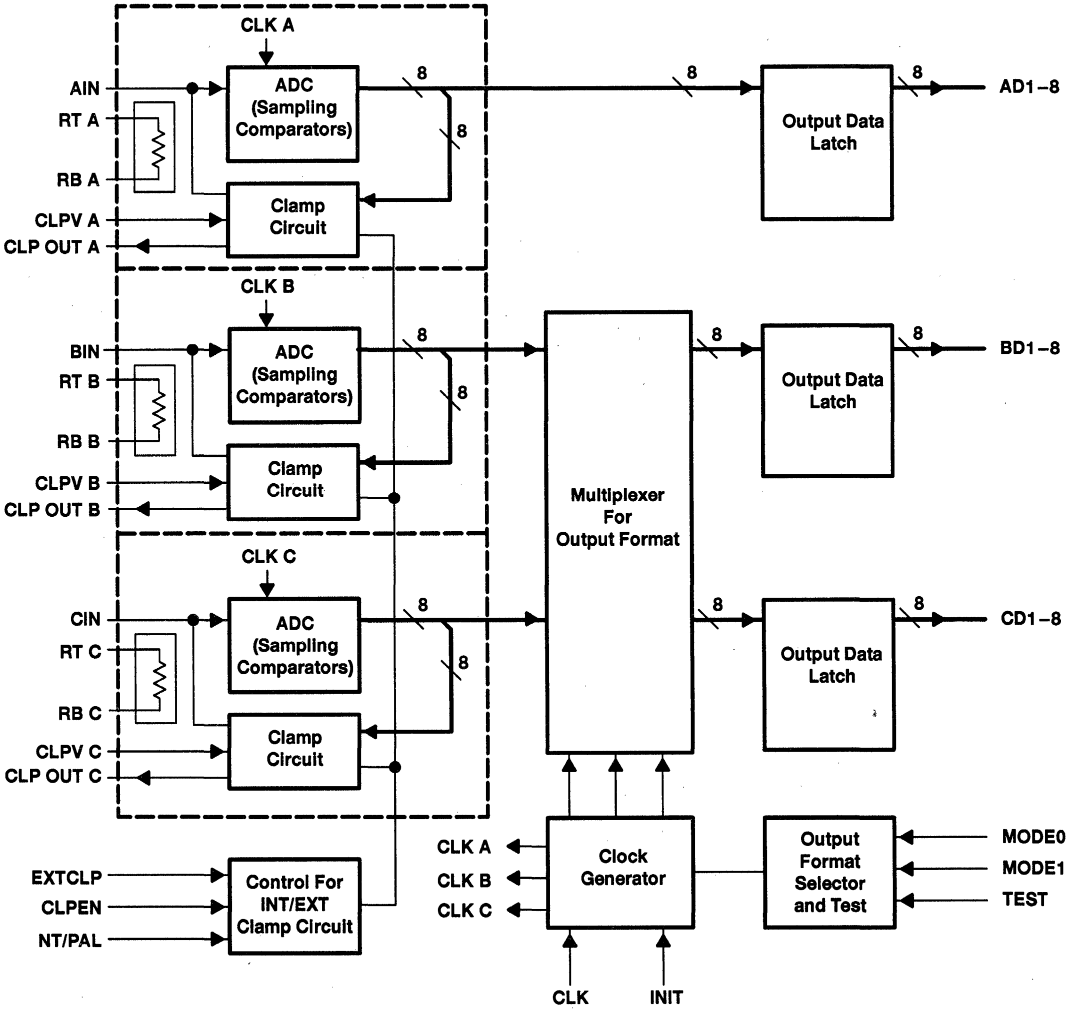


† COMPOSITE SYNC refers to the externally generated synchronizing signal that is a combination of vertical and horizontal sync information used in display and TV systems.

AVAILABLE OPTIONS

T_A	PACKAGE
	QUAD FLATPACK
−20°C to 75°C	TLC5733IPM

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
A AV_{CC}	62	I	Analog V_{CC} of ADC A
AD8–AD1	6–13	O	Data output of ADC A (LSB: AD1, MSB:AD8)
AIN	63	I	Analog input of ADC A
B AV_{CC}	51	I	Analog V_{CC} of ADC B
BD8–BD1	17–24	O	Data output of ADC B (LSB: BD1, MSB:BD8)
BIN	50	I	Analog input of ADC B
C AV_{CC}	30	I	Analog V_{CC} of ADC C
CD8–CD1	36–43	O	Data output of ADC C (LSB:CD1, MSB: CD8) When MODE0 = L, MODE1 = L, CD8 outputs MSB flag of BD8–BD5 When MODE0 = L, MODE1 = L, CD7 outputs MSB flag of BD8–BD5 When MODE0 = L, MODE1 = H, CD8 outputs B channel flag of CD8–BD1 When MODE0 = L, MODE1 = H, CD8 outputs B channel flag of CD8–BD1
CIN	31	I	Analog input of ADC C
CLK	56	I	Clock input. The clock frequency is normally 4 fsc for most video systems (see Table 3). The nominal clock frequency is 14.31818 MHz for NTSC and 17.745 MHz for PAL.
CLPEN	57	I	Clamp enable. When using an internal clamp pulse, CLPEN should be high. When using an external clamp pulse, CLPEN should be low.
CLP OUT A	59	O	Clamping bias current of ADC A. A resistor-capacitor combination is used to set the clamp timing.
CLP OUT B	54	O	Clamping bias current of ADC B. A resistor-capacitor combination is used to set the clamp timing.
CLP OUT C	27	O	Clamping bias current of ADC C. A resistor-capacitor combination is used to set the clamp timing.
CLPV A	60	O	Clamping level of ADC A. A capacitor is connected to CLPV A to set the clamp timing. The clamp level at this terminal is connected to an output code of 16 (0010000).
CLPV B	53	O	Clamping level of ADC B. A capacitor is connected to CLPV B to set the clamp timing. The clamp level at this terminal is connected to an output code of 128 (1000000).
CLPV C	28	O	Clamping level of ADC C. A capacitor is connected to CLPV C to set the clamp timing. The clamp level at this terminal is connected to an output code of 128 (1000000).
DGND	15	I	Digital ground
DV_{DD}	26	I	Digital V_{DD}
EXTCLP	55	I	External clamp pulse input. When this terminal is low and CLPEN is low, the internal clamp circuit cannot be used.
GND A	64	I	Ground of ADC A
GND B	49	I	Ground of ADC B
GND C	32	I	Ground of ADC C
INIT	58	I	Output initialized. The output data is synchronous when INIT is taken high from low. This control terminal allows the external system to initialize the TLC5733 data conversion cycle. It is usually used upon power up or system reset.
MODE0	46	I	Output format mode selector 0
MODE1	45	I	Output format mode selector 1
NT/PAL	3	I	NTSC/PAL control. The NTSC/PAL terminal should be: NTSC = low level, PAL = high level.
$\overline{OE}$ A	2	I	Output enable of ADC A
$\overline{OE}$ B	47	I	Output enable of ADC B
$\overline{OE}$ C	34	I	Output enable of ADC C
QA DGND	5	I	Digital ground for output port of ADC A
QA DV_{DD}	14	I	Digital V_{DD} for output of ADC A
QB DGND	25	I	Digital ground for output of ADC B
QB DV_{DD}	16	I	Digital V_{DD} for output of ADC B

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
QC DGND	44	I	Digital ground for output of ADC C
QC DV_{DD}	35	I	Digital V_{DD} for output of ADC C
RB A	1	I	Reference voltage bottom of ADC A
RB B	48	I	Reference voltage bottom of ADC B
RB C	33	I	Reference voltage bottom of ADC C
RT A	61	I	Reference voltage top of ADC A. The nominal externaly applied DC voltage between the RT A terminal and the RB A terminal is 2 V for video signals.
RT B	52	I	Reference voltage top of ADC B. The nominal externaly applied DC voltage between the RT B terminal and the RB B terminal is 2 V for video signals.
RT C	29		Reference voltage top of ADC C. The nominal externaly applied DC voltage between the RT C terminal and the RB C terminal is 2 V for video signals.
TEST	4	I	Test. This terminal should be tied low when using this device.

absolute maximum ratings†

Supply voltage, V_{CC}, V_{DD} .... 7 V
Reference voltage input range, $V_{ref(RT\ A)}$, $V_{ref(RT\ B)}$, $V_{ref(RT\ C)}$, $V_{ref(RB\ A)}$, $V_{ref(RB\ B)}$, $V_{ref(RB\ C)}$ .... AGND to VCC
Analog input voltage range .... AGND to V_{CC}
Digital input voltage range, V_I .... DGND to V_{DD}
Digital output voltage range, V_O .... DGND to V_{DD}
Operating free-air temperature range, T_A .... –20°C to 75°C
Storage temperature range, T_{stg} .... –55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage	V_{CC}–AGND	4.75	5	5.25	V
	V_{DD}–DGND	4.75	5	5.25	V
	AGND–DGND	–100	0	100	mV
Reference input voltage, $V_{ref(RT\ A)}$, $V_{ref(RT\ B)}$, $V_{ref(RT\ C)}$		$V_{ref(RB)}$+2		V_{CC}	V
Reference input voltage, $V_{ref(RB\ A)}$, $V_{ref(RB\ B)}$, $V_{ref(RB\ C)}$		0		$V_{ref(RT)}$–2	V
Analog input voltage, V_I		0		$V_{ref(RT)}$	V
High-level input voltage, V_{IH}		4			V
Low-level input voltage, V_{IL}				1	V
High-level pulse duration, $t_{w(H)}$		25			ns
Low-level pulse duration, $t_{w(L)}$		25			ns
Setup time for INIT input, t_{su1}		5			ns
Operating free-air temperature range, T_A		–20		75	°C

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electrical characteristics at V_{DD} = 5 V, $V_{ref(RT)}$ = 2.5 V, $V_{ref(BB)}$ = 0.5 V, f_s = 20 MSPS, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Clamp level accuracy				±1		LSB
R_{ref}	Reference voltage resistor	Measured between RT and RB		160	220	350	Ω
C_i	Analog input capacitance	V_I = 1.5 V + 0.07 V_{rms}			16		pF
I_{IH}	High-level input current	V_{DD} = MAX†,	V_{IH} = V_{DD}			5	μA
I_{IL}	Low-level input current	V_{DD} = MAX†,	V_{IL} = 0			5	
I_{OH}	High-level output current	V_{DD} = MIN†,	V_{OH} = V_{DD}–0.5 V	–1.5			mA
I_{OL}	Low-level output current	V_{DD} = MIN†,	V_{OL} = 0.4 V	2.5			
I_{OZH}	High-level output leakage current	V_{DD} = MAX†,	V_{OH} = V_{DD}			16	μA
I_{OZL}	Low-level output leakage current	V_{DD} = MIN†,	V_{OL} = 0			16	
I_{CC}	Supply current	f_s = 20 MSPS,	NTSC ramp wave input			75	mA

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

operating characteristics at V_{DD} = 5 V, $V_{ref(RT)}$ = 2.5 V, $V_{ref(RB)}$ = 0.5 V, f_s = 20 MSPS, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
E_{ZS}	Zero-scale error	V_{ref} = REFT – REFB = 2 V		–18	–43	–68	mV
E_{FS}	Full-scale error	V_{ref} = REFT – REFB = 2 V		–20	0	20	mV
E_L	Linearity error	f_s = 20 MSPS,	V_I = 0.5 V to 2.5 V		±0.4	±0.75	LSB
		f_s = 20 MSPS, T_A = –20°C to 75°C	V_I = 0.5 V to 2.5 V		±0.4	±1	
E_D	Linearity error, differential	f_s = 20 MSPS,	V_I = 0.5 V to 2.5 V		±0.3	±0.5	LSB
		f_s = 20 MSPS, T_A = –20°C to 75°C	V_I = 0.5 V to 2.5 V		±0.3	±0.75	
f_s	Maximum conversion rate	V_I = 0.5 V – 2.5 V,	f_I = 1-kHz ramp wave form	20			MSPS
BW	Analog input bandwidth	At – 1 dB			14		MHz
t_{pd}	Digital output delay time	C_L = 10 pF			18	30	ns
	Differential gain	NTSC 40 IRE modulation wave, f_s = 14.3 MSPS			1%		
	Differential phase				0.7		deg
t_{AJ}	Aperture jitter time				30		ps
t_{ps}	Sampling delay time				4		ns

detailed description

clamp function

The clamp function is optimized for a YUV video signal and has two clamp modes. The first mode uses the COMPOSITE SYNC signal as the input to the EXTCLP terminal to generate an internal clamp pulse and the second mode uses an externally generated clamp pulse as the input to the EXTCLP terminal.

In the first mode, the device detects false pulses in the COMPOSITE SYNC signal by monitoring the rising edges and falling edges of the COMPOSITE SYNC signal pulses. This monitoring prevents faulty operation caused by disturbances and missing pulses of the COMPOSITE SYNC signal input on EXTCLP and external spike noise. When fault pulses are detected, the device internally generates a train of clamp pulses at the proper positions (1H) by an internal 910-counter for NTSC and a 1136-counter for PAL. The device checks clamp pulses for 1H time and generates clamp pulses at correct positions if COMPOSITE SYNC pulses are in error in time.

The internal counter continually produces a horizontal sync period (1H) that is NTSC or PAL compatible as selected by the condition of the NT/PAL terminal.

clamp voltages and selection

Table 1 shows the clamping level during the clamp interval. Table 2 shows the selection of the internal or external clamp pulse. With either NTSC or PAL, the internal clamp pulse is always used.

Table 1. Clamp Level (Internal Connection Level)

CHANNEL OF ADC	OUTPUT CODE	APPLICATION
ADC A · $V_{I(A)}$	00010000	Y
ADC B · $V_{I(B)}$	10000000	(U, V)
ADC C · $V_{I(C)}$	10000000	(U, V)

Table 2. Clamp Level (Internal Connection Level)

CONDITION			FUNCTION (EACH ADC)	
CLPEN	EXTCLP	NT/PAL	INTERNAL CLAMP	CLAMP PULSE
L	⎍	Don't Care	Inactive	External clamp pulse
	L	Don't Care	Inactive	No clamping
H	COMPOSITE SYNC input	L	Active	Synchronous with NTSC
		H	Active	Synchronous with PAL

The clamp circuit is shown in Figure 6. The clamp voltage is stored on capacitor C2 during the back porch of the horizontal blanking period.

During the clamp pulse the input to channel A is clamped to

$$V_C(A) = (16/256) \times (\text{voltage difference from terminal RT A to RB A})$$

$$V_C(B) = (128/256) \times (\text{voltage difference from terminal RT B to RB B})$$

$$V_C(C) = (128/256) \times (\text{voltage difference from terminal RT C to RB C})$$

COMPOSITE SYNC time monitoring

When CLPEN is high, COMPOSITE SYNC generates an internal clamp pulse on the horizontal blanking interval back porch. The TLC5733 has a timing window into which the horizontal sync tip must occur. There is a noise time window for the falling edge and a noise time window for the rising edge. Refer to Figure 1, Figure 2, and Table 3.

correct COMPOSITE SYNC timing

The Noise Gate 1 signal provides the timing window for the COMPOSITE SYNC falling edge. After an interval A of 867 clocks for NTSC or 1075 for PAL from the last falling edge of COMPOSITE SYNC, Noise Gate 1 goes high for 43 clocks for NTSC or 61 clocks for PAL (interval B). The falling edge of the input signal to the EXTCLP terminal can occur at any time within this window to be a valid COMPOSITE SYNC falling edge.

The Noise Gate 2 signal provides the timing window for the COMPOSITE SYNC rising edge. On the falling edge of the horizontal sync tip, the internal logic generates Noise Gate 2 as a low signal for 58 clocks (interval C) for both NTSC and PAL and then returns to a high active state. If, at this time, the input to the EXTCLP terminal is still low, it is considered a valid COMPOSITE SYNC signal.

normal clamp pulse generation

On the rising edge of the COMPOSITE SYNC signal, the internal logic generates an internal delay (interval D) and then generates the internal positive clamp pulse 54 clocks wide (interval F).

clamp operation with incorrect COMPOSITE SYNC timing

noise suppression

If the input to the EXTCLP terminal goes low prior to Noise Gate 1 going high (within 43 clocks for NTSC or 61 clocks for PAL of the normal 1H timing for the falling edge of COMPOSITE SYNC) then that input is not considered a valid COMPOSITE SYNC and is ignored.

If the input to the EXTCLP terminal is high when Noise Gate 2 goes to the high state, the input signal is considered noise and is ignored.

Therefore, the correct signal must be high a maximum of 43 clocks for NTSC or 61 clocks for PAL, before the 1H timing, to be a valid sync signal. Also, the input to the EXTCLP terminal must be at least 58 clocks wide (interval C) to be valid.

This function of monitoring the timing eliminates spurious noise spikes from falsely synchronizing the system.

timing error of COMPOSITE SYNC

The internal counter resets to zero on the first falling edge of COMPOSITE SYNC. After that time, if there is a missing COMPOSITE SYNC signal, then the internal logic waits an interval of 76 clocks (interval E) for NTSC or 93 for PAL from the counter zero count and then generates an internal clamp pulse 54 clocks wide (interval F).

This function maintains the synchronization pattern when COMPOSITE SYNC is not present.

summary of device operation with COMPOSITE SYNC

This internal timing allows the TLC5733 to correctly position the clamp pulse when an external COMPOSITE SYNC input occurs as follows:

- Is delayed with respect to the horizontal sync period
- Is early with respect to the horizontal sync period
- Is nonexistent during the horizontal sync period
- Has falling edge noise spikes within the horizontal sync period

The device operation is summarized as follows for these improper external clamp conditions.

- Under all four conditions on the EXTCLP terminal, the internal clamp generation circuit generates a clamp pulse at the proper time after the horizontal sync period as shown in Figure 1.
- The TLC5733 internal clamp circuit generates an internal clamp pulse each 1H time for the entire time interval that the COMPOSITE SYNC input is missing.

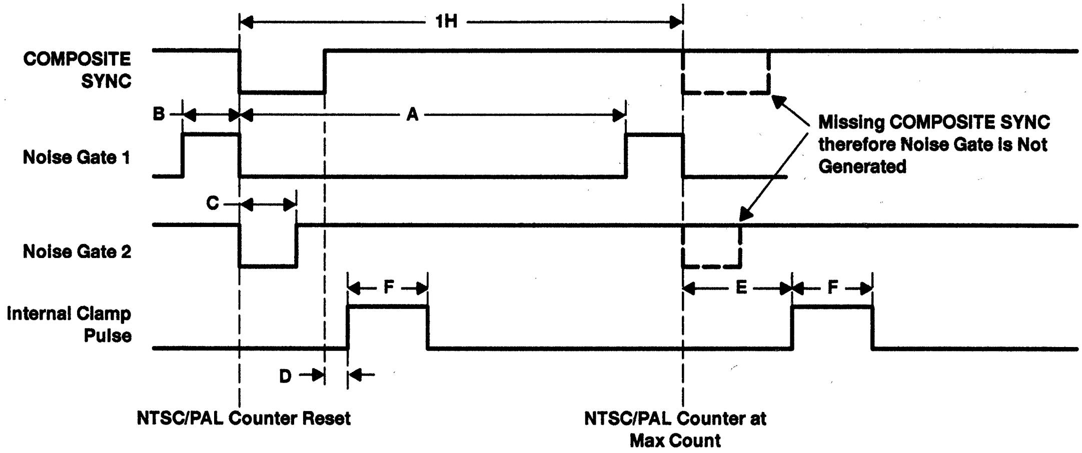


Figure 1. COMPOSITE SYNC and Internal Clamp Timing

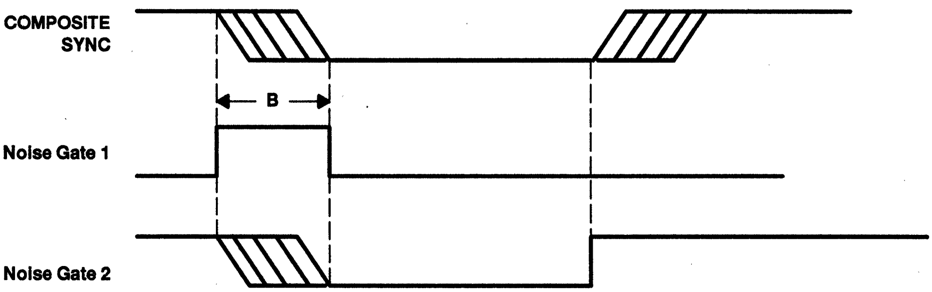


Figure 2. Proper COMPOSITE SYNC Timing

Table 3. Sync and Clamp Timing for NTSC and PAL with CLK = 4 fsc

TIME INTERVAL	NTSC		PAL	
	NO. OF CLOCKS	TIME (µs)	NO. OF CLOCKS	TIME (µs)
A	867	60.6	1075	60.7
B	43	3	61	3.5
C	58	4.05	58	3.27
D	6	0.42	6	0.34
E	76	5.3	93	5.25
F	54	3.77	84	4.74
fsc	3.58 MHz		4.43 MHz	

using an external clamp pulse

When CLPEN is taken low, the EXTCLP terminal accepts an externally generated active-high clamp pulse. This pulse must occur within the horizontal blanking interval back porch. CLPEN low inhibits the internal counters and no internal clamp pulse is generated.

output digital code (for each channel of ADC)

Table 4. Input Signal Versus Output Digital Code

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE MSB							LSB
$V_{ref(RT)}$	255	1	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	128	1	0	0	0	0	0	0	0
•	127	0	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
$V_{ref(RB)}$	0	0	0	0	0	0	0	0	0

output data format

The TLC5733 can select three output data formats to various TV/VCR (video) data processing by the combination of MODE0 and MODE1. The output is synchronous when INIT is taken high.

Table 5. Output Data Format Selection

CONDITION		OUTPUT DATA	
MODE1	MODE0	OUTPUT DATA FORMAT	RATIO OF Y:U:V
L	L	Format 1	4:1:1
L	H	Format 2	4:4:4
H	L	Format 3	4:2:2
H	H	Not used	N/A

output data format (continued)

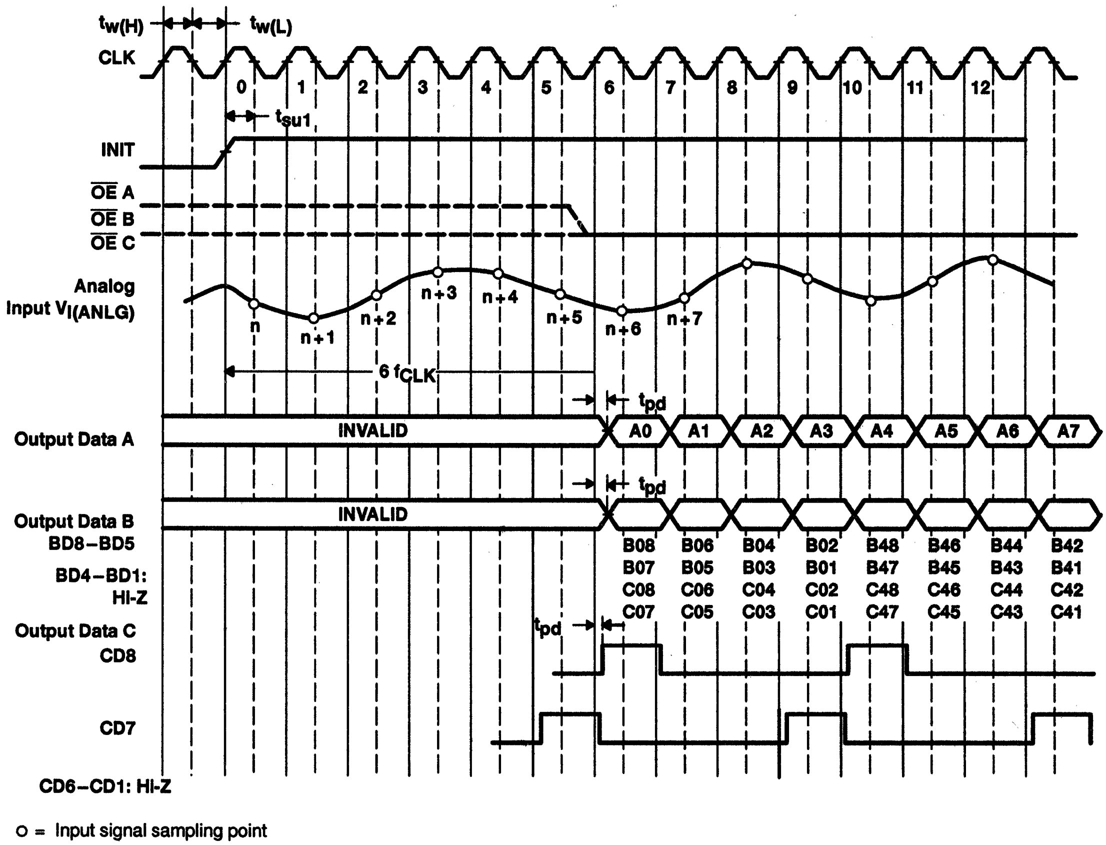


Figure 3. Format 1, 4:1:1

output data format (continued)

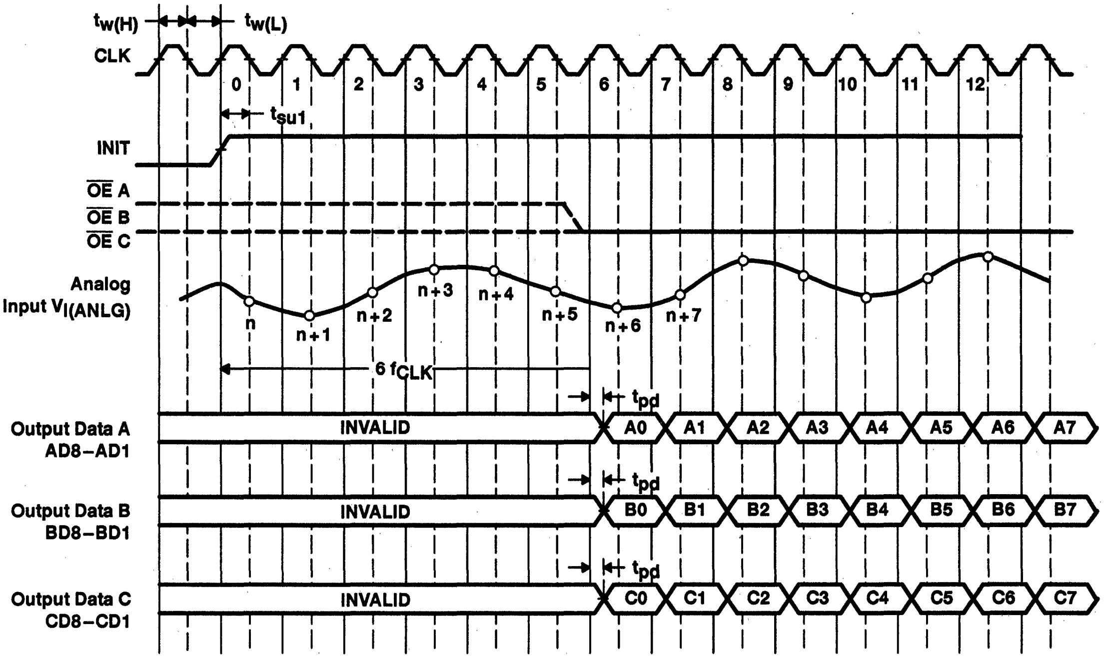
A06
- Bit
- Value of Sampling Data
- Channel of ADC

Table 6. Format 1

CHANNEL OF ADC	BIT	OUTPUT DATA							
A	AD8	A08	A18	A28	A38	A48	A58	A68	A78
	AD7	A07	A17	A27	A37	A47	A57	A67	A77
	AD6	A06	A16	A26	A36	A46	A56	A66	A76
	AD5	A05	A15	A25	A35	A45	A55	A65	A75
	AD4	A04	A14	A24	A34	A44	A54	A64	A74
	AD3	A03	A13	A23	A33	A43	A53	A63	A73
	AD2	A02	A12	A22	A32	A42	A52	A62	A72
	AD1	A01	A11	A21	A31	A41	A51	A61	A71
B	BD8	B08	B06	B04	B02	B48	B46	B44	B42
	BD7	B07	B05	B03	B01	B47	B45	B43	B41
	BD6	C08	C06	C04	C02	C48	C46	C44	C42
	BD5	C07	C05	C03	C01	C47	C45	C43	C41
	BD4	Hi-Z							
	BD3	Hi-Z							
	BD2	Hi-Z							
	BD1	Hi-Z							
C	CD8	H	L	L	L	H	L	L	L
	CD7	L	L	L	H	L	L	L	H
	CD6	Hi-Z							
	CD5	Hi-Z							
	CD4	Hi-Z							
	CD3	Hi-Z							
	CD2	Hi-Z							
	CD1	Hi-Z							
CLK (see Note 2)		6	7	8	9	10	11	12	13

NOTES: 1. Hi-Z = high impedance
2. The value of the first sampling clock at A–D conversion is CLK 0.

output data format (continued)



o = Input signal sampling point

Figure 4. Format 2, 4:4:4

output data format (continued)

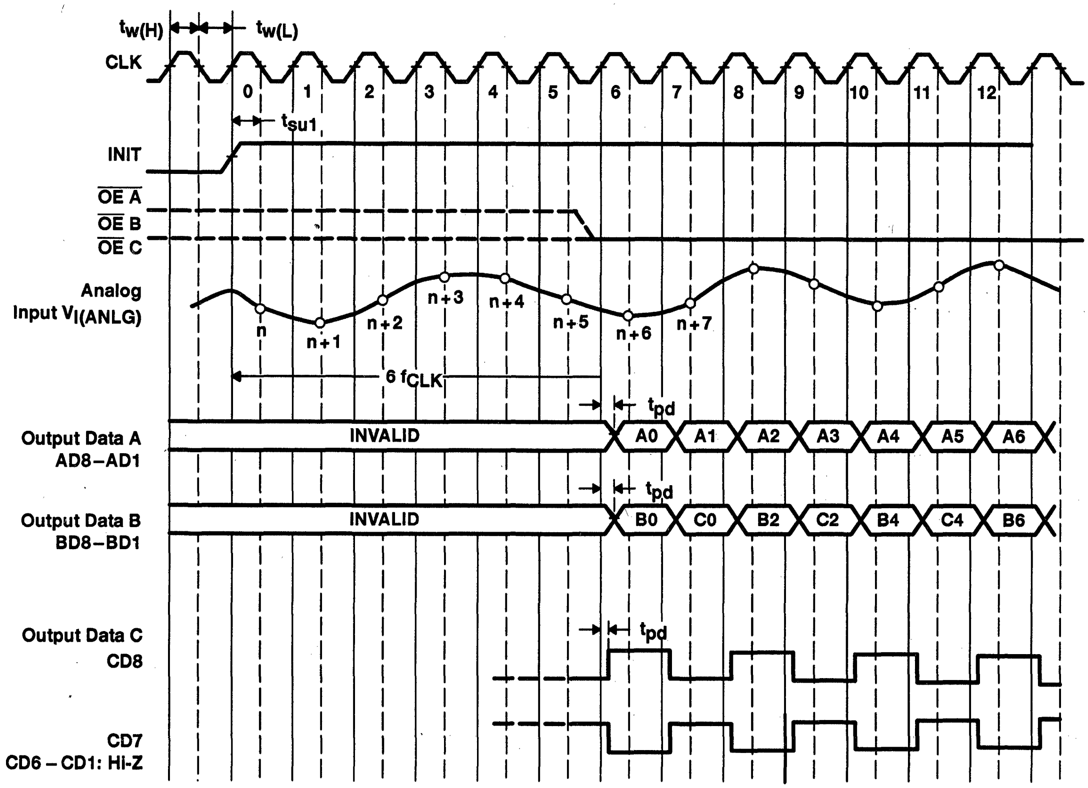
A06
- **Bit**
- **Value of Sampling Data**
- **Channel of ADC**

Table 7. Format 2

CHANNEL OF ADC	BIT	OUTPUT DATA							
A	AD8	A08	A18	A28	A38	A48	A58	A68	A78
	AD7	A07	A17	A27	A37	A47	A57	A67	A77
	AD6	A06	A16	A26	A36	A46	A56	A66	A76
	AD5	A05	A15	A25	A35	A45	A55	A65	A75
	AD4	A04	A14	A24	A34	A44	A54	A64	A74
	AD3	A03	A13	A23	A33	A43	A53	A63	A73
	AD2	A02	A12	A22	A32	A42	A52	A62	A72
	AD1	A01	A11	A21	A31	A41	A51	A61	A71
B	BD8	B08	B18	B28	B38	B48	B58	B68	B78
	BD7	B07	B17	B27	B37	B47	B57	B67	B77
	BD6	B06	B16	B26	B36	B46	B56	B66	B76
	BD5	B05	B15	B25	B35	B45	B55	B65	B75
	BD4	B04	B14	B24	B34	B44	B54	B64	B74
	BD3	B03	B13	B23	B33	B43	B53	B63	B73
	BD2	B02	B12	B22	B32	B42	B52	B62	B72
	BD1	B01	B11	B21	B31	B41	B51	B61	B71
C	CD8	C08	C18	C28	C38	C48	C58	C68	C78
	CD7	C07	C17	C27	C37	C47	C57	C67	C77
	CD6	C06	C16	C26	C36	C46	C56	C66	C76
	CD5	C05	C15	C25	C35	C45	C55	C65	C75
	CD4	C04	C14	C24	C34	C44	C54	C64	C74
	CD3	C03	C13	C23	C33	C43	C53	C63	C73
	CD2	C02	C12	C22	C32	C42	C52	C62	C72
	CD1	C01	C11	C21	C31	C41	C51	C61	C71
CLK (see Note 2)		6	7	8	9	10	11	12	13

NOTE 2: The value of the first sampling clock at A–D conversion is CLK 0.

output data format (continued)



o = Input signal sampling point

Figure 5. Format 3, 4:2:2

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output data format (continued)

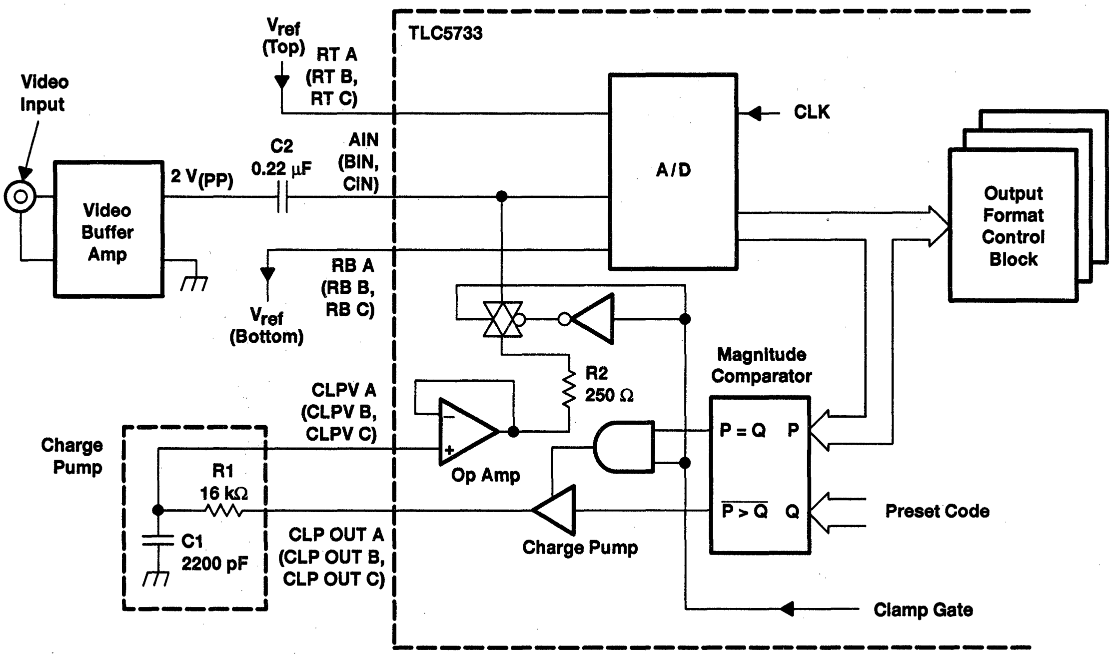
A06
- Bit
- Value of Sampling Data
- Channel of ADC

Table 8. Format 3

CHANNEL OF ADC	BIT	OUTPUT DATA							
A	AD8	A08	A18	A28	A38	A48	A58	A68	A78
	AD7	A07	A17	A27	A37	A47	A57	A67	A77
	AD6	A06	A16	A26	A36	A46	A56	A66	A76
	AD5	A05	A15	A25	A35	A45	A55	A65	A75
	AD4	A04	A14	A24	A34	A44	A54	A64	A74
	AD3	A03	A13	A23	A33	A43	A53	A63	A73
	AD2	A02	A12	A22	A32	A42	A52	A62	A72
	AD1	A01	A11	A21	A31	A41	A51	A61	A71
B	BD8	B08	C08	B28	C28	B48	C48	B68	C68
	BD7	B07	C07	B27	C27	B47	C47	B67	C67
	BD6	B06	C06	B26	C26	B46	C46	B66	C66
	BD5	B05	C05	B25	C25	B45	C45	B65	C65
	BD4	B04	C04	B24	C24	B44	C44	B64	C64
	BD3	B03	C03	B23	C23	B43	C43	B63	C63
	BD2	B02	C02	B22	C22	B42	C42	B62	C62
	BD1	B01	C01	B21	C21	B41	C41	B61	C61
C	CD8	H	L	H	L	H	L	H	L
	CD7	L	H	L	H	L	H	L	H
	CD6	Hi-Z							
	CD5	Hi-Z							
	CD4	Hi-Z							
	CD3	Hi-Z							
	CD2	Hi-Z							
	CD1	Hi-Z							
CLK (see Note 2)		6	7	8	9	10	11	12	13

NOTES: 1. Hi-Z = high impedance
2. The value of the first sampling clock at A–D conversion is CLK 0.

APPLICATION INFORMATION



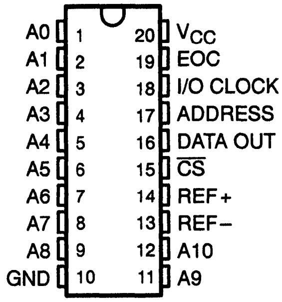
FUNCTION FOR FEEDBACK CLAMP AND CHARGE PUMP

INPUT DATA CONDITIONS	OUTPUT		CHARGE PUMP CONDITIONS
	$\overline{P=Q}$	$\overline{P>Q}$	
P < Q	Active	H	Charge
P = Q	Hold	Z	Hold
P > Q	Active	L	Discharge

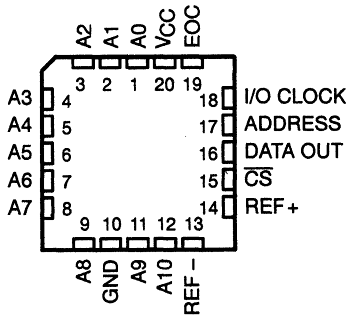
Figure 6. Feedback Clamp Circuit

- **3.3-V Supply Operation**
- **10-Bit-Resolution A/D Converter**
- **11 Analog Input Channels**
- **Three Built-In Self-Test Modes**
- **Inherent Sample and Hold**
- **Total Unadjusted Error . . . ±1 LSB Max**
- **On-Chip System Clock**
- **End-of-Conversion (EOC) Output**
- **Pin Compatible With TLC1543**
- **CMOS Technology**

**DB, DW, FK, J, OR N PACKAGE
(TOP VIEW)**



**FN PACKAGE
(TOP VIEW)**



description

The TLV1543C and TLV1543M are CMOS 10-bit, switched-capacitor, successive-approximation, analog-to-digital converters. These devices have three inputs and a 3-state output [chip select ($\overline{CS}$), input-output clock (I/O CLOCK), address input (ADDRESS), and data output (DATA OUT)] that provide a direct 4-wire interface to the serial port of a host processor. The devices allow high-speed data transfers from the host.

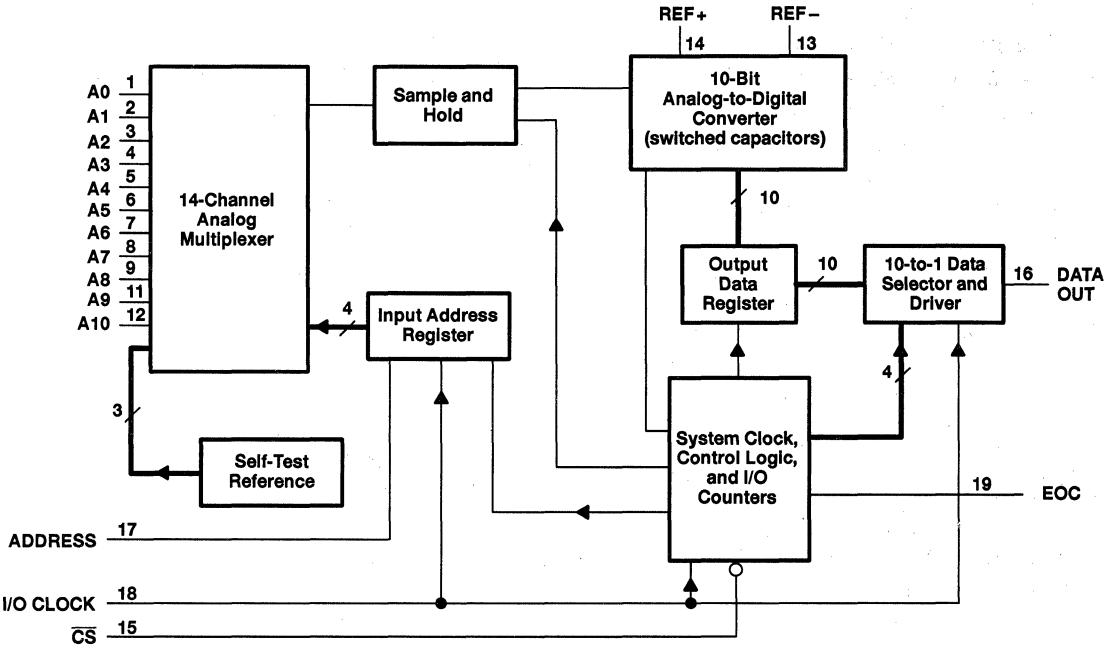
In addition to a high-speed A/D converter and versatile control capability, these devices have an on-chip 14-channel multiplexer that can select any one of 11 analog inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of A/D conversion, the end-of-conversion (EOC) output goes high to indicate that conversion is complete. The converter incorporated in the devices features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating free-air temperature range.

The TLV1543C is characterized for operation from 0°C to 70°C. The TLV1543M is characterized for operation over the full military temperature range of −55°C to 125°C.

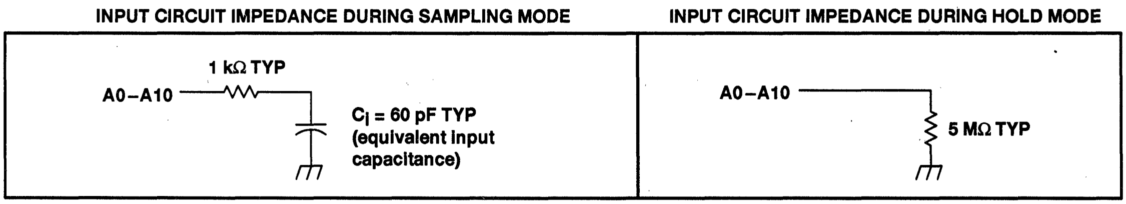
AVAILABLE OPTIONS

T_A	PACKAGE					
	SMALL OUTLINE (DB)	SMALL OUTLINE (DW)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	PLASTIC CHIP CARRIER (FN)
0°C to 70°C	TLV1543CDB	TLV1543CDW	—	—	TLV1543CN	TLV1543CFN
−55°C to 125°C	—	—	TLV1543MFK	TLV1543MJ	—	—

functional block diagram



typical equivalent inputs



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADDRESS	17	I	Serial address. A 4-bit serial address selects the desired analog input or test voltage that is to be converted next. The address data is presented with the MSB first and is shifted in on the first four rising edges of I/O CLOCK. After the four address bits have been read into the address register, ADDRESS is ignored for the remainder of the current conversion period.
A0–A10	1–9, 11, 12	I	Analog signal. The 11 analog inputs are applied to A0–A10 and are internally multiplexed. The driving source impedance should be less than or equal to 1 kΩ.
$\overline{CS}$	15	I	Chip select. A high-to-low transition on $\overline{CS}$ resets the internal counters and controls and enables DATA OUT, ADDRESS, and I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock. A low-to-high transition disables ADDRESS and I/O CLOCK within a setup time plus two falling edges of the internal system clock.
DATA OUT	16	O	The 3-state serial output for the A/D conversion result. DATA OUT is in the high-impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low. With a valid chip select, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB value of the previous conversion result. The next falling edge of I/O CLOCK drives DATA OUT to the logic level corresponding to the next most significant bit, and the remaining bits are shifted out in order with the LSB appearing on the ninth falling edge of I/O CLOCK. On the tenth falling edge of I/O CLOCK, DATA OUT is driven to a low logic level so that serial interface data transfers of more than ten clocks produce zeroes as the unused LSBs.
EOC	19	O	End of conversion. EOC goes from a high- to a low- logic level on the trailing edge of the tenth I/O CLOCK and remains low until the conversion is complete and data are ready for transfer.
GND	10	I	The ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
I/O CLOCK	18	I	Input/output clock. I/O CLOCK receives the serial I/O CLOCK input and performs the following four functions: 1) It clocks the four input address bits into the address register on the first four rising edges of I/O CLOCK with the multiplex address available after the fourth rising edge. 2) On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplex input begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLOCK. 3) It shifts the nine remaining bits of the previous conversion data out on DATA OUT. 4) It transfers control of the conversion to the internal state controller on the falling edge of the tenth clock.
REF+	14	I	The upper reference voltage value (nominally V_{CC}) is applied to REF+. The maximum input voltage range is determined by the difference between the voltage applied to REF+ and the voltage applied to the REF– terminal.
REF–	13	I	The lower reference voltage value (nominally ground) is applied to REF–.
V_{CC}	20	I	Positive supply voltage

detailed description

With chip select ($\overline{CS}$) inactive (high), the ADDRESS and I/O CLOCK inputs are initially disabled and DATA OUT is in the high-impedance state. When the serial interface takes $\overline{CS}$ active (low), the conversion sequence begins with the enabling of I/O CLOCK and ADDRESS and the removal of DATA OUT from the high-impedance state. The host then provides the 4-bit channel address to ADDRESS and the I/O CLOCK sequence to I/O CLOCK. During this transfer, the host serial interface also receives the previous conversion result from DATA OUT. I/O CLOCK receives an input sequence that is between 10 and 16 clocks long from the host. The first four I/O clocks load the address register with the 4-bit address on ADDRESS selecting the desired analog channel and the next six clocks providing the control timing for sampling the analog input.

detailed description (continued)

There are six basic serial interface timing modes that can be used with the device. These modes are determined by the speed of I/O CLOCK and the operation of $\overline{CS}$ as shown in Table 1. These modes are (1) a fast mode with a 10-clock transfer and $\overline{CS}$ inactive (high) between conversion cycles, (2) a fast mode with a 10-clock transfer and $\overline{CS}$ active (low) continuously, (3) a fast mode with an 11- to 16-clock transfer and $\overline{CS}$ inactive (high) between conversion cycles, (4) a fast mode with a 16-bit transfer and $\overline{CS}$ active (low) continuously, (5) a slow mode with an 11- to 16-clock transfer and $\overline{CS}$ inactive (high) between conversion cycles, and (6) a slow mode with a 16-clock transfer and $\overline{CS}$ active (low) continuously.

The MSB of the previous conversion appears on DATA OUT on the falling edge of $\overline{CS}$ in mode 1, mode 3, and mode 5, on the rising edge of EOC in mode 2 and mode 4, and following the 16th clock falling edge in mode 6. The remaining nine bits are shifted out on the next nine falling edges of I/O CLOCK. Ten bits of data are transmitted to the host through DATA OUT. The number of serial clock pulses used also depends on the mode of operation, but a minimum of ten clock pulses is required for conversion to begin. On the 10th clock falling edge, the EOC output goes low and returns to the high logic level when conversion is complete and the result can be read by the host. On the 10th clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero if the I/O CLOCK transfer is more than ten clocks long.

Table 1 lists the operational modes with respect to the state of $\overline{CS}$, the number of I/O serial transfer clocks that can be used, and the timing edge on which the MSB of the previous conversion appears at the output.

Table 1. Mode Operation

MODES		$\overline{CS}$	NO. OF I/O CLOCKS	MSB AT DATA OUT†	TIMING DIAGRAM
Fast Modes	Mode 1	High between conversion cycles	10	$\overline{CS}$ falling edge	Figure 9
	Mode 2	Low continuously	10	EOC rising edge	Figure 10
	Mode 3	High between conversion cycles	11 to 16‡	$\overline{CS}$ falling edge	Figure 11
	Mode 4	Low continuously	16‡	EOC rising edge	Figure 12
Slow Modes	Mode 5	High between conversion cycles	11 to 16‡	$\overline{CS}$ falling edge	Figure 13
	Mode 6	Low continuously	16‡	16th clock falling edge	Figure 14

† These edges also initiate serial-interface communication.
‡ No more than 16 clocks should be used.

fast modes

The device is in a fast mode when the serial I/O CLOCK data transfer is completed before the conversion is completed. With a 10-clock serial transfer, the device can only run in a fast mode since a conversion does not begin until the falling edge of the 10th I/O CLOCK.

mode 1: fast mode, $\overline{CS}$ inactive (high) between conversion cycles, 10-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O CLOCK transfers and each transfer is ten clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 2: fast mode, $\overline{CS}$ active (low) continuously, 10-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O CLOCK transfers and each transfer is ten clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions; the rising edge of EOC then begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previous conversion to appear immediately on this output.

mode 3: fast mode, $\overline{CS}$ inactive (high) between conversion cycles, 11- to 16-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 4: fast mode, $\overline{CS}$ active (low) continuously, 16-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions; the rising edge of EOC then begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previous conversion to appear immediately on this output.

slow modes

In a slow mode, the conversion is completed before the serial I/O CLOCK data transfer is completed. A slow mode requires a minimum 11-clock transfer into I/O CLOCK, and the rising edge of the eleventh clock must occur before the conversion period is complete; otherwise, the device loses synchronization with the host serial interface, and $\overline{CS}$ has to be toggled to initialize the system. The eleventh rising edge of the I/O CLOCK must occur within 9.5 μs after the tenth I/O clock falling edge.

mode 5: slow mode, $\overline{CS}$ inactive (high) between conversion cycles, 11- to 16-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 6: slow mode, $\overline{CS}$ active (low) continuously, 16-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions. The falling edge of the sixteenth I/O CLOCK then begins each sequence by removing DATA OUT from the low state, allowing the MSB of the previous conversion to appear immediately at DATA OUT. The device is then ready for the next 16-clock transfer initiated by the serial interface.

address bits

The 4-bit analog channel-select address for the next conversion cycle is presented to the ADDRESS terminal (MSB first) and is clocked into the address register on the first four leading edges of I/O CLOCK. This address selects one of 14 inputs (11 analog inputs or 3 internal test inputs).

analog inputs and test modes

The 11 analog inputs and the 3 internal test inputs are selected by the 14-channel multiplexer according to the input address as shown in Tables 2 and 3. The input multiplexer is a break-before-make type to reduce input-to-input noise injection resulting from channel switching.

Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK, and sampling continues for six I/O CLOCK periods. The sample is held on the falling edge of the tenth I/O CLOCK. The three test inputs are applied to the multiplexer, sampled, and converted in the same manner as the external analog inputs.

Table 2. Analog-Channel-Select Address

ANALOG INPUT SELECTED	VALUE SHIFTED INTO ADDRESS INPUT	
	BINARY	HEX
A0	0000	0
A1	0001	1
A2	0010	2
A3	0011	3
A4	0100	4
A5	0101	5
A6	0110	6
A7	0111	7
A8	1000	8
A9	1001	9
A10	1010	A

Table 3. Test-Mode-Select Address

INTERNAL SELF-TEST VOLTAGE SELECTED†	VALUE SHIFTED INTO ADDRESS INPUT		OUTPUT RESULT (HEX)‡
	BINARY	HEX	
$\frac{V_{ref+} - V_{ref-}}{2}$	1011	B	200
V_{ref-}	1100	C	000
V_{ref+}	1101	D	3FF

† V_{ref+} is the voltage applied to the REF + input, and V_{ref-} is the voltage applied to the REF – input.
‡ The output results shown are the ideal values and vary with the reference stability and with internal offsets.

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF–) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF–. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half the V_{CC} voltage), a bit 0 is placed in the output register and the 512-weight capacitor is switched to REF–. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and the 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are counted.

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to count and weigh the bits from MSB to LSB.

converter and analog input (continued)

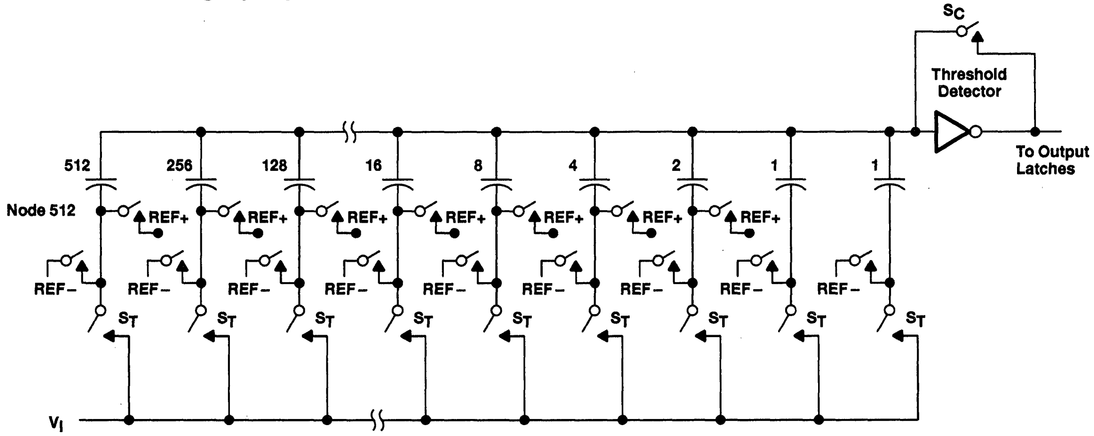


Figure 1. Simplified Model of the Successive-Approximation System

chip-select operation

The trailing edge of $\overline{CS}$ starts all modes of operation, and $\overline{CS}$ can abort a conversion sequence in any mode. A high-to-low transition on $\overline{CS}$ within the specified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the contents of the output data register remain at the previous conversion result). Exercise care to prevent $\overline{CS}$ from being taken low close to completion of conversion because the output data can be corrupted.

reference voltage inputs

There are two reference inputs used with these devices: REF+ and REF–. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero-scale reading respectively. The values of REF+, REF–, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and at zero when the input signal is equal to or lower than REF–.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1): TLV1543C	–0.5 V to 6.5 V
TLV1543M	–0.5 V to 6 V
Input voltage range, V_I (any input)	–0.3 V to V_{CC} + 0.3 V
Output voltage range, V_O	–0.3 V to V_{CC} + 0.3 V
Positive reference voltage, V_{ref+}	V_{CC} + 0.1 V
Negative reference voltage, V_{ref-}	–0.1 V
Peak input current (any input)	±20 mA
Peak total input current (all inputs)	±30 mA
Operating free-air temperature range, T_A: TLV1543C	0°C to 70°C
TLV1543M	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to digital ground with REF– and GND wired together (unless otherwise noted).

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	TLV1543C		3	3.3	5.5	V
	TLV1543M		3	3.3	3.6	V
Positive reference voltage, V_{ref+} (see Note 2)				V_{CC}		V
Negative reference voltage, V_{ref-} (see Note 2)				0		V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)			2.5	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)			0		V_{CC}	V
High-level control input voltage, V_{IH}	TLV1543C	V_{CC} = 3 V to 5.5 V	2			V
	TLV1543M	V_{CC} = 3 V to 3.6 V	2			V
Low-level control input voltage, V_{IL}	TLV1543C	V_{CC} = 3 V to 5.5 V			0.6	V
	TLV1543M	V_{CC} = 3 V to 3.6 V			0.8	V
Setup time, address bits at data input before I/O CLOCK↑, $t_{su(A)}$ (see Figure 4)			100			ns
Hold time, address bits after I/O CLOCK↑, $t_{h(A)}$ (see Figure 4)			0			ns
Hold time, $\overline{CS}$ low after last I/O CLOCK↓, $t_{h(CS)}$			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3)			1.425			µs
Clock frequency at I/O CLOCK (see Note 4)	TLC1543C		0		1.1	MHz
	TLC1543M		0		2.1	MHz
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$			190			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$			190			ns
Transition time, I/O CLOCK, $t_{t(I/O)}$ (see Note 5)					1	µs
Transition time, ADDRESS and $\overline{CS}$, $t_{t(CS)}$					10	µs
Operating free-air temperature, T_A	TLV1543C		0		70	°C
	TLV1543M		−55		125	°C

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF− convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.

3. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}$↓ before responding to control input signals. No attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

4. For 11- to 16-bit transfers, after the tenth I/O CLOCK falling edge (≤ 2 V), at least one I/O clock rising edge (≥ 2 V) must occur within 9.5 µs.

5. This is the time required for the clock input signal to fall from V_{IH}min to V_{IL}max or to rise from V_{IL}max to V_{IH}min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 µs for remote data-acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 3 V to 5.5 V, I/O CLOCK frequency = 1.1 MHz for the TLV1543C, $V_{CC} = V_{ref+}$ = 3 V to 3.6 V, I/O CLOCK frequency = 2.1 MHz for the TLV1543M (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	TLV1543C	V_{CC} = 3 V,	I_{OH} = –1.6 mA	2.4			V
			V_{CC} = 3 V to 5.5 V,	I_{OH} = 20 µA	V_{CC}–0.1			V
		TLV1543M	V_{CC} = 3 V,	I_{OH} = –1.6 mA	2.4			V
			V_{CC} = 3 V to 3.6 V,	I_{OH} = 20 µA	V_{CC}–0.1			V
V_{OL}	Low-level output voltage	TLV1543C	V_{CC} = 3 V,	I_{OL} = 1.6 mA			0.4	V
			V_{CC} = 3 V to 5.5 V,	I_{OL} = 20 µA			0.1	V
		TLV1543M	V_{CC} = 3 V,	I_{OL} = 1.6 mA			0.4	V
			V_{CC} = 3 V to 3.6 V,	I_{OL} = 20 µA			0.1	V
I_{OZ}	Off-state (high-impedance-state) output current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}			10	µA
			V_O = 0,	$\overline{CS}$ at V_{CC}			–10	
I_{IH}	High-level input current		$V_I = V_{CC}$			0.005	2.5	µA
I_{IL}	Low-level input current		V_I = 0			–0.005	–2.5	µA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			0.8	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC},	Unselected channel at 0 V			1	µA
			Selected channel at 0 V,	Unselected channel at V_{CC}			–1	
	Maximum static analog reference current into REF +		$V_{ref+} = V_{CC}$,	V_{ref-} = GND			10	µA
C_i	Input capacitance, Analog inputs	TLV1543C				7	55	pF
		TLV1543M				7		
	Input capacitance, Control inputs	TLV1543C				5	15	pF
		TLV1543M				5		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 3 V to 5.5 V, I/O CLOCK frequency = 1.1 MHz for the TLV1543C, $V_{CC} = V_{ref+}$ = 3 V to 3.6 V, I/O CLOCK frequency = 2.1 MHz for the TLV1543M

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Linearity error (see Note 6)				±1	LSB
	Zero error (see Note 7)	See Note 2			±1	LSB
	Full-scale error (see Note 7)	See Note 2			±1	LSB
	Total unadjusted error (see Note 8)				±1	LSB
	Self-test output code (see Table 3 and Note 9)	ADDRESS = 1011		512		
		ADDRESS = 1100		0		
		ADDRESS = 1101		1023		
t_{conv}	Conversion time	See Figures 9–14			21	µs
t_c	Total cycle time (access, sample, and conversion)	See Figures 9–14 and Note 10			21 +10 I/O CLOCK periods	µs
t_{acq}	Channel acquisition time (sample)	See Figures 9–14 and Note 10			6	I/O CLOCK periods
t_v	Valid time, DATA OUT remains valid after I/O CLOCK↓	See Figure 6	10			ns
$t_{d(I/O-DATA)}$	Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 6			240	ns
$t_{d(I/O-EOC)}$	Delay time, tenth I/O CLOCK↓ to EOC↓	See Figure 7		70	240	ns
$t_{d(EOC-DATA)}$	Delay time, EOC↑ to DATA OUT (MSB)	See Figure 8			100	ns
t_{PZH}, t_{PZL}	Enable time, $\overline{CS}$↓ to DATA OUT (MSB driven)	See Figure 3			1.3	µs
t_{PHZ}, t_{PLZ}	Disable time, $\overline{CS}$↑ to DATA OUT (high impedance)	See Figure 3			150	ns
$t_{r(EOC)}$	Rise time, EOC	See Figure 8			300	ns
$t_{f(EOC)}$	Fall time, EOC	See Figure 7			300	ns
$t_{r(bus)}$	Rise time, data bus	See Figure 6			300	ns
$t_{f(bus)}$	Fall time, data bus	See Figure 6			300	ns
$t_{d(I/O-CS)}$	Delay time, tenth I/O CLOCK↓ to $\overline{CS}$↓ to abort conversion (see Note 11)				9	µs

† All typical values are at T_A = 25°C.

NOTES:
2. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF– convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.
6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
7. Zero-scale error is the difference between 0000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.
8. Total unadjusted error comprises linearity, zero-scale, and full-scale errors.
9. Both the input address and the output codes are expressed in positive logic.
10. I/O CLOCK period = 1/(I/O CLOCK frequency) (see Figure 6).
11. Any transitions of $\overline{CS}$ are recognized as valid only if the level is maintained for a setup time plus two falling edges of the internal clock (1.425 µs) after the transition.

PARAMETER MEASUREMENT INFORMATION

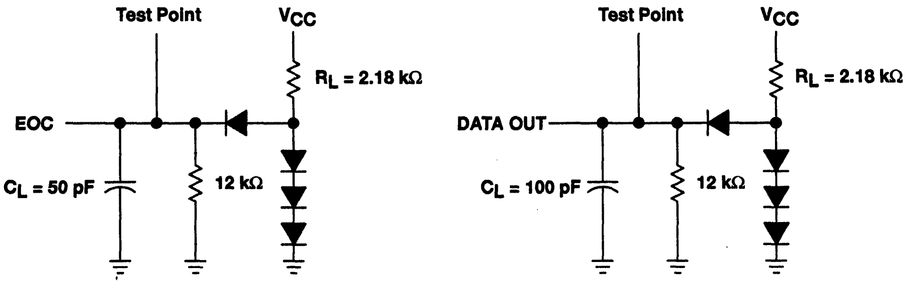


Figure 2. Load Circuits

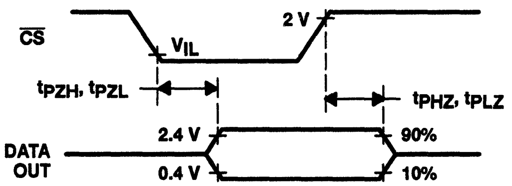


Figure 3. DATA OUT to Hi-Z Voltage Waveforms

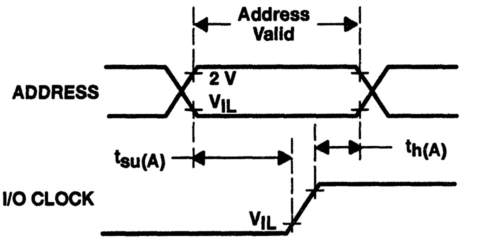


Figure 4. ADDRESS Setup Voltage Waveforms

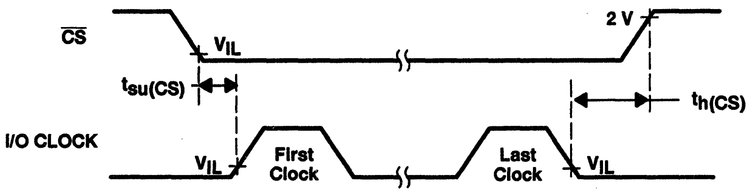


Figure 5. $\overline{CS}$ and I/O CLOCK Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

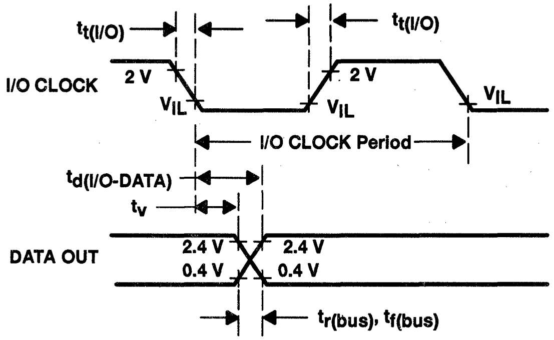


Figure 6. DATA OUT and I/O CLOCK Voltage Waveforms

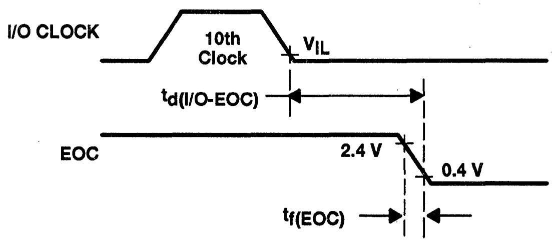


Figure 7. I/O CLOCK and EOC Voltage Waveforms

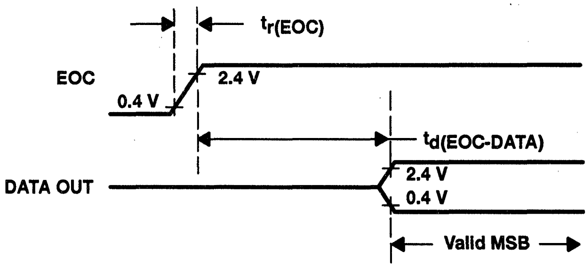


Figure 8. EOC and DATA OUT Voltage Waveforms

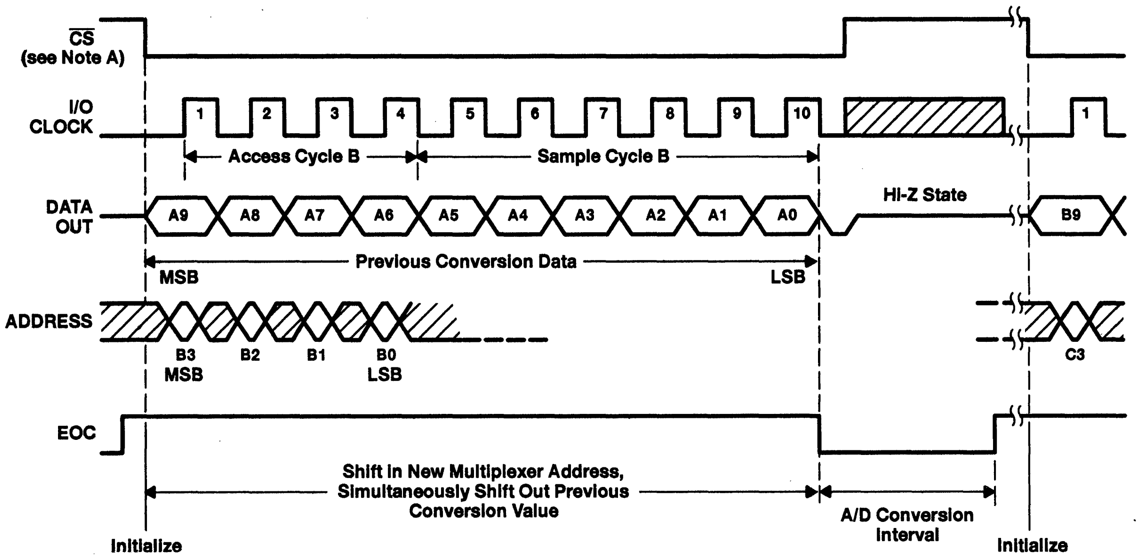


Figure 9. Timing for 10-Clock Transfer Using $\overline{CS}$

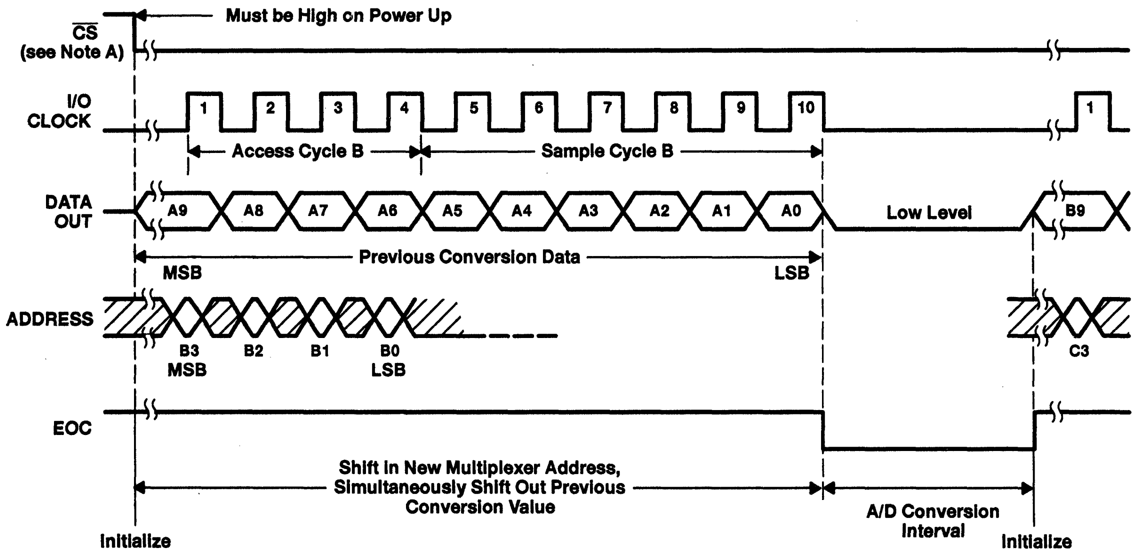


Figure 10. Timing for 10-Clock Transfer Not Using $\overline{CS}$

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

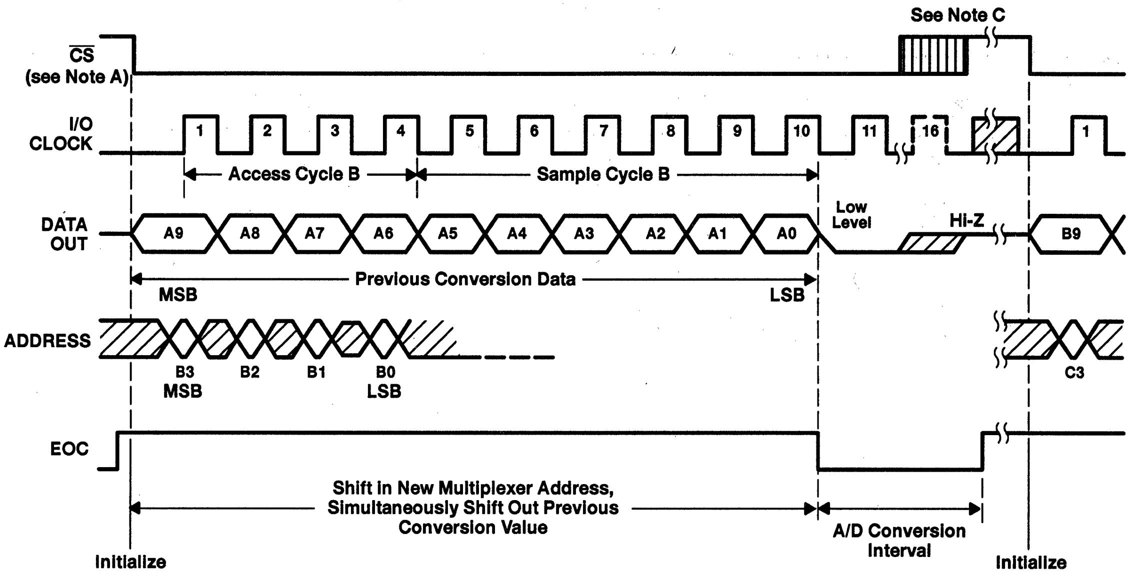


Figure 11. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$ (Serial Transfer Interval Shorter Than Conversion)

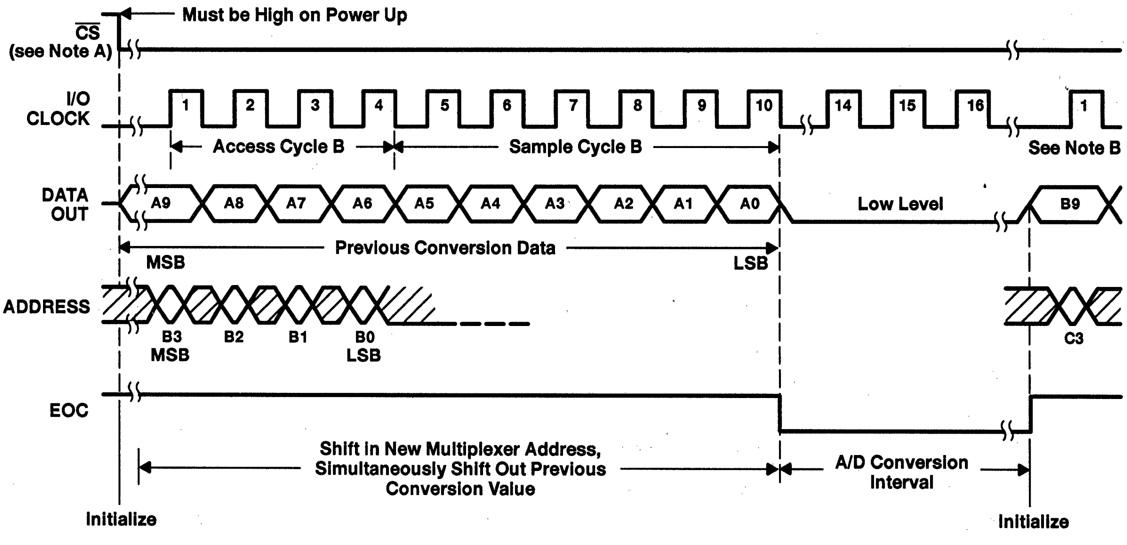


Figure 12. Timing for 16-Clock Transfer Not Using $\overline{CS}$ (Serial Transfer Interval Shorter Than Conversion)

NOTES: A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a set up time plus two falling edges of the internal system clock after $\overline{CS}$↓ before responding to control input signals. No attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

B. The first I/O CLOCK must occur after the rising edge of EOC.

C. A low-to-high transition of $\overline{CS}$ disables ADDRESS and the I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.

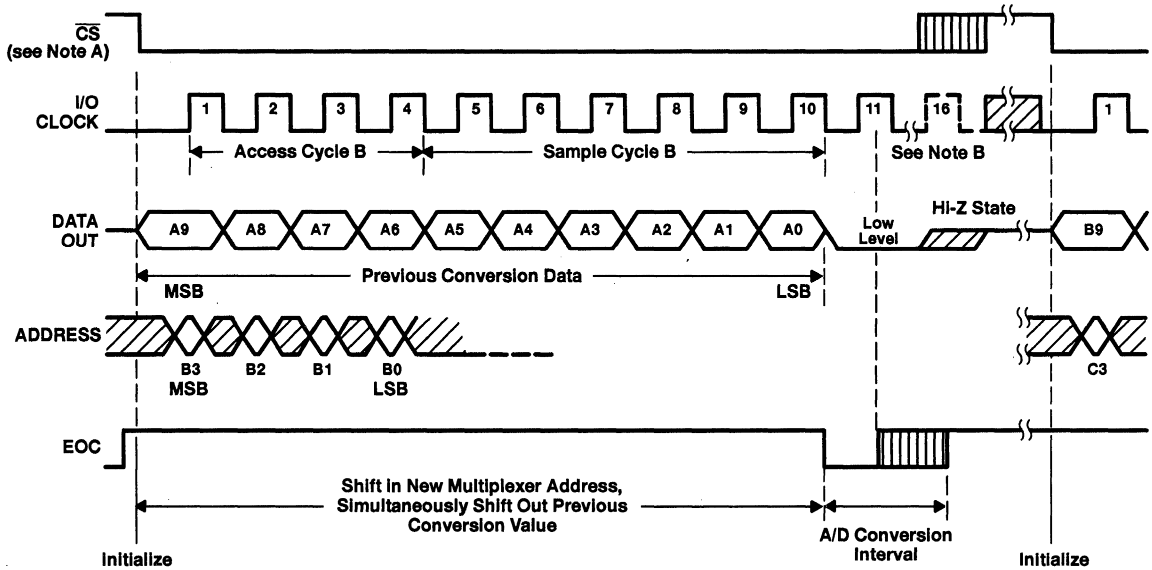


Figure 13. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$ (Serial Transfer Interval Longer Than Conversion)

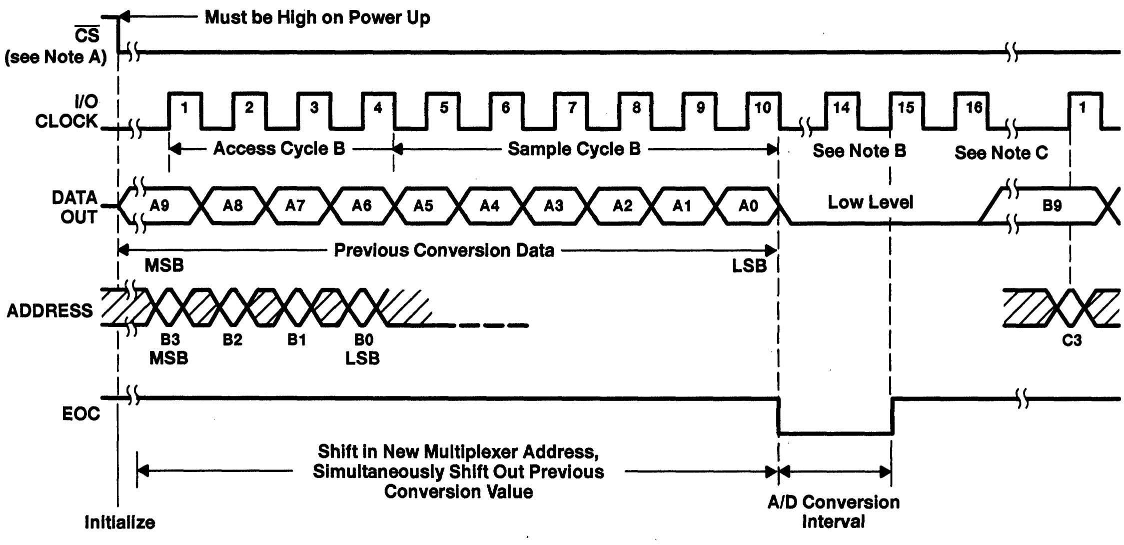


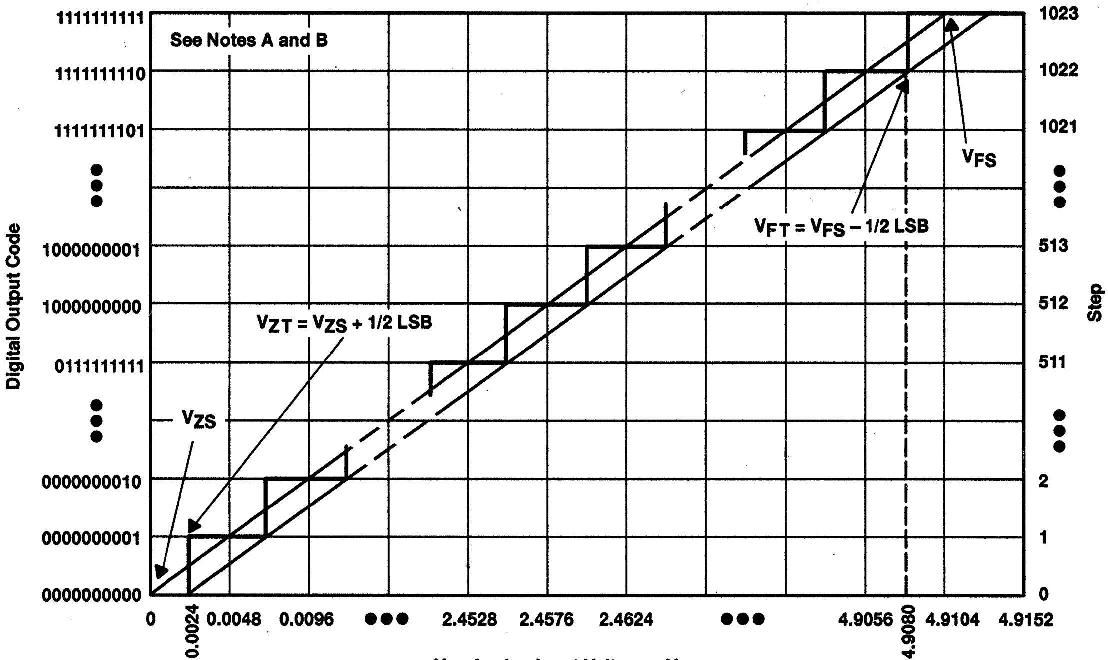
Figure 14. Timing for 16-Clock Transfer Not Using $\overline{CS}$ (Serial Transfer Interval Longer Than Conversion)

NOTES: A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a set up time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in an address until the minimum chip $\overline{CS}$ setup time has elapsed.

B. The eleventh rising edge of the I/O CLOCK sequence must occur before the conversion is complete to prevent losing serial interface synchronization.

C. The I/O CLOCK sequence is exactly 16 clock pulses long.

APPLICATION INFORMATION



NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0024 V and the transition to full scale (V_{FT}) is 4.908 V. 1 LSB = 4.8 mV.

B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 15. Ideal Conversion Characteristics

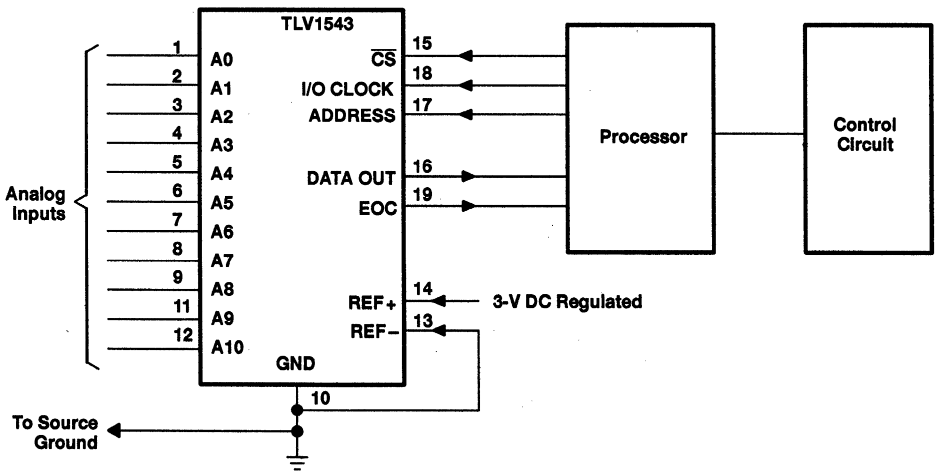


Figure 16. Serial Interface

APPLICATION INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 17, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S\left(1-e^{-t_c/R_tC_i}\right) \tag{1}$$

where

$R_t = R_s + r_i$

The final voltage to 1/2 LSB is given by

$$V_C\ (1/2\ \text{LSB}) = V_S - (V_S/2048) \tag{2}$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S/2048) = V_S\left(1-e^{-t_c/R_tC_i}\right) \tag{3}$$

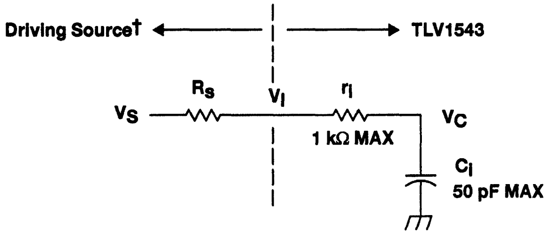
and

$$t_c\ (1/2\ \text{LSB}) = R_t \times C_i \times \ln(2048) \tag{4}$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c\ (1/2\ \text{LSB}) = (R_s + 1\ \text{k}\Omega) \times 60\ \text{pF} \times \ln(2048) \tag{5}$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at A0–A10
V_S = External Driving Source Voltage
R_s = Source Resistance
r_i = Input Resistance
C_i = Input Capacitance

† Driving source requirements:
- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_s must be real at the input frequency.

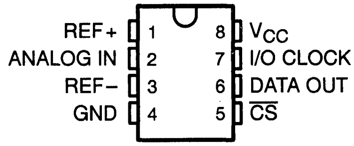
Figure 17. Equivalent Input Circuit Including the Driving Source

TLV1549C, TLV1549I, TLV1549M
10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

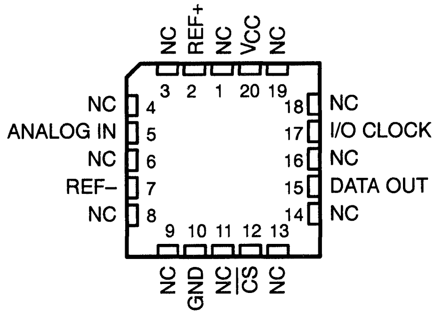
SLAS071C – JANUARY 1993 – REVISED MARCH 1995

- **3.3-V Supply Operation**
- **10-Bit-Resolution Analog-to-Digital Converter (ADC)**
- **Inherent Sample and Hold Function**
- **Total Unadjusted Error . . . ±1 LSB Max**
- **On-Chip System Clock**
- **Terminal Compatible With TLC1549 and TLC1549x**
- **Application Report Available†**
- **CMOS Technology**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLV1549C, TLV1549I, and TLV1549M are 10-bit, switched-capacitor, successive-approximation, analog-to-digital converters. The devices have two digital inputs and a 3-state output [chip select ($\overline{CS}$), input-output clock (I/O CLOCK), and data output (DATA OUT)] that provide a three-wire interface to the serial port of a host processor.

The sample-and-hold function is automatic. The converter incorporated in the device features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating free-air temperature range.

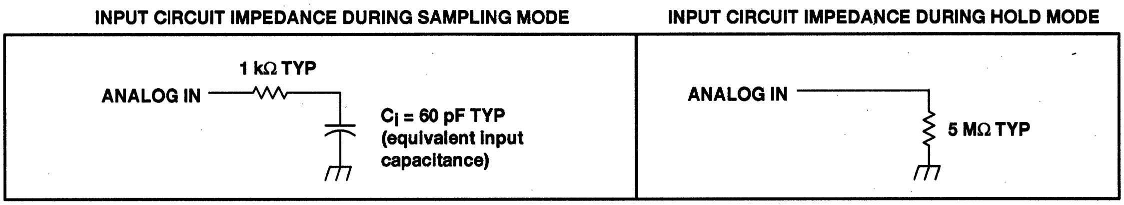
The TLV1549C is characterized for operation from 0°C to 70°C. The TLV1549I is characterized for operation from −40°C to 85°C. The TLV1549M is characterized for operation over the full military temperature range of −55°C to 125°C.

AVAILABLE OPTIONS

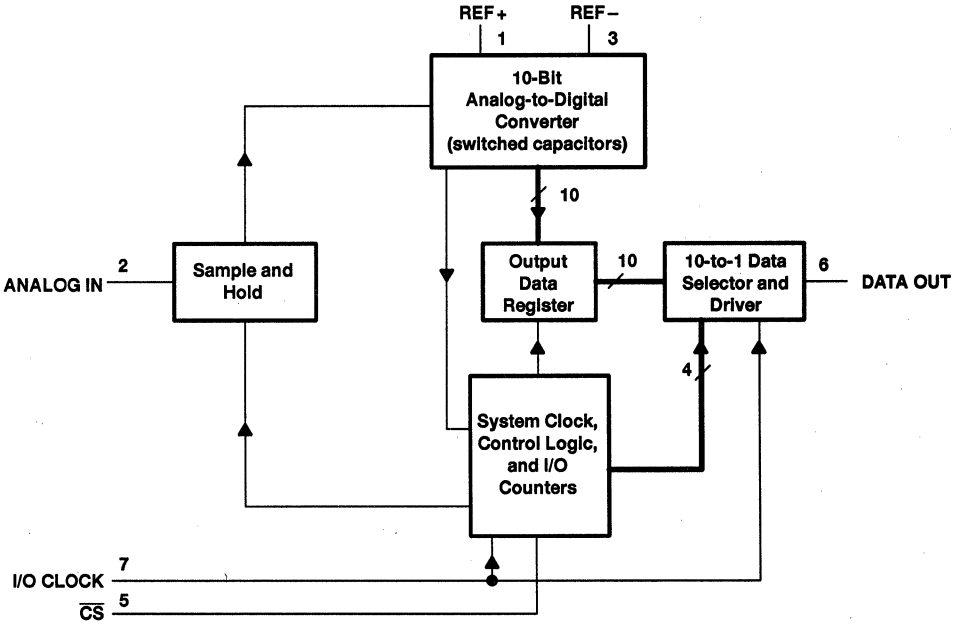
T_A	PACKAGE			
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	TLV1549CD	—	—	TLV1549CP
−40°C to 85°C	TLV1549ID	—	—	TLV1549IP
−55°C to 125°C	—	TLV1549MFK	TLV1549MJG	—

† Interfacing the TLV1549 10-Bit Serial-Out ADC to Popular 3.3-V Microcontrollers (SLAA005)

typical equivalent inputs



functional block diagram



Terminal numbers shown are for the D, JG, and P packages only.

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ANALOG IN	2	I	Analog input. The driving source impedance should be ≤ 1 kΩ. The external driving source to ANALOG IN should have a current capability ≥ 10 mA.
$\overline{CS}$	5	I	Chip select. A high-to-low transition on $\overline{CS}$ resets the internal counters and controls and enables DATA OUT and I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock. A low-to-high transition disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.
DATA OUT	6	O	This 3-state serial output for the A/D conversion result is in the high-impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low. With a valid chip select, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB value of the previous conversion result. The next falling edge of I/O CLOCK drives DATA OUT to the logic level corresponding to the next most significant bit, and the remaining bits are shifted out in order with the LSB appearing on the ninth falling edge of I/O CLOCK. On the tenth falling edge of I/O CLOCK, DATA OUT is driven to a low logic level so that serial interface data transfers of more than ten clocks produce zeroes as the unused LSBs.
GND	4	I	The ground return for internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
I/O CLOCK	7	I	The input/output clock receives the serial I/O CLOCK input and performs the following three functions: 1) On the third falling edge of I/O CLOCK, the analog input voltage begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLOCK. 2) It shifts the nine remaining bits of the previous conversion data out on DATA OUT. 3) It transfers control of the conversion to the internal state controller on the falling edge of the tenth clock.
REF+	1	I	The upper reference voltage value (nominally V_{CC}) is applied to REF+. The maximum input voltage range is determined by the difference between the voltage applied to REF+ and the voltage applied to REF–.
REF–	3	I	The lower reference voltage value (nominally ground) is applied to this REF–.
V_{CC}	8	I	Positive supply voltage

detailed description

With chip select ($\overline{CS}$) inactive (high), the I/O CLOCK input is initially disabled and DATA OUT is in the high-impedance state. When the serial interface takes $\overline{CS}$ active (low), the conversion sequence begins with the enabling of I/O CLOCK and the removal of DATA OUT from the high-impedance state. The serial interface then provides the I/O CLOCK sequence to I/O CLOCK and receives the previous conversion result from DATA OUT. I/O CLOCK receives an input sequence that is between 10 and 16 clocks long from the host serial interface. The first ten I/O clocks provide the control timing for sampling the analog input.

There are six basic serial interface timing modes that can be used with the TLV1549. These modes are determined by the speed of I/O CLOCK and the operation of $\overline{CS}$ as shown in Table 1. These modes are: (1) a fast mode with a 10-clock transfer and $\overline{CS}$ inactive (high) between transfers, (2) a fast mode with a 10-clock transfer and $\overline{CS}$ active (low) continuously, (3) a fast mode with an 11- to 16-clock transfer and $\overline{CS}$ inactive (high) between transfers, (4) a fast mode with a 16-bit transfer and $\overline{CS}$ active (low) continuously, (5) a slow mode with an 11- to 16-clock transfer and $\overline{CS}$ inactive (high) between transfers, and (6) a slow mode with a 16-clock transfer and $\overline{CS}$ active (low) continuously.

The MSB of the previous conversion appears on DATA OUT on the falling edge of $\overline{CS}$ in mode 1, mode 3, and mode 5, within 21 μs from the falling edge of the tenth I/O CLOCK in mode 2 and mode 4, and following the 16th clock falling edge in mode 6. The remaining nine bits are shifted out on the next nine falling edges of the I/O CLOCK. Ten bits of data are transmitted to the host serial interface through DATA OUT. The number of serial clock pulses used also depends on the mode of operation, but a minimum of ten clock pulses is required for conversion to begin. On the tenth clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero if the I/O CLOCK transfer is more than ten clocks long.

Table 1 lists the operational modes with respect to the state of $\overline{CS}$, the number of I/O serial transfer clocks that can be used, and the timing on which the MSB of the previous conversion appears at the output.

Table 1. Mode Operation

MODES		$\overline{CS}$	NO. OF I/O CLOCKS	MSB AT DATA OUT†	TIMING DIAGRAM
Fast Modes	Mode 1	High between conversion cycles	10	$\overline{CS}$ falling edge	Figure 6
	Mode 2	Low continuously	10	Within 21 µs	Figure 7
	Mode 3	High between conversion cycles	11 to 16‡	$\overline{CS}$ falling edge	Figure 8
	Mode 4	Low continuously	16‡	Within 21 µs	Figure 9
Slow Modes	Mode 5	High between conversion cycles	11 to 16‡	$\overline{CS}$ falling edge	Figure 10
	Mode 6	Low continuously	16‡	16th clock falling edge	Figure 11

† This timing also initiates serial-interface communication.
‡ No more than 16 clocks should be used.

All the modes require a minimum period of 21 µs after the falling edge of the tenth I/O CLOCK before a new transfer sequence can begin. During a serial I/O CLOCK data transfer, $\overline{CS}$ must be active (low) so that the I/O CLOCK input is enabled. When $\overline{CS}$ is toggled between data transfers (modes 1, 3, and 5), the transitions at $\overline{CS}$ are recognized as valid only if the level is maintained for a minimum period of 1.425 µs after the transition. If the transfer is more than ten I/O clocks (modes 3, 4, 5, and 6), the rising edge of the eleventh clock must occur within 9.5 µs after the falling edge of the tenth I/O CLOCK; otherwise, the device could lose synchronization with the host serial interface and $\overline{CS}$ has to be toggled to restore proper operation.

fast modes

The device is in a fast mode when the serial I/O CLOCK data transfer is completed within 21 µs from the falling edge of the tenth I/O CLOCK. With a 10-clock serial transfer, the device can only run in a fast mode.

mode 1: fast mode, $\overline{CS}$ inactive (high) between transfers, 10-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O-CLOCK transfers and each transfer is ten clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 2: fast mode, $\overline{CS}$ active (low) continuously, 10-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O-CLOCK transfers and each transfer is ten clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions. Within 21 µs after the falling edge of the tenth I/O CLOCK, the MSB of the previous conversion appears at DATA OUT.

mode 3: fast mode, $\overline{CS}$ inactive (high) between transfers, 11- to 16-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O-CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 4: fast mode, $\overline{CS}$ active (low) continuously, 16-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O-CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions. Within 21 µs after the falling edge of the tenth I/O CLOCK, the MSB of the previous conversion appears at DATA OUT.

slow modes

In a slow mode, the serial I/O CLOCK data transfer is completed after 21 µs from the falling edge of the tenth I/O CLOCK.

mode 5: slow mode, $\overline{CS}$ inactive (high) between transfers, 11- to 16-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O-CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 6: slow mode, $\overline{CS}$ active (low) continuously, 16-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O-CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions. The falling edge of the sixteenth I/O CLOCK then begins each sequence by removing DATA OUT from the low state, allowing the MSB of the previous conversion to appear immediately at DATA OUT. The device is then ready for the next 16-clock transfer initiated by the serial interface.

analog input sampling

Sampling of the analog input starts on the falling edge of the third I/O CLOCK, and sampling continues for seven I/O CLOCK periods. The sample is held on the falling edge of the tenth I/O CLOCK.

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF–) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF–. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half V_{CC}), a bit 0 is placed in the output register and the 512-weight capacitor is switched to REF–. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and this 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are determined.

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to determine the bits from MSB to LSB.

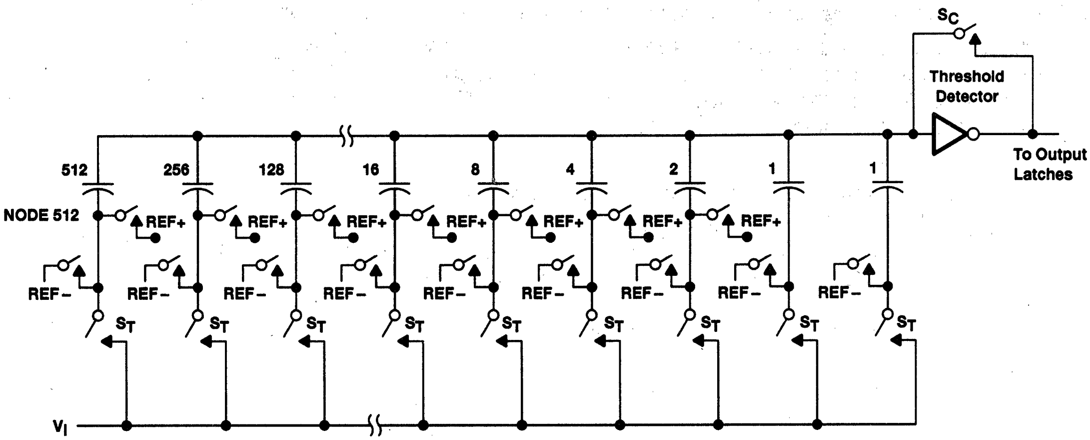


Figure 1. Simplified Model of the Successive-Approximation System

chip-select operation

The trailing edge of $\overline{CS}$ starts all modes of operation, and $\overline{CS}$ can abort a conversion sequence in any mode. A high-to-low transition on $\overline{CS}$ within the specified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the contents of the output data register remain at the previous conversion result). Exercise care to prevent $\overline{CS}$ from being taken low close to completion of conversion because the output data may be corrupted.

reference voltage inputs

There are two reference inputs used with the TLV1549: REF+ and REF–. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero reading, respectively. The values of REF+, REF–, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and at zero when the input signal is equal to or lower than REF–.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1):	TLV1549C	–0.5 V to 6.5 V
	TLV1549I	–0.5 V to 6.5 V
	TLV1549M	–0.5 V to 6 V
Input voltage range, V_I (any input)		–0.3 V to V_{CC} + 0.3 V
Output voltage range, V_O		–0.3 V to V_{CC} + 0.3 V
Positive reference voltage, V_{ref+}		V_{CC} + 0.1 V
Negative reference voltage, V_{ref-}		–0.1 V
Peak input current (any input)		±20 mA
Peak total input current (all inputs)		±30 mA
Operating free-air temperature range, T_A:	TLV1549C	0°C to 70°C
	TLV1549I	–40°C to 85°C
	TLV1549M	–55°C to 125°C
Storage temperature range, T_{stg}		–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds		260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to ground with REF– and GND wired together (unless otherwise noted).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
Positive reference voltage, V_{ref+} (see Note 2)			V_{CC}		V
Negative reference voltage, V_{ref-} (see Note 2)			0		V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)		2.5	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)		0		V_{CC}	V
High-level control input voltage, V_{IH}	V_{CC} = 3 V to 3.6 V	2			V
Low-level control input voltage, V_{IL}	V_{CC} = 3 V to 3.6 V			0.6	V
Clock frequency at I/O CLOCK (see Note 3)		0		2.1	MHz
Setup time, $\overline{CS}$ low before first I/O CLOCK↑, $t_{su(CS)}$ (see Note 4)		1.425			µs
Hold time, $\overline{CS}$ low after last I/O CLOCK↓, $t_{h(CS)}$		0			ns
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$		190			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$		190			ns
Transition time, I/O CLOCK, $t_{t(I/O)}$ (see Note 5 and Figure 5)				1	µs
Transition time, $\overline{CS}$, $t_{t(CS)}$				10	µs
Operating free-air temperature, T_A	TLV1549C	0		70	°C
	TLV1549I	−40		85	°C
	TLV1549M	−55		125	°C

NOTES: 2. Analog input voltages greater than that applied to REF + convert as all ones (1111111111), while input voltages less than that applied to REF – convert as all zeros (0000000000). The TLV1549 is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.

3. For 11- to 16-bit transfers, after the tenth I/O CLOCK falling edge (≤ 2 V), at least one I/O CLOCK rising edge (≥ 2 V) must occur within 9.5 µs.

4. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}$↓ before responding to the I/O CLOCK. Therefore, no attempt should be made to clock out the data until the minimum $\overline{CS}$ setup time has elapsed.

5. This is the time required for the clock input signal to fall from V_{IH}min to V_{IL}max or to rise from V_{IL}max to V_{IH}min. In the vicinity of normal room temperature, the device functions with input clock transition time as slow as 1 µs for remote data-acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 3 V to 3.6 V, I/O CLOCK frequency = 2.1 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 3 V,	I_{OH} = –1.6 mA	2.4			V
			V_{CC} = 3 V to 3.6 V,	I_{OH} = –20 µA	V_{CC}–0.1			
V_{OL}	Low-level output voltage		V_{CC} = 3 V,	I_{OL} = 1.6 mA			0.4	V
			V_{CC} = 3 V to 3.6 V,	I_{OL} = 20 µA			0.1	
I_{OZ}	Off-state (high-impedance-state) output current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}			10	µA
			V_O = 0,	$\overline{CS}$ at V_{CC}			–10	
I_{IH}	High-level input current		$V_I = V_{CC}$			0.005	2.5	µA
I_{IL}	Low-level input current		V_I = 0			–0.005	–2.5	µA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			0.4	2.5	mA
	Analog input leakage current		$V_I = V_{CC}$				1	µA
			V_I = 0				–1	
	Maximum static analog reference current into REF+		$V_{ref+} = V_{CC}$,	V_{ref-} = GND			10	µA
C_i	Input capacitance	TLV1549C, I (Analog)	During sample cycle			30	55	pF
		TLV1549M, (Analog)	During sample cycle			30		
		TLV1549C, I (Control)				5	15	
		TLV1549M, (Control)				5		

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 3 V to 3.6 V, I/O CLOCK frequency = 2.1 MHz

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
	Linearity error (see Note 6)			±1	LSB
	Zero error (see Note 7)	See Note 2		±1	LSB
	Full-scale error (see Note 7)	See Note 2		±1	LSB
	Total unadjusted error (see Note 8)			±1	LSB
t_{conv}	Conversion time	See Figures 6–11		21	μs
t_c	Total cycle time (access, sample, and conversion)	See Figures 6–11 and Note 9		21 +10 I/O CLOCK periods	μs
t_v	Valid time, DATA OUT remains valid after I/O CLOCK↓	See Figure 5	10		ns
$t_{d(I/O\text{-}DATA)}$	Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 5		240	ns
t_{PZH}, t_{PZL}	Enable time, $\overline{CS}$↓ to DATA OUT (MSB driven)	See Figure 3		1.3	μs
t_{PHZ}, t_{PLZ}	Disable time, $\overline{CS}$↑ to DATA OUT (high impedance)	See Figure 3		180	ns
$t_{r(bus)}$	Rise time, data bus	See Figure 5		300	ns
$t_{f(bus)}$	Fall time, data bus	See Figure 5		300	ns
$t_{d(I/O\text{-}CS)}$	Delay time, 10th I/O CLOCK↓ to $\overline{CS}$↓ to abort conversion (see Note 10)			9	μs

NOTES:
2. Analog input voltages greater than that applied to REF + convert as all ones (1111111111), while input voltages less than that applied to REF – convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V ($V_{ref+} - V_{ref-}$); however, the electrical specifications are no longer applicable.
6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
7. Zero error is the difference between 0000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.
8. Total unadjusted error comprises linearity, zero, and full-scale errors.
9. I/O CLOCK period = 1/(I/O CLOCK frequency). Sampling begins on the falling edge of the third I/O CLOCK, continues for seven I/O CLOCK periods, and ends on the falling edge of the tenth I/O CLOCK (see Figure 5).
10. Any transitions of $\overline{CS}$ are recognized as valid only if the level is maintained for a minimum of a setup time plus two falling edges of the internal clock (1.425 μs) after the transition.

PARAMETER MEASUREMENT INFORMATION

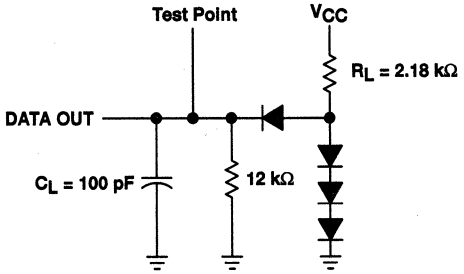


Figure 2. Load Circuit

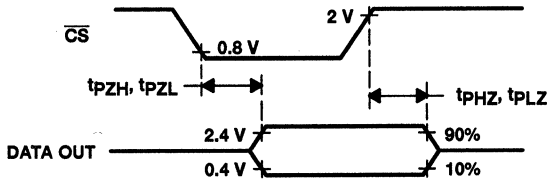


Figure 3. DATA OUT to Hi-Z Voltage Waveforms

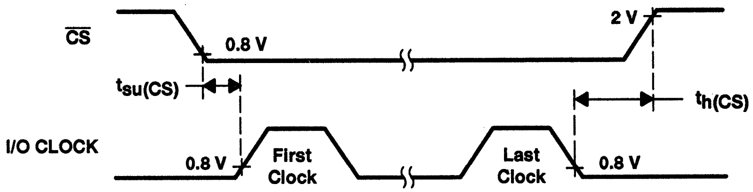


Figure 4. $\overline{CS}$ to I/O CLOCK Voltage Waveforms

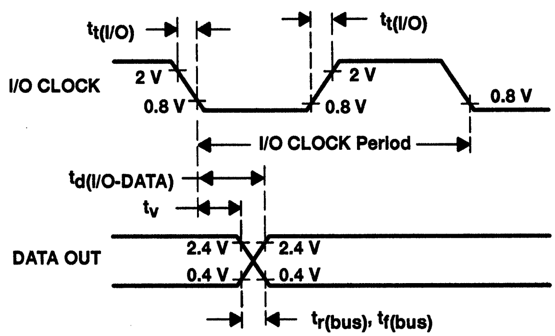


Figure 5. I/O CLOCK and DATA OUT Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

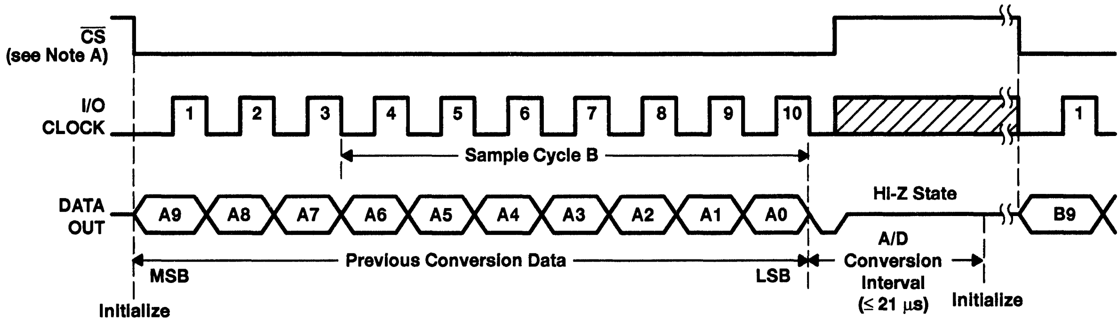


Figure 6. Timing for 10-Clock Transfer Using $\overline{CS}$

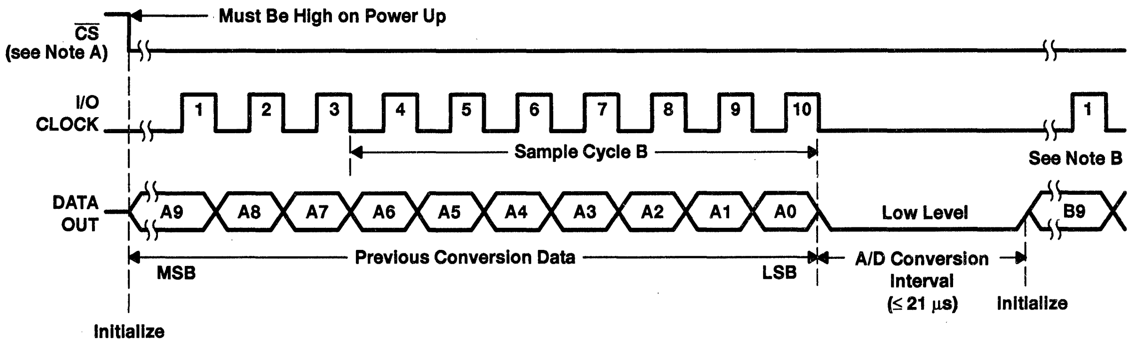


Figure 7. Timing for 10-Clock Transfer Not Using $\overline{CS}$

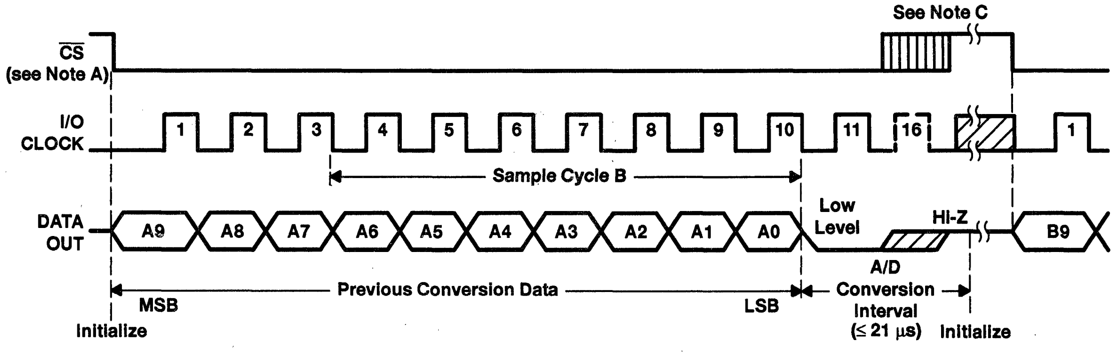


Figure 8. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$ (Serial Transfer Completed Within 21 µs)

NOTES: A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}$↓ before responding to the I/O CLOCK. No attempt should be made to clock out the data until the minimum $\overline{CS}$ setup time has elapsed.

B. A low-to-high transition of $\overline{CS}$ disables I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.

C. The first I/O CLOCK must occur after the end of the previous conversion.

PARAMETER MEASUREMENT INFORMATION

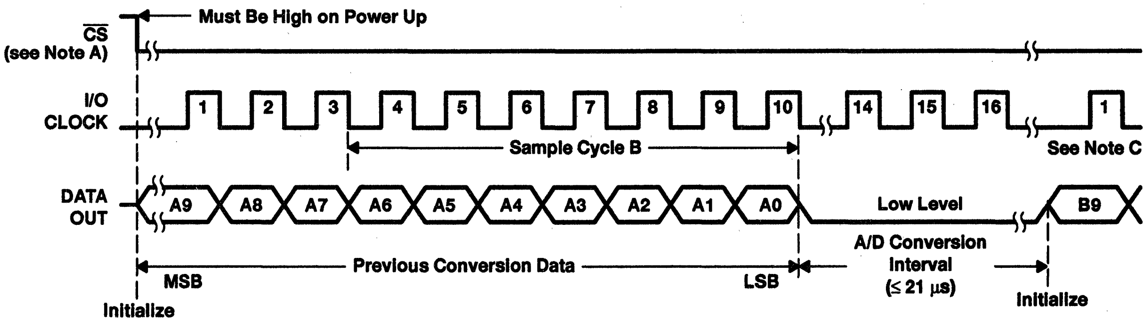


Figure 9. Timing for 16-Clock Transfer Not Using $\overline{CS}$ (Serial Transfer Completed Within 21 µs)

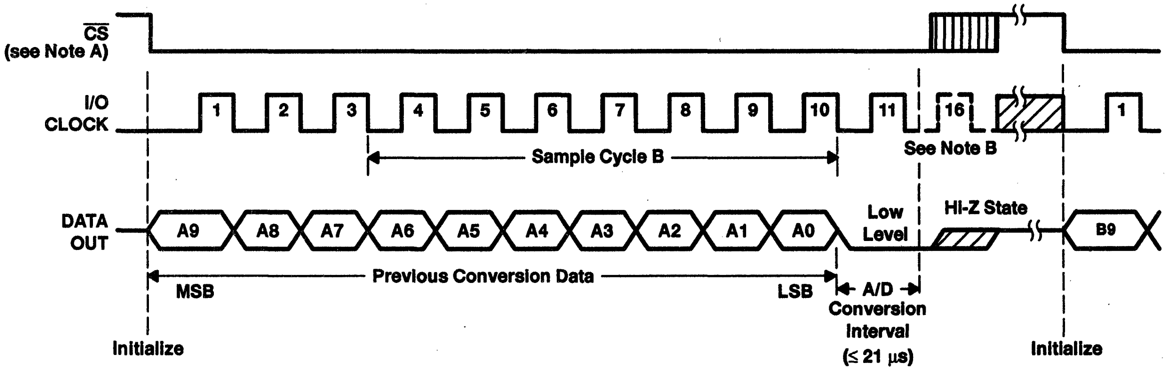


Figure 10. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$ (Serial Transfer Completed After 21 µs)

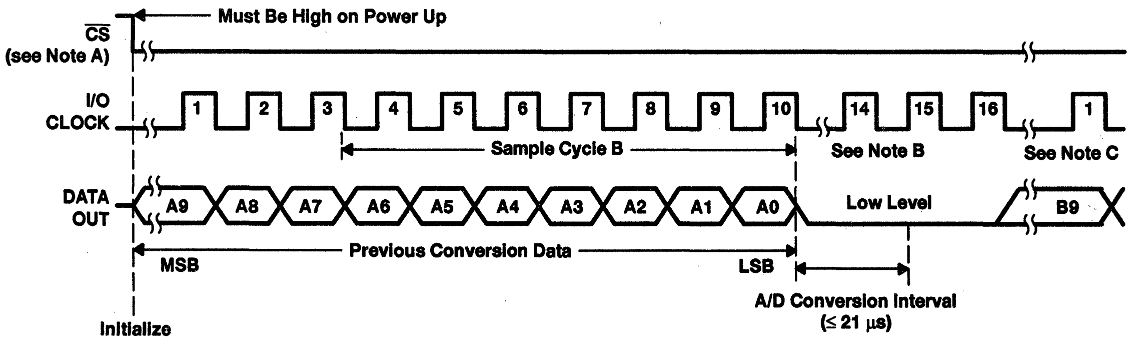


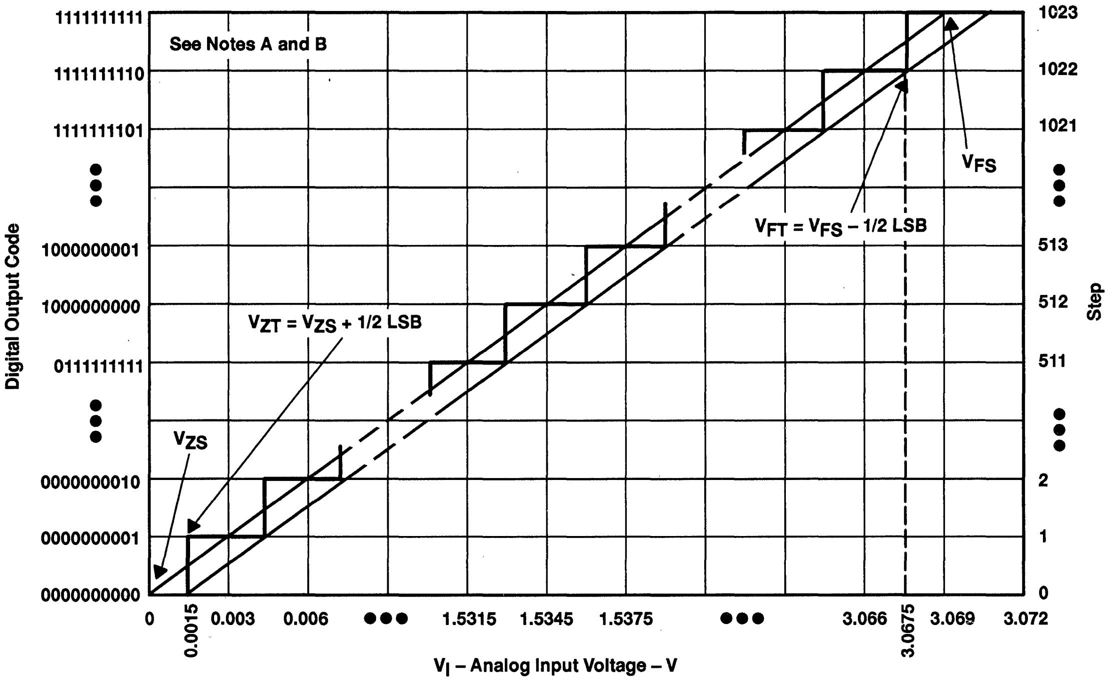
Figure 11. Timing for 16-Clock Transfer Not Using $\overline{CS}$ (Serial Transfer Completed After 21 µs)

NOTES: A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a set up time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to the I/O CLOCK. No attempt should be made to clock out the data until the minimum $\overline{CS}$ setup time has elapsed.

B. A low-to-high transition of $\overline{CS}$ disables I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.

C. The first I/O CLOCK must occur after the end of the previous conversion.

APPLICATION INFORMATION



NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0015 V and the transition to full scale (V_{FT}) is 3.0675 V. 1 LSB = 3 mV.

B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 12. Ideal Conversion Characteristics

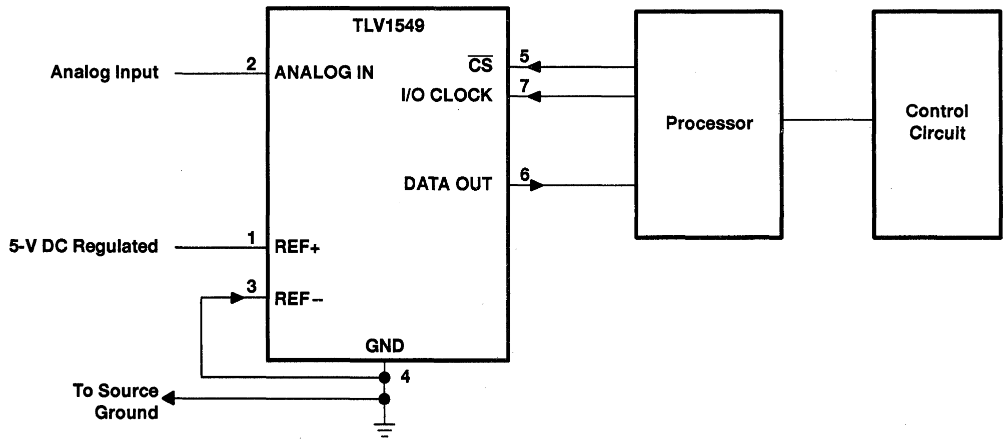


Figure 13. Typical Serial Interface

APPLICATION INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 14, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S\left(1-e^{-t_c/R_tC_i}\right) \tag{1}$$

where

$R_t = R_s + r_i$

The final voltage to 1/2 LSB is given by

$$V_C\ (1/2\ \text{LSB}) = V_S - (V_S/2048) \tag{2}$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - \left(V_S/2048\right) = V_S\left(1-e^{-t_c/R_tC_i}\right) \tag{3}$$

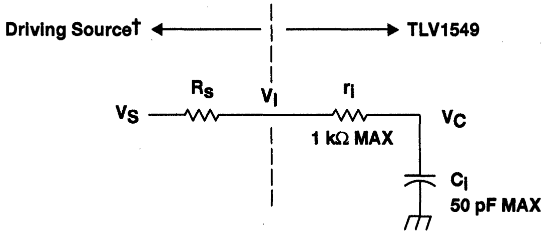
and

$$t_c\ (1/2\ \text{LSB}) = R_t \times C_i \times \ln(2048) \tag{4}$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c\ (1/2\ \text{LSB}) = (R_s + 1\ \text{k}\Omega) \times 60\ \text{pF} \times \ln(2048) \tag{5}$$

This time must be less than the converter sample time shown in the timing diagrams.



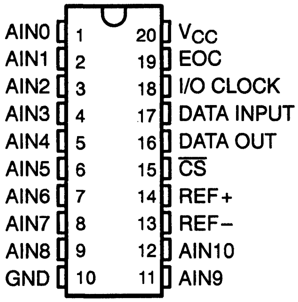
V_I = Input Voltage at ANALOG IN
V_S = External Driving Source Voltage
R_s = Source Resistance
r_i = Input Resistance
C_i = Equivalent Input Capacitance

† Driving source requirements:
- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_s must be real at the input frequency.

Figure 14. Equivalent Input Circuit Including the Driving Source

- **12-Bit-Resolution A/D Converter**
- **10-μs Conversion Time Over Operating Temperature**
- **11 Analog Input Channels**
- **3 Built-In Self-Test Modes**
- **Inherent Sample and Hold**
- **Linearity Error . . . ±1 LSB Max**
- **On-Chip System Clock**
- **End-of-Conversion (EOC) Output**
- **Unipolar or Bipolar Output Operation (Signed Binary With Respect 1/2 the Applied Referenced Voltage)**
- **Programmable MSB or LSB First**
- **Programmable Power Down**
- **Programmable Output Data Length**
- **CMOS Technology**

**DB, DW, OR N PACKAGE
(TOP VIEW)**



PRODUCT PREVIEW

description

The TLV2543C and TLV2543I are 12-bit, switched-capacitor, successive-approximation, analog-to-digital converters (ADCs). Each device has three control inputs [chip select ($\overline{CS}$), the input-output clock (I/O CLOCK), and the address input (DATA INPUT)] and is designed for communication with the serial port of a host processor or peripheral through a serial 3-state output. The device allows high-speed data transfers from the host.

In addition to the high-speed converter and versatile control capability, the device has an on-chip 14-channel multiplexer that can select any one of 11 inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of conversion, the end-of-conversion (EOC) output goes high to indicate that conversion is complete. The converter incorporated in the device features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating temperature range.

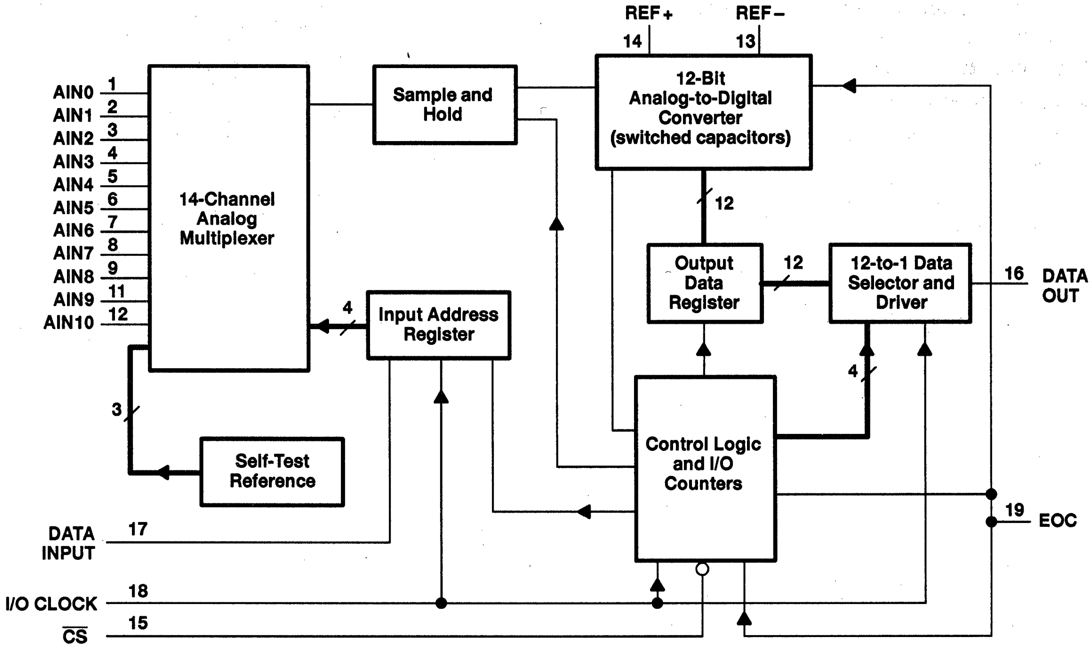
The TLV2543 is available in the DW, FN, and N packages. The TLV2543C is characterized for operation from 0°C to 70°C, and the TLV2543I is characterized for operation from −40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGE		
	SMALL OUTLINE		PLASTIC DIP
	DW	DB†	N
0°C to 70°C	TLV2543CDW	TLV2543CDB	TLV2543CN
−40°C to 85°C	TLV2543IDW	TLV2543IDB	TLV2543IN

† Available in tape and reel and ordered as the TLV2543CDBR or TLV2543IDBR.

functional block diagram



PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AIN0 – AIN10	1–9, 11, 12	I	These 11 analog-signal inputs are internally multiplexed. The driving source impedance should be less than or equal to 50 Ω for 4.1-MHz I/O CLOCK operation and capable of slewing the analog input voltage into a capacitance of 60 pF.
$\overline{CS}$	15	I	Chip select. A high-to-low transition on $\overline{CS}$ resets the internal counters and controls and enables DATA OUT, DATA INPUT, and I/O CLOCK. A low-to-high transition disables DATA INPUT and I/O CLOCK within a setup time.
DATA INPUT	17	I	Serial-data input. A 4-bit serial address selects the desired analog input or test voltage to be converted next. The serial data is presented with the MSB first and is shifted in on the first four rising edges of I/O CLOCK. After the four address bits are read into the address register, I/O CLOCK clocks the remaining bits in order.
DATA OUT	16	O	The 3-state serial output for the A/D conversion result. DATA OUT is in the high-impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low. With a valid $\overline{CS}$, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB/LSB value of the previous conversion result. The next falling edge of I/O CLOCK drives DATA OUT to the logic level corresponding to the next MSB/LSB, and the remaining bits are shifted out in order.
EOC	19	O	End of conversion goes from a high to a low logic level after the falling edge of the last I/O CLOCK and remains low until the conversion is complete and data are ready for transfer.
GND	10		The ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
I/O CLOCK	18	I	Input/output clock. I/O CLOCK receives the serial input and performs the following four functions: 1. It clocks the eight input data bits into the input data register on the first eight rising edges of I/O CLOCK with the multiplexer address available after the fourth rising edge. 2. On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplexer input begins charging the capacitor array and continues to do so until the last falling edge of I/O CLOCK. 3. It shifts the 11 remaining bits of the previous conversion data out on DATA OUT. Data changes on the falling edge of I/O CLOCK. 4. It transfers control of the conversion to the internal state controller on the falling edge of the last I/O CLOCK.
REF+	14	I	The upper reference voltage value (nominally V_{CC}) is applied to REF+. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to the REF– terminal.
REF–	13	I	The lower reference voltage value (nominally ground) is applied to REF–.
V_{CC}	20		Positive supply voltage

PRODUCT PREVIEW

detailed description

Initially, with chip select ($\overline{CS}$) high, I/O CLOCK and DATA INPUT are disabled and DATA OUT is in the high-impedance state. $\overline{CS}$, going low, begins the conversion sequence by enabling I/O CLOCK and DATA INPUT and removes DATA OUT from the high-impedance state.

The input data is an 8-bit data stream consisting of a 4-bit analog channel address (D7–D4), a 2-bit data length select (D3–D2), an output MSB or LSB first bit (D1), and a unipolar or bipolar output select bit (D0) that are applied to DATA INPUT. The I/O CLOCK sequence applied to the I/O CLOCK terminal transfers this data to the input data register.

During this transfer, the I/O CLOCK sequence also shifts the previous conversion result from the output data register to DATA OUT. I/O CLOCK receives the input sequence of 8, 12, or 16 clocks long depending on the data-length selection in the input data register. Sampling of the analog input begins on the fourth falling edge of the input I/O CLOCK sequence and is held after the last falling edge of the I/O CLOCK sequence. The last falling edge of the I/O CLOCK sequence also takes EOC low and begins the conversion.

converter operation

The operation of the converter is organized as a succession of two distinct cycles: 1) the I/O cycle and 2) the actual conversion cycle. The I/O cycle is defined by the externally provided I/O CLOCK and lasts 8, 12, or 16 clock periods, depending on the selected output data length.

1. I/O cycle

   During the I/O cycle, two operations take place simultaneously.

   a. An 8-bit data stream consisting of address and control information is provided to DATA INPUT. This data is shifted into the device on the rising edge of the first eight I/O CLOCKs. DATA INPUT is ignored after the first eight clocks during 12 or 16 clock I/O transfers.

   b. The data output, with a length of 8, 12, or 16 bits, is provided serially on DATA OUT. If $\overline{CS}$ is held low, the first output data bit occurs on the rising edge of EOC. If $\overline{CS}$ is negated between conversions, the first output data bit occurs on the falling edge of $\overline{CS}$. This data is the result of the previous conversion period, and after the first output data bit, each succeeding bit is clocked out on the falling edge of each succeeding I/O CLOCK.

2. Conversion cycle

   The conversion cycle is transparent to the user, and it is controlled by an internal clock synchronized to I/O CLOCK. During the conversion period, the device performs a successive-approximation conversion on the analog input voltage. The EOC output goes low at the start of the conversion cycle and goes high when conversion is complete and the output data register is latched. A conversion cycle is started only after the I/O cycle is completed, which minimizes the influence of external digital noise on the accuracy of the conversion.

PRODUCT PREVIEW

power up and initialization

After power up, $\overline{CS}$ must be taken from high to low to begin an I/O cycle. EOC is initially high, and the input data register is set to all zeroes. The contents of the output data register are random, and the first conversion result should be ignored. To initialize during operation, $\overline{CS}$ is taken high and returned low to begin the next I/O cycle. The first conversion after the device has returned from the power-down state may not read accurately due to internal device settling.

operational terminology

Current (N) I/O cycle	The entire I/O CLOCK sequence that transfers address and control data into the data register and clocks the digital result from the previous conversion from DATA OUT
Current (N) conversion cycle	The conversion cycle starts immediately after the current I/O cycle. The end of the current I/O cycle is the last clock falling edge in the I/O CLOCK sequence. The current conversion result is loaded into the output register when conversion is complete.
Current (N) conversion result	The current conversion result is serially shifted out on the next I/O cycle.
Previous (N−1) conversion cycle	The conversion cycle just prior to the current I/O cycle
Next (N+1) I/O cycle	The I/O period that follows the current conversion cycle

Example: In the 12-bit mode, the result of the current conversion cycle is a 12-bit serial-data stream clocked out during the next I/O cycle. The current I/O cycle must be exactly 12 bits long to maintain synchronization, even if this corrupts the output data from the previous conversion. The current conversion begins immediately after the twelfth falling edge of the current I/O cycle.

data input

The data input is internally connected to an 8-bit serial-input address and control register. The register defines the operation of the converter and the output data length. The host provides the data word with the MSB first. Each data bit is clocked in on the rising edge of the I/O CLOCK sequence (see Table 1 for the data register format).

data input address bits

The four MSBs (D7 – D4) of the data register are used to address one of the 11 input channels, a reference-test voltage, or the power-down mode. The address bits affect the current conversion, which is the conversion that immediately follows the current I/O cycle. The reference voltage is nominally equal to $V_{ref+} - V_{ref-}$.

data output length

The next two bits (D3 and D2) of the data register select the output data length. The data-length selection is valid for the current I/O cycle (the cycle in which the data is read). The data-length selection, being valid for the current I/O cycle, allows device start up without losing I/O synchronization. A data length of 8, 12, or 16 bits can be selected. Since the converter has 12-bit resolution, a data length of 12 bits is suggested.

With D3 and D2 set to 00 or 10, the device is in the 12-bit data-length mode and the result of the current conversion is output as a 12-bit serial-data stream during the next I/O cycle. The current I/O cycle must be exactly 12 bits long for proper synchronization, even if this means corrupting the output data from a previous conversion. The current conversion is started immediately after the twelfth falling edge of the current I/O cycle.

With bits D3 and D2 set to 11, the 16-bit data-length mode is selected, which allows convenient communication with 16-bit serial interfaces. In the 16-bit mode, the result of the current conversion is output as a 16-bit serial-data stream during the next I/O cycle with the four LSBs always set to 0 (pad bits). The current I/O cycle must be exactly 16 bits long to maintain synchronization even if this means corrupting the output data from the previous conversion. The current conversion is immediately started after the 16th falling edge of the current I/O cycle.

With bits D3 and D2 set to 01, the 8-bit data-length mode is selected, which allows fast communication with 8-bit serial interfaces. In the 8-bit mode, the result of the current conversion is output as an 8-bit serial-data stream during the next I/O cycle. The current I/O cycle must be exactly 8 bits long to maintain synchronization, even if this means corrupting the output data from the previous conversion. The four LSBs of the conversion result are truncated and discarded. The current conversion is immediately started after the eighth falling edge of the current I/O cycle.

Since D3 and D2 take effect on the current I/O cycle when the data length is programmed, there can be a conflict with the previous cycle when the data-word length is changed from one cycle to the next. This may occur when the data format is selected to be least significant bit first, since at the time the data length change becomes effective (6 rising edges of I/O CLOCK), the previous conversion result has already started shifting out.

In actual operation, if different data lengths are required within an application and the data length is changed between two conversions, no more than one conversion result can be corrupted and only if it is shifted out in LSB first format.

sampling period

During the sampling period, one of the analog inputs is internally connected to the capacitor array of the converter to store the analog input signal. The converter starts sampling the selected input immediately after the four address bits have been clocked into the input data register. Sampling starts on the fourth falling edge of I/O CLOCK. The converter remains in the sampling mode until the eighth, twelfth, or sixteenth falling edge of the I/O CLOCK depending on the data-length selection. After the EOC delay time from the last I/O CLOCK falling edge, the EOC output goes low indicating that the sampling period is over and the conversion period has begun. After EOC goes low, the analog input can be changed without affecting the conversion result. Since the delay from the falling edge of the last I/O CLOCK to EOC low is fixed, time-varying analog input signals can be digitized at a fixed rate without introducing systematic harmonic distortion or noise due to timing uncertainty.

After the 8-bit data stream has been clocked in, DATA INPUT should be held at a fixed digital level until EOC goes high (indicating the conversion is complete) to maximize the sampling accuracy and minimize the influence of external digital noise.

data register, LSB first

D1 in the input data register (LSB first) is used to control the direction of the output binary data transfer. When D1 is set to 0, the conversion result is shifted out MSB first. When set to 1, the data is shifted out LSB first. Selection of MSB first or LSB first always affects the next I/O cycle and not the current I/O cycle. When changing from one data direction to another, the current I/O cycle is never disrupted.

data register, bipolar format

D0 in the input data register is used to control the binary data format used to represent the conversion result. When D0 is set to 0, the conversion result is represented as unipolar (unsigned binary) data. Nominally, the conversion result of an input voltage equal to V_{ref-} is a code of all zeros (000 . . . 0), the conversion result of an input voltage equal to V_{ref+} is a code of all ones (111 . . . 1), and the conversion result of $(V_{ref+} + V_{ref-})/2$ is a code of a one followed by zeros (100 . . . 0).

When D0 is set to 1, the conversion result is represented as bipolar (BIP) (signed binary) data. Nominally, conversion of an input voltage equal to V_{ref-} is a code of a 1 followed by zeros (100 . . . 0), conversion of an input voltage equal to V_{ref+} is a code of a 0 followed by all ones (011 . . . 1), and the conversion of $(V_{ref+} + V_{ref-})/2$ is a code of all zeros (000 . . . 0). The MSB is interpreted as the sign bit. The bipolar data format is related to the unipolar format in that the MSBs are always each other's complement.

Selection of the unipolar or bipolar format always affects the current conversion cycle, and the result is output during the next I/O cycle. When changing between unipolar and bipolar formats, the data output during the current I/O cycle is not affected.

EOC output

The EOC signal indicates the beginning and the end of conversion. In the reset state, EOC is always high. During the sampling period (beginning after the fourth falling edge of the I/O CLOCK sequence), EOC remains high until the internal sampling switch of the converter is safely opened. The opening of the sampling switch occurs after the eighth, twelfth, or sixteenth I/O CLOCK falling edge, depending on the data-length selection in the input data register. After the EOC signal goes low, the analog input signal can be changed without affecting the conversion result.

The EOC signal goes high again after the conversion is completed and the conversion result is latched into the output data register. The rising edge of EOC returns the converter to a reset state and a new I/O cycle begins. On the rising edge of EOC, the first bit of the current conversion result is on DATA OUT if $\overline{CS}$ is low. If $\overline{CS}$ is negated between conversions, the first bit of the current conversion result occurs at DATA OUT on the falling edge of $\overline{CS}$.

data format and pad bits

D3 and D2 of the input data register determine the number of significant bits in the digital output that represent the conversion result. The LSB-first bit determines the direction of the data transfer while the BIP bit determines the arithmetic conversion. The numerical data is always justified toward the MSB in any output format.

The internal conversion result is always 12 bits long. When an 8-bit data transfer is selected, the four LSBs of the internal result are discarded to provide a faster one-byte transfer. When a 12-bit transfer is used, all bits are transferred. When a 16-bit transfer is used, four LSB pad bits are always appended to the internal conversion result. In the LSB-first mode, four leading zeros are output. In the MSB-first mode, the last four bits output are zeros.

When $\overline{CS}$ is held low continuously, the first data bit of the just completed conversion occurs on DATA OUT on the rising edge of EOC. When a new conversion is started after the last falling edge of I/O CLOCK, EOC goes low and the serial output is forced to a logic zero until EOC goes high again.

When $\overline{CS}$ is negated between conversions, the first data bit occurs on DATA OUT on the falling edge of $\overline{CS}$. On each subsequent falling edge of I/O CLOCK after the first data bit appears, the data is changed to the next bit in the serial conversion result until the required number of bits has been output.

chip-select input ($\overline{CS}$)

The chip-select input ($\overline{CS}$) enables and disables the device. During normal operation, $\overline{CS}$ should be low. Although the use of $\overline{CS}$ is not necessary to synchronize a data transfer, it can be brought high between conversions to coordinate the data transfer of several devices sharing the same bus.

When $\overline{CS}$ is brought high, the serial-data output is immediately brought to the high-impedance state, releasing its output data line to other devices that may share it. After an internally generated debounce time, the I/O CLOCK is inhibited, thus preventing any further change in the internal state.

When $\overline{CS}$ is subsequently brought low again, the device is reset. $\overline{CS}$ must be held low for an internal debounce time before the reset operation takes effect. After $\overline{CS}$ is debounced low, I/O CLOCK must remain inactive (low) for a minimum time before a new I/O cycle can start.

$\overline{CS}$ can be used to interrupt any ongoing data transfer or any ongoing conversion. If $\overline{CS}$ is debounced low long enough before the end of the current conversion cycle, the previous conversion result is saved in the internal output buffer and shifted out during the next I/O cycle.

power-down features

When a binary address of 1110 is clocked into the input data register during the first four I/O CLOCK cycles, the power-down mode is selected. Power down is activated on the falling edge of the fourth I/O CLOCK pulse.

During power down, all internal circuitry is put in a low-current standby mode. No conversions are performed, and the internal output buffer keeps the previous conversion cycle data results, provided that all digital inputs are held above V_{CC} – 0.5 V or below 0.5 V. The I/O logic remains active so the current I/O cycle must be completed even when the power-down mode is selected. Upon power-on reset and before the first I/O cycle, the converter normally begins in the power-down mode. The device remains in the power-down mode until a valid (other than 1110) input address is clocked in. Upon completion of that I/O cycle, a normal conversion is performed with the results being shifted out during the next I/O cycle.

analog input, test, and power-down mode

The 11 analog inputs, three internal voltages, and power-down mode are selected by the input multiplexer according to the input addresses shown in Tables 2, 3, and 4. The input multiplexer is a break-before-make type to reduce input-to-input noise rejection resulting from channel switching. Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK and continues for the remaining I/O CLOCK pulses. The sample is held on the falling edge of the last I/O CLOCK pulse. The three internal test inputs are applied to the multiplexer, sampled, and converted in the same manner as the external analog inputs. The first conversion after the device has returned from the power-down state may not read accurately due to internal device settling.

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detailed description (continued)

Table 1. Input-Register Format

FUNCTION SELECT	INPUT DATA BYTE							
	ADDRESS BITS				L1	L0	LSBF	BIP
	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
Select input channel								
AIN0	0	0	0	0				
AIN1	0	0	0	1				
AIN2	0	0	1	0				
AIN3	0	0	1	1				
AIN4	0	1	0	0				
AIN5	0	1	0	1				
AIN6	0	1	1	0				
AIN7	0	1	1	1				
AIN8	1	0	0	0				
AIN9	1	0	0	1				
AIN10	1	0	1	0				
Select test voltage								
$(V_{ref+} - V_{ref-})/2$	1	0	1	1				
V_{ref-}	1	1	0	0				
V_{ref+}	1	1	0	1				
Software power down	1	1	1	0				
Output data length								
8 bits					0	1		
12 bits					X	0		
16 bits					1	1		
Output data format								
MSB first							0	
LSB first							1	
Unipolar (binary)								0
Bipolar (2s complement)								1

Table 2. Analog-Channel-Select Address

ANALOG INPUT SELECTED	VALUE SHIFTED INTO DATA INPUT	
	BINARY	HEX
AIN0	0000	0
AIN1	0001	1
AIN2	0010	2
AIN3	0011	3
AIN4	0100	4
AIN5	0101	5
AIN6	0110	6
AIN7	0111	7
AIN8	1000	8
AIN9	1001	9
AIN10	1010	A

detailed description (continued)

Table 3. Test-Mode-Select Address

INTERNAL SELF-TEST VOLTAGE SELECTED†	VALUE SHIFTED INTO DATA INPUT		UNIPOLAR OUTPUT RESULT (HEX)‡
	BINARY	HEX	
$\frac{V_{ref+} - V_{ref-}}{2}$	1011	B	200
V_{ref-}	1100	C	000
V_{ref+}	1101	D	3FF

† V_{ref+} is the voltage applied to REF+, and V_{ref-} is the voltage applied to REF−.
‡ The output results shown are the ideal values and may vary with the reference stability and with internal offsets.

Table 4. Power-Down-Select Address

INPUT COMMAND	VALUE SHIFTED INTO DATA INPUT		RESULT
	BINARY	HEX	
Power down	1110	E	$I_{CC} \leq 25\ \mu A$

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF−) voltage. In the switching sequence, 12 capacitors are examined separately until all 12 bits are identified and the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 4096). Node 4096 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF−. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half V_{CC}), a bit 0 is placed in the output register and the 4096-weight capacitor is switched to REF−. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and this 4096-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 2048-weight capacitor, the 1024-weight capacitor, and so forth, down the line until all bits are determined. With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to determine the bits from MSB to LSB.

reference voltage inputs

There are two reference voltage inputs on the device: REF+ and REF−. The voltage values on these terminals establish the upper and lower limits of the analog input to produce a full-scale and zero-scale reading respectively. These voltages and the analog input should not exceed the positive supply or be lower than ground consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ terminal voltage and at zero when the input signal is equal to or lower than REF− terminal voltage.

detailed description (continued)

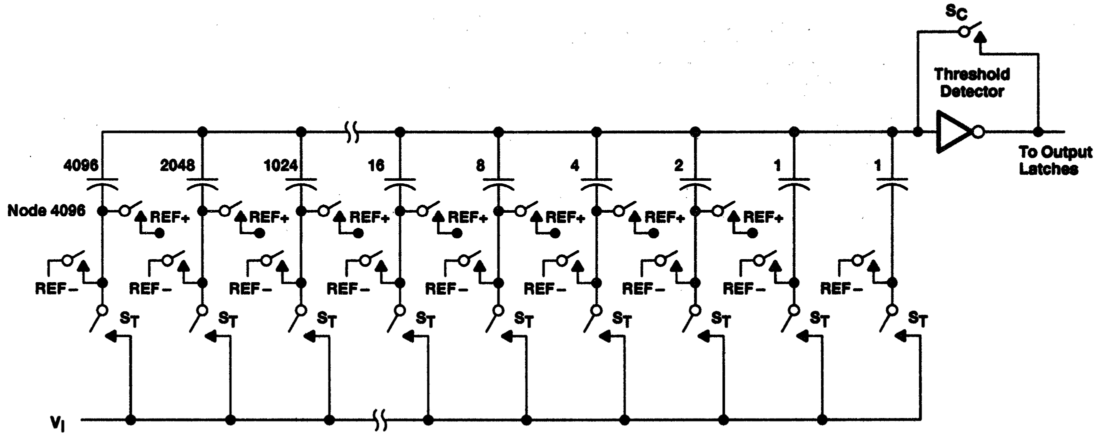

Figure 1. Simplified Model of the Successive-Approximation System

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) .... −0.5 V to 6.5 V
Input voltage range, V_I (any input) .... −0.3 V to V_{CC} + 0.3 V
Output voltage range, V_O .... −0.3 V to V_{CC} + 0.3 V
Positive reference voltage, V_{ref+} .... V_{CC} + 0.1 V
Negative reference voltage, V_{ref-} .... −0.1 V
Peak input current, I_I (any input) .... ±20 mA
Peak total input current (all inputs) .... ±30 mA
Operating free-air temperature range, T_A: TLV2543C .... 0°C to 70°C
TLV2543I .... −40°C to 85°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminal with REF− and GND wired together (unless otherwise noted).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
Positive reference voltage, V_{ref+} (see Note 2)			V_{CC}		V
Negative reference voltage, V_{ref-} (see Note 2)			0		V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)		2.5	V_{CC}	V_{CC}+0.1	V
Analog input voltage (see Note 2)		0		V_{CC}	V
High-level control input voltage, V_{IH}	V_{CC} = 3 V to 3.6 V	2			V
Low-level control input voltage, V_{IL}	V_{CC} = 3 V to 3.6 V			0.8	V
Clock frequency at I/O CLOCK		0	3		MHz
Setup time, address bits at DATA INPUT before I/O CLOCK↑, $t_{su(A)}$ (see Figure 5)		100			ns
Hold time, address bits after I/O CLOCK↑, $t_{h(A)}$ (see Figure 5)		0			ns
Hold time, $\overline{CS}$ low after last I/O CLOCK↓, $t_{h(CS)}$ (see Figure 6)		0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3 and Figure 6)		1.425			µs
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$		190			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$		190			ns
Transition time, I/O CLOCK, $t_{t(I/O)}$ (see Note 4 and Figure 7)				1	µs
Transition time, DATA INPUT and $\overline{CS}$, $t_{t(CS)}$				10	µs
Operating free-air temperature, T_A	TLV2543C	0		70	°C
	TLV2543I	−40		85	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (111111111111), while input voltages less than that applied to REF− convert as all zeros (000000000000).

3. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for a setup time after $\overline{CS}$↓ before responding to control input signals. No attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IH}min to V_{IL}max or to rise from V_{IL}max to V_{IH}min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

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electrical characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 3 V to 3.6 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 3 V,	I_{OH} = –0.3 mA	2.4			V
			V_{CC} = 3 V to 3.6 V,	I_{OH} = –20 µA	V_{CC}–0.1			
V_{OL}	Low-level output voltage		V_{CC} = 3 V,	I_{OL} = 0.8 mA			0.4	V
			V_{CC} = 3 V to 3.6 V,	I_{OL} = 20 µA			0.1	
I_{OZ}	Off-state (high-impedance-state) output current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}		1	2.5	µA
			V_O = 0,	$\overline{CS}$ at V_{CC}		1	–2.5	
I_{IH}	High-level input current		$V_I = V_{CC}$			1	2.5	µA
I_{IL}	Low-level input current		V_I = 0			1	–2.5	µA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1	2.5	mA
$I_{CC(PD)}$	Power-down current		For all digital inputs, $0 \le V_I \le 0.5$ V or $V_I \ge V_{CC} - 0.5$ V			4	25	µA
	Selected channel leakage current		Selected channel at V_{CC},	Unselected channel at 0 V			1	µA
			Selected channel at 0 V,	Unselected channel at V_{CC}			–1	
	Maximum static analog reference current into REF+		$V_{ref+} = V_{CC}$,	V_{ref-} = GND		1	2.5	µA
C_i	Input capacitance	Analog inputs				30	60	pF
		Control inputs				5	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

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operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 3 V to 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error (see Note 6)	See Figure 2			±1	LSB
E_D	Differential linearity error	See Figure 2			±1	LSB
E_O	Offset error (see Note 7)	See Note 2 and Figure 2			±1.5	LSB
E_G	Gain error (see Note 7)	See Note 2 and Figure 2			±1	LSB
E_T	Total unadjusted error (see Note 8)				±1.75	LSB
	Self-test output code (see Table 3 and Note 9)	DATA INPUT = 1011		2048		
		DATA INPUT = 1100		0		
		DATA INPUT = 1101		4095		
t_{conv}	Conversion time	See Figures 10–15		8		µs
t_c	Total cycle time (access, sample, and conversion)	See Figures 10–15 and Note 10			10 + total I/O CLOCK periods + $t_{d(I/O-EOC)}$	µs
t_{acq}	Channel acquisition time (sample)	See Figures 10–15 and Note 10	4		12	I/O CLOCK periods
t_v	Valid time, DATA OUT remains valid after I/O CLOCK↓	See Figure 7	10			ns
$t_{d(I/O-DATA)}$	Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 7			150	ns
$t_{d(I/O-EOC)}$	Delay time, last I/O CLOCK↓ to EOC↓	See Figure 8		1.5	2.2	µs
$t_{d(EOC-DATA)}$	Delay time, EOC↑ to DATA OUT (MSB/LSB)	See Figure 9			100	ns
t_{PZH}, t_{PZL}	Enable time, $\overline{CS}$↓ to DATA OUT (MSB/LSB driven)	See Figure 4		0.7	1.3	µs
t_{PHZ}, t_{PLZ}	Disable time, $\overline{CS}$↑ to DATA OUT (high impedance)	See Figure 4		70	150	ns
$t_{r(EOC)}$	Rise time, EOC	See Figure 9		15	50	ns
$t_{f(EOC)}$	Fall time, EOC	See Figure 8		15	50	ns
$t_{r(bus)}$	Rise time, data bus	See Figure 7		15	50	ns
$t_{f(bus)}$	Fall time, data bus	See Figure 7		15	50	ns
$t_{d(I/O-CS)}$	Delay time, last I/O CLOCK↓ to $\overline{CS}$↓ to abort conversion (see Note 11)				5	µs

† All typical values are at T_A = 25°C.

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (111111111111), while input voltages less than that applied to REF– convert as all zeros (000000000000).
6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
7. Gain error is the difference between the actual midstep value and the nominal midstep value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. Offset error is the difference between the actual midstep value and the nominal midstep value at the offset point.
8. Total unadjusted error comprises linearity, zero-scale, and full-scale errors.
9. Both the input address and the output codes are expressed in positive logic.
10. I/O CLOCK period = 1/(I/O CLOCK frequency) (see Figure 7).
11. Any transitions of $\overline{CS}$ are recognized as valid only if the level is maintained for a setup time. $\overline{CS}$ must be taken low at ≤ 5 µs of the tenth I/O CLOCK falling edge to assure a conversion is aborted. Between 5 µs and 10 µs, the result is uncertain as to whether the conversion is aborted or the conversion results are valid.

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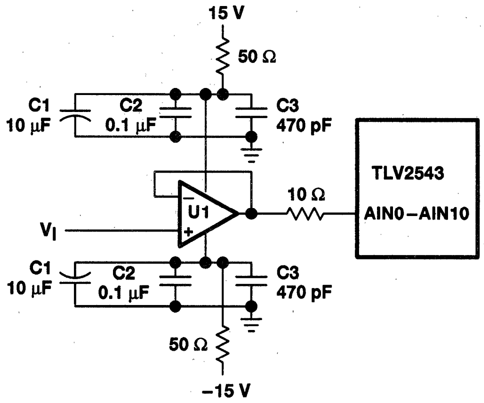
PARAMETER MEASUREMENT INFORMATION



LOCATION	DESCRIPTION	PART NUMBER
U1	OP27	—
C1	10-µF 35-V tantalum capacitor	—
C2	0.1-µF ceramic NPO SMD capacitor	AVX 12105C104KA105 or equivalent
C3	470-pF porcelain high-Q SMD capacitor	Johanson 201S420471JG4L or equivalent

Figure 2. Analog Input Buffer to Analog Inputs AIN0–AIN10

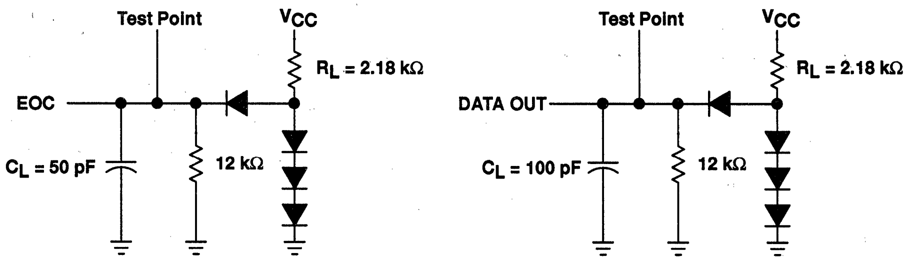


Figure 3. Load Circuits

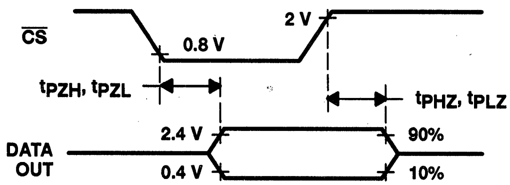


Figure 4. DATA OUT to Hi-Z Voltage Waveforms

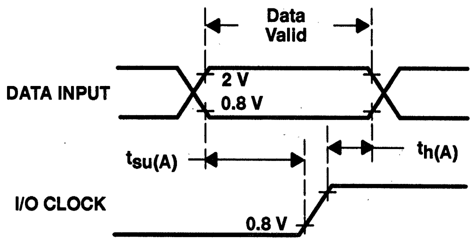


Figure 5. DATA INPUT and I/O CLOCK Voltage Waveforms

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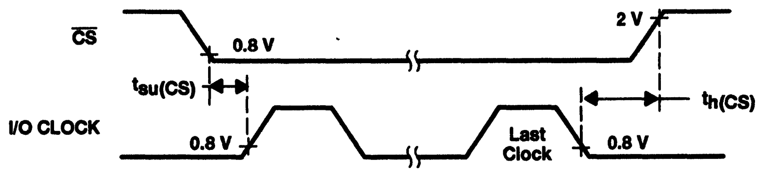

Figure 6. $\overline{CS}$ and I/O CLOCK Voltage Waveforms†

† To ensure full conversion accuracy, it is recommended that no input signal change occurs while a conversion is ongoing.

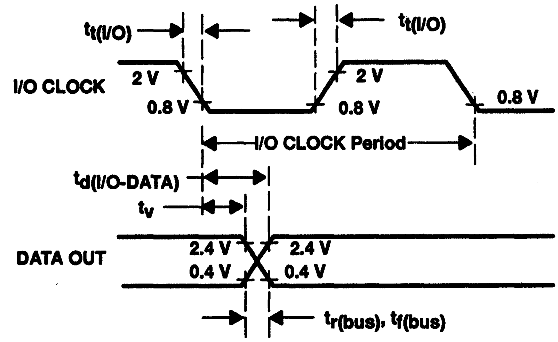

Figure 7. I/O CLOCK and DATA OUT Voltage Waveforms

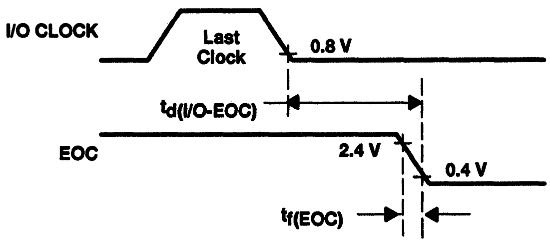

Figure 8. I/O CLOCK and EOC Voltage Waveforms

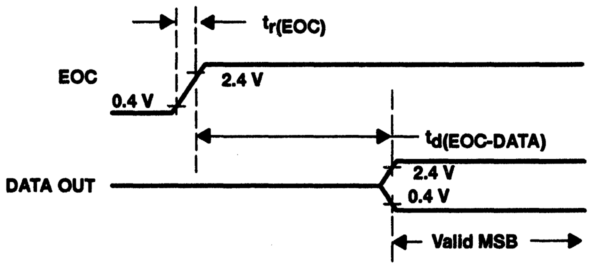

Figure 9. EOC and DATA OUT Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

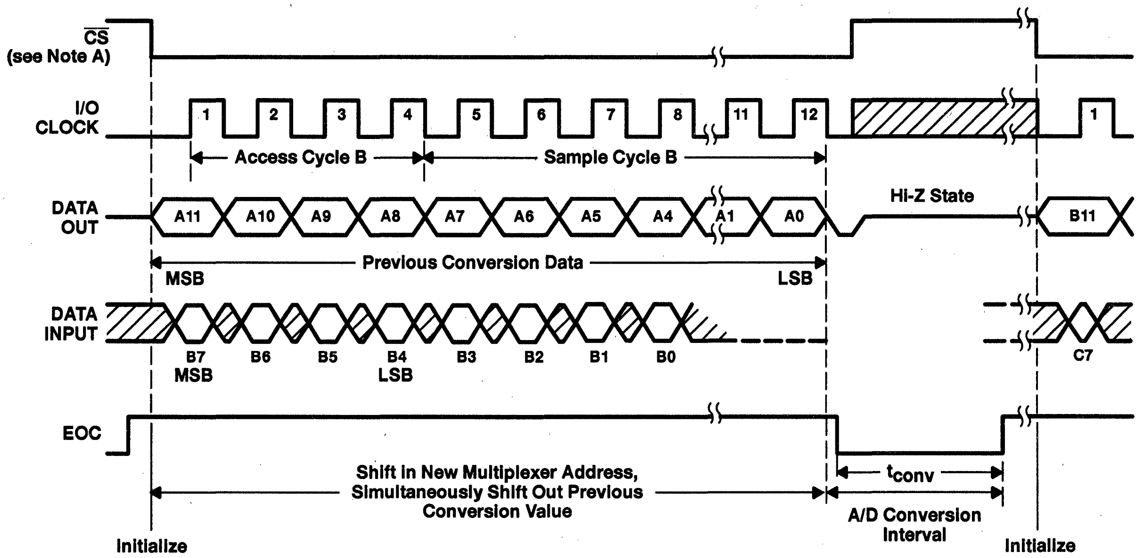

Figure 10. Timing for 12-Clock Transfer Using $\overline{CS}$ With MSB First

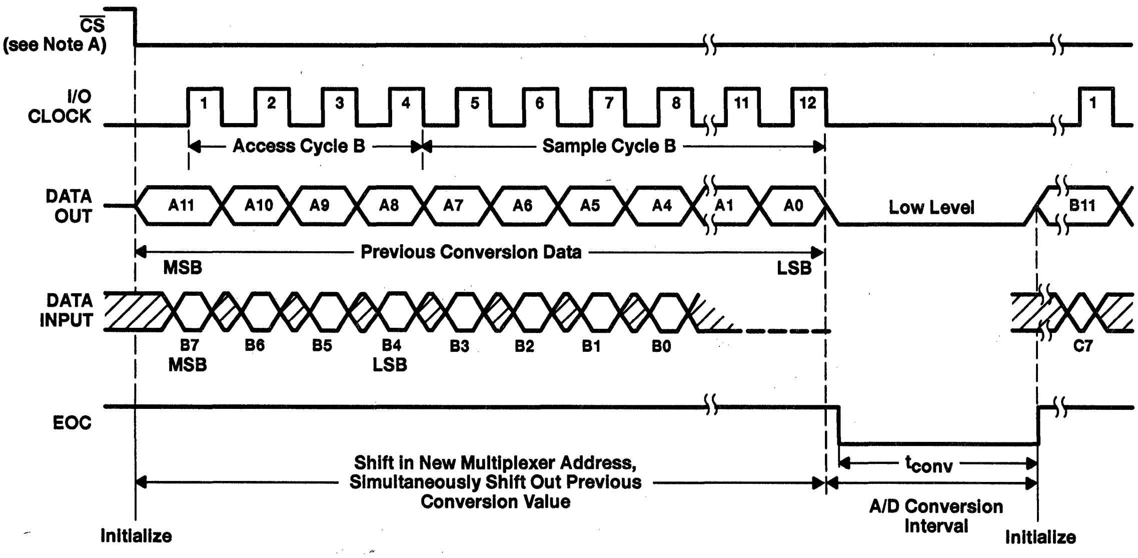

Figure 11. Timing for 12-Clock Transfer Not Using $\overline{CS}$ With MSB First

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

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PARAMETER MEASUREMENT INFORMATION

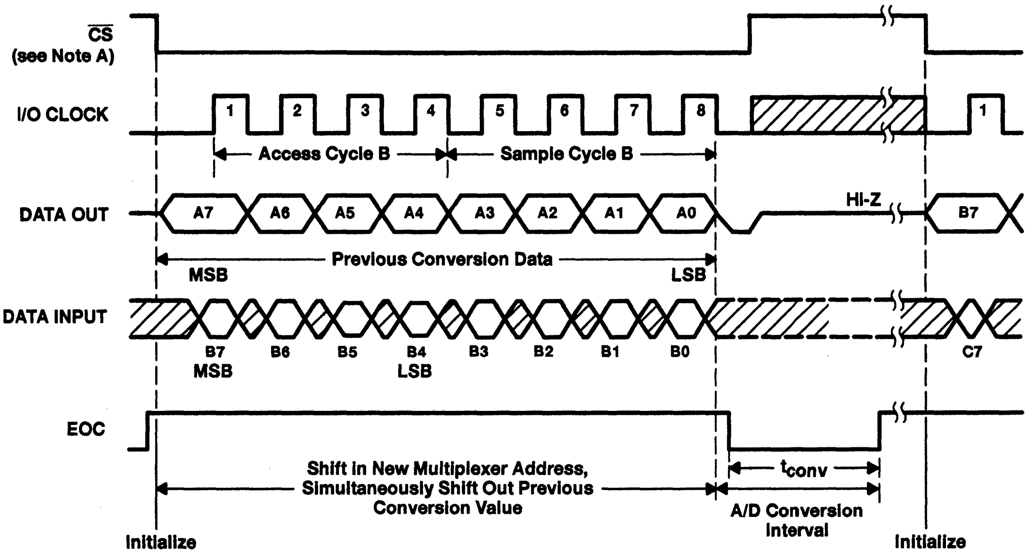

Figure 12. Timing for 8-Clock Transfer Using $\overline{CS}$ With MSB First

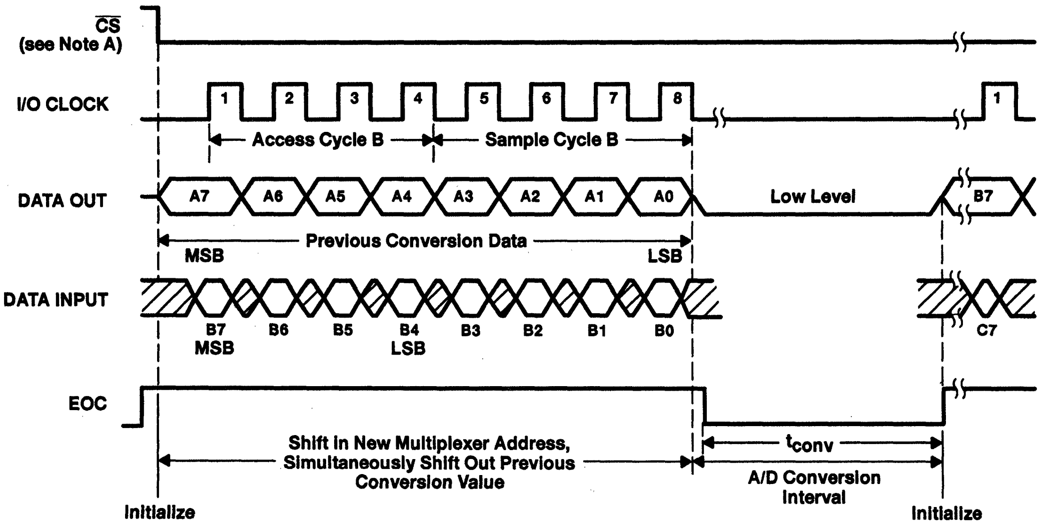

Figure 13. Timing for 8-Clock Transfer Not Using $\overline{CS}$ With MSB First

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}$↓ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

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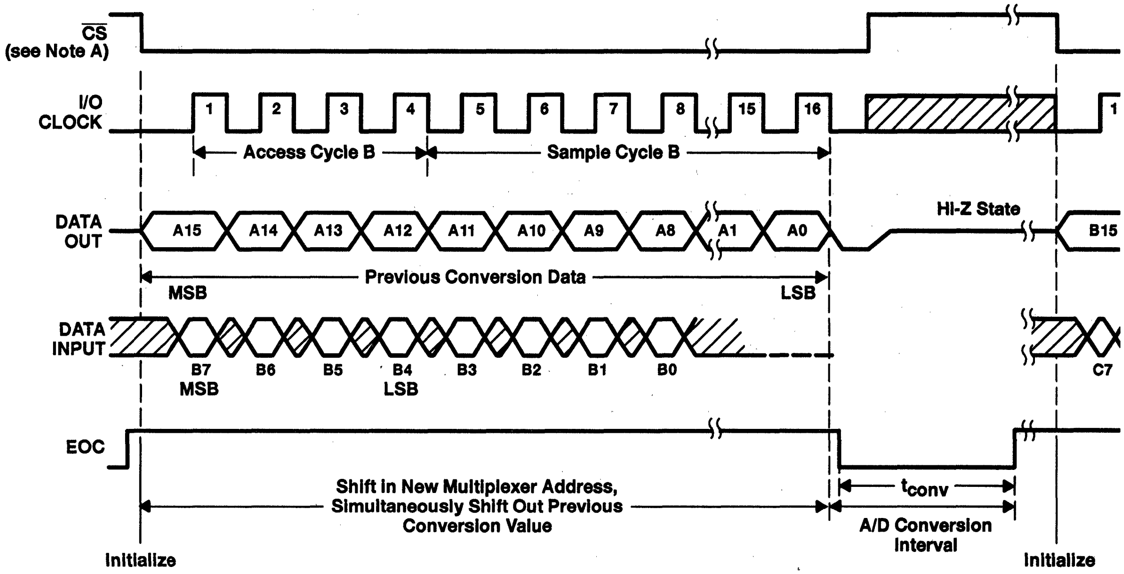


Figure 14. Timing for 16-Clock Transfer Using $\overline{CS}$ With MSB First

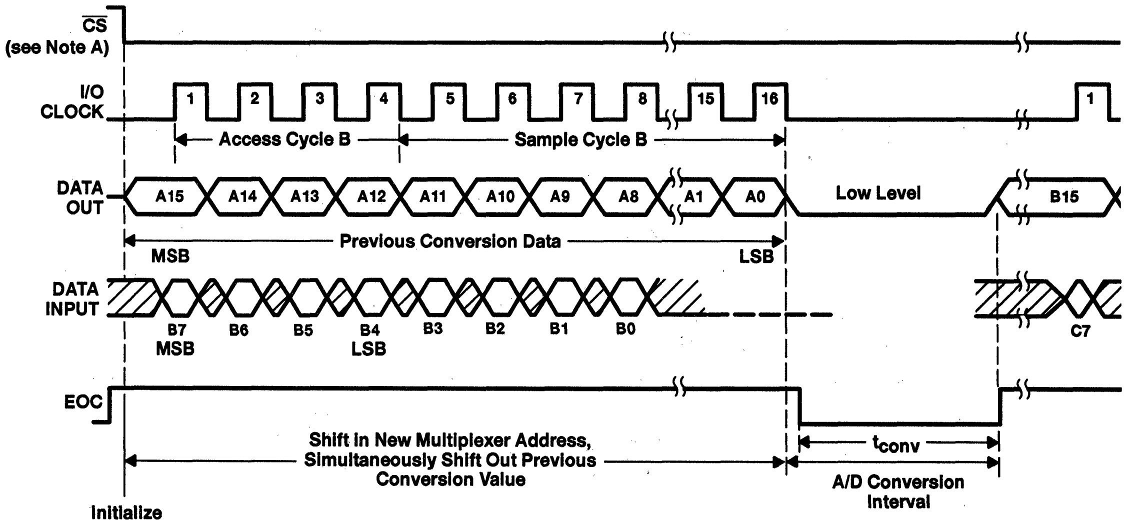
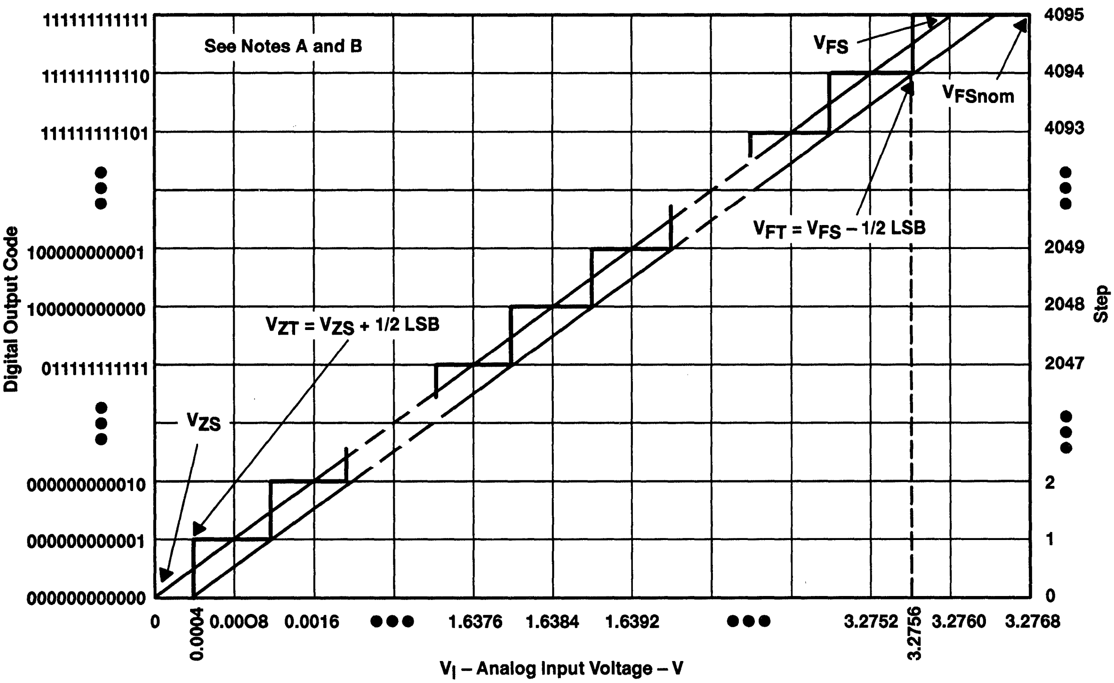


Figure 15. Timing for 16-Clock Transfer Not Using $\overline{CS}$ With MSB First

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

APPLICATION INFORMATION



NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0006 V and the transition to full scale (V_{FT}) is 4.9134 V. 1 LSB = 1.2 mV.

B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 16. Ideal Conversion Characteristics

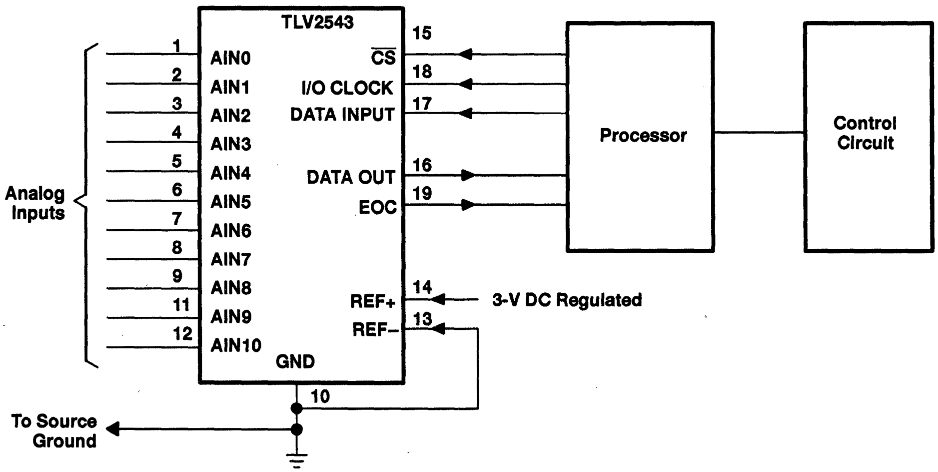


Figure 17. Serial Interface

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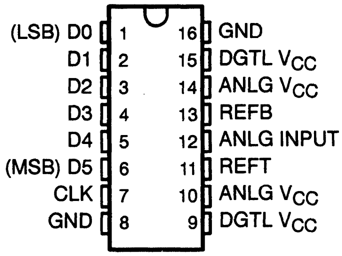
SLAS026 – D3163, OCTOBER 1989 – REVISED APRIL 1990

- 6-Bit Resolution
- Linearity Error . . . ±0.8%
- Maximum Conversion Rate . . . 30 MHz Typ
- Analog Input Voltage Range
  V_{CC} to V_{CC} –2 V
- Analog Input Dynamic Range . . . 1 V
- TTL Digital I/O Level
- Low Power Consumption
  200 mW Typ
- 5-V Single-Supply Operation
- Interchangeable With Fujitsu MB40576

N PACKAGE
(TOP VIEW)

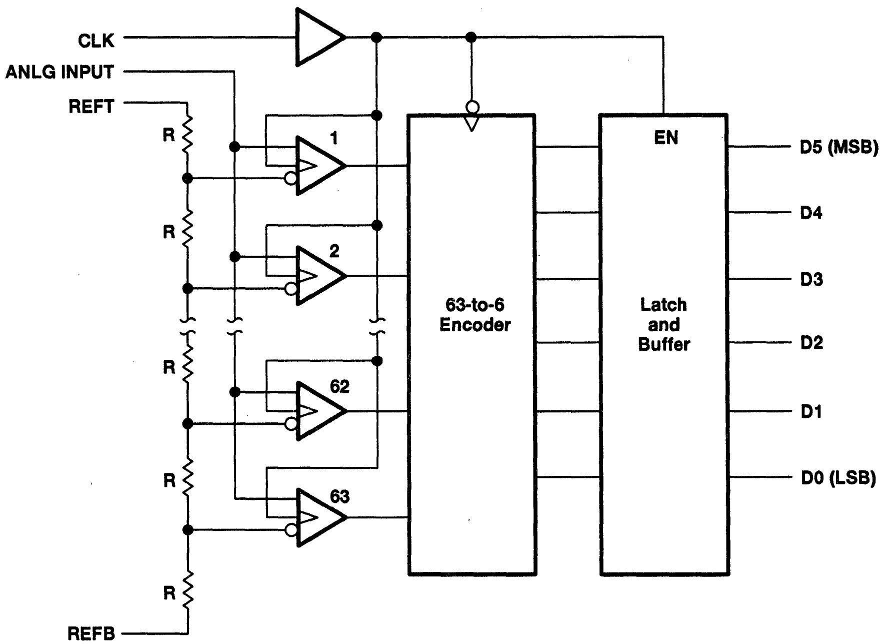


description

The TL5501 is a low-power ultra-high-speed video-band analog-to-digital converter that uses the Advanced Low-Power Schottky (ALS) process. It utilizes the full-parallel comparison (flash method) for high-speed conversion. It converts wide-band analog signals (such as a video signal) to a digital signal at a sampling rate of dc to 30 MHz. Because of this high-speed capability, the TL5501 is suitable for digital video applications such as digital TV, video processing with a computer, or radar signal processing.

The TL5501 is characterized for operation from 0°C to 70°C.

functional block diagram



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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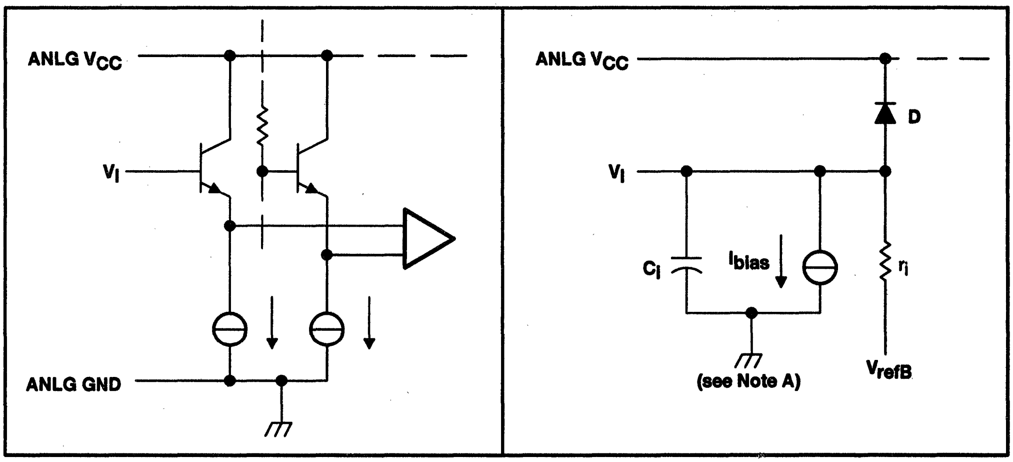
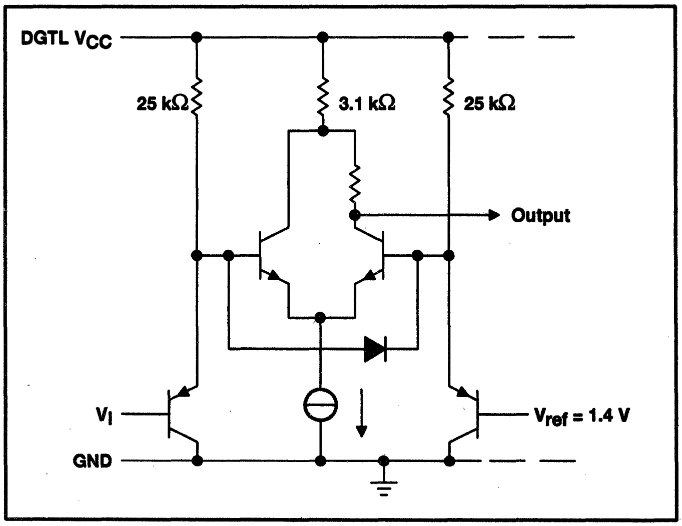
equivalents of analog input circuit



NOTE A: C_i – nonlinear emitter-follower junction capacitance
r_i – linear resistance model for input current transition caused by comparator switching. $V_I < V_{refB}$: Infinite; CLK high: infinite.
V_{refB} – voltage at REFB terminal
I_{bias} – constant input bias current
D – base-collector junction diode of emitter-follower transistor

equivalent of digital input circuit



FUNCTION TABLE

STEP	ANALOG INPUT VOLTAGE	DIGITAL OUTPUT CODE					
0	3.992 V	L	L	L	L	L	L
1	4.008 V	L	L	L	L	L	H
|	|				|		
31	4.488 V	L	H	H	H	H	H
32	4.508 V	H	L	L	L	L	L
33	4.520 V	H	L	L	L	L	H
|	|				|		
62	4.984 V	H	H	H	H	H	L
63	5.000 V	H	H	H	H	H	H

† These values are based on the assumption that V_{refB} and V_{refT} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 4.000 V and the transition to full scale (V_{FT}) is 4.992 V. 1 LSB = 16 mV.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, ANLG V_{CC} (see Note 1) .... −0.5 V to 7 V
Supply voltage range, DGTL V_{CC} .... −0.5 V to 7 V
Input voltage range at digital input, V_I .... −0.5 V to 7 V
Input voltage range at analog input, V_I .... −0.5 V to ANLG V_{CC} +0.5 V
Analog reference voltage range, V_{ref} .... −0.5 V to ANLG V_{CC} +0.5 V
Storage temperature range .... −55°C to 150°C
Operating free-air temperature range .... 0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, ANLG V_{CC}	4.75	5	5.25	V
Supply voltage, DGTL V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Input voltage at analog input, V_I (see Note 2)	4		5	V
Analog reference voltage (top side), V_{refT} (see Note 2)	4	5	5.1	V
Analog reference voltage (bottom side), V_{refB} (see Note 2)	3	4	4.1	V
High-level output current, I_{OH}	−400			µA
Low-level output current, I_{OL}			4	mA
Clock pulse duration, high-level or low-level, t_w	25			ns
Operating free-air temperature, T_A	0		70	°C

NOTE 2: $V_{refB} < V_I < V_{refT}$, $V_{refT} - V_{refB} = 1\ V \pm 0.1\ V$.

electrical characteristics over operating supply voltage range, T_A = 25°C (unless otherwise noted)

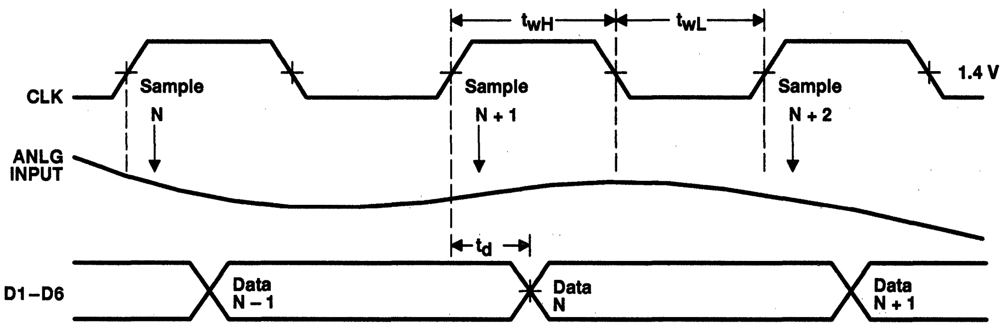
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Analog input current	V_I = 5 V			75	μA
		V_I = 4 V			73	
I_{IH}	Digital high-level input current	V_I = 2.7 V		0	20	μA
I_{IL}	Digital low-level input current	V_I = 0.4 V	– 400	–40		μA
I_I	Digital input current	V_I = 7 V			100	μA
I_{refB}	Reference current	V_{IrefB} = 4 V		–4	–7.2	mA
I_{refT}	Reference current	V_{IrefB} = 5 V		4	7.2	mA
V_{OH}	High-level output voltage	I_{OH} = –400 μA	2.7			V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
r_i	Analog input resistance		100			kΩ
$1C_i$	Analog input capacitance			35	65	pF
I_{CC}	Supply current			40	60	mA

operating characteristics over operating supply voltage range, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error				±0.8	%FSR
f_{max}	Maximum converstion rate		20	30		MHz
t_d	Digital output delay time	See Figure 3		15	30	ns

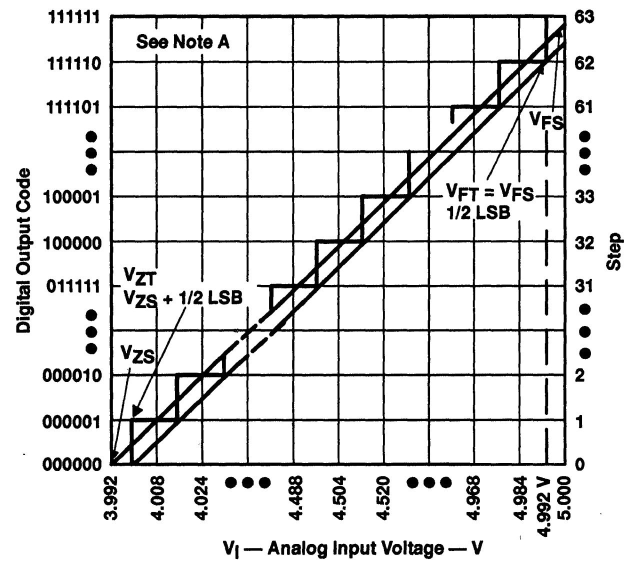
† All typical values are at V_{CC} = 5 V, V_{ref} = 4 V, T_A = 25°C.

timing diagram



TYPICAL CHARACTERISTICS

IDEAL CONVERSION CHARACTERISTICS



NOTE A: This curve is based on the assumption that V_{refB} and V_{refT} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 4.000 V and the transition to full scale (V_{FT}) is 4.992 V. 1 LSB = 16 mV.

Figure 1

END-POINT LINEARITY ERROR

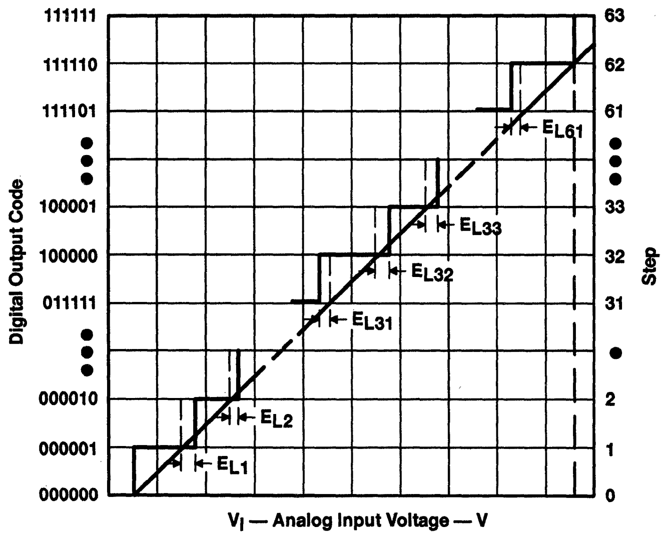


Figure 2

PARAMETER MEASUREMENT INFORMATION

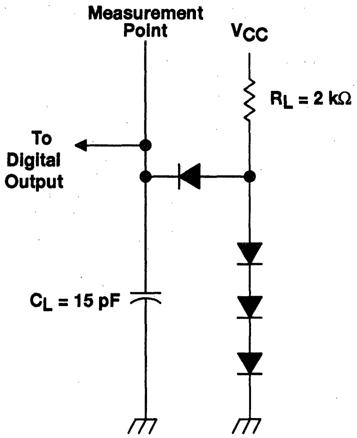


Figure 3. Load Circuit

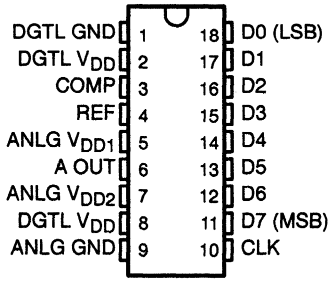
- **8-Bit Resolution**
- **±0.2% Linearity**
- **Maximum Conversion Rate**
  30 MHz Typ
  20 MHz Min
- **Analog Output Voltage Range**
  V_{DD} to V_{DD} –1 V
- **TTL Digital Input Voltage**
- **5-V Single Power-Supply Operation**
- **Low Power Consumption . . . . . . 80 mW Typ**
- **Interchangeable With Fujitsu MB40778**

description

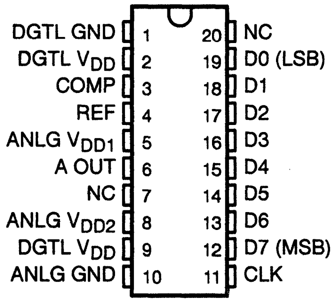
The TLC5602x devices are low-power, ultra-high-speed video, digital-to-analog converters that use the LinEPIC™ 1-µm CMOS process. The TLC5602x converts digital signals to analog signals at a sampling rate of dc to 20 MHz. Because of high-speed operation, the TLC5602x devices are suitable for digital video applications such as digital television, video processing with a computer, and radar-signal processing.

The TLC5602C is characterized for operation from 0°C to 70°C. The TLC5602M is characterized over the full military temperature range of –55°C to 125°C.

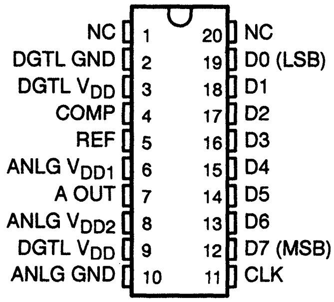
N PACKAGE
(TOP VIEW)



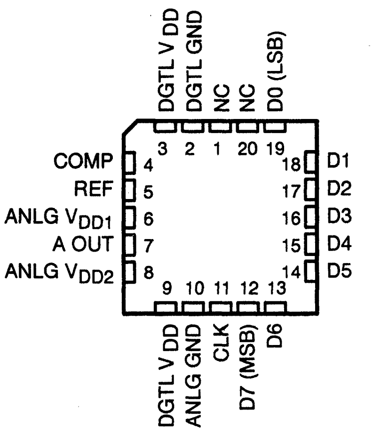
DW PACKAGE
(TOP VIEW)



J PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



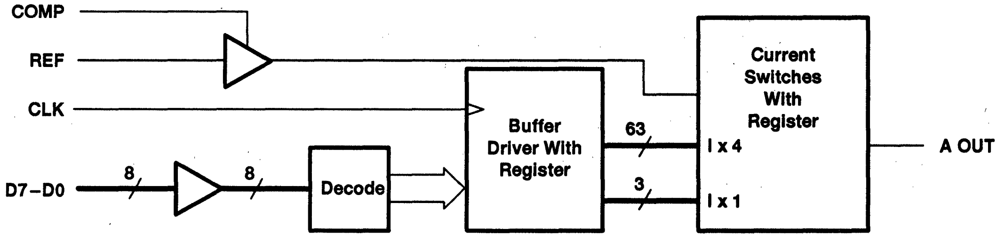
NC—No internal connection

LinEPIC is a trademark of Texas Instruments Incorporated.

AVAILABLE OPTIONS

T_A	PACKAGE			
	WIDE-BODY SMALL OUTLINE (DW)	CERAMIC CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	TLC5602CDW			TLC5602CN
−55°C to 125°C		TLC5602MFK	TLC5602MJ	

functional block diagram

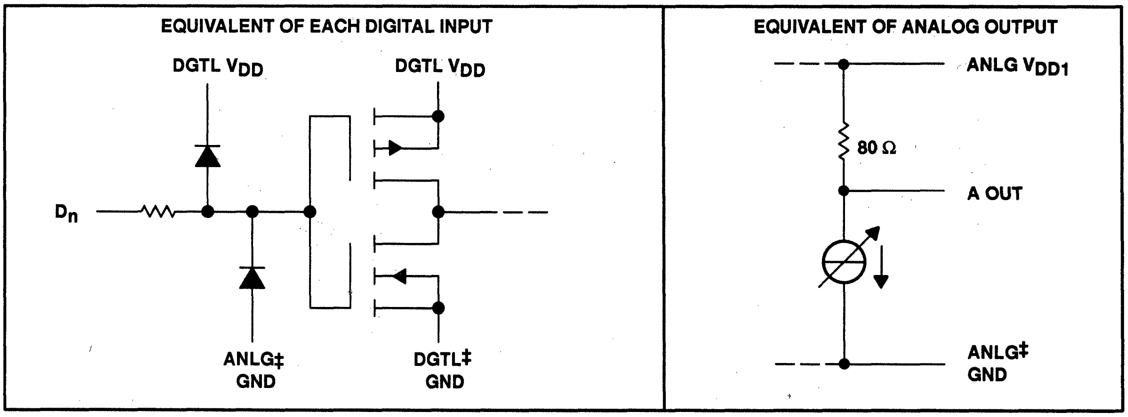


FUNCTION TABLE

STEP	DIGITAL INPUTS								OUTPUT VOLTAGE†
	D7	D6	D5	D4	D3	D2	D1	D0	
0	L	L	L	L	L	L	L	L	3.980 V
1	L	L	L	L	L	L	L	H	3.984 V
|					|				|
127	L	H	H	H	H	H	H	H	4.488 V
128	H	L	L	L	L	L	L	L	4.492 V
129	H	L	L	L	L	L	L	H	4.496 V
|					|				|
254	H	H	H	H	H	H	H	L	4.996 V
255	H	H	H	H	H	H	H	H	5.000 V

† V_{DD} = 5 V and V_{ref} = 4.02 V

schematics of equivalent input and output



‡ ANLG GND and DGTL GND do not connect internally and should be tied together as close to the device terminals as possible.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, ANLG V_{DD}, DGTL V_{DD} .... –0.5 V to 7 V
Digital input voltage range, V_I .... –0.5 V to 7 V
Analog reference voltage range, V_{ref} .... V_{DD}–1.7 V to V_{DD}+0.5 V
Operating free-air temperature range, T_A: TLC5602C .... 0°C to 70°C
TLC5602M .... –55°C to 125°C
Storage temperature range, T_{stg} .... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.75	5	5.25	V
Analog reference voltage, V_{ref}		3.8	4	4.2	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Pulse duration, CLK high or low, t_w		25			ns
Setup time, data before CLK↑, t_{su}		16.5			ns
Hold time, data after CLK↑, t_h		12.5			ns
Phase compensation capacitance, C_{comp} (see Note 1)		1			μF
Load resistance, R_L		75k			Ω
Operating free-air temperature, T_A	TLC5602C	0		70	°C
	TLC5602M	–55		125	°C

NOTE 1: The phase compensation capacitor should be connected between COMP and ANLG GND.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
I_{IH}	High-level input current	Digital inputs	V_I = 5 V				±1	μA
I_{IL}	Low-level input current	Digital inputs	V_I = 0 V				±1	μA
I_{ref}	Input reference current		V_{ref} = 4 V				10	μA
V_{FS}	Full-scale analog output voltage		V_{DD} = 5 V, V_{ref} = 4.02 V		V_{DD}–15	V_{DD}	V_{DD}+15	mV
V_{ZS}	Zero-scale analog output voltage		V_{DD} = 5 V, V_{ref} = 4.02 V, T_A = full range§	TLC5602C	3.919	3.98	4.042	V
				TLC5602M	3.919	3.98	4.042	V
				TLC5602M	3.919	3.98	4.062	V
r_o	Output resistance		T_A = 25°C	TLC5602C	60	80	120	Ω
			T_A = full range§	TLC5602M				
C_i	Input capacitance		f_{clock} = 1 MHz, T_A = 25°C			15		pF
I_{DD}	Supply current		f_{clock} = 20 MHz, V_{ref} = V_{DD}–0.95 V			16	25	mA

‡ All typical values are at V_{DD} = 5 V and T_A = 25°C.
§ Full range for the TLC5602C is 0°C to 70°C, and full range for the TLC5602M is –55°C to 125°C.

operating characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$E_{L(adj)}$	Linearity error, best-straight-line	T_A = full range‡	TLC5602C			±0.2%	
		T_A = 25°C	TLC5602M			±0.2%	
		T_A = full range‡				±0.4%	
E_L	Linearity error, end point				±0.15%		
E_D	Linearity error, differential					±0.2%	
G_{diff}	Differential gain	NTSC 40-IRE modulated ramp, f_{clock} = 14.3 MHz, $Z_L \geq 75$ kΩ			0.7%		
ϕ_{diff}	Differential phase				0.4°		
t_{pd}	Propagation delay time, CLK to analog output	C_L = 10 pF			25		ns
t_s	Settling time to within 1/2 LSB	C_L = 10 pF			30		ns

† All typical values are at V_{DD} = 5 V and T_A = 25°C.
‡ Full range for the TLC5602C is 0°C to 70°C, and full range for the TLC5602M is –55°C to 125°C.

PARAMETER MEASUREMENT INFORMATION

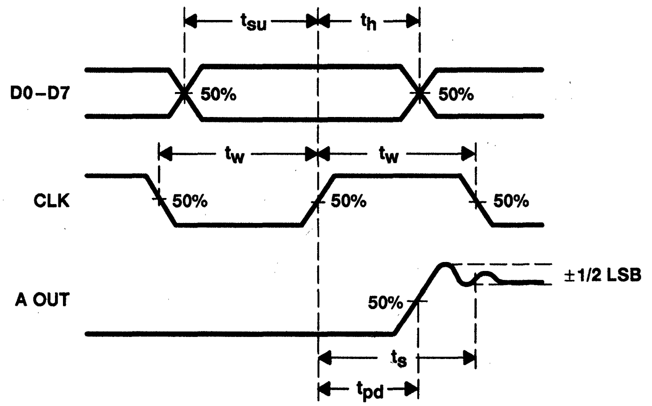


Figure 1. Voltage Waveforms

TYPICAL CHARACTERISTICS

IDEAL CONVERSION CHARACTERISTICS

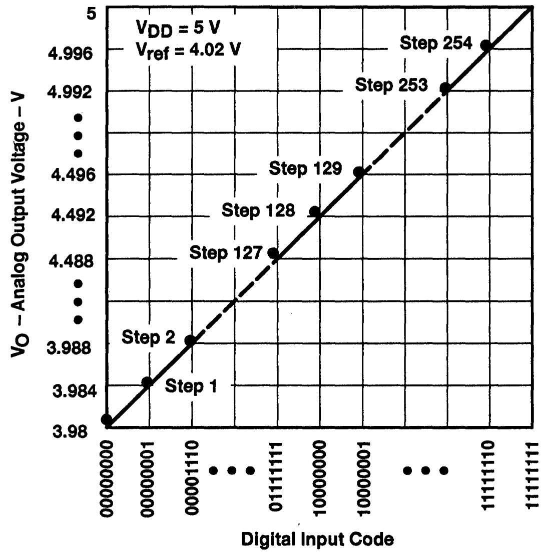


Figure 2

BEST-STRAIGHT-LINE LINEARITY ERROR

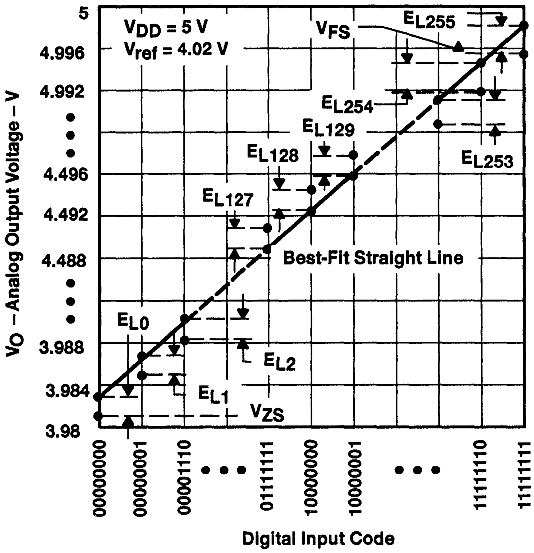
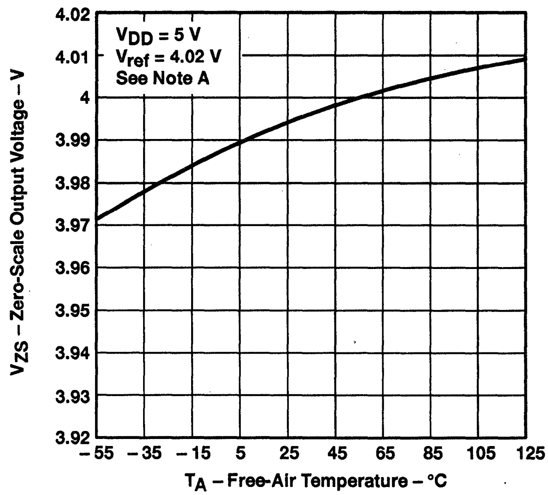


Figure 3

ZERO-SCALE OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE



NOTE A: V_{ref} is relative to ANLG GND. V_{DD} is the voltage between ANLG V_{DD} and DGTL V_{DD} tied together and ANLG GND and DGTL GND tied together.

Figure 4

OUTPUT RESISTANCE vs FREE-AIR TEMPERATURE

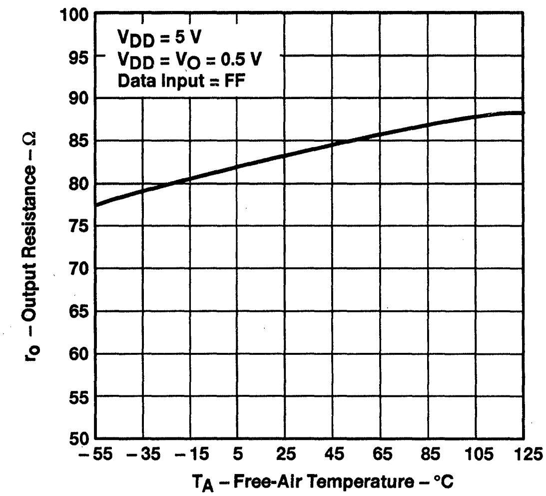


Figure 5

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

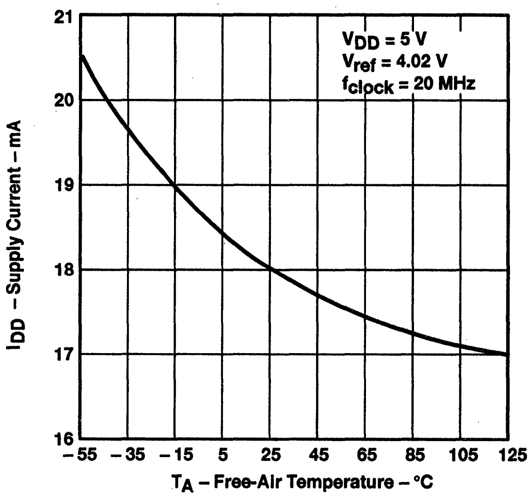
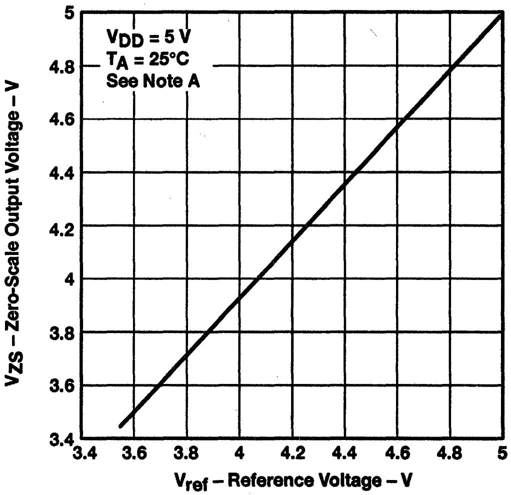


Figure 6

ZERO-SCALE OUTPUT VOLTAGE vs REFERENCE VOLTAGE



NOTE A: V_{ref} is relative to ANLG GND. V_{DD} is the voltage between ANLG V_{DD} and DGTL V_{DD} tied together and ANLG GND and DGTL GND tied together.

Figure 7

APPLICATION INFORMATION

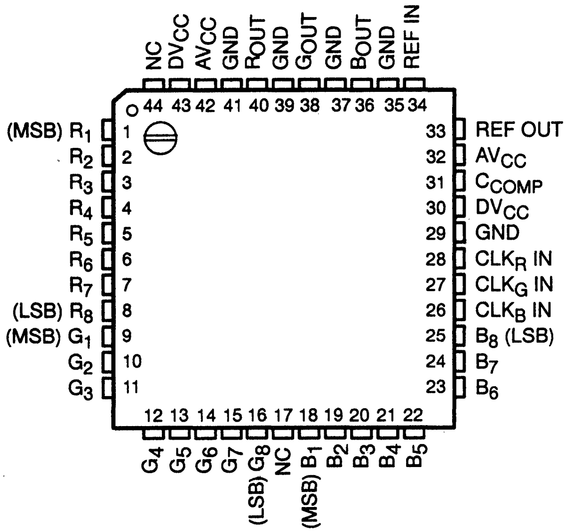
The following design recommendations benefit the TLC5602 user:

- Physically separate and shield external analog and digital circuitry as much as possible to reduce system noise.
- Use RF breadboarding or RF printed-circuit-board (PCB) techniques throughout the evaluation and production process.
- Since ANLG GND and DGTL GND are not connected internally, these terminals need to be connected externally. With breadboards, these ground lines should connect to the power-supply ground through separate leads with proper supply bypassing. A good method is to use a separate twisted pair for the analog and digital supply lines to minimize noise pickup.

  Use wide ground leads or a ground plane on the PCB layouts to minimize parasitic inductance and resistance. The ground plane is the better choice for noise reduction.
- ANLG V_{DD} and DGTL V_{DD} are also separated internally, so they must connect externally. These external PCB leads should also be made as wide as possible. Place a ferrite bead or equivalent inductance in series with ANLG V_{DD} and the decoupling capacitor as close to the device terminals as possible before the ANLG V_{DD} and DGTL V_{DD} leads are connected together on the board.
- Decouple ANLG V_{DD} to ANLG GND and DGTL V_{DD} to DGTL GND with a 1-µF and 0.01-µF capacitor, respectively, as close as possible to the appropriate device terminals. A ceramic chip capacitor is recommended for the 0.01-µF capacitor.
- Connect the phase compensation capacitor between COMP and ANLG GND with as short a lead-in as possible.
- The no-connection (NC) terminals on the small-outline package should be connected to ANLG GND.
- Shield ANLG V_{DD}, ANLG GND, and A OUT from the high-frequency terminals CLK and D7–D0. Place ANLG GND traces on both sides of the A OUT trace on the PCB.

- **8-Bit Resolution**
- **Linearity . . . ±1/2 LSB Maximum**
- **Differential Nonlinearity . . . ±1/2 LSB Maximum**
- **Conversion Rate . . . 60 MHz Min**
- **Nominal Output Signal Operating Range V_{CC} to V_{CC} – 1 V**
- **TTL Digital Input Voltage**
- **5-V Single Power Supply Operation**
- **Low Power Consumption . . . 350 mW Typ**

**FR PACKAGE
(TOP VIEW)**



NC – No internal connection

description

The TL5632C is a low-power ultra-high-speed video digital-to-analog converter that uses the Advanced Low-Power Schottky (ALS) process. The device has a three channel I/O; the red, the blue, and the green channel. The red, blue, and green signals are referred to collectively as the RGB signal. An internally generated reference is also provided for the standard video output voltage range. Conversion of digital signals to analog signals can be at a sampling rate of dc to 60 MHz. The high conversion rate makes the TL5632C suitable for digital television, computer digital video processing, and high-speed data conversion.

The TL5632C is characterized for operation from 0°C to 70°C.

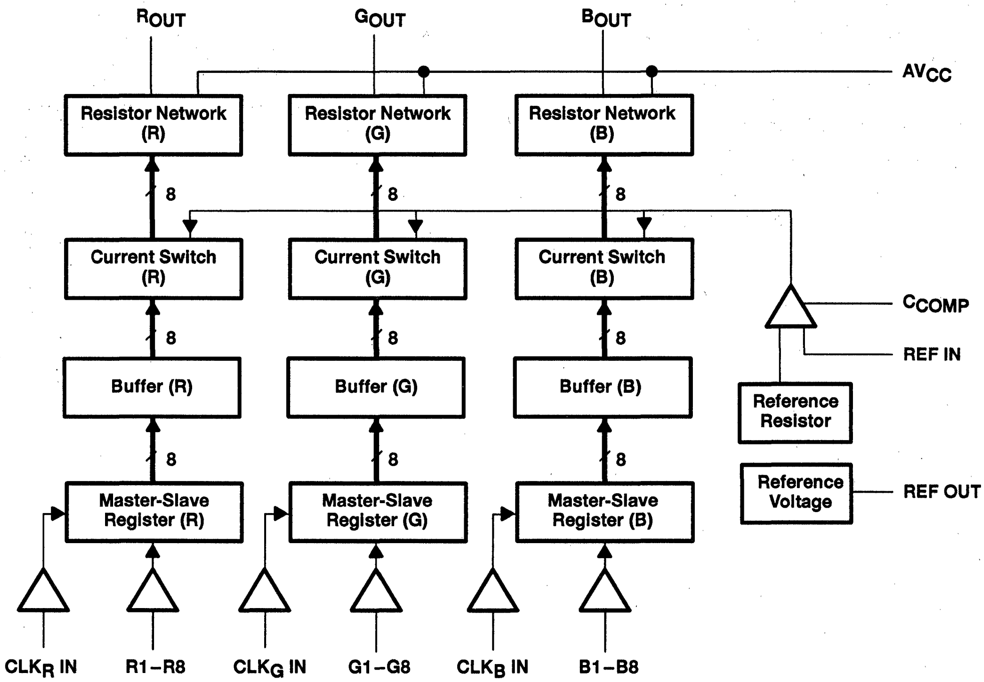
FUNCTION TABLE

STEP	DIGITAL INPUT	OUTPUT VOLTAGE
0	L L L L L L L L	3.980 V
1	L L L L L L L H	3.984 V
•	•	•
•	•	•
•	•	•
127	L H H H H H H H	4.488 V
128	H L L L L L L L	4.492 V
129	H L L L L L L H	4.996 V
•	•	•
•	•	•
•	•	•
254	H H H H H H H L	4.996 V
255	H H H H H H H H	5.000 V

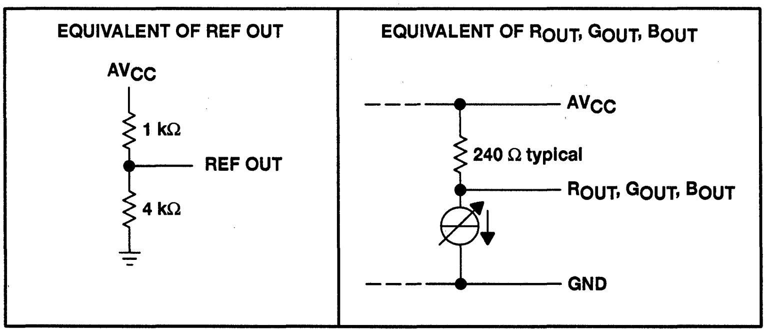
AVAILABLE OPTIONS

T_A	PACKAGE
0°C to 70°C	TL5632CFR

functional block diagram



schematics of outputs



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$B_1 - B_8$	18 – 25	I	B-channel digital input (B_1 = MSB)
B_{OUT}	36	O	B-channel analog output
C_{COMP}	31		Phase compensation capacitance. A 1 μF capacitor is connected from C_{COMP} to GND.
CLK_B IN	26	I	B-channel clock input
CLK_G IN	27	I	G-channel clock input
CLK_R IN	28	I	R-channel clock input
$G_1 - G_8$	9 – 16	I	G-Channel digital input (G_1 = MSB)
GND	29, 35, 37, 39, 41		Ground. All GND terminals are connected internally; however, all GND terminals should be connected externally to a ground plane or equivalent low impedance ground return.
G_{OUT}	38	O	G-channel analog output
NC	17, 44		No connection internally
$R_1 - R_8$	1 – 8	I	R-channel digital input (R_1 = MSB)
R_{OUT}	40	O	R-channel analog output
AV_{CC}	32, 42		Analog power supply voltage
DV_{CC}	30, 43		Digital power supply voltage
REF IN	34	I	Reference voltage input. REF IN accepts the reference voltage on REF OUT. An external reference can also be applied consistent with Note 1.
REF OUT	33	O	Reference voltage output. An internal voltage divider generates the voltage level (see schematics of outputs, page 2).

NOTE 1: $V_{CC} - V_{ref} \leq 1.2$ V

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Power supply voltage range, AV_{CC}, DV_{CC} (see Note 2) .... −0.3 V to 7 V
Digital input voltage range, V_I .... −0.3 V to DV_{CC}
Analog output voltage range, R_{OUT}, G_{OUT}, B_{OUT}, C_{COMP} (externally applied) .... −0.3 V to AV_{CC} + 0.3 V
Reference input range, REF IN .... −0.3 V to AV_{CC} + 0.3 V
Reference output range, REF OUT .... −0.3 V to AV_{CC} + 0.3 V
Operating free-air temperature range, T_A .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: All voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, AV_{CC}, DV_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Reference voltage, V_{ref} (see Note 1)	3.8	4	4.2	V
Setup time, data before CLK↑, t_{su1}	10			ns
Hold time, data after CLK↑, t_{h1}	3			ns
Pulse duration at high level, t_{w1}	8.3			ns
Pulse duration at low level, t_{w2}	8.3			ns
External phase compensation capacitance, C_{COMP}	1			µF
Operating free-air temperature, T_A	0		70	°C

NOTE 1: $V_{CC} - V_{ref} \leq 1.2$ V

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

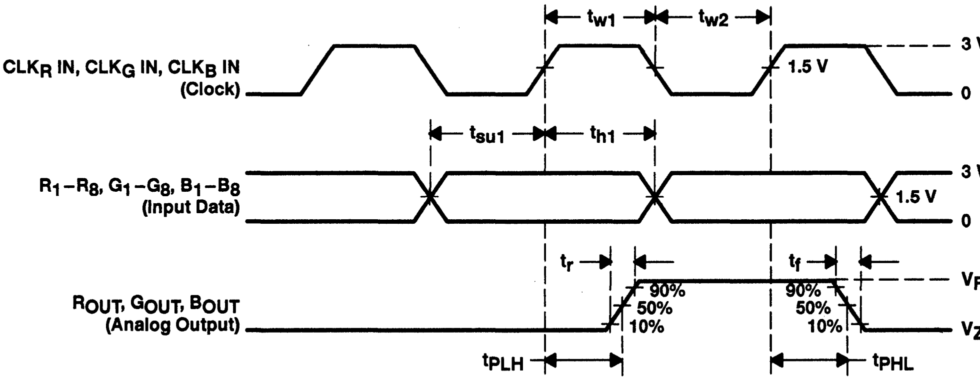
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
	Resolution					8	Bit
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_{IH} = 2.7 V			20	µA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_{IH} = 2.7 V	−400			µA
I_{ref}	Reference input current	REF IN = 4 V				10	µA
V_{ref}	Reference output voltage	V_{CC} = 5 V,	With internal reference	3.8	4	4.2	V
V_{FS}	Full-scale analog output voltage	V_{IH} = 2 V,	REF IN = 4 V	AV_{CC}−15	AV_{CC}	AV_{CC}+15	mV
V_{ZS}	Zero-scale analog output voltage	V_{IL} = 0.8 V,	REF IN = 4 V	3.9	3.98	4.05	V
	RGB full-scale ratio			0%	4%	8%	
z_o	Output impedance			200	240	280	Ω
I_{CC}	Supply current				70	90	mA

operating characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
E_L	Linearity error	End point,	REF IN = 4 V			±0.5	LSB
E_D	Differential linearity error	REF IN = 4 V				±0.5	LSB
f_c	Maximum conversion rate			60			MHz
t_{PLH}	Propagation delay time, low-to-high level	T_A = 25°C,	$C_L \leq 5$ pF‡		10		ns
t_{PHL}	Propagation delay time, high-to-low level	T_A = 25°C,	$C_L \leq 5$ pF‡		10		ns
t_r	Rise time	T_A = 25°C,	$C_L \leq 5$ pF‡		5		ns
t_f	Fall time	T_A = 25°C,	$C_L \leq 5$ pF‡		5		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ C_L includes probe and jig capacitances.

PARAMETER MEASUREMENT INFORMATION



TYPICAL CHARACTERISTICS

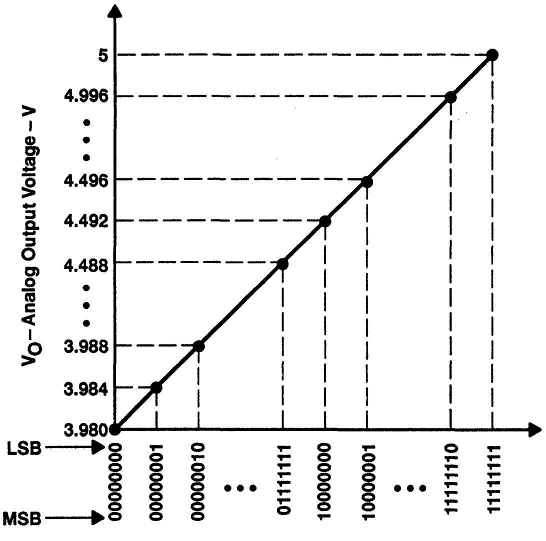


Figure 1. Ideal Conversion Characteristics

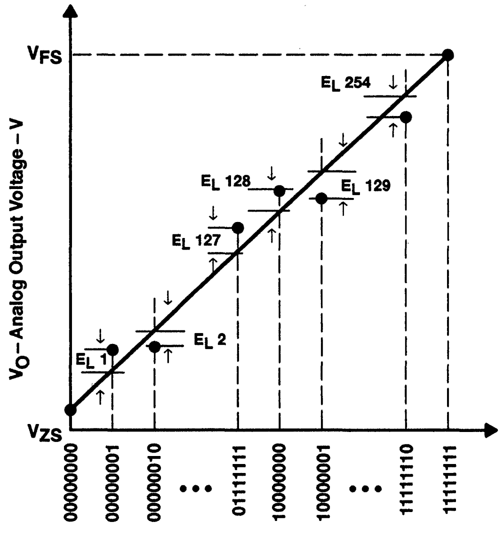


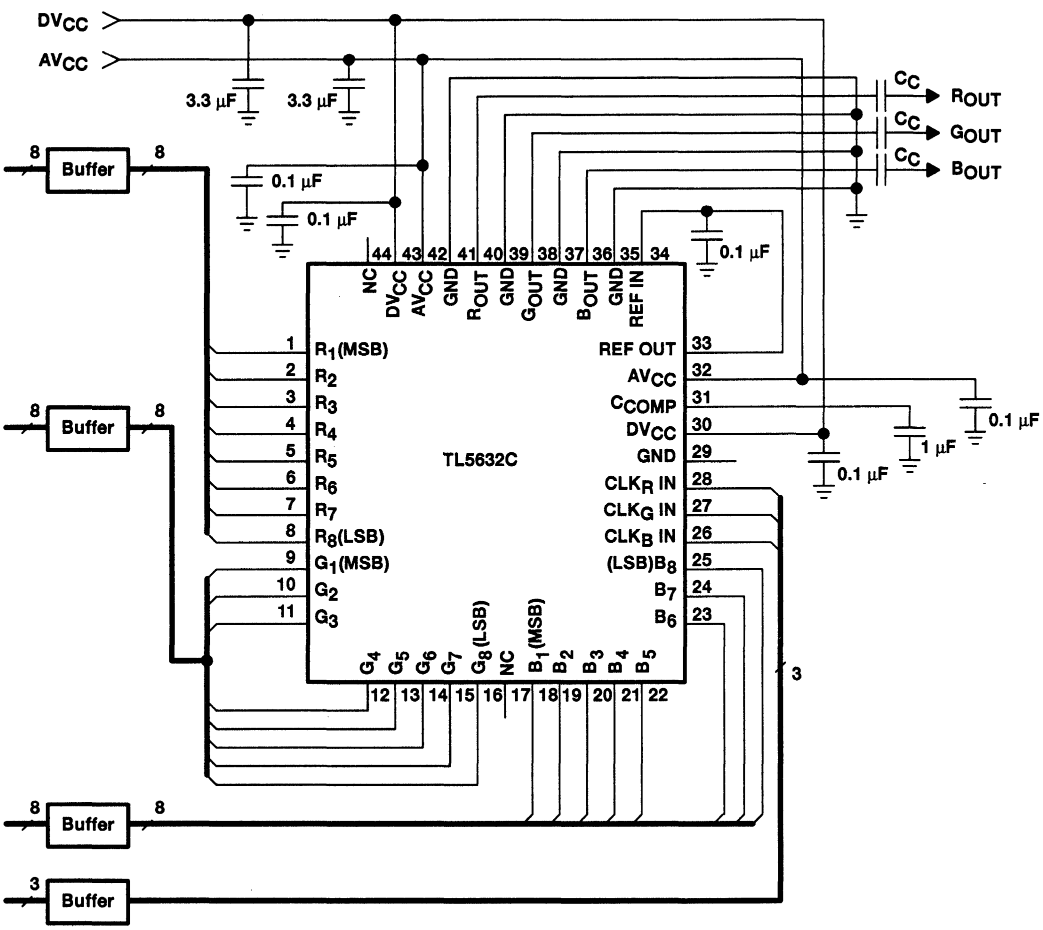
Figure 2. End-Point Linearity Error

APPLICATION INFORMATION

The following design procedures should be used for optimum operation.

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or RF printed-circuit-board (PCB) techniques should be used throughout the evaluation and production process.
- Wide ground leads or a ground plane should be used on the PCB layouts to minimize parasitic inductance and resistance. A ground plane is the better choice for noise reduction.
- AV_{CC} and DV_{CC} are also separate internally, so they must be connected externally. These external PCB leads should also be made as wide as possible. A ferrite bead or equivalent inductance should be placed in series with AV_{CC} and the decoupling capacitor before the AV_{CC} and DV_{CC} leads are connected together on the board. It is critical that the supply voltage applied to AV_{CC} be as noise free and ripple free as possible. Ripple and noise rejection should be a minimum of 60 dB below the full-scale output range of 1 V peak-to-peak.
- AV_{CC} to GND and DV_{CC} to GND should be decoupled with 3.3-µF and 0.1-µF capacitors, respectively, as close as possible to the appropriate device terminals. A ceramic chip capacitor is recommended for the 0.1-µF capacitor.
- The phase compensation capacitor should be connected between C_{COMP} and GND with as short a lead-in as possible.
- The no-connection (NC) terminals on the small-outline package should be connected to GND.
- AV_{CC}, DV_{CC}, and R_{OUT}, G_{OUT}, and B_{OUT} should be shielded from the high-frequency terminals CLK_R IN, CLK_G IN ,and CLK_B IN and the input data terminals. GND traces should be placed on both sides of the R_{OUT}, G_{OUT}, and B_{OUT} traces on the PCB to the following signal processing stage. These output traces should be as short as possible.

APPLICATION INFORMATION



NOTES: A. Buffers are SN74AS244 or equivalent.
B. 0.1 µF capacitors should be placed as close to the device terminals as possible.
C. The coupling capacitor (C_C) value is application specific and selectable by the user.

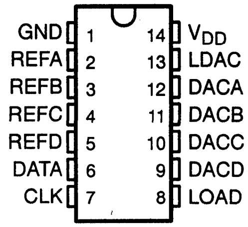
Figure 3. Typical Bypass, Buffer, and Output Configuration

TLC5620C, TLC5620I
QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS081A – NOVEMBER 1994 – REVISED JANUARY 1995

- **Four 8-Bit Voltage Output DACs**
- **5-V Single-Supply Operation**
- **Serial Interface**
- **High-Impedance Reference Inputs**
- **Programmable 1 or 2 Times Output Range**
- **Simultaneous-Update Facility**
- **Internal Power-On Reset**
- **Low Power Consumption**
- **Half-Buffered Output**

N OR D PACKAGE
(TOP VIEW)



applications

- **Programmable Voltage Sources**
- **Digitally-Controlled Amplifiers/Attenuators**
- **Mobile Communications**
- **Automatic Test Equipment**
- **Process Monitoring and Control**
- **Signal Synthesis**

description

The TLC5620C and TLC5620I are quadruple 8-bit voltage output digital-to-analog converters (DACs) with buffered reference inputs (high impedance). The DACs produce an output voltage that ranges between either one or two times the reference voltages and GND, and the DACs are monotonic. The device is simple to use, running from a single supply of 5 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

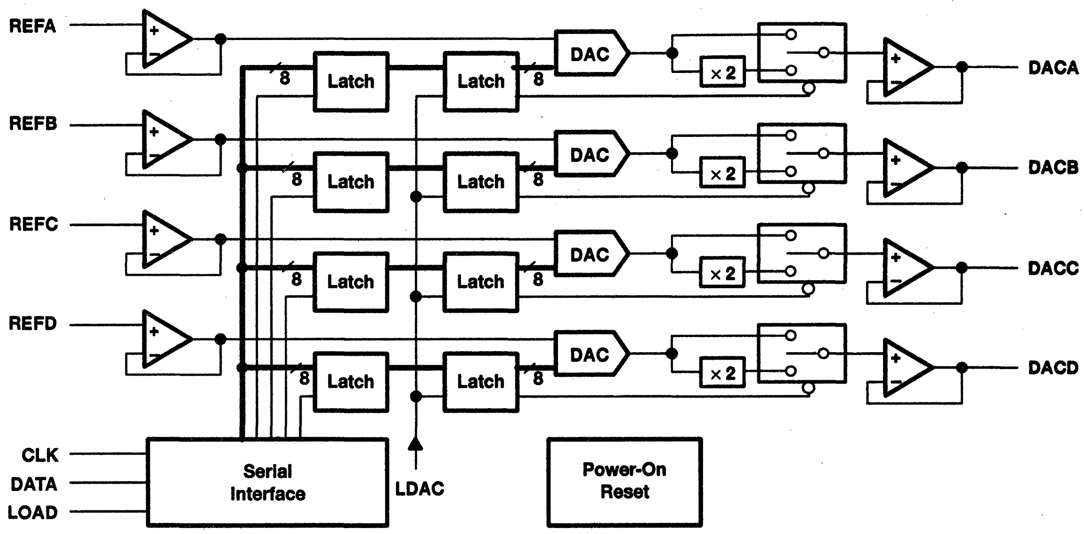
Digital control of the TLC5620C and TLC5620I are over a simple 3-wire serial bus that is CMOS compatible and easily interfaced to all popular microprocessor and microcontroller devices. The 11-bit command word comprises 8 bits of data, 2 DAC select bits and a range bit, the latter allowing selection between the times 1 or times 2 output range. The DAC registers are double buffered, allowing a complete set of new values to be written to the device, then all DAC outputs updated simultaneously through control of the LDAC terminal. The digital inputs feature Schmitt triggers for high noise immunity.

The 14-terminal small-outline (SO) package allows digital control of analog functions in space-critical applications. The TLC5620C is characterized for operation from 0°C to 70°C. The TLC5620I is characterized for operation from −40°C to 85°C. The TLC5620C and TLC5620I do not require external trimming.

AVAILABLE OPTIONS

T_A	PACKAGE	
	SMALL OUTLINE (D)	PLASTIC DIP (N)
0°C to 70°C	TLC5620CD	TLC5620CN
−40°C to 85°C	TLC5620ID	TLC5620IN

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLK	7	I	Serial-interface clock, data enters on the negative edge
DACA	12	O	DAC A analog output
DACB	11	O	DAC B analog output
DACC	10	O	DAC C analog output
DACD	9	O	DAC D analog output
DATA	6	I	Serial-interface digital-data input
GND	1	I	Ground return and reference terminal
LDAC	13	I	DAC-update latch control
LOAD	8	I	Serial-interface load control
REFA	2	I	Reference voltage input to DACA
REFB	3	I	Reference voltage input to DACB
REFC	4	I	Reference voltage input to DACC
REFD	5	I	Reference voltage input to DACD
V_{DD}	14	I	Positive supply voltage

detailed description

The TLC5620 is implemented using four resistor-string digital-to-analog converters (DACs). The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes listed in Table 2. One end of each resistor string is connected to the GND terminal and the other end is fed from the output of the reference input buffer. Monotonicity is maintained by use of the resistor strings. Linearity depends upon the matching of the resistor elements and upon the performance of the output buffer. Because the inputs are buffered, the DACs always presents a high-impedance load to the reference source.

detailed description (continued)

Each DAC output is buffered by a configurable-gain output amplifier, which can be programmed to times 1 or times 2 gain.

On powerup, the DACs are reset to CODE 0.

Each output voltage is given by:

$$V_O(\text{DACA|B|C|D}) = \text{REF} \times \frac{\text{CODE}}{256} \times (1 + \text{RNG bit value})$$

where CODE is in the range 0 to 255 and the range (RNG) bit is a 0 or 1 within the serial-control word.

data interface

With LOAD high, data is clocked into the DATA terminal on each falling edge of CLK. Once all data bits have been clocked in, LOAD is pulsed low to transfer the data from the serial-input register to the selected DAC as shown in Figure 1. If LDAC is low, the selected DAC output voltage is updated and LOAD goes low. If LDAC is high during serial programming, the new value is stored within the device and can be transferred to the DAC output at a later time by pulsing LDAC low as shown in Figure 2. Data is entered MSB first.

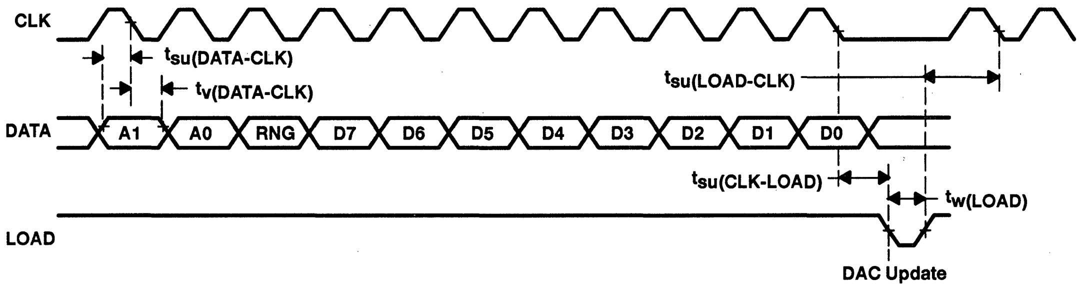


Figure 1. LOAD-Controlled Update (LDAC = Low)

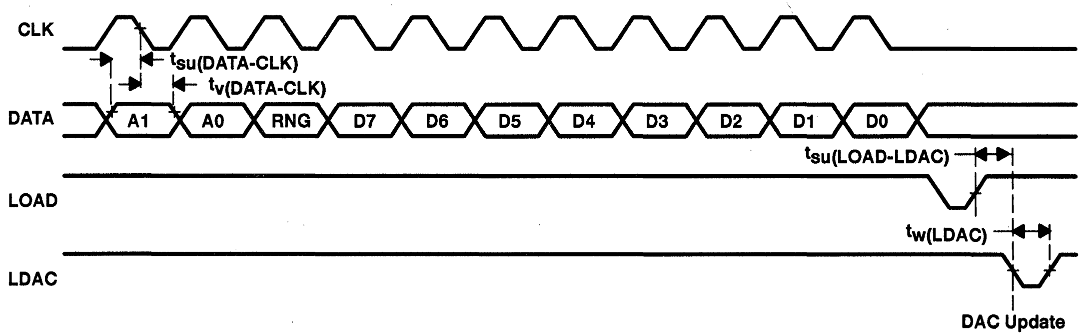


Figure 2. LDAC-Controlled Update

data interface (continued)

Table 1 lists the A1 and A0 bits and the selection of the updated DACs. The RNG bit controls the DAC output range. When RNG = low, the output range is between the applied reference voltage and GND, and when RNG = high, the range is between twice the applied reference voltage and GND.

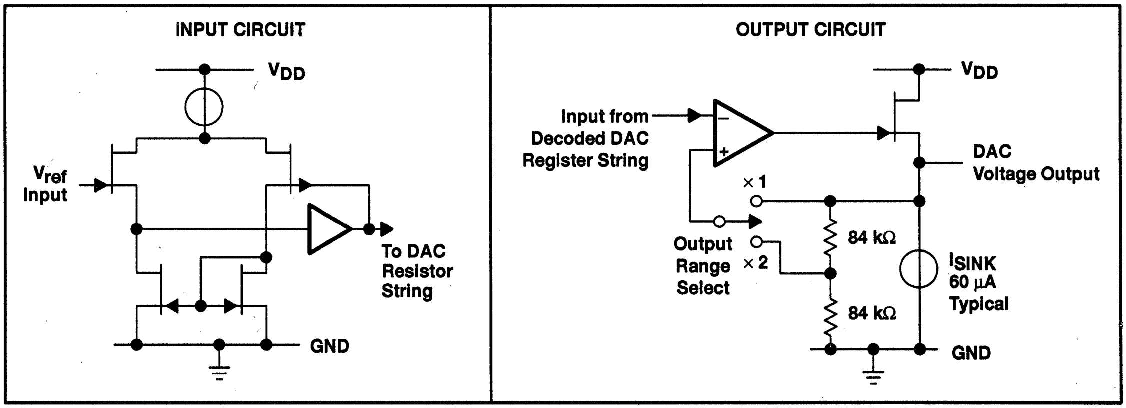
Table 1. Serial-Input Decode

A1	A0	DAC UPDATED
0	0	DACA
0	1	DACB
1	0	DACC
1	1	DACD

Table 2. Ideal-Output Transfer

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	(1/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	(127/256) × REF (1+RNG)
1	0	0	0	0	0	0	0	(128/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	(255/256) × REF (1+RNG)

equivalent inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} – GND) .... 7 V
Digital input voltage range .... GND – 0.3 V to V_{DD} + 0.3 V
Reference input voltage range, V_{ID} .... GND – 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A: TLC5620C .... 0°C to 70°C
TLC5620I .... –40°C to 85°C
Storage temperature range, T_{stg} .... –50°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 230°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.75		5.25	V
High-level digital input voltage, V_{IH}		0.8 V_{DD}			V
Low-level digital input voltage, V_{IL}				0.8	V
Reference voltage, V_{ref} [A|B|C|D]			V_{DD}–1.5		V
Load resistance, R_L		10			kΩ
Setup time, data input, $t_{su(DATA-CLK)}$ (see Figures 1 and 2)		50			ns
Valid time, data input valid after CLK↓, $t_{v(DATA-CLK)}$ (see Figures 1 and 2)		50			ns
Setup time, CLK 11th falling edge to LOAD, $t_{su(CLK-LOAD)}$ (see Figure 1)		50			ns
Setup time, LOAD↑ to CLK↓, $t_{su(LOAD-CLK)}$ (see Figure 1)		50			ns
Pulse duration, LOAD, $t_{w(LOAD)}$ (see Figure 1)		250			ns
Pulse duration, LDAC, $t_{w(LDAC)}$ (see Figure 1)		250			ns
Setup time, LOAD↑ to LDAC↓, $t_{su(LOAD-LDAC)}$ (see Figure 1)		0			ns
CLK frequency				1	MHz
Operating free-air temperature, T_A	TLC5620C	0		70	°C
	TLC5620I	–40		85	°C

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V ± 5%, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current	$V_I = V_{DD}$			±10	µA
I_{IL}	Low-level digital input current	V_I = 0 V			±10	µA
$I_{O(sink)}$	Output sink current	Each DAC output	20			µA
$I_{O(source)}$	Output source current	Each DAC output	2			mA
C_i	Input capacitance			15		pF
C_i	Reference input capacitance			15		pF
I_{DD}	Supply current	V_{DD} = 5 V			2	mA
I_{ref}	Reference input current	V_{DD} = 5 V, V_{ref} = 2 V			±10	µA
E_L	Linearity error (end point corrected)	V_{ref} = 2 V, × 2 gain (see Note 1)			±1	LSB
E_D	Differential-linearity error	V_{ref} = 2 V, × 1 gain (see Note 2)			±0.9	LSB
E_{ZS}	Zero-scale error	V_{ref} = 2 V, × 2 gain (see Note 3)	0		30	mV
	Zero-scale error temperature coefficient	V_{ref} = 2 V, × 2 gain (see Note 4)		10		µV/°C
E_{FS}	Full-scale error	V_{ref} = 2 V, × 2 gain (see Note 5)			±60	mV
	Full-scale error temperature coefficient	V_{ref} = 2 V, × 2 gain (see Note 6)		±25		µV/°C
PSRR	Power-supply sensitivity	See Notes 7 and 8		0.5		mV/V

NOTES: 1. Integral nonlinearity (INL) is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full-scale errors).
2. Differential nonlinearity (DNL) is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
3. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
4. Zero-scale error temperature coefficient is given by: ZSETC = $[ZSE(T_{max}) - ZSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
5. Full-scale error is the deviation from the ideal full-scale output (V_{ref} – 1 LSB) with an output load of 10 kΩ.
6. Full-scale temperature coefficient is given by: FSETC = $[FSE(T_{max}) - FSE\ (T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
7. Zero-scale error rejection ratio (ZSE-RR) is measured by varying the V_{DD} voltage from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
8. Full-scale error rejection ratio (FSE-RR) is measured by varing the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage.

operating characteristics over recommended operating free-air temperature range, V_{DD} = 5 V ± 5%, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate	C_L = 100 pF, R_L = 10 kΩ		1		V/µs
Output settling time	To 0.5 LSB, C_L = 100 pF, R_L = 10 kΩ, See Note 9		10		µs
Large-signal bandwidth	Measured at –3 dB point		100		kHz
Digital crosstalk	CLK = 1-MHz square wave measured at DACA-DACD		–50		dB
Reference feedthrough	See Note 10		–60		dB
Channel-to-channel isolation	See Note 11		–60		dB
Reference input bandwidth	See Note 12		100		kHz

NOTES: 9. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 00 hex to FF hex or FF hex to 00 hex. For TLC5620C: V_{DD} = 5 V, V_{ref} = 2 V and range = ×2. For TLC5620I: V_{DD} = 3 V, V_{ref} = 1.25 V and range ×2.
10. Reference feedthrough is measured at any DAC output with an input code = 00 hex with a V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
11. Channel-to-channel isolation is measured by setting the input code of one DAC to FF hex and the code of all other DACs to 00 hex with V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
12. Reference bandwidth is the –3 dB bandwidth with an input at V_{ref} = 1.25 V dc + 2 V_{pp}, with a digital input code of full-scale.

PARAMETER MEASUREMENT INFORMATION

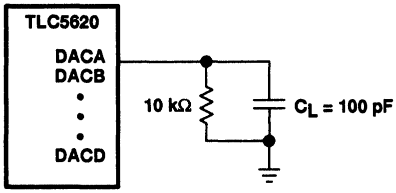


Figure 3. Slewing Settling Time and Linearity Measurements

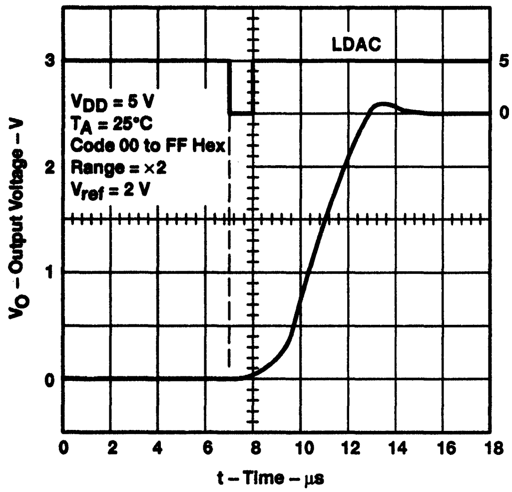


Figure 4. Positive Rise and Setting Time V_{DD} = 5 V

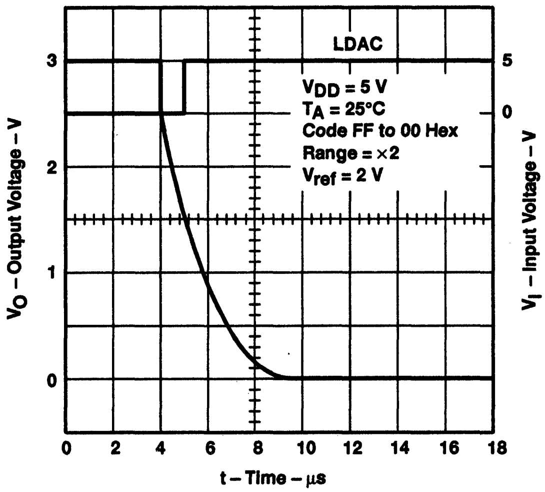


Figure 5. Negative Fall and Setting Time V_{DD} = 5 V

TYPICAL CHARATERISTICS

OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE

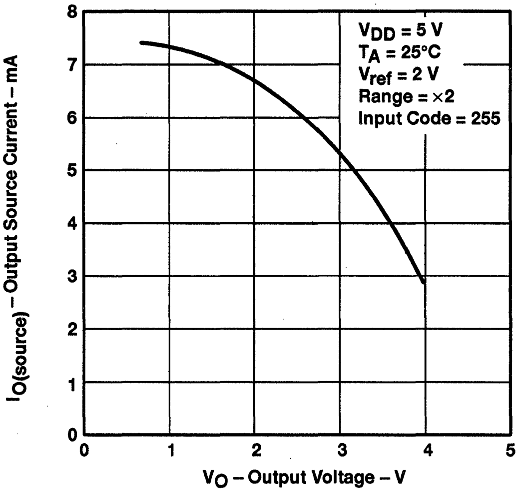


Figure 6

SUPPLY CURRENT vs TEMPERATURE

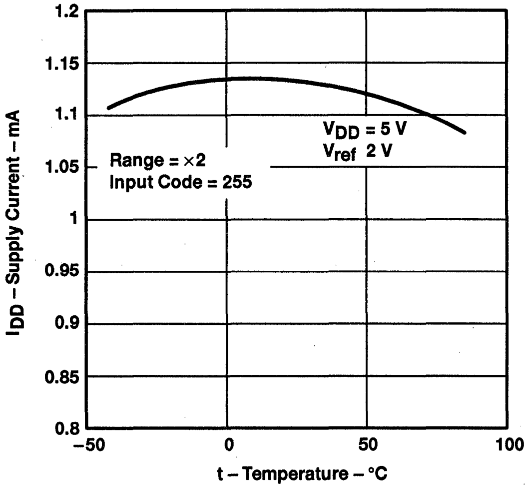


Figure 7

RELATIVE GAIN vs FREQUENCY

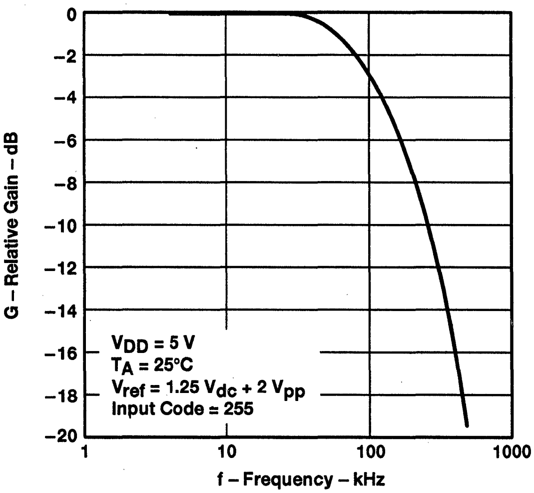


Figure 8

RELATIVE GAIN vs FREQUENCY

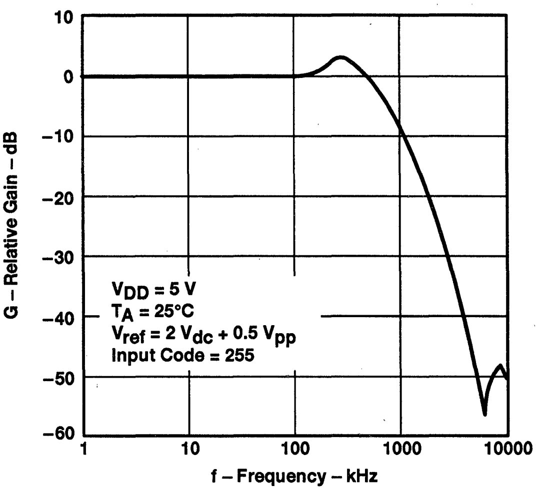
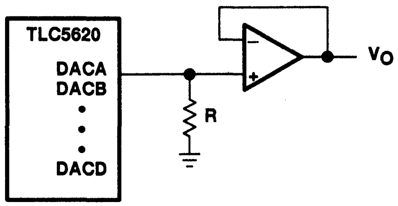


Figure 9

APPLICATION INFORMATION

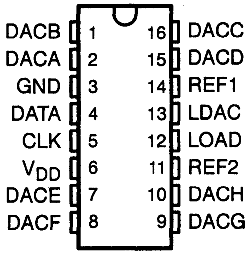


NOTE A: Resistor R ≥ 10 kΩ

Figure 10. Output Buffering Schemes

- **Eight 8-Bit Voltage Output DACs**
- **5-V Single-Supply Operation**
- **Serial Interface**
- **High-Impedance Reference Inputs**
- **Programmable 1 or 2 Times Output Range**
- **Simultaneous-Update Facility**
- **Internal Power-On Reset**
- **Low Power Consumption**
- **Half-Buffered Output**

N OR DW PACKAGE
(TOP VIEW)



applications

- **Programmable Voltage Sources**
- **Digitally-Controlled Amplifiers/Attenuators**
- **Mobile Communications**
- **Automatic Test Equipment**
- **Process Monitoring and Control**
- **Signal Synthesis**

description

The TLC5628C and TLC5628I are octal 8-bit voltage output digital-to-analog converters (DACs) with buffered reference inputs (high impedance). The DACs produce an output voltage that ranges between either one or two times the reference voltages and GND and are monotonic. The device is simple to use, running from a single supply of 5 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

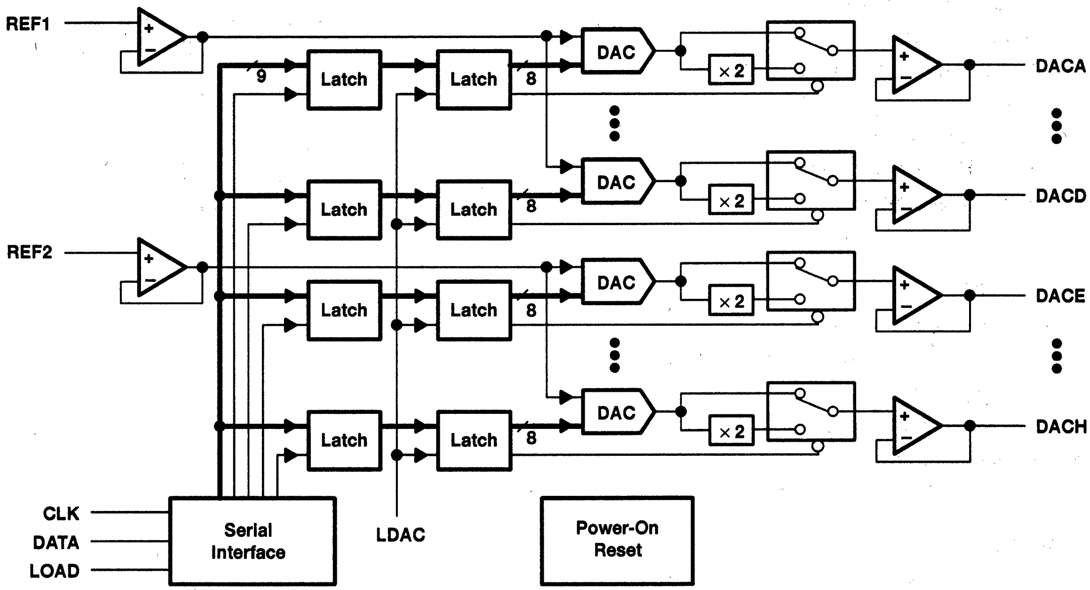
Digital control of the TLC5628C and TLC5628I are over a simple 3-wire serial bus that is CMOS compatible and easily interfaced to all popular microprocessor and microcontroller devices. The 12-bit command word comprises 8 bits of data, 3 DAC select bits and a range bit, the latter allowing selection between the times 1 or times 2 output range. The DAC registers are double buffered, allowing a complete set of new values to be written to the device, then all DAC outputs updated simultaneously through control of the LDAC terminal. The digital inputs feature Schmitt triggers for high noise immunity.

The 16-terminal small-outline (DW) package allows digital control of analog functions in space-critical applications. The TLC5628C is characterized for operation from 0°C to 70°C. The TLC5628I is characterized for operation from –40°C to 85°C. The TLC5628C and TLC5628I do not require external trimming.

AVAILABLE OPTIONS

	PACKAGE	
T_A	SMALL OUTLINE (DW)	PLASTIC DIP (N)
0°C to 70°C	TLC5628CDW	TLC5628CN
–40°C to 85°C	TLC5628IDW	TLC5628IN

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
CLK	5	I	Serial-interface clock, data enters on the negative edge
DACA	2	O	DACA analog output
DACB	1	O	DACB analog output
DACC	16	O	DACC analog output
DACD	15	O	DACD analog output
DACE	7	O	DACE analog output
DACF	8	O	DACF analog output
DACG	9	O	DACG analog output
DACH	10	O	DACH analog output
DATA	4	I	Serial-interface digital data input
GND	3	I	Ground return and reference terminal
LDAC	13	I	DAC-update latch control
LOAD	12	I	Serial-interface load control
REF1	14	I	Reference voltage input to DACA
REF2	11	I	Reference voltage input to DACB
V_{DD}	6	I	Positive supply voltage

detailed description

The TLC5628 is implemented using eight resistor-string digital-to-analog converters (DACs). The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes listed in Table 2. One end of each resistor string is connected to the GND terminal and the other end is fed from the output of the reference input buffer. Monotonicity is maintained by use of the resistor strings. Linearity depends upon the matching of the resistor elements and upon the performance of the output buffer. Because the inputs are buffered, the DACs always present a high-impedance load to the reference sources. There are two input reference terminals; REF1 is used for DACA through DACD and REF2 is used by DACE through DACH.

Each DAC output is buffered by a configurable-gain output amplifier, which can be programmed to times 1 or times 2 gain.

On powerup, the DACs are reset to CODE 0.

Each output voltage is given by:

$$V_O(\mathrm{DACA|B|C|D|E|F|G|H}) = \mathrm{REF} \times \frac{\mathrm{CODE}}{256} \times (1 + \mathrm{RNG\ bit\ value})$$

where CODE is in the range 0 to 255 and the range (RNG) bit is a 0 or 1 within the serial-control word.

data interface

With LOAD high, data is clocked into the DATA terminal on each falling edge of CLK. Once all data bits have been clocked in, LOAD is pulsed low to transfer the data from the serial-input register to the selected DAC as shown in Figure 1. If LDAC is low, the selected DAC output voltage is updated and LOAD goes low. If LDAC is high during serial programming, the new value is stored within the device and can be transferred to the DAC output at a later time by pulsing LDAC low as shown in Figure 2. Data is entered MSB first.

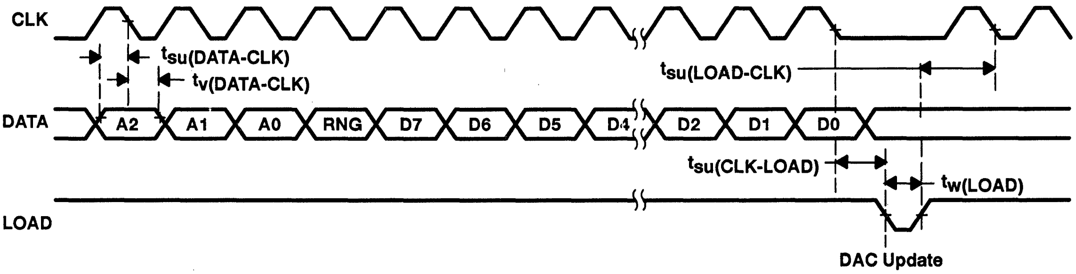


Figure 1. LOAD-Controlled Update (LDAC = Low)

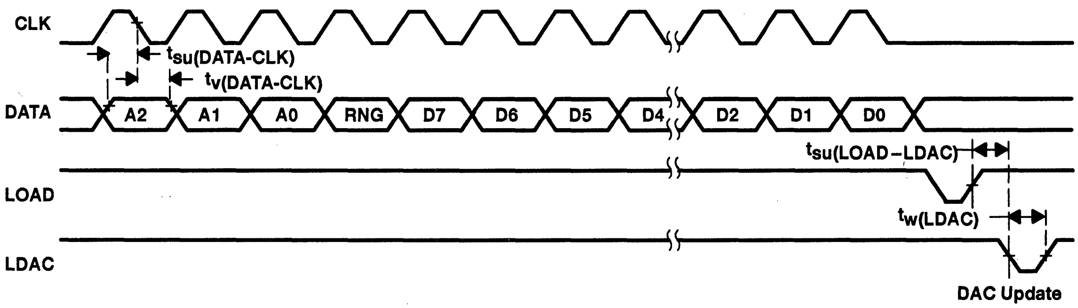


Figure 2. LDAC-Controlled Update

data interface (continued)

Table 1 lists the A1 and A0 bits and the selection of the updated DACs. The RNG bit controls the DAC output range. When RNG = low, the output range is between the applied reference voltage and GND, and when RNG = high, the range is between twice the applied reference voltage and GND.

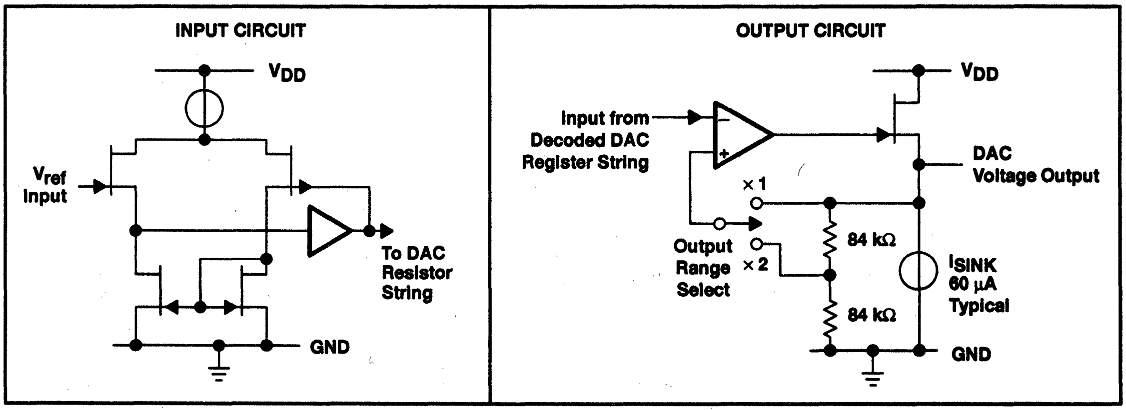
Table 1. Serial-Input Decode

A2	A1	A0	DAC UPDATED
0	0	0	DACA
0	0	1	DACB
0	1	0	DACC
0	1	1	DACD
1	0	0	DACE
1	0	1	DACF
1	1	0	DACG
1	1	1	DACH

Table 2. Ideal-Output Transfer

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	(1/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	(127/256) × REF (1+RNG)
1	0	0	0	0	0	0	0	(128/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	(255/256) × REF (1+RNG)

equivalent of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} – GND) .... 7 V
Digital input voltage range, V_{ID} .... GND – 0.3 V to V_{DD} + 0.3 V
Reference input voltage range .... GND – 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A: TLC5628C .... 0°C to 70°C
TLC5628I .... –40°C to 85°C
Storage temperature range, T_{stg} .... –50°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 230°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.75	5.25	V
High-level digital input voltage, V_{IH}		0.8 V_{DD}		V
Low-level digital input voltage, V_{IL}			0.8	V
Reference voltage, V_{ref} [A|B|C|D|E|F|G|H]			V_{DD} – 1.5	V
Load resistance, R_L		10		kΩ
Setup time, data input, $t_{su(DATA-CLK)}$ (see Figures 1 and 2)		50		ns
Valid time, data input valid after CLK↓, $t_{v(DATA-CLK)}$ (see Figures 1 and 2)		50		ns
Setup time, CLK 11th falling edge to LOAD, $t_{su(CLK-LOAD)}$ (see Figure 1)		50		ns
Setup time, LOAD↑ to CLK↓, $t_{su(LOAD-CLK)}$ (see Figure 1)		50		ns
Pulse duration, LOAD, $t_{w(LOAD)}$ (see Figure 1)		250		ns
Pulse duration, LDAC, $t_{w(LDAC)}$ (see Figure 2)		250		ns
Setup time, LOAD↑ to LDAC↓, $t_{su(LOAD-LDAC)}$ (see Figure 2)		0		ns
CLK frequency			1	MHz
Operating free-air temperature, T_A	TLC5628C	0	70	°C
	TLC5628I	–40	85	°C

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V ± 5%, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current	$V_I = V_{DD}$			±10	μA
I_{IL}	Low-level digital input current	V_I = 0 V			±10	μA
$I_{O(sink)}$	Output sink current	Each DAC output	20			μA
$I_{O(source)}$	Output source current	Each DAC output	2			mA
C_i	Input capacitance			15		pF
C_i	Reference input capacitance			15		pF
I_{DD}	Supply current	V_{DD} = 5 V			4	mA
I_{ref}	Reference input current	V_{DD} = 5 V, V_{ref} = 2 V			±10	μA
E_L	Linearity error (end point corrected)	V_{ref} = 2 V, × 2 gain (see Note 1)			±1	LSB
E_D	Differential-linearity error	V_{ref} = 2 V, × 2 gain (see Note 2)			±0.9	LSB
E_{ZS}	Zero-scale error	V_{ref} = 2 V, × 2 gain (see Note 3)	0		30	mV
	Zero-scale error temperature coefficient	V_{ref} = 2 V, × 2 gain (see Note 4)		10		μV/°C
E_{FS}	Full-scale error	V_{ref} = 2 V, × 2 gain (see Note 5)			±60	mV
	Full-scale error temperature coefficient	V_{ref} = 2 V, × 2 gain (see Note 6)		±25		μV/°C
PSRR	Power-supply sensitivity	See Notes 7 and 8		0.5		mV/V

NOTES: 1. Integral nonlinearity (INL) is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full-scale errors).
2. Differential nonlinearity (DNL) is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
3. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
4. Zero-scale error temperature coefficient is given by: $ZSETC = [ZSE(T_{max}) - ZSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
5. Full-scale error is the deviation from the ideal full-scale output (V_{ref} – 1 LSB) with an output load of 10 kΩ.
6. Full-scale temperature coefficient is given by: $FSETC = [FSE(T_{max}) - FSE\ (T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
7. Zero-scale error rejection ratio (ZSE-RR) is measured by varying the V_{DD} voltage from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
8. Full-scale error rejection ratio (FSE-RR) is measured by varing the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage.

operating characteristics over recommended operating free-air temperature range, V_{DD} = 5 V ± 5%, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate	C_L = 100 pF, R_L = 10 kΩ		1		V/μs
Output settling time	To 0.5 LSB, C_L = 100 pF, R_L = 10 kΩ, See Note 9		10		μs
Large-signal bandwidth	Measured at –3 dB point		100		kHz
Digital crosstalk	CLK = 1-MHz square wave measured at DACA-DACD		–50		dB
Reference feedthrough	See Note 10		–60		dB
Channel-to-channel isolation	See Note 11		–60		dB
Reference input bandwidth	See Note 12		100		kHz

NOTES: 9. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 00 hex to FF hex or FF hex to 00 hex. For TLC5628C: V_{DD} = 5 V, V_{ref} = 2 V and range = ×2. For TLC5628I: V_{DD} = 3 V, V_{ref} = 1.25 V and range ×2.
10. Reference feedthrough is measured at any DAC output with an input code = 00 hex with a V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
11. Channel-to-channel isolation is measured by setting the input code of one DAC to FF hex and the code of all other DACs to 00 hex with V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
12. Reference bandwidth is the –3 dB bandwidth with an input at V_{ref} = 1.25 V dc + 2 V_{pp}, with a digital input code of full-scale.

PARAMETER MEASUREMENT INFORMATION

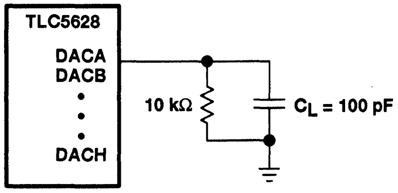


Figure 3. Slewing Settling Time and Linearity Measurements

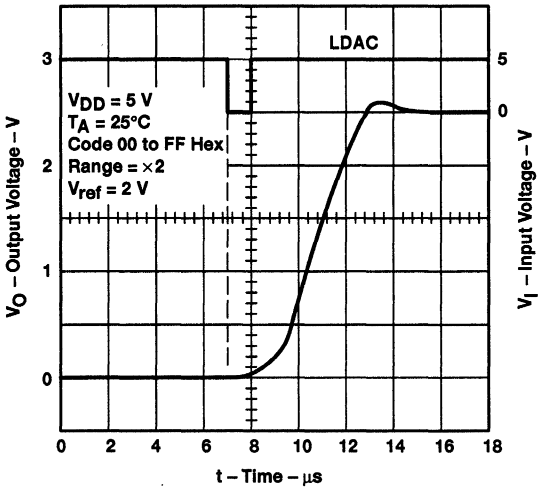


Figure 4. Positive Rise and Setting Time V_{DD} = 5 V

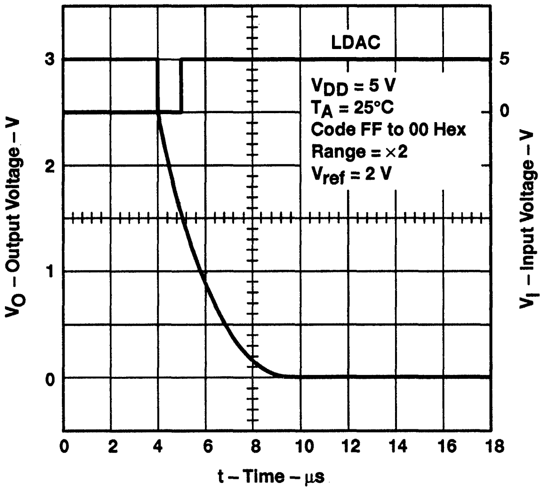


Figure 5. Negative Fall and Setting Time V_{DD} = 5 V

TYPICAL CHARATERISTICS

OUTPUT SOURCE CURRENT
vs
OUTPUT VOLTAGE

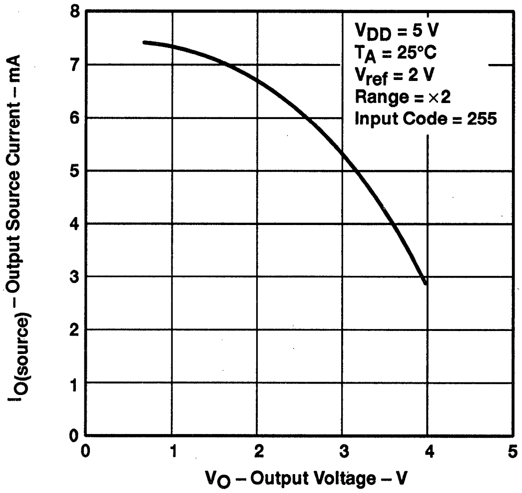


Figure 6

SUPPLY CURRENT
vs
TEMPERATURE

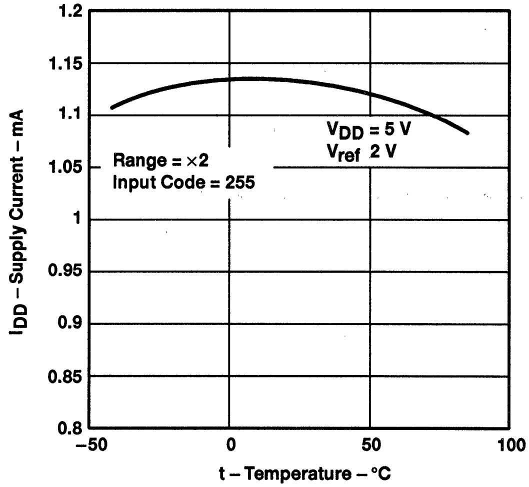


Figure 7

RELATIVE GAIN
vs
FREQUENCY

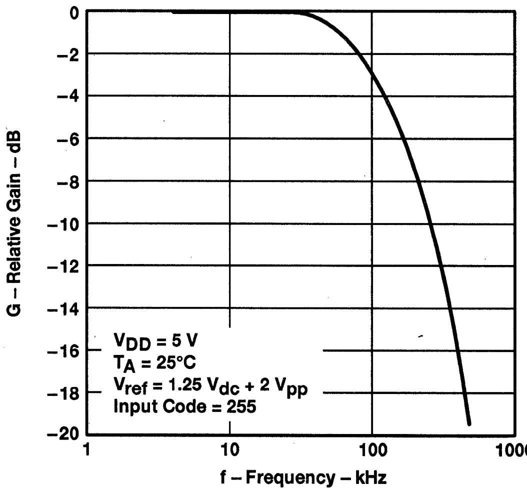


Figure 8

RELATIVE GAIN
vs
FREQUENCY

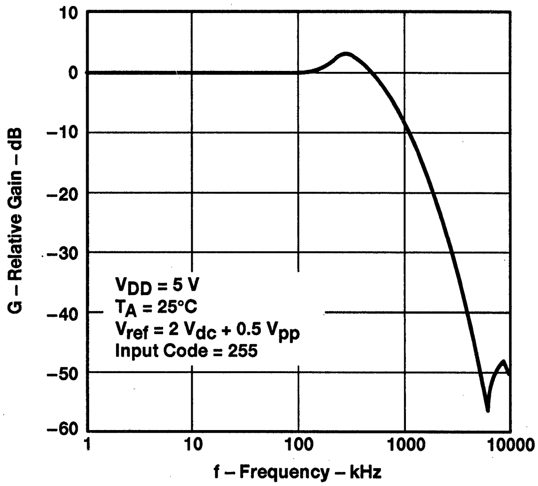
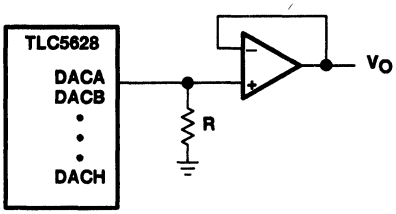


Figure 9

APPLICATION INFORMATION



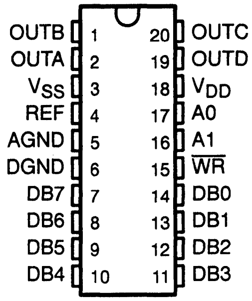
NOTE A: Resistor R ≥ 10 kΩ

Figure 10. Output Buffering Schemes

features

- Four 8-Bit D/A Converters
- Microprocessor Compatible
- TTL/CMOS Compatible
- No User Trim Required
- Single Supply Operation Possible
- Simultaneous Update Facility
- CMOS Technology

DW OR N PACKAGE
(TOP VIEW)



applications

- Process Control
- Automatic Test Equipment
- Automatic Calibration of Large System Parameters e.g., Gain/Offset

description

The TLC7226C and TLC7226I consist of four, 8-bit, voltage-output, digital-to-analog converters with output buffer amplifiers and interface logic on a single monolithic chip. No external trims are required to achieve full specified performance for the part.

Separate on-chip latches are provided for each of the four D/A converters. Data is transferred into one of these data latches through a common, 8-bit, TTL/CMOS-compatible (5 V) input port. Control inputs A0 and A1 determine which D/A converter is loaded when WR goes low. The control logic is speed compatible with most 8-bit microprocessors. Since all four D/A converters are fabricated on the same chip at the same time, precise matching and tracking between them is inherent.

Each D/A converter includes an output buffer amplifier capable of sourcing up to 5 mA of output current.

The TLC7226 performance is specified for input reference voltages from 2 V to 12.5 V with dual supplies. The voltage mode configuration of the D/A converters allow the TLC7226 to be operated from a single power supply rail at a reference of 10 V.

The TLC7226 is fabricated in a LinBiCMOS™ process that has been specifically developed to allow high-speed digital logic circuits and precision analog circuits to be integrated on the same chip. The TLC7226 has a common 8-bit data bus with individual D/A converter latches. This provides a versatile control architecture for simple interface to microprocessors. All latch-enable signals are level triggered.

Combining four D/A converters, four operational amplifiers, and interface logic into either a 0.3-inch wide, 20-pin DIP or a small 20-pin small-outline IC (SOIC) allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. The pinout is aimed at optimizing board layout with all of the analog inputs and outputs at one end of the package and all of the digital inputs at the other.

The TLC7226C is characterized for operation from 0°C to 70°C. The TLC7226I is characterized for operation from –25°C to 85°C.

PRODUCT PREVIEW

AVAILABLE OPTIONS

T_A	PACKAGE	
	SMALL OUTLINE (DW)	PLASTIC DIP (N)
0°C to 70°C	TLC7226CDW	TLC7226CN
–25°C to 85°C	TLC7226IDW	TLC7226IN

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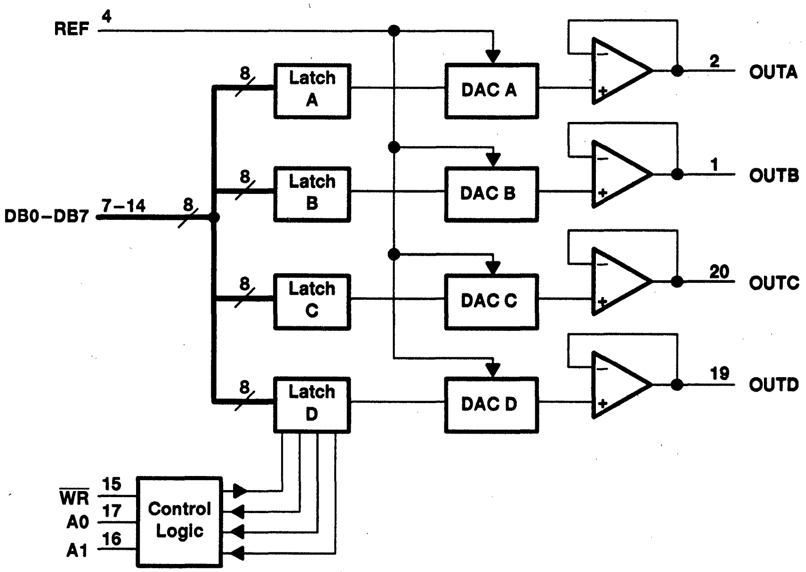
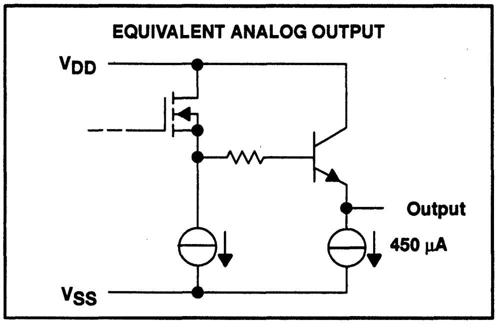
functional block diagram



schematic of outputs



PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	NO.†	I/O	DESCRIPTION
AGND	5		Analog ground
A0, A1	16, 17	I	DAC select inputs
DGND	6		Digital ground
DB0–DB7	7–14	I	Digital DAC data inputs
OUTA	2	O	DACA output
OUTB	1	O	DACB output
OUTC	20	O	DACC output
OUTD	19	O	DACD output
REF	4	I	Voltage reference input
V_{DD}	18		Positive supply voltage
V_{SS}	3		Negative supply voltage
$\overline{WR}$	15	I	Write input selects DAC transparency or latch mode. The selected input latch is transparent when $\overline{WR}$ is low.

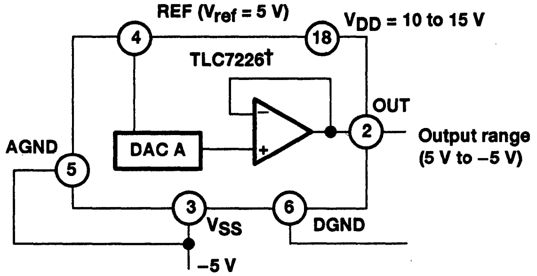
† Terminal numbers shown are for the DW and N packages.

PRODUCT PREVIEW

detailed description

AGND bias for direct bipolar output operation

The TLC7226 can be used in bipolar operation without adding more external operational amplifiers as shown in Figure 1 by biasing AGND to V_{SS}. This configuration provides an excellent method for providing a direct bipolar output with no additional components. The transfer values are shown in Table 1.



† Digital inputs omitted for clarity.

Figure 1. AGND Bias for Direct Bipolar Operation

AGND bias for direct bipolar output operation (continued)

Table 1. Bipolar (Offset Binary) Code

DAC LATCH CONTENTS MSB	LSB	ANALOG OUTPUT
1111	1111	$+V_{ref}\left(\frac{127}{128}\right)$
1000	0001	$+V_{ref}\left(\frac{1}{128}\right)$
1000	0000	0 V
0111	1111	$-V_{ref}\left(\frac{1}{128}\right)$
0000	0001	$-V_{ref}\left(\frac{127}{128}\right)$
0000	0000	$-V_{ref}\left(\frac{128}{128}\right) = -V_{ref}$

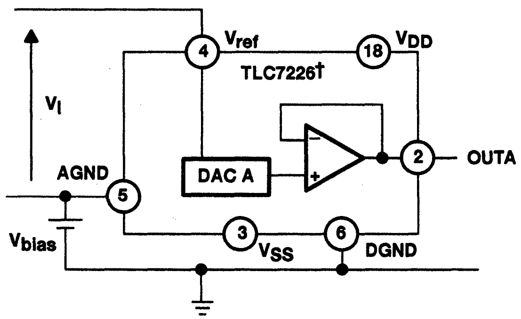
AGND bias for positive output offset

The TLC7226 AGND terminal can be biased above or below the system ground terminal, DGND, to provide an offset zero analog output voltage level. Figure 2 shows a circuit configuration to achieve this for channel A of the TLC7226. The output voltage, V_O, at OUTA can be expressed as:

$$V_O = V_{BIAS} + D_A\left(V_I\right)$$

Where D_A is a fractional representation of the digital input word ($0 \le D \le 255/256$).

Increasing AGND above system GND reduces the output range. $V_{DD} - V_{ref}$ must be at least 4 V to ensure specified operation. Because the AGND terminal is common to all four DACs, this method biases up the output voltages of all the DACs in the TLC7226. Supply voltages V_{DD} and V_{SS} for the TLC7226 should be referenced to DGND.



† Digital inputs omitted for clarity.

Figure 2. AGND Bias Circuit

PRODUCT PREVIEW

bipolar output operation using external amplifier

Each of the DACs of the TLC7226 can also be individually configured to provide bipolar output operation, using an external amplifier and two resistors per channel. Figure 3 shows a circuit used to implement offset binary coding (bipolar operation) with DAC A of the TLC7226. In this case:

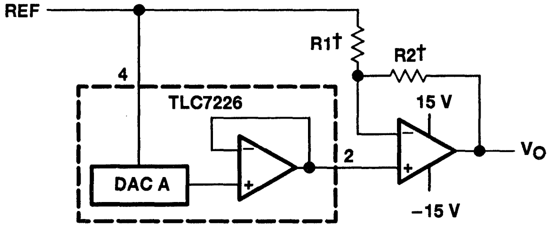
$$V_O = 1 + \frac{R2}{R1} \times \left(D_A \times V_{ref}\right) - \frac{R2}{R1} \times \left(V_{ref}\right)$$

With R1 = R2

$$V_O = \left(2D_A - 1\right) \times V_{ref}$$

Where D_A is a fractional representation of the digital word in latch A.

Mismatch between R1 and R2 causes gain and offset errors. Therefore, these resistors must match and track over temperature. The TLC7226 can be operated with a single supply or from positive and negative supplies.



† R1 = R2 = 10 kΩ ±0.1%

Figure 3. Bipolar Output Circuit

staircase window comparator

In many test systems, it is important to be able to determine whether some parameter lies within defined limits. The staircase window comparator shown in Figure 4 is a circuit that can be used, to measure the V_{OH} and V_{OL} thresholds of a TTL device under test. Upper and lower limits on both V_{OH} and V_{OL} can be programmed using the TLC7226. Each adjacent pair of comparators forms a window of programmable size (see Figure 5). When the test voltage (V_{test}) lines horizonal within a window, then the output for that window is higher. With a reference of 2.56 V applied to the REF input, the minimum window size is 10 mV.

PRODUCT PREVIEW

PRODUCT PREVIEW

staircase window comparator (continued)

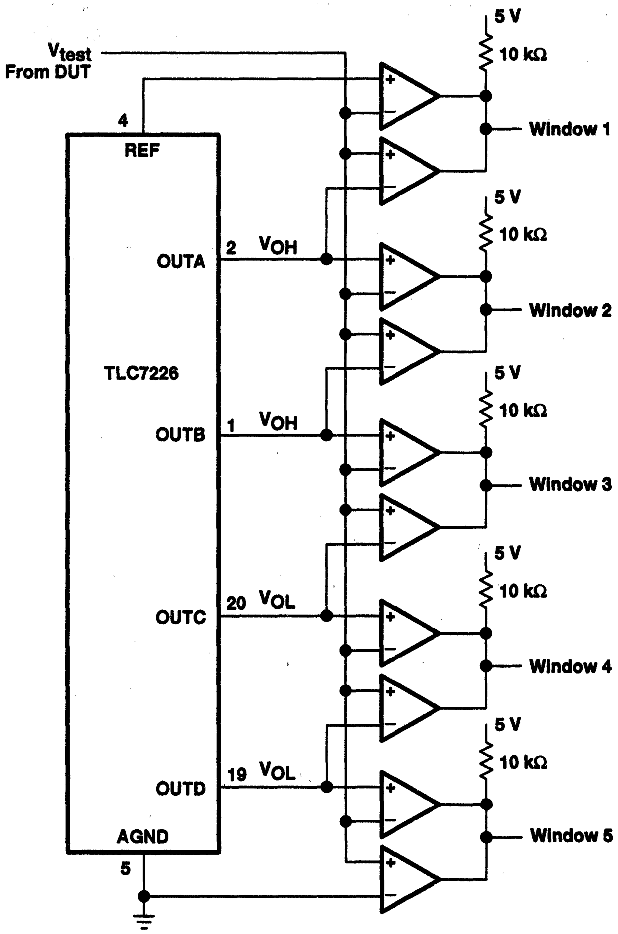


Figure 4. Logic Level Measurement

staircase window comparator (continued)

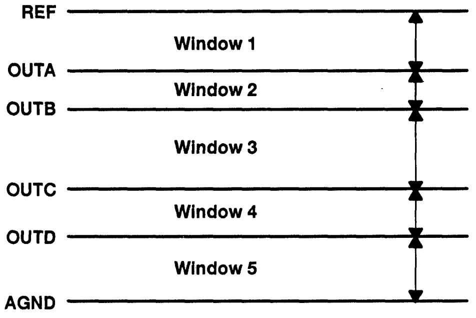


Figure 5. Window Structure

The circuit can easily be adapted to allow for overlapping of windows as shown in Figure 6. When the three outputs from this circuit are decoded, five different nonoverlapping programmable windows can again be defined (see Figure 7).

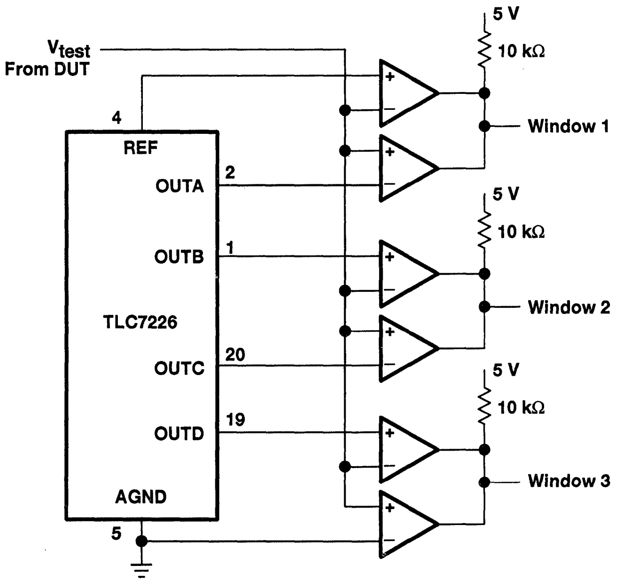


Figure 6. Overlapping Windows

PRODUCT PREVIEW

staircase window comparator (continued)

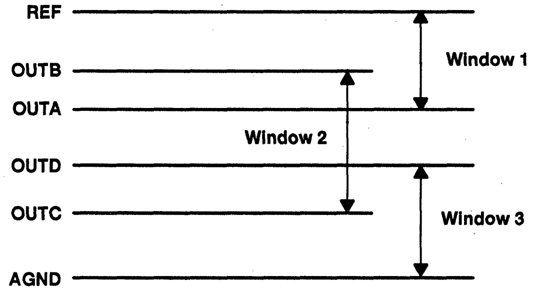


Figure 7. Window Structure

output buffer amplifier

The unity-gain output amplifier is capable of sourcing 5 mA into a 2-kΩ load and can drive a 3300-pF capacitor. The output can be shorted to AGND indefinitely or can be shorted to any voltage between V_{SS} and V_{DD} consistent with the maximum device power dissipation.

multiplying DAC

The TLC7226 can be used as a multiplying DAC if the reference signal is maintained between 2 V and V_{DD} −4 V. When this configuration is used, V_{DD} should be 14.25 V to 15.75 V. A low output impedance buffer should be used so that the input signal is not loaded by the resistor ladder. Figure 8 shows the general schematic.

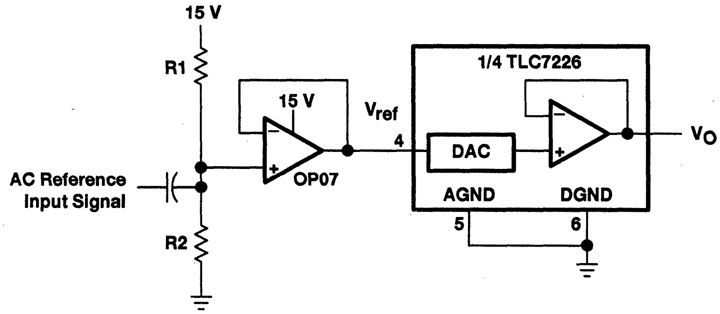


Figure 8. AC Signal Input Scheme

interface logic information

Address lines A0 and A1 select which D/A converter accepts data from the input port. The following function table shows the selection table for the four DACs. Figure 9 shows the input control logic. When the $\overline{WR}$ signal is low, the input latches of the selected DAC are transparent and the output responds to activity on the data bus. The data is latched into the addressed DAC latch on the rising edge of $\overline{WR}$. While $\overline{WR}$ is high, the analog outputs remain at the value corresponding to the data held in their respective latches.

FUNCTION TABLE

CONTROL INPUTS			OPERATION
$\overline{WR}$	A1	A2	
H	X	X	No operation Device not selected
L	L	L	DAC A transparent
↑	L	L	DAC A latched
L	L	H	DAC B transparent
↑	L	H	DAC B latched
L	H	L	DAC C transparent
↑	H	L	DAC C latched
L	H	H	DAC D transparent
↑	H	H	DAC D latched

L = low, H = high, X = irrelevant

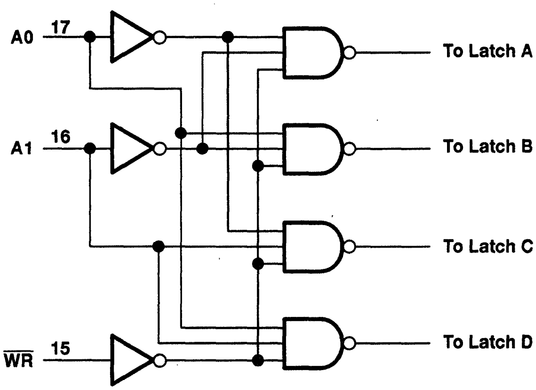


Figure 9. Input Control Logic

PRODUCT PREVIEW

unipolar output operation

The unipolar output operation is the basic mode of operation for each channel of the TLC7226, with the output voltages having the same positive polarity as V_{ref}. The TLC7226 can be operated with a single supply (V_{SS} = AGND) or with positive/negative supplies. The voltage at V_{ref} must never be negative with respect to AGND to prevent parasitic transistor turn-on. Connections for the unipolar output operation are shown in Figure 10. Transfer values are shown in Table 2.

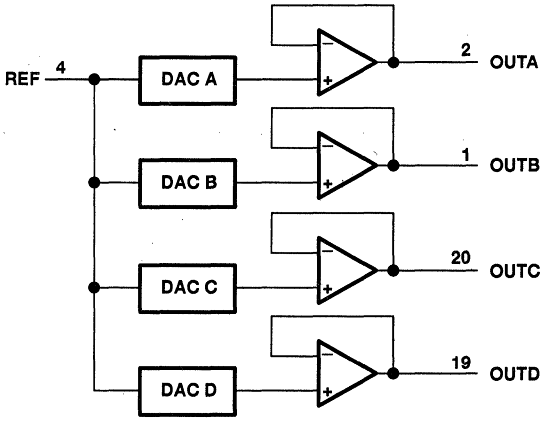


Figure 10. Unipolar Output Circuit

Table 2. Unipolar Code

DAC LATCH CONTENTS MSB	LSB	ANALOG OUTPUT
1111	1111	$+V_{ref}\left(\frac{255}{256}\right)$
1000	0001	$+V_{ref}\left(\frac{129}{256}\right)$
1000	0000	$+V_{ref}\left(\frac{128}{256}\right) = +\frac{V_{ref}}{2}$
0111	1111	$+V_{ref}\left(\frac{127}{256}\right)$
0000	0001	$+V_{ref}\left(\frac{1}{256}\right)$
0000	0000	0 V

NOTE: $1\text{ LSB} = \left(V_{ref}\,2^{-8}\right) = V_{ref}\left(\frac{1}{256}\right)$

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD}: to AGND or DGND .... −0.3 V to 17 V
to V_{SS}‡ .... −0.3 V to 24 V
Supply voltage range, V_{SS}: to AGND or DGND .... −17 V to + 0.3 V
Voltage range between AGND and DGND .... −17 V to 17 V
Input voltage range, V_I (to DGND) .... −0.3 V to V_{DD} + 0.3 V
Reference voltage range: V_{ref} (to AGND) .... −0.3 V to V_{DD}
V_{ref} (to V_{SS}) .... −0.3 V to 20 V
Output voltage range, V_O (to AGND) (see Note 1) .... V_{SS} to V_{DD}
Continuous total power dissipation at (or below) T_A = 25°C (see Note 2) .... 500 mW
Operating free-air temperature range, T_A: C suffix .... 0°C to 70°C
I suffix .... −25°C to 85°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N packages .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ The V_{SS} terminal is connected to the substrate and must be tied to the most negative supply voltage applied to the device.

NOTES: 1. Output voltages may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typically short circuit current to AGND is 60 mA.
2. For operation above T_A = 75°C derate linearly at the rate of 2.0 mC/°C.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	16.5	V
Supply voltage, V_{SS}		−0.6	−5.5	V
High-level input voltage, V_{IH}	V_{DD} = 4.75 V	2		V
	V_{DD} = 15.75 V	2		
Low-level input voltage, V_{IL}	V_{DD} = 4.75 V		0.8	V
Reference voltage, V_{ref}		0	V_{DD}−4	V
Load resistance, R_L		2		kΩ
Setup time, address valid before $\overline{WR}$, $t_{su(AW)}$		0		ns
Setup time, data valid before $\overline{WR}$, $t_{su(DW)}$	V_{DD} = 4.75 V to 5.25 V	70		ns
	V_{DD} = 4.75 V to 5.25 V	180		
Hold time, address valid before $\overline{WR}$, $t_{h(AW)}$	V_{DD} = 4.75 V to 5.25 V	10		ns
	V_{DD} = 4.75 V to 5.25 V	20		
Hold time, data valid before $\overline{WR}$, $t_{h(DW)}$	V_{DD} = 4.75 V to 5.25 V	0		ns
	V_{DD} = 4.75 V to 5.25 V	20		
Pulse duration, $\overline{WR}$ low, t_w	V_{DD} = 4.75 V to 5.25 V	50		ns
	V_{DD} = 4.75 V to 5.25 V	180		
Operating free-air temperature, T_A	C suffix	0	70	°C
	I suffix	−25	85	°C

PRODUCT PREVIEW

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range

dual power supply over recommended supply and reference voltage ranges, AGND = DGND = 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Input current, digital		V_I = 0 V or V_{DD}			±1	µA
I_{DD}	Supply current		$V_I = V_{IL}$ or V_{IH}, No load		6	12	mA
I_{SS}	Supply current		$V_I = V_{IL}$ or V_{IH}, No load		4	10	mA
$r_{i(ref)}$	Reference input resistance			2	4		kΩ
	Power supply sensitivity		ΔV_{DD} = ±5%			0.01	%/%
C_i	Input capacitance	REF input	All 0's loaded	65			pF
			All 1's loaded			300	
		Digital inputs				8	

single power supply, V_{DD} = 14.25 V to 15.75 V, V_{SS} = AGND = DGND = 0 V, V_{ref} = 10 V

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
I_I	Input current, digital		V_I = 0 V or V_{DD}		±1	µA
I_{DD}	Supply current		$V_I = V_{IL}$ or V_{IH}, No load		13	mA
	Power supply sensitivity		ΔV_{DD} = ±5%		0.01	%/%
C_i	Input capacitance	REF input	All 0's loaded	65		pF
			All 1's loaded		300	
		Digital inputs			8	

single or dual power supplies, V_{DD} = 4.75 V to 5.25 V, V_{SS} = AGND = DGND = 0 V or V_{SS} = –5 V, V_{ref} = 1.25 V

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
I_I	Input current, digital		V_I = 0 V or V_{DD}		±1	µA
I_{DD}	Supply current		$V_I = V_{IL}$ or V_{IH}, No load		12	mA
r_i	Input resistance			2		kΩ
	Power supply sensitivity		ΔV_{DD} = ±5%		0.01	%/%
C_i	Input capacitance	REF input	All 0's loaded	65		pF
			All 1's loaded		300	
		Digital inputs			8	

operating characteristics over recommended operating free-air temperature range

dual power supply over recommended supply and reference voltage ranges, AGND = DGND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Slew rate			2.5			V•µs
Settling time to 1/2 LSB	Positive full scale	V_{ref} = 10 V			5	µs
	Negative full scale				7	
Resolution				8		Bits
Total unadjusted error		V_{DD} = 15 V ±5%, V_{ref} = 10 V			±2	LSB
Linearity error	Differential/integral				±1	LSB
Full-scale error					±1.5	LSB
Temperature coefficient of gain	Full scale	V_{DD} = 14 V to 16.5 V, V_{ref} = 10 V		±20		ppm/°C
	Zero-code error			±50		µV/°C
Zero-code error					±30	mV
Digital crosstalk glitch impulse area		V_{ref} = 0 V		50		nV•s

single power supply, V_{DD} = 14.25 V to 15.75 V, V_{SS} = AGND = DGND = 0 V, V_{ref} = 10 V (unless otherwise noted)

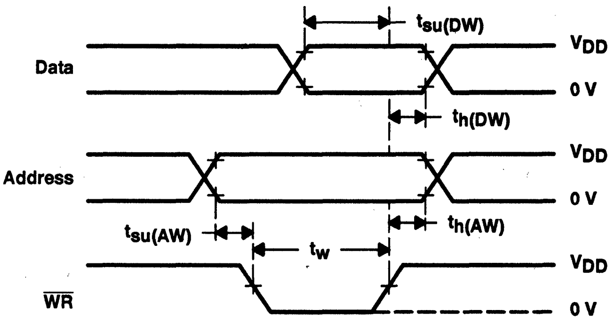
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Slew rate			2			V•µs
Settling time to 1/2 LSB	Positive full scale				5	µs
	Negative full scale				20	
Resolution				8		Bits
Total unadjusted error					±2	LSB
Full-scale error					±1.5	LSB
Temperature coefficient of gain	Full scale	V_{DD} = 14 V to 16.5 V, V_{ref} = 10 V		±20		ppm/°C
	Zero-code error			±50		µV/°C
Linearity error	Differential				±1	LSB
Digital crosstalk glitch impulse area				50		nV•s

single or dual power supplies, V_{DD} = 4.75 V to 5.25 V, V_{SS} = AGND = DGND or V_{SS} = –5 V, V_{ref} = 1.25 V (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
Linearity error	Differential		±1	LSB
Full-scale error			±4	LSB
Zero-code error			±30	mV

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. $t_r = t_f = 20$ ns over V_{DD} range.
B. The timing measurement reference level is equal to $V_{IH} + V_{IL}$ divided by 2.
C. The selected input latch is transparent while $\overline{WR}$ is low. Invalid data during this time can cause erroneous outputs.

Figure 11. Write-Cycle Voltage Waveforms

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

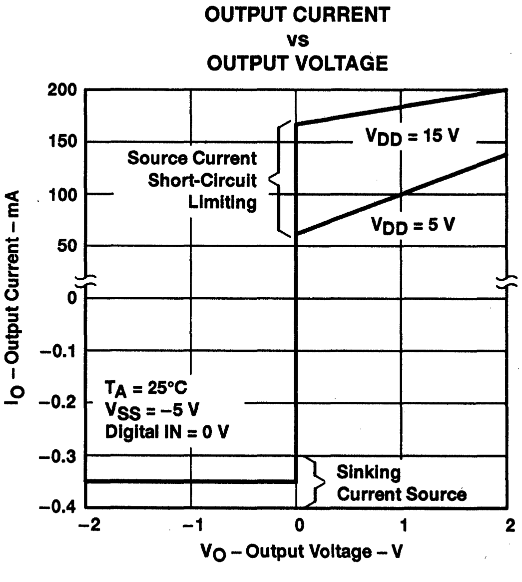


Figure 12

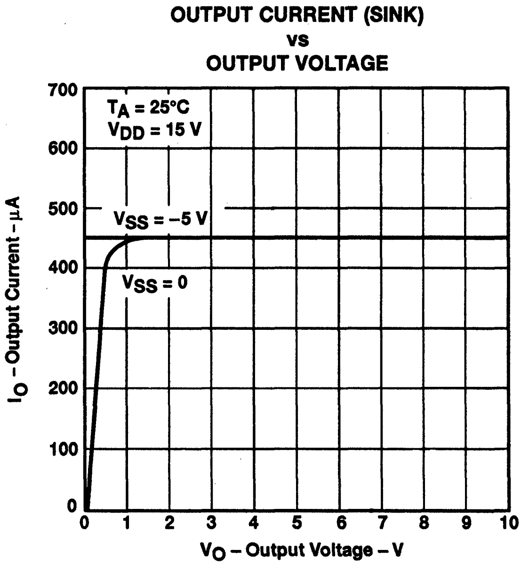
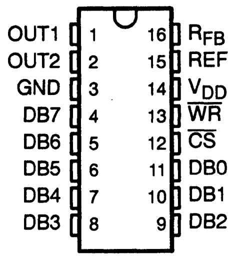


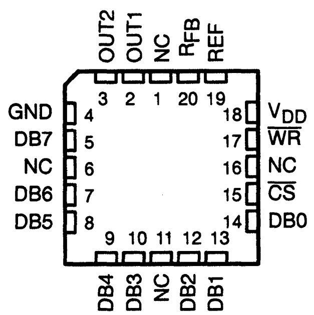
Figure 13

- **Easily Interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Monotonic Over the Entire A/D Conversion Range**
- **Segmented High-Order Bits Ensure Low-Glitch Output**
- **Interchangeable With Analog Devices AD7524, PMI PM-7524, and Micro Power Systems MP7524**
- **Fast Control Signaling for Digital Signal-Processor Applications Including Interface With TMS320**
- **CMOS Technology**

D OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC–No internal connection

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 Bits
Linearity error	1/2 LSB Max
Power dissipation at V_{DD} = 5 V	5 mW Max
Setting time	100 ns Max
Propagation delay time	80 ns Max

description

The TLC7524C, TLC7524E, and TLC7524I are CMOS, 8-bit, digital-to-analog converters (DACs) designed for easy interface to most popular microprocessors.

The devices are 8-bit, multiplying DACs with input latches and load cycles similar to the write cycles of a random access memory. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, which produce the highest glitch impulse. The devices provide accuracy to 1/2 LSB without the need for thin-film resistors or laser trimming, while dissipating less than 5 mW typically.

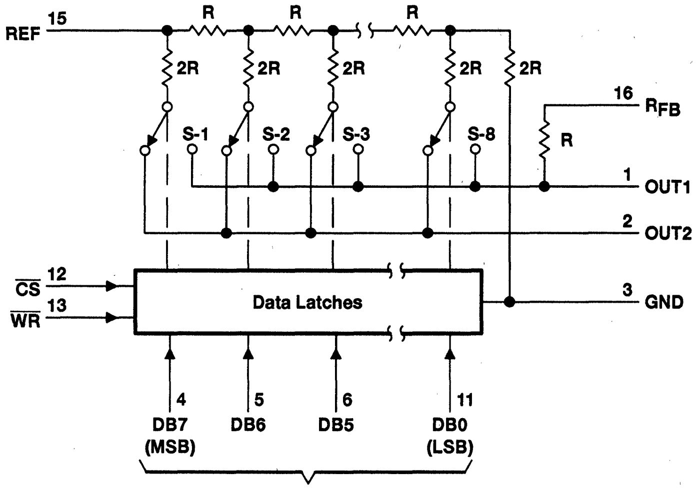
Featuring operation from a 5-V to 15-V single supply, these devices interface easily to most microprocessor buses or output ports. The 2- or 4-quadrant multiplying makes these devices an ideal choice for many microprocessor-controlled gain-setting and signal-control applications.

The TLC7524C is characterized for operation from 0°C to 70°C. The TLC7524I is characterized for operation from −25°C to 85°C. The TLC7524E is characterized for operation from −40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGE		
	SMALL OUTLINE PLASTIC DIP (D)	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	TLC7524CD	TLC7524CFN	TLC7524CN
−25°C to 85°C	TLC7524ID	TLC7524IFN	TLC7524IN
−40°C to 85°C	TLC7524ED	TLC7524EFN	TLC7524EN

functional block diagram



Terminal numbers shown are for the D or N package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{DD}		−0.3 V to 16.5 V
Digital input voltage range, V_I		−0.3 V to V_{DD} + 0.3 V
Reference voltage, V_{ref}		±25 V
Peak digital input current, I_I		10 μA
Operating free-air temperature range, T_A:	TLC7524C	0°C to 70°C
	TLC7524I	−25°C to 85°C
	TLC7524E	−40°C to 85°C
Storage temperature range, T_{stg}		−65°C to 150°C
Case temperature for 10 seconds, T_C: FN package		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260°C

recommended operating conditions

		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4.75	5	5.25	14.5	15	15.5	V
Reference voltage, V_{ref}			±10			±10		V
High-level input voltage, V_{IH}		2.4						V
Low-level input voltage, V_{IL}				0.8			1.5	V
CS setup time, $t_{su(CS)}$		40			40			ns
CS hold time $t_{h(CS)}$		0			0			ns
Data bus input setup time $t_{su(D)}$		25			25			ns
Data bus input hold time $t_{h(D)}$		10			10			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$		40			40			ns
Operating free-air temperature, T_A	TLC7524C	0		70	0		70	°C
	TLC7524I	−25		85	−25		85	
	TLC7524E	−40		85	−40		85	

electrical characteristics over recommended operating free-air temperature range, V_{ref} = ±10 V, OUT1 and OUT2 at GND (unless otherwise noted)

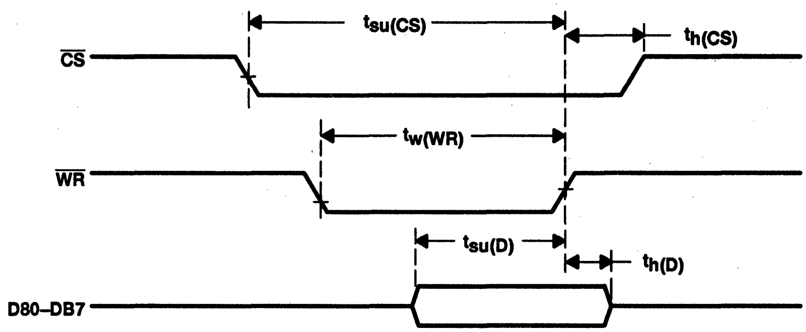
PARAMETER			TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{IH}	High-level input current		$V_I = V_{DD}$			10			10	µA
I_{IL}	Low-level input current		V_I = 0			−10			−10	µA
I_{lkg}	Output leakage current	OUT1	DB0–DB7 at 0 V, $\overline{WR}$, $\overline{CS}$ at 0 V, V_{ref} = ±10 V			±400			±200	nA
		OUT2	DB0–DB7 at V_{DD}, $\overline{WR}$, $\overline{CS}$ at 0 V, V_{ref} = ±10 V			±400			±200	
I_{DD}	Supply current	Quiescent	DB0–DB7 at V_{IH}min or V_{IL}max			1			2	mA
		Standby	DB0–DB7 at 0 V or V_{DD}			500			500	µA
k_{SVS}	Supply voltage sensitivity, Δgain/ΔV_{DD}		ΔV_{DD} = ±10%		0.01	0.16		0.005	0.04	%FSR/%
C_i	Input capacitance, DB0–DB7, $\overline{WR}$, $\overline{CS}$		V_I = 0			5			5	pF
C_o	Output capacitance	OUT1	DB0–DB7 at 0 V, $\overline{WR}$, $\overline{CS}$ at 0 V			30			30	pF
		OUT2				120			120	
		OUT1	DB0–DB7 at V_{DD}, $\overline{WR}$, $\overline{CS}$ at 0 V			120			120	
		OUT2				30			30	
	Reference input impedance (REF to GND)			5		20	5		20	kΩ

operating characteristics over recommended operating free-air temperature range, V_{ref} = ±10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 15 V MIN	V_{DD} = 15 V TYP†	V_{DD} = 15 V MAX	UNIT
Linearity error				±0.5			±0.5	LSB
Gain error	See Note 1			±2.5			±2.5	LSB
Settling time (to 1/2 LSB)	See Note 2			100			100	ns
Propagation delay from digital input to 90% of final analog output current	See Note 2			80			80	ns
Feedthrough at OUT1 or OUT2	Vref = ±10 V (100-kHz sinewave) $\overline{WR}$ and $\overline{CS}$ at 0 V, DB0–DB7 at 0 V			0.5			0.5	%FSR
Temperature coefficient of gain	T_A = 25°C to MAX		±0.004			±0.001		%FSR/°C

NOTES: 1. Gain error is measured using the internal feedback resistor. Nominal full scale range (FSR) = V_{ref} – 1 LSB.
2. OUT1 load = 100 Ω, C_{ext} = 13 pF, $\overline{WR}$ at 0 V, $\overline{CS}$ at 0 V, DB0–DB7 at 0 V to V_{DD} or V_{DD} to 0 V.

operating sequence



APPLICATION INFORMATION

voltage-mode operation

It is possible to operate the current-multiplying DAC in these devices in a voltage mode. In the voltage mode, a fixed voltage is placed on the current output terminal. The analog output voltage is then available at the reference voltage terminal. Figure 1 is an example of a current-multiplying DAC, which is operated in voltage mode.

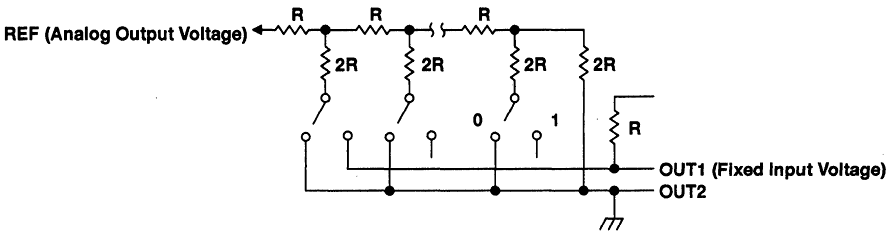


Figure 1. Voltage Mode Operation

The relationship between the fixed-input voltage and the analog-output voltage is given by the following equation:

$$V_O = V_I \, (D/256)$$

where

V_O = analog output voltage
V_I = fixed input voltage
D = digital input code converted to decimal

In voltage-mode operation, these devices meet the following specification:

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Linearity error at REF	V_{DD} = 5 V, OUT1 = 2.5 V, OUT2 at GND, T_A = 25°C		1	LSB

PRINCIPLES OF OPERATION

The TLC7524C, TLC7524E, and TLC7524I are 8-bit multiplying DACs consisting of an inverted R-2R ladder, analog switches, and data input latches. Binary-weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state. The high-order bits are decoded. These decoded bits, through a modification in the R-2R ladder, control three equally-weighted current sources. Most applications only require the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is seen in Figure 2. With all digital inputs low, the entire reference current, I_{ref}, is switched to OUT2. The current source I/256 represents the constant current flowing through the termination resistor of the R-2R ladder, while the current source I_{lkg} represents leakage currents to the substrate. The capacitances appearing at OUT1 and OUT2 are dependent upon the digital input code. With all digital inputs high, the off-state switch capacitance (30 pF maximum) appears at OUT2 and the on-state switch capacitance (120 pF maximum) appears at OUT1. With all digital inputs low, the situation is reversed as shown in Figure 2. Analysis of the circuit for all digital inputs high is similar to Figure 2; however, in this case, I_{ref} would be switched to OUT1.

The DAC on these devices interfaces to a microprocessor through the data bus and the $\overline{CS}$ and $\overline{WR}$ control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, analog output on these devices responds to the data activity on the DB0–DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0–DB7 inputs are latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

These devices are capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figures 3 and 4. Tables 1 and 2 summarize input coding for unipolar and bipolar operation respectively.

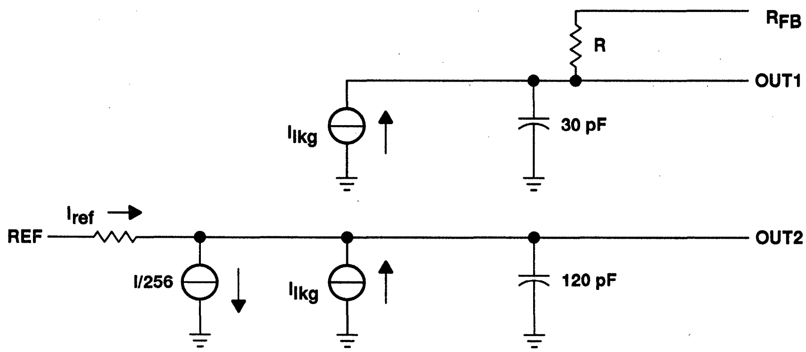


Figure 2. TLC7524 Equivalent Circuit With All Digital Inputs Low

PRINCIPLES OF OPERATION

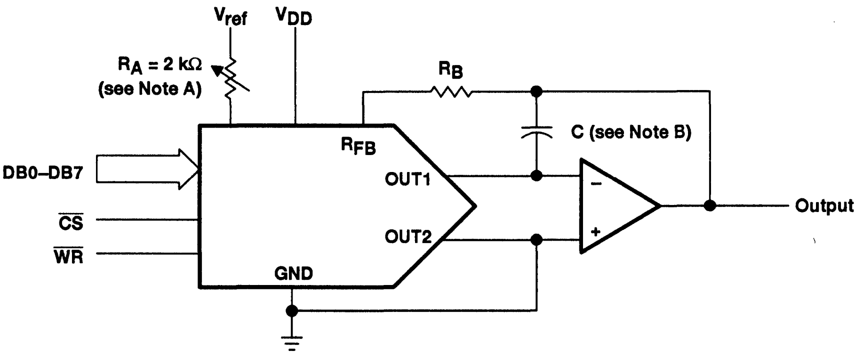


Figure 3. Unipolar Operation (2-Quadrant Multiplication)

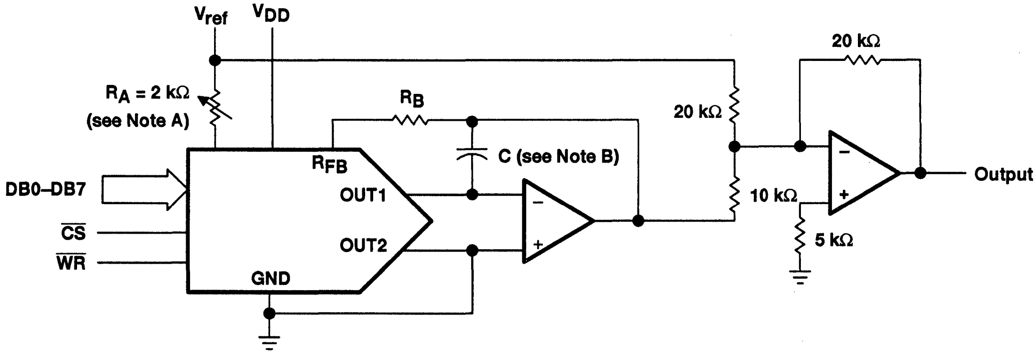


Figure 4. Bipolar Operation (4-Quadrant Operation)

NOTES: A. R_A and R_B used only if gain adjustment is required.
B. C phase compensation (10-15 pF) is required when using high-speed amplifiers to prevent ringing or oscillation.

Table 1. Unipolar Binary Code

DIGITAL INPUT (see Note 3) MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$-V_{ref}$ (255/256)
1 0 0 0 0 0 0 1	$-V_{ref}$ (129/256)
1 0 0 0 0 0 0 0	$-V_{ref}$ (128/256) = $-V_{ref}/2$
0 1 1 1 1 1 1 1	$-V_{ref}$ (127/256)
0 0 0 0 0 0 0 1	$-V_{ref}$ (1/256)
0 0 0 0 0 0 0 0	0

Table 2. Bipolar (Offset Binary) Code

DIGITAL INPUT (see Note 4) MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	V_{ref} (127/128)
1 0 0 0 0 0 0 1	V_{ref} (1/128)
1 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1	$-V_{ref}$ (1/128)
0 0 0 0 0 0 0 1	$-V_{ref}$ (127/128)
0 0 0 0 0 0 0 0	$-V_{ref}$

NOTES: 3. LSB = 1/256 (V_{ref})
4. LSB = 1/128 (V_{ref})

PRINCIPLES OF OPERATION

microprocessor interfaces

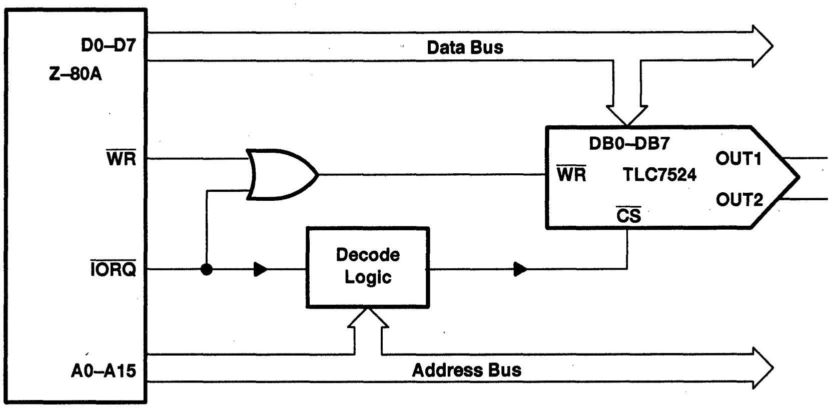


Figure 5. TLC7524 – Z-80A Interface

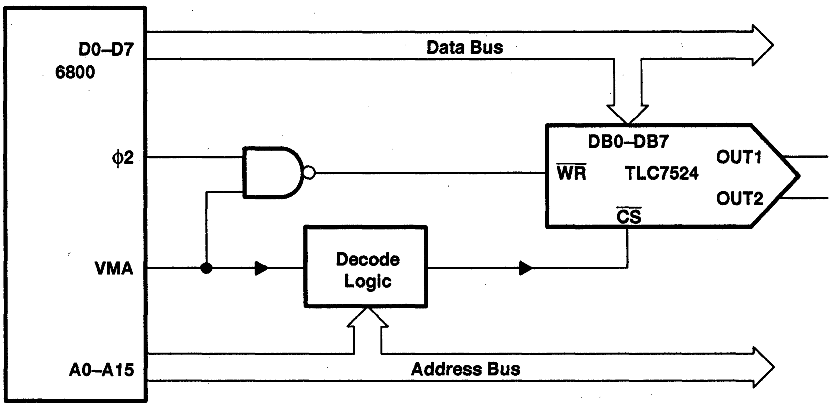


Figure 6. TLC7524 – 6800 Interface

microprocessor interfaces (continued)

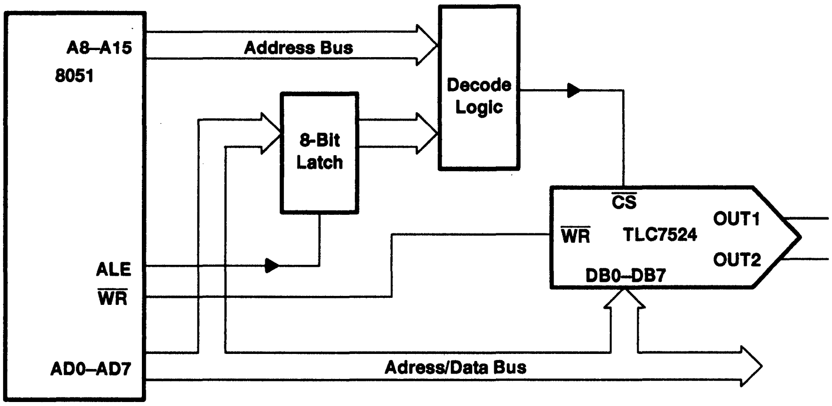
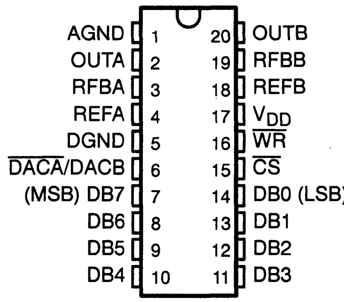


Figure 7. TLC7524 – 8051 Interface

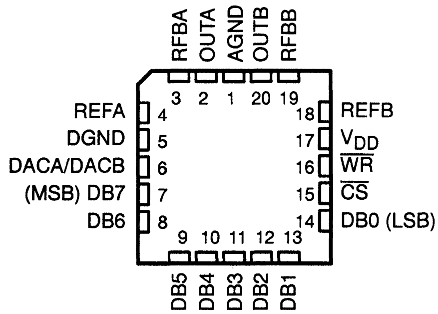
- **Easily Interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Monotonic Over the Entire A/D Conversion Range**
- **Interchangeable With Analog Devices AD7528 and PMI PM-7528**
- **Fast Control Signaling for Digital Signal Processor (DSP) Applications Including Interface With TMS320**
- **Voltage-Mode Operation**
- **CMOS Technology**

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 bits
Linearity Error	1/2 LSB
Power Dissipation at V_{DD} = 5 V	20 mW
Settling Time at V_{DD} = 5 V	100 ns
Propagation Delay Time at V_{DD} = 5 V	80 ns

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TLC7528C, TLC7528E, and TLC7528I are dual, 8-bit, digital-to-analog converters designed with separate on-chip data latches and feature exceptionally close DAC-to-DAC matching. Data is transferred to either of the two DAC data latches through a common, 8-bit, input port. Control input DACA/DACB determines which DAC is to be loaded. The load cycle of these devices is similar to the write cycle of a random-access memory, allowing easy interface to most popular microprocessor buses and output ports. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, where glitch impulse is typically the strongest.

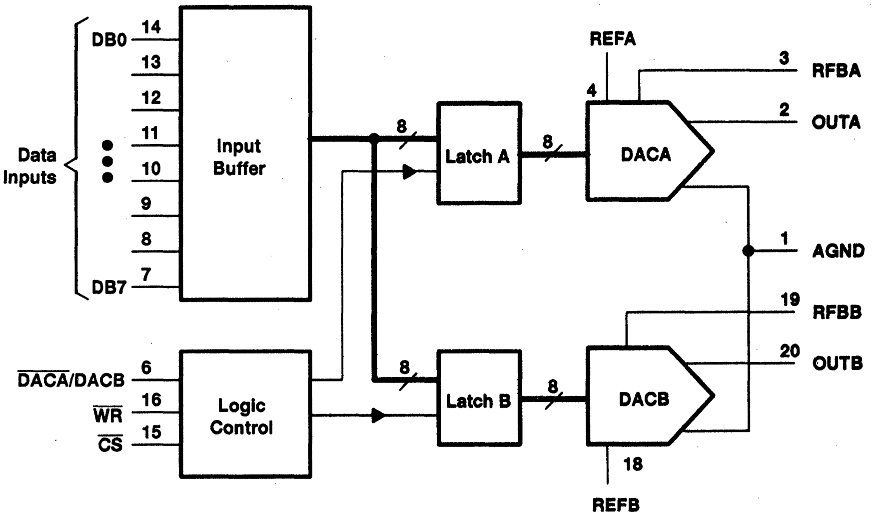
These devices operate from a 5-V to 15-V power supply and dissipates less than 15 mW (typical). The 2- or 4-quadrant multiplying makes these devices a sound choice for many microprocessor-controlled gain-setting and signal-control applications. It can be operated in voltage mode, which produces a voltage output rather than a current output. Refer to the typical application information in this data sheet.

The TLC7528C is characterized for operation from 0°C to 70°C. The TLC7528I is characterized for operation from −25°C to 85°C. The TLC7528E is characterized for operation from −40°C to 85°C.

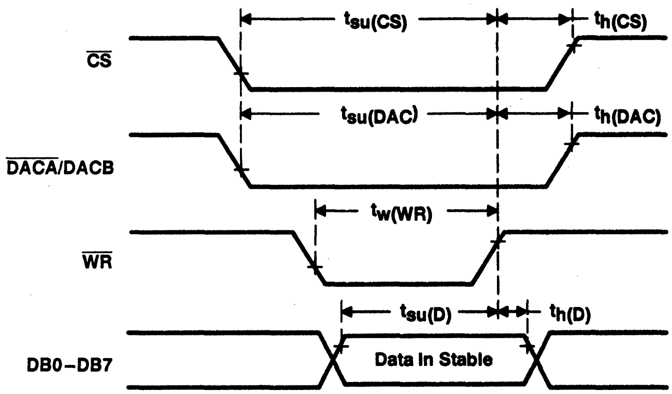
AVAILABLE OPTIONS

T_A	PACKAGE		
	SMALL OUTLINE (DW)	CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	TLC7528CDW	TLC7528CFN	TLC7528CN
−25°C to 85°C	TLC7528IDW	TLC7528IFN	TLC7528IN
−40°C to 85°C	TLC7528EDW	TLC7528EFN	TLC7528EN

functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (to AGND or DGND) .... −0.3 V to 16.5 V
Voltage between AGND and DGND .... $\pm V_{DD}$
Input voltage range, V_I (to DGND) .... −0.3 V to V_{DD} + 0.3
Reference voltage, V_{refA} or V_{refB} (to AGND) .... ±25 V
Feedback voltage V_{RFBA} or V_{RFBB} (to AGND) .... ±25 V
Output voltage, V_{OA} or V_{OB} (to AGND) .... ±25 V
Peak input current .... 10 μA
Operating free-air temperature range, T_A: TLC7528C .... 0°C to 70°C
TLC7528I .... −25°C to 85°C
TLC7528E .... −40°C to 85°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Case temperature for 10 seconds, T_C: FN package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		V_{DD} = 4.75 V to 5.25 V			V_{DD} = 14.5 V to 15.5 V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Reference voltage, V_{refA} or V_{refB}			±10			±10		V
High-level input voltage, V_{IH}		2.4			13.5			V
Low-level input voltage, V_{IL}				0.8			1.5	V
$\overline{CS}$ setup time, $t_{su(CS)}$		50			50			ns
$\overline{CS}$ hold time, $t_{h(CS)}$		0			0			ns
DAC select setup time, $t_{su(DAC)}$		50			50			ns
DAC select hold time, $t_{h(DAC)}$		10			10			ns
Data bus input setup time $t_{su(D)}$		25			25			ns
Data bus input hold time $t_{h(D)}$		10			10			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$		50			50			ns
Operating free-air temperature, T_A	TLC7628C	0		70	0		70	°C
	TLC7628I	−25		85	−25		85	
	TLC7628E	−40		85	−40		85	

electrical characteristics over recommended operating free-air temperature range, $V_{refA} = V_{refB} = 10$ V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	$V_{DD} = 5$ V MIN	$V_{DD} = 5$ V TYP†	$V_{DD} = 5$ V MAX	$V_{DD} = 15$ V MIN	$V_{DD} = 15$ V TYP†	$V_{DD} = 15$ V MAX	UNIT
I_{IH}	High-level input current		$V_I = V_{DD}$			10			10	µA
I_{IL}	Low-level input current		$V_I = 0$	5	12	−10	5	12	−10	µA
	Reference input impedance REFA or REFB to AGND					20			20	kΩ
I_{lkg}	Output Leakage Current	OUTA	DAC data latch loaded with 00000000, $V_{refA} = \pm 10$ V			±400			±200	nA
		OUTB	DAC data latch loaded with 00000000, $V_{refB} = \pm 10$ V			±400			±200	
	Input resistance match (REFA to REFB)					±1%			±1%	
	DC supply sensitivity, $\Delta gain/\Delta V_{DD}$		$\Delta V_{DD} = \pm 10\%$			0.04			0.02	%/%
I_{DD}	Supply current (quiescent)		All digital inputs at V_{IH}min or V_{IL}max			2			2	mA
I_{DD}	Supply current (standby)		All digital inputs at 0 V or V_{DD}			0.5			0.5	mA
C_i	Input capacitance	DB0–DB7				10			10	pF
		$\overline{WR}$, $\overline{CS}$, $\overline{DACA}$/DACB				15			15	pF
C_o	Output capacitance (OUTA, OUTB)		DAC data latches loaded with 00000000			50			50	pF
			DAC data latches loaded with 11111111			120			120	

† All typical values are at $T_A = 25°C$.

operating characteristic over recommended operating free-air temperature range, V_{refA} = V_{refB} = 10 V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Linearity error					±1/2			±1/2	LSB
Settling time (to 1/2 LSB)		See Note 1			100			100	ns
Gain error		See Note 2			2.5			2.5	LSB
AC feedthrough	REFA to OUTA	See Note 3			−65			−65	dB
	REFB to OUTB				−65			−65	
Temperature coefficient of gain		See Note 4			0.007			0.0035	%FSR/°C
Propagation delay (from digital input to 90% of final analog output current)		See Note 5			80			80	ns
Channel-to-channel isolation	REFA to OUTB	See Note 6		77			77		dB
	REFB to OUTA	See Note 7		77			77		
Digital-to-analog glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C		160			440		nV•s
Digital crosstalk		Measured for code transition from 00000000 to 11111111, T_A = 25°C		30			60		nV•s
Harmonic distortion		V_i = 6 V, f = 1 kHz, T_A = 25°C		−85			−85		dB

NOTES: 1. OUTA, OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0–DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
2. Gain error is measured using an internal feedback resistor. Nominal full scale range (FSR) = V_{ref} – 1 LSB.
3. V_{ref} = 20 V peak-to-peak, 100-kHz sine wave; DAC data latches loaded with 00000000.
4. Temperature coefficient of gain measured from 0°C to 25°C or from 25°C to 70°C.
5. V_{refA} = V_{refB} = 10 V; OUTA/OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0–DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
6. Both DAC latches loaded with 11111111; V_{refA} = 20 V peak-to-peak, 100-kHz sine wave; V_{refB} = 0; T_A = 25°C.
7. Both DAC latches loaded with 11111111; V_{refB} = 20 V peak-to-peak, 100-kHz sine wave; V_{refA} = 0; T_A = 25°C.

PRINCIPLES OF OPERATION

These devices contain two identical, 8-bit-multiplying D/A converters, DACA and DACB. Each DAC consists of an inverted R-2R ladder, analog switches, and input data latches. Binary-weighted currents are switched between DAC output and AGND, thus maintaining a constant current in each ladder leg independent of the switch state. Most applications require only the addition of an external operational amplifier and voltage reference. A simplified D/A circuit for DACA with all digital inputs low is shown in Figure 1.

Figure 2 shows the DACA equivalent circuit. A similar equivalent circuit can be drawn for DACB. Both DACs share the analog ground terminal 1 (AGND). With all digital inputs high, the entire reference current flows to OUTA. A small leakage current (I_{lkg}) flows across internal junctions, and as with most semiconductor devices, doubles every 10°C. C_o is due to the parallel combination of the NMOS switches and has a value that depends on the number of switches connected to the output. The range of C_o is 50 pF to 120 pF maximum. The equivalent output resistance (r_o) varies with the input code from 0.8R to 3R where R is the nominal value of the ladder resistor in the R-2R network.

These devices interface to a microprocessor through the data bus, $\overline{CS}$, $\overline{WR}$, and $\overline{DACA}$/DACB control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the TLC7528 analog output, specified by the $\overline{DACA}$/DACB control line, responds to the activity on the DB0–DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0–DB7 inputs is latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

PRINCIPLES OF OPERATION

The digital inputs of these devices provide TTL compatibility when operated from a supply voltage of 5 V. These devices can operate with any supply voltage in the range from 5 V to 15 V; however, input logic levels are not TTL compatible above 5 V.

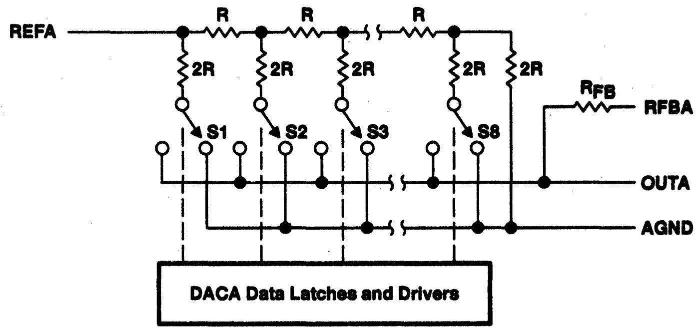


Figure 1. Simplified Functional Circuit for DACA

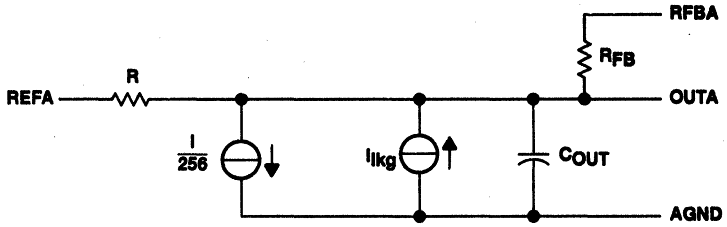


Figure 2. TLC7528 Equivalent Circuit, DACA Latch Loaded With 11111111

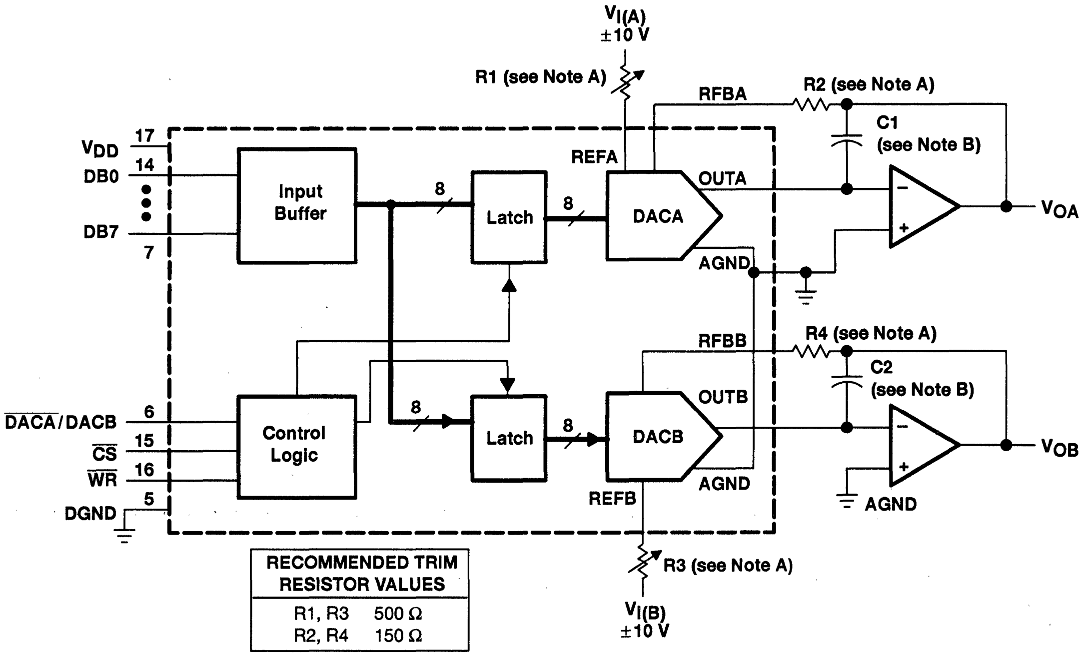
MODE SELECTION TABLE

$\overline{DACA}$/DACB	$\overline{CS}$	$\overline{WR}$	DACA	DACB
L	L	L	Write	Hold
H	L	L	Hold	Write
X	H	X	Hold	Hold
X	X	H	Hold	Hold

L = low level, H = high level, X = don't care

APPLICATION INFORMATION

These devices are capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant and 4-quadrant multiplication are shown in Figures 3 and 4. Tables 1 and 2 summarize input coding for unipolar and bipolar operation.



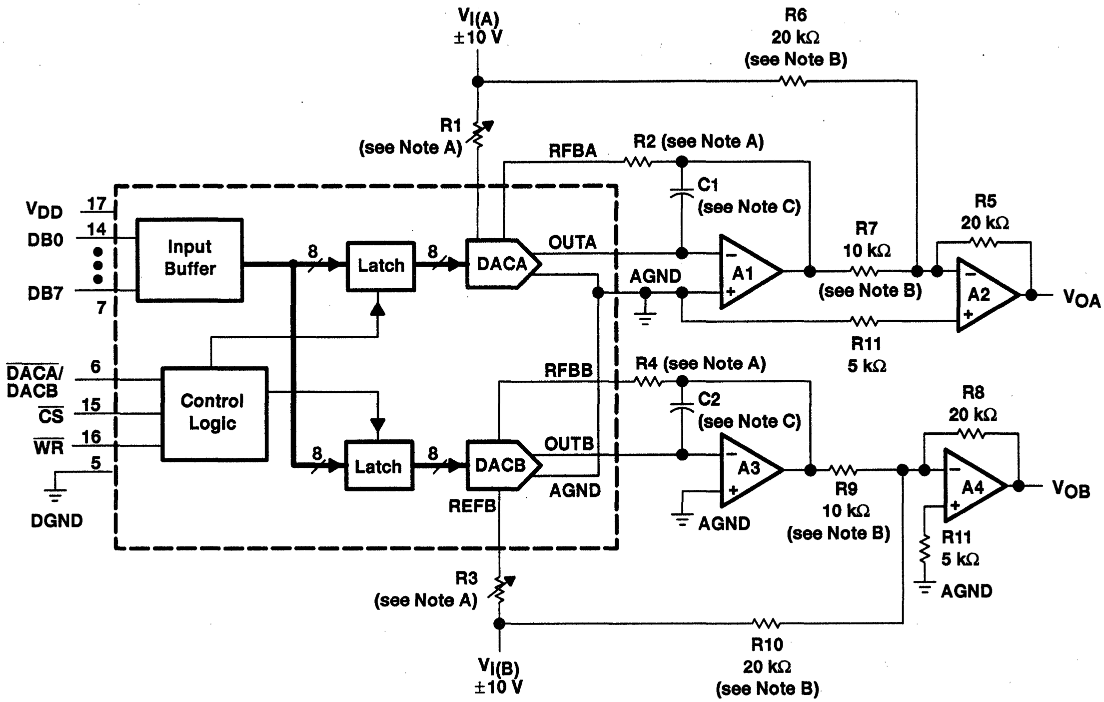
RECOMMENDED TRIM RESISTOR VALUES	
R1, R3	500 Ω
R2, R4	150 Ω

NOTES: A. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.

B. C1 and C2 phase compensation capacitors (10 pF to 15 pF) are required when using high-speed amplifiers to prevent ringing or oscillation.

Figure 3. Unipolar Operation (2-Quadrant Multiplication)

APPLICATION INFORMATION



NOTES: A. R1, R2, R3, and R4 are used only if gain adjustment is required. See table in Figure 3 for recommended values. Adjust R1 for V_{OA} = 0 V with code 10000000 in DACA latch. Adjust R3 for V_{OB} = 0 V with 10000000 in DACB latch.
B. Matching and tracking are essential for resistor pairs R6, R7, R9, and R10.
C. C1 and C2 phase compensation capacitors (10 pF to 15 pF) may be required if A1 and A3 are high-speed amplifiers.

Figure 4. Bipolar Operation (4-Quadrant Operation)

Table 1. Unipolar Binary Code

DAC LATCH CONTENTS MSB LSB†	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$-V_I$ (255/256)
1 0 0 0 0 0 0 1	$-V_I$ (129/256)
1 0 0 0 0 0 0 0	$-V_I$ (128/256) = $-V_I/2$
0 1 1 1 1 1 1 1	$-V_I$ (127/256)
0 0 0 0 0 0 0 1	$-V_I$ (1/256)
0 0 0 0 0 0 0 0	$-V_I$ (0/256) = 0

† 1 LSB = $(2^{-8})V_I$

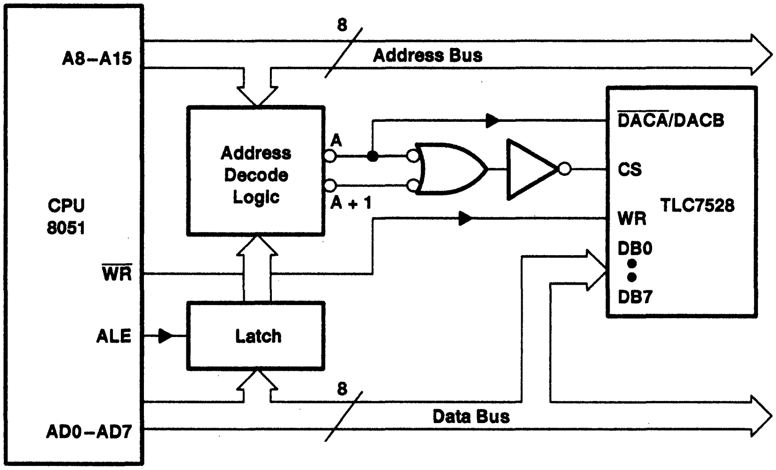
Table 2. Bipolar (Offset Binary) Code

DAC LATCH CONTENTS MSB LSB‡	ANALOG OUTPUT
1 1 1 1 1 1 1 1	V_I (127/128)
1 0 0 0 0 0 0 1	V_I (1/128)
1 0 0 0 0 0 0 0	0 V
0 1 1 1 1 1 1 1	$-V_I$ (1/128)
0 0 0 0 0 0 0 1	$-V_I$ (127/128)
0 0 0 0 0 0 0 0	$-V_I$ (128/128)

‡ 1 LSB = $(2^{-7})V_I$

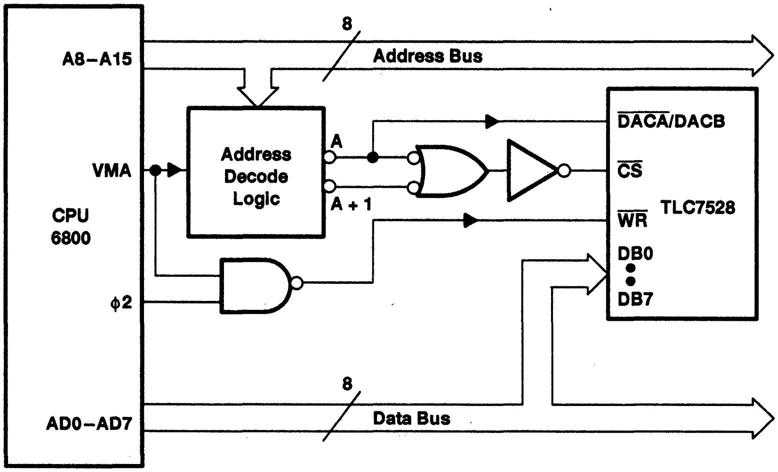
APPLICATION INFORMATION

microprocessor interface information



NOTE A: A = decoded address for TLC7528 DACA
A + 1 = decoded address for TLC7528 DACB

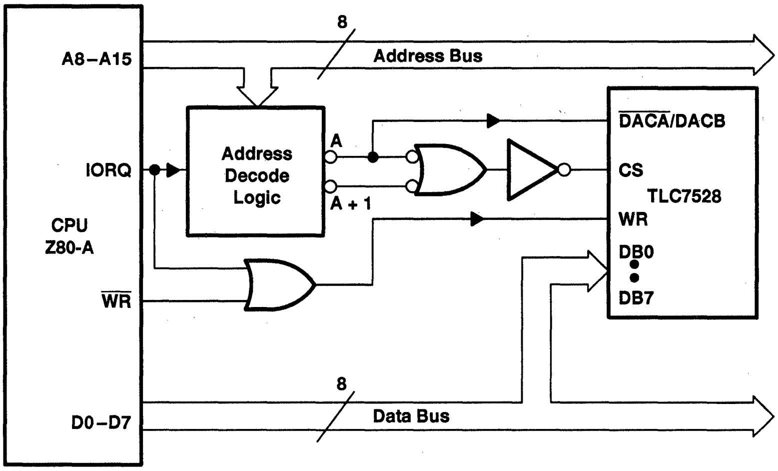
Figure 5. TLC7528 – Intel 8051 Interface



NOTE A: A = decoded address for TLC7528 DACA
A + 1 = decoded address for TLC7528 DACB

Figure 6. TLC7528 – 6800 Interface

APPLICATION INFORMATION



NOTE A: A = decoded address for TLC7528 DACA
A + 1 = decoded address for TLC7528 DACB

Figure 7. TLC7528 To Z-80A Interface

programmable window detector

The programmable window comparator shown in Figure 8 determines if voltage applied to the DAC feedback resistors are within the limits programmed into the data latches of these devices. Input signal range depends on the reference and polarity, that is, the test input range is 0 to $-V_{ref}$. The DACA and DACB data latches are programmed with the upper and lower test limits. A signal within the programmed limits drives the output high.

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APPLICATION INFORMATION

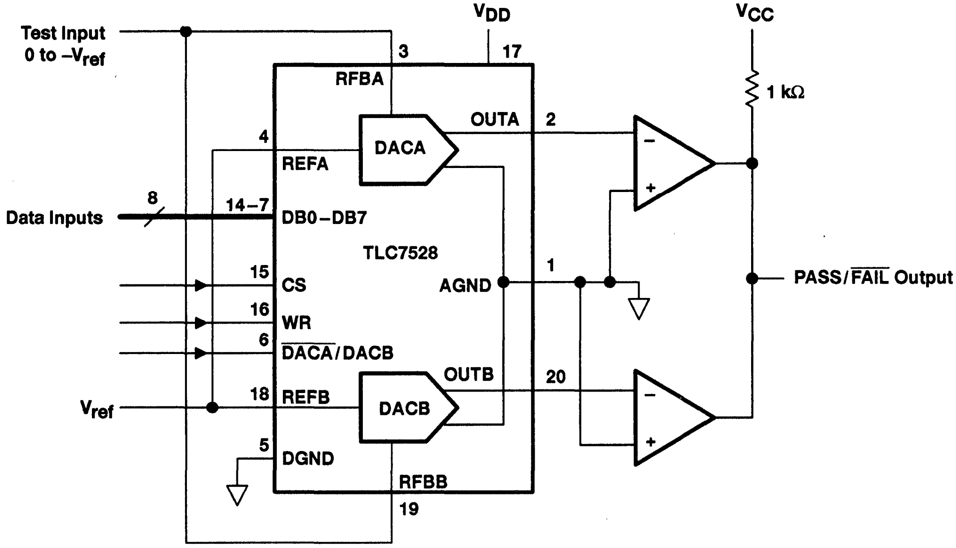


Figure 8. Digitally-Programmable Window Comparator (Upper- and Lower-Limit Tester)

digitally controlled signal attenuator

Figure 9 shows a TLC7528 configured as a two-channel programmable attenuator. Applications include stereo audio and telephone signal level control. Table 3 shows input codes vs attenuation for a 0 to 15.5 dB range.

Attenuation dB = $-20 \log_{10}$ D/256, D = digital input code

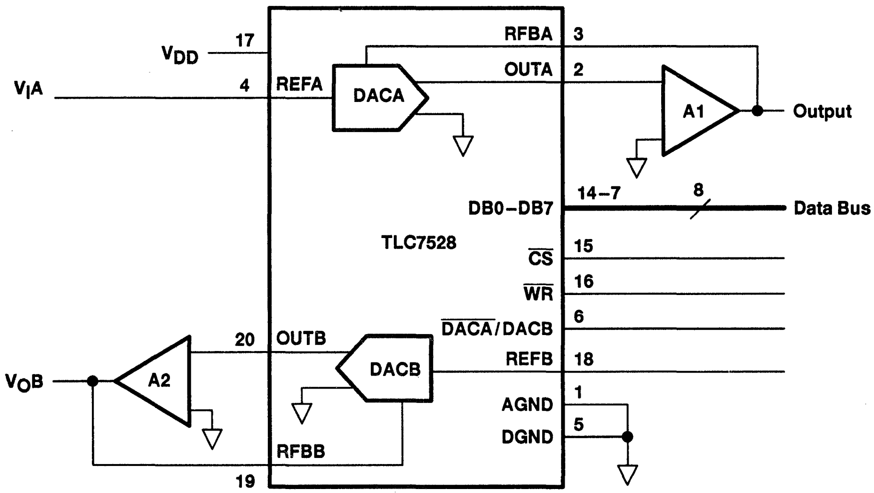


Figure 9. Digitally Controlled Dual Telephone Attenuator

APPLICATION INFORMATION

Table 3. Attenuation vs DACA, DACB Code

ATTN (dB)	DAC INPUT CODE	CODE IN DECIMAL	ATTN (dB)	DAC INPUT CODE	CODE IN DECIMAL
0	11111111	255	8.0	01100110	102
0.5	11110010	242	8.5	01100000	96
1.0	11100100	228	9.0	01011011	91
1.5	11010111	215	9.5	01010110	86
2.0	11001011	203	10.0	01010001	81
2.5	11000000	192	10.5	01001100	76
3.0	10110101	181	11.0	01001000	72
3.5	10101011	171	11.5	01000100	68
4.0	10100010	162	12.0	01000000	64
4.5	10011000	152	12.5	00111101	61
5.0	10011111	144	13.0	00111001	57
5.5	10001000	136	13.5	00110110	54
6.0	10000000	128	14.0	00110011	51
6.5	01111001	121	14.5	00110000	48
7.0	01110010	114	15.0	00101110	46
7.5	01101100	108	15.5	00101011	43

programmable state-variable filter

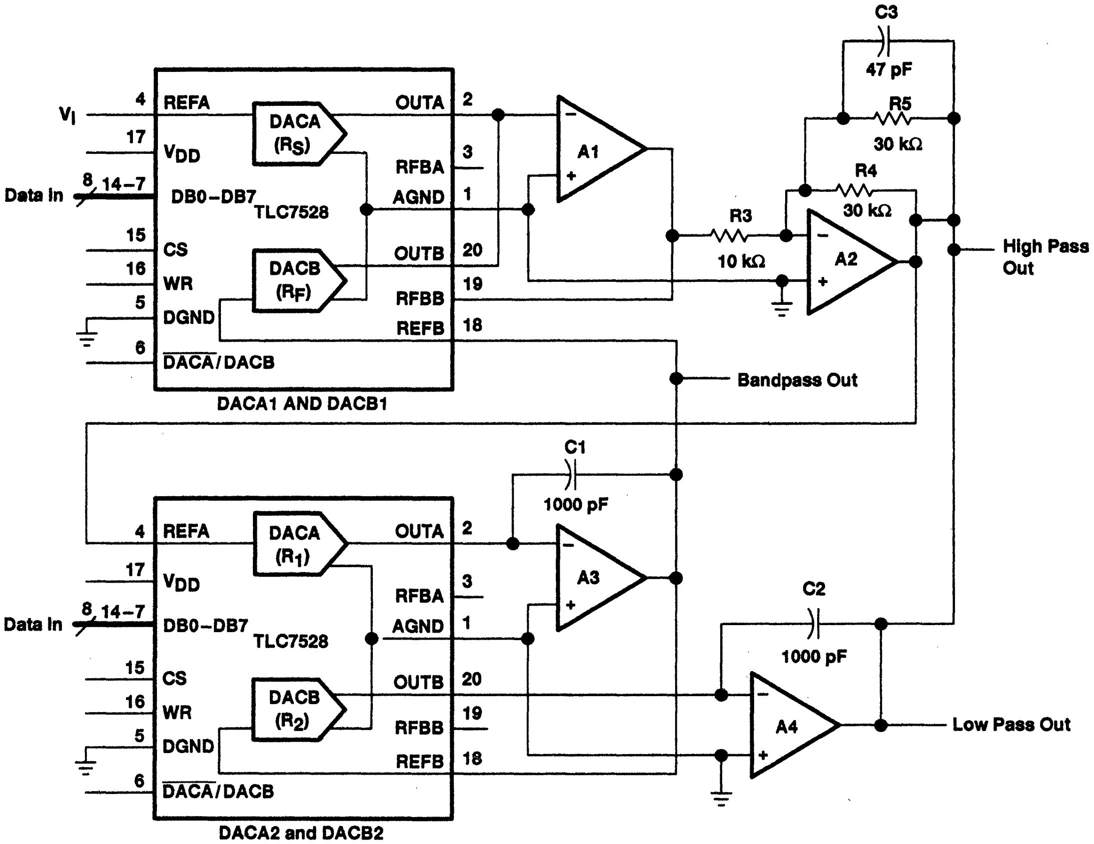
This programmable state-variable or universal filter configuration provides low-pass, high-pass, and bandpass outputs, and is suitable for applications requiring microprocessor control of filter parameters.

As shown in Figure 10, DACA1 and DACB1 control the gain and Q of the filter while DACA2 and DACB2 control the cutoff frequency. Both halves of the DACA2 and DACB2 must track accurately in order for the cutoff-frequency equation to be true. With the TLC7528, this is easy to achieve.

$$f_C = \frac{1}{2\pi\ R1C1}$$

The programmable range for the cutoff or center frequency is 0 to 15 kHz with a Q ranging from 0.3 to 4.5. This defines the limits of the component values.

APPLICATION INFORMATION



Circuit Equations:

$C_1 = C_2,\ R_1 = R_2,\ R_4 = R_5$

$$Q = \frac{R_3}{R_4} \cdot \frac{R_F}{R_{fb(DACB1)}}$$

where:

R_{fb} **is the internal resistor connected between OUTB and RFBB**

$$G = -\frac{R_F}{R_S}$$

NOTES: A. Op-amps A1, A2, A3, and A4 are TL287.
B. $\overline{CS}$ compensates for the op-amp gain-bandwidth limitations.
C. DAC equivalent resistance equals $\frac{256 \times (\text{DAC ladder resistance})}{\text{DAC digital code}}$

Figure 10. Digitally Controlled State-Variable Filter

APPLICATION INFORMATION

voltage-mode operation

It is possible to operate the current multiplying D/A converter of these devices in a voltage mode. In the voltage mode, a fixed voltage is placed on the current output terminal. The analog output voltage is then available at the reference voltage terminal. Figure 11 is an example of a current multiplying D/A, that operates in the voltage mode.

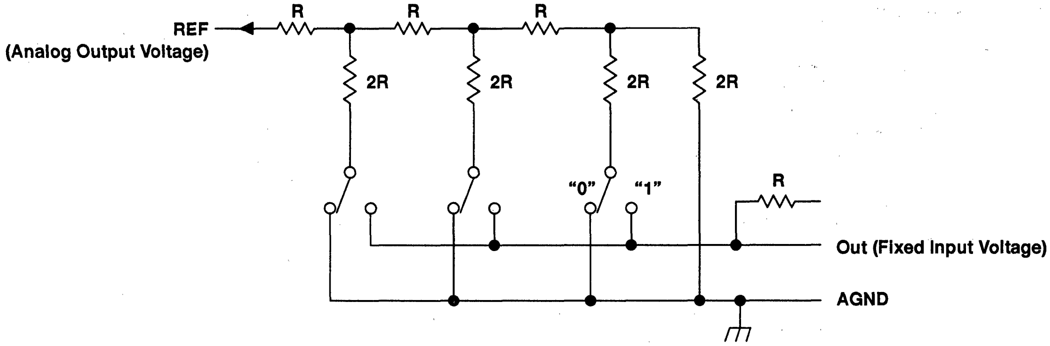


Figure 11. Voltage-Mode Operation

The following equation shows the relationship between the fixed input voltage and the analog output voltage:

$V_O = V_I\ (D/256)$

where

V_O = analog output voltage
V_I = fixed input voltage
D = digital input code converted to decimal

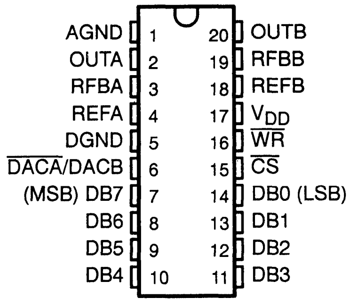
In voltage-mode operation, these devices meets the following specification:

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Linearity error at REFA or REFB	V_{DD} = 5 V, OUTA or OUTB at 2.5 V, T_A = 25°C		1	LSB

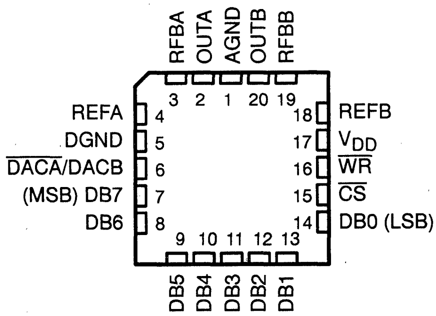
- **Easy Microprocessor Interface**
- **On-Chip Data Latches**
- **Digital Inputs Are TTL-Compatible With 10.8-V to 15.75-V Power Supply**
- **Monotonic Over the Entire A/D Conversion Range**
- **Fast Control Signaling for Digital Signal Processor (DSP) Applications Including Interface With TMS320**
- **CMOS Technology**

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 bits
Linearity Error	1/2 LSB
Power Dissipation	20 mW
Settling Time	100 ns
Propagation Delay Time	80 ns

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TLC7628C, TLC7628E, and TLC2628I are dual, 8-bit, digital-to-analog converters (DACs) designed with separate on-chip data latches and feature exceptionally close DAC-to-DAC matching. Data is transferred to either of the two DAC data latches through a common, 8-bit input port. Control input $\overline{\text{DACA}}$/DACB determines which DAC is loaded. The load cycle of these devices is similar to the write cycle of a random-access memory, allowing easy interface to most popular microprocessor buses and output ports. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, where glitch impulse is typically the strongest.

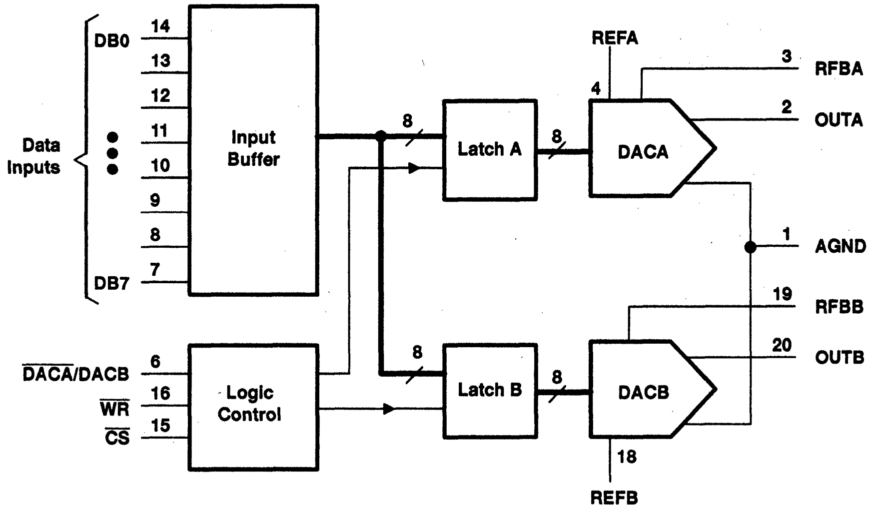
The TLC7628C operates from a 10.8-V to 15.75-V power supply and is TTL-compatible over this range. 2- or 4-quadrant multiplying makes these devices a sound choice for many microprocessor-controlled gain-setting and signal-control applications.

The TLC6728C is characterized for operation from 0°C to 70°C. The TLC7628I is characterized for operation from −25°C to 85°C. The TLC7628E is characterized for operation from −40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGE		
	SMALL OUTLINE PLASTIC DIP (DW)	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	TLC7628CDW	TLC7628CFN	TLC7628CN
−25°C to 85°C	TLC7628IDW	TLC7628IFN	TLC7628IN
−40°C to 85°C	TLC7628EDW	TLC7628EFN	TLC7628EN

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (to AGND or DGND)		−0.3 V to 17 V
Voltage between AGND and DGND		V_{DD}
Input voltage range, V_I (to DGND)		−0.3 V to V_{DD} + 0.3 V
Reference voltage range, V_{refA} or V_{refB} (to AGND)		±25 V
Feedback voltage range, V_{RFBA} or V_{RFBB} (to AGND)		±25 V
Output voltage range, V_{OA} or V_{OB} (to AGND)		±25 V
Peak input current		10 µA
Operating free-air temperature range, T_A:	TLC7628C	0°C to 70°C
	TLC7628I	−25°C to 85°C
	TLC7628E	−40°C to 85°C
Storage temperature range, T_{stg}		−65°C to 150°C
Case temperature for 10 seconds, T_C: FN package		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package		260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		10.8		15.75	V
Reference voltage, V_{refA} or V_{refB}			±10		V
High-level input voltage, V_{IH}		2.4			V
Low-level input voltage, V_{IL}				0.8	V
$\overline{CS}$ setup time, $t_{su(CS)}$		50			ns
$\overline{CS}$ hold time, $t_{h(CS)}$ (see Figure 1)		0			ns
DAC select setup time, $t_{su(DAC)}$ (see Figure 1)		60			ns
DAC select hold time, $t_{h(DAC)}$ (see Figure 1)		10			ns
Data bus input setup time $t_{su(D)}$ (see Figure 1)		25			ns
Data bus input hold time $t_{h(D)}$ (see Figure 1)		10			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$ (see Figure 1)		50			ns
Operating free-air temperature, T_A	TLC7628C	0		70	°C
	TLC7628I	−25		85	
	TLC7628E	−40		85	

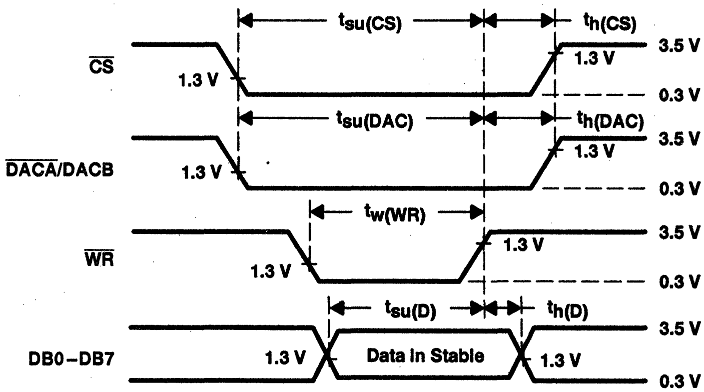
electrical characteristics over recommended ranges of operating free-air temperature and V_{DD}, $V_{refA} = V_{refB} = 10$ V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
I_{IH}	High-level input current		$V_I = V_{DD}$	Full range		10	μA
				25°C		1	
I_{IL}	Low-level input current		$V_I = 0$	Full range		−10	μA
				25°C		−1	
	Reference input impedance REFA or REFB to AGND				5	20	kΩ
I_{kg}	Output leakage current	OUTA	DAC data latch loaded with 00000000, $V_{refA} = \pm 10$ V	Full range		±200	nA
				25°C		±50	
		OUTB	DAC data latch loaded with 00000000, $V_{refB} = \pm 10$ V	Full range		±200	
				25°C		±50	
	Input resistance match (REFA to REFB)					±1%	
	DC supply sensitivity $\Delta gain/\Delta V_{DD}$		$\Delta V_{DD} = \pm 5$ %	Full range		0.02	%/%
				25°C		0.01	
I_{DD}	Supply current	Quiescent	All digital inputs at V_{IH}min or V_{IL}max			2	mA
		Standby	All digital inputs at 0 V or V_{DD}	Full range		0.5	
				25°C		0.1	
C_i	Input capacitance	DB0–DB7				10	pF
		$\overline{WR}$, $\overline{CS}$, $\overline{DACA}$/DACB				15	
C_o	Output capacitance (OUTA, OUTB)		DAC data latches loaded with 00000000			25	pF
			DAC data latches loaded with 11111111			60	

operating characteristics over recommended ranges of operating free-air temperature and V_{DD}, $V_{refA} = V_{refB} = 10$ V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Linearity error						±1/2	LSB
Settling time (to 1/2 LSB)		See Note 1				100	ns
Gain error		See Note 2	Full range			±3	LSB
			25°C			±2	
AC feedthrough	REFA to OUTA	See Note 3	Full range			−65	dB
	REFB to OUTB		25°C			−75	
Temperature coefficient of gain						±0.0035	%FSR/°C
Propagation delay (from digital input to 90% of final analog output current)		See Note 4				80	ns
Channel-to-channel isolation	REFA to OUTB	See Note 5	25°C		80		dB
	REFB to OUTA	See Note 6	25°C		80		
Digital-to-analog glitch impulse area		Measured for code transition from 00000000 to 11111111, $T_A = 25°C$			330		nV•s
Digital crosstalk		Measured for code transition from 00000000 to 11111111, $T_A = 25°C$			60		nV•s
Harmonic distortion		$V_i = 6$ V, f = 1 kHz, $T_A = 25°C$			−85		dB

NOTES: 1. OUTA, OUTB load = 100 Ω, $C_{ext} = 13$ pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0–DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
2. Gain error is measured using an internal feedback resistor. Nominal full scale range (FSR) = V_{ref} − 1 LSB. Both DAC latches are loaded with 11111111.
3. $V_{ref} = 20$ V peak-to-peak, 10-kHz sine wave
4. $V_{refA} = V_{refB} = 10$ V; OUTA/OUTB load = 100 Ω, $C_{ext} = 13$ pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0–DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
5. $V_{refA} = 20$ V peak-to-peak, 10-kHz sine wave; $V_{refB} = 0$
6. $V_{refB} = 20$ V peak-to-peak, 10-kHz sine wave; $V_{refA} = 0$

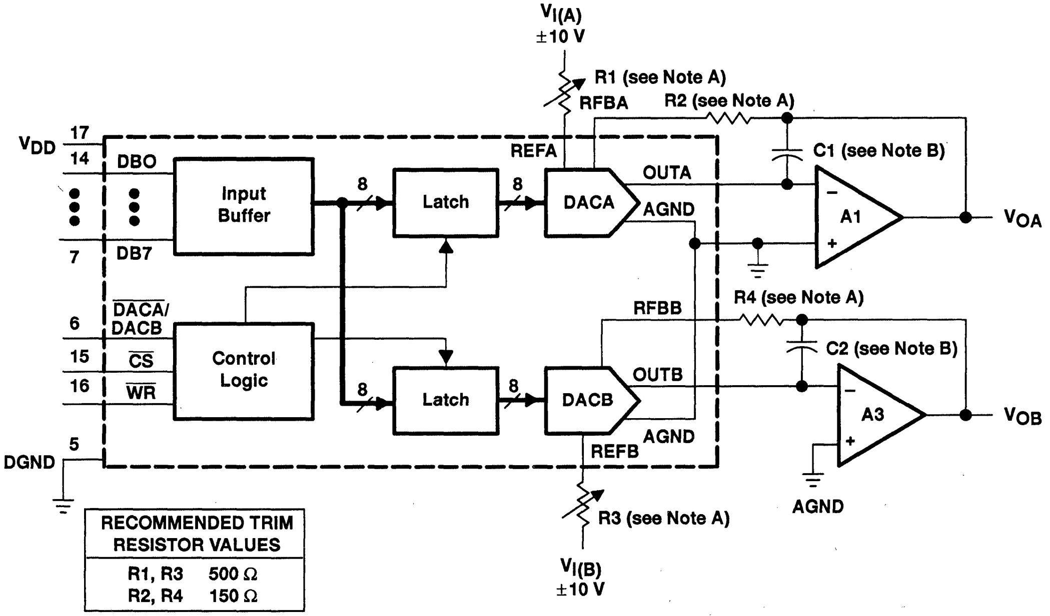


For all input signals, $t_r = t_f = 5$ ns (10% to 90% points).

Figure 1. Setup and Hold Times

APPLICATION INFORMATION

These devices are capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant and 4-quadrant multiplication are shown in Figures 2 and 3. Input coding for unipolar and bipolar operation are summarized in Tables 2 and 3, respectively.



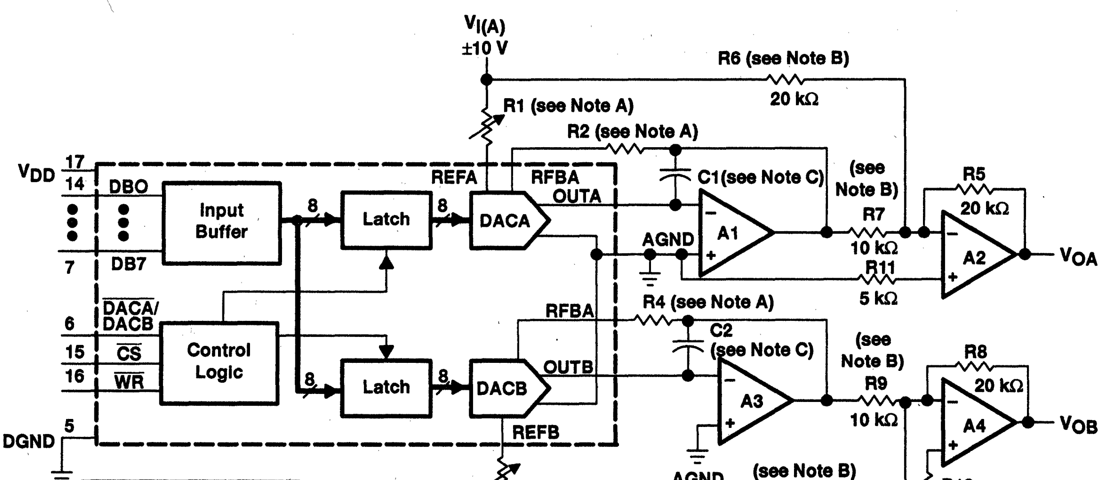
RECOMMENDED TRIM RESISTOR VALUES	
R1, R3	500 Ω
R2, R4	150 Ω

NOTES: A. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.

B. C1 and C2 phase compensation capacitors (10 pF to 15 pF) are required when using high-speed amplifiers to prevent ringing or oscillation.

Figure 2. Unipolar Operation (2-Quadrant Multiplication)

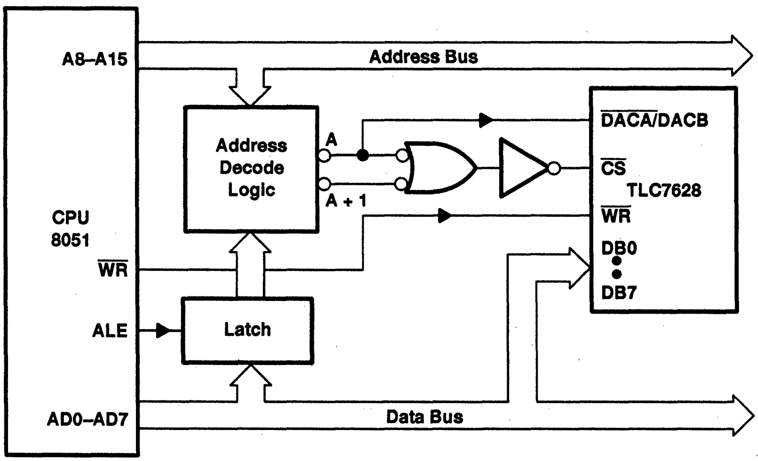
APPLICATION INFORMATION



RECOMMENDED TRIM RESISTOR VALUES	
R1, R3	500 Ω
R2, R4	150 Ω

NOTES: A. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Adjust R1 for V_{OA} = 0 V with code 10000000 in DACA latch. Adjust R3 for V_{OB} = 0 V with 10000000 in DACB latch.
B. Matching and tracking are essential for resistor pairs R6, R7, R9, and R10.
C. C1 and C2 phase compensation capacitors (10 pF to 15 pF) may be required if A1 and A3 are high-speed amplifiers.

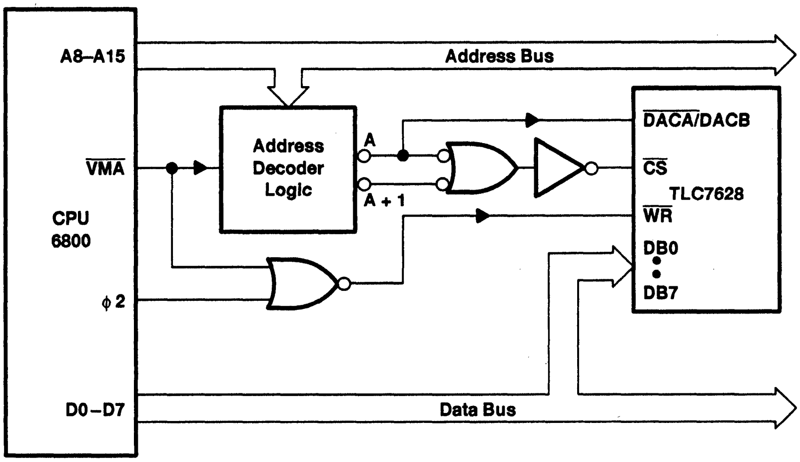
Figure 3. Bipolar Operation (4-Quadrant Operation)



NOTE A: A = decoded address for TLC7628 DACA
A + 1 = decoded address for TLC7628 DACB

Figure 4. TLC7628 — Intel 8051 Interface

APPLICATION INFORMATION



NOTE A: A = decoded address for TLC7628 DACA
A + 1 = decoded address for TLC7628 DACB

Figure 5. TLC7628 – 6800 Interface

voltage-mode operation

The current-multiplying DAC in these devices can be operated in a voltage mode. In the voltage mode, a fixed voltage is placed on the current output terminal. The analog output voltage is then available at the reference voltage terminal. An example of a current-multiplying DAC operating in voltage mode is shown in Figure 6. The relationship between the fixed input voltage and the analog output voltage is given by the following equation:

Analog output voltage = fixed input voltage (D/256)

where D = the digital input. In voltage-mode operation, these devices meet the following specification:

LINEARITY ERROR	TEST CONDITIONS	MIN	MAX	UNIT
Analog output voltage for REFA, REFB	V_{DD} = 12 V, OUTA or OUTB at 5 V, T_A = 25°C		1	LSB

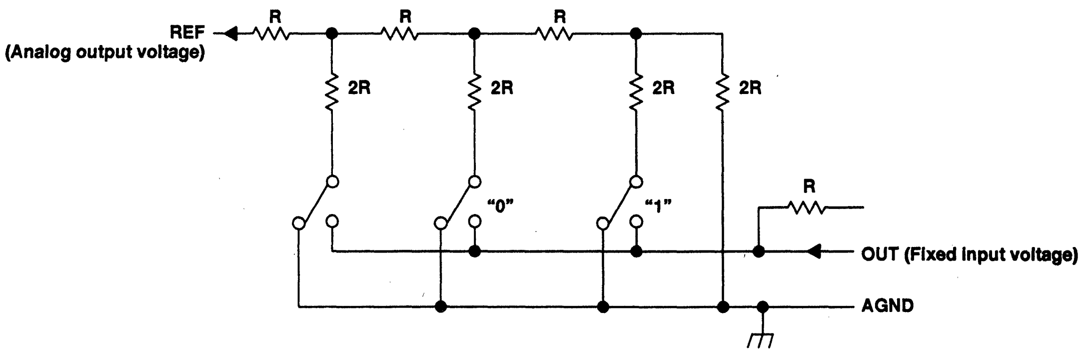


Figure 6. Current-Multiplying DAC Operating in Voltage Mode

PRINCIPLES OF OPERATION

These devices contain two, identical, 8-bit, multiplying DACs, DACA and DACB. Each DAC consists of an inverted R-2R ladder, analog switches, and input data latches. Binary-weighted currents are switched between the DAC output and AGND, thus maintaining a constant current in each ladder leg independent of the switch state. Most applications require only the addition of an external operational amplifier and voltage reference. A simplified D/A circuit for DACA or DACB with all digital inputs low is shown in Figure 7.

Figure 8 shows the DACA or DACB equivalent circuit. Both DACs share the analog ground terminal 1 (AGND). With all digital inputs high, the reference current flows to OUTA. A small leakage current (I_{lkg}) flows across internal junctions, and as with most semiconductor devices, doubles every 10°C. The C_O is caused by the parallel combination of the NMOS switches and has a value that depends on the number of switches connected to the output. The range of C_O is 25 pF to 60 pF maximum. The equivalent output resistance (r_O) varies with the input code from 0.8R to 3R where R is the nominal value of the ladder resistor in the R-2R network.

These devices interface to a microprocessor through the data bus, $\overline{CS}$, $\overline{WR}$, and $\overline{DACA}$/DACB control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the analog output on these devices, specified by the $\overline{DACA}$/DACB control line, responds to the activity on the DB0–DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0–DB7 inputs is latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled, regardless of the state of the $\overline{WR}$ signal.

The digital inputs of these devices provide TTL compatibility when operated from a supply voltage of 10.8 V to 15.75 V.

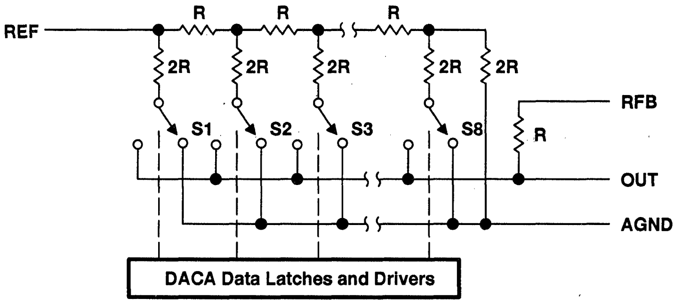


Figure 7. Simplified Functional Circuit for DACA or DACB

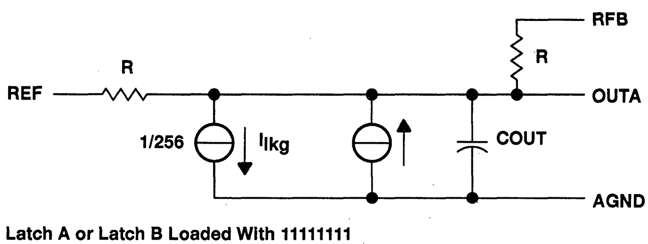


Figure 8. TLC7628 Equivalent Circuit for DACA or DACB

PRINCIPLES OF OPERATION

Table 1. MODE SELECTION TABLE

$\overline{\text{DACA}}$/DACB	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DACA	DACB
L	L	L	Write	Hold
H	L	L	Hold	Write
X	H	X	Hold	Hold
X	X	H	Hold	Hold

L = low level, H = high level, X = don't care

Table 2. Unipolar Binary Code

DAC LATCH CONTENTS (see Note 7) MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$-V_I$ (255/256)
1 0 0 0 0 0 0 1	$-V_I$ (129/256)
1 0 0 0 0 0 0 0	$-V_I$ (128/256) = $-V_i$ /2
0 1 1 1 1 1 1 1	$-V_I$ (127/256)
0 0 0 0 0 0 0 1	$-V_I$ (1/256)
0 0 0 0 0 0 0 0	$-V_I$ (0/256) = 0

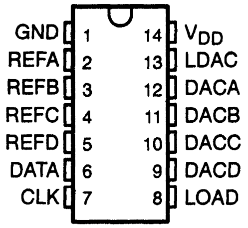
Table 3. Bipolar (Offset Binary) Code

DAC LATCH CONTENTS (see Note 8) MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	V_I (127/128)
1 0 0 0 0 0 0 1	V_I (1/128)
1 0 0 0 0 0 0 0	0 V
0 1 1 1 1 1 1 1	$-V_I$ (1/128)
0 0 0 0 0 0 0 1	$-V_I$ (127/128)
0 0 0 0 0 0 0 0	$-V_I$ (128/128)

NOTES: 7. 1 LSB = $(2^{-8})V_I$
8. 1 LSB = $(2^{-7})V_I$

- Four 8-Bit Voltage Output DACs
- 3-V Single-Supply Operation
- Serial Interface
- High-Impedance Reference Inputs
- Programmable 1 or 2 Times Output Range
- Simultaneous-Update Facility
- Internal Power-On Reset
- Low Power Consumption
- Half-Buffered Output

N OR D PACKAGE
(TOP VIEW)



applications

- Programmable Voltage Sources
- Digitally-Controlled Amplifiers/Attenuators
- Mobile Communications
- Automatic Test Equipment
- Process Monitoring and Control
- Signal Synthesis

description

The TLV5620C and TLV5620I are quadruple 8-bit voltage output digital-to-analog converters (DACs) with buffered reference inputs (high impedance). The DACs produce an output voltage that ranges between either one or two times the reference voltages and GND and the DACs are monotonic. The device is simple to use, running from a single supply of 3 to 3.6 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the TLV5620C and TLV5620I are over a simple 3-wire serial bus that is CMOS compatible and easily interfaced to all popular microprocessor and microcontroller devices. The 11-bit command word comprises 8 bits of data, 2 DAC select bits and a range bit, the latter allowing selection between the times 1 or times 2 output range. The DAC registers are double buffered, allowing a complete set of new values to be written to the device, then all DAC outputs updated simultaneously through control of the LDAC terminal. The digital inputs feature Schmitt triggers for high noise immunity.

The 14-terminal small-outline (SO) package allows digital control of analog functions in space-critical applications. The TLV5620C is characterized for operation from 0°C to 70°C. The TLV5620I is characterized for operation from −40°C to 85°C. The TLV5620C and TLV5620I do not require external trimming.

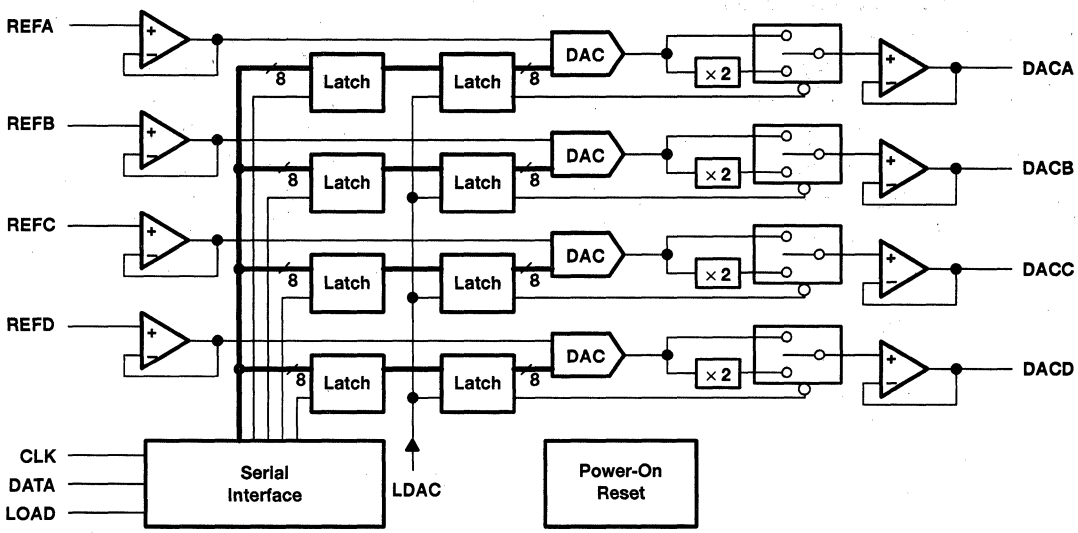
PRODUCT PREVIEW

AVAILABLE OPTIONS

T_A	PACKAGE	
	SMALL OUTLINE (D)	PLASTIC DIP (N)
0°C to 70°C	TLV5620CD	TLV5620CN
−40°C to 85°C	TLV5620ID	TLV5620IN

PRODUCT PREVIEW

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLK	7	I	Serial-interface clock, data enters on the negative edge
DACA	12	O	DAC A analog output
DACB	11	O	DAC B analog output
DACC	10	O	DAC C analog output
DACD	9	O	DAC D analog output
DATA	6	I	Serial-interface digital-data input
GND	1	I	Ground return and reference terminal
LDAC	13	I	DAC-update latch control
LOAD	8	I	Serial-interface load control
REFA	2	I	Reference voltage input to DACA
REFB	3	I	Reference voltage input to DACB
REFC	4	I	Reference voltage input to DACC
REFD	5	I	Reference voltage input to DACD
V_{DD}	14	I	Positive supply voltage

detailed description

The TLV5620 is implemented using four resistor-string digital-to-analog converters (DACs). The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes listed in Table 2. One end of each resistor string is connected to the GND terminal and the other end is fed from the output of the reference input buffer. Monotonicity is maintained by use of the resistor strings. Linearity depends upon the matching of the resistor elements and upon the performance of the output buffer. Because the inputs are buffered, the DACs always presents a high-impedance load to the reference source.

detailed description (continued)

Each DAC output is buffered by a configurable-gain output amplifier, which can be programmed to times 1 or times 2 gain.

On powerup, the DACs are reset to CODE 0.

Each output voltage is given by:

$$V_O(DACA|B|C|D) = REF \times \frac{CODE}{256} \times (1 + RNG\ bit\ value)$$

where CODE is in the range 0 to 255 and the range (RNG) bit is a 0 or 1 within the serial-control word.

data interface

With LOAD high, data is clocked into the DATA terminal on each falling edge of CLK. Once all data bits have been clocked in, LOAD is pulsed low to transfer the data from the serial-input register to the selected DAC as shown in Figure 1. If LDAC is low, the selected DAC output voltage is updated and LOAD goes low. If LDAC is high during serial programming, the new value is stored within the device and can be transferred to the DAC output at a later time by pulsing LDAC low as shown in Figure 2. Data is entered MSB first.

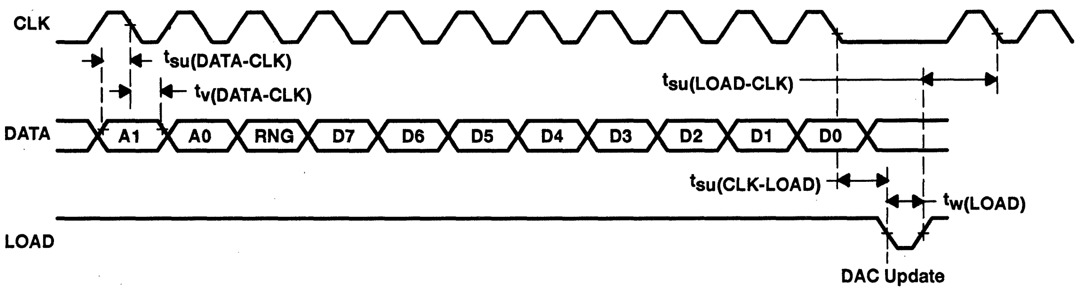


Figure 1. LOAD-Controlled Update (LDAC = Low)

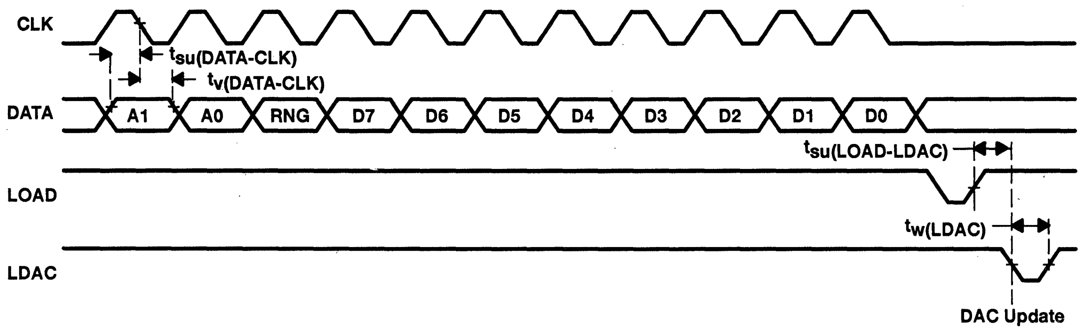


Figure 2. LDAC-Controlled Update

data interface (continued)

Table 1 lists the A1 and A0 bits and the selection of the updated DACs. The RNG bit controls the DAC output range. When RNG = low, the output range is between the applied reference voltage and GND, and when RNG = high, the range is between twice the applied reference voltage and GND.

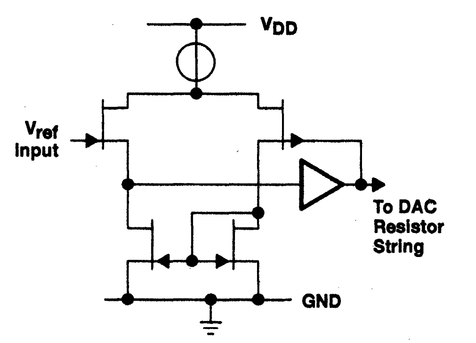
Table 1. Serial-Input Decode

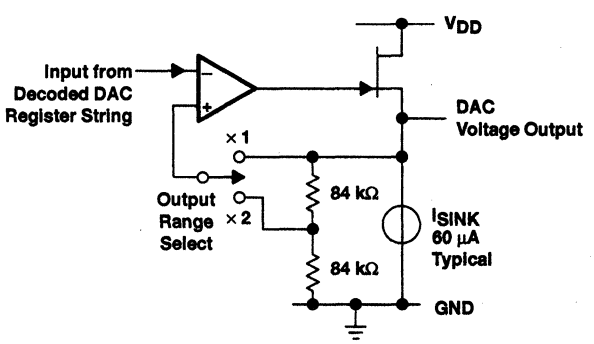
A1	A0	DAC UPDATED
0	0	DACA
0	1	DACB
1	0	DACC
1	1	DACD

Table 2. Ideal-Output Transfer

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	(1/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	(127/256) × REF (1+RNG)
1	0	0	0	0	0	0	0	(128/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	(255/256) × REF (1+RNG)

equivalent inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} – GND) .... 7 V
Digital input voltage range .... GND – 0.3 V to V_{DD} + 0.3 V
Reference input voltage range, V_{ID} .... GND – 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A: TLV5620C .... 0°C to 70°C
TLV5620I .... –40°C to 85°C
Storage temperature range, T_{stg} .... –50°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 230°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		2.7	3.3	5.25	V
High-level digital input voltage, V_{IH}		0.8 V_{DD}			V
Low-level digital input voltage, V_{IL}				0.8	V
Reference voltage, V_{ref} [A|B|C|D], x1 gain				V_{DD}–1.5	V
Load resistance, R_L		10			kΩ
Setup time, data input, $t_{su(DATA\text{-}CLK)}$ (see Figures 1 and 2)		50			ns
Valid time, data input valid after CLK↓, $t_{v(DATA\text{-}CLK)}$ (see Figures 1 and 2)		50			ns
Setup time, CLK eleventh falling edge to LOAD, $t_{su(CLK\text{-}LOAD)}$ (see Figure 1)		50			ns
Setup time, LOAD↑ to CLK↓, $t_{su(LOAD\text{-}CLK)}$ (see Figure 1)		50			ns
Pulse duration, LOAD, $t_{w(LOAD)}$ (see Figure 1)		250			ns
Pulse duration, LDAC, $t_{w(LDAC)}$ (see Figure 2)		250			ns
Setup time, LOAD↑ to LDAC↓, $t_{su(LOAD\text{-}LDAC)}$ (see Figure 2)		0			ns
CLK frequency				1	MHz
Operating free-air temperature, T_A	TLV5620C	0		70	°C
	TLV5620I	–40		85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 3 V to 3.6 V, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current	$V_I = V_{DD}$			±10	µA
I_{IL}	Low-level digital input current	V_I = 0 V			±10	µA
$I_{O(sink)}$	Output sink current	Each DAC output	20			µA
$I_{O(source)}$	Output source current	Each DAC output	2			mA
C_i	Input capacitance			15		pF
C_i	Reference input capacitance			15		pF
I_{DD}	Supply current	V_{DD} = 3.3 V			2	mA
I_{ref}	Reference input current	V_{DD} = 3.3 V, V_{ref} = 1.5 V			±10	µA
E_L	Linearity error (end point corrected)	V_{ref} = 1.25 V, × 2 gain (see Note 1)			±1	LSB
E_D	Differential linearity error	V_{ref} = 1.25 V, × 2 gain (see Note 2)			±0.9	LSB
E_{ZS}	Zero-scale error	V_{ref} = 1.25 V, × 2 gain (see Note 3)	0		30	mV
	Zero-scale error temperature coefficient	V_{ref} = 1.25 V, × 2 gain (see Note 4)		10		µV/°C
E_{FS}	Full-scale error	V_{ref} = 1.25 V, × 2 gain (see Note 5)			±60	mV
	Full-scale error temperature coefficient	V_{ref} = 1.25 V, × 2 gain (see Note 6)		±25		µV/°C
PSRR	Power-supply sensitivity	See Notes 7 and 8		0.5		mV/V

NOTES: 1. Integral nonlinearity (INL) is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full-scale errors).
2. Differential nonlinearity (DNL) is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
3. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
4. Zero-scale error temperature coefficient is given by: ZSETC = $[ZSE(T_{max}) - ZSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
5. Full-scale error is the deviation from the ideal full-scale output (V_{ref} – 1 LSB) with an output load of 10 kΩ.
6. Full-scale temperature coefficient is given by: FSETC = $[FSE(T_{max}) - FSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
7. Zero-scale error rejection ratio (ZSE-RR) is measured by varying the V_{DD} voltage from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
8. Full-scale error rejection ratio (FSE-RR) is measured by varing the V_{DD} from 3.0 V to 3.6 V dc and measuring the proportion of this signal imposed on the full-scale output voltage.

operating characteristics over recommended operating free-air temperature range, V_{DD} = 3 V to 3.6 V, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate	C_L = 100 pF, R_L = 10 kΩ		1		V/µs
Output settling time	To 0.5 LSB, C_L = 100 pF, R_L = 10 kΩ, See Note 9		10		µs
Large-signal bandwidth	Measured at –3 dB point		100		kHz
Digital crosstalk	CLK = 1-MHz square wave measured at DACA-DACD		–50		dB
Reference feedthrough	See Note 10		–60		dB
Channel-to-channel isolation	See Note 11		–60		dB
Reference input bandwidth	See Note 12		100		kHz

NOTES: 9. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 00 hex to FF hex or FF hex to 00 hex. For TLV5620C: V_{DD} = 5 V, V_{ref} = 2 V and range = ×2. For TLV5620I: V_{DD} = 3 V, V_{ref} = 1.25 V and range ×2.
10. Reference feedthrough is measured at any DAC output with an input code = 00 hex with a V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
11. Channel-to-channel isolation is measured by setting the input code of one DAC to FF hex and the code of all other DACs to 00 hex with V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
12. Reference bandwidth is the –3 dB bandwidth with an input at V_{ref} = 1.25 V dc + 2 V_{pp}, with a digital input code of full-scale.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

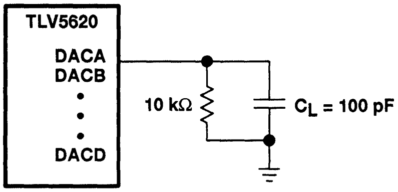
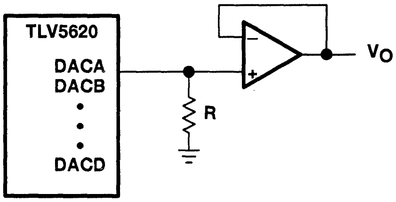


Figure 3. Slewing Settling Time and Linearity Measurements

APPLICATION INFORMATION



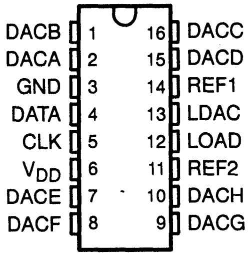
NOTE A: Resistor R ≥ 10 kΩ

Figure 4. Output Buffering Schemes

PRODUCT PREVIEW

- **Eight 8-Bit Voltage Output DACs**
- **3-V Single-Supply Operation**
- **Serial Interface**
- **High-Impedance Reference Inputs**
- **Programmable 1 or 2 Times Output Range**
- **Simultaneous-Update Facility**
- **Internal Power-On Reset**
- **Low Power Consumption**
- **Half-Buffered Output**

N OR D PACKAGE
(TOP VIEW)



applications

- **Programmable Voltage Sources**
- **Digitally-Controlled Amplifiers/Attenuators**
- **Mobile Communications**
- **Automatic Test Equipment**
- **Process Monitoring and Control**
- **Signal Synthesis**

description

The TLV5628C and TLV5628I are octal 8-bit voltage output digital-to-analog converters (DACs) with buffered reference inputs (high impedance). The DACs produce an output voltage that ranges between either one or two times the reference voltages and GND, and the DACs are monotonic. The device is simple to use, running from a single supply of 3 to 3.6 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the TLV5628C and TLV5628I is over a simple 3-wire serial bus that is CMOS compatible and easily interfaced to all popular microprocessor and microcontroller devices. The 12-bit command word comprises 8 bits of data, 3 DAC select bits and a range bit, the latter allowing selection between the times 1 or times 2 output range. The DAC registers are double buffered, allowing a complete set of new values to be written to the device, then all DAC outputs updated simultaneously through control of the LDAC terminal. The digital inputs feature Schmitt triggers for high noise immunity.

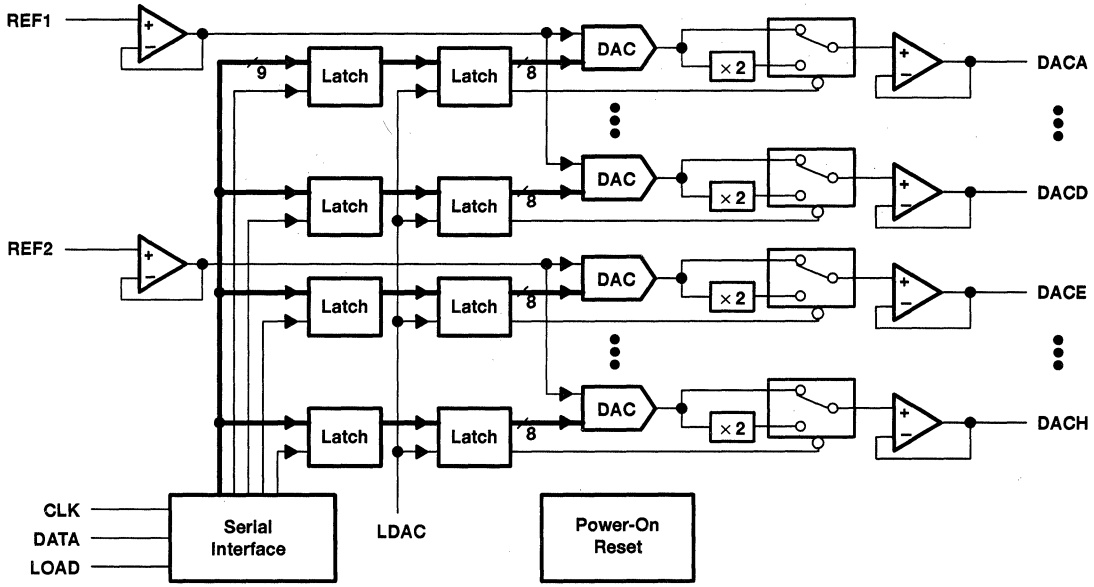
The 16-terminal small-outline D package allows digital control of analog functions in space-critical applications. The TLV5628C is characterized for operation from 0°C to 70°C. The TLV5628I is characterized for operation from –40°C to 85°C. The TLV5628C and TLV5628I do not require external trimming.

PRODUCT PREVIEW

AVAILABLE OPTIONS

T_A	PACKAGE SMALL OUTLINE (D)	PACKAGE PLASTIC DIP (N)
0°C to 70°C	TLV5628CD	TLV5628CN
–40°C to 85°C	TLV5628ID	TLV5628IN

functional block diagram



PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLK	5	I	Serial-interface clock, data enters on the negative edge
DACA	2	O	DACA analog output
DACB	1	O	DACB analog output
DACC	16	O	DACC analog output
DACD	15	O	DACD analog output
DACE	7	O	DACE analog output
DACF	8	O	DACF analog output
DACG	9	O	DACG analog output
DACH	10	O	DACH analog output
DATA	4	I	Serial-interface digital data input
GND	3	I	Ground return and reference terminal
LDAC	13	I	DAC-update latch control
LOAD	12	I	Serial-interface load control
REF1	14	I	Reference voltage input to DACA
REF2	11	I	Reference voltage input to DACB
V_{DD}	6	I	Positive supply voltage

detailed description

The TLV5628 is implemented using eight resistor-string DACs. The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes listed in Table 2. One end of each resistor string is connected to the GND terminal and the other end is fed from the output of the reference input buffer. Monotonicity is maintained by use of the resistor strings. Linearity depends upon the matching of the resistor elements and upon the performance of the output buffer. Because the inputs are buffered, the DACs always present a high-impedance load to the reference sources. There are two input reference terminals; REF1 is used for DACA through DACD and REF2 is used by DACE through DACH.

Each DAC output is buffered by a configurable-gain output amplifier, which can be programmed to times 1 or times 2 gain.

On powerup, the DACs are reset to CODE 0.

Each output voltage is given by:

$$V_O(\mathrm{DACA|B|C|D|E|F|G|H}) = \mathrm{REF} \times \frac{\mathrm{CODE}}{256} \times (1 + \mathrm{RNG\ bit\ value})$$

where CODE is in the range 0 to 255 and the range (RNG) bit is a 0 or 1 within the serial-control word.

data interface

With LOAD high, data is clocked into the DATA terminal on each falling edge of CLK. Once all data bits have been clocked in, LOAD is pulsed low to transfer the data from the serial-input register to the selected DAC as shown in Figure 1. If LDAC is low, the selected DAC output voltage is updated and LOAD goes low. If LDAC is high during serial programming, the new value is stored within the device and can be transferred to the DAC output at a later time by pulsing LDAC low as shown in Figure 2. Data is entered MSB first.

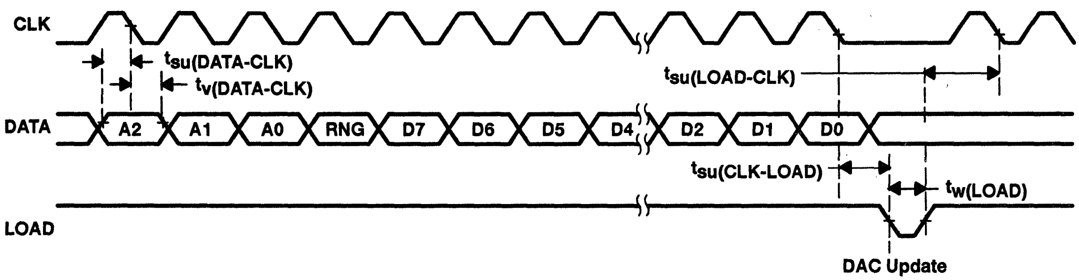


Figure 1. LOAD-Controlled Update (LDAC = Low)

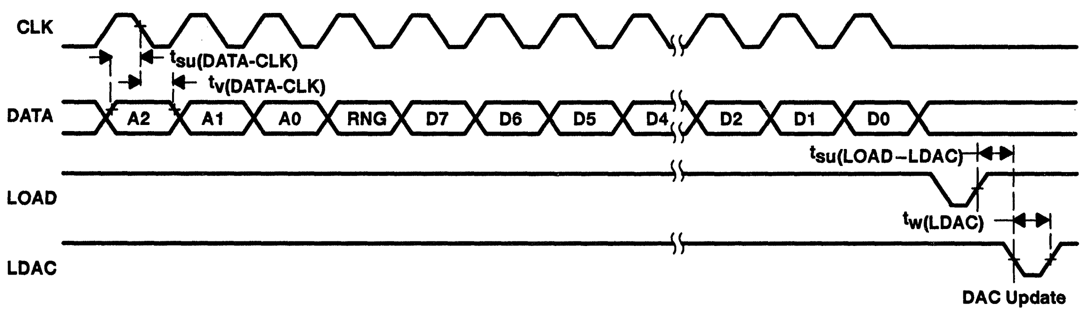


Figure 2. LDAC-Controlled Update

data interface (continued)

Table 1 lists the A1 and A0 bits and the selection of the updated DACs. The RNG bit controls the DAC output range. When RNG = low, the output range is between the applied reference voltage and GND, and when RNG = high, the range is between twice the applied reference voltage and GND.

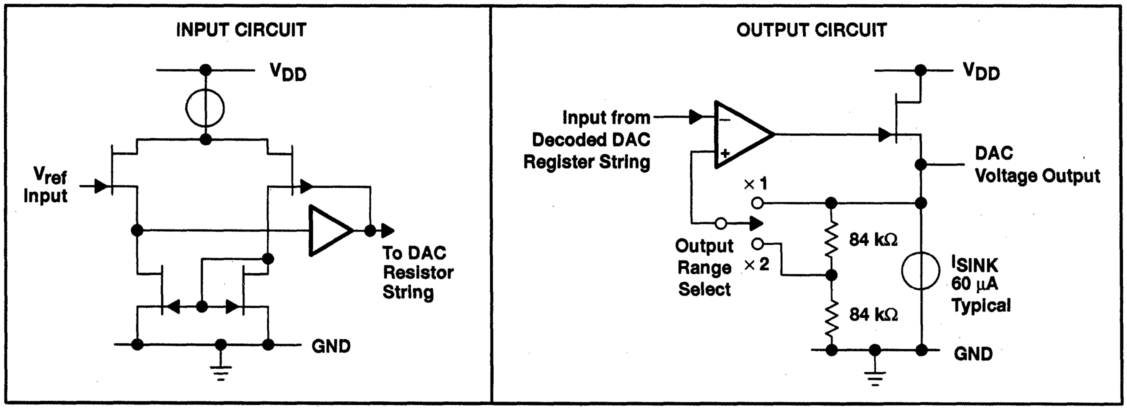
Table 1. Serial-Input Decode

A2	A1	A0	DAC UPDATED
0	0	0	DACA
0	0	1	DACB
0	1	0	DACC
0	1	1	DACD
1	0	0	DACE
1	0	1	DACF
1	1	0	DACG
1	1	1	DACH

Table 2. Ideal-Output Transfer

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	(1/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	(127/256) × REF (1+RNG)
1	0	0	0	0	0	0	0	(128/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	(255/256) × REF (1+RNG)

equivalent inputs and outputs



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} – GND) .... 7 V
Digital input voltage range, V_{ID} .... GND – 0.3 V to V_{DD} + 0.3 V
Reference input voltage range .... GND – 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A: TLV5628C .... 0°C to 70°C
TLV5628I .... –40°C to 85°C
Storage temperature range, T_{stg} .... –50°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 230°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		2.7	3.3	5.25	V
High-level digital input voltage, V_{IH}		0.8 V_{DD}			V
Low-level digital input voltage, V_{IL}				0.8	V
Reference voltage, V_{ref} [A|B|C|D|E|F|G|H], X1 gain				V_{DD}–0.5	V
Load resistance, R_L		10			kΩ
Setup time, data input, $t_{su(DATA\text{-}CLK)}$ (see Figures 1 and 2)		50			ns
Valid time, data input valid after CLK↓, $t_{v(DATA\text{-}CLK)}$ (see Figures 1 and 2)		50			ns
Setup time, CLK eleventh falling edge to LOAD, $t_{su(CLK\text{-}LOAD)}$ (see Figure 1)		50			ns
Setup time, LOAD↑ to CLK↓, $t_{su(LOAD\text{-}CLK)}$ (see Figure 1)		50			ns
Pulse duration, LOAD, $t_{w(LOAD)}$ (see Figure 1)		250			ns
Pulse duration, LDAC, $t_{w(LDAC)}$ (see Figure 2)		250			ns
Setup time, LOAD↑ to LDAC↓, $t_{su(LOAD\text{-}LDAC)}$ (see Figure 2)		0			ns
CLK frequency				1	MHz
Operating free-air temperature, T_A	TLV5628C	0		70	°C
	TLV5628I	–40		85	°C

PRODUCT PREVIEW

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 3 V to 3.6 V, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current	$V_I = V_{DD}$			±10	µA
I_{IL}	Low-level digital input current	V_I = 0 V			±10	µA
$I_{O(sink)}$	Output sink current	Each DAC output	20			µA
$I_{O(source)}$	Output source current	Each DAC output	1			mA
C_i	Input capacitance			15		pF
C_i	Reference input capacitance			15		pF
I_{DD}	Supply current	V_{DD} = 3.3 V			4	mA
I_{ref}	Reference input current	V_{DD} = 3.3 V, V_{ref} = 1.5 V			±10	µA
E_L	Linearity error (end point corrected)	V_{ref} = 1.25 V, × 2 gain (see Note 1)			±1	LSB
E_D	Differential-linearity error	V_{ref} = 1.25 V, × 2 gain (see Note 2)			±0.9	LSB
E_{ZS}	Zero-scale error	V_{ref} = 1.25 V, × 2 gain (see Note 3)	0		30	mV
	Zero-scale error temperature coefficient	V_{ref} = 1.25 V, × 2 gain (see Note 4)		10		µV/°C
E_{FS}	Full-scale error	V_{ref} = 1.25 V, × 2 gain (see Note 5)			±60	mV
	Full-scale error temperature coefficient	V_{ref} = 1.25 V, × 2 gain (see Note 6)		±25		µV/°C
PSRR	Power-supply sensitivity	See Notes 7 and 8		0.5		mV/V

NOTES: 1. Integral nonlinearity (INL) is the maximum deviation of the output from the line between zero-scale and full scale (excluding the effects of zero code and full-scale errors).
2. Differential nonlinearity (DNL) is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
3. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
4. Zero-scale error temperature coefficient is given by: $ZSETC = [ZSE(T_{max}) - ZSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
5. Full-scale error is the deviation from the ideal full-scale output (V_{ref} – 1 LSB) with an output load of 10 kΩ.
6. Full-scale temperature coefficient is given by: $FSETC = [FSE(T_{max}) - FSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
7. Zero-scale error rejection ratio (ZSE-RR) is measured by varying the V_{DD} voltage from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
8. Full-scale error rejection ratio (FSE-RR) is measured by varing the V_{DD} from 3.0 V to 3.6 V dc and measuring the proportion of this signal imposed on the full-scale output voltage.

operating characteristics over recommended operating free-air temperature range, V_{DD} = 3 V to 3.6 V, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate	C_L = 100 pF, R_L = 10 kΩ		1		V/µs
Output settling time	To 0.5 LSB, C_L = 100 pF, R_L = 10 kΩ, See Note 9		10		µs
Large-signal bandwidth	Measured at –3 dB point		100		kHz
Digital crosstalk	CLK = 1-MHz square wave measured at DACA-DACH		–50		dB
Reference feedthrough	See Note 10		–60		dB
Channel-to-channel isolation	See Note 11		–60		dB
Reference input bandwidth	See Note 12		100		kHz

NOTES: 9. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 00 hex to FF hex or FF hex to 00 hex. For TLC5628C: V_{DD} = 5 V, V_{ref} = 2 V and range = ×2. For TLC5628I: V_{DD} = 3 V, V_{ref} = 1.25 V and range ×2.
10. Reference feedthrough is measured at any DAC output with an input code = 00 hex with a V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
11. Channel-to-channel isolation is measured by setting the input code of one DAC to FF hex and the code of all other DACs to 00 hex with V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
12. Reference bandwidth is the –3 dB bandwidth with an input at V_{ref} = 1.25 V dc + 2 V_{pp}, with a digital input code of full-scale.

PARAMETER MEASUREMENT INFORMATION

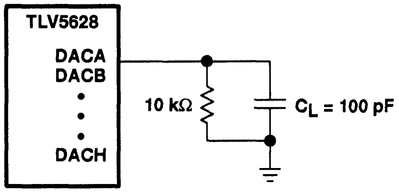
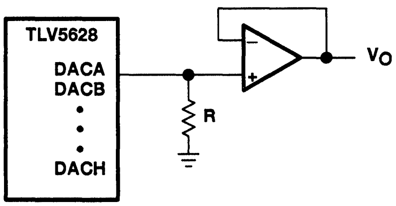


Figure 3. Slewing Settling Time and Linearity Measurements

APPLICATION INFORMATION



NOTE A: Resistor R ≥ 10 kΩ

Figure 4. Output Buffering Schemes

PRODUCT PREVIEW

- **Single 5-V Power Supply**
- **Sample Rates (F_S) up to 48 kHz**
- **18-Bit Resolution**
- **Pulse-Width-Modulation (PWM) Output**
- **Deemphasis Filter for Sample Rates of 32, 37.8, 44.1, and 48 kHz**
- **Mute With Zero-Data-Detect Flags**
- **Digital Attenuation to −60 dB**
- **Total Harmonic Distortion of 0.004% Maximum**
- **Total-Channel Dynamic Range of 96 dB Minimum**
- **Serial-Port Interface**
- **Differential Architecture**
- **CMOS Technology**
- **2s-Complement Data Format**

DWB PACKAGE
(TOP VIEW)

$\overline{\text{INIT}}$	1	28	DV_{DD}
TEST	2	27	L1
ATT	3	26	AV_{DDL}
SHIFT	4	25	L2
$\overline{\text{LATCH}}$	5	24	AGNDL
256FSO	6	23	XGND
TEST	7	22	XIN
DGND	8	21	XOUT
TEST	9	20	XV_{DD}
BCK	10	19	AGNDR
DATA	11	18	R2
LRCK	12	17	AV_{DDR}
$\overline{\text{MUTEL}}$	13	16	R1
$\overline{\text{MUTER}}$	14	15	DV_{DD}

description

The TMS57014A is a stereo, oversampled sigma-delta, digital-to-analog converter (DAC) designed for use in systems such as compact disks, digital audio tapes, multimedia, and video cassette recorders. The device provides high-resolution signal conversion. This device consists of two identical synchronous conversion paths for left and right audio channels. Other overhead functions provide on-chip timing and control.

Additional features include muting, attenuation, deemphasis, and zero-data detection. Control words (16-bit) from a host controller or processor implement these functions.

The TMS57014A is characterized for operation from 0°C to 70°C.

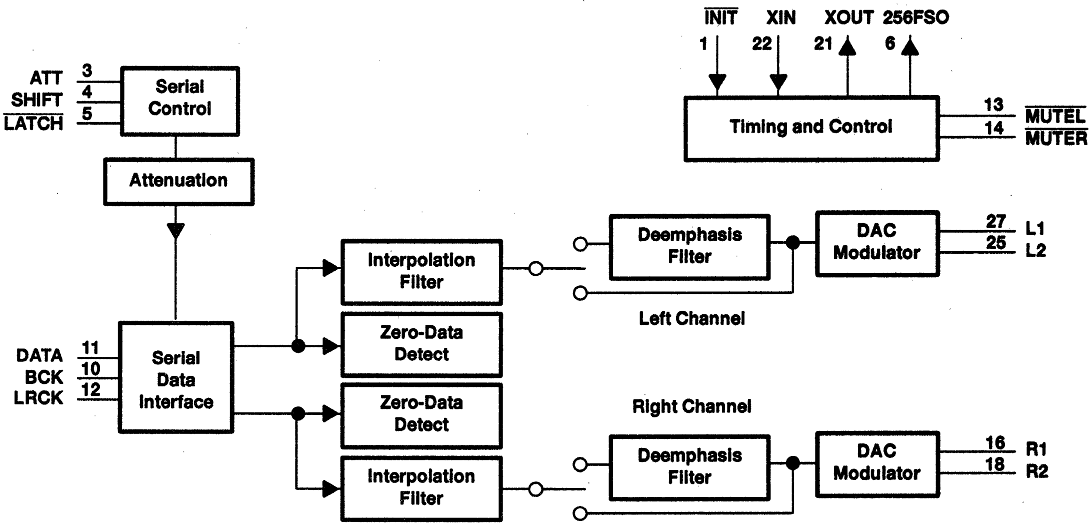
AVAILABLE OPTION†

T_A	PACKAGE SMALL OUTLINE (DWB)
0°C to 70°C	TMS57014ADWBLE

† Available on tape and reel (LE) only.

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ATT	3	I	Serial control data. ATT is a 16-bit word configured as LSB first (see Tables 2, 3, and 4).
AV_{DDL}	26	I	Analog power supply (left channel)
AV_{DDR}	17	I	Analog power supply (right channel)
AGNDL	24	I	Analog ground (left channel)
AGNDR	19	I	Analog ground (right channel)
BCK	10	I	Bit clock input. The shift clock signal clocks serial audio data into the device.
DATA	11	I	Audio data input. DATA can be configured as 16 or 18 bits with MSB or LSB first. DATA is 2s complement.
DV_{DD}	15, 28	I	Digital supply
DGND	8	I	Digital ground
$\overline{\text{INIT}}$	1	I	Reset. When $\overline{\text{INIT}}$ is brought low, the device is reset. The device is activated on the rising edge of $\overline{\text{INIT}}$. The LRCK signal must be applied to the device for a reset to occur.
$\overline{\text{LATCH}}$	5	I	Serial-control data latch. Control data loads into the internal registers when $\overline{\text{LATCH}}$ is brought low.
LRCK	12	I	Left/right clock. LRCK signifies whether the serial data is associated with the left-channel DAC (when high) or the right-channel DAC (when low).
$\overline{\text{MUTEL}}$	13	O	Left-channel mute flag active. When the left channel is mute or the data through the channel remains at zero for the system-register selected time, $\overline{\text{MUTEL}}$ is brought low.
$\overline{\text{MUTER}}$	14	O	Right-channel mute flag active. When the right channel is mute or the data through the channel remains at zero for the system-register selected time, $\overline{\text{MUTER}}$ is brought low.
L1	27	O	Left PWM output 1
L2	25	O	Left PWM output 2
R1	16	O	Right PWM output 1
R2	18	O	Right PWM output 2
SHIFT	4	I	Shift clock. SHIFT clocks the control data into the internal registers.
TEST	2, 7, 9	I	All TEST inputs should be tied low.
XIN	22	I	Master clock in. XIN derives all the key logic signals of the device. XIN runs at 512Fs, where F_S is the sample rate.
XOUT	21	O	Master clock out
XV_{DD}	20	I	Power supply for clock section
XGND	23	I	Ground for clock section
256FSO	6	O	System clock out. 256FSO reflects the master clock input divided by 2. The rate is 256Fs, where F_S is the sample rate.

detailed description

The TMS57014A incorporates an interpolation FIR filter and oversampled modulator. The pulse-width-modulation (PWM) digital output feeds into an external low-pass filter to recover the analog audio signal.

Two control registers configure the device, the attenuation register controls the attenuation range and the system register controls additional functions (see register set section).

reset/initialization

When $\overline{\text{INIT}}$ is brought low, an internal reset signal becomes active approximately 120 cycles of the sampling frequency (F_S) after the falling edge of $\overline{\text{INIT}}$. Under this condition, all internal circuits are initialized and the PWM output is held at zero data (50% duty cycle). When $\overline{\text{INIT}}$ is brought high, the internal reset signal goes inactive for a maximum of five LRCK periods after the rising edge of $\overline{\text{INIT}}$. At this point, internal clocks are synchronous with LRCK and the PWM output is valid (see Figure 1). The LRCK signal must be applied for proper initialization.

reset/initialization (continued)

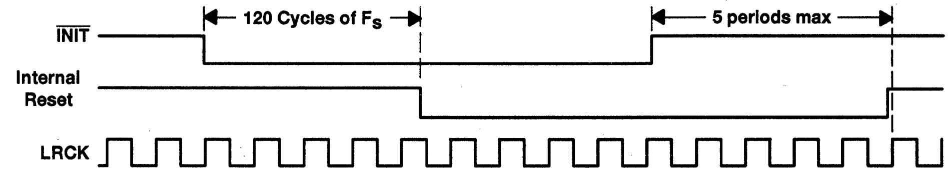


Figure 1. Reset Timing Relationships

timing and control

The timing and control circuit generates and distributes necessary clocks throughout this design. XIN is the external master clock input. The sample rate of the data paths is set as LRCK = XIN/512. With a fixed oversampling ratio of 32x and each PWM output value requiring 16 XIN cycles, the effect of changing XIN is shown in Table 1.

The DAC can be operated at any conversion rate between 48 kHz and 32 kHz by choosing the appropriate master-clock frequency. Some of the functions of the converter, such as the deemphasis filter, operate only at the frequencies in Table 1.

Table 1. Master Clock to Sample Rate Comparison

XIN (MHz)	256FSO (MHz)	LRCK (kHz)
24.5760	12.2880	48.0
22.5792	11.2896	44.1
19.3536	9.6768	37.8
16.3840	8.1920	32.0

digital audio data interface

The conversion cycle is synchronized to the rising edge of LRCK, and the data must meet the setup requirements specified in the timing requirements table. The input data is 16 or 18 bits with the MSB or LSB first as selected in the system register. The BCK frequency must be equal to or greater than 32 F_S for 16-bit data or 36 F_S for 18-bit data where F_S is the sample rate. Figure 2 illustrates the input timing.

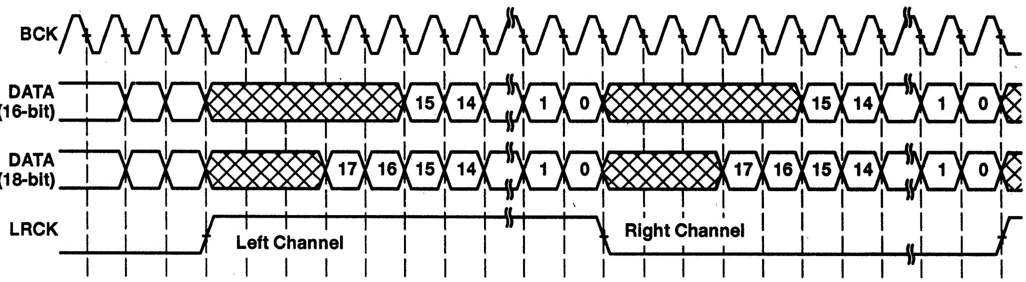


Figure 2. Audio-Data Input Timing

serial-control interface

This device uses the most-significant-bit-first format. Therefore, for a 16-bit word, D15 is the most significant bit and D0 is the least significant bit. Unless otherwise specified, all values are in 2s-complement format.

serial-control-data input

The 16-bit control-data input implements the device-control functions. The TMS57014A has two registers for this data: the system register and the attenuation register. The system register contains most of the system configuration information, and the attenuation register controls audio output level, deemphasis, and mute. Figure 3 illustrates the input timing for $\overline{\text{ATT}}$, $\overline{\text{SHIFT}}$, and $\overline{\text{LATCH}}$. The data loads internally on the falling edge of $\overline{\text{LATCH}}$. The shift clock should be high for the $\overline{\text{LATCH}}$ setup time before $\overline{\text{LATCH}}$ goes low.

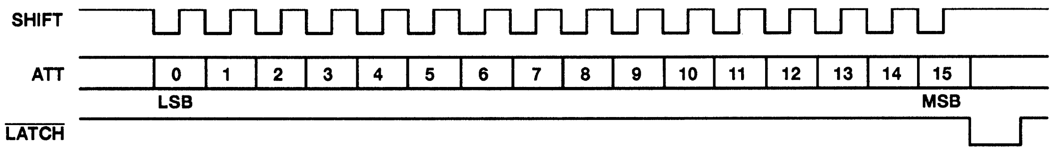


Figure 3. Control-Data-Input Timing

mute

When mute is activated, the output PWM becomes zero data (50% duty cycle). The two mute flags, $\overline{\text{MUTEL}}$ and $\overline{\text{MUTER}}$, are independently set low based on the data in the respective channel being zero. This function becomes active under the following conditions:

1. When the zero-data detector detects that the input data has been zero for 2500 cycles of F_S or 12500 cycles of F_S (as selected in the control registers), output is 50% duty cycle.
2. When the MUTE register value is set high by means of the serial-control data.
3. When $\overline{\text{INIT}}$ is active (low), output is 50% duty cycle.

zero-data detect

After the input data remains zero for 2500 or 12500 cycles of F_S as set by the system register (D4, D5), the channel-mute flag becomes active. Zero-data detection is available for both channels independently, so the two outputs ($\overline{\text{MUTER}}$ and $\overline{\text{MUTEL}}$) indicate that zero data has been detected on the respective channel. The zero-detect register value in the serial-control data selects the detection period. The mute flag returns high immediately when nonzero input data is received.

deemphasis filter

Four sets of deemphasis-filter coefficients support four sampling rates (F_S): 32, 37.8, 44.1, and 48 kHz. Internal register values select the filter coefficients. The internal register values enable or disable the filter. Figure 4 illustrates the deemphasis characteristics.

Many audio sources have been recorded with preemphasis characteristics that are the inverse of the deemphasis characteristics shown in Figure 4. This device provides reconstruction of the original frequency response.

deemphasis filter (continued)

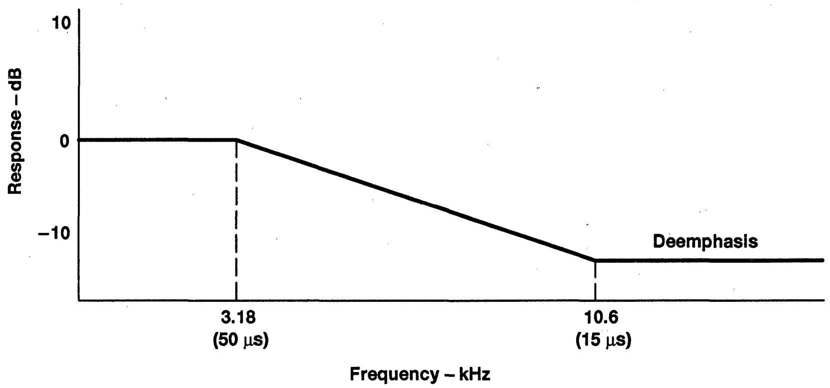


Figure 4. Deemphasis Characteristics

digital attenuation

A value selected in the internal attenuation register determines the attenuation of the digital-audio-data input. The attenuation value is 11 bits long with a valid range of hex values from 400h to 000h. A data value of 001h corresponds to an attenuation value of –60 dB and a data value of 400h corresponds to 0 dB. The attenuation function is nonlinear (see equation 1). Figure 5 demonstrates the attenuation function in dB. The default attenuation value is 400h.

$$\text{Attenuation} = 20 \log \left(\frac{\text{attenuation data}}{1024} \right) \tag{1}$$

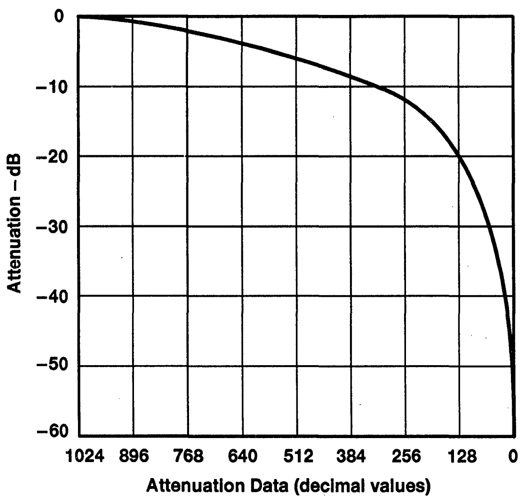


Figure 5. Digital Attenuation Characteristics

register set

Table 2 contains the register-set selection. Tables 3 and 4 list the bit functions.

Table 2. Register-Set Selection

BITS 15	BITS 14	DESCRIPTION
0	0	Attenuation register
0	1	System register
1	x	Invalid condition†

† Bit 15 should always be set to 0 when writing data for proper operation.

Table 3. Attenuation-Register Bit Functions

BITS 13	12	11	10–0	FUNCTION
0	—	—	—	Deemphasis off
1	—	—	—	Deemphasis on
—	0	—	—	Channel mute off
—	1	—	—	Channel mute on
—	—	0	—	Bit 11 must be low
—	—	—	0	Digital attenuation, mute
—	—	—	1	Digital attenuation, –60.2 dB
—	—	—	2	Digital attenuation, –54.2 dB
—	—	—	3	Digital attenuation, –50.7 dB
—	—	—	. . .	
—	—	—	1FF	Digital attenuation, –6.04 dB
—	—	—	200	Digital attenuation, –6.02 dB
—	—	—	201	Digital attenuation, –6.00 dB
—	—	—	. . .	
—	—	—	3FF	Digital attenuation, –0.01 dB
—	—	—	400	Digital attenuation, 0.00 dB

default 0400h

NOTE: The attenuation values shown are typical values. Refer to the digital attenuation section for a description of the attenuation function.

Table 4. System-Register Bit Functions

BITS								FUNCTION
13	12	11–6	5	4	3–2	1	0	
0	—	—	—	—	—	—	—	MSB first, audio data
1	—	—	—	—	—	—	—	LSB first, audio data
—	0	—	—	—	—	—	—	16-bit, audio data
—	1	—	—	—	—	—	—	18-bit, audio data
—	—	0	—	—	—	—	—	Bits 11–6 must be low
—	—	—	0	—	—	—	—	Zero data detect period (2500 cycles of F_S)
—	—	—	1	—	—	—	—	Zero data detect period (12500 cycles of F_S)
—	—	—	—	0	—	—	—	Bit 4 must be low
—	—	—	—	—	0	—	—	Deemphasis –44.1 kHz
—	—	—	—	—	1	—	—	Deemphasis –48.0 kHz
—	—	—	—	—	2	—	—	Deemphasis –37.8 kHz
—	—	—	—	—	3	—	—	Deemphasis –32.0 kHz
—	—	—	—	—	—	0	—	LRCK and PWM are not synchronized
—	—	—	—	—	—	1	—	LRCK and PWM synchronized
—	—	—	—	—	—	—	0	Bit 0 must be low

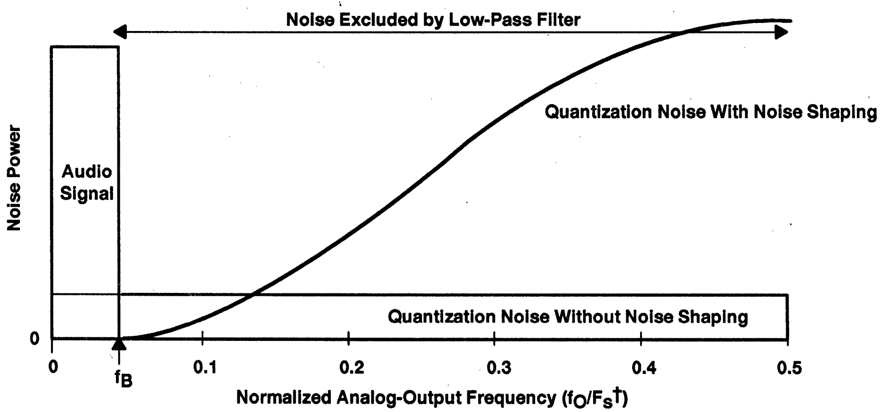
Default = 0000h

interpolation filter

The interpolation filter used prior to the DAC increases the digital data rate from the LRCK speed to the oversampled rate by interpolating with a ratio of 1:32. The oversampling modulator receives the output of this filter with deemphasis as an option.

DAC modulator

The DAC is a 3rd-order modulator with 32 times oversampling. The DAC provides high-resolution, low-noise performance using a 15-value PWM output as shown in Figure 6.



† f_O is the output frequency at the low-pass filter output (V_O) shown in Figure 10.

Figure 6. Oversampling Noise Power With and Without Noise Shaping

PWM output (L2–L1 and R2–R1)

The L2–L1 and the R2–R1 output pairs are pulse-width-modulated (PWM) signals with the L2–L1 differential pulse duration determining the left-channel analog voltage and the R2–R1 differential pulse duration determining the right-channel analog voltage.

Each DAC left and right output consists of 15 levels of PWM and provides a differential signal as the input to two external differential amplifiers configured as a low-pass filter to produce the left and right audio outputs (see Figure 9).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Analog supply voltage range, AV_{DDL}, AV_{DDR} (see Note 1) . . . . −0.3 V to 7 V
Digital supply voltage range, DV_{DD} (see Note 2) . . . . −0.3 V to 7 V
Clock supply voltage range, XV_{DD} (see Note 3) . . . . −0.3 V to 7 V
Output voltage range, V_O: L1, L2 . . . . −0.3 V to AV_{DDL} + 0.3 V
R1, R2 . . . . −0.3 V to AV_{DDR} + 0.3 V
Input voltage range, V_I . . . . −0.3 V to DV_{DD} + 0.3 V
Operating free-air temperature range, T_A . . . . 0°C to 70°C
Case temperature for 10 seconds, T_C . . . . 260°C
Storage temperature range, T_{stg} . . . . −55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values for maximum ratings are with respect to AGNDL and AGNDR respectively.
2. Voltage values for maximum ratings are with respect to DGND.
3. Voltage values for maximum ratings are with respect to XGND.

recommended operating conditions (see Note 4)

		MIN	NOM	MAX	UNIT
Analog supply voltage, AV_{DDL}, AV_{DDR}		4.75	5	5.25	V
Digital supply voltage, DV_{DD}		4.75	5	5.25	V
Clock supply voltage, XV_{DD}		4.75	5	5.25	V
High-level input voltage, V_{IH}	XIN	0.9 V_{DD}			V
	All other digital inputs	0.76 V_{DD}			
Low-level input voltage, V_{IL}	XIN			0.1 V_{DD}	V
	All other digital inputs			0.24 V_{DD}	
Load resistance at PWM, R_L			10		kΩ
Master clock frequency at XIN		16.3		24.6	MHz
Operating free-air temperature, T_A		0		70	°C

NOTE 4: DV_{DD}, AV_{DDL}, XV_{DD} and AV_{DDR} tied together represents V_{DD}.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

digital interface, $AV_{DD} = DV_{DD} = 5\ V \pm 5\%$ (see Note 4)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	256FSO	$I_O = -0.4$ mA	$V_{DD}-0.5$			V
		L1, L2, R1, R2	$I_O = -12$ mA	$V_{DD}-0.5$			
		XOUT	$I_O = -1.2$ mA	$V_{DD}-0.5$			
		$\overline{MUTEL}$, $\overline{MUTER}$	$I_O = -1$ mA	$V_{DD}-0.5$			
V_{OL}	Low-level output voltage	256FSO	$I_O = 0.4$ mA			0.4	V
		L1, L2, R1, R2	$I_O = 12$ mA			0.5	
		XOUT	$I_O = 1.2$ mA			0.5	
		$\overline{MUTEL}$, $\overline{MUTER}$	$I_O = 1$ mA			0.4	
I_{IH}	High-level input current, any digital input				±1	±5	µA
I_{IL}	Low-level input current, any digital input				±1	±5	µA
C_i	Input capacitance				5		pF
C_o	Output capacitance				5		pF

† All typical values are at $T_A = 25°C$.
NOTE 4: DV_{DD}, AV_{DDL}, XV_{DD} and AV_{DDR} tied together represents V_{DD}.

supplies, $AV_{DD} = DV_{DD} = 5\ V \pm 5\%$, no load

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Analog power supply current	AV_{DDL} and AV_{DDR} are shorted together		15		mA
Digital power supply current			15		mA
Total device supply current over operating temperature range				60	mA
Power dissipation				350	mW

† All typical values are at $T_A = 25°C$.

DAC modulator, $AV_{DD} = DV_{DD} = 5\ V \pm 5\%$, sample rate ($F_s$) = 44.1 kHz, full-scale input sine wave at 1 kHz, $T_A = 25°C$, bandwidth is 20 Hz to 20 kHz

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Resolution	See Note 5		18			bits
Signal-to-noise ratio	A-weighted, 20 Hz to 20 kHz, See Figure 10, Table 5, and Note 5	Deemphasis not selected	96	100		dB
Total harmonic distortion	20 Hz to 20 kHz, See Note 5			0.003%	0.004%	

† All typical values are at $T_A = 25°C$.
NOTE 5: These specifications are measured at the output (V_O) of the low-pass filter shown in Figure 9.

filter characteristics, $AV_{DD} = DV_{DD} = 5\ V \pm 5\%$, deemphasis disabled

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Pass-band ripple	Sample rate (F_s) = 48 kHz, See Note 5	−0.002		0.002	dB
Stop-band attenuation		75			dB
Pass band (−3 dB) (DAC)	See Note 5	0		0.46 F_s	kHz
Stop band		0.54 F_s			kHz
Group delay			29/F_s		s

† All typical values are at $T_A = 25°C$.
NOTE 5: These specifications are measured at the output (V_O) of the low-pass filter shown in Figure 7.

timing requirements (see Figures 8 and 9 and Note 6)

		MIN	MAX	UNIT
t_{w1}	Pulse duration, BCK	160		ns
t_{su1}	Setup time, DATA before BCK↑	20		ns
t_{h1}	Hold time, DATA after BCK↑	20		ns
t_{su2}	Setup time, LRCK before BCK↑	50		ns
t_{h2}	Hold time, LRCK after BCK↑	50		ns
t_{w2}	Pulse duration, SHIFT	100		ns
t_{su3}	Setup time, ATT before SHIFT↑	20		ns
t_{h3}	Hold time, ATT after SHIFT↑	20		ns
t_{w3}	Pulse duration, $\overline{\text{LATCH}}$	100		ns
t_{su4}	Setup time, $\overline{\text{LATCH}}$ before SHIFT↑	100		ns
t_{h4}	Hold time, $\overline{\text{LATCH}}$ after SHIFT↑	t_{w2} + 20		ns

NOTE 6: All timing measurements were taken at the $V_{DD}/2$ voltage level.

PARAMETER MEASUREMENT INFORMATION

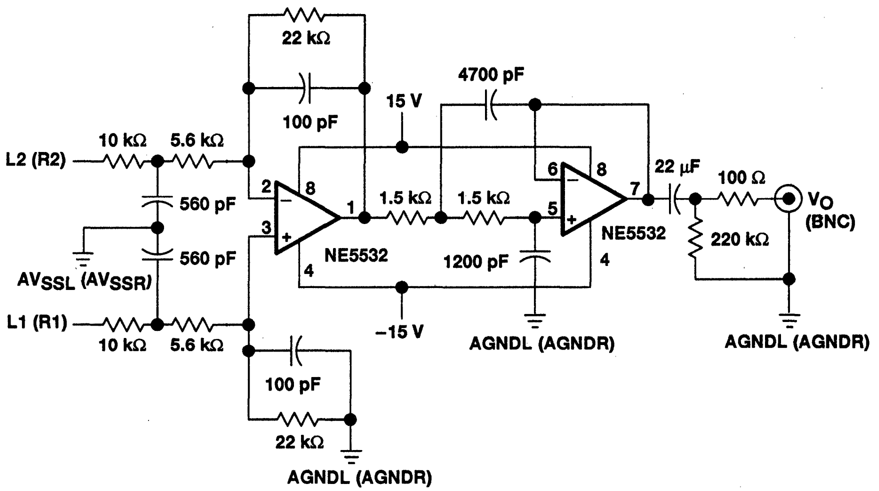


Figure 7. Analog Low-Pass Filter Recommended for Measuring the Dynamic Specifications of the TMS57014A

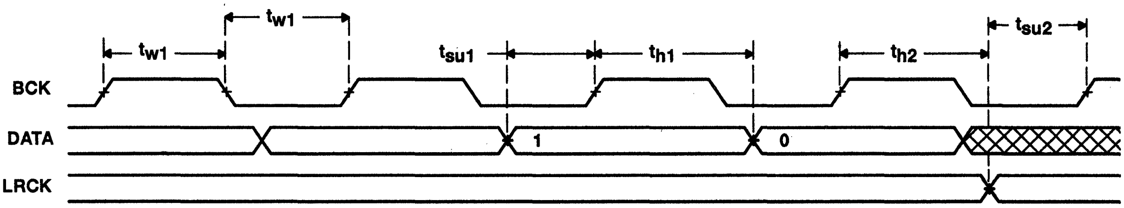


Figure 8. Audio-Data Serial Timing

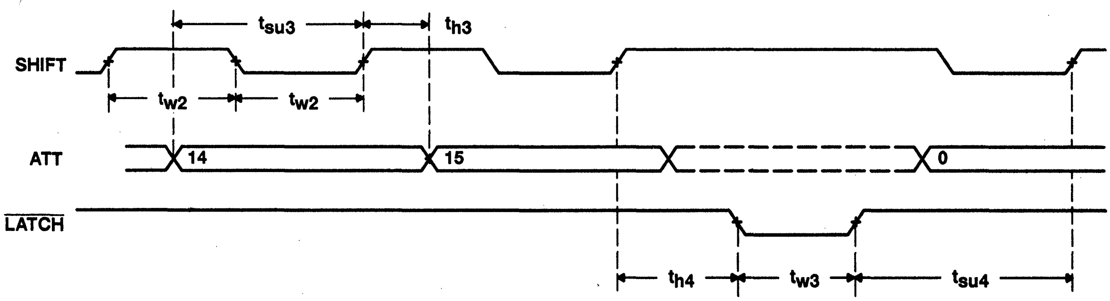


Figure 9. Control-Data Serial Timing

PARAMETER MEASUREMENT INFORMATION

Table 5. A-Weighted Data

FREQUENCY	A WEIGHTING (dB)	FREQUENCY	A WEIGHTING (dB)
25	−44.6 ±2	800	−0.1 ±1
31.5	−39.2 ±2	1000	0 ±0
40	−34.5 ±2	1250	0.6 ±1
50	−30.2 ±2	1600	1.0 ±1
63	−26.1 ±2	2000	1.2 ±1
80	−22.3 ±2	2500	1.2 ±1
100	−19.1 ±1	3150	1.2 ±1
125	−16.1 ±1	4000	1.0 ±1
160	−13.2 ±1	5000	0.5 ±1
200	−10.8 ±1	6300	−0.1 ±1
250	−8.6 ±1	8000	−1.1 ±1
315	−6.5 ±1	10000	−2.4 ±1
400	−4.8 ±1	12500	−4.2 ±2
500	−3.2 ±1	16000	−6.5 ±2
630	−1.9 ±1		

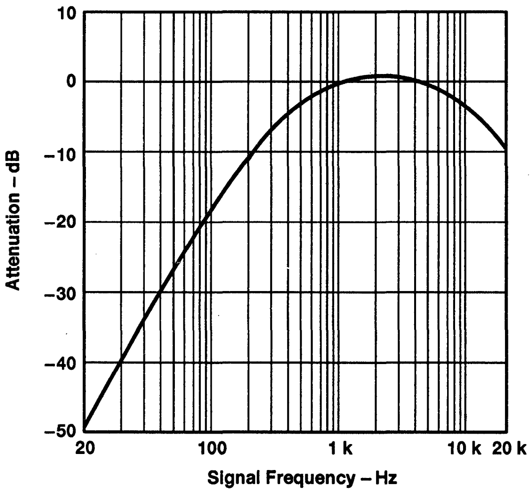


Figure 10. A-Weighted Function

APPLICATION INFORMATION

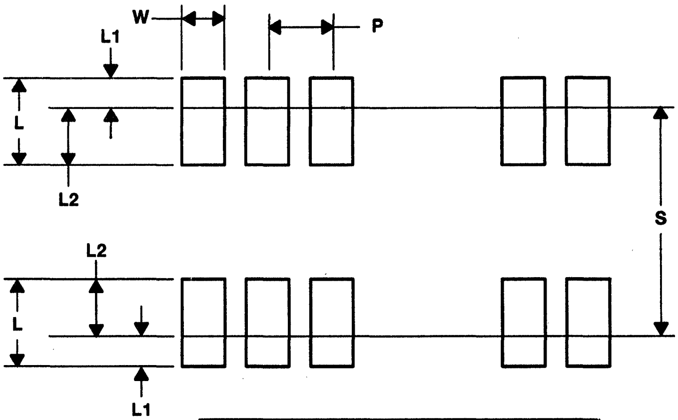
circuit and layout considerations

The designer should follow these guidelines for the best device performance.

- Separate digital and analog ground planes should be used. All digital device functions should be over the digital ground plane, and all analog device functions should be over the analog ground plane. The ground planes should be connected at only one point to the direct power supply, and this is usually at the connector edge of the board.
- A single crystal-controlled clock should synchronously generate all digital signals
- All power supply lines should include a 0.1-µF and a 1-µF capacitor. If clock noise is excessive, a toroidal inductance of 10 µH should be placed in series with XV_{DD} before connecting to DV_{DD}.
- The digital input control signals should be buffered if they are generated off the card.
- Clock jitter should be minimized, and precautions taken to prevent clock overshoot. This minimizes any high-frequency coupling to the analog output.

PCB footprint

Figure 11 shows the printed-circuit-board (PCB) land pattern for the TMS57014A small-outline package.



P	S	W	L	L1	L2
1.27	9.53	0.76	1.55	0.64	0.91

NOTE A: All linear dimensions are in millimeters.

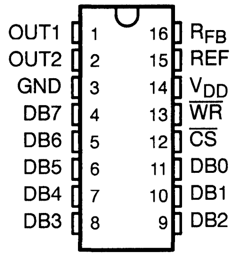
Figure 11. Land Pattern for PCB Layout

AD7524M
Advanced LinCMOS™ 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

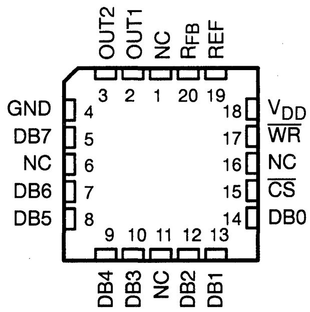
SGLS028A – SEPTEMBER 1989 – REVISED MARCH 1995

- **Advanced LinCMOS™ Silicon-Gate Technology**
- **Easily Interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Monotonicity Over Entire A/D Conversion Range**
- **Segmented High-Order Bits Ensure Low-Glitch Output**
- **Designed to Be Interchangeable With Analog Devices AD7524, PMI PM-7524, and Micro Power Systems MP7524**
- **Fast Control Signaling for Digital Signal Processor Applications Including Interface With SMJ320**

J PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC–No internal connection

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 Bits
Linearity error	1/2 LSB Max
Power dissipation at V_{DD} = 5 V	5 mW Max
Settling time	100 ns Max
Propagation delay	80 ns Max

description

The AD7524M is an Advanced LinCMOS™ 8-bit digital-to-analog converter (DAC) designed for easy interface to most popular microprocessors.

The AD7524M is an 8-bit multiplying DAC with input latches and with a load cycle similar to the write cycle of a random access memory. Segmenting the high-order bits minimizes glitches during changes in the most-significant bits, which produce the highest glitch impulse. The AD7524M provides accuracy to 1/2 LSB without the need for thin-film resistors or laser trimming, while dissipating less than 5 mW typically.

Featuring operation from a 5-V to 15-V single supply, the AD7524M interfaces easily to most microprocessor buses or output ports. Excellent multiplying (2 or 4 quadrant) makes the AD7524M an ideal choice for many microprocessor-controlled gain-setting and signal-control applications.

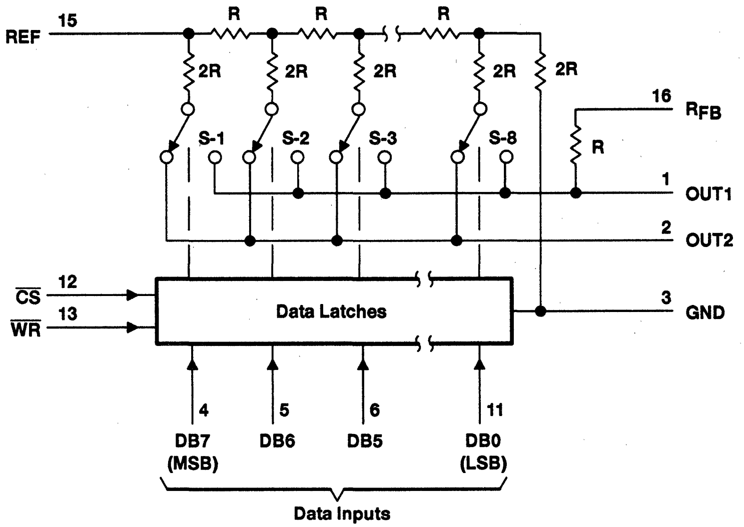
The AD7524M is characterized for operation from –55°C to 125°C.

AVAILABLE OPTIONS

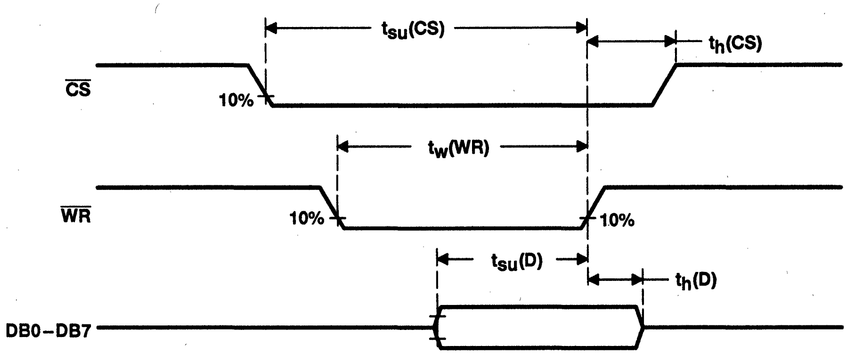
T_A	PACKAGE	
	CERAMIC CHIP CARRIER (FK)	CERAMIC DIP (J)
–55°C to 125°C	AD7524MFK	AD7524MJ

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} .... −0.3 V to 17 V
Voltage between R_{FB} and GND .... ±25 V
Digital input voltage range, V_I .... −0.3 V to V_{DD}+0.3 V
Reference voltage range, V_{ref} .... ±25 V
Peak digital input current, I_I .... 10 μA
Operating free-air temperature range, T_A .... −55°C to 125°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Case temperature for 60 seconds, T_C: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package .... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}	4.75	5	5.25	14.5	15	15.5	V
Reference voltage, V_{ref}		±10			±10		V
High-level input voltage, V_{IH}	2.4			13.5			V
Low-level input volage, V_{IL}			0.8			1.5	V
$\overline{CS}$ setup time, $t_{su(CS)}$	40			40			ns
$\overline{CS}$ hold time, $t_{h(CS)}$	0			0			ns
Data bus input setup time, $t_{su(D)}$	25			25			ns
Data bus input hold time, $t_{h(D)}$	10			10			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$	40			40			ns
Operating free-air temperature, T_A	−55		125	−55		125	°C

electrical characteristics over recommended operating free-air temperature range, V_{ref} = 10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 15 V MIN	V_{DD} = 15 V TYP	V_{DD} = 15 V MAX	UNIT
I_{IH}	High-level input current		$V_I = V_{DD}$	Full-range			10			10	µA
				25°C			1			1	
I_{IL}	Low-level input current		V_I = 0	Full-range			−10			−10	µA
				25°C			−1			−1	
I_{pkg}	Output leakage current	OUT1	DB0–DB7 at 0, $\overline{WR}$ and $\overline{CS}$ at 0 V	Full-range			±400			±200	nA
			V_{ref} = ±10 V	25°C			±50			±50	
		OUT2	DB0–DB7 at V_{DD}, $\overline{WR}$ and $\overline{CS}$ at 0	Full-range			±400			±200	
			V_{ref} = ±10 V	25°C			±50			±50	
I_{DD}	Supply current	Quiescent	DB0–DB7 at V_{IH}min or V_{IL}max				2			2	mA
		Standby	DB0–DB7 at 0 V or V_{DD}	Full-range			500			500	µA
				25°C			100			100	
k_{SVS}	Supply voltage sensitivity, $\Delta gain/\Delta V_{DD}$		ΔV_{DD} = 10%	Full-range			0.16			0.04	%/%
				25°C		0.002	0.02		0.001	0.02	pF
C_i	Input capacitance, DB0–DB7, $\overline{WR}$, $\overline{CS}$		V_I = 0				5			5	pF
C_o	Output capacitance	OUT1	DB0–DB7 at 0, $\overline{WR}$ and $\overline{CS}$ at 0 V				30			30	pF
		OUT2					120			120	
		OUT1	DB0–DB7 at V_{DD}, $\overline{WR}$ and $\overline{CS}$ at 0 V				120			120	
		OUT2					30			30	
	Reference input impedance (REF to GND)				5		20	5		20	kΩ

operating characteristics over recommended operating free-air temperature range, V_{ref} = 10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC} = 5 V MIN	V_{CC} = 5 V MAX	V_{DD} = 15 V MIN	V_{DD} = 15 V MAX	UNIT
Linearity error				±0.2		±0.2	%FSR
Gain error	See Note 1	Full range		±1.4		±0.6	%FSR
		25°C		±1		±0.5	
Settling time (to 1/2 LSB)	See Note 2			100		100	ns
Propagation delay from digital input to 90% of final analog output current	See Note 2			80		80	ns
Feedthrough at OUT1 or OUT2	V_{ref} = ±10 V (100 kHz sinewave), $\overline{WR}$ and $\overline{CS}$ at 0, DB0–DB7 at 0	Full range		0.5		0.5	%FSR
		25°C		0.25		0.25	
Temperature coefficient of gain	T_A = 25°C to t_{min} or t_{max}			±0.004		±0.001	%FSR/°C

NOTES: 1. Gain error is measured using the internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB.
2. OUT1 load = 100 Ω, C_{ext} = 13 pF, $\overline{WR}$ at 0 V, $\overline{CS}$ at 0 V, DB0–DB7 at 0 V to V_{DD} or V_{DD} to 0 V.

PRINCIPLES OF OPERATION

The AD7524M is an 8-bit multiplying D/A converter consisting of an inverted R-2R ladder, analog switches, and data input latches. Binary weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state. The high-order bits are decoded and these decoded bits, through a modification in the R-2R ladder, control three equally weighted current sources. Most applications only require the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is seen in Figure 1. With all digital inputs low, the entire reference current, I_{ref}, is switched to OUT2. The current source 1/256 represents the constant current flowing through the termination resistor of the R-2R ladder, while the current source I_{lkg} represents leakage currents to the substrate. The capacitances appearing at OUT1 and OUT2 are dependent upon the digital input code. With all digital inputs high, the off-state switch capacitance (30 pF maximum) appears at OUT2 and the on-state switch capacitance (120 pF maximum) appears at OUT1. With all digital inputs low, the situation is reversed as shown in Figure 1. Analysis of the circuit for all digital inputs high is similar to Figure 1; however, in this case, I_{ref} would be switched to OUT1.

Interfacing the AD7524M D/A converter to a microprocessor is accomplished via the data bus and the $\overline{CS}$ and $\overline{WR}$ control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the AD7524M analog output responds to the data activity on the DB0–DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the CS signal or WR signal goes high, the data on the DB0–DB7 inputs are latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The AD7524M is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figures 2 and 3. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

PRINCIPLES OF OPERATION

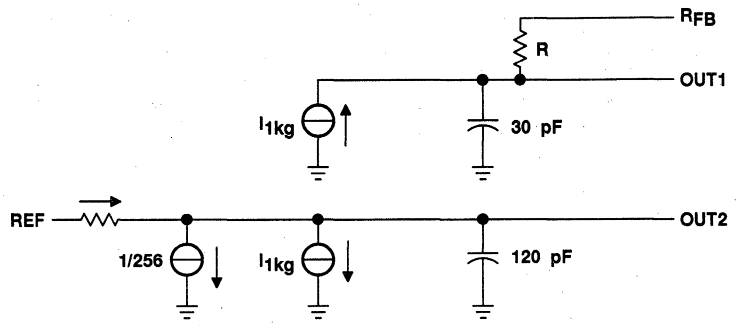


Figure 1. AD7524M Equivalent Circuit With All Digital Inputs Low

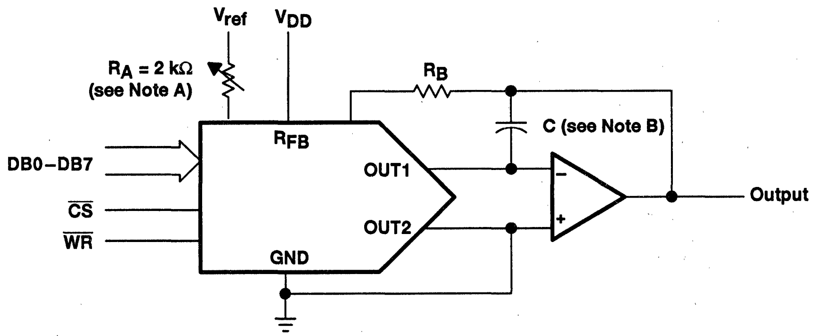


Figure 2. Unipolar Operation (2-Quadrant Multiplication)

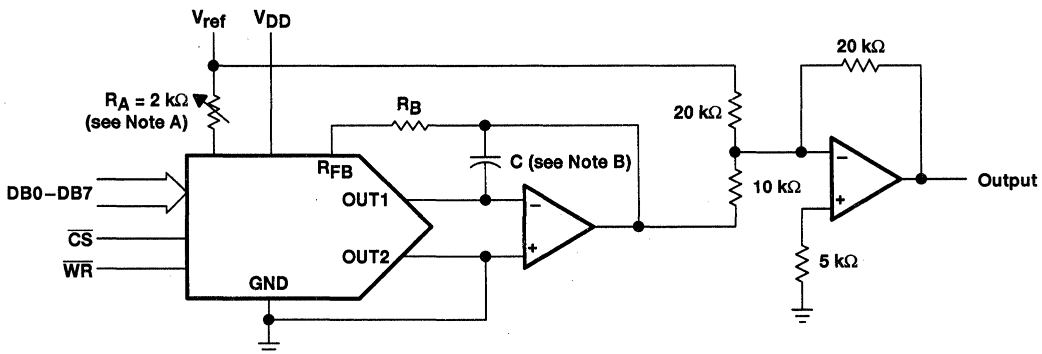


Figure 3. Bipolar Operation (4-Quadrant Operation)

NOTES: A. R_A and R_B used only if gain adjustment is required.
B. C phase compensation (10 – 15 pF) is required when using high-speed amplifiers to prevent ringing or oscillation.

PRINCIPLES OF OPERATION

Table 1. Unipolar Binary Code

DIGITAL INPUT (SEE NOTE 3) MSB LSB	ANALOG OUTPUT
11111111	$-V_{ref}$ (255/256)
10000001	$-V_{ref}$ (129/256)
10000000	$-V_{ref}$ (128/256) = $-V_{ref}/2$
01111111	$-V_{ref}$ (127/256)
00000001	$-V_{ref}$ (1/256)
00000000	0

Table 2. Bipolar (Offset Binary) Code

DIGITAL INPUT (SEE NOTE 4) MSB LSB	ANALOG OUTPUT
11111111	V_{ref} (127/128)
10000001	V_{ref} (128)
10000000	0
01111111	$-V_{ref}$ (128)
00000001	$-V_{ref}$ (127/128)
00000000	$-V_{ref}$

NOTES: 3. LSB = 1/256 (V_{ref}).
4. LSB = 1/128 (V_{ref}).

microprocessor interfaces

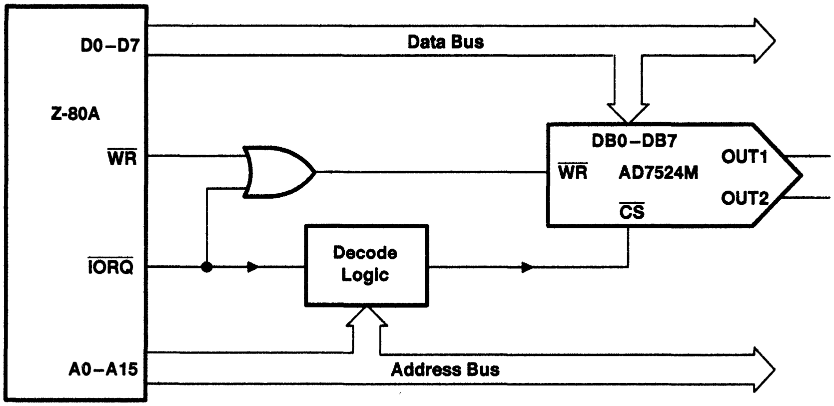


Figure 4. AD7524M–Z-80A Interface

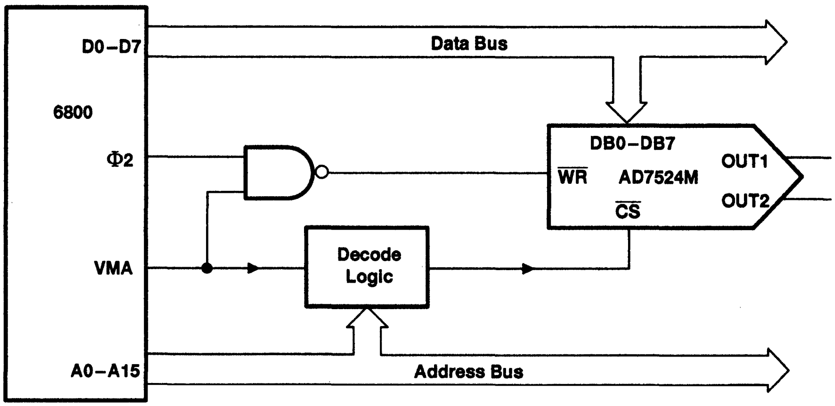


Figure 5. AD7524M–6800 Interface

microprocessor interfaces (continued)

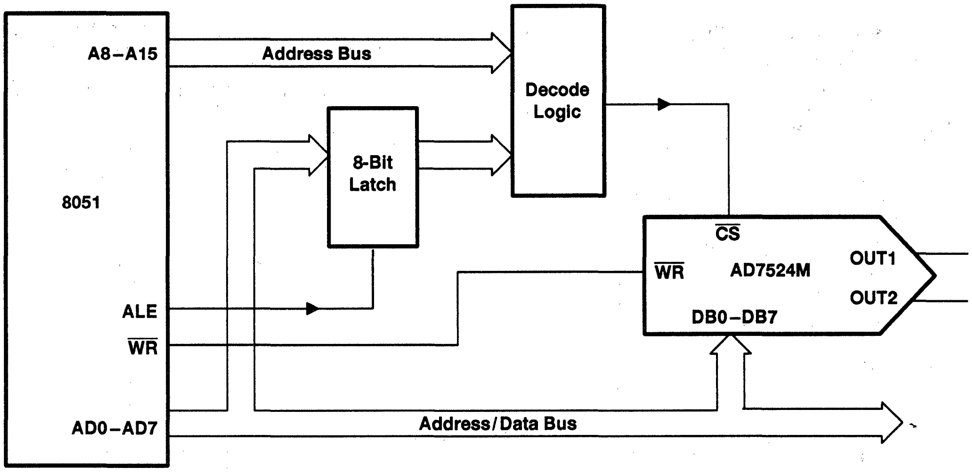


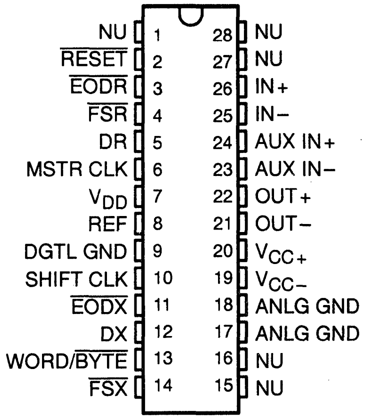
Figure 6. AD7524M–8051 Interface

TLC32040C, TLC32040I, TLC32041C, TLC32041I ANALOG INTERFACE CIRCUITS

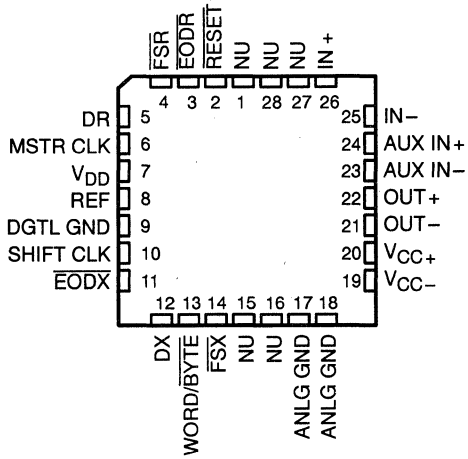
SLAS014E – SEPTEMBER 1987 – REVISED MAY 1995

- **14-Bit Dynamic Range ADC and DAC**
- **Variable ADC and DAC Sampling Rate Up to 19,200 Samples per Second**
- **Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter**
- **Serial Port for Direct Interface to TMS32011, TMS320C17, TMS32020, and TMS320C25 Digital Signal Process**
- **Synchronous or Asynchronous ADC and DAC Conversion Rate With Programmable Incremental ADC and DAC Conversion Timing Adjustments**
- **Serial Port Interface to SN74299 Serial-to-Parallel Shift Register for Parallel Interface to TMS32010, TMS320C15, or Other Digital Processors**
- **600-Mil Wide N Package (C_L to C_L)**
- **2s Complement Format**
- **CMOS Technology**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NU – Nonusable; no external connection should be made to these terminals.

PART NUMBER	DESCRIPTION
TLC32040	Analog interface circuit with internal reference. Also a plug-in replacement for TLC32041.
TLC32041	Analog interface circuit without internal reference

description

The TLC32040 and TLC32041 are complete analog-to-digital and digital-to-analog input/output systems, each on a single monolithic CMOS chip. This device integrates a bandpass switched-capacitor antialiasing input filter, a 14-bit-resolution A/D converter, four microprocessor-compatible serial port modes, a 14-bit-resolution D/A converter, and a low-pass switched-capacitor output-reconstruction filter.

AVAILABLE OPTIONS

T_A	PACKAGE	
	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	TLC32040CFN TLC32041CFN	TLC32040CN TLC32041CN
−40°C to 85°C		TLC32040IN TLC32041IN

description (continued)

The device offers numerous combinations of master clock input frequencies and conversion/sampling rates, which can be changed via digital processor control.

Typical applications for this integrated circuit include modems (7.2-, 8-, 9.6-, 14.4-, and 19.2-kHz sampling rate), analog interface for digital signal processors (DSPs), speech recognition/storage systems, industrial process control, biomedical instrumentation, acoustical signal processing, spectral analysis, data acquisition, and instrumentation recorders. Four serial modes, which allow direct interface to the TMS32011, TMS320C17, TMS32020, and TMS320C25 digital signal processors, are provided. Also, when the transmit and receive sections of the analog interface circuit (AIC) are operating synchronously, it can interface to two SN74299 serial-to-parallel shift registers. These serial-to-parallel shift registers can then interface in parallel to the TMS32010, TMS320C15, other digital signal processors, or external FIFO circuitry. Output data pulses are emitted to inform the processor that data transmission is complete or to allow the DSP to differentiate between two transmitted bytes. A flexible control scheme is provided so that the functions of this integrated circuit can be selected and adjusted coincidentally with signal processing via software control.

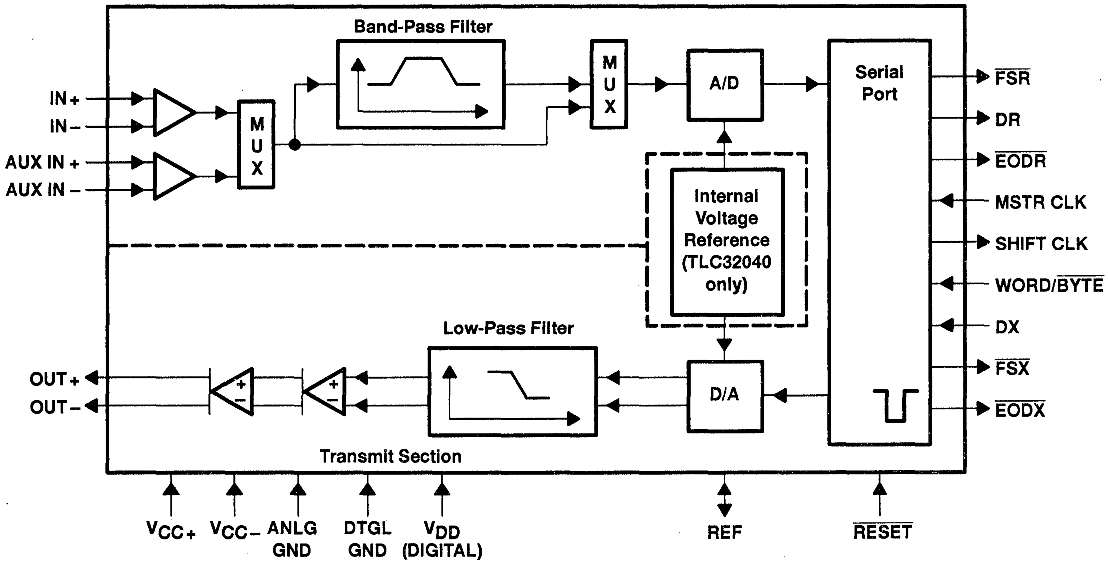
The antialiasing input filter comprises seventh-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively and a fourth-order equalizer. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When no filtering is desired, the entire composite filter can be switched out of the signal path. A selectable, auxiliary, differential analog input is provided for applications where more than one analog input is required.

The A/D and D/A converters each have 14 bits of resolution. The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided on the TLC32040 to ease the design task and to provide complete control over the performance of this integrated circuit. The internal voltage reference is brought out to a terminal and is available to the designer. Separate analog and digital voltage supplies and grounds are provided to minimize noise and ensure a wide dynamic range. Also, the analog circuit path contains only differential circuitry to keep noise to an absolute minimum. The only exception is the DAC sample and hold, which utilizes pseudo-differential circuitry.

The output-reconstruction filter is a seventh-order CC-type (Chebyshev/elliptic transitional low-pass filter followed by a fourth-order equalizer) and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the digitally encoded signal.

The TLC32040C and TLC32041C are characterized for operation from 0°C to 70°C, and the TLC32040I and TLC32041I are characterized for operation from −40°C to 85°C.

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ANLG GND	17,18		Analog ground return for all internal analog circuits. Not internally connected to DGTL GND.
AUX IN+	24	I	Noninverting auxiliary analog input state. This input can be switched into the bandpass filter and A/D converter path via software control. If the appropriate bit in the control register is a 1, the auxiliary inputs replace the IN+ and IN– inputs. If the bit is a 0, the IN+ and IN– inputs are used (see the AIC DX data word format section).
AUX IN–	23	I	Inverting auxiliary analog input (see the above AUX IN+ description)
DGTL GND	9		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
DR	5	O	DR is used to transmit the ADC output bits from the AIC to the TMS320 serial port. This transmission of bits from the AIC to the TMS320 serial port is synchronized with the SHIFT CLK signal.
DX	12	I	DX is used to receive the DAC input bits and timing and control information from the TMS320. This serial transmission from the TMS320 serial port to the AIC is synchronized with the SHIFT CLK signal.
EODR	3	O	End of data receive. See the WORD/BYTE description and the Serial Port Timing diagrams. During the word-mode timing, EODR is a low-going pulse that occurs immediately after the 16 bits of A/D information have been transmitted from the AIC to the TMS320 serial port. EODR can be used to interrupt a microprocessor upon completion of serial communications. Also, EODR can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM, and to facilitate parallel data bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, EODR goes low after the first byte has been transmitted from the AIC to the TMS320 serial port and is kept low until the second byte has been transmitted. The TMS32011 or TMS320C17 can use this low-going signal to differentiate between the two bytes as to which is first and which is second. EODR does not occur after secondary communication.

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{EODX}}$	11	O	End of data transmit. See the WORD/$\overline{\text{BYTE}}$ description and the Serial Port Timing diagram. During the word-mode timing, $\overline{\text{EODX}}$ is a low-going pulse that occurs immediately after the 16 bits of D/A converter and control or register information have been transmitted from the TMS320 serial port to the AIC. $\overline{\text{EODX}}$ can be used to interrupt a microprocessor upon the completion of serial communications. Also, $\overline{\text{EODX}}$ can be used to strobe and enable external serial-to-parallel shift registers, latches, or an external FIFO RAM, and to facilitate parallel data-bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, $\overline{\text{EODX}}$ goes low after the first byte has been transmitted from the TMS320 serial port to the AIC and is kept low until the second byte has been transmitted. The TMS32011 or TMS320C17 can use this low-going signal to differentiate between the two bytes as to which is first and which is second.
$\overline{\text{FSR}}$	4	O	Frame sync receive. In the serial transmission modes, which are described in the WORD/$\overline{\text{BYTE}}$ description, $\overline{\text{FSR}}$ is held low during bit transmission. When $\overline{\text{FSR}}$ goes low, the TMS320 serial port begins receiving bits from the AIC via DR of the AIC. The most significant DR bit is present on DR before $\overline{\text{FSR}}$ goes low. (See Serial Port Timing and Internal Timing Configuration diagrams.) $\overline{\text{FSR}}$ does not occur after secondary communication.
FSX	14	O	Frame sync transmit. When FSX goes low, the TMS320 serial port begins transmitting bits to the AIC via DX of the AIC. In all serial transmission modes, which are described in the WORD/$\overline{\text{BYTE}}$ description, $\overline{\text{FSX}}$ is held low during bit transmission (see the Serial Port Timing and Internal Timing Configuration diagrams).
IN+	26	I	Noninverting input to analog input amplifier stage
IN–	25	I	Inverting input to analog input amplifier stage
MSTR CLK	6	I	Master clock. MSTR CLK is used to derive all the key logic signals of the AIC, such as the shift clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The Internal Timing Configuration diagram shows how these key signals are derived. The frequencies of these key signals are synchronous submultiples of the master clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the A/D and D/A converters (see the Internal Timing Configuration).
OUT+	22	O	Noninverting output of analog output power amplifier. OUT+ can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
OUT–	21	O	Inverting output of analog output power amplifier. OUT– is functionally identical with and complementary to OUT+.
REF	8	I/O	Internal voltage reference for the TLC32040. For the TLC32040 and TLC32041 an external voltage reference can be applied to this terminal.
$\overline{\text{RESET}}$	2	I	Reset. A reset function is provided to initialize the TA, TA', TB, RA, RA', RB, and control registers. This reset function initiates serial communications between the AIC and DSP. The reset function initializes all AIC registers including the control register. After a negative-going pulse on $\overline{\text{RESET}}$, the AIC registers are initialized to provide an 8-kHz data conversion rate for a 5.184-MHz master clock input signal. The conversion rate adjust registers, TA' and RA', are reset to 1. The control register bits are reset as follows (see AIC DX data word format section): d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1 This initialization allows normal serial-port communication to occur between AIC and DSP.
SHIFT CLK	10	O	Shift clock. SHIFT CLK is obtained by dividing the master clock signal frequency by four. SHIFT CLK is used to clock the serial data transfers of the AIC, described in the WORD/$\overline{\text{BYTE}}$ description below (see the Serial Port Timing and Internal Timing Configuration diagrams).
V_{DD}	7		Digital supply voltage, 5 V ±5%
V_{CC+}	20		Positive analog supply voltage, 5 V ±5%
V_{CC-}	19		Negative analog supply voltage, –5 V ±5%

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
WORD/$\overline{\mathrm{BYTE}}$	13	I	WORD/$\overline{\mathrm{BYTE}}$, in conjunction with a bit in the control register, is used to establish one of four serial modes. These four serial modes are described below. *AIC transmit and receive sections are operated asynchronously.* The following description applies when the AIC is configured to have asynchronous transmit and receive sections. If the appropriate data bit in the control register is a 0 (see the AIC DX data word format section), the transmit and receive sections are asynchronous. L Serial port directly interfaces with the serial port of the TMS32011 or TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams). 1. $\overline{\mathrm{FSX}}$ or $\overline{\mathrm{FSR}}$ is brought low. 2. One 8-bit byte is transmitted or one 8-bit byte is received. 3. $\overline{\mathrm{EODX}}$ or $\overline{\mathrm{EODR}}$ is brought low. 4. $\overline{\mathrm{FSX}}$ or $\overline{\mathrm{FSR}}$ emits a positive frame-sync pulse that is four shift clock cycles wide. 5. One 8-bit byte is transmitted or one 8-bit byte is received. 6. $\overline{\mathrm{EODX}}$ or $\overline{\mathrm{EODR}}$ is brought high. 7. $\overline{\mathrm{FSX}}$ or $\overline{\mathrm{FSR}}$ is brought high. H Serial port directly interfaces with the serial port of the TMS32020, TMS320C25, or TMS320C30 and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): 1. $\overline{\mathrm{FSX}}$ or $\overline{\mathrm{FSR}}$ is brought low. 2. One 16-bit word is transmitted or one 16-bit word is received. 3. $\overline{\mathrm{FSX}}$ or $\overline{\mathrm{FSR}}$ is brought high. 4. $\overline{\mathrm{EODX}}$ or $\overline{\mathrm{EODR}}$ emits a low-going pulse. *AIC transmit and receive sections are operated synchronously.* If the appropriate data bit in the control register is a 1, the transmit and receive sections are configured to be synchronous. In this case, the bandpass switched-capacitor filter and the A/D conversion timing are derived from the TX counter A, TX counter B, and TA, TA', and TB registers, rather than the RX counter A, RX counter B, and RA, RA', and RB registers. In this case, the AIC $\overline{\mathrm{FSX}}$ and $\overline{\mathrm{FSR}}$ timing are identical during primary data communication; however, $\overline{\mathrm{FSR}}$ is not asserted during secondary data communication since there is no new A/D conversion result. The synchronous operation sequences are as follows (see Serial Port Timing diagrams). L Serial port directly interfaces with the serial port of the TMS32011 or TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams): 1. $\overline{\mathrm{FSX}}$ and $\overline{\mathrm{FSR}}$ are brought low. 2. One 8-bit byte is transmitted and one 8-bit byte is received. 3. $\overline{\mathrm{EODX}}$ and $\overline{\mathrm{EODR}}$ are brought low. 4. $\overline{\mathrm{FSX}}$ and $\overline{\mathrm{FSR}}$ emit positive frame-sync pulses that are four shift clock cycles wide 5. One 8-bit byte is transmitted and one 8-bit byte is received. 6. $\overline{\mathrm{EODX}}$ and $\overline{\mathrm{EODR}}$ are brought high. 7. $\overline{\mathrm{FSX}}$ and $\overline{\mathrm{FSR}}$ are brought high. H Serial port directly interfaces with the serial port of the TMS32020, TMS320C25, or TMS320C30 and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): 1. $\overline{\mathrm{FSX}}$ and $\overline{\mathrm{FSR}}$ are brought low. 2. One 16-bit word is transmitted and one 16-bit word is received. 3. $\overline{\mathrm{FSX}}$ and $\overline{\mathrm{FSR}}$ are brought high. 4. $\overline{\mathrm{EODX}}$ or $\overline{\mathrm{EODR}}$ emit low-going pulses. Since the transmit and receive sections of the AIC are now synchronous, the AIC serial port with additional NOR and AND gates will interface to two SN74299 serial-to-parallel shift registers. Interfacing the AIC to the SN74299 shift register allows the AIC to interface to an external FIFO RAM and facilitates parallel data bus communications between the AIC and the digital signal processor. The operation sequence is the same as the above sequence (see Serial Port Timing diagrams).

detailed description

analog input

Two sets of analog inputs are provided. Normally, the IN+ and IN– input set is used; however, the auxiliary input set, AUX IN+ and AUX IN–, can be used if a second input is required. Each input set can be operated in either differential or single-ended modes, since sufficient common-mode range and rejection are provided. The gain for the IN+, IN–, AUX IN+, and AUX IN– inputs can be programmed to be either 1, 2, or 4 (see Table 2). Either input circuit can be selected via software control. It is important to note that a wide dynamic range is assured by the differential internal analog architecture and by the separate analog and digital voltage supplies and grounds.

A/D bandpass filter, A/D bandpass filter clocking, and A/D conversion timing

The A/D bandpass filter can be selected or bypassed via software control. The frequency response of this filter is presented in the following pages. This response results when the switched-capacitor filter clock frequency is 288 kHz. Several possible options can be used to attain a 288-kHz switched-capacitor filter clock. When the filter clock frequency is not 288 kHz, the filter transfer function is frequency scaled by the ratio of the actual clock frequency to 288 kHz. The low-frequency roll-off of the high-pass section is 300 Hz.

The internal timing configuration and AIC DX data word format sections of this data sheet indicate the many options for attaining a 288-kHz bandpass switched-capacitor filter clock. These sections indicate that the RX counter A can be programmed to give a 288-kHz bandpass switched-capacitor filter clock for several master clock input frequencies.

The A/D conversion rate is then attained by frequency dividing the 288-kHz bandpass switched-capacitor filter clock with the RX counter B. Thus, unwanted aliasing is prevented because the A/D conversion rate is an integral submultiple of the bandpass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

A/D converter performance specifications

Fundamental performance specifications for the A/D converter circuitry are presented in the A/D converter operating characteristics section of this data sheet. The realization of the A/D converter circuitry with switched-capacitor techniques provides an inherent sample-and-hold.

analog output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out of this integrated circuit. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

D/A low-pass filter, D/A low-pass filter clocking, and D/A conversion timing

The frequency response of this filter is presented in the following pages. This response results when the low-pass switched-capacitor filter clock frequency is 288 kHz. Like the A/D filter, the transfer function of this filter is frequency scaled when the clock frequency is not 288 kHz. A continuous-time filter is provided on the output on the output of the D/A low-pass filter to greatly attenuate any switched-capacitor clock feedthrough.

The D/A conversion rate is then attained by frequency dividing the 288-kHz switched-capacitor filter clock with TX counter B. Thus, unwanted aliasing is prevented because the D/A conversion rate is an integral submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.

asynchronous versus synchronous operation

If the transmit section of the AIC (low-pass filter and DAC) and receive section (bandpass filter and ADC) are operated asynchronously, the low-pass and band-pass filter clocks are independently generated from the master clock signal. Also, the D/A and A/D conversion rates are independently determined. If the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and bandpass filters. In synchronous operation, the A/D conversion timing is derived from, and is equal to, the D/A conversion timing. (See description of WORD/$\overline{\text{BYTE}}$ in the Terminal Functions table.)

D/A converter performance specifications

Fundamental performance specifications for the D/A converter circuitry are presented in the D/A converter operating characteristics section of the data sheet. The D/A converter has a sample-and-hold that is realized with a switched-capacitor ladder.

system frequency response correction

The (sin x) / x correction circuitry is performed in the digital processor software. The system frequency response can be corrected via DSP software to ±0.1-dB accuracy to band edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, which requires only seven TMS320 instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of only 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the (sin x) / x correction section for more details).

serial port

The serial port has four possible modes that are described in detail in the Terminal Functions table. These modes are briefly described below and in the description for WORD/$\overline{\text{BYTE}}$ in the Terminal Functions Table.

- The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32011 and TMS320C17.
- The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32020 and the TMS320C25.
- The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32011 and TMS320C17.
- The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, or two SN74299 serial-to-parallel shift registers, which can then interface in parallel to the TMS320C10, TMS32015, to any other digital signal processor, or to external FIFO circuitry.

operation of TLC32040 with internal voltage reference

The internal reference of the TLC32040 eliminates the need for an external voltage reference and provides overall circuit cost reduction. Thus, the internal reference eases the design task and provides complete control over the performance of this integrated circuit. The internal reference is brought out to a terminal and is available to the designer. To keep the amount of noise on the reference signal to a minimum, an external capacitor may be connected between REF and ANLG GND.

operation of TLC32040 or TLC32041 with external voltage reference

REF can be driven from an external reference circuit if so desired. This external circuit must be capable of supplying 250 μA and must be adequately protected from noise such as crosstalk from the analog input.

reset

A reset function is provided to initiate serial communications between the AIC and DSP and allow fast, cost-effective testing during manufacturing. The reset function initializes all AIC registers, including the control register. After a negative-going pulse on $\overline{\text{RESET}}$, the AIC is initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX data word format section).

loopback

This feature allows the user to test the circuit remotely. In loopback, OUT+ and OUT– are internally connected to IN+ and IN–. Thus, the DAC bits (d15 to d2), which are transmitted to DX, can be compared with the ADC bits (d15 to d2), which are received from DR. An ideal comparison would be that the bits on DR equal the bits on DX. However, in practice there is some difference in these bits due to the ADC and DAC output offsets.

In loopback, if IN+ and N– are enabled, the external signals on IN+ and IN– are ignored. If AUX IN+ and AUX IN– are enabled, the external signals on these terminals are added to the OUT+ and OUT– signals in loopback operation.

The loopback feature is implemented with digital signal processor control by transmitting the appropriate serial port bit to the control register (see AIC DX data word format section).

explanation of internal timing configuration

All of the internal timing of the AIC is derived from the high-frequency clock signal that drives the master clock input. The shift clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the master clock input signal frequency by four.

$$\text{SCF Clock Frequency} = \frac{\text{Master Clock Frequency}}{2 \times \text{Contents of Counter A}}$$

$$\text{Conversion Frequency} = \frac{\text{SCF Clock Frequency}}{\text{Contents of Counter B}}$$

$$\text{Shift Clock Frequency} = \frac{\text{Master Clock Frequency}}{4}$$

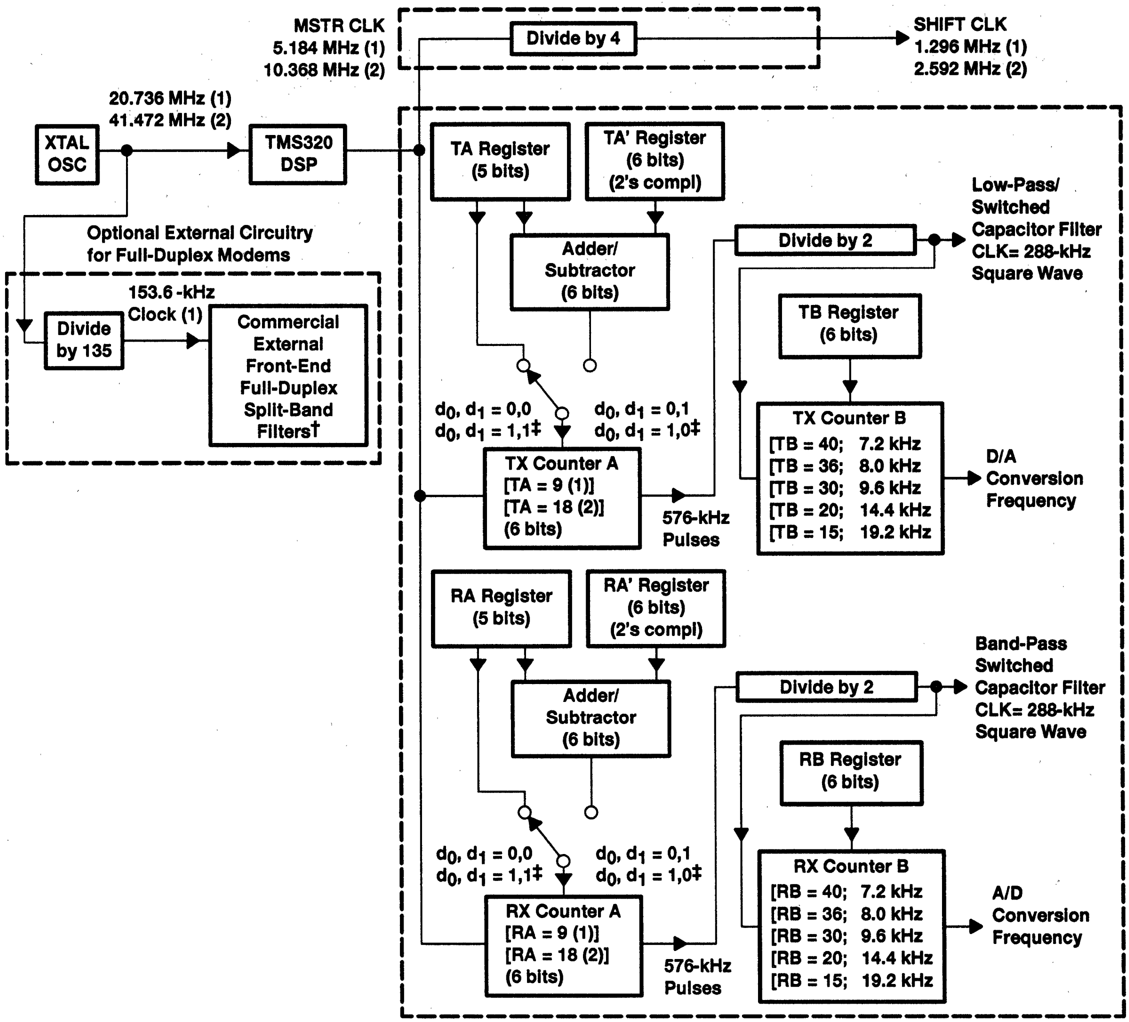
TX counter A and TX counter B, which are driven by the master clock signal, determine the D/A conversion timing. Similarly, RX counter A and RX counter B determine the A/D conversion timing. In order for the switched-capacitor low-pass and band pass filters to meet their transfer function specifications, the frequency of the clock inputs of the switched-capacitor filters must be 288 kHz. If the frequencies of the clock inputs are not 288 kHz, the filter transfer function frequencies are scaled by the ratios of the clock frequencies to 288 kHz. Thus, to obtain the specified filter responses, the combination of master clock frequency and TX counter A and RX counter A values must yield 288-kHz switched-capacitor clock signals. These 288-kHz clock signals can then be divided by the TX counter B and RX counter B to establish the D/A and A/D conversion timings.

TX counter A and TX counter B are reloaded every D/A conversion period, while RX counter A and RX counter B are reloaded every A/D conversion period. The TX counter B and RX counter B are loaded with the values in the TB and RB registers, respectively. Via software control, the TX counter A can be loaded with either the TA register, the TA register less the TA' register, or the TA register plus the TA' register. By selecting the TA register less the TA' register option, the upcoming conversion timing will occur earlier by an amount of time that equals TA' times the signal period of the master clock. By selecting the TA register plus the TA' register option, the upcoming conversion timing will occur later by an amount of time that equals TA' times the signal period of the master clock. Thus, the D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. In this case, however, the RX counter A can be programmed via software control with the RA register, the RA register less the RA' register, or the RA register plus the RA' register.

explanation of internal timing configuration (continued)

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing. This feature can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.

If the transmit and receive sections are configured to be synchronous (see WORD/$\overline{\text{BYTE}}$ description), then both the low-pass and bandpass switched-capacitor filter clocks are derived from TX counter A. Also, both the D/A and A/D conversion timing are derived from the TX counter A and TX counter B. When the transmit and receive sections are configured to be synchronous, the RX counter A, RX counter B, RA register, RA' register, and RB registers are not used.



$$\text{SCF Clock Frequency} = \frac{\text{Master Clock Frequency}}{2 \times \text{Contents of Counter A}}$$

† Split-band filtering can alternatively be performed after the analog input function via software in the TMS320.
‡ These control bits are described in the AIC DX data word format section.

NOTE A: Frequency 1 (20.736 MHz) is used to show how 153.6 kHz (for commercially available modem split-band filter clock), popular speech and modem sampling signal frequencies, and an internal 288-kHz switched-capacitor filter clock can be derived synchronously and as submultiples of the crystal oscillator frequency. Since these derived frequencies sre synchronous submultiples of the crystal frequency, aliasing does not occur as the sampled analog signal passes between the analog converter and switched-capacitor filter stages. Frequency 2 (41.472 MHz) is used to show that the AIC can work with high-frequency signals, which are used by high-speed digital signal processors.

Figure 1. Internal Timing Configuration

AIC DR or DX word bit pattern

A/D or D/A MSB, 1st bit sent							1st bit sent of 2nd byte					A/D or D/A LSB			
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

AIC DX data word format section

<table>
<tr><th>d15</th><th>d14</th><th>d13</th><th>d12</th><th>d11</th><th>d10</th><th>d9</th><th>d8</th><th>d7</th><th>d6</th><th>d5</th><th>d4</th><th>d3</th><th>d2</th><th>d1</th><th>d0</th><th>COMMENTS</th></tr>
<tr><td colspan="16">primary DX serial communication protocol</td><td></td></tr>
<tr><td colspan="14">←d15 (MSB) through d2 go to the D/A converter register →</td><td>0</td><td>0</td><td>The TX and RX counter As are loaded with the TA and RA register values. The TX and RX counter Bs are loaded with TB and RB register values.</td></tr>
<tr><td colspan="14">←d15 (MSB) through d2 go to the D/A converter register →</td><td>0</td><td>1</td><td>The TX and RX counter As are loaded with the TA + TA' and RA + RA' register values. The TX and RX counter Bs are loaded with TB and RB register values. Bits d1 = 0 and d0 =1 cause the next D/A and A/D conversion periods to be changed by the addition of TA' and RA' master clock cycles, in which TA' and R/A' can be positive or negative or zero (refer to Table 1).</td></tr>
<tr><td colspan="14">←d15 (MSB) through d2 go to the D/A converter register →</td><td>1</td><td>0</td><td>The TX and RX counter As are loaded with the TA – TA' and RA – RA' register values. The TX and RX counter Bs are loaded with TB and RB register values. Bits d1 = 1 and d0 = 0 cause the next D/A and A/D conversion periods to be changed by the subtraction of TA' and RA' master clock cycles, in which TA' and R/A' can be positive or negative or zero (refer to Table 1).</td></tr>
<tr><td colspan="14">←d15 (MSB) through d2 go to the D/A converter register →</td><td>1</td><td>1</td><td>The TX and RX counter As are loaded with the TA and RA register values. The TX and RX counter Bs are loaded with the TB and RB register values. After a delay of four shift clock cycles, a secondary transmission immediately follows to program the AIC to operate in the desired configuration.</td></tr>
</table>

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (primary communications) to the AIC initiates secondary communications upon completion of the primary communications.

Upon completion of the primary communication, $\overline{FSX}$ remains high for four SHIFT CLK cycles and then goes low and initiates the secondary communication. The timing specifications for the primary and secondary communications are identical. In this manner, the secondary communication, if initiated, is interleaved between successive primary communications. This interleaving prevents the secondary communication from interfering with the primary communications and DAC timing, thus preventing the AIC from skipping a DAC output. In the synchronous mode, $\overline{FSR}$ is not asserted during secondary communications.

secondary DX serial communication protocol

x x I ← to TA register → I x x I ← to RA register → I	0 0	d13 and d6 are MSBs (unsigned binary)
x I ← to TA' register → I x I ← to RA' register → I	0 1	d14 and d7 are 2's complement sign bits
x I ← to TB register → I x I ← to RB register → I	1 0	d14 and d7 are MSBs (unsigned binary)
x x x x x x x x d7 d6 d5 d4 d3 d2	1 1	
Control register		d2 = 0/1 deletes/inserts the bandpass filter
		d3 = 0/1 disables/enables the loopback function
		d4 = 0/1 disables/enables the AUX IN+ and AUX IN− terminals
		d5 = 0/1 asynchronous/synchronous transmit receive sections
		d6 = 0/1 gain control bits (see gain control section)
		d7 = 0/1 gain control bits (see gain control section)

reset function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After power has been applied to the AIC, a negative-going pulse on $\overline{\text{RESET}}$ initializes the AIC registers to provide an 8-kHz A/D and D/A conversion rate for a 5.184-MHz master clock input signal. The AIC, except the control register, is initialized as follows (see AIC DX data word format section):

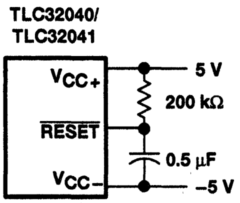
REGISTER	INITIALIZED REGISTER VALUE (HEX)
TA	9
TA'	1
TB	24
RA	9
RA'	1
RB	24

The control register bits are reset as follows (see AIC DX data word format section):

d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1

This initialization allows normal serial port communications to occur between AIC and DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA', and TB register need to be programmed, since both transmit and receive timing are synchronously derived from these registers (see the terminal descriptions and AIC DX word format sections).

The circuit shown below provides a reset on power up when power is applied in the sequence given under power-up sequence. The circuit depends on the power supplies reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.



power-up sequence

To ensure proper operation of the AIC, and as a safeguard against latch-up, it is recommended that a Schottky diode with a forward voltage less than or equal to 0.4 V be connected from V_{CC-} to ANLG GND (see Figure 17). In the absence of such a diode, power should be applied in the following sequence: ANLG GND and DGTL GND, V_{CC-}, then V_{CC+} and V_{DD}. Also, no input signal should be applied until after power up.

AIC responses to improper conditions

The AIC has provisions for responding to improper conditions. These improper conditions and the response of the AIC to these conditions are presented in Table 1 below.

AIC register constraints

The following constraints are placed on the contents of the AIC registers:

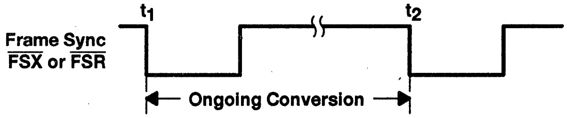
1. TA register must be ≥ 4 in word mode (WORD/$\overline{\text{BYTE}}$ = high).
2. TA register must be ≥ 5 in byte mode (WORD/$\overline{\text{BYTE}}$ = low).
3. TA' register can be either positive, negative, or zero.
4. RA register must be ≥ 4 in word mode (WORD/$\overline{\text{BYTE}}$ = high).
5. RA register must be ≥ 5 in byte mode (WORD/$\overline{\text{BYTE}}$ = low).
6. RA' register can be either positive, negative, or zero.
7. (TA register ± TA' register) must be > 1.
8. (RA register ± RA' register) must be > 1.
9. TB register must be > 1.

Table 1. AIC Responses To Improper Conditions

IMPROPER CONDITIONS	AIC RESPONSE
TA register + TA' register = 0 or 1 TA register – TA' register = 0 or 1	Reprogram TX counter A with TA register value
TA register + TA' register < 0	MODULO 64 arithmetic is used to ensure that a positive value is loaded into the TX counter A, i.e., TA register + TA' register + 40 hex is loaded into TX counter A.
RA register + RA' register = 0 or 1 RA register – RA' register = 0 or 1	Reprogram RX counter A with RA register value
RA register + RA' register = 0 or 1	MODULO 64 arithmetic is used to ensure that a positive value is loadsd into RX counter A, i.e., RA register + RA' register + 40 hex is loaded into RX counter A.
TA register = 0 or 1 RA register = 0 or 1	The AIC is shut down.
TA register < 4 in word mode TA register < 5 in byte mode RA register < 4 in word mode RA register < 5 in byte mode	The AIC serial port no longer operates.
TB register = 0 or 1	Reprogram TB register with 24 hex
RB register = 0 or 1	Reprogram RB register with 24 hex
AIC and DSP cannot communicate	Hold last DAC output

improper operation due to conversion times being too close together

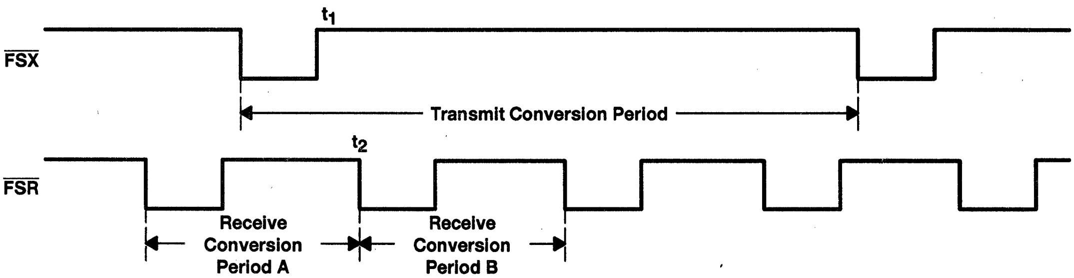
If the difference between two successive D/A conversion frame syncs is less than 1/19.2 kHz, the AIC operates improperly. In this situation, the second D/A conversion frame sync occurs too quickly and there is not enough time for the ongoing conversion to be completed. This situation can occur if the A and B registers are improperly programmed or if the A + A' register or A – A' register result is too small. When incrementally adjusting the conversion period via the A + A' register options, the designer should be very careful not to violate this requirement (see following diagram).



$t_2 - t_1 \geq 1/19.2$ kHz

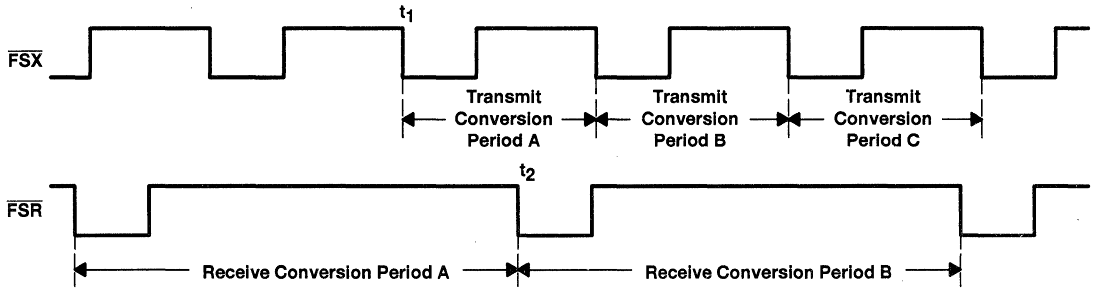
asynchronous operation — more than one receive frame sync occurring between two transmit frame syncs

When incrementally adjusting the conversion period via the A + A' or A – A' register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during a $\overline{FSX}$ frame sync. The ongoing conversion period is then adjusted. However, either receive conversion period A or B may be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. Therefore, if there is sufficient time between t_1 and t_2, the receive conversion period adjustment is performed during receive conversion period A. Otherwise, the adjustment is performed during receive conversion period B. The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent $\overline{FSX}$ frame (see figure below).



asynchronous operation — more than one receive frame sync occurring between two receive frame syncs

When incrementally adjusting the conversion period via the A + A' or A – A' register options, a specific protocol is followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during a $\overline{FSX}$ frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment in the diagram as shown in the following figure. If the adjustment command is issued during transmit conversion period A, receive conversion period A is adjusted if there is sufficient time between t_1 and t_2. Or, if there is not sufficient time between t_1 and t_2, receive conversion period B is adjusted. Or, the receive portion of an adjustment command can be ignored if the adjustment command is sent during a receive conversion period, which is already being or is adjusted due to a prior adjustment command. For example, if adjustment commands are issued during transmit conversion periods A, B, and C, the first two commands can cause receive conversion periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during receive conversion period B, which already is adjusted via the transmit conversion period B adjustment command.



asynchronous operation — more than one set of primary and secondary DX serial communication occurring between two receive frame sync (see AIC DX data word format section)

The TA, TA', TB, and control register information that is transmitted in the secondary communications is always accepted and is applied during the ongoing transmit conversion period. If there is sufficient time between t_1 and t_2, the TA, RA', and RB register information, which is sent during transmit conversion period A, is applied to receive conversion period A. Otherwise, this information is applied during receive conversion period B. If RA, RA', and RB register information has already been received and is being applied during an ongoing conversion period, any subsequent RA, RA', or RB information that is received during this receive conversion period is disregarded (see diagram below).

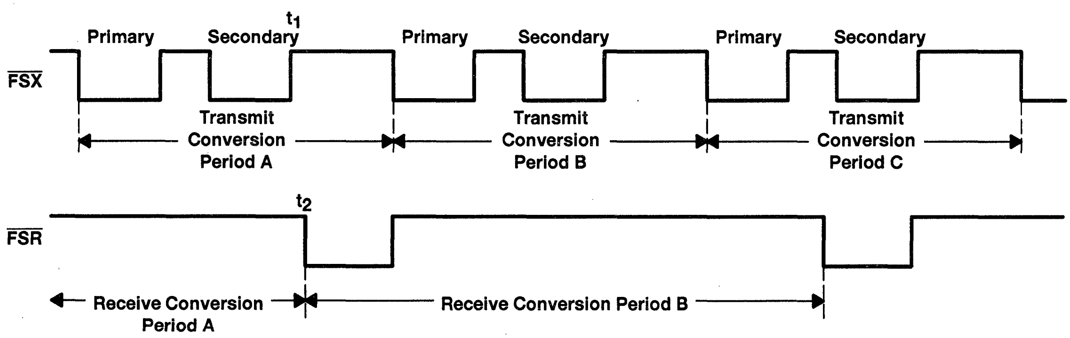
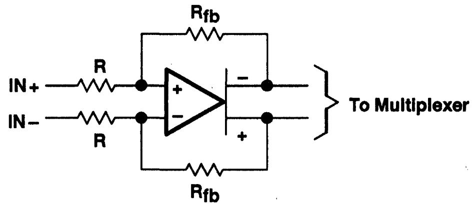


Table 2. Gain Control Table Analog Input Signal Required for Full-Scale A/D Conversion

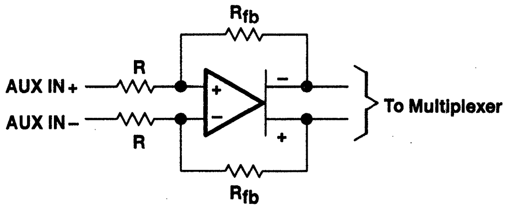
INPUT CONFIGURATIONS	CONTROL REGISTER BITS d6	CONTROL REGISTER BITS d7	ANALOG INPUT†	A/D CONVERSION RESULT
Differential configuration Analog input = IN+ – IN– = AUX IN+ – AUX IN–	1	1	±6 V	Full scale
	0	0		
	1	0	±3 V	Full scale
	0	1	±1.5 V	Full scale
Single-ended configuration Analog input = IN+ – ANLG GND = AUX IN+ – ANLG GND	1	1	±3 V	Half scale
	0	0		
	1	0	±3 V	Full scale
	0	1	±1.5 V	Full scale

† In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0, d7 = 1

Figure 2. IN+ and IN– Gain Control Circuitry



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0, d7 = 1

Figure 3. AUX IN+ and AUX IN– Gain Control Circuitry

(sin x)/x correction section

The AIC does not have (sin x)/x correction circuitry after the digital-to-analog converter.The (sin x)/x correction can be accomplished easily and efficiently in digital signal processor (DSP) software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results, which are shown below, are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires only seven instruction cycles per sample on the TMS320 DSPs. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction adds a slight amount of group delay at the upper edge of the 300–3000-Hz band.

(sin x)/x roll-off for a zero-order hold function

The (sin x)/x roll-off for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in the table below.

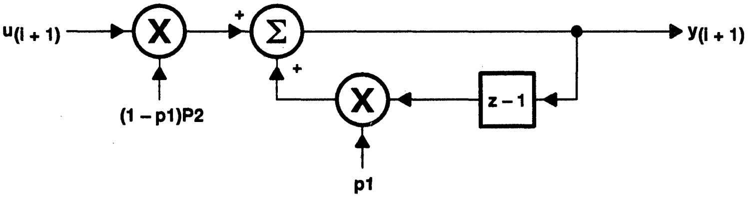
Table 3. (sin x)/x Roll-Off

f_s (Hz)	20 log $\frac{\sin \pi f/f_s}{\pi f/f_s}$ (f = 3000 Hz) (dB)
7200	−2.64
8000	−2.11
9600	−1.44
14400	−0.63
19200	−0.35

The actual AIC (sin x)/x roll-off is slightly less than the above figures, because the AIC has less than a 100% duty cycle hold interval.

correction filter

To compensate for the (sin x)/x roll-off of the AIC, a first-order correction filter shown below, is recommended.



The difference equation for this correction filter is:

$$y_{i+1} = p2(1 - p1)(u_{i+1}) + p1\, y_i$$

where the constant p1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$|H(f)|^2 = \frac{p2^2(1 - p1)^2}{1 - 2p1 \cos(2\pi f/f_s) + p1^2}$$

correction results

Table 4 below shows the optimum p values and the corresponding correction results for 8000-Hz and 9600-Hz sampling rates.

Table 4. Correction Results

f (Hz)	ERROR (dB) f_S = 8000 Hz p1 = −0.14813 p2 = 0.9888	ERROR (dB) f_S = 9600 Hz p1 = −0.1307 p2 = 0.9951
300	−0.099	−0.043
600	−0.089	−0.043
900	−0.054	0
1200	−0.002	0
1500	0.041	0
1800	0.079	0.043
2100	0.100	0.043
2400	0.091	0.043
2700	−0.043	0
3000	−0.102	−0.043

TMS320 software requirements

The digital correction filter equation can be written in state variable form as follows:

$$Y = k1 \times Y + k2 \times U$$

Where

$k1 = p1$

$k2 = (1 - p1) \times p2$

Y = filter state

U = next I/O sample

The coefficients k1 and k2 must be represented as 16-bit integers. The SACH instruction (with the proper shift) will yield the correct result. With the assumption that the TMS320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC+} (see Note 1)	−0.3 V to 15 V
Supply voltage range, V_{DD}	−0.3 V to 15 V
Output voltage range, V_O	−0.3 V to 15 V
Input voltage range, V_I	−0.3 V to 15 V
Digital ground voltage range	−0.3 V to 15 V
Operating free-air temperature range, T_A: TLC32040C, TLC32041C	0°C to 70°C
TLC32040I, TLC32041I	−40°C to 85°C
Storage temperature range, T_{stg}	−40°C to 125°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values for maximum ratings are with respect to V_{CC-}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} (see Note 2)		4.75	5	5.25	V
Supply voltage, V_{CC-} (see Note 2)		−4.75	−5	−5.25	V
Digital supply voltage, V_{DD} (see Note 2)		4.75	5	5.25	V
Digital ground voltage with respect to ANLG GND, DGTL GND			0		V
Reference input voltage, $V_{ref(ext)}$ (see Note 2)		2		4	V
High-level input voltage, V_{IH}		2		V_{DD}+0.3	V
Low-level input voltage, V_{IL} (see Note 3)		−0.3		0.8	V
Load resistance at OUT+ and/or OUT−, R_L		300			Ω
Load capacitance at OUT+ and/or OUT−, C_L				100	pF
MSTR CLK frequency (see Note 4)		0.075	5	10.368	MHz
Analog input amplifier common mode input voltage (see Note 5)				±1.5	V
A/D or D/A conversion rate				20	kHz
Operating free-air temperature, T_A	TLC32040C, TLC32041C	0		70	°C
	TLC32040I, TLC32041I	−40		85	

NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+}, and V_{CC-}, are with respect to ANLG GND. Voltages at digital inputs and outputs and V_{DD} are with respect to DGTL GND.
3. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.
4. The bandpass low-pass switched-capacitor filter response specifications apply only when the switched-capacitor clock frequency is 288 kHz. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.
5. This range applies when (IN+ − IN−) or (AUX IN+ − AUX IN−) equals ± 6 V.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted)

total device, MSTR CLK frequency = 5.184 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 4.75 V, I_{OH} = −300 µA	2.4			V
V_{OL}	Low-level output voltage		V_{DD} = 4.75 V, I_{OL} = 2 mA			0.4	V
I_{CC+}	Supply current from V_{CC+}	TLC3204_C				35	mA
		TLC3204_I				40	
I_{CC-}	Supply current from V_{CC-}	TLC3204_C				−35	mA
		TLC3204_I				−40	
I_{DD}	Supply current from V_{DD}		$f_{MSTR\ CLK}$ = 5.184 MHz			7	mA
V_{ref}	Internal reference output voltage			3		3.3	V
$\propto V_{ref}$	Temperature coefficient of internal reference voltage				200		ppm/°C
r_o	Output resistance at REF				100		kΩ

receive amplifier input

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	A/D converter offset error (filters bypassed)			25	65	mV
	A/D converter offset error (filters in)			25	65	mV
CMRR	Common-mode rejection ratio at IN+, IN−, or AUX IN+, AUX IN−	See Note 6		55		dB
r_I	Input resistance at IN+, IN−, or AUX IN+,AUX IN−, REF			100		kΩ

transmit filter output

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset voltage at OUT+, OUT−, (single-ended relative to ANLG GND)			15	75	mV
V_{OM}	Maximum peak output voltage swing across R_L at OUT+ or OUT−, (single ended)	$R_L \geq$ 300 Ω, Offset voltage = 0	±3			V
V_{OM}	Maximum peak output voltage swing between R_L at OUT+ and OUT−, (differential output)	$R_L \geq$ 600 Ω	±6			V

system distortion specifications, SCF clock frequency = 288 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Attenuation of second harmonic of A/D input signal	Single ended	V_I = −0.5 dB to −24 dB referred to V_{ref}, See Note 7		70		dB
	Differential		62	70		
Attenuation of third and higher harmonics of A/D input signal	Single ended	V_I = −0.5 dB to −24 dB referred to V_{ref}, See Note 7		65		dB
	Differential		57	65		
Attenuation of second harmonic of D/A input signal	Single ended	V_I = −0 dB to −24 dB referred to V_{ref}, See Note 7		70		dB
	Differential		62	70		
Attenuation of third and higher harmonics of D/A input signal	Single ended	V_I = −0 dB to −24 dB referred to V_{ref}, See Note 7		65		dB
	Differential		57	65		

† All typical values are at T_A = 25°C.

NOTES: 6. The test condition is a 0-dBm, 1-kHz input signal with an 8-kHz conversion rate.

7. The test condition V_I is a 1-kHz input signal with an 8-kHz conversion rate (0 dB relative to V_{ref}). The load impedance for the DAC is 600 Ω.

A/D channel signal-to-distortion ratio

PARAMETER	TEST CONDITIONS (see Note 7)	A_V = 1† MIN	A_V = 1† MAX	A_V = 2† MIN	A_V = 2† MAX	A_V = 4† MIN	A_V = 4† MAX	UNIT
A/D channel signal-to-distortion ratio	V_I = –6 dB to –0.1 dB	58		>58§		>58§		dB
	V_I = –12 dB to –6 dB	58		58		>58§		
	V_I = –18 dB to –12 dB	56		58		58		
	V_I = –24 dB to –18 dB	50		56		58		
	V_I = –30 dB to –24 dB	44		50		56		
	V_I = –36 dB to –30 dB	38		44		50		
	V_I = –42 dB to –36 dB	32		38		44		
	V_I = –48 dB to –42 dB	26		32		38		
	V_I = –54 dB to –48 dB	20		26		32		

D/A channel signal-to-distortion ratio

PARAMETER	TEST CONDITIONS (see Note 7)	MIN	MAX	UNIT
D/A channel signal-to-distortion ratio	V_I = –6 dB to 0 dB	58		dB
	V_I = –12 dB to –6 dB	58		
	V_I = –18 dB to –12 dB	56		
	V_I = –24 dB to –18 dB	50		
	V_I = –30 dB to –24 dB	44		
	V_I = –36 dB to –30 dB	38		
	V_I = –42 dB to –36 dB	32		
	V_I = –48 dB to –42 dB	26		
	V_I = –54 dB to –48 dB	20		

gain and dynamic range

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Absolute transmit gain tracking error while transmitting into 600 Ω	–48-dB to 0-dB signal range, See Note 8		±0.05	±0.15	dB
Absolute receive gain tracking error	–48-dB to 0-dB signal range, See Note 8		±0.05	±0.15	dB
Absolute gain of the A/D channel	Signal input is a –0.5-dB, 1-kHz sinewave		0.2		dB
Absolute gain of the D/A channel	Signal input is a 0-dB, 1-kHz sinewave		–0.3		dB

power supply rejection and crosstalk attenuation

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{CC+} or V_{CC-} supply voltage rejection ratio, receive channel	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at DR (ADC output)		30		dB
	f = 30 kHz to 50 kHz			45		
V_{CC+} or V_{CC-} supply voltage rejection ratio, transmit channel (single ended)	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at OUT+		30		dB
	f = 30 kHz to 50 kHz			45		
Crosswalk attenuation, transmit-to-receive (single ended)				80		dB

† A_V is the programmable gain of the input amplifier.
‡ All typical values are at T_A = 25°C.
§ A value >58 is overrange and signal clipping occurs.

NOTES: 7. The test condition V_{in} is a 1-kHz input signal with an 8-kHz conversion rate (0 dB relative to V_{ref}). The load impedance for the DAC is 600 Ω.
8. Gain tracking is relative to the absolute gain at 1 kHz and 0 dB (0 dB relative to V_{ref}).

delay distortion, SCF clock frequency = 288 kHz ±2%, input (IN+ – IN–) is ±3-V sinewave

Refer to filter response graphs for delay distortion specifications.

TLC32040 and TLC32041 bandpass filter transfer function (see curves), SCF clock frequency = 288 kHz, ±2%, input (IN+ – IN–) is a ±3-V sinewave (see Note 9)

PARAMETER	TEST CONDITIONS	FREQUENCY RANGE	MIN	MAX	UNIT
Filter gain, (see Note 10)	Input signal reference is 0 dB	f = 100 Hz		–42	dB
		f = 170 Hz		–25	
		300 Hz ≤ f ≤ 3.4 kHz	–0.5	0.5	
		f = 4 kHz		–16	
		f ≥ 4.6 kHz		–58	

low-pass filter transfer function, SCF clock frequency = 288 kHz ±2% (see Note 9)

PARAMETER	TEST CONDITIONS	FREQUENCY RANGE	MIN	MAX	UNIT
Filter gain, (see Note 10)	Output signal reference is 0 dB	f ≤ 3.4 kHz	–0.5	0.5	dB
		f = 3.6 kHz		–4	
		f = 4 kHz		–30	
		f ≥ 4.4 kHz		–58	

serial port

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –300 µA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
I_I	Input current				±10	µA
C_i	Input capacitance			15		pF
C_o	Output capacitance			15		pF

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = –5 V, V_{DD} = 5 V

noise (measurement includes low-pass and bandpass switched-capacitor filters)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit noise	Single ended	DX input = 00000000000000, constant input code		200		µV rms
	Differential			300	500	µV rms
				20		dBrncO
Receive noise (see Note 11)		Inputs grounded, gain = 1		300	475	µV rms
				20		dBrncO

† All typical values are at T_A = 25°C.

NOTES: 9. The above filter specifications are for a switched-capacitor filter clock range of 288 kHz ±2%. For switched-capacitor filter clocks at frequencies other than 288 kHz ±2%, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

10. The filter gain outside of the passband is measured with respect to the gain at 1 kHz. The filter gain within the passband is measured with respect to the average gain within the passband. The passbands are 300 to 3400 Hz and 0 to 3400 Hz for the bandpass and low-pass filters respectively.

11. The noise is reffered to the input with a buffer gain of one. If the buffer gain is two or four, the noise figure is correspondingly reduced. The noise is computed by statistically evaluating the digital output of the A/D converter.

timing requirements

serial port recommended input signals

		MIN	MAX	UNIT
$t_{c(MCLK)}$	Master clock cycle time	95		ns
$t_{r(MCLK)}$	Master clock rise time		10	ns
$t_{f(MCLK)}$	Master clock fall time		10	ns
	Master clock duty cycle	42%	58%	
	$\overline{\text{RESET}}$ pulse duration (see Note 12)	800		ns
$t_{su(DX)}$	DX setup time before SCLK↓	20		ns
$t_{h(DX)}$	DX hold time after SCLK↓	$t_{c(SCLK)}/4$		ns

serial port – AIC output signals, C_L = 30 pF for SHIFT CLK output, C_L = 15 pF for all other outputs

		MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time	380			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time		3	8	ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time		3	8	ns
	Shift clock (SCLK) duty cycle	45		55	%
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{\text{FSR}}$/$\overline{\text{FSX}}$/$\overline{\text{FSD}}$↓		30		ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{\text{FSR}}$/$\overline{\text{FSX}}$/$\overline{\text{FSD}}$↑		35	90	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑			90	ns
$t_{d(CH-EL)}$	Delay from SCLK↑ to $\overline{\text{EODX}}$/$\overline{\text{EODR}}$↓ in word mode			90	ns
$t_{d(CH-EH)}$	Delay from SCLK↑ to $\overline{\text{EODX}}$/$\overline{\text{EODR}}$↑ in word mode			90	ns
$t_{f(EODX)}$	$\overline{\text{EODX}}$ fall time		2	8	ns
$t_{f(EODR)}$	$\overline{\text{EODR}}$ fall time		2	8	ns
$t_{d(CH-EL)}$	Delay from SCLK↑ to $\overline{\text{EODX}}$/$\overline{\text{EODR}}$↓ in byte mode			90	ns
$t_{d(CH-EH)}$	Delay from SCLK↑ to $\overline{\text{EODX}}$/$\overline{\text{EODR}}$↑ in byte mode			90	ns
$t_{d(MH-SL)}$	Delay from MSTR CLK↑ to SCLK↓		65	170	ns
$t_{d(MH-SH)}$	Delay from MSTR CLK↑ to SCLK↑		65	170	ns

† Typical values are at T_A = 25°C.

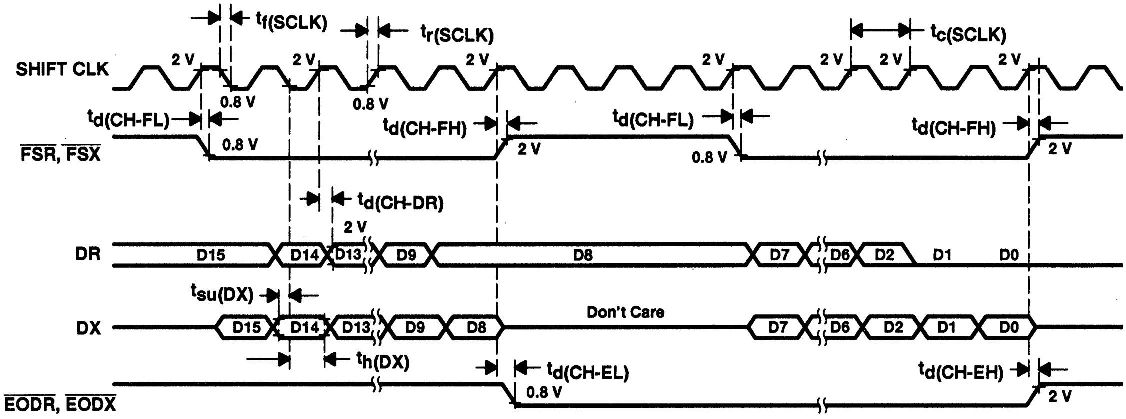
NOTE 12: $\overline{\text{RESET}}$ pulse duration is the amount of time that the reset terminal is held below 0.8 V after the power supplies have reached their recommended values.

serial port – AIC output signals

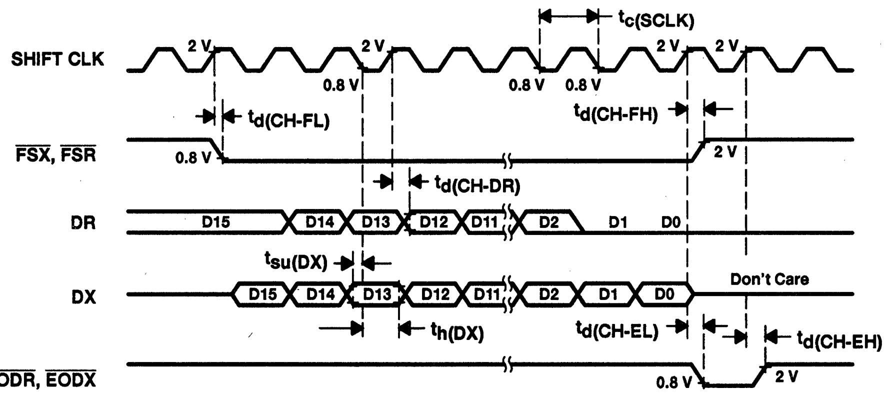
		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time		380			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time				50	ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time				50	ns
	Shift clock (SCLK) duty cycle		45		55	%
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{FSR}/\overline{FSX}$↓	$C_L = 50$ pF			52	ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{FSR}/\overline{FSX}$↑	$C_L = 50$ pF			52	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑				90	ns
$t_{d(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↓ in word mode				90	ns
$t_{d(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↑ in word mode				90	ns
$t_{f(EODX)}$	$\overline{EODX}$ fall time				15	ns
$t_{f(EODR)}$	$\overline{EODR}$ fall time				15	ns
$t_{d(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↓ in byte mode				100	ns
$t_{d(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↑ in byte mode				100	ns
$t_{d(MH-SL)}$	Delay from MSTR CLK↑ to SCLK↓			65		ns
$t_{d(MH-SH)}$	Delay from MSTR CLK↑ to SCLK↑			65		ns

† Typical values are at $T_A = 25°C$.

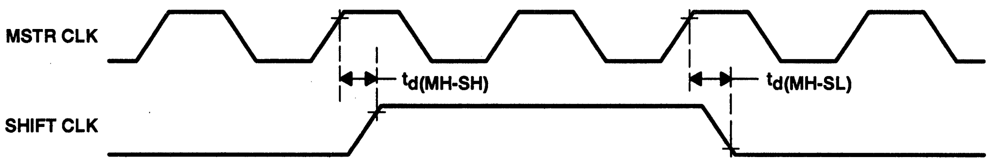
PARAMETER MEASUREMENT INFORMATION



(a) BYTE-MODE TIMING



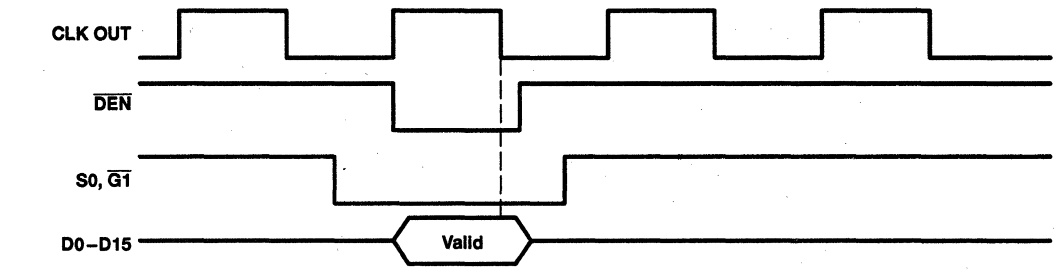
(b) WORD-MODE TIMING



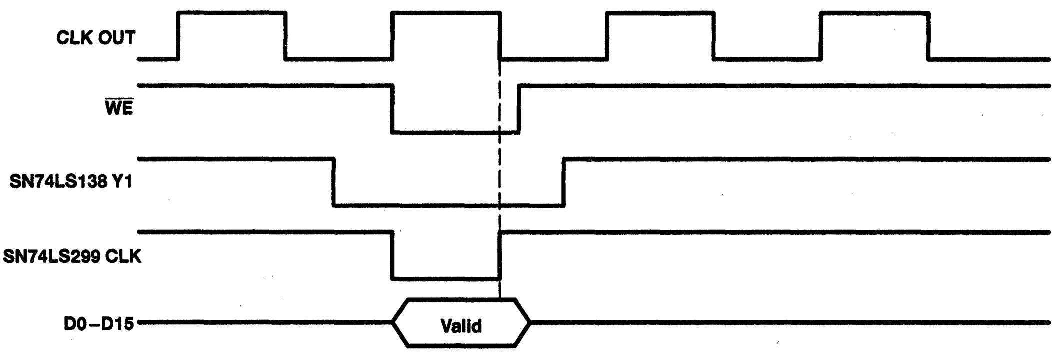
(c) SHIFT-CLOCK TIMING

Figure 4. Serial Port Timing

PARAMETER MEASUREMENT INFORMATION



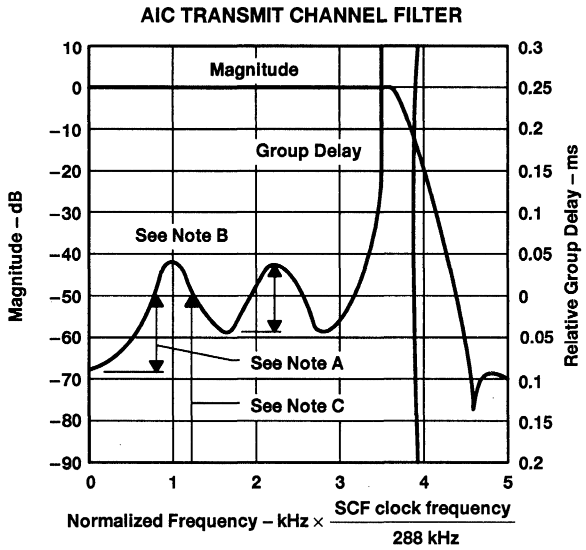
(a) IN INSTRUCTION TIMING



(b) OUT INSTRUCTION TIMING

Figure 5. TMS32010-TLC32040/TLC32041 Interface Timing

TYPICAL CHARACTERISTICS

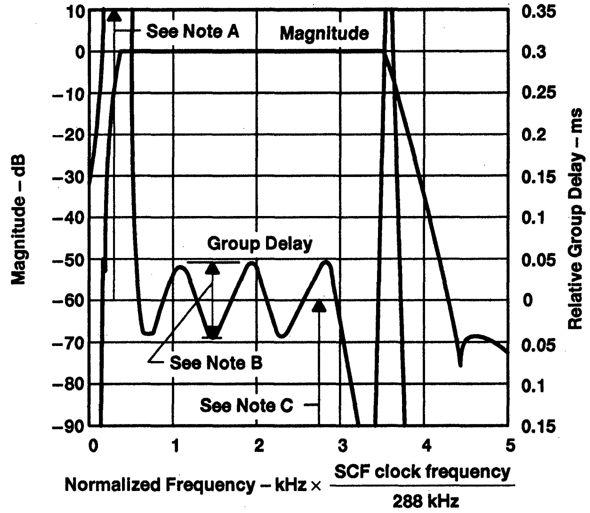


NOTES: A. Maximum relative delay (0 Hz to 600 Hz) = 125 μs
B. Maximum relative delay (600 Hz to 3000 Hz) = ± 50 μs
C. Absolute delay (600 Hz to 3000 Hz) = 700 μs
D. Test conditions are V_{CC+}, V_{CC-}, and V_{DD} within recommended operating conditions, SCF clock f = 288 kHz ±2% input = ±3-V sinewave, and T_A = 25°C.

Figure 6

TYPICAL CHARACTERISTICS

TLC32040 AND TLC32041 RECEIVE CHANNEL FILTER



NOTES: A. Maximum relative delay (200 Hz to 600 Hz) = 3350 µs
B. Maximum relative delay (600 Hz to 3000 Hz) = ± 50 µs
C. Absolute delay (600 Hz to 3000 Hz) = 1230 µs
D. Test conditions are V_{CC+}, V_{CC-}, and V_{DD} within recommended operating conditions, SCF clock f = 288 kHz ±2%, input = ±3-V sinewave, and T_A = 25°C.

Figure 7

TYPICAL CHARACTERISTICS

A/D SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL

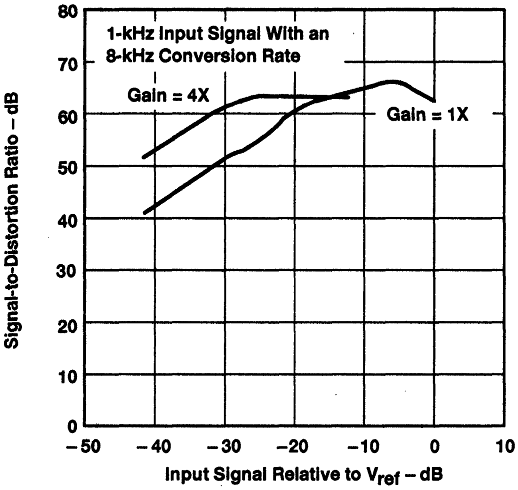


Figure 8

A/D GAIN TRACKING
(GAIN RELATIVE TO GAIN
AT 0-dB INPUT SIGNAL)

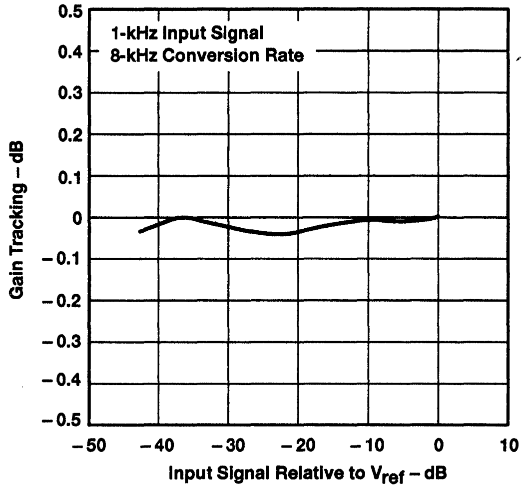


Figure 9

D/A CONVERTER SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL

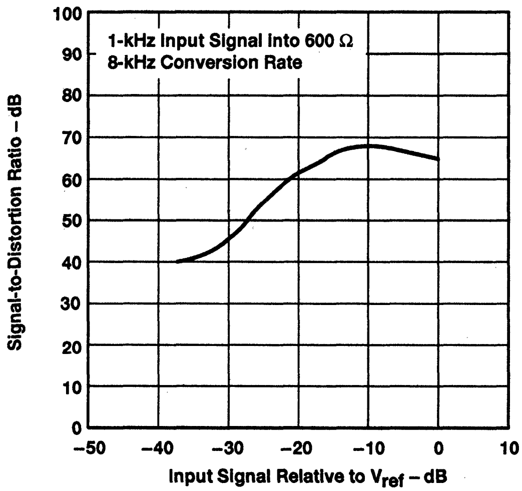


Figure 10

D/A GIAN TRACKING
vs
(GAIN RELATIVE TO GAIN
AT 0 0dB INPUT SIGNAL)

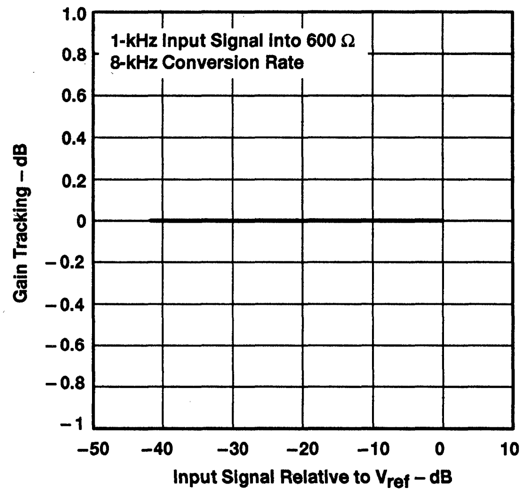


Figure 11

NOTE: Test conditions are V_{CC+}, V_{CC-}, V_{DD} and within recommended operating conditions set clock f = 288 kHz ±2%, and T_A = 25°C.

TYPICAL CHARACTERISTICS

ATTENUATION OF SECOND HARMONIC OF A/D INPUT vs INPUT SIGNAL

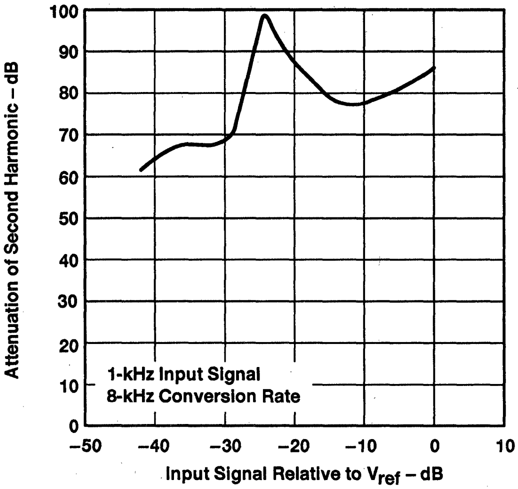


Figure 12

ATTENUATION OF THIRD HARMONIC OF A/D INPUT vs INPUT SIGNAL

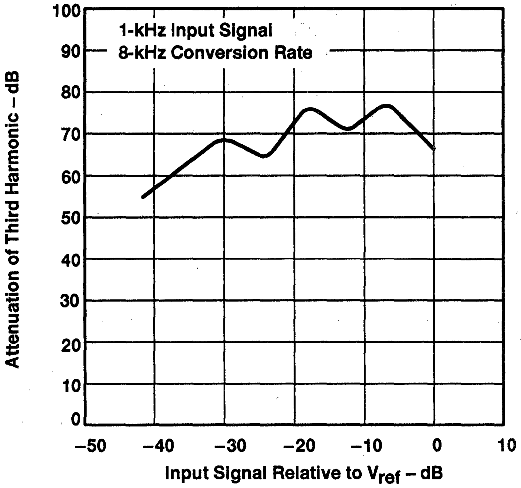


Figure 13

ATTENUATION OF SECOND HARMONIC OF D/A INPUT vs INPUT SIGNAL

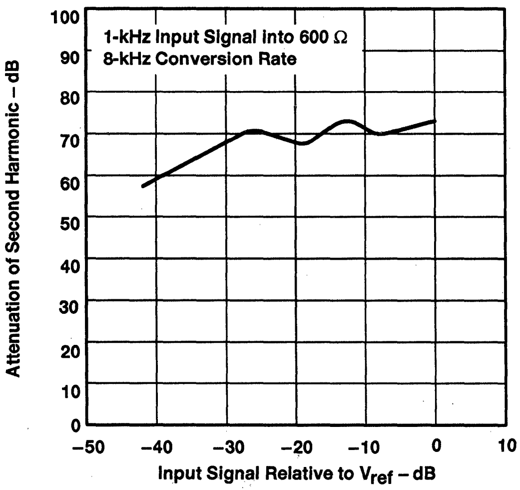


Figure 14

ATTENUATION OF THIRD HARMONIC OF D/A INPUT vs INPUT SIGNAL

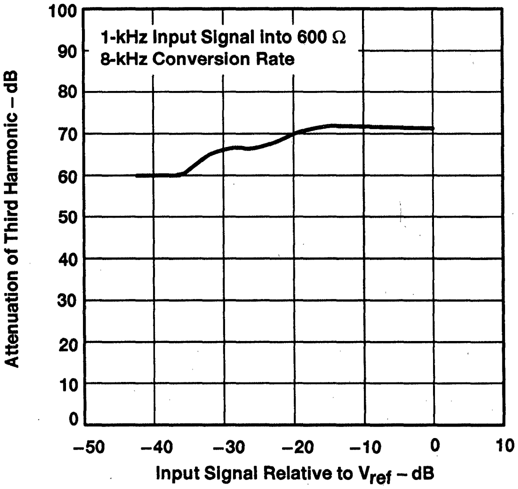


Figure 15

NOTE: Test conditions are V_{CC+}, V_{CC-}, and V_{DD} within recommended operating conditions set clock f = 288 kHz ±2%, and T_A = 25°C.

APPLICATION INFORMATION

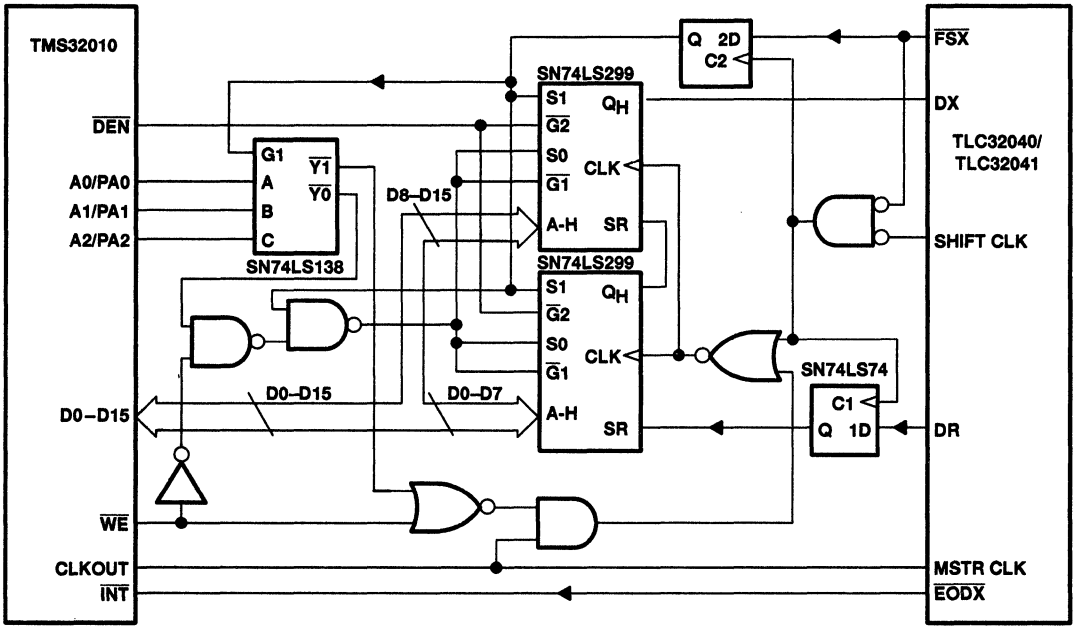
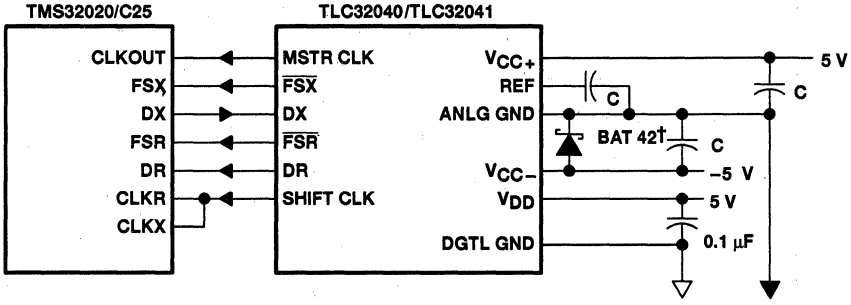


Figure 16. TMS32010-TLC32040/TLC32041 Interface Circuit

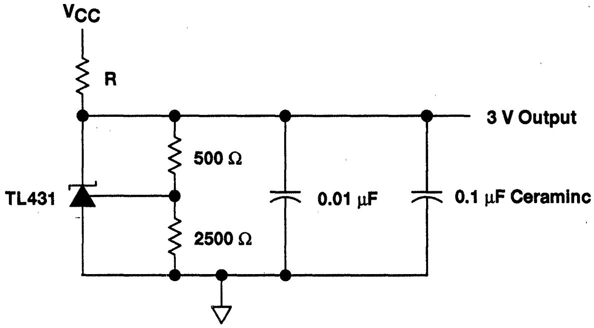
APPLICATION INFORMATION



C = 0.2 µF, Ceramic

Figure 17. AIC Interface to the TMS32020/C25 Showing Decoupling Capacitors and Schottky Diode†

† Thomson Semiconductors

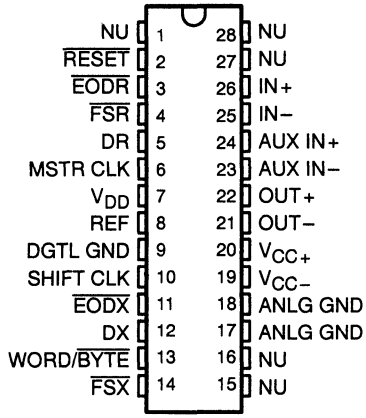


For: V_{CC} = 12 V, R = 7200 Ω
V_{CC} = 10 V, R = 5600 Ω
V_{CC} = 5 V, R = 1600 Ω

Figure 18. External Reference Circuit For TLC32045

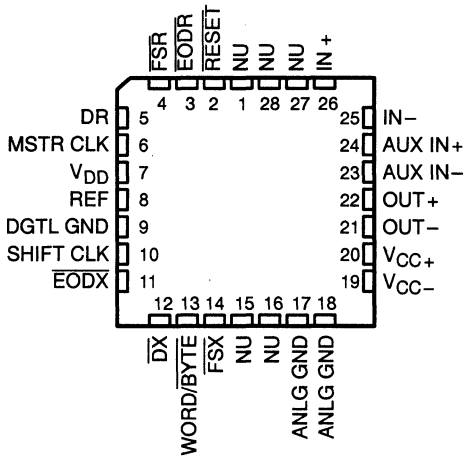
- **14-Bit Dynamic Range ADC and DAC**
- **2's Complement Format**
- **Variable ADC and DAC Sampling Rate Up to 19,200 Samples per Second**
- **Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter**
- **Serial Port for Direct Interface to TMS(SMJ)320C17, TMS(SMJ)32020, TMS(SMJ)320C25, and TMS320C30 Digital Signal Processors**
- **Synchronous or Asynchronous ADC and DAC Conversion Rates With Programmable Incremental ADC and DAC Conversion Timing Adjustments**
- **Serial Port Interface to SN74(54)299 Serial-to-Parallel Shift Register for Parallel Interface to TMS(SMJ)32010, TMS(SMJ)320C15, or Other Digital Processors**
- **Internal Reference for Normal Operation and External Purposes, or Can Be Overridden by External Reference**
- **CMOS Technology**

J† OR N PACKAGE
(TOP VIEW)



† Refer to the mechanical data for the JT package.

FK OR FN PACKAGE
(TOP VIEW)



NU – Nonusable; no external connection should be made to these terminals (see Table 2).

description

The TLC32044 and TLC32045 are complete analog-to-digital and digital-to-analog input and output systems on single monolithic CMOS chips. The TLC32044 and TLC32045 integrate a bandpass switched-capacitor antialiasing input filter, a 14-bit-resolution A/D converter, four microprocessor-compatible serial port modes, a 14-bit-resolution D/A converter, and a low-pass switched-capacitor output-reconstruction filter. The devices offer numerous combinations of master clock input frequencies and conversion/sampling rates, which can be changed via digital processor control.

AVAILABLE OPTIONS

T_A	PACKAGE			
	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)	CERAMIC DIP (J)	CHIP CARRIER (FK)
0°C to 70°C	TLC32044CFN	TLC32044CN		
	TLC32045CFN	TLC32045CN		
−20°C to 85°C	TLC32044EFN			
−40°C to 85°C		TLC32044IN		
		TLC32045IN		
−55°C to 125°C			TLC32044MJ	TLC32044MFK

description (continued)

Typical applications for the TLC32044 and TLC32045 include speech encryption for digital transmission, speech recognition/ storage systems, speech synthesis, modems (7.2-, 8-, 9.6-, 14.4-, and 19.2-kHz sampling rate), analog interface for digital signal processors (DSPs), industrial process control, biomedical instrumentation, acoustical signal processing, spectral analysis, data acquisition, and instrumentation recorders. Four serial modes, which allow direct interface to the TMS(SMJ)320C17, TMS(SMJ)32020, TMS(SMJ)320C25, and TMS(SMJ)320C30 digital signal processors, are provided. Also, when the transmit and receive sections of the analog interface circuit (AIC) are operating synchronously, it will interface to two SN74(54)299 serial-to-parallel shift registers. These serial-to-parallel shift registers can then interface in parallel to the TMS(SMJ)32010, TMS(SMJ)320C15, and other digital signal processors, or external FIFO circuitry. Output data pulses are emitted to inform the processor that data transmission is complete or to allow the DSP to differentiate between two transmitted bytes. A flexible control scheme is provided so that the functions of the TLC32044 or TLC32045 can be selected and adjusted coincidentally with signal processing via software control.

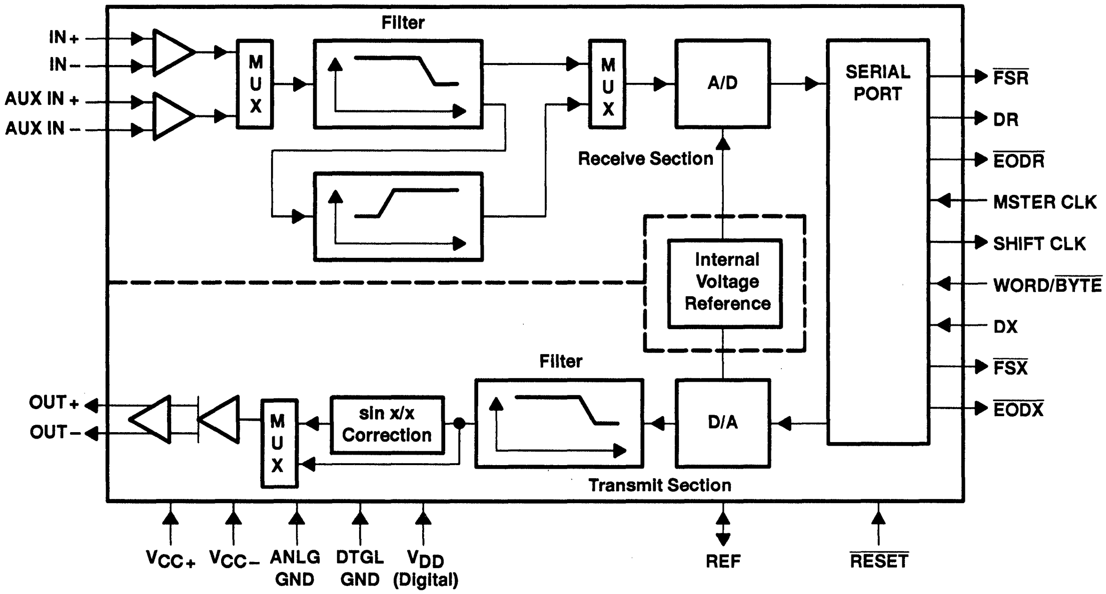
The antialiasing input filter comprises eighth-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When only low-pass filtering is desired, the high-pass filter can be switched out of the signal path. A selectable, auxiliary, differential analog input is provided for applications where more than one analog input is required.

The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided to ease the design task and to provide complete control over the performance of the TLC32044 or TLC32045. The internal voltage reference is brought out to a terminal and is available to the designer. Separate analog and digital voltage supplies and grounds are provided to minimize noise and ensure a wide dynamic range. Also, the analog circuit path contains only differential circuitry to keep noise to an absolute minimum. The only exception is the DAC sample and hold, which utilizes pseudo-differential circuitry.

The output-reconstruction filter is an eighth-order CC-type (Chebyshev/elliptic transitional low-pass filter) followed by a second-order (sin x)/x correction filter and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the digitally encoded signal. The on-board (sin x)/x correction filter can be switched out of the signal path using digital signal processor control, if desired.

The TLC32044C and TLC32045C are characterized for operation from 0°C to 70°C. The TLC32044E is characterized for operation from −20°C to 85°C. The TLC32044I and TLC32045I are characterized for operation from −40°C to 85°C. The TLC32044M is characterized for operation from −55°C to 125°C.

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ANLG GND	17,18		Analog ground return for all internal analog circuits. Not internally connected to DGTL GND.
AUX IN+	24	I	Noninverting auxiliary analog input stage. AUX IN+ can be switched into the bandpass filter and A/D converter path via software control. If the appropriate bit in the control register is a 1, the auxiliary inputs will replace the IN+ and IN– inputs. If the bit is a 0, the IN+ and IN– inputs will be used (see the AIC DX data word format section).
AUX IN–	23	I	Inverting auxiliary analog input (see the above AUX IN+ description).
DGTL GND	9		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
DR	5	O	Data receive. DR is used to transmit the ADC output bits from the AIC to the TMS320 (SMJ320) serial port. This transmission of bits from the AIC to the TMS320 (SMJ320) serial port is synchronized with the SHIFT CLK signal.
DX	12	I	Data transmit. DX is used to receive the DAC input bits and timing and control information from the TMS320 (SMJ320). This serial transmission from the TMS320 (SMJ320) serial port to the AIC is synchronized with the SHIFT CLK signal.
$\overline{\text{EODR}}$	3	O	End of data receive. (See the WORD/$\overline{\text{BYTE}}$ description and Serial Port Timing diagram.) During the word-mode timing, $\overline{\text{EODR}}$ is a low-going pulse that occurs immediately after the 16 bits of A/D information have been transmitted from the AIC to the TMS320 (SMJ320) serial port. $\overline{\text{EODR}}$ can be used to interrupt a microprocessor upon completion of serial communications. Also, $\overline{\text{EODR}}$ can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM, and to facilitate parallel data bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, $\overline{\text{EODR}}$ goes low after the first byte has been transmitted from the AIC to the TMS320 (SMJ320) serial port and is kept low until the second byte has been transmitted. The DSP can use this low-going signal to differentiate between the two bytes as to which is first and which is second. $\overline{\text{EODR}}$ does not occur after secondary communication.

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{EODX}}$	11	O	End of data transmit. (See the WORD/$\overline{\text{BYTE}}$ description and Serial Port Timing diagram.) During the word-mode timing, $\overline{\text{EODX}}$ is a low-going pulse that occurs immediately after the 16 bits of D/A converter and control or register information have been transmitted from the TMS320 (SMJ320) serial port to the AIC. $\overline{\text{EODX}}$ can be used to interrupt a microprocessor upon the completion of serial communications. Also, $\overline{\text{EODX}}$ can be used to strobe and enable external serial-to-parallel shift registers, latches, or an external FIFO RAM, and to facilitate parallel data-bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, $\overline{\text{EODX}}$ goes low after the first byte has been transmitted from the TMS320 (SMJ320) serial port to the AIC and is kept low until the second byte has been transmitted. The DSP can use this low-going signal to differentiate between the two bytes as to which is first and which is second.
$\overline{\text{FSR}}$	4	O	Frame sync receive. In the serial transmission modes, which are described in the WORD/$\overline{\text{BYTE}}$ description, $\overline{\text{FSR}}$ is held low during bit transmission. When $\overline{\text{FSR}}$ goes low, the TMS320 (SMJ320) serial port begins receiving bits from the AIC via DR of the AIC. The most significant DR bit is present on DR before $\overline{\text{FSR}}$ goes low. (See Serial Port Timing and Internal Timing Configuration diagrams.) $\overline{\text{FSR}}$ does not occur after secondary communications.
$\overline{\text{FSX}}$	14	O	Frame sync transmit. When FSX goes low, the TMS320 (SMJ320) serial port begins transmitting bits to the AIC via DX of the AIC. In all serial transmission modes, which are described in the WORD/$\overline{\text{BYTE}}$ description, $\overline{\text{FSX}}$ is held low during bit transmission (see Serial Port Timing and Internal Timing Configuration diagrams).
IN+	26	I	Noninverting input to analog input amplifier stage
IN–	25	I	Inverting input to analog input amplifier stage
MSTR CLK	6	I	Master clock. MSTR CLK is used to derive all the key logic signals of the AIC, such as the shift clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The Internal Timing Configuration diagram shows how these key signals are derived. The frequencies of these key signals are synchronous submultiples of the master clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the A/D and D/A converters (see the Internal Timing Configuration diagram).
OUT+	22	O	Noninverting output of analog output power amplifier. OUT+ can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
OUT–	21	O	Inverting output of analog output power amplifier. OUT– is functionally identical with and complementary to OUT+.
REF	8	I/O	Internal voltage reference. An internal reference voltage is brought out on REF. An external voltage reference can also be applied to REF.
$\overline{\text{RESET}}$	2	I	Reset function. $\overline{\text{RESET}}$ is provided to initialize the TA, TA', TB, RA, RA', RB, and control registers. A reset initiates serial communications between the AIC and DSP. A reset initializes all AIC registers including the control register. After a negative-going pulse on $\overline{\text{RESET}}$, the AIC registers are initialized to provide an 8-khz data conversion rate for a 5.184-MHz master clock input signal. The conversion rate adjust registers, TA' and RA', are reset to 1. The control register bits are reset as follows (see AIC DX data word format section): d9 = 1, d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1. This initialization allows normal serial-port communication to occur between the AIC and DSP.
SHIFT CLK	10	O	Shift clock. SHIFT CLK is obtained by dividing the master clock signal frequency by four. SHIFT CLK is used to clock the serial data transfers of the AIC, described in the WORD/$\overline{\text{BYTE}}$ description below (see the Serial Port Timing and Internal Timing Configuration diagrams).
V_{DD}	7		Digital supply voltage, 5 V ±5%
V_{CC+}	20		Positive analog supply voltage, 5 V ±5%
V_{CC-}	19		Negative analog supply voltage, –5 V ±5%

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
WORD/$\overline{\text{BYTE}}$	13	I	Used in conjunction with a bit in the control register, WORD/$\overline{\text{BYTE}}$ is used to establish one of four serial modes. These four serial modes are described below. *AIC transmit and receive sections are operated asynchronously.* The following description applies when the AIC is configured to have asynchronous transmit and receive sections. If the appropriate data bit in the control register is a 0 (see the AIC DX data word format section), the transmit and receive sections are asynchronous. L Serial port directly interfaces with the serial port of the DSP and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams). 1. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ is brought low. 2. One 8-bit byte is transmitted or one 8-bit byte is received. 3. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ is brought low. 4. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ emits a positive frame-sync pulse that is four shift clock cycles wide. 5. One 8-bit byte is transmitted or one 8-bit byte is received. 6. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ is brought high. 7. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ is brought high. H Serial port directly interfaces with the serial ports of the TMS(SMJ)32020, TMS(SMJ)320C25, or TMS(SMJ)320C30, and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): 1. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ is brought low. 2. One 16-bit word is transmitted or one 16-bit word is received. 3. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ is brought high. 4. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ emits a low-going pulse. *AIC transmit and receive sections are operated synchronously.* If the appropriate data bit in the control register is 1, the transmit and receive sections are configured to be synchronous. In this case, the bandpass switched-capacitor filter and the A/D conversion timing are derived from the TX counter A, TX counter B, and TA, TA', and TB registers, rather than the RX counter A, RX counter B, and RA, RA', and RB registers. In this case, the AIC $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ timing are identical during primary data communication; however, $\overline{\text{FSR}}$ is not asserted during secondary data communication since there is no new A/D conversion result. The synchronous operation sequences are as follows (see Serial Port Timing diagrams). L Serial port directly interfaces with the serial port of the DSP and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams): 1. $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ are brought low. 2. One 8-bit byte is transmitted and one 8-bit byte is received. 3. $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ are brought low. 4. $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ emit positive frame-sync pulses that are four shift clock cycles wide. 5. One 8-bit byte is transmitted and one 8-bit byte is received. 6. $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ are brought high. 7. $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ are brought high. H Serial port directly interfaces with the serial port of the TMS(SJM)32020, TMS(SMJ)320C25, or TMS320C30, and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): 1. $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ are brought low. 2. One 16-bit word is transmitted and one 16-bit word is received. 3. $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ are brought high. 4. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ emit low-going pulses. Since the transmit and receive sections of the AIC are now synchronous, the AIC serial port with additional NOR and AND gates interface to two SN74(54)299 serial-to-parallel shift registers. Interfacing the AIC to the SN74(54)299 shift register allows the AIC to interface to an external FIFO RAM and facilitates parallel, data bus communications between the AIC and the digital signal processor. The operation sequence is the same as the above sequence (see Serial Port Timing diagrams).

PRINCIPLES OF OPERATION

analog input

Two sets of analog inputs are provided. Normally, the IN+ and IN– input set is used; however, the auxiliary input set, AUX IN + and AUX IN–, can be used if a second input is required. Each input set can be operated in either differential or single-ended modes, since sufficient common-mode range and rejection are provided. The gain for the IN +, IN–, AUX IN +, and AUX IN– inputs can be programmed to be either 1, 2, or 4 (see Table 2). Either input circuit can be selected via software control. It is important to note that a wide dynamic range is assured by the differential internal analog architecture and by the separate analog and digital voltage supplies and grounds.

A/D bandpass filter, A/D bandpass filter clocking, and A/D conversion timing

The A/D high-pass filter can be selected or bypassed via software control. The frequency response of this filter is presented in the following pages. This response results when the switched-capacitor filter clock frequency is 288 kHz and the A/D sample rate is 8 kHz. Several possible options can be used to attain a 288-kHz switched-capacitor filter clock. When the filter clock frequency is not 288 kHz, the low-pass filter transfer function is frequency scaled by the ratio of the actual clock frequency to 288 kHz. The ripple bandwidth and 3-dB low-frequency roll-off points of the high-pass section are 150 Hz and 100 Hz, respectively. However, the high-pass section low-frequency roll-off is frequency scaled by the ratio of the A/D sample rate to 8 kHz.

The internal timing configuration and AIC DX data word format sections of this data sheet indicate the many options for attaining a 288-kHz bandpass switched-capacitor filter clock. These sections indicate that the RX counter A can be programmed to give a 288-kHz bandpass switched-capacitor filter clock for several master clock input frequencies.

The A/D conversion rate is then attained by frequency dividing the 288-kHz bandpass switched-capacitor filter clock with the RX counter B. Unwanted aliasing is prevented because the A/D conversion rate is an integral submultiple of the bandpass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

A/D converter performance specifications

Fundamental performance specifications for the A/D converter circuitry are presented in the A/D converter operating characteristics section of this data sheet. The realization of the A/D converter circuitry with switched-capacitor techniques provides an inherent sample-and-hold.

analog output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

D/A low-pass filter, D/A low-pass filter clocking, and D/A conversion timing

The frequency response of this filter is presented in the following pages. This response results when the low-pass switched-capacitor filter clock frequency is 288 kHz. Like the A/D filter, the transfer function of this filter is frequency scaled when the clock frequency is not 288 kHz. A continuous-time filter is provided on the output of the (sin x) / x correction filter to eliminate the periodic sample data signal information, which occurs at multiples of the 288-kHz switched-capacitor filter clock. The continuous time filter also greatly attenuates any switched-capacitor clock feedthrough.

PRINCIPLES OF OPERATION

D/A low-pass filter, D/A low-pass filter clocking, and D/A conversion timing (continued)

The D/A conversion rate is attained by frequency dividing the 288-kHz switched-capacitor filter clock with TX Counter B. Unwanted aliasing is prevented because the D/A conversion rate is an integral submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.

asynchronous versus synchronous operation

If the transmit section of the AIC (low-pass filter and DAC) and receive section (bandpass filter and ADC) are operated asynchronously, the low-pass and bandpass filter clocks are independently generated from the master clock signal. Also, the D/A and A/D conversion rates are independently determined. If the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and bandpass filters. In synchronous operation, the A/D conversion timing is derived from, and is equal to, the D/A conversion timing (see description of the WORD/$\overline{\text{BYTE}}$ in the Terminal Functions table.)

D/A converter performance specifications

Fundamental performance specifications for the D/A converter circuitry are presented in the D/A converter operating characteristics section of the data sheet. The D/A converter has a sample-and-hold that is realized with a switched-capacitor ladder.

system frequency response correction

The (sin x)/x correction for the D/A converter zero-order sample-and-hold output can be provided by an on-board second-order (sin x)/x correction filter. This (sin x)/x correction filter can be inserted into or deleted from the signal path by digital signal processor control. When inserted, the (sin x)/x correction filter follows the switched-capacitor low-pass filter. When the TB register (see Internal Timing Configuration section) equals 36, the correction results of Figures 11 and 12 can be obtained.

The (sin x)/x correction can also be accomplished by deleting the on-board second-order correction filter and performing the (sin x)/x correction in digital signal processor software. The system frequency response can be corrected via DSP software to ±0.1-dB accuracy to a band edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, which requires only seven TMS320 (SMJ320) instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of only 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the (sin x)/x correction section for more details).

serial port

The serial port has four possible modes that are described in detail in the Terminal Functions table. These modes are briefly described below and in the functional description for WORD/$\overline{\text{BYTE}}$.

- The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the DSP.
- The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS(SMJ)32020, TMS(SMJ)320C25, and the TMS(SMJ)320C30.
- The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the DSP.
- The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS(SMJ)32020, TMS(SMJ)320C25, TMS(SMJ)320C30, or two SN74(54)299 serial-to-parallel shift registers, which can then interface in parallel to the TMS(SMJ)32010, TMS(SMJ)320C15, and SMJ320E15 to any other digital signal processor or to external FIFO circuitry.

PRINCIPLES OF OPERATION

operation of TLC32044 or TLC32045 with internal voltage reference

The internal reference eliminates the need for an external voltage reference and provides overall circuit cost reduction. Thus, the internal reference eases the design task and provides complete control over device performance. The internal reference is brought out to a terminal and is available to the designer. To keep the amount of noise on the reference signal to a minimum, an external capacitor can be connected between REF and ANLG GND.

operation of TLC32044 or TLC32045 with external voltage reference

REF can be driven from an external reference circuit. This external circuit must be capable of supplying 250 μA and must be adequately protected from noise such as crosstalk from the analog input.

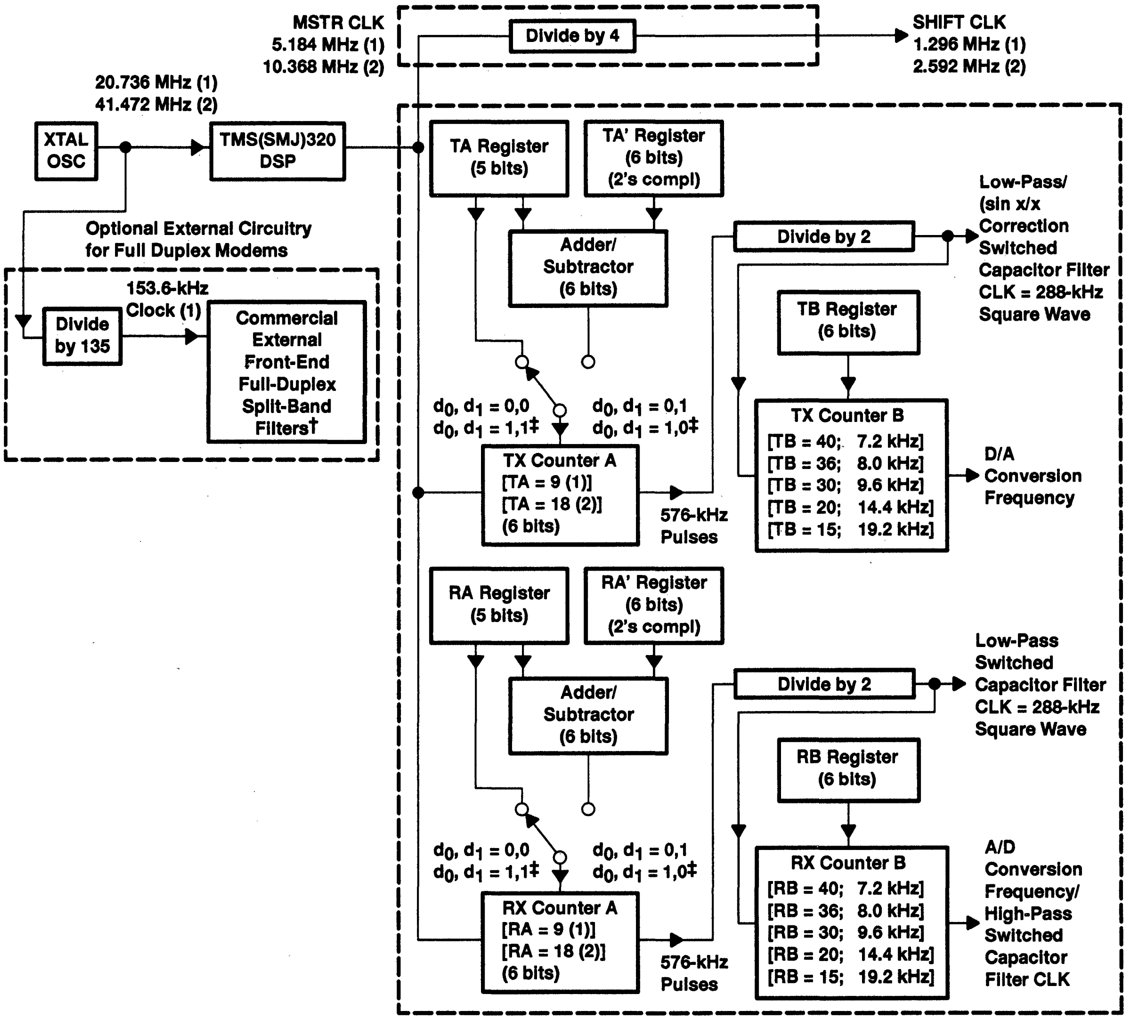
reset

A reset function is provided to initiate serial communications between the AIC and DSP and to allow fast, cost-effective testing during manufacturing. The reset function initializes all AIC registers, including the control register. After a negative-going pulse on $\overline{\text{RESET}}$, the AIC is initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX data word format section).

loopback

This feature allows the user to test the circuit remotely. In loopback, OUT+ and OUT– are internally connected to the IN+ and IN–. Thus, the DAC bits (d15 to d2), which are transmitted to DX, can be compared with the ADC bits (d15 to d2), which are received from DR. An ideal comparison would be that the bits on DR equal the bits on DX. However, there are some difference in these bits due to the ADC and DAC output offsets. The loopback feature is implemented with digital signal processor control by transmitting the appropriate serial port bit to the control register (see AIC DX data word format section).

INTERNAL TIMING CONFIGURATION



† Split-band filtering can alternatively be performed after the analog input function via software in the TMS(SMJ)320.
‡ These control bits are described in the AIC DX data word format section.

NOTE: Frequency 1 (20.736 MHz) is used to show how 153.6 kHz (for a commercially available modem split-band filter clock), popular speech and modem sampling signal frequencies, and an internal 288-kHz switched-capacitor filter clock can be derived synchronously and as submultiples of the crystal oscillator frequency. Since these derived frequencies are synchronous submultiples of the crystal frequency, aliasing does not occur as the sampled analog signal passes between the analog converter and switched-capacitor filter stages. Frequency 2 (41.472 MHz) is used to show that the AIC can work with high-frequency signals, which are used by high-speed digital signal processors.

explanation of internal timing configuration

All of the internal timing of the AIC is derived from the high-frequency clock signal that drives the master clock input. The shift clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the master clock input signal frequency by four.

Low-pass:

$$\text{SCF Clock Frequency (D/A or A/D path)} = \frac{\text{Master Clock Frequency}}{2 \times \text{Contents of Counter A}}$$

$$\text{Conversion Frequency} = \frac{\text{SCF Clock Frequency (D/A or A/D path)}}{\text{Contents of Counter B}}$$

High-pass:

$$\text{SCF Clock Frequency (A/D Path)} = \text{A/D Conversion Frequency}$$

$$\text{Shift Clock Frequency} = \frac{\text{Master Clock Frequency}}{4}$$

TX counter A and TX counter B, which are driven by the master clock, determine the D/A conversion timing. Similarly, RX counter A and RX counter B determine the A/D conversion timing. In order for the low-pass switched-capacitor filter in the D/A path to meet its transfer function specifications, the frequency of its clock input must be 288 kHz. If the clock frequency is not 288 kHz, the filter transfer function frequencies are frequency-scaled by the ratios of the clock frequency to 288 kHz. Thus, to obtain the specified filter response, the combination of master clock frequency and TX counter A and RX counter A values must yield a 288-kHz switched-capacitor clock signal. This 288-kHz clock signal can then be divided by the TX counter B to establish the D/A conversion timing.

The transfer function of the bandpass switched-capacitor filter in the A/D path is a composite of its high-pass and low-pass section transfer functions. The high-frequency roll-off of the low-pass section meets the bandpass filter transfer function specification when the low-pass section SCF is 288 kHz. Otherwise, the high-frequency roll-off will be frequency-scaled by the ratio of the high-pass section's SCF clock to 288 kHz. The low-frequency roll-off of the high-pass section meets the bandpass filter transfer function specification when the A/D conversion rate is 8 kHz. Otherwise, the low-frequency roll-off of the high-pass section is frequency-scaled by the ratio of the A/D conversion rate to 8 kHz.

TX counter A and TX counter B are reloaded every D/A conversion period, while RX counter A and RX counter B are reloaded every A/D conversion period. The TX counter B and RX counter B are loaded with the values in the TB and RB registers, respectively. Via software control, the TX counter A can be loaded with either the TA register, the TA register less the TA' register, or the TA register plus the TA' register. By selecting the TA register less the TA' register option, the upcoming conversion timing occurs earlier by an amount of time that equals TA' times the signal period of the master clock. By selecting the TA register plus the TA' register option, the upcoming conversion timing occurs later by an amount of time that equals TA' times the signal period of the master clock. The D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. In this case, however, the RX counter A can be programmed via software control with the RA register, the RA register less the RA' register, or the RA register plus the RA' register.

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing. This feature can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.

explanation of internal timing configuration (continued)

If the transmit and receive sections are configured to be synchronous (see WORD/$\overline{\text{BYTE}}$ description), then both the low-pass and bandpass switched-capacitor filter clocks are derived from TX counter A. Also, both the D/A and A/D conversion timing are derived from the TX counter A and TX counter B. When the transmit and receive sections are configured to be synchronous, the RX counter A, RX counter B, RA register, RA' register, and RB registers are not used.

AIC DR or DX word bit pattern

A/D or D/A MSB, 1st bit sent								1st bit sent of 2nd byte					A/D or D/A LSB		
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

AIC DX data word format section

d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	Comments
primary DX serial communication protocol																
←d15 (MSB) through d2 go to the D/A converter register →														0	0	The TX and RX counter As are loaded with the TA and RA register values. The TX and RX counter Bs are loaded with TB and RB register values.
←d15 (MSB) through d2 go to the D/A converter register →														0	1	The TX and RX counter As are loaded with the TA + TA' and RA + RA' register values. The TX and RX counter Bs are loaded with the TB and RB register values. LSBs d1 = 0 and d0 =1 cause the next D/A and A/D conversion periods to be changed by the addition of TA' and RA' master clock cycles, in which TA' and RA' can be positive or negative or zero (refer to Table 1).
←d15 (MSB) through d2 go to the D/A converter register →														1	0	The TX and RX counter As are loaded with the TA – TA' and RA – RA' register values. The TX and RX counter Bs are loaded with the TB and RB register values. LSBs d1 = 1 and d0 = 0 cause the next D/A and A/D conversion periods to be changed by the subtraction of TA' and RA' master clock cycles, in which TA' and RA' can be positive or negative or zero (refer to Table 1).
←d15 (MSB) through d2 go to the D/A converter register →														1	1	The TX and RX counter As are loaded with the TA and RA register converter register values. The TX and RX counter Bs are loaded with the TB and RB register values. After a delay of four shift clock cycles, a secondary transmission immediately follows to program the AIC to operate in the desired configuration.

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (primary communications) to the AIC initiates secondary communications upon completion of the primary communications. Upon completion of the primary communication, $\overline{\text{FSX}}$ remains high for four shift clock cycles and then goes low and initiates the secondary communication. The timing specifications for the primary and secondary communications are identical. In this manner, the secondary communication, if initiated, is interleaved between successive primary communications. This interleaving prevents the secondary communication from interfering with the primary communications and DAC timing, thus preventing the AIC from skipping a DAC output. In the synchronous mode, $\overline{\text{FSR}}$ is not asserted during secondary communications.

secondary DX serial communication protocol

x x I ← to TA register → I x x I ← to RA register → I	0 0	d13 and d6 are MSBs (unsigned binary)
x I ← to TA' register → I x I ← to RA' register → I	0 1	d14 and d7 are 2's complement sign bits
x I ← to TB register → I x I ← to RB register → I	1 0	d14 and d7 are MSBs (unsigned binary)
x x x x x x d9 x d7 d6 d5 d4 d3 d2	1 1	
Control Register		d2 = 0/1 deletes/inserts the A/D high-pass filter d3 = 0/1 disables/enables the loopback function d4 = 0/1 disables/enables the AUX IN+ and AUX IN– d5 = 0/1 asynchronous/synchronous transmit and receive sections d6 = 0/1 gain control bits (see gain control section) d7 = 0/1 gain control bits (see gain control section) d9 = 0/1 delete/insert on-board second-order (sin x)/x correction filter

reset function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After power has been applied to the AIC, a negative-going pulse on $\overline{\text{RESET}}$ initializes the AIC registers to provide an 8-kHz A/D and D/A conversion rate for a 5.184 MHz master clock input signal. The AIC, except the control register, is initialized as follows (see AIC DX data word format section):

REGISTER	INITIALIZED REGISTER VALUE (HEX)
TA	9
TA'	1
TB	24
RA	9
RA'	1
RB	24

The control register bits are reset as follows (see AIC DX data word format section):

d9 = 1, d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1

This initialization allows normal serial port communications to occur between AIC and DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA', and TB register need to be programmed, since both transmit and receive timing are synchronously derived from these registers (see the terminal functions table and AIC DX word format sections).

The circuit shown in Figure 1 provides a reset on power up when power is applied in the sequence given under power-up sequence. The circuit depends on the power supplies reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.

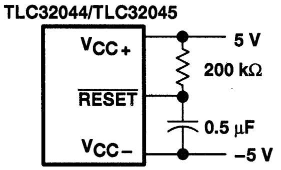


Figure 1. Power-Up Reset

power-up sequence

To ensure proper operation of the AIC and as a safeguard against latch-up, it is recommended that Schottky diodes with forward voltages less than or equal to 0.4 V be connected from V_{CC-} to ANLG GND and from V_{CC-} to DGTL GND (see Figure 21). In the absence of such diodes, power should be applied in the following sequence: ANLG GND and DGTL GND, V_{CC-}, then V_{CC+} and V_{DD}. Also, no input signal should be applied until after power up.

AIC responses to improper conditions

The AIC has provisions for responding to improper conditions. These improper conditions and the response of the AIC to these conditions are presented in Table 1 below.

AIC register constraints

The following constraints are placed on the contents of the AIC registers:

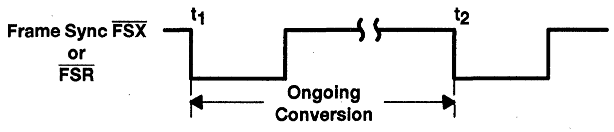
1. TA register must be ≥ 4 in word mode (WORD/$\overline{\text{BYTE}}$ = high).
2. TA register must be ≥ 5 in byte mode (WORD/$\overline{\text{BYTE}}$ = low).
3. TA' register can be either positive, negative, or zero.
4. RA register must be ≥ 4 in word mode (WORD/$\overline{\text{BYTE}}$ = high).
5. RA register must be ≥ 5 in byte mode (WORD/$\overline{\text{BYTE}}$ = low).
6. RA' register can be either positive, negative, or zero.
7. (TA register ± TA' register) must be > 1.
8. (RA register ± RA' register) must be > 1.
9. TB register must be > 1.

Table 1. AIC Responses to Improper Conditions

IMPROPER CONDITION	AIC RESPONSE
TA register + TA' register = 0 or 1 TA register – TA' register = 0 or 1	Reprogram TX counter A with TA register value
TA register + TA' register < 0	MODULO 64 arithmetic is used to ensure that a positive value is loaded into the TX counter A, i.e., TA register + TA' register + 40 hex is loaded into TX counter A.
RA register + RA' register = 0 or 1 RA register – RA' register = 0 or 1	Reprogram RX counter A with RA register value
RA register + RA' register = 0 or 1	MODULO 64 arithmetic is used to ensure that a positive value is loaded into RX counter A, i.e., RA register + RA' register + 40 hex is loaded into RX counter A.
TA register = 0 or 1 RA register = 0 or 1	AIC is shut down.
TA register < 4 in word mode TA register < 5 in byte mode RA register < 4 in word mode RA register < 5 in byte mode	The AIC serial port no longer operates.
TB register = 0 or 1	Reprogram TB register with 24 hex
RB register = 0 or 1	Reprogram RB register with 24 hex
AIC and DSP cannot communicate	Hold last DAC output

improper operation due to conversion times being too close together

If the difference between two successive D/A conversion frame syncs is less than 1/19.2 kHz, the AIC operates improperly. In this situation, the second D/A conversion frame sync occurs too quickly and there is not enough time for the ongoing conversion to be completed. This situation can occur if the A and B registers are improperly programmed or if the A + A' register or A – A' register result is too small. When incrementally adjusting the conversion period via the A + A' register options, the designer should be careful not to violate this requirement (see following diagram).



$t_2 - t_1 \geq 1/19.2$ kHz

asynchronous operation — more than one receive frame sync occurring between two transmit frame syncs

When incrementally adjusting the conversion period via the A + A' or A – A' register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during a $\overline{FSX}$ frame sync. The ongoing conversion period is then adjusted. However, either receive conversion period A or B can be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. Therefore, if there is sufficient time between t_1 and t_2, the receive conversion period adjustment is performed during receive conversion period A. Otherwise, the adjustment is performed during receive conversion period B. The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent $\overline{FSX}$ frame (see figure below).

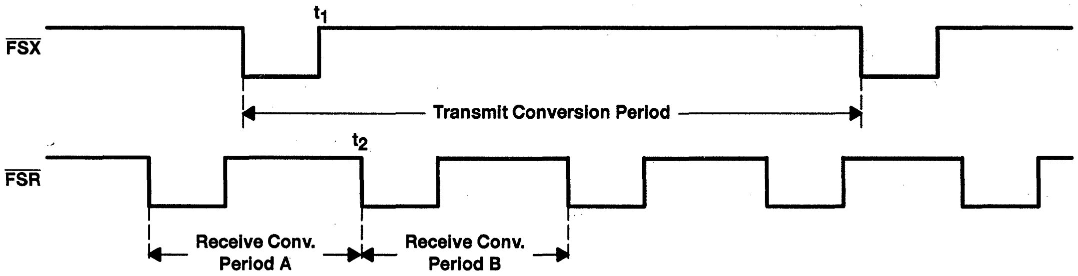


Figure 2. Adjusted Transmit and Receive Conversion Periods

asynchronous operation — more than one transmit frame sync occurring between two receive frame syncs

When incrementally adjusting the conversion period via the A + A' or A – A' register options, a specific protocol is followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during a $\overline{FSX}$ frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment in the diagram as shown in the following figure. If the adjustment command is issued during transmit conversion period A, receive conversion period A is adjusted if there is sufficient time between t_1 and t_2. If there is not sufficient time between t_1 and t_2, receive conversion period B is adjusted. The receive portion of an adjustment command can be ignored if the adjustment command is sent during a receive conversion period, which is already being or will be adjusted due to a prior adjustment command. For example, if adjustment commands are issued during transmit conversion periods A, B, and C, the first two commands can cause receive conversion periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during receive conversion period B, which already is adjusted via the transmit conversion period B adjustment command.

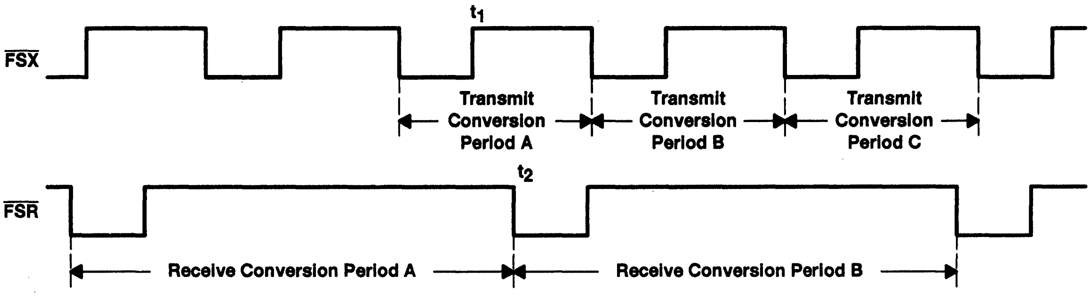


Figure 3. Receive and Transmit Conversion Period Adjustments

asynchronous operation — more than one set of primary and secondary DX serial communication occurring between two receive frame sync (see AIC DX data word format section)

The TA, TA', TB, and control register information that is transmitted in the secondary communications is always accepted and is applied during the ongoing transmit conversion period. If there is sufficient time between t_1 and t_2, the TA, RA', and RB register information, which is sent during transmit conversion period A, is applied to receive conversion period A. Otherwise, this information is applied during receive conversion period B. If RA, RA', and RB register information has already been received and is being applied during an ongoing conversion period, any subsequent RA, RA', or RB information that is received during this receive conversion period is disregarded (see Figure 4).

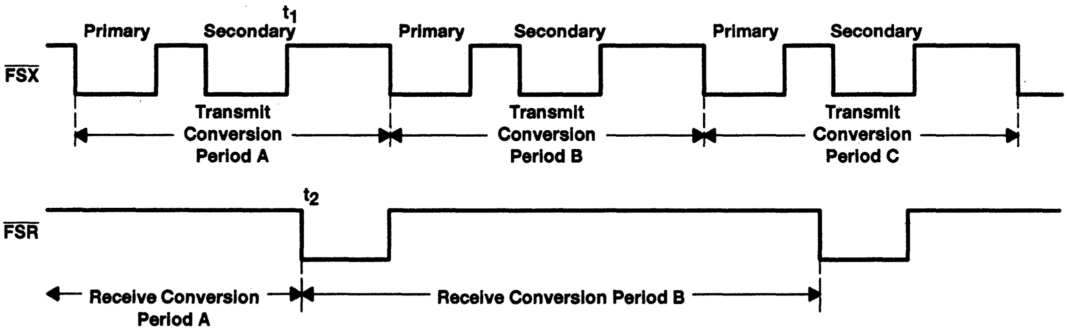


Figure 4. Receive and Transmit Periods for Primary and Secondary Data

test modes†

The TLC32044 or TLC32045 can be operated in special test modes. These test modes are used by Texas Instruments to facilitate testing of the device during manufacturing. They are not intended to be used in real applications, however, they allow the filters in the A/D and D/A paths to be used without using the A/D and D/A converters.

In normal operation, the nonusable (NU) terminals are left unconnected. These NU terminals are used by the factory to speed up testing of the TLC32044 or TLC32045 analog interface circuits (AIC). When the device is used in normal (non-test mode) operation, the NU terminal (terminal 1) has an internal pulldown to −5 V. Externally connecting 0 V or 5 V to terminal 1 puts the device in test-mode operation. Selecting one of the possible test modes is accomplished by placing a particular voltage on certain terminals. A description of these modes is provided in Table 2 and Figures 5 and 6.

Table 2. List of Test Modes

TEST TERMINALS	D/A PATH TEST (TERMINAL 1 to 5 V)	A/D PATH TEST (TERMINAL 1 to 0)
	TEST FUNCTION	**TEST FUNCTION**
5	The low-pass switched-capacitor filter clock is brought out to DR. This clock signal is normally internal.	The bandpass switched-capacitor filter clock is brought out to DR. This clock signal is normally internal.
11	No change from normal operation. The $\overline{\text{EODX}}$ signal is brought out to $\overline{\text{EODX}}$.	The pulse that initiates the A/D conversion is brought out here. This signal is normally internal.
3	The pulse that initiates the D/A conversion is brought out here.	No change from normal operation. The $\overline{\text{EODR}}$ signal is brought out.
27 and 28	There are no test output signals provided on these terminals.	The outputs of the A/D path low-pass or bandpass filter (depending upon control bit d2 – see AIC DX data word format section) are brought out to these terminals. If the high-pass section is inserted, the output will have a (sin x) / x droop. The slope of the droop is determined by the ADC sampling frequency, which is the high-pass section clock frequency (see diagram of bandpass or low-pass filter test for receive section). These outputs drive small (30-pF) loads.
15 and 16	**D/A PATH LOW-PASS FILTER TEST; (WORD/$\overline{\text{BYTE}}$) to −5 V**	
	TEST FUNCTION	
	The inputs of the D/A path low-pass filter are brought out to terminals 15 and 16. The D/A input to this filter is removed. If (sin x) / x correction filter is inserted, the OUT+ and OUT− signals have a flat response (see Figure 2). The common-mode range of these inputs must not exceed ±0.5 V.	

† In the test mode, the AIC responds to the setting of WORD/$\overline{\text{BYTE}}$ to −5 V, as if WORD/$\overline{\text{BYTE}}$ were set to 0 V. Thus, the byte mode is selected for communicating between DSP and AIC. Either of the path tests (D/A or A/D) can be performed simultaneously with the D/A low-pass filter test. In this situation, WORD/$\overline{\text{BYTE}}$ must be connected to −5 V, which initiates byte-mode communications.

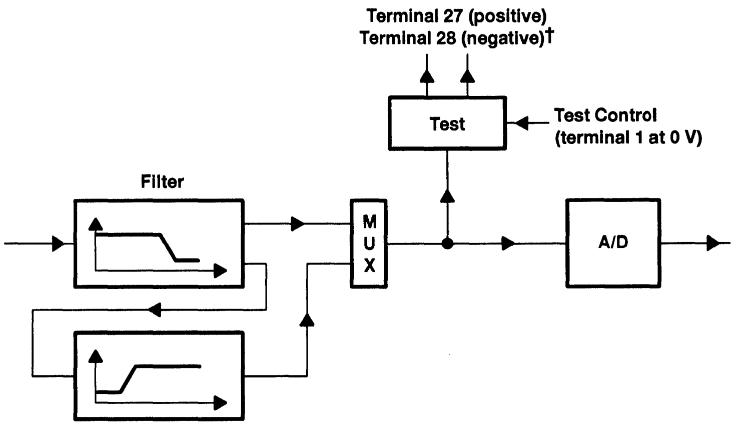


Figure 5. Bandpass or Low-Pass Filter Test for Receiver Section

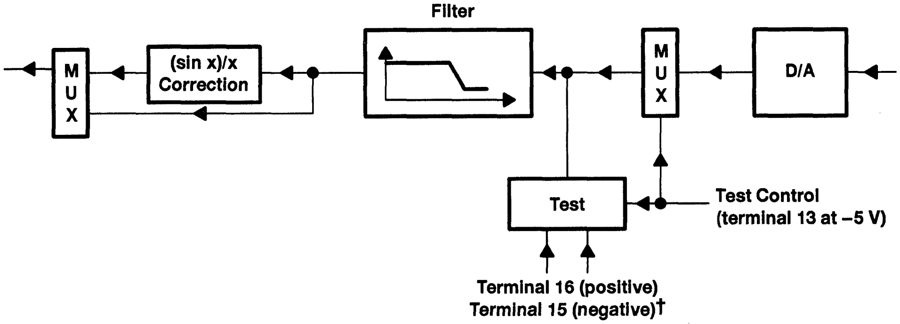


Figure 6. Low-Pass Filter Test for Transmit Section

† All analog signal paths have differential architecture and hence have positive and negative components.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC+} (see Note 1) .... –0.3 V to 15 V
Supply voltage range, V_{DD} .... –0.3 V to 15 V
Output voltage range, V_O .... –0.3 V to 15 V
Input voltage range, V_I .... –0.3 V to 15 V
Digital ground voltage range .... –0.3 V to 15 V
Operating free-air temperature range: TLC32044C, TLC32045C .... 0°C to 70°C
TLC32044E .... –20°C to 85°C
TLC32044I, TLC32045I .... –40°C to 85°C
TLC32044M .... –55°C to 125°C
Storage temperature range: TLC32044C, I, TLC32045C, I .... –40°C to 125°C
TLC32044M .... –65°C to 150°C
Case temperature for 10 seconds: FN or FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package .... 260°C
J package .... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values for maximum ratings are with respect to V_{CC-}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} (see Note 2)		4.75	5	5.25	V
Supply voltage, V_{CC-} (see Note 2)		–4.75	–5	–5.25	V
Digital supply voltage, V_{DD} (see Note 2)		4.75	5	5.25	V
Digital ground voltage with respect to ANLG GND, DGTL GND			0		V
Reference input voltage, $V_{ref(ext)}$ (see Note 2)		2		4	V
High-level input voltage, V_{IH}		2		V_{DD}+0.3	V
Low-level input voltage, V_{IL} (see Note 3)		–0.3		0.8	V
Load resistance at OUT+ and/or OUT–, R_L		300			Ω
Load capacitance at OUT+ and/or OUT–, C_L				100	pF
MSTR CLK frequency (see Note 4)		0.075	5	10.368	MHz
Analog input amplifier common mode input voltage (see Note 5)				±1.5	V
A/D or D/A conversion rate				20	kHz
Operating free-air temperature, T_A	TLC32044C, TLC32045C	0		70	°C
	TLC32044E	–20		85	
	TLC32044I, TLC32045I	–40		85	
	TLC32044M	–55		125	

NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+}, and V_{CC-}, are with respect to the ANLG GND terminal. Voltages at digital inputs and outputs and V_{DD} are with respect to the DGTL GND terminal.
3. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.
4. The bandpass switched-capacitor filter (SCF) specifications apply only when the low-pass section SCF clock is 288 kHz and the high-pass section SCF clock is 8 kHz. If the low-pass SCF clock is shifted from 288 kHz, the low-pass roll-off frequency will shift by the ratio of the low-pass SCF clock to 288 kHz. If the high-pass SCF is shifted from 8 kHZ, the high-pass roll-off frequency will shift by the ratio of the high-pass SCF clock to 8 kHz. Similarly, the low-pass switched-capacitor filter (SCF) specifications apply only when the SCF clock is 288 kHz. If the SCF clock is shifted from 288 kHz, the low-pass roll-off frequency will shift by the ratio of the SCF clock to 288 kHz.
5. This range applies when (IN+ – IN–) or (AUX IN+ – AUX IN–) equals ± 6 V.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted)

total device, MSTR CLK frequency = 5.184 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 4.75 V, I_{OH} = −300 μA	2.4			V
V_{OL}	Low-level output voltage		V_{DD} = 4.75 V, I_{OL} = 2 mA			0.4	V
I_{CC+}	Supply current from V_{CC+}	TLC32044C, TLC32045C				35	mA
		TLC32044I, TLC32045I, TLC32044E, TLC32044M				40	mA
I_{CC-}	Supply current from V_{CC-}	TLC32044C, TLC32045C				−35	mA
		TLC32044I, TLC32045I, TLC32044E, TLC32044M				−40	mA
I_{DD}	Supply current from V_{DD}	TLC3204xC, E, I	$f_{MSTR\ CLK}$ = 5.184 MHz			7	mA
		TLC32044M				8	mA
V_{ref}	Internal reference output voltage	TLC3204xC, E, I		3		3.3	V
		TLC32044M		2.9		3.3	V
αV_{ref}	Temperature coefficient of internal reference voltage				200		ppm/°C
r_o	Output resistance at REF				100		kΩ

receive amplifier input

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	A/D converter offset error (filters in)	TLC32044C, E, I			10	70	mV
		TLC32044M			10	85	mV
		TLC32045C, I			10	75	mV
CMRR	Common-mode rejection ratio at IN+, IN−, or AUX IN+, AUX IN−	TLC3204xC, E, I	See Note 6		55		dB
		TLC32044M	See Note 6	35	55		dB
r_i	Input resistance at IN+, IN−, or AUX IN+, AUX IN−, REF				100		kΩ

transmit filter output

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset voltage at OUT+ OUT− (single-ended relative to ANLG GND)	TLC3204xC, E, I			15	80	mV
		TLC32044M			15	75	mV
V_{OM}	Maximum peak output voltage swing across R_L at OUT+ or OUT− (single ended)		R_L ≥ 300 Ω, Offset voltage = 0	±3			V
V_{OM}	Maximum peak output voltage swing between OUT+ and OUT− (differential output)		R_L ≥ 600 Ω	±6			V

† All typical values are at T_A = 25°C.
NOTE 6: The test condition is a 0-dBm, 1-kHz input signal with an 8-kHz conversion rate.

system distortion specifications, SCF clock frequency = 288 kHz (see Note 7)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Attenuation of second harmonic of A/D input signal	Single ended	TLC3204xC, E, I	V_I = −0.5 dB to −24 dB referred to V_{ref}, T_A = 25°C		70		dB
		TLC32044M		62	70		
	Differential	TLC32044C, E, I	V_I = −0.5 dB to −24 dB referred to V_{ref}	62	70		
		TLC32045C, I		55	70		
Attenuation of third and higher harmonics of A/D input signal	Single ended	TLC3204xC, E, I	V_I = −0.5 dB to −24 dB referred to V_{ref}, T_A = 25°C		65		
		TLC32044M		57	65		
	Differential	TLC32044C, E, I	V_I = −0.5 dB to −24 dB referred to V_{ref}	57	65		
		TLC32045C, I		55	65		
Attenuation of second harmonic of D/A input signal	Single ended	TLC3204xC, I, M	V_I = −0 dB to −24 dB referred to V_{ref}		70		
	Differential	TLC32044C, E, I		62	70		
		TLC32045C, I		55	70		
Attenuation of third and higher harmonics of D/A input signal	Single ended	TLC3204xC, I, M	V_I = −0 dB to −24 dB referred to V_{ref}		65		
	Differential	TLC32044C, E, I		57	65		
		TLC32045C, I		55	65		

† All typical values are at T_A = 25°C.

NOTE 7: The test condition V_I is a 1-kHz input signal with an 8-kHz conversion rate (0 dB relative to V_{ref}). The load impedance for the DAC is 600 Ω (300 Ω for TLC32044M).

A/D channel signal-to-distortion ratio (see Note 7)

PARAMETER	TEST CONDITIONS	$A_V = 1$† MIN	$A_V = 1$† MAX	$A_V = 2$† MIN	$A_V = 2$† MAX	$A_V = 4$† MIN	$A_V = 4$† MAX	UNIT
A/D channel signal-to-distortion ratio, TLC32044C, TLC32044I, TLC32044E	V_I = −6 dB to −0.1 dB	58		>58‡		>58‡		dB
	V_I = −12 dB to −6 dB	58		58		>58‡		
	V_I = −18 dB to −12 dB	56		58		58		
	V_I = −24 dB to −18 dB	50		56		58		
	V_I = −30 dB to −24 dB	44		50		56		
	V_I = −36 dB to −30 dB	38		44		50		
	V_I = −42 dB to −36 dB	32		38		44		
	V_I = −48 dB to −42 dB	26		32		38		
	V_I = −54 dB to −48 dB	20		26		32		
A/D channel signal-to-distortion ratio, TLC32044M	V_I = −6 dB to −0.5 dB	58		>58‡		>58‡		
	V_I = −12 dB to −6 dB	58		58		>58‡		
	V_I = −18 dB to −12 dB	56		58		58		
	V_I = −24 dB to −18 dB	50		56		58		
	V_I = −30 dB to −24 dB	44		50		56		
	V_I = −36 dB to −30 dB	38		44		50		
	V_I = −42 dB to −36 dB	32		38		44		
	V_I = −48 dB to −42 dB	26		32		38		
	V_I = −54 dB to −48 dB	20		26		32		
A/D channel signal-to-distortion ratio, TLC32045C, TLC32045I	V_I = −6 dB to −0.1 dB	55		>55‡		>55‡		
	V_I = −12 dB to −6 dB	55		55		>55‡		
	V_I = −18 dB to −12 dB	53		55		55		
	V_I = −24 dB to −18 dB	47		53		55		
	V_I = −30 dB to −24 dB	41		47		53		
	V_I = −36 dB to −30 dB	35		41		47		
	V_I = −42 dB to −36 dB	29		35		41		
	V_I = −48 dB to −42 dB	23		29		35		
	V_I = −54 dB to −48 dB	17		23		29		

† A_V is the programmable gain of the input amplifier.
‡ A value >60 is over range and signal clipping occurs.
NOTE 7: The test condition V_I is a 1-kHz input signal with an 8-kHz conversion rate (0 dB relative to V_{ref}). The load impedance for the DAC is 600 Ω (300 Ω for TLC32044M).

D/A channel signal-to-distortion ratio (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
D/A channel signal-to-distortion ratio, TLC32044C, TLC32044E, TLC32044I, TLC32044M	V_I = −6 dB to 0 dB	58		dB
	V_I = −12 dB to −6 dB	58		
	V_I = −18 dB to −12 dB	56		
	V_I = −24 dB to −18 dB	50		
	V_I = −30 dB to −24 dB	44		
	V_I = −36 dB to −30 dB	38		
	V_I = −42 dB to −36 dB	32		
	V_I = −48 dB to −42 dB	26		
	V_I = −54 dB to −48 dB	20		
D/A channel signal-to-distortion ratio, TLC32045C, TLC32045I	V_I = −6 dB to 0 dB	55		
	V_I = −12 dB to −6 dB	55		
	V_I = −18 dB to −12 dB	53		
	V_I = −24 dB to −18 dB	47		
	V_I = −30 dB to −24 dB	41		
	V_I = −36 dB to −30 dB	35		
	V_I = −42 dB to −36 dB	29		
	V_I = −48 dB to −42 dB	23		
	V_I = −54 dB to −48 dB	17		

NOTE 7: The test condition V_I is a 1-kHz input signal with an 8-kHz conversion rate (0 dB relative to V_{ref}). The load impedance for the DAC is 600 Ω (300 Ω for TLC32044M).

gain and dynamic range

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Absolute transmit gain tracking error while transmitting into 600 Ω	−48-dB to 0-dB signal range, See Note 8		±0.05	±0.15	dB
Absolute transmit gain tracking error while transmitting into 300 Ω, TLC32044M	−48-dB to 0-dB signal range, T_A = 25°C, See Note 8		±0.05	±0.25	dB
Absolute transmit gain tracking error while transmitting into 300 Ω, TLC32044M	−48-dB to 0-dB signal range, T_A = −55°C to 125°C, See Note 8			±0.4	dB
Absolute receive gain tracking error	−48-dB to 0-dB signal range, See Note 8		±0.05	±0.15	dB
Absolute receive gain tracking error, TLC32044M	−48-dB to 0-dB signal range, T_A = 25°C, See Note 8		±0.05	±0.25	dB
Absolute receive gain tracking error, TLC32044M	−48-dB to 0-dB signal range, T_A = −55°C to 125°C, See Note 8			±0.4	dB
Absolute gain of the A/D channel	Signal input is a −0.5-dB, 1-kHz sinewave		0.2		dB
Absolute gain of the D/A channel	Signal input is a 0-dB, 1-kHz sinewave		−0.3		

† All typical values are at T_A = 25°C.

NOTE 8: Gain tracking is relative to the absolute gain at 1 kHz and 0 dB (0 dB relative to V_{ref}).

power supply rejection and crosstalk attenuation

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC+} or V_{CC-} supply voltage rejection ratio, receive channel	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at DR (ADC output)		30		dB
	f = 30 kHz to 50 kHz			45		
V_{CC+} or V_{CC-} supply voltage rejection ratio, transmit channel (single ended)	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at OUT+		30		
	f = 30 kHz to 50 kHz			45		
Crosstalk attenuation, transmit-to-receive (single ended)	TLC3204xC, E, I			80		
	TLC32044M		65	80		
Crosstalk attenuation, receive-to-transmit, TLC32044M		Inputs grounded, Gain = 1, 2, 4	65			

† All typical values are at T_A = 25°C.

delay distortion

bandpass filter transfer function, SCF f_{clock} = 288 kHz IN+ – IN– is a ±3 V sinewave† (see Note 9)

PARAMETER	TEST CONDITIONS	FREQUENCY RANGE	ADJUSTMENT ADDEND‡	MIN	TYP§	MAX	UNIT
Filter gain, TLC32044C, TLC32044E, TLC32044I	Input signal reference to 0 dB	f ≤ 50 Hz	K1 × 0 dB	–33	–29	–25	dB
		f = 100 Hz	K1 × –0.26 dB	–4	–2	–1	
		f = 150 Hz to 3100 Hz	K1 × 0 dB	–0.25	0	0.25	
		f = 3100 Hz to 3300 Hz	K1 × 0 dB	–0.3	0	0.3	
		f = 3300 Hz to 3650 Hz	K1 × 0 dB	–0.5	0	0.5	
		f = 3800 Hz	K1 × 2.3 dB		–3	–1	
		f = 4000 Hz	K1 × 2.7 dB		–17	–16	
		f ≥ 4400 Hz	K1 × 3.2 dB			–40	
		f ≥ 5000 Hz	K1 × 0 dB			–65	
Filter gain, TLC32044M	Input signal reference to 0 dB	f ≤ 50 Hz	K1 × 0 dB	–33	–29	–25	
		f = 100 Hz	K1 × –0.26 dB	–4	–2	–1	
		f = 150 Hz to 3100 Hz	K1 × 0 dB	–0.25	0	0.25	
		f = 3100 Hz to 3300 Hz	K1 × 0 dB	–0.3	0	0.3	
		f = 3300 Hz to 3500 Hz	K1 × 0 dB	–0.5	0	0.5	
		f = 3800 Hz	K1 × 2.3 dB		–3	–0.5	
		f = 4000 Hz	K1 × 2.7 dB		–17	–16	
		f ≥ 4400 Hz	K1 × 3.2 dB			–40	
		f ≥ 5000 Hz	K1 × 0 dB			–65	
Filter gain, TLC32045C, TLC32045I	Input signal reference to 0 dB	f ≤ 50 Hz	K1 × 0 dB	–33	–29	–25	
		f = 100 Hz	K1 × –0.26 dB	–4	–2	–1	
		f = 150 Hz to 3100 Hz	K1 × 0 dB	–0.25	0	0.25	
		f = 3100 Hz to 3300 Hz	K1 × 0 dB	–0.3	0	0.3	
		f = 3300 Hz to 3650 Hz	K1 × 0 dB	–0.5	0	0.5	
		f = 3800 Hz	K1 × 2.3 dB		–3	–1	
		f = 4000 Hz	K1 × 2.7 dB		–17	–16	
		f ≥ 4400 Hz	K1 × 3.2 dB			–40	
		f ≥ 5000 Hz	K1 × 0 dB			–65	

† See filter curves in typical characteristics

‡ The MIN, TYP, and MAX specifications are given for a 288-kHz SCF clock frequency. A slight error in the 288-kHz SCF may result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where K1 = 100 •[(SCF frequency – 288 kHz) / 288 kHz]. For errors greater than 0.25%, see Note 8.

§ All typical values are at T_A = 25°C.

NOTE 9: The filter gain outside of the passband is measured with respect to the gain at 1 kHz. The filter gain within the passband is measured with respect to the average gain within the passband. The passbands are 150 to 3600 Hz and 0 to 3600 Hz for the bandpass and low-pass filters respectively. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

low-pass filter transfer function†, SCF f_{clock} = 288 kHz (see Note 9)

PARAMETER	TEST CONDITIONS	FREQUENCY RANGE	ADJUSTMENT ADDEND‡	MIN	TYP§	MAX	UNIT
Filter gain, TLC32044C, TLC32044E, TLC32044I	Input signal reference is 0 dB	f = 0 Hz to 3100 Hz	K1 × 0 dB	−0.25	0	0.25	dB
		f = 3100 Hz to 3300 Hz	K1 × 0 dB	−0.3	0	0.3	
		f = 3300 Hz to 3650 Hz	K1 × 0 dB	−0.5	0	0.5	
		f = 3800 Hz	K1 × 2.3 dB		−3	−1	
		f = 4000 Hz	K1 × 2.7 dB		−17	−16	
		f ≥ 4400 Hz	K1 × 3.2 dB			−40	
		f ≥ 5000 Hz	K1 × 0 dB			−65	
Filter gain, TLC32044M	Input signal reference is 0 dB	f = 0 Hz to 3100 Hz	K1 × 0 dB	−0.25	0	0.25	
		f = 3100 Hz to 3300 Hz	K1 × 0 dB	−0.3	0	0.3	
		f = 3300 Hz to 3500 Hz	K1 × 0 dB	−0.5	0	0.5	
		f = 3800 Hz	K1 × 2.3 dB		−3	−0.5	
		f = 4000 Hz	K1 × 2.7 dB		−17	−16	
		f ≥ 4400 Hz	K1 × 3.2 dB			−40	
		f ≥ 5000 Hz	K1 × 0 dB			−65	
Filter gain, TLC32045C, TLC32045I	Input signal reference is 0 dB	f = 0 Hz to 3100 Hz	K1 × 0 dB	−0.25	0	0.25	
		f = 3100 Hz to 3300 Hz	K1 × 0 dB	−0.3	0	0.3	
		f = 3300 Hz to 3650 Hz	K1 × 0 dB	−0.5	0	0.5	
		f = 3800 Hz	K1 × 2.3 dB		−3	−1	
		f = 4000 Hz	K1 × 2.7 dB		−17	−16	
		f ≥ 4400 Hz	K1 × 3.2 dB			−40	
		f ≥ 5000 Hz	K1 × 0 dB			−65	

† See filter curves in typical characteristics
‡ The MIN, TYP, and MAX specifications are given for a 288-kHz SCF clock frequency. A slight error in the 288-kHz SCF may result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where K1 = 100 ·[(SCF frequency – 288 kHz) / 288 kHz]. For errors greater than 0.25%, see Note 8.
§ All typical values are at T_A = 25°C.

NOTE 9: The filter gain outside of the passband is measured with respect to the gain at 1 kHz. The filter gain within the passband is measured with respect to the average gain within the passband. The passbands are 150 to 3600 Hz and 0 to 3600 Hz for the bandpass and low-pass filters respectively. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

serial port

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −300 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
I_I	Input current				±10	μA
C_i	Input capacitance			15		pF
C_o	Output capacitance			15		pF

† All typical values are at T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V

noise (measurement includes low-pass and bandpass switched-capacitor filters)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit noise	TLC32044C, E, I	With sin x/x correction	DX input = 00000000000000, constant input code			550	μV rms
	TLC32044M					575	μV rms
	TLC32045C, I					600	μV rms
	TLC32044C, E, I	Without sin x/x correction			325	425	μV rms
	TLC32044M				325	450	μV rms
	TLC32045C, I					450	μV rms
	TLC32044C, E, I				18		dBrncO
	TLC32045C, I				24		dBrncO
Receive noise (see Note 10)	TLC32044C, E, I, M		Inputs grounded, gain = 1		300	500	μV rms
	TLC32045C, I					530	μV rms
	TLC32044C, E, I, M				18		dBrncO
	TLC32045C, I				24		dBrncO

† All typical values are at T_A = 25°C.
NOTE 10: The noise is computed by statistically evaluating the digital output of the A/D converter.

timing requirements

serial port recommended input signals

		MIN	MAX	UNIT
$t_{c(MCLK)}$	Master clock cycle time	95		ns
	Master clock cycle time, TLC32044M	100	192	ns
$t_{r(MCLK)}$	Master clock rise time		10	ns
$t_{f(MCLK)}$	Master clock fall time		10	ns
	Master clock duty cycle	25%	75%	
	Master clock duty cycle, TLC32044M	42%	58%	
	$\overline{\text{RESET}}$ pulse duration (see Note 11)	800		ns
$t_{su(DX)}$	DX setup time before SCLK↓	20		ns
	DX setup time before SCLK↓, TLC32044M	28		ns
$t_{h(DX)}$	DX hold time after SCLK↓	$t_{c(SCLK)}/4$		ns

NOTE 11: $\overline{\text{RESET}}$ pulse duration is the amount of time that the reset pin is held below 0.8 V after the power supplies have reached their recommended values.

serial port — AIC output signals

		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time		380			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time				50	ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time				50	ns
	Shift clock (SCLK) duty cycle		45		55	%
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{FSR}/\overline{FSX}$↓	$C_L = 50$ pF			52	ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{FSR}/\overline{FSX}$↑	$C_L = 50$ pF			52	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑				90	ns
$t_{d(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↓ in word mode				90	ns
$t_{d(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↑ in word mode				90	ns
$t_{f(EODX)}$	$\overline{EODX}$ fall time				15	ns
$t_{f(EODR)}$	$\overline{EODR}$ fall time				15	ns
$t_{d(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↓ in byte mode				100	ns
$t_{d(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↑ in byte mode				100	ns
$t_{d(MH-SL)}$	Delay from MSTR CLK↑ to SCLK↓			65		ns
$t_{d(MH-SH)}$	Delay from MSTR CLK↑ to SCLK↑			65		ns

serial port — AIC output signals, TLC32044M

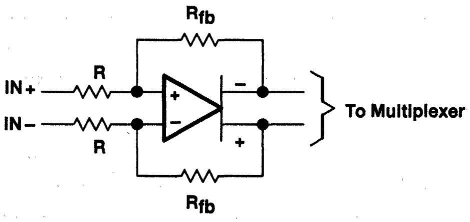
		MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time	400			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time		50		ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time		50		ns
	Shift clock (SCLK) duty cycle		50		%
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{FSR}/\overline{FSX}$↓			260	ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{FSR}/\overline{FSX}$↑			260	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑			316	ns
$t_{d(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↓ in word mode			280	ns
$t_{d(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↑ in word mode			280	ns
$t_{f(EODX)}$	$\overline{EODX}$ fall time		15		ns
$t_{f(EODR)}$	$\overline{EODR}$ fall time		15		ns
$t_{d(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↓ in byte mode		100		ns
$t_{d(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↑ in byte mode		100		ns
$t_{d(MH-SL)}$	Delay from MSTR CLK↑ to SCLK↓		65		ns
$t_{d(MH-SH)}$	Delay from MSTR CLK↑ to SCLK↑		65		ns

† Typical values are at $T_A = 25°C$.

Table 3. Gain Control Table (Analog Input Signal Required for Full-Scale A/D Conversion)

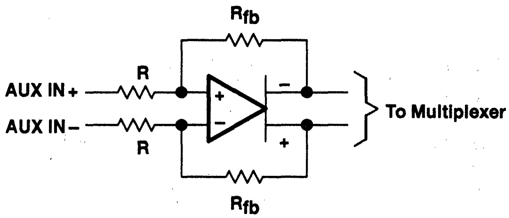
INPUT CONFIGURATIONS	CONTROL REGISTER BITS d6	CONTROL REGISTER BITS d7	ANALOG INPUT‡	A/D CONVERSION RESULT
Differential configuration Analog input = IN+ – IN– = AUX IN+ – AUX IN–	1	1	±6 V	Full-scale
	0	0		
	1	0	±3 V	Full-scale
	0	1	±1.5 V	Full-scale
Single-ended configuration Analog input = IN+ – ANLG GND = AUX IN+ – ANLG GND	1	1	±3 V	Half-scale
	0	0		
	1	0	±3 V	Full-sale
	0	1	±1.5 V	Full-scale

‡ In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0, d7 = 1

Figure 7. IN+ and IN– Gain Control Circuitry



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0, d7 = 1

Figure 8. AUX IN+ and AUX IN– Gain Control Circuitry

(sin x)/x correction

The AIC does not have (sin x)/x correction circuitry after the digital-to-analog converter. (Sin x)/x correction can be accomplished easily and efficiently in digital signal processor (DSP) software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results, which are shown in Table 4, are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires only seven instruction cycles per sample on the TMS(SMJ)320 DSPs. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction adds a slight amount of group delay at the upper edge of the 300–3000-Hz band.

(sin x)/x roll-off for a zero-order hold function

The (sin x)/x roll-off for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in the table below.

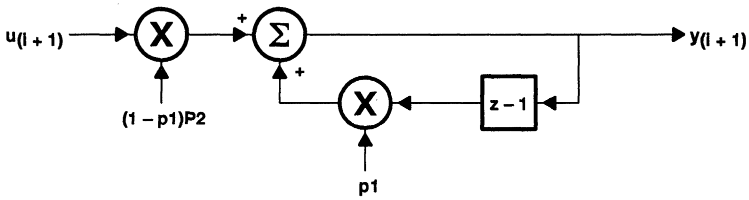
Table 4. (sin x)/x Roll-Off

f_s (Hz)	$20 \log \frac{\sin \pi f/f_s}{\pi f/f_s}$ (f = 3000 Hz) (dB)
7200	−2.64
8000	−2.11
9600	−1.44
14400	−0.63
19200	−0.35

The actual AIC (sin x)/x roll-off will be slightly less than the above figures because the AIC has less than a 100% duty cycle hold interval.

correction filter

To compensate for the (sin x)/x roll-off of the AIC, a first-order correction filter (shown below) is recommended.



The difference equation for this correction filter is:

$$y_{i+1} = p2(1 - p1)(u_{i+1}) + p1\, y_i$$

where the constant p1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$|H(f)|^2 = \frac{p2^2 (1-p1)^2}{1 - 2p1 \cos(2 \pi f/f_s) + p1^2}$$

correction results

Table 5 shows the optimum p values and the corresponding correction results for 8000-Hz and 9600-Hz sampling rates.

Table 5. Optimum P Values

f (Hz)	ERROR (dB) f_s = 8000 Hz p1 = −0.14813 p2 = 0.9888	ERROR (dB) f_s = 9600 Hz p1 = −0.1307 p2 = 0.9951
300	−0.099	−0.043
600	−0.089	−0.043
900	−0.054	0
1200	−0.002	0
1500	0.041	0
1800	0.079	0.043
2100	0.100	0.043
2400	0.091	0.043
2700	−0.043	0
3000	−0.102	−0.043

TMS(SMJ)320 software requirements

The digital correction filter equation can be written in state variable form as follows:

$$Y = k1 \times Y + k2 \times U$$

Where

$k1 = p1$

$k2 = (1 - p1) \times p2$

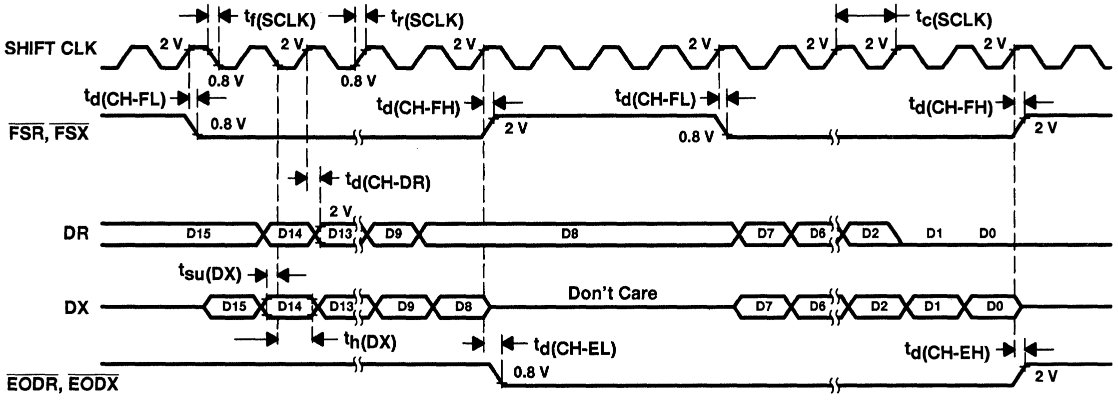
Y = filter state

U = next I/O sample

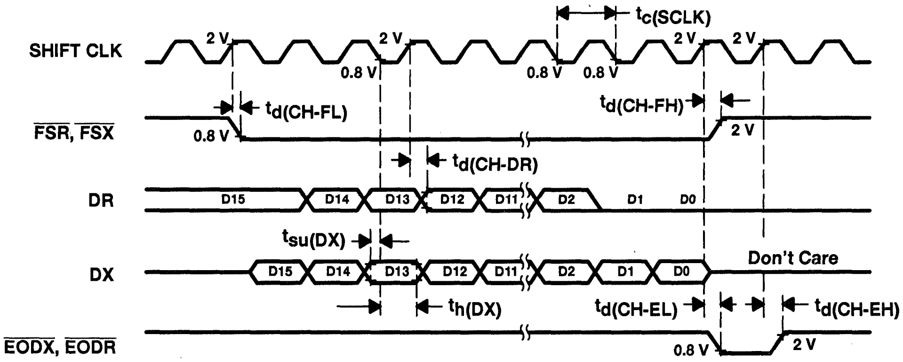
The coefficients k1 and k2 must be represented as 16-bit integers. The SACH instruction (with the proper shift) yields the correct result. With the assumption that the TMS(SMJ)320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

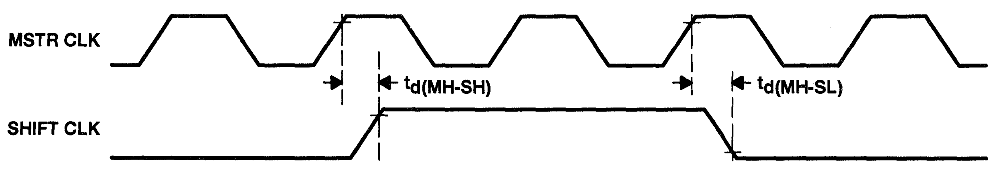
PARAMETER MEASUREMENT INFORMATION



(a) BYTE-MODE TIMING



(b) WORD-MODE TIMING



(c) SHIFT-CLOCK TIMING

Figure 9. Serial-Port Timing

PARAMETER MEASUREMENT INFORMATION

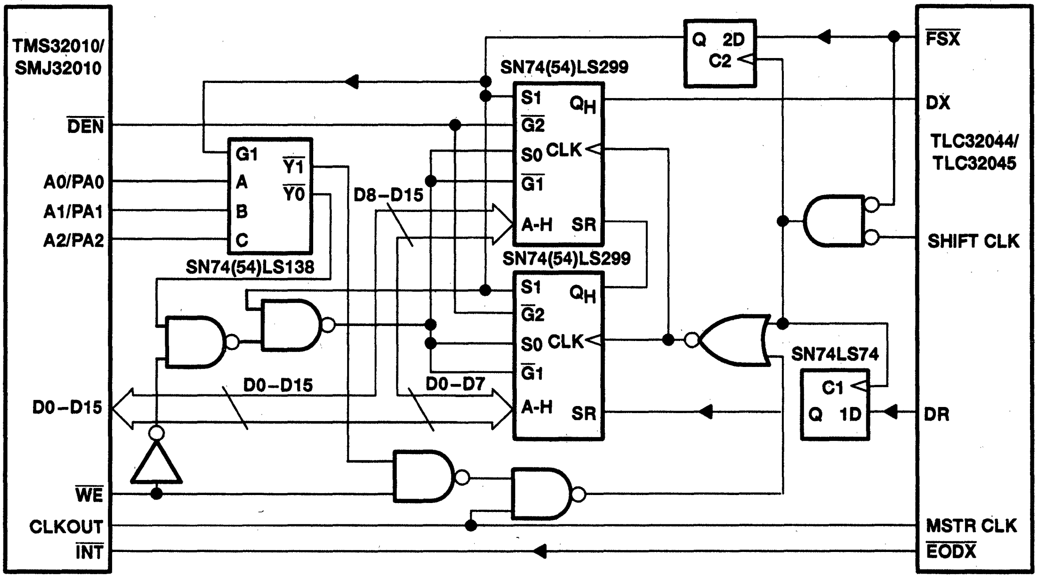


Figure 10. TMS(SMJ)32010/TMS(SMJ)320C15/(SMJ320E15)-TLC32044/45 Interface Circuit

PARAMETER MEASUREMENT INFORMATION

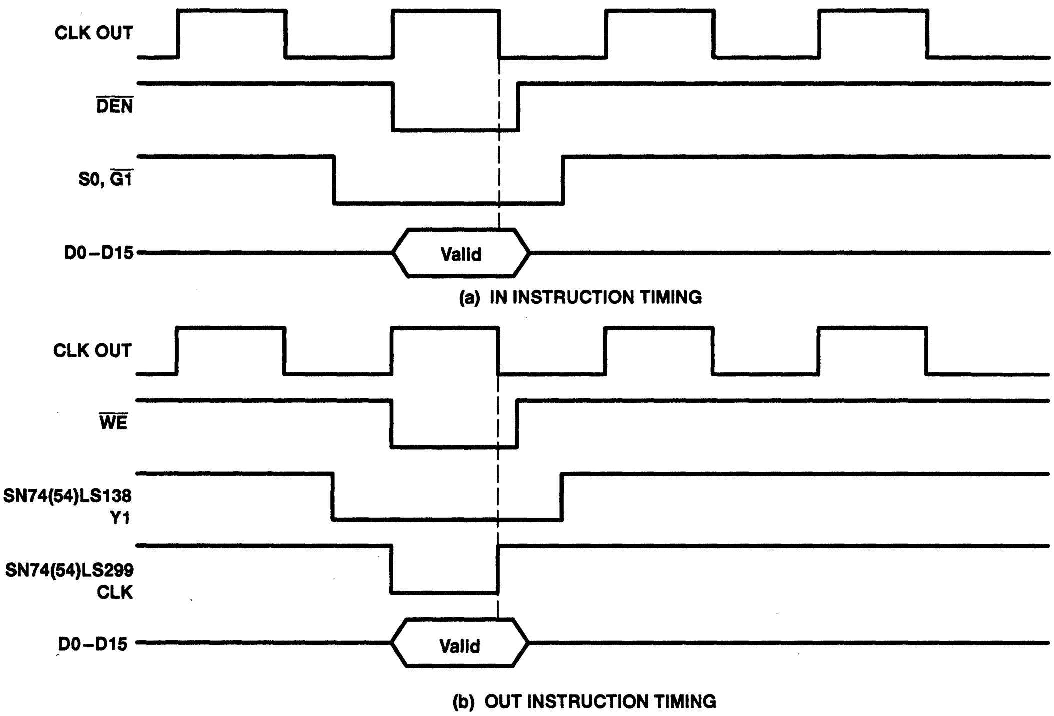


Figure 11. TMS(SMJ)32010/TMS(SMJ)320C15-TLC32044/TLC32045 Interface Timing

TYPICAL CHARACTERISTICS

AIC TRANSMIT AND RECEIVE LOW-PASS FILTER

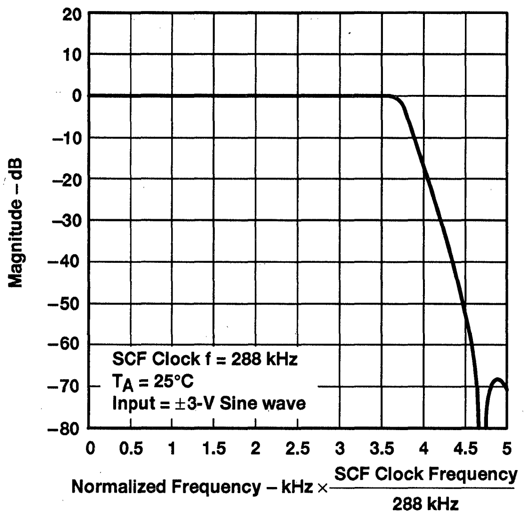


Figure 12

AIC TRANSMIT AND RECEIVE LOW-PASS FILTER

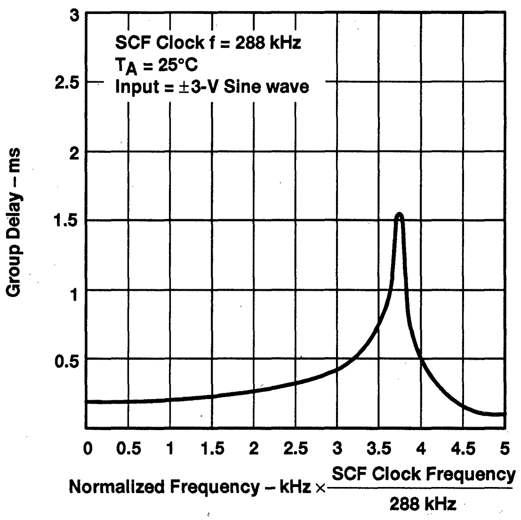


Figure 13

AIC RECEIVE-CHANNEL BANDPASS FILTER

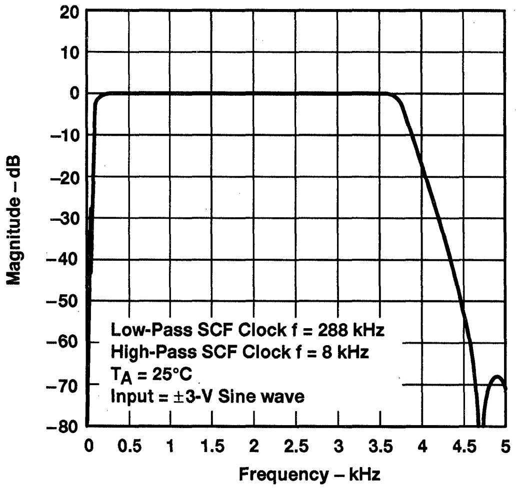


Figure 14

AIC RECEIVE-CHANNEL HIGH-PASS FILTER

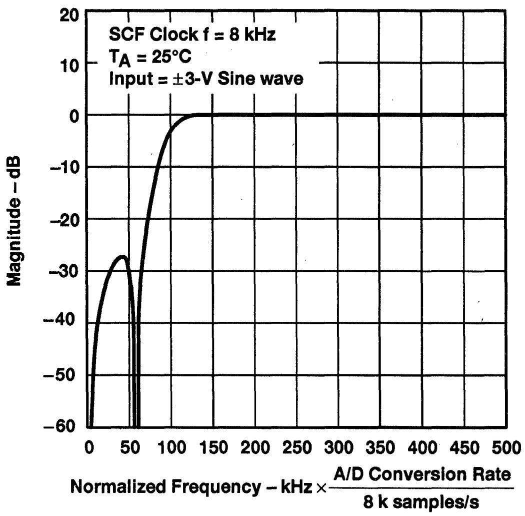


Figure 15

TYPICAL CHARACTERISTICS

AIC RECEIVE CHANNEL BANDPASS FILTER

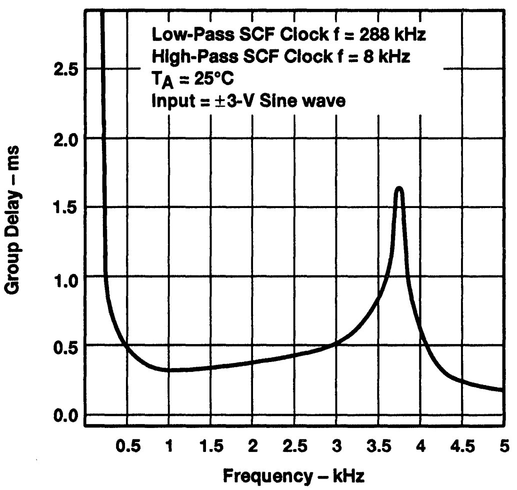


Figure 16

AIC (sin x)/x CORRECTION FILTER

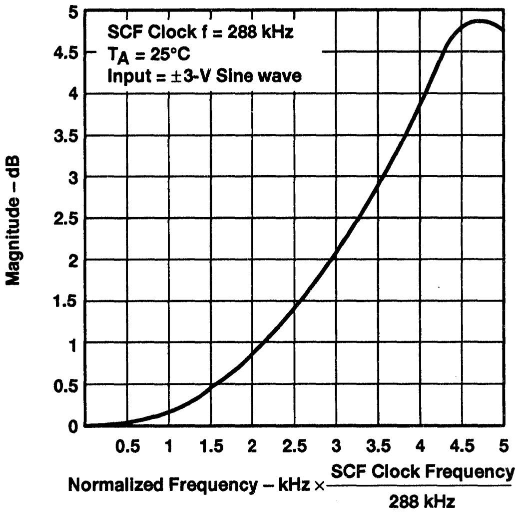


Figure 17

AIC (sin x)/x CORRECTION FILTER

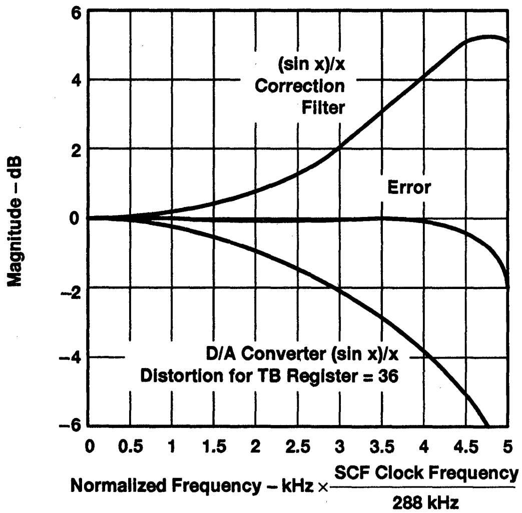


Figure 18

A/D SIGNAL-TO-DISTORTION RATIO vs INPUT-SIGNAL LEVEL

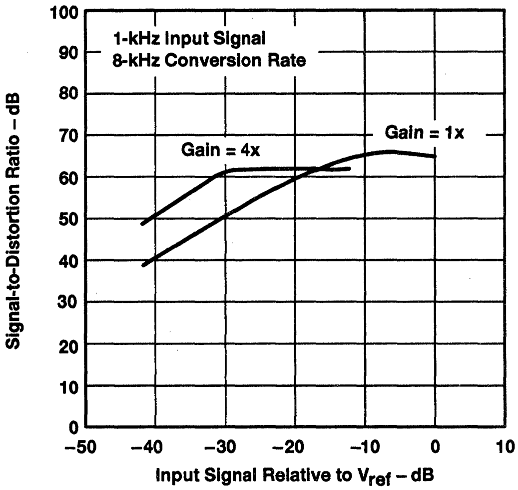


Figure 19

TYPICAL CHARACTERISTICS

A/D GAIN TRACKING
(GAIN RELATIVE TO GAIN
AT 0-dB INPUT-SIGNAL LEVEL)

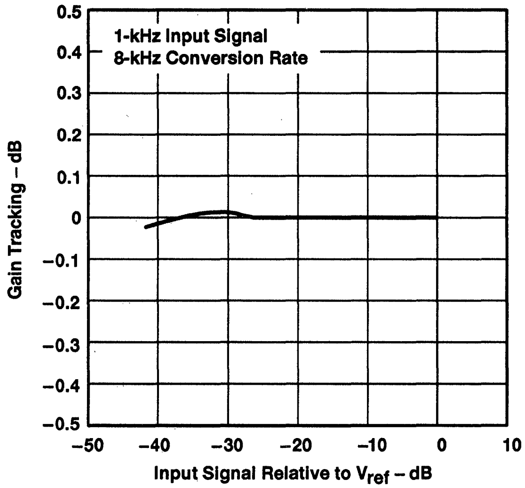


Figure 20

D/A CONVERTER SIGNAL-TO-DISTORTION RATIO
vs
INPUT-SIGNAL LEVEL

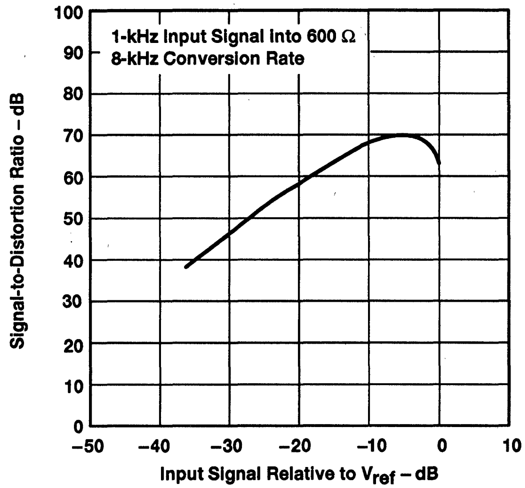


Figure 21

D/A GAIN TRACKING
(GAIN RELATIVE TO GAIN
AT 0-dB INPUT-SIGNAL LEVEL)

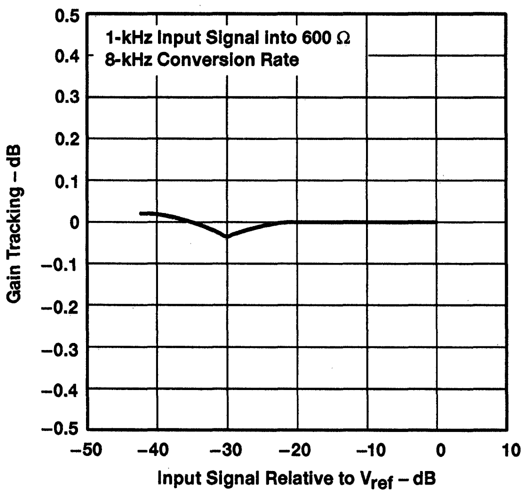


Figure 22

A/D SECOND HARMONIC DISTORTION
vs
INPUT-SIGNAL LEVEL

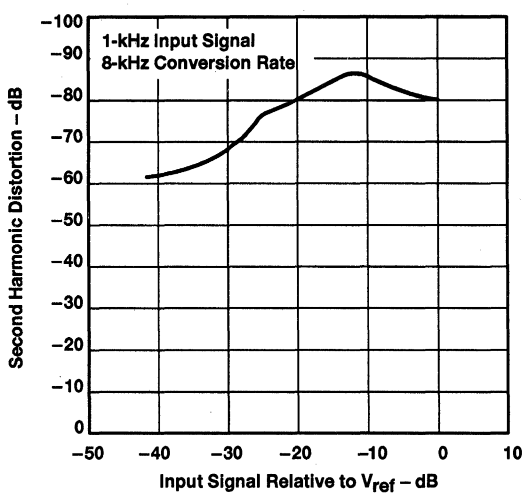


Figure 23

TYPICAL CHARACTERISTICS

D/A SECOND HARMONIC DISTORTION vs INPUT-SIGNAL LEVEL

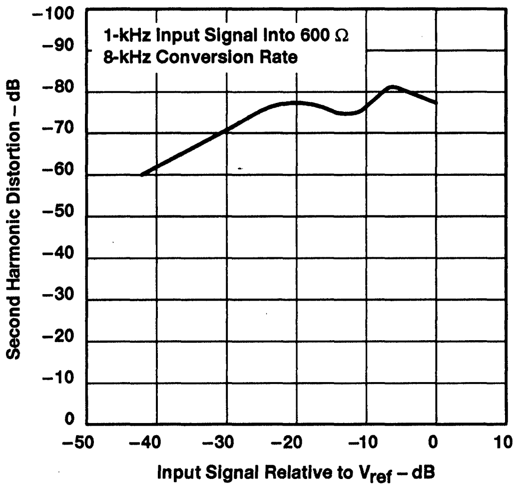


Figure 24

A/D THIRD HARMONIC DISTORTION vs INPUT-SIGNAL LEVEL

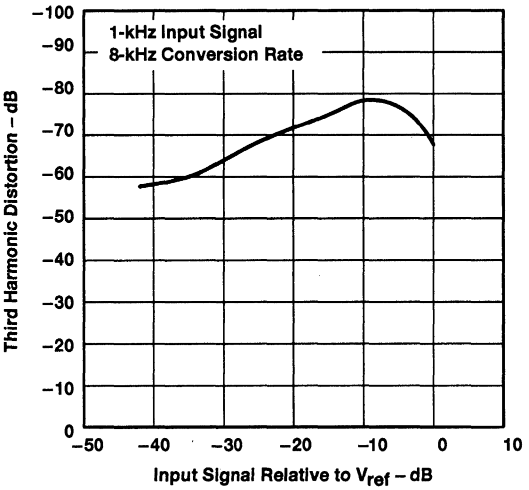


Figure 25

D/A THIRD HARMONIC DISTORTION vs INPUT-SIGNAL LEVEL

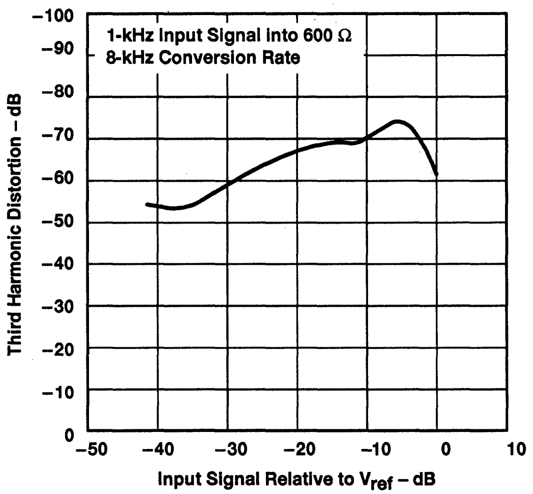


Figure 26

APPLICATION INFORMATION

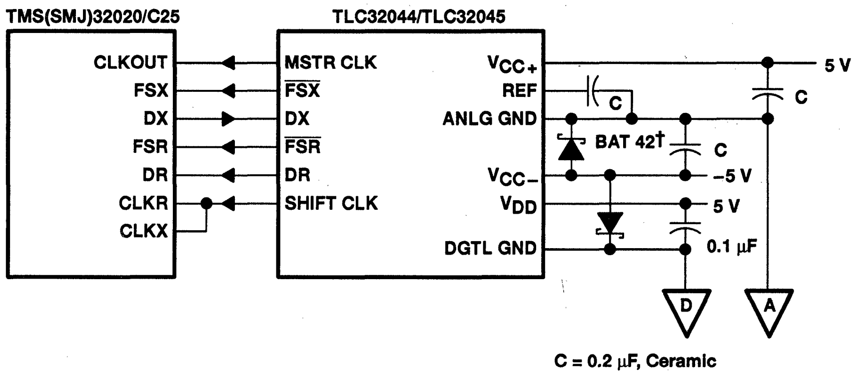


Figure 27. AIC Interface to the TMS(SMJ)32020/C25 Showing Decoupling Capacitors and Schottky Diode†

† Thomson Semiconductors

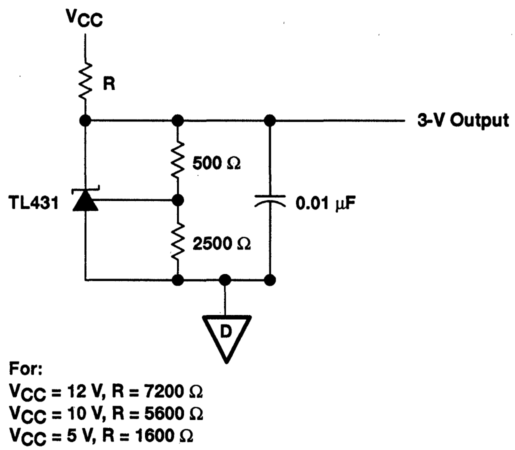


Figure 28. External Reference Circuit For TLC32044/TLC32045

- **CMOS Technology**
- **Single 5-V Power Supply Voltage or 5-V Analog and 3-V Digital Supply Voltages**
- **Power Dissipation:**
  - **Operating Mode . . . 150 mW Max**
  - **Power-Down Mode . . . 1 mW Max**
- **General Purpose 16-Bit Signal Processing**
- **2s-Complement Data Format**
- **Dynamic Range . . . 91-dB Typ**
- **Total Signal-to-(Noise + Distortion):**
  - **ADC . . . 88-dB Min**
  - **DAC . . . 88-dB Min**
- **Differential Architecture**
- **Internal Reference Voltage (V_{ref})**
- **Internal 64× Oversampling**
- **Serial Port Interface**
- **Phone-Mode Output Control**
- **System-Test Mode, Digital-Loopback Test**
- **Supports All V.34 Sample Rates**
- **Supports Business-Audio Applications**
- **Variable Conversion Rate Selected As MCLK/(Fk × 256), Fk = 1, 2, 3,..., 256**
- **Master Clock Input Can Connect Directly To CLOCKOUT On TMS320C5x**

description

The TLC320AD56C provides high resolution, low-speed signal conversion from digital-to-analog (D/A) and from analog-to-digital (A/D) using oversampling sigma-delta technology. This device consists of two serial-synchronous conversion paths (one for each data direction) and includes an interpolation filter before the DAC and a decimation filter after the ADC. Other overhead functions provide on-chip timing and control. The sigma-delta architecture produces high resolution analog-to-digital and digital-to-analog conversion at low system speeds and low cost.

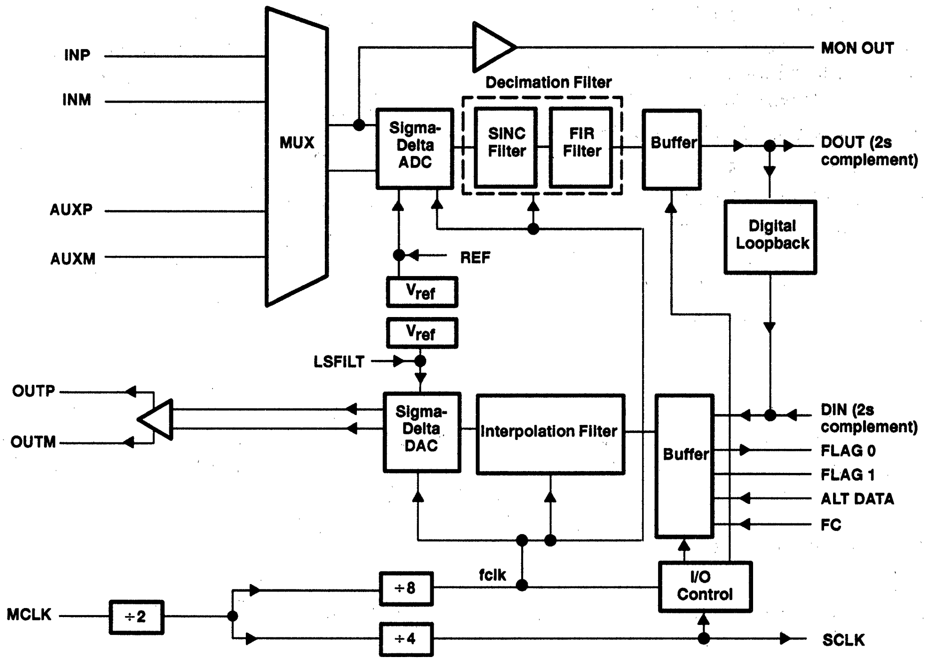
The options and the circuit configurations of this device can be programmed through the serial interface. The options include reset, power-down, communications protocol, serial clock rate, signal sampling rate, and test mode. The TLC320AD56C is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	PACKAGE	
	PLASTIC CHIP CARRIER (FN)	QUAD FLATPACK (PTB)
0°C to 70°C	TLC320AD56CFN	TLC320AD56CPTB

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

- Single 5-V Power Supply
- Stereo 16-Bit Sigma-Delta Audio Converter
- General Purpose 16-Bit Signal Processing
- Sample Rates from 4 kHz to 48 kHz
- High Current Capacity Output Drivers For Driving Line Outputs or 32 Ω Stereo Headphones
- On-Chip Support Real Time Data Compression/Decompression For A-Law, μ-Law, and Adaptive Differential Pulse Code Modulation-International Multimedia Association (ADPCM-IMA)
- Differential Architecture
- Register Compatible Functional Upgrade From AD1848, CS4248, and CS4231
- Stereo Microphone Preamplifier–Uniquely Mixable in Capture A/D Path
- Fully Independent Analog Input Capture and Playback Mixing Capability
- Mono Channel Input
- Mono Speaker Driver With 32 Ω Drive Capability
- Internal Reference Voltage (V_{ref})
- Supports Little and Big Endian Formats
- Byte Wide Parallel Port Interface For ISA, EISA Bus Support
- Full Duplex Transfers With Host PC Using On-Chip Dual DMA Count Registers
- 8-Bit DMA Data Transfers With Host Utilizing On-Chip Dual 64 Byte FIFOs With Independent Capture and Playback Programmable Interrupt Flag Depth

description

The TLC320AD65C sigma-delta technology audio stereo codec provides 16-bit audio for computer multimedia applications.

The TLC320AD65C provides upgraded functionality, flexibility, and performance from the 16-bit AD1848, CS4248, and the CS4231. Flexible analog mixing for both record and playback paths, provide capability for either the normal ADC with DAC playback paths or an all analog input to output mixing path without any digital conversions. This device consists of four synchronous conversion paths. Four stereo inputs and one mono input are provided. The stereo line outputs are capable of driving 32-Ω stereo headphones. The mono channel output driver is capable of driving a 32-Ω speaker. Gain and mixing control and sample rate selections are provided for maximum flexibility. Additional functions provide digital filtering and on-chip timing and control. The TLC320AD65C is characterized for operation from 0°C to 70°C.

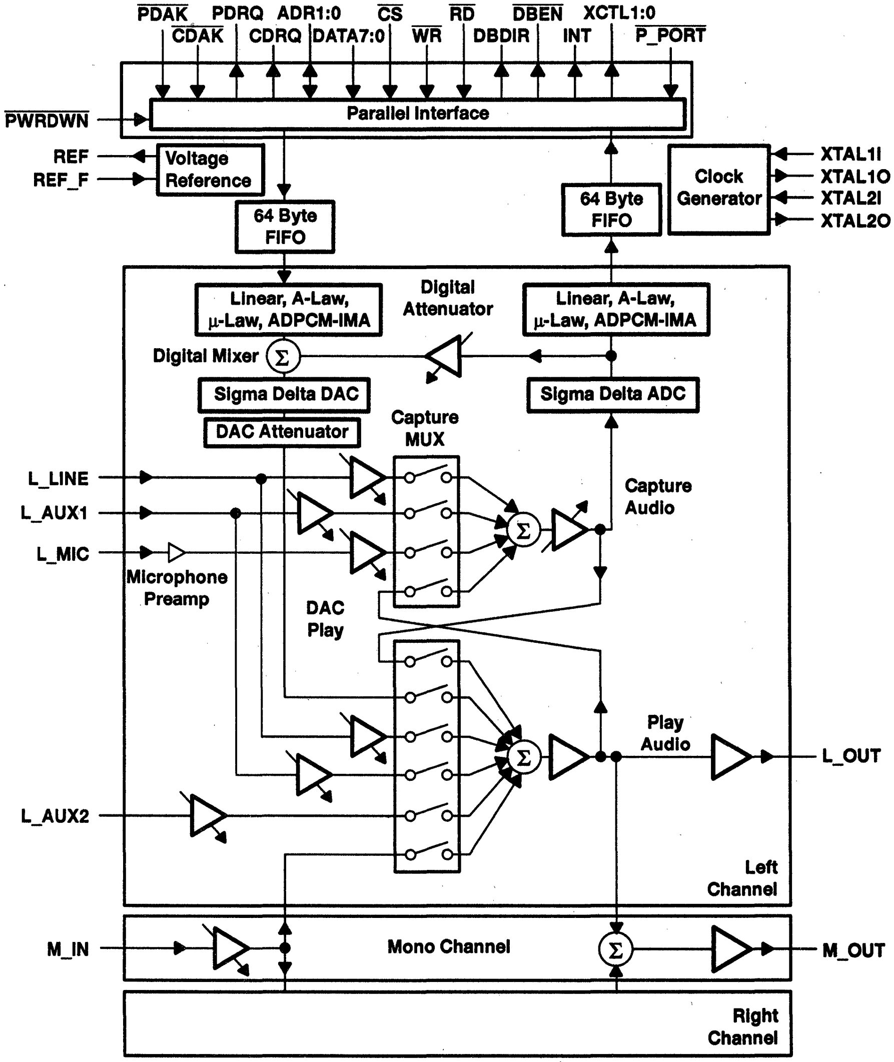
AVAILABLE OPTIONS

T_A	PACKAGE	
	PLASTIC CHIP CARRIER (FN)	QUAD FLATPACK (PZ)
0°C to 70°C	TLC320AD65CFN	TLC320AD65CPZ

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

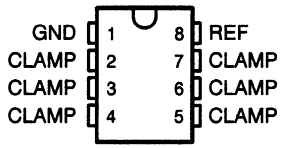
functional block diagram



SLAS078 – D4102, SEPTEMBER 1993

- **Protects Against Latch-Up**
- **25-mA Current Sink in Active State**
- **Less Than 1-mW Dissipation in Standby Condition**
- **Ideal for Applications in Environments Where Large Transient Spikes Occur**
- **Stable Operation for All Values of Capacitive Load**
- **No Output Overshoot**

D OR P PACKAGE
(TOP VIEW)



description

The TL7726C, TL7726I, and TL7726Q each consist of six identical clamping circuits that monitor an input voltage with respect to a reference value, REF. For an input voltage (V_I) in the range of GND to < REF, the clamping circuits present a very high impedance to ground, drawing current of less than 10 μA. The clamping circuits are active for V_I < GND or V_I > REF when they have a very low impedance and can sink up to 25 mA.

These characteristics make the TL7726C, TL7726I, and TL7726Q ideal as protection devices for CMOS semiconductor devices in environments where there are large positive or negative transients to protect analog-to-digital converters in automotive or industrial systems. The use of clamping circuits provides a safeguard against potential latch-up.

The TL7726C is characterized for operation over the temperature range of 0°C to 70°C. The TL7726I is characterized for operation over the temperature range of −25°C to 85°C. The TL7726Q is characterized for operation over the temperature range of −40°C to 125°C.

AVAILABLE OPTIONS

OPERATING TEMPERATURE RANGE	DEVICE	PACKAGE
0°C – 70°C	TL7726CD	8-pin SO
0°C – 70°C	TL7726CP	8-pin DIP
−25°C – 85°C	TL7726ID	8-pin SO
−25°C – 85°C	TL7726IP	8-pin DIP
−40°C – 125°C	TL7726QD	8-pin SO
−40°C – 125°C	TL7726QP	8-pin DIP

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Reference voltage, V_{ref} . . . . 6 V
Clamping current, I_{IK} . . . . ±50 mA
Junction temperature, T_J . . . . 150°C
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: TL7726C . . . . 0°C to 70°C
TL7726I . . . . −40°C to 85°C
TL7726Q . . . . −40°C to 125°C
Storage temperature range . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A \le 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	728 mW	5.8 mW/°C	460 mW	374 mW	144 mW
P	924 mW	9.5 mW/°C	757 mW	615 mW	237 mW

recommended operating conditions

		MIN	MAX	UNIT
Reference voltage, V_{ref}		4.5	5.5	V
Input clamping current, I_{IK}	$V_I \ge V_{ref}$		25	mA
	$V_I \le GND$	−25		mA

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

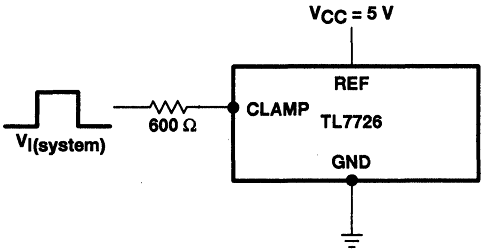
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK+}	Positive clamp voltage	$I_I = 20$ mA	V_{ref}		$V_{ref}+200$	mV
V_{IK-}	Negative clamp voltage	$I_I = 20$ mA	−200		0	mV
I_Z	Reference current	$V_{ref} = 5$ V		25	60	µA
I_I	Input current	$V_{ref} - 50\text{ mV} \le V_I \le V_{ref}$			10	µA
		$GND \le V_I \le 50$ mV	−10			µA
		$50\text{ mV} \le V_I \le V_{ref} - 50$ mV	−1		1	µA

† All typical values are at $T_A = 25°C$.

switching characteristics specified at $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_s	Settling time	$V_{I(system)} = \pm13$ V, $R_I = 600\ \Omega$, $t_t < 1$ µs, Measured at 10% to 90%, See Figure 1		30	µs

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

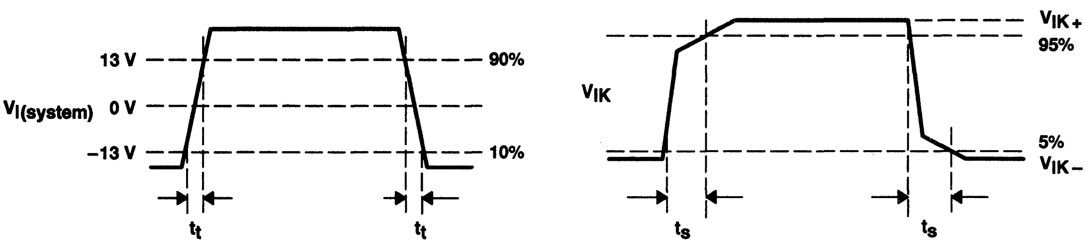


Figure 1. Switching Characteristics

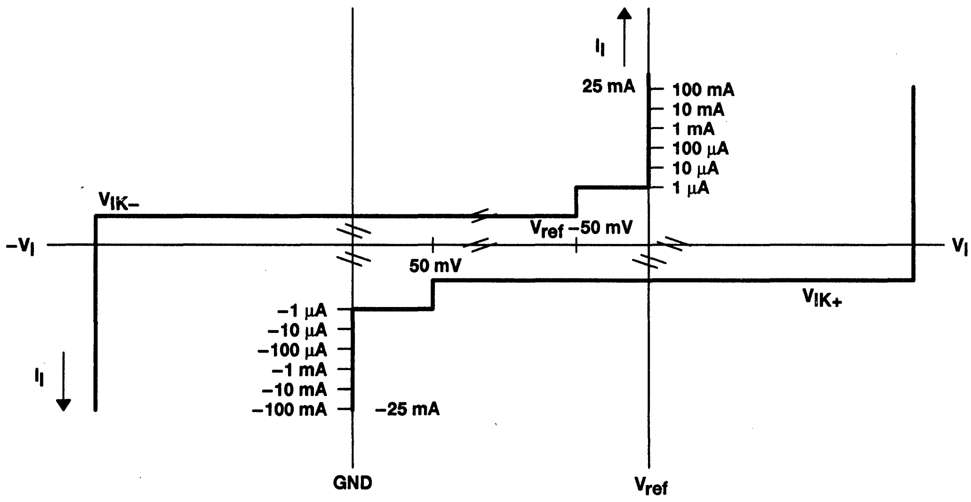
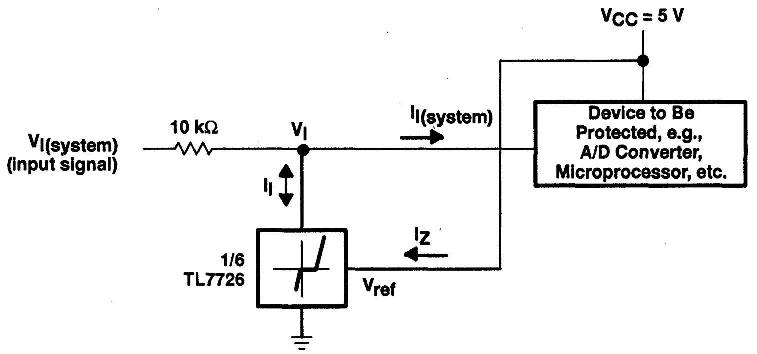


Figure 2. Tolerance Band for Clamping Circuit

APPLICATION INFORMATION



Example: If $I_I >> I_{I(system)}$, i.e., $V_{I(system)} > V_{ref} + 200$ mV

where:

$I_{I(system)}$ = Input current to the device being protected

$V_{I(system)}$ = Input voltage to the device being protected

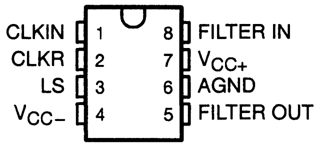
then the maximum input voltage

$$V_{I(system)}max = V_{ref} + I_I max(10k\Omega)$$
$$= 5\ V + 25\ mA(10k\Omega)$$
$$= 5\ V + 250\ V$$
$$= 255\ V$$

Figure 3. Typical Application

- **Low Clock-to-Cutoff-Frequency Ratio Error**
  TLC04/MF4A-50 . . . ±0.8%
  TLC14/MF4A-100 . . . ±1%
- **Filter Cutoff Frequency Dependent Only on External-Clock Frequency Stability**
- **Minimum Filter Response Deviation Due to External Component Variations Over Time and Temperature**
- **Cutoff Frequency Range From 0.1 Hz to 30 kHz, $V_{CC\pm} = \pm 2.5$ V**
- **5-V to 12-V Operation**
- **Self Clocking or TTL-Compatible and CMOS-Compatible Clock Inputs**
- **Low Supply-Voltage Sensitivity**
- **Designed to be Interchangeable With National MF4-50 and MF4-100**

D OR P PACKAGE
(TOP VIEW)



description

The TLC04/MF4A-50 and TLC14/MF4A-100 are monolithic Butterworth low-pass switched-capacitor filters. Each is designed as a low-cost, easy-to-use device providing accurate fourth-order low-pass filter functions in circuit design configurations.

Each filter features cutoff frequency stability that is dependent only on the external-clock frequency stability. The cutoff frequency is clock tunable and has a clock-to-cutoff frequency ratio of 50:1 with less than ±0. 8% error for the TLC04/MF4A-50 and a clock-to-cutoff frequency ratio of 100:1 with less than ±1% error for the TLC14/MF4A-100. The input clock features self-clocking or TTL- or CMOS-compatible options in conjunction with the level shift (LS) terminal.

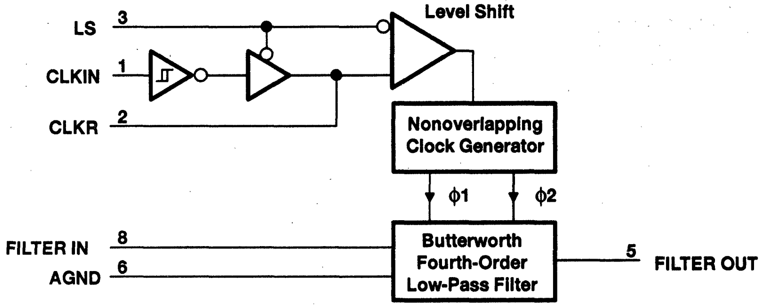
The TLC04C/MF4A-50C and TLC14C/MF4A-100C are characterized for operation from 0°C to 70°C. The TLC04I/MF4A-50I and TLC14I/MF4A-100I are characterized for operation from −40°C to 85°C. The TLC04M/MF4A-50M and TLC14M/MF4A-100M are characterized over the full military temperature range of −55°C to 125°C.

AVAILABLE OPTIONS

T_A	CLOCK-TO-CUTOFF FREQUENCY RATIO	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	50:1 100:1	TLC04CD/MF4A-50CD TLC14CD/MF4A-100CD	TLC04CP/MF4A-50CP TLC14CP/MF4A-100CP
−40°C to 85°C	50:1 100:1	TLC04ID/MF4A-50ID TLC14ID/MF4A-100ID	TLC04IP/MF4A-50IP TLC14IP/MF4A-100IP
−55°C to 125°C	50:1 100:1		TLC04MP/MF4A-50MP TLC14MP/MF4A-100MP

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC04CDR/MF4A-50CDR).

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AGND	6	I	Analog ground. The noninverting input to the operational amplifiers of the Butterworth fourth-order low-pass filter.
CLKIN	1	I	Clock in. CLKIN is the clock input terminal for CMOS-compatible clock or self-clocking options. For either option, LS is at V_{CC-}. For self-clocking, a resistor is connected between CLKIN and CLKR and a capacitor is connected from CLKIN to ground.
CLKR	2	I	Clock R. CLKR is the clock input for a TTL-compatible clock. For a TTL clock, LS is connected to midsupply and CLKIN can be left open, but it is recommended that it be connected to either V_{CC+} or V_{CC-}.
FILTER IN	8	I	Filter input
FILTER OUT	5	O	Butterworth fourth-order low-pass filter output
LS	3	I	Level shift. LS accommodates the various input clocking options. For CMOS-compatible clocks or self-clocking, LS is at V_{CC-} and for TTL-compatible clocks, LS is at midsupply.
V_{CC+}	7	I	Positive supply voltage terminal
V_{CC-}	4	I	Negative supply voltage terminal

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC\pm}$ (see Note 1) .... ±7 V
Operating free-air temperature range, T_A: TLC04C/MF4A-50C, TLC14C/MF4A-100C ...... 0°C to 70°C
TLC04I/MF4A-50I, TLC14I/MF4A-100I .... –40°C to 85°C
TLC04M/MF4A-50M, TLC14M/MF4A-100M .. –55°C to 125°C
Storage temperature range, T_{stg} .... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the AGND terminal.

recommended operating conditions

		TLC04/MF4A-50 MIN	TLC04/MF4A-50 MAX	TLC14/MF4A-100 MIN	TLC14/MF4A-100 MAX	UNIT
Positive supply voltage, V_{CC+}		2.25	6	2.25	6	V
Negative supply voltage, V_{CC-}		–2.25	–6	–2.25	–6	V
High-level input voltage, V_{IH}		2		2		V
Low-level input voltage, V_{IL}			0.8		0.8	V
Clock frequency, f_{clock} (see Note 2)	$V_{CC\pm}$ = ±2.5 V	5	1.5×10^6	5	1.5×10^6	Hz
	$V_{CC\pm}$ = ±5 V	5	2×10^6	5	2×10^6	
Cutoff frequency, f_{co} (see Note 3)		0.1	40×10^3	0.05	20×10^3	Hz
Operating free-air temperature, T_A	TLC04C/MF4A-50C, TLC14C/MF4A-100C	0	70	0	70	°C
	TLC04I/MF4A-50I, TLC14I/MF4A-100I	–40	85	–40	85	
	TLC04M/MF4A-50M, TLC14M/MF4A-100M	–55	125	–55	125	

NOTES: 2. Above 250 kHz, the input clock duty cycle should be 50% to allow the operational amplifiers the maximum time to settle while processing analog samples.
3. The cutoff frequency is defined as the frequency where the response is 3.01 dB less than the dc gain of the filter.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 2.5 V, V_{CC-} = –2.5 V, $f_{clock} \leq$ 250 kHz (unless otherwise noted)

filter section

PARAMETER			TEST CONDITIONS	TLC04/MF4A-50 MIN	TLC04/MF4A-50 TYP‡	TLC04/MF4A-50 MAX	TLC14/MF4A-100 MIN	TLC14/MF4A-100 TYP‡	TLC14/MF4A-100 MAX	UNIT
V_{OO}	Output offset voltage				25			50		mV
V_{OM}	Peak output voltage	V_{OM+}	R_L = 10 kΩ	1.8	2		1.8	2		V
		V_{OM-}		–1.25	–1.7		–1.25	–1.7		
I_{OS}	Short-circuit output current	Source	T_A = 25°C, See Note 4		–0.5			–0.5		mA
		Sink			4			4		
I_{CC}	Supply current		f_{clock} = 250 kHz		1.2	2.25		1.2	2.25	mA

‡ All typical values are at T_A = 25°C.

NOTE 4: $I_{OS(source)}$ is measured by forcing the output to its maximum positive voltage and then shorting the output to the V_{CC-} terminal. $I_{OS(sink)}$ is measured by forcing the output to its maximum negative voltage and then shorting the output to the V_{CC+} terminal.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, $f_{clock} \leq$ 250 kHz (unless otherwise noted)

filter section

PARAMETER			TEST CONDITIONS	TLC04/MF4A-50			TLC14/MF4A-100			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OO}	Output offset voltage				150			200		mV
V_{OM}	Peak output voltage	V_{OM+}	R_L = 10 kΩ	3.75	4.3		3.75	4.5		V
		V_{OM-}		−3.75	−4.1		−3.75	−4.1		
I_{OS}	Short-circuit output current	Source	T_A = 25°C, See Note 4		−2			−2		mA
		Sink			5			5		
I_{CC}	Supply current		f_{clock} = 250 kHz		1.8	3		1.8	3	mA
k_{SVS}	Supply voltage sensitivity (see Figures 1 and 2)				−30			−30		dB

† All typical values are at T_A = 25°C.

NOTE 4: $I_{OS(source)}$ is measured by forcing the output to its maximum positive voltage and then shorting the output to the V_{CC-} terminal. $I_{OS(sink)}$ is measured by forcing the output to its maximum negative voltage and then shorting the output to the V_{CC+} terminal.

clocking section

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	CLKIN	V_{CC+} = 10 V,	V_{CC-} = 0	6.1	7	8.9	V
			V_{CC+} = 5 V,	V_{CC-} = 0	3.1	3.5	4.4	
V_{IT-}	Negative-going input threshold voltage		V_{CC+} = 10 V,	V_{CC-} = 0	1.3	3	3.8	V
			V_{CC+} = 5 V,	V_{CC-} = 0	0.6	1.5	1.9	
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)		V_{CC+} = 10 V,	V_{CC-} = 0	2.3	4	7.6	V
			V_{CC+} = 5 V,	V_{CC-} = 0	1.2	2	3.8	
V_{OH}	High-level output voltage	CLKR	V_{CC} = 10 V	I_O = −10 µA	9			V
			V_{CC} = 5 V		4.5			
V_{OL}	Low-level output voltage		V_{CC} = 10 V	I_O = 10 µA			1	V
			V_{CC} = 5 V				0.5	
	Input leakage current		V_{CC} = 10 V	LS at midsupply, T_A = 25°C			2	µA
			V_{CC} = 5 V				2	
I_O	Output current		V_{CC} = 10 V	CLKR and CLKIN shortened to V_{CC-}	−3	−7		mA
			V_{CC} = 5 V		−0.75	−2		
			V_{CC} = 10 V	CLKR and CLKIN shortened to V_{CC+}	3	7		mA
			V_{CC} = 5 V		0.75	2		

† All typical values are at T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 2.5 V, V_{CC-} = –2.5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLC04/MF4A-50			TLC14/MF4A-100			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Maximum clock frequency, f_{max}	See Note 2		1.5	3		1.5	3		MHz
Clock-to-cutoff-frequency ratio (f_{clock}/f_{co})	f_{clock} ≤ 250 kHz, T_A = 25°C		49.27	50.07	50.87	99	100	101	Hz/Hz
Temperature coefficient of clock-to-cutoff frequency ratio	f_{clock} ≤ 250 kHz			±25			±25		ppm/°C
Frequency response above and below cutoff frequency (see Note 5)	f_{co} = 5 kHz, f_{clock} = 250 kHz, T_A = 25°C	f = 6 kHz	–7.9	–7.57	–7.1				dB
		f = 4.5 kHz	–1.7	–1.46	–1.3				
	f_{co} = 5 kHz, f_{clock} = 250 kHz, T_A = 25°C	f = 3 kHz				–7.9	–7.42	–7.1	dB
		f = 2.25 kHz				–1.7	–1.51	–1.3	
Dynamic range (see Note 6)	T_A = 25°C			80			78		dB
Stop-band frequency attentuation at 2 f_{co}	f_{clock} ≤ 250 kHz		24	25		24	25		dB
Voltage amplification, dc	f_{clock} ≤ 250 kHz, RS ≤ 2 kΩ		–0.15	0	0.15	–0.15	0	0.15	dB
Peak-to-peak clock feedthrough voltage	T_A = 25°C			5			5		mV

† All typical values are at T_A = 25°C.

NOTES: 2. Above 250 kHz, the input clock duty cycle should be 50% to allow the operational amplifiers the maximum time to settle while processing analog samples.

5. The frequency responses at f are referenced to a dc gain of 0 dB.
6. The dynamic range is referenced to 1.06 V rms (1.5 V peak) where the wideband noise over a 30-kHz bandwidth is typically 106 µV rms for the TLC04/MF4A-50 and 135 µV rms for the TLC14/MF4A-100.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = –5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLC04/MF4A-50			TLC14/MF4A-100			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Maximum clock frequency, f_{max}	See Note 2		2	4		2	4		MHz
Clock-to-cutoff-frequency ratio (f_{clock}/f_{co})	f_{clock} ≤ 250 kHz, T_A = 25°C		49.58	49.98	50.38	99	100	101	Hz/Hz
Temperature coefficient of clock-to-cutoff frequency ratio	f_{clock} ≤ 250 kHz			±15			±15		ppm/°C
Frequency response above and below cutoff frequency (see Note 5)	f_{co} = 5 kHz, f_{clock} = 250 kHz, T_A = 25°C	f = 6 kHz	–7.9	–7.57	–7.1				dB
		f = 4.5 kHz	–1.7	–1.44	–1.3				
	f_{co} = 5 kHz, f_{clock} = 250 kHz, T_A = 25°C	f = 3 kHz				–7.9	–7.42	–7.1	dB
		f = 2.25 kHz				–1.7	–1.51	–1.3	
Dynamic range (see Note 6)	T_A = 25°C			86			84		dB
Stop-band frequency attentuation at 2 f_{co}	f_{clock} ≤ 250 kHz		24	25		24	25		dB
Voltage amplification, dc	f_{clock} ≤ 250 kHz, RS ≤ 2 kΩ		–0.15	0	0.15	–0.15	0	0.15	dB
Peak-to-peak clock feedthrough voltage	T_A = 25°C			7			7		mV

† All typical values are at T_A = 25°C.

NOTES: 2. Above 250 kHz, the input clock duty cycle should be 50% to allow the operational amplifiers the maximum time to settle while processing analog samples.

5. The frequency responses at f are referenced to a dc gain of 0 dB.
6. The dynamic range is referenced to 2.82 V rms (4 V peak) where the wideband noise over a 30-kHz bandwidth is typically 142 µV rms for the TLC04/MF4A-50 and 178 µV rms for the TLC14/MF4A-100.

TYPICAL CHARACTERISTICS

FILTER OUTPUT
vs
SUPPLY VOLTAGE V_{CC+} RIPPLE FREQUENCY

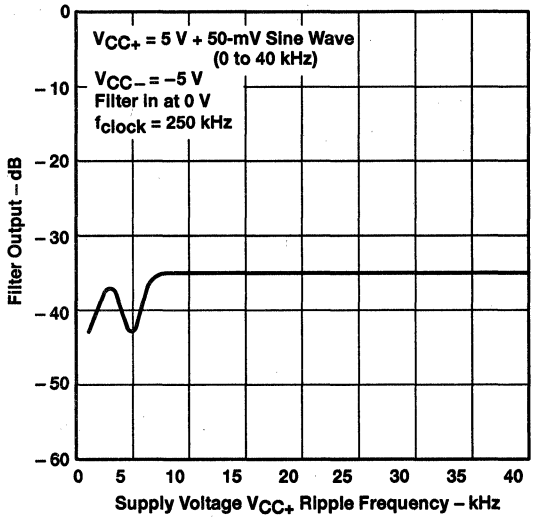


Figure 1

FILTER OUTPUT
vs
SUPPLY VOLTAGE V_{CC-} RIPPLE FREQUENCY

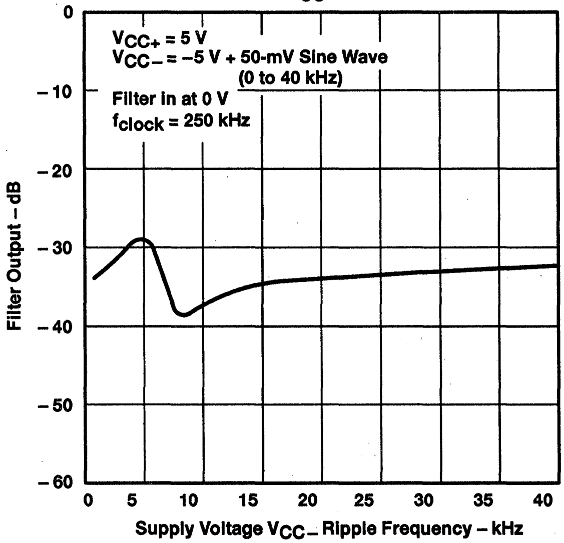


Figure 2

APPLICATION INFORMATION

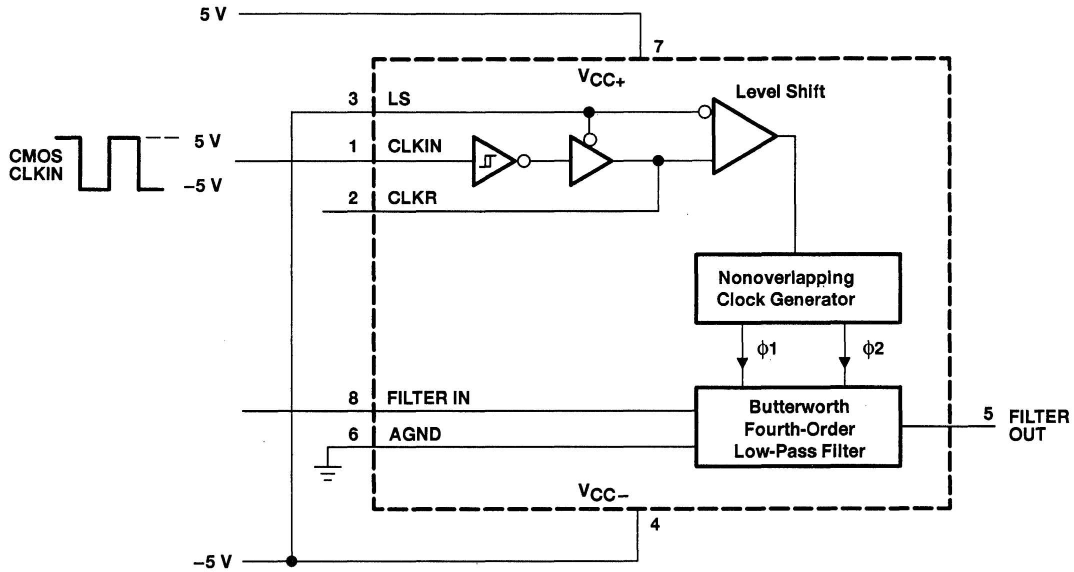


Figure 3. CMOS-Clock-Driven Dual-Supply Operation

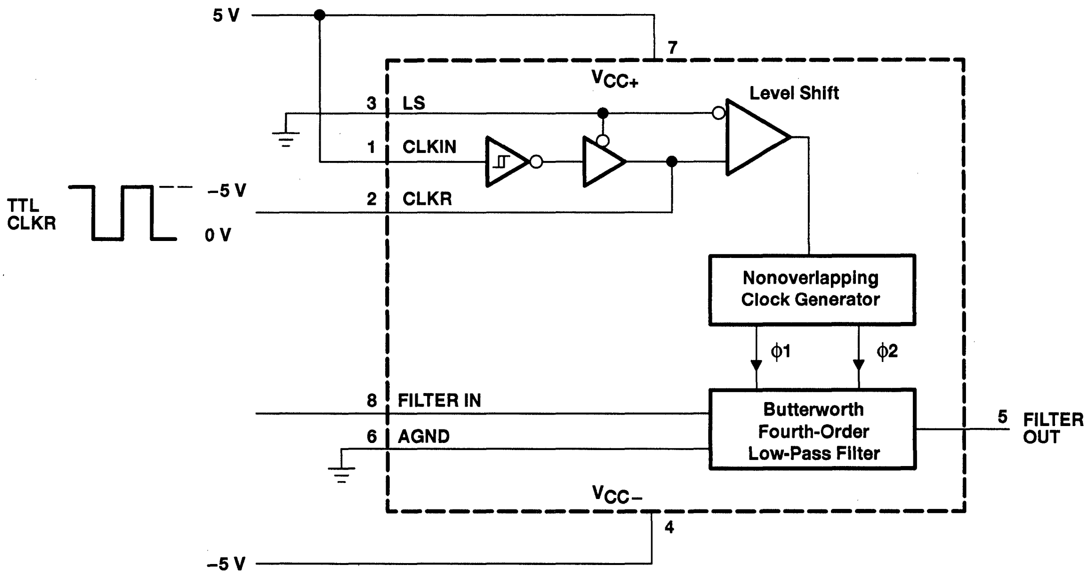
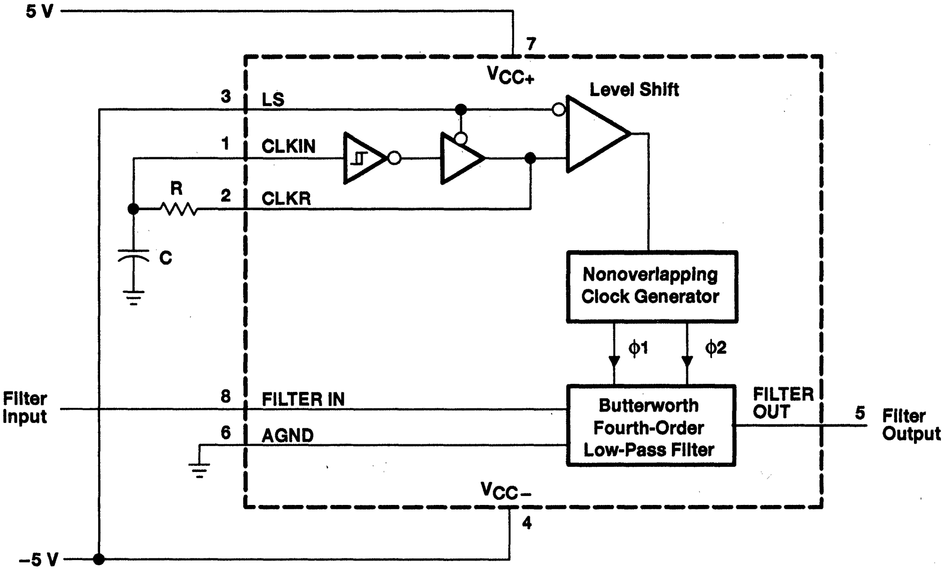


Figure 4. TTL-Clock-Driven Dual-Supply Operation

APPLICATION INFORMATION



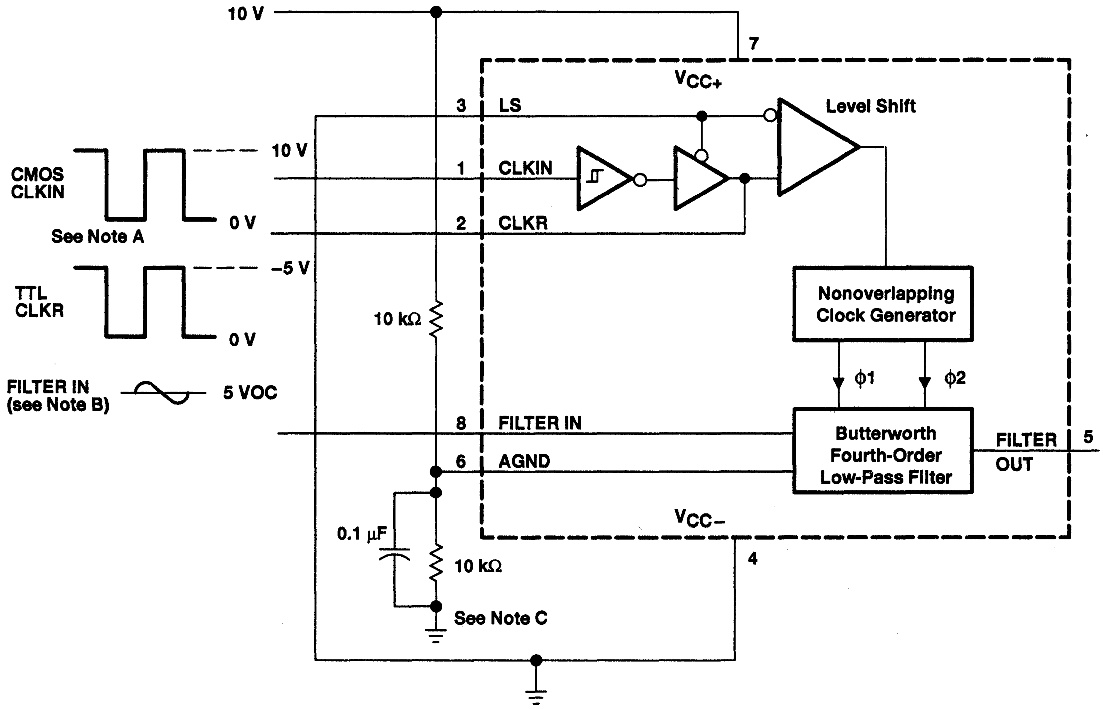
$$f_{clock} = \frac{1}{RC \times \ln\left[\left(\frac{V_{CC}-V_{IT-}}{V_{CC}-V_{IT+}}\right)\left(\frac{V_{IT+}}{V_{IT-}}\right)\right]}$$

For V_{CC} = 10 V

$$f_{clock} = \frac{1}{1.69\ RC}$$

Figure 5. Self-Clocking Through Schmitt-Trigger Oscillator Dual-Supply Operation

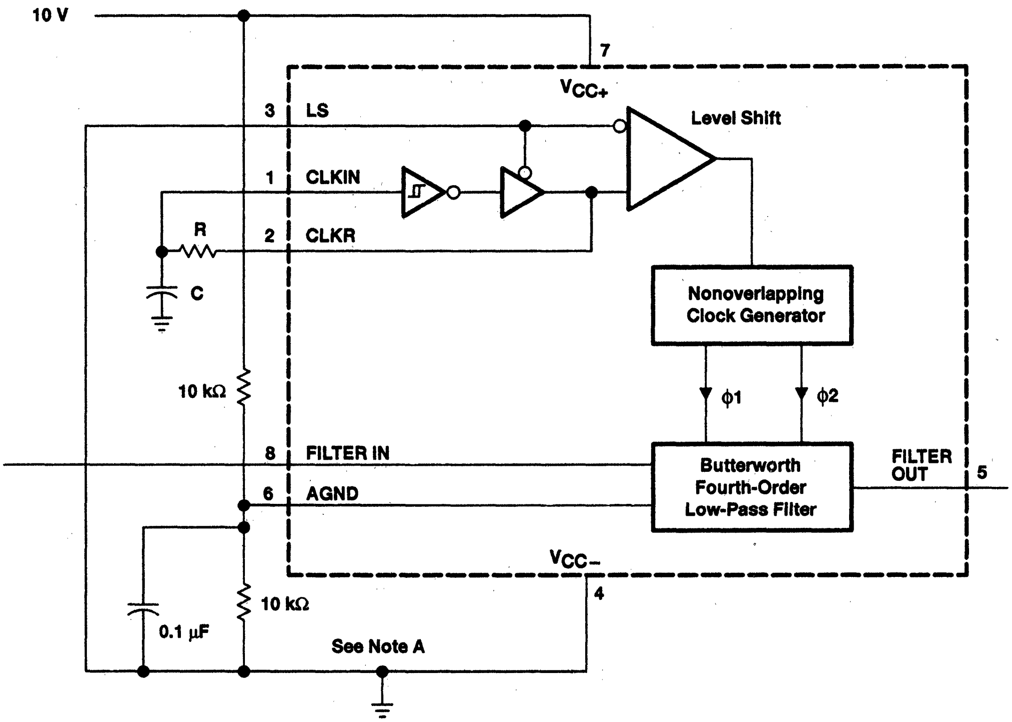
APPLICATION INFORMATION



NOTES: A. The external clock used must be of CMOS level because the clock is input to a CMOS Schmitt trigger.
B. The filter input signal should be dc-biased to midsupply or ac-coupled to the terminal.
C. AGND must be biased to midsupply.

Figure 6. External-Clock-Driven Single-Supply Operation

APPLICATION INFORMATION



$$f_{clock} = \frac{1}{RC \times \ln\left[\left(\frac{V_{CC}-V_{IT-}}{V_{CC}-V_{IT+}}\right)\left(\frac{V_{IT+}}{V_{IT-}}\right)\right]}$$

For V_{CC} = 10 V

$$f_{clock} = \frac{1}{1.69\ RC}$$

NOTE A: AGND must be biased to midsupply.

Figure 7. Self Clocking Through Schmitt-Trigger Oscillator Single-Supply Operation

APPLICATION INFORMATION

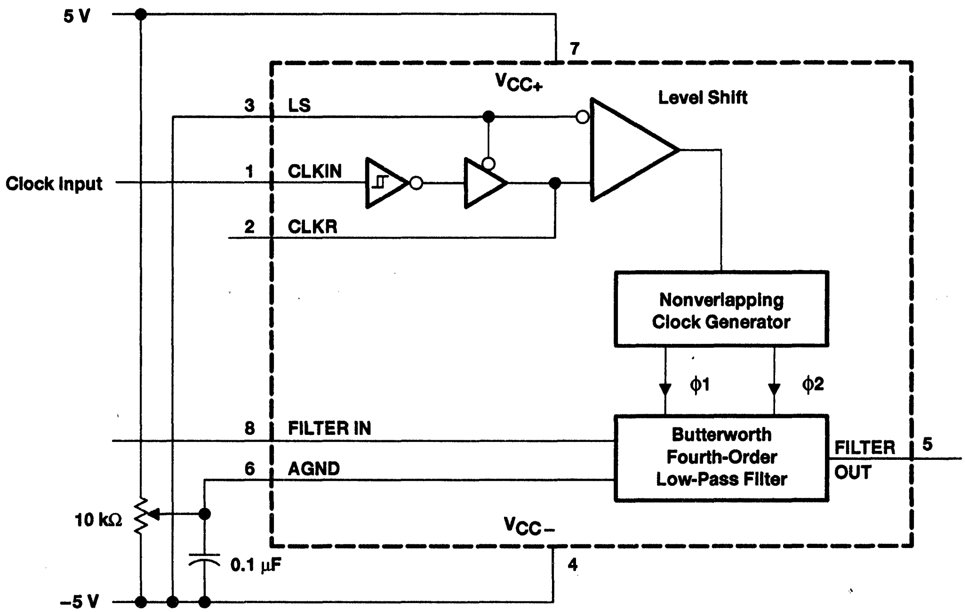
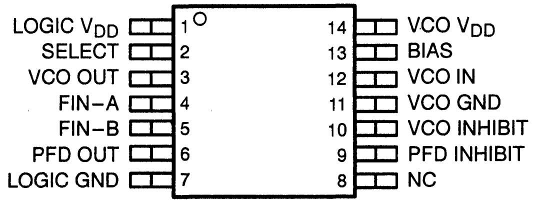


Figure 8. DC Offset Adjustment

- **Voltage-Controlled Oscillator (VCO) Section:**
  - **Complete Oscillator Using Only One External Bias Resistor (R_{BIAS})**
  - **Lock Frequency:**
    - **22 MHz to 50 MHz (V_{DD} = 5 V ±5%, T_A = –20°C to 75°C, ×1 Output)**
    - **11 MHz to 25 MHz (V_{DD} = 5 V ±5%, T_A = –20°C to 75°C, ×1/2 Output)**
  - **Output Frequency . . . ×1 and ×1/2 Selectable**
- **Phase-Frequency Detector (PFD) Section:**
  - **High Speed, Edge-Triggered Detector With Internal Charge Pump**
- **Independent VCO, PFD Power-Down Mode**
- **Thin Small-Outline Package (14 terminal)**
- **CMOS Technology**
- **Typical Applications:**
  - **Frequency Synthesis**
  - **Modulation/Demodulation**
  - **Fractional Frequency Division**
- **Application Report Available†**
- **CMOS Input Logic Level**

PW PACKAGE†
(TOP VIEW)

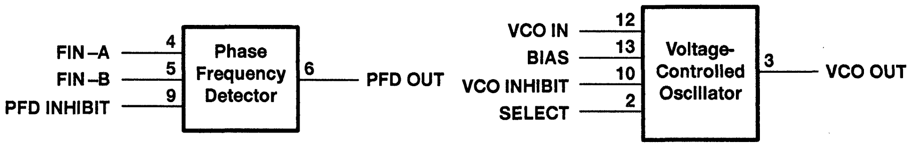


† Available in tape and reel only and ordered as the TLC2932IPWLE.
NC – No internal connection

description

The TLC2932I is designed for phase-locked-loop (PLL) systems and is composed of a voltage-controlled oscillator (VCO) and an edge-triggered type phase frequency detector (PFD). The oscillation frequency range of the VCO is set by an external bias resistor (R_{BIAS}). The VCO has a 1/2 frequency divider at the output stage. The high speed PFD with internal charge pump detects the phase difference between the reference frequency input and signal frequency input from the external counter. Both the VCO and the PFD have inhibit functions, which can be used as a power-down mode. Due to the TLC2932I high speed and stable oscillation capability, the TLC2932I is suitable for use as a high-performance PLL.

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGE SMALL OUTLINE (PW)
–20°C to 75°C	TLC2932IPWLE

† TLC2932 Phase-Locked-Loop Building Block With Analog Voltage-Controlled Oscillator and Phase Frequency Detector (SLAA011).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
FIN−A	4	I	Input reference frequency $f_{(REF\ IN)}$ is applied to FIN−A.
FIN−B	5	I	Input for VCO external counter output frequency $f_{(FIN-B)}$. FIN−B is nominally provided from the external counter, see functional block diagram.
LOGIC GND	7		GND for the internal logic.
LOGIC V_{DD}	1		Power supply for the internal logic. This power supply should be separate from VCO V_{DD} to reduce cross-coupling between supplies.
NC	8		No internal connection.
PFD INHIBIT	9	I	PFD inhibit control. When PFD INHIBIT is high, PFD output is in the high-impedance state, see Table 3.
PFD OUT	6	O	PFD output. When the PFD INHIBIT is high, PFD output is in the high-impedance state.
BIAS	13	I	Bias supply. An external resistor (R_{BIAS}) between VCO V_{DD} and BIAS supplies bias for adjusting the oscillation frequency range.
SELECT	2	I	VCO output frequency select. When SELECT is high, the VCO output frequency is ×1/2 and when low, the output frequency is ×1, see Table 1.
VCO IN	12	I	VCO control voltage input. Nominally the external loop filter output connects to VCO IN to control VCO oscillation frequency.
VCO INHIBIT	10	I	VCO inhibit control. When VCO INHIBIT is high, VCO OUT is low (see Table 2).
VCO GND	11		GND for VCO.
VCO OUT	3	O	VCO output. When the VCO INHIBIT is high, VCO output is low.
VCO V_{DD}	14		Power supply for VCO. This power supply should be separated from LOGIC V_{DD} to reduce cross-coupling between supplies.

detailed description

VCO oscillation frequency

The VCO oscillation frequency is determined by an external resistor (R_{BIAS}) connected between the VCO V_{DD} and the BIAS terminals. The oscillation frequency and range depends on this resistor value. The bias resistor value for the minimum temperature coefficient is nominally 3.3 kΩ with 3-V V_{DD} and nominally 2.2 kΩ with 5-V V_{DD}. For the lock frequency range refer to the recommended operating conditions. Figure 1 shows the typical frequency variation and VCO control voltage.

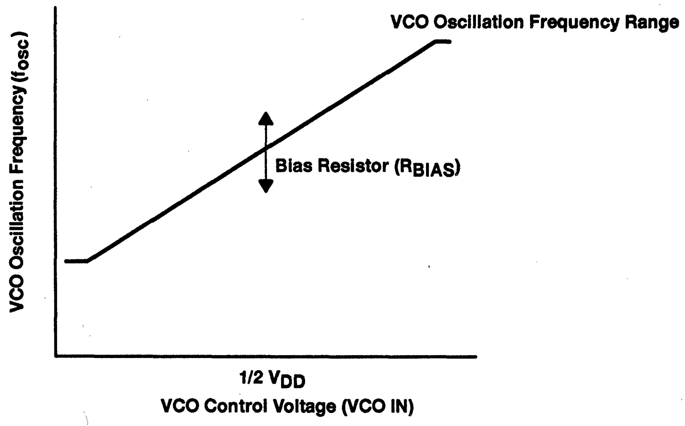


Figure 1. VCO Oscillation Frequency

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VCO output frequency 1/2 divider

The TLC2932I SELECT terminal can select between the f_{OSC} and 1/2 f_{OSC} VCO output frequencies as shown in Table 1. The 1/2 f_{OSC} output should be used for minimum VCO output jitter.

Table 1. VCO Output 1/2 Divider Function

SELECT	VCO OUTPUT
Low	f_{OSC}
High	1/2 f_{OSC}

VCO inhibit function

The VCO has an externally controlled inhibit function which inhibits the VCO output. A high level on the VCO INHIBIT terminal stops the VCO oscillation and powers down the VCO. The output maintains a low level during the power-down mode, refer to Table 2.

Table 2. VCO Inhibit Function

VCO INHIBIT	VCO OSCILLATOR	VCO OUTPUT	$I_{DD(VCO)}$
Low	Active	Active	Normal
High	Stopped	Low level	Power Down

PFD operation

The PFD is a high-speed, edge-triggered detector with an internal charge pump. The PFD detects the phase difference between two frequency inputs supplied to FIN–A and FIN–B as shown in Figure 2. Nominally the reference is supplied to FIN–A, and the frequency from the external counter output is fed to FIN–B. For clock recovery PLL systems, other types of phase detectors should be used.

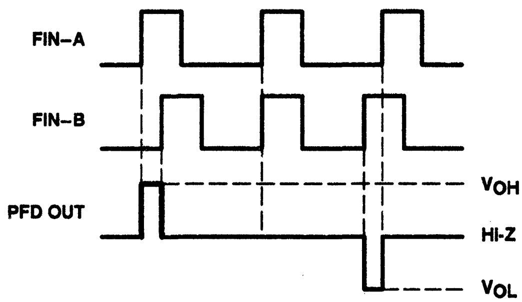


Figure 2. PFD Function Timing Chart

PFD output control

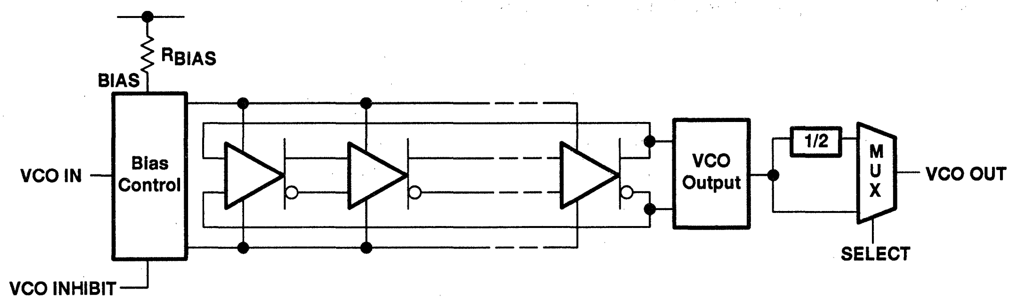
A high level on the PFD INHIBIT terminal places the PFD output in the high-impedance state and the PFD stops phase detection as shown in Table 3. A high level on the PFD INHIBIT terminal also can be used as the power-down mode for the PFD.

Table 3. VCO Output Control Function

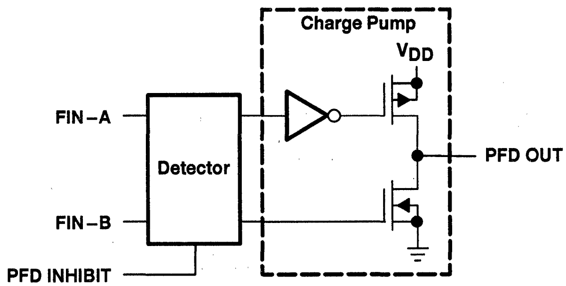
PFD INHIBIT	DETECTION	PFD OUTPUT	$I_{DD(PFD)}$
Low	Active	Active	Normal
High	Stop	Hi-Z	Power Down

schematics

VCO block schematic



PFD block schematic



absolute maximum ratings†

Supply voltage (each supply), V_{DD} (see Note 1)	7 V
Input voltage range (each input), V_I (see Note 1)	–0.5 V to V_{DD} + 0.5 V
Input current (each input), I_I	±20 mA
Output current (each output), I_O	±20 mA
Continuous total dissipation, at (or below) T_A = 25°C	700 mW
Operating free-air temperature range, T_A	–20°C to 75°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network GND.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 5.6 mW/°C.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (each supply, see Note 3)	V_{DD} = 3 V	2.85	3	3.15	V
	V_{DD} = 5 V	4.75	5	5.25	
Input voltage, V_I (inputs except VCO IN)		0		V_{DD}	V
Output current, I_O (each output)		0		±2	mA
VCO control voltage at VCO IN		0.9		V_{DD}	V
Lock frequency (×1 output)	V_{DD} = 3 V	14		21	MHz
	V_{DD} = 5 V	22		50	
Lock frequency (×1/2 output)	V_{DD} = 3 V	7		10.5	MHz
	V_{DD} = 5 V	11		25	
Bias resistor, R_{BIAS}	V_{DD} = 3 V	2.2	3.3	4.3	kΩ
	V_{DD} = 5 V	1.5	2.2	3.3	

NOTE 3: It is recommended that the logic supply terminal (LOGIC V_{DD}) and the VCO supply terminal (VCO V_{DD}) should be at the same voltage and separated from each other.

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 3 V (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.3	V
V_{IT}	Input threshold voltage at SELECT, VCO INHIBIT		0.9	1.5	2.1	V
I_I	Input current at SELECT, VCO INHIBIT	V_I = V_{DD} or GND			±1	µA
$Z_{i(VCO\ IN)}$	Input impedance	VCO IN = 1/2 V_{DD}		10		MΩ
$I_{DD(INH)}$	VCO supply current (inhibit)	See Note 4		0.01	1	µA
$I_{DD(VCO)}$	VCO supply current	See Note 5		5	15	mA

NOTES: 4. Current into VCO V_{DD}, when VCO INHIBIT = V_{DD}, PFD is inhibited.
5. Current into VCO V_{DD}, when VCO IN = 1/2 V_{DD}, R_{BIAS} = 3.3 kΩ, VCO INHIBIT = GND, and PFD is inhibited.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	2.7			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.2	V
I_{OZ}	High-impedance-state output current	PFD INHIBIT = high, V_I = V_{DD} or GND			±1	µA
V_{IH}	High-level input voltage at FIN–A, FIN–B		2.7			V
V_{IL}	Low-level input voltage at FIN–A, FIN–B				0.5	V
V_{IT}	Input threshold voltage at PFD INHIBIT		0.9	1.5	2.1	V
C_i	Input capacitance at FIN–A, FIN–B			5		pF
Z_i	Input impedance at FIN–A, FIN–B			10		MΩ
$I_{DD(Z)}$	High-impedance-state PFD supply current	See Note 6		0.01	1	µA
$I_{DD(PFD)}$	PFD supply current	See Note 7		0.1	1.5	mA

NOTES: 6. Current into LOGIC V_{DD}, when FIN–A, FIN–B = GND, PFD INHIBIT = V_{DD}, no load, and VCO OUT is inhibited.
7. Current into LOGIC V_{DD}, when FIN–A, FIN–B = 1 MHz ($V_{I(PP)}$ = 3 V, rectangular wave), NC = GND, no load, and VCO OUT is inhibited.

operating characteristics over recommended operating free-air temperature range, V_{DD} = 3 V (unless otherwise noted)

VCO section

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Operating oscillation frequency	R_{BIAS} = 3.3 kΩ, VCO IN = 1/2 V_{DD}	15	19	23	MHz
$t_{s(fosc)}$	Time to stable oscillation (see Note 8)	Measured from VCO INHIBIT↓			10	µs
t_r	Rise time	C_L = 15 pF, See Figure 3		7	14	ns
		C_L = 50 pF, See Figure 3		14		
t_f	Fall time	C_L = 15 pF, See Figure 3		6	12	ns
		C_L = 50 pF, See Figure 3		10		
	Duty cycle at VCO OUT	R_{BIAS} = 3.3 kΩ, VCO IN = 1/2 V_{DD},	45%	50%	55%	
$\alpha_{(fosc)}$	Temperature coefficient of oscillation frequency	R_{BIAS} = 3.3 kΩ, VCO IN = 1/2 V_{DD}, T_A = –20°C to 75°C		0.04		%/°C
$k_{SVS(fosc)}$	Supply voltage coefficient of oscillation frequency	R_{BIAS} = 3.3 kΩ, VCO IN = 1.5 V, V_{DD} = 2.85 V to 3.15 V		0.02		%/mV
	Jitter absolute (see Note 9)	R_{BIAS} = 3.3 kΩ		100		ps

NOTES: 8. The time period to the stable VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.
9. The LPF circuit is shown in Figure 28 with calculated values listed in Table 7. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully designed PCB with no device socket.

PFD section

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operating frequency		20			MHz
t_{PLZ}	PFD output disable time from low level	See Figures 4 and 5 and Table 4		21	50	ns
t_{PHZ}	PFD output disable time from high level			23	50	
t_{PZL}	PFD output enable time to low level			11	30	ns
t_{PZH}	PFD output enable time to high level			10	30	
t_r	Rise time	C_L = 15 pF, See Figure 4		2.3	10	ns
t_f	Fall time			2.1	10	ns

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −2 mA	4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.5	V
V_{IT}	Input threshold voltage at SELECT, VCO INHIBIT		1.5	2.5	3.5	V
I_I	Input current at SELECT, VCO INHIBIT	$V_I = V_{DD}$ or GND			±1	μA
$Z_{i(VCO\ IN)}$	Input impedance	VCO IN = 1/2 V_{DD}		10		MΩ
$I_{DD(INH)}$	VCO supply current (inhibit)	See Note 4		0.01	1	μA
$I_{DD(VCO)}$	VCO supply current	See Note 5		15	35	mA

NOTES: 4. Current into VCO V_{DD}, when VCO INHIBIT = V_{DD}, and PFD is inhibited.
5. Current into VCO V_{DD}, when VCO IN = 1/2 V_{DD}, R_{BIAS} = 3.3 kΩ, VCO INHIBIT = GND, and PFD is inhibited.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 2 mA	4.5			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.2	V
I_{OZ}	High-impedance-state output current	PFD INHIBIT = high, $V_I = V_{DD}$ or GND			±1	μA
V_{IH}	High-level input voltage at FIN–A, FIN–B		4.5			V
V_{IL}	Low-level input voltage at FIN–A, FIN–B				1	V
V_{IT}	Input threshold voltage at PFD INHIBIT		1.5	2.5	3.5	V
C_i	Input capacitance at FIN–A, FIN–B			5		pF
Z_i	Input impedance at FIN–A, FIN–B			10		MΩ
$I_{DD(Z)}$	High-impedance-state PFD supply current	See Note 6		0.01	1	μA
$I_{DD(PFD)}$	PFD supply current	See Note 7		0.15	3	mA

NOTES: 6. Current into LOGIC V_{DD}, when FIN–A, FIN–B = GND, PFD INHIBIT = V_{DD}, no load, and VCO OUT is inhibited.
7. Current into LOGIC V_{DD}, when FIN–A, FIN–B = 1 MHz ($V_{I(PP)}$ = 5 V, rectangular wave), PFD INHIBIT = GND, no load, and VCO OUT is inhibited.

operating characteristics over recommended operating free-air temperature range, V_{DD} = 5 V (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Operating oscillation frequency	R_{BIAS} = 2.2 kΩ, VCO IN = 1/2 V_{DD}	30	41	52	MHz
$t_{s(fosc)}$	Time to stable oscillation (see Note 8)	Measured from VCO INHIBIT↓			10	µs
t_r	Rise time	C_L = 15 pF, See Figure 3		5.5	10	ns
		C_L = 50 pF, See Figure 3		8		
t_f	Fall time	C_L = 15 pF, See Figure 3		5	10	ns
		C_L = 50 pF, See Figure 3		6		
	Duty cycle at VCO OUT	R_{BIAS} = 2.2 kΩ, VCO IN = 1/2 V_{DD},	45%	50%	55%	
$\alpha_{(fosc)}$	Temperature coefficient of oscillation frequency	R_{BIAS} = 2.2 kΩ, VCO IN = 1/2 V_{DD}, T_A = –20°C to 75°C		0.06		%/°C
$k_{SVS(fosc)}$	Supply voltage coefficient of oscillation frequency	R_{BIAS} = 2.2 kΩ, VCO IN = 2.5 V, V_{DD} = 4.75 V to 5.25 V		0.006		%/mV
	Jitter absolute (see Note 9)	R_{BIAS} = 2.2 kΩ		100		ps

NOTES: 8: The time period to the stable VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.
9. The LPF circuit is shown in Figure 28 with calculated values listed in Table 7. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully designed PCB with no device socket.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operating frequency		40			MHz
t_{PLZ}	PFD output disable time from low level	See Figures 4 and 5 and Table 4		21	40	ns
t_{PHZ}	PFD output disable time from high level			20	40	
t_{PZL}	PFD output enable time to low level			7.3	20	ns
t_{PZH}	PFD output enable time to high level			6.5	20	
t_r	Rise time	C_L = 15 pF, See Figure 4		2.3	10	ns
t_f	Fall time			1.7	10	ns

PARAMETER MEASUREMENT INFORMATION

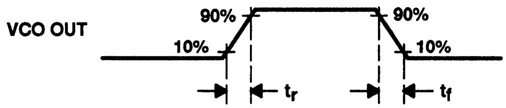
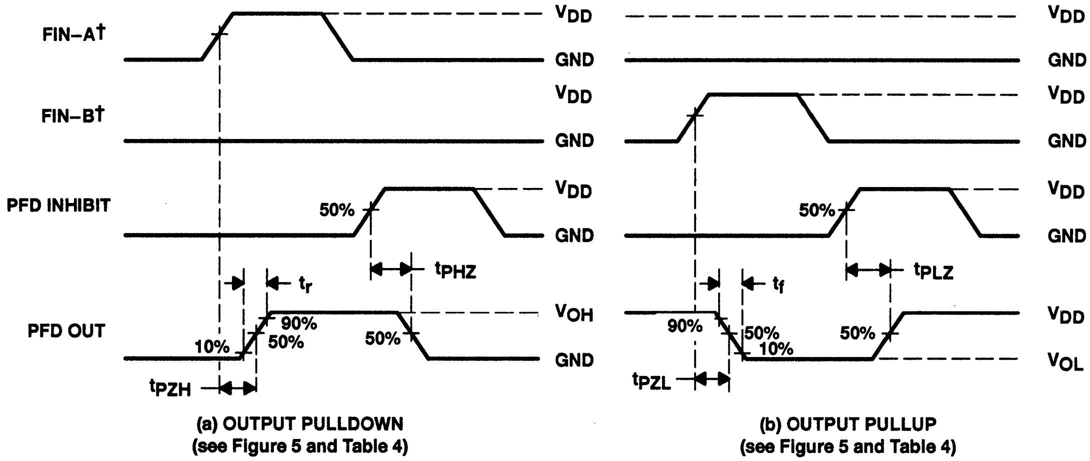


Figure 3. VCO Output Voltage Waveform



† FIN–A and FIN–B are for reference phase only, not for timing.

Figure 4. PFD Output Voltage Waveform

PARAMETER MEASUREMENT INFORMATION

Table 4. PFD Output Test Conditions

PARAMETER	R_L	C_L	S_1	S_2
t_{PZH}	1 kΩ	15 pF	Open	Close
t_{PHZ}				
t_r				
t_{PZL}			Close	Open
t_{PLZ}				
t_f				

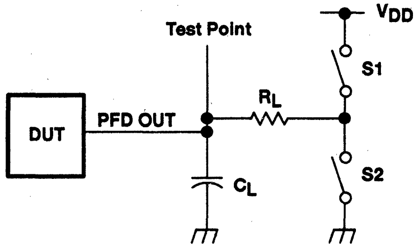


Figure 5. PFD Output Test Conditions

TYPICAL CHARACTERISTICS

VCO OSCILLATION FREQUENCY vs VCO CONTROL VOLTAGE

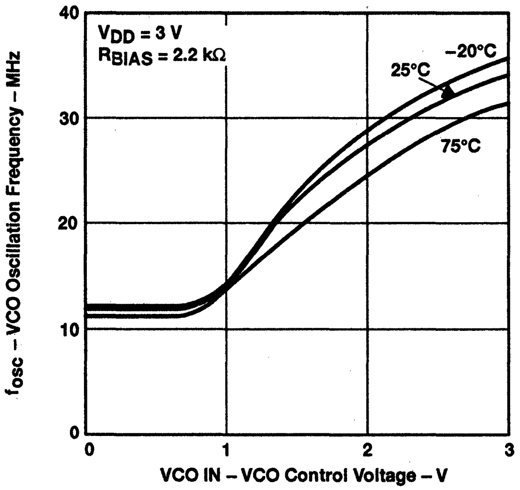


Figure 6

VCO OSCILLATION FREQUENCY vs VCO CONTROL VOLTAGE

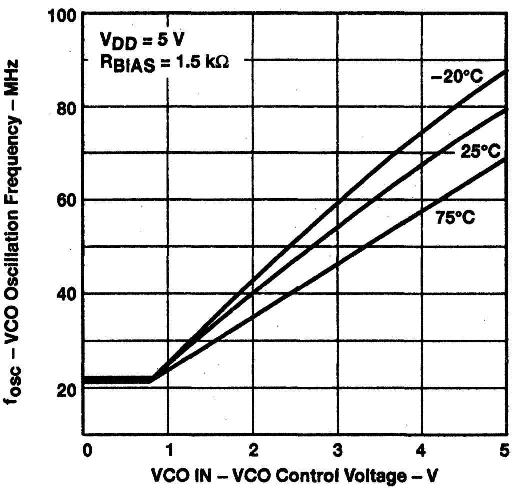


Figure 7

TYPICAL CHARACTERISTICS

VCO OSCILLATION FREQUENCY vs VCO CONTROL VOLTAGE

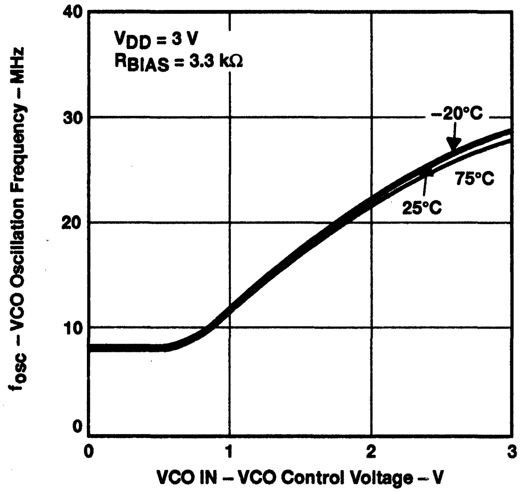


Figure 8

VCO OSCILLATION FREQUENCY vs VCO CONTROL VOLTAGE

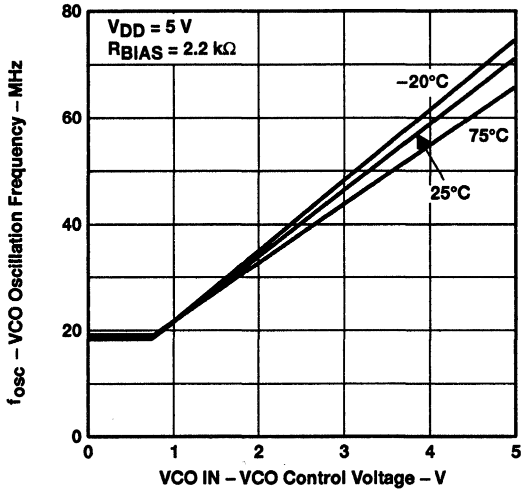


Figure 9

VCO OSCILLATION FREQUENCY vs VCO CONTROL VOLTAGE

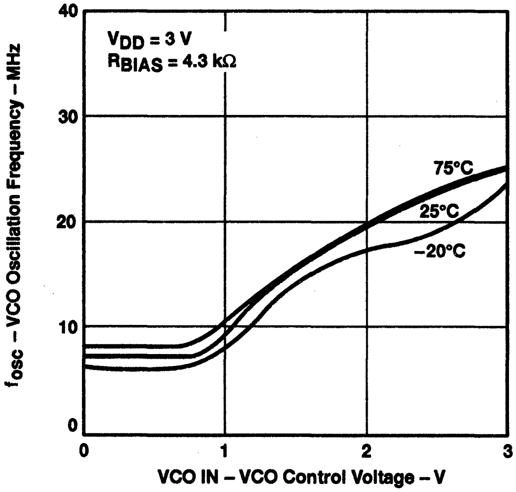


Figure 10

VCO OSCILLATION FREQUENCY vs VCO CONTROL VOLTAGE

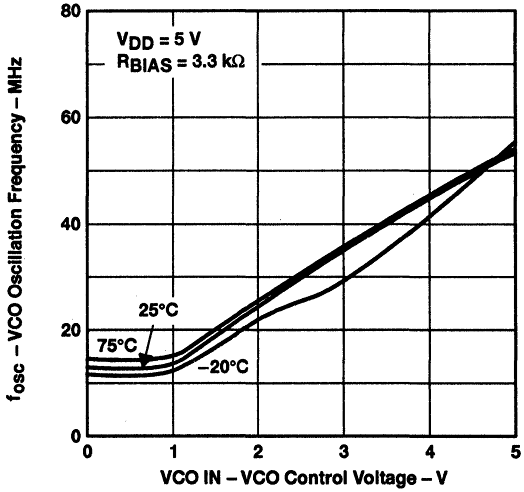


Figure 11

TYPICAL CHARACTERISTICS

VCO OSCILLATION FREQUENCY vs BIAS RESISTOR

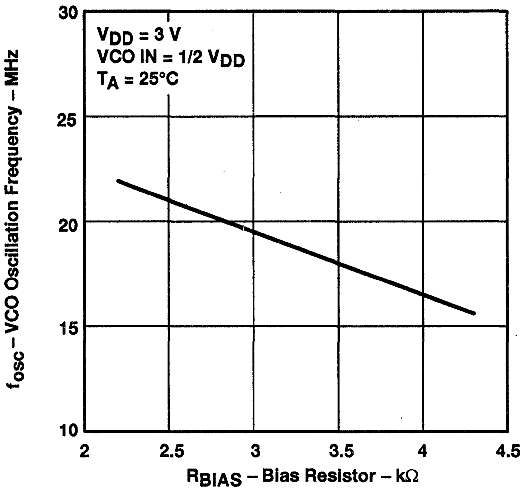


Figure 12

VCO OSCILLATION FREQUENCY vs BIAS RESISTOR

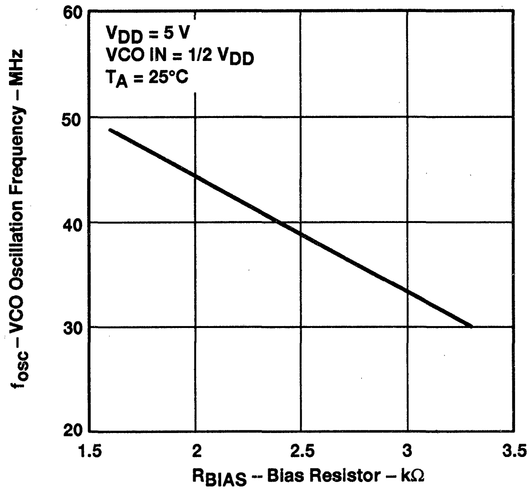


Figure 13

TEMPERATURE COEFFICIENT OF OSCILLATION FREQUENCY vs BIAS RESISTOR

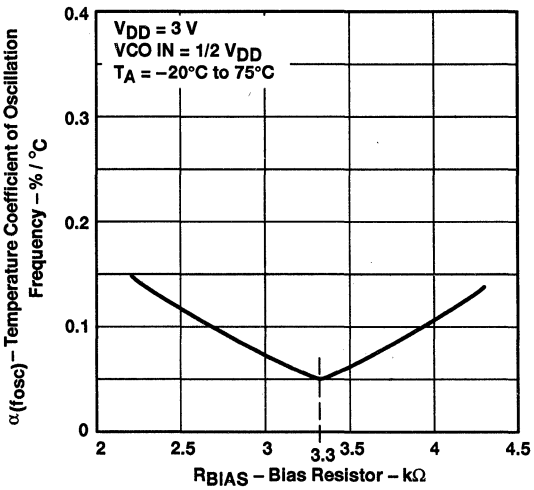


Figure 14

TEMPERATURE COEFFICIENT OF OSCILLATION FREQUENCY vs BIAS RESISTOR

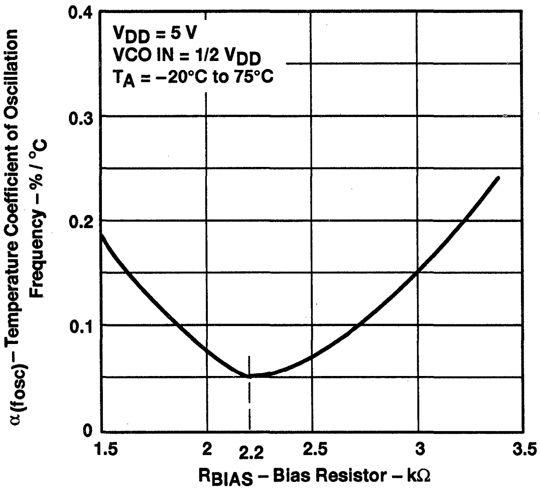


Figure 15

TYPICAL CHARACTERISTICS

VCO OSCILLATION FREQUENCY
vs
VCO SUPPLY VOLTAGE

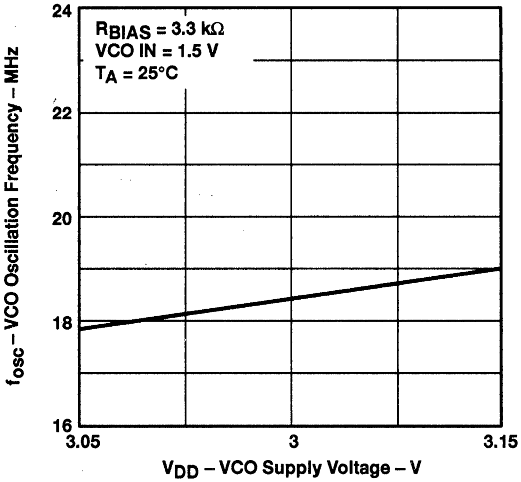


Figure 16

VCO OSCILLATION FREQUENCY
vs
VCO SUPPLY VOLTAGE

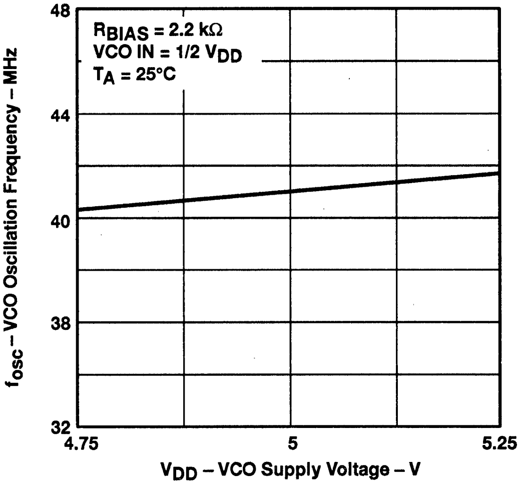


Figure 17

SUPPLY VOLTAGE COEFFICIENT OF VCO
OSCILLATION FREQUENCY
vs
BIAS RESISTOR

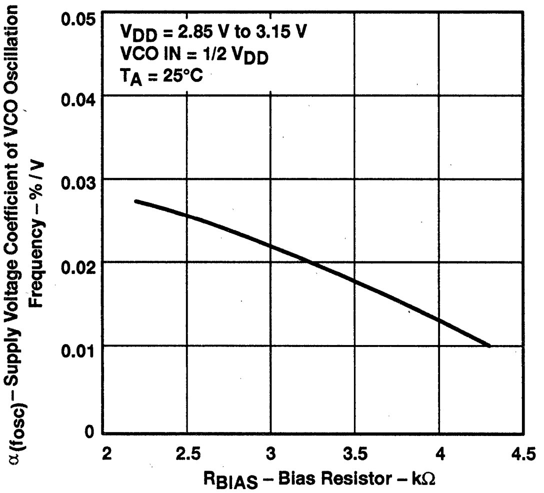


Figure 18

SUPPLY VOLTAGE COEFFICIENT OF VCO
OSCILLATION FREQUENCY
vs
BIAS RESISTOR

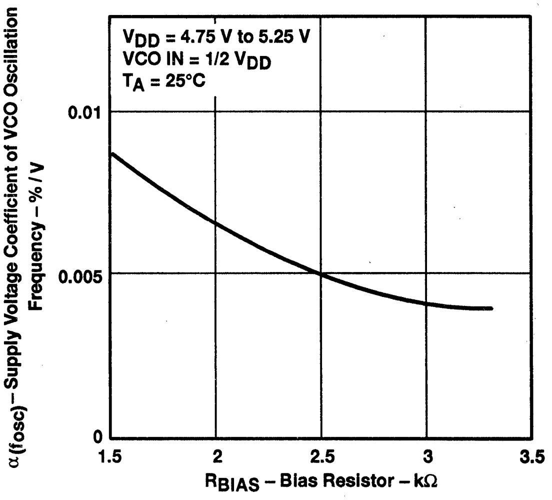


Figure 19

APPLICATION INFORMATION

RECOMMENDED LOCK FREQUENCY (×1 OUTPUT) vs BIAS RESISTOR

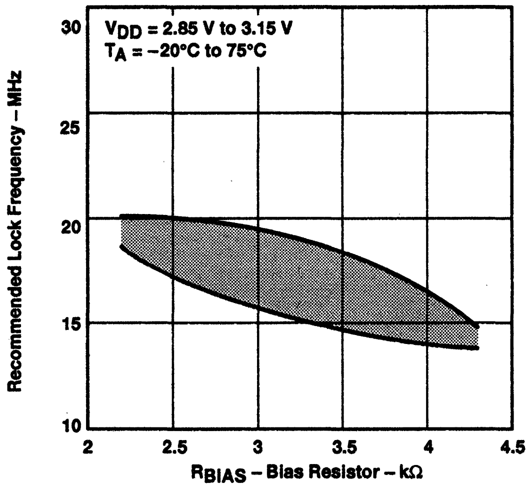


Figure 20

RECOMMENDED LOCK FREQUENCY (×1 OUTPUT) vs BIAS RESISTOR

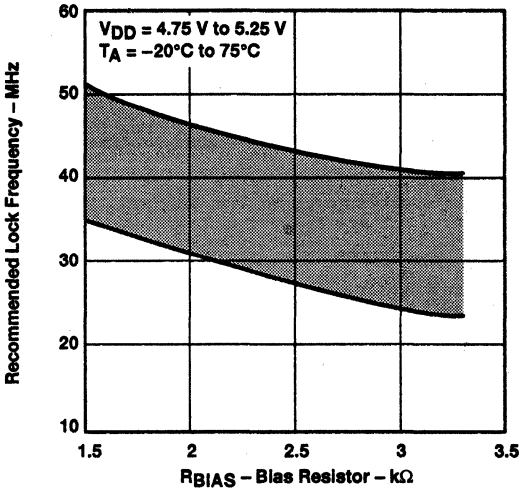


Figure 21

RECOMMENDED LOCK FREQUENCY (×1/2 OUTPUT) vs BIAS RESISTOR

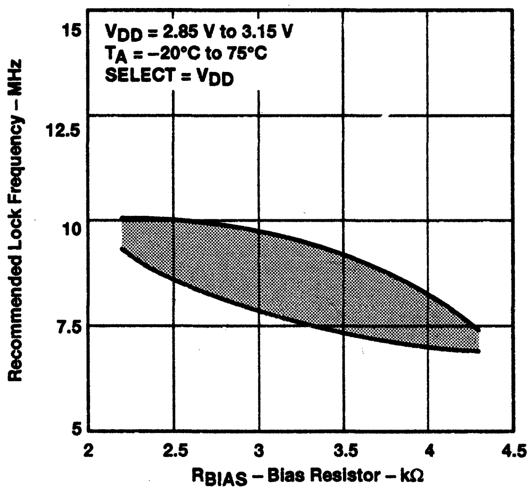


Figure 22

RECOMMENDED LOCK FREQUENCY (×1/2 OUTPUT) vs BIAS RESISTOR

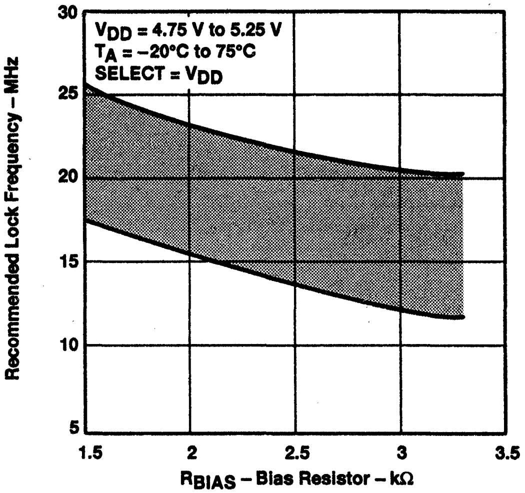


Figure 23

APPLICATION INFORMATION

gain of VCO and PFD

Figure 24 is a block diagaram of the PLL. The countdown N value depends on the input frequency and the desired VCO output frequency according to the system application requirements. The K_p and K_V values are obtained from the operating characteristics of the device as shown in Figure 24. K_p is defined from the phase detector V_{OL} and V_{OH} specifications and the equation shown in Figure 24(c). K_V is defined from Figures 8, 9, 10, and 11 as shown in Figure 24(c).

The parameters for the block diagram with the units are as follows:

- K_V : VCO gain (rad/s/V)
- K_p : PFD gain (V/rad)
- K_f : LPF gain (V/V)
- K_N : count down divider gain (1/N)

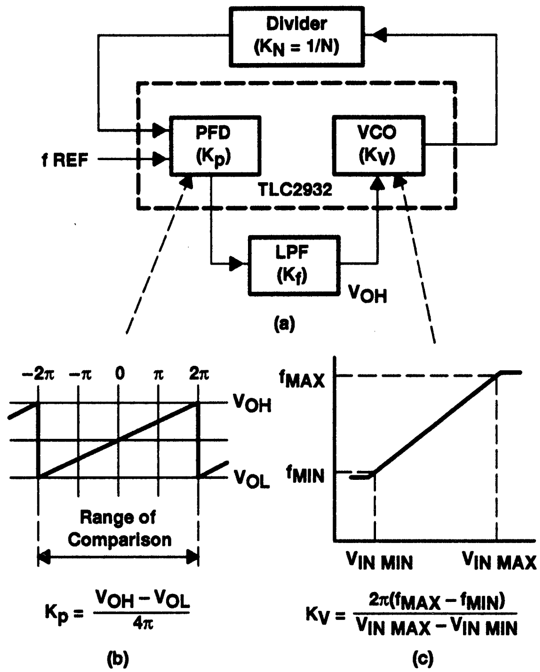


Figure 24. Example of a PLL Block Diagram

external counter

When a large N counter is required by the application, there is a possibility that the PLL response becomes slow due to the counter response delay time. In the case of a high frequency application, the counter delay time should be accounted for in the overall PLL design.

R_{BIAS}

The external bias resistor sets the VCO center frequency with 1/2 V_{DD} applied to the VCO IN terminal. However, for optimum temperature performance, a resistor value of 3.3 kΩ with a 3-V supply and a resistor value of 2.5 kΩ for a 5-V supply is recommended. For the most accurate results, a metal-film resistor is the better choice but a carbon-compositiion resistor can be used with excellent results also. A 0.22 μF capacitor should be connected from the BIAS terminal to ground as close to the device terminals as possible.

hold-in range

From the technical literature, the maximum hold-in range for an input frequency step for the three types of filter configurations shown in Figure 25 is as follows:

$$\Delta\omega_H \simeq 0.8 \left(K_p\right) \left(K_V\right) \left(K_f\,(\infty)\right)$$

Where

$K_f\,(\infty)$ = the filter transfer function value at $\omega = \infty$

APPLICATION INFORMATION

low-pass-filter (LPF) configurations

Many excellent references are available that include detailed design information about LPFs and should be consulted for additional information. Lag-lead filters or active filters are often used. Examples of LPFs are shown in Figure 25. When the active filter of Figure 25(c) is used, the reference should be applied to FIN-B because of the amplifier inversion. Also, in practical filter implementations, C_f is used as additional filtering at the VCO input. The value of C_f should be equal to or less than one tenth the value of C.

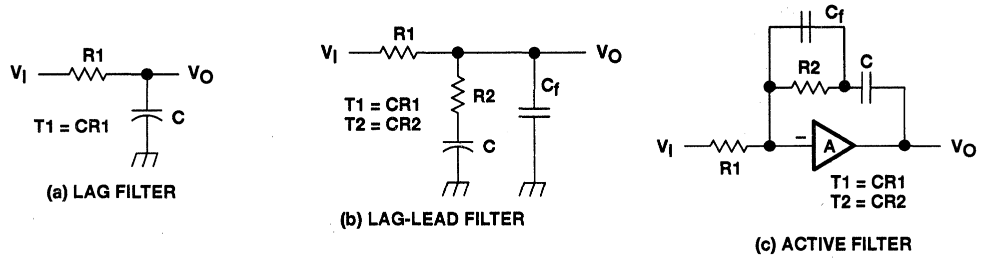


Figure 25. LPF Examples for PLL

the passive filter

The transfer function for the low-pass filter shown in Figure 25(b) is

$$\frac{V_O}{V_{IN}} = \frac{1 + s \cdot T2}{1 + s \cdot (T1 + T2)}$$

Where

$$T1 = R1 \cdot Cf \text{ and } T2 = R2 \cdot Cf$$

Using this filter makes the closed loop PLL system a second order type 1 system. The response curves of this system to a unit step are shown in Figure 27.

the active filter

When using the active integrator shown in Figure 25(c), the phase detector inputs must be reversed since the integrator adds an additional inversion. Therefore, the input reference frequency should be applied to the FIN-B terminal and the output of the VCO divider should be applied to the input reference terminal, FIN-A.

The transfer function for the active filter shown in Figure 25(c) is:

$$F(s) = \frac{1 + s \cdot R2 \cdot C}{s \cdot R1 \cdot C}$$

Using this filter makes the closed loop PLL system a second-order type 2 system. The response curves of this system to a unit step are shown in Figure 27.

basic design example

The following design example presupposes that the input reference frequency and the required frequency of the VCO are within the respective ranges of the device.

Assume the loop has to have a 100 µs settling time (t_S) with a countdown N = 8. Using the Type 1, second order response curves of Figure 26, a value of 4.5 radians is selected for $\omega_n t_S$ with a damping factor of 0.7. This selection gives a good combination for settling time, accuracy, and loop gain margin. The initial parameters are summarized in Table 5. The loop constants, K_V and K_p, are calculated from the data sheet specifications and Table 6 shows these values.

The natural loop frequency is calculated as follows:

Since

$$\omega_n t_S = 4.5$$

Then

$$\omega_n = \frac{4.5}{100\ \mu s} = 45 \text{ k-radians/sec}$$

Table 5. Design Parameters

PARAMETER	SYMBOL	VALUE	UNITS
Division factor	N	8	
Lockup time	t	100	µs
Radian value to selected lockup time	$\omega_n t$	4.5	rad
Damping factor	ζ	0.7	

Table 6. Device Specifications

PARAMETER	SYMBOL	VALUE	UNITS
VCO gain		76.6	Mrad/V/s
f_{MAX}		50	MHz
f_{MIN}	K_V	20	MHz
$V_{IN\ MAX}$		5	V
$V_{IN\ MIN}$		0.9	V
PFD gain	K_p	0.342357	V/rad

Table 7. Calculated Values

PARAMETER	SYMBOL	VALUE	UNITS
Natural angular frequency	ω_n	45000	rad/sec
$K = (K_V \bullet K_p)/N$		3.277	Mrad/sec
Lag-lead filter Calculated value Nearest standard value	R1	15870 16000	Ω
Calculated value Nearest standard value	R2	308 300	Ω
Selected value	C1	1	µF

APPLICATION INFORMATION

Using the low-pass filter in Figure 25(b) and divider ratio N, the transfer function for phase and frequency are shown in equations 1 and 2. Note that the transfer function for phase differs from the transfer function for frequency by only the divider value N. The difference arises from the fact that the feedback for phase is unity while the feedback for frequency is 1/N.

Hence, transfer function of Figure 24 (a) for phase is

$$\frac{\Phi 2(s)}{\Phi 1(s)} = \frac{K_p \cdot K_V}{N \cdot (T1 + T2)} \left[\frac{1 + s \cdot T2}{s^2 + s\left[1 + \frac{K_p \cdot K_V \cdot T2}{N \cdot (T1+T2)}\right] + \frac{K_p \cdot K_V}{N \cdot (T1+T2)}} \right] \tag{1}$$

and the transfer function for frequency is

$$\frac{F_{OUT(s)}}{F_{REF(s)}} = \frac{K_p \cdot K_V}{(T1 + T2)} \left[\frac{1 + s \cdot T2}{s^2 + s \cdot \left[1 + \frac{K_p \cdot K_V \cdot T2}{N \cdot (T1+T2)}\right] + \frac{K_p \cdot K_V}{N \cdot (T1+T2)}} \right] \tag{2}$$

The standard two pole denominator is $D = s^2 + 2\,\zeta\,\omega_n\,s + \omega_n{}^2$ and comparing the coefficients of the denominator of equation (1) and (2) with the standard two pole denominator gives the following results.

$$\omega_n = \sqrt{\frac{K_p \cdot K_V}{N \cdot (T1 + T2)}}$$

Solving for T1 + T2

$$T1 + T2 = \frac{K_p \cdot K_V}{N \cdot \omega_n{}^2} \tag{3}$$

and by using this value for T1 + T2 in equation (3) the damping factor is

$$\zeta = \frac{\omega_n}{2} \cdot \left(T2 + \frac{N}{K_p \cdot K_V} \right)$$

solving for T2

$$T2 = \frac{2\,\zeta}{\omega} - \frac{N}{K_p \cdot K_V}$$

then by substituting for T2 in equation (3)

$$T1 = \frac{K_V \cdot K_p}{N \cdot \omega_n{}^2} - \frac{2\,\zeta}{\omega_n} + \frac{N}{K_p \cdot K_V}$$

APPLICATION INFORMATION

From the circuit constants and the initial design parameters then

$$R2 = \left[\frac{2\,\zeta}{\omega_n} - \frac{N}{K_p \cdot K_V} \right] \frac{1}{C_f}$$

$$R1 = \left[\frac{K_p \cdot K_V}{{\omega_n}^2 \cdot N} - \frac{2\,\zeta}{\omega_n} + \frac{N}{K_p \cdot K_V} \right] \frac{1}{C_f}$$

The capacitor, C_f, is usually chosen between 1 µF and 0.1 µF to allow for reasonable resistor values and physical capacitor size. In this example, C_f is chosen to be 1 µF and the corresponding R1 and R2 calculated values are listed in Table 7.

APPLICATION INFORMATION

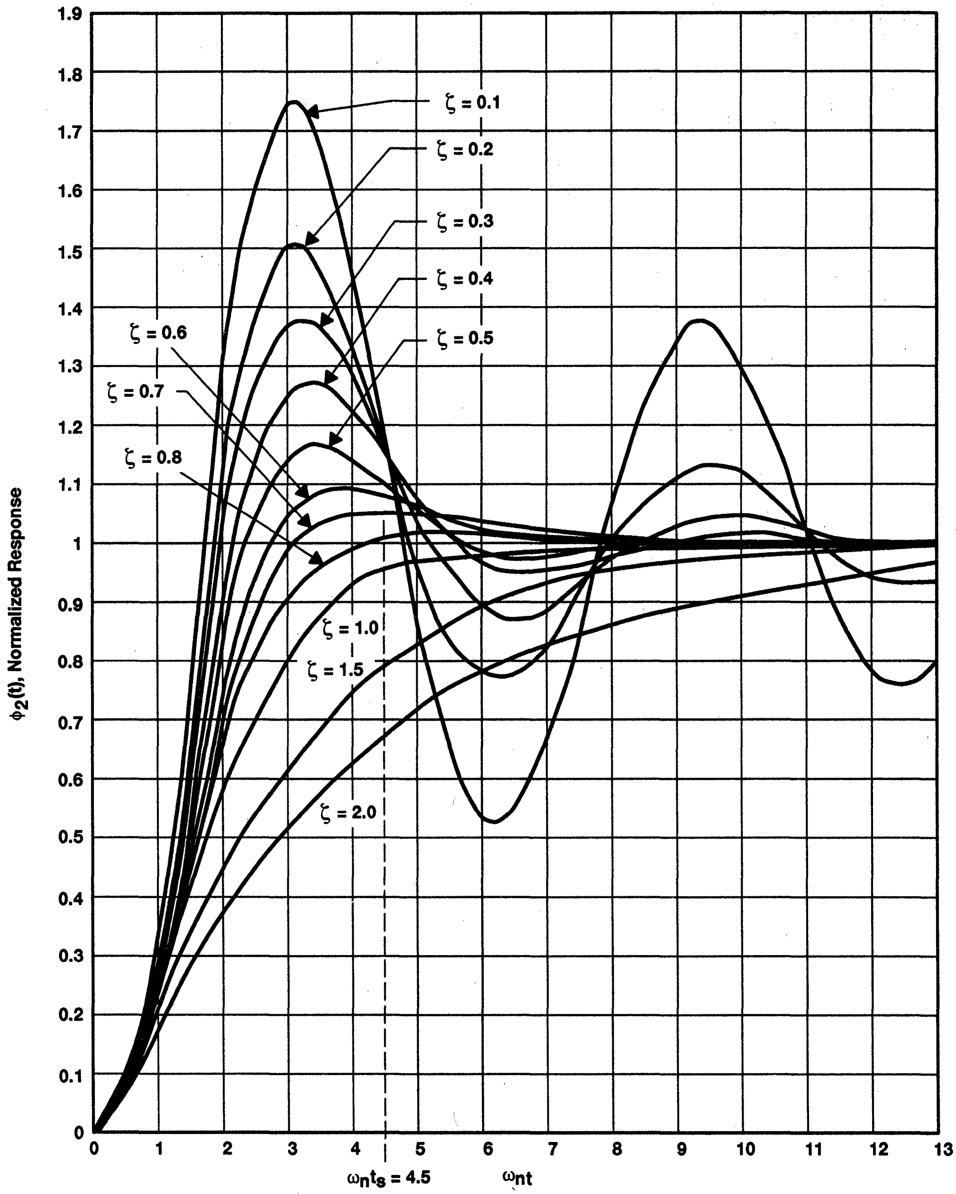


Figure 26. Type 1 Second Order Step Response

APPLICATION INFORMATION

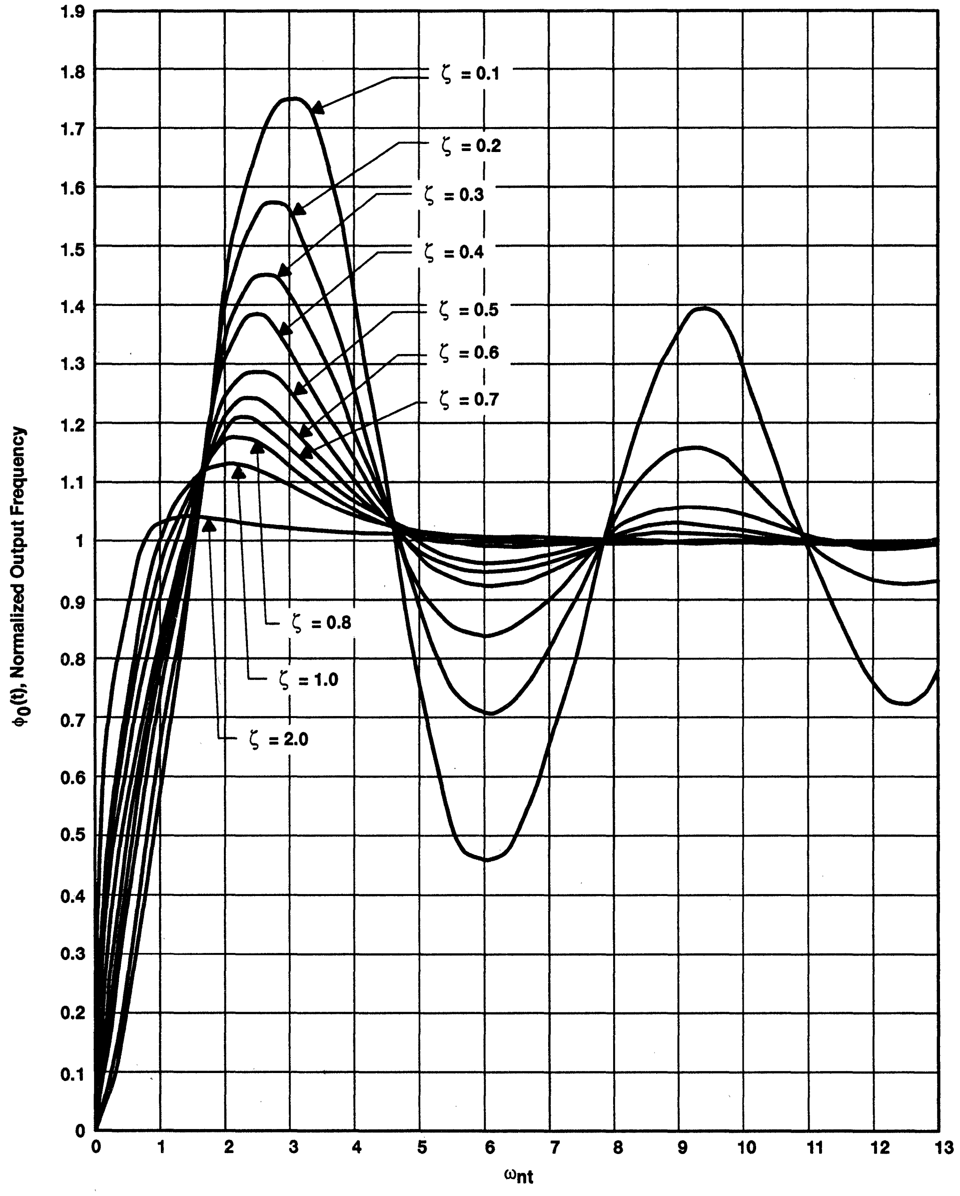
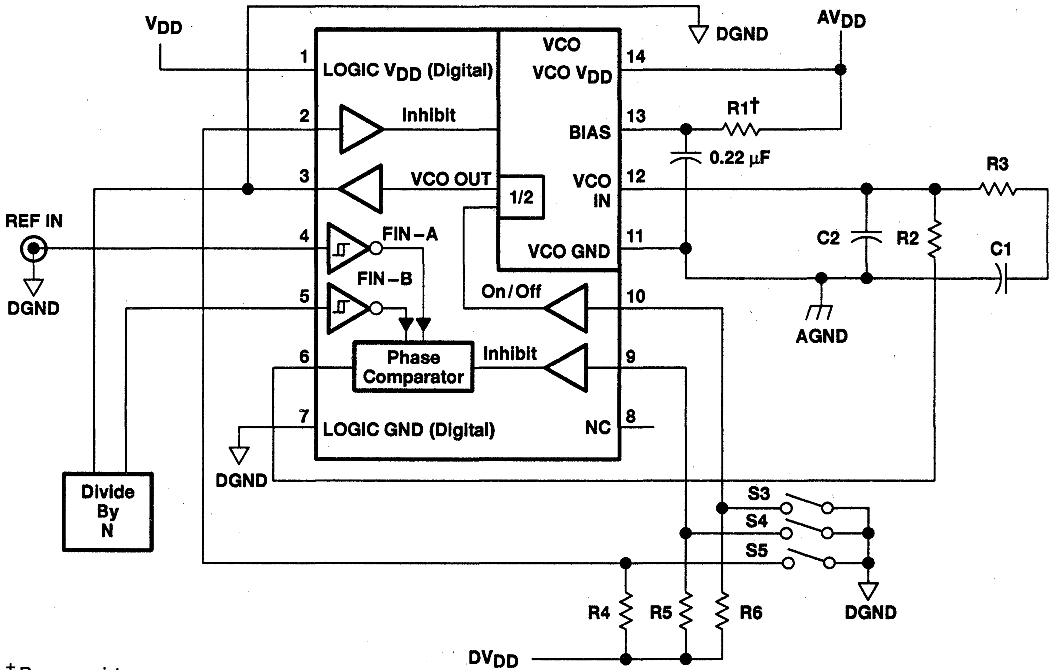


Figure 27. Type 2 Second Order Step Response

APPLICATION INFORMATION



† R_{BIAS} resistor

Figure 28. Evaluation and Operation Schematic

PCB layout considerations

The TLC2932I contains a high frequency analog oscillator; therefore, very careful breadboarding and printed-circuit-board (PCB) layout is required for evaluation.

The following design recommendations benefit the TLC2932I user:

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or RF PCB techniques should be used throughout the evaluation and production process.
- Wide ground leads or a ground plane should be used on the PCB layouts to minimize parasitic inductance and resistance. The ground plane is the better choice for noise reduction.
- LOGIC V_{DD} and VCO V_{DD} should be separate PCB traces and connected to the best filtered supply point available in the system to minimize supply cross-coupling.
- VCO V_{DD} to GND and LOGIC V_{DD} to GND should be decoupled with a 0.1-µF capacitor placed as close as possible to the appropriate device terminals.
- The no-connection (NC) terminal on the package should be connected to GND.

- **Analog Front-End Integrated Circuit for the 18-Bit Stereo Audio Sigma-Delta Analog-to-Digital Converter TLC320AD58C and Equivalent Analog-to-Digital Converters**
- **Single-Ended to Differential Signal Conversion**
- **Low Distortion, Low Noise**
  - **THD+N . . . –100-dB Typ**
  - **S/N . . . 108-dB Typ**
- **Adjustable Signal Gain**
- **5-V Single Supply Operation**
- **Internal Voltage Reference**
- **Operating Temperature . . . –20°C to 70°C**

NS PACKAGE
(TOP VIEW)

REF L1	1	20	REF R1
AV_{SS}	2	19	IN R+
IN L+	3	18	IN R–
IN L–	4	17	OUT R
OUT L	5	16	REF R
REF L	6	15	FLTR 1
FLTL 1	7	14	FLTR 2
FLTL 2	8	13	AOUT R–
AOUT L–	9	12	AOUT R+
AOUT L+	10	11	AV_{DD}

description

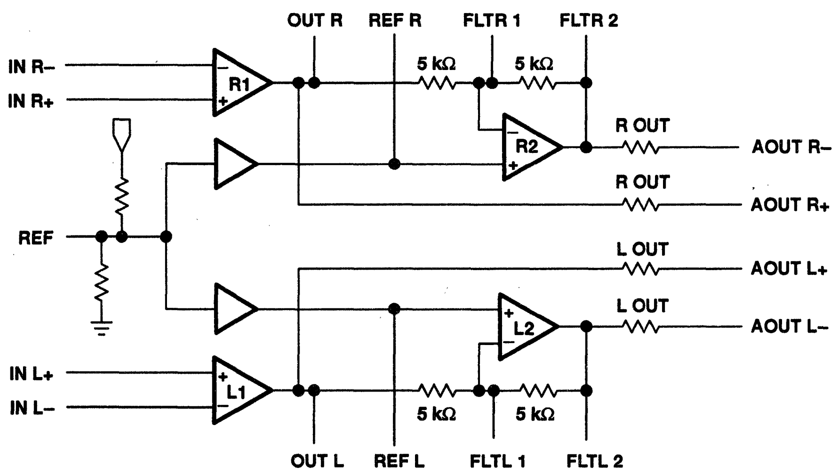
The TL32088 is an analog signal conditioning integrated circuit built using a proprietary Texas Instruments bipolar process. This device is used for the analog signal input stage of the 18-bit, stereo audio, sigma-delta, analog-to-digital converter (ADC) TLC320AD58C or equivalent converters. The TL32088 converts a single-ended audio signal to a differential signal with externally controlled gain for the input of a sigma-delta ADC, differential-analog signal input. The differential output can be connected to the TLC320AD58C directly. The TLC32088 is composed of high performance amplifiers that offer wide output swing with low distortion and low noise. The reference voltage for the internal amplifiers circuit is provided from an internal voltage reference circuit.

AVAILABLE OPTIONS

T_A	PACKAGE SMALL OUTLINE (NS)
–20°C to 70°C	TL32088INS

The TL32088 operates in a single 5-V supply high end audio system providing wide output swing while maintaining –100-dB THD+N and 108-dB SNR.

functional block diagram



PRODUCT PREVIEW

absolute maximum rating over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Differential input voltage, V_{ID} (see Note 2)	7 V
Input voltage range, V_I (any input) (see Notes 1 and 3)	–0.3 to V_{CC}
Output voltage, V_O	–0.3 to V_{CC}
Output current, I_O	20 mA
Duration of short-circuit current at or below 25°C (output shorted to GND)	unlimited
Continuous total dissipation, P_D ($T_A \le 25°C$) (see Note 4)	625 mW
Operating free-air temperature range, T_A	–20°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltage, are with respect to GND.
2. Differential voltage is at the noninverting input with respect to the inverting input.
3. All input voltage values must not exceed V_{CC}.
4. Derating factor above T_A = 25°C is 10 mW/°C.

PRODUCT PREVIEW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		5		V
Input voltage range, V_I (see Note 5)	1.1		3.9	V
Operating free-air temperature, T_A	–20		70	°C

NOTE 5: The output voltage is undetermined when the input voltage exceeds recommended input voltage range.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V (unless otherwise noted)

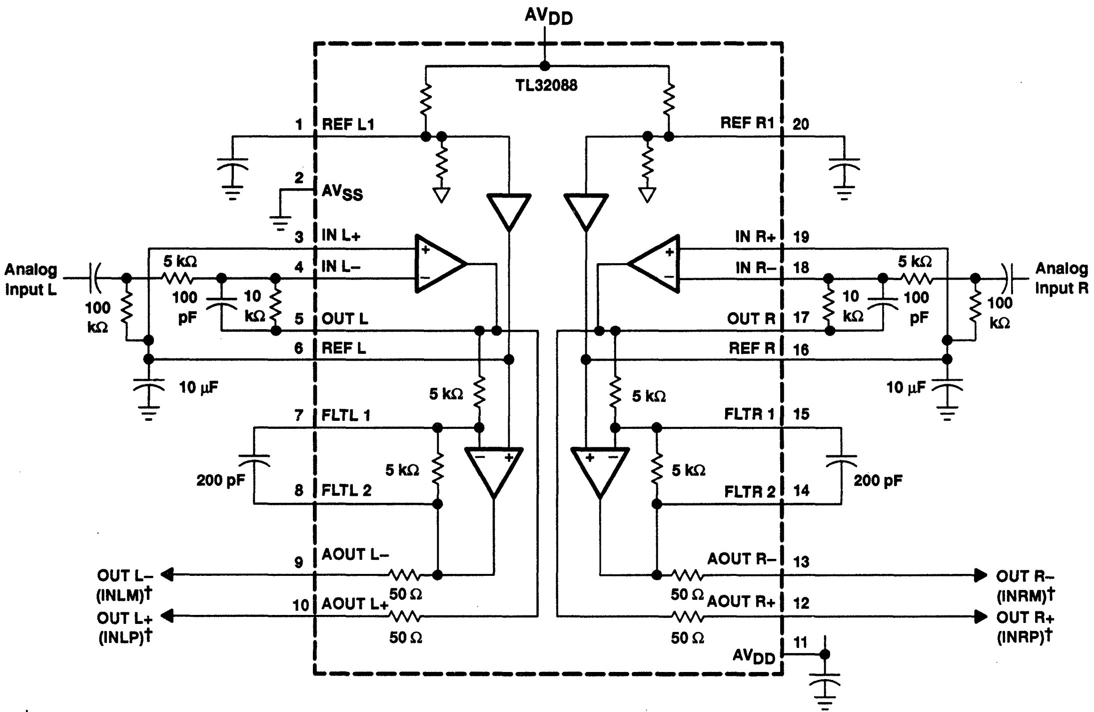
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 2.5 V, V_O = 2.5 V (AMP L1, R1)	T_A = 25°C		1		mV
			T_A = –20°C to 70°C		7.5		
I_{IO}	Input offset current	V_{IC} = 2.5 V, V_O = 2.5 V (AMP L1, R1)	T_A = 25°C		5		nA
			T_A = –20°C to 70°C		150		
I_{IB}	Input bias current	V_{IC} = 2.5 V, V_O = 2.5 V (AMP L1, R1)	T_A = 25°C		20		nA
			T_A = –20°C to 70°C				
V_{IC}	Common-mode input voltage	$V_O \le 7.5$ mV (AMP L1, R1)	T_A = 25°C	0.9		4.1	V
			T_A = –20°C to 70°C	1.1		3.9	
V_{OM+}	Maximum positive-peak output voltage		T_A = –20°C to 70°C	4.4			V
V_{OM-}	Maximum negative-peak output voltage		T_A = –20°C to 70°C			0.6	V
A_{vd}	Differential voltage amplification	$V_O = 2.5 V \pm 1 V$ (AMP L1, R1)	T_A = 25°C		60		dB
CMRR	Common-mode rejection ratio	$V_O = 2.5 V \pm 5 V$ (AMP L1, R1)	T_A = 25°C		85		dB
V_{ref}	Reference voltage		T_A = –20°C to 70°C	2.45	2.5	2.55	V
E_G	Gain error	See Note 6	T_A = –20°C to 70°C			±3%	
r_o	Output resistance		T_A = 25°C		50		Ω
I_{CC}	Supply current (both channels)	V_O = 2.5 V, No load	T_A = 25°C			15	mA
			T_A = –20°C to 70°C			18	

NOTE 6: Gain error is between OUT L and FLTL 1, OUT R and FLTR 1.

operating characteristics over recommended operating free-air temperature range, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate	A_V = 1, V_I = 2.5 V + 0.5 V (AMP L1, R1)		3		V/µs
B_1	Unity-gain bandwidth	AMP L1, R1		7		MHz
SNR	Signal-to-noise ratio (EIAJ)	A-Weight test circuit		108		dB
THD+N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 3.2 V, f = 1 kHz, BW = 10 Hz to 20 kHz test circuit		–100		dB

APPLICATION INFORMATION



† TLC320AD58C input terminals.

Figure 1. TL32088 to TLC320AD58C Connections

PRODUCT PREVIEW

- CMOS Technology
- 135-MHz Pipelined Architecture
- Available Clock Rate . . . 80, 110, 135 MHz
- Dual-Port Color RAM
  256 Words x 24 Bits
- Bit-Plane Read and Blink Masks
- EIA RS-343-A Compatible Outputs
- Functionally Interchangeable With Brooktree® Bt458
- Direct Interface to SMJ340xx Graphics Processors (110M)
- Direct Interface to TMS340XX Graphics Processors
- Standard Microprocessor Unit (MPU) Palette Interface
- Multiplexed-TTL Pixel Ports
- Triple Digital-to-Analog Converters (DACs)
- Dual-Port Overlay Registers . . . 4 × 24 Bits
- 5-V Power Supply
- Data Sheet Available†

description

The TLC34058 color-palette integrated circuit is specifically developed for high-resolution color graphics in such applications as CAE/CAD/CAM, image processing, and video reconstruction. The architecture provides for the display of 1280 × 1024 bit-mapped color graphics (up to eight bits per pixel resolution) with two bits of overlay information. The TLC34058 has a 256-word × 24-bit RAM used as a lookup table with three 8-bit, video, D/A converters.

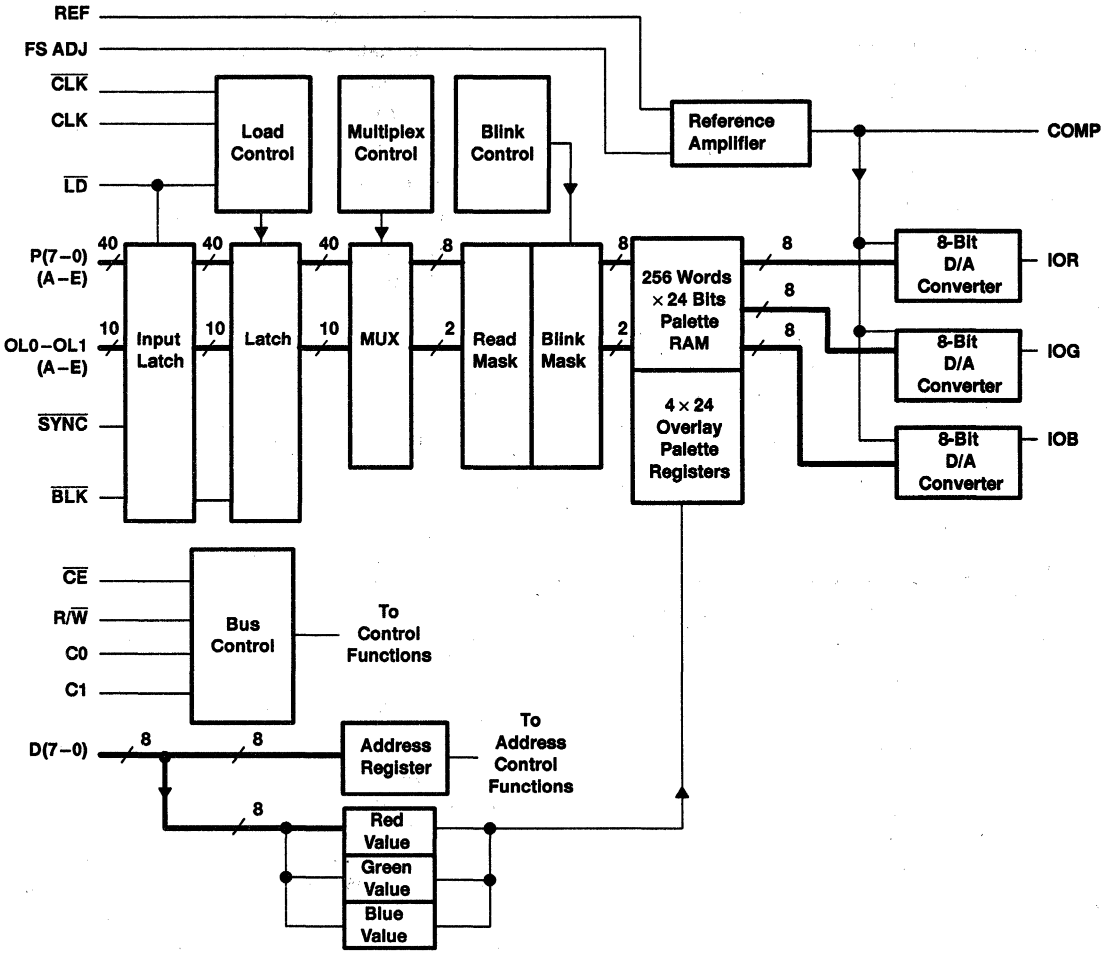
On-chip features such as high-speed pixel clock logic minimize costly ECL interface. Multiple pixel ports and internal multiplexing provide TTL-compatible interface (up to 32 MHz) to the frame buffer while maintaining sophisticated color graphic data rates (up to 135 MHz). Programmable blink rates, bit plane masking and blinking, color overlay capability, and a dual-port palette RAM are other key features. The TLC34058 generates red, green, and blue signals compatible with EIA RS-343-A and can drive 75-Ω coaxial cables terminated at each end without external buffering.

AVAILABLE OPTIONS

T_A	SPEED	DAC RESOLUTION	PACKAGE		
			CERAMIC GRID ARRAY (GA)	PLASTIC CHIP CARRIER (FN)	QUAD FLATPACK (HFG)
0°C to 70°C	80 MHz	8 Bits	–	TLC34058-80FN	–
	110 MHz	8 Bits	–	TLC34058-110FN	–
	135 MHz	8 Bits	–	TLC34058-135FN	–
–55°C to 125°C	110 MHz	8 Bits	TLC34058-110MGA	–	TLC34058-110MHFG

† For the complete data sheet, refer to the Graphics and Imaging Data Book (SLAD002).
Brooktree is a registered trademark of Brooktree Corporation.

functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

- **Versatile Multiplexing Interface Allows Lower Pixel Bus Rate**
- **High Level of Integration Provides Lower System Cost and Complexity**
- **Versatile Pixel Bus Interface Supports Little- and Big-Endian Data Formats**
- **Directly Interfaces to TMS34010/TMS34020 and Other Graphics Processors**
- **Single 8-Bit D/A Converters**
- **Low Cost Monochrome and Gray-Scale System**
- **Pin Compatible With TLC34075 and TLC34076**
- **135-, 170-, and 200-MHz Versions**
- **On-Chip Voltage Reference**
- **RS-343A-Compatible Outputs**
- **TTL-Compatible Inputs**
- **Standard MPU Interface**
- **On-Chip Clock Selection**
- **Directly Interfaces to Video RAM**
- **Supports Split Shift-Register Transfers**
- **TIGA™ Software-Standard Compatible**
- **CMOS Technology**
- **Data Manual Available†**

description

The TLC34074 video interface DAC (VID) is designed for monochrome and gray-scale graphics systems, providing lower system cost with a higher level of integration by incorporating all the high-speed timing, synchronizing, and multiplexing logic usually associated with graphics systems into one device, thus greatly reducing chip count. Since all high-speed signals (excluding the clock source) are contained on-chip, RF noise considerations are simplified. Maximum flexibility is provided through the pixel multiplexing scheme, which allows for 32-, 16-, 8-, and 4-bit pixel buses to be accommodated without any circuit modification. This enables the system to be easily reconfigured for varying amounts of available video RAM. Additionally, data can be split into 1, 2, 4, or 8-bit gray-scale.

The TLC34074 is also designed to be terminal compatible with the TLC34075 and TLC34076 video interface palettes. Therefore, a single graphics design can be configured into a color or black-and-white system by using either the TLC34075/076 or the TLC34074 to reduce the system cost and increase the resolution. Like the TLC34076, the TLC34074 can be programmed for little or big-endian data format for the pixel bus frame buffer interface.

The TLC34074 has an 8-bit video digital-to-analog converter (DAC) capable of directly driving a doubly terminated 75-Ω line. Sync generation can be incorporated onto the output channel when so enabled. Hsync and Vsync are fed through the device and optionally inverted to indicate screen resolution to the monitor. Bit stuffing logic repeats the intended gray-scale pattern to the least significant bits when the gray-scale is not 8 bits wide. This allows the 8-bit DAC to achieve full RS-343A output levels while maintaining uniform linearity for all codes.

AVAILABLE OPTIONS

T_A	SPEED	DAC RESOLUTION	PACKAGE PLASTIC CHIP CARRIER (FN)
0°C to 70°C	135 MHz	8 Bits	TLC34074-135FN
	170 MHz	8 Bits	TLC34074-170FN
	200 MHz	8 Bits	TLC34074-200FN

† For the complete data manual, refer to the Graphics and Imaging Data Book (SLAD002).
TIGA is a trademark of Texas Instruments Incorporated.

description (continued)

Clocking is provided through one of four inputs (3 TTL- and 1 ECL/TTL-compatible) and is software selectable. The video and shift-clock outputs provide a software-selected divide ratio of the chosen clock input.

The TLC34074 can be connected directly to the serial port of VRAM devices, eliminating the need for any discrete logic. Support for split shift-register transfers is also provided.

functional block diagram

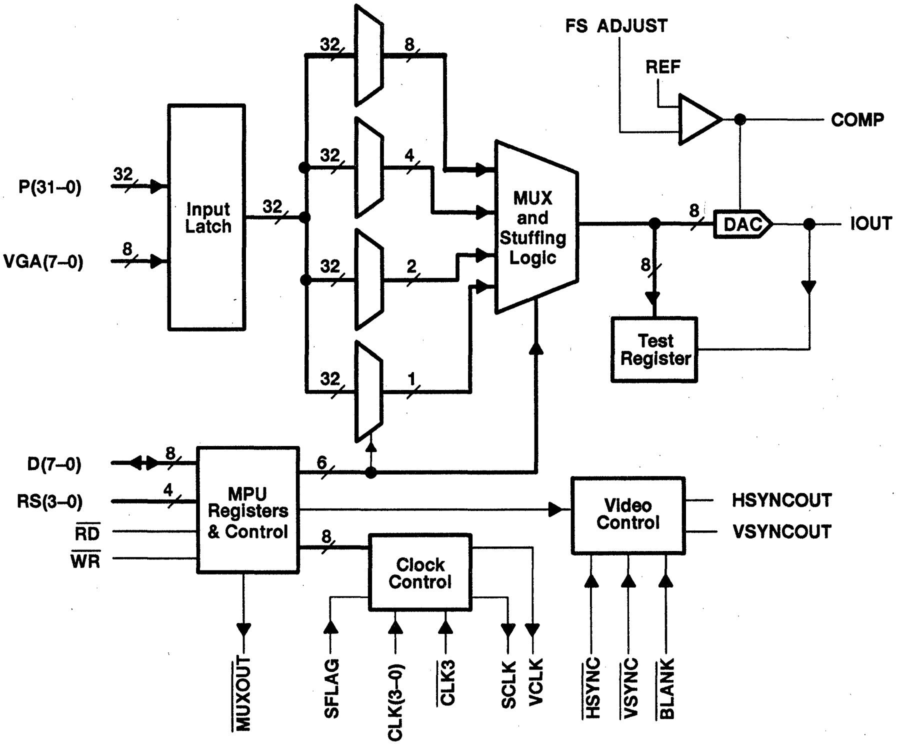


Figure 1. Functional Block Diagram

- **Versatile Multiplexing Interface Allows Lower Pixel Bus Rate**
- **High Level of Integration Provides Lower System Cost and Complexity**
- **Direct VGA Pass-Through Capability**
- **Directly Interfaces to TMS34010/TMS34020 and Other Graphics Processors**
- **Triple 8-Bit D/A Converters**
- **66-, 85-, 110, and 135-MHz Versions**
- **256-Word Color Palette RAM**
- **Palette Page Register**
- **On-Chip Voltage Reference**
- **RS-343A-Compatible Outputs**
- **TTL-Compatible Inputs**
- **Standard MPU Interface**
- **Pixel Word Mask**
- **On-Chip Clock Selection**
- **True Color (Direct Addressing) Mode**
- **Directly Interfaces to Video RAM**
- **Supports Split Shift Register Transfers**
- **Software Downward-Compatible With INMOS IMSG176/8 and Brooktree™ Bt476/8 Color Palettes**
- **TIGA™ Software-Standard Compatible**
- **CMOS Technology**
- **Data Manual Available†**

description

The TLC34075A video interface palette (VIP) is designed to provide lower system cost with a higher level of integration by incorporating all the high-speed timing, synchronizing, and multiplexing logic usually associated with graphics systems into one device, thus greatly reducing chip count. Since all high-speed signals (excluding the clock source) are contained on-chip, RF noise considerations are simplified. Maximum flexibility is provided through the pixel multiplexing scheme, which allows for 32-, 16-, 8-, and 4-bit pixel buses to be accommodated without any circuit modification. This enables the system to be easily reconfigured for varying amounts of available video RAM. Data can be split into 1-, 2-, 4-, or 8-bit planes. The TLC34075A is software-compatible with the INMOS IMSG176/8 and Brooktree Bt476/8 color palettes.

The TLC34075A features a separate VGA bus that allows data from the feature connector of most VGA-supported personal computers to be fed directly into the palette without the need for external data multiplexing. This allows a replacement graphics board to remain downward compatible by utilizing the existing graphics circuitry often located on the motherboard. The TLC34075A also provides a true-color mode in which 24 (3 by 8) bits of color information are transferred directly from the pixel port to the DACs. This mode of operation supplies an overlay function using the 8 remaining bits of the pixel bus.

The TLC34075A has a 256-by-24 color lookup table with triple, 8-bit video, D/A converters capable of directly driving a doubly terminated, 75-Ω line. Sync generation is incorporated on the green output channel. HSYNC and VSYNC are fed through the device and optionally inverted to indicate screen resolution to the monitor. A palette page register provides the additional bits of palette address when 1-, 2-, or 4-bit planes are used. This allows the screen colors to be changed with only one MPU write cycle.

Clocking is provided through one of four or five inputs (three TTL- and either one ECL- or two TTL-compatible) and is software selectable. The video and shift clock outputs provide a software-selected divide ratio of the chosen clock input.

The TLC34075A can be connected directly to the serial port of VRAM devices, eliminating the need for any discrete logic. Support for split shift-register transfers is also provided.

The TLC34075A is an optimized version of the original TLC34075 video interface palette. Because all of the critical speed paths have been strengthened on the device, a slightly higher supply current specification is required. The new specification also includes revised SCLK/VCLK timing and a clock-counter reset function.

† For the complete data manual, refer to the Graphics and Imaging Data Book (SLAD002).

AVAILABLE OPTIONS

T_A	SPEED	DAC RESOLUTION	PACKAGE PLASTIC CHIP CARRIER (FN)
0°C to 70°C	66 MHz	8 Bits	TLC34075-66AFN
	85 MHz	8 Bits	TLC34075-85AFN
	110 MHz	8 Bits	TLC34075-110AFN
	135 MHz	8 Bits	TLC34075-135AFN

functional block diagram

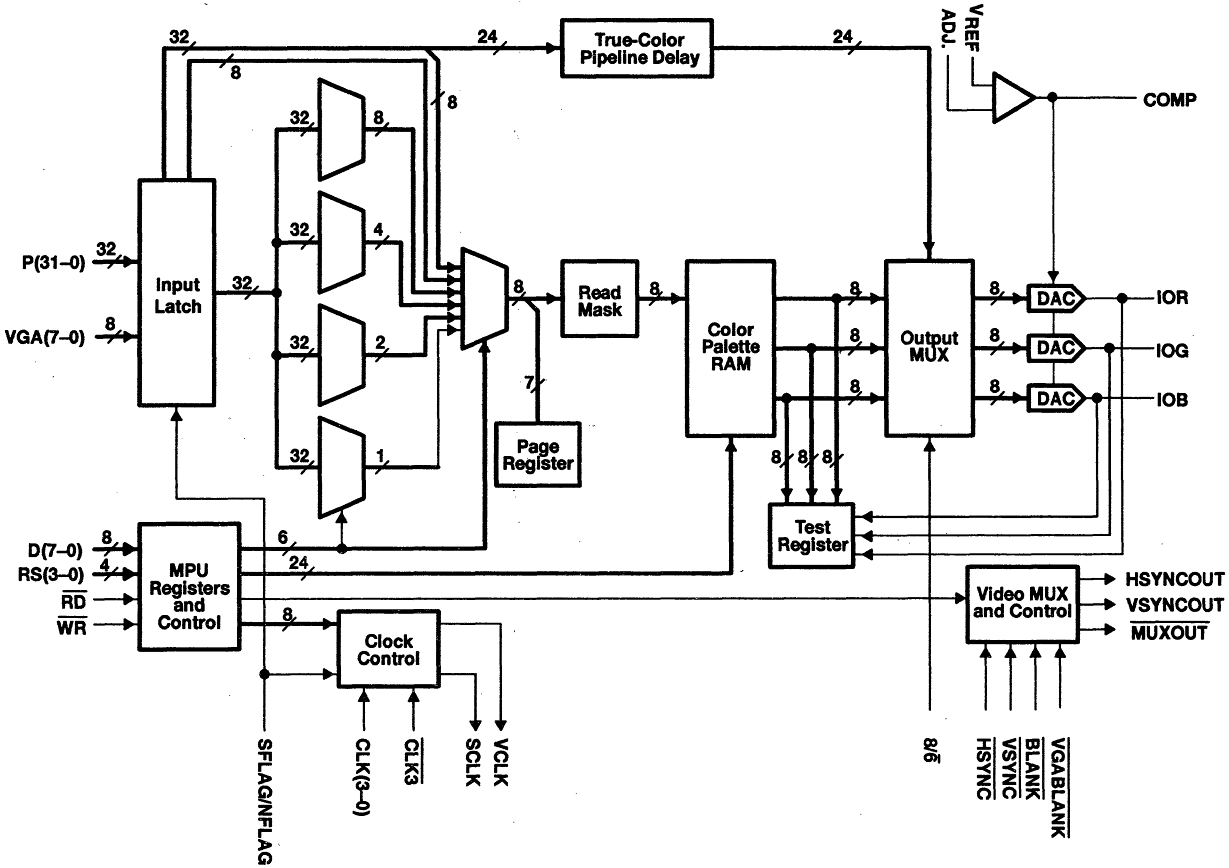


Figure 1. Functional Block Diagram

- CMOS Technology
- Versatile Multiplexing Interface Allows Lower Pixel Bus Rate
- High Level of Integration Provides Lower System Cost and Complexity
- Direct VGA Pass-Through Capability
- Versatile Pixel Bus Interface Supports Little- and Big-Endian Data Formats
- True-Color (Direct Addressing) Modes Support Various 24- and 16-Bit Formats
- XGA™-Format Compatible (5–6–5)
- TARGA™-Format Compatible (5–5–5)
- Directly Interfaces to TMS34010/TMS34020 and Other Graphics Processors
- Triple 8-Bit D/A Converters
- 85-, 110-, 135-, and 170- MHz Versions
- 256-Word Color Palette RAM
- Palette Page Register
- On-Chip Voltage Reference
- RS-343A-Compatible Outputs
- TTL-Compatible Inputs
- Standard MPU Interface
- Pixel Word Mask
- On-Chip Clock Selection
- Directly Interfaces to Video RAM
- Supports Split Shift-Register Transfers
- Software Downward-Compatible With INMOS IMSG176/8 and Brooktree™ BT476/8 Color Palettes
- TIGA™ Software-Standard Compatible
- Data Manual Available†

description

The TLC34076 video interface palette (VIP) is designed to provide lower system cost with a higher level of integration. The device incorporates all of the high-speed timing, synchronization, and multiplexing logic usually associated with graphics systems into one device, thus greatly reducing chip count. Since all high-speed signals (excluding the clock source) are contained on-chip, RF noise considerations are simplified. Maximum flexibility is provided through the pixel multiplexing scheme, which allows for 32-, 16-, 8-, and 4-bit pixel buses to be accommodated without any circuit modification. This enables the system to be easily reconfigured for varying amounts of available video RAM. Data can be split into 1-, 2-, 4-, or 8-bit planes. The TLC34076 is software-compatible with the IMSG176/8 and Brooktree BT476/8 color palettes.

The TLC34076 VIP is terminal-for-terminal compatible with the TLC34075 VIP but contains additional 24- and 16-bit true-color modes as well as the ability to select little- or big-endian data formats for the pixel bus frame-buffer interface.

The TLC34076 features a separate video graphics adapter (VGA) bus that allows data from the feature connector of most VGA-supported personal computers to be fed directly into the palette without the need for external data multiplexing. This allows a replacement graphics board to remain downward compatible by utilizing the existing graphics circuitry often located on the motherboard.

The 24- and 16-bit true-color modes that are provided allow bits of color information to be transferred directly from the pixel port to the digital-to-analog converters (DACs). Depending on which true-color mode is selected, an overlay function is provided using the remaining bits of the pixel bus. The 24-bit modes allow overlay with the eight remaining bits of the pixel bus, while the TARGA (5-5-5) 16-bit mode allows overlay with the one remaining bit of the divided pixel bus.

The TLC34076 has a 256-by-24 color-lookup table with triple, 8-bit video, D/A converters capable of directly driving a doubly terminated, 75-Ω line. Synchronization generation is incorporated on the green output channel. $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are fed through the device and optionally inverted to indicate screen resolution to the monitor. A palette page register provides the additional bits of palette address when 1-, 2-, or 4-bit planes are used. This allows the screen colors to be changed with only one MPU write cycle.

† For the complete data manual, refer to the Graphics and Imaging Data Book (SLAD002).

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Brooktree is a trademark of Brooktree Corporation.
TIGA is a trademark of Texas Instruments Incorporated.

description (continued)

Clocking is provided through one of four or five inputs (three TTL- and either one ECL- or two TTL-compatible) and is software selectable. The video and shift-clock outputs provide a software-selected divide ratio of the chosen clock input.

The TLC34076 can be connected directly to the serial port of VRAM devices, eliminating the need for any discrete logic. Support for split shift-register transfers is also provided.

AVAILABLE OPTIONS

T_A	SPEED	DAC RESOLUTION	PACKAGE	
			PLASTIC CHIP CARRIER (FN)	GRID ARRAY (GA)
0°C to 70°C	85 MHz	8 Bits	TLC34076-85FN	–
	110 MHz	8 Bits	TLC34076-110FN	–
	135 MHz	8 Bits	TLC34076-135FN	–
	170 MHz	8 Bits	TLC34076-170FN	–
–55°C to 125°C	135 MHz	8 Bits	–	TLC34076-135MGA

function block diagram

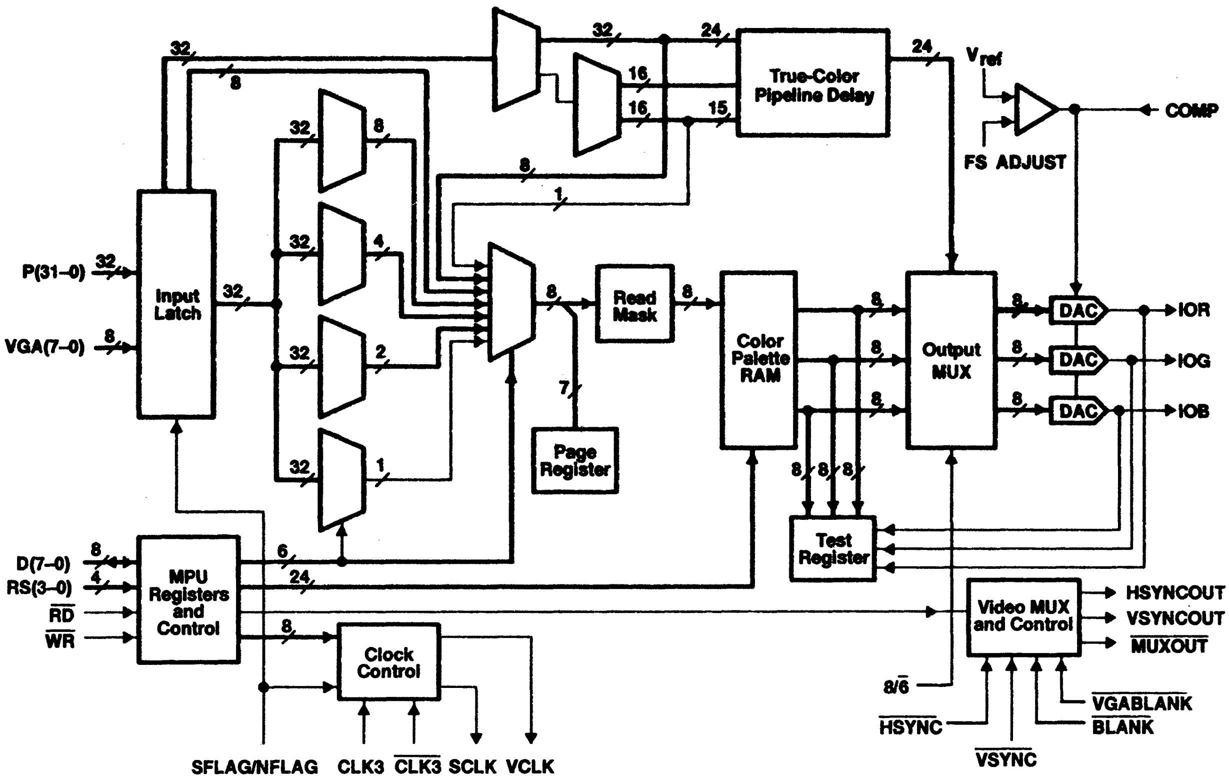

Figure 1. Functional Block Diagram

- Versatile Multiplexing Interface Allows Lower Pixel Bus Rate
- High Level of Integration Provides Lower System Cost and Complexity
- Direct VGA Pass-Through Capability
- True-Color (Direct Addressing) Modes Support Various 24- and 16-Bit Formats
- XGA™-Format Compatible (5-6-5)
- TARGA™-Format Compatible (5-5-5)
- Directly Interfaces to Most Graphics Processors
- Triple 8-Bit D/A Converters
- 110- and 135-MHz Versions
- 256-Word Color Palette RAM
- On-Chip Voltage Reference
- RS-343A-Compatible Outputs
- TTL-Compatible Inputs
- Standard MPU Interface
- Pixel Word Mask
- On-Chip Clock Selection
- Software Downward-Compatible With INMOS IMSG176/8 and BrookTree™ Bt476/8 Color Palettes
- TIGA™ Software-Standard Compatible
- CMOS Technology
- Data Manual Available†

description

The TLC34077 video interface palette (VIP) is designed to provide lower system cost with a higher level of integration by incorporating all the high-speed timing, synchronization, and multiplexing logic usually associated with graphics systems into one device, thus greatly reducing chip count. Since all high-speed signals (excluding the clock source) are contained on-chip, RF noise considerations are simplified. Maximum flexibility is provided through the pixel multiplexing scheme, which allows for 32-, 16-, and 8-bit pixel buses to be accommodated without any circuit modification. The TLC34077 is software compatible with the IMSG176/8 and Brooktree Bt476/8 color palettes.

The TLC34077 VIP is terminal-for-terminal compatible with the TLC34076 VIP, but with a reduced feature set optimized for cost-sensitive, high-performance, PC graphics applications. The TLC34077 is compatible with a variety of graphics processors, including the ATI 68800 *mach 32* series of graphics accelerators.

The TLC34077 features a separate VGA bus that allows data from the feature connector of most VGA-supported personal computers to be fed directly into the palette without the need for external data multiplexing. This allows a replacement graphics board to remain downward compatible by utilizing the existing graphics circuitry often located on the motherboard.

The 24- and 16-bit true-color modes that are provided allow bits of color information to be transferred directly from the pixel port to the DACs.

The TLC34077 has a 256-by-24 color-lookup table with triple, 8-bit video, D/A converters capable of directly driving a doubly terminated, 75-Ω line. Synchronization generation is incorporated on the green output channel.

Clocking is provided through one of two TTL-compatible inputs and is software selectable. The video clock output provides a software-selected divide ratio of the chosen clock input.

AVAILABLE OPTIONS

T_A	SPEED	DAC RESOLUTION	PACKAGE
			PLASTIC CHIP CARRIER (FN)
0°C to 70°C	110 MHz	8 Bits	TLC34077-110FN
	135 MHz	8 Bits	TLC34077-135FN

† For the complete data manual, refer to the Graphics and Imaging Data Book (SLAD002).

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Brooktree is a trademark of Brooktree Corporation.
TIGA is a trademark of Texas Instruments Incorporated.

functional block diagram

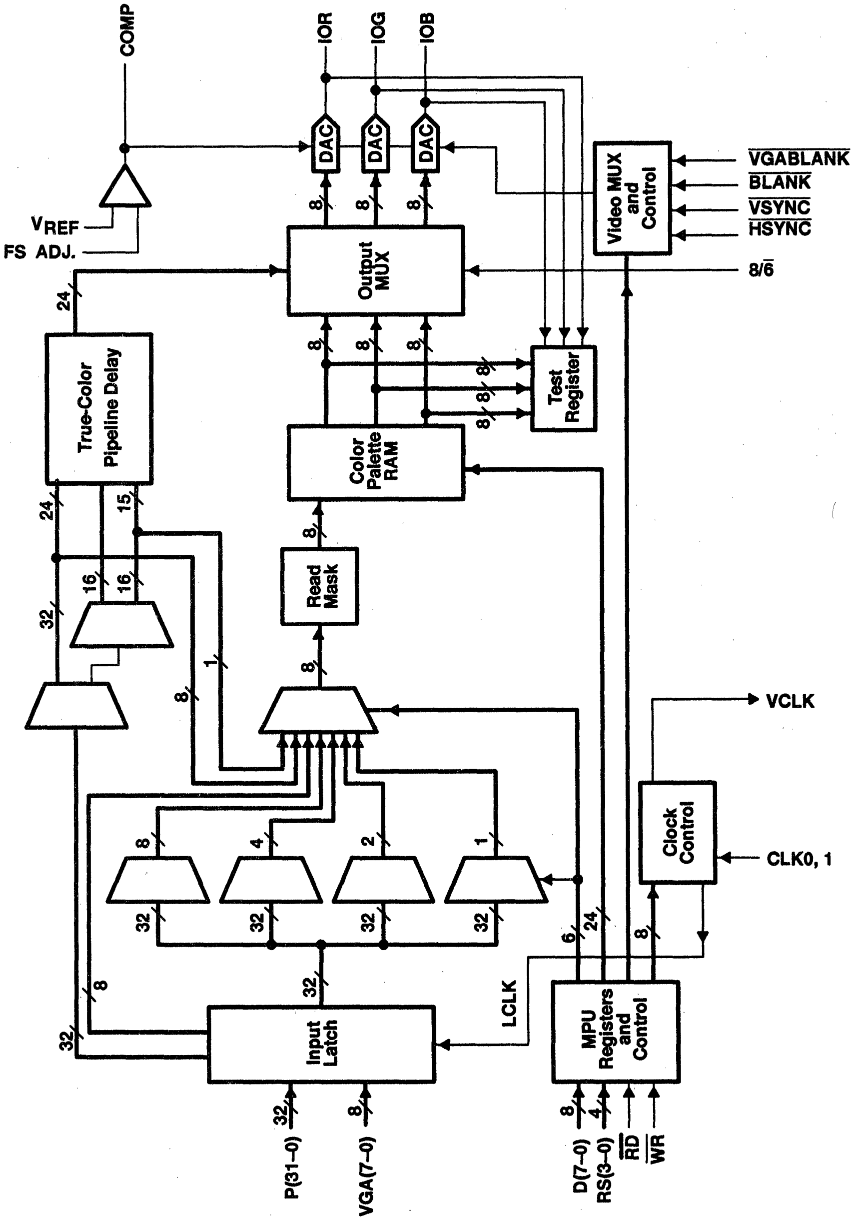

Figure 1. Functional Block Diagram

TEXAS INSTRUMENTS
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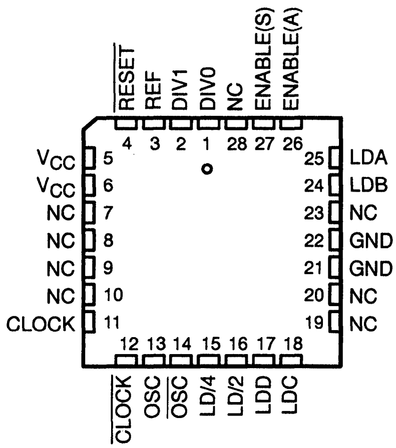
- **135-MHz Operation**
- **Differential ECL Clock Generation**
- **Divide by 3, 4, 5, or 8 of the Clock**
- **Divide by 2 and 4 of the Load**
- **Resets Pipeline Delay of the TLC34058**
- **1.235-V Voltage Reference Output**
- **5-V Single Power-Supply Operation**
- **28-Pin PLCC (FN) Package**
- **Low Power Consumption . . . 400 mW Max**
- **Designed to Be Interchangeable With Brooktree™ Bt438**
- **Data Sheet Available†**

FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TVP2002 is a clock driver for the Texas Instruments TLC34058 and functionally equivalent color palettes. It interfaces to a 10 KH-ECL oscillator operating from a single 5-V supply 'to the TLC34058, generating the necessary clock and control signals.

The clock output may be divided by 3, 4, 5, or 8 to generate the load signal. The load signal is also divided by 2 and 4 for clocking video timing logic, for example. A second load signal may be synchronously or asynchronously controlled to enable starting and stopping of the VRAM clock.

The TVP2002 also optionally configures the pipeline delay of the TLC34058 to a fixed-pipeline delay. An on-chip 1.235-V reference is provided and may be used to provide the reference voltage for the color palette.

AVAILABLE OPTIONS

T_A	PACKAGE
	PLASTIC CHIP CARRIER (FN)
0°C to 70°C	TVP2002FN

† For the complete data sheet, refer to the Graphics and Imaging Data Book (SLAD002).
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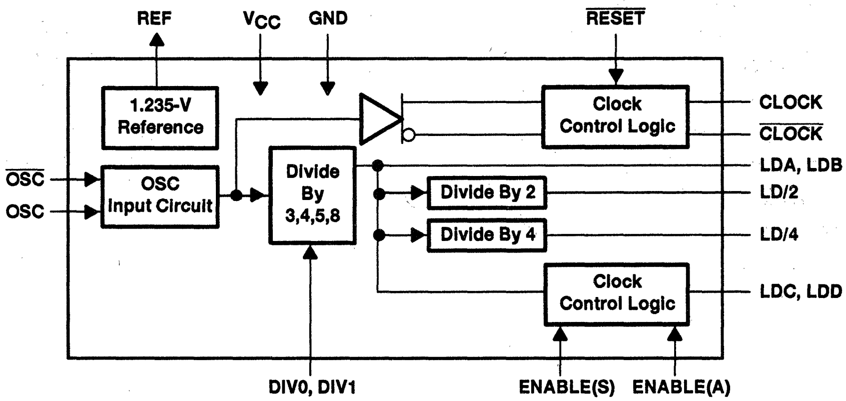
functional block diagram



- Second-Generation Video Interface Palette
- Supports System Resolutions of:
  - 1600 × 1280 × 1, 2, 4, 8, 16 Bits/Pixel at 60-Hz Refresh Rate
  - 1280 × 1024 × 1, 2, 4, 8, 16 Bits/Pixel at 60-Hz and 72-Hz Refresh Rates
  - 1024 × 768 × 1, 2, 4, 8, 16, 24 Bits/Pixel at 60-Hz and 72-Hz Refresh Rates
  - Lower Resolutions
- Direct-Color Modes:
  - 24-Bit/Pixel with 8-Bit Overlay
  - 16-Bit/Pixel (5, 6, 5) XGA™ Configuration
  - 16-Bit/Pixel (6, 6, 4) Configuration
  - 15-Bit/Pixel With 1-Bit Overlay (5, 5, 5, 1) TARGA™ Configuration
  - 12-Bit/Pixel With 4-Bit Overlay (4, 4, 4, 4)
- True-Color Modes:
  - 24-Bit/Pixel With Gamma Correction
  - 16-Bit/Pixel (5, 6, 5) XGA Configuration With Gamma Correction
  - 16-Bit/Pixel (6, 6, 4) Configuration with Gamma Correction
  - 15-Bit/Pixel (5, 5, 5) TARGA Configuration With Gamma Correction
  - 12-Bit/Pixel (4, 4, 4) With Gamma Correction
- RCLK/SCLK/LCLK Data Latching Allows Flexible Control of VRAM Timing
- Direct Interfacing to Video RAM
- Supports Split Shift-Register Transfers
- 64-Bit Wide Pixel Bus
- On-Chip Hardware Cursor:
  - 64 × 64 × 2 Cursor (XGA Functionally Compatible)
  - Full-Window Crosshair
  - Dual-Cursor Mode
- 85-, 110-, 135- and 170-MHz Versions
- Supports Overscan For Creation of Custom Screen Borders
- Versatile Pixel Bus Interface Supports Little- and Big-Endian Data Formats
- Windowed Overlay, VGA Capability
- Color-Keyed Switching of Direct Color and Overlay
- On-Chip Clock Selection
- Internal Frequency Doubler
- Triple 8-Bit D/A Converters
- Analog Output Comparators
- Triple 256 × 8 Color Palette RAMs
- RS-343A-Compatible Outputs
- Direct VGA Pass-Through Capability
- Palette-Page Register
- Horizontal Zooming Capability
- Software Downward Compatible With IMSG176/8 and Bt476/8
- Directly Interfaces to Graphics Processors
- CMOS Technology
- Data Manual Available†

description

The TVP3010 palette is an advanced video interface palette (VIP) from Texas Instruments implemented in the EPIC™ 0.8-micron CMOS process. Maximum flexibility is provided by the pixel multiplexing scheme. The scheme accommodates 64-, 32-, 16-, 8-, and 4-bit pixel buses without any circuit modification. This enables the system to be easily reconfigured for varying amounts of available video RAM. The device supports selection of little- or big-endian data format for the pixel-bus/frame-buffer interface. Data can be split into 1-, 2-, 4-, or 8-bit planes for pseudo-color mode or split into 12-, 16- or 24-bit true-color and direct-color modes. For the 24-bit direct color modes, an 8-bit overlay plane is available. The 16-bit direct- and true-color modes can be configured to IBM™ XGA (5, 6, 5), TARGA (5, 5, 5, 1), or (6, 6, 4) as another existing format. An additional 12-bit mode (4, 4, 4, 4) is supported with 4 bits for each color and overlay. An on-chip, IBM XGA-compatible hardware cursor is incorporated so that further increases in graphics system performance are possible. The device is also software compatible with the IMSG176/8 and Bt476/8 color palettes.

† For the complete data manual, refer to the Graphics and Imaging Data Book (SLAD002).

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IBM is a trademark of International Business Machines Corporation.

description (continued)

An internal frequency doubler is incorporated, allowing convenient and cost-effective clock source alternatives to be utilized. An auxiliary windowing function and a pixel-port-select function are provided so that overlay or VGA graphics can be displayed on top of direct color inside or outside a specified auxiliary window. Color-keyed switching of direct color and overlay is also supported.

Clocking is provided through one of five TTL inputs, CLK0–CLK4, and is software selectable. Additionally, CLK1/CLK2 and CLK3/CLK4 can be selected as differential ECL clock sources. The video, shift clock, and reference clock outputs provide a software-selected divide ratio of the chosen clock input. The reference clock can optionally be provided as an output on CLK3, and a data latch clock can optionally be input on CLK4.

The TVP3010 has three 256-by-8 color lookup tables with triple, 8-bit video, digital-to-analog converters (DACs) capable of directly driving a doubly terminated 75-Ω line. The lookup tables are designed with a dual-ported RAM architecture that enables ultra-high speed operation. Sync generation is incorporated on the green output channel. Horizontal sync and vertical sync are fed through the device and optionally inverted to indicate screen resolution to the monitor. A palette-page register provides the additional bits of palette address when 1-, 2-, or 4-bit planes are used. This allows the screen colors to be changed with only one microprocessor interface unit (MPU) write cycle.

The device features a separate VGA bus that allows data from the feature connector of most VGA-supported personal computers to be fed directly into the palette without the need for external data multiplexing. This allows a replacement graphics board to remain downward compatible by utilizing the existing graphics circuitry often located on the motherboard.

The TVP3010 VIP is highly system integrated. It can be connected to the serial port of VRAM devices without external buffer logic and connected to many graphics engines directly. The split shift-register transfer function, which is supported by VRAM, is also supported by the TVP3010.

The system-integration concept is carried to manufacturing test and field diagnosis. To support these, several highly integrated test functions have been designed to enable simplified testing of the palette, the graphics board, and the graphics system.

The 32-bit TVP3010 is terminal compatible with the TLC3407X VIP, allowing convenient performance upgrades when using devices in the TI Video Interface Palette family.

AVAILABLE OPTIONS

T_A	SPEED	DAC RESOLUTION	PACKAGE	
			PLASTIC CHIP CARRIER (FN)	GRID ARRAY (GA)
0°C to 70°C	85 MHz	8 Bits	TVP3010-85FN	–
	110 MHz	8 Bits	TVP3010-110FN	–
	135 MHz	8 Bits	TVP3010-135FN	–
	170 MHz	8 Bits	TVP3010-170FN	–
–55°C to 125°C	135 MHz	8 Bits	–	TVP3010-135MGA

functional block diagram

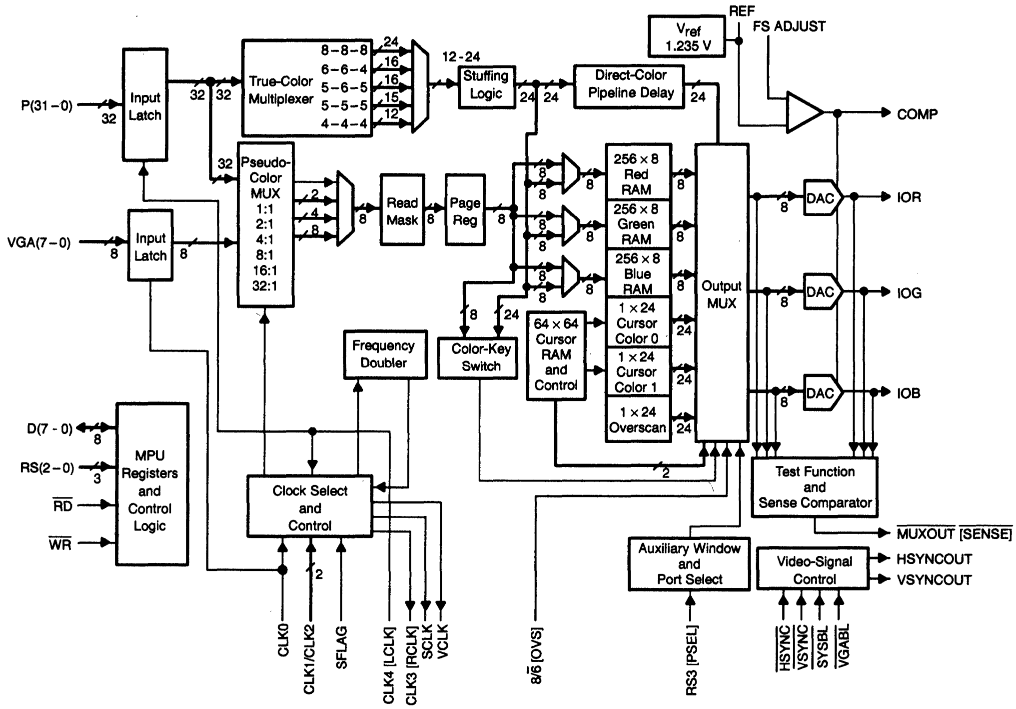

Figure 1. Functional Block Diagram

- **Second-Generation Video Interface Palette**
- **Supports System Resolutions of:**
  - **1600 × 1280 × 1, 2, 4, 8, 16, 24 Bits/Pixel at 60-Hz and 72-Hz Refresh Rate**
  - **1280 × 1024 × 1, 2, 4, 8, 16, 24 Bits/Pixel at 60-Hz and 72-Hz Refresh Rate**
  - **1024 × 768 × 1, 2, 4, 8, 16, 24 Bits/Pixel at 60-Hz and 72-Hz Refresh Rate**
  - **And lower resolutions**
- **Direct-Color Modes:**
  - **24-Bit/Pixel With 8-Bit Overlay**
  - **16-Bit/Pixel (5, 6, 5) XGA® Configuration**
  - **16-Bit/Pixel (6, 6, 4) Configuration**
  - **15-Bit/Pixel With 1-Bit Overlay (5, 5, 5, 1) TARGA Configuration**
  - **12-Bit/Pixel With 4-Bit Overlay (4, 4, 4, 4)**
- **True-Color Modes:**
  - **24-Bit/Pixel With Gamma Correction**
  - **16-Bit/Pixel (5, 6, 5) XGA Configuration With Gamma Correction**
  - **16-Bit/Pixel (6, 6, 4) Configuration With Gamma Correction**
  - **15-Bit/Pixel (5, 5, 5) TARGA® Configuration With Gamma Correction**
  - **12-Bit/Pixel (4, 4, 4) With Gamma Correction**
- **RCLK/SCLK/LCLK Data Latching Allows Flexible Control of VRAM Timing**
- **Direct Interfacing to Video RAM**
- **Supports Split Shift-Register Transfers**
- **64-Bit-Wide Pixel Bus**
- **On-Chip Hardware Cursor:**
  - **64 × 64 × 2 Cursor (XGA Functionally Compatible)**
  - **Full-Window Crosshair**
  - **Dual-Cursor Mode**
- **135-, 170-, and 200-MHz Versions**
- **Supports Overscan for Creation of Custom Screen Borders**
- **Versatile Pixel Bus Interface Supports Little- and Big-Endian Data Formats**
- **Windowed Overlay, VGA Capability**
- **Color-Keyed Switching of Direct Color and Overlay**
- **On-Chip Clock Selection**
- **Internal Frequency Doubler**
- **Triple 8-Bit D/A Converters**
- **Analog-Output Comparators**
- **Triple 256 × 8 Color Palette RAMs**
- **RS-343A-Compatible Outputs**
- **Direct VGA Pass-Through Capability**
- **Palette-Page Register**
- **Horizontal Zooming Capability**
- **Software Downward Compatible With IMSG176/8 and Bt476/8**
- **Directly Interfaces to Graphics Processors**
- **CMOS Technology**
- **Data Manual Available†**

description

The TVP3020 viewpoint palette is an advanced video interface palette (VIP) from Texas Instruments implemented in EPIC™ 0.8-micron CMOS process. Maximum flexibility is provided by the pixel multiplexing scheme. The scheme accommodates 64-, 32-, 16-, 8-, and 4-bit pixel buses without any circuit modification. This enables the system to be easily reconfigured for varying amounts of available video RAM. The device supports selection of little- or big-endian data format for the pixel-bus-frame buffer interface. Data can be split into 1-, 2-, 4-, or 8-bit planes for pseudo-color mode or split into 12-, 16- or 24-bit true-color and direct-color modes. For the 24-bit direct color modes, an 8-bit overlay plane is available. The 16-bit direct- and true-color modes can be configured to IBM XGA® (5, 6, 5), TARGA® (5, 5, 5, 1), or (6, 6, 4) as another existing format. An additional 12-bit mode (4, 4, 4, 4) is supported with 4 bits for each color and overlay. An on-chip, IBM XGA-compatible hardware cursor is incorporated so that further increases in graphics system performance are possible. The device is also software compatible with the IMSG176/8 and Bt476/8 color palettes.

† For the complete data manual, refer to the Graphics and Imaging Data Book (SLAD002).

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TARGA is a trademark of Truevision Incorporated.

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description (continued)

An internal frequency doubler is incorporated, allowing convenient and cost-effective clock source alternatives to be utilized.

An auxiliary windowing function and a pixel-port-select function are provided so that overlay or VGA graphics can be displayed on top of direct color inside or outside a specified auxiliary window. Color-keyed switching of direct color and overlay is also supported.

Clocking is provided through one of three inputs (two TTL- and one ECL/TTL-compatible) and is software selectable. The video clock, shift clock, and reference clock outputs provide a software-selected divide ratio of the chosen clock input.

The TVP3020 has three 256-by-8 color lookup tables with triple, 8-bit video, digital-to-analog converters (DACs) capable of directly driving a doubly terminated, 75-Ω line. The lookup tables are designed with a dual-ported RAM architecture that enables ultra-high speed operation. Sync generation is incorporated on the green output channel. Horizontal sync (HSYNC) and vertical sync (VSYNC) are fed through the device and optionally inverted to indicate screen resolution to the monitor. A palette-page register provides the additional bits of the palette address when 1-, 2-, or 4-bit planes are used. This allows the screen colors to be changed with only one microprocessor interface unit (MPU) write cycle.

The device features a separate VGA bus that allows data from the feature connector of most VGA-supported personal computers to be fed directly into the palette without the need for external data multiplexing. This allows a replacement graphics board to remain downward compatible by utilizing the existing graphics circuitry often located on the motherboard.

The viewpoint VIP is highly system integrated. It can be connected to the serial port of VRAM devices without external buffer logic and connected to many graphics engines directly. The split shift-register transfer function, which is supported by VRAM, is also supported by the TVP3020.

The system-integration concept is carried to manufacturing test and field diagnosis. To support these, several highly integrated test functions have been designed to enable simplified testing of the palette, the graphics board, and the graphics system.

AVAILABLE OPTIONS

T_A	SPEED	DAC RESOLUTION	PACKAGE	
			FLAT PACK (MDN)	FLAT PACK (PCE)
0°C to 70°C	135 MHz	8 Bits	–	TVP3020–135PCE
	170 MHz	8 Bits	–	TVP3020–170PCE
	200 MHz	8 Bits	TVP3020–200MDN	–

functional block diagram

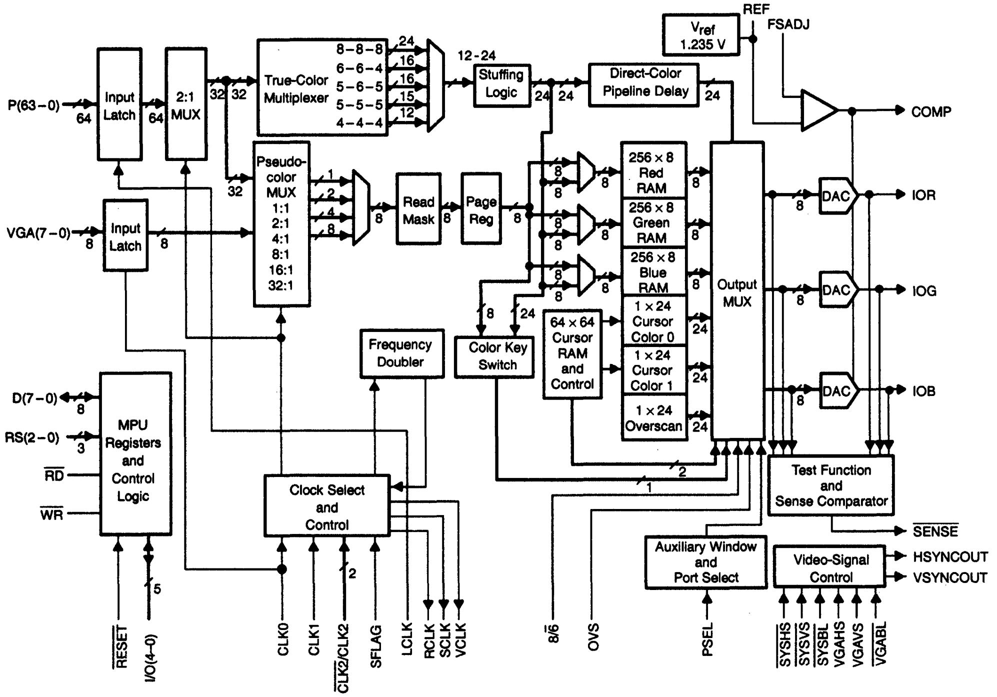

Figure 1. Functional Block Diagram

- 64-Bit Wide Pixel Bus
- Compatible With the S3 Vision964™ and 86C928
- Brooktree BT485 Register Map Emulation
- Supports System Resolutions of:
  - 1600 × 1280 × 1-, 2-, 4-, 8-, 16-, 24-Bits/Pixel at 60-Hz, 72, and 76-Hz Refresh Rate
  - 1536 × 1152 × 1-, 2-, 4-, 8-, 16-, 24-Bits/Pixel at 60-Hz and 72-Hz and Higher Refresh Rates
  - 1280 × 1024 × 1-, 2-, 4-, 8-, 16-, 24-Bits/Pixel at 60-Hz and 72-Hz and Higher Refresh Rates
  - 1024 × 768 × 1-, 2-, 4-, 8-, 16-, 24-Bits/Pixel at 60-Hz and 72-Hz and Higher Refresh Rates
  - And lower resolutions
- Direct-Color Modes:
  - 24-Bit/Pixel with 8-Bit Overlay
  - 16-Bit/Pixel (5, 6, 5) XGA™ Configuration
  - 16-Bit/Pixel (6, 6, 4) Configuration
  - 15-Bit/Pixel With 1-Bit Overlay (5, 5, 5, 1) TARGA™ Configuration
  - 12-Bit/Pixel With 4-Bit Overlay (4, 4, 4, 4)
- True-Color Modes:
  - 24-Bit/Pixel With Gamma Correction
  - 16-Bit/Pixel (5, 6, 5) XGA Configuration With Gamma Correction
  - 16-Bit/Pixel (6, 6, 4) Configuration with Gamma Correction
  - 15-Bit/Pixel (5, 5, 5) TARGA Configuration With Gamma Correction
  - 12-Bit/Pixel (4, 4, 4) With Gamma Correction
- RCLK/SCLK/LCLK Data Latching Allows Flexible Control of VRAM Timing
- Direct Interfacing to Video RAM
- Supports Split Shift-Register Transfers
- 135-, 170-, and 200-MHz Versions
- Integrated Pixel Clock and Memory Clocks Phase-Locked Loops (PLL)
- On-Chip Hardware Cursor:
  - 64 × 64 × 2 Cursor (XGA Functionally Compatible)
  - Full-Window Crosshair
  - Dual-Cursor Mode
- On-Chip Clock Selection
- Supports Overscan For Creation of Custom Screen Borders
- Versatile Pixel Bus Interface Supports Little- and Big-Endian Data Formats
- Windowed Overlay, VGA Capability
- Color-Keyed Switching of Direct Color and Overlay
- Horizontal Zooming Capability
- Triple 8-Bit D/A Converters
- Analog-Output Comparators
- Triple 256 × 8 Color Palette RAMs
- RS-343A-Compatible Outputs
- Direct VGA Pass-Through Capability
- Palette-Page Register
- Software Downward Compatible With IMSG176/8 and Bt476/8
- CMOS Technology
- Data Manual Available†

description

The TVP3025 is an advanced video interface palette (VIP) from Texas Instruments implemented in EPIC™ 0.8-micron CMOS process. The TVP3025 is a superset of the 64-bit TVP3020 VIP with the addition of Brooktree Bt485 register map emulation and frequency synthesis phase-locked loops (PLLs). The BT485 register emulation mode allows the device to be software compatible with many graphics controllers, including the S3 Vision964™ and 86C928 VRAM-based graphics accelerators. This new 64-bit device provides an effective migration path from lower performance graphics systems which utilize previous generation 32-bit color palettes.

† For the complete data manual, refer to the Graphics and Imaging Data Book (SLAD002).

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XGA is a trademark of International Business Machines Corporation.
TARGA is a trademark of Truevision Incorporated.
Vision964 is a trademark of S3 Corporation.

description (continued)

The TVP3025 is a functional superset of the TVP3020 and features the same 64-bit programmable pixel bus interface. Data can be split into 1-, 2-, 4-, or 8-bit planes for pseudo-color mode or split into 12-, 16- or 24-bit true-color and direct-color modes. For the 24-bit direct color modes, an 8-bit overlay plane is available. The 16-bit direct- and true-color modes can be configured to IBM XGA (5, 6, 5), TARGA (5, 5, 5, 1), or (6, 6, 4) as another existing format.

An additional 12-bit mode (4, 4, 4, 4) is supported with 4 bits for each color and overlay. All color modes support selection of little or big endian data format for the pixel bus. Additionally, the device is also software compatible with the IMSG176/8 and Bt476/8 color palettes.

Clocking is provided through one of four inputs (two TTL- and one ECL/TTL-compatible) or two crystal oscillator inputs, and is software selectable. The video, shift clock, and reference clock outputs provide a software-selected divide ratio of the chosen clock input. Two fully programmable PLLs for pixel clock and memory clock functions are provided, as well as a simple frequency doubler for dramatic improvements in graphics system cost and integration. A third loop clock PLL is incorporated making pixel data latch timing much simpler than with other existing color palettes.

Like the TVP3020, the TVP3025 also integrates a complete, IBM XGA-compatible hardware cursor on chip, making significant graphics performance enhancements possible. Additionally, auxiliary windowing, port-select and color-keyed switching functions are provided, giving the user several efficient means of producing graphical overlays on direct-color backgrounds.

The TVP3025 has three 256-by-8 color lookup tables with triple, 8-bit video, digital-to-analog converters (DACs) capable of directly driving a doubly terminated, 75-Ω line. The lookup tables are designed with a dual-ported RAM architecture that enables ultra-high speed operation. Sync generation is incorporated on the green output channel. Horizontal sync (HSYNC) and vertical sync (VSYNC) are fed through the device and optionally inverted to indicate screen resolution to the monitor. A palette-page register is available to provide the additional bits of palette address when 1-, 2-, or 4-bit planes are used. This allows the screen colors to be changed with only one microprocessor interface unit (MPU) write cycle.

The device features a separate VGA bus that allows data from the feature connector of most VGA-supported personal computers to be fed directly into the palette without the need for external data multiplexing. The separate bus also is useful in graphics accelerator applications, allowing efficient VGA and text mode support.

The TVP3025 is highly system integrated. It can be connected to the serial port of VRAM devices without external buffer logic and connected to many graphics engines directly. It also supports the split shift-register transfer function, which is common to many industry standard VRAM devices.

The system-integration concept is carried to manufacturing test and field diagnosis. To support these, several highly integrated test functions have been designed to enable simplified testing of the palette and the entire graphics system.

AVAILABLE OPTIONS

T_A	SPEED	DAC RESOLUTION	PACKAGE	
			FLAT PACK (MDN)	FLAT PACK (PCE)
0°C to 70°C	135 MHz	8 Bits	–	TVP3025–135PCE
	170 MHz	8 Bits	–	TVP3025–170PCE
	200 MHz	8 Bits	TVP3025–200MDN	–

functional block diagram

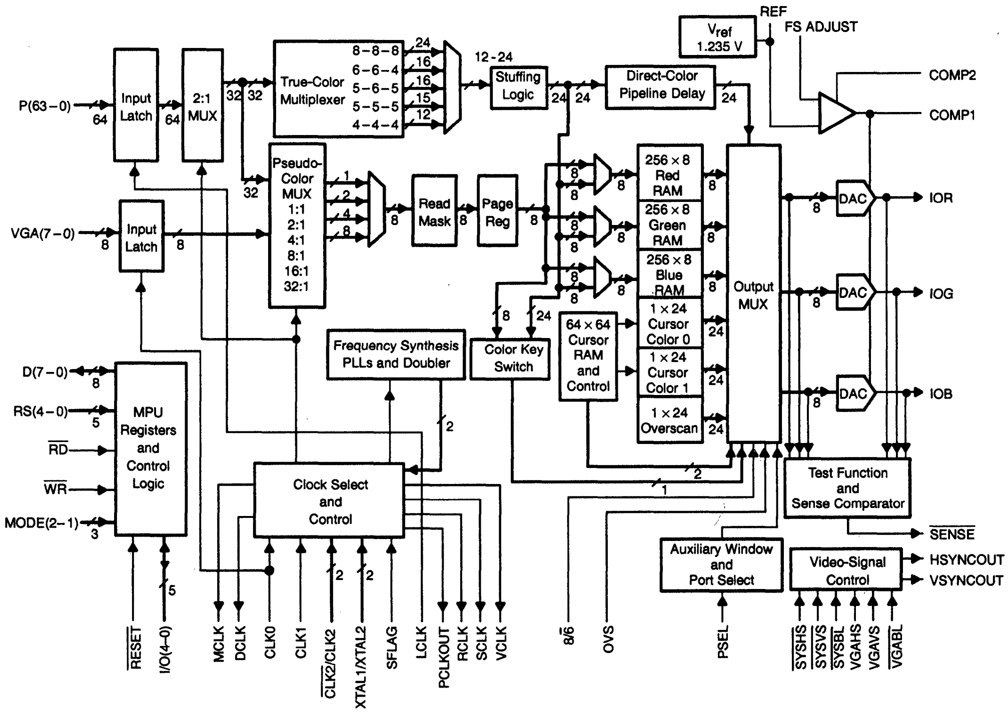

Figure 1. Functional Block Diagram

- Supports System Resolutions up to 1600 × 1280 at 76-Hz Refresh Rate
- Supports Color Depths of 4-, 8-, 16-, 24-, and 32-Bit/Pixel
- Versatile Direct-Color Modes:
  - 24-Bit/Pixel with 8-Bit Overlay (O, R, G, B)
  - 24-Bit/Pixel (R, G, B)
  - 16-Bit/Pixel (5, 6, 5) XGA™ Configuration
  - 16-Bit/Pixel (6, 6, 4) Configuration
  - 15-Bit/Pixel With 1-Bit Overlay (1, 5, 5, 5) TARGA™ Configuration
  - 12-Bit/Pixel With 4-Bit Overlay (4, 4, 4, 4)
- True-Color Gamma Correction
- Supports Packed Pixel Formats for 24-Bit/Pixel Using a 32- or 64-Bit/Pixel Bus
- 50% Duty Cycle Reference Clock for Higher Screen Refresh Rates in Packed-24 Modes
- Programmable Frequency Synthesis Phase-Locked Loops (PLL) for Dot Clock and Memory Clock
- Loop Clock PLL Compensates for System Delay and Ensures Reliable Data Latching
- Versatile Pixel Bus Interface Supports Little- and Big-Endian Data Formats
- 135-, 175-, and 220-MHz Versions
- On-Chip Hardware Cursor, 64 × 64 × 2 Cursor (XGA and X-Window™ Functionally Compatible)
- Direct Interfacing to Video RAM
- Supports Overscan For Creation of Custom Screen Borders
- Color-Keyed Switching of Direct Color and and True Color or Overlay
- Hardware Port Select Switching Between Direct Color and True Color or Overlay
- Triple 8-Bit D/A Converters
- Analog-Output Comparators for Monitor Detection
- RS-343A-Compatible Outputs
- Direct VGA Pass-Through Capability
- Palette-Page Register
- Horizontal Zooming Capability
- CMOS Technology
- Data Manual Available†

description

The TVP3026 is an advanced video interface palette (VIP) from Texas Instruments implemented in EPIC™ 0.8-micron CMOS process. The TVP3026 is a 64-bit VIP that supports packed-24 modes enabling 24-bit true color and high resolution at the same time without excessive amounts of frame buffer memory. For example, a 24-bit true color display with 1280 x 1024 resolution may be packed into 4 megabytes of VRAM. A PLL-generated, 50% duty cycle reference clock is output in the packed-24 modes, maximizing VRAM cycle time and screen refresh rate.

The TVP3026 supports all of the pixel formats of the TVP3020 VIP. Data can be split into 4- or 8-bit planes for pseudo-color mode or split into 12-, 16- or 24-bit true-color and direct-color modes. For the 24-bit direct color modes, an 8-bit overlay plane is available. The 16-bit direct- and true-color modes can be configured to IBM™ XGA (5, 6, 5), TARGA (1, 5, 5, 5), or (6, 6, 4) as another existing format. An additional 12-bit mode (4, 4, 4, 4) is supported with 4 bits for each color and overlay. All color modes support selection of little- or big-endian data format for the pixel bus. Additionally, the device is also software compatible with the IMSG176/8 and Bt476/8 color palettes.

Two fully programmable PLLs for pixel clock and memory clock functions are provided, as well as a simple frequency doubler for dramatic improvements in graphics system cost and integration. A third loop clock PLL is incorporated, making pixel data latch timing much simpler than with other existing color palettes. In addition, four digital clock inputs (two TTL- and two ECL/TTL-compatible) can be used and are software selectable. The video clock provides a software-selected divide ratio of the chosen pixel clock. The shift clock output can be used directly as the VRAM shift clock. The reference clock output is driven by the loop clock PLL and provides a timing reference to the graphics accelerator.

† For the complete data manual, refer to the Graphics and Imaging Data Book (SLAD002).

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X-Window is a trademark of the Massachusetts Institute of Technology

description (continued)

Like the TVP3020, the TVP3026 also integrates a complete, IBM XGA-compatible hardware cursor on chip, making significant graphics performance enhancements possible. Additionally, hardware port select and color-keyed switching functions allow the user several options for producing graphical overlays on direct-color backgrounds.

The TVP3026 has three 256-by-8 color lookup tables with triple, 8-bit video, digital-to-analog converters (DACs) capable of directly driving a doubly terminated, 75-Ω line. The lookup tables are designed with a dual-port RAM architecture that enables ultra-high speed operation. Sync generation is incorporated on the green output channel. Horizontal sync (HSYNC) and vertical sync (VSYNC) are pipeline delayed through the device and optionally inverted to indicate screen resolution to the monitor. A palette-page register is available to select from multiple color maps in RAM when 4 bit planes are used. This allows the screen colors to be changed with only one microprocessor write cycle.

The device features a separate VGA bus that supports the integrated VGA modes in graphics accelerator applications, allowing efficient support for VGA graphics and text modes. The separate bus also is useful for accepting data from the feature connector of most VGA-supported personal computers, without the need for external data multiplexing.

The TVP3026 is highly system integrated. It can be connected to the serial port of VRAM devices without external buffer logic and connected to many graphics engines directly. It also supports the split shift-register transfer function, which is common to many industry standard VRAM devices.

The system-integration concept is even carried further to manufacturing test and field diagnosis. To support these, several highly integrated test functions have been designed to enable simplified testing of the palette and the entire graphics system.

AVAILABLE OPTIONS

T_A	SPEED	DAC RESOLUTION	PACKAGE FLAT PACK (PCE)
0°C to 70°C	135 MHz	8 Bits	TVP3026–135PCE
	175 MHz	8 Bits	TVP3026–175PCE
	220 MHz	8 Bits	TVP3026–220PCE

functional block diagram

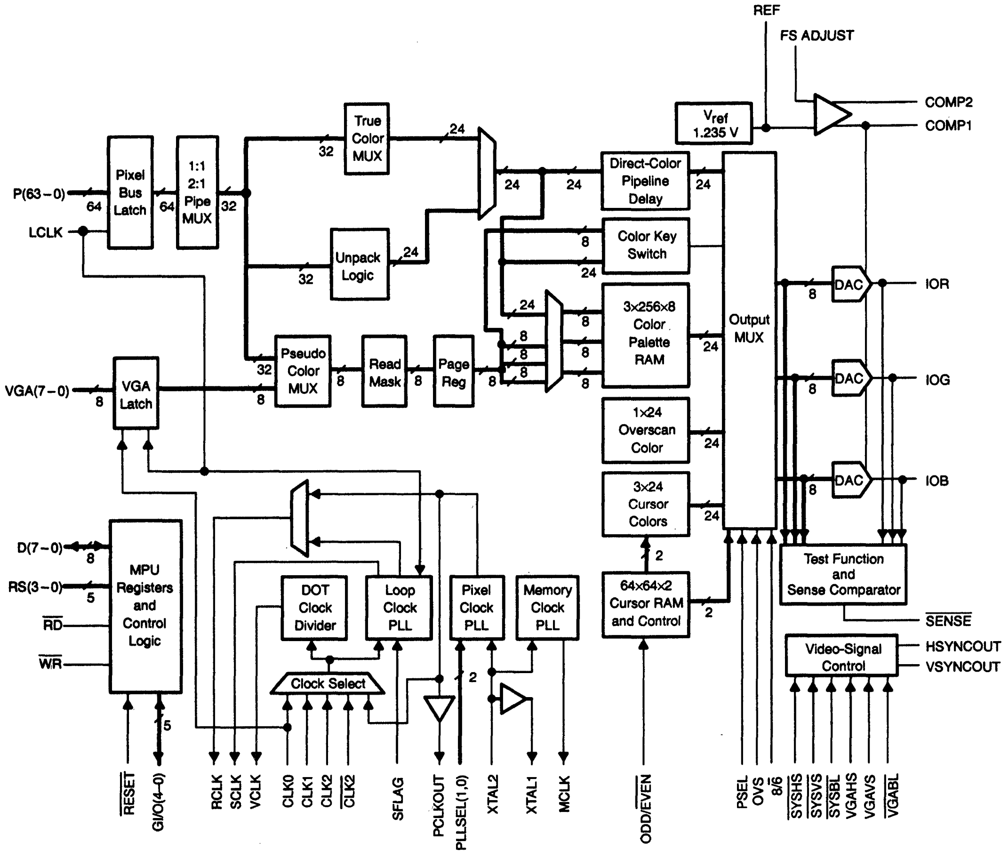

Figure 1. Functional Block Diagram

- Supports System Resolutions up to 1600 × 1280 at 76-Hz Refresh Rate
- Supports Color Depths of 4-, 8-, 16-, 24-, and 32-Bit/Pixel
- 64-Bit-Wide Pixel Bus
- Versatile Direct-Color Modes:
  - 24-Bit/Pixel with 8-Bit Overlay (O, R, G, B)
  - 24-Bit/Pixel (R, G, B)
  - 16-Bit/Pixel (5, 6, 5) XGA® Configuration
  - 16-Bit/Pixel (6, 6, 4) Configuration
  - 15-Bit/Pixel With 1-Bit Overlay (1, 5, 5, 5) TARGA® Configuration
  - 12-Bit/Pixel With 4-Bit Overlay (4, 4, 4, 4)
- True-Color Gamma Correction
- Supports Packed Pixel Formats for 24-Bit/Pixel Using a 32- or 64-Bit/Pixel Bus
- 50% Duty Cycle Reference Clock for Higher Screen Refresh Rates in Packed-24 Modes
- Programmable Frequency Synthesis Phase-Locked Loops (PLLs) for Dot Clock and Memory Clock
- Loop Clock PLL Compensates for System Delay and Ensures Reliable Data Latching
- Versatile Pixel Bus Interface Supports Little- and Big-Endian Data Formats
- 135-, 175-, and 220-MHz Versions
- On-Chip Hardware Cursor, 64 × 64 × 2 Cursor (XGA and X-Windows Functionally Compatible)
- Direct Interfacing to Video RAM
- Supports Overscan For Creation of Custom Screen Borders
- Color-Keyed Switching of Direct Color and and True Color or Overlay
- Hardware Port Select Switching Between Direct Color and True Color or Overlay
- Triple 8-Bit D/A Converters
- Analog-Output Comparators for Monitor Detection
- RS-343A-Compatible Outputs
- Direct VGA Pass-Through Capability
- Palette-Page Register
- Horizontal Zooming Capability
- CMOS Technology
- DOS OM-1 Compatible for 16-Bit Video with Graphics
- Additional VGA Clock Frequencies Pullups Added to Pixel Port Terminals
- Dot Clock Added to RCLK Output Multiplexor
- VESA Advanced-Feature Connector (VAFC) Baseline Connector Compatible
- Pixel Port Bank Switching
- Data Manual Available†

PRODUCT PREVIEW

description

The TVP3027 is an advanced video interface palette (VIP) from Texas Instruments implemented in EPIC™ 0.8-micron CMOS process. The TVP3027 is an enhanced TVP3026. As such, it supports all modes and pixel formats of the TVP3026 VIP, including packed 24-bit true color with the phase-locked loop (PLL) generated, 50% duty cycle reference clock. In addition, the TVP3027 supports 16-bit video switching with graphics and VAFC baseline compatibility.

Like previous VIPs, data can be split into 4- or 8-bit planes for pseudo-color mode or split into 12-, 16- or 24-bit true-color and direct-color modes. For the 24-bit direct color modes, an 8-bit overlay plane is available. The 16-bit direct- and true-color modes can be configured to IBM XGA® (5, 6, 5), TARGA® (1, 5, 5, 5), or (6, 6, 4) as another existing format. An additional 12-bit mode (4, 4, 4, 4) is supported with 4 bits for each color and overlay. All color modes support selection of little or big endian data format for the pixel bus. Additionally, the device is also software compatible with the IMSG176/8 and Bt476/8 color palettes.

Two fully programmable PLLs for pixel clock and memory clock functions are provided for dramatic improvements in graphics system cost and integration. A third loop clock PLL is incorporated making pixel data latch timing much

† For the complete data manual, refer to the Graphics and Imaging Data Book (SLAD002).

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description (continued)

simpler than with other existing color palettes. In addition, four digital clock inputs (two TTL- and two ECL/TTL-compatible) may be utilized and are software selectable. The video clock provides a software selected divide ratio of the chosen pixel clock. The shift clock output may be used directly as the VRAM shift clock. The reference clock output is driven by the loop clock PLL and provides a timing reference to the graphics accelerator.

Like the TVP3026, the TVP3027 integrates a complete, 64 × 64 × 2 hardware cursor on chip, making significant graphics performance enhancements possible. Additionally, hardware port select and color keyed switching functions are provided, giving the user several efficient means of producing graphical overlays on direct-color backgrounds.

The TVP3027 has three 256-by-8 color lookup tables with triple, 8-bit video, digital-to-analog converters (DACs) capable of directly driving a doubly-terminated, 75-Ω line. The lookup tables are designed with a dual-ported RAM architecture that enables ultra-high speed operation. Sync generation is incorporated on the green output channel. Horizontal sync (HSYNC) and vertical sync (VSYNC) are pipeline delayed through the device and optionally inverted to indicate screen resolution to the monitor. A palette-page register is available to select from multiple color maps in RAM when 4-bit planes are used. This allows the screen colors to be changed with only one microprocessor write cycle.

The device features a separate VGA bus which supports the integrated VGA modes in graphics accelerator applications, allowing efficient support for VGA graphics and text modes. The separate bus is also useful for accepting data from the feature connector of most VGA-supported personal computers, without the need for external data multiplexing.

The TVP3027 is highly system integrated. It can be connected to the serial port of video RAM (VRAM) devices without external buffer logic and connected to many graphics engines directly. It also supports the split shift-register transfer function, which is common to many industry standard VRAM devices.

The system-integration concept is even carried further to manufacturing test and field diagnosis. To support these, several highly integrated test functions have been designed to enable simplified testing of the palette and the entire graphics system.

PRODUCT PREVIEW

AVAILABLE OPTIONS

T_A	SPEED	DAC RESOLUTION	PACKAGE FLAT PACK (PCE)
0°C to 70°C	135 MHz	8 Bits	TVP3027–135PCE
	175 MHz	8 Bits	TVP3027–175PCE
	220 MHz	8 Bits	TVP3027–220PCE

functional block diagram

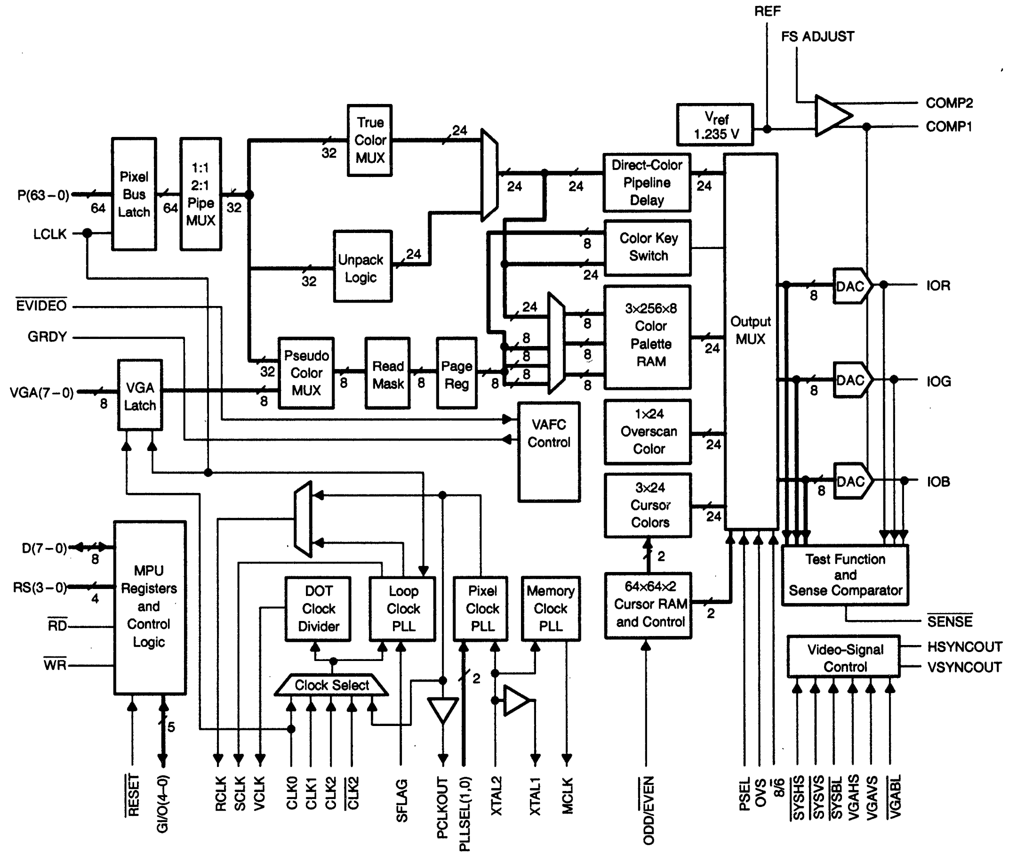

Figure 1. Functional Block Diagram

PRODUCT PREVIEW

- Supports System Resolutions up to 1600 × 1280 at 86-Hz Refresh Rate
- Supports Color Depths of 4-, 8-, 16-, 24-, and 32-Bit/Pixel, All at Maximum Resolution
- 128-Bit-Wide Pixel Bus
- Versatile Direct-Color Modes:
  - 24-Bit/Pixel With 8-Bit Overlay (O, R, G, B)
  - 24-Bit/Pixel (R, G, B)
  - 16-Bit/Pixel (5, 6, 5) XGA® Configuration
  - 16-Bit/Pixel (6, 6, 4) Configuration
  - 15-Bit/Pixel With 1-Bit Overlay (1, 5, 5, 5) TARGA® Configuration
  - 12-Bit/Pixel With 4-Bit Overlay (4, 4, 4, 4)
- True-Color Gamma Correction
- Supports Packed Pixel Formats for 24-Bit/Pixel Using a 32-, 64-, or 128-Bit/Pixel Bus
- 50% Duty Cycle Reference Clock for Higher Screen Refresh Rates in Packed-24 Modes
- Programmable Frequency Synthesis PLLs for Dot Clock and Memory Clock
- Loop Clock PLL Compensates for System Delay and Ensures Reliable Data Latching
- Versatile Pixel Bus Interface Supports Little- and Big-Endian Data Formats
- 175-, 220-, and 250-MHz Versions
- On-Chip Hardware Cursor, 64 × 64 × 2 Cursor (XGA and X-Windows Functionally Compatible)
- Byte Router Allows Use of R,G, or B Direct-Color Channels Individually
- Direct Interfacing to Video RAM
- Supports Overscan for Creation of Custom Screen Borders
- Color-Keyed Switching of Direct Color and and True Color or Overlay
- Triple 8-Bit D/A Converters
- Analog Output Comparators for Monitor Detection
- RS-343A-Compatible Outputs
- Direct VGA Pass-Through Capability
- Palette-Page Register
- Horizontal Zooming Capability
- CMOS Technology
- Data Manual Available†

description

The TVP3030 is an advanced video interface palette (VIP) from Texas Instruments implemented in EPIC™ 0.8-micron CMOS process. The TVP3030 is a 128-bit VIP that provides virtually all features of the 64-bit TVP3026. The TVP3030 doubles the pixel bus bandwidth, enabling 24-bit/pixel displays at resolutions up to 1600 × 1280 at a 76-Hz refresh rate. Also, 24-bit/pixel graphics at 1280 × 1024 resolution may be implemented at higher refresh rates with or without the use of pixel packing.

With the wider pixel bus comes additional 24-bit/pixel multiplexing modes: 4:1 [128-bit bus width for overlay, red, green, and blue (RGB)] and 5:1 (120-bit bus width for RGB). The byte router function allows pseudo-color or monochrome image data to be taken from the red, green, or blue color channels. This enables high performance 24-bit/pixel architectures organized as red, green, and blue memory banks to provide 8-bit/pixel modes as well.

The TVP3030 extends the packed-24 modes to include 16:3 (pixels:load clocks) using a 128-bit pixel bus width. This enables, for example, 24-bit/pixel graphics at 220 MHz pixel rate with only a 40 MHz VRAM serial output. With the 8:3 packed-24 mode (64-bit pixel bus width), a 24-bit/pixel display with 1280 x 1024 resolution may be packed into 4 megabytes of VRAM. A phase-locked loop (PLL) generated, 50 % duty cycle reference clock is output in the packed-24 modes, maximizing VRAM cycle time.

The TVP3030 supports all of the pixel formats of the TVP3026 VIP. Data can be split into 4- or 8-bit planes for pseudo-color mode or split into 12-, 16- or 24-bit true-color and direct-color modes. For the 24-bit direct color modes, an 8-bit overlay plane is available. The 16-bit direct- and true-color modes can be configured to IBM XGA® (5, 6, 5), TARGA® (5, 5, 5, 1), or (6, 6, 4) as another existing format. An additional 12-bit mode (4, 4, 4, 4) is supported with 4 bits for each color and overlay. All color modes support selection of little or big endian data format for the pixel bus. Additionally, the device is also software compatible with the IMSG176/8 and Bt476/8 color palettes.

† For the complete data manual, refer to the Graphics and Imaging Data Book (SLAD002).

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TARGA is a registered trademark of Truevision Incorporated.

description (continued)

Two fully programmable PLLs for pixel clock and memory clock functions are provided for dramatic improvements in graphics system cost and integration. A third loop clock PLL is incorporated making pixel data latch timing much simpler than with other existing color palettes. In addition, an external digital clock input is provided for VGA modes. The reference clock output is driven by the loop clock PLL and provides a timing reference to the graphics accelerator. The shift clock output may be used directly as the VRAM shift clock.

Like the TVP3026, the TVP3030 also integrates a complete, IBM XGA-compatible hardware cursor on chip, making significant graphics performance enhancements possible. Additionally, color-keyed switching is provided, giving the user an efficient means of combining graphic overlays and direct-color images on-screen.

The TVP3030 has three 256-by-8 color lookup tables with triple, 8-bit video, digital-to-analog converters (DACs) capable of directly driving a doubly-terminated, 75-Ω line. The lookup tables are designed with a dual-ported RAM architecture that enables ultra-high speed operation.

The device features a separate VGA bus which supports the integrated VGA modes in graphics accelerator applications, allowing efficient support for VGA graphics and text modes. The separate bus is also useful for accepting data from the feature connector of most VGA-supported personal computers, without the need for external data multiplexing.

The TVP3030 is highly system integrated. It can be connected to the serial port of VRAM devices without external buffering and connected to many graphics engines directly. It also supports the split shift-register transfer operation, which is common to many industry standard VRAM devices. To aid in manufacturing test and field diagnosis, several highly integrated test functions have been designed to enable simplified testing of the palette and the entire graphics subsystem.

AVAILABLE OPTIONS

T_A	SPEED	DAC RESOLUTION	PACKAGE	
			FLAT PACK (PPA)	FLAT PACK (MEP)
0°C to 70°C	175 MHz	8 Bits	TVP3030–175PPA	–
	220 MHz	8 Bits	TVP3030–220PPA	–
	250 MHz	8 Bits	–	TVP3030–250MEP

functional block diagram

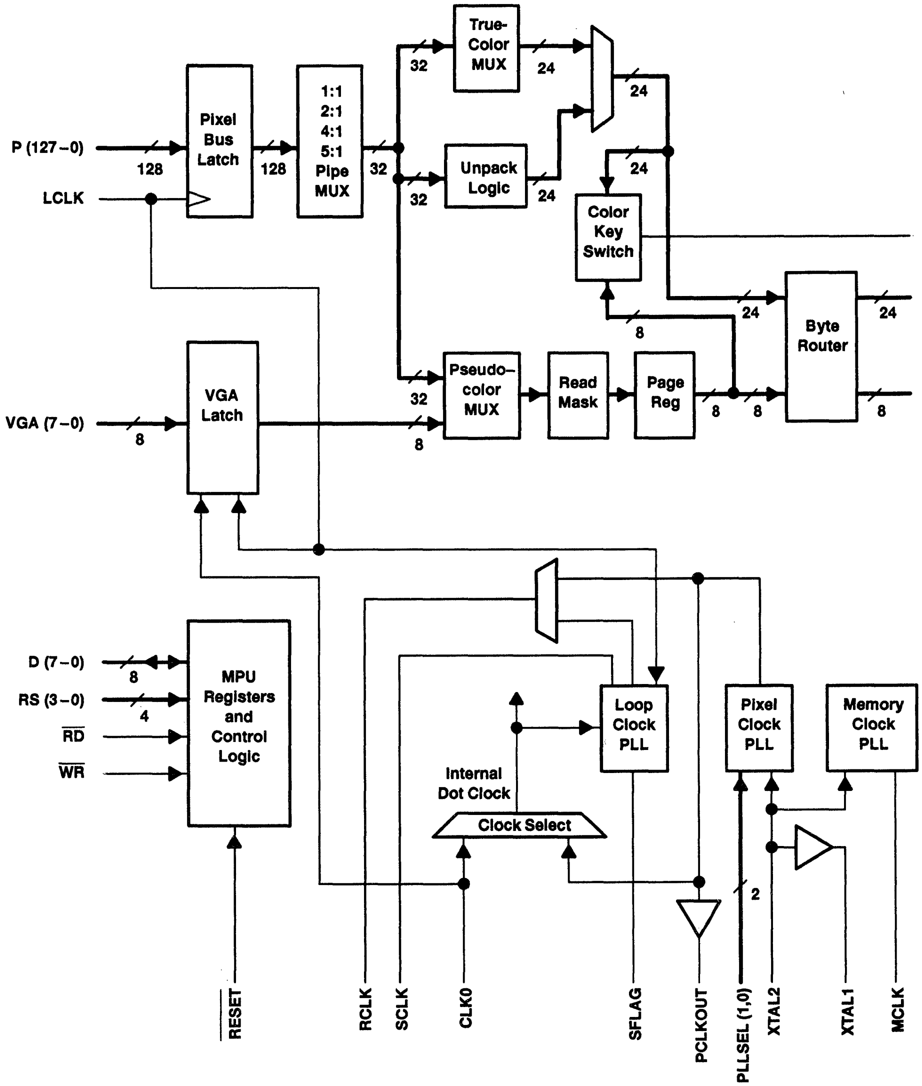

Figure 1. Functional Block Diagram

functional block diagram (continued)

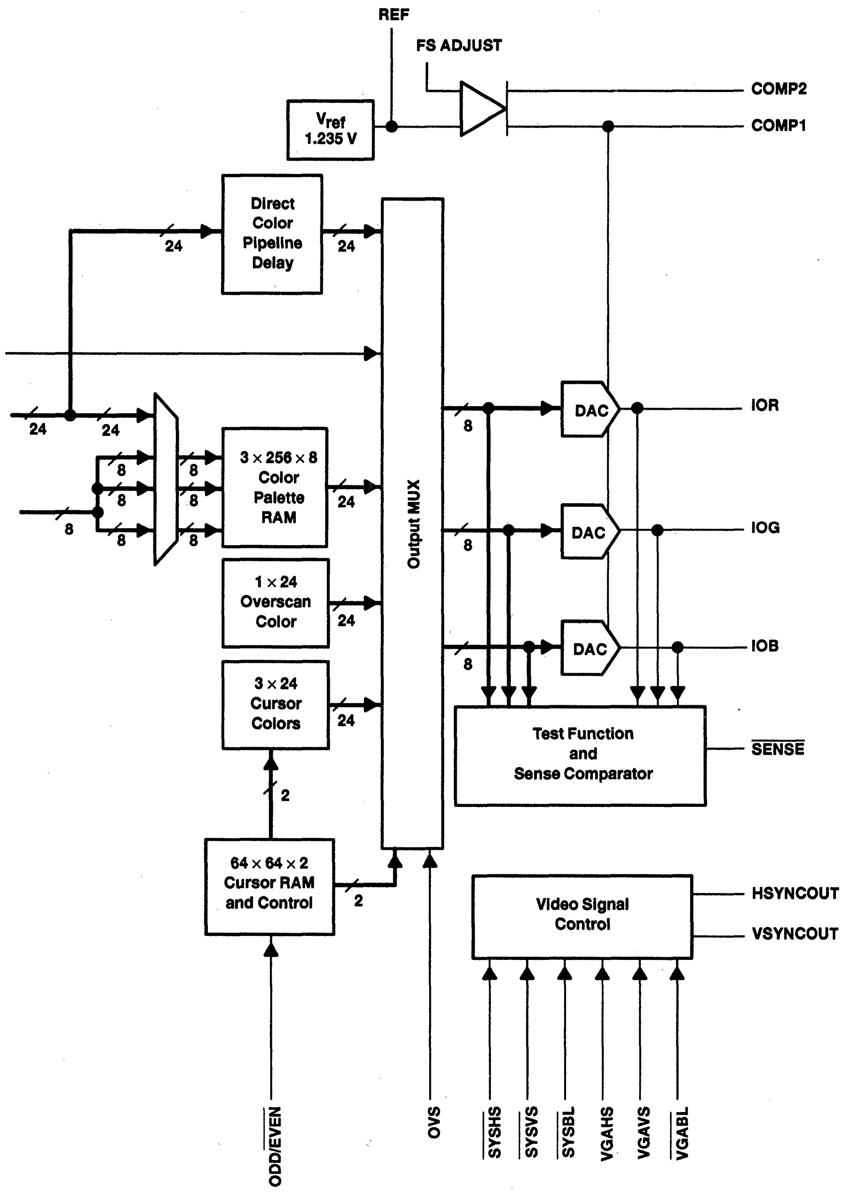

Figure 2. Functional Block Diagram

features

- Functionally Interchangeable With ATT20C409
- 170/135 MHz
  - 170 MHz 2:1 Multiplexer Rate for 8-Bit Pseudocolor Operation
  - 73 MHz True-Color Operation
- 16-Bit Pixel Port, Usable as 8-Bit Port
  - Compatible With ATT20C490 Using P(7-0)
  - Compatible With ATT20C498 Using P(15-0)
- 9 Software-Selectable Color Modes
  - 24-Bit Packed Pixels
  - 24-Bit 16-Bit True Color
  - 8-Bit Pseudocolor
- 2:1 and 1:1 Pixel Multiplexing
- Power Dissipation of 1.19 W at 135 MHz Typ
- Dual Programmable-Clock Synthesizers
  - Pixel Clock
  - Memory Clock
  - Reset to 28.322 MHz and 25.175 MHz VGA Frequencies
  - Strobe Input Latches Frequency Select Lines
- On-Chip PLL Clock Doubler
  - 85 MHz Input
  - 170 MHz Pixel Output
- 256 × 24 Color RAM
- Software Compatible With the AT&T ATT20C498/499/409
- 68-Terminal Plastic Leaded Chip Carrier (PLCC) Package
- Data Manual Available†

applications

- Screen Resolutions (noninterlaced)
  - 1600 × 1280, 8-Bit/Pixel, 60 Hz
  - 1280 × 1024, 16-Bit/Pixel, 60 Hz
  - 1024 × 768, 16-Bit/Pixel, 85 Hz
  - 1024 × 768, 24-Bit/Pixel, Packed, 70 Hz
  - 800 × 600, 24-Bit/Pixel, Unpacked, 72 Hz
- True-Color Desktop, PC Add-in Card
- X-Windows Terminals
- Green PCs

PRODUCT PREVIEW

description

The TVP3409 is functionally interchangable with the ATT20C409 RAMDAC.

The TVP3409 RAMDAC supports 8-bit multiplexed operation that can be input on 16-pixel terminals. The TVP3409 retains register compatiblity with the ATT21C498 and ATT20C499 parts.

The TVP3409 features 24-bit, packed pixel modes that provide 24-bit graphics in a 3-Mbyte frame buffer at 1024 x 768 screen resolution. Dual clock synthesizers offer two programmable and two fixed frequencies in phase-locked loop (PLL) (A), and one programmable and three fixed frequencies in PLL (B). After reset the frequencies are:

PLL (A): 25.175, 28.322, 50, and 75 MHz

PLL (B): 30, 40, 50, and 60 MHz

AVAILABLE OPTIONS

T_A	SPEED	DAC RESOLUTION	PACKAGE CHIP CARRIER (FN)
0°C to 70°C	135 MHz	8 Bits	TVP3409–135CFN
	170 MHz	8 Bits	TVP3409–170CFN

† For the complete data manual, refer to the Graphics and Imaging Data Book (SLAD002).

functional block diagram

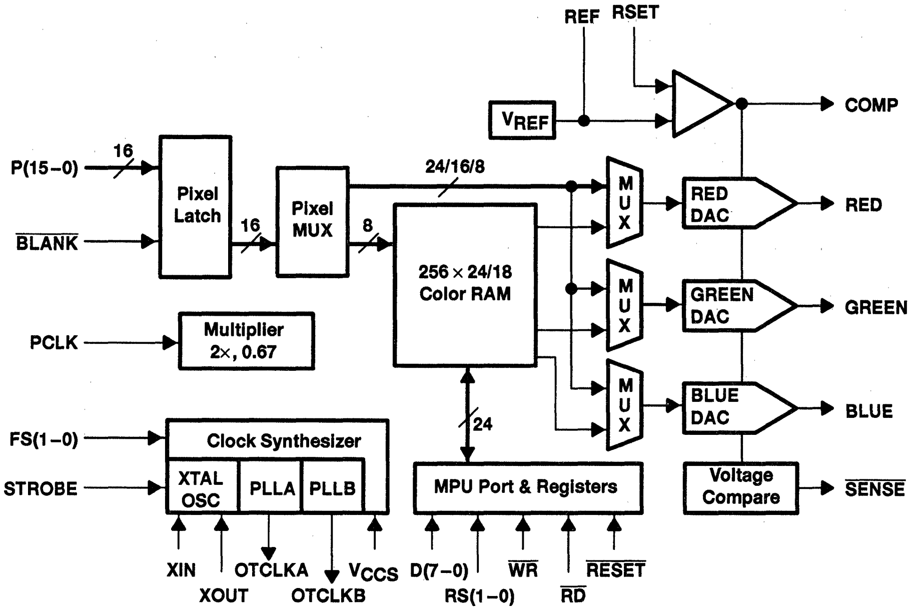

Figure 1. Functional Block Diagram

PRODUCT PREVIEW

- **Fully Integrated Dual Clock Synthesizer and 16-Bit Pixel Port True-Color RAMDAC**
- **Two Phase-Locked-Loop (PLL) Synthesizers Provide Independently Controlled Video and Memory Clock Outputs**
- **Functionally Interchangeable with STG1703**
- **On-Chip PLL Clock Reference Requires Single External Crystal**
- **16-Bit Pixel Port Supports VGA High-Color and True-Color Standards Up to 170 MHz**
- **Programmable Power-Down Features**
- **On-Chip Cyclic Redundancy Check (CRC) Test**
- **Data Sheet Available†**

applications

- **Screen resolutions (noninterlaced)**
  - **1600 × 1280, 8 bit/pixel, 60 Hz**
  - **1280 × 1024, 16 bit/pixel, 60 Hz**
  - **1024 × 768, 16 bit/pixel, 85 Hz**
  - **1024 × 768, 24 bit/pixel, packed, 70 Hz**
  - **800 × 600, 24 bit/pixel, unpacked, 72 Hz**
- **True-color desktop, PC add-in cards**

description

The TVP3703 is a super VGA (SVGA) compatible, true-color CMOS RAMDAC with integrated clock synthesizers that can provide the memory and pixel clock signals for a PC graphics subsystem. The video clock can be one of two VGA base frequencies or 14 VESA standard frequencies that can also be reprogrammed through the standard microport interface.

The memory clock output is also user programmable at frequencies up to 80 MHz. The pixel modes supported by the TVP3703 include:

- Serializing 16-bit pixel port providing 170 MHz 8-bit and 73 MHz 24-bit packed pixel modes using an internal PLL
- 16-bit pixel port providing faster high-color/true-color operation up to the 110-MHz sampling rate
- 8-bit pixel port giving standard SVGA and high-color/true-color modes up to the 110-MHz sampling rate

The 68-terminal plastic leaded chip carrier (PLCC) package is designed to be interchangeable with the STG1703.

AVAILABLE OPTIONS

T_A	SPEED	DAC RESOLUTION	PACKAGE CHIP CARRIER (FN)
0°C to 70°C	135 MHz	8 Bits	TVP3703-135CFN
	170 MHz	8 Bits	TVP3703-170CFN

PRODUCT PREVIEW

† For the complete data sheet, refer to the Graphics and Imaging Data book (SLAD002).

functional block diagram

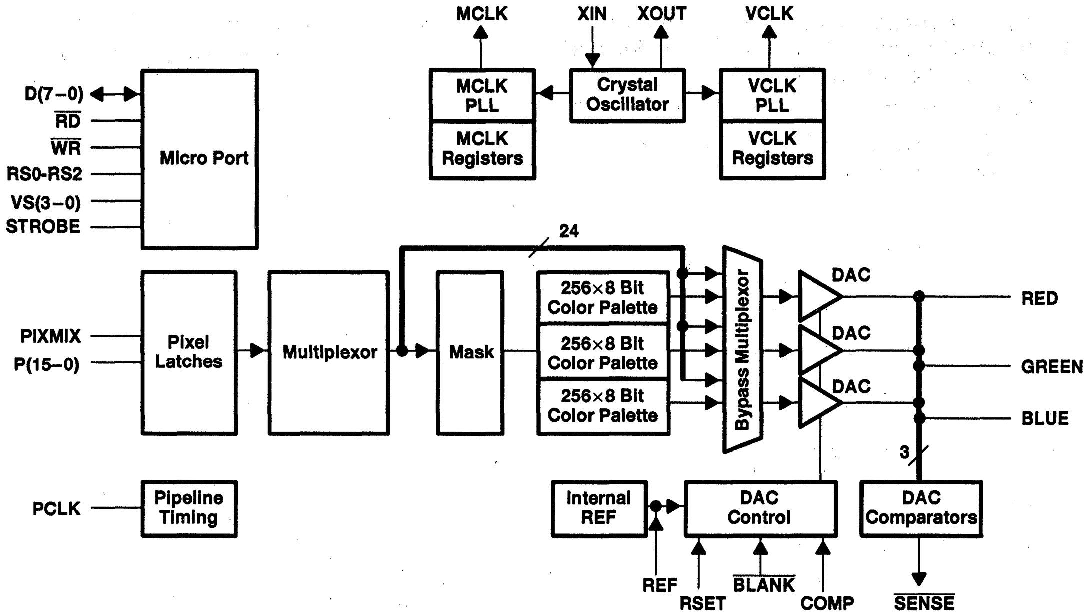

Figure 1. Functional Block Diagram

PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

TLC32046C, TLC32046I, TLC32046M Data Manual

Wide-Band Analog Interface Circuit

TEXAS INSTRUMENTS

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1 Introduction

The TLC32046C, TLC32046I, and TLC32046M wide-band analog interface circuits (AIC) are a complete analog-to-digital and digital-to-analog interface system for advanced digital signal processors (DSPs) similar to the TMS32020, TMS320C25, and TMS320C30. The TLC32046C and TLC32046I offer a powerful combination of options under DSP control: three operating modes (dual-word [telephone interface], word, and byte) combined with two word formats (8 bits and 16 bits) and synchronous or asynchronous operation. It provides a high level of flexibility in that conversion and sampling rates, filter bandwidths, input circuitry, receive and transmit gains, and multiplexed analog inputs are under processor control.

This AIC features a

- band-pass switched-capacitor antialiasing input filter
- 14-bit-resolution A/D converter
- 14-bit-resolution D/A converter
- low-pass switched-capacitor output-reconstruction filter.

The antialiasing input filter comprises eighth-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When low-pass filtering is desired, the high-pass filter can be switched out of the signal path. A selectable auxiliary differential analog input is provided for applications where more than one analog input is required.

The output-reconstruction filter is an eighth-order CC-type (Chebyshev/elliptic transitional low-pass filter) followed by a second-order (sin x)/x correction filter and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the sample data signal. The on-board (sin x)/x correction filter can be switched out of the signal path using digital signal processor control.

The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided to ease the design task and to provide complete control over the performance of the IC. The internal voltage reference is brought out to REF. Separate analog and digital voltage supplies and ground are provided to minimize noise and ensure a wide dynamic range. The analog circuit path contains only differential circuitry to keep noise to a minimum. The exception is the DAC sample-and-hold, which utilizes pseudo-differential circuitry.

The TLC32046C is characterized for operation from 0°C to 70°C, the TLC32046I is characterized for operation from −40°C to 85°C, and the TLC32046M is characterized for operation from −55°C to 125°C.

1.1 Features

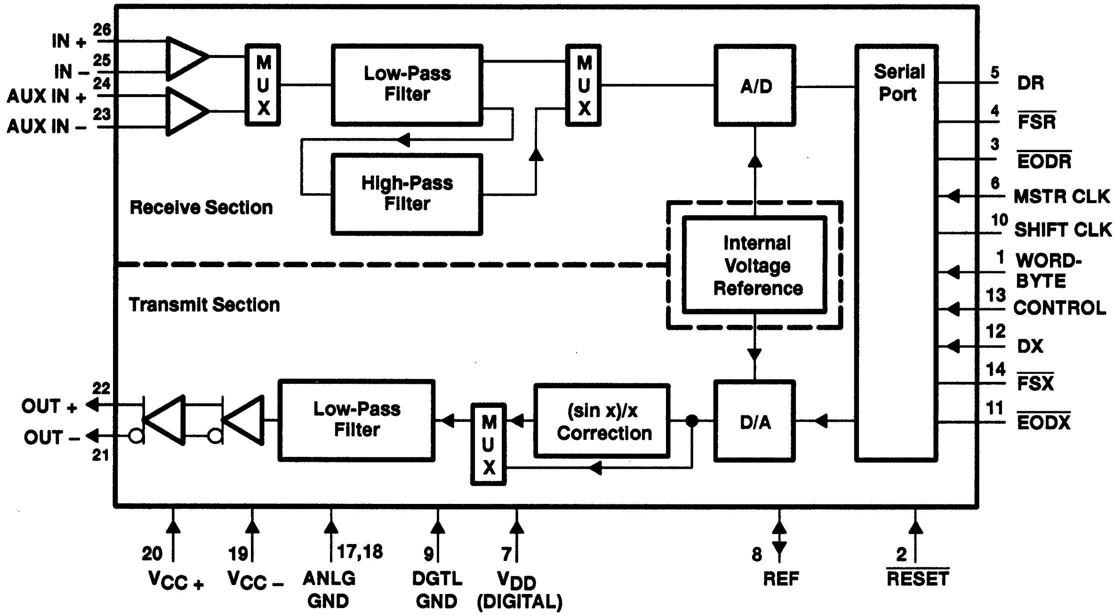
- **14-Bit Dynamic Range ADC and DAC**
- **16-Bit Dynamic Range Input With Programmable Gain**
- **Synchronous or Asynchronous ADC and DAC Sampling Rates Up to 25,000 Samples Per Second**
- **Programmable Incremental ADC and DAC Conversion Timing Adjustments**
- **Typical Applications**
  - **Speech Encryption for Digital Transmission**
  - **Speech Recognition and Storage Systems**
  - **Speech Synthesis**
  - **Modems at 8-kHz, 9.6-kHz, and 16-kHz Sampling Rates**
  - **Industrial Process Control**
  - **Biomedical Instrumentation**
  - **Acoustical Signal Processing**
  - **Spectral Analysis**
  - **Instrumentation Recorders**
  - **Data Acquisition**
- **Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter**
- **Three Fundamental Modes of Operation: Dual-Word (Telephone Interface), Word, and Byte**
- **600-mil Wide N Package**
- **Digital Output in Twos Complement Format**
- **CMOS Technology**

FUNCTION TABLE

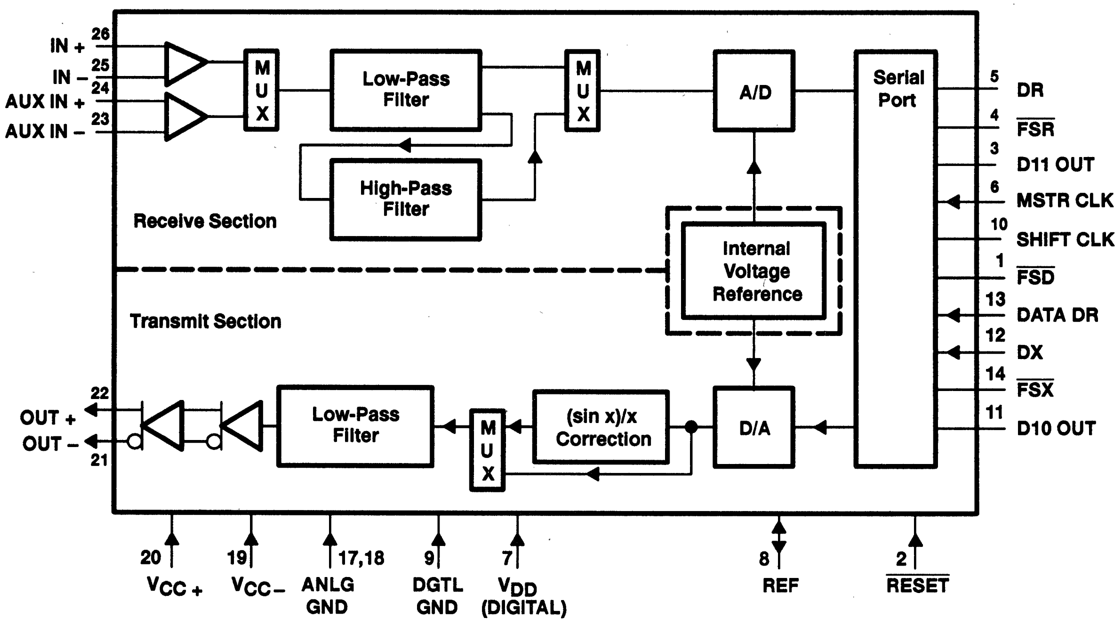
DATA COMMUNICATIONS FORMAT	SYNCHRONOUS (CONTROL REGISTER BIT D5 = 1)	ASYNCHRONOUS (CONTROL REGISTER BIT D5 = 0)	FORCING CONDITION	DIRECT INTERFACE
16-bit format	Dual-word (telephone interface) mode	Dual-word (telephone interface) mode	Terminal 13 = 0 to 5 V Terminal 1 = 0 to 5 V	TMS32020, TMS320C25, TMS320C30
16-bit format	Word mode	Word mode	Terminal 13 = V_{CC-} (–5 V nom) Terminal 1 = V_{CC+} (5 V nom)	TMS32020, TMS320C25, TMS320C30, indirect interface to TMS320C10. (see Figure 7).
8-bit format (2 bytes required)	Byte mode	Byte mode	Terminal 13 = V_{CC-} (–5 V nom) Terminal 1 = V_{CC-} (–5 V nom)	TMS320C17

1.2 Functional Block Diagrams

WORD OR BYTE MODE



DUAL-WORD (TELEPHONE INTERFACE) MODE



FRAME SYNCHRONIZATION FUNCTIONS

Function	Frame Sync Output
Receiving serial data on DX from processor to internal DAC	$\overline{FSX}$ low
Transmitting serial data on DR from internal ADC to processor, primary communications	$\overline{FSR}$ low
Transmitting serial data on DR from Data-DR to processor, secondary communications in dual-word (telephone interface) mode only	$\overline{FSD}$ low

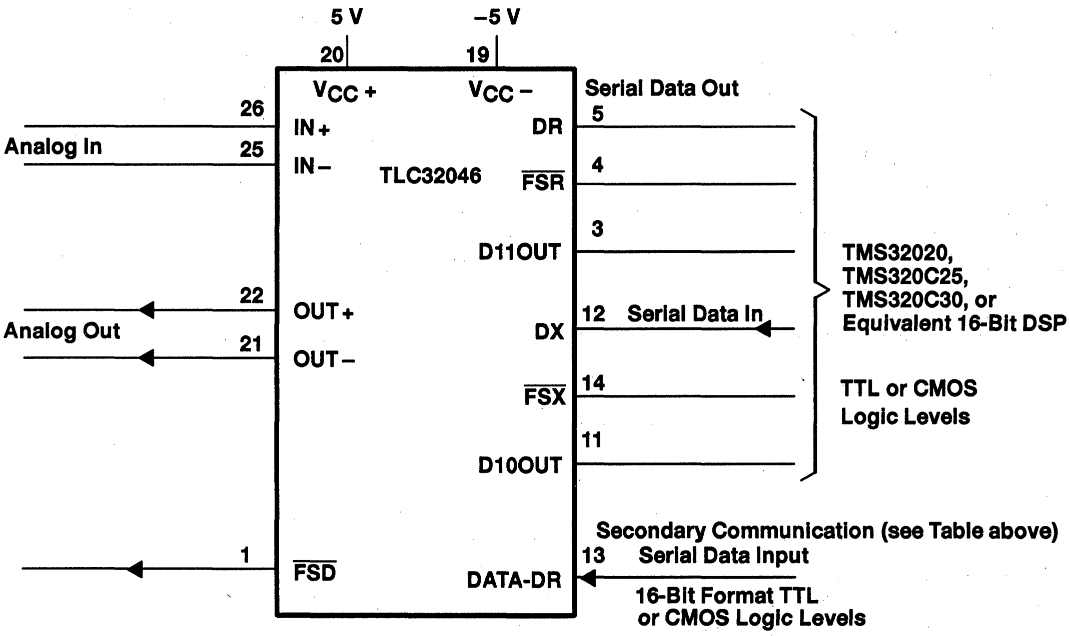


Figure 1–1. Dual-Word (Telephone Interface) Mode

When the DATA-DR/CONTROL input is tied to a logic signal source varying between 0 and 5 V, the TLC32046 is in the dual-word (telephone interface) mode. This logic signal is routed to the DR line for input to the DSP only when data frame synchronization ($\overline{FSD}$) outputs a low level. The $\overline{FSD}$ pulse duration is 16 shift clock pulses. Also, in this mode, the control register data bits D10 and D11 appear on D10OUT and D11OUT, respectively, as outputs.

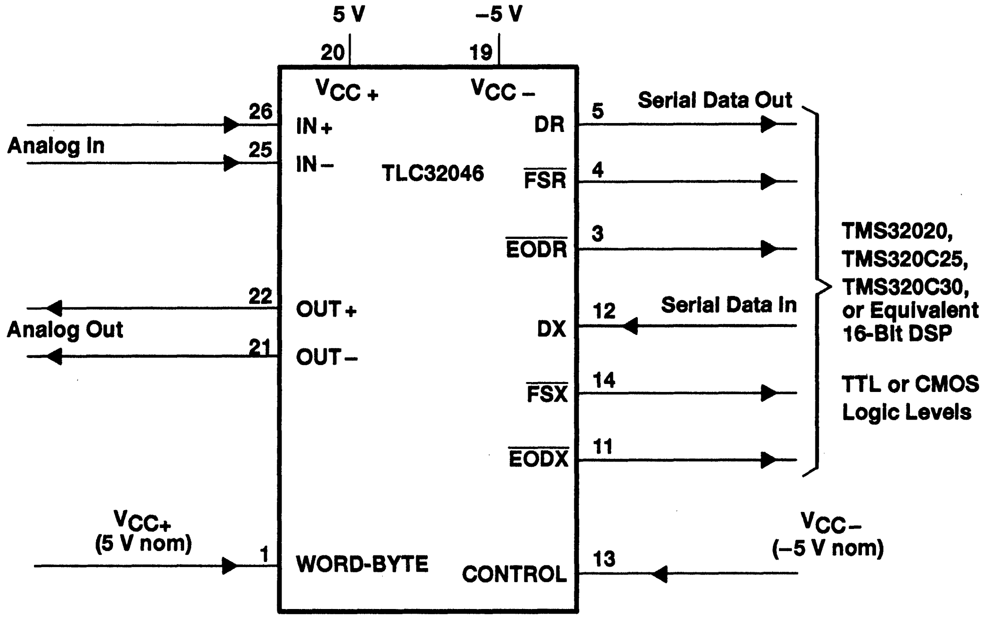


Figure 1–2. Word Mode

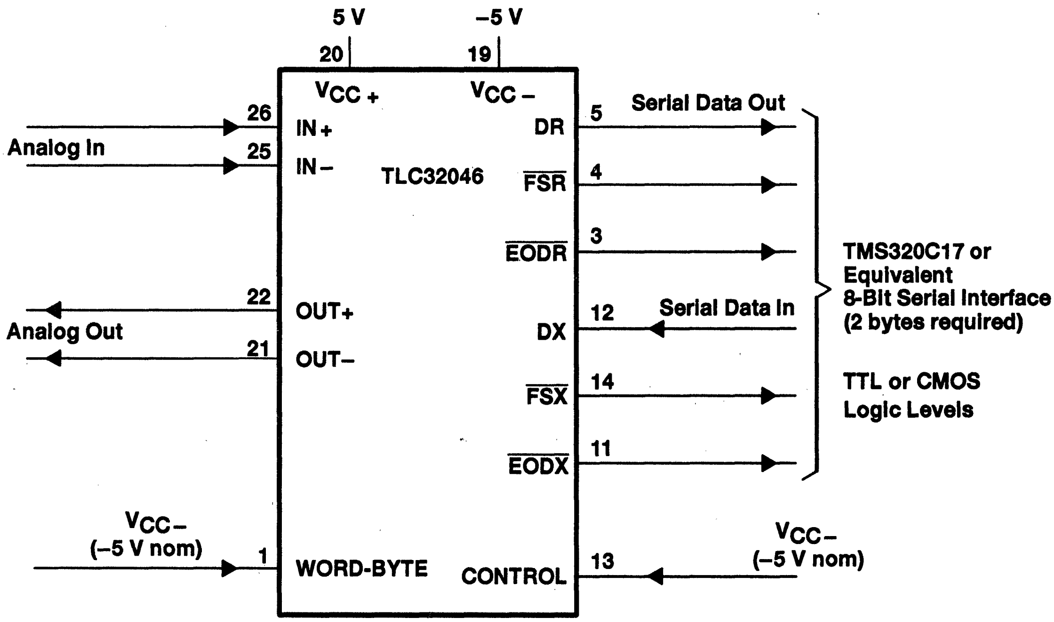
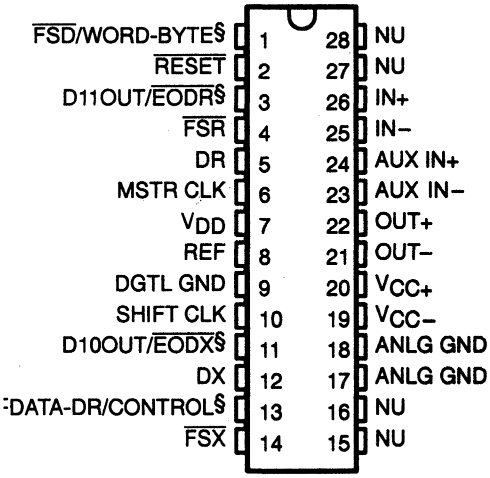


Figure 1–3. Byte Mode

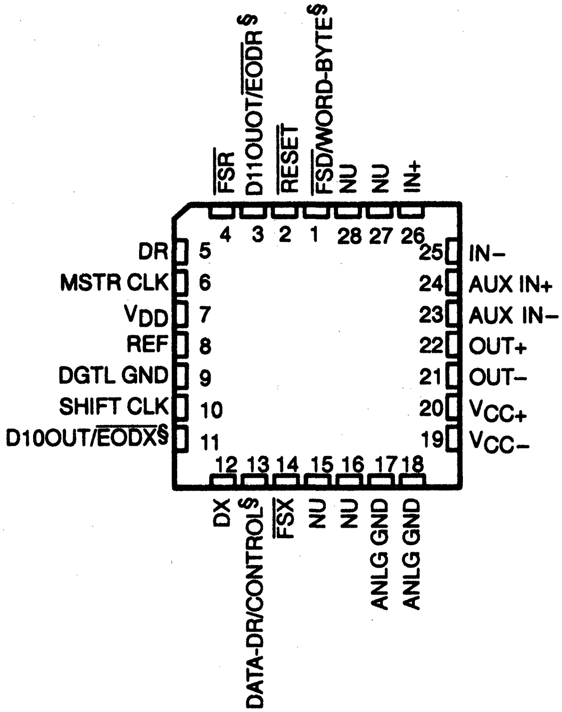
The word or byte mode is selected by first connecting the DATA-DR/CONTROL input to V_{CC-}. $\overline{\text{FSD}}$/WORD-BYTE becomes an input and can then be used to select either word or byte transmission formats. The end-of-data transmit ($\overline{\text{EODX}}$) and the end-of-data receive ($\overline{\text{EODR}}$) signals respectively, are used to signal the end of word or byte communication (see the Terminal Functions section).

1.3 Terminal Assignments

J† OR N PACKAGE‡
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



NU - Nonusable; no external connection should be made to these terminals.

† Refer to the mechanical data for the JT package.
‡ 600-mil wide
§ The portion of the terminal name to the left of the slash is used for the dual-word (telephone interface) mode. The portion of the terminal name to the right of the slash is used for word-byte mode.

1.4 Ordering Information

AVAILABLE OPTIONS

T_A	PACKAGE			
	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)	CERAMIC DIP (J)	CHIP CARRIER (FK)
0°C to 70°C	TLC32046CFN	TLC32046CN		
−40°C to 85°C	TLC32046IFN	TLC32046IN		
−55°C to 125°C			TLC32046MJ	TLC32046MFK

1.5 Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
ANLG GND	17,18		Analog ground return for all internal analog circuits. Not internally connected to DGTL GND.
AUX IN+	24	I	Noninverting auxiliary analog input stage. AUX IN+ can be switched into the band-pass filter and ADC path via software control. If the appropriate bit in the control register is a 1, the auxiliary inputs replace the IN+ and IN– inputs. If the bit is a 0, the IN+ and IN– inputs are used (see the DX Serial Data Word Format).
AUX IN–	23	I	Inverting auxiliary analog input (see the above AUX IN+ description).
DATA-DR	13	I	The dual-word (telephone interface) mode, selected by applying an input logic level between 0 and 5 V to DATA-DR, allows this terminal to function as a data input. The data is then framed by the $\overline{\mathrm{FSD}}$ signal and transmitted as an output to the DR line during secondary communication. The functions $\overline{\mathrm{FSD}}$, D11OUT, and D10OUT are valid with this mode selection (see Table 2–1).
CONTROL			When CONTROL is tied to V_{CC-}, the device is in the word or byte mode. The functions WORD-BYTE, $\overline{\mathrm{EODR}}$, and $\overline{\mathrm{EODX}}$ are valid in this mode. CONTROL is then used to select either the word or byte mode (see Function Table).
DR	5	O	DR is used to transmit the ADC output bits from the AIC to the TMS320 serial port. This transmission of bits from the AIC to the TMS320 serial port is synchronized with SHIFT CLK.
DX	12	I	DX is used to receive the DAC input bits and timing and control information from the TMS320. This serial transmission from the TMS320 serial port is synchronized with SHIFT CLK.
D10OUT	11	O	In the dual-word (telephone interface) mode, bit D10 of the control register is output to D10OUT. When the device is reset, bit D10 is initialized to 0 (see DX Serial Data Word Format). The output update is immediate upon changing bit D10.
$\overline{\mathrm{EODX}}$			End-of-data transmit. During the word-mode timing, a low-going pulse occurs on $\overline{\mathrm{EODX}}$ immediately after the 16 bits of DAC and control or register information have transmitted from the TMS320 serial port to the AIC.This signal can be used to interrupt a microprocessor upon completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM and to facilitate parallel data bus communications between the DSP and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the TMS320 serial port to the AIC and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate first and second bytes.
D11OUT	3	O	In the dual-word (telephone interface) mode, bit D11 of the control register is output to D11OUT. When the device is reset, bit D11 is initialized to 0 (see DX Serial Data Word Format). The output update is immediate upon changing bit D11.
$\overline{\mathrm{EODR}}$			End-of-data receive. During the word-mode timing, a low-going pulse occurs on $\overline{\mathrm{EODR}}$ immediately after the 16 bits of A/D information have been transmitted from the AIC to the TMS320 serial port. This signal can be used to interrupt a microprocessor upon completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM, and to facilitate parallel data bus communications between the DSP and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the AIC to the TMS320 serial port and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate between first and second bytes.

1.5 Terminal Functions (continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
DGTL	9		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
$\overline{\text{FSD}}$	1	O	Frame sync data. The $\overline{\text{FSD}}$ output remains high during primary communication. In the dual-word (telephone interface) mode, $\overline{\text{FSD}}$ is identical to $\overline{\text{FSX}}$ during secondary communication.
WORD-BYTE		I	WORD-BYTE allows differentiation between the word and byte data format (see DATA-DR/CONTROL and Table 2-1 for details).
$\overline{\text{FSR}}$	4	O	Frame sync receive. $\overline{\text{FSR}}$ is held low during bit transmission. When $\overline{\text{FSR}}$ goes low, the TMS320 serial port begins receiving bits from the AIC via DR of the AIC. The most significant DR bit is present on DR before $\overline{\text{FSR}}$ goes low (see Serial Port Sections and Internal Timing Configuration Diagrams).
$\overline{\text{FSX}}$	14	O	Frame sync transmit. When FSX goes low, the TMS320 serial port begins transmitting bits to the AIC via DX of the AIC. $\overline{\text{FSX}}$ is held low during bit transmission (see Serial Port Sections and Internal Timing Configuration Diagrams).
IN+	26	I	Noninverting input to analog input amplifier stage
IN−	25	I	Inverting input to analog input amplifier stage
MSTR CLK	6	I	The master clock signal is used to derive all the key logic signals of the AIC, such as the shift clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The Internal Timing Configuration diagram shows how these key signals are derived. The frequencies of these signals are synchronous submultiples of the master clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the ADC and DAC converters (see the Internal Timing Configuration).
OUT+	22	O	Noninverting output of analog output power amplifier. OUT+ drives transformer hybrids or high-impedance loads directly in a differential or a single-ended configuration.
OUT−	21	O	Inverting output of analog output power amplifier. OUT− is functionally identical with and complementary to OUT+.
REF	8	I/O	The internal voltage reference is brought out on REF. An external voltage reference can be applied to REF to override the internal voltage reference.
$\overline{\text{RESET}}$	2	I	A reset function is provided to initialize TA, TA', TB, RA, RA', RB (see Figure 2-1), and the control registers. This reset function initiates serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After a negative-going pulse on $\overline{\text{RESET}}$, the AIC registers are initialized to provide a 16-kHz data conversion rate for a 10.368-MHz master clock input signal. The conversion rate adjust registers, TA' and RA', are reset to 1. The CONTROL register bits are reset as follows (see AIC DX Data Word Format section): D11 = 0, D10 = 0, D9 = 1, D7 = 1, D6 = 1, D5 = 1, D4 = 0, D3 = 0, D2 = 1 The shift clock (SCLK) is held high during $\overline{\text{RESET}}$. This initialization allows normal serial-port communication to occur between the AIC and the DSP.
SHIFT CLK	10	O	The shift clock signal is obtained by dividing the master clock signal frequency by four. SHIFT CLK is used to clock the serial data transfers of the AIC.
V_{DD}	7		Digital supply voltage, 5 V ±5%
V_{CC+}	20		Positive analog supply voltage, 5 V ±5%
V_{CC-}	19		Negative analog supply voltage, −5 V ±5%

2 Detailed Description

Table 2–1. Mode-Selection Function Table

<table>
<tr><th>DATA-DR/ CONTROL (Terminal 13)</th><th>$\overline{\text{FSD}}$/ WORD-BYTE (Terminal 1)</th><th>CONTROL REGISTER BIT (D5)</th><th>OPERATING MODE</th><th>SERIAL CONFIGURATION</th><th>DESCRIPTION</th></tr>
<tr><td>Data in (0 V to 5 V)</td><td>FSD out (0 V to 5 V)</td><td>1</td><td>Dual Word (Telephone Interface)</td><td>Synchronous, One 16-Bit Word</td><td>Terminal functions DATA-DR†, $\overline{\text{FSD}}$†, D11OUT, and D10OUT are applicable in this configuration. $\overline{\text{FSD}}$ is asserted during secondary communication, but $\overline{\text{FSR}}$ is not asserted. However, $\overline{\text{FSD}}$ remains high during primary communication.</td></tr>
<tr><td>Data in (0 V to 5 V)</td><td>FSD out (0 V to 5 V)</td><td>0</td><td>Dual Word (Telephone Interface)</td><td>Synchronous, One 16-Bit Word</td><td>Terminal functions DATA-DR †, $\overline{\text{FSD}}$†, D11OUT, and D10OUT are applicable in this configuration. $\overline{\text{FSD}}$ is asserted during secondary communication, but $\overline{\text{FSR}}$ is not asserted. However, $\overline{\text{FSD}}$ remains high during primary communication. If secondary communications occur while the A/D conversion is being transmitted from DR, $\overline{\text{FSD}}$ cannot go low, and data from DATA-DR cannot go onto DR.</td></tr>
<tr><td rowspan="4">V_{CC-}</td><td rowspan="2">V_{CC+}</td><td>1</td><td rowspan="2">WORD</td><td>Synchronous, One 16-Bit Word</td><td>Terminal functions CONTROL†, WORD-BYTE†, $\overline{\text{EODR}}$, and $\overline{\text{EODX}}$ are applicable in this configuration.</td></tr>
<tr><td>0</td><td>Asynchronous, One 16-bit Word</td><td>Terminal functions CONTROL†, WORD-BYTE†, $\overline{\text{EODR}}$, and $\overline{\text{EODX}}$ are applicable in this configuration.</td></tr>
<tr><td rowspan="2">V_{CC-}</td><td>1</td><td rowspan="2">BYTE</td><td>Synchronous, Two 8-Bit Bytes</td><td>Terminal functions CONTROL†, WORD-BYTE†, $\overline{\text{EODR}}$, and $\overline{\text{EODX}}$ are applicable in this configuration.</td></tr>
<tr><td>0</td><td>Asynchronous, Two 8-Bit Bytes</td><td>Terminal functions CONTROL†, WORD-BYTE†, $\overline{\text{EODR}}$, and $\overline{\text{EODX}}$ are applicable in this configuration.</td></tr>
</table>

† DATA-DR/CONTROL has an internal pulldown resistor to −5 V, and $\overline{\text{FSD}}$/WORD-BYTE has an internal pullup resistor to 5 V.

2.1 Internal Timing Configuration (see Figure 2–1)

All the internal timing of the AIC is derived from the high-frequency clock signal that drives the master clock input. The shift clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the master clock input signal frequency by four.

The TX(A) counter and the TX(B) counter, which are driven by the master clock signal, determine the D/A conversion timing. Similarly, the RX(A) counter and the RX(B) counter determine the A/D conversion timing. In order for the low-pass switched-capacitor filter in the D/A path (see Functional Block Diagram) to meet its transfer function specifications, the frequency of its clock input must be 288 kHz. If the clock frequency is not 288 kHz, the filter transfer function frequencies are frequency-scaled by the ratios of the clock frequency to 288 kHz:

$$\text{Absolute Frequency (kHz)} = \frac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{288} \tag{1}$$

For Low-Pass SCF f_{clock} > 288 kHz, please call the factory.

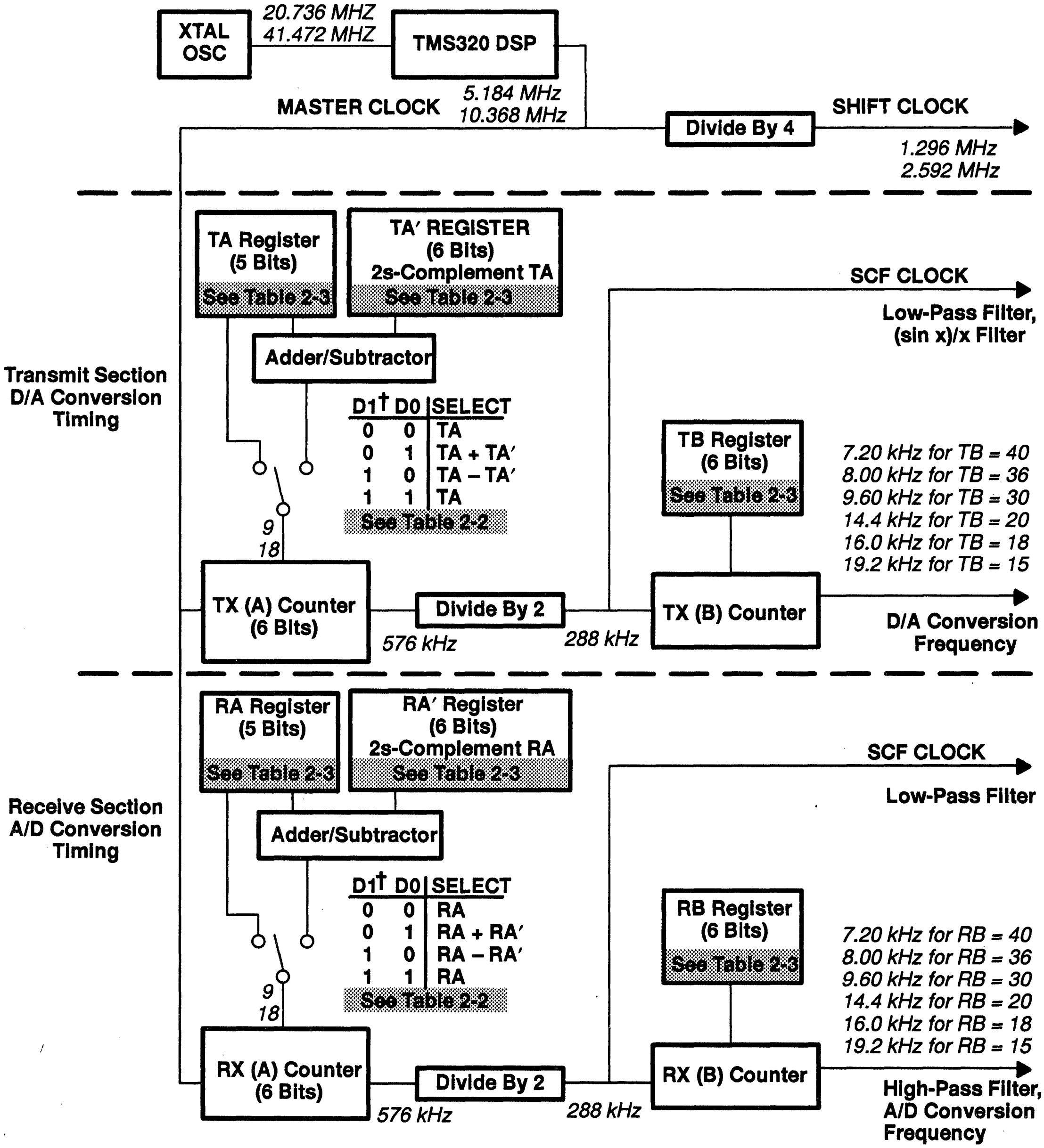
To obtain the specified filter response, the combination of master clock frequency and the TX(A) counter and the RX(A) counter values must yield a 288-kHz switched-capacitor clock signal. This 288-kHz clock signal can then be divided by the TX(B) counter to establish the D/A conversion timing.

The transfer function of the band-pass switched-capacitor filter in the A/D path (see Functional Block Diagram) is a composite of its high-pass and low-pass transfer functions. When the shift-clock frequency (SCF) is 288 kHz, the high-frequency roll-off of the low-pass section will meet the band-pass filter transfer function specification. Otherwise, the high-frequency roll-off is frequency-scaled by the ratio of the high-pass section SCF clock to 288 kHz (see Figure 5–5). The low-frequency roll-off of the high-pass section meets the band-pass filter transfer function specification when the A/D conversion rate is 16 kHz. If not, the low-frequency roll-off of the high-pass section is frequency-scaled by the ratio of the A/D conversion rate to 16 kHz.

The TX(A) counter and the TX(B) counter are reloaded each D/A conversion period, while the RX(A) counter and the RX(B) counter are reloaded every A/D conversion period. The TX(B) counter and the RX(B) counter are loaded with the values in the TB and RB registers, respectively. Via software control, the TX(A) counter can be loaded with the TA register, the TA register less the TA′ register, or the TA register plus the TA′ register. By selecting the TA register less the TA′ register option, the upcoming conversion timing occurs earlier by an amount of time that equals TA′ times the signal period of the master clock. If the TA register plus the TA′ register option is executed, the upcoming conversion timing occurs later by an amount of time that equals TA′ times the signal period of the master clock. Thus, the D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. However, the RX(A) counter can be programmed via software control with the RA register, the RA register less the RA′ register, or the RA register plus the RA′ register.

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing and can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.

If the transmit and receive sections are configured to be synchronous, then the low-pass and band-pass switched-capacitor filter clocks are derived from the TX(A) counter. Also, both the D/A and A/D conversion timings are derived from the TX(A) counter and the TX(B) counter. When the transmit and receive sections are configured to be synchronous, the RX(A) counter, RX(B) counter, RA register, RA′ register, and RB registers are not used.



† These control bits are described in the DX Serial Data Word Format section.

NOTES: A. Tables 2–2 and 2–3 are primary and secondary communication protocols, respectively.

B. In synchronous operation, RA, RA', RB, RX(A), and RX(B) are not used. TA, TA', TB, TX(A), and TX(B) are used instead.

C. Items in italics refer only to frequencies and register contents, which are variable. A crystal oscillator driving 20.736 MHz into the TMS320-series DSP provides a master clock frequency of 5.184 MHz. The TLC32046 produces a shift clock frequency of 1.296 MHz. If the TX(A) register contents equal 9, the SCF clock frequency is 288 kHz, and the D/A conversion frequency is 288 kHz ÷ T(B).

Figure 2–1. Asynchronous Internal Timing Configuration

2.2 Analog Input

Two pairs of analog inputs are provided. Normally, the IN+ and IN– input pair is used; however, the auxiliary input pair, AUX IN+ and AUX IN–, can be used if a second input is required. Since sufficient common-mode range and rejection are provided, each input set can be operated in differential or single-ended modes. The gain for the IN+, IN–, AUX IN+, and AUX IN– inputs can be programmed to 1, 2, or 4 (see Table 4–1). Either input circuit can be selected via software control. Multiplexing is controlled with the D4 bit (enable/disable AUX IN+ and AUX IN–) of the secondary DX word (see Table 2–3). The multiplexing requires a 2-ms wait at SCF = 288 kHz (see Figure 5–3) for a valid output signal. A wide dynamic range is ensured by the differential internal analog architecture and the separate analog and digital voltage supplies and grounds.

2.3 A/D Band-Pass Filter, Clocking, and Conversion Timing

The receive-channel A/D high-pass filter can be selected or bypassed via software control (see Functional Block Diagram). The frequency response of this filter is found in the electrical characteristic section. This response results when the switched-capacitor filter clock frequency is 288 kHz and the A/D sample rate is 16 kHz. Several possible options can be used to attain a 288-kHz switched-capacitor filter clock. When the filter clock frequency is not 288 kHz, the low-pass filter transfer function is frequency-scaled by the ratio of the actual clock frequency to 288 kHz (see Typical Characteristics section). The ripple bandwidth and 3-dB low-frequency roll-off points of the high-pass section are 300 Hz and 200 Hz, respectively. However, the high-pass section low-frequency roll-off is frequency-scaled by the ratio of the A/D sample rate to 16 kHz.

Figure 2–1 and the DX serial data word format sections of this data manual indicate the many options for attaining a 288-kHz band-pass switched-capacitor filter clock. These sections indicate that the RX(A) counter can be programmed to give a 288-kHz band-pass switched-capacitor filter clock for several master clock input frequencies.

The A/D conversion rate is attained by frequency-dividing the band-pass switched-capacitor filter clock with the RX(B) counter. Unwanted aliasing is prevented because the A/D conversion rate is an integer submultiple of the band-pass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

2.4 A/D Converter

Fundamental performance specifications for the receive channel ADC circuitry are in the electrical characteristic section of this data manual. The ADC circuitry, using switched-capacitor techniques, provides an inherent sample-and-hold function.

2.5 Analog Output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out of the IC. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

2.6 D/A Low-Pass Filter, Clocking, and Conversion Timing

The frequency response results when the low-pass switched-capacitor filter clock frequency is 288 kHz (see equation 1). Like the A/D filter, the transfer function of this filter is frequency-scaled when the clock frequency is not 288 kHz (see Typical Characteristics section). A continuous-time filter is provided on the output of the low-pass filter to eliminate the periodic sample data signal information, which occurs at multiples of the 288-kHz switched-capacitor clock feedthrough.

The D/A conversion rate is attained by frequency-dividing the 288-kHz switched-capacitor filter clock with the T(B) counter. Unwanted aliasing is prevented because the D/A conversion rate is an integer submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.

2.7 D/A Converter

Fundamental performance specifications for the transmit channel DAC circuitry are in the electrical characteristic section. The DAC has a sample-and-hold function that is realized with a switched-capacitor ladder.

2.8 Serial Port

The serial port has four possible configurations summarized in the function table on page 1–2. These configurations are briefly described below.

- The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS320C17. The communications protocol is two 8-bit bytes.
- The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, and TMS320C30. The communications protocol is one 16-bit word.
- The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS320C17. The communications protocol is two 8-bit bytes.
- The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, TMS320C30, or two SN74299 serial-to-parallel shift registers, which can interface in parallel to the TMS32010, TMS320C15, to any other digital signal processor, or to external FIFO circuitry. The communications protocol is one 16-bit word.

2.9 Synchronous Operation

When the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and band-pass filters (see Functional Block Diagram). The A/D conversion timing is derived from and equal to the D/A conversion timing. When data bit D5 in the control register is a logic 1, transmit and receive sections are synchronous. The band-pass switched-capacitor filter and the A/D converter timing are derived from the TX(A) counter, the TX(B) counter, and the TA and TA' registers. In synchronous operation, both the A/D and the D/A channels operate from the same frequencies. The $\overline{\text{FSX}}$ and the $\overline{\text{FSR}}$ timing is identical during primary communication, but $\overline{\text{FSR}}$ is not asserted during secondary communication because there is no new A/D conversion result.

2.9.1 One 16-Bit Word (Dual-Word [Telephone Interface] or Word Mode)

The serial port interfaces directly with the serial ports of the TMS32020, TMS320C25, and the TMS320C30, and communicates in one 16-bit word. The operation sequence is as follows:

1. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low by the TLC32046 AIC.
2. One 16-bit word is transmitted and one 16-bit word is received.
3. $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ are brought high.
4. $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ emit low-going pulses one shift clock wide. $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ are valid in the word or byte mode only.

If the device is in the dual-word (telephone interface) mode, $\overline{\text{FSD}}$ goes low during the secondary communication period and enables the data word received at the DATA-DR/CONTROL input to be routed to the DR line. The secondary communication period occurs four shift clocks after completion of primary communications.

2.9.2 Two 8-Bit Bytes (Byte Mode)

The serial port interfaces directly with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows:

1. $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ are brought low.
2. One 8-bit word is transmitted and one 8-bit word is received.
3. $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ are brought low.
4. $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ emit positive frame-sync pulses that are four shift clock cycles wide.
5. One 8-bit byte is transmitted and one 8-bit byte is received.
6. $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ are brought high.
7. $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ are brought high.

2.9.3 Synchronous Operating Frequencies

The synchronous operating frequencies are determined by the following equations.

Switched capacitor filter (SCF) frequencies (see Figure 2–1):

$$\text{Low-pass SCF clock frequency (D/A and A/D channels)} = \frac{\text{master clock frequency}}{T(A) \times 2}$$

$$\text{High-pass SCF clock frequency (A/D channel)} = \text{A/D conversion frequency}$$

$$\text{Conversion frequency (A/D and D/A channels)} = \frac{\text{low-pass SCF clock frequency}}{T(B)}$$

$$= \frac{\text{master clock frequency}}{T(A) \times 2 \times T(B)}$$

NOTE: T(A), T(B), R(A), and R(B) are the contents of the TA, TB, RA, and RB registers, respectively.

2.10 Asynchronous Operation

When the transmit and the receive sections are operated asynchronously, the low-pass and band-pass filter clocks are independently generated from the master clock. The D/A and the A/D conversion timing is also determined independently.

D/A timing is set by the counters and registers described in synchronous operation, but the RA and RB registers are substituted for the TA and TB registers to determine the A/D channel sample rate and the A/D path switched-capacitor filter frequencies. Asynchronous operation is selected by control register bit D5 being zero.

2.10.1 One 16-Bit Word (Word Mode)

The serial port interfaces directly with the serial ports of the TMS32020, TMS320C25, and TMS320C30 and communicates with 16-bit word formats. The operation sequence is as follows:

1. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ are brought low by the TLC32046 AIC.
2. One 16-bit word is transmitted or one 16-bit word is received.
3. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ are brought high.
4. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ emit low-going pulses one shift clock wide. $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ are valid in either the word or byte mode only.

2.10.2 Two 8-Bit Bytes (Byte Mode)

The serial port interfaces directly with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operating sequence is as follows:

1. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ are brought low by the TLC32046 AIC.
2. One byte is transmitted or received.
3. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ are brought low.
4. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ are brought high for four shift clock periods and then brought low.
5. The second byte is transmitted or received.
6. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ are brought high.
7. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ are brought high.

2.10.3 Asynchronous Operating Frequencies

The asynchronous operating frequencies are determined by the following equations.

Switched-capacitor filter frequencies (see Figure 2–1):

$$\text{Low-pass D/A SCF clock frequency} = \frac{\text{master clock frequency}}{T(A) \times 2}$$

$$\text{Low-pass A/D SCF clock frequency} = \frac{\text{master clock frequency}}{\text{R(A)} \times 2}$$

$$\text{High-pass SCF clock frequency (A/D channel)} = \text{A/D conversion frequency} \quad (2)$$

Conversion frequency:

$$\text{D/A conversion frequency} = \frac{\text{low-pass D/A SCF clock frequency}}{\text{T(B)}}$$

$$\text{A/D conversion frequency} = \frac{\text{low-pass A/D SCF clock frequency (for low pass receive filter)}}{\text{R(B)}} \quad (3)$$

NOTE: T(A), T(B), R(A), and R(B) are the contents of the TA, TB, RA, and RB registers, respectively.

2.11 Operation of TLC32046 With Internal Voltage Reference

The internal reference of the TLC32046 eliminates the need for an external voltage reference and provides overall circuit cost reduction. The internal reference eases the design task and provides complete control of the IC performance. The internal reference is brought out to REF. To keep the amount of noise on the reference signal to a minimum, an external capacitor can be connected between REF and ANLG GND.

2.12 Operation of TLC32046 With External Voltage Reference

REF can be driven from an external reference circuit. This external circuit must be capable of supplying 250 μA and must be protected adequately from noise and crosstalk from the analog input.

2.13 Reset

A reset function is provided to initiate serial communications between the AIC and DSP and to allow fast, cost-effective testing during manufacturing. The reset function initializes all AIC registers, including the control register. After a negative-going pulse on $\overline{\text{RESET}}$, the AIC is initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX Data Word Format section). After RESET, TA=TB=RA=RB=18 (or 12 hexadecimal), TA′=RA′=01 (hexadecimal), the A/D high-pass filter is inserted, the loop-back function is deleted, AUX IN+ and AUX IN− are disabled, transmit and receive sections are in synchronous operation, programmable gain is set to 1, the on-board (sin x)/x correction filter is not selected, D10OUT is set to 0, and D11OUT is set to 0.

2.14 Loopback

This feature allows the circuit to be tested remotely. In loopback, OUT+ and OUT− are internally connected to IN+ and IN−. The DAC bits (D15 to D2), which are transmitted to DX, can be compared with the ADC bits (D15 to D2), received from DR. The bits on DR equal the bits on DX. However, there is some difference in these bits due to the ADC and DAC output offsets.

The loopback feature is implemented with digital signal processor control by transmitting a logic 1 for data bit D3 in the DX secondary communication to the control register (see Table 2–3).

2.15 Communications Word Sequence

In the dual-word (telephone interface) mode, there are two data words that are presented to the DSP or µP from the DR terminal. The first data word is the ADC conversion result occurring during the FSR time, and the second is the serial data applied to DATA-DR during the FSD time. FSR is not asserted during secondary communications and FSD is not asserted during primary communications.

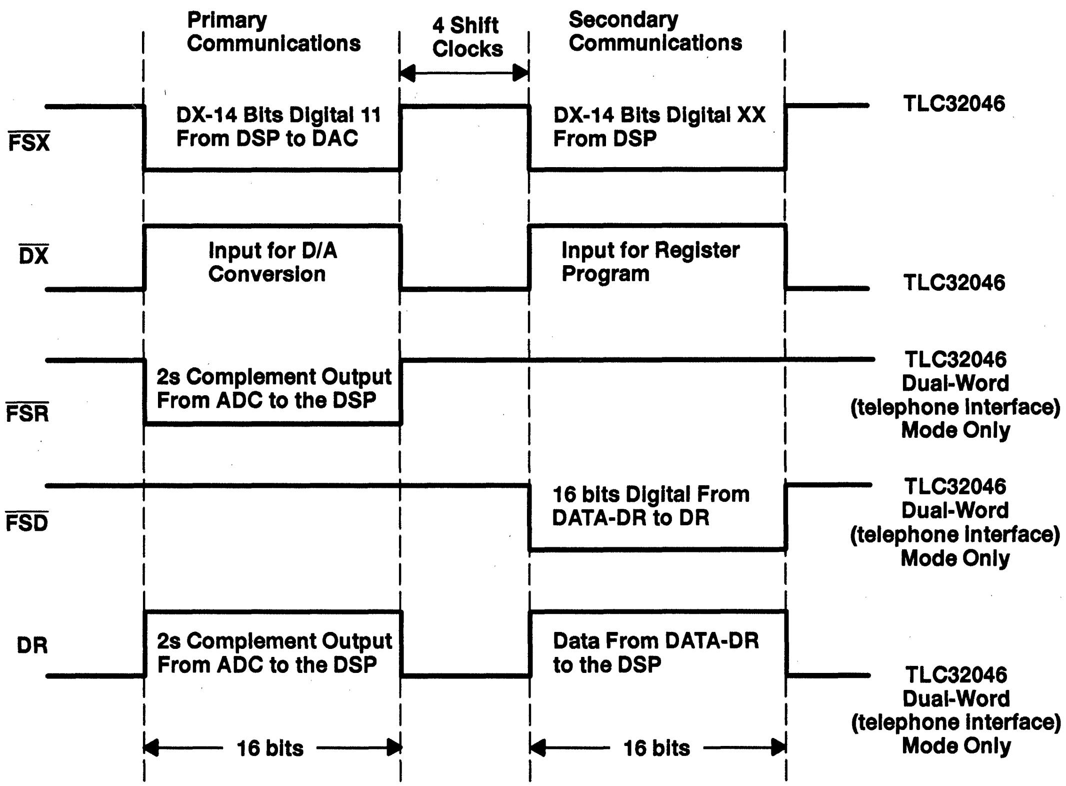


Figure 2–2. Primary and Secondary Communications Word Sequence

2.15.1 DR Word Bit Pattern

The data word is the 14-bit conversion result of the receive channel to the processor in 2s complement format. With 16-bit processors, the data is 16 bits long with the two LSBs at zero.

A/D MSB
1st bit sent ↓ | A/D LSB ↓

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

2.15.2 Primary DX Word Bit Pattern

Using 8-bit processors, the data word is transmitted in the same order as one 16-bit word, but as two bytes with the two LSBs of the second byte set to zero.

A/D OR D/A MSB

1st bit sent — 1st bit sent of 2nd byte — A/D or D/A LSB

↓ ↓ ↓

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 2–2. Primary DX Serial Communication Protocol

FUNCTIONS	D1	D0
D15 (MSB)-D2 → DAC Register. TA → TX(A), RA → RX(A) (see Figure 2–1). TB → TX(B), RB → RX(B) (see Figure 2–1).	0	0
D15 (MSB)-D2 → DAC Register. TA+TA′ → TX(A), RA+RA′ → RX(A) (see Figure 2–1). TB → TX(B), RB → RX(B) (see Figure 2–1). The next D/A and A/D conversion period is changed by the addition of TA′ and RA′ master clock cycles, in which TA′ and RA′ can be positive, negative, or zero (refer to Table 2–4).	0	1
D15 (MSB)-D2 → DAC Register. TA–TA′ → TX(A), RA–RA′ → RX(A) (see Figure 2–1). TB → TX(B), RB → RX(B) (see Figure 2–1). The next D/A and A/D conversion period is changed by the subtraction of TA′ and RA′ master clock cycles, in which TA′ and RA′ can be positive, negative, or zero (refer to Table 2–4).	1	0
D15 (MSB)-D2 → DAC Register. TA → TX(A), RA → RX(A) (see Figure 2–1). TB → TX(B), RB → RX(B) (see Figure 2–1). After a delay of four shift cycles, a secondary transmission follows to program the AIC to operate in the desired configuration. In the telephone interface mode, data on DATA DR is routed to DR during secondary transmission.	1	1

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (primary communications) to the AIC initiates secondary communications upon completion of the primary communications. When the primary communication is complete, $\overline{\text{FSX}}$ remains high for four SHIFT CLOCK cycles and then goes low and initiates the secondary communication. The timing specifications for the primary and secondary communications are identical. In this manner, the secondary communication, if initiated, is interleaved between successive primary communications. This interleaving prevents the secondary communication from interfering with the primary communications and DAC timing. This prevents the AIC from skipping a DAC output. $\overline{\text{FSR}}$ is not asserted during secondary communications activity. However, in the dual-word (telephone interface) mode, $\overline{\text{FSD}}$ is asserted during secondary communications but not during primary communications.

2.15.3 Secondary DX Word Bit Pattern

D/A MSB 1st bit sent ↓								1st bit sent of 2nd byte ↓					D/A LSB ↓		
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 2–3. Secondary DX Serial Communication Protocol

FUNCTIONS	D1	D0
D13 (MSB)-D9 → TA , 5 bits unsigned binary (see Figure 2–1). D6 (MSB)-D2 → RA, 5 bits unsigned binary (see Figure 2–1). D15, D14, D8, and D7 are unassigned.	0	0
D14 (sign bit)-D9 → TA′, 6 bits 2s complement (see Figure 2–1). D7 (sign bit)-D2 → RA′, 6 bits 2s complement (see Figure 2–1). D15 and D8 are unassigned.	0	1
D14 (MSB)-D9 → TB, 6 bits unsigned binary (see Figure 2–1). D7 (MSB)-D2 → RB, 6 bits unsigned binary (see Figure 2–1). D15 and D8 are unassigned.	1	0
D2 = 0/1 deletes/inserts the A/D high-pass filter. D3 = 0/1 deletes/inserts the loopback function. D4 = 0/1 disables/enables AUX IN+ and AUX IN–. D5 = 0/1 asynchronous/synchronous transmit and receive sections. D6 = 0/1 gain control bits (see Table 4–1). D7 = 0/1 gain control bits (see Table 4–1). D9 = 0/1 delete/insert on-board second-order (sinx)/x correction filter D10 = 0/1 output to D10OUT (dual-word (telephone interface) mode) D11 = 0/1 output to D11OUT (dual-word (telephone interface) mode) D8, D12–D15 are unassigned.	1	1

2.16 Reset Function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After power has been applied to the AIC, a negative-going pulse on $\overline{\text{RESET}}$ initializes the AIC registers to provide a 16-kHz A/D and D/A conversion rate for a 10.368-MHz master clock input signal. Also, the pass-bands of the A/D and D/A filters are 300 Hz to 7200 Hz and 0 Hz to 7200 Hz, respectively; therefore, the filter bandwidths are half those shown in the filter transfer function specification section. The AIC, except the CONTROL register, is initialized as follows (see AIC DX Data Word Format section):

REGISTER	TA	TA′	TB	RA	RA′	RB
INITIALIZED VALUE (HEX)	12	01	12	12	01	12

The CONTROL register bits are reset as follows (see Table 2–3):

D11 = 0, D10 = 0, D9 = 1, D7 = 1, D6 = 1, D5 = 1, D4 = 0, D3 = 0, D2 = 1

This initialization allows normal serial port communications to occur between the AIC and the DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA′, and TB register need to be programmed. Both transmit and receive timing are synchronously derived from these registers (see the Terminal Functions and DX Serial Data Word Format sections).

Figure 2–3 shows a circuit that provides a reset on power-up when power is applied in the sequence given in the power-up sequence section. The circuit depends on the power supplies reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.

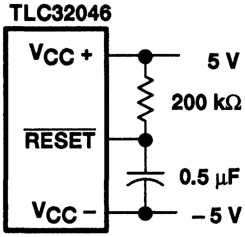


Figure 2–3. Reset on Power-Up Circuit

2.17 Power-Up Sequence

To ensure proper operation of the AIC and as a safeguard against latch-up, it is recommended that Schottky diodes with forward voltages less than or equal to 0.4 V be connected from V_{CC-} to ANLG GND and from V_{CC-} to DGTL GND. In the absence of such diodes, power is applied in the following sequence: ANLG GND and DGTL GND, V_{CC-}, then V_{CC+} and V_{DD}. Also, no input signal is applied until after power-up.

2.18 AIC Register Constraints

The following constraints are placed on the contents of the AIC registers:

1. TA register must be ≥ 4 in word mode (WORD/BYTE= high).
2. TA register must be ≥ 5 in byte mode (WORD/BYTE= low).
3. TA′ register can be either positive, negative, or zero.
4. RA register must be ≥ 4 in word mode (WORD/BYTE = high).
5. RA register must be ≥ 5 in byte mode (WORD/BYTE = low).
6. RA′ register can be either positive, negative, or zero.
7. (TA register ± TA′ register) must be > 1.
8. (RA register ± RA′ register) must be > 1.
9. TB register must be ≥ 15.
10. RB register must be ≥ 15.

2.19 AIC Responses to Improper Conditions

The AIC has provisions for responding to improper conditions. These improper conditions and the response of the AIC to these conditions are presented in Table 2–4.

Table 2–4. AIC Responses to Improper Conditions

IMPROPER CONDITION	AIC RESPONSE
TA register + TA′ register = 0 or 1 TA register − TA′ register = 0 or 1	Reprogram TX(A) counter with TA register value
TA register + TA′ register < 0	MODULO 64 arithmetic is used to ensure that a positive value is loaded into TX(A) counter, i.e., TA register + TA′ register + 40 HEX is loaded into TX(A) counter.
RA register + RA′ register = 0 or 1 RA register − RA′ register = 0 or 1	Reprogram RX(A) counter with RA register value
RA register + RA′ register = 0 or 1	MODULO 64 arithmetic is used to ensure that a positive value is loaded into RX(A) counter, i.e., RA register + RA′ register + 40 HEX is loaded into RX(A) counter.
TA register = 0 or 1 RA register = 0 or 1	AIC is shut down. Reprogram TA or RA registers after a reset.
TA register < 4 in word mode TA register < 5 in byte mode RA register < 4 in word mode RA register < 5 in byte mode	The AIC serial port no longer operates. Reprogram TA or RA registers after a reset.
TB register < 15	Reprogram TB register with 12 HEX
RB register < 15	Reprogram RB register with 12 HEX
AIC and DSP cannot communicate	Hold last DAC output

2.20 Operation With Conversion Times Too Close Together

If the difference between two successive D/A conversion frame syncs is less than 1/25 kHz, the AIC operates improperly. In this situation, the second D/A conversion frame sync occurs too quickly, and there is not enough time for the ongoing conversion to be completed. This situation can occur if the A and B registers are improperly programmed or if the A + A′ register result is too small. When incrementally adjusting the conversion period via the A + A′ register options, the designer should not violate this requirement (see Figure2–4).

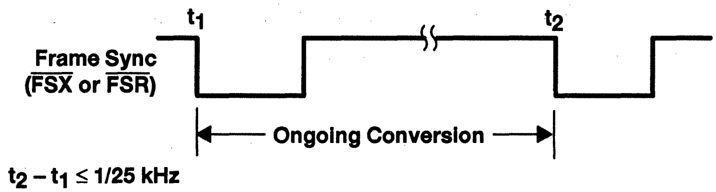


Figure 2–4. Conversion Times Too Close Together

2.21 More Than One Receive Frame Sync Occurring Between Two Transmit Frame Syncs – Asynchronous Operation

When incrementally adjusting the conversion period via the A + A′ or A – A′ register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during an $\overline{FSX}$ frame sync. The ongoing conversion period is then adjusted; however, either receive conversion period A or conversion period B can be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. If there is sufficient time between t_1 and t_2, the receive conversion period adjustment is performed during receive conversion period A. Otherwise, the adjustment is performed during receive conversion period B.

The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent $\overline{FSX}$ frame (see Figure 2–5).

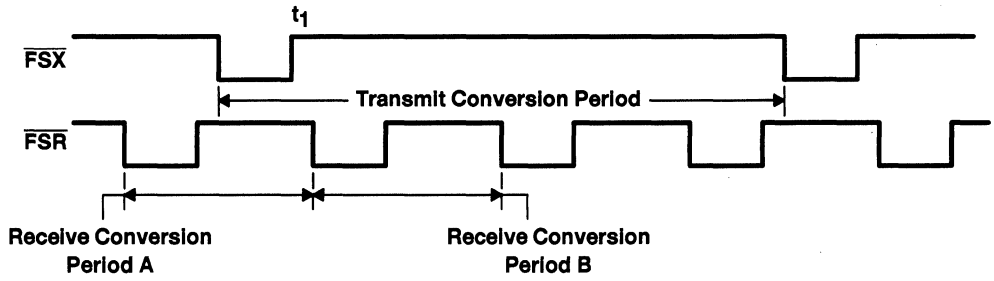


Figure 2–5. More Than One Receive Frame Sync Between Two Transmit Frame Syncs

2.22 More Than One Transmit Frame Sync Occurring Between Two Receive Frame Syncs – Asynchronous Operation

When incrementally adjusting the conversion period via the A + A′ or A – A′ register options, a specific protocol must be followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during an $\overline{FSX}$ frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment as shown in Figure 2–6. When the adjustment command is issued during transmit conversion period A, receive conversion period A is adjusted if there is sufficient time between t_1 and t_2. If there is not sufficient time between t_1 and t_2, receive conversion period B is adjusted. The third option is that the receive portion of an adjustment command can be ignored if the adjustment command is sent during a receive conversion period, which is adjusted due to a prior adjustment command. For example, if adjustment commands are issued during transmit conversion periods A, B, and C, the first two commands may cause receive conversion periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during receive conversion period B, which already is adjusted via the transmit conversion period B adjustment command.

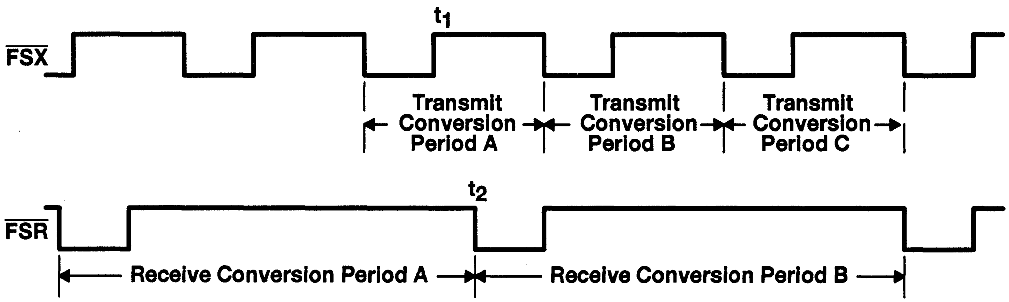


Figure 2–6. More Than One Transmit Frame Sync Between Two Receive Frame Syncs

2.23 More than One Set of Primary and Secondary DX Serial Communications Occurring Between Two Receive Frame Syncs (See DX Serial Data Word Format section) – Asynchronous Operation

The TA, TA′, TB, and control register information that is transmitted in the secondary communication is accepted and applied during the ongoing transmit conversion period. If there is sufficient time between t_1 and t_2, the TA, RA′, and RB register information, sent during transmit conversion period A, is applied to receive conversion period A; otherwise, this information is applied during receive conversion period B. If RA, RA′, and RB register information has been received and is being applied during an ongoing conversion period, any subsequent RA, RA′, or RB information received during this receive conversion period is disregarded (see Figure 2–7).

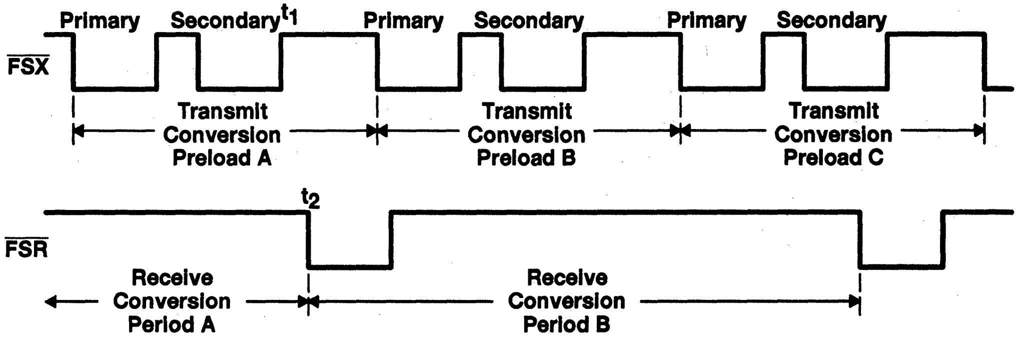


Figure 2–7. More Than One Set of Primary and Secondary DX Serial Communications Between Two Receive Frame Syncs

2.24 System Frequency Response Correction

The (sin x)/x correction for the DAC zero-order sample-and-hold output can be provided by an on-board second-order (sin x)/x correction filter (see Functional Block Diagram). This (sin x)/x correction filter can be inserted into or omitted from the signal path by digital-signal-processor control (data bit D9 in the DX secondary communications). When inserted, the (sin x)/x correction filter precedes the switched-capacitor low-pass filter. When the TB register (see Figure 2–1) equals 15, the correction results of Figures 5–5, 5–6, and 5–7 can be obtained.

The (sin x)/x correction [see section (sin x)/x] can also be accomplished by disabling the on-board second-order correction filter and performing the (sin x)/x correction in digital signal processor software. The system frequency response can be corrected via DSP software to ± 0.1 dB accuracy to a band edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, that requires seven TMS320 instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the (Sin x)/x Correction Section for more details).

2.25 (Sin x)/x Correction

If the designer does not wish to use the on-board second-order (sin x)/x correction filter, correction can be accomplished in digital signal processor (DSP) software. (Sin x)/x correction can be accomplished easily and efficiently in digital signal processor software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results shown are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires seven instruction cycles per sample on the TMS320 DS. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction adds a slight amount of group delay at the upper edge of the 300-Hz to 3000-Hz band.

2.26 (Sin x)/x Roll-Off for a Zero-Order Hold Function

The (sin x)/x roll-off error for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in Table 2–5 (see Figure 5–7).

Table 2–5. (sin x)/x Roll-Off Error

f_s (Hz)	Error = 20 log $\frac{\sin \pi f/f_s}{\pi f/f_s}$ f = 3000 Hz (dB)
7200	−2.64
8000	−2.11
9600	−1.44
14400	−0.63
16000	−0.50
19200	−0.35
25000	−0.21

The actual AIC (sin x)/x roll-off is slightly less than the figures in Table 2–5 because the AIC has less than 100% duty cycle hold interval.

2.27 Correction Filter

To externally compensate for the (sin x)/x roll-off of the AIC, a first-order correction filter can be implemented as shown in Figure 2–8.

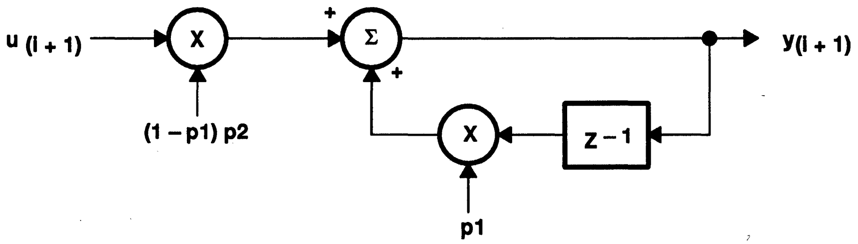


Figure 2–8. First-Order Correction Filter

The difference equation for this correction filter is:

$$y_{(i+1)} = p2 \cdot (1 - p1) \cdot u_{(i+1)} + p1 \cdot y_{(i)} \tag{4}$$

where the constant p1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$| H (f) |^2 = \frac{(p2)^2 \, V \, (1-p1)^2}{1-2 \, V \, p1 \, V \cos (2p \, f/f_s) + (p1)^2} \tag{5}$$

2.28 Correction Results

Table 2-6 shows the optimum p values and the corresponding correction results for 8000-Hz and 9600-Hz sampling rates (see Figures 5–8, 5–9, and 5–10).

Table 2–6. (Sin x)/x Correction Table for f_s = 8000 Hz and f_s = 9600 Hz

f (Hz)	ROLL-OFF ERROR (dB) f_s = 8000 Hz p1 = −0.14813 p2 = 0.9888	ROLL-OFF ERROR (dB) f_s = 9600 Hz p1 = −0.1307 p2 = 0.9951
300	−0.099	−0.043
600	−0.089	−0.043
900	−0.054	0
1200	−0.002	0
1500	0.041	0
1800	0.079	0.043
2100	0.100	0.043
2400	0.091	0.043
2700	−0.043	0
3000	−0.102	−0.043

2.29 TMS320 Software Requirements

The digital correction filter equation can be written in state variable form as follows:

$$y_{(i+1)} = y_{(i)} \cdot k1 + u_{(i+1)} \cdot k2$$

Where

k1 = p1

k2 = (1 − p1) p2

y(i) = filter state

u(i+1) = next I/O sample

The coefficients k1 and k2 must be represented as 16-bit integers. The SACH instruction (with the proper shift) yields the correct result. With the assumption that the TMS320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)

Supply voltage range, V_{CC+} (see Note 1) .... −0.3 V to 15 V
Supply voltage range, V_{DD} .... −0.3 V to 15 V
Output voltage range, V_O .... −0.3 V to 15 V
Input voltage range, V_I .... −0.3 V to 15 V
Digital ground voltage range .... −0.3 V to 15 V
Operating free-air temperature range: TLC32046C .... 0°C to 70°C
TLC32046I .... −40°C to 85°C
TLC32046M .... −55°C to 125°C
Storage temperature range: TLC32046C, TLC32046I .... −40°C to 125°C
TLC32046M .... −65°C to 150°C
Case temperature for 10 seconds: FN or FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds:
N or J package .... 260°C

NOTE 1: Voltage values for maximum ratings are with respect to V_{CC-}.

3.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} (see Note 2)		4.75	5	5.25	V
Supply voltage, V_{CC-} (see Note 2)		−4.75	−5	−5.25	V
Digital supply voltage, V_{DD} (see Note 2)		4.75	5	5.25	V
Digital ground voltage with respect to ANLG GND, DGTL GND			0		V
Reference input voltage, $V_{ref(ext)}$ (see Note 2)		2		4	V
High-level input voltage, V_{IH}		2		V_{DD}+0.3	V
Low-level input voltage, V_{IL} (see Note 3)		−0.3		0.8	V
Load resistance at OUT+ and/or OUT−, R_L		300			Ω
Load capacitance at OUT+ and/or OUT−, C_L				100	pF
MSTR CLK frequency (see Note 4)			5	10.368	MHz
Analog input amplifier common mode input voltage (see Note 5)				±1.5	V
A/D or D/A conversion rate				25	kHz
Operating free-air temperature range, T_A	TLC32046C	0		70	°C
	TLC32046I	−40		85	
	TLC32046M	−55		125	

NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+}, and V_{CC-} are with respect to ANLG GND. Voltages at digital inputs and outputs and V_{DD} are with respect to DGTL GND.
3. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data manual for logic voltage levels only.
4. The band-pass switched-capacitor filter (SCF) specifications apply only when the low-pass section SCF clock is 288 kHz and the high-pass section SCF clock is 16 kHz. If the low-pass SCF clock is shifted from 288 kHz, the low-pass roll-off frequency shifts by the ratio of the low-pass SCF clock to 288 kHz. If the high-pass SCF clock is shifted from 16 kHz, the high-pass roll-off frequency shifts by the ratio of the high-pass SCF clock to 16 kHz. Similarly, the low-pass switched-capacitor filter (SCF) specifications apply only when the SCF clock is 288 kHz. If the SCF clock is shifted from 288 kHz, the low-pass roll-off frequency shifts by the ratio of the SCF clock to 288 kHz.
5. This range applies when (IN+ − IN−) or (AUX IN+ − AUX IN−) equals ± 6 V.

3.3 Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, V_{CC+} = 5 V, V_{CC-} = –5 V, V_{DD} = 5 V (Unless Otherwise Noted)

3.3.1 Total Device, MSTR CLK Frequency = 5.184 MHz, Outputs Not Loaded

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 4.75 V, I_{OH} = –300 μA	2.4			V
V_{OL}	Low-level output voltage		V_{DD} = 4.75 V, I_{OL} = 2 mA			0.4	V
I_{CC+}	Supply current from V_{CC+}	TLC32046C				35	mA
		TLC32046I				40	
		TLC32046M				45	
I_{CC-}	Supply current from V_{CC-}	TLC32046C				–35	mA
		TLC32046I				–40	
		TLC32046M				–45	
I_{DD}	Supply current from V_{DD}					7	mA
V_{ref}	Internal reference output voltage	TLC32046M		2.9		3.3	V
αV_{ref}	Temperature coefficient of internal reference voltage				250		ppm/°C
r_o	Output resistance at REF				100		kΩ

3.3.2 Power Supply Rejection and Crosstalk Attenuation

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC+} or V_{CC-} supply voltage rejection ratio, receive channel	f = 0 kHz to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at DR (ADC output)		30		dB
	f = 30 kHz to 50 kHz			45		
V_{CC+} or V_{CC-} supply voltage rejection ratio, transmit channel (single-ended)	f = 0 kHz to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at OUT+		30		dB
	f = 30 kHz to 50 kHz			45		
Crosstalk attenuation, transmit-to-receive (single-ended)	TLC32046C, I			80		dB
	TLC32046M		60	80		
Crosstalk attenuation, receive-to-transmit (single-ended)	TLC32046M		70	80		dB

3.3.3 Serial Port

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –300 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
I_I	Input current				±10	μA
I_I	Input current, DATA-DR/CONTROL				±100	μA
C_i	Input capacitance			15		pF
C_o	Output capacitance			15		pF

† All typical values are at T_A = 25°C.

3.3.4 Receive Amplifier Input

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	A/D converter offset error (filters in)			10	70	mV
CMRR	Common-mode rejection ratio at IN+, IN–, or AUX IN+, AUX IN–	See Note 6		55		dB
r_i	Input resistance at IN+, IN– or AUX IN+, AUX IN+, AUX IN–, REF			100		kΩ

NOTE 6: The test condition is a 0-dBm, 1-kHz input signal with a 16-kHz conversion rate.

3.3.5 Transmit Filter Output

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset voltage at OUT+ or OUT– (single-ended relative to ANLG GND)	TLC32046C, I			15	80	mV
		TLC32046M			15	85	mV
V_{OM}	Maximum peak output voltage swing across R_L at OUT+ or OUT– (single-ended)	TLC32046C, I	$R_L \geq 300\ \Omega$, Offset voltage = 0	±3			V
	Maximum peak output voltage swing between OUT+ and OUT– (differential output)		$R_L \geq 600\ \Omega$	±6			V

† All typical values are at $T_A = 25°C$.

3.3.6 Receive and Transmit Channel System Distortion, SCF Clock Frequency = 288 kHz (see Note 7)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Attenuation of second harmonic of A/D input signal	Single-ended	$V_I = -0.1$ dB to -24 dB		70		dB
	Differential		62	70		
Attenuation of third and higher harmonics of A/D input signal	Single-ended			65		dB
	Differential		57	65		
Attenuation of second harmonic of D/A input signal	Single-ended	$V_I = -0$ dB to -24 dB		70		dB
	Differential		62	70		
Attenuation of third and higher harmonics of D/A input signal	Single-ended			65		dB
	Differential		57	65		

† All typical values are at $T_A = 25°C$.

3.3.7 Receive Channel Signal-to-Distortion Ratio (see Note 7)

PARAMETER	TEST CONDITIONS	$A_V = 1$‡		$A_V = 2$‡		$A_V = 4$‡		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
A/D channel signal-to-distortion ratio	$V_I = -6$ dB to -0.1 dB	58		§		§		dB
	$V_I = -12$ dB to -6 dB	58		58		§		
	$V_I = -18$ dB to -12 dB	56		58		58		
	$V_I = -24$ dB to -18 dB	50		56		58		
	$V_I = -30$ dB to -24 dB	44		50		56		
	$V_I = -36$ dB to -30 dB	38		44		50		
	$V_I = -42$ dB to -36 dB	32		38		44		
	$V_I = -48$ dB to -42 dB	26		32		38		
	$V_I = -54$ dB to -48 dB	20		26		32		

‡ A_V is the programmable gain of the input amplifier.

§ Measurements under these conditions are unreliable due to overrange and signal clipping.

NOTE 7: The test condition is a 1-kHz input signal with a 16-kHz conversion rate. The load impedance for the DAC is 600 Ω. Input and output voltages are referred to V_{ref}.

3.3.8 Transmit Channel Signal-to-Distortion Ratio (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
D/A channel signal-to-distortion ratio	$V_I = -6$ dB to -0.1 dB	58		dB
	$V_I = -12$ dB to -6 dB	58		
	$V_I = -18$ dB to -12 dB	56		
	$V_I = -24$ dB to -18 dB	50		
	$V_I = -30$ dB to -24 dB	44		
	$V_I = -36$ dB to -30 dB	38		
	$V_I = -42$ dB to -36 dB	32		
	$V_I = -48$ dB to -42 dB	26		
	$V_I = -54$ dB to -48 dB	20		

NOTE 7: The test condition is a 1-kHz input signal with a 16-kHz conversion rate. The load impedance for the DAC is 600 Ω. Input and output voltages are referred to V_{ref}.

3.3.9 Receive and Transmit Gain and Dynamic Range (see Note 8)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit gain tracking error	C, I	$V_O = -48$ dB to 0 dB signal range		±0.05	±0.15	dB
Receive gain tracking error	C, I	$V_I = -48$ dB to 0 dB signal range		±0.05	±0.15	dB
Transmit gain tracking error	M	$V_O = -48$ dB to 0 dB signal range, $T_A = 25°C$		±0.05	±0.25	dB
Receive gain tracking error	M	$V_I = -48$ dB to 0 dB signal range, $T_A = 25°C$		±0.05	±0.25	dB
Transmit gain tracking error	M	$V_O = -48$ dB to 0 dB signal range, $T_A = -55°C$ TO 125°C			±0.4	dB
Receive gain tracking error	M				±0.4	dB

NOTE 8: Gain tracking is relative to the absolute gain at 1 kHz and 0 dB (0 dB relative to V_{ref}).

3.3.10 Receive Channel Band-Pass Filter Transfer Function, SCF f_{clock} = 288 kHz, Input (IN+ – IN–) Is A ±3-V Sine Wave‡ (see Note 9)

PARMETER	TEST CONDITION	FREQUENCY	ADJUSTMENT	MIN	TYP†	MAX	UNIT
Filter gain	Input signal reference is 0 dB	f ≤ 100 Hz	K1 × 0 dB	−33	−29	−25	dB
		f = 200 Hz	K1 × −0.26 dB	−4	−2	−1	
		f = 300 Hz to 6200 Hz	K1 × 0 dB	−0.25	0	0.25	
		f = 6200 Hz to 6600 Hz	K1 × 0 dB	−0.3	0	0.3	
		f = 6600 Hz to 7300 Hz	K1 × 0 dB		0	0.5	
		f = 7600 Hz	K1 × 2.3 dB		−2	−0.5	
		f = 8000 Hz	K1 × 2.7 dB		−16	−14	
		f ≥ 8800 Hz	K1 × 3.2 dB			−40	
		f ≥ 10000 Hz	K1 × 0 dB			−65	

3.3.11 Receive and Transmit Channel Low-Pass Filter Transfer Function, SCF f_{clock} = 288 kHz (see Note 9)

	TEST CONDITION	FREQUENCY RANGE	ADJUSTMENT ADDEND‡	MIN	TYP†	MAX	UNIT
Filter gain	Input signal reference is 0 dB	f = 0 Hz to 6200 Hz	K1 × 0 dB	−0.25	0	0.25	dB
		f = 6200 Hz to 6600 Hz	K1 × 0 dB	−0.3	0	0.3	
		f = 6600 Hz to 7300 Hz	K1 × 0 dB	−0.5	0	0.5	
		f = 7600 Hz	K1 × 2.3 dB		−2	−0.5	
		f = 8000 Hz	K1 × 2.7 dB		−16	−14	
		f ≥ 8800 Hz	K1 × 3.2 dB			−40	
		f ≥ 10000 Hz	K1 × 0 dB			−65	

† All typical values are at T_A = 25°C.

‡ The MIN, TYP, and MAX specifications are given for a 288-kHz SCF clock frequency. A slight error in the 288-kHz SCF may result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where K1 = 100 • [(SCF frequency – 288 kHz)/288 kHz]. For errors greater than 0.25%, see Note 9.

NOTE 9: The filter gain outside of the pass band is measured with respect to the gain at 1 kHz (2 kHz for M version). The filter gain within the pass band is measured with respect to the average gain within the pass band. The pass bands are 300 Hz to 7200 Hz and 0 to 7200 Hz for the band-pass and low-pass filters, respectively. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

3.4 Operating Characteristics Over Recommended Operating Free-Air Temperature Range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V

3.4.1 Receive and Transmit Noise (measurement includes low-pass and band-pass switched-capacitor filters)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit noise	Broadband with (sin x)/x	DX input = 00000000000000, Constant input code		250	500	μVrms
	Broadband without (sin x)/x			200	450	
	0 to 30 kHz with (sin x)/x			200	400	
	0 to 30 kHz without (sin x)/x			200	400	
	0 to 3.4 kHz with (sin x)/x			180	300	
	0 to 3.4 kHz without (sin x)/x			160	300	
	0 to 6.8 kHz with (sin x)/x (wide-band operation with 7.2 kHz roll-off)			180	350	
	0 to 6.8 kHz without (sin x)/x (wide-band operation with 7.2 kHz roll-off)			160	350	
Receive noise (see Note 10)		Inputs grounded, Gain = 1		300	500	μVrms
				18		dBrnc0

† All typical values are at T_A = 25°C.
NOTE 10: The noise is computed by statistically evaluating the digital output of the A/D converter.

3.5 Timing Requirements

3.5.1 Serial Port Recommended Input Signals, TLC32046C and TLC32046I

PARAMETER		MIN	MAX	UNIT
$t_{c(MCLK)}$	Master clock cycle time	95		ns
$t_{r(MCLK)}$	Master clock rise time		10	ns
$t_{f(MCLK)}$	Master clock fall time		10	ns
	Master clock duty cycle	25%	75%	
	$\overline{\text{RESET}}$ pulse duration (see Note 11)	800		ns
$t_{su(DX)}$	DX setup time before SCLK↓	20		ns
$t_{h(DX)}$	DX hold time after SCLK↓	$t_{c(SCLK)}/4$		ns

NOTE 11: $\overline{\text{RESET}}$ pulse duration is the amount of time that the $\overline{\text{RESET}}$ is held below 0.8 V after the power supplies have reached their recommended values.

3.5.2 Serial Port Recommended Input Signals, TLC32046M

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{c(MCLK)}$	Master clock cycle time	95			ns
$t_{r(MCLK)}$	Master clock rise time		10		ns
$t_{f(MCLK)}$	Master clock fall time		10		ns
	Master clock duty cycle		50%		
	$\overline{\text{RESET}}$ pulse duration (see Note 11)	800			ns
$t_{su(DX)}$	DX setup time before SCLK↓	28			ns
$t_{h(DX)}$	DX hold time after SCLK↓	$t_{c(SCLK)}/4$			ns

NOTE 11: $\overline{\text{RESET}}$ pulse duration is the amount of time that the $\overline{\text{RESET}}$ is held below 0.8 V after the power supplies have reached their recommended values.

3.5.3 Serial Port – AIC Output Signals, C_L = 30 pF for SHIFT CLK Output, C_L = 15 pF For All Other Outputs, TLC32046C and TLC32046I

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time	380			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time		3	8	ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time		3	8	ns
	Shift clock (SCLK) duty cycle	45%		55%	
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{\text{FSR/FSX/FSD}}$↓		30		ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{\text{FSR/FSX/FSD}}$↑		35	90	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑			90	ns
$t_{d(CH-EL)}$	Delay from SCLK↑ to $\overline{\text{EODX/EODR}}$↓ in word mode			90	ns
$t_{d(CH-EH)}$	Delay from SCLK↑ to $\overline{\text{EODX/EODR}}$↑ in word mode			90	ns
$t_{f(EODX)}$	$\overline{\text{EODX}}$ fall time		2	8	ns
$t_{f(EODR)}$	$\overline{\text{EODR}}$ fall time		2	8	ns
$t_{d(CH-EL)}$	Delay from SCLK↑ to $\overline{\text{EODX/EODR}}$↓ in byte mode			90	ns
$t_{d(CH-EH)}$	Delay from SCLK↑ to $\overline{\text{EODX/EODR}}$↑ in byte mode			90	ns
$t_{d(MH-SL)}$	Delay from MSTR CLK↑ to SCLK↓		65	170	ns
$t_{d(MH-SH)}$	Delay from MSTR CLK↑ to SCLK↑		65	170	ns

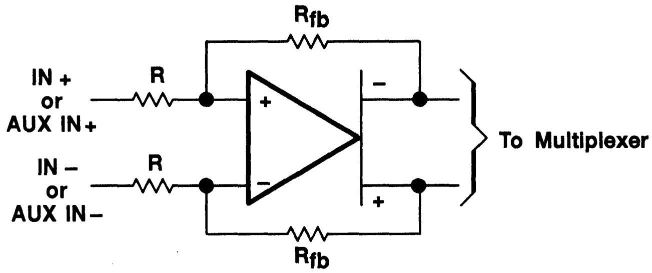
† Typical values are at T_A = 25°C.

3.5.4 Serial Port – AIC Output Signals, C_L = 30 pF for SHIFT CLK Output, C_L = 15 pF For All Other Outputs, TLC32046M

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time	400			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time		3		ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time		3		ns
	Shift clock (SCLK) duty cycle	45%		55%	
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{\text{FSR/FSX/FSD}}$↓		30	250	ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{\text{FSR/FSX/FSD}}$↑		35	250	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑			250	ns
$t_{d(CH-EL)}$	Delay from SCLK↑ to $\overline{\text{EODX/EODR}}$↓ in word mode			250	ns
$t_{d(CH-EH)}$	Delay from SCLK↑ to $\overline{\text{EODX/EODR}}$↑ in word mode			250	ns
$t_{f(EODX)}$	$\overline{\text{EODX}}$ fall time		2		ns
$t_{f(EODR)}$	$\overline{\text{EODR}}$ fall time		2		ns
$t_{d(CH-EL)}$	Delay from SCLK↑ to $\overline{\text{EODX/EODR}}$↓ in byte mode			250	ns
$t_{d(CH-EH)}$	Delay from SCLK↑ to $\overline{\text{EODX/EODR}}$↑ in byte mode			250	ns
$t_{d(MH-SL)}$	Delay from MSTR CLK↑ to SCLK↓		65	170	ns
$t_{d(MH-SH)}$	Delay from MSTR CLK↑ to SCLK↑		65	170	ns

† Typical values are at T_A = 25°C.

4 Parameter Measurement Information



R_{fb} = R for D6 = 1 and D7 = 1
D6 = 0 and D7 = 0
R_{fb} = 2R for D6 = 1 and D7 = 0
R_{fb} = 4R for D6 = 0, and D7 = 1

Figure 4–1. IN+ and IN – Gain Control Circuitry

Table 4–1. Gain Control Table (Analog Input Signal Required for Full-Scale Bipolar A/D Conversion Twos Complement)†

INPUT CONFIGURATIONS	CONTROL REGISTER BITS		ANALOG INPUT‡§	A/D CONVERSION RESULT
	D6	D7		
Differential configuration Analog input = IN+ – IN– = AUX IN+ – AUX IN–	1 0	1 0	$V_{ID} = \pm 6$ V	±full scale
	1	0	$V_{ID} = \pm 3$ V	±full scale
	0	1	$V_{ID} = \pm 1.5$ V	±full scale
Single-ended configuration Analog input = IN+ – ANLG GND = AUX IN+ –ANLG GND	1 0	1 0	$V_I = \pm 3$ V	±half scale
	1	0	$V_I = \pm 3$ V	±full scale
	0	1	$V_I = \pm 1.5$ V	±full scale

† $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $V_{DD} = 5$ V
‡ V_{ID} = Differential Input Voltage, V_I = Input voltage referenced to ground with IN– or AUX IN– connected to GND.
§ In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.

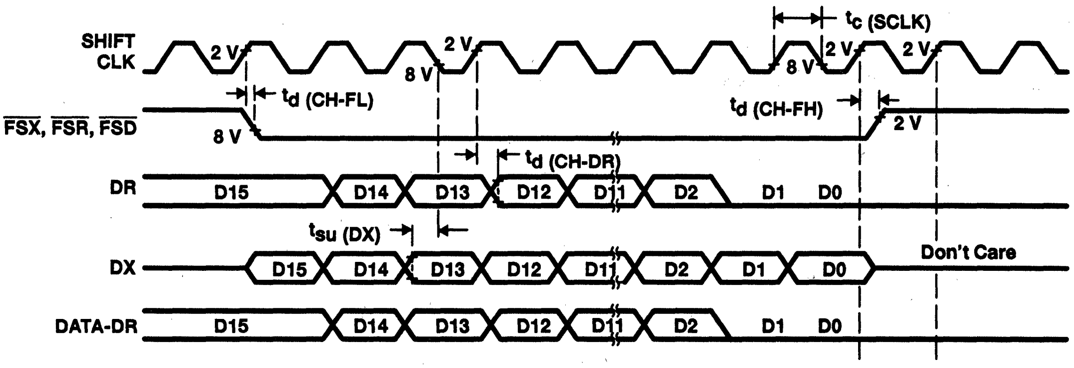


Figure 4–2. Dual-Word (Telephone Interface) Mode Timing

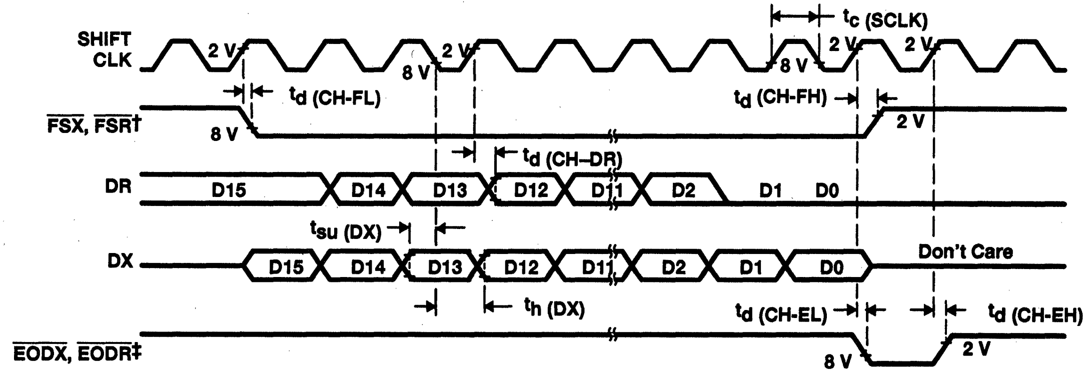


Figure 4–3. Word Timing

† The time between falling edges of $\overline{FSR}$ is the A/D conversion period and the time between falling edges of $\overline{FSX}$ is the D/A conversion period.

‡ In the word format, $\overline{EODX}$ and $\overline{EODR}$ go low to signal the end of a 16-bit data word to the processor. The word-cycle is 20 shift-clocks wide, giving a four-clock period setup time between data words.

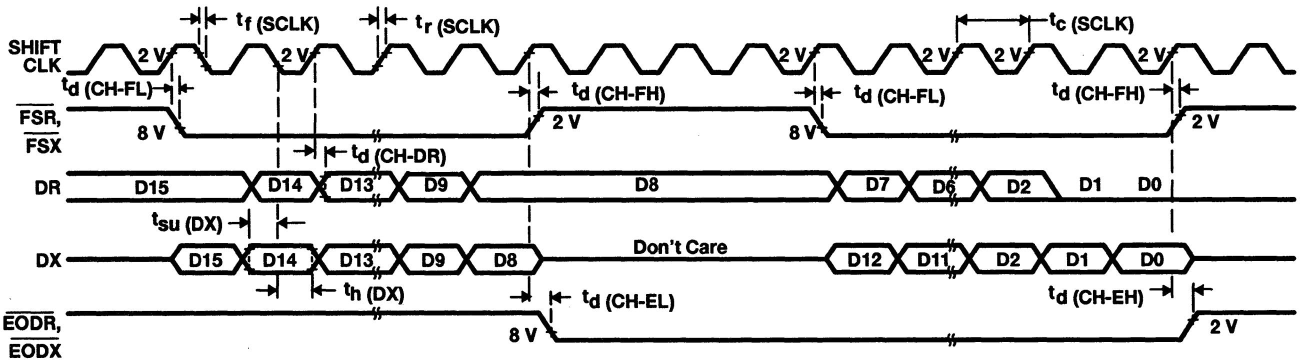


Figure 4–4. Byte-Mode Timing

† The time between falling edges of FSR is the A/D conversion period, and the time between fallling edges of $\overline{FSX}$ is the D/A conversion period.

‡ In the byte mode, when $\overline{EODX}$ or $\overline{EODR}$ is high, the first byte is transmitted or received, and when these signals are low, the second byte is transmitted or received. Each byte-cycle is 12 shift-clocks long, allowing for a four-shift-clock setup time between byte transmissions.

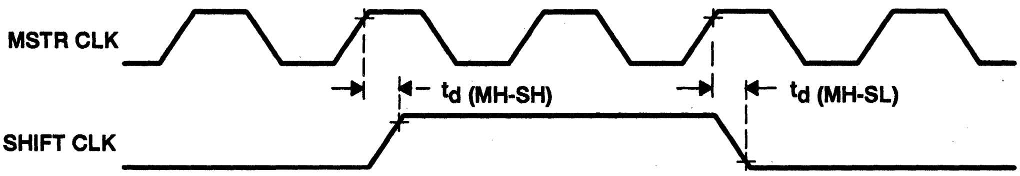


Figure 4–5. Shift-Clock Timing

4.1 TMS32010/TMS320C15 – TLC32046 Interface Circuit

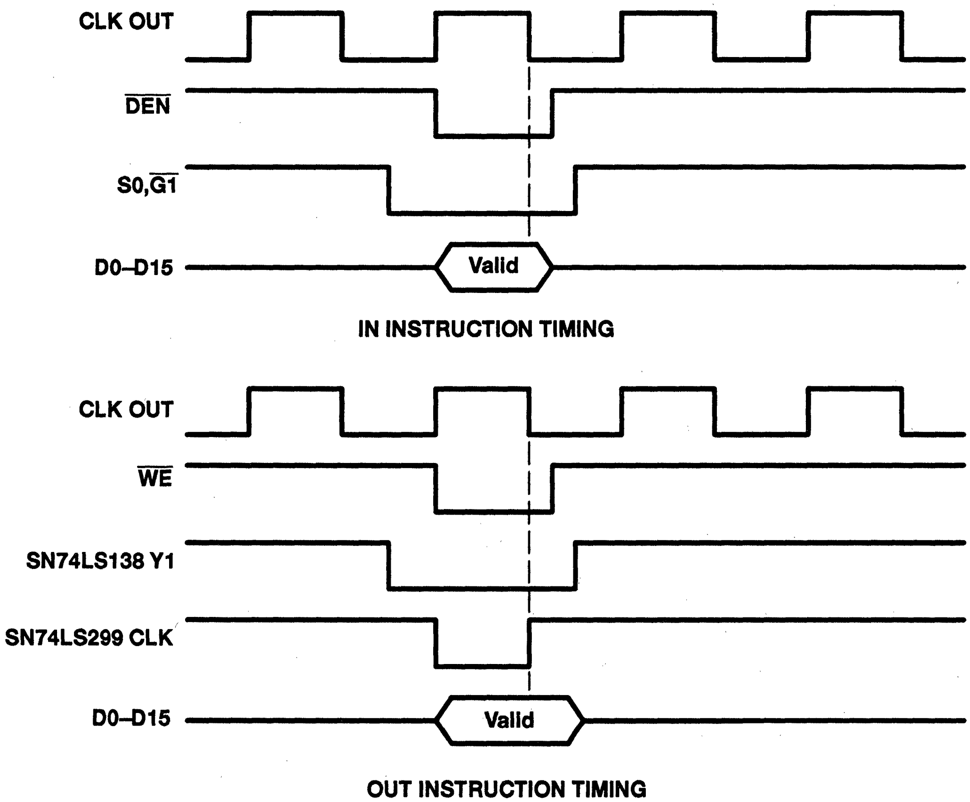


Figure 4–6. TMS32010/TMS320C15–TLC32046 Interface Timing

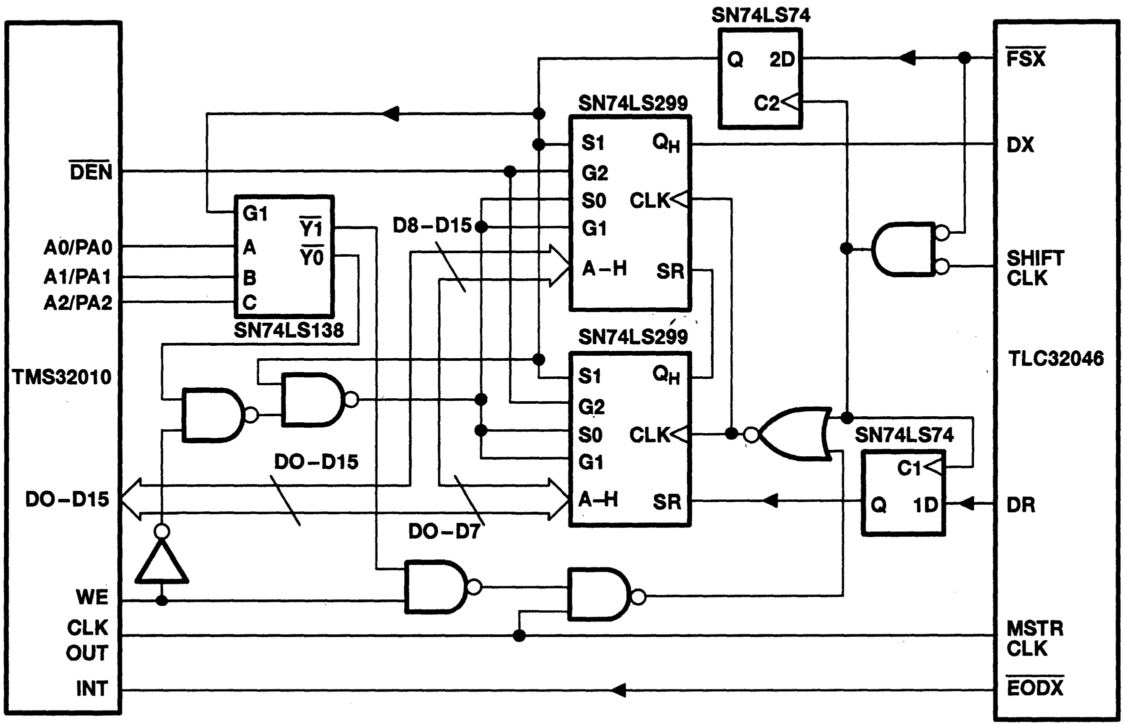


Figure 4–7. TMS32010/TMS320C15 – TLC32046 Interface Circuit

5 Typical Characteristics

D/A AND A/D LOW-PASS FILTER RESPONSE SIMULATION

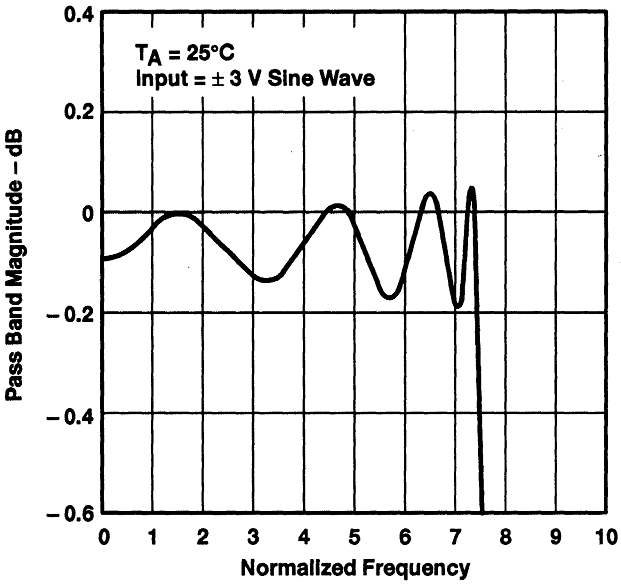


Figure 5–1

D/A AND A/D LOW-PASS FILTER RESPONSE

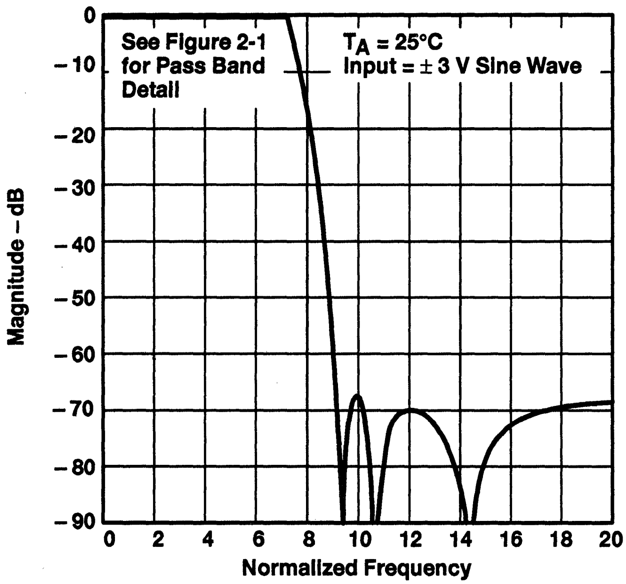


Figure 5–2

NOTE : $\text{Absolute Frequency (kHz)} = \dfrac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{288}$

For Low-Pass SCF f_{clock} > 288 kHz, please call the factory.

D/A AND A/D LOW-PASS GROUP DELAY

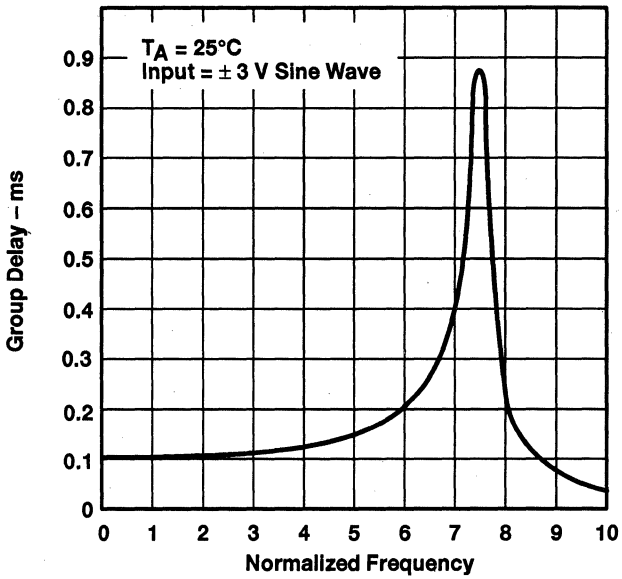


Figure 5–3

A/D BAND-PASS RESPONSE

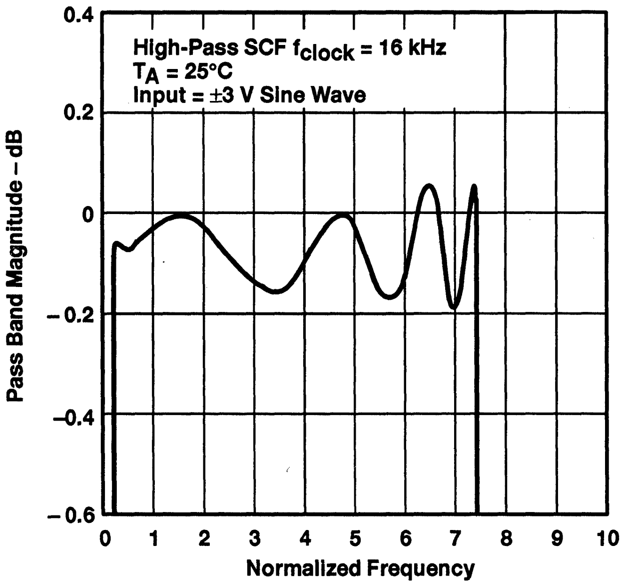


Figure 5–4

$$\text{NOTE : Absolute Frequency (kHz)} = \frac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{288}$$

For Low-Pass SCF f_{clock} > 288 kHz, please call the factory.

A/D BAND-PASS FILTER RESPONSE SIMULATION

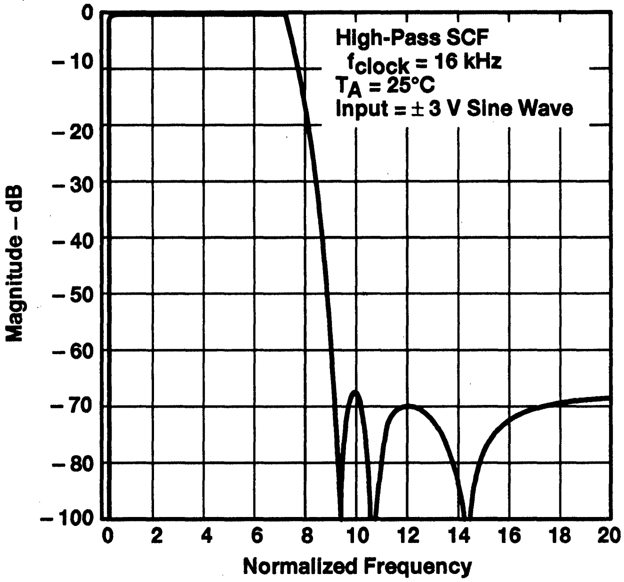


Figure 5–5

A/D BAND-PASS FILTER GROUP DELAY

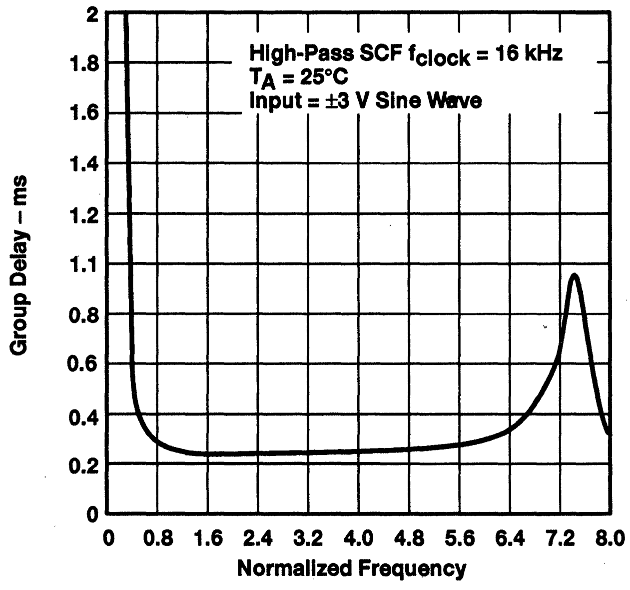


Figure 5–6

NOTE : $\text{Absolute Frequency (kHz)} = \dfrac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{288}$

For Low-Pass SCF f_{clock} > 288 kHz, please call the factory.

A/D CHANNEL HIGH-PASS FILTER

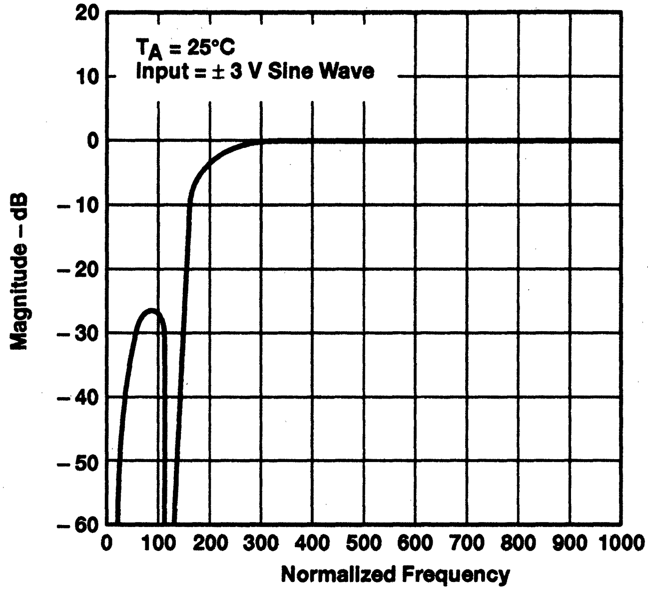


Figure 5–7

D/A (sin x)/x CORRECTION FILTER RESPONSE

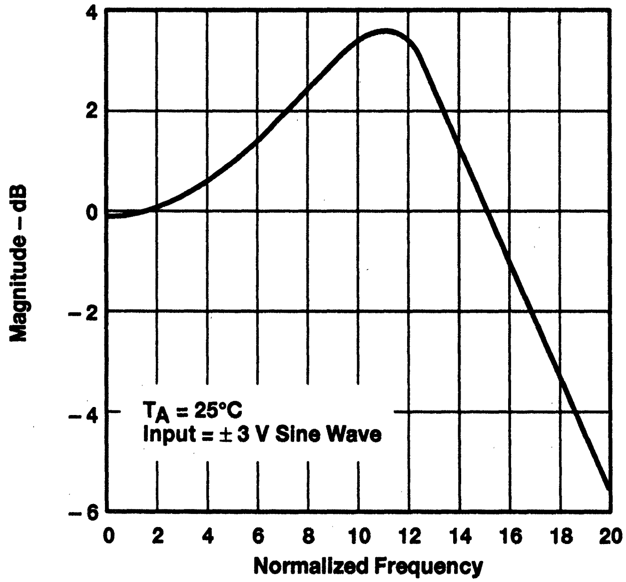


Figure 5–8

NOTE : $\text{Absolute Frequency (kHz)} = \dfrac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{288}$

For Low-Pass SCF f_{clock} > 288 kHz, please call the factory.

D/A (sin x)/x CORRECTION FILTER RESPONSE

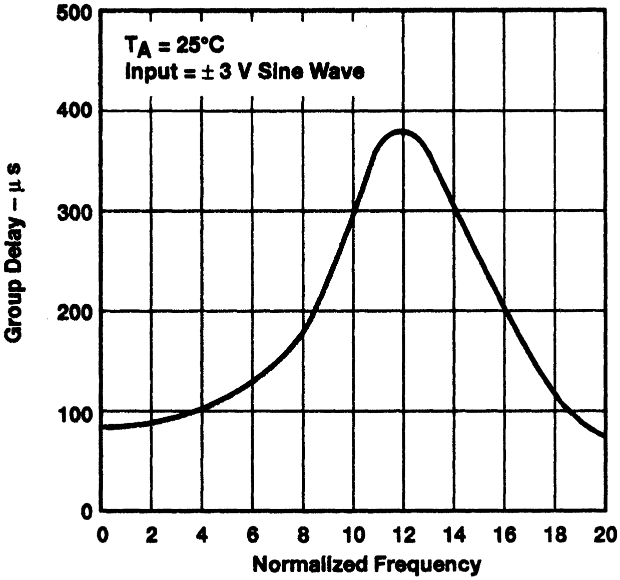


Figure 5–9

D/A (sin x)/x CORRECTION ERROR

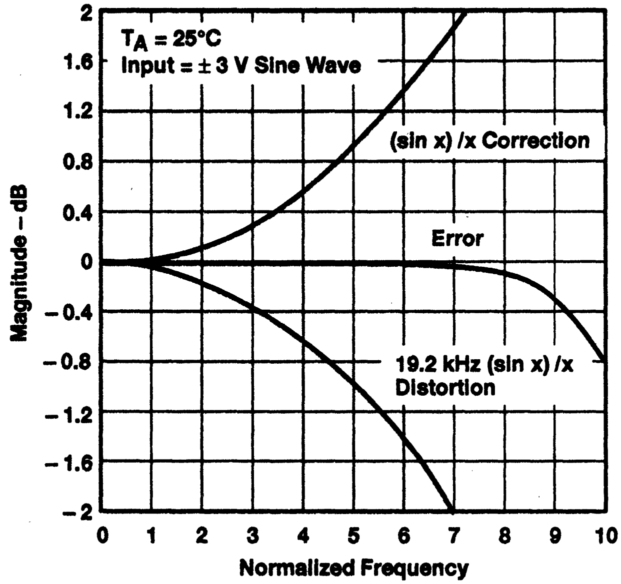


Figure 5–10

NOTE : $\text{Absolute Frequency (kHz)} = \dfrac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{288}$

For Low-Pass SCF f_{clock} > 288 kHz, please call the factory.

A/D BAND-PASS GROUP DELAY

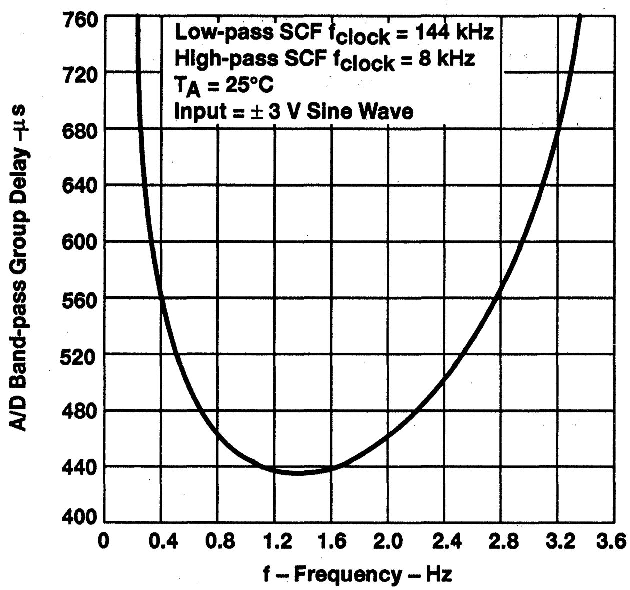


Figure 5–11

D/A LOW-PASS GROUP DELAY

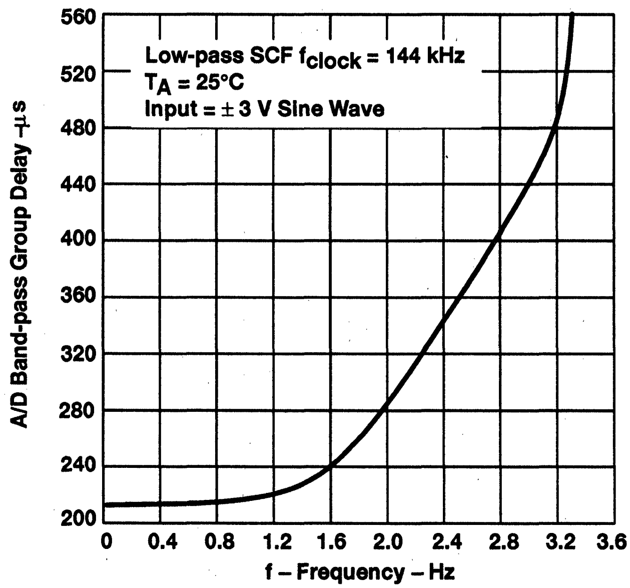


Figure 5–12

A/D SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL

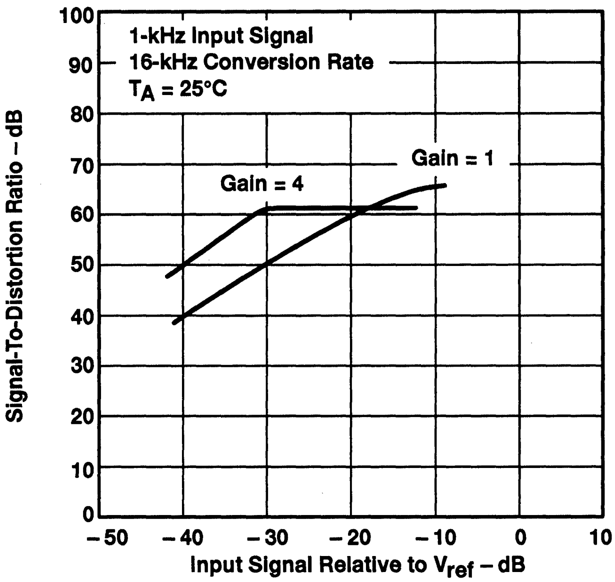


Figure 5–13

A/D GAIN TRACKING
(GAIN RELATIVE TO GAIN AT 0-dB INPUT SIGNAL)

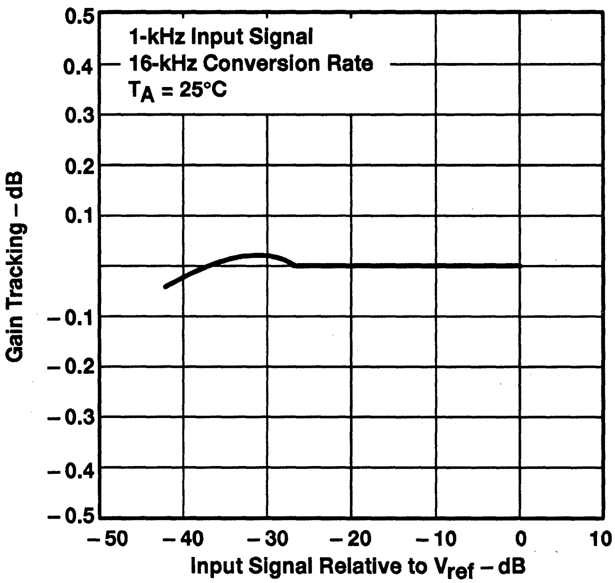


Figure 5–14

D/A CONVERTER SIGNAL-TO-DISTORTION RATIO vs INPUT SIGNAL

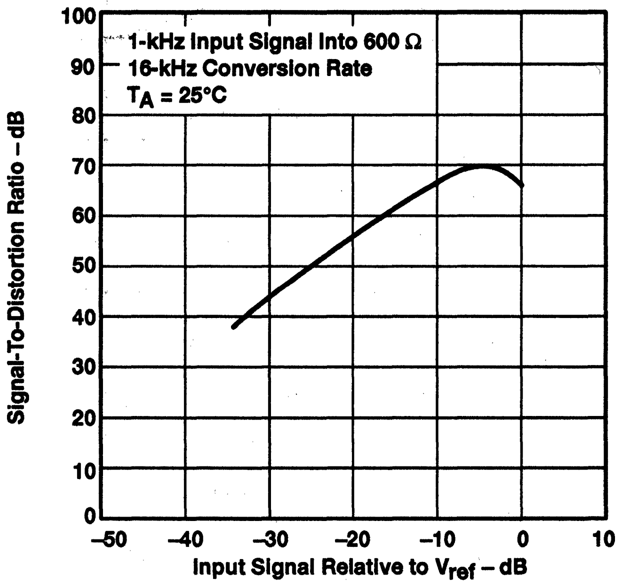


Figure 5–15

D/A GAIN TRACKING (GAIN RELATIVE TO GAIN AT 0-dB INPUT SIGNAL)

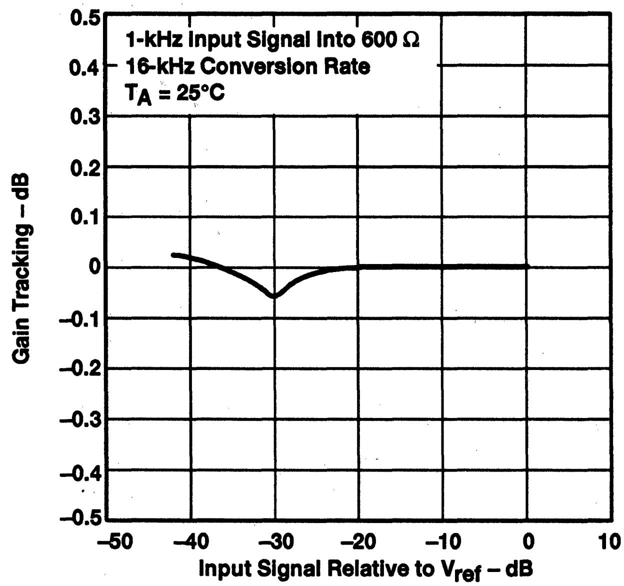


Figure 5–16

A/D SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

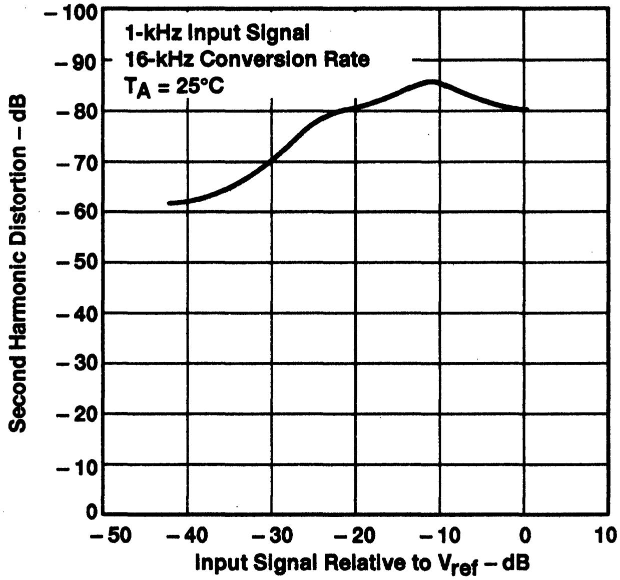


Figure 5–17

D/A SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

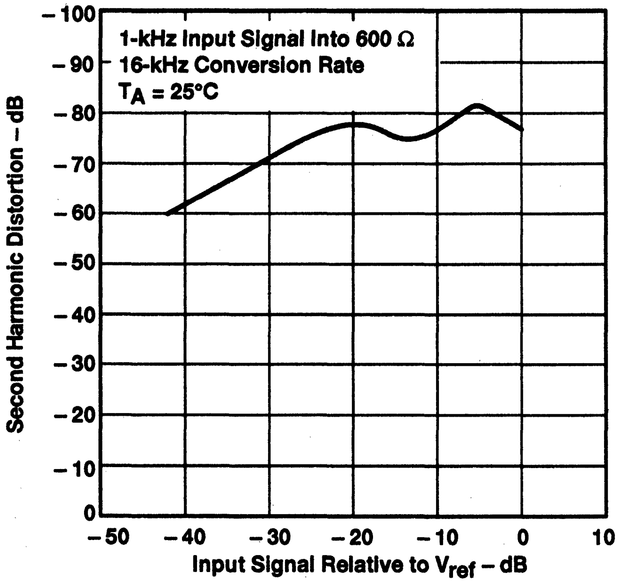


Figure 5–18

A/D THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL

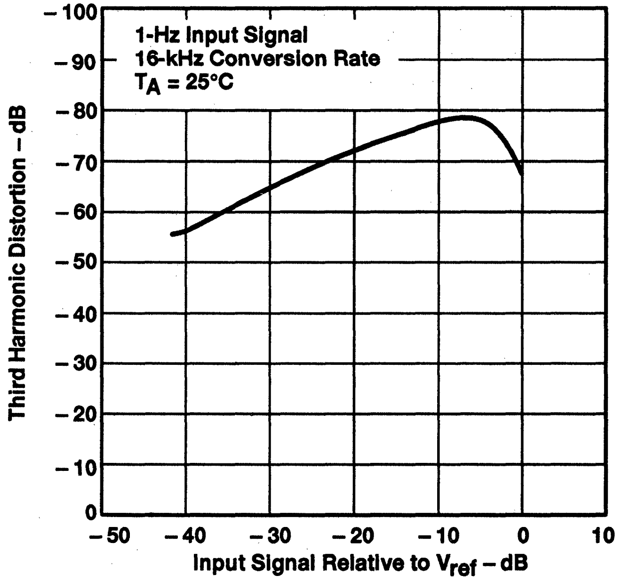


Figure 5–19

D/A THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL

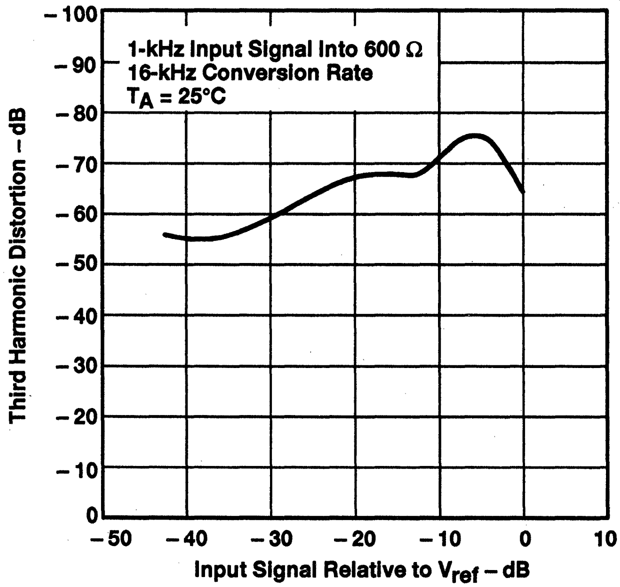


Figure 5–20

6 Application Information

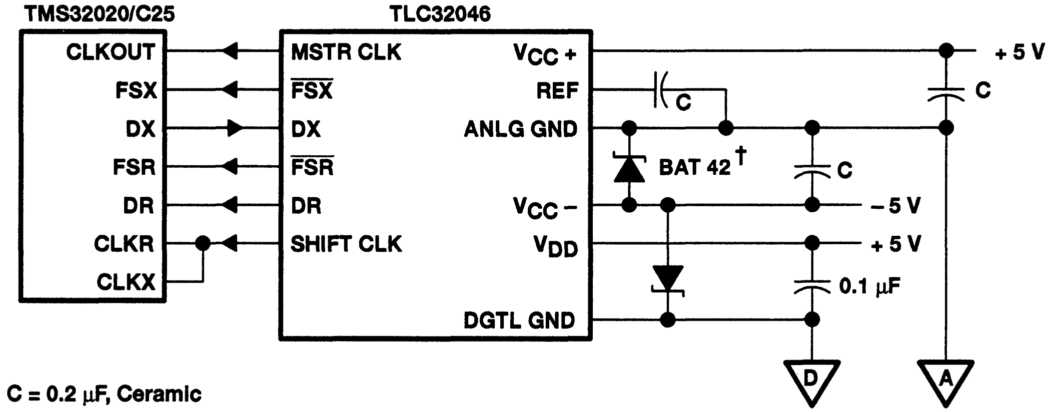


Figure 6–1. AIC Interface to the TMS32020/C25 Showing Decoupling Capacitors and Schottky Diode†

† Thomson Semiconductors

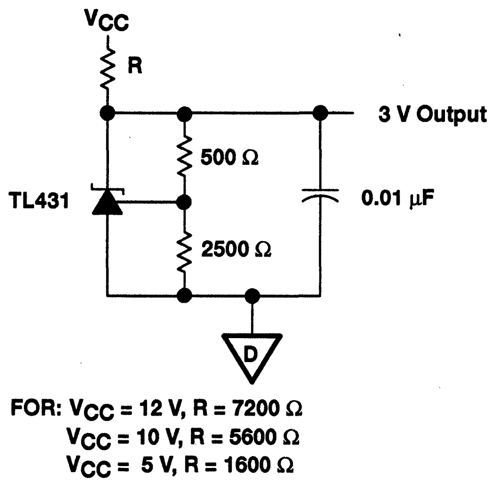


Figure 6–2. External Reference Circuit for TLC32046

TLC32047C, TLC32047I
Data Manual

Wide-Band Analog Interface Circuit

TEXAS INSTRUMENTS

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1 Introduction

The TLC32047 wide-band analog interface circuit (AIC) is a complete analog-to-digital and digital-to-analog interface system for advanced digital signal processors (DSPs) similar to the TMS32020, TMS320C25, and TMS320C30. The TLC32047 offers a powerful combination of options under DSP control: three operating modes [dual-word (telephone interface), word, and byte] combined with two word formats (8 bits and 16 bits) and synchronous or asynchronous operation. It provides a high level of flexibility in that conversion and sampling rates, filter bandwidths, input circuitry, receive and transmit gains, and multiplexed analog inputs are under processor control.

This AIC features a

- band-pass switched-capacitor antialiasing input filter
- 14-bit-resolution A/D converter
- 14-bit-resolution D/A converter
- low-pass switched-capacitor output-reconstruction filter

The antialiasing input filter comprises eighth-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When low-pass filtering is desired, the high-pass filter can be switched out of the signal path. A selectable auxiliary differential analog input is provided for applications where more than one analog input is required.

The output-reconstruction filter is an eighth-order CC-type (Chebyshev/elliptic transitional low-pass filter) followed by a second-order (sin x)/x correction filter and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the sample data signal. The on-board (sin x)/x correction filter can be switched out of the signal path using digital signal processor control.

The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided to ease the design task and to provide complete control over the performance of the IC. The internal voltage reference is brought out to REF. Separate analog and digital voltage supplies and ground are provided to minimize noise and ensure a wide dynamic range. The analog circuit path contains only differential circuitry to keep noise to a minimum. The exception is the DAC sample-and-hold, which utilizes pseudo-differential circuitry.

The TLC32047C is characterized for operation from 0°C to 70°C, and the TLC32047I is characterized for operation from −40°C to 85°C.

1.1 Features

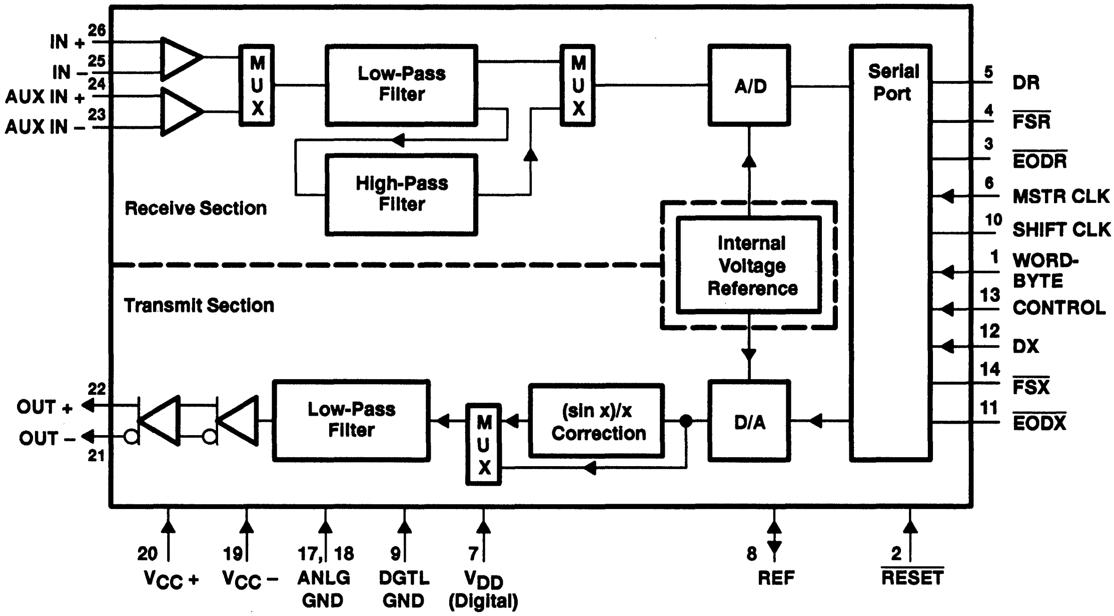
- **14-Bit Dynamic Range ADC and DAC**
- **16-Bit Dynamic Range Input With Programmable Gain**
- **Synchronous or Asynchronous ADC and DAC Sampling Rates Up to 25,000 Samples Per Second**
- **Programmable Incremental ADC and DAC Conversion Timing Adjustments**
- **Typical Applications**
  - **Speech Encryption for Digital Transmission**
  - **Speech Recognition and Storage Systems**
  - **Speech Synthesis**
  - **Modems at 8-kHz, 9.6-kHz, and 16-kHz Sampling Rates**
  - **Industrial Process Control**
  - **Biomedical Instrumentation**
  - **Acoustical Signal Processing**
  - **Spectral Analysis**
  - **Instrumentation Recorders**
  - **Data Acquisition**
- **Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter**
- **Three Fundamental Modes of Operation: Dual-Word (Telephone Interface), Word, and Byte**
- **600-mil Wide N Package**
- **Digital Output in Twos Complement Format**
- **CMOS Technology**

FUNCTION TABLE

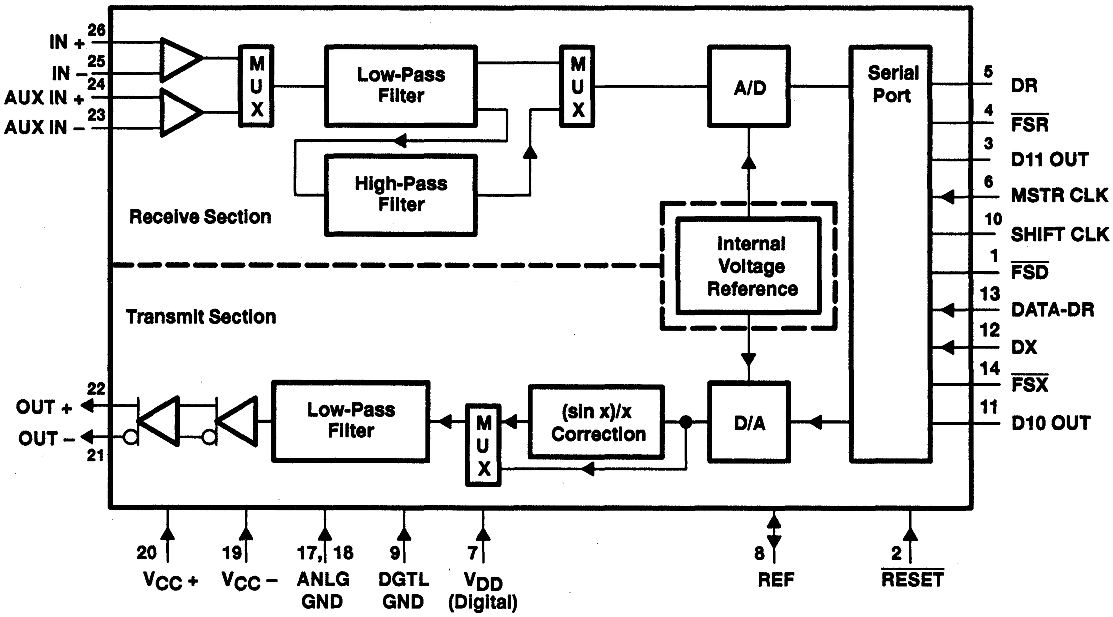
DATA FORMAT	SYNCHRONOUS (CONTROL REGISTER BIT D5 = 1)	ASYNCHRONOUS (CONTROL REGISTER BIT D5 = 0)	FORCING CONDITION	DIRECT INTERFACE
16-bit format	Dual-word (telephone interface) mode	Dual-word (telephone interface) mode	DATA-DR/CONTROL = 0 to 5 V $\overline{\text{FSD}}$/WORD-BYTE = 0 to 5 V	TMS32020, TMS320C25, TMS320C30
16-bit format	Word mode	Word mode	DATA-DR/CONTROL = V_{CC-} (−5 V nom) $\overline{\text{FSD}}$/WORD-BYTE = V_{CC+} (5 V nom)	TMS32020, TMS320C25, TMS320C30, indirect interface to TMS320C10 (see Figure 7)
8-bit format (2 bytes required)	Byte mode	Byte mode	DATA-DR/CONTROL = V_{CC-} (−5 V nom) $\overline{\text{FSD}}$/WORD-BYTE = V_{CC-} (−5 V nom)	TMS320C17

1.2 Functional Block Diagrams

WORD OR BYTE MODE



DUAL-WORD (TELEPHONE INTERFACE) MODE



FRAME SYNCHRONIZATION FUNCTIONS

TLC32047 Function	Frame Sync Output
Receiving serial data on DX from processor to internal DAC	$\overline{FSX}$ low
Transmitting serial data on DR from internal ADC to processor, primary communications	$\overline{FSR}$ low
Transmitting serial data on DR from DATA-DR to processor, secondary communications in dual-word (telephone interface) mode only	$\overline{FSD}$ low

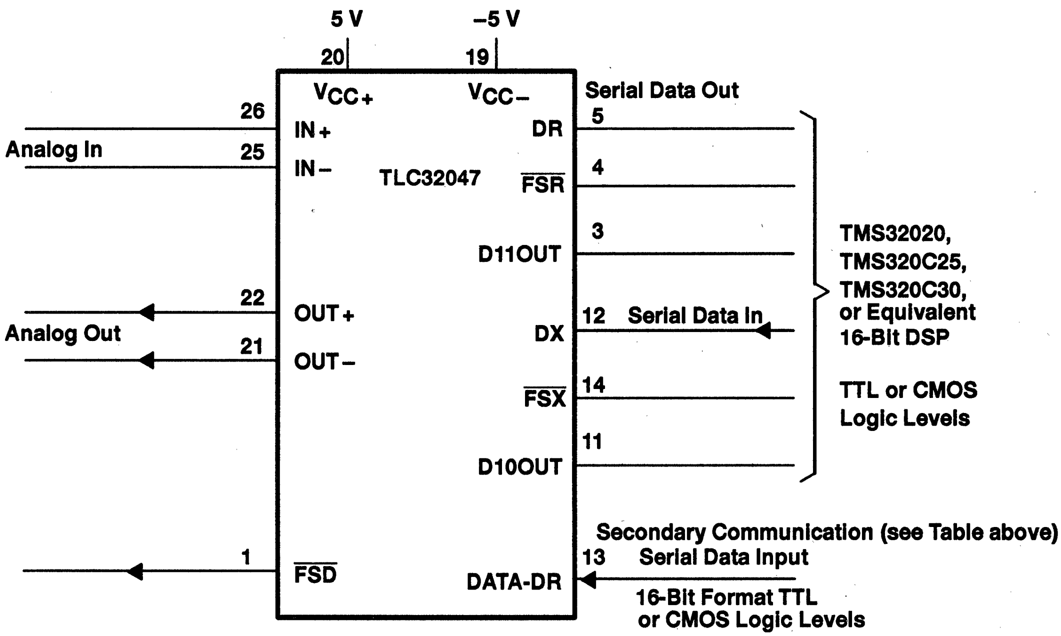


Figure 1–1. Dual-Word (Telephone Interface) Mode

When the DATA-DR/CONTROL input is tied to a logic signal source varying between 0 and 5 V, the TLC32047 is in the dual-word (telephone interface) mode. This logic signal is routed to the DR line for input to the DSP only when terminal 1, data frame synchronization ($\overline{FSD}$), outputs a low level. The $\overline{FSD}$ pulse duration is 16 shift clock pulses. Also, in this mode, the control register data bits D10 and D11 appear on D10OUT and D11OUT, respectively, as outputs.

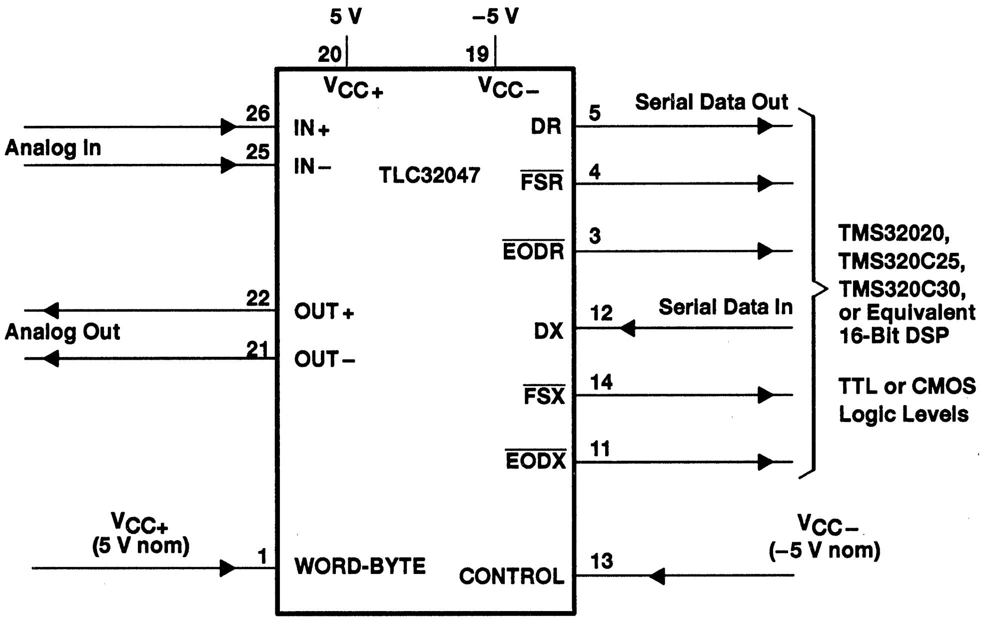


Figure 1–2. Word Mode

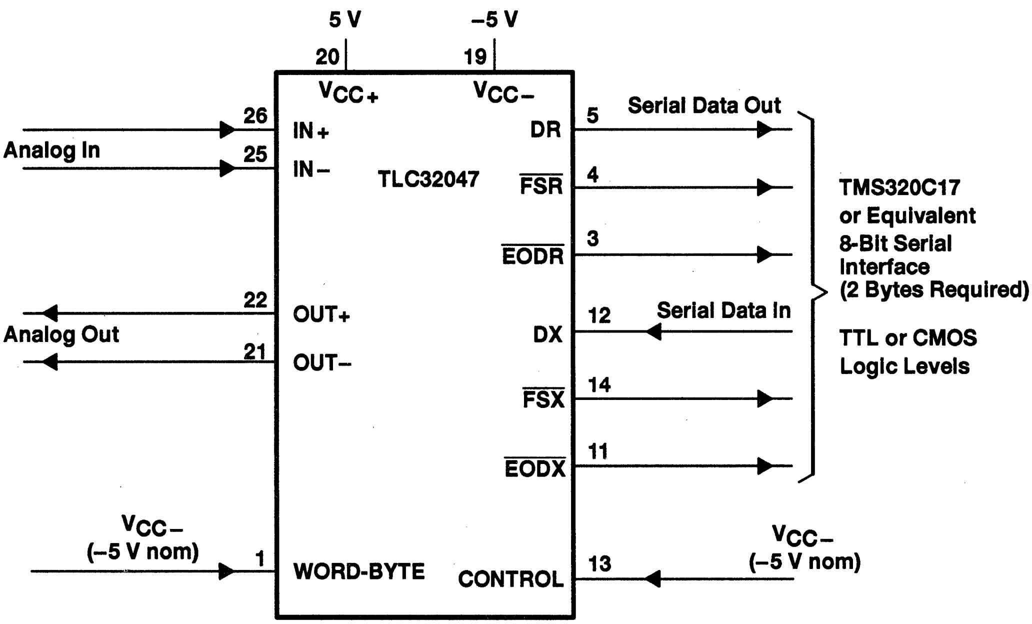
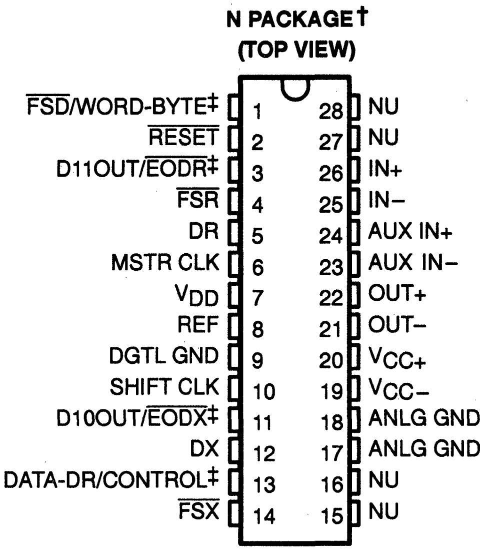
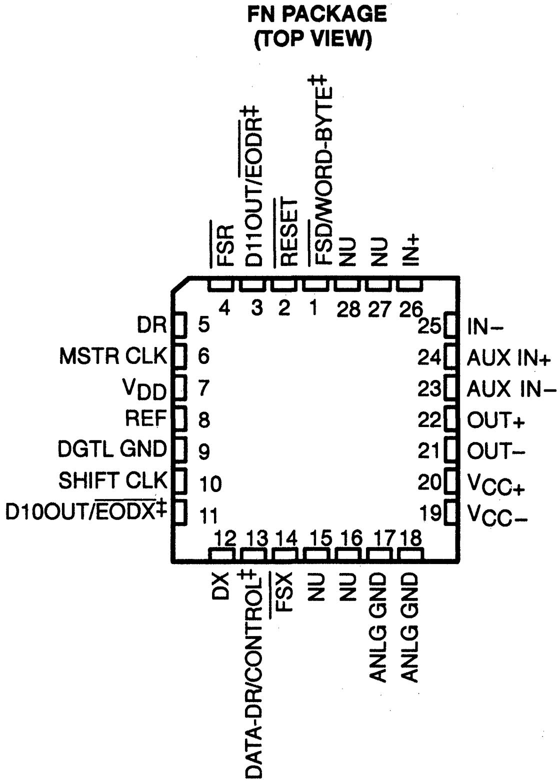


Figure 1–3. Byte Mode

The word or byte mode is selected by first connecting the DATA-DR/CONTROL input to V_{CC-}. FSD/WORD-BYTE becomes an input and can then be used to select either word or byte transmission formats. The end-of-data transmit ($\overline{EODX}$) and the end-of-data receive ($\overline{EODR}$) signals on terminals 11 and 3, respectively, are used to signal the end of word or byte communication (see the Terminal Functions section).

1.3 Terminal Assignments





NU - Nonusable; no external connection should be made to these pins.

† 600-mil wide

‡ The portion of the terminal name to the left of the slash is used for the dual-word (telephone interface) mode. The portion of the terminal name to the right of the slash is used for word-byte mode.

1.4 Ordering Information

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	TLC32047CFN	TLC32047CN
−40°C to 85°C	TLC32047IFN	TLC32047IN

1.5 Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
ANLG GND	17,18		Analog ground return for all internal analog circuits. ANLG GND is internally connected to DGTL GND.
AUX IN+	24	I	Noninverting auxiliary analog input stage. AUX IN+ can be switched into the band-pass filter and ADC path via software control. If the appropriate bit in the control register is a 1, the auxiliary inputs replace the IN+ and IN– inputs. If the bit is a 0, the IN+ and IN– inputs are used (see the DX Serial Data Word Format).
AUX IN–	23	I	Inverting auxiliary analog input (see the above AUX IN+ description).
DATA-DR	13	I	The dual-word (telephone interface) mode, selected by applying an input logic level between 0 and 5 V to DATA-DR, allows DATA-DR to function as a data input. The data is then framed by the $\overline{\text{FSD}}$ signal and transmitted as an output to DR during secondary communication. The functions $\overline{\text{FSD}}$, D11OUT, and D10OUT are valid with this mode selection (see Table 2–1).
CONTROL			When CONTROL is tied to V_{CC-}, the device is in the word or byte mode. The functions WORD-BYTE, $\overline{\text{EODR}}$, and $\overline{\text{EODX}}$ are valid in this mode. $\overline{\text{FSD}}$/WORD-BYTE is then used to select either the word or byte mode (see Function Table).
DR	5	O	DR is used to transmit the ADC output bits from the AIC to the TMS320 serial port. This transmission of bits from the AIC to the TMS320 serial port is synchronized with the SHIFT CLK signal.
DX	12	I	DX is used to receive the DAC input bits and timing and control information from the TMS320. This serial transmission from the TMS320 serial port is synchronized with the SHIFT CLK signal.
D10OUT	11	O	In the dual-word (telephone interface) mode, bit D10 of the control register is output to D10OUT. When the device is reset, bit D10 is initialized to 0 (see DX Serial Data Word Format). The output update is immediate upon changing bit D10.
EODX			End of data transmit. During the word-mode timing, a low-going pulse occurs on EODX immediately after the 16 bits of DAC and control or register information have been transmitted from the TMS320 serial port to the AIC. EODX can be used to interrupt a microprocessor upon completion of serial communications. Also, EODX can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM and to facilitate parallel data bus communications between the DSP and the serial-to-parallel shift registers. During the byte-mode timing, EODX goes low after the first byte has been transmitted from the TMS320 serial port to the AIC and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate first and second bytes.

1.5 Terminal Functions (continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
D11OUT	3	O	In the dual-word (telephone interface) mode, bit D11 of the control register is output to D11OUT. When the device is reset, bit D11 is initialized to 0 (see DX Serial Data Word Format). The output update is immediate upon changing bit D11.
EODR			End of data receive. During the word-mode timing, a low-going pulse occurs on EODR immediately after the 16 bits of A/D information have been transmitted from the AIC to the TMS320 serial port. EODR can be used to interrupt a microprocessor upon completion of serial communications. Also, EODR can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM, and to facilitate parallel data bus communications between the DSP and the serial-to-parallel shift registers. During the byte-mode timing, EODR goes low after the first byte has been transmitted from the AIC to the TMS320 serial port and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate between first and second bytes.
DGTL GND	9		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
$\overline{\text{FSD}}$	1	O	Frame sync data. The $\overline{\text{FSD}}$ output remains high during primary communication. In the dual-word (telephone interface) mode, the $\overline{\text{FSD}}$ output is identical to the $\overline{\text{FSX}}$ output during secondary communication.
WORD-BYTE		I	WORD-BYTE allows differentiation between the word and byte data format (see DATA-DR/CONTROL and Table 2-1 for details).
$\overline{\text{FSR}}$	4	O	Frame sync receive. $\overline{\text{FSR}}$ is held low during bit transmission. When $\overline{\text{FSR}}$ goes low, the TMS320 serial port begins receiving bits from the AIC via DR of the AIC. The most significant DR bit is present on DR before $\overline{\text{FSR}}$ goes low (see Serial Port Sections and Internal Timing Configuration Diagrams).
$\overline{\text{FSX}}$	14	O	Frame sync transmit. When $\overline{\text{FSX}}$ goes low, the TMS320 serial port begins transmitting bits to the AIC via DX of the AIC. $\overline{\text{FSX}}$ is held low during bit transmission (see Serial Port Sections and Internal Timing Configuration Diagrams).
IN+	26	I	Noninverting input to analog input amplifier stage
IN−	25	I	Inverting input to analog input amplifier stage
MSTR CLK	6	I	Master clock. MSTR CLK is used to derive all the key logic signals of the AIC, such as the shift clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The internal timing configuration diagram shows how these key signals are derived. The frequencies of these signals are synchronous submultiples of the master clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the ADC and DAC converters (see the Internal Timing Configuration).
OUT+	22	O	Noninverting output of analog output power amplifier. OUT+ drives transformer hybrids or high-impedance loads directly in a differential or a single-ended configuration.
OUT−	21	O	Inverting output of analog output power amplifier. OUT− is functionally identical with and complementary to OUT+.
REF	8	I/O	Internal voltage reference is brought out on REF. An external voltage reference can be applied to REF to override the internal voltage reference.

1.5 Terminal Functions (continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
$\overline{\text{RESET}}$	2	I	Reset. A reset function is provided to initialize TA, TA', TB, RA, RA', RB (see Figure 2-1), and the control registers. This reset function initiates serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After a negative-going pulse on $\overline{\text{RESET}}$, the AIC registers are initialized to provide a 16-kHz data conversion rate for a 10.368-MHz master clock input signal. The conversion rate adjust registers, TA' and RA', are reset to 1. The CONTROL register bits are reset as follows (see AIC DX Data Word Format section): D11 = 0, D10 = 0, D9 = 1, D7 = 1, D6 = 1, D5 = 1, D4 = 0, D3 = 0, D2 = 1 The shift clock (SCLK) is held high during $\overline{\text{RESET}}$. This initialization allows normal serial-port communication to occur between the AIC and the DSP.
SHIFT CLK	10	O	Shift clock. SHIFT CLK is obtained by dividing the master clock signal frequency by four. SHIFT CLK is used to clock the serial data transfers of the AIC.
V_{DD}	7		Digital supply voltage, 5 V ±5%
V_{CC+}	20		Positive analog supply voltage, 5 V ±5%
V_{CC-}	19		Negative analog supply voltage, −5 V ±5%

2 Detailed Description

Table 2–1. Mode-Selection Function Table

DATA-DR/ CONTROL	$\overline{\text{FSD}}$/ WORD-BYTE	CONTROL REGISTER BIT (D5)	OPERATING MODE	SERIAL CONFIGURATION	DESCRIPTION
Data in (0 to 5 V)	$\overline{\text{FSD}}$ out (0 to 5 V)	1	Dual-Word (Telephone Interface)	Synchronous, One 16-Bit Word	Terminal functions DATA-DR†, $\overline{\text{FSD}}$†, D11OUT, and D10OUT are applicable in this configuration. $\overline{\text{FSD}}$ is asserted during secondary communication, but the $\overline{\text{FSR}}$ is not asserted. However, $\overline{\text{FSD}}$ remains high during primary communication.
Data in (0 to 5 V)	$\overline{\text{FSD}}$ out (0 to 5 V)	0	Dual-Word (Telephone Interface)	Asynchronous, One 16-bit Word	Terminal functions DATA-DR†, $\overline{\text{FSD}}$†, D11OUT, and D10OUT are applicable in this configuration. $\overline{\text{FSD}}$ is asserted during secondary communication, but the $\overline{\text{FSR}}$ is not asserted. However, $\overline{\text{FSD}}$ remains high during primary communication. If secondary communications occur while the A/D conversion is being transmitted from DR, $\overline{\text{FSD}}$ cannot go low, and data from DATA-DR cannot go onto DR.
V_{CC-}	V_{CC+}	1	WORD	Synchronous, One 16-Bit Word	Terminal functions CONTROL†, WORD-BYTE†, $\overline{\text{EODR}}$, and $\overline{\text{EODX}}$ are applicable in this configuration.
		0		Asynchronous, One 16-bit Word	Terminal functions CONTROL†, WORD-BYTE†, $\overline{\text{EODR}}$, and $\overline{\text{EODX}}$ are applicable in this configuration.
	V_{CC-}	1	BYTE	Synchronous, Two 8-Bit Bytes	Terminal functions CONTROL†, WORD-BYTE†, $\overline{\text{EODR}}$, and $\overline{\text{EODX}}$ are applicable in this configuration.
		0		Asynchronous, Two 8-Bit Bytes	Terminal functions CONTROL†, WORD-BYTE†, $\overline{\text{EODR}}$, and $\overline{\text{EODX}}$ are applicable in this configuration.

† DATA-DR/CONTROL has an internal pulldown resistor to −5 V, and $\overline{\text{FSD}}$/WORD-BYTE has an internal pullup resistor to 5 V.

2.1 Internal Timing Configuration (see Figure 2–1)

All the internal timing of the AIC is derived from the high-frequency clock signal that drives the master clock input. The shift clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the master clock input signal frequency by four.

The TX(A) counter and the TX(B) counter, which are driven by the master clock signal, determine the D/A conversion timing. Similarly, the RX(A) counter and the RX(B) counter determine the A/D conversion timing. In order for the low-pass switched-capacitor filter in the D/A path (see Functional Block Diagram) to meet its transfer function specifications, the frequency of its clock input must be 432 kHz. If the clock frequency is not 432 kHz, the filter transfer function frequencies are frequency-scaled by the ratios of the clock frequency to 432 kHz:

$$\text{Absolute Frequency (kHz)} = \frac{\text{Normalized Frequency} \times \text{SCF } f_{clock}\ \text{(kHz)}}{432} \qquad (1)$$

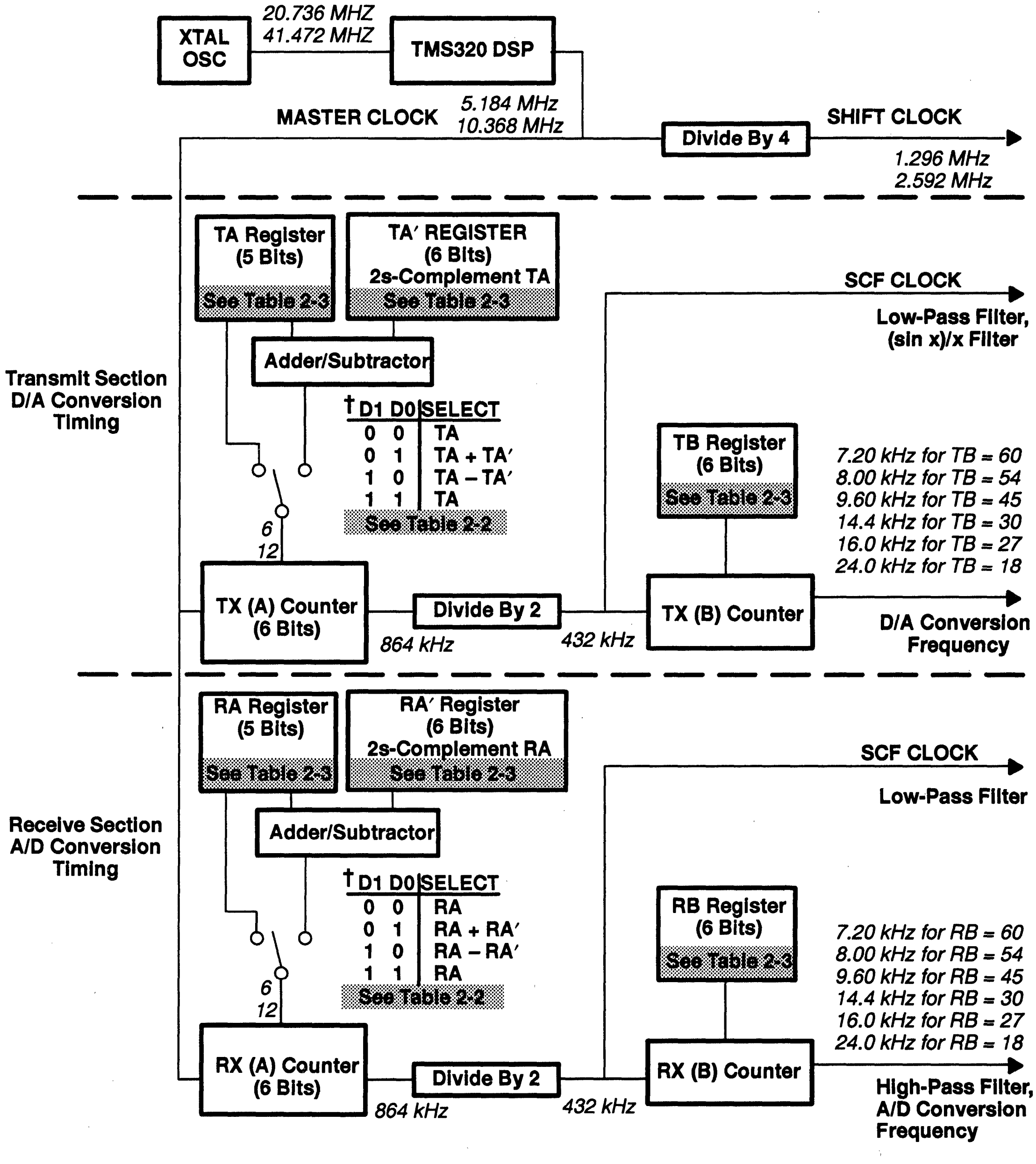
To obtain the specified filter response, the combination of master clock frequency and the TX(A) counter and the RX(A) counter values must yield a 432-kHz switched-capacitor clock signal. This 432-kHz clock signal can then be divided by the TX(B) counter to establish the D/A conversion timing.

The transfer function of the band-pass switched-capacitor filter in the A/D path (see Functional Block Diagram) is a composite of its high-pass and low-pass transfer functions. When the shift clock frequency (SCF) is 432 kHz, the high-frequency roll-off of the low-pass section meets the band-pass filter transfer function specification. Otherwise, the high-frequency roll-off is frequency-scaled by the ratio of the high-pass section's SCF clock to 432 kHz (see Figure 5–5). The low-frequency roll-off of the high-pass section meets the band-pass filter transfer function specification when the A/D conversion rate is 24 kHz. If not, the low-frequency roll-off of the high-pass section is frequency-scaled by the ratio of the A/D conversion rate to 24 kHz.

The TX(A) counter and the TX(B) counter are reloaded each D/A conversion period, while the RX(A) counter and the RX(B) counter are reloaded every A/D conversion period. The TX(B) counter and the RX(B) counter are loaded with the values in the TB and RB registers, respectively. Via software control, the TX(A) counter can be loaded with the TA register, the TA register less the TA′ register, or the TA register plus the TA′ register. By selecting the TA register less the TA′ register option, the upcoming conversion timing occurs earlier by an amount of time that equals TA′ times the signal period of the master clock. If the TA register plus the TA′ register option is executed, the upcoming conversion timing occurs later by an amount of time that equals TA′ times the signal period of the master clock. Thus, the D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. However, the RX(A) counter can be programmed via software control with the RA register, the RA register less the RA′ register, or the RA register plus the RA′ register.

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing and can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.

If the transmit and receive sections are configured to be synchronous, then the low-pass and band-pass switched-capacitor filter clocks are derived from the TX(A) counter. Also, both the D/A and A/D conversion timings are derived from the TX(A) counter and the TX(B) counter. When the transmit and receive sections are configured to be synchronous, the RX(A) counter, RX(B) counter, RA register, RA′ register, and RB registers are not used.



† These control bits are described in the DX Serial Data Word Format section.

NOTES: D. Tables 2–2 and 2–3 (pages 2–9 and 2–10) are primary and secondary communication protocols, respectively.

E. In synchronous operation, RA, RA', RB, RX(A), and RX(B) are not used. TA, TA', TB, TX(A), and TX(B) are used instead.

F. Items in italics refer only to frequencies and register contents, which are variable. A crystal oscillator driving 20.736 MHz into the TMS320-series DSP provides a master clock frequency of 5.184 MHz. The TLC32047 produces a shift clock frequency of 1.296 MHz. If the TX(A) register contents equal 6, the SCF clock frequency is then 432 kHz, and the D/A conversion frequency is 432 kHz ÷ T(B).

Figure 2–1. Asynchronous Internal Timing Configuration

2.2 Analog Input

Two pairs of analog inputs are provided. Normally, the IN+ and IN– input pair is used; however, the auxiliary input pair, AUX IN+ and AUX IN–, can be used if a second input is required. Since sufficient common-mode range and rejection are provided, each input set can be operated in differential or single-ended modes. The gain for the IN+, IN–, AUX IN+, and AUX IN– inputs can be programmed to 1, 2, or 4 (see Table 4–1). Either input circuit can be selected via software control. Multiplexing is controlled with the D4 bit (enable/disable AUX IN+ and AUX IN–) of the secondary DX word (see Table 2–3). The multiplexing requires a 2-ms wait at SCF = 432 kHz (see Figure 5–3) for a valid output signal. A wide dynamic range is ensured by the differential internal analog architecture and the separate analog and digital voltage supplies and grounds.

2.3 A/D Band-Pass Filter, A/D Band-Pass Filter Clocking, and A/D Conversion Timing

The receive-channel A/D high-pass filter can be selected or bypassed via software control (see Functional Block Diagram). The frequency response of this filter is on page 3-5. This response results when the switched-capacitor filter clock frequency is 432 kHz and the A/D sample rate is 24 kHz. Several possible options can be used to attain a 432-kHz switched-capacitor filter clock. When the filter clock frequency is not 432 kHz, the low-pass filter transfer function is frequency-scaled by the ratio of the actual clock frequency to 432 kHz (see Typical Characteristics section). The ripple bandwidth and 3-dB low-frequency roll-off points of the high-pass section are 450 Hz and 300 Hz, respectively. However, the high-pass section low-frequency roll-off is frequency-scaled by the ratio of the A/D sample rate to 24 kHz.

Figure 2–1 and the DX Serial Data Word Format sections of this data manual indicate the many options for attaining a 432-kHz band-pass switched-capacitor filter clock. These sections indicate that the RX(A) counter can be programmed to give a 432-kHz band-pass switched-capacitor filter clock for several master clock input frequencies.

The A/D conversion rate is attained by frequency-dividing the band-pass switched-capacitor filter clock with the RX(B) counter. Unwanted aliasing is prevented because the A/D conversion rate is an integer submultiple of the band-pass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

2.4 A/D Converter

Fundamental performance specifications for the receive channel ADC circuitry are on pages 3-2 and 3-3 of this data manual. The ADC circuitry, using switched-capacitor techniques, provides an inherent sample-and-hold function.

2.5 Analog Output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out of the IC. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

2.6 D/A Low-Pass Filter, D/A Low-Pass Filter Clocking, and D/A Conversion Timing

The frequency response of these filters is on page 3-5. This response results when the low-pass switched-capacitor filter clock frequency is 432 kHz (see Equation 1). Like the A/D filter, the transfer function of this filter is frequency-scaled when the clock frequency is not 432 kHz (see Typical Characteristics section). A continuous-time filter is provided on the output of the low-pass filter to eliminate the periodic sample data signal information, which occurs at multiples of the 432-kHz switched-capacitor clock feedthrough.

The D/A conversion rate is attained by frequency-dividing the 432-kHz switched-capacitor filter clock with the T(B) counter. Unwanted aliasing is prevented because the D/A conversion rate is an integer submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.

2.7 D/A Converter

Fundamental performance specifications for the transmit channel DAC circuitry are on pages 3-3 and 3-4. The DAC has a sample-and-hold function that is realized with a switched-capacitor ladder.

2.8 Serial Port

The serial port has four possible configurations summarized in the function table on page 1-2. These configurations are briefly described below.

- The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS320C17. The communications protocol is two 8-bit bytes.
- The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, and TMS320C30. The communications protocol is one 16-bit word.
- The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS320C17. The communications protocol is two 8-bit bytes.
- The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, TMS320C30, or two SN74299 serial-to-parallel shift registers, which can interface in parallel to the TMS32010, TMS320C15, to any other digital signal processor, or to external FIFO circuitry. The communications protocol is one 16-bit word.

2.9 Synchronous Operation

When the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and band-pass filters (see Functional Block Diagram). The A/D conversion timing is derived from and equal to the D/A conversion timing. When data bit D5 in the control register is a logic 1, transmit and receive sections are synchronous. The band-pass switched-capacitor filter and the A/D converter timing are derived from the TX(A) counter, the TX(B) counter, and the TA and TA' registers. In synchronous operation, both the A/D and the D/A channels operate from the same frequencies. The $\overline{FSX}$ and the $\overline{FSR}$ timing is identical during primary communication, but $\overline{FSR}$ is not asserted during secondary communication because there is no new A/D conversion result.

2.9.1 One 16-Bit Word [Dual-Word (Telephone Interface) or Word Mode]

The serial port interfaces directly with the serial ports of the TMS32020, TMS320C25, and the TMS320C30, and communicates in one 16-bit word. The operation sequence is as follows:

1. $\overline{FSX}$ and $\overline{FSR}$ are brought low by the TLC32047 AIC.
2. One 16-bit word is transmitted and one 16-bit word is received.
3. $\overline{FSX}$ and $\overline{FSR}$ are brought high.
4. $\overline{EODX}$ and $\overline{EODR}$ emit low-going pulses one shift clock wide. $\overline{EODX}$ and $\overline{EODR}$ are valid in the word or byte mode only.

If the device is in the dual-word (telephone interface) mode, $\overline{FSD}$ goes low during the secondary communication period and enables the data word received at the DATA-DR/CONTROL input to be routed to the DR line. The secondary communication period occurs four shift clocks after completion of primary communications.

2.9.2 Two 8-Bit Bytes (Byte Mode)

The serial port interfaces directly with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows:

1. $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ are brought low.
2. One 8-bit word is transmitted and one 8-bit word is received.
3. $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ are brought low.
4. $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ emit positive frame-sync pulses that are four shift clock cycles wide.
5. One 8-bit byte is transmitted and one 8-bit byte is received.
6. $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ are brought high.
7. $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ are brought high.

2.9.3 Synchronous Operating Frequencies

The synchronous operating frequencies are determined by the following equations.

Switched capacitor filter (SCF) frequencies (see Figure 2–1):

$$\text{Low-pass SCF clock frequency (D/A and A/D channels)} = \frac{\text{master clock frequency}}{\text{T(A)} \times 2}$$

$$\text{High-pass SCF clock frequency (A/D channel)} = \text{A/D conversion frequency}$$

$$\text{Conversion frequency (A/D and D/A channels)} = \frac{\text{Low pass SCF clock frequency}}{\text{T(B)}}$$

$$= \frac{\text{master clock frequency}}{\text{T(A)} \times 2 \times \text{T(B)}}$$

NOTE: T(A), T(B), R(A), and R(B) are the contents of the TA, TB, RA, and RB registers, respectively.

2.10 Asynchronous Operation

When the transmit and the receive sections are operated asynchronously, the low-pass and band-pass filter clocks are independently generated from the master clock. The D/A and the A/D conversion timing is also determined independently.

D/A timing is set by the counters and registers described in synchronous operation, but the RA and RB registers are substituted for the TA and TB registers to determine the A/D channel sample rate and the A/D path switched-capacitor filter frequencies. Asynchronous operation is selected by control register bit D5 being zero.

2.10.1 One 16-Bit Word (Word Mode)

The serial port interfaces directly with the serial ports of the TMS32020, TMS320C25, and TMS320C30 and communicates with 16-bit word formats. The operation sequence is as follows:

1. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ are brought low by the TLC32047 AIC.
2. One 16-bit word is transmitted or one 16-bit word is received.
3. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ are brought high.
4. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ emit low-going pulses one shift clock wide. $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ are valid in either the word or byte mode only.

2.10.2 Two 8-Bit Bytes (Byte Mode)

The serial port interfaces directly with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operating sequence is as follows:

1. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ are brought low by the TLC32047 AIC.
2. One byte is transmitted or received.

3. $\overline{EODX}$ or $\overline{EODR}$ are brought low.
4. $\overline{FSX}$ or $\overline{FSR}$ are brought high for four shift clock periods and then brought low.
5. The second byte is transmitted or received.
6. $\overline{FSX}$ or $\overline{FSR}$ are brought high.
7. $\overline{EODX}$ or $\overline{EODR}$ are brought high.

2.10.3 Asynchronous Operating Frequencies

The asynchronous operating frequencies are determined by the following equations.

Switched-capacitor filter frequencies (see Figure 2–1):

$$\text{Low pass D/A SCF clock frequency} = \frac{\text{master clock frequency}}{T(A) \times 2}$$

$$\text{Low pass A/D SCF clock frequency} = \frac{\text{master clock frequency}}{R(A) \times 2}$$

$$\text{High pass SCF clock frequency (A/D channel)} = \text{A/D conversion frequency} \qquad (2)$$

Conversion frequency:

$$\text{D/A conversion frequency} = \frac{\text{Low pass D/A SCF clock frequency}}{T(B)}$$

$$\text{A/D conversion frequency} = \frac{\text{Low pass A/D SCF clock frequency (for low pass receive filter)}}{R(B)} \qquad (3)$$

NOTE: T(A), T(B), R(A), and R(B) are the contents of the TA, TB, RA, and RB registers, respectively.

2.11 Operation of TLC32047 With Internal Voltage Reference

The internal reference of the TLC32047 eliminates the need for an external voltage reference and provides overall circuit cost reduction. The internal reference eases the design task and provides complete control of the IC performance. The internal reference is brought out to REF. To keep the amount of noise on the reference signal to a minimum, an external capacitor can be connected between REF and ANLG GND.

2.12 Operation of TLC32047 With External Voltage Reference

REF can be driven from an external reference circuit. This external circuit must be capable of supplying 250 μA and must be protected adequately from noise and crosstalk from the analog input.

2.13 Reset

A reset function is provided to initiate serial communications between the AIC and DSP and to allow fast, cost-effective testing during manufacturing. The reset function initializes all AIC registers, including the control register. After a negative-going pulse on $\overline{RESET}$, the AIC is initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX Data Word Format section). After a reset, TA=TB=RA=RB=18 (or 12 hexadecimal), TA′=RA′=01 (hexadecimal), the A/D high-pass filter is inserted, the loop-back function is deleted, AUX IN+ and AUX IN− are disabled, the transmit and receive sections are in synchronous operation, programmable gain is set to 1, the on-board (sin x)/x correction filter is not selected, D10 OUT is set to 0, and D11 OUT is set to 0.

2.14 Loopback

This feature allows the circuit to be tested remotely. In loopback, OUT+ and OUT− are internally connected to IN+ and IN−. The DAC bits (D15 to D2), which are transmitted to DX, can be compared with the ADC bits (D15 to D2) received from DR. The bits on DR equal the bits on DX. However, there is some difference in these bits due to the ADC and DAC output offsets.

The loopback feature is implemented with digital signal processor control by transmitting a logic 1 for data bit D3 in the DX secondary communication to the control register (see Table 2–3).

2.15 Communications Word Sequence

In the dual-word (telephone interface) mode, there are two data words that are presented to the DSP or µP from DR. The first data word is the ADC conversion result occurring during the FSR time, and the second is the serial data applied to DATA-DR during the FSD time. FSR is not asserted during secondary communications and FSD is not asserted during primary communications.

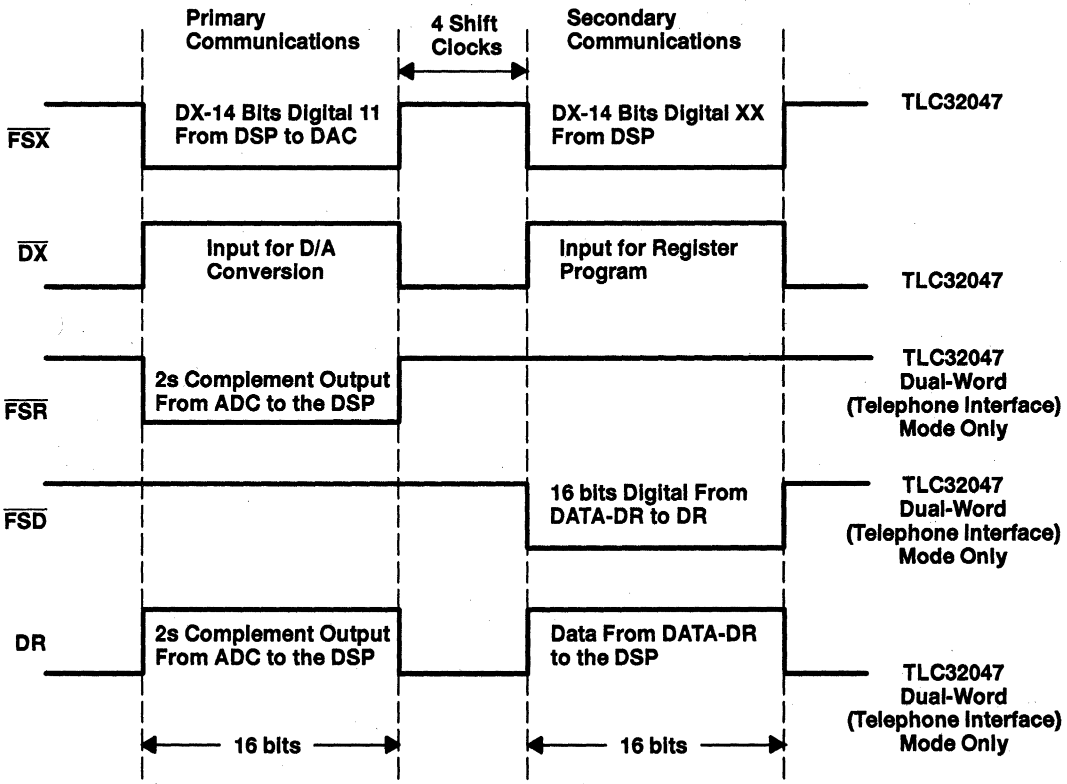


Figure 2–2. Primary and Secondary Communications Word Sequence

2.15.1 DR Word Bit Pattern

A/D MSB
1st bit sent ↓ A/D LSB ↓

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

The data word is the 14-bit conversion result of the receive channel to the processor in 2s complement format. With 16-bit processors, the data is 16 bits long with the two LSBs at zero. Using 8-bit processors, the data word is transmitted in the same order as one 16-bit word, but as two bytes with the two LSBs of the second byte set to zero.

2.15.2 Primary DX Word Bit Pattern

A/D OR D/A MSB 1st bit sent ↓								1st bit sent of 2nd byte ↓					A/D or D/A LSB ↓		
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 2–2. Primary DX Serial Communication Protocol

FUNCTIONS	D1	D0
D15 (MSB)-D2 → DAC Register. TA → TX(A), RA → RX(A) (see Figure 2–1). TB → TX(B), RB → RX(B) (see Figure 2–1).	0	0
D15 (MSB)-D2 → DAC Register. TA+TA′ → TX(A), RA+RA′ → RX(A) (see Figure 2–1). TB → TX(B), RB → RX(B) (see Figure 2–1). The next D/A and A/D conversion period is changed by the addition of TA′ and RA′ master clock cycles, in which TA′ and RA′ can be positive, negative, or zero (refer to Table 2–4, AIC Responses to Improper Conditions).	0	1
D15 (MSB)-D2 → DAC Register. TA–TA′ → TX(A), RA–RA′ → RX(A) (see Figure 2–1). TB → TX(B), RB → RX(B) (see Figure 2–1). The next D/A and A/D conversion period is changed by the subtraction of TA′ and RA′ master clock cycles, in which TA′ and RA′ can be positive, negative, or zero (refer to Table 2–4, AIC Responses to Improper Conditions).	1	0
D15 (MSB)-D2 → DAC Register. TA → TX(A), RA → RX(A) (see Figure 2–1). TB → TX(B), RB → RX(B) (see Figure 2–1). After a delay of four shift cycles, a secondary transmission follows to program the AIC to operate in the desired configuration. In the telephone interface mode, data on DATA-DR is routed to DR (Serial Data Output) during secondary transmission.	1	1

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (primary communications) to the AIC initiates secondary communications upon completion of the primary communications. When the primary communication is complete, $\overline{\text{FSX}}$ remains high for four shift clock cycles and then goes low and initiates the secondary communication. The timing specifications for the primary and secondary communications are identical. In this manner, the secondary communication, if initiated, is interleaved between successive primary communications. This interleaving prevents the secondary communication from interfering with the primary communications and DAC timing. This prevents the AIC from skipping a DAC output. $\overline{\text{FSR}}$ is not asserted during secondary communications activity. However, in the dual-word (telephone interface) mode, $\overline{\text{FSD}}$ is asserted during secondary communications but not during primary communications.

2.15.3 Secondary DX Word Bit Pattern

D/A MSB 1st bit sent ↓								1st bit sent of 2nd byte ↓					D/A LSB ↓		
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 2–3. Secondary DX Serial Communication Protocol

FUNCTIONS	D1	D0
D13 (MSB)-D9 → TA , 5 bits unsigned binary (see Figure 2–1). D6 (MSB)-D2 → RA, 5 bits unsigned binary (see Figure 2–1). D15, D14, D8, and D7 are unassigned.	0	0
D14 (sign bit)-D9 → TA′, 6 bits 2s complement (see Figure 2–1). D7 (sign bit)-D2 → RA′, 6 bits 2s complement (see Figure 2–1). D15 and D8 are unassigned.	0	1
D14 (MSB)-D9 → TB, 6 bits unsigned binary (see Figure 2–1). D7 (MSB)-D2 → RB, 6 bits unsigned binary (see Figure 2–1). D15 and D8 are unassigned.	1	0
D2 = 0/1 deletes/inserts the A/D high-pass filter. D3 = 0/1 deletes/inserts the loopback function. D4 = 0/1 disables/enables AUX IN+ and AUX IN–. D5 = 0/1 asynchronous/synchronous transmit and receive sections. D6 = 0/1 gain control bits (see Table 4–1). D7 = 0/1 gain control bits (see Table 4–1). D9 = 0/1 delete/insert on-board second-order (sin x)/x correction filter D10 = 0/1 output to D10OUT [dual-word (telephone interface) mode] D11 = 0/1 output to D11OUT [dual-word (telephone interface) mode] D8, D12–D15 are unassigned.	1	1

2.16 Reset Function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After power has been applied to the AIC, a negative-going pulse on $\overline{\text{RESET}}$ initializes the AIC registers to provide a 16-kHz A/D and D/A conversion rate for a 10.368-MHz master clock input signal. Also, the pass-bands of the A/D and D/A filters are 300 Hz to 7200 Hz and 0 Hz to 7200 Hz, respectively. Therefore, the filter bandwidths are 66% of those shown in the filter transfer function specification section. The AIC, excepting the control register, is initialized as follows (see AIC DX Data Word Format section):

REGISTER	TA	TA′	TB	RA	RA′	RB
INITIALIZED VALUE (HEX)	12	01	12	12	01	12

The control register bits are reset as follows (see Table 2–3):

D11 = 0, D10 = 0, D9 = 1, D7 = 1, D6 = 1, D5 = 1, D4 = 0, D3 = 0, D2 = 1

This initialization allows normal serial port communications to occur between the AIC and the DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA′, and TB register need to be programmed. Both transmit and receive timing are synchronously derived from these registers (see the Terminal Functions and DX Serial Data Word Format sections).

Figure 2–3 shows a circuit that provides a reset on power-up when power is applied in the sequence given in the Power-Up Sequence section. The circuit depends on the power supplies reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.

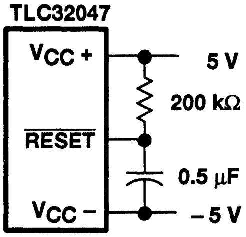


Figure 2–3. Reset on Power-Up Circuit

2.17 Power-Up Sequence

To ensure proper operation of the AIC and as a safeguard against latch-up, it is recommended that Schottky diodes with forward voltages less than or equal to 0.4 V be connected from V_{CC-} to ANLG GND and from V_{CC-} to DGTL GND. In the absence of such diodes, power is applied in the following sequence: ANLG GND and DGTL GND, V_{CC-}, then V_{CC+} and V_{DD}. Also, no input signal is applied until after power-up.

2.18 AIC Register Constraints

The following constraints are placed on the contents of the AIC registers:

1. TA register must be ≥ 4 in word mode (WORD/BYTE= High).
2. TA register must be ≥ 5 in byte mode (WORD/BYTE= Low).
3. TA′ register can be either positive, negative, or zero.
4. RA register must be ≥ 4 in word mode (WORD/BYTE = High).
5. RA register must be ≥ 5 in byte mode (WORD/BYTE = Low).
6. RA′ register can be either positive, negative, or zero.
7. (TA register ± TA′ register) must be > 1.
8. (RA register ± RA′ register) must be > 1.
9. TB register must be ≥ 15.
10. RB register must be ≥ 15.

2.19 AIC Responses to Improper Conditions

The AIC has provisions for responding to improper conditions. These improper conditions and the response of the AIC to these conditions are presented in Table 2–4. The general procedure for correcting any improper operation is to apply a reset and reprogram the registers to the proper value.

Table 2–4. AIC Responses to Improper Conditions

IMPROPER CONDITION	AIC RESPONSE
TA register + TA′ register = 0 or 1 TA register – TA′ register = 0 or 1	Reprogram TX(A) counter with TA register value
TA register + TA′ register < 0	MODULO 64 arithmetic is used to ensure that a positive value is loaded into TX(A) counter, i.e., TA register + TA′ register + 40 hex is loaded into TX(A) counter.
RA register + RA′ register = 0 or 1 RA register – RA′ register = 0 or 1	Reprogram RX(A) counter with RA register value
RA register + RA′ register = 0 or 1	MODULO 64 arithmetic is used to ensure that a positive value is loaded into RX(A) counter, i.e., RA register + RA′ register + 40 hex is loaded into RX(A) counter.
TA register = 0 or 1 RA register = 0 or 1	AIC is shut down. Reprogram TA or RA registers after a reset.
TA register < 4 in word mode TA register < 5 in byte mode RA register < 4 in word mode RA register < 5 in byte mode	The AIC serial port no longer operates. Reprogram TA or RA registers after a reset.
TB register < 15	ADC no longer operates
RB register < 15	DAC no longer operates
AIC and DSP cannot communicate	Hold last DAC output

2.20 Operation With Conversion Times Too Close Together

If the difference between two successive D/A conversion frame syncs is less than 1/25 kHz, the AIC operates improperly. In this situation, the second D/A conversion frame sync occurs too quickly, and there is not enough time for the ongoing conversion to be completed. This situation can occur if the A and B registers are improperly programmed or if the A + A′ register result is too small. When incrementally adjusting the conversion period via the A + A′ register options, the designer should not violate this requirement. See Figure2–4.

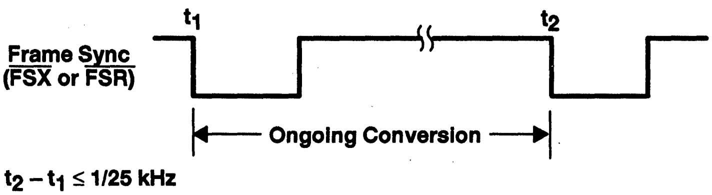


Figure 2–4. Conversion Times Too Close Together

2.21 More Than One Receive Frame Sync Occurring Between Two Transmit Frame Syncs – Asynchronous Operation

When incrementally adjusting the conversion period via the A + A′ or A – A′ register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during an $\overline{FSX}$ frame sync. The ongoing conversion period is then adjusted; however, either receive conversion period A or conversion period B may be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. If there is sufficient time between t_1 and t_2, the receive conversion period adjustment is performed during receive conversion period A. Otherwise, the adjustment is performed during receive conversion period B. The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent $\overline{FSX}$ frame (see Figure 2–5).

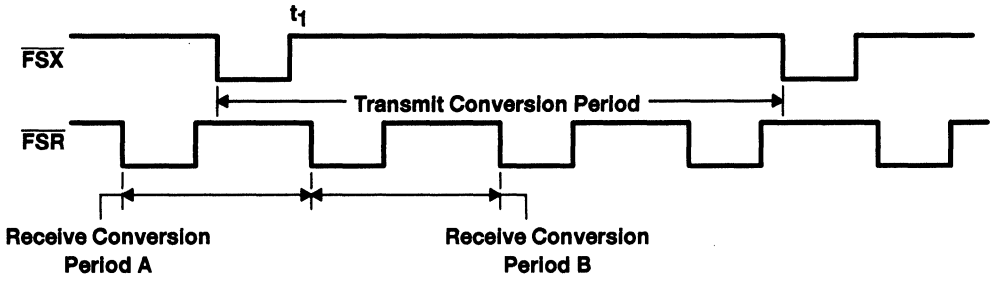


Figure 2–5. More Than One Receive Frame Sync Between Two Transmit Frame Syncs

2.22 More Than One Transmit Frame Sync Occurring Between Two Receive Frame Syncs – Asynchronous Operation

When incrementally adjusting the conversion period via the A + A′ or A – A′ register options, a specific protocol must be followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during an $\overline{FSX}$ frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment as shown in Figure 2–6. When the adjustment command is issued during transmit conversion period A, receive conversion period A is adjusted if there is sufficient time between t_1 and t_2. If there is not sufficient time between t_1 and t_2, receive conversion period B is adjusted. The third option is that the receive portion of an adjustment command can be ignored if the adjustment command is sent during a receive conversion period, which is adjusted due to a prior adjustment command. For example, if adjustment commands are issued during transmit conversion periods A, B, and C, the first two commands may cause receive conversion periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during receive conversion period B, which already is adjusted via the transmit conversion period B adjustment command.

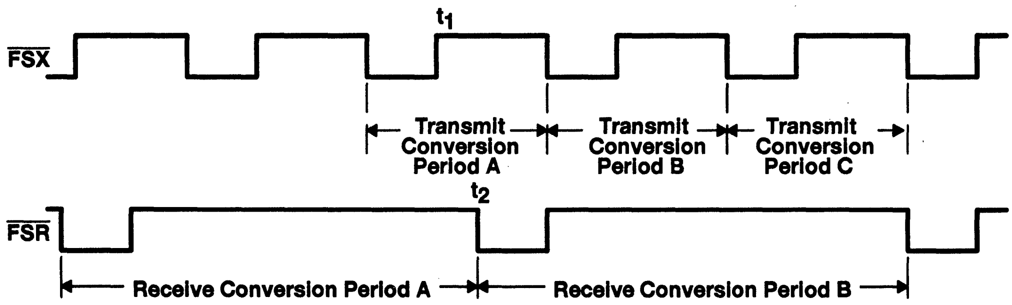


Figure 2–6. More Than One Transmit Frame Sync Between Two Receive Frame Syncs

2.23 More than One Set of Primary and Secondary DX Serial Communications Occurring Between Two Receive Frame Syncs (See DX Serial Data Word Format section) – Asynchronous Operation

The TA, TA′, TB, and control register information that is transmitted in the secondary communication is accepted and applied during the ongoing transmit conversion period. If there is sufficient time between t_1 and t_2, the TA, RA′, and RB register information, sent during transmit conversion period A, is applied to receive conversion period A. Otherwise, this information is applied during receive conversion period B. If RA, RA′, and RB register information has been received and is being applied during an ongoing conversion period, any subsequent RA, RA′, or RB information received during this receive conversion period is disregarded. See Figure 2–7.

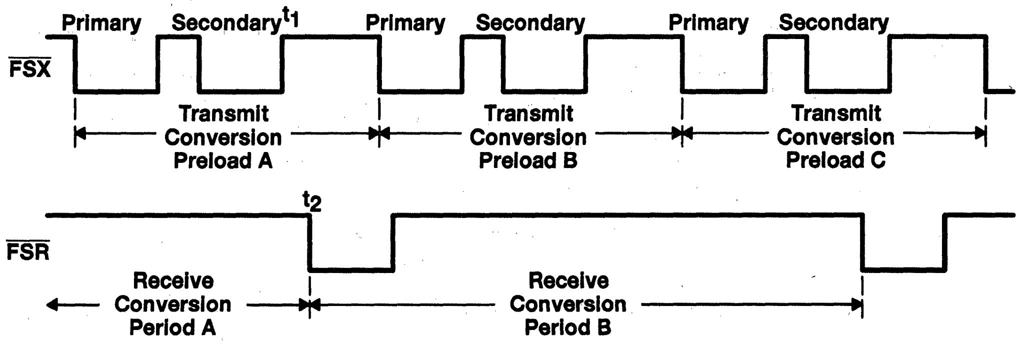


Figure 2–7. More Than One Set of Primary and Secondary DX Serial Communications Between Two Receive Frame Syncs

2.24 System Frequency Response Correction

The (sin x)/x correction for the DAC zero-order sample-and-hold output can be provided by an on-board second-order (sin x)/x correction filter (see Functional Block Diagram). This (sin x)/x correction filter can be inserted into or omitted from the signal path by digital-signal-processor control (data bit D9 in the DX secondary communications). When inserted, the (sin x)/x correction filter precedes the switched-capacitor low-pass filter. When the TB register (see Figure 2–1) equals 15, the correction results of Figures 5–8, 5–9, and 5–10 can be obtained.

The (sin x)/x correction can also be accomplished by disabling the on-board second-order correction filter and performing the (sin x)/x correction in digital signal processor software. The system frequency response can be corrected via DSP software to ± 0.1 dB accuracy to a band edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, that requires seven TMS320 instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the (sin x)/x Correction Section for more details).

2.25 (sin x)/x Correction

If the designer does not wish to use the on-board second-order (sin x)/x correction filter, correction can be accomplished in digital signal processor (DSP) software. (sin x)/x correction can be accomplished easily and efficiently in digital signal processor software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results shown below are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires seven instruction cycles per sample on the TMS320 DSP. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction adds a slight amount of group delay at the upper edge of the 300-Hz to 3000-Hz band.

2.26 (sin x)/x Roll-Off for a Zero-Order Hold Function

The (sin x)/x roll-off error for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in Table 2–5 (see Figure 5–10).

Table 2–5. (sin x)/x Roll-Off Error

f_s (Hz)	Error = $20 \log \frac{\sin \pi f/f_s}{\pi f/f_s}$ f = 3000 Hz (dB)
7200	−2.64
8000	−2.11
9600	−1.44
14400	−0.63
16000	−0.50
19200	−0.35
25000	−0.21

The actual AIC (sin x)/x roll-off is slightly less than the figures above because the AIC has less than 100% duty cycle hold interval.

2.27 Correction Filter

To externally compensate for the (sin x)/x roll-off of the AIC, a first-order correction filter can be implemented as shown in Figure 2–8.

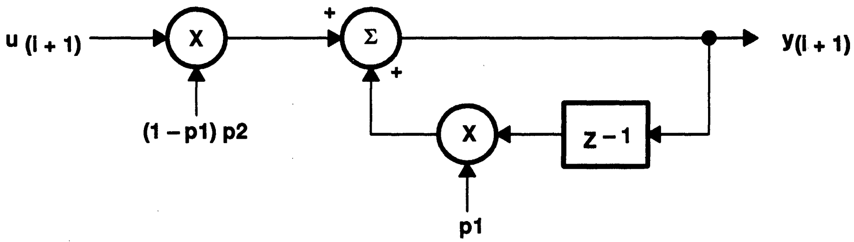


Figure 2–8. First-Order Correction Filter

The difference equation for this correction filter is:

$$y_{(i+1)} = p2 \cdot (1 - p1) \cdot u_{(i+1)} + p1 \cdot y_{(i)} \tag{4}$$

where the constant p1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$| H(f) |^2 = \frac{(p2)^2 \cdot (1-p1)^2}{1 - 2 \cdot p1 \cdot \cos(2\pi f/f_s) + (p1)^2} \tag{5}$$

2.28 Correction Results

Table 2-6 shows the optimum p values and the corresponding correction results for 8000-Hz and 9600-Hz sampling rates (see Figures 5–8, 5–9, and 5–10).

Table 2–6. (sin x)/x Correction Table for f_s = 8000 Hz and f_s = 9600 Hz

f (Hz)	ROLL-OFF ERROR (dB) f_s = 8000 Hz p1 = −0.14813 p2 = 0.9888	ROLL-OFF ERROR (dB) f_s = 9600 Hz p1 = −0.1307 p2 = 0.9951
300	−0.099	−0.043
600	−0.089	−0.043
900	−0.054	0
1200	−0.002	0
1500	0.041	0
1800	0.079	0.043
2100	0.100	0.043
2400	0.091	0.043
2700	−0.043	0
3000	−0.102	−0.043

2.29 TMS320 Software Requirements

The digital correction filter equation can be written in state variable form as follows:

$$y_{(i+1)} = y_{(i)} \times k1 + u_{(i+1)} \times k2$$

where

k1 = p1
k2 = (1 − p1)p2
y(i) is the filter state
u(i+1)

The coefficients k1 and k2 must be represented as 16-bit integers. The SACH instruction (with the proper shift) yields the correct result. With the assumption that the TMS320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, V_{CC+} (see Note 1)	−0.3 V to 15 V
Supply voltage range, V_{CC-} (see Note 1)	−0.3 V to 15 V
Supply voltage range, V_{DD}	−0.3 V to 15 V
Output voltage range, V_O	−0.3 V to 15 V
Input voltage range, V_I	−0.3 V to 15 V
Digital ground voltage range	−0.3 V to 15 V
Operating free-air temperature range: TLC32047C	0°C to 70°C
TLC32047I	−40°C to 85°C
Storage temperature range	−40°C to 125°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values for maximum ratings are with respect to V_{CC-}.

3.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} (see Note 2)		4.75	5	5.25	V
Supply voltage, V_{CC-} (see Note 2)		−4.75	−5	−5.25	V
Digital supply voltage, V_{DD} (see Note 2)		4.75	5	5.25	V
Digital ground voltage with respect to ANLG GND, DGTL GND			0		V
Reference input voltage, $V_{ref(ext)}$ (see Note 2)		2		4	V
High-level input voltage, V_{IH}		2		V_{DD}	V
Low-level input voltage, V_{IL} (see Note 3)		0		0.8	V
Load resistance at OUT+ and/or OUT−, R_L		300			Ω
Load capacitance at OUT+ and/or OUT−, C_L				100	pF
MSTR CLK frequency (see Note 4)			5	10.368	MHz
Analog input amplifier common mode input voltage (see Note 5)				±1.5	V
A/D or D/A conversion rate				25	kHz
Operating free-air temperature range, T_A	TLC32047C	0		70	°C
	TLC32047I	−40		85	°C

NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+}, and V_{CC-} are with respect to ANLG GND. Voltages at digital inputs and outputs and V_{DD} are with respect to DGTL GND.
3. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data manual for logic voltage levels only.
4. The band-pass switched-capacitor filter (SCF) specifications apply only when the low-pass section SCF clock is 432 kHz and the high-pass section SCF clock is 24 kHz. If the low-pass SCF clock is shifted from 432 kHz, the low-pass roll-off frequency shifts by the ratio of the low-pass SCF clock to 432 kHz. If the high-pass SCF clock is shifted from 24 kHz, the high-pass roll-off frequency shifts by the ratio of the high-pass SCF clock to 24 kHz. Similarly, the low-pass switched-capacitor filter (SCF) specifications apply only when the SCF clock is 432 kHz. If the SCF clock is shifted from 432 kHz, the low-pass roll-off frequency shifts by the ratio of the SCF clock to 432 kHz.
5. This range applies when (IN+ − IN−) or (AUX IN+ − AUX IN−) equals ± 6 V.

3.3 Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (Unless Otherwise Noted)

3.3.1 Total Device, MSTR CLK Frequency = 5.184 MHz, Outputs Not Loaded

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 4.75 V, I_{OH} = −300 µA	2.4			V
V_{OL}	Low-level output voltage		V_{DD} = 4.75 V, I_{OL} = 2 mA			0.4	V
I_{CC+}	Supply current from V_{CC+}	TLC32047C				35	mA
		TLC32047I				40	mA
I_{CC-}	Supply current from V_{CC-}	TLC32047C				−35	mA
		TLC32047I				−40	mA
I_{DD}	Supply current from V_{DD}					7	mA
V_{ref}	Internal reference output voltage			3		3.3	V
αV_{ref}	Temperature coefficient of internal reference voltage				250		ppm/°C
r_o	Output resistance at REF				100		kΩ

† All typical values are at T_A = 25°C.

3.3.2 Power Supply Rejection and Crosstalk Attenuation

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC+} or V_{CC-} supply voltage rejection ratio, receive channel	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at DR (ADC output)		30		dB
	f = 30 kHz to 50 kHz			45		
V_{CC+} or V_{CC-} supply voltage rejection ratio, transmit channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at OUT+		30		dB
	f = 30 kHz to 50 kHz			45		
Crosstalk attenuation, transmit-to-receive (single-ended)				80		dB

† All typical values are at T_A = 25°C.

3.3.3 Serial Port

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -300\ \mu A$	2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 2$ mA			0.4	V
I_I	Input current				±10	µA
I_I	Input current, DATA-DR/CONTROL				±100	µA
C_i	Input capacitance			15		pF
C_o	Output capacitance			15		pF

† All typical values are at T_A = 25°C.

3.3.4 Receive Amplifier Input

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	A/D converter offset error (filters in)			10	70	mV
CMRR	Common-mode rejection ratio at IN+, IN–, or AUX IN+, AUX IN–	See Note 6		55		dB
r_i	Input resistance at IN+, IN– or AUX IN+, AUX IN–, REF			100		kΩ

† All typical values are at T_A = 25°C.

NOTE 6: The test condition is a 0-dBm, 1-kHz input signal with a 24-kHz conversion rate.

3.3.5 Transmit Filter Output

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset voltage at OUT+ or OUT– (single-ended relative to ANLG GND)			15	80	mV
V_{OM}	Maximum peak output voltage swing across R_L at OUT+ or OUT– (single-ended)	$R_L \geq 300\ \Omega$, Offset voltage = 0	±3			V
	Maximum peak output voltage swing between OUT+ and OUT– (differential output)	$R_L \geq 600\ \Omega$,	±6			V

† All typical values are at T_A = 25°C.

3.3.6 Receive and Transmit Channel System Distortion, SCF Clock Frequency = 432 kHz (see Note 7)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Attenuation of second harmonic of A/D input signal	single-ended	$V_I = -0.1$ dB to -24 dB		70		dB
	differential		62	70		
Attenuation of third and higher harmonics of A/D input signal	single-ended			65		dB
	differential		57	65		
Attenuation of second harmonic of D/A input signal	single-ended	$V_I = -0$ dB to -24 dB		70		dB
	differential		62	70		
Attenuation of third and higher harmonics of D/A input signal	single-ended			65		dB
	differential		57	65		

† All typical values are at $T_A = 25°C$.

3.3.7 Receive Channel Signal-to-Distortion Ratio (see Note 7)

PARAMETER	TEST CONDITIONS	A_V = 1 V/V‡		A_V = 2 V/V‡		A_V = 4 V/V‡		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
A/D channel signal-to-distortion ratio	$V_I = -6$ dB to -0.1 dB	56		§		§		dB
	$V_I = -12$ dB to -6 dB	56		56		§		
	$V_I = -18$ dB to -12 dB	53		56		56		
	$V_I = -24$ dB to -18 dB	47		53		56		
	$V_I = -30$ dB to -24 dB	41		47		53		
	$V_I = -36$ dB to -30 dB	35		41		47		
	$V_I = -42$ dB to -36 dB	29		35		41		
	$V_I = -48$ dB to -42 dB	23		29		35		
	$V_I = -54$ dB to -48 dB	17		23		29		

‡ A_V is the programmable gain of the input amplifier.
§ Measurements under these conditions are unreliable due to overrange and signal clipping.
NOTE 7: The test condition is a 1-kHz input signal with a 24-kHz conversion rate. The load impedance for the DAC is 600 Ω. Input and output voltages are referred to V_{ref}.

3.3.8 Transmit Channel Signal-to-Distortion Ratio (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
D/A channel signal-to-distortion ratio	V_I = −6 dB to −0.1 dB	58		dB
	V_I = −12 dB to −6 dB	58		
	V_I = −18 dB to −12 dB	56		
	V_I = −24 dB to −18 dB	50		
	V_I = −30 dB to −24 dB	44		
	V_I = −36 dB to −30 dB	38		
	V_I = −42 dB to −36 dB	32		
	V_I = −48 dB to −42 dB	26		
	V_I = −54 dB to −48 dB	20		

NOTE 7: The test condition is a 1-kHz input signal with a 24-kHz conversion rate. The load impedance for the DAC is 600 Ω. Input and output voltages are referred to V_{ref}.

3.3.9 Receive and Transmit Gain and Dynamic Range (see Note 8)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit gain tracking error	V_O = −48 dB to 0 dB signal range		±0.05	±0.25	dB
Receive gain tracking error	V_I = −48 dB to 0 dB signal range		±0.05	±0.25	dB

NOTE 8: Gain tracking is relative to the absolute gain at 1 kHz and 0 dB (0 dB relative to V_{ref}).

3.3.10 Receive Channel Band-Pass Filter Transfer Function, SCF f_{clock} = 432 kHz, Input (IN+ − IN−) is a ±3-V Sine Wave‡ (see Note 9)

PARAMETER	TEST CONDITION	FREQUENCY	ADJUSTMENT	MIN	TYP†	MAX	UNIT
Filter gain	Input signal reference is 0 dB	f ≤ 150 Hz	K1 × 0 dB	−33	−29	−25	dB
		f = 300 Hz	K1 × −0.26 dB	−4	−2	−1	
		f = 450 Hz to 9300 Hz	K1 × 0 dB	−0.25	0	0.25	
		f = 9300 Hz to 9900 Hz	K1 × 0 dB	−0.3	0	0.3	
		f = 9900 Hz to 10950 Hz	K1 × 0 dB	−0.5	0	0.5	
		f = 11.4 kHz	K1 × 2.3 dB		−2	−0.5	
		f = 12 kHz	K1 × 2.7 dB		−16	−14	
		f ≥ 13.2 kHz	K1 × 3.2 dB			−40	
		f ≥ 15 kHz	K1 × 0 dB			−60	

† All typical values are at T_A = 25°C.

‡ The MIN, TYP, and MAX specifications are given for a 432-kHz SCF clock frequency. A slight error in the 432-kHz SCF can result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where K1 = 100 × [(SCF frequency − 432 kHz)/432 kHz]. For errors greater than 0.25%, see Note 9.

NOTE 9: The filter gain outside of the pass band is measured with respect to the gain at 1 kHz. The filter gain within the pass band is measured with respect to the average gain within the pass band. The pass bands are 450 Hz to 10.95 kHz and 0 to 10.95 kHz for the band-pass and low-pass filters, respectively. For switched-capacitor filter clocks at frequencies other than 432 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 432 kHz.

3.3.11 Receive and Transmit Channel Low-Pass Filter Transfer Function, SCF f_{clock} = 432 kHz (see Note 9)

PARAMETER	TEST CONDITION	FREQUENCY RANGE	ADJUSTMENT ADDEND‡	MIN	TYP†	MAX	UNIT
Filter gain	Input signal reference is 0 dB	f = 0 Hz to 9300 Hz	K1 × 0 dB	−0.25	0	0.25	dB
		f = 9300 Hz to 9900 Hz	K1 × 0 dB	−0.3	0	0.3	
		f = 9900 Hz to 10950 Hz	K1 × 0 dB	−0.5	0	0.5	
		f = 11.4 kHz	K1 × 2.3 dB	−5	−2	−0.5	
		f = 12 kHz	K1 × 2.7 dB		−16	−14	
		f ≥ 13.2 kHz	K1 × 3.2 dB			−40	
		f ≥ 15 kHz	K1 × 0 dB			−60	

† All typical values are at T_A = 25°C.

‡ The MIN, TYP, and MAX specifications are given for a 432-kHz SCF clock frequency. A slight error in the 432-kHz SCF may result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where K1 = 100 × [(SCF frequency − 432 kHz)/432 kHz]. For errors greater than 0.25%, see Note 9.

NOTE 9: The filter gain outside of the pass band is measured with respect to the gain at 1 kHz. The filter gain within the pass band is measured with respect to the average gain within the pass band. The pass bands are 450 Hz to 10.95 kHz and 0 to 10.95 kHz for the band-pass and low-pass filters, respectively. For switched-capacitor filter clocks at frequencies other than 432 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 432 kHz.

3.4 Operating Characteristics Over Recommended Operating Free-Air Temperature Range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V

3.4.1 Receive and Transmit Noise (Measurement Includes Low-Pass and Band-Pass Switched-Capacitor Filters)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit noise	broadband with (sin x)/x	DX = input = 00000000000000, constant input code		280	500	μV rms
	broadband without (sin x)/x			250	450	
	0 to 12 kHz with (sin x)/x			250	400	
	0 to 12 kHz without (sin x)/x			240	400	
Receive noise (see Note 10)		Inputs grounded, gain = 1		300	500	μV rms
				18		dBrnc0

† All typical values are at T_A = 25°C.

NOTE 10: The noise is computed by statistically evaluating the digital output of the A/D converter.

3.5 Timing Requirements

3.5.1 Serial Port Recommended Input Signals

PARAMETER		MIN	MAX	UNIT
$t_{c(MCLK)}$	Master clock cycle time	95		ns
$t_{r(MCLK)}$	Master clock rise time		10	ns
$t_{f(MCLK)}$	Master clock fall time		10	ns
	Master clock duty cycle	25%	75%	
	$\overline{\text{RESET}}$ pulse duration (see Note 11)	800		ns
$t_{su(DX)}$	DX setup time before SCLK$\downarrow$	20		ns
$t_{h(DX)}$	DX hold time after SCLK$\downarrow$	$t_{c(SCLK)}/4$		ns

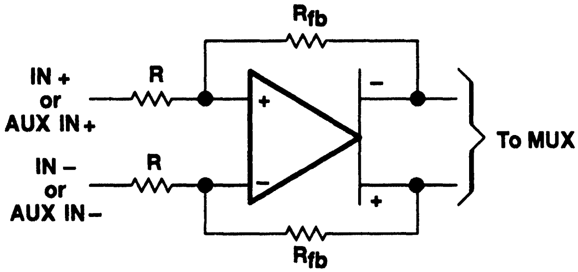
NOTE 11: $\overline{\text{RESET}}$ pulse duration is the amount of time that the reset pin is held below 0.8 V after the power supplies have reached their recommended values.

3.5.2 Serial Port – AIC Output Signals, C_L = 30 pF for SHIFT CLK Output, C_L = 15 pF For All Other Outputs

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time	380			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time		3	8	ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time		3	8	ns
	Shift clock (SCLK) duty cycle	45		55	%
$t_{d(CH\text{-}FL)}$	Delay from SCLK$\uparrow$ to $\overline{\text{FSR}}/\overline{\text{FSX}}/\overline{\text{FSD}}\downarrow$		30		ns
$t_{d(CH\text{-}FH)}$	Delay from SCLK$\uparrow$ to $\overline{\text{FSR}}/\overline{\text{FSX}}/\overline{\text{FSD}}\uparrow$		35	90	ns
$t_{d(CH\text{-}DR)}$	DR valid after SCLK$\uparrow$			90	ns
$t_{d(CH\text{-}EL)}$	Delay from SCLK$\uparrow$ to $\overline{\text{EODX}}/\overline{\text{EODR}}\downarrow$ in word mode			90	ns
$t_{d(CH\text{-}EH)}$	Delay from SCLK$\uparrow$ to $\overline{\text{EODX}}/\overline{\text{EODR}}\uparrow$ in word mode			90	ns
$t_{f(EODX)}$	$\overline{\text{EODX}}$ fall time		2	8	ns
$t_{f(EODR)}$	$\overline{\text{EODR}}$ fall time		2	8	ns
$t_{d(CH\text{-}EL)}$	Delay from SCLK$\uparrow$ to $\overline{\text{EODX}}/\overline{\text{EODR}}\downarrow$ in byte mode			90	ns
$t_{d(CH\text{-}EH)}$	Delay from SCLK$\uparrow$ to $\overline{\text{EODX}}/\overline{\text{EODR}}\uparrow$ in byte mode			90	ns
$t_{d(MH\text{-}SL)}$	Delay from MSTR CLK$\uparrow$ to SCLK$\downarrow$		65	170	ns
$t_{d(MH\text{-}SH)}$	Delay from MSTR CLK$\uparrow$ to SCLK$\uparrow$		65	170	ns

† Typical values are at T_A = 25°C.

4 Parameter Measurement Information



R_{fb} = R for D6 = 1 and D7 = 1
D6 = 0 and D7 = 0
R_{fb} = 2R for D6 = 1 and D7 = 0
R_{fb} = 4R for D6 = 0, and D7 = 1

Figure 4–1. IN+ and IN− Gain Control Circuitry

Table 4–1. Gain Control Table (Analog Input Signal Required for Full-Scale Bipolar A/D Conversion Twos Complement)†

INPUT CONFIGURATIONS	CONTROL REGISTER BITS		ANALOG INPUT‡§	A/D CONVERSION RESULT
	D6	D7		
Differential configuration Analog input = IN+ – IN– = AUX IN+ – AUX IN–	1 0	1 0	V_{ID} = ±6 V	±full scale
	1	0	V_{ID} = ±3 V	±full scale
	0	1	V_{ID} = ±1.5 V	±full scale
Single-ended configuration Analog input = IN+ – ANLG GND = AUX IN+ – ANLG GND	1 0	1 0	V_I = ±3 V	±half scale
	1	0	V_I = ±3 V	±full scale
	0	1	V_I = ±1.5 V	±full scale

† V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V
‡ V_{ID} = Differential Input Voltage, V_I = Input voltage referenced to ground with IN− or AUX IN− connected to ground.
§ In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.

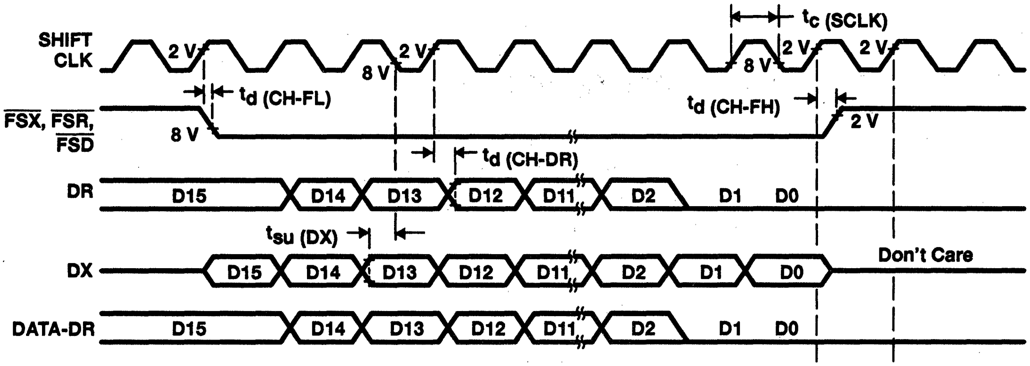


Figure 4–2. Dual-Word (Telephone Interface) Mode Timing

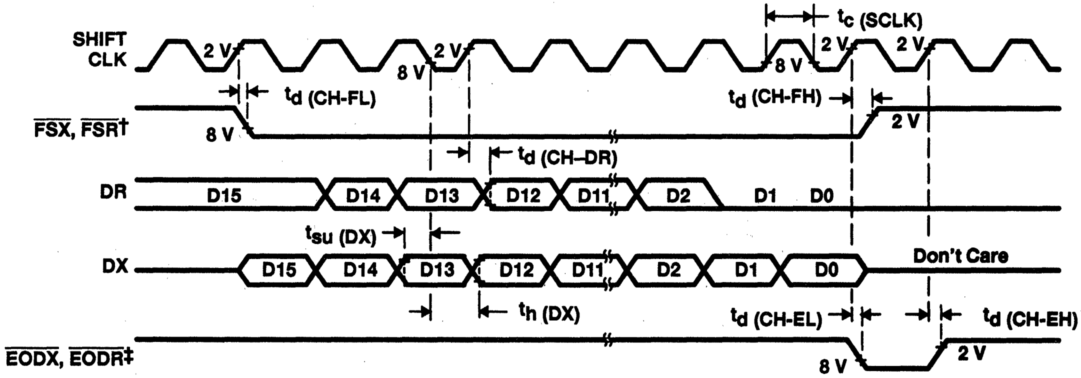


Figure 4–3. Word Timing

† The time between falling edges of $\overline{FSR}$ is the A/D conversion period and the time between falling edges of $\overline{FSX}$ is the D/A conversion period.

‡ In the word format, $\overline{EODX}$ and $\overline{EODR}$ go low to signal the end of a 16-bit data word to the processor. The word-cycle is 20 shift-clocks wide, giving a four-clock period setup time between data words.

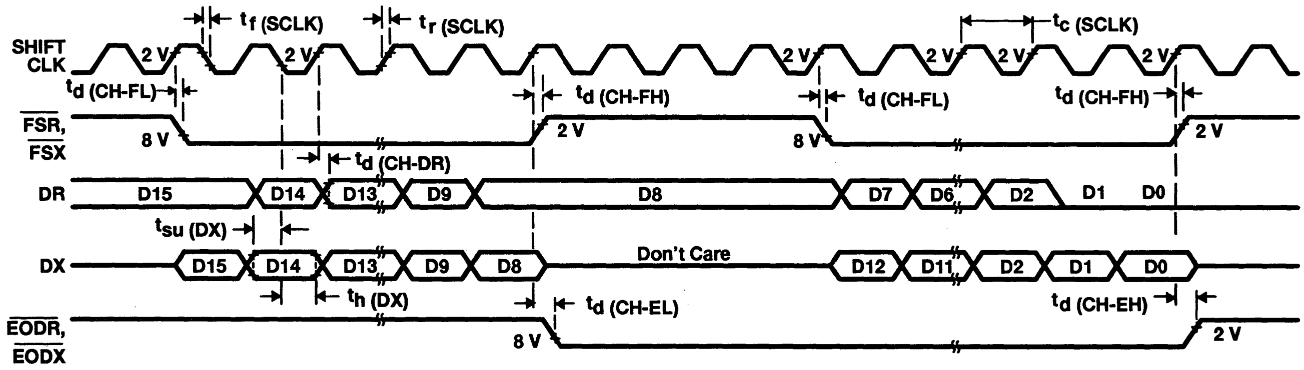


Figure 4–4. Byte-Mode Timing

†The time between falling edges of FSR is the A/D conversion period, and the time between falling edges of $\overline{\text{FSX}}$ is the D/A conversion period.

‡In the byte mode, when $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ is high, the first byte is transmitted or received, and when these signals are low, the second byte is transmitted or received. Each byte-cycle is 12 shift-clocks long, allowing for a four-shift-clock setup time between byte transmissions.

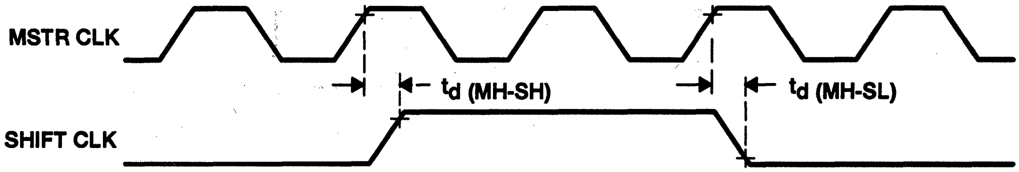


Figure 4–5. Shift-Clock Timing

4.1 TMS32047 – Processor Interface

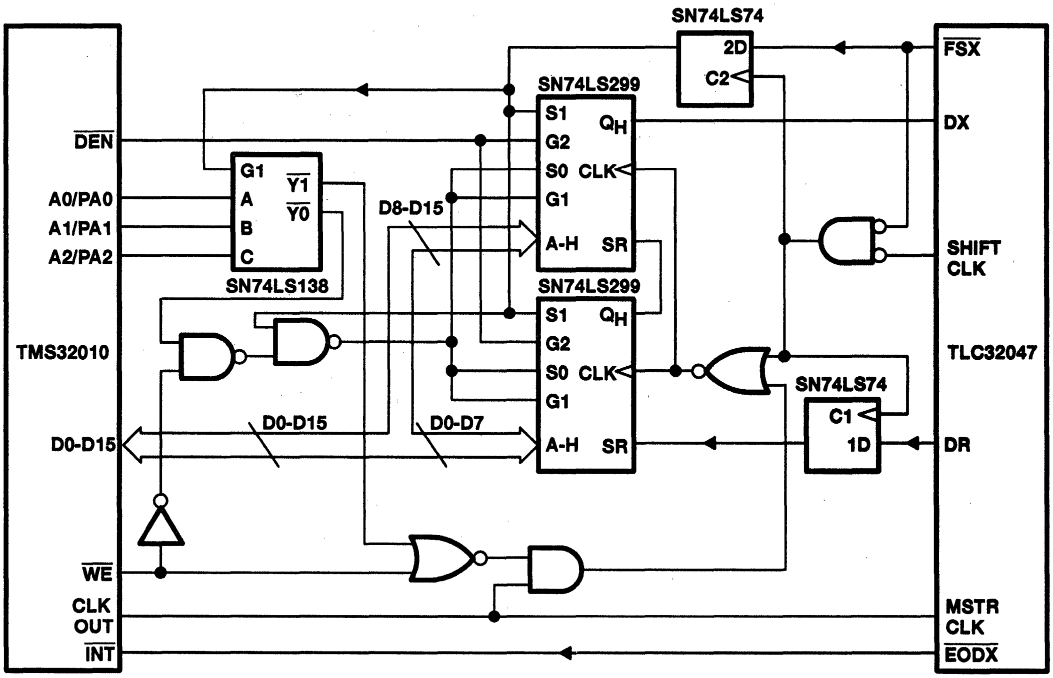
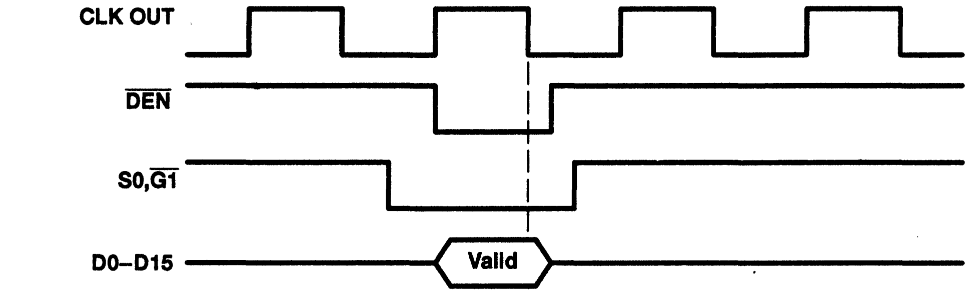
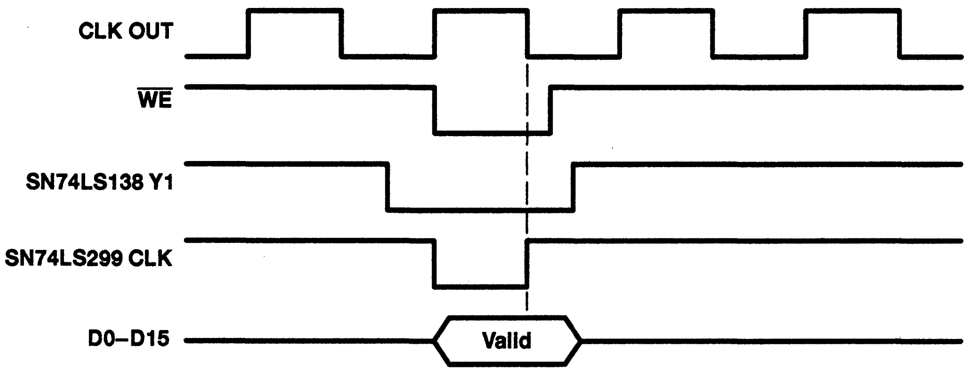


Figure 4–6. TMS32010/TMS320C15–TLC32047 Interface Circuit



(a) IN INSTRUCTION TIMING



(b) OUT INSTRUCTION TIMING

Figure 4–7. TMS32010/TMS320C15–TLC32047 Interface Timing

5 Typical Characteristics

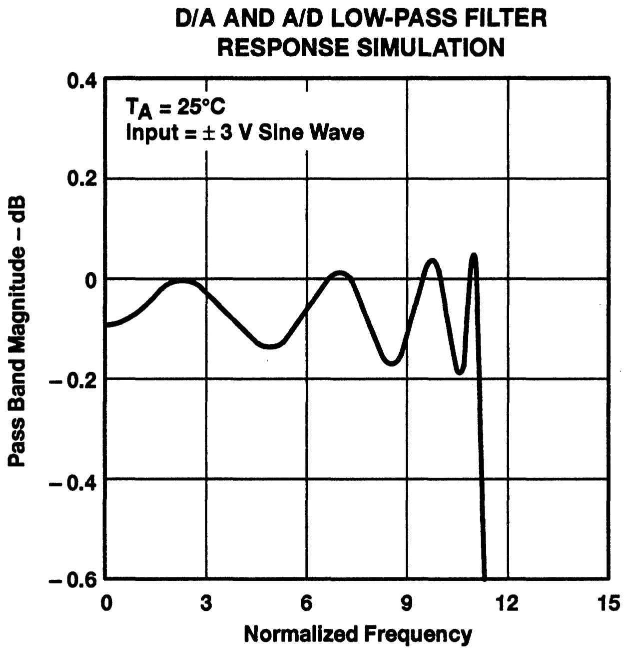


Figure 5–1

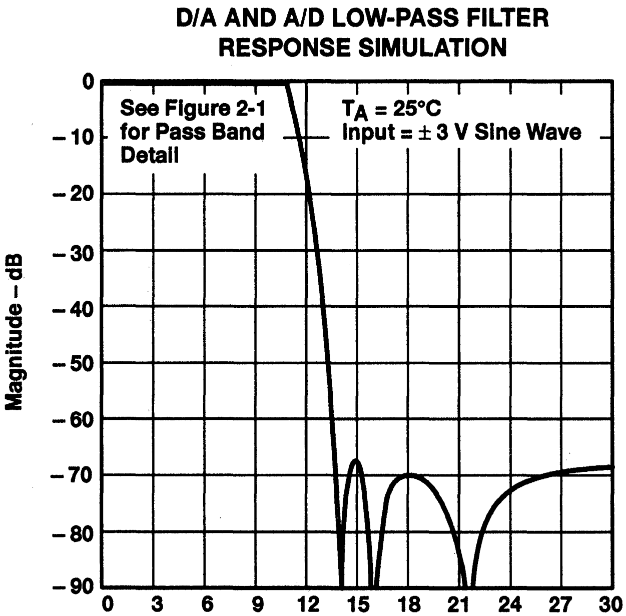


Figure 5–2

NOTE : $\text{Absolute Frequency (kHz)} = \dfrac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{432}$

D/A AND A/D LOW-PASS GROUP DELAY

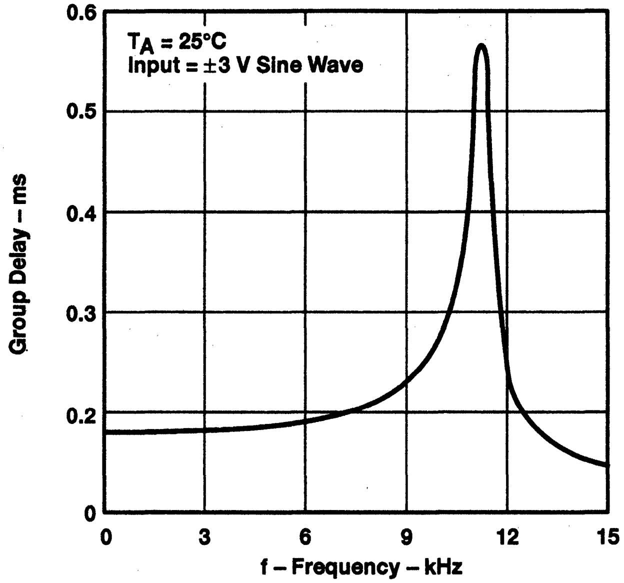


Figure 5–3

A/D BAND-PASS RESPONSE

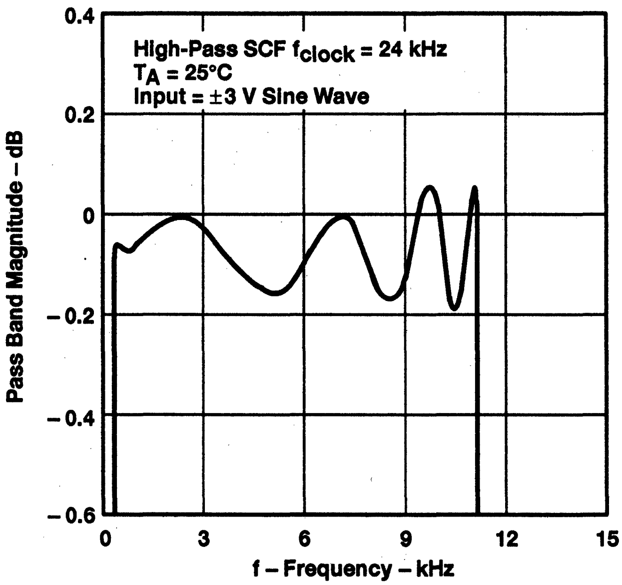


Figure 5–4

$$\text{NOTE : Absolute Frequency (kHz)} = \frac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{432}$$

A/D BAND-PASS FILTER RESPONSE SIMULATION

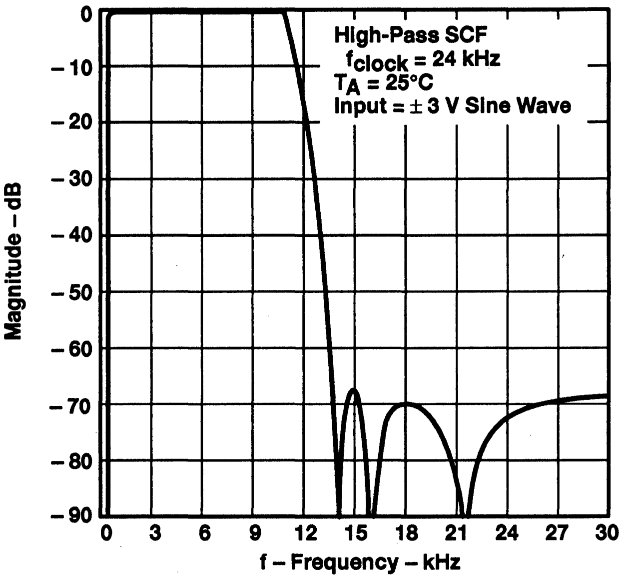


Figure 5–5

A/D BAND-PASS FILTER GROUP DELAY

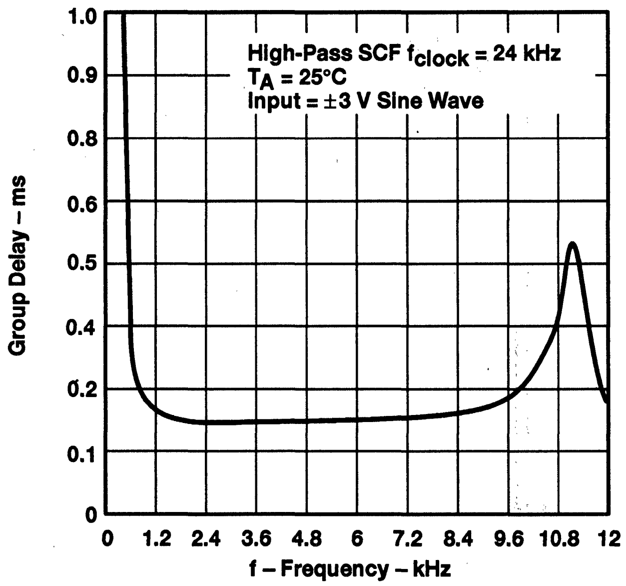


Figure 5–6

NOTE : $\text{Absolute Frequency (kHz)} = \dfrac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{432}$

A/D CHANNEL HIGH-PASS FILTER

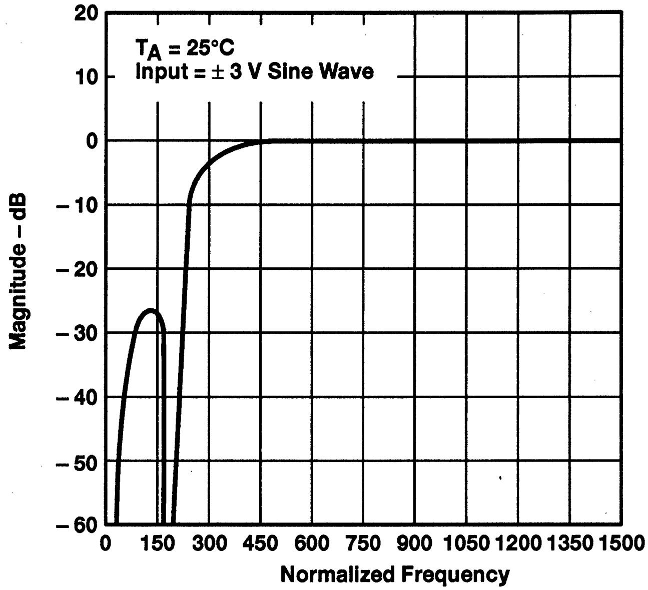


Figure 5–7

D/A (sin x)/x CORRECTION FILTER RESPONSE

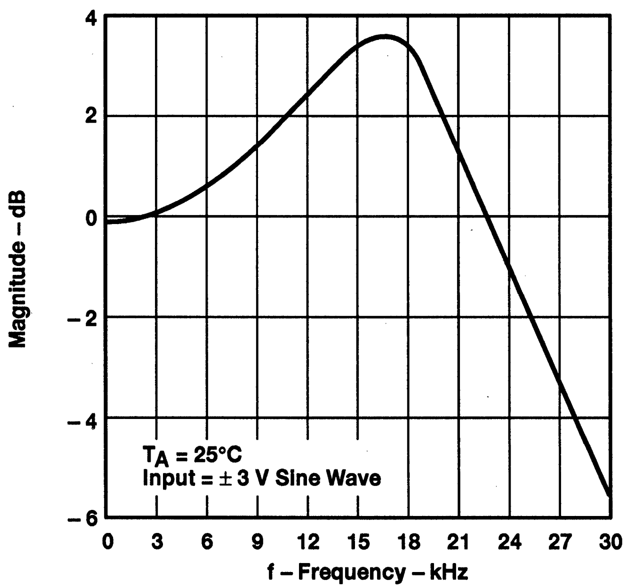


Figure 5–8

NOTE : $\text{Absolute Frequency (kHz)} = \dfrac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{432}$

D/A (sin x)/x CORRECTION FILTER RESPONSE

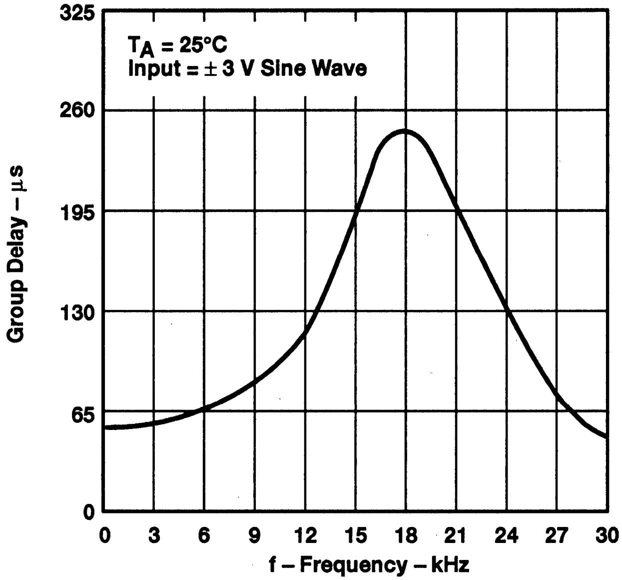


Figure 5–9

D/A (sin x)/x CORRECTION ERROR

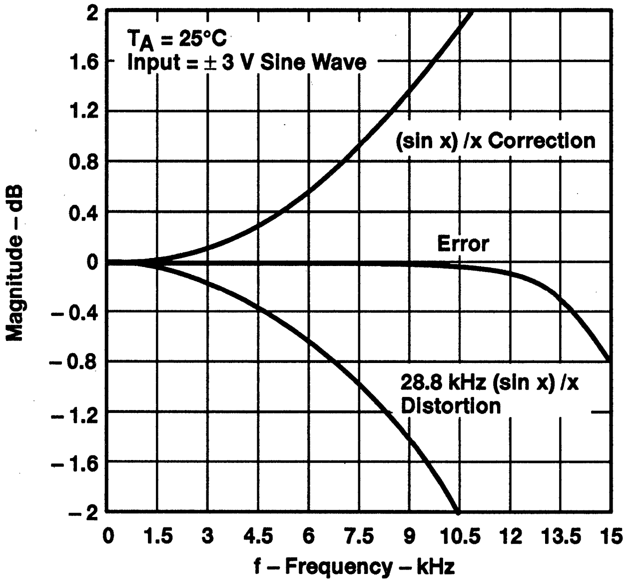


Figure 5–10

NOTE : $\text{Absolute Frequency (kHz)} = \dfrac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{432}$

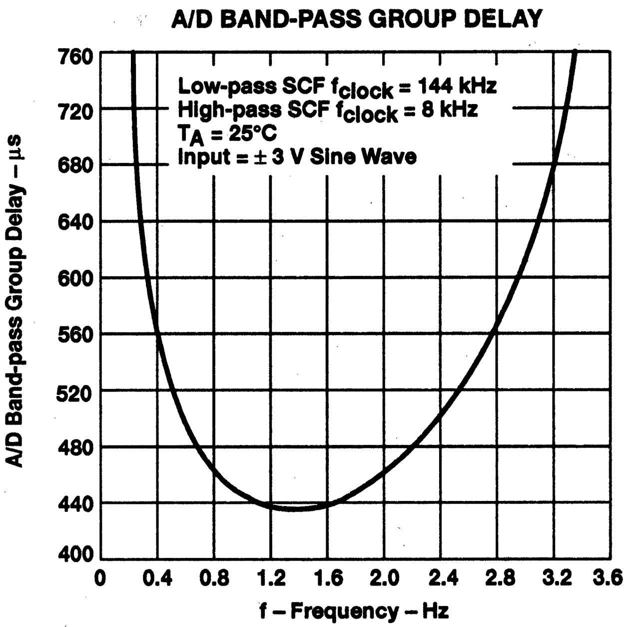


Figure 5–11

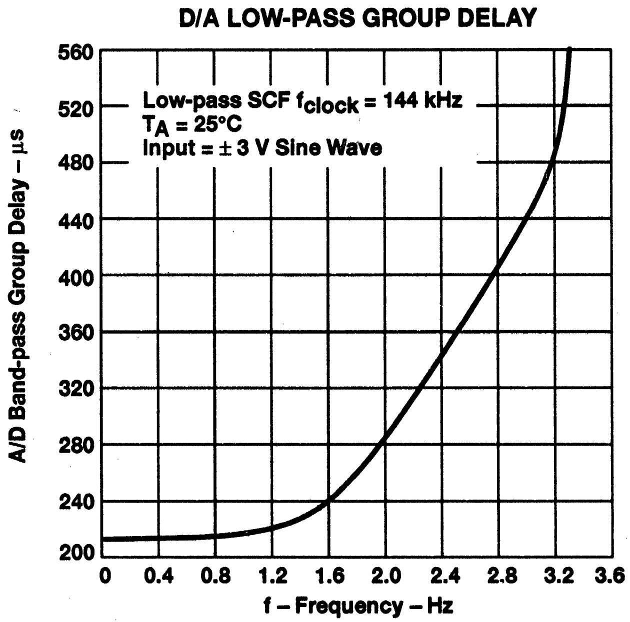


Figure 5–12

A/D SIGNAL-TO-DISTORTION RATIO vs INPUT SIGNAL

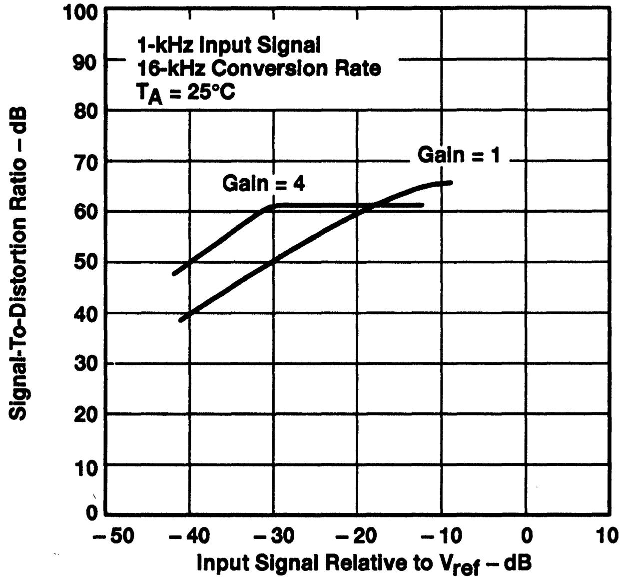


Figure 5–13

A/D GAIN TRACKING (GAIN RELATIVE TO GAIN AT 0-dB INPUT SIGNAL)

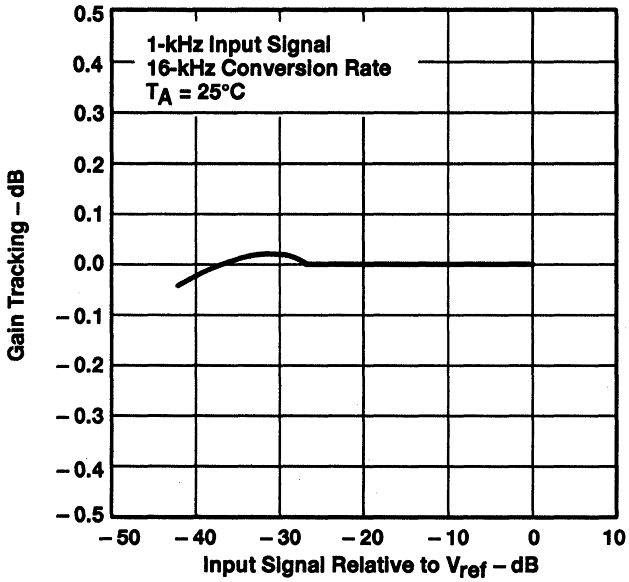


Figure 5–14

D/A CONVERTER SIGNAL-TO-DISTORTION RATIO vs INPUT SIGNAL

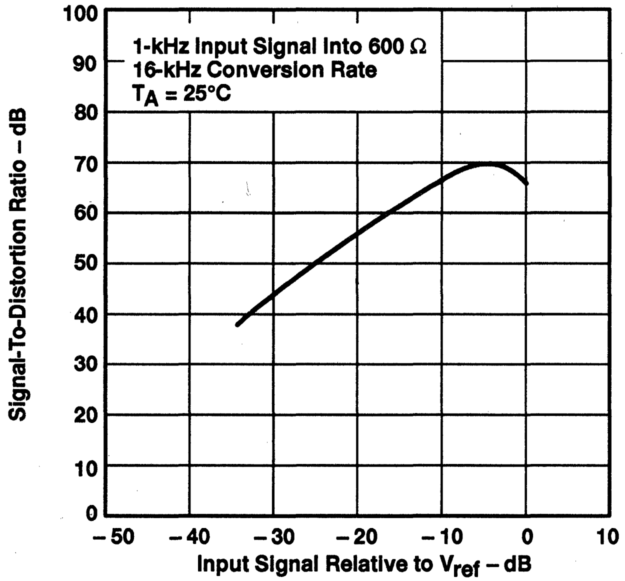


Figure 5–15

D/A GAIN TRACKING (GAIN RELATIVE TO GAIN AT 0-dB INPUT SIGNAL)

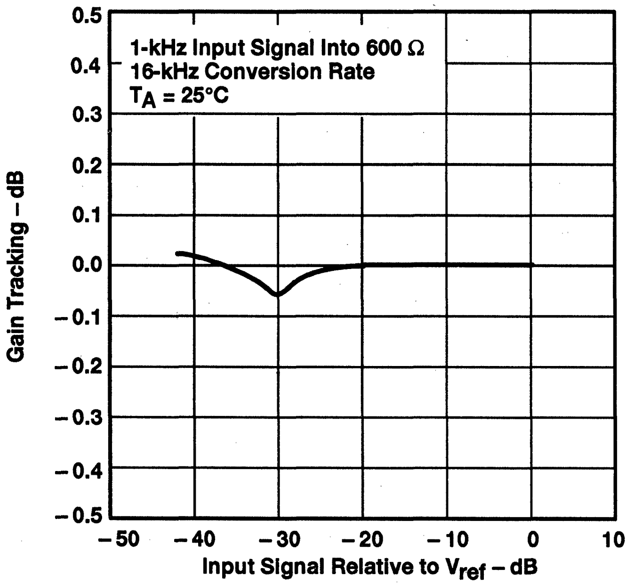


Figure 5–16

A/D SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

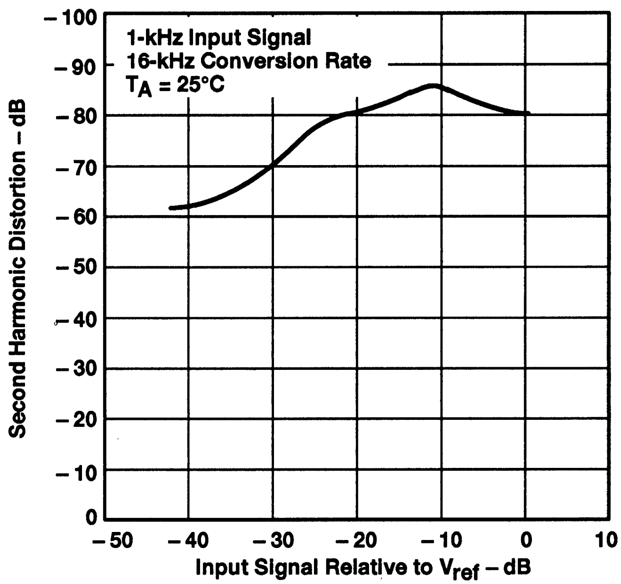


Figure 5–17

D/A SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

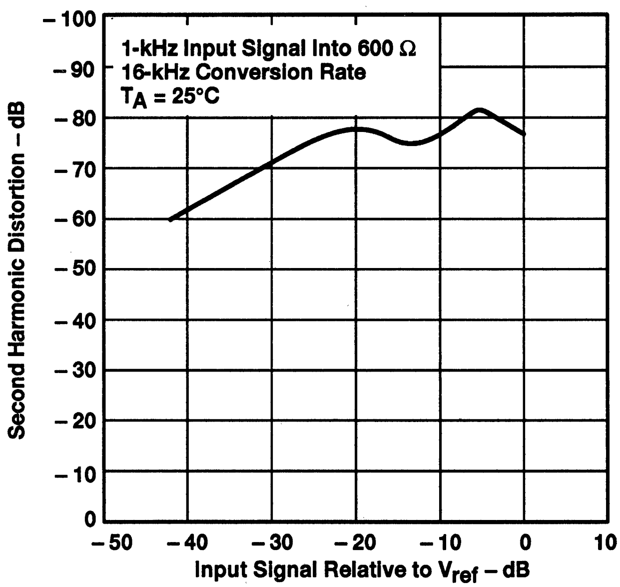


Figure 5–18

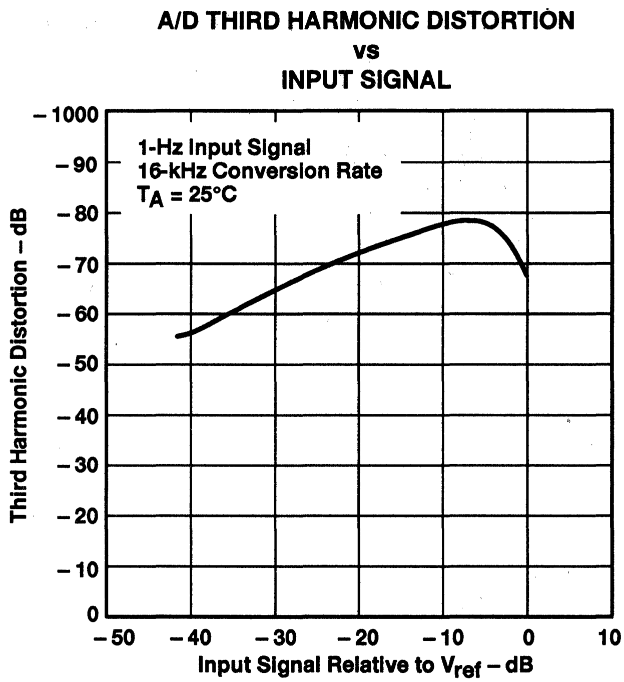


Figure 5–19

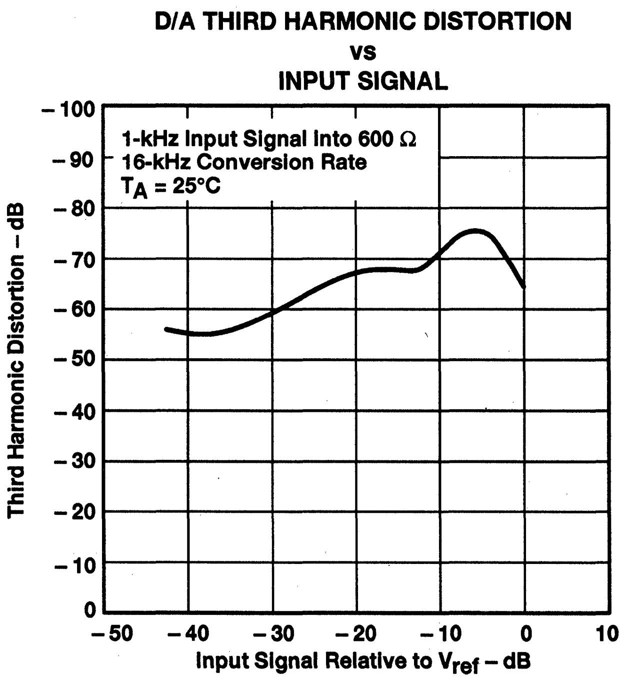


Figure 5–20

6 Application Information

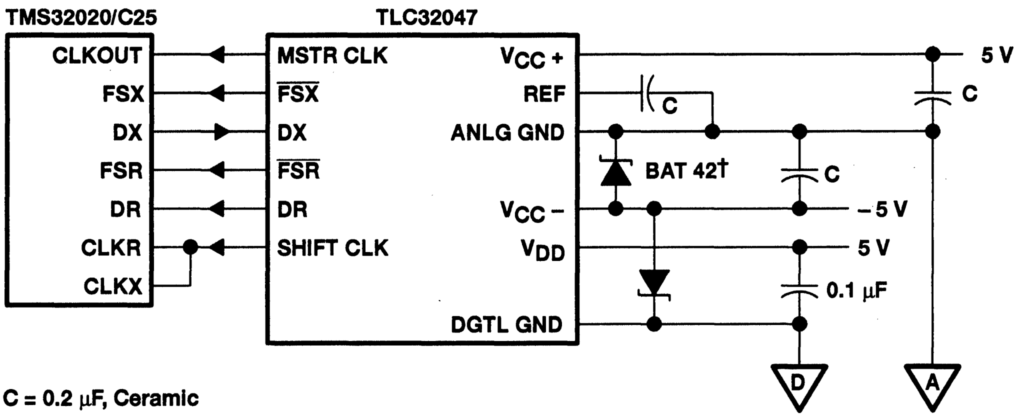


Figure 6–1. AIC Interface to the TMS32020/C25 Showing Decoupling Capacitors and Schottky Diode†

† Thomson Semiconductors

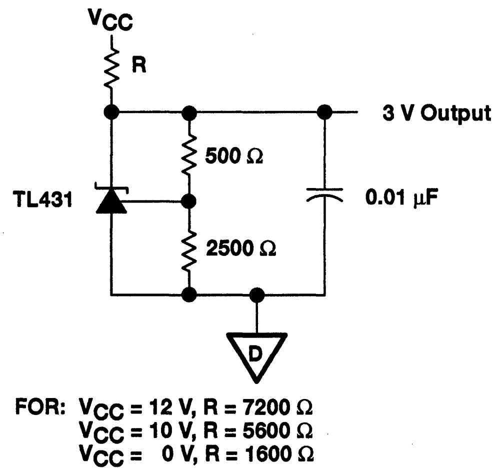


Figure 6–2. External Reference Circuit for TLC32047

TLC320AC01C
Data Manual

Single-Supply Analog Interface Circuit

TEXAS INSTRUMENTS

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1 Introduction

The TLC320AC01† analog interface circuit (AIC) is an audio-band processor that provides an analog-to-digital and digital-to-analog input/output interface system on a single monolithic CMOS chip. This device integrates a band-pass switched-capacitor antialiasing input filter, a 14-bit-resolution analog-to-digital converter (ADC), a 14-bit-resolution digital-to-analog converter (DAC), a low-pass switched-capacitor output-reconstruction filter, (sin x)/x compensation, and a serial port for data and control transfers.

The internal circuit configuration and performance parameters are determined by reading control information into the eight available data registers. The register data sets up the device for a given mode of operation and application.

The major functions of the TLC320AC01 are:

1. To convert audio-signal data to digital format by the ADC channel
2. To provide the interface and control logic to transfer data between its serial input and output terminals and a digital signal processor (DSP) or microprocessor
3. To convert received digital data back to an audio signal through the DAC channel

The antialiasing input low-pass filter is a switched-capacitor filter with a sixth-order elliptic characteristic. The high-pass filter is a single-pole filter to preserve low-frequency response as the low-pass filter cutoff is adjusted. There is a three-pole continuous-time filter that precedes this filter to eliminate any aliasing caused by the filter clock signal.

The output-reconstruction switched-capacitor filter is a sixth-order elliptic transitional low-pass filter followed by a second-order (sin x)/x correction filter. This filter is followed by a three-pole continuous-time filter to eliminate images of the filter clock signal.

The TLC320AC01 consists of two signal-processing channels, an ADC channel and a DAC channel, and the associated digital control. The two channels operate synchronously; data reception at the DAC channel and data transmission from the ADC channel occur during the same time interval. The data transfer is in 2s-complement format.

There are three basic modes of operation available: the stand-alone analog-interface mode, the master-slave mode, and the linear-codec mode. In the stand-alone mode, the TLC320AC01 generates the shift clock and frame synchronization for the data transfers and is the only AIC used. The master-slave mode has one TLC320AC01 as the master that generates the master-shift clock and frame synchronization; the remaining AICs are slaves to these signals. In the linear-codec mode, the shift clock and the frame-synchronization signals are externally generated and the timing can be any of the standard codec-timing patterns.

Typical applications for this device include modems, speech processing, analog interface for DSPs, industrial-process control, acoustical-signal processing, spectral analysis, data acquisition, and instrumentation recorders.

The TLC320AC01C is characterized for operation from 0°C to 70°C.

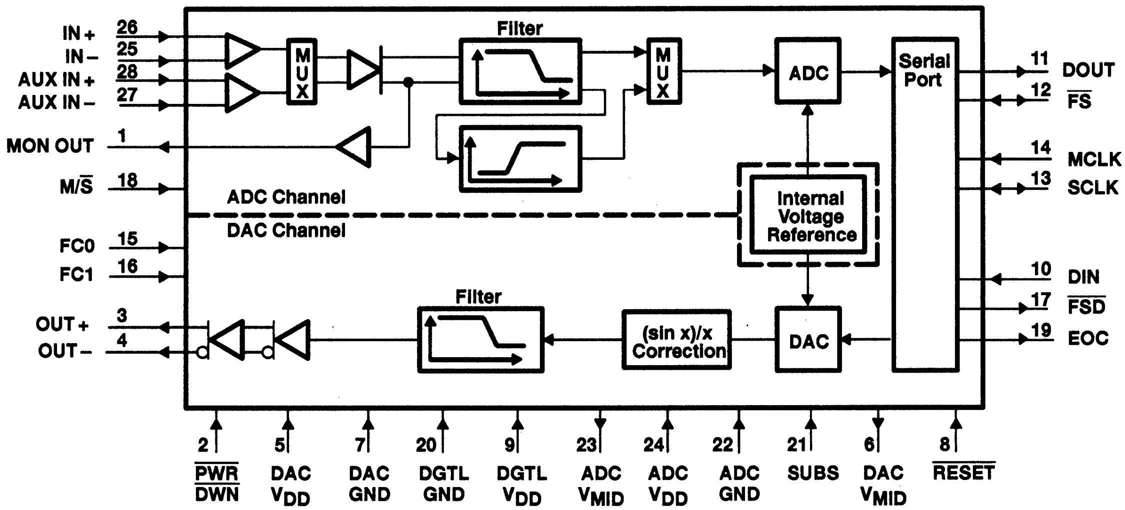
† The TLC320AC01 is functionally equivalent to the TLC320AC02 and differs in the electrical specifications as shown in Appendix C.

1.1 Features

- General-Purpose Signal-Processing Analog Front End (AFE)
- Single 5-V Power Supply
- Power Dissipation . . . 100 mW Typ
- Signal-to-Distortion Ratio . . . 70 dB Typ
- Programmable Filter Bandwidths (Up to 10.8 kHz) and Synchronous ADC and DAC Sampling
- Serial-Port Interface
- Monitor Output With Programmable Gains of 0 dB, –8 dB, –18 dB, and Squelch
- Two Sets of Differential Inputs With Programmable Gains of 0 dB, 6 dB, 12 dB, and Squelch
- Differential or Single-Ended Analog Output With Programmable Gains of 0 dB, –6 dB, –12 dB, and Squelch
- Differential Outputs Drive 3-V Peak into a 600-Ω Differential Load
- Differential Architecture Throughout
- 1-µm Advanced LinEPIC™ Process
- 14-Bit Dynamic-Range ADC and DAC
- 2s-Complement Data Format
- Application Report Available†

† Designing with the TLC320AC01 Analog Interface for DSPs (SLAA006)

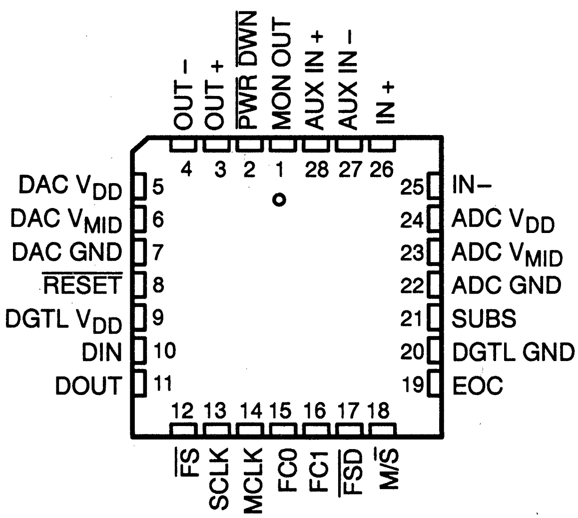
1.2 Functional Block Diagram



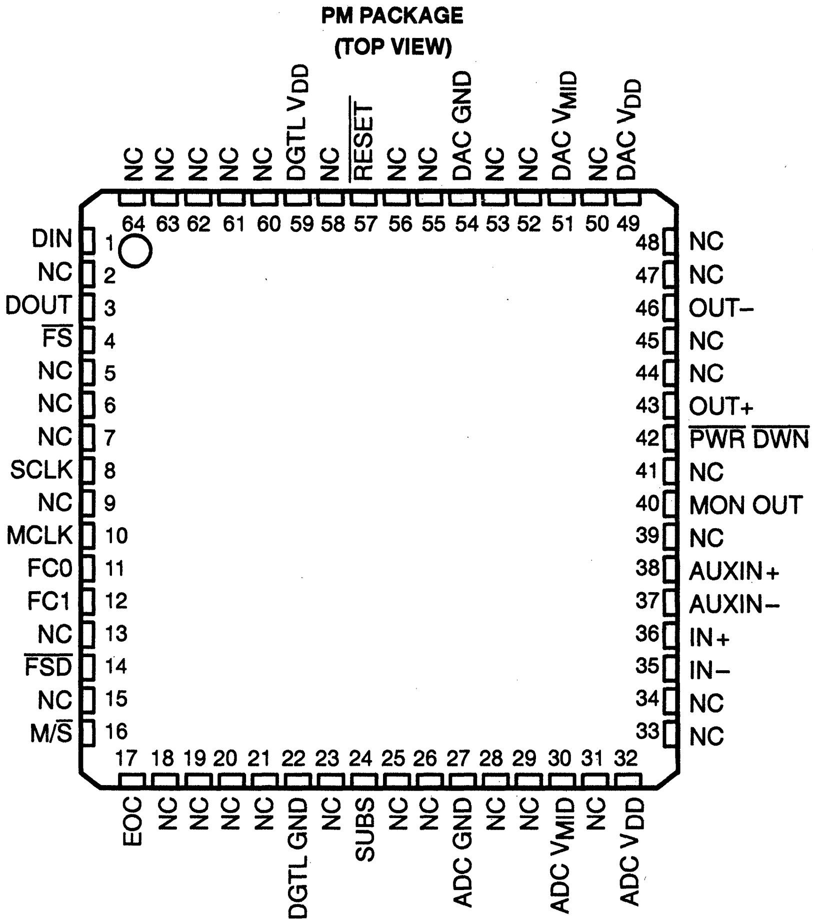
Terminal numbers shown are for the FN package.

1.3 Terminal Assignments

FN PACKAGE
(TOP VIEW)



1.3 Terminal Assignments (Continued)



NC – No internal connection

1.4 Terminal Functions

TERMINAL NAME	NO.†	NO.‡	I/O	DESCRIPTION
ADC V_{DD}	24	32	I	Analog supply voltage for the ADC channel
ADC V_{MID}	23	30	O	Midsupply for the ADC channel (requires a bypass capacitor). ADC V_{MID} must be buffered when used as an external reference.
ADC GND	22	27	I	Analog ground for the ADC channel
AUX IN+	28	38	I	Noninverting input to auxiliary analog input amplifier
AUX IN−	27	37	I	Inverting input to auxiliary analog input amplifier
DAC V_{DD}	5	49	I	Digital supply voltage for the DAC channel
DAC V_{MID}	6	51	O	Midsupply for the DAC channel (requires a bypass capacitor). DAC V_{MID} must be buffered when used as an external reference.
DAC GND	7	54	I	Analog ground for the DAC channel
DIN	10	1	I	Data input. DIN receives the DAC input data and command information and is synchronized with SCLK.
DOUT	11	3	O	Data output. DOUT outputs the ADC data results and register read contents. DOUT is synchronized with SCLK.
DGTL V_{DD}	9	59	I	Digital supply voltage for control logic
DGTL GND	20	22	I	Digital ground for control logic
EOC	19	17	O	End-of-conversion output. EOC goes high at the start of the ADC conversion period and low when conversion is complete. EOC remains low until the next ADC conversion period begins and indicates the internal device conversion period.
FC0	15	11	I	Hardware control input. FC0 is used in conjunction with FC1 to request secondary communication and phase adjustments. FC0 should be tied low if it is not used.
FC1	16	12	I	Hardware control input. FC1 is used in conjunction with FC0 to request secondary communication and phase adjustments. FC1 should be tied low if it is not used.
$\overline{FS}$	12	4	I/O	Frame synchronization. When $\overline{FS}$ goes low, DIN begins receiving data bits and DOUT begins transmitting data bits. In master mode, $\overline{FS}$ is low during the simultaneous 16-bit transmission to DIN and from DOUT. In slave mode, $\overline{FS}$ is externally generated and must be low for one shift-clock period minimum to initiate the data transfer.
$\overline{FSD}$	17	14	O	Frame-synchronization delayed output. This active-low output synchronizes a slave device to the frame synchronization timing of the master device. $\overline{FSD}$ is applied to the slave $\overline{FS}$ input and is the same duration as the master $\overline{FS}$ signal but delayed in time by the number of shift clocks programmed in the $\overline{FSD}$ register.
IN+	26	36	I	Noninverting input to analog input amplifier
IN−	25	35	I	Inverting input to analog input amplifier
MCLK	14	10	I	The master-clock input drives all the key logic signals of the AIC.
MON OUT	1	40	O	The monitor output allows monitoring of analog input and is a high-impedance output.
M/$\overline{S}$	18	16	I	Master/slave select input. When M/$\overline{S}$ is high, the device is the master and when low, it is a slave.

† Terminal numbers shown are for the FN package.
‡ Terminal numbers shown are for the PM package.

1.4 Terminal Functions (Continued)

TERMINAL NAME	NO.†	NO.‡	I/O	DESCRIPTION
OUT+	3	43	O	Noninverting output of analog output power amplifier. OUT+ can drive transformer hybrids or high-impedance loads directly in a differential connection or a single-ended configuration with a buffered V_{MID}.
OUT–	4	46	O	Inverting output of analog output power amplifier. OUT– is functionally identical with and complementary to OUT+.
$\overline{\text{PWR DWN}}$	2	42	I	Power-down input. When $\overline{\text{PWR DWN}}$ is taken low, the device is powered down such that the existing internally programmed state is maintained. When $\overline{\text{PWR DWN}}$ is brought high, full operation resumes.
$\overline{\text{RESET}}$	8	57	I	Reset input that initializes the internal counters and control registers. $\overline{\text{RESET}}$ initiates the serial data communications, initializes all of the registers to their default values, and puts the device in a preprogrammed state. After a low-going pulse on $\overline{\text{RESET}}$, the device registers are initialized to provide a 16-kHz data-conversion rate and 7.2-kHz filter bandwidth for a 10.368-MHz master clock input signal.
SCLK	13	8	I/O	Shift clock. SCLK clocks the digital data into DIN and out of DOUT during the frame-synchronization interval. When configured as an output (M/$\overline{\text{S}}$ high), SCLK is generated internally by dividing the master clock signal frequency by four. When configured as an input (M/$\overline{\text{S}}$ low), SCLK is generated externally and synchronously to the master clock. This signal clocks the serial data into and out of the device.
SUBS	21	24	I	Substrate connection. SUBS should be tied to ADC GND.

† Terminal numbers shown are for the FN package.
‡ Terminal numbers shown are for the PM package.

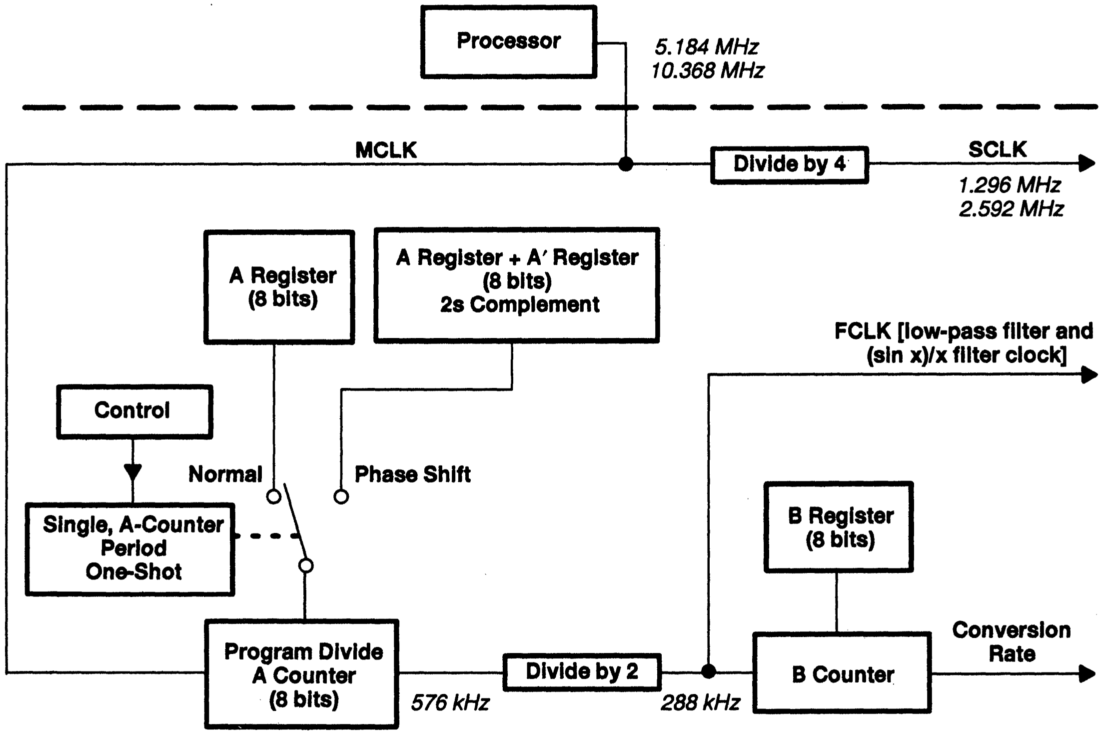


Figure 1–1. Control Flow Diagram

Table 1–1. Operating Frequencies

FCLK (kHz)	LOW-PASS FILTER BANDWIDTH (kHz)	B REGISTER CONTENTS (Program No. of Filter Clocks) (Decimal)	CONVERSION RATE (kHz)	HIGH-PASS POLE FREQUENCY (Hz)
144	3.6	20 (see Note 1)	7.2	36
		18	8	40
		15	9.6	48
		10 (see Note 2)	14.4	72
288	7.2	20 (see Note 1)	14.4	72
		18	16	80
		15	19.2	96
		10 (see Notes 2 and 3)	28.8	144
432	10.8	20 (see Note 1)	21.6	108
		18	24	120
		15 (see Note 3)	28.8	144
		10 (see Notes 2 and 3)	43.2	216

NOTES: 1. The B register can be programmed for values greater than 20; however, since the sample rate is lower than 7.2 kHz and the internal filter remains at 3.6 kHz, an external antialiasing filter is required.

2. When the B register is programmed for a value less than 10, the ADC and the DAC conversions are not completed before the next frame-sync signal and the results are in error.

3. The maximum sampling rate for the ADC channel is 43.2 kHz. The maximum rate for the DAC channel is 25 kHz.

1.5 Register Functional Summary

There are nine data registers that are used as follows:

Register 0 — The No-op register. The 0 address allows phase adjustments to be made without reprogramming a data register.

Register 1 — The A register controls the count of the A counter.

Register 2 — The B register controls the count of the B counter.

Register 3 — The A′ register controls the phase adjustment of the sampling period. The adjustment is equal to the register value multiplied by the input master period.

Register 4 — The amplifier gain register controls the gains of the input, output, and monitor amplifiers.

Register 5 — The analog configuration register controls:

- The addition/deletion of the high-pass filter to the ADC signal path
- The enable/disable of the analog loopback
- The selection of the regular inputs or auxiliary inputs
- The function that allows processing of signals that are the sum of the regular inputs and the auxiliary inputs ($V_{IN} + V_{AUX\ IN}$)

Register 6 — The digital configuration register controls:

- Selection of the free-run function
- $\overline{\text{FSD}}$ [frame-synchronization (sync) delay] output enable/disable
- Selection of 16-bit function
- Forcing secondary communications
- Software reset
- Software power down

Register 7 — The frame-sync delay register controls the time delay between the master-device frame sync and slave-device frame sync. Register 7 must be the last register programmed when using slave devices since all register data is latched and valid on the sixteenth falling edge of SCLK. On the sixteenth falling edge of SCLK, all delayed frame-sync intervals are shifted by this programmed amount.

Register 8 — The frame-sync number register informs the master device of the number of slaves that are connected in the chain. The frame-sync number is equal to the number of slaves plus one.

2 Detailed Description

2.1 Definitions and Terminology

ADC Channel	All signal processing circuits between the analog input and the digital conversion results at DOUT
Codec Mode	The operating mode under which the device receives shift clock and frame-sync signals from a host processor. The device has no slaves.
d	The d represents valid programmed or default data in the control register format (see Section 2.19, Secondary Serial Communications) when discussing other data-bit portions of the register.
Dxx	Bit position in the primary data word (xx is the bit number)
DAC Channel	All signal processing circuits between the digital data word applied to DIN and the differential output analog signal available at OUT+ and OUT–
Data Transfer Interval	The time during which data is transferred from DOUT and to DIN. This interval is 16 shift clocks regardless of whether the shift clock is internally or externally generated. The data transfer is initiated by the falling edge of the frame-sync signal.
DSxx	Bit position in the secondary data word (xx is the bit number)
FCLK	An internal clock frequency that is a division of MCLK that controls the low-pass filter and (sinx)/x filter clock (see Figure 1–1 and Table 1-1).
f_i	The analog input frequency of interest
Frame Sync	The falling edge of the signal that initiates the data-transfer interval. The primary frame sync starts the primary communications, and the secondary frame sync starts the secondary communications.
Frame Sync and Sampling Period	The time between falling edges of successive primary frame-sync signals
Frame-Sync Interval	The time period occupied by 16 shift clocks. Regardless of the mode of operation, there is always an internal frame-sync interval signal that goes low on the rising edge of SCLK and remains low for 16 shift clocks. It is used for synchronization of the serial-port internal signals. It goes high on the seventeenth rising edge of SCLK.
f_s	The sampling frequency that is the reciprocal of the sampling period.
Host	Any processing system that interfaces to DIN, DOUT, SCLK, or $\overline{FS}$.
Master Mode	The operating mode under which the device generates and uses its own shift clock and frame-sync signal and generates all delayed frame-sync signals necessary to support slave devices.
Phase Adjustment	The programmed time variation from the falling edge of one frame-sync signal to the falling edge of the next frame sync signal. The time variation is determined by the contents of the A′ register. Since the time between falling edges of successive frame-sync signals is the the sampling period, the sampling period is adjusted.
Primary (Serial) Communications	The digital data-transfer interval. Since the device is synchronous, the signal data words from the ADC channel and to the DAC channel occur simultaneously.
Secondary (Serial) Communications	The digital control and configuration data-transfer interval into DIN and the register read-data cycle from DOUT. The data-transfer interval occurs when requested by hardware or software.
Signal Data	The input signal and all of the converted representations through the ADC channel and return through the DAC channel to the analog output. This is contrasted with the purely digital software-control data.
Slave Mode	The operating mode under which the device receives shift clock and frame-sync signals from a master device.

Stand-Alone Mode — The operating mode under which the device generates and uses its own shift clock and frame-sync signal. The device has no slave devices.

X — The X represents a don't-care bit position within the control register format.

2.2 Reset and Power-Down Functions

2.2.1 Reset

The TLC320AC01 resets both the internal counters and registers, including the programmed registers, by any of the following:

- Applying power to the device, causing a power-on reset (POR)
- Applying a low reset pulse to $\overline{\text{RESET}}$
- Reading in the programmable software reset bit (DS01 in register 6)

$\overline{\text{PWR}}\ \overline{\text{DWN}}$ resets the counters only and preserves the programmed register contents.

2.2.2 Conditions of Reset

The two internal reset signals used for the reset and synchronization functions are as follows:

1. Counter reset: This signal resets all flip-flops and latches that are not externally programmed with the exception of those generating the reset pulse itself. In addition, this signal resets the software power-down bit.

   Counter reset = power-on reset + $\overline{\text{RESET}}$ + RESET bit + $\overline{\text{PWR}}\ \overline{\text{DWN}}$

2. Register reset: This signal resets all flip-flops and latches that are not reset by the counter reset except those generating the reset pulse itself.

   Register reset = power-on reset + $\overline{\text{RESET}}$ + RESET bit

Both reset signals are at least one master-clock period long and release on the falling edge of the master clock.

2.2.3 Software and Hardware Power-Down

Given the definitions and conditions of $\overline{\text{RESET}}$, the software-programmed power-down condition is cleared by resetting the software bit (DS00 in register 6) to zero. It is also cleared by either cycling the power to the device, bringing $\overline{\text{PWR}}\ \overline{\text{DWN}}$ low, or bringing $\overline{\text{RESET}}$ low.

$\overline{\text{PWR}}\ \overline{\text{DWN}}$ powers down the entire chip (< 1 mA). The software-programmable power-down bit only powers down the analog section of the chip (< 3 mA), which allows a software power-up function. Cycling $\overline{\text{PWR}}\ \overline{\text{DWN}}$ high to low and back to high resets all flip-flops and latches that are not externally programmed, thereby preserving the register contents.

When $\overline{\text{PWR}}\ \overline{\text{DWN}}$ is not used, it should be tied high.

2.2.4 Register Default Values After POR, Software Reset, or $\overline{\text{RESET}}$ Is Applied

Register 1 – The A Register

The default value of the A-register data is decimal 18 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	0	1	0

Register 2 – The B Register

The default value of the B-register data is decimal 18 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	0	1	0

Register 3 – The A′ Register

The default value of the A′-register data is decimal 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

Register 4 – The Amplifier Gain-Select Register

The default value of the amplifier gain-select register data is shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	1	0	1

Register 5 – The Analog Control Configuration Register

The power-up and reset conditions are as shown below. In the read mode, eight bits are read but the four LSBs are repeated as the four MSBs.

DS03	DS02	DS01	DS00
0	0	0	1

Register 6 – The Digital Configuration Register

The default value of DS07 – DS00 is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

Register 7 – The Frame-Sync Delay Register

The default value of DS07 – DS00 is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

Register 8 – The Frame-Sync Number Register

The default value of DS07 – DS00 is 1 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	1

2.3 Master-Slave Terminal Function

Table 2–1 describes the function of the master/slave ($M/\overline{S}$) input. The only difference between master and slave operations in the TLC320AC01 is that SCLK and $\overline{FS}$ are outputs when $M/\overline{S}$ is high and inputs when $M/\overline{S}$ is low.

Table 2–1. Master-Slave Selection

MODE	$M/\overline{S}$†	$\overline{FS}$	SCLK
Master and Stand Alone	H	Output	Output
Slave and Codec Emulation	L	Input	Input

† When the stand-alone mode is desired or when the device is permanently in the master mode, $M/\overline{S}$ must be high.

2.4 ADC Signal Channel

To produce excellent common-mode rejection of unwanted signals, the analog signal is processed differentially until it is converted to digital data. The signal is amplified by the input amplifier at one of three software selectable gains (typically 0 dB, 6 dB, or 12 dB). A squelch mode can also be programmed for the input amplifier.

The amplifier output is filtered and applied to the ADC input. The ADC converts the signal into discrete digital words in 2s-complement format corresponding to the analog-signal value at the sampling time. These 16-bit digital words, representing sampled values of the analog input signal, are clocked out of the serial port (DOUT), one word for each primary communication interval. During secondary communications, the data previously programmed into the registers can be read out with the appropriate register address and with the read bit set to 1. When a register read is not requested, all 16 bits are 0.

2.5 DAC Signal Channel

DIN receives the 16-bit serial data word (2s complement) from the host during the primary communications interval and latches the data on the seventeenth rising edge of SCLK. The data are converted to an analog voltage by the DAC with a sample and hold and then through a (sin x)/x correction circuit and a smoothing filter. An output buffer with three software-programmable gains (0 dB, −6 dB, and −12 dB), as shown in register 4, drives the differential outputs OUT+ and OUT−. A squelch mode can also be programmed for the output buffer. During secondary communications, the configuration program data are read into the device control registers.

2.6 Serial Interface

The digital serial interface consists of the shift clock, the frame-synchronization signal, the ADC-channel data output, and the DAC-channel data input. During the primary 16-bit frame-synchronization interval, the SCLK transfers the ADC channel results from DOUT and transfers 16-bit DAC data into DIN.

During the secondary frame-synchronization interval, the SCLK transfers the register read data from DOUT when the read bit is set to a 1. In addition, the SCLK transfers control and device parameter information into DIN. The functional sequence is shown in Figure 2–1.

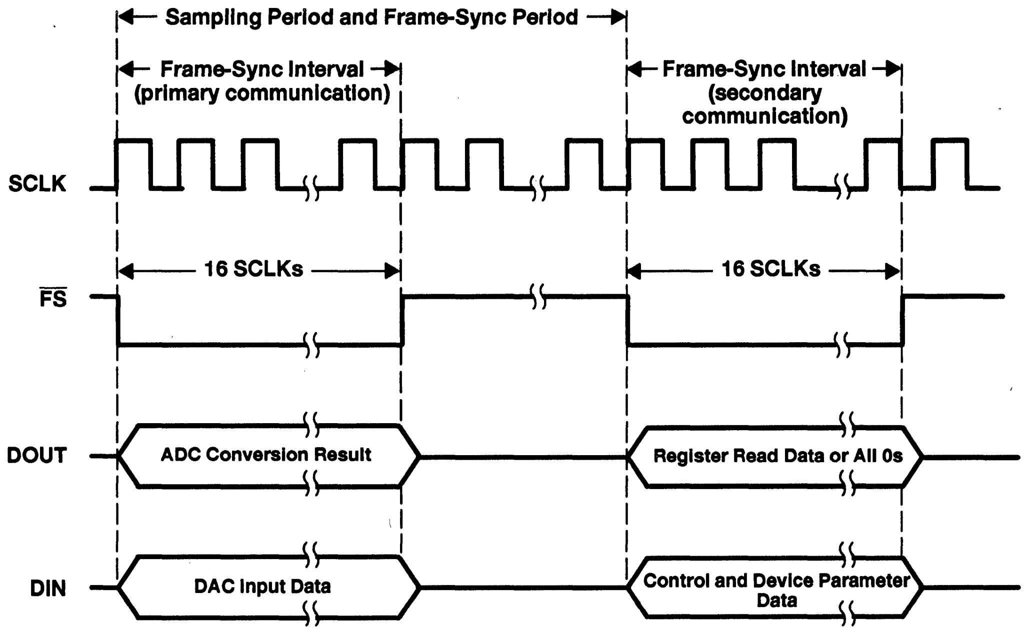


Figure 2–1. Functional Sequence for Primary and Secondary Communication

2.7 Number of Slaves

The number of slaves is determined by the sum of the individual device delays from the frame-sync ($\overline{FS}$) input low to the frame-sync delayed ($\overline{FSD}$) low for all slaves as follows:

$$(n) \times tp(FS-FSD) < 1/2 \text{ shift-clock period}$$

Where:

n is the number of slave devices.

Example:

From the above equation, the number of slaves is given by:

$$(n) \le \frac{1}{2} \times (\text{SCLK period}) \times \frac{1}{tp(FS - FSD)}$$

assuming the shift clock is 2.4 MHz and tp(FS – FSD) is 40 ns, then the number of slaves is:

$$n \le \frac{1}{2.4 \text{ MHz}} \times \frac{1}{2} \times \frac{1}{40 \text{ ns}} = \frac{1000}{192} = 5.2$$

The maximum number of slaves under these conditions is five. As the SCLK increases in frequency, the number of slaves that can be used decreases.

2.8 Operating Frequencies

2.8.1 Master and Stand-Alone Operating Frequencies

The sampling (conversion) frequency is derived from the master-clock (MCLK) input by the following equation:

$$f_S = \text{Sampling (conversion) frequency} = \frac{\text{MCLK}}{(\text{A register value}) \times (\text{B register value}) \times 2}$$

The inverse is the time between the falling edges of two successive primary frame-synchronization signals. The input and output data clock (SCLK) is given by:

$$\text{SCLK frequency} = \frac{\text{MCLK frequency}}{4}$$

2.8.2 Slave and Codec Operating Frequencies

The slave and codec conversion and the data frequencies are determined by the externally applied SCLK and $\overline{\text{FS}}$ signals.

2.9 Switched-Capacitor Filter Frequency (FCLK)

The filter clock (FCLK) is an internal clock signal that determines the filter band-pass frequency and is the B counter clock. The frequency of the filter clock is derived by the following equation:

$$\text{FCLK} = \frac{\text{MCLK}}{(\text{A register value}) \times 2}$$

2.10 Filter Bandwidths

The low-pass (LP) filter −3 dB corner is derived by:

$$f\ (\text{LP}) = \frac{\text{FCLK}}{40} = \frac{\text{MCLK}}{40 \times (\text{A register value}) \times 2}$$

The high-pass (HP) filter −3 dB corner is derived by:

$$f\ (\text{HP}) = \frac{\text{Sampling frequency}}{200} = \frac{\text{MCLK}}{200 \times 2 \times (\text{A register value}) \times (\text{B register value})}$$

2.11 Required Minimum Number of MCLK Periods

The number of MCLKs necessary for proper operation when only the primary communications are used is:

Total number of MCLKs = (16 + 2) SCLKs × 4 MCLKs per SCLK
= 72 MCLKs minimum

The number of MCLKs necessary for proper operation if both the primary and secondary communications are used is:

Total number of MCLKs = (16 + 2) SCLKs × 2 × 4 MCLKs per SCLK
= 144 MCLKs minimum

Even though the TLC320AC01 can perform with this number of MCLKs, the host may need more time to execute the required software instructions between primary and secondary communication intervals.

2.12 Master and Stand-Alone Modes

The difference between the master and stand-alone modes is that in the stand-alone mode there are no slave devices. Functionally these two modes are the same. In both, the AIC internally generates the shift clock and frame-sync signal for the serial communications. These signals and the filter clock (FCLK) are derived from the input master clock.The master clock applied at the MCLK input determines the internal device timing. The shift clock frequency is a divide-by-four of the master clock frequency and shifts both the input and output data at DIN and DOUT, respectively, during the frame-sync interval (16 shift clocks long). To begin the communication sequence, the device is reset (see Section 2.2.1, Reset), and the first frame sync occurs approximately 648 master clocks after the reset condition disappears.

2.12.1 Register Programming

All register programming occurs during secondary communications, and data is latched and valid on the sixteenth falling edge of SCLK. After a reset condition, eight primary and secondary communications cycles are required to set up the eight programmable registers. Registers 1 through 8 are programmed in secondary communications intervals 1 through 8, respectively. If the default value for a particular register is desired, that register does not need to be addressed during the secondary communications. The no-op command addresses the pseudo-register (register 0), and no register programming takes place during this communications. The no-op command allows phase shifts of the sampling period without reprogramming any register.

During the eight register programming cycles, DOUT is in the high-impedance state. DOUT is released on the rising edge of the eighth primary internal frame-sync interval. In addition, each register can be read back during DOUT secondary communications by setting the read bit to 1 in the appropriate register. Since the register is in the read mode, no data can be written to the register during this cycle. To return this register to the write mode requires a subsequent secondary communication (see Section 2.19, Secondary Serial Communications for detailed register description).

2.12.2 Master and Stand-Alone Functional Sequence

The A counter counts according to the contents of the A register, and the A counter frequency is divided by two to produce the filter clock (FCLK). The B counter is clocked by FCLK with the following functional sequence:

1. The B counter starts counting down from the B register value minus one. Each count remains in the counter for one FCLK period including the zero count. This total counter time is referred to as the B cycle. The end of the zero count is called the end of B cycle.
2. When the B counter gets to a count of nine, the analog-to-digital (A-to-D) conversion starts.
3. The A-to-D conversion is complete ten FCLK periods later.
4. $\overline{\text{FS}}$ goes low on a rising edge of SCLK after the A-to-D conversion is complete. That rising edge of SCLK must be preceded by a falling edge of SCLK, which is the first falling edge to occur after the end of B cycle.
5. The D-to-A conversion cycle begins on the rising edge of the internal frame-sync interval and is complete ten FCLK periods later.

2.13 Slave and Codec Modes

The only difference between the slave and codec modes is that the codec mode is controlled directly by the host and does not use a delayed frame-sync signal. In both modes, the shift clock and the frame sync are both externally generated and must be synchronous with MCLK. The conversion frequency is set by the time interval of externally applied frame-sync falling edges except when the free-run function is selected by bit 5 of register 6 (see Section 2.15.4, Free-Run Mode). The slave device or devices share the shift clock generated by the master device but receive the frame sync from the previous slave in the chain. The Nth slave $\overline{\text{FS}}$ receives the (N−1)st slave $\overline{\text{FSD}}$ output and so on. The first slave device in the chain receives $\overline{\text{FSD}}$ from the master.

2.13.1 Slave and Codec Functional Sequence

The A counter counts according to the contents of the A register, and the A counter frequency is divided by two to produce the FCLK. The device function in the slave or codec mode is the same as steps 1 through 3 of the B cycle description in the master mode but differs as follows:

1. Same as master
2. Same as master
3. Same as master
4. All internal clocks stop 1/2 FCLK before the end of count 0 in the B counter cycle.
5. All internal clocks are restarted on the first rising edge of MCLK after the external $\overline{FS}$ input goes low. This operation provides the synchronization necessary when using an external $\overline{FS}$ signal.
6. The D-to-A conversion starts on the rising edge of the internally generated frame-sync interval at the end of the 16-shift clock data transfer.

In the slave mode, the master controls the phase adjustments for itself and all slaves since all devices are programmed in the same frame-sync interval. In the codec mode, the shift clock and frame sync are externally generated and provide the timing for the ADC and DAC if the free-run function has not been selected (see Section 2.15.4, Free-Run Mode). In the codec mode, there is usually no need for phase adjustments; however, any required phase adjustments must be made by adjusting the external frame-sync timing (sampling time).

2.13.2 Slave Register Programming

When slave devices are used on power-up or reset, all slave frame-sync signals occur at the same time as the master frame-sync signal and all slave devices are programmed during the master secondary frame-sync interval with the same data as the master. The last register programmed must be the frame-sync delay (FSD) register because the delay starts immediately on the rising edge of the seventeenth shift clock of that frame- sync interval. After the FSD register programming is completed for the master and slave, the slave primary frame interval is shifted in time (time slot allocated) according to the data contained in the slave FSD registers. The master then generates frame-sync intervals for itself and each slave to synchronize the host serial port for data transfers for itself and all slave devices.

The number of slaves is specified in the FSN register (register 8); therefore, the number of frame-sync intervals generated by the master is equal to the number of slaves plus one (see Section 2.7, Number of Slaves). These master frame-sync intervals are separated in time by the delay time specified by the FSD register (register 7). These master-generated intervals are the only frame-sync interval signals applied to the host serial port to provide the data-transfer time slot for the slave devices.

2.14 Terminal Functions

2.14.1 Frame-Sync Function

The frame-sync signal indicates that the device is ready to send and receive data for both master and slave modes. The data transfer begins on the falling edge of the frame-sync signal.

2.14.1.1 Frame Sync ($\overline{FS}$), Master Mode

The frame sync is generated internally. $\overline{FS}$ goes low on the rising edge of SCLK and remains low for the 16-bit data transfer. In addition to generating its own frame-sync interval, the master also outputs a frame sync for each slave that is being used.

2.14.1.2 Frame-Sync Delayed ($\overline{FSD}$), Master Mode

For the master, the frame-sync delayed output occurs 1/2 shift-clock period ahead of $\overline{FS}$ to compensate for the time delay through the master and slave devices. The timing relationships are as follows:

1. When the FSD register data is 0, then $\overline{FSD}$ goes low on the falling edge of SCLK prior to the rising edge of SCLK when $\overline{FS}$ goes low (see Figure 4–4).
2. When the FSD register data is greater than 16, then $\overline{FSD}$ goes low on a rising edge of SCLK that is the FSD register number of SCLKs after the falling edge of $\overline{FS}$.

Register data values from 1 to 16 result in the default register value of zero.

2.14.1.3 Frame Sync ($\overline{FS}$), Slave Mode

The frame-sync timing is generated externally, applied to $\overline{FS}$, and controls the ADC and DAC timing (see Section 2.15.4, Free-Run Mode). The external frame-sync width must be a minimum of one shift clock to be recognized and can remain low until the next data frame is required.

2.14.1.4 Frame-Sync Delayed ($\overline{FSD}$), Slave Mode

This output is fed from the master to the first slave and the first slave $\overline{FSD}$ output to the second and so on down the chain. The FSD timing sequence in the slave mode is as follows:

1. When the FSD register data is 0, then $\overline{FSD}$ goes low after $\overline{FS}$ goes low (see Figure 4–5).
2. When the FSD register data is greater than 16, $\overline{FSD}$ goes low on a rising edge of SCLK that is the FSD register number of SCLKs after the falling edge of $\overline{FS}$.

Data values from 1 to 16 are constrained because the data transfer requires 16 clock periods.

2.14.2 Data Out (DOUT)

DOUT is placed in the high-impedance state on the seventeenth rising edge of SCLK (internal or external) after the falling edge of frame sync. In the primary communication, the data word is the ADC conversion result. In the secondary communication, the data is the register read results when requested by the read/write (R/$\overline{W}$) bit with the eight MSBs set to 0 (see Section 2.16, Serial Communications). If no register read is requested, the secondary word is all zeroes.

2.14.2.1 Data Out, Master Mode

In the master mode, DOUT is taken from the high-impedance state by the falling edge of frame sync. The most significant data bit then appears on DOUT.

2.14.2.2 Data Out, Slave Mode

In the slave mode, DOUT is taken from the high-impedance state by the falling edge of the external frame sync or the rising edge of the external SCLK, whichever occurs first (see Figure 4–7). The falling edge of frame sync can occur ±1/4 SCLK period around the SCLK rising edge (see Figure 4–3). The most significant data bit then appears on DOUT.

2.14.3 Data In (DIN)

In the primary communication, the data word is the digital input signal to the DAC channel. In the secondary communication, the data is the control and configuration data to set up the device for a particular function (see Section 2.16, Serial Communications).

2.14.4 Hardware Program Terminals (FC1 and FC0)

These inputs provide for hardware programming requests for secondary communication or phase adjustment. These inputs work in conjunction with the control bits D01 and D00 of the primary data word or control bits DS15 and DS14 of the secondary data word. The data on FC1 and FC0 are latched on the rising edge of the next internally generated primary or secondary frame-sync interval. These inputs should be tied low if not used (see Section 2.17, Request for Secondary Serial Communication and Table 2–3).

2.14.5 Midpoint Voltages (ADC V_{MID} and DAC V_{MID})

Since the device operates at a single-supply voltage, two midpoint voltages are generated for internal signal processing. ADC V_{MID} is used for the ADC channel reference, and DAC V_{MID} is used for the DAC channel reference. Two references minimize channel-to-channel noise and crosstalk. ADC V_{MID} and DAC V_{MID} must be buffered when used as a reference for external signal processing.

2.15 Device Functions

2.15.1 Phase Adjustment

In some applications, such as modems, the device sampling period may require an adjustment to synchronize with the incoming bit stream to improve the signal-to-noise ratio. The TLC320AC01 can adjust the sampling period through the use of the A′ register and the control bits.

2.15.1.1 Phase-Adjustment Control

A phase adjustment is a programmed variation in the sampling period. A sampling period is adjusted according to the data value in the A′ register, and the phase adjustment is that number of master clocks (MCLK). An adjustment is made during device operation with data bits D01 and D00 in the primary communication, with data bits DS15 and DS14 in the secondary word or in combination with the hardware terminals FC1 and FC0 (see Table 2–3). This adjustment request is latched on the rising edge of the next internal frame-sync interval and is only valid for the next sampling period. To repeat the phase adjustment, another phase request must be initiated.

2.15.1.2 Use of the A′ Register for Phase Adjustment

The A′ register value makes slight timing adjustments to the sampling period. The sampling period increases or decreases according to the sign of the programmed A′ register value and the state of data bits D01 and D00 in the primary data word.

The general equation for the conversion frequency is given as:

$$f_s = \text{conversion frequency} = \frac{\text{MCLK}}{(2 \times \text{A register value} \times \text{B register value}) \pm (\text{A}' \text{ register value})}$$

Therefore, if A′ = 0, the device conversion (sampling) frequency and period is constant.

If a nonzero A′ value is programmed, the sampling frequency and period responds as shown in Table 2–2.

Table 2–2. Sampling Variation With A′

D01	D00	SIGN OF THE A′ REGISTER VALUE	
		PLUS VALUE (+)	NEGATIVE VALUE (–)
0	1 (increase command)	Frequency decreases, period increases	Frequency increases, period decreases
1	0 (decrease command)	Frequency increases, period decreases	Frequency decreases, period increases

An adjustment to the sampling period, which must be requested through D01 and D00 of the primary data word to DIN, is valid for the following sampling period only. When the adjustment is required for the subsequent sampling period, it must be requested again through D01 and D00 of the primary data word. For each request, only the sampling period occurring immediately after the primary data word request is affected.

The amount of time shift in the entire sampling period ($1/f_S$) is as follows:

When the sampling period is set to 125 μs (8 kHz), the A′ register is loaded with decimal 10 and the TLC320AC01 master clock frequency is 10.386 MHz. The amount of time each sampling period is increased or decreased, when requested, is:

Time shift = (A′ register value) × (MCLK period)

The device changes the entire sampling period by only the MCLK period times the A′ register value.

Change in sampling period = contents of A′ register × master clock period
= 10 × 96.45 ns = 964 ns (less than 1% of the sampling period)

The sampling period changes by 964.5 ns each time the phase adjustment is requested by the primary data word (i.e., once per sampling period).

It is evident then that the change in sampling period is very small compared to the sampling period. To observe this effect over a long period of time (> sampling period), this change must be continuously requested by the primary data word. If the adjustment is not requested again, the sampling period changes only once and it may appear that there was no execution of the command. This is especially true when bench testing the device. Automatic test equipment can test for results within a single sampling period.

Internally, the A′ register value only affects one cycle (period) of the A counter. The A and A′ values are additive, but only for one A-counter period. The A counter begins the first count at the default or programmed A-register value and counts down to the A′-register value. As the A′ value increases or decreases, the first clock cycle from the A counter is lengthened or shortened. The initial A-counter period is the only counter period affected by the A′ register such that only this single period is increased or decreased.

2.15.2 Analog Loopback

This function allows the circuit to be tested remotely. In loopback, OUT+ and OUT– are internally connected to IN+ and IN–. The DAC data bits D15 to D02 that are applied to DIN can be compared with the ADC output data bits D15 to D02 at DOUT. There are some differences due to the ADC and DAC channel offset. The loopback function is implemented by setting DS01 and DS00 to zero in control register 5 (see Section 2.19, Secondary Serial Communications).

2.15.3 16-Bit Mode

In the 16-bit mode, the device ignores the last two control bits (D01 and D00) of the primary word and requests continual secondary communications to occur. By ignoring the last two primary communication bits, compatibility with existing 16-bit software can be maintained. This function is implemented by setting bit DS03 to 1 in register 6. To return to normal operation, DS03 must be reprogrammed to 0.

2.15.4 Free-Run Mode

With the free-run bit set in register 6, the external shift clock and frame sync control only the data transfer. The ADC and DAC timing are controlled by the A and B register values, and the phase-shift adjustment must be done as if the device is in stand-alone mode (by the software or the state of FC1 and FC0).

Phase adjustment cannot be made by adjustment of the frame-sync timing. The external frame sync must occur within 1/2 FCLK period of the internal frame sync (FCLK as determined by the values of the A and B registers).

When the external frame sync occurs simultaneously with the internal load, the data-transfer request by the external frame sync takes precedence over an internal load command. The latching of the ADC conversion data in the output register is inhibited until the current 16 bits are shifted out of the register by the shift clock.

2.15.5 Force Secondary Communication

With bit 2 in register 6 set to 1, secondary communication is requested continuously. It overrides all software and hardware requests concerning secondary communication. Phase shifting, however, can still be performed with the software and hardware.

2.15.6 Enable Analog Input Summing

By setting bits DS01 and DS00 to 11 in register 5, the normal analog input voltage is summed with the auxiliary input voltage. The gain for the analog input amplifier is set by data bits DS03 and DS02 in register 4.

2.15.7 DAC Channel (sin x)/x Error Correction

The (sin x)/x compensation filter is designed for zero (sin x)/x error using a B-register value of 15. Since the filter cannot be removed from the signal path, operation using another B-register value results in an error in the reconstructed analog output. The error is given by the following equation. Any error compensation needed by a given application can be performed in the software.

$$\text{DAC channel frequency response error} = 20 \times \log_{10}\left[\frac{\sin\left(\frac{2\pi \times A \times B}{f_{MCLK}} \times f\right)}{\sin\left(\frac{30\pi \times A}{f_{MCLK}} \times f\right)} \times \frac{15}{B}\right]$$

where:

- f = the frequency of interest
- f_{MCLK} = the TLC320AC01 master-clock frequency
- A = the A-register value
- B = the B-register value

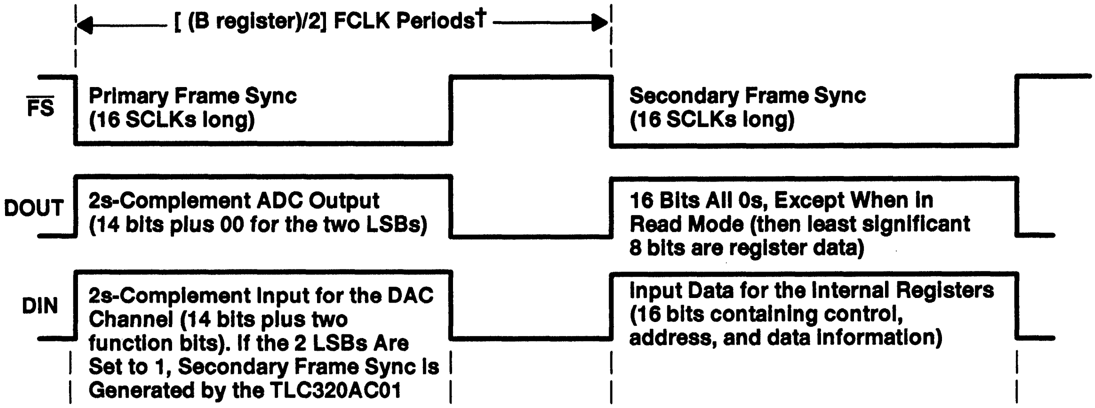
and the arguments of the sin functions are in radians.

2.16 Serial Communications

2.16.1 Stand-Alone and Master-Mode Word Sequence and Information Content During Primary and Secondary Communications

For the stand-alone and master modes, the sequence in Figure 2–2 shows the relationship between the primary and secondary communications interval, the data content into DIN, and the data content from DOUT.

The TLC320AC01 can provide a phase-shift command or the next secondary communications interval by decoding 1) the programmed state of the FC1 and FC0 inputs and the D01 and D00 data bits in the primary data word, or 2) the state of the FC1 and FC0 inputs and the DS15 and DS14 data bits in the secondary data word (see Table 2–3). When DS13 (the R/$\overline{W}$ bit) is the default value of 0, all 16 bits from DOUT are 0 during secondary communication. However, when the R/$\overline{W}$ bit is set to 1 in the secondary communication control word, the secondary transmission from DOUT still contains 0s in the eight MSBs. The lower order eight bits contain the data of the register currently being addressed. This function provides register status information for the host.

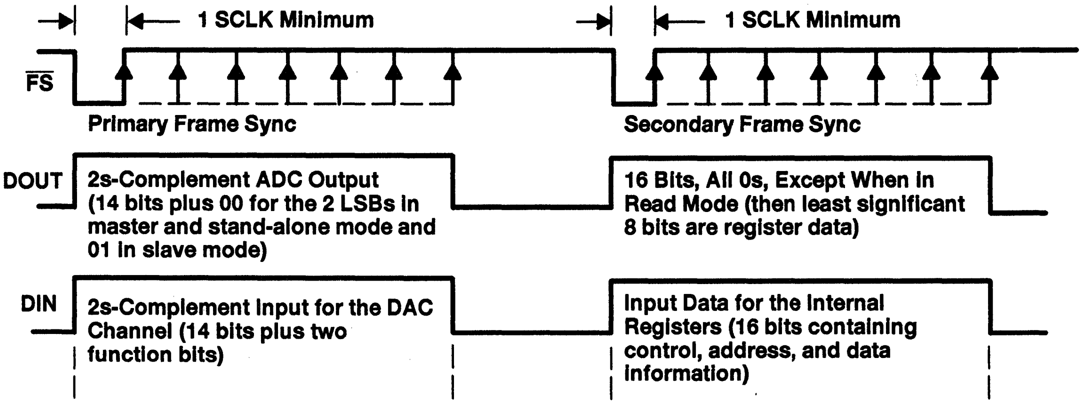


† The time between the primary and secondary frame sync is the time equal to filter clock (FCLK) period multiplied by the B-register contents divided by two. The time interval is rounded to the nearest shift clock. The secondary frame-sync signal goes from high to low on the next shift clock low-to-high transition after (B register/2) filter clock periods.

Figure 2–2. Master and Stand-Alone Functional Sequence

2.16.2 Slave- and Codec-Mode Word Sequence and Information Content During Primary and Secondary Communications

For the slave and codec modes, the sequence is basically the same as the stand-alone and master modes with the exception that the frame sync and the shift clock are generated and controlled externally as shown in Figure 2–3. For the codec mode, the frame-sync pulse width needs to be a minimum of one shift clock long. The timing relationship between the frame sync and shift clock is shown in the timing diagrams. Phase shifting is usually not required in the slave or codec mode because the frame-sync timing can be adjusted externally if required.



NOTE: The time between the primary and secondary frame syncs is determined by the application; however, enough time must be provided so that the host can execute the required number of software instructions in the time between the end of the primary data transfer (rising edge of the primary frame-sync interval) and the falling edge of the secondary frame sync (start of secondary communications).

Figure 2–3. Slave and Codec Functional Sequence

2.17 Request for Secondary Serial Communication and Phase Shift

The following paragraphs describe a request for secondary serial communication and phase shift using hardware control inputs FC1 and FC0, primary data bits D01 and D00, and secondary data bits DS15 and DS14.

2.17.1 Initiating a Request

Combinations of FC1 and FC0 input conditions, bits D01 and D00 in the primary serial data word, FC1 and FC0, and bits DS15 and DS14 in the secondary serial data word can initiate a secondary serial communication or request a phase shift according to the following rules (see Table 2–3).

1. Primary word phase shifts can be requested by either the hardware or software when the other set of signals are 11 or 00. If both hardware and software request phase shifts, the software request is performed.
2. Secondary words can be requested by either the software or hardware at the same time that the other set of signals is requesting a phase shift.
3. Hardware inputs FC1 and FC0 are ignored during the secondary word unless DS15 and DS14 are 11. When DS15 and DS14 are 01 or 10, the corresponding phase shift is performed. When DS15 and DS14 are 00, no phase shift is performed even when the hardware requests a phase shift.

2.17.2 Normal Combinations of Control

The normal combinations of control are as follows:

1. Use D01 and D00 and DS15 and DS14 to request phase shifts and secondary words by holding FC1 and FC0 to 00.
2. Use FC1 and FC0 exclusively to request phase shifts and secondary words by holding D01 and D00 to 00 and DS15 and DS14 to 11.
3. Use D01 and D00 only to request secondary words and FC1 and FC0 to perform phase shifts once per period by holding DS15 and DS14 to 00.

2.17.3 Additional Control Options

Additional control options are unusual and are rarely needed or used; however, they are as follows:

1. Use D01 and D00 only to request secondary words and FC1 and FC0 to perform phase shifts twice per period by holding DS15 and DS14 to 11.
2. Use FC1 and FC0 exclusively to request secondary words and D01 and D00 and DS15 and DS14 to perform phase shifts twice per period.
3. Use FC1 and FC0 to perform the phase shift after the primary word and DS15 and DS14 to perform a phase shift after the secondary word by holding D01 and D00 to 11.

Table 2–3. Software and Hardware Requests for Secondary Serial-Communication and Phase-Shift Truth Table

WITHIN PRIMARY OR SECONDARY DATA WORD	CONTROL BITS		HARDWARE TERMINALS		PHASE-SHIFT ADJUSTMENT (see Section 2.15.1)		SECONDARY REQUEST (see Note 1)
	D01	D00	FC1	FC0	EARLIER	LATER	
Primary	0	0	0	0	0	0	0
	0	0	0	1	0	1	0
	0	0	1	0	1	0	0
	0	0	1	1	0	0	1
	0	1	0	0	0	1	0
	0	1	0	1	0	1	0
	0	1	1	0	0	1	0
	0	1	1	1	0	1	1
	1	0	0	0	1	0	0
	1	0	0	1	1	0	0
	1	0	1	0	1	0	0
	1	0	1	1	1	0	1
	1	1	0	0	0	0	1
	1	1	0	1	0	1	1
	1	1	1	0	1	0	1
	1	1	1	1	0	0	1
Secondary	DS15	DS14	FC1	FC0	EARLIER	LATER	No request can be made for secondary communication within the secondary word.
	0	0	0	0	0	0	
	0	0	0	1	0	0	
	0	0	1	0	0	0	
	0	0	1	1	0	0	
	0	1	0	0	0	1	
	0	1	0	1	0	1	
	0	1	1	0	0	1	
	0	1	1	1	0	1	
	1	0	0	0	1	0	
	1	0	0	1	1	0	
	1	0	1	0	1	0	
	1	0	1	1	1	0	
	1	1	0	0	0	0	
	1	1	0	1	0	1	
	1	1	1	0	1	0	
	1	1	1	1	0	0	

NOTE 1: The 0 state indicates that a secondary communication is not being requested. The 1 state indicates that a secondary communication is being requested.

2.18 Primary Serial Communications

Primary serial communications transfer the 14-bit DAC input plus two control bits (D01 and D00) to DIN of the TLC320AC01.They simultaneously transfer the 14-bit ADC conversion result from DOUT to the processor. The two LSBs are set to 0 in the ADC result.

2.18.1 Primary Serial Communications Data Format

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

14-bit DAC Conversion Result (D15–D02)
2s-Complement Format†

Control Bits (D01–D00)

† Since the supply voltage is single ended, the reference for 2s-complement format is ADC V_{MID}. Voltages above this reference have a 0 as the MSB, and voltages below this reference have a 1 as the MSB.

During primary serial communications, when D01 and D00 are both high in the DAC data word to DIN, a subsequent 16 bits of control information is received by the device at DIN during a secondary serial-communication interval. This secondary serial-communication interval begins at 1/2 the programmed conversion time when the B register data value is even or 1/2 the programmed value minus one FCLK when the B register data value is odd. The time between primary and secondary serial communication is measured from the falling edge of the primary frame sync to the falling edge of the secondary frame sync (see Section 2.19, Secondary Serial Communications for function and format of control words).

2.18.2 Data Format From DOUT During Primary Serial Communications

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

14-Bit ADC Conversion Result (D15–D02)
2s-Complement Format
D15 is the Sign Bit

Master Mode { D01 = 0, D00 = 0

Slave Mode { D01 = 0, D00 = 1

2.19 Secondary Serial Communications

2.19.1 Data Format to DIN During Secondary Serial Communications

There are nine 16-bit configuration and control registers numbered from zero to eight. All register data contents are represented in 2s-complement format. The general format of the commands during secondary serial communications is as follows.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits (2 bits)		R/$\overline{W}$ Bit	Register Address (5 bits)					Register Data Value (8 bits)							

All control register words are latched in the register and valid on the sixteenth falling edge of SCLK.

2.19.2 Control Data-Bit Function in Secondary Serial Communication

2.19.2.1 DS15 and DS14

In the secondary data word, bits DS15 and DS14 perform the same control function as the primary control bits D01 and D00 do in the primary data word.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	Register Address					Register Data							

Hardware terminals FC1 and FC0 are valid inputs when DS15 and DS14 are both high, and they are ignored for all other conditions.

2.19.2.2 DS13 (R/$\overline{W}$ Bit)

Reset and power-up procedures set this bit to a 0, placing the device in the write mode. When this bit is set to 1, however, the previous data content of the register being addressed is read out to the host from DOUT as the least significant eight bits of the 16-bit secondary word. The first eight bits remain set to 0. Reading the data out is nondestructive, and the contents of the register remain unchanged.

A. Write Mode (DS13 = 0)

Data In. The data word to DIN has the following general format in the write mode.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		0	Register Address					Register Data							

Data Out. The shift clock shifts out all 0s as the pattern to the host from DOUT.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

B. Read Mode (DS13 = 1)

Data In. The data word to DIN has the following format to allow a register read. Phase shifts can also be done in the read mode.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		1	Register Address					Ignored							

Data Out. The shift clock clocks out the data of the register addressed from DOUT in the read mode in the eight LSBs.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0	Register Data							

2.20 Internal Register Format

2.20.1 Pseudo-Register 0 (No-Op Address)

This address represents a no-operation command. No register I/O operation takes place, so the device can receive secondary commands for phase adjustment without reprogramming any register. A read of the no-op is 0. The format of the command word is as follows.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		X	0	0	0	0	0	X	X	X	X	X	X	X	X

2.20.2 Register 1 (A Register)

The following command loads DS07 (MSB) – DS00 into the A register.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	0	0	0	0	1	Register Data							

The data in DS07 – DS00 determines the division of the master clock to produce the internal FCLK.

FCLK frequency = MCLK/(A register contents × 2)

The default value of the A-register data is decimal 18 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	0	1	0

2.20.3 Register 2 (B Register)

The following command loads DS07 (MSB) – DS00 into the B register.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	0	0	0	1	0	Register Data							

The data in DS07 – DS00 controls the division of FCLK to generate the conversion clock.

$$\text{Conversion frequency} = \text{FCLK}/(\text{B register contents})$$

$$= \frac{\text{MCLK}}{2 \times \text{A register contents} \times \text{B register contents}}$$

The default value of the B-register data is decimal 18 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	0	1	0

2.20.4 Register 3 (A′ Register)

The following command contains the A′-register address and loads DS07(MSB) – DS00 into the A′ register.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	0	0	0	1	1	Register Data							

The data in DS07 – DS00 is in 2s-complement format and controls the number of master-clock periods that the sampling time is shifted.

The default value of the A′-register data is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

2.20.5 Register 4 (Amplifier Gain-Select Register)

The following command contains the amplifier gain-select register address with selection code for the monitor output (DS05–DS04), analog input (DS03–DS02), and analog output (DS01–DS00) programmable gains.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/W̄	0	0	1	0	0	X	X	*	*	*	*	*	*
Monitor output gain = squelch →										0	0				
Monitor output gain = 0 dB →										0	1				
Monitor output gain = −8 dB →										1	0				
Monitor output gain = −18 dB →										1	1				
Analog input gain = squelch →												0	0		
Analog input gain = 0 dB →												0	1		
Analog input gain = 6 dB →												1	0		
Analog input gain = 12 dB →												1	1		
Analog output gain = squelch →														0	0
Analog output gain = 0 dB →														0	1
Analog output gain = −6 dB →														1	0
Analog output gain = −12 dB →														1	1

The default value of the monitor output gain is squelch, which corresponds to data bits DS05 and DS04 equal to 00 (binary).
The default value of the analog input gain is 0 dB, which corresponds to data bits DS03 and DS02 equal to 01 (binary).
The default value of the analog output gain is 0 dB, which corresponds to data bits DS01 and DS00 equal to 01 (binary).

The default data value is shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	1	0	1

2.20.6 Register 5 (Analog Configuration Register)

The following command loads the analog configuration register with the individual bit functions described below.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/W̄	0	0	1	0	1	X	X	X	X	*	*	*	*
Must be set to 0 →												0			
High-pass filter disabled →													1		
High-pass filter enabled →													0		
Analog loopback enabled →														0	0
Enables IN+ and IN− (disables AUXIN+ and AUXIN−) →														0	1
Enables AUXIN+ and AUXIN− (disables IN+ and IN−) →														1	0
Enable analog input summing →														1	1

The default value of the high-pass-filter enable bit is 0, which places the high-pass filter in the signal path. The default values of DS01 and DS00 are 0 and 1 which enables IN+ and IN−.

The power-up and reset conditions are as shown below.

DS03	DS02	DS01	DS00
0	0	0	1

In the read mode, eight bits are read but the four LSBs are repeated as the four MSBs.

2.20.7 Register 6 (Digital Configuration Register)

The following command loads the digital configuration register with the individual bit functions described below.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		$R/\overline{W}$	0	0	1	1	0	X	X	*	*	*	*	*	*
ADC and DAC conversion free run Inactive										1 0					
$\overline{FSD}$ output disable Enable											1 0				
16-Bit mode, ignore primary LSBs Normal operation												1 0			
Force secondary communications Normal operation													1 0		
Software reset (upon reset, this bit is automatically reset to 0) Inactive reset														1 0	
Software power-down active (automatically reset to 0 after $\overline{PWR}$ $\overline{DWN}$ is cycled high to low and back to high) Power-down function external (uses $\overline{PWR}$ $\overline{DWN}$)															1 0

The default value of DS07–DS00 is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

2.20.8 Register 7 (Frame-Sync Delay Register)

The following command contains the frame-sync delay (FSD) register address and loads DS07 (MSB)–DS00 into the FSD register. The data byte (DS01–DS00) determines the number of SCLKs between $\overline{FS}$ and the delayed frame-sync signal, $\overline{FSD}$. The minimum data value for this register is decimal 18.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		$R/\overline{W}$	0	0	1	1	1	Register Data							

The default value of DS07 – DS00 is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

When using a slave device, register 7 must be the last register programmed.

2.20.9 Register 8 (Frame-Sync Number Register)

The following command contains the frame-sync number (FSN) register address and loads DS07 (MSB) – DS00 into the FSN register. The data byte determines the number of frame-sync signals generated by the TLC320AC01. This number is equal to the number of slaves plus one.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		$R/\overline{W}$	0	1	0	0	0	Register Data							

The default value of DS07 – DS00 is 1 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	1

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, DGTL V_{DD} (see Notes 1 and 2) .... −0.3 V to 6.5 V
Supply voltage range, DAC V_{DD} (see Notes 1 and 2) .... −0.3 V to 6.5 V
Supply voltage range, ADC V_{DD} (see Notes 1 and 2) .... −0.3 V to 6.5 V
Differential supply voltage range, DGTL V_{DD} to DAC V_{DD} .... −0.3 V to 6.5 V
Differential supply voltage range, all positive supply voltages to
ADC GND, DAC GND, DGTL GND, SUBS .... −0.3 V to 6.5 V
Output voltage range, DOUT .... −0.3 V to DGTL V_{DD} + 0.3 V
Input voltage range, DIN .... −0.3 V to DGTL V_{DD} + 0.3 V
Ground voltage range, ADC GND, DAC GND,
DGTL GND, SUBS .... −0.3 V to DGTL V_{DD} + 0.3 V
Operating free-air temperature range, T_A .... 0°C to 70°C
Storage temperature range, T_{stg} .... −40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{DD}	Positive supply voltage	4.5	5	5.5	V
	Steady-state differential voltage between any two supplies			0.1	V
V_{IH}	High-level digital input voltage	2.2			V
V_{IL}	Low-level digital input voltage			0.8	V
I_O	Load output current from ADC V_{MID} and DAC			100	µA
	Conversion time for the ADC and DAC channels	10 FCLK periods			
f_{MCLK}	Master-clock frequency		10.368	15	MHz
$V_{ID(PP)}$	Analog input voltage (differential, peak to peak)		6		V
R_L	Differential output load resistance	600			Ω
R_L	Single-ended to buffered DAC V_{MID} voltage load resistance	300			Ω
T_A	Operating free-air temperature	0		70	°C

NOTES: 1. Voltage values for DGTL V_{DD} are with respect to DGTL GND, voltage values for DAC V_{DD} are with respect to DAC GND, and voltage values for ADC V_{DD} are with respect to ADC GND. For the subsequent electrical, operating, and timing specifications, the symbol V_{DD} denotes all positive supplies. DAC GND, ADC GND, DGTL GND, and SUBS are at 0 V unless otherwise specified.

2. To avoid possible damage to these CMOS devices and associated operating parameters, the sequence below should be followed when applying power:
   (1) Connect SUBS, DGTL GND, ADC GND, and DAC GND to ground.
   (2) Connect voltages ADC V_{DD},and DAC V_{DD}.
   (3) Connect voltage DGTL V_{DD}.
   (4) Connect the input signals.

   When removing power, follow the steps above in reverse order.

3.3 Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, MCLK = 5.184 MHz, V_{DD} = 5 V, Outputs Unloaded, Total Device

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{DD}	Supply current	$\overline{PWR}$ $\overline{DWN}$ = 1 and clock signals present		20	25	mA
		$\overline{PWR}$ $\overline{DWN}$ = 0 after 500 μs and clock signals present		1	2	mA
P_D	Power dissipation	$\overline{PWR}$ $\overline{DWN}$ = 1 and clock signals present		100		mW
		$\overline{PWR}$ $\overline{DWN}$ = 0 after 500 μs and clock signals present		5		mW
		Software power down, (bit D00, register 6 set to 1)		15	20	mW
ADC V_{MID}	Midpoint voltage	No load	ADC $V_{DD}/2$ −0.1		ADC $V_{DD}/2$ +0.1	V
DAC V_{MID}	Midpoint voltage	No load	DAC $V_{DD}/2$ −0.1		DAC $V_{DD}/2$ +0.1	V

3.4 Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, V_{DD} = 5 V, Digital I/O Terminals (DIN, DOUT, EOC, FC0, FC1, $\overline{FS}$, $\overline{FSD}$, MCLK, M/$\overline{S}$, SCLK)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −1.6 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
I_{IH}	High-level input current, any digital input	V_I = 2.2 V to DGTL V_{DD}			10	μA
I_{IL}	Low-level input current, any digital input	V_I = 0 V to 0.8 V			10	μA
C_i	Input capacitance			5		pF
C_o	Output capacitance			5		pF

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

3.5 Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, V_{DD} = 5 V, ADC and DAC Channels

3.5.1 ADC Channel Filter Transfer Function, FCLK = 144 kHz, f_s = 8 kHz

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Gain relative to gain at f_i = 1020 Hz (see Note 3)	f_i = 50 Hz		−2	dB
	f_i = 200 Hz	−1.8	−0.15	
	f_i = 300 Hz to 3 kHz	−0.15	0.15	
	f_i = 3.3 kHz	−0.35	0.03	
	f_i = 3.4 kHz	−1	−0.1	
	f_i = 4 kHz		−14	
	$f_i \geq$ 4.6 kHz		−32	

NOTE 3: The differential analog input signals are sine waves at 6 V peak to peak. The reference gain is at 1020 Hz.

3.5.2 ADC Channel Input, V_{DD} = 5 V, Input Amplifier Gain = 0 dB (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{I(PP)}$	Peak-to-peak input voltage (see Note 4)	Single-ended		3		V
		Differential		6		V
	ADC converter offset error	Band-pass filter selected		10	30	mV
CMRR	Common-mode rejection ratio at IN+, IN–, AUX IN+, AUX IN– (see Note 5)			55		dB
r_i	Input resistance at IN+, IN–, AUX IN+, AUX IN–			100		kΩ
	Squelch	DS03, DS02 = 0 in register 4		60		dB

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTES: 4. The differential range corresponds to the full-scale digital output.

5. Common-mode rejection ratio is the ratio of the ADC converter offset error with no signal and the ADC converter offset error with a common-mode nonzero signal applied to either IN+ and IN– together or AUX IN+ and AUX IN– together.

3.5.3 ADC Channel Signal-to-Distortion Ratio, V_{DD} = 5 V, f_s = 8 kHz (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	A_V = 0 dB		A_V = 6 dB		A_V = 12 dB		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
ADC channel signal-to-distortion ratio (see Note 6)	V_I = –6 dB to –1 dB	68		—		—		dB
	V_I = –12 dB to –6 dB	63		68		—		
	V_I = –18 dB to –12 dB	56		63		68		
	V_I = –24 dB to –18 dB	51		57		63		
	V_I = –30 dB to –24 dB	43		51		57		
	V_I = –36 dB to –30 dB	39		45		51		
	V_I = –42 dB to –36 dB	33		39		45		
	V_I = –48 dB to –42 dB	27		32		39		

NOTE 6: The analog-input test signal is a 1020-Hz sine wave with 0 dB = 6 V peak to peak as the reference level for the analog-input signal.

3.5.4 DAC Channel Filter Transfer Function, FCLK = 144 kHz, f_s = 9.6 kHz, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Gain relative to gain at f_i = 1020 Hz (see Note 7)	f_i < 200 Hz		0.15	dB
	f_i = 200 Hz	–0.5	0.15	
	f_i = 300 Hz to 3 kHz	–0.15	0.15	
	f_i = 3.3 kHz	–0.35	0.03	
	f_i = 3.4 kHz	–1	–0.1	
	f_i = 4 kHz		–14	
	f_i ≥ 4.6 kHz		–32	

NOTE 7: The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak.

3.5.5 DAC Channel Signal-to-Distortion Ratio, V_{DD} = 5 V, f_s = 8 kHz (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	A_V = 0 dB		A_V = −6 dB		A_V = −12 dB		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
DAC channel signal-to-distortion ratio (see Note 8)	V_O = −6 dB to 0 dB	68		—		—		dB
	V_O = −12 dB to −6 dB	63		68		—		
	V_O = −18 dB to −12 dB	57		63		68		
	V_O = −24 dB to −18 dB	51		57		63		
	V_O = −30 dB to −24 dB	45		51		57		
	V_O = −36 dB to −30 dB	39		45		51		
	V_O = −42 dB to −36 dB	33		39		48		
	V_O = −48 dB to −42 dB	27		33		39		

NOTE 8: The input signal, V_I, is the digital equivalent of a 1020-Hz sine wave (full-scale analog output at full-scale digital input = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT−.

3.5.6 System Distortion, V_{DD} = 5 V, f_s = 8 kHz, FCLK = 144 kHz (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
ADC channel attenuation	Second harmonic	Single-ended input (see Note 9)		82		dB
		Differential input (see Note 9)	70	82		
	Third harmonic and higher harmonics	Single-ended input (see Note 9)		77		
		Differential input (see Note 9)	70	77		
DAC channel attenuation	Second harmonic	Single-ended output (buffered DAC V_{MID}) (see Note 10)		82		
		Differential output (see Note 10)	70	82		
	Third harmonic and higher harmonics	Single-ended output (see Note 10)		77		
		Differential output (see Note 10)	70	77		

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTES: 9. The input signal is a 1020-Hz sine wave for the ADC channel. Harmonic distortion is defined for an input level of −1 dB.

10. The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT−. Harmonic distortion is specified for a signal input level of 0 dB.

3.5.7 Noise, Low-Pass and Band-Pass Switched-Capacitor Filters Included, V_{DD} = 5 V (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
ADC idle-channel noise		Inputs tied to ADC V_{MID}, f_s = 8 kHz, FCLK = 144 kHz, (see Note 11)		180	300	μVrms
DAC idle-channel noise	Broad-band noise	DIN INPUT = 00000000000000, f_s = 8 kHz, FCLK = 144 kHz, (see Note 12)		180	300	μVrms
	Noise (0 to 7.2 kHz)			180	300	μVrms
	Noise (0 to 3.6 kHz)			180	300	μVrms

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTES: 11. The ADC channel noise is calculated by taking the RMS value of the digital output codes of the ADC channel and converting to microvolts.

12. The DAC channel noise is measured differentially from OUT+ to OUT− across 600 Ω.

3.5.8 Absolute Gain Error, V_{DD} = 5 V, f_s = 8 kHz (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
ADC channel absolute gain error (see Note 13)	−1-dB input signal	T_A = 25°C		±0.5	dB
		T_A = 0 − 70°C		±1	dB
DAC channel absolute gain error (see Note 14)	0-dB input signal, R_L = 600 Ω	T_A = 25°C		±0.5	dB
		T_A = 0 − 70°C		±1	dB

NOTES: 13. ADC absolute gain error is the variation in gain from the ideal gain over the specified input signal levels. The gain is measured with a −1-dB, 1020-Hz sine wave. The −1-dB input signal allows for any positive gain or offset error that may affect gain measurements at or close to 0-dB input signal levels.

14. The DAC input signal is the digital equivalent of a 1020-Hz sine wave (full-scale analog output at digital full-scale input = 0 dB). The nominal differential DAC channel output voltage with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT−.

3.5.9 Relative Gain and Dynamic Range, V_{DD} = 5 V, f_s = 8 kHz (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
ADC channel relative gain tracking error (see Note 15)	−48-dB to −1-dB input signal range		±0.15	dB
DAC channel relative gain tracking error (see Note 16)	−48-dB to 0-dB input signal range $R_{L(diff)}$ = 600 Ω		±0.15	dB

NOTES: 15. ADC gain tracking is the ratio of the measured gain at one ADC channel input level to the gain measured at any other input level. The ADC channel input is a −1-dB 1020-Hz sine wave input signal. A −1-dB input signal allows for any positive gain or offset error that may affect gain measurements at or close to 0-dB ADC input signal levels.

16. DAC gain tracking is the ratio of the measured gain at one DAC channel digital input level to the gain measured at any other input level. The DAC-channel input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output voltage with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT−.

3.5.10 Power-Supply Rejection, V_{DD} = 5 V (Unless Otherwise Noted) (see Note 17)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
ADC V_{DD}	Supply-voltage rejection ratio, ADC channel	f_i = 0 to 30 kHz		50		dB
		f_i = 30 to 50 kHz		55		
DAC V_{DD}	Supply-voltage rejection ratio, DAC channel	f_i = 0 to 30 kHz		40		
		f_i = 30 to 50 kHz		45		
DGTL V_{DD}	Supply-voltage rejection ratio, ADC channel	f_i = 0 to 30 kHz		50		
		f_i = 30 to 50 kHz		55		
DGTL V_{DD}	Supply-voltage rejection ratio, DAC channel	Single ended, f_i = 0 to 30 kHz		40		
		f_i = 30 to 50 kHz		45		
		Differential, f_i = 0 to 30 kHz		40		
		f_i = 30 to 50 kHz		45		

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTE 17: Power supply rejection measurements are made with both the ADC and the DAC channels idle and a 200-mV peak-to-peak signal applied to the appropriate supply.

3.5.11 Crosstalk Attenuation, V_{DD} = 5 V (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
ADC channel crosstalk attenuation	DAC channel idle with DIN = 00000000000000, ADC input = 0 dB, 1020-Hz sine wave, Gain = 0 dB (see Note 18)		80		dB
DAC channel crosstalk attenuation	ADC channel idle with INP, INM, AUX IN+, and AUX IN– at ADC V_{MID}		80		dB
	DAC channel input = digital equivalent of a 1020-Hz sine wave (see Note 19)		80		

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTES: 18. The test signal is a 1020-Hz sine wave with a 0 dB = 6-V peak-to-peak reference level for the analog input signal.

19. The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT–.

3.5.12 Monitor Output Characteristics, V_{DD} = 5 V (Unless Otherwise Noted) (see Note 20)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{O(PP)}$	Peak-to-peak ac output voltage	Quiescent level = ADC V_{MID} Z_L = 10 kΩ and 60 pF	1.3	1.5		V
V_{OO}	Output offset voltage	No load, single ended relative to ADC V_{MID}		5	10	mV
V_{OC}	Output common-mode voltage	No load	0.4 ADC V_{DD}	0.5 ADC V_{DD}	0.6 ADC V_{DD}	V
r_o	DC output resistance			50		Ω
A_V	Voltage gain (see Note 21)	Gain = 0 dB	−0.2	0	0.2	dB
		Gain 2 = −8 dB	−8.2	−8	−7.8	
		Gain 3 = −18 dB	−18.4	−18	−17.6	
		Squelch (see Note 22)			−60	

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTES: 20. All monitor output tests are performed with a 10-kΩ load resistance.

21. Monitor gains are measured with a 1020-Hz, 6-V peak-to-peak sine wave applied differentially between IN+ and IN−. The monitor output gains are nominally 0 dB, −8 dB, and −18 dB relative to its input; however, the output gains are −6 dB relative to IN+ and IN− or AUX IN+ and AUX IN−.
22. Squelch is measured differentially with respect to ADC V_{MID}.

3.6 Timing Requirements and Specifications in Master Mode

3.6.1 Recommended Input Timing Requirements for Master Mode, V_{DD} = 5 V

		MIN	NOM	MAX	UNIT
$t_{r(MCLK)}$	Master clock rise time		5		ns
$t_{f(MCLK)}$	Master clock fall time		5		ns
	Master clock duty cycle	40%		60%	
$t_{w(RESET)}$	$\overline{\text{RESET}}$ pulse duration	1 MCLK			
$t_{su(DIN)}$	DIN setup time before SCLK low (see Figure 4–2)	25			ns
$t_{h(DIN)}$	DIN hold time after SCLK low (see Figure 4–2)			20	ns

3.6.2 Operating Characteristics Over Recommended Range of Operating Free-Air Temperature, V_{DD} = 5 V (Unless Otherwise Noted) (see Note 23)

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{f(SCLK)}$	Shift clock fall time (see Figure 4–2)		13	18	ns
$t_{r(SCLK)}$	Shift clock rise time (see Figure 4–2)		13	18	ns
	Shift clock duty cycle	45%		55%	
$t_{d(CH\text{-}FL)}$	Delay time from SCLK high to $\overline{\text{FSD}}$ low (see Figures 4–2 and 4–4 and Note 24)		5	20	ns
$t_{d(CH\text{-}FH)}$	Delay time from SCLK high to $\overline{\text{FS}}$ high (see Figure 4–2)		5	20	ns
$t_{d(CH\text{-}DOUT)}$	Delay time from SCLK high to DOUT valid (see Figures 4–2 and 4–7)			20	ns
$t_{d(CH\text{-}DOUTZ)}$	Delay time from SCLK↑ to DOUT in high-impedance state (see Figure 4–8)		20		ns
$t_{d(ML\text{-}EL)}$	Delay time from MCLK low to EOC low (see Figure 4–9)		40		ns
$t_{d(ML\text{-}EH)}$	Delay time from MCLK low to EOC high (see Figure 4–9)		40		ns
$t_{f(EL)}$	EOC fall time (see Figure 4–9)		13		ns
$t_{r(EH)}$	EOC rise time (see Figure 4–9)		13		ns
$t_{d(MH\text{-}CH)}$	Delay time from MCLK high to SCLK high			50	ns
$t_{d(MH\text{-}CL)}$	Delay time from MCLK high to SCLK low			50	ns

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTES: 23. All timing specifications are valid with C_L = 20 pF.

24. $\overline{\text{FSD}}$ occurs 1/2 shift-clock cycle ahead of $\overline{\text{FS}}$ when the device is operating in the master mode.

3.7 Timing Requirements and Specifications in Slave Mode and Codec Emulation Mode

3.7.1 Recommended Input Timing Requirements for Slave Mode, V_{DD} = 5 V

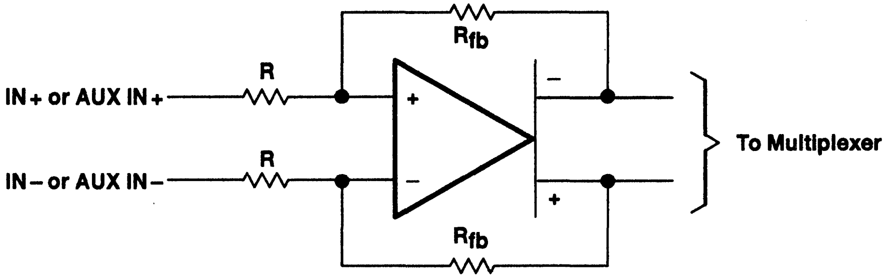
		MIN	NOM	MAX	UNIT
$t_{r(MCLK)}$	Master clock rise time		5		ns
$t_{f(MCLK)}$	Master clock fall time		5		ns
	Master clock duty cycle	40%		60%	
$t_{w(RESET)}$	$\overline{\text{RESET}}$ pulse duration	1 MCLK			
$t_{su(DIN)}$	DIN setup time before SCLK low (see Figure 4–3)	20			ns
$t_{h(DIN)}$	DIN hold time after SCLK high (see Figure 4–3)			20	ns
$t_{su(FL-CH)}$	Setup time from $\overline{\text{FS}}$ low to SCLK high			±SCLK/4	ns

3.7.2 Operating Characteristics Over Recommended Range of Operating Free-Air Temperature, V_{DD} = 5 V (Unless Otherwise Noted) (see Note 23)

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock cycle time (see Figure 4–3)	125			ns
$t_{f(SCLK)}$	Shift clock fall time (see Figure 4–3)			18	ns
$t_{r(SCLK)}$	Shift clock rise time (see Figure 4–3)			18	ns
	Shift clock duty cycle	45%		55%	
$t_{d(CH-FDL)}$	Delay time from SCLK high to $\overline{\text{FSD}}$ low (see Figure 4–6)			50	ns
$t_{d(CH-FDH)}$	Delay time from SCLK high to $\overline{\text{FSD}}$ high			40	ns
$t_{d(FL-FDL)}$	Delay time from $\overline{\text{FS}}$ low to $\overline{\text{FSD}}$ low (slave to slave) (see Figure 4–5)			40	ns
$t_{d(CH-DOUT)}$	Delay time from SCLK high to DOUT valid (see Figures 4–3 and 4–7)			40	ns
$t_{d(CH-DOUTZ)}$	Delay time from SCLK↑ to DOUT in high-impedance state (see Figure 4–8)		20		ns
$t_{d(ML-EL)}$	Delay time from MCLK low to EOC low (see Figure 4–9)		40		ns
$t_{d(ML-EH)}$	Delay time from MCLK low to EOC high (see Figure 4–9)		40		ns
$t_{f(EL)}$	EOC fall time (see Figure 4–9)		13		ns
$t_{r(EH)}$	EOC rise time (see Figure 4–9)		13		ns
$t_{d(MH-CH)}$	Delay time from MCLK high to SCLK high			50	ns
$t_{d(MH-CL)}$	Delay time from MCLK high to SCLK low			50	ns

† All typical values are at V_{DD} = 5 V and T_A = 25°C.
NOTE 23: All timing specifications are valid with C_L = 20 pF.

4 Parameter Measurement Information



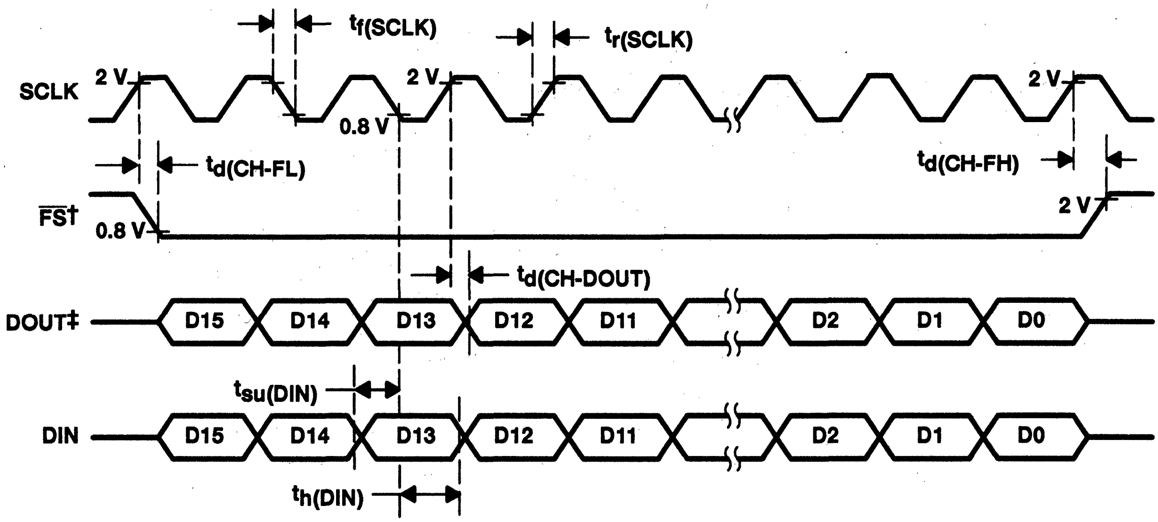
R_{fb} = R for DS03 = 0 and DS02 = 1
R_{fb} = 2R for DS03 = 1 and DS02 = 0
R_{fb} = 4R for DS03 = 1 and DS02 = 1
R = 100 kΩ nominal

Figure 4−1. IN+ and IN− Gain-Control Circuitry

Table 4−1. Gain Control (Analog Input Signal Required for Full-Scale Bipolar A/D-Conversion 2s Complement)†

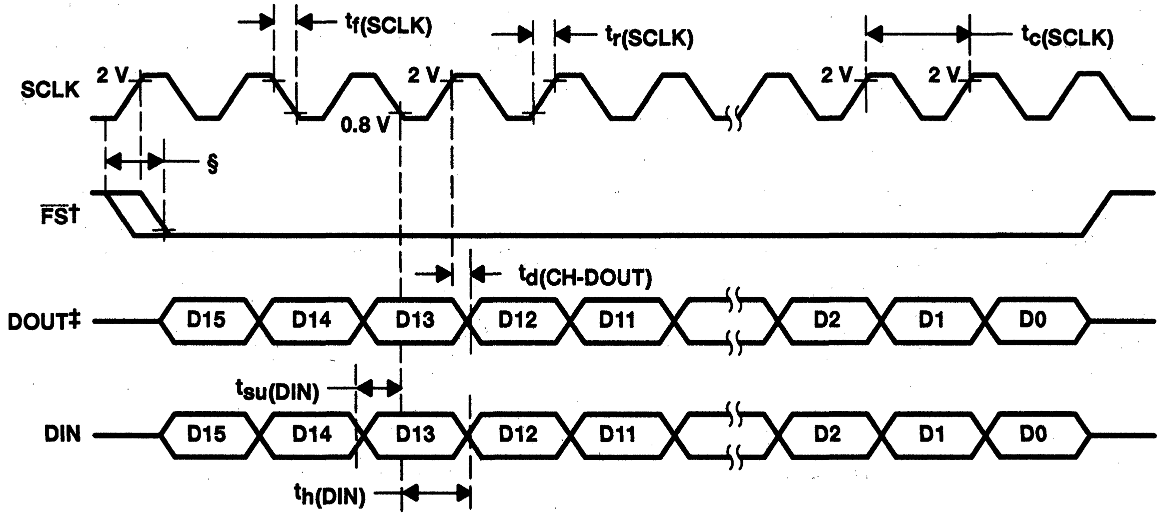
INPUT CONFIGURATION	CONTROL REGISTER 4		ANALOG INPUT‡	A/D CONVERSION RESULT
	DS03	DS02		
Differential configuration Analog input = IN+ − IN− = AUX IN+ − AUX IN−	0	0	All	Squelch
	0	1	V_{ID} = ±3 V	±Full scale
	1	0	V_{ID} = ±1.5 V	±Full scale
	1	1	V_{ID} = ±0.75 V	±Full scale
Single-ended configuration§ Analog input = IN+ − V_{MID} = AUX IN+ − V_{MID}	0	0	All	Squelch
	0	1	V_I = ±1.5 V	±Half scale
	1	0	V_I = ±1.5 V	±Full scale
	1	1	V_I = ±0.75 V	±Full scale

† V_{DD} = 5 V
‡ V_{ID} = differential input voltage, V_I = input voltage referenced to ADC V_{MID} with IN− or AUX IN− connected to ADC V_{MID}. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.
§ For single-ended inputs, the analog input voltage should not exceed the supply rails. All single-ended inputs should be referenced to the internal reference voltage, ADC V_{MID}, for best common-mode performance.



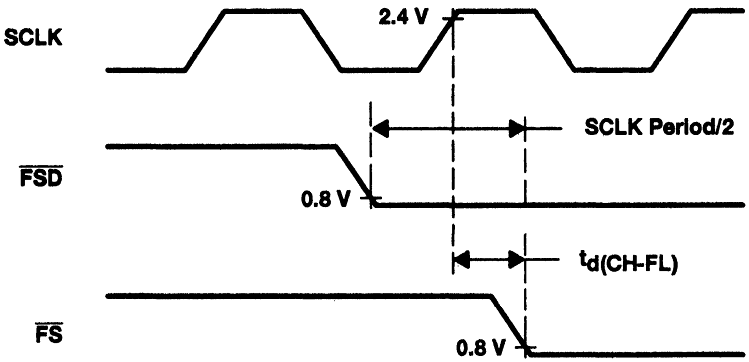
† The time between falling edges of two primary $\overline{FS}$ signals is the conversion period.
‡ The data on DOUT are shifted out on the rising edge of the shift clock, and the data on DIN are shifted in on the falling edge of the shift clock.

Figure 4–2. AIC Stand-Alone and Master-Mode Timing



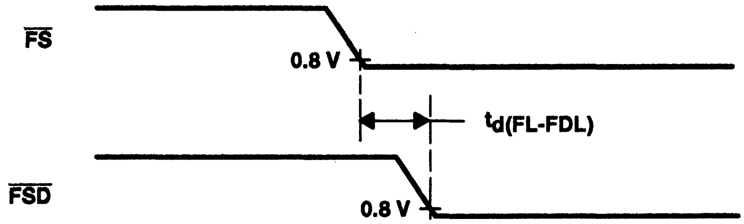
† The time between falling edges of two primary $\overline{FS}$ signals is the conversion period.
‡ The data on DOUT are shifted out on the rising edge of the shift clock, and the data on DIN are shifted in on the falling edge of the shift clock.
§ The high-to-low transition of $\overline{FS}$ must must occur within ±1/4 of a shift-clock period around the 2-V level of the shift clock.

Figure 4–3. AIC Slave and Codec Emulation Mode



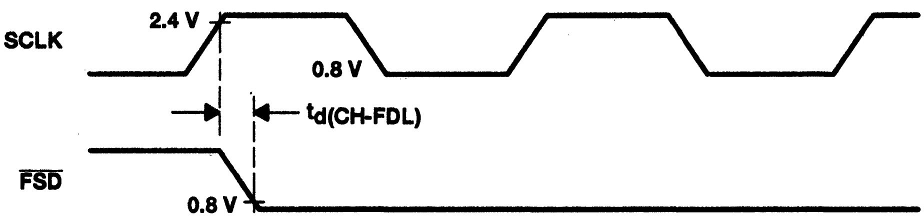
NOTE: Timing shown is for the TLC320AC01 operating as the master or as a stand-alone device.

Figure 4–4. Master or Stand-Alone $\overline{FS}$ and $\overline{FSD}$ Timing



NOTE: Timing shown is for the TLC320AC01 operating in the slave mode ($\overline{FS}$ and SCLK signals are generated externally). The programmed data value in the FSD register is 0.

Figure 4–5. Slave $\overline{FS}$ to $\overline{FSD}$ Timing



NOTE: Timing shown is for the TLC320AC01 operating in the slave mode ($\overline{FS}$ and SCLK signals are generated externally). There is a data value in the FSD register greater than 18 decimal.

Figure 4–6. Slave SCLK to $\overline{FSD}$ Timing

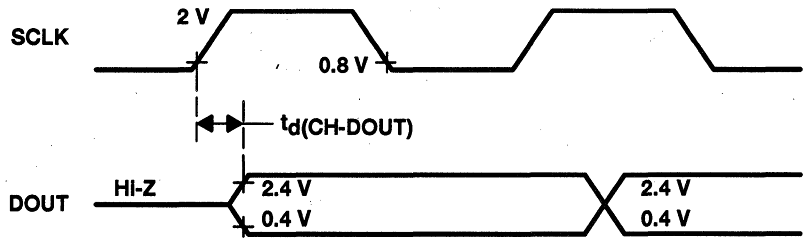


Figure 4–7. DOUT Enable Timing From Hi-Z

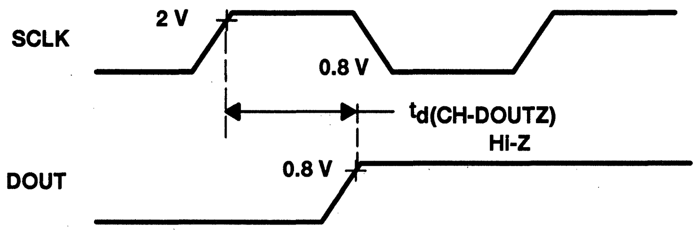


Figure 4–8. DOUT Delay Timing to Hi-Z

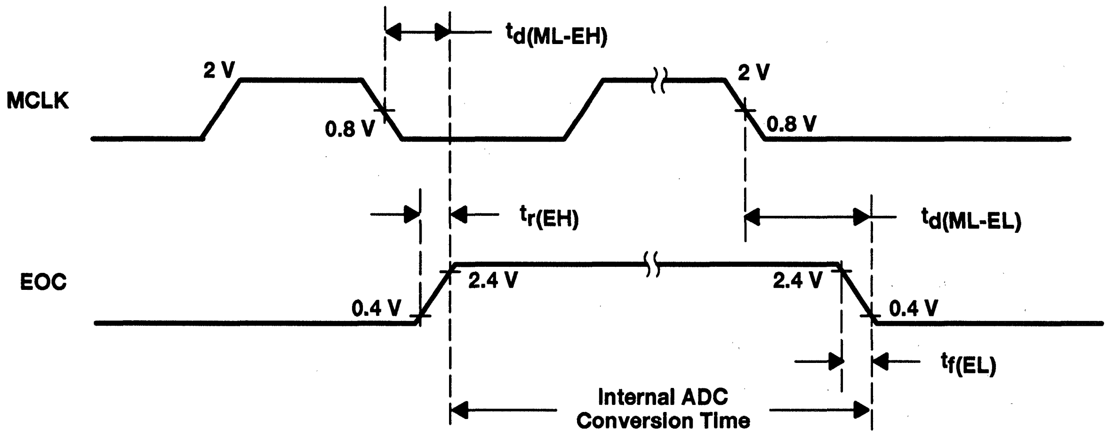
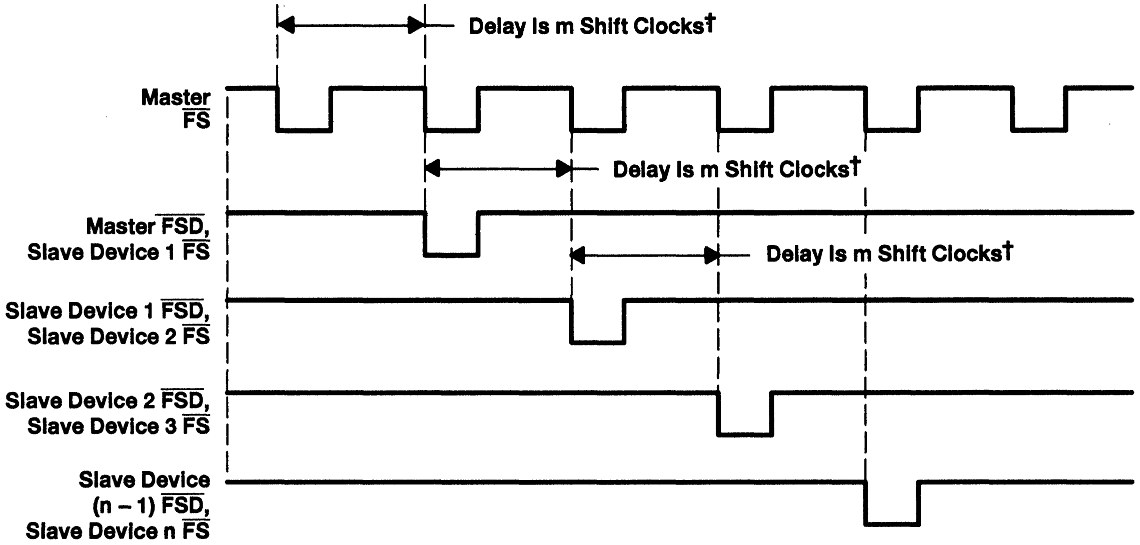
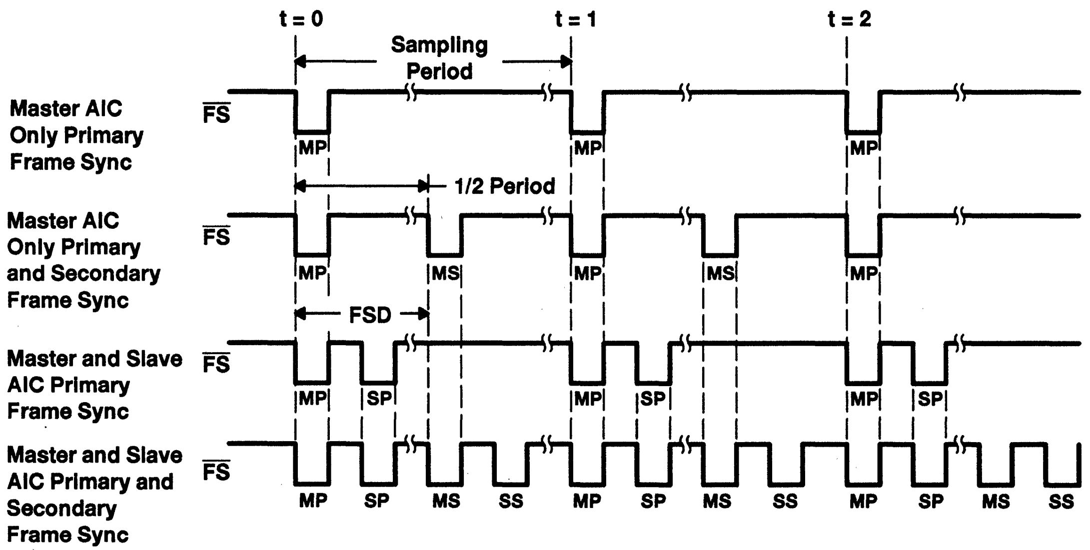


Figure 4–9. EOC Frame Timing



† The delay time from any $\overline{FS}$ signals to the corresponding $\overline{FSD}$ signals is m shift clocks with the value of m being the numerical value of the data programmed into the FSD register. In the master mode with slaves, the same data word programs the master and all slave devices; therefore, master to slave 1, slave 1 to slave 2, slave 2 to slave 3, etc., have the same delay time.

Figure 4–10. Master-Slave Frame-Sync Timing After a Delay Has Been Programmed Into the FSD Registers



MP = Master Primary
MS = Master Secondary
SP = Slave Primary
SS = Slave Secondary

Figure 4–11. Master and Slave Frame-Sync Sequence with One Slave

5 Typical Characteristics

ADC LOW-PASS RESPONSE

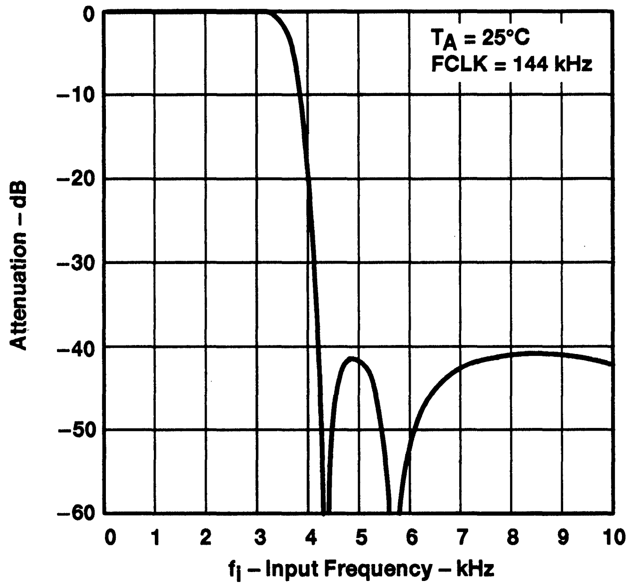


Figure 5−1

ADC LOW-PASS RESPONSE

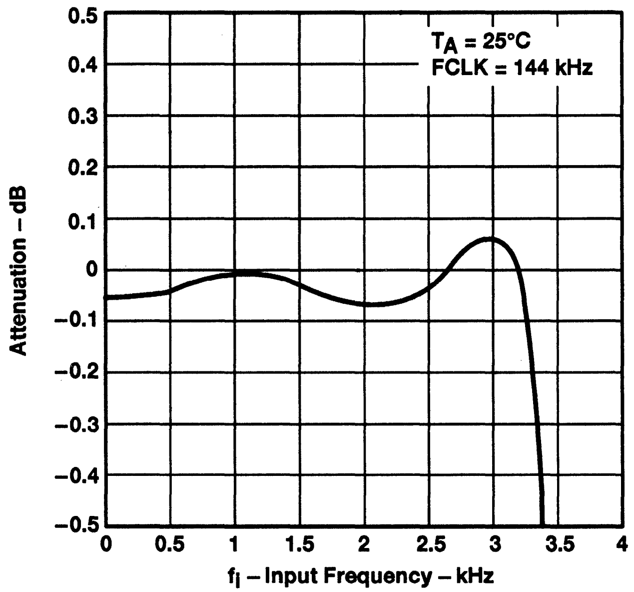


Figure 5−2

NOTE : $\text{Absolute Frequency (kHz)} = \dfrac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

ADC GROUP DELAY

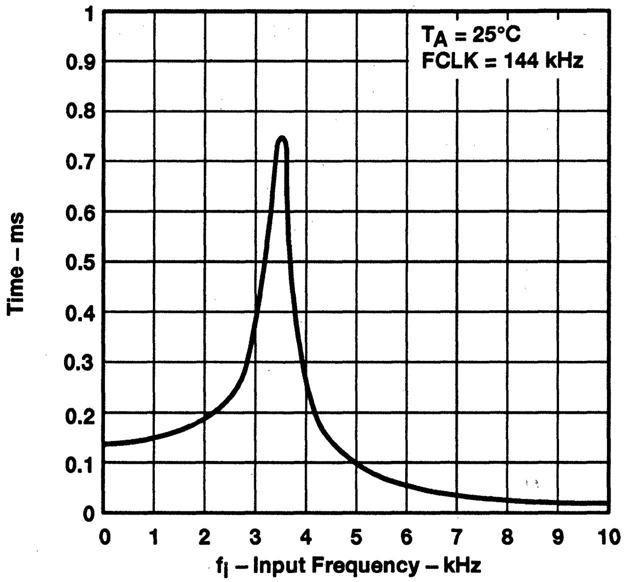


Figure 5–3

ADC BAND-PASS RESPONSE

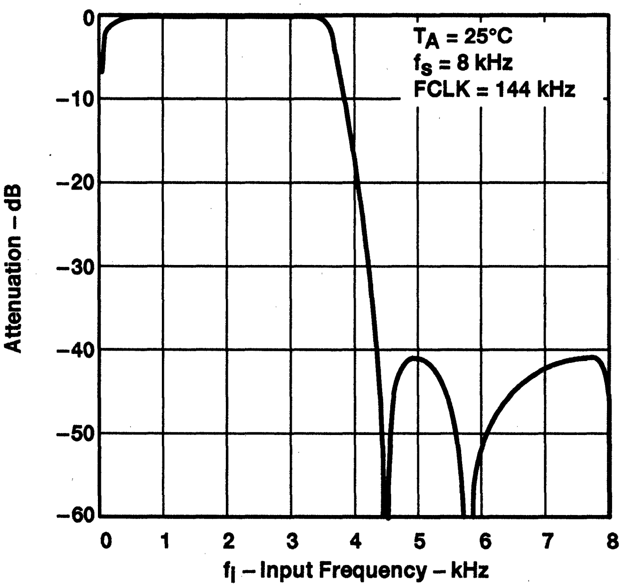


Figure 5–4

NOTE : $\text{Absolute Frequency (kHz)} = \dfrac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

ADC BAND-PASS RESPONSE

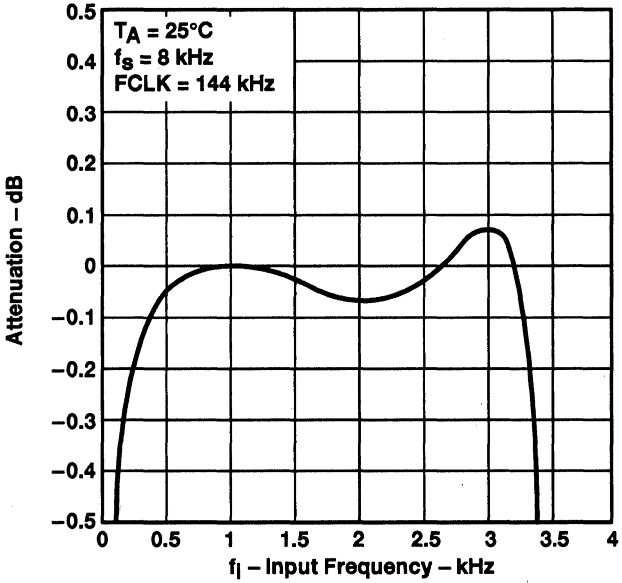


Figure 5–5

ADC HIGH-PASS RESPONSE

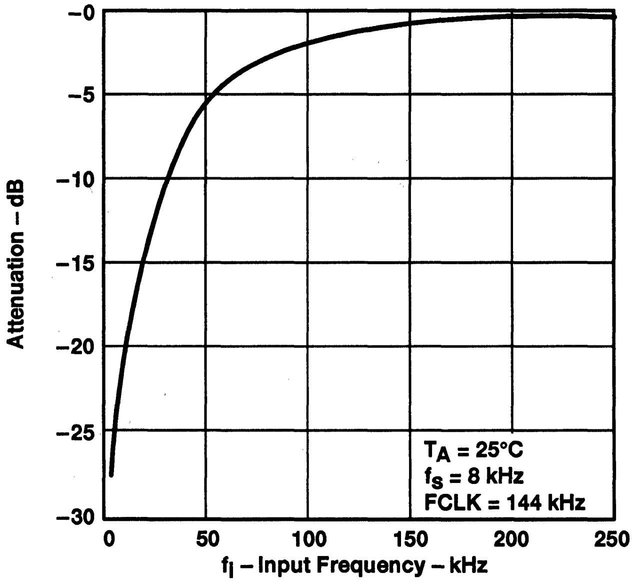


Figure 5–6

NOTE : $\text{Absolute Frequency (kHz)} = \dfrac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

ADC BAND-PASS GROUP DELAY

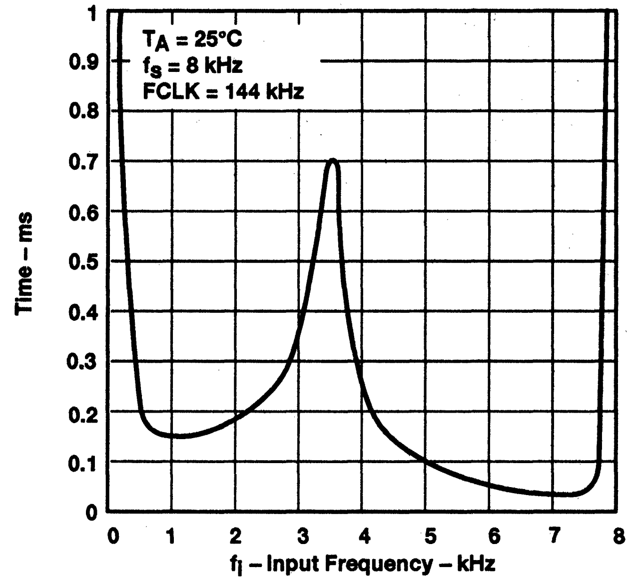


Figure 5–7

DAC LOW-PASS RESPONSE

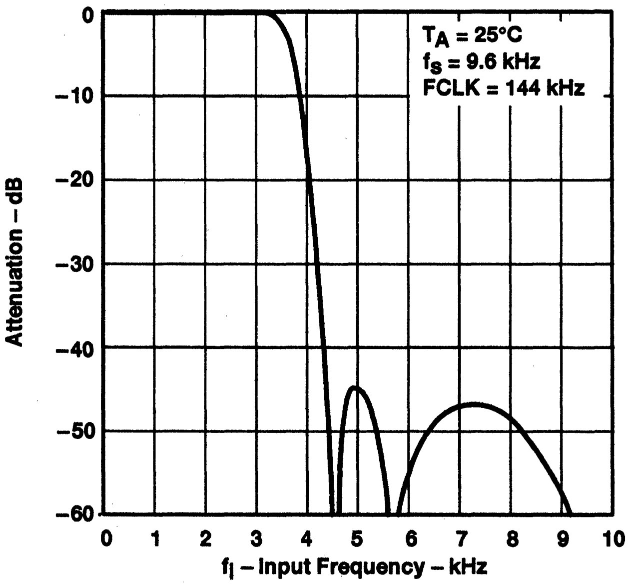


Figure 5–8

NOTE : $\text{Absolute Frequency (kHz)} = \dfrac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

DAC LOW-PASS RESPONSE

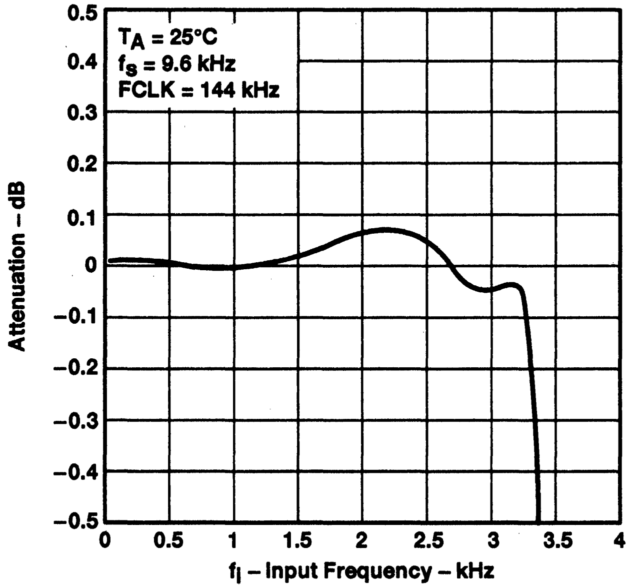


Figure 5–9

DAC LOW-PASS GROUP DELAY

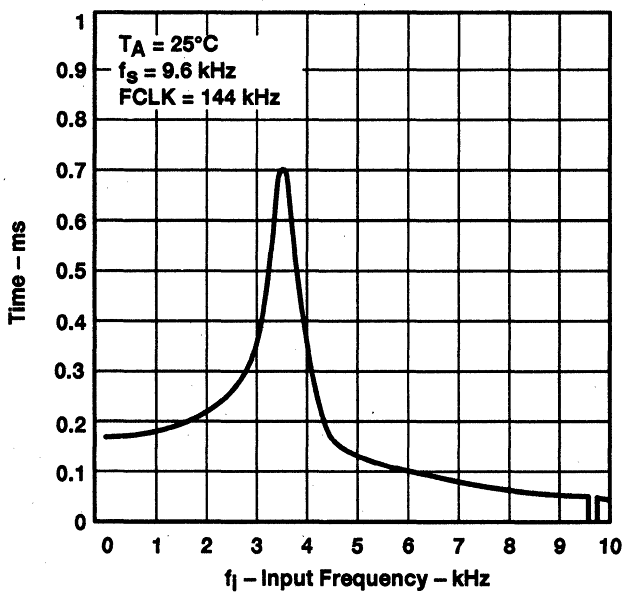


Figure 5–10

NOTE : $\text{Absolute Frequency (kHz)} = \dfrac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

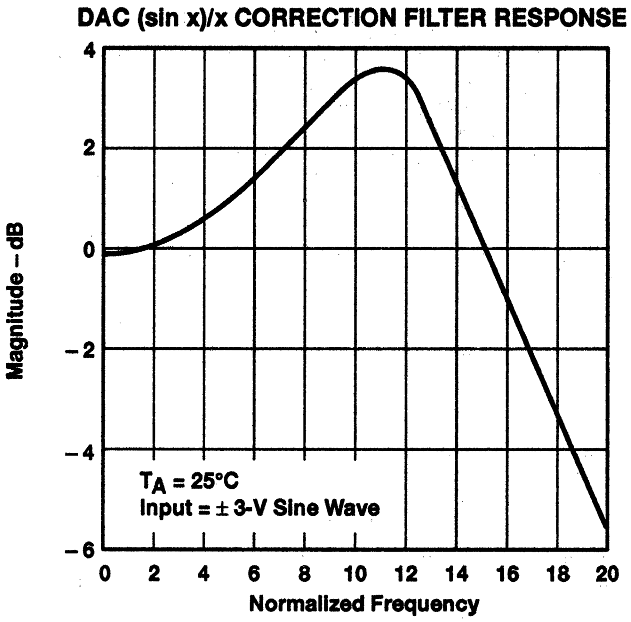


Figure 5–11

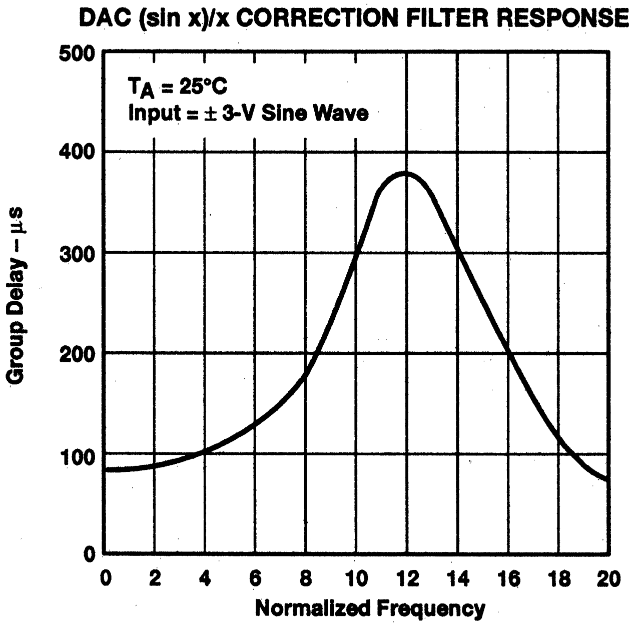


Figure 5–12

NOTE : Absolute Frequency (kHz) $= \dfrac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{288}$

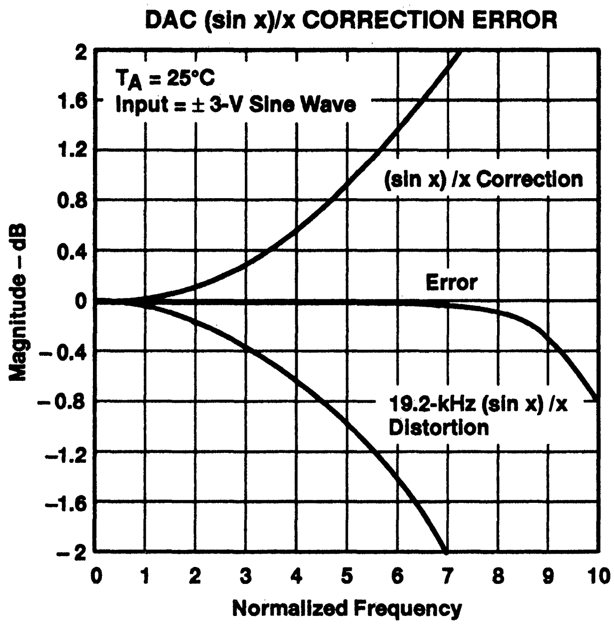


Figure 5–13

$$\text{NOTE : Absolute Frequency (kHz)} = \frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{288}$$

6 Application Information

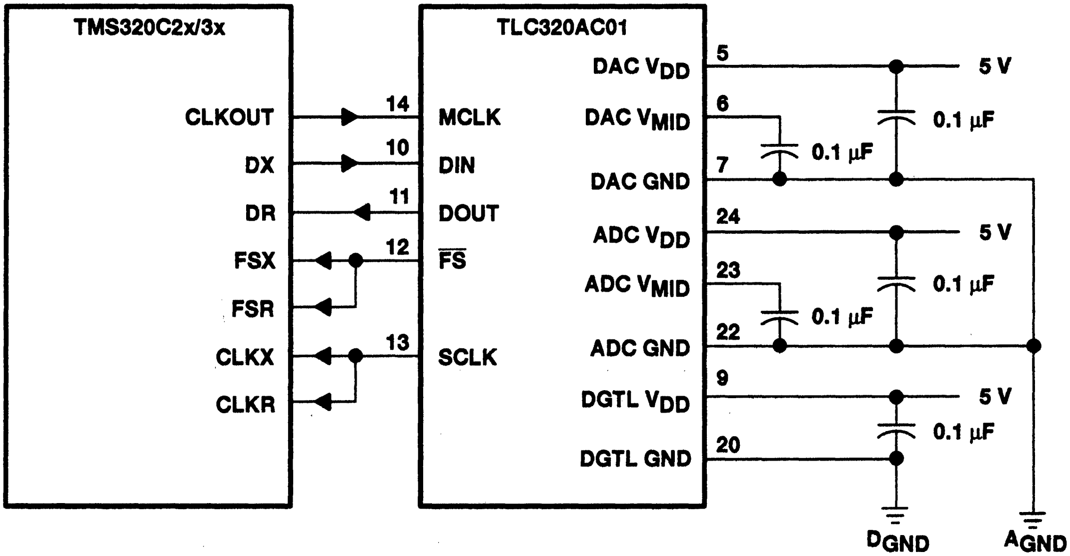


Figure 6–1. Stand-Alone Mode (to DSP Interface)

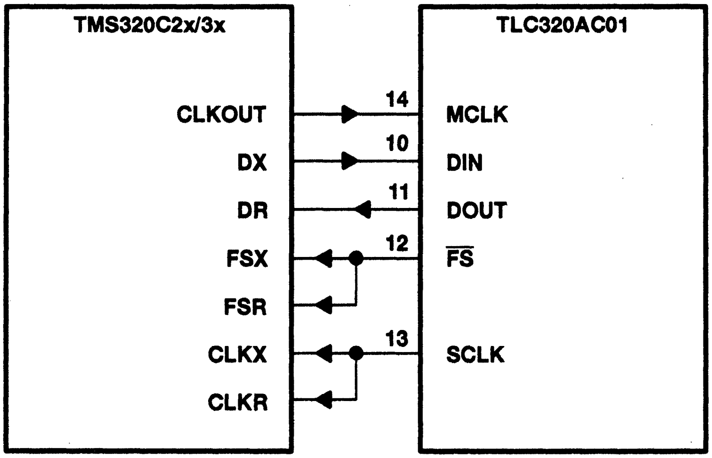
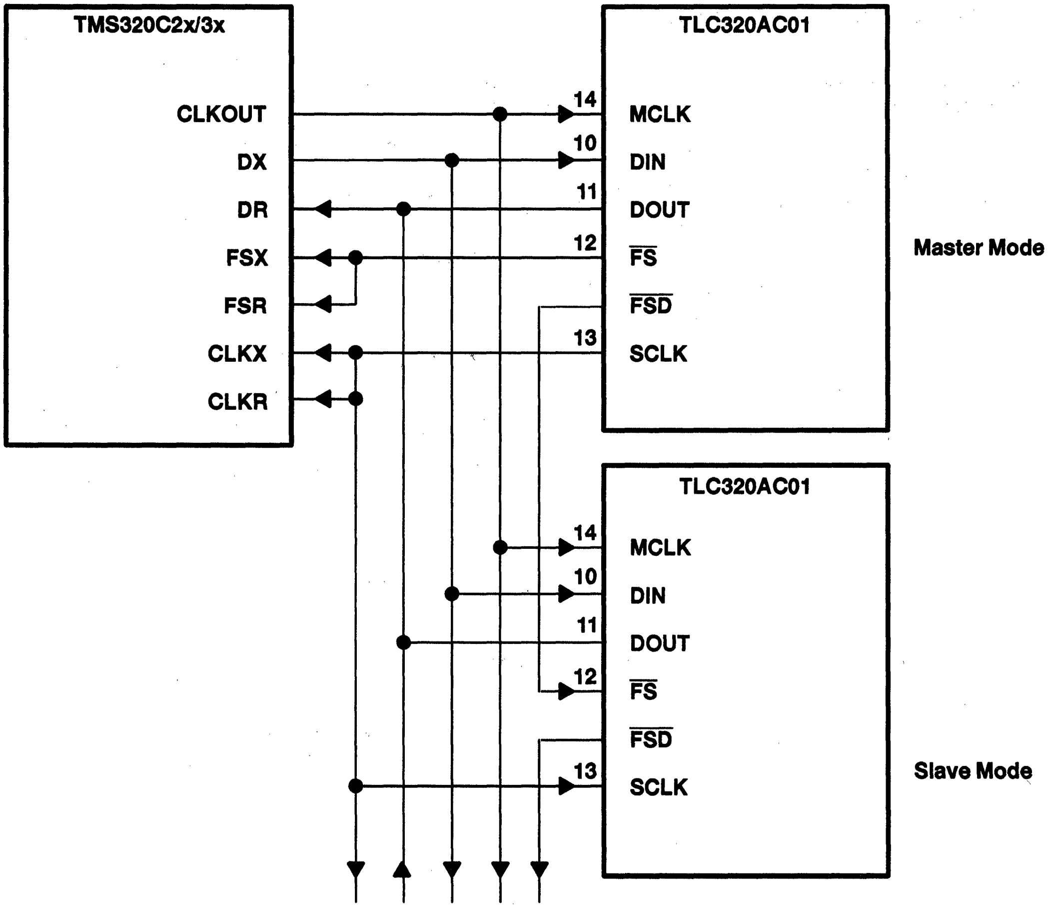


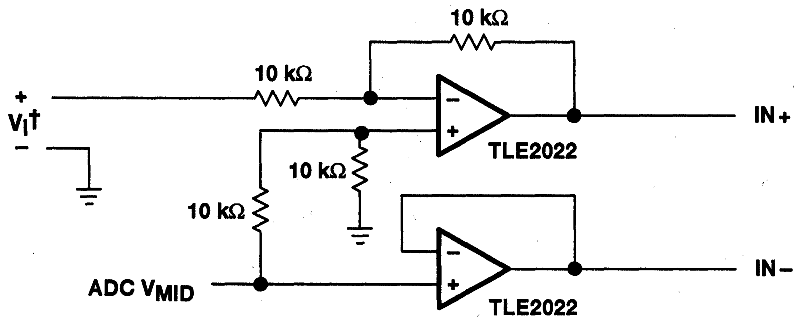
Figure 6–2. Codec Mode (to DSP Interface)

Terminal numbers shown are for the FN package.



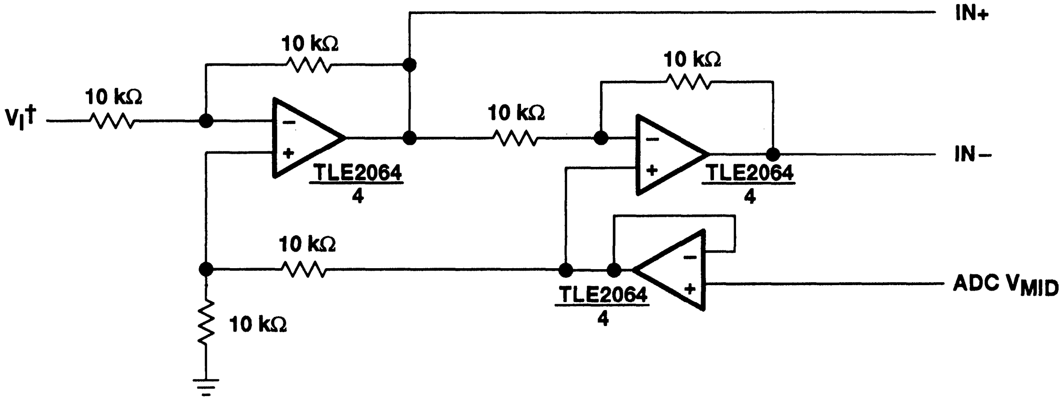
Terminal numbers shown are for the FN package.

Figure 6–3. Master With Slave (to DSP Interface)



† The V_I source must be capable of sinking a current equal to [ADC V_{MID} + $|V_I|$(max)]/10 kΩ.

Figure 6–4. Single-Ended Input (Ground Referenced)



† The V_I source must be capable of sinking a current equal to [(ADC V_{MID}/2) + |V_I|(max)]/10 kΩ.

Figure 6–5. Single-Ended to Differential Input (Ground Referenced)

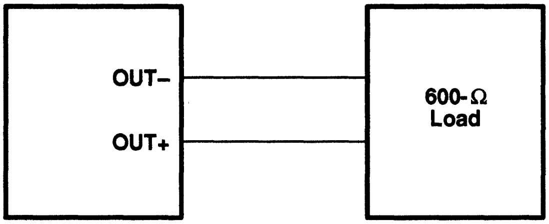
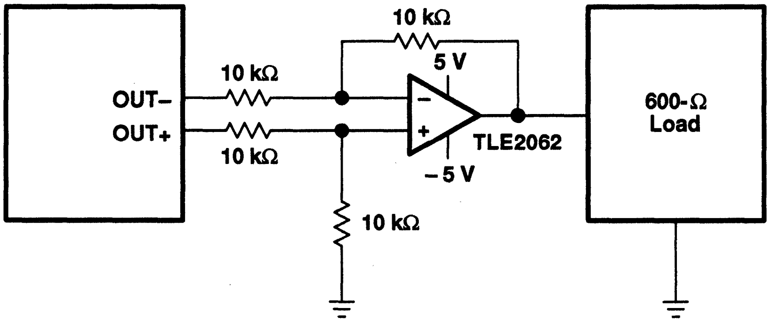


Figure 6–6. Differential Load



NOTE: When a signal changes from a single supply with a nonzero reference system to a grounded load, the operational amplifier must be powered from plus and minus supplies or the load must be capacitively coupled.

Figure 6–7. Differential Output Drive (Ground Referenced)

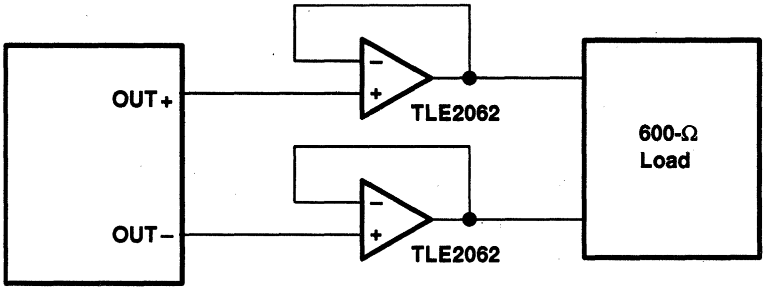
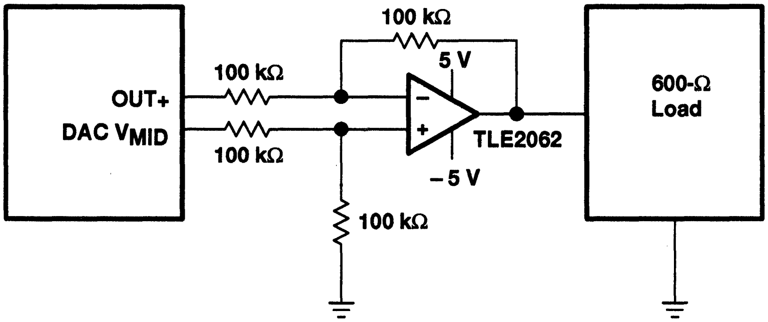


Figure 6−8. Low-Impedance Output Drive



NOTE: When a signal changes from a single supply with a nonzero reference system to a grounded load, the operational amplifier must be powered from plus and minus supplies or the load must be capacitively coupled.

Figure 6−9. Single-Ended Output Drive (Ground Referenced)

Appendix A
Primary Control Bits

The function of the primary-word control bits D01 and D00 and the hardware terminals FC0 and FC1 are shown below. Any combinational state of D01, D00, FC1, and FC0 not shown is ignored.

CONTROL FUNCTION OF CONTROL BITS

BITS		TERMINALS		
D01	D00	FC1	FC0	
0	0	0	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT.
0	0	0	1	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of the next internal $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods equal to the value contained in the A′ register. When the A′ register value is negative, the internal falling edge of $\overline{FS}$ occurs earlier.
0	0	1	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of FC1 and FC0 such that on the rising edge of the next internal $\overline{FS}$, the next ADC/DAC sample time occurs earlier by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, the internal falling edge of $\overline{FS}$ occurs later.
0	0	1	1	On the next falling edge of the primary $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. When FC0 and FC1 are both taken high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary $\overline{FS}$.
0	1	0	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, the falling edge of $\overline{FS}$ occurs earlier.
1	0	0	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00. On the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs earlier by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, the internal falling edge of $\overline{FS}$ occurs later.
1	1	0	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. When D00 and D01 are both high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary $\overline{FS}$.

CONTROL FUNCTION OF CONTROL BITS (Continued)

BITS		TERMINALS		
D01	D00	FC1	FC0	
0	1	1	1	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, $\overline{FS}$ occurs earlier. When FC0 and FC1 are both taken high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary $\overline{FS}$.
1	0	1	1	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00. On the next rising edge of $\overline{FS}$, the next ADC/DAC sample time occurs earlier by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, $\overline{FS}$ occurs later. When FC0 and FC1 are both taken high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary $\overline{FS}$.
1	1	1	1	On the next falling edge of the primary $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. When FC1 and FC0 are both high or D01 and D00 are both high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary $\overline{FS}$ occurs at 1/2 the sampling time measured from the falling edge of the primary $\overline{FS}$.
1	1	0	1	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. When D00 and D01 are high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary $\overline{FS}$. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, $\overline{FS}$ occurs earlier.
1	1	1	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. When D00 and D01 are high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary $\overline{FS}$. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, $\overline{FS}$ occurs earlier.
1	1	1	1	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. When FC1 and FC0 are both high or D01 and D00 are both high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary $\overline{FS}$ occurs at 1/2 the sampling time measured from the falling edge of the primary $\overline{FS}$.

Appendix B
Secondary Communications

The function of the control bits DS15 and DS14 and the hardware terminals FC0 and FC1 are shown below. Any combinational state of DS15, DS14, FC1, and FC0 not shown is ignored.

CONTROL FUNCTION OF SECONDARY COMMUNICATION

BITS		TERMINALS		
DS15	**DS14**	**FC1**	**FC0**	
0	0	Ignored		On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.
0	1	Ignored		On the next falling edge of the $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of DS15 and DS14 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, $\overline{FS}$ occurs earlier.
1	0	Ignored		On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00. On the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs earlier by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, $\overline{FS}$ occurs later.
1	1	0	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.
1	1	0	1	On the next falling edge of the $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, $\overline{FS}$ occurs earlier.
1	1	1	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs earlier by the number of MCLK periods determined by the value contained in the A′ register. When the A′ register value is negative, $\overline{FS}$ occurs later.
1	1	1	1	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.

Appendix C
TLC320AC01C/TLC320AC02C Specification Comparisons

Texas Instruments manufactures the TLC320AC01C and the TLC320AC02C specified for the 0°C to 70°C commercial temperature range and the TLC320AC02I specified for the −40°C to 85°C temperature range. The TLC320AC02C and TLC320AC02I operate at a relaxed TLC320AC01C specification. The differences are listed in the following tables.

ADC Channel Signal-to-Distortion Ratio, V_{DD} = 5 V, f_s = 8 kHz (Unless Otherwise Noted) (see Note 1)

PARAMETER	TEST CONDITIONS	A_V = 0 dB		A_V = 6 dB		A_V = 12 dB		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
TLC320AC01	V_I = −6 dB to −1 dB	68		—		—		dB
TLC320AC02		64		—		—		
TLC320AC01	V_I = −12 dB to −6 dB	63		68		—		
TLC320AC02		59		64		—		
TLC320AC01	V_I = −18 dB to −12 dB	57		63		68		
TLC320AC02		56		59		64		
TLC320AC01	V_I = −24 dB to −18 dB	51		57		63		
TLC320AC02		50		56		59		
TLC320AC01	V_I = −30 dB to −24 dB	45		51		57		
TLC320AC02		44		50		56		
TLC320AC01	V_I = −36 dB to −30 dB	39		45		51		
TLC320AC02		38		44		50		
TLC320AC01	V_I = −42 dB to −36 dB	33		39		45		
TLC320AC02		32		38		44		
TLC320AC01	V_I = −48 dB to −42 dB	27		33		39		
TLC320AC02		26		32		38		

NOTE 1: The analog-input test signal is a 1020-Hz sine wave with 0 dB = 6 V peak to peak as the reference level for the analog input signal.

DAC Channel Signal-to-Distortion Ratio, V_{DD} = 5 V, f_s = 8 kHz (Unless Otherwise Noted) (see Note 2)

PARAMETER	TEST CONDITIONS	A_V = 0 dB		A_V = −6 dB		A_V = −12 dB		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
TLC320AC01	V_O = −6 dB to 0 dB	68		—		—		dB
TLC320AC02		64		—		—		
TLC320AC01	V_O = −12 dB to −6 dB	63		68		—		
TLC320AC02		59		64		—		
TLC320AC01	V_O = −18 dB to −12 dB	57		63		68		
TLC320AC02		56		59		64		
TLC320AC01	V_O = −24 dB to −18 dB	51		57		63		
TLC320AC02		50		56		59		
TLC320AC01	V_O = −30 dB to −24 dB	45		51		57		
TLC320AC02		44		50		56		
TLC320AC01	V_O = −36 dB to −30 dB	39		45		51		
TLC320AC02		38		44		50		
TLC320AC01	V_O = −42 dB to −36 dB	33		39		45		
TLC320AC02		32		38		44		
TLC320AC01	V_O = −48 dB to −42 dB	27		33		39		
TLC320AC02		26		32		38		

NOTE 2: The input signal, V_I, is the digital equivalent of a 1020-Hz sine wave (full-scale analog output at full-scale digital input = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT−.

System Distortion, ADC Channel Attenuation, V_{DD} = 5 V, f_s = 8 kHz, FCLK = 144 kHz (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
TLC320AC01	Second harmonic	Differential input (see Note 3)	70		dB
TLC320AC02	Second harmonic	Differential input (see Note 3)	64		dB
TLC320AC01	Third harmonic and higher harmonics	Differential input (see Note 3)	70		dB
TLC320AC02	Third harmonic and higher harmonics	Differential input (see Note 3)	64		dB

NOTE 3: The input signal is a 1020 Hz-sine wave for the ADC channel. Harmonic distortion is defined for an input level of −1 dB.

System Distortion, DAC Channel Attenuation, V_{DD} = 5 V, f_s = 8 kHz, FCLK = 144 kHz (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
TLC320AC01	Second harmonic	Differential output (see Note 4)	70		dB
TLC320AC02	Second harmonic	Differential output (see Note 4)	64		dB
TLC320AC01	Third harmonic and higher harmonics	Differential output (see Note 4)	70		dB
TLC320AC02	Third harmonic and higher harmonics	Differential output (see Note 4)	64		dB

NOTE 4: The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT−. Harmonic distortion is specified for a signal input level of 0 dB.

TLC320AC02C, TLC320AC02I
Data Manual

Single-Supply Analog Interface Circuit

TEXAS INSTRUMENTS

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1 Introduction

The TLC320AC02† analog interface circuit (AIC) is an audio-band processor that provides an analog-to-digital and digital-to-analog input/output interface system on a single monolithic CMOS chip. This device integrates a band-pass switched-capacitor antialiasing input filter, a 14-bit-resolution analog-to-digital converter (ADC), a 14-bit-resolution digital-to-analog converter (DAC), a low-pass switched-capacitor output-reconstruction filter, (sin x)/x compensation, and a serial port for data and control transfers.

The internal circuit configuration and performance parameters are determined by reading control information into the eight available data registers. The register data are used to set up the device for a given mode of operation and application.

The major functions of the TLC320AC02 are:

1. To convert audio-signal data to digital format by the ADC channel
2. To provide the interface and control logic to transfer data between its serial input and output terminals and a digital signal processor (DSP) or microprocessor
3. To convert received digital data back to an audio signal through the DAC channel

The antialiasing input low-pass filter is a switched-capacitor filter with a sixth-order elliptic characteristic. The high-pass filter is a single-pole filter to preserve low-frequency response as the low-pass filter cutoff is adjusted. There is a three-pole continuous-time filter that precedes this filter to eliminate any aliasing caused by the filter clock signal.

The output-reconstruction switched-capacitor filter is a sixth-order elliptic transitional low-pass filter followed by a second-order (sin x)/x correction filter. This filter is followed by a three-pole continuous-time filter to eliminate images of the filter clock signal.

The TLC320AC02 consists of two signal-processing channels, an ADC channel and a DAC channel, and the associated digital control. The two channels operate synchronously; data reception at the DAC channel and data transmission from the ADC channel occur during the same time interval. The data transfer is in 2s-complement format.

There are three basic modes of operation available: the stand-alone analog-interface mode, the master-slave mode, and the linear-codec mode. In the stand-alone mode, the TLC320AC02 generates the shift clock and frame synchronization for the data transfers and is the only AIC used. The master-slave mode has one TLC320AC02 as the master that generates the master-shift clock and frame synchronization; the remaining AICs are slaves to these signals. In the linear-codec mode, the shift clock and the frame-synchronization signals are externally generated and the timing can be any of the standard codec-timing patterns.

Typical applications for this device include modems, speech processing, analog interface for DSPs, industrial-process control, acoustical-signal processing, spectral analysis, data acquisition, and instrumentation recorders.

The TLC320AC02I is characterized for operation from −40°C to 85°C, and the TLC320AC02C is characterized for operation from 0°C to 70°C.

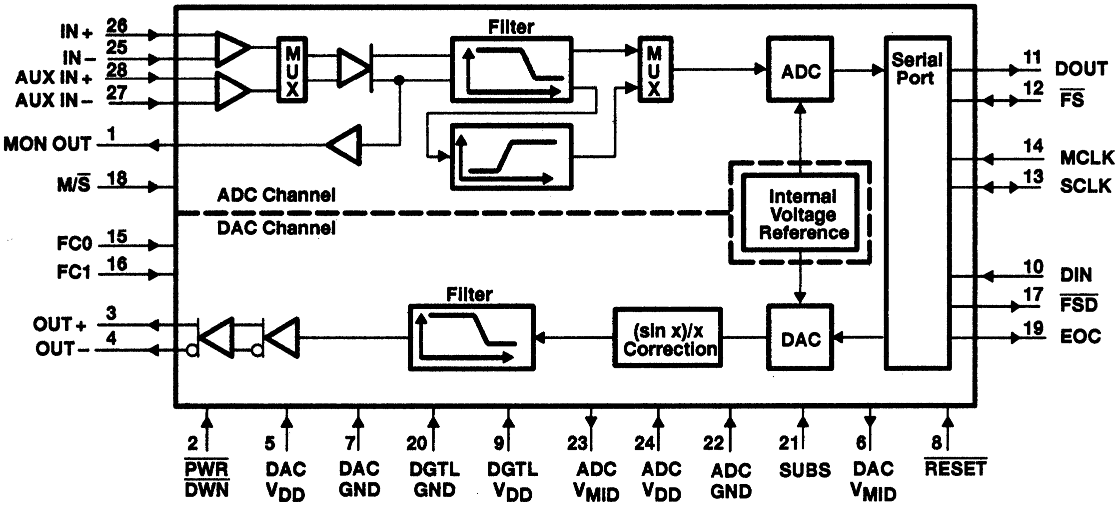
† The TLC320AC02 is functionally equivalent to the TLC320AC01 and differs only in the electrical specifications as shown in Appendix C.

1.1 Features

- General-Purpose Signal-Processing Analog Front End (AFE)
- Single 5-V Power Supply
- Power Dissipation . . . 100 mW Typ
- Signal-to-Distortion Ratio . . . 70 dB Typ
- Programmable Filter Bandwidths (up to 10.8 kHz) and Synchronous ADC and DAC Sampling
- Serial-Port Interface
- Monitor Output With Programmable Gains of 0 dB, −8 dB, −18 dB, and Squelch
- Two Sets of Differential Inputs With Programmable Gains of 0 dB, 6 dB, 12 dB, and Squelch
- Differential or Single-Ended Analog Output With Programmable Gains of 0 dB, −6 dB, −12 dB, and Squelch
- Differential Outputs Drive 3-V Peak into a 600-Ω Differential Load
- Differential Architecture Throughout
- 1-µm Advanced LinEPIC™ Process
- 14-Bit Dynamic-Range ADC and DAC
- 2s-Complement Data Format

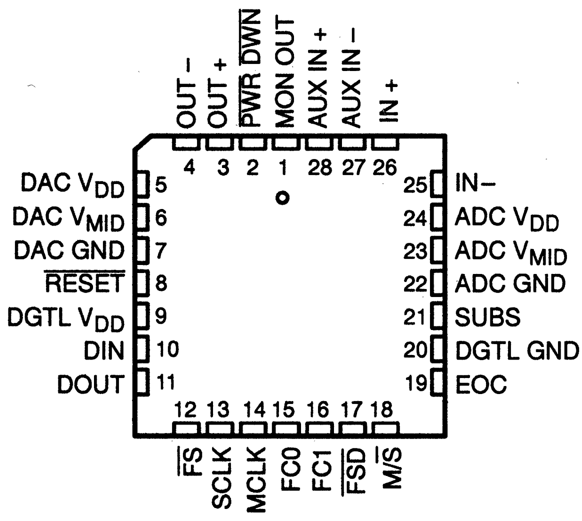
LinEPIC is a trademark of Texas Instruments Incorporated.

1.2 Functional Block Diagram



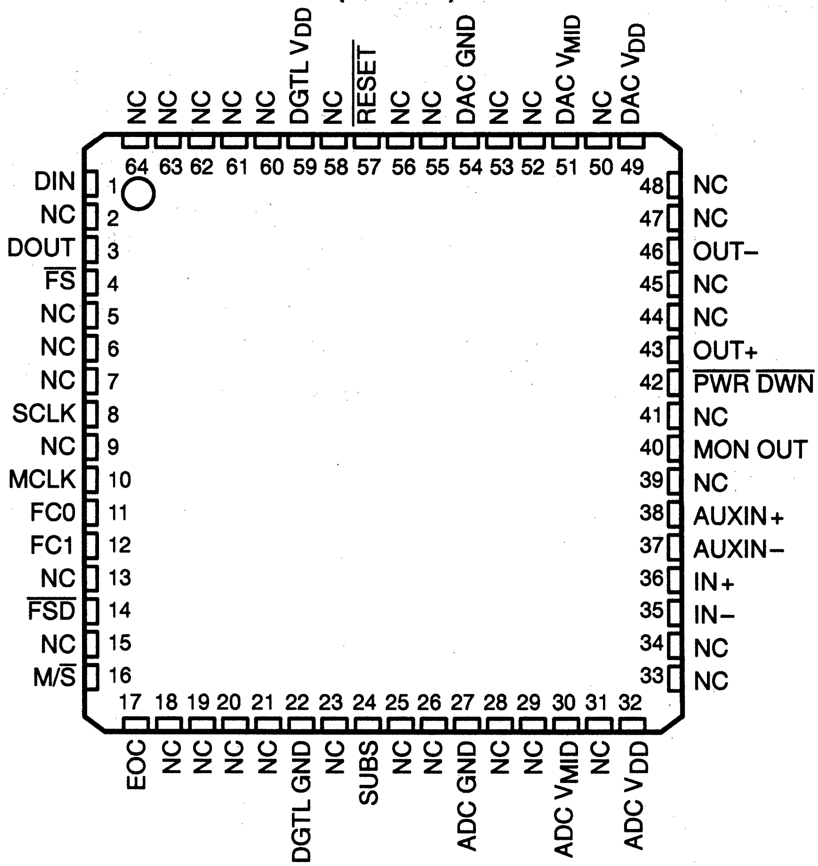
Terminal numbers shown are for the FN package.

1.3 Terminal Assignments



1.3 Terminal Assignments (Continued)

PM PACKAGE
(TOP VIEW)



NC – No internal connection

1.4 Terminal Functions

TERMINAL NAME	NO.†	NO.‡	I/O	DESCRIPTION
ADC V_{DD}	24	32	I	Analog supply voltage for the ADC channel
ADC V_{MID}	23	30	O	Midsupply for the ADC channel (requires a bypass capacitor). ADC V_{MID} must be buffered when used as an external reference.
ADC GND	22	27	I	Analog ground for the ADC channel
AUX IN+	28	38	I	Noninverting input to auxiliary analog input amplifier
AUX IN–	27	37	I	Inverting input to auxiliary analog input amplifier
DAC V_{DD}	5	49	I	Digital supply voltage for the DAC channel
DAC V_{MID}	6	51	O	Midsupply for the DAC channel (requires a bypass capacitor). DAC V_{MID} must be buffered when used as an external reference.
DAC GND	7	54	I	Analog ground for the DAC channel
DIN	10	1	I	Data input. DIN is used to receive the DAC input data and command information and is synchronized with SCLK.
DOUT	11	3	O	Data output. This terminal outputs the ADC data results and register read contents. DOUT is synchronized with SCLK.
DGTL V_{DD}	9	59	I	Digital supply voltage for control logic
DGTL GND	20	22	I	Digital ground for control logic
EOC	19	17	O	End-of-conversion output. EOC goes high at the start of the ADC conversion period and low when conversion is complete. EOC remains low until the next ADC conversion period begins and indicates the internal device conversion period.
FC0	15	11	I	Hardware control input. FC0 is used in conjunction with FC1 to request secondary communication and phase adjustments. FC0 should be tied low if it is not used.
FC1	16	12	I	Hardware control input. FC1 is used in conjunction with FC0 to request secondary communication and phase adjustments. FC1 should be tied low if it is not used.
$\overline{FS}$	12	4	I/O	Frame synchronization. When $\overline{FS}$ goes low, DIN begins receiving data bits and DOUT begins transmitting data bits. In master mode, $\overline{FS}$ is low during the simultaneous 16-bit transmission to DIN and from DOUT. In slave mode, $\overline{FS}$ is externally generated and must be low for one shift-clock period minimum to initiate the data transfer.
$\overline{FSD}$	17	14	O	Frame synchronization delayed output. This active-low output is used to synchronize a slave device to the frame synchronization timing of the master device. $\overline{FSD}$ is applied to the slave $\overline{FS}$ input and is the same duration as the master $\overline{FS}$ signal but delayed in time by the number of shift clocks programmed in the $\overline{FSD}$ register.
IN+	26	36	I	Noninverting input to analog input amplifier
IN–	25	35	I	Inverting input to analog input amplifier
MCLK	14	10	I	The master clock input is used to drive all the key logic signals of the AIC.
MON OUT	1	40	O	The monitor output allows monitoring of analog input and is a high-impedance output.
M/$\overline{S}$	18	16	I	Master/slave select input. When M/$\overline{S}$ is high, the device is the master and when low, it is a slave.

† Terminal numbers shown are for the FN package.
‡ Terminal numbers shown are for the PM package.

1.4 Terminal Functions (Continued)

TERMINAL NAME	NO.†	NO.‡	I/O	DESCRIPTION
OUT+	3	43	O	Noninverting output of analog output power amplifier. OUT+ can drive transformer hybrids or high-impedance loads directly in a differential connection or a single-ended configuration with a buffered V_{MID}.
OUT−	4	46	O	Inverting output of analog output power amplifier. OUT− is functionally identical with and complementary to OUT+.
$\overline{\text{PWR DWN}}$	2	42	I	Power-down input. When $\overline{\text{PWR DWN}}$ is taken low, the device is powered down such that the existing internally programmed state is maintained. When $\overline{\text{PWR DWN}}$ is brought high, full operation resumes.
$\overline{\text{RESET}}$	8	57	I	Reset input that initializes the internal counters and control registers. $\overline{\text{RESET}}$ initiates the serial data communications, initializes all of the registers to their default values, and puts the device in a preprogrammed state. After a low-going pulse on $\overline{\text{RESET}}$, the device registers are initialized to provide a 16-kHz data-conversion rate and 7.2-kHz filter bandwidth for a 10.368-MHz master clock input signal.
SCLK	13	8	I/O	Shift clock. SCLK clocks the digital data into DIN and out of DOUT during the frame-synchronization interval. When configured as an output (M/$\overline{\text{S}}$ high), SCLK is generated internally by dividing the master clock signal frequency by four. When configured as an input (M/$\overline{\text{S}}$ low), SCLK is generated externally and synchronously to the master clock. This signal is used to clock the serial data into and out of the device.
SUBS	21	24	I	Substrate connection. SUBS should be tied to ADC GND.

† Terminal numbers shown are for the FN package.
‡ Terminal numbers shown are for the PM package.

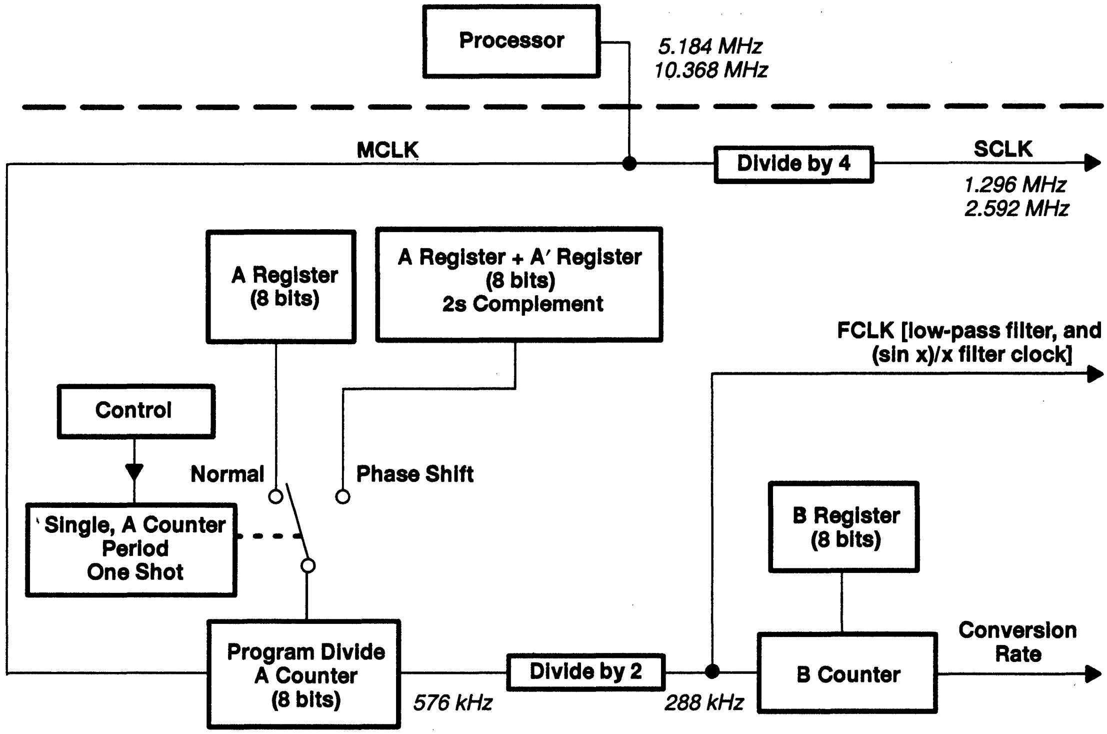


Figure 1–1. Control Flow Diagram

Table 1–1. Operating Frequencies

FCLK (kHz)	LOW-PASS FILTER BANDWIDTH (kHz)	B REGISTER CONTENTS (Program No. of Filter Clocks) (Decimal)	CONVERSION RATE (kHz)	HIGH-PASS POLE FREQUENCY (Hz)
144	3.6	20 (see Note 1)	7.2	36
		18	8	40
		15	9.6	48
		10 (see Note 2)	14.4	72
288	7.2	20 (see Note 1)	14.4	72
		18	16	80
		15	19.2	96
		10 (see Notes 2 and 3)	28.8	144
432	10.8	20 (see Note 1)	21.6	108
		18	24	120
		15 (see Note 3)	28.8	144
		10 (see Notes 2 and 3)	43.2	216

NOTES:
1. The B register can be programmed for values greater than 20; however, since the sample rate is lower than 7.2 kHz and the internal filter remains at 3.6 kHz, an external antialiasing filter is required.
2. If the B register is programmed for a value less than 10, the ADC and the DAC conversions are not completed before the next frame-sync signal and the results are in error.
3. The maximum sampling rate for the ADC channel is 43.2 kHz. The maximum rate for the DAC channel is 25 kHz.

1.5 Register Functional Summary

There are nine data registers that are used as follows:

Register 0 The No-op register. The 0 register allows phase adjustments to be made without reprogramming a data register.

Register 1 The A register controls the count of the A counter.

Register 2 The B register controls the count of the B counter.

Register 3 The A′ register controls the phase adjustment of the sampling period. The adjustment is equal to the register value multiplied by the input master period.

Register 4 The amplifier gain-select register controls the gains of the input, output, and monitor amplifiers.

Register 5 The analog control configuration register controls:

- The addition/deletion of the high-pass filter to the ADC signal path
- The enable/disable of the analog loopback
- The selection of the regular inputs or auxiliary inputs
- The function that allows processing of signals that are the sum of the regular inputs and the auxiliary inputs ($V_{IN} + V_{AUX\ IN}$).

Register 6 The digital configuration register controls:

- Selection of the free-run function
- $\overline{FSD}$ [frame-synchronization (sync) delay] output enable/disable
- Selection of 16-bit function
- Forcing secondary communications
- Software reset
- Software power down

Register 7 The frame-sync delay register controls the time delay between the master-device frame sync and slave-device frame sync. Register 7 must be the last register programmed when using slave devices since all register data is latched and valid on the 16th falling edge of SCLK. On the 16th falling edge of SCLK, all delayed frame-sync intervals are shifted by this programmed amount.

Register 8 The frame-sync number register informs the master device of the number of slaves that are connected in the chain.

2 Detailed Description

2.1 Definitions and Terminology

ADC Channel	All signal processing circuits between the analog input and the digital conversion results at DOUT
Codec Mode	The operating mode under which the device receives shift clock and frame-sync signals from a host processor. The device has no slaves.
d	The d represents valid programmed or default data in the control register format (see Section 2.19, Secondary Serial Communications) when discussing other data-bit portions of the register.
Dxx	Bit position in the primary data word (xx is the bit number)
DAC Channel	All signal processing circuits between the digital data word applied to DIN and the differential output analog signal available at OUT+ and OUT–
Data Transfer Interval	The time during which data is transferred from DOUT and to DIN. This interval is 16 shift clocks regardless of whether the shift clock is internally or externally generated. The data transfer is initiated by the falling edge of the frame-sync signal.
DSxx	Bit position in the secondary data word (xx is the bit number)
FCLK	An internal clock frequency that is a division of MCLK that controls the low-pass filter and (sinx)/x filter clock (see Figure 1–1 and Table 1–1).
f_i	The analog input frequency of interest
Frame Sync	The falling edge of the signal that initiates the data-transfer interval. The primary frame sync starts the primary communications, and the secondary frame sync starts the secondary serial communications.
Frame Sync and Sampling Period	The time between falling edges of successive primary frame-sync signals
Frame-Sync Interval	The time period occupied by 16 shift clocks. Regardless of the mode of operation, there is always an internal frame-sync interval signal that goes low on the rising edge of SCLK and remains low for 16 shift clocks. It is used for synchronization of the serial-port internal signals. It goes high on the 17th rising edge of SCLK.
f_s	The sampling frequency that is the reciprocal of the sampling period
Host	Any processing system that interfaces to DIN, DOUT, SCLK, or $\overline{\text{FS}}$
Master Mode	The operating mode under which the device generates and uses its own shift clock and frame-sync signal and generates all delayed frame-sync signals necessary to support slave devices
Phase Adjustment	The programmed time variation from the falling edge of one frame-sync signal to the falling edge of the next frame sync signal. The time variation is determined by the contents of the A′ register. Since the time between falling edges of successive frame sync signals is the the sampling period, the sampling period is adjusted.
Primary (Serial) Communications	The digital data-transfer interval. Since the device is synchronous, the signal data words from the ADC channel and to the DAC channel occur simultaneously.
Secondary (Serial) Communications	The digital control and configuration data-transfer interval into DIN and the register read-data cycle from DOUT. The data-transfer interval occurs when requested by hardware or software.
Signal Data	The input signal and all of the converted representations through the ADC channel and return through the DAC channel to the analog output. This is contrasted with the purely digital software control data.

Slave Mode	The operating mode under which the device receives shift clock and frame-sync signals from a master device
Stand-Alone Mode	The operating mode under which the device generates and uses its own shift clock and frame-sync signal. The device has no slave devices.
X	The X represents a don't care bit position within the control register format

2.2 Reset and Power-Down Functions

2.2.1 Reset

The TLC320AC02 resets both the internal counters and registers, including the programmed registers, by any of the following:

- Applying power to the device, causing a power-on reset (POR)
- Applying a low reset pulse to $\overline{\text{RESET}}$
- Reading in the programmable software reset bit (DS01 in register 6)

$\overline{\text{PWR}}$ $\overline{\text{DWN}}$ resets the counters only and preserves the programmed register contents.

2.2.2 Conditions of Reset

The two internal reset signals used for the reset and synchronization functions are as follows:

1. Counter reset: this signal resets all flip-flops and latches that are not externally programmed with the exception of those generating the reset pulse itself. In addition, this signal resets the software power-down bit.

   Counter reset = power-on reset + $\overline{\text{RESET}}$ + RESET bit + $\overline{\text{PWR}}$ $\overline{\text{DWN}}$

2. Register reset: this signal resets all flip-flops and latches that are not reset by the counter reset except those generating the reset pulse itself.

   Register reset = power-on reset + $\overline{\text{RESET}}$ + RESET bit

Both reset signals are at least one master clock period long and release on the falling edge of the master clock.

2.2.3 Software and Hardware Power Down

Given the definitions and conditions of $\overline{\text{RESET}}$, the software-programmed power-down condition is cleared by resetting the software bit (DS00 in register 6) to zero. It is also cleared by either cycling the power to the device, bringing $\overline{\text{PWR}}$ $\overline{\text{DWN}}$ low, or bringing $\overline{\text{RESET}}$ low.

$\overline{\text{PWR}}$ $\overline{\text{DWN}}$ powers down the entire chip (< 1 mA). The software-programmable power-down bit only powers down the analog section of the chip (< 3 mA), which allows a software power-up function. Cycling $\overline{\text{PWR}}$ $\overline{\text{DWN}}$ high to low and back to high resets all flip-flops and latches that are not externally programmed, thereby preserving the register contents.

If $\overline{\text{PWR}}$ $\overline{\text{DWN}}$ is not used, it should be tied high.

2.2.4 Register Default Values After POR, Software Reset, or $\overline{\text{RESET}}$ Is Applied

Register 1 – The A Register

The default value of the A-register data is decimal 18 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	0	1	0

Register 2 – The B Register

The default value of the B-register data is decimal 18 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	0	1	0

Register 3 – The A′ Register

The default value of the A′-register data is decimal 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

Register 4 – The Amplifier Gain-Select Register

The default value of the amplifier gain-select register data is shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	1	0	1

Register 5 – The Analog Control Configuration Register

The power-up and reset conditions are as shown below. In the read mode, eight bits are read but the four LSBs are repeated as the four MSBs.

DS03	DS02	DS01	DS00
0	1	0	1

Register 6 – The Digital Configuration Register

The default value of DS07 – DS00 is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

Register 7 – The Frame-Sync Delay Register

The default value of DS07 – DS00 is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

Register 8 – The Frame-Sync Number Register

The default value of DS07 – DS00 is 1 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	1

2.3 Master-Slave Terminal Function

Table 2–1 describes the function of the master/slave ($M/\overline{S}$) input. The only difference between master and slave operations in the TLC320AC02 is that SCLK and $\overline{FS}$ are outputs when $M/\overline{S}$ is high and inputs when $M/\overline{S}$ is low.

Table 2–1. Master-Slave Selection

MODE	$M/\overline{S}$†	$\overline{FS}$	SCLK
Master and Stand-Alone	H	Output	Output
Slave and Codec Emulation	L	Input	Input

† If the stand-alone mode is desired or if the device is permanently in the master mode, $M/\overline{S}$ must be high.

2.4 ADC Signal Channel

To produce excellent common-mode rejection of unwanted signals, the analog signal is processed differentially until it is converted to digital data. The signal is amplified by the input amplifier at one of three software-selectable gains (typically 0 dB, 6 dB, or 12 dB). A squelch mode can also be programmed for the input amplifier.

The amplifier output is filtered and applied to the ADC input. The ADC converts the signal into discrete digital words in 2s-complement format corresponding to the analog-signal value at the sampling time. These 16-bit digital words, representing sampled values of the analog input signal, are clocked out of the serial port, (DOUT), one word for each primary communication interval. During secondary communications, the data previously programmed into the registers can be read out with the appropriate register address and with the read bit set to 1. If no register read is requested, all 16 bits are 0.

2.5 DAC Signal Channel

DIN receives the 16-bit serial data word (2s complement) from the host during the primary communications interval and latches the data on the 17th rising edge of SCLK. The data are converted to an analog voltage by the DAC with a sample and hold and then through a (sin x)/x correction circuit and a smoothing filter. An output buffer with three software-programmable gains (0 dB, −6 dB, and −12 dB), as shown in Section 2.20.5, Register 4 (Amplifier Gain-Select Register), drives the differential outputs OUT+ and OUT−. A squelch mode can also be programmed for the output buffer. During secondary communications, the configuration program data are read into the device control registers.

2.6 Serial Interface

The digital serial interface consists of the shift clock, the frame-synchronization signal, the ADC-channel data output, and the DAC-channel data input. During the primary 16-bit frame-synchronization interval, the SCLK transfers the ADC channel results from DOUT and transfers 16-bit DAC data into DIN.

During the secondary frame-synchronization interval, the SCLK transfers the register read data from DOUT if the read bit is set to a one. In addition, the SCLK transfers control and device parameter information into DIN. The functional sequence is shown in Figure 2–1.

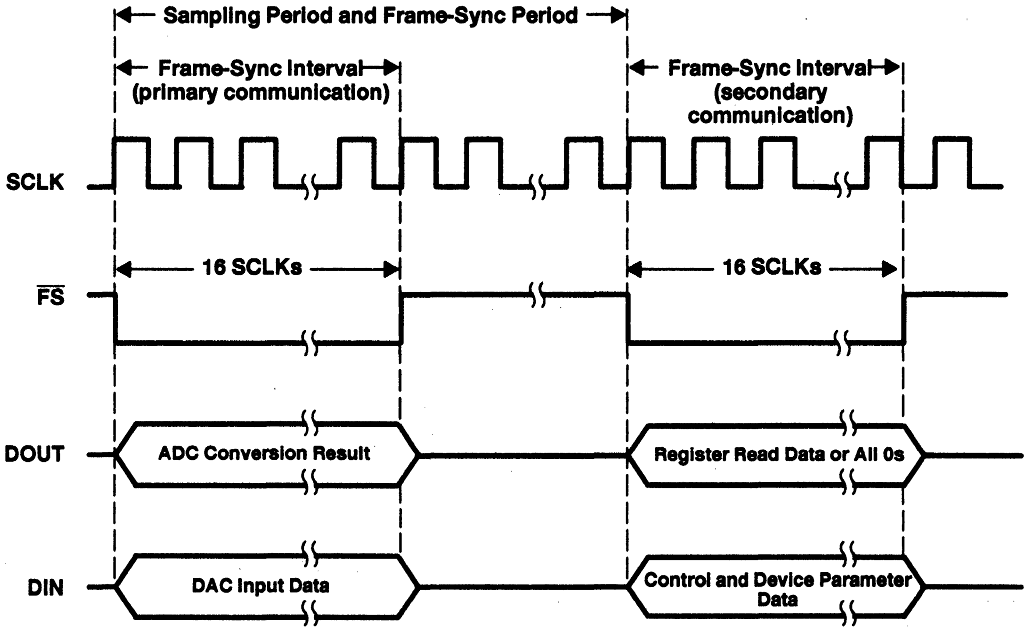


Figure 2–1. Functional Sequence for Primary and Secondary Communication

2.7 Number of Slaves

The number of slaves is determined by the sum of the individual device delays from the frame-sync ($\overline{FS}$) input low to the frame-sync delayed ($\overline{FSD}$) low for all slaves as follows:

$$(n) \times tp(FS-FSD) < 1/2 \text{ shift-clock period}$$

Where:

n is the number of slave devices.

Example:

From the above equation, the number of slaves is given by:

$$(n) \le \frac{1}{2} \times (\text{SCLK period}) \times \frac{1}{tp(FS - FSD)}$$

and assuming the shift clock is 2.4 MHz and tp(FS – FSD) is 40 ns, then the number of slaves is:

$$n \le \frac{1}{2.4\ \text{MHz}} \times \frac{1}{2} \times \frac{1}{40\ \text{ns}} = \frac{1000}{192} = 5.2$$

The maximum number of slaves under these conditions is five. As the SCLK increases in frequency, the number of slaves that can be used decreases.

2.8 Operating Frequencies

2.8.1 Master and Stand-Alone Operating Frequencies

The sampling (conversion) frequency is derived from the master clock (MCLK) input by the following equation:

$$f_S = \text{Sampling (conversion) frequency} = \frac{\text{MCLK}}{(\text{A register value}) \times (\text{B register value}) \times 2}$$

The inverse is the time between the falling edges of two successive primary frame synchronization signals. The input and output data clock (SCLK) is given by:

$$\text{SCLK frequency} = \frac{\text{MCLK frequency}}{4}$$

2.8.2 Slave and Codec Operating Frequencies

The slave and codec conversion and the data frequencies are determined by the externally applied SCLK and $\overline{\text{FS}}$ signals.

2.9 Switched-Capacitor Filter Frequency (FCLK)

The filter clock (FCLK) is an internal clock signal that is used to determine the filter band-pass frequency and is the B counter clock. The frequency of the filter clock is derived by the following equation:

$$\text{FCLK} = \frac{\text{MCLK}}{(\text{A register value}) \times 2}$$

2.10 Filter Bandwidths

The low-pass (LP) filter −3 dB corner is derived by:

$$f\ (\text{LP}) = \frac{\text{FCLK}}{40} = \frac{\text{MCLK}}{40 \times (\text{A register value}) \times 2}$$

The high-pass (HP) filter −3 dB corner is derived by:

$$f\ (\text{HP}) = \frac{\text{Sampling frequency}}{200} = \frac{\text{MCLK}}{200 \times 2 \times (\text{A register value}) \times (\text{B register value})}$$

2.11 Required Minimum Number of MCLK Periods

The number of MCLKs necessary for proper operation if only the primary communications are used is:

Total number of MCLKs = (16 + 2) SCLKs × 4 MCLKs per SCLK
= 72 MCLKs minimum

The number of MCLKs necessary for proper operation if both the primary and secondary communications are used is:

Total number of MCLKs = (16 + 2) SCLKs × 2 × 4 MCLKs per SCLK
= 144 MCLKs minimum

Even though the TLC320AC02 can perform with this number of MCLKs, the host may need more time to execute the required software instructions between primary and secondary communication intervals.

2.12 Master and Stand-Alone Modes

The difference between the master and stand-alone modes is that in the stand-alone mode there are no slave devices. Functionally these two modes are the same. In both, the AIC internally generates the shift clock and frame-sync signal for the serial communications. These signals and the filter clock (FCLK) are derived from the input master clock.The master clock applied at the MCLK input determines the internal device timing. The shift clock frequency is a divide-by-four of the master clock frequency and shifts both the input and output data at DIN and DOUT, respectively, during the frame-sync interval (16 shift clocks long). To begin the communication sequence, the device is reset (see Section 2.2.1, Reset), and the first frame sync occurs approximately 648 master clocks after the reset condition disappears.

2.12.1 Register Programming

All register programming occurs during secondary communications, and data is latched and valid on the 16th falling edge of SCLK. After a reset condition, eight primary and secondary communications cycles are required to set up the eight programmable registers. Registers 1 through 8 are programmed in secondary communications intervals 1 through 8, respectively. If the default value for a particular register is desired, that register does not need to be addressed during the secondary communications. The no-op command addresses the pseudo-register (register 0), and no register programming takes place during this communication. The no-op command allows phase shifts of the sampling period without reprogramming any register.

During the eight register programming cycles, DOUT is in the high-impedance state. DOUT is released on the rising edge of the eighth primary internal frame-sync interval. In addition, each register can be read back during DOUT secondary communications by setting the read bit to 1 in the appropriate register. Since the register is in the read mode, no data can be written to the register during this cycle. To return this register to the write mode requires a subsequent secondary communication (see Section 2.19, Secondary Serial Communications for detailed register description).

2.12.2 Master and Stand-Alone Functional Sequence

The A counter counts according to the contents of the A register, and the A counter frequency is divided by two to produce the filter clock (FCLK). The B counter is clocked by FCLK with the following functional sequence:

1. The B counter starts counting down from the B register value minus one. Each count remains in the counter for one FCLK period including the zero count. This total counter time is referred to as the B cycle. The end of the zero count is called the end of B cycle.
2. When the B counter gets to a count of nine, the A-to-D conversion starts.
3. The A-to-D conversion is complete ten FCLK periods later.
4. $\overline{FS}$ goes low on a rising edge of SCLK after the A-to-D conversion is complete. That rising edge of SCLK must be preceded by a falling edge of SCLK, which is the first falling edge to occur after the end of B cycle.
5. The D-to-A conversion cycle begins on the rising edge of the internal frame-sync interval and is complete ten FCLK periods later.

2.13 Slave and Codec Modes

The only difference between the slave and codec modes is that the codec mode is controlled directly by the host and does not use a delayed frame-sync signal. In these modes, the shift clock and the frame sync are both externally generated and must be synchronous with MCLK. The conversion frequency is set by the time interval of externally applied frame sync falling edges except when the free-run function is selected by bit 5 of register 6 (see Section 2.15.4, Free-Run Mode). The slave device or devices share the shift clock generated by the master device but receive the frame sync from the previous slave in the chain. The Nth slave $\overline{FS}$ receives the (N−1)st slave $\overline{FSD}$ output and so on. The first slave device in the chain receives $\overline{FSD}$ from the master.

2.13.1 Slave and Codec Functional Sequence

The A counter counts according to the contents of the A register, and the A counter frequency is divided by two to produce the filter clock (FCLK). The device function in the slave or codec mode is the same as steps 1 through 3 of the B cycle description in the master mode but differs as follows:

1. Same as master
2. Same as master
3. Same as master
4. All internal clocks stop 1/2 FCLK before the end of count 0 in the B counter cycle.
5. All internal clocks are restarted on the first rising edge of MCLK after the external $\overline{FS}$ input goes low. This operation provides the synchronization necessary when using an external $\overline{FS}$ signal.
6. The D-to-A conversion starts on the rising edge of the internally generated frame-sync interval at the end of the 16-shift clock data transfer.

In the slave mode, the master controls the phase adjustments for itself and all slaves since all devices are programmed in the same frame-sync interval. In the codec mode, the shift clock and frame sync are externally generated and provide the timing for the ADC and DAC if the free-run function has not been selected (see Section 2.15.4, Free-Run Mode). In the codec mode, there is usually no need for phase adjustments; however, any required phase adjustments must be made by adjusting the external frame-sync timing (sampling time).

2.13.2 Slave Register Programming

When slave devices are used on power up or reset, all slave frame-sync signals occur at the same time as the master frame-sync signal and all slave devices are programmed during the master secondary frame-sync interval with the same data as the master. The last register programmed must be the frame-sync delay (FSD) register because the delay starts immediately on the rising edge of the 17th shift clock of that frame-sync interval. After the FSD register programming is completed for the master and slave, the slave primary frame interval is shifted in time (time slot allocated) according to the data contained in the slave FSD registers. The master then generates frame-sync intervals for itself and each slave to synchronize the host serial port for data transfers for itself and all slave devices.

The number of slaves is specified in the frame-sync number (FSN) register (register 8); therefore, the number of frame-sync intervals generated by the master is equal to the number of slaves plus one (see Section 2.7, Number of Slaves). These master frame-sync intervals are separated in time by the delay time specified by the FSD register (register 7). These master-generated intervals are the only frame-sync interval signals applied to the host serial port to provide the data transfer time slot for the slave devices.

2.14 Terminal Functions

2.14.1 Frame-Sync Function

The frame-sync signal is used to indicate that the device is ready to send and receive data for both master and slave modes. The data transfer begins on the falling edge of the frame-sync signal.

2.14.1.1 Frame Sync ($\overline{FS}$), Master Mode

The frame sync is generated internally. $\overline{FS}$ goes low on the rising edge of SCLK and remains low for the 16-bit data transfer. In addition to generating its own frame-sync interval, the master also outputs a frame sync for each slave that is being used.

2.14.1.2 Frame-Sync Delayed ($\overline{FSD}$), Master Mode

For the master, the frame-sync delayed output occurs 1/2 shift-clock period ahead of $\overline{FS}$ to compensate for the time delay through the master and slave devices. The timing relationships are as follows:

1. If the FSD register data is 0, then $\overline{FSD}$ goes low on the falling edge of SCLK and prior to the rising edge of SCLK when $\overline{FS}$ goes low (see Figure 4–4).
2. If the FSD register data is greater than 16, then $\overline{FSD}$ goes low on a rising edge of SCLK that is the FSD register number of SCLKs after the falling edge of $\overline{FS}$.

Register data values from 1 to 16 result in the default register value of zero.

2.14.1.3 Frame Sync ($\overline{FS}$), Slave Mode

The frame-sync timing is generated externally, applied to $\overline{FS}$, and controls the ADC and DAC timing (see Section 2.15.4, Free-Run Mode). The external frame-sync width must be a minimum of one shift clock to be recognized and can be as long as 16 shift clocks.

2.14.1.4 Frame-Sync Delayed ($\overline{FSD}$), Slave Mode

This output is fed from the master to the first slave and the first slave $\overline{FSD}$ output to the second and so on down the chain. The FSD timing sequence in the slave mode is as follows:

1. If the FSD register data is 0, then $\overline{FSD}$ goes low after $\overline{FS}$ goes low (see Figure 4–5).
2. When the FSD register data is greater than 16, $\overline{FSD}$ goes low on a rising edge of SCLK that is the FSD register number of SCLKs after the falling edge of $\overline{FS}$.

Data values from 1 to 16 are constrained because the data transfer requires 16 clock periods.

2.14.2 Data Out (DOUT)

DOUT is placed in the high-impedance state on the 17th rising edge of SCLK (internal or external) after the falling edge of frame sync. In the primary communication, the data word is the ADC conversion result. In the secondary communication, the data is the register-read results when requested by the read/write (R/$\overline{W}$) bit with the eight MSBs set to zero (see the Serial Communications section). If no register read is requested, the secondary word is all zeroes.

2.14.2.1 Data Out, Master Mode

In the master mode, DOUT is taken from the high-impedance state by the falling edge of frame sync. The most significant data bit then appears on DOUT.

2.14.2.2 Data Out, Slave Mode

In the slave mode, DOUT is taken from the high-impedance state by the falling edge of the external frame sync or the rising edge of the external SCLK, whichever occurs first (see Figure 4–7). The falling edge of frame sync can occur ±1/4 SCLK period around the SCLK rising edge (see Figure 4–3). The most significant data bit then appears on DOUT.

2.14.3 Data In (DIN)

In the primary communication, the data word is the digital input signal to the DAC channel. In the secondary communication, the data is the control and configuration data to set up the device for a particular function (see Section 2.16, Serial Communications).

2.14.4 Hardware Program Terminals (FC1 and FC0)

These inputs provide for hardware programming requests for secondary communication or phase adjustment. These inputs work in conjunction with the control bits D01 and D00 of the primary data word or control bits DS15 and DS14 of the secondary data word. The data on FC1 and FC0 are latched on the rising edge of the next internally generated primary or secondary frame-sync interval. These inputs should be tied low if not used (see Section 2.17, Request for Secondary Serial Communication and Table 2–3).

2.14.5 Midpoint Voltages (ADC V_{MID} and DAC V_{MID})

Since the device operates at a single-supply voltage, two midpoint voltages are generated for internal signal processing. ADC V_{MID} is used for the ADC channel reference, and DAC V_{MID} is used for the DAC channel reference. Two references are used to minimize channel-to-channel noise and crosstalk. ADC V_{MID} and DAC V_{MID} must be buffered if used as a reference for external signal processing.

2.15 Device Functions

2.15.1 Phase Adjustment

In some applications, such as modems, the device sampling period may require an adjustment to synchronize with the incoming bit stream to improve the signal-to-noise ratio. The TLC320AC02 can adjust the sampling period through the use of the A′ register and the control bits.

2.15.1.1 Phase-Adjustment Control

A phase adjustment is a programmed variation in the sampling period. A sampling period is adjusted according to the data value in the A′ register, and the phase adjustment is that number of master clocks (MCLK). An adjustment is made during device operation with data bits D01 and D00 in the primary communication, with data bits DS15 and DS14 in the secondary word or in combination with the hardware pins FC1 and FC0 (see Table 2–3). This adjustment request is latched on the rising edge of the next internal frame-sync interval and is only valid for the next sampling period. To repeat the phase adjustment, another phase request must be initiated.

2.15.1.2 Use of the A′ Register for Phase Adjustment

The A′ register value is used to make slight timing adjustments to the sampling period. The sampling period increases or decreases according to the sign of the programmed A′ register value and the state of data bits D01 and D00 in the primary data word.

The general equation for the conversion frequency is given as:

$$f_s = \text{conversion frequency} = \frac{\text{MCLK}}{(2 \times \text{A register value} \times \text{B register value}) \pm (\text{A}' \text{ register value})}$$

Therefore, if A′ = 0, the device conversion (sampling) frequency and period is constant.

If a nonzero A′ value is programmed, the sampling frequency and period responds as shown in Table 2–2.

Table 2–2. Sampling Variation With A′

D01	D00	SIGN OF THE A′ REGISTER VALUE	
		PLUS VALUE (+)	NEGATIVE VALUE (–)
0	1 (increase command)	Frequency decreases, period increases	Frequency increases, period decreases
1	0 (decrease command)	Frequency increases, period decreases	Frequency decreases, period increases

An adjustment to the sampling period, which must be requested through D01 and D00 of the primary data word to DIN, is valid for the following sampling period only. If the adjustment is required for the subsequent sampling period, it must be requested again through D01 and D00 of the primary data word. For each request, only the sampling period occurring immediately after the primary data word request is affected.

The amount of time shift in the entire sampling period ($1/f_S$) is as follows:

If the sampling period is set to 125 µs (8 kHz), the A′ register is loaded with decimal 10 and the TLC320AC02 master clock frequency is 10.386 MHz. The amount of time each sampling period is increased or decreased, when requested, is:

Time shift = (A′ register value) × (MCLK period)

The device changes the entire sampling period by only the MCLK period times the A′ register value.

Change in sampling period = contents of A′ register × master clock period
= 10 × 96.45 ns = 964 ns (less than 1% of the sampling period)

The sampling period changes by 964.5 ns each time the phase adjustment is requested by the primary data word (i.e., once per sampling period).

It is evident then that the change in sampling period is very small compared to the sampling period. To observe this effect over a long period of time (> sampling period), this change must be continuously requested by the primary data word. If the adjustment is not requested again, the sampling period changes only once and it may appear that there was no execution of the command. This is especially true when bench testing the device. Automatic test equipment can test for results within a single sampling period.

Internally, the A′ register value only affects one cycle (period) of the A counter. The A and A′ values are additive, but only for one A-counter period. The A counter begins the first count at the default or programmed A-register value and counts down to the A′-register value. As the A′ value increases or decreases, the first clock cycle from the A counter is lengthened or shortened. The initial A-counter period is the only counter period affected by the A′ register such that only this single period is increased or decreased.

2.15.2 Analog Loopback

This function allows the circuit to be tested remotely. In loopback, OUT+ and OUT– are internally connected to IN+ and IN–. The DAC data bits D15 to D02 that are applied to DIN can be compared with the ADC output data bits D15 to D02 at DOUT. There are some differences due to the ADC and DAC channel offset. The loopback function is implemented by setting DS01 and DS00 to zero in control register 5 (see Section 2.19, Secondary Serial Communications).

2.15.3 16-Bit Mode

In the 16-bit mode, the device ignores the last two control bits (D01 and D00) of the primary word and requests continual secondary communications to occur. By ignoring the last two primary communication bits, compatibility with existing 16-bit software can be maintained. This function is implemented by setting bit DS03 to one in register 6. To return to normal operation, DS03 must be reprogrammed to zero.

2.15.4 Free-Run Mode

With the free-run bit set in register 6, the external shift clock and frame sync control only the data transfer. The ADC and DAC timing are controlled by the A and B register values, and the phase-shift adjustment must be done as if the device is in stand-alone mode (by the software or state of FC1 and FC0).

Phase adjustment cannot be made by adjustment of the frame-sync timing. The external frame sync must occur within 1/2 FCLK period of the internal frame sync (FCLK as determined by the values of the A and B registers).

If the external frame sync occurs simultaneously with the internal load, the data-transfer request by the external frame sync takes precedence over the internal load command. The latching of the ADC conversion data in the output register is inhibited until the current 16 bits are shifted out of the register by the shift clock.

2.15.5 Force Secondary Communication

With bit 2 in register 6 set to 1, secondary communication is requested continuously. It overrides all software and hardware requests concerning secondary communication. Phase shifting, however, can still be performed with the software and hardware.

2.15.6 Enable Analog Input Summing

By setting bits DS01 and DS00 to 11 in register 5, the normal analog input voltage is summed with the auxiliary input voltage. The gain for the analog input amplifier is set by data bits DS03 and DS02 in register 4.

2.15.7 DAC Channel (sin x)/x Error Correction

The (sin x)/x compensation filter is designed for zero (sin x)/x error using a B-register value of 15. Since the filter cannot be removed from the signal path, operation using another B-register value results in an error in the reconstructed analog output. The error is given by the following equation. Any error compensation needed by a given application can be performed in the software.

$$\text{DAC channel frequency response error} = 20 \times \log_{10}\left[\frac{\sin\left(\dfrac{2\pi \times A \times B}{f_{MCLK}} \times f\right)}{\sin\left(\dfrac{30\pi \times A}{f_{MCLK}} \times f\right)} \times \frac{15}{B}\right]$$

where:

f = the frequency of interest
f_{MCLK} = the TLC320AC02 master clock frequency
A = the A-register value
B = the B-register value

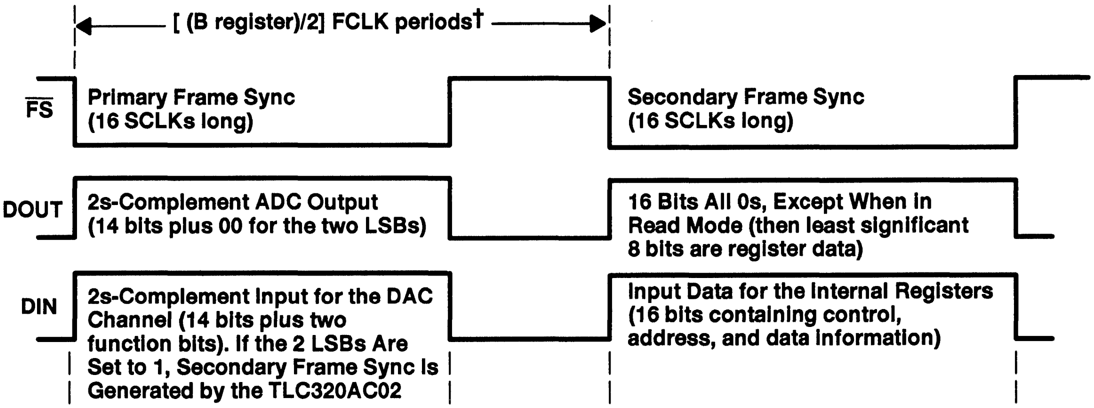
and the arguments of the sin functions are in radians.

2.16 Serial Communications

2.16.1 Stand-Alone and Master-Mode Word Sequence and Information Content During Primary and Secondary Communications

For the stand-alone and master modes, the sequence in Figure 2–2 shows the relationship between the primary and secondary communications interval, the data content into DIN, and the data content from DOUT.

The TLC320AC02 can provide a phase-shift command or the next secondary communications interval by decoding 1) the programmed state of the FC1 and FC0 inputs and the D01 and D00 data bits in the primary data word or 2) the state of the FC1 and FC0 inputs and the DS15 and DS14 data bits in the secondary data word (see Table 2–3). If DS13 (the R/$\overline{W}$ bit) is the default value of zero, all 16 bits from DOUT are 0 during secondary communication. However, when the R/$\overline{W}$ bit is set to one in the secondary communication control word, the secondary transmission from DOUT still contains 0s in the eight MSBs. The lower order eight bits contain the data of the register currently being addressed. This function provides register status information for the host.

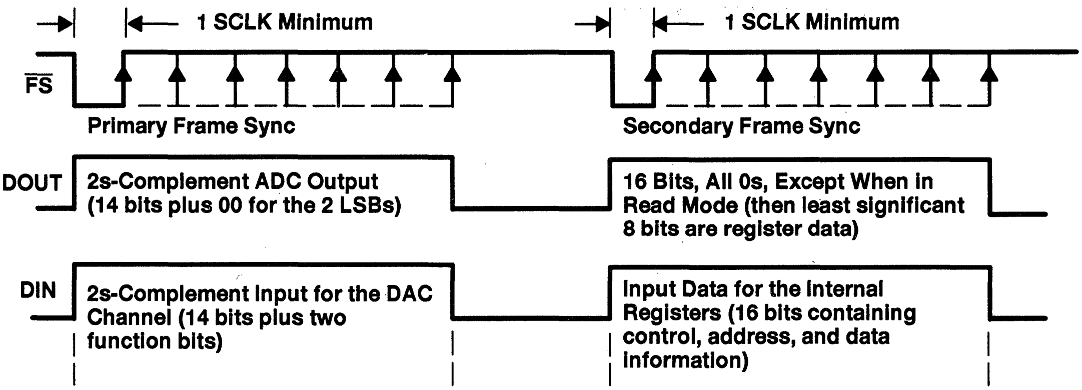


† The time between the primary and secondary frame sync is the time equal to FCLK period multiplied by the B-register contents. The time interval is rounded to the nearest shift clock. The secondary frame-sync signal goes from high to low on the next shift clock low-to-high transition after (B register/2) filter clock periods.

Figure 2–2. Master and Stand-Alone Functional Sequence

2.16.2 Slave- and Codec-Mode Word Sequence and Information Content During Primary and Secondary Communications

For the slave and codec modes, the sequence is basically the same as the stand-alone and master modes with the exception that the frame sync and the shift clock are generated and controlled externally as shown in Figure 2–3. For the codec mode, the frame-sync pulse width needs to be a minimum of one shift clock long. The timing relationship between the frame sync and shift clock is shown in the timing diagrams. Phase shifting is usually not required in the slave or codec mode because the frame-sync timing can be adjusted externally if required.



NOTE: The time between the primary and secondary frame syncs is determined by the application; however, enough time must be provided so that the host can execute the required number of software instructions in the time between the end of the primary data transfer (rising edge of the primary frame-sync interval) and the falling edge of the secondary frame sync (start of secondary communications).

Figure 2–3. Slave and Codec Functional Sequence

2.17 Request for Secondary Serial Communication and Phase Shift

The following paragraphs describe a request for secondary serial communication and phase shift using hardware control inputs FC1 and FC0, primary data bits D01 and D00, and secondary data bits DS15 and DS14.

2.17.1 Initiating a Request

Combinations of FC1 and FC0 input conditions, bits D01 and D00 in the primary serial data word, FC1 and FC0, and bits DS15 and DS14 in the secondary serial data word can be used to initiate a secondary serial communication or request a phase shift according to the following rules (see Table 2–3).

1. Primary word phase shifts can be requested by either the hardware or software if the other set of signals are 11 or 00. If both hardware and software request phase shifts, the software request is performed.
2. Secondary words can be requested by either the software or hardware at the same time that the other set of signals is requesting a phase shift.
3. Hardware inputs FC1 and FC0 are ignored during the secondary word unless DS15 and DS14 are 11. If DS15 and DS14 are 01 or 10, the corresponding phase shift is performed. If DS15 and DS14 are 00, no phase shift is performed even if the hardware requests a phase shift.

2.17.2 Normal Combinations of Control

The normal combinations of control are as follows:

1. Use D01 and D00 and DS15 and DS14 to request phase shifts and secondary words by holding FC1 and FC0 to 00
2. Use FC1 and FC0 exclusively to request phase shifts and secondary words by holding D01 and D00 to 00 and DS15 and DS14 to 11
3. Use D01 and D00 only to request secondary words and FC1 and FC0 to perform phase shifts once per period by holding DS15 and DS14 to 00

2.17.3 Additional Control Options

Additional control options are unusual and rarely needed or used; however, they are as follows:

1. Use D01 and D00 only to request secondary words and FC1 and FC0 to perform phase shifts twice per period by holding DS15 and DS14 to 11
2. Use FC1 and FC0 exclusively to request secondary words and D01 and D00 and DS15 and DS14 to perform phase shifts twice per period
3. Use FC1 and FC0 to perform the phase shift after the primary word and DS15 and DS14 to perform a phase shift after the secondary word by holding D01 and D00 to 11

Table 2–3. Software and Hardware Requests for Secondary Serial-Communication and Phase-Shift Truth Table

WITHIN PRIMARY OR SECONDARY DATA WORD	CONTROL BITS		HARDWARE TERMINALS		PHASE-SHIFT ADJUSTMENT (see Section 2.15.1)		SECONDARY REQUEST (see Note 1)
	D01	D00	FC1	FC0	EARLIER	LATER	
Primary	0	0	0	0	0	0	0
	0	0	0	1	0	1	0
	0	0	1	0	1	0	0
	0	0	1	1	0	0	1
	0	1	0	0	0	1	0
	0	1	0	1	0	1	0
	0	1	1	0	0	1	0
	0	1	1	1	0	1	1
	1	0	0	0	1	0	0
	1	0	0	1	1	0	0
	1	0	1	0	1	0	0
	1	0	1	1	1	0	1
	1	1	0	0	0	0	1
	1	1	0	1	0	1	1
	1	1	1	0	1	0	1
	1	1	1	1	0	0	1
	DS15	DS14	FC1	FC0	EARLIER	LATER	
Secondary	0	0	0	0	0	0	No request can be made for secondary communication within the secondary word.
	0	0	0	1	0	0	
	0	0	1	0	0	0	
	0	0	1	1	0	0	
	0	1	0	0	0	1	
	0	1	0	1	0	1	
	0	1	1	0	0	1	
	0	1	1	1	0	1	
	1	0	0	0	1	0	
	1	0	0	1	1	0	
	1	0	1	0	1	0	
	1	0	1	1	1	0	
	1	1	0	0	0	0	
	1	1	0	1	0	1	
	1	1	1	0	1	0	
	1	1	1	1	0	0	

NOTE 1: The 0 state indicates that a secondary communication is not being requested. The 1 state indicates that a secondary communication is being requested.

2.18 Primary Serial Communications

Primary serial communications transfer the 14-bit DAC input plus two control bits (D01 and D00) to DIN of the TLC320AC02.They simultaneously transfer the 14-bit ADC conversion result from DOUT to the processor. The two LSBs are set to zero in the ADC result.

2.18.1 Primary Serial Communications Data Format

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
14-bit DAC Conversion Result 2s-Complement Format†														Control Bits	

† Since the supply voltage is single ended, the reference for 2s-complement format is ADC V_{MID}. Voltages above this reference have a 0 as the MSB, and voltages below this reference have a 1 as the MSB.

During primary serial communications, if D01 and D00 are both high in the DAC data word to DIN, a subsequent 16 bits of control information is received by the device at DIN during a secondary serial-communication interval. This secondary serial-communication interval begins at 1/2 the programmed conversion time if the B register data value is even or 1/2 the programmed value minus one FCLK if the B register data value is odd. The time between primary and secondary serial communication is measured from the falling edge of the primary frame sync to the falling edge of the secondary frame sync (see Section 2.19, Secondary Serial Communications for function and format of control words).

2.18.2 Data Format From DOUT During Primary Serial Communications

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
14-Bit ADC Conversion Result 2s-Complement Format D15 is the Sign Bit														D01 = 0 D00 = 0	

2.19 Secondary Serial Communications

2.19.1 Data Format to DIN During Secondary Serial Communications

There are nine 16-bit configuration and control registers numbered from zero to eight. All register data contents are represented in 2s-complement format. The general format of the commands during secondary serial communications is as follows.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits (2 bits)		R/$\overline{W}$ Bit	Register Address (5 bits)					Register Data Value (8 bits)							

All control register words are latched in the register and valid on the 16th falling edge of SCLK.

2.19.2 Control Data-Bit Function in Secondary Serial Communication

2.19.2.1 DS15 and DS14

In the secondary data word, bits DS15 and DS14 perform the same control function as the primary control bits D01 and D00 do in the primary data word.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	Register Address					Register Data							

Hardware terminals FC1 and FC0 are valid inputs when DS15 and DS14 are both high, and they are ignored for all other conditions.

2.19.2.2 DS13 (R/$\overline{W}$ Bit)

Reset and power-up procedures set this bit to a zero, placing the device in the write mode. When this bit is set to one, however, the previous data content of the register being addressed is read out to the host from DOUT as the least significant eight bits of the 16-bit secondary word. The first eight bits remain set to zero. Reading the data out is nondestructive, and the contents of the register remain unchanged.

A. Write Mode (DS13 = 0)

Data In. The data word to DIN has the following general format in the write mode.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		0	Register Address					Register Data							

Data Out. The shift-clock shifts out all zeros as the pattern to the host from DOUT.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

B. Read Mode (DS13 = 1)

Data In. The data word to DIN has the following format to allow a register read. Phase shifts can also be done in the read mode.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		1	Register Address					Ignored							

Data Out. The shift-clock clocks out the data of the register addressed from DOUT in the read mode in the eight LSBs.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0	Register Data							

2.20 Internal Register Format

2.20.1 Pseudo-Register 0 (No-Op Address)

This address represents a no-operation command. No register I/O operation takes place, so the device can receive secondary commands for phase adjustment without reprogramming any register. A read of the no-op is zero. The format of the command word is as follows.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		X	0	0	0	0	0	X	X	X	X	X	X	X	X

2.20.2 Register 1 (A Register)

The following command loads DS07 (MSB) – DS00 into the A register.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	0	0	0	0	1	Register Data							

The data in DS07 – DS00 determines the division of the master clock to produce the internal FCLK.

FCLK frequency = MCLK/(A register contents × 2)

The default value of the A-register data is decimal 18 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	0	1	0

2.20.3 Register 2 (B Register)

The following command loads DS07 (MSB) – DS00 into the B register.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	0	0	0	1	0	Register Data							

The data in DS07 – DS00 controls the division of FCLK to generate the conversion clock.

$$\text{Conversion frequency} = \text{FCLK}/(\text{B register contents})$$

$$= \frac{\text{MCLK}}{2 \times \text{A register contents} \times \text{B register contents}}$$

The default value of the B-register data is decimal 18 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	1	0	0	1	0

2.20.4 Register 3 (A′ Register)

The following command contains the A′-register address and loads DS07(MSB) – DS00 into the A′ register.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	0	0	0	1	1	Register Data							

The data in DS07 – DS00 is in 2s-complement format and controls the number of master clock periods that the sampling time is shifted.

The default value of the A′-register data is 0 as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

2.20.5 Register 4 (Amplifier Gain-Select Register)

The following command contains the amplifier gain-select register address with selection code for the monitor output (DS05–DS04), analog input (DS03–DS02), and analog output (DS01–DS00) programmable gains.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	0	0	1	0	0	X	X	*	*	*	*	*	*
Monitor output gain = squelch →										0	0				
Monitor output gain = 0 dB →										0	1				
Monitor output gain = −8 dB →										1	0				
Monitor output gain = −18 dB →										1	1				
Analog input gain = squelch →												0	0		
Analog input gain = 0 dB →												0	1		
Analog input gain = 6 dB →												1	0		
Analog input gain = 12 dB →												1	1		
Analog output gain = squelch →														0	0
Analog output gain = 0 dB →														0	1
Analog output gain = −6 dB →														1	0
Analog output gain = −12 dB →														1	1

The default value of the monitor output gain is squelch, which corresponds to data bits DS05 and DS04 equal to 00 (binary).
The default value of the analog input gain is 0 dB, which corresponds to data bits DS03 and DS02 equal to 01 (binary).
The default value of the analog output gain is 0 dB, which corresponds to data bits DS01 and DS00 equal to 01 (binary).

The default data value is shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	1	0	1

2.20.6 Register 5 (Analog Configuration Register)

The following command is used to load the analog configuration register with the individual bit functions described below.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	0	0	1	0	1	X	X	X	X	*	*	*	*
Must be set to 0 →												0			
High-pass filter disabled →													1		
High-pass filter enabled →													0		
Analog loopback enabled →														0	0
Enables IN+ and IN– (disables AUXIN+ and AUXIN–) →														0	1
Enables AUXIN+ and AUXIN– (disables IN+ and IN–) →														1	0
Enable analog input summing →														1	1

The default value of the high-pass-filter enable bit is zero, which places the high-pass filter in the signal path. The default values of DS01 and DS00 are zero and one, which enables IN+ and IN–.

The power-up and reset conditions are as shown below.

DS03	DS02	DS01	DS00
0	0	0	1

In the read mode, eight bits are read but the four LSBs are repeated as the four MSBs.

2.20.7 Register 6 (Digital Configuration Register)

The following command is used to load the digital configuration register with the individual bit functions described below.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	0	0	1	1	0	X	X	*	*	*	*	*	*
ADC and DAC conversion free run → Inactive →										1 0					
$\overline{FSD}$ output disable → Enable →											1 0				
16-Bit mode, ignore primary LSBs → Normal operation →												1 0			
Force secondary communications → Normal operation →													1 0		
Software reset → (upon reset, this bit is automatically reset to 0) Inactive reset →														1 0	
Software power-down active (automatically reset to 0 after $\overline{PWR\ DWN}$ is cycled high to low and back to high) → Power-down function external (uses $\overline{PWR\ DWN}$) →															1 0

The default value of DS07–DS00 is zero, as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

2.20.8 Register 7 (Frame-Sync Delay Register)

The following command contains the frame-sync delay (FSD) register address and loads DS07 (MSB)–DS00 into the FSD register. The data byte (DS01–DS00) determines the number of SCLKs between $\overline{FS}$ and the delayed frame-sync signal, $\overline{FSD}$. The minimum data value for this register is decimal 18.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	0	0	1	1	1	Register Data							

The default value of DS07 – DS00 is zero, as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	0

When using a slave device, register 7 must be the last register programmed.

2.20.9 Register 8 (Frame-Sync Number Register)

The following command contains the frame-sync number (FSN) register address and loads DS07 (MSB) – DS00 into the FSN register. The data byte determines the number of frame-sync signals generated by the TLC320AC02.

DS15	DS14	DS13	DS12	DS11	DS10	DS09	DS08	DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
Control Bits		R/$\overline{W}$	0	1	0	0	0	Register Data							

The default value of DS07 – DS00 is one, as shown below.

DS07	DS06	DS05	DS04	DS03	DS02	DS01	DS00
0	0	0	0	0	0	0	1

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, DGTL V_{DD} (see Notes 1 and 2) .... −0.3 V to 6.5 V
Supply voltage range, DAC V_{DD} (see Notes 1 and 2) .... −0.3 V to 6.5 V
Supply voltage range, ADC V_{DD} (see Notes 1 and 2) .... −0.3 V to 6.5 V
Differential supply voltage range, DGTL V_{DD} to DAC V_{DD} .... −0.3 V to 6.5 V
Differential supply voltage range, all positive supply voltages to
ADC GND, DAC GND, DGTL GND, SUBS .... −0.3 V to 6.5 V
Output voltage range, DOUT .... −0.3 V to DGTL V_{DD} + 0.3 V
Input voltage range, DIN .... −0.3 V to DGTL V_{DD} + 0.3 V
Ground voltage range, ADC GND, DAC GND,
DGTL GND, SUBS .... −0.3 V to DGTL V_{DD} + 0.3 V
Operating free-air temperature range: TLC320AC02C .... 0°C to 70°C
TLC320AC02I .... −40°C to 85°C
Storage temperature range .... −40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{DD}	Positive supply voltage		4.5	5	5.5	V
	Steady-state differential voltage between any two supplies				0.1	V
V_{IH}	High-level digital input voltage		2.2			V
V_{IL}	Low-level digital input voltage				0.8	V
I_O	Load current from ADC V_{MID} and DAC				100	µA
	Conversion time for the ADC and DAC channels		10 FCLK periods			
f_{MCLK}	Master clock frequency			10.368	15	MHz
$V_{ID(PP)}$	Analog input voltage (differential, peak to peak)			6		V
R_L	Differential output load resistance		600			Ω
R_L	Single-ended to buffered DAC V_{MID} voltage load resistance		300			Ω
T_A	Operating free-air temperature	TLC320AC02C	0		70	°C
T_A	Operating free-air temperature	TLC320AC02I	−40		85	°C

NOTES: 1. Voltage values for DGTL V_{DD} are with respect to DGTL GND, voltage values for DAC V_{DD} are with respect to DAC GND, and voltage values for ADC V_{DD} are with respect to ADC GND. For the subsequent electrical, operating, and timing specifications, the symbol V_{DD} is used to denote all positive supplies. DAC GND, ADC GND, DGTL GND, and SUBS are at 0 V unless otherwise specified.

2. To avoid possible damage to these CMOS devices and associated operating parameters, the sequence below should be followed when applying power:
   (1) Connect SUBS, DGTL GND, ADC GND, and DAC GND to ground.
   (2) Connect voltages ADC V_{DD}, and DAC V_{DD}.
   (3) Connect voltage DGTL V_{DD}.
   (4) Connect the input signals.
   When removing power, follow the steps above in reverse order.

3.3 Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, MCLK = 5.184 MHz, V_{DD} = 5 V, Outputs Unloaded, Total Device

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{DD}	Supply current	$\overline{\text{PWR DWN}}$ = 1 and clock signals present		20	22	mA
		$\overline{\text{PWR DWN}}$ = 0 after 500 µs and clock signals present		1	2	mA
P_D	Power dissipation	$\overline{\text{PWR DWN}}$ = 1 and clock signals present		100		mW
		$\overline{\text{PWR DWN}}$ = 0 after 500 µs and clock signals present		5		mW
		Software power down, (bit D00, register 6 set to 1)		15	20	mW
ADC V_{MID}		No load	ADC $V_{DD}/2$ −0.1		ADC $V_{DD}/2$ +0.1	V
DAC V_{MID}		No load	DAC $V_{DD}/2$ −0.1		DAC $V_{DD}/2$ +0.1	V

3.4 Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, V_{DD} = 5 V, Digital I/O Terminals (DIN, DOUT, EOC, FC0, FC1, $\overline{\text{FS}}$, $\overline{\text{FSD}}$, MCLK, M/$\overline{\text{S}}$, SCLK)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −1.6 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
I_{IH}	High-level input current, any digital input	V_I = 2.2 V to DGTL V_{DD}			10	µA
I_{IL}	Low-level input current, any digital input	V_I = 0 V to 0.8 V			10	µA
C_i	Input capacitance			5		pF
C_o	Output capacitance			5		pF

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

3.5 Electrical Characteristics Over Recommended Range of Operating Free-Air Temperature, V_{DD} = 5 V, ADC and DAC Channels

3.5.1 ADC Channel Filter Transfer Function, FCLK = 144 kHz, f_s = 8 kHz

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Gain relative to gain at f_i = 1020 Hz (see Note 3)	f_i = 50 Hz		−2	dB
	f_i = 200 Hz	−1.8	−0.2	
	f_i = 300 Hz to 3 kHz	−0.2	0.2	
	f_i = 3.3 kHz	−0.35	0.03	
	f_i = 3.4 kHz	−1	−0.1	
	f_i = 4 kHz		−14	
	$f_i \geq$ 4.6 kHz		−32	

NOTE 3: The differential analog input signals are sine waves at 6 V peak to peak. The reference gain is at 1020 Hz.

3.5.2 ADC Channel Input, V_{DD} = 5 V, Input Amplifier Gain = 0 dB (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{I(PP)}$	Peak-to-peak input voltage (see Note 4)	Single ended		3		V
		Differential		6		V
	ADC converter offset error	Band-pass filter selected		10	30	mV
CMRR	Common-mode rejection ratio at IN+, IN–, AUX IN+, AUX IN– (see Note 5)			55		dB
r_i	Input resistance at IN+, IN–, AUX IN+, AUX IN–			100		kΩ
	Squelch	DS03, DS02 = 0 in register 4		60		dB

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTES: 4. The differential range corresponds to the full-scale digital output.

5. Common-mode rejection ratio is the ratio of the ADC converter offset error with no signal and the ADC converter offset error with a common-mode nonzero signal applied to either IN+ and IN– together or AUX IN+ and AUX IN– together.

3.5.3 ADC Channel Signal-to-Distortion Ratio, V_{DD} = 5 V, f_s = 8 kHz (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	A_V = 0 dB		A_V = 6 dB		A_V = 12 dB		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
ADC channel signal-to-distortion ratio (see Note 6)	V_I = –6 dB to –1 dB	64		—		—		dB
	V_I = –12 dB to –6 dB	59		64		—		
	V_I = –18 dB to –12 dB	56		59		64		
	V_I = –24 dB to –18 dB	50		56		59		
	V_I = –30 dB to –24 dB	44		50		56		
	V_I = –36 dB to –30 dB	38		44		50		
	V_I = –42 dB to –36 dB	32		38		44		
	V_I = –48 dB to –42 dB	26		32		38		

NOTE 6: The analog input test signal is a 1020-Hz sine wave with 0 dB ≙ 6 V peak to peak as the reference level for the analog input signal.

3.5.4 DAC Channel Filter Transfer Function, FCLK = 144 kHz, f_s = 9.6 kHz, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Gain relative to gain at f_i = 1020 Hz (see Note 7)	f_i < 200 Hz		0.15	dB
	f_i = 200 Hz	–0.5	0.2	
	f_i = 300 Hz to 3 kHz	–0.2	0.2	
	f_i = 3.3 kHz	–0.35	0.03	
	f_i = 3.4 kHz	–1	–0.1	
	f_i = 4 kHz		–14	
	f_i ≥ 4.6 kHz		–32	

NOTE 7: The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak.

3.5.5 DAC Channel Signal-to-Distortion Ratio, V_{DD} = 5 V, f_s = 8 kHz (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	A_V = 0 dB		A_V = −6 dB		A_V = −12 dB		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
DAC channel signal-to distortion ratio (see Note 8)	V_O = −6 dB to 0 dB	64		—		—		dB
	V_O = −12 dB to −6 dB	59		64		—		
	V_O = −18 dB to −12 dB	56		59		64		
	V_O = −24 dB to −18 dB	50		56		59		
	V_O = −30 dB to −24 dB	44		50		56		
	V_O = −36 dB to −30 dB	38		44		50		
	V_O = −42 dB to −36 dB	32		38		44		
	V_O = −48 dB to −42 dB	26		32		38		

NOTE 8: The input signal, V_I, is the digital equivalent of a 1020-Hz sine wave (full-scale analog output at full-scale digital input = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT−.

3.5.6 System Distortion, V_{DD} = 5 V, f_s = 8 kHz, FCLK = 144 kHz (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
ADC channel attenuation	Second harmonic	Single-ended input (see Note 9)		82		dB
		Differential input (see Note 9)	64	82		
	Third harmonic and higher harmonics	Single-ended input (see Note 9)		77		
		Differential input (see Note 9)	64	77		
DAC channel attenuation	Second harmonic	Single-ended output (buffered DAC V_{MID}) (see Note 10)		82		
		Differential output (see Note 10)	64	82		
	Third harmonic and higher harmonics	Single-ended output (see Note 10)		77		
		Differential output (see Note 10)	64	77		

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTES: 9. The input signal is a 1020-Hz sine wave for the ADC channel. Harmonic distortion is defined for an input level of −1 dB.

10. The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT−. Harmonic distortion is specified for a signal input level of 0 dB.

3.5.7 Noise, Low-Pass and Band-Pass Switched-Capacitor Filters Included, V_{DD} = 5 V (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
ADC idle channel noise		Inputs tied to ADC V_{MID} f_s = 8 kHz, FCLK = 144 kHz, (see Note 11)		180	300	µVrms
DAC idle channel noise	Broad-band noise	DIN INPUT = 00000000000000 f_s = 8 kHz, FCLK = 144 kHz, (see Note 12)		180	300	
	Noise (0 to 7.2 kHz)			180	300	
	Noise (0 to 3.6 kHz)			180	300	

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTES: 11. The ADC channel noise is calculated by taking the RMS value of the digital output codes of the ADC channel and converting to microvolts.

12. The DAC channel noise is measured differentially from OUT+ to OUT− across 600 Ω.

3.5.8 Absolute Gain Error, V_{DD} = 5 V, f_s = 8 kHz (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
ADC channel absolute gain error (see Note 13)	−1-dB input signal	T_A = −40 to 85°C		±1	dB
DAC channel absolute gain error (see Note 14)	0-dB input signal, R_L = 600 Ω	T_A = −40 to 85°C		±1	

NOTES: 13. ADC absolute gain error is the variation in gain from the ideal gain over the specified input signal levels. The gain is measured with a −1-dB, 1020-Hz sine wave. The −1-dB input signal allows for any positive gain or offset error that may affect gain measurements at or close to 0-dB input signal levels.

14. The DAC input signal is the digital equivalent of a 1020-Hz sine wave (full-scale analog output at digital full-scale input = 0 dB). The nominal differential DAC channel output voltage with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT−.

3.5.9 Relative Gain and Dynamic Range, V_{DD} = 5 V, f_s = 8 kHz (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
ADC channel relative gain tracking error (see Note 15)	−48-dB to −1-dB input signal range		±0.2	dB
DAC channel relative gain tracking error (see Note 16)	−48-dB to 0-dB input signal range $R_{L(diff)}$ = 600 Ω		±0.2	

NOTES: 15. ADC gain tracking is the ratio of the measured gain at one ADC channel input level to the gain measured at any other input level. The ADC channel input is a −1-dB 1020-Hz sine wave input signal. A −1-dB input signal allows for any positive gain or offset error that may affect gain measurements at or close to 0-dB ADC input signal levels.

16. DAC gain tracking is the ratio of the measured gain at one DAC channel digital input level to the gain measured at any other input level. The DAC channel input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output voltage with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT−.

3.5.10 Power-Supply Rejection, V_{DD} = 5 V (Unless Otherwise Noted)(see Note 17)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
ADC V_{DD}	Supply-voltage rejection ratio, ADC channel	f_i = 0 to 30 kHz		50		dB
		f_i = 30 to 50 kHz		55		
DAC V_{DD}	Supply-voltage rejection ratio, DAC channel	f_i = 0 to 30 kHz		40		
		f_i = 30 to 50 kHz		45		
DGTL V_{DD}	Supply-voltage rejection ratio, ADC channel	f_i = 0 to 30 kHz		50		
		f_i = 30 to 50 kHz		55		
DGTL V_{DD}	Supply-voltage rejection ratio, DAC channel	Single ended, f_i = 0 to 30 kHz		40		
		f_i = 30 to 50 kHz		45		
		Differential, f_i = 0 to 30 kHz		40		
		f_i = 30 to 50 kHz		45		

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTE 17: Power-supply rejection measurements are made with both the ADC and the DAC channels idle and a 200-mV peak-to-peak signal applied to the appropriate supply.

3.5.11 Crosstalk Attenuation, V_{DD} = 5 V (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
ADC channel crosstalk attenuation	DAC channel idle with DIN = 00000000000000, ADC input = 0 dB, 1020-Hz sine wave, Gain = 0 dB (see Note 18)		80		dB
DAC channel crosstalk attenuation	ADC channel idle with INP, INM, AUX IN+, and AUX IN− at ADC V_{MID}		80		dB
	DAC channel input = digital equivalent of a 1020-Hz sine wave (see Note 19)		80		

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTES: 18. The test signal is a 1020-Hz sine wave with a 0 dB = 6-V peak-to-peak reference level for the analog input signal.

19. The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT−.

3.5.12 Monitor Output Characteristics, V_{DD} = 5 V (Unless Otherwise Noted) (see Note 20)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{O(PP)}$	Peak-to-peak ac output voltage	Quiescent level = ADC V_{MID} Z_L = 10 kΩ and 60 pF	1.3	1.5		V
V_{OO}	Output offset voltage	No load, single ended relative to ADC V_{MID}		5	10	mV
r_o	DC output resistance			50		Ω
V_{OC}	Output common-mode voltage	No load	0.4 ADC V_{DD}	0.5 ADC V_{DD}	0.6 ADC V_{DD}	V
A_V	Voltage gain (see Note 21)	Gain = 0 dB	−0.2	0	0.2	dB
		Gain 2 = −8 dB	−8.2	−8	−7.8	
		Gain 3 = −18 dB	−18.4	−18	−17.6	
		Squelch (see Note 22)			−60	

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTES: 20. All monitor output tests are performed with a 10-kΩ load resistance.

21. Monitor gains are measured with a 1020-Hz, 6-V peak-to-peak sine wave applied differentially between IN+ and IN−. The monitor output gains are nominally 0 dB, −8 dB, and −18 dB relative to its input; however, the output gains are −6 dB relative to IN+ and IN− or AUX IN+ and AUX IN−.

22. Squelch is measured differentially with respect to ADC V_{MID}.

3.6 Timing Requirements and Specifications in Master Mode

3.6.1 Recommended Input Timing Requirements for Master Mode, V_{DD} = 5 V

		MIN	NOM	MAX	UNIT
$t_{r(MCLK)}$	Master clock rise time		5		ns
$t_{f(MCLK)}$	Master clock fall time		5		ns
	Master clock duty cycle	40%		60%	
$t_{w(RESET)}$	$\overline{\text{RESET}}$ pulse duration	1 MCLK			
$t_{su(DIN)}$	DIN setup time before SCLK low (see Figure 4–2)	25			ns
$t_{h(DIN)}$	DIN hold time after SCLK high (see Figure 4–2)			20	ns

3.6.2 Operating Characteristics Over Recommended Range of Operating Free-Air Temperature, V_{DD} = 5 V (Unless Otherwise Noted) (see Note 23)

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{f(SCLK)}$	Shift clock fall time (see Figure 4–2)		13	18	ns
$t_{r(SCLK)}$	Shift clock rise time (see Figure 4–2)		13	18	ns
	Shift clock duty cycle	45%		55%	
$t_{d(CH\text{-}FL)}$	Delay time from SCLK high to $\overline{\text{FSD}}$ low (see Figures 4–2 and 4–4 and Note 24)		5	20	ns
$t_{d(CH\text{-}FH)}$	Delay time from SCLK high to $\overline{\text{FS}}$ high (see Figure 4–2)		5	20	ns
$t_{d(CH\text{-}DOUT)}$	Delay time from SCLK high to DOUT valid (see Figures 4–2 and 4–7)			20	ns
$t_{d(CH\text{-}DOUTZ)}$	Delay time from SCLK↑ to DOUT in high-impedance state (see Figure 4–8)		20		ns
$t_{d(ML\text{-}EL)}$	Delay time from MCLK low to EOC low (see Figure 4–9)		40		ns
$t_{d(ML\text{-}EH)}$	Delay time from MCLK low to EOC high (see Figure 4–9)		40		ns
$t_{f(EL)}$	EOC fall time (see Figure 4–9)		13		ns
$t_{r(EH)}$	EOC rise time (see Figure 4–9)		13		ns
$t_{d(MH\text{-}CH)}$	Delay time from MCLK high to SCLK high			50	ns
$t_{d(MH\text{-}CL)}$	Delay time from MCLK high to SCLK low			50	ns

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

NOTES: 23. All timing specifications are valid with C_L = 20 pF.

24. $\overline{\text{FSD}}$ occurs 1/2 shift-clock cycle ahead of $\overline{\text{FS}}$ when the device is operating in the master mode.

3.7 Timing Requirements and Specifications in Slave Mode and Codec Emulation Mode

3.7.1 Recommended Input Timing Requirements for Slave Mode, V_{DD} = 5 V

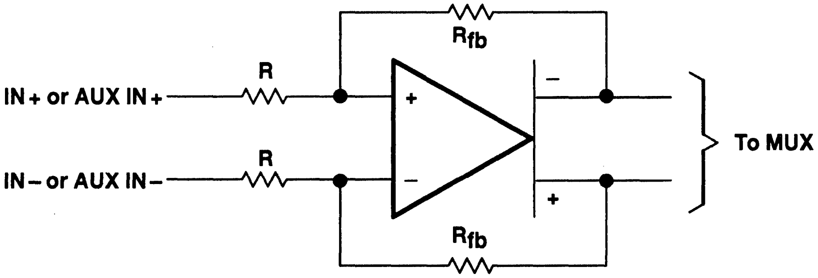
		MIN	NOM	MAX	UNIT
$t_{r(MCLK)}$	Master clock rise time		5		ns
$t_{f(MCLK)}$	Master clock fall time		5		ns
	Master clock duty cycle	40%		60%	
$t_{w(RESET)}$	$\overline{\text{RESET}}$ pulse duration	1 MCLK			
$t_{su(DIN)}$	DIN setup time before SCLK low (see Figure 4–3)	20			ns
$t_{h(DIN)}$	DIN hold time after SCLK high (see Figure 4–3)			20	ns
$t_{su(FL-CH)}$	Setup time from $\overline{\text{FS}}$ low to SCLK high			±SCLK/4	ns

3.7.2 Operating Characteristics Over Recommended Range of Operating Free-Air Temperature, V_{DD} = 5 V (Unless Otherwise Noted) (see Note 23)

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock cycle time (see Figure 4–3)	125			ns
$t_{f(SCLK)}$	Shift clock fall time (see Figure 4–3)			18	ns
$t_{r(SCLK)}$	Shift clock rise time (see Figure 4–3)			18	ns
	Shift clock duty cycle	45%		55%	
$t_{d(CH-FDL)}$	Delay time from SCLK high to $\overline{\text{FSD}}$ low (see Figure 4–6)			50	ns
$t_{d(CH-FDH)}$	Delay time from SCLK high to $\overline{\text{FSD}}$ high			40	ns
$t_{d(FL-FDL)}$	Delay time from $\overline{\text{FS}}$ low to $\overline{\text{FSD}}$ low (slave to slave) (see Figure 4–5)			40	ns
$t_{d(CH-DOUT)}$	Delay time from SCLK high to DOUT valid (see Figures 4–3 and 4–7)			40	ns
$t_{d(CH-DOUTZ)}$	Delay time from SCLK↑ to DOUT in high-impedance state (see Figure 4–8)		20		ns
$t_{d(ML-EL)}$	Delay time from MCLK low to EOC low (see Figure 4–9)		40		ns
$t_{d(ML-EH)}$	Delay time from MCLK low to EOC high (see Figure 4–9)		40		ns
$t_{f(EL)}$	EOC fall time (see Figure 4–9)		13		ns
$t_{r(EH)}$	EOC rise time (see Figure 4–9)		13		ns
$t_{d(MH-CH)}$	Delay time from MCLK high to SCLK high			50	ns
$t_{d(MH-CL)}$	Delay time from MCLK high to SCLK low			50	ns

† All typical values are at V_{DD} = 5 V and T_A = 25°C.
NOTE 23: All timing specifications are valid with C_L = 20 pF.

4 Parameter Measurement Information



R_{fb} = R for DS03 = 0 and DS02 = 1
R_{fb} = 2R for DS03 = 1 and DS02 = 0
R_{fb} = 4R for DS03 = 1 and DS02 = 1
R = 100 kΩ nominal

Figure 4–1. IN+ and IN– Gain-Control Circuitry

Table 4–1. Gain Control (Analog Input Signal Required for Full-Scale Bipolar A/D Conversion 2s Complement)†

INPUT CONFIGURATION	CONTROL REGISTER 4		ANALOG INPUT‡	A/D CONVERSION RESULT
	DS03	DS02		
Differential configuration Analog input = IN+ – IN– = AUX IN+ – AUX IN–	0	0	All	Squelch
	0	1	V_{ID} = ±3 V	±Full scale
	1	0	V_{ID} = ±1.5 V	±Full scale
	1	1	V_{ID} = ±0.75 V	±Full scale
Single-ended configuration§ Analog input = IN+ – V_{MID} = AUX IN+ – V_{MID}	0	0	All	Squelch
	0	1	V_I = ±1.5 V	±Half scale
	1	0	V_I = ±1.5 V	±Full scale
	1	1	V_I = ±0.75 V	±Full scale

† V_{DD} = 5 V
‡ V_{ID} = differential input voltage, V_I = input voltage referenced to ADC V_{MID} with IN– or AUX IN– connected to ADC V_{MID}. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.
§ For single-ended inputs, the analog input voltage should not exceed the supply rails. All single-ended inputs should be referenced to the internal reference voltage, ADC V_{MID}, for best common-mode performance.

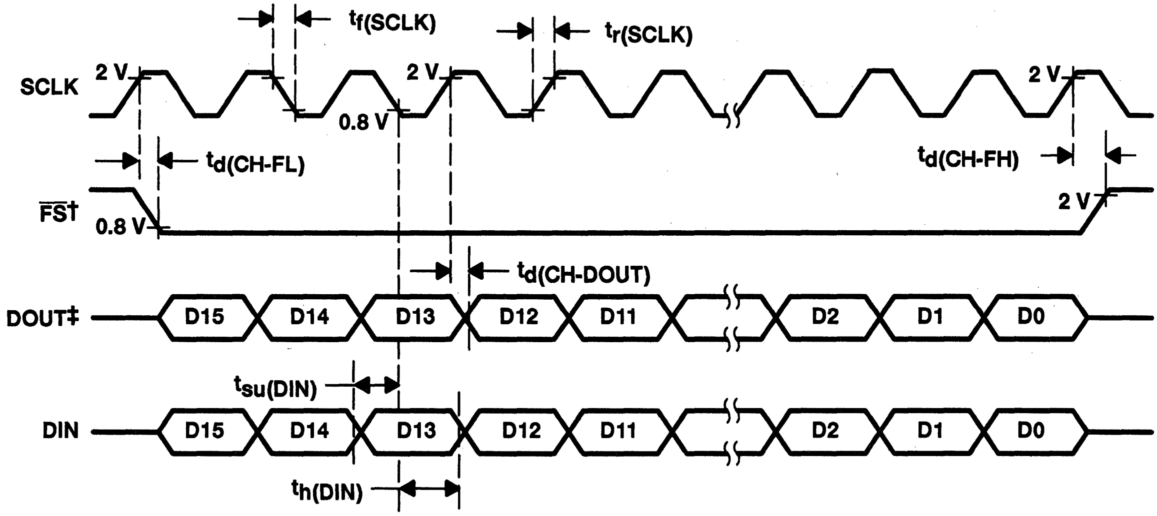


Figure 4–2. AIC Stand-Alone and Master-Mode Timing

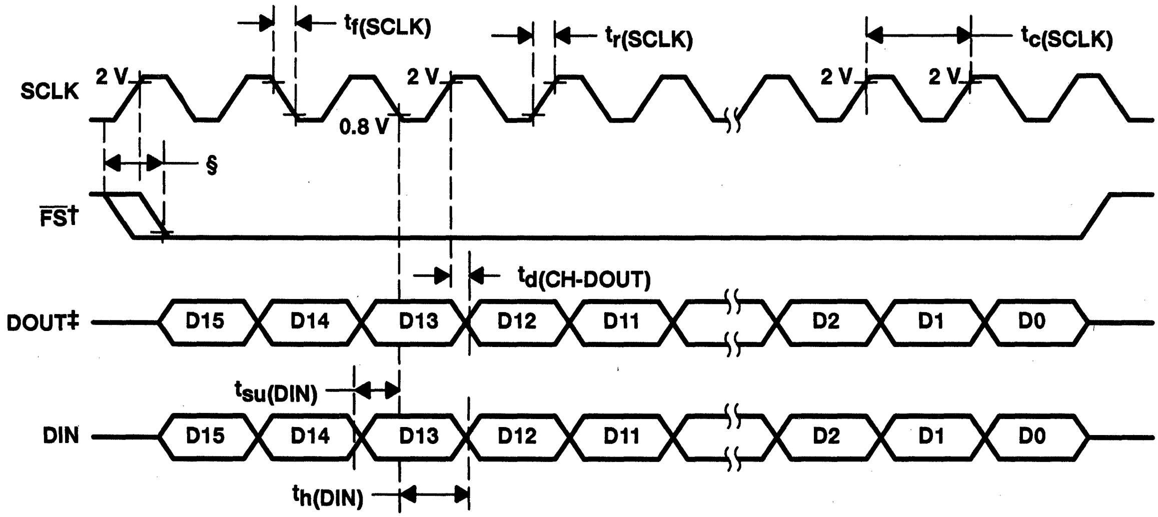
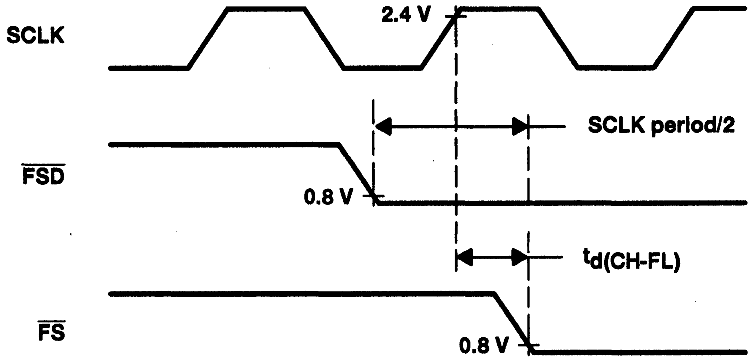


Figure 4–3. AIC Slave and Codec Emulation Mode

† The time between falling edges of two primary $\overline{FS}$ signals is the conversion period.

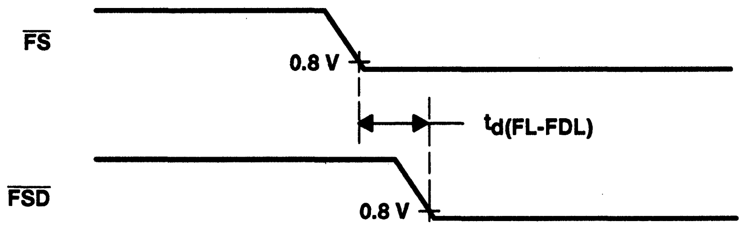
‡ The data on DOUT are shifted out on the rising edge of the shift clock, and the data on DIN are shifted in on the falling edge of the shift clock.

§ The high-to-low transition of $\overline{FS}$ must must occur within ±1/4 of a shift-clock period around the 2-V level of the shift clock.



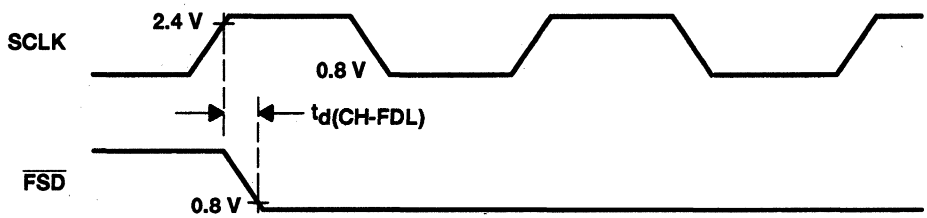
NOTE: Timing shown is for the TLC320AC02 operating as the master or as a stand-alone device.

Figure 4–4. Master or Stand-Alone $\overline{FS}$ and $\overline{FSD}$ Timing



NOTE: Timing shown is for the TLC320AC02 operating in the slave mode ($\overline{FS}$ and SCLK signals generated externally). The programmed data value in the FSD register is 0.

Figure 4–5. Slave $\overline{FS}$ to $\overline{FSD}$ Timing



NOTE: Timing shown is for the TLC320AC02 operating in the slave mode ($\overline{FS}$ and SCLK signals generated externally). There is a data value in the FSD register greater than 18 decimal.

Figure 4–6. Slave SCLK to $\overline{FSD}$ Timing

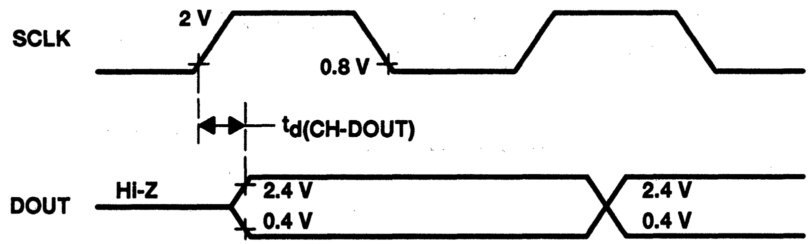


Figure 4–7. DOUT Enable Timing from Hi-Z

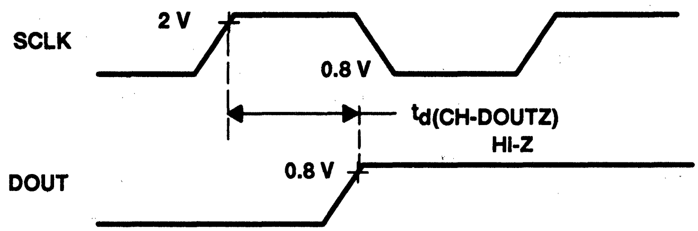


Figure 4–8. DOUT Delay Timing to Hi-Z

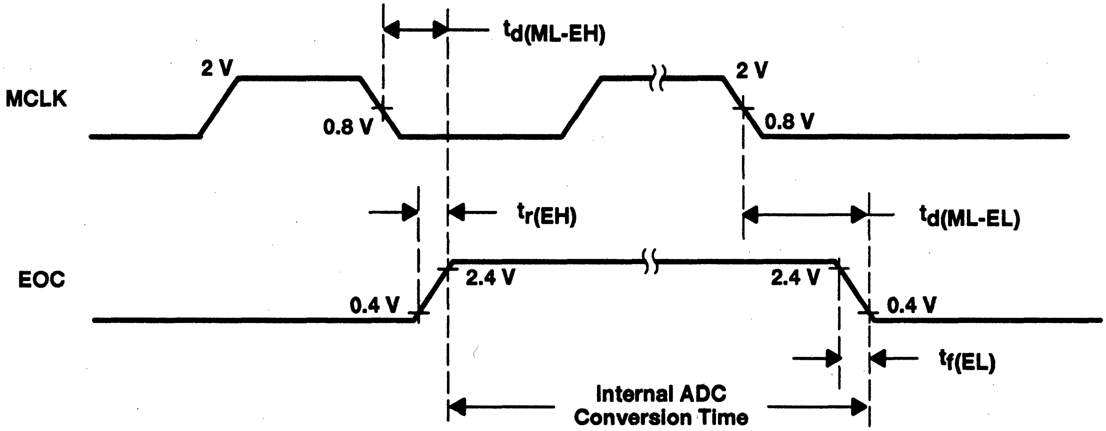
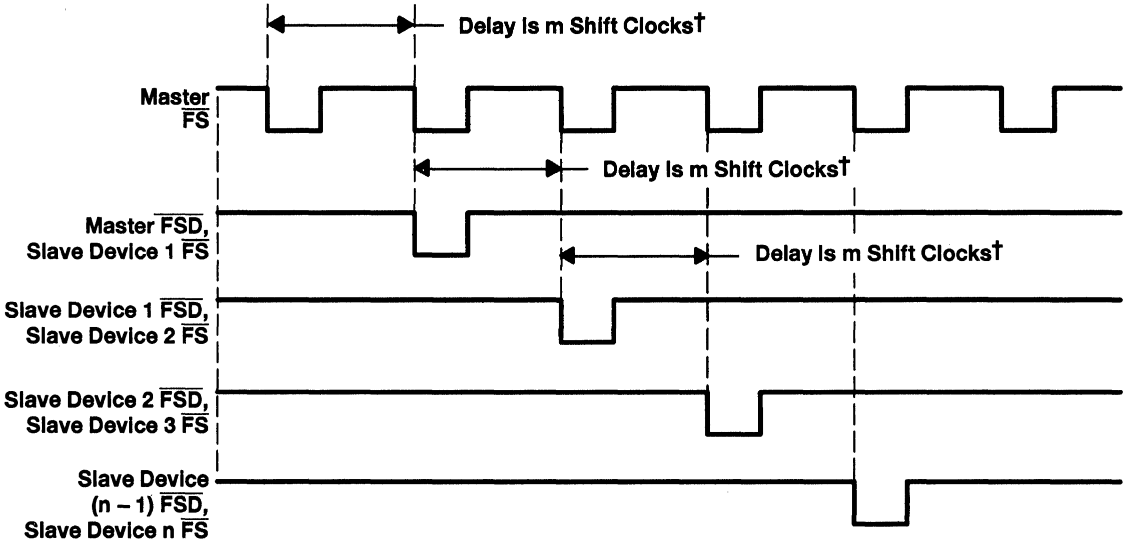


Figure 4–9. EOC Frame Timing



† The delay time from any $\overline{FS}$ signals to the corresponding $\overline{FSD}$ signals is m shift clocks with the value of m being the numerical value of the data programmed into the FSD register. In the master mode with slaves, the same data word is used to program the master and all slave devices; therefore, master to slave 1, slave 1 to slave 2, slave 2 to slave 3, etc., have the same delay time.

Figure 4–10. Master-Slave Frame-Sync Timing After a Delay Has Been Programmed Into the FSD Registers

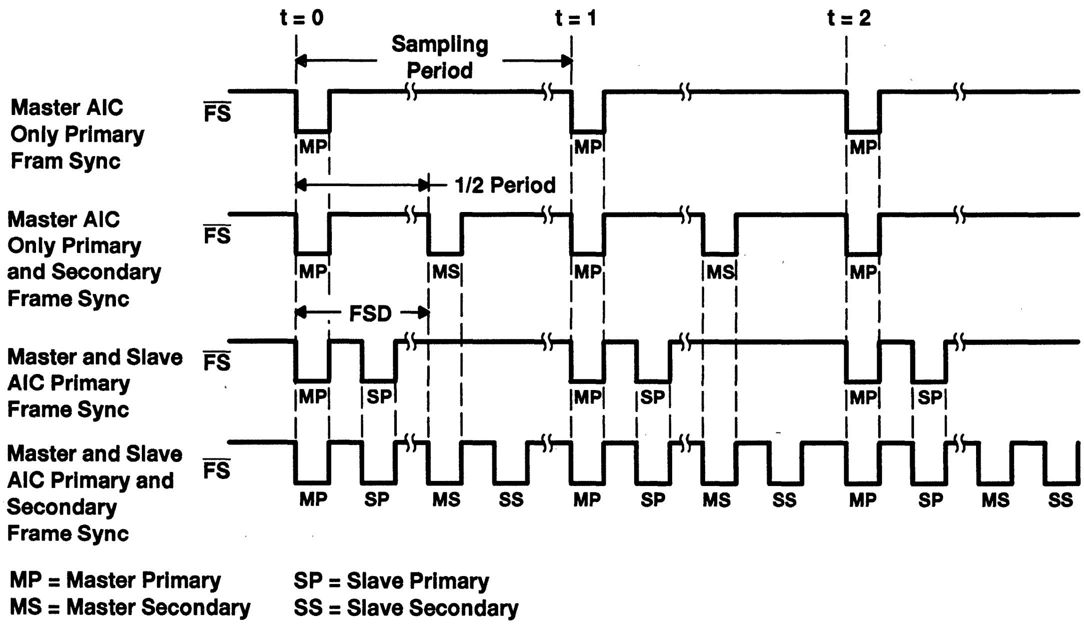


Figure 4–11. Master and Slave Frame-Sync Sequence with One Slave

5 Typical Characteristics

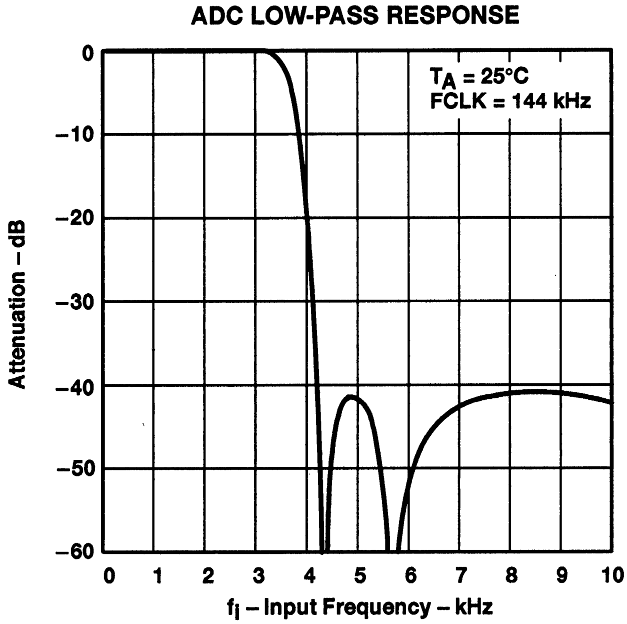


Figure 5–1

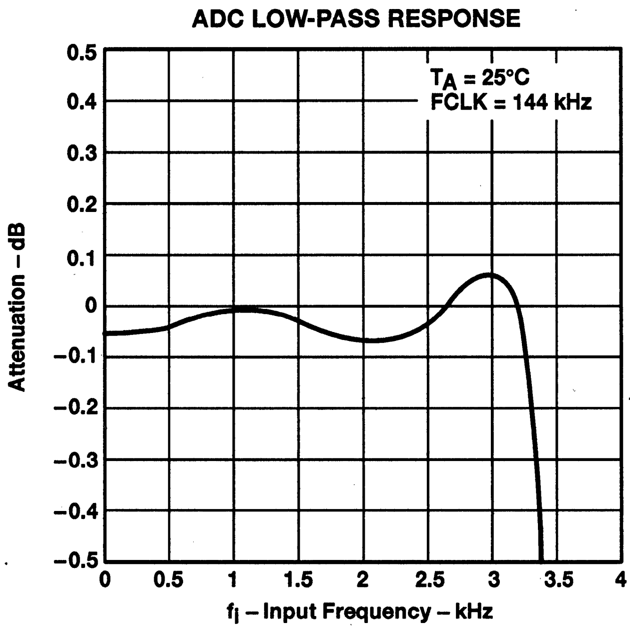


Figure 5–2

$$\text{NOTE : Absolute Frequency (kHz)} = \frac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$$

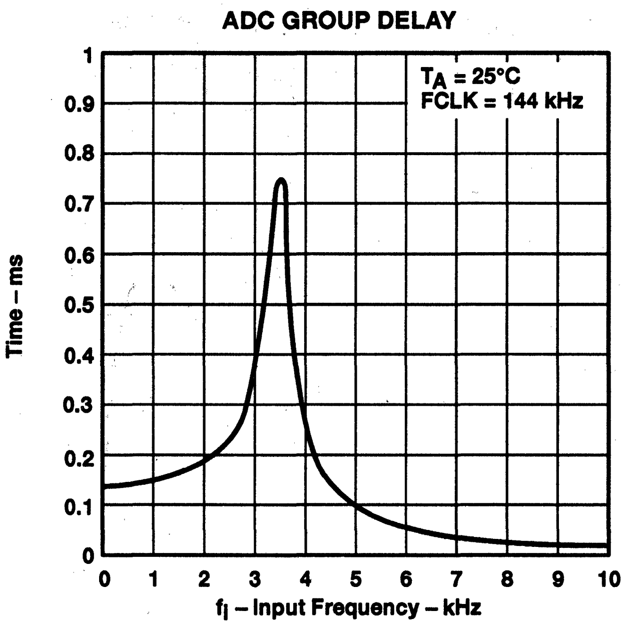


Figure 5–3

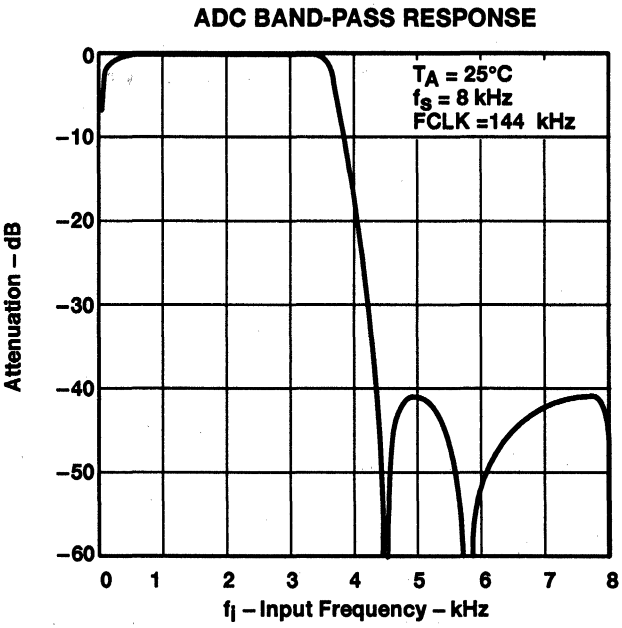


Figure 5–4

NOTE : $\text{Absolute Frequency (kHz)} = \dfrac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

ADC BAND-PASS RESPONSE

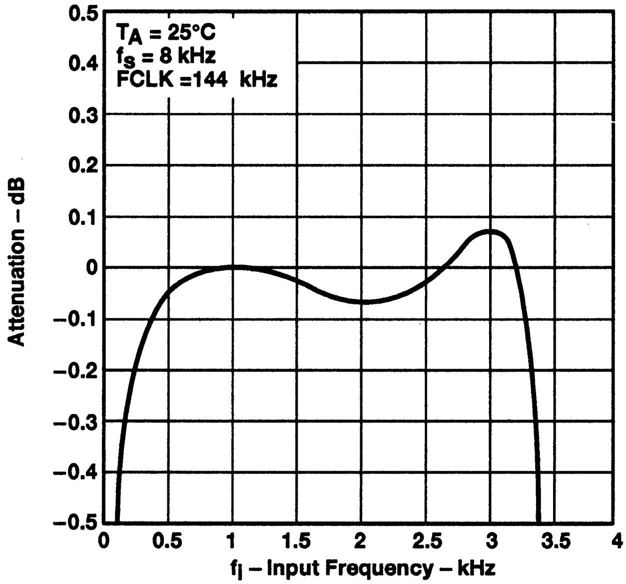


Figure 5–5

ADC HIGH-PASS RESPONSE

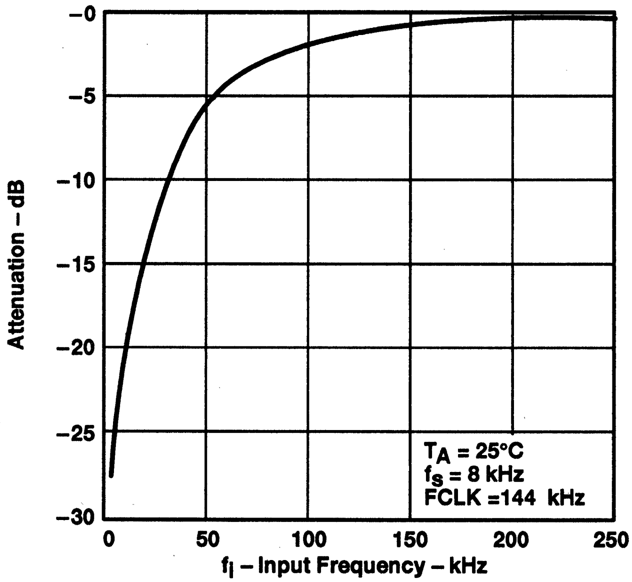


Figure 5–6

NOTE : $\text{Absolute Frequency (kHz)} = \dfrac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

ADC BAND-PASS GROUP DELAY

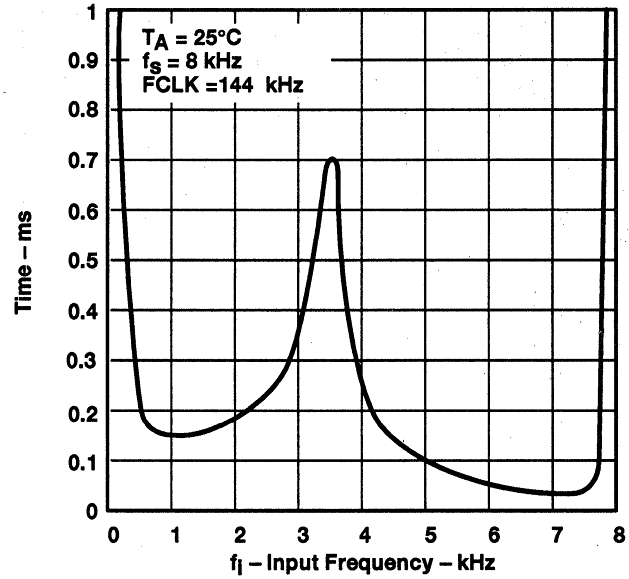


Figure 5–7

DAC LOW-PASS RESPONSE

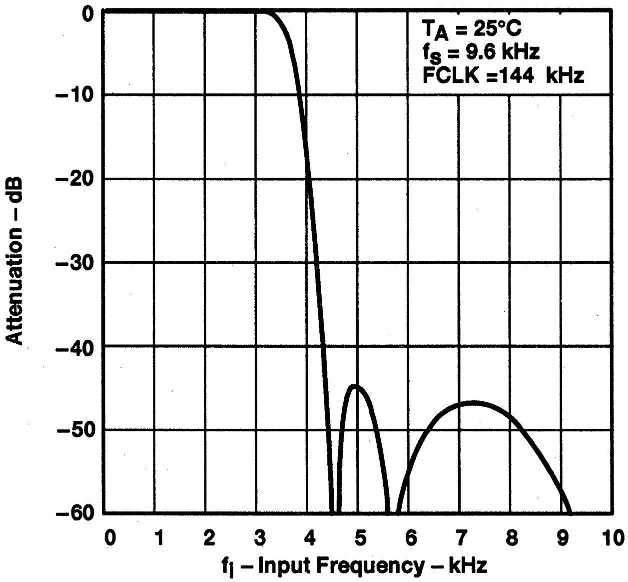


Figure 5–8

NOTE : $\text{Absolute Frequency (kHz)} = \dfrac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

DAC LOW-PASS RESPONSE

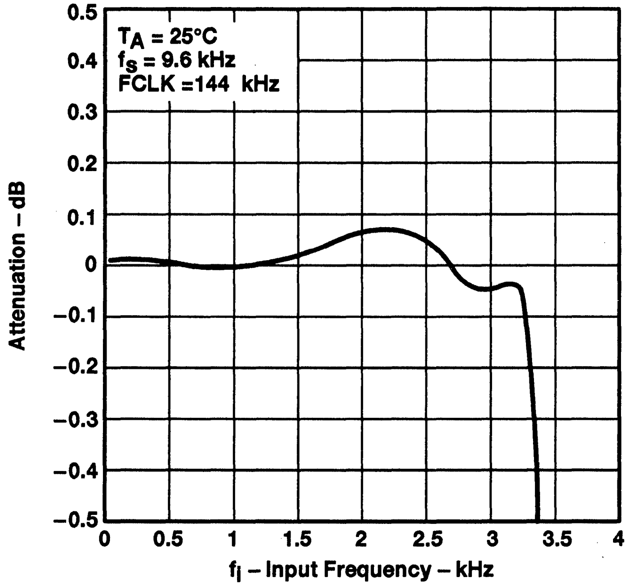


Figure 5–9

DAC LOW-PASS GROUP DELAY

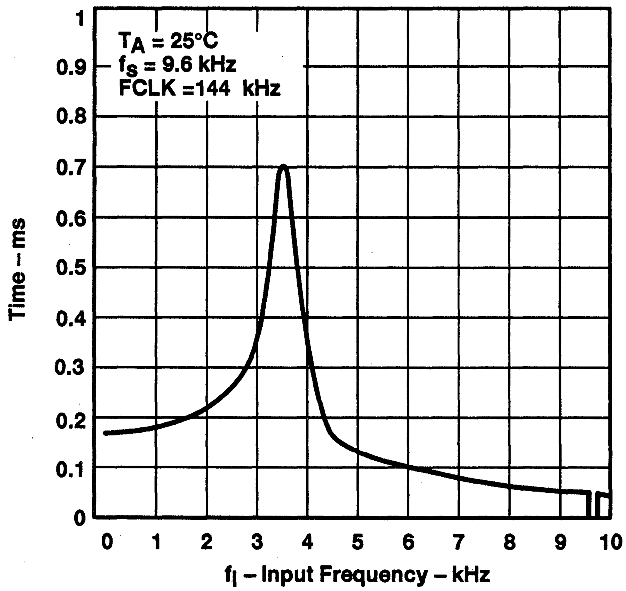


Figure 5–10

NOTE : $\text{Absolute Frequency (kHz)} = \dfrac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{144}$

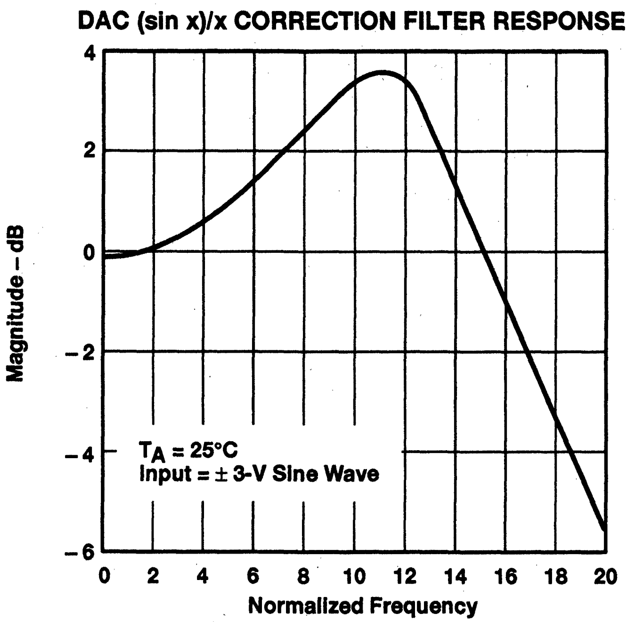


Figure 5–11

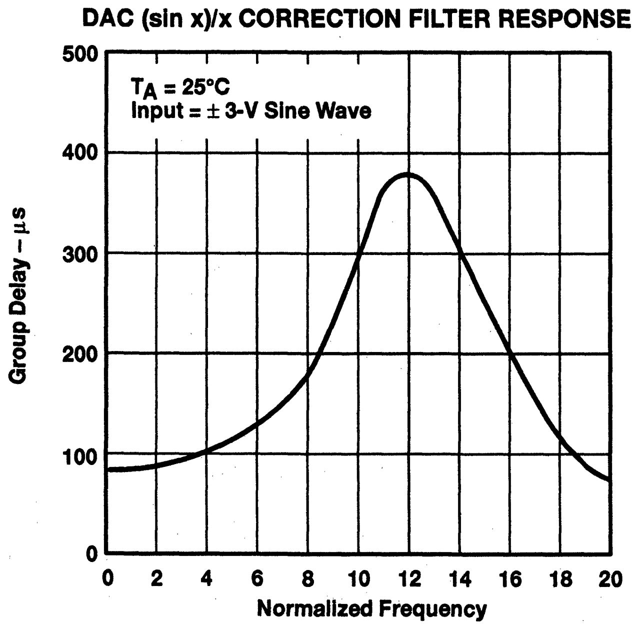


Figure 5–12

NOTE : $\text{Absolute Frequency (kHz)} = \dfrac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{288}$

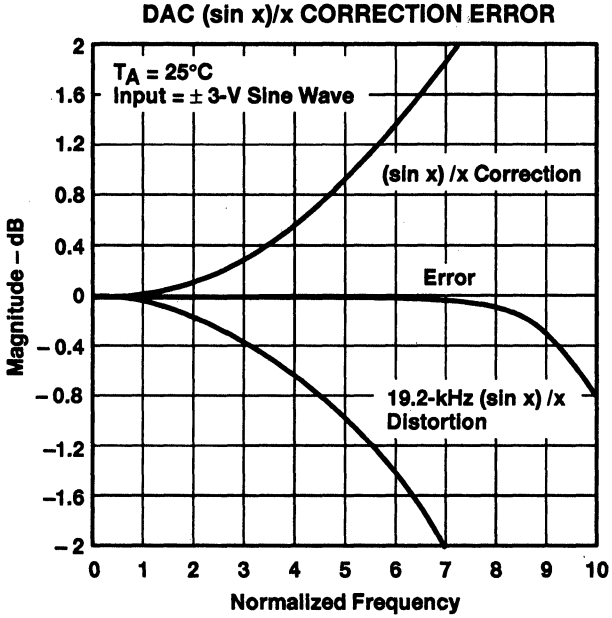


Figure 5–13

NOTE : $\text{Absolute Frequency (kHz)} = \dfrac{\text{Normalized Frequency} \times \text{FCLK (kHz)}}{288}$

6 Application Information

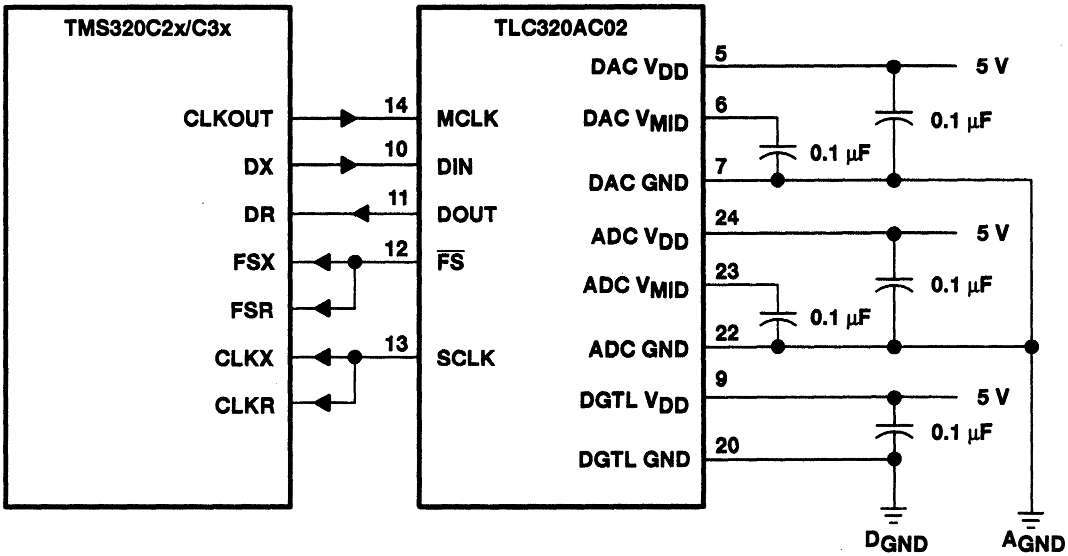


Figure 6–1. Stand-Alone Mode (to DSP Interface)

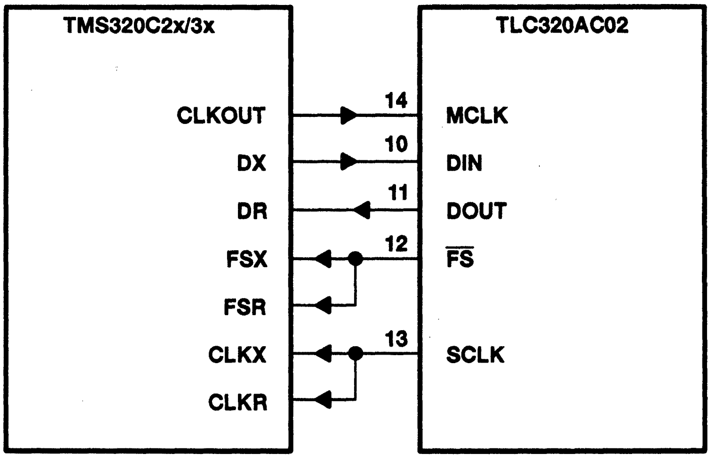
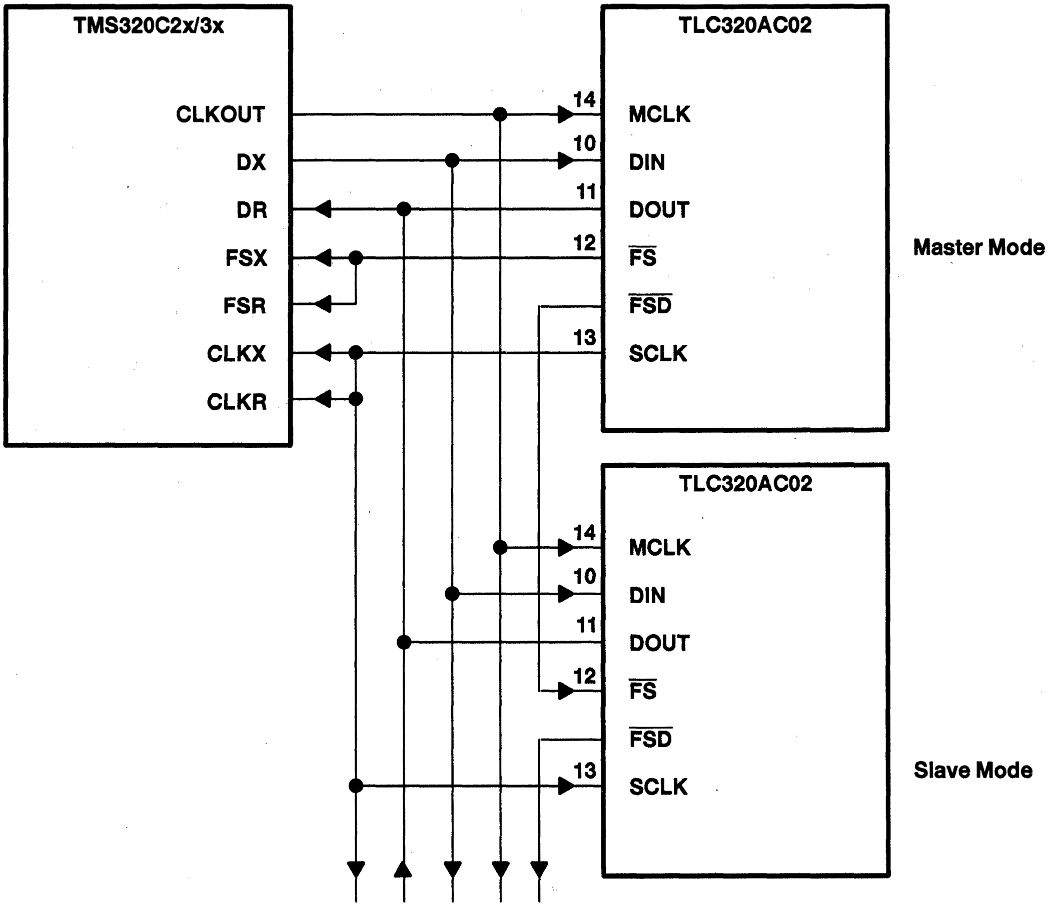


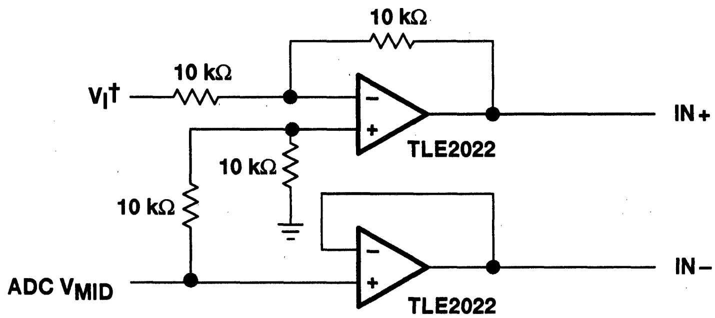
Figure 6–2. Codec Mode (to DSP Interface)

Terminal numbers shown are for the FN package.



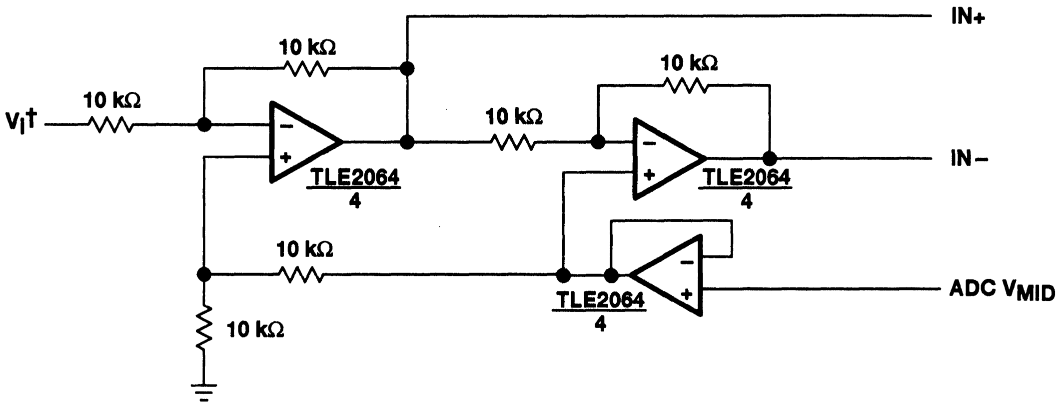
Terminal numbers shown are for the FN package.

Figure 6–3. Master With Slave (to DSP Interface)



† The V_I source must be capable of sinking a current equal to [ADC V_{MID} + $|V_I|(max)$]/10 kΩ.

Figure 6–4. Single-Ended Input (Ground Referenced)



† The V_I source must be capable of sinking a current equal to [(ADC V_{MID}/2) + $|V_I|$(max)]/10 kΩ.

Figure 6–5. Single-Ended to Differential Input (Ground Referenced)

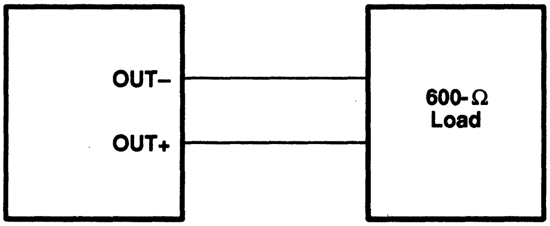
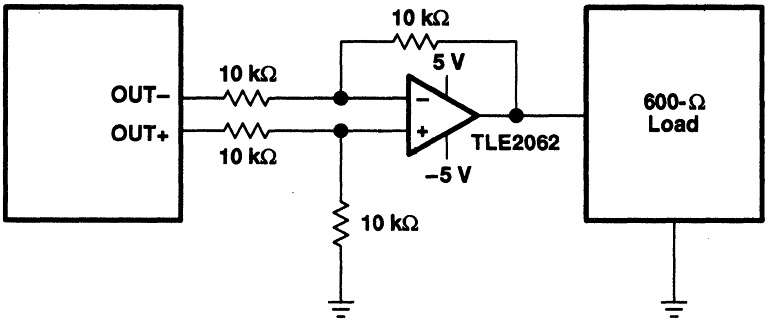


Figure 6–6. Differential Load



NOTE: When a signal is changed from a single supply with a nonzero reference system to a grounded load, the operational amplifier must be powered from plus and minus supplies or the load must be capacitively coupled.

Figure 6–7. Differential Output Drive (Ground Referenced)

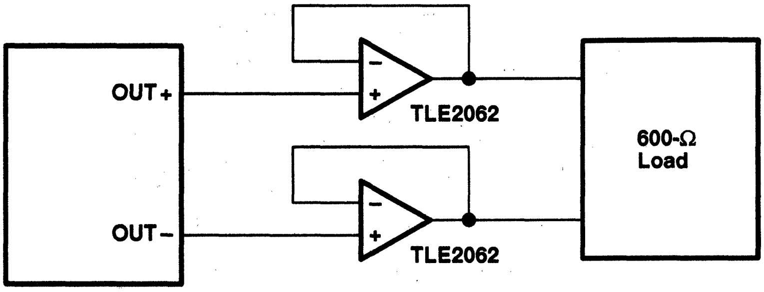
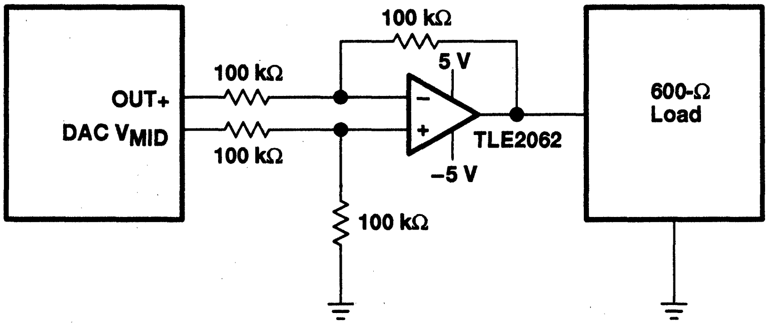


Figure 6−8. Low-Impedance Output Drive



NOTE: When a signal is changed from a single supply with a nonzero reference system to a grounded load, the operational amplifier must be powered from plus and minus supplies or the load must be capacitively coupled.

Figure 6−9. Single-Ended Output Drive (Ground Referenced)

Appendix A
Primary Control Bits

The function of the primary-word control bits D01 and D00 and the hardware terminals FC0 and FC1 are shown below. Any combinational state of D01, D00, FC1, and FC0 not shown is ignored.

CONTROL FUNCTION OF CONTROL BITS

BITS		TERMINALS		DESCRIPTION
D01	D00	FC1	FC0	
0	0	0	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT.
0	0	0	1	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of the next internal $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods equal to the value contained in the A′ register. If the A′ register value is negative, the internal falling edge of $\overline{FS}$ occurs earlier.
0	0	1	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of the next internal $\overline{FS}$, the next ADC/DAC sample time occurs earlier by the number of MCLK periods determined by the value contained in the A′ register. If the A′ register value is negative, the internal falling edge of $\overline{FS}$ occurs later.
0	0	1	1	On the next falling edge of the primary $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. When FC0 and FC1 are both taken high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary $\overline{FS}$.
0	1	0	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A′ register. If the A′ register value is negative, the falling edge of $\overline{FS}$ occurs earlier.
1	0	0	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00. On the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs earlier by the number of MCLK periods determined by the value contained in the A′ register. If the A′ register value is negative, the internal falling edge of $\overline{FS}$ occurs later.
1	1	0	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. When D00 and D01 are both high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary $\overline{FS}$.

CONTROL FUNCTION OF CONTROL BITS (CONTINUED)

BITS		TERMINALS		DESCRIPTION
D01	D00	FC1	FC0	
0	1	1	1	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A′ register. If the A′ register value is negative, $\overline{FS}$ occurs earlier. When FC0 and FC1 are both taken high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary $\overline{FS}$.
1	0	1	1	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00.On the next rising edge of $\overline{FS}$, the next ADC/DAC sample time occurs earlier by the number of MCLK periods determined by the value contained in the A′ register. If the A′ register value is negative, $\overline{FS}$ occurs later. When FC0 and FC1 are both taken high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary $\overline{FS}$.
1	1	1	1	On the next falling edge of the primary $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. When FC1 and FC0 are both high or D01 and D00 are both high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary $\overline{FS}$ occurs at 1/2 the sampling time measured from the falling edge of the primary $\overline{FS}$.
1	1	0	1	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02, to DIN and transmits the ADC data D15–D00 from DOUT. When D00 and D01 are high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary $\overline{FS}$. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A′ register. If the A′ register value is negative, $\overline{FS}$ occurs earlier.
1	1	1	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 to DIN and transmits the ADC data D15–D00 from DOUT. When D00 and D01 are high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary frame sync occurs at 1/2 the sampling time as measured from the falling edge of the primary $\overline{FS}$. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A′ register. If the A′ register value is negative, $\overline{FS}$ occurs earlier.
1	1	1	1	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. When FC1 and FC0 are both high or D01 and D00 are both high, the AIC initiates a secondary $\overline{FS}$ to receive a secondary control word at DIN. The secondary $\overline{FS}$ occurs at 1/2 the sampling time measured from the falling edge of the primary $\overline{FS}$.

Appendix B
Secondary Communications

The function of the control bits DS15 and DS14 and the hardware terminals FC0 and FC1 are shown below. Any combinational state of DS15, DS14, FC1, and FC0 not shown is ignored.

CONTROL FUNCTION OF SECONDARY COMMUNICATION

BITS		TERMINALS		
DS15	**DS14**	**FC1**	**FC0**	
0	0	Ignored		On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.
0	1	Ignored		On the next falling edge of the $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of DS15 and DS14 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A′ register. If the A′ register value is negative, $\overline{FS}$ occurs earlier.
1	0	Ignored		On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of D01 and D00. On the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs earlier by the number of MCLK periods determined by the value contained in the A′ register. If the A′ register value is negative, $\overline{FS}$ occurs later.
1	1	0	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.
1	1	0	1	On the next falling edge of the $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs later by the number of MCLK periods determined by the value contained in the A′ register. If the A′ register value is negative, $\overline{FS}$ occurs earlier.
1	1	1	0	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT. The phase adjustment is determined by the state of FC1 and FC0 such that on the next rising edge of $\overline{FS}$, the next ADC/DAC sampling time occurs earlier by the number of MCLK periods determined by the value contained in the A′ register. If the A′ register value is negative, $\overline{FS}$ occurs later.
1	1	1	1	On the next falling edge of $\overline{FS}$, the AIC receives DAC data D15–D02 at DIN and transmits the ADC data D15–D00 from DOUT.

Appendix C
TLC320AC01C/TLC320AC02C Specification Comparisons

Texas Instruments manufactures the TLC320AC01C and the TLC320AC02C specified for the 0°C to 70°C commercial temperature range and the TLC320AC02I specified for the −40°C to 85°C temperature range. The TLC320AC02C and TLC320AC02I operate at a relaxed TLC320AC01C specification. The differences are listed in the following tables.

ADC Channel Signal-to-Distortion Ratio, V_{DD} = 5 V, f_s = 8 kHz (Unless Otherwise Noted) (see Note 1)

PARAMETER	TEST CONDITIONS	A_V = 0 dB		A_V = 6 dB		A_V = 12 dB		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
TLC320AC01	V_I = −6 dB to −1 dB	68		—		—		dB
TLC320AC02		64		—		—		
TLC320AC01	V_I = −12 dB to −6 dB	63		68		—		
TLC320AC02		59		64		—		
TLC320AC01	V_I = −18 dB to −12 dB	57		63		68		
TLC320AC02		56		59		64		
TLC320AC01	V_I = −24 dB to −18 dB	51		57		63		
TLC320AC02		50		56		59		
TLC320AC01	V_I = −30 dB to −24 dB	45		51		57		
TLC320AC02		44		50		56		
TLC320AC01	V_I = −36 dB to −30 dB	39		45		51		
TLC320AC02		38		44		50		
TLC320AC01	V_I = −42 dB to −36 dB	33		39		45		
TLC320AC02		32		38		44		
TLC320AC01	V_I = −48 dB to −42 dB	27		33		39		
TLC320AC02		26		32		38		

NOTE 1: The analog input test signal is a 1020-Hz sine wave with 0 dB = 6 V peak to peak as the reference level for the analog input signal.

DAC Channel Signal-to-Distortion Ratio, V_{DD} = 5 V, f_s = 8 kHz (Unless Otherwise Noted) (see Note 2)

PARAMETER	TEST CONDITIONS	A_V = 0 dB		A_V = −6 dB		A_V = −12 dB		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
TLC320AC01	V_O = −6 dB to 0 dB	68		—		—		dB
TLC320AC02		64		—		—		
TLC320AC01	V_O = −12 dB to −6 dB	63		68		—		
TLC320AC02		59		64		—		
TLC320AC01	V_O = −18 dB to −12 dB	57		63		68		
TLC320AC02		56		59		64		
TLC320AC01	V_O = −24 dB to −18 dB	51		57		63		
TLC320AC02		50		56		59		
TLC320AC01	V_O = −30 dB to −24 dB	45		51		57		
TLC320AC02		44		50		56		
TLC320AC01	V_O = −36 dB to −30 dB	39		45		51		
TLC320AC02		38		44		50		
TLC320AC01	V_O = −42 dB to −36 dB	33		39		45		
TLC320AC02		32		38		44		
TLC320AC01	V_O = −48 dB to −42 dB	27		33		39		
TLC320AC02		26		32		38		

NOTE 2: The input signal, V_I, is the digital equivalent of a 1020-Hz sine wave (full-scale analog output at full-scale digital input = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT−.

System Distortion, ADC Channel Attenuation, V_{DD} = 5 V, f_s = 8 kHz, FCLK = 144 kHz (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
TLC320AC01	Second harmonic	Differential input (see Note 3)	70		dB
TLC320AC02	Second harmonic	Differential input (see Note 3)	64		dB
TLC320AC01	Third harmonic and higher harmonics	Differential input (see Note 3)	70		dB
TLC320AC02	Third harmonic and higher harmonics	Differential input (see Note 3)	64		dB

NOTE 3: The input signal is a 1020 Hz-sine wave for the ADC channel. Harmonic distortion is defined for an input level of −1 dB.

System Distortion, DAC Channel Attenuation, V_{DD} = 5 V, f_s = 8 kHz, FCLK = 144 kHz (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
TLC320AC01	Second harmonic	Differential output (see Note 4)	70		dB
TLC320AC02	Second harmonic	Differential output (see Note 4)	64		dB
TLC320AC01	Third harmonic and higher harmonics	Differential output (see Note 4)	70		dB
TLC320AC02	Third harmonic and higher harmonics	Differential output (see Note 4)	64		dB

NOTE 4: The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT−. Harmonic distortion is specified for a signal input level of 0 dB.

TLC320AD55C Data Manual

Sigma-Delta Analog Interface Circuit

TEXAS INSTRUMENTS

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1 Introduction

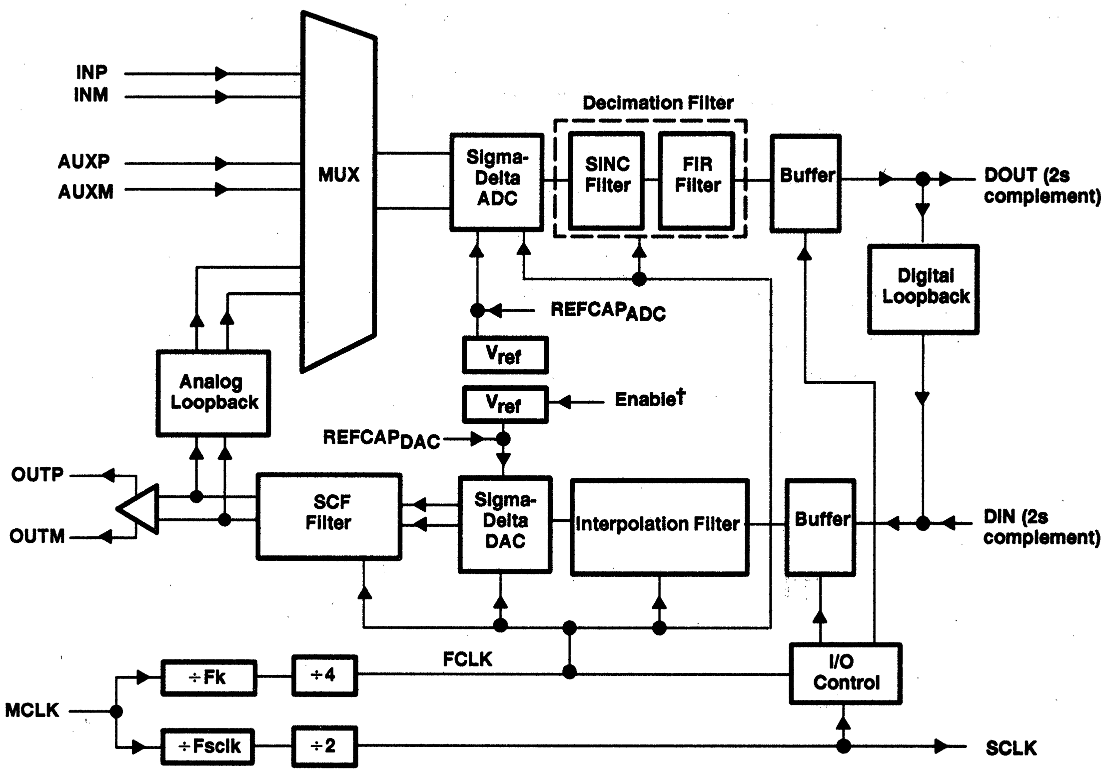
The TLC320AD55C provides high resolution low-speed signal conversion from digital-to-analog (D/A) and from analog-to-digital (A/D) using oversampling sigma-delta technology. This device consists of two, serial, synchronous conversion paths (one for each data direction) and includes an interpolation filter before the digital-to-analog converter (DAC) and a decimation filter after the analog-to-digital converter (ADC) (see Figure 1–1). Other overhead functions provide analog filtering and on-chip timing and control. The sigma-delta architecture produces high resolution, analog-to-digital and digital-to-analog conversion at low system speeds and low cost.

The options and the circuit configurations of this device can be programmed through the serial interface. The options include reset, power-down, communications protocol, serial clock rate, signal sampling rate, and test mode as outlined in Appendix A. The circuit configurations could include a selection of input ports to the ADC, analog loopback, digital loopback, decimator sinc filter output, decimator finite-duration impulse-response (FIR) filter output, interpolator sinc filter output, and interpolator FIR filter output. The TLC320AD55C is characterized for operation from 0°C to 70°C.

1.1 Features

- Single 5-V power supply
- Power dissipation (P_D) of 150 mW maximum in the operating mode
- Power-down mode to 1 mW
- General-purpose 16-bit signal processing
- 2s-complement format
- Serial port interface
- Minimum 80-dB harmonic distortion plus noise
- Differential architecture
- Internal reference voltage (V_{ref})
- Internal 64 × oversampling
- Analog output with programmable gain of 1, 1/2, 1/4, and 0 (squelch)
- Phone-mode output control
- Variable conversion rate selected as MCLK/(Fk × 256), Fk = 1,2,3,...,256
- System test mode:
  - Digital loopback test
  - Analog loopback test

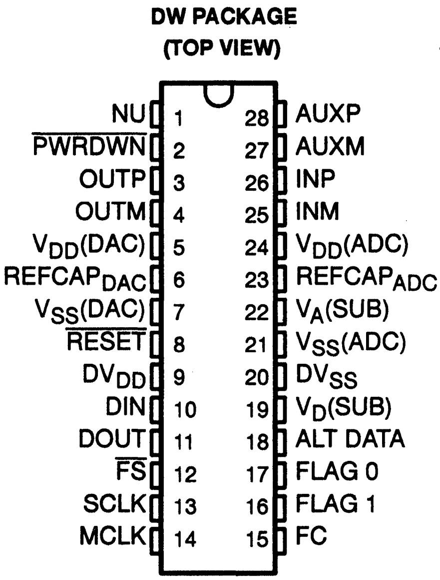
1.2 Functional Block Diagram



† See control 3 register in Appendix A.

Figure 1–1. Functional Block Diagram

1.3 Terminal Assignments



NU – Make no external connection

Figure 1–2. Terminal Assignments

1.4 Ordering Information

T_A	PACKAGE SMALL OUTLINE (DW)
0°C to 70°C	TLC320AD55CDW

1.5 Terminal Functions

TERMINALS NAME	NO.	I/O	DESCRIPTION
AUXM	27	I	Inverting input to auxiliary analog input
AUXP	28	I	Noninverting input to auxiliary analog input
ALT DATA	18	I	Signals on ALT DATA are routed to DOUT during secondary communiction when phone mode is enabled.
DIN	10	I	Data input. DIN receives the DAC input data and command information from the DSP and is synchronized to SCLK.
DOUT	11	O	Data output. DOUT transmits the ADC output bits and is synchronized to SCLK. DOUT is at Hi-Z when $\overline{FS}$ is not activated.
DV_{DD}	9	I	Digital power supply
DV_{SS}	20	I	Digital ground
FC	15	I	Function control. FC is sampled and latched on the rising edge of $\overline{FS}$ for the primary serial communication. Refer to Section 3 Serial Communications for more details.
FLAG 0	17	O	During phone mode, FLAG 0 contains the value set in control 2 register.
FLAG 1	16	O	During phone mode, FLAG 1 contains the value set in control 2 register.
$\overline{FS}$	12	O	Frame sync. When $\overline{FS}$ goes low, the serial communication port is activated. In all serial transmission modes, $\overline{FS}$ is held low during bit transmission. Refer to Section 3 Serial Communications for a detailed description.
INM	25	I	Inverting input to analog input
INP	26	I	Noninverting input to analog input
MCLK	14	I	Master clock. MCLK derives the internal clocks of the sigma-delta analog interface circuit.
OUTM	4	O	Inverting output of the DAC analog power amplifier. Functionally identical with and complementary to OUTP. OUTM and OUTP can drive 600 Ω differentially. OUTM should not be used alone for single-ended operation.
OUTP	3	O	Noninverting output of the DAC analog power amplifier. OUTM and OUTP can drive 600 Ω differentially. OUTP should not be used alone for single-ended operation.
$\overline{PWRDWN}$	2	I	Power down. When $\overline{PWRDWN}$ is pulled low, the device goes into a power-down mode; the serial interface is disabled and most of the high-speed clocks are disabled. However, all of the registers' values are sustained and the device resumes full power operation without reinitialization when $\overline{PWRDWN}$ is pulled high again. $\overline{PWRDWN}$ resets the counters only and preserves the programmed register contents. Refer to Section 2.2.1.3 Software and Hardware Power-Down.
$REFCAP_{ADC}$	23	O	Analog-reference voltage connection for external capacitor for the ADC. The nominal voltage on $REFCAP_{ADC}$ is 3.4 V. A buffer must be used when this voltage is used externally. $REFCAP_{ADC}$ is not to be used as the mid-supply voltage reference for single-ended operation.
$REFCAP_{DAC}$	6	O	Analog-reference voltage connection for external capacitor for the DAC. The nominal voltage on $REFCAP_{DAC}$ is 3.4 V. A buffer must be used when this voltage is used externally.
$\overline{RESET}$	8	I	Reset. The reset function initializes all of the internal registers to their default values. The serial port can be configured to the default state accordingly. Refer to Appendix A Table A–2 Control 1 Register and Section 2.2.1 Reset and Power-Down for more detailed descriptions.
SCLK	13	O	Shift clock. SCLK is derived from MCLK and clocks serial data into DIN and out of DOUT.

NOTE 1: All digital inputs and outputs are TTL compatible unless otherwise noted.

1.5 Terminal Functions (Continued)

TERMINALS NAME	NO.	I/O	DESCRIPTION
V_A(SUB)	22	I	Analog substrate. V_A(SUB) must be grounded.
V_D(SUB)	19	I	Digital substrate. V_D(SUB) must be grounded.
V_{DD}(ADC)	24	I	Analog ADC path supply
V_{DD}(DAC)	5	I	Analog DAC path supply
V_{SS}(ADC)	21	I	Analog ADC path ground
V_{SS}(DAC)	7	I	Analog DAC path ground

NOTE 1: All digital inputs and outputs are TTL compatible unless otherwise noted.

1.6 Definitions and Terminology

Data Transfer Interval	The time during which data is transferred from DOUT and to DIN. The interval is 16 shift clocks and this data transfer is initiated by the falling edge of the frame-sync signal.
Signal Data	The input signal and all of the converted representations through the ADC channel and return through the DAC channel to the analog output. This is contrasted with the purely digital software control data.
Primary Communications	The digital data transfer interval. Since the device is synchronous, the signal data words from the ADC channel and to the DAC channel occur simultaneously.
Secondary Communications	The digital control and configuration data transfer interval into DIN and the register read data cycle from DOUT. The data transfer interval occurs when requested by hardware or software.
Frame Sync	The falling edge of the signal that initiates the data transfer interval. The primary frame sync starts the primary communications, and the secondary frame sync starts the secondary communications.
Frame Sync and Sampling Period	The time between falling edges of successive primary frame-sync signals.
f_s	The sampling frequency that is the reciprocal of the sampling period.
Frame-Sync Interval	The time period occupied by 16 shift clocks. It goes high on the sixteenth rising edge of SCLK after the falling edge of the frame sync.
ADC Channel	All signal processing circuits between the analog input and the digital conversion results at DOUT.
DAC Channel	All signal processing circuits between the digital data word applied to DIN and the differential output analog signal available at OUTP and OUTM.
Host	Any processing system that interfaces to DIN, DOUT, SCLK, or $\overline{FS}$.
Dxx	A bit position in the primary data word (xx is the bit number).
DSxx	A bit position in the secondary data word (xx is the bit number).
d	The alpha character d is used to represent valid programmed or default data in the control register format (see secondary serial communications) when discussing other data bit portions of the register.
X	The alpha character X represents a don't-care bit position within the control register format.
FIR	Finite-duration impulse response.

1.7 Register Functional Summary

There are six data and control registers that are used as follows:

Register 0 The No-op register. The 0 register allows secondary requests without altering any other register.

Register 1 The control 1 register. The data in this register controls:

- The software reset
- The software power-down
- Selection of the normal or auxiliary analog inputs
- The output amplifier gain (1, 1/2, 1/4, or squelch)
- Selection of the analog loopback
- Selection of the digital loopback
- 16-bit or 15-bit mode of operation

Register 2 The control 2 register. The data in this register:

- Contains the output flag indicating a decimator FIR filter overflow
- Contains Flag 0 and Flag 1 output values for use in the phone mode
- Selects the phone mode
- Selects or bypasses the decimation FIR filter
- Selects or bypasses the interpolater FIR filter

Register 3 The Fk divide register. This register controls the filter clock rate and the sample period.

Register 4 The Fsclk divide register. This register controls the shift (data) clock rate.

Register 5 The control 3 register. This register enables and disables the DAC reference.

2 Functional Description

2.1 Device Functions

The following sections describe the functions of the device.

2.1.1 Operating Frequencies

The sampling (conversion) frequency is derived from the master clock (MCLK) input by the following equation:

$$f_S = \text{Sampling (conversion) frequency} = \frac{\text{MCLK frequency}}{(\text{Fk register value}) \times 256}$$

The inverse is the time between the falling edges of two successive primary frame-synchronization signals and it is the conversion period.

The input and output data clock (SCLK) is given by:

$$\text{SCLK frequency} = \frac{\text{MCLK frequency}}{(\text{Fsclk register value}) \times 2}$$

2.1.2 ADC Signal Channel

To produce excellent common-mode rejection of unwanted signals, the analog signal is processed differentially until it is converted to digital data.

The ADC converts the signal into discrete output digital words in 2s-complement format, corresponding to the analog-signal value at the sampling time. These 16-bit digital words, representing sampled values of the analog input signal, are clocked out of the serial port, DOUT, during the frame-sync interval (one word for each primary communication interval). During secondary communications, the data previously programmed into the registers can be read out with the appropriate register address, and the read bit set to 1. When a register read is not requested, all 16 bits are 0 in the secondary word.

2.1.3 DAC Signal Channel

DIN receives the 16-bit serial data word (2s complement) from the host during the primary communications interval and latches the data on the seventeenth rising edge of SCLK. The data are converted to an analog voltage by the DAC and then passed through a (sin x)/x correction circuit and a smoothing filter. An output buffer with three software-programmable gains (0 dB, −6 dB, and −12 dB) drives the differential outputs OUTP and OUTM. A squelch mode can also be programmed for the output buffer. During secondary communications, the configuration program data are read into the device control registers.

2.1.4 Serial Interface

The digital serial interface consists of the shift clock, the frame synchronization signal, the ADC-channel data output, and the DAC-channel data input. During the primary 16-bit frame synchronization interval, SCLK transfers the ADC channel results from DOUT and transfers 16-bit DAC data into DIN.

During the secondary frame-synchronization interval, the SCLK transfers the register read data from DOUT when the read bit is set to a one. In addition, SCLK transfers control and device parameter information into DIN. The functional sequence is shown in Figure 3–1.

2.1.5 Register Programming

All register programming occurs during secondary communications, and data are latched and valid on the rising edge of the frame-sync signal. When the default value for a particular register is desired, that register does not need to be addressed during secondary communications. The no-op command addresses the no-op register (register 0), and register programming does not take place during this communication.

DOUT is released from the high-impedance state on the falling edge of the primary or secondary frame-sync interval. In addition, each register can be read back during DOUT secondary communications by setting the read bit D13 to 1 in the addressed register (refer to Appendix A). When the register is in the read mode, no data can be written to the register during this cycle. To return this register to the write mode requires a subsequent secondary communication.

2.1.6 Sigma-Delta ADC

The sigma-delta ADC is a fourth-order, sigma-delta modulator with 64-times oversampling. The ADC provides high-resolution, low-noise performance using oversampling techniques.

2.1.7 Decimation Filter

The decimation filter reduces the digital data rate to the sampling rate. This is accomplished by decimating with a ratio of 1:64. The output of this filter is a sixteen-bit, 2s-complement data word clocking at the sample rate.

NOTE

The sample rate is determined through a programmable relationship of MCLK/(Fk × 256), Fk = 1,2,3,...,256

2.1.8 Sigma-Delta DAC

The sigma-delta DAC is a fourth-order, sigma-delta modulator with 64-times oversampling. The DAC provides high-resolution, low-noise performance from a one-bit converter using oversampling techniques.

2.1.9 Interpolation Filter

The interpolation filter resamples the digital data at a rate of 64 times the incoming sample rate. The high-speed data output from this filter is then used in the sigma-delta DAC.

2.1.10 Switched-Capacitor Filter (SCF)

A switched-capacitor filter network is implemented on the analog output to provide low-pass operation with high rejection in the stop band.

2.1.11 Analog/Digital Loopback

The loopbacks provide a means of testing the ADC/DAC channels and can be used for in-circuit, system-level tests. The loopbacks feed the appropriate output to the corresponding input on the device.

The test capabilities include an analog loopback between the two analog paths and a digital loopback between the two digital paths. Each loopback is enabled by setting the D1 or D2 bit in control 1 register (see Appendix A).

2.1.12 DAC Voltage Reference Enable

The DAC voltage reference can be disabled through the control 3 register. This allows the use of an external voltage reference applied to the DAC channel modulator. By supplying an external reference, the user can scale the output voltage range of this channel. The internal reference value is 3.6 V which provides a 6-V, peak-to-peak, differential output. The ratio of an external reference to the internal reference determines the output voltage range of the DAC channel as shown in the following equation:

$$V_{O(PP)} = \frac{V(EXT\ REF)}{3.6} \times 6\ V$$

NOTE

The distortion and noise specifications listed in Section 4 Specifications apply only under the following condition:

$$\frac{V(EXT\ REF)}{3.6} \leq 1$$

2.1.13 FIR Overflow Flag

The decimator FIR filter provides an overflow flag to the control 2 register to indicate that the input to the filter has exceeded the range of the internal filter calculations. When this bit is set in the register, it remains set until the register is read by the user. Reading this value always resets the overflow flag.

2.2 Terminal Descriptions

The following sections describe the terminal functions.

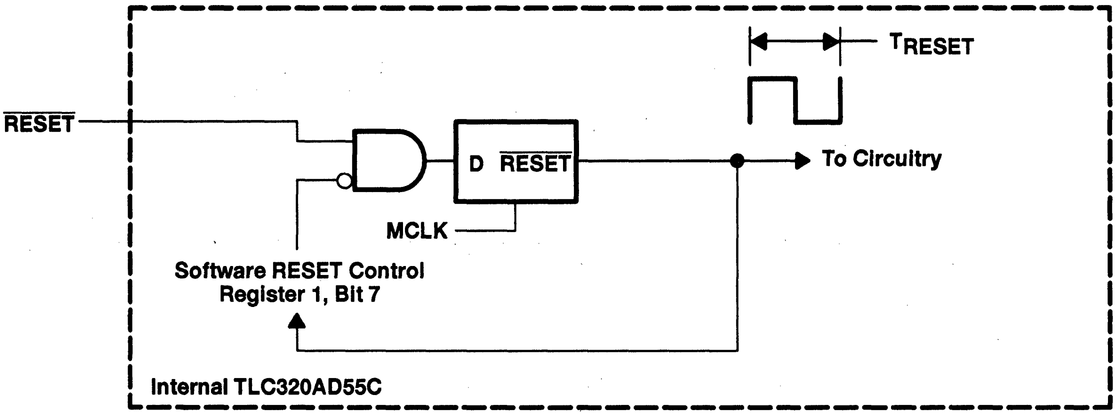
2.2.1 Reset and Power-Down

2.2.1.1 Reset

As shown in Figure 2–1, the TLC320AD55C resets both the internal counters and registers, including the programmed registers, in two ways:

- By appling a low-going reset pulse to the $\overline{\text{RESET}}$ terminal
- By writing to the programmable software reset bit (D07 in control 1 register)

$\overline{\text{PWRDWN}}$ resets the counters only and preserves the programmed register contents. The DAC resets to the 15-bit mode.



NOTE A: $\overline{\text{RESET}}$ to circuitry is at least 6 MCLK periods long and releases on the positive edge of MCLK.

Figure 2–1. Reset Function

2.2.1.2 Conditions of Reset

The two internal reset signals used for the reset and synchronization functions are:

- Counter reset –This signal resets all flip-flops and latches that are not externally programmed, with the exception of those generating the reset pulse itself. Additionally, this signal resets the software power-down bit.

  Counter reset =$\overline{\text{RESET}}$ terminal or reset bit or $\overline{\text{PWRDWN}}$ terminal

- Register reset –This signal resets all flip-flops and latches that are not reset by the counter reset, except those generating the reset pulse itself.

  Register reset =$\overline{\text{RESET}}$ terminal or reset bit

Both reset signals are at least six MCLK periods long (T_{RESET}) and release on the trailing edge of MCLK.

2.2.1.3 Software and Hardware Power-Down

Given the definitions above, the software-programmed power-down condition is cleared by programming the software bit (control 1 register bit 6) to a 0 or is cleared by cycling the power to the device, bringing $\overline{\text{PWRDWN}}$ low, or bringing $\overline{\text{RESET}}$ low (see Figure 2–2).

$\overline{\text{PWRDWN}}$ removes power to the entire chip. The software-programmable, power-down bit only removes power from the analog section of the chip, which allows a software power-up function. Cycling the power-down terminal from high to low and back to high resets all flip-flops and latches that are not externally programmed, thereby preserving the register contents with the exception that the software power-down bit is cleared.

When $\overline{\text{PWRDWN}}$ is not being used, it should be tied high [V_{DD}(ADC) is preferred].

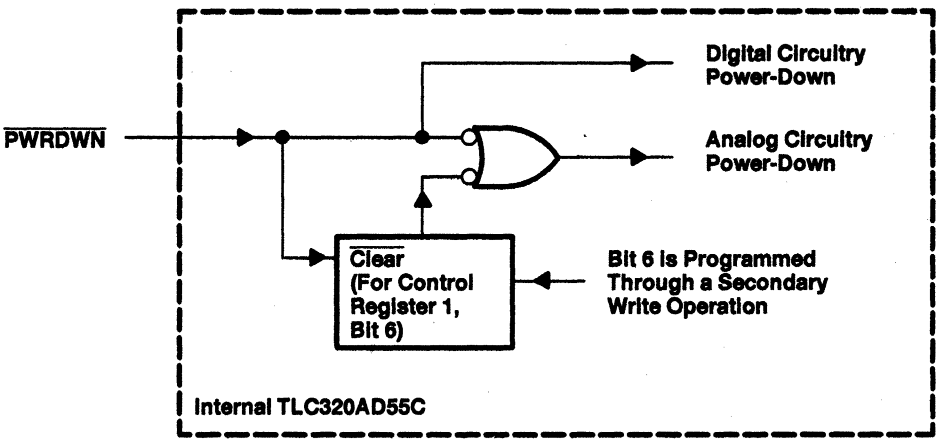


Figure 2–2. Internal Power-Down Logic

2.2.2 Master Clock Circuit

The clock circuit generates and distributes necessary clocks throughout the device. MCLK is the external master clock input. SCLK is derived from MCLK [SCLK = MCLK/(Fsclk × 2), Fsclk = 1,2,3,...,256] in order to provide clocking of the serial communications between the device and a digital signal processor (DSP). The sample rate of the data paths is set as MCLK/(Fk × 256). Fk and Fsclk are programmable register values used as divisors of MCLK. The default value for the Fk and Fsclk register is 8 (decimal).

2.2.3 Data Out (DOUT)

DOUT is taken from the high-impedance state by the falling edge of the frame-sync signal. The most significant data bit then appears on DOUT.

DOUT is placed in a high-impedance state on the sixteenth rising edge of SCLK (internal or external) after the falling edge of the frame-sync signal. In the primary communication, the data word is the ADC conversion result. In the secondary communication, the data is the register read results when requested by the read/write (R/$\overline{\text{W}}$) bit with the eight MSBs set to zero (see the serial communications section). When a register read is not requested, the secondary word is all zeroes.

2.2.4 Data In (DIN)

In the primary communication, the data word is the input digital signal to the DAC channel. In the secondary communication, the data is the control and configuration data to set up the device for a particular function (see Section 3 Serial Communications).

2.2.5 Hardware Program Terminal (FC)

This input provides for hardware programming requests for secondary communication. It works in conjunction with the control bit D00 of the secondary data word. The signal on FC is latched 1/2 shift clock after the rising edge of the next internally generated primary frame-sync interval. FC should be tied low when not being used (see Section 3.2 Secondary Serial Communication).

2.2.6 Frame-Sync

The frame-sync signal indicates that the device is ready to send and receive data. The data transfer from DOUT and into DIN begins on the falling edge of the frame-sync signal.

The frame sync is generated internally and goes low on the rising edge of SCLK and remains low during the 16-bit data transfer.

2.2.7 Multiplexed Analog Input

The two differential analog inputs (INP and INM or AUXP and AUXM) are multiplexed into the sigma-delta modulator. The performance of the AUX channel is similar to the normal input channel.

2.2.8 Analog Input

The signal applied to the terminals INM and INP should be differential to preserve the device specifications (see Figure 2–3). A single-ended input signal should always be converted to a differential input signal prior to being used by the TLC320AD55C. The signal source driving the analog inputs (INM, INP, AUXM, AUXP) should have a low source-impedance for lowest noise performance and accuracy.

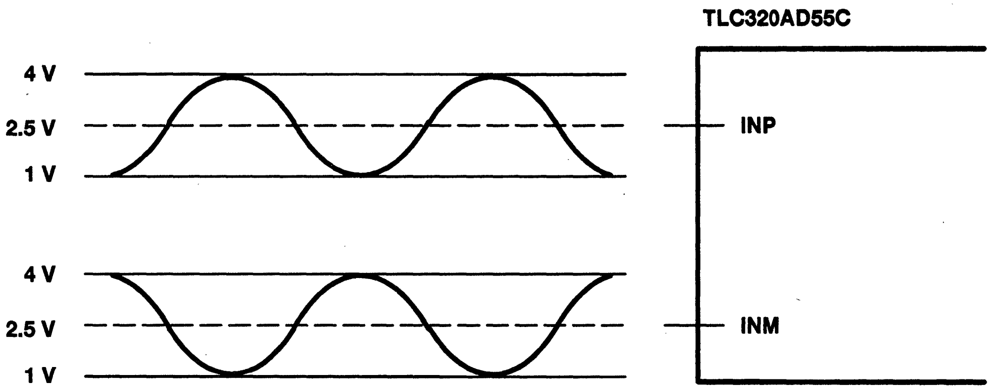


Figure 2–3. Differential Analog Input Configuration

3 Serial Communications

DOUT, DIN, SCLK, $\overline{FS}$, and FC are the serial communication signals. The digital output data from the ADC is taken from DOUT. The digital input data for the DAC is applied to DIN. The synchronizing clock for the serial communication data and the frame sync is taken from SCLK. The frame-synchronization pulse that encloses the ADC/DAC data transfer interval is taken from $\overline{FS}$. For signal (audio) data transmitted from the ADC or to the DAC, primary serial communication is used. To read or write words that control both the options and the circuit configurations of the device, secondary communication is used.

The purpose of the primary and secondary communications is to allow conversion data and control data to be transferred across the same serial port. A primary transfer is always dedicated to conversion data. A secondary transfer sets up and reads the register values described in Appendix A. A primary transfer occurs for every conversion period. A secondary transfer occurs only when requested. Two methods exist for requesting a secondary command. Terminal FC can request a secondary communication when it is asserted, or the LSB of the DAC data within a primary transfer can request a secondary communication. The selection of which method is enabled is provided in control 1 register (bit 0) as shown in Appendix A.

For all serial communications, the most significant bit is transferred first. For a 16-bit ADC word and a 16-bit DAC word, D15 is the most significant bit and D0 is the least significant bit. For a 15-bit DAC data word in the 16-bit primary communication, D15 is the most significant bit, D1 is the least significant bit, and D0 is used for the embedded function control. All digital data values are in 2s-complement format.

These logic signals are compatible with TTL-voltage levels and CMOS current levels.

3.1 Primary Serial Communication

Primary serial communication is used both to transmit and receive conversion signal data. The ADC word length is always 16 bits. The DAC word length depends on the status of D0 in the control 1 register. After power-up or reset, the device defaults to the 15-bit mode (not 16-bit mode). The DAC word length is 15 bits and the last bit of the primary 16-bit serial communication word is a function-control bit used to request secondary serial communications. In the 16-bit mode, all 16 bits of the primary communications word are used as data for the DAC and the hardware terminal FC must be used to request secondary communications.

Figure 3–1 shows the timing relationship for SCLK, $\overline{FS}$, DOUT and DIN in a primary communication. The timing sequence for this operation is as follows:

1. The TLC320AD55C takes $\overline{FS}$ low.
2. One 16-bit word is transmitted from the ADC (DOUT) and one 16-bit word is received for the DAC (DIN).
3. The TLC320AD55C takes $\overline{FS}$ high.

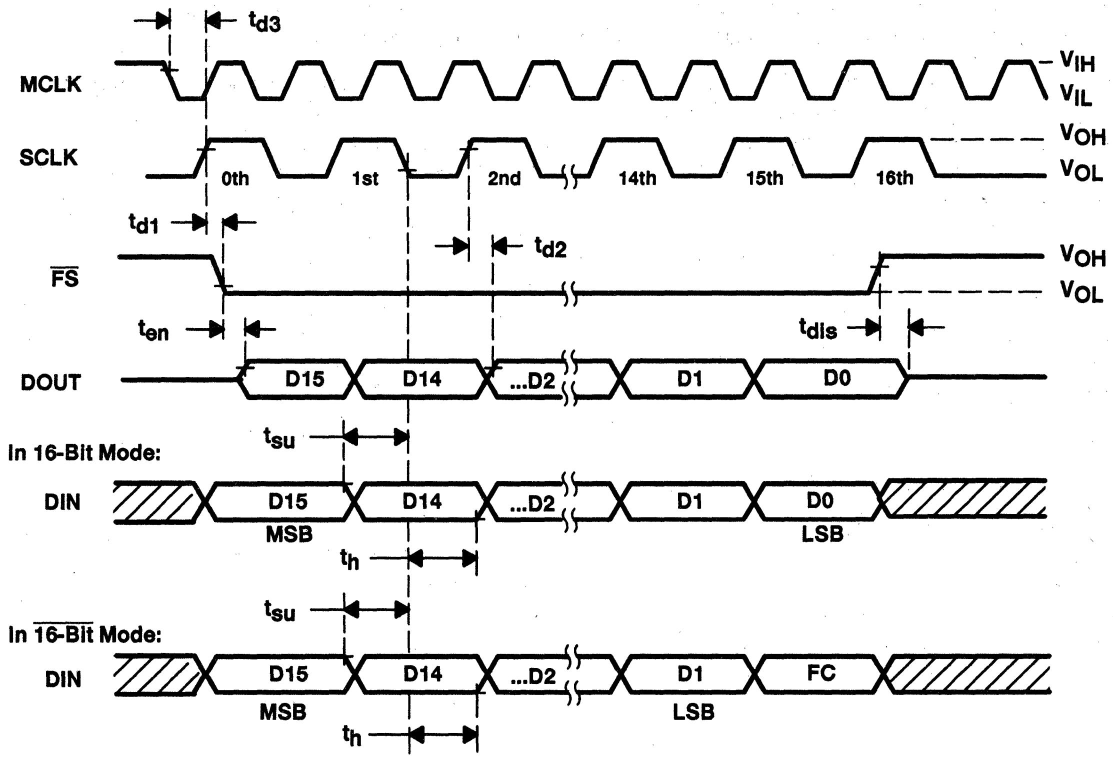


Figure 3–1. Primary Serial Communication Timing

When a secondary request is made through the LSB of the DAC data word ($\overline{16\text{-bit}}$ mode), the format shown in Figure 3–2 is used:

D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0

◄—— 15-bit DAC 2s-complement format ——► (D15–D1) ◄—► control (D0)

◄—— 16-bit ADC 2s-complement format ——► (D15–D0)

Figure 3–2. DAC and ADC Word Lengths

3.2 Secondary Serial Communication

Secondary serial communication reads or writes 16-bit words that program both the options and the circuit configurations of the device. All register programming occurs during secondary communications. Four primary and secondary communication cycles are required to program the four registers. When the default value for a particular register is desired, the user can omit addressing it during secondary communication. A no-op command addresses the no-op register (register 0), and no register programming takes place during this secondary communication.

There are two methods for initiating secondary communications (see Figure 3–3):
1) by asserting a high level on FC, or 2) by asserting the LSB of DIN 16-bit serial communication high while not in 16-bit mode (see control 1 register bit 0).

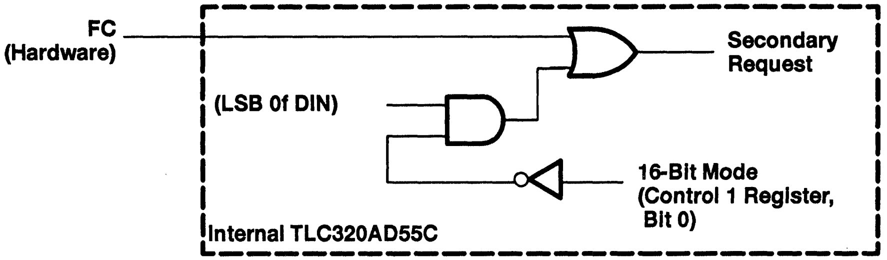


Figure 3–3. Hardware and Software Methods to Initate a Secondary Request

1. Figures 3–5 and 3–6 show the two different methods by which FC requests secondary communication words as well as the timing for $\overline{FS}$, DOUT, DIN, and SCLK. The examples span two primary communication frames. Figure 3–5 shows the use of hardware function control.

   During a secondary communication, a register can be written to or read from. When writing a value to a register, DIN contains the value to be written (see Figure 3–7). The data returned on DOUT is 00(hex). When performing a read function, DIN can still provide data to be written to an addressed register; however, DOUT contains the most recent value contained in the register addressed by DIN.

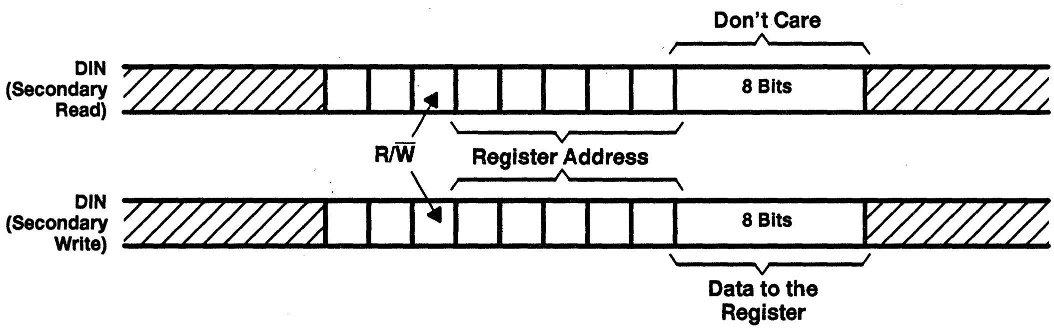


Figure 3–4. Secondary DIN Format

In Figure 3–5, FC clocks in and latches on the rising edge of frame sync ($\overline{FS}$). This causes the start of the secondary update 32 FCLKs (see Fk divide register, Appendix A) after the start of the primary communication frame. Read and write examples are shown for DIN and DOUT.

2. Figure 3–6 shows the use of software function control.

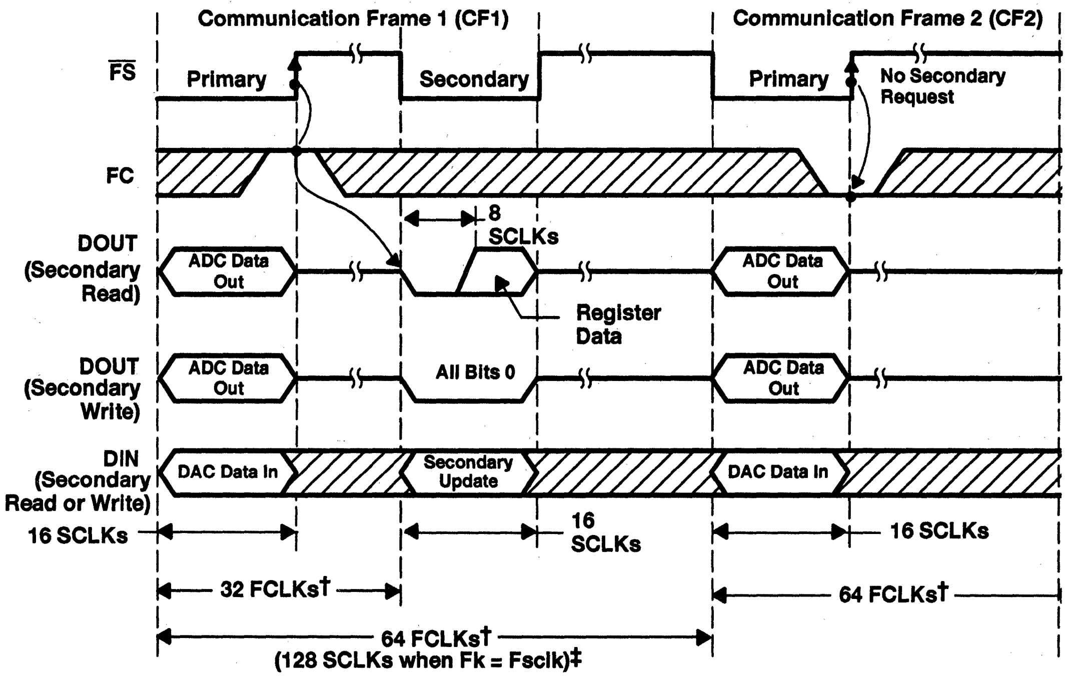
   The software request for function control is typically used when the required resolution of the DAC channel is less than 16 bits. Then the least significant bit (D0) can be used for the secondary requests as shown in Table 3–1.

Table 3–1. Least-Significant-Bit Control Function

CONTROL BIT D0	CONTROL BIT FUNCTION
0	No operation (no-op)
1	Secondary communication request

On the falling edge of the next $\overline{FS}$, D15 through D1 is input to DIN or D15 through D0 is output to DOUT.

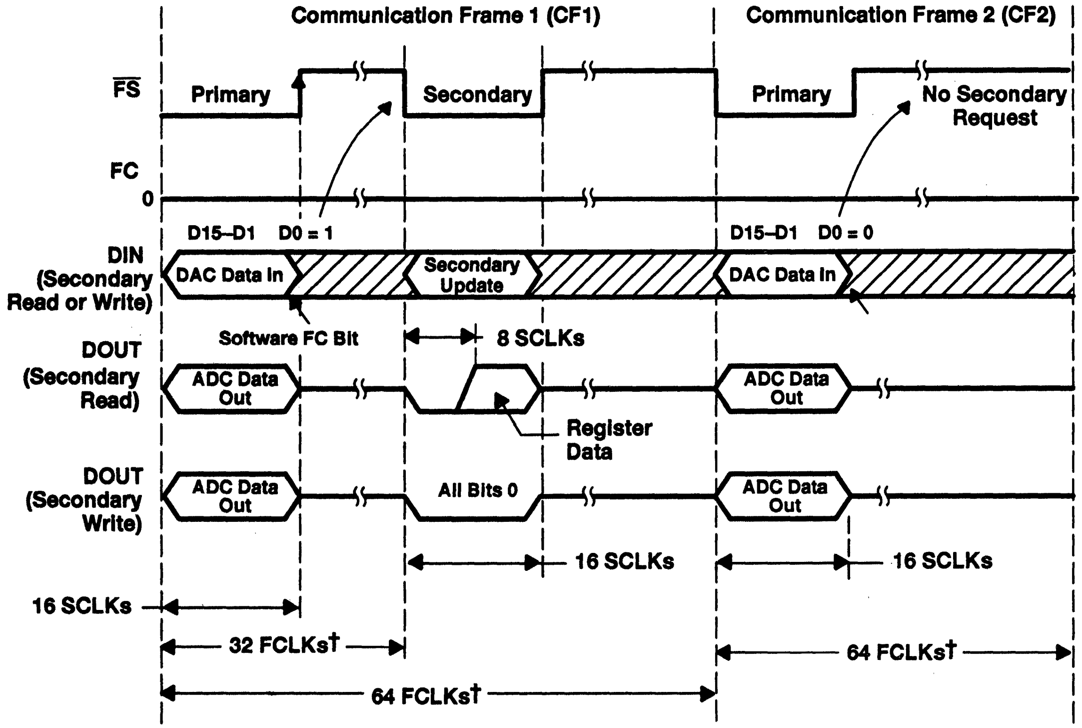
When a secondary communication request is made, $\overline{FS}$ goes low for 32 FCLKs (see Fk divide register, Appendix A) after the beginning of the primary frame.



† See Fk divide register in Appendix A.
‡ For a selected MCLK, Fk and Fsclk: SCLK = 2 Fk/Fsclk × FCLK

Figure 3–5. Hardware FC Secondary Request (Phone Mode Disabled)

In Figure 3–6, FC hardware terminal 15 is left in its nonasserted state (0). FC is asserted through software by embedding an asserted high level (1) in the LSB of the 16-bit primary word. This is possible when not in 16-bit mode (control 1 register bit 2 = 0) because the user is using only 15 bits of DAC information.



† See Fk divide register in Appendix A.

NOTE A: For a read cycle, the last 8 bits are don't care.

Figure 3–6. Software FC Secondary Request (Phone Mode Disabled)

Table 3–2 shows the secondary communications format. D13 is the R/$\overline{W}$ bit, the read/not-write bit.

D12 through D8 are address bits. The register map is specified in the register set section in Appendix A. D7 through D0 are data bits. The data bits are values for the specified register addressed by data bits D12 through D8.

Table 3–2. Secondary Communication Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	R/$\overline{W}$	A	A	A	A	A	D	D	D	D	D	D	D	D

3.3 Conversion Rate Versus Serial Port

The SCLK frequency can be programmed independently from the FCLK frequency. This can create a problem with the interpretation of the serial port data. The serial port is designed to initiate a primary communication every 64 SCLKs. There must be an integer number of SCLKs ≥ 40 per sample period. Two examples follow to demonstrate the possible output of the serial port. SCLK must be fast enough to collect all data from each frame.

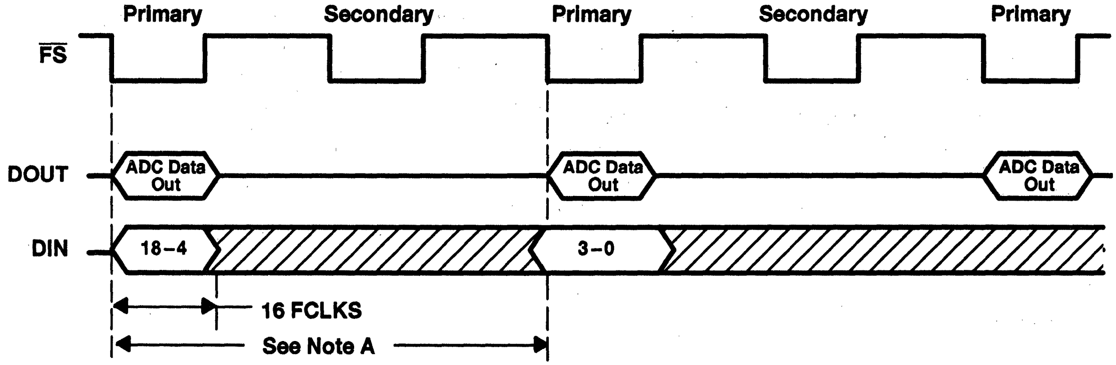
Example 1: MCLK = 4.096 MHz, sample rate = 8 kHz, 8 kHz = MCLK/(Fk × 256), set Fk = 2, SCLK = MCLK/(Fsclk × 2), set Fsclk = 2, SCLK = 1.024 MHz. With this configuration, SCLK = sample rate × 128. Therefore, each primary communication is a valid sample.

Example 2: All variables above remain the same except Fsclk = 1, SCLK = 2.048 MHz = sample rate × 256. In this configuration, two consecutive primary communications represent the same data sample.

3.4 FIR Bypass Mode

An option is provided to bypass the FIR sections of the decimation filter and the interpolation filter. This is selected through the control 2 register. The sinc filters of the two paths cannot be bypassed.

The timing requirements for this mode of operation are shown in Figure 3–7.



NOTE A: The number of clocks between primary cycles is a function of FCLK. When either FIR is bypassed, this period is 16 FCLKs. See Fk divide register in Appendix A.

Figure 3–7. FIR Bypass Timing

3.5 Phone Mode Control

This function is provided for applications that need hardware control and monitor of external events. By allowing the device to drive two FLAG terminals (set through the control 2 register), the host digital signal processor (DSP) is capable of system control through the same serial port connection to the device. Along with this control is the capability for monitoring the value of the ALT DATA terminal during a secondary communication cycle. One application for this function is in monitoring ring detect or offhook detect from a phone answering system. The two FLAG terminals allow response to these incoming control signals. Figure 3–8 shows the timing associated with this operating mode.

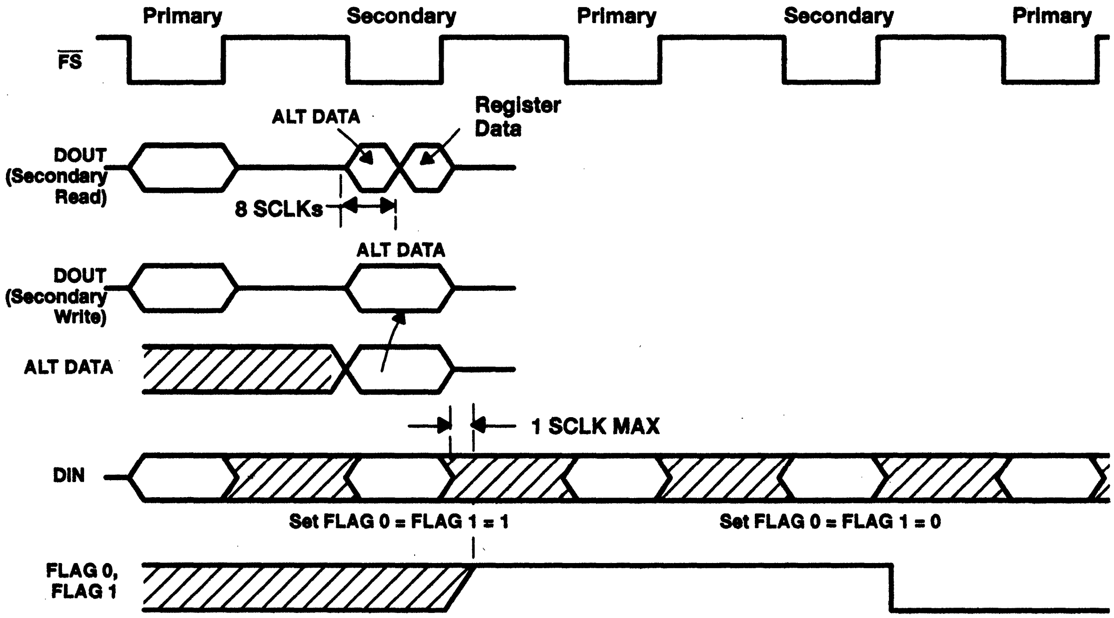


Figure 3–8. Phone Mode Timing

4 Specifications

4.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage range, DV_{DD}, V_{DD}(ADC, DAC)(see Note 1) .... –0.3 V to 6.5 V
Output voltage range, DOUT, $\overline{FS}$, SCLK, FLAG 0, FLAG 1 ... –0.3 V to DV_{DD} + 0.3 V
Output voltage range, OUTP, OUTM .... –0.3 V to V_{DD} + 0.3 V
Input voltage range, DIN, $\overline{PWRDWN}$, $\overline{RESET}$, ALT DATA,
MCLK, FC .... –0.3 V to DV_{DD} + 0.3 V
Input voltage range, INP, INM, AUXP, AUXM .... –0.3 V to V_{DD} + 0.3 V
Case temperature for 10 seconds, T_C: DW package .... 260°C
Operating free-air temperature range, T_A .... 0°C to 70°C
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}(DAC) for DAC channel measurements and V_{SS}(ADC) for ADC channel measurements.

4.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}(ADC, DAC)		4.5		5.5	V
Analog signal input voltage, V_I	Differential, (INP–INM) peak, for full scale operation			6	V
Load resistance for OUTP and OUTM, R_L		0.3	10		kΩ
Load capacitance for OUTP and OUTM, C_L				100	pF
ADC or DAC conversion rate (Nyquist)			8		kHz
Operating free-air temperature, T_A		0		70	°C

4.3 Recommended Operating Conditions, DV_{DD} = 5 V

	MIN	NOM	MAX	UNIT
Supply voltage, DV_{DD}	4.5		5.5	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
MCLK frequency (see Note 2), duty cycle = 50 ±10%		16.384		MHz

NOTE 2: The default state for an 8 kHz conversion rate requires a 16.384 MHz MCLK frequency.

4.4 Electrical Characteristics, T_A = 25°C, V_{DD}(ADC) = V_{DD}(DAC) = DV_{DD} = 5 V, MCLK = 16.384 MHz, Fk = 8 (unless otherwise noted)

4.4.1 Digital Inputs and Outputs, Outputs Not Loaded

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, DOUT	I_O = 360 µA	2.4	4.6		V
V_{OL}	Low-level output voltage, DOUT	I_O = 2 mA		0.2	0.4	V
I_{IH}	High-level input current, any digital input	V_{IH} = 5 V			10	µA
I_{IL}	Low-level input current, any digital input	V_{IL} = 0.8 V			10	µA
C_i	Input capacitance			5		pF
C_o	Output capacitance			5		pF

4.4.2 ADC Path Filter (see Note 3)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter gain relative to gain at 1020 Hz	20 Hz	−0.5	−0.15	0.2	dB
	200 Hz	−0.5	0.03	0.15	
	300 Hz to 3 kHz	−0.15	0	0.15	
	3.3 kHz	−0.35	−0.5	0.3	
	3.4 kHz	−1	−0.6	−0.1	
	4 kHz		−20	−14	
	≥ 4.6 kHz			−40	

NOTE 3: The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The analog input test signal is a sine wave with 0 dB = 6 $V_{I(PP)}$ as the reference level for the analog input signal. The passband is 0 to 3400 Hz.

4.4.3 ADC Dynamic Performance

4.4.3.1 ADC Signal-to-Noise (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise ratio (SNR)	V_I = −1 dB	80	85		dB
	V_I = −9 dB	72	77		
	V_I = −40 dB	40	45		
	V_I = −65 dB	14	21		
	$V_{I(AUXM,\ AUXP)}$ = −9 dB	72	78		

NOTE 4: The test condition is the digital equivalent of a 1020 Hz input signal with an 8 kHz conversion rate. The load impedance is 600 Ω. Input and output voltages are referred to V_{DD}/2.

4.4.3.2 ADC Signal-to-Distortion (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion (THD)	V_I = −1 dB	80	92		dB
	V_I = −9 dB	80	94		
	V_I = −40 dB	40	60		
	V_I = −65 dB	15	40		
	$V_{I(AUXM,\ AUXP)}$ = −9 dB	80	92		

NOTE 4: The test condition is the digital equivalent of a 1020 Hz input signal with an 8 kHz conversion rate. The load impedance is 600 Ω. Input and output voltages are referred to V_{DD}/2.

4.4.3.3 ADC Signal-to-Distortion+Noise (see Note 5)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total harmonic distortion+noise (THD+N)	$V_I = -9$ dB	80	83		dB
	$V_I = -1$ dB	72	76		
	$V_I = -40$ dB	40	45		
	$V_I = -65$ dB	14	20		
	$V_{I(AUXM, AUXP)} = -9$ dB	72	77		

NOTE 5: The test condition is a 1020 Hz input signal with an 8 kHz conversion rate. Input and output voltages are referred to $V_{DD}/2$.

4.4.4 ADC Channel

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Dynamic range			86		dB
	Interchannel isolation		80			dB
	Gain error	$V_I = -1$ dB at 1020 Hz			±0.5	dB
	Gain error, dc	INP = 3 V, INM = 2 V		±0.6		dB
	Off-set error, ADC converter			8		mV
CMRR	Common-mode rejection ratio INM, INP or AUXM, AUXP	$V_I = 0$ dB at 1020 kHz	80			dB
	Idle channel noise (on-chip reference)				50	µV rms
R_i	Input resistance	$T_A = 25°C$	70	100		kΩ

4.4.5 DAC Path Filter (see Note 6)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter gain relative to gain at 1020 Hz	20 Hz	−0.5	0.08	0.15	dB
	200 Hz	−0.5	0.08	0.15	
	300 Hz to 3 kHz	−0.15	0.08	0.15	
	3.3 kHz	−0.35	0.11	0.3	
	3.4 kHz	−1	−.48	−0.1	
	4 kHz		−20	−14	
	≥ 4.6 kHz			−40	

NOTE 6: The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dB). The nominal differential DAC channel peak-to-peak output voltage with this input condition is 6 V. The pass band is 0 to 3600 Hz.

4.4.6 DAC Dynamic Performance

4.4.6.1 DAC Signal-to-Noise (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise ratio (SNR)	V_O = 0 dB	74	80		dB
	V_O = −9 dB	70	74		
	V_O = −40 dB	38	44		
	V_O = −65 dB	14	18		

NOTE 4: The test condition is the digital equivalent of a 1020 Hz input signal with an 8 kHz conversion rate. The load impedance is 600 Ω. Input and output voltages are referred to $V_{DD}/2$.

4.4.6.2 DAC Signal-to-Distortion (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion (THD)	V_O = 0 dB	74	84		dB
	V_O = −9 dB	74	84		
	V_O = −40 dB	40	58		
	V_O = −65 dB	18	30		

NOTE 4: The test condition is the digital equivalent of a 1020 Hz input signal with an 8 kHz conversion rate. The load impedance is 600 Ω. Input and output voltages are referred to $V_{DD}/2$.

4.4.6.3 DAC Signal-to-Distortion+Noise (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total harmonic distortion+noise (THD+N)	V_O = 0 dB	72	78		dB
	V_O = −9 dB	68	74		
	V_O = −40 dB	38	44		
	V_O = −65 dB	14	20		

NOTE 4: The test condition is the digital equivalent of a 1020 Hz input signal with an 8 kHz conversion rate. The load impedance is 600 Ω. Input and output voltages are referred to $V_{DD}/2$.

4.4.7 DAC Channel

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Dynamic range			80		dB
	Interchannel isolation		80			dB
	Gain error, 0 dB	V_O = 0 dB at 1020 Hz			±0.5	dB
	Gain error, dc	Digital input offset = 1 V dc		±0.2		dB
	Idle channel broad-band noise	See Note 7			100	μV rms
	Idle channel narrow-band noise	0 – 4 kHz, See Note 7			40	μV rms
V_{OO}	Output offset voltage at OUT (differential)	DIN = All 0s		8		mV
V_O	Analog output voltage, peak-to-peak, OUTP−OUTM (differential)	R_L = 600, With internal reference and full-scale digital input, (see Note 8)			6	V

NOTES: 7. The conversion rate is 8 kHz; the out-of-band measurement is made from 4800 Hz to $F_{MCLK}/2$.
8. The digital input to the DAC channel at DIN is in 2s complement.

4.4.8 Power Supplies, V_{DD}(ADC) = V_{DD}(DAC) = DV_{DD} = 5 V, No Load (unless otherewise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD} (ADC)	Power supply current, ADC	Operating		12	20	mA
		Power-down		400		μA
I_{DD} (DAC)	Power supply current, DAC	Operating		16	24	mA
		Power-down		2.5		mA
I_{DD} (Digital)	Power supply current, digital	Operating		2	6	mA
		Power-down		300		μA
P_D	Power dissipation	Operating		150	250	mW
		Power-down		16	30	

4.4.9 Timing Requirements (see Notes 9 and 10)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d1}	Delay time, SCLK↑ to $\overline{FS}$↓	C_L = 20 pF		10	15	ns
t_{d2}	Delay time, SCLK↑ to DOUT			6	20	
t_{su}	Setup time, DIN before SCLK↓		20			
t_h	Hold time, DIN after SCLK↓				20	
t_{en}	Enable time, $\overline{FS}$↓ to DOUT			10	25	
t_{dis}	Disable time, $\overline{FS}$↑ to DOUT Hi-Z			20		
t_{d3}	Delay time MCLK↓ to SCLK↑			25	50	

NOTES: 9. Refer to Figure 3–1 for timing diagram.
10. When $\overline{FS}$ occurs after SCLK, it shortens the MSB (D15) duration.

5 Application Information

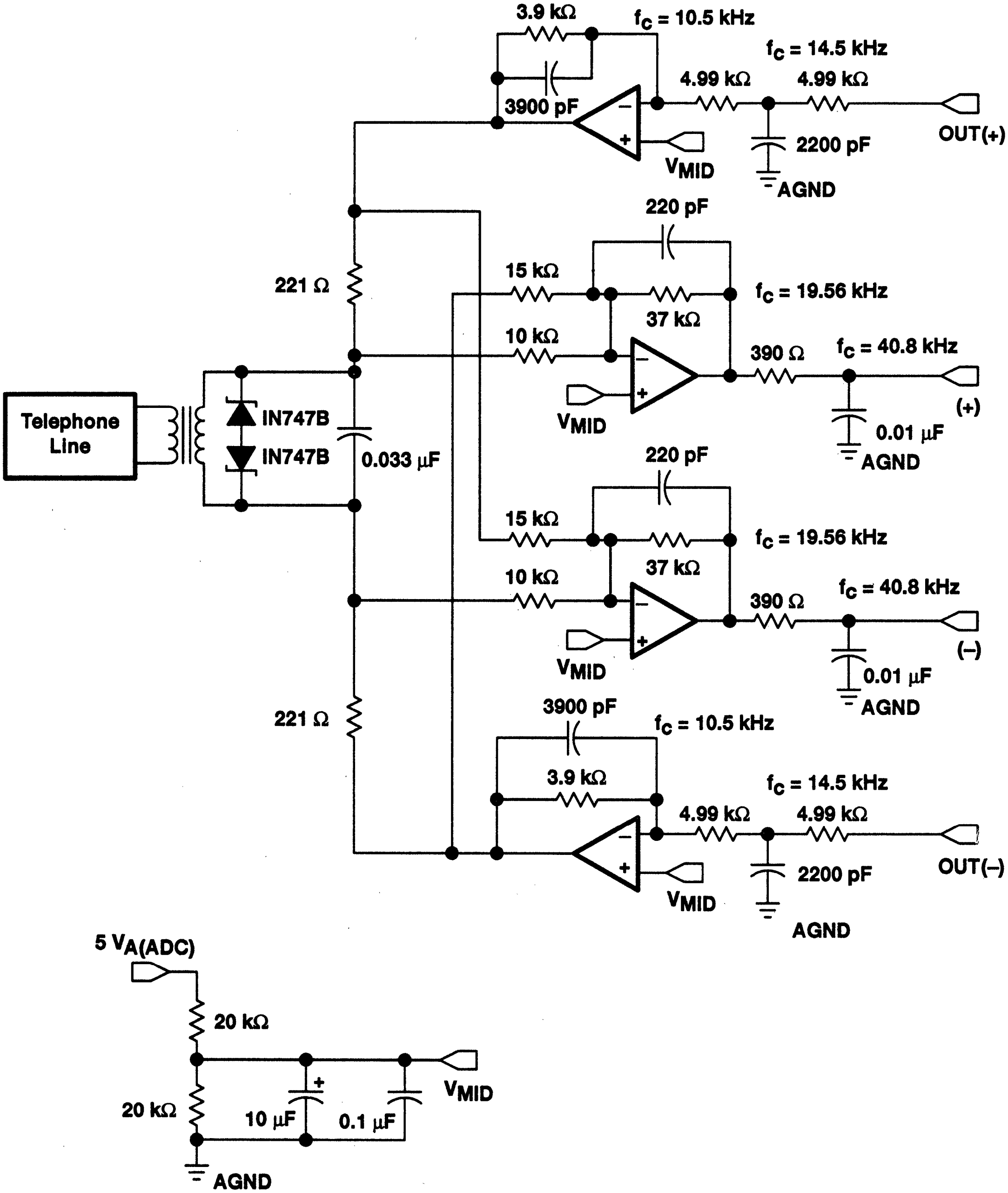


Figure 5–1. TLC320AD55C Application Schematic

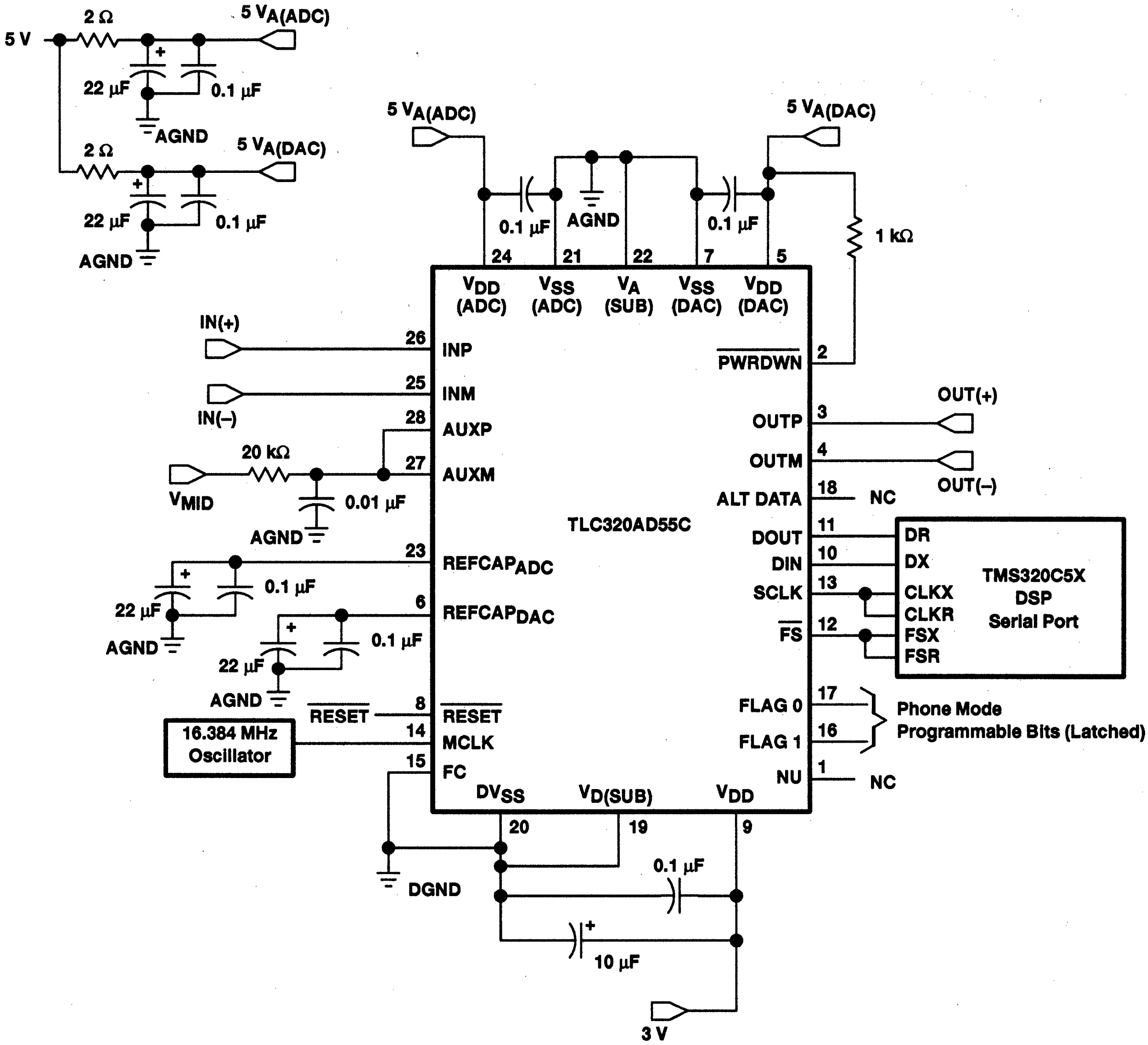


Figure 5–2. TLC320AD55C I/O Buffer and V_{MID} Generator Schematic

Appendix A
Register Set

Data bits D12 through D8 in the secondary serial communication contain the address of the register, and data bits D7 through D0 contain the data that is to be written to the register. Data bit D13 determines a read or write cycle to the addressed register. When data bit D13 is low, a write cycle is selected.

The following table shows the register map:

Table A–1. Register Map

REGISTER NO.	D15	D14	D13	D12	D11	D10	D9	D8	REGISTER NAME
0	0	0	0	0	0	0	0	0	No operation
1	0	0	0	0	0	0	0	1	Control 1
2	0	0	0	0	0	0	1	0	Control 2
3	0	0	0	0	0	0	1	1	Fk divide
4	0	0	0	0	0	1	0	0	Fsclk divide
5	0	0	0	0	0	1	0	1	Control 3

Table A–2. Control 1 Register

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1	–	–	–	–	–	–	–	Software reset
0	–	–	–	–	–	–	–	Software reset not asserted
–	1	–	–	–	–	–	–	Software power down (analog and filters)
–	0	–	–	–	–	–	–	Software power down (not asserted)
–	–	1	–	–	–	–	–	Select AUXP and AUXM
–	–	0	–	–	–	–	–	Select INP and INM
–	–	–	0	0	–	–	–	Analog output gain = 1
–	–	–	0	1	–	–	–	Analog output gain = 1/2
–	–	–	1	0	–	–	–	Analog output gain = 1/4
–	–	–	1	1	–	–	–	Analog output gain = 0 (squelch)
–	–	–	–	–	1	–	–	Analog loopback asserted
–	–	–	–	–	0	–	–	Analog loopback not asserted
–	–	–	–	–	–	1	–	Digital loopback asserted
–	–	–	–	–	–	0	–	Digital loopback not asserted
–	–	–	–	–	–	–	1	16-bit mode (hardware secondary requests)
–	–	–	–	–	–	–	0	Not 16-bit mode (software secondary requests)

Default register value: 00000000

The software reset is a one-shot operation and this bit is cleared to zero after reset. It is not necessary to write a zero to end the master reset operation.

Table A–3. Control 2 Register

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
X	X	–	–	–	–	–	–	Reserved
–	–	X	–	–	–	–	–	Decimator FIR overflow flag (valid only during read cycle)
–	–	–	X	–	–	–	–	FLAG 1 output value
–	–	–	–	X	–	–	–	FLAG 0 output value
–	–	–	–	–	1	–	–	Phone mode enabled
–	–	–	–	–	0	–	–	Phone mode disabled
–	–	–	–	–	–	0	–	Normal operation with decimator FIR filter
–	–	–	–	–	–	1	–	Bypass decimator FIR filter
–	–	–	–	–	–	–	0	Normal operation with interpolator filter
–	–	–	–	–	–	–	1	Bypass interpolator FIR filter

Default register value: 00000000

Writing zeros to the reserved bits is suggested.

Table A–4. Fk Divide Register

D7	D6	D5	D4	D3	D2	D1	D0	DIVIDE VALUE
1	1	1	1	1	1	1	1	255
		⋮				⋮		
1	0	0	0	0	0	0	0	128
		⋮				⋮		
0	0	1	0	0	0	0	0	32
		⋮				⋮		
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	256

Default register value: 00001000

The oversampling clock (FCLK) is set as MCLK/(Fk × 4). MCLK/(Fk × 256) is the sample frequency (conversion rate) for the converter. When Fk is programmed to zero, its value is interpreted as 256.

Table A–5. Fsclk Divide Register

D7	D6	D5	D4	D3	D2	D1	D0	DIVIDE VALUE
1	1	1	1	1	1	1	1	255
		⋮				⋮		
1	0	0	0	0	0	0	0	128
		⋮				⋮		
0	0	1	0	0	0	0	0	32
		⋮				⋮		
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	256

Default register value: 00001000

SCLK is set by MCLK/(2 × Fsclk). SCLK is for the serial transfer of data to and from the TLC320AD55C. When Fsclk is programmed to zero, its value is interpreted as 256.

Table A–6. Control 3 Register

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
0	0	0	0	1	0	0	0	DAC reference disabled
0	0	0	0	0	0	0	0	DAC reference enabled

TLC320AD57C Data Manual

Sigma-Delta Stereo Analog-to-Digital Converter

TEXAS INSTRUMENTS

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Contents

List of Illustrations

List of Tables

1 Introduction

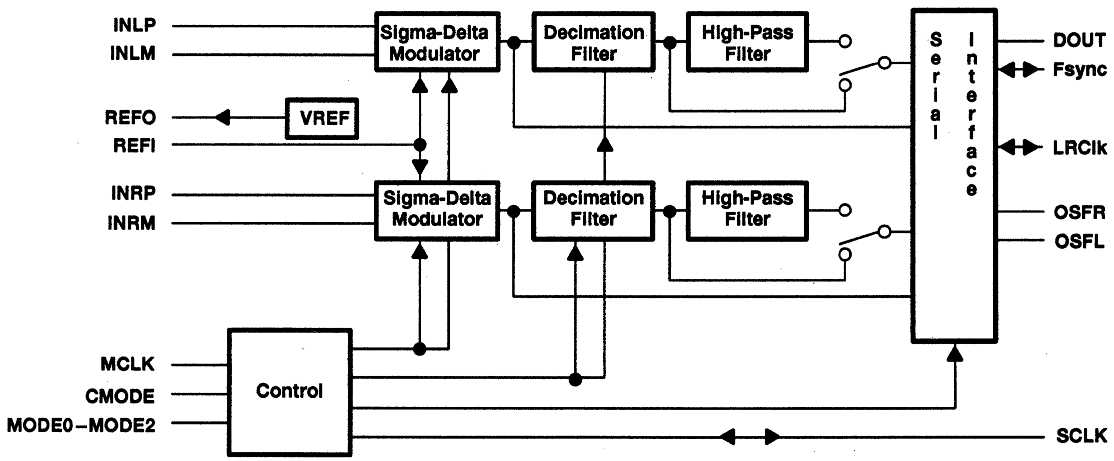
The TLC320AD57C provides high-resolution signal conversion from analog to digital using oversampling sigma-delta technology. This device consists of two synchronous conversion paths. Also included is a decimation filter after the modulator as shown in the functional block diagram. Other functions provide analog filtering and on-chip timing and control.

A functional block diagram of the TLC320AD57C is included in section 1.2. Each block is described in the Detailed Description section.

1.1 Features

- Single 5-V Power Supply
- Sample Rates (f_s) up to 48 kHz
- 18-Bit Resolution
- Signal-to-Noise (EIAJ) of 97 dB
- Dynamic Range of 95 dB
- Total Signal-to-Noise+Distortion of 91 dB
- Internal Reference Voltage (V_{ref})
- Serial Port Interface
- Differential Architecture
- Power Dissipation of 200 mW. Power-Down Mode for Low-Power Applications
- One Micron Advanced LinEPIC1Z™ Process

1.2 Functional Block Diagram



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1.3 Terminal Assignments

DW PACKAGE
(TOP VIEW)

INLP	1	28	INRP
INLM	2	27	INRM
REFI	3	26	REFO
AV_{DD}	4	25	LGND
AV_{SS}	5	24	Vlogic
AnaPD	6	23	NC
HPByp	7	22	MODE1
MODE2	8	21	OSFR
OSFL	9	20	MCLK
DigPD	10	19	DV_{SS}
TEST	11	18	DV_{DD}
CMODE	12	17	Fsync
MODE0	13	16	DOUT
LRClk	14	15	SCLK

NC – No internal connection

1.4 Ordering Information

T_A	PACKAGE SMALL OUTLINE (DW)
0°C to 70°C	TLC320AD57CDW

1.5 Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AnaPD	6	I	Analog power-down mode. The analog power-down mode disables the analog modulators. The single-bit modulator outputs become invalid, which renders the outputs of the digital filters invalid. When AnaPD is pulled low, normal operation of the device resumes.
AV_{DD}	4	I	Analog supply voltage
AV_{SS}	5	I	Analog ground
CMODE	12	I	Clock mode. CMODE selects between two methods of determining the master clock frequency. When CMODE is high, the master clock input is 384× the conversion frequency. When CMODE is low, the master clock input is 256× the conversion frequency.
DOUT	16	O	Data output. DOUT transmits the sigma-delta audio analog-to-digital converter (ADC) output data to a digital signal processor (DSP) serial port or other compatible serial interface and is synchronized to SCLK. DOUT is low when DigPD is high.
DV_{DD}	18	I	Digital supply voltage

1.5 Terminal Functions (Continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
DV_{SS}	19	I	Digital ground
DigPD	10	I	Digital power-down mode. The digital power-down mode shuts down the digital filters and clock generators. All digital outputs are brought to unasserted levels. When DigPD is pulled low, normal operation of the device resumes.
Fsync	17	I/O	Frame synchronization. Fsync designates valid data from the ADC.
HPByp	7	I	High-pass filter bypass. When HPByp is high, the high-pass filter is bypassed. This allows dc analog signal conversion.
INLM	2	I	Inverting input to left analog input amplifier
INLP	1	I	Noninverting input to left analog input amplifier
INRM	27	I	Inverting input to right analog input amplifier
INRP	28	I	Noninverting input to right analog input amplifier
LGND	25	I	Logic-power-supply ground for analog modulator
LRClk	14	I/O	Left/right clock. LRClk signifies whether the serial data is associated with the left channel ADC (when high) or the right channel ADC (when low). LRClk is low when DigPD is high.
MCLK	20	I	Master clock. MCLK derives all of the key logic signals of the sigma-delta audio ADC. The nominal input frequency range is 18.432 MHz to 256 kHz.
MODE0–MODE2	8, 13, 22	I	Serial modes. MODE0–MODE2 configure this device for many different modes of operation. The different configurations are: Master versus slave 16 bit versus 18 bit MSB first versus LSB first Slave: Fsync controlled versus Fsync high Each of these modes is described in the Serial Interface section with timing diagrams. MODE 0 1 2 — MASTER/SLAVE — BITS — MSB/LSB FIRST 0 0 0 — slave — up to 18 — MSB 0 0 1 — slave — 18 — LSB 0 1 0 — slave — up to 18 — MSB 0 1 1 — master — 16 — MSB 1 0 0 — master — 18 — MSB 1 0 1 — master — 18 — LSB 1 1 0 — master — 16 — MSB 1 1 1 — master — 16 — LSB
OSFL, OSFR	9, 21	O	Over scale flag left/right. If the left/right channel analog input exceeds the full scale input range for two consecutive conversions, OSFL and OSFR are set high for 4096 LRClk periods. OSFL and OSFR are low when DigPD is high.
SCLK	15	I/O	Shift clock. If SCLK is confirgured as an input, SCLK clocks serial data out of the sigma-delta audio ADC. If SCLK is configured as an output, SCLK stops clocking when DigPD is high.
TEST	11	I	Test mode. TEST should be low for normal operation.
REFI	3	I	Input voltage for modulator reference (normally connected to REFO, terminal 26).
REFO	26	I	Internal voltage reference
Vlogic	24	I	Logic power supply (5 V) for analog modulator

2 Detailed Description

The following sections contain a detailed description of the TLC320AD57C.

2.1 Power-Down and Reset Functions

The following sections contain descriptions of the power-down and reset functions of the TLC320AD57C.

2.1.1 Power Down

The power-down state is comprised of a separate digital and analog power down. The power consumption of each is detailed in Section 3.3, Electrical Characteristics.

The digital power-down mode shuts down the digital filters and clock generators. All digital outputs are set to an unasserted level. When the digital power-down terminal (DigPD) is pulled low, normal operation of the device is initiated.

In slave mode, the conversion process must synchronize to an input on the LRClk terminal and the SCLK terminal. Therefore, the conversion process is not initiated until the first rising edges on both SCLK and LRClk are detected after DigPD is pulled low. This synchronizes the conversion cycle. All conversions are performed at a fixed LRClk rate [MCLK/256 (CMODE low) or MCLK/384 (CMODE high)] after the initial synchronization. After the digital power-down terminal is brought low, the output of the digital filters remains invalid for 50 LRClk cycles [see Figures 2–1(a) and 2–1(b)].

In master mode, LRClk is an output; therefore, the conversion process initiates based on internal timing. The first valid data out occurs as shown in Figure 2–1(c).

The analog power-down mode disables the analog modulators. The single-bit modulator outputs become invalid, which renders the outputs of the digital filters invalid. When the analog power-down terminal is brought low, the modulators are brought back online; however, the outputs of the digital filters require 50 LRClk cycles for valid results.

2.1.2 Reset Function

The conversion process is not initiated until the first rising edges on both SCLK and LRClk are detected after DigPD is pulled low. This synchronizes the conversion cycle. All conversions are performed at a fixed LRClk rate [MCLK/256 (CMODE low) or MCLK/384 (CMODE high)] after the initial synchronization.

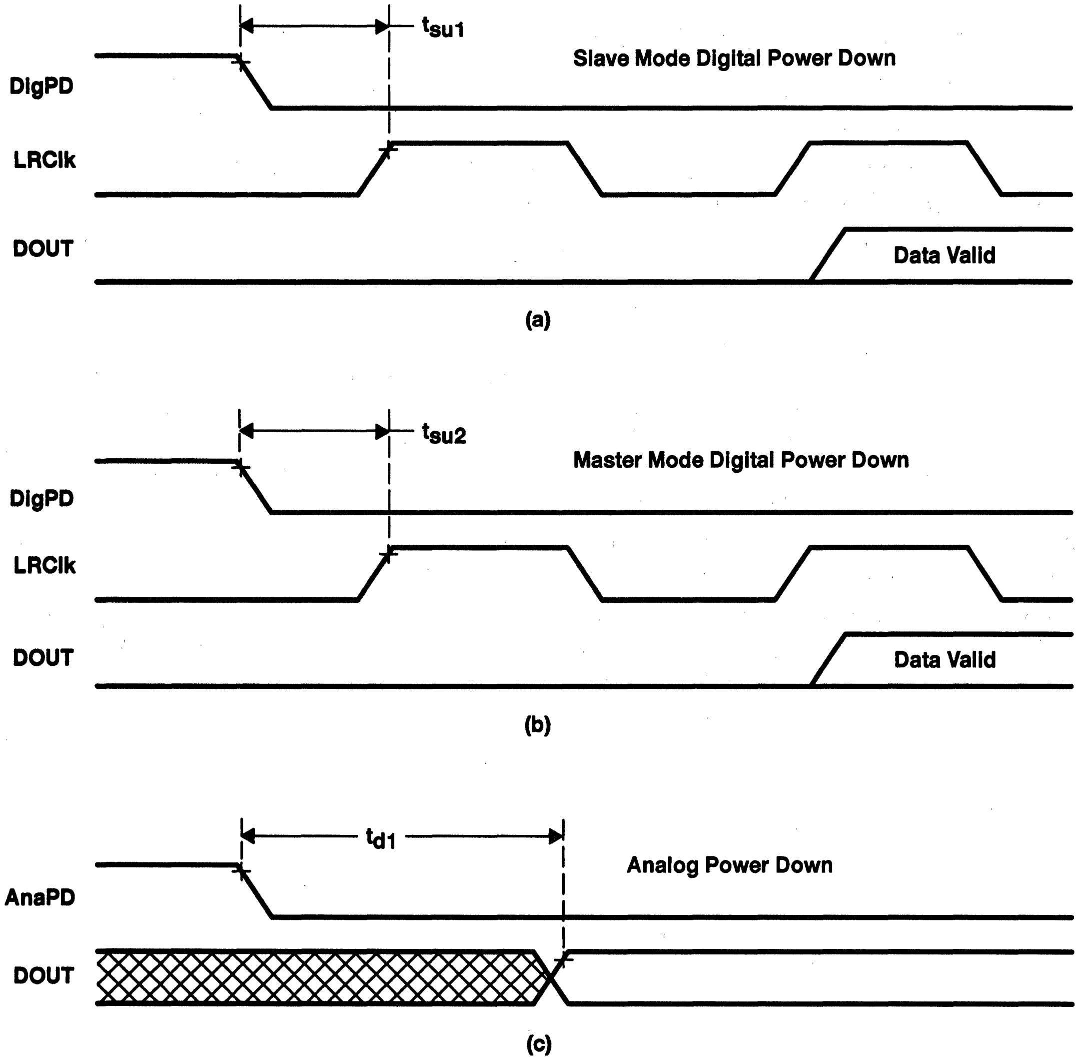

Figure 2–1. Power-Down Timing Relationships

2.2 Differential Input

The input is differential in order to provide common-mode noise rejection and increase the input dynamic range. Figure 2–2 shows the analog input signals used in a differential configuration to achieve 6.4-V peak-to-peak differential swing with a 3.2-V peak-to-peak swing per input line.

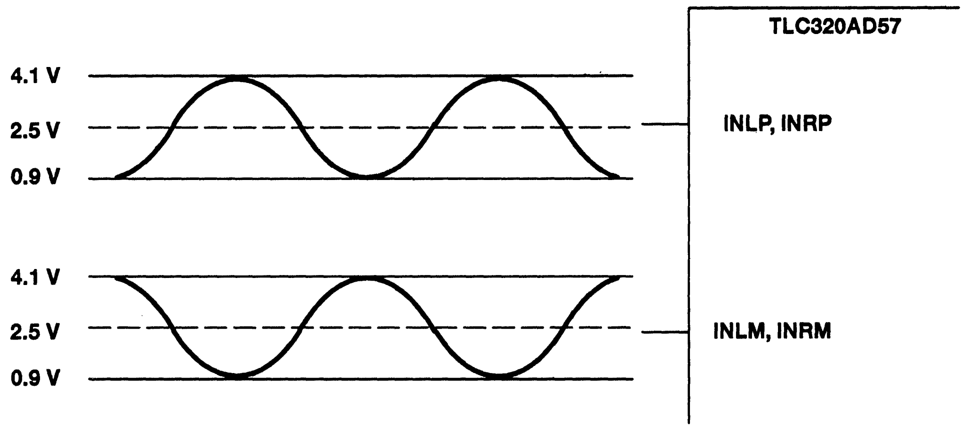

Figure 2–2. Differential Analog Input Configuration

2.3 Sigma-Delta Modulator

The modulator is a fourth order sigma-delta modulator with 64 times oversampling. The ADC provides high-resolution, low-noise performance from a one-bit converter using oversampling techniques.

2.4 Decimation Filter

The decimation filter used after the sigma-delta modulator reduces the digital data rate to the sampling rate of LRClk. This is accomplished by decimating with a ratio of 1:64. The output of this filter is a 2s complement data word of up to 18 bits serially clocked out.

If the input value exceeds the full range of the converter, the output of the decimator is held at the appropriate extreme until the input returns to within the dynamic range of the device.

2.5 High-Pass Filter

The high-pass filter removes dc from the input. With this filtering, offset calibration is not needed. The high-pass filter can be circumvented by asserting the HPByp terminal to pass dc signals through the converter. However, an offset due to the converter can be present when bypassing the high-pass filter.

2.6 Master-Clock Circuit

The master-clock circuit generates and distributes necessary clocks throughout the device. MCLK is the external master-clock input. CMODE selects the relationship of MCLK to the sample rate, LRClk. When CMODE is low, the sample rate of the data paths is set to LRClk = MCLK/256. When CMODE is high, the sample rate is set to LRClk = MCLK/384. With a fixed oversampling ratio of 64×, the effect of changing MCLK is shown in Table 2–1.

When the device is in master mode, SCLK is derived from MCLK in order to provide clocking of the serial communications between the sigma-delta audio ADC and a digital signal processor (DSP) or control logic. This is equivalent to a clock running at 64 × LRClk.

When the device is in slave mode, SCLK is externally derived.

Table 2–1. Master-Clock to Sample-Rate Comparison (modes 1, 3, 4, 5)

MCLK (MHz)	CMODE	SCLK (MHz)	LRClk (kHz)
12.2880	Low	3.0720	48
18.4320	High		
11.2896	Low	2.8224	44.1
16.9344	High		
8.1920	Low	2.0480	32
12.2880	High		
0.2560	Low	0.0640	1
0.3840	High		

2.7 Test

When the TEST input is high, the test mode is selected, which routes the high speed one-bit modulator result to the serial port output. When in the test mode, the SCLK output frequency is equal to the data output rate. LRClk is an input when the test mode is selected. This allows for the selection of the left or right modulator output to be routed to the serial port (high = left and low = right).

2.8 Serial Interface

Although the serial data is shifted out in two seperate time packets that represent the left and right channels, the inputs are sampled and converted simultaneously.

The serial interface protocol has master and slave modes each with different read-out modes. The master mode sources the control signals for conversion synchronization while the slave mode allows an external controller to provide conversion synchronization signals.

The five master modes are shown in Figures 2–3(a) through 2–3(e) and the three slave modes are shown in Figures 2–4(a) through 2–4(c). For a 16-bit word, D15 is the most significant bit and D0 is the least significant bit. Unless otherwise specified, all values are in 2s complement format.

In the master mode, SCLK is generated internally and is sourced as an output. The relationship of SCLK to LRClk is 64× (modes 1, 3, 4, 5) or 32× (modes 6, 7). In the slave mode, SCLK is an input. SCLK timing must meet the timing specifications listed in the Recommended Operating Conditions section.

2.8.1 Master Mode

As the master, the TLC320AD57C generates LRClk, Fsync, and SCLK from MCLK. These signals are provided for synchronizing the serial port of a DSP or other control devices.

Fsync designates valid data from the ADC, and accomplishes this in the master modes by one of two methods. The first method is to place a single pulse on Fsync prior to valid data. This indicates the starting point for the data. The second method of frame synchronization is to hold Fsync high during the entire valid data cycle which provides boundaries for the data.

LRClk is generated internally from MCLK. The frequency of this signal is fixed at the sampling frequency f_S [MCLK/256 (CMODE low) or MCLK/384 (CMODE high)]. During the high period of this signal, the left channel data is serially shifted to the output; during the low period, the right channel data is shifted to the output. The conversion cycle synchronizes with the rising edge of LRClk.

Five modes are available when the device is configured as a master. Two modes are for 18-bit communications. These modes differ from each other in that the MSB is transferred first in one mode while the LSB is transferred first in the second mode [see Figures 2–3(b) and 2–3(c)]. When the LSB is transferred first, the data is right justified to the LRClk [see Figures 2–3(a) through 2–3(e)]. The three other modes available as a master are 16-bit modes. Two of the modes differ as MSB first versus LSB first. These two modes set SCLK = LRClk × 32. This is one half the frequency used in the other transfer modes [see Figures 2–3(d) and 2–3(e)]. The third 16-bit mode provides the data MSB first with one clock delay after LRClk [see Figure 2–3(a)].

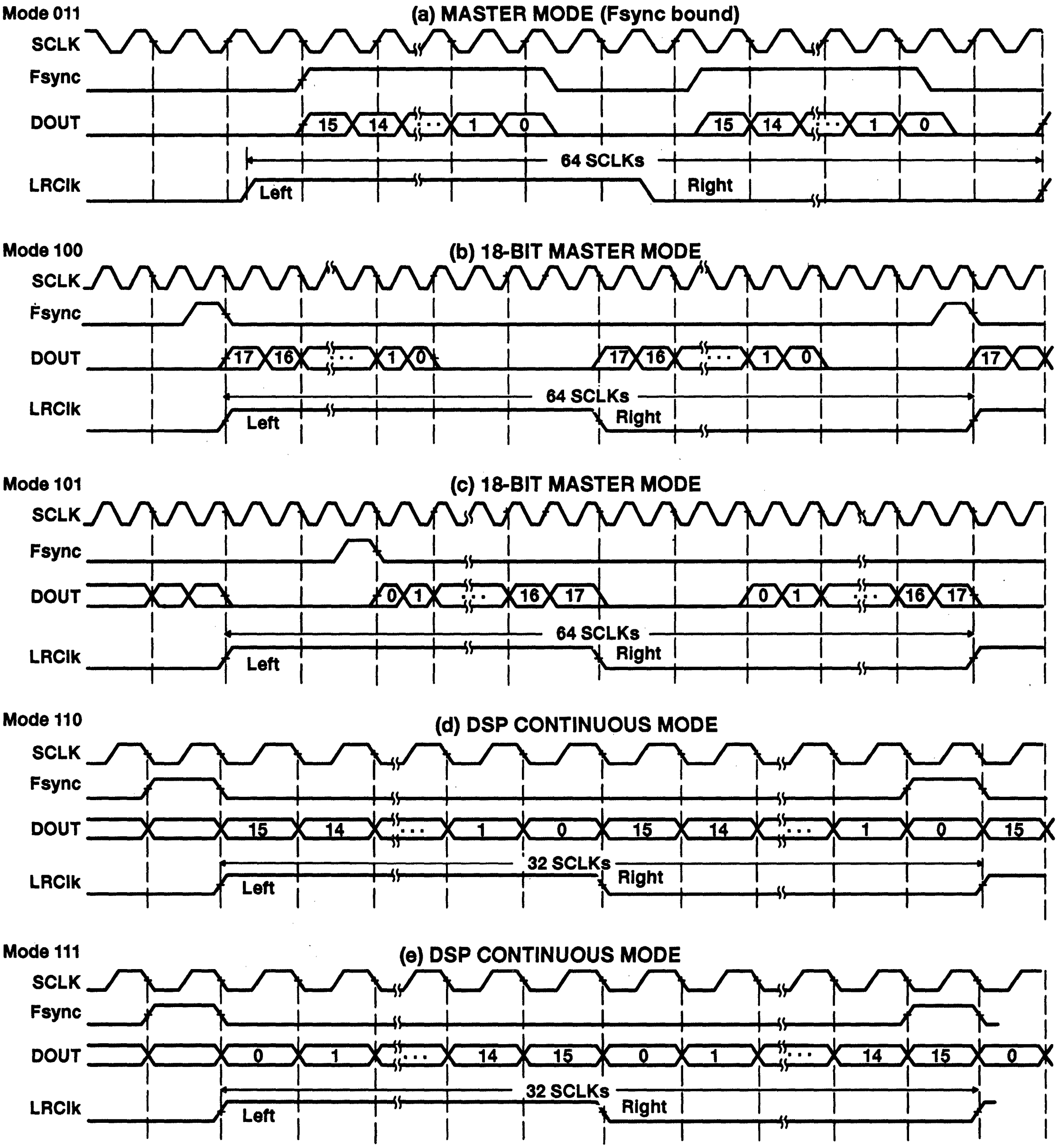

Figure 2–3. Serial Master Transfer Modes

2.8.2 Slave Mode

As a slave, the TLC320AD57C receives LRClk, Fsync, and SCLK as inputs. The conversion cycle synchronizes to the rising edge of LRClk, and the data synchronizes to the falling edge of SCLK. SCLK must meet the setup time requirements specified in Section 3.2, Recommended Operating Conditions. Synchronization of the slave modes is accomplished with the digital power-down control.

In slave mode, Fsync is an input. Three modes are provided as shown in Figures 2–4(a) through 2–4(c).

SCLK and LRClk are externally generated and sourced. The first rising edges of SCLK and LRClk after a power-down cycle initiate the conversion cycle. Refer to Section 2.8.1, Master Mode for signal functions.

Several modes are available when the TLC320AD57C is configured as a slave. Using the Mode0, Mode1, and Mode2 terminals, the TLC320AD57C can be set to shift out the MSB first or the LSB first [see Figures 2–4(a) and 2–4(b)]. The number of bits shifted out can be controlled by the number of valid SCLK cycles provided within the left or right channel period. If only enough clocks are provided to shift out 16 data bits before LRClk changes state, this is equivalent to a 16-bit mode.

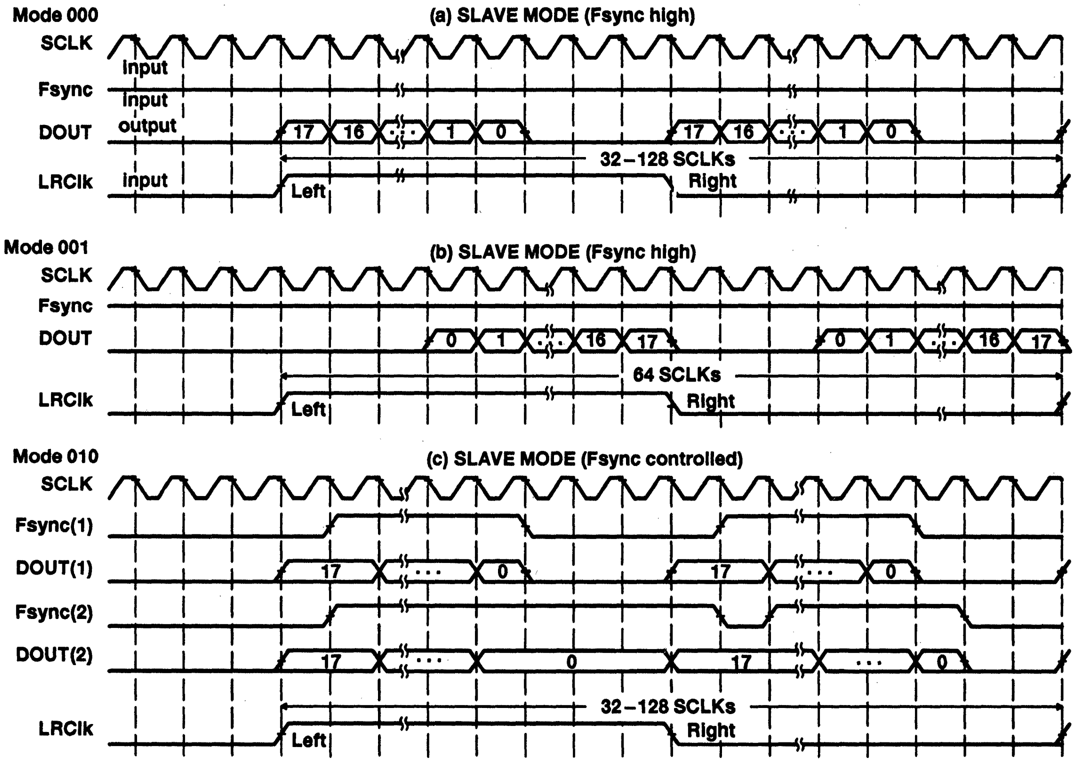

Figure 2–4. Serial Slave Transfer Modes

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Analog supply voltage range, AV_{DD} (see Note 1) .... –0.3 V to 6.5 V
Digital supply voltage range, DV_{DD} (see Note 2) .... –0.3 V to 6.5 V
Digital output voltage range, (externally applied) .... –0.3 V to DV_{DD} + 0.3 V
Digital input voltage range, MODE0 – MODE2 .... –0.3 V to DV_{DD} + 0.3 V
Analog input voltage range, INLP, INLM, INRP, INRM ...... –0.3 V to AV_{DD} + 0.3 V
Operating free-air temperature range, T_A .... 0°C to 70°C
Storage temperature range, T_{stg} .... –65°C to 150°C
Case temperature for 10 seconds, T_C .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values for maximum ratings are with respect to AV_{SS}.
2. Voltage values for maximum ratings are with respect to DV_{SS}.

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Analog supply voltage, AV_{DD} (see Note 3)	4.75	5	5.25	V
Digital supply voltage, DV_{DD}	4.75	5	5.25	V
Analog logic supply voltage, at Vlogic	4.75	5	5.25	V
Reference voltage, V_{ref}		3.2		V
Setup time, DigPD↓ to LRClk↑, slave mode, t_{su1} (see Figure 2–1(a))		30		ns
Setup time, DigPD↓ to LRClk↑, master mode, t_{su2} (see Figure 2–1(b))		30		ns
Setup time, SCLK↑ to LRClk, slave mode, t_{su3} (see Figures 4–5 and 4–6)	30			ns
Setup time, LRClk to SCLK↑, slave mode, t_{su4} (see Figure 4–5)	30			ns
Setup time, SCLK↑ to Fsync, slave mode, t_{su5} (see Figure 4–6)	30			ns
Setup time, Fsync to SCLK↑, slave mode, t_{su6} (see Figure 4–6)	30			ns
Load resistance at DOUT, R_L		10		kΩ
Operating free-air temperature, T_A	0		70	°C

NOTE 3: Voltages at analog inputs and outputs and AV_{DD} are with respect to the AV_{SS} terminal.

3.3 Electrical Characteristics

3.3.1 Digital Interface, T_A = 25°C, AV_{DD} = DV_{DD} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2	4.6		V
V_{IL}	Low-level input voltage			0.2	0.8	V
V_{OH}	High-level output voltage, DOUT	I_{OH} = 2 mA	2.4	4.6		V
V_{OL}	Low-level output voltage, DOUT	I_{OL} = 2 mA		0.2	0.4	V
I_{IH}	High-level input current, any digital input			1		µA
I_{IL}	Low-level input current, any digital input			1		µA
C_i	Input capacitance			5		pF
C_o	Output capacitance			5		pF

3.3.2 Analog Interface

3.3.2.1 ADC Modulator, T_A = 25°C, AV_{DD} = DV_{DD} = 5 V, f_s = 48 kHz, Bandwidth = 24 kHz, HPByp = 1, CMODE = 0, MODE0 – 2 = 101

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			18		Bits
DYNAMIC PERFORMANCE					
Signal to noise (EIAJ)	INLP = INRP = 2.5 V dc INLM = INRM = 2.5 V dc	93	97		dB
Dynamic range	–1dB down from 6-V differential input between INRP (INLP) and INRM (INLM)	91	95		dB
Signal to noise + distortion (THD + N)			91		dB
Total harmonic distortion (THD)			0.001%		
Interchannel isolation			108		dB
DC ACCURACY					
Gain error			±0.2		dB
Interchannel gain mismatch			±0.2		dB
Offset error (18-bit resolution)			±5		mV
Offset drift			±0.17		LSB/°C

3.3.2.2 Inputs/Supplies, T_A = 25°C, AV_{DD} = DV_{DD} = 5 V, f_s = 48 kHz, Bandwidth = 24 kHz, HPByp = 1

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Input voltage	Differential input		6.4		V
	Single-ended input		3.2		
Input impedance			50		kΩ
POWER SUPPLIES					
Power-supply current	I_{DD} (analog), operating		22	30	mA
	I_{DD} (digital), operating		24	32	mA
	I_{DD} (analog), power down		100		μA
	I_{DD} (digital), power down		40		μA
Power dissipation			230		mW

3.3.3 Channel Characteristics, T_A = 25°C, AV_{DD}=DV_{DD} = 5 V, f_s = 48 kHz, HPByp = 1

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband (–3 dB)	HPByp = 0	0.001		24	kHz
Passband ripple	30 Hz – 21.8 kHz		±0.01		dB
Stopband attenuation	26.2 kHz – 3046 kHz	80			dB
Group delay			$25/F_s$		s

3.4 Switching Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
t_{d1}	Delay time, AnaPD↓ to DOUT valid (see Figure 2–1(c))		30		ns
$t_{d(MFSD)}$	Delay time, SCLK↓ to Fsync, master mode (see Figures 4–1, 4–2, 4–3, and 4–4)	–20		20	ns
$t_{d(MDD)}$	Delay time, SCLK↓ to DOUT, master mode (see Figures 4–1, 4–2, 4–3, and 4–4)	0		50	ns
$t_{d(MIRD)}$	Delay time, SCLK↓ to LRClk, master mode (see Figures 4–2 and 4–4)	–20		20	ns
$t_{d(SDD1)}$	Delay time, LRClk to DOUT, slave mode (see Figure 4–5)			50	ns
$t_{d(SDD2)}$	Delay time, SCLK↓ to DOUT, slave mode (see Figures 4–5 and 4–6)			50	ns

4 Parameter Measurement Information

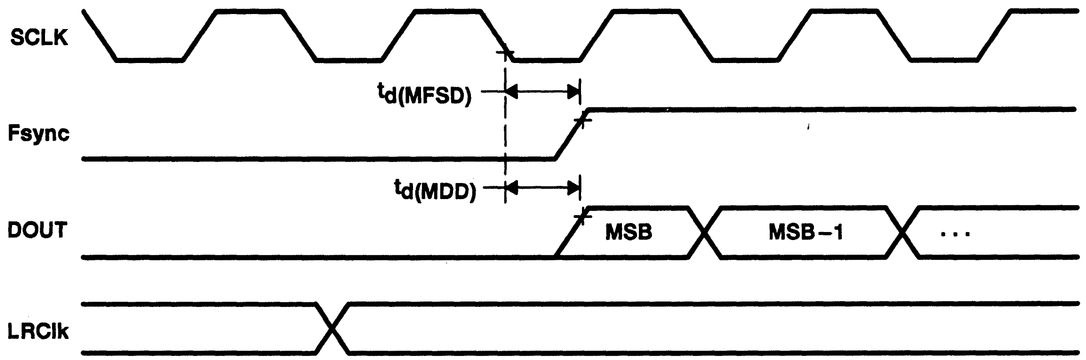

Figure 4–1. SCLK to Fsync and DOUT – Master Mode 3

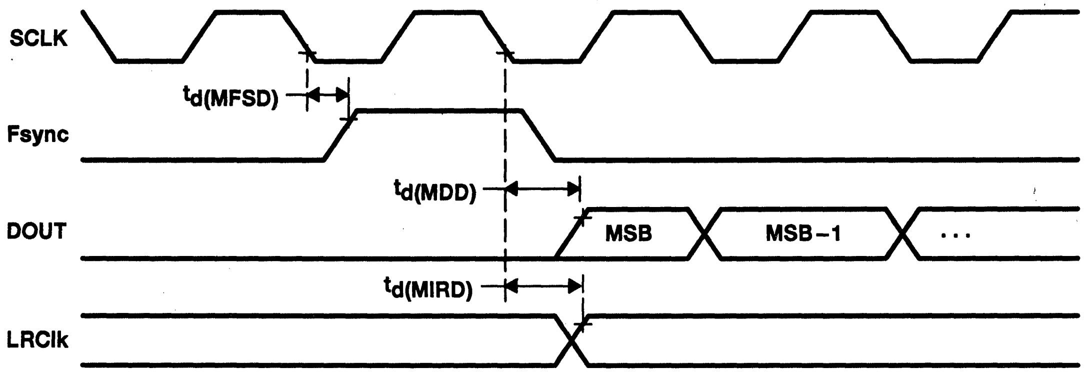

Figure 4–2. SCLK to Fsync, DOUT, and LRClk – Master Modes 4 and 6

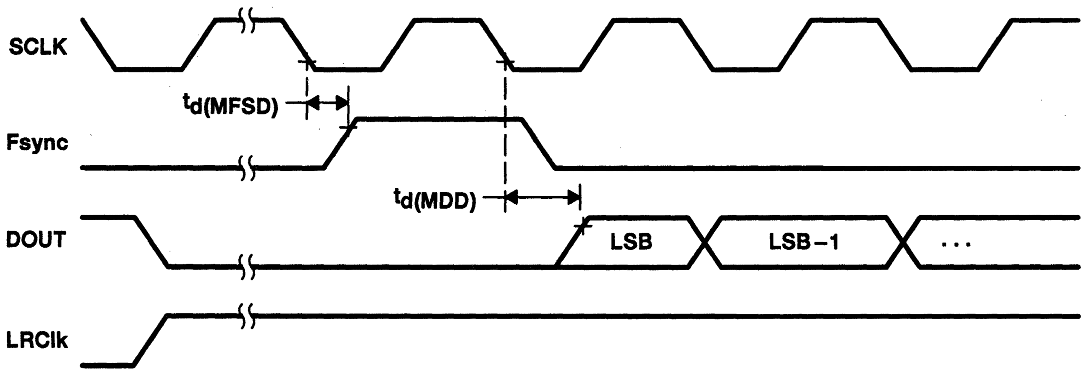

Figure 4–3. SCLK to Fsync, DOUT, and LRClk – Master Mode 5

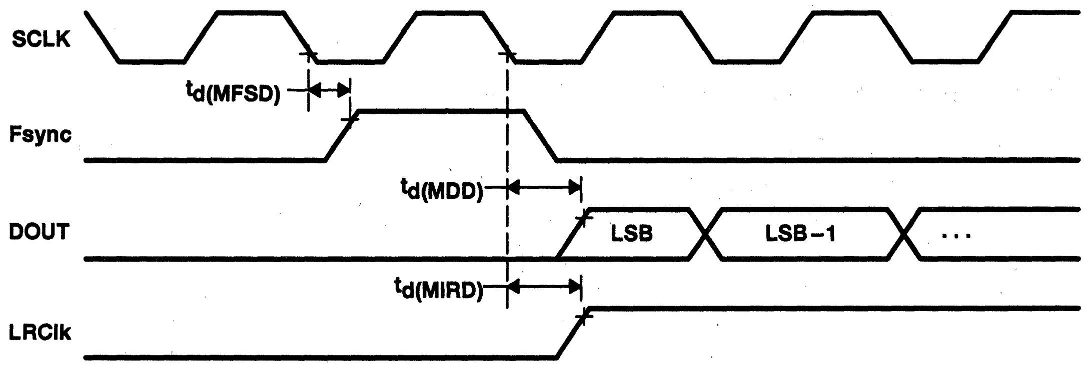

Figure 4–4. SCLK to Fsync, DOUT, and LRClk – Master Mode 7

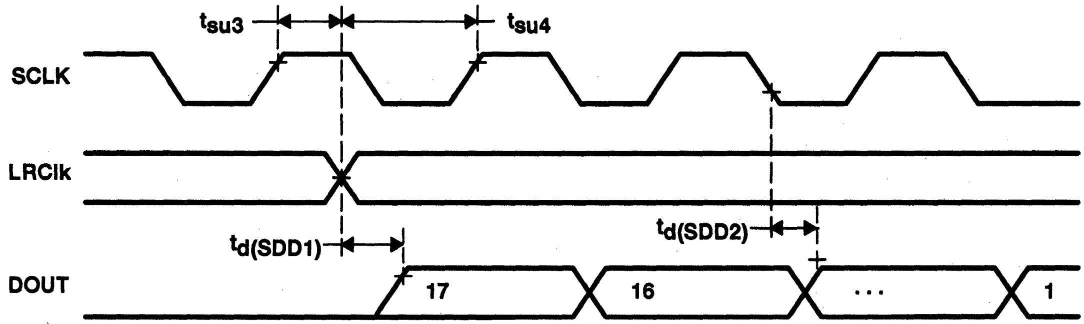

Figure 4–5. SCLK to LRClk and DOUT – Slave Mode 0, Fsync High

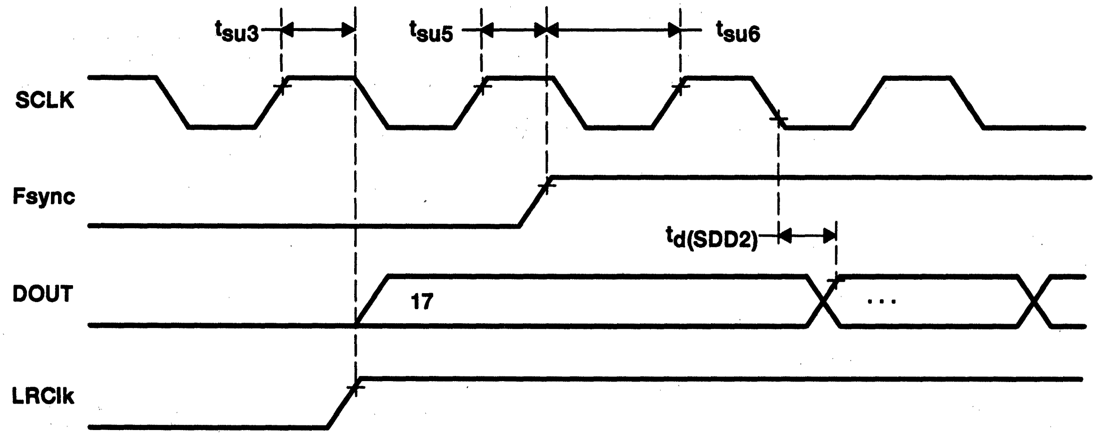

Figure 4–6. SCLK to Fsync, LRClk, and DOUT – Slave Mode 2, Fsync Controlled

TLC320AD58C Data Manual

Sigma-Delta Stereo Analog-to-Digital Converter

TEXAS INSTRUMENTS

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Contents

List of Illustrations

List of Tables

1 Introduction

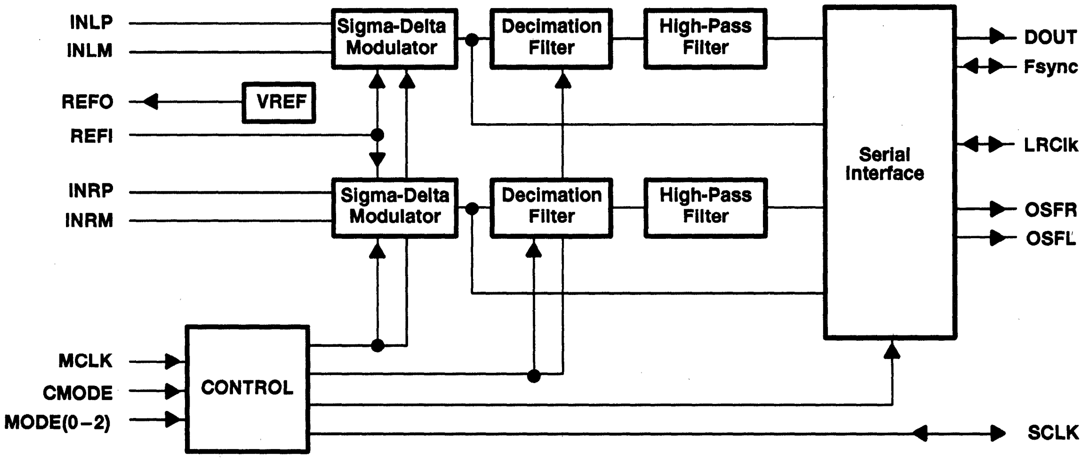
The TLC320AD58C provides high-resolution signal conversion from analog to digital using oversampling sigma-delta technology. This device consists of two synchronous conversion paths. Also included is a decimation filter after the modulator as shown in the functional block diagram. Other functions provide analog filtering and on-chip timing and control.

A functional block diagram of the TLC320AD58C is included in Section 1.2. Each block is described in the detailed description section.

1.1 Features

- Single 5-V Power Supply
- Sample Rates up to 48 kHz
- 18-Bit Resolution
- Signal-to-Noise Ratio (EIAJ) of 97 dB
- Dynamic Range of 95 dB
- Total Signal-to-Noise+Distortion of 95 dB
- Internal Reference Voltage (V_{ref})
- Serial-Port Interface
- Differential Architecture
- Power Dissipation of 200 mW. Power-Down Mode for Low-Power Applications
- One-Micron Advanced LinEPIC1Z™ Process

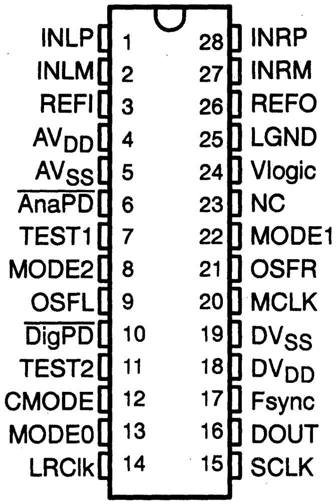
1.2 Functional Block Diagram



LinEPIC1Z is a trademark of Texas Instruments Incorporated.

1.3 Terminal Assignments

DW PACKAGE
(TOP VIEW)



NC – No internal connection

1.4 Ordering Information

T_A	PACKAGE SMALL OUTLINE (DW)
0°C to 70°C	TLC320AD58CDW

1.5 Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
$\overline{\text{AnaPD}}$	6	I	Analog power-down mode. The analog power-down mode disables the analog modulators. The single-bit modulator outputs become invalid, rendering the outputs of the digital filters invalid. When $\overline{\text{AnaPD}}$ is pulled high, normal operation of the device is resumed.
AV_{DD}	4	I	Analog supply voltage
AV_{SS}	5	I	Analog ground
CMODE	12	I	Clock mode. CMODE is used to select between two methods of determining the master clock frequency. When CMODE is high, the master clock input is 384× the conversion frequency. When CMODE is low, the master clock input is 256× the conversion frequency.
DOUT	16	O	Data output. DOUT is used to transmit the sigma-delta audio ADC output data to a DSP serial port or other compatible serial interface and is synchronized to SCLK. This output is low when $\overline{\text{DigPD}}$ is high.
DV_{DD}	18	I	Digital supply voltage
DV_{SS}	19	I	Digital ground
$\overline{\text{DigPD}}$	10	I	Digital power-down mode. The digital power-down mode shuts down the digital filters and clock generators. All digital outputs are brought to unasserted states. When $\overline{\text{DigPD}}$ is pulled high, normal operation of the device is resumed.
Fsync	17	I/O	Frame sync. Frame sync is used to designate the valid data from the ADC.

1.5 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
INLM	2	I	Inverting input to left analog input amplifier
INLP	1	I	Noninverting input to left analog input amplifier
INRM	27	I	Inverting input to right analog input amplifier
INRP	28	I	Noninverting input to right analog input amplifier
LGND	25	I	Logic power supply ground for analog modulator
LRClk	14	I/O	Left/right clock. LRClk signifies whether the serial data is associated with the left channel ADC (when LRClk is high) or the right channel ADC (when LRClk is low). LRClk is low when $\overline{\text{DigPD}}$ is low.
MCLK	20	I	Master clock. MCLK is used to derive all the key logic signals of the sigma-delta audio ADC. The nominal input frequency range is 18.432 MHz to 256 kHz.
MODE(0–2)	13, 22, 8	I	Serial modes. MODE(0–2) configure this device for many different modes of operation. The different configurations are: Master versus slave 16 bit versus 18 bit MSB first versus LSB first Slave: Fsync controlled versus Fsync high Each of these modes is described in the serial interface section along with timing diagrams. (See mode table below.)
OSFL, OSFR	9, 21	O	Over scale flag left/right. If the left/right channel digital output exceeds full scale output range for two consecutive conversions, this flag is set high for 4096 LRClk periods. OSFL and OSFR are low when $\overline{\text{DigPD}}$ is low.
SCLK	15	I/O	Shift clock. If SCLK is configured as an input, SCLK is used to clock serial data out of the sigma-delta audio ADC. If SCLK is configured as an output, SCLK stops clocking when $\overline{\text{DigPD}}$ is low.
TEST1	7	I	Test mode 1. TEST1 should be low for normal operation.
TEST2	11	I	Test mode 2. TEST2 should be low for normal operation.
REFI	3	I	Input voltage for modulator reference (normally connected to REFO, terminal 26).
REFO	26	I	Internal voltage reference
Vlogic	24	I	Logic power supply voltage (5 V) for analog modulator

MODE 0 1 2	MASTER/ SLAVE	BITS	MSB/LSB FIRST
0 0 0	slave	up to 18	MSB
0 0 1	slave	18	LSB
0 1 0	slave	up to 18	MSB
0 1 1	master	16	MSB
1 0 0	master	18	MSB
1 0 1	master	18	LSB
1 1 0	master	16	MSB
1 1 1	master	16	LSB

2 Detailed Description

The sigma-delta converter allows for simple antialias external filtering. Typically, a first order RC filter is sufficient.

2.1 Power-Down and Reset Functions

2.1.1 Power Down

The power-down state is comprised of a separate digital and analog power down. The power consumption of each is detailed in the electrical characteristics section.

The digital power-down mode shuts down the digital filters and clock generators. All digital outputs are set to an unasserted level. When the digital power-down terminal is pulled high, normal operation of the device is initiated. In slave mode, the conversion process must synchronize to an input on the LRClk terminal as well as the SCLK terminal. Therefore, the conversion process is not initiated until the first rising edges of both SCLK and LRClk are detected after $\overline{\text{DigPD}}$ is pulled high. This synchronizes the conversion cycle; all conversions are performed at a fixed LRClk rate [MCLK/256 (CMODE low) or MCLK/384 (CMODE high)] after the initial synchronization. After the digital power-down terminal is brought high, the output of the digital filters remains invalid for 50 LRClk cycles [see Figures 2–1(a) and 2–1(b)].

In master mode, LRClk is an output; therefore, the conversion process initiates based on internal timing. The first valid data out occurs as shown in Figure 2–1(c).

The analog power-down mode disables the analog modulators. The single-bit modulator outputs become invalid which renders the outputs of the digital filters invalid. When the analog power-down terminal is brought high, the modulators are brought back online; however, the outputs of the digital filters require 50 LRClk cycles for valid results.

2.1.2 Reset Function

The conversion process is not initiated until the first rising edges of both SCLK and LRClk are detected after $\overline{\text{DigPD}}$ is pulled high. This synchronizes the conversion cycle; all conversions are performed at a fixed LRClk rate [MCLK/256 (CMODE low) or MCLK/384 (CMODE high)] after the initial synchronization.

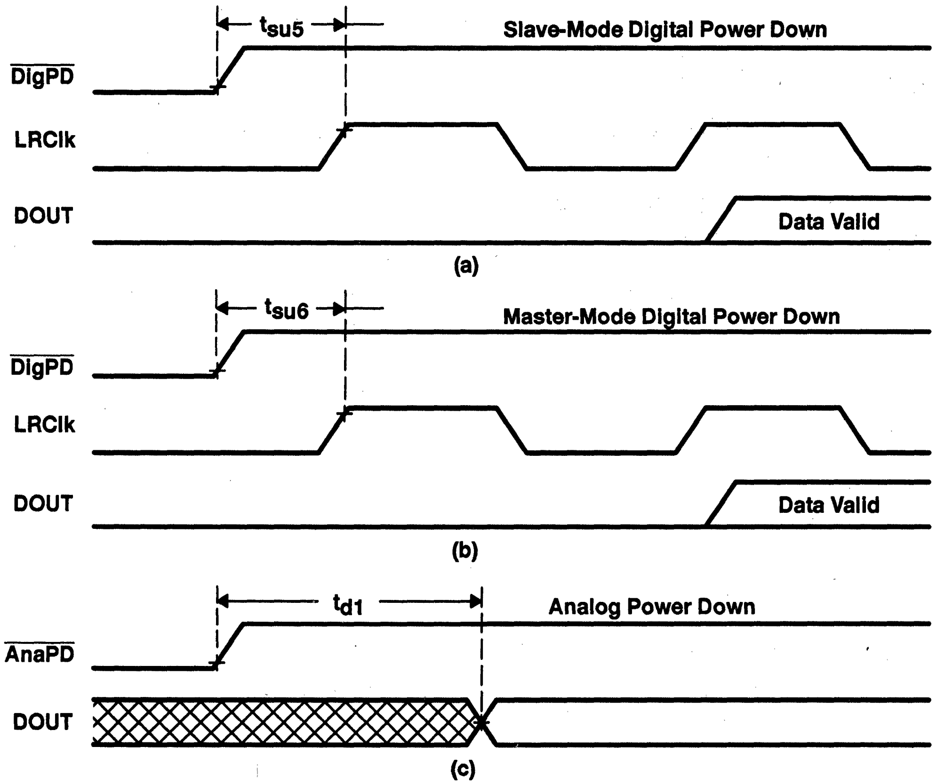


Figure 2–1. Power-Down Timing Relationships

2.2 Differential Input

The input is differential in order to provide common-mode noise rejection and increase the input dynamic range. Figure 2–2 shows the analog input signals used in a differential configuration to achieve a 6.4 $V_{I(PP)}$ differential swing with a 3.2 $V_{I(PP)}$ swing per input line. Both a differential and a single-ended configuration are shown in the application information section.

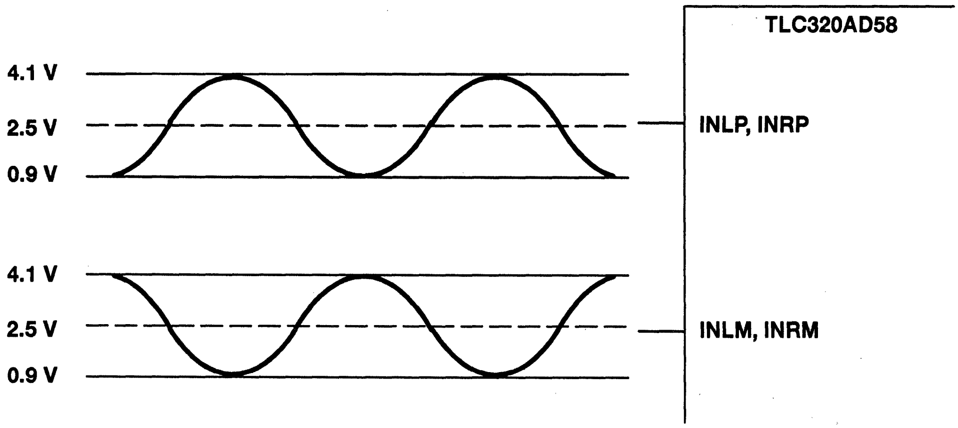


Figure 2–2. Differential Analog Input Configuration

2.3 Sigma-Delta Modulator

The modulator is a fourth-order sigma-delta modulator with 64 times oversampling. The ADC provides high-resolution, low-noise performance from a one-bit converter using oversampling techniques.

2.4 Decimation Filter

The decimation filter used after the sigma-delta modulator reduces the digital data rate to the sampling rate of LRClk. This is accomplished by decimating with a ratio of 1:64. The output of this filter is a 2s complement data word of up to 18 bits serially clocked out.

If the input value exceeds the full range of the converter, the output of the decimator is held at the appropriate extreme until the input returns to the dynamic range of this device.

2.5 High-Pass Filter

The high-pass filter removes dc from the input.

2.6 Master-Clock Circuit

The master-clock circuit is used to generate and distribute necessary clocks throughout the device. MCLK is the external master clock input. CMODE is used to select the relationship of MCLK to the sample rate of LRClk. When CMODE is low, the sample rate of the data paths is set as LRClk = MCLK/256. When CMODE is high, the sample rate is set as LRClk = MCLK/384. With a fixed oversampling ratio of 64×, the effect of changing MCLK is shown in Table 2–1.

When the TLC320AD58C is in master mode, SCLK is derived from MCLK in order to provide clocking of the serial communications between the sigma-delta audio ADC and a digital signal processor (DSP) or control logic. This is equivalent to a clock running at 64 × LRClk.

When the TLC320AD58C is in slave mode, SCLK is externally derived.

Table 2–1. Master-Clock to Sample-Rate Comparison (Modes 1, 3, 4, 5)

MCLK (MHz)	CMODE	SCLK (MHz)	LRClk (kHz)
12.2880	Low	3.0720	48
18.4320	High		
11.2896	Low	2.8224	44.1
16.9344	High		
8.1920	Low	2.0480	32
12.2880	High		
0.2560	Low	0.0640	1
0.3840	High		

2.7 Test

TEST1 and TEST2 are reserved for factory test and should be tied to digital ground (DV_{SS}).

2.8 Serial Interface

Although the serial data is shifted out in two seperate time packets that represent the left and right channels, the inputs are sampled and converted simultaneously.

The serial interface protocol has master and slave modes each with different read out modes. The master mode is used to source the control signals for conversion synchronization, while the slave mode allows an external controller to provide conversion synchronization signals.

The five master modes are shown in Figures 2–3(a) through 2–3(e), and the three slave modes are shown in Figures 2–4(a) through 2–4(c). For a 16-bit word, D15 is the most significant bit and D0 is the least significant bit. Unless otherwise specified, all values are in 2s complement format.

In master mode, SCLK is generated internally and is sourced as an output. The relationship of SCLK to LRClk is 64× (modes 1, 3, 4, 5) or 32× (modes 6, 7). In slave mode, SCLK is an input. SCLK timing must meet the timing specifications shown in the recommended operating conditions section.

2.8.1 Master Mode

As the master, the TLC320AD58C generates LRClk, Fsync, and SCLK from MCLK. These signals are provided for synchronizing the serial port of a digital signal processor (DSP) or other control devices.

Fsync is used to designate the valid data from the ADC, and this is accomplished in the master modes by one of two methods. The first is a single pulse on Fsync prior to valid data. This indicates the starting point for the data. The second method of frame synchronization is to hold Fsync high during the entire valid data cycle, which provides boundaries for the data.

LRClk is generated internally from MCLK. The frequency of this signal is fixed at the sampling frequency f_S [MCLK/256 (CMODE low) or MCLK/384 (CMODE high)]. During the high period of this signal, the left channel data is serially shifted to the output; during the low period, the right channel data is shifted to the output. The conversion cycle is synchronized with the rising edge of LRClk.

Five modes are available when the device is configured as a master. Two modes are for 18-bit communications. These modes differ from each other in that the MSB is transferred first in one mode while the LSB is transferred first in the second mode [see Figures 2–3(b) and 2–3(c)]. When the LSB is transferred first, the data is right justified to the LRClk [see Figures 2–3(a) through 2–3(e)]. The three other master modes are 16-bit modes. Once again, two of the modes differ as MSB first versus LSB first. These two modes set SCLK = LRClk × 32. This is half the frequency used in the other transfer modes [see Figures 2–3(d) and 2–3(e)]. The third 16-bit mode provides the data MSB first with one clock delay after LRClk [see Figure 2–3(a)].

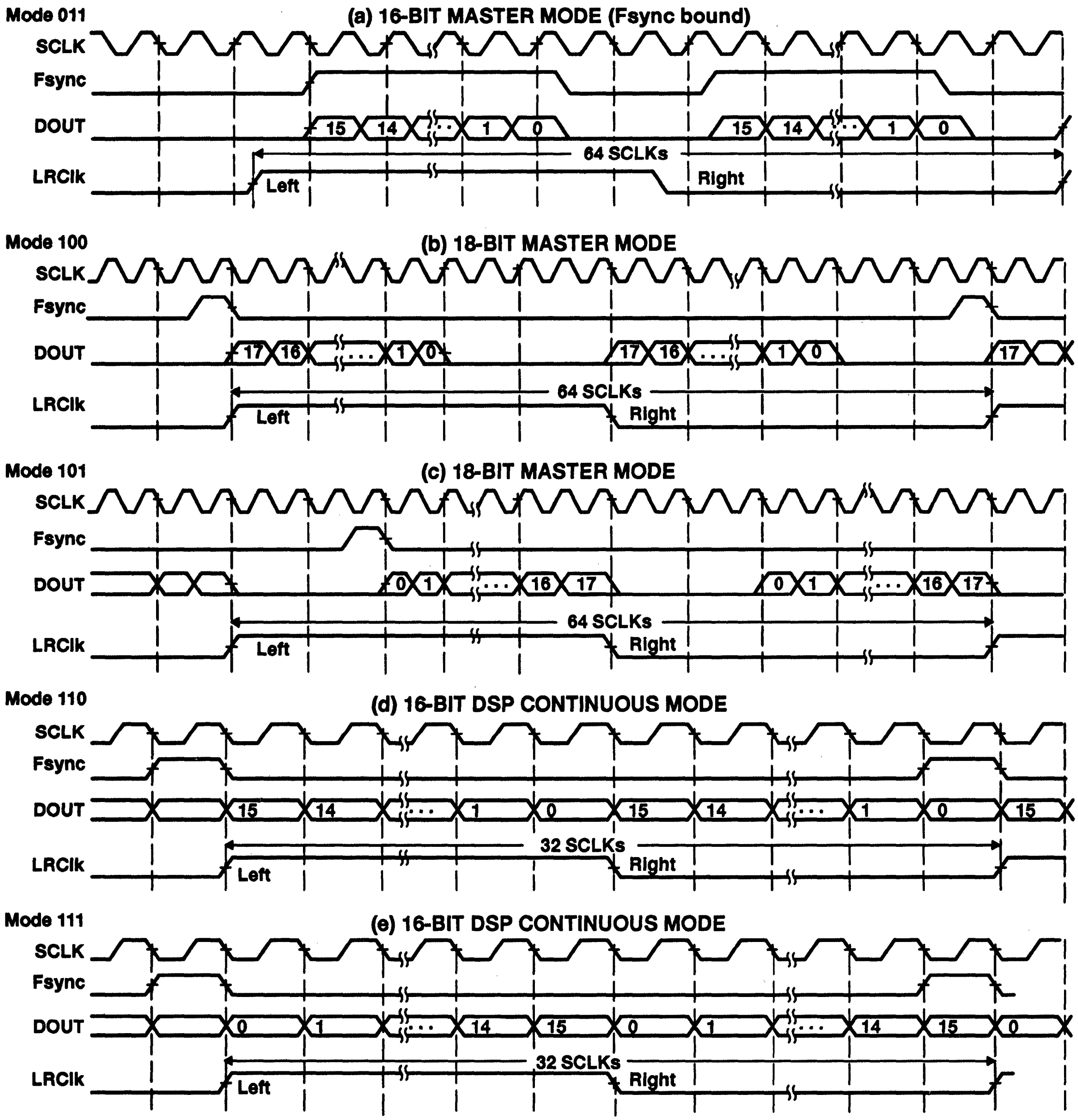


Figure 2–3. Serial Master Transfer Modes

2.8.2 Slave Mode

As a slave, the TLC320AD58C receives LRClk, Fsync, and SCLK as inputs. The conversion cycle is synchronized to the rising edge of LRClk, and the data is synchronized to the falling edge of SCLK. SCLK must meet the setup requirements specified in the recommended operating conditions section. Synchronization of the slave modes is accomplished with the digital power-down control.

In slave mode, Fsync is an input. Three modes are provided as shown in Figures 2–4(a) through 2–4(c).

SCLK and LRClk are externally generated and sourced. The first rising edges of SCLK and LRClk after a power-down cycle initiate the conversion cycle. Refer to the master-mode section for signal functions.

Several modes are available when the TLC320AD58C is configured as a slave. Using the Mode0, Mode1, and Mode2 terminals, the TLC320AD58C can be set to shift out the MSB first or the LSB first [see Figures 2–4(a) and 2–4(b)]. The number of bits shifted out, however, can be controlled by the number of valid SCLK cycles provided within the left or right channel period. If only enough clocks are provided to shift out 16 data bits before LRClk changes state, then this is equivalent to a 16-bit mode. Modes 1 and 2 both require 64 SCLK periods per LRClk period.

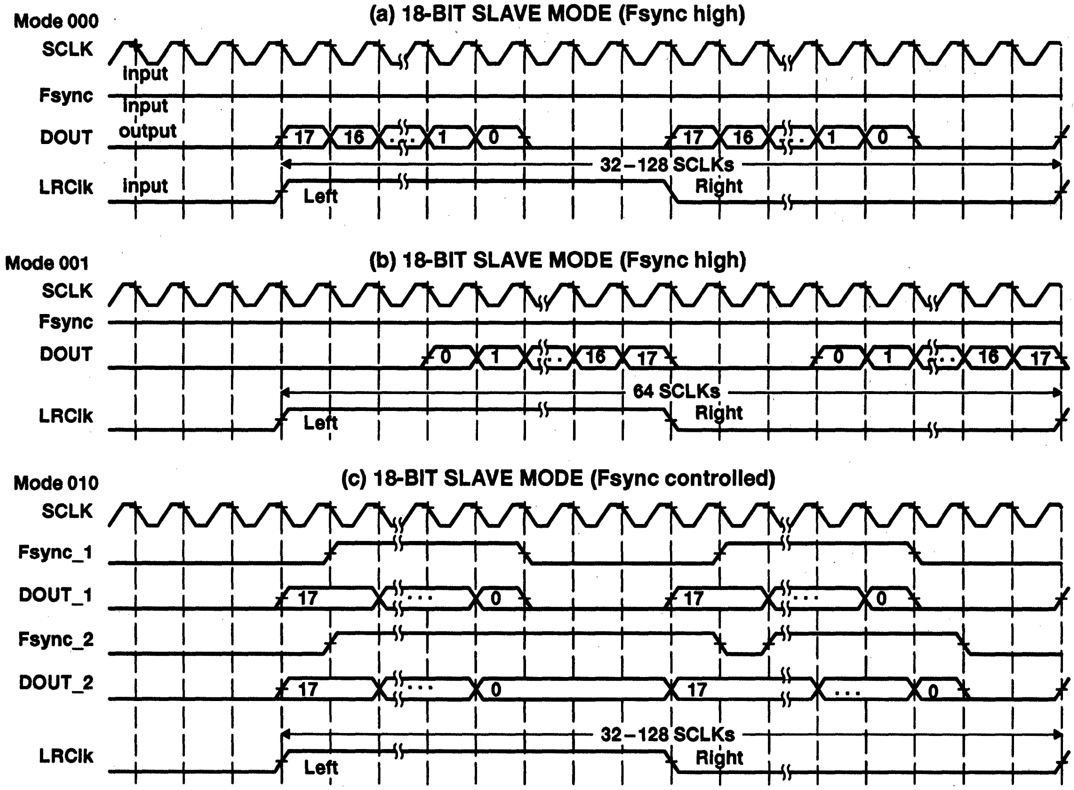


Figure 2–4. Serial Slave Transfer Modes

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage range, AV_{DD} (see Note 1) .... −0.3 V to 6.5 V
Supply voltage range, DV_{DD} (see Note 2) .... −0.3 V to 6.5 V
Analog input voltage range, INLP, INLM, INRP, INRM .... −0.3 V to 6.5 V
Operating free-air temperature range, T_A .... −0°C to 70°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Case temperature for 10 seconds .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values for maximum ratings are with respect to AV_{SS}.
2. Voltage values for maximum ratings are with respect to DV_{SS}.

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Analog supply voltage, AV_{DD} (see Note 3)	4.75	5	5.25	V
Digital supply voltage, DV_{DD}	4.75	5	5.25	V
Analog logic supply voltage, Vlogic	4.75	5	5.25	V
Reference voltage, V_{ref}		3.2		V
Setup time, SCLK↑ to LRClk, slave mode, t_{su1}	30			ns
Setup time, LRClk to SCLK↑, slave mode, t_{su2}	30			ns
Setup time, SCLK↑ to Fsync, slave mode, t_{su3}	30			ns
Setup time, Fsync to SCLK↑, slave mode, t_{su4}	30			ns
Setup time, $\overline{\text{DigPD}}$ to LRClk↑, slave mode, t_{su5}		30		ns
Setup time, $\overline{\text{DigPD}}$ to LRClk↑, master mode, t_{su6}		30		ns
Load resistance at DOUT, R_L		10		kΩ
Input dc offset range	−50	0	50	mV
Operating free-air temperature, T_A	0		70	°C

NOTE 3: Voltages at analog inputs and outputs and AV_{DD} are with respect to the AV_{SS} terminal.

3.3 Electrical Characteristics

3.3.1 Digital Interface, T_A = 25°C, AV_{DD} = DV_{DD} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2	4.6		V
V_{IL}	Low-level input voltage			0.2	0.8	V
V_{OH}	High-level output voltage at DOUT	I_{OH} = 2 mA	2.4	4.6		V
V_{OL}	Low-level output voltage at DOUT	I_{OL} = 2 mA		0.2	0.4	V
I_{IH}	High-level input current, any digital input			1		µA
I_{IL}	Low-level input current, any digital input			1		µA
C_i	Input capacitance			5		pF
C_o	Output capacitance			5		pF

3.3.2 Analog Interface

3.3.2.1 ADC Modulator, T_A = 25°C, AV_{DD} = DV_{DD} = 5 V, f_s = 48 kHz, Bandwidth = 24 kHz, CMODE = 0, MODE(0–2) = 000

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			18		Bits
DYNAMIC PERFORMANCE	ANSI A-weighting filter				
Signal to noise (EIAJ)	INLP = INRP = 2.5 V dc INLM = INRM = 2.5 V dc	96	100		dB
Dynamic range	–1 dB down from 6-V differential input	90	95		dB
Signal to noise + distortion (THD + N)		88	93		dB
Total harmonic distortion (THD)			0.0015%		
Interchannel isolation			120		dB
DC ACCURACY					
Absolute gain error			±0.6		dB
Interchannel gain mismatch			±0.2		dB
Offset error (18-bit resolution)			120±5		mV
Offset drift			±0.17		LSB/°C

3.3.2.2 Inputs/Supplies, T_A = 25°C, AV_{DD} = DV_{DD} = 5 V, f_s = 48 kHz, Bandwidth = 24 kHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Input voltage range	(differential)		6.2		V
	(0 to peak)		3.1		V
Input impedance			200		kΩ
POWER SUPPLIES					
Power-supply current	I_{DD} (analog), normal mode		24	32	mA
	I_{DD} (digital), normal mode		26	32	mA
	I_{DD} (analog), power down		250		µA
	I_{DD} (digital), power down		150		µA
Power dissipation			250		mW

3.3 Electrical Characteristics (Continued)

3.3.3 Channel Characteristics, T_A = 25°C, AV_{DD} = DV_{DD} = 5 V, f_s = 48 kHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband (−3 dB)		0.001		24	kHz
Passband ripple	30 Hz – 21.8 kHz		±0.01		dB
Stopband attenuation	26.2 kHz – 3046 kHz	80			dB
Group delay			$25/f_s$		s

3.4 Switching Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
t_{d1}	Delay time, $\overline{\text{AnaPD}}$ to DOUT valid		30		ns
$t_{d(MFSD)}$	Delay time, SCLK↓ to Fsync, master mode	−20		20	ns
$t_{d(MDD)}$	Delay time, SCLK↓ to DOUT, master mode	0		50	ns
$t_{d(MIRD)}$	Delay time, SCLK↓ to LRClk, master mode	−20		20	ns
$t_{d(SDD1)}$	Delay time, LRClk to DOUT, slave mode			50	ns
$t_{d(SDD2)}$	Delay time, SCLK↓ to DOUT, slave mode			50	ns

4 Parameter Measurement Information

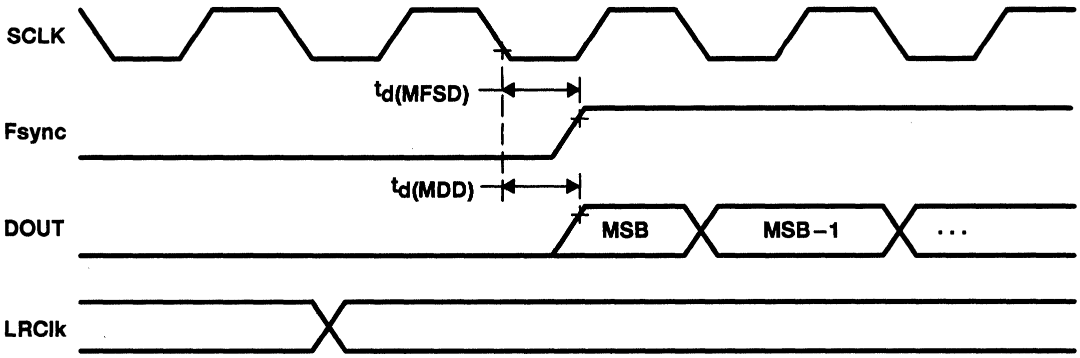


Figure 4–1. SCLK to Fsync and DOUT – Master Mode 3

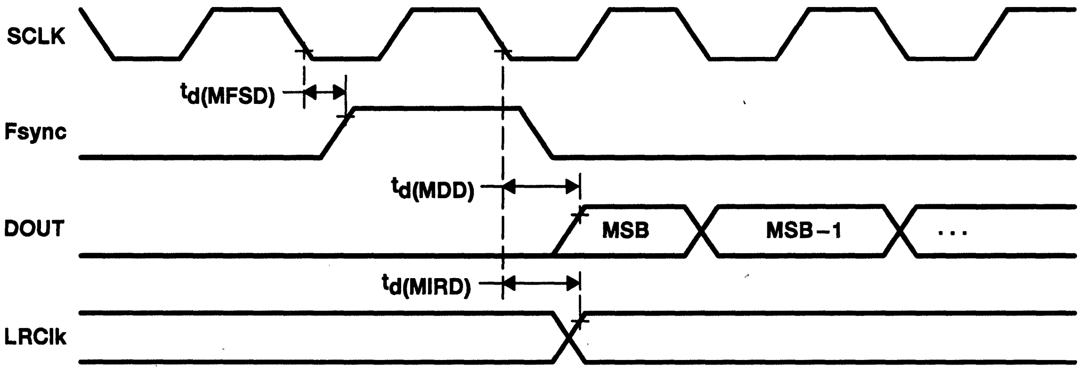


Figure 4–2. SCLK to Fsync, DOUT, and LRClk – Master Modes 4 and 6

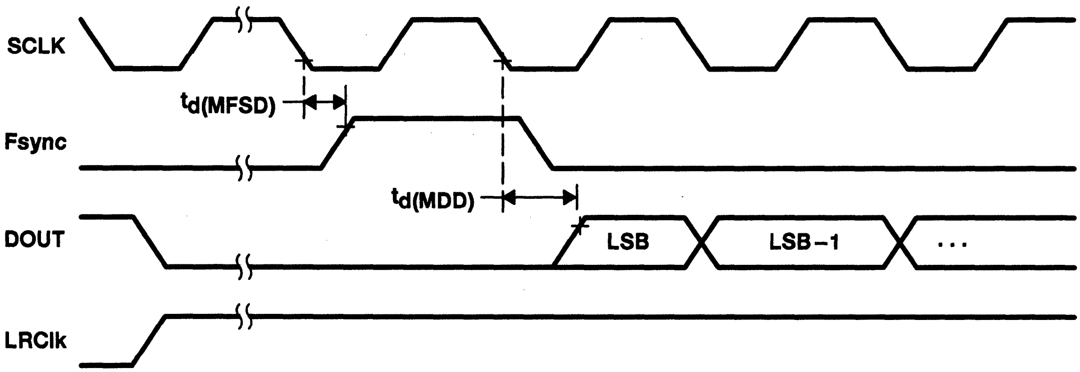


Figure 4–3. SCLK to Fsync, DOUT, and LRClk – Master Mode 5

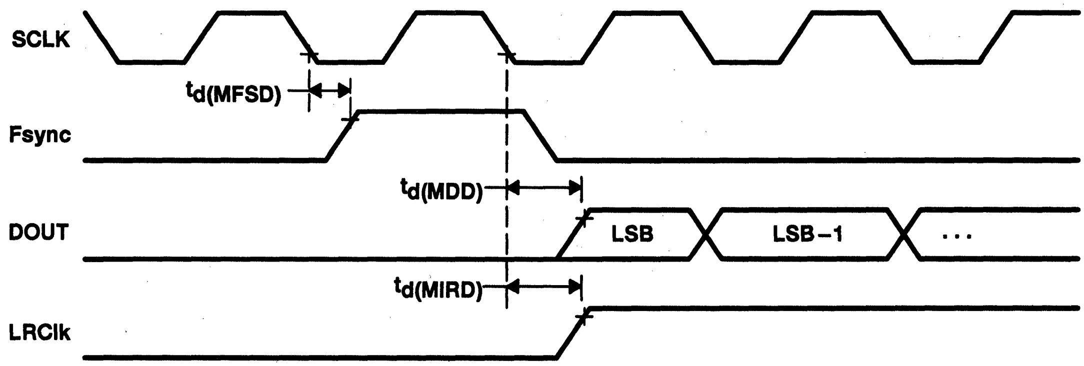


Figure 4–4. SCLK to Fsync, DOUT, and LRClk – Master Mode 7

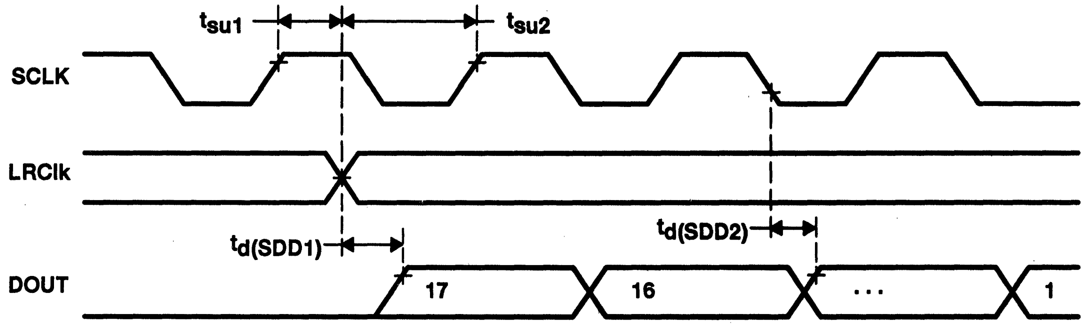


Figure 4–5. SCLK to LRClk and DOUT – Slave Mode 0, Fsync High

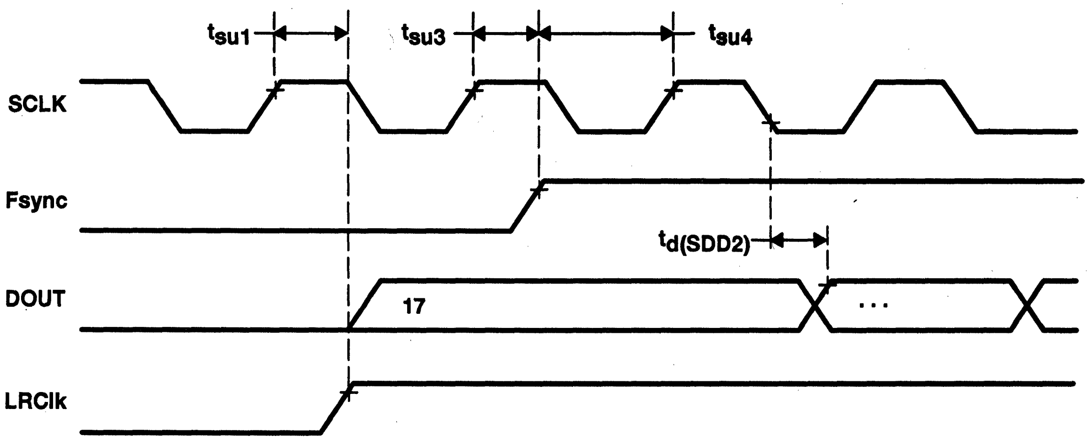


Figure 4–6. SCLK to Fsync, LRClk, and DOUT – Slave Mode 2, Fsync Controlled

5 Application Information

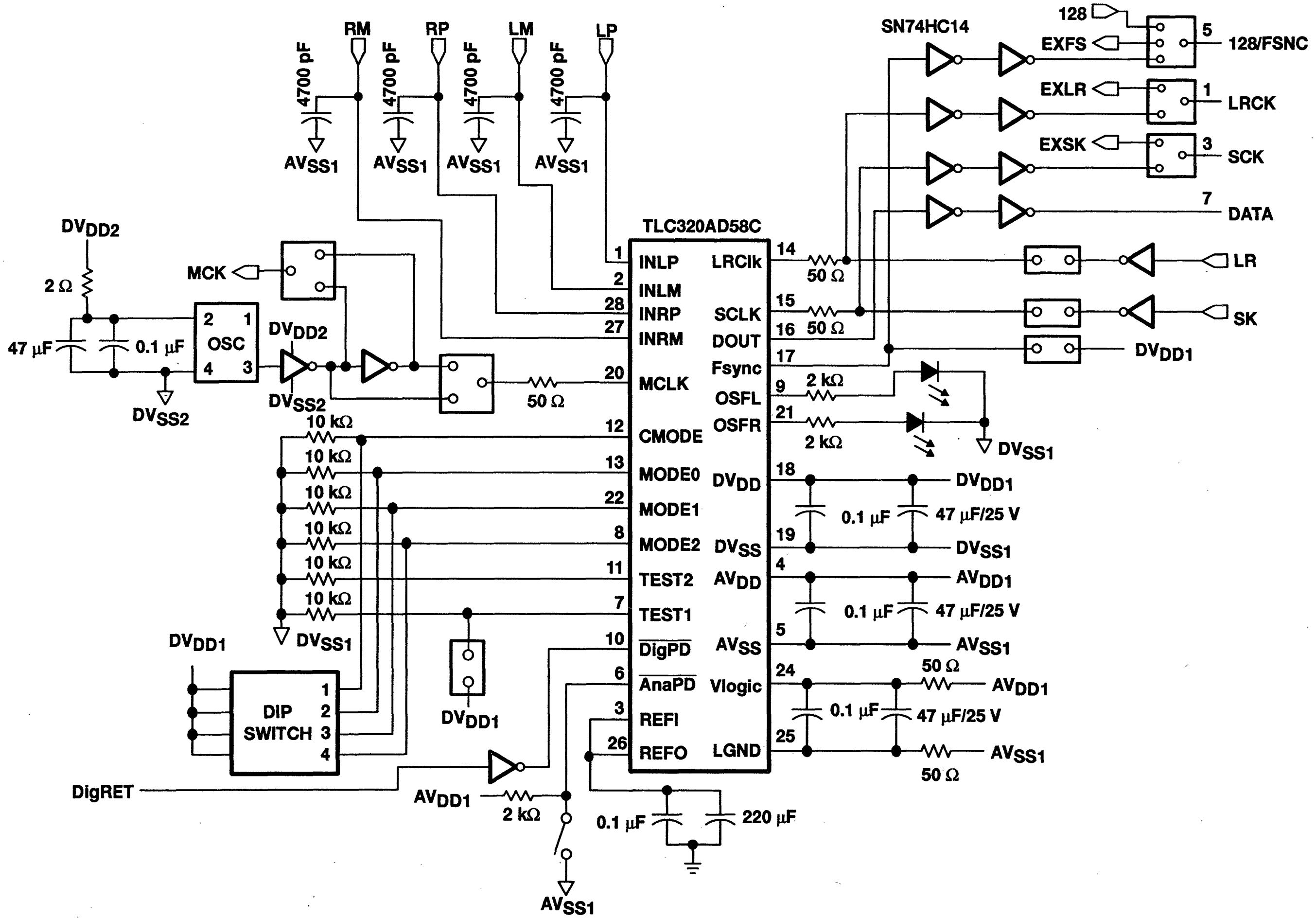


Figure 5–1. TLC320AD58C Configuration Schematic

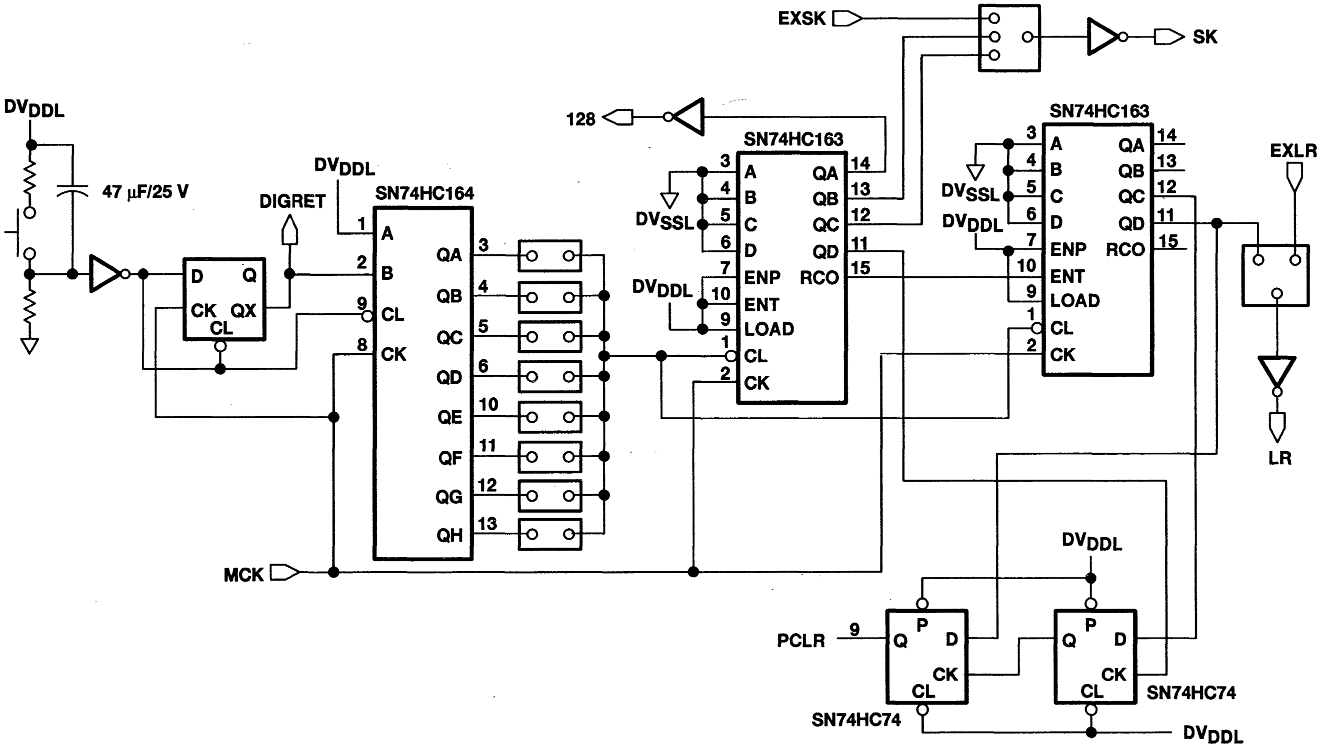


Figure 5–2. TLC320AD58C External Digital Timing and Control-Signal Generation Schematic

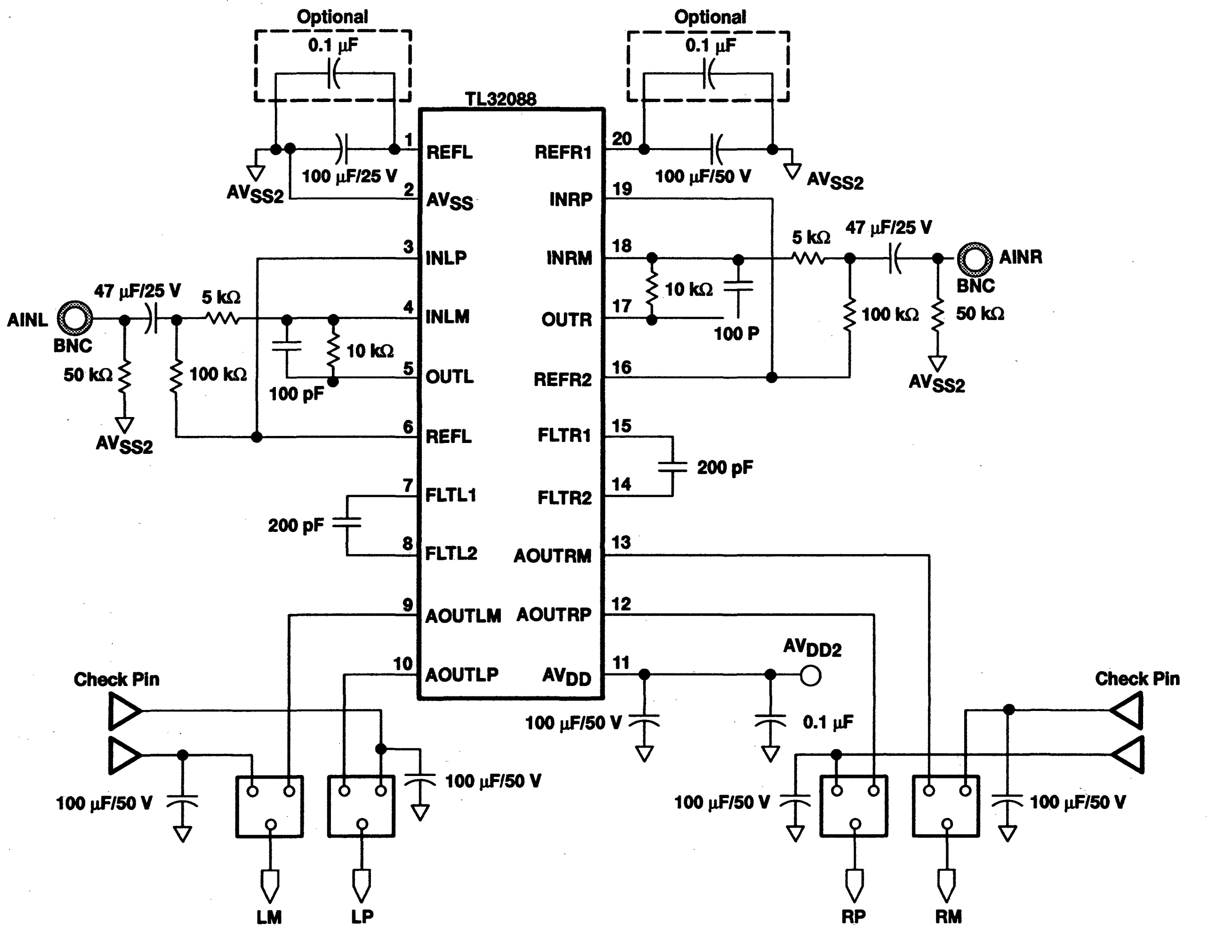


Figure 5–3. TLC320AD58C External Analog Input Buffer Schematic

TL7726
Hex Clamping Circuit

TEXAS INSTRUMENTS

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Contents

List of Illustrations

Introduction

This application report describes both the parasitic effects present in integrated circuits (ICs) and the problems that can result when protecting precision analog components with conventional methods. Specifically illustrated are how these problems can be overcome by using the TL7726 hex clamping circuit.

All semiconductor ICs, regardless of function and manufacturer, are vulnerable to voltages and currents exceeding the absolute maximum ratings. Although semiconductor manufacturers often build in protection features such as electrostatic-discharge (ESD) protection, voltage clamping, and current limitation, the devices may fail if operated outside the manufacturer's absolute maximum ratings.

Main failure mechanisms result from overvoltage stress of the semiconductor material. CMOS devices are particularly vulnerable in this regard, even at low-voltage levels, due to inherent parasitic structures. The best understood parasitic effect is latch-up, which is caused by parasitic thyristor action caused by overvoltage stress. If sufficient current is injected into either the input or output pins of the device, the thyristor triggers and a short circuit results between the supply rails (latch-up). This usually results in catastrophic device failure.

Through careful semiconductor design and by using the device within the manufacturers' absolute maximum voltage ratings, the effects of overvoltage stress can be greatly reduced. For precision analog circuits, this externally applied voltage level should be tightly controlled; the voltage should be no more than 0.3 V above the positive supply or 0.3 V below ground. Since it is difficult to predict if an applied voltage falls within these limits, external clamping circuits in the form of silicon diodes are often employed.

Zener diodes seem to be an obvious choice for this function. Unfortunately, due to poor voltage tolerance and asymmetrical clamping, the protected circuitry may not only be inadequately clamped but may suffer from reduced performance. For example, the dynamic range of an analog-to-digital converter may be reduced.

The preferred use of Schottky diodes proves similarly inadequate. The forward voltage of a Schottky diode is 400 mV. While this can protect the device for the majority of fault conditions, it still allows voltage levels in excess of the manufacturers' absolute maximum levels to be developed across the device. In effect, the device is being operated outside the recommended conditions and its continued function may be impaired.

Parasitic Transistors in Complementary MOS Circuits

The normal operating effects of the parasitic transistors inherent when making complementary MOS (CMOS) components is not particularly critical; however, the resultant structures shown in Figure 1 allow a clear explanation of parasitic effects when operation is not restricted to normal ranges.

The manufacturing process of high-speed digital CMOS circuits begins with an N-doped substrate (see Figure 1) into which a P-doped well is diffused followed by N-doped regions for the drains and sources of the N-channel transistors; the well itself is connected via a P-doped contact to the substrate (GND). P-doped zones in the N-doped substrate provide the drains and sources of the P-channel transistors.

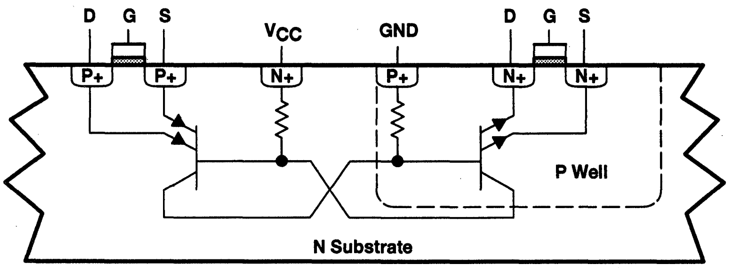

Figure 1. Parasitic Bipolar Transistors in CMOS Circuits

Latch-Up

The substrate itself is connected to the positive supply voltage (V_{CC}) via an N-doped contact. This produces both parasitic npn and pnp transistors; together these make up a pnpn structure of a thyristor (see Figure 2). The anode of this parasitic thyristor is connected to the positive supply and the cathode to GND; all other connections to this element (inputs and outputs) are gates of the thyristor. If a large enough current is injected into the input or output of this element, the thyristor is triggered. This effect is known as latch-up, and the resulting short circuit between the supply rails usually causes destruction of the component.

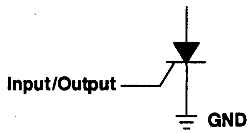

Figure 2. Structure of Parasitic Thyristor

Guard Rings

Latch-up effects have been reduced by incorporating additional guard rings in the structure. Guard rings are circular N- or P-doped zones surrounding the endangered elements, the N zones being connected to the positive supply rail and the P zones to the most negative supply rail (usually the substrate supply rails). These guard rings (see Figure 3) provide additional collectors for the parasitic transistors, which collect most of the current circulating in the substrate and divert it to the supply voltage rails; to a large extent, these eliminate the danger of latch-up. With modern logic circuits, such as high-speed CMOS, guard rings prevent latch-up from occurring until at least 300 mA is injected into an input or output at an operating temperature of 125°C. Since the gain of the parasitic transistors decreases at lower temperatures, the sensitivity of the thyristors at lower temperatures is reduced. At normal temperatures with careful device design, currents of over 1 A are necessary to provoke latch-up.

Linear CMOS (analog process) ICs are tested for susceptibility to latch-up by injecting a current pulse with an amplitude of 100 mA at an ambient temperature of 25°C into the inputs and outputs. This current is chosen to simulate a practical overload condition, while eliminating any risk of damage. The protective elements of ICs are in fact designed to withstand, without risk of damage, a continuous current of 5 mA in the clamping diodes.

The danger of component destruction as a result of latch-up due to parasitic transistors can therefore be reduced with careful chip design but does not entirely eliminate them; this is particularly evident with high-impedance (high-sensitivity) circuits.

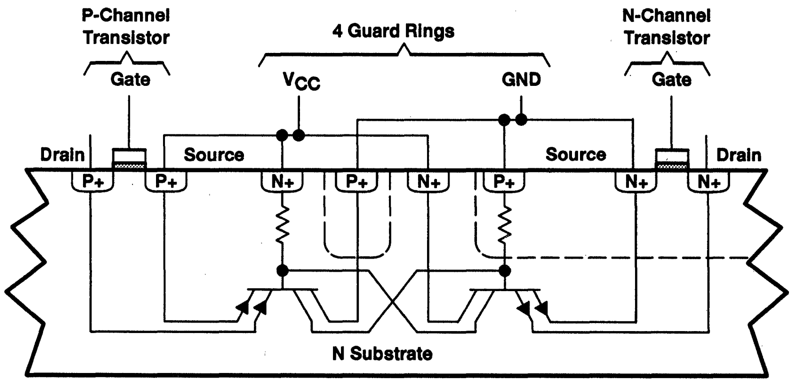

Figure 3. Guard Rings in CMOS Circuits

CMOS Internal-Input-Protection Circuitry

Use CMOS-input diode-protection circuitry, as shown in Figure 4, and assume the input is derived from the voltage source V1 = 24 V. The supply voltage (V_{CC}) is 5 V. A series resistor (R1 = 100 kΩ) ensures that the current in the internal clamping diode (D1) is limited to an acceptable value. A potential problem can occur if a neighboring input is connected similarly and is then controlled by the voltage source V2 = 0 V. In this case, a pnp transistor is created between the two clamping diodes D1 and D2. As a result, part of the current flowing through D1 (emitter) is diverted to D2 (collector); the N-doped substrate, which is connected to the supply voltage, then functions as the base of a parasitic transistor. Even when the gain of this transistor is comparatively low (0.01 – 0.1), the current through the R2 resistor creates a voltage drop that distorts the signal at the input and causes malfunction.

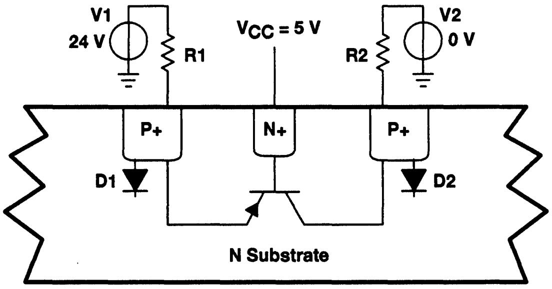

Figure 4. Parasitic Transistors in Input-Protection Circuits

This effect can be reduced through the use of additional guard rings (see Figure 3) but not entirely eliminated. Absolute maximum input voltages are given in data sheets, and if these limits are observed, parasitic effects will be insignificant. With digital CMOS circuits, it is permissible for the input voltage to be up to 0.5 V more positive than V_{CC} or 0.5 V more negative than the substrate without danger of malfunction. With analog circuits that operate at currents several orders of magnitude lower, voltage must be more tightly controlled; the input voltage should not be allowed to be more than 0.3 V above or below the supply voltage.

Silicon integrated protection or clamping diodes have a typical forward voltage (V_f) of 0.7 V at room temperature. The input voltage delta is 0.3 V, since the negative temperature coefficient of the forward voltage (≈ –2 mV/°C) must be taken into account. As mentioned before, sensitive circuits can malfunction with currents of only a few microamps, at which the forward voltage of a silicon diode at room temperature may be significantly below 0.7 V.

If under any conditions input voltages could exceed these maximum values, then additional precautions are necessary; these usually take the form of external clamping diodes on the input (see Figure 5).

External Clamping Diodes

Silicon diodes are of only limited use for protection since their forward voltage is close to that of the clamping diodes that are already integrated into an IC; therefore, only a part of the excess current is diverted into the external diodes. This approach is suitable when the circuit needs to be protected only from destruction. Because of their smaller geometry, the integrated clamping diodes have a higher forward resistance so a majority of the current is diverted to the external diodes. As protection against malfunction, conventional silicon diodes are not totally effective.

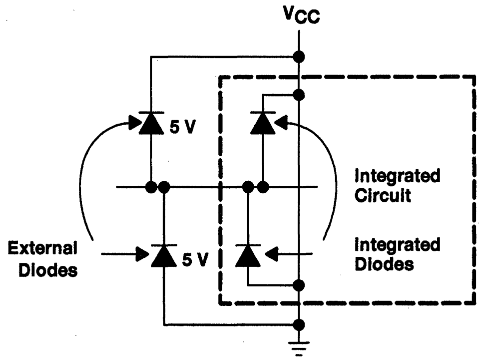

Figure 5. Protection Circuit With External Clamping Diodes

Better results can be expected with the use of germanium or Schottky diodes. These have significantly lower forward voltages (germanium: $V_f = 0.3$ V, Schottky: $V_f = 0.4$ V). Germanium diodes are seldom used at the present time, have high-leakage characteristics, and can be hard to obtain. If either diode has excessively high forward resistance, they are ineffective anyway.

TL7726 Hex Clamping Circuit

In order to prevent the activation of parasitic transistors, clamping diodes with exceptionally low forward voltages are necessary, and these can only be realized with an active circuit, as shown in Figure 6.

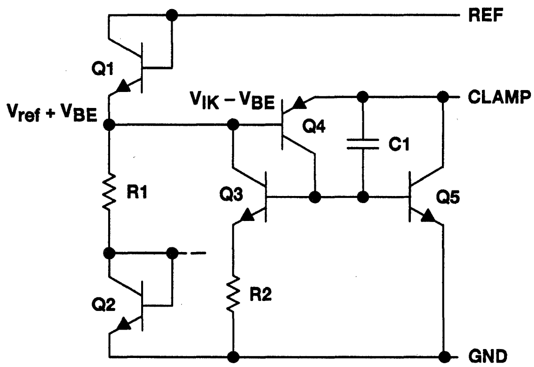

Figure 6. Simplified Circuit of the TL7726

Due to the effects described previously, neither diodes or conventional components are a panacea for protection, particularly for the demanding requirements of analog applications. For this reason, Texas Instruments has developed a dedicated IC that fully meets such requirements, the TL7726 hex clamping circuit. Figure 7 compares the current and voltage characteristics for a range of silicon diodes and a typical TL7726.

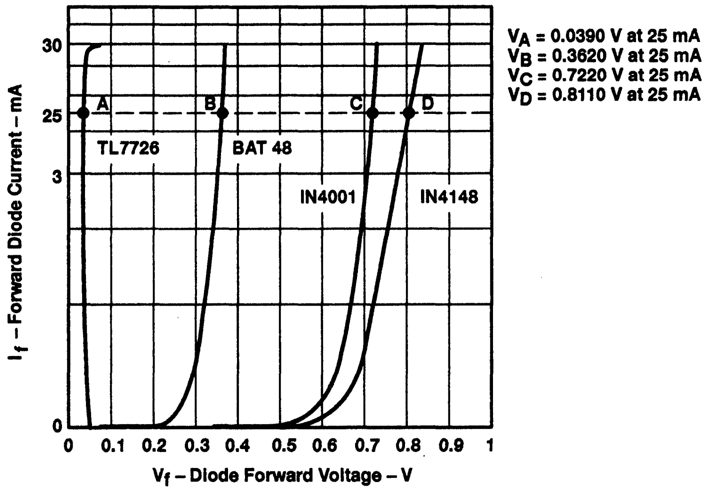

Figure 7. Current and Voltage Characteristics for Various Devices

Device Description

The TL7726 is comprised of six identical active voltage clamping circuits that have been specifically designed to protect vulnerable analog inputs from overvoltage stress. Under fault conditions, the TL7726 provides a forward-voltage drop of only 200 mV at 20 mA. Furthermore, the device provides symmetrical protection to both positive- and negative-going transient voltages (effectively replacing up to twelve diodes).

Under normal operation, the TL7726 offers a very high input impedance to ground and draws less than 10 µA; however, under fault conditions, a low-impedance path is offered to clamp the protected node at a voltage between V_{ref} to V_{ref} + 200 mV and between GND to GND −200 mV. This clamping operation is specified over the full operating temperature range.

The TL7726 is available in an 8-pin DIP (P package) or an 8-pin SOIC (D package). The TL7726C is characterized for operation from 0°C to 70°C. The TL7726I is characterized for operation from −40°C to 85°C. The TL7726Q is characterized for operation from −40°C to 125°C.

Circuit Operation

As shown in Figure 6, an internal reference voltage is generated across transistor Q1. This reference connected as a diode is a diode forward-voltage drop more negative than the external connection REF. The current through Q1, which is determined by the resistor R1, is only a few microamps; therefore, the supply rail of the circuit to be protected (usually connected to REF) is only very slightly loaded, allowing the TL7726 to be used with battery-powered equipment. The transistor Q2 generates a reference voltage with a circuit complementary to Q1 that limits voltages more negative than GND.

The voltage to be limited is connected to CLAMP. If the voltage at this input becomes more positive than the internal reference voltage at the emitter of Q1 plus the forward voltage of the base-emitter diode of Q4, a collector current flows in Q4. This current comes in part from the base of Q3, whose collector current further increases the base current of Q4. This feedback ensures that the base current of Q5 and the collector current increase simultaneously. This circuit approach ensures that a current of only a few microamps flows in REF as long as the clamp voltage, V_{IK}, is the same as or smaller than the reference voltage, V_{ref}. A small increase of the voltage at CLAMP causes the current to increase very rapidly (see Figures 8 and 9). The circuit behaves like an external low-resistance Zener diode whose breakdown voltage can be set by a reference voltage at REF.

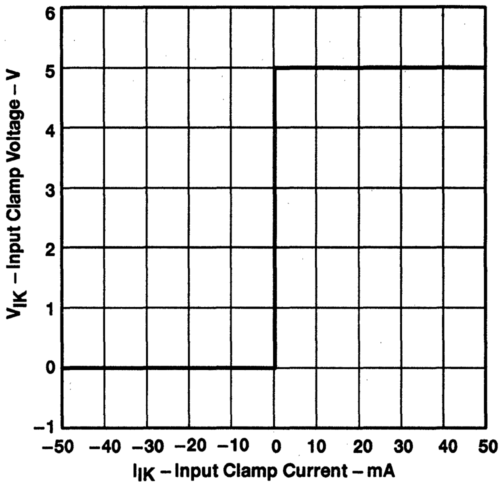

Figure 8. Characteristics of the TL7726 (V_{ref} = 5 V)

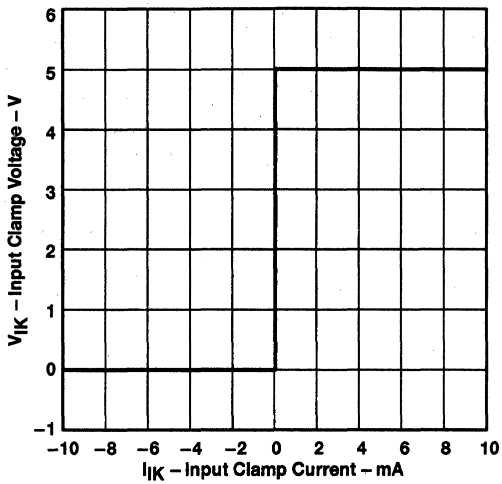

Figure 9. Characteristics of the TL7726 at Low Current (V_{ref} = 5 V)

A complementary circuit has the effect that if the input sees a voltage that is more negative than GND, the resulting current (flowing outward) also increases very rapidly. In this voltage range, the circuit behaves like a very low resistance diode having a forward voltage of only some tenths of a millivolt.

The characteristics of the TL7726 cannot be properly represented using linear axes. Therefore, mixed log/linear axes are used (see Figure 10) so the voltage limits over a very wide range can be shown in detail.

Overvoltages at device pins are often of very short duration but of high amplitude. The hex clamping circuit must be able to provide reliable protection under these conditions, so the device has been designed such that a continuous current of 50 mA is permissible at the clamp input. However, the maximum power dissipation of the package must be taken into account in case such currents flow simultaneously into several inputs.

Extremely rapid operation of the hex clamping circuit has been achieved with the capacitor C1 (see Figure 6), which essentially consists of the collector-base (Miller) capacitance of Q5. This ensures that Q5 is immediately switched on if there are rapid voltage changes. Figure 11 shows that voltage limiting is achieved with virtually no delay. Figure 12 shows the circuit used to make these measurements. Since this circuit reacts to practically any voltage change, it must be noted that several microseconds elapse from a change of amplitude until a new stable value is reached (see Figure 13).

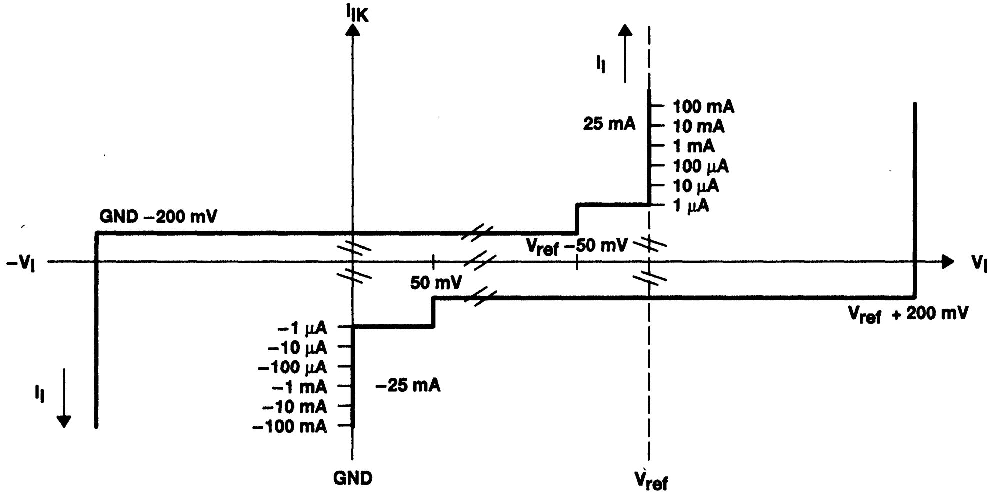

Figure 10. Current and Voltage Limits of TL7726

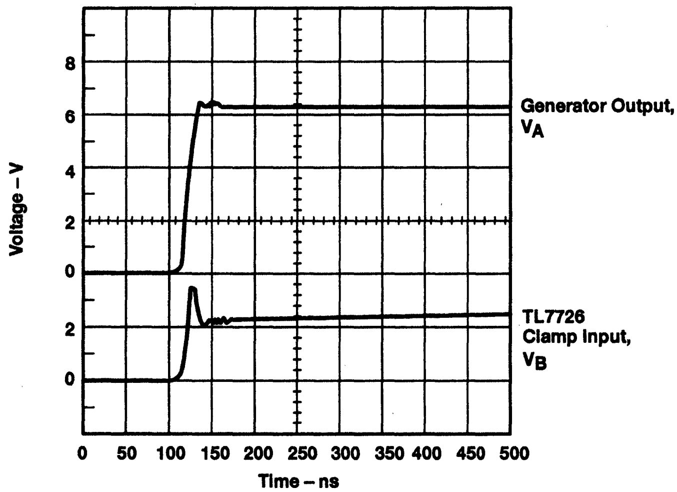

Figure 11. Behavior of TL7726 With Rapid Voltage Changes

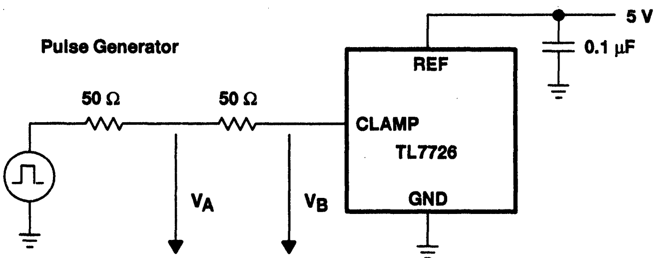

Figure 12. Measurement Circuit

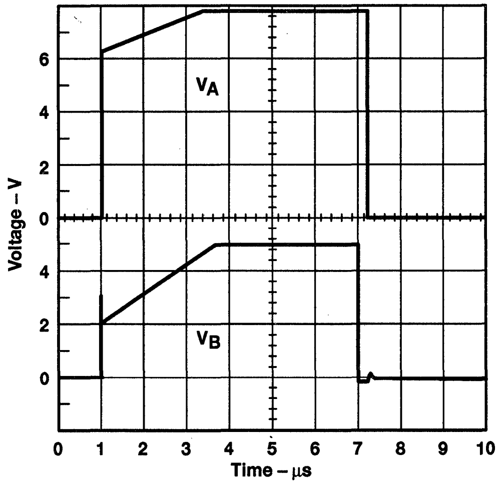

Figure 13. Settling Time at the Input of the Hex Clamping Circuit

Application Examples Using the TL7726

The TL7726 was developed to protect the inputs of linear (analog) ICs against overvoltage and to ensure the reliable operation of these components both in demanding applications and in harsh environments. A typical application of the TL7726 is extremely simple, as shown in Figure 14.

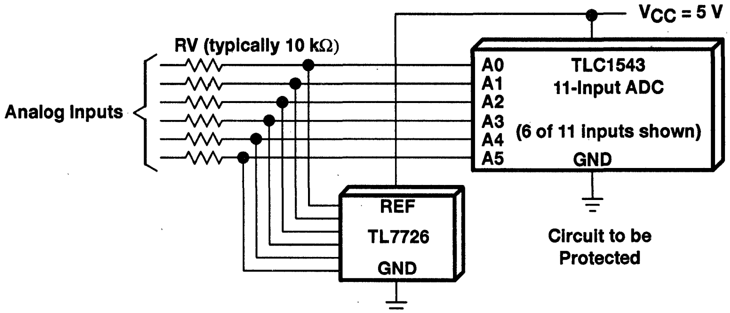

Figure 14. Typical Application of the Hex Clamping-Circuit TL7726

The TL7726 is ideal for protecting the inputs of the TI range of multiple input analog-to-digital converters. The TL7726 can reliably handle currents up to 50 mA. The series current-limit resistor (RV) is chosen to limit the current to this level. The clamp voltage level is set to be within 200 mV of V_{ref} and GND.

The reference voltage pin (REF) of the hex clamping circuit is connected to the supply voltage (V_{CC}) of the circuit to be protected whose inputs are connected to the CLAMP inputs (see Figure 14). The requirement for series resistors depends on the particular application. If the input signal to be limited is supplied by a comparatively high-impedance source, and if only undefined currents must be prevented from flowing into the substrate of the circuit to be protected, such resistors are not needed. However, in most cases, voltages of considerable amplitude can be expected. These are coupled into the signal inputs and cause significant interference. In such cases, the TL7726 should also be protected against damage; this can only be ensured if the current that flows can be limited to an acceptable amount with a series resistor. The TL7726 reliably diverts currents up to ±50 mA where the difference of the voltage between the input voltage (V_{IK}) and the reference voltage (depending on whether current is flowing to REF or GND) is only a few hundred millivolts. The RV series resistor can be chosen over a wide range depending on the requirements of the circuit to be protected. Resistors from a few tens of ohms up to several tens of kilohms (i.e., 20 Ω to 40 kΩ) can be used.

When choosing series resistors used to limit current flowing into the TL7726, consideration should be given to the maximum power dissipation [$P_{D(max)}$] that the TL7726 can withstand. The limiting factors are the maximum permissible device temperature of 150°C and the thermal resistance ($R_{\theta JA}$) between the device and ambient temperature. The following expression applies (see the TL7726 data sheet):

$$P_{D(max)} = \frac{150°C - T_A}{R_{\theta JA}}$$

where:

T_A = ambient temperature
$R_{\theta JA}$ (D package) = 172°C/W
$R_{\theta JA}$ (P package) = 105°C/W

given the following derating factors

Derating factor (D package) = $1/R_{\theta JA}$ = 5.8 mW/°C
Derating factor (P package) = $1/R_{\theta JA}$ = 9.5 mW/°C

Current Flow

Consideration should be given to the path taken by the current that flows into the TL7726. A positive current flowing into a CLAMP terminal is channeled to GND (see Figure 6 and Figure 15); similarly, a negative current flows to REF. Since REF is normally connected to the V_{CC} rail supplying other circuits, this voltage source must be able to withstand the current flow. In most cases, only short duration voltages need to be limited; this usually means that the filter capacitor in the power supply must be of sufficiently large capacitance and the ground return of sufficiently large size to prevent excessive ground bounce.

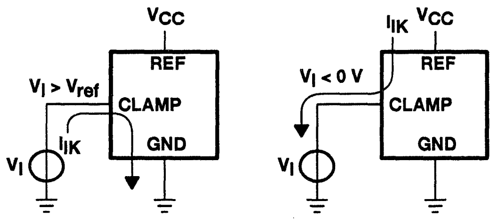

Figure 15. Current Flow Paths

Summary

Until recently, the protection of analog circuits in harsh environments where the inputs could be subjected to undefined overvoltages was only possible with considerable extra circuitry. Although this circuitry gave protection against destruction, it often limited the performance of the protected device. The availability of the TL7726 hex clamping circuit now provides both reliable and transparent protection operation for up to six analog inputs in a single package.

Microcontroller Based Data Acquisition Using the TLC2543 12-Bit Serial-Out ADC

TEXAS INSTRUMENTS

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Contents

List of Illustrations

Introduction

Scope of this Application Report

This application report describes how to construct 12-bit data acquisition systems using the TLC2543 serial-out analog-to-digital converter (ADC) in conjunction with a range of four popular microcontrollers.

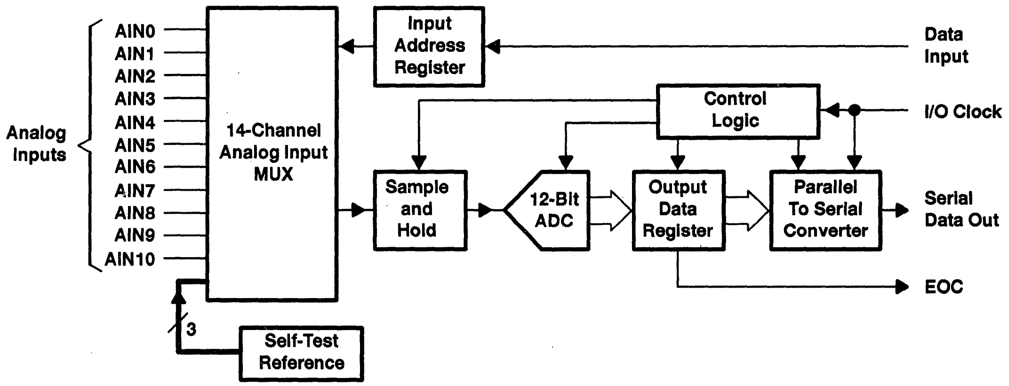
The four microcontrollers used are the TMS370, H8/300, 68HC11 and 80C51.

The TLC2543

The TLC2543 is a 12-bit ADC which uses the switched capacitor successive approximation technique to perform the conversion process and provides a maximum sampling rate of 66k samples per second (KSPS) while using only 1 mA (typical) of supply current.

The block diagram of the TLC2543 is shown in Figure 1. Any one of eleven analog input channels can be selected by programming the four most significant bits (MSBs) of the eight bit channel/mode control byte applied serially to the DATA INPUT terminal of the device. In addition three internal test voltages [V_{ref-}, V_{ref+} and $(V_{ref+} - V_{ref-})/2$] can be applied to the converter for calibration or other purposes by applying the appropriate code to the same four MSBs.

The four least significant bits (LSBs) of the channel/mode control byte are used to select the output data length (8, 12 or 16 bits), the output data order (MSB first or LSB first) and whether unipolar (binary) or bipolar (2's complement around $(V_{ref+} - V_{ref-})/2$) format is required.



- 12-Bit Resolution ADC
- 66-KSPS Sampling Rate
- 11 Analog Input Channels
- Low Supply Current – 1 mA (Typ)
- Power-Down Mode – 4 μA (Typ)
- SPI Compatible Serial Interface

Figure 1. TLC2543 Block Diagram

Interface Timing

Four transfer methods are available for obtaining the full 12 bits of resolution from the TLC2543. Either 12 or 16 clock cycles can be used for each conversion and data transfer.

A chip select ($\overline{CS}$) pulse can be inserted at the start of each conversion or only once at the beginning of each sequence of conversions with $\overline{CS}$ remaining low until the sequence is completed.

Figure 2 shows the timing for the method which uses 16 clock cycles for each conversion and data transfer cycle and which inserts $\overline{CS}$ between each of these transfer cycles. Figure 3 shows the timing for the method which uses 16 clock cycles for each conversion and data transfer cycle but inserts $\overline{CS}$ only once at the start of each sequence of conversions.

This application report describes various microcontroller interfaces, each of which uses 16 clock cycles for each conversion data transfer. $\overline{CS}$ is applied at the start of each conversion and data transfer. This method allows for the general case where one or more conversions may be required. It also simplifies the required software.

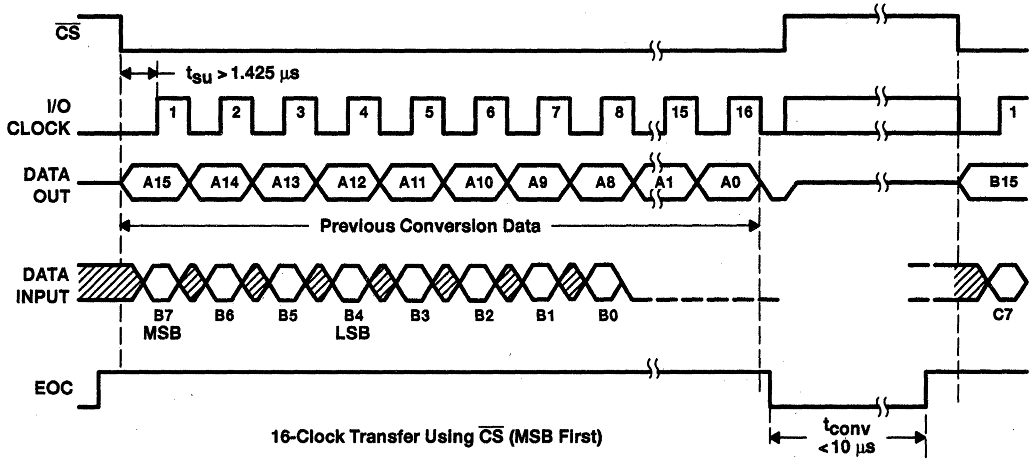


Figure 2. Timing for 16-Clock Transfer Using $\overline{CS}$ With MSB First

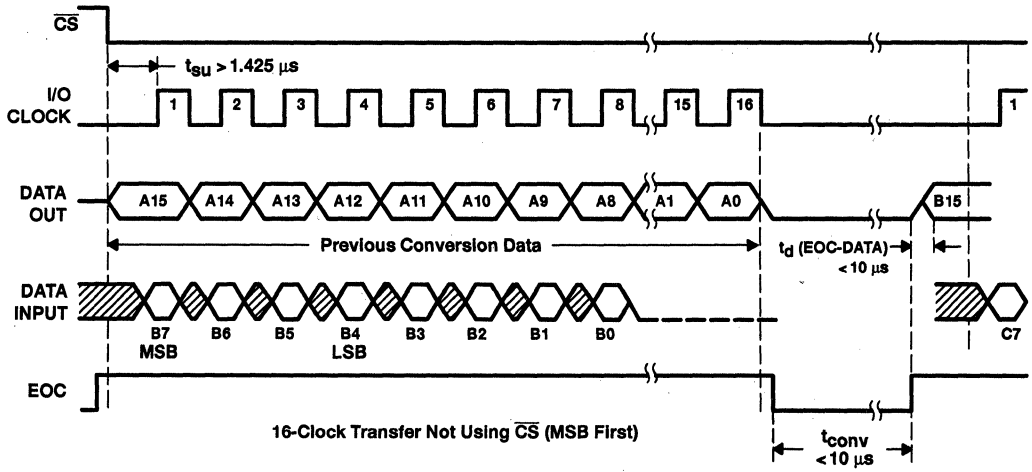


Figure 3. Timing for 16-Clock Transfer Not Using $\overline{CS}$ With MSB First

Minimum Number of Data Transfers per Channel

It should be noted that in any single data transfer cycle between the TLC2543 and the chosen microcontroller the data output from the ADC is the result of the previous conversion. The software listings included in this application report have been written for the general case where the conversion results may be required for any individual channel or sequence of channels. In this case the program included for each microcontroller interface must be run at least twice per channel so that valid data corresponding to the required analogue input channel and ADC mode is delivered.

Software can be written to implement the consecutive channel scanning mode of operation of the TLC2543. In this case the result from the first analog-to-digital conversion should be ignored or overwritten.

Serial Peripheral Interface (SPI)

The fastest and most efficient method of implementing a data transfer between the TLC2543 and a microcontroller is to use the serial peripheral interface (SPI) of the microcontroller, if this is available.

The TMS370 (Texas Instruments), H8/300 (Hitachi) and MC68HC11 (Motorola) all offer SPIs (or the equivalent) in a subset of each of these families of microcontrollers. The H8/300 offers a serial communications interface (SCI) which can be configured to operate in a similar way to that of the standard SPI's offered by the TMS370 and MC68HC11.

The principle features of the SPI are:

- Simultaneous serial data input and output
- Synchronous operation
- Provision of frequency programmable serial clock
- Data transfer complete flag

Figure 4 shows the structure of the SPI. In this case the TMS370C010 is used to illustrate the main elements of the interface.

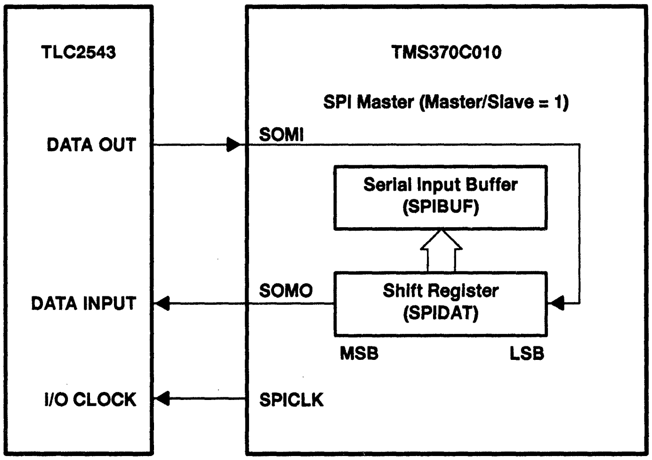


Figure 4. Serial Peripheral Interface – Internal Structure and Data Flow

The microcontroller can be configured by software to perform as the SPI master or slave. When operating as the master, data is input to the SPI shift register (SPIDAT) via the slave out master in (SOMI) terminal. At the same time data is output from the SPIDAT via the slave in master out (SIMO) terminal.

The SPI functions as follows. The SPIDAT should be loaded with the first byte of data to be sent. This automatically initiates the transmission of this byte. During this transmission time data is received at the other end of the SPIDAT shift register. The SPI INT FLAG is regularly checked. As soon as the last bit of the input data byte is received the SPI INT FLAG is set to 1. This then signals that the received byte can be read from the serial input buffer (SPIBUF) and that the SPIDAT is ready to accept the next byte of data to be transmitted.

Additional SPI features which apply to the specific microcontrollers are described in their respective sections which follow.

TLC2543 to SPI Interface Timing

The timing digram for the 16 clock transfer TLC2543 to SPI interface is shown in Figure 5. The channel select/mode data is read into the TLC2543 on the positive going edges of the I/O clock and analog-to-digital conversion results are read into the microcontroller on the negative going edges of the I/O clock.

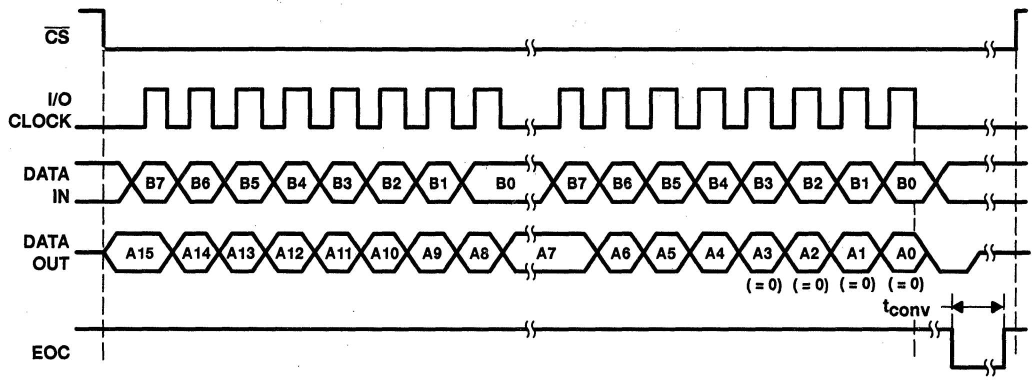


Figure 5. TLC2543 to SPI Interface Timing

Software Flowcharts

Figures 6, 7, and 8 show the flow charts for the main program and subroutines used in the TLC2543 to TMS370C010 interface software shown in this application report. The same program structure also applies to the other three interfaces included in this report.

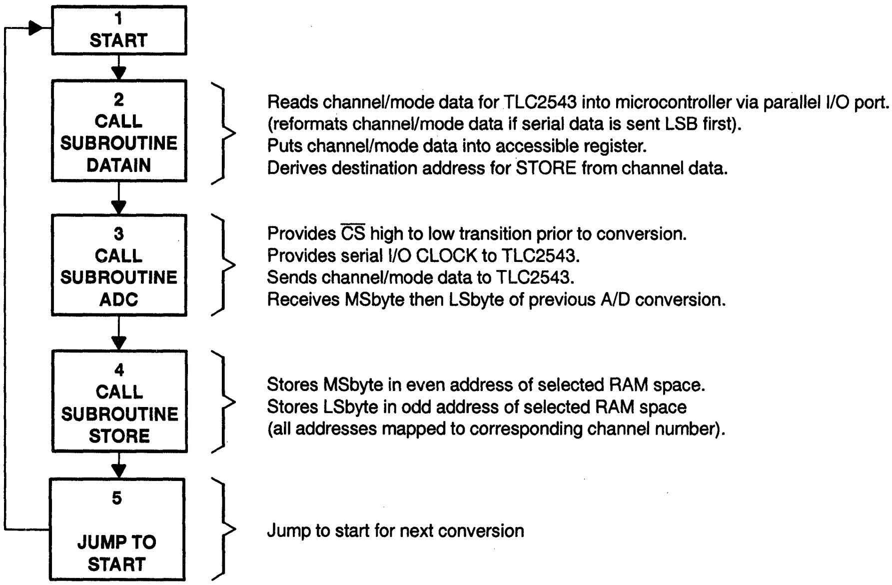


Figure 6. Flowchart for Main Program of TLC2543 to TMS370C010

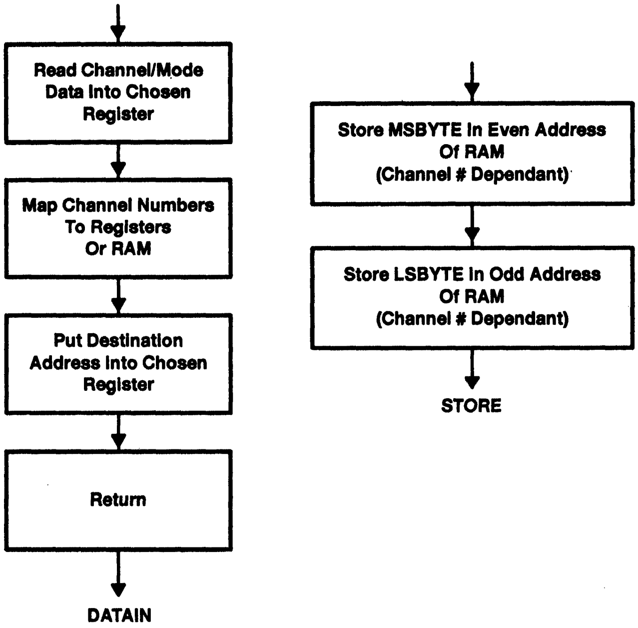


Figure 7. Flowcharts of Subroutine DATAIN and STORE for TLC2543 to TMS370C010 Interface Software

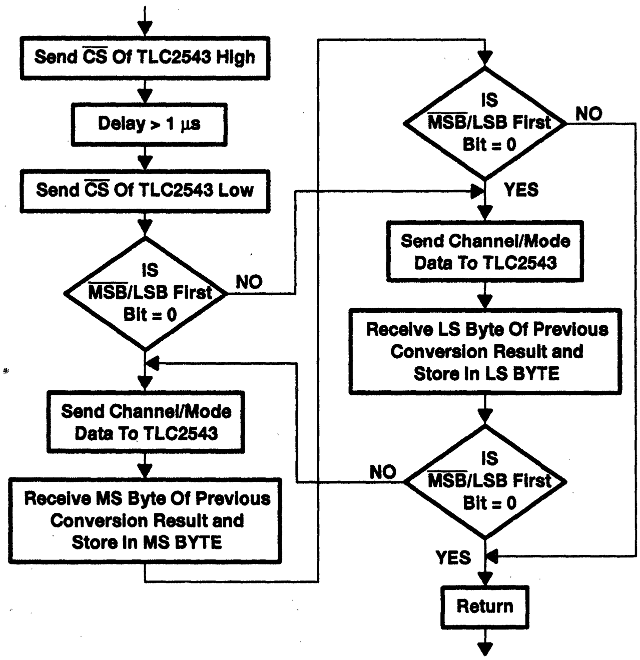


Figure 8. Flowcharts of Subroutine ADC for TLC2543 to TMS370C010 Interface Software

TLC2543 TO TMS370 Microcontroller Interface

Microcontroller Features

Within the family of TMS370 microcontrollers there are several versions which contain a serial peripheral interface (SPI) facility. One of these versions should be chosen to implement the interface method described below. One such version is the TMS370C010 which is used to illustrate the method.

Interface Circuit

Figure 9 shows the circuit interconnections for the TLC2543 to TMS370C010 microcontroller interface. Note that no extra logic is required to implement this interface.

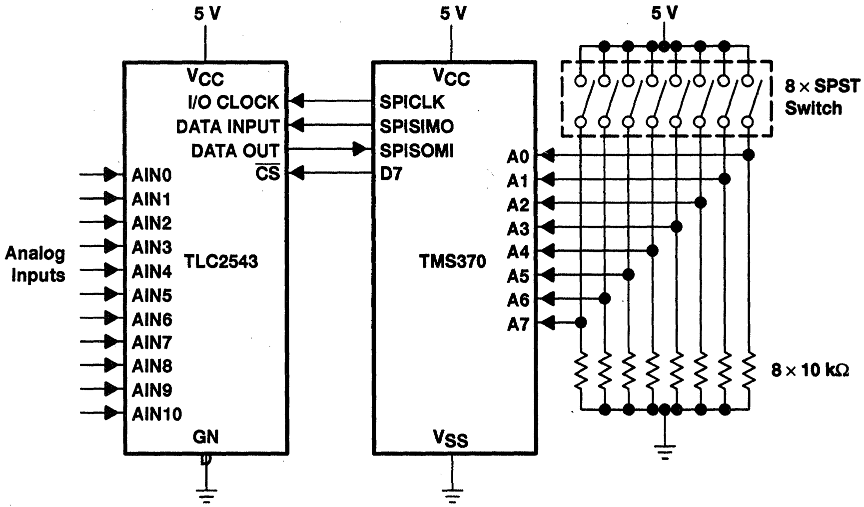


Figure 9. TLC2543 to TMS370C010 Interface Circuit

Depending upon the layout of the particular printed circuit board used it may be necessary to insert a small value capacitor of between 50 and 100 pF between the I/O CLOCK input of the TLC2543 and ground. This has the effect of ensuring that data applied to the DATA INPUT terminal of the TLC2543 is valid before the positive going transition of the I/O CLOCK.

The positive reference, REF+, to the TLC2543 is provided directly from the V_{CC+} supply.

The four digital interface terminals, I/O CLOCK, DATA INPUT, DATA OUT, and $\overline{CS}$, of the TLC2543 connect directly to the SPICLK, SPISIMO, SPISOMI and D7 terminals respectively of the TMS370C010.

The operation mode and channel number of the TLC2543 is determined by the serial data which is sent to its DATA INPUT terminal.

Software

List 1 contains the software listing for the program which controls the interface illustrated in Figure 5. The software consists of the main program and three subroutines called DATA IN, ADC and STORE. DATAIN reads in the channel select and mode control data into a holding register and maps the channel select number to a corresponding pair of registers between R64 and R91. The mapping vector is held in register R10. ADC provides the chip select pulse, controls the SPI operation, and puts the MSByte and LSByte of each conversion result into registers R20 and R21 respectively. STORE puts the MSByte into the even number register and the LSByte into the odd number register mapped by the contents of register R10.

The user can put channel select and ADC mode control data into the holding register within the microcontroller, via the 8-bit wide port A bidirectional I/O port, using a bank of eight toggle switches as shown in Figure 9. Alternatively, the mode and channel data can be sent to the microcontroller holding register via the asynchronous serial communications interface (SCI). This option is available only on those versions of the TMS370, such as the TMS370C020, which include both SPI and SCI interfaces. Additional software to control the SCI must be appended to the software shown in List 1 to provide this method of control.

List 1

```
LOC      OBJ          SOURCE
                      ;*  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *
                      ;*                                            *
                      ;* TLC2543 to TMS 370Cx10 Interface Program   *
                      ;*                                            *
                      ;* This program reads channel select and mode *
                      ;* control data (provided by toggle switches) *
                      ;* into the microcontroller, using subroutine *
                      ;* DATAIN.                                    *
                      ;* It then provides the control signals to    *
                      ;* the TLC2543 to perform a 12 bit analog to  *
                      ;* conversion, using subroutine ADC. It       *
                      ;* finally stores the MSByte and LSByte of    *
                      ;* each conversion in consecutive even and    *
                      ;* odd number registers respectively starting *
                      ;* at R64 corresponding to channel 0, using   *
                      ;* subroutine STORE.                          *
                      ;*  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *
         0030         SPICCR  .EQU P030       ;*  *  *  *  *  *  *  *
         0031         SPICTL  .EQU P031       ;*                    *
         0037         SPIBUF  .EQU P037       ;*                    *
         0039         SPIDAT  .EQU P039       ;*                    *
         003d         SPIPC1  .EQU P03D       ;*                    *
         003e         SPIPC2  .EQU P03E       ;* Name Peripheral    *
         003f         SPIPRI  .EQU P03F       ;* Registers          *
         0021         APORT2  .EQU P021       ;*                    *
         0022         ADATA   .EQU P022       ;*                    *
         0023         ADIR    .EQU P023       ;*                    *
         002c         DPORT1  .EQU P02C       ;*                    *
         002d         DPORT2  .EQU P02D       ;*                    *
         002e         DDATA   .EQU P02E       ;*                    *
         002f         DDIR    .EQU P02F       ;*  *  *  *  *  *  *  *
         7ffe         RESET   .EQU 7FFEH      ;Reset vector named
         2e           CSBIT   .DBIT 7,DDATA   ;TLC2543 Chip Select bit
                                              ;named CSBIT
                      ;
                      ;

4000                          .TEXT 4000H     ;Start program at 4000H
                      ;Main Program
4000     5260         START   MOV #60H,B      ;
4002     fd                   LDSP            ;Set SP to address 60H
4003 *   88400000             MOVW #4000H,A
4007     8b7ffe               MOV A,RESET     ;Set reset vector
400a     b5                   CLR A
400b     2121                 MOV A,APORT2
400d     2123                 MOV A,ADIR
400f     f7802f               MOV #080H,DDIR
4012     2280                 MOV #80H,A
4014     2130                 MOV A,SPICCR
4016     2207                 MOV #07,A       ;Configure SPI for 8-bit
4018     2130                 MOV A,SPICCR    ;character length.
401a     2203                 MOV #03,A       ;Configure SPICLK
401c     213d                 MOV A,SPIPC1    ;function and direction.
401e     2222                 MOV #22H,A      ;Configure SPISOMI and
4020     213e                 MOV A,SPIPC2    ;SPISIMO pin functions.
         31           SPIF    .DBIT 6,SPICTL  ;SPI INT FLAG named SPINTF
         0b           MSLSB   .DBIT 1,R11     ;Bit 1 of R11 named MSLSB
4022     '8e402d              CALL DATAIN
4025     '8e403e              CALL ADC
4028     '8e409d              CALL STORE
```

List 1 (Continued)

```
LOC   OBJ              SOURCE

402b  '00d3                    JMP START

                       ;
                       ;Subroutine :- DATAIN
                       ;
402d   9122            DATAIN  MOV ADATA,B      ;Read ADC mode/channel
402f   d10b                    MOV B,R11        ;Put ADC mode/channel
                                                ;in R11
4031   53f0                    AND #0F0H,B      ;Retain channel number
4033   cc                      RR B             ;* * * * * * * * *
4034   cc                      RR B             ;* Map channel numbers  *
4035   cc                      RR B             ;* to registers R64-R91 *
4036   cc                      RR B             ;* R10 contains storage *
4037   5c02                    MPY #002,B       ;* address              *
4039   5840                    ADD #40H,B       ;* Even numbers - MS Byte*
403b   d10a                    MOV B,R10        ;* Odd numbers - LS Byte *
                                                ;* * * * * * * * *
403d   f9                      RTS
                       ;
                       ;Subroutine :- ADC
                       ;
403e   2203            ADC     MOV #003H,A
4040   a4802e                  SBIT1 CSBIT      ;Set ADC Chip Select high.
4043   b2              LOOP1   DEC A            ;Chip Select stays high
4044  '06fd                    JNE LOOP1        ;while A is not 0.
4046   c5                      CLR B
4047   512e                    MOV B,DDATA      ;CS goes low
4049   2207                    MOV #7,A
404b   2131                    MOV A,SPICTL     ;Enable SPI transmission
404d  '76020b19                JBIT1 MSLSB,LS1ST
4051   120b                    MOV R11,A
4053   2139                    MOV A,SPIDAT
                       ;       MOV R11,SPIDAT   ;Send mode/channel data
                                                ;to TLC2543
4055  'a74031fc        FLAG1   JBIT0 SPIF,FLAG1;If SPIF=0, repeat check.
4059   a21437                  MOV SPIBUF,R20   ;Put received MS Byte
                                                ;in R20
405c   71390b                  MOV R11,SPIDAT   ;Send mode/channel data
                                                ;to TLC2543
405f  'a74031fc        FLAG2   JBIT0 SPIF,FLAG2;If SPIF=0, repeat check.
4063   a21537                  MOV SPIBUF,R21   ;Put received LS Byte
                                                ; in R21
4066  '77020b32                JBIT0 MSLSB,RETURN ;If MSLSB=0, go
                                                  ;to RETURN
406a   120b            LS1ST   MOV R11,A
406c   2139                    MOV A,SPIDAT
406e  'a74031fc        FLAG3   JBIT0 SPIF,FLAG3;If SPIF=0, repeat check.
4072   a21537                  MOV SPIBUF,R21   ;Put received LS Byte
                                                ;in R21
4075   120b                    MOV R11,A
4077   2139                    MOV A,SPIDAT
4079  'a74031fc        FLAG4   JBIT0 SPIF,FLAG4;If SPIF=0, repeat check.
407d   a21437                  MOV SPIBUF,R20   ;Put received MS Byte
                                                ;in R20
4080   2208                    MOV #08,A        ;* * * * * * * * *
4082   d516                    CLR R22          ;*                 *
4084   dd14            LOOP2   RRC R20          ;*  Reformat MS Byte  *
4086   df16                    RLC R22          ;*                 *
4088   b2                      DEC A            ;*  Put result in R20 *
4089  '06f9                    JNZ LOOP2        ;*                 *
408b   421614                  MOV R22, R20     ;* * * * * * * * *
408e   2208                    MOV #08,A        ;* * * * * * * * *
4090   d517                    CLR R23          ;*                 *
4092   dd15            LOOP3   RRC R21          ;*  Reformats LS Byte *
4094   df17                    RLC R23          ;*                 *
4096   b2                      DEC A            ;*  Put result in R21 *
4097  '06f9                    JNZ LOOP3        ;*                 *
4099   421715                  MOV R23,R21      ;* * * * * * * * *
```

List 1 (Continued)

```
LOC    OBJ     SOURCE
409c   f9      RETURN   RTS
               ;
               ;Subroutine :- STORE
               ;
409d   1214    STORE    MOV R20,A       ;Put MS Byte into even
409f   9b0a             MOV A,@R10      ;address contained in R10
40a1   d30a             INC R10         ;(R10)+1
40a3   1215             MOV R21,A       ;Put LS Byte into odd
40a5   9b0a             MOV A,@R10      ;address contained in R10
40a7   f9               RTS
                        .END
```

Opto-Isolated 12-Bit Data Acquisition System

The serial nature of the data flow between the TLC2543 analog-to-digital converter and the accompanying microcontroller makes this ADC an ideal choice for isolated 12-bit data acquisition. Figure 10 shows an opto-isolated system which uses four optocouplers to provide a 3-kV isolation barrier.

Note that the optocoupler which routes conversion result data from the TLC2543 to the microcontroller is a single device and does not share the same piece of silicon with any of the other optocouplers used. This ensures that the full 3 kV of isolation is maintained between the ADC and microcontroller.

The choice of VP0610 P-channel enhancement MOSFETs avoids the use of an extra inverter stage for each optocoupler driver. In addition, the relatively low input capacitance of the VP0610 (typically 15 pF) allows data rates up to 100 kHz to be achieved without the need for external buffers to be added at the outputs of the TLC2543 and TMS370.

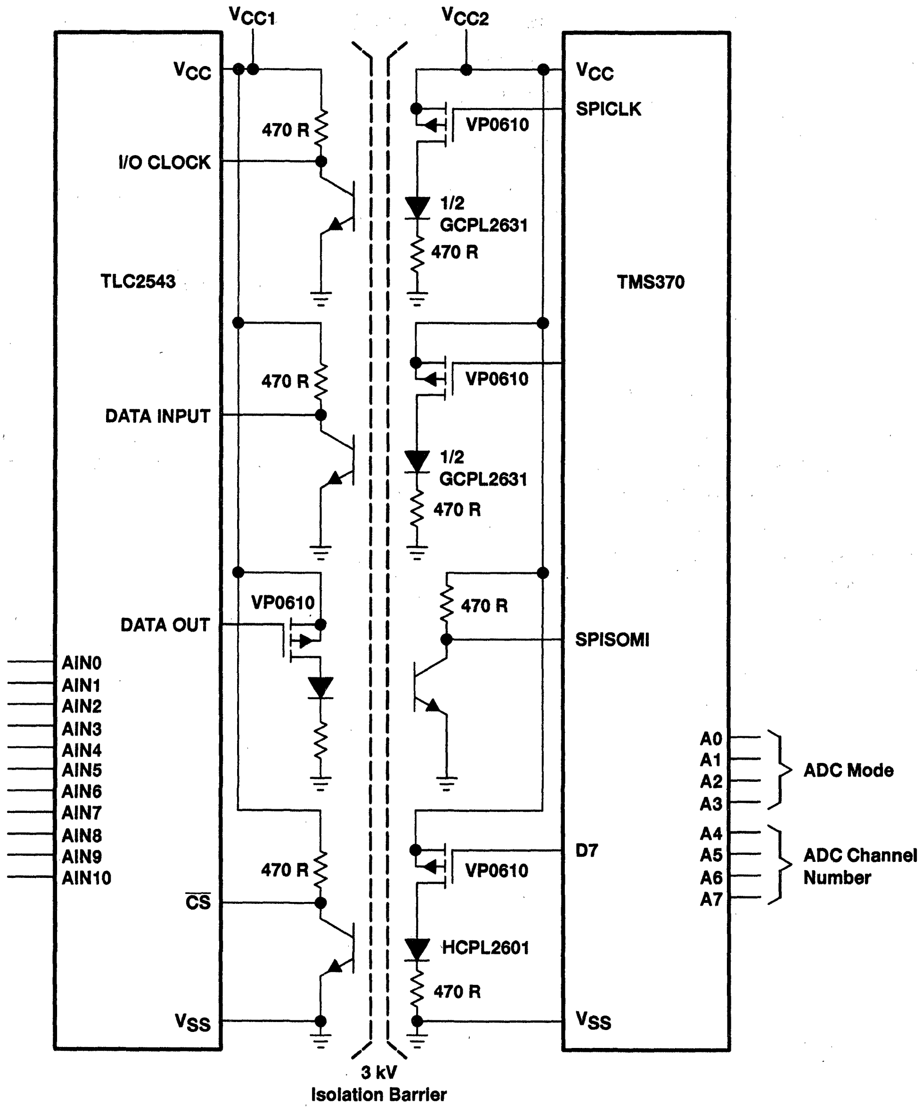


Figure 10. Opto-Isolated 12-Bit Data Acquisition System

TLC2543 to H8/325 Microcontroller Interface

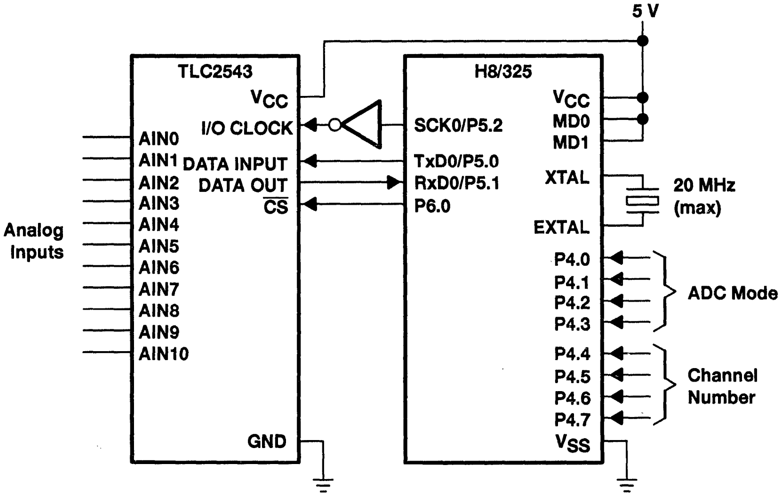
Microcontroller Features

The individual members of the H8 family of microcontrollers can be differentiated by various criteria, for example the inclusion or otherwise of an on-board 8-bit resolution analog-to-digital converter (ADC). Those members which include an ADC generally cost between 10 and 20 percent more than their counterparts which do not.

System requirements such as ADC resolution, remote location of ADC, flexibility, and total cost all influence the final choice of microcontroller architecture. The H8/325, used for this application report, does not include an on-board ADC but provides 1K of RAM, 32K of ROM, and two serial I/O ports. It is therefore well suited to interfacing with the TLC2543 serial output ADC.

Interface Circuit

Figure 11 illustrates a typical 12-bit data acquisition system which uses the H8/325 microcontroller to coordinate the operation of the TLC2543 ADC via one of its serial (SCI) ports. The circuit uses the H8's 8-bit parallel I/O port 4 to route ADC channel and mode information into the microcontroller. This information could be provided by a host system data bus or, as in Figure 6, by a bank of eight manually operated toggle switches situated on the same printed circuit board as the microcontroller.



NOTE: Single Chip Mode (MD0 = MD1 = 1)

Figure 11. TLC2543 to H8/300 Microcontroller Interface Circuit

Software

List 2 shows the program which was written to coordinate the interface. It uses three subroutines to implement the overall interface to the TLC2543. The first of these is called DATAIN which reads ADC channel and mode information into the microcontroller. It also maps converter channel numbers to corresponding addresses in RAM where conversion results can be stored. In this case the addresses from 0040H to 0067H were chosen to store the results. The most significant byte of each result is placed in an even address and the least significant byte of each result is placed in the corresponding adjacent odd address.

The conversion result of each channel is stored in left justified format and therefore occupies the upper 12 bits of the 16-bit words which occupy even addresses from 0040H up to 0066H.

The second subroutine to be used is ADC. This begins by producing a chip-select high pulse. The trailing negative edge of this pulse is rapidly followed by the transmission of channel and mode information to the converter.

List 2

```
LOC  OBJ       SOURCE

                ;* * * * * * * * * * * * * * * * * * * * *
                ;*                                                          *
                ;*   TLC2543 to H8 Microcontroller Interface Program.       *
                ;*                                                          *
                ;*  This program contains subroutines DATAIN, ADC,          *
                ;*  FORMAT and STORE.                                       *
                ;*  DATAIN reads channel number and mode data into the      *
                ;*  microcontroller via Port4. "ADC" controls A to D        *
                ;*  conversion. "FORMAT" changes conversion results from    *
                ;*  LSB first format to MSB first format. "Store" places    *
                ;*  results in memory addresses 40 to 5B (MS Bytes in even  *
                ;*  addresses, LS Bytes in odd addresses) according to      *
                ;*  channel number.                                         *
                ;* * * * * * * * * * * * * * * * * * * * *
                ;
                ; * Define special function register names *
                ;
FFDD            RDR     EQU H'FFDD          ;Receive Data Register - RDR
FFDB            TDR     EQU H'FFDB          ;Transmit Data Register - TDR
FFD8            SMR     EQU H'FFD8          ;Serial Mode Register - SMR
FFDA            SCR     EQU H'FFDA          ;Serial Control Register - SCR
FFDC            SSR     EQU H'FFDC          ;Serial Status Register - SSR
FFD9            BRR     EQU H'FFD9          ;Bit Rate Register - BRR
FFB8            P5DDR   EQU H'FFB8          ;Port5 Data Direction Register
FFBA            P5DR    EQU H'FFBA          ;Port5 Data Register - P5DR
FFB5            P4DDR   EQU H'FFB5          ;Port4 Data Direction Register
FFB7            P4DR    EQU H'FFB7          ;Port4 Data register - P4DR
FFB9            P6DDR   EQU H'FFB9          ;Port6 Data Direction register
FFBB            P6DR    EQU H'FFBB          ;Port6 Data Register


1000                    ORG H'1000          ;Sets start of program
                ;
                ; * Main Program *
                ;
1000 79001000           MOV.W #H'1000, R0
                ;       MOV.W R0, @H'0000   ;Sets reset vector to START
1004 7907FD00           MOV.W #H'FD00, SP   ;Sets contents of Stack Pointer
1008 F984       START   MOV.B #H'84, R1L    ;* * * * * * * * * * * * * * *
100A 39D8               MOV.B R1L, @SMR:8   ;* Sets up serial port        *
100C F931               MOV.B #H'31,R1L     ;* registers for simultaneous*
100E 39DA               MOV.B R1L, @SCR:8   ;* transmit and receive       *
1010 F901               MOV.B #H'01,R1L     ;*                            *
1012 39D9               MOV.B R1L, @BRR:8   ;* * * * * * * * * * * * * * *
1014 F901               MOV.B #H'01, R1L    ;Sets R1(Low Byte) to 01H
1016 6A89FFB9           MOV.B R1L, @P6DDR   ;Set Bit0 of Port6 as Output
101A 5E001082           JSR @DATAIN:16      ;Read in ADC channel/mode data
101E 5E00102C           JSR @ADC:16         ;Do A/D conversion
1022 5E0010B4           JSR @FORMAT:16      ;Reformat A/D conversion result
1026 5E0010AC           JSR @STORE:16       ;Store A/D conversion result
102A 40DC               BRA START           ;Repeat above routine.
                ;
                ; * Subroutine ADC which controls the conversion process *
                ;
102C FA05       ADC     MOV.B #H'05, R2L    ;Put 05 in R2L
102E 7FBB7000           BSET #0, @P6DR:8    ;TLC2543 chip select goes high
1032 1A0A       CSHIGH  DEC R2L             ;(R2L) - 1
1034 46FC               BNE CSHIGH          ;If not zero, CS stays high
1036 7FBB7200           BCLR #0, @P6DR:8    ;TLC2543 chip select goes low
103A 6A0CFFB7           MOV.B @P4DR, R4L    ;Puts channel/mode data in R4L
103E 731C               BTST #1, R4L        ;Is LSBF of channel/mode data
1040 461E               BNE LSBYTE          ;If not, do LSBYTE first
1042 7EDC7370   MSBYTE  BTST #7, @SSR:8     ;Is TDR empty ?
1046 47FA               BEQ MSBYTE          ;If not empty, repeat check.
1048 34DB               MOV.B R4H, @TDR:8   ;Put channel/mode data in TDR
104A 7FDC7270           BCLR #7, @SSR:8     ;Reset TDRE bit of SSR to 0
104E 7EDC7360   TESTB61 BTST #6, @SSR:8     ;Is receive shift reg. empty ?
```

List 2 (Continued)

```
LOC  OBJ                SOURCE
1052 47FA               BEQ TESTB61            ;If not empty, repeat check
1054 23DD               MOV.B @RDR:8, R3H      ;Put MS Byte of conversion
                                               ;result in R3H
1056 7FDC7260           BCLR #6, @SSR:8        ;Reset RDRF bit of SSR to 0
105A 68D3               MOV.B R3H, @R5         ;Put MS Byte in even address
                                               ;mapped by channel number.
105C 731C               BTST #1, R4L           ;Is LSBF of channel/mode data 0
105E 4620               BNE RETURN             ;If not, return from subroutine
1060 7EDC7370  LSBYTE   BTST #7, @SSR:8        ;Is TDR empty ?
1064 47FA               BEQ LSBYTE             ;If not empty, repeat check
1066 34DB               MOV.B R4H, @TDR:8      ;Put channel/mode data in TDR
1068 7FDC7270           BCLR #7, @SSR:8        ;Reset TDRE bit of SSR to 0
106C 7EDC7360  TESTB62  BTST #6, @SSR:8        ;Is receive shift reg. empty ?
1070 47FA               BEQ TESTB62            ;If not empty, repeat check
1072 0A0D               INC R5L                ;(R5L) + 1
1074 2BDD               MOV.B @RDR:8, R3L      ;Put LS Byte of conversion
                                               ;result in R3L
1076 7FDC7260           BCLR #6, @SSR:8        ;Reset RDRF bit of SSR to 0
107A 68DB               MOV.B R3L, @R5         ;Put LS Byte in odd address
                                               ;mapped by channel number.
107C 731C               BTST #1, R4L           ;Is LSBF of channel/mode data 0
107E 46C2               BNE MSBYTE             ;If not, go to MSBYTE
1080 5470      RETURN   RTS                    ;Return from subroutine
               ;
               ; * Subroutine "DATAIN" which reads in ADC channel/mode data *
               ;
1082 79040000  DATAIN   MOV.W #H'0000, R4
1086 79050000           MOV.W #H'0000, R5
108A 6A0CFFB7           MOV.B @P4DR, R4L       ;Puts channel/mode data in R4L
108E 0CCD               MOV.B R4L, R5L         ;Puts (R4L) in R5L
1090 110D               SHLR R5L               ;*  *  *  *  *  *  *  *  *  *
1092 110D               SHLR R5L               ;* Retain only channel      *
1094 110D               SHLR R5L               ;* number in R5L            *
1096 110D               SHLR R5L               ;*  *  *  *  *  *  *  *  *  *
1098 79060002           MOV.W #0002, R6        ;*  *  *  *  *  *  *  *  *  *
109C 50E5               MULXU R6L, R5          ;* Maps channel numbers to  *
109E 8D40               ADD.B #H'40, R5L       ;* even addresses 40H to 5AH*
                                               ;* Put address in R5L       *
                                               ;*  *  *  *  *  *  *  *  *  *
10A0 F008               MOV.B #H'08, R0H       ;Put 08 in R0H
10A2 110C      NEXTBIT  SHLR R4L               ;*  *  *  *  *  *  *  *  *  *  *
10A4 1204               ROTXL R4H              ;* Reformats channel/mode data*
10A6 1A00               DEC R0H                ;* from MSB first to LSB first*
10A8 46F8               BNE NEXTBIT            ;*  *  *  *  *  *  *  *  *  *  *
10AA 5470               RTS
               ;
               ; * Subroutine "STORE" stores A/D conversion results in RAM *
               ;
10AC 68D3      STORE    MOV.B R3H, @R5         ;Store MS Byte in even address
                                               ;corresponding to channel
                                               ;number
10AE 0A0D               INC R5L                ;(R5) + 1
10B0 68DB               MOV.B R3L, @R5         ;Store LS Byte in odd address
                                               ;corresponding to channel
                                               ;number
10B2 5470               RTS                    ;Return from subroutine
               ;
               ; * Subroutine "FORMAT" changes received data format   *
               ; * ( LSB first ) into MSB first format                *
               ;
10B4 F008      FORMAT   MOV.B #H'08, R0H       ;Put 08 in R0H
10B6 1103      LOOP1    SHLR R3H               ;*  *  *  *  *  *  *  *  *
10B8 1207               ROTXL R7H              ;*                        *
10BA 1A00               DEC R0H                ;*   Reformats MSBYTE     *
10BC 46F8               BNE LOOP1              ;*                        *
10BE 0C73               MOV.B R7H, R3H         ;*  *  *  *  *  *  *  *  *
10C0 F008               MOV.B #H'08, R0H       ;Put 08 in R0H
10C2 110B      LOOP2    SHLR R3L               ;*  *  *  *  *  *  *  *  *
```

List 2 (Continued)

```
   LINE   LOC    OBJ              SOURCE

136  10C4 120F               ROTXL R7L          ;*                         *
137  10C6 1A00               DEC R0H            ;*   Reformats LSBYTE      *
138  10C8 46F8               BNE LOOP2          ;*                         *
139  10CA 0CFB               MOV.B R7L, R3L     ;*  *  *  *  *  *  *  *    *
140  10CC 5470               RTS                ;Return from subroutine
141  10CE                    END
```

TLC2543 to MC68HC11 Microcontroller Interface

Microcontroller Features

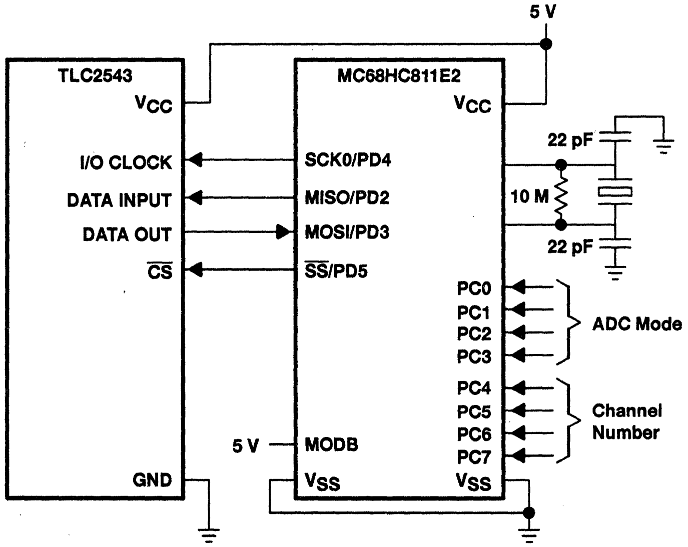
All members of the MC68HC11 family of microcontrollers contain an SPI. As is the case for the TMS370, the user is able to set the idle level of the serial clock of the 68HC11. This eliminates the need for an external inverter to be used to invert the microcontroller's serial clock output prior to its arrival at the TLC2543's serial clock input.

The 68HC11D0, 68HC11D3 and 68HC711D3 versions do not contain an on-board ADC. One of these three devices may prove to be the most cost effective choice when used with the TLC2543. All other versions contain either an 8- or 10-bit resolution ADC.

Interface Circuit

Figure 12 shows the circuit diagram of the interface between the 68HC11 and the TLC2543. The microcontroller device type used to illustrate this interface is the 48-pin dual-in-line version of the MC68HC811E2.

The master in slave out (MISO), master out slave in (MOSI) and serial clock (SCK) terminals of the SPI are available as the alternative, user selectable, functions of port D pins PD2, PD3, and PD4 respectively. When the SPI is configured to operate as a master, the $\overline{\text{SS}}$/PD5 terminal can be used as an output to drive the chip select ($\overline{\text{CS}}$) terminal of the TLC2543. This leaves all other bidirectional I/O ports of the microcontroller uncommitted and available for other uses. Note that no extra glue logic is required to implement the interface.



NOTES: A. Configured for single chip mode of operation
B. Maximum SPI data rate = crystal frequency/8

Figure 12. TLC2543 to MC68HC811E2 Microcontroller Interface

Software

The listing of the program which was written to coordinate and control the interface between the TLC2543 and the 68HC811E2 is shown in List 3. The software consists of the main program and two subroutines named TLC2543 and STORE. TLC2543 begins by providing the ADC's chip select pulse. It then reads in channel/mode data via the port C parallel I/O port and subsequently sends this data to the TLC2543 via the MOSI terminal of the SPI. At the same time, the first byte of the result from the previous analog-to-digital conversion is received at the MISO terminal of the SPI.

List 3

```
  LOC   OBJ     SOURCE

A                 * * * * * * * * * * * * * * * * * * * * * *
A                 *                                                          *
A                 * TLC2543 12-bit Serial Out ADC to MC68HC11 Microcontroller *
A                 *     Interface Program              *
A                 *                                                          *
A                 * This program contains subroutines "TLC2543" and "STORE".  *
A                 * "TLC2543" reads in ADC mode control and channel select    *
A                 * data via Port C. It then sends this data to the TLC2543   *
A                 * and at the same time receives the result of the previous  *
A                 * conversion.                                               *
A                 * "STORE" puts the results into addresses $30 to $4B with   *
A                 * MSBytes in even addresses and LSBytes in odd addresses.   *
A                 * Channel 0 result in addresses $30 and $31       *
A                 * Channel 1 result in addresses $32 and $33 etc.      *
A                 *                                                          *
A                 * * * * * * * * * * * * * * * * * * * * * *
A
A      1000       BASEADD  EQU    $1000                 Register block start
A      0000       PORTA    EQU    $00                   Port A Data Register
A      0003       PORTC    EQU    $03                   Port C Data Register
A      0007       DDRC     EQU    $07                   Port C Data Dir Reg
A      0008       PORTD    EQU    $08                   Port D Data Register
A      0009       DDRD     EQU    $09                   Port D Data Dir Reg
A      0028       SPCR     EQU    $28                   SPI Control Register
A      0029       SPSR     EQU    $29                   SPI Status Register
A      002A       SPDR     EQU    $2A                   SPI Data Register
A      00F0       MSBYTE   EQU    $F0                   MSBYTE address
A      00F1       LSBYTE   EQU    $F1                   LSBYTE address
A      00F2       TEMP     EQU    $F2                   TEMP address
A 0000
A      F800                ORG    $F800                 Start @ $F800
A                 * LDS #$0070 Set Stack Pointer
A F800 863E       START    LDAA   #$3E                  Load 3EH in AA
A F802 A709                STAA   DDRD,X                Store 3EH in DDRD
A F804 8650                LDAA   #$50                  Load 50H into AA
A F806 A728                STAA   SPCR,X                Set SPI as master
A F808 8600                LDAA   #$00                  Load 00 into AA
A F80A A707                STAA   DDRC,X                Set PORTC - all I/Ps
A F80C 1C0820              BSET   PORTD,X#$20           ;ADC CS high
A F80F BDF817              JSR    TLC2543               Do A/D conversion
A F812 BDF84A              JSR    STORE                 Store results
A F815 20E9                BRA    START                 Repeat above
A
A F817 CE1000     TLC2543  LDX    #BASEADD
A F81A 8602                LDAA   #02
A F81C 1C0820     CSHIGH   BSET   PORTD,X#$20
A                 *  Set Port A bit 6 (TLC2543 CS) high
A F81F 4A                  DECA
A F820 26FA                BNE    CSHIGH
A F822 1D0820              BCLR   PORTD,X#$20           ADC CS low
A F825 1E030210            BRSET  PORTC,X#$02 LSB       Do LSB first
A                 *    if LSBF set.
A F829 A603       MSB      LDAA   PORTC,X               Load Chan/mode data
A F82B A72A                STAA   SPDR,X                Send the data to ADC
A                 *    and receive MSByte
A F82D 1F2980FC   LOOP1    BRCLR  SPSR,X#$80 LOOP1      If SPIF=0,
A                 *   repeat check
A F831 A62A                LDAA   SPDR,X
A F833 97F0                STAA   MSBYTE                Store MSByte
A F835 1E030210            BRSET  PORTC,X#$02 RETURN
A                 * If MSB/LSB-first bit = 1, return
A F839 A603       LSB      LDAA   PORTC,X               Load chan/mode data
A F83B A72A                STAA   SPDR,X                Send the data to ADC
A                 *    and receive LSByte
A F83D 1F2980FC   LOOP2    BRCLR  SPSR,X#$80 LOOP2      If SPIF=0,
A F841 A62A                LDAA   SPDR,X                repeat check
A F843 97F1                STAA   LSBYTE                Store LSByte
A F845 1E0302E0            BRSET  PORTC,X#$02 MSB
```

List 3 (Continued)

```
   LINE   LOC    OBJ    SOURCE

69 A                   * If MSB/LSB-first bit = 1 go to MSB
70 A F849 39           RETURN     RTS
71 A                   *
72 A                   *  S'routine stores MSByte in even address
73 A                   *                    LSByte in odd address
74 A                   *  Channel 0 result in $30 and $31
75 A                   *  Channel 1 result in $32 and $33 etc.
76 A                   *  (Reserve addresses $30-$4B for results
77 A                   *   of all channels)
78 A F84A A603         STORE      LDAA       PORTC,X
79 A F84C CE0030                  LDX        #$30
80 A F84F 97F2                   STAA       TEMP
81 A F851 86F0                   LDAA       #$F0
82 A F853 94F2                   ANDA       TEMP
83 A F855 46                     RORA
84 A F856 46                     RORA
85 A F857 46                     RORA
86 A F858 46                     RORA
87 A F859 16                     TAB
88 A F85A 8602                   LDAA       #$02
89 A F85C 3D                     MUL
90 A F85D DDF2                   STD        TEMP
91 A F85F 96F0                   LDAA       MSBYTE
92 A F861 A7F2                   STAA       TEMP,X
93 A F863 08                     INX
94 A F864 96F1                   LDAA       LSBYTE
95 A F866 A7F2                   STAA       TEMP,X
95 A F866 A7F2                   STAA    TEMP,X
96 A F868 39                     RTS
97 A                             END
```

TLC2543 to 80C51 Microcontroller Interface

Microcontroller Features

The 80C51 microcontroller family does not provide an SPI or equivalent facility. In order to implement the interface with the TLC2543 analog-to-digital converter, it is necessry to use software to synthesize the operation of an SPI. This results in a slower data transfer rate which is governed by the microcontroller's instruction cycle times. These are, in turn, influenced by the clock frequency of the microcontroller. The highest clock frequency possible should therefore be selected for the microcontroller to minimize instruction cycle times and thus optimize the data transfer rate of the interface.

Interface Circuit

Figure 13 shows the circuit for the interface of the TLC2543 to the 80C51 microcontroller. The I/O CLOCK, DATA INPUT and $\overline{CS}$ inputs to the TLC2543 are provided via the bidirectional parallel port 1 terminals P1.0, P1.1, and P1.3 respectively. Conversion result data from the TLC2543 is received by the 80C51 through the P1.2 terminal of port 1. The channel select/mode data is input to the microcontroller via port 3.

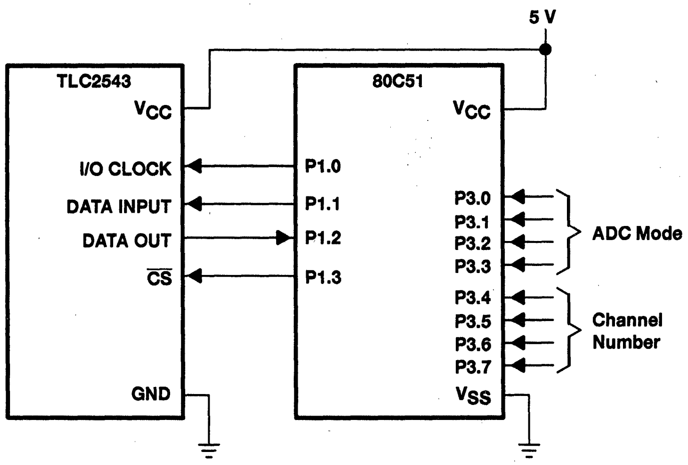


Figure 13. TLC2543 to 80C51 Microcontroller Interface

Software

The listing for the program used to control the interface circuit mentioned above is shown in List 4. As for the other microcontroller interface programs, it consists of a main program and two subroutines – TLC2543 and STORE.

The main program initializes the directions of the port 1 I/O terminals. P1.2 is configured as an input. P1.0, P1.1, and P1.3 are all programmed to perform as outputs. The chip select terminal of the TLC2543 is set high by setting P1.3. TLC2543 is then called. This subroutine contains the instructions which synthesize the SPI function and controls the exchange of data between the microcontroller and the TLC2543. The least significant bit first (LSBF) flag which is bit 1 of the channel select/mode data byte is checked to determine which byte (most significant – MSByte, least significant – LSByte) of the conversion result is to be expected first.

The SPI function is synthesized by using the accumulator in conjunction with the rotate left through carry (RLC) instruction to act as the SPI shift register. The following sequence provides a slow motion version of the SPI function.

The first bit of the first byte of the conversion result is read into the carry (C) bit. The contents of the accumulator are rotated left through carry and the first bit of the channel select/mode data is then output from P1.1. The first pulse of the serial clock is then provided by toggling the P1.0 bit of port 1 first high and then low. This sequence is repeated seven more times to complete the transfer of the first byte of data.

The second byte of data is tranferred between the TLC2543 and the 80C51 by repeating the entire sequence of eight sets of data transfer and clock pulse. The MSByte is placed in register 2 (R2) and the LSByte is placed in register 3 (R3). The subroutine STORE is used to map the MSByte and LSByte conversion results into even and odd number RAM addresses corresponding to the particular channel number which has been selected.

List 4

```
     LINE   LOC   OBJ   SOURCE
                    ;*  *  *  *  *  *  *  *  *  *  *  *  *  *  *
                    ;*                                          *
                    ;*  TLC2543 12-bit Serial Out ADC to 80C51  *
                    ;*                                          *
                    ;*  Microcontroller Interface Program       *
                    ;*                                          *
                    ;*  *  *  *  *  *  *  *  *  *  *  *  *  *  *
                    ;This program reads mode/channel select data into the
                    ;80C51 via Port 4 and transmits this data to the
                    ;TLC2543 at the same time as reading the result from
                    ;the previous conversion and storing the result in an
                    ;adjacent pair of memory locations from 30H to 4CH.
                    ;MSByte - Even Address  LSByte - Odd Address
                    ;MSByte Channel 0 in 30H, MSByte Channel 1 in 32H etc.
                    ;
0100                        ORG 100H
0100 758150         START:  MOV SP,#50H       ;Initialise Stack Pointer
0103 759004                 MOV P1,#04H       ;Initialize port 1 I/O Pins
0106 C290                   CLR P1.0          ;Set I/O clock low
0108 D293                   SETB P1.3         ;Set chip select high
010A 74FF                   MOV A,#00FFH
010C 3112                   ACALL TLC2543
010E 313F                   ACALL STORE
0110 80EE                   JMP START

0112 ACB0           TLC2543:MOV R4,P3         ;Read mode/channel data into R4
0114 EC                     MOV A,R4          ;and A
0115 C293                   CLR P1.3          ;Set chip select low
0117 20E112                 JB ACC.1,LSB      ;If bit 1 of A is 1,
                                              ;do LSByte first
011A 7D08           MSB:    MOV R5,#08        ;Load MS bit counter
011C A292           LOOP1:  MOV C,P1.2        ;Read data bit into carry
011E 33                     RLC A             ;Rotate into accumulator
011F 9291                   MOV P1.1,C        ;Output mode/channel bit
0121 D290                   SETB P1.0         ;Set I/O clock high
0123 C290                   CLR P1.0          ;Set I/O clock low
0125 DDF5                   DJNZ R5,LOOP1     ;Get/send another bit
0127 FA                     MOV R2,A          ;Put MSByte in R2
0128 EC                     MOV A,R4          ;Put mode/channel data in A
0129 20E112                 JB ACC.1,RETURN   ;
012C 7D08           LSB:    MOV R5,#08        ;Load LS bit counter
012E A292           LOOP2:  MOV C,P1.2        ;Read data bit into carry
0130 33                     RLC A             ;Rotate into accumulator
0131 9291                   MOV P1.1,C        ;Output mode/channel bit
0133 D290                   SETB P1.0         ;Set I/O clock high
0135 C290                   CLR P1.0          ;Set I/O clock low
0137 DDF5                   DJNZ R5,LOOP2     ;Get/send another bit
0139 FB                     MOV R3,A          ;Put LSByte in R3
013A EC                     MOV A,R4          ;Put mode/channel data in A
013B 20E1DC                 JB ACC.1,MSB      ;If bit 1 of R4 is 1,
                                              ;do MSbyte next
013E 22             RETURN: RET

013F EC             STORE:  MOV A,R4          ;Put mode/channel data in A
0140 54F0                   ANL A,#0F0H       ;Retain only channel number
0142 C4                     SWAP A            ;Swap high and low nibble of A
0143 75F002                 MOV B,#02
```

List 4 (Continued)

```
     LINE    LOC    OBJ    SOURCE

0146 A4                         MUL AB
0147 2430                       ADD A,#030H      ;Add 30H to accumulator
0149 F9                         MOV R1,A
014A EA                         MOV A,R2
014B F7                         MOV @R1,A        ;Put MSByte in corresponding
                                                 ;even number address :-
                                                 ;Channel 0 in address 30H,
                                                 ;Channel 1 in address 32H etc.
014C 09                         INC R1
014D EB                         MOV A,R3
014E F7                         MOV @R1,A        ;Put LSByte in corresponding
                                                 ;odd number address :-
                                                 ;Channel 0 in address 31H,
                                                 ;Channel 1 in address 33H etc.
014F 22                         RET
                                END
```

Analog Considerations

Power Supply Decoupling

Care should be taken with the design of the printed circuit board when using 12-bit devices such as the TLC2543. The power supply terminal of each analog integrated circuit should be separately decoupled to the analog ground using a 0.1 µF ceramic capacitor. The inclusion of a 10 µF tantalum capacitor in parallel with the ceramic capacitor at each device supply terminal is also recommended, particularly in noisy environments.

Grounding

Separate ground return paths for analog and digital components back to the power supply should be used to prevent any noise currents induced by digital components from passing through the analog ground return path. These noise currents can induce noise voltages to occur in the analog ground return and thus corrupt the analog signal. Remember that, for a 5-V full scale signal, only 600 microvolts represents approximately half an LSB for a 12-bit ADC.

The important point to remember is that all ground return paths have a finite impedance. This impedance should be kept to a minimum by the use of wide printed circuit board tracks or ground planes where possible. A separate star connected ground topology is recommended for the analog components. This involves connecting each analog component's ground terminal to a central star point, which can then be connected via a wide printed circuit track to the power supply ground connection.

Board Layout

Digital devices and power switching elements should be kept as far away physically from analog components, such as the TLC2543, as possible. Particular attention should be paid to the use of switching power supplies. The high frequency switching currents which flow in the ground return paths of these space saving power blocks can introduce several LSBs of noise into 12-bit analog circuits. Linear regulated power supplies should be used or, if essential, switching regulators should be as far as possible from the analog circuitry with their outputs decouple.

Judicious use of ground planes can help to reduce analog ground impedances.

Figure 14 illlustrates a typical bypassing scheme for the TLC2543-to-TMS370 microcontroller interface.

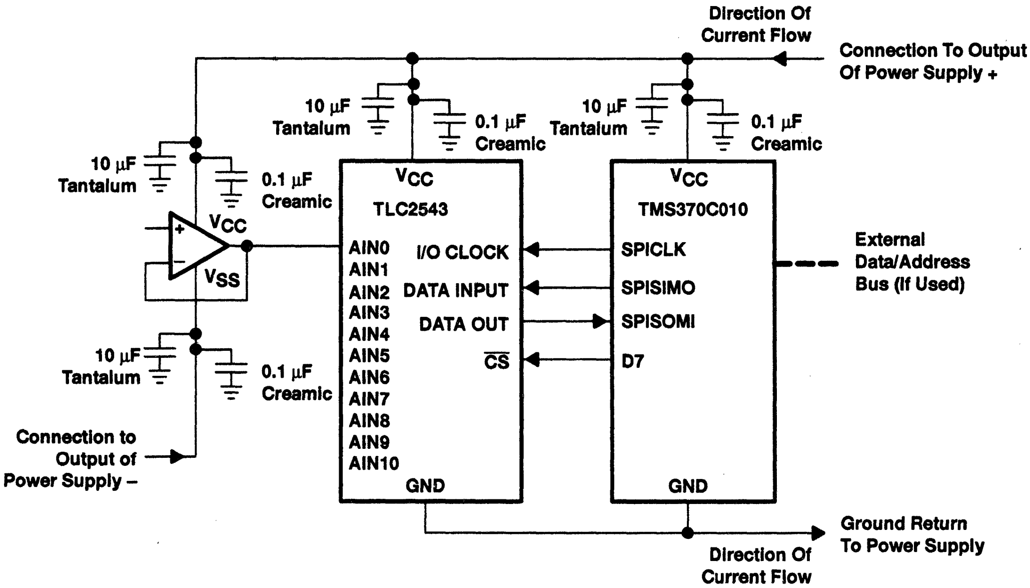


Figure 14. TLC2543 to Microcontroller Interface: Grounding and Decoupling Scheme

Appendix A

References

H8/325 Hardware User's Manual	Hitachi
H8/300 Series Programming Manual	Hitachi
Embedded Microcontrollers and Processors Vol 1	Intel Corporation
M68HC11 Reference Manual (1991)	Motorola Inc.
TMS370 Family Data Manual (1993)	Texas Instruments Incorporated
TLC2543 Data Sheet (Dec. '93)	Texas Instruments Incorporated

Acknowledgement

I wish to express my thanks to Mike Williams (Microcontroller Field Applications Engineer – Northern European Industrial Segment) for his useful comments on the TMS370 interface.

Interfacing the TLC32040 Family to the TMS320 Family

TEXAS INSTRUMENTS

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1 Introduction

The TLC32040 and TLC32041 analog interface circuits are designed to provide a high level of system integration and performance. The analog interface circuits combine high resolution A/D and D/A converters, programmable filters, digital control and timing circuits as well as programmable input amplifiers and multiplexers. Emphasis is placed on making the interface to digital signal processors (the TMS320 family) and most microprocessors as simple as possible. This application report describes the software and circuits necessary to interface to numerous members of the TMS320 family. It presents three circuits for interfacing the TLC32040 Analog Interface Circuit to the TMS320 family of digital signal processors. Details of the hardware and software necessary for these interfaces are provided.

To facilitate the discussion of the software the following definitions and naming conventions are used:

1. >nnnn – a number represented in hexadecimal.
2. Interrupt service routine – a subroutine called in direct response to a processor interrupt.
3. Interrupt subroutine – any routine called by the interrupt service routine.
4. Application program (application routine) – the user's application dependent software (e.g., digital filtering routines, signal generation routines, etc.)

2 TLC32040 Interface to the TMS32010/E15

2.1 Hardware

Because the TLC32040 (Analog Interface Circuit) is a serial-I/O device, the interface to the TMS32010, which has no serial port, requires a small amount of glue-logic. The circuit shown in Figure 1 accomplishes the serial-to-parallel conversion for the AIC operating in synchronous mode.

2.1.1 Parts List

The interface circuit for the TMS32010 uses the following standard logic circuits:

1. One SN74LS138 3-to-8-line address decoder
2. One SN74LS02 Quad NOR-Gate
3. One SN74LS00 Quad NAND-Gate
4. One SN74LS04 Hex Inverter
5. One SN74LS74 Dual D-Flip-Flop
6. Two SN74LS299 8-bit Shift Registers

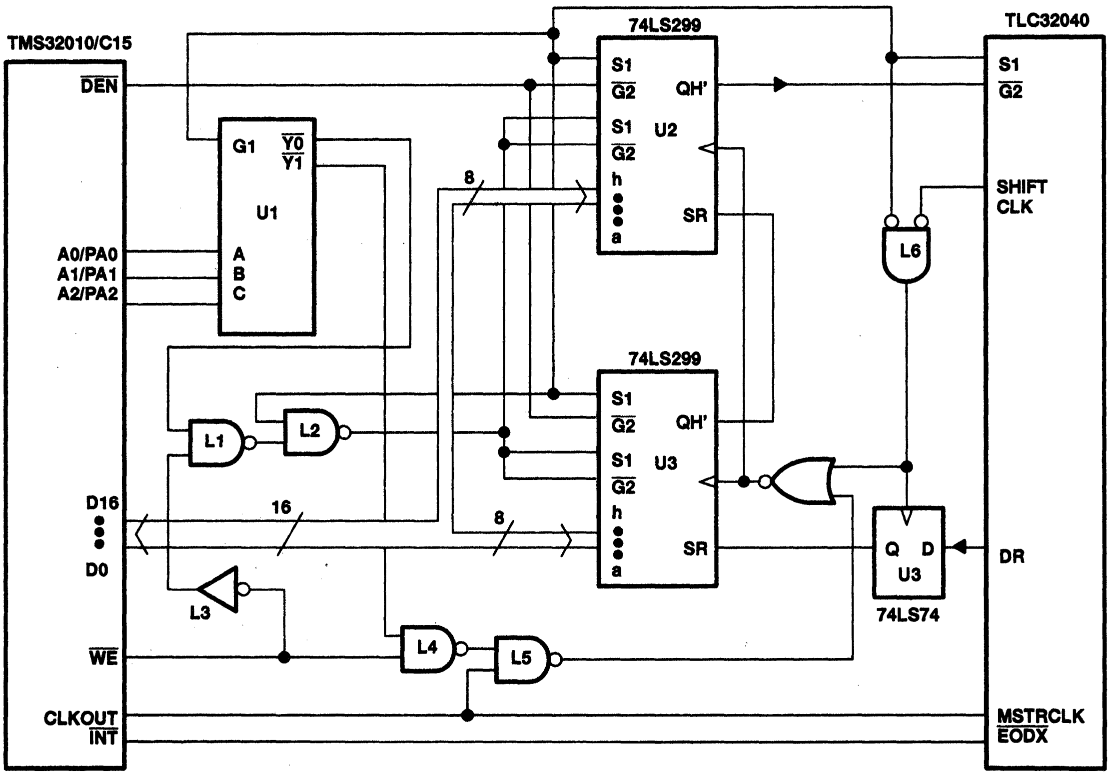


Figure 1. AIC Interface to TMS32010/E15

2.1.2 Hardware Description

The SN74LS138 is used to decode the addresses of the ports to which the TLC32040 and the interface logic have been mapped. If no other ports are needed in the development system, this device may be eliminated and the address lines of the TMS32010 used directly in place of $\overline{\mathrm{Y1}}$ and $\overline{\mathrm{Y0}}$ (see Figure 1).

Since the interface circuits are only addressed when the TMS32010 executes an IN or an OUT instruction, gates L1, L2, L3, L4, and L5 are required to enable reading and writing to the shift registers only on these instructions. The TBLW instruction is prohibited because it has the same timing as the OUT instruction. Flip-flop U4 ensures that the setup and hold times of SN74LS299 shift registers are met.

Although not shown in the circuit diagram, it is recommended that the $\overline{\mathrm{CLR}}$ pins of the SN74LS299 shift registers as well as the $\overline{\mathrm{RESET}}$ pin of the AIC be tied to the power-up reset circuit shown in the AIC data sheet. This ensures that the registers are clear when the AIC begins to transfer data and decrease the possibility that the AIC will shift in bad data which could cause the AIC to shut down or behave in an unexpected manner.

2.2 Software

The flowcharts for the communication program along with the TMS32010 program listing are presented in Appendix A. If this software is to be used, and application program that moves data into and out of the transmit and receive registers must be supplied.

2.2.1 Initializing the Digital Signal Processor

As shown in the flowcharts in Appendix A, the program begins with an initialization routine which clears both the transmit/receive-end flag and the secondary communication flag, and stores the addresses of the interrupt subroutines. The program uses the MPYK...PAC instruction sequence to load data memory locations with the 12-bit address of the subroutines. This sequence is only necessary if the subroutines are to reside in program memory locations larger than >00FF. Otherwise, the instructions LACK and SACL may be used to initialize the subroutine-address storage locations.

2.2.2 Communicating with the TLC32040

After the storage registers and status register have been initialized, the interrupt is enabled and control is passed to the user's application routine (i.e., the system-dependent software that processes received data and prepares data for transmission). The program ignores the first interrupt that occurs after interrupts are enabled (page 22, line 207, IGINT routine), allowing the AIC to stabilize after a reset. The application routine should not write to the shift registers while data is moving into (and out of) them. In addition, it should ensure that no primary data is written to the shift registers between a primary and secondary data-communication pair. The first objective can be accomplished by writing to the SN74LS299 shift registers as quickly as possible after the receive interrupt. The number of instruction cycles between the data transfers can be calculated from the conversion frequency. By counting instruction cycles in the application program, it is possible to determine whether the data transfer will conflict with the OUT instruction to the shift register. The second objective can be accomplished by monitoring SNDFLG in the application program. If SNDFLG is true (>00FF), secondary communication has not been completed.

When the processors receives an interrupt, the program counter is pushed onto the hardware stack and then the program counter is set to >0002, the location of the interrupt service routine, INTSVC (page 19, line 46). The interrupt service routine then saves the contents of the accumulator and the status register and calls the interrupt subroutine to which XVECT points. If secondary communication is to follow the upcoming primary communication, XVECT, is set by the application program to refer to SINT1, otherwise, XVECT defaults to NINT (i.e., the normal interrupt routine).

Because the interrupt subroutine makes one subroutine call and uses two levels of the hardware stack, the application program can only use two levels of nesting (i.e., if stack extension is not used). This means that any subroutine called by the application program can only call subroutines containing no instructions that use the hardware stack (e.g., TBLW) and that make no other subroutine calls. In addition, if the application program and communication program are being implemented on an XDS series emulator, the emulator consumes one level of the hardware stack and allows the application program only one level of nesting (i.e., one level of subroutine calls).

As shown in the flowcharts in Appendix A, the normal interrupt routine reads the A/D data from the shift registers and then sets the receive/transmit end-flag (RXEFLG). The application program must write the outgoing D/A data word to the shift registers at a time convenient to the application routine. It should have the restriction that the data be written before the next data transfer.

2.2.3 TLC32040 Secondary Communication

If it is necessary to write to the control register of the AIC or configure any of the AIC internal counters, the application program must initiate a primary/secondary communication pair. This can be accomplished by placing a data word in which bits 0 and 1 are both high into DXMT, placing the secondary control word (see program listing page 19) in D2ND, and placing the address of the secondary communication subroutine, SINT1, in XVECT. When the next interrupt occurs, the interrupt subroutine will call routine SINT1. SINT1 reads the A/D information from the shift registers and writes the secondary communication word to the shift registers.

3 TLC32040 Interface to the TMS32020/C25

3.1 Hardware Description

Because the TLC32040 is designed specifically to interface with the serial port of the TMS32020/C25, the interface requires no external hardware. Except for CLKR and CLKX, there is a one-to-one correspondence between the serial port control and data pins of TMS32020 and TLC32040. CLKR and CLKX are tied together since both the transmit and the receive operations are synchronized with SHIFT CLK of the TLC32040. The interface circuit, along with the communication program (page 26), allows the AIC to communicate with the TMS32020/C25 in both synchronous and asynchronous modes. See Figures 2, 3, and 4.

3.2 Software

The program listed in Appendix B allows the AIC to communicate with the TMS32020 in synchronous or asynchronous mode. Although originally written for the TMS32020, it will work just as well for the TMS320C25.

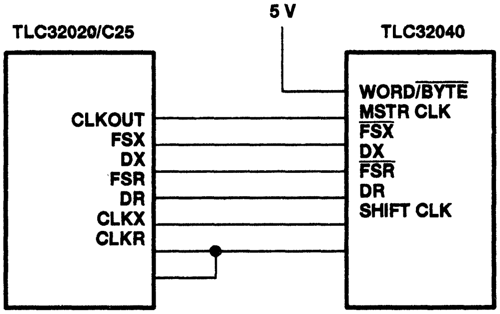
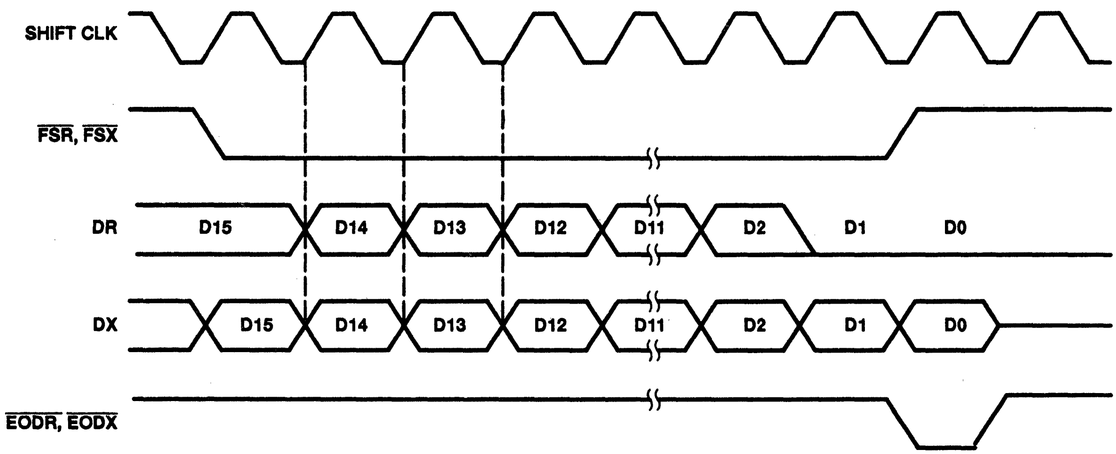


Figure 2. AIC Interface to TMS32020/C25



The sequence of operation is:
1. The FSX or FSR pin is brought low.
2. One 16-bit word is transmitted or one 16-bit byte is received.
3. The FSX or FSR pin is brought high.
4. The EODX or EODR pin emits a low-going pulse as shown.

Figure 3. Operating Sequence for AIC-TMC32020/C25 Interface

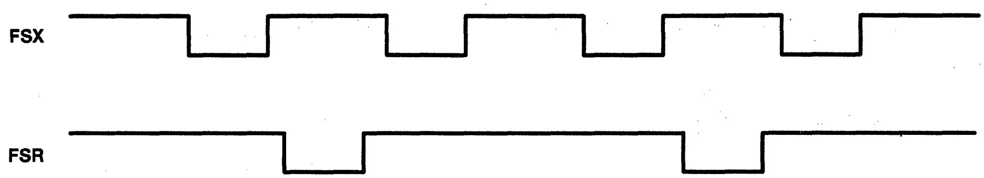


Figure 4. Asynchronous Communication AIC-TMS32020/C25 Interface

3.2.1 Initializing the TMS32020/C25

This program starts by calling the initialization routine. The working storage registers for the communication program and the transmit and receive registers of the DSP are cleared, and the status registers and interrupt mask register of the TMS32020/C25 are set (see program flow charts in Appendix B). The addresses of the transmit and receive interrupt subroutines are placed in their storage locations, and the addresses of the routines which ignore the first transmit and receive interrupts are placed in the transmit and receive subroutine pointers (XVECT and RVECT). The TMS32020/C25 serial port is configured to allow transmission of 16-bit data words (FO), the serial port format bit of the TMS32020/C25 must be set to zero) with an externally generated frame synchronization ($\overline{\text{FSX}}$ and $\overline{\text{FXR}}$ are inputs, TXM bit is set to 0).

3.2.2 Communicating with the TLC32040

After the TMS32020/C25 has been initialized, interrupts are enabled and the program calls subroutine IGR. The processor is instructed to wait for the first transmit and receive interrupts (XINT and RINT) and ignore them. After the TMS32020 has received both a receive and a transmit interrupt, the IGR routine will transfer control back to the main program and IGR will not be called again.

If the transmit interrupt is enabled, the processor branches to location 28 in program memory at the end of a serial transmission. This is the location of the transmit interrupt service routine. The program context is saved by storing the status registers and the contents of the accumulator. Then the interrupt service routine calls the interrupt subroutine whose address is stored in the transmit interrupt pointer (XVECT).

A similar procedure occurs on completion of a serial receive. If the receive interrupt is enabled, the processor branches to location 26 in program memory. As with the transmit interrupt service routine (XINT, page 30, line 226), the receive interrupt service routine (page 30, line 194) saves context and then calls the interrupt subroutine whose address is stored in the receive interrupt pointer (RVECT). It is important that during the execution of either the receive or transmit interrupt service routines, all interrupts are disabled and must be re-enabled when the interrupt service routine ends.

The main program is the application program. Procedures such as digital filtering, tone-generation and detection, and secondary communication judgment can be placed in the application program. In the program listing shown in Appendix B, a subroutine (C2ND) is provided which will prepare for secondary communication. If secondary communication is required, the user must first write the data with the secondary code to the DXMT register. This data word should have the two least significant bits set high (e.g., >0003). The first 14 bits transmitted will go to the D/A converter and the last two bits indicate to the AIC that secondary communication will follow. After writing to the SXMT register, the secondary communication word should be written to the D2ND register.

This data may be used to program the AIC internal counters or to reconfigure the AIC (e.g., to change from synchronous to asynchronous mode or to bypass the bandpass filter). After both data words are stored in their respective registers, the application program can then call the subroutine C2ND which will prepare the TMS32020 to transmit the secondary communication word immediately after primary communication.

3.2.3 Secondary Communicating – Special Considerations

This communication program disables the receive interrupt (RINT) when secondary communication is requested. Because of the critical timing between the primary and secondary communication words and because RINT carries a higher priority than the transmit interrupt, the receive interrupt cannot be allowed to interrupt the processor before the secondary data word can be written to the data-transmit register. If this situation were to occur, the AIC would not receive the correct secondary control word and the AIC could be shut down.

In many applications, the AIC internal registers need only be set at the beginning of operation, (i.e., just after initialization). Thereafter, the DSP only communicates with the AIC using primary communication. In cases such as these, the communication program can be greatly simplified.

4 TMS32040 Interface to the TMS320C17

4.1 Hardware Description

As shown in Figure 5, the TMS320C17 interfaces directly with the TLC32040. However, because the TMS320C17 responds more slowly to interrupts than the TMS32010/E15 or the TMS32020/C25, additional circuit connections are necessary to ensure that the TMS320C17 can respond to the interrupt, accomplish the context-switching that is required when an interrupt is serviced, and proceed with the interrupt vector. This must all be accomplished within the strict timing requirements imposed by the TLC32040. To meet these requirements, $\overline{\text{FSX}}$ of the TLC32040 is connected to the $\overline{\text{EXINT}}$ pin of the TMS320C17. This allows the TMS320C17 to recognize the transmit interrupt before the transmission is complete. This allows the interrupt service routine to complete its context-switching while the data is being transferred. The interrupt service routine branches to the interrupt subroutines only after the FSX flag bit has been set. This signals the end of data transmission.

The other hardware modification involves connecting the $\overline{\text{EODX}}$ pin of the TLC32040 to the $\overline{\text{BIO}}$ pin of the TMS320C17. Because the TMS320C17 serial port accepts data in 8-bit bytes (see Figure 6) and the TLC32040 controls the byte sequence (i.e., which byte is transmitted first, the high-order byte or the low-order byte) it is important that the TMS320C17 be able to distinguish between the two transmitted bytes. The $\overline{\text{EODX}}$ signal is asserted only once during each transmission pair, making it useful for marking the end of a transmission pair and synchronizing the TMS320C17 with the AIC byte sequence. After synchronization has been established, the $\overline{\text{BIO}}$ line is no longer needed by the interface program and may be used elsewhere.

Because the TMS320C17 serial port operates only in byte mode, 16-bit transmit data should be separated into two 8-bit bytes and stored in separate registers before a transmit interrupt is acknowledged. Alternatively, the data can be prepared inside the interrupt service routine before the interrupt subroutine is called. From the time that the interrupt is recognized to the end of the data transmission is equivalent to 28 TMS320C17 instruction cycles.

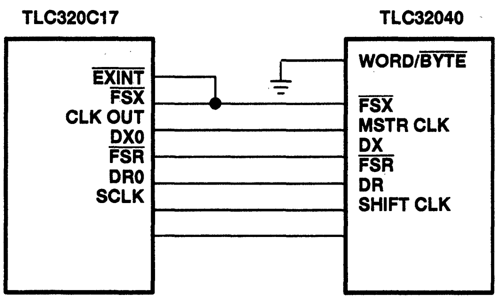
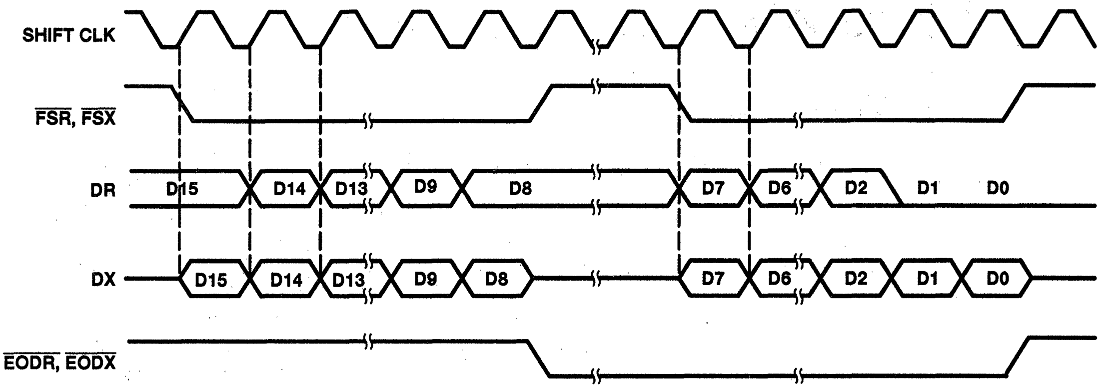


Figure 5. AIC Interface to TMS320C17



The sequence of operation is:
1. The FSX or FSR pin is brought low.
2. One 8-bit word is transmitted or one 8-bit byte is received.
3. The EODX or EODR pins are brought low.
4. The FSX or FSR emit a positive frame-sync pulse that is four shift clock cycles wide.
5. One 8-bit byte is transmitted and one 8-bit byte is received.
6. The EODX and EODR pins are brought high.
7. The FSX and FSR pins are brought high.

Figure 6. Operating Sequence for AIC-TMS320C17

4.2 Software

The software listed in Appendix C only allows the AIC to communicate with the TMS320C17 in synchronous mode. This communication program is supplied with an application routine, DLB (Appendix C, program listing line 253), which returns the most recently received data word back to the AIC (digital loopback).

4.2.1 Initializing the TMS320C17

The program begins with an initialization routine (INIT, page 40, line 120). Interrupts are disabled and all the working storage registers used by the communication program are cleared. Both transmit registers are cleared, the constants used by the program are initialized and the addresses of the subroutines called by the program are placed in data memory. This enables the interrupt service routine to call subroutines located in program-memory addresses higher than 255. After the initialization is complete, the TMS320C17 monitors the FSX interrupt flag in the control register to establish synchronization with the AIC.

4.2.2 AIC Communications and Interrupt Management

Because the AIC FSX pin is tied to the EXINT line of the TMS320C17 and the delay through the interrupt multiplexer, the interrupt service routine is called four instruction cycles after the falling edge of FSX. The interrupt service routine (INTSVC, Appendix C, program listing, line 90) completes its context switching and then monitors the lower control register, polling the FSX flag bit that indicates the end of the 8-bit serial data transfer. If the FSX flag bit is set, the transfer is complete. After this bit is set, control is transferred to the interrupt subroutine whose address is stored in VECT. The serial communication must be complete before data is read from the data receive register.

When no secondary communication is to follow, the interrupt subroutines, NINT1 and NINT2, are called. If data has been stored in DXMT2 (the low-order eight bits of the transmit data word), which does not indicate that secondary communication is to follow, the interrupt service routine calls NINT1 when the first 8-bit serial transfer is complete. NINT1 immediately writes the second byte of transmit data, (i.e., the contents of DXMT2) to transmit data register 0 (TR0). It then moves the first byte of the received data (i.e., the high-order byte of the A/D conversion result) into DRCV1. NINT1 then stores in VECT the address of NINT2. NINT2 is called at the end of the next 8-bit data transfer and resets the FSX interrupt flag bit by writing a logic high to it. The next interrupt (a falling edge of EXINT) occurs before the interrupt service routine returns control to the main program. This is an acceptable situation since the TMS320C17, on leaving the interrupt service routine, recognizes that an interrupt has occurred and immediately responds by servicing the interrupt.

The interrupt subroutine NINT2 is similar in operation to NINT1. It stores the low-order byte of receive data (bits 7 through 0 of the A/D conversion result) and stores the address of the next interrupt subroutine in VECT. NINT2 does not write to the transmit data register, TR0. This task has been left to the application program. After the transmit data has been prepared by the main program and the data has been stored in DXMT1 and DXMT2, the main program stores the first byte of the transmit data in transmit data register 0 (TR0).

4.2.3 Secondary Communications

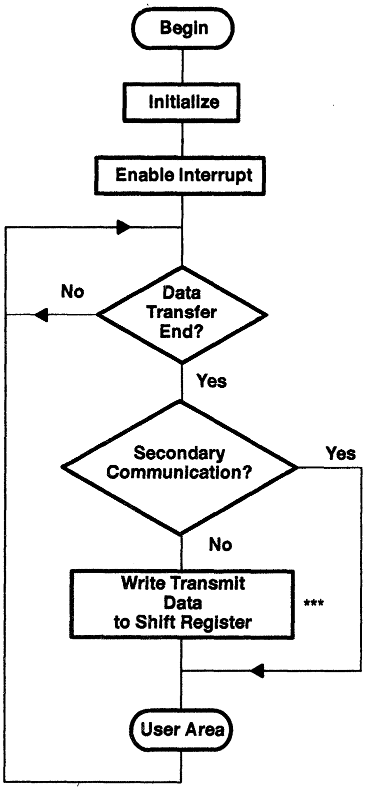
The interrupt subroutines SINT1 through SINT4 are called when secondary communication is required. For secondary communication, DXMT1 and DXMT2 will hold the primary communication word. DXMT3 and DXMT4 will hold the secondary communication word. VECT, the subroutine pointer should then be initialized to the address of SINT1. As with the normal (primary communication only) interrupt subroutines (i.e., NINT1 and NINT2), the secondary communication routines will change VECT to point to the succeeding routine (e.g., SINT1 will point to SINT2, SINT2 will point to SINT3, etc.).

5 Summary

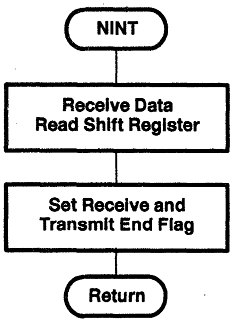
The TLC32040 is an excellent choice for many digital signal processing applications such as speech recognition/storage systems and industrial process control. The different serial modes of the AIC (synchronous, asynchronous, 8- and 16-bit) allow it to interface easily with all of the serial port members of the TMS320 family as well as other processors.

A TLC32040 and TMS32010 Flowcharts and Communication Program

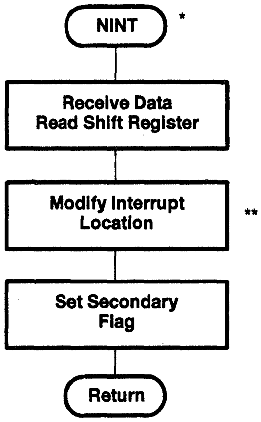
A.1 Flowcharts



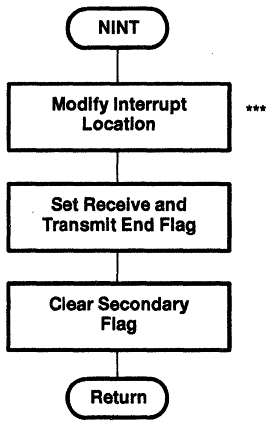
a. MAIN



b. PRIMARY INTERRUPT ROUTINE



c. SECONDARY DATA COMMUNICATIONS 1



d. SECONDARY DATA COMMUNICATIONS 2

* Set, if need secondary.
** Modify to call SINT2.
*** Modify to call NINT.
**** Must execute before transfer beginning.

A.2 Communication Program List

```
                ***********************************************************
                * When using this program, the circuit in the TLC32040   *
                * data sheet or its equivalent circuit must be fused     *
                * port 1 are reserved for data receiving and data        *
                * transmitting. The TBLW command is prohibited because   *
                * it has the same timing as the OUT command. TLC32040 is *
                * used only in synchronous mode.                         *
                ***********************************************************
                *
          0002  RXEFLG    EQU   >02   receive and xmit end flag.
          0003  SNDFLG    EQU   >03   secondary communication flag.
          0004  DRCV      EQU   >04   receive data storage.
          0005  DXMT      EQU   >05   xmit data storage.
          0006  D2ND      EQU   >06   secondary data storage.
          0007  XVECT     EQU   >07   interrupt address storage.
          0008  ACHSTK    EQU   >08   ACCH stack.
          0009  ACLSTK    EQU   >09   ACCL stack.
          000A  SSTSTK    EQU   >0A   Status stack.
          000C  ANINT     EQU   >0C   interrupt address 1
          000D  ASINT1    EQU   >0D   interrupt address 2
          000E  ASINT2    EQU   >0E   interrupt address 3
          000F  TMP0      EQU   0F    temporary register.
                *
          00FF  SET       EQU   >FF
          0001  ONE       EQU   >01
                *    =================
                *       Reset vector.
                          =================
     0000                 AORG  >0000 program start address.
     0000 F900            B     EPIL  jump to initialization.
     0001 000D

                ***********************************************************
                * =================                                       *
                * Interrupt vector.                                       *
                * =================                                       *
                * When secondary communication, modify the content of    *
                * XVECT to the address of secondary communication and    *
                * store secondary data in D2ND.                          *
                * ex.                                                    *
                *         LAC   ASINT1,0  modify XVECT                   *
                *         SACL  XVECT,0                                  *
                *               |                                        *
                *         LAC   D2ND,0    store secondary data.          *
                ***********************************************************
```

```
0002                    AORG   >0002      interrupt vector.
0002
0002  7C0A  INTSVC      SST    SSTSTK     push status register.
0003  6E01              LDPK   ONE        set data pointer one.
0004  5808              SACH   ACHSTK     push ACCH.
0005  5009              SACL   ACLSTK     push ACCL.
0006  2007              LAC    XVECT,0    load interuput address.
0007  7F8C              CALA              branch to interruupt routine.
0008  6508              ZALH   ACHSTK     pop ACCH
0009  7A09              OR     ACLSTK     pop ACCL.
000A  7B0A              LST    SSTSTK     pop stack register.
000B  7F82              EINT              enable interrupt.
000C  7F8D              RET               return from interrupt routine.
            ********************************************************
            *           ===========================                *
            *           Initialization after reset.                *
            *           ==========================                 *
            *                                                      *
            *     Data RAM locations 82H(130) through 8FH(143),    *
            *     12 words of page 1, are reserved for this        *
            *     program. The user must set the status register   *
            *     by adding the SST command at the end of the      *
            *     the initialization routine.                      *
            ********************************************************
            *
            *
            *
000D                    AORG   $          initial program.
000D
000D  6E01  EPIL        LDPK   ONE        set data page pointer one.
000E
000E  7E01              LACK   ONE        save normal communication
000F  500F              SACL   TMP0       address to its storage.
0010  6A0F              LT     TMP0
0011  802C              MPYK   NINT
0012  7F8E              PAC
0013  500C              SACl   ANINT
0014
0014  8030              MPYK   SINT1      save secondary communication
0015  7F8E              PAC               address1 to its storage.
0016  500D              SACL   ASINT1
0017
0017  8037              MPYK   SINT2      save secondary communication
0018  7F8E              PAC               address2 to its storage.
0019  500E              SACL   ASINT2
001A
001A  803A              MPYK   IGINT      ignore interrupt once after
001B  7F8E              PAC               master reset.
001C  5007              SACL   XVECT
001D
001D  7F89              ZAC               clear flags.
001E  5002              SACL   RXFLG,0
001F
001F  5003              SACL   SNDFLG,0
```

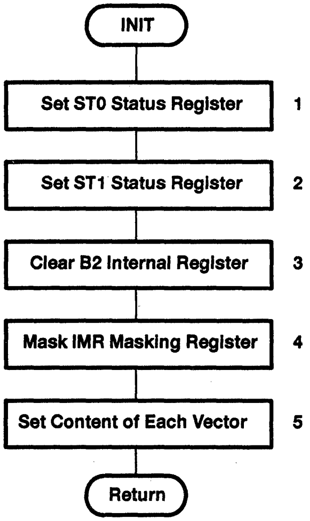
```
0020
0020
0020
0020  7F82        EINT            enable interrupt.
            *
            *********************************************************
            *         ==============                                *
            *         Main program.                                 *
            *         =============                                 *
            *                                                       *
            *  This program allows the user two levels of nesting   *
            *  since one level is used as stack for the interrupt.  *
            *  When the RXEFLG flag is false then no data transfer  *
            *  has ocurred, if it is true then data transfer has    *
            *  finished. User rountines such as digital filter,     *
            *  secondary-data-communication judgement etc., must be *
            *  placed in this location. Depending on the sampling   *
            *  rate (conversion rate), these user routines must     *
            *  write the xmit data to the shift registers within    *
            *  approximately 500 instruction cycles. If the user    *
            *  requires secondary communication, it will be         *
            *  necessary to delay the OUT instruction until the     *
            *  secondary data transfer has finished.                *
0021        *********************************************************
0021  2002  MAIN  LAC   RXEFLG,0  wait for interrupt.
0022  FF00        BZ    MAIN
0023  0021
0024
0024  2003        LAC   SNDFLG,0  skip OUT instruction during
0025  FE00        BNZ   MAIN1     secondary communication.
0026  0028
0027
0027  4905        OUT   DXMT,PA1  write xmit data to shift register.
0028
0028  7F89  MAIN1 ZAC             clear flags.
0029  5002        SACL  RXEFLG
002A
002A  F900        B     MAIN      loop.
002B  0021
            *
            *********************************************************
            *         =========================                     *
            *         Normal interrupt rountine.                    *
            *         ==========================                    *
            *                   destroy ACC, DP.                    *
            *                                                       *
            *  Write the contents of DXMT to the 'LS299s, receive   *
            *  DAC data in DRCV, and set RXEFLG flag.               *
            *********************************************************
002C
002C  4004  NINT  IN    DRCV,PA0 receive data from shift register.
002D
```

```
002D  7EFF        LACK  SET       set receive and xmit ended flag.
002E  5002        SACL  RXEFLG
002F
002F  7F8D        RET             return.
                *
                *********************************************************
                *     =============================================     *
                *     Secondary communication interrupt routine 1.      *
                *     =============================================     *
                *                     destroy ACC,DP                    *
                *                                                       *
                *   Write the contents of D2ND to the 'LS299s, receive  *
                *   data in DRCV, and modify XVECT for secondary        *
                *   communication interrupt.                            *
                *********************************************************
0030
0030  4004  SINT1 IN    DRCV,PA0 receive data from shift register.
0031
0031  4906        OUT   D2ND,PA1 write secondary data to shift
                *       register.
0032  200E        LAC   ASINT2,0  modify interrupt location.
0033  5007        SACL  XVECT     secondary communication 2
0034
0034  7EFF        LACK  SET       set secondary communication flag.
0035  5003        SACL  SNDFLG,0
0036
0036  7F8D        RET             return.
0037
                *********************************************************
                *     =============================================     *
                *     Secondary communication interrupt routine 2.      *
                *     =============================================     *
                *                     destroy ACC,DP                    *
                *                                                       *
                *   Modify XVECT for normal communication, and set      *
                *   RXEFLG flag.                                        *
                *********************************************************
0037
0037  200C  SINT2 LAC   ANINT     modify interrupt location
0038  5007        SACL  XVECT     normal communication.
0039
0039  7EFF        LACK  SET       set receive and xmit ended flag.
003A  SACL  RXEFLG
003B
003B  7F89        ZAC             clear secondary communication flag.
003C  5003        SACL  SNDFLG,0
003D
003D  7F8D        RET             return.
003E
```

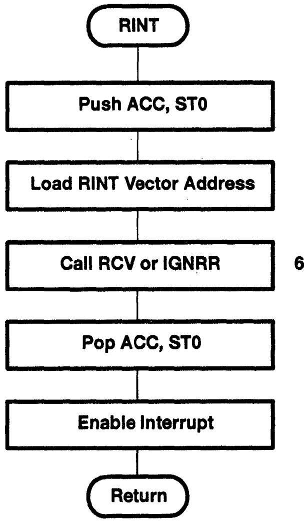
```
          ********************************************************
          *    ==========================================        *
          *    Ignoring the first interrupt after reset.         *
          *    ==========================================        *
          *                   destroy ACC,DP.                    *
          *                                                      *
          *  Ignore the first interrupt after reset. the TLC32040 *
          *  receives zero as DAC data but no ADC data in DRCV.  *
          *                                                      *
          ********************************************************
003E
003E  200C  IGINT LAC   ANINT     modify interrupt location
003F  5007        SACL  XVECT     normal communication.
0040
0040  7F8D        RET             return.
0041
                  END
NO ERRORS, NO WARNINGS
```

B TLC32040 and TMS32020 Flowcharts and Communication Program

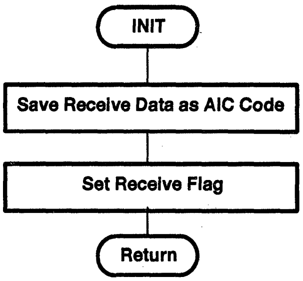
B.1 Flowcharts



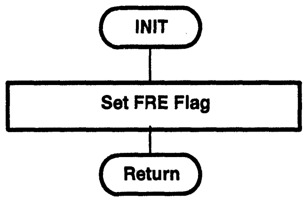
a. INITIALIZATION



b. RECEIVED INTERRUPT SERVICE ROUTINE

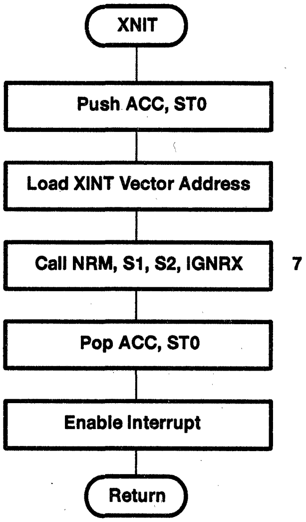


c. RECEIVE SUBROUTINE

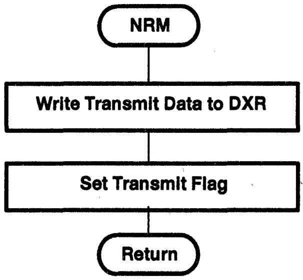


d. IGNORE INTERRUPT

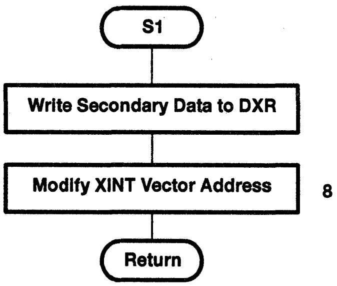
1 – Alterable AR pointer and OVM.
2 – Alterable CNF, SXM and XF.
3 – Must clear at least 108 through 127, 19 of internal RAM.
4 – If IMR is changed by user program. INST must be changed.
5 – Their contents will be changed by their routine locations.
6 – IGNRR is executed only once after reset.



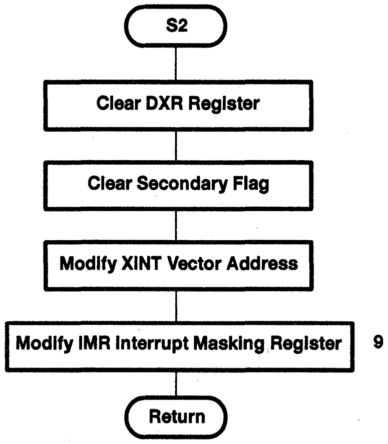
e. TRANSMIT INTERRUPT SERVICE ROUTINE



f. PRIMARY TRANSMISSION ROUTINE

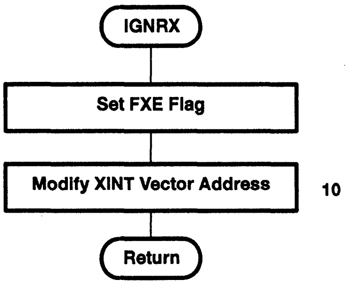


g. PRIMARY-SECONDARY COMMUNICATIONS 1

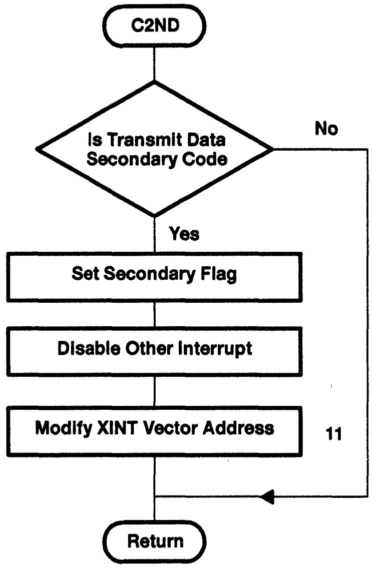


h. PRIMARY-SECONDARY COMMUNICATIONS 2

7 – IGNRX is executed only once after reset.
8 – Modify to S2 address.
9 – Modify to NRM address.

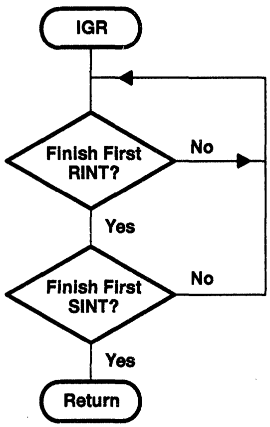


l. IGNORE TRANSMIT INTERRUPT



j. SECONDARY COMMUNICATION JUDGEMENT

10 – Modify to NRM address.
11 – Modify to S1 address.



k. IGNORE FIRST INTERRUPTS

B.2 Communication Program List

```
          ***********************************************************
          * ===========================================             *
          *  TLC32040 & TMS32020 communication program.             *
          * ===========================================             *
          *            by H.Okubo & W.Rowand                        *
          *           version 1.1    7/22/88.                       *
          *                                                         *
          * This is a TMS32020 - TLC32040 communication program     *
          * that can be used in many systems. To use this program   *
          * the TMS32020 and the TLC32040 (AIC) must be connected   *
          * as shown in the publication: Linear and Interface       *
          * Circuit Applications, Volume 3. The program reserves    *
          * TMS32020 internal data memory 108 through 127 (B2) as   *
          * flags and storage. When secondary communication is      *
          * needed, every maskable interrupt except XINT is         *
          * disabled until that communication finishes.             *
          *                                                         *
          * If you have any questions, please let us know.          *
          ***********************************************************
          *
          *
          * ======================
          * Memory mapped register.
          * ======================
          *
0000      DRR  EQU0            * data receive register address.
0001      DXR  EQU       1     * data xmit register address.
0004      IMR  EQU       4     * interrupt mask register address.
          *
          * ==============================================
          *    Reserved onchip RAM as flags and storages.
          *           (block B2 108 through 127.)
          * ==============================================
          *
006C      FXE  EQU       108   * ignore first XINT flag.
006D      FRE  EQU       109   * ignore first RINT flag.
006F      TMPO EQU       111   * temporary register.
0070      ACCHST EQU     12    * stack for ACCH.
0071      CCLST  EQU     113   * stack for ACCL.
0072      SSTST  EQU     114   * stack for STO register.
0073      INTST  EQU     115   * stack for IMR register.
0074      RVECT  EQU     116   * vector for RINT.
0075      XVECT  EQU     117   * vector for XINT.
0076      VRCV EQU       118   * RINT vector storage.
0077      VNRM EQU       119   * XINT vector storage.
0078      VS1  EQU       120   * secondary vector storage1.
0079      VS2  EQU       121   * secondary vector storage2.
007A      DRCV EQU       122   * receive data storage.
007B      DXMT EQU       123   * xmit data storage.
007C      D2ND EQU       124   * secondary data storage.
007D      FRCV EQU       125   * receive flag.
007E      FXMT EQU       126   * xmit flag.
007F      F2ND EQU       127   * secondary communication flag.
          *
```

```
                ************************************************************
                * Processor starts at this address after reset.          *
                *                                                          *
     0000             AORG     0   * program start address.                *
     0000    FF80     B     STRT   * jump to initialization routine.       *
     0001    0020
                ************************************************************
                *
                ************************************************************
                * Receive interrupt location.                              *
                *                                                          *
     001A             AORG     26  * Rint vector.                          *
     001A    FF80     B   RINT     * jump to receive interrupt             *
     00IB    004A                  * routine.                              *
                ************************************************************
                *
                ************************************************************
                * Transmit interrupt location.                             *
                *                                                          *
     ODIC             AORG     28  * Xint vector.                          *
     001C    FF80     B      XINT  * jump to xmit interrupt routine.       *
     001D    005A
                ************************************************************
                *
     0020             AORG     32  * start initial program.
                *
                ************************************************************
                * User must initialize DSP with the routine INIT.          *
                * The user may modify this routine to suit his             *
                * requirements as he likes.                                *
                ************************************************************
     0020    FE80 STRT  CALL INIT  *
     0021    0025
     0022    CE00       EINT       * enable interrupt.
     0023    FE80       CALL IGR
     0024    008D
                *
```

```
     *****************************************************************
     *                ================                               *
     *                   User area                                   *
     *                ================                               *
     *                         *
     * This program allows the user two levels of nesting,           *
     * since two levels are used as stack for the interrupt.         *
     * When the FXMT flag is false no data has occurred              *
     * When the FRCV flag is false, no data has been                 *
     * received. As those flags are not reset by any                 *
     * routine in this program, the user must reset the              *
     * flags if he chooses to use them and note that >00ff           *
     * means true, >0000 means false. User routines such as          *
     * digital filtering, FFTs etc. must be placed in this           *
     * location. Depending on the sampling rate (conver-             *
     * sion rate), these user routines must write the xmit           *
     * data to the DXMT registers within approximately 500           *
     * instruction cycles. If the user requires secondary            *
     * communication, data with the secondary code (xxx              *
     * xxxx xxxx xx11) should first be written to DXMT and           *
     * then secondary data should be written to D2ND. Next,          *
     * a call should be made to C2ND to set up SVECT and the         *
     * F2ND flag to perform the secondary communication.             *
     * Note that all maskable interrupts except XINT are             *
     * disabled until secondary communication has completed.         *
     *****************************************************************
     *
     *****************************************************************
     *            =====================                              *
     *            Initialization routine.                            *
     *            =====================                              *
     * This routine initializes the status registers, flags,         *
     * vector storage contents and internal data locations           *
     * 96 through 107. Note that the user can modify these           *
     * registers (i.e., STO ST1 IMR), as long as the contents        *
     *do not conflict with the operation of the AIC.                 *
     ************************************************************
0025 C800 INIT  LDPK  0          * set status0 register.
0026 D00I LALK  >OE00,0          * 0000 1110 0000 D000B
0027 OE00
0028 606F SACL  TMPO,0           * ARP=0 AR pointer 0
0029 506F LST   TMPO             * OV =0 (Overflow reg-clear)
     *                           * OVM=1 (Overflow mode set to 1)
     *                           * ? =1 Not affected.
     *                           * INTM=1 Not affected
     *                           * DP 000000000 page 0
     *
     *                           * set statusl register.
     *
002A D00I LALK  >03F0            * 0000 0011 1111 0000B
002B 03F0
002C 606F SACL  TMPO,0           * APB=0
002D 516F LST1  TMPO             * CNF=0 (Set B0 data memory)
002E
```

```
                *                          * TC =0
                *                          * SXM=1 (enable sign extend mode.)
                *                          * D9-D5=111111 not affected.
                *                          * F=1 (XF pin status.)
                *                          * F0=0 (16-bit data transfer mode.)
                *                          * TXM=0 (FSX input)
                *
                *
                *
002E CA00             ZAC                  * clear registers
002F 6001             SACL  DXR,0          *
0030 6000             SACL  DRR,0          *
0031 C060             LARK  AR0,96         * clear Block B2.
0032 CBIF             RPTK 31              *
0033 6OA0             SACL  +,0            *
                *
                *  Interrupt masking
                *
0034 CA30             LACK  >30            * 0000 0000 0011 0000B
0035 6004             SACL  IMR,0          * INT ________|| ||||
0036 6073             SACL  INTST,0        * RINT_________| ||||
                                           * TINT___________||||
                *                          * INT2____________|||
                *                          * INT1_____________||
                                           * INTO______________|
                *
0037 D001             LALK  NRM,0          * normal xint routine address.
0038 0067
0039 6077             SACL  VNRM,0         *

003A D001             LALK  S1,0           * secondary xint routine address 1.
003B 006C
003C 6078             SACL  VS1,0          *
                *
003D D001             LALK  S2,0           * secondary xint routine address 2.
003E 0071
003F 6079             SACL  VS2,0          *
                *
0040 D001             LALK  RCV,0          * rint routine address.
0041 0055
0042 6076             SACL  VRCV,0
                *
0043 D001             LALK  IGNRR,0        * set ignore first rint address.
0044 0094
0045 6074             SACL  RVECT,0
                *
0046 D001             LALK  IGNRX,0        * set ignore first xint address.
0047 0099
0048 6075             SACL  XVECT,0
0049 CE26             RET                  * return.
004A
```

```
               *
               **********************************************************
               *           ==========================               *
               *             Receive interrupt routine.              *
               *           ==========================               *
               * This routine stores receive data in its storage DRCV  *
               * (112 page0) and sets the receive flag FRCV (125 page0)*
               * As two levels of nesting are used, this routine       *
               * allows the user two levels, without stack extension . *
               **********************************************************
004A 7872 RINT  SST    SSTST        * push STO register.
004B C800       LDPK 0              * data pointer page 0.
004C 6071       SACL   ACCLST,0     * push ACCL.
004D 6870       SACH   ACCHST,0     * push ACCH.
004E 2074       LAC    RVECT,0      * load ACC vector address.
004F CE24       CALA
0050 4171       ZALS   ACCLST       * pop ACC
0051 4870       ADDH   ACCHST
0052 5072       LST    SSTST        * pop ST register.
0053 CE00       EINT                * enable interrupts.
0054 CE26       RET                 * return.
               *
0055 2000 RCV   LAC    DRR,0        * load data from DRR.
0056 607A       SACL   DRCV,0       * save it to its storage.
0057 CAFF       LACK   >FF          * set receive flag.
0058 607D       SACL   FRCV         *
0059 CE26       RET                 * return.
               *
               **********************************************************
               *           ==========================               *
               *              xmit interrupt routine.                *
               *           ==========================               *
               * This routine writes xmit data C%the contents of DXMT  *
               * (123 page0)) to the DXR register according to the type*
               * of communication, i.e. normal communication or secondary *
               * communication. For normal communication, call the normal *
               * communication routine (NRM). For secondary, call the  *
               * secondary communication routines (S1 and S2). Because *
               * these routines use two levels of nesting, the user is *
               * allowed two levels of nesting if stack extension is   *
               * not used.                                             *
               **********************************************************
005A 7872 XINT  SST    SSTST        * push ST register.
005B C800       LDPK   0            * data pointer page 0.
005C 6071       SACL   ACCLST,0     * push ACCL.
005D 6870       SACH   ACCHST,0     * push ACCH.
005E 207C       LAC    D2ND,0       * preload dxr with secondary
005F 6001       SACL   DXR,0        * communication data.
0060 2075       LAC    XVECT,0      * load vector address.
0061 CE24       CALA                * call xmit routine.
0062 4171       ZALS   ACCLST       * POP ACC
0063 4870       ADDH   ACCHST
0064 5072       LST    SSTST        * pop ST register.
0065 CE00       EINT                * enable interrupt.
0066 CE26       RET                 * return.
```

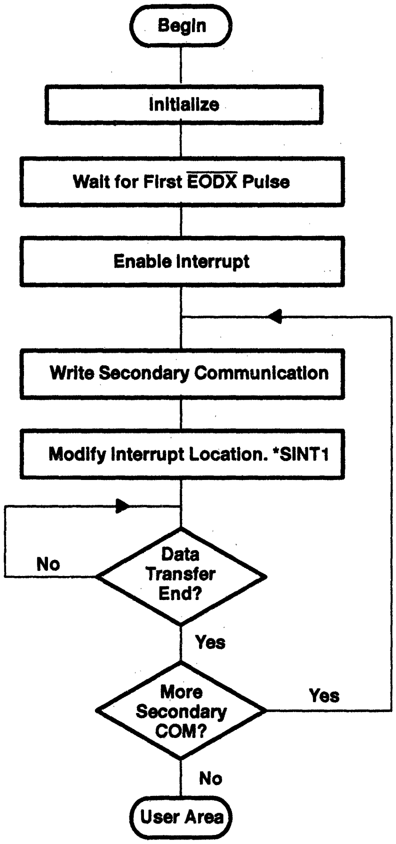
```
               ************************************************************
               *         ============================                     *
               *           Normal data write routine.                     *
               *         ============================                     *
               * This routine is called when normal communication occurs.*
               * This routine writes xmit data to DXR, and sets the       *
               * transmit flag (126 page0).                               *
               ************************************************************
               *
0067 207B NRM     LAC  DXMT,0      * write DXR data.
0068 6001         SACL DXR,0
0069 CAFF         LACK >FF         * set flag.
006A 607E         SACL FXMT
006B CE26        RET               * return.
               ************************************************************
               *         =================================                *
                          Secondary data write routine 1.                 *
               *         =================================                *
               * This routine is called when secondary communication      *
               * occurs. It writes secondary data to DXR, and modifies *
               * the content of XVECT(117 page0) for continuing secondary*
               * communication.                                           *
               ************************************************************
006C 207  S1      LAC  D2ND,0      * write DXR 2nd data.
006D 6001         SACL DXR,0
006E 2079         LAC  VS2,0       * modify for next XINT.
006F 6075         SACL XVECT,0
0070 CE26         RET              * return.
               *
               ************************************************************
               *         =================================                *
               *         Secondary data writing routine 2.                *
               *         =================================                *
               *
               * This routine is called when secondary communication      *
               * occurs. It writes dummy data to DXR to ensure that       *
               * secondary communication is not inadvertently             *
               * initiated on the next XINT. It also modifies the         *
               * content of XVECT for normal communication.               *
               ************************************************************
0071 CA00 S2      ZAC              * clear data for protection.
0072 6001         SACL DXR,0       * of double secondary communication.
0073 607F         SACL F2ND        * clear secondary flag.
0074 CAFF         LACK >FF         * set xmit end flag.
0075 607E         SACL FXMT,0
0076 2077         LAC  VNRM,0      * set normal communication vector.
0077 6075         SACL XVECT,0
0078 2073         LAC  INTST,0     * enable all interrupts.
0079 6004         SACL IMR,0
007A CE26         RET              * return.
```

```
               *
               *********************************************************
               *           ====================                        *
               *            Check secondary code.  destroy DP pointer. *
               *           ====================           ACC.         *
               *                                                       *
               * This routine checks whether the data in DXMT (123 pageo)*
               * has secondary code or not. If secondary code exists,  *
               * then disable maskable interrupts except XINT, modify the*
               * contents of XVECT(117 page0) for secondary communi-   *
               * cation, and set secondary flag. Note that we recommend*
               * calling this routine to send control words to the AIC.*
               *********************************************************
007B C800 C2ND    LDPK 0          * data page pointer 0.
007C CA03         LACK 03
007D 606F         SACL TMPO
007E 207B         LAC  DXMT,0     * is this data secondary code
007F 4E6F         AND  TMPO
0080 106F         SUB  TMPO,0
0081 F680         BZ   C2ND1      * if yes, then next.
0082 0084
0083 CE26         RET             * else return.
               *
0084 CAFF C2NDI   LACK >FF        * set secondary flag.
0085 607F         SACL F2ND,0
0086 CA20         LACK >20        * enable only XINT.
0087 6004         SACL IMR,0
0088 2078         LAC  VSI,0      * modify vector address for secondary
0089 6075         SACL XVECT,0    * communication.
00BA 207B         LAC  DXMT,0     * write primary data to DXR.
008B 6001         SACL DXR,0
00BC CE26         RET             * return.
               *
               *********************************************************
               *                                                       *
               *           ====================                        *
               *           Check first interrupt                       *
               *           ====================                        *
               *                                                       *
               * This routine checks if both first interrupts have     *
               * occurred. If this routine is called after reset, it   *
               * waits for both interrupts then returns.               *
               *********************************************************
008D 206D IGR     LAC  FRE,0      * check first interrupt after
008E F680         BZ   IGR        * master reset.
008F 008D
0090 206C         LAC  FXE,0
0091 F680         BZ   IGR
0092 008D
0093 CE26         RET
0094
```

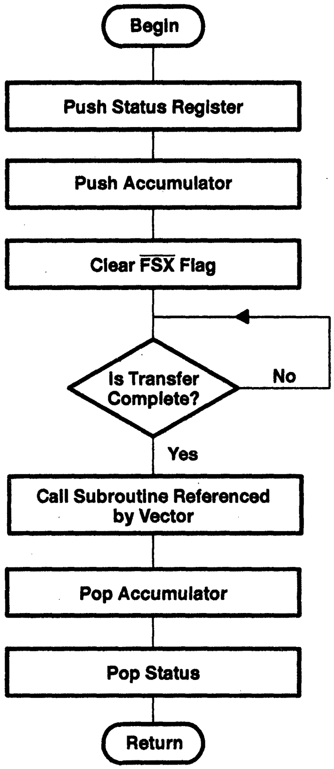
```
               *
               ***********************************************************
               *           ==========================                   *
               *             Ignore interrupt routine.                   *
               *           ==========================                   *
               * These routines are used so that the first RINT and     *
               * XINT after the %DSP reset can be ignored. They set     *
               * flags and modify each vector address to the normal     *
               * interrupt address but do not read or write to the      *
               * serial ports. Note that the first data that the AIC will*
               * receive after the DSP reset is >0000.                  *
               ***********************************************************
0094 CAFF IGNRR   LACK >FF
0095 606D         SACL FRE,0
0096 2076         LAC  VRCV,0      * set normal receive address.
0097 6074         SACL RVECT,0     *
0098 CE26         RET              * return.
               *
0099 CAFF IGNRX   LACK >FF
009A 606C         SACL FXE,0
009B 2077         LAC  VNRM,0      * set normal xmit address.
009C 6075         SACL XVECT,0     *
009D CE26         RET              * return.
               *
                  END
NO ERRORS, NO WARNINGS
```

C TLC32040 and TMS320C17 Flowcharts and Communication Program

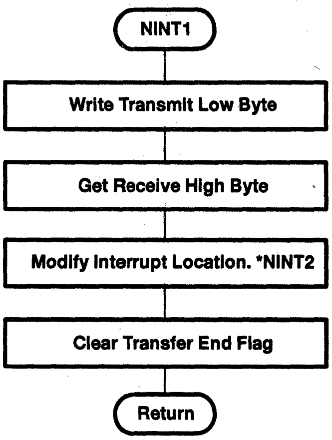
C.1 Flowcharts



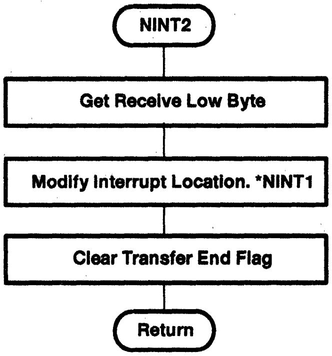
a. MAIN



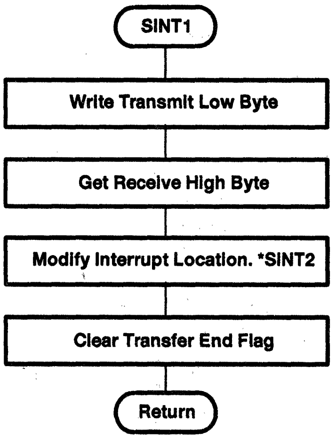
b. INTERRUPT SERVICE ROUTINE



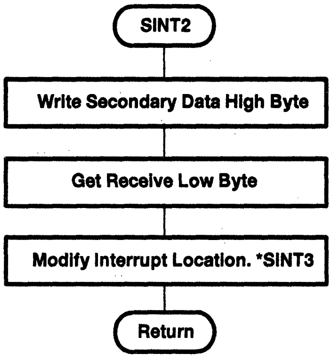
c. PRIMARY COMMUNICATION 1



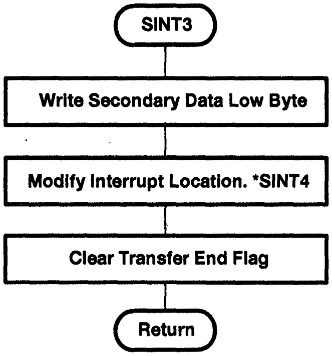
d. PRIMARY COMMUNICATION 2



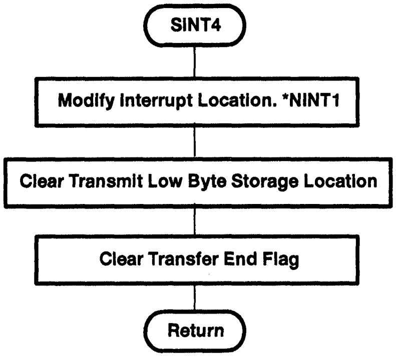
e. PRIMARY-SECONDARY COMMUNICATION 1



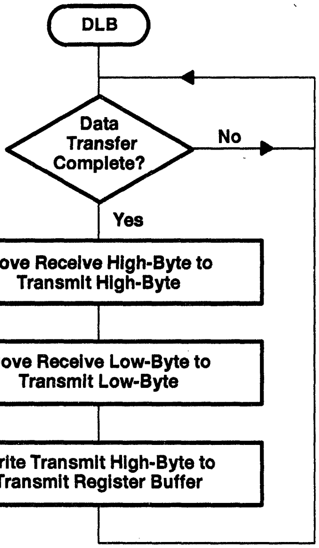
f. PRIMARY-SECONDARY COMMUNICATION 2



g. PRIMARY-SECONDARY COMMUNICATION 3



h. PRIMARY-SECONDARY COMMUNICATION 4



i. DIGITAL LOOPBACK

C.2 Communication Program List

```
          ***********************************************************
          *                                                         *
          *=========================================================*
          *      TLC32040 to TMS320C17 Communication Program        *
          *                    version 1.2                          *
          *                   revised 7/22/88                       *
          *                                                         *
          *         by Hironori Okubo and Woody Rowand              *
          *                 Texas Instruments                       *
          *                   (214) 997-3460                        *
          *=========================================================*
          *                                                         *
          * This program uses the circuit published in the Volume *
          * 3 of the Linear and Interface Circuit Applications    *
          * book with the following modification:                  *
          *      *                                                  *
          *   1. INT- of the TMS320C17 must be connected to        *
          *      EODX- of the TLC32040.                             *
          *                                                         *
          *                                                         *
          * In this configuration, the program will allow the      *
          * TLC32040 to communicate with the TLC320C17 with the    *
          * restriction that all interrupts except INT- are        *
          * prohibited and only synchronous communication can      *
          * occur. The program allows the user two levels of       *
          * nesting in the main program; the remaining two levels *
          * are reserved for the interrupt vector and subroutines.*
          *                                                         *
          * If desired, this program may be used with the TMS32011*
          * digital signal processor with the following change.   *
          * Since the TMS32011 has only sixteen words of data RAM *
          * on data page 1, all of the registers used by this     *
          * program should be moved to data page 0, except for    *
          * SSTSTK (the temporary storage location for the status *
          * register) which must remain on page %I (since the     *
          * SST instruction always addresses page 1).             *
          *                                                         *
          ***********************************************************
     0000 SSTSTK  EQU  >00   stack for status (SST) register.
     0001 ACHSTK  EQU  >01   stack for accumulator high (ACCH).
     0002 ACLSTK  EQU  >02   stack for accumulator low (ACCL).
     0003 RXEFLG  EQU  >03   xmit/receive in progress.
     0004 DRCV1   EQU  >04   storage for high byte receive data.
     0005 DRCV2   EQU  >05   storage for low byte receive data.
     0006 DXMT1   EQU  >06   storage for high byte xmit data.
     0007 DXMT2   EQU  >07   storage for low byte xmit data.
     0008 DXMT3   EQU  >08   storage for high byte secndry data.
     0009 DXMT4   EQU  >09   storage for low byte secndry data.
     D00A VECT    EQU  >OA   storage for interrupt vector addr.
     000B ANINT1  EQU  >OB   storage for normal xmit/rcv vect 1.
     000C ANINT2  EQU  >OC   storage for normal xmit/rcv vect 2.
     000D ASINTI  EQU  >OD   storage for secndry xmit/rcv vect 1.
     000E ASINT2  EQU  >OE   storage for secndry xmit/rcv vect 2.
     000F ASINT3  EQU  >OF   storage for secndry xmit/rcv vect 3.
```

```
0000
     0010   ASINT4  EQU   >10   storage for secndry xmit/rcv vect 4.
     0011   CNTREG  EQU   >11   storage for control register.
     0012   MXINT   EQU   >12   storage for xmit interrupt mask.
     0013   CLRX    EQU   >13   storage for xmit interrupt clear
     0014   CLRX1   EQU   >14   storage for xmit intrpt clear/mask.
     0015   TEMP    EQU   >15   temporary register.
     00FF   FLAG    EQU   >FF   flag set.
                    *    =========================
                    *        Branch to initialization routine.
                    *   =========================
0000                    AORG       >0000
0000 F900               B   INIT  branch to initialization routine.
0001 0013
  00020069          ***************************************************************
                    *  =======================                                  *
                    *   Interrupt service routine.                              *
                    *  =======================                                  *
                    *                                                           *
                    *   To initiate secondary communication, change the         *
                    *   contents of VECT to the address of the secondary        *
                    *   communication subroutine and store the                  *
                    *   in DXMT3 and DXMT4.                                     *
                    *                                                           *
                    *                                                           *
                    * e.g.                          *
                    *   LAC ASINTI      modify VECT.                            *
                    *   SACL      VECT                                          *
                    *      |                                                    *
                    *   LAC H1          store high-byte of                      *
                    *   SACL      DXMT3       secondary information in          *
                    *   LAC H2          DXMT4 store low-byte in DXMT4.          *
                    *   SACL      DXMT4                                         *
                    *                                                           *
                    ***********************************************************
0002                        AORG  >02
0002 6EOI           INTSVC  LDPK  1
0003 7C00                   SST   SSTSTK      push status register.
0004 5801                   SACH  ACHSTK      push accumulator high.
0005 5002                   SACL  ACLSTK      push accumulator low.
0006 4813                   OUT   CLRXPAO     make sure FSX-flag is clear.
0007 4011           WAIT1   IN    CNTREG,PAO  read control register.
0008 2011                   LAC   CNTREG,0    load accumulator with control
0009 7912                   AND   MXINT       reg mask-off xmit interrupt
000A FF00                   BZ    WAIT1       flag loop until xmit interrupt
000B 0007                                     flag is recognized.
000C
                    *
000C 200A                   LAC   VECT        load acc with interrupt vector.
000D 7F8C                   CALA              call appropriate xmit/rcv
                                              routines
000E 6501                   ZALH  ACHSTK      pop accumulator high.
000F 7A02                   OR    ACLSTK      pop accumulator low.
0010 7B00                   LST   SSTSTK      pop status register.
0011 7F82                   EINT              enable interrupts.
0012 7F8D                   RET               return to main program.
```

```
0013
          ***********************************************************
          *    ==============================                       *
          *      Initialization after reset.                        *
          *    ==============================                       *
          *                                                         *
          *    Data RAM locations >80 through >92 are reserved      *
          *    by this program. The user must set the status        *
          *    register at the end of this program with the SST     *
          *    command or a combination of SOVM, LDPK etc.          *
          *                                                         *
          ***********************************************************
0013 7F81 INIT DINT                     disable interrupts.
0014 6E01      LDPK    1                set data page pointer one.
0015 7F89      ZAC                      clear registers.
0016 6880      LARP    0
0017 7083      LARK    0,RXEFLG+>80
0018 50A8      SACL    *+
0019 50A8      SACL    *+
001A 50A8      SACL    *+
001B 50A8      SACL    *+
001C 50A8      SACL    *+
001D 50A8      SACL    *+
001E 50A8      SACL    *+
001F 5088      SACL    *
0020 4906      OUT     DXMT1,PA1        clear transmit registers.
0021 4906      OUT     DXMT1,PAI
0022 7E04      LACK    ?00000100
0023 5012      SACL    MXINT            initialize xmit-int mask.prepare
0024 7E01      LACK    1                for serial port initialization
0025 5015      SACL    TEMP             and initialization of registers
0026 6A15      LT      TEMP             containing 16-bit constants.
0027 80A1      MPYK    CLX1             initialize interrupt flag clear.
0028 7F8E      PAC
0029 6713      TBLR    CLRX
002A 80A2      MPYK    CLX2             initialize interrupt flag clear
002B 7F8E      PAC                      with interrupts disabled.
00IC 6714      TBLR    CLRX1
002D 809D      MPYK    IGN
002E 7F8E      PAC
002F 500A      SACL    VECT             initialize interrupt vector.
0030 8077      MPYK    NINT1            save normal communication
0031 7F8E      PAC                      address to its storage.
0032 500B      SACL    ANINT1
0033 807D      MPYK    NINT2            save normal communication
0034 7F8E      PAC                      address 2 to its storage.
0035 500C      SACL    ANINT2
0036 8084      MPYK    SINTI            save secondary communication
0037 7F8E      PAC                      address 1 to its storage.
0038 500D      SACL    ASINT1
0039 808A      MPYK    SINT2            save secondary communication
003A 7F8E      PAC                      address 2 to its storage.
003B 500E      SACL    ASINT2
003C 8090      MPYK    SINT3            save secondary communication
003D 7FBE      PAC                      address 3 to its storage.
003E 600F      SACL    ASINT3
003F A095      MPYK    SINT4            save secondary communication
```

```
0040 CE14      PAC       address 4 to its storage.
0041 6010      SACL     ASINT4
0042
          ***********************************************************
          *   ==========================================          *
          *    Synchronize high/low byte transmission.            *
          *   ==========================================          *
          *                                                       *
          * The time between FSX- interrupts is approximately     *
          * ten microseconds (50 cycles). Wait for first if       *
          * FSX-, this is the first interrupt, delay 60 cycles    *
          * (past the second interrupt). If it is the second      *
          * interrupt, no harm done.                              *
          *                                                       *
          ***********************************************************
0042 E014         OUT   CLRX1,PAO  clear interrupt flags,disableint.
0043 8011 IGNOR   IN    CNTREG,PAO read control register.
0044 2011         LAC   CNTREG     wait
0045 4E12         AND   MXINT         for
0046 F680         BZ    IGNOR            FSX- flag.
0047 0043
0048
0048 C014         LARK  0,20       wait 60 cycles (20 × 3 cycles) in
0049 5500 IGNOR1  NOP              case FSX- int. is first of the
                                   pair.
004A FB90         BANZ  IGNOR1     if FSXI- int was the second, delay
004B 0049
004C
004C E013         OUT CLRX,PAO     anyway.
004D
004D CEDO         EINT             enable interrupt.
          ***********************************************************
          *    ===============================                    *
          *        Main program (user area)                       *
          *    ===============================                    *
          *                                                       *
          * This program allows the user two levels of nesting,   *
          * since one level is used as stack for the interrupt and *
          * the interrupt service routine makes one subroutine    *
          * call. User routines such as digital filtering, FFTS,  *
          * and secondary communication judgement may be placed   *
          * here. The number of instruction cycles between        *
          * interrupts varies with the sampling rate. In the      *
          * power-up condition this is approximately 500 cycles.  *
          *                                                       *
          * In the example below, the first two transmissions send *
          * secondary information to the AIC. The first configures *
          * the TB and RB registers. The second configures the    *
          * control register.                                     *
          *                                                       *
          ***********************************************************
004E CA00 MAIN    ZAC              prepare first control word.
004F 6006         SACL  DXMTI
0050 CA03         LACK  >03
0051 5007      SACL     DXMT2                  should be xxxx xx11.
0052 7E24      LACK     >24
```

```
0053  5008      SACL  DXMT3
0054  7E92      LACK  >92
0055  5009      SACL  DXMT4
0056  200D      LAC   ASINT1      set VECT for secondary
0057
0057  500A      SACL  VECT     communications.
0058  4906      OUT   DXMTI,PAI   store first transmit byte in
          *                 transmit buffer.
0059  7F89      ZAC
005A  5003      SACL  RXEFLG      clear xmit/rcv end flag.
005B  2003  MAIN1 LAC   RXEFLG
005C  FF00  BZ        MAINI    wait for data transfer to
005D  005B                        complete.
005E
005E  7F89      ZAC            prepare second control word.
005F  5006      SACL  DXMT1
0060  7EO3      LACK  >03
0061  5007      SACL  DXMT2
0062  7E00      LACK  >00
0063  5008      SACL  DXMT3
0064  7E67      LACK  >67
0065  5009      SACL  DXMT4
0066  200D      LAC   ASINTI
0067  500A      SACL  VECT
0068  4906      OUT   DXMTI,PAL
0069  7F89      ZAC
006A  5003      SACL  RXEFLG      clear xmit/rcv end flag.
          *********************************************************
          *  ========================  *
          *     Digital loop-back program  *
          *  ========================  *
          *              *
          *  This program serves as an example of what can   *
          *  be done in the user area.  *
          *              *
          **********************************************************
006B  2003  DLB   LAC   RXEFLG   wait for data transfer to complete.
006C  FF00      BZ    DLB
006D  006B
006E
006E  2004      LAC   DRCV1    move receive data to transmit
006F  5006      SACL  DXMT1    registers.
0070  2005      LAC   DRCV2
0071  5007      SACL  DXMT2
0072  4906      OUT   DXMTI,PAL   write first transmit byte to
          *                 transmit buffer.
0073  7F89      ZAC
0074  5003      SACL  RXEFLG      clear rcv/xmit-end flag.
0075  F900      B     DLB
0076  006B
0077
```

```
                *************************************************************
                      ===================================                   *
                *       Normal interrupt routines.                          *
                *     ===================================                   *
                *                                                           *
                *     These routines destroy the contents of the            *
                *     accumulator and the data page pointer, making it      *
                *     necessary to save these before the routines begin     *
                *                                                           *
                *     Write the contents of DXMT2 to the transmit buffer    *
                *     and read the receive buffer into DRCV1.               *
                *                                                           *
                *************************************************************
0077
0077 4907 NINT1 OUT     DXMT2,PAI     write xmit-low to xmit register.
0078 4104       IN      DRCVI,PAI     read rcv-data-high from rcv reg.
0079 200C       LAC     ANINT2        prepare next interrupt vector.
007A 500A SACL  VECT
007B 4813 OUT   CLRX,PAO                  clear xmit interrupt flag.
007C 7F8D RET
007D 4105 NINT2 IN      DRCV2,PAI     read receive-data-low from rcv
                                      reg.
007E 200B LAC   ANINTI                prepare next interrupt vector.
007F 500A SACL  VECT
0080 4813 OUT   CLRX, PAO             clear xmit interrupt flag.
0081 7EFF LACK  FLAG
0082 5003 SACL  RXEFLG                set xmi%t/rcv end flag.
0083 7F8D RET
                *************************************************************
                *     ===================================                   *
                *       Secondary interrupt routines                        *
                *     ===================================                   *
                *       These routines destroy the contents of the          *
                *       accumulator and the data page pointer.
                *                                                           *
                *       The following routines write the low byte of        *
                *       the primary data word and the high and low byte     *
                *       of the secondary data word. They also read the      *
                *       A/D information in the receive registers.           *
                *************************************************************
0084 4907 SINT1 OUT     DXMT2,PA1     write xmit-data-low to xmit reg.
0085 4104       IN      DRCVI,PA1     read receive-data-high from rcv
                                      reg
0086 200E       LAC     ASINT2        prepare next interrupt vector.
0087 500A       SACL    VECT
0088 4813       OUT     CLRX,PAO      clear xmit interrupt flag.
0089 7F8D       RET
008A 4908 SINT2 OUT     DXMT3,PAI     write secondary-data-high to
                                      xmit.
008B 4105       IN      DRCV2,PA1     read receive-data-low from rcv.
008C 200F       LAC     ASINT3        prepare next interrupt vector.
008D 500A       SACL    VECT
008E 4813       OUT     CLRX,PAO          clear xmit interrupt flag.
008F 7F8D       RET
0090 4909 SINT3 OUT     DXMT4,PAI     write secondary-data-low to xmit
0091 2010       LAC     ASINT4        prepare next interrupt vector.
```

```
0092 500A SACL  VECT
0093 4813       OUT     CLRX,PAO      clear xmit interrupt flag.
0094 7F8D       RET
0095 200B SINT4 LAC     ANINT1        prepare next interrupt vector.
0096 500A       SACL    VECT
0097 4813       OUT     CLRX,PAO          clear xmit interrupt flag.
0098 7F89       ZAC
0099 5007       SACL    DXMT2         clear DXMT2 immediately to
eliminate
009A 7EFF       LACK    FLAG          unnexpected secondary
communications
009B 5003       SACL    RXEFLG        set xmit/rcv end flag.
009C 7FBD       RET
          ***********************************************************
          * ==================================                      *
          * Ignore first interrupt.                                 *
          * ==================================                      *
          *    This routine is used to ignore the first data        *
          *    transmission and also to synchronize the AIC         *
          *    with the processor.
          ***********************************************************
009D 200B IGN   LAC     ANINT1
009E 500A       SACL    VECT
009F 4813       OUT     CLRX,0
00A0 7F8D       RET
          ***********************************************************
          *                                                         *
          *    CONTROL REGISTER INFORMATION                         *
          *                                                         *
          *    SERIAL-PORT CONFIG.   INT. MASK INT. FLAG            *
          *    | 1 0 0 0 1 1 1 0 |   | 0 0 0 1 0 1 0 0 |            *
          *     15 14 13 12 11 10 9  8 7 6 5 4 3 2 1 0              *
          *                   |              | | | |___INT          *
          *                   |_XF status    | | |_____ FSR         *
          *                                  |__________FSX         *
          *                                  |__________FR          *
          *                                                         *
          *                            (write 1's to clear)         *
          ***********************************************************
00A1 8E1F CLXI  DATA    >8EIF
00A2 8EOF CLX2  DATA    >8EOF
                END
NO ERRORS, NO WARNINGS
```

```
009D 200B IGN   LAC      ANINT1
009E 500A       SACL     VECT
009F 4813       OUT      CLRX,0
00A0 7F8D       RET
               ***********************************************************
               *                                                         *
               *    CONTROL REGISTER INFORMATION                         *
               *                                                         *
               *    SERIAL-PORT CONFIG.   INT. MASK INT. FLAG            *
               *    | 1 0 0 0 1 1 1 0 |   | 0 0 0 1 0 1 0 0 |            *
               *     15 14 13 12 11 10 9  8  7  6  5  4  3  2  1  0      *
               *                   |              | | | |___INT          *
               *                   |_XF status    | | |_____ FSR         *
               *                                  |___________FSX        *
               *                                  |___________FR         *
               *                                                         *
               *                             (write 1's to clear)        *
               ***********************************************************
00A1 8E1F CLX1  DATA     >8E1F
00A2 8E0F CLX2  DATA     >8E0F
                END
NO ERRORS, NO WARNINGS
```

Designing with the TLC320AC01 Analog Interface for DSPs

TEXAS INSTRUMENTS

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List of Illustrations

1 INTRODUCTION

This application report was prepared by John Walliker and Julian Daley of University College London. It is based on their experience of using the device as part of a specialized signal processing hearing aid. However the techniques described, for both the analog and digital interfaces, are appropriate for a wide variety of applications.

Measurements of performance quoted in this application note are those achieved with the particular samples and test set-up. For the full device specification see the TLC320AC01 data manual, reference SLAS057A.

Some features of the TLC320AC01 were not used in this design and therefore have not been covered here. They are phase adjustment and the use of multiple devices.

1.1 Overview of Device

The TLC320AC01 is a 14-bit resolution, audio frequency (approximately 12-kHz bandwidth) analog interface for DSP with integral anti-aliasing and reconstruction filters. It has a synchronous, serial, digital interface designed for ease of connection to many DSP chips.

The internal circuit configuration and the performance parameters, such as input source, sampling rate, filter bandwidths and gain, are determined by writing in control information to eight data registers. These registers are used to set-up the device for a given mode of operation and given application. The ADC channel and the DAC channel operate synchronously and data is transferred in 2's complement format.

The anti-aliasing filter is a switched-capacitor low-pass filter with a sixth-order elliptic characteristic. The high-pass is a single-pole filter, which can be switched out if required. There is a 3-pole continuous-time filter that precedes the switched-capacitor filter to eliminate aliasing caused by sampling in the switched-capacitor filter.

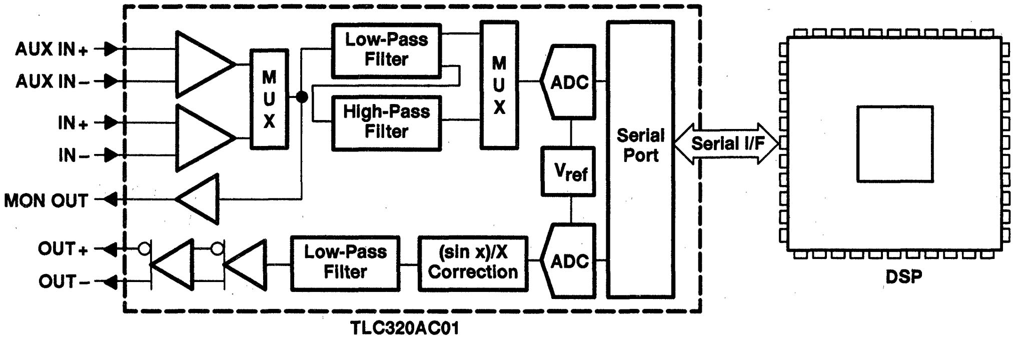
The output-reconstruction filter is also a switched-capacitor low-pass filter with a sixth-order elliptic characteristic and it is followed by a second-order (sin x)/x correction filter. This is followed by a three-pole continuous-time filter to eliminate images caused by sampling in the switched-capacitor filter.

There are three basic modes of operation available:

- Stand-alone analog-interface mode, where the TLC320AC01 generates the shift clock and the frame sync for the data transfers and is the only AIC used.
- Master-slave mode, where the master TLC320AC01 generates the shift clock and the frame sync and the rest are slaves to these signals.
- Linear-codec mode, where the shift clock and the frame sync are generated externally and the timing can be any of the standard codec timing patterns.

The TLC320AC01 is available in a standard 28-pin plastic J-lead chip carrier (FN suffix) and a 64-pin plastic-quad-flat-pack (PM suffix) which is only 1,5 mm thick, making it suitable for use in portable systems.

The device has a maximum power dissipation of 110 mW in the active mode and 10 mW in the power down mode. It runs from a single 5-V supply, both for digital and analog circuitry. This is particularly useful for portable equipment, but does require extra care in the design of the analog input and output stages.



- 14-bit A/D converter
- 14-bit D/A converter
- Antialiasing filter
- Anti-imaging filter
- (sin x)/x correction
- Input and output amplifiers
- Programmable bandwidth, sampling rate, gain, I/P source
- Single 5 V supply
- 70 dB typical signal to noise+distortion ratio
- 100 mW typical power consumption
- Analog bandwidth up to 10.8 kHz

Figure 1. TLC320AC01 Analog Interface for DSP

2 ANALOG INPUT

2.1 Signal-to-Noise and Signal-to-Distortion Measurements

With the internal gain of the TLC320AC01 set to 0 dB, a full scale signal corresponds to 6 V peak-peak at the analog input (equivalent to $6/(2\sqrt{2}) = 2.12$ V RMS).

The input signal-to-noise ratio of the TLC320AC01 can be expressed in terms of the number of least significant bits (LSB) of noise present in the digital signal, when both its inputs are connected to V_{MID}. The RMS value of the noise was measured on the test boards at 0.5 LSB. This corresponds to a noise voltage of approximately 180 µV RMS at the input (i.e., a signal-to-noise ratio of 81 dB). The intermodulation measurements are shown in Figure 2. The stimulus was the sum of a 1 kHz signal at –6 dB referred to full scale plus a 1.2 kHz signal at –12 dB referred to full scale. Distortion products are approximately 80 dB down throughout the pass band. The low frequency peaks that can be seen are multiples of 50 Hz interference.

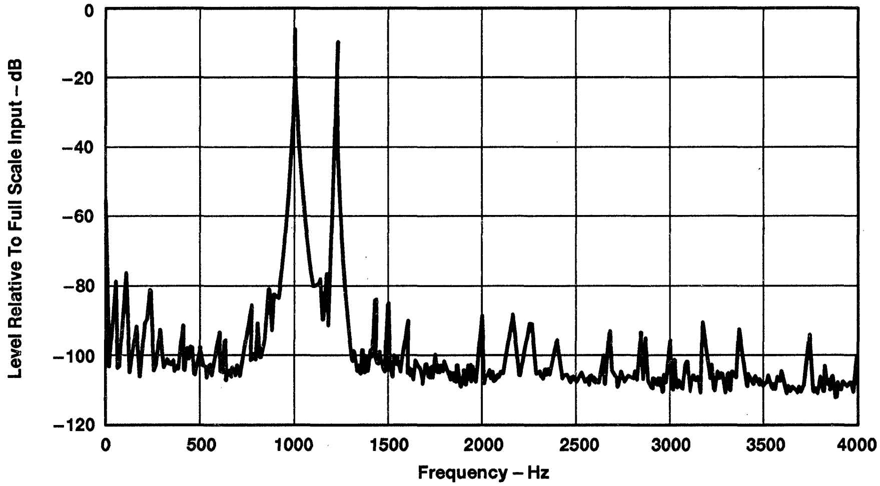


Figure 2. ADC Noise and Distortion Measurement

In the test circuit, the dc accuracy on the samples measured was 14 LSB, equivalent to 5 mV of dc offset.

2.2 Input Preamp Design

2.2.1 Noise Considerations

In order that the input preamp does not significantly affect the noise performance of the system, it should produce a noise level at least 6 dB below the TLC320AC01, (i.e., less than 90 µV RMS) at the TLC320AC01 input.

Consider the case of a microphone producing 20 mV peak-to-peak at the maximum sound level, a preamp is needed with a gain of 6 V.20 mV = 300 to get a full scale input at the ADC. So the input noise produced by the preamp must be less than 90 µV/300 = 300 nV RMS.

For a preamp with a bandwidth of 10 kHz the input noise voltage should be less than

$$\frac{300 \text{ nV}}{\sqrt{10 \text{ kHz}}} = 3 \text{ nV}/\sqrt{\text{Hz}}$$

This noise is made up of the operational amplifier's noise voltage combined with the thermal noise of the equivalent series resistance of the input source. Resistor values need to be carefully chosen, since a 10 kΩ resistor produces thermal noise of 14 nV/$\sqrt{\text{Hz}}$ at room temperature. (spectral noise voltage density for a resistor is given by $\sqrt{4KTR}$, where K is Boltzman's constant, T is the absolute temperature and R the resistance). In this case, a 100-Ω resistor was chosen (producing a thermal noise of 1.4 nV/√Hz at room temperature). A MAX410 operational amplifier was chosen for the first gain stage as this has a noise voltage of 2.4 nV/√Hz. Noise voltages combine as the root of the sum of the squares, so the total noise is given by:

$$\sqrt{\left(2.4\ \mathrm{nV}^2 + 1.4\ \mathrm{nV}^2\right)} = 2.8\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$$

The gain is split between two operational amplifiers. The first, low noise, operational amplifier configured as a noninverting amplifier with a gain of 100, followed by a second noninverting stage with a gain of three. This second operational amplifier does not need such a low noise voltage specification since its input noise is only being amplified by three. The TLC2272 dual operational amplifier, which has a noise voltage of 9 nV/√Hz, is chosen for its low power consumption, low input offset and well behaved performance under overload. (These operational amplifiers do not exhibit the behavior of BiFETs which can produce phase reversal of the output when the inputs go out of negative common mode range).

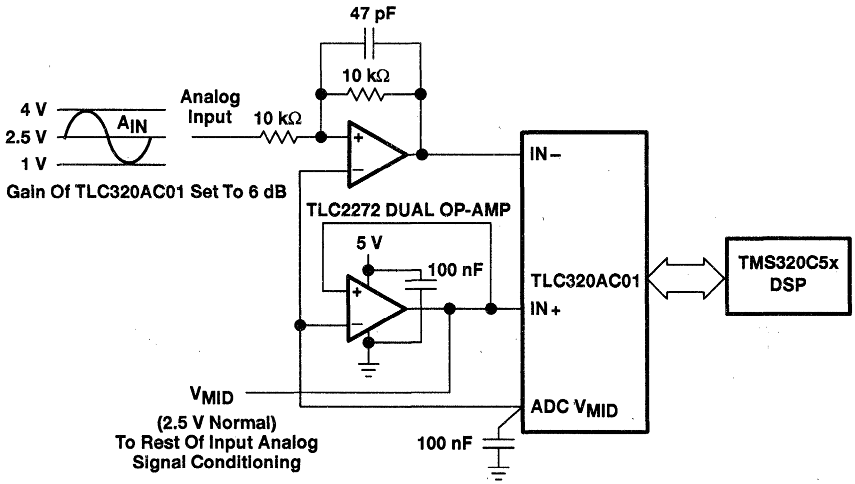


Figure 3. V_{MID} Referenced Input Circuit

2.2.2 V_{MID} Referenced Input Circuit Configuration

The configuration of the input circuitry requires extra care since all internal signals are referenced to V_{MID} rather than ground, to allow single supply operation. The PSRR at the internally generated V_{MID} point is low, so it is important that both the differential inputs are referenced to V_{MID} with any noise on V_{MID} appearing equally on both inputs. There are two ways of fulfilling this criterion. The first is to reference the whole input circuit to V_{MID} (using this as a virtual ground) as shown in Figure 3.

This configuration has the advantage of simplicity although there are some drawbacks. The buffered V_{MID} point has to be capable of driving the virtual ground and since many operational amplifiers are unhappy driving large capacitive loads this problem must not be overlooked. The TLC2272 is a good choice for this application. The input needs to be referenced to V_{MID}, which may cause a problem if interfacing to an externally powered, ground referenced signal. In this case the input needs to be ac coupled.

2.2.3 0-V Referenced Input Circuit Configuration

The second method is to level shift the signal just before the ADC inputs as shown in Figure 4. In this circuit, the preamp input is referenced to 0 V. This circuit allows a full range input swing (V_{MID} ± 1.5 V on each input) for an input signal of ±1.5 V. Any noise on V_{MID} appears equally on both differential inputs and is therefore cancelled. The common mode range of the inputs does not exceed the supply rails, so V_{MID} noise must not take the input signal outside the supply rails. The eight resistors can conveniently be in one thin film resistor package, giving good matching of resistor values and hence good power supply rejection ratio (PSRR) and dc accuracy. Amplifier A1 must have ±5 V or greater power rails but A2 to A4 only need a single 5-V rail.

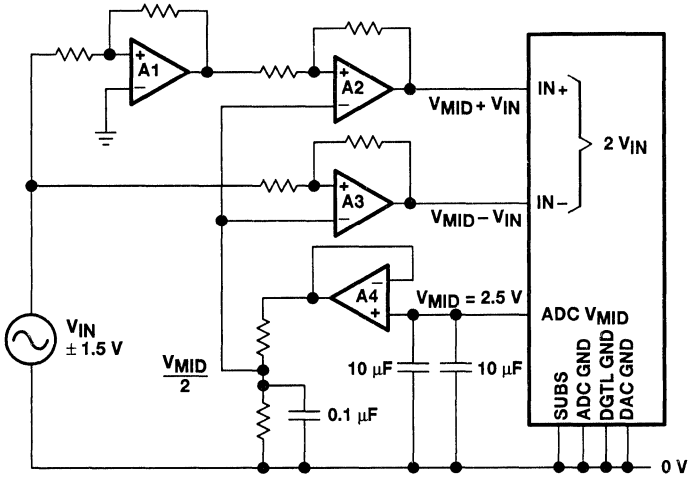


Figure 4. 0-V Referenced Input Circuit

2.2.4 Gain Control

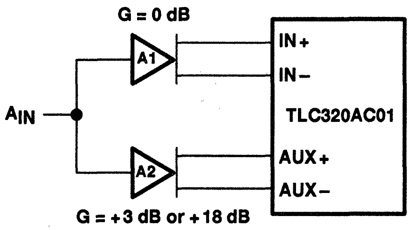
The internal preamp of the TLC320AC01 has software selectable internal gain of 0 dB, 6 dB or 12 dB plus a squelch mode (–60 dB). With 0 dB gain, plus or minus full scale result is given for a differential input of ±3 V. With a single ended input configuration (one input tied to V_{MID}), this would not allow plus or minus full scale before the operational amplifiers run out of headroom, so the gain must be set to 6 dB or 12 dB which would give plus or minus full scale with ±1.5 V and ±0.75 V, respectively, at the TLC320AC01 input.

Most of the input noise is associated with the converter itself, rather than the input amplifiers or multiplexers. Therefore, the signal-to-noise ratio is hardly affected by the chosen input gain. However, it is easier to ensure good rejection of power supply noise coupled through V_{MID} at low gains.

The TLC320AC01 has two sets of differential inputs, IN and AUX IN which can be individually selected (or both selected simultaneously for mixing).

If more gain settings are required, a combination of software switching of input source and input gain coupled with an extra hardware gain stage (see Figure 5) allows six software selectable gain steps as shown in the following table.

EXTERNAL GAIN 3 dB			EXTERNAL GAIN 18 dB		
NORM/AUX INPUT	INTERNAL GAIN (dB)	TOTAL GAIN (dB)	NORM/AUX INPUT	INTERNAL GAIN (dB)	TOTAL GAIN (dB)
NORM	0	0	NORM	0	0
AUX	0	3	NORM	6	6
NORM	6	6	NORM	12	12
AUX	6	9	AUX	0	18
NORM	12	12	AUX	6	24
AUX	12	15	AUX	12	30



Internal Gain Settings 0 dB, 6 dB, 12 dB

Figure 5. Input Circuit for 6 S/W Selectable Gain Settings

2.3 Layout and Grounding

Although earthing and PCB layout do not seem to be too critical for this device, it is good practice to ensure that the ground current from sensitive devices such as the ADC does not flow in the same copper as currents from other devices. This means having a central ground point near the device or using power planes with splits where necessary to isolate return current from other devices.

The substrate (SUBS) should be connected to ADC ground. Failure to do so can result in noisy and unstable operation. The circuit should be well decoupled for low and high frequencies to minimize noise injection from the supplies.

2.4 Power Supply

With a master clock frequency of 10 MHz, the TLC320AC01 samples typically drew 10 mA at 5 V with default register values. The supply current depends principally on the filter clock frequency. If a negative supply is needed for operational amplifiers, etc., it may be convenient to generate it using a negative voltage converter. Since the negative supply generally draws little current this is a feasible solution and avoids the need for a second battery in portable systems. The ICL7660 needs no external inductors and is available in an 8-pin small outline package. As the internal oscillator of the ICL7660 free runs at about 10 kHz, noise generated from this oscillator can find its way into the ADC input, often beating with the sampling clock creating a whirring type noise. It is however possible to lock this oscillator to the ADC clock by linking the conversion complete signal to the oscillator input on the ICL7660. Coupling via a 100-pF capacitor allows the converter to free-run if the ADC is not operative (e.g., during start-up). Any noise that now gets coupled into the ADC will be the same for each sample, creating a dc result that is much easier to deal with. Alternatively the TLE2682 provides a negative rail generator supplying up to 100 mA (which can be phase locked) plus a dual operational amplifier in one 16-pin wide body SO package).

2.5 Sampling Rate and Filters

Within limits, the sampling rate of the device (both ADC and DAC are inherently synchronous) can be set under software control. If the DAC is not used then the ADC can run at up to 43.2k samples/sec. However, if the DAC is to be used the sampling rate must be limited to 25k samples/sec.

The anti-aliasing filters (switched capacitor type) track the sampling rate by setting the corner frequency of the filter to some fraction of the sampling rate. This allows for the possibility of sub-Nyquist sampling, which should be avoided in most cases. The ratio of sampling rate to anti-aliasing filter corner frequency is set by the B register value (REG_B). The anti-aliasing corner frequency is set by the A register value (REG_A) within the TLC320AC01.

Conversion rate is given by:

$$f_{sample} = \frac{f_{MCLK}}{\left(2 \times Reg_A \times Reg_B\right)}$$

The anti-aliasing corner frequency is given by:

$$f_{lp} = \frac{f_{MCLK}}{80 \times Reg_A}$$

$$\frac{f_{sample}}{f_{lp}} = \frac{40}{Reg_B}$$

To satisfy Nyquist's sampling theorem:

$$\frac{f_{sample}}{f_{lp}} \geq 2$$

$$\therefore Reg_B \leq 20$$

The default of 18 for the B register gives $f_{sample}/f_{lp} = 2.2$. This ensures that energy above the Nyquist frequency is well into the filter's stop band.

The product of the A and B registers must be greater than 65 to allow for 17 serial clock cycles between conversions (16 data bits plus one extra cycle for frame sync in master or standalone mode). The B register must not be less than 10, since the ADC conversion takes 10 B register counts to complete. The A and B registers have a maximum value of 255.

2.5.1 High-Pass Filter

The TLC320AC01 also has a high-pass filter which can be used to attenuate subsonic noise and remove dc offsets. The importance of subsonic noise filtering should not be underestimated. For example: air conditioning systems are a notorious source of low frequency noise and a slamming door can produce extremely high levels of subsonic energy. The filter in the TLC320AC01 has a corner frequency of $f_S/200$ and a slope of 6 dB per octave. The corner frequency cannot be changed independently of the sampling frequency.

3 ANALOG OUTPUT

As previously mentioned, the maximum sample rate for the DAC, at 25 kHz, is lower than for the ADC. This limits the bandwidth of the output signal to less than 12.5 kHz.

3.1 Signal-to-Noise and Signal-to-Distortion Ratio

Figure 6 shows the result of intermodulation distortion measurements for the DAC made on the test boards. The noise floor can be seen at approximately –90 dB in the pass band, falling to approximately –108 dB at frequencies above $f_s/2$. There are some distortion products in the pass band at approximately –85 dB. The double peaks at approximately 7 kHz and 9 kHz are images of the signal that have been only partially attenuated by the reconstruction filter. Images are the digital to analog equivalents of aliases in analog to digital conversion. They occur at frequencies given by:

$$f_{image} = N\, f_S \pm f_{in}$$

N = 1, 2, 3 . . .
f_S = sampling frequency

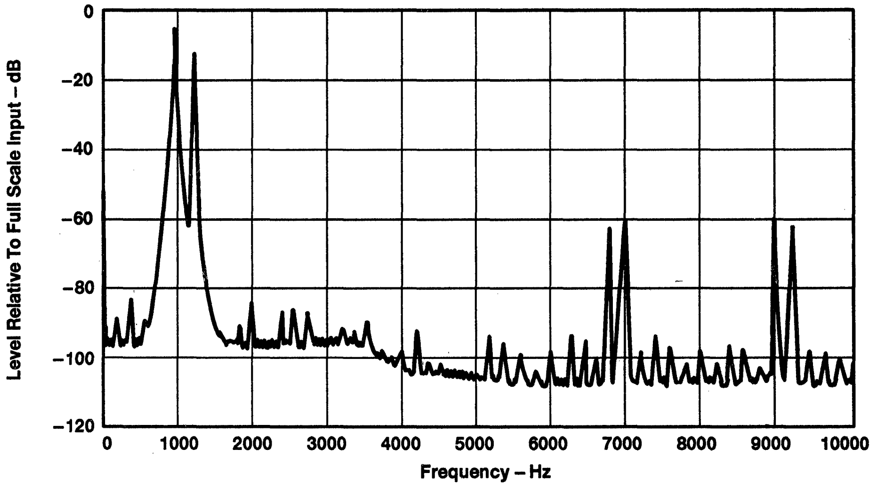


Figure 6. DAC Noise and Distortion Measurements

If the images are to large for a given application they can be removed by continuous-time low-pass filtering at the output of the DAC. The size of the images reflects the 45 dB stop-band attenuation of the reconstruction filter.

3.2 Voltage Swing and PSRR

The voltage swing at the differential output is ±6 V for a full scale output. There are software selectable attenuators giving outputs of 0 dB, –12 dB and a squelch mode of –60 dB. Although there is not a large improvement in SNR ratio by using a differential output stage, it has the added advantage of increasing the PSRR and allowing level shifting to a ground referenced output without having to ac couple the signal. Using a thin film resistor pack for the differential amplifier gives the well matched resistors needed for good common mode rejection and accurate gain. Using a differential amplifier in this way the PSRR was improved from 49 dB to 53 dB (see Figure 7).

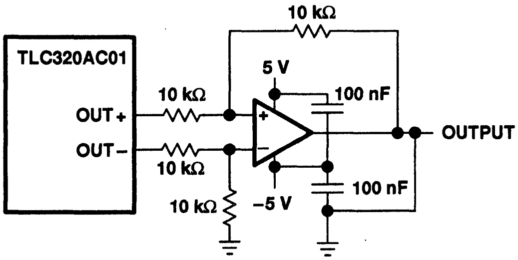


Figure 7. Differential to Single Ended Output Circuit

3.3 (Sin x)/x Correction

(Sin x)/x error arises because the output from a digital-to-analog converter is held constant between samples rather than smoothly joining them up. The TLC320AC01 has a (sin x)/x correction filter. It gives a correct response for a B register value of 15, which gives a ratio of sample rate to ADC anti-aliasing filter of 2.67. But as it does not track the B register, other values for the B register will produce an error in the magnitude of a given output frequency. Figure 8 shows a graph of calculated error versus frequency for various values of B register with a master clock of 10 MHz and sample rate of approximately 8 kHz. Other values can be calculated using the equation given in section 2.15.7 of the TLC320AC01 data manual.

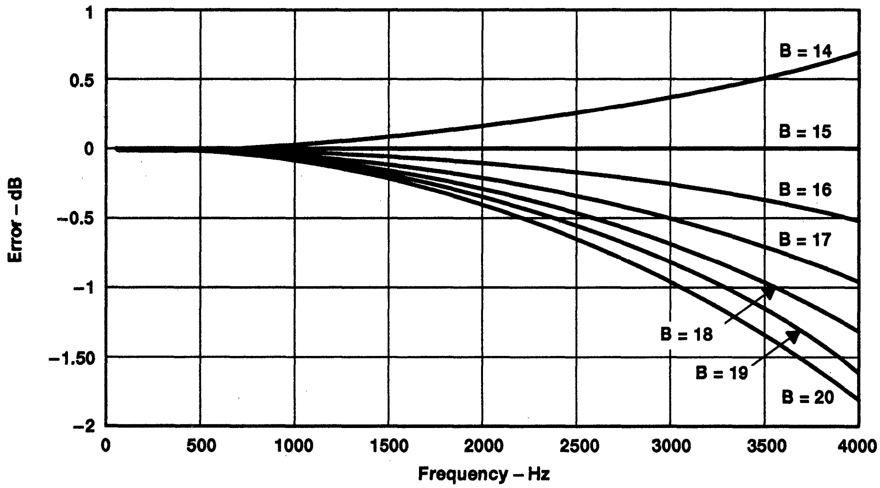


Figure 8. (Sin x)/x Error

4 DIGITAL DESIGN CONSIDERATIONS

4.1 DSP Serial Interface

The TLC320AC01 can be connected directly to the synchronous serial port of a TMS320C25 as shown in Figures 6–1 and 6–3 of the TLC320AC01 data manual. Interfacing the TMS320C50 family requires some caution because the CLKOUT signal will usually exceed the maximum 15 MHz MCLK frequency of the TLC320AC01. So a divider is required. Most makes of DSP chip support the synchronous serial interface and should connect directly to the TLC320AC01.

4.1.1 Maximum Clock Rate

It is highly desirable that the DSP chip and TLC320AC01 are clocked from a common master oscillator. This ensures that the digital noise which is often coupled into the ADC and DAC of the TLC320AC01 in miniature systems is aliased to a stable frequency, preferably dc. Texas Instruments has found that the signal-to-noise ratio can be degraded by as much as 6 dB in a breadboard system when independent clocks are used compared with a fully synchronous system.

A convenient way of phase locking the TLC320AC01 to the processor is to drive the MCLK input of the TLC320AC01 from the CLKOUT of a TMS320C25 or TMS320C50 or from the H1 or H3 output of a TMS320C30. However, because of the higher speed of the TMS320C50 an external one or two stage divider must be used to lower the CLKOUT frequency (which can be between 20 MHz and 40 MHz depending on which speed grade of processor is used) to 15 MHz or less. A SN74ACT74 was chosen for its high maximum clock frequency, relatively low power consumption and availability in surface mount package. The divider power supply current was measured at 6.5 mA at 5 V and 3.17 mA at 3 V when dividing by 2 at 20 MHz; and 20.3 mA at 5 V and 9.6 mA at 3 V when dividing by 4 at 40 MHz.

4.1.2 Synchronization of Negative Rail Generator

If switching power supplies are used in the system, for example to generate a negative supply rail, it is advantageous to phase lock the switching frequency to the sampling frequency. The EOC output from the TLC320AC01 is close to a square wave for reasonable sampling frequencies and can be connected to the OSC pin of a ICL7660 negative supply generator through a small (100 pF) capacitor to force the normally free running oscillator. The small capacitor allows the ICL7660 to free run in the absence of an EOC signal. The ICL7660 divides this signal by two internally, so that power supply ripple is at exactly the Nyquist frequency and hence appears as a small dc offset rather than as an unstable whistle.

4.1.3 Edge Timing

It is important to ensure that the rise and fall times of the serial clock signal between the codec and DSP chip are within specification, particularly if level shifting circuits are used for mixed 5 V and 3 V operation. Failure to do so can result in data or frame sync signals being sampled on the wrong clock edge, causing erratic errors. The shift clock output rise and fall times for the TLC320AC01 in master mode are specified at 19 ns maximum and 13 ns typical in the data manual. The maximum serial clock input rise and fall times for the TMS320C25 are 25 ns, and for the TMS320C30 and TMS320C50 are 8 ns. While it might seem from these specifications that the TLC320AC01 cannot satisfactorily drive the TMS320C30 or TMS320C50 without buffering, these devices do work reliably together as long as very short connections are used.

In order to discover whether the system was operating with a reasonable safety margin, the rise and fall times of SCLK were measured. The measurements were made using a LeCroy oscilloscope sampling at 1 GHz and a FET probe with SCLK from the TLC320AC01 driving the parallel inputs CLKX and CLKR on the TMS320C50. The PCB track length was approximately 10 cm and the width 0.25 mm. The results (shown below) were well within the requirements of the TLC320C50.

	V_{DD} = 5 V	V_{DD} = 4 V
Rise time (0.8 V to 2 V)	2.3 ns	4.1 ns
Fall time (2 V to 0.8 V)	4.4 ns	5.6 ns

4.2 Hardware Design of TMS320C50 Based DSP System

A relatively simple yet powerful DSP system can be built using a TMS320C50 family digital signal processor and a TLC320AC01 AIC, as shown in Figure 9. The circuit shown is a simplified version of one that we have used extensively. It can readily be expanded to include parallel input and output ports. The TMS320C50 has 10K words of on-chip RAM, allowing complex algorithms to be implemented without the need to use external RAM. Some means of program storage is needed. A pair of 8-bit wide 1-Mbit flash EPROMs (N28F001BX-B120 from Intel) were used which completely fill the program and data address spaces, allowing the use of very large data tables. They have the advantages of reasonably low power consumption, especially when idle, the ability to be reprogrammed in-circuit or in a standard programmer (if socketed) and have a hardware protected boot block. The boot block is an 8K byte segment starting at address zero which can be protected against erasure by opening a switch. This allows the EPROM programming algorithm to be safely stored within the EPROM itself, downloaded to on-chip memory and executed from there to reprogram the rest of the flash EPROM with data transmitted through one of the serial ports. This is very convenient when portable equipment is to be reprogrammed in the field, especially when surface mounted devices are permanently soldered into the circuit. The initial bootstrap code can either be loaded using a standard programmer before assembly, or afterwards using the XDS510 in-circuit emulator interface which is brought out to a 14-pin header. These flash EPROMs have an internal state machine to control the erasure and programming algorithms. This is very important, not only because it simplifies programming, but it ensures that the essential precharge step before erasure is applied to all locations. This cannot easily be done with earlier generations of flash memory because those addresses that overlap internal registers and memory cannot easily be accessed. 100 kΩ pull-up resistor packs were used on the data bus and serial port signals to minimize power consumption when the bus is in a high impedance condition, which is the normal condition when executing from on-chip RAM.

A standard, 40 MHz, third overtone crystal oscillator was used to clock the TMS320C50. Exactly 8 kHz or 16 kHz sampling frequencies cannot be obtained with a 40 MHz MCLK. If this is a requirement, an MCLK of 41.475 MHz should be used. A 2.2 µH surface mount inductor blocks oscillation at the fundamental frequency of the crystal. The 330 kΩ resistor biases the on-chip oscillator inverter. Some care is needed in the choice of this value to ensure stable operation and reliable start-up. With the component values shown, the oscillator starts at a supply voltage of approximately 2 V and is stable up to the absolute maximum of 7 V. Alternatively, CLKMD2 of the TMS320C50 can be grounded and an external 20 MHz clock fed into CLKIN2. This provides a divide by 1 option whereby the CPU clock operates at the same 20-MHz frequency. The 20 MHz, CLKOUT1 signal from the TMS320C50 is divided by two using half a SN74ACT74 D-type flip-flop to provide a 10 MHz MCLK to the TLC320AC01.

4.3 Battery Operation

4.3.1 Reset Considerations

The TLC320AC01 undergoes a power-on reset when V_{DD} falls below 4 V with the samples tested. In battery powered systems it is important to ensure that the supply never dips this low, otherwise all the programmed registers will return to their default values. To guard against undetected resetting, the system supply should be monitored, using a comparator as shown in Figure 9 or a supply voltage supervisor such as the TL7702B. Also, one of the registers that has been changed from its default should periodically be read back and checked.

4.3.2 Interfacing to a 3-V DSP Processor

There is a strong incentive to operate DSPs at 3 V or 3.3 V to save power. As the TLC320AC01 resets at a V_{DD} of about 4 V, separate power supplies and level shifting circuits must be used. The signals from a true CMOS DSP such as the TMS320C50 swing from 0 to V_{DD}, that is from 0 V to 3 V. As this is greater than the 2.2-V logic high threshold of the TLC320AC01, all signals from the DSP to the TLC320AC01 can be directly connected, provided that the 5-V supply rises and falls faster than the logic supply at switch on and off, respectively. If the power sequence cannot be guaranteed, the TLC320AC01 inputs should be protected with a series resistor of about 3.3 kΩ compensated with a parallel capacitor of about 1 nF. There will be a small increase in I_{DD} of the TLC320AC01 compared with driving from 0 V to 5 V due to simultaneous conduction by both FETs in the input circuits. Signals from the TLC320AC01 to the DSP cannot be directly connected, however. The simplest interface circuit is a series resistor, to limit the current flowing through the upper protection diode, with parallel compensating capacitor to preserve the rise and fall times, as shown in Figure 10.

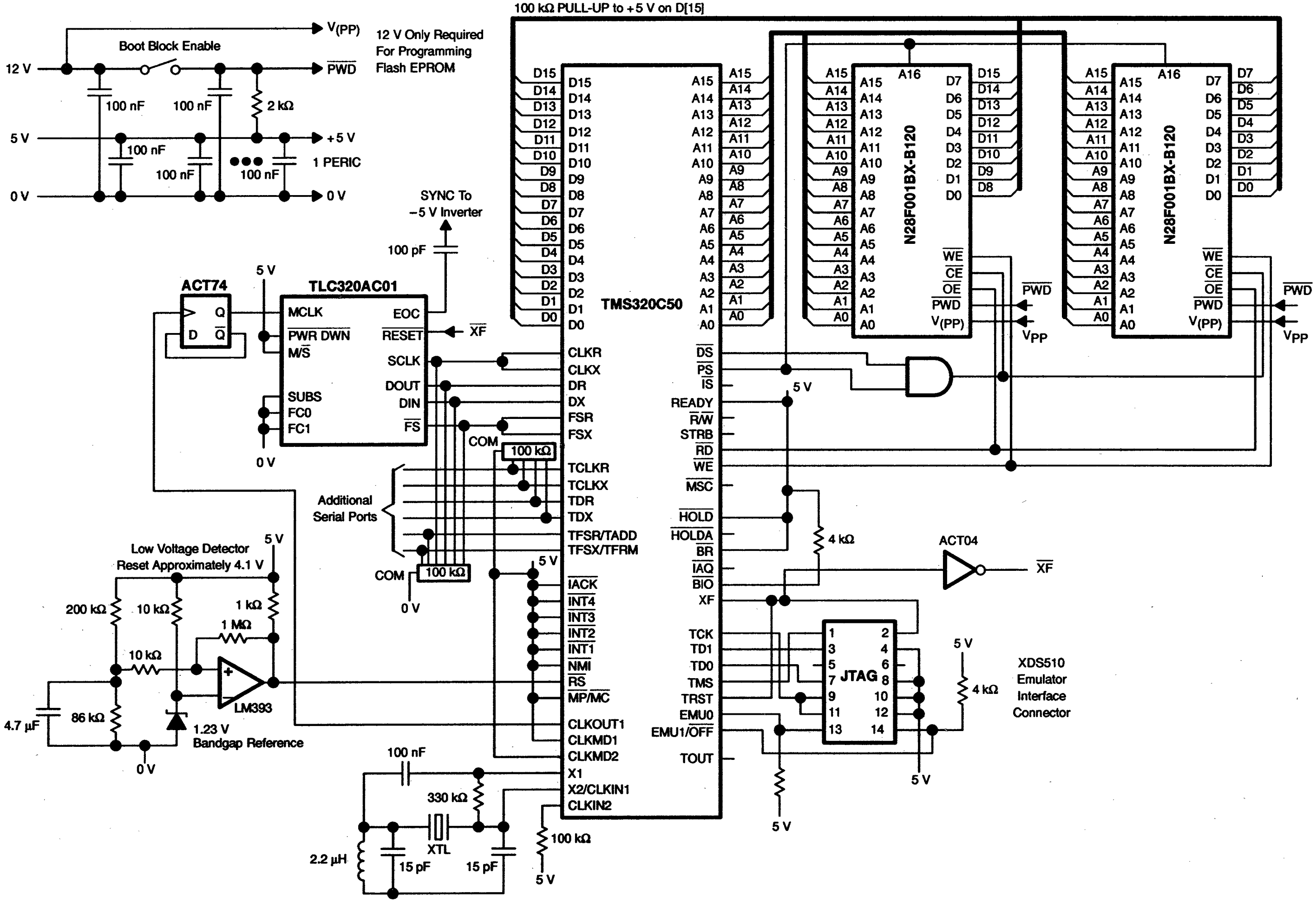


Figure 9. TLC320AC01 to TMS320C50 Hardware Schematic

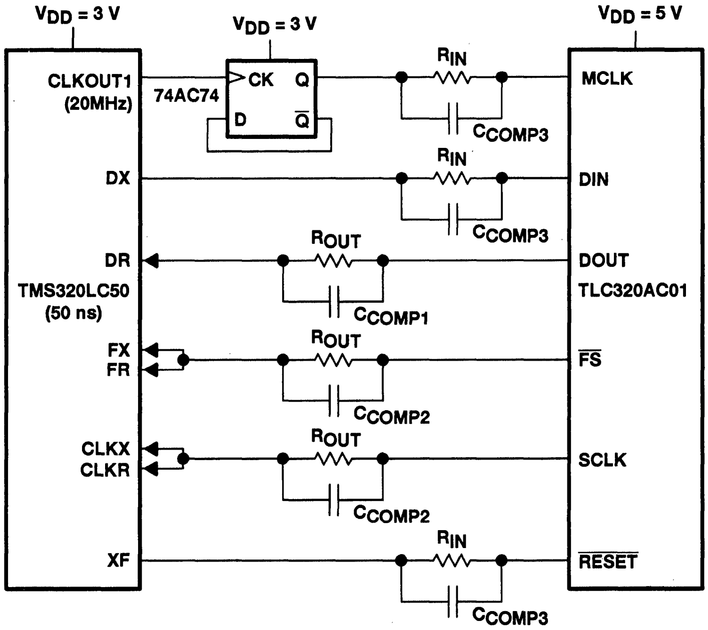


Figure 10. Interfacing to 3-V DSP

4.3.3 Calculation of Interface Component Values

Assuming that a transient input current through the protection diodes of 1 mA at power-up is safe for both devices and that the order of rise and fall is unknown. Then, 3.3 kΩ resistors (R_{IN}) in series with the TLC320AC01 inputs and 5.6 kΩ resistors (R_{OUT}) in series with the outputs provide full protection.

To calculate the appropriate compensation capacitor for signals from the TLC320AC01 to the TMS320C50, treat the parallel combination of C_{IN} and C_{STRAY} in conjunction with C_{COMP} as a capacitive divider where:

$$V_{OUT} = \frac{V_{IN} C_{COMP}}{C_{COMP} + C_{IN+STRAY}}$$

rearranging:

$$C_{COMP} = \frac{C_{IN+STRAY} V_{OUT}}{V_{IN} - V_{OUT}}$$

Substituting for worst case power supplies of 3.3 V and 4.5 V with one TMS320C50 input load of 15 nF and 10 pF stray capacitance:

For one input:

$$C_{COMP1} = \frac{(15 + 10) \times 3.3}{4.5 – 3.3} \approx 68 \text{ pF}$$

For two inputs:

$$C_{COMP2} = \frac{(15 = 15 + 10) \times 3.3}{4.5 – 3.3} \approx 120 \text{ pF}$$

These capacitor values should not be greatly increased because the input protection diodes of the TMS320C50 would then be driven into transient conduction on each rising logic edge.

The same method is applied to calculate the compensation capacitor for signals going to the TLC320AC01 (e.g., $\overline{\text{RESET}}$, MCLK and DIN). Assume a TLC320AC01 input capacitance of 5 pF and 10 pF stray capacitance, a worst case V_{DD} for the TMS320C50 and TLC320AC01 input threshold of 2.2 V.

$$C_{COMP3} = 68 \text{ pF}$$

This is a minimum value. C_{COMP} should be as large as possible for lowest power consumption and best noise margin. The maximum value of C_{COMP} depends upon the DSP chip power supply rise time. Switching three series connected 1.2 Ah NiCd cells with a total internal resistance of 30 mΩ into 200 µF of decoupling capacitance gives a maximum dV/dt of approximately 1 V/µs. In practice, wiring inductance and the resistance of protective fuses limit dV/dt to <0.1 V/µs.

$$C_{IN}\Big|_{MAX} = I_{IN}\Big|_{MAX} * \frac{dV_{DD}}{dt}\Big|_{MAX}$$

Therefore, C_{IN} should not greatly exceed 1 nF.

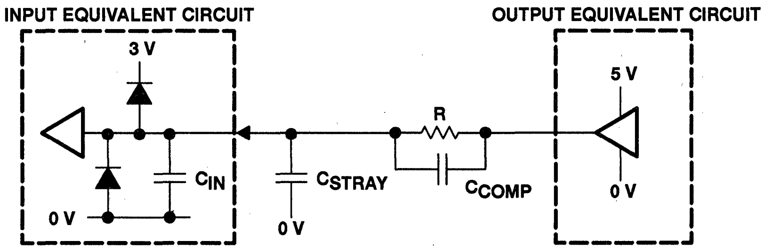


Figure 11. Interfacing to 3-V DSP – Component Values

4.4 Programming

4.4.1 Initialization

Only those registers that have to be changed from their defaults need to be reprogrammed. The initialization process consists of sending pairs of data values from the 16-bit synchronous serial interface of the DSP chip to the TLC320AC01. In most cases the first word of the pair will be 0000 0000 0000 0011B. The 14 most significant bits of this value (bits 15 to 2) specify that an output sample of zero be sent and the two least significant bits (bits 1 and 0) specify that the next word transmitted will be interpreted as a secondary communication.

The secondary data value is used to reprogram one of the nine registers. Bits 15 and 14, which control phase shifting in modem applications will usually be zero, bit 13 = 0 specifies that data is to be written to a register, bits 12 to 8 define the address of the register that is to be changed. Bits 7 to 0 contain the data to be stored in the register.

4.5 Register Descriptions

4.5.1 Pseudo Register 0 (no-op)

The main purpose of R0 is to allow phase shift commands to be sent as secondary communications without reprogramming any other register. It is not needed for most applications.

4.5.2 Register 1 (A Register)

The A register sets half the number by which the master clock input (MCLK) is divided to provide the switched capacitor filter clock (FCLK). This is also the principal method for setting the sampling frequency.

4.5.3 Register 2 (B Register)

The B register sets the ratio between the low-pass filter corner frequency and the sampling frequency. For most purposes the default, or a value close to it will be appropriate.

4.5.4 Register 3 (A′ Register)

The A′ register is used for phase shift control and can be ignored for most purposes.

4.5.5 Register 4 (Amplifier Gain Select Register)

This allows the gains of the analog input and output to be varied by –6 dB or –12 dB or disabled. The monitor output can be varied by –8 dB or –18 dB or disabled.

4.5.6 Register 5 (Analog Configuration Register)

This selects whether the high-pass filter is to be disabled, thus allowing the codec to respond to dc, and controls the input multiplexer.

4.5.7 Register 6 (Digital Configuration Register)

Control operating modes and power-down options. The defaults will be suitable for many applications.

4.5.8 Register 7 (Frame-Sync Delay Register)

This controls the timing of the serial data transmission of a slave converter in multi-channel multiplexed systems.

4.5.9 Register 8 (Frame-Sync Number Register)

This controls the number of frame-sync pulses generated, corresponding to the number of channels being multiplexed on to the bused serial interface. The default of 1 is suitable for single channel operation.

4.6 TLC320AC01/TMS320C50 Demonstration Program

The demonstration program AC01DEMO.ASM carries out the simplest possible operation, reading in a sample from the ADC in the TLC320AC01 and then writing it to the DAC. It is assembled and linked using the commands in the batch file MAKE.BAT. This is called as follows: MAKE AC01DEMO.

The program begins with the definition of some variables and allocation of their memory locations. The COFF assembler used here does not assign absolute addresses, but instead relative positions within named blocks of memory. The linker then resolves these references in conjunction with information stored in the linker command file AC01DEMO.CMD.

The next section of the program is the definition of macros that will be used later. Using macros makes the main program listing easier to understand by hiding some of the frequently repeated details.

The section called vectors is loaded into flash EPROM at address zero, which is where the TMS320C50 starts executing after reset. The .text section is the main body of the program, and would typically be loaded into the memory section flashp defined in the command file. In this example, however, it has been placed immediately after the vectors section in the protected bootstrap area for convenience of testing.

The main program starts by initializing certain processor registers that are undefined or have unsuitable defaults at start-up, then clearing the memory variables. The code which is to run in real-time is copied from flash EPROM to the on-chip single-access RAM block for maximum speed of execution. The serial port is initialized to use external clock and frame synchronization pulses, and to transfer 16-bit data words. The initial behavior of the serial port is unpredictable when it is reset with the frame sync input high, as is the case when the TLC320AC01 is inactive. Therefore, a dummy value of zero is sent, and afterwards the TLC320AC01 is again reset briefly. Now the interface is properly initialized and the program branches to the real-time processing loop.

The processor waits in a low power idle mode until an interrupt is received. Then it determines whether the interrupt was from the serial port, in which case it executes the processing loop. The processed results from the previous sample are written to the serial port data transmit register, then the fresh ADC data is read in from the data receive register and processed. The results are stored ready to be sent to the DAC on the next interrupt. This double buffering method maximizes the processing time available because processing can take place while serial data is being transmitted and received. The two least significant bits of the output data are masked out to ensure that a secondary communication request is not inadvertently sent.

The serial port receive interrupt routine simply sets a flag to indicate that data is available. There is no need to have a separate transmit interrupt because the transmit and receive operations are inherently synchronous with each other.

4.7 TMS320C50 Assembler Listing

```
    .title "'AC01 demonstration program"
    .width 200
    .version 50          ; Makes assembler generate C50 code
    .mmregs              ; Predefine names for memory mapped registers

; This program initializes the 'C50 processor and serial port, then initializes the '
; 'AC01 codec and starts the main signal processing loop. In this example, a data
; sample is read from the adc and written back to the dac unchanged.

; Using rev 6.40 or higher assembler tools, use the following make file

; @echo off
; if "%1" == "" goto  :nofile
; dspa %1.asm -x -w -s -v50 -1
; if not errorlevel 1 dsplnk %1.obj -o %1.out -m %1.map %1.cmd
' gpt  "dpme
; :nofile
; echo no source file!
; :done

; -s option makes all symbols global, and thus accessible to the emulator and
; simulator.
; -w option warns about pipeline conflicts.
; -x option makes a cross reference table.
; -1 option generates listing file

; If an eprom programmer is used it may also be necessary to use the DSPHEX conversion
; program to split the linker output file which is in COFF format into a pair of high
; and low byte files in HEX format.

FSAMP     .set 16      ; 8 seslects 8 kHz, 16 selects 16 kHz

; The following 2 variables must be in memory block b2 and dp set to 0 because they
; are accessed by direct addressing

gotdataflag  .usect    "b2", 1   ; used to signal that an interrupt came from the
                                 ; serial input port
outputbuffer .usect    "b2", 1   ; temporarily store output sample

; Macro definitions

waitint .macro
waitint?
       lacc   gotdataflag
       bz     waitint?          ; wait for semaphore to be changed
       splk   #0, gotdataflag   ; set it again
       .endm

progreg .macro progval
       splk   #11b, dxr         ; request secondary comms
       waitint                  ; wait for transmission
       splk   #:progval:, dxr   ; send value
       waiting                  ; wait . . . .
       .endm

       .sect "vectors"          ; vectors is the starting point of a block of program
                                ; memory starting at address zero

Interrupt vectors - these start at address zero
; unused interrupts branch to themselves so that if they are inadvertently activated
; they can be identified using the xds510 emulator
rs      b  mainentry
intl    b  intl
int2    b  int2
int3    b  int3
tint    b  tint
rint    b  getdata
xint    b  xint
trnt    b  trnt
txnt    b  txnt
int4    b  int4
rsvd14  b  rsvd14
rsvd16  b  rsvd16
rsvd18  b  rsvd18
rsvd1A  b  rsvd1A
rsvd1C  b  rsvd1C
```

```
rsvd1E  b  rsvd1E
rsvd20  b  rsvd20
trap    b  trap
nmi     b  nmi
rsvd26  b  rsvd26
rsvd28  b  rsvd28

       .text     ; .text indicates start of main program storage block in flash eprom

mainentry        ; this is the startu entry point
   ldp    #0     ; data page pointer to page zero
   setc   INTM   ; globally disable interrupts
   setc   SXM    ; set sign extension mode
   setc   OVM    ; set saturation on arithmetic overflow

; Disable address visibility (to save power by not driving address bus)
; set up on-chip single access ram and B0 to be in data space for initialization.
   splk   #0000000010101000b, PMST
   circ   CNF    ; B0 is in data space

; Set up wait state control registers for 2 wait states when accessing flash eprom
   splk   #00000b,  CWSR
   splk   #1010101010101010,  PDWSR

   splk   #0, gotdataflag      ; zero data received flag
   splk   #0, outputbuffer     ; zero output storage buffer

; relocate speed critical part of program to on chip ram
   lrlk   AR1, 800h            ; address in data memory of start of ram block
   larp   AR1
   lacc   #ocramstart          ; address in flash memory of start of code
   rpt    #ocramend-ocramstart-1
   tblr   *+

   apl    #1111111111011111b, PMST      ; remove ram from data space
   opl    #0000000000100000b, PMST      ; put it in program space

; set all interrupt masks except serial receive
   splk   #000010000b, IMR

; set up serial port
   splk   #0, dxr              ; zero the data transmit register
   splk   #0001000b, SPC       ; use ext clock and frame sync
   opl    #0c0h, SPC           ; take it out of reset

; clear all interrupt flag bits
   splk   #0ffffh, IFR
   clrc   intm                 ; enable interrupts

   clrc   xf         ; release codec from reset
waitint              ; waiat for interrupt from serial port

; this code assumes that XF is inverted in hardware
; reset the codec and release it again to make it ignore first garbage word
; generated by serial port in revision 1 'C50 silicon
   setc   xf
   rpt #10           ; hold 'AC01 reset low for at least 1 MCLK period
   nop               ; ie > 100 ns for MCLK = 10 MHz
   clrc   xf

; serial interface and 'AC01 are now in a stable state

; setup codec - only need to reprogram those registers that need to be changed from
; their defaults
                                        ; reg 0 = no op
                                        ; reg 1 = A register (18 = default)
       .if FSAMP = 8
          progreg 0000000101000101b     ; 36 -> 8 kHz @10.368 MHz clockin
       ;endif                           ; 35 -> 7.937 kHz @10 MHz

       .if FSAMP = 16
          progreg 0000000100100010b     ; 18 -> 16 kHz @10.368 MHz clockin
       .endif                           ; 17 -> 16.34 kHz @10 MHz
```

```
          progreg    0000001000010010b       ; reg 2 = B register (18 = default)
;                    ||||||||||||||||
;                    ||||||||++++++++----- data
;                    |||+++++------------- address
;                    ||+------------------ 0 = write
;                    ++------------------- Phase shift

                                             ; reg 3 = A' register
          progreg    0000010000011001b       ; reg 4 = amplifier gain select
;                    ||||||||||||||||
;                    ||||||||||||||++----- output     0=sq, 1=0 dB, 2=-6 dB, 3=-12 dB
;                    ||||||||||||++------- input      0=sq, 1=0 dB, 2=+6 dB, 3=+12 dB
;                    ||||||||||++--------- monitor    0=sq, 1=0 dB, 2=-8 dB, 3=-18 dB
;                    ||||||||++----------- no used
;                    |||+++++------------- address
;                    ||+------------------ 0 = write
;                    ++------------------- Phase shift
          progreg    0000010100000101b       ; reg 5 = analog configuration
;                    ||||||||||||||++----- 0=loopback, 1=norm i/p, 2=aux i/p, 3=both
;                    |||||||||||||+------- 0=hp filter on, 1=hp filter off
;                    ||||||||||||+-------- 0=echo off, 1=echo on
;                    ||||||||++++--------- not used
;                    |||+++++------------- address
;                    ||+------------------ 0=write
;                    ++------------------- Phase shift

                                             ; reg 6 = digital configuratjon
                                             ; reg 7 = frame sync delay
                                             ; reg 8 = frame sync number

    b   passthrough      ; branch to real-time code in on-chip ram
; This section is relocated to on-chip single access ram block for faster operation

      .sect "ocram"
      .label ocramstart   ; this label referes to the address where the following
                          ; code is stored in eprom, not the address from which it
                          ; is executed

passsthrough              ; this label refers to the execution address in on-chip ram
; Main signal processing loop

      clrc   intm         ; Wait for any interrupt, determine whether
      nop                 ; it is caused by serial data input and branch
      idle                ; back to idle if not.
      setc   intm         ; WARNING - The manipulation of INTM and the
      lacc   gotdataflag  ; nop, idle sequence are necessary to prevent
      bz     passthrough  ; serial interrupts from being missed if they
      clrc   intm         ; occur just after another interrupt!
      splk   #0, gotdataflag  ; clear the data received flag

      out outputbuffer, dxr   ; write the data derived from the previous input sample
                              ; to the serial port data transmit register
      lacc   drr    ; read a codec input sample from the serial port data receive
                    ; register. Data is in low accumulator
      ; do the signal processing here, leaving result in accumulator
      ; . . .
      ; . . .
      ; . . .

      and    #1111111111111100b  ; mask out bottom two bits to ensure that secondary
                                 ; communications are not accidentally requested

      sacl outputbuffer          ; save the result of the prcessing until the next
                                 ; interrupt, and only then write it to the serial
                                 ; port. This maximizes the processing time available.

      b      passthrough
; Interrupt handlers
; because the transmit and receive operations of the 'AC01 are synchronous
; only one serial port interrupt handler is needed
```

```
getdata   splk   #1, gotdataflag  ; set a flag to indicate data available
          rete   ; return from interrupt, restoring context and re-enabling interrupts

          .label ocramend  ; end of block transferred to on-chip ram
.end
```

4.8 Linker Command File: AC01DEMO.CMD Listing

```
MEMORY          /* memory map for C50 */
{
page 0  :/* program memory */
reset   : origin = 0,     length = 800h /* booth block up to start of on chip ram +/
onchipp :origin = 800h, length = 2400h /* on chip program memory*/

flashp : origin = 8000h, length = 7200h /* top half flash prog except b0 */
param2 : origin = 3000h, length = 1000h /* second parameter block in eprom */
                                     /* par. block is overlaid by on-chip ram */

page 1 : /* data memory */
   b3  : origin = 60 h, length = 20h
   b0b1   :origin = 800h, length = 240h /* ocram is on-chip data if OVLY=1 */
                                      /* external flash eprom if OVLY=0 */

}
SECTIONS
{      vectors    : load = reset page 0
       .text  : load = flashp page 0
       param2 : load = param2 page 0
       ocram  : load = flashp page 0 run = onchipp page 0

       be     : load = b2 page 1 /* data page 0 on-chip ram */
       .bss   : load = b0b1 page 1
}
```

4.9 Measuring the DAC Filter Response with a White Noise Generator

A convenient way of measuring the frequency response of a linear system is to excite it with white noise and measure the response with a spectrum analyzer. This example shows how white noise can be generated by a very short random bit generator program and used to measure the response of the TLC320AC01's DAC reconstruction filter.

The random bit generator implements a recurrence relation in a primitive polynomial modulo 2 of order 31 (reference 1). This gives a maximal length sequence of pseudo-random bits which only repeats after $2^{31}-1$ iterations. The polynomial used is $x^{31}+x^3+x^0$, although there are many others to choose from. A 32-bit variable, noise_sr, which is initially seeded with any non zero value, stores the state between iterations. On each iteration, the accumulator is loaded from noise_sr and shifted left one bit. The most significant bit (now in the carry bit) is then exclusive ORed (XOR) with the remaining non zero terms. Each bit that has been XORed is stored back into the same location in the accumulator and the result is saved. This is implemented by testing the carry bit after the shift with the execute conditional (XC) instruction. If C was 0, do nothing because anything XORed with 0 is 0 and bit zero of the accumulator is filled with a 0 after a shift. If C was 1, XOR the low accumulator with the constant 10010b which achieves the desired result.

There are three main limitations to this technique. Because the XOR is only carried out on the 16 least significant bits there must not be any non zero terms in the polynomial above x15 apart from x31. The contents of the accumulator should not be used directly as a random number because successive values are correlated as the bits work their way to the left. This is overcome in the example by iterating the code 14 times for each sample. Although the noise has a white long-term spectrum (that is equal power per unit frequency), it is nongaussian. This does not matter for frequency response measurements.

Figure 12 shows the response of the TLC320AC01 reconstruction filter measured at a sampling rate of 7.937 kHz. The A register value is 42, the B register value is 15 and the MCLK frequency is 10 MHz.

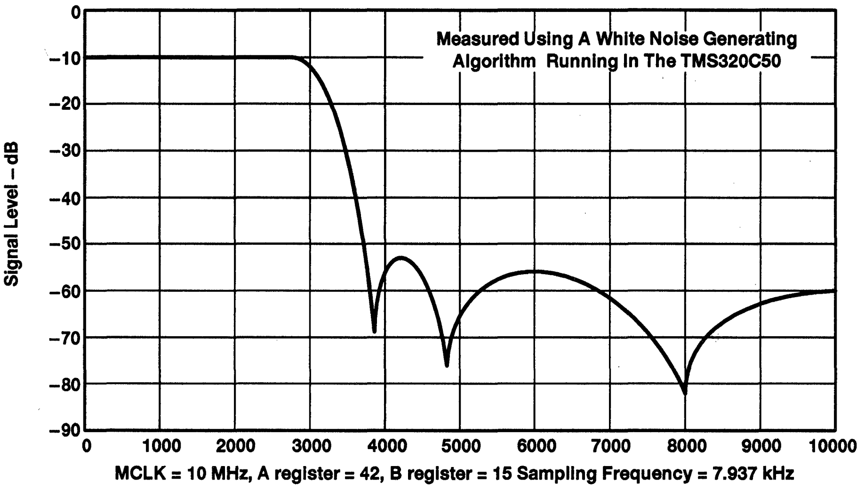


Figure 12. DAC Channel Frequency Response

4.10 Example Noise Generator Code Listing

```
noise_sr      .usect "b2", 2   ; allocate 32 bits of data memory
;. . .
       larp   AR1    ; seed random bit generator with 2
       lrlk   AR1, noise_sr
       lac    #2
       sacl   *+
       zac
       sacl   *

; . . .

; execute this section once per dac output sample
       larp   AR1
       lrlk   AR1, noise_sr
       lacl   *+              ; load low accumulator from data memory
       add    *, 16           ; load high accumulator
       splk   #13, brcr       ; repeat block 14 times to decorrelate sequential bits
       rptb   end_noise - 1
       sfl                    ; need a 1 cycle gap between sfl and xc to
       nop                    ; allow for pipeline delay
       xc     1, C            ; execute next instruction if carry set
       xor #10010b            ; xor bit 3 with bit 31, copy bit 31 to bit 0
end_noise

       sach   *-              ; save high accumulator to data memory
       sacl   *               ; save low accumulator

; Write low accumulator to transmit data register (after masking out bottom 2 bits)
```

5 SAMPLING AND QUANTIZATION – TUTORIAL

5.1 Sampling

5.1.1 Ideal Sampling

In converting a continuous time signal into a discrete digital representation, the process of sampling is a fundamental requirement. In an ideal case, the sampling signal is a train of impulses (infinitesimally narrow with unit area). The frequency of these impulses is the sampling rate (f_S). The input signal can also be idealized by considering it to be truly band limited, containing no components in its spectrum above a certain frequency.

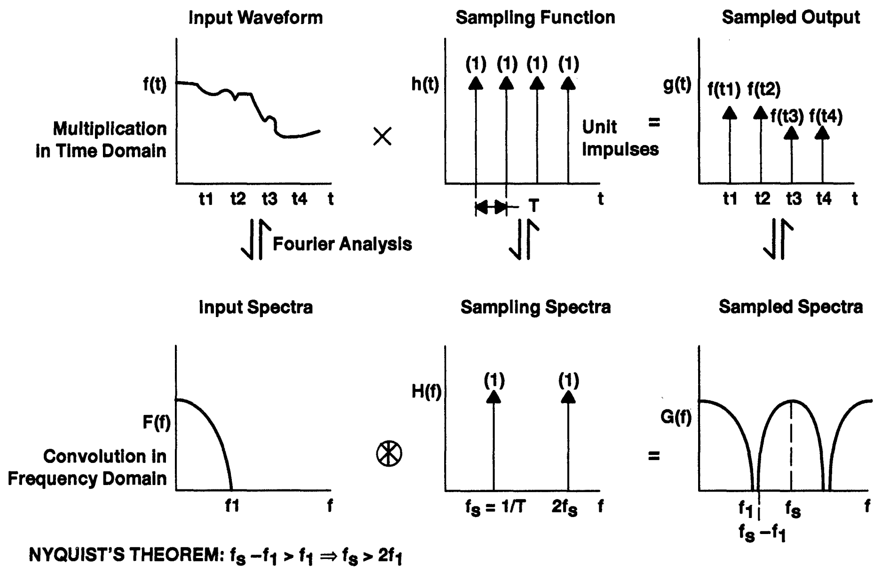


Figure 13. Ideal Sampling

The ideal sampling condition is shown in Figure 13, represented in both the frequency and time domains. The effect of sampling in the time domain is to produce an amplitude modulated train of impulses representing the value of the input signal at the instant of sampling. In the frequency domain, the spectrum of the pulse train is a series of discrete frequencies at multiples of the sampling rate. Sampling convolves the spectrum of the input signal with that of the pulse train to produce the combined spectrum shown, with double sidebands around each discrete frequency which are produced by the amplitude modulation. In effect, some of the higher frequencies are folded back so that they produce interference at lower ones. This interference causes distortion which is called aliasing. Aliases cannot be removed by subsequent processing.

As shown in the diagram, if the input signal is band limited to a frequency f_1 and is sampled at frequency f_S, the overlap (and hence aliasing) cannot occur if

$$f_1 < f_S - f_1 \text{ or } 2f_1 < f_S$$

Therefore, if sampling is performed at a frequency at least twice as great as the maximum frequency of the input signal, no aliasing occurs and all of the signal information can be extracted. This is *Nyquist's Sampling Theorem*, and it provides a basic criterion for the selection of the sampling rate required by the converter to process an input signal of a given bandwidth.

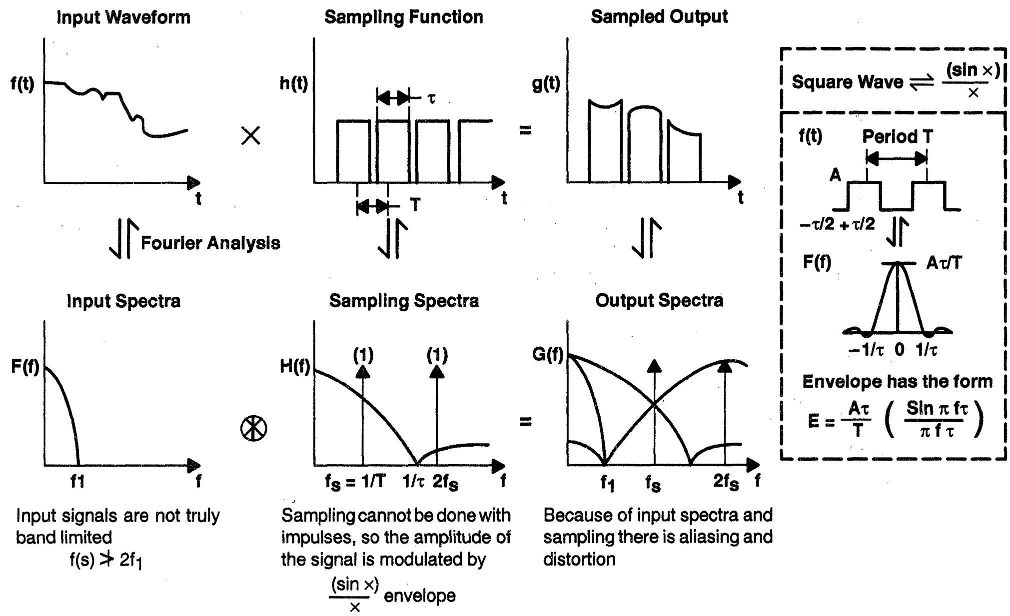


Figure 14. Real Sampling

5.1.2 Real Sampling

The concept of an impulse is a useful one to simplify the analysis of sampling. However, it is a theoretical ideal which can be approached but never reached in practice. Instead the real signal is a series of pulses with a period equalling the reciprocal of the sampling frequency. The result of sampling with this pulse train is a series of amplitude modulated pulses.

Examining the spectrum of a square wave pulse train shows a series of discrete frequencies, as with the impulse train, but the amplitude of these frequencies is modified by an envelope which is defined by (sin x)/x (sometimes written sinc(x)) where x in this case is πf_s. For a square wave of amplitude A, the envelope of the spectrum is defined as

$$\text{Envelope} = A\left(\frac{\tau}{T}\right)\left[\sin(\pi f_s \tau)\right]/\pi f_s \tau$$

The error resulting from this can be controlled with a filter which compensates for the sinc envelope. This can be implemented as a digital filter, in a DSP, or using conventional analog techniques. (The TLC320AC01 analog interface circuit has an on-chip (sin x)/x correction filter after its DAC output for this purpose.)

5.1.3 Aliasing Effects and Considerations

In practice, any real signal has infinite bandwidth. However, the energy of the higher frequency components become increasingly smaller so that at a certain value they can be considered to be irrelevant. This value is a choice that must be made by the system designer.

As shown, the amount of aliasing is affected by the sampling frequency and by the relevant bandwidth of the input signal, filtered as required. The factor that determines how much aliasing can be tolerated is ultimately the resolution of the system. If the system has low resolution, the noise floor is already relatively high and aliasing can have an insignificant effect. However, with a high resolution system, aliasing can increase the noise floor considerably and therefore needs to be controlled.

As shown, increasing the sampling rate is one way to prevent aliasing. However, there is a limit on what frequency this can be, determined by the type of converter used and also by the maximum clock rate of the digital processor receiving and transmitting the data. Therefore, to reduce the effects of aliasing to within acceptable levels, analog filters must be used to alter the input signal spectrum.

5.2 Theoretical SNR for a 14-Bit Device

The analog input to an ADC is a continuous signal with an infinite number of possible states, whereas the digital output is by its nature a discrete function with a number of different states determined by the resolution of the device. It follows from this therefore, that in converting from one form to the other, certain parts of the analog signal that were represented by a different voltage on the input, are represented by the same digital code at the output. Some information has been lost and distortion has been introduced into the signal. This is quantization noise.

For an ideal staircase transfer function of an ADC, the error between the actual input and its digital form has a uniform probability density function if the input signal is assumed to be random. It can vary in the range of $\pm 1/2$ least significant bit (LSB) or $\pm q/2$ where q is the width of one step.

$$p(\varepsilon) = 1/q \text{ for } -q/2 \le \varepsilon \le +q/2$$

$$p(\varepsilon) = 0 \text{ otherwise}$$

The average noise power (mean square) of the error over a step is given by

$$E^2(\epsilon) = \frac{1}{q} \int_{q/2}^{+q/2} \epsilon^2 d\epsilon$$

which gives $E^2(\varepsilon) = q^2/12$

The total mean square error, N^2, over the whole conversion area is the sum of each quantization level's mean square multiplied by its associated probability. Assuming the converter is ideal, the width of each code step is identical and therefore has an equal probability. Hence for the ideal case

$$N^2 = \frac{q^2}{12}$$

Considering a sine wave input F(t) of amplitude A so that

$$F(t) = A \sin \omega t$$

which has a mean square value of $F^2(t)$, where

$$F^2(t) = \frac{1}{2\pi} \int_0^{2\pi} A^2 \sin^2(\omega t) dt$$

which is the signal power. Therefore the signal-to-noise ratio (SNR) is given by

$$\text{SNR(dB)} = 10 \text{ Log}\left[\left(\frac{A^2}{2}\right)\Big/\left(\frac{q^2}{12}\right)\right]$$

But $q = 1 \text{ LSB} = 2A/2^n = A/2^{n-1}$

Substituting for q gives

$$\text{SNR} = 10 \text{ Log}\left[\left(\frac{A^2}{2}\right)\Big/\left(\frac{A^2}{3 \times 2^{2n}}\right)\right] = 10 \text{ Log}\left(\frac{3 \times 2^{2n}}{2}\right)$$

$$\Rightarrow 6.02n + 1.76 \text{ dB}$$

This gives the ideal value for a perfect n-bit converter and shows that each extra bit of resolution provides approximately 6 dB improvement in the SNR. In practice, errors in the ADC introduce non-linearities that lead to a reduction of this value.

For a perfect 14-bit converter, the SNR is:

$$6.02 \times 14 + 1.76 \approx 86 \text{ dB}$$

5.3 References

1. William H. Press, Brian P. Flannery, Saul A. Teukolsky and William T. Vetterling, 1988, Numerical Recipies in C – The Art of Scientific Computing, (Cambridge: Cambridge University Press) pp 224–228.
2. TLC320AC01 Analog Interface Circuit Data Manual; SLAS057A
3. TMS320C2x User's Guide; SPRU014C
4. TMS320C5x User's Guide; SPRU056B
5. TMS320 Fixed-Point DSP Assembly Language Tools; SPRU018C

Interfacing the TLV1549 10-Bit Serial-Out ADC to Popular 3.3-V Microcontrollers

TEXAS INSTRUMENTS

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Contents

List of Illustrations

INTRODUCTION

The TLV1549 is a 10-bit serial out analog-to-digital converter that operates from a 3.3-V (±0.3 V) single supply. It uses a switched-capacitor successive-approximation method to perform the conversion in a maximum of 21 μs.

This application report describes how to interface the TLV1549 to three popular microcontrollers which operate from a single 3.3-V supply rail. These are the 68HC05, the TMS70C02, and the 80C51-L.

Interface Timing

The timing for each of the interfaces described in this application report is illustrated in Figure 1. One chip-select ($\overline{CS}$) pulse is used for each 10-bit conversion and 16 CLOCK I/O pulses are between each $\overline{CS}$.

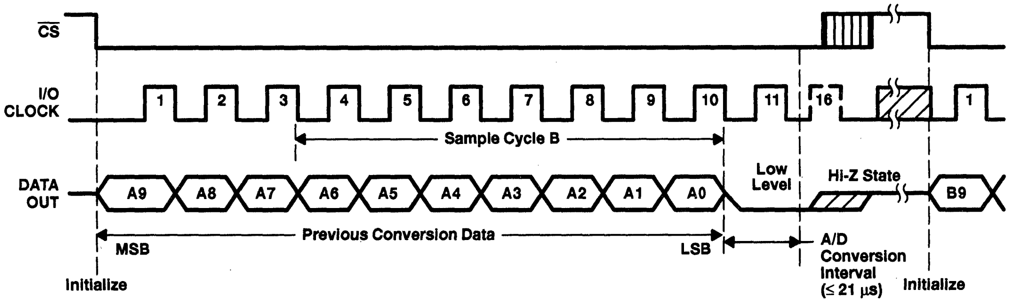


Figure 1. Timing for the 11- to 16-Clock Transfer Using $\overline{CS}$ (Serial Transfer Completed After 21 μs)

Use of Software Subroutines

The subroutines included in this application report have been developed as much as possible as relocatable pieces of software. They include a provision for setting the number of consecutive conversions to be performed. This is either set in the main program as in the TMS7000 and 80C51-L examples or inside the subroutine as used in the 68HC05 example, by programming the number of conversions into COUNT. It is recommended that at least two conversions are performed either after a power-up reset or after a protracted interval between the last conversion. This enables the TLV1549 on-board sample-and-hold to acquire the most recent signal level during the first conversion cycle before converting it into digital form during the second cycle.

Data Format

In whatever format the data arrives at the microcontroller, it is important to ensure that any reformatting, if required, puts the data into a convenient final format. This application report places the most significant byte of the conversion result in one byte of random access memory (RAM) and the least significant byte in an adjacent byte of RAM. The two least significant bits of the 10-bit result are placed in the least significant bit locations of their RAM location.

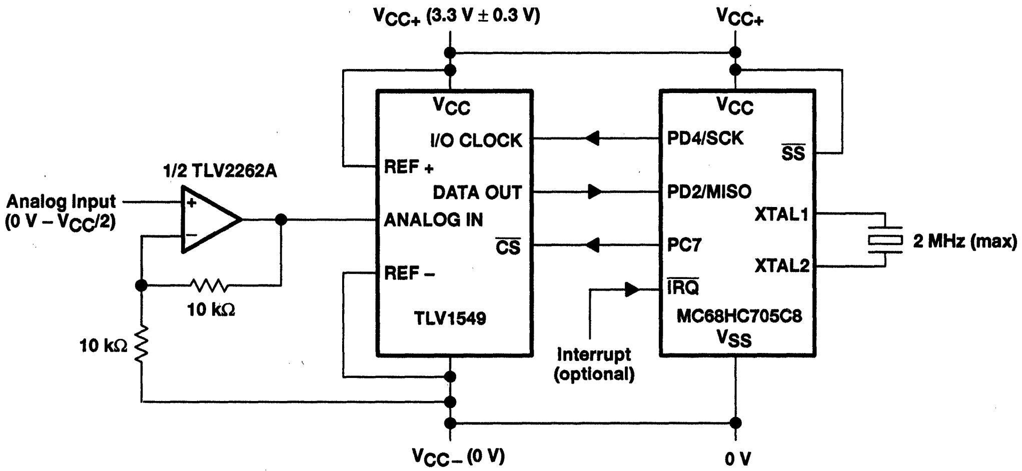
This format gives the user the flexibility to use only 8-bit precision data, if so required, to add the MS and LS bytes together for use in 16 bit wide architectures, to view the two least significant bits of the result for fine tuning applications, or to reformat into another more convenient format.

TLV1549-TO-68HC05 INTERFACE

Microcontroller Features

The M68HC05 family of microcontrollers consists of several different product variants of the basic architecture. It is important that the correct product type is specified to ensure that it contains all the features and attributes necessary to fulfill all its eventual system requirements.

In the case of its suitability for interfacing to the TLV1549 serial out ADC, the M68HC05 product type should contain a serial peripheral interface (SPI). Several types contain this feature including the MC68HC705C8, which was chosen as the target for this ADC interface.



NOTE: For 68HC05 operating off 3.3 V dc supply:
Maximum I/O clock frequency = maximum crystal clock frequency/4 = 0.5 MHz

Figure 2. TLV1549 10-Bit Serial Out ADC-to-MC68HC705C8 Microcontroller Interface

Interface Circuit

Figure 2 shows the circuit interconnections for the TLV1549 – MC68HC705C8 microcontroller interface. No glue logic is required. The positive reference to the TLV1549 is provided directly from the V_{CC+} supply. The analog signal is scaled by an appropriate factor (a gain of two in this case) and buffered by one half of a TLV2262A dual operational amplifier.

The three digital interface terminals, I/O CLOCK, DATA OUT, and $\overline{CS}$ of the TLV1549 connect directly to the PD4/SCK, PD2/MISO, and PC7 terminals respectively of the microcontroller. When the SPI is enabled, PD4 becomes SCK, which is the serial clock output, and PD2 becomes the master in slave out (MISO) terminal. When programmed to be a master device, the microcontroller receives serial data at its MISO terminal.

Figure 3 shows the shift register operation of the SPI when connected to a serial output peripheral component such as the TLV1549. The MC68HC705C8 operates as the master device and the TLV1549 acts as the slave.

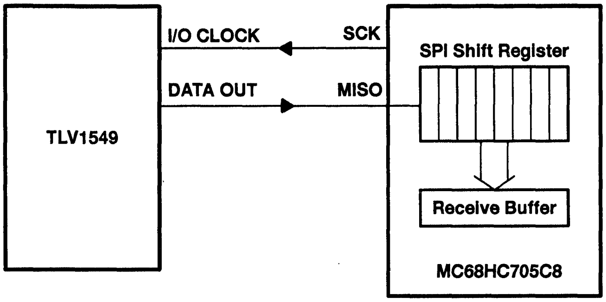


Figure 3. Shift Register Operation of the Serial Peripheral Interface (SPI)

Software Considerations

The three registers which are used for SPI communications are:

Serial peripheral control register (SPCR)
Serial peripheral status register (SPSR)
Serial peripheral data I/O register (SPDR)

Serial Peripheral Control Register (SPCR)

Bits 0 and 1 of the SPCR program the SPI master bit rate. With bits 0 and 1 set to 0, SCK runs at the internal processor clock/2. This means that SCK operates at one quarter of the microcontroller XTAL frequency.

Bit 2 determines the phase relationship between the clock transmitted at SCK and the data appearing on the MISO terminal. If a 0 is placed in bit 3, SCK idles low. This is the correct condition for the TLV1549. A 1 in bit 6 of the SPCR enables the SPI. A 0 in bit 6 disables the SPI. A 1 in bit 4 (MSTR) confers the status of master to the microcontroller.

Serial Peripheral Status Register (SPSR)

The most important bit of the SPSR is bit 7 (SPIF). When set to 1, it indicates that a data transfer between the TLV1549 and the microcontroller has been completed. The SPIF bit is automatically cleared when the SPSR is read and the SPI data register is accessed.

Serial Peripheral Data I/O Register (SPDR)

When the SPIF bit of the SPSR is 1, the SPDR contains the received byte of information from the converter. The contents of SPDR can then be read into a suitable register or location.

Program Listing

The program listing for the TLV1549-to-MC68HC705 interface shown in Figure 2 is included in the following section. COUNT has been set to 2; this ensures that two conversions are performed each time the ADC subroutine is used. The first conversion flushes out potentially erroneous data from the converter output registers. For test purposes, the main program simply performs continuous repeat jumps to the ADC subroutine.

The SPI expects the most significant bit of each received byte to arrive first which is compatible with the order of the TLV1549 output bit stream. This means that no reformatting of the most significant bit of the 10-bit conversion result is required. However, the least significant byte does need to be shifted right by 6 bits.

Program Listing for the TLV1549-to-MC68HC705 Interface

```
              * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
              *                                                           *
              *        TLV1549 - MC68HC705C8 Interface Program            *
              *                                                           *
              *   This program contains a subroutine ADC which reads      *
              *   the serial data from two conversions of the TLV1549     *
              *   and places the MSByte in address 50H and the LSByte     *
              *   in address 51H.                                         *
              *   The data from the first conversion(potentially          *
              *   erroneous) is overwritten by the result from the        *
              *   second conversion.                                      *
              *                                                           *
              * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
000A          SPCR     EQU 0AH        * * * * * * * * * * * * * * * * * * *
000B          SPSR     EQU 0BH        *                                   *
000C          SPDR     EQU 0CH        *                                   *
0002          PORTC    EQU 02H        * Names, Peripheral, and            *
0006          DDRC     EQU 06H        * Control Registers                 *
0011          SCDAT    EQU 11H        *                                   *
000E          SCCR1    EQU 0EH        *                                   *
000F          SCCR2    EQU 0FH        *                                   *
0010          SCSR     EQU 10H        * * * * * * * * * * * * * * * * * * *
0050          MSBYTE   EQU 50H        * * * * * * * * * * * * * * * * * * *
0051          LSBYTE   EQU 51H        * Names working RAM addresses       *
1FFE          RESETH   EQU 1FFEH      *                                   *
1FFF          RESETL   EQU 1FFFH      *                                   *
0052          COUNT    EQU 52H        * * * * * * * * * * * * * * * * * * *
0160                   ORG 160H       Start Program at 160H
0160  A601             LDA #01H
0162  C71FFE           STA RESETH     Load Reset Vector High Byte
0165  A660             LDA #60H
0167  C71FFF           STA RESETL     Load Reset Vector Low Byte
016A  CD016F  START    JSR ADC
016D  20FB             BRA START
016F  1E06    ADC      BSET 7, DDRC
0171  A602             LDA #02H
0173  B752             STA COUNT
0175  A610    CONVERT  LDA #10H
0177  1E02    CSHIGH   BSET 7, PORTC  Set Port C bit 7 (TLV1549 CS) high
0179  4A               DECA
017A  26FB             BNE CSHIGH
017C  1F02             BCLR 7, PORTC  Reset TLV1549 CS (Low)
017E  A650             LDA #50H       Load accumulator with 50H
0180  B70A             STA SPCR       Load SPI control register
0182  A600             LDA #00H       Load dummy data into accumulator
0184  B70C             STA SPDR       Receive SPI data
0186  0F0BFD  HBYTE    BRCLR 7, SPSR, HBYTE
0189  B60C             LDA SPDR
018B  B750             STA MSBYTE     Put MSBYTE in Location 50
018D  A600             LDA #00H       Load dummy data into accumulator
018F  B70C             STA SPDR       Receive SPI data
0191  0F00FD  LBYTE    BRCLR 7, 0B, LBYTE
0194  B60C             LDA SPDR
0196  B751             STA LSBYTE     Put LSBYTE in Location 51
0198  3A52             DEC COUNT
019A  B652             LDA COUNT
019C  26D7             BNE CONVERT    If COUNT = 1, do another conversion
019E  A606             LDA #06H       * * * * * * * * * * * * * * * * * * *
01A0  98      FORMAT   CLC            *                                   *
01A1  3651             ROR LSBYTE     *      Reformats LSBYTE             *
01A3  4A               DECA           *                                   *
01A4  26FA             BNE FORMAT     * * * * * * * * * * * * * * * * * * *
01A6  81               RTS
01A7                   END
```

TLV1549-TO-TMS7000 INTERFACE

Microcontroller Features

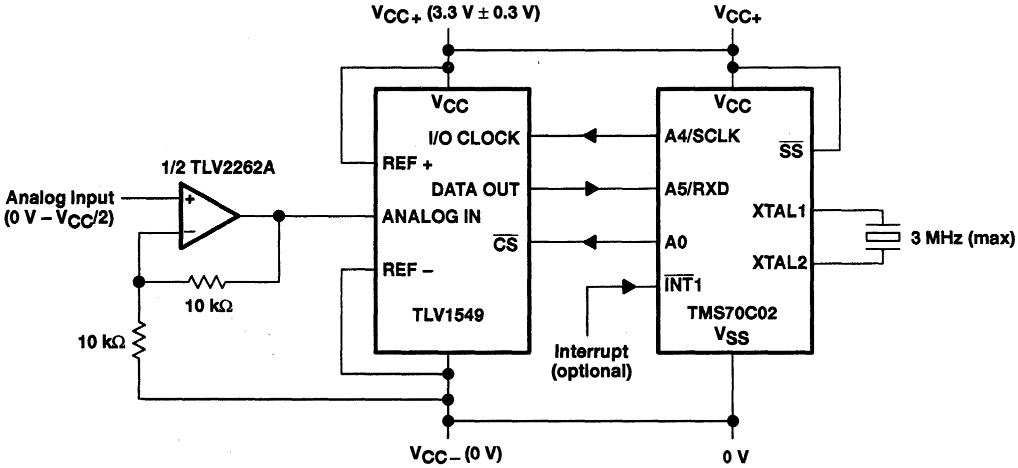
The entire range of TMS7000 microcontrollers can be operated with a 3-V supply. However, the maximum crystal frequency they will tolerate at this supply voltage (over the full temperature range) is 3 MHz. The inherently longer instruction cycle times that this yields should be taken into account when deciding how many software delay loops are necessary to produce the required delay.

Within the family of TMS7000 microcontrollers, three types are available that have a serial port: TMS70Cx2, TMS77C82, and TMS70Cx8. This application report refers to the TMS70Cx2, but any one of these three types could be chosen to efficiently implement a serial interface to the TLV1549.

Three modes of serial communication are available for the serial port: asynchronous mode, isosynchronous mode, and the serial I/O mode. The most suitable of these for interfacing the TMS70Cx2 to the TLV1549 is the serial I/O mode.

Interface Circuit

The TLV1549-to-TMS70C02 interface circuit is shown in Figure 4. The chip select ($\overline{CS}$) of the TLV1549 is controlled by the output from A0 (bit 0 of peripheral port A).



NOTE: Maximum I/O clock frequency = microcontroller crystal frequency/8

Figure 4. TLV1549 10-Bit Serial Out ADC-to-TMS70C02 Microcontroller Interface

Serial I/O Mode

Four peripheral registers are used to set up and control the serial I/O mode of the microcontroller:

Serial mode register (SMODE)
Serial control register 0 (SCTL0)
Serial control register 1 (SCTL1)
Serial port status register (SSTAT)

The contents of the SMODE register determine the data format and type of communication mode (serial I/O for example). In the serial I/O mode, the frame format of each character is five to eight data bits followed by a stop bit. Setting the number of bits to eight can simplify the software necessary to implement the interface.

SCTL0 enables either transmit or receive communication. SCTL1 determines the source of SCLK and programs the frequency of SCLK.

SSTAT is a read-only register that is used for checking the status of the serial port. Bit 1 (RXRDY) of SSTAT is 0 when the receive buffer (RXBUF) is empty and 1 when RXBUF is full.

Provision of TLV1549 Chip Select ($\overline{CS}$)

On power-up and/or system reset, the TLV1549 chip-select terminal ($\overline{CS}$) should be initialized to a high level. To provide this, one of the bidirectional peripheral port bits can be programmed as an output and set to a 1 for a period of at least 21 µs. This period is provided by a delay loop at the beginning of the ADC subroutine. The number of times the loop is excuted in order to achieve at least 21 µs is dependent on the clock frequency of the microcontroller and the number of instruction cycles contained within the delay loop. The example program listing shown in the section program listing for TLV1549-to-TMS70C02 microcontroller interface executes the loop 16 times, but the loop can be executed less times to optimize the conversion throughput rate.

On completion of this delay loop, the particular peripheral port bit is reset to 0, and the converter is now ready to send out data from the previously performed conversion.

Data Reformatting and Storage

After RXBUF is checked to verify it is full, its contents can be read to a suitable register for subsequent access and processing. In the case of the 10-bit conversion result from the TLV1549, two successive bytes of data are received and each are placed in RXBUF to be read consecutively into two convenient memory locations.

The TLV1549 sends the digital result of each conversion with the most significant bit first and the least significant bit last. This is the reverse of the order that the TMS70C02 expects. A few software instructions are therefore inserted near the end of the conversion subroutine that reformat the data into the correct order for interpretation by the microcontroller.

Other Software Considerations

The subroutine that services the TLV1549 conversion should be located in a convenient area of memory that is compatible with the rest of the system. For example, all serial port versions of the TMS7000 family have 8K bytes of EPROM. This EPROM is located between addresses E000H (hex) and FFFFH. A converter subroutine start address at the midpoint of this EPROM memory space may be convenient in that it leaves the first half of this space for the location of the main program. The example program listing in the section Program Listing for TLV1549-to-TMS70C02 Microcontroller Interface uses a start location of F006 which is convenient for the emulation system it was developed on.

On system reset, the stack pointer is at location 0001H. In programs that include nested subroutines where the number of RAM locations taken up by the stack becomes large, the stack can interfere with other useful or even critical RAM locations. It is therefore prudent to reposition the stack pointer, immediately after reset, at a higher address in RAM such as 0060H. This allows the stack plenty of room to grow and avoids interference with lower address RAM locations.

Software Listing

The following program listing reads in the results of two 10-bit conversions from the TLV1549. The software routine ADC actually reads in the results from N conversions, where N is the contents of the register COUNT. The first conversion in a sequence of conversions may be erroneous because the data received is derived from a previous (probably invalid) sample of the analog signal. It is often useful to flush out this first spurious reading before receiving a second valid conversion result. The setting of the contents of COUNT is performed within the main program and should normally be set to a minimum of two.

Program Listing for TLV1549-to-TMS70C02 Microcontroller Interface

```
                  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
                  *            TLV1549 - TMS70C02 Interface Program             *
                  *                                                             *
                  *     This program contains a subroutine ADC which reads in   *
                  *     the serial data from two conversions of the TLV1549. The *
                  *     data (potentially erroneous) from the first conversion  *
                  *     is overwritten by the data from the second conversion.  *
                  *     The most significant byte is placed in register 16. The *
                  *     least significant byte is placed in register 17.        *
                  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
           0004   APORT   EQU P4        * * * * * * * * * * * * * * * * * * * * *
           0005   ADDR    EQU P5        *                                       *
           0014   SMODE   EQU P20       *                                       *
           0015   SCTL0   EQU P21       *                                       *
           0016   SSTAT   EQU P22       *   Name Peripheral Registers           *
           0018   SCTL1   EQU P24       *                                       *
           0019   RXBUF   EQU P25       *                                       *
           001A   TXBUF   EQU P26       *                                       *
           0009   COUNT   EQU R9        *   Name Count and Result Registers     *
           0010   MSBYTE  EQU R16       *                                       *
           0011   LSBYTE  EQU R17       * * * * * * * * * * * * * * * * * * * * *
      F006                AORG >F006    Set start address of program
      F006  52    START   MOV %>60,B    Set stack register
      F007  60
      F008  0D            LDSP
      F009  A2            MOVP %>11,ADDR   Set up Port A Data Direction Register
      F00A  11
      F00B  05
      F00C  A2            MOVP %>0C,SMODE  Set up Serial Mode Register
      F00D  0C
      F00E  14
      F00F  72            MOV %>02,COUNT   Set COUNT = 2
      F010  02
      F011  09
      F012  8E            CALL @ADC        Call Subroutine ADC
      F013 F017
      F015  E0            JMP START        On return from Subroutine ADC, jump to START
      F016  EF
      F017  22    ADC     MOV %>03,A       Put 03 in register A
      F018  03
      F019  A2    CSHIGH  MOVP %>01,APORT  TLV1549 Chip Select goes high
      F01A  01
      F01B  04
      F01C  B2            DEC A            Decrement the contents of Register A by 1
      F01D  E6            JNZ CSHIGH       and jump to CSHIGH if result is not zero
      F01E  FA
      F01F  A2            MOVP %>00,APORT  TLV1549 Chip Select goes low
      F020  00
      F021  04
      F022  A2            MOVP %>16,SCTL0  Set up Serial Control Register 0
      F023  16
      F024  15
      F025  A2            MOVP %>C0,SCTL1  Set up Serial Control Register 1
      F026  C0
      F027  18
      F028  80    LABEL1  MOVP SSTAT,A     Put contents of Serial Status Register in A
      F029  16
      F02A  26            BTJO %>2,A,LABEL2 If bit 1 of A is 1, jump to LABEL2
      F02B  02
      F02C  02
      F02D  E0            JMP LABEL1       and if not, jump to LABEL1
      F02E  F9
      F02F  80    LABEL2  MOVP RXBUF,A     Put contents of RXBUF (MSByte) in A
      F030  19
      F031  D0            MOV A,R10        Put contents of A into Register 10
      F032  0A
      F033  A2            MOVP %>16,SCTL0  Set up Serial Control Register 0
      F034  16
      F035  15
```

```
0043 F036   A2              MOVP %>C0,SCTL1  Set up Serial Control Register 1
     F037   C0
     F038   18
0044 F039   80      LABEL3  MOVP SSTAT,A     Put contents of Serial Status Register in A
     F03A   16
0045 F03B   26              BTJO %>2,A,LABEL4  If bit 1 of A is 1, jump to LABEL1
     F03C   02
     F03D   02
0046 F03E   E0              JMP LABEL3       and if not, jump to LABEL3
     F03F   F9
0047 F040   80      LABEL4  MOVP RXBUF,A     Put contents of RXBUF (LSByte) in A
     F041   19
0048 F042   D0              MOV A,R11        Put contents of A in Register 11
     F043   0B
0049 F044   D2              DEC COUNT        (COUNT) - 1
     F045   09
0050 F046   E6              JNZ ADC          If COUNT is not zero do another conversion
     F047   CF
0051 F048   B0              CLRC             clear carry bit
0052 F049   DD              RRC R11          * * * * * * * * * * * * * * * * * * * * *
     F04A   0B                               *                                       *
0053 F04B   E7              JNC LSBIT0       *  Reformats Least Significant Byte     *
     F04C   03                               *                                       *
0054 F04D   74              OR %>2,R11       * * * * * * * * * * * * * * * * * * * * *
     F04E   02
     F04F   0B
0055 F050   42      LSBIT0  MOV R11,LSBYTE   Put reformatted LSByte in LSBYTE
     F051   0B
     F052   11
0056 F053   D5              CLR R12          clear register 12
     F054   0C
0057 F055   D5              CLR R14          and register 14
     F056   0E
0058 F057   22              MOV %>8,A        Set contents of A to 8
     F058   08
0059 F059   42              MOV R10,R12      Put contents of register 10 in register 12
     F05A   0A
     F05B   0C
0060 F05C   B0      FORMAT CLRC              * * * * * * * * * * * * * * * * * * * * *
0061 F05D   DD              RRC R12          *                                       *
     F05E   0C                               *                                       *
0062 F05F   DF              RLC R14          *  Reformats Most Significant Byte      *
     F060   0E                               *                                       *
0063 F061   B2              DEC A            *                                       *
0064 F062   E6              JNZ FORMAT       * * * * * * * * * * * * * * * * * * * * *
     F063   F8
0065 F064   42              MOV R14,MSBYTE   Put reformatted MSByte into MSBYTE
     F065   0E
     F066   10
0066 F067   0A              RETS             Return from subroutine ADC
0067 FFFE                   AORG >FFFE       Configure Reset vector
0068 FFFE F006              DATA START       to point to START
0069                        END
```

TLV1549-TO-80C51-L INTERFACE

Microcontroller Features

The 80C51-L is the 3.3-V supply version of the 80C51 family of microcontrollers. Various 3.3-V supply versions of the 80C51 architecture are available from different manufacturers. Individual data sheets should be consulted to establish at which maximum crystal frequency each specific device type can operate.

As indicated for the previously described interfaces, the most suitable method of receiving the serial output from the TLV1549 is to configure the serial port of the microcontroller to perform like an 8-bit shift register. The same is true for the 80C51-L.

Serial I/O Mode 0

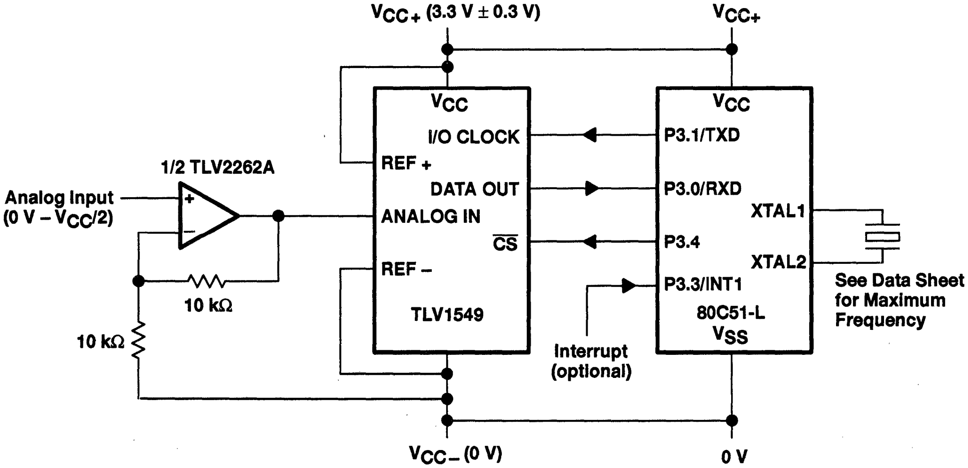
The type of serial communication to and from the 80C51-L is determined by the data inserted into the serial port control register (SCON). The contents of the most significant bits of SCON (bits 7 and 6) determine the operating mode (modes 0, 1, 2, and 3) of the serial port.

Mode 0 is the shift register mode and is programmed by placing a 0 in each of bits 7 and 6 of the SCON. Bit 4 (REN) of the SCON is the receive enable bit. This bit is set to 1, while bit 1 (RI) of the SCON is 0, to receive serial data. In this configuration, data is received at bit 0 of port 3 (P3.0). The synchronizing signal for clocking in this data is output at TXD, which is bit 1 of port 3 (P3.1).

When configured for mode 0, eight bits are received with no trailing stop bit for each enabling of serial reception. The data is received with the least significant bit expected first, the reverse of the order in which the TLV1549 serial data arrives. Reformatting of the received data is therefore necessary.

Interface Circuit

Figure 5 shows the interconnections necessary to implement the interface of the TLV1549 to the 80C51-L microcontroller. $\overline{CS}$ of the TLV1549 is driven by bit 4 of port 3 (P3.4) of the 80C51-L.



NOTE: I/O clock frequency = microcontroller clock frequency/12

Figure 5. TLV1549 10-Bit Serial Out ADC-to-80C51-L Microcontroller Interface

Software Listing

Similar to the previously described program listings, the following listing contains the subroutine ADC that reads into the 80C51-L ten bits of serial data resulting from a single conversion of the TLV1549. The number of consecutive conversions performed for each jump to subroutine ADC is equal to the number placed in COUNT. The result of each conversion is overwritten by that of the next conversion in the sequence.

Program Listing for the TLV1549-to-80C51-L Interface

```
LOC   OBJ     SOURCE
              ;* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
              ;*                                                              *
              ;*          TLV1549 - 80C51-L Interface Program                  *
              ;*                                                              *
              ;*    This program contains a subroutine ADC which reads         *
              ;*    in the serial data from the TLV1549 10-bit ADC             *
              ;*    and places the most significant byte in address 20H        *
              ;*    and least significant byte in address 21H                  *
              ;*                                                              *
              ;* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

0020          MSBYTE    EQU 20H         ;* * * * * * * * * * * * * * * * * * * *
0021          LSBYTE    EQU 21H         ;*     Name data destinations          *
REG           COUNT     EQU R3          ;*     and COUNT register              *
                                        ;* * * * * * * * * * * * * * * * * * * *
0022                    ORG 22H         ;Set start address
0022  7B02    START:    MOV COUNT, #02H ;Set COUNT=2 (Do 2 conversions)
0024  020029            JMP ADC         ;Jump to subroutine ADC
0027  80F9              JMP START       ;Repeat above again
0029  D2B4    ADC:      SETB P3.4       ;* * * * * * * * * * * * * * * * * * * *
002B  7410              MOV A, #10H     ;*  Set Port3 (bit 4) high             *
002D  14      DELAY:    DEC A           ;* (Sets CS of TLV1549 high)           *
002E  70FD              JNZ DELAY       :* * * * * * * * * * * * * * * * * * * *
0030  C2B4              CLR P3.4
0032  759810            MOV SCON, #10H
0035  3098FD  LABEL1:   JNB SCON.0, LABEL1      ;Read in
0038  C298              CLR SCON.0              ;most significant
003A  A899              MOV R0,SBUF             ;byte, place in R0
003C  3098FD  LABEL2:   JNB SCON.0, LABEL2      ;Read in
003F  C29C              CLR SCON.4              ;least significant
0041  C298              CLR SCON.0              ;byte,
0043  A999              MOV R1, SBUF            ;place in R1
0045  1B                DEC COUNT       ;COUNT-1
0046  EB                MOV A, COUNT    ;
0047  70E0              JNZ ADC         ;If COUNT not = 0,
                                        ;do another conversion
0049  7C08              MOV R4, #08H    ;Put 08H in R4
004B  AA00              MOV R2, 00H
004D  C3      LOOP:     CLR C           :* * * * * * * * * * * * * * * * * * * *
004E  E8                MOV A, R0       ;*                                     *
004F  13                RRC A           ;*                                     *
0050  F8                MOV R0, A       ;*        Reformats MSByte             *
0051  EA                MOV A, R2       ;*                                     *
0052  33                RLC A           ;*                                     *
0053  FA                MOV R2, A       ;*                                     *
0054  1C                DEC R4          ;*                                     *
0055  EC                MOV A, R4       ;*                                     *
0056  70F5              JNZ LOOP        ;* * * * * * * * * * * * * * * * * * * *
0058  EA                MOV A, R2       ;
0059  F520              MOV 20H, A      ;
005B  E9                MOV A, R1       ;* * * * * * * * * * * * * * * * * * * *
005C  13                RRC A           ;*                                     *
005D  F521              MOV 21H, A      ;*        Reformats LSByte             *
005F  9209              MOV 21H.1, C    ;*                                     *
0061  C20F              CLR 21H.7       ;* * * * * * * * * * * * * * * * * * * *
0063  22                RET             ;Return from subroutine
                        END
```

ANALOG CONSIDERATIONS

Analog Reference for the TLV1549

The REF+ terminal of the TLV1549 can be directly connected to the V_{CC} rail of the device. This produces accurate results for analog input signals right up to the supply rail. However, if the operational amplifier driving the input is supplied from the same single supply as the ADC, the output of the operational amplifier could possibly be nonlinear up to the rail voltage. If this is a concern, a lower reference voltage as shown in Figure 6 can be applied to REF+ providing more headroom for the amplifier.

The output of the TL2262A 3-V single-supply operational amplifier can swing to within 10 mV of its positive supply rail. This effectively loses only two least significant bits (LSBs) off the top of the digital output range of the TLV1549 when both the amplifier and ADC are powered from the same 3-V supply. The circuit shown in Figure 6 provides a 2.5-V reference to the converter, which restores those bits to the digital output of the TLV1549 while the maximum analog input swing is reduced to 2.5 V.

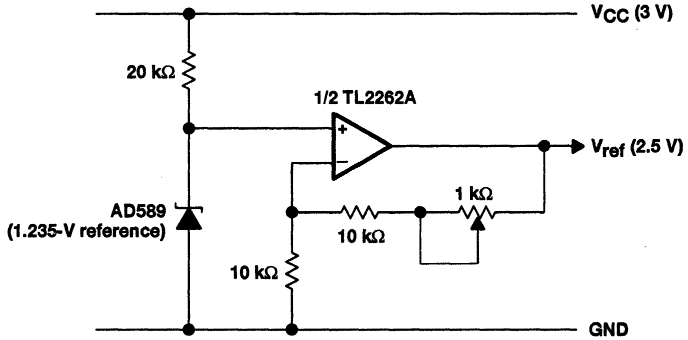


Figure 6. User Adjustable 2.5-V Reference Circuit

PCB Layout

As with all precision analog components, care should be taken in laying out the printed-circuit board (PCB) on which the TLV1549 and chosen microcontroller are placed. The interaction between digital and analog signal paths should be minimized by keeping them as far apart as is physically possible within the constraints of the dimensions of the PCB.

Grounding and Decoupling

Each supply terminal to both the TLV1549 and the microcontroller should be decoupled by a ceramic capacitor of approximately 100 nF in value, situated close to the terminal of the device. Digital and analog ground return paths should be kept separate to prevent any digitally generated currents from corrupting the analog signal.

APPENDIX A

References

MC68HC705C8 Technical Data Manual (1990)	Motorola
M68HC05 Applications Guide	Motorola
TLV1549 Data Sheet	Texas Instruments Incorporated
TMS7000 Family Data Manual (1991)	Texas Instruments Incorporated
Embedded Microcontrollers and Processors Vol. 1	Intel Corporation

TLC2932

Phase-Locked-Loop Building Block With Analog Voltage-Controlled Oscillator and Phase Frequency Detector

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1 INTRODUCTION

The TLC2932IPW integrated circuit (IC) contains a voltage-controlled oscillator (VCO) and a phase frequency detector (PFD) for use in phase-locked-loop (PLL) circuit blocks. A standalone PLL circuit can be designed with the addition of an external frequency divider and a loop filter.

Because the on-chip analog VCO has a wide usable lock frequency range and can cover a wide range of frequencies (11 MHz–50 MHz) previously unavailable, many new applications are now possible. A stable clock output can be achieved with only one external resistor required for the oscillator. The on-chip PFD uses a widely accepted edge-triggered charge pump circuit. The TLC2932IPW is designed for use as clock frequency generator blocks in digital signal processor (DSP) applications involving video where many video signal frequency bands are possible. Refer to the TLC2932 data sheet (SLAS097) for other features.

For the proper usage of the TLC2932IPW, basic concepts relating to conventional PLL blocks and examples based on experimental results are described in this application report. In the design of a high performance PLL circuit, the parameters of the peripheral circuits such as the counter frequency division setting and the loop filter parameters are determined by the application. The fundamentals needed to produce a high performance PLL are discussed, and the VCO, PFD, frequency divider, and loop filter are examined individually and then as a group.

2 THEORY OF AN ANALOG PHASE-LOCKED LOOP (PLL)

2.1 Overview

A phase-locked loop is a feedback controlled circuit that maintains a constant phase difference between a reference signal and an oscillator output signal.

2.2 General Operation of a PLL

Figure 2–1 shows a basic block diagram of a PLL. A phase frequency detector compares the phase of the VCO output frequency, f_{osc}, with the phase of a reference signal frequency, f_{ref}. A phase detector output pulse is generated in proportion to that phase difference. This pulse is smoothed by passing it through a loop filter. The resulting dc component is used as the input voltage for controlling the VCO. The output of the VCO, f_{osc}, is fed back to the phase frequency detector input for comparison which in turn controls the VCO oscillating frequency to minimize the phase difference. Therefore, both frequency and phase are made the same, i.e., $f_{osc} = f_{ref}$ and $\theta_{osc} = \theta_{ref}$, such that the phase and frequency of the VCO and the reference signal source are in a locked state.

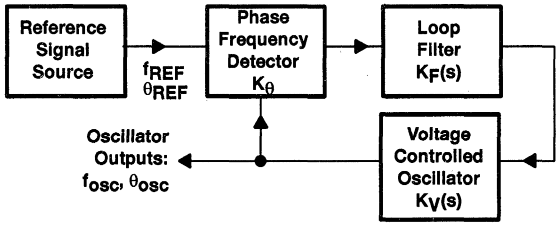


Figure 2–1. Basic PLL Block Diagram

Therefore, the PLL is a negative feedback circuit which compares the current value to a reference value to make the difference as close to zero as possible.

2.2.1 Analysis of a PLL as a Feedback Control System

An analysis can be performed using the linearized block diagram in Figure 2–2.

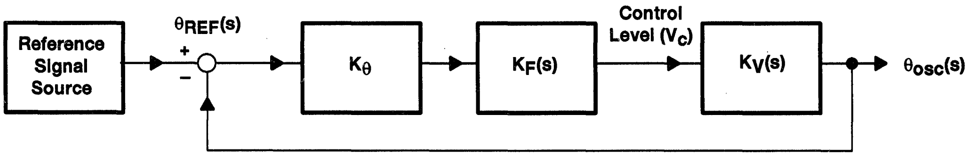


Figure 2–2. Linearized PLL Block Diagram

The parameters in Figure 2–2 are defined as follows:

K_θ = gain of the phase frequency detector (V/rad)
K_F = transfer function of the loop filter (V/V)
V_c = VCO control level
V_c = VCO control level
s = Laplace variable

Using a Laplace transform, the closed-loop transfer function can be expressed as:

$$\frac{\theta_{osc}(s)}{\theta_{REF}(s)} = \frac{K_\theta \times K_F(s) \times K_V(s)}{1 + K_\theta \times K_F(s) \times K_V(s)} = W(s) \tag{2.1}$$

The VCO transform gain, K_V, is a function of time. Since phase is the time integral of frequency, the gain can be expressed as follows:

$$K_V(s) = \frac{K_V}{s} \tag{2.2}$$

The phase frequency detector gain is assumed to not to be a function of frequency.

From equation 2.1 and equation 2.2

$$W(s) = \frac{K_{\theta} \times K_F(s) \times K_V}{s + K_{\theta} \times K_F(s) \times K_V} \tag{2.3}$$

This equation is the general linear transfer function for a PLL.

The PLL has become widely used as a frequency synthesizer by generating frequencies from a single reference signal source such as a crystal oscillator.

Consider the operation of the PLL frequency synthesizer in Figure 2–3.

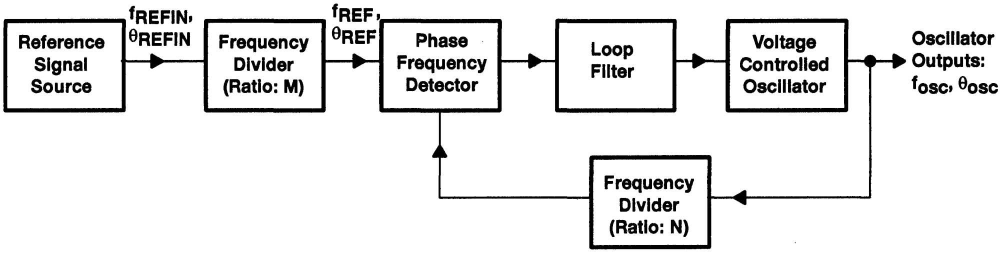


Figure 2–3. PLL Frequency Synthesizer Block Diagram

Since the signal from the reference signal source is used to generate the desired frequency in a frequency synthesizer, only frequencies at multiples of the reference frequency can be obtained.

The phase frequency detector compares the signal from the 1/N frequency divider which divides the output signal of the VCO, and the signal from the 1/M frequency divider which divides the output signal of the reference signal source, and controls the VCO frequency in such a way so that both frequency and phase are the same.

Therefore $\frac{f_{refin}}{M} = \frac{f_{osc}}{N}$ (2.4)

and the oscillating frequency, $f_{osc} = f_{refin} \times \frac{N}{M}$ (2.5)

The closed-loop transfer function of the PLL in equation 2.1 can now be considered. If 1/M and 1/N frequency dividers are inserted into the block diagram of Figure 2–3, then Figure 2–2 becomes Figure 2–4.

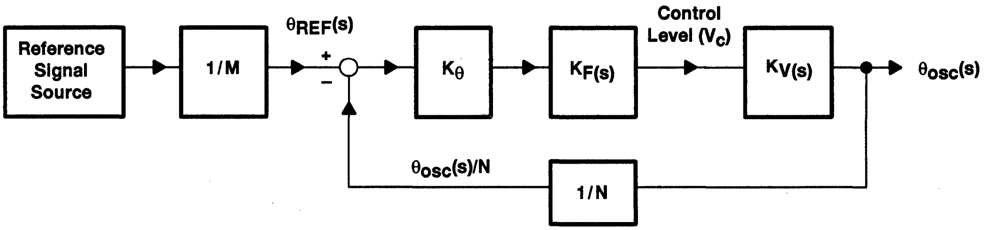


Figure 2–4. Linearized PLL Frequency Synthesizer Block Diagram

Thus, the closed-loop transfer function can be expressed by the following equation:

$$W(s) = \frac{K_{\theta} \times K_F(s) \times K_V}{s + \frac{K_{\theta} \times K_F(s) \times K_V}{N}} \tag{2.6}$$

If the multiplication parameter N is set to 1 in equation 2.6, it becomes equation 2.3.

In this application report, equation 2.6 is used as the closed-loop transfer function for the PLL.

From equations 2.3 and 2.6, the closed-loop transfer function of the PLL is heavily dependent on the characteristics of the loop filter which is discussed later in this application report.

2.2.2 Definitions

2.2.2.1 Free Running Frequency

The free oscillating frequency of the VCO when it is in an unlocked state is called the free running frequency.

2.2.2.2 Hold-In Range (Lock Range) and Lock-In Range (Capture Range)

When the PLL is in the phase-locked state, the frequency range in which the frequency of the input reference signal, f_{REF}, can slowly be pulled away from the free running frequency of the VCO but still maintain the phase-locked condition is called the hold-in range or lock range. When the PLL is not in the phase-locked state, if the frequency of the input signal, f_{REF}, slowly approaches the free running frequency of the VCO, the frequency range in which the input signal becomes phase-locked is called the lock-in range or capture range.

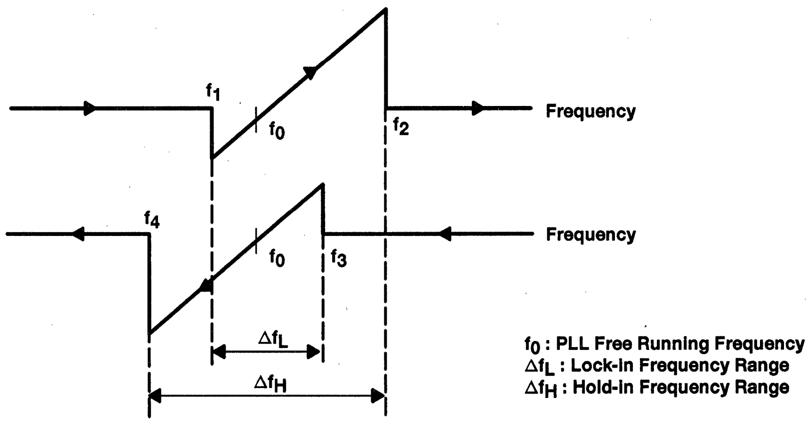


Figure 2–5. Concept Behind Hold-In Range and Lock-In Range

Referring to the conceptual diagram in Figure 2–5, if the input signal frequeny is increased slowly from a very low frequency not phase-locked to the VCO free running frequency, phase-lock occurs at frequency f_1. If the input signal frequency continually increases, it will pass through the free running frequency and then become unlocked at frequency f_2. Conversely, if the input signal frequency is decreased slowly from a very high frequency not phase-locked to the VCO free running frequency, phase lock occurs at frequency f_3. If the input signal frequency continually increases, it will pass through the free running frequency and the PLL becomes unlocked at frequency f_4. The hold-in range, Δf_H, and lock-in range, Δf_L, can be expressed as the following equations:

$$\Delta f_H = \left(f_2 - f_4\right) \tag{2.7}$$

$$\Delta f_L = \left(f_3 - f_1\right) \tag{2.8}$$

Normally, the relationship of $\Delta f_H > \Delta f_L$ exists.

2.2.2.3 Lock-Up Time (Acquisition Time)

The amount of time required for the loop to phase lock is called lock-up time or acquisition time.

2.3 PLL Functional Blocks

2.3.1 Voltage-Controlled Oscillator (VCO)

The VCO is an oscillator circuit with the following characteristics whose output frequency is controlled by a voltage.

- K_V = VCO gain (rad/V/sec) from Section 2.2.1
- Stable with respect to external disturbances (change in voltage, temperature, etc.)
- Control voltage versus oscillating frequency should ideally be linear
- Frequency adjustment should be simple

Because it is extremely difficult to satisfy all these conditions at the same time, a suitable oscillator should be chosen based on the application.

Oscillators that are typically used include the following:

- Crystal oscillator
- LC oscillator
- CR oscillator

For a VCO utilizing any of the above oscillation techniques, many excellent technical books and articles on VCO circuit design should be used.

2.3.2 Phase Detector Operation and Types

A phase detector detects phase differences between two input signals and produces a voltage based on this phase difference.

Phase detectors can be either analog or digital. For analog, representative devices are ring modulators and multipliers which are also called double balanced mixers. For digital, representative devices are OR-gates, ExOR-gates, RS flip-flops, 3-state buffers, and phase frequency detectors.

Only the digital phase detectors are discussed in this application report.

2.3.2.1 OR-Gate Type Phase Detector

The simplest form of digital type phase detectors is the OR-gate type shown in Figure 2–6(a).

For an OR-gate type phase detector, the output signal duty cycle varies depending on the phase difference, as shown in Figure 2–6(b). Then this output signal is smoothed by an integrator. The resulting output voltage in relation to the phase difference is shown in Figure 2–6(c).

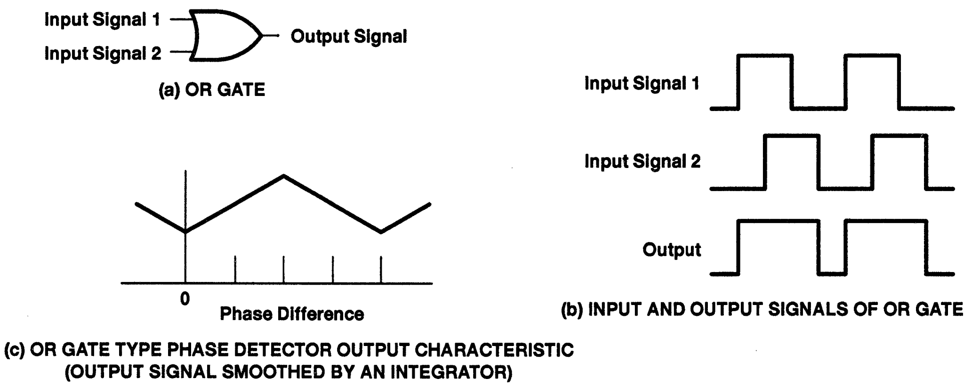
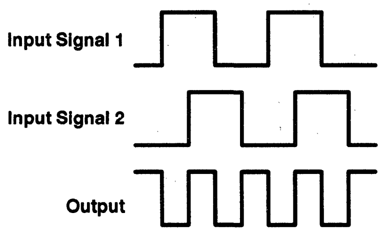


Figure 2–6. OR Gate Type Phase Detector

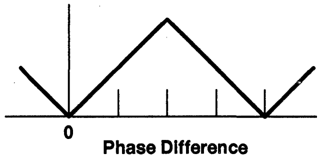
2.3.2.2 ExOR-Gate Type Phase Detector

An ExOR gate phase detector is shown in Figure 2–7(a).

(a) ExOR GATE



(b) ExOR GATE INPUT AND OUTPUT SIGNALS



(c) ExOR GATE TYPE PHASE DETECTOR OUTPUT CHARACTERISTIC (OUTPUT SIGNAL SMOOTHED BY AN INTEGRATOR)

Figure 2–7. ExOR Gate Type Phase Detector

For this type of phase detector, the duty cycle of the output signal varies depending on the phase difference, as shown in Figure 2–7(b). This output signal is also smoothed by an integrator. The resulting output voltage in relation to the phase difference is shown in Figure 2–7(c).

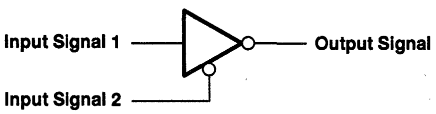
For this ExOR-gate type of phase detector, as compared to an OR-gate type of phase detector, the integrator output signal swings from 0 V to the supply voltage, V_{DD}. Moreover, because the ExOR-gate output frequency is twice that of the OR-gate, the high frequency components are more easily filtered out by the integrator.

However, when using an ExOR-gate as a phase detector, if each input signal duty cycle is not 50%, the output voltage generated from the phase difference does not have acceptable linear characteristics. Therefore, care must be exercised when using this type of phase detector.

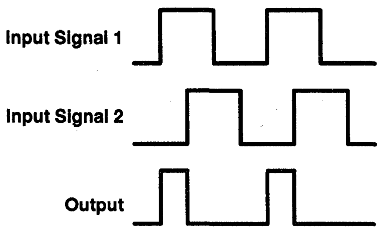
2.3.2.3 3-State Buffer Type Phase Detector

A 3-state buffer phase detector is shown in Figure 2–8(a).

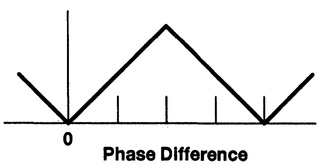
The 3-state buffer phase detector output characteristic, as shown in Figure 2–8(c), is basically the same as ExOR gate phase detector. However, when input signal 2 is high, the output is in a high impedance state as shown in Figure 2–8(b).



(a) 3-STATE BUFFER



(b) 3-STATE BUFFER INPUT AND OUTPUT SIGNALS (OUTPUT HIGH IMPEDANCE WHEN INPUT SIGNAL 2 IS HIGH)



(c) 3-STATE BUFFER TYPE PHASE DETECTOR OUTPUT CHARACTERISTIC (OUTPUT SIGNAL SMOOTHED BY AN INTEGRATOR)

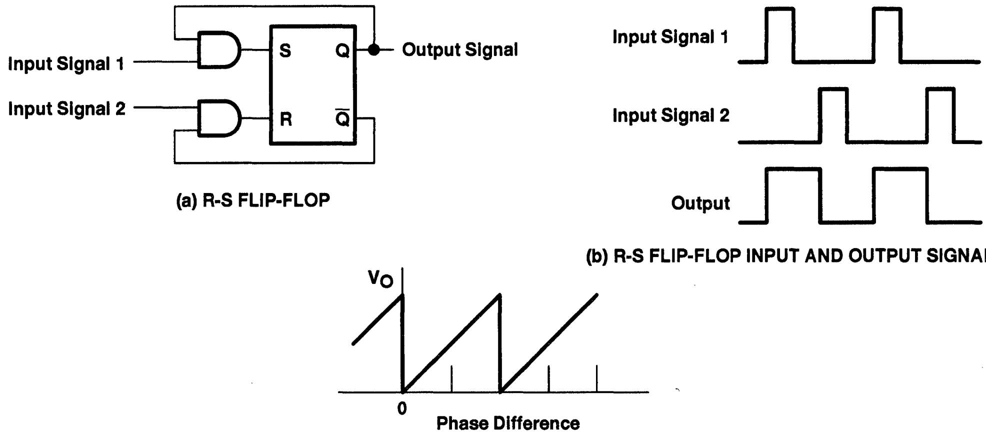
Figure 2–8. 3-State Buffer Type Phase Detector

2.3.2.4 R-S Flip-Flop Type Phase Detector

A R-S flip-flop phase detector is shown in Figure 2–9, and the input and output signals are shown in Figure 2–9(b).

As shown in Figure 2–9(c), a RS flip-flop type phase detector has twice the comparison range of an ExOR gate type phase detector.

The R-S flip-flop type phase detector can be constructed using only an R-S flip flop. The pulse width of the input signal pulses is small, so a SET-RESET error difference do not cause a significant error. This condition can be solved by inserting AND-gates as shown in Figure 2–9(a).



(a) R-S FLIP-FLOP

(b) R-S FLIP-FLOP INPUT AND OUTPUT SIGNALS

(c) R-S FLIP-FLOP TYPE PHASE DETECTOR OUTPUT CHARACTERISTIC (OUTPUT SIGNAL SMOOTHED BY AN INTEGRATOR)

Figure 2–9. RS Flip-Flop Type Phase Detector

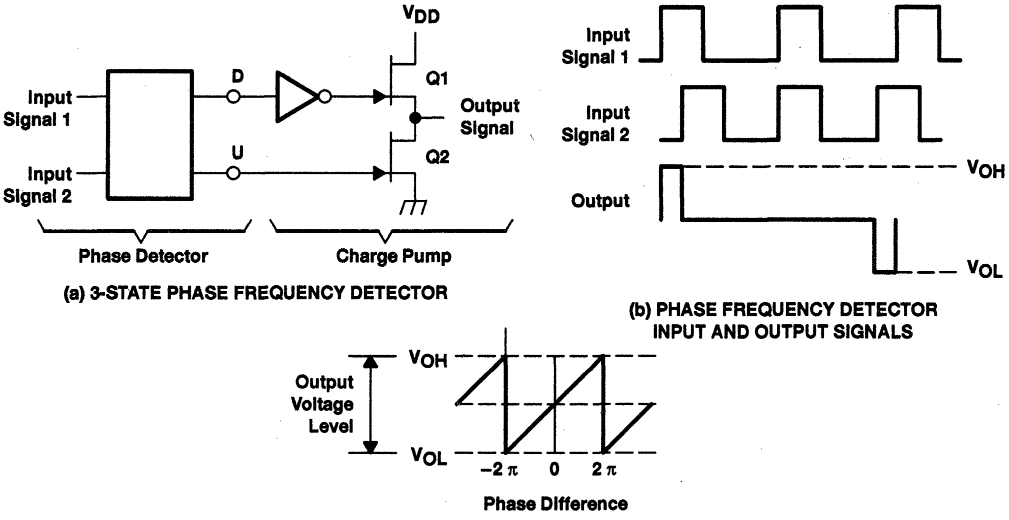
2.3.2.5 Phase Frequency Detector (PFD)

Of the phase detectors currently available, the most commonly used in a PLL is a circuit called a phase frequency detector. Figure 2–10(a) shows an example of a phase frequency detector.

In Figure 2–10(b), when the input signal 2 phase lags that of input signal 1, phase detector output D goes high starting from the rising edge of input signal 1 to the rising edge of input signal 2, that is, during the period of time corresponding to a phase difference between inputs 1 and 2, output D goes high. During this same period, output U stays low. When the phase of input 2 leads that of input 1, output D stays low from the rising edge of input 2 to the rising edge of input 1. During that time, U goes high.

When both inputs 1 and 2 have the same phase, both outputs D and U stay low. Depending on the phase detector outputs D and U, the charge pump MOS transistors are turned on and off resulting in output levels of V_{OH}, V_{OL}, or high impedance. So when D is high and U is low, the MOS transistor Q_1 is on and Q_2 is off, therefore, the output level is V_{OH}. When U is high and D is low, Q_2 is on and Q_1 is off, resulting in the output level of V_{OL}. When both D and U are low, Q_1 and Q_2 are both off and the output becomes high impedance.

In this way, the output level is proportional to the phase difference. The output signal characteristic is shown in Figure 2–10(c).



(a) 3-STATE PHASE FREQUENCY DETECTOR

(b) PHASE FREQUENCY DETECTOR INPUT AND OUTPUT SIGNALS

(c) PHASE FREQUENCY DETECTOR OUTPUT CHARACTERISTIC

Figure 2–10. 3-State Phase Frequency Detector

2.4 Loop Filter

The loop filter smooths the output pulses of the phase detector and the resulting dc component is the VCO input. From the closed-loop transfer function (equation 2.6) obviously the loop filter is very important in determining the characteristics of the PLL response.

Some examples of a loop filter are a lag filter, a lag-lead filter, and an active filter. Among these, the most commonly used are the lag-lead filter and the active filter. For these two filters, the PLL closed loop transfer functions are derived, and design examples for the filter parameters are shown.

2.5 Transfer Function Using a Lag-Lead Filter

First, the lag-lead filter transfer function is derived from Figure 2–11. If a Laplace transform is taken, then

$$\frac{V_O}{V_D} = K_F(s) = \frac{1 + sC1 \times R2}{1 + sC1(R1 + R2)} = \frac{1 + s\tau_2}{1 + s\left(\tau_1 + \tau_r\right)} \tag{2.9}$$

Where

$$\tau_1 = C1 \times R1,\ \tau_2 = C1 \times R2 \tag{2.10}$$

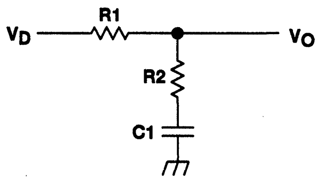


Figure 2–11. Lag-Lead Filter

By substituting equation 2.9 into equation 2.6 and rearranging the terms, the PLL closed-loop transfer function is

$$W(s) = \frac{1 + s\tau_2}{\left\{\left(\tau_1 + \tau_2\right)/K\right\} \times s^2 + \left\{\left(N + K \times \tau_2\right)/(N \times K)\right\} \times s + 1/N} \tag{2.11}$$

Where

$$K_\theta \times K_V = K \tag{2.12}$$

If this equation is further expanded, it becomes

$$W(s) = W_1(s) + W_2(s) = \frac{1}{\left\{\left(\tau_1 + \tau_2\right)/K\right\} \times s^2 + \left\{\left(N + K \times \tau_2\right)/(N \times K)\right\} \times s + 1/N} + \frac{s\tau_2}{\left\{\left(\tau_1 + \tau_2\right)/K\right\} \times s^2 + \left\{\left(N + K \times \tau_2\right)/(N \times K)\right\} \times s + 1/N} \tag{2.13}$$

The general transfer function for a second order system is shown below

$$G(s) = \frac{1}{\left(1/\omega_n^2\right) \times s^2 + \left(2\varsigma/\omega_n\right) \times s + 1} \tag{2.14}$$

Where ω_n is the natural angular frequency and ζ is the damping factor.

If, in equation 2.15 the right hand side first term is designated as $W_1(s)$ and the second term as $W_2(s)$, then $W_1(s)$ is a second order system as in equation 2.14 and $W_2(s)$ is a second order lag with gain of τ_2 multiplied by s.

If $W_1(s)$ is equated to equation 2.14 and the coefficients compared

$$W_1(s) = \frac{1 + s\tau_2}{\left\{\left(\tau_1 + \tau_2\right)/K\right\} \times s^2 + \left\{\left(N + K \times \tau_2\right)/(N \times K)\right\} \times s + 1/N} = \frac{1}{\left(1/\omega_n^2\right) \times s^2 + \left(2\varsigma/\omega_n\right) \times s + 1} \tag{2.15}$$

the following are derived

$$\omega_n = \sqrt{\frac{K}{N\left(\tau_1 + \tau_2\right)}} \tag{2.16}$$

$$\varsigma = \frac{1 + K\tau_2}{2\sqrt{N\left(\tau_1 + \tau_2\right) \times K}} = \frac{\omega_n}{2}\left(\tau_2 + \frac{N}{K}\right) \tag{2.17}$$

Similarly for $W_2(s)$

$$W_2(s) = \frac{s\tau_2}{\left\{\left(\tau_1 + \tau_2\right)/K\right\} \times s^2 + \left\{\left(N + K \times \tau_2\right)/(N \times K)\right\} \times s + 1/N} = \frac{\left(2\zeta/\omega_n - N/K\right) \times s}{\left(1/\omega_n^2\right) \times s^2 + \left(2\zeta/\omega_n\right) \times s + 1} \tag{2.18}$$

Thus, using a lag-lead filter, the PLL closed-loop transfer function becomes

$$W(s) = W_1(s) + W_2(s) = \frac{1 + (2\zeta/\omega_n - N/K) \times s}{\left(1/\omega_n^2\right) \times s^2 + (2\zeta/\omega_n) \times s + 1} \tag{2.19}$$

From the above result, design equations for lag-lead filter parameters are derived.

If $\tau_1 = C1 \times R1$ and $\tau_2 = C2 \times R2$ are substituted into equations 2.16 and 2.17 respectively and solved for R1 and R2, the following equations are derived:

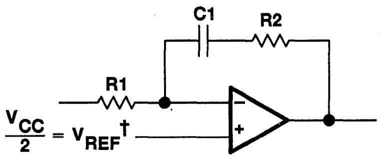
$$R1 = \left(\frac{K}{\omega_n{}^2} \times \frac{1}{N} - \frac{2\zeta}{\omega_n} + \frac{N}{K}\right) \times \frac{1}{C1} \tag{2.20}$$

$$R2 = \left(\frac{2\zeta}{\omega_n} - \frac{N}{K}\right) \times \frac{1}{C1} \tag{2.21}$$

2.6 Transfer Function Using an Active Filter

When using an active filter, the PLL closed-loop transfer function and design equation for filter parameters are derived in the same fashion as in Section 2.5.

First, the Laplace transform is taken and the transfer function of an active filter is derived. Figure 2–12 shows an example of an active filter.



† Voltage used for single ended power supply systems.

Figure 2–12. Active Filter

The transfer function for the active filter is

$$K_F(s) = \frac{1 + sC1 \times R2}{sC1(R1 + R2)} = \frac{1 + s\tau_2}{s\tau_1} \tag{2.22}$$

Where

$$\tau_1 = C1 \times R1 \text{ and } \tau_2 = C1 \times R2 \tag{2.23}$$

From the PLL closed-loop transfer function, if $K_F(s)$ is substituted into equation 2.6 and equation 2.6 is simplified, it becomes

$$W(s) = \frac{1 + s\tau_2}{\left(\tau_1/K\right) \times s^2 + \left(\tau_2/N\right) \times s + 1/N} \tag{2.24}$$

Where

$$K_\theta \times K_V = K \text{ as before.} \tag{2.25}$$

If this equation is expanded further, it becomes

$$W(s) = W_1(s) + W_2(s) = \frac{1}{\left(\tau_1/K\right) \times s^2 + \left(\tau_2/N\right) \times s + 1/N} + \frac{s\tau_2}{\left(\tau_1/K\right) \times s^2 + \left(\tau_2/N\right) \times s + 1/N} \tag{2.26}$$

As shown before, second order lag resonators can be expressed as equation 2.14.

Following the procedure in Section 2.5.

If $W_1(s)$ is equated to equation 2.14

$$W_1(s) = \frac{1}{\left(\tau_1/K\right) \times s^2 + \left(\tau_2/N\right) \times s + 1/N} = \frac{1}{\left(1/\omega_n{}^2\right) \times s^2 + (2\zeta/\omega_n) \times s + 1} \qquad (2.27)$$

the following are derived

$$\omega_n = \sqrt{\frac{K}{N\,\tau_1}} \qquad (2.28)$$

$$\zeta = \frac{\tau_2}{2N} = \sqrt{\tau_1/(N/K)} = \frac{\omega_n}{2}\,\tau_2 \qquad (2.29)$$

Similarly for $W_2(s)$

$$W_2(s) = \frac{s\tau_2}{\left(\tau_1/K\right) \times s^2 + \left(\tau_2/N\right) \times s + 1/N} = \frac{(2\zeta/\omega_n) \times s}{\left(1/\omega_n{}^2\right) \times s^2 + (2\zeta/\omega_n) \times s + 1} \qquad (2.30)$$

Thus for the active filter, the PLL closed-loop transfer function becomes

$$W(s) = W_1(s) + W_2(s) = \frac{1 + (2\zeta/\omega_n) \times s}{\left(1/\omega_n^2\right) \times s^2 + (2\zeta/\omega_n) \times s + 1} \qquad (2.31)$$

From the above result, the design equation for active filter parameters can be derived.

If $\tau_1 = C1 \times R1$ and $\tau_2 = C1 \times R2$ are substituted into equations 2.28 and 2.29 respectively, and solved for R1 and R2, the following two equations are derived:

$$R1 = \frac{K}{\omega_n{}^2} \times \frac{1}{N} \times \frac{1}{C1} \qquad (2.32)$$

$$R2 = \frac{2\zeta}{\omega_n} \times \frac{1}{C1} \qquad (2.33)$$

2.7 General Design Procedures

Based on a PLL step response, the damping factor can be chosen, the natural angular frequency can be evaluated, and the characteristics of response time and relative stability can be examined. For the PLL transfer function in equation 2.31, the step responses of several cases are shown in Figure 2–13. As shown, the smaller the ζ value the larger the ringing, and a large ζ value results in little or no ringing. Also, a larger ω_n results in a faster response time.

The step response for a PLL using an active filter as a loop filter is shown in Figure 2–13. When a passive lag-lead filter is used, if the condition $\omega_n << K/N$ is met for equation 2.19, the step response is similar to the step response shown.

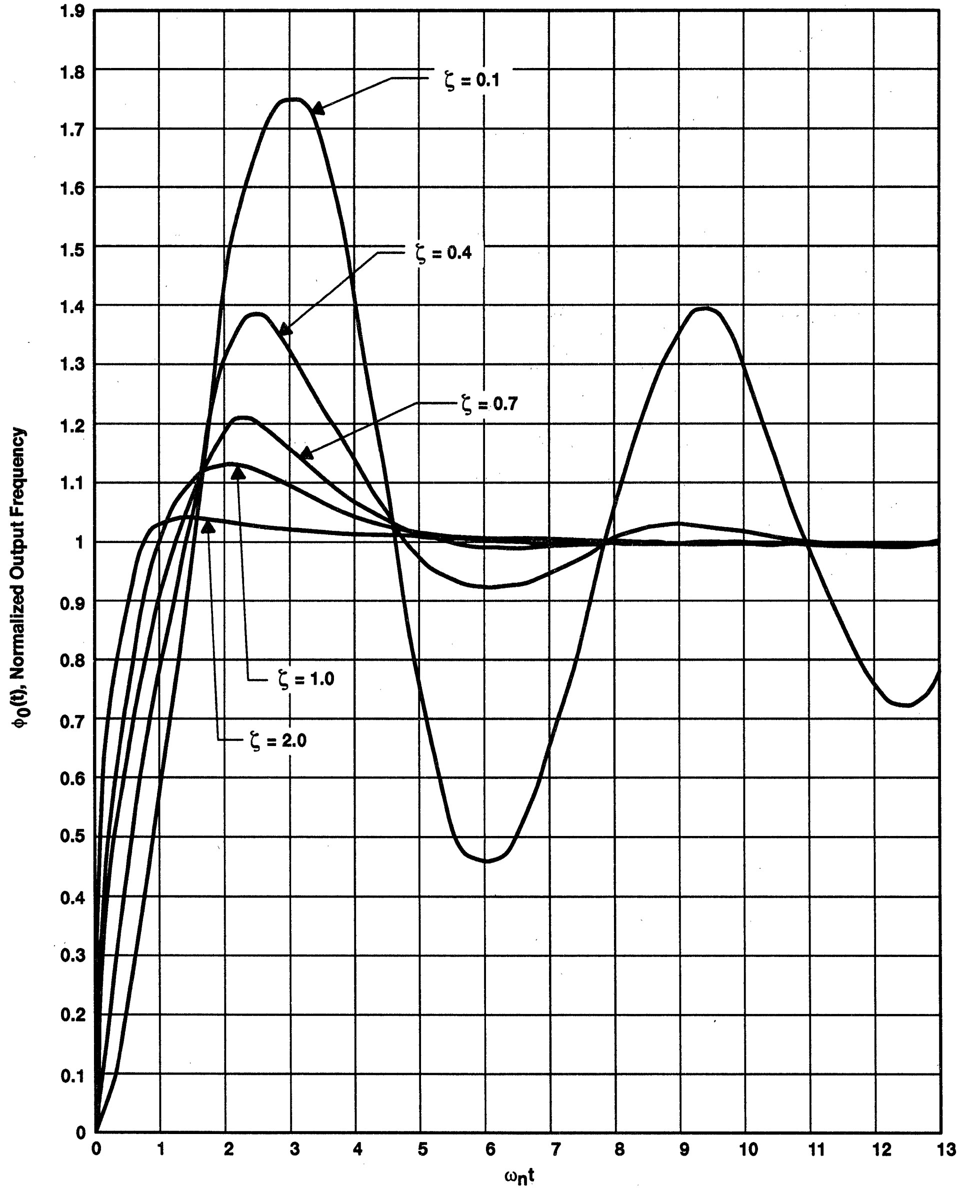


Figure 2–13. PLL Step Response Using the Active Filter in Figure 2–17

To design a PLL system, ζ is selected first. Then from the step response characteristic, the value of $\omega_n t$, at which the response is decayed to within 5% of the final value, is found. Then $\omega_n t$ is divided by the desired lock-up time, t_s, to determine ω_n. The following steps should be followed.

1. ζ is a measure of stability. and usually ζ is selected to be between 0.6 to 0.8.
2. Assume ζ is selected to be 0.7.
3. The value of $\omega_n t$ from the step response characteristic is determined to be 4.5 for response settling within 5%.
4. Lock-up time, t_s, is determined by system requirements.
5. The PLL natural angular frequency, ω_n, is

$$\omega_n = \frac{\omega_n \tau}{t_s} = \frac{4.5}{t_s} \text{ (rad/sec)} \qquad (2.34)$$

   This criterion varies depending on the system application. It is appropriate to pick the natural frequency ($f_n = \omega_n/2\pi$) to be one tenth to one hundredth of the reference frequency of the phase frequency detector.

6. The frequency division ratio is determined from the reference frequency and the desired frequency according to equation 2.5.
7. Determine the VCO gain parameter, K_V. An example of a VCO oscillating frequency characteristic is shown in Figure 2–14.

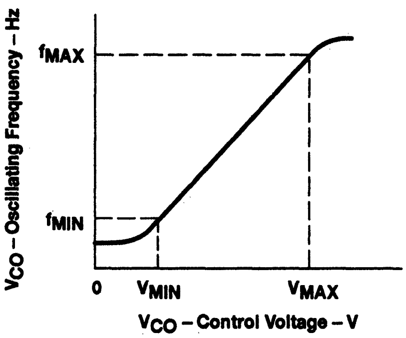


Figure 2–14. VCO Oscillating Frequency Characteristic

From the oscillating frequency characteristic of Figure 2–14, the VCO gain can be determined using the following equation:

$$K_V = \frac{f_{MAX} - f_{MIN}}{V_{MAX} - V_{MIN}} \times 2\pi \text{ [rad/sec/V]} \qquad (2.35)$$

Where

f_{MAX} = maximum frequency at which the linearity of the oscillating frequency versus the VCO control voltage can be maintained.

f_{MIN} = minimum frequency at which the linearity of the oscillating frequency versus the VCO control voltage can be maintained.

V_{MAX} = control voltage at which the VCO oscillating frequency is f_{MAX}

V_{MIN} = control voltage at which the VCO oscillating frequency is f_{MIN}

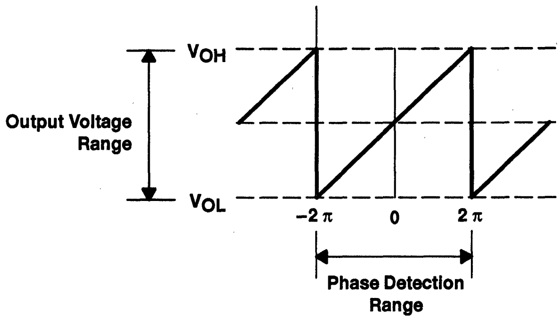


Figure 2–15. Phase Frequency Detector Output Characteristic

8. Determine the phase detector gain parameter, K_θ

   Based on the phase frequency detector output characteristic in Figure 2–15, the phase detector gain can be determined from equation 2.36.

$$K_\theta = \frac{V_{OH} - V_{OL}}{4\pi} \quad [\mathrm{V/rad}] \tag{2.36}$$

   Where
   V_{OH} = maximum output voltage
   V_{OL} = minimum output voltage

   For other types of phase detectors, the phase detector gain can be determined in the same fashion.

9. Filter parameters can be determined by substituting each of the values determined in steps 1 through 8 into the corresponding equations.

   For the lag-lead filter, substituting the desired values of ω_n, ζ, N, and K into equations 2.20 and 2.21, the filter parameters can be determined by choosing an appropriate value for C1.

   For a practical loop filter, a second order lag-lead filter with an additional capacitor C2, as shown in Figure 2–16, to minimize spurious noise at the VCO input should be used.

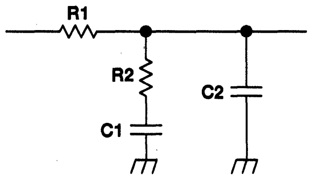


Figure 2–16. Lag-Lead Filter (With Additional Capacitor)

The value of C2 should be less than or equal to C1/10 to keep C2 from affecting the low-pass filter response while providing adequate noise filtering.

Similarly for the case of an active filter, substituting the desired values of ω_n, ζ, N, and K into equations 2.32 and 2.33, the filter parameters can be determined by choosing an appropriate value for C1.

Also when using an active filter as the loop filter, as shown in Figure 2–17, a second order active filter with one additional capacitor should be used.

The additional capacitor C2 is used for compensating the R2 high frequency response. The cutoff frequency, ω_c, of C2 and R2 should be chosen to be 10 times that of the natural frequency, ω_n, of the PLL.

$$\omega_c = \frac{1}{(C2 \times R2)} \cong 10\omega_n \tag{2.37}$$

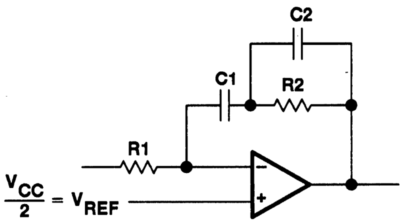


Figure 2–17. Active Filter (With Additional Capacitor)

2.8 Frequency Division

When given an input signal with frequency f, a circuit that generates a f/N (N an integer) signal synchronized to the input signal is called a frequency divider. Usually frequency dividers use programmable counters like the one shown in Figure 2–18 (programmable meaning that the frequency divide ratio N can be changed and controlled externally).

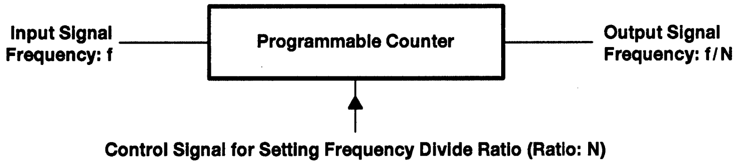


Figure 2–18. Programmable Counter

The construction of a PLL frequency divider using a programmable counter, and the prescaler and pulse swallow methods (2s modulus prescaler method) are discussed in the following sections.

2.8.1 Prescaler Method

If the frequency, f, of an input signal is too high, a divide can be added using an additional programmable counter in the feedback path. As shown in Figure 2–19, the frequency can be divided before the programmable counter using a fixed frequency divider (prescaler) operating at high speed, this lowers the input frequency to the programmable counter. This method is called the prescaler method.

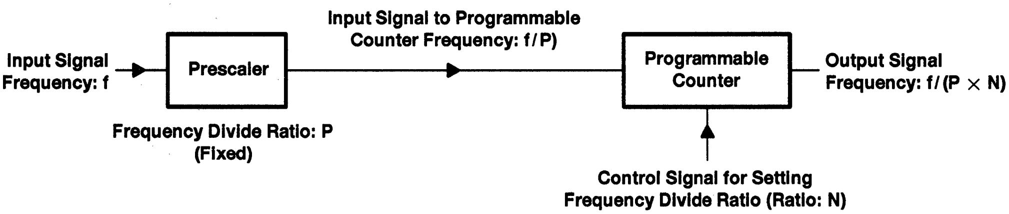


Figure 2–19. Prescaler Method

The prescaler frequency dividing ratio is fixed. As shown in Figure 2–19, if the prescaler frequency divide ratio is P and the programmable counter frequency dividing ratio is N, then the total frequency divide ratio becomes P × N. As shown in Figure 2–20, if the frequency dividing ratios M and N of the programmable counters are changed, the VCO oscillating frequency is changed in steps of P/M times the phase-reference frequency. Thus the channel space (frequency resolution) becomes $f_{REF} \times P/M$. The PLL f_{REF} should be chosen to be M/P of the channel space. Thus, if f_{REF} is low, the loop-filter time parameters must be designed to be large with respect to f_{REF}; however, the lock-up time can become too large for the application. Noise effects must be considered as well.

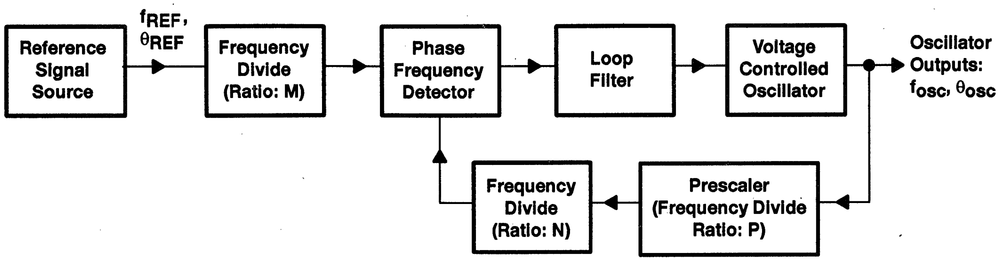


Figure 2–20. PLL Synthesizer Using Prescaler

2.8.2 Pulse Swallow Method (2s Modulus Prescaler Method)

When the channel space is equal to 1/M of the reference frequency, f_{REF}, the technique is called the pulse swallow method. This method uses a prescaler whose frequency divide ratio can be changed by a control signal as shown in Figure 2–21.

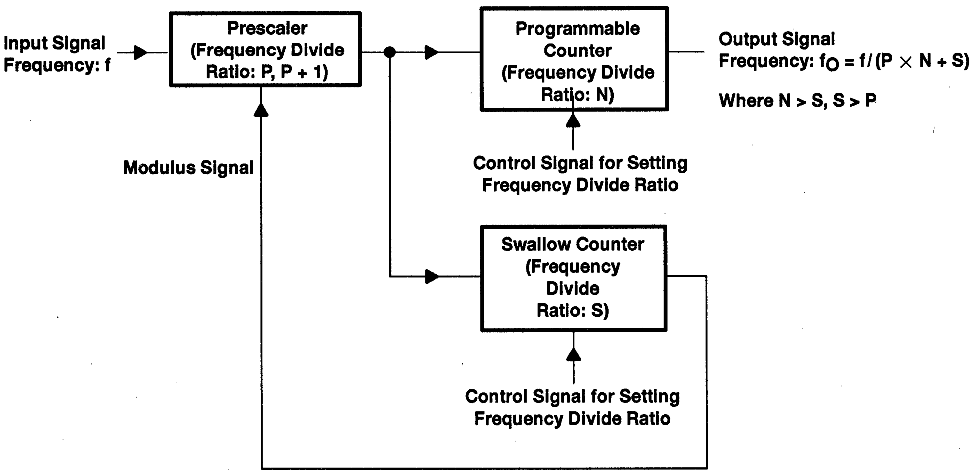


Figure 2–21. Pulse Swallow Method (2s Modulus Prescaler Method)

The prescaler frequency divide ratio is P or P+1. The counter consists of a programmable counter and a swallow counter which is used to control the prescaler. The frequency divide ratios are N and S respectively.

When the swallow counter is operating, the prescaler frequency divide ratio is P+1. The programmable counter and the swallow counter operate in parallel with the condition N > S. The swallow counter counts up to S and then generates a modulus signal to switch the prescaler. Then the prescaler's frequency divide ratio becomes P.

Thus, during the time period in which the swallow counter is dividing the frequency while counting up to S (time period S/N), the total frequency divide ratio is $(P+1) \times N$. During the remaining time period, N–S, in which the programmable counter divides the frequency [time period (N–S)/N], the total frequency divide ratio is $P \times N$. Now the output signal frequency can be expressed by the following equation:

$$f_O = f/(P \times N + S) \tag{2.38}$$

By examining the actual operation of the PLL shown in Figure 2–22 and equation 2.38, P is the coefficient for N but not for S. Thus, each time the value of S changes, the frequency only changes by f_{REF}/M. By using the pulse swallow method and a prescaler, a channel space of f_{REF}/M can be obtained.

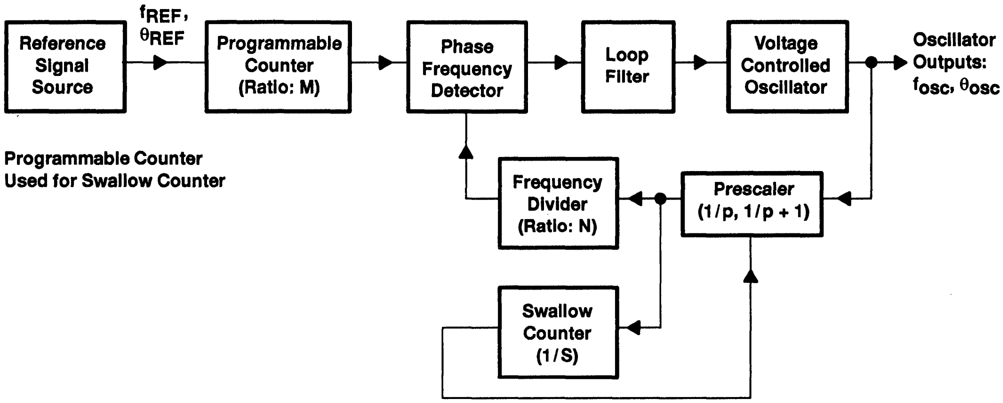


Figure 2–22. PLL Frequency Synthesizer Based on Pulse Swallow Method

Many variations exist by combining frequency dividers. A specific frequency divider technique can be adopted according to the application.

3 TLC2932IPW

3.1 Overview

The TLC2932IPW can be used for designing high performance PLLs and consists of a voltage controlled oscillator (VCO) operating at up to 50 MHz and an edge detection type phase frequency detector (PFD).

In the design of a PLL, the VCO lock range is determined by the value of a single external bias resistor. In addition, by using the inhibit function, the VCO can be turned off to reduce power dissipation. By switching the VCO output select terminal externally, the output frequency can be divided in half. Thus, lower frequencies can be produced and a 50% duty cycle can be achieved.

With the on-chip charge pump, the PFD detects the phase difference between the rising edges of an external input signal and a phase-reference signal from a reference signal source. Also the PFD output can be controlled externally by the input state to a high impedance output.

The design of a TLC2932IPW system, calculations of loop filters, layout considerations, and input-output protection circuits are explained in the following sections.

3.2 Voltage-Controlled Oscillator (VCO)

The TLC2932IPW VCO has the following special features:

- The VCO only requires one external bias resistor for oscillation and for setting the VCO variable oscillating frequency range. As shown in Figure 3–1, the possible lock frequency range is from 22 MHz to 50 MHz. The range of possible settings for bias resistance is 1.5 kΩ to 3.3 kΩ.

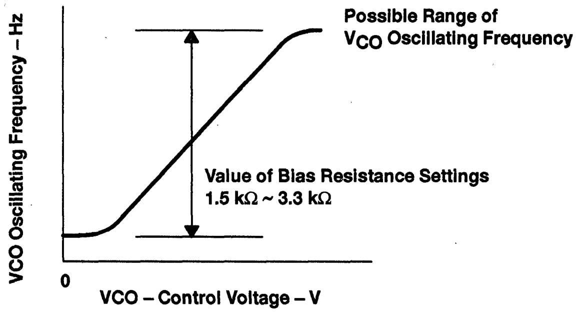


Figure 3–1. Setting the VCO Oscillating Frequency

- By switching the VCO select terminal externally, the output frequency can be divided in half to produce a lower frequency; moreover, a duty cycle of 50% is possible. By using this function, the possible frequency range is extended to 11 MHz. Video applications at 14.31818 MHz are possible.
- TLC2932IPW VCO has an inhibit function that is controlled externally
  - the output waveform can be initialized
  - power dissipation during power down can be reduced

For detailed specifications, refer to the TLC2932 data sheet.

3.3 Phase Frequency Detector (PFD)

TLC2932IPW PFD has the following special features:

- The PFD is a high speed edge triggered type with charge pump. As shown in Figure 3–2, the difference between the rising edges of two input signal frequencies can be detected.
- Depending on the external controller, the PFD output
  - can be placed in a high impedance state
  - is static when put in the power down mode

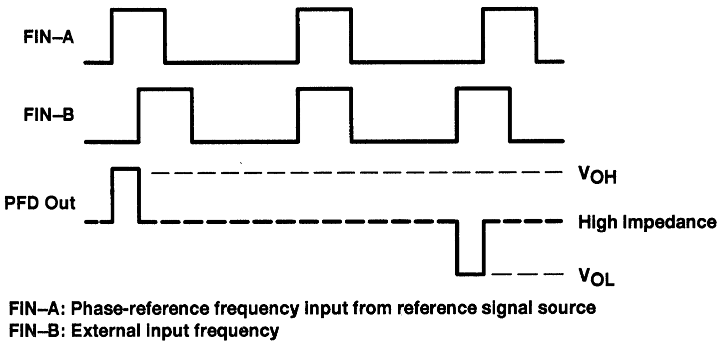


Figure 3–2. Timing of PFD Operation

3.4 Loop Filter

The loop filter design shown is based on the design equations for loop filter parameters derived in Sections 2.5. and 2.6.

Figure 3.3 shows a design based on the block diagram of a PLL synthesizer using the prescaler method.

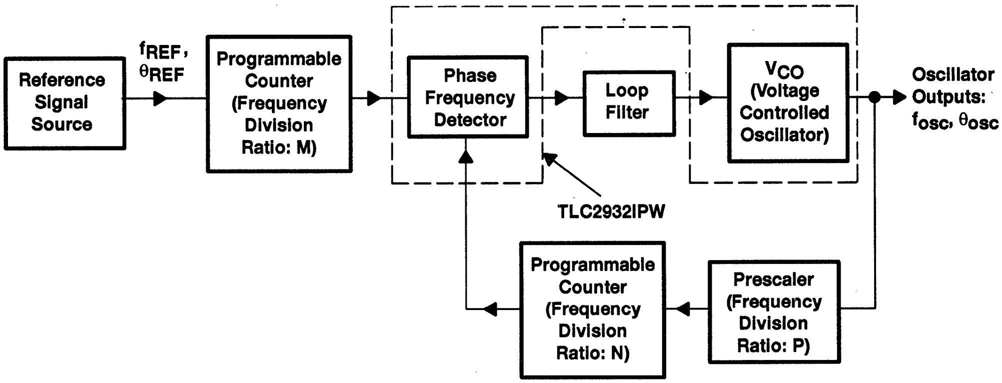


Figure 3–3. Block Diagram of PLL Synthesizer Using the Prescaler Method

3.5 Setting System Parameters

3.5.1 Setting the Phase Reference Frequency and Output Frequency from a Reference Signal Source

Each frequency is set to the values shown in Table 3–1. A 14.31818 MHz crystal is used as the reference signal source. This frequency is divided by 910 so that it can be used as the phase reference frequency. Then, the VCO output signal is 14.31818 MHz.

Table 3–1. Frequency Settings

REFERENCE SIGNAL SOURCE	SYMBOL	VALUE	UNIT
Oscillating frequency	f_{REF}	14.31818	MHz
Phase reference frequency	f_{ref}/M	14.31818/910	MHz
Output frequency	f_{osc}	14.31818	MHz

3.5.2 Setting the Frequency Division Ratios of the Programmable Counter and Prescaler

Using the settings in Table 3–1, the frequency division ratios of the programmable counter and prescaler can be determined. However, this time the design proceeds based on the settings in Table 3–2. In practice, the frequency division ratio for the prescaler is based on the frequency operating range of the programmable counter input signal.

Table 3–2. Settings for Frequency Division Ratios of the Programmable Counters and Prescaler

NAME	PARAMETER	VALUE
Programmable counter (Phase reference frequency side)	M	910
Programmable counter	N	455
Prescaler	P	2

Therefore, the total frequency division ratio becomes $P \times N = 910$.

3.5.3 Setting the Lock-Up Time

The required lock-up time is 2 ms which is the time it takes for the phase to lock and is dependent on system requirements.

3.5.4 Determining the Damping factor, ζ

The damping factor, ζ, is chosen to be 0.7.

3.5.5 Calculating the PLL Natural Angular Frequency, ω_n

For $\zeta = 0.7$ and from equation 2.34, ω_n is calculated to be

$$\omega_n = \frac{\omega_n \tau}{t} = \frac{4.5}{2 \times 10^{-3}} = 2250 \text{ (rad/sec)}$$

3.5.6 Calculating VCO Gain, K_V

Figure 3–4 shows an example of the oscillating frequency characteristic of the TLC2932 internal VCO. The VCO gain is calculated from a characteristic curve in the data sheet. By switching the SELECT terminal, the output frequency is divided in half and the resulting characteristic curve is shown in Figure 3–4.

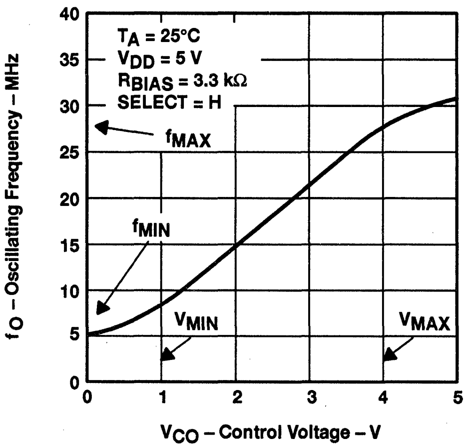


Figure 3–4. VCO Oscillating Frequency Characteristic

The VCO gain, K_V, from equation 2.35 is

$$K_V = \frac{f_{MAX} - f_{MIN}}{V_{MAX} - V_{MIN}} \times 2\pi = \frac{(27.5 - 7) \times 10^6}{4 - 1} \times 2\pi \cong 41 \times 10^6 \text{ [rad/sec/V]} \qquad (3.1)$$

3.5.7 Calculating PFD Gain, K_θ

The PFD output characteristic is shown in Figure 2–15. By substituting the values obtained from the data sheet into equation 2.36, the PFD gain is calculated to be

$$K_\theta \cong 0.34 \text{ [V/rad]} \qquad (3.2)$$

The design and circuit specifications mentioned above are listed in Tables 3–3 and 3–4.

Table 3–3. PLL Design Specifications

DESIGN SPECIFICATIONS			
NAME	SYMBOL	VALUE	UNIT
PLL damping factor	ζ	0.7	
Radian value to selected lock-up time	$\omega_n t$	4.5	rad
Lock-up time	t	0.002	s
Desired output frequency	f_{osc}	14.318180	MHz
Phase reference frequency	f_{REF}	15734.26374	Hz

Table 3–4. PLL Circuit Specifications (SELECT Terminal = H Level)

CIRCUIT SPECIFICATIONS (V_{DD} = 5 V, R_{BIAS} = 3.3 kΩ, T_A = 25°C)			
NAME	SYMBOL	VALUE	UNIT
VCO frequency range	f_{MAX}	27	MHz
	f_{MIN}	7.5	
VCO control voltage range	V_{MAX}	4	V
	V_{MIN}	1	
Phase detector output level	V_{OH}	4.5	V
	V_{OL}	0.2	
Phase detector range of detection		12.56	rad
Frequency divide ratio	N	910	
PLL natural angular frequency	ω_n	2250	rad/sec

3.5.8 Lag-Lead Filter Case

From the design and circuit specifications above and using the lag-lead filter of Figure 2–16, C2 is selected to be 1/10 of the C1 value.

The calculations are shown in Table 3–5. The transfer function gain characteristics and phase characteristics are shown in Figure 3–5 and the step response is shown in Figure 3–6.

Table 3–5. Calculation Example of Lag-Lead Filter Parameters

LAG-LEAD FILTER		
PARAMETER	VALUE	UNIT
C1	1.00E–0.6	F
R1	2476	Ω
R2	557	Ω
C2	1.00E–07	F

Where C2 = C1 × 1/10

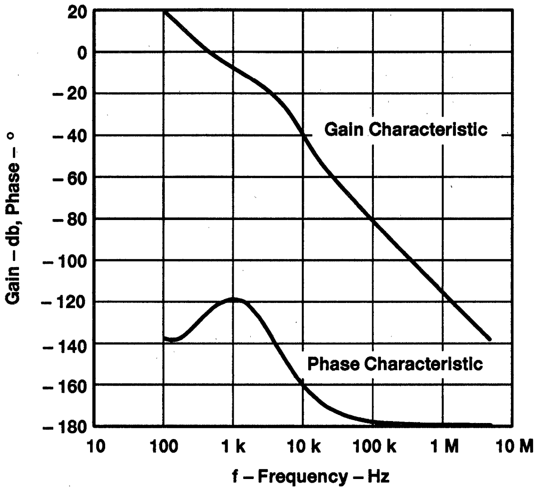


Figure 3–5. PLL Transfer Function Gain Characteristics and Phase Characteristics (Lag-Lead Filter used as Loop Filter)

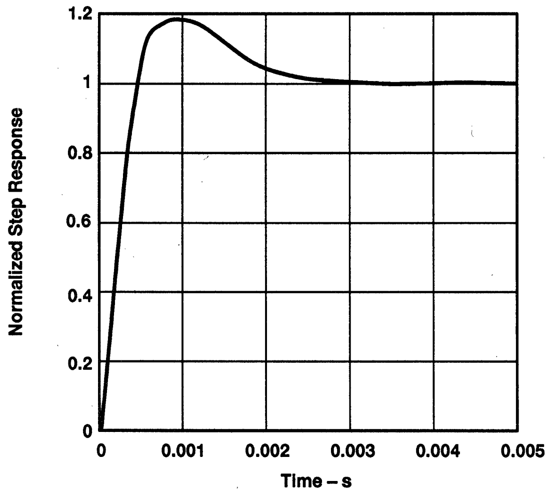


Figure 3–6. PLL Step Response Characteristic (Lag-Lead Filter used as Loop Filter)

3.5.9 Active Filter Case

The active filter is shown in Figure 2–17. Each parameter can be calculated using equations 2.32 and 2.33. C2 is calculated from equation 2.37 in Section 2.7.

Table 3–6 shows an example of these calculations. Figure 3–7 shows the transfer function gain characteristics and phase characteristics of a PLL using the filter parameters in Table 3–6. Figure 3–8 shows the step response of utilizing the filter parameters in Table 3–6.

Table 3–6. Calculation Example of Active Filter Parameters

ACTIVE FILTER		
PARAMETER	VALUE	UNIT
C1	1.00E–0.6	F
R1	3033	Ω
R2	622	Ω
C2	7.14E–07	F

Where C2 = R2/10 ω_n

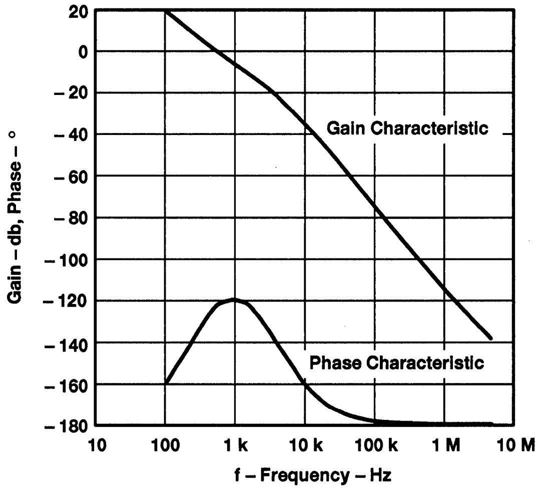


Figure 3–7. PLL Transfer Function Gain Characteristics and Phase Characteristics (Active Filter used as Loop Filter)

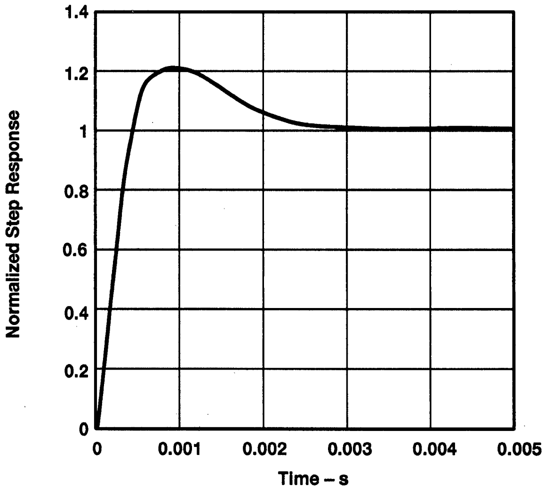


Figure 3–8. PLL Step Response Characteristic (Active Filter used as Loop Filter)

A basic design example for a PLL loop filter is somewhat of an ideal case. In practice, the PLL characteristics greatly depend on the evaluation board used and the layout of components in the system. Consequently, it is necessary to plan the evaluation board and system carefully.

Section 4, contains the evaluation results of the loop filters.

3.6 Layout Considerations

When designing an evaluation or production board, the following precautions, based on techniques used with high frequency analog circuits must be exercised.

- Depending on the IC socket used, increased circuit resistance, inductance, and capacitance can degrade the performance in some cases. If possible, do not use IC sockets. Direct connection to the board is recommended.
- Extreme care should be exercised with wiring and connections. Casual wiring should be avoided.
- Power supplied to the V_{DD} terminal of the VCO should be separated from the digital portion. Moreover, by inserting high pass capacitors, noise coupling can be avoided as much as possible.
- It is necessary to consider the VCO ground terminal. The analog portion and digital portion must be separated. The analog portion should be connected to a ground plane. The design should avoid the coupling of switching noise from the digital portion.
- The loop filter ground should be connected to analog ground..
- External components (such as the loop filter and high pass capacitors) should be placed as close as possible to the IC.

Layouts and bread boards must be carefully designed to realize the full potential of the TLC2932. These techniques must be used to ensure proper operation of the PLL design.

3.7 Input-Output Protection Circuits

The input and output protection circuits are shown in Table 3–7.

Table 3–7. Input-Output Protection Circuits

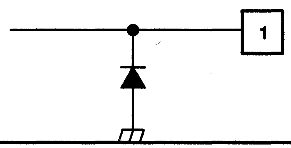
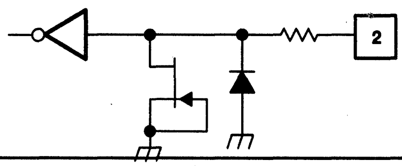
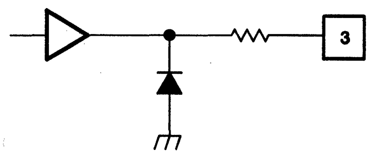
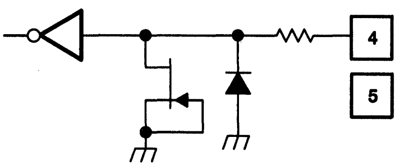
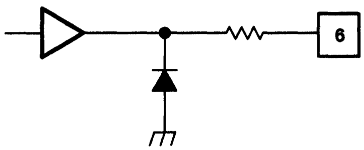
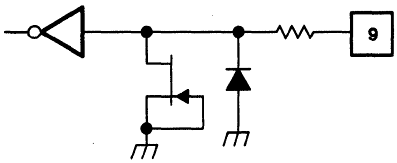
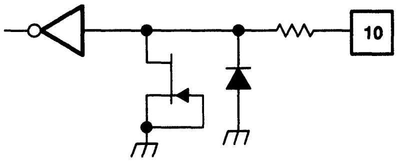
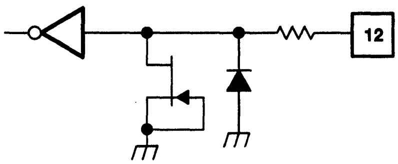
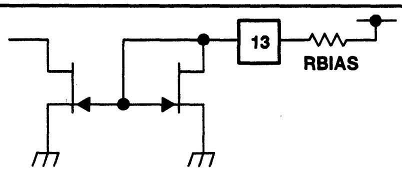
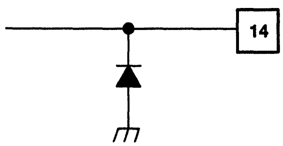
TERMINAL NAME	TERMINAL NO.	CIRCUIT	FUNCTION
LOGIC V_{DD}	1		Voltage supply terminal for internal logic. It is desirable to separate completely from the VCO voltage supply terminal.
SELECT	2		VCO output frequency 1/2 divider select terminal. By controlling this terminal using external logic, the VCO output frequency can be divided in half.
VCO OUT	3		VCO output terminal. During inhibit, this terminal is taken low.
FIN-A,B	4, 5		The two input terminals used for detecting the edge difference of reference frequency, f_{ref}-IN, and external counter's frequency. Usually f_{ref}-IN is connected to the FIN-A terminal and the external counter output frequency is connected to the FIN-B terminal.

Table 3–7. Input-Output Protection Circuits (Continued)

TERMINAL NAME	TERMINAL NO.	CIRCUIT	FUNCTION
PFD OUT	6		The PFD output terminal can be put in high impedance state.
LOGIC GND	7		Internal logic ground terminal.
NC	8		Not connected internally.
PFD INHIBIT	9		The PFD inhibit function control terminal.
VCO INHIBIT	10		The VCO inhibit function control pin
VCO GND	11		VCO ground terminal
VCO IN	12		The VCO control voltage input terminal usually connected to VCO control voltage from the external loop filter of PLL.
R BIAS	13		The terminal for connecting the bias resistor for setting the VCO oscillating frequency. To provide a bias for the operation of internal VCO and for frequency setting and tuning, a bias resistor is connected between this terminal and the power supply line.
VCO V_{DD}	14		This terminal supplies the supply voltage to the VCO. It is desirable to completely separate this from the logic power terminal.

4 APPLICATION EXAMPLE

4.1 Introduction

An evaluation example using the TLC2932IPW in a PLL application is described in the following sections.

4.2 National Television System Committee (NTSC) Method 4 Frequency Sub-Carrier (fsc), 8 fsc Output Signal Evaluation

Table 4–1 shows that by combining a phase reference frequency and loop filter, the NTSC method of 4 fsc and 8 fsc output signals can be generated.

The block diagram is shown in Figure 4–1. Figure 4–2 shows the circuit for evaluation, using a passive lag-lead filter as the loop filter. This evaluation circuit is based on the conditions stated in number 2 of Table 4–1.

When an active filter is used, because of additional inversion added to the loop, the phase frequency detector input signal is reversed from that in the passive lag-lead filter case.

Table 4–1. Evaluation Conditions (V_{DD} = 5 V, T_A = 25°C, R_{BIAS} = 3.3 kΩ)

NO.	PHASE REFERENCE FREQUENCY	OUTPUT FREQUENCY	LOOP FILTER	EVALUATION RESULT
1	fsc (NTSC) = 3.579545 MHz	4 fsc (NTSC) = 14.31818 MHz	Lag-lead and active	Section 4.3
2	HD (NTSC) = 4 fsc/910 ≈ 15.7 kHz	4 fsc (NTSC) = 14.31818 MHz		Section 4.6
3	HD (NTSC) = 4 fsc/910 ≈ 15.7 kHz	8 fsc = 28.63636 MHz		Section 4.9

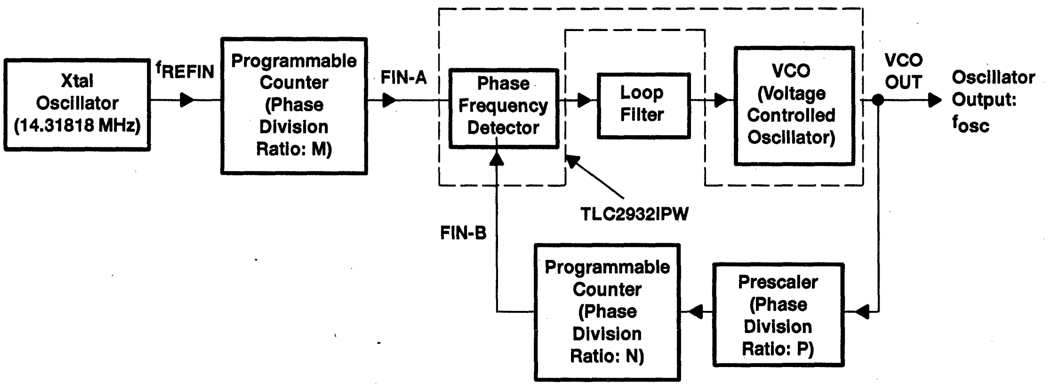


Figure 4–1. 4 fsc Output Evaluation Block Diagram

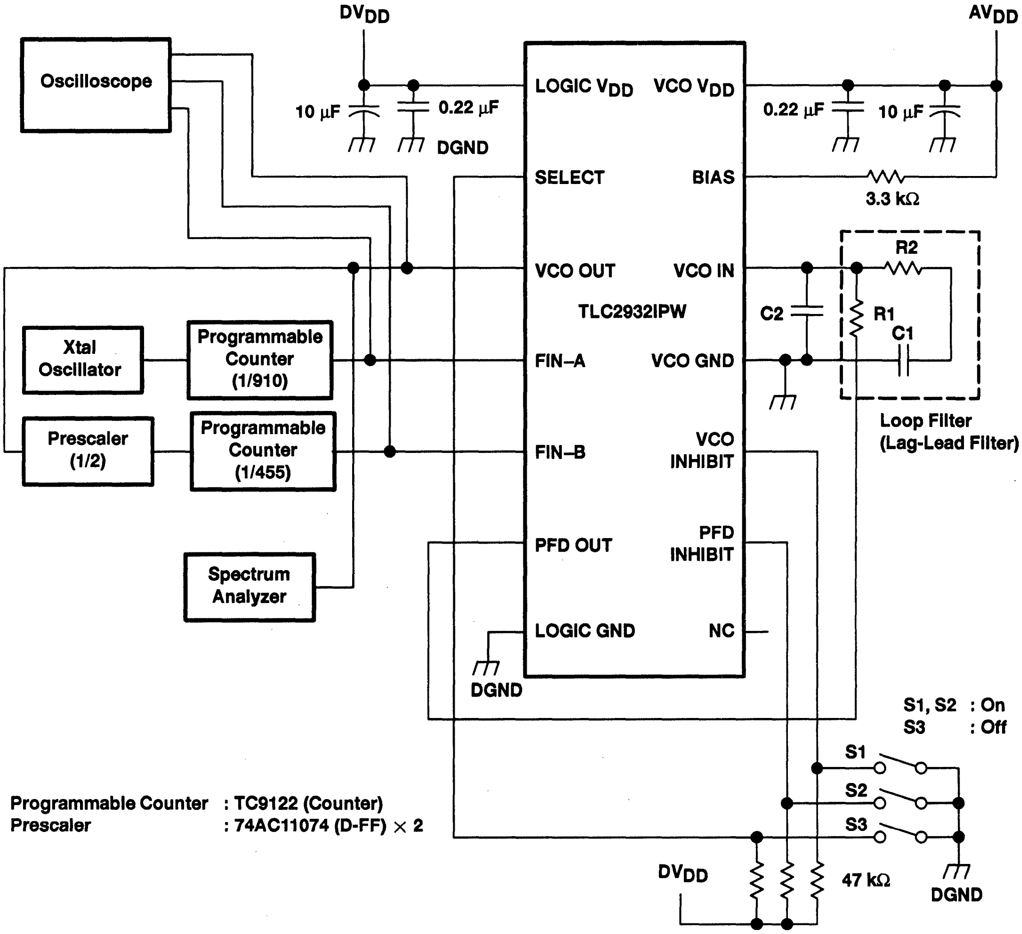


Figure 4–2. Evaluation Circuit (Based on Number 2 of Table 4–1) (Lag-Lead Filter Used as Loop Filter)

4.3 Evaluation Results (Phase Reference Frequency = fsc, Output Frequency = 4 fsc)

In this evaluation, the fsc (3.579545 MHz) shown as number 1 in Table 4–1, is used as the phase reference frequency to generate a 4 fsc (14.31818 MHz) output frequency. The details and results for the cases of using a lag-lead filter and an active filter as the loop filter are described in the following sections.

4.3.1 Programmable Counter and Prescaler Frequency Division Ratio Settings

Based on the evaluation block diagram of Figure 4–1, the frequency division ratio settings for the programmable counters and prescaler are listed in Table 4–2.

Table 4–2. Frequency Division Ratio Settings

FREQUENCY DIVISION RATIO	M	P	N	P×N
Frequency divide value	4	1	4	4

4.3.2 Loop Filter Parameter Settings

From the loop filter design procedures of Sections 2.5 and 2.6, the setting of each parameter is listed in Table 4–3.

Table 4–3. Loop Filter Parameter Settings

LOOP FILTER TYPE	C1	R1	R2	C2	CIRCUIT CONSTRUCTION
Lag-lead filter	1 µF	1.6 kΩ	36 Ω	0.1 µF	Figure 2–16
Active filter	1 µF	1.6 kΩ	36 Ω	0.1 µF	Figure 2–17

NOTE: The numerical values in Table 4–3 are the capacitance and resistance closest to the calculated values.

4.3.3 Passive Lag-Lead Filter Used as a Loop Filter

The evaluation results of using a lag-lead filter as the loop filter are illustrated in Figure 4–3 and Figure 4–4. Figure 4–3 shows the individual waveforms as observed from an oscilloscope. Figure 4–4 shows the output signal measured by a spectrum analyzer.

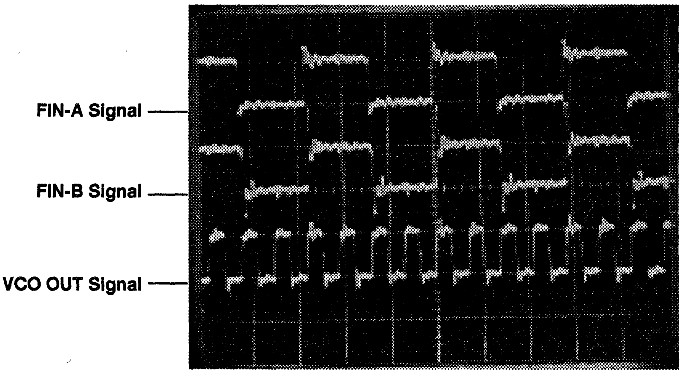


Figure 4–3. Waveforms Using Passive Lag-Lead Filter (100 ns/div on horizontal axis)

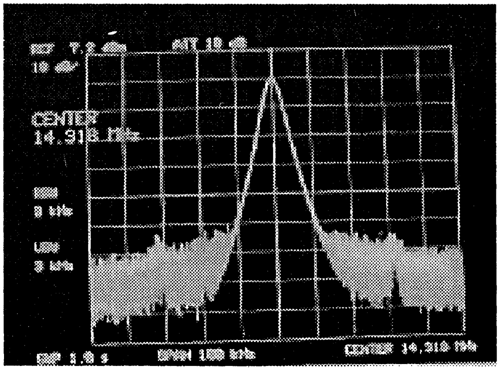


Figure 4–4. Spectrum of the VCO Output Signal When Using a Passive Lag-Lead Filter (100 kHz/div on horizontal axis)

4.3.4 Active Filter Used as a Loop Filter

The evaluation results of using an active filter as the loop filter are illustrated in Figure 4–5 and Figure 4–6. Figure 4–5 shows the individual waveforms as observed from an oscilloscope. Figure 4–6 shows the output signal measured by a spectrum analyzer.

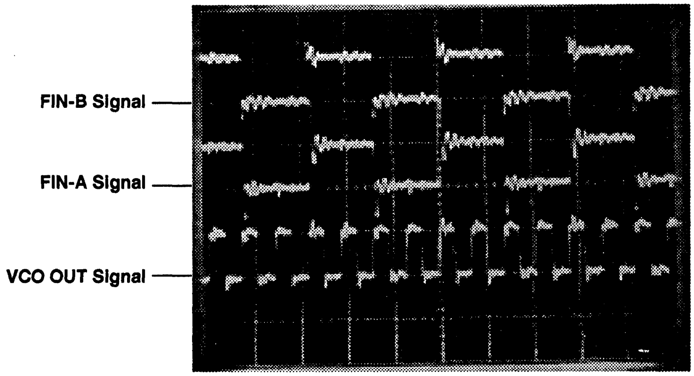


Figure 4–5 Waveforms Using Active Filter (100 ns/div on horizontal axis)

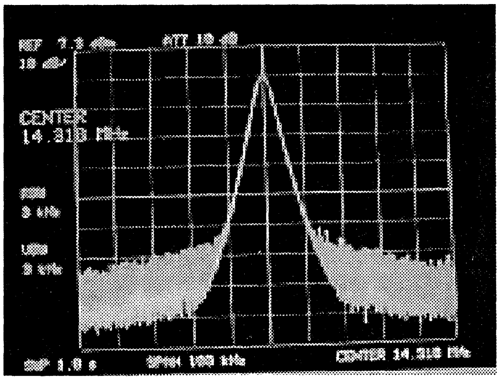


Figure 4–6. Spectrum of the VCO Output Signal When Using an Active Filter (100 kHz/div on horizontal axis)

4.4 Evaluation Results (Phase Reference Frequency = 4 fsc/910, Output Frequency = 4 fsc)

In this evaluation of number 2 in Table 4–1, fsc/910 (15.7 kHz) is used as the phase reference frequency to generate a 4 fsc (14.31818 MHz) output frequency. The details and results for the cases of using a lag-lead filter and an active filter as the loop filter are described in the following sections.

4.4.1 Programmable Counter and Prescaler Frequency Division Ratio Settings

Based on the evaluation block diagram of Figure 4–1, the frequency division ratio settings for the programmable counter and prescaler are listed in Table 4–4.

Table 4–4. Frequency Division Ratio Settings

FREQUENCY DIVISION RATIO	M	P	N	P × N
Frequency divide value	910	2	455	910

4.4.2 Loop Filter Settings

Following the loop filter design procedures of Sections 2.5 and 2.6, the setting of each parameter is listed in Table 4–5.

Table 4–5. Loop Filter Parameter Settings

LOOP FILTER	C1	R1	R2	C2	CIRCUIT CONSTRUCTION
Lag-lead filter	1 μF	2.4 kΩ	560 Ω	0.1 μF	Figure 2–16
Active filter	1 μF	3 kΩ	620 Ω	0.1 μF	Figure 2–17

NOTE: Numerical values in Table 4–5 are the capacitance and resistance closest to the calculated values.

4.4.3 Passive Lag-Lead Filter Used as a Loop Filter

Using lag-lead filter as the loop filter, the evaluation results are illustrated in Figure 4–7 and Figure 4–8. Figure 4–7 shows the individual waveforms as observed from an oscilloscope. Figure 4–8 shows the output signal measured by a spectrum analyzer.

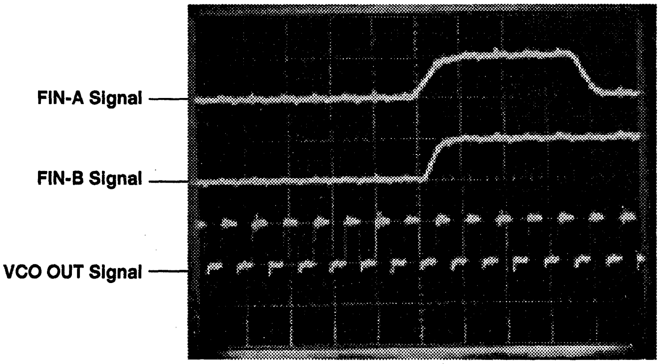


Figure 4–7. Waveforms Using Passive Lag-Lead Filter (100 ns/div on horizontal axis)

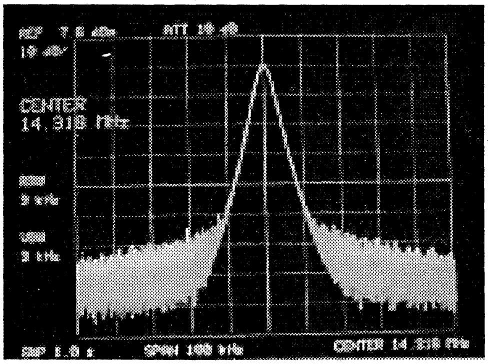


Figure 4–8. Spectrum of the VCO Output Signal When Using a Passive Lag-Lead Filter (100 kHz/div on horizontal axis)

4.4.4 Active Filter Used as a Loop Filter

Using an active filter as the loop filter, the evaluation results are illustrated in Figure 4–9 and Figure 4–10. Figure 4–9 shows the individual waveforms as observed from an oscilloscope. Figure 4–10 shows the output signal measured by a spectrum analyzer.

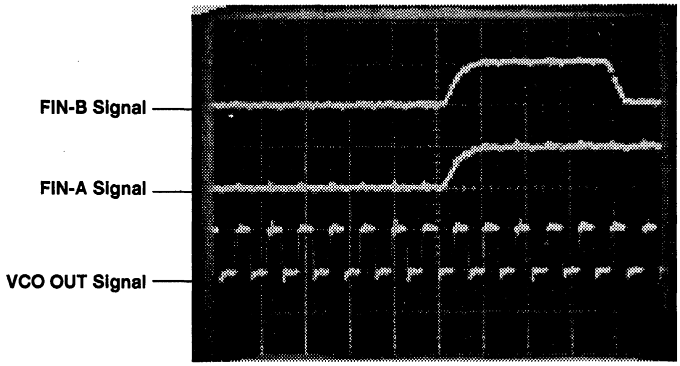


Figure 4–9. Waveforms Using Active Filter
(100 ns/div on horizontal axis)

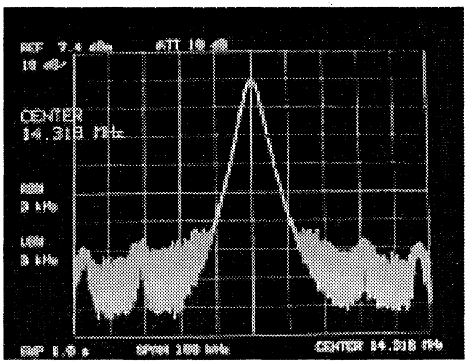


Figure 4–10. Spectrum of the VCO Output Signal When Using an Active Filter
(100 kHz/div on horizontal axis)

4.5 Evaluation Results (Phase Reference Frequency = fsc/910, Output Frequency = 8 fsc)

In this evaluation of number 1 in Table 4–1, fsc (3.579545 kHz) is used as the phase reference frequency to generate a 8 fsc (2 × 14.31818 MHz) output frequency. The details and results for the cases of using a lag-lead filter and an active filter as the loop filter are described in the following sections.

4.5.1 Programmable Counter and Prescaler Frequency Division Ratio Settings

Based on the evaluation block diagram of Figure 4–1, the frequency division settings for programmable counters and prescaler are listed in Table 4–6.

Table 4–6. Frequency Division Ratio Settings

FREQUENCY DIVIDE RATIO	M	P	N	P × N
Frequency dividing value	910	4	455	1820

4.5.2 Loop Filter Settings

Following the loop filter design procedures of Sections 2.5 and 2.6, the setting of each parameter is listed in Table 4–7.

Table 4–7. Loop Filter Parameter Settings

LOOP FILTER	C1	R1	R2	C2	CIRCUIT CONSTRUCTION
Lag-lead filter	1 µF	2.4 kΩ	560 Ω	0.1 µF	Figure 2–16
Active Filter	1 µF	3 kΩ	620 Ω	0.1 µF	Figure 2–17

NOTE: Numerical values in Table 4–6 are the capacitance and resistance closest to the calculated values.

4.5.3 Passive Lag-Lead Filter Used as a Loop Filter

The evaluation results of using a lag-lead filter as the loop filter are illustrated in Figure 4–11 and Figure 4–12. Figure 4–11 shows the individual waveforms as observed from an oscilloscope. Figure 4–12 shows the output signal measured by a spectrum analyzer.

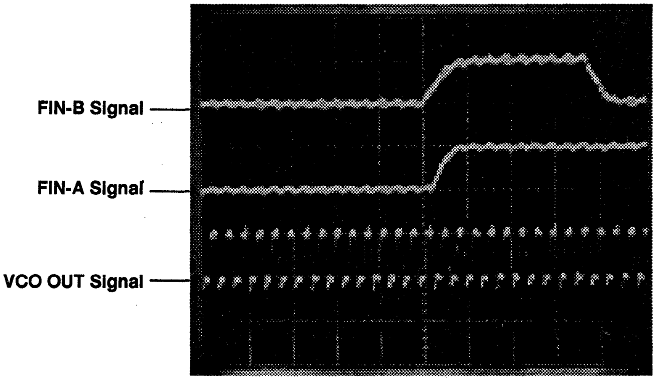


Figure 4–11. Waveforms Using Passive Lag-Lead Filter (100 ns/div on horizontal axis)

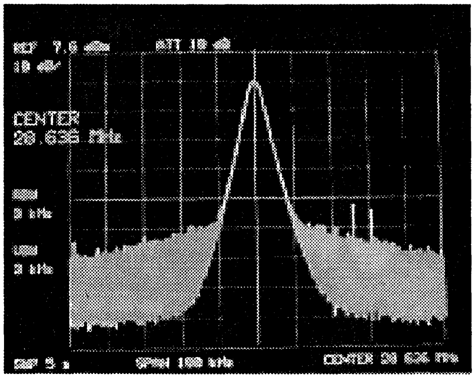


Figure 4–12. Spectrum of the VCO Output Signal When Using a Passive Lag-Lead Filter (100 kHz/div on horizontal axis)

4.5.4 Active Filter Used as a Loop Filter

The evaluation results of using an active filter as the loop filter are illustrated in Figure 4–13 and Figure 4–14. Figure 4–13 shows the individual waveforms as observed from an oscilloscope. Figure 4–14 shows the output signal measured by a spectrum analyzer.

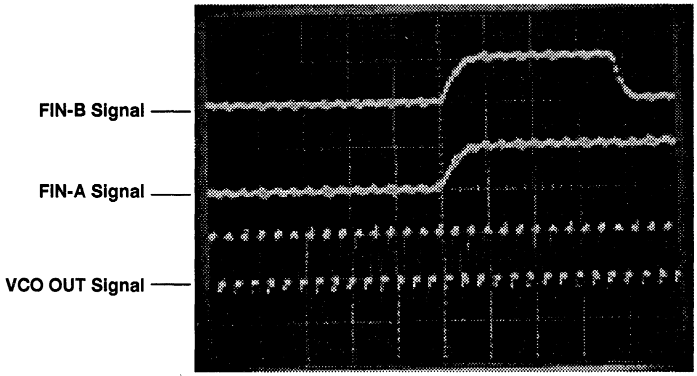


Figure 4–13. Waveforms Using an Active Filter (100 ns/div on horizontal axis)

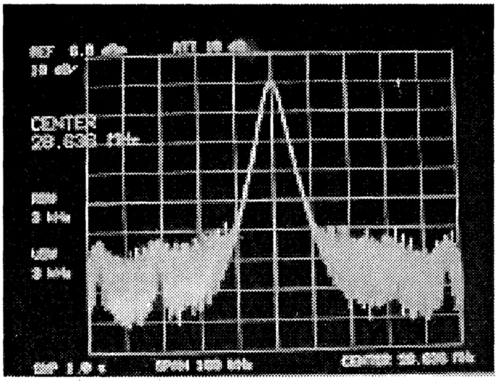


Figure 4–14. Spectrum of the VCO Output Signal When Using an Active Filter (100 kHz/div on horizontal axis)

4.6 Summary

The evaluation results shown were with the practical resistance and practical capacitance values closest to the calculated values used for the loop filter. The evaluations were carried out with a TLC2932IPW placed in the IC socket on an evaluation board with power supplies, and the BIAS terminal was bypassed directly on the bottom of the socket.

Better results can be achieved however by placing the TLC2932IPW directly on the evaluation board.

4.7 Examples of a PLL Application

The following sections contain PLL application examples.

4.7.1 Generating a 4 fsc NTSC Signal from a NTSC Signal

A NTSC signal horizontal synchronization frequency (f_H) is multiplied by 910 to generate a 4 fsc NTSC signal. Figure 4–15 shows a block diagram of the PLL.

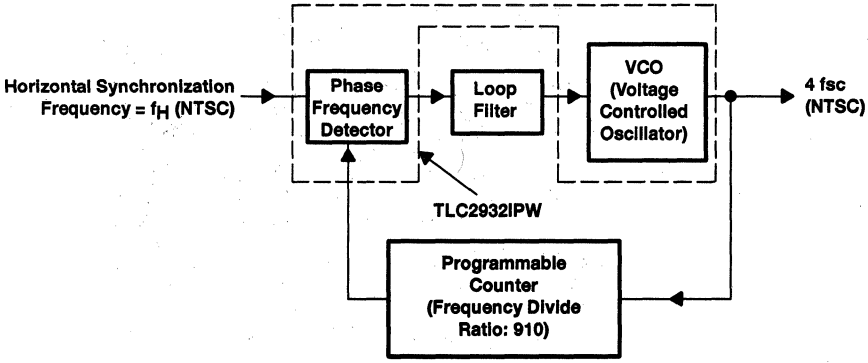


Figure 4–15. Generating a 4 fsc (NTSC) Signal by Multiplying the Horizontal Synchronization Frequency

4.7.2 Generating a 4 fsc PAL Signal from a PAL Signal

A phase alteration line (PAL) signal horizontal synchronization frequency (f_H) is multiplied by 910 to generate a 4 fsc PAL signal. Figure 4–16 shows a block diagram of the PLL.

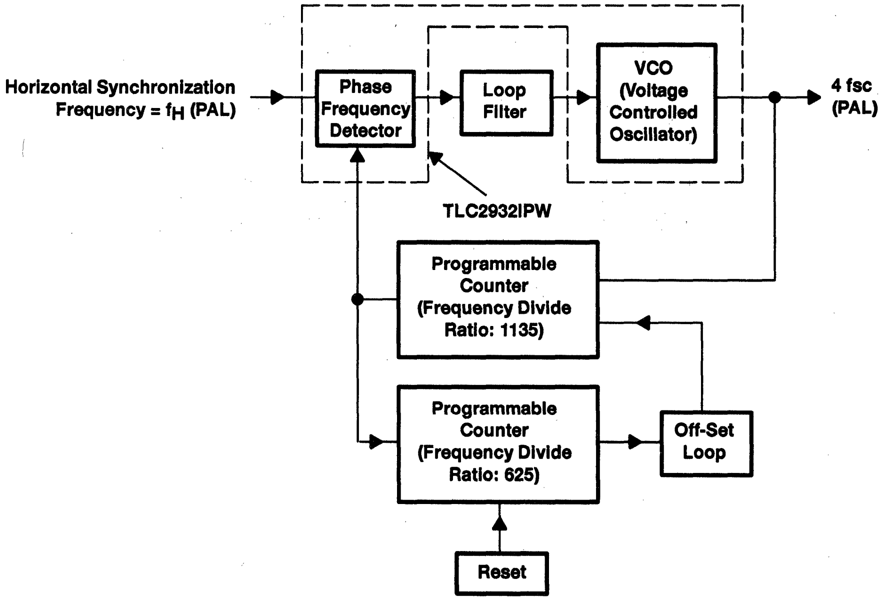


Figure 4–16. Generating a 4 fsc (PAL) Signal by Multiplying the Horizontal Synchronization Frequency

4.7.3 Generating a 13.5 MHz Output from a NTSC or PAL Signal

Figure 4–17 shows the derivative of a 4 fsc signal from a PAL or NTSC horzontial synchronization frequency.

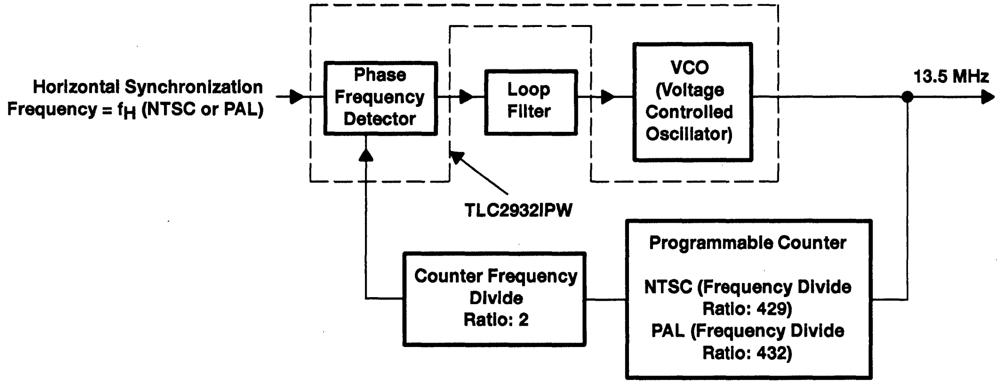


Figure 4–17. Multiplying the Horizontal Synchronization Frequency of a NTSC Signal or PAL Signal to Generate a 13.5 MHz Output

Understanding Data Converters

TEXAS INSTRUMENTS

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Contents

List of Illustrations

1 INTRODUCTION

This application report discusses the way the specifications for a data converter are defined on a manufacturers data sheet and considers some of the aspects of designing with data conversion products. It covers the sources of error that change the characteristics of the device from an ideal function to reality.

2 THE IDEAL TRANSFER FUNCTION

The theoretical ideal transfer function for an ADC is a straight line, however, the practical ideal transfer function is a uniform staircase characteristic shown in Figure 1. The DAC theoretical ideal transfer function would also be a straight line with an infinite number of steps but practically it is a server of points that fall on the ideal straight line as shown in Figure 2.

2.1 Analog-to-Digital Converter (ADC)

An ideal ADC uniquely represents all analog inputs within a certain range by a limited number of digital output codes. The diagram in Figure 1 shows that each digital code represents a fraction of the total analog input range. Since the analog scale is continuous, while the digital codes are discrete, there is a quantization process that introduces an error. As the number of discrete codes increases, the corresponding step width gets smaller and the transfer function approaches an ideal straight line. The steps are designed to have transitions such that the midpoint of each step corresponds to the point on this ideal line.

The width of one step is defined as 1 LSB (one least significant bit) and this is often used as the reference unit for other quantities in the specification. It is also a measure of the resolution of the converter since it defines the number of divisions or units of the full analog range. Hence, 1/2 LSB represents an analog quantity equal to one half of the analog resolution.

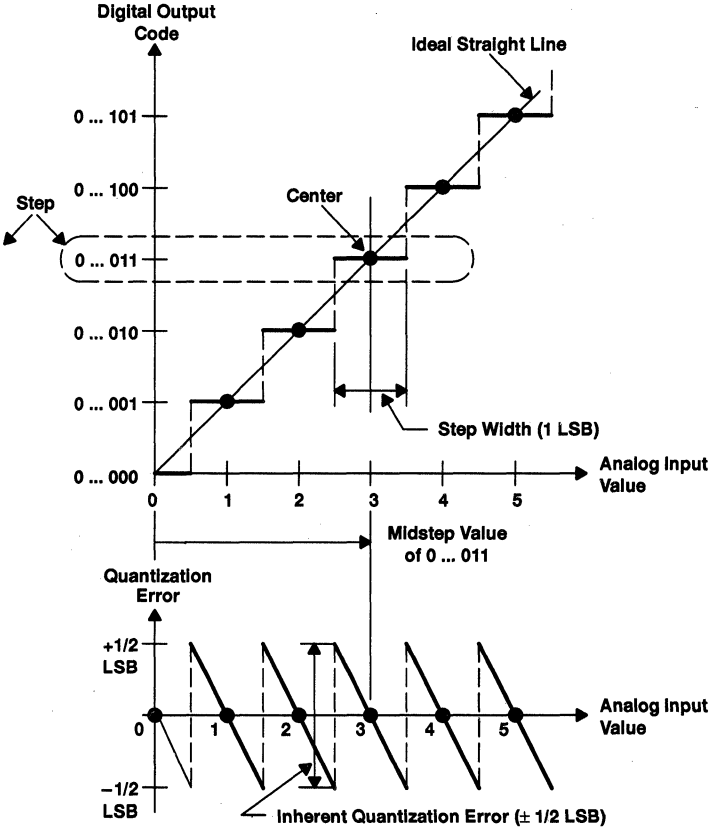
The resolution of an ADC is usually expressed as the number of bits in its digital output code. For example, an ADC with an n-bit resolution has 2^n possible digital codes which define 2^n step levels. However, since the first (zero) step and the last step are only one half of a full width, the full-scale range (FSR) is divided into $2^n - 1$ step widths.

Hence

$$1 \text{ LSB} = \text{FSR}/(2^n - 1) \text{ for an n-bit converter}$$

CONVERSION CODE

RANGE OF ANALOG INPUT VALUES	DIGITAL OUTPUT CODE
4.5 • 5.5	0 ... 101
3.5 • 4.5	0 ... 100
2.5 • 3.5	0 ... 011
1.5 • 2.5	0 ... 010
0.5 • 1.5	0 ... 001
0 • 0.5	0 ... 000

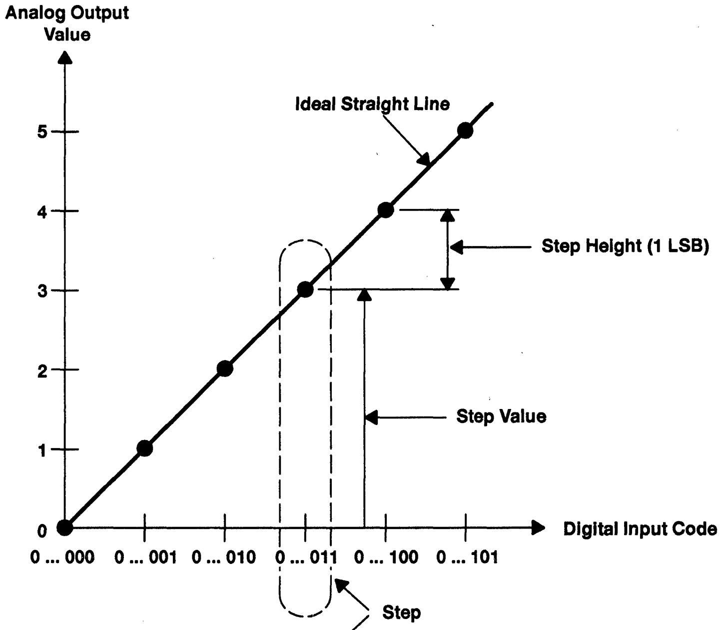


Elements of Transfer Diagram for an Ideal Linear ADC

Figure 1. The Ideal Transfer Function (ADC)

2.2 Digital-to-Analog Converter (DAC)

A DAC represents a limited number of discrete digital input codes by a corresponding number of discrete analog output values. Therefore, the transfer function of a DAC is a series of discrete points as shown in Figure 2. For a DAC, 1 LSB corresponds to the height of a step between successive analog outputs, with the value defined in the same way as for the ADC. A DAC can be thought of as a digitally controlled potentiometer whose output is a fraction of the full scale analog voltage determined by the digital input code.



CONVERSION CODE

Digital Input Code	0 ... 000	0 ... 001	0 ... 010	0 ... 011	0 ... 100	0 ... 101
Analog Output Value	0	1	2	3	4	5

Elements of Transfer Diagram for an Ideal Linear DAC

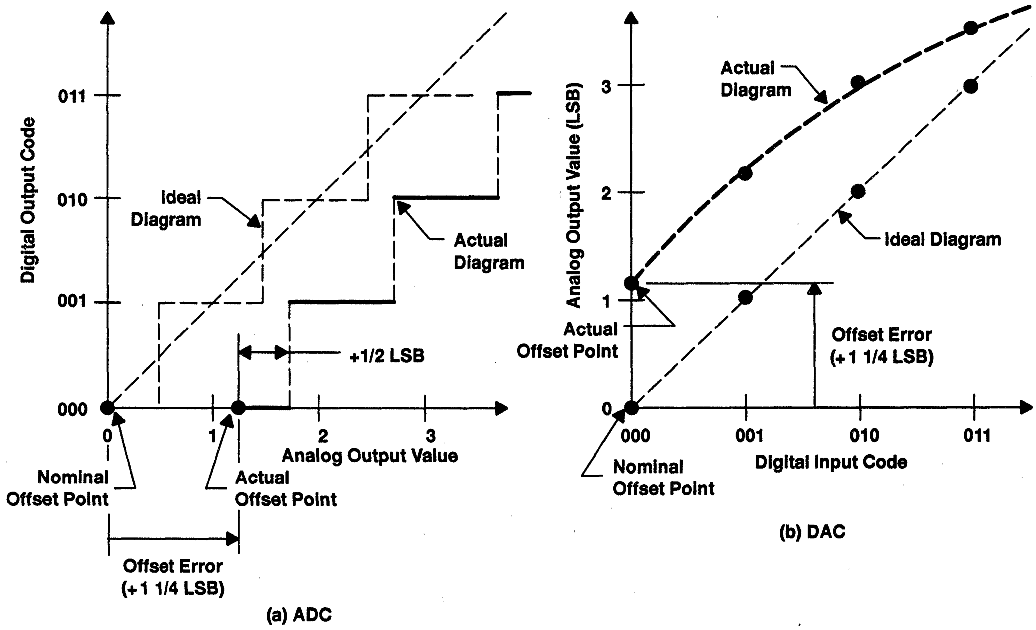
Figure 2. The Ideal Transfer Function (DAC)

3 SOURCES OF STATIC ERROR

Static errors, that is those errors that affect the accuracy of the converter when it is converting static (dc) signals, can be completely described by just four terms. These are offset error, gain error, integral nonlinearity and differential nonlinearity. Each can be expressed in LSB units or sometimes as a percentage of the FSR. For example, an error of 1/2 LSB for an 8-bit converter corresponds to 0.2% FSR.

3.1 Offset Error

The offset error as shown in Figure 3 is defined as the difference between the nominal and actual offset points. For an ADC, the offset point is the midstep value when the digital output is zero, and for a DAC it is the step value when the digital input is zero. This error affects all codes by the same amount and can usually be compensated for by a trimming process. If trimming is not possible, this error is referred to as the zero-scale error.

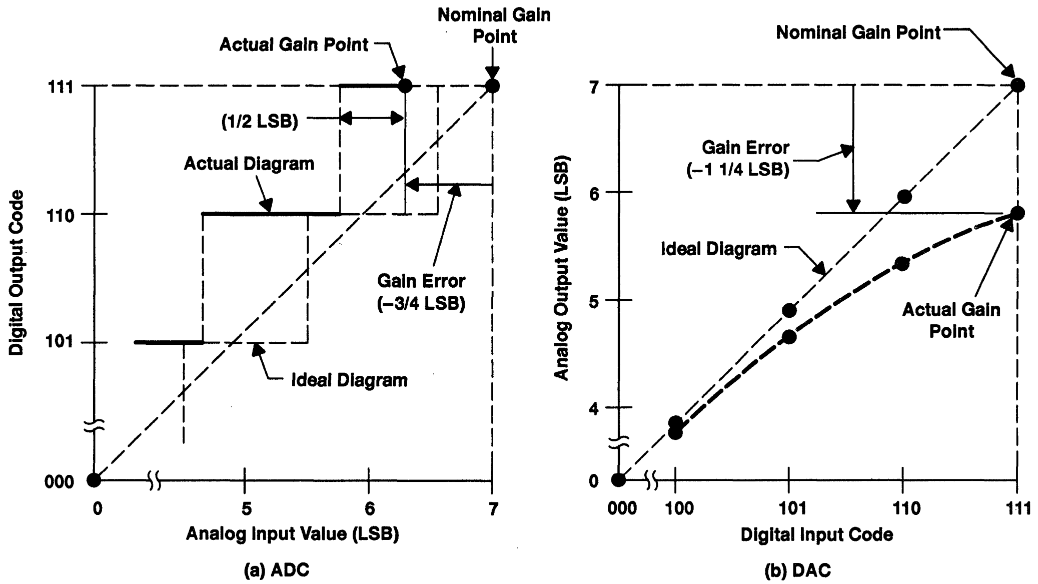


Offset error of a Linear 3-Bit Natural Binary Code Converter
(Specified at Step 000)

Figure 3. Offset Error

3.2 Gain Error

The gain error shown in Figure 4 is defined as the difference between the nominal and actual gain points on the transfer function after the offset error has been corrected to zero. For an ADC, the gain point is the midstep value when the digital output is full scale, and for a DAC it is the step value when the digital input is full scale. This error represents a difference in the slope of the actual and ideal transfer functions and as such corresponds to the same percentage error in each step. This error can also usually be adjusted to zero by trimming.

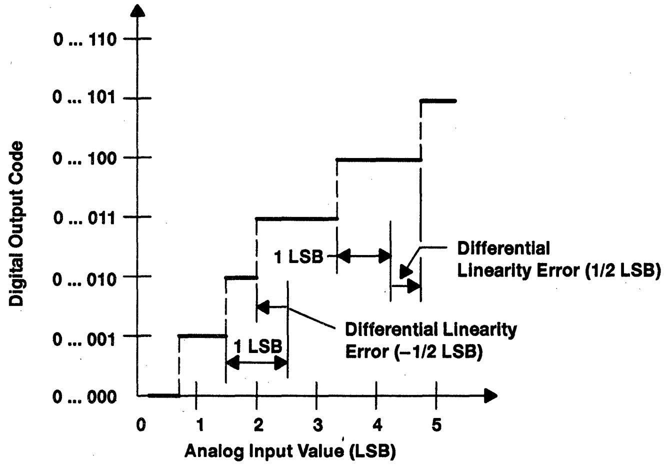


Gain Error of a Linear 3-Bit Natural Binary Code Converter (Specified at Step 111), After Correction of the Offset Error

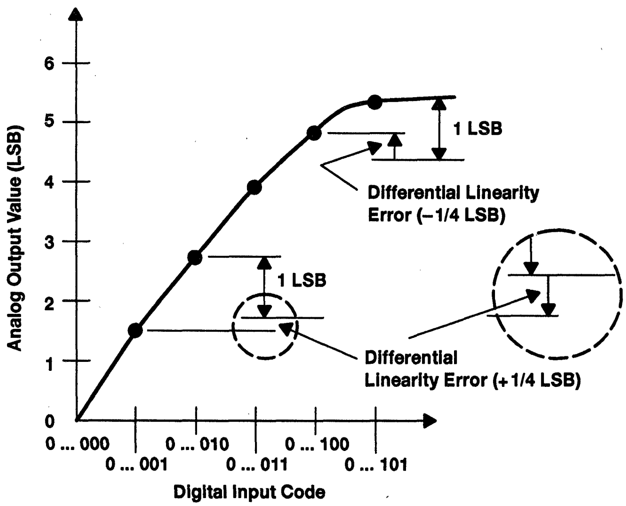
Figure 4. Gain Error

3.3 Differential Nonlinearity (DNL) Error

The differential nonlinearity error shown in Figure 5 (sometimes seen as simply differential linearity) is the difference between an actual step width (for an ADC) or step height (for a DAC) and the ideal value of 1 LSB. Therefore if the step width or height is exactly 1 LSB, then the differential nonlinearity error is zero. If the DNL exceeds 1 LSB, there is a possibility that the converter can become nonmonotonic. This means that the magnitude of the output gets smaller for an increase in the magnitude of the input. In an ADC there is also a possibility that there can be missing codes i.e., one or more of the possible 2^n binary codes are never output.



(a) ADC



(b) DAC

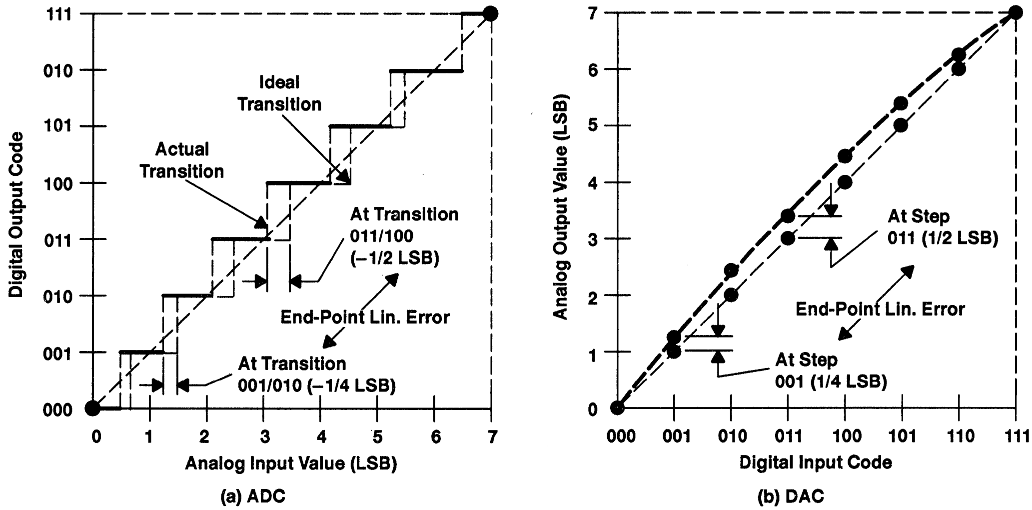
Differential Linearity Error of a Linear ADC or DAC

Figure 5. Differential Nonlinearity (DNL)

3.4 Integral Nonlinearity (INL) Error

The integral nonlinearity error shown in Figure 6 (sometimes seen as simply linearity error) is the deviation of the values on the actual transfer function from a straight line. This straight line can be either a best straight line which is drawn so as to minimize these deviations or it can be a line drawn between the end points of the transfer function once the gain and offset errors have been nullified. The second method is called end-point linearity and is the usual definition adopted since it can be verified more directly.

For an ADC the deviations are measured at the transitions from one step to the next, and for the DAC they are measured at each step. The name integral nonlinearity derives from the fact that the summation of the differential nonlinearities from the bottom up to a particular step, determines the value of the integral nonlinearity at that step.

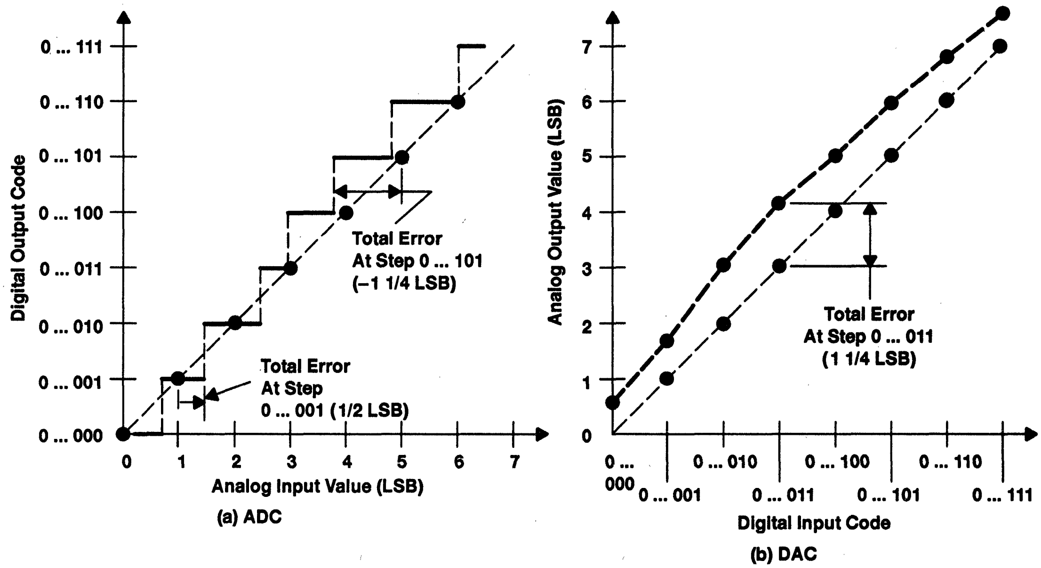


End-Point Linearity Error of a Linear 3-Bit Natural Binary-Coded ADC or DAC
(Offset Error and Gain Error are Adjusted to the Value Zero)

Figure 6. Integral Nonlinearity (INL) Error

3.5 Absolute Accuracy (Total) Error

The absolute accuracy or total error of an ADC as shown in Figure 7 is the maximum value of the difference between an analog value and the ideal midstep value. It includes offset, gain, and integral linearity errors and also the quantization error in the case of an ADC.



Absolute Accuracy or Total Error of a Linear ADC or DAC

Figure 7. Absolute Accuracy (Total) Error

4 APERTURE ERROR

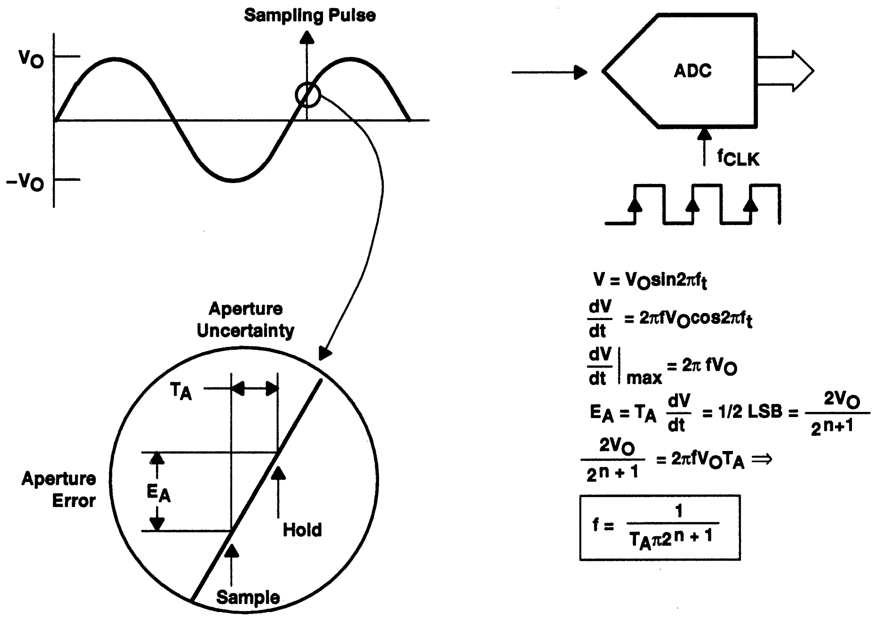


Figure 8. Aperture Error

Aperture error is caused by the uncertainty in the time at which the sample/hold goes from sample mode to hold mode as shown in Figure 8. This variation is caused by noise on the clock or the input signal. The effect of the aperture error is to set another limitation on the maximum frequency of the input sine wave because it defines the maximum slew rate of that signal. For a sine wave input as shown, the value of the input V is defined as:

$$V = V_O \sin 2\pi ft$$

The maximum slew rate occurs at the zero crossing point and is given by:

$$\left.\frac{dV}{dt}\right|_{max} = 2\pi fV_O$$

If the aperture error is not to affect the accuracy of the converter, it must be less than 1/2 LSB at the point of maximum slew rate. For an n bit converter therefore:

$$E_A = T_A \frac{dV}{dt} = 1/2\ \text{LSB} = \frac{2\ V_O}{2^{n+1}}$$

Substituting into this gives

$$\frac{2\ V_O}{2^{n+1}} = 2\pi fV_O T_A$$

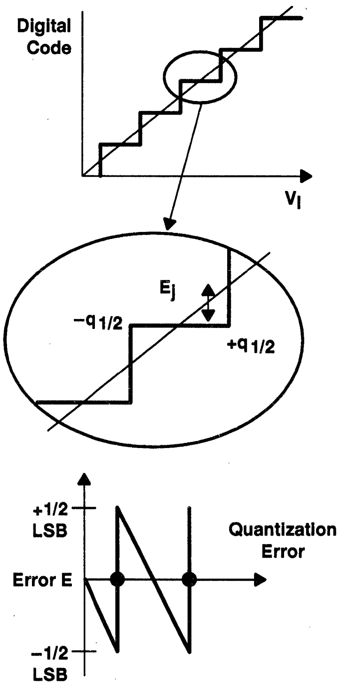
So that the maximum frequency is given by

$$f_{MAX} = \frac{1}{T_A \pi 2^{n+1}}$$

5 QUANTIZATION EFFECTS

The real world analog input to an ADC is a continuous signal with an infinite number of possible states, whereas the digital output is by its nature a discrete function with a number of different states determined by the resolution of the device. It follows from this therefore, that in converting from one form to the other, certain parts of the analog signal that were represented by a different voltage on the input are represented by the same digital code at the output. Some information has been lost and distortion has been introduced into the signal. This is quantization noise.

For the ideal staircase transfer function of an ADC, the error between the actual input and its digital form has a uniform probability density function if the input signal is assumed to be random. It can vary in the range ±1/2 LSB or ±q/2 where q is the width of one step as shown in Figure 9.



Error at the jth step

$E_j = (V_j - V_I)$

The mean square error over the step

$$\bar{E}_j^2 = \frac{1}{q_1}\int_{-q/2}^{+q/2} E_j^2\, dE = \frac{q^2}{12}$$

Assuming equal steps, the total error is

$\bar{N}^2 = q^2/12$ **(Mean square quantization noise)**

For an input sine wave F(t) = A sinωt, the signal power

$$\bar{F}^2(t) = \frac{1}{2\pi}\int_0^{2\pi} A^2 \sin^2\omega t\, d\omega t = \frac{A^2}{2}$$

$$\text{and } q = \frac{2A}{2^n} = \frac{A}{2^{n-1}}$$

$$SNR = 10\ \mathrm{Log}\left(\frac{F^2}{n^2}\right) = 10\ \mathrm{Log}\left(\frac{A^2/2}{A^2/3 \times 2^n}\right)$$

$$SNR = 6.02n + 1.76\ \mathrm{dB}$$

Figure 9. Quantization Effects

Where

$$p(\epsilon) = \frac{1}{q} \text{ for } \left(-\frac{q}{2} \le \epsilon \le +\frac{q}{2}\right)$$

Otherwise

$$p(\epsilon) = 0$$

The average noise power (mean square) of the error over a step is given by

$$\bar{N}^2 = \frac{1}{q}\int_{-q/2}^{q/2} \epsilon^2 d\epsilon$$

which gives

$$\bar{N}^2 = \frac{q^2}{12}$$

The total mean square error, N^2, over the whole conversion area is the sum of each quantization levels mean square multiplied by its associated probability. Assuming the converter is ideal, the width of each code step is identical and therefore has an equal probability. Hence for the ideal case

$$N^2 = \frac{q^2}{12}$$

Considering a sine wave input F(t) of amplitude A so that

$$F(t) = A\sin\omega t$$

which has a mean square value of $F^2(t)$, where

$$F^2(t) = \frac{1}{2\pi}\int_0^{2\pi} A^2 \sin^2(\omega t)dt$$

which is the signal power. Therefore the signal to noise ratio SNR is given by

$$\mathrm{SNR(dB)} = 10\mathrm{Log}\left[\left(\frac{A^2}{2}\right)\Big/\left(\frac{q^2}{12}\right)\right]$$

But

$$q = 1\ \mathrm{LSB} = \frac{2A}{2^n} = \frac{A}{2^{n-1}}$$

Substituting for q gives

$$\mathrm{SNR(dB)} = 10\mathrm{Log}\left[\left(\frac{A^2}{2}\right)\Big/\left(\frac{A^2}{3 \times 2^{2n}}\right)\right] = 10\ \mathrm{Log}\left(\frac{3 \times 2^{2n}}{2}\right)$$

$$\Rightarrow \underline{\underline{6.02n + 1.76\mathrm{dB}}}$$

This gives the ideal value for an n bit converter and shows that each extra 1 bit of resolution provides approximately 6 dB improvement in the SNR.

In practice, the errors mentioned in section 3 introduce nonlinearities that lead to a reduction of this value. The limit of a 1/2 LSB differential linearity error is a missing code condition which is equivalent to a reduction of 1 bit of resolution and hence a reduction of 6 dB in the SNR. This then gives a worst case value of SNR for an n-bit converter with 1/2 LSB linearity error.

$$\mathrm{SNR\ (worst\ case)} = 6.02n + 1.76 - 6 = 6.02n - 4.24\ \mathrm{dB}$$

Hence we have established the boundary conditions for the choice of the resolution of the converter based upon a desired level of SNR.

6 IDEAL SAMPLING

In converting a continuous time signal into a discrete digital representation, the process of sampling is a fundamental requirement. In an ideal case, sampling takes the form of a pulse train of impulses which are infinitesimally narrow yet have unit area. The reciprocal of the time between each impulse is called the sampling rate. The input signal is also idealized by being truly bandlimited, containing no components in its spectrum above a certain value (see Figure 10).

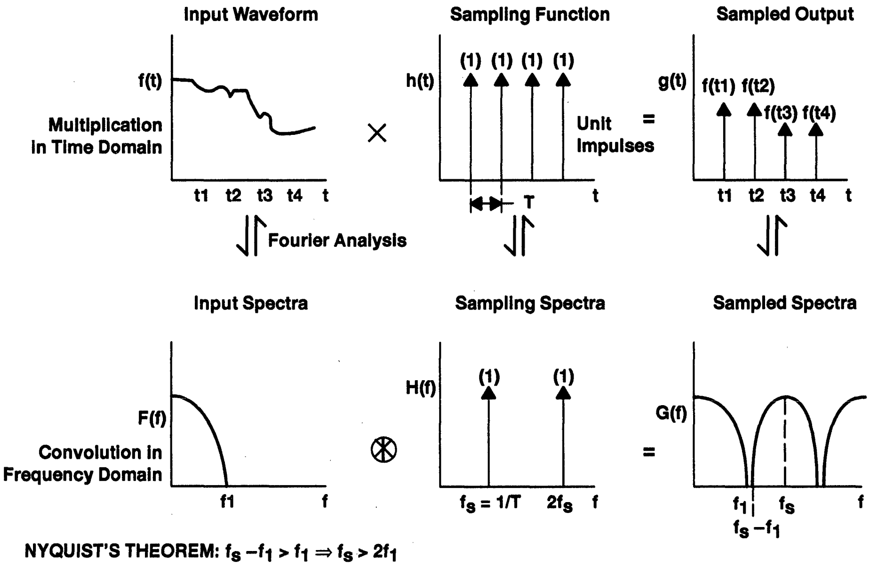


Figure 10. Ideal Sampling

The ideal sampling condition shown is represented in both the frequency and time domains. The effect of sampling in the time domain is to produce an amplitude modulated train of impulses representing the value of the input signal at the instant of sampling. In the frequency domain, the spectrum of the pulse train is a series of discrete frequencies at multiples of the sampling rate. Sampling convolves the spectra of the input signal with that of the pulse train to produce the combined spectrum shown, with double sidebands around each discrete frequency which are produced by the amplitude modulation. In effect some of the higher frequencies are folded back so that they produce interference at lower frequencies. This interference causes distortion which is called aliasing.

If the input signal is bandlimited to a frequency f1 and is sampled at frequency f_S, as shown in the figure, overlap (and hence aliasing) does not occur if

$$f1 < f_S - f1 \qquad \text{i.e.,}\ 2f1 < f_S$$

Therefore if sampling is performed at a frequency at least twice as great as the maximum frequency of the input signal, no aliasing occurs and all of the signal information can be extracted. This is Nyquist's Sampling Theorem, and it provides the basic criteria for the selection of the sampling rate required by the converter to process an input signal of a given bandwidth.

7 REAL SAMPLING

The concept of an impulse is a useful one to simplify the analysis of sampling. However, it is a theoretical ideal which can be approached but never reached in practice. Instead the real signal is a series of pulses with the period equalling the reciprocal of the sampling frequency. The result of sampling with this pulse train is a series of amplitude modulated pulses (see Figure 11).

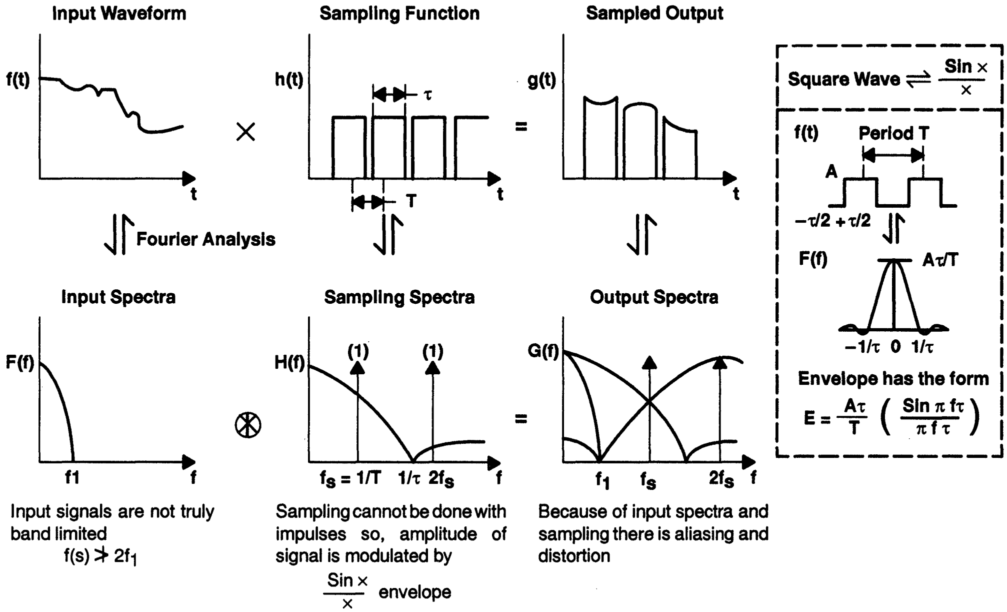


Figure 11. Real Sampling

Examining the spectrum of the square wave pulse train shows a series of discrete frequencies, as with the impulse train, but the amplitude of these frequencies is modified by an envelope which is defined by (sin x)/x [sometimes written sinc(x)] where x in this case is πf_S. For a square wave of amplitude A, the envelope of the spectrum is defined as

$$\text{Envelope} = A\left(\frac{\tau}{T}\right)\left[\sin(\pi f_S \tau)\right] \;/\; \pi f_S \tau$$

The error resulting from this can be controlled with a filter which compensates for the sinc envelope. This can be implemented as a digital filter, in a DSP, or using conventional analog techniques.

8 ALIASING EFFECTS AND CONSIDERATIONS

No signal is truly deterministic and therefore in practice has infinite bandwidth. However, the energy of higher frequency components becomes increasingly smaller so that at a certain value it can be considered to be irrelevant. This value is a choice that must be made by the system designer.

As shown, the amount of aliasing is affected by the sampling frequency and by the relevant bandwidth of the input signal, filtered as required. The factor that determines how much aliasing can be tolerated is ultimately the resolution of the system. If the system has low resolution, then the noise floor is already relatively high and aliasing does not have a significant effect. However, with a high resolution system, aliasing can increase the noise floor considerably and therefore needs to be controlled more completely.

One way to prevent aliasing is to increase the sampling rate, as shown. However, the frequency is limited by the type of converter used and also by the maximum clock rate of the digital processor receiving and transmitting the data. Therefore, to reduce the effects of aliasing to within acceptable levels, analog filters must be used to alter the input signal spectrum (see Figure 12).

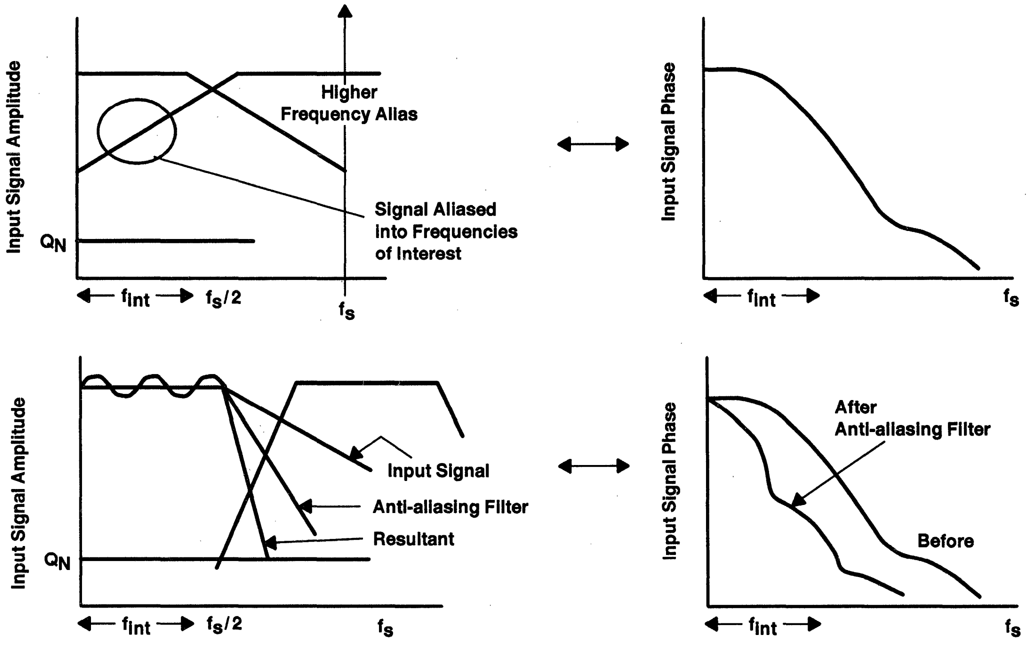


Figure 12. Aliasing Effects and Considerations

8.1 Choice of Filter

As shown with sampling, there is an ideal solution to the choice of a filter and a practical realization that compromises must be made. The ideal filter is a so-called brickwall filter which introduces no attenuation in the passband, and then cuts down instantly to infinite attenuation in the stopband. In practice, this is approximated by a filter that introduces some attenuation in the passband, has a finite rolloff, and passes some frequencies in the stopband. It can also introduce phase distortion as well as amplitude distortion. The choice of the filter order and type must be decided upon so as to best meet the requirements of the system.

8.2 Types of Filter

The basic types of filters available to the designer are briefly presented for comparison purposes. This is not intended to be a full analysis of the subject; therefore, other texts should be referenced for more details.

8.2.1 Butterworth Filter

A Butterworth (maximally flat) filter is the most commonly used general purpose filter. It has a monotonic passband with the attenuation increasing up to its 3-dB point which is known as the natural frequency. This frequency is the same regardless of the order of the filter. However, by increasing the order of the filter, the roll-off in the passband moves closer to its natural frequency and the roll-off in the transition region between the natural frequency and the stopband becomes sharper.

8.2.2 Chebyshev Filter

The Chebyshev equal ripple filter distributes the roll-off across the whole passband. It introduces more ripple in the passband but provides a sharper roll-off in the transition region. This type of filter has poorer transient and step responses due to its higher Q values in the stages of the filter.

8.2.3 Inverse Chebyshev Filter

Both the Butterworth and Chebyshev filters are monotonic in the transition region and stopband. Since ripple is allowed in the stopband, it is possible to make the roll-off sharper. This is the principle of the Inverse Chebyshev, based on the reciprocal of the angular frequency in the Chebyshev filter response. This filter is monotonic in the passband and can be flatter than the Butterworth filter while providing a greater initial roll-off than the Chebyshev filter.

8.2.4 Cauer Filter

The Cauer or (Elliptic) filter is nonmonotonic in both the pass and stop bands, but provides the greatest roll-off in any of the standard filter configurations.

8.2.5 Bessel-Thomson Filter

All of the types mentioned above introduce nonlinearities into the phase relationship of the component frequencies of the input spectrum. This can be a problem in some applications when the signal is reconstructed. The Bessel-Thomson or linear delay filter is designed to introduce no phase distortion but this is achieved at the expense of a poorer amplitude response.

In general, the performance of all of these types can be improved by increasing the number of stages, i.e., the order of the filter. The penalty for this of course is the increased cost of components and board space required. For this reason, an integrated solution using switched capacitor filter building blocks which provide comparable performance with a discrete solution over a range of frequencies from about 1 kHz to 100 kHz might be appropriate. They also provide the designer with a compact and cost effective solution.

8.3 TLC04 Anti-Aliasing Butterworth Filter

The TLC04 fourth order Butterworth filter features include the following:

- Low clock to cutoff frequency error . . . 0.8%
- Cutoff depends only on stability of external clock
- Cutoff range of 0.1 Hz to 30 kHz
- 5-V to 12-V operation
- Self clocking or both TTL and COS compatible

As detailed previously the Butterworth filter generally provides the best compromise in filter configurations and is by far the easiest to design. The Butterworth filter's characteristic is based on a circle which means that when designing filters, all stages to the filter have the same natural frequency enabling simpler filter design. Most modern designs which use operational amplifiers are based on building the whole transfer function by a series of second order numerator and denominator stages (a Biquad stage). The Butterworth design is simplified, when using these stages, because each stage has the same natural frequency. This can easily be converted to a switched capacitor filter (SCF) which has very good capacitor matching and accurately synthesized RC time constants.

The switched capacitor technique is demonstrated in Figure 13. Two clocks operating at the same frequency but in complete antiphase, alternately connect the capacitor C_2 to the input and the inverting input of an operational amplifier. During Φ_1, charge Q flows onto the capacitor equal to $V_I C_2$. The switch is considered to be ideal so that there is no series resistance and the capacitor charges instantaneously. During Φ_2, the switches change so that C_2 is now connected to the virtual earth at the operational amplifier input. It discharges instantaneously delivering the stored charge Q.

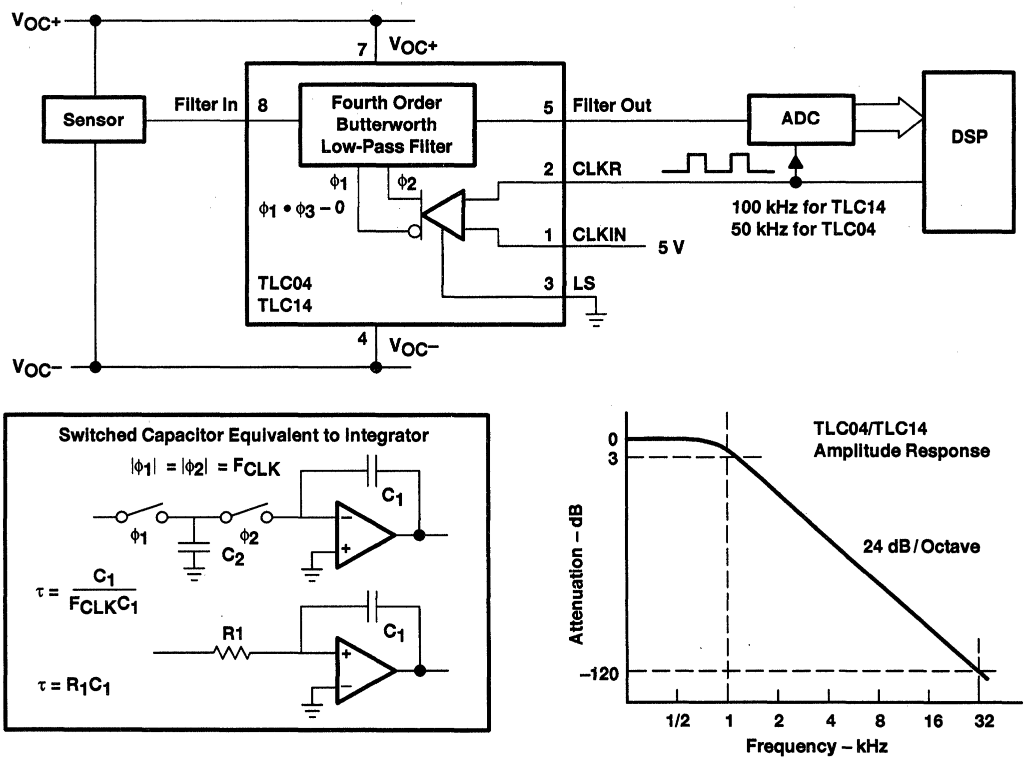


Figure 13. TLC04 Anti-aliasing Butterworth Filter

The average current that flows I_{AV} depends on the frequency of the clocks T so that

$$I_{AV} = \frac{Q}{T} = V_I \frac{C_2}{T} = V_I C_2 F_{CLK}$$

Therefore, the switched capacitor looks like a resistor of value

$$R_{eq} = \frac{V_I}{I_{AV}} = \frac{1}{C_2 F_{CLK}}$$

The advantage of the technique is that the time constant of the integrator can be programmed by altering this equivalent resistance, and this is done by simply altering the clock frequency. This provides precision in the filter design, because the time constant then depends on the ratio of two capacitors which can be fabricated in silicon to track each other very closely with voltage and temperature. Note that the analysis assumes V_I to be constant so that for an ac signal, the clock frequency must be much higher than the frequency of the input.

The TLC04 is one such filter which is internally configured to provide the Butterworth low-pass filter response, and the cut-off frequency for the device is controlled by a digital clock. For this device, the cut-off frequency is set simply by the clock frequency so that the clock to cut-off frequency ratio is 50:1 with an accuracy of 0.8%. This enables the cut-off frequency of the filter to be tied to the sampling rate, so that only one fundamental clock signal is required for the system as a whole. Another advantage of SCF techniques means that fourth order filters can be attained using only one integrated circuit and they are much more easily controlled.

The response of an nth order Butterworth filter is described by the following equation.

$$\text{Attenuation} = \left[1 + \left(\frac{f}{f_c}\right)2^n\right]^{1/2}$$

The table below lists the fourth order realization in the TLC04.

FREQUENCY	ATTENUATION (FACTOR)	ATTENUATION (dB)	PHASE (DEGREE)
$F_c/2$	0.998	0.02	26.6
F_c	0.707	3	45
$2F_c$	0.0624	24	63.4
$4F_c$	0.00391	48	76
$8F_c$	0.000244	72	82.9
$12F_c$	0.000048	86	85.2
$16F_c$	0.000015	96	86.4

This means that sampling at 8 times the cut off frequency gives an input-to-aliased signal ratio of 72 dB, which is less than ten bit quantization noise distortion.

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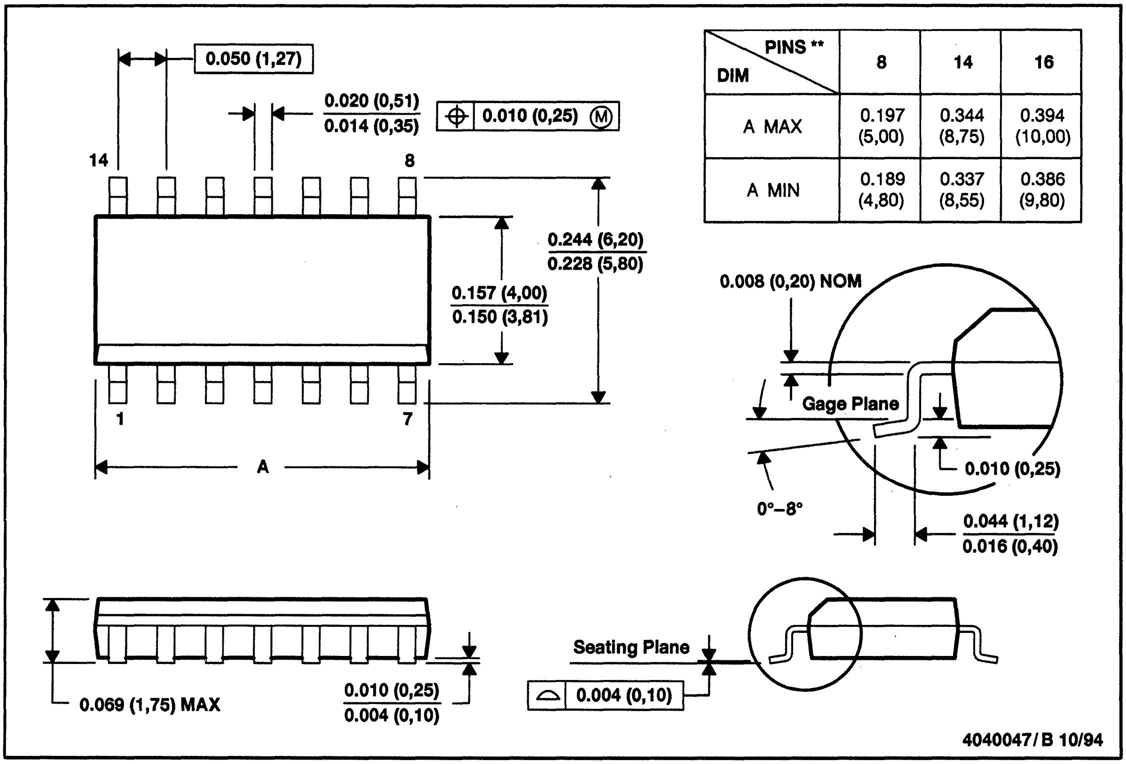
D (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Four center pins are connected to die mount pad
- E. Falls within JEDEC MS-012

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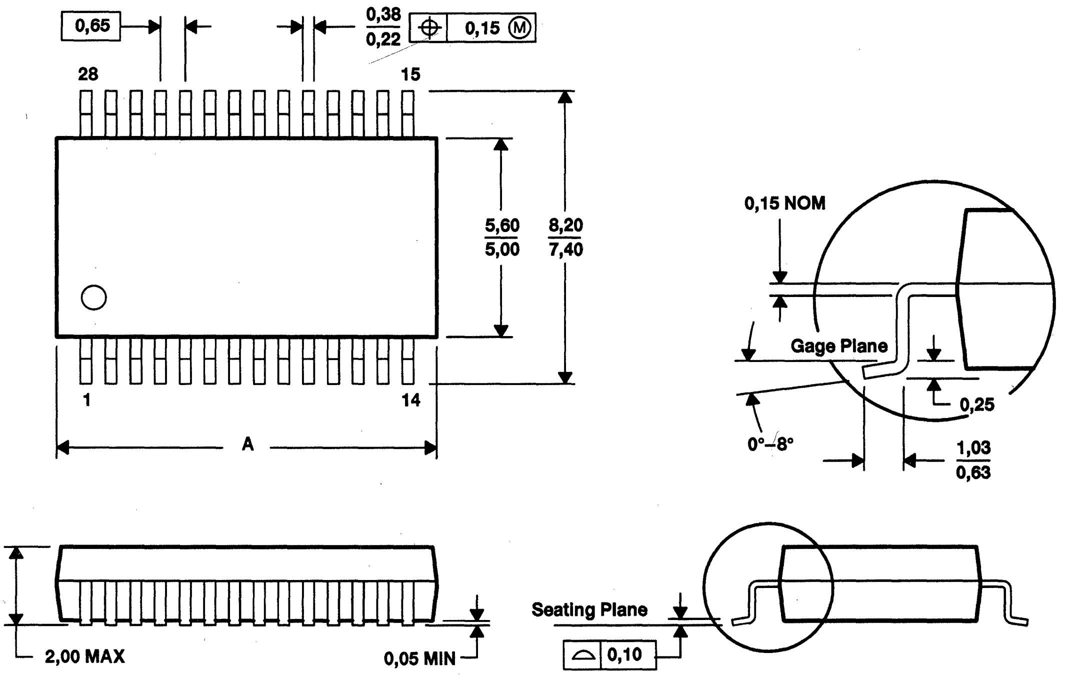
DB (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

28 PIN SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 / B 10/94

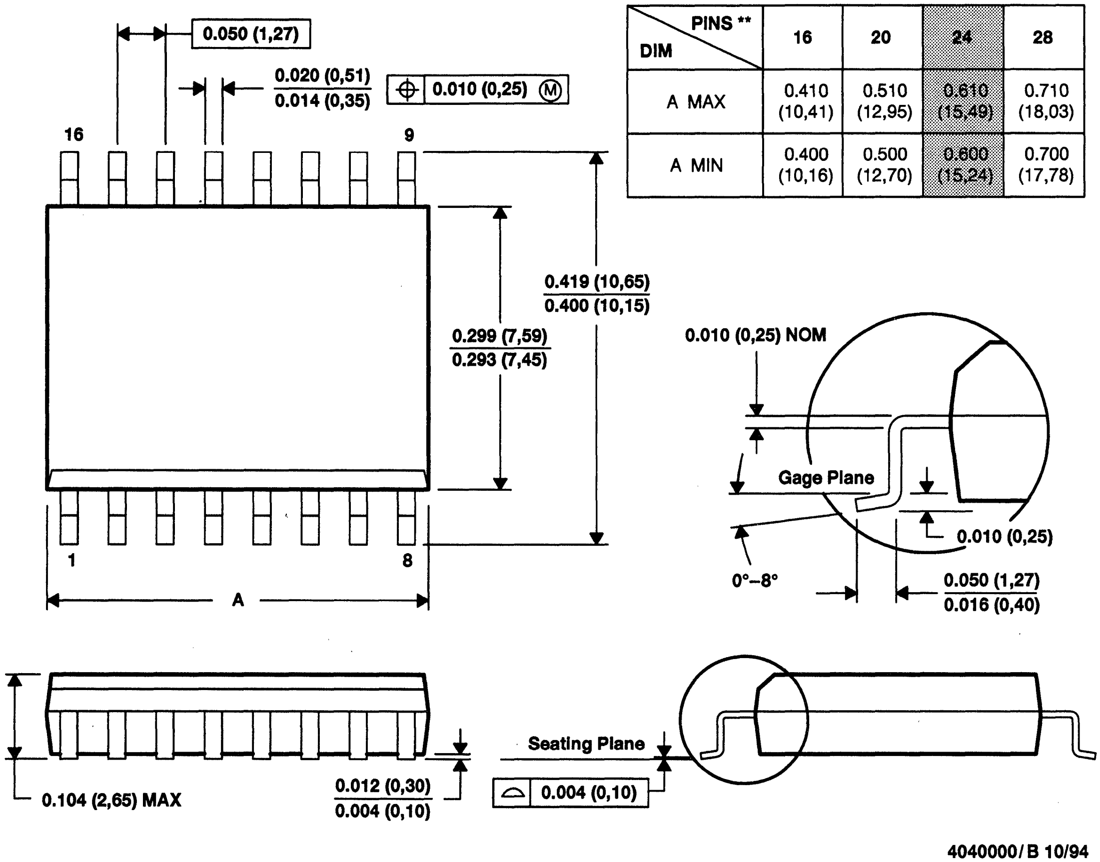
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

AUGUST 1995

DW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

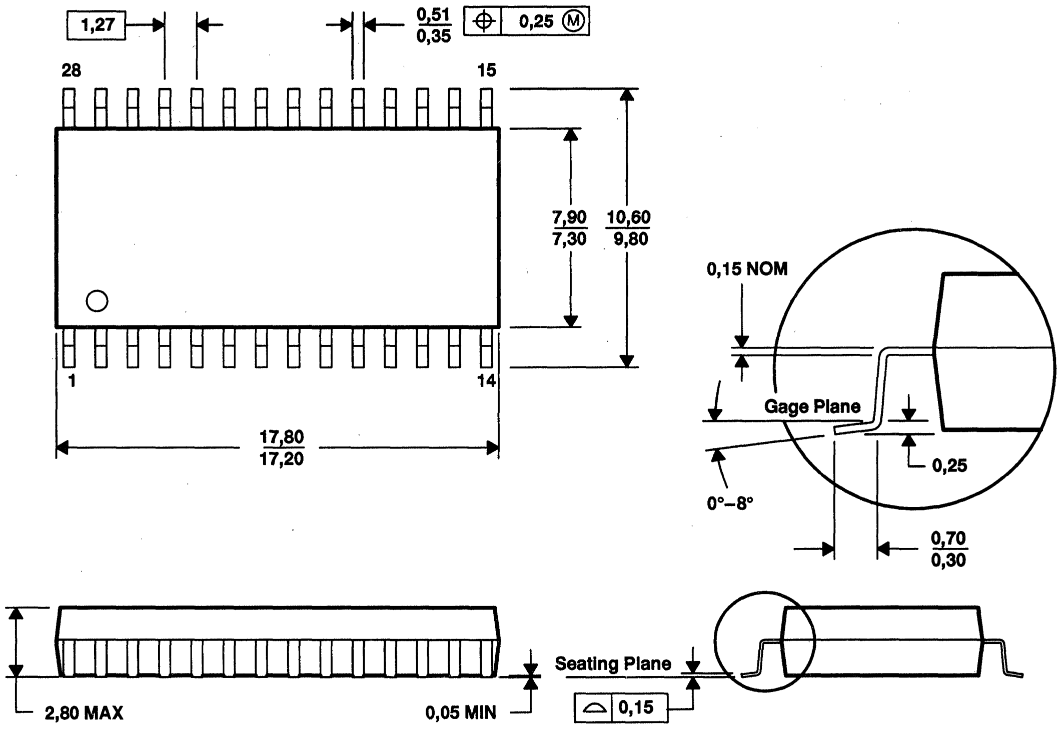
16 PIN SHOWN

DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

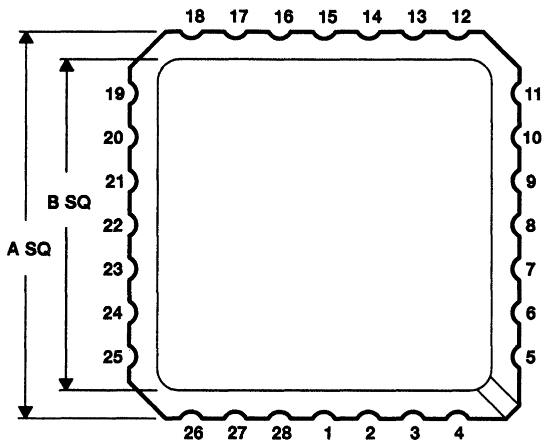
DWB (R-PDSO-G28) **PLASTIC SMALL-OUTLINE PACKAGE**



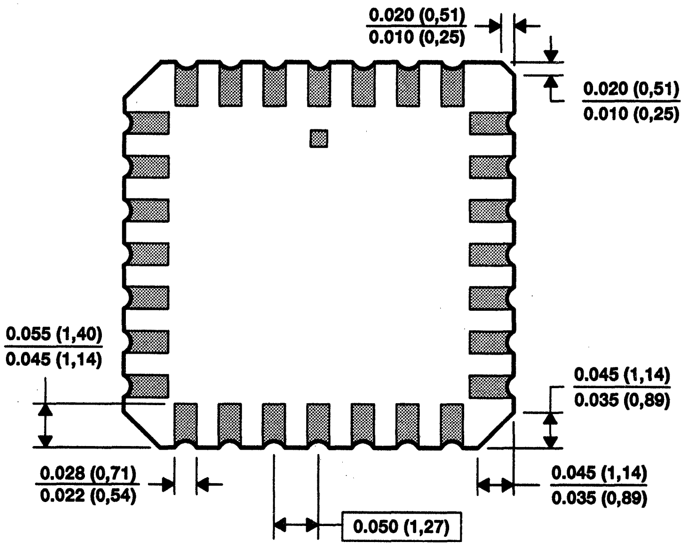
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

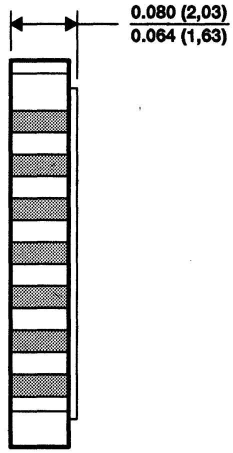
FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.422 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.730 (18,78)	0.761 (19,32)	0.485 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)





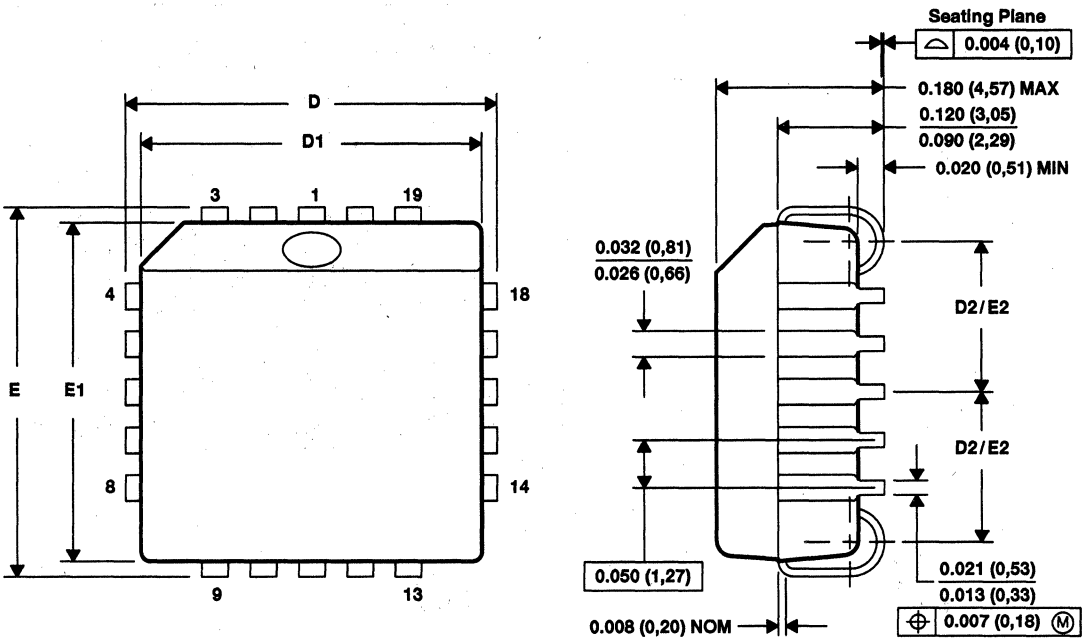
4040140/B 10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

AUGUST 1995

FN (S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



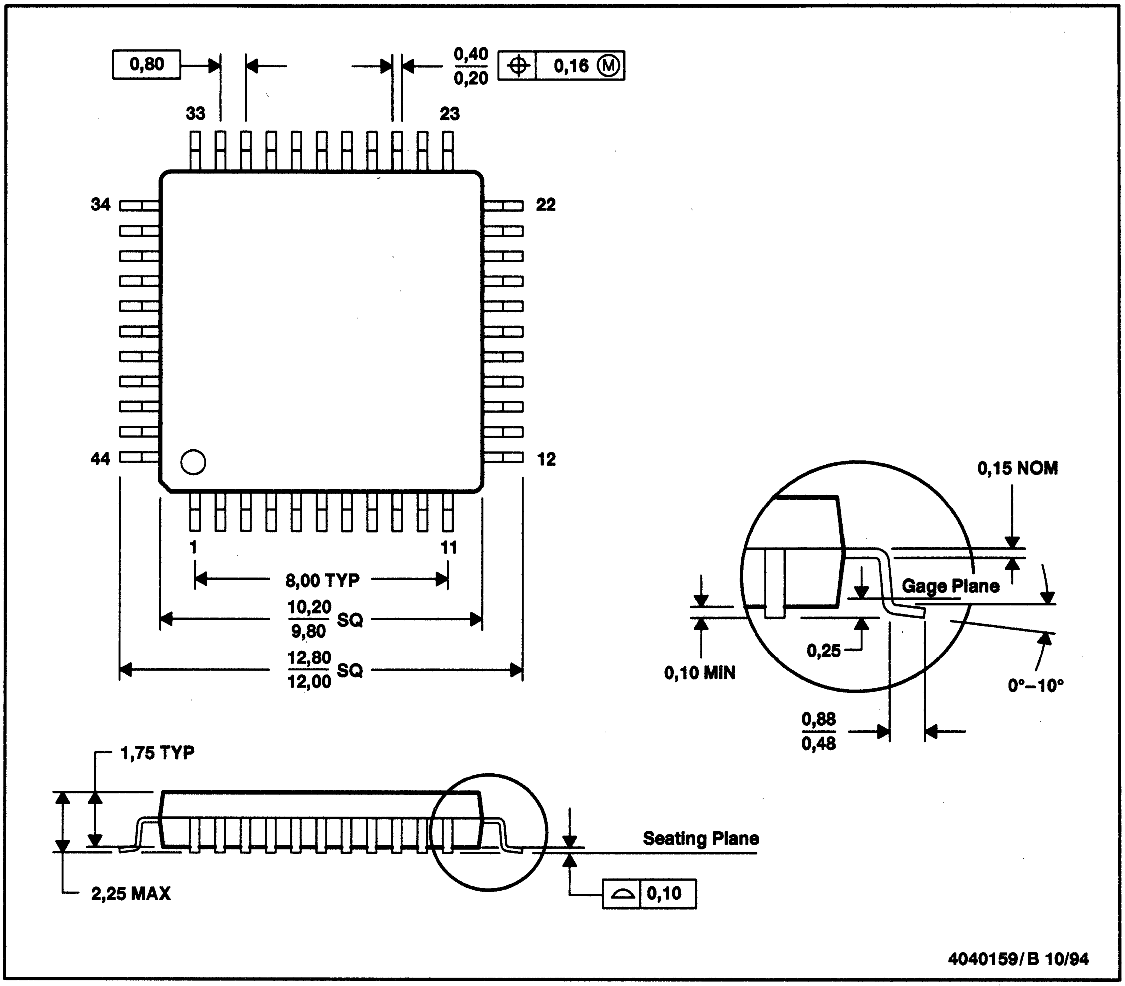
NO. OF PINS **	D / E		D1 / E1		D2 / E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005 / B 10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

AUGUST 1995

FR (S-PDFP-G44) **PLASTIC QUAD FLATPACK**

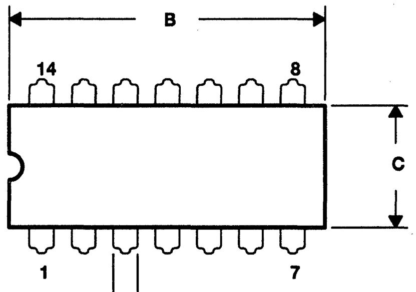


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

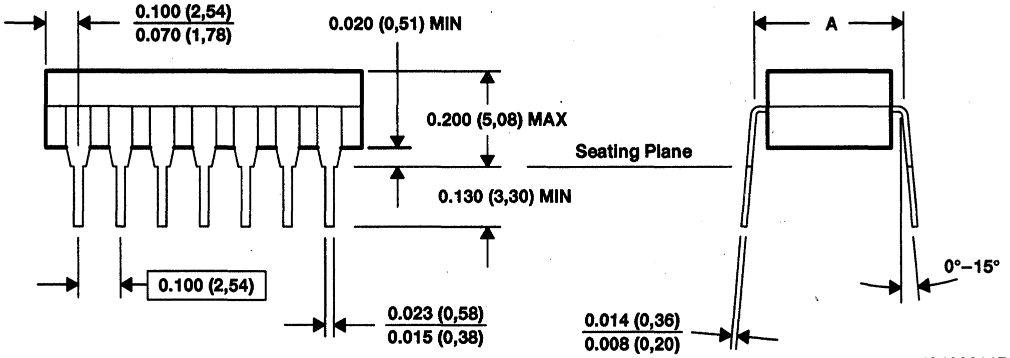
AUGUST 1995

J (R-GDIP-T**) CERAMIC DUAL-IN-LINE PACKAGE

14 PIN SHOWN



PINS ** / DIM	14	16	18	20	22
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.410 (10,41)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.390 (9,91)
B MAX	0.785 (19,94)	0.785 (19,94)	0.910 (23,10)	0.975 (24,77)	1.100 (28,00)
B MIN	0.755 (19,18)	0.755 (19,18)	—	0.930 (23,62)	—
C MAX	0.280 (7,11)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.388 (9,65)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	—

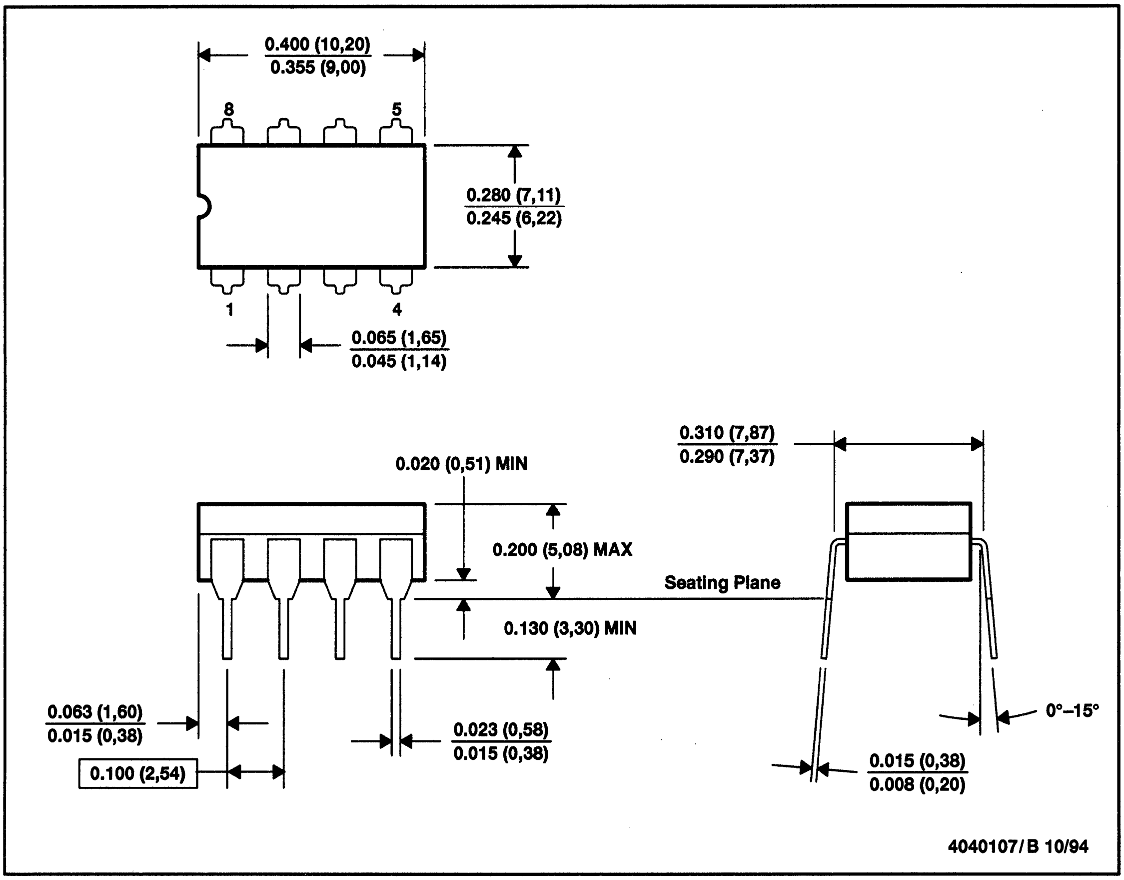


4040083/B 10/94

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
- E. Falls within MIL-STD-1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, GDIP1-T20, and GDIP1-T22

AUGUST 1995

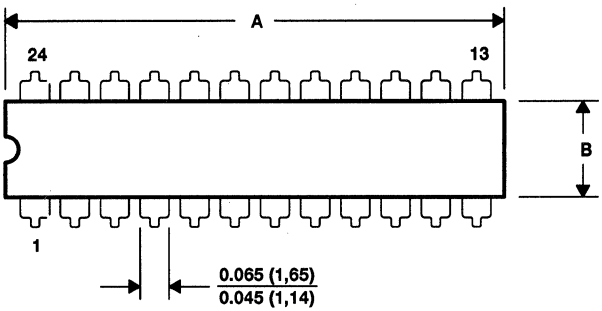
JG (R-GDIP-T8) — CERAMIC DUAL-IN-LINE PACKAGE



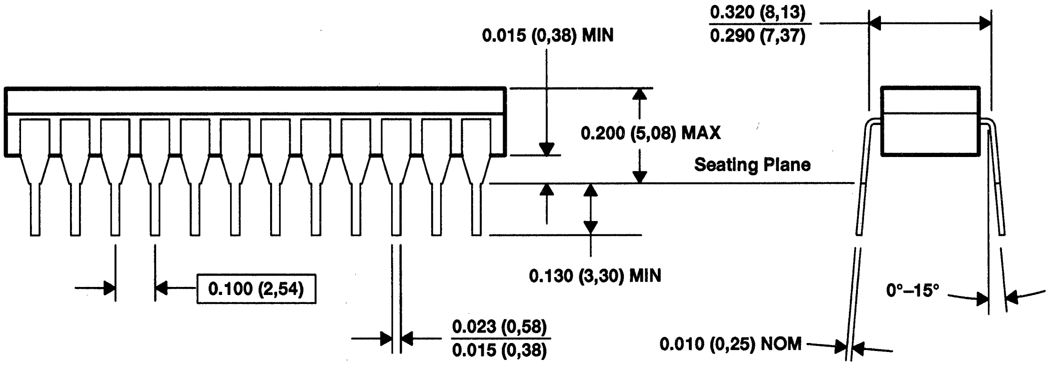
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
E. Falls within MIL-STD-1835 GDIP1-T8

JT (R-GDIP-T)** **CERAMIC DUAL-IN-LINE PACKAGE**

24 PIN SHOWN



DIM \ PINS**	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)



4040110/B 10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
E. Falls within MIL-STD-1835 GDIP-T24 and GDIP-T28 and JEDEC MO-058AA and MO-058AB

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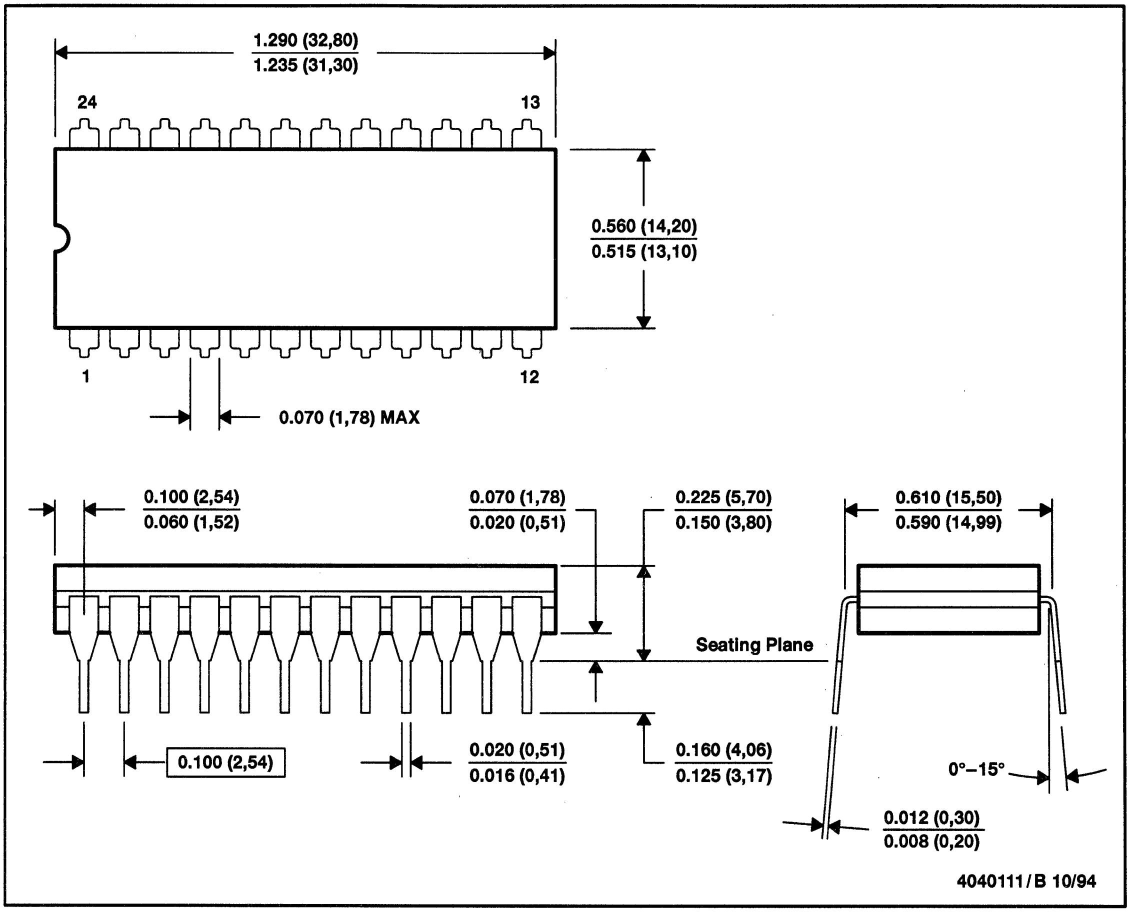
JW (R-GDIP-T24) **CERAMIC DUAL-IN-LINE PACKAGE**

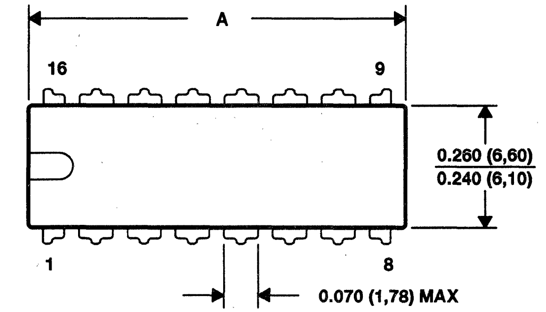


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
E. Falls within MIL-STD-1835 GDIP5-T24

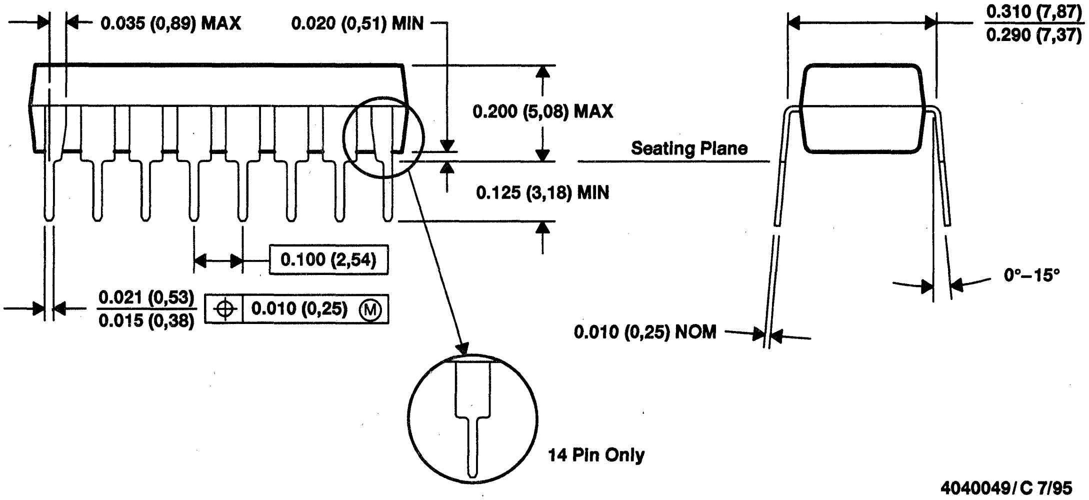
AUGUST 1995

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



4040049/C 7/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001)

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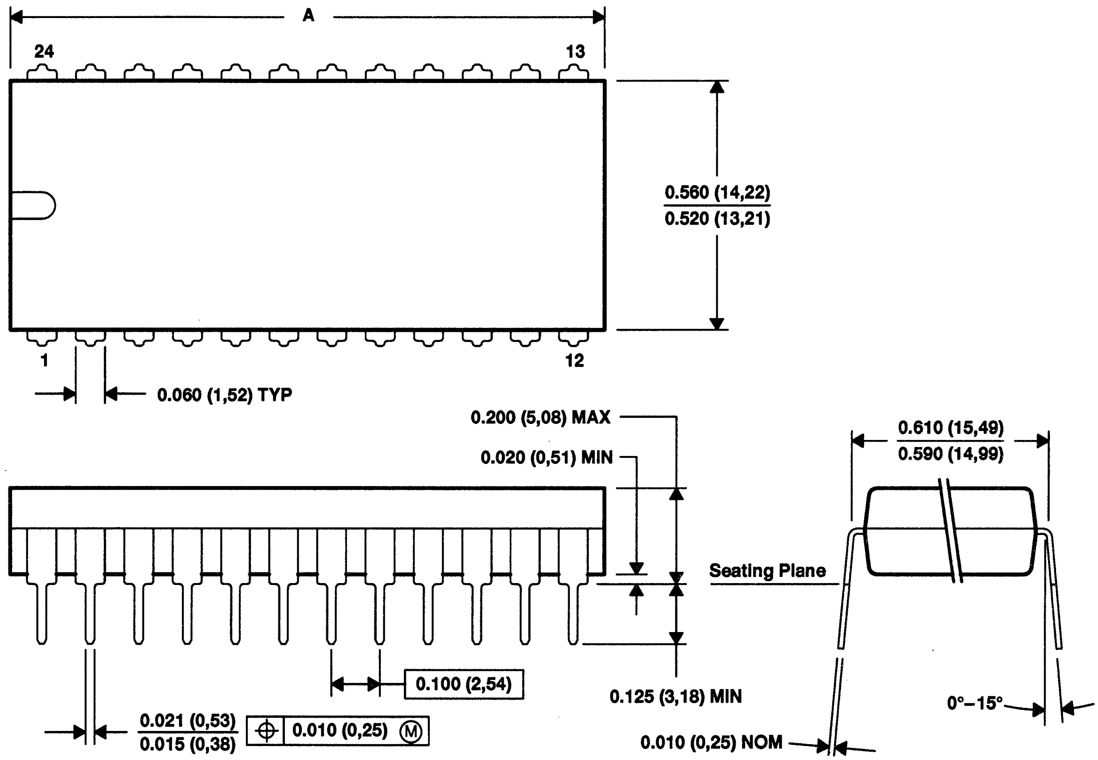
N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN



DIM \ PINS **	24	28	32	40	48	52
A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)	2.650 (67,31)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)

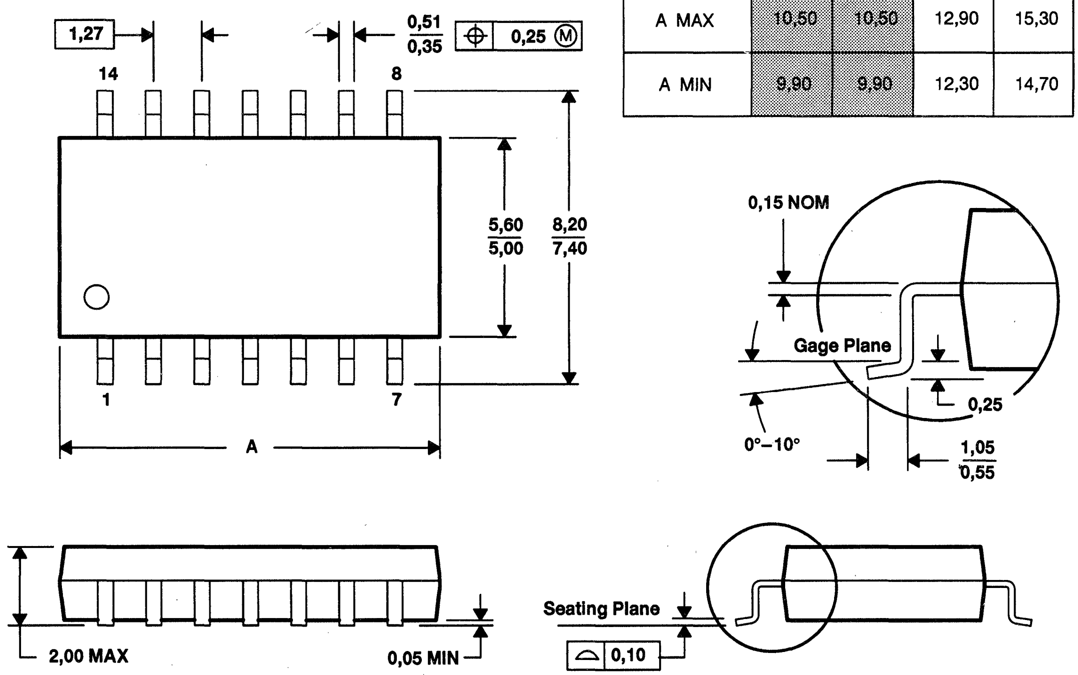
4040053/ B 10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-011
D. Falls within JEDEC MS-015 (32 pin only)

AUGUST 1995

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



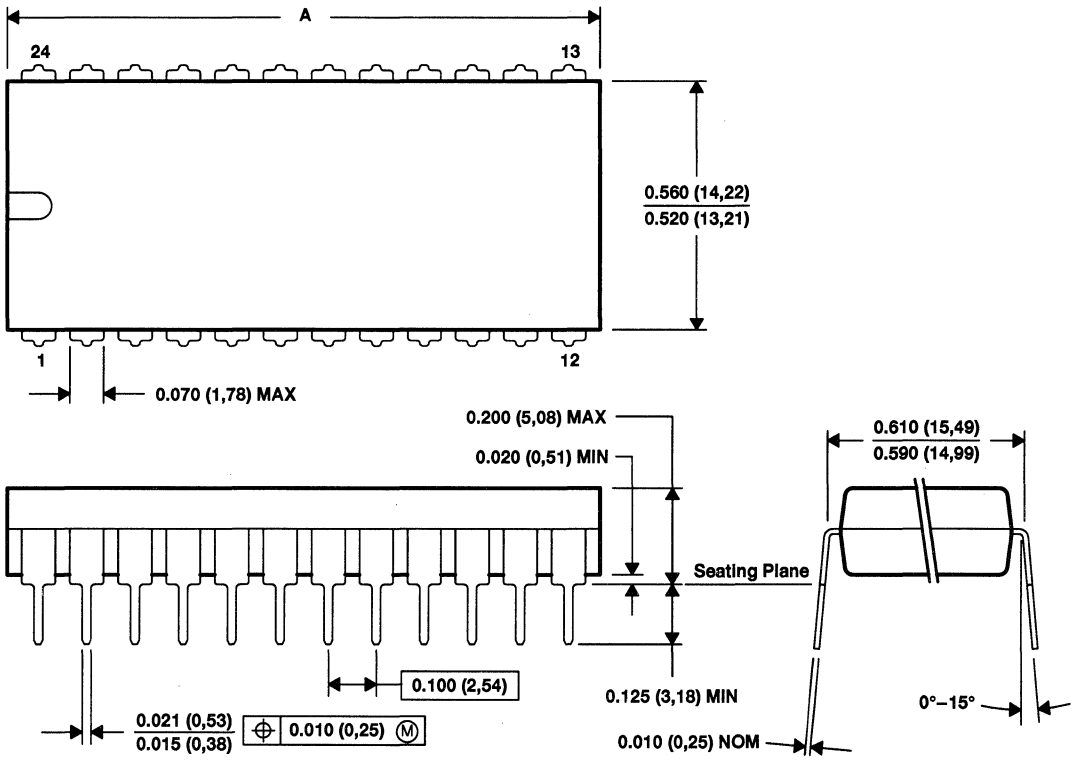
PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/B 10/94

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

NW (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

24 PIN SHOWN

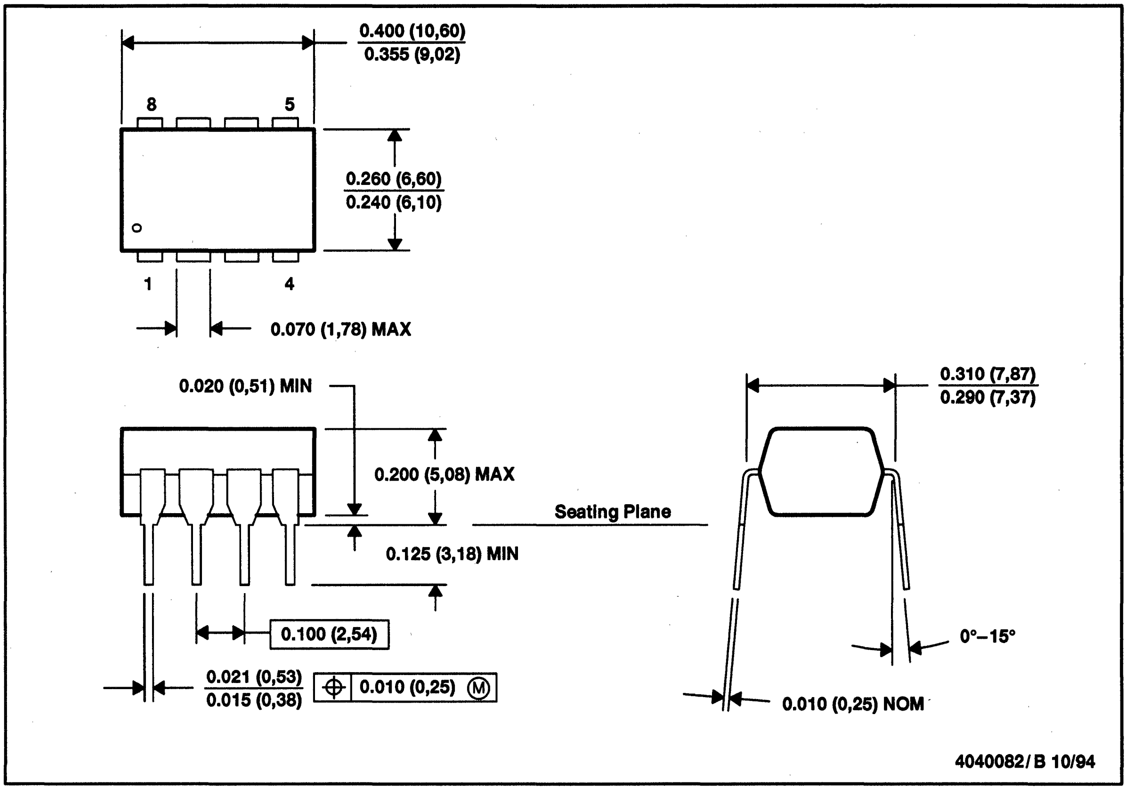


DIM \ PINS **	24	28	40	48
A MAX	1.290 (32,77)	1.440 (36,60)	2.090 (53,09)	2.450 (62,23)
A MIN	1.260 (32,00)	1.400 (35,56)	2.040 (51,82)	2.390 (60,71)

4040079/B 10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-011

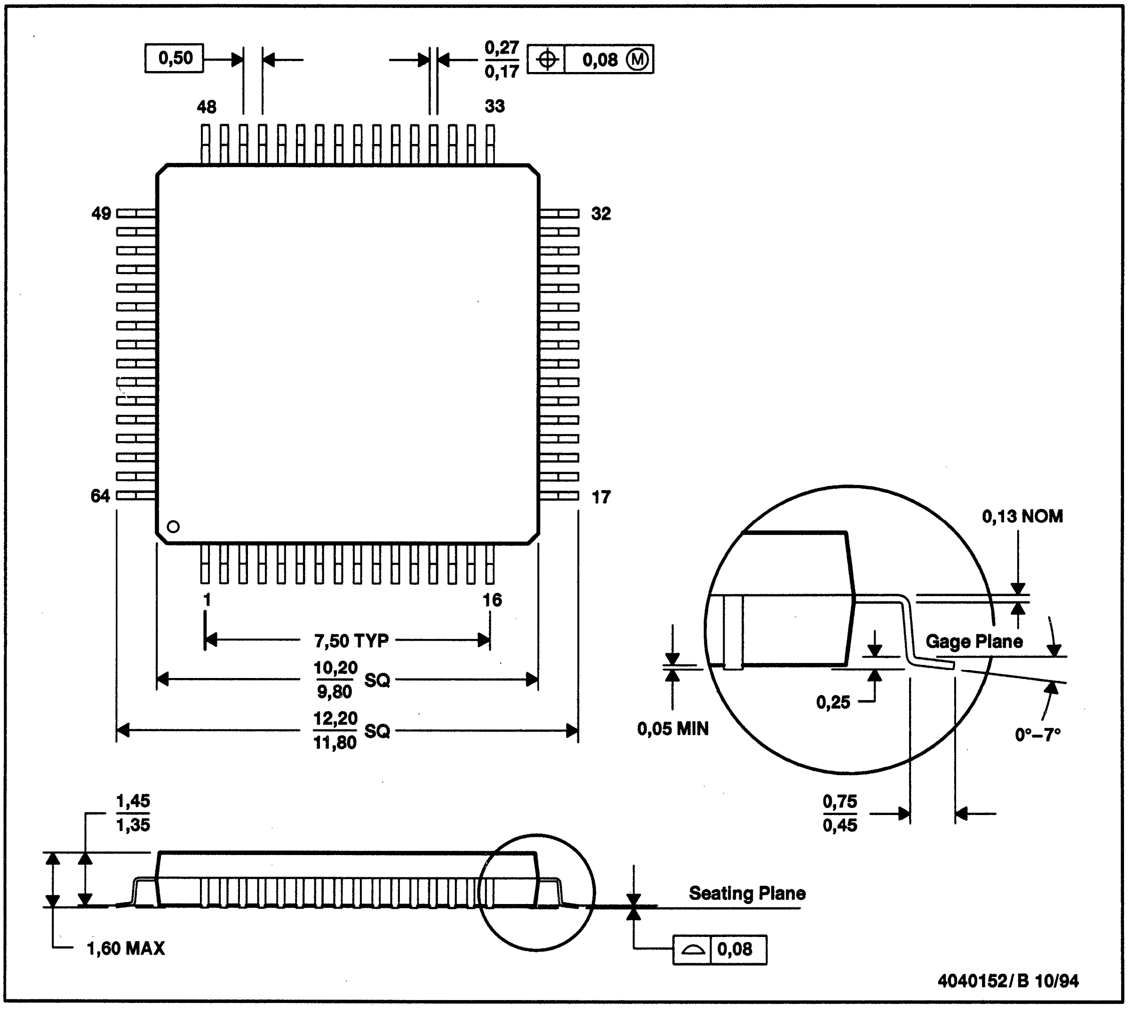
P (R-PDIP-T8) PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

AUGUST 1995

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**

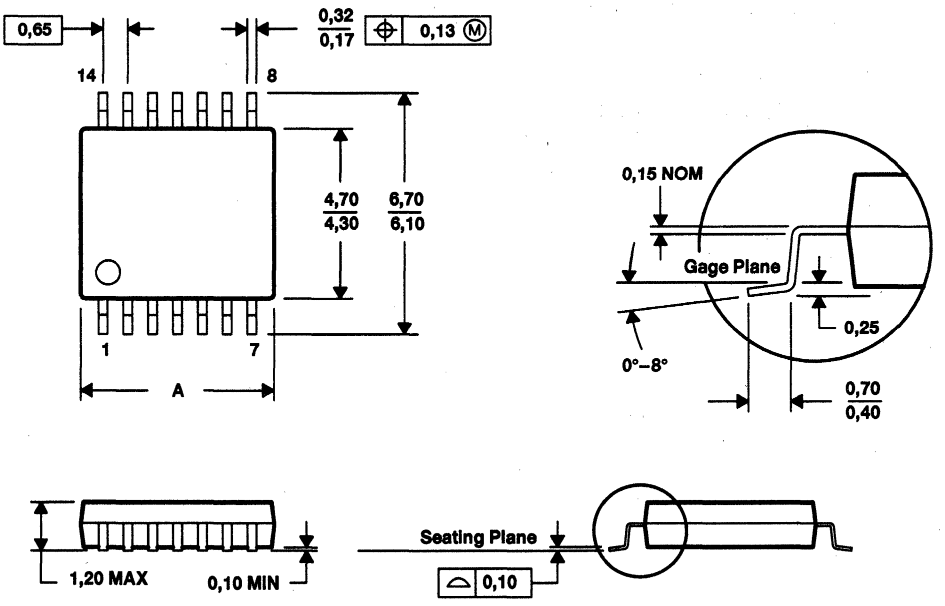


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

AUGUST 1995

PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



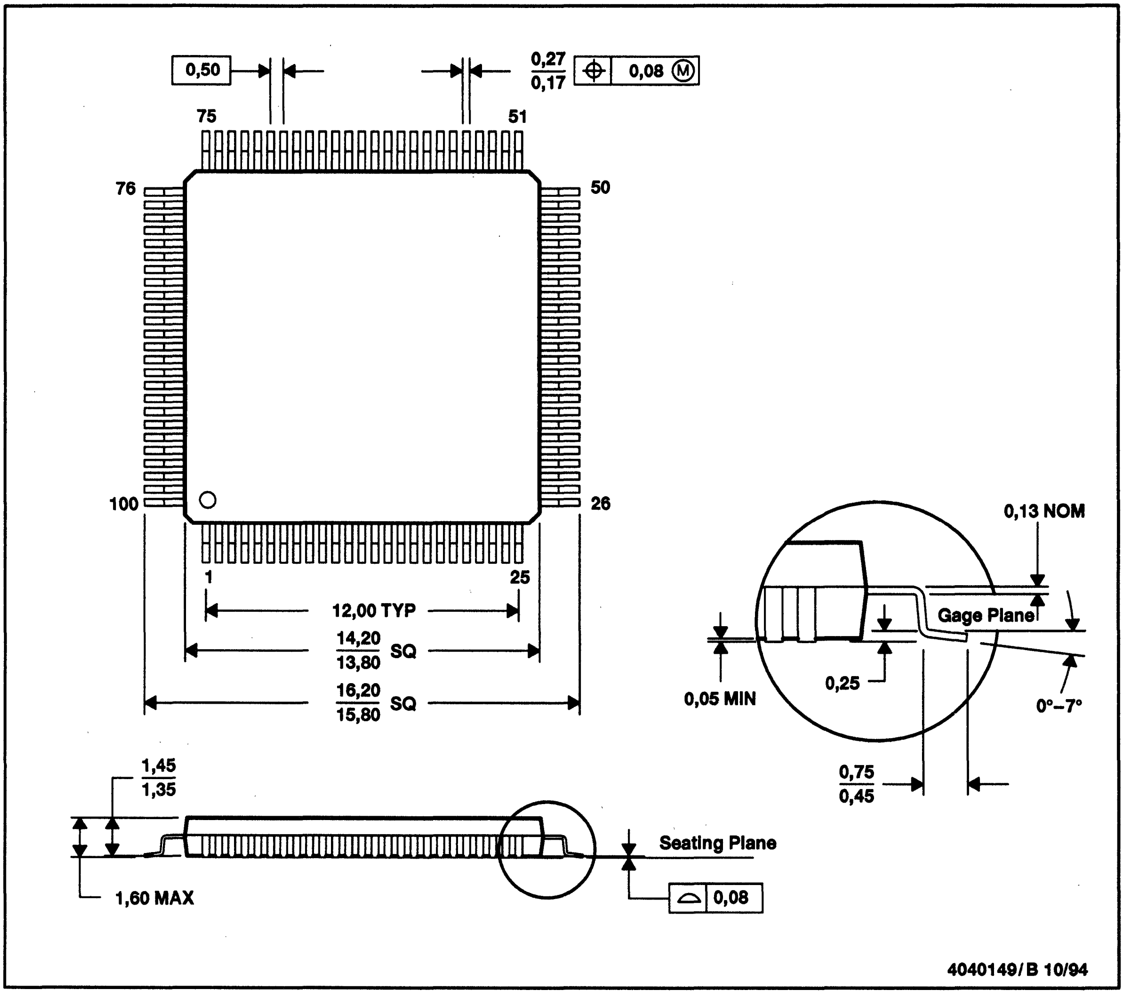
PINS ** / DIM	8	14	16	20	24	28
A MAX	3,30	5,30	5,30	6,80	8,10	10,00
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/B 10/94

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

AUGUST 1995

PZ (S-PQFP-G100) PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

A

Appendix

Appendix A

Analog Interface Peripherals and Applications

Texas Instruments offers many products for total system solutions, including memory options, data acquisition, and analog input/output devices. This appendix describes a variety of devices that interface directly to the TMS320 DSPs in rapidly expanding applications.

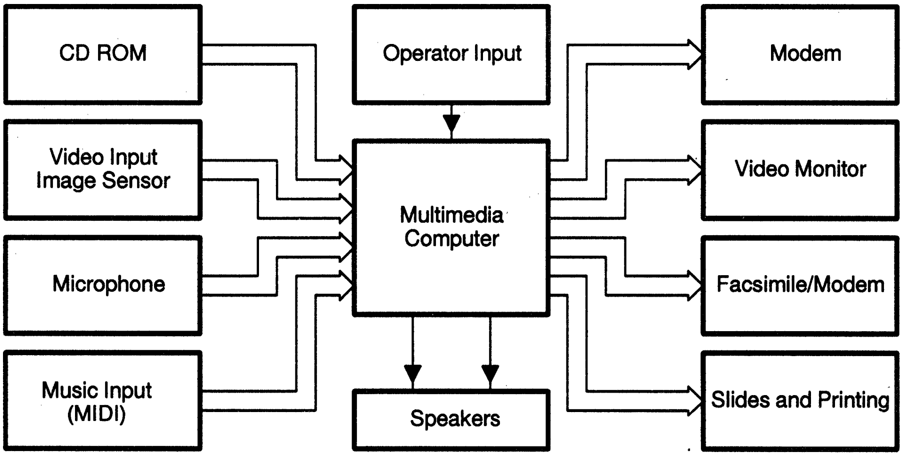
Section **Page**

A.1 Multimedia Applications

Multimedia integrates different media through a centralized computer. These media can be visual or audio and can be input to or output from the central computer via a number of technologies. The technologies can be digital based or analog based (such as audio or video tape recorders). The integration and interaction of media enhances the transfer of information and can accommodate both analysis of problems and synthesis of solutions.

Figure A–1. System Block Diagram

Figure A–1 shows both the central role of the multimedia computer and the multimedia system's ability to integrate the various media to optimize information flow and processing.



A.1.1 System Design Considerations

Multimedia systems can include various grades of audio and video quality. The most popular video standard currently used (VGA) covers 640×480 pixels with 1, 2, 4, and 8-bit memory-mapped color. Also, 24-bit true color is supported, and 1024×768 (beyond VGA) resolution has emerged. There are two grades of audio. The lower grade accommodates 11.25-kHz sampling for 8-bit monaural systems, while the higher grade accommodates 44.1-kHz sampling for 16-bit stereo.

Audio specifications include a musical instrument digital interface (MIDI) with compression capability, which is based on keystroke encoding, and an input/output port with a 3-disc voice synthesizer. In the media control area, video disc, CD audio, and CD ROM player interfaces are included. Figure A–2 shows a multimedia subsystem.

The TLC320AC01 wide-band analog interface circuit (AIC) is well suited for multimedia applications because it features wide-band audio and up to 25-kHz sampling rates. The TLC320AC01 is a complete analog-to-digital and digital-to-analog interface system for the TMS320 DSPs. The nominal bandwidths of the filters accommodate 11.4 kHz, and this bandwidth is programmable. The application circuit shown in Figure A–2 handles both speech encoding and modem communication functions, which are associated with multimedia applications.

Figure A–2. Multimedia Speech Encoding and Modem Communication

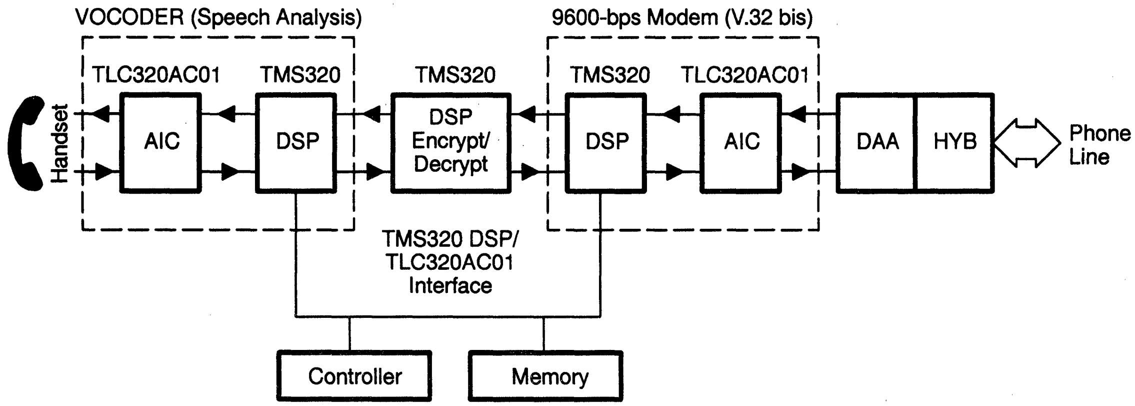
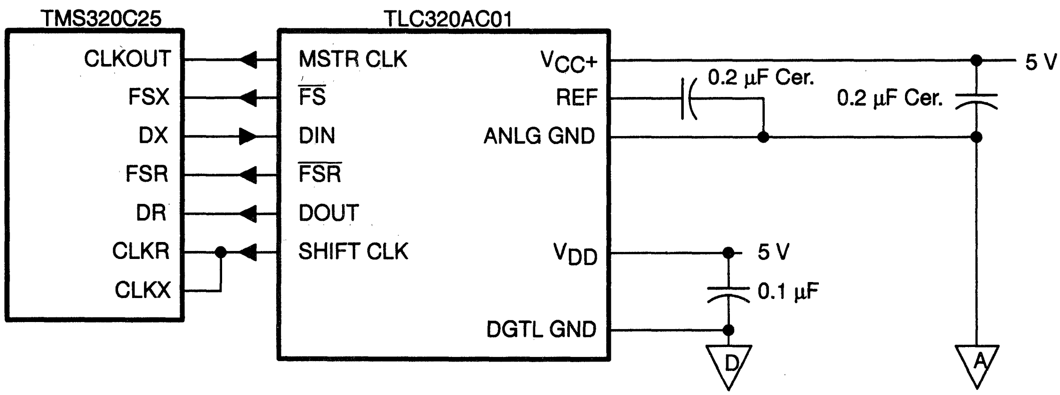


Figure A–3 shows the interfacing of the TMS320C25 DSP to the TLC320AC01 AIC that constitutes the building blocks of the 9600-bps V.32 bis modem shown in Figure A–2.

Figure A–3. TMS320C25 to TLC32047 Interface



A.1.2 Multimedia-Related Devices

As shown in Table A–1, TI provides a complete array of analog and graphics interface devices. These devices support the TMS320 DSPs for complete multimedia solutions.

Table A–1. Data Converter ICs

Device	Description	I/O	Resolution (Bits)	Conversion CLK Rate	Application
TLC320AC01	Analog interface (5 V only, Low Power, 0 to 70°C)	Serial	14	25 kHz	Portable modem and speech, multimedia
TLC320AD57	Analog interface (5 V only, Low power, –40 to 85°C	Serial	14	25 kHz	Portable modem and speech
TLC32047	Analog interface (11.4 kHz BW) (AIC)	Serial	14	25 kHz	Speech, modem, and multimedia
TLC32046	Analog interface (AIC)	Serial	14	25 kHz	Speech and modems
TLC32044	Analog interface (AIC)	Serial	14	19.2 kHz	Speech and modems
TLC32040	Analog interface (AIC)	Serial	14	19.2 kHz	Speech and modems
TLC34075/6	Video palette	Parallel	Triple 8	135 MHz	Graphics
TLC34058	Video palette	Parallel	Triple 8	135 MHz	Graphics
TLC5510	Flash ADC	Parallel	8	20 MHz	Video
TLC5602	Video DAC	Parallel	8	20 MHz	Video
TLC5501	Video ADC	Parallel	6	20 MHz	Video
TLC1550/1	ADC	Parallel	10	150 kHz	Servo ctrl / speech
TLC320AD57	Dual ADC and filter	Serial	16	48 kHz	Audio
TMS57014	Dual audio DAC+ digital filter	Serial	16/18	32, 37.8, 44.1, 48 kHz	Digital audio

Table A–2. Switched-Capacitor Filter ICs

Device	Function	Order	Roll-Off	Power Out	Power Down
TLC2470	Differential audio filter amplifier	4	5 kHz	500 mW	Yes
TLC2471	Differential audio filter amplifier	4	3.5 kHz	500 mW	Yes
TLC04/14	Low pass, Butterworth filter	4	CLK ÷ 50 CLK ÷ 100	N/A	No

For application assistance or additional information, please call TI Linear Applications at (214) 997–3772.

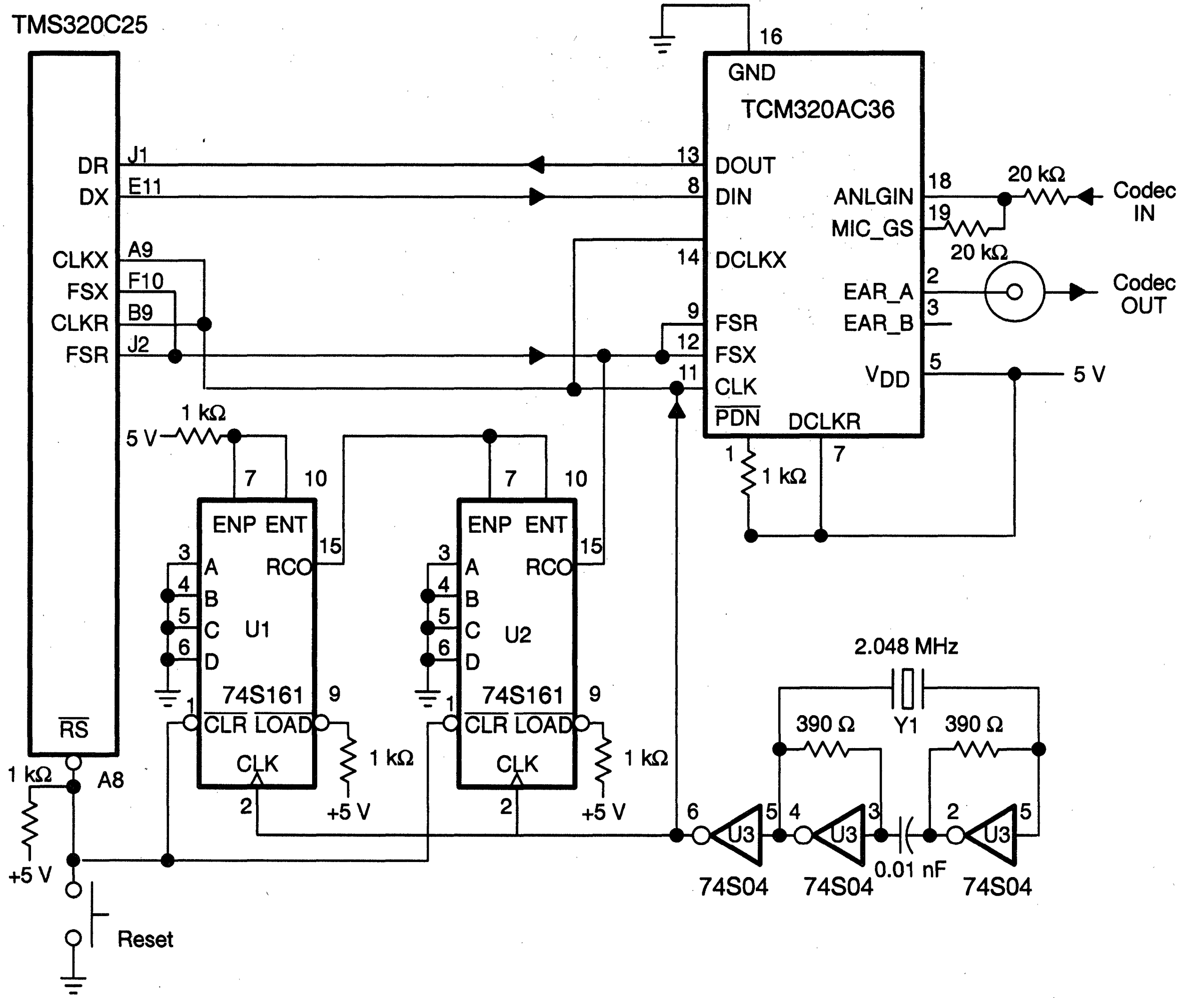
A.2 Telecommunications Applications

The TI linear product line focuses on three primary telecommunications application areas: subscriber instruments (telephones, modems, etc.), central office line card products, and personal communications. Subscriber instruments include the TCM508x DTMF tone encoder family, the TCM150x tone ringer family, the TCM1520 ring detector, and the TCM3105 FSK modem. Central office line card products include the TCM29Cxx combo (combined PCM filter plus codec) family, the TCM420x subscriber line control circuit family, and the TCM1030/60 line card transient protector. Personal communication (PCN) and cellular products include the TCM320AC3x, TCM320AC4x family of 5-volt voice-band audio processors (VBAP).

TI continues to develop new telecom integrated circuits, such as a high-performance 3-volt combo family for personal communications applications, and an RF power amplifier family for hand-held and mobile cellular phones.

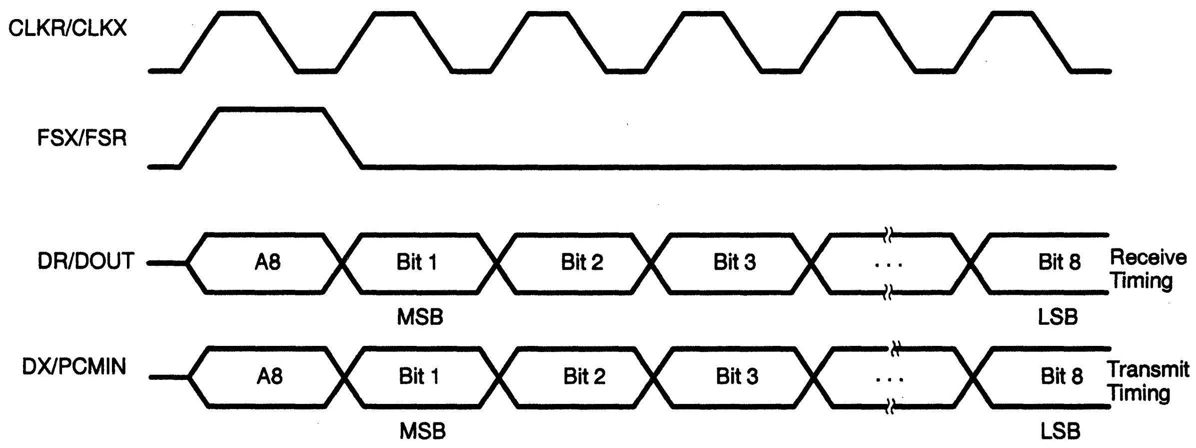
System Design Considerations. The size, network complexity, and compatibility requirements of telecommunications central office systems create demanding performance requirements. Combo voice-band filter performance is typically ± 0.15 dB in the passband. Idle channel noise must be on the order of 15 dBrnc0. Gain tracking (S/Q) and distortion must also meet stringent requirements. The key parameters for a SLIC device are gain, longitudinal balance, and return loss.

Figure A–4. Typical DSP/Combo Interface



The TCM320AC36 combo interfaces directly to the TMS320C25 serial port with a minimum of external components, as shown in Figure A–4. Half of hex inverter U3 and crystal Y1 form an oscillator that provides clock timing to the TCM320AC36. The synchronous 4-bit counters U1 and U2 generate an 8-kHz frame sync signal. DCLKR on the TCM320AC36 is connected to V_{DD}, placing the combo in fixed data-rate mode. Two 20-kΩ resistors connected to ANLGIN and MIC_GS set the gain of the analog input amplifier to 1. The timing is shown in Figure A–5.

Figure A–5. DSP/Combo Interface Timing



Telecommunications-Related Devices. Data sheets for the devices in Table A–3 are contained in the *1993 Telecommunications Circuits Databook*, (literature number SCTD001). To request your copy, contact your nearest Texas Instruments field sales office or call the Customer Response Center at (800) 336–5236.

Table A–3. Telecom Devices

Device Number	Coding Law	Clock Rates MHz†	# of Bits	Comments
Codec/Filter				
TCM29C13	A and μ	1.544, 1.536, 2.048	8	C.O. and PBX line cards
TCM29C14	A and μ	1.544, 1.536, 2.048	8	Includes 8th-bit signal
TCM29C16	μ	2.048	8	16-pin package
TCM29C17	A	2.048	8	16-pin package
TCM29C18	μ	2.048	8	Low-cost DSP interface
TCM29C19	μ	1.536	8	Low-cost DSP interface
TCM29C23	A and μ	Up to 4.096	8	Extended frequency range
TCM29C26	A and μ	Up to 4.096	8	Low-power TCM29C23
TCM320AC36	μ and Linear	Up to 4.096	8 and 13	Single voltage (+5) VBAP
TCM320AC37	A and Linear	Up to 4.096	8 and 13	Single voltage (+5) VBAP
TCM320AC38	μ and Linear	Up to 4.096	8 and 13	Single voltage (+5) GSM
TCM320AC39	A and Linear	Up to 4.096	8 and 13	Single voltage (+5) GSM
TP3054/64	μ	1.544, 1.536, 2.048	8	National Semiconductor second source
TP3054/67	A	1.544, 1.536, 2.048	8	National Semiconductor second source
TLC320AC01/02	Linear	25 kHz	14	5-volt-only analog interface
TLC32040/1	Linear	Up to 19.2-kHz sampling	14	For high-dynamic linearity
TLC32044/5	Linear	Up to 19.2-kHz sampling	14	For high-dynamic linearity
TLC32046	Linear	Up to 25-kHz sampling	14	For high-dynamic linearity
TLC32047	Linear	Up to 25-kHz sampling	14	For high-dynamic linearity
Transient Suppressor				
TCM1030	Transient suppressor for SLIC-based line card			(30 A max)
TCM1060	Transient suppressor for SLIC-based line card			(60 A max)

† Unless otherwise noted

Table A–4. Switched-Capacitor Filter ICs

Device	Function	Order	Roll-Off	Power Out	Power Down
TLC2470	Differential audio filter amplifier	4	5 kHz	500 mW	Yes
TLC2471	Differential audio filter amplifier	4	3.5 kHz	500 mW	Yes
TLC04/14	Low pass, Butterworth filter	4	CLK ÷ 50 CLK ÷ 100	N/A	No

For further information on these telecommunications products, please call (214) 997–3772.

Figure A–6. General Telecom Applications

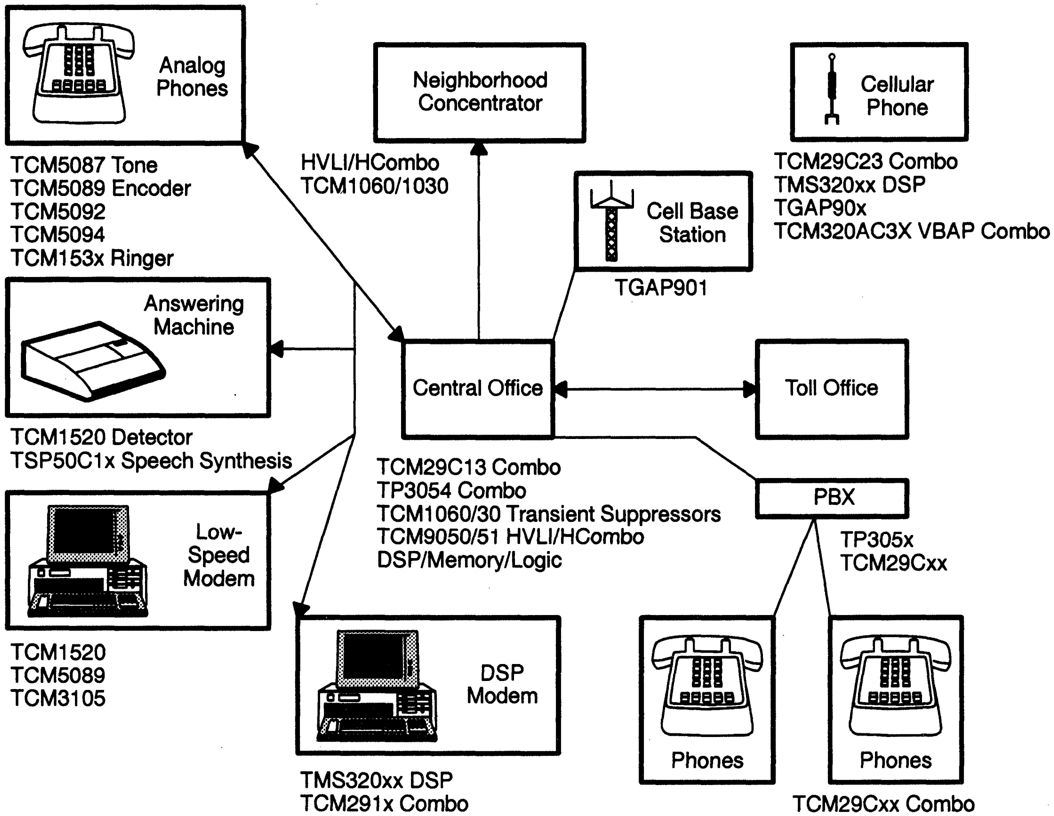
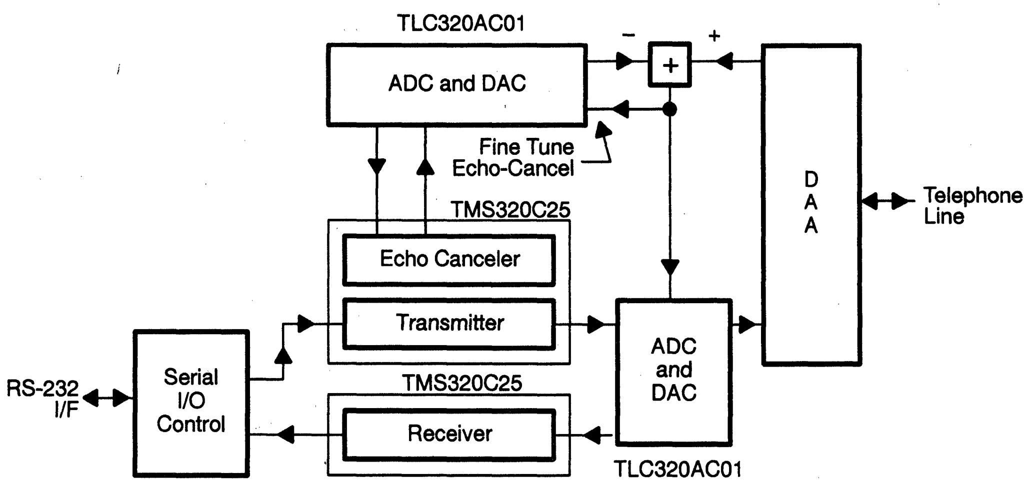


Figure A–7. Generic Telecom Application



A.3 Dedicated Speech Synthesis Applications

For dedicated speech synthesis applications, Texas Instruments offers a family of dedicated speech synthesizer chips. This speech technology has been used in a wide range of products including games, toys, burglar alarms, fire alarms, automobiles, airplanes, answering machines, voice mail, industrial control machines, office machines, advertisements, novelty items, exercise machines, and learning aids.

Dedicated speech synthesis chips are a good alternative for low-cost applications. The speech synthesis technology provided by the dedicated chips is either LPC (linear-predictive coding) or CVSD (continuously variable slope delta modulation). Table A–5 shows the characteristics of the TI voice synthesizers.

Table A–5. Voice Synthesizers

TI Voice Synthesizers:						
Device	**Microprocessor**	**Synthesis Method**	**I/O Pins**	**On-Chip Memory (Bits)**	**External Memory**	**Data Rate (Bits/Sec)**
TSP50C4x	8-bit	LPC–10	20/32	64K/128K	VROM	1200–2400
TSP50C1x	8-bit	LPC–12	10	64K/128K	VROM	1200–2400
TSP53C30	8-bit	LPC–10	20	N/A	From host µP	1200–2400
TSP50C20	8-bit	LPC–10	32	N/A	EPROM	1200–2400
TMS3477	N/A	CVSD	2	None	DRAM	16K–32K

In addition to the speech synthesizers, TI has low-cost memories that are ideal for use with these chips. Texas Instruments can also be of assistance in developing and processing the speech data that is used in these speech synthesis systems. Table A–6 shows speech memory devices of different capabilities. Additionally, audio filters are outlined in Table A–7.

Table A–6. Speech Memories

TSP60Cxx Family of Speech ROMs					
	TSP60C18	TSP60C19	TSP60C20	TSP60C80	TSP60C81
Size	256K	256K	256K	1M	1M
No. of Pins	16	16	28	28	28
Interface	Parallel 4-bit	Serial	Parallel/serial 8-bit	Serial	Parallel 4-bit
For use with:	TSP50C1x	TSP50C4x	TSP50C4x	TSP50C4x	TSP50C1x

Table A–7. Switched-Capacitor Filter ICs

Device	Function	Order	Roll-Off	Power Out	Power Down
TLC2470	Differential audio filter amplifier	4	5 kHz	500 mW	Yes
TLC2471	Differential audio filter amplifier	4	3.5 kHz	500 mW	Yes
TLC04/14	Low pass, Butterworth filter	4	CLK ÷ 50 CLK ÷ 100	N/A	No

Speech Synthesis Development Tools

Software:	
EVM	Code development tool
Speech:	
SAB	Speech audition board
SD85000	PC-based speech analysis system

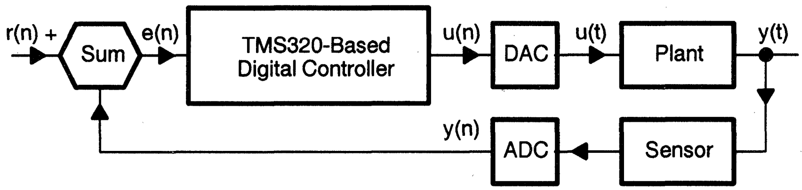
System:	
SEB	System emulator board
SEB60Cxx	System emulator boards for speech memories

For further information on these speech synthesis products, please call TI Linear Applications at (214) 997–3772.

A.4 Servo Control/Disk Drive Applications

Several years ago, most servo control systems used only analog circuitry. However, the growth of digital signal processing has made digital control theory a reality. Figure A–8 shows a block diagram of a generic digital control system using a DSP, along with an ADC and DAC.

Figure A–8. Generic Servo Control Loop



In a DSP-based control system, the control algorithm is implemented via software. No component aging or temperature drift is associated with digital control systems. Additionally, sophisticated algorithms can be implemented and easily modified to upgrade system performance.

System Design Considerations. TMS320 DSPs have facilitated the development of high-speed digital servo control for disk drive and industrial control applications. Disk drives have increased storage capacity from 5 megabytes to over 1 gigabyte in the past decade, which equates to a 23,900 percent growth in capacity. To accommodate these increasingly higher densities, the data on the servo platters, whether servo-positioning or actual storage information, must be converted to digital electronic signals at increasingly closer points in relation to the platter “pick-off” point. The ADC must have increasingly higher conversion rates and greater resolution to accommodate the increasing bandwidth requirements of higher storage densities. In addition, the ADC conversion rates must increase to accommodate the shorter data retrieval access time.

Table A–8. Control Related Devices

Function	Device	Bits	Speed	Channels	Interface
ADC	TLC1550	10	3–5 μs	1	Parallel
	TLC1551	10	3–5 μs	1	Parallel
	TLC0820	8	1.5 μs	1	Parallel
	TLC1225	13	12 μs	1 (Diff.)	Parallel
	TLC1543	10	21 μs	11	Serial
	TLC1549	10	21 μs	1	Serial
	TLV1543	10	21 μs	11	Serial
	TLV1549	10	21 μs	1	Serial
	TLC2543	12	10 μs	11	Serial
DAC	TLC7524	8	9 MHz	1	Parallel
	TLC7628	8	9 MHz	(Dual)	Parallel
	TLC5602	8	30 MHz	1	Parallel

A.5 Modem Applications

High-speed modems (9,600 bps and above) require a great deal of analog signal processing in addition to digital signal processing. Designing both high-speed capabilities and slower fall-back modes poses significant engineering challenges. TI offers a number of analog front-end (AFE) circuits to support various high-speed modem standards.

The TLC32040, TLC32044, TLC32046, TLC32047, and TLC320AC01/02 analog interface circuits (AIC) are especially suited for modem applications by the integration of an input multiplexer, switched capacitor filters, high resolution 14-bit ADC and DAC, a four-mode serial port, and control and timing logic. These converters feature adjustable parameters, such as filtering characteristics, sampling rates, gain selection, (sin x)/x correction (TLC32044, TLC32046, TLC32047 and TLC320AC01/02 only), and phase adjustment. All these parameters are software programmable, making the AIC suitable for a variety of applications. Table A–9 has the description and characteristics of these devices.

Table A–9. Modem AFE Data Converters

Device	Description	I/O	Resolution (Bits)	Conversion Rate
TLC32040	Analog interface chip (AIC)	Serial	14	19.2 kHz
TLC32041	AIC without on-board V_{REF}	Serial	14	19.2 kHz
TLC32044	Telephone speed/modem AIC	Serial	14	19.2 kHz
TLC32045	Low-cost version of the TLC32044	Serial	14	19.2 kHz
TLC32046	Wide-band AIC	Serial	14	25 kHz
TLC32047	AIC with 11.4-kHz BW	Serial	14	25 kHz
TLC320AC01/02	5-volt-only AIC	Serial	14	25 kHz
TCM29C18	Companding codec/filter	PCM	8	8 kHz
TCM29C23	Companding codec/filter	PCM	8	16 kHz
TCM29C26	Low-power codec/filter	PCM	8	16 kHz
TCM320AC36	Single-supply codec/filter	PCM and Linear	8	25 kHz

The AIC interfaces directly with serial-input TMS320 DSPs, which execute the modem's high-speed encoding and decoding algorithms. The TLC3204x family performs level-shifting, filtering, and A/D and D/A data conversion. The DSP's many software-programmable features provide the flexibility required for modem operations and make it possible to modify and upgrade systems easily. Under DSP control, the AIC's sampling rates permit designers to include fall-back modes without additional analog hardware in most cases. Phase adjustments can be made in real time so that the A/D and D/A conversions can be synchronized with the upcoming signal. In addition, the chip has a built-in loopback feature to support modem self-test requirements.

For further information or application assistance, please call TI Linear Applications at (214) 997–3772.

Figure A–9. High-Speed V.32 Bis and Multistandard Modem With the TLC320AC01 AIC

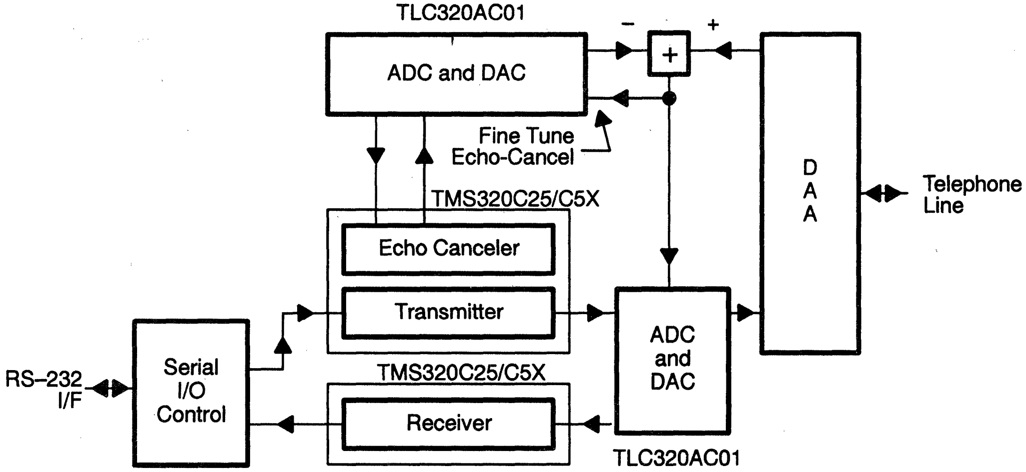


Figure A–9 shows a V.32 bis modem implementation using the TMS320C25 and a TLC320AC01. The upper TMS320C25 performs echo cancellation and transmit data functions, while the lower TMS320C25 performs receive data and timing recovery functions. The echo canceler simulates the telephone channel and generates an estimated echo of the transmit data signal. The TLC320AC01 performs the following functions:

Upper TLC320AC01 D/A Path: Converts the estimated echo, as computed by the upper TMS320C25, into an analog signal, which is subtracted from the receive signal.

Upper TLC320AC01 A/D Path: Converts the residual echo to a digital signal for purposes of monitoring the residual echo and continuously training the echo canceler for optimum performance. The converted signal is sent to the upper TMS320C25.

Lower TLC320AC01 D/A Path: Converts the upper TMS320C25 transmit output to an analog signal, performs a smoothing filter function, and drives the DAC.

Lower TLC320AC01 D/A Path: Converts the echo-free receive signal to a digital signal, which is sent to the lower TMS320C25 to be decoded.

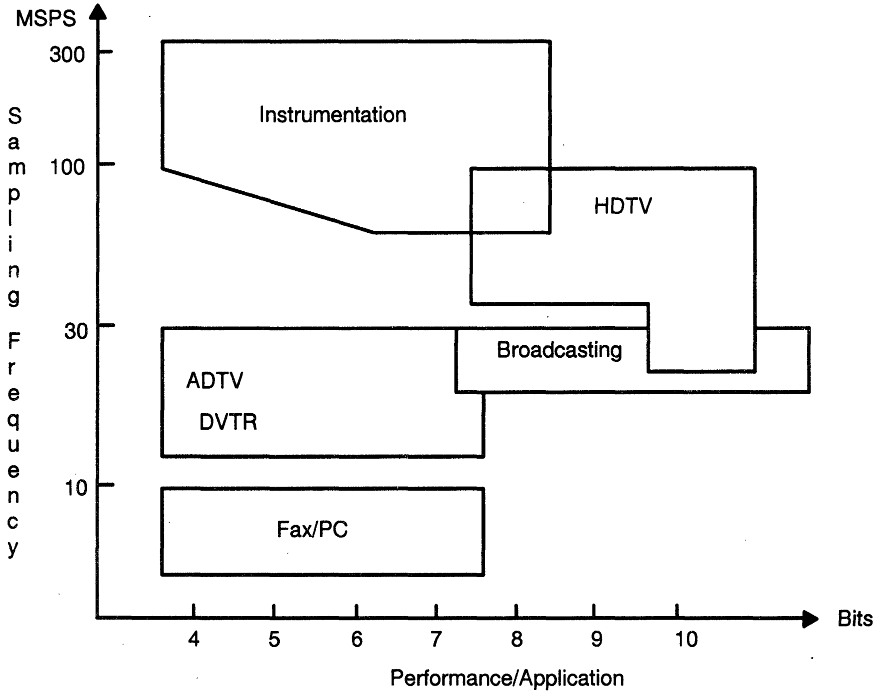
Note: About the Above Example

The example above is for illustration only. In reality, one single TMS320C5x DSP can implement high-speed modem functions.

A.6 Advanced Digital Electronics Applications for Consumers

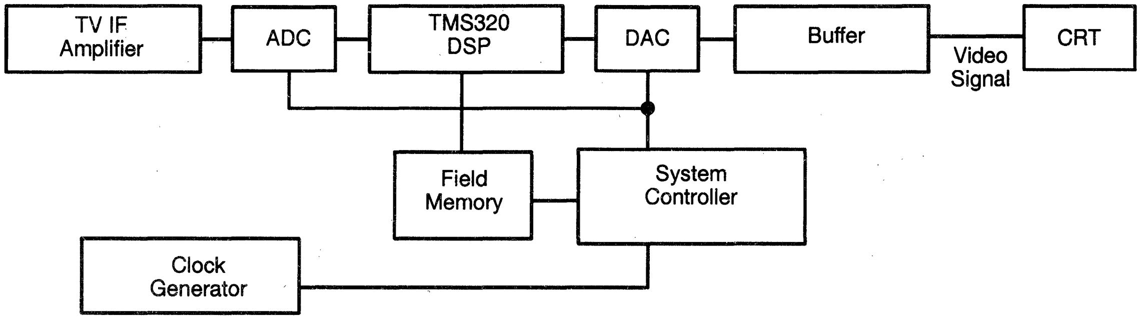
With the extensive use of the TMS320 DSPs in consumer electronics, much electromechanical control and signal processing can be done in the digital domain. Digital systems generally require some form of analog interface, usually in the form of high-performance ADCs and DACs. Figure A–10 shows the general performance requirements for a variety of applications.

Figure A–10. Applications Performance Requirements



Advanced Television System Design Considerations. Advanced Digital Television (ADTV) is a technology that uses digital signal processing to enhance video and audio presentations and to reduce noise and ghosting. Because of these DSP techniques, a variety of features can be implemented, including frame store, picture-in-picture, improved sound quality, and zoom. The bandwidth requirements remain at the existing 6-MHz television allocation. From the IF(intermediate frequency) output, the video signal is converted by an 8-bit video ADC. The digital output can be processed in the digital domain to provide noise reduction, interpolation or averaging for digitally increased sharpness, and higher quality audio. The DSP digital output is converted back to analog by a video DAC, as shown in Figure A–11.

Figure A–11. Video Signal Processing Basic System



VCRs, compact disc and DAT players, and PCs are a few of the products that have taken a major position in the marketplace in the last ten years. The audio channels for compact disc and DAT require 16-bit A/D resolution to meet the distortion and noise standards. See NO TAG for a block diagram of a typical digital audio system.

The audio processing becomes more demanding as higher fidelity is required. Better fidelity translates into lower noise and distortion in the output signal.

The TMS57014DW 1-bit digital-to-analog converters (DAC) include an 8 times over sampling digital filter designed for digital audio systems, such as CDPs, DATs, CDIs, LDPs, digital amplifiers, car stereos, and BS tuners. They are also suitable for all systems that include digital sound processing like TVs, VCRs, musical instruments, NICAM systems, multimedia, etc.

The converters have dual channels so that the right and left stereo signals can be transformed into analog signals with only one chip. There are some functions that allow the customers to select the conditions according to their applications, such as muting, attenuation, de-emphasis, and zero data detection. These functions are controlled by external 16-bit serial data from a controller like a microcomputer.

The TMS57014DW has a 129-tap FIR filter and third-order $\Delta\ \Sigma$ modulation to get –75-dB stop band attenuation and 96-dB SNR. The output is PWM wave, which facilitates analog signal through a low-pass filter.

Table A–10 lists TI products for analog interfacing to digital systems.

Table A–10. Audio/Video Analog/Digital Interface Devices

Function	Device	Bits	Speed	Channels	Interface
Dual audio DAC+ digital filter	TMS57013	16/18	32, 37.8, 44.1, 48 kHz	2	Serial
A/D	TLC1225	12	12 μs	1	Parallel
A/D	TLC1550	10	6 μs	1	Parallel
Video D/A	TLC5602	8	50 ns	1	Parallel
Triple video D/A	TL5632	8	16 ns	3	Parallel
Triple flash A/D	TLC5733	8	70 ns	3	Parallel
Pipelined A/D	TLC5510	8	50 ns	1	Parallel
Semiflash A/D	TLC5540	8	25 ns	1	Parallel

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