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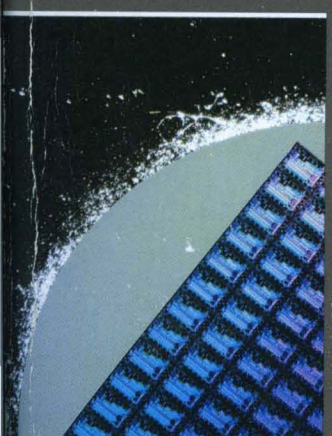

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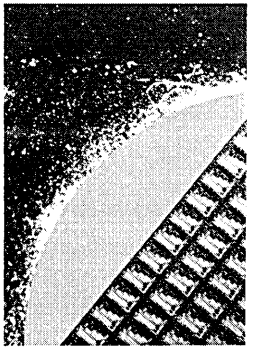
VLSI DATA BOOK



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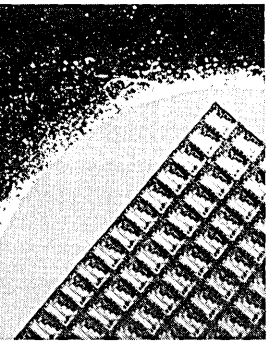

Introduction

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Challenging the Future

As the world leader of high-speed data acquisition and digital signal processing components, TRW LSI Products has made a commitment to the future. In the early 1960s, TRW developed TTL and pioneered the evolution of Integrated Circuit and VLSI technologies. Today TRW LSI is conducting research to create new products and set high-performance standards in the design, development and manufacture of components. 1-micron technology is now the standard used at TRW in both bipolar and CMOS processes. This represents a major breakthrough in IC manufacturing, producing faster and more cost-effective products.

As system technologies change and grow, the group of dedicated employees at TRW LSI Products has committed the future to setting even higher standards in order to provide the customer with better, more reliable, and more useful products. TRW LSI Products currently offers a diverse line of DSP components, including: multipliers, multiplier-accumulators, A/D and D/A converters, shift registers, floating point processors, and others.

The use of innovative designs and state-of-the-art manufacturing processes has resulted in product quality that is unsurpassed in the industry. Each device receives thorough testing, and passes stringent quality control requirements. TRW LSI's components have been proven in many applications, ranging from telecommunications and broadcasting to oil and space exploration, medical electronics and underwater surveillance.

TRW LSI Products prides itself in its responsiveness to customers' requirements and needs. As world technological advances intensify, the most modern research techniques are applied to real-life situations in order to produce devices designed to improve system reliability while reducing circuit cost, size and power requirements.

Our superior products meet all of your specific needs. Follow us as we develop components that will require less space, less energy consumption and less design effort for your system. Follow us as we challenge the future.

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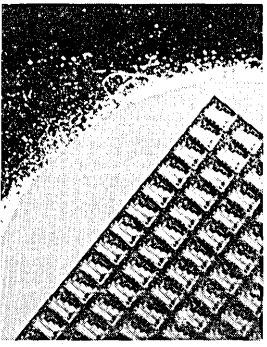

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A/D Converters		Catalog Page Number
TDC1001	8-Bit, 2.5MSPS	D 5
TDC1002	8-Bit, 1.0MSPS	D 5
TDC1007	8-Bit, 20MSPS	D 15
TDC1014	6-Bit, 25MSPS	D 27
TDC1019	9-Bit, 15MSPS	D 37
TDC1019-1	9-Bit, 18MSPS	D 37
TDC1021	4-Bit, 25MSPS	D 49
TDC1025	8-Bit, 50MSPS	D 59
TDC1027	7-Bit, 18MSPS	D 75
TDC1029	6-Bit, 100MSPS	D 85
TDC1044	4-Bit, 25MSPS	D 97
TDC1046	6-Bit, 25MSPS	D 107
TDC1047	7-Bit, 20MSPS	D 117
TDC1048	8-Bit, 20MSPS	D 127
TDC1147	7-Bit, 15MSPS	D 139

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TDC1014E1C/P1C	6-Bit, 25MSPS	E 21
TDC1019E1C	9-Bit, 15MSPS	E 35
TDC1025E1C	8-Bit, 50MSPS	E 49
TDC1029E1C	6-Bit, 100MSPS	E 61
TDC1047E1C	7-Bit, 20MSPS	E 73
TDC1048E1C	8-Bit, 20MSPS	E 83

D/A Converters		
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TDC1016-9	9-Bit, 20MSPS	F 5
TDC1016-10	10-Bit, 20MSPS	F 5
TDC1018	8-Bit, 125MSPS	F 17
TDC1034	4-Bit, 125MSPS	F 31

Multipliers		
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MPY112K	12 x 12 Bit, 50ns Cycle Time	G 39
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TDC1022	22–Bit, 10MHz, Floating Point Arithmetic Unit	I 13
TDC1023	64 x 1 Bit, 15MHz, Digital Correlator, Digital Output	I 29
TDC1028	4 x 4 x 8 Bit, 10MHz, Digital Filter (FIR)	I 43

Memory/Storage Products

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TDC1006	256 x 1 Bit, 25MHz, Shift Register	J 11
TDC1011	8–Bit, 18MHz, Variable Length Shift Register	J 17
TDC1030	64 x 9, 15MHz, First–In First–Out Memory	J 25

See pages C 3–C 25 for information on our future products.

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MPY008H	8 x 8 Bit Multiplier, 90ns Cycle Time	G 5
MPY008H-1	8 x 8 Bit Multiplier, 65ns Cycle Time	G 5
MPY08HU	8 x 8 Bit Multiplier, 90ns Cycle Time	G 15
MPY08HU-1	8 x 8 Bit Multiplier, 65ns Cycle Time	G 15
MPY012H	12 x 12 Bit Multiplier, 115ns Cycle Time	G 25
MPY016H	16 x 16 Bit Multiplier, 145ns Cycle Time	G 49
MPY016K	16 x 16 Bit Multiplier, 45ns Cycle Time	G 63
MPY016K-1	16 x 16 Bit Multiplier, 40ns Cycle Time	G 63
MPY112K	12 x 12 Bit Multiplier, 50ns Cycle Time	G 39
TDC1001	8-Bit A/D Converter, 2.5MSPS, Successive Approximation	D 5
TDC1002	8-Bit A/D Converter, 1.0MSPS, Successive Approximation	D 5
TDC1004	64 x 1 Bit Digital Correlator, 10MHz, Analog Output	I 5
TDC1005	64 x 2 Bit Shift Register, 25MHz	J 5
TDC1006	256 x 1 Bit Shift Register, 25MHz	J 11
TDC1007	8-Bit A/D Converter, 20MSPS	D 15
TDC1007E1C	8-Bit Evaluation Board, 20MSPS	E 5
TDC1008	8 x 8 Bit Multiplier-Accumulator, 100ns Cycle Time	H 5
TDC1009	12 x 12 Bit Multiplier-Accumulator, 135ns Cycle Time	H 17
TDC1010	16 x 16 Bit Multiplier-Accumulator, 165ns Cycle Time	H 29
TDC1011	8-Bit Variable Length Shift Register, 18MHz	J 17
TDC1014	6-Bit A/D Converter, 25MSPS	D 27
TDC1014E1C	6-Bit Evaluation Board, 25MSPS	E 21
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TDC1016-10	10-Bit D/A Converter, 20MSPS	F 5
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TDC1019E1C	9-Bit Evaluation Board, 15MSPS	E 35
TDC1021	4-Bit, A/D Converter, 25MSPS	D 49
TDC1022	22-Bit Floating Point Arithmetic Unit, 10MHz	I 13
TDC1023	64 x 1 Bit Digital Correlator, 15MHz, Digital Output	I 29
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TDC1028	4 x 4 x 8 Bit Digital Filter (FIR), 10MHz	I 43
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TDC1029E1C	6-Bit Evaluation Board, 100MSPS	E 61
TDC1030	64 x 9 Bit First-In First-Out Memory, 15MHz	J 25
TDC1034	4-Bit D/A Converter, 125MSPS	F 31
TDC1043	16 x 16 Bit Multiplier-Accumulator, 100ns Cycle Time	H 41
TDC1044	4-Bit A/D Converter, 25MSPS	D 97
TDC1046	6-Bit A/D Converter, 25MSPS	D 107
TDC1047	7-Bit A/D Converter, 20MSPS	D 117
TDC1047E1C	7-Bit Evaluation Board, 20MSPS	E 73
TDC1048	8-Bit A/D Converter, 20MSPS, Low Power	D 127
TDC1048E1C	8-Bit Evaluation Board, 20MSPS	E 83
TDC1147	7-Bit A/D Converter, 15MSPS	D 139

TMC2009	12 x 12 Bit CMOS Multiplier-Accumulator, 135ns Cycle Time	H 53
TMC2010	16 x 16 Bit CMOS Multiplier-Accumulator, 160ns Cycle Time	H 65
TMC2110	16 x 16 Bit CMOS Multiplier-Accumulator, 100ns Cycle Time	H 77
TMC216H	16 x 16 Bit CMOS Multiplier, 145ns Cycle Time	G 77

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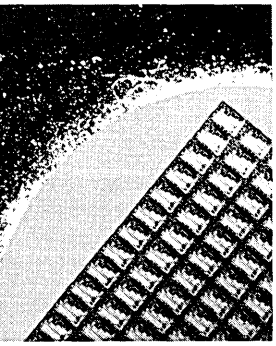

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TDC1033
Advance Information

TRW

Floating Point Registered Arithmetic/Logic Unit
22-bit (with 16-bit compatibility mode)

The TRW TDC1033 is a monolithic integrated circuit arithmetic/logic unit with an on-chip register file. It operates on numbers represented in two formats: 16-bit fixed point two's complement and 22-bit floating point. The 22-bit floating point format has a 16-bit two's complement significand and a 6-bit two's complement exponent giving full 16-bit precision over a 384dB dynamic range.

In the 16-bit fixed point mode, the TDC1033 is function and microcode compatible with an array of four industry standard 2901-bit slice processors including the 2902 carry-look-ahead chip. The 22-bit floating point arithmetic functions are parallel to the fixed-point arithmetic functions providing an easy way for the designer to upgrade system performance without reprogramming microcode.

Either saturation or wrap-around treatment of overflow and underflow conditions may be selected for floating point operation.

To retain compatibility with the 2901-bit slice processors, there is a single data input port and a single data output port; these ports are fully TTL compatible. All data inputs and outputs are registered. The data outputs are three-state to allow use on a bus.The 2901's internal dual-port RAM has been retained and widened to 22 bits. Likewise, the internal bus paths are 22 bits wide. Twenty-seven pins are used to supply instructions, controls and addresses to the TDC1033. It operates at up to 6 million operations/second (6MHz clock).

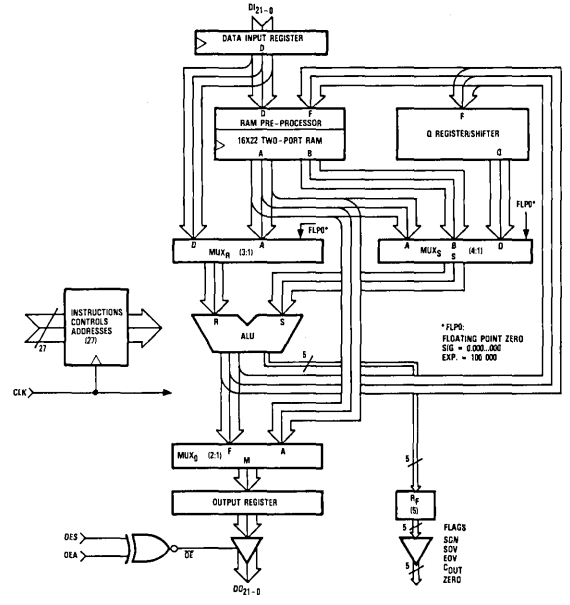
Features

- Microprogrammable (Replaces Four 2901-Bit Slice Units) In Fixed Point Mode
- Eases Upgrade Of Systems To Floating Point
- Full 16-Bit Precision Over Wide Dynamic Range
- Two's Complement Fixed And Floating Point Operation
- User-Selectable Saturation Limiting Or Wrap-Around Overflow Handling
- Three-State TTL Outputs
- Available In 84 Lead Pin Grid Array Or Leadless Chip Carrier

Applications

- Fast Fourier Transformers
- Digital Filters
- Geometric Transformations For Image Processing And Computer Graphics
- Array Processors
- High-Speed Controllers
- Arithmetic Element Module (With TDC1042 Multiplier)

Simplified Block Diagram



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Instructions

Floating Point	Fixed Point	Flags
R + S	R + S	SIGN
S - R	S - R	Significand Overflow
R - S	R - S	ZERO
Normalize R + S	R OR A	Exponent Overflow
Denormalize R	R AND S	Significand Carry Out
	$\overline{R}$ AND S	
	R XOR S	
	R XNOR S	

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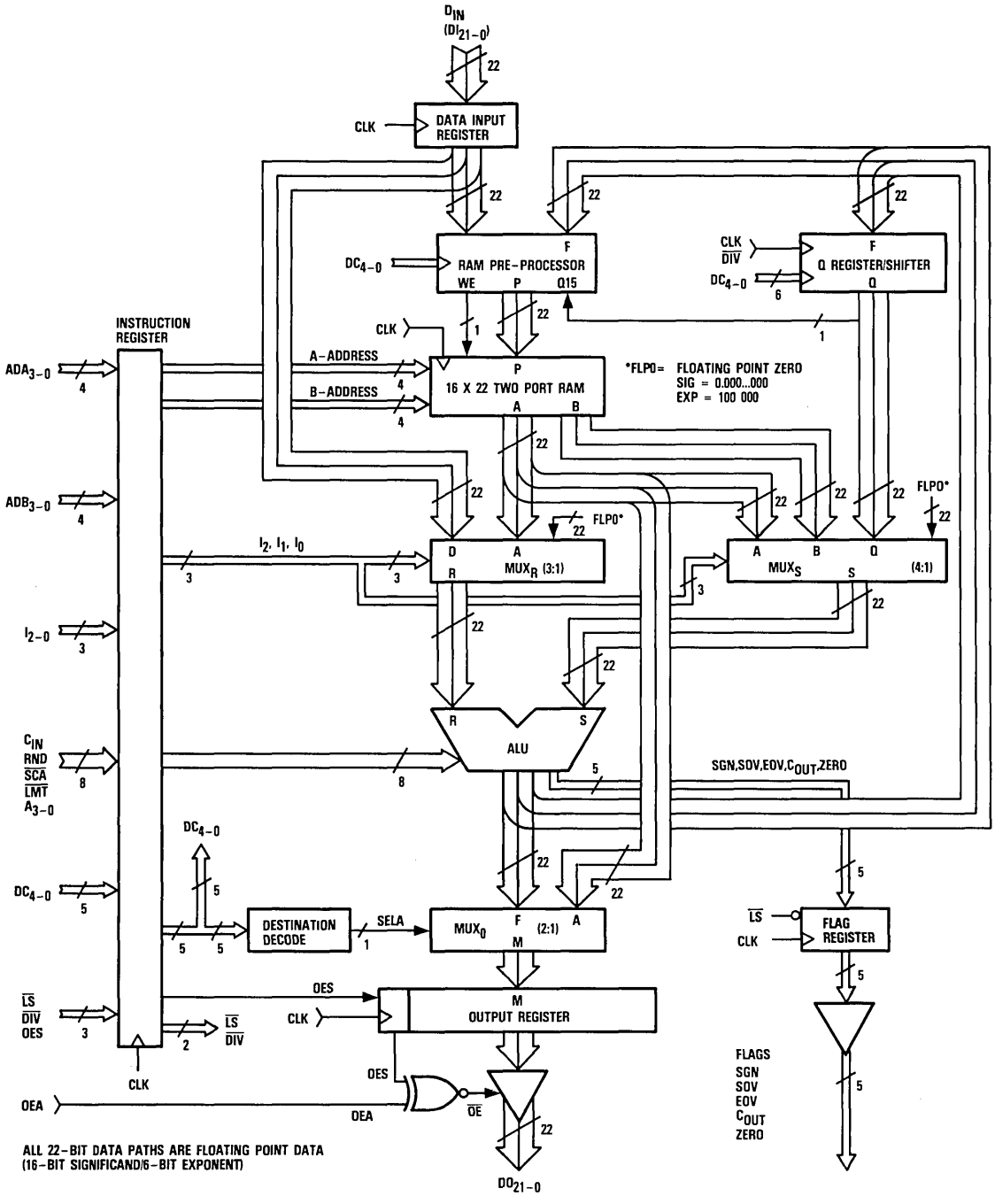
Functional Block Diagram



Functional Description

The TDC1033 consists of five functional sections:

1. The Source Multiplexers For The ALU
2. The Arithmetic/Logic Unit (ALU) Itself
3. The Two-Port RAM (Register File) And RAM Shifter
4. The Q Register And Shifter
5. The Output Multiplexer

Source Multiplexers

The source multiplexers select which inputs will be applied to the ALU Section. The operation of these multiplexers is controlled by three microcode instruction bits, I_2-I_0.

The R multiplexer is a one-of-three data selector which applies to either:

1. The present data input to the chip
2. The RAM "A" output (i.e., the word in register file "A" selected by the A Address, ADA_3-ADA_0) or
3. A floating point zero

to the "A" input port of the ALU Section.

The S multiplexer is a one-of-four data selector which applies either:

1. The RAM "A" output (as defined above)
2. The RAM "B" output (i.e., the word in register file "B" selected by the B Address, ADB_3-ADB_0)
3. The Q register output or
4. A floating point zero

to the "B" input port of the ALU Section.

Arithmetic/Logic Unit

The ALU receives two numbers, denoted R and S, from the source multiplexers. It then performs one of eight fixed point operations, or one of five floating point operations on those quantities. The output of the ALU is bused to the RAM shifter, the Q register shifter and the output multiplexer. The ALU is controlled by eight registered inputs (A_3-A_0), Carry In (CIN), Round (RND), Scale (SCA) and Limit (LMT).

The ALU consists of four blocks:

1. The Denormalize Section
2. The Adder/Logic Section
3. The Renormalize Section
4. The Round/Scale/Limit Section

The Denormalize and Renormalize sections are enabled in the floating point mode and disabled in the fixed point mode. The Denormalize Section compares the two operands' exponents and shifts the significand of the smaller by the difference between the exponents. In floating point mode, the Adder/Logic Section operates on the significand of the result. In fixed-point mode, the Adder/Logic Section operates on the selected 16-bit operands as directed by the control inputs to the device with no denormalization. The Renormalize Section performs the necessary shifts to remove redundant sign bits adjusting the exponent as required. The flags SGN (Significand SiGN), SOV (Significand OVerflow), EOV (Exponent OVerflow), ZERO (zero significand) and COUT (significand Carry OUT) are generated in the Renormalize Section. Note that while the significand flags are active in the fixed point mode, the EOV flag will not be active in the fixed point mode. In floating point mode only, the Round/Scale/Limit Section adjusts the result according to its controls. These controls and their effects are: RND (add a ONE to the bit position just below the LSB), SCA (subtract one from the exponent effectively, divide the result by two) and LMT (force the output to the maximum representable magnitude on overflow and force the output to floating point zero on underflow).

RAM

The RAM is a two-port 16-deep by 22-bit wide register file. The RAM preprocessor allows one of the following to be loaded into RAM:

1. The input data register contents
2. The full 22 bits of the current ALU output
3. Half the value of the significand of the current ALU output (sign-extended, but retaining the same exponent)
4. Twice the value of the significand of the current ALU output (with the same exponent)

Controls DC_4-DC_0 select which preprocessor function is to be performed. Two data words ("A" and "B", selected by the appropriate address bits) can be accessed from the RAM during one machine cycle. The RAM Write Enable (WE) is

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strobed by the rising edge of the chip master clock except in the NOP and Q register write cases.

There are four instructions which control the loading of the RAM:

1. NOP (No OPeration)
2. Load F
3. Load F/2
4. Load 2F

(What is loaded into the RAM is the value selected by the RAM preprocessor.)

In the Load F/2 case, a one-bit right shift of the significand is performed and the Most Significant Bit (MSB) is loaded from one of four sources:

1. One
2. Zero
3. MSB of F (two's complement sign extension)
4. LSB of F (for rotation)

In the Load 2F case, a one-bit left shift of the significand is performed and the Least Significant Bit (LSB) is loaded from one of four sources:

1. One
2. Zero
3. MSB of F for 16-bit word rotation
4. Q shifter significand MSB (used for 32-bit word shift or rotation)

Q Register/Shifter

The Q register/shifter is a 22-bit register which is reloaded each clock cycle with either the previous ALU output value (this is used for performing accumulation, division, etc.) or variously shifted versions of its own present contents. The control signals to this section are DC_4-DC_0 and the DIVide control (DIV). There are nine Q register functions:

1. Load current ALU output. Load significand and hold exponent if DIV = 0
2. Shift significand right one place and shift a zero into the MSB
3. Shift significand right one place and shift the significand LSB of the ALU output into the MSB
4. Shift significand right one place and sign extend
5. Shift significand left one place and shift a zero into the LSB of the significand
6. Shift significand left one place and force ALU significand MSB into the LSB of the significand
7. Rotate Q register contents left (MSB into LSB)
8. Rotate Q register contents right (LSB into MSB)
9. NOP (no operation-i.e., hold current Q register contents)

Use of the Q register is especially advantageous in double-precision fixed point calculations. Note that the exponent field is UNAFFECTED by any Q register shift.

Output Multiplexer

The output multiplexer is a one-of-two data selector which applies either the ALU output or the RAM "A" output to the output register. The selection is internally decoded from control signals DC_4-DC_0.

TDC1042
Advance Information

Floating Point Multiplier
22-bit (with 16-bit fixed point compatibility mode)

The TRW TDC1042 is a monolithic integrated circuit multiplier which operates on numbers represented in a 22-bit floating point format or in a 16-bit fixed point format. The floating point format has a 16-bit two's complement significand and a 6-bit two's complement exponent giving full 16-bit precision over a 384dB dynamic range. Either saturation or wrap-around treatment of overflow conditions may be selected.

Each of the two inputs and the output has its own fully TTL compatible port providing high-speed (non-multiplexed) I/O. All data inputs and outputs are registered as well as the three instruction inputs and one of the control inputs. The data outputs are three-state to allow use on a bus.

Two internal registers and a source-selection multiplexer on the multiplicand ("B") input allow efficient implementation of complex multiplication. An internal pipeline register can be enabled to reach a data throughput rate of 10MHz (guaranteed over temperature and supply voltage variations). The device can provide a new product every 100 nanoseconds. The non-pipelined "feedthrough" mode permits 6MHz operation without the extra stage of pipeline latency.

Features

- Microprogrammable
- Full 16-Bit Precision Over Wide Dynamic Range
- Two's Complement Fixed Or Floating Point Multiplication
- Selectable Pipelining
- User-Selectable Saturation Limiting Or Wrap-Around Overflow Handling
- Fully Parallel I/O Structure
- Fixed Point Operation Available
- Three-State TTL Outputs
- Available In 84 Lead Pin Grid Array Or Leadless Chip Carrier

Applications

- Fast Fourier Transformers
- Digital Filters
- Companion Multiplier For ALU In Microprogrammed Signal Processors
- Coprocessor To TDC1033 Registered Arithmetic Logic Unit
- Geometric Transformations For Image Processing And Computer Graphics

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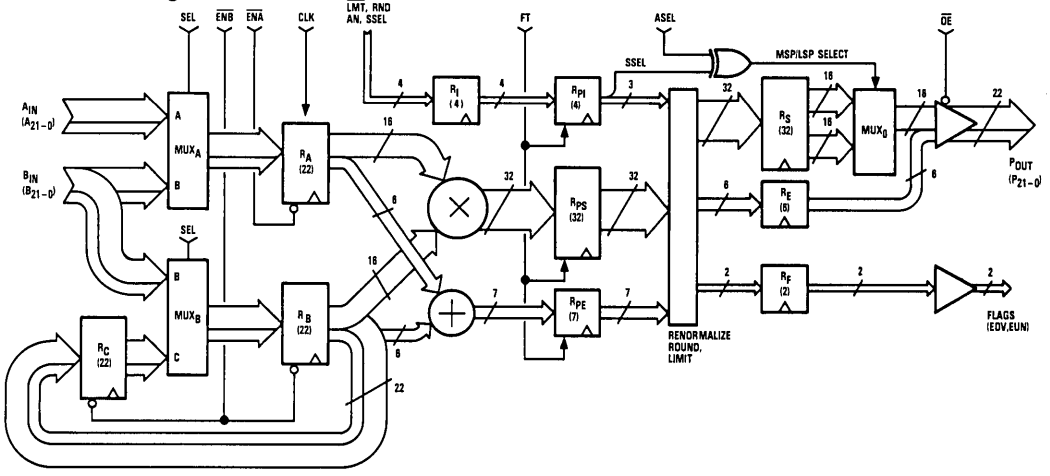
Functional Block Diagram



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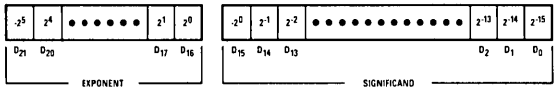
Floating Point Data Format

Input, Output with MSP Selected



Exponent

The exponent is represented by bits D_{16} through D_{21}. It is a two's complement integer with D_{21} the two's complement sign bit. The exponent ranges from −32 to 31.

$$\text{Exponent} = D_{21} \times (-2^5) + \sum_{n=16}^{20} D_n \times 2^{(n-16)}$$

Zero

Zero is represented as follows:

Significand = 0.000 0000 0000 0000
Exponent = 100 000

Significand

The significand (sometimes referred to as the MANTISSA) is represented by bits D_{15} through D_0. It is a fractional two's complement number with 16-bit precision: D_{15} is the two's complement sign bit. The significand ranges from $(1-2^{-15})$ to −1.

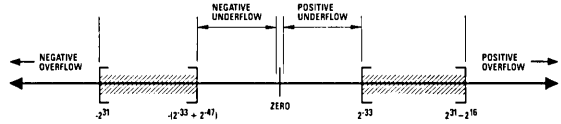
$$\text{Significand} = D_{15} \times (-1) + \sum_{n=0}^{14} D_n \times 2^{(n-15)}$$

Output with LSP Selected

The exponent field is duplicated. The significand field (D_{15} - D_0) carries binary weighting from 2^{-16} through 2^{-31}, respectively. Thus, the significand is $\sum_{n=0}^{15} D_n \times 2^{(n-31)}$ when the LSP is output. The two LSBs (2^{-30} and 2^{-31}) are zero-filled as required by internal significand shifting.

Representable Floating Point (FLP) Number Range

Normalized Floating Point Range: A normalized floating point number is one for which the first two bits of the significand (D_{15} and D_{14}) are different, that is $D_{15} \oplus D_{14} = 1$.



TDC1334
Advance Information

Digital–To–Analog Converter
Triple 4–bit, 100MSPS

The TRW TDC1334 consists of three separate 4–bit D/A converters on a single monolithic integrated circuit. The TDC1334 has been designed for high–speed operation and is compatible with ECL logic families. All data and control inputs to the device are registered on the rising edge of the clock (CONV) input.

A single on–chip band–gap voltage source is used as the reference for all three D/A converters and a single external resistor determines gain of the TDC1334. Video controls, Sync and Blank, are included on the TDC1334 for accurately setting D/A output levels during synchronization and CRT blanking intervals. A brightness enhancement control, Bright, is used for emphasizing portions of a CRT display and cursor identification.

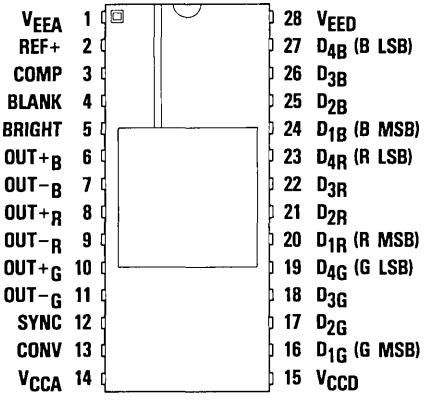
Each of the three D/A converters has two complementary current output terminals that can drive 75 Ohm lines. The device has been designed to minimize digital feedthrough and for optimum printed circuit board layout. Analog and digital grounds have been kept separate for maximum flexibility in system grounding.

Features

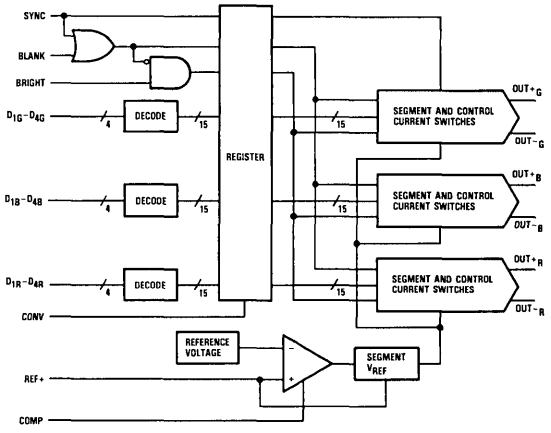
- Complete, Monolithic, "Graphics Ready"
- Three Identical 4–Bit D/A Converters
- Registered Data Inputs
- Registered Sync, Blank, And Bright Controls
- On–Board Reference
- Linearity Error Less Than 1/8 LSB
- 100MSPS Operation
- ECL Compatible Inputs
- Complementary Current Outputs
- Single –5.2 Volt Power Supply Required
- Can Be Operated In TTL Systems
- Available In A 28 Lead Ceramic DIP

C

Pin Assignments



Functional Block Diagram



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TMC2220/TMC2221
Advance Information

CMOS Programmable Digital Output Correlators
4 x 32 Bit, 20MHz
1 x 128 Bit, 20MHz

The TMC2220 is a high-speed digital CMOS correlator divided into four separate 1 x 32 bit correlator modules. The four module correlation scores are weighted and combined according to user programming. Possible configurations include a single 4 x 32 bit, 2 x 64 bit, or 1 x 128 and a pair of separate 1 x 64, or 2 x 32 correlators. In addition, a bit-by-bit masking capability within each module provides total word length flexibility. Each 32-bit module consists of a serial reference shift register, a parallel reference holding latch, a serial data shift register, a masking latch and a parallel counter.

A decoder controls the four two-input reference multiplexers and reference register enables to choose one of eight reference loading schemes. For each of the correlator modules, the reference word is serially shifted into the B register through one of the two multiplexed ports. By clocking the R latch, the reference residing in B is parallel-loaded into R. This allows the user to preload a new reference word into the B register while correlation is being performed between the data and present reference. The four A data registers can be loaded individually or simultaneously with the use of the independent data clock enables. The masking function is defined with the LM control; loading a zero into a cell of the latch will mask the corresponding correlation bit. When the mask latch is in the transparent mode (LM held HIGH), all 32 correlation bits are active.

During the correlation process, the latched reference and data words are continually compared bit-for-bit by exclusive-NOR circuits and ANDed with the latched mask function. Each exclusive-NOR bit contributes one bit to the parallel counter - all bits with a zero in the mask latch have no effect. The output represents the number of positions which match at any one time between the A data register and R reference latch. The module correlation score can be selected by the user as unipolar (0 to 32) or bipolar (-16 to +16) with the TC control.

A 3-bit instruction determines the weighting factor for each of the correlator modules. The weighted outputs are combined into pairs and are available as two independent correlations, Q and I, through the 10-bit main output port and the 8-bit auxiliary port. A programmable matrix combines the Q and I outputs to obtain three additional functions through the main port: Q+I, Q+I/2, and a Max (|Q|, |I|) + 1/2 MIN (|Q|, |I|) approximation for the magnitude quantity SQRT ($I^2 + Q^2$). To simplify interface timing, the programming controls are synchronous, and are appropriately delayed to accommodate the pipelining through the weighting and recombining circuitry.

The TMC2221 combines four 1 x 32 correlator modules in series for a fixed single channel configuration. The reduced complexity and package size of the TMC2221 are ideal for those applications requiring less versatility than the TMC2220. By making use of the masking function, any size single channel length of up to 128 is possible.

With the TMC2221, the reference word is serially loaded through the single two-input multiplexed reference port of the first correlator module. Although the configuration is fixed, the reference loading process and basic operation for each module are similar to those of the TMC2220. The outputs are summed with equal weighting, and the result is output through the single 8-bit port.

C

Features

- 20MHz Correlation Rate
- Single +5V Power Supply
- Low Power CMOS Process Technology
- Three-State TTL Compatible Outputs
- Data Bit Masking Capability
- Two's Complement Or Unsigned Magnitude Correlation Score
- TMC2220 Provides User Programmable Reference Multiplexing, Module Weighting Factors And Recombining Circuitry for 256 Different Correlation Modes.
- Multibit Correlation With TMC2220 Allows for Improved Detection Accuracy In Noisy Environments
- TMC2220 Available In A 64 Lead Ceramic DIP, 68 Contact Chip Carrier, Or 68 Leaded Chip Carrier
- TMC2221 Package Size Reduced With Fixed Single Channel Configuration (1 x 1 Through 1 x 128)
- TMC2221 Available In A 28 Lead Ceramic DIP, 28 Lead CERDIP, Or 28 Contact Chip Carrier

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Applications

- Signal Detection
- Radar Signature Recognition
- Secure Communications
- Robotics
- Automatic Testing Equipment
- Electro-Optical Navigation
- Pattern And Character Recognition

Module Weighting Factor Programming

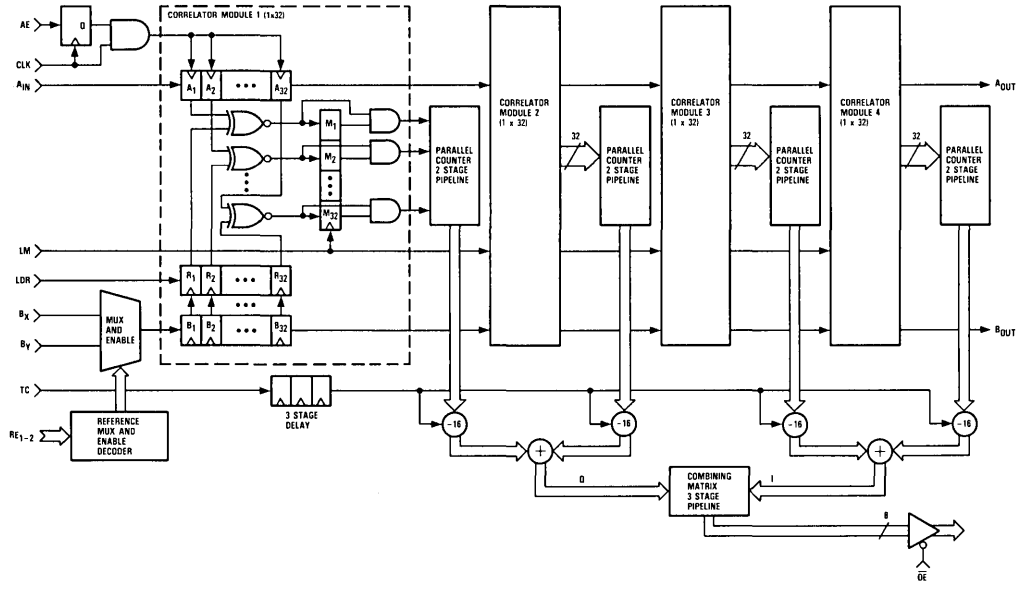
Decoder Inputs			Internal Channel Configuration TMC2220	
W_2	W_1	W_0	Q	I
0	0	0	$Q_a + Q_b$	$I_c + I_d$
0	0	1	$3Q_a + Q_b$	$3I_c + I_d$
0	1	0	$4Q_a + Q_b$	$4I_c + I_d$
0	1	1	Q_b	I_d
1	0	0	Q_a	I_c
1	0	1	$3Q_a + 2Q_b$	$3I_c + 2I_d$
1	1	0	$4Q_a + 2Q_b$	$4I_c + 2I_d$
1	1	1	$5Q_a + 2Q_b$	$5I_c + 2I_d$

Reference Multiplex and Enable Programming

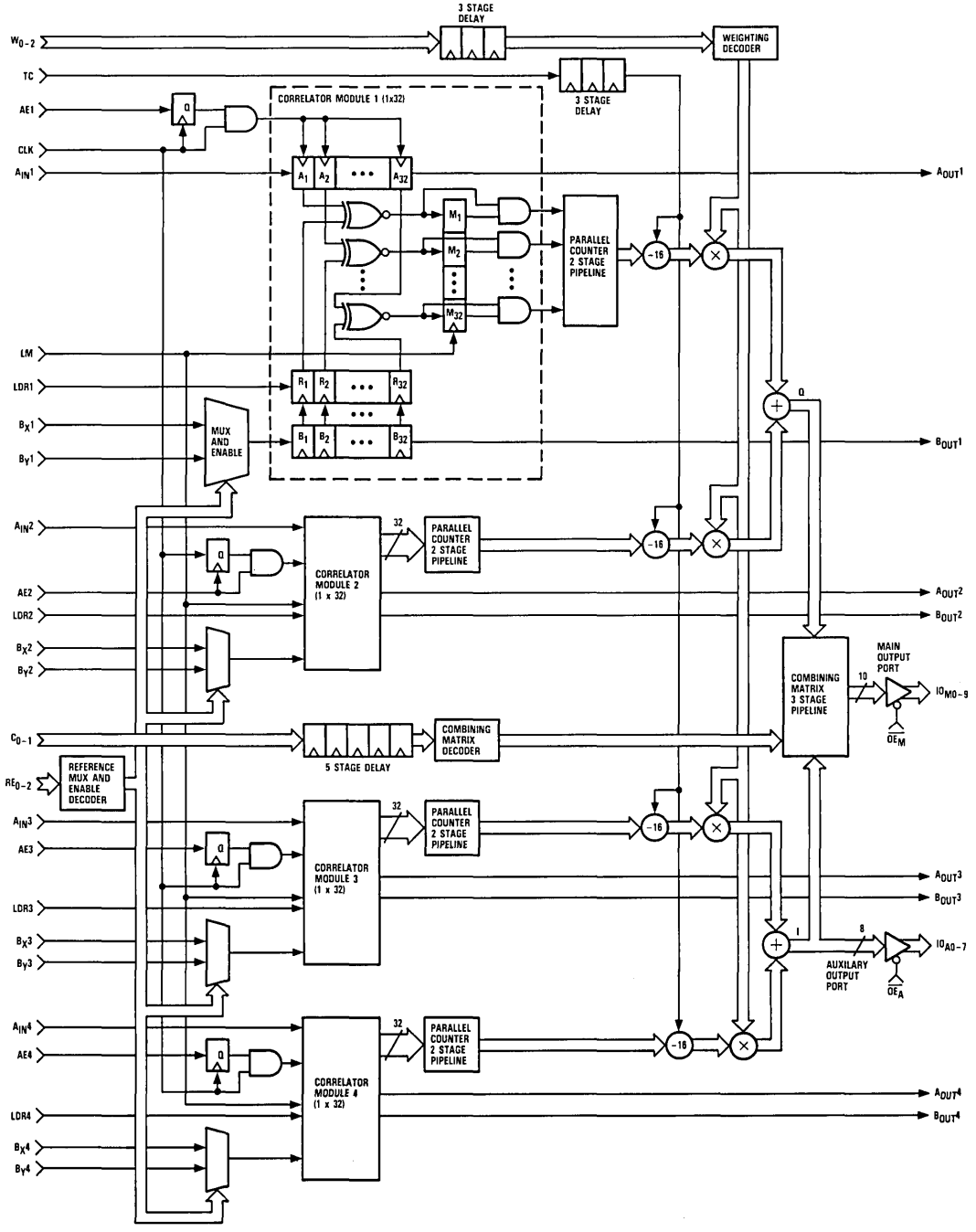
Decoder Inputs			Module Reference Port Selected	
			TMC2220	TMC2221
RE_2	RE_1	RE_0[1]	a b c d	a
0	0	0	0 0 0 0	0
0	0	1	0 0 0 X	
0	1	0	0 0 Y X	invalid
0	1	1	0 0 Y Y	
1	0	0	X X X X	X
1	0	1	Y X X X	
1	1	0	Y X Y X	Y
1	1	1	Y Y Y Y	

Note: The LSB of the decoder, RE_0, is not used on the TMC2221.

TMC2221 Functional Block Diagram



TMC2220 Functional Block Diagram



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TMC2243
Advance Information

Systolic FIR Filter Module
10-bit, 20MHz

The TRW TMC2243 is a three-stage, 10-bit systolic FIR filter module. This device is fully expandable and is specifically configured to support video signal processing requirements. The TMC2243 comprises three 10-bit multiply and add (MAD) cells, each with special "feedthrough registers" which support zero coefficient taps. These registers are ordinarily in transparent mode; enabling them will insert a zero coefficient tap into the filter. On each clock cycle, a 2-bit coefficient write enable control allows any one of the three coefficients to be modified using the data at the coefficient input bus. Adaptive filtering is facilitated by this programmability.

The function SUMOUT(n) = SUMIN(n-3) + D(n-4)K1 + D(n-3)K2 + D(n-2)K3 is performed by the device, the basic computation of a FIR filter. The data, D(i), and the coefficients, K(i), are 10-bit two's complement numbers. The SUMIN and SUMOUT buses are 16 bits wide to allow for word growth. The 16-bit incoming sum ($SUMIN_{21-6}$) is sign-extended by one bit, yielding a 17-bit two's complement number. Additionally, 1/2 LSB rounding is implemented by appending 100000, thereby expanding the data to 23 bits. In order to minimize rounding and overflow errors, the internal summation paths are 23 bits. An overflow flag indicates when two's complement overflow beyond the representable number range has occurred.

The TMC2243 is built with TRW's OMICRON-C™ 1-micron CMOS process. The device operates at a clock rate of 20MHz (50ns) in order to support video speed applications.

Features

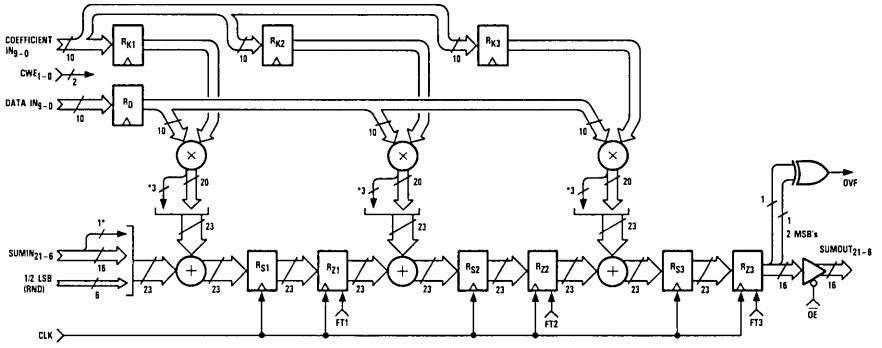
- 20MHz Guaranteed Clock Rate Over Standard Temperature Range (0° to 70°C)
- Systolic Architecture Allows For Expansion
- Efficient Implementation Of Zero Coefficient Taps
- Wide Internal Summation Paths For Overflow Protection
- Programmable Coefficients
- All Inputs And Outputs Registered
- Three-State Outputs
- Available In 64 Lead DIP

Applications

- FIR Filters
- Adaptive Filters
- One And Two Dimensional Convolution
- Video Processing

C

TMC2243 Functional Block Diagram



Note:
1. *The MSB is duplicated, thereby sign-extending.

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TMC3200
Advance Information

Floating Point Arithmetic Unit
32/34 bits, 125ns

The TRW TMC3200 is a 32/34-bit floating point arithmetic unit. It performs operations on floating point numbers in either IEEE standard 32-bit or an extended 34-bit format, and also accommodates a 24-bit two's complement integer (fixed point) format. Full conversion flexibility between the three data formats is available. The TMC3200 is built with TRW's OMICRON-C™ 1-micron CMOS process. With a cycle time of 125ns, the throughput rate of the TMC3200 is 8Mflops (Million floating point operations per second).

All data and instructions are registered. The input operands are selected from the input bus, floating point zero, and the accumulate path. The input operands each enter on 17-bit buses at alternate rising edges of the double-speed chip master clock (16MHz). The 8-bit instruction register latches inputs which control the operand selection, the ALU instruction, the data format and the rounding method. Renormalizing, rounding, and limiting logic are provided to ensure proper handling of special cases and correct output data formatting. The result is output as two words on successive chip master clock cycles, and it emerges through a 17-bit three-state output port.

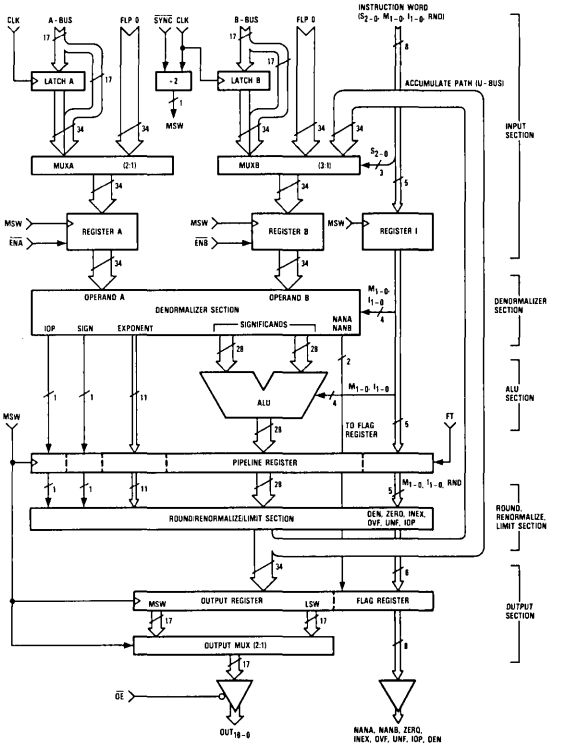
Features

- 8Mflop Throughput Rate (125ns Pipelined Cycle Time)
- IEEE Standard 754 Draft 10.0 32-Bit Or Extended 34-Bit Floating Point Data Format
- Integer Two's Complement 24-Bit (Fixed Point) Data Format
- Full Conversion Between All Data Formats
- Flexible Data Source Selection
- Internal Accumulator Feedback Path
- Selection Of Unbiased Round-To-Nearest And Round-Toward-Zero
- Automatic Limiting For Overflow/Underflow Cases
- All Inputs And Outputs TTL Compatible
- Available In 84 Contact Chip Carrier or 88 Pin Grid Array

Applications

- Matrix Operations And Geometric Transforms
- ALU In Microprogrammed Array Processors
- Graphics And Image Processing
- Floating Point Digital Filters And FFTs
- Radar And Sonar Signal Processors
- Use With 16-Bit Machines (Arithmetic Processors)

TMC3200 Functional Block Diagram



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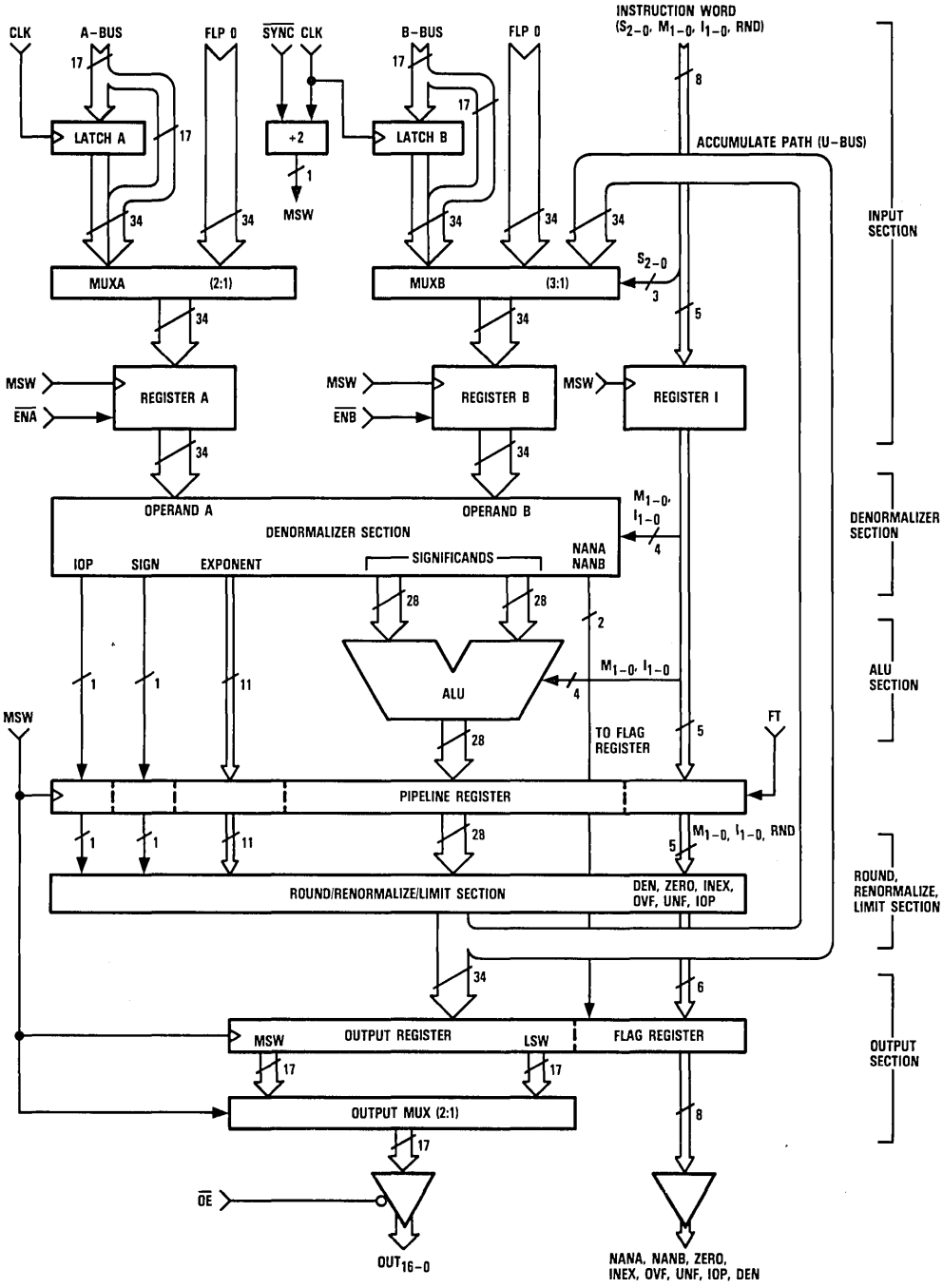
Functional Block Diagram



Functional Description

The TMC3200 is functionally divided into five sections: the input section, the denormalizer, the ALU, the round/renormalize/limit section, and the output section.

Input Section

The input section accepts the A and B operands, along with the 8-bit instruction word. The instruction is decoded in this section, determining the action of the A and B source multiplexers, the ALU operation, the rounding mode, and data format of the operands. The chip master clock (CLK) is divided by two, generating the Most Significant Word (MSW) signal, which is used internally for I/O multiplexing and is also available as an output flag.

The A and B operands each enter on their respective 17-bit input buses. Input preload registers clocked by the 16MHz chip master clock latch in the data on the input buses at the rising edge of CLK. Provided the enable controls for the operand registers ($\overline{ENA}$ and $\overline{ENB}$) are LOW, the data present at the preload registers and the data present at the input bus are simultaneously loaded into the operand registers at the rising edge of internal signal MSW. This means that the preload registers need to have the MSW loaded with the rising edge of CLK one cycle before the MSW signal goes HIGH, and the LSW must be present at the input bus when signal MSW goes HIGH. The SYNChronization control ($\overline{SYNC}$) aligns the MSW signal with the chip master clock. The MSW and LSW of the incoming operands must be present at the input bus on alternate cycles of CLK.

The operand registers are loaded with every other cycle of the master clock. Note that the preload register is strobed every cycle of CLK, though its contents are loaded into the operand registers only on alternate cycles of CLK.

The 8-bit instruction word is loaded into the instruction register at the rising edge of CLK, so it must be input at the same time as the MSW of the operands with which it is associated. The instruction word must be held through both load cycles (MSW and LSW input) of the data to which it applies. The instruction word is divided into four fields: one to control the operand source multiplexers (S_{2-0}), one to select the data format (M_{1-0}), one to control the arithmetic operation performed (OP_{1-0}), and one to control the rounding method ($\overline{RND}$). The A operand can be selected from two possible sources: the A input bus or a hardwired floating point zero. The B operand can be selected from three possible sources: the B input bus, the accumulator feedback path, or a floating point zero. The input and output data formats may be selected from 32-bit floating point, 34-bit floating point, or 24-bit integer (fixed point). The input and output formats may differ. The arithmetic operation performed is selected from A+B, A-B, B-A, -A-B, and CONVB (convert B to different data format). The rounding method is either IEEE (unbiased) round-to-nearest, or IEEE round-toward-zero (truncation).

Denormalizer Section

This section prepares the operands for the ALU by denormalizing the operand with the smaller exponent. This section also expands the exponent field to 11 bits and the significand field to 28 bits. This is done to accommodate the calculation of intermediate results to the precision required by the IEEE 32-bit and the extended 34-bit data formats. Since integers require no denormalization, this section is bypassed when integers are input.

The denormalizer section consists of an exponent comparator, a sign processor, zero-detectors, a denormalizing barrel shifter, and the subtraction inverter. The denormalizer generates floating point numbers with identical exponents (if possible) which can be directly added by the ALU. Input traps identify special cases which require separate treatment.

The exponent comparator detects the special IEEE trap conditions of zero (-512 in the 34-bit format) and 255 (511 in the 34-bit format), identifies the larger exponent, and calculates the absolute difference between the two exponents. The magnitude of the difference between the two exponents determines the amount of shift performed by the denormalizing barrel shifter.

The denormalizing barrel shifter can right-shift the significand of the operand having the smaller exponent as required, up to 25 places (after which the significand field becomes zero, with the "sticky bit" set). The amount of right-shift is equal to the difference between the exponents, as computed by the exponent comparator. Guard, round, and sticky bits are generated as specified in the IEEE standard. The MSBs of the shifted significand are zero-filled as they are downshifted. A no-shift capability handles the cases of equal operand exponents and integer operands.

The sign processor and the subtraction inverter handle the signs of the operands and support subtraction, respectively. The operands entering the ALU are modified as needed to ensure that a positive fraction field results; the appropriate sign is computed and appended.

ALU Section

The outputs of the denormalizer section are the larger incoming exponent, various status flags, sign information, and the two 28-bit significands. The ALU handles the 28-bit significands and the sign information. Input to this section is "preconditioned" so that it can perform either "A + B" or "A - B." The arithmetic follows the standard IEEE 32-bit, extended 34-bit, or integer rules, as appropriate. The ALU output is a 28-bit significand field.

The ALU output, the exponent, the sign information, the Invalid OPeration (IOP) flag, and five instruction bits are the inputs to the 46-bit pipeline register. This register may be enabled by bringing the FeedThrough (FT) control LOW. When FT=1, the pipeline register is transparent.

Round/Renormalize/Limit Section

The TMC3200 supports IEEE standards for "unbiased rounding toward nearest" when rounding is enabled ($\overline{RND}$ is LOW). When $\overline{RND}$ is HIGH, the TMC3200 truncates the result. The rounding adder is directly after the pipeline register and operates on the result generated by the ALU. The rounded result is the input to the renormalizer.

The renormalizer is able to shift right one bit, shift left up to 25 bits, or not shift at all, based on the state of the overflow bit and the other bits of the significand. If the overflow bit is set, the data is right-shifted to renormalize the number. If the overflow bit is not set, the number may be normalized already, in which case, no shift is required. In the event the number is not already normalized, the significand is left-shifted enough places to place a "1" in the (hidden) bit position immediately below the overflow bit. The direction and number of places shifted is noted and this information is used to adjust the exponent. The renormalizing shifter also provides the status flag "inexact result." The renormalize section also contains an exponent adder which modifies the exponent passed to it by the denormalizer (the larger of the two operand exponents). The exponent is decremented by one for each left shift which was required for the renormalization of the significand. In the event of a right shift, the exponent is incremented by one, and the exponent remains the same in the case of no shift. This exponent is examined for overflow or underflow of the output data format. There are two cases in which the renormalizer is disabled: when converting floating point to integer and when converting from 34-bit to 32-bit IEEE denormalized format.

The limiter uses the flags and the value of the exponent in order to replace overflowing numbers with a signed infinity or full-scale positive or negative integers as appropriate, underflowing numbers are replaced with zero. Invalid operations (infinity minus infinity or NaN plus any number) trigger NaN output. In cases other than described above, the limiter will output the result of the renormalizer unchanged.

Output Section

The output section contains the feedback accumulate path (U path), the 42-bit output register (34-bit output data, 8 flags), the output multiplexer, and the output buffers.

The U path is a 34-bit feedback path to the input section of the TMC3200 which feeds into the B operand multiplexed register. This bus carries the output of the limiter section back so that a 34-bit representation of the result being clocked into the output register is available simultaneously at the input of the B operand register, meeting the setup requirements of this register.

The output register is clocked by the MSW signal, which runs at half the rate of the system clock. The contents of this register will be the 34-bit output from the limit section, along with the flags (ZERO, DENormalized result, OVerFlow, UNderFlow, INEXact result, NAN in A, NAN in B, Invalid OPeration).

The flags are valid for the duration for which a result is held in the output register, except for the NANA and NANB flags. These flags are set when their particular input operand is a NAN and will remain set until a new legal operand is loaded. These flags are based on the operands only; ALU results flushed to NANs do not set the NAN flags. The remaining flags become valid with their corresponding results and remain as long as the associated result is in the output register. Since the flags are not three-stated, they are independent of the $\overline{OE}$ control.

The output multiplexer selects either the most or least significant word of the result and presents it at the inputs of the output buffers. The output multiplexer is controlled by the signal MSW, selecting the most significant word when MSW is HIGH, the least significant word when MSW is LOW. The output buffers are three-stated. When Output Enable ($\overline{OE}$) is LOW, the buffers drive the output bus, when $\overline{OE}$ is HIGH, the drivers are in the high-impedance state.

TMC3201
Advance Information

Floating Point Multiplier
32/34 bits, 125ns

The TRW TMC3201 is a 32/34-bit floating point multiplier. It multiplies numbers in either IEEE standard 32-bit or extended 34-bit floating point formats. The TMC3201 is built with TRW's OMICRON-C™ 1-micron CMOS process. With a cycle time of 125ns, the throughput rate of the TMC3201 is 8Mflops (Million floating point operations per second).

The data, controls, and status flags are registered. The input operands each enter on 17-bit buses at alternate rising edges of the double-speed chip master clock (16MHz). The instruction register latches in controls for rounding mode and data format. Renormalizing, rounding, and limiting logic are provided to ensure proper handling of special cases and proper formatting of the output data. The result is output as two words on successive chip master clock cycles, and it emerges through a 17-bit three-state output port.

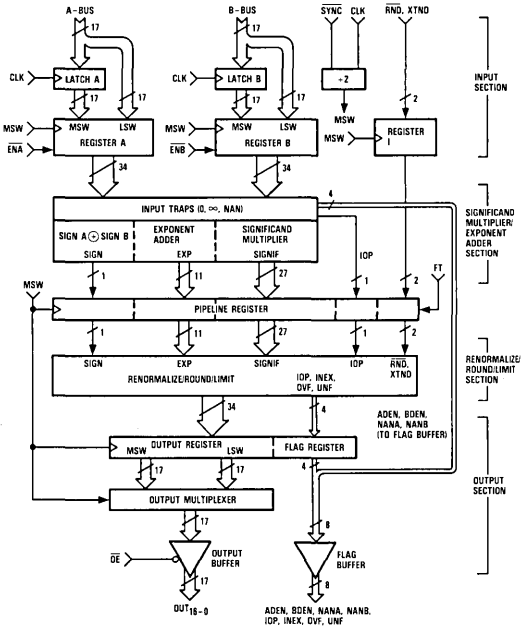
Features

- 8Mflop Throughput Rate (125ns Pipelined Cycle Time)
- IEEE Standard 754 Draft 10.0 32-Bit Or Extended 34-Bit Floating Point Data Format
- Selection Of Unbiased Round-To-Nearest And Round-Toward-Zero
- Automatic Limiting For Overflow/Underflow Cases
- All Inputs And Outputs TTL Compatible
- Available In 84 Contact Chip Carrier Or 88 Pin Grid Array

Applications

- Matrix Operations And Geometric Transforms
- ALU In Microprogrammed Array Processors
- Graphics And Image Processing
- Floating Point Digital Filters And FFTs
- Radar And Sonar Signal Processors
- Use With 16-Bit Machines (Arithmetic Processor)

TMC3201 Functional Block Diagram



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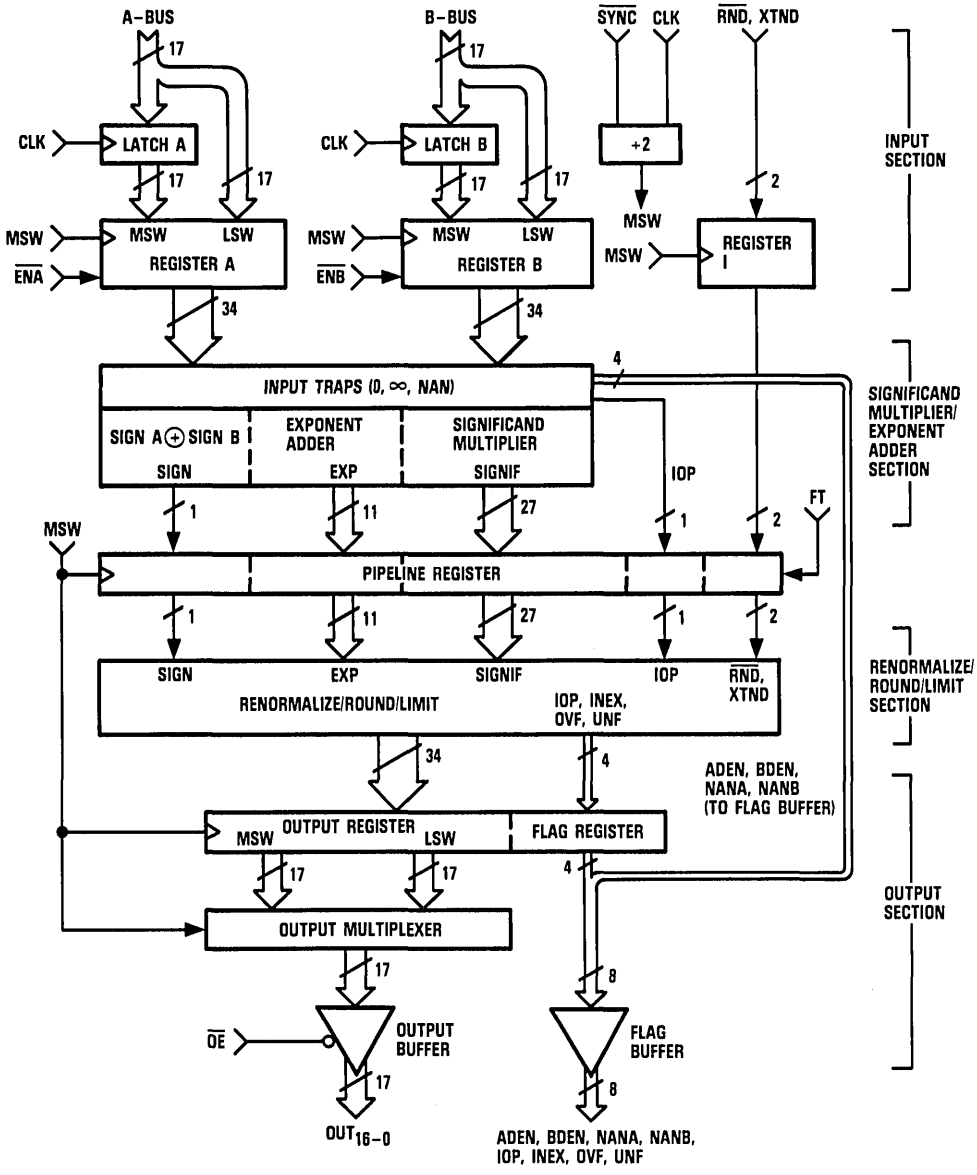
Functional Block Diagram



Functional Description

The TMC3201 is functionally divided into four sections: the input section, the significand multiplier/exponent adder, the renormalize/round/limit section, and the output section.

Input Section

The input section accepts the A and B operands, along with the 2-bit instruction word. The instruction is decoded in this section, determining the rounding mode and data format of the operands. The chip master clock (CLK) is divided by two, generating the Most Significant Word (MSW) signal, which is used internally for I/O multiplexing and is also available as an output flag.

The A and B operands each enter on their respective 17-bit input buses. Input preload registers clocked by the 16MHz chip master clock latch in the data on the input buses at the rising edge of CLK. Provided the enable controls for the operand registers ($\overline{ENA}$ and $\overline{ENB}$) are LOW, the data present at the preload registers and the data present at the input bus are simultaneously loaded into the operand registers at the rising edge of internal signal MSW. This means that the preload registers need to have the MSW loaded with the rising edge of CLK one cycle before the MSW signal goes HIGH, and the LSW must be present at the input bus when signal MSW goes HIGH. The SYNChronization control ($\overline{SYNC}$) aligns the MSW signal with the chip master clock. The MSW and LSW of the incoming operands must be present at the input bus on alternate cycles of CLK. The operand registers are loaded with every other cycle of the master clock. Note that the preload register is strobed every cycle of CLK, though its contents are loaded into the operand registers only on alternate cycles of CLK.

During the input operation, the inputs A and B are tested for the special cases of infinity, zero, NaNs, and denormalized numbers. Internal flags which identify these cases are generated. If NaNs are found, NANA or NANB flag is set immediately; these internal flags are also available as output signals. In this event, the product output will be the product NaN and the Invalid OPeration (IOP) flag will be set. Multiplication of zero x infinity also triggers a NaN output and sets the IOP flag. The TMC3201 is not able to process denormalized operands, and in the event of denormalized incoming operands, the appropriate ADEN or BDEN flags are set. The product output in this case will be zero.

Significand Multiplier/Exponent Adder

Floating point multiplication involves multiplication of the significand fields and addition of the exponent fields. The 24 x 24 bit multiplier generates the most significant 26 bits of the product, along with a "sticky bit" which is the logical OR of the low order 22 bits of the binary product. The 23 bits of the input fractional fields are input along with the implicit "hidden bit" (assumed to be a "1"). The 24-bit numbers are multiplied, though only the high order 26 bits are output. The output of the significand multiplier is a 27-bit number consisting of the overflow bit, the "hidden bit," the 23 bits of the fractional output, a guard bit, and a "sticky bit." This output is latched by the pipeline register which follows the multiplier array.

The exponents in floating point multiplication are added. The A and B exponent fields are added, generating an 11-bit nonbiased two's complement product exponent. This result is passed to the pipeline registers, and the exponent adjust section performs further processing before final output.

The 27-bit significand and the 11-bit exponent are the inputs to the pipeline register, along with the instructions, the Invalid OPeration flag (IOP), and the sign information. This 42-bit word is latched into the pipeline register on the rising edge of the signal MSW, provided that the FeedThrough control (FT) is LOW.

Renormalize/Round/Limit Section

The significand emerging from the pipeline register is tested for overflow. The significand field overflow bit is the MSB of the 27-bit significand, and if it is a "1," an overflow has occurred. This is compensated for by a right shift of one bit with an associated increment of the exponent by one. After the shift (if one was required), the overflow and hidden bits are no longer needed, hence they are dropped from the significand field. The renormalized significand is passed to the rounding adder.

If the $\overline{RND}$ control is LOW, the TMC3201 will round-to-nearest, according to IEEE standard rules. If $\overline{RND}$ is HIGH, the TMC3201 will truncate (IEEE round-toward-zero). Note that there is exactly one case where rounding can generate an overflowed result. In this case, the product is right-shifted and the exponent is incremented by one. The rounded product is output as a 23-bit number, with the "hidden bit" now guaranteed to be a "1."

C

The exponent emerging from the pipeline register is an 11-bit doubly biased exponent. The extra IEEE bias of decimal 127 is subtracted from the "raw exponent" and any increments necessary due to right-shifting of the significand field are made. This 12-bit exponent is checked for values of greater than or equal to 255 decimal (for IEEE 32-bit format) or 511 (for extended 34-bit format). These conditions signify an overflow. Underflow has occurred if the exponent is less than or equal to zero (IEEE 32-bit) or -512 (extended 34-bit). The ten LSBs of the exponent and the rounded significand enter the limit section.

The limiter forces the significand and exponent fields to clean signed infinities, clean zero, or the TMC3201 NaN if appropriate. Overflow cases are forced to the signed infinities, underflow and zero cases are forced to a clean zero, and invalid operation cases are forced to the NaN. Additionally, the two status flags, OVerFlow (OVF) and UNderFlow (UNF), are generated for output in this section. The output of this section is a 34-bit field, interpreted as either IEEE 32-bit or extended 34-bit data. The output of the limit section goes directly to the product register.

Output Section

The output section contains the 38-bit output register (34-bit output data, 4 flags), the output multiplexer, and the output buffers. The output register is clocked by the MSW signal, which runs at half the rate of the system clock. The contents of this register will be the 34-bit output from the limit section, along with the flags. The flags are valid for the duration for which a result is held in the output register, except for the NANA, NANB, ADEN, and BDEN flags. These flags are set when their particular input operand is a NAN or denormalized, respectively, and will remain set until a new legal operand is loaded. These flags are based on the operands only; results flushed to NANs (for example, zero x infinity) do not set the NAN flags. The remaining flags become valid with their corresponding results and remain as long as the associated result is in the output register. Since the flags are not three-stated, they are independent of the $\overline{OE}$ control.

The output multiplexer selects either the most or least significant word of the result and presents it at the inputs of the output buffers. The output multiplexer is controlled by the signal MSW, selecting the most significant word when MSW is HIGH, the least significant word when MSW is LOW. The output buffers are three-stated. When Output Enable ($\overline{OE}$) is LOW, the buffers drive the output bus, when $\overline{OE}$ is HIGH, the drivers are in the high-impedance state.

TMC3220
Advance Information

Three Port Register File
16 words x 9 bits, 20MHz

The TRW TMC3220 is a 16-word x 9-bit three port register file with two independent read ports and one write port. Internally, the device comprises two separate cores of 16-word x 9-bit dual port RAMs. Separate write enables, along with a single 4-bit write address allow either or both core RAMs to receive a given input data word. On each clock cycle, the two 4-bit read addresses can each access any of the 16 words of memory. Ordinarily, the two write enables are tied together, and the TMC3220 functions as a 16-word x 9-bit three port RAM. Separating the write enables causes the device to function as two independent two port RAMs.

The TMC3220 is specifically designed to operate with the TMC3200/3201 families of floating point devices, providing scratch memory and programmable interconnection supporting a variety of applications. The TMC3220 is built with TRW's OMICRON-C™ 1-micron CMOS process and will operate at a guaranteed clock rate of 20MHz. The clock rate of the TMC3220 also makes it suitable for video speed applications.

Features

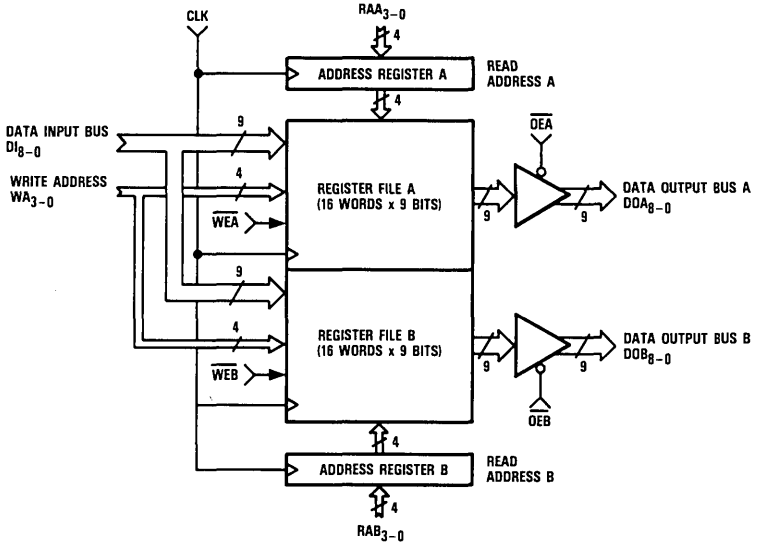
- Guaranteed 20MHz Clock Rate Over Standard Temperature Range (0° to 70°C)
- Configured For Use With 32/34 Bit Floating Point Family
- Two Fully Independent Read Ports
- Separate Write Enables
- Easily Cascadable In Word Size And Number of Words
- Low Power Consumption CMOS Process
- Three-State Outputs
- Available In 48 Lead DIP or 44 Contact Chip Carrier

Applications

- Cache Memory For High-Speed Processors
- Graphics And Image Processors
- High-Speed Program Memory And Controllers
- Storage For Video Processors

C

TMC3220 Functional Block Diagram



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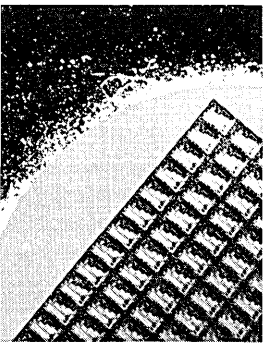
V L S I

D A T A

B O O K



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Evaluation Boards
D/A Converters
Multipliers
Multiplier-Accumulators
Special Function Products
Memory/Storage Products
Reliability
Package Information
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Application Notes And Reprints (Listings)

TRW LSI's line of monolithic high-speed analog-to-digital (A/D) converters consists primarily of devices that employ parallel "flash" architecture. The exceptions are the TDC1001 and TDC1002 successive approximation A/D converters. The entire line of A/D converters covers resolutions from four to nine bits and conversion rates from 1 to 100MSPS. All of these devices are built with TRW's proven 3D (triple-diffused) bipolar technology which provides significant advantages in performance, size, power, and reliability. Many products are now available manufactured with TRW's new OMICRON-B™ 1-micron process.

TRW LSI Products pioneered the development of monolithic high-speed A/D converters by introducing the TDC1007 in 1977. This device is an 8-bit 20MSPS A/D converter which has become an industry standard in video, radar, and imaging applications. The development of fine lithography techniques has yielded faster, more accurate, and less expensive A/D converters. Most of TRW LSI's A/D converters are available with an evaluation board which contains all peripheral circuitry necessary for quick and convenient operation of the device.

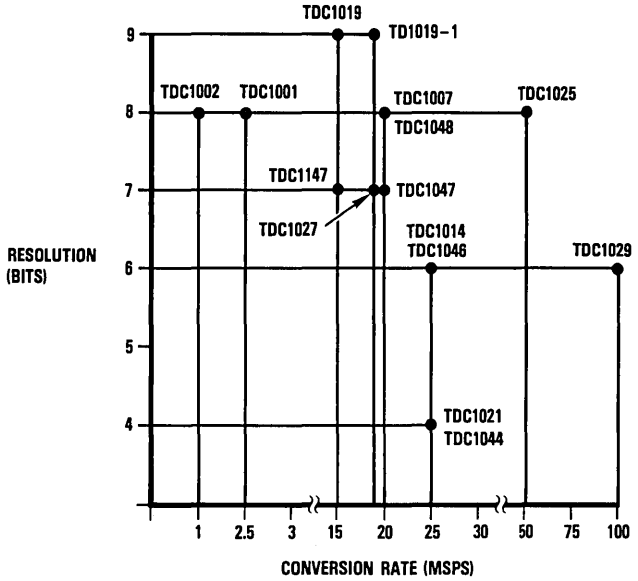


Figure 1. Resolution vs. Conversion Rate For TRW-LSI A/D Converters.

"Flash" A/D Converters

"Flash" A/D converters have three major functional sections: the comparator array, encoding logic, and output data latches. The input voltage to the A/D is compared with (2^N)-1 separate reference voltage points which differ from adjacent points by a voltage equivalent to one Least Significant Bit (LSB). N is the number of data outputs, or the resolution of the A/D converter in bits. The comparator reference voltage points are tapped from a reference resistor chain which is driven by an external reference voltage source.

The outputs from the (2^N)-1 comparators form a code sometimes referred to as a "thermometer" code (all comparators referred to voltages more positive than the input signal will be off, and those referred to voltages more negative then the input signal will be on). The "thermometer" code from the comparator array is then encoded into an N-bit binary word.

The conversion operation is controlled by a single CONVert (clock) signal which latches the N-bit results from the encoding logic. The output latches of the converter hold data valid while the conversion is taking place and are updated by the CONVert signal. Some converters have additional data controls which allow data formatting of straight binary, inverse binary, two's complement, or inverse two's complement notation.

Successive Approximation A/D Converters

Successive approximation A/D converters have three major functional sections: the comparator, D/A converter, and successive approximation register (SAR). The comparator compares the unknown input voltage to the output of the internal D/A. Successive approximation is an iterative process during which the SAR stores data from the comparator and presents new data to the D/A converter. At the end of the process, the data in the SAR drives the D/A converter to a level which is within 1/2 LSB of the unknown input voltage. At this time, the SAR data is the binary equivalent of the unknown input voltage.

Once the iterative process has terminated, the SAR data is latched in an output register and a "BUSY" signal will change state indicating that new output data is available.

Product	Resolution Bits	Conversion Rate [1] (MSPS)	Power Dissipation (Watts)	Package	Notes
TDC1001	8	2.5	0.7	J8	Successive approximation
TDC1002	8	1.0	0.7	J8	Successive approximation
TDC1007	8	20	2.7	J1, C1, L1	
				E1, P1	Evaluation boards
TDC1014	6	25	1.1	J7, B7	
				E1, P1	Evaluation boards
TDC1019	9	15	4.7	J1, C1, L1	ECL compatible
				E1	Evaluation board
TDC1019-1	9	18	4.7	J1, C1, L1	Speed selected version
TDC1021	4	25	0.6	J9	
TDC1025	8	50	3.9	C1, L1	ECL compatible
				E1	Evaluation board
TDC1027	7	18	1.8	J7, B7	
TDC1029	6	100	2.1	J7, J6	ECL compatible
				E1	Evaluation board
TDC1044	4	25	0.4	J9, N9	
TDC1046	6	25	0.8	J8, B8	
TDC1047	7	20	1.1	J7, B7, C3	
				E1	Evaluation Board
TDC1048	8	20	1.6	J6, C3, B6	
				E1	Evaluation board
TDC1147	7	15	1.1	J7, B7, C3	

Note: 1. Guaranteed, Worst Case, T_A = 0°C to 70°C.

TDC1001 (400ns)
TDC1002 (1μsec)

Successive Approximation A/D Converters

8-bit, 2.5MSPS, 1MSPS

The TRW TDC1001 and TDC1002 analog-to-digital converters are high-speed, 8-bit successive approximation devices. These bipolar, monolithic converters offer significant advantages in size, cost, and performance, as well as high reliability and low-power consumption.

All digital interfaces are TTL compatible. A single +5VDC supply is required by the digital circuitry while -5VDC is required by the analog portion of the device. The analog and digital ground planes are internally isolated.

The TDC1001 and TDC1002 consist of a comparator, reference buffer, 8-bit D/A converter, successive approximation register, output register, and control circuitry.

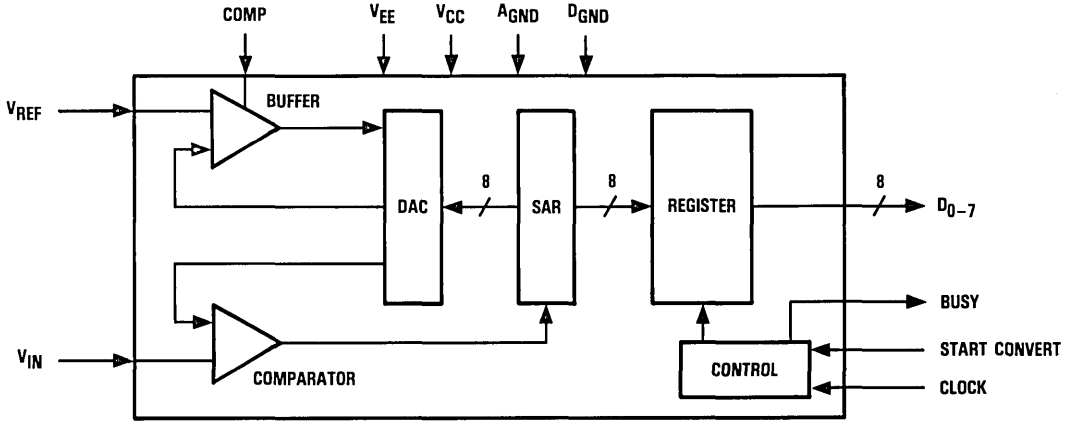
Features

- 8-Bit Resolution
- Binary Output Coding
- TTL Compatible
- ±1/2 LSB Linearity
- Parallel Output Register
- 600mW Power Dissipation
- Available In 18 Lead DIP

Applications

- Microprocessor Systems
- Numerical Control Interface
- Data Acquisition Systems

Functional Block Diagram



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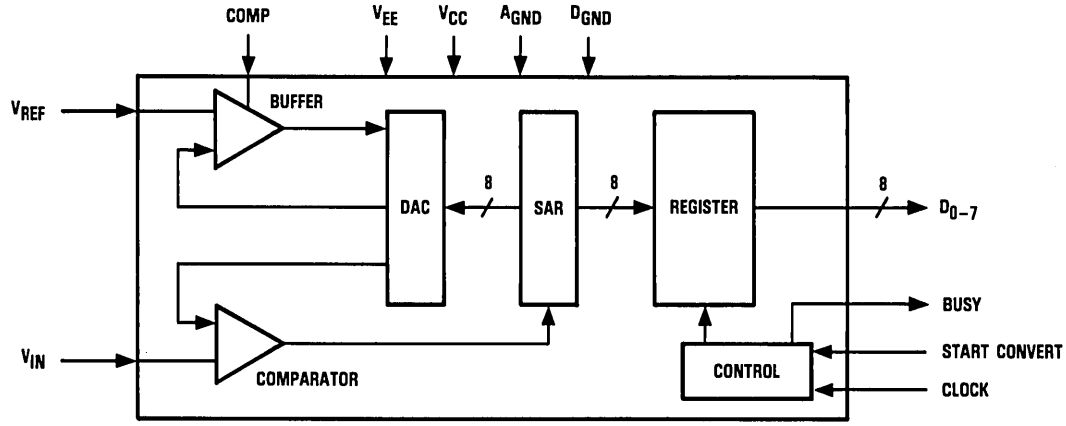
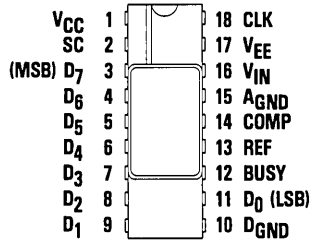
Functional Block Diagram



Pin Assignments



18 Lead DIP – J8 Package

Functional Description

General Information

The TDC1001 and TDC1002 consist of six functional sections: comparator for the analog input, reference buffer, 8-bit D/A converter (DAC), successive approximation register (SAR), output register, and control circuitry. The SAR and comparator will sequentially compare the analog input to the DAC output. The conversion process requires nine clock cycles.

Power

The TDC1001 and TDC1002 operate from separate analog and digital power supplies. Analog power (V_{EE}) is −5.0VDC and digital power (V_{CC}) is +5.0VDC. All power and ground pins must be connected.

Separate decoupling for each supply is recommended. The return for I_{EE}, the current drawn from the V_{EE} supply, is A_{GND}. The return for I_{CC}, the current drawn from the V_{CC} supply, is D_{GND}.

Name	Function	Value	J8 Package
V_{EE}	Analog Supply Voltage	−5.0VDC	Pin 17
V_{CC}	Digital Supply Voltage	+5.0VDC	Pin 1
A_{GND}	Analog Ground	0.0VDC	Pin 15
D_{GND}	Digital Ground	0.0VDC	Pin 10

Reference

The TDC1001 and 1002 accept a nominal input reference voltage of −0.5VDC. The voltage should be supplied by a precision voltage reference, as the accuracy of this voltage will have a significant effect on the overall accuracy of the system. The reference voltage input pin should be bypassed to A_{GND} as close as possible to the device terminal.

Name	Function	Value	J8 Package
V_{REF}	Reference Voltage Input	−0.5VDC	Pin 13

Analog Input

The analog input range of the device is set by the reference voltage. This is nominally −0.5VDC with an absolute tolerance of ±0.1VDC. Since the device is a successive approximation type A/D converter, a sample-and-hold circuit may be required in some applications.

Name	Function	Value	J8 Package
V_{IN}	Analog Input	0 to −0.5V	Pin 16

D

Conversion Timing Description

The timing sequence of the TDC1001 and 1002 is typical of successive approximation converters. Nine clock cycles are required for each conversion. Start Convert must transition from LOW to HIGH a minimum of t_S prior to the leading edge of the first convert pulse, and must remain HIGH a minimum of t_H after the edge.

This first cycle clears the BUSY flag and prepares the device for a new conversion. The following eight clock cycles convert each data bit (MSB first, LSB last). During these eight clock cycles, the analog input must be held stable (to within 1/2 LSB). At t_D nanoseconds after the rising edge of the eighth clock pulse, the seven most significant bits are valid (and the BUSY signal goes LOW). At t_D nanoseconds after the ninth clock pulse the LSB is valid, and the conversion is completed.

Name	Function	Value	J8 Package
SC	Start Convert Input	TTL	Pin 2
BUSY	Busy Flag Output	TTL	Pin 12
CLOCK	Convert Clock Input	TTL	Pin 18

Data Outputs

The outputs of the TDC1001 and 1002 are TTL compatible and capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. The outputs hold the previous data a minimum time (t_D) after the rising edge of Start Convert (SC).

Name	Function	Value	J8 Package
D_7	MSB Output	TTL	Pin 3
D_6		TTL	Pin 4
D_5		TTL	Pin 5
D_4		TTL	Pin 6
D_3		TTL	Pin 7
D_2		TTL	Pin 8
D_1		TTL	Pin 9
D_0	LSB Output	TTL	Pin 11

Compensation Pin

The COMPensation pin (COMP), is provided for external compensation of the internal reference amplifier. The compensation capacitor must be connected between this pin and V_{EE}. A tantalum capacitor greater than 10μF is recommended for proper operation.

Name	Description	Value	J8 Package
COMP	Compensation Pin	>10μF	Pin 14

Output Coding

An analog input voltage of 0.0V will produce a digital output code of all zeros; an analog input voltage of -0.50V will produce a digital output code of all ones.

Figure 1. Timing Diagram

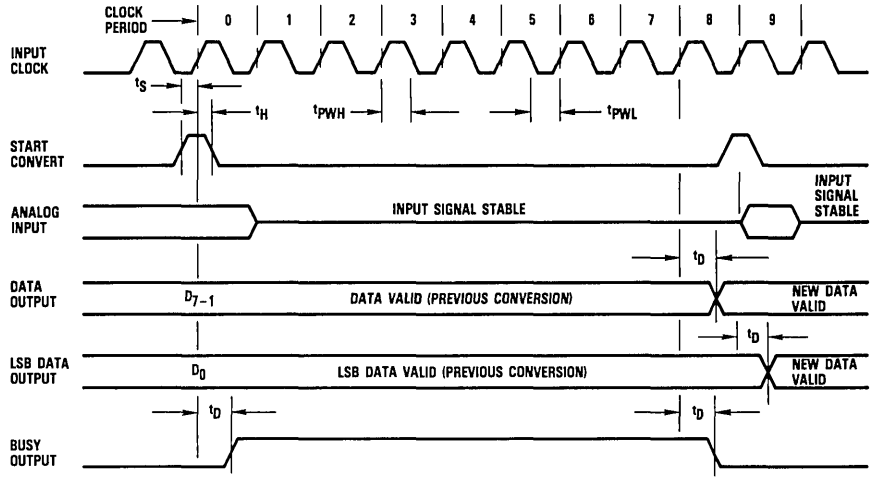


Figure 2. Simplified Analog Input Equivalent Circuit

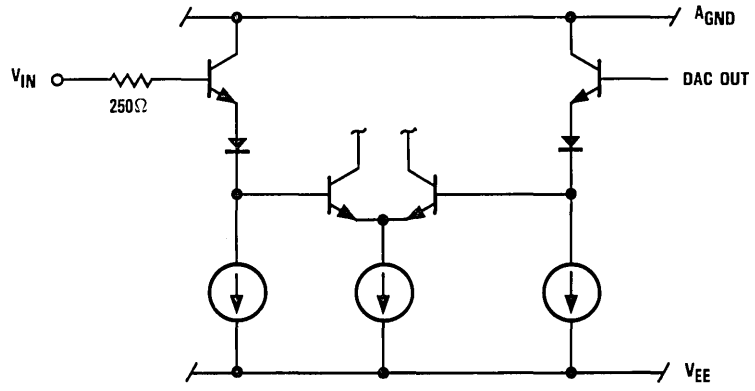


Figure 3. Digital Input Equivalent Circuit

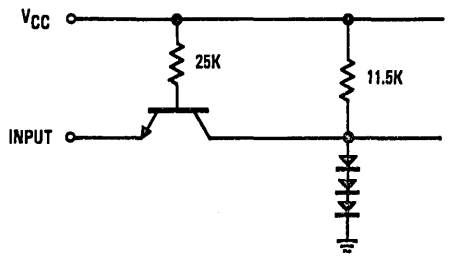
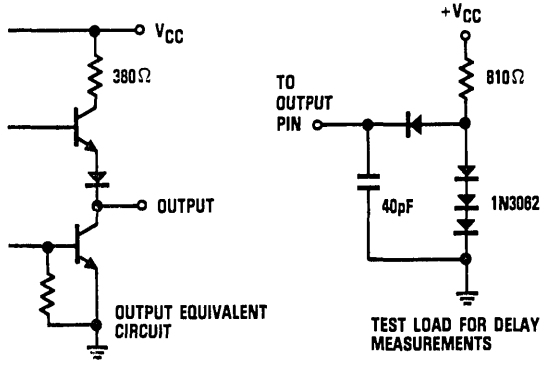


Figure 4. Output Circuits



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Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage

V_{CC} (measured to D_{GND}) ..... 0 to +6.0V
V_{EE} (measured to A_{GND}) ..... 0 to −6.0V
A_{GND} (measured to D_{GND}) ..... −0.5 to + 0.5V

Input Voltages

CLK, SC (measured to D_{GND}) ..... −0.5 to +5.5V
V_{IN}, V_{REF} (measured to A_{GND}) ..... +0.5V to V_{EE}V

Output

Applied voltage (measured to D_{GND}) ..... −0.5 to +5.5V [2]
Applied current, externally forced ..... −1.0 to +6.0ma [3,4]
Short circuit duration (single output in high state to D_{GND}) ..... 1 sec

Temperature

Operating, case ..... −60 to +140°C
junction ..... +175°C
Lead, soldering (10 seconds) ..... +300°C
Storage ..... −65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{EE}	Negative Supply Voltage	−4.75	−5.0	−5.25	−4.75	−5.0	−5.25	V
A_{GND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0.0	+0.1	−0.1	0.0	+0.1	V
t_{PWL}	Clock Pulse Width, LOW	20			20			ns
t_{PWH}	Clock Pulse Width, HIGH	20			20			ns
t_S	Start Convert, Set-Up Time	7			7			ns
t_H	Start Convert, Hold Time	16			16			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
V_{REF}	Reference Voltage	−0.4	−0.5	−0.6	−0.4	−0.5	−0.6	V
V_{IN}	Analog Input Voltage	0.0		−0.6	0.0		−0.6	V
T_A	Ambient Temperature, Still Air	0		+70				°C
T_C	Case Temperature				−20		+85	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = MAX, Static[1]		40		40	mA
I_{EE}	Negative Supply Current	V_{EE} = MAX, T_C = −20°C to +85°C		−80		−80	mA
I_{BIAS}	Analog Input Bias Current			10		10	μA
I_{REF}	Reference Current	V_{REF} = NOM		2.5		2.5	μA
R_{REF}	Total Reference Resistance		200		200		kOhms
R_{IN}	Analog Input Equivalent Resistance	V_{REF} = NOM	50		50		kOhms
C_{IN}	Analog Input Capacitance			10		10	pF
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.5V		−1.0		−1.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V		75		75	μA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OS}	Output Short Circuit Current			−25		−25	mA

Note:
1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Clock Rate	V_{CC}, V_{EE} = MIN TDC1001	22.5		22.5		MHz
		TDC1002	9.0		9.0		MHz
t_C	Conversion Time	V_{CC}, V_{EE} = MIN TDC1001		400		400	ns
		TDC1002		1000		1000	ns
t_D	Digital Output Delay	V_{CC}, V_{EE} = MIN		50		50	ns

D

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
E_{LI}	Linearity Error Integral, Independent	V_{CC}, V_{EE} = NOM		0.2		0.2	%
E_{LD}	Linearity Error Differential			0.2		0.2	%
T_{CG}	Gain Temperature Coefficient	V_{CC}, V_{EE} = NOM		+10		+10	ppm/°C
E_O	Offset Voltage			±7		±7	mV
T_{CO}	Offset Temperature Coefficient	V_{CC}, V_{EE} = NOM		−10		−10	μV/°C
E_G	Gain Error			1.5		2.0	%
T_{CIB}	I_{BIAS} Temperature Coefficient	V_{CC}, V_{EE} = NOM		−1.0		−1.0	%/°C

Application

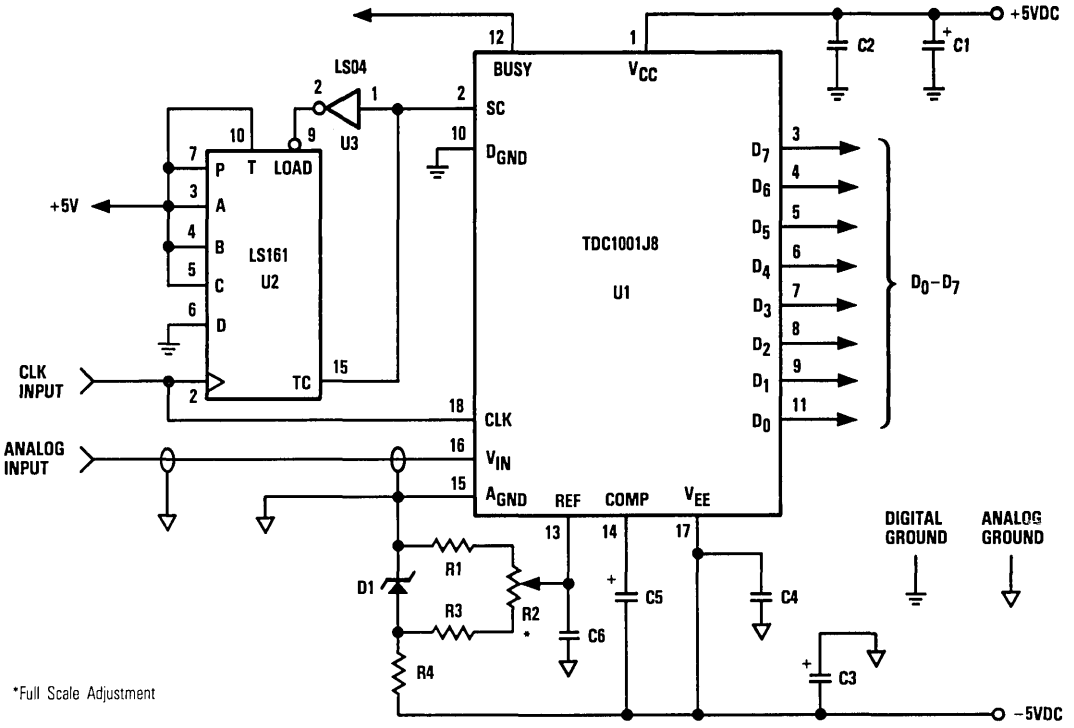
The TDC1001 and TDC1002 are high-speed, TTL compatible, SAR type A/D converters. The combination of very small analog signals and high-speed digital circuitry requires careful design of supporting analog/digital circuitry. Proper physical component layout, trace routing, and provision for sizeable analog and digital grounds are as important as the electrical design.

Two key design areas for fast, accurate A/D conversion are timing and grounding. The timing requirements for this device are detailed in Figure 1. Proper grounding is highly dependent on the board's mechanical layout and design constraints. In general, the noise associated with improper digital and analog ground isolation is synchronous with the clock and appears on the analog input.

Proper Design Practices Include:

- Sensitive signals such as clock, start convert, analog input, and reference should be properly routed and terminated to minimize ground noise pick-up and crosstalk. (Wirewrap is not recommended for these signals).
- Analog and digital ground planes should be substantial and common at one point only. Analog and digital power supplies should be referenced to their respective ground planes.
- Reference voltage should be stable and free of noise. Accuracy of the conversion is highly dependent on the integrity of this signal.
- The analog input should be driven from a low-impedance source (<25 Ohms). This will minimize the possibility of picking up extraneous noise.
- Ceramic high frequency bypass capacitors (0.001 to 0.01μF) should be used at the input pins of V_{CC}, V_{EE}, and REF. All pins should be bypassed to A_{GND} except V_{CC}.
- A tantalum capacitor of greater than 10μF should be connected from COMP (pin 14) to V_{EE}.

Figure 5. Typical Interface Circuit



Parts List

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Resistors

R1	909 Ohms	1%	1/8W
R2	100 Ohms		Multi-Turn Cermet Pot
R3	1.33 kOhms	1%	1/8W
R4	2.49 kOhms	1%	1/8W

Capacitors

C1, C3, C5	10.0 μF	25V
C2, C4	0.001 μF	50V
C6	0.005 μF	50V

Integrated Circuits

U1	TDC1001J8	TRW 8-bit A/D Converter
U2	74LS161	TTL 4-bit Counter
U3	74LS04	TTL Hex Inverter
D1	LM113-1.22	1.22V Bandgap Voltage Reference

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1001J8C	STD-T_A = 0°C to 70°C	Commercial	18 Lead DIP	1001J8C
TDC1001J8G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	18 Lead DIP	1001J8G
TDC1001J8R	EXT-T_C = -20°C to 85°C	Commercial	18 Lead DIP	1001J8R
TDC1001J8T	EXT-T_C = -20°C to 85°C	High Reliability[1]	18 Lead DIP	1001J8T
TDC1001J8H	EXT-T_C = -20°C to 85°C	Commercial With Burn-In	18 Lead DIP	1001J8H
TDC1002J8C	STD-T_A = 0°C to 70°C	Commercial	18 Lead DIP	1002J8C
TDC1002J8G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	18 Lead DIP	1002J8G
TDC1002J8R	EXT-T_C = -20°C to 85°C	Commercial	18 Lead DIP	1002J8R
TDC1002J8T	EXT-T_C = -20°C to 85°C	High Reliability[1]	18 Lead DIP	1002J8T
TDC1002J8H	EXT-T_C = -20°C to 85°C	Commercial With Burn-In	18 Lead DIP	1002J8H

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Note:
1. Per TRW document 70Z01757.

TDC1007

Monolithic Video A/D Converter
8-bit, 20MSPS

The TDC1007 is an 8-bit fully parallel (flash) analog-to-digital converter, capable of digitizing an input signal at rates up to 20MSPS (MegaSamples Per Second). It will operate accurately without the use of an external sample-and-hold amplifier, with analog input signals having frequency components up to 7MHz.

A single CONVert (CONV) signal controls the conversion operation of the device which consists of 255 sampling comparators, encoding logic, and a latched output buffer register. The device will recover from a full-scale input step in 20ns. Control inputs are provided to format the output in binary, two's complement, or inverse data coding formats.

The TDC1007 is patented under U.S. Patent No. 3283170 with other patents pending.

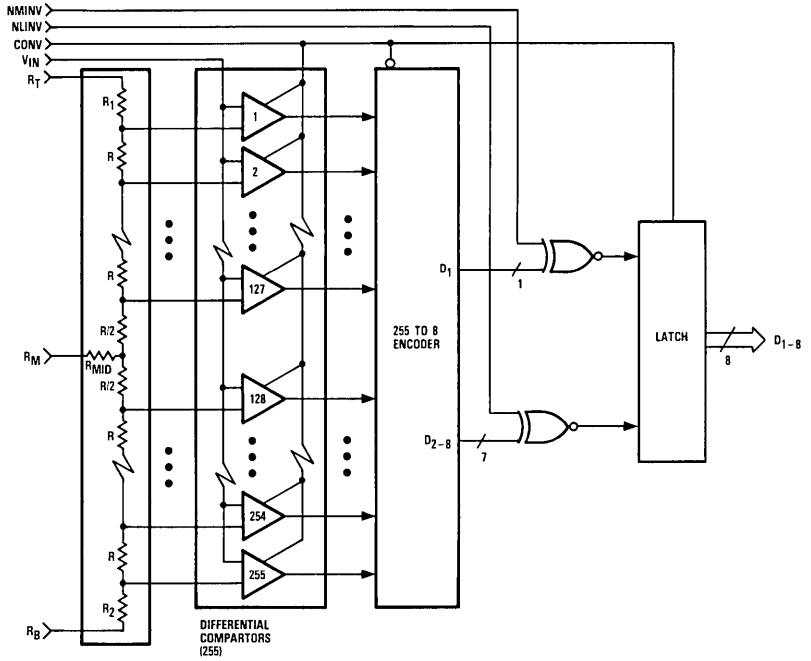
Features

- 8-Bit Resolution
- Conversion Rates Up to 20MSPS
- Sample-And-Hold Amplifier Not Required
- Bipolar Monolithic Construction
- TTL Compatible Inputs and Outputs
- Binary or Two's Complement Mode
- Differential Phase = 1.0 Degrees
- Differential Gain = 1.7%
- Evaluation Boards Available: TDC1007E1C or TDC1007P1C

Applications

- Video Systems 3x or 4x Subcarrier, NTSC or PAL
- Radar Systems
- High-Speed Multiplexed Data Acquisition
- Digital Signal Processing

Functional Block Diagram



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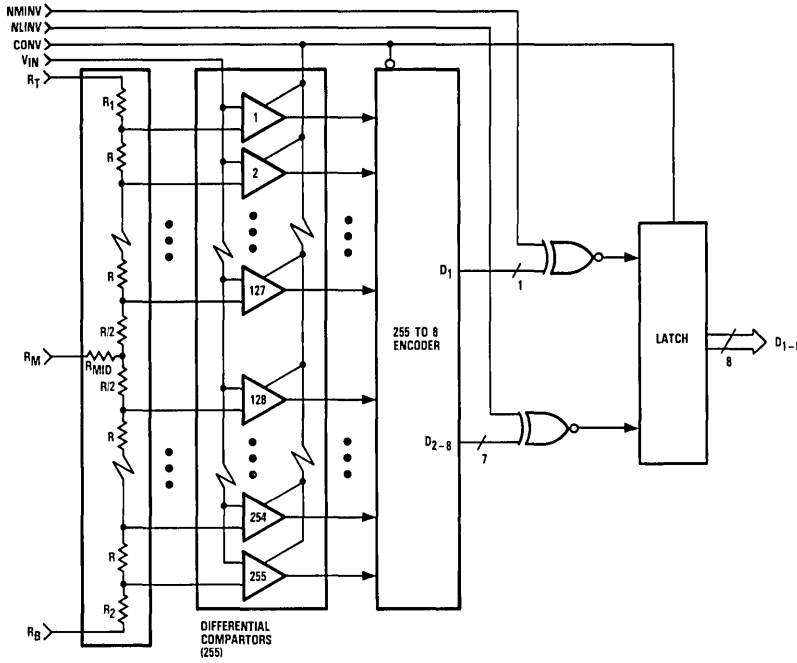
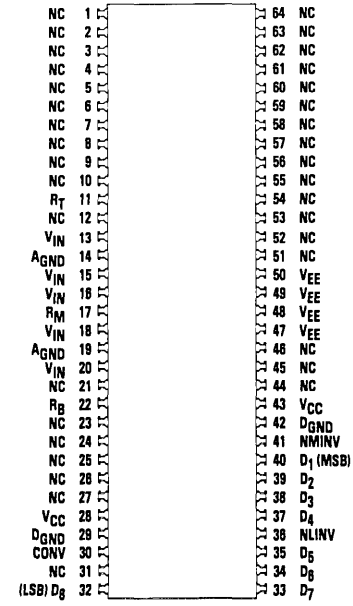
Functional Block Diagram

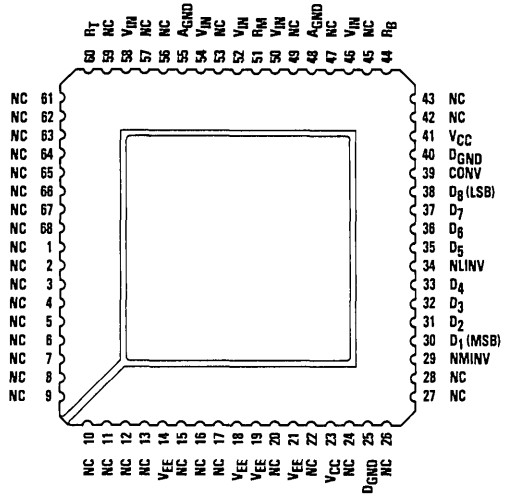


Pin Assignments



64 Lead DIP – J1 Package

Pin Assignments



68 Contact Or Leaded Chip Carrier – C1, L1 Package

Functional Description

General Information

The TDC1007 has three major functional sections: a comparator array, encoding logic, and output data latches. The input voltage is compared with 255 separate reference voltage points tapped from the reference resistor chain. The 255 comparator outputs form a code (sometimes referred to as a "thermometer" code, as all the comparators referred to voltages more positive than the input signal will be off, and those referred to voltages more negative than the input signal will be on). The "thermometer" code from the comparator array is encoded into an eight-bit binary word by the encoding logic section. Each of these eight results is sent through an exclusive-OR gate where they are inverted by use of the NMINV or NLINV inputs. This allows operation in binary, two's complement, or inverted data formats.

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Power

The TDC1007 operates from two supply voltages, +5.0V and −6.0V. The return for I_{CC}, the current drawn from the +5.0V supply, is D_{GND}. The return path for I_{EE}, the current drawn from the −6.0V supply, is A_{GND}. All power and ground pins must be connected.

Name	Function	Value	C1, L1 Package	J1 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pins 23, 41	Pins 28, 43
V_{EE}	Negative Supply Voltage	−6.0V	Pins 14, 18, 19, 21	Pins 47, 48, 49, 50
D_{GND}	Digital Ground	0.0V	Pins 25, 40	Pins 29, 42
A_{GND}	Analog Ground	0.0V	Pins 48, 55	Pins 14, 19

Reference

The TDC1007 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. V_{RT} (the voltage applied to the pin at the top of the reference resistor chain), and V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) should be between +0.1V and −2.1V, with the difference between them less than 2.1V. V_{RT} should be more positive than V_{RB} within that range. In order to insure optimum operation of the TDC1007, these points should be driven by low-impedance sources capable of providing the necessary reference resistor chain current. The voltages on R_T and R_B may be varied dynamically up to 7MHz. Due to variations in reference current with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are varied dynamically (as in an AGC application) a low-impedance reference source is required.

Name	Function	Value	C1, L1 Package	J1 Package
R_T	Reference Resistor (Top)	0.0V	Pin 60	Pin 11
R_M	Reference Resistor (Middle)	−1.0V	Pin 51	Pin 17
R_B	Reference Resistor (Bottom)	−2.0V	Pin 44	Pin 22

Control

Two control inputs are provided on the TDC1007 for changing the format of the output data. When NMINV is tied to a logic "0", the most significant bit of the output data is inverted; when NLINV is tied to a logic "0", the seven least significant bits of the output are inverted. By using these controls, the output data format can be binary, inverted binary, two's complement, or inverted two's complement. Output data versus input voltage and control input state is illustrated in the Output Coding table.

Name	Function	Value	C1, L1 Package	J1 Package
NMINV	Not Most Significant Bit INVert	TTL	Pin 29	Pin 41
NLINV	Not Least Significant Bit INVert	TTL	Pin 34	Pin 36

Convert

The analog input to the TDC1007 is sampled (comparators are latched) approximately 10ns after the rising edge of the CONV Signal. This time delay is the sampling time offset (t_{STO}) and varies only by a few nanoseconds from device to device and as a function of temperature. The short-term uncertainty (jitter) in sampling time offset is approximately 30 picoseconds. The output data is encoded from the 255 comparators on the falling edge of the CONV signal. The coded result is transferred to the output latches on the next rising edge of the CONV signal. Note that there are minimum pulse width (t_{PWH}, t_{PWL}) requirements on the waveshape of the CONV signal.

Name	Function	Value	C1, L1 Package	J1 Package
CONV	Convert	TTL	Pin 39	Pin 30

Analog Input

The input impedance of the TDC1007 varies with input signal level. As the signal varies, the comparator input transistors change from active to cut-off, causing the net input resistance and capacitance to change. To prevent this action from degrading the integrity or accuracy of the output data, it is desirable to drive the TDC1007 inputs from a low-impedance source (less than 25 Ohms). The input signal level should remain within the range of V_{EE} to +0.5V in order to prevent damage to the device. When the input is at a level between V_{RT} and V_{RB} reference voltages, the output data value will be directly proportional to the amplitude of the analog input signal. When the analog input is beyond the range of the reference voltage, the output data will be the appropriate full-scale value. Note that there are two components to the input bias current flowing into the V_{IN} pins. One component is constant for constant input voltage and is the sum of the bias currents of the subset of comparators that are active (I_{CB}). The other component is related to the action of the CONV signal on the comparator chain (I_{SB}). All analog input pins of the TDC1007 must be used in order to insure operation over the full input range.

Name	Function	Value	C1, L1 Package	J1 Package
V_{IN}	Analog Input Signal	0V to -2V	Pins 48, 50, 52, 54, 58	Pins 13, 15, 16, 18, 20

Outputs

The outputs of the TDC1007 are TTL compatible and capable of driving four low-power Schottky unit loads (54/74 LS). The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal, and the new data becomes valid after a maximum time of t_D. For optimum performance, 2.2 kOhm pull-up resistors are recommended.

Name	Function	Value	C1, L1 Package	J1 Package
D_1	MSB Output	TTL	Pin 30	Pin 40
D_2		TTL	Pin 31	Pin 39
D_3		TTL	Pin 32	Pin 38
D_4		TTL	Pin 33	Pin 37
D_5		TTL	Pin 35	Pin 35
D_6		TTL	Pin 36	Pin 34
D_7		TTL	Pin 37	Pin 33
D_8	LSB Output	TTL	Pin 38	Pin 32

D

No Connects

There are several pins labeled No Connect (NC), which have no connections to the chip. These pins may be left open.

Name	Function	Value	C1, L1 Package	J1 Package
NC	No Connect	Open	Pins 1-13, 15-17, 20, 22, 24, 26-28, 42, 43, 45, 47, 49, 53, 56, 57, 59, 61, 62-68	Pins 1-10, 12, 24-27, 31, 44-46, 51-64

Figure 1. Timing Diagram

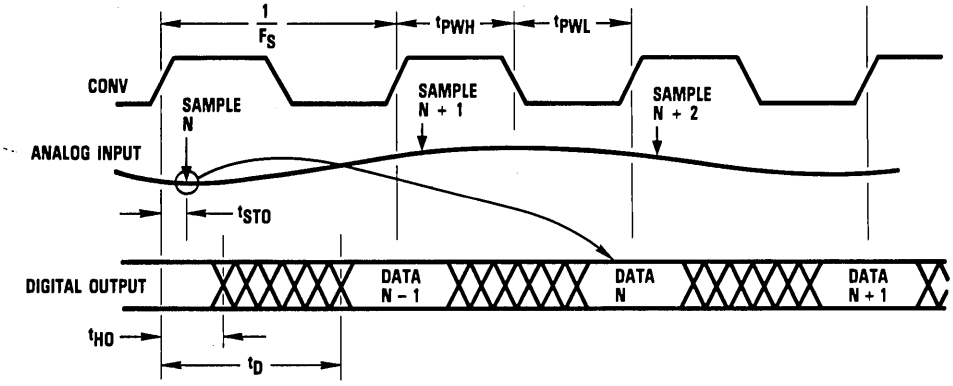
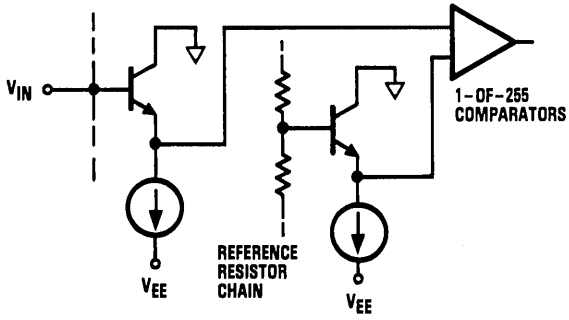
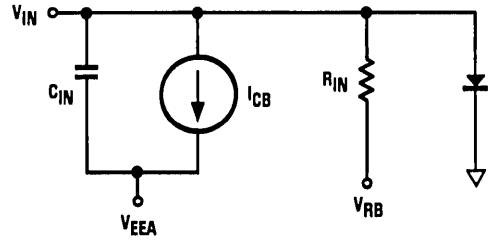


Figure 2. Simplified Analog Input Equivalent Circuit





C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

Figure 3. Digital Input Equivalent Circuit

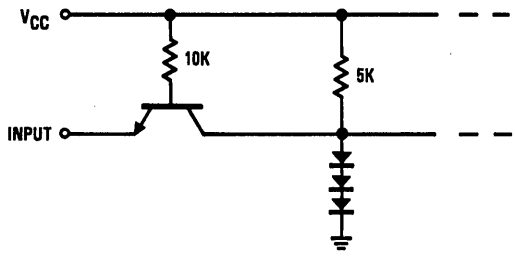
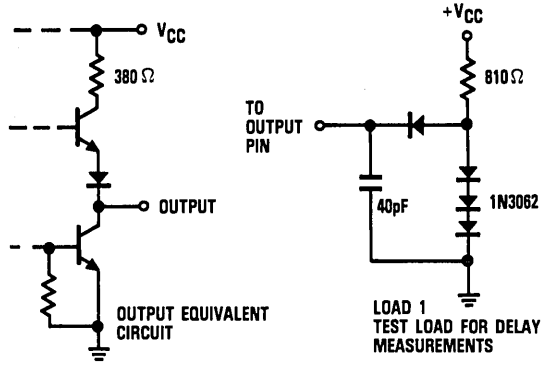


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	−1.0 to +1.0V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EE}V
V_{RT} (measured to V_{RB})	+2.2 to −2.2V

Output

Applied voltage (measured to D_{GND})	−0.5 to +5.5V [2]
Applied current, externally forced	−1.0 to +6.0mA [3,4]
Short circuit duration (single output in high state to ground)	1 sec

Temperature

Operating, ambient	−60 to +140°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage (Measured to D_{GND})	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Supply Voltage (Measured to A_{GND})	−5.75	−6.0	−6.25	−5.75	−6.0	−6.25	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0.0	0.1	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	25			25			ns
t_{PWH}	CONV Pulse Width, HIGH	15			15			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
V_{RT}	Most Positive Reference Input [1]	−1.1	0.0	0.1	−1.1	0.0	0.1	V
V_{RB}	Most Negative Reference Input [1]	−0.9	−2.0	−2.1	−0.9	−2.0	−2.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	1.0	2.0	2.2	1.0	2.0	2.2	V
V_{IN}	Input Voltage	V_{RT}		V_{RB}	V_{RT}		V_{RB}	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Note:

1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = MAX, Static[1]		30		35	mA
I_{EE}	Negative Supply Current	V_{EE} = MAX, Static[1]					
		T_A = 0°C to 70°C		-400			mA
		T_A = 70°C		-350			mA
		T_C = -55°C to 125°C				-470	mA
		T_C = 125°C				-320	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM		35		40	mA
R_{REF}	Total Reference Resistance		57		50		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}	5		5		kOhms
C_{IN}	Input Capacitance			250		250	pF
I_{CB}	Input Constant Bias Current	V_{EE} = MAX		400		500	μA
I_{SB}	Input Clock Synchronous Bias			200		200	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.5V		-2.0		-2.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V		75		75	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH		2.4		2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, Output HIGH, one pin to ground, one second duration.		-25		-25	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:

1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{CC} = MIN, V_{EE} = MIN	20		20		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = MIN, V_{EE} = MIN	0	10	0	10	ns
t_D	Output Delay Time	V_{CC} = MIN, V_{EE} = MIN, Load 1		40		45	ns
t_{HO}	Output Hold Time	V_{CC} = MIN, V_{EE} = MIN, Load 1	10		10		ns

System performance characteristics within specified operating conditions

Parameter			Test Conditions	Temperature Range				Units
				Standard		Extended		
				Min	Max	Min	Max	
E_{LI}	Linearity Error	Integral, Independent	V_{RT}, V_{RB} = NOM		0.3		0.3	%
E_{LD}	Linearity Error	Differential	V_{RT}, V_{RB}		0.3		0.3	%
Q	Code Size		V_{RT}, V_{RB} = NOM	15	185	15	185	% Nominal
E_{OT}	Offset Error	Top	V_{IN} = V_{RT}		35		45	mV
E_{OB}	Offset Error	Bottom	V_{IN} = V_{RB}		−22		−24	mV
T_{CO}	Offset Error	Temperature Coefficient			±50		±50	μV/°C
BW	Bandwidth, Full Power Input			7		5		MHz
t_{TR}	Transient Response, Full Scale				20		20	ns
SNR	Signal-to-Noise Ratio		10MHz Bandwidth 20MSPS Conversion Rate					
		Peak Signal/RMS Noise	1.248MHz Input	53		52		dB
			2.438MHz Input	50		49		dB
		RMS Signal/RMS Noise	1.248MHz Input	44		43		dB
			2.438MHz Input	41		40		dB
NPR	Noise Power Ratio		DC to 8MHz White Noise Bandwidth 4 Sigma Loading 1.248MHz Slot 20MSPS Conversion Rate	36.5		36.5		dB
E_{AP}	Aperture Error				60		60	ps
DP	Differential Phase		NTSC @ 4x Color Subcarrier		1.0		1.0	Degree
DG	Differential Gain		NTSC @ 4x Color Subcarrier		1.7		1.7	%

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Output Coding (Input range from 0.000 to −2.000V)

Input Voltage (−7.84 mV/Step)	Binary		Offset Two's Complement	
	True	Inverted	True	Inverted
	NMINV = 1	0	0	1
	NLINV = 1	0	1	0
0.000	00000000	11111111	10000000	01111111
•	•	•	•	•
•	•	•	•	•
−0.0078	00000001	11111110	10000001	01111110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−0.9960	01111111	10000000	11111111	00000000
−1.0039	10000000	01111111	00000000	11111111
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−1.9921	11111110	00000001	01111110	10000001
•	•	•	•	•
•	•	•	•	•
−2.000	11111111	00000000	01111111	10000000

Calibration

To calibrate the TDC1007, the top of the reference resistor chain, R_T, is connected to analog ground. The reference voltage is then set up by adjusting the bottom of the resistor chain to −2.0V. When this technique is used, offset errors are generated by the inherent parasitic resistance between the package pin and the actual resistor chain on the A/D. These parasitic resistors are shown as R_1 and R_2 in the Functional Block Diagram. The offset voltage error is the result of the resistor chain current flowing through the parasitic resistance. These errors can be compensated for by applying an equal offset to the analog input signal or by adjusting the voltages on R_T and R_B.

The effect of the offset error at the bottom of the resistor chain manifests itself in the form of a slight gain error which can be compensated for by varying the voltage applied to R_B. This voltage will necessarily be more negative than the desired reference level of −2.0V. The actual operating range of the A/D converter will be:

$$(V_{AGND} - (I_{REF} \times R1)) \text{ to } (V_{RB} + (I_{REF} \times R2)).$$

However, if both ends of the resistor chain are driven by transistor-buffered operational amplifiers, the voltages on R_T and R_B could then be adjusted to remove the effect of the parasitic resistances and therefore eliminate the need to apply a compensating offset voltage to the analog input signal. Here the operating range of the A/D will be:

$$(V_{RT} - (I_{REF} \times R1)) \text{ to } (V_{RB} + (I_{REF} \times R2)).$$

Since both V_{RT} and V_{RB} are adjustable, the offset voltage error effect can be cancelled and the A/D operated with gain and offset errors removed.

The TDC1007 provides access to the mid-point of the reference resistor chain, R_M. This point can be sensed by external circuitry for temperature compensation or gain tracking functions in the system. It can also be driven in the manner shown in Figure 6 for fine linearity correction.

Typical Application

Figure 5 shows a typical interface circuit for a TDC1007, an input buffer amplifier, and the reference voltage source. The reference voltage is supplied by an inverting amplifier that has been buffered with a PNP transistor. The transistor sinks the current flowing through the reference resistor chain and keeps the driving impedance at the bottom end of the resistor chain low. The gain of the overall circuit is adjusted by varying the input voltage to the operational amplifier.

The input amplifier is a bipolar wideband operational amplifier followed by an NPN transistor buffer. The transistor drives the input capacitance of the A/D converter and keeps the overall circuit frequency stable. The offset error is compensated by varying the current into the summing junction of the op-amp. Note that all five V_{IN} points are connected together and the buffer amplifier feedback loop is closed at that point. The buffer amplifier has a gain of two, raising the 1V p-p video input signal to 2V p-p at the input to the A/D converter. The A/D converter operates with a 2V full-scale.

Figure 5. Typical Interface Circuit

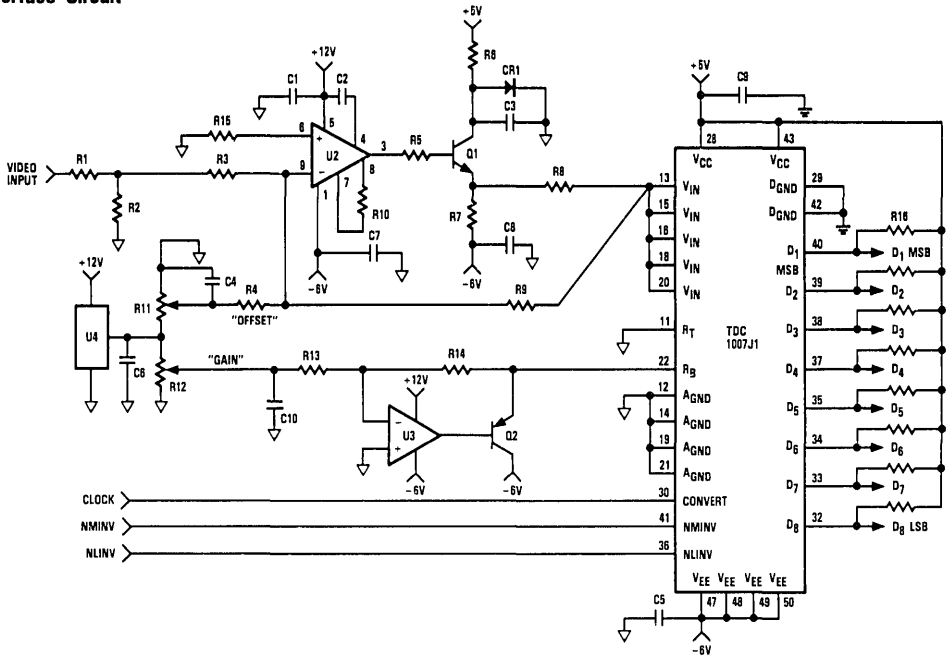
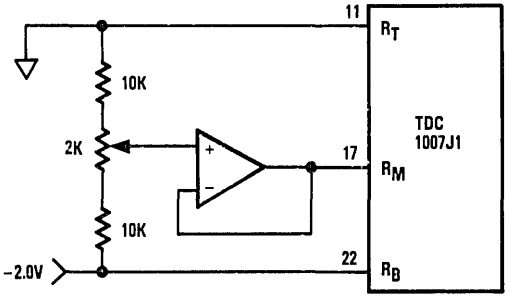


Figure 6. Method For Driving Mid-Point Of Resistor Chain



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Parts List

Resistors

R1	†	1/4W	
R2	†	1/4W	
R3	1K	1/4W	5%
R4	4.3K	1/4W	5%
R5	10	1/4W	5%
R6	56	1/2W	5%
R7	240	2W	5%
R8	6.8	1/2W	5%
R9	2K	1/2W	5%
R10	*	1/4W	5%
R11	2K	1/4W	10-turn
R12	2K	1/4W	10-turn
R13	1.3K	1/4W	5%
R14	2.2K	1/4W	5%
R15	680	1/4W	5%
R16	2.2K	SIP	5%

Capacitors

C1	0.1μF	50V
C2	*	50V
C3	0.1μF	50V
C4	0.1μF	50V
C5	0.1μF	50V
C6	1.0μF	15V
C7	0.1μF	50V
C8	0.1μF	50V
C9	0.1μF	50V
C10	0.1μF	50V

Integrated Circuits

U1	TDC1007J1
U2	Plessey SL541C
U3	μA741
U4	MC1403

Diodes

CR1	1N4001

Transistors

Q1	2N5836
Q2	2N2907

† Indicates input terminator/divider

* Indicates amplifier compensation

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1007C1F	EXT-T_C = -55°C to 125°C	Commercial	68 Contact Chip Carrier	1007C1F3
TDC1007C1A	EXT-T_C = -55°C to 125°C	High Reliability[1]	68 Contact Chip Carrier	1007C1A3
TDC1007J1C	STD-T_A = 0°C to 70°C	Commercial	64 Lead DIP	1007J1C3
TDC1007J1G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	64 Lead DIP	1007J1G3
TDC1007L1F	EXT-T_C = -55°C to 125°C	Commercial	68 Leaded Chip Carrier	1007L1F3
TDC1007L1A	EXT-T_C = -55°C to 125°C	High Reliability[1]	68 Leaded Chip Carrier	1007L1A3

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Note:

1. Per TRW document 70Z01757.

TDC1014

Monolithic Video A/D Converter
6-Bit, 25MSPS

The TRW TDC1014 is a 25 MegaSample Per Second (MSPS) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 12MHz into 6-bit digital words. A sample-and-hold circuit is not necessary. All digital inputs and outputs are TTL compatible.

The TDC1014 consists of 63 clocked latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

Note: TRW recommends the use of the TDC1046 for new designs.

Features

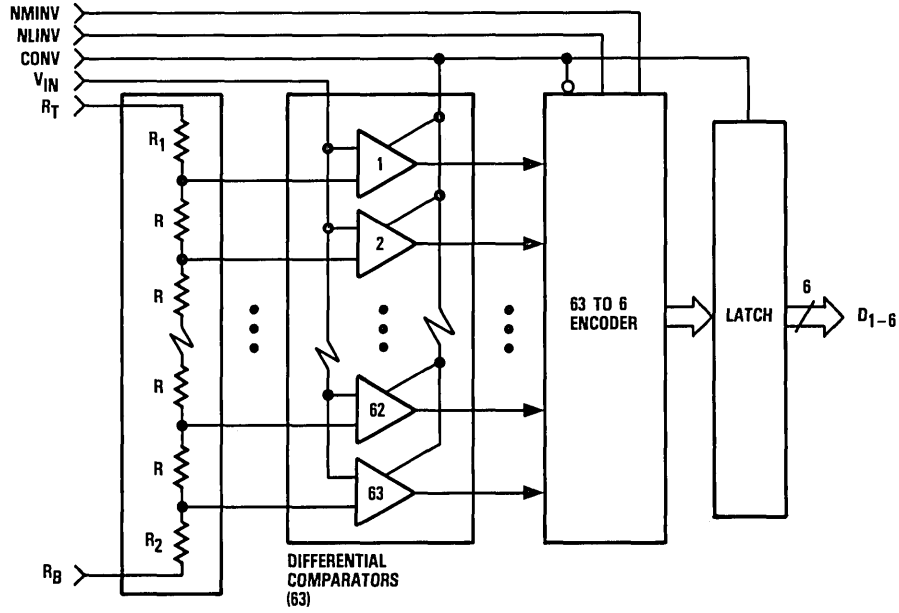
- 6-Bit Resolution
- 1/4 LSB Linearity
- Sample-And-Hold Circuit Not Required
- TTL Compatible
- 25MSPS Conversion Rate
- Selectable Output Format
- Available In 24 Lead DIP Or CERDIP
- Evaluation Boards - TDC1014E1C, TDC1014P1C

Applications

- Low-Cost Video Digitizing
- Medical Imaging
- Data Acquisition
- TV Special Effects
- Video Simulators
- Radar Data Conversion

D

Functional Block Diagram



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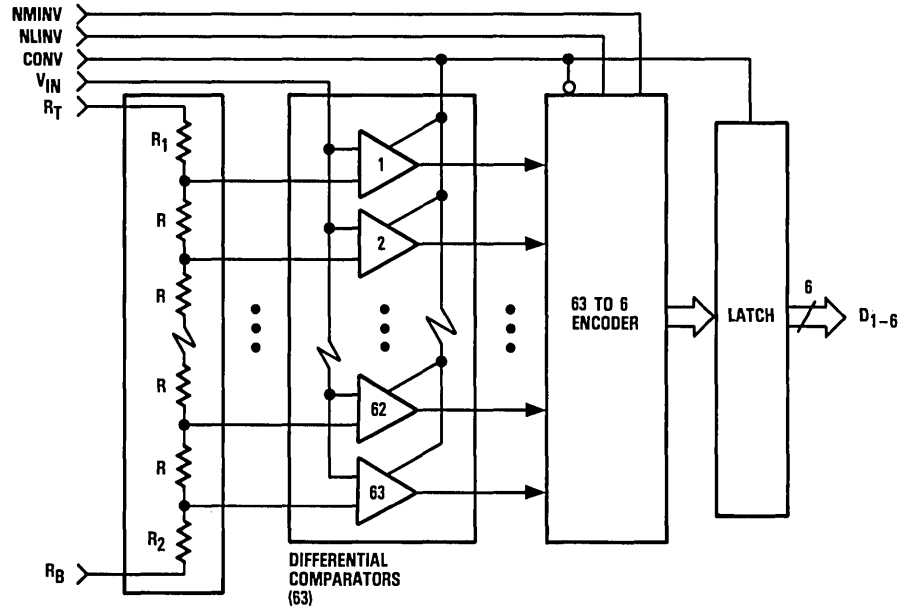
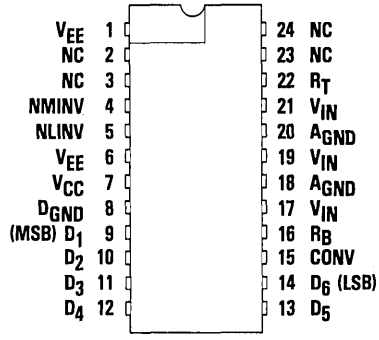
Functional Block Diagram



Pin Assignments



24 Lead DIP - J7 Package
24 Lead CERDIP - B7 Package

Functional Description

General Information

The TDC1014 has three functional sections: a comparator array, encoding logic, and output latches. The comparator array compares the input signal with 63 reference voltages to produce an N-of-63 code (sometimes referred to as a "thermometer" code, as all the comparators below the signal will be on, and all those above the signal will be off). The encoding logic converts the N-of-63 code into binary or offset two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV. The output latch holds the output constant between updates.

Power

The TDC1014 operates from two supply voltages, +5.0V and -6.0V. The return for I_{CC}, the current drawn from the +5.0V supply, is D_{GND}. The return for I_{EE}, the current drawn from the -6.0V supply, is A_{GND}. All power and ground pins must be connected.

Name	Function	Value	J7, B7 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pin 7
V_{EE}	Negative Supply Voltage	-6.0V	Pins 1, 6
D_{GND}	Digital Ground	0.0V	Pin 8
A_{GND}	Analog Ground	0.0V	Pins 18, 20

Reference

The TDC1014 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between +0.1V and -2.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain (V_{RT} - V_{RB}) must be between 0.8V and 1.2V. The current in the reference resistor chain can be supplied directly by a 741 type operational amplifier. The nominal voltages are, V_{RT} = 0.0V, V_{RB} = -1.0V. These voltages may be varied dynamically up to 12MHz. Due to variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically (as in an AGC circuit), a bypass capacitor is inappropriate and a low-impedance reference source is required.

Name	Function	Value	J7, B7 Package
R_T	Reference Resistor (Top)	0.0V	Pin 22
R_B	Reference Resistor (Bottom)	-1.0V	Pin 16

Control

Two function control pins, NMINV and NLINV, are provided. These controls are for DC (i.e. steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the Output Coding table. These pins are active LOW, as signified by the prefix "N" in the signal name. They may be tied to V_{CC} for a logic "1," and D_{GND} for a logic "0."

Name	Function	Value	J7, B7 Package
NMINV	Not Most Significant Bit INVert	TTL	Pin 4
NLINV	Not Least Significant Bit INVert	TTL	Pin 5

Convert

The TDC1014 requires a convert (CONV) signal. A sample is taken (the comparators are latched) approximately 10ns after a rising edge on the CONV pin. This time is t_{STO}, Sampling Time Offset. This delay varies by a few nanoseconds from part to part and as a function of temperature. The 63 to 6 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output latches on the next rising edge. The outputs require a minimum value of t_D (output delay) after a rising edge of the CONV signal. This permits the previous conversion result to be acquired by external circuitry at that rising edge, i.e. data for sample N is acquired by the external circuitry while the TDC1014 is taking input sample N + 2.

Name	Function	Value	J7, B7 Package
CONV	Convert	TTL	Pin 15

Analog Input

The TDC1014 uses strobed latching comparators which cause the input bias current to vary by approximately 5% with the convert (CONV) signal. This variation is "I_{SB}, clock synchronous bias current." The comparators also cause the input impedance, resistive and capacitive, to vary with the signal level, as comparator input transistors are cut-off or become active. As a result, for optimal performance, the source impedance of the device must have less than 25 Ohms impedance. The input signal will not damage the TDC1014 if it remains within the range of V_{EE} to +0.5V. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number between 0 and 63 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction. All three analog input pins must be connected together.

Name	Function	Value	J7, B7 Package
V_{IN}	Analog Signal Input	0V to -1V	Pins 17, 19, 21

Outputs

The outputs of the TDC1014 are TTL compatible, capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. To improve rise time of outputs, it is recommended that the 2.2 kOhm pull-up resistors to V_{CC} be connected to data outputs. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal.

Name	Function	Value	J7, B7 Package
D_1	MSB Output	TTL	Pin 9
D_2		TTL	Pin 10
D_3		TTL	Pin 11
D_4		TTL	Pin 12
D_5		TTL	Pin 13
D_6	LSB Output	TTL	Pin 14

No Connects

There are several pins labeled No Connect (NC), which have no connections to the chip. Connect these pins to A_{GND} for noise reduction.

Name	Function	Value	J7, B7 Package
NC	No Connection	A_{GND}	Pins 2, 3, 23, 24

Figure 1. Timing Diagram

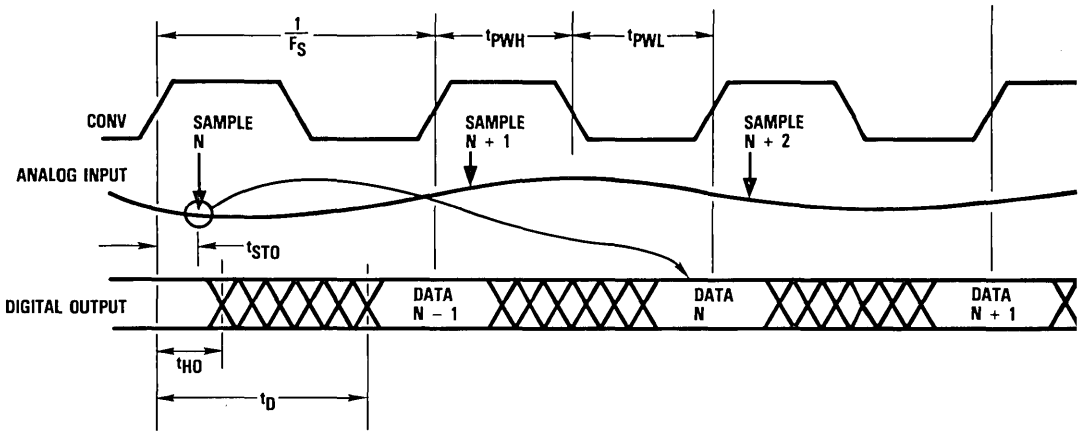
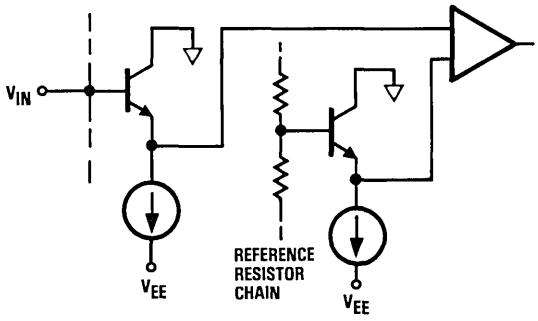
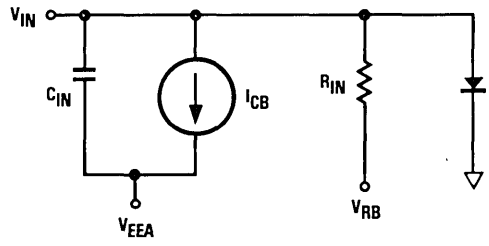


Figure 2. Simplified Analog Input Equivalent Circuit





C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

D

Figure 3. Digital Input Equivalent Circuit

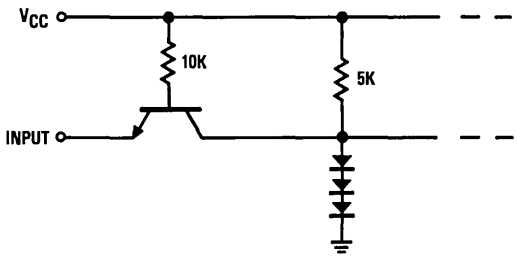
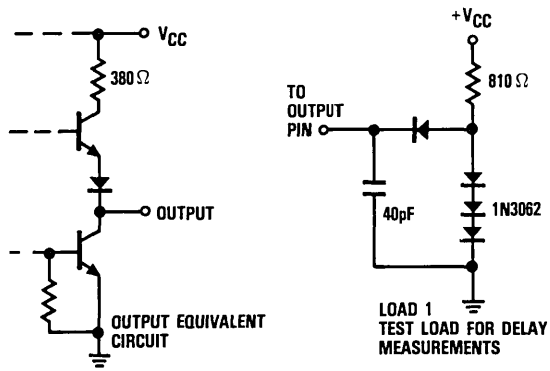


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND}) ..... 0.0 to +7.0V
V_{EE} (measured to A_{GND}) ..... 0.0 to −7.0V
A_{GND} (measured to D_{GND}) ..... −1.0 to +1.0V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND}) ..... −0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND}) ..... +0.5 to V_{EE}V
V_{RT} (measured to V_{RB}) ..... +2.2 to −2.2V

Output

Applied voltage (measured to D_{GND}) ..... −0.5 to 5.5V [2]
Applied current, externally forced ..... −1.0 to 6.0mA [3,4]
Short circuit duration (single output in high state to ground) ..... 1 sec

Temperature

Operating, ambient ..... −60 to +140°C
junction ..... +175°C
Lead, soldering (10 seconds) ..... +300°C
Storage ..... −65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage (Measured to D_{GND})	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Supply Voltage (Measured to A_{GND})	−5.75	−6.0	−6.25	−5.75	−6.0	−6.25	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0.0	0.1	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	19			19			ns
t_{PWH}	CONV Pulse Width, HIGH	15			15			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
V_{RT}	Most Positive Reference Input [1]	−1.1	0.0	0.1	−1.1	0.0	0.1	V
V_{RB}	Most Negative Reference Input [1]	−0.9	−1.0	−2.1	−0.9	−1.0	−2.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	0.8	1.0	1.2	0.8	1.0	1.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Note:

1. V_{RT} Must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = MAX, static[1]		30		30	mA
I_{EE}	Negative Supply Current	V_{EE} = MAX, static[1]					
		T_A = 0°C to 70°C		-150			mA
		T_A = 70°C		-110			mA
		T_C = -55°C to 125°C				-180	mA
		T_C = 125°C				-100	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM	2.0	8.0	2.0	8.0	mA
R_{REF}	Total Reference Resistance		125	500	125	500	Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}	20		20		kOhms
C_{IN}	Input Capacitance			75		75	pF
I_{CB}	Input Constant Bias Current	V_{EE} = MAX		150		150	μA
I_{SB}	Input Clock Synchronous Bias			20		20	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.5V		-2.0		-2.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V		75		75	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, Output HIGH, one pin to ground, one second duration.		25		25	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:

1. Worst case, all digital inputs and outputs LOW.

D

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{CC} = MIN, V_{EE} = MIN	25		25		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = MIN, V_{EE} = MIN	-2	10	-3	12	ns
t_D	Digital Output Delay	V_{CC} = MIN, V_{EE} = MIN Load 1		35		35	ns
t_{HO}	Output Hold Time	V_{CC} = MIN, V_{EE} = MIN Load 1	15		15		ns

System performance characteristics within specified operating conditions

Parameter			Test Conditions	Temperature Range				Units
				Standard		Extended		
				Min	Max	Min	Max	
E_{LI}	Linearity Error	Integral, Independent	V_{RT}, V_{RB} = NOM		0.4		0.4	%
E_{LD}	Linearity Error	Differential			0.4		0.4	%
Q	Code Size		V_{RT}, V_{RB} = NOM	50	150	50	150	% Nominal
E_{OT}	Offset Error	Top	V_{IN} = V_{RT}		30		30	mV
E_{OB}	Offset Error	Bottom	V_{IN} = V_{RB}		-24		-24	mV
T_{CO}	Offset Error	Temperature Coefficient			±100		±100	µV/°C
BW	Bandwidth, Full Power Input			12		12		MHz
t_{TR}	Transient Response, Full Scale				20		20	ns
SNR	Signal-to-Noise Ratio		10MHz Bandwidth, 25MSPS Conversion Rate					
		Peak Signal/RMS Noise	1.248MHz Input	44		44		dB
			2.438MHz Input	43		43		dB
		RMS Signal/RMS Noise	1.248MHz Input	35		35		dB
			2.438MHz Input	34		34		dB
NPR	Noise Power Ratio		DC to 8MHz White Noise Bandwidth 4 Sigma Loading 1.248MHz Slot 25MSPS Conversion Rate	26		26		dB
E_{AP}	Aperture Error				60		60	ps

Output Coding

Step	Range		Binary		Offset Two's Complement	
			True	Inverted	True	Inverted
	-1.0000V FS 15.8730 mV STEP	-1.0080V FS 16.0000 mV STEP	NMINV = 1 NLINV = 1	0 0	0 1	1 0
00	0.0000V	0.0000V	000000	111111	100000	011111
01	-0.0159V	-0.0160V	000001	111110	100001	011110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
31	-0.4921V	-0.4960V	011111	100000	111111	000000
32	-0.5079V	-0.5120V	100000	011111	000000	111111
33	-0.5238V	-0.5280V	100001	011110	000001	111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
62	-0.9841V	-0.9920V	111110	000001	011110	100001
63	-1.000V	-1.0080V	111111	000000	011111	100000

Note:

Voltages are code midpoints when calibrated by the procedure given in the Calibration section.

Calibration

To calibrate the TDC1014, adjust V_{RT} and V_{RB} to set the 1st and 63rd thresholds to the desired voltages. Note on the block diagram that R_1 is greater than R, ensuring calibration with a positive voltage on R_T. Assuming a 0V to −1V desired range, continuously strobe the converter with −0.0079V on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −0.9921V and adjust V_{RB} for toggling between codes 62 and 63. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with a buffer offset control. R_B is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in Figure 5.

Typical Interface Circuit

The Typical Interface Circuit in Figure 5 shows a simple buffer amplifier and voltage reference circuit that may be used with the TDC1014. U2 is a wide-band operational amplifier with a gain factor of −2. A small value resistor, R12, serves to help isolate the input capacitance of the A/D converter from the amplifier output and insure frequency stability. The pulse and frequency response of the buffer amplifier are optimized by variable capacitor C12.

The reference voltage for the TDC1014 is generated by amplifier U3 and PNP transistor Q1 which supplies the reference current. System gain is adjusted by varying R9 which controls the reference voltage level to the A/D converter.

Input voltage range and input impedance for the circuit are determined by resistors R1 and R2. Formulas for calculating values for these input resistors are:

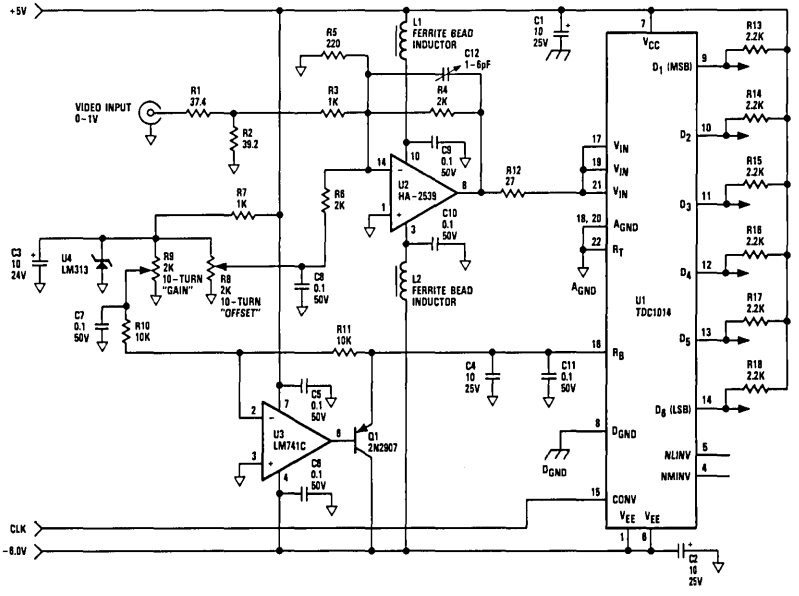
$$R1 = \frac{1}{\left(\frac{2VR}{Z_{IN}}\right) - \frac{1}{1000}}$$

and

$$R2 = Z_{IN} - \left(\frac{1000\ R1}{1000 + R1}\right)$$

where VR is the input voltage range of the circuit, Z_{IN} is the input impedance of the circuit, and the constant 1000 comes from the value of R3. As shown, the circuit is set up for 1 Volt p-p 75 Ohm video input.

Figure 5. Typical Interface Circuit



Ordering Information[1]

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1014J7C	STD-T_A = 0°C to 70°C	Commercial	24 Lead DIP	1014J7C
TDC1014J7G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	24 Lead DIP	1014J7G
TDC1014J7F	EXT-T_C = -55°C to 125°C	Commercial	24 Lead DIP	1014J7F
TDC1014J7A	EXT-T_C = -55°C to 125°C	High Reliability[2]	24 Lead DIP	1014J7A
TDC1014B7C	STD-T_A = 0°C to 70°C	Commercial	24 Lead CERDIP	1014B7C
TDC1014B7G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	24 Lead CERDIP	1014B7G

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Notes:

1. TRW recommends the use of the TDC1046 for new designs.
2. Per TRW document 70Z01757.

TDC1019
Preliminary Information

Monolithic Video A/D Converter
9-bit, 18MSPS

The TRW TDC1019 is an 18 MegaSample Per Second (MSPS) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 5MHz into 9-bit digital words. A sample-and-hold circuit is not required. All digital inputs and outputs are differential ECL.

The TDC1019 consists of 512 clocked latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The outputs can be connected to give either true or inverted outputs in binary or offset two's complement coding.

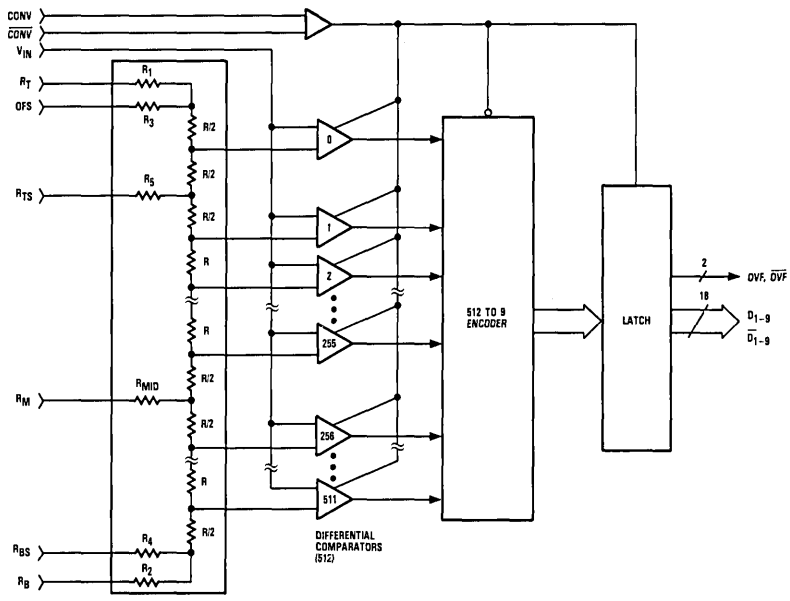
Features

- 9-Bit Resolution
- 18MSPS Conversion Rate, TDC1019-1
- 15MSPS Conversion Rate, TDC1019
- Overflow Flag
- Sample-And-Hold Circuit Not Required
- Differential Phase 1.0 Degree
- Differential Gain 2.0%
- Differential ECL Interface
- Selectable Output Format
- Single -5.2V Power Supply
- Available in 64 Lead DIP, 68 Contact Chip Carrier Or 68 Leaded Chip Carrier
- Evaluation Board - TDC1019E1C

Applications

- Video Data Conversion
- Radar Data Conversion
- Data Acquisition
- IR Processors

Functional Block Diagram



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Telex: 697-957
TWX: 910-335-1571

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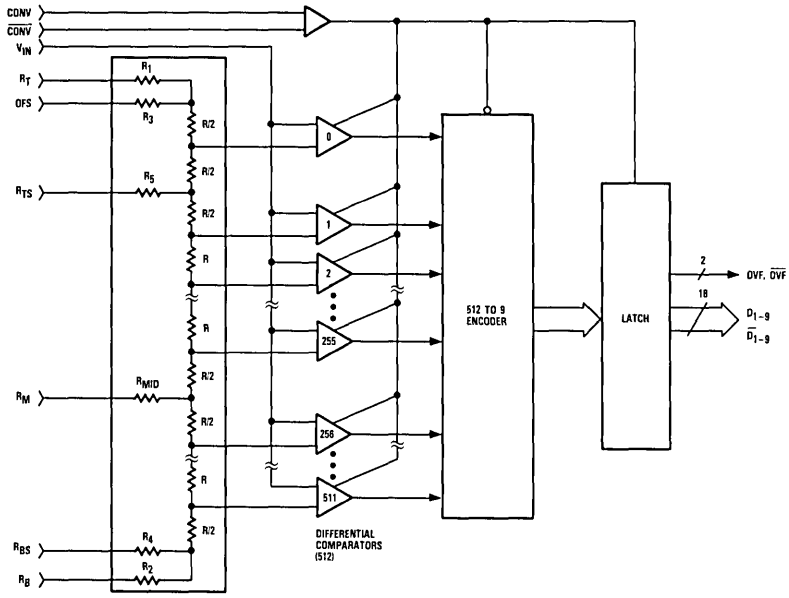
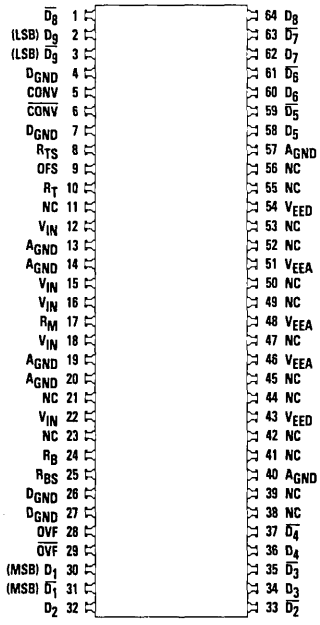
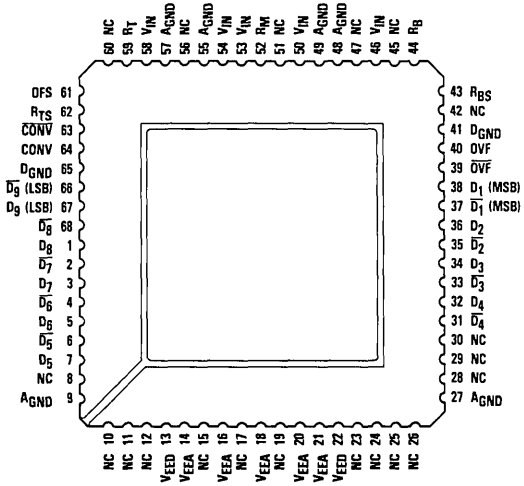
Functional Block Diagram



Pin Assignments



64 Lead DIP - J1 Package



68 Contact Or Leaded Chip Carrier - C1, L1 Package

Functional Description

General Information

The TDC1019 has three functional sections: a comparator array, encoding logic and output latches. The comparator array compares the input signal with 512 reference voltages to produce an N-of-512 code (sometimes referred to as a "thermometer" code, as all the comparators below the signal will be on, and all those above the signal will be off). The encoding logic converts the N-of-512 code into binary data. The output latch holds the output constant between updates.

Power

The TDC1019 operates from separate analog and digital power supplies, V_{EEA} and V_{EED}, respectively. Since the required voltage for both V_{EEA} and V_{EED} is -5.2V, they may ultimately be connected to the same power source, but separate decoupling for each supply is recommended. The return for the current drawn from V_{EED} and V_{EEA} is D_{GND} and A_{GND}, respectively. All power and ground pins must be connected.

Name	Function	Value	J1 Package	C1, L1 Package
V_{EEA}	Analog Supply Voltage	-5.2V	Pins 46, 48, 51	Pins 14, 16, 18, 20, 21
V_{EED}	Digital Supply Voltage	-5.2V	Pins 43, 54	Pins 13, 22
D_{GND}	Digital Ground	0.0V	Pins 4, 7, 26, 27	Pins 41, 65
A_{GND}	Analog Ground	0.0V	Pins 13, 14, 19, 20, 40, 57	Pins 9, 27, 48, 49, 55, 57

Reference

The TDC1019 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between +0.1V and -2.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain ($V_{RT}-V_{RB}$) must be between 1.8V and 2.2V. The nominal voltages are V_{RT} = 0.0V and V_{RB} = -2.0V. Parasitic resistances, R_1 and R_2, introduce offsets at the top and bottom of the reference resistor chain. Sense points R_{TS}, R_{BS} and OFS may be used to null out these offsets. Note that R_1 is greater than R, ensuring that a positive voltage is required at R_T. R_3, R_4 and R_5 are not designed to carry the reference current. OverFlow Sense (OFS) may be used to null out offsets at the overflow (most positive) comparator whenever the OVerFlow (OVF) flag is used. If the sense points are not used, they should be left open. The reference voltages may be varied dynamically up to 5MHz. If these inputs are exercised dynamically, a low-impedance reference source is required. If the reference is not varied, a bypass capacitor is recommended. A midpoint tap, R_M, allows the converter to be adjusted for optimum linearity. It can also be used to achieve a non-linear transfer function. This node should be driven from a low-impedance source. Noise introduced at this point, as well as the reference inputs (R_T, R_{TS}, R_B, R_{BS}, OFS), may result in encoding errors.

Name	Function	Value	J1 Package	C1, L1 Package
R_T	Reference Resistor (Top)	0.0V	Pin 10	Pin 59
R_{TS}	Reference Resistor (Top) Sense	0.0V	Pin 8	Pin 62
R_B	Reference Resistor (Bottom)	-2.0V	Pin 24	Pin 44
R_{BS}	Reference Resistor (Bottom) Sense	-2.0V	Pin 25	Pin 43
R_M	Reference Resistor (Midpoint)	-1.0V	Pin 17	Pin 52
OFS	OverFlow Sense	0.0V	Pin 9	Pin 61

D

Convert

The TDC1019 requires a differential CONVert (CONV and $\overline{CONV}$) signal. A sample is taken (the comparators are latched) approximately 10ns after the rising edge of the CONV signal. This time is t_{STO}, Sampling Time Offset. This delay varies by a few nanoseconds from part to part and as a function of temperature, but the short term uncertainty (jitter) in sampling offset time is less than 100 picoseconds. The 512 to 9 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output latches on the next rising edge. Data is held valid at the output register for at least t_{HO}, Output Hold Time, after the rising edge of CONV. New data becomes valid after a Digital Output Delay, t_D, time. In a synchronous system data for sample N is acquired by the external circuitry while the TDC1019 is taking input sample N + 2.

Name	Function	Value	J1 Package	C1, L1 Package
CONV	Convert	ECL	Pin 5	Pin 64
$\overline{CONV}$	Convert, Complement	ECL	Pin 6	Pin 63

Analog Input

The TDC1019 uses strobed latching comparators which cause the input impedance, resistive and capacitive, to vary with the signal level, as comparator input transistors are cut-off or become active. As a result, for optimal performance, the source impedance must be less than 25 Ohms. The input signal will not damage the TDC1019 if it remains within the range of V_{EEA} to +0.5V. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number between 0 and 511 inclusive. All five analog input pins must be connected.

Name	Function	Value	J1 Package	C1, L1 Package
V_{IN}	Analog Signal Input	0V to −2V	Pins 12, 15, 16, 18, 22	Pins 46, 50, 53, 54, 58

Outputs

The outputs of the TDC1019 are differential ECL levels. The recommended load is 500 Ohms to −2V. For optimum operation over the full temperature range, differential line receivers should be used. An OVerFlow (OVF) signal indicates that the analog input has exceeded the threshold of the most positive comparator. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONVert signal.

Name	Function	Value	J1 Package	C1, L1 Package
D_1	MSB Output	ECL	Pin 30	Pin 38
$\overline{D_1}$	MSB Output Complement	ECL	Pin 31	Pin 37
D_2		ECL	Pin 32	Pin 36
$\overline{D_2}$		ECL	Pin 33	Pin 35
D_3		ECL	Pin 34	Pin 34
$\overline{D_3}$		ECL	Pin 35	Pin 33
D_4		ECL	Pin 36	Pin 32
$\overline{D_4}$		ECL	Pin 37	Pin 31
D_5		ECL	Pin 58	Pin 7
$\overline{D_5}$		ECL	Pin 59	Pin 6
D_6		ECL	Pin 60	Pin 5
$\overline{D_6}$		ECL	Pin 61	Pin 4
D_7		ECL	Pin 62	Pin 3
$\overline{D_7}$		ECL	Pin 63	Pin 2
D_8		ECL	Pin 64	Pin 1
$\overline{D_8}$		ECL	Pin 1	Pin 68
D_9	LSB Output	ECL	Pin 2	Pin 67
$\overline{D_9}$	LSB Output Complement	ECL	Pin 3	Pin 66
OVF	Overflow Output	ECL	Pin 28	Pin 40
$\overline{OVF}$	Overflow Output Complement	ECL	Pin 29	Pin 39

No Connects

There are several pins labeled No Connect (NC). These pins should be left open.

Name	Function	Value	J1 Package	C1, L1 Package
NC	No Connect	Open	Pins 11, 21, 23, 38, 39, 41, 42, 44, 45, 47, 49, 50, 52, 53, 55, 56	Pins 8, 10, 11, 12, 15, 17, 19, 23, 24, 26, 28, 29, 30, 42, 45, 47, 51, 56, 60

Figure 1. Timing Diagram

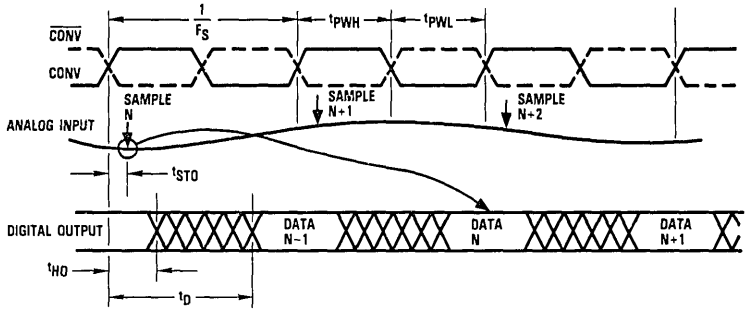
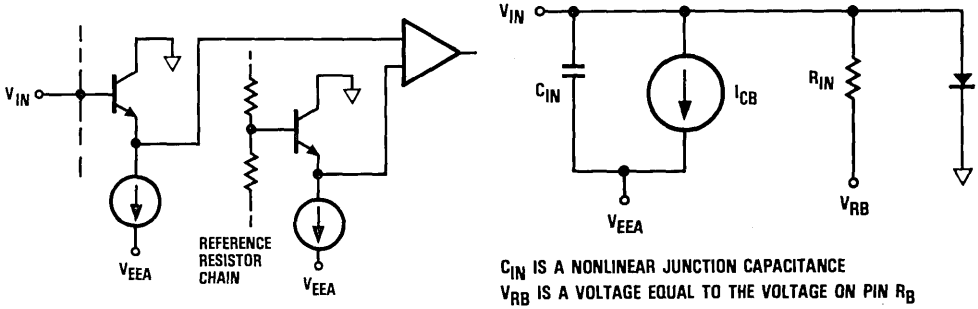


Figure 2. Simplified Analog Input Equivalent Circuit



C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

Figure 3. Digital Input Equivalent Circuit

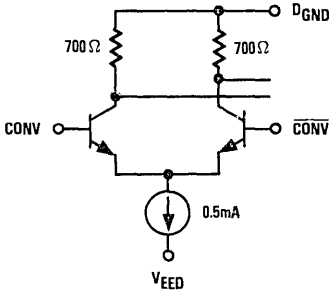
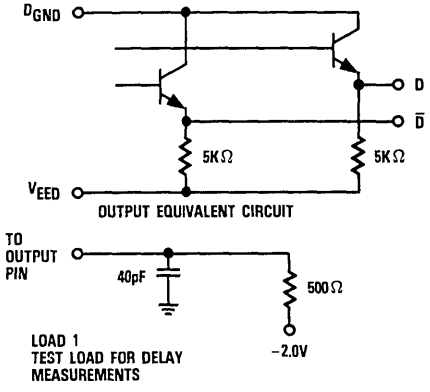


Figure 4. Output Circuits



D

Absolute maximum ratings (beyond which the device will be damaged)[1]

Supply Voltages

V_{EED} (measured to D_{GND})	+0.5 to −7.0V
V_{EEA} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	+1.0 to −1.0V
V_{EEA} (measured to V_{EED})	+0.5 to −0.5V

Input Voltage

CONV. $\overline{CONV}$ (measured to D_{GND})	+0.5 to V_{EE}V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EE}V
V_{RT} (measured to V_{RB})	+2.5 to −2.5V

Outputs

Short circuit duration (single output to GND)	Indefinite

Temperature

Operating, case	−60 to +140°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Note:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.

Operating conditions

Parameter			Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{EED}	Digital Supply Voltage (measured to D_{GND})		−4.9	−5.2	−5.5	V
V_{EEA}	Analog Supply Voltage (measured to A_{GND})		−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (measured to DGND)		−0.1	0.0	+0.1	V
$V_{EEA}-V_{EED}$	Supply Voltage Differential		−0.1	0.0	+0.1	V
t_{PWL}	CONV Pulse Width, LOW	Standard	25			ns
		−1 Version	22			ns
t_{PWH}	CONV Pulse Width, HIGH	Standard	32			ns
		−1 Version	28			ns
V_{IL}	Input Voltage, Logic LOW				−1.4	V
V_{IH}	Input Voltage, Logic HIGH		−1.0			V
V_{RT}	Most Positive Reference Input[1]		−0.1	0.0	+0.1	V
V_{RB}	Most Negative Reference Input[1]		−1.9	−2.0	−2.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential		1.8	2.0	2.2	V
V_{IN}	Input Voltage		V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air[2]		0		+70	°C

Notes:

1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.
2. 500 L.F.P.M. moving air required above 50°C.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
I_{EE}	Supply Current	V_{EED}, V_{EEA} = MAX			
		T_A = 0°C to 70°C		-850	mA
		T_A = 50°C		-725	mA
		T_A = 70°C (500 LFPM)		-700	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM	10	36	mA
R_{REF}	Total Reference Resistance		56	200	Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}	2.0		kOhms
C_{IN}	Input Capacitance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}		280	pF
I_{CB}	Input Constant Bias Current	V_{EEA} = MAX, V_{IN} = 0.0V		750	μA
I_I	Digital Input Current	V_{EED} = MAX, V_I = -0.7V		150	μA
V_{OL}	Output Voltage, Logic LOW	V_{EED} = NOM, I_{OL} = Test Load[1]		-1.6	V
V_{OH}	Output Voltage, Logic HIGH	V_{EED} = NOM, I_{OH} = Test Load[1]	-0.95		V
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		35	pF

Note:
1. Test Load = 500 Ohms to -2.0V.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
F_S	Maximum Conversion Rate	V_{EED}, V_{EEA} = MIN Standard	15		MSPS
		V_{EED}, V_{EEA} = MIN -1 Version	18		MSPS
t_{STO}	Sampling Time Offset	V_{EED}, V_{EEA} = MIN	0	15	ns
t_D	Output Delay	V_{EED}, V_{EEA} = MIN, Load[1]		35	ns
t_{HO}	Output Hold Time	V_{EED}, V_{EEA} = MIN, Load[1]	3		ns

Note:
1. Test load = 500 Ohms to -2.0V.

D

System performance characteristics within specified operating conditions

Parameter			Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
E_{LI}	Linearity Error	Integral, Independent	V_{RT}, V_{RB} = NOM		0.3	%
			V_{RT}, V_{RB} = NOM[1], t_{PWH} = 28ns		0.15	%
E_{LD}	Linearity Error	Differential	V_{RT}, V_{RB} = NOM		0.15	%
Q	Code Size		V_{RT}, V_{RB} = NOM	15	185	% Nominal
E_{OTS}	Offset Error	Top	V_{IN} = V_{RT}, R_{TS} Connected		±4	mV
E_{OT}	Offset Error	Top	V_{IN} = V_{RT}		+40	mV
E_{OBS}	Offset Error	Bottom	V_{IN} = V_{RB}, R_{BS} Connected		±4	mV
E_{OB}	Offset Error	Bottom	V_{IN} = V_{RB}		−40	mV
T_{CO}	Offset Error	Temperature Coefficient			20	µV/°C
t_{TR}	Transient Response, Full Scale				20	ns
BW	Bandwidth, Full Power Input			5		MHz
SNR	Signal-to-Noise Ratio		5MHz Bandwidth, 18MSPS Conversion Rate			
		Peak Signal/RMS Noise	1.25MHz Input	52		dB
			2.438MHz Input	49		dB
		RMS Signal/RMS Noise	1.25MHz Input	43		dB
			2.438MHz Input	40		dB
E_{AP}	Aperture Error				100	ps
DP		Differential Phase[1,2]	4 x NTSC Subcarrier		1.0	Degrees
DG		Differential Gain[1,2]	4 x NTSC Subcarrier		2.0	%

Notes:

1. Voltage at midpoint (R_M) adjusted.
2. In excess of quantization.

Output Coding

Step	Range		Binary		Offset Two's Complement	
			True	Inverted	True	Inverted
	−2000V FS 3.9139 mV Step	−2.0440V FS 4.000 mV Step		All Outputs Inverted	D_1 Inverted	D_2–D_9 Inverted
000	0.0000V	0.0000V	000000000	111111111	100000000	011111111
001	0.0039V	0.0040V	000000001	111111110	100000001	011111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
255	0.9980V	1.0200V	011111111	10000000	11111111	000000000
256	1.0020V	1.0240V	100000000	01111111	00000000	111111111
257	1.0059V	1.0280V	100000001	01111110	00000001	111111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
510	1.9961V	1.9980V	111111110	000000001	011111110	100000001
511	2.0000V	2.0200V	111111111	000000000	011111111	100000000

Notes:

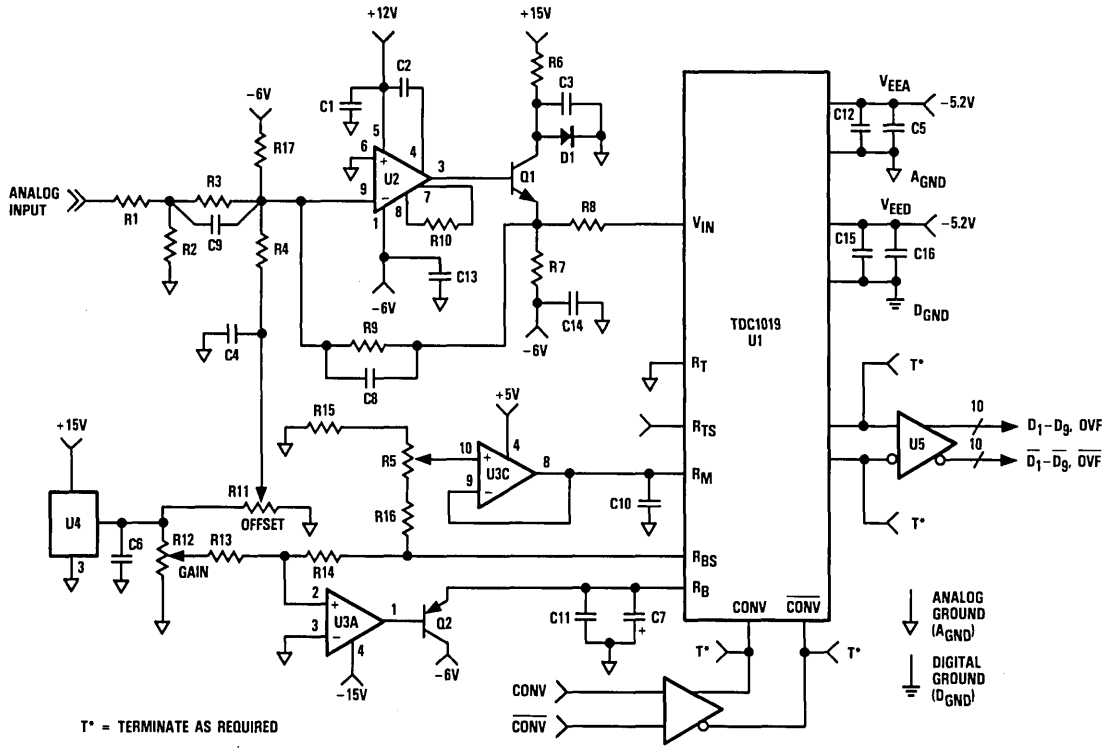
1. Any output may be inverted by interchanging connections to the true (D_N) and complement ($\overline{D_N}$) output pins.
2. Voltages are code midpoints when calibrated by the procedure given below.

Calibration

To calibrate the TDC1019, adjust V_{RT} and V_{RB} to set the 1st and 511th thresholds to the desired voltages. Note that R_1 is greater than R, ensuring calibration with a positive voltage on R_T. Assuming a 0V to −2V desired range, continuously strobe the converter with −0.00196V on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −1.9980V and adjust V_{RB} for toggling between codes 510 and 511. The Overflow flag is calibrated similarly to V_{RT} except that the converter input is set 1 LSB more positive than the top of the encoding range (−0.00196V in this example). Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with a buffer offset control. R_B is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in Figure 5.

D

Figure 5. Typical Interface Circuit



Parts List

Resistors

R1	.0Ω [1]		
R2	80.6Ω [1]	1/4W	2%
R3	1.0KΩ	1/4W	2%
R4	4.2KΩ	1/4W	2%
R5	2.0KΩ	1W	Multiturn Cermet Pot
R6	100.0Ω	3W	5%
R7	120.0Ω	3W	5%
R8	10.0Ω	1/4W	5%
R9	2.0KΩ	1/4W	2%
R10	(See Note 2)		
R11	2.0KΩ	1W	Multiturn Cermet Pot
R12	2.0KΩ	1W	Multiturn Cermet Pot
R13	20.0KΩ	1/4W	2%
R14	20.0KΩ	1/4W	2%
R15	2.0KΩ	1/4W	2%
R16	2.0KΩ	1/4W	2%
R17	75.0KΩ	1/4W	2%

Capacitors

C1	0.1μF	50V
C2	2.0μF	50V
C3	0.1μF	50V
C4	0.1μF	50V
C5	0.1μF	50V
C6	1.0μF	10V
C7	0.0μF	10V
C8	(See Note 2)	
C9	(See Note 2)	
C10	0.1μF	50V
C11	0.1μF	50V
C12	0.1μF	50V
C13	0.1μF	50V
C14	0.1μF	50V
C15	0.1μF	50V
C16	0.1μF	50V

Integrated Circuits

U1	TRW TDC1019
U2	Plessey SL541C
U3	MC4741
U4	MC1403
U5	MC10116

Transistors

Q1	2N5836
Q2	2N2907

Diodes

D1	1N4001

Notes:

1. Selected for desired input impedance and voltage range.
2. Selected for amplifier compensation.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1019J1C	STD-T_A = 0°C to 70°C	Commercial	64 Lead DIP	1019J1C
TDC1019J1C1	STD-T_A = 0°C to 70°C	Commercial	64 Lead DIP	1019J1C1
TDC1019J1G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	64 Lead DIP	1019J1G
TDC1019J1G1	STD-T_A = 0°C to 70°C	Commercial With Burn-In	64 Lead DIP	1019J1G1
TDC1019C1C	STD-T_A = 0°C to 70°C	Commercial	68 Contact Chip Carrier	1019C1C
TDC1019C1C1	STD-T_A = 0°C to 70°C	Commerical	68 Contact Chip Carrier	1019C1C1
TDC1019C1G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	68 Contact Chip Carrier	1019C1G
TDC1019C1G1	STD-T_A = 0°C to 70°C	Commercial With Burn-In	68 Contact Chip Carrier	1019C1G1
TDC1019L1C	STD-T_A = 0°C to 70°C	Commercial	68 Leaded Chip Carrier	1019L1C
TDC1019L1C1	STD-T_A = 0°C to 70°C	Commercial	68 Leaded Chip Carrier	1019L1C1
TDC1019L1G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	68 Leaded Chip Carrier	1019L1G
TDC1019L1G1	STD-T_A = 0°C to 70°C	Commercial With Burn-In	68 Leaded Chip Carrier	1019L1G1

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Preliminary Information describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact TRW for current information.

TDC1021

Monolithic A/D Converter
4-bit, 25MSPS

The TRW TDC1021 is a 25 MegaSample Per Second (MSPS) full-parallel (flash) analog-to-digital converter, capable of converting signals with full-power frequency components up to 10MHz into 4-bit digital words. A sample-and-hold circuit is not required. All digital inputs and outputs are TTL compatible.

The TDC1021 consists of 15 clocked latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs, in binary or offset two's complement coding.

Note: TRW recommends the use of the TDC1044 for new designs.

Features

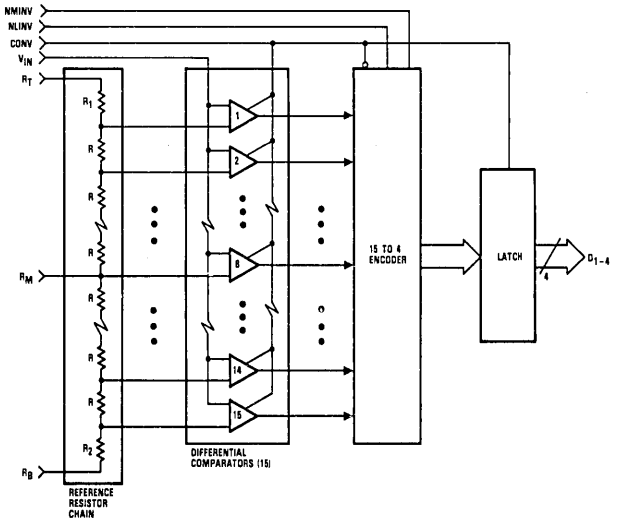
- 4-Bit Resolution
- ±1/4 LSB Linearity
- Sample-And-Hold Circuit Not Required
- TTL Compatible
- 25MSPS Conversion Rate
- Selectable Output Format
- Available In 16 Lead DIP
- Standard/Extended Temperature Range

Applications

- Video Special Effects
- Radar Data Conversion
- High-Speed Multiplexed Data Acquisition
- Medical Imaging
- Image Processing

D

Functional Block Diagram



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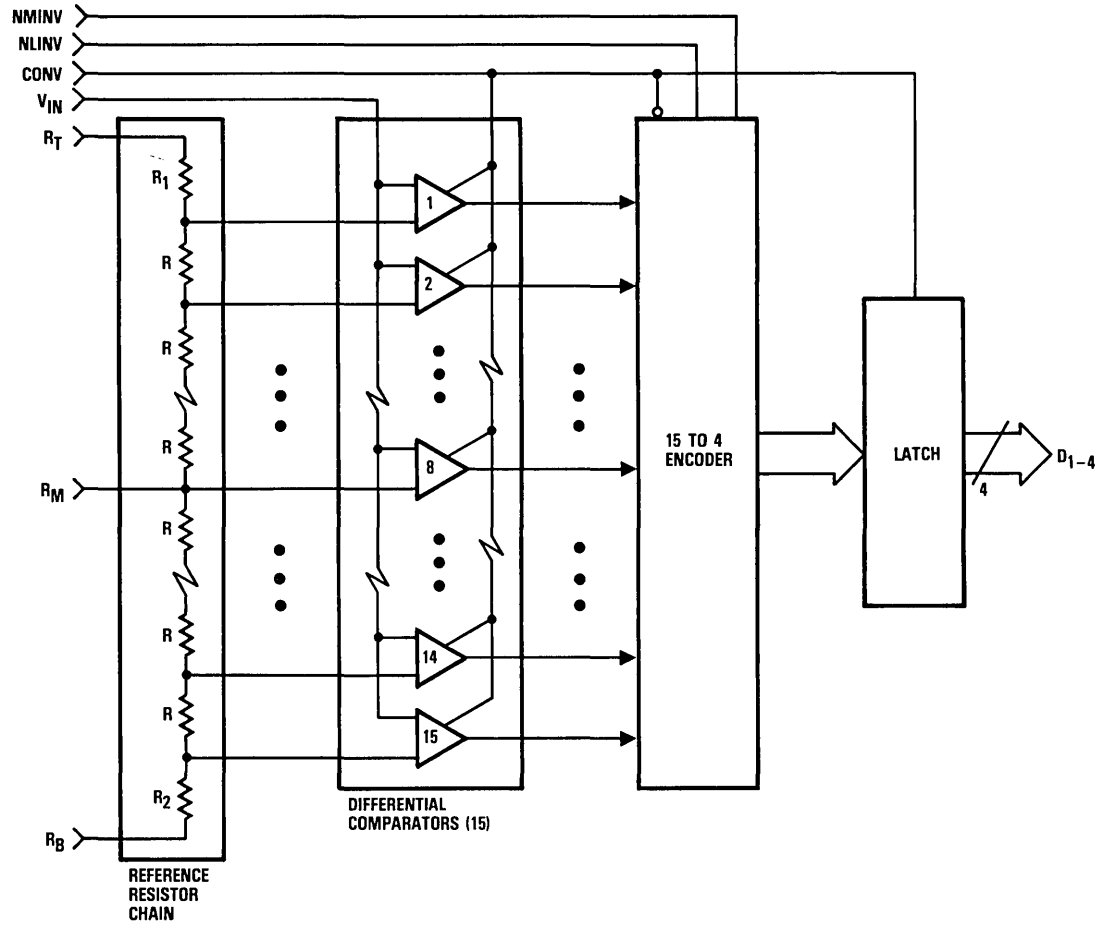
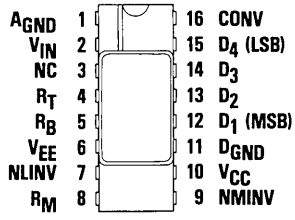
Functional Block Diagram



Pin Assignments



16 Lead DIP – J9 Package

Functional Description

General Information

The TDC1021 has three functional sections: a comparator array, encoding logic and output latches. The comparator array compares the input signal with 15 reference voltages to produce an N-of-15 code (sometimes referred to as a "thermometer" code, as all the comparators below the signal will be on, and all those above the signal will be off).

The encoding logic converts the N-of-15 code into binary or offset two's complement coding and can invert either output code. This coding function is selected by DC controls on pins NMINV and NLINV. The output latch holds the data on the output constant between updates.

Power

The TDC1021 operates from two supply voltages: +5.0V which is referenced to D_{GND}, and -6.0V which is referenced to A_{GND}. All power and ground pins must be connected.

Name	Function	Value	J9 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pin 10
V_{EE}	Negative Supply Voltage	-6.0V	Pin 6
D_{GND}	Digital Ground	0.0V	Pin 11
A_{GND}	Analog Ground	0.0V	Pin 1

Reference

The TDC1021 converts signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. V_{RB} (the voltage applied at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between +0.1V and -2.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain ($V_{RT}-V_{RB}$) must be between 0.4V and 1.3V. The current in the reference resistor chain can be supplied directly by an operational amplifier. These voltages may be varied dynamically up to 10MHz. Due to variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically (as in an AGC circuit), a bypass capacitor is inappropriate and a low-impedance reference source is required. A reference middle is also provided; this may be used as an input to adjust the mid-scale point in order to improve integral linearity. This point may also be used as a tap to supply a mid-scale voltage to offset the analog input. If V_{RM} is used as an output, it must be connected to a high input impedance device which has negligible offset current. Noise generated at this point will adversely affect the performance of the device.

Name	Function	Value	J9 Package
V_{RT}	Reference Resistor (Top)	0.04V	Pin 4
V_{RM}	Reference Resistor (Middle)	-0.5V	Pin 8
V_{RB}	Reference Resistor (Bottom)	-1.04V	Pin 5

D

Control

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either binary or offset two's complement, in either true or inverted sense, according to the Output Coding table. These pins are active LOW, as signified by the prefix "N" in the signal name. They may be tied to V_{CC} for a logic "1" and D_{GND} for a logic "0."

Name	Function	Value	J9 Package
NMINV	Not Most Significant Bit INVert	TTL	Pin 9
NLINV	Not Least Significant Bit INVert	TTL	Pin 7

Convert

The TDC1021 requires a convert (CONV) signal. A sample is taken (the comparators are latched) approximately 10ns after a rising edge on the CONV pin. This time is t_{STO}, Sampling Time Offset. This delay varies by a few nanoseconds from part to part and as a function of temperature. The 15 to 4 encoding is performed on the falling edge of the CONV signal. The coded result is then transferred to the output latches on the next rising edge. Data is held valid at the output register for at least t_{HO}, Output Hold Time, after the rising edge of CONV. This permits the previous conversion result to be acquired by external circuitry at that rising edge, i.e., data for sample N is acquired by the external circuitry while the TDC1021 is taking input sample N+2.

Name	Function	Value	J9 Package
CONV	Convert	TTL	Pin 16

Analog Input

The TDC1021 uses strobed latching comparators which cause the input bias current to vary by approximately 5% with the convert (CONV) signal. This variation is "I_{SB}, clock synchronous bias current." The comparators also cause the input impedance, resistive and capacitive, to vary with the signal level as comparator input transistors are cut-off or become active. As a result, for optimal performance, the source impedance must be less than 25 Ohms. The input signal will not damage the TDC1021 if it remains within the range of V_{EE} to +0.5V. If the input signal is between the the V_{RT} and V_{RB} references, the output will be a valid representation of the input. A signal outside this range will indicate either full-scale positive or full-scale negative, depending upon whether the signal is off-scale in the positive or negative direction.

Name	Function	Value	J9 Package
V_{IN}	Analog Signal Input	0V to -1V	Pin 2

Outputs

The outputs of the TDC1021 are TTL compatible, capable of driving four low-power Schottky TTL (54/74LS) unit loads or the equivalent. To improve rise time of outputs, it is recommended that 2.2 kOhm pull-up resistors to V_{CC} be connected to data outputs. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal.

Name	Function	Value	J9 Package
D_1	MSB Output	TTL	Pin 12
D_2		TTL	Pin 13
D_3		TTL	Pin 14
D_4	LSB Output	TTL	Pin 15

No Connects

Pin 3 of the TDC1021 is labeled No Connect (NC), and has no connection to the chip. Connect this pin to A_{GND} for noise reduction.

Name	Function	Value	J9 Package
NC	No Connect	A_{GND}	Pin 3

Figure 1. Timing Diagram

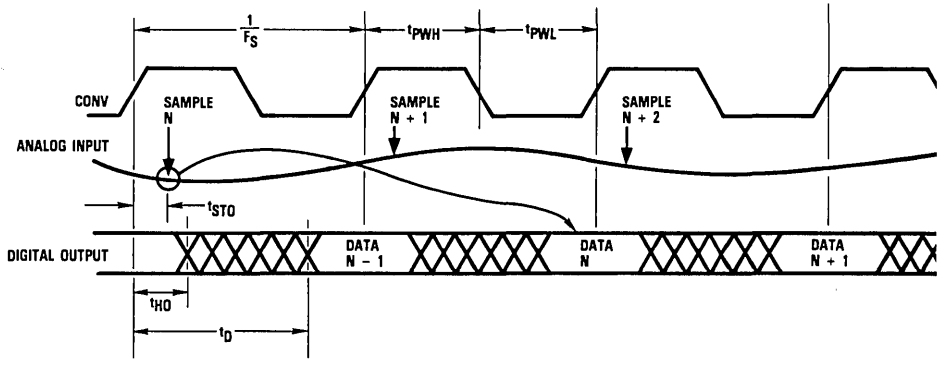
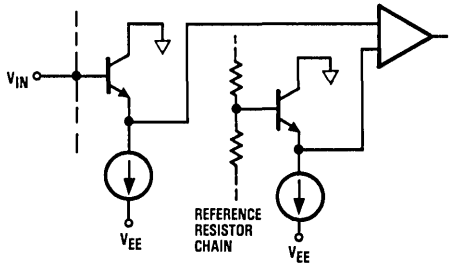
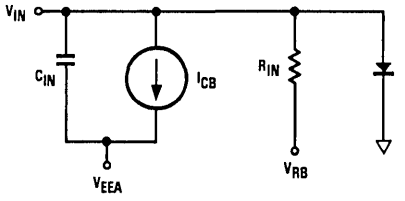


Figure 2. Simplified Analog Input Equivalent Circuit





C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

Figure 3. Digital Input Equivalent Circuit

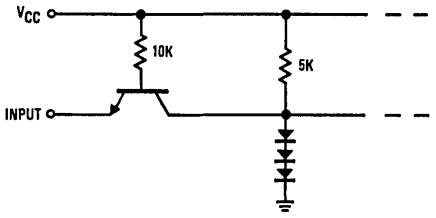
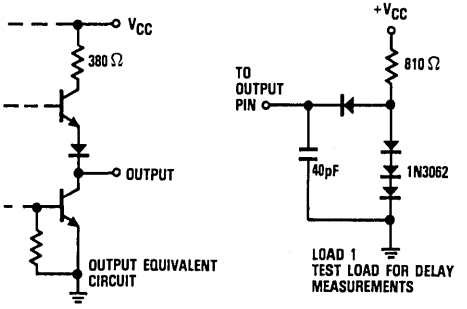


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	+1.0 to −1.0V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EE}V
V_{RT} (measured to V_{RB})	+2.2 to −2.2V

Output

Applied voltage (measured to D_{GND})	−0.5 to +7.0V [2]
Applied current, externally forced	−1.0 to +6.0 mA [3,4]
Short circuit duration (single output in high state to ground)	1 sec

Temperature

Operating, ambient	−60 to +150°C
junction	+175°C
Lead, soldering (10 sec.)	+300°C
Storage	−65 to +160°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage (Measured to D_{GND})	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Supply Voltage (Measured to A_{GND})	−5.75	−6.0	−6.25	−5.75	−6.0	−6.25	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0.0	0.1	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	19			19			ns
t_{PWH}	CONV Pulse Width, HIGH	15			15			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
V_{RT}	Most Positive Reference Input [1]	−1.9	0.0	0.1	−1.9	0.0	0.1	V
V_{RB}	Most Negative Reference Input [1]	−2.1	−1.0	−0.1	−2.1	−0.1	−0.1	V
V_{RT}−V_{RB}	Voltage Reference Differential	0.2	1.0	2.0	0.2	1.0	2.0	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Note:

1. V_{RT} must be more positive than V_{RB} and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = MAX, static[1]		35		35	mA
I_{EE}	Negative Supply Current	V_{EE} = MAX, static[1]		-60		-60	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM		4.0		4.0	mA
R_{REF}	Total Reference Resistance		250		250		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}	60		60		kOhms
C_{IN}	Input Capacitance			25		25	pF
I_{CB}	Input Constant Bias Current	V_{EE} = MAX		20		30	μA
I_{SB}	Input Clock Synchronous Bias			5		5	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.5V		-2.0		-2.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V		75		75	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, Output HIGH, one pin to ground, one second duration		-25		-25	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:

1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{CC} = MIN, V_{EE} = MIN	25		25		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = MIN, V_{EE} = MIN		10		15	ns
t_D	Output Delay	V_{CC} = MIN, V_{EE} = MIN Load 1		35		35	ns
t_{HO}	Output Hold Time	V_{CC} = MIN, V_{EE} = MIN Load 1	5		5		ns

D

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB} = NOM		1.6		1.6	%
E_{LD}	Linearity Error Differential			1.6		1.6	%
Q	Code Size	V_{RT}, V_{RB} = NOM	50	150	50	150	% Nominal
E_{OT}	Offset Error Top	V_{IN} = V_{RT}		50		50	mV
E_{OB}	Offset Error Bottom	V_{IN} = V_{RB}		50		50	mV
T_{CO}	Offset Error Temperature Coefficient			±100		±100	μV/°C
BW	Bandwidth, Full Power Input		10		10		MHz
t_{TR}	Transient Response, Full Scale			20		20	ns
E_{AP}	Aperture Error			50		50	ps

Output Coding

Step	Range		Binary		Offset Two's Complement	
			True	Inverted	True	Inverted
	−1.0000V FS 66.667 mV STEP	−0.960V FS 64.000 mV STEP	NMINV = 1 NLINV = 1	0 0	0 1	1 0
00	0.000V	0.000V	0000	1111	1000	0111
01	−0.067V	−0.064V	0001	1110	1001	0110
02	−0.133V	−0.128V	0010	1101	1010	0101
03	−0.200V	−0.192V	0011	1100	1011	0100
04	−0.267V	−0.256V	0100	1011	1100	0011
05	−0.333V	−0.320V	0101	1010	1101	0010
06	−0.400V	−0.384V	0110	1001	1110	0001
07	−0.467V	−0.448V	0111	1000	1111	0000
08	−0.533V	−0.512V	1000	0111	0000	1111
09	−0.600V	−0.576V	1001	0110	0001	1110
10	−0.667V	−0.640V	1010	0101	0010	1101
11	−0.733V	−0.704V	1011	0100	0011	1100
12	−0.800V	−0.768V	1100	0011	0100	1011
13	−0.867V	−0.832V	1101	0010	0101	1010
14	−0.933V	−0.896V	1110	0001	0110	1001
15	−1.000V	−0.960V	1111	0000	0111	1000

NMINV and NLINV are to be considered DC controls. They may be tied to V_{CC} for a logical "1" and tied to digital ground for a logical "0."

Calibration

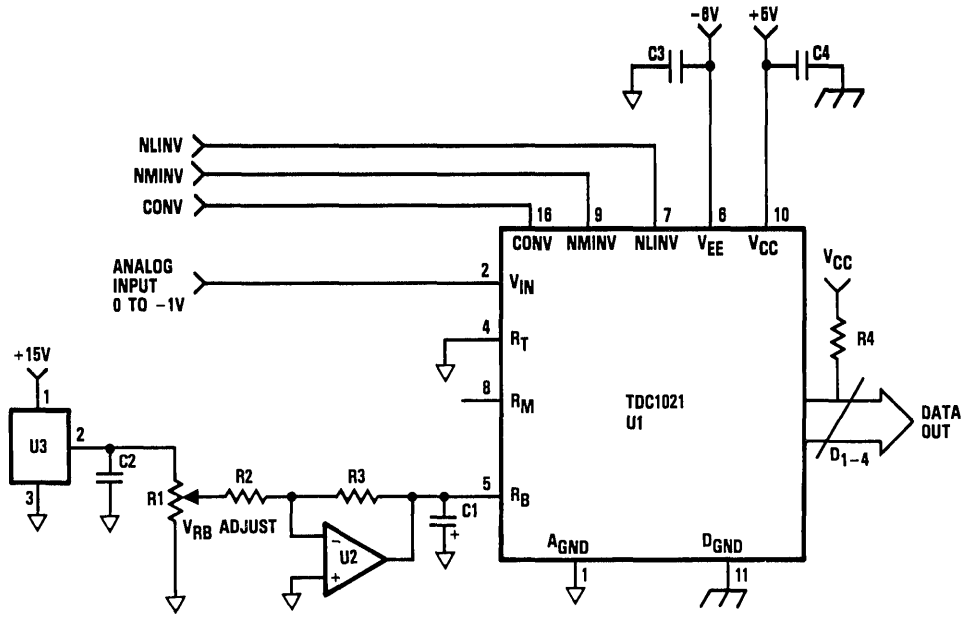
To calibrate the TDC1021, adjust V_{RT} and V_{RB} to set the 1st and 15th thresholds to the desired voltages. Assuming a 0V to −1.0V desired range, continuously strobe the converter with −0.0335V on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −0.9665V and adjust V_{RB} for toggling between codes 14 and 15. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with an analog input buffer offset control. R_B is a convenient point for gain adjust that is not in the analog signal path.

Typical Interface Circuit

Figure 5 shows a typical interface circuit. In this circuit the input has the range of 0.067V to −0.933V. The range is the difference between the voltages at which the transition from code 0 to code 1 occurs and the transition from code 14 to 15 occurs, +1 LSB. This extra LSB is produced when the analog to digital converter is calibrated with the transition from the 0 code to the 1st code occurring 1/2 LSB away from ground, and the transition from the 14th to 15th codes occurring 1/2 LSB away from full-scale. If a range from 0.000V to 1.000V is required, then V_{RT} must be adjusted (see calibration) and another buffer circuit added.

The TDC1021 does not require a buffer to drive the analog input, however, a buffer circuit may be used to provide signal conditioning such as filtering or gain/offset.

Figure 5. Typical Interface Circuit



Parts List

Resistors

R1	2.0KΩ	1/4W	Multiturn Cermet Pot
R2	21.5KΩ	1/4W	2%
R3	21.5KΩ	1/4W	2%
R4	2.2KΩ	1/4W	5%

Capacitors

C1	10 μF	10V
C2	1 μF	10V
C3	0.1 μF	50V
C4	0.1 μF	50V

Integrated Circuits

U1	TRW TDC1021
U2	741 Op-Amp
U3	Motorola MC1403U

Ordering Information[1]

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1021J9C	STD-T_A = 0°C to 70°C	Commercial	16 Lead DIP	1021J9C
TDC1021J9G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	16 Lead DIP	1021J9G
TDC1021J9F	EXT-T_C = -55°C to 125°C	Commercial	16 Lead DIP	1021J9F
TDC1021J9A	EXT-T_C = -55°C to 125°C	High Reliability[2]	16 Lead DIP	1021J9A

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Notes:

1. TRW recommends the use of the TDC1044 for new designs.
2. Per TRW document 70Z01757.

TDC1025
Preliminary Information

Monolithic A/D Converter
8-bit, 50MSPS

The TRW TDC1025 is a 50 MegaSample Per Second (MSPS) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 12MHz into 8-bit digital words. A sample-and-hold circuit is not necessary. All digital inputs and outputs are ECL compatible.

The TDC1025 consists of 255 latching comparators, combining logic, and an output register. A differential ECL convert signal controls the conversion operation. The digital outputs will interface with differential or single-ended ECL. The device requires a single -5.2V power supply.

Features

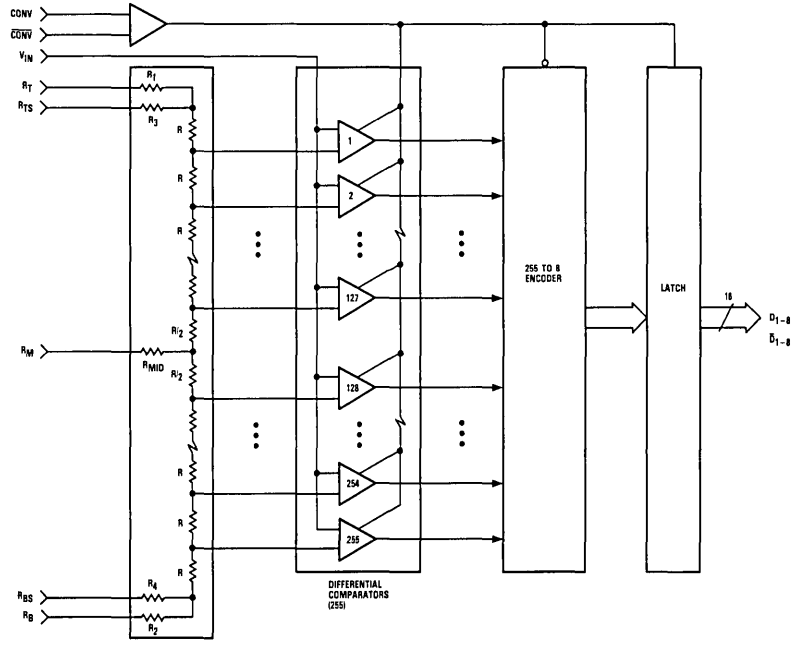
- 8-Bit Resolution
- 50MSPS Conversion Rate
- Sample-And-Hold Circuit Not Required
- Differential Or Single-Ended ECL Compatible
- Single -5.2V Power Supply
- Available In 68 Contact Or Leaded Chip Carrier
- Evaluation Board - TDC1025E1C

Applications

- Medical Electronics
- Fluid Flow Analysis
- Seismic Analysis
- Radar/Sonar
- Transient Analysis
- High-Speed Image Processing

D

Functional Block Diagram



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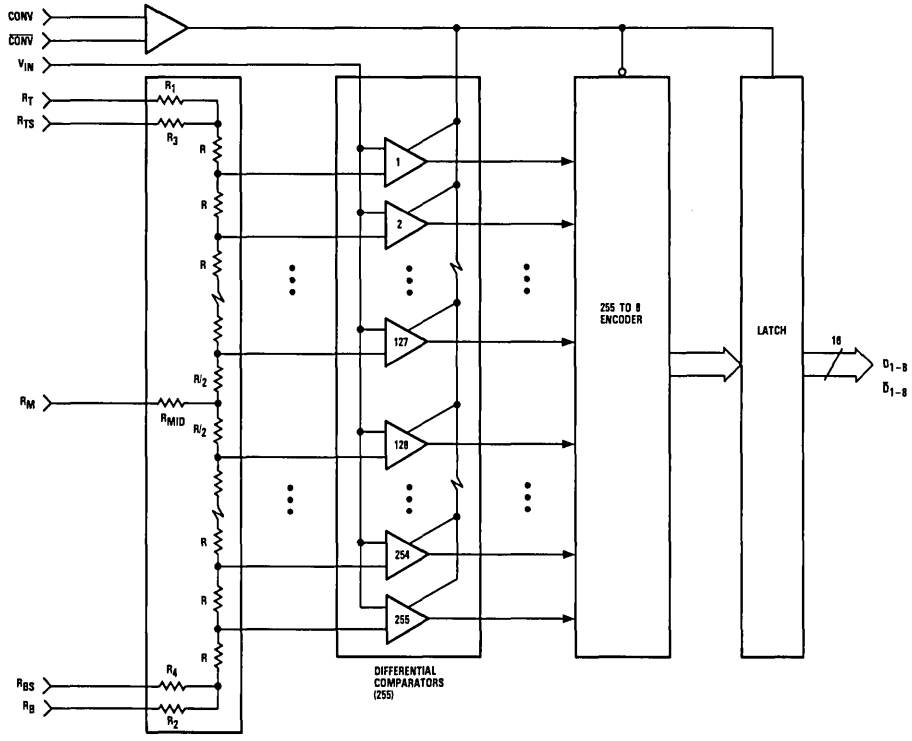
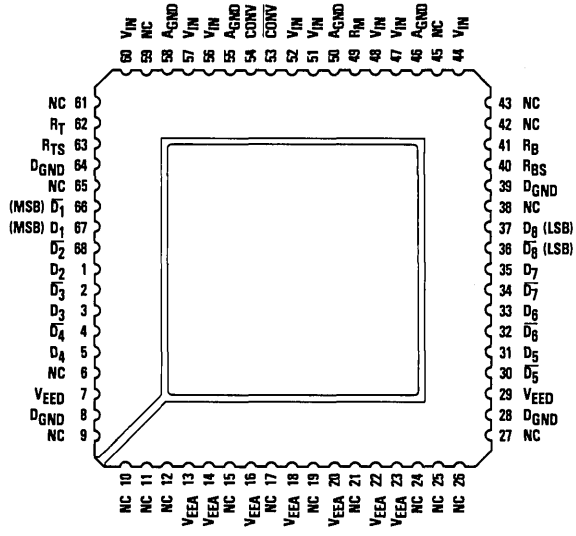
Functional Block Diagram



Pin Assignments



68 Contact Or Leaded Chip Carrier – C1, L1 Package

Functional Description

General Information

The TDC1025 has three functional sections: a comparator array, encoding logic, and output latches. The comparator array compares the input signal with 255 reference voltages to produce an N-of-255 code (sometimes referred to as a "thermometer" code, as all the comparators below the signal will be on, and all those above the signal will be off). The encoding logic converts the N-of-255 code into binary format. The output latch holds the output constant between updates.

Power

The TDC1025 operates from a single -5.2V power supply. The separate analog and digital power pins, V_{EEA} and V_{EED}, both require -5.2V, and may be connected to the same power supply. However, separate decoupling of the analog and digital power pins is recommended (refer to Figure 5 for a typical decoupling circuit). The return for I_{EED}, the current drawn from the V_{EED} supply, is D_{GND}. The return for I_{EEA}, the current drawn from the V_{EEA} supply, is A_{GND}. The analog and digital ground planes should be separated to minimize ground noise and prevent ground loops, and connected back at the power supply. All power and ground pins must be connected.

Name	Function	Value	C1, L1 Package
V_{EED}	Digital Supply Voltage	-5.2V	Pins 7, 29
V_{EEA}	Analog Supply Voltage	-5.2V	Pins 13, 14, 16, 18, 20, 22, 23
D_{GND}	Digital Ground	0.0V	Pins 8, 28, 39, 64
A_{GND}	Analog Ground	0.0V	Pins 46, 50, 55, 58

Reference

The TDC1025 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between +0.1V and -2.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain ($V_{RT}-V_{RB}$) must be between 1.8V and 2.2V. The nominal voltages are V_{RT} = 0.0V, V_{RB} = -2.0V.

Two sense points, R_{TS} and R_{BS}, may be used to minimize the offset errors and temperature sensitivity. With sensing, resistors R_1 and R_2 (as shown in the Functional Block Diagram) are contained within the feedback loop, and no longer contribute to the offset error. The remaining offset errors, E_{OTS} and E_{OBS}, can be eliminated by the calibration method discussed under Calibration. The temperature sensitivity of this remaining offset error is specified by t_{COS}, Temperature Coefficient, Sensed. The sense resistors, R_3 and R_4 (as shown in the Functional Block Diagram) are approximately 1 kOhm. These resistors are not designed to carry the total reference current, and should not be used as reference inputs. If the sensed points are not used, these pins should be left open. The circuit in Figure 5 shows a typical sensing configuration.

A midpoint tap, R_M, allows the converter to be adjusted for optimum linearity, although adjustment is not necessary to meet the linearity specification. It can also be used to achieve a non-linear transfer function. The circuit shown in Figure 7 will provide approximately 1/2 LSB adjustment of the linearity midpoint. The characteristic impedance at this node is approximately 75 Ohms, and should be driven from a low-impedance source. Note that any load applied to this node will affect linearity. Noise introduced at this point, as well as the reference inputs and sense points may degrade the quantization process, resulting in encoding errors.

Due to the variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically, (as in an Automatic Gain Control circuit), a low-impedance reference source is required. The reference voltages may be varied dynamically at rates up to 10MHz.

D

Reference (Cont.)

Name	Function	Value	C1, L1 Package
R_T	Reference Resistor (Top)	0.0V	Pin 62
R_{TS}	Reference Resistor Sense (Top)		Pin 63
R_M	Reference Resistor (Middle)	-1.0V	Pin 49
R_B	Reference Resistor (Bottom)	-2.0V	Pin 41
R_{BS}	Reference Resistor Sense (Bottom)		Pin 40

Convert

The TDC1025 requires a differential ECL Convert ($\overline{CONV}$) signal. Both convert inputs must be connected, with CONV being the complement of CONV. A sample is taken (the comparators are latched) within 10ns after the rising edge on the CONV pin. This time is t_{STO}, Sampling Time Offset. This delay may vary from part to part and as a function of temperature, but the short-term uncertainty (jitter) in sampling time offset is less than 50 picoseconds. The 255 to 8 encoding is performed on the falling edge of the CONV signal. The coded output is transferred to the output latches on the next rising edge. Data is held valid at the output register for at least t_{HO}, Output Hold Time, after the rising edge of CONV. New data becomes valid after a Digital Output Delay, t_D. This permits the previous conversion result to be acquired by external circuitry on that rising edge, i.e. data for sample N is acquired by the external circuitry while the TDC1025 is taking input sample N + 2. Note that there are minimum pulse width (t_{PWL} and t_{PWH}) requirements on the waveshape of the CONV signal. (Refer to Figure 1)

Name	Function	Value	C1, L1 Package
CONV	Convert	ECL	Pin 54
$\overline{CONV}$	Convert Complement	ECL	Pin 53

Analog Input

The TDC1025 comparator array causes the input impedance to vary slightly with the signal level, as comparator input transistors are cut-off or become active. For optimal performance, the source impedance driving the device must be less than 25 Ohms. The input signal will not damage the TDC1025 if it remains within the range of +0.5V to V_{EEA}. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number between 0 and 255, proportional to the magnitude of the analog input. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction. All eight analog input pins should be connected through resistors near the chip to provide a balanced analog input to all portions of the comparator array. The optimized values are shown in Figure 6.

The analog input bandwidth, specified for a full-power input, is limited by the slew rate capabilities of the internal comparators. Decreasing the analog input amplitude will reduce the slew rate, and thus increase the effective bandwidth. Note that other system performance characteristics are specified for the recommended 2V p-p amplitude, and may degrade with the decreased analog input signal. A sample-and-hold circuit at the analog input will also extend performance beyond the specified bandwidth.

Name	Function	Value	C1, L1 Package
V_{IN}	Analog Signal Input	0V to -2V	Pins 44, 47, 48, 51, 52, 56, 57, 60

Outputs

The outputs of the TDC1025 are both differential and single-ended ECL compatible. The outputs should be terminated with a 1.5 kOhm impedance into a -5.2V source to meet the specified logic levels. Using the outputs in a differential mode will provide increased noise immunity.

Name	Function	Value	C1, L1 Package
$\overline{D_1}$	MSB Output, Complement	ECL	Pin 66
D_1	MSB Output	ECL	Pin 67
$\overline{D_2}$		ECL	Pin 68
D_2		ECL	Pin 1
$\overline{D_3}$		ECL	Pin 2
D_3		ECL	Pin 3
$\overline{D_4}$		ECL	Pin 4
D_4		ECL	Pin 5
$\overline{D_5}$		ECL	Pin 30
D_5		ECL	Pin 31
$\overline{D_6}$		ECL	Pin 32
D_6		ECL	Pin 33
$\overline{D_7}$		ECL	Pin 34
D_7		ECL	Pin 35
$\overline{D_8}$	LSB Output, Complement	ECL	Pin 36
D_8	LSB Output	ECL	Pin 37

No Connects

There are several pins labeled No Connect (NC), which have no connections to the chip. These pins should be left open.

Name	Function	Value	C1, L1 Package
NC	No Connect	Open	Pins 6, 9, 10, 11, 12, 15, 17, 19, 21, 24, 25, 26, 27, 38, 42, 43, 45, 59, 61, 65

D

Thermal Design

The case temperature must be limited to a maximum of 80°C for the standard temperature range and 125°C for the extended temperature range. For ambient temperatures above 45°C, 500 L.F.P.M. moving air is required for specified performance. In addition to moving air, heat sinking is an efficient method to optimize thermal management.

Figure 1. Timing Diagram

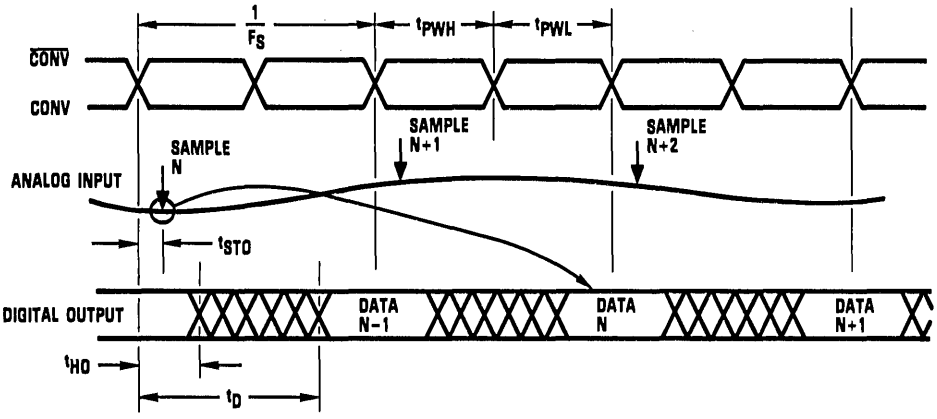
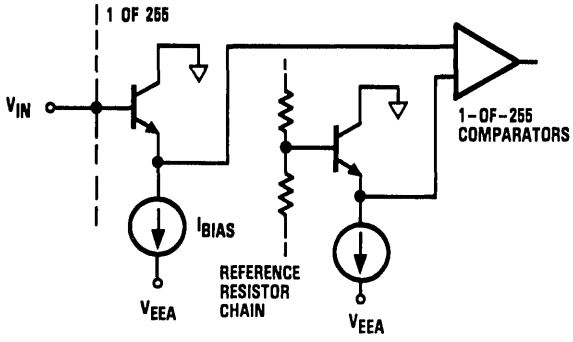
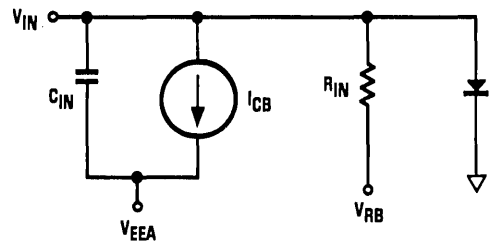


Figure 2. Simplified Analog Input Equivalent Circuit





C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

Figure 3. Convert Input Equivalent Circuit

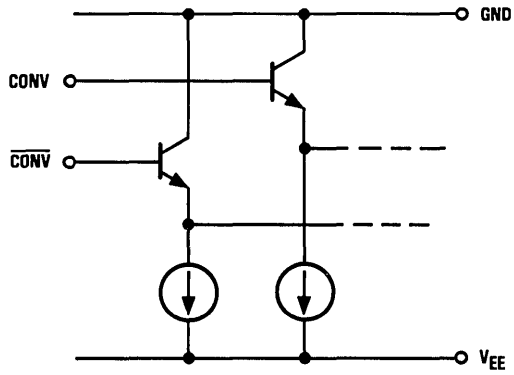
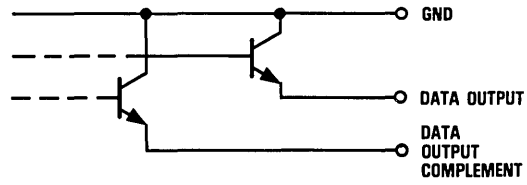
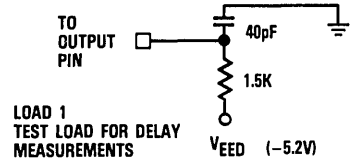


Figure 4. Output Circuits

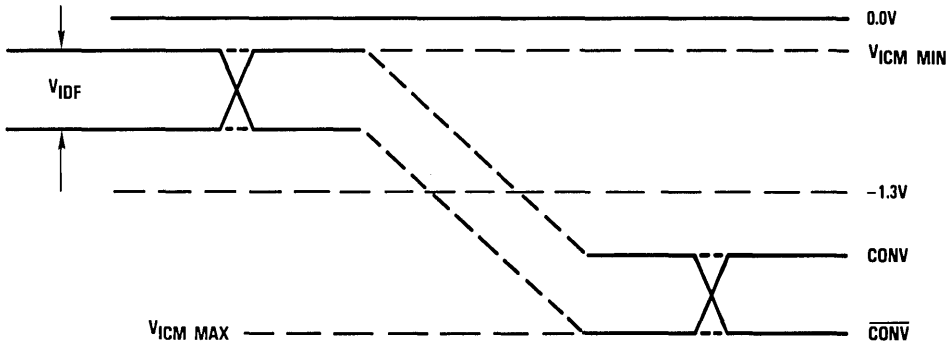


OUTPUT EQUIVALENT CIRCUIT



LOAD 1
TEST LOAD FOR DELAY MEASUREMENTS

Figure 5. CONVert, $\overline{\text{CONV}}$ert Switching Levels



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltages

V_{EED} (measured to D_{GND})	+0.5 to −7.0V
V_{EEA} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	+0.5 to −0.5V
V_{EEA} (measured to V_{EED})	+0.5 to −0.5V

Input Voltages

CONV, $\overline{\text{CONV}}$ (measured to D_{GND})	+0.5 to V_{EED}V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EEA}V
V_{RT} (measured to V_{RB})	0 to +2.5V

Output

Short-circuit duration (single output in high state to ground)	Indefinite

Temperature

Operating, ambient	−55 to +125°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Note:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.

D

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Extended Min	Extended Nom	Extended Max	Units
V_{EED}	Digital Supply Voltage	-4.9	-5.2	-5.5	-4.9	-5.2	-5.5	V
V_{EEA}	Analog Supply Voltage	-4.9	-5.2	-5.5	-4.9	-5.2	-5.5	V
$V_{EEA}-V_{EED}$	Supply Voltage Differential	-0.1	0.0	+0.1	-0.1	0.0	+0.1	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	-0.1	0.0	+0.1	-0.1	0.0	+0.1	V
t_{PWL}	CONV Pulse Width, LOW	8			8			ns
t_{PWH}	CONV Pulse Width, HIGH	10			10			ns
V_{ICM}	CONV Input Voltage, Common Mode	-0.5		-2.5	-0.5		-2.5	V
V_{IDF}	CONV Input Voltage, Differential	0.3		1.2	0.3		1.2	V
V_{RT}	Most Positive Reference Input [1]	-0.1	0.0	+0.1	-0.1	0.0	+0.1	V
V_{RB}	Most Negative Reference Input [1]	-1.9	-2.0	-2.1	-1.9	-2.0	-2.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	1.8	2.0	2.2	1.8	2.0	2.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature [2]	0		70				°C
T_C	Case Temperature [2]	0		100	-55		+125	°C

Notes:

1. V_{RT} Must be more positive than V_{RB}, and voltage reference differential must be within specified range.
2. 500 L.F.P.M. moving air required above 45°C ambient.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
I_{EE}	Supply Current	V_{EEA}, V_{EED} = MAX					
		T_A = 0°C to 70°C		725			mA
		T_A = 70°C		575			mA
		T_C = -55°C to 125°C				850	mA
		T_C = 125°C				500	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM	10	35	10	40	mA
R_{REF}	Total Reference Resistance		57	200	50	200	Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}	10		10		kOhms
C_{IN}	Input Capacitance			160		160	pF
I_{CB}	Input Constant Bias Current	V_{EEA}, V_{EED} = MAX, V_{IN} = 0.0V		750		1200	μA
I_I	Digital Input Current	V_{EEA}, V_{EED} = MAX, V_I = -0.7V		160		240	μA
V_{OL}	Output Voltage, Logic LOW	V_{EEA}, V_{EED} = NOM, I_{OL} = Test Load [1]		-1.6		-1.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{EEA}, V_{EED} = NOM, I_{OH} = Test Load [1]	-0.95		-1.1		V
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		20		20	pF

Note:

1. Test load = 1.5 kOhms to -5.2V, C = 40pF.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{EEA}, V_{EED} = MIN	50		50		MSPS
t_{STO}	Sampling Time Offset	V_{EEA}, V_{EED} = MIN		10		10	ns
t_D	Digital Output Delay	V_{EEA}, V_{EED} = MIN, Load [1]		17		18	ns
t_{HO}	Digital Output Hold Time	V_{EEA}, V_{EED} = MIN, Load [1]	2		2		ns

Note:

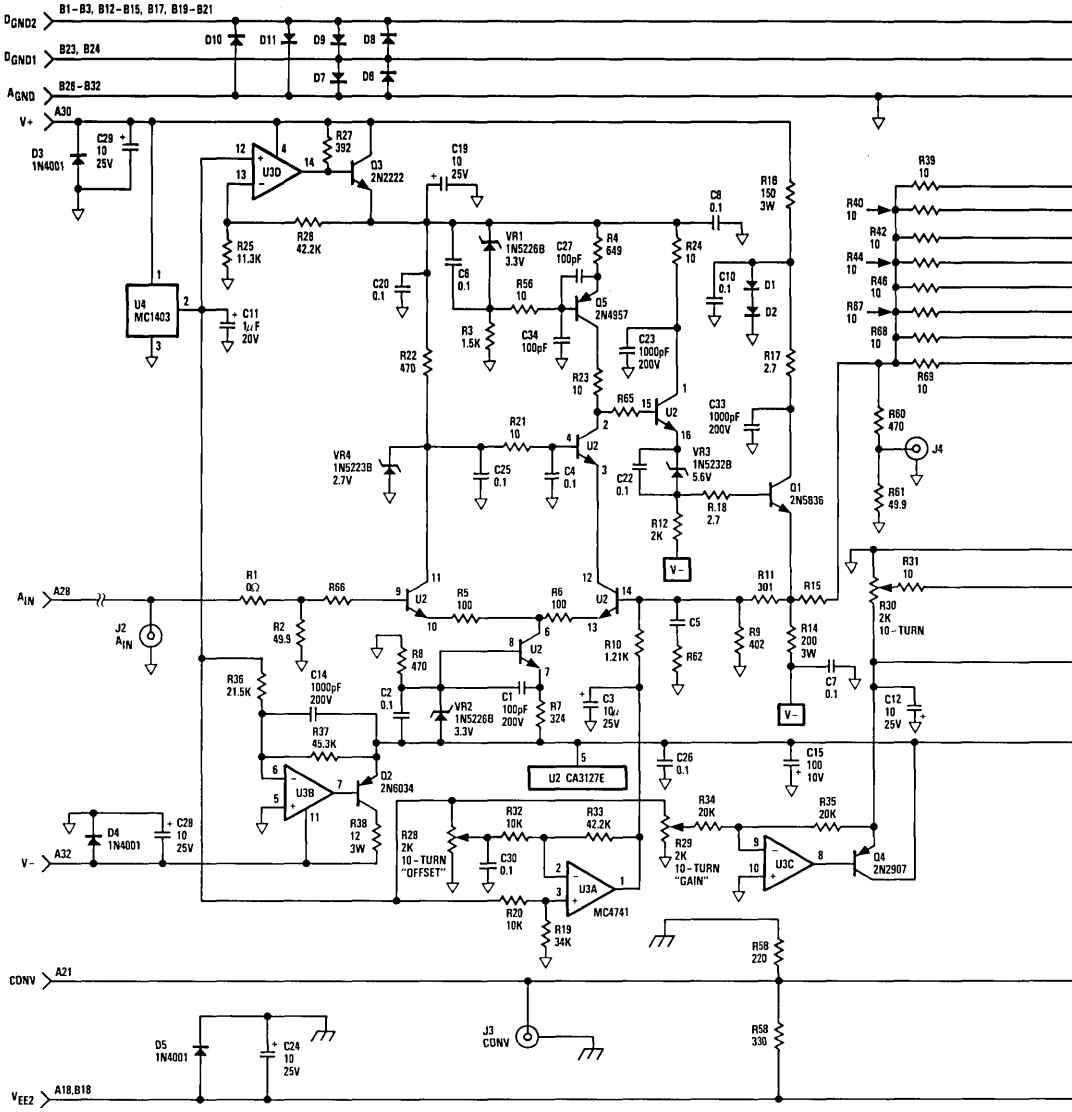
1. Test load = 1.5 kOhms to -5.2V, C = 40pF.

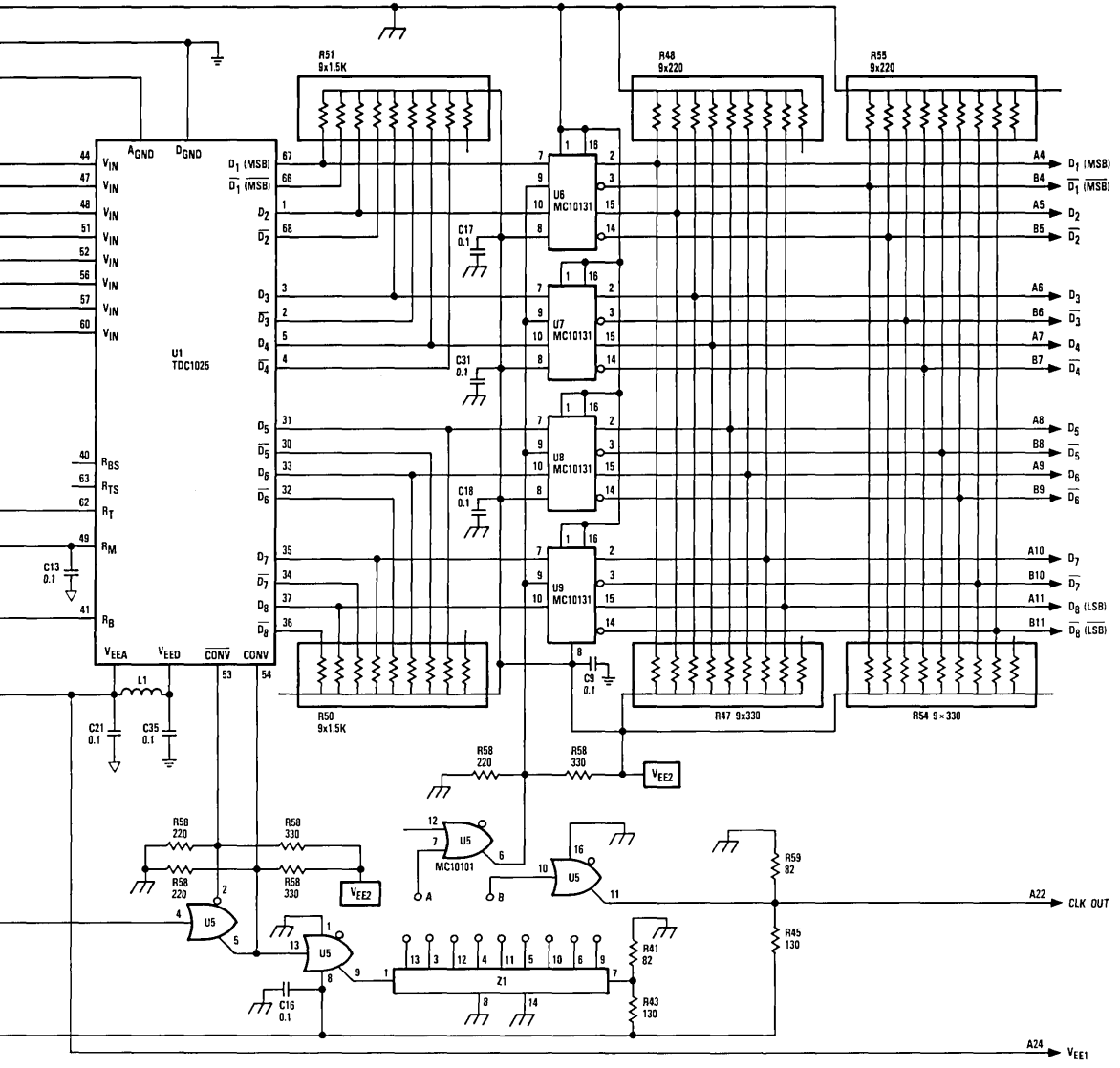
System performance characteristics within specified operating conditions

Parameter			Test Conditions	Temperature Range				Units
				Standard		Extended		
				Min	Max	Min	Max	
E_{LI}	Linearity	Integral, Independent	V_{RT}, V_{RB} = NOM		0.3		0.3	%
E_{LD}	Linearity	Differential			0.3		0.3	%
Q	Code Size		V_{RT}, V_{RB} = NOM	15	185	15	185	% Nominal
E_{OT}	Offset Error	Top	V_{IN} = V_{RT}		+40		+45	mV
E_{OTS}	Offset Error	Top, Sensed			+10		±10	mV
E_{OB}	Offset Error	Bottom	V_{IN} = V_{RB}		-40		-45	mV
E_{OBS}	Offset Error	Bottom, Sensed			-10		±15	mV
T_{COS}	Offset Error	Temperature Coefficient, Sensed			80		80	µV/°C
BW	Bandwidth, Full Power Input			12.5		12.5		MHz
t_{TR}	Transient Response, Full Scale Input Change				10		10	ns
SNR	Signal-to-Noise Ratio		20MHz Bandwidth, 50MSPS Conversion Rate					
		Peak Signal/RMS Noise	1.25MHz Input	53		53		dB
			5.34MHz Input	51		51		dB
			10.0MHz Input			47		dB
			12.0MHz Input	47				dB
		RMS Signal/RMS Noise	1.25MHz Input	44		44		dB
			5.34MHz Input	42		42		dB
			10.0MHz Input			38		dB
			12.0MHz Input	38				dB
EAP	Aperture Error				40		40	ps

D

Figure 6. TDC1025E1C Evaluation Board Schematic




R51
9x1.5K
R48
9x220
R55
9x220
U1
TDC1025
U6
MC10131
U7
MC10131
U8
MC10131
U9
MC10131
C17
0.1
C31
0.1
C18
0.1
C9
0.1
C13
0.1
L1
C21
0.1
C35
0.1
R50
9x1.5K
R47 9x330
R54 9×330
R58
220
R58
330
VEE2
U5
MC10101
R59
82
R45
130
R41
82
R43
130
Z1
C16
0.1
A4
B4
A5
B5
A6
B6
A7
B7
A8
B8
A9
B9
A10
B10
A11
B11
D1 (MSB)
D1 (MSB)
D2
D2
D3
D3
D4
D4
D5
D5
D6
D6
D7
D7
D8 (LSB)
D8 (LSB)
A22
CLK OUT
A24
VEE1

D

Notes for Figure 6

1. All resistor values are in Ohms.
2. All resistors are 1/8W unless otherwise noted.
3. All capacitor values are in microFarads unless otherwise noted.
4. All capacitors are 50WVDC unless otherwise noted.
5. All diodes are 1N4148 unless otherwise noted.
6. R58 is a quad 220/330 Ohm terminator SIP.
7. Z1 is a digital delay line, 2ns per tap, 20ns total Rhombus TZB12-5.
8. L1 is a ferrite bead inductor, Fair-rite part number 2743001112.
9. A_{GND} pins on the TDC1025L1 are: 46, 50, 55, 58.
10. D_{GND} pins on the TDC1025L1 are: 8, 28, 39, 64.
11. V_{EEA} pins on the TDC1025L1 are: 13, 14, 16, 18, 20, 22, 23.
12. V_{EED} pins on the TDC1025L1 are: 7, 29.
13. Values for components C5, R15, R62, R65, R66 are determined during the manufacturing process.
14. Component designators C32, R49, R57, R63, R64, J1 are not used on the TDC1025E1C board.
15. Components R30, R31, R45, R47, R48, R54, R55, R59, R60, R61, J4, are user options and are not included with the board.

Typical Interface

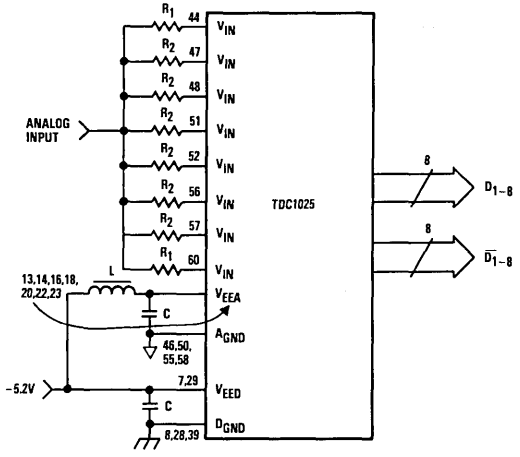
Figure 6 shows an example of a typical interface circuit for the TDC1025. The analog input amplifier is a discrete differential amplifier followed by an NPN transistor. The transistor satisfies the input drive requirement of the A/D converter. The analog input resistors, attached close to the V_{IN} pins, provide frequency stability and a balanced analog input to all portions of the comparator array. All eight V_{IN} pins are connected together close to the device package, and the feedback loop should be closed at that point. Bipolar inputs may be used by adjusting the offset control. The amplifier has a gain of two, increasing a 1 Volt p-p input signal to the recommended 2 Volt p-p input for the A/D.

The top reference, R_T, is grounded, with the sense point, R_{TS}, left open. The offset error introduced at the top of the reference chain is cancelled by the offset adjustment. The bottom reference voltage, V_{RB} is supplied by an amplifier, and a PNP transistor. The feedback loop through the sense, R_{BS}, minimizes the offset error and related temperature variations at the bottom of the resistor chain. Additional gain adjustment can be made by varying the input voltage to the sensing op-amp.

The differential clock is provided by an ECL gate, with termination close to the TDC1025 to minimize ringing or overshoot. The convert clock is delayed by approximately 5-10ns to latch the data at the output. The data outputs are terminated with 1.5 kOhms to -5.2V. The standard Thevenin equivalent (220 Ohms-330 Ohms to -5.2V) is used where additional termination is required.

The analog and digital ground planes are separated to minimize ground noise and prevent ground loops, and are connected back at the power supply. The independent ECL digital ground aids in maintaining the chip digital ground, especially in a system with high-speed ECL logic. Protective diodes between all three ground planes avoid damage due to excessive differences in ground potential.

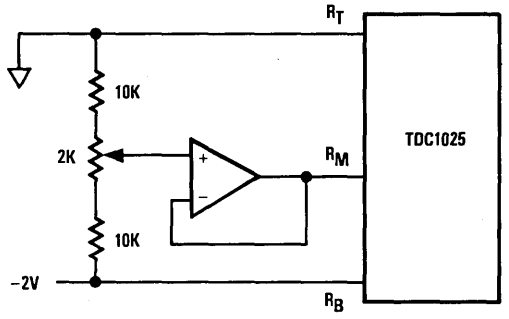
Figure 7. Power Decoupling and Input Network



L = FERRITE BEAD INDUCTOR
R_1 = 10Ω, 1% CARBON COMPOSITION OR CERAMIC CHIP RESISTOR
R_2 = 10Ω, 1% CARBON COMPOSITION OR CERAMIC CHIP RESISTOR
C = 0.1μF CERAMIC DISC CAPACITOR
⏚ = ANALOG GROUND
⏚ = DIGITAL GROUND

Note: Pins are shown for L1, C1 packages

Figure 8. Typical Reference Midpoint Adjust Circuit



D

Output Coding

Step	Range		Binary		Offset Two's Complement	
			True	Inverted	True	Inverted
	−2.0000V FS 7.8431 mV Step	−2.0480V FS 8.000 mV Step		All Outputs Inverted	D_1 Inverted	D_2–D_9 Inverted
000	0.0000V	0.0000V	000000000	111111111	100000000	011111111
001	−0.0078V	−0.0080V	000000001	111111110	100000001	011111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
127	−0.9961V	−1.0160V	011111111	100000000	111111111	000000000
128	−1.0039V	−1.0240V	100000000	011111111	000000000	111111111
129	−1.0118V	−1.0320V	100000001	011111110	000000001	111111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
254	−1.9921V	−2.0392V	111111110	000000001	011111110	100000001
255	−2.0000V	−2.0400V	111111111	000000000	011111111	100000000

Note:

1. Voltages are code midpoints after calibration.
2. Any output may be inverted by interchanging connections to the true (D_N) and complement ($\overline{D_N}$) output pins.

Calibration

To calibrate the TDC1025, adjust V_{RT} and V_{RB} to set the 1st and 255th thresholds to the desired voltages. Note that R_1 is greater than R, ensuring calibration with a positive voltage on R_T. Assuming a 0V to −2V desired range, continuously strobe the converter with −0.0039V (1/2 LSB from 0V) on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −1.996V (1/2 LSB from −2V) and adjust V_{RB} for toggling between codes 254 and 255.

The degree of required adjustment is indicated by the offset errors, E_{OT} and E_{OB}. Offset errors are generated by the inherent parasitic resistance between the package pin and the actual resistor chain on the integrated circuit. These parasitic resistors are shown as R_1 and R_2 in the Functional Block Diagram. Calibration will cancel all offset voltages, eliminating offset and gain errors.

The above method of calibration requires that both ends of the resistor chain, R_T and R_B, are driven by buffered operational amplifiers. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with a buffer offset control. The offset error at the bottom of the resistor chain results in a slight gain error, which can be compensated for by varying the voltage applied to R_B. The bottom reference is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in Figure 5.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1025C1C	STD-T_C = 0°C to 80°C	Commercial	68 Contact Chip Carrier	1025C1C
TDC1025C1G	STD-T_C = 0°C to 80°C	Commercial With Burn-In	68 Contact Chip Carrier	1025C1G
TDC1025C1F	EXT-T_C = -55°C to 125°C	Commercial	68 Contact Chip Carrier	1025C1F
TDC1025C1A	EXT-T_C = -55°C to 125°C	High Reliability[1]	68 Contact Chip Carrier	1025C1A
TDC1025L1C	STD-T_C = 0°C to 80°C	Commercial	68 Leaded Chip Carrier	1025L1C
TDC1025L1G	STD-T_C = 0°C to 80°C	Commercial With Burn-In	68 Leaded Chip Carrier	1025L1G
TDC1025L1F	EXT-T_C = -55°C to 125°C	Commercial	68 Leaded Chip Carrier	1025L1F
TDC1025L1A	EXT-T_C = -55°C to 125°C	High Reliability[1]	68 Leaded Chip Carrier	1025L1A

Note:

1. Per TRW document 70Z01757.

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Preliminary Information describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact TRW for current information.

D

TDC1027

Monolithic Video A/D Converter
7-bit, 18MSPS

The TRW TDC1027 is an 18 MegaSample Per Second (MSPS) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 5MHz into 7-bit digital words. A sample-and-hold circuit is not necessary. All digital inputs and outputs are TTL compatible.

The TDC1027 consists of 127 clocked latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

Note: TRW recommends the use of the TDC1047 for new designs.

Features

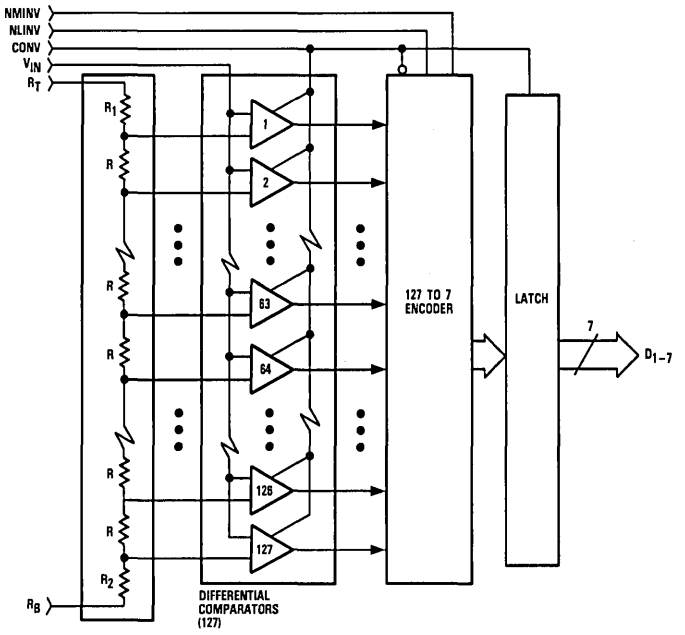
- 7-Bit Resolution
- 1/2 LSB Linearity
- Sample-And-Hold Circuit Not Required
- TTL Compatible
- 18MSPS Conversion Rate
- Selectable Output Format
- Available In 24 Lead DIP or CERDIP
- Low Cost

Applications

- Low-Cost Video Digitizing
- Medical Imaging
- Data Acquisition
- TV Special Effects
- Video Simulators
- Radar Data Conversion

D

Functional Block Diagram



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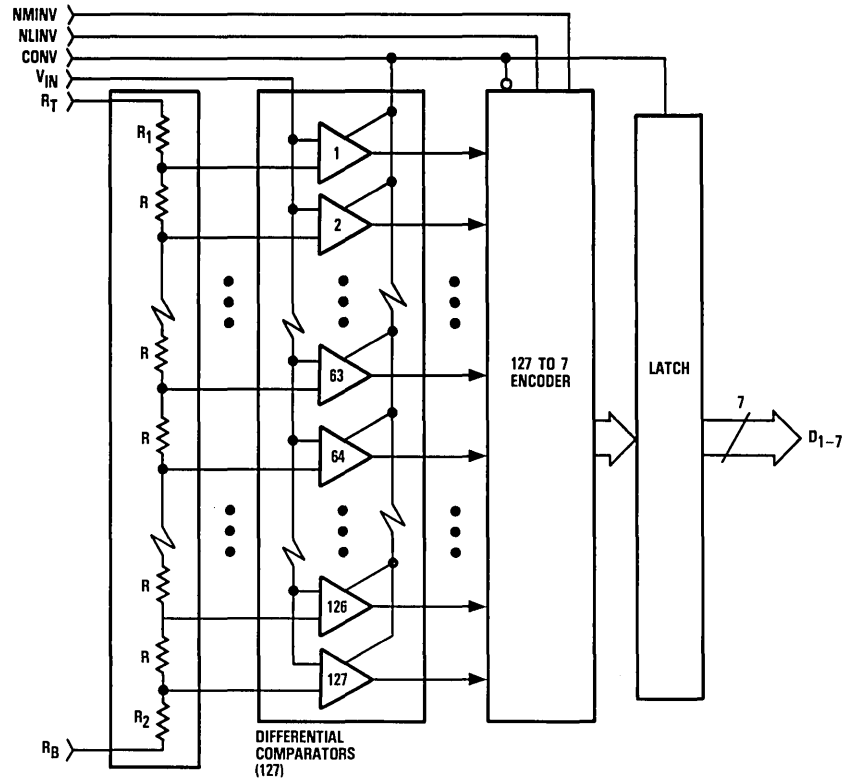
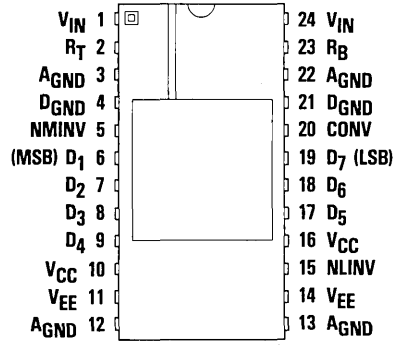
Functional Block Diagram



Pin Assignments



24 Lead DIP – J7 Package
24 Lead CERDIP – B7 Package

Functional Description

General Information

The TDC1027 has three functional sections: a comparator array, encoding logic, and output latches. The comparator array compares the input signal with 127 reference voltages to produce an N-of-127 code (sometimes referred to as a "thermometer" code, as all the comparators below the signal will be on, and all those above the signal will be off). The encoding logic converts the N-of-127 code into binary or offset two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV. The output latch holds the output constant between updates.

Power

The TDC1027 operates from two supply voltages, +5.0V and -5.2V. The return for I_{CC}, the current drawn from the +5.0V supply, is D_{GND}. The return for I_{EE}, the current drawn from the -5.2V supply, is A_{GND}. All power and ground pins must be connected.

Name	Function	Value	J7, B7 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pins 10, 16
V_{EE}	Negative Supply Voltage	-5.2V	Pins 11, 14
D_{GND}	Digital Ground	0.0V	Pins 4, 21
A_{GND}	Analog Ground	0.0V	Pins 3, 12, 13, 22

Reference

The TDC1027 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between +0.1V and -2.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain ($V_{RT}-V_{RB}$) must be between 0.8V and 1.2V. The nominal voltages are V_{RT} = 0.05V and V_{RB} = -1.04V. These voltages may be varied dynamically up to 5MHz. Due to variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically (as in an AGC circuit), a low-impedance reference source is required.

Name	Function	Value	J7, B7 Package
R_T	Reference Resistor (Top)	0.0V	Pin 2
R_B	Reference Resistor (Bottom)	-1.0V	Pin 23

Controls

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e. steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the Output Coding table given on page 8. These pins are active LOW as signified by the prefix "N" in the signal name. They may be tied to V_{CC} for a logic "1" and D_{GND} for a logic "0."

Name	Function	Value	J7, B7 Package
NMINV	Not Most Significant Bit INVert	TTL	Pin 5
NLINV	Not Least Significant Bit INVert	TTL	Pin 15

Convert

The TDC1027 requires a CONVert (CONV) signal. A sample is taken (the comparators are latched) approximately 10ns after a rising edge on the CONV pin. This time is t_{STO}, Sampling Time Offset. This delay varies by a few nanoseconds from part to part and as a function of temperature, but the short-term uncertainty (jitter) in sampling offset time is less than 100 picoseconds. The 127 to 7 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output latches on the next rising edge. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONVert signal. This permits the previous conversion result to be acquired by external circuitry at that rising edge, i.e. data for sample N is acquired by the external circuitry while the TDC1027 is taking input sample N + 2.

Name	Function	Value	J7, B7 Package
CONV	Convert	TTL	Pin 20

Analog Input

The TDC1027 uses strobed latching comparators which cause the input impedance to vary with the signal level, as comparator input transistors are cut-off or become active. As a result, for optimal performance, the source impedance of the driving device must be less than 25 Ohms. The input signal will not damage the TDC1027 if it remains within the range of V_{EE} to +0.5V. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number between 0 and 127 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction. Both analog input pins must be connected through individual 10 Ohm resistors to the input driver.

Name	Function	Value	J7, B7 Package
V_{IN}	Analog Signal Input	0V to -1V	Pins 1, 24

Outputs

The outputs of the TDC1027 are TTL compatible, and capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. For optimum performance, 2.2 kOhm pull-up resistors are recommended.

Name	Function	Value	J7, B7 Package
D_1	MSB Output	TTL	Pin 6
D_2		TTL	Pin 7
D_3		TTL	Pin 8
D_4		TTL	Pin 9
D_5		TTL	Pin 17
D_6		TTL	Pin 18
D_7	LSB Output	TTL	Pin 19

Figure 1. Timing Diagram

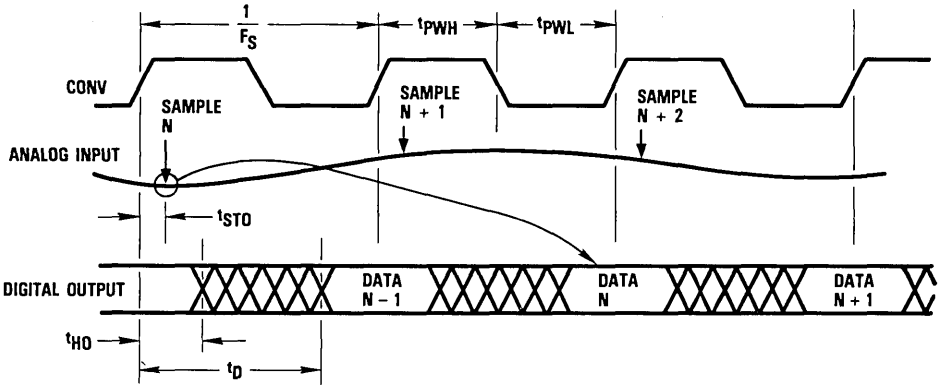
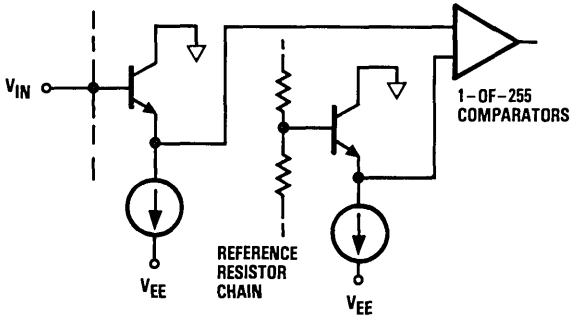
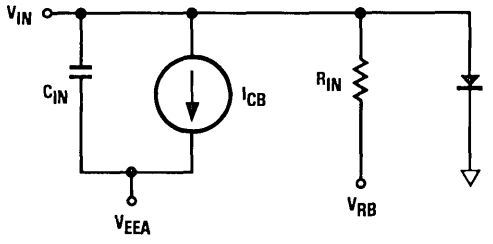


Figure 2. Simplified Analog Input Equivalent Circuit





C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

D

Figure 3. Digital Input Equivalent Circuit

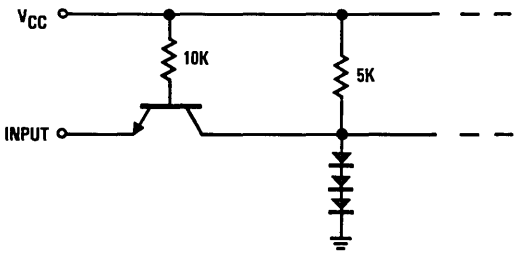
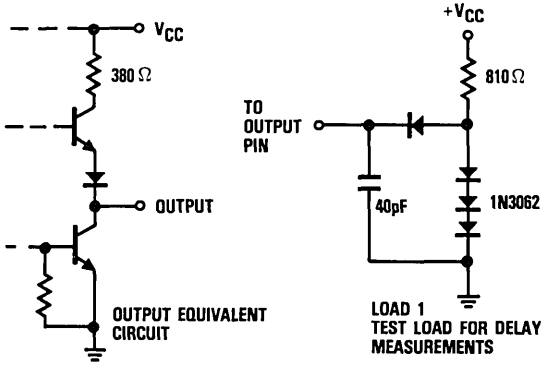


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND})	0.0 to +7.0V
V_{EE} (measured to A_{GND})	0.0 to −7.0V
A_{GND} (measured to D_{GND})	−1.0 to +1.0V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EE}V
V_{RT} (measured to V_{RB})	+2.2 to −2.2V

Output

Applied voltage (measured to D_{GND})	−0.5 to 5.5V [2]
Applied current, externally forced	−1.0 to 6.0 mA [3,4]
Short circuit duration (single output in high state to ground)	1 sec

Temperature

Operating, ambient	−60 to +140°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{CC}	Positive Supply Voltage (Measured to D_{GND})	4.75	5.0	5.25	V
V_{EE}	Negative Supply Voltage (Measured to A_{GND})	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	24			ns
t_{PWH}	CONV Pulse Width, HIGH	28			ns
V_{IL}	Input Voltage, Logic LOW			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			V
I_{OL}	Output Current, Logic LOW			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400	μA
V_{RT}	Most Positive Reference Input [1]	−1.1	0.0	0.1	V
V_{RB}	Most Negative Reference Input [1]	−0.9	−1.0	−2.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	0.8	1.0	1.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70	°C

Note:

1. V_{RT} Must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
I_{CC}	Positive Supply Current	V_{CC} = MAX, static[1]		40	mA
I_{EE}	Negative Supply Current	V_{EE} = MAX, static[1]			
		T_A = 0°C to 70°C		-275	mA
		T_A = 70°C		-180	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM	5.0	30	mA
R_{REF}	Total Reference Resistance		30	200	Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}	5.0		kOhms
C_{IN}	Input Capacitance			100	pF
I_{CB}	Input Constant Bias Current	V_{EE} = MAX		200	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.5V			
		NLINV		-2.4	mA
		CLK, NMINV		-2.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V		100	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, Output HIGH, one pin to ground, one second duration.		-25	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15	pF

Note:

1. Worst case, all digital inputs and outputs LOW.

D

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
F_S	Maximum Conversion Rate	V_{CC} = MIN, V_{EE} = MIN	18		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = MIN, V_{EE} = MIN	0	15	ns
t_D	Output Delay	V_{CC} = MIN, V_{EE} = MIN, Load 1		35	ns
t_{HO}	Output Hold Time	V_{CC} = MIN, V_{EE} = MIN, Load 1	10		ns

System performance characteristics within specified operating conditions

Parameter			Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
E_{LI}	Linearity Error	Integral, Independent	V_{RT}, V_{RB} = NOM		0.4	%
E_{LD}	Linearity Error	Differential			0.4	%
Q	Code Size		V_{RT}, V_{RB} = NOM	30	170	% Nominal
E_{OT}	Offset Error	Top	V_{IN} = V_{RT}		45	mV
E_{OB}	Offset Error	Bottom	V_{IN} = V_{RB}		−35	mV
T_{CO}	Offset Error	Temperature Coefficient			±40	μV/°C
BW	Bandwidth, Full Power Input			5		MHz
t_{TR}	Transient Response, Full Scale				30	ns
SNR	Signal-to-Noise Ratio		5MHz Bandwidth, 18MSPS Conversion Rate			
		Peak Signal/RMS Noise	1.248MHz Input	48		dB
			2.438MHz Input	47		dB
		RMS Signal/RMS Noise	1.248MHz Input	39		dB
			2.438MHz Input	38		dB
NPR	Noise Power Ratio		DC to 8MHz White Noise Bandwidth, 4 Sigma Loading, 1.248MHz Slot, 18MSPS Conversion Rate	30		dB
E_{AP}	Aperture Error				50	ps

Output Coding

Step	Range		Binary True	Binary Inverted	Offset Two's Complement True	Offset Two's Complement Inverted
	−1.0000V FS 7.874 mV STEP	−1.0160V FS 8.000 mV STEP	NMINV = 1 NLINV = 1	0 0	0 1	1 0
000	0.0000V	0.0000V	0000000	1111111	1000000	0111111
001	−0.0078V	−0.0080V	0000001	1111110	1000001	0111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
127	−1.0000V	−1.0160V	1111111	0000000	0111111	1000000

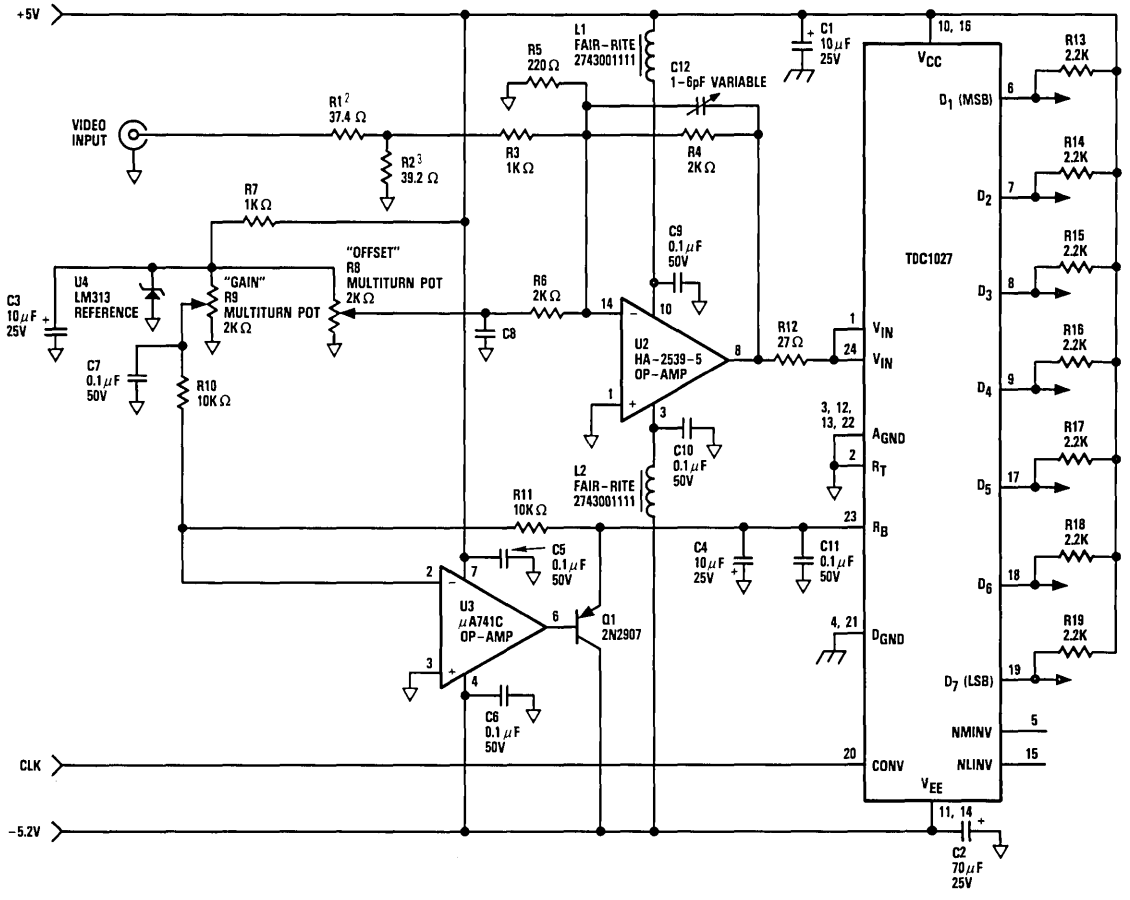
Note:

1. Voltages are code midpoints when calibrated using the procedure given on page 9.

Calibration

To calibrate the TDC1027, adjust V_{RT} and V_{RB} to set the 1st and 127th thresholds to the desired voltages. Note that R_1 is greater than R, ensuring calibration with a positive voltage on R_T. Assuming a 0V to −1V desired range, continuously strobe the converter with −0.0039V on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −0.9961V and adjust V_{RB} for toggling between codes 126 and 127. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with a buffer offset control. R_B is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in Figure 5.

Figure 5. Typical Interface Circuit



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1027J7C	STD-T_A = 0°C to 70°C	Commercial	24 Lead DIP	1027J7C
TDC1027J7G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	24 Lead DIP	1027J7G
TDC1027B7C	STD-T_A = 0°C to 70°C	Commercial	24 Lead CERDIP	1027B7C
TDC1027B7G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	24 Lead CERDIP	1027B7G

Notes:

1. Per TRW document 70Z01757.
2. TRW recommends the use of the TDC1047 for new designs.

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Preliminary Information describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact TRW for current information.

TDC1029
Preliminary Information

Monolithic A/D Converter
6-bit, 100MSPS

The TRW TDC1029 is a 100 MegaSample Per Second (MSPS) fully-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full power frequency components up to 50MHz into 6-bit digital words. A sample-and-hold circuit is not required. All digital inputs and outputs are ECL compatible.

The TDC1029 consists of 63 latching comparators, combining logic, and an output register. A differential convert (CONV) signal controls the conversion operation. The digital outputs are single-ended ECL with the exception of the MSB which is differential enabling binary or offset two's complement output format.

The device is offered in two packages, a 24 lead DIP and a 28 lead DIP. The only difference between these packages is that the midpoint taps are available when using the 28 lead DIP.

Features

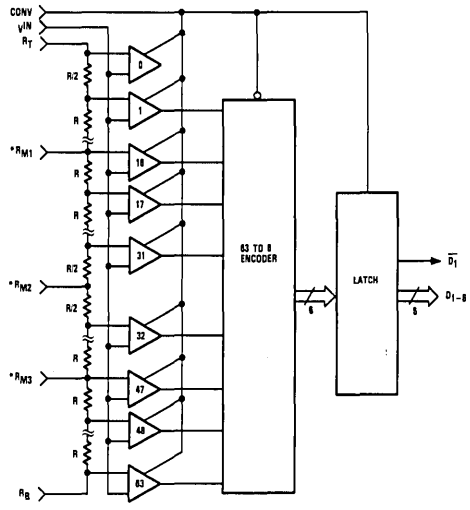
- 6-Bit Resolution
- 100MSPS Conversion Rate
- 50MHz Input Bandwidth
- Low Cost
- 1/2 LSB Linearity
- Sample-And-Hold Circuit Not Required
- 1V Input Range
- Binary Or Two's Complement Output Format
- 1/4, 1/2 And 3/4 Scale Reference Resistor Taps On J6 Package
- Available In 24 Or 28 Lead DIP
- Evaluation Board - TDC1029E1C

Applications

- Transient Digitizers
- Direct Digital Receivers
- Radar Data Conversion
- Data Acquisition
- Telecommunications
- Medical Imaging
- High-Energy Physics Experimentation

D

Functional Block Diagram



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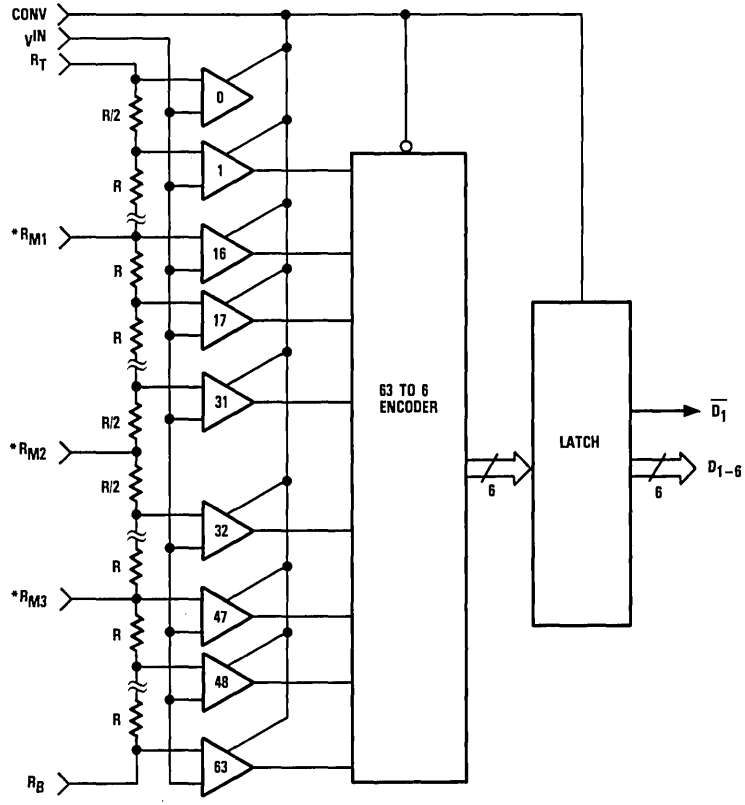
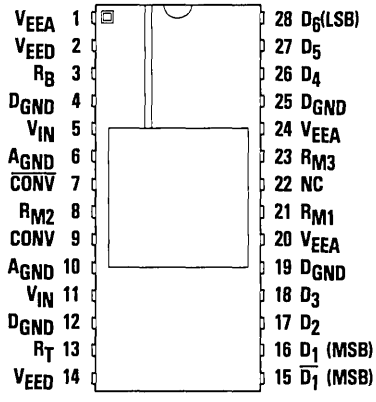
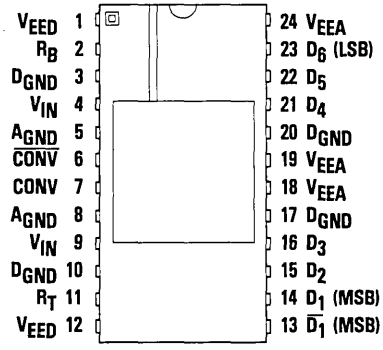
Functional Block Diagram



Pin Assignments



28 Lead DIP - J6 Package



24 Lead DIP - J7 Package

Functional Description

General Information

The TDC1029 has three functional sections: a comparator array, encoding logic, and output latches. The comparator array compares the input signal with 63 reference voltages to produce an N-of-63 code (sometimes referred to as a "thermometer" code, as all the comparators biased more positive than the input signal will be on, and all the rest will be off.) The encoding logic converts the N-of-63 code into binary data, with the complement of the MSB available for offset two's complement output format. The output latch holds the output data constant between updates.

Power

The TDC1029 operates from separate analog and digital power supplies, V_{EEA} and V_{EED}. Since the required voltage for both V_{EEA} and V_{EED} is -5.2V, these should ultimately be connected to the same power source, but separate decoupling for each is recommended. A typical decoupling network is shown in the typical interface circuit. The return path for I_{EED}, the current drawn from the V_{EED} supply is D_{GND}. The return path for I_{EEA}, the current drawn from the V_{EEA} supply, is A_{GND}. All power and ground pins must be connected.

Name	Function	Value	J7 Package	J6 Package
V_{EEA}	Analog Supply Voltage	-5.2V	18, 19, 24	1, 20, 24
V_{EED}	Digital Supply Voltage	-5.2V	1, 12	2, 14
D_{GND}	Digital Ground	0.0V	3, 10, 17, 20	4, 12, 19, 25
A_{GND}	Analog Ground	0.0V	5, 8	6, 10

Thermal Design

The TDC1029 has thermal characteristics similar to other high-performance ECL devices and is rated for a maximum ambient temperature of 70°C. For ambient temperatures above 40°C, 500 L.F.P.M. moving air is required for specified performance. The maximum case temperature should be no greater than 110°C.

D

Reference

The TDC1029 comes in two different packages. In the 24 lead DIP the reference voltage is applied between R_T and R_B. TDC1029 converts analog signals in the range $V_{RB} \geq V_{IN} \geq V_{RT}$ into digital form. In the 28 lead DIP package three additional reference points are provided. These reference points can either be used to help improve the integral linearity to a level beyond that listed for non-corrected integral linearity, E_{LI}, or the user may find other uses for the added taps as shown in the Applications section. The voltage applied across the reference resistor chain (V_{RT}-V_{RB}) must be between 0.9V and 1.1V. V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between -0.2V and -1.4V. V_{RT} should be more positive than V_{RB} within that range. The nominal voltages are: V_{RT} = -0.3V, V_{RB} = -1.3V. These voltages may be varied dynamically up to 25MHz. Due to slight variations in the reference current with changes in clock and input signals, R_T and R_B should be low-impedance points. For circuits in which the reference is not varied, a bypass capacitor to A_{GND} is recommended. If the reference inputs are varied dynamically (as in an AGC circuit), a low-impedance reference source is required.

Name	Function	Value	J7 Package	J6 Package
R_T	Reference Top	-0.30V	11	13
R_{M1}	1/4 Scale Tap	-0.55V	N/A	21
R_{M2}	1/2 Scale Tap	-0.80V	N/A	8
R_{M3}	3/4 Scale Tap	-1.05V	N/A	23
R_B	Reference Bottom	-1.30V	2	3

Convert

The TDC1029 requires a differential ECL CONVert (CONV) signal. A sample is taken (the comparators are latched) t_{STO} after a rising edge on the CONV pin. The result from the encoding logic is transferred to the output latches on the next rising edge. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONVert signal. New data becomes valid after a maximum delay time t_D. Both convert inputs must be connected, with CONV being the complement of $\overline{CONV}$.

Name	Function	Value	J7 Package	J8 Package
CONV	Convert	ECL	7	9
$\overline{CONV}$	Convert Complement	ECL	8	7

Analog Input

The TDC1029 uses latching comparators which cause the input impedance to vary slightly with the signal level. For optimal performance, the source impedance driving the device must be less than 25 Ohms. The input signal will not damage the TDC1029 if it remains within the range of +0.5V to V_{EEA}. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number between 0 and 63 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction. Both analog input pins MUST be connected through 15 Ohm resistors as shown in the Typical Interface Circuit.

Name	Function	Value	J7 Package	J8 Package
V_{IN}	Analog Signal Input	See Text	4, 9	5, 11

Outputs

The outputs of the TDC1029 are ECL compatible. Outputs D_{2-6} are single-ended, while the MSB (D_1) is differential. Offset two's complement format is available by cross-wiring the MSB, i.e. interchanging D_1 and $\overline{D_1}$. The outputs should be terminated with a 100 Ohm (or greater) impedance into a -2.0V source.

Name	Function	Value	J7 Package	J8 Package
$\overline{D_1}$	MSB Output Complement	ECL	13	15
D_1	MSB Output	ECL	14	16
D_2		ECL	15	17
D_3		ECL	16	18
D_4		ECL	21	26
D_5		ECL	22	27
D_6	LSB Output	ECL	23	28

Figure 1. Timing Diagram

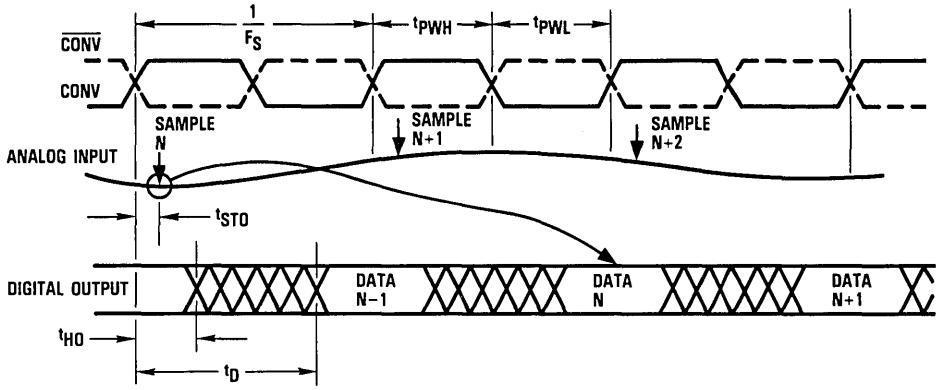
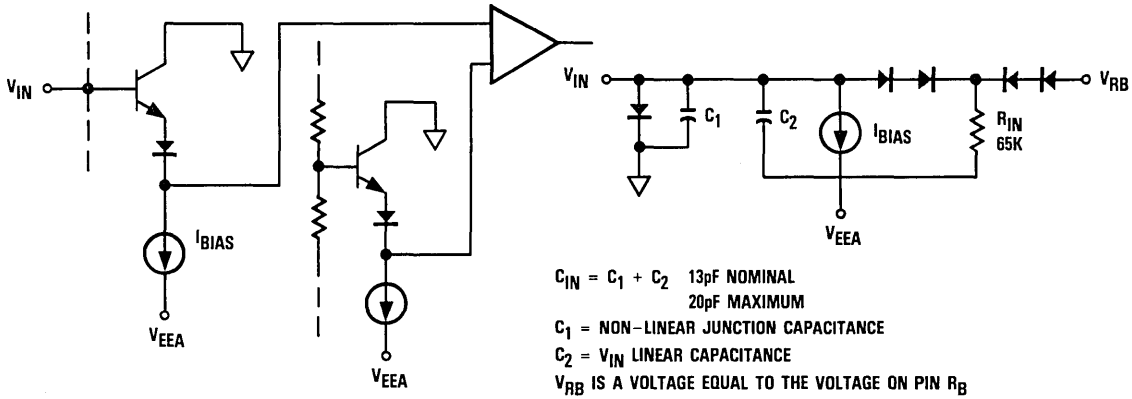


Figure 2. Simplified Analog Input Equivalent Circuit



$C_{IN} = C_1 + C_2$ 13pF NOMINAL
20pF MAXIMUM
C_1 = NON-LINEAR JUNCTION CAPACITANCE
C_2 = V_{IN} LINEAR CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

D

Figure 3. Convert Input Equivalent Circuit

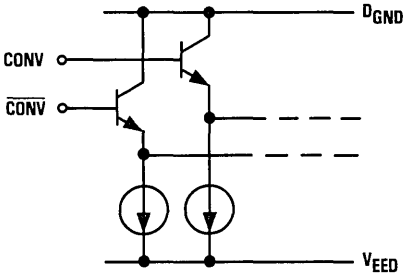
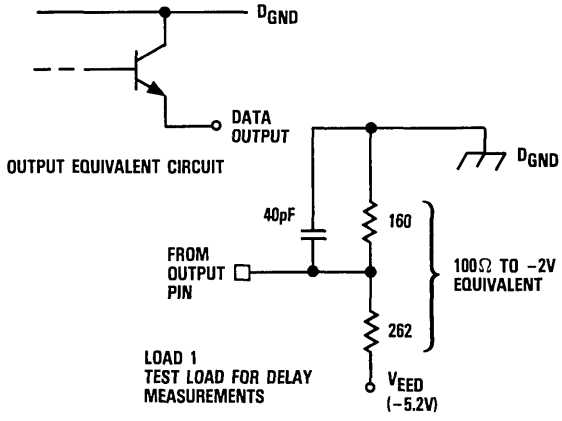


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltages

V_{EED} (measured to D_{GND})	0.5 to −7.0V
V_{EEA} (measured to A_{GND})	0.5 to −7.0V
A_{GND} (measured to D_{GND})	1.0 to −1.0V
V_{EEA} (measured to V_{EED})	0.5 to −0.5V

Input Voltages

CONV, $\overline{CONV}$ (measured to D_{GND})	+0.5 to V_{EED}V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EEA}V
V_{RT} (measured to V_{RB})	+1.5 to −1.5V

Output

Short circuit duration (single output to ground)	Indefinite

Temperature

Operating, ambient	−60 to +115°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Note:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{EED}	Digital Supply Voltage	−4.9	−5.2	−5.5	V
V_{EEA}	Analog Supply Voltage	−4.9	−5.2	−5.5	V
$V_{EEA}-V_{EED}$	Supply Voltage Differential	−0.1	0.0	0.1	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	3	4		ns
t_{PWH}	CONV Pulse Width, HIGH	5	6		ns
V_{ICM}	CONV Input Voltage, Common Mode Range (Figure 6)	−0.5		−2.5	V
V_{IDF}	CONV Input Voltage, Differential (Figure 6)	0.4		1.2	V
V_{RT}	Most Positive Reference Input [1]	−0.2	−0.3	−0.4	V
V_{RB}	Most Negative Reference Input [1]	−1.2	−1.3	−1.4	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	0.9	1.0	1.1	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V
T_A	Ambient Temperature [2]	0		70	°C

Notes:

1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.
2. 500 L.F.P.M. moving air required above 40°C.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
$I_{EEA}+I_{EED}$	Supply Current	V_{EEA}, V_{EED} = MAX			
		T_A = 0°C to 70°C		-375	mA
		T_A = 70°C		-300	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM	10	35	mA
R_{REF}	Total Reference Resistance		29	100	Ohm
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}, V_{EE} = MAX	6		kOhm
C_{IN}	Input Equivalent Capacitance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}		20	pF
I_{CB}	Input Constant Bias Current	V_{EEA}, V_{EED} = MAX, V_{IN} = -0.3V		500	μA
I_I	Input Current	V_{EEA}, V_{EED} = MAX, V_I = -0.5V		250	μA
V_{OL}	Output Voltage, Logic LOW	V_{EEA}, V_{EED} = NOM, Test Load 1		-1.650	V
V_{OH}	Output Voltage, Logic HIGH	V_{EEA}, V_{EED} = NOM, Test Load 1	-0.950		V
C_I	Digital Input Capacitance	T_A = 25°C		15	pF

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
F_S	Maximum Conversion Rate	V_{EEA}, V_{EED} = MIN	100		MSPS
t_{STO}	Sampling Time Offset	V_{EEA}, V_{EED} = MIN	0	6	ns
t_D	Output Delay	V_{EEA}, V_{EED} = MIN, Load 1		7	ns
t_{HO}	Output Hold Time	V_{EEA}, V_{EED} = MIN, Load 1	1.5		ns

D

System performance characteristics within specified operating conditions

Parameter			Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
E_{LI}	Linearity Error	Integral, Terminal Based	V_{RT}, V_{RB} = NOM		±0.8	%
E_{LD}	Linearity Error	Differential			±0.8	%
Q	Code Size		V_{RT}, V_{RB} = NOM	50	150	% Nominal
E_{OT}	Offset Error	Top	V_{IN} = V_{RT}		20	mV
E_{OB}	Offset Error	Bottom	V_{IN} = V_{RB}		-8	mV
T_{CO}	Offset Error	Temperature Coefficient			±35	µV/°C
BW	Bandwidth, Full Power Input [1]		F_S = 100MSPS	50		MHz
t_{TR}	Transient Response, Full-Scale Input Change				6	ns
SNR	Signal-To-Noise-Ratio [2]		100MSPS Conversion Rate			
		Peak Signal/RMS Noise	25MHz Input	42		dB
			50MHz Input	39		dB
		RMS Signal/RMS Noise	25MHz Input	33		dB
			50MHz Input	30		dB
E_{AP}	Aperture Error				30	ps

Notes:

1. Beat frequency sinusoidal reconstruction producing no errors greater then 3 LSBs, t_{PWH} = 6ns.
2. Single frequency sinusoidal input attenuated 3dB at 1/2 sampling frequency (anti-alias prefilter).

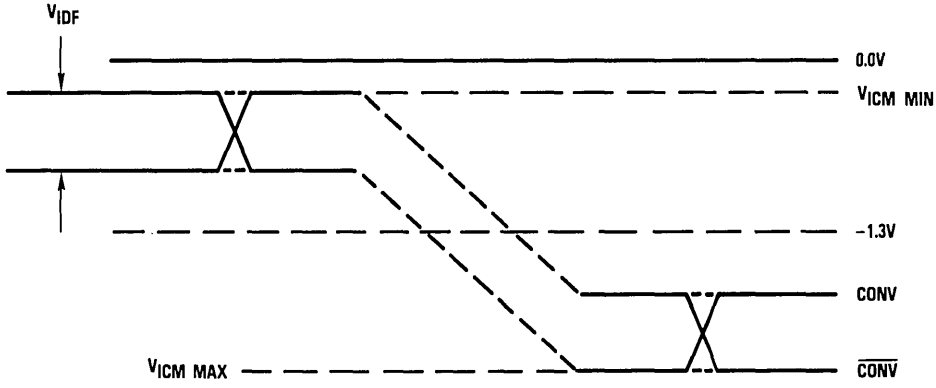
Output Coding [1]

Step	Range		Binary	Offset Two's Complement
	-1.3000V FS 15.8730mV STEP	-1.3080V FS 16.0000mV STEP	MSB LSB	MSB LSB
00	-0.3000V	-0.3000V	000000	100000
01	-0.3159V	-0.3160V	000001	100001
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
31	-0.7921V	-0.7960V	011111	111111
32	-0.8079V	-0.8120V	100000	000000
33	-0.8238V	-0.8280V	100001	000001
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
62	-1.2841V	-1.2920V	111110	011110
63	-1.3000V	-1.3080V	111111	011111

Note:

1. Voltages are code midpoints after calibration.

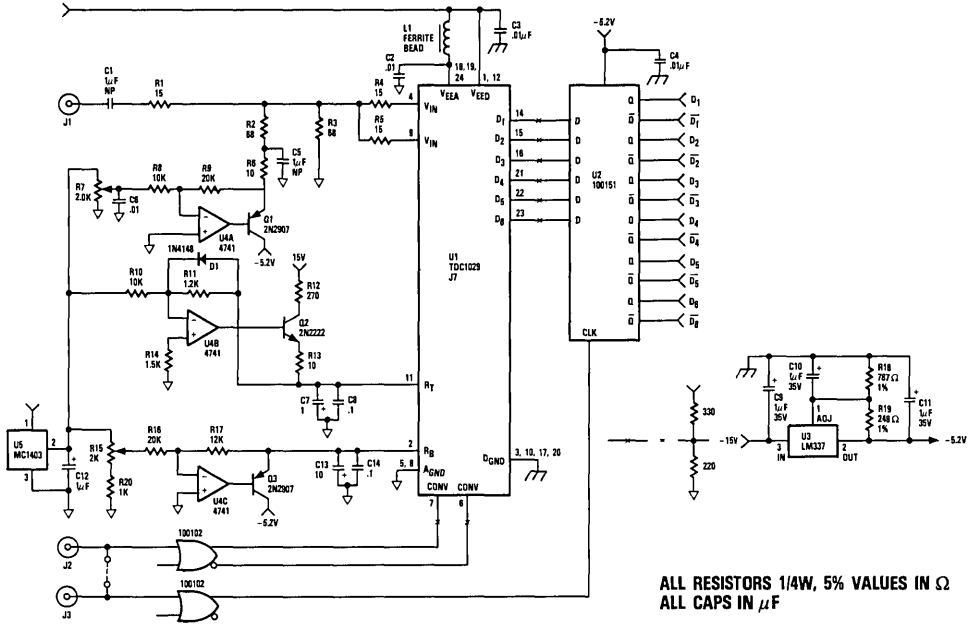
Figure 5. CONVert, $\overline{\text{CONVert}}$ Switching Levels



Calibration

To calibrate the TDC1029, adjust V_{RT} and V_{RB} to set 1st and 63rd thresholds to the desired voltages. Assuming a −0.3V to −1.3V desired range, continuously strobe the converter with −0.3079V (1/2 LSB from −0.300V) on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −1.2921V (1/2 LSB from −1.300V) and adjust V_{RB} for toggling between codes 62 and 63. Instead of adjusting V_{RT}, R_T can be connected to a fixed voltage and the most positive end of the range calibrated with an offset control. R_B is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in Figure 6.

Figure 6. Typical Interface Circuit



Typical Interface Circuit

Figure 6 shows an example of a typical interface circuit for the TDC1029. The analog input is AC coupled with a 1μF non polar capacitor, then offset by −0.8V with a 741 type operational amplifier and an emitter follower. System offset is adjusted via a variable resistor which alters the gain of the amplifier that provides the offset to the analog input signal. The reference voltages for the TDC1029 are both supplied by 741 type operational amplifiers configured as inverting amplifiers with emitter followers. The reference bottom is adjustable via a variable resistor to allow the system gain to be adjusted. The power supply to the TDC1029 has been regulated with an LM337 three-terminal regulator, then V_{EEA} has a ferrite bead inductor in series with the supply and a parallel bypass capacitor to ground. The purpose of the inductor is to isolate the analog supply from the noise and voltage spikes that might be present on the digital supply. The digital data that is generated by the TDC1029 is latched with a 100151 ECL latch.

Applications

The TDC1029J6 (28 lead DIP) has three additional reference resistor taps available. These may be used in a variety of ways. Below are depicted two possible applications of these taps (Figures 7 and 8). In Figure 7 the potential at the reference middle point is sensed and fed back as an offset to the input amplifier so that the input voltage is automatically offset the proper amount for accurate conversion. In Figure 8 the reference taps are driven at different potentials so that the dynamic range of the converter is similar to that of an 8-bit converter. The dynamic range is expanded because the quantization steps are not of equal size. Figure 9 is an illustration of the transfer function of the circuit in Figure 8.

Figure 7. Midpoint Feedback

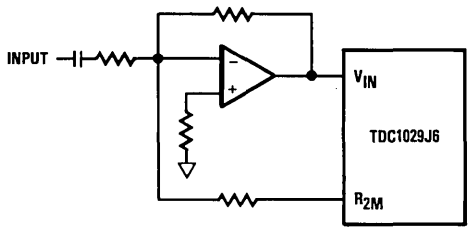


Figure 8. External Voltage Divider

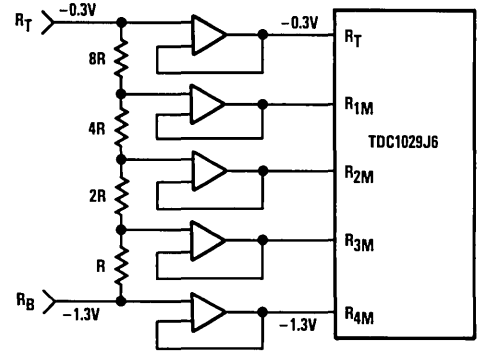
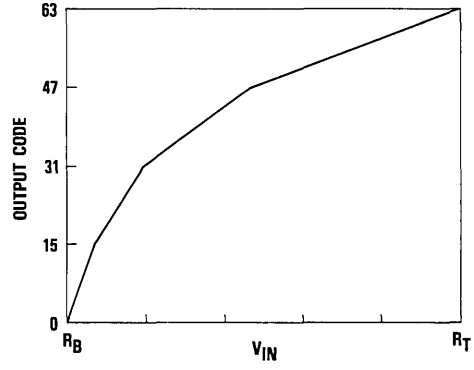


Figure 9. Piecewise Linear Transfer Function



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1029J7C	STD-T_A = 0°C to 70°C	Commercial	24 Lead DIP	1029J7C
TDC1029J7G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	24 Lead Dip	1029J7G
TDC1029J6C	STD-T_A = 0°C to 70°C	Commercial	28 Lead DIP	1029J6C
TDC1029J6G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	28 Lead DIP	1029J6G

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TDC1044
Preliminary Information

Monolithic Video A/D Converter
4-bit, 25MSPS

The TRW TDC1044 is a 25 MegaSample Per Second (MSPS) fully parallel analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 12.5MHz into 4-bit digital words. Use of a sample-and-hold circuit is not necessary for operation of the TDC1044. All digital inputs and outputs are TTL compatible.

The TDC1044 consists of 15 latching comparators, encoding logic, and an output register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

Features

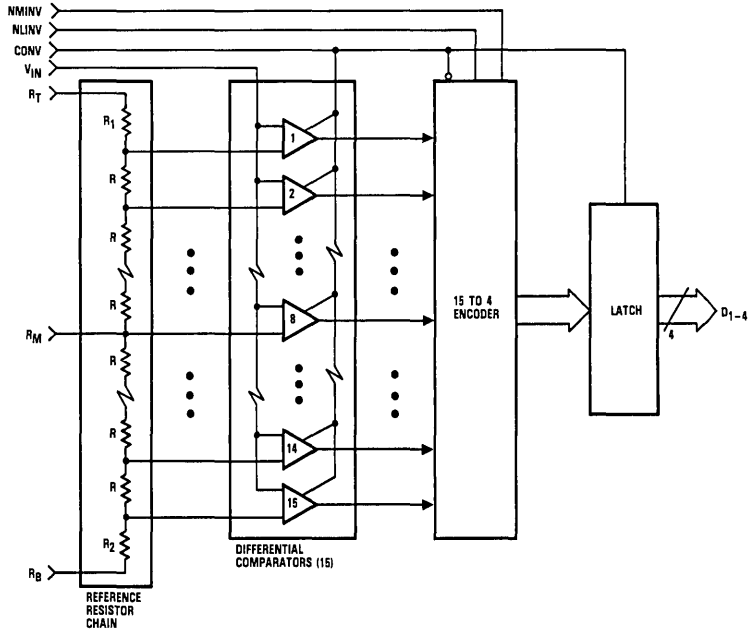
- 4-Bit Resolution
- 1/4 LSB Non-Linearity
- Sample-And-Hold Circuit Not Required
- 25MSPS Conversion Rate
- Selectable Output Format
- Available In A 16 Lead DIP

Applications

- Video Special Effects
- Radar Data Conversion
- Medical Imaging
- Image Processing

D

Functional Block Diagram



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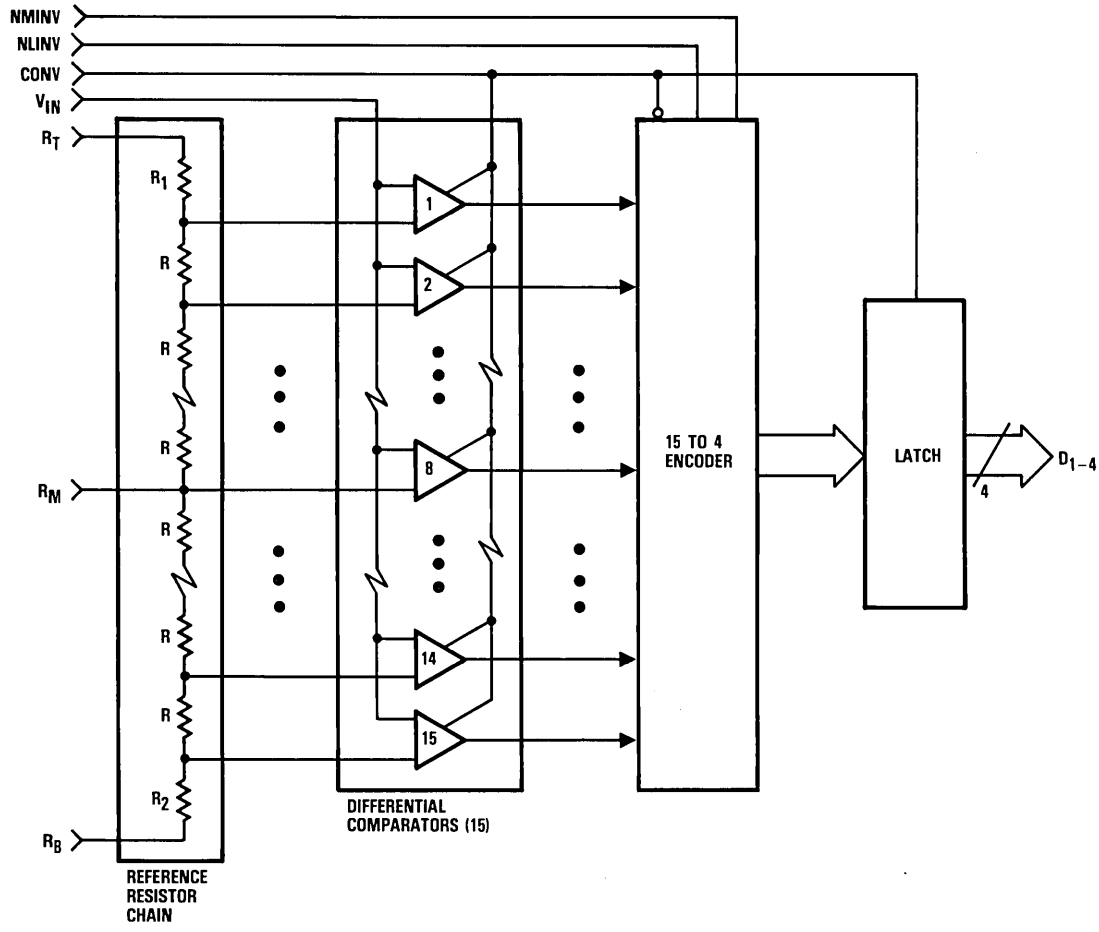
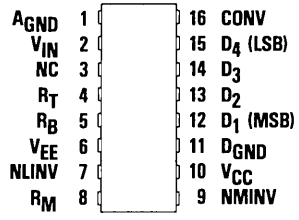
Functional Block Diagram



Pin Assignments



16 Lead DIP – J9 Package
16 Lead Plastic DIP – N9 Package

Functional Description

General Information

The TDC1044 has three functional sections: a comparator array, encoding logic, and an output register. The comparator array compares the input signal with 15 reference voltages to produce an N-of-15 code (sometimes referred to as a "thermometer" code, as all the comparators referred to voltages more positive than the input signal will be off, and those referred to voltages more negative than the input signal will be on). The encoding logic converts the N-of-15 code into binary or two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV. The output register holds the output constant between updates.

Power

The TDC1044 operates from two power supply voltages, +5.0V and -5.2V. The return for I_{CC} (the current drawn from the +5.0V supply) is D_{GND}. The return for I_{EE} (the current drawn from the -5.2V supply) is A_{GND}. All power and ground pins must be connected.

Name	Function	Value	J9, N9 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pin 10
V_{EE}	Negative Supply Voltage	-5.2V	Pin 6
D_{GND}	Digital Ground	0.0V	Pin 11
A_{GND}	Analog Ground	0.0V	Pin 1

Reference

The TDC1044 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RB}$ into digital form. V_{RB} (the voltage applied to R_B at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to R_T at the top of the reference resistor chain) should be between +0.1V and -1.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain (V_{RT} - V_{RB}) must be between 0.4V and 1.3V. The nominal voltages are V_{RT} = 0.00V and V_{RB} = -1.00V. These voltages may be varied dynamically up to 10MHz. Due to slight variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are varied dynamically (as in an Automatic Gain Control circuit), a low-impedance reference source is required. A reference middle, R_M, is also provided; this may be used as an input to adjust the mid-scale point in order to improve integral linearity. This point may also be used as a tap to supply a mid-scale voltage to offset the analog input. If V_{RM} is used as an output, it must be connected to a high input impedance device which has small input current. Noise at this point may adversely affect the performance of the device.

Name	Function	Value	J9, N9 Package
R_T	Reference Resistor Top	0.00V	Pin 4
R_M	Reference Resistor Middle	-0.5V	Pin 8
R_B	Reference Resistor Bottom	-1.00V	Pin 5

Controls

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e. steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the Output Coding Table. These pins are active LOW as signified by the prefix "N" in the signal name. They may be tied to V_{CC} for a logic "1" and D_{GND} for a logic "0."

Name	Function	Value	J9, N9 Package
NMINV	Not Most Significant Bit INVert	TTL	Pin 9
NLINV	Not Least Significant Bit INVert	TTL	Pin 7

Convert

The TDC1044 requires a CONVert (CONV) signal. A sample is taken (the comparators are latched) within t_{STO} after a rising edge of CONV. The coded result is translated to the output latches on the next rising edge. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. New data becomes valid after a maximum delay time, t_D.

Name	Function	Value	J9, N9 Package
CONV	Convert	TTL	Pin 16

Analog Input

The TDC1044 uses latching comparators which cause the input impedance to vary slightly with the signal level. For optimal performance, the source impedance of the driving circuit must be less than 25 Ohms. The input signal will not damage the device if it remains within the range of V_{EE} to +0.5V. If the input signal is at a voltage between V_{RT} and V_{RB}, the output will be a binary code between 0 and 15 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction.

Name	Function	Value	J9, N9 Package
V_{IN}	Analog Signal Input	0V to -1V	Pin 2

Outputs

The outputs of the TDC1044 are TTL compatible, and capable of driving four low-power Schottky TTL (54/74 LS) unit loads. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. Data becomes valid after a maximum delay time (t_D) after the rising edge of CONV. For optimum performance, 2.2 kOhm pull-up resistors are recommended.

Name	Function	Value	J9, N9 Package
D_1	Most Significant Bit Output	TTL	Pin 12
D_2		TTL	Pin 13
D_3		TTL	Pin 14
D_4	Least Significant Bit Output	TTL	Pin 15

No Connects

Pin 3 of the TDC1044 is labeled No Connect (NC), and has no connection to the chip. Connect this pin to A_{GND} for best noise performance.

Name	Function	Value	J9, N9 Package
NC	No Connect	A_{GND}	Pin 3

Figure 1. Timing Diagram

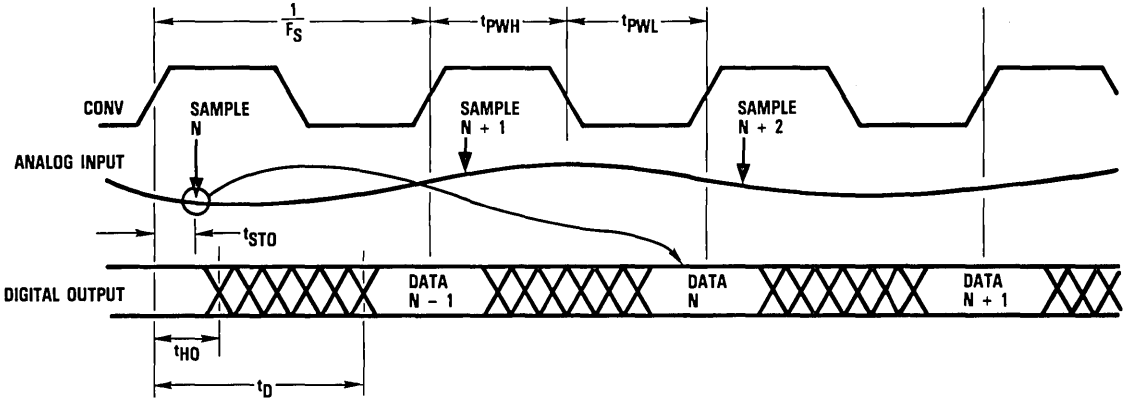
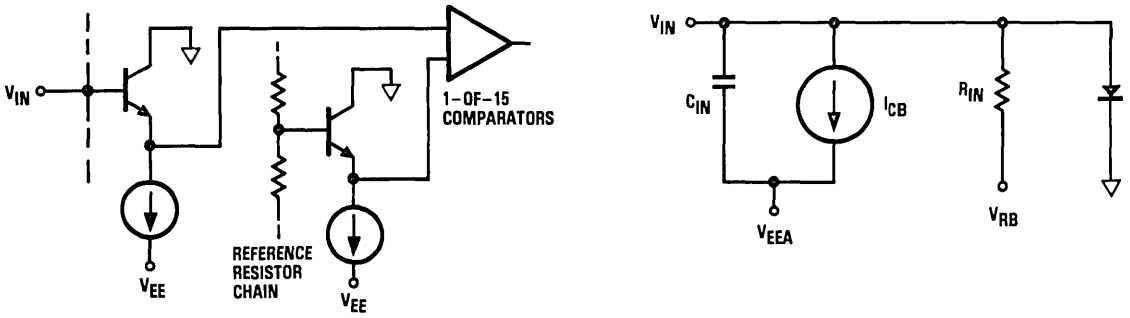


Figure 2. Simplified Analog Input Equivalent Circuit



D

Figure 3. Digital Input Equivalent Circuit

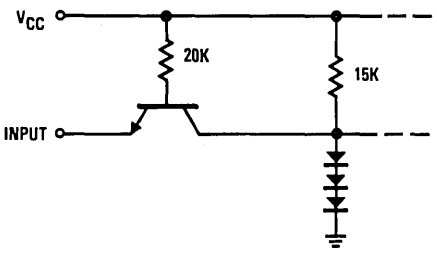
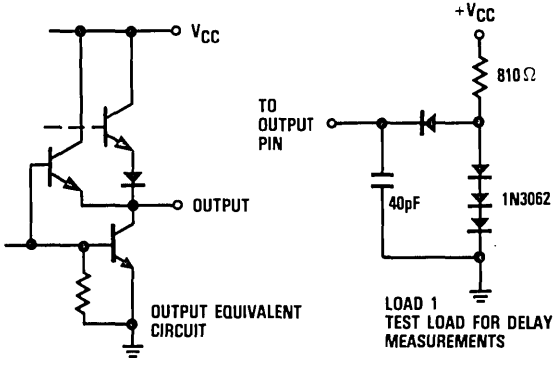


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	−0.5 to +0.5V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EE}V
V_{RT} (measured to V_{RB})	−2.2 to +2.2V

Output

Applied voltage (measured to D_{GND})	−0.5 to +5.5V [2]
Applied current, externally forced	−1.0 to +6.0mA [3,4]
Short circuit duration (single output in high state to ground)	1 sec

Temperature

Operating, ambient	−55 to +125°C
junction	+150°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{CC}	Positive Supply Voltage (Measured to D_{GND})	4.75	5.0	5.25	V
V_{EE}	Negative Supply Voltage (Measured to A_{GND})	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	17			ns
t_{PWH}	CONV Pulse Width, HIGH	17			ns
V_{IL}	Input Voltage, Logic LOW			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			V
I_{OL}	Output Current, Logic LOW			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400	μA
V_{RT}	Most Positive Reference	−1.9	0.0	0.1	V
V_{RB}	Most Negative Reference	−2.1	−1.0	−0.1	V
$V_{RT}-V_{RB}$	Reference Differential	0.2	1.0	2.0	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
I_{CC}	Positive Supply Current	V_{CC} = MAX, static[1]		25	mA
I_{EE}	Negative Supply Current	V_{EE} = MAX, static[1]			
		T_A = 0°C to 70°C		−50	mA
		T_A = 70°C		−35	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM		2	mA
R_{REF}	Total Reference Resistance		500		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}	300		kOhms
C_{IN}	Input Capacitance			25	pF
I_{CB}	Input Constant Bias Current	V_{EE} = MAX		25	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.5V CONV		−0.4	mA
		NMINV, NLINV		−0.6	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, One pin to ground, one second duration, Output HIGH.		−30	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15	pF

Note:

1. Worst case: all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

D

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
F_S	Maximum Conversion Rate	V_{CC} = MIN, V_{EE} = MIN	25		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = MIN, V_{EE} = MIN		10	ns
t_D	Digital Output Delay	V_{CC} = MIN, V_{EE} = MIN, Load 1		30	ns
t_{HO}	Digital Output Hold Time	V_{CC} = MAX, V_{EE} = MAX, Load 1	5		ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
E_{LI}	Linearity Error Integral, Independent	V_{RB} = NOM		1.6	%
E_{LD}	Linearity Error Differential			1.6	%
CS	Code Size	V_{RT}, V_{RB} = NOM	75	125	% Nominal
E_{OT}	Offset Error Top	V_{IN} = V_{RT}		+30	mV
E_{OB}	Offset Error Bottom	V_{IN} = V_{RB}		+40	mV
T_{CO}	Offset Error Temperature Coefficient			±20	μV/°C
BW	Bandwidth, Full Power Input		12.5		MHz
t_{TR}	Transient Response, Full Scale			10	ns
E_{AP}	Aperture Error			30	ps

Output Coding Table[1]

Range	Binary True	Binary Inverted	Offset Two's Complement True	Offset Two's Complement Inverted
-1.00V FS	NMINV = 1	0	0	1
	NLINV = 1	0	1	0
0.000V	0000	1111	1000	0111
-0.067V	0001	1110	1001	0110
-0.133V	0010	1101	1010	0101
-0.200V	0011	1100	1011	0100
-0.267V	0100	1011	1100	0011
-0.333V	0101	1010	1101	0010
-0.400V	0110	1001	1110	0001
-0.467V	0111	1000	1111	0000
-0.533V	1000	0111	0000	1111
-0.600V	1001	0110	0001	1110
-0.667V	1010	0101	0010	1101
-0.733V	1011	0100	0011	1100
-0.800V	1100	0011	0100	1011
-0.867V	1101	0010	0101	1010
-0.933V	1110	0001	0110	1001
-1.000V	1111	0000	0111	1000

Note:

1. Input voltages are at code centers.

Calibration

To calibrate the TDC1044, adjust V_{RT} and V_{RB} to set the 1st and 15th thresholds to the desired voltages. Assuming a 0V to −1V desired range, continuously strobe the converter with −0.0033V (1/2 LSB from 0.000V) on the analog input, and adjust V_{RT} for output toggling between codes 0000 and 0001. Then apply −0.967V (1/2 LSB from −1.000V) and adjust V_{RB} for toggling between codes 1110 and 1111. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with an amplifier offset control. R_B is a convenient point for gain adjustment that is not in the analog signal path.

Typical Interface Circuit

The TDC1044 does not require a special input buffer amplifier to drive the analog input because of its low input capacitance. A terminated low-impedance transmission line (< 100 Ohms) connected to the V_{IN} terminal of the device is sufficient if the input voltage levels match those of the A/D converter.

However, many driver circuits lack sufficient offset control, drive current, or gain stability. The Typical Interface Circuit in Figure 6 shows a simple amplifier and voltage reference circuit that may be used with the device. U2 is a wide-band operational amplifier with a gain factor of −1. A small value resistor, R12, serves to isolate the small input capacitance of the A/D converter from the amplifier output and insure frequency stability. The pulse and frequency response of the amplifier are optimized by variable capacitor C12. The reference voltage for the TDC1044 is generated by amplifier U3. System gain is adjusted by varying R9 which controls the reference voltage level to the A/D converter.

Input voltage range and input impedance for the circuit are determined by resistors R1 and R2. Formulas for calculating values for these input resistors are:

$$R1 = \frac{1}{\left(\frac{2VR}{Z_{IN}}\right) - \frac{1}{1000}}$$

and

$$R2 = Z_{IN} - \left(\frac{1000\ R1}{1000 + R1}\right)$$

where VR is the input voltage range of the circuit, Z_{IN} is the input impedance of the circuit, and the constant 1000 comes from the value of R3. As shown, the circuit is set up for 1 Volt p-p 75 Ohm video input.

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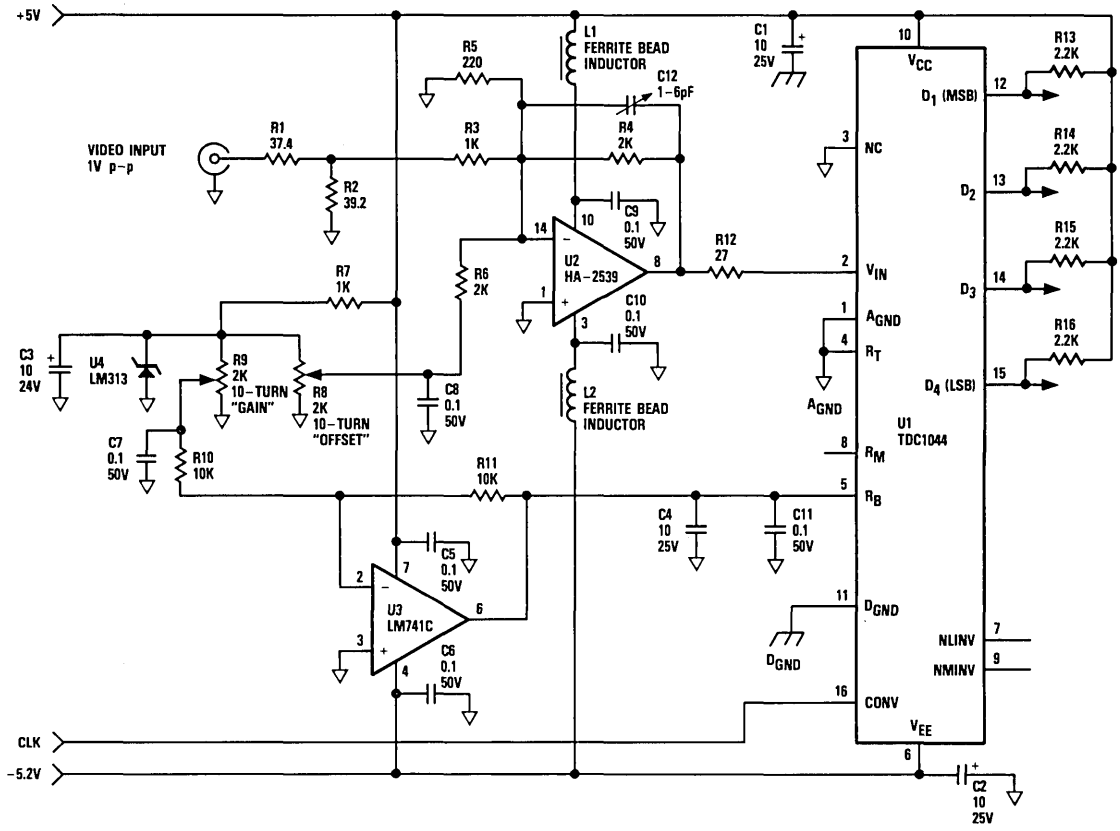
Figure 5. Typical Interface Circuit



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1044J9C	STD-T_A = 0°C to 70°C	Commercial	16 Lead DIP	1044J9C
TDC1044J9G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	16 Lead DIP	1044J9G
TDC1044N9C	STD-T_A = 0°C to 70°C	Commercial	16 Lead Plastic DIP	1044N9C

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Preliminary Information describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact TRW for current information.

TDC1046
Preliminary Information

Monolithic Video A/D Converter
6-bit, 25MSPS

The TRW TDC1046 is a 25 MegaSample Per Second (MSPS) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 12.5MHz into 6-bit digital words. Use of a sample-and-hold circuit is not necessary for operation of the TDC1046. All digital inputs and outputs are TTL compatible.

The TDC1046 consists of 63 clocked latching comparators, encoding logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

Features

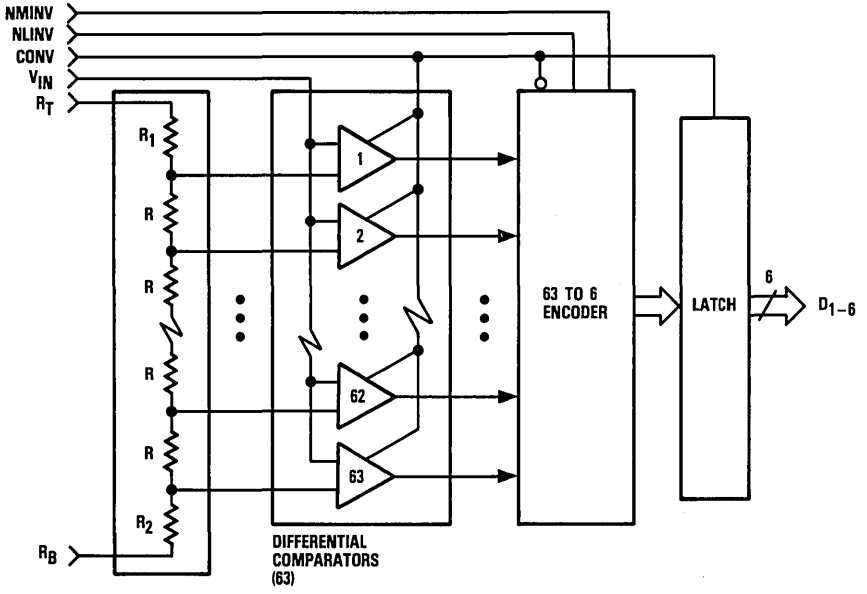
- 6-Bit Resolution
- 1/4 LSB Linearity
- Sample-And-Hold Circuit Not Required
- TTL Compatible
- 25MSPS Conversion Rate
- Selectable Output Format
- Available In An 18 Lead DIP
- Low Cost
- Low Analog Input Capacitance

Applications

- Low-Cost Video Digitizing
- Medical Imaging
- Data Acquisition
- TV Special Effects
- Video Simulators
- Radar Data Conversion

D

Functional Block Diagram



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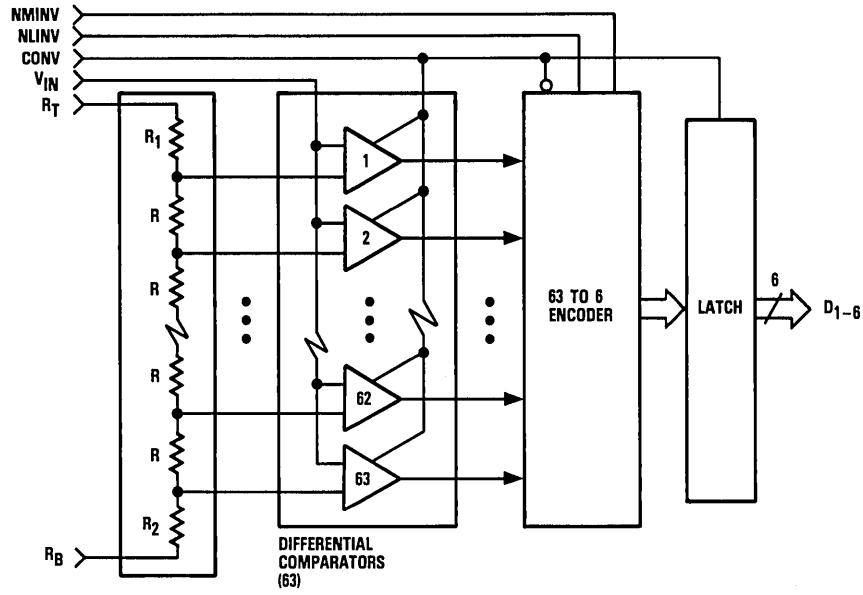
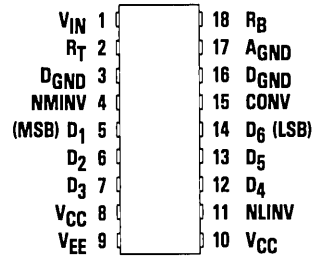
Functional Block Diagram



Pin Assignments



18 Lead DIP - J8 Package
18 Lead CERDIP - B8 Package

Functional Description

General Information

The TDC1046 has three functional sections: a comparator array, encoding logic, and output latches. The comparator array compares the input signal with 63 reference voltages to produce an N-of-63 code (sometimes referred to as a "thermometer" code, as all the comparators referred to voltages more positive than the input signal will be off, and those referred to voltages more negative than the input signal will be on). The encoding logic converts the N-of-63 code into binary or offset two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV. The output latch holds the output constant between updates.

Power

The TDC1046 operates from two supply voltages, +5.0V and −5.2V. The return for I_{CC}, the current drawn from the +5.0V supply, is D_{GND}. The return for I_{EE}, the current drawn from the −5.2V supply, is A_{GND}. All power and ground pins must be connected.

Name	Function	Value	J8, B8 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pins 8, 10
V_{EE}	Negative Supply Voltage	−5.2V	Pin 9
D_{GND}	Digital Ground	0.0V	Pins 3, 16
A_{GND}	Analog Ground	0.0V	Pin 17

Reference

The TDC1046 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. V_{RB} (the voltage applied to R_B at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to R_T at the top of the reference resistor chain) should be between +0.1V and −1.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain ($V_{RT} - V_{RB}$) must be between 0.8V and 1.2V. The nominal voltages are V_{RT} = 0.00V and V_{RB} = −1.00V. These voltages may be varied dynamically up to 12.5MHz. Due to variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically (as in an Automatic Gain Control circuit), a low-impedance reference source is required.

Name	Function	Value	J8, B8 Package
V_{RT}	Reference Resistor (Top)	0.00V	Pin 2
V_{RB}	Reference Resistor (Bottom)	−1.00V	Pin 18

Controls

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e. steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the Output Coding Table. These pins are active LOW as signified by the prefix "N" in the signal name. They may be tied to V_{CC} for a logic "1" and D_{GND} for a logic "0."

Name	Function	Value	J8, B8 Package
NMINV	Not Most Significant Bit INVert	TTL	Pin 4
NLINV	Not Least Significant Bit INVert	TTL	Pin 11

Convert

The TDC1046 requires a CONVert (CONV) signal. A sample is taken (the comparators are latched) within 5ns (t_{STO}) after a rising edge on the CONV pin. This time is t_{STO}, Sampling Time Offset. The 63 to 6 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output latches on the next rising edge. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal.

Name	Function	Value	J8, B8 Package
CONV	Convert	TTL	Pin 15

Analog Input

The TDC1046 uses strobed latching comparators which cause the input impedance to vary with the signal level, as comparator input transistors are cut-off or become active. For optimal performance, the source impedance of the driving circuit must be less than 50 Ohms. The input signal will not damage the TDC1046 if it remains within the range of V_{EE} to +0.5V. If the input signal is at a voltage between V_{RT} and V_{RB}, the output will be a binary number between 0 and 63 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction.

Name	Function	Value	J8, B8 Package
V_{IN}	Analog Signal Input	0V to -1V	Pin 1

Outputs

The outputs of the TDC1046 are TTL compatible, and capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. Data is guaranteed to be valid after a maximum delay time (t_D) after the rising edge of CONV. For optimum performance, 2.2 kOhm pull-up resistors are recommended.

Name	Function	Value	J8, B8 Package
D_1	MSB Output	TTL	Pin 5
D_2		TTL	Pin 6
D_3		TTL	Pin 7
D_4		TTL	Pin 12
D_5		TTL	Pin 13
D_6	LSB Output	TTL	Pin 14

Figure 1. Timing Diagram

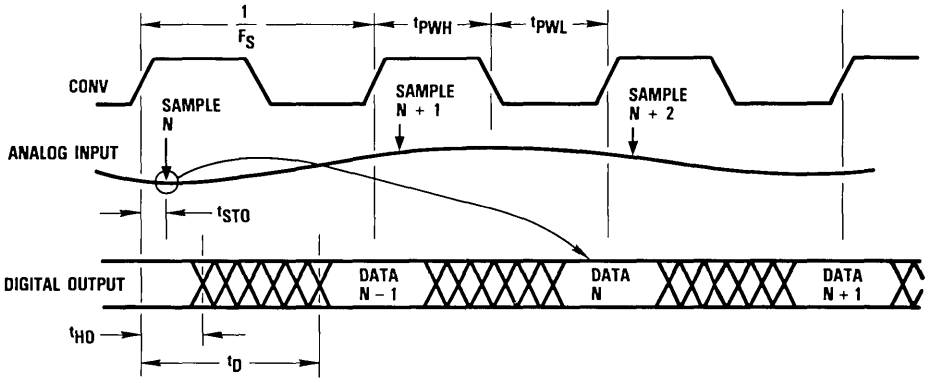


Figure 2. Simplified Analog Input Equivalent Circuit

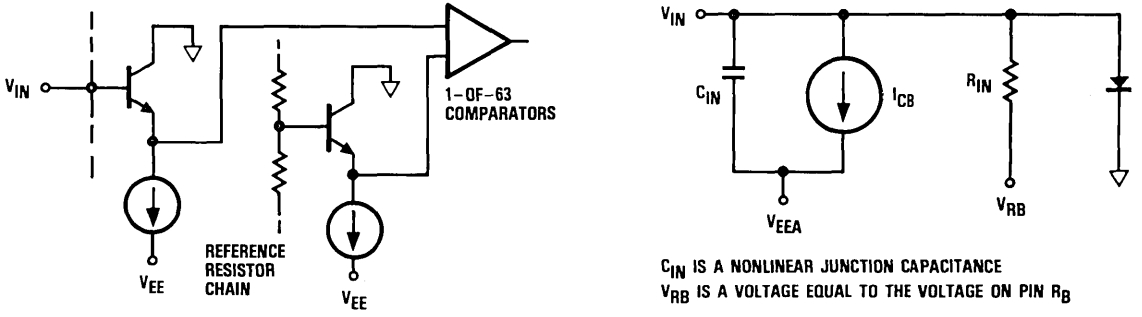


Figure 3. Digital Input Equivalent Circuit

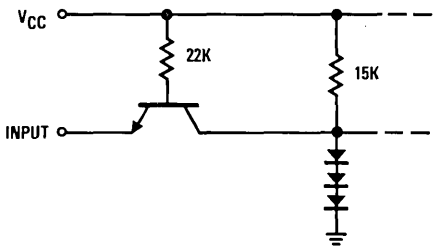
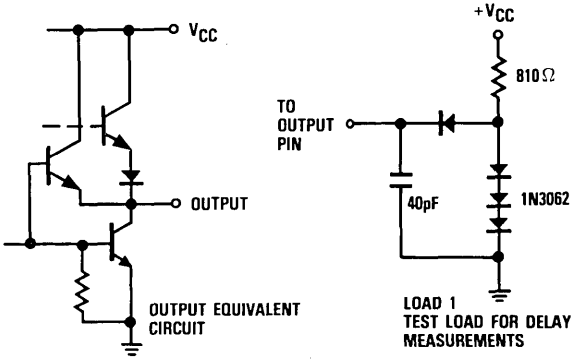


Figure 4. Output Circuits



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Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	−0.5 to +0.5V

Input voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EE}
V_{RT} (measured to V_{RB})	+1.2 to −1.2V

Output

Applied voltage (measured to D_{GND})	−0.5 to 5.5V [2]
Applied current, externally forced	−1.0 to 6.0mA [3,4]
Short circuit duration (single output in high state to ground)	1 sec

Temperature

Operating, case	−55 to +125°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Nom	Max	Units
V_{CC}	Positive Supply Voltage (measured to D_{GND})	4.75	5.0	5.25	V
V_{EE}	Negative Supply Voltage (measured to A_{GND})	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width (LOW)	15			ns
t_{PWH}	CONV Pulse Width (HIGH)	17			ns
V_{IL}	Input Voltage, Logic LOW			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			V
I_{OL}	Output Current, Logic LOW			4.0	mA
I_{OH}	Output Current, Logic HIGH			−0.4	mA
V_{RT}	Most Positive Reference Input [1]	−0.1	0.0	0.1	V
V_{RB}	Most Negative Reference Input [1]	−0.9	−1.0	−1.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	0.8		1.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70	°C

Note:

1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
I_{CC}	Positive Supply Current	V_{CC} = MAX, static[1]		20	mA
I_{EE}	Negative Supply Current	V_{EE} = MAX, static[1]			
		T_A = 0°C to 70°C		−95	mA
		T_A = 70°C		−75	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM		10	mA
R_{REF}	Total Reference Resistance	V_{RT} − V_{RB} = MAX	120		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}	150		kOhms
C_{IN}	Input Capacitance			30	pF
I_{CB}	Input Constant Bias Current	V_{EE} = MAX		75	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.5V CONV		−0.4	mA
		NMINV, NLINV		−0.6	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, One pin to ground, one second duration, output HIGH		−30	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15	pF

Note:
1. Worst Case: All digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

D

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
F_S	Maximum Conversion Rate	V_{CC} = MIN, V_{EE} = MIN	25		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = MIN, V_{EE} = MIN		5	ns
t_D	Output Delay	V_{CC} = MIN, V_{EE} = MIN, Load 1		25	ns
t_{HO}	Output Hold Time	V_{CC} = MAX, V_{EE} = MAX, Load 1	5		ns

System performance characteristics within specified operating conditions

Parameter			Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
E_{LI}	Linearity Error	Integral, Independent	V_{RT}, V_{RB} = NOM		0.4	%
E_{LD}	Linearity Error	Differential			0.4	%
CS	Code Size		V_{RT}, V_{RB} = NOM	50	150	% Nominal
E_{OT}	Offset Error	Top	V_{IN} = V_{RT}		+50	mV
E_{OB}	Offset Error	Bottom	V_{IN} = V_{RB}		−30	mV
T_{CO}	Temperature Coefficient (Offset Voltage)				±20	μV/°C
BW	Bandwidth, Full Power Input			12.5		MHz
t_{TR}	Transient Response, Full Scale				10	ns
SNR	Signal-to-Noise Ratio		12.5MHz Bandwidth, 25MSPS Conversion Rate			
		Peak Signal/RMS Noise	1MHz Input	42		dB
			12.5MHz Input	40		dB
		RMS Signal/RMS Noise	1MHz Input	33		dB
			12.5MHz Input	31		dB
E_{AP}	Aperture Error				30	ps

Output Coding Table[1]

Range	Binary True	Binary Inverted	Two's Complement True	Two's Complement Inverted
	NMINV = 1	0	0	1
15.8730 mV STEP	NLINV = 1	0	1	0
0.0000V	000000	111111	100000	011111
−0.0159V	000001	111110	100001	011110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−0.4921V	011111	100000	111111	000000
−0.5079V	100000	011111	000000	111111
−0.5238V	100001	011110	000001	111110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−0.9841V	111110	000001	011110	100001
−1.000V	111111	000000	011111	100000

Note:

1. Voltages are code midpoints when calibrated (see Calibration section).

Calibration

To calibrate the TDC1046, adjust V_{RT} and V_{RB} to set the 1st and 63rd thresholds to the desired voltages. In the Block Diagram, note that R_1 is greater than R, ensuring calibration with a positive voltage on R_T. Assuming a 0V to −1V desired range, continuously strobe the converter with −0.0079V on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −0.9921V and adjust V_{RB} for toggling between codes 62 and 63. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with a buffer offset control. R_B is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in Figure 5.

Typical Interface Circuit

The TDC1046 does not require a special input buffer amplifier to drive the analog input because of its low analog input capacitance. A terminated low-impedance transmission line (< 100 Ohms) connected to the V_{IN} terminals of the TDC1046 is sufficient if the input voltage levels match those of the A/D converter.

However, many driver circuits lack sufficient offset control, drive current, or gain control. The Typical Interface Circuit in Figure 6 shows a simple buffer amplifier and voltage reference circuit that may be used with the TDC1046. U2 is a wide-band operational amplifier with a gain factor of −2. A small value resistor, R12, serves to help isolate the input capacitance of the A/D converter from the amplifier output and insure frequency stability. The pulse and frequency response of the buffer amplifier are optimized by variable capacitor C12.

The reference voltage for the TDC1046 is generated by amplifier U3 and PNP transistor Q1 which supplies the reference current. System gain is adjusted by varying R9 which controls the reference voltage level to the A/D converter.

Input voltage range and input impedance for the circuit are determined by resistors R1 and R2. Formulas for calculating values for these input resistors are:

$$R1 = \frac{1}{\left(\frac{2VR}{Z_{IN}}\right) - \frac{1}{1000}}$$

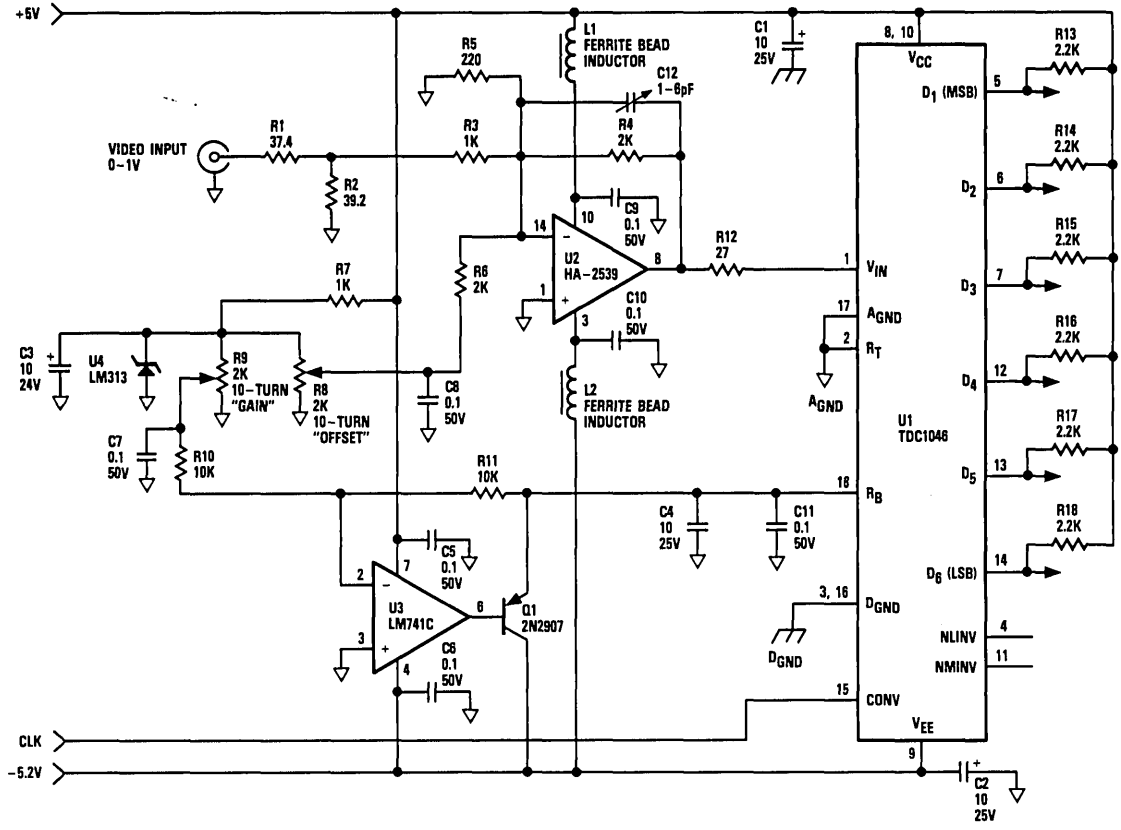
and

$$R2 = Z_{IN} - \left(\frac{1000\ R1}{1000 + R1}\right)$$

where VR is the input voltage range of the circuit, Z_{IN} is the input impedance of the circuit, and the constant 1000 comes from the value of R3. As shown, the circuit is set up for 1 Volt p-p 75 Ohm video input.

D

Figure 5. Typical Interface Circuit



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1046J8C	STD - T_A = 0°C to 70°C	Commercial	18 Lead DIP	1046J8C
TDC1046J8G	STD - T_A = 0°C to 70°C	Commercial With Burn-In	18 Lead DIP	1046J8G
TDC1046B8C	STD - T_A = 0°C to 70°C	Commercial	18 Lead CERDIP	1046B8C
TDC1046B8G	STD - T_A = 0°C to 70°C	Commercial With Burn-In	18 Lead CERDIP	1046B8G

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TDC1047
Preliminary Information

Monolithic Video A/D Converter
7-bit, 20MSPS

The TRW TDC1047 is a 20 MegaSample Per Second (MSPS) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 7MHz into 7-bit digital words. A sample-and-hold circuit is not necessary. All digital inputs and outputs are TTL compatible.

The TDC1047 consists of 127 clocked latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

The TDC1047 is pin and function compatible with TRW's TDC1027, and offers increased performance with lower power dissipation.

Features

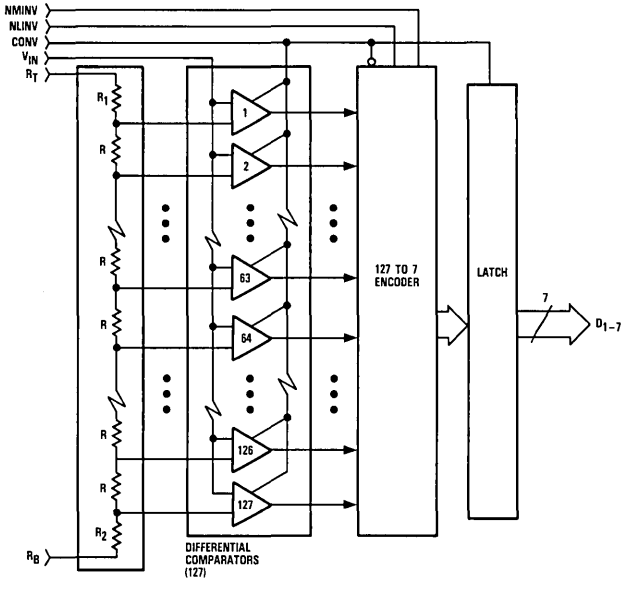
- 7-Bit Resolution
- 1/2 LSB Linearity
- Sample-And-Hold Circuit Not Required
- 20MSPS Conversion Rate
- Selectable Output Format
- Available In 24 Lead DIP Or CERDIP
- Evaluation Board - TDC1047E1C

Applications

- Low-Cost Video Digitizing
- Medical Imaging
- TV Special Effects
- Video Simulators
- Radar Data Conversion

D

Functional Block Diagram



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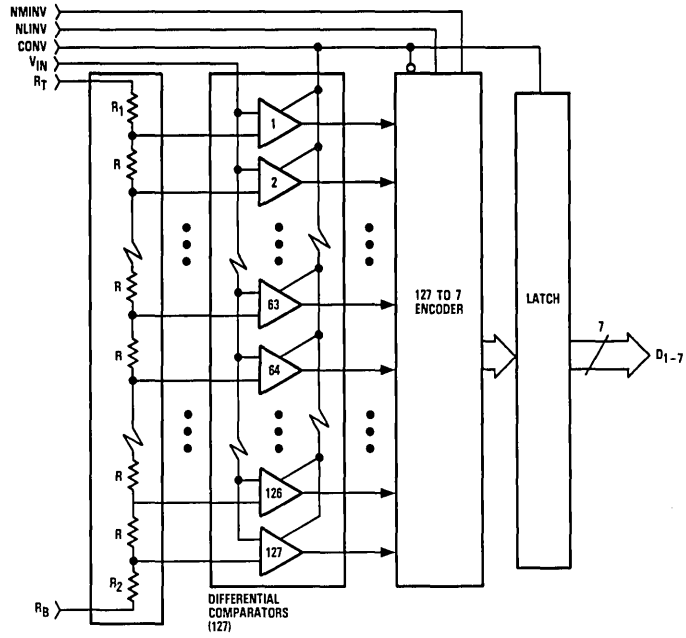
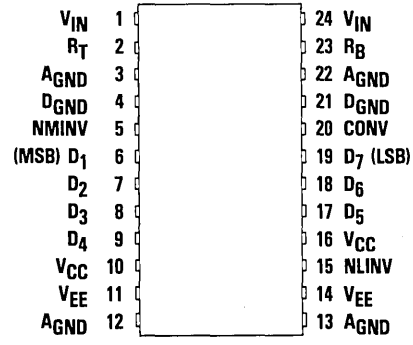
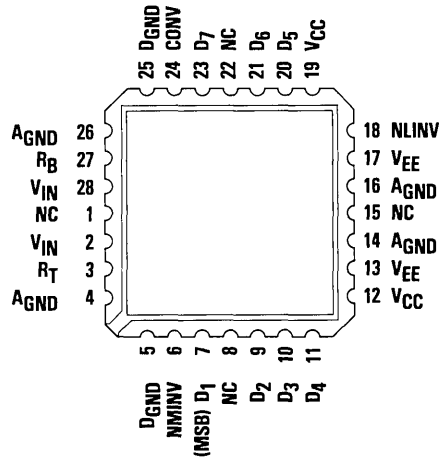
Functional Block Diagram



Pin Assignments



24 Lead DIP – J7 Package
24 Lead CERDIP – B7 Package



28 Contact Chip Carrier – C3 Package

Functional Description

General Information

The TDC1047 has three functional sections: a comparator array, encoding logic, and output latches. The comparator array compares the input signal with 127 reference voltages to produce an N-of-127 code (sometimes referred to as a "thermometer" code, as all the comparators referred to voltages more positive than the input signal will be off, and those referred to voltages more negative than the input signal will be on). The encoding logic converts the N-of-127 code into binary or offset two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV. The output latch holds the output constant between updates.

Power

The TDC1047 operates from two supply voltages, +5.0V and -5.2V. The return for I_{CC}, the current drawn from the +5.0V supply, is D_{GND}. The return for I_{EE}, the current drawn from the -5.2V supply, is A_{GND}. All power and ground pins must be connected.

Name	Function	Value	J7, B7 Package	C3 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pins 10, 16	Pin 12
V_{EE}	Negative Supply Voltage	-5.2V	Pins 11, 14	Pins 13, 17
D_{GND}	Digital Ground	0.0V	Pins 4, 21	Pins 5, 25
A_{GND}	Analog Ground	0.0V	Pins 3, 12, 13, 22	Pins 4, 14, 16, 26

Reference

The TDC1047 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between +0.1V and -1.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain ($V_{RT} - V_{RB}$) must be between 0.8V and 1.2V. The nominal voltages are V_{RT} = 0.00V and V_{RB} = -1.00V. These voltages may be varied dynamically up to 7MHz. Due to variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically as in an Automatic Gain Control (AGC) circuit, a low-impedance reference source is recommended.

Name	Function	Value	J7, B7 Package	C3 Package
R_T	Reference Resistor (Top)	0.00V	Pin 2	Pin 3
R_B	Reference Resistor (Bottom)	-1.00V	Pin 23	Pin 27

Controls

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e. steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the output coding table. These pins are active LOW as signified by the prefix "N" in the signal name. They may be tied to V_{CC} for a logic "1" and D_{GND} for a logic "0."

Name	Function	Value	J7, B7 Package	C3 Package
NMINV	Not Most Significant Bit INVert	TTL	Pin 5	Pin 6
NLINV	Not Least Significant Bit INVert	TTL	Pin 15	Pin 18

Convert

The TDC1047 requires a CONVert (CONV) signal. A sample is taken (the comparators are latched) within the Sampling Time Offset (t_{STO}) of a rising edge on the CONV pin. The 127 to 7 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output latches on the next rising edge. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. This permits the previous conversion result to be acquired by external circuitry at that rising edge, i.e. data for sample N is acquired by the external circuitry while the TDC1047 is taking input sample N + 2.

Name	Function	Value	J7, B7 Package	C3 Package
CONV	Convert	TTL	Pin 20	Pin 24

Analog Input

The TDC1047 uses strobed latching comparators which cause the input impedance to vary with the signal level, as comparator input transistors are cut-off or become active. For optimal performance, both V_{IN} pins must be used and the source impedance of the driving circuit must be less than 30 Ohms. The input signal will not damage the TDC1047 if it remains within the range of V_{EE} to +0.5V. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number between 0 and 127 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction.

Name	Function	Value	J7, B7 Package	C3 Package
V_{IN}	Analog Signal Input	0V to -1V	Pins 1, 24	Pins 2, 28

Outputs

The outputs of the TDC1047 are TTL compatible, and capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. For optimum performance, 2.2 kOhm pull-up resistors are recommended.

Name	Function	Value	J7, B7 Package	C3 Package
D_1	MSB Output	TTL	Pin 6	Pin 7
D_2		TTL	Pin 7	Pin 9
D_3		TTL	Pin 8	Pin 10
D_4		TTL	Pin 9	Pin 11
D_5		TTL	Pin 17	Pin 20
D_6		TTL	Pin 18	Pin 21
D_7	LSB Output	TTL	Pin 19	Pin 23

Figure 1. Timing Diagram

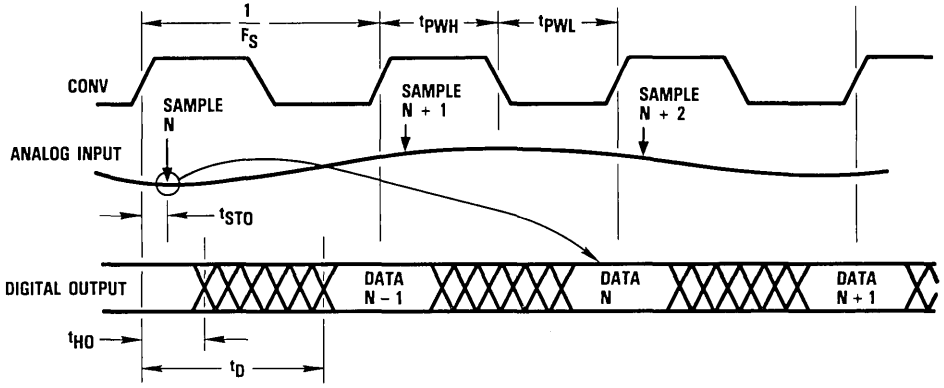
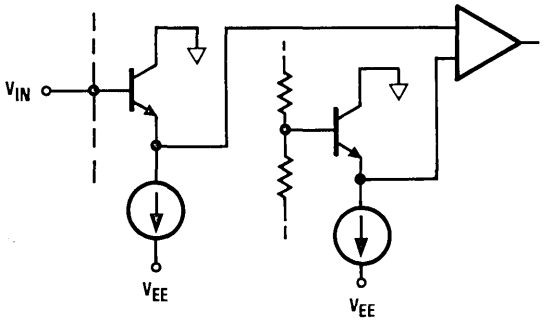
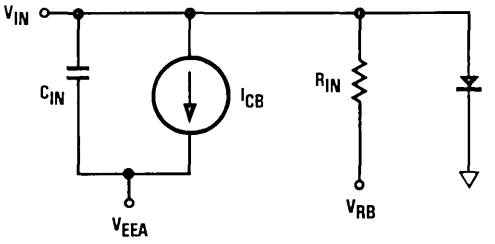


Figure 2. Simplified Analog Input Equivalent Circuit





C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

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Figure 3. Digital Input Equivalent Circuit

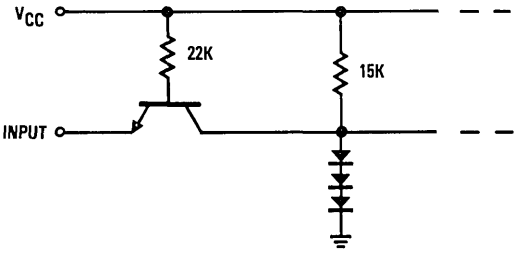
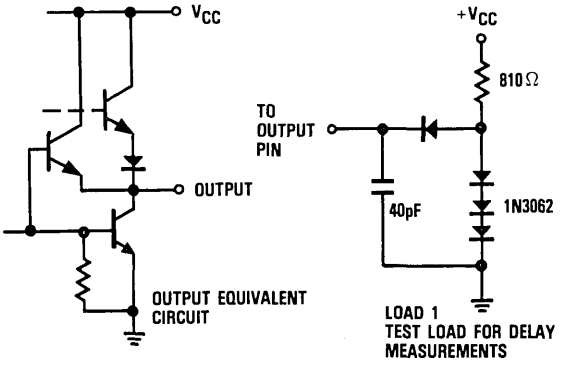


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device will be damaged)[1]

Supply Voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	−0.5 to +0.5V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EE}
V_{RT} (measured to V_{RB})	+2.2 to −2.2V

Output

Applied voltage (measured to D_{GND})	−0.5 to 5.5V[2]
Applied current, externally forced	−1.0 to 6.0mA[3,4]
Short circuit duration (single output in high state to ground)	1 sec

Temperature

Operating, case	−55 to + 125°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Nom	Max	Units
V_{CC}	Positive Supply Voltage (measured to D_{GND})	4.75	5.0	5.25	V
V_{EE}	Negative Supply Voltage (measured to A_{GND})	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	14			ns
t_{PWH}	CONV Pulse Width, HIGH	14			ns
V_{IL}	Input Voltage, Logic LOW			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			V
I_{OL}	Output Current, Logic LOW			4.0	mA
I_{OH}	Output Current, Logic HIGH			−0.4	mA
V_{RT}	Most Positive Reference Input[1]	−0.1	0.00	0.1	V
V_{RB}	Most Negative Reference Input[1]	−0.9	−1.00	−1.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	0.8	1.0	1.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70	°C

Note:

1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
I_{CC}	Positive Supply Current	V_{CC} = MAX, static[1]		25	mA
I_{EE}	Negative Supply Current	V_{EE} = MAX, static[1]			
		T_A = 0°C to 70°C		−170	mA
		T_A = 70°C		−135	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM		35	mA
R_{REF}	Total Reference Resistance		28		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}	100		kOhms
C_{IN}	Input Capacitance			60	pF
I_{CB}	Input Constant Bias Current	V_{EE} = MAX		150	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.5V CONV		−0.4	mA
		NMINV, NLINV		−0.6	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, Output HIGH, one pin to ground, one second duration.		−30	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15	pF

Note:
1. Worst Case: All digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

D

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
F_S	Maximum Conversion Rate	V_{CC} = MIN, V_{EE} = MIN	20		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = MIN, V_{EE} = MIN		7	ns
t_D	Output Delay	V_{CC} = MIN, V_{EE} = MIN, Load 1		30	ns
t_{HO}	Output Hold Time	V_{CC} = MAX, V_{EE} = MAX, Load 1	5		ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB} = NOM		0.4	%
E_{LD}	Linearity Error Differential			0.4	%
CS	Code Size	V_{RT}, V_{RB} = NOM	30	170	% Nominal
V_{OT}	Offset Voltage Top	V_{IN} = V_{RT}		+50	mV
V_{OB}	Offset Voltage Bottom	V_{IN} = V_{RB}		−30	mV
T_{CO}	Temperature Coefficient			±20	µV/°C
BW	Bandwidth, Full Power Input		7		MHz
t_{TR}	Transient Response, Full Scale			10	ns
SNR	Signal-to-Noise Ratio	7MHz Bandwith, 20MSPS Conversion Rate			
	Peak Signal/RMS Noise	1MHz Input	48		dB
		7MHz Input	46		dB
	RMS Signal/RMS Noise	1MHz Input	39		dB
		7MHz Input	37		dB
E_{AP}	Aperture Error			50	ps
DP	Differential Phase Error[1]	F_S = 4 × NTSC		1.5	Degree
DG	Differential Gain Error[1]	F_S = 4 × NTSC		2.5	%

Note:

1. In excess of quantization.

Output Coding

Step	Range	Binary True	Binary Inverted	Offset Two's Complement True	Offset Two's Complement Inverted
	−1.0000V FS	NMINV = 1	0	0	1
	7.874mV STEP	NLINV = 1	0	1	0
000	0.0000V	0000000	1111111	1000000	0111111
001	−0.0078V	0000001	1111110	1000001	0111110
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
063	−0.4960V	0011111	1100000	1011111	0100000
064	−0.5039V	0100000	1011111	1100000	0011111
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
126	−1.9921V	1111110	0000001	0111110	1000001
127	−1.0000V	1111111	0000000	0111111	1000000

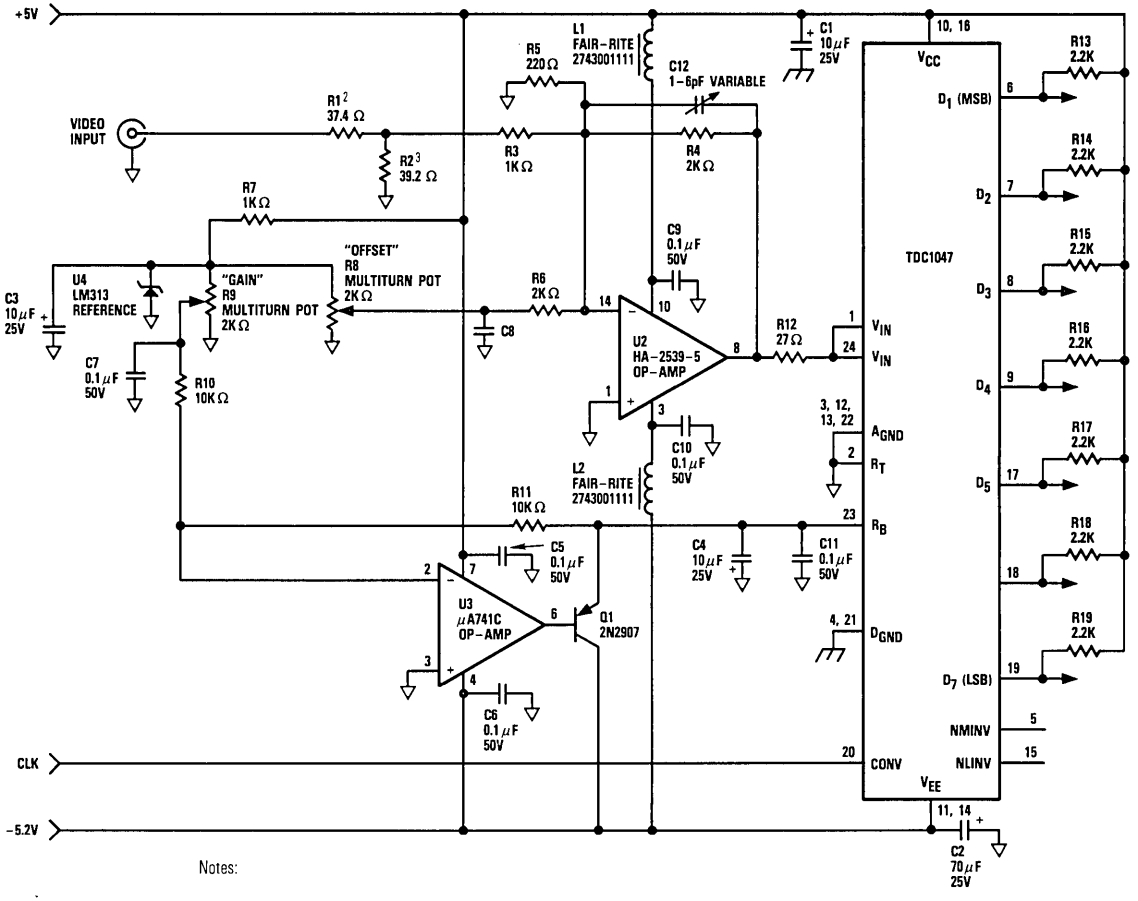
Note:

1. Voltages are code midpoints when calibrated (see Calibration Section).

Calibration

To calibrate the TDC1047, adjust V_{RT} and V_{RB} to set the 1st and 127th thresholds to the desired voltages in the block diagram. Note that R_1 is greater than R, ensuring calibration with a positive voltage on R_T. Assuming a 0V to −1V desired range, continuously strobe the converter with −0.0039V on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −0.9961V and adjust V_{RB} for toggling between codes 126 and 127. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with a buffer offset control. R_B is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in Figure 5.

Figure 5. Typical Interface Circuit



Notes:

1. Unless otherwise specified, all resistors are 1/4W, 2%.
2. $R1 = Z_{IN} - \left(\frac{1000\ R2}{1000 + R2}\right)$
3. $R2 = \frac{1}{\left(\frac{2V_{Range}}{V_{REF}\ Z_{IN}}\right) - 0.001}$

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1047J7C	STD-T_A = 0°C to 70°C	Commercial	24 Lead DIP	1047J7C
TDC1047J7G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	24 Lead DIP	1047J7G
TDC1047B7C	STD-T_A = 0°C to 70°C	Commercial	24 Lead CERDIP	1047B7C
TDC1047B7G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	24 Lead CERDIP	1047B7G
TDC1047C3C	STD-T_A = 0°C to 70°C	Commercial	28 Contact Chip Carrier	1047C3C
TDC1047C3G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	28 Contact Chip Carrier	1047C3G

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TDC1048

Monolithic Video A/D Converter
8-bit, 20MSPS

The TRW TDC1048 is a 20 MegaSample Per Second (MSPS) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 7MHz into 8-bit digital words. A sample-and-hold circuit is not necessary. Low power consumption eases thermal considerations, and board space is minimized with a 28 lead package. All digital inputs and outputs are TTL compatible.

The TDC1048 consists of 255 clocked latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

Features

- 8-Bit Resolution
- 20MSPS Conversion Rate
- Low Power Consumption, 1.6W (Worst Case)
- Sample-And-Hold Circuit Not Required
- Differential Phase 1 Degree
- Differential Gain 2%
- 1/2 LSB Linearity
- TTL Compatible
- Selectable Output Format
- Available In 28 Lead DIP, CERDIP, Or Contact Chip Carrier
- Evaluation Board - TDC1048E1C

Applications

- Low-Cost Video Digitizing
- Radar Data Conversion
- Data Acquisition
- Medical Imaging

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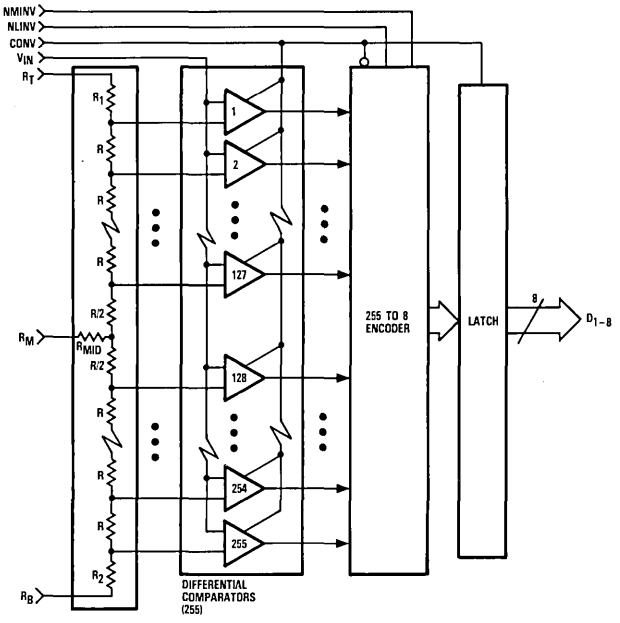
Functional Block Diagram



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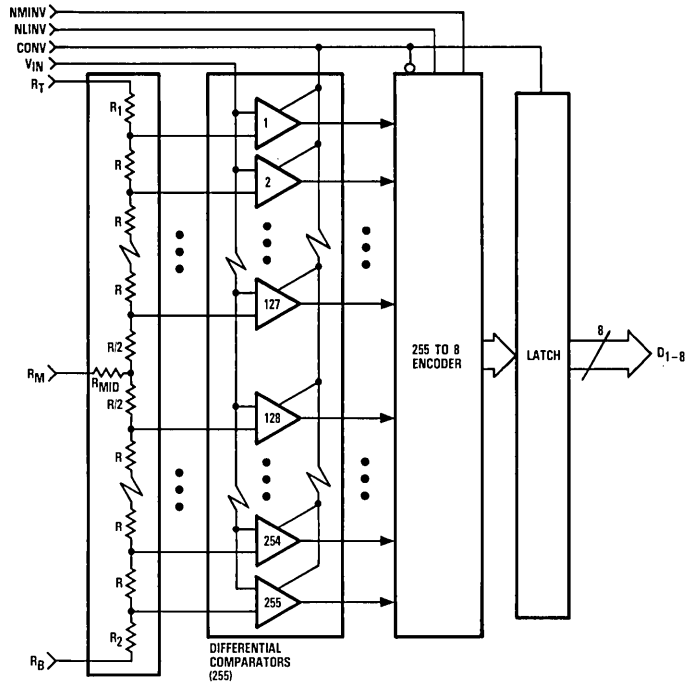
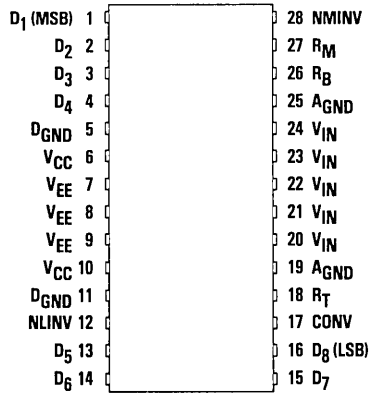
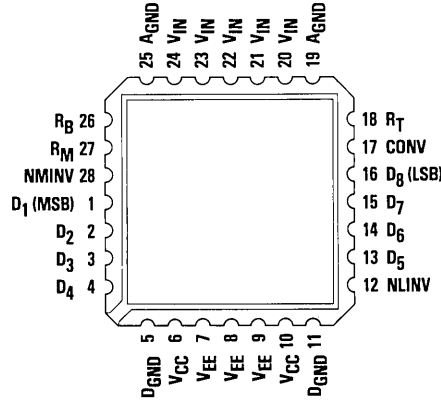


Pin Assignments



28 Lead DIP – J6 Package
28 Lead CERDIP – B6 Package



28 Contact Chip Carrier – C3 Package

Functional Description

General Information

The TDC1048 has three functional sections: a comparator array, encoding logic, and output latches. The comparator array compares the input signal with 255 reference voltages to produce an N-of-255 code (sometimes referred to as a "thermometer" code, as all the comparators below the signal will be on, and all those above the signal will be off). The encoding logic converts the N-of-255 code into binary or offset two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV. The output latch holds the output constant between updates.

Power

The TDC1048 operates from two supply voltages, +5.0V and -5.2V. The return for I_{CC}, the current drawn from the +5.0V supply, is D_{GND}. The return for I_{EE}, the current drawn from the -5.2V supply, is A_{GND}. All power and ground pins must be connected.

Name	Function	Value	J6, B6, C3 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pins 6, 10
V_{EE}	Negative Supply Voltage	-5.2V	Pins 7, 8, 9
D_{GND}	Digital Ground	0.0V	Pins 5, 11
A_{GND}	Analog Ground	0.0V	Pins 19, 25

Reference

The TDC1048 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between +0.1V and -2.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain ($V_{RT}-V_{RB}$) must be between 1.8V and 2.2V. The nominal voltages are V_{RT} = 0.0V, V_{RB} = -2.0V.

A midpoint tap, R_M, allows the converter to be adjusted for optimum linearity, although adjustment is not necessary to meet the linearity specification. It can also be used to achieve a nonlinear transfer function. The circuit shown in Figure 5 will provide approximately 1/2 LSB adjustment of the linearity midpoint. The characteristic impedance seen at this node is approximately 220 Ohms, and should be driven from a low-impedance source. Note that any load applied to this node will affect linearity, and noise introduced at this point will degrade the quantization process.

Due to the variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically, (as in an automatic gain control circuit), a low-impedance reference source is required. The reference voltages may be varied dynamically up to 5MHz.

Name	Function	Value	J6, B6, C3 Package
R_T	Reference Resistor (Top)	0.0V	Pin 18
R_M	Reference Resistor (Middle)	-1.0V	Pin 27
R_B	Reference Resistor (Bottom)	-2.0V	Pin 26

D

Control

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e. steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the Output Coding table on page 121. These pins are active LOW, as signified by the prefix "N" in the signal name. They may be tied to V_{CC} for a logic "1" and D_{GND} for a logic "0."

Name	Function	Value	J6, B6, C3 Package
NMINV	Not Most Significant Bit INVert	TTL	Pin 28
NLINV	Not Least Significant Bit INVert	TTL	Pin 12

Convert

The TDC1048 requires a convert (CONV) signal. A sample is taken (the comparators are latched) within 15ns after a rising edge on the CONV pin. This time is t_{STO}, Sampling Time Offset. This delay varies by a few nanoseconds from part to part and as a function of temperature, but the short-term uncertainty (jitter) in sampling offset time is less than 100 picoseconds. The 255 to 8 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output latches on the next rising edge. Data is held valid at the output register for at least t_{HO}, Output Hold Time, after the rising edge of CONV. New data becomes valid after a Digital Output Delay, t_D, time. This permits the previous conversion result to be acquired by external circuitry at that rising edge, i.e. data for sample N is acquired by the external circuitry while the TDC1048 is taking input sample N + 2.

Name	Function	Value	J6, B6, C3 Package
CONV	Convert	TTL	Pin 17

Analog Input

The TDC1048 uses strobed latching comparators which cause the input impedance to vary with the signal level, as comparator input transistors are cut-off or become active. As a result, for optimal performance, the source impedance of the driving device must be less than 25 Ohms. The input signal will not damage the TDC1048 if it remains within the range of V_{EE} to +0.5V. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number between 0 and 255 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction. All five analog input pins must be connected together.

Name	Function	Value	J6, B6, C3 Package
V_{IN}	Analog Signal Input	0V to -2V	Pins 20, 21, 22, 23, 24

Outputs

The outputs of the TDC1048 are TTL compatible, capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONVert signal. For optimum performance, 2.2 kOhm pull-up resistors are recommended.

Name	Function	Value	J6, B6, C3 Package
D_1	MSB Output	TTL	Pin 1
D_2		TTL	Pin 2
D_3		TTL	Pin 3
D_4		TTL	Pin 4
D_5		TTL	Pin 13
D_6		TTL	Pin 14
D_7		TTL	Pin 15
D_8	LSB Output	TTL	Pin 16

Figure 1. Timing Diagram

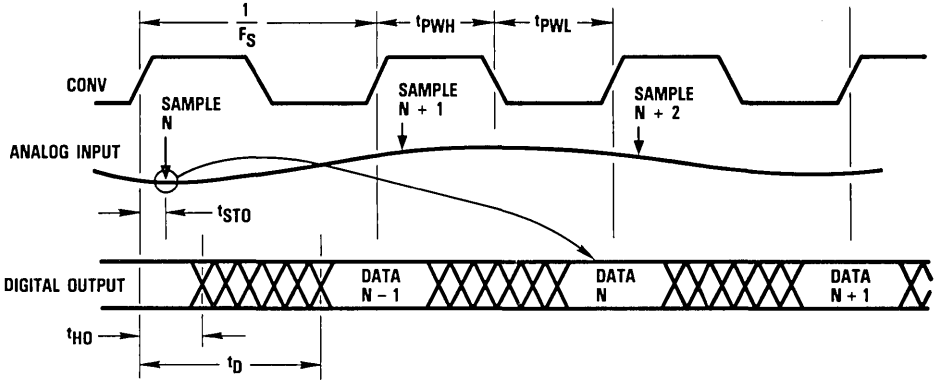


Figure 2. Simplified Analog Input Equivalent Circuit

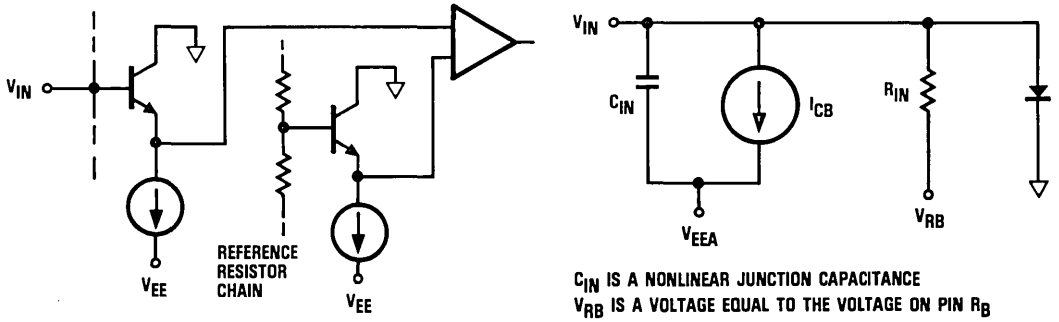


Figure 3. Convert Input Equivalent Circuit

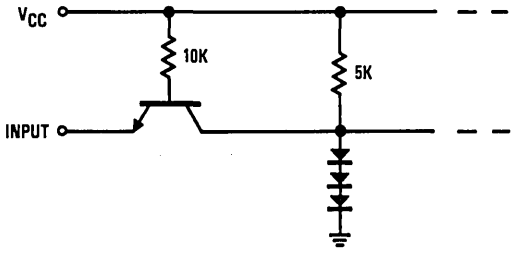
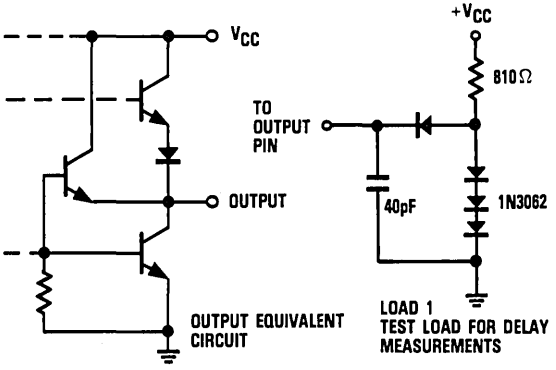


Figure 4. Output Circuits



D

Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND}) ..... −0.5 to +7.0V
V_{EE} (measured to A_{GND}) ..... +0.5 to −7.0V
A_{GND} (measured to D_{GND}) ..... −0.5 to +0.5V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND}) ..... −0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND}) ..... +0.5 to V_{EE}V
V_{RT} (measured to V_{RB}) ..... +2.2 to −2.2V

Output

Applied voltage (measured to D_{GND}) ..... −0.5 to +5.5V[2]
Applied current, externally forced ..... −1.0 to +6.0mA[3,4]
Short circuit duration (single output in high state to ground) ..... 1 sec

Temperature

Operating, ambient ..... −55 to +125°C
junction ..... +175°C
Lead, soldering (10 seconds) ..... +300°C
Storage ..... −65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage	4.75	5.0	5.25	4.50	5.0	5.50	V
V_{EE}	Negative Supply Voltage	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0	+0.1	−0.1	0	+0.1	V
t_{PWL}	CONV Pulse Width, LOW	18			18			ns
t_{PWH}	CONV Pulse Width, HIGH	22			22			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
V_{RT}	Most Positive Reference Input [1]	−0.1	0.0	0.1	−0.1	0.0	+0.1	V
V_{RB}	Most Negative Reference Input [1]	−1.9	−2.0	−2.1	−1.9	−2.0	−2.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	1.8	2.0	2.2	1.8	2.0	2.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Note:

1. V_{RT} Must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = MAX, static[1]		35		40	mA
I_{EE}	Negative Supply Current	V_{EE} = MAX, static[1]					
		T_A = 0°C to 70°C		-260			mA
		T_A = 70°C		-185			mA
		T_C = -55°C to 125°C				-320	mA
		T_C = 125°C				-180	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM		35		45	mA
R_{REF}	Total Reference Resistance		67		50		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}	10		10		kOhms
C_{IN}	Input Capacitance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}		100		100	pF
I_{CB}	Input Constant Bias Current	V_{EE} = MAX		200		550	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.5V					
		CONV		-0.4		-0.4	mA
		NMINV, NLINV		-0.6		-0.6	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V		50		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, Output HIGH, one pin to ground, one second duration.		-30		-30	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:

1. Worst case, all digital inputs and outputs LOW.

D

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{CC} = MIN, V_{EE} = MIN	20		20		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = MIN, V_{EE} = MIN	0	10	0	15	ns
t_D	Digital Output Delay	V_{CC} = MIN, V_{EE} = MIN, Load 1		30		35	ns
t_{HO}	Digital Output Hold Time	V_{CC} = MAX, V_{EE} = MAX, Load 1	5		5		ns

System performance characteristics within specified operating conditions

Parameter			Test Conditions	Temperature Range				Units
				Standard		Extended		
				Min	Max	Min	Max	
E_{LI}	Linearity Error	Integral, Independent	V_{RT}, V_{RB} = NOM		0.2		0.2	%
E_{LD}	Linearity Error	Differential			0.2		0.2	%
CS	Code Size			25	175	25	175	% Nominal
E_{OT}	Offset Error	Top	V_{IN} = V_{RT}		+45		+45	mV
E_{OB}	Offset Error	Bottom	V_{IN} = V_{RB}		−30		−30	mV
T_{CO}	Offset Error	Temperature Coefficient			±20		±20	μV/°C
BW	Bandwidth, Full Power Input			7		5		MHz
t_{TR}	Transient Response, Full Scale				20		20	ns
SNR	Signal-to-Noise Ratio		20MSPS Conversion Rate, 10MHz Bandwidth					
		Peak Signal/RMS Noise	1.248MHz Input	54		53		dB
			2.438MHz Input	53		52		dB
		RMS Signal/RMS Noise	1.248MHz Input	45		44		dB
			2.438MHz Input	44		43		dB
E_{AP}	Aperture Error				60		60	ps
DP	Differential Phase Error		F_S = 4 x NTSC		1.0		1.0	Degree
DG	Differential Gain Error		F_S = 4 x NTSC		2.0		2.0	%
NPR	Noise Power Ratio		DC to 8MHz White Noise Bandwidth 4 Sigma Loading 1.248MHz Slot 20MSPS Conversion Rate	36.5		36.5		dB

Output Coding

Step	Range		Binary		Offset Two's Complement	
			True	Inverted	True	Inverted
	−2.0000V FS	−2.0480V FS	NMINV = 1	0	0	1
	7.8431 mV STEP	8.000 mV STEP	NLINV = 1	0	1	0
000	0.0000V	0.0000V	0000000	1111111	1000000	0111111
001	−0.0078V	−0.0080V	0000001	1111110	1000001	0111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
127	−0.9961V	−1.0160V	01111111	10000000	11111111	00000000
128	−1.0039V	−1.0240V	10000000	01111111	00000000	11111111
129	−1.0118V	−1.0320V	10000001	01111110	00000001	11111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
254	−1.9921V	−2.0320V	11111110	00000001	01111110	10000001
255	−2.0000V	−2.0400V	11111111	00000000	01111111	10000000

Notes:

1. NMINV and NLINV are to be considered DC controls. They may be tied to +5V for a logical "1" and tied to ground for a logical "0."
2. Voltages are code midpoints when calibrated by the procedure given below.

Calibration

To calibrate the TDC1048, adjust V_{RT} and V_{RB} to set the 1st and 255th thresholds to the desired voltages. Note that R_1 is greater than R, ensuring calibration with a positive voltage on R_T. Assuming a 0V to −2V desired range, continuously strobe the converter with +0.0039V (1/2 LSB from 0V) on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −1.996V (1/2 LSB from −2V) and adjust V_{RB} for toggling between codes 254 and 255.

The degree of required adjustment is indicated by the offset error, E_{OT} and E_{OB}. Offset errors are generated by the inherent parasitic resistance between the package pin and the actual resistor chain on the integrated circuit. These parasitic resistors are shown as R_1 and R_2 in the Functional Block Diagram. Calibration will cancel all offset voltages, eliminating offset and gain errors.

The above method of calibration requires that both ends of the resistor chain, R_T and R_B, are driven by buffered operational amplifiers. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with a buffer offset control. The offset error at the bottom of the resistor chain results in a slight gain error, which can be compensated for by varying the voltage applied to R_B. The bottom reference is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in Figure 6.

Typical Interface

Figure 6 shows an example of a typical interface circuit for the TDC1048. The analog input amplifier is a bipolar wideband operational amplifier, which is used to directly drive the A/D converter. Bipolar inputs may be accommodated by adjusting the offset control. A zener diode provides a stable reference for both the offset and gain control. All five V_{IN} pins are connected close to the device package, and the buffer amplifier feedback loop should be closed at that point. The buffer has a gain of minus two, increasing a 1 Volt p-p video input signal to the recommended 2 Volt p-p input for the A/D converter. Proper decoupling is recommended for all systems, although the degree of decoupling shown may not be needed. A variable capacitor permits buffer optimization, by either step response or frequency response. This may be replaced with a fixed value capacitor, as determined by the layout and desired optimization.

The bottom reference voltage, V_{RB}, is supplied by an inverting amplifier, buffered with a PNP transistor. The transistor provides a low-impedance source and is necessary to sink the current flowing through the reference resistor chain. The bottom reference voltage can be adjusted to cancel the gain error introduced by the offset voltage, E_{OB}, as discussed in the calibration section.

Figure 5. Typical Reference Midpoint Adjust Circuit

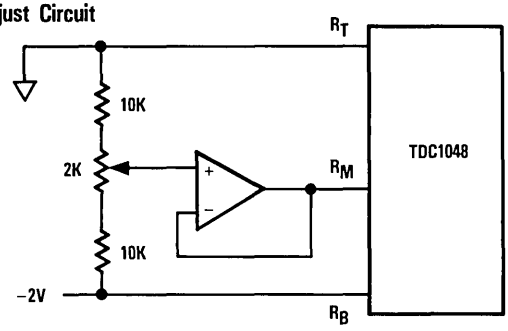
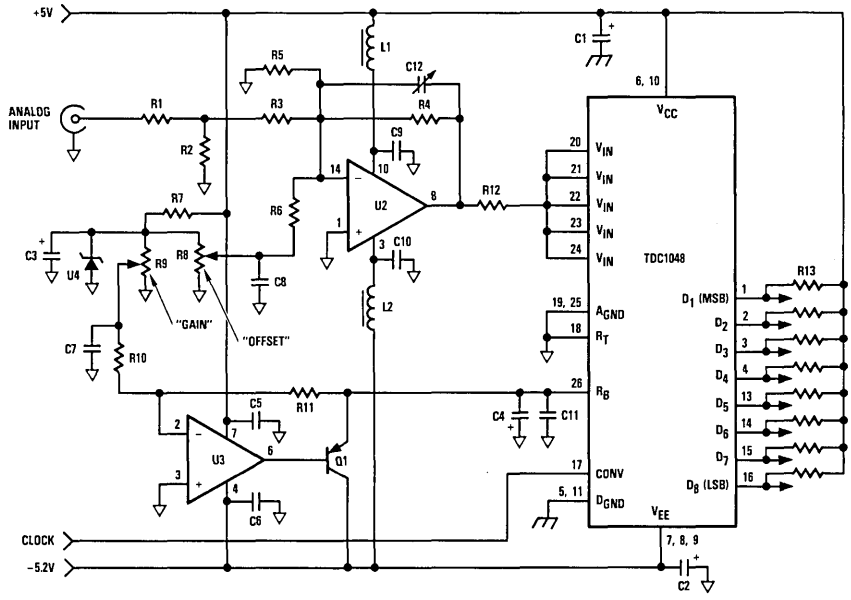


Figure 6. TDC1048 Typical Interface Circuit



Parts List

Resistors

R1	0.0Ω	1/4W	5%
R2	80.7Ω	1/4W	5%
R3	1KΩ	1/4W	5%
R4	2KΩ	1/4W	5%
R5	220Ω	1/4W	5%
R6	2KΩ	1/4W	5%
R7	1KΩ	1/4W	5%
R8	2KΩ	1/4W	Multiturn Pot
R9	2KΩ	1/4W	Multiturn Pot
R10	10KΩ	1/4W	5%
R11	20KΩ	1/4W	5%
R12	27Ω	1/4W	5%
R13	2.2KΩ	SIP	5%

Capacitors

C1-C4	10μF	25V
C5-C11	0.1μF	50V
C12	1-6pF	variable

Integrated Circuits

U1	TRW TDC1048
U2	HA-2539-5 op-amp
U3	uA741C op-amp
U4	LM313 reference

Transistors

Q1	2N2907

Inductors

L1, L2	Ferrite beads

$$R2 = \frac{1}{\frac{2V_{Range}}{V_{REF}\,Z_{IN}} - 0.001} \qquad R1 = Z_{IN} - \frac{1000\,R2}{1000 + R2}$$

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1048J6C	STD-T_A = 0°C to 70°C	Commercial	28 Lead DIP	1048J6C
TDC1048J6G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	28 Lead DIP	1048J6G
TDC1048J6F	EXT-T_C = -55°C to 125°C	Commercial	28 Lead DIP	1048J6F
TDC1048J6A	EXT-T_C = -55°C to 125°C	High Reliability[1]	28 Lead DIP	1048J6A
TDC1048C3C	STD-T_A = 0°C to 70°C	Commercial	28 Contact Chip Carrier	1048C3C
TDC1048C3G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	28 Contact Chip Carrier	1048C3G
TDC1048C3F	EXT-T_C = -55°C to 125°C	Commercial	28 Contact Chip Carrier	1048C3F
TDC1048C3A	EXT-T_C = -55°C to 125°C	High Reliability[1]	28 Contact Chip Carrier	1048C3A
TDC1048B6C	STD-T_A = 0°C to 70°C	Commercial	28 Lead CERDIP	1048B6C
TDC1048B6G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	28 Lead CERDIP	1048B6G

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Preliminary Information describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact TRW for current information.

Note:

1. Per TRW document 70Z01757.

TDC1147
Preliminary Information

Monolithic Video A/D Converter
7-bit, 15MSPS

The TDC1147 is a 7-bit "flash" analog-to-digital converter which has no pipeline delay between sampling and valid data. The output data register normally found on flash A/D converters has been bypassed, allowing data to transfer directly to output drivers from the encoding logic section of the circuit. The converter requires only one clock pulse to perform the complete conversion operation. The conversion time is guaranteed to be less than 60 nanoseconds.

The TDC1147 is function and pin-compatible with TRW's TDC1047 7-bit flash A/D converter which has an output data register. The TDC1147 will operate accurately at sampling rates up to 15MSPS and has an analog bandwidth of 7MHz. Linearity errors are guaranteed to be less than 0.4% over the operating temperature range.

Features

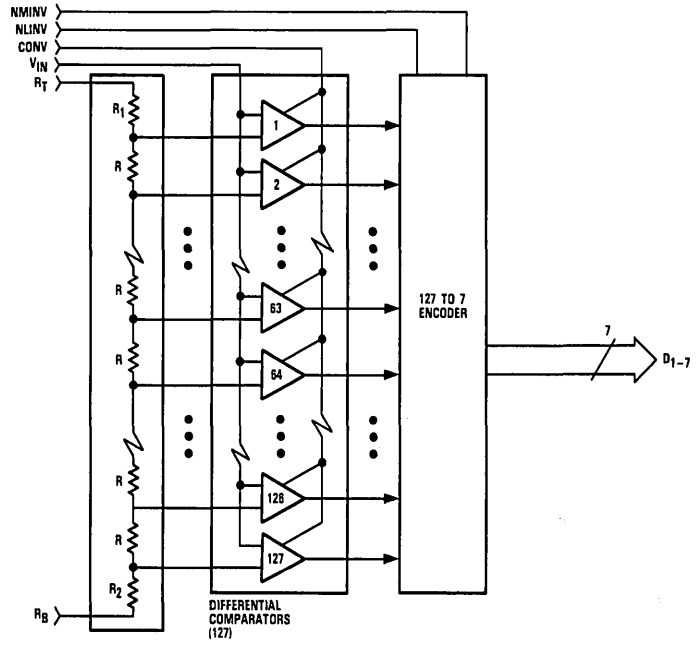
- No Digital Pipeline Delay
- 7-Bit Resolution
- 1/2 LSB Linearity
- Sample-And-Hold Circuit Not Required
- TTL Compatible
- Selectable Output Format
- Available In 24 Lead DIP Or CERDIP

Applications

- Low-Cost Video Digitizing
- Medical Imaging
- Data Acquisition
- High Resolution A/D Converters
- Telecommunications Systems
- Radar Data Conversion

D

Functional Block Diagram



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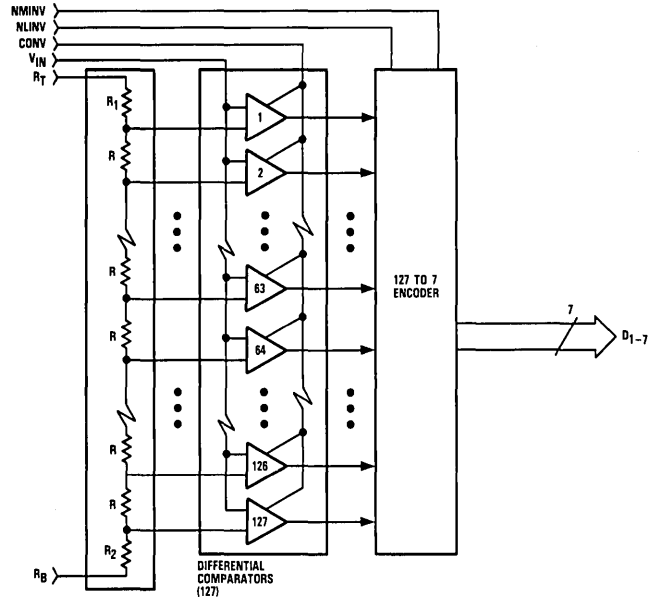
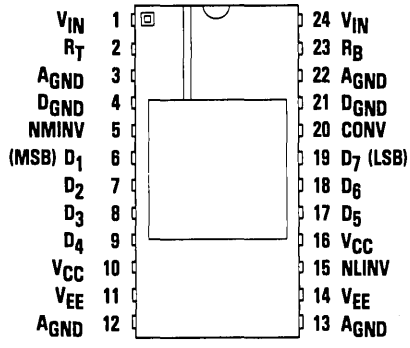
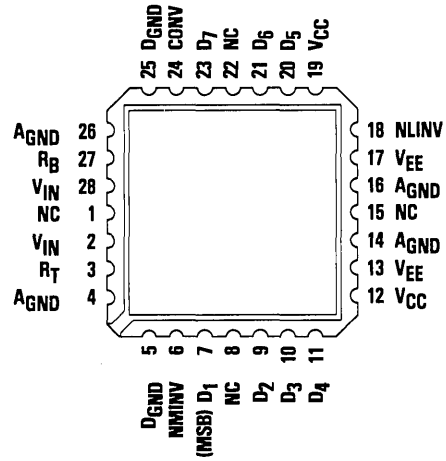
Functional Block Diagram



Pin Assignments



24 Lead DIP – J7 Package
24 Lead CERDIP – B7 Package



28 Contact Chip Carrier – C3 Package

Functional Description

General Information

The TDC1147 has two functional sections: a comparator array and encoding logic. The comparator array compares the input signal with 127 reference voltages to produce an N-of-127 code (sometimes referred to as a "thermometer" code, as all the comparators referred to voltages more positive than the input signal will be off, and those referred to voltages more negative than the input signal will be on). The encoding logic converts the N-of-127 code into binary or offset two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV.

Power

The TDC1147 operates from two supply voltages, +5.0V and -5.2V. The return path for I_{CC} (the current drawn from the +5.0V supply) is D_{GND}. The return path for I_{EE} (the current drawn from the -5.2V supply) is A_{GND}. All power and ground pins must be connected.

Name	Function	Value	J7, B7 Package	C3 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pins 10, 16	Pin 12
V_{EE}	Negative Supply Voltage	-5.2V	Pins 11, 14	Pins 13, 17
D_{GND}	Digital Ground	0.0V	Pins 4, 21	Pins 5, 25
A_{GND}	Analog Ground	0.0V	Pins 3, 12, 13, 22	Pins 4, 14, 16, 26

Reference

The TDC1147 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between +0.1V and -1.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain (V_{RT} - V_{RB}) must be between 0.8V and 1.2V. The nominal voltages are V_{RT} = 0.00V and V_{RB} = -1.00V. These voltages may be varied dynamically up to 7MHz. Due to slight variations in the reference current with clock and input signals, R_T and R_B should be low-impedance points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are varied dynamically as in an Automatic Gain Control (AGC) circuit, a low-impedance reference source is recommended.

Name	Function	Value	J7, B7 Package	C3 Package
R_T	Reference Resistor (Top)	0.00V	Pin 2	Pin 3
R_B	Reference Resistor (Bottom)	-1.00V	Pin 23	Pin 27

Controls

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e. steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the Output Coding Table.

Name	Function	Value	J7, B7 Package	C3 Package
NMINV	Not Most Significant Bit INVert	TTL	Pin 5	Pin 6
NLINV	Not Least Significant Bit INVert	TTL	Pin 15	Pin 18

Convert

The TDC1147 uses a CONVert (CONV) input signal to initiate the A/D conversion process. Unlike other flash A/D converters which have a one-clock-cycle pipeline delay between sampling and output data, the TDC1147 requires only a single pulse to perform the entire conversion operation. The analog input is sampled (comparators are latched) within the maximum Sampling Time Offset (t_{STO}, see Figure 1). Data from that sample becomes valid after a maximum Output Delay Time (t_D) while data from the previous sample is held at the outputs for a minimum Output Hold Time (t_{HO}). This allows data from the TDC1147 to be acquired by an external register or other circuitry. Note that there are minimum time requirements for the HIGH and LOW portions (t_{PWH}, t_{PWL}) of the CONV waveform and all output timing specifications are measured with respect to the rising edge of CONV.

Name	Function	Value	J7, B7 Package	C3 Package
CONV	Convert	TTL	Pin 20	Pin 24

Analog Input

The TDC1147 uses latching comparators which cause the input impedance to vary slightly with the signal level. For optimal performance, both V_{IN} pins must be used and the source impedance of the driving circuit must be less than 30 Ohms. The input signal will not damage the TDC1147 if it remains within the range of V_{EE} to +0.5V. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number between 0 and 127 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction.

Name	Function	Value	J7, B7 Package	C3 Package
V_{IN}	Analog Signal Input	0V to -1V	Pins 1, 24	Pins 2, 28

Outputs

The outputs of the TDC1147 are TTL compatible, and capable of driving four low-power Schottky TTL (54/74 LS) unit loads. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. New data becomes valid after a maximum time (t_D) after the rising edge of the CONV signal. The use of 2.2 kOhm pull-up resistors is recommended.

Name	Function	Value	J7, B7 Package	C3 Package
D_1	Most Significant Bit Output	TTL	Pin 6	Pin 7
D_2		TTL	Pin 7	Pin 9
D_3		TTL	Pin 8	Pin 10
D_4		TTL	Pin 9	Pin 11
D_5		TTL	Pin 17	Pin 20
D_6		TTL	Pin 18	Pin 21
D_7	Least Significant Bit Output	TTL	Pin 19	Pin 23

Figure 1. Timing Diagram

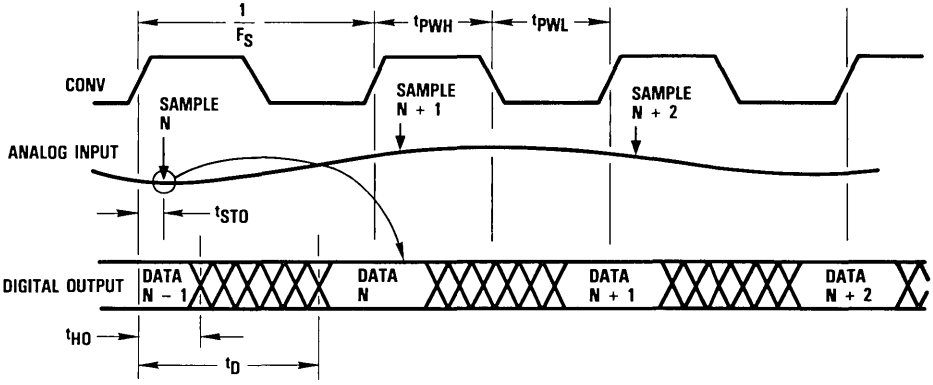
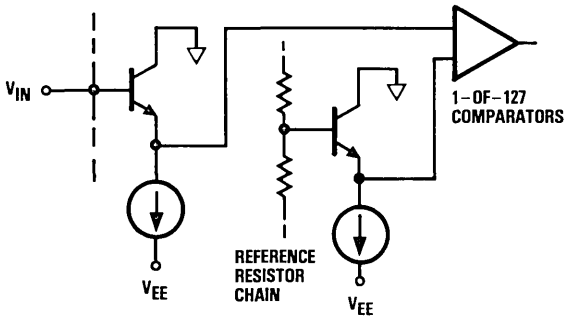
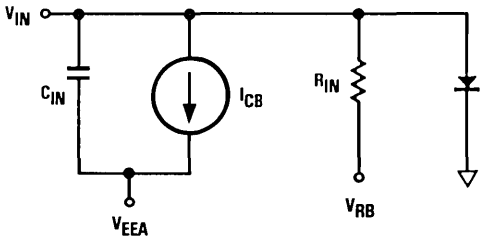


Figure 2. Simplified Analog Input Equivalent Circuit





C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

D

Figure 3. Digital Input Equivalent Circuit

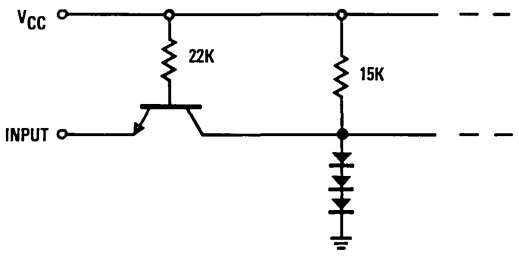
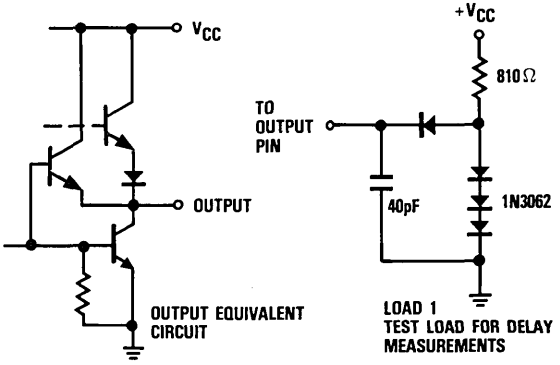


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	−0.5 to +0.5V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EE}
V_{RT} (measured to V_{RB})	+2.2 to −2.2V

Output

Applied voltage (measured to D_{GND})	−0.5 to 5.5V [2]
Applied current, externally forced	−1.0 to 6.0mA [3,4]
Short circuit duration (single output in high state to ground)	1 sec

Temperature

Operating, case	−55 to +125°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{CC}	Positive Supply Voltage (measured to D_{GND})	4.75	5.0	5.25	V
V_{EE}	Negative Supply Voltage (measured to A_{GND})	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	22			ns
t_{PWH}	CONV Pulse Width, HIGH	18			ns
V_{IL}	Input Voltage, Logic LOW			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			V
I_{OL}	Output Current, Logic LOW			4.0	mA
I_{OH}	Output Current, Logic HIGH			−0.4	mA
V_{RT}	Most Positive Reference Input [1]	−0.1	0.00	0.1	V
V_{RB}	Most Negative Reference Input [1]	−0.9	−1.00	−1.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	0.8	1.0	1.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V
T_A	*Ambient Temperature, Still Air*	0		70	°C

Note:

1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
I_{CC}	Positive Supply Current	V_{CC} = MAX, static[1]		25	mA
I_{EE}	Negative Supply Current	V_{EE} = MAX, static[1]			
		T_A = 0°C to 70°C		170	mA
		T_A = 70°C		135	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM		35	mA
R_{REF}	Total Reference Resistance		34		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}	100		kOhms
C_{IN}	Input Capacitance			60	pF
I_{CB}	Input Constant Bias Current	V_{EE} = MAX		160	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.5V CONV		−0.4	mA
		NMINV, NLINV		−0.6	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, Output HIGH, one pin to ground, one second duration.		−30	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15	pF

Note:
1. Worst case: All digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

D

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
F_S	Maximum Conversion Rate	V_{CC} = MIN, V_{EE} = MIN	15		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = MIN, V_{EE} = MIN		7	ns
t_D	Output Delay	V_{CC} = MIN, V_{EE} = MIN, Load 1		60	ns
t_{HO}	Output Hold Time	V_{CC} = MAX, V_{EE} = MAX, Load 1	15		ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB} = NOM		0.4	%
E_{LD}	Linearity Error Differential			0.4	%
CS	Code Size	V_{RT}, V_{RB} = NOM	30	170	% Nominal
V_{OT}	Offset Voltage Top	V_{IN} = V_{RT}		+50	mV
V_{OB}	Offset Voltage Bottom	V_{IN} = V_{RB}		−30	mV
T_{CO}	Offset Voltage Temperature Coefficient			±20	µV/°C
BW	Bandwidth, Full Power Input		7		MHz
t_{TR}	Transient Response, Full Scale			10	ns
SNR	Signal-to-Noise Ratio	7MHz Bandwith, 20MSPS Conversion Rate			
	Peak Signal/RMS Noise	1MHz Input	45		dB
		7MHz Input	43		dB
	RMS Signal/RMS Noise	1MHz Input	36		dB
		7MHz Input	34		dB
E_{AP}	Aperture Error			50	ps
DP	Differential Phase Error[1]	F_S = 4 × NTSC		1.5	Degree
DG	Differential Gain Error[1]	F_S = 4 × NTSC		2.5	%

Note:

1. In excess of quantization.

Output Coding

Range	Binary True	Binary Inverted	Offset Two's Complement True	Offset Two's Complement Inverted
−1.00V FS	NMINV = 1	0	0	1
	NLINV = 1	0	1	0
0.0000V	0000000	1111111	1000000	0111111
−0.0078V	0000001	1111110	1000001	0111110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−0.4960V	0111111	1000000	1111111	0000000
−0.5039V	1000000	0111111	0000000	1111111
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−0.9921V	1111110	0000001	0111110	1000001
−1.0000V	1111111	0000000	0111111	1000000

Note:

1. Voltages are code midpoints.

Calibration

To calibrate the TDC1147, adjust V_{RT} and V_{RB} to set the 1st and 127th thresholds to the desired voltages. Assuming a 0V to −1V input range, continuously strobe the converter with −0.0039V (1/2 LSB from 0V) on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −0.996V (1/2 LSB from −1V) and adjust V_{RB} for toggling between codes 126 and 127.

The degree of required adjustment is indicated by the offset voltages, V_{OT} and V_{OB}. Offset voltages are generated by the inherent parasitic resistance between the package pin and the actual resistor chain on the integrated circuit. These parasitic resistors are shown as R_1 and R_2 in the Functional Block Diagram. Calibration will cancel all offset voltages, eliminating offset and gain errors.

The above method for calibration requires that both ends of the resistor chain, R_T and R_B, are driven by variable voltage sources. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with an input amplifier offset control. The offset error at the bottom of the resistor chain causes a slight gain error, which can be compensated for by varying the voltage applied to R_B. The bottom reference is a convenient point for gain adjust that is not in the analog signal path.

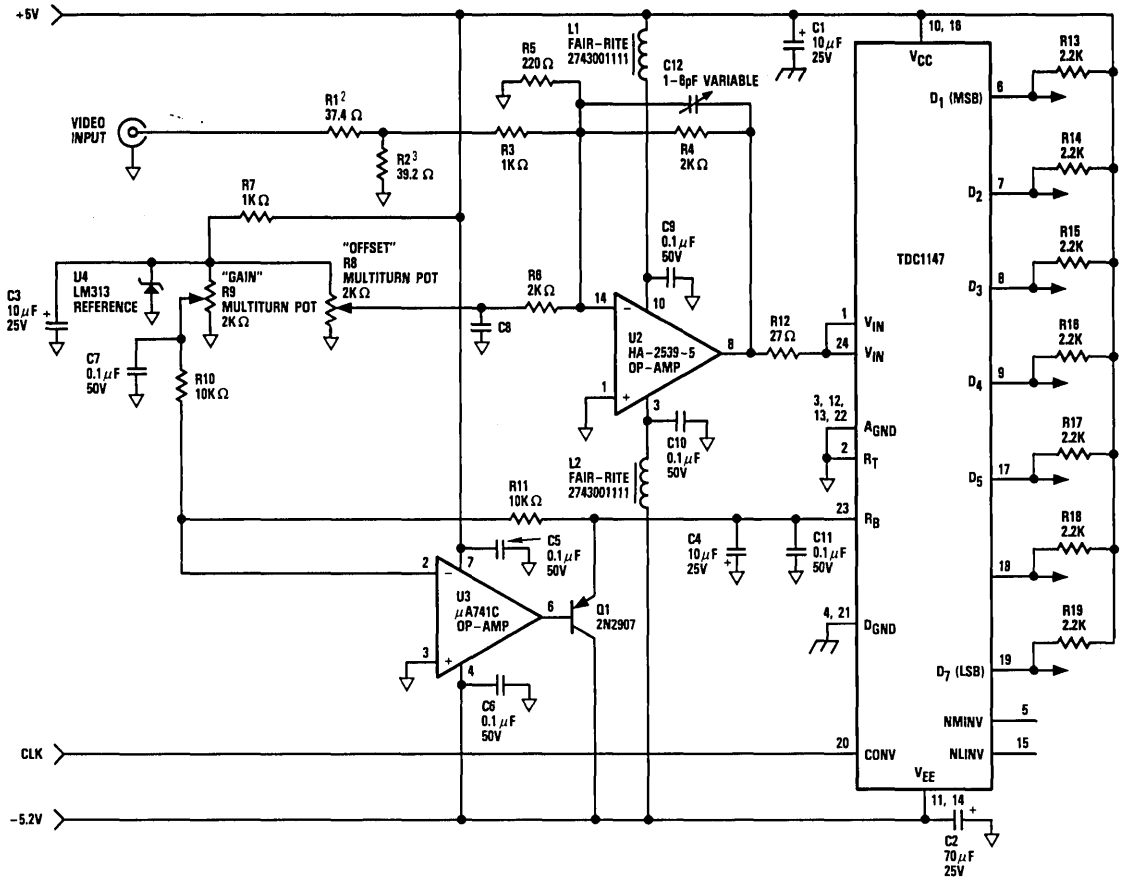
Typical Interface Circuit

Figure 6 shows an example of a typical interface circuit for the TDC1147. The analog input amplifier is a bipolar wideband operational amplifier, which is used to directly drive the A/D converter. Bipolar inputs may be accommodated by adjusting the offset control. A zener diode provides a stable reference for both the offset and gain control. The amplifier has a gain of −1 providing the recommended 1 Volt p-p input for the A/D converter. Proper decoupling is recommended for all supplies, although the degree of decoupling shown may not be needed. A variable capacitor permits either step response or frequency response optimization. This may be replaced with a fixed capacitor, whose value depends upon the circuit board layout and desired optimization.

The bottom reference voltage, V_{RB}, is supplied by an inverting amplifier, followed with a PNP transistor. The transistor provides a low-impedance source and is necessary to sink the current flowing through the reference resistor chain. The bottom reference voltage can be adjusted to cancel the gain error introduced by the offset voltage, V_{OB}, as discussed in the Calibration section.

D

Figure 5. Typical Interface Circuit



Notes:

1. Unless otherwise specified, all resistors are 1/4W, 2%.
2. $R1 = Z_{IN} - \left(\frac{1000\ R2}{1000 + R2}\right)$
3. $R2 = \frac{1}{\left(\frac{2V_{Range}}{V_{REF}\ Z_{IN}}\right) - 0.001}$

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1147J7C	STD-T_A = 0°C to 70°C	Commercial	24 Lead DIP	1147J7C
TDC1147J7G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	24 Lead DIP	1147J7G
TDC1147B7C	STD-T_A = 0°C to 70°C	Commercial	24 Lead CERDIP	1147B7C
TDC1147B7G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	24 Lead CERDIP	1147B7G
TDC1147C3C	STD-T_A = 0°C to 70°C	Commercial	28 Contact Chip Carrier	1147C3C
TDC1147C3G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	28 Contact Chip Carrier	1147C3G

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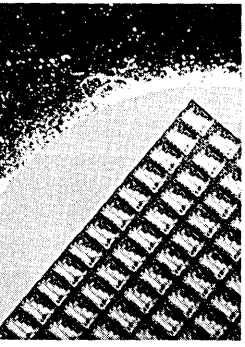
Preliminary Information describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact TRW for current information.

D

V L S I

D A T A

B O O K



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Evaluation Boards

TRW LSI Products provides individual evaluation boards which are intended to be used as prototyping aids in the evaluation of particular TRW devices, or as incoming inspection test fixtures. Each board is fully assembled and tested and contains all the necessary peripheral circuitry which allows for quick and convenient operation of the device. Built on double–sided printed circuit boards, all of TRW's evaluation boards meet Eurocard (DIN 41612B) format requirements.

Board	Resolution (Bits)	Conversion Rate (MSPS)	ECL/TTL
TDC1007E1C/P1C	8	20	TTL
TDC1014E1C/P1C	6	25	TTL
TDC1019E1C	9	15	ECL
TDC1025E1C	8	50	ECL
TDC1029E1C	6	100	ECL
TDC1047E1C	7	20	TTL
TDC1048E1C	8	20	TTL

TDC1007P1C
TDC1007E1C

A/D Converter Evaluation Board
8-bit, 20MSPS

The TDC1007 evaluation board is a fully assembled and tested circuit board designed to aid in the evaluation of TRW's TDC1007J1 8-bit video analog-to-digital (A/D) converter. The board contains circuitry for buffering input signals, generating reference voltages, and regulating on-board power supply voltages. All digital inputs and outputs are TTL compatible, and provisions are made for gain and offset adjustments. The board *requires +5 and ±15 Volt power supplies.*

There are two versions of the TDC1007 evaluation board. The P1C board has a standard 22/44 format edge connector interface, and the E1C uses the Eurocard connector format.

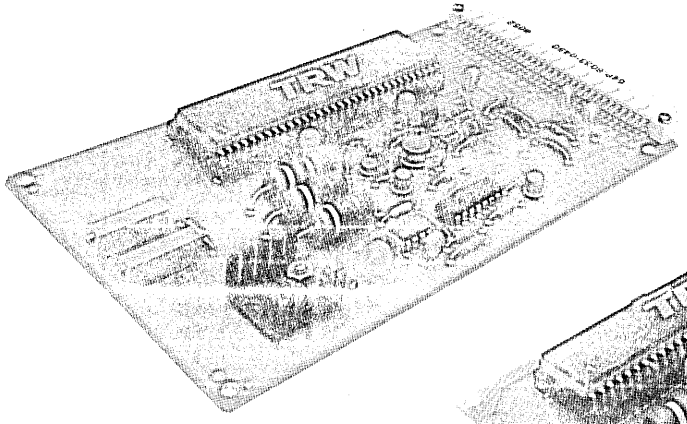
Features

- Includes TDC1007J1C 8-bit A/D Converter
- User-Selectable Input Impedance
- User-Selectable Input Voltage Range
- Unipolar Or Bipolar Operation
- Gain And Offset Calibration Controls
- Operates From +5 And ±15 Volt Power Supplies
- Provision For Optional Digital Output Buffers
- Eurocard (E1C) Or 22/44 Edge Connector (P1C) Format

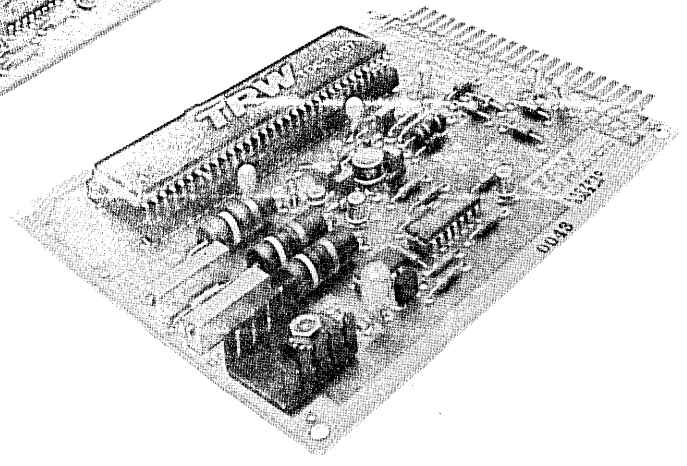
Applications

- Evaluation Of TDC1007 A/D Converter
- System Prototyping Aid
- Incoming Inspection Test Fixture

TDC1007E1C



TDC1007P1C



E

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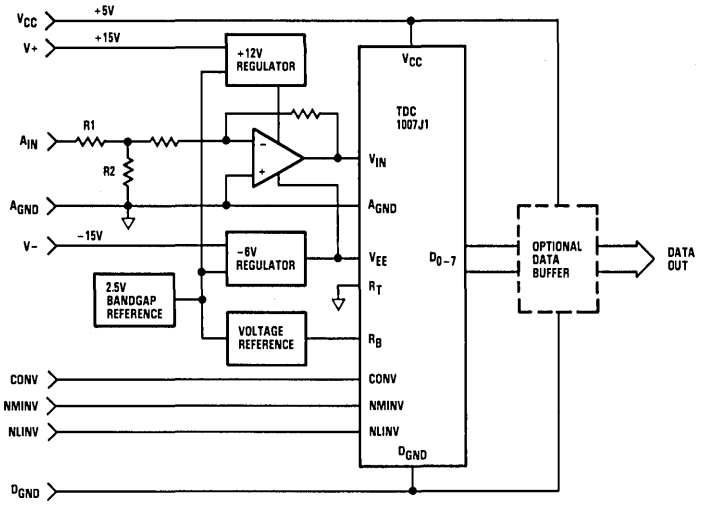
Functional Block Diagram



Pin Assignments

NC	A	1	A_{GND}
NC	B	2	A_{GND}
NC	C	3	A_{GND}
NC	D	4	A_{GND}
V-	E	5	A_{GND}
REF 2	F	6	A_{GND}
V+	H	7	A_{GND}
REF 1	J	8	A_{GND}
A_{IN}	K	9	A_{GND}
NC	L	10	NC
V_{CC}	M	11	D_{GND}
CONV	N	12	D_{GND}
(LSB) D_8	P	13	D_{GND}
NMINV	R	14	D_{GND}
(MSB) D_1	S	15	D_{GND}
D_2	T	16	D_{GND}
D_3	U	17	D_{GND}
D_4	V	18	D_{GND}
NLINV	W	19	D_{GND}
D_5	X	20	D_{GND}
D_6	Y	21	D_{GND}
D_7	Z	22	-6V

TDC1007P1C

D_{GND}	A1	B1	-6V
D_{GND}	A2	B2	D_{GND}
D_{GND}	A3	B3	D_7
D_{GND}	A4	B4	D_6
D_{GND}	A5	B5	D_5
D_{GND}	A6	B6	NLINV
D_{GND}	A7	B7	D_4
D_{GND}	A8	B8	D_3
D_{GND}	A9	B9	D_{GND}
D_{GND}	A10	B10	D_{GND}
D_{GND}	A11	B11	D_2
D_{GND}	A12	B12	D_1 (MSB)
D_{GND}	A13	B13	NMINV
D_{GND}	A14	B14	D_8 (LSB)
D_{GND}	A15	B15	CONV
D_{GND}	A16	B16	D_{GND}
D_{GND}	A17	B17	D_{GND}
D_{GND}	A18	B18	V_{CC}
NC	A19	B19	NC
A_{GND}	A20	B20	NC
A_{GND}	A21	B21	A_{IN}
A_{GND}	A22	B22	A_{GND}
A_{GND}	A23	B23	REF 1
A_{GND}	A24	B24	V+
A_{GND}	A25	B25	A_{GND}
A_{GND}	A26	B26	REF 2
A_{GND}	A27	B27	V-
A_{GND}	A28	B28	A_{GND}
A_{GND}	A29	B29	NC
A_{GND}	A30	B30	NC
A_{GND}	A31	B31	NC
A_{GND}	A32	B32	NC

TDC1007E1C

LSI Products Division
TRW Electronic Components Group

Functional Description

General Information

The TDC1007 evaluation board consists of four functional sections: buffer amplifier, reference voltage generator, voltage regulators, and A/D converter. The board is configured for optional output data buffers. Analog and digital grounds are separated on the board in order to provide flexibility in system grounding.

Buffer Amplifier

The input buffer amplifier has been designed specifically for standard baseband video. This amplifier is optimized for 75 Ohm, 1 Volt p-p levels. It provides a gain of -2 and offsets the output so that the A/D converter receives a full-scale input signal from 0 to -2 Volts.

The buffer amplifier is designed to drive the input capacitance of the TDC1007 A/D converter. An NPN transistor buffer follows the wideband operational amplifier to provide improved current drive and insure frequency stability.

Components C2 and R10 optimize the performance of the amplifier and are selected as part of the manufacturing process. The buffer amplifier is operated from +12 and -6 Volt regulators which are included on the evaluation board.

Voltage Reference

The reference voltage for the TDC1007 is generated by operational amplifier U3B. This amplifier is buffered by a PNP transistor (Q4) in order to supply the reference current for the A/D converter. The system gain is adjusted by varying the reference voltage (R12).

Voltage Regulators

Two voltage regulator circuits are provided on the evaluation board for supplying power to the buffer amplifier. U3D and Q3 provide +12 Volts for the buffer amplifier. U3A and Darlington transistor Q2 provide -6 Volts for the buffer amplifier and the A/D converter. U4 is a 2.5 Volt bandgap voltage reference for both regulators and the voltage reference source.

A/D Converter

The TDC1007 integrated circuit is an 8-bit fully parallel (flash) analog-to-digital (A/D) converter capable of digitizing an input signal at rates up to 20MSPS (MegaSamples Per Second). A single convert (CONV) signal controls the conversion operation of the device. The TDC1007 consists of 255 sampling comparators, encoding logic, and a latched output register. On the rising edge of the CONV signal, the comparators are latched and their outputs are encoded. On the next rising edge of the CONV signal, data is transferred to the TTL data outputs of the TDC1007.

Output Interface

The TDC1007E1C and P1C boards have provisions for 74S04 Schottky TTL hex inverters for buffering data and improving output drive and fan-out capability. Provision is also made for pull-up resistors on the data outputs. The use of pull-up resistors or data buffers is recommended when the board is to drive long data lines. The data outputs of the TDC1007 are routed directly to the edge connector.

Mechanical Design

The two versions of the evaluation board (P1C, E1C) differ in mechanical configuration. The P1C board is designed to interface with a standard 22/44 contact edge connector. The E1C board is designed to meet the "Eurocard" format and interface with a standard 64 conductor Eurocard connector. Mating edge connectors are included with each evaluation board.

The evaluation board can also accommodate a TDC1014 6-bit A/D converter by using the 24 lead DIP footprint found inside the perimeter of the TDC1007's 64 lead DIP footprint and by appropriate electrical changes.

The board has a standard 64 lead DIP socket for the TDC1007 integrated circuit. These may be substituted with a "Zero Insertion Force" (ZIF) socket when the board is used as a test fixture. A recommended ZIF socket is made by Textool, Inc., part number 264-4493-00-0602.

Power Supplies

The TDC1007 evaluation board operates from three power supply voltages: +5.0, +15, and −15 Volts. The return path for I_{CC} (current from the +5.0 Volt power supply) is D_{GND}. The return path for I+ and I− (current from the +15 and −15 Volt supplies) is A_{GND}. A user-installed jumper option routes the −6.0 Volt regulator output to the edge connector. The use of all ground pins is recommended. Diodes D_2 through D_6 function as voltage clamps which will prevent damage to the board if improper power supply voltages are applied.

Name	Function	Value	E1C	P1C
V_{CC}	Positive Logic Power Supply	+5V	B18	M
V+	Positive Analog Power Supply	+15V	B24	H
V−	Negative Analog Power Supply	−15V	B27	E
A_{GND}	Analog Ground	0V	A20-A32 B22 B25 B28	1-9
D_{GND}	Digital Ground	0V	A1-A18 B2 B9 B10 B16 B17	11-21
−6V	Jumper Optional −6 Volt Output	−6V	B1	22

Analog Input

The TDC1007 evaluation board is supplied with a nominal input impedance of 75 Ohms and an input voltage range of 1 Volt p-p. Both input impedance and input voltage range may be changed. The values of input resistors R1 and R2 determine the input impedance and voltage range of the evaluation board. Suggested values are shown in the Input Resistor Selection Table for various input impedances and voltage ranges.

Name	Function	Value	E1C	P1C
A_{IN}	Analog Input Voltage	See Text	B21	K

Reference

The TDC1007 evaluation board includes circuitry for generating the voltage reference for the A/D converter. In addition, there is an auxilliary −1.0 Volt reference voltage provided. These voltages are available at the edge connectors.

Name	Function	Value	E1C	P1C
REF 1	Auxilliary −1.0 Volt Output	−1V	B23	J
REF 2	−2.0 Volt Reference Output	−2V	B26	F

Control Inputs

Two control inputs are provided on the TDC1007 evaluation board for modifying the format of the output data. When NMINV is tied to a logic "0," the most significant bit of the output data is inverted. When NLINV is tied to a logic "0," the seven least significant bits of the output data are inverted. By using these DC controls, the output data can be represented in binary, inverse binary, two's complement, or inverse two's complement formats. Output data versus input voltage and control input state is illustrated in the Output Coding Table.

Name	Function	Value	E1C	P1C
NMINV	Not Most Significant Bit INVert	TTL	B13	R
NLINV	Not Least Significant Bit INVert	TTL	B6	W

Convert

The TDC1007 A/D converter is sampled within 10ns (t_{STO}) after the rising edge of the CONV signal. Delays through buffer amplifier U2 are not included in t_{STO}. Output data is latched on the next rising edge of the CONV signal. Note that there are minimum pulse width (t_{PWH}, t_{PWL}) requirements on the waveshape of the CONV signal.

Name	Function	Value	E1C	P1C
CONV	A/D Clock Input	TTL	B15	N

Data Outputs

The outputs of the TDC1007 evaluation board are TTL compatible and capable of driving four low-power Schottky unit loads (54/74LS). Data remains valid after the rising edge of the CONV signal for a minimum time, t_{HO}, and the next data becomes valid after a maximum time of t_D. The evaluation board has provisions for optional 74S04 data buffers (U5, U6). When installing these circuits, it is necessary to open traces on the board which connect the inverter inputs to their corresponding outputs.

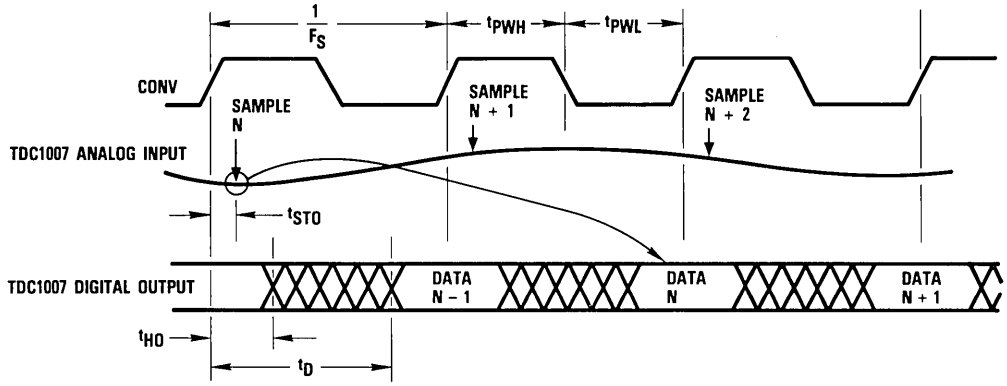
Name	Function	Value	E1C	P1C
D_1 MSB	Most Significant Data Bit	TTL	B12	S
D_2		TTL	B11	T
D_3		TTL	B8	U
D_4		TTL	B7	V
D_5		TTL	B5	X
D_6		TTL	B4	Y
D_7		TTL	B3	Z
D_8 LSB	Least Significant Data Bit	TTL	B14	P

No Connects

There are several pins or contacts to the TDC1007 evaluation board that have no connection to the circuit. These pins may be left open.

Name	Function	Value	E1C	P1C
NC	No Connect	Open	A19	10
			B19	A, B
			B20	C, D
			B29–B32	L

Figure 1. Timing Diagram



Absolute maximum ratings (beyond which the board may be damaged) [1]

Power Supply Voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V+ (measured to A_{GND})	−0.5 to +18.0V
V− (measured to A_{GND})	+0.5 to −18.0V
A_{GND} (measured to D_{GND})	+0.5 to −0.5V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
A_{IN} (measured to A_{GND})	+4.5 to −4.5V [6]

Output

Applied voltage	−0.5 to +5.5 V [2,5]
Applied current, externally forced	−1.0 to +6.0 mA [3,4,5]
Short circuit duration (single output in HIGH state to D_{GND})	1 sec [5]

Temperature

Operating, ambient	−40 to +90°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.
5. Applies to TDC1007 IC only, excluding optional data buffers.
6. With input impedance of 75 Ohms, as supplied.

Operating conditions

Parameter		Min	Nom	Max	Units
V_{CC}	Positive Supply Voltage (measured to D_{GND})	4.75	5.0	5.25	V
V+	Positive Supply Voltage (measured to A_{GND})	14.25	15.0	15.75	V
V−	Negative Supply Voltage (measured to A_{GND})	−14.25	−15.0	−15.75	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, LOW [1]	25			ns
t_{PWH}	CONV Pulse Width, HIGH [1]	15			ns
V_{IL}	Input Voltage, Logic LOW			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			V
I_{OL}	Output Current, Logic LOW [2]			4.0	mA
I_{OH}	Output Current, Logic HIGH [2]			−400	μA
A_{IN}	Input Voltage Range [3]	0.0		1.0	V
T_A	Ambient Temperature, Still Air	0		70	°C

Notes:

1. Applies to the TDC1007 IC only.
2. TDC1007 IC only, excludes optional output data buffers.
3. 75Ω Input Impedance as supplied, U2 offset zeroed.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Min	Max	Units
I_{CC}	Positive Supply Current	V_{CC} = MAX		100	mA
I+	Positive Supply Current	V+ = MAX		40	mA
I−	Negative Supply Current	V− = MAX		−540	mA
Z_{IN}	Input Impedance [1]		70	80	Ohms
I_{IL}	Input Current, Logic LOW [2]	V_{CC} = MAX, V_I = 0.5		−2.0	mA
I_{IH}	Input Current, Logic HIGH [2]	V_{CC} = MAX, V_I = 2.4V		75	μA
V_{OL}	Output Voltage, Logic LOW [2]	V_{CC} = MIN, I_{OL} = 4mA		0.5	V
V_{OH}	Output Voltage, Logic HIGH [2]	V_{CC} = MIN, I_{OH} = −400μA	2.4		V

Notes:

1. As supplied, user selectable.
2. Applies to the TDC1007 IC only, excludes optional output data buffers.

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Min	Max	Units
F_S	Maximum Conversion Rate	V_{CC} = MIN, V_{EE} = MIN	20		MHz
t_{STO}	Sampling Time Offset [2]	V_{CC} = MIN, V_{EE} = MIN	0	10	ns
t_D	Output Delay Time [3]	V_{CC} = MIN, V_{EE} = MIN		40	ns
t_{HO}	Output Data Hold Time [3]	V_{CC} = MIN, V_{EE} = MIN	10		ns

Notes:

1. All parameters apply to TDC1007 IC only.
2. Excludes delay from buffer amplifier, U2.
3. Excludes optional output data buffers.

TDC1007J1C performance characteristics within specified operating conditions [1]

Parameter		Test Conditions	Min	Max	Units
E_{LI}	Linearity Error Integral, Independent			0.3	%
E_{LD}	Linearity Error Differential			0.3	%
BW	Bandwidth, Full Power Input		7		MHz
DP	Differential Phase Error	NTSC @ 4x Color Subcarrier		1.0	Degrees
DG	Differential Gain Error	NTSC @ 4x Color Subcarrier		1.7	%

Note:

1. Items listed in this table are for the A/D converter only. Contributions to these parameters from the buffer amplifier are not significant.

Output Coding

Input Voltage[1]	Binary		Two's Complement	
	True	Inverted	True	Inverted
	NMINV = 1 NLINV = 1	0 0	0 1	1 0
0.0000	00000000	11111111	10000000	01111111
+0.0039	00000001	11111110	10000001	01111110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
+0.4978	01111111	10000000	11111111	00000000
+0.5017	10000000	01111111	00000000	11111111
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
+0.9956	11111110	00000001	01111110	10000001
+1.0000	11111111	00000000	01111111	10000000

Note:

1. Input voltage range is from 0.00 to +1.00 Volt. (Input voltages are at code centers and the voltage offset of the buffer amplifier is nulled.)

Calibration

The evaluation board is calibrated by adjusting the offset and gain trim resistors, R11 and R12. Offset can be calibrated when a voltage corresponding to 1/2 LSB above "zero-scale" is applied to the board input. The "OFFSET" potentiometer is then turned to a point where the output data toggles between "00000000" and "00000001." Gain is calibrated by applying voltage 1/2 LSB below full-scale and turning the "GAIN" pot until the output data toggles between "11111110" and "11111111."

E

Input Resistor Selection Table (Values in Ohms)

Z_{IN}	Input Voltage Range									
	1V		2V		4V		5V		10V	
	R1	R2	R1	R2	R1	R2	R1	R2	R1	R2
50	0	52.3	24.9	24.3	37.4	12.7	40.2	10	45.3	4.99
75	0	80.6	37.4	39.2	56.2	19.1	60.4	15.4	68.1	7.5
93	0	102	46.4	48.7	69.8	23.7	75	19.1	84.5	9.31
1k	0	Open	499	1k	750	332	806	249	909	110

For input voltage ranges and input impedances not covered by the Input Resistor Selection Table, the following formulas may be used to calculate R1 and R2:

$$R2 = \frac{1}{\left(\frac{VR}{Z_{IN}}\right) - \frac{1}{1000}}$$

$$R1 = Z_{IN} - \left(\frac{1000\ R2}{R2 + 1000}\right)$$

where VR is the desired input voltage range of the board, Z_{IN} is the desired input impedance of the board, and the constant value 1000 is given by the value of R3.

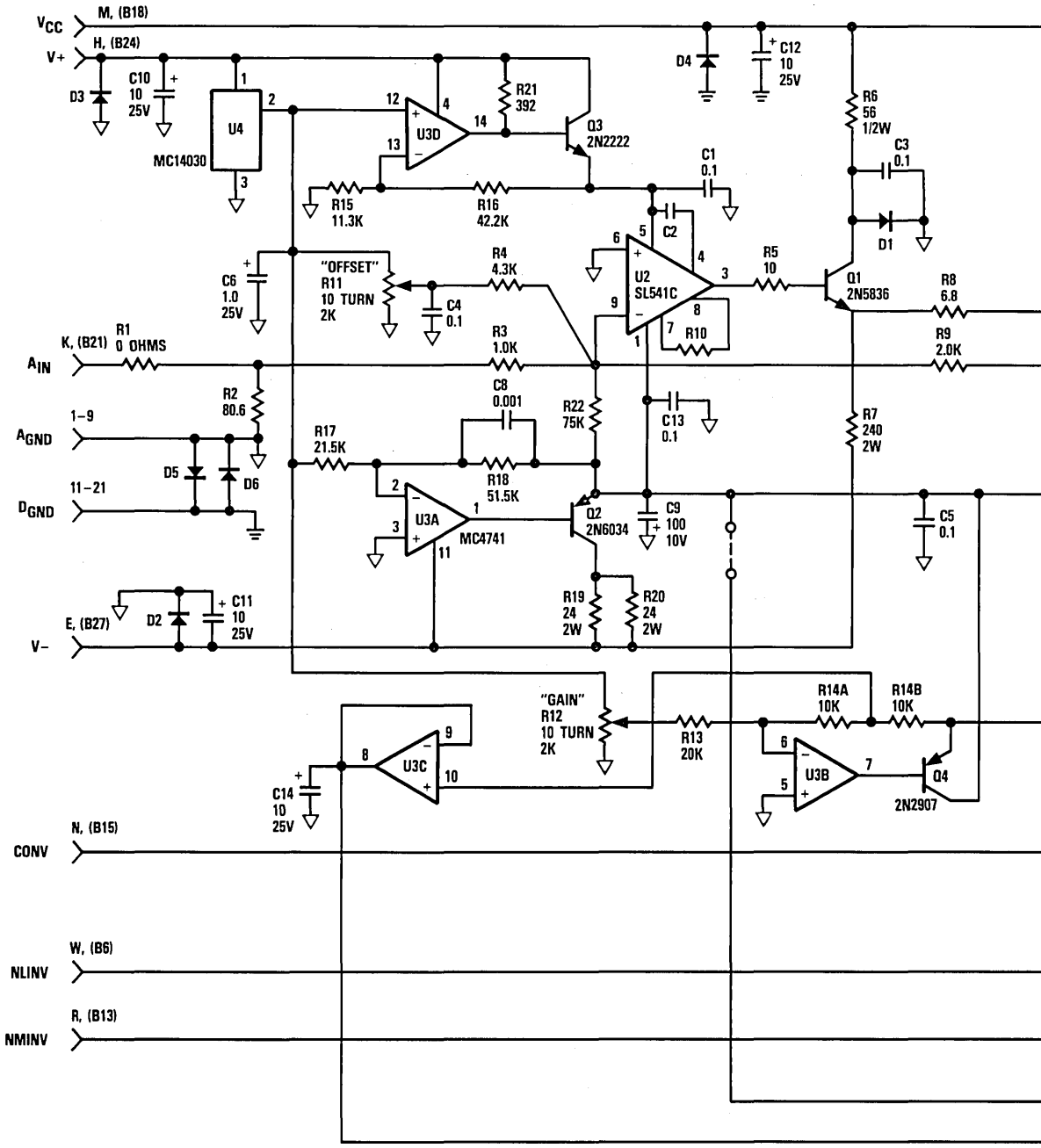
Miscellaneous parts for evaluation boards

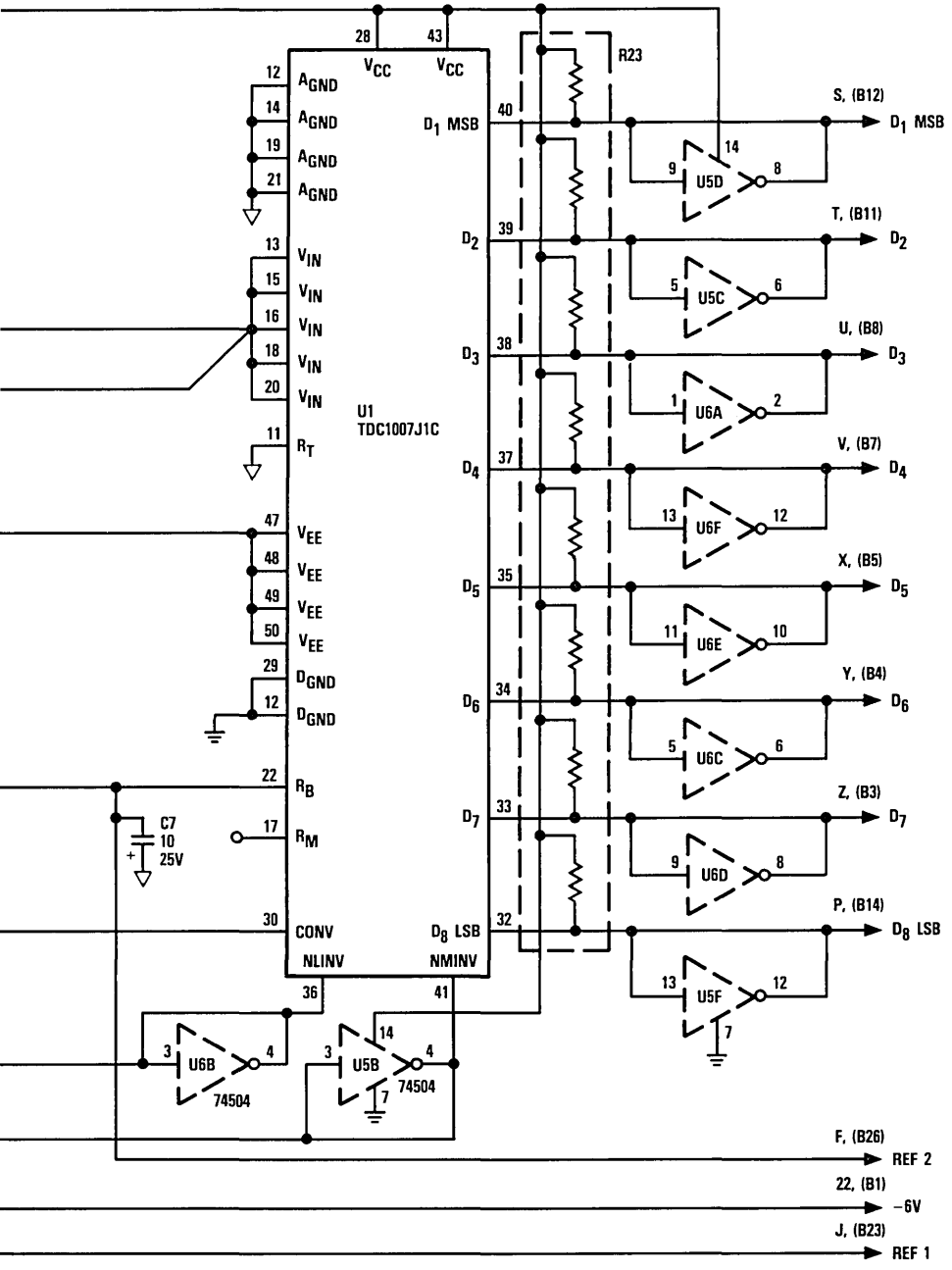
Edge connector for mating with TDC1007P1C	TRW Cinch 271-22-30-1690
Eurocard connector mounted on TDC1007E1C	Winchester 64P-6033-0430, DIN 41612 B
Eurocard connector for mating with TDC1007E1C	Winchester 64S-6033-0422-1, DIN 41612 B
64 lead IC socket for U1	Robinson-Nugent ICN-649-S5-G1 or ICN-649-S5-U1
Heat sink for Q2	Thermalloy 6D738
Mica washer for Q2	Delbert Blinn 500-125-2
Stitch-weld pins for R1 and R2	Moore Systems 700508

Notes for Figure 2. Schematic of Evaluation Board

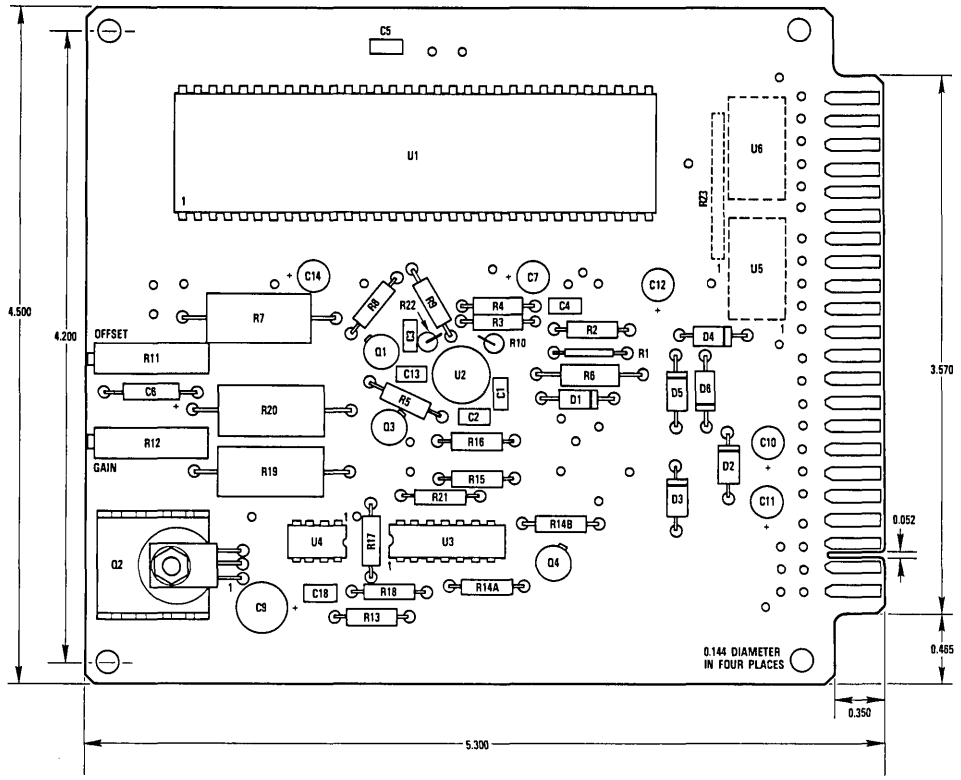
1. All capacitor values are in microFarads (μF) unless otherwise noted.
2. All capacitor voltage ratings are 50WVDC unless otherwise noted.
3. All resistors are 1/8W unless otherwise noted.
4. All resistor values are in Ohms.
5. All Diodes are 1N4001.
6. Values for C2 and R10 are selected during manufacturing.
7. R23 is an eight-resistor SIP, 2.2 kOhms, 1/4W (not supplied).
8. Edge connector numbers in parentheses (B18, etc.) are for TDC1007E1C.
9. A_{GND} pins for TDC1007E1C are B22, B25, B28, A20 to A32.
10. D_{GND} pins for TDC1007E1C are B2, B9, B10, B16, B17, A1 to A18.
11. Pins 27, 31, 44, and 45 of U1 are connected to D_{GND}.
12. Pins 1-10, 23-25, and 51-64 of U1 are connected to A_{GND}.

Figure 2. Schematic Of Evaluation Board




U1
TDC1007J1C
28
43
V_{CC}
V_{CC}
12
14
19
21
A_{GND}
A_{GND}
A_{GND}
A_{GND}
13
15
16
18
20
V_{IN}
V_{IN}
V_{IN}
V_{IN}
V_{IN}
11
R_T
47
48
49
50
V_{EE}
V_{EE}
V_{EE}
V_{EE}
29
12
D_{GND}
D_{GND}
22
R_B
17
R_M
C7
10
25V
30
CONV
NLINV
D_8 LSB
NMINV
36
41
R23
40
39
38
37
35
34
33
32
D_1 MSB
D_2
D_3
D_4
D_5
D_6
D_7
D_8 LSB
U5D
U5C
U6A
U6F
U6E
U6C
U6D
U5F
U6B
U5B
74504
74504
S, (B12)
T, (B11)
U, (B8)
V, (B7)
X, (B5)
Y, (B4)
Z, (B3)
P, (B14)
D_1 MSB
D_2
D_3
D_4
D_5
D_6
D_7
D_8 LSB
F, (B26)
REF 2
22, (B1)
−6V
J, (B23)
REF 1

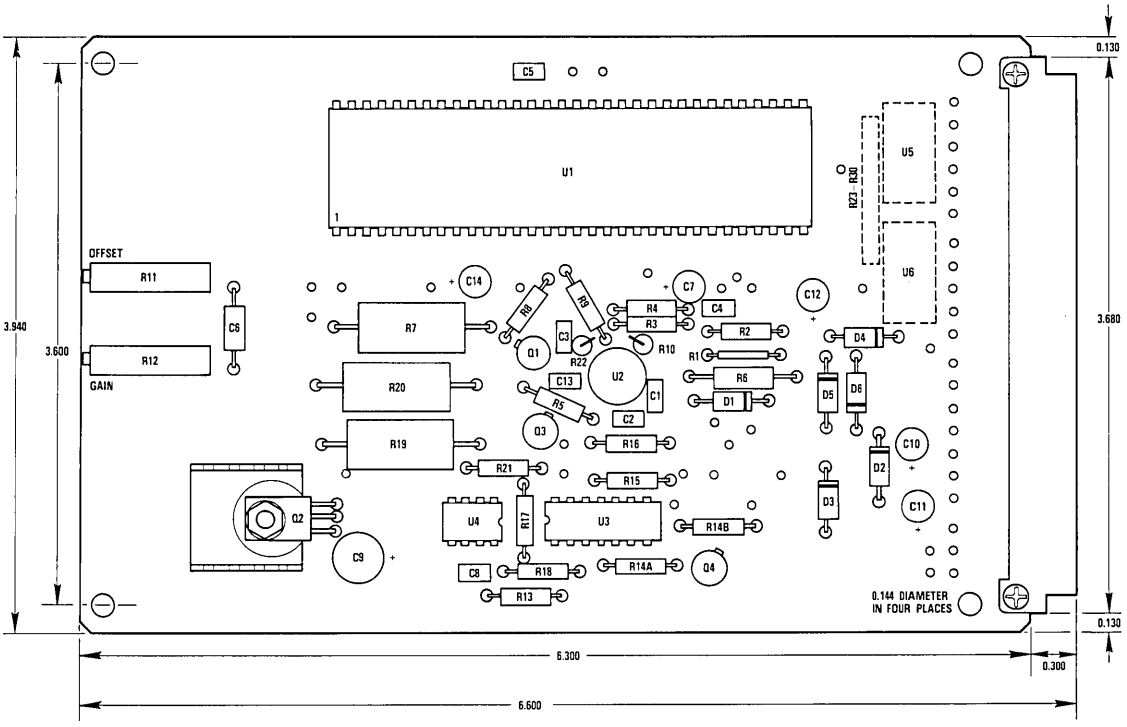
TDC1007P1C Assembly



Notes:

1. R23, U5 and U6 not supplied.
2. All dimensions in inches.

TDC1007E1C Assembly



Notes:

1. R23, U5 and U6 not supplied.
2. All dimensions in inches.

E

Ordering Information

Product Number	Description	Order Number
TDC1007E1C	Eurocard Format Board With A/D Converter	TDC1007E1C
TDC1007P1C	22/44 Edge Format Board With A/D Converter	TDC1007P1C

TDC1014E1C
TDC1014P1C

A/D Converter Evaluation Board
6-bit, 25MSPS

The TDC1014 evaluation board is a fully assembled and tested circuit board designed to aid in the evaluation of TRW's TDC1014 6-bit video analog-to-digital (A/D) converter. The board contains circuitry for buffering input signals, generating reference voltages, and regulating on-board power supply voltages. All digital inputs and outputs are TTL compatible, and provisions are made for gain and offset adjustments. The board requires +5 and ±15 Volt power supplies.

There are two versions of the TDC1014 evaluation board. The P1C board has a standard 22/44 format edge connector interface, and the E1C uses the Eurocard (DIN 41612B) connector format.

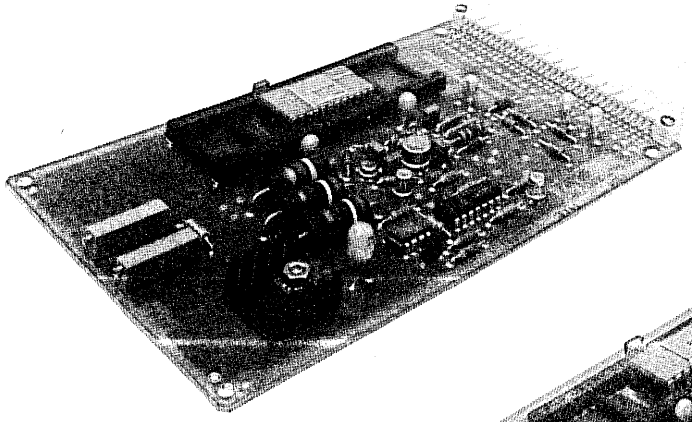
Features

- Includes TDC1014 6-Bit A/D Converter
- User-Selectable Input Impedance
- User-Selectable Input Voltage Range
- Unipolar Or Bipolar Operation
- Gain And Offset Calibration Controls
- Operates From +5 and ±15 Volt Power Supplies
- Optional Digital Output Buffers
- Eurocard (E1C) Or 22/44 Edge Connector (P1C) Format

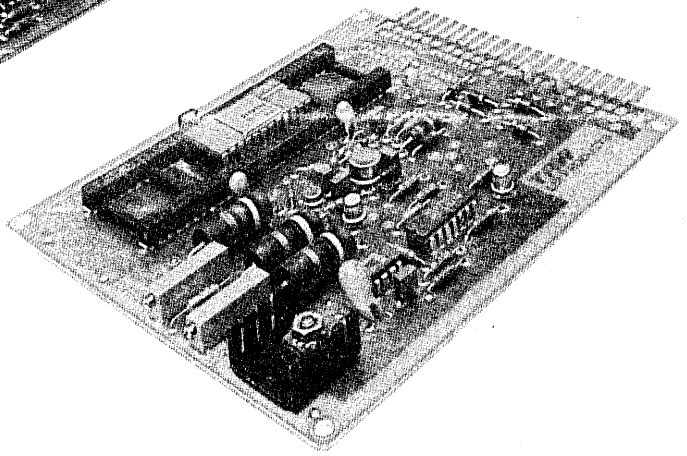
Applications

- Evaluation Of TDC1014 A/D Converter
- System Prototyping Aid
- Incoming Inspection Test Fixture

TDC1014E1C



TDC1014P1C



E

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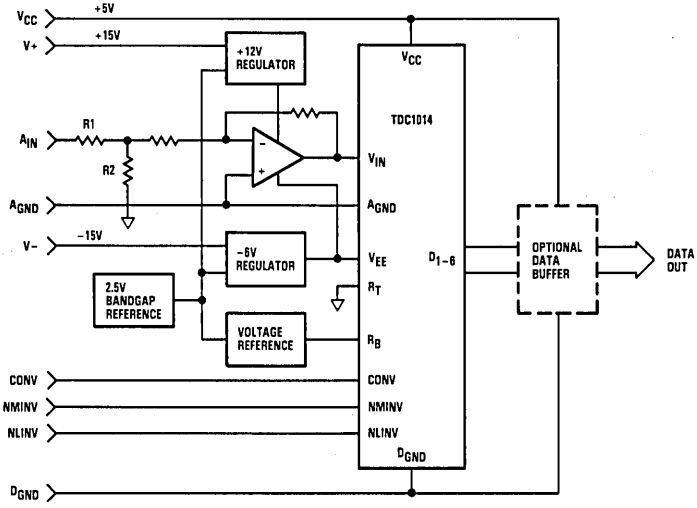
Functional Block Diagram



Pin Assignments

D_{GND}	A1	B1	-6V
D_{GND}	A2	B2	D_{GND}
D_{GND}	A3	B3	NC
D_{GND}	A4	B4	D_6 (LSB)
D_{GND}	A5	B5	D_5
D_{GND}	A6	B6	NLINV
D_{GND}	A7	B7	D_4
D_{GND}	A8	B8	D_3
D_{GND}	A9	B9	D_{GND}
D_{GND}	A10	B10	D_{GND}
D_{GND}	A11	B11	D_2
D_{GND}	A12	B12	D_1 (MSB)
D_{GND}	A13	B13	NMINV
D_{GND}	A14	B14	NC
D_{GND}	A15	B15	CONV
D_{GND}	A16	B16	D_{GND}
D_{GND}	A17	B17	D_{GND}
D_{GND}	A18	B18	V_{CC}
NC	A19	B19	NC
A_{GND}	A20	B20	NC
A_{GND}	A21	B21	A_{IN}
A_{GND}	A22	B22	A_{GND}
A_{GND}	A23	B23	REF 1
A_{GND}	A24	B24	V+
A_{GND}	A25	B25	A_{GND}
A_{GND}	A26	B26	REF 2
A_{GND}	A27	B27	V-
A_{GND}	A28	B28	A_{GND}
A_{GND}	A29	B29	NC
A_{GND}	A30	B30	NC
A_{GND}	A31	B31	NC
A_{GND}	A32	B32	NC

TDC1014E1C

NC	A	1	A_{GND}
NC	B	2	A_{GND}
NC	C	3	A_{GND}
NC	D	4	A_{GND}
V-	E	5	A_{GND}
REF 2	F	6	A_{GND}
V+	H	7	A_{GND}
REF 1	J	8	A_{GND}
A_{IN}	K	9	A_{GND}
NC	L	10	NC
V_{CC}	M	11	D_{GND}
CONV	N	12	D_{GND}
NC	P	13	D_{GND}
NMINV	R	14	D_{GND}
(MSB) D_1	S	15	D_{GND}
D_2	T	16	D_{GND}
D_3	U	17	D_{GND}
D_4	V	18	D_{GND}
NLINV	W	19	D_{GND}
D_5	X	20	D_{GND}
(LSB) D_6	Y	21	D_{GND}
NC	Z	22	-6V

TDC1014P1C

Functional Description

General Information

The TDC1014 evaluation board consists of four functional sections: Buffer amplifier, reference voltage generator, voltage regulators, and A/D converter. The board is configured for optional input and output data buffers. Analog and digital grounds are separated on the board in order to provide flexibility in system grounding.

Buffer Amplifier

The input buffer amplifier has been designed specifically for standard baseband video. This amplifier is optimized for 75 Ohm 1 Volt p-p input levels. It provides a gain of -1 and offsets the output so that the A/D converter receives a full-scale input signal from 0 to -1 Volt.

The buffer amplifer is capable of driving the input capacitance of the TDC1014 A/D converter. An NPN transistor buffer follows the wideband operational amplifier to provide improved current drive and insure frequency stability.

Components C2 and R10 optimize the performance of the amplifier and are selected as part of the manufacturing process. The buffer amplifier is operated from +12 and -6 Volt regulators which are included on the evaluation board.

Voltage Reference

The reference voltage for the TDC1014 is generated by operational amplifiers U3B and U3C. The system gain is adjusted by varying the reference voltage (R12).

Voltage Regulators

Two voltage regulator circuits are provided on the evaluation board for supplying power to the buffer amplifier. U3D and Q3 provide +12 Volts for the buffer amplifier. U3A and Darlington transistor Q2 provide -6 Volts for the buffer amplifier and the A/D converter. U4 is a 2.5 Volt bandgap voltage reference for both regulators and the voltage reference source.

A/D Converter

The TDC1014 integrated circuit is a 6-bit fully parallel (flash) analog-to-digital (A/D) converter capable of digitizing an input signal at rates up to 25MSPS (MegaSamples Per Second). A single convert (CONV) signal controls the conversion operation of the device. The TDC1014 consists of 63 sampling comparators, encoding logic, and a latched output register. On the rising edge of the CONV signal, the comparators are latched and their outputs are encoded. On the next rising edge of the CONV signal, that data is transferred to the TTL data outputs of the TDC1014.

Output Interface

The TDC1014E1C and P1C boards have provisions for 74S04 Schottky TTL hex inverters for buffering data and improving output drive and fan-out capability. Provision is also made for pull-up resistors on the data outputs. The use of pull-up resistors or data buffers is recommended for optimum results. The data outputs of the TDC1014 are routed directly to the edge connector.

Mechanical Design

The two versions of the evaluation board (P1C, E1C) differ in mechanical configuration. The P1C board is designed to interface with a standard 22/44 contact edge connector. The E1C board is designed to meet the "Eurocard" format and interface with a standard 64 conductor Eurocard (DIN 41612B) connector. Mating edge connectors are included with each evaluation board.

The evaluation board can also accommodate a TDC1007 8-bit A/D converter by using the 64 lead DIP footprint (found outside the perimeter of the TDC1014's 24 lead DIP footprint) with appropriate circuit changes.

The board has a standard 28 pin socket for the TDC1014 integrated circuit. It may be substituted with a "Zero Insertion Force" (ZIF) socket if the board is used as a test fixture.

Power Supplies

The TDC1014 evaluation board operates from three power supply voltages: +5.0, +15, and −15 Volts. The return path for I_{CC} (current from the +5.0 Volt power supply) is D_{GND}. The return paths for I+ and I− (current from the +15 and −15 Volt supplies) is A_{GND}. A user-installed jumper option routes the −6.0 Volt regulator output to the edge connector. The use of all ground pins is recommended. Diodes D_2 through D_6 function as voltage clamps which will prevent damage to the board if improper power supply voltages are applied.

Name	Function	Value	E1C	P1C
V_{CC}	Positive Power Supply	+5V	B18	M
V+	Positive Power Supply	+15V	B24	H
V−	Negative Power Supply	−15V	B37	E
A_{GND}	Analog Ground	0V	A20-A32	1-9
			B22	
			B25	
			B28	
D_{GND}	Digital Ground	0V	A1-A18	11-21
			B2	
			B9	
			B10	
			B16	
			B17	
−6V	Jumper Optional −6 Volt Output	−6V	B1	22

Analog Input

The TDC1014 evaluation board is configured with a nominal input impedance of 75 Ohms and an input voltage range of 1 Volt p-p. The input impedance and input voltage range may be modified by the user. The values of input resistors R1 and R2 determine the input impedance and voltage range of the evaluation board. Suggested values are shown in the Input Resistor Selection Table for various input impedances and voltage ranges.

Name	Function	Value	E1C	P1C
A_{IN}	Analog Input Voltage	See Text	B21	K

Reference

The TDC1014 evaluation board includes circuitry for generating the voltage reference for the A/D converter. In addition, there is an auxilliary −2.0 Volt reference voltage provided. These voltages are available at the edge connectors.

Name	Function	Value	E1C	P1C
REF 1	−1.0 Volt Reference Output	−1V	B23	J
REF 2	Auxilliary −2.0 Volt Output	−2V	B26	F

Control Inputs

Two control inputs are provided on the TDC1014 evaluation board for modifying the format of the output data. When NMINV is tied to a logic "0," the most significant bit of the output data is inverted. When NLINV is tied to a logic "0," the five least significant bits of the output data are inverted. By using these DC controls, the output data can be represented in binary, inverse binary, two's complement, or inverse two's complement formats. Output data versus input voltage and control input state is illustrated in the Output Coding Table.

Name	Function	Value	E1C	P1C
NMINV	Not Most Significant Bit INVert	TTL	B13	R
NLINV	Not Least Significant Bit INVert	TTL	B6	W

Convert

The comparators in the TDC1014 A/D converter are latched within 10ns (t_{STO}) after the rising edge of the CONV signal. Delays through the buffer amplifier are not included in t_{STO}. Output data is latched on the next rising edge of the CONV signal. Note that there are minimum pulse width (t_{PWH}, t_{PWL}) requirements on the waveshape of the CONV signal.

Name	Function	Value	E1C	P1C
CONV	A/D Clock Input	TTL	B15	N

Data Outputs

The outputs of the TDC1014 evaluation board are TTL compatible and capable of driving four low-power Schottky unit loads (54/74LS). Data remains valid after the rising edge of the CONV signal for a minimum time, t_{HO}, and the next data becomes valid after a maximum time of t_D. The evaluation board has provisions for optional data buffers (74S04). When installing these circuits, it is necessary to open traces on the board which connect the inverter inputs to their corresponding outputs.

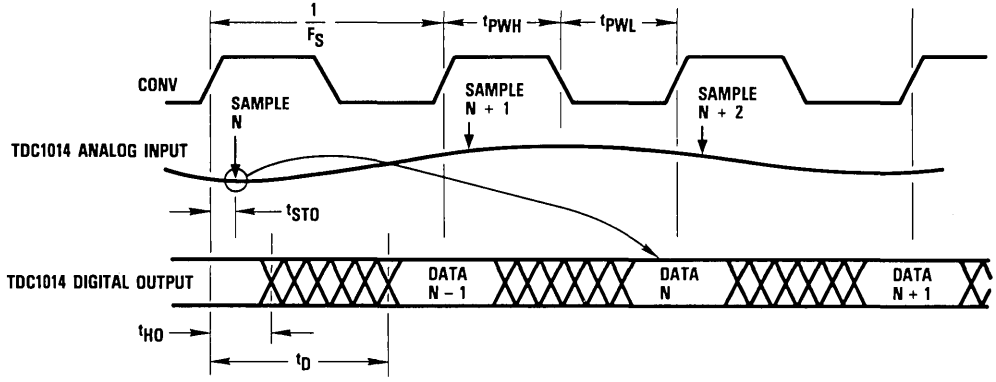
Name	Function	Value	E1C	P1C
D_1 (MSB)	Most Significant Data Bit	TTL	B12	S
D_2		TTL	B11	T
D_3		TTL	B8	U
D_4		TTL	B7	V
D_5		TTL	B5	X
D_6 (LSB)	Least Significant Data Bit	TTL	B4	Y

No Connects

There are several pins or contacts to the TDC1014 evaluation board that have no connection to the circuit. These pins may be left open.

Name	Function	Value	E1C	P1C
NC	No Connect	Open	A19	10
			B19	A, B
			B20	C, D
			B29 - B32	L
			B3	Z
			B14	P

Figure 1. Timing Diagram



Absolute maximum ratings (beyond which the board may be damaged) [1]

Power Supply Voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V+ (measured to A_{GND})	−0.5 to +18.0V
V− (measured to A_{GND})	+0.5 to −18.0V
A_{GND} (measured to D_{GND})	+0.5 to −0.5V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
A_{IN} (measured to A_{GND})	+4.5 to −4.5V [6]

Output

Applied voltage	−0.5 to +5.5V [2,5]
Applied current, externally forced	−1.0 to +6.0mA [3,4,5]
Short circuit duration (single output in HIGH state to D_{GND})	1 sec [5]

Temperature

Operating, ambient	−40 to 90°C
Storage	−65 to 150°C

Note:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.
5. Applies to TDC1014 IC only; excludes optional output data buffers.
6. With input impedance of 75 Ohms, as supplied.

Operating conditions

Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage (Measured to D_{GND})	4.75	5.0	5.25	V
V+	Positive Supply Voltage (Measured to A_{GND})	14.25	15.0	15.75	V
V−	Negative Supply Voltage (Measured to A_{GND})	−14.25	−15.0	−15.75	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0.0	+0.1	V
t_{PWL}	CONV Pulse Width, LOW [1]	19			ns
t_{PWH}	CONV Pulse Width, HIGH [1]	15			ns
V_{IL}	Input Voltage, Logic LOW			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			V
I_{OL}	Output Current, Logic LOW [2]			4.0	mA
I_{OH}	Output Current, Logic HIGH [2]			−400	μA
A_{IN}	Input Voltage Range [3]	0.0		1.0	V
T_A	Ambient Temperature, Still Air	0		70	°C

Notes:

1. Applies to the TDC1014 IC only.
2. TDC1014 IC only; excludes optional output data buffers.
3. 75 Ω input impedance, as supplied, U2 offset zeroed.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Min	Max	Units
I_{CC}	Supply Current	V_{CC} = MAX		100	mA
$I+$	Positive Supply Current	V+ = MAX		40	mA
$I-$	Negative Supply Current	V− = MAX		−300	mA
Z_{IN}	Input Impedance		70	80	Ohms
I_{IL}	Input Current, Logic LOW [1]	V_{CC} = MAX, VI = 0.5V		−2.0	mA
I_{IH}	Input Current, Logic HIGH [1]	V_{CC} = MAX, VI = 2.4V		75	μA
V_{OL}	Output Voltage, Logic LOW [1]	V_{CC} = MIN, I_{OL} = 4mA		0.5	V
V_{OH}	Output Voltage, Logic HIGH [1]	V_{CC} = MIN, I_{OH} = −400 μA	2.4		V

Note:

1. Applies to the TDC1014 IC only; excludes optional output data buffers.

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Min	Max	Units
F_S	Maximum Conversion Rate	V_{CC} = MIN, V_{EE} = MIN	25		MSPS
t_{STO}	Sampling Time Offset [2]	V_{CC} = MIN, V_{EE} = MIN	−2	10	ns
t_D	Output Delay [3]	V_{CC} = MIN, V_{EE} = MIN		35	ns
t_{HO}	Output Hold Time [3]	V_{CC} = MIN, V_{EE} = MIN	10		ns

Note:

1. All parameters apply to the TDC1014 IC only.
2. Excludes delay from buffer amplifier, U2.
3. Excludes optional output data buffers.

TDC1014J7C performance characteristics within specified operating conditions [1]

Parameter		Min	Max	Units
E_{LI}	Linearity Error Integral, Independent		0.4	%
E_{LD}	Linearity Error Differential		0.4	%
BW	Bandwidth, Full power Input	12		MHz

Note:

1. Items listed in this table are for the A/D converter only. Contributions to these parameters for the buffer amplifier are not significant.

Output Coding[1]

Input Voltage	Binary		Two's Complement	
	True	Inverted	True	Inverted
	NMINV = 1 NLINV = 1	0 0	0 1	1 0
0.0000	000000	111111	100000	011111
+0.0159	000001	111110	100001	011110
•	•	•	•	•
•	•	•	•	•
+0.4920	011111	100000	111111	000000
+0.5079	100000	011111	000000	111111
•	•	•	•	•
•	•	•	•	•
+0.9841	111110	000001	011110	100001
+1.0000	111111	000000	011111	100000

Note:

1. Input voltage range is from 0.00 to +1.00 Volt, no offset added. (Input voltages are at code centers and the voltage offset of the buffer amplifier is nulled.)

Calibration

The evaluation board is calibrated by adjusting the offset and gain trim resistors, R11 and R12. Offset can be calibrated when a voltage corresponding to 1/2 LSB greater than "zero-scale" is applied to the board input. The "OFFSET" potentiometer is then adjusted to a point where the output data toggles between "000000" and "000001." Gain is calibrated by applying a voltage 1/2 LSB less than full-scale and adjusting the "GAIN" pot until the output data toggles between "111110" and "111111."

Input Resistor Selection Table (values in Ohms)

	Input Voltage Range									
Z_{IN}	1V		2V		4V		5V		10V	
	R1	R2	R1	R2	R1	R2	R1	R2	R1	R2
50	24.9	25.5	37.4	12.7	43.2	6.19	45.3	4.99	47.5	2.49
75	37.4	39.2	56.2	19.1	64.9	9.53	68.1	7.50	71.5	3.74
93	46.4	48.7	69.8	23.7	80.6	11.8	84.5	9.31	88.7	4.64
1K	499	1000	750	332	866	143	909	110	953	52.3

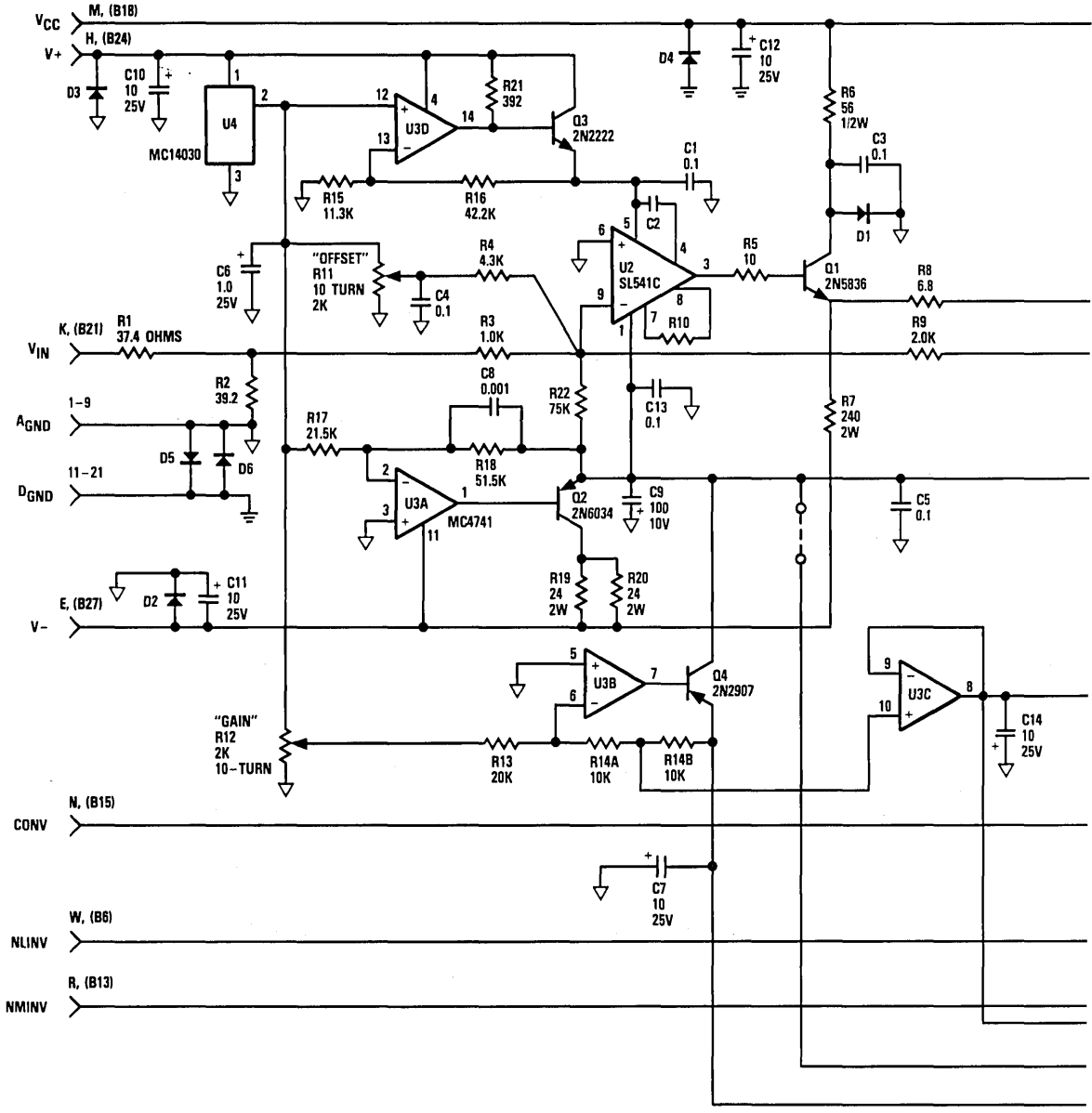
For input voltage ranges and input impedances not covered by the Input Resistor Selection Table, the following formulas may be used to calculate R1 and R2:

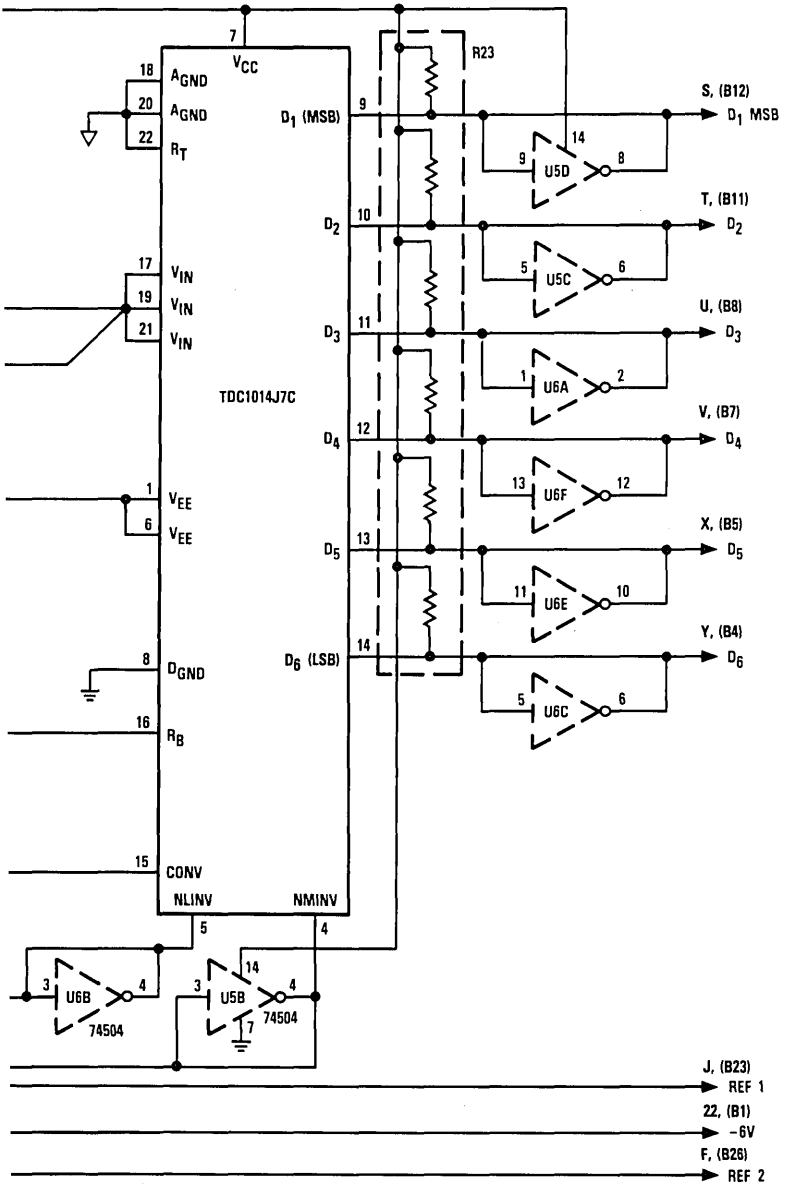
$$R2 = \frac{1}{\left(\frac{2VR}{Z_{IN}}\right) - \frac{1}{1000}}$$

$$R1 = Z_{IN} - \left(\frac{1000\ R2}{R2 + 1000}\right)$$

where VR is the desired input voltage range of the board, Z_{IN} is the desired input impedance of the board, and the constant value 1000 is given by the value of R3.

Schematic of Evaluation Board




7
V_{CC}
18
A_{GND}
20
A_{GND}
22
R_T
17
V_{IN}
19
V_{IN}
21
V_{IN}
TDC1014J7C
1
V_{EE}
6
V_{EE}
8
D_{GND}
16
R_B
15
CONV
NLINV
NMINV
5
4
D_1 (MSB)
9
D_2
10
D_3
11
D_4
12
D_5
13
D_6 (LSB)
14
R23
U5D
U5C
U6A
U6F
U6E
U6C
U6B
U5B
74504
74504
S, (B12)
D_1 MSB
T, (B11)
D_2
U, (B8)
D_3
V, (B7)
D_4
X, (B5)
D_5
Y, (B4)
D_6
J, (B23)
REF 1
22, (B1)
−6V
F, (B26)
REF 2

E

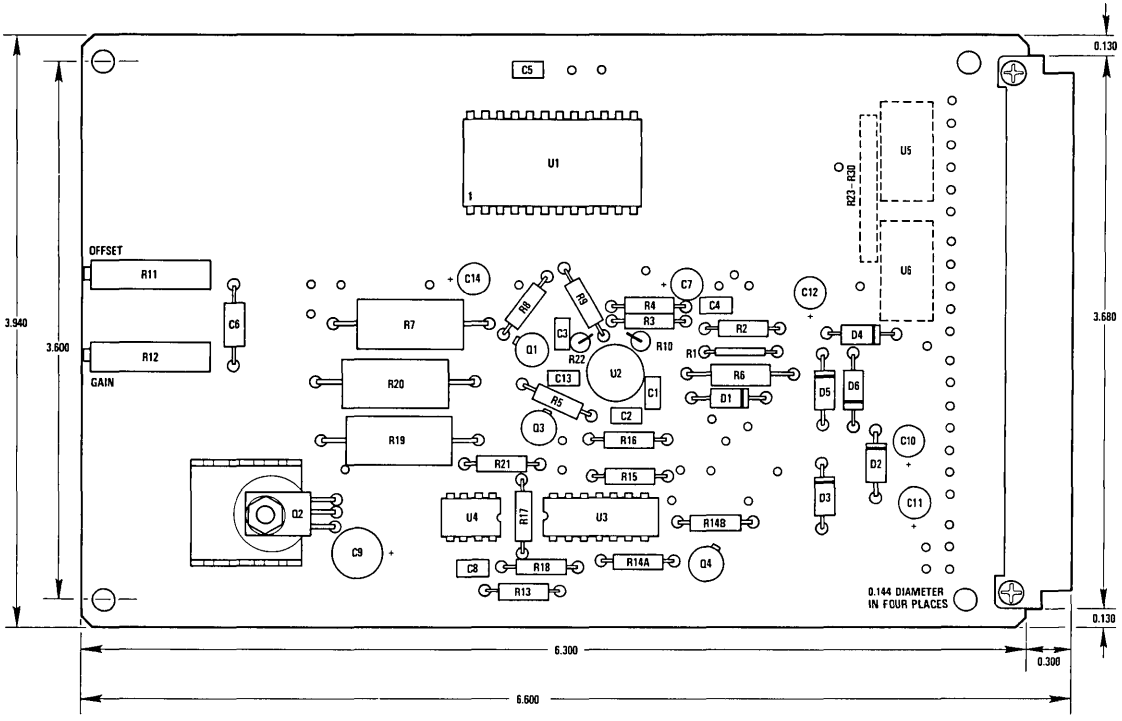
Notes for Schematic of Evaluation Board

1. All capacitor values are in microFarads (μF).
2. All capacitor voltage ratings are 50WVDC unless otherwise noted.
3. All resistors are 1/8W unless otherwise noted.
4. All resistor values are in Ohms.
5. All diodes are 1N4001.
6. Values for C2 and R10 are selected during manufacturing.
7. R23 is an eight-resistor SIP, 2.2kOhms 1/4W (not supplied).
8. Edge connector numbers in parenthes (B18, etc.) are for TDC1014E1C.
9. A_{GND} pins for TDC1014E1C are B22, B25, B28, A20 to A32.
10. D_{GND} pins for TDC1014E1C are B2, B9, B10, B16, B17, A1 to A18.

Miscellaneous

Edge connector for mating with TDC1014P1C	TRW Cinch 271-22-30-1690
Eurocard connector mounted on TDC1014E1C	Winchester 64P-6033-0430, DIN 41612B
Eurocard connector for mating with TDC1014E1C	Winchester 64S-6033-0422-1, DIN 41612B
Heatsink for Q2	Thermalloy 6D738
Mica washer for Q2	Delbert Blinn 500-125-2
Stitch-weld pins for R1 and R2	Moore Systems 700508

TDC1014E1C Assembly

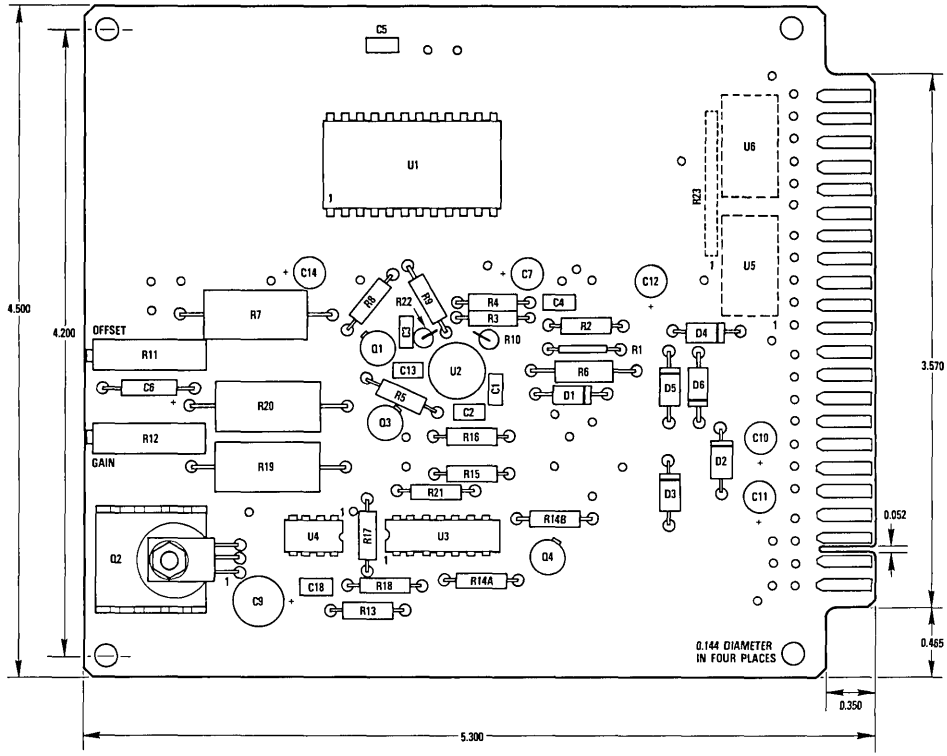


Notes:

1. R23, U5 and U6 not supplied.
2. All dimensions in inches.

E

TDC1014P1C Assembly



Notes:

1. R23, U5 and U6 not supplied.
2. All dimensions in inches.

Ordering Information

Product Number	Description	Order Number
TDC1014E1C	Eurocard Format Board With A/D Converter	TDC1014E1C
TDC1014P1C	22/44 Edge Format Board With A/D Converter	TDC1014P1C

TDC1019E1C

A/D Converter Evaluation Board
9-Bit, 15MSPS

The TDC1019 evaluation board is a fully assembled and tested circuit board designed to aid in the evaluation of TRW's TDC1019 9-bit video analog-to-digital (A/D) converter. The board contains circuitry for buffering the input signal, generating reference voltages, regulating supply voltages, and buffering output data. All digital inputs and outputs are ECL compatible. Provisions are made for gain, offset, and linearity adjustments. The board requires -5.2 and ±15 Volt power supplies.

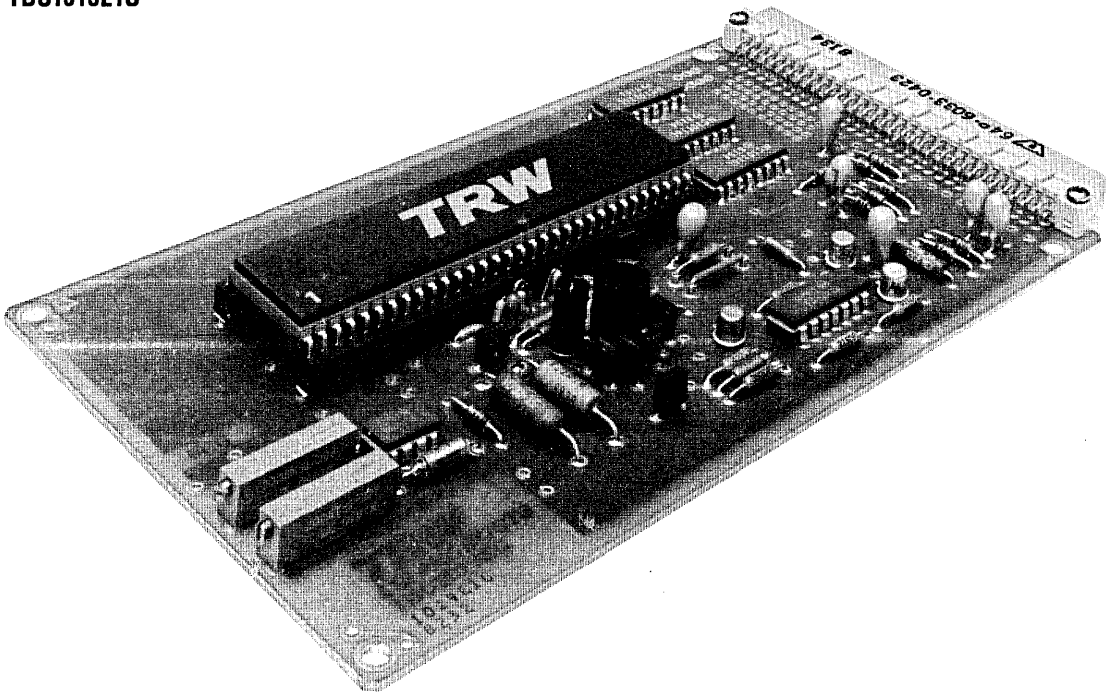
Features

- Includes TDC1019 9-Bit A/D Converter
- User-Selectable Input Impedance
- User-Selectable Input Voltage Range
- Unipolar Or Bipolar Operation
- Gain And Offset Calibration Controls
- Mid-Scale Linearity Adjustment Control
- Operates From ±15 and -5.2 Volt Power Supplies
- Differential ECL Output Buffers
- Low Profile Eurocard Format

Applications

- System Prototyping Aid
- Incoming Inspection Test Fixture
- Evaluation Of TDC1019 A/D Converter

TDC1019E1C



E

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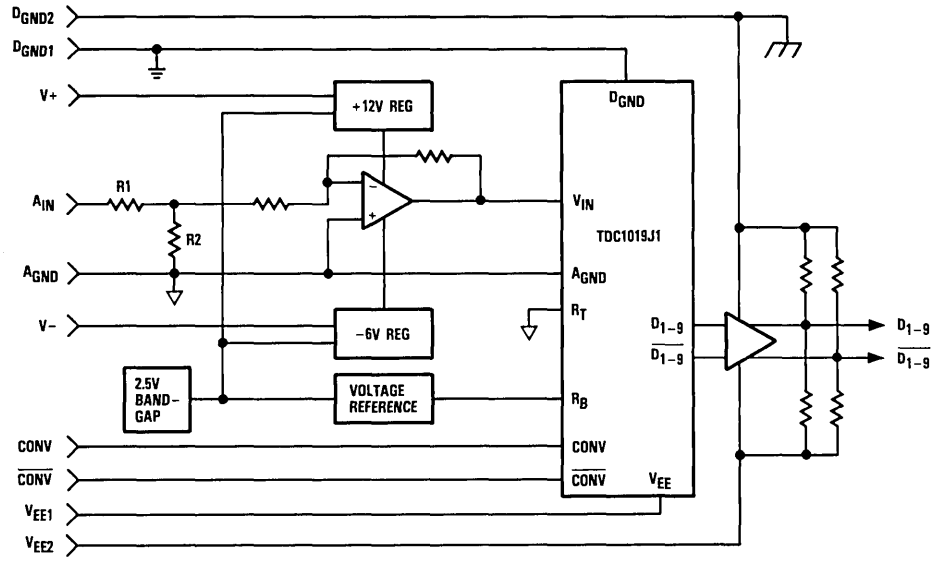
Functional Block Diagram



Pin Assignments

D_{GND2}	A1	B1	D_{GND2}
$\overline{CONV}$	A2	B2	CONV
(LSB) $\overline{D_9}$	A3	B3	D_9 (LSB)
$\overline{D_8}$	A4	B4	D_8
$\overline{D_7}$	A5	B5	D_7
$\overline{D_6}$	A6	B6	D_6
$\overline{D_5}$	A7	B7	D_5
$\overline{D_4}$	A8	B8	D_4
$\overline{D_3}$	A9	B9	D_3
$\overline{D_2}$	A10	B10	D_2
(MSB) $\overline{D_1}$	A11	B11	D_1 (MSB)
D_{GND2}	A12	B12	NC
D_{GND2}	A13	B13	NC
D_{GND2}	A14	B14	V_{EE2}
D_{GND2}	A15	B15	NC
D_{GND2}	A16	B16	NC
D_{GND2}	A17	B17	D_{GND2}
D_{GND1}	A18	B18	NC
D_{GND1}	A19	B19	V_{EE1}
D_{GND1}	A20	B20	NC
D_{GND1}	A21	B21	D_{GND1}
A_{GND}	A22	B22	NC
A_{GND}	A23	B23	V_{RBS}
A_{GND}	A24	B24	V_{REF}
A_{GND}	A25	B25	NC
A_{GND}	A26	B26	A_{IN}
A_{GND}	A27	B27	-6V
A_{GND}	A28	B28	V+
A_{GND}	A29	B29	NC
A_{GND}	A30	B30	V-
A_{GND}	A31	B31	Q1 SUPPLY
A_{GND}	A32	B32	NC

TDC1019E1C, E2C

Functional Description

General Information

The TDC1019 evaluation board consists of four circuit blocks: the buffer amplifier, reference voltage generator, voltage regulators, and A/D converter. The board also contains differential ECL output data buffers. Analog and digital grounds are separated on the board in order to provide flexibility in system grounding.

Buffer Amplifier

The input buffer amplifier has been designed specifically for standard baseband video. This amplifier is optimized for a 75 Ohm, 1 Volt p-p input level. It has a gain factor of -2 and can offset the output so that the A/D converter receives a full-scale input signal of 0 to -2 Volts.

The buffer amplifier is designed to drive the input capacitance of the A/D converter. An NPN transistor buffer follows the wideband operational amplifier to provide improved current drive capability and insure frequency stability.

Components C2, C8, C18, and R10 optimize the performance of the amplifier and are selected during the manufacturing process. The buffer amplifier is operated from +12 and -6 Volt regulators which are included on the evaluation board.

Voltage Reference

The reference Voltage for the TDC1019 is generated by operational amplifier U3A. This amplifier is buffered by PNP transistor, Q4, in order to supply the reference current for the A/D converter. Gain is adjusted by varying R12 which changes the reference voltage. The sense tap at the bottom of the reference resistor chain is used inside the loop of U3A to minimize the offset Voltage caused by parasitic resistances associated with the RB pin of the TDC1019.

Voltage Regulators

Two voltage regulator circuits are provided on the evaluation board to supply power to the buffer amplifier. U3C and Q3 provide +12 Volts while U3D and transistor Q2 provide -6 Volts. Both regulators and the voltage reference circuit are referred to the output of U4, a 2.5 Volt bandgap voltage reference device.

A/D Converter

The TDC1019 integrated circuit is a 9-bit fully parallel (flash) analog-to-digital (A/D) converter capable of digitizing an input signal at rates up to 18MSPS (MegaSamples Per Second). TDC1019 evaluation boards come with the standard 15MSPS A/D converter installed. A speed selected (-1) version of the TDC1019 is capable of 18MSPS operation. A differential ECL CONVert (CONV) signal controls the conversion operation of the device. The TDC1019 consists of 512 sampling comparators, encoding logic, and a latched output register. On each rising edge of the CONV signal, the comparators are latched and their outputs encoded into binary data. On the next rising edge of the CONV signal, the encoded result is transferred to the differential ECL data outputs of the A/D converter.

Output Interface

The evaluation board includes differential ECL line receivers (MC10116) for buffering the output data. Provisions are also made for terminating all data outputs. Termination resistors are not included with the board.

Mechanical Design

The board is designed to meet standard "Eurocard" format and interface with a standard 64 conductor Eurocard connector. A DIN 41612B mating connector is included with each evaluation board for the user's convenience.

A standard 64 pin socket for the TDC1019 integrated circuit is used on the board. The board is arranged so that this socket may be replaced by a "Zero Insertion Force" (ZIF) socket if the evaluation board is used as a test fixture. A recommended ZIF socket is made by Textool Inc, part number 264-4493-00-0602.

Power Supplies

The TDC1019 evaluation board operates from three power supplies, -5.2, +15, and -15 Volts (V_{EE1} and V_{EE2}, V+, and V-). Power to the A/D is supplied by V_{EE1} while the ECL output buffers are powered from V_{EE2}. These are kept separate on the board but may be connected to the same power source. The return path for I_{EE1} (current from V_{EE1}) is D_{GND1}. The return path for I_{EE2} (current from V_{EE2}) is D_{GND2}. The return path for I+ and I- (current from V+ and V-) is A_{GND}. It is recommended that all ground pins be used. The output of the -6 Volt regulator is routed to the edge connector for the user's convenience. Power for the collector of Q1 may be supplied to the board separately by breaking jumper A-B and using egde connector pin B31. Diodes D_2 through Dg function as voltage clamps which prevent damage to the board should improper power supplies be applied.

Name	Function	Value	E1C
V+	Positive Analog Power Supply	15V	B28, B31
V-	Negative Analog Power Supply	-15V	B30
V_{EE1}	Negative Supply For A/D Converter	-5.2V	B19
V_{EE2}	Negative Supply For Data Buffers	-5.2V	B14
A_{GND}	Analog Ground	0.0V	A22-A32
D_{GND1}	Digital Ground	0.0V	A18-A21
			B21
D_{GND2}	Digital Ground For Data Buffers	0.0V	A1, B1
			A12-A17
			B17
-6.0	-6 Volt Regulator Output	-6.0V	B27
Q1 Supply	Optional Positive Power Supply	15V	B31

Analog Input

The TDC1019 evaluation board is configured with a nominal input impedance of 75 Ohms and an input voltage range of 1 Volt p-p. Both input impedance and input voltage range may be changed. The values of input resistors R1 and R2 determine the input impedance and voltage range of the evaluation board. Suggested values for various input impedances and voltage ranges are shown in the Input Resistor Selection Table.

Name	Function	Value	E1C
A_{IN}	Signal Input To Board	See Text	B26

Reference

The evaluation board contains all of the circuitry needed for generation of a stable reference voltage for the A/D converter. The reference voltage and reference sense points are accessible through the edge connector.

Name	Function	Value	E1C
V_{REF}	Reference Output Voltage	−2.0V	B24
V_{RBS}	Reference Sense Output	−2.0V	B23

Convert

The TDC1019 A/D converter is sampled within 10ns (t_{STO}) of the rising edge of the CONV signal. Delays through buffer amplifier U2 are not included in t_{STO}. Output data is latched on the next rising edge of the CONV signal. Note that there are minimum pulse width (t_{PWH}, t_{PWL}) requirements on the waveshape of the CONV signal.

Name	Function	Value	E1C
CONV	CONVert Command Input	ECL	B2
$\overline{CONV}$	CONVert Command Input (Complement)	ECL	A2

Digital Outputs

The outputs of the TDC1019 evaluation board are differential ECL compatible. Provisions are made for terminating resistors for each data output. Data remains valid after the rising edge of the CONV signal for a minimum time, t_{HO}, and the next data becomes valid after a maximum time of t_D.

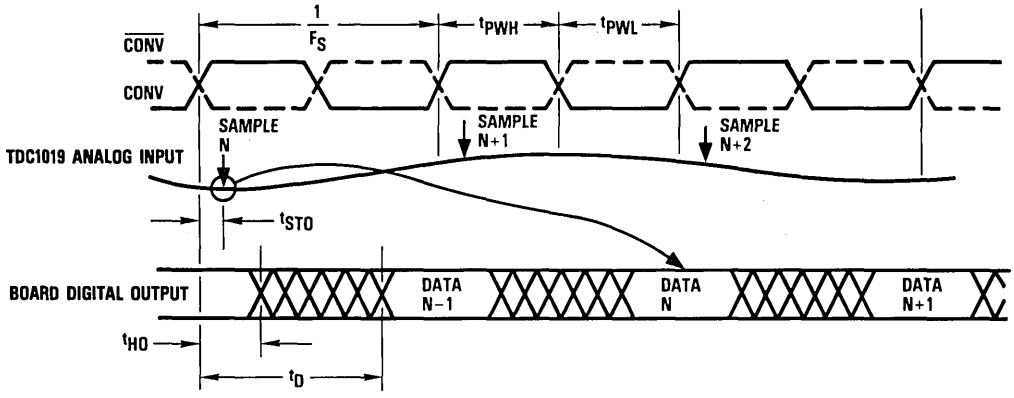
Name	Function	Value	E1C
D1 (MSB)	Most Significant Data Output	ECL	B11
$\overline{D_1}$ (MSB)	Most Significant Data Output (Inv)	ECL	A11
D_2		ECL	B10
$\overline{D_2}$		ECL	A10
D_3		ECL	B9
$\overline{D_3}$		ECL	A9
D_4		ECL	B8
$\overline{D_4}$		ECL	A8
D_5		ECL	B7
$\overline{D_5}$		ECL	A7
D_6		ECL	B6
$\overline{D_6}$		ECL	A6
D_7		ECL	B5
$\overline{D_7}$		ECL	A5
D_8		ECL	B4
$\overline{D_8}$		ECL	A4
D_9 (LSB)	Least Significant Data Output	ECL	B3
$\overline{D_9}$ (LSB)	Least Significant Data Output (Inv)	ECL	A3

No Connects

There are several pins on the TDC1019 evaluation board that have no connections to the circuit. These pins may be left open.

Name	Function	Value	E1C
NC	No Connection	Open	B12, B13 B15, B16 B18, B20 B22, B25 B29, B32

Figure 1. Timing Diagram



Absolute maximum ratings (beyond which the board may be damaged) [1]

Power Supply Voltages

V_{EE1} (measured to D_{GND1})	+0.5 to −7.0V
V_{EE2} (measured to D_{GND2})	+0.5 to −7.0V
V+ (measured to A_{GND})	−0.5 to +18.0V
V− (measured to A_{GND})	+0.5 to −18.0V
V_{AGND} (measured to D_{GND1})	+0.5 to −0.5V
V_{DGND2} (measured to D_{GND1})	+0.5 to −0.5V

Input Voltages

CONV, $\overline{CONV}$ (measured to D_{GND})	+0.5 to −7.0V
A_{IN} (measured to A_{GND})	+4.5 to −4.5V [2]

Temperature

Operating ambient	−40 to 90°C
Storage	−65 to 150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. With input impedance of 75 Ohms, as supplied.

Operating conditions

Parameter		Min	Nom	Max	Units
V_{EE1}	Negative Power Supply (measured to D_{GND1})	−4.9	−5.2	−5.5	V
V_{EE2}	Negative Power Supply (measured to D_{GND2})	−4.9	−5.2	−5.5	V
V+	Positive Power Supply (measured to A_{GND})	+14.25	+15.0	+15.75	V
V−	Negative Power Supply (measured to A_{GND})	−14.25	−15.0	−15.75	V
V_{AGND}	Analog Ground (measured to D_{GND1})	−0.1	0.0	+0.1	V
V_{DGND2}	Digital Ground (measured to D_{GND1})	−0.1	0.0	+0.1	V
t_{PWL}	CONV Pulse Width LOW [1]	25			ns
t_{PWH}	CONV Pulse Width HIGH [1]	32			ns
V_{IL}	Input Voltage Logic LOW [1]			−1.4	V
V_{IH}	Input Voltage Logic HIGH [1]	−1.0			V
A_{IN}	Input Voltage Range [2]	0.0		1.0	V
T_A	Ambient Temperature Range, Still Air	0		+50	°C

Notes:

1. Applies to the TDC1019J1C integrated circuit only.
2. 75 Ohm input impedance, as supplied, U2 offset zeroed.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Min	Max	Units
I_{EE1}	Negative Supply Current	V_{EE1} = MAX[1]		-850	mA
I_{EE2}	Negative Supply Current	V_{EE2} = MAX[2]		-70	mA
I+	Positive Supply Current	V+ = MAX		125	mA
I-	Negative Supply Current	V- = MAX		-150	mA
Z_{IN}	Input Impedance		70	80	Ohms
V_{OL}	Output Voltage, Logic LOW	V_{EE1}=NOM[2]		-1.85	V
V_{OH}	Output Voltage, Logic HIGH	V_{EE1}=NOM[2]	-0.81		V

Notes:

1. Applies to the TDC1019 integrated circuit only.
2. Applies to the MC10116s only, without termination.

Switching characteristics within specified operating conditions[1]

Parameter		Test Conditions	Min	Max	Units
F_S	Maximum Conversion Rate	V_{EE1} = MIN	15		MSPS
t_{STO}	Sampling Time Offset[1,2]	V_{EE1} = MIN	0	10	ns
t_D	Output Delay Time[3]	V_{EE1} = MIN		39	ns
t_{HO}	Output Data Hold Time[3]	V_{EE1} = MIN	7		ns

Note:

1. Applies to the TDC1019 integrated circuit only.
2. Delays through buffer amplifier U2 not included.
3. Delays through data buffers U7, U8, and U9 are included.

TDC1019J1C performance characteristics within specified operating conditions[1]

Parameter		Test Conditions	Min	Max	Units
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB} = NOM, VRM unadjusted		0.3	%
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB} = NOM, VRM adjusted		0.15	%
E_{LD}	Linearity Error Differential	V_{RT}, V_{RB} = NOM		0.15	%
BW	Bandwidth Full Power Input		5		MHz
DP	Differential Phase	NTSC @ 4x Color Subcarrier, VRM adjusted		1.0	degrees
DG	Differential Gain	NTSC @ 4x Color Subcarrier, VRM adjusted		2.0	%

Note:

1. Items listed in this table are for the A/D Converter only. Contributions to these parameters from the buffer amplifier are not significant.

Calibration

The evaluation board is calibrated by adjusting the "OFFSET" and "GAIN" trim resistors, R11 and R12. Offset is calibrated when a voltage corresponding to 1/2 LSB greater than "zero-scale" is applied to the board input. The "OFFSET" potentiometer is then adjusted until the output data toggles between "000000000" and "000000001." Gain is calibrated by applying a voltage 1/2 LSB less than full-scale and adjusting the "GAIN" potentiometer until the output data toggles between "111111110" and "111111111." A linearity adjustment potentiometer ("MID", R5) is included on the board to provide the user with a fine adjustment of the integral linearity of the A/D converter.

1019E1C Output Coding Table [1]

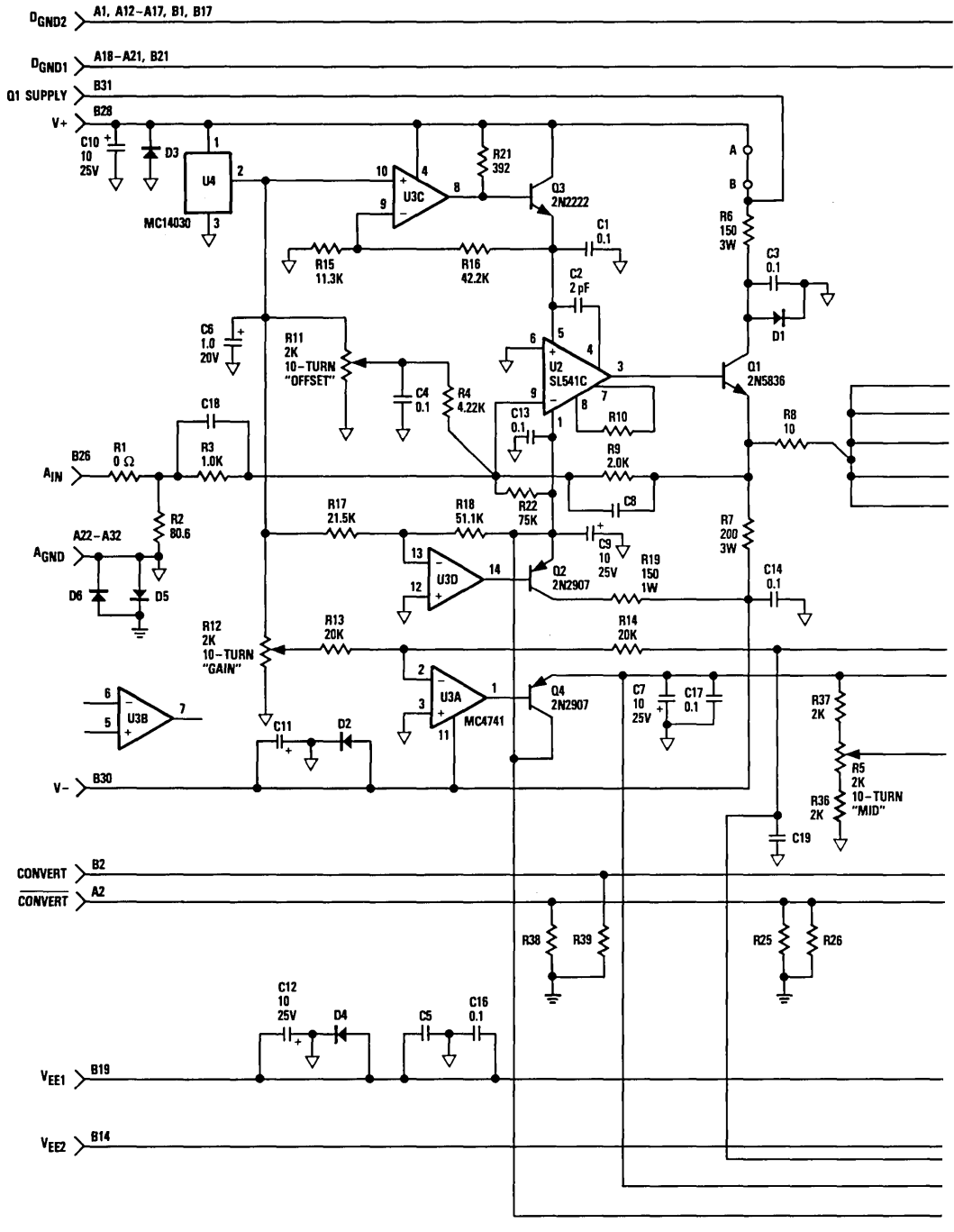
	OVF[2]	$\overline{OVF}$[2]	D_{1-9}	$\overline{D_{1-9}}$
-0.00195	1	0	000000000	111111111
0.000	0	1	000000000	111111111
+0.00195	0	1	000000001	111111110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
+0.4990	0	1	0111111111	100000000
+0.50097	0	1	1000000000	011111111
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
+.99804	0	1	111111110	000000001
+1.000	0	1	111111111	000000000
+1.00192	0	1	111111111	000000000

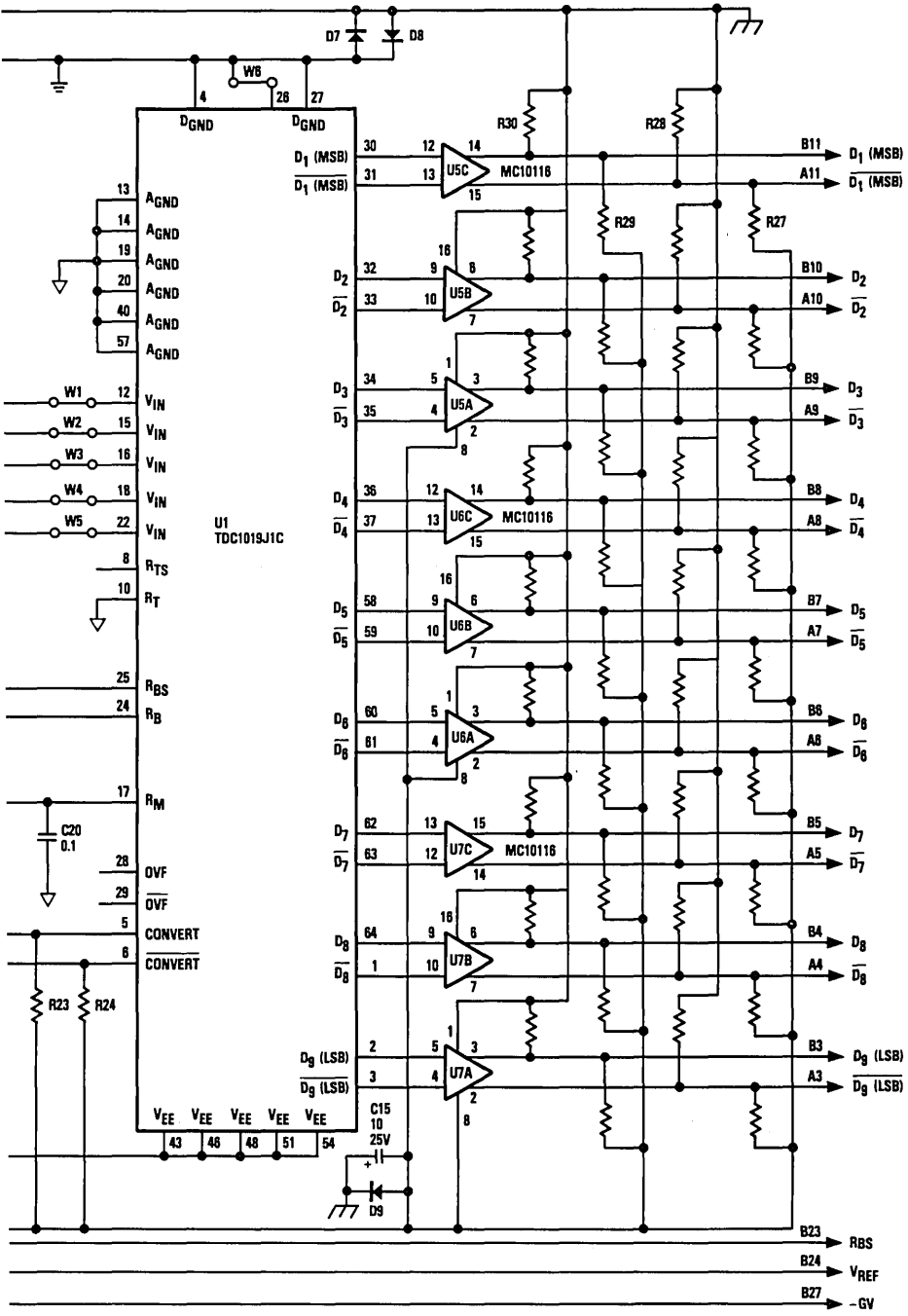
Note:

1. Input voltage range is from 0.00 to +1.00 Volt, no offset added. (Input voltages are at code centers and the voltage offset of the buffer amplifier is nulled.)
2. Applies to TDC1019J1C integrated circuit only (Pins 28 and 29).

E

Schematic of Evaluation Board




D7
D8
W6
4
26
27
DGND
DGND
U1
TDC1019J1C
AGND
VIN
W1
W2
W3
W4
W5
RTS
RT
RBS
RB
RM
C20
0.1
OVF
CONVERT
R23
R24
VEE
C15
10
25V
D9
U5C
U5B
U5A
U6C
U6B
U6A
U7C
U7B
U7A
MC10116
R30
R28
R29
R27
D1 (MSB)
D2
D3
D4
D5
D6
D7
D8
D9 (LSB)
B11
A11
B10
A10
B9
A9
B8
A8
B7
A7
B6
A6
B5
A5
B4
A4
B3
A3
B23
RBS
B24
VREF
B27
-GV

Notes for Schematic of Evaluation Board

1. All capacitor values are in microFarads (μF).
2. All capacitor voltage rating are 50WVDC unless other wise noted.
3. All resistors are 1/8W unless otherwise noted.
4. All resistor values are in Ohms.
5. All diodes are 1N4001 unles otherwise specified.
6. Values for C2, C8, C18 and R10 are selected during manufacturing.
7. R27 through R30 are eight-resistor SIPs, 2.2kOhms 1/4W (not supplied).

Miscellaneous

Eurocard Connector mounted on TDC1019E1C	Winchester 64P-6033-0430, DIN 41612B
Eurocard Connector for mating TDC1019E1C	Winchester 64S-6033-0422-1, DIN 41612B
64-pin IC socket for U1	Robinson-Nugent ICN-649-S5-G1 or ICN-649-S5-U1
Stitch-Weld pins for R1 and R2	Moore Systems 700508

Input Resistor Selection Table (Values in Ohms)

Input Voltage Range

Z_{IN}	1V		2V		4V		5V		10V	
	R1	R2	R1	R2	R1	R2	R1	R2	R1	R2
50	0	52.3	24.9	24.3	37.4	12.7	40.2	10	45.3	4.99
75	0	80.6	37.4	39.2	56.2	19.1	60.4	15.4	68.1	7.5
93	0	102	46.4	48.7	69.8	23.7	75	19.1	84.5	9.31
1k	0	open	499	1k	750	332	806	249	909	110

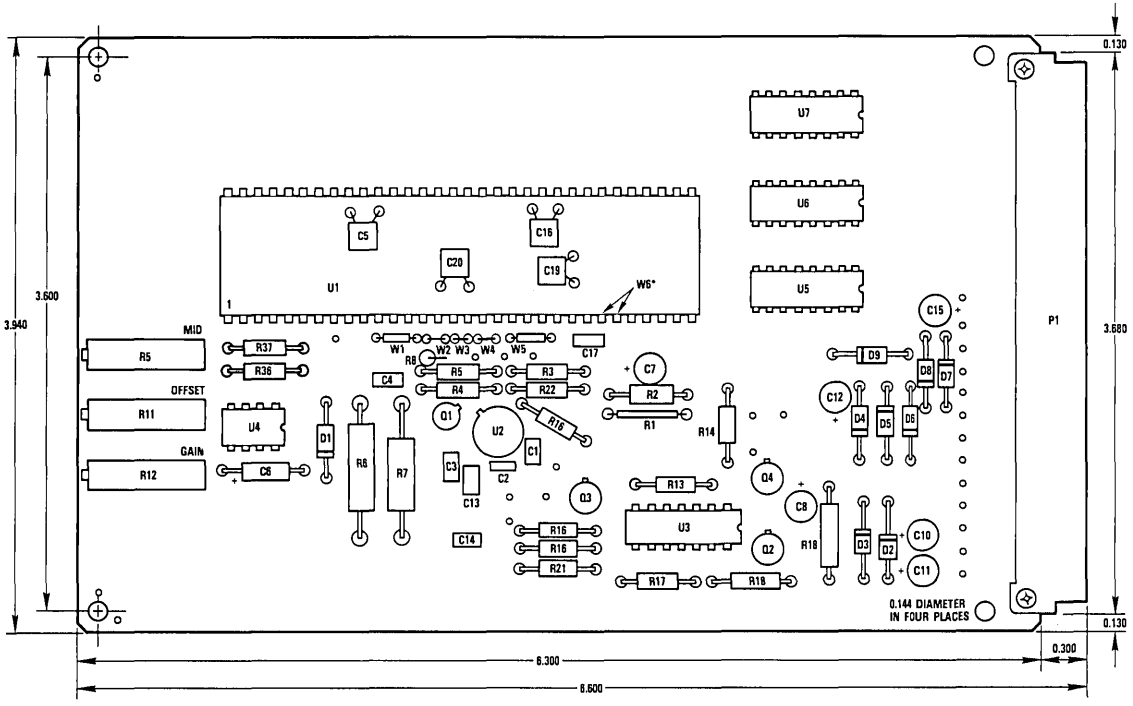
For input voltage ranges and input impedances not covered by the Input Resistor Selection Table, the following formulas may be used to calculate R1, and R2:

$$R2 = \frac{1}{\left(\frac{VR}{Z_{IN}}\right) - \frac{1}{1000}}$$

$$R1 = Z_{IN} - \left(\frac{1000\ R2}{R2 + 1000}\right)$$

Where VR is the desired input voltage range of the board, Z_{IN} is the desired input impedance of the board, and the constant value 1000 is given by the value of R3.

TDC1019E1C Assembly



Note: 1. *These two pins wired together to make W6.

Ordering Information

Product Number	Description	Order Number
TDC1019E1C	Eurocard Format Board With A/D Converter	TDC1019E1C

E

TDC1025E1C

High–Speed A/D Converter Evaluation Board
8–Bit, 50MSPS

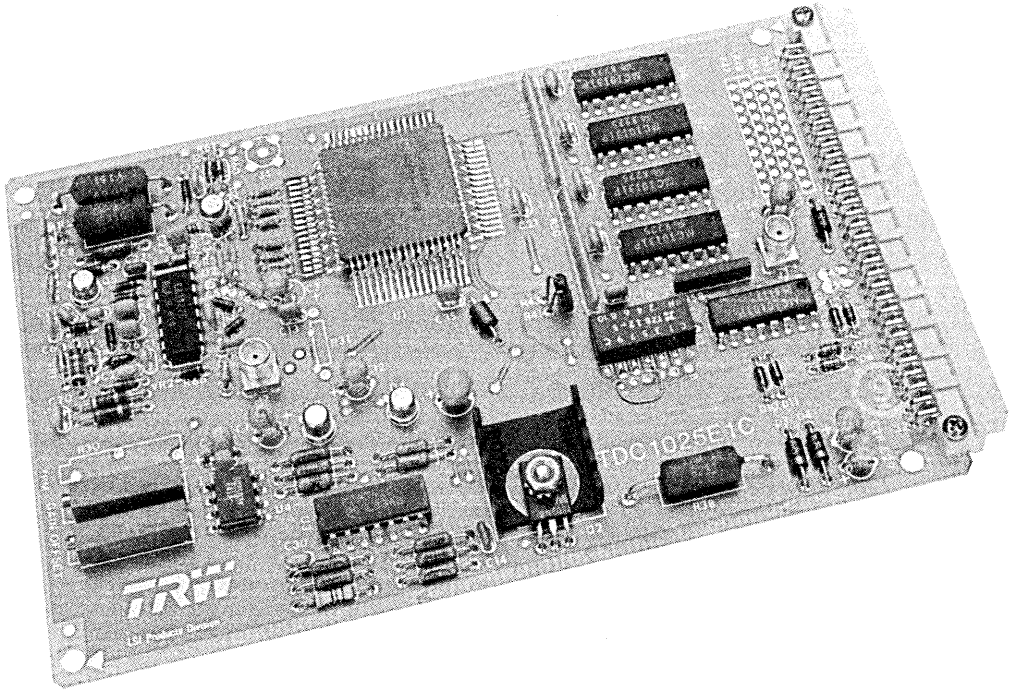
The TDC1025 evaluation board is a fully assembled and tested circuit board designed to aid in the evaluation of TRW's TDC1025 8–bit, high–speed analog–to–digital (A/D) converter. The board contains circuitry for buffering the input signal, generating reference voltages, regulating supply voltages, and latching output data. All digital inputs and outputs are ECL compatible. Provisions are made for gain and offset adjustments. The board requires –5.2 and ±15 Volt power supplies.

Features:

- Includes TDC1025 8–Bit A/D Converter
- User Selectable Input Impedance
- User Selectable Input Voltage Range
- Adjustable Offset For Unipolar Or Bipolar Operation
- Gain And Offset Calibration Controls
- Differential ECL Output Data
- Eurocard Format

Applications

- Evaluation Of TDC1025 A/D Converter
- System Prototyping Aid
- Incoming Inspection Test Fixture



E

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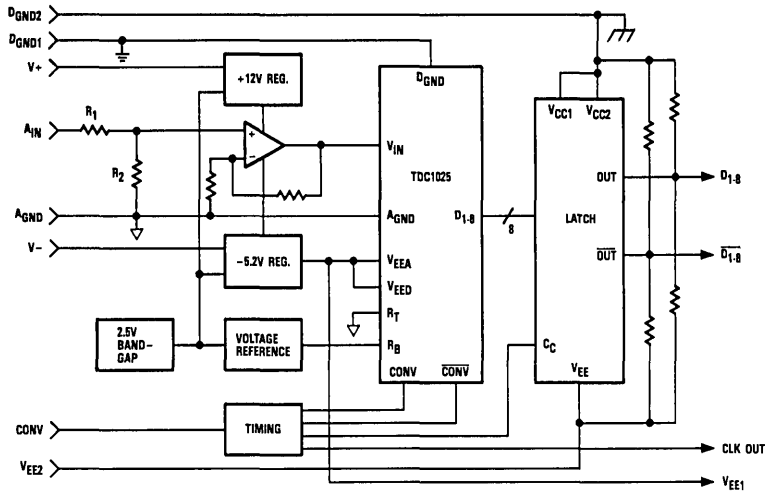
Functional Block Diagram



TDC1025E1C Eurocard Edgeconnector Pinout

A1	NC	B1	D_{GND2}
A2	NC	B2	D_{GND2}
A3	NC	B3	D_{GND2}
A4	D_1 (MSB)	B4	$\overline{D_1}$ (MSB)
A5	D_2	B5	$\overline{D_2}$
A6	D_3	B6	$\overline{D_3}$
A7	D_4	B7	$\overline{D_4}$
A8	D_5	B8	$\overline{D_5}$
A9	D_6	B9	$\overline{D_6}$
A10	D_7	B10	$\overline{D_7}$
A11	D_8 (LSB)	B11	$\overline{D_8}$ (LSB)
A12	NC	B12	D_{GND2}
A13	NC	B13	D_{GND2}
A14	NC	B14	D_{GND2}
A15	NC	B15	D_{GND2}
A16	NC	B16	NC
A17	NC	B17	D_{GND2}
A18	V_{EE2}	B18	V_{EE2}
A19	NC	B19	D_{GND2}
A20	NC	B20	D_{GND2}
A21	CONV	B21	D_{GND2}
A22	CLK OUT	B22	NC
A23	NC	B23	D_{GND1}
A24	V_{EE1}	B24	D_{GND1}
A25	NC	B25	NC
A26	NC	B26	A_{GND}
A27	NC	B27	A_{GND}
A28	A_{IN}	B28	A_{GND}
A29	NC	B29	A_{GND}
A30	V+	B30	A_{GND}
A31	NC	B31	A_{GND}
A32	V-	B32	A_{GND}

Functional Description

General Information

The TDC1025 evaluation board consists of five functional sections: the input buffer amplifier, reference voltage generator, voltage regulators, A/D converter, and output data latches.

Analog and digital grounds are separated on the board for flexibility in system grounding.

Buffer Amplifier

The analog input amplifier provided on the evaluation board is a differential amplifier comprised of transistor array U2, Q5, and Q1. The input signal is routed to the non-inverting input of the buffer through R1 and R2. These two resistors may be selected to provide scaling of the input voltage and input impedance. Values of R1 and R2 for various input ranges and impedances are shown in the Input Resistor Selection Table. The amplifier has a non-inverting gain of 2 and a 3dB bandwidth of approximately 90MHz. The TDC1025E1C is supplied with a 1V p-p input voltage range and a 50 Ohm input impedance referenced to A_{GND} (R1 = 0, R2 = 49.9 Ohms).

An offset adjustment potentiometer (R28) is provided to level shift input signals. The offset adjustment is also useful in calibration of the A/D converter. This voltage is fed from U3A through R10 and decoupled by C3. Q1 provides current buffering to drive the analog input of the A/D converter and to insure frequency stability. Resistors R15, 39, 40, 42, 44, 46, 67, 68 and 69 provide isolation between the amplifier output and the analog input pins of the A/D converter. R11 closes the feedback loop around the buffer amplifier.

Resistor locations for a -20dB test port are provided on the board. This allows the user to observe the signal at the buffer output. This test port is created by inserting an SMA connector (Omni-Spectra 2062-0000-00 or equivalent) at J4, and R60 and R61 onto the board. The suggested values are 470 Ohms for R60 and 49.9 Ohms for R61.

Voltage Reference

On the TDC1025E1C, R_T of the A/D converter is connected to A_{GND}, and R_B is connected to the -2V reference voltage. This sets the full-scale conversion range of 0 to -2 Volts at the A/D converter's analog input. The evaluation board provides a footprint for installing a potentiometer (R30) for the adjustment of R_M. This adjustment allows optimization of integral linearity, although this is not required to meet the converter specifications. A preferred low-impedance midpoint driving circuit is shown in the TDC1025 data sheet.

The master voltage reference is provided by U4 (+2.5V band-gap voltage source). This voltage is applied to potentiometer R29 which functions as a GAIN scaling adjustment. The voltage on R29 is inverted by op-amp U3. The output of this op-amp is then followed by a transistor, Q4, in order to provide current drive. The GAIN potentiometer is adjusted to set the full-scale conversion range of the A/D converter.

The sense points, R_{BS} and R_{TS}, are not used on the evaluation board, but are recommended for higher performance system design to minimize the offset error voltage. Use of the sense points is discussed in the TDC1025 A/D converter data sheet.

Voltage Regulators

Two voltage regulators are provided on the evaluation board to supply power to the buffer amplifier and the A/D converter. U3D and Q3 supply +12 Volts and U3B and Q2 supply -5.2 Volts. Both regulators and the voltage reference circuit, U3C and Q4, are referred to the output of U4, a 2.5 Volt band-gap reference device.

A/D Converter

The TDC1025 integrated circuit is an 8-bit, fully parallel (flash) A/D converter, capable of digitizing an input signal at rates up to 50MSPS (MegaSamples Per Second). The TDC1025E1C evaluation board has the A/D converter in a leaded chip carrier package (L1) installed. A differential ECL CONVert (CONV) signal controls 255 sampling comparators, encoding logic, and a latched output register. On each rising edge of the CONV signal, the comparators are latched and their outputs encoded into binary data. On the next rising edge of the CONV signal, the encoded result is transferred to the differential ECL data outputs of the A/D converter. Note that there are minimum pulse width (t_{PWL}, t_{PWH}) requirements on the CONV signal. Refer to the Timing Diagram (Figure 1) for timing requirements.

The evaluation board includes differential output data latches (U6 thru U9) for driving the board outputs. Provision has been made for ECL terminating resistors near the board edge connector.

Mechanical Design

The TDC1025E1C board is designed to meet "Eurocard" format and is compatible with the standard DIN 41612B connector. A mating connector is included with each evaluation board.

Mounting holes and pads are provided in the board for installing a contact chip carrier socket (for TDC1025C1) when the evaluation board is used as a test fixture. The user must remove the A/D converter before installing the chip carrier socket. Application Note TP-34 "Design Tips For The TDC1025 High-Speed A/D Converter" discusses sockets appropriate for use with the evaluation board.

Thermal Considerations

The TDC1025L1 supplied with the board has thermal characteristics similar to other high-performance ECL devices. With ambient temperatures above 45°C, 500 L.F.P.M. moving air is required to cool both the A/D and the ECL interface devices. Uniform cooling also ensures that temperature induced logic-level shifts between devices are minimized, resulting in good noise immunity. The ambient temperature of the TDC1025L1 should not be allowed to exceed 70°C during operation. A heatsink should be added if dictated by the system environment.

Analog Input

The SMA connector (J2) is one of two analog inputs available on the evaluation board. The other analog input is located at the Eurocard edge connector, pin A28. Analog ground (A_{GND}) returns are located on pins A_{26-32} of the edge connector. The use of J2 will provide superior performance at higher frequencies. A jumper must be installed on the board in order to use the analog input connection at the edge connector. The trace to the edge connector is left open to prevent noise pickup when the SMA connector is in use.

Name	Function	Value	E1C
A_{IN}	Analog Input Signal	1V p-p	A28, J2

Convert

A single-ended CONV signal may be applied via an on-board SMA connector (J3), or Pin A21 of the edge connector. A differential ECL CONV signal is generated from the single-ended input CONV signal by U5. This differential CONV signal is applied to the A/D converter as well as the delay line (Z1). The delay line provides the user with programmable delay taps (2ns increments) for strobing the output registers as well as providing a delayed clock output for external devices.

Name	Function	Value	E1C
CONV	Single-Ended CONV Signal Input	ECL	A21
CLK OUT	Delayed Clock Output	ECL	A22

Power

The TDC1025E1C evaluation board operates from three external power sources: −5.2VDC (V_{EE2}), +15VDC (V+), and −15VDC (V−). Other voltages are generated on the board by voltage regulator circuits: −5.2VDC (V_{EE1}), and +12VDC. The A/D converter chip and amplifier are powered from V_{EE1}, while the ECL output latches and terminators are powered from V_{EE2}. V_{EE1} and V_{EE2} are separated in order to keep the A/D converter supply as noise-free as possible. The return path for I_{EE1} (current from V_{EE1}) is A_{GND} and D_{GND1}. The return path for I_{EE2} (current from V_{EE2}) is D_{GND2}. The return path for I+ and I− (current from V+ and V−) is A_{GND}. All power and ground pins must be used. Diodes connected between grounds (D_6 through D_{11}) are provided for protection in case of excessive differential ground potentials or reversed supply polarity.

Ground isolation on the board is provided for flexibility in system grounding. Optimizing the A/D performance can be accomplished by connecting all grounds at the power source or directly at the chip. Since no two systems are alike, experiments with various ground connections should be made to achieve the best A/D performance. Analog ground noise should be minimized (i.e. from digital switching, clocks, etc.) whenever possible.

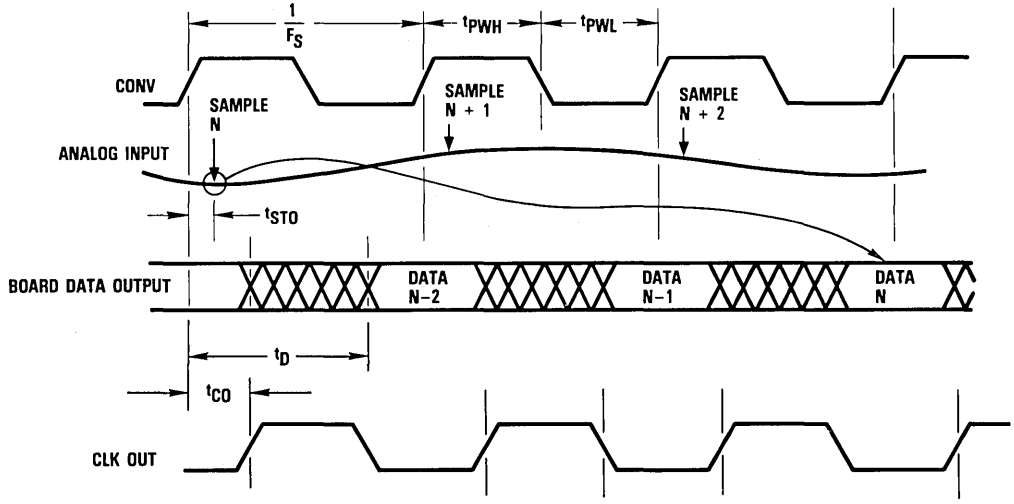
Name	Function	Value	E1C
V+	Positive Analog Power Supply	+15V	A30
V−	Negative Analog Power Supply	−15V	A32
V_{EE1}	Negative Supply Output	−5.2V	A24
V_{EE2}	Negative Supply For Data Latch	−5.2V	A18, B18
A_{GND}	Analog Ground	0.0V	B26-B32
D_{GND1}	TDC1025 Digital Ground	0.0V	B23, B24
D_{GND2}	Digital Ground For Data Latch	0.0V	B1-3, B12-15, B17, B19-21

Digital Outputs

The Q and $\overline{Q}$ outputs of the data latches (U6 thru U9) are routed to the edge connector. Provisions have been made on the board for installing terminator resistor SIPS on each data line. Standard ECL practices require source or load terminating resistors in order to minimize ringing and overshoot. If the data lines are routed to another circuit board or system, termination at the signal destination is recommended. If the data lines are only observed at the edge connector, then termination on the evaluation board is recommended.

Name	Function	Value	E1C
D_1 (MSB)	Most Significant Data Output	ECL	A4
$\overline{D_1}$ (MSB)	Most Significant Data Output Complement	ECL	B4
D_2		ECL	A5
$\overline{D_2}$		ECL	B5
D_3		ECL	A6
$\overline{D_3}$		ECL	B6
D_4		ECL	A7
$\overline{D_4}$		ECL	B7
D_5		ECL	A8
$\overline{D_5}$		ECL	B8
D_6		ECL	A9
$\overline{D_6}$		ECL	B9
D_7		ECL	A10
$\overline{D_7}$		ECL	B10
D_8 (LSB)	Least Significant Data Output	ECL	A11
$\overline{D_8}$ (LSB)	Least Significant Data Output Complement	ECL	B11

Figure 1. Timing Diagram



Absolute maximum ratings (beyond which the board may be damaged)[1]

Power Supply Voltages

V_{EE2} (measured to D_{GND2})	+0.5 to −7.0V
V+ (measured to A_{GND})	−0.5 to +18.0V
V− (measured to A_{GND})	+0.5 to −18.0V
D_{GND1} (measured to A_{GND})	+0.5 to −0.5V
D_{GND2} (measured to A_{GND})	+0.5 to −0.5V

Input Voltages

CONV (measured to D_{GND2})	+0.5 to −5.5V
A_{IN} (measured to A_{GND})	+2.5 to −2.5V[2]

Output

Short circuit duration (single output to D_{GND2})	indefinite

Temperature

Operating ambient	0 to +70°C[3]
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. With input impedance of 50 Ohms, as supplied.
3. With 500 L.F.P.M. moving air.

Operating conditions

Parameter		Min	Nom	Max	Units
V_{EE1}	Negative Power Supply (measured to D_{GND1})[3]	-4.9	-5.2	-5.5	V
V_{EE2}	Negative Power Supply (measured to D_{GND2})	-4.9	-5.2	-5.5	V
V+	Positive Power Supply (measured to A_{GND})	+14.25	+15.0	+15.75	V
V-	Negative Power Supply (measured to A_{GND})	-14.25	-15.0	-15.75	V
V_{AGND}	Analog Ground (measured to D_{GND1})	-0.1	0.0	+0.1	V
V_{DGND1}	Digital Ground (measured to D_{GND2})	-0.1	0.0	+0.1	V
t_{PWL}	CONV Pulse Width, LOW	8			ns
t_{PWH}	CONV Pulse Width, HIGH	10			ns
V_{IL}	Input Voltage, Logic LOW[1]			-1.63	V
V_{IH}	Input Voltage, Logic HIGH[1]	-0.98			V
A_{IN}	Input Voltage Range[4]	0.0		-1.0	V
T_A	Ambient Temperature Range[2]	0		70	°C

Notes:

1. Applies to U5 only.
2. 500 L.F.P.M. required above 45°C.
3. V_{EE1} is generated on the TDC1025E1C.
4. 50 Ohm input impedance, as supplied, buffer amplifier offset zeroed.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Min	Max	Units
I_{EE2}	Negative Supply Current	V_{EE2} = MAX		-500	mA
I+	Positive Supply Current	V+ = MAX, V- = MAX		150	mA
I-	Negative Supply Current	V+ = MAX, V- = MAX		-900	mA
V_{OL}	Output Voltage, Logic LOW	V_{EE1} = NOM[1]		-1.85	V
V_{OH}	Output Voltage, Logic HIGH	V_{EE1} = NOM[1]	-0.81		V

Note:

1. Applies to data latches (U_5 through U_9) only.

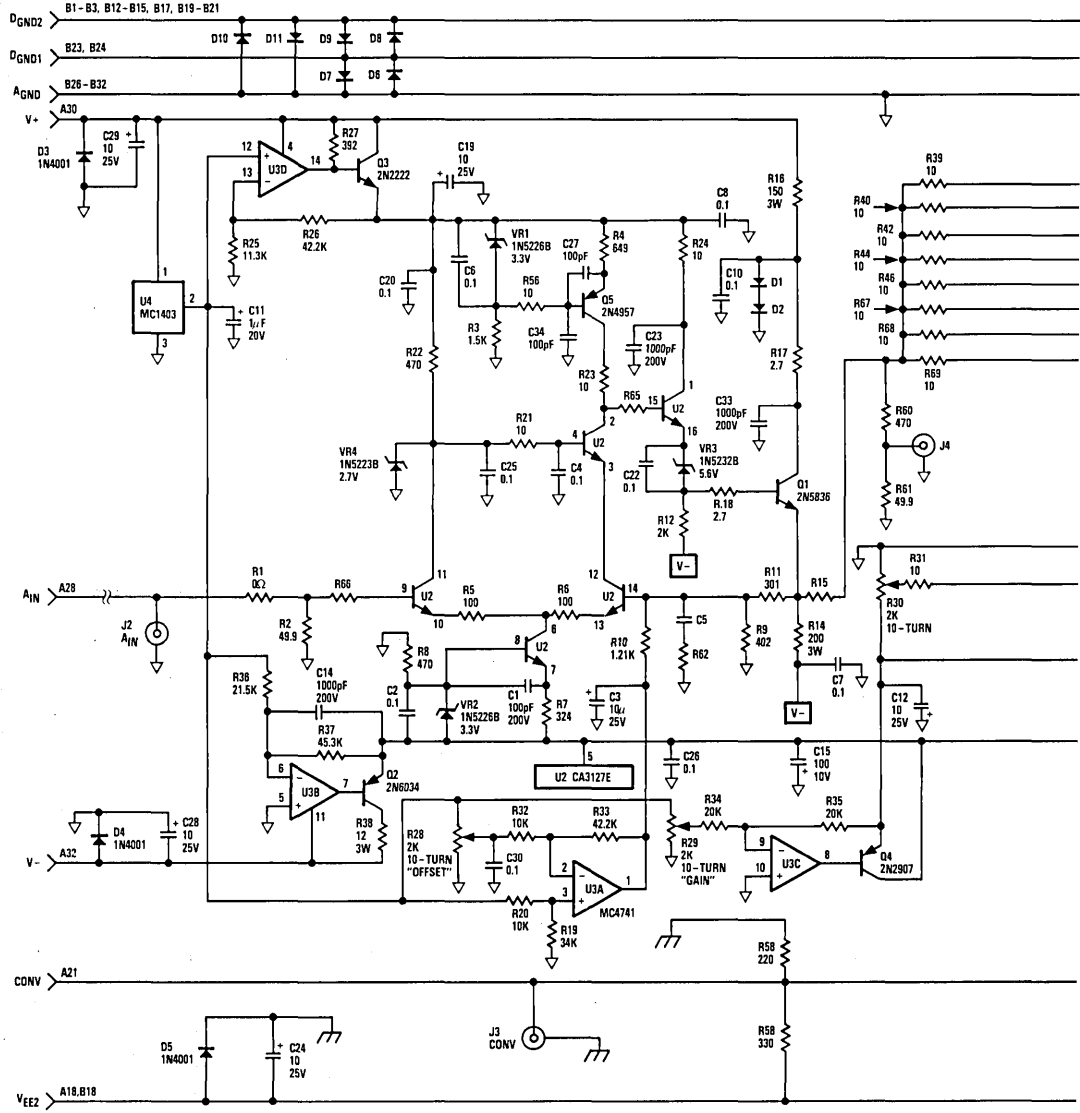
Switching characteristics within specified operating conditions

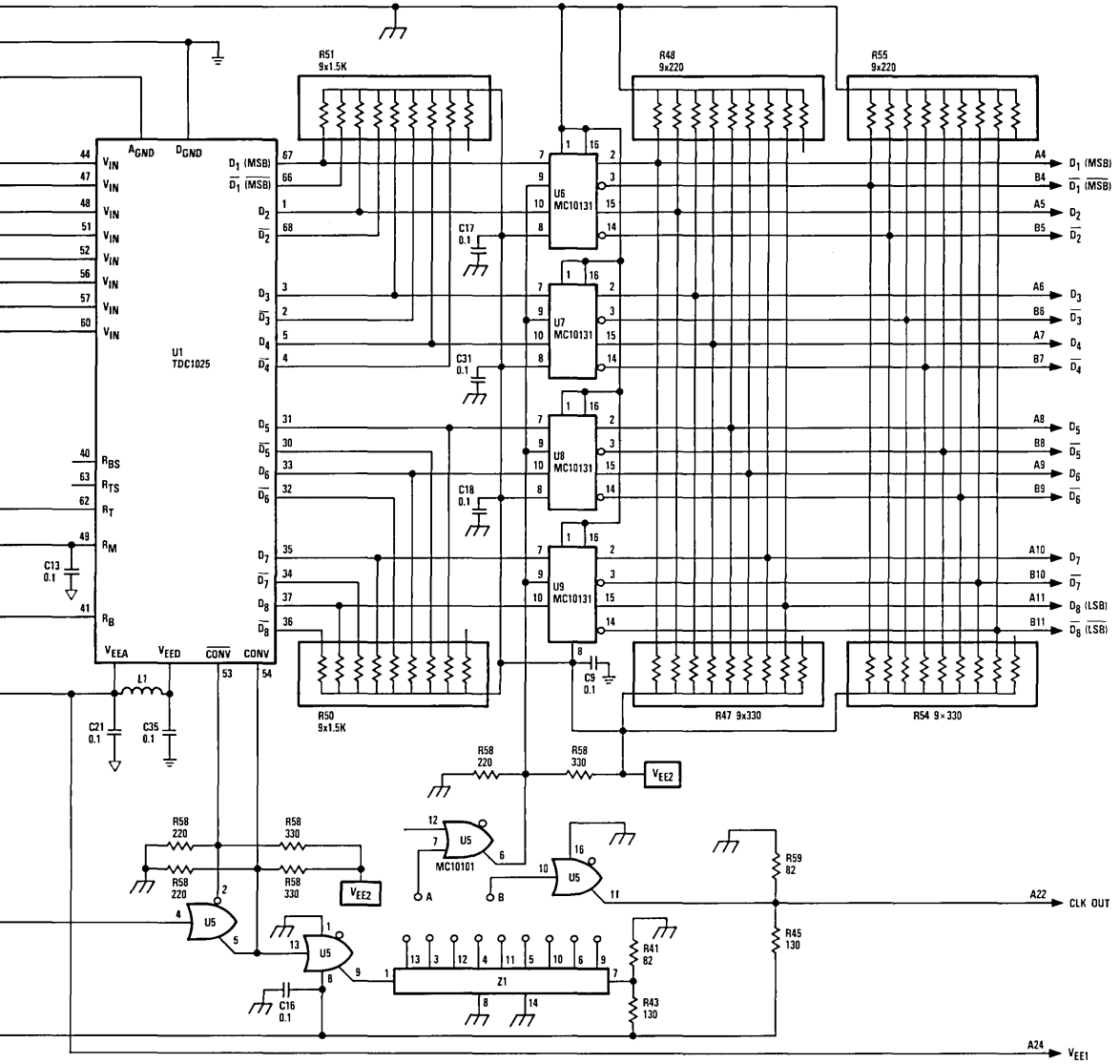
Parameter		Test Conditions	Min	Max	Units
F_S	Maximum Conversion Rate		50		MSPS
t_D	Data Output Delay	V_{EE2} = MIN	note 2	note 2	ns
t_{STO}	Sampling Time Offset[1]			10	ns
t_{CO}	CLK OUT Delay		note 3	note 3	ns

Notes:

1. Applies to TDC1025 integrated circuit only (excludes buffer amplifier).
2. Delay time determined in manufacturing process.
3. User selectable with delay line, Z1.

Schematic of Evaluation Board




R51 9x1.5K
R48 9x220
R55 9x220
U1 TDC1025
U5 MC10131
U6 MC10131
U7 MC10131
U8 MC10131
U9 MC10131
MC10101
C17 0.1
C31 0.1
C18 0.1
C9 0.1
C13 0.1
C21 0.1
C35 0.1
C16 0.1
L1
R50 9x1.5K
R47 9x330
R54 9x330
R58 220
R58 330
R59 82
R45 130
R41 82
R43 130
Z1
A4 D1 (MSB)
B4 D1 (MSB)
A5 D2
B5 D2
A6 D3
B6 D3
A7 D4
B7 D4
A8 D5
B8 D5
A9 D6
B9 D6
A10 D7
B10 D7
A11 D8 (LSB)
B11 D8 (LSB)
A22 CLK OUT
A24 VEE1
VEE2

Device performance characteristics within operating conditions

Parameter	Test Conditions	Min	Max	Units
E_{LI} Linearity Error, Integral, Independent	V_{RT}, V_{RB} = NOM[1,2]		0.3	%
E_{LD} Linearity Error, Differential	V_{RT}, V_{RB} = NOM[1,2]		0.3	%
Bandwidth, Full Power Input[1]		12.5		MHz

Notes:

1. Applies to TDC1025 integrated circuit only. Contributions from buffer amplifier are negligible.
2. RM is not adjusted.

Calibraton

The evaluation board is calibrated by adjusting the "OFFSET" and "GAIN" trim resistors, R28 and R29. Offset is calibrated when a voltage corresponding to 1/2 LSB greater than "zero-scale" is applied to the board input. The "OFFSET" potentiometer is then adjusted until the output data toggles between "00000000" and"00000001." Gain is calibrated by applying a voltage 1/2 LSB less than full-scale and adjusting the "GAIN" potentiometer until the output data toggles between "11111110" and "11111111." A linearity adjustment potentiometer (R30) can be installed by the user on the board to provide a fine adjustment of the integral linearity of the A/D converter.

Input Resistor Selection Table (Values in Ohms)

Z_{IN} Input Impedance	Input Voltage Range									
	1V		2V		4V		5V		10V	
	R1	R2	R1	R2	R1	R2	R1	R2	R1	R2
50Ω	0.00	49.9	24.9	24.9	37.4 ¼W	12.4	40.2 ½W	10.0	45.3 3W	4.99 ½W
75Ω	0.00	75.0	37.4	37.4	56.2 ¼W	18.7	60.4 ½W	15.0	68.1 2W	7.50 ¼W
93Ω	0.00	93.1	46.4	46.4	69.8 ¼W	23.2	75.0 ¼W	18.7	84.5 2W	9.31
1000Ω	0.00	1.0K	499	499	750	249	806	200	909	100

Notes:

1. 50Ω, 1V option supplied.
2. Resistors are 1%, 1/8 Watt unless otherwise specified.

For input voltage ranges or input impedances not shown in the table, the following formulas may be used to calculate R1 and R2:

$$Z_{IN} = R1 + R2 \qquad V_{RANGE} = \frac{R1 + R2}{R2}$$

Notes for Schematic of Evaluation Board

1. All resistor values are in Ohms.
2. All resistors are 1/8W unless otherwise noted.
3. All capacitor values are in microFarads unless otherwise noted.
4. All capacitors are 50WVDC unless otherwise noted.
5. All diodes are 1N4148 unless otherwise noted.
6. R58 is a quad 220/330 Ohm terminator SIP.
7. Z1 is a digital delay line, 2ns per tap, 20ns total Rhombus TZB12-5.
8. L1 is a ferrite bead inductor, Fair-rite part number 2743001112.
9. A_{GND} pins on the TDC1025L1 are: 46, 50, 55, 58.
10. D_{GND} pins on the TDC1025L1 are: 8, 28, 39, 64.
11. V_{EEA} pins on the TDC1025L1 are: 13, 14, 16, 18, 20, 22, 23.
12. V_{EED} pins on the TDC1025L1 are: 7, 29.
13. Values for components C5, R15, R62, R65, R66 are determined during the manufacturing process.
14. Component designators C32, R49, R57, R63, R64, J1 are not used on the TDC1025E1C board.
15. Components R30, R31, R45, R47, R48, R54, R55, R59, R60, R61, J4, are user options and are not included with the board.

Miscellaneous Evaluation Board Parts

J2 - J4 SMA PCB Jack (3) (J4 not included)	Winchester Plug 64P-6033-0430
Omni-Spectra P/N 2062-0000-00	Winchester Socket 64S-6033-0422-1

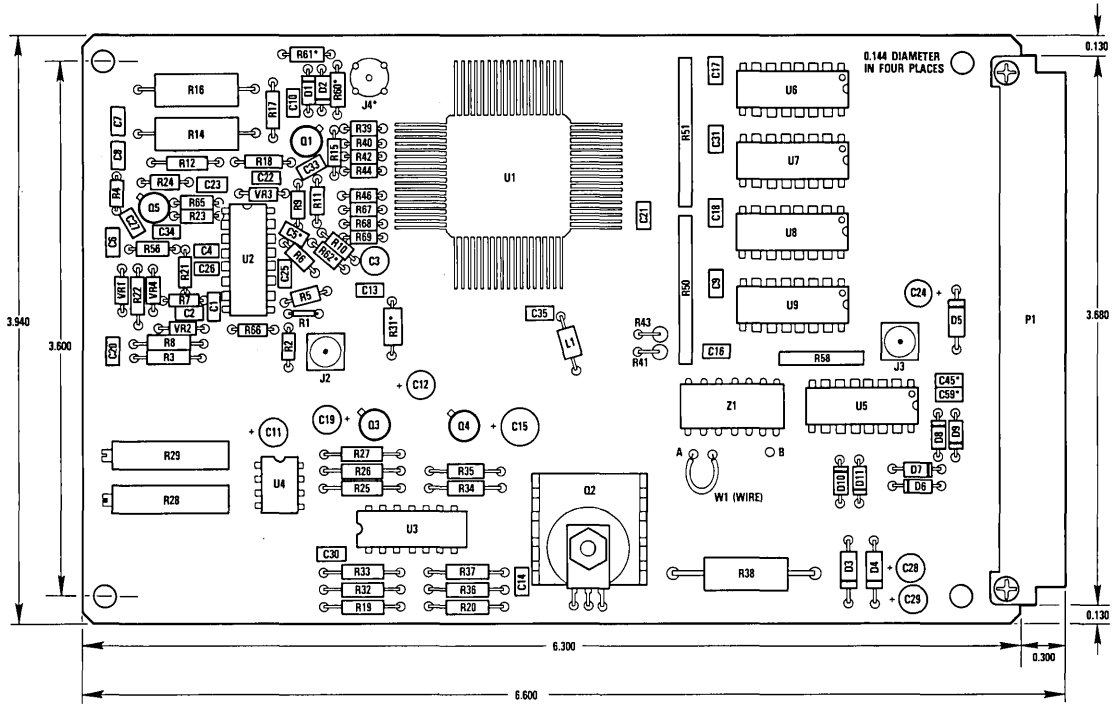
E

Output Coding Table

Input voltage range is from 0.00 to -1.00 Volt. (Input voltages are at code centers and the voltage offset of the buffer amplifier is nulled.)

Input Voltage	Binary Output
0.000V	00000000
-0.0039V	00000001
•	•
•	•
•	•
-0.4980V	01111110
-0.5020V	01111111
-0.5059V	10000000
•	•
•	•
•	•
-0.9961V	11111110
-1.0000V	11111111

TDC1025E1C Assembly



Notes:

1. Dimensions are in inches.
2. * not supplied.

Ordering Information

Product No.	Description	Order No.
TDC1025E1C	Eurocard Format Board With A/D Converter	TDC1025E1C

TDC1029E1C
Preliminary Information

High–Speed A/D Converter Evaluation Board
6–bit, 100MSPS

The TRW TDC1029E1C is a fully assembled and tested circuit board designed to aid in evaluating the high–speed TDC1029 flash A/D converter. The board comes complete with the A/D converter installed in a socket, ready to accept and digitize a 1V p–p 50 Ohm signal. Other ranges and impedances may be selected by plug–in resistor substitutions on the board. An offset adjustment is provided which can establish a unipolar or bipolar input range.

The board enables the converter to operate to its full specifications over the 0°C to 70°C ambient temperature range [1], is compatible with the 100mm x 160mm Eurocard format, and offers a number of user options for application flexibility.

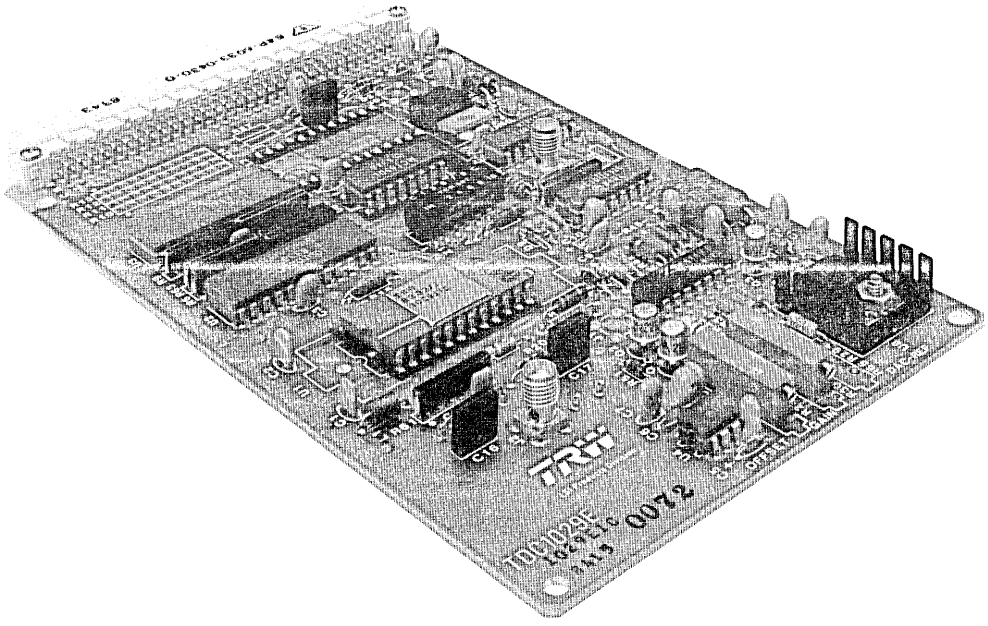
Features

- 100 MegaSamples Per Second (MSPS)
- 50MHz Input Bandwidth
- Includes TDC1029J7C A/D LSI Converter
- Selectable Input Impedance
- 1V Input Range
- Adjustable Offset For Unipolar Or Bipolar Inputs
- Configured For On–Board DAC Reconstruction
- Balanced ECL Output Buffering
- Comparator Circuit For Clock Generation
- Low Profile Eurocard Format DIN 41612B

Applications

- TDC1029 Evaluation
- System Prototyping
- Test Fixture

Note: 1. 500 L.F.P.M. moving air required above 40°C.



E

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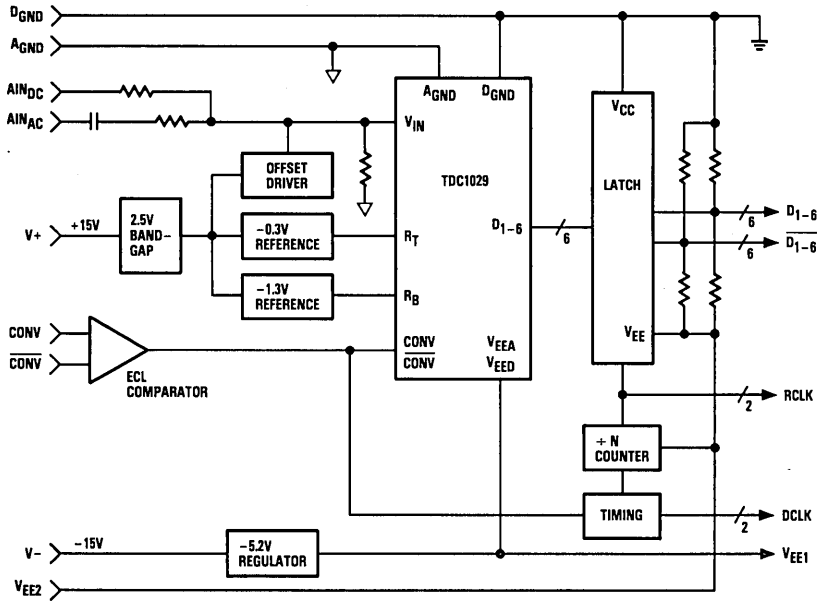
Functional Block Diagram



Pin Assignments

NC	A1	B1	D_{GND}
NC	A2	B2	D_{GND}
NC	A3	B3	NC
D_1 (MSB)	A4	B4	$\overline{D_1}$ (MSB)
D_2	A5	B5	$\overline{D_2}$
D_3	A6	B6	$\overline{D_3}$
D_4	A7	B7	$\overline{D_4}$
D_5	A8	B8	$\overline{D_5}$
D_6 (LSB)	A9	B9	$\overline{D_6}$ (LSB)
D_7 IN	A10	B10	$\overline{D_7}$ IN
D_8 IN	A11	B11	$\overline{D_8}$ IN
RCLK	A12	B12	$\overline{RCLK}$
D/A OUT-	A13	B13	NC
D/A OUT+	A14	B14	D_{GND}
NC	A15	B15	D_{GND}
NC	A16	B16	D_{GND}
NC	A17	B17	D_{GND}
V_{EE2}	A18	B18	V_{EE2}
NC	A19	B19	D_{GND}
NC	A20	B20	D_{GND}
CONV	A21	B21	$\overline{CONV}$
DCLK	A22	B22	D_{GND}
$\overline{DCLK}$	A23	B23	D_{GND}
V_{EE1}	A24	B24	D_{GND}
V_{EE1}	A25	B25	NC
NC	A26	B26	A_{GND}
NC	A27	B27	A_{GND}
AIN_{AC}	A28	B28	A_{GND}
NC	A29	B29	A_{GND}
V+	A30	B30	A_{GND}
V-	A31	B31	A_{GND}
V-	A32	B32	A_{GND}

Functional Description

General Information

The TDC1029E1C has been designed to simplify the interface and evaluation of TRW's 6-bit parallel A/D converter. The board provides all conditions necessary for the operation of the A/D converter, including impedance matching, timing and logic interface, power supply regulation, and generation of references.

The A/D converter is mounted into the board with low-inductance pin sockets. These sockets will withstand up to ten removal cycles.

The board is frequently used in prototyping a system, and is later converted to an incoming inspection test fixture. A variety of zero insertion force (ZIF) sockets are accommodated by the board to support this application. If clearance for a ZIF socket is not sufficient, bypass capacitors C1 and C2 can be removed and reverse-mounted on the foil side of the board.

Power and Grounding

The TDC1029E1C operates from three supply voltages, +15.0V, -15.0V and -5.2V, which must be supplied through the edge connector. For optimum performance, power supply noise should be less than 10mV p-p at specified current. All power and ground pins must be connected.

The V_{EE1} supply is derived from the -15.0V supply by regulator U8, and furnishes power for the A/D. This supply is connected to pins A24 and A25 of the edge connector for monitoring, and may supply up to 200mA for peripheral circuitry. However, the current available from V_{EE1} is not sufficient to supply V_{EE2} and should not be used for that purpose.

From a system standpoint, it is usually better to maintain separate analog and digital grounds to avoid ground loops. In this case the analog and digital grounds are connected at one common point; usually at the power supplies. For optimum performance of the TDC1029E1C where inducing ground loops elsewhere is not a concern, analog ground and digital ground can be connected together at the edge connector of the evaluation board.

Name	Function	Value	Connector
V+	Positive Supply Voltage	+15.0V	A30
V-	Negative Supply Voltage	-15.0V	A31, A32
V_{EE2}	Digital ECL Supply	- 5.2V	A18, B18
A_{GND}	Analog Ground	0.0V	B26-B32
D_{GND}	Digital Ground	0.0V	B1, B2, B14-B17, B19, B20, B22-B24

Voltage References

The full-scale range of conversion in a flash A/D converter is given by the voltage across the reference resistor chain. Highest performance from the TDC1029 A/D converter is achieved when the analog signal lies between -0.3V and -1.3V. Therefore, the two reference potentials V_{RT} and V_{RB} must be offset 0.3V below analog ground. V_{RT} is fixed at -0.3V (nominal), while V_{RB} may be adjusted between -0.5V and -1.5V.

Voltage reference U4 provides a master reference of 2.5V, from which both V_{RB} and V_{RT} are derived. The 2.5V is inverted and scaled by U5, which drives current-follower Q2. Capacitors C9 and C10 bypass V_{RT} to give a stable reference of -0.3V.

Gain-control dividers R30 and R49 provide between 0.8V and 2.5V from the 2.5V reference, which is amplified by U5. Current gain is given by Q1, which is capable of sinking 40mA, and providing from -0.5V to -1.5V to V_{RB}. Capacitors C6 and C7 bypass any spurious noise to analog ground.

Convert

The TDC1029E1C is configured to accommodate a 400mV p-p (nominal) input from a generator with a 50 Ohm source impedance. There are two methods of inputting the clock (CONV) to the board. The SMA connector labeled J3 is used for single-ended inputs only. This is also connected to pin A21 of the Eurocard edge connector. Pin A21 can be used to input a single-ended CONV, or used in conjunction with B21 ($\overline{CONV}$) for balanced inputs. Clocking the board from the edge connector will limit high-frequency performance; however, this feature is useful for low-frequency testing. The input termination for CONV consists of R56 and R62. These resistors may be changed as required to match the impedance of the board to that of the driving source.

A single-ended ECL clock is generated from CONV by U6. This clock is converted to differential ECL by U2. The sampling process is initiated by the rising edge of CONV, as shown in Figure 1. After a delay of t_{STO} (ns), the input comparators of the A/D are latched, thus sampling the analog input. There is a one clock cycle pipeline delay in the A/D converter. The digital data is valid on the A/D outputs t_{DO} (ns) after the next rising edge of CONV. The output data is registered by U3 on the rising edge of the Register CLocK (RCLK). After an output delay of t_{RDO} (ns), the data sample is available at the edge connector. Register U3 provides differential ECL digital outputs from the board. All digital outputs must be terminated by the user. Pads for SIP resistor networks are provided. For 130 Ohm source termination, R10 = R12 = 220 Ohms, and R11 = R13 = 330 Ohms. Alternatively, the digital outputs may be driven into any Thevenin equivalent of -2 Volts and 50 Ohms minimum terminating impedance.

Delay line Z1 provides delays from 1 to 10ns in 1ns increments. One of these taps has been chosen to optimize the timing of register U3. At the user's option, jumper W6 can be adjusted to provide timing for other peripheral circuitry, including an on-board DAC (U7) if one is used. This Delayed CLocK (DCLK) is available on pin A22 of the edge connector. A complementary clock output ($\overline{DCLK}$) is provided on pin A23 for driving differential ECL lines.

Gate U9 is programmed to divide by one, two or four, depending on the configuration of W1 and W2, which allows U3 to register all, every other, or every fourth digital output from the A/D. As configured, the board will output a new word for each conversion cycle. For special testing (such as beat frequency), W1 and W2 can be configured as shown in Table 1 to decimate the output data by two or four. The decimated U3 register clock (RCLK) is available on pin A12 of the edge connector. A complementary output ($\overline{RCLK}$) is provided on pin B12 for driving differential ECL lines.

Name	Function	Value	Connector
CONV	CONVert Clock Input	Text	A21
$\overline{CONV}$	CONVert Input Complement	Text	B21
RCLK	Register Clock Input	ECL	A12
$\overline{RCLK}$	Register Clock Complement	ECL	B12
DCLK	Delayed Clock Output	ECL	A22
$\overline{DCLK}$	Delayed Clock Complement	ECL	A23

Analog Input

The SMA connector labeled J2 is one of two analog inputs to the board. By installing a jumper (W3), this point is also connected to pin A28 of the Eurocard edge connector. Ground return for the edge connector analog input is provided by pin B28. The edge connector should be used for analog inputs below 25MHz only. When J2 is used as the analog input, W3 should be left open to avoid reflections from the unterminated line presented by the edge connector input trace. Similarly, when using the edge connector to input analog signals, J2 should be left open. The input source to the board must be able to drive a 25pF capacitive load up to the highest frequency of interest.

The input signal is capacitively coupled to the input termination consisting of R21, R50, and R52. The board presents a 50 Ohm impedance to the analog input, with a full-scale range of 1.4V p-p. The values of R21 and R50 can be adjusted by the user for other input impedances.

Analog Input (Cont.)

The input termination (R21, R50, R52) results in a 3dB attenuation, giving a 1.0V p-p full-scale input at the A/D. The input range of the A/D is fixed by the reference endpoints V_{RB} and V_{RT}, which are factory adjusted to -1.3V and -0.3V, respectively. Thus, it is necessary to offset the analog input to lie within the range of V_{RB} and V_{RT}. The OFFSET adjustment performs this function by drawing an offset bias current through the input termination.

Potentiometer R28 is the OFFSET adjustment. The 2.5V (U4) reference is divided by R28, then inverted by U5. Emitter-follower Q3 gives current gain and a low-impedance output which sinks up to 35mA through the termination network. The resulting offset voltage is 0.0V to -2.4V, depending on the setting of R28.

The response at the A/D input is attenuated less than 1dB at 60MHz when driven from J2. Low-frequency rolloff begins at approximately 1.5KHz, with an attenuation of 20dB per decade rate below this point. C16 can be replaced with a jumper if low-frequency signals are to be digitized, in which case the input signal can be externally offset.

Connector J1 and jumper W5 may be installed in the pads provided to monitor the analog input. A capacitor may be used in place of W5 to provide AC coupling. The insertion loss from J2 to J1 is approximately 25dB for frequencies up to 60MHz when terminated with 50 Ohms.

R_1 and R_{14} help match the A/D analog input impedance to the coaxial source impedance, minimizing reflections and equalizing delay to each of the analog inputs.

Name	Function	Value	Connector
AIN_{AC}	AC-Coupled Analog Input	Text	J2, A28
AIN_{DC}	DC-Coupled Analog Input	Text	J1

Data Outputs

The digital outputs D_1-D_6 are available on pins A4-A9 of the edge connector. Complementary outputs are provided on pins B4-B9 for driving differential ECL lines. A two's complement output is attained by cross-wiring the MSB (D_1), as shown in Table 2.

Name	Function	Value	Connector
D_1 (MSB)	Most Significant Data Output	ECL	A4
$\overline{D_1}$ (MSB)	MSB Output Complement	ECL	B4
D_2		ECL	A5
$\overline{D_2}$		ECL	B5
D_3		ECL	A6
$\overline{D_3}$		ECL	B6
D_4		ECL	A7
$\overline{D_4}$		ECL	B7
D_5		ECL	A8
$\overline{D_5}$		ECL	B8
D_6 (LSB)	Least Significant Data Output	ECL	A9
$\overline{D_6}$ (LSB)	LSB Output Complement	ECL	B9

Digital-to-Analog Converter

Pads are provided to mount a high-speed 8-bit registered digital-to-analog (D/A) converter (U7) on the board for signal reconstruction. The pinout is configured for the TDC1018J7, an 8-bit, 125MSPS D/A, available from TRW. Other D/As may be used by installing jumpers between the circuit board traces and pads as required.

Name	Function	Value	Connector
D/A OUT+	D/A Converter Output	Text	A14
D/A OUT-	D/A Converter Output	Text	A13
D_7 IN	D/A Converter Data Input	ECL	A10
$\overline{D_7}$ IN	D/A Converter Data Input	ECL	B10
D_8 IN	D/A Converter Data Input	ECL	A11
$\overline{D_8}$ IN	D/A Converter Data Input	ECL	B11

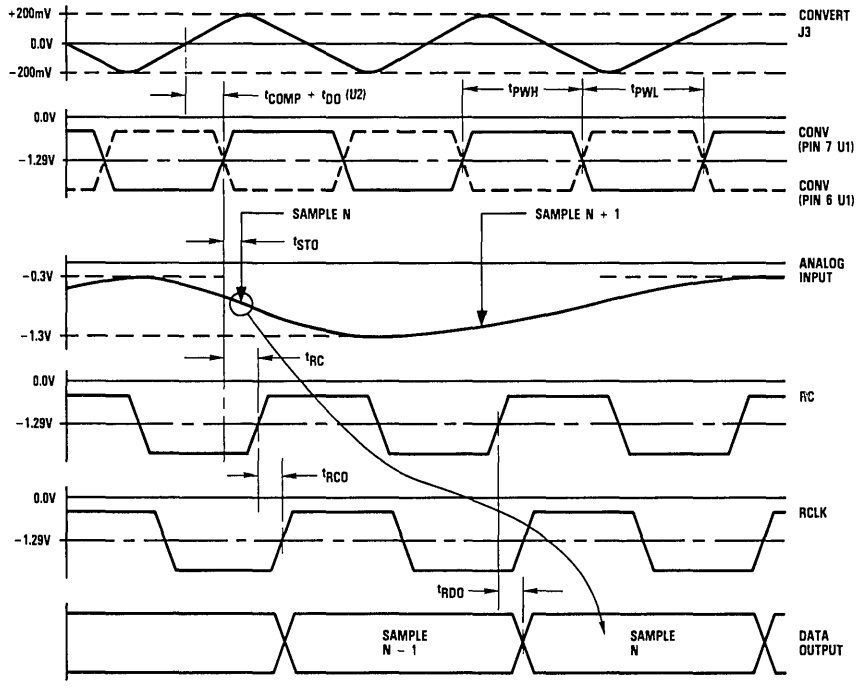
Thermal and Mechanical Considerations

The TDC1029J7C supplied with the board has thermal characteristics similar to other high-performance ECL devices. With ambient temperatures up to 40°C, the TDC1029E1C assembly will operate in still air. For ambient temperatures above 40°C, 500 L.F.P.M. moving air is required to cool both the A/D and the ECL interface devices. Uniform cooling also ensures that temperature induced logic-level shifts between devices are minimized, giving the best noise margin.

The TDC1029E1C is assembled to meet the "Eurocard" format standards (DIN 41612B).

Installation of a ZIF socket requires careful penetration of the RTV pin socket sealer. The high profile of a zero insertion force socket may restrict board clearance and add parasitic inductance to the signal input leads, which may reduce the high-frequency performance of the system.

Figure 1. TDC1029E1C Timing Diagram



Parts List

Resistors

R1	15.0Ω	1/8W	1%
R6	220/330 x 4 SIP		2%
R9	220/330 x 4 SIP		2%
R14	15.0Ω	1/8W	1%
R15	51.1 KΩ	1/4W	1%
R16	220/330 x 4 SIP		2%
R19	220/330 x 4 SIP		2%
R20	470Ω	1/4W	1%
R21	68Ω	1/4W	5%
R24	220/330 x 4 SIP		2%
R28	2 KΩ POT		5%
R29	11.3 KΩ	1/4W	1%
R30	2 KΩ POT		5%
R31	270Ω	1/2W	5%
R35	10.0 KΩ	1/4W	1%
R36	4.22 KΩ	1/4W	1%
R37	20.0 KΩ	1/4W	1%
R38	20.0 KΩ	1/4W	1%
R39	10Ω	1/8W	5%
R40	10.0 KΩ	1/4W	1%
R41	1.21 KΩ	1/4W	1%
R43	1.5 KΩ	1/4W	5%
R44	10.0 KΩ	1/4W	1%
R46	82Ω	1/4W	5%
R49	1.00 KΩ	1/4W	1%
R50	18Ω	1/4W	5%
R51	10Ω	1/8W	5%
R52	68Ω	1/4W	5%
R53	324Ω	1/8W	1%
R54	100Ω	1/8W	1%
R55	220/330 x 4 SIP		2%
R56	49.9Ω	1/8W	1%
R57	130Ω	1/4W	5%
R60	49.9Ω	1/8W	1%
R61	220/330 x 4 SIP		2%
R62	49.9Ω	1/8W	1%
R63	220/330 x 4 SIP		2%
R64	220/330 x 4 SIP		2%
R66	12Ω	3W	5%
R67	12Ω	3W	5%

Transistors

Q1, Q3	2N2907
Q2	2N2222

Capacitors

C1–C4	0.1 μF	50V	
C5	1.0 μF	35V	Polarized
C6	10.0 μF	25V	Polarized
C7–C9	0.1 μF	50V	
C10	1.0 μF	35V	Polarized
C11	0.1 μF	50V	
C14	1.0 μF	50V	Non-polar
C15	10.0 μF	25V	Polarized
C16, C17	1.0 μF	50V	Non-polar
C18, C19	1.0 μF	35V	Polarized
C20–C22	0.1 μF	50V	
C23, C24	1.0 μF	35V	Polarized
C25, C26	10.0 μF	25V	Polarized
C27	0.1 μF	50V	
C28, C29	1.0 μF	35V	Polarized

Integrated Circuits

U1	TDC1029J7
U2	100102D
U3	100151D
U4	3503Y
U5	4741CL
U6	MC1650L
U8	337T
U9	10H131L
U10	10H102L
U11	7805C

Diodes

D1, D3, D4, D9	1N4148
D2, D7, D8	1N4001
D5, D6	1N5711

Inductors

L1	Bead Inductor

Delay Lines

Z1	TCR507

E

Table 1. Register Options

W1	W2	Function
0	0	÷4; Every Fourth Sample Registered
0	I	÷2; Every Other Sample Registered
I	I	All Data Registered, As Shipped

0 = Open

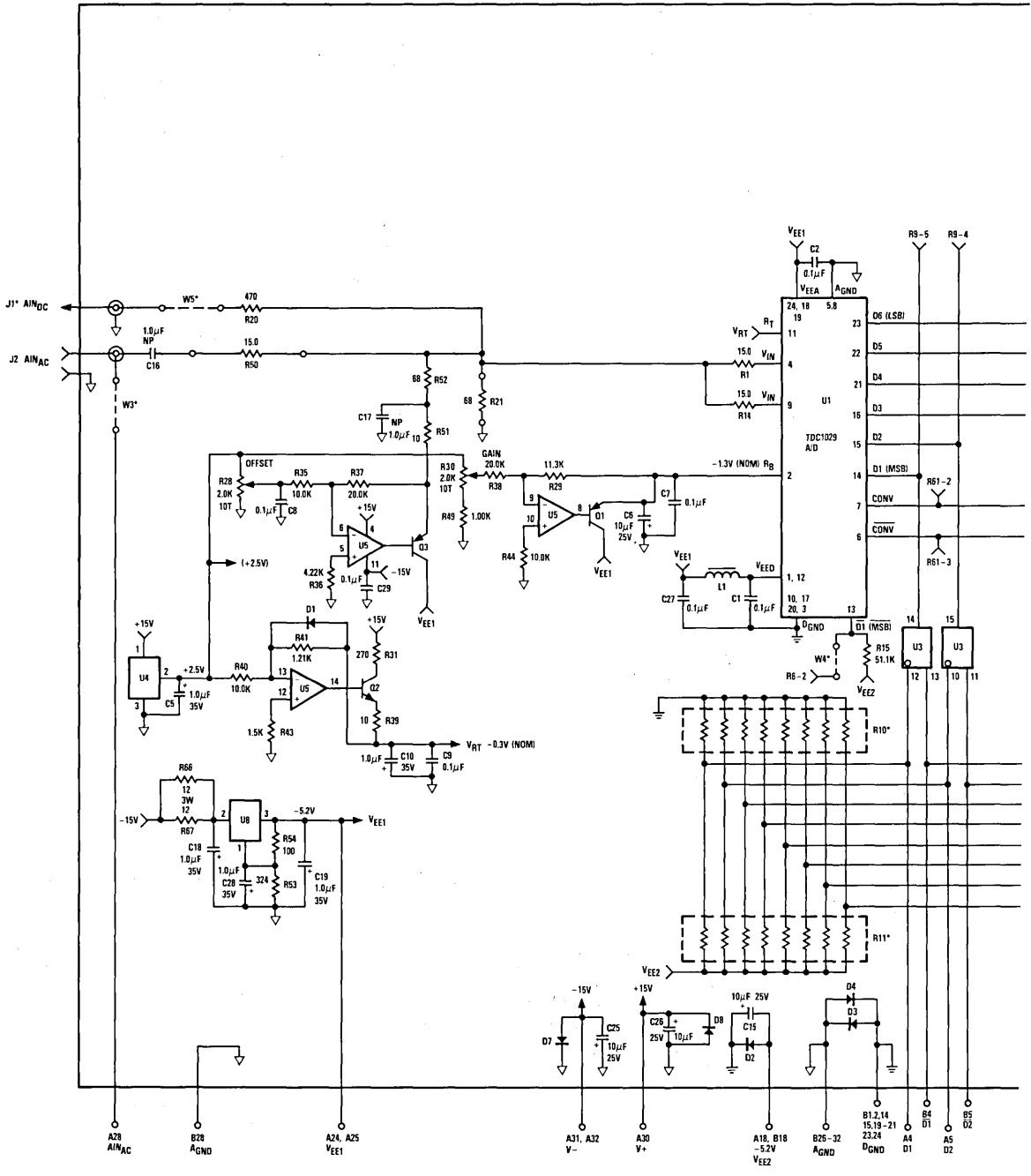
I = Installed

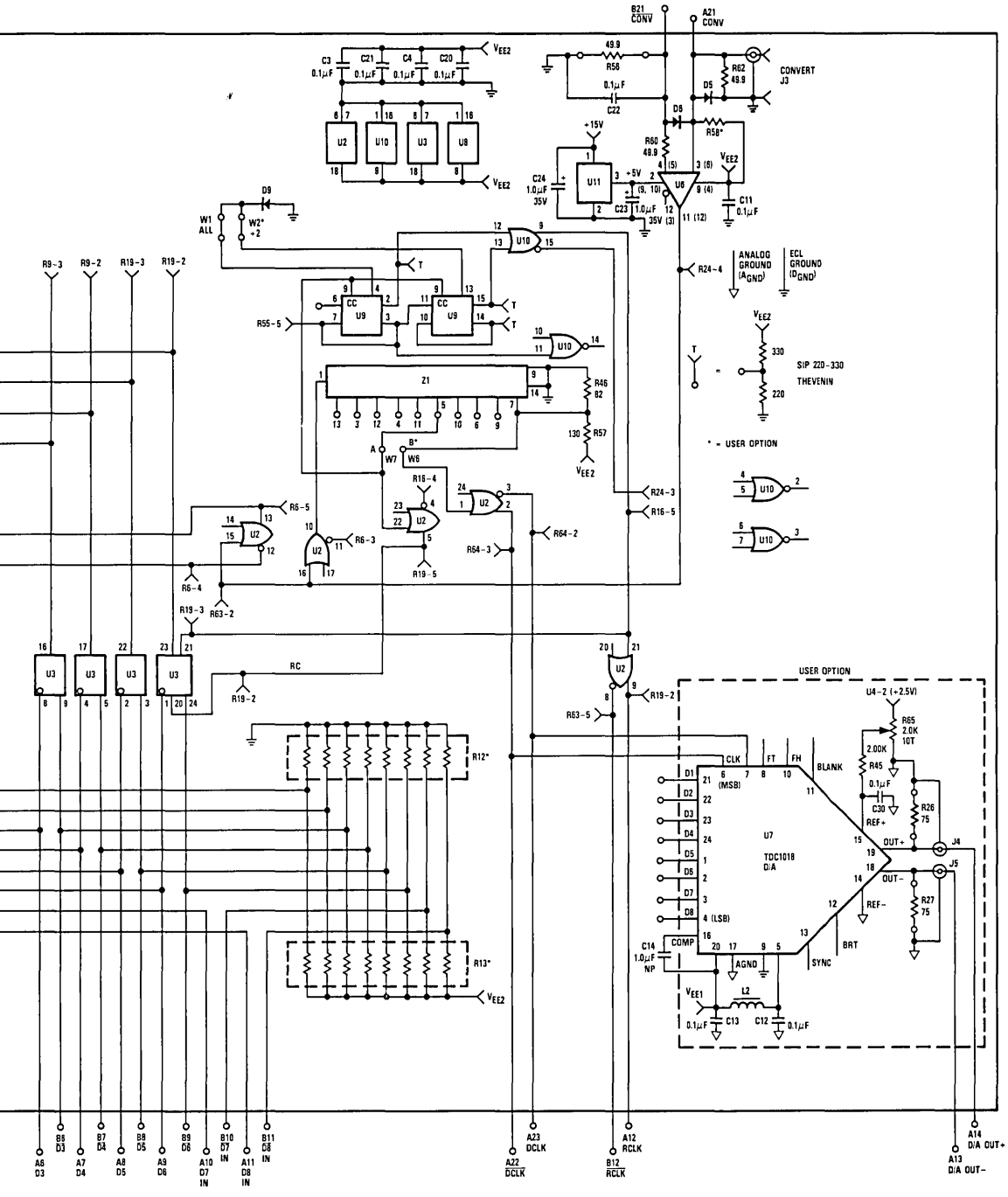
Table 2. Output Format

Analog Input[1]	Binary	Two's Complement
0.7V	111111	011111
•	•	•
•	•	•
•	•	•
-0.7V	000000	100000

Note: 1. AC Coupled

Figure 2. Schematic of Evaluation Board




B21 CONV
A21 CONV
CONVERT J3
ANALOG GROUND (AGND)
ECL GROUND (DGND)
SIP 220-330 THEVENIN
* = USER OPTION
USER OPTION
U7 TDC1018 D/A
U4-2 (+2.5V)
R65 2.0K 10T
R45 2.00K
R26 75
R27 75
J4
J5
W1 ALL
W2* ÷2
R9-3
R9-2
R19-3
R19-2
R55-5
R46 82
R57 130
R16-4
R16-5
R24-3
R24-4
R6-5
R6-3
R6-4
R63-2
R64-2
R64-3
R19-5
R63-5
RC
R12*
R13*
A6 D3
B6 D3
A7 D4
B7 D4
A8 D5
B8 D5
A9 D6
B9 D6
A10 D7 IN
B10 D7 IN
A11 D8 IN
B11 D8 IN
A22 DCLK
A23 DCLK
B12 RCLK
A12 RCLK
A13 D/A OUT-
A14 D/A OUT+

E

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_+ (Measured to A_{GND})	−0.5 to +18.0V
V_- (Measured to A_{GND})	+0.5 to −18.0V
V_{EE2} (Measured to D_{GND})	+0.5 to −7.0V
A_{GND} (Measured to D_{GND})	+0.5 to −0.5V

Input Voltages

Convert, $\overline{\text{Convert}}$ (50 Ohm input)	+1.0 to −2.0V
AIN_{DC} (50 Ohm 1V input configuration)	+1.5 to V_{EE}V

Temperature

Operating, ambient	−30 to 70 °C
Storage	−55 to +125 °C

Note:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.

Operating conditions

Parameter		Temperature Range			Units
		Min	Nom	Max	
V_+	Positive Supply Voltage (Measured to A_{GND})	+14.25	+15.0	+15.75	V
V_-	Negative Supply Voltage (Measured to A_{GND})	−14.25	−15.0	−15.75	V
V_{EE2}	ECL Supply Voltage (Measured to D_{GND})	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0.0	+0.1	V
V_{RT}	Reference Input, Top (R_T) [1,2]	−0.2	−0.3	−0.4	V
V_{RB}	Reference Input, Bottom (R_B) [1,2]	−1.2	−1.3	−1.4	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	0.9	1.0	1.1	V
t_{PWH}	CONVert Pulse Width, HIGH [2]	5	6		ns
t_{PWL}	CONVert Pulse Width, LOW [2]	3	4		ns
V_C	CONVERT Input Voltage Amplitude	200	400	2000	mV p-p
V_A	Analog Input Voltage Amplitude		1.4	2.1	V p-p
T_A	Temperature, Ambient [3]	0		70	°C

Notes:

1. V_{RT} must be more positive than V_{RB} and the reference voltage differential must be within specified range.
2. Specification applies to TDC1029J7.
3. 500 L.F.P.M. moving air required above 40°C.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Min	Temperature Range Max	Units
I_+	Supply Current [1]	V_+ = MAX		60	mA
I_-	Supply Current [1]	V_- = MAX		400	mA
I_{EE2}	Supply Current	V_{EE2} = MAX		1000	mA

Note:

1. V_{RT}, V_{RB} = Nominal, as shipped.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Min	Temperature Range Max	Units
F_S	Maximum Conversion Rate	V_+, V_-, V_{EE2} = MIN	100		MSPS
t_{COMP} + $t_{DO(U2)}$	Comparator + Gate Delay	V_+, V_-, V_{EE2} = MIN		8	ns
t_{STO}	Sampling Time Offset [1]	V_+, V_-, V_{EE2} = MIN		5	ns
t_{RC}	Register Clock Delay	V_+, V_-, V_{EE2} = MIN		8	ns
t_{RCO}	Register Clock Output Delay	V_+, V_-, V_{EE2} = MIN		5	ns
t_{RDO}	Register Output Delay	V_+, V_-, V_{EE2} = MIN		3	ns

Note:

1. Specification applies to TDC1029J7.

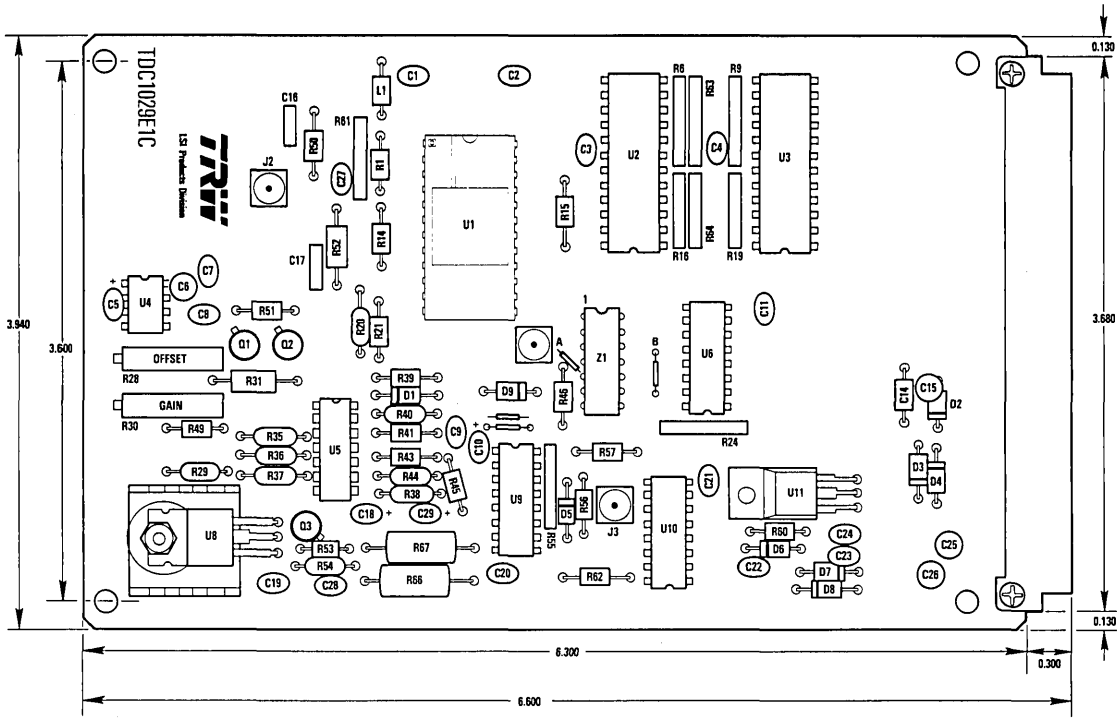
System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Min	Temperature Range Max	Units
BW	Bandwidth, Full Power Input [1]	F_S = 100MSPS	50		MHz
SNR	Signal-to-Noise Ratio [2]	100MSPS Conversion Rate			
	Peak Signal/RMS Noise	25MHz Input	41		dB
		50MHz Input	38		dB
	RMS Signal/RMS Noise	25MHz Input	32		dB
		50MHz Input	29		dB

Notes:

1. Beat frequency sinusoidal reconstruction producing no errors greater than 3 LSB's, t_{PWH} = 6ns.
2. Single frequency sinusoidal input attenuated 3dB at 1/2 sampling frequency (anti-alias prefilter).

Eurocard Assembly



Ordering Information

Product Number	Description	Order Number
TDC1029E1C	Eurocard Format Board With A/D Converter	TDC1029E1C

TDC1047E1C
Preliminary Information

A/D Converter Evaluation Board
7-bit, 20MSPS

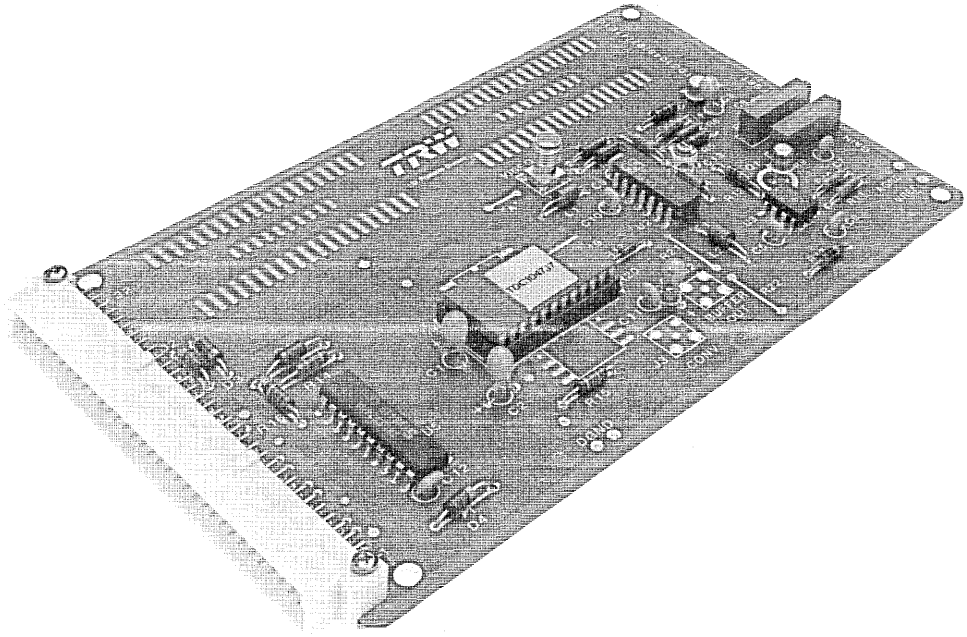
The TDC1047 evaluation board is a fully assembled and tested circuit board designed to aid in the evaluation of TRW's TDC1047 7-bit video analog-to-digital converter. The board contains circuitry for buffering the input signal, generating reference voltages, and latching output data. All digital inputs and outputs are TTL compatible. Provisions are made for gain and offset adjustments. The board requires +5 and -5.2 Volt power supplies, and is configured to interface with the Eurocard (DIN 41612B) connector format.

Features

- Includes TDC1047 7-Bit A/D Converter
- User-Selectable Input Impedance
- User-Selectable Input Voltage Range
- Unipolar Or Bipolar Operation
- Gain And Offset Calibration Controls
- Operates From +5.0 And -5.2 Volt Power Supplies
- Digital Output Buffers Included
- Eurocard Connector Format
- Uncommitted Prototyping Area

Applications

- Evaluation Of TDC1047 A/D Converter
- System Prototyping Aid
- Incoming Inspection Test Fixture



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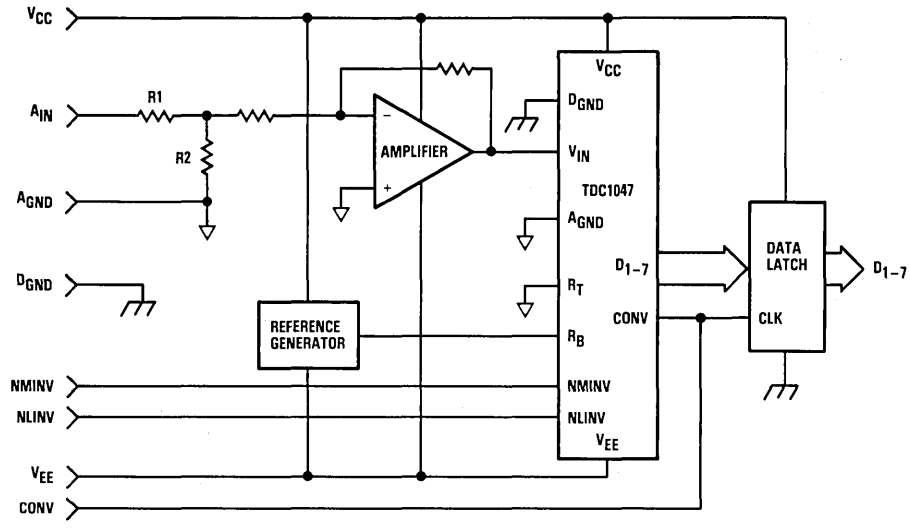
Functional Block Diagram



Pin Assignment

D_{GND}	A1	B1	V_{EE}
D_{GND}	A2	B2	D_{GND}
D_{GND}	A3	B3	D_7 (LSB)
D_{GND}	A4	B4	D_6
D_{GND}	A5	B5	D_5
D_{GND}	A6	B6	NLINV
D_{GND}	A7	B7	D_4
D_{GND}	A8	B8	D_3
D_{GND}	A9	B9	D_{GND}
D_{GND}	A10	B10	D_{GND}
D_{GND}	A11	B11	D_2
D_{GND}	A12	B12	D_1 (MSB)
D_{GND}	A13	B13	NMINV
D_{GND}	A14	B14	NC
D_{GND}	A15	B15	CONV
D_{GND}	A16	B16	D_{GND}
D_{GND}	A17	B17	D_{GND}
D_{GND}	A18	B18	V_{CC}
NC	A19	B19	NC
A_{GND}	A20	B20	NC
A_{GND}	A21	B21	A_{IN}
A_{GND}	A22	B22	A_{GND}
A_{GND}	A23	B23	NC
A_{GND}	A24	B24	NC
A_{GND}	A25	B25	A_{GND}
A_{GND}	A26	B26	NC
A_{GND}	A27	B27	NC
A_{GND}	A28	B28	NC
A_{GND}	A29	B29	NC
A_{GND}	A30	B30	NC
A_{GND}	A31	B31	NC
A_{GND}	A32	B32	NC

Functional Description

General Information

The TDC1047 evaluation board consists of four circuit blocks: the buffer amplifier, reference voltage generator, A/D converter, and output data latch. Analog and digital grounds are separated on the board to provide flexibility in system grounding.

Buffer Amplifier

The input buffer amplifier has been designed specifically for standard baseband video. This amplifier is optimized for 75 Ohm 1 Volt p-p levels. The input resistor network (R1 and R2), the amplifier gain factor of -2, and the amplifier's adjustable offset are arranged so that the A/D converter receives a full-scale input signal from 0 to -1 Volt.

The amplifier drives the A/D converter directly without an emitter follower stage. Frequency response and pulse response are adjusted by the variable capacitor, C13. The board has provision for a resistive voltage divider and SMA output connector for convenient monitoring of amplifier response.

Voltage Reference

The reference voltage for the TDC1047 is generated by operational amplifier U3 and PNP transistor, Q1, which supplies the reference current. System "GAIN" is adjusted by varying potentiometer R9 which controls the reference voltage to the A/D converter. The adjustable reference voltage range is 0 to -1.2 Volts.

A/D Converter

The TDC1047 integrated circuit is a 7-bit fully parallel (flash) analog-to-digital converter capable of digitizing an input signal at rates up to 20MSPS (MegaSamples Per Second). A single convert (CONV) signal controls the conversion operation of the device. The TDC1047 consists of 127 sampling comparators, encoding logic, and a latched output register. On the rising edge of the CONV signal, the comparators are latched and their outputs encoded. On the next rising edge of the CONV signal, that data is transferred to the outputs of the TDC1047.

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Output Interface

Data from the TDC1047 is latched by U5 on the rising edge of the CONV signal. This 74LS374 octal edge-triggered latch improves output drive and fan-out capability for the board while adding one clock cycle of pipeline delay. Substituting a 74LS373 for U5 and connecting its clock input to a logic "1" will eliminate the extra pipeline delay while improving the data output drive capability of the board.

Mechanical Design

The TDC1047E1C is designed to be compatible with the "Eurocard" format and mate with a standard 64 conductor DIN Eurocard connector. Mating edge connectors are included with each evaluation board.

The TDC1047E1C evaluation board may also be used with the TDC1048 8-bit A/D converter by removing the TDC1047 socket and installing a 28 lead DIP socket in the footprint oriented at right angles to that of the TDC1047. In addition, electrical changes must be made to the board in order to use the TDC1048. (Refer to TDC1048E1C Data Sheet.)

Standard 24 pin sockets for the TDC1047 integrated circuit are used on the boards. The boards are arranged so that this socket may be replaced by a "Zero Insertion Force" (ZIF) socket when the evaluation board is used as a test fixture.

Power Supplies

The TDC1047E1C evaluation board operates from two power supply voltages: +5.0 and −5.2 Volts. The return path for I_{CC} (current from the +5.0 Volt power supply) is D_{GND}. The return paths for I_{EE} (current from the −5.2 Volt supply) is A_{GND}. It is recommended that all ground pins be used. Diodes D1 through D4 function as voltage clamps which will prevent damage to the board if improper power supply voltages are applied.

Name	Function	Value	Pin
V_{CC}	Positive Power Supply	+5.0V	B18
V_{EE}	Negative Power Supply	−5.2V	B1
A_{GND}	Analog Ground	0.0V	A20−A32
			B22
			B25
			B28
D_{GND}	Digital Ground	0.0V	A1−A18
			B2
			B9
			B10
			B16
			B17

Analog Input

The TDC1047 evaluation board is supplied with a nominal input impedance of 75 Ohms and an input voltage range of 1 Volt p−p. Both input impedance and input voltage range may be changed for operation in other modes. The values of input resistors R1 and R2 determine the input impedance and voltage range of the evaluation board. Suggested values are shown in the Input Resistor Selection Table for various input impedances and voltage ranges. Note that the video input to the board is through an SMA connector (J1, Video In). Video input to the board can be routed through the edge connector by installing jumper "A" and using edge connector pin B21.

Name	Function	Value	Pin
A_{IN}	Analog Input Voltage	See text	B21

Control Inputs

Two control inputs are provided for changing the format of the output data. When NMINV is tied to a logic "0," the most significant bit of the output data is inverted. When NLINV is tied to a logic "0," the six least significant bits of the output data are inverted. By using these DC controls, the output data can be read in binary, inverse binary, two's complement, or inverse two's complement formats. Output data versus input voltage and control input state is illustrated in the Output Coding Table. Pull−up resistors are provided on the board for disabling these control functions when their pins are left open.

Name	Function	Value	Pin
NMINV	Not Most Significant Bit INVert	TTL	B13
NLINV	Not Least Significant Bit INVert	TTL	B6

Reference

The TDC1047 evaluation board includes circuitry for generating the voltage reference for the A/D converter. This voltage is brought out to a test point located on the side of the board opposite that of the edge connector.

Convert

The TDC1047 A/D converter is sampled within 8ns after the rising edge of the CONV signal. Output data is latched on the next rising edge of the CONV signal. Data from U5 is also latched on the rising edge of the CONV signal. U5 adds one clock cycle of pipeline delay to data sent off the board. Note that there are minimum pulse width (t_{PWH}, t_{PWL}) requirements on the waveshape of the CONV signal. A footprint for an SMA connector is located on the board near the A/D converter (J3, CONV) for a convenient monitoring or input point.

Name	Function	Value	Pin
CONV	A/D Clock Input	TTL	B15

Data Outputs

The outputs of the TDC1047 evaluation board are TTL compatible and capable of driving several TTL loads.

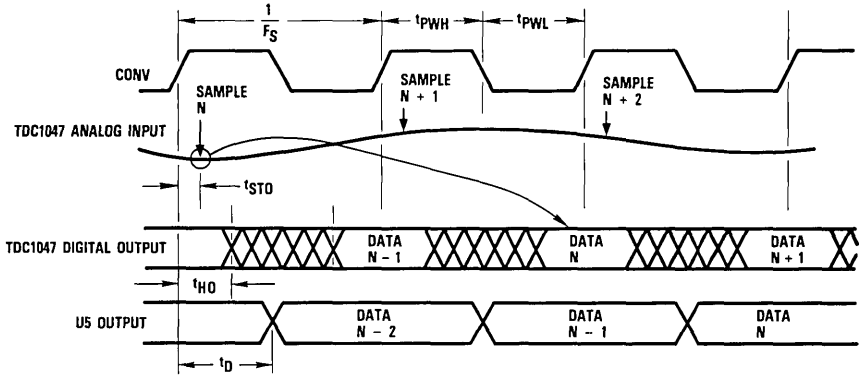
Name	Function	Value	Pin
D_1 (MSB)	Most Significant Data Bit	TTL	B12
D_2		TTL	B11
D_3		TTL	B8
D_4		TTL	B7
D_5		TTL	B5
D_6		TTL	B4
D_7 (LSB)	Least Significant Data Bit	TTL	B3

No Connects

There are several pins on the TDC1047 evaluation board that have no connection to the circuit. These pins may be left open. Note that pin B14 is connected to an output of U5 and must be left open.

Name	Function	Value	Pin
NC	No Connection	Open	A19
			B14
			B19
			B20
			B29–B32

Figure 1. Timing Diagram



Absolute maximum ratings (beyond which board may be damaged) [1]

Power Supply Voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	+0.5 to −0.5V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V

Output

Applied voltage	−0.5 to +5.5V [2]
Applied current externally forced	−1.0 to +6.0mA [3,4]
Short circuit duration (single output in HIGH state to D_{GND})	1 sec.

Temperature

Operating, ambient	−40 to +90°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the board.

Operating conditions

Parameter		Min	Nom	Max	Units
V_{CC}	Positive Power Supply (measured to D_{GND})	4.75	5.0	5.25	V
V_{EE}	Negative Power Supply (measured to A_{GND})	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground (measured to D_{GND})	−0.1	0.0	+0.1	V
t_{PWH}	CONV Pulse Width, HIGH [1]	14			ns
t_{PWL}	CONV Pulse Width, LOW [1]	14			ns
V_{IL}	Input Voltage, Logic LOW [1]			0.8	V
V_{IH}	Input Voltage, Logic HIGH [1]	2.0			V
I_{OL}	Output Current, Logic LOW [2]			4.0	mA
I_{OH}	Output Current, Logic HIGH [2]			−400	μA
A_{IN}	Input Voltage Range [3]	0.0		1.0	V
T_A	Ambient Temperature Range	0		70	°C

Notes:

1. Applies to logic input pins of the TDC1047 only.
2. Applies to outputs of U5 only.
3. 75 Ohm input impedance, as supplied, U2 offset zeroed.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Min	Max	Units
I_{CC}	Positive Supply Current	V_{CC} = MAX		100	mA
I_{EE}	Negative Supply Current	V_{EE} = MAX		245	mA
Z_{IN}	Input Impedance		70	80	Ohms
I_{IL}	Input Current, Logic LOW[1]	V_{CC} = MAX, VI = 0.5V		-0.4	mA
I_{IH}	Input Current, Logic HIGH[1]	V_{CC} = MAX, VI = 2.4V		50	μA
V_{OL}	Output Voltage, Logic LOW[2]	V_{CC} = MIN, I_{OL} = 4mA		0.5	V
V_{OH}	Output Voltage, Logic HIGH[2]	V_{CC} = MIN, I_{OH} = -400 μA	2.4		V

Notes:
1. Applies to the TDC1047 logic inputs only.
2. Applies to U5 outputs only.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Min	Max	Units
F_S	Maximum Conversion Rate	V_{CC} = MIN, V_{EE} = MIN	20		MHz
t_{STO}	Sampling Time Offset[1]			7	ns
t_D	Output Delay Time[2]	V_{CC} = MIN, V_{EE} = MIN		30	ns
t_{HO}	Output Data Hold Time[1]	V_{CC} = MIN, V_{EE} = MAX	15		ns

Notes:
1. Applies to TDC1047 only.
2. Applies to U5 only.

TDC1047J7C performance characteristics within specified operating conditions[1]

Parameter		Test Conditions	Min	Max	Units
E_{LI}	Integral Linearity Error			0.4	%
E_{LD}	Differential Linearity Error			0.4	%
BW	Bandwidth Full-Power Input		7		MHz
DP	Differential Phase	NTSC @ 4x Color Subcarrier (14.32MHz)		1.5	degree
DG	Differential Gain	NTSC @ 4x Color Subcarrier (14.32MHz)		2.5	%

Note:
1. Items listed in this table apply to the A/D converter only. Contributions to these parameters from the buffer amplifier are not significant.

Calibration

The evaluation board is calibrated by adjusting the offset and gain trim resistors, R8 and R9. Offset can be calibrated when a voltage 1/2 LSB greater than "zero-scale" is applied to the board input. The "OFFSET" pot is then turned to a point where the output data toggles between "0000000" and "0000001." Gain is calibrated by applying a voltage 1/2 LSB less than full-scale and turning the "GAIN" pot until the output data toggles between "1111110" and "1111111."

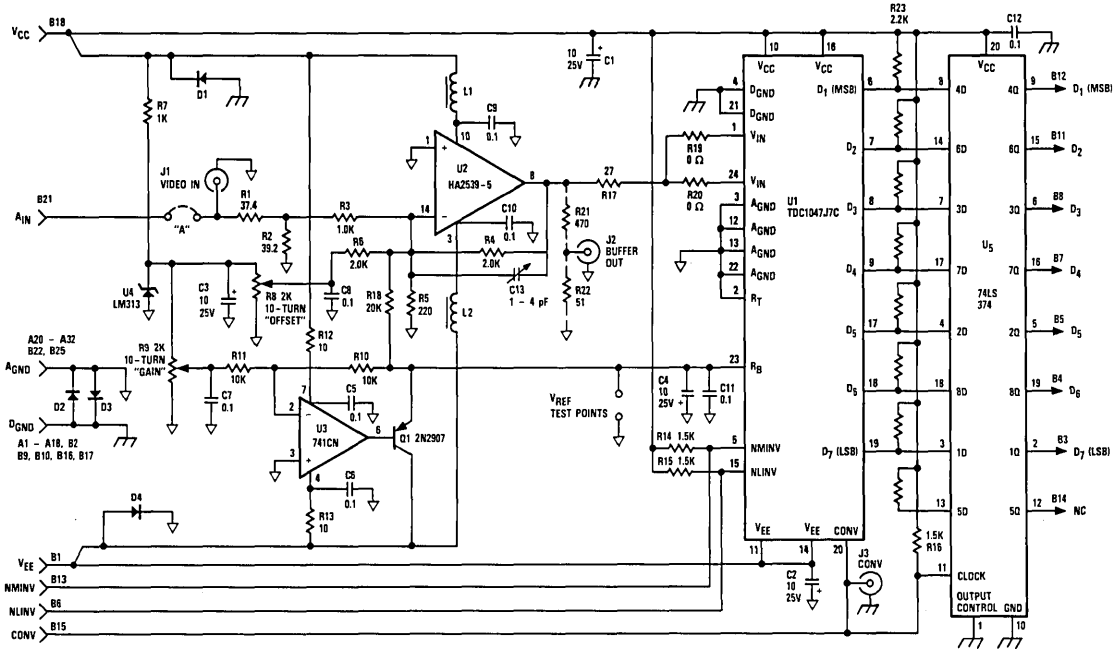
Output Coding Table [1]

Input Voltage	Binary		Two's Complement	
	True	Inverted	True	Inverted
	NMINV = 1 NLINV = 1	0 0	0 1	1 0
0.0000	0000000	1111111	1000000	0111111
+0.0079	0000001	1111110	1000001	0111110
•	•	•	•	•
•	•	•	•	•
+0.4960	0111111	1000000	1111111	0000000
+0.5079	1000000	0111111	0000000	1111111
•	•	•	•	•
•	•	•	•	•
+0.9921	1111110	0000001	0111110	1000001
+1.0000	1111111	0000000	0111111	1000000

Note:

1. Input voltages are at code centers and buffer amplifier offset voltage is nulled.

Figure 2. Schematic of Evaluation Board



Notes for Figure 2. Schematic of Evaluation Board

1. All capacitor values are in microfarads (μF).
2. All capacitor voltage ratings are 50WVDC unless otherwise noted.
3. All resistors are 1/4W unless otherwise noted.
4. All resistor values are in Ohms.
5. All diodes are 1N4001.

Miscellaneous Evaluation Board Parts

Eurocard connector DIN 41612B 2-row 64-contact board mount male	Winchester 64P-6033-0430
Eurocard connector DIN 41612B 2-row 64-contact wire-wrap female	Winchester 64S-6033-0422-1
J1-J3 SMA coax connector (J2, J3 not included)	Sealectro 50-651-0000-31 or Omni-spectra 2062-0000-00
L1, L2 ferrite bead inductors	Fair-Rite Corp. 2743001112

Input Resistor Selection Table (values in Ohms)

	Input Voltage Range									
Z_{IN}	1V		2V		4V		5V		10V	
	R1	R2	R1	R2	R1	R2	R1	R2	R1	R2
50	24.9	25.5	37.4	12.7	43.2	6.19	45.3	4.99	47.5	2.49
75	37.4	39.2	56.2	19.1	64.9	9.53	68.1	7.50	71.5	3.74
93	46.4	48.7	69.8	23.7	80.6	11.8	84.5	9.31	88.7	4.64
1K	499	1000	750	332	866	143	909	110	953	52.3

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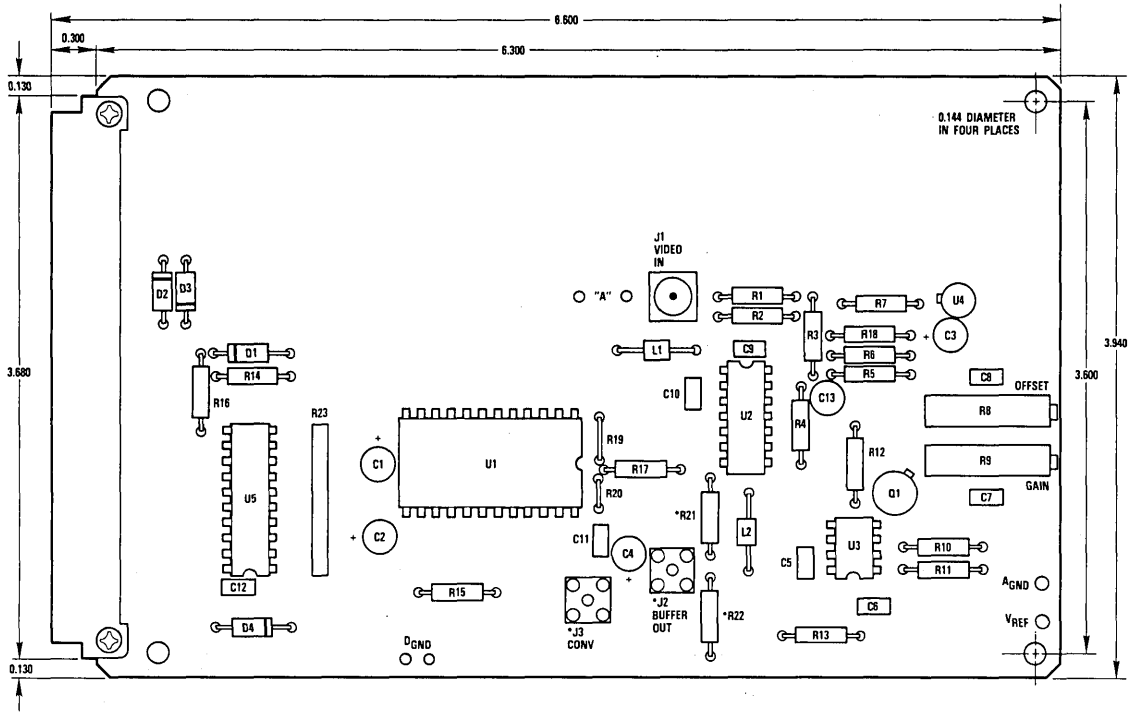
For input voltage ranges and input impedances not covered by the Input Resistor Selection Table, the following formulas may be used to calculate R1 and R2:

$$R2 = \frac{1}{\left(\frac{2VR}{Z_{IN}}\right) + \frac{1}{1000}}$$

$$R1 = Z_{IN} - \left(\frac{1000\ R2}{R2 + 1000}\right)$$

where VR is the desired input voltage range of the board, Z_{IN} is the desired input impedance of the board, and the constant value 1000 is given by the value of R3.

Assembly For TDC1047E1C



Notes:

1. * not supplied.
2. Dimensions in inches.

Ordering Information

Product Number	Description	Order Number
TDC1047E1C	Eurocard Format Board With A/D Converter	TDC1047E1C

TDC1048E1C
Preliminary Information

A/D Converter Evaluation Board
8-bit, 20MSPS

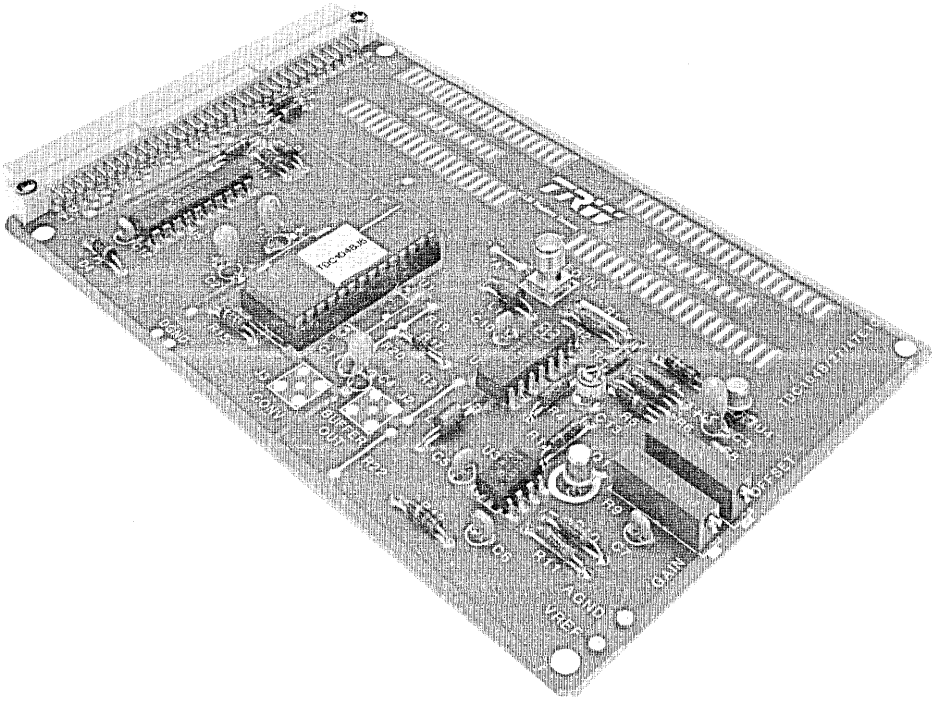
The TDC1048 evaluation board is a fully assembled and tested circuit board designed to aid in the evaluation of TRW's TDC1048 8-bit video analog-to-digital converter. The board contains circuitry for buffering the input signal, generating reference voltages, and latching output data. All digital inputs and outputs are TTL compatible. Provisions are made for gain and offset adjustments. The board requires +5 and -5.2 Volt power supplies. The board is configured to interface with the Eurocard (DIN 41612B) connector format.

Features

- Includes TDC1048 8-Bit A/D Converter
- User-Selectable Input Impedance
- User-Selectable Input Voltage Range
- Unipolar Or Bipolar Operation
- Gain And Offset Calibration Controls
- Operates From +5.0 And -5.2 Volt Power Supplies
- Digital Output Buffers Included
- Eurocard Connector Format
- Uncommitted Prototyping Area

Applications

- Evaluation Of TDC1048 A/D Converter
- System Prototyping Aid
- Incoming Inspection Test Fixture



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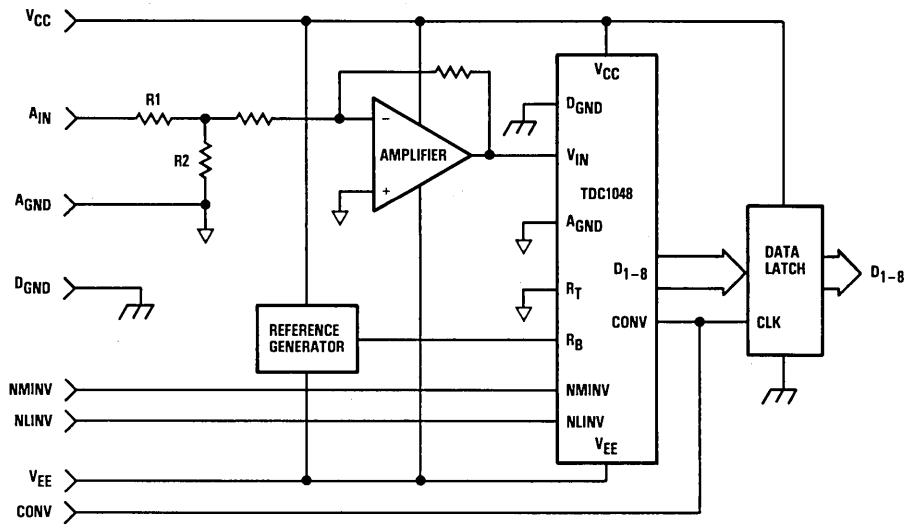
Functional Block Diagram TDC1048



Pin Assignments

D_{GND}	A1	B1	V_{EE}
D_{GND}	A2	B2	D_{GND}
D_{GND}	A3	B3	D_7
D_{GND}	A4	B4	D_6
D_{GND}	A5	B5	D_5
D_{GND}	A6	B6	NLINV
D_{GND}	A7	B7	D_4
D_{GND}	A8	B8	D_3
D_{GND}	A9	B9	D_{GND}
D_{GND}	A10	B10	D_{GND}
D_{GND}	A11	B11	D_2
D_{GND}	A12	B12	D_1 (MSB)
D_{GND}	A13	B13	NMINV
D_{GND}	A14	B14	D_8 (LSB)
D_{GND}	A15	B15	CONV
D_{GND}	A16	B16	D_{GND}
D_{GND}	A17	B17	D_{GND}
D_{GND}	A18	B18	V_{CC}
NC	A19	B19	NC
A_{GND}	A20	B20	NC
A_{GND}	A21	B21	A_{IN}
A_{GND}	A22	B22	A_{GND}
A_{GND}	A23	B23	NC
A_{GND}	A24	B24	NC
A_{GND}	A25	B25	A_{GND}
A_{GND}	A26	B26	NC
A_{GND}	A27	B27	NC
A_{GND}	A28	B28	NC
A_{GND}	A29	B29	NC
A_{GND}	A30	B30	NC
A_{GND}	A31	B31	NC
A_{GND}	A32	B32	NC

TDC1048E1C

Functional Description

General Information

The TDC1048 evaluation board consists of four circuit blocks: the buffer amplifier, reference voltage generator, A/D converter, and output data latch. Analog and digital grounds are separated on the board to provide flexibility in system grounding.

Buffer Amplifier

The input buffer amplifier has been designed specifically for standard baseband video. This amplifier is optimized for 75 Ohm 1 Volt p-p levels. Its gain factor is -2 and its offset is adjustable so that the A/D converter receives a full-scale input signal from 0 to -2 Volts.

The amplifier drives the A/D converter directly, without an emitter follower stage. Frequency response and pulse response are adjusted by the variable capacitor, C13. The board has provision for a resistive voltage divider and SMA output connector for convenient monitoring of amplifier response.

Voltage Reference

The reference voltage for the TDC1048 is generated by operational amplifier U3 and PNP transistor Q1, which supplies the reference current. System "GAIN" is adjusted by varying potentiometer R9 which controls the reference voltage to the A/D converter. The adjustable reference voltage range to the TDC1048 is 0 to -2.4 Volts.

A/D Converter

The TDC1048 integrated circuit is an 8-bit fully parallel (flash) analog-to-digital converter capable of digitizing an input signal at rates up to 20MSPS (MegaSamples Per Second). A single CONVert (CONV) signal controls the conversion operation of the device. The TDC1048 consists of 255 sampling comparators, encoding logic, and a latched output register. On the rising edge of the CONV signal, the comparators are latched and their outputs encoded. On the next rising edge of the CONV signal that data is transferred to the outputs of the TDC1048.

Output Interface

Data from the TDC1048 is latched by U5 on the rising edge of the CONV signal. This 74LS374 octal edge-triggered latch improves output drive and fan-out capability for the board while adding one clock cycle of pipeline delay. Substituting a 74LS373 for U5 and connecting its clock input to a logic "1" will eliminate the extra pipeline delay while improving the data output drive capability of the board.

Mechanical Design

The TDC1048E1C is designed to be compatible with the "Eurocard" format and mate with a standard 64 conductor Eurocard DIN connector. Mating edge connectors are included with each evaluation board.

The TDC1048E1C evaluation board may also be used with the TDC1047 7-bit A/D converter by removing the TDC1048 socket and installing a 24 lead DIP socket in the footprint oriented at right angles to that of the TDC1048. In addition, electrical changes must be made to the board in order to use the TDC1047. (Refer to TDC1047E1C Data Sheet.)

Standard 28 pin sockets for the TDC1048 integrated circuit are used on the boards. The boards are arranged so that this socket may be replaced by a "Zero Insertion Force" (ZIF) socket when the evaluation board is used as a test fixture.

Power Supplies

The TDC1048E1C evaluation board operates from two power supply voltages: +5.0 and −5.2 Volts. The return path for I_{CC} (current from the +5.0 Volt power supply) is D_{GND}. The return paths for I_{EE} (current from the −5.2 Volt supply) is A_{GND}. It is recommended that all ground pins be used. Diodes D1 through D4 function as voltage clamps, which will prevent damage to the board should improper power supply voltages be applied.

Name	Function	Value	Pin
V_{CC}	Positive Power Supply	+5.0V	B18
V_{EE}	Negative Power Supply	−5.2V	B1
A_{GND}	Analog Ground	0.0V	A20−A32
			B22
			B25
			B28
D_{GND}	Digital Ground	0.0V	A1−A18
			B2
			B9
			B10
			B16
			B17

Analog Input

The TDC1048 evaluation board is supplied with a nominal input impedance of 75 Ohms and an input voltage range of 1 Volt p−p. Both input impedance and input voltage range may be changed for operation in other modes. The values of input resistors R1 and R2 determine the input impedance and voltage range of the evaluation board. Suggested values are shown in the Input Resistor Selection Table for various input impedances and voltage ranges. Note that the video input to the board is through an SMA connector (J1, "Video In"). Video input to the board can be routed through the edge connector by installing jumper "A" and using edge connector pin B21.

Name	Function	Value	Pin
A_{IN}	Analog Input Voltage	See Text	B21

Control Inputs

Two control inputs are provided for changing the format of the output data. When NMINV is tied to a logic "0," the most significant bit of the output data is inverted. When NLINV is tied to a logic "0," the seven least significant bits of the output data are inverted. By using these DC controls, the output data can be read in binary, inverse binary, two's complement, or inverse two's complement formats. Output data versus input voltage and control input state is illustrated in the Output Coding Table. Pull−up resistors are provided on the board for disabling these control functions when their pins are left open.

Name	Function	Value	Pin
NMINV	Not Most Significant Bit INVert	TTL	B13
NLINV	Not Least Significant Bit INVert	TTL	B6

Reference

The TDC1048 evaluation board includes circuitry for generating the voltage reference for the A/D converter. This voltage is brought out to a test point (V_{REF}) located on the side of the board opposite that of the edge connector.

Convert

The TDC1048 A/D converter is sampled within 10ns after the rising edge of the CONV signal. Output data is latched on the next rising edge of the CONV signal. Data from U5 is also latched on the rising edge of the CONV signal. U5 adds one clock cycle of pipeline delay to data sent off the board. Note that there are minimum pulse width (t_{PWH}, t_{PWL}) requirements on the waveshape of the CONV signal. A footprint for an SMA connector is located on the board near the A/D converter (J3, CONV) for a convenient monitoring or input point.

Name	Function	Value	Pin
CONV	A/D Clock Input	TTL	B15

Data Outputs

The outputs of the TDC1048 evaluation board are TTL compatible and capable of driving several TTL loads.

Name	Function	Value	Pin
D_1 (MSB)	Most Significant Data Bit	TTL	B12
D_2		TTL	B11
D_3		TTL	B8
D_4		TTL	B7
D_5		TTL	B5
D_6		TTL	B4
D_7		TTL	B3
D_8 (LSB)	Least Significant Data Bit	TTL	B14

No Connects

There are several pins on the TDC1048 evaluation board that have no connection to the circuit. These pins may be left open.

Name	Function	Value	Pin
NC	No Connection	Open	A19
			B19
			B20
			B29–B32

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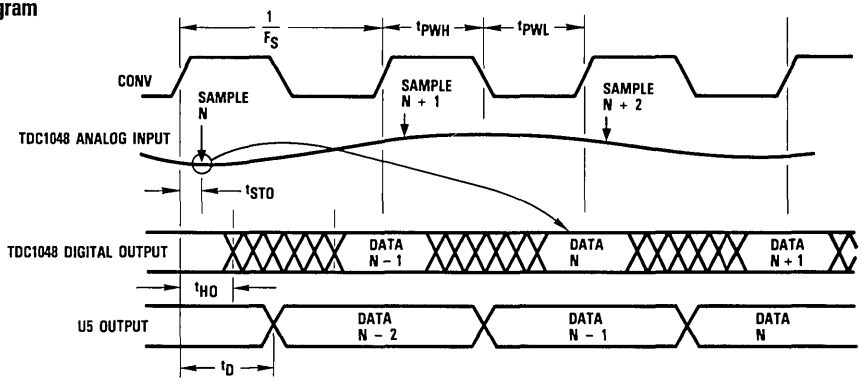
Figure 1. Timing Diagram



Absolute maximum ratings (beyond which the board may be damaged) [1]

Power Supply Voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to −7.0V
A_{GND}(measured to D_{GND})	+0.5 to −0.5V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V

Output

Applied voltage	−0.5 to +5.5V [2]
Applied current externally forced	−1.0 to +6.0mA [3,4]
Short circuit duration (single output in HIGH state to D_{GND})	1 sec.

Temperature

Operating, ambient	−40 to +90°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the board.

Operating conditions

Parameter		Min	Nom	Max	Units
V_{CC}	Positive Power Supply (measured to D_{GND})	4.75	5.0	5.25	V
V_{EE}	Negative Power Supply (measured to A_{GND})	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground (measured to D_{GND})	−0.1	0.0	+0.1	V
t_{PWH}	CONV Pulse Width, HIGH [1]	22			ns
t_{PWL}	CONV Pulse Width, LOW [1]	18			ns
V_{IL}	Input Voltage, Logic LOW [1]			0.8	V
V_{IH}	Input Voltage, Logic HIGH [1]	2.0			V
I_{OL}	Output Current, Logic LOW [2]			4.0	mA
I_{OH}	Output Current, Logic HIGH [2]			−400	μA
A_{IN}	Input Voltage Range [3]	0.0		1.0	V
T_A	Ambient Temperature Range	0		70	°C

Notes:

1. Applies to logic input pins of the TDC1048 only.
2. Applies to outputs of U5 only.
3. 75 Ohm input impedance, as supplied, U2 offset zeroed.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Min	Max	Units
I_{CC}	Positive Supply Current	V_{CC} = MAX		110	mA
I_{EE}	Negative Supply Current	V_{EE} = MAX		355	mA
Z_{IN}	Input Inpedance		70	80	Ohms
I_{IL}	Input Current, Logic LOW[1]	V_{CC} = MAX, V_I = 0.5V		-0.4	mA
I_{IH}	Input Current, Logic HIGH[1]	V_{CC} = MAX, V_I = 2.4V		50	μA
V_{OL}	Output Voltage, Logic LOW[2]	V_{CC} = MIN, I_{OL} = 4mA		0.5	V
V_{OH}	Output Voltage, Logic HIGH[2]	V_{CC} = MIN, I_{OH} = -400mA	2.4		V

Notes:
1. Applies to the TDC1048 logic inputs only.
2. Applies to U5 outputs only.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Min	Max	Units
F_S	Maximum Conversion Rate	V_{CC} = MIN, V_{EE} = MIN	20		MHz
t_{STO}	Sampling Time Offset[1]		0	10	ns
t_D	Output Delay Time[2]	V_{CC} = MIN, V_{EE} = MIN		28	ns
t_{HO}	Output Data Hold Time[1]	V_{CC} = MIN, V_{EE} = MIN	15		ns

Notes:
1. Applies to TDC1048 only.
2. Applies to U5 only.

TDC1048J6C performance characteristics within specified operating conditions[1]

Parameter		Test Conditions	Min	Max	Units
E_{LI}	Integral Linearity Error			0.2	%
E_{LD}	Differential Linearity Error			0.2	%
BW	Bandwidth Full-Power Input		7		MHz
DP	Differential Phase	NTSC @ 4x Color Subcarrier (14.32MHz)		1.0	degree
DG	Differential Gain	NTSC @ 4x Color Subcarrier (14.32MHz)		2.0	%

Note:
1. Items listed in this table apply to the A/D converter only. Contributions to these parameters from the buffer amplifier are not significant.

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Calibration

The evaluation board is calibrated by adjusting the offset and gain trim resistors, R8 and R9. Offset can be calibrated when a voltage 1/2 LSB greater than "zero-scale" is applied to the board input. The "Offset" pot is then turned to a point where the output data toggles between "00000000" and "00000001." Gain is calibrated by applying a voltage 1/2 LSB less than full-scale and turning the "GAIN" pot until the output data toggles between "11111110" and "11111111."

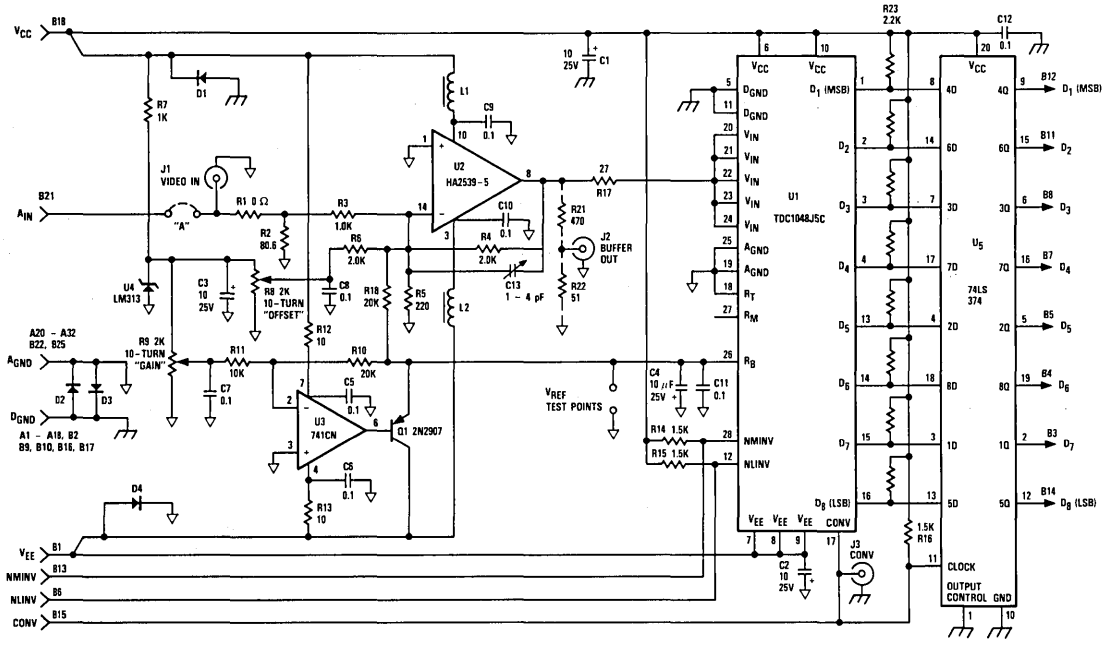
Output Coding Table[1]

Input Voltage	Binary		Two's Complement	
	True	Inverted	True	Inverted
	NMINV=1 NLINV=1	0 0	0 1	1 0
0.0000	00000000	11111111	10000000	01111111
+0.0039	00000001	11111110	10000001	01111110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
+0.4990	01111111	10000000	11111111	00000000
+0.5019	10000000	01111111	00000000	11111111
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
+0.9960	11111110	00000001	01111110	10000001
+1.0000	11111111	00000000	01111111	10000000

Note:

1. Input voltages are at code centers and buffer amplifier offset voltage is nulled.

Figure 2. Schematic of Evalution Board



Notes for Figure 2. Schematic of Evaluation Board

1. All capacitor values are in microfarads (μF).
2. All capacitor voltage ratings are 50WVDC unless otherwise noted.
3. All resistors are 1/8W unless otherwise noted.
4. All resistor values are in Ohms.
5. All diodes are 1N4001.

Miscellaneous Evaluation Board Parts

Eurocard connector DIN 41612B 2-row 64-contact board mount male	Winchester 64P-6033-0430
Eurocard connector DIN 41612B 2-row 64-contact wire-wrap female	Winchester 64S-6033-0422-1
J1-J3 SMA coax connector (J2, J3 not included)	Sealectro 50-651-0000-31 or Omni-spectra 2062-0000-00
L1, L2 ferrite bead inductors	Fair-Rite Products Corp. 2743001112

Input Resistor Selection Table (values in Ohms)

	Input Voltage Range									
Z_{IN}	1V		2V		4V		5V		10V	
	R1	R2	R1	R2	R1	R2	R1	R2	R1	R2
50	0	52.3	24.9	24.3	37.4	12.7	40.2	10	45.3	4.99
75	0	80.6	37.4	39.2	56.2	19.1	60.4	15.4	68.1	7.5
93	0	102	46.4	48.7	69.8	23.7	75	19.1	84.5	9.31
1k	0	open	499	1k	750	332	806	249	909	110

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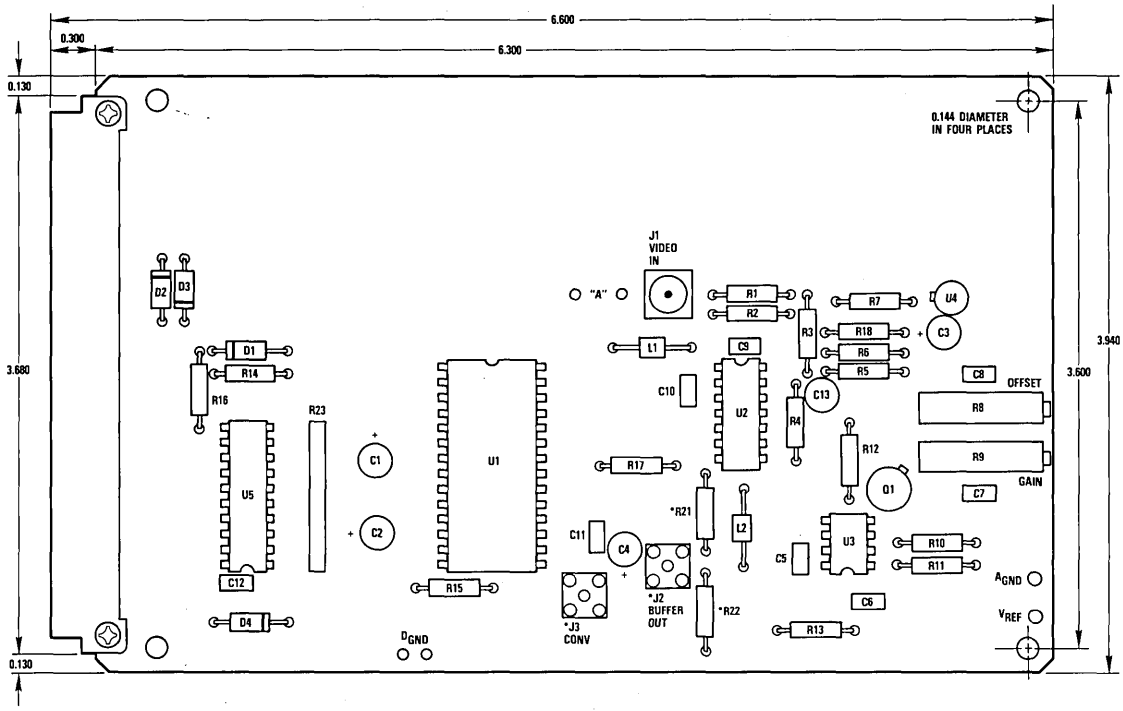
For input voltage ranges and input impedances not covered by the Input Resistor Selection Table, the following formulas may be used to calculate R1 and R2:

$$R2 = \frac{1}{\left(\frac{VR}{Z_{IN}}\right) + \frac{1}{1000}}$$

$$R1 = Z_{IN} - \left(\frac{1000\ R2}{R2 + 1000}\right)$$

where VR is the desired input voltage range of the board, Z_{IN} is the desired input impedance of the board, and the constant value 1000 is given by the value of R3.

Assembly For TDC1048E1C



Note:

1. * not supplied.
2. Dimensions in inches.

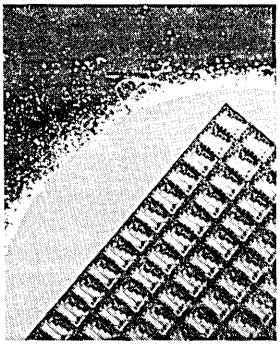
Ordering Information

Product Number	Description	Order Number
TDC1048E1C	Eurocard Format Board With A/D Converter	TDC1048E1C

V L S I

D A T A

B O O K



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Evaluation Boards
D/A Converters
Multipliers
Multiplier-Accumulators
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Reliability
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Application Notes And Reprints (Listings)

TRW LSI's line of monolithic, high-speed D/A converters employ segmented current switching techniques. These D/A converters have resolutions of 4, 8 and 10 bits, and are exceptionally well suited for video, vector, and raster graphics applications. These devices are built with TRW LSI's proven 3D (triple-diffused) bipolar technology which provides significant advantages in performance, size, power, and reliability. The development of fine lithography techniques has yielded faster, more accurate, and more economical D/A converters. The TDC1018 and TDC1034 are manufactured with OMICRON-B™, TRW's new 1-micron process.

Operation

D/A converters have four major functional sections: data input registers, decoding logic, output current switches and reference amplifier. The primary function of the data registers is to hold data values constant during conversion. The registers assure precise matching of propagation delays to reduce glitching to a minimum. The decoding logic selects the current switches and special video functions, such as SYNC, BLANK, BRIGHT, and FORCE HIGH. The two analog outputs of the TDC1018 and the TDC1034 are complementary currents, which vary in proportion to the input data, controls, and reference current. The TDC1016 has an internal resistor to provide a voltage output which varies in proportion to the magnitude of input data and reference voltage. The reference amplifier drives the current switches. The full-scale output value may be adjusted over a limited range by varying the reference voltage or current.

Most applications of these devices require no extra registering, buffering, or deglitching. Four special level controls make the TDC1018 and the TDC1034 ideal for RGB raster graphics applications. The TDC1016 can be operated in either TTL or ECL compatible modes, with controls for selecting input data format. Binary, inverse binary, two's complement, and inverse two's complement formats are supported.

Product	Bits	Integral Linearity Error (%)	Conversion Rate[1] (MSPS)	Power Dissipation (Watts)	Package	Notes
TDC1016[2]	8	0.20	20	0.7	J5, J7, C2, B7	TTL/ECL Compatible
	9	0.10	20	0.7	J5, J7, C2, B7	TTL/ECL Compatible
	10	0.05	20	0.7	J5, J7, C2, B7	TTL/ECL Compatible
TDC1018	8	0.20	125	0.8	J7, B7, C3	ECL Compatible
TDC1034	4	0.80	125	0.7	J8, B8	ECL Compatible

Notes: 1. Guaranteed, Worst Case, T_A = 0°C to 70°C.

2. The TDC1016 has 10-bit resolution, and is available in three linearity grades to meet 8, 9, and 10-bit system requirements.

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TDC1016

Video Speed D/A Converter
10-bit, 20MSPS

The TDC1016 is a bipolar monolithic digital-to-analog converter which can convert digital data into an analog voltage at rates up to 20 MegaSamples Per Second (MSPS). The device includes an input data register and operates without an external deglitcher or amplifier.

Operating the TDC1016 from a single -5.2 Volt power supply will bias the digital inputs for ECL levels, while operating from a dual ±5 Volts power supply will bias the digital inputs for TTL levels.

All versions of the TDC1016 are 10-bit digital-to-analog converters, but are available with linearity specifications of either 8, 9, or 10 bits. The TDC1016 is patented under U.S. patent number 3283120 with other patents pending.

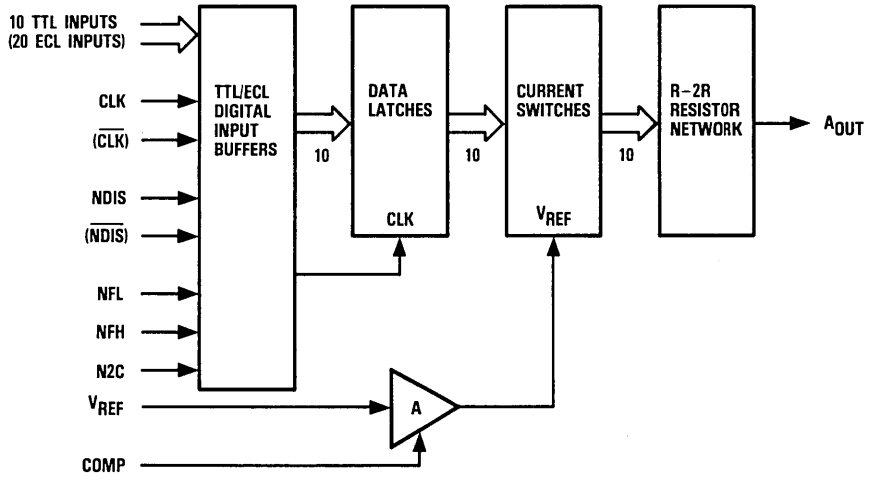
Features

- 20MSPS Conversion Rate
- 8, 9, or 10-Bit Linearity
- Voltage Output, No Amplifier Required
- Single Supply Operation (-5.2V, ECL Compatible)
- Dual Supply Operation (±5.0V, TTL Compatible)
- Internal 10-Bit Latched Data Register
- Low Glitch Energy
- Disabling Controls, Forcing Full-Scale, Zero, And Inverting Input Data
- Binary Or Two's Complement Input Data Formats
- Differential Gain = 1.5%, Differential Phase = 1.0 Degree

Applications

- Construction of Video Signals From Digital Data. 3x Or 4x NTSC Or PAL Color Subcarrier Frequency
- CRT Graphics Displays, RBG, Raster, Vector
- Waveform Synthesis

Functional Block Diagram



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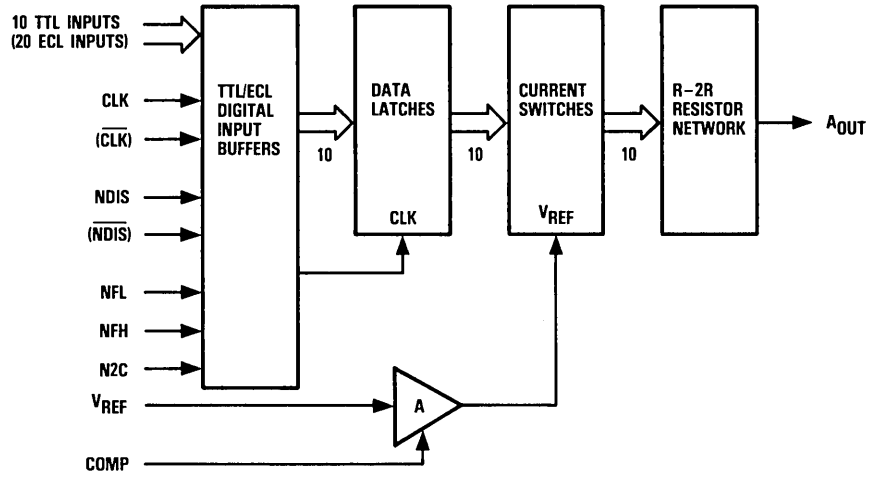
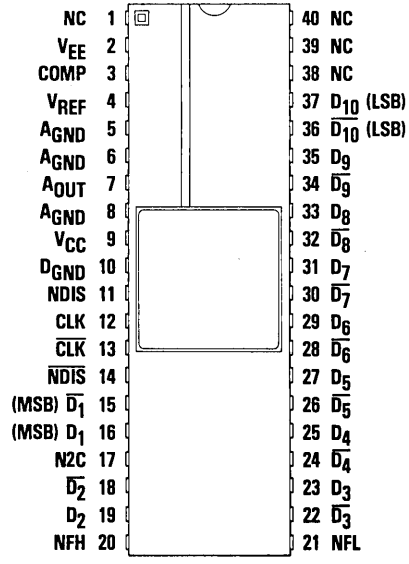
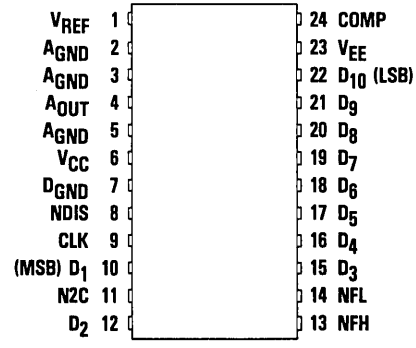
Functional Block Diagram



Pin Assignments

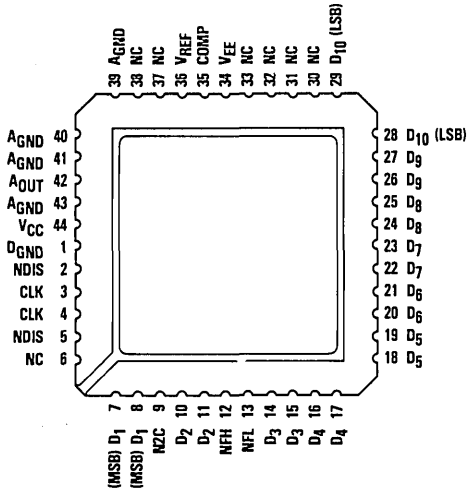


40 Lead DIP – J5 Package



24 Lead DIP – J7 Package
24 Lead CERDIP – B7 Package

Pin Assignments



44 Contact Chip Carrier – C2 Package

Functional Description

General Information

TTL/ECL buffers are used for all digital inputs to the TDC1016. Logic family compatibility depends upon the connection of power supplies. When single power supply (–5.2V) operation is employed, all data, clock, and disable inputs are compatible with differential ECL logic levels. All digital inputs become compatible with TTL levels when dual power supply (±5.0V) operation is used.

The internal 10-bit register latches data on the rising edge of the clock (CLK) pulse. Currents from the current sources are switched accordingly and combined in the resistor network to give an analog output voltage. The magnitude of the output voltage is directly proportional to the magnitude of the digital input word.

The NFL and NFH inputs can be used to simplify system calibration by forcing the analog output voltage to either its zero-scale or full-scale value. The TDC1016 can be operated in binary, inverse binary, two's complement, or inverse two's complement input data formats.

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Power

The TDC1016 can be operated from a single –5.2 Volts power supply or from a dual ±5.0 Volts power supply. For single power supply operation, V_{CC} is connected to D_{GND} and all inputs to the device become ECL compatible. When V_{CC} is tied to +5.0 Volts, the inputs are TTL compatible.

The return path for the output from the 10 current sources is A_{GND}. The current return path for the digital section is D_{GND}. D_{GND} and A_{GND} should be returned to system power supply ground by way of separate conductive paths to prevent digital ground noise from disturbing the analog circuitry of the TDC1016. All A_{GND} pins must be connected to system analog ground.

Name	Function	Value	J5 Package	C2 Package	J7, B7 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pin 9	Pin 44	Pin 6
V_{EE}	Negative Supply Voltage	–5.0V	Pin 2	Pin 34	Pin 23
A_{GND}	Analog Ground	0.0V	Pins 5, 6, 8	Pins 39, 40, 41, 43	Pins 2, 3, 5
D_{GND}	Digital Ground	0.0V	Pin 10	Pin 1	Pin 7

Reference

The reference input is normally set to −1.0V with respect to A_{GND}. Adjusting this voltage is equivalent to adjusting system gain. The temperature stability of the TDC1016 analog output (A_{OUT}) depends primarily upon the temperature stability of the applied reference voltage.

The internal operational amplifier of the TDC1016 is frequency stabilized by an external 1 microfarad tantalum capacitor connected between the COMP pin and V_{EE}. A minimum of 1 microfarad is adequate for most applications, but 10 microfarads or more is recommended for optimum performance. The negative side of this capacitor should be connected to V_{EE}.

Name	Function	Value	J5 Package	C2 Package	J7, B7 Package
V_{REF}	Reference Voltage In	−1.0V	Pin 4	Pin 36	Pin 1
COMP	Compensation	1 μF	Pin 3	Pin 35	Pin 24

Control

The NDIS inputs are used to disable the TDC1016 by forcing its output to the zero-scale value (current sources off). The NDIS inputs are asynchronous, active without regard to the CLK inputs. The other digital control inputs are synchronous, latched on the rising edge of the CLK pulse.

The rising edge of the CLK pulse transfers data from the input lines to the internal 10-bit register. In TTL mode, the inverted inputs for CLK, DATA, and NDIS are inactive and should be left open.

The Input Coding table illustrates the function of the digital control inputs. A two's complement mode is created by activating N2C with a logic "0." When NFH and NFL are both activated with a logic "0," the input data to the 10-bit register is inverted.

Name	Function	Value	J5 Package	C2 Package	J7, B7 Package
NDIS	Not Disable	TTL/ECL	Pin 11	Pin 2	Pin 8
$\overline{\text{NDIS}}$	Not Disable (Inv)	ECL	Pin 14	Pin 5	
CLK	Clock	TTL/ECL	Pin 12	Pin 3	Pin 9
$\overline{\text{CLK}}$	Clock (Inv)	ECL	Pin 13	Pin 4	
N2C	Not Two's Complement	TTL/ECL	Pin 17	Pin 9	Pin 11
NFH	Not Force HIGH	TTL/ECL	Pin 20	Pin 12	Pin 13
NFL	Not Force LOW	TTL/ECL	Pin 21	Pin 13	Pin 14

Data Input

Data inputs are ECL compatible when single power supply operation is employed. The J5 and C2 packages allow for differential ECL inputs while the J7 and B7 packages have only single-ended inputs. When differential ECL data is used, any data input can be inverted simply by reversing the connections to the true and inverted data input pins. All inverted input pins should be left open if single-ended ECL or TTL modes are used. All data inputs have an internal 40 kOhm pull-up resistor to V_{CC}.

Data Input (Cont.)

Name	Function	Value	J5 Package	C2 Package	J7, B7 Package
D_1	Data Bit 1 (MSB)	TTL/ECL	Pin 16	Pin 8	Pin 10
$\overline{D_1}$	Data Bit 1 (MSB Inv)	ECL	Pin 15	Pin 7	
D_2		TTL/ECL	Pin 19	Pin 11	Pin 12
$\overline{D_2}$		ECL	Pin 18	Pin 10	
D_3		TTL/ECL	Pin 23	Pin 15	Pin 15
$\overline{D_3}$		ECL	Pin 22	Pin 14	
D_4		TTL/ECL	Pin 25	Pin 17	Pin 16
$\overline{D_4}$		ECL	Pin 24	Pin 16	
D_5		TTL/ECL	Pin 27	Pin 19	Pin 17
$\overline{D_5}$		ECL	Pin 26	Pin 18	
D_6		TTL/ECL	Pin 29	Pin 21	Pin 18
$\overline{D_6}$		ECL	Pin 28	Pin 20	
D_7		TTL/ECL	Pin 31	Pin 23	Pin 19
$\overline{D_7}$		ECL	Pin 30	Pin 22	
D_8		TTL/ECL	Pin 33	Pin 25	Pin 20
$\overline{D_8}$		ECL	Pin 32	Pin 24	
D_9		TTL/ECL	Pin 35	Pin 27	Pin 21
$\overline{D_9}$		ECL	Pin 34	Pin 26	
D_{10}	Data Bit 10 (LSB)	TTL/ECL	Pin 37	Pin 29	Pin 22
$\overline{D_{10}}$	Data Bit 10 (LSB Inv)	ECL	Pin 36	Pin 28	

Analog Output

The analog output voltage is negative with respect to A_{GND} and varies proportionally with the magnitude of the input data word. The output resistance at this point is 80 Ohms, nominally.

Name	Function	Value	J5 Package	C2 Package	J7, B7 Package
A_{OUT}	Analog Output Voltage	0V to −1V	Pin 7	Pin 42	Pin 4

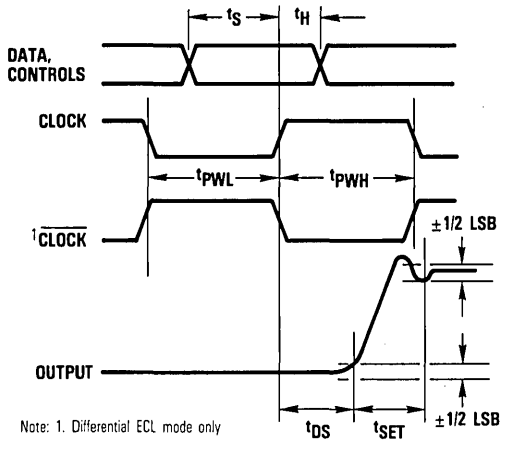
F

No Connect

There are several pins labeled no connect (NC) on the TDC1016 J5 and C2 packages, which have no connections to the chip. These pins should be left open.

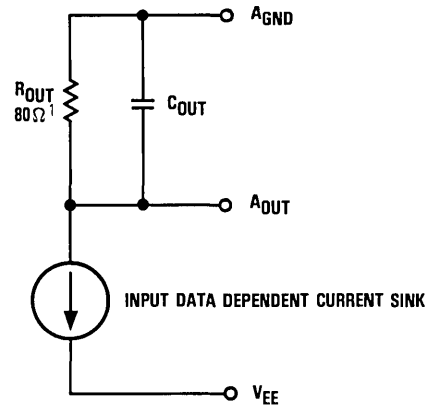
Name	Function	Value	J5 Package	C2 Package	J7, B7 Package
NC	No Connect	Open	Pins 1, 38, 39, 40	Pins 6, 30, 31, 32, 33, 37, 38	None

Figure 1. Timing Diagram



Note: 1. Differential ECL mode only

Figure 2. Analog Output Equivalent Circuit, TTL & ECL Mode



Note: 1. 75Ω requires outside trim

Figure 3. Digital Input Equivalent Circuit, TTL Mode

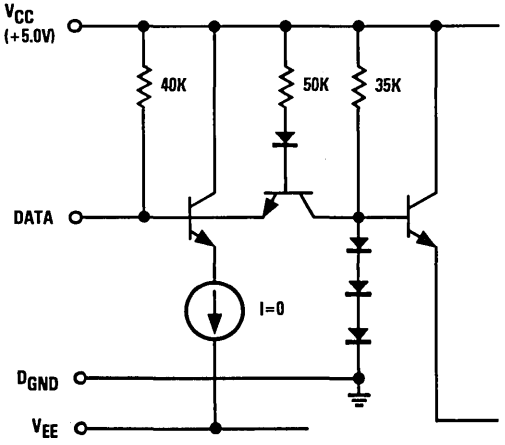
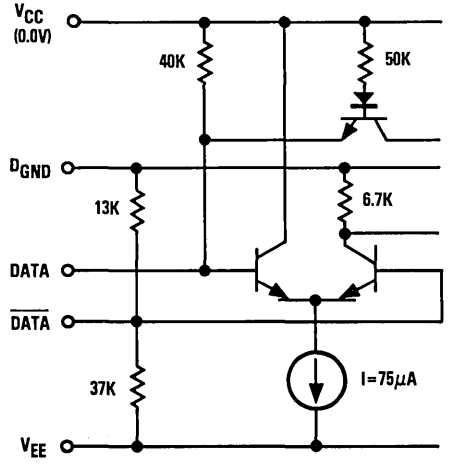


Figure 4. Digital Input Equivalent Circuit, ECL Mode



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltages

V_{CC} (measured To D_{GND})	−0.5 to +7.0V
V_{EE} (measured To A_{GND})	+0.5 to −7.0V
A_{GND} (measured To D_{GND})	+1.0 to −1.0V

Input Voltages

Digital (measured To D_{GND})	+7.0 to −7.0V
Reference (measured To A_{GND})	−1.5 to +0.5V

Output

Applied voltage (measured To A_{GND})	+2.0 to −2.0V [2]
Short-circuit duration	indefinite

Temperature

Operating ambient	+125°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.

Operating conditions

Parameter			Temperature Range: Standard Min	Standard Nom	Standard Max	Extended Min	Extended Nom	Extended Max	Units
V_{CC}	Positive Supply Voltage	TTL Mode	4.75	5.0	5.25	4.50	5.0	5.50	V
		ECL Mode	−0.25	0.0	0.25	−0.25	0.0	0.25	V
V_{EE}	Negative Supply Voltage		−4.5	−5.0	−5.5	−4.5	−5.0	−5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})		−0.1	0.0	0.1	−0.1	0.0	0.1	V
t_{PWL}	CLK Pulse Width, LOW		15			20			ns
t_{PWH}	CLK Pulse Width, HIGH		15			20			ns
t_S	Input Register Set-up Time	TTL Mode	20			20			ns
		ECL Mode	25			25			ns
t_H	Input Register Hold Time		2			2			ns
V_{IL}	Logic "0"	TTL Mode	D_{GND}		0.8	D_{GND}		0.8	V
		ECL Mode			−1.475			−1.475	V
V_{IH}	Logic "1"	TTL Mode	2.0		V_{CC}	2.0		V_{CC}	V
		ECL Mode	−1.105			−1.105			V
V_{REF}	Reference Voltage		−0.8	−1.0	−1.2	−0.8	−1.0	−1.2	V
C_{COMP}	Compensation Capacitor		1.0			1.0			μF
T_A	Ambient Temperature		0		70				°C
T_C	Case Temperature					−55		125	°C

F

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Power Supply Current	TTL Mode, V_{CC} = MAX, V_{EE} = MAX		20		20	mA
I_{EE}	Power Supply Current	TTL Mode, V_{CC} = MAX, V_{EE} = MAX[1]		-120		-150	mA
I_{REF}	Reference Input Current	V_{EE} = MAX, V_{REF} = -1.0V		10		10	μA
I_{IL}	Logic "0" Input Current	TTL Mode, V_{CC} = MAX, V_{EE} = MAX		-1.0		-1.0	mA
		ECL Mode, V_{CC} = 0.0, V_{EE} = MAX		-300		-300	μA
I_{IH}	Logic "1" Input Current	TTL Mode, V_{CC} = MAX, V_{EE} = MAX		75		75	μA
		ECL Mode, V_{CC} = 0.0, V_{EE} = MAX		350		350	μA
C_{OUT}	Output Capacitance	A_{OUT} to A_{GND} (Figure 2)		10		10	pF
C_{IN}	Digital Input Capacitance	Any Digital Input to D_{GND}		35		35	pF
R_{OUT}	Output Resistance	A_{OUT} to A_{GND} (Figure 2)	70	95	70	95	Ohms

Note:

1. Return current from V_{EE} flows through A_{GND}.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_C	Maximum Data Rate	TTL Mode Full-Scale Output Step	20		20		MSPS
		ECL Mode Full-Scale Output Step	18		18		MSPS
t_{DS}	Data Turn-on Delay	RL = 75 Ohms		20		20	ns
t_{SET}	Settling Time	TDC1016-8 to 0.2%		30		30	ns
		TDC1016-9 to 0.1%		35		35	ns
		TDC1016-10 to .05%		40		40	ns
t_{RV}	Output 10% to 90% Risetime	V_{EE} = NOM, RL = 75 Ohms Full-Scale Step		5.5		5.5	ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
RES	Resolution	All TDC1016 Devices		10		10	bits
ELI, ELD	Linearity Error Integral and Differential Terminal Based	TDC1016-8		0.2		0.2	% FS
		TDC1016-9		0.1		0.1	% FS
		TDC1016-10		0.05		0.05	% FS
V_{OFS}	Full-Scale Output Voltage	V_{EE} = NOM V_{REF} = -1.000V	-0.95	-1.05	-0.95	-1.05	Volts
V_{OZS}	Zero-Scale Output Voltage	V_{EE} = NOM, RL = 75 Ohms V_{REF} = -1.000V		±15		±15	mV
DP	Differential Phase	NTSC 4x subcarrier [1]		1.0		1.0	Degree
DG	Differential Gain	NTSC 4x subcarrier [1]		1.5		1.5	%
GE	Glitch "Energy" (Area)	RL = 75 Ohms, Midscale		100		100	pV-sec
GV	Glitch Voltage	RL = 75 Ohms, Midscale		35		35	mV

Note:

1. In excess of theoretical DP and DG due to quantizing error.

Input Coding Table

NDIS	N2C	NFH	NFL	Data	Output	Description
0	x	x	x	xxxxxxxxxx	0.0	Output Disabled
1	1	1	1	1111111111	0.0	Binary (Default State for
1	1	1	1	0000000000	-1.0	TTL Mode Control) Inputs Open
1	1	0	0	1111111111	-1.0	Inverse Binary
1	1	0	0	0000000000	0.0	
1	0	1	1	0111111111	0.0	Two's Complement
1	0	1	1	1000000000	-1.0	
1	0	0	0	0111111111	-1.0	Inverse Two's Complement
1	0	0	0	1000000000	0.0	
1	x	0	1	xxxxxxxxxx	0.0	Force HIGH
1	x	1	0	xxxxxxxxxx	-1.0	Force LOW

Notes:

1. For TTL, $0.0 < V_{IL} < +0.8$ Volts is logic "0"
2. For TTL, $+2.0 < V_{IH} < +5.0$ Volts is logic "1"
3. For ECL, $-1.85 < V_{IL} < -1.47$ Volts is logic "0"
4. For ECL, $-1.10 < V_{IH} < -0.8$ Volts is logic "1"
5. "x" = "don't care"

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Calibration

The TDC1016 is calibrated by adjusting the voltage reference to give the desired full-scale output voltage. The current switches can be turned on either by loading the data register with full-scale data or by bringing the NFH input to a logic zero.

Note that all 10 current switches are activated by the NFH input and the resulting full-scale output voltage will be greater than if the system used only eight or nine bits for full-scale data.

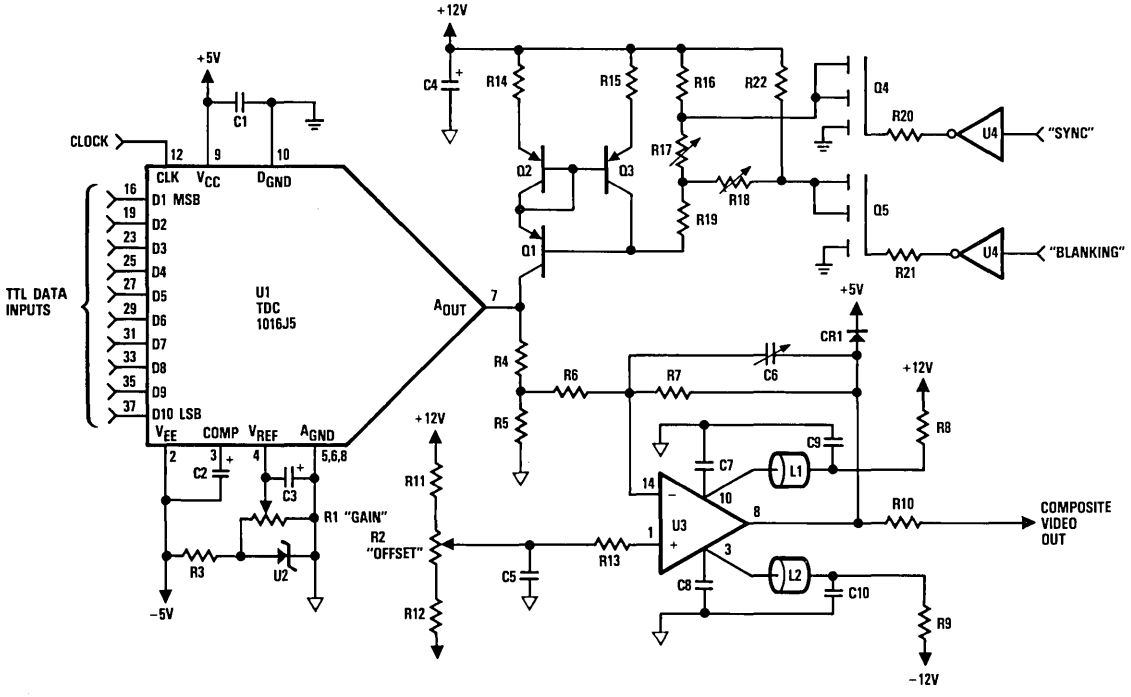
Typical Application

The Typical Interface Circuit (Figure 5) shows the TDC1016 in a typical application, reconstructing video signals from digital data. Television timing signals, SYNC and BLANKING, are added by injecting current from the Wilson current source into a resistor divider circuit at the output of the TDC1016.

The TDC1016 output and currents from the SYNC and BLANKING inputs are summed and amplified by the HA2539 wide-band operational amplifier. Note the careful power supply decoupling at the power input pins of the amplifier. The output of the circuit is a composite video signal with SYNC and BLANKING levels coming from external sources. This technique allows the TDC1016 to use its entire dynamic range for the video information while pulses are added by other means.

The reference for the TDC1016 is generated by dividing the output voltage from a two-terminal band-gap voltage reference. System gain is calibrated by adjusting variable resistor R1. Analog and digital grounds should be routed back to system power supply ground by separate paths.

Figure 5. Typical Interface Circuit



Parts List

Resistors

R1	5K	1/4W	10-turn
R2	1K	1/4W	10-turn
R3	1K	1/4W	5%
R4	43	1/4W	5%
R5	33	1/4W	5%
R6	330	1/4W	5%
R7	750	1/4W	5%
R8,R9	10	1/4W	5%
R10	75	1/4W	2%
R11,R12	10K	1/4W	5%
R13	220	1/4W	5%
R14,R15	100	1/4W	5%
R16,R22	390	1/4W	5%
R17,R18	2K	1/4W	10-turn
R19	1K	1/4W	5%
R20,R21	1K	1/4W	5%

Capacitors

C1	0.01μF	50V
C2	1.0μF	10V
C3	1.0μF	10V
C4	2.2μF	25V
C5	0.1μF	50V
C6	2-5 pF	50V
C7	0.1μF	50V
C8	0.1μF	50V
C9	0.1μF	50V
C10	0.1μF	50V
RF Chokes		
L1,L2	Ferrite beads	

Diodes

CR1	1N4001

Transistors

Q1	2N2907
Q2	2N2907
Q3	2N2907
Q4	2N6660
Q5	2N6660

Integrated Circuits

U1	TRW TDC1016
U2	LM113
U3	HA2539
U4	SN7404

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1016J5CX	T_A = 0°C to 70°C	Commercial	40 Lead DIP	1016J5CX
TDC1016J5GX	T_A = 0°C to 70°C	Commercial With Burn-In	40 Lead Dip	1016J5GX
TDC1016J5FX[3]	T_C = -55°C to 125°C	Commercial	40 Lead Dip	1016J5FX
TDC1016J5AX[3]	T_C = -55°C to 125°C	High Reliability[1]	40 Lead Dip	1016J5AX
TDC1016J7CX	T_A = 0°C to 70°C	Commercial	24 Lead DIP	1016J7CX
TDC1016J7GX	T_A = 0°C to 70°C	Commercial With Burn-In	24 Lead DIP	1016J7GX
TDC1016J7FX[3]	T_C = -55°C to 125°C	Commercial	24 Lead DIP	1016J7FX
TDC1016J7AX[3]	T_C = -55°C to 125°C	High Reliability[1]	24 Lead DIP	1016J7AX
TDC1016B7CX	T_A = 0°C to 70°C	Commercial	24 Lead CERDIP	1016B7CX
TDC1016B7GX	T_A = 0°C to 70°C	Commercial With Burn-In	24 Lead CERDIP	1016B7GX
TDC1016C2CX	T_A = 0°C to 70°C	Commercial	44 Contact Chip Carrier	1016C2CX
TDC1016C2GX	T_A = 0°C to 70°C	Commercial With Burn-In	44 Contact Chip Carrier	1016C2GX
TDC1016C2FX[3]	T_C = -55°C to 125°C	Commercial	44 Contact Chip Carrier	1016C2FX
TDC1016C2AX[3]	T_C = -55°C to 125°C	High Reliability[1]	44 Contact Chip Carrier	1016C2AX

Note:

1. Per TRW document 70Z01757.
2. "X" in part and mark number indicates grade. The TDC1016 devices are available in three grades. Grade "8" is for 8-bit linearity, grade "9" for 9-bit linearity, and grade "10" for 10-bit linearity. The 8-bit version of the B7 (CERDIP) package does not have "-8" marking.
3. The TDC1016 with F or A screening is available in 8 or 9-bit linearity only.

TRW reserves the right to change products and specifications without notice. This information does not convey any license under patent rights of TRW Inc. or others.

TDC1018
Preliminary Information

D/A Converter
8-bit, 125MSPS

The TRW TDC1018 is a 125 MegaSample Per Second (MSPS), 8-bit digital-to-analog converter, capable of directly driving a 75 Ohm load to standard video levels. Most applications require no extra registering, buffering, or deglitching. Four special level controls make the device ideal for video applications. All data and control inputs are ECL compatible.

The TDC1018 is built with TRW's OMICRON-B™ 1-micron bipolar process. On-chip data registers and precise matching of propagation delays make the TDC1018 inherently low-glitching. The TDC1018 offers high performance, low power consumption, and video compatibility in a 24 lead DIP or a 28 Contact Chip Carrier.

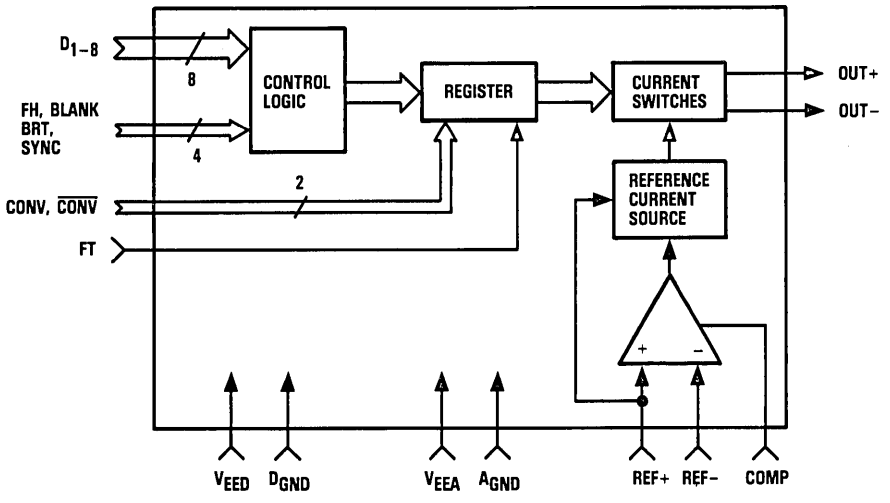
Features

- "Graphics-Ready"
- 125MSPS Conversion Rate
- 8-Bit
- 1/2 LSB Linearity
- Power Supply Noise Rejection > 50dB
- Registered Data And Video Controls
- Differential Current Outputs
- Video Controls: SYNC, BLANK, BRighT, Force High
- Inherently Low Glitch Energy
- ECL Compatible
- Multiplying Mode Capability
- Power Dissipation < 940mW
- Available In 24 Lead DIP And 28 Contact Chip Carrier
- Single -5.2V Power Supply

Applications

- RGB Graphics
- High Resolution Video
- Raster Graphic Displays
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

Functional Block Diagram



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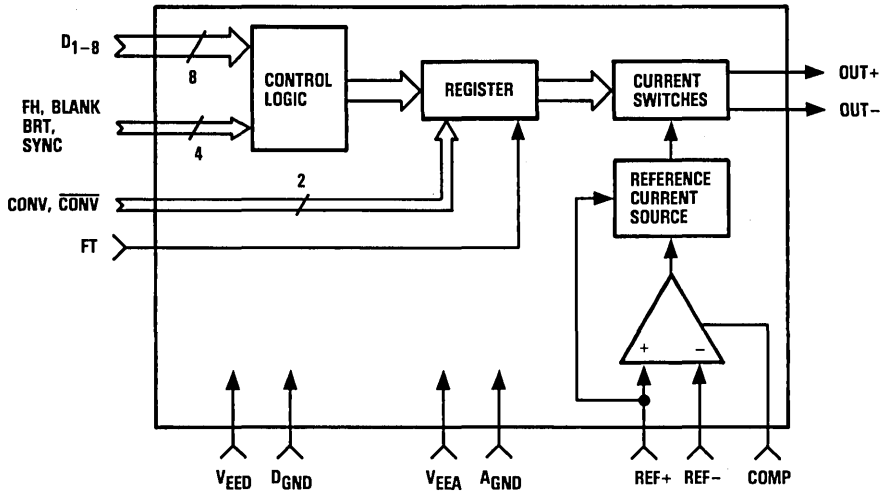
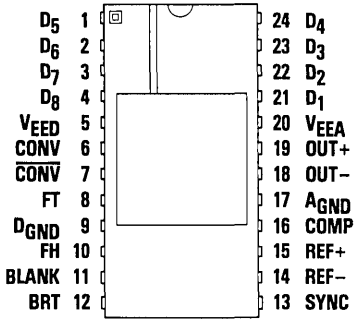
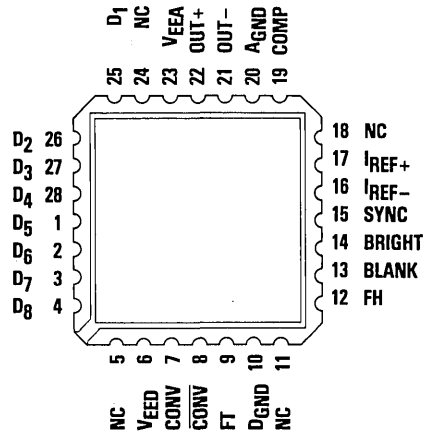
Functional Block Diagram



Pin Assignments



24 Lead DIP – J7 Package



28 Contact Chip Carrier – C3 Package

Functional Description

General Information

The TDC1018 develops complementary analog output currents proportional to the product of the digital input data and analog reference current. All data and control inputs are compatible with standard ECL logic levels. FeedThrough control (FT) determines whether data and control inputs are synchronous or asynchronous. If FT is LOW, each rising edge of the CONVert clock (CONV) latches decoded data and control values into an internal D-type register. The registered values are then converted into the appropriate analog output by switched current sinks. When FT is HIGH, data and control inputs are not registered, and the analog output asynchronously tracks the input values. FT is the only asynchronous input, and is normally used as a DC control.

The TDC1018 uses a segmented approach in which the four MSBs of the input data are decoded into a parallel "Thermometer" code, which drives fifteen identical current sinks to produce sixteen coarse output levels. The LSBs of the input drive four binary-weighted current switches, with a total contribution of one-sixteenth of full scale. The LSB and MSB currents are summed to provide 256 analog output levels.

Special control inputs, SYNC, BLANK, Force High (FH) and BRighT (BRT), drive appropriately weighted current sinks which add to the output current to produce specific output levels especially useful in video applications.

Power

To provide highest noise immunity, the TDC1018 operates from separate analog and digital power supplies, V_{EEA} and V_{EED}, respectively. Since the required voltage for both V_{EEA} and V_{EED} is -5.2V, these may ultimately be connected to the same power source, but individual high-frequency decoupling for each supply is recommended. A typical decoupling network is shown in Figure 7. The return for I_{EED}, the current drawn from the V_{EED} supply, is D_{GND}. The return for I_{EEA} is A_{GND}. All power and ground pins MUST be connected.

Although the TDC1018 is specified for a nominal supply of -5.2V, operation from a +5.0V supply is possible provided that the relative polarities of all voltages are maintained.

Name	Function	Value	J7 Package	C3 Package
V_{EEA}	Analog Supply Voltage	-5.2V	Pin 20	Pin 23
V_{EED}	Digital Supply Voltage	-5.2V	Pin 5	Pin 6
A_{GND}	Analog Ground	0.0V	Pin 17	Pin 20
D_{GND}	Digital Ground	0.0V	Pin 9	Pin 10

F

Reference

The TDC1018 has two reference inputs: REF+ and REF−, which are noninverting and inverting inputs of an internal reference buffer amplifier. The output of this operational amplifier serves as a reference for the current sinks. The feedback loop is internally connected around one of the current sinks to achieve high accuracy (see Figure 4).

The analog output currents are proportional to the digital data and reference current, I_{REF}. The full-scale output value may be adjusted over a limited range by varying the reference current. Accordingly, the stability of the analog output depends primarily upon the stability of the reference. A method of achieving a stable reference is shown in Figure 7.

The reference current is fed into the REF+ input, while REF− is typically connected to a negative reference voltage through a resistor chosen to minimize input offset bias current effects.

A COMPensation input (COMP), is provided for external compensation of the TDC1018's reference amplifier. A capacitor (C_C) should be connected between COMP and the V_{EEA} supply, keeping lead lengths as short as possible. The value of the compensation capacitor determines the effective bandwidth of the amplifier. In general, decreasing C_C increases bandwidth and decreases amplifier stability. For applications in which the reference is constant, C_C should be large, while smaller values of C_C may be chosen if dynamic modulation of the reference is required.

Name	Function	Value	J7 Package	C3 Package
REF−	Reference Current − Input	Op-Amp Virtual Ground	Pin 14	Pin 16
REF+	Reference Current + Input	Op-Amp Virtual Ground	Pin 15	Pin 17
COMP	COMPensation Input	C_C	Pin 16	Pin 19

Controls

The TDC1018 has four special video control inputs: SYNC, BLANK, Force High (FH), and BRighT (BRT), in addition to a clock FeedThrough control (FT). All controls are standard ECL level compatible, and include internal pulldown resistors to force unused controls to a logic LOW (inactive) state.

Typically the TDC1018 is operated in the synchronous mode, which assures the highest conversion rate and lowest spurious output noise. By asserting FT, the input registers are disabled, allowing data and control changes to asynchronously feed through to the analog output. Propagation delay from input change (control or data) to analog output is minimized in the asynchronous mode of operation.

In the synchronous mode, the video control inputs are registered by the rising edge of the CONV clock in a manner similar to the data inputs. The controls, like data, must be present at the inputs for a setup time of t_S (ns) before, and a hold time of t_H (ns) after the rising edge of CONV in order to be registered. In the asynchronous mode, the setup and hold times are irrelevant and minimum pulse widths HIGH and LOW become the limiting factor.

Asserting the video controls produces various output levels which are used for frame synchronization, horizontal blanking, etc., as described in video system standards such as RS-170 and RS-343A. The effect of the video controls on the analog outputs is shown in Table 1. Special internal logic governs the interaction of these controls to simplify their use in video applications. BLANK, SYNC, and Force High override the data inputs. SYNC overrides all other inputs, and produces full negative video output. Force High drives the internal digital data to full scale, giving a reference white video level output. The BRT control creates a "whiter than white" level by adding 10% of the full scale value to the present output level, and is especially useful in graphics displays for highlighting cursors, warning messages, or menus. For non-video applications, the special controls can be left unconnected.

Name	Function	Value	J7 Package	C3 Package
FT	Register FeedThrough Control	ECL	Pin 8	Pin 9
FH	Data Force High Control	ECL	Pin 10	Pin 12
BLANK	Video BLANK Input	ECL	Pin 11	Pin 13
BRT	Video BRighT Input	ECL	Pin 12	Pin 14
SYNC	Video SYNC Input	ECL	Pin 13	Pin 15

Data Inputs

Data inputs to the TDC1018 are standard single-ended ECL level compatible. Internal pulldown resistors force unconnected data inputs to logic LOW. Input registers are provided for synchronous data entry and lowest differential data propagation delay (skew), which minimizes glitching.

In the registered mode, valid data must be present at the input a setup time t_S (ns) before, and a hold time t_H (ns) after the rising edge of CONV. When FT is HIGH, data input is asynchronous and the input registers are disabled. In this case the analog output changes asynchronously in direct response to the input data.

Name	Function	Value	J7 Package	C3 Package
D_1	Data Bit 1 (MSB)	ECL	Pin 21	Pin 25
D_2		ECL	Pin 22	Pin 26
D_3		ECL	Pin 23	Pin 27
D_4		ECL	Pin 24	Pin 28
D_5		ECL	Pin 1	Pin 1
D_6		ECL	Pin 2	Pin 2
D_7		ECL	Pin 3	Pin 3
D_8	Data Bit 8 (LSB)	ECL	Pin 4	Pin 4

Convert

CONVert (CONV) is a differential ECL compatible clock input whose rising edge synchronizes data and control entry into the TDC1018. Within the constraints shown in Figure 2, the actual switching threshold of CONV is determined by $\overline{\text{CONV}}$. CONV may be driven single-ended by connecting $\overline{\text{CONV}}$ to a suitable bias voltage (V_{BB}). The bias voltage chosen will determine the switching threshold of CONV. However, for best performance, CONV must be driven differentially. This will minimize clock noise and power supply/output intermodulation. Both clock inputs must normally be connected, with $\overline{\text{CONV}}$ being the complement of CONV.

Name	Function	Value	J7 Package	C3 Package
CONV	CONVert Clock Input	ECL	Pin 6	Pin 7
$\overline{\text{CONV}}$	CONVert Clock Input, Complement	ECL	Pin 7	Pin 8

Analog Outputs

The two analog outputs of the TDC1018 are high-impedance complementary current sinks which vary in proportion to the input data, controls, and reference current values. The outputs are capable of directly driving a dual 75 Ohm load to standard video levels. The output voltage will be the product of the output current and effective load impedance, and will usually be between 0V and −1.07V in the standard configuration (see Figure 5). In this case, the OUT− output gives a DC shifted video output with "sync down." The corresponding output from OUT+ is also DC shifted and inverted, or "sync up."

Name	Function	Value	J7 Package	C3 Package
OUT−	Output Current −	Current Sink	Pin 18	Pin 21
OUT+	Output Current +	Current Sink	Pin 19	Pin 22

F

Figure 1. Timing Diagram

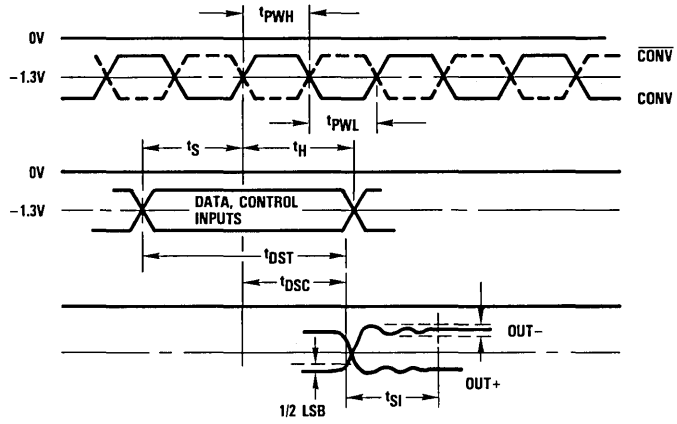


Figure 2. CONVert, CONVert Switching Levels

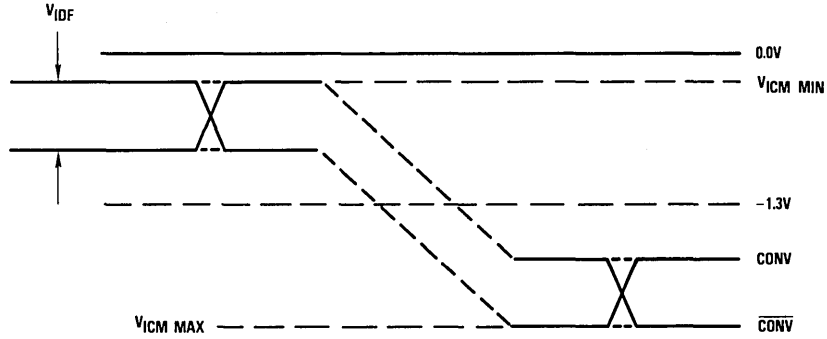


Figure 3. Equivalent Input Circuits

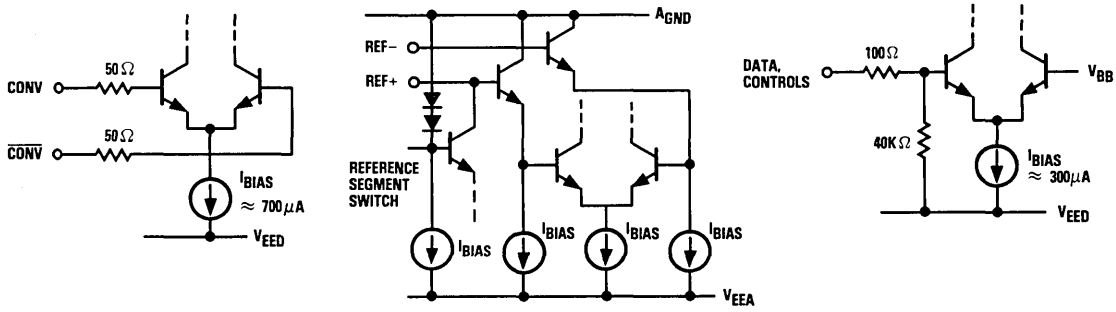


Figure 4. Equivalent Output Circuit

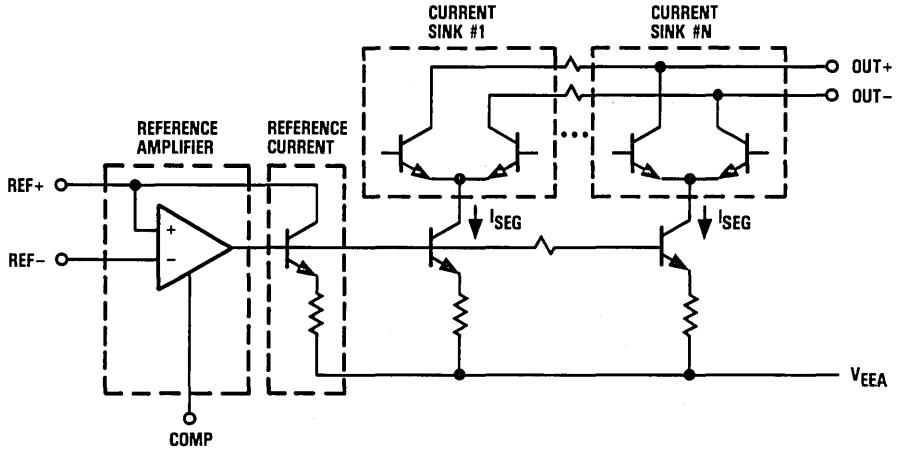
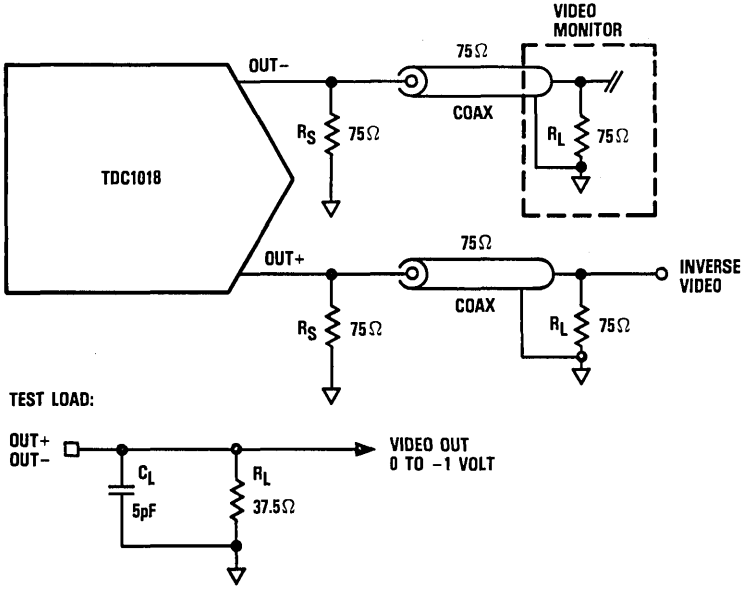


Figure 5. Standard Load Configuration



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Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltages

V_{EED} (measured to D_{GND})	−7.0 to 0.5V
V_{EEA} (measured to A_{GND})	−7.0 to 0.5V
A_{GND} (measured to D_{GND})	−0.5 to 0.5V

Input Voltages

CONV, Data, and Controls (measured to D_{GND})	V_{EED} to 0.5V
Reference input, applied voltage (measured to A_{GND}) [2]	
REF+	V_{EEA} to 0.5V
REF−	V_{EEA} to 0.5V
Reference input, applied current, externally forced [3,4]	
REF+	6.0mA
REF−	0.5mA

Output

Analog output, applied voltage (measured to A_{GND})	
OUT+	−2.0 to +2.0V
OUT−	−2.0 to +2.0V
Analog output, applied current, externally forced [3,4]	
OUT+	50mA
OUT−	50mA
Short circuit duration	Unlimited sec

Temperature

Operating, ambient	−60 to +140°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−60 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

Operating conditions

Parameter			Temperature Range Standard Min	Nom	Max	Units
V_{EED}	Digital Supply Voltage (measured to D_{GND})		-4.9	-5.2	-5.5	V
V_{EEA}	Analog Supply Voltage (measured to A_{GND})		-4.9	-5.2	-5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})		-0.1	0.0	+0.1	V
$V_{EEA}-V_{EED}$	Supply Voltage Differential		-0.1	0.0	+0.1	V
V_{ICM}	CONV Input Voltage, Common Mode Range (Figure 2)		-0.5		-2.5	V
V_{IDF}	CONV Input Voltage, Differential (Figure 2)		0.4		1.2	V
t_{PWL}	CONV Pulse Width, LOW		4			ns
t_{PWH}	CONV Pulse Width, HIGH		4			ns
t_S	Setup Time, Data and Controls		5			ns
t_H	Hold Time, Data and Controls		0			ns
V_{IL}	Input Voltage, Logic LOW		-1.49			V
V_{IH}	Input Voltage, Logic HIGH				-1.045	V
I_{REF}	Reference Current	Video standard output levels[1]	1.059	1.115	1.171	mA
		8-bit linearity	1.0		1.3	mA
C_C	Compensation Capacitor		2000	3900		pF
T_A	Ambient Temperature, Still Air		0		70	°C

Note:

1. Minimum and Maximum values allowed by ±5% variation given in RS343A and RS170 after initial gain correction of device.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Max	Units
$I_{EEA}+I_{EED}$	Supply Current	$V_{EEA} - V_{EED}$ = MAX, static[1]			
		T_A = 0°C to 70°C		170	mA
		T_A = 70°C		130	mA
C_{REF}	Equivalent Input Capacitance, REF+, REF-			5	pF
C_I	Input Capacitance, Data and Controls			5	pF
V_{OCP}	Compliance Voltage, + Output		-1.2	+1.5	V
V_{OCN}	Compliance Voltage, - Output		-1.2	+1.5	V
R_O	Equivalent Output Resistance		20		kOhms
C_O	Equivalent Output Capacitance			20	pF
I_{OP}	Max Current, + Output	V_{EEA} = NOM, SYNC = BLANK = 0, FH = BRT = 1	30		mA
I_{ON}	Max Current, - Output	V_{EEA} = NOM, SYNC = 1	30		mA
I_{IL}	Input Current, Logic LOW, Data and Controls	V_{EED} = MAX, V_I = -1.40V		200	μA
I_{IH}	Input Current, Logic HIGH, Data and Controls	V_{EED} = MAX, V_I = -1.00V		200	μA
I_{IC}	Input Current, Convert	V_{EED} = MAX, $-2.5V < V_I < -0.5V$		50	μA

Note:

1. Worst case over all data and control states.

F

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
F_S	Maximum Conversion Rate	V_{EEA}, V_{EED} = MIN	125		MSPS
t_{DSC}	Clock to Output Delay, Clocked Mode	V_{EEA}, V_{EED} = MIN, FT = 0		8	ns
t_{DST}	Data to Output Delay, Transparent Mode	V_{EEA}, V_{EED} = MIN, FT = 1		13	ns
t_{SI}	Current Settling Time, Clocked Mode	V_{EEA}, V_{EED} = MIN, FT = 0			
		0.2%		10	ns
		0.8%		8	ns
		3.2%		5	ns
t_{RI}	Risetime, Current	10% to 90% of Gray Scale		1.7	ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
E_{LI}	Linearity Error Integral, Terminal Based	V_{EEA}, V_{EED}, I_{REF} = NOM		0.2	% of Gray Scale
E_{LD}	Linearity Error Differential	V_{EEA}, V_{EED}, I_{REF} = NOM		0.2	% of Gray Scale
I_{OF}	Output Offset Current	V_{EEA}, V_{EED} = MAX, SYNC = BLANK = 0, FH = BRT = 1		10	μA
E_G	Absolute Gain Error	V_{EEA}, V_{EED} = MIN, I_{REF} = NOM		±5	% of Gray Scale
TC_G	Gain Error Tempco			±0.024	% of Gray Scale/°C
BWR	Reference Bandwidth, -3dB	C_C = MIN, ΔV_{REF} = 1mV p-p	1		MHz
DP	Differential Phase	4 x NTSC		1.0	Degrees
DG	Differential Gain	4 x NTSC		2.0	%
PSRR	Power Supply Rejection Ratio	V_{EEA}, V_{EED}, I_{REF} = NOM[1]		45	dB
		V_{EEA}, V_{EED}, I_{REF} = NOM[2]		55	dB
PSS	Power Supply Sensitivity	V_{EEA}, V_{EED}, I_{REF} = NOM		120	μA/V
G_C	Peak Glitch Charge	Registered Mode[3,4]		800	fCoulomb
G_I	Peak Glitch Current	Registered Mode		1.2	mA
G_E	Peak Glitch "Energy" (Area)	Registered Mode[4]		30	pV-Sec
FT_C	Feedthrough Clock	Data = Constant[5]		-50	dB
FT_D	Feedthrough Data	Clock = Constant[5]		-50	dB

Notes:

1. 20KHz, ±0.3V ripple superimposed on V_{EEA}, V_{EED}; dB relative to full gray scale.
2. 60Hz, ±0.3V ripple superimposed on V_{EEA}, V_{EED}; dB relative to full gray scale.
3. fCoulombs = microamps x nanoseconds
4. 37.5Ω load. *Because glitches tend to be symmetric, average glitch area approaches zero.*
5. dB relative to full gray scale, 250MHz bandwidth limit.

Table 1 Video Control Truth Table

Sync	Blank	Force High	Bright	Data Input	Out– (mA)[1]	Out– (V)[2]	Out– (IRE)[3]	Description[4]
1	X	X	X	X	28.57	–1.071	–40	Sync Level
0	1	X	X	X	20.83	–0.781	0	Blank Level
0	0	1	1	X	0.00	0.00	110	Enhanced High Level
0	0	1	0	X	1.95	–0.073	100	Normal High Level
0	0	0	0	000...	19.40	–0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	–0.073	100	Normal High Level
0	0	0	1	000...	17.44	–0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.00	110	Enhanced High Level

Notes:

1. Out+ is complementary to Out–. Current is specified as conventional current when flowing into the device.
2. Voltage produced when driving the standard load configuration (37.5 Ohms). See Figure 5.
3. 140 IRE units = 1.00V.
4. RS-343-A tolerance on all control values is assumed.

Figure 6. Video Output Waveform for Out– and Standard Load Configuration

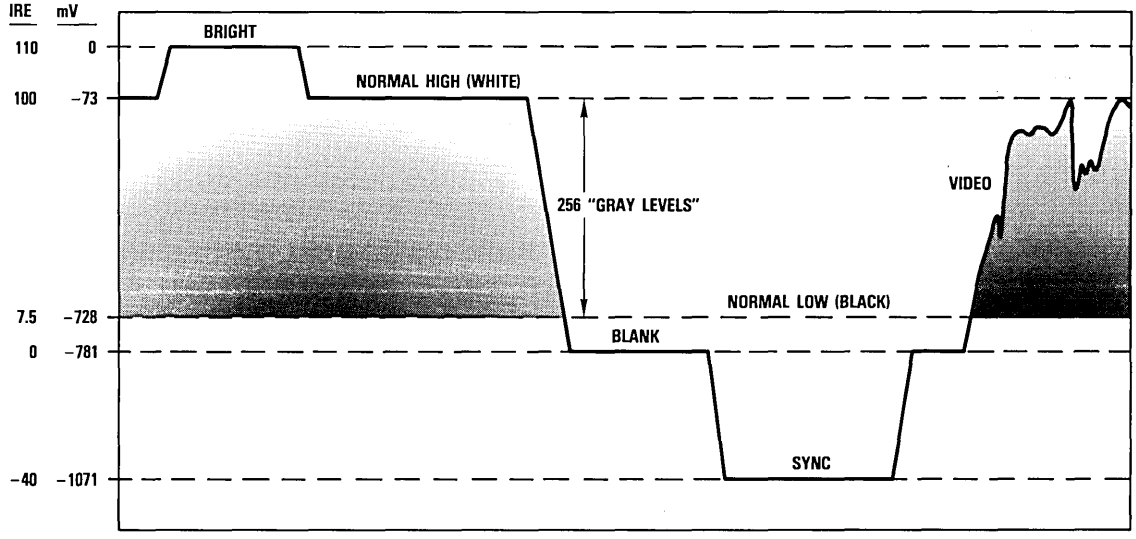

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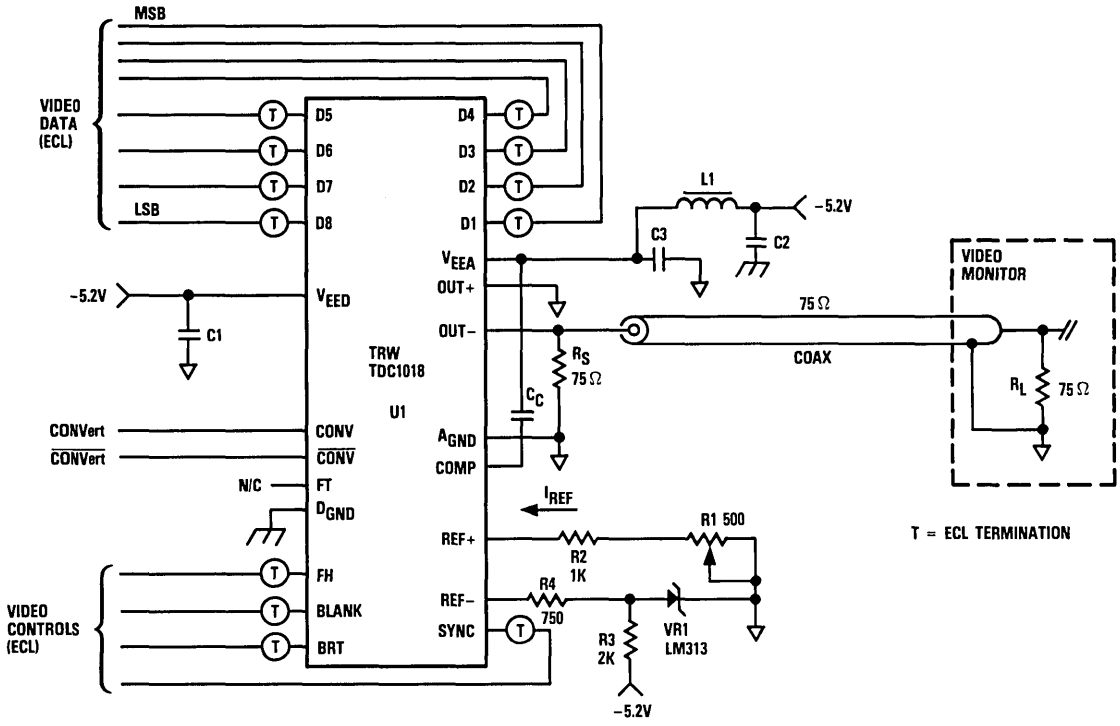
Figure 7. Typical Interface Circuit



Parts List

Resistors

R1	1KΩ	Pot	10 Turn
R2	1.00KΩ	1/8W	1% Metal Film
R3	2.00KΩ	1/8W	1% Metal Film
R4	1.00KΩ	1/8W	1% Metal Film

Capacitors

C1-C3	0.1μF	50V	Ceramic disc
C_C	0.01μF	50V	Ceramic disc

Integrated Circuits

U1	TDC1018	D/A Converter

Voltage References

VR1	LM113 or LM313	Bandgap Reference

Inductors

L1	Ferrite Bead Shield Inductor Fair-Rite P/N 2743001112 or Similar

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1018J7C	STD-T_A = 0°C to 70°C	Commercial	24 Lead DIP	1018J7C
TDC1018J7G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	24 Lead DIP	1018J7G
TDC1018C3C	STD-T_A = 0°C to 70°C	Commercial	28 Contact Chip Carrier	1018C3C
TDC1018C3G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	28 Contact Chip Carrier	1018C3G

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TDC1034

Preliminary Information

D/A Converter
4-bit, 125MSPS

The TRW TDC1034 is a 125 MegaSample Per Second (MSPS), 4-bit digital-to-analog converter, capable of directly driving a 75 Ohm load to standard video levels. Most applications require no extra registering, buffering, or deglitching. Three special level controls make the device ideal for video applications. All data and control inputs are ECL compatible.

The TDC1034 is built with TRW's OMICRON-B™ 1-micron bipolar process. On-chip data registers and precise matching of propagation delays insure low glitch energy. The TDC1034 offers high performance, low power consumption, and video compatibility in an 18 lead DIP package.

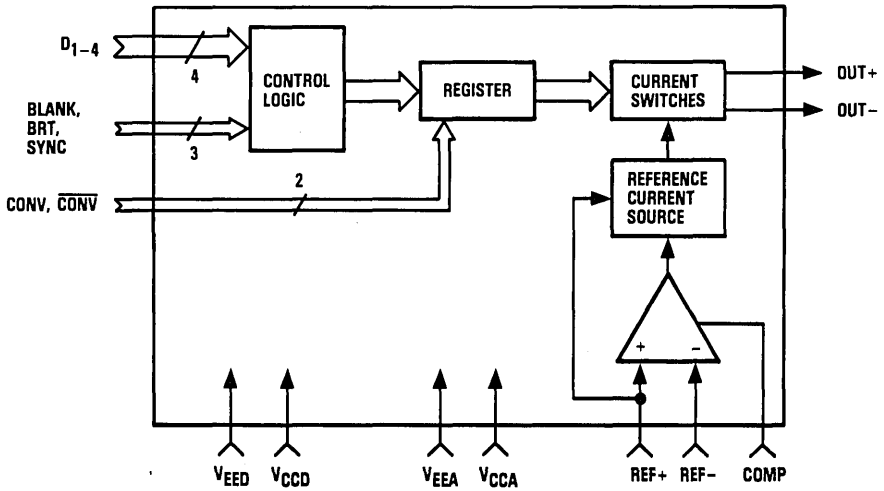
Features

- "Graphics-Ready"
- 125MSPS Conversion Rate
- 1/8 LSB Linearity
- Power Supply Noise Rejection > 50dB
- Registered Data And Video Controls
- Differential Current Outputs
- Video Controls: SYNC, BLANK, BRighT
- Low Glitch Energy
- ECL Compatible
- Low Power Dissipation
- Available In 18 Lead DIP And CERDIP Packages
- Single -5.2V Power Supply

Applications

- CAD
- RGB Graphics
- Raster Graphic Displays
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

Functional Block Diagram



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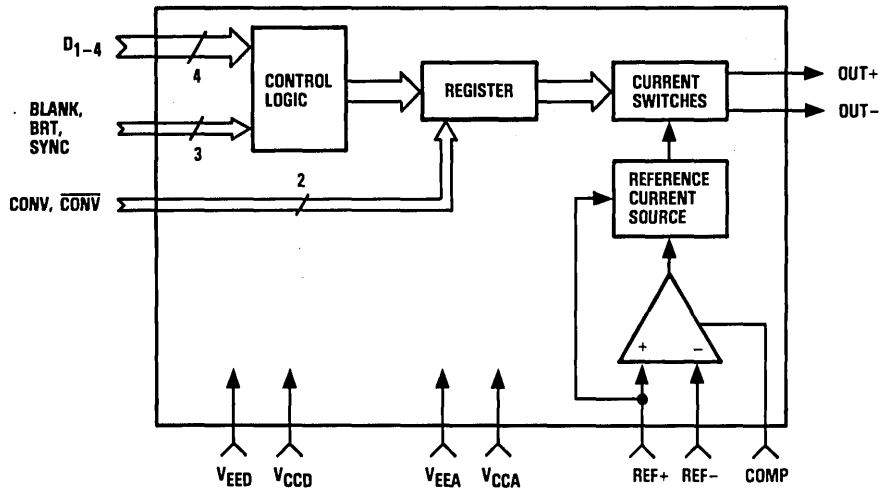
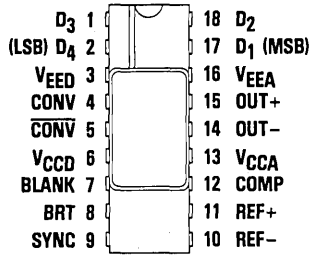
Functional Block Diagram



Pin Assignments



18 Lead DIP - J8 Package
18 Lead CERDIP - B8 Package

Functional Description

General Information

The TDC1034 develops complementary analog output currents proportional to the product of the digital input data and analog reference current. All data and control inputs are compatible with standard ECL logic levels. Each rising edge of the CONVert clock (CONV) latches data and control values into an internal D-type register. The registered values are then converted into an analog output by switched current sinks.

The TDC1034 uses a segmented circuit design scheme in which the input data is decoded into a parallel "Thermometer" code, which drives fifteen identical current sinks to produce sixteen output levels.

Special control inputs, SYNC, BLANK and BRighT (BRT), drive appropriately weighted current sinks which add to the output current to produce specific output levels especially useful in video applications.

Power

To provide highest noise immunity, the TDC1034 operates from separate analog and digital power supplies, V_{EEA} and V_{EED}, respectively. Since the required voltage for both V_{EEA} and V_{EED} is −5.2V, these may ultimately be connected to the same power source, but high-frequency decoupling for each supply is recommended. A typical decoupling network is shown in Figure 7. The return for I_{EED}, the current drawn from the V_{EED} supply, is V_{CCD}. The return for I_{EEA} is V_{CCA}. All V_{EE} and V_{CC} pins MUST be connected.

Although the TDC1034 is specified for a nominal supply of −5.2V, operation from a +5.0V supply is possible provided that the relative polarities of all voltages are correctly maintained.

Name	Function	Value	J8, B8 Package
V_{EEA}	Analog Supply Voltage	−5.2V	Pin 16
V_{EED}	Digital Supply Voltage	−5.2V	Pin 3
V_{CCA}	Analog Supply Voltage	0.0V	Pin 13
V_{CCD}	Digital Supply Voltage	0.0V	Pin 6

Reference

The TDC1034 has two reference inputs: REF+ and REF−, which are noninverting and inverting inputs to an internal reference buffer amplifier. The output of this operational amplifier serves as a reference for the current sinks. The feedback loop is internally connected around one of the current sinks to achieve high accuracy (see Figure 4).

The analog output currents are proportional to the digital data and reference current, I_{REF}. The full scale output value may be adjusted over a limited range by varying the reference current. Accordingly, the stability of the analog output depends primarily upon the stability of the reference. A method of achieving a stable reference is shown in Figure 7.

The reference current flows into the REF+ input, while REF− is typically connected to a negative reference voltage through a resistor chosen to minimize input offset current effects.

A COMPensation input (COMP), is provided for external compensation of the TDC1034's reference amplifier. A capacitor (C_C) should be connected between COMP and the V_{EEA} supply, keeping lead lengths as short as possible. The value of the compensation capacitor determines the effective bandwidth of the amplifier. In general, decreasing C_C increases bandwidth and decreases amplifier stability. For applications in which the reference is constant, C_C should be large, while smaller values of C_C may be chosen when dynamic modulation of the reference is required.

Name	Function	Value	J8, B8 Package
REF−	Reference Current − Input	Op-Amp Virtual Ground	Pin 10
REF+	Reference Current + Input	Op-Amp Virtual Ground	Pin 11
COMP	COMPensation Input	C_C	Pin 12

F

Controls

The TDC1034 has three special video control inputs: SYNC, BLANK and BRighT (BRT). All controls are standard ECL level compatible, and include internal pulldown resistors to force unused controls to a logic LOW (inactive) state.

The video control inputs are registered by the rising edge of the CONV clock in a manner similar to the data inputs. These inputs, like data, must be valid for a setup time of t_S before, and a hold time of t_H after the rising edge of CONV in order to be registered.

Asserting the video controls produces various output levels which are used for frame synchronization, horizontal blanking, etc., as described in video system standards such as RS-170 and RS-343A. The effect of the video controls on the analog outputs is shown in Table 1. Internal logic governs the interaction of these controls to simplify their use in video applications. BLANK and SYNC override the data inputs. SYNC overrides all other inputs, and produces full-scale output. The BRT control creates a "whiter than white" level by adding 10% of the full-scale value to the present output level, and is especially useful in graphics display for highlighting cursors, warning messages, or menus. For non-video applications, these controls may be left unconnected.

Name	Function	Value	J8, B8 Package
BLANK	Video BLANK Input	ECL	Pin 7
BRT	Video BRighT Input	ECL	Pin 8
SYNC	Video SYNC Input	ECL	Pin 9

Data Inputs

Data inputs to the TDC1034 are standard single-ended ECL compatible. Internal pulldown resistors force unconnected data inputs to logic LOW. Input registers are provided for synchronous data entry and lowest differential data propagation delay (skew), which minimizes glitching.

Valid data must be present at the input a setup time t_S before, and a hold time t_H after the rising edge of CONV.

Name	Function	Value	J8, B8 Package
D_1	Data Bit 1 (MSB)	ECL	Pin 17
D_2		ECL	Pin 18
D_3		ECL	Pin 1
D_4	Data Bit 4 (LSB)	ECL	Pin 2

Convert

CONVert (CONV) is a differential ECL compatible clock input whose rising edge synchronizes data and control entry into the TDC1034. Within the constraints shown in Figure 2, the actual switching threshold of CONV is determined by $\overline{\text{CONV}}$. CONV may be driven single-ended by connecting $\overline{\text{CONV}}$ to a suitable bias voltage (V_{BB}). The bias voltage chosen will determine the switching threshold of CONV. However, for best performance, CONV must be driven differentially. This will minimize clock noise and power supply/output intermodulation. Both clock inputs must normally be connected.

Name	Function	Value	J8, B8 Package
CONV	CONVert Clock Input	ECL	Pin 4
$\overline{\text{CONV}}$	CONVert Clock Input, Complement	ECL	Pin 5

Analog Outputs

The two analog outputs of the TDC1034 are high impedance complementary current sinks which vary in proportion to the input data, controls, and reference current values. The outputs are capable of directly driving dual 75 Ohm loads to standard video levels. The output voltage is the product of the output current and effective load impedance, and is usually between 0V and −1.07V in the standard configuration (see Figure 5). In this case, the OUT− output gives a DC shifted video output with "sync down." The corresponding output from OUT+ is also DC shifted and inverted, or "sync up."

Name	Function	Value	J8, B8 Package
OUT−	Output Current −	See Text	Pin 14
OUT+	Output Current +	See Text	Pin 15

Figure 1. Timing Diagram

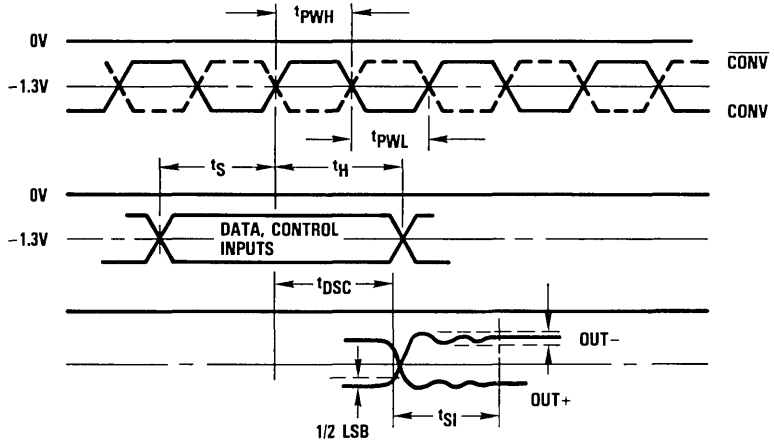


Figure 2. CONV, $\overline{\text{CONV}}$ Switching Levels

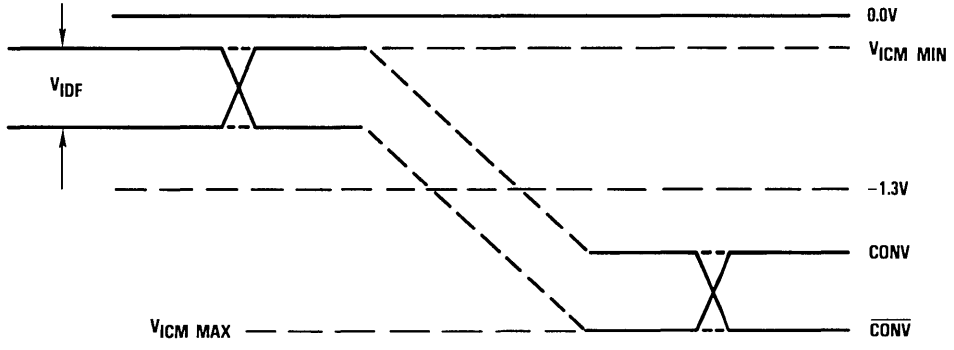


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Figure 3. Equivalent Input Circuits

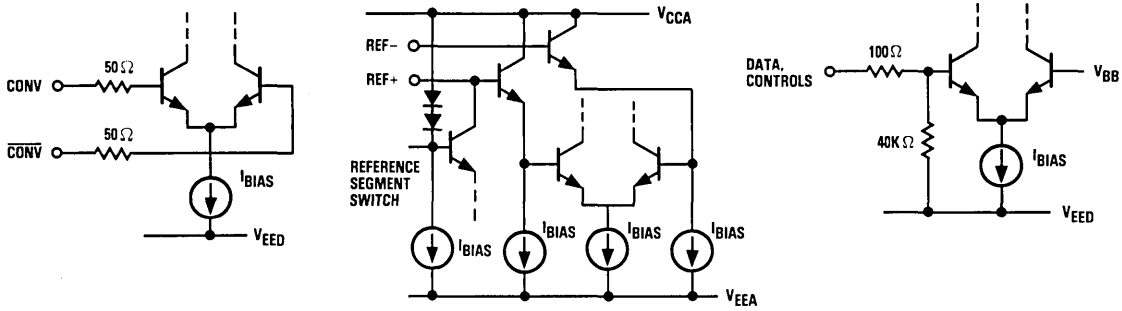


Figure 4. Equivalent Output Circuit

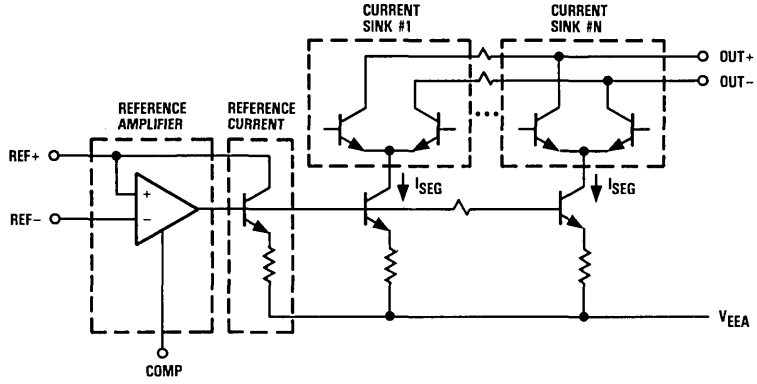
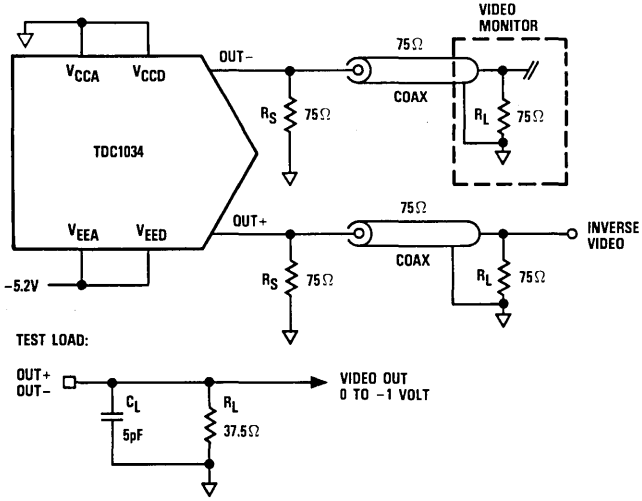


Figure 5. Standard Load Configuration



Absolute maximum ratings (beyond which the device will be damaged)[1]

Supply Voltages

V_{EED} (measured to V_{CCD})	-7.0 to 0.5V
V_{EEA} (measured to V_{CCA})	-7.0 to 0.5V
V_{EEA} (measured to V_{EED})	-0.5 to 0.5V
V_{CCA} (measured to V_{CCD})	-0.5 to 0.5V

Input Voltages

CONV, Data, and Controls (measured to V_{CCD})	V_{EED} to 0.5V
Reference input, applied voltage (measured to V_{CCA})[2]	
REF+	V_{EEA} to 0.5V
REF-	V_{EEA} to 0.5V
Reference input, applied current, externally forced[3,4]	
REF+	6.0mA
REF-	0.5mA

Output

Analog output, applied voltage (measured to V_{CCA})	
OUT+	-2.0 to +2.0V
OUT-	-2.0 to +2.0V
Analog output, applied current, externally forced[3,4]	
OUT+	50mA
OUT-	50mA
Short circuit duration	Unlimited sec

Temperature

Operating, ambient	-60 to +140°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	-60 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

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Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{EED}	Digital Supply Voltage (measured to V_{CCD})	−4.75	−5.2	−5.5	V
V_{EEA}	Analog Supply Voltage (measured to V_{CCA})	−4.75	−5.2	−5.5	V
$V_{CCA}-V_{CCD}$	Supply Voltage Differential	−0.1	0.0	+0.1	V
$V_{EEA}-V_{EED}$	Supply Voltage Differential	−0.1	0.0	+0.1	V
V_{ICM}	CONV Input Voltage, Common Mode Range (Figure 2)	−0.5		−2.5	V
V_{IDF}	CONV Input Voltage, Differential (Figure 2)	0.3		1.2	V
t_{PWL}	CONV Pulse Width, LOW	4			ns
t_{PWH}	CONV Pulse Width, HIGH	4			ns
t_S	Setup Time, Data and Controls	5			ns
t_H	Hold Time, Data and Controls	0			ns
V_{IL}	Input Voltage, Logic LOW	−1.49			V
V_{IH}	Input Voltage, Logic HIGH			−1.045	V
I_{REF}	Reference Current Video standard output levels[1]	1.10	1.17	1.24	mA
	6-bit linearity	1.0		1.3	mA
C_C	Compensation Capacitor	1000	2700		pF
T_A	Ambient Temperature, Still Air	0		70	°C

Note: 1. Minimum and Maximum values allowed by ±5% variation given in RS343A and RS170 after intitial gain correction of device.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Units
$I_{EEA}+I_{EED}$	Supply Current	V_{EEA} = V_{EED} MAX, static[1]			
		T_A = 0°C to 70°C		−145	mA
		T_A = 70°C		−130	mA
C_{REF}	Equivalent Input Capacitance, REF+, REF−			5	pF
C_I	Input Capacitance, Data and Controls			5	pF
V_{OCP}	Compliance Voltage, + Output[2]	Measured with respect to V_{CCA}	−1.2	+1.5	V
V_{OCN}	Compliance Voltage, − Output[2]		−1.2	+1.5	V
R_O	Equivalent Output Resistance		50		K
C_O	Equivalent Output Capacitance			20	pF
I_{OP}	Max Current, + Output	V_{EEA} = NOM, SYNC = BLANK =0, BRT = 1	30		mA
I_{ON}	Max Current, − Output	V_{EEA} = NOM, SYNC = 1	30		mA
I_{IL}	Input Current, Logic LOW, Data and Controls	V_{EED} = MAX, V_I = −1.40V		200	μA
I_{IH}	Input Current, Logic HIGH, Data and Controls	V_{EED} = MAX, V_I = −1.00V		200	μA
I_{IC}	Input Current, Convert	V_{EED} = MAX, $-2.5 < V_I < -0.5$		50	μA

Notes: 1. Worst case over all data and control states.
2. EG ≤ 6% of gray scale.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
F_S	Maximum Conversion Rate	V_{EEA}, V_{EED} = MIN	125		MSPS
t_{DSC}	Clock to Output Delay	V_{EEA}, V_{EED} = MIN		8	ns
t_{SI}	Current Settling Time, Clocked Mode	V_{EEA}, V_{EED} = MIN, 3.2%		5	ns
t_{RI}	Rise Time, Current	10% to 90% of Gray Scale		2.0	ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
E_{LI}	Linearity Error Integral, Terminal Based	V_{EEA}, V_{EED}, I_{REF} = NOM		0.8	% of Gray Scale
E_{LD}	Linearity Error Differential	V_{EEA}, V_{EED}, I_{REF} = NOM		0.8	% of Gray Scale
I_{OF}	Output Offset Current	V_{EEA}, V_{EED} = MAX, SYNC = BLANK = 0, BRT = 1		10	μA
EG	Absolute Gain Error	V_{EEA}, V_{EED} = MIN		6	% of Gray Scale
TC_G	Gain Error Tempco	I_{REF} = NOM		0.01	% of Gray Scale/°C
BWR	Reference Bandwidth, −3dB	C_C = MIN, ΔV_{REF} = 1mV p-p	1		MHz
PSRR	Power Supply Rejection Ratio	V_{EEA}, V_{EED}, I_{REF} = NOM[1]		45	dB
		V_{EEA}, V_{EED}, I_{REF} = NOM[2]		46	dB
PSS	Power Supply Sensitivity	V_{EEA}, V_{EED}, I_{REF} = NOM		120	μA/V
G_C	Peak Glitch Charge[3,4]			800	f Coulomb
G_I	Peak Glitch Current			1.2	mA
G_E	Peak Glitch "Energy" (Area)[4]			30	pV-Sec
FT_C	Feedthrough Clock[5]	Data = Constant BW = 250MHz		−36	dB
		BW = 50MHz		−50	dB
FT_D	Feedthrough Data[5]	CONV = Constant BW = 250MHz		−42	dB
		= 50MHz		−50	dB

Notes:
1. 20KHz, 0.75V p-p ripple superimposed on V_{EEA}, V_{EED}; dB relative to full gray scale.
2. 60KHz, 0.75V p-p ripple superimposed on V_{EEA}, V_{EED}; dB relative to full gray scale.
3. fCoulombs = microamps × nanoseconds.
4. 37.5Ω load. Because glitches tend to be symmetric, average glitch energy approaches zero.
5. dB relative to full gray scale.

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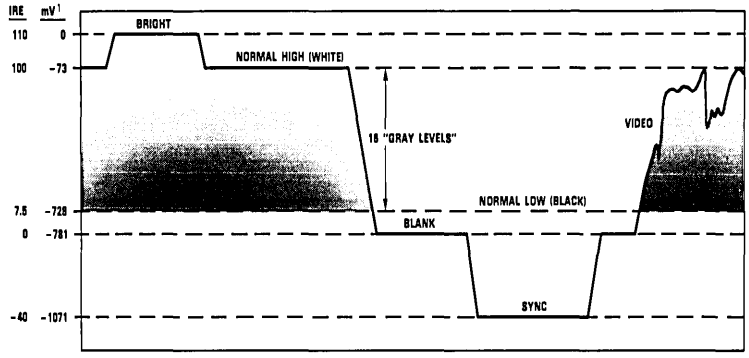
Table 1 Video Control Truth Table

Sync	Blank	Bright	Data Input	Out– (mA)[1]	Out– (V)[2]	Out– (IRE)[3]	Description[4]
1	X	X	X	28.57	–1.071	–40	Sync Level
0	1	X	X	20.83	–0.781	0	Blank Level
0	0	0	0000	19.40	–0.728	7.5	Normal Low Level
0	0	0	1111	1.95	–0.073	100	Normal High Level
0	0	1	0000	17.44	–0.654	7.5	Enhanced Low Level
0	0	1	1111	0.00	0.00	110	Enhanced High Level

Notes:

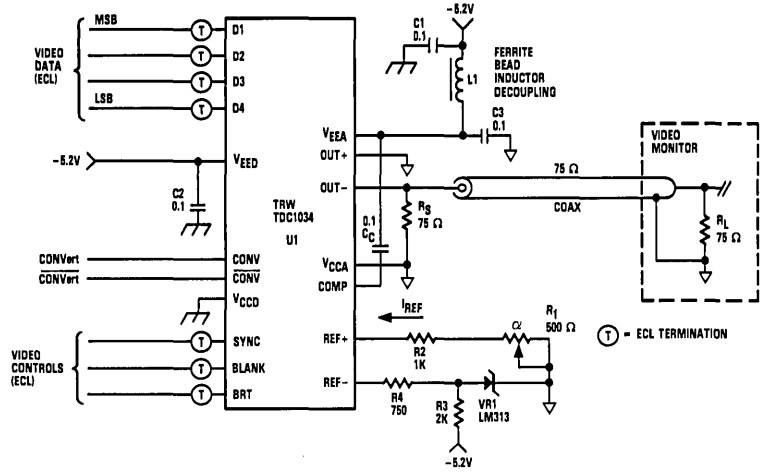
1. Out+ is complementary to Out–. Current is specified as conventional current when flowing into the device.
2. Voltage produced when driving the standard load configuration (37.5 Ohms to V_{CCA}). See Figure 5.
3. 140 IRE units = 1.00V.
4. RS–343–A tolerance on all control values is assumed.

Figure 6. Video Output Waveform for Out– and Standard Load Configuration



Note: 1. Output voltage is measured with standard load connected between Out– and V_{CCA}.

Figure 7. Typical Interface Circuit



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1034J8C	STD-T_A = 0°C to 70°C	Commercial	18 Lead DIP	1034J8C
TDC1034J8G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	18 Lead DIP	1034J8G
TDC1034B8C	STD-T_A = 0°C to 70°C	Commercial	18 Lead CERDIP	1034B8C
TDC1034B8G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	18 Lead CERDIP	1034B8G

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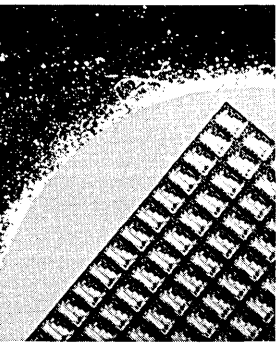
V L S I

D A T A

B O O K



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Product Indexes
Advance Information
A/D Converters
Evaluation Boards
D/A Converters
Multipliers
Multiplier-Accumulators
Special Function Products
Memory/Storage Products
Reliability
Package Information
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Ordering Information
Application Notes And Reprints (Listings)

Digital signal processing (DSP) relies heavily on multiplication. TRW LSI offers a family of parallel multipliers in a variety of word sizes (8, 12, 16 bits) and speeds (40ns to 145ns multiply times). Parallel multipliers accept two n-bit input operands and output the 2n-bit product. Independently clocked registers are provided for the inputs and outputs. Three-state outputs are provided to ease interfacing. All TRW multipliers are TTL compatible.

Multipliers have three functional sections: an input section, the asynchronous multipler array, and the output section. The input section has two n-bit registers, comprised of positive-edge-triggered D-type flip-flops. Except as noted, the operands may be either two's complement or unsigned magnitude numbers.

The asynchronous multiplier array generates the n partial products. The properly weighted partial products are summed by an asynchronous group of adders. The product is rounded and the format is adjusted as appropriate, before entering the product register.

The output section includes the product registers and the three-state output ports. The Most Significant Product (MSP) and the Least Significant Product (LSP) each have their own individually clocked n-bit register. The MSP and LSP have separate three-state output ports.

"H" Series Bipolar Multipliers
The MPY008H/MPY08HU (8-bit), MPY012H (12-bit), and MPY016H (16-bit) devices are fabricated using a two-micron triple-diffused bipolar technology.

"H" Series CMOS Multipliers
The TMC216H (16-bit) is a TRW CMOS multiplier which is pin and function compatible with the bipolar MPY016H. It operates at the same speed with about one-fifth the power dissipation.

"K" Series Bipolar Multipliers
The MPY112K (12-bit) and MPY016K (16-bit) devices have been developed for high-speed applications using TRW's OMICRON-B™ one-micron triple-diffused bipolar technology. The MPY112K has been optimized for minimum package size and operation at video processing speeds (20MHz). The MPY016K is a faster yet pin-compatible version of the MPY016H.

Product	Size	Multiplication Time[1] (ns)	Power Dissipation[2] (Watts)	Package	Notes
MPY008H	8x8	90	2.0	J5, C2	Two's complement
MPY008H-1	8x8	65	2.0	J5, C2	Two's complement
MPY08HU	8x8	90	2.0	J5	Unsigned magnitude
MPY08HU-1	8x8	65	2.0	J5	Unsigned magnitude
MPY012H	12x12	115	3.7	J1, C1, L1, F1	
MPY112K	12x12	50	2.4	J4	16-Bit product
MPY016H	16x16	145	4.6	J1, C1, L1, F1	
MPY016K	16x16	45	4.6	J1, C1, L1	
MPY016K-1	16x16	40	4.6	J1, C1, L1	
TMC216H	16x16	145	.37	J3, C1, L1	CMOS

Notes:

1. Guaranteed, Worst Case, T_A = 0°C to 70°C.
2. Bipolar: Worst Case T_A = 0°C to 70°C.
   CMOS: All inputs toggling at MAX clock rate, unloaded. T_A = 0°C to 70°C.

MPY008H

Multiplier
8 X 8 Bit, 65ns

The MPY008H is a high-speed 8 x 8 bit parallel multiplier which operates at a 65 nanosecond cycle time. The multiplicand and the multiplier are both two's complement numbers, yielding a full-precision 16-bit two's complement product.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The MPY008H is built with TRW's 2-micron bipolar process.

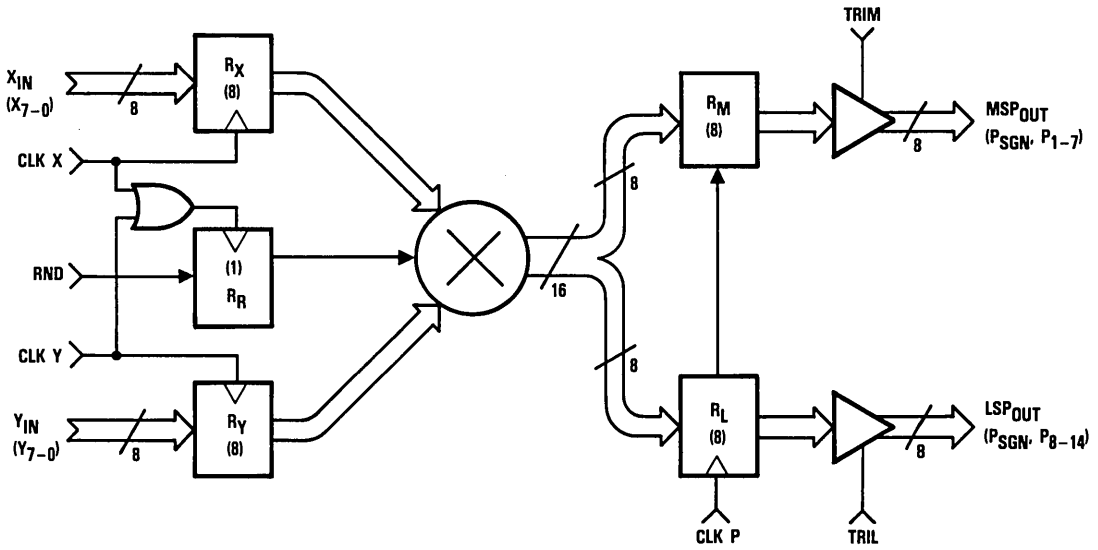
Features

- 65ns Multiply Time: MPY008H-1
- 90ns Multiply Time: MPY008H
- 8 x 8 Bit Parallel Multiplication With 16-Bit Product Output
- Three-State Outputs
- Fully TTL Compatible
- Two's Complement Multiplication
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In 40 Lead Ceramic DIP Or 44 Contact Chip Carrier

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



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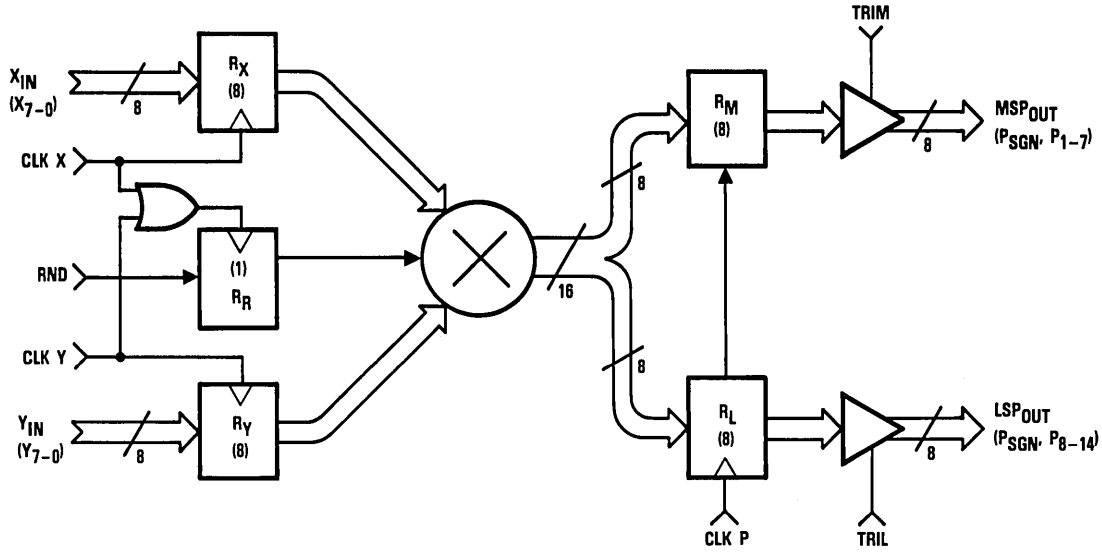
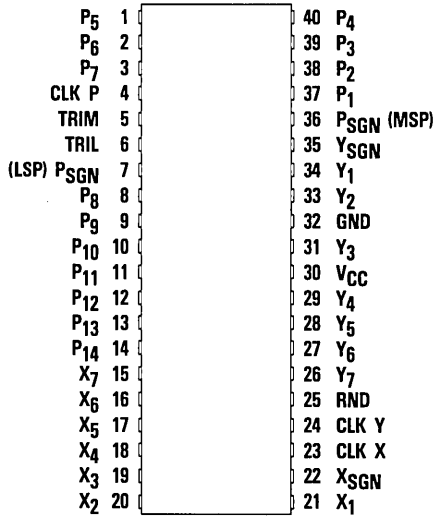
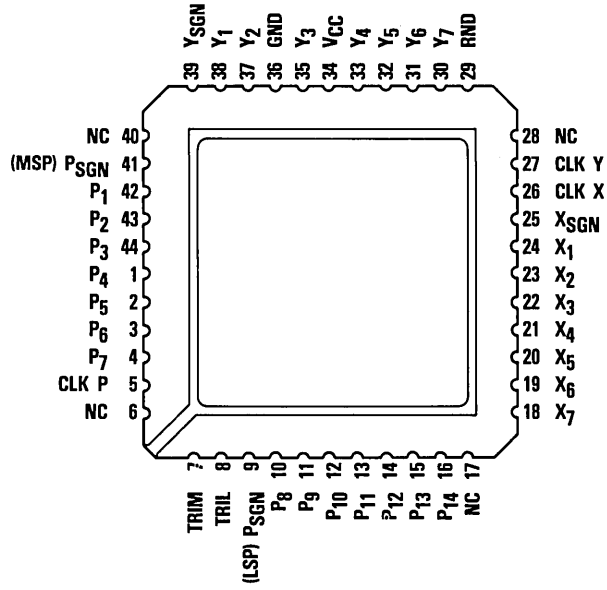
Functional Block Diagram



Pin Assignments



40 Lead DIP – J5 Package



44 Contact Chip Carrier – C2 Package

Functional Description

General Information

The MPY008H has three functional sections: input registers, an asynchronous multiplier array, and output registers. The input registers store the two 8-bit numbers which are to be multiplied and the instruction which controls the output rounding. This rounding control is used when a single-word output is desired. Each input operand is stored independently, simplifying multiplication by a constant. The asynchronous multiplier array is a network of AND gates and adders, designed to handle two's complement numbers only. The output registers hold the product as two 8-bit words, the Most Significant Product (MSP) and the Least Significant Product (LSP). Three-state output drivers allow the MPY008H to be used on a bus, or allow the least and most significant outputs to be multiplexed over the same 8-bit output lines.

Power

The MPY008H operates from a single +5 Volt supply. All power and ground lines must be connected.

Name	Function	Value	J5 Package	C2 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pin 30	Pin 34
GND	Ground	0.0V	Pin 32	Pin 36

Data Inputs

The MPY008H has two 8-bit two's complement data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_{SGN} and Y_{SGN}, carry the sign information for the two's complement notation. The remaining bits are denoted X_1 through X_7 and Y_1 through Y_7 (with X_7 and Y_7 the Least Significant Bits). The input and output formats for fractional two's complement notation and integer two's complement notation are shown in Figures 1 and 2, respectively.

Name	Function	Value	J5 Package	C2 Package
X_{SGN}	X Data Sign Bit (MSB)	TTL	Pin 22	Pin 25
X_1		TTL	Pin 21	Pin 24
X_2		TTL	Pin 20	Pin 23
X_3		TTL	Pin 19	Pin 22
X_4		TTL	Pin 18	Pin 21
X_5		TTL	Pin 17	Pin 20
X_6		TTL	Pin 16	Pin 19
X_7	X Data LSB	TTL	Pin 15	Pin 18
Y_{SGN}	Y Data Sign Bit (MSB)	TTL	Pin 35	Pin 39
Y_1		TTL	Pin 34	Pin 38
Y_2		TTL	Pin 33	Pin 37
Y_3		TTL	Pin 31	Pin 35
Y_4		TTL	Pin 29	Pin 33
Y_5		TTL	Pin 28	Pin 32
Y_6		TTL	Pin 27	Pin 31
Y_7	Y Data (LSB)	TTL	Pin 26	Pin 30

Data Outputs

The MPY008H has a 16-bit two's complement output which is the product of the two input data values. This output is divided into two 8-bit output words, the Most Significant Product (MSP) and Least Significant Product (LSP). The Most Significant Bit (MSB) of both the MSP and the LSP is always the sign bit, P_{SGN}. The input and output formats for fractional two's complement notation and integer two's complement notation are shown in Figures 1 and 2, respectively. Note that since +1 cannot be denoted in fractional two's complement notation while −1 can be, some provision for handling the case (−1) x (−1) must be made. The MPY008H provides a −1 output in this case. As a result, external error handling provisions may be required.

Name	Function	Value	J5 Package	C2 Package
P_{SGN}	Product Sign Bit (MSP)	TTL	Pin 36	Pin 41
P_1		TTL	Pin 37	Pin 42
P_2		TTL	Pin 38	Pin 43
P_3		TTL	Pin 39	Pin 44
P_4		TTL	Pin 40	Pin 1
P_5		TTL	Pin 1	Pin 2
P_6		TTL	Pin 2	Pin 3
P_7		TTL	Pin 3	Pin 4
P_{SGN}	Product Sign Bit (LSP)	TTL	Pin 7	Pin 9
P_8		TTL	Pin 8	Pin 10
P_9		TTL	Pin 9	Pin 11
P_{10}		TTL	Pin 10	Pin 12
P_{11}		TTL	Pin 11	Pin 13
P_{12}		TTL	Pin 12	Pin 14
P_{13}		TTL	Pin 13	Pin 15
P_{14}	Product LSB	TTL	Pin 14	Pin 16

Clocks

The MPY008H has three clock lines, one for each of the input registers and one for the product register. Data present at the inputs of these registers are loaded into the registers at the rising edge of the appropriate clock. The RND input is registered, and clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with loading this control signal can be avoided by the use of normally LOW clocks.

Name	Function	Value	J5 Package	C2 Package
CLK X	Clock Input Data X	TTL	Pin 23	Pin 26
CLK Y	Clock Input Data Y	TTL	Pin 24	Pin 27
CLK P	Clock Product Register	TTL	Pin 4	Pin 5

No Connects

The contact chip carrier version of the MPY008H has four pins which are not connected internally. These should be left unconnected.

Name	Function	Value	J5 Package	C2 Package
NC	No Connection	Open	None	Pins 6, 17, 28, 40

Control

The MPY008H has three control lines:

TRIM,TRIL — Three-state enable lines for the MSP and the LSP. The output driver is in the high-impedance state when TRIM or TRIL is HIGH, and enabled when the appropriate control is LOW.

RND — The RND input is registered, and clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention is required if normally HIGH clock signals are used. Problems with loading these control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J5 Package	C2 Package
RND	Round Control Bit	TTL	Pin 25	Pin 29
TRIM	MSP Three-State Control	TTL	Pin 5	Pin 7
TRIL	LSP Three-State Control	TTL	Pin 6	Pin 8

Figure 1. Fractional Two's Complement Notation

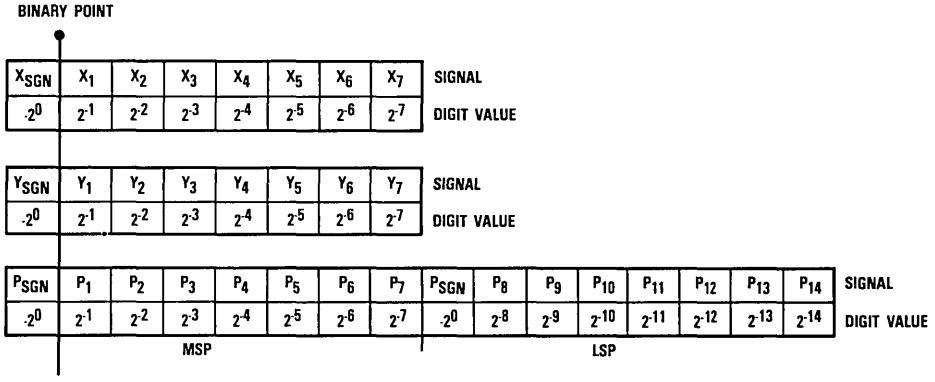


Figure 2. Integer Two's Complement Notation

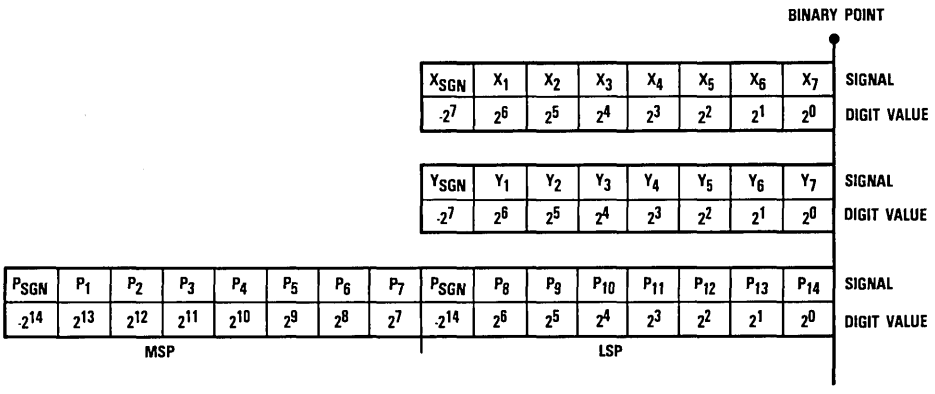


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Figure 3. Timing Diagram

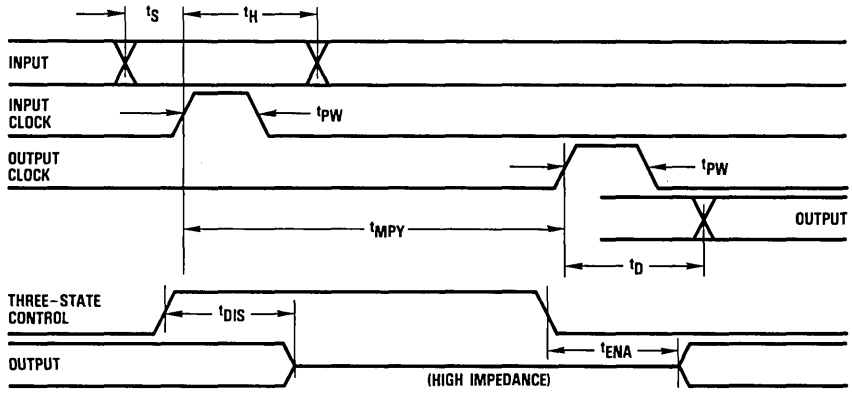
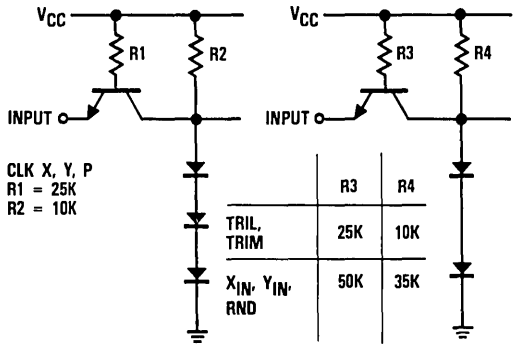


Figure 4. Equivalent Input Circuit



	R3	R4
TRIL, TRIM	25K	10K
X_{IN}, Y_{IN}, RND	50K	35K

Figure 5. Equivalent Output Circuit

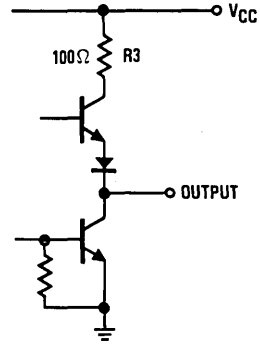


Figure 6. Test Load

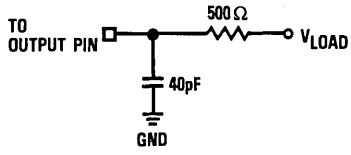
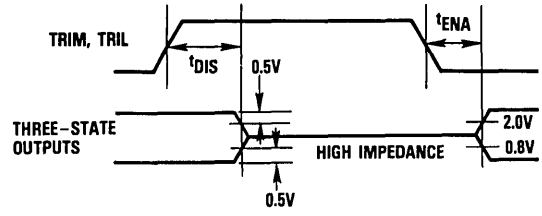


Figure 7. Transition Levels For Three-State Measurements



Application Notes

Multiplication By A Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and that the selected register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection Of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the MPY008H does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64.$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design.

Because common design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 and 2.

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Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage ..... −0.5 to +7.0V

Input

Applied voltage ..... −0.5 to +5.5V [2]

Forced current ..... −6.0 to +6.0mA

Output

Applied voltage ..... −0.5 to +5.5V [2]

Forced current ..... −1.0 to +6.0mA [3,4]

Short-circuit duration (single output in high state to ground) ..... 1 sec.

Temperature

Operating, case ..... −55 to +125°C

junction ..... 175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PW}	Clock Pulse Width	25			30			ns
t_S	Input Register Setup Time	25			30			ns
t_H	Input Register Hold Time	0			3			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		+125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
I_{CC}	Supply Current	V_{CC} = MAX, Static[1]		375		450	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V					
		X_{IN}, Y_{IN}, RND		-0.4		-0.4	mA
		CLK X, CLK Y, TRIM, TRIL		-1.0		-1.0	mA
		CLK P		-2.0		-2.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V					
		X_{IN}, Y_{IN}, RND		75		100	μA
		CLK X, CLK Y, TRIM, TRIL		75		100	μA
		CLK P		150		200	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{CC} = MAX, V_I = 0.4V		-40		-40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{CC} = MAX, V_I = 2.4V		40		40	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = MAX, one pin to ground, one second duration max, output HIGH		-50		-50	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:
1. All inputs and outputs LOW.

Switching characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
t_{MPY}	Multiply Time	V_{CC} = MIN MPY008H-1		65			ns
		V_{CC} = MIN MPY008H		90		115	ns
t_D	Output Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V		40		45	ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 1.8V		40		45	ns
t_{DIS}	Three-State Output Disable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1}[2]		40		45	ns

Notes:
1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in figure 7.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

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Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
MPY008HJ5C	STD-T_A = 0°C to 70°C	Commercial	40 Lead DIP	008HJ5C
MPY008HJ5G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	40 Lead DIP	008HJ5G
MPY008HJ5F	EXT-T_C = -55°C to 125°C	Commercial	40 Lead DIP	008HJ5F
MPY008HJ5A	EXT-T_C = -55°C to 125°C	High Reliability[2]	40 Lead DIP	008HJ5A
MPY008HJ5C1	STD-T_A = 0°C to 70°C	Commercial	40 Lead DIP	008HJ5C1
MPY008HJ5G1	STD-T_A = 0°C to 70°C	Commercial With Burn-In	40 Lead DIP	008HJ5G1
MPY008HC2C	STD-T_A = 0°C to 70°C	Commercial	44 Contact Chip Carrier	008HC2C
MPY008HC2G[1]	STD-T_A = 0°C to 70°C	Commercial With Burn-In	44 Contact Chip Carrier	008HC2G
MPY008HC2F	EXT-T_C = -55°C to 125°C	Commercial	44 Contact Chip Carrier	008HC2F
MPY008HC2A	EXT-T_C = -55°C to 125°C	High Reliability[2]	44 Contact Chip Carrier	008HC2A

Notes:

1. Contact factory for availability.
2. Per TRW document 70Z01757.

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MPY08HU

High-Speed Parallel Multiplier
8 bit, 65ns

The TRW MPY08HU is a high-speed 8-bit parallel multiplier which operates at a 65 nanosecond cycle time (15MHz multiplication rate). The multiplicand and the multiplier are both unsigned magnitude numbers, yielding a full-precision 16-bit product.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. Three-state outputs with separate output enable lines for the MSP and the LSP are employed.

The MPY08HU is built with TRW's radiation hard 2-micron process, and is the unsigned magnitude version of the industry standard MPY008H.

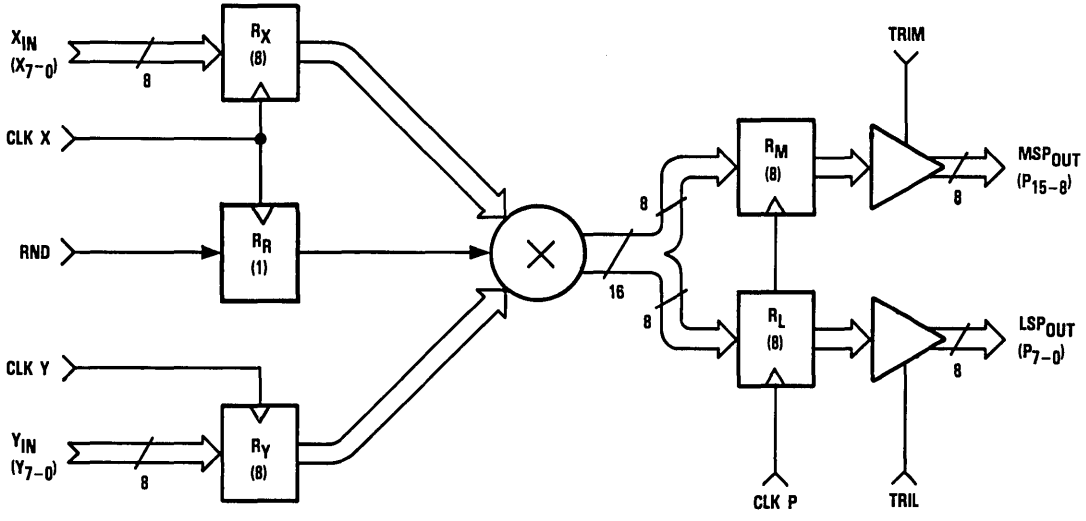
Features

- 65ns Multiply Time: MPY08HU-1
- 90ns Multiply Time: MPY08HU
- 8 x 8 Bit Parallel Multiplication With 16-Bit Product Output
- Independent Most Significant Product and Least Significant Product Outputs
- Three-State Outputs
- Fully TTL Compatible
- Unsigned Magnitude Multiplication
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In 40 Lead DIP

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



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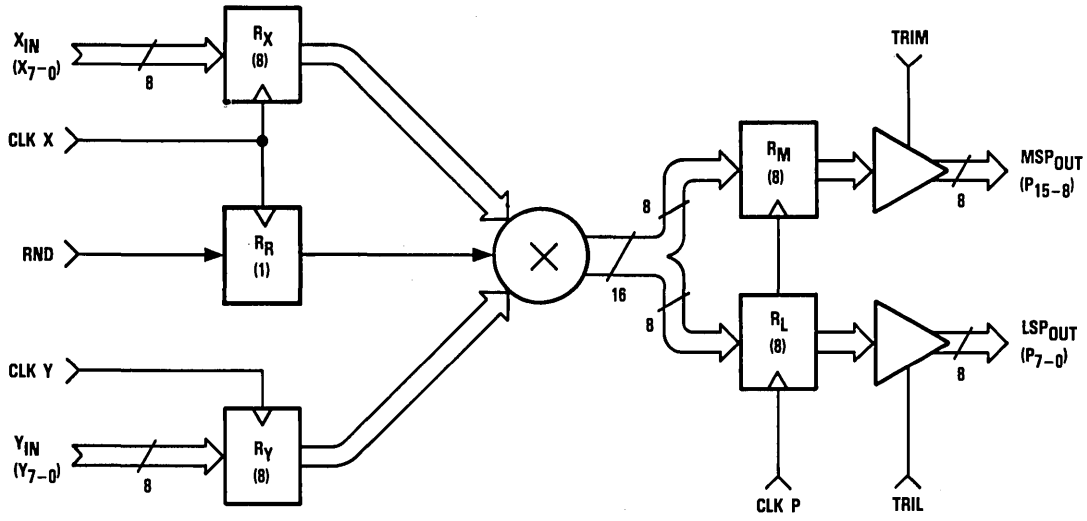
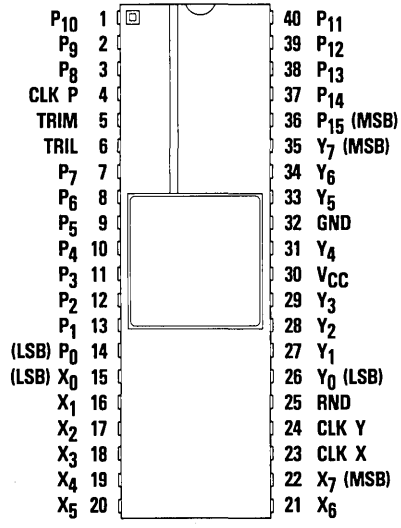
Functional Block Diagram



Pin Assignments



40 Lead DIP – J5 Package

Functional Description

General Information

The MPY08HU has three functional sections: input registers, an asynchronous multiplier array, and output registers. The input registers store the two 8-bit numbers which are to be multiplied and the instruction which controls the output rounding. This rounding control is used when a single-word output is desired. Each number is stored independently, simplifying multiplication by a constant. The asynchronous multiplier array is a network of AND gates and adders, designed to handle unsigned magnitude numbers. The output registers hold the product as two 8-bit words, the Most Significant Product (MSP) and the Least Significant Product (LSP). Three-state output drivers allow the MPY08HU to be used on a bus, or allow the outputs to be multiplexed over the same 8-bit output lines.

Power

The MPY08HU operates from a single +5 Volt supply.

Name	Function	Value	J5 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pin 30
GND	Ground	0.0V	Pin 32

Data Inputs

The MPY08HU has two data 8-bit unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs) are denoted X_7 and Y_7; the remaining bits are denoted X_0 through X_6 and Y_0 through Y_6 (with X_0 and Y_0 the Least Significant Bits). The input and output formats for fractional unsigned magnitude notation and integer unsigned magnitude notation are shown in Figures 1 and 2, respectively.

Name	Function	Value	J5 Package
X_7	X Data MSB	TTL	Pin 22
X_6		TTL	Pin 21
X_5		TTL	Pin 20
X_4		TTL	Pin 19
X_3		TTL	Pin 18
X_2		TTL	Pin 17
X_1		TTL	Pin 16
X_0	X Data LSB	TTL	Pin 15
Y_7	Y Data MSB	TTL	Pin 35
Y_6		TTL	Pin 34
Y_5		TTL	Pin 33
Y_4		TTL	Pin 31
Y_3		TTL	Pin 29
Y_2		TTL	Pin 28
Y_1		TTL	Pin 27
Y_0	Y Data LSB	TTL	Pin 26

Data Outputs

The MPY08HU has a 16-bit unsigned magnitude output which is the product of the two input data values. This output is divided into two 8-bit output words, the Most Significant Product (MSP) and Least Significant Product (LSP). The Most Significant Bit (MSB) of the MSP is Product bit P_{15}. Product bit P_0 is the Least Significant Bit (LSB). The input and output formats for fractional unsigned magnitude notation and integer unsigned magnitude notation are shown in Figures 1 and 2, respectively.

Name	Function	Value	J5 Package
P_{15}	Product MSB	TTL	Pin 36
P_{14}		TTL	Pin 37
P_{13}		TTL	Pin 38
P_{12}		TTL	Pin 39
P_{11}		TTL	Pin 40
P_{10}		TTL	Pin 1
P_9		TTL	Pin 2
P_8		TTL	Pin 3
P_7		TTL	Pin 7
P_6		TTL	Pin 8
P_5		TTL	Pin 9
P_4		TTL	Pin 10
P_3		TTL	Pin 11
P_2		TTL	Pin 12
P_1		TTL	Pin 13
P_0	Product LSB	TTL	Pin 14

Clocks

The MPY08HU has three clock lines, one for each of the input registers and one for the product register. Data present at the inputs of these registers are loaded into the registers at the rising edge of the appropriate clock.

Name	Function	Value	J5 Package
CLK X	Clock Input Data X	TTL	Pin 23
CLK Y	Clock Input Data Y	TTL	Pin 24
CLK P	Clock Product Register	TTL	Pin 4

Controls

The MPY08HU has three control lines:

TRIM, TRIL — Three-state enable lines for the MSP and the LSP. The output driver is in the high-impedance state when TRIM or TRIL is HIGH, and enabled when the appropriate control is LOW.

RND — The RND input is registered, and clocked in at the rising edge of CLK X. A one is added to the MSB of the LSP when RND is HIGH. The RND control is used when a rounded 8-bit product is desired.

Name	Function	Value	J5 Package
RND	Round Control Bit	TTL	Pin 25
TRIM	MSP Three-State Control	TTL	Pin 5
TRIL	LSP Three-State Control	TTL	Pin 6

Figure 1. Fractional Unsigned Magnitude Notation

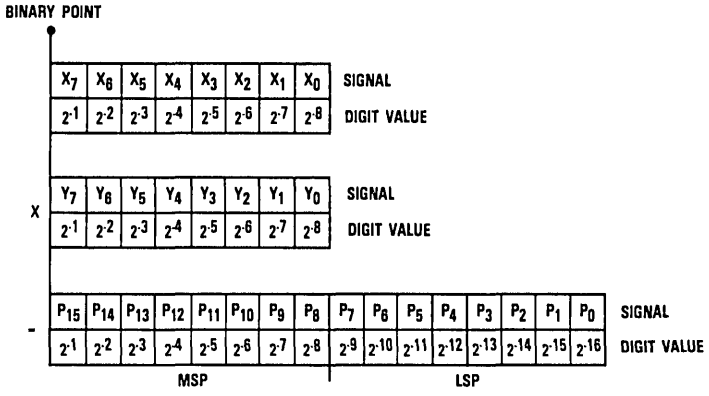


Figure 2. Integer Unsigned Magnitude Notation

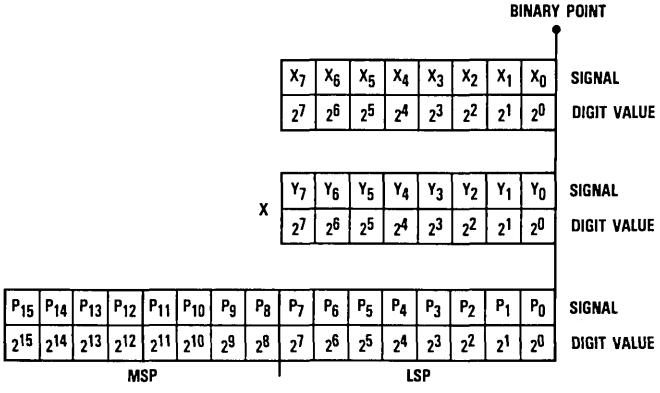


Figure 3. Timing Diagram

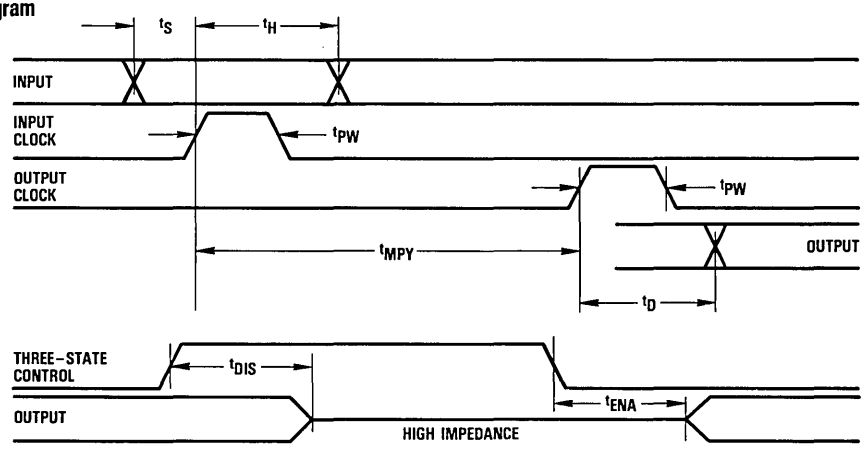


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Figure 4. Equivalent Input Circuit

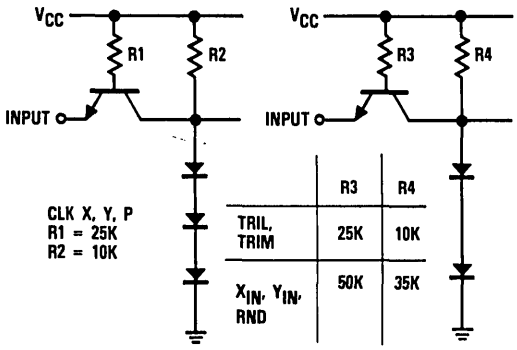


Figure 5. Equivalent Output Circuit

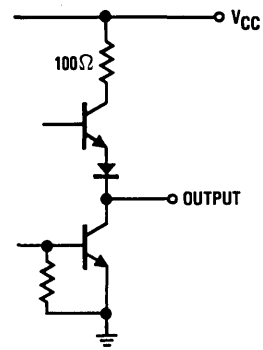


Figure 6. Test Load

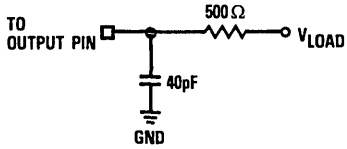
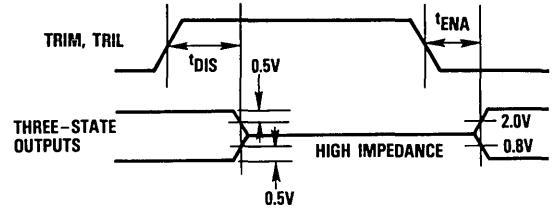


Figure 7. Transition Levels For Three-State Measurements



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−6.0 to +6.0mA
Output	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−1.0 to +6.0mA [3,4]
Short-circuit duration (single output in high state to ground)	1 sec.
Temperature	
Operating, case	−55 to +125°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.50	5.0	5.5	V
t_{PW}	Clock Pulse Width	25			30			ns
t_S	Input Setup Time	25			30			ns
t_H	Input Hold Time	0			3			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		+125	°C

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Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = MAX, Static[1]		375		450	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V					
		X_{IN}, Y_{IN}, RND		-0.4		-0.4	mA
		CLK X, CLK Y, TRIM, TRIL		-1.0		-1.0	mA
		CLK P		-2.0		-2.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V					
		CLK P		150		200	μA
		(All others)		75		100	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{CC} = MAX, V_I = 0.4V		-40		-40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{CC} = MAX, V_I = 2.4V		40		40	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = MAX, one pin to ground, one second duration max, output HIGH		-50		-50	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		10		10	pF

Note:

1. Static: All inputs and outputs LOW.

Switching characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MPY}	Multiply Time	V_{CC} = MIN MPY08HU-1		65			ns
		V_{CC} = MIN MPY08HU		90		115	ns
t_D	Output Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V		40		45	ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 1.8V		40		45	ns
t_{DIS}	Three-State Output Disable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1}[2]		40		45	ns

Notes:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in figure 7.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

Application Notes

Multiplication By A Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and that the register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the MPY08HU does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64.$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 and 2.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
MPY08HUJ5C	STD-T_A = 0°C to 70°C	Commercial	40 Lead DIP	08HUJ5C
MPY08HUJ5C1	STD-T_A = 0°C to 70°C	Commercial	40 Lead DIP	08HUJ5C1
MPY08HUJ5G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	40 Lead DIP	08HUJ5G
MPY08HUJ5G1	STD-T_A = 0°C to 70°C	Commercial With Burn-In	40 Lead DIP	08HUJ5G1
MPY08HUJ5F[1]	EXT-T_C = 55°C to 125°C	Commercial	40 Lead DIP	08HUJ5F
MPY08HUJ5A[1]	EXT-T_C = 55°C to 125°C	High Reliability[2]	40 Lead DIP	08HUJ5A

Notes:

1. Contact factory for availability.
2. Per TRW document 70Z01757.

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MPY012H

Multiplier
12 X 12 bit, 115ns

The MPY012H is a high-speed 12 x 12 bit parallel multiplier which operates at a 115 nanosecond cycle time (8.7MHz multiplication rate). The multiplicand and the multiplier may be independently specified as two's complement or unsigned magnitude, yielding a full-precision 24-bit product.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The MPY012H is built with TRW's 2-micron bipolar process.

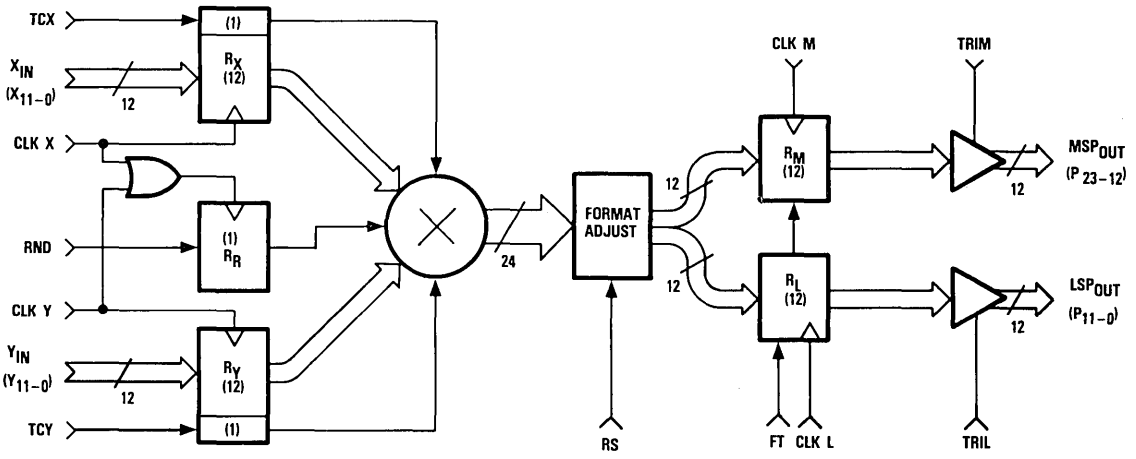
Features

- 115ns Multiply Time (Worst Case)
- 12 x 12 Bit Parallel Multiplication With 24-Bit Product Output
- Three-State Outputs
- Fully TTL Compatible
- Two's Complement, Unsigned Magnitude, And Mixed Mode Multiplication
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In 64 Lead Ceramic DIP, 68 Contact Chip Carrier, 68 Leaded Chip Carrier, Or 64 Leaded Flatpack

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



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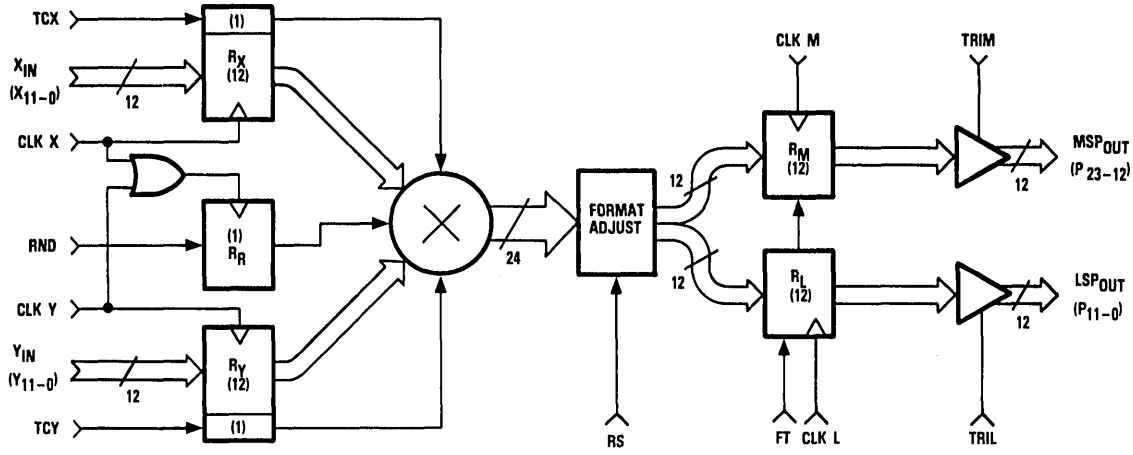
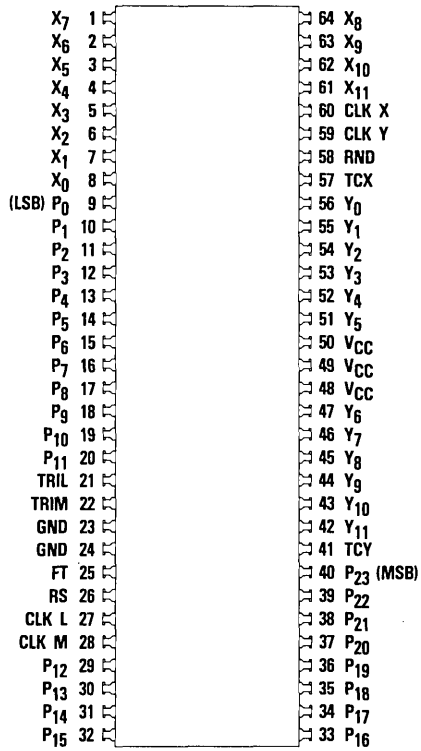
Functional Block Digram

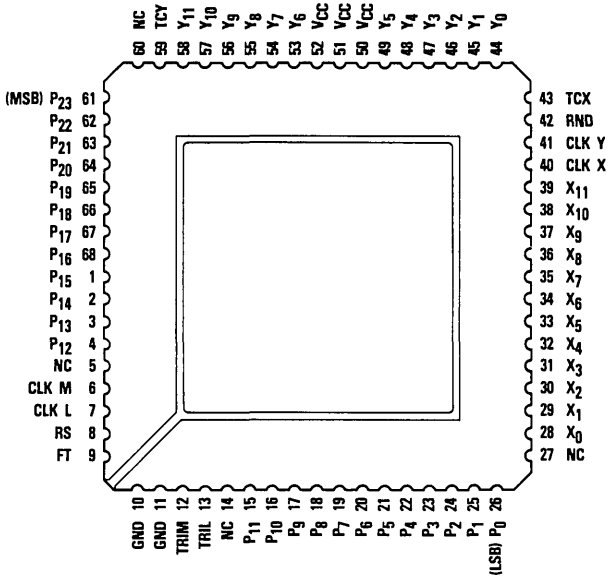


Pin Assignments



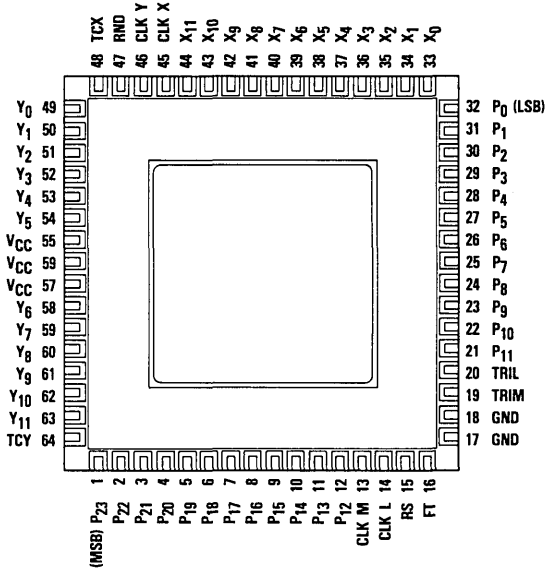
64 Lead DIP - J1 Package

Pin Assignments



68 Contact Or Leaded Chip Carrier – C1, L1 Package

Pin Assignments



64 Leaded Flatpack – F1 Package

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Functional Description

General Information

The MPY012H has three functional sections: input registers, an asynchronous multiplier array, and output registers. The input registers store the two 12-bit numbers which are to be multiplied and the instruction which controls the output rounding. This rounding control is used when a single-word output is desired. Each input operand is stored independently, simplifying multiplication by a constant. The asynchronous multiplier array is a network of AND gates and adders, designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 12-bit words, the Most Significant Product (MSP) and the Least Significant Product (LSP). Three-state output drivers allow the MPY012H to be used on a bus, or allow the least and most significant outputs to be multiplexed over the same 12-bit output lines.

Power

The MPY012H operates from a single +5 Volt supply. All power and ground lines must be connected.

Name	Function	Value	J1 Package	C1, L1 Package	F1 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pins 48, 49, 50	Pins 50, 51, 52	Pins 55, 56, 57
GND	Ground	0.0V	Pins 23, 24	Pins 10, 11	Pins 17, 18

Control

The MPY012H has seven control lines:

FT — A control line which makes the output register transparent if it is HIGH.

TRIM, TRIL — Three-state enable lines for the MSP and the LSP. The output driver is in the high-impedance state when TRIM or TRIL is HIGH, and enabled when the appropriate control is LOW.

RS — RS is an output format control. A HIGH level on RS deletes the sign bit from the LSP and shifts the MSP down one bit. This is mandatory for unsigned magnitude, mixed mode, and two's complement integer operations.

RND — When RND is HIGH, a one is added to the MSB of the LSP. Note that this bit depends on the state of the RS control. If RS is LOW when RND is HIGH, a one will be added to the 2^{-12} bit (P_{10}). If RS is HIGH when RND is HIGH, a one will be added to the 2^{-11} bit (P_{11}). In either case, the LSP output will reflect this addition when RND is HIGH. Note also that rounding always occurs in the positive direction; in some systems this may introduce a systematic bias.

TCX, TCY — Control how the device interprets data on the X and Y inputs. A HIGH on TCX or TCY forces the MPY012H to consider the appropriate input as a two's complement number, while a LOW forces the MPY012H to consider the appropriate input as a magnitude only number.

FT, RS, TRIM and TRIL are not registered. The TCX input is registered, and clocked in at the rising edge of the X clock signal, CLK X. The TCY input is also registered, and clocked in at the rising edge of the Y clock signal, CLK Y. The RND input is registered, and clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with loading the RND control signal can be avoided by the use of normally LOW clocks.

Control (Cont.)

Name	Function	Value	J1 Package	C1, L1 Package	F1 Package
RND	Round Control Bit	TTL	Pin 58	Pin 42	Pin 47
TCX	X Input, Two's Complement	TTL	Pin 57	Pin 43	Pin 48
TCY	Y Input, Two's Complement	TTL	Pin 41	Pin 59	Pin 64
FT	Output Register Feedthrough	TTL	Pin 25	Pin 9	Pin 16
RS	Output Right Shift	TTL	Pin 26	Pin 8	Pin 15
TRIM	MSP Three-State Control	TTL	Pin 22	Pin 12	Pin 19
TRIL	LSP Three-State Control	TTL	Pin 21	Pin 13	Pin 20

Data Inputs

The MPY012H has two 12-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_{11} and Y_{11}, carry the sign information for the two's complement notation. The remaining bits are denoted X_0 through X_{10} and Y_0 through Y_{10} (with X_0 and Y_0 the Least Significant Bits). The input and output formats for fractional two's complement, fractional unsigned magnitude, fractional mixed mode, integer two's complement, integer unsigned magnitude, and integer mixed mode notation are shown in Figures 1 through 6.

Name	Function	Value	J1 Package	C1, L1 Package	F1 Package
X_{11}	X Data MSB	TTL	Pin 61	Pin 39	Pin 44
X_{10}		TTL	Pin 62	Pin 38	Pin 43
X_9		TTL	Pin 63	Pin 37	Pin 42
X_8		TTL	Pin 64	Pin 36	Pin 41
X_7		TTL	Pin 1	Pin 35	Pin 40
X_6		TTL	Pin 2	Pin 34	Pin 39
X_5		TTL	Pin 3	Pin 33	Pin 38
X_4		TTL	Pin 4	Pin 32	Pin 37
X_3		TTL	Pin 5	Pin 31	Pin 36
X_2		TTL	Pin 6	Pin 30	Pin 35
X_1		TTL	Pin 7	Pin 29	Pin 34
X_0	X Data LSB	TTL	Pin 8	Pin 28	Pin 33
Y_{11}	Y Data MSB	TTL	Pin 42	Pin 58	Pin 63
Y_{10}		TTL	Pin 43	Pin 57	Pin 62
Y_9		TTL	Pin 44	Pin 56	Pin 61
Y_8		TTL	Pin 45	Pin 55	Pin 60
Y_7		TTL	Pin 46	Pin 54	Pin 59
Y_6		TTL	Pin 47	Pin 53	Pin 58
Y_5		TTL	Pin 51	Pin 49	Pin 54
Y_4		TTL	Pin 52	Pin 48	Pin 53
Y_3		TTL	Pin 53	Pin 47	Pin 52
Y_2		TTL	Pin 54	Pin 46	Pin 51
Y_1		TTL	Pin 55	Pin 45	Pin 50
Y_0	Y Data LSB	TTL	Pin 56	Pin 44	Pin 49

Data Outputs

The MPY012H has a 24-bit two's complement or unsigned magnitude output which is the product of the two input data values. This output is divided into two 12-bit output words, the Most Significant Product (MSP) and Least Significant Product (LSP). The Most Significant Bit (MSB) of both the MSP and the LSP is the sign bit if fractional two's complement notation is used (TCX=TCY=1, RS=0). The input and output formats for fractional two's complement, fractional unsigned magnitude, fractional mixed mode, integer two's complement, integer unsigned magnitude, and integer mixed mode notation are shown in Figures 1 through 6. For the MSP and LSP to be read, the respective TRIM and TRIL controls must be LOW. RS is an output format control. A logical "1" on RS deletes the sign bit from the LSP and shifts the MSP down one bit. This is mandatory for unsigned magnitude, mixed mode, or integer two's complement operation.

Name	Function	Value	J1 Package	C1, L1 Package	F1 Package
P_{23}	Product MSB	TTL	Pin 40	Pin 61	Pin 1
P_{22}		TTL	Pin 39	Pin 62	Pin 2
P_{21}		TTL	Pin 38	Pin 63	Pin 3
P_{20}		TTL	Pin 37	Pin 64	Pin 4
P_{19}		TTL	Pin 36	Pin 65	Pin 5
P_{18}		TTL	Pin 35	Pin 66	Pin 6
P_{17}		TTL	Pin 34	Pin 67	Pin 7
P_{16}		TTL	Pin 33	Pin 68	Pin 8
P_{15}		TTL	Pin 32	Pin 1	Pin 9
P_{14}		TTL	Pin 31	Pin 2	Pin 10
P_{13}		TTL	Pin 30	Pin 3	Pin 11
P_{12}		TTL	Pin 29	Pin 4	Pin 12
P_{11}		TTL	Pin 20	Pin 15	Pin 21
P_{10}		TTL	Pin 19	Pin 16	Pin 22
P_9		TTL	Pin 18	Pin 17	Pin 23
P_8		TTL	Pin 17	Pin 18	Pin 24
P_7		TTL	Pin 16	Pin 19	Pin 25
P_6		TTL	Pin 15	Pin 20	Pin 26
P_5		TTL	Pin 14	Pin 21	Pin 27
P_4		TTL	Pin 13	Pin 22	Pin 28
P_3		TTL	Pin 12	Pin 23	Pin 29
P_2		TTL	Pin 11	Pin 24	Pin 30
P_1		TTL	Pin 10	Pin 25	Pin 31
P_0	Product LSB	TTL	Pin 9	Pin 26	Pin 32

Clocks

The MPY012H has four clock lines, one for each of the input registers and one for each product register. Data and two's complement instructions present at the inputs of these registers are loaded into the registers at the rising edge of the appropriate clock. The RND input is registered, and clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with loading this control signal can be avoided by the use of normally LOW clocks.

Name	Function	Value	J1 Package	C1, L1 Package	F1 Package
CLK X	Clock Input Data X	TTL	Pin 60	Pin 40	Pin 45
CLK Y	Clock Input Data Y	TTL	Pin 59	Pin 41	Pin 46
CLK L	Clock LSP Register	TTL	Pin 27	Pin 7	Pin 14
CLK M	Clock MSP Register	TTL	Pin 28	Pin 6	Pin 13

No Connects

The contact and leaded chip carrier versions of the MPY012H have four pins which are not connected internally. These should be left unconnected.

Name	Function	Value	J1 Package	C1, L1 Package	F1 Package
NC	No Connection	Open	None	Pins 5, 14, 27, 60	None

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Figure 1. Fractional Two's Complement Notation

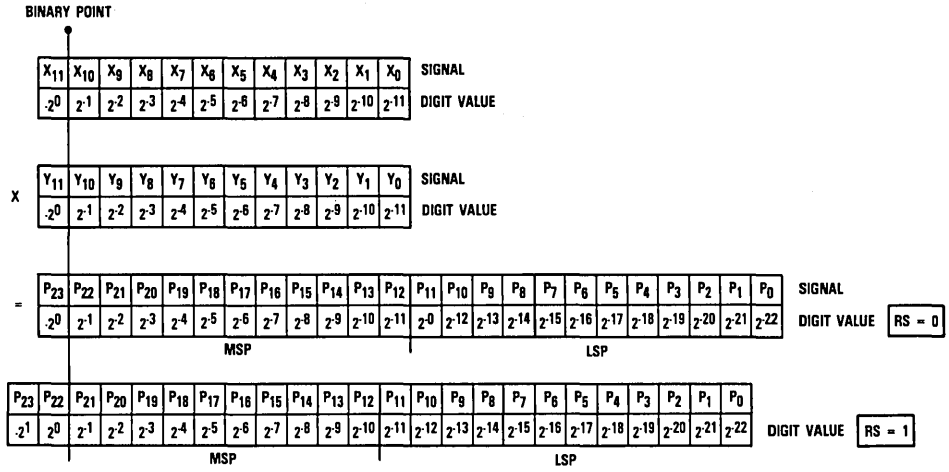

Figure 2. Fractional Unsigned Magnitude Notation

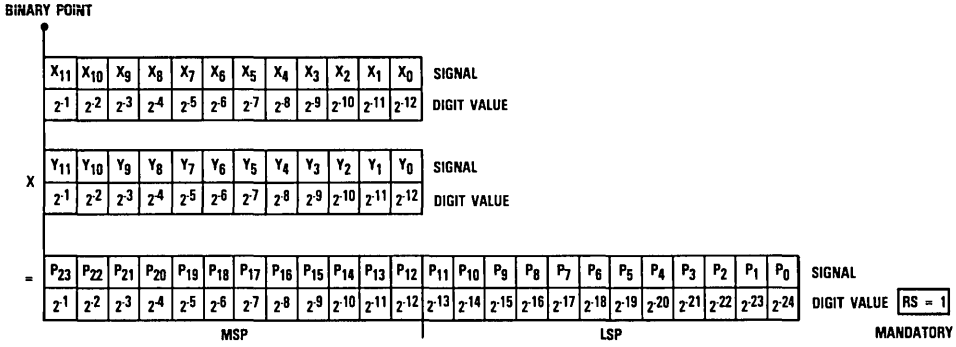

Figure 3. Fractional Mixed Mode Notation

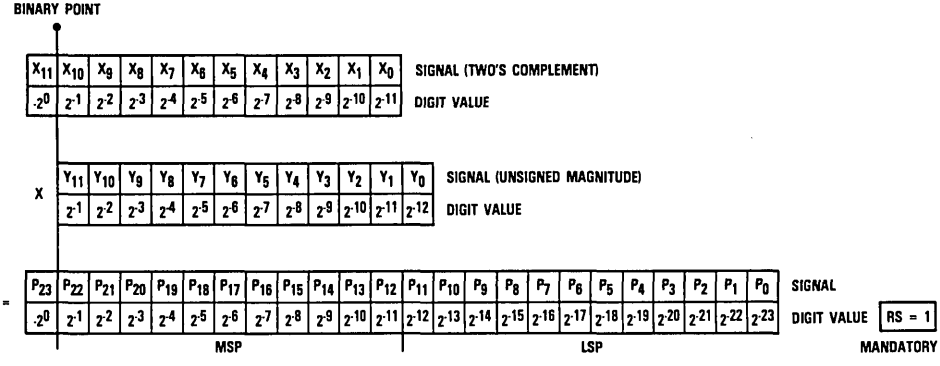

Figure 4. Integer Two's Complement Notation

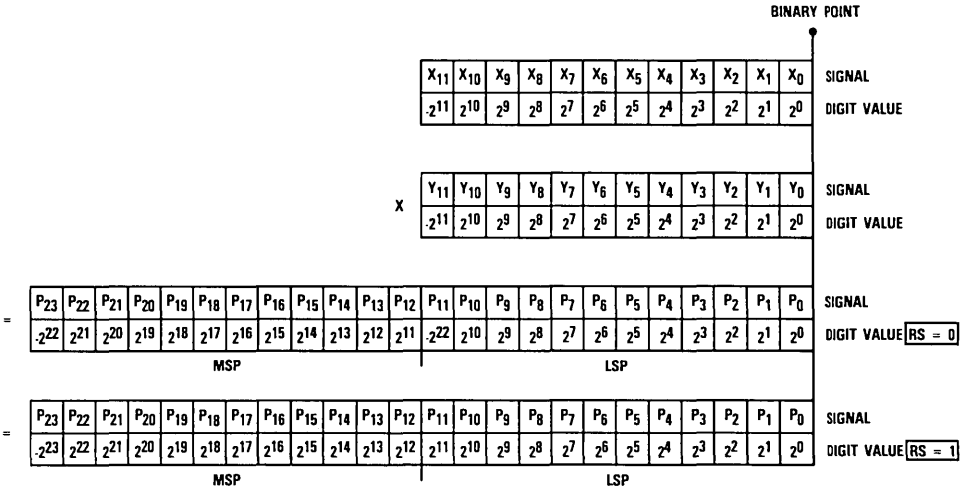

Figure 5. Integer Unsigned Magnitude Notation

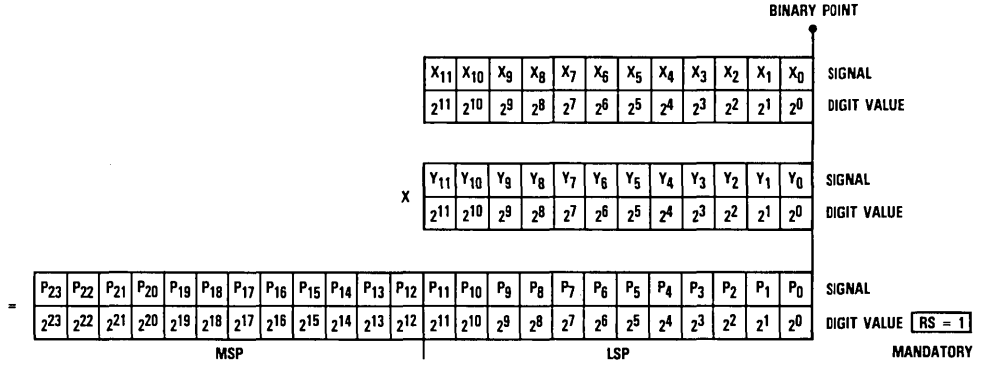

Figure 6. Integer Mixed Mode Notation

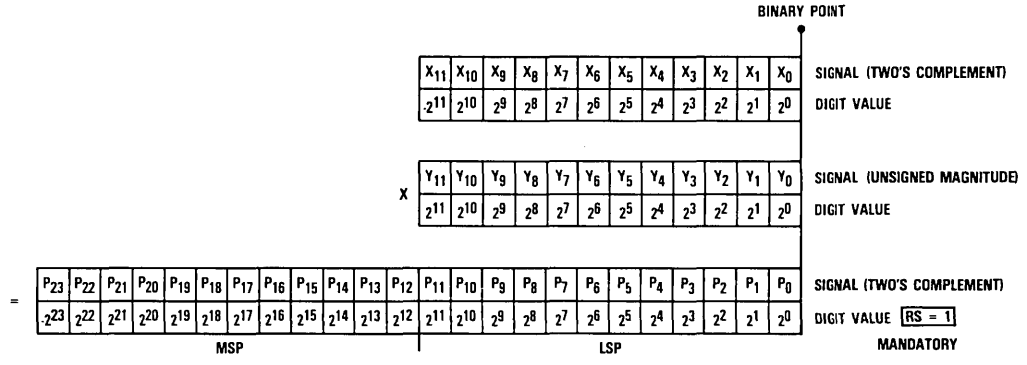

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Figure 7. Timing Diagram

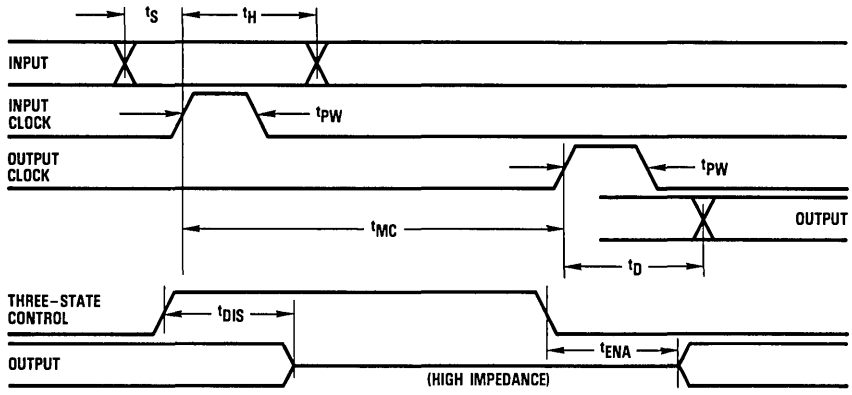


Figure 8. Timing Diagram, Unclocked Mode

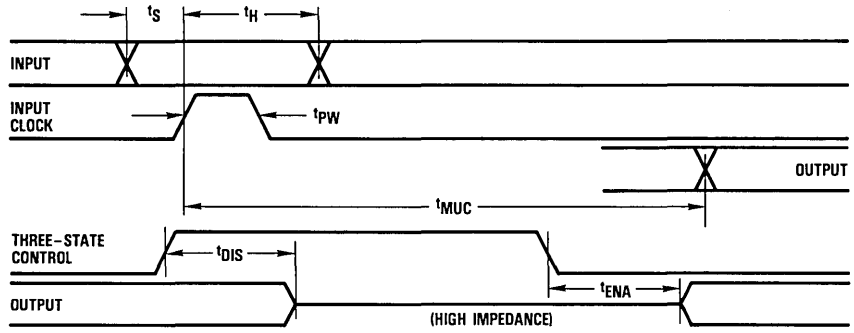
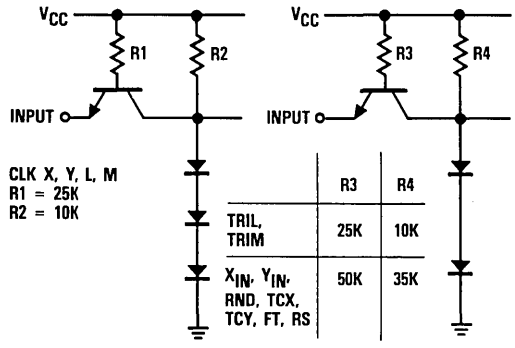


Figure 9. Equivalent Input Circuit



	R3	R4
TRIL, TRIM	25K	10K
X_{IN}, Y_{IN}, RND, TCX, TCY, FT, RS	50K	35K

Figure 10. Equivalent Output Circuit

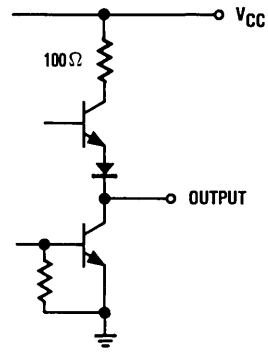


Figure 11. Test Load

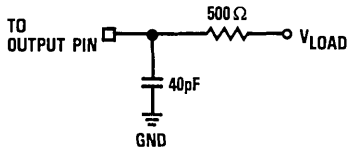
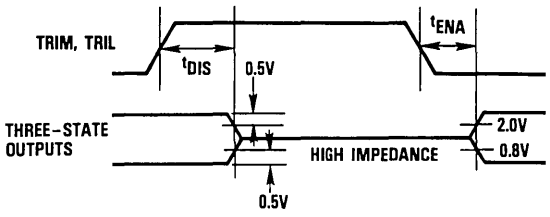


Figure 12. Three-State Delay Test Load



Application Notes

Mixed Mode Multiplication

There are several applications in which mixed mode multiplication may be advantageous. For example, inputs to a digital signal processor are often generated as unsigned magnitude numbers (e.g., data from an analog-to-digital converter). These numbers are effectively all positive values. In contrast, filter coefficients must often be negative. As a result, either the unsigned magnitude data must be converted to two's complement notation (which requires an additional bit), or the multiplier must be capable of mixed mode operation. The MPY012H provides this capability by independently specifying the mode of the multiplicand (X) and the multiplier (Y) on the TCX and TCY pins. No additional circuitry is required and the resulting product is in two's complement notation.

Multiplication By A Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and that the selected register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection Of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the MPY012H does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64.$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design.

Because common design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 6.

Register Shift (RS) Control

In two's complement notation, the acceptable range of values for a given word size is not the same for positive and negative numbers. The largest negative number is one LSB larger than the largest positive number. This is true for either fractional or integer notation. A problem can arise when the largest representable negative number is multiplied by itself. This should give a positive number of the same magnitude. However, the largest representable positive number is one LSB less than this value. As a result, this product cannot be correctly represented without using one additional output bit.

The MPY012H has a Register Shift (RS) control that permits shifting of the result to provide a correct answer for every two's complement multiplication. When RS is active, the value of all bits in the MSP is doubled (i.e., shifted left one position), which provides the capability to represent the largest possible product. The MSB of the Least Significant Product is changed from a duplicate of the sign bit to the necessary bit to fill in the output word. The effects of this control are illustrated in Figures 1 and 4. Note that for unsigned magnitude operation, the RS control must be HIGH.

Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−6.0 to +6.0mA
Output	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−1.0 to +6.0mA [3,4]
Short-circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, case	−55 to +125°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to 150°C

Notes:

1. *Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions.* Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Extended Min	Extended Nom	Extended Max	Units
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PW}	Clock Pulse Width	25			30			ns
t_S	Input Register Setup Time	25			30			ns
t_H	Input Register Hold Time	0			3			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
I_{CC}	Supply Current	V_{CC} = MAX, Static[1]		700		750	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V					
		X_{IN}, Y_{IN}, RND, FT		−0.4		−0.4	mA
		$\overline{TCX}$, TCY, RS		−0.8		−0.8	mA
		CLK L, M, X, and Y; TRIM, TRIL		−1.0		−1.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V					
		X_{IN}, Y_{IN}, RND, FT		75		100	μA
		$\overline{TCX}$, TCY, RS		75		100	μA
		CLK L, M, X, and Y; TRIM, TRIL		75		100	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{CC} = MAX, V_I = 0.4V		−40		−40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{CC} = MAX, V_I = 2.4V		40		40	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = MAX, one pin to ground, one second duration max, output HIGH		−50		−50	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:

1. All inputs and outputs LOW.

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Switching characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MC}	Multiply Time, Clocked	V_{CC} = MIN		115		140	ns
t_{MUC}	Multiply Time, Unclocked	V_{CC} = MIN		155		185	ns
t_D	Output Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V		40		45	ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 1.8V		40		45	ns
t_{DIS}	Three-State Output Disable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1}[2]		40		45	ns

Notes:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in Figure 12.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
MPY012HJ1C	STD-T_A = 0°C to 70°C	Commercial	64 Lead DIP	012HJ1C
MPY012HJ1G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	64 Lead DIP	012HJ1G
MPY012HJ1F	EXT-T_C = -55°C to 125°C	Commercial	64 Lead DIP	012HJ1F
MPY012HJ1A	EXT-T_C = -55°C to 125°C	High Reliability[2]	64 Lead DIP	012HJ1A
MPY012HC1F[1]	EXT-T_C = -55°C to 125°C	Commercial	68 Contact Chip Carrier	012HC1F
MPY012HC1A	EXT-T_C = -55°C to 125°C	High Reliability[2]	68 Contact Chip Carrier	012HC1A
MPY012HL1F[1]	EXT-T_C = -55°C to 125°C	Commercial	68 Leaded Chip Carrier	012HL1F
MPY012HL1A[1]	EXT-T_C = -55°C to 125°C	High Reliability[2]	68 Leaded Chip Carrier	012HL1A
MPY012HF1F[1]	EXT-T_C = -55°C to 125°C	Commercial	64 Lead Flatpack	012HF1F
MPY012HF1A	EXT-T_C = -55°C to 125°C	High Reliability[2]	64 Lead Flatpack	012HF1A

Notes:

1. Contact factory for availability.
2. Per TRW document 70Z01757.

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MPY112K
Preliminary Information

Multiplier
12 x 12 bit, 50ns

The MPY112K is a video-speed 12 x 12 bit parallel multiplier which operates at a 50 nanosecond cycle time (20MHz multiplication rate). The multiplicand and the multiplier may be specified together as two's complement or unsigned magnitude, yielding a 16-bit result. Mixed mode operation is not available on this device.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The most significant 16 bits of the product are available at the output register. The output is a single three-state port.

Built with TRW's OMICRON-B™ 1-micron bipolar process, the MPY112K is similar to the industry standard MPY012H but operates with more than twice the speed at about three-quarters of the power dissipation. The MPY112K is the industry's first true video-speed 12-bit multiplier.

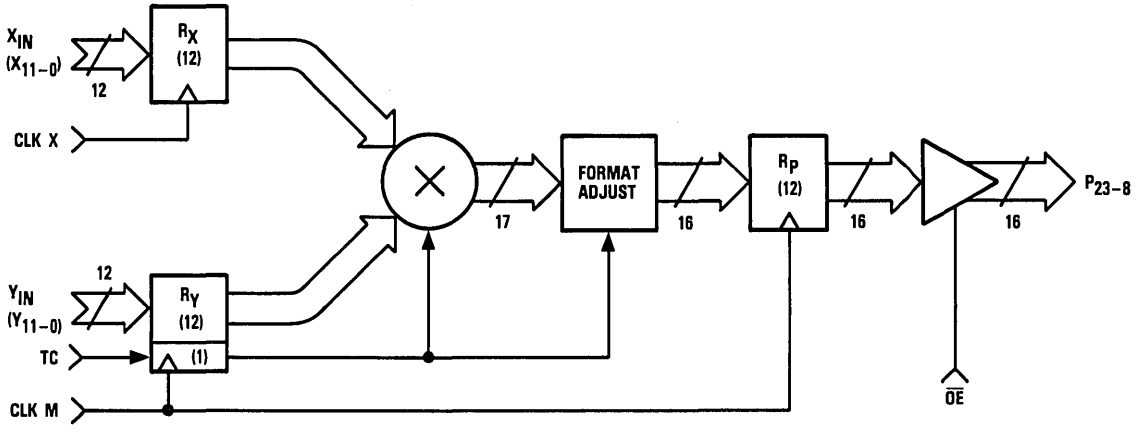
Features

- 50ns Multiply Time (Worst Case)
- 12 x 12 Bit Parallel Multiplication With 16-Bit Product Output
- Fully TTL Compatible
- Three-State Outputs
- Two's Complement Or Unsigned Magnitude Multiplication
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In 48 Lead Ceramic DIP

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



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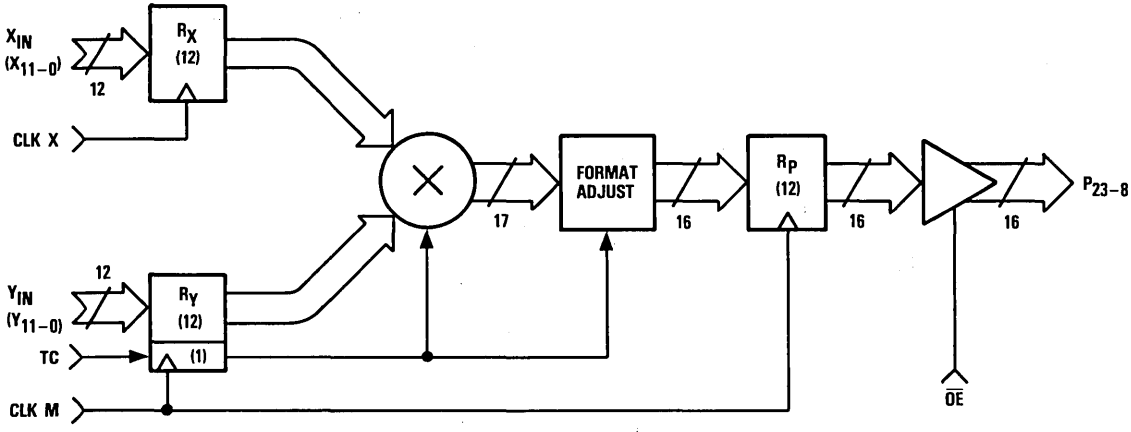
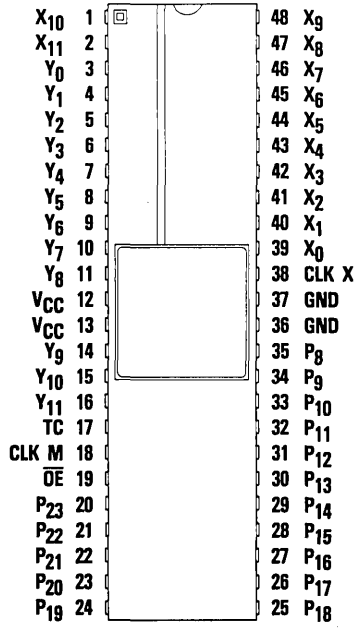
Functional Block Diagram



Pin Assignments



48 Lead DIP – J4 Package

Functional Description

General Information

The MPY112K has three functional sections: input registers, an asynchronous multiplier array, and output registers. The input registers store the two 12-bit numbers which are to be multiplied and the instruction which controls whether the inputs are to be considered as two's complement or unsigned magnitude numbers. Each input operand is stored independently, simplifying multiplication by a constant; however, since the product and the Y input share a common clock, any constant should be stored in the X register. The asynchronous multiplier array is a network of AND gates and adders which have been designed to handle two's complement or unsigned magnitude numbers. The output register holds the most significant 16 bits of the product. Three-state output drivers allow the MPY112K to be used on a bus.

Power

The MPY112K operates from a single +5 Volt supply. Note that the maximum voltage for proper operation over the extended temperature range is 5.25 Volts. All power and ground lines must be connected.

Name	Function	Value	J4 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pins 12, 13
GND	Ground	0.0V	Pins 36, 37

Data Inputs

The MPY112K has two 12-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_{11} and Y_{11}, carry the sign information for the two's complement notation. The rest of the bits are denoted X_0 through X_{10} and Y_0 through Y_{10} (with X_0 and Y_0 the Least Significant Bits). The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

Name	Function	Value	J4 Package
X_{11}	X Data MSB	TTL	Pin 2
X_{10}		TTL	Pin 1
X_9		TTL	Pin 48
X_8		TTL	Pin 47
X_7		TTL	Pin 46
X_6		TTL	Pin 45
X_5		TTL	Pin 44
X_4		TTL	Pin 43
X_3		TTL	Pin 42
X_2		TTL	Pin 41
X_1		TTL	Pin 40
X_0	X Data LSB	TTL	Pin 39

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Data Inputs (Cont.)

Name	Function	Value	J4 Package
Y_{11}	Y Data MSB	TTL	Pin 16
Y_{10}		TTL	Pin 15
Y_9		TTL	Pin 14
Y_8		TTL	Pin 11
Y_7		TTL	Pin 10
Y_6		TTL	Pin 9
Y_5		TTL	Pin 8
Y_4		TTL	Pin 7
Y_3		TTL	Pin 6
Y_2		TTL	Pin 5
Y_1		TTL	Pin 4
Y_0	Y Data LSB	TTL	Pin 3

Data Outputs

The MPY112K has a 16-bit two's complement or unsigned magnitude output which is the product of the two input data values. This output is the most significant 16 bits of the complete product. The output is truncated to this length, not rounded. The Most Significant Bit (MSB) of the product is the sign bit if two's complement notation is used (TC=1). The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively. The output driver is in the high-impedance state when $\overline{OE}$ is HIGH, and enabled when $\overline{OE}$ is LOW.

Name	Function	Value	J4 Package
P_{23}	Product MSB	TTL	Pin 20
P_{22}		TTL	Pin 21
P_{21}		TTL	Pin 22
P_{20}		TTL	Pin 23
P_{19}		TTL	Pin 24
P_{18}		TTL	Pin 25
P_{17}		TTL	Pin 26
P_{16}		TTL	Pin 27
P_{15}		TTL	Pin 28
P_{14}		TTL	Pin 29
P_{13}		TTL	Pin 30
P_{12}		TTL	Pin 31
P_{11}		TTL	Pin 32
P_{10}		TTL	Pin 33
P_9		TTL	Pin 34
P_8		TTL	Pin 35

Clocks

The MPY112K has two clock lines, one for the X input register and one for both the Y input register and the product register. Data present at the X input are loaded into the registers at the rising edge of CLK X. Data present at the Y input, the two's complement instruction, and the product present at the output of the asynchronous multiplier array are loaded into the appropriate registers at the rising edge of CLK M.

Name	Function	Value	J4 Package
CLK X	Clock Input Data X	TTL	Pin 38
CLK M	Master Clock	TTL	Pin 18

Controls

The MPY112K has two control lines. $\overline{OE}$ is a three-state enable line for the output. The output drivers are in the high-impedance state when $\overline{OE}$ is HIGH, and enabled when $\overline{OE}$ is LOW. The device will interpret data as two's complement when TC is HIGH, and as unsigned magnitude when TC is LOW. $\overline{OE}$ is not registered. TC is registered and clocked in at the rising edge of CLK M.

Name	Function	Value	J4 Package
TC	Two's Complement	TTL	Pin 17
$\overline{OE}$	Three-State Control	TTL	Pin 19

Figure 1. Fractional Two's Complement Notation

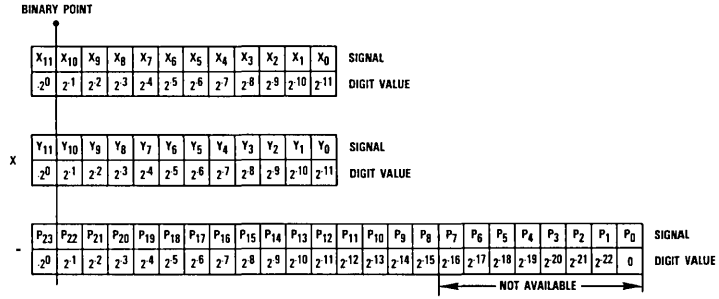


Figure 2. Fractional Unsigned Magnitude Notation

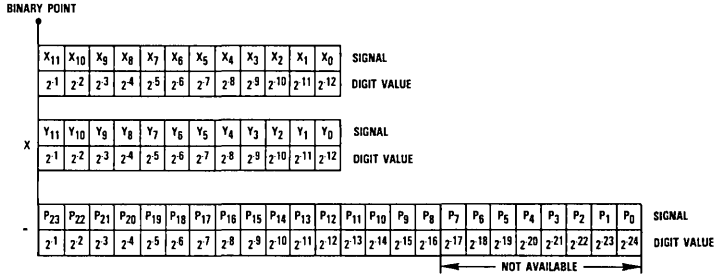


Figure 3. Integer Two's Complement Notation

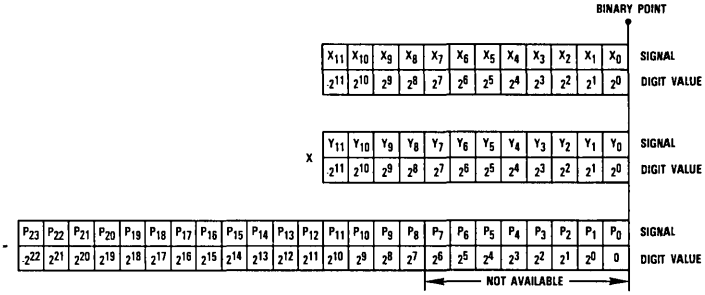


Figure 4. Integer Unsigned Magnitude Notation

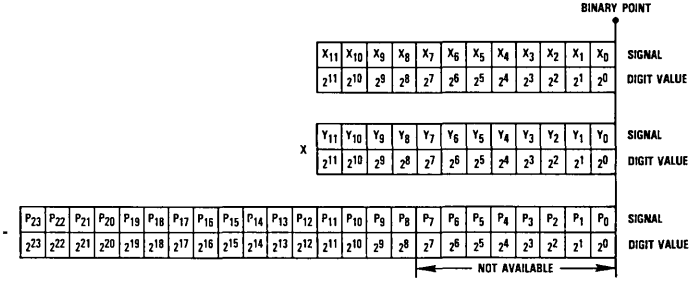


Figure 5. Timing Diagram

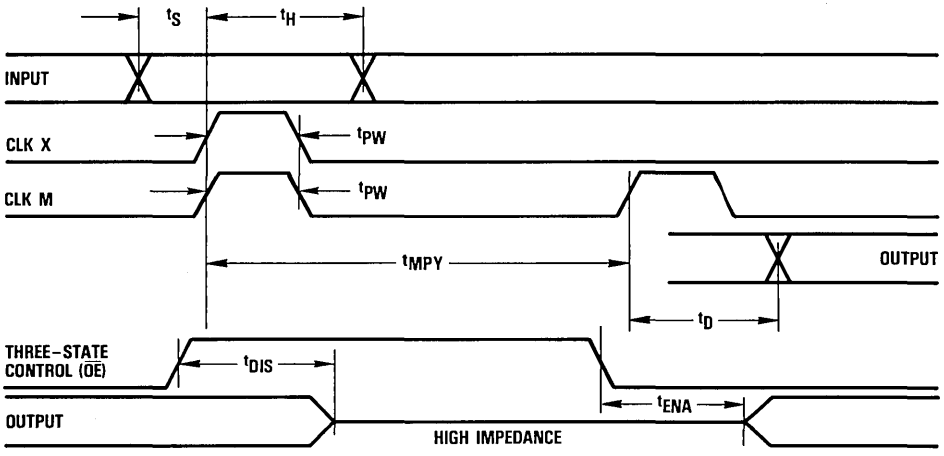


Figure 6. Equivalent Input Circuit

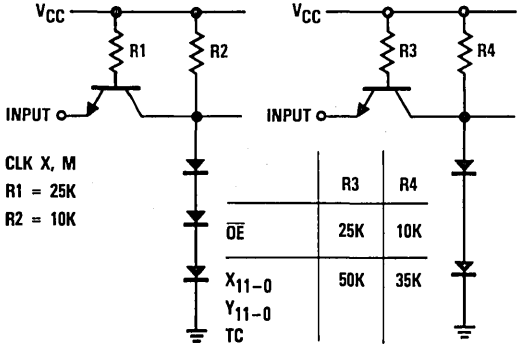


Figure 7. Equivalent Output Circuit

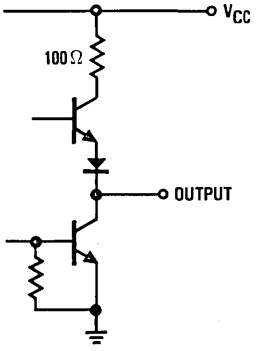


Figure 8. Test Load

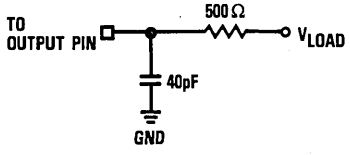
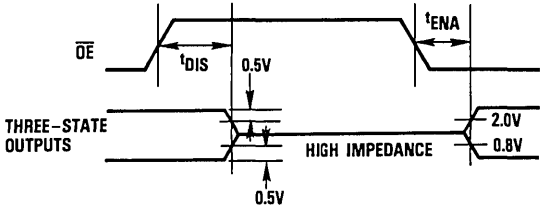


Figure 9. Transition Levels For Three-State Measurements



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage ..... −0.5 to +7.0V

Input

Applied voltage ..... −0.5 to +5.5V [2]

Forced current ..... −6.0 to +6.0mA

Output

Applied voltage ..... −0.5 to +5.5V [2]

Forced current ..... −1.0 to +6.0mA [3,4]

Short-circuit duration (single output in high state to ground) ..... 1 sec

Temperature

Operating, case ..... −55 to +125°C

junction ..... 175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to 150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.25	V
t_{PWL}	Clock Pulse Width, LOW	20			25			ns
t_{PWH}	Clock Pulse Width, HIGH	20			25			ns
t_S	Input Setup Time	25			30			ns
t_H	Input Hold Time	5			10			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			2.5	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
I_{CC}	Supply Current[1]	V_{CC} = MAX, Static		450		550	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V					
		Data Inputs, TC		-0.2		-0.3	mA
		CLK X, $\overline{OE}$		-0.6		-0.75	mA
		CLK M		-1.2		-1.5	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V					
		Data Inputs, TC		50		50	μA
		CLK X, $\overline{OE}$		50		50	μA
		CLK M		100		100	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MAX, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{CC} = MAX, V_I = 0.4V	-40	40	-40	40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{CC} = MAX, V_I = 2.4V	-40	40	-40	40	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = MAX, Output HIGH, one pin to ground, one second duration max		-50		-50	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:

1. Worst case, all inputs and outputs LOW.

Switching characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
t_{MPY}	Multiply Time	V_{CC} = MIN		50		55	ns
t_D	Output Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V		35		45	ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 1.8V		30		45	ns
t_{DIS}	Three-State Output Enable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.6V t_{DIS0}, 0.0V for t_{DIS1}[2]		30		45	ns

Notes:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in Figure 9.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

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Application Notes

Mixed-Mode Multiplication

There are several applications in which it may be advantageous to perform mixed-mode multiplication. Video data are often generated as unsigned magnitude numbers (e.g., data from an analog-to-digital converter.) These numbers are effectively all positive values. In contrast, filter coefficients must often be negative. As a result, either the video data must be converted to two's complement notation (which requires an additional bit), or the multiplier must be capable of mixed-mode operation. The MPY112K can only provide this capability by making the MSB of the unsigned magnitude number a zero, thus reducing its precision to eleven bits. No additional circuitry is required.

Multiplication By A Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and that the register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register. Due to the sharing of the CLK M pin by the Y input register and the output register, all constants should be kept in the X register.

Selection Of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the MPY112K does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 4.

Exceptional Case

The most negative number that can be represented in two's complement notation is greater in magnitude than the largest representable positive number by one LSB. This is only a problem when the full-scale negative number is squared. If fractional notation is used, this means that $(-1) \times (-1)$ with the MPY112K will yield the (incorrect) result (-1). In the full-precision series of multipliers the correct result can be obtained by the use of the RS control, which was not included on the MPY112K due to pin count limitations.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
MPY112KJ4C	STD-T_A = 0°C to 70°C	Commercial	48 Lead DIP	112KJ4C
MPY112KJ4G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	48 Lead DIP	112KJ4G
MPY112KJ4F[1]	EXT-T_C = -55°C to 125°C	Commercial	48 Lead DIP	112KJ4F
MPY112KJ4A[1]	EXT-T_C = -55°C to 125°C	High Reliability[2]	48 Lead DIP	112KJ4A

Notes:

1. Contact Factory for availability.
2. Per TRW document 70Z1757.

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Preliminary Information describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact TRW for current information.

MPY016H

Multiplier
16 X 16 bit, 145ns

The MPY016H is a high-speed 16 x 16 bit parallel multiplier which operates at a 145 nanosecond cycle time (6.9MHz multiplication rate). The multiplicand and the multiplier may be independently specified as two's complement or unsigned magnitude, yielding a full precision 32-bit product.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The Most Significant Product (MSP) has a dedicated output port. The Least Significant Product (LSP) shares a bidirectional port with the Y input. Three-state outputs are employed throughout. The MPY016H is built with TRW's state-of-the-art 2-micron bipolar process.

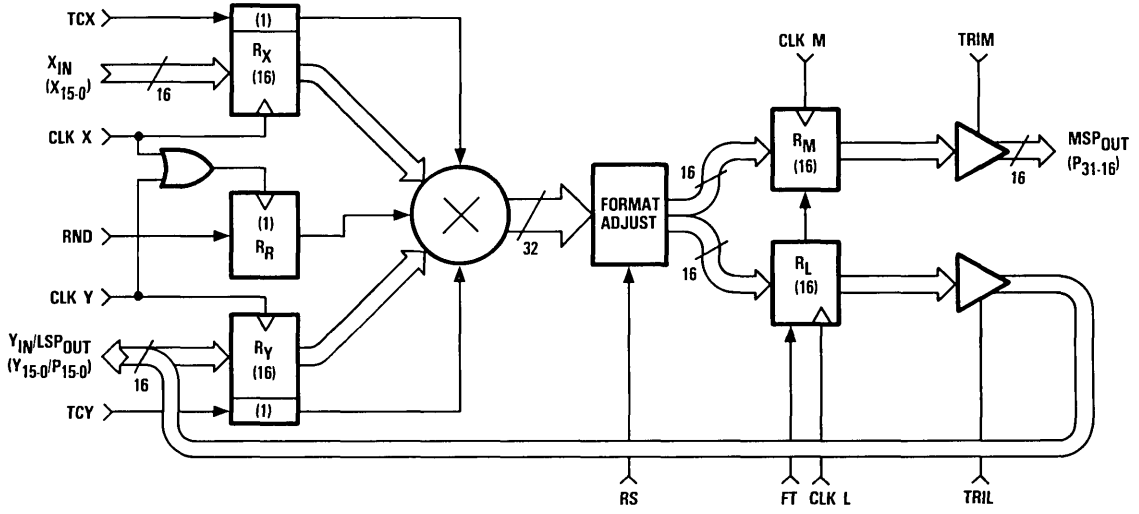
Features

- 145ns Multiply Time (Worst Case)
- 16 x 16 Bit Parallel Multiplication With 32-Bit Product Output
- Three-State Outputs
- Fully TTL Compatible
- Two's Complement, Unsigned Magnitude, and Mixed Mode Multiplication
- Proven, High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available in 64 Lead Ceramic DIP, 68 Contact Chip Carrier, 68 Leaded Chip Carrier, or 64 Leaded Flatpack

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



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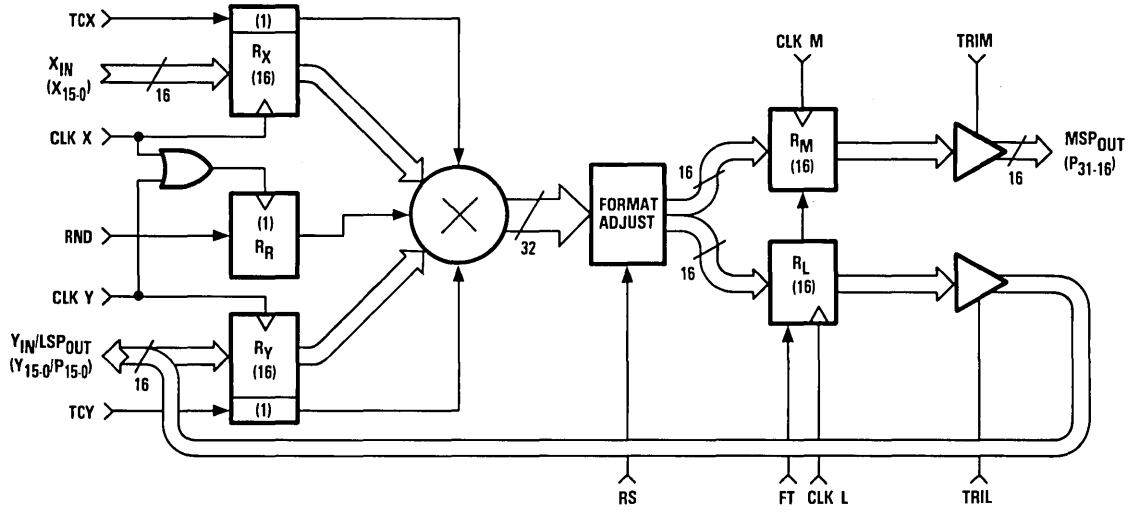
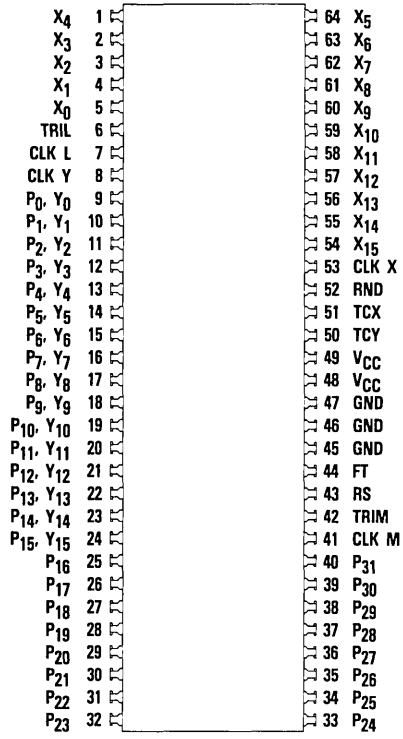
Functional Block Diagram

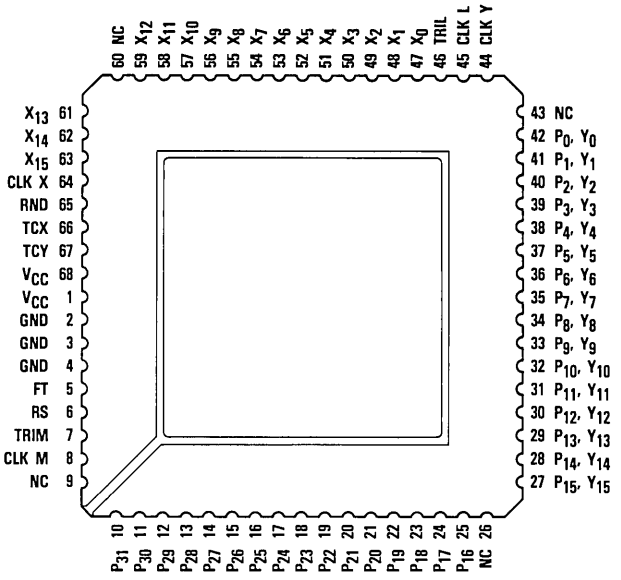


Pin Assignments



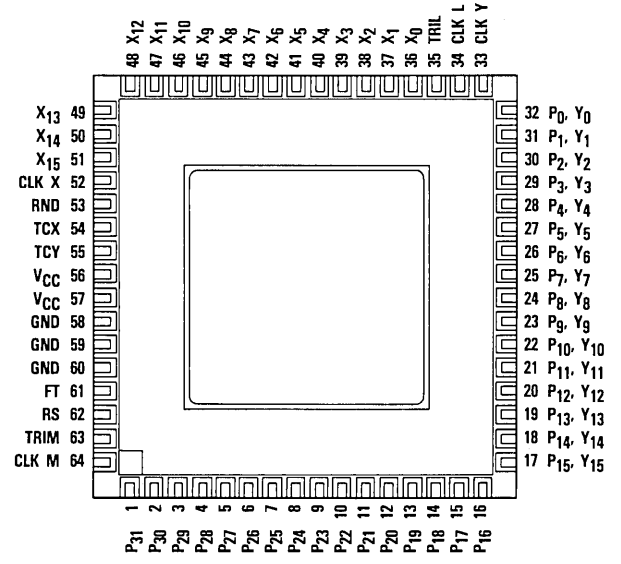
64 Lead DIP – J1 Package

Pin Assignments



68 Contact Or Leaded Chip Carrier – C1, L1 Package

Pin Assignments



64 Leaded Flatpack – F1 Package

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Functional Description

General Information

The MPY016H has three functional sections: input registers, an asynchronous multiplier array, and output registers. The input registers store the two 16-bit numbers which are to be multiplied and the instruction which controls the output rounding. This rounding control is used when a single-word output is desired. Each input operand is stored independently, simplifying multiplication by a constant. The asynchronous multiplier array is a network of AND gates and adders, designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 16-bit words, the Most Significant Product (MSP) and the Least Significant Product (LSP). Three-state output drivers allow the MPY016H to be used on a bus, or allow the least and most significant outputs to be multiplexed over the same 16-bit output lines. The Least Significant Product (LSP) is multiplexed with the Y input.

Power

The MPY016H operates from a single +5 Volt supply. All power and ground lines must be connected.

Name	Function	Value	J1 Package	C1, L1 Package	F1 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pins 48, 49	Pins 1, 68	Pins 56, 57
GND	Ground	0.0V	Pins 45, 46, 47	Pins 2, 3, 4	Pins 58, 59, 60

Control

The MPY016H has seven control lines:

FT — A control line which makes the output register transparent if it is HIGH.

TRIM, TRIL — Three-state enable lines for the MSP and the LSP. The output driver is in the high-impedance state when TRIM or TRIL is HIGH, and enabled when the respective control is LOW.

RS — RS is an output format control. A HIGH level on RS deletes the sign bit from the LSP and shifts the MSP down one bit. This is mandatory for unsigned magnitude, mixed mode, and two's complement integer operations.

RND — When RND is HIGH, a one is added to the MSB of the LSP. Note that this bit depends on the state of the RS control. If RS is LOW when RND is HIGH, a one will be added to the 2^{-16} bit (P_{14}). If RS is HIGH when RND is HIGH, a one will be added to the 2^{-15} bit (P_{15}). In either case, the LSP output will reflect this addition when RND is HIGH. Note also that rounding always occurs in the positive direction; in some systems this may introduce a systematic bias.

TCX, TCY — Control how the device interprets data on the X and Y inputs. A HIGH on TCX or TCY forces the MPY016H to consider the appropriate input as a two's complement number, while a LOW forces the MPY016H to consider the appropriate input as a magnitude only number.

FT, RS, TRIM and TRIL are not registered. The TCX input is registered, and clocked in at the rising edge of the X clock signal, CLK X. The TCY input is also registered, and clocked in at the rising edge of the Y clock signal, CLK Y. The RND input is registered, and clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with loading these control signals can be avoided by the use of normally LOW clocks.

Control (Cont)

Name	Function	Value	J1 Package	C1, L1 Package	F1 Package
RND	Round Control Bit	TTL	Pin 52	Pin 65	Pin 53
TCX	X Input Two's Complement	TTL	Pin 51	Pin 66	Pin 54
TCY	Y Input Two's Complement	TTL	Pin 50	Pin 67	Pin 55
FT	Output Register Feedthrough	TTL	Pin 44	Pin 5	Pin 61
RS	Output Right Shift	TTL	Pin 43	Pin 6	Pin 62
TRIM	MSP Three-State Control	TTL	Pin 42	Pin 7	Pin 63
TRIL	LSP Three-State Control	TTL	Pin 6	Pin 46	Pin 35

Data Inputs

The MPY016H has two 16-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_{15} and Y_{15}, carry the sign information for the two's complement notation. The remaining bits are denoted X_0 through X_{14} and Y_0 through Y_{14} (with X_0 and Y_0 the Least Significant Bits). The input and output formats for fractional two's complement, fractional unsigned magnitude, integer two's complement and integer unsigned magnitude notation are shown in Figures 1 through 6. The Y inputs are multiplexed with the LSP outputs, and hence can only be used when the TRIL control is in a HIGH state.

Name	Function	Value	J1 Package	C1, L1 Package	F1 Package
X_{15}	X Data MSB	TTL	Pin 54	Pin 63	Pin 51
X_{14}		TTL	Pin 55	Pin 62	Pin 50
X_{13}		TTL	Pin 56	Pin 61	Pin 49
X_{12}		TTL	Pin 57	Pin 59	Pin 48
X_{11}		TTL	Pin 58	Pin 58	Pin 47
X_{10}		TTL	Pin 59	Pin 57	Pin 46
X_9		TTL	Pin 60	Pin 56	Pin 45
X_8		TTL	Pin 61	Pin 55	Pin 44
X_7		TTL	Pin 62	Pin 54	Pin 43
X_6		TTL	Pin 63	Pin 53	Pin 42
X_5		TTL	Pin 64	Pin 52	Pin 41
X_4		TTL	Pin 1	Pin 51	Pin 40
X_3		TTL	Pin 2	Pin 50	Pin 39
X_2		TTL	Pin 3	Pin 49	Pin 38
X_1		TTL	Pin 4	Pin 48	Pin 37
X_0	X Data LSB	TTL	Pin 5	Pin 47	Pin 36
Y_{15}	Y Data MSB	TTL	Pin 24	Pin 27	Pin 17
Y_{14}		TTL	Pin 23	Pin 28	Pin 18
Y_{13}		TTL	Pin 22	Pin 29	Pin 19
Y_{12}		TTL	Pin 21	Pin 30	Pin 20
Y_{11}		TTL	Pin 20	Pin 31	Pin 21
Y_{10}		TTL	Pin 19	Pin 32	Pin 22
Y_9		TTL	Pin 18	Pin 33	Pin 23
Y_8		TTL	Pin 17	Pin 34	Pin 24
Y_7		TTL	Pin 16	Pin 35	Pin 25
Y_6		TTL	Pin 15	Pin 36	Pin 26
Y_5		TTL	Pin 14	Pin 37	Pin 27
Y_4		TTL	Pin 13	Pin 38	Pin 28
Y_3		TTL	Pin 12	Pin 39	Pin 29

Data Inputs (Cont.)

Name	Function	Value	J1 Package	C1, L1 Package	F1 Package
Y_2		TTL	Pin 11	Pin 40	Pin 30
Y_1		TTL	Pin 10	Pin 41	Pin 31
Y_0	Y Data LSB	TTL	Pin 9	Pin 42	Pin 32

Data Outputs

The MPY016H has a 32-bit two's complement or unsigned magnitude output which is the product of the two input data values. This output is divided into two 16-bit output words, the Most Significant Product (MSP) and Least Significant Product (LSP). The Most Significant Bit (MSB) of both the MSP and the LSP is the sign bit if fractional two's complement notation is used (TCX=TCY=1, RS=0). The input and output formats for fractional two's complement, fractional unsigned magnitude, fractional mixed mode, integer two's complement, integer unsigned magnitude, and integer mixed mode notation are shown in Figures 1 through 6. The LSP Output can be taken from the Y inputs only when TRIL is LOW. Care must be taken to enable these shared input lines only at the proper time. For an output from the MSP lines to be read, the TRIM control must be LOW. RS is an output format control. A logical "1" on RS deletes the sign bit from the LSP and shifts the MSP down one bit. This is mandatory for unsigned magnitude, mixed mode, or integer two's complement operation.

Name	Function	Value	J1 Package	C1, L1 Package	F1 Package
P_{31}	Product MSB	TTL	Pin 40	Pin 10	Pin 1
P_{30}		TTL	Pin 39	Pin 11	Pin 2
P_{29}		TTL	Pin 38	Pin 12	Pin 3
P_{28}		TTL	Pin 37	Pin 13	Pin 4
P_{27}		TTL	Pin 36	Pin 14	Pin 5
P_{26}		TTL	Pin 35	Pin 15	Pin 6
P_{25}		TTL	Pin 34	Pin 16	Pin 7
P_{24}		TTL	Pin 33	Pin 17	Pin 8
P_{23}		TTL	Pin 32	Pin 18	Pin 9
P_{22}		TTL	Pin 31	Pin 19	Pin 10
P_{21}		TTL	Pin 30	Pin 20	Pin 11
P_{20}		TTL	Pin 29	Pin 21	Pin 12
P_{19}		TTL	Pin 28	Pin 22	Pin 13
P_{18}		TTL	Pin 27	Pin 23	Pin 14
P_{17}		TTL	Pin 26	Pin 24	Pin 15
P_{16}		TTL	Pin 25	Pin 25	Pin 16
P_{15}		TTL	Pin 24	Pin 27	Pin 17
P_{14}		TTL	Pin 23	Pin 28	Pin 18
P_{13}		TTL	Pin 22	Pin 29	Pin 19
P_{12}		TTL	Pin 21	Pin 30	Pin 20
P_{11}		TTL	Pin 20	Pin 31	Pin 21
P_{10}		TTL	Pin 19	Pin 32	Pin 22
P_9		TTL	Pin 18	Pin 33	Pin 23
P_8		TTL	Pin 17	Pin 34	Pin 24
P_7		TTL	Pin 16	Pin 35	Pin 25
P_6		TTL	Pin 15	Pin 36	Pin 26
P_5		TTL	Pin 14	Pin 37	Pin 27
P_4		TTL	Pin 13	Pin 38	Pin 28
P_3		TTL	Pin 12	Pin 39	Pin 29
P_2		TTL	Pin 11	Pin 40	Pin 30
P_1		TTL	Pin 10	Pin 41	Pin 31
P_0	Product LSB	TTL	Pin 9	Pin 42	Pin 32

Clocks

The MPY016H has four clock lines, one for each of the input registers and one for each product register. Data and two's complement instructions present at the inputs of these registers are loaded into the registers at the rising edge of the appropriate clock. The RND input is registered, and clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with loading this control signal can be avoided by the use of normally LOW clocks.

Name	Function	Value	J1 Package	C1, L1 Package	F1 Package
CLK X	Clock Input Data X	TTL	Pin 53	Pin 64	Pin 52
CLK Y	Clock Input Data Y	TTL	Pin 8	Pin 44	Pin 33
CLK L	Clock LSP Register	TTL	Pin 7	Pin 45	Pin 34
CLK M	Clock MSP Register	TTL	Pin 4	Pin 8	Pin 64

No Connects

The chip carrier version of the MPY016H has four pins which are not connected internally. These should be left unconnected.

Name	Function	Value	J1 Package	C1, L1 Package	F1 Package
NC	No Connection	Open	None	Pins 9, 26, 43, 60	None

G

Figure 1. Fractional Two's Complement Notation

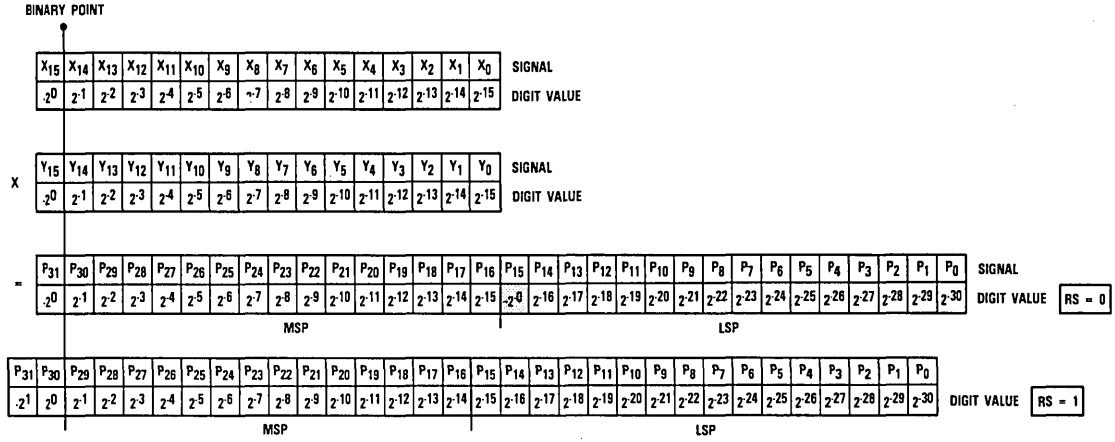

Figure 2. Fractional Unsigned Magnitude Notation

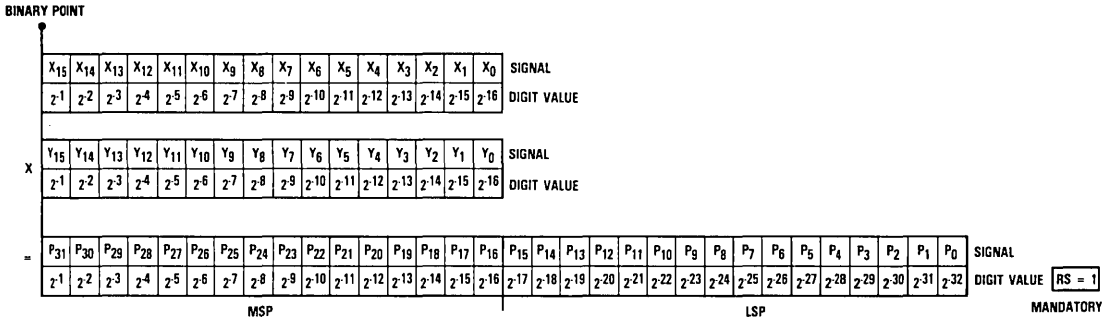

Figure 3. Fractional Mixed Mode Notation

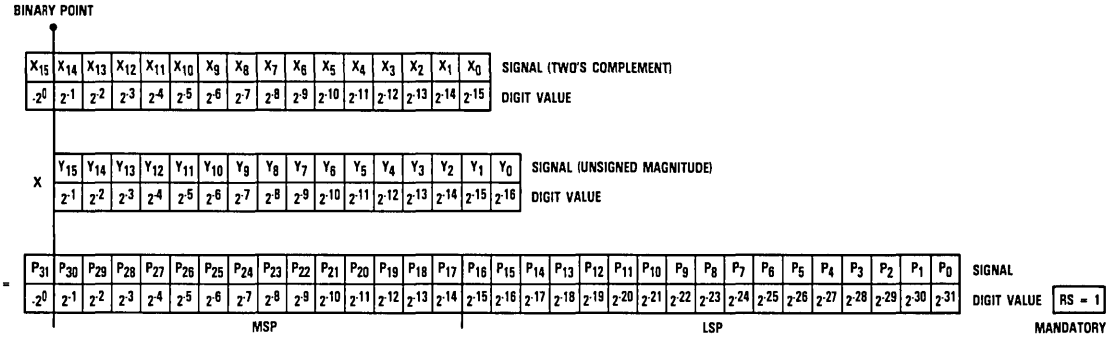

Figure 4. Integer Two's Complement Notation

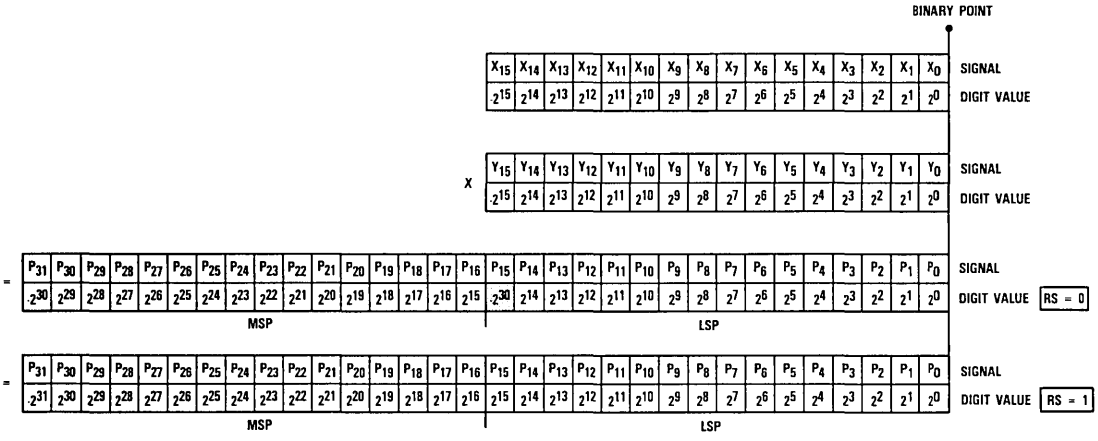

Figure 5. Integer Unsigned Magnitude Notation

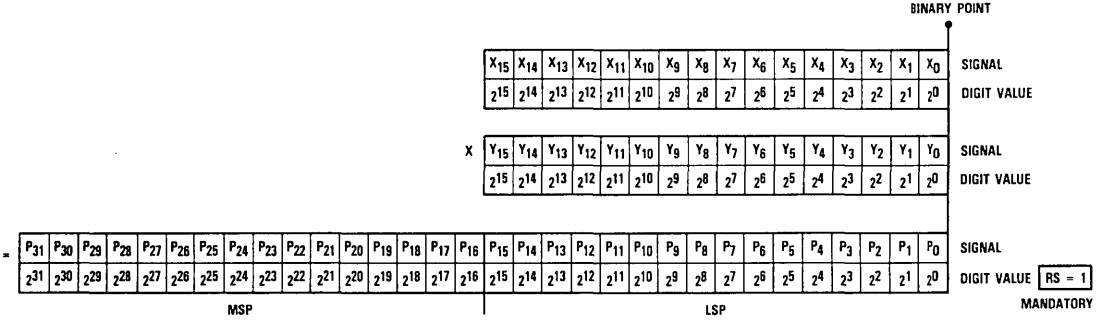

Figure 6. Integer Mixed Mode Notation

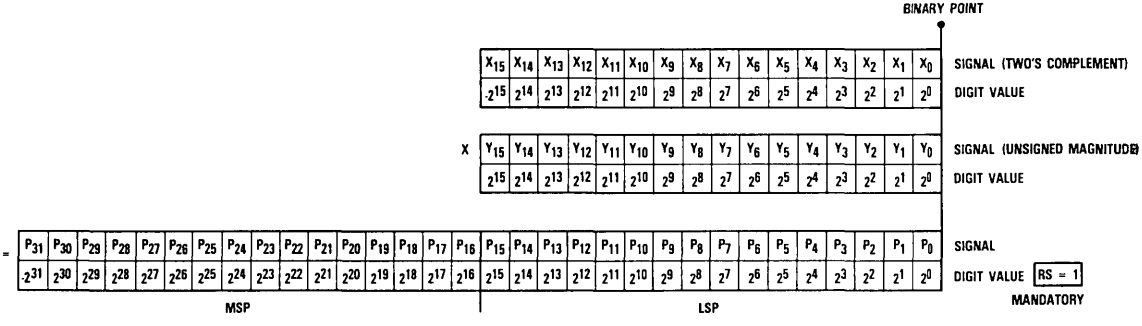

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Figure 7. Timing Diagram

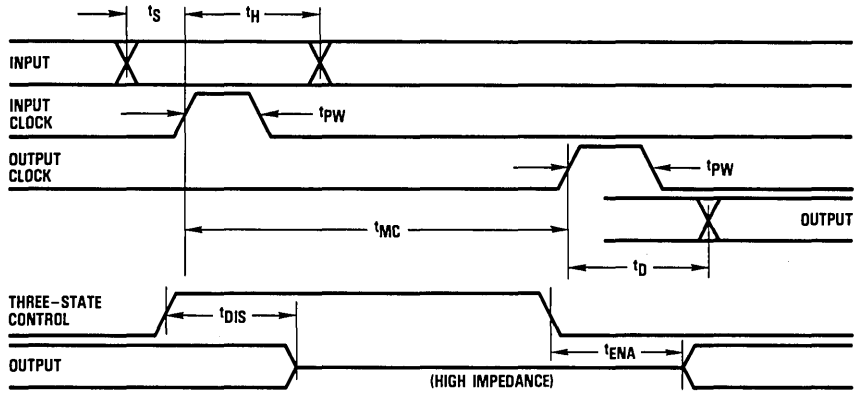


Figure 8. Timing Diagram, Unclocked Mode

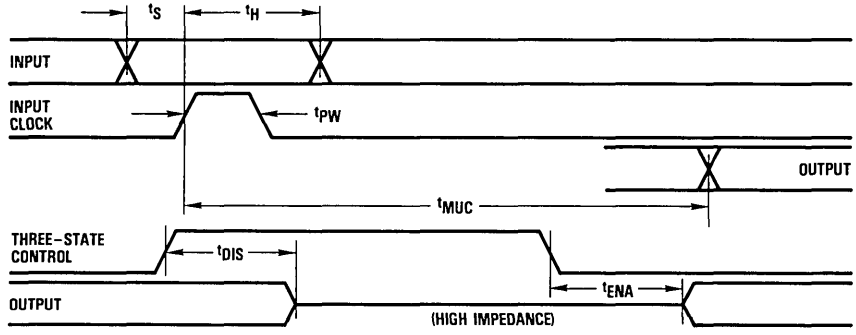
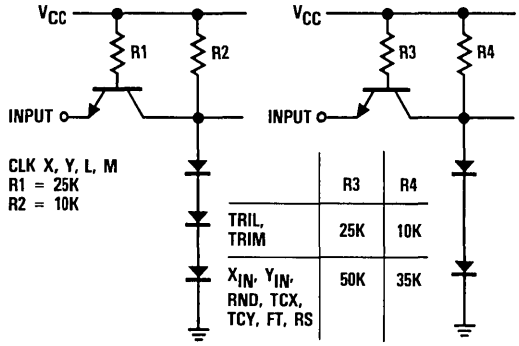


Figure 9. Equivalent Input Circuit



	R3	R4
TRIL, TRIM	25K	10K
X_{IN}, Y_{IN}, RND, TCX, TCY, FT, RS	50K	35K

Figure 10. Equivalent Output Circuit

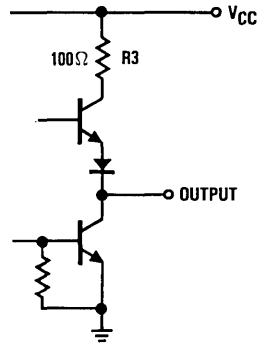


Figure 11. Test Load

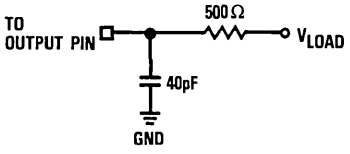
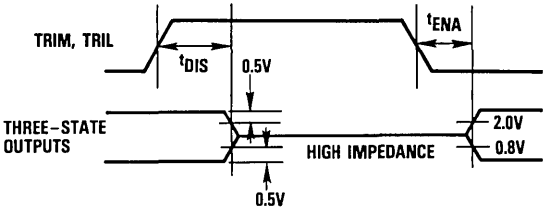


Figure 12. Transition Levels For Three-State Measurements



Application Notes

Mixed Mode Multiplication

There are several applications in which mixed mode multiplication may be advantageous. For example, inputs to a digital signal processor are often generated as unsigned magnitude numbers (e.g., data from an analog-to-digital converter). These numbers are effectively all positive values. In contrast, filter coefficients must often be negative. As a result, either the unsigned magnitude data must be converted to two's complement notation (which requires an additional bit), or the multiplier must be capable of mixed mode operation. The MPY016H provides this capability by independently specifying the mode of the multiplicand (X) and the multiplier (Y) on the TCX and TCY pins. No additional circuitry is required and the resulting product is in two's complement notation.

Multiplication By A Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and that the selected register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection Of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the MPY016H does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64.$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 6.

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Register Shift (RS) Control

In two's complement notation, the acceptable range of values for a given word size is not the same for positive and negative numbers. The largest negative number is one LSB larger than the largest positive number. This is true for either fractional or integer notation. A problem can arise when the largest representable negative number is multiplied by itself. This should give a positive number of the same magnitude. However, the largest representable positive number is one LSB less than this value. As a result, this product cannot be correctly represented without using one additional output bit.

The MPY016H has a Register Shift (RS) control that permits shifting of the result to provide a correct answer for every two's complement multiplication. When RS is active, the value of all bits in the MSP is doubled (i.e., shifted left one position), which provides the capability to represent the largest possible product. The MSB of the Least Significant Product is changed from a duplicate of the sign bit to the necessary bit to fill in the output word. The effects of this control are illustrated in Figures 1 and 4. Note that for unsigned magnitude operation, the RS control must be HIGH.

Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage		−0.5 to +7.0V
Input		
	Applied voltage	−0.5 to +5.5V [2]
	Forced current	−6.0 to +6.0mA
Output		
	Applied voltage	−0.5 to +5.5V [2]
	Forced current	−0.1 to +6.0mA [3,4]
	Short-circuit duration (single output in high state to ground)	1 sec
Temperature		
	Operating, case	−55 to +125°C
	junction	175°C
	Lead, soldering (10 seconds)	300°C
	Storage	−65 to + 150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PW}	Clock Pulse Width	25			30			ns
t_S	Input Register Setup Time	25			30			ns
t_H	Input Register Hold Time	0			3			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = MAX, Static[1]		875		1050	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V					
		X_{IN}, Y_{IN}, RND, FT		−0.4		−0.4	mA
		$\overline{TCX}$, $\overline{TCY}$, $\overline{RS}$		−0.8		−0.8	mA
		CLK L, M, and X; TRIM, $\overline{TRIL}$		−1.0		−1.0	mA
		CLK Y		−2.0		−2.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V					
		X_{IN}, Y_{IN}, RND, FT		75		100	μA
		$\overline{TCX}$, $\overline{TCY}$, $\overline{RS}$		75		100	μA
		CLK L, M, and X; TRIM, $\overline{TRIL}$		75		100	μA
		CLK Y		100		200	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{CC} = MAX, V_I = 0.4V		−40		−40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{CC} = MAX, V_I = 2.4V		40		40	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = MAX, One pin to ground one second duration max, output HIGH		−50		−50	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		10		10	pF

Note:

1. Worst case, all inputs and outputs LOW.

G

Switching characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MC}	Multiply Time, Clocked	V_{CC} = MIN		145		185	ns
t_{MUC}	Multiply Time, Unclocked	V_{CC} = MIN		185		230	ns
t_D	Output Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V		40		45	ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 1.8V		40		45	ns
t_{DIS}	Three-State Output Disable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1}[2]		40		45	ns

Notes:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in Figure 12.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
MPY016HJ1C	STD-T_A = 0°C to 70°C	Commercial	64 Lead DIP	016HJ1C
MPY016HJ1G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	64 Lead DIP	016HJ1G
MPY016HJ1F	EXT-T_C = -55°C to 125°C	Commercial	64 Lead DIP	016HJ1F
MPY016HJ1A	EXT-T_C = -55°C to 125°C	High Reliability[2]	64 Lead DIP	016HJ1A
MPY016HC1F[1]	EXT-T_C = -55°C to 125°C	Commercial	68 Contact Chip Carrier	016HC1F
MPY016HC1A	EXT-T_C = -55°C to 125°C	High Reliability[2]	68 Contact Chip Carrier	016HC1A
MPY016HL1F[1]	EXT-T_C = -55°C to 125°C	Commercial	68 Leaded Chip Carrier	016HL1F
MPY016HL1A[1]	EXT-T_C = -55°C to 125°C	High Reliability[2]	68 Leaded Chip Carrier	016HL1A
MPY016HF1F[1]	EXT-T_C = -55°C to 125°C	Commercial	64 Leaded Flatpack	016HF1F
MPY016HF1A	EXT-T_C = -55°C to 125°C	High Reliability[2]	64 Leaded Flatpack	016HF1A

Notes:

1. Contact Factory for availability.
2. Per TRW document 70Z1757.

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MPY016K
Preliminary Information

VLSI Multiplier
16 X 16 bit, 40ns

The TRW MPY016K is a video-speed 16 X 16 bit parallel multiplier which operates at a 40 nanosecond cycle time (25MHz multiplication rate). The multiplicand and the multiplier may be independently specified as two's complement or unsigned magnitude, yielding a full precision 32-bit product.

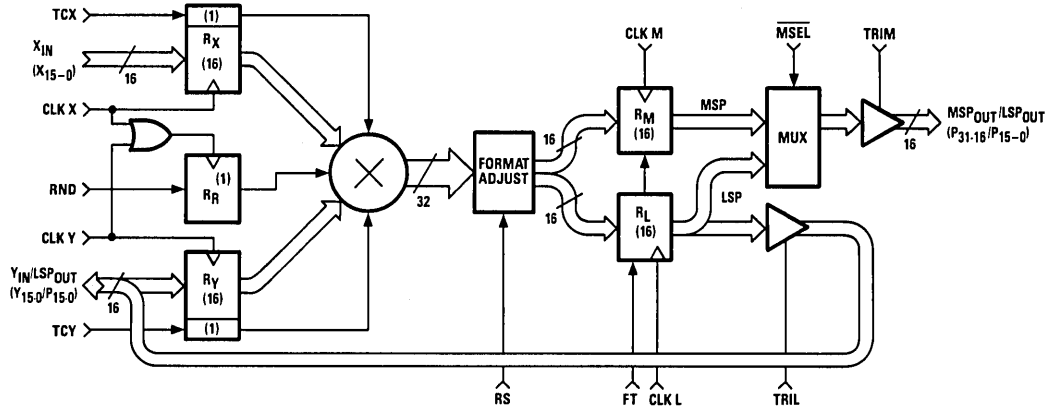
Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The Most Significant Product (MSP) and Least Significant Product (LSP) can be multiplexed through a dedicated output port, or the LSP can share a bidirectional port with the Y input. All outputs are three-state.

Built with TRW's OMICRON-B™ 1-micron bipolar process, the MPY016K is pin compatible with the industry standard MPY016H, and operates with three times the speed at comparable power dissipation. The MPY016K is the industry's first true video-speed 16-bit multiplier.

Features
- 40ns Multiply Time: MPY016K-1 (Worst Case)
- 45ns Multiply Time: MPY016K (Worst Case)
- Pin Compatible With TRW MPY016H
- 16 X 16 Bit Parallel Multiplication With 32-Bit Output
- Two Least Significant Product Output Modes: Multiplexed With Most Significant Product Or Multiplexed With Y Input
- Output Registers Can Be Made Transparent
- Three-State TTL Output
- Two's Complement, Unsigned Magnitude, Or Mixed Mode Multiplication
- Fully TTL Compatible
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In 64 Lead Ceramic DIP, 68 Contact Chip Carrier Or 68 Leaded Chip Carrier

Applications
- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



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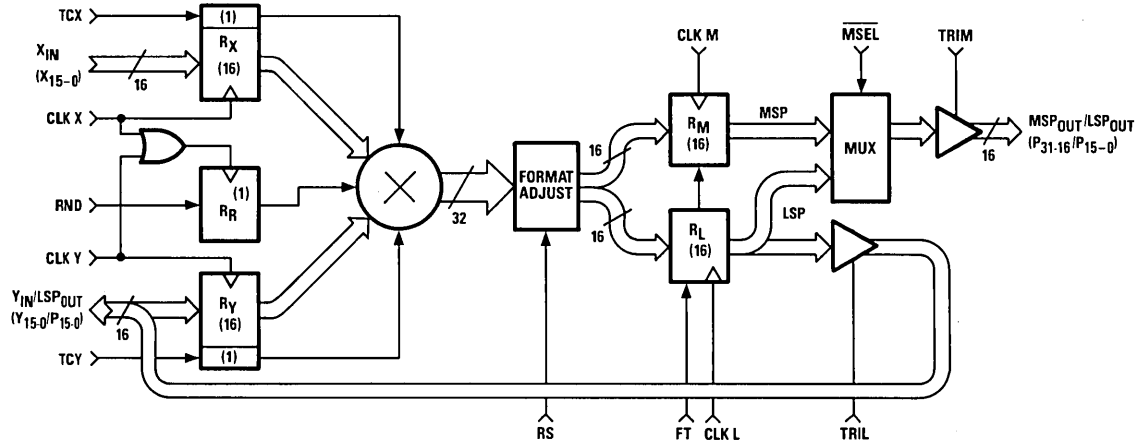
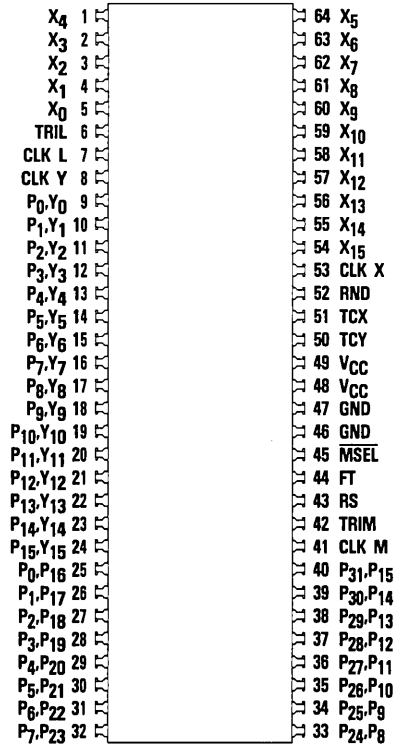
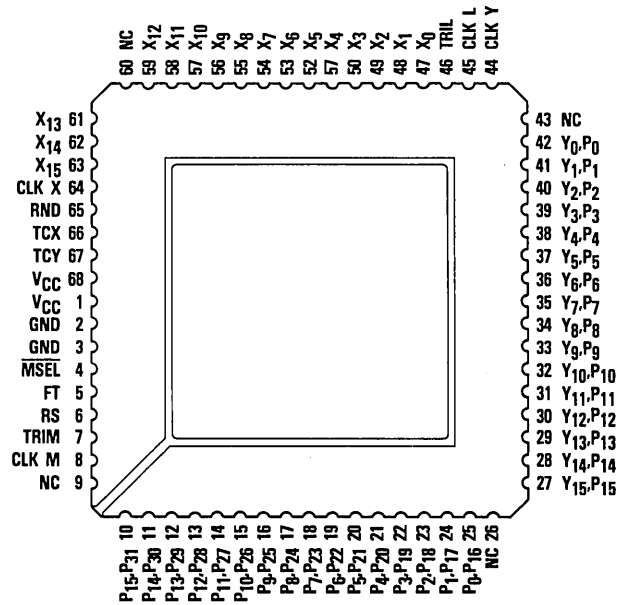
Functional Block Diagram



Pin Assignments



64 Lead DIP – J1 Package



68 Contact or Leaded Chip Carrier – C1, L1 Package

Functional Description

General Information

The MPY016K has three functional sections: Input registers, an asynchronous multiplier array, and output registers. The input registers store the two 16-bit numbers which are to be multiplied and the instruction which controls the output rounding. The rounding control is used when a single-word output is desired. Each input operand is stored independently, simplifying multiplication by a constant. The asynchronous multiplier array is a network of AND gates and adders, designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 16-bit words, the Most Significant Product (MSP) and the Least Significant Product (LSP). Three-state output drivers allow the MPY016K to be used on a bus, or allow the least and most significant outputs to be multiplexed over the same 16-bit output lines. The Least Significant Product (LSP) is multiplexed with the Y input.

Power

The MPY016K operates from a single +5.0V supply. All power and ground lines must be connected. Note that the device is pin-compatible with the MPY016H, which has an additional ground pin; this is a control lead in the MPY016K. A ground on this pin (which must exist in all MPY016H applications) will cause the MPY016K to function like an MPY016H.

Name	Function	Value	J1 Package	C1, L1 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pins 48, 49	Pins 1, 68
GND	Ground	0.0V	Pins 46, 47	Pins 2, 3

Data Inputs

The MPY016K has two 16-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_{15} and Y_{15}, carry the sign information for the two's complement notation. The remaining bits are denoted X_0 through X_{14} and Y_0 through Y_{14} (with X_0 and Y_0 the Least Significant Bits). The input and output formats for fractional two's complement, fractional unsigned magnitude, fractional mixed mode, integer two's complement, integer unsigned magnitude, and integer mixed mode notation are shown in Figures 1 through 6, respectively. The Y inputs are multiplexed with the LSP outputs, and hence can only be used when the TRIL control is in a HIGH state. This is true whether or not the LSP is also multiplexed out through the MSP output port.

Name	Function	Value	J1 Package	C1, L1 Package
X_{15}	X Data MSB	TTL	Pin 54	Pin 63
X_{14}		TTL	Pin 55	Pin 62
X_{13}		TTL	Pin 56	Pin 61
X_{12}		TTL	Pin 57	Pin 59
X_{11}		TTL	Pin 58	Pin 58
X_{10}		TTL	Pin 59	Pin 57
X_9		TTL	Pin 60	Pin 56
X_8		TTL	Pin 61	Pin 55
X_7		TTL	Pin 62	Pin 54
X_6		TTL	Pin 63	Pin 53
X_5		TTL	Pin 64	Pin 52
X_4		TTL	Pin 1	Pin 51
X_3		TTL	Pin 2	Pin 50
X_2		TTL	Pin 3	Pin 49
X_1		TTL	Pin 4	Pin 48
X_0	X Data LSB	TTL	Pin 5	Pin 47

Data Inputs (Cont.)

Name	Function	Value	J1 Package	C1, L1 Package
Y_{15}	Y Data MSB	TTL	Pin 24	Pin 27
Y_{14}		TTL	Pin 23	Pin 28
Y_{13}		TTL	Pin 22	Pin 29
Y_{12}		TTL	Pin 21	Pin 30
Y_{11}		TTL	Pin 20	Pin 31
Y_{10}		TTL	Pin 19	Pin 32
Y_9		TTL	Pin 18	Pin 33
Y_8		TTL	Pin 17	Pin 34
Y_7		TTL	Pin 16	Pin 35
Y_6		TTL	Pin 15	Pin 36
Y_5		TTL	Pin 14	Pin 37
Y_4		TTL	Pin 13	Pin 38
Y_3		TTL	Pin 12	Pin 39
Y_2		TTL	Pin 11	Pin 40
Y_1		TTL	Pin 10	Pin 41
Y_0	Y Data LSB	TTL	Pin 9	Pin 42

Data Outputs

The MPY016K has a 32-bit two's complement or unsigned magnitude output which is the product of the two input data values. This output is divided into two 16-bit output words, the Most Significant Product (MSP) and Least Significant Product (LSP). The Most Significant Bit (MSB) of both the MSP and the LSP is the sign bit if fractional two's complement notation is used (TCX = TCY = 1, RS = 0). The input and output formats for fractional two's complement, fractional unsigned magnitude, fractional mixed mode, integer two's complement, integer unsigned magnitude, and integer mixed mode notation are shown in Figures 1 through 6, respectively.

If $\overline{\text{MSEL}}$ is LOW, the LSP output can be taken from the Y input pins only when TRIL is LOW. Care must be taken to enable these shared input lines only at the proper time. If $\overline{\text{MSEL}}$ is HIGH, the LSP output is made available at the MSP lines, as well as at the Y input pins. For an output from the MSP lines to be read, the TRIM control must be active.

RS is an output format control. A HIGH on RS deletes the sign bit from the LSP and shifts the MSP down one bit. This is mandatory for unsigned magnitude, mixed mode, or integer two's complement operation.

Name	Function	Value	J1 Package	C1, L1 Package
P_{31}	Product MSB	TTL	Pin 40	Pin 10
P_{30}		TTL	Pin 39	Pin 11
P_{29}		TTL	Pin 38	Pin 12
P_{28}		TTL	Pin 37	Pin 13
P_{27}		TTL	Pin 36	Pin 14
P_{26}		TTL	Pin 35	Pin 15
P_{25}		TTL	Pin 34	Pin 16
P_{24}		TTL	Pin 33	Pin 17
P_{23}		TTL	Pin 32	Pin 18
P_{22}		TTL	Pin 31	Pin 19
P_{21}		TTL	Pin 30	Pin 20
P_{20}		TTL	Pin 29	Pin 21
P_{19}		TTL	Pin 28	Pin 22
P_{18}		TTL	Pin 27	Pin 23
P_{17}		TTL	Pin 26	Pin 24
P_{16}		TTL	Pin 25	Pin 25

Data Outputs (Cont.)

Name	Function	Value	J1 Package	C1, L1 Package
			MUXED	
			Input/Output	Input/Output
P_{15}		TTL	Pin 24/Pin 40	Pin 27/Pin 10
P_{14}		TTL	Pin 23/Pin 39	Pin 28/Pin 11
P_{13}		TTL	Pin 22/Pin 38	Pin 29/Pin 12
P_{12}		TTL	Pin 21/Pin 37	Pin 30/Pin 13
P_{11}		TTL	Pin 20/Pin 36	Pin 31/Pin 14
P_{10}		TTL	Pin 19/Pin 35	Pin 32/Pin 15
P_9		TTL	Pin 18/Pin 34	Pin 33/Pin 16
P_8		TTL	Pin 17/Pin 33	Pin 34/Pin 17
P_7		TTL	Pin 16/Pin 32	Pin 35/Pin 18
P_6		TTL	Pin 15/Pin 31	Pin 36/Pin 19
P_5		TTL	Pin 14/Pin 30	Pin 37/Pin 20
P_4		TTL	Pin 13/Pin 29	Pin 38/Pin 21
P_3		TTL	Pin 12/Pin 28	Pin 39/Pin 22
P_2		TTL	Pin 11/Pin 27	Pin 40/Pin 23
P_1		TTL	Pin 10/Pin 26	Pin 41/Pin 24
P_0	Product LSB	TTL	Pin 9/Pin 25	Pin 42/Pin 25

Clocks

The MPY016K has four clock lines, one for each input register and one for each product register. Data and two's complement instructions present at the inputs of these registers are loaded into the registers at the rising edge of the appropriate clock. The RND input is registered, clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with loading this control signal can be avoided by the use of normally LOW clocks.

Name	Function	Value	J1 Package	C1, L1 Package
CLK X	Clock Input Data X	TTL	Pin 53	Pin 64
CLK Y	Clock Input Data Y	TTL	Pin 8	Pin 44
CLK L	Clock LSP Register	TTL	Pin 7	Pin 45
CLK M	Clock MSP Register	TTL	Pin 41	Pin 8

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Controls

The MPY016K has eight control lines.

FT — A control line which makes the output register transparent if it is HIGH.

TRIM, TRIL — Three-state enable lines for the MSP and the LSP. The output driver is in the high-impedance state when TRIM or TRIL is HIGH, and enabled when the appropriate control is LOW.

RS — RS is an output format control. A HIGH level on RS deletes the sign bit from the LSP and shifts the MSP down one bit. This is mandatory for unsigned magnitude, mixed mode, and two's complement integer operations.

$\overline{\text{MSEL}}$ — $\overline{\text{MSEL}}$ is an output multiplex control. When $\overline{\text{MSEL}}$ is LOW, the MSP is available to the output three-state drivers at the MSP port, and the LSP is available to the output three-state drivers at the LSP/Y input port. When $\overline{\text{MSEL}}$ is HIGH, the LSP is available to both three-state drivers and the MSP is not available.

RND — When RND is HIGH, a one is added to the MSB of the LSP. Note that this bit depends on the state of the RS control. If RS is LOW when RND is HIGH, a one will be added to the 2^{-16} bit (P_{14}). If RS is HIGH when RND is HIGH, a one will be added to the 2^{-15} bit (P_{15}). In either case, the LSP output will reflect this addition when RND is HIGH. Note also that rounding always occurs in the positive direction; in some systems this may introduce a systematic bias.

TCX, TCY — Control how the device interprets data on the X and Y inputs. A HIGH on TCX or TCY makes the appropriate input a two's complement input, while a LOW makes the appropriate input a magnitude only input.

FT, RS, $\overline{\text{MSEL}}$, TRIM, and TRIL are not registered. The TCX input is registered, and clocked in at the rising edge of the X clock signal, CLK X. The TCY input is also registered, and clocked in at the rising edge of the Y clock signal, CLK Y. The RND input is registered, and clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention is required if normally HIGH clock signals are used. Problems with loading of these control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J1 Package	C1, L1 Package
RND	Round Control Bit	TTL	Pin 52	Pin 65
TCX	X Input Two's Complement	TTL	Pin 51	Pin 66
TCY	Y Input Two's Complement	TTL	Pin 50	Pin 67
FT	Output Register Feedthrough	TTL	Pin 44	Pin 5
RS	Output Register Shift	TTL	Pin 43	Pin 6
$\overline{\text{MSEL}}$	Output Select	TTL	Pin 45	Pin 4
TRIM	MSP Three-State Control	TTL	Pin 42	Pin 7
TRIL	LSP Three-State Control	TTL	Pin 6	Pin 46

No Connects

The contact and leaded chip carrier versions of the MPY016K have four pins which are not connected internally. These may be left unconnected.

Name	Function	Value	J1 Package	C1, L1 Package
NC	No Connection	Open	None	Pins 9, 26, 43, 60

Figure 1. Fractional Two's Complement Notation

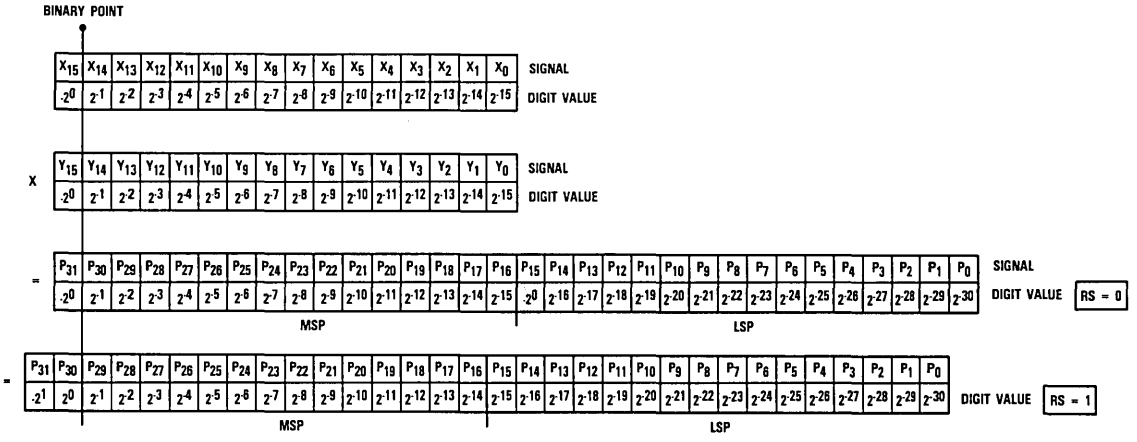

Figure 2. Fractional Unsigned Magnitude Notation

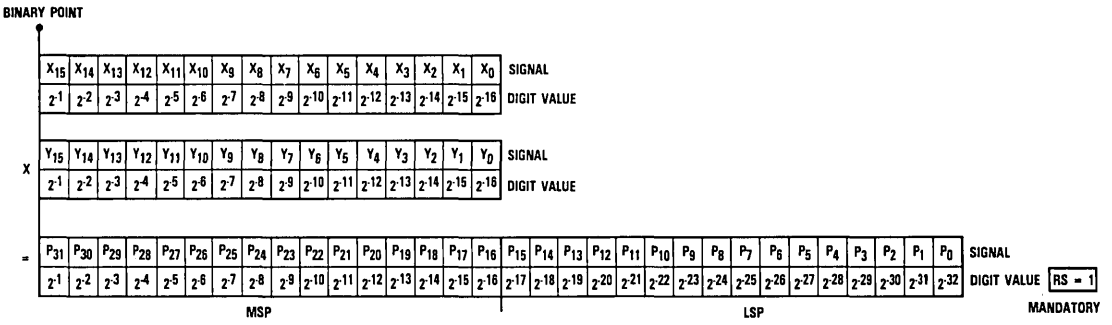

Figure 3. Fractional Mixed Mode Notation

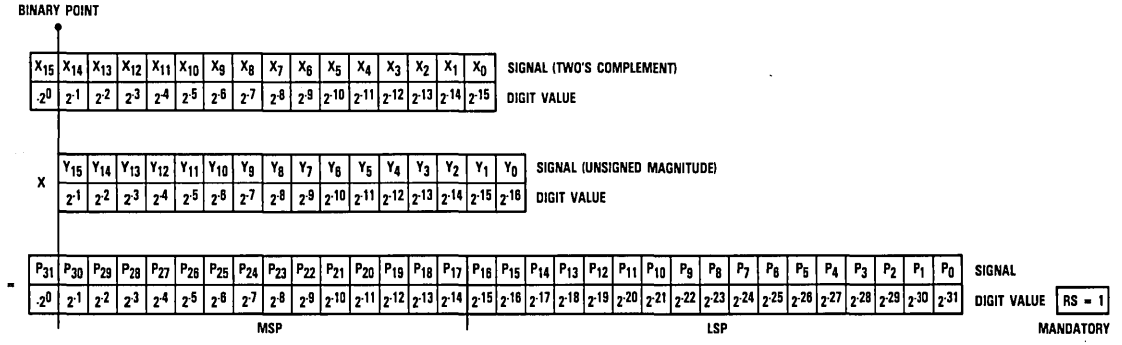

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Figure 4. Integer Two's Complement Notation

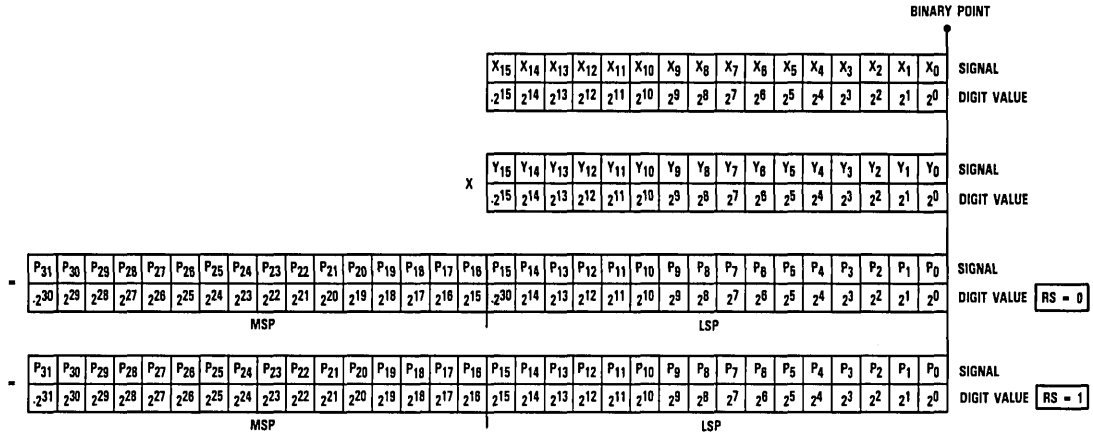

Figure 5. Integer Unsigned Magnitude Notation

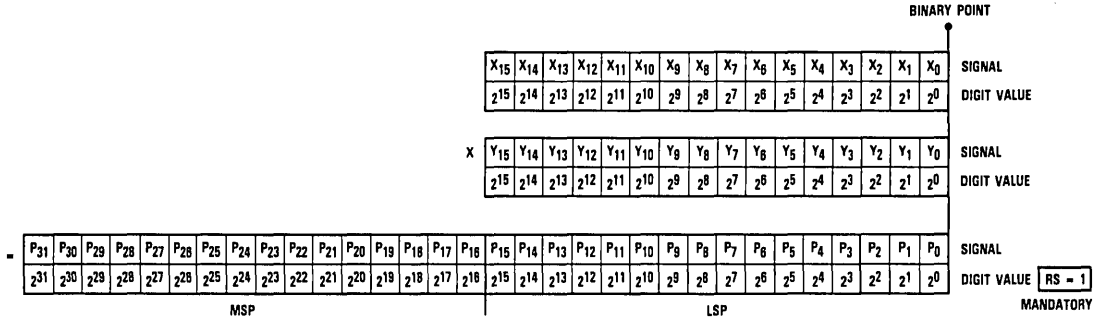

Figure 6. Integer Mixed Mode Notation

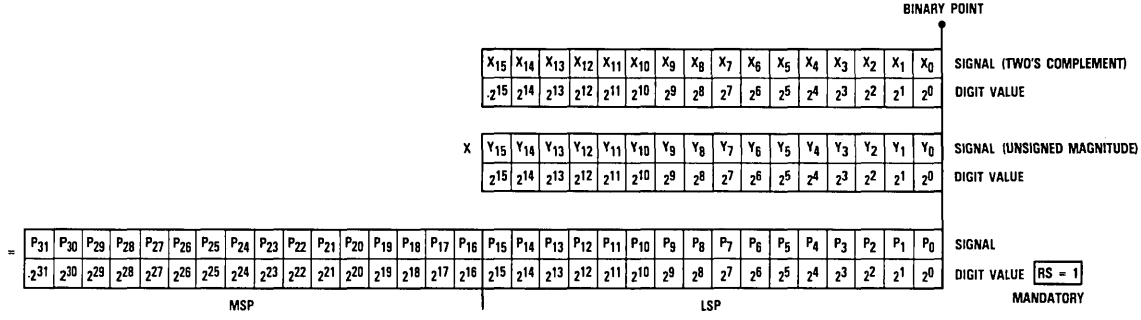

Figure 7. Timing Diagram, Non-Multiplexed Output

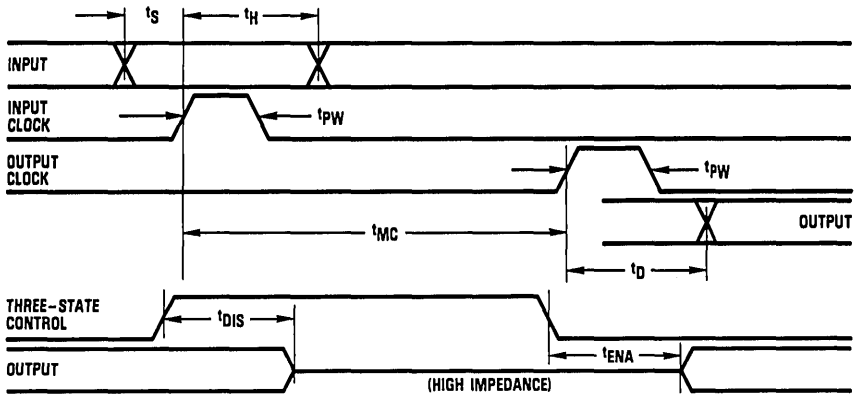

Figure 8. Timing Diagram, Unclocked Mode, Non-Multiplexed Output

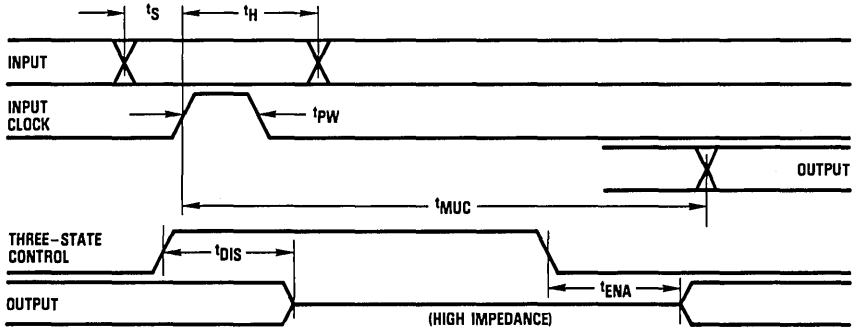

Figure 9. Timing Diagram, Multiplexed Output

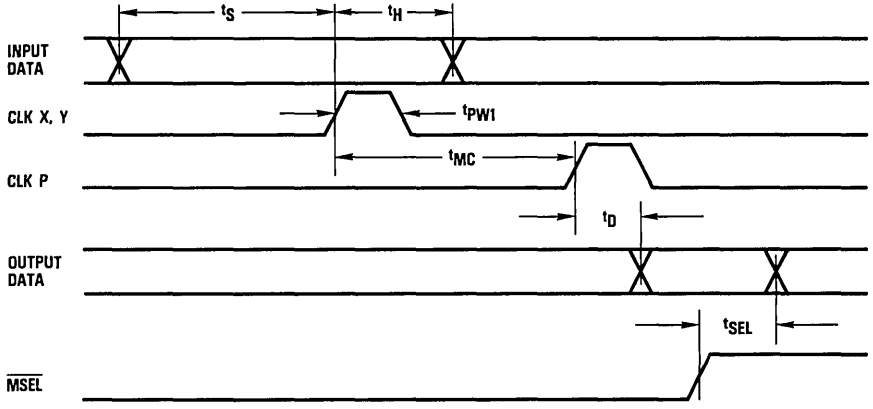

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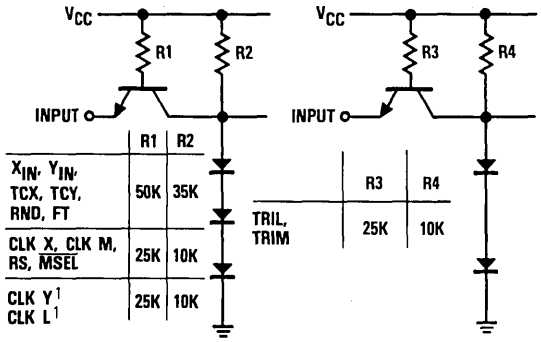
Figure 10. Equivalent Input Circuit



	R1	R2
X_{IN}, Y_{IN}, TCX, TCY, RND, FT	50K	35K
CLK X, CLK M, RS, $\overline{MSEL}$	25K	10K
CLK Y[1] CLK L[1]	25K	10K

	R3	R4
TRIL, TRIM	25K	10K

Note: 1. CLK Y and CLK L each drive two equivalent inputs.

Figure 11. Equivalent Output Circuit

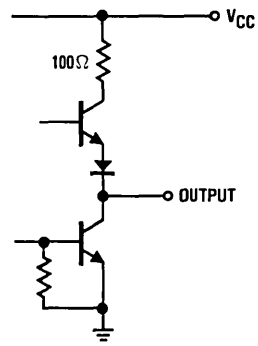


Figure 12. Test Load

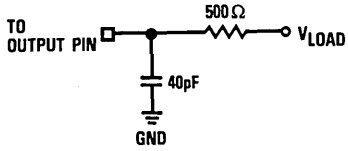
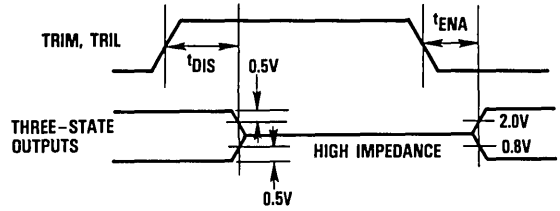


Figure 13. Transition Levels For Three-State Measurements



Application Notes

Mixed Mode Multiplication

There are several applications in which mixed mode multiplication may be advantageous. For example, inputs to a digital signal processor are often generated as unsigned magnitude numbers (e.g., data from an analog-to-digital converter). These numbers are effectively all positive values. In contrast, filter coefficients must often be negative. As a result, either the data must be converted to two's complement notation (which requires an additional bit), or the multiplier must be capable of mixed mode operation. The MPY016K provides this capability by independently specifying the mode of the multiplicand (X) and the multiplier (Y) on the TCX and TCY pins. No additional circuitry is required and the resulting product is in two's complement notation.

Multiplication By A Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and that the desired register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection Of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the MPY016K does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64.$$

The difference lies in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 6.

Register Shift (RS) Control

In two's complement notation, the acceptable range of values for a given word size is not the same for positive and negative numbers. The largest negative number is one LSB larger than the largest positive number. This is true for either fractional or integer notation. A problem can arise when the largest representable negative number is multiplied by itself. This should give a positive number of the same magnitude. However, the largest representable positive number is one LSB less than this value. As a result, this product cannot be correctly represented without using one additional output bit. The MPY016K has a Register Shift (RS) control that permits shifting of the result to provide a correct answer for every two's complement multiplication. When RS is active, the value of all bits in the MSP is doubled (i.e. shifted left one position), which provides the capability to represent the largest possible product. The MSB of the Least Significant Product is changed from a duplicate of the sign bit to the necessary bit to fill in the output word. The effects of this control are illustrated in Figures 1 and 4. Note that for unsigned magnitude operation, the RS control must be HIGH.

Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−6.0 to +6.0mA
Output	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−0.1 to +6.0mA [3,4]
Short-circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, case	−60 to +140°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Extended Min	Extended Nom	Extended Max	Units
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PWL}	Clock Pulse Width, LOW	15			22			ns
t_{PWH}	Clock Pulse Width, HIGH	15			22			ns
t_S	Input Setup Time (MPY016K)	20			25			ns
	(MPY016K-1)	20			20			ns
t_H	Input Hold Time	0			2			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		+125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = MAX, Static[1]					
		T_A = 0°C to 70°C		875			mA
		T_A > 25°C[2]		860			mA
		T_C = −55°C to +125°C				1050	mA
		T_C > 35°C				960	mA
		V_{CC} = 5.0V					
		T_A > 25°C		840			mA
		T_C > 35°C				920	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V					
		X_{IN}, Y_{IN}, TCY, TCX, FT, RND		−0.2		−0.2	mA
		CLK Y, CLK L		−1.2		−1.2	mA
		CLK X, CLK M, $\overline{\text{MSEL}}$, TRIM, TRIL, RS		−0.6		−0.6	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V					
		X_{IN}, Y_{IN}, TCY, TCX, FT, RND		50		50	μA
		CLK Y, CLK L		100		100	μA
		CLK X, CLK M, $\overline{\text{MSEL}}$, TRIM, TRIL, RS		50		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MAX, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{CC} = MAX, V_I = 0.4V					
		Non-Shared Pins		−40		−50	μA
		Shared Pins		−200		−200	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{CC} = MAX, V_I = 2.4V					
		Non-Shared Pins		40		50	μA
		Shared Pins		50		50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, One pin to ground, one second duration, output HIGH.	−4	−50	−4	−50	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		10		10	pF

Notes:

1. Worst case, all inputs and outputs LOW.
2. Part has a negative temperature coefficient, i.e., power consumption falls as temperature increases.

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Switching characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MC}	Multiply Time, Clocked	V_{CC} = MIN (MPY016K)		45		50	ns
		V_{CC} = MIN (MPY016K-1)		40		45	ns
t_{MUC}	Multiply Time, Unclocked	V_{CC} = MIN (MPY016K)		75		85	ns
		V_{CC} = MIN (MPY016K-1)		70		75	ns
t_D	Output Delay	V_{CC} = MIN, (MPY016K) Test Load: V_{LOAD} = 2.2V		30		35	ns
		V_{CC} = MIN, (MPY016K-1) Test Load: V_{LOAD} = 2.2V		30		30	ns
t_{SEL}	Output Multiplex Select Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V		20		25	ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 1.8V		30		35	ns
t_{DIS}	Three-State Output Disable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1}[2]		30		35	ns

Notes:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in Figure 13.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
MPY016KJ1C	STD-T_A = 0°C to 70°C	Commercial	64 Lead DIP	016KJ1C
MPY016KJ1C1	STD-T_A = 0°C to 70°C	Commercial	64 Lead DIP	016KJ1C1
MPY016KJ1G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	64 Lead DIP	016KJ1G
MPY016KJ1G1	STD-T_A = 0°C to 70°C	Commercial With Burn-In	64 Lead DIP	016KJ1G1
MPY016KJ1F	EXT-T_C = -55°C to 125°C	Commercial	64 Lead DIP	016KJ1F
MPY016KJ1F1	EXT-T_C = -55°C to 125°C	Commercial	64 Lead DIP	016KJ1F1
MPY016KJ1A	EXT-T_C = -55°C to 125°C	High Reliability[2]	64 Lead DIP	016KJ1A
MPY016KJ1A1	EXT-T_C = -55°C to 125°C	High Reliability[2]	64 Lead DIP	016KJ1A1
MPY016KC1F[1]	EXT-T_C = -55°C to 125°C	Commercial	68 Contact Chip Carrier	016KC1F
MPY016KC1A[1]	EXT-T_C = -55°C to 125°C	High Reliability[2]	68 Contact Chip Carrier	016KC1A
MPY016KL1F[1]	EXT-T_C = -55°C to 125°C	Commercial	68 Leaded Chip Carrier	016KL1F
MPY016KL1A[1]	EXT-T_C = -55°C to 125°C	High Reliability[2]	68 Leaded Chip Carrier	016KL1A

Notes:

1. Contact factory for availability.
2. Per TRW document 70Z1757.

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Preliminary Information describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact TRW for current information.

TMC216H
Preliminary Information

CMOS Multiplier
16 X 16 bit, 145ns

The TRW TMC216H is a high-speed 16 X 16 bit parallel multiplier which operates at a 145 nanosecond cycle time (6.9MHz multiplication rate). The multiplicand and the multiplier may be independently specified as two's complement or unsigned magnitude, yielding a full precision 32-bit product.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The Least Significant Product (LSP) shares a bidirectional port with the Y input. All outputs are three-state.

Built with TRW's state of the art 2-micron CMOS process, the TMC216H is pin and function compatible with the industry standard MPY016H and operates with the same speed at approximately one-fifth the power dissipation.

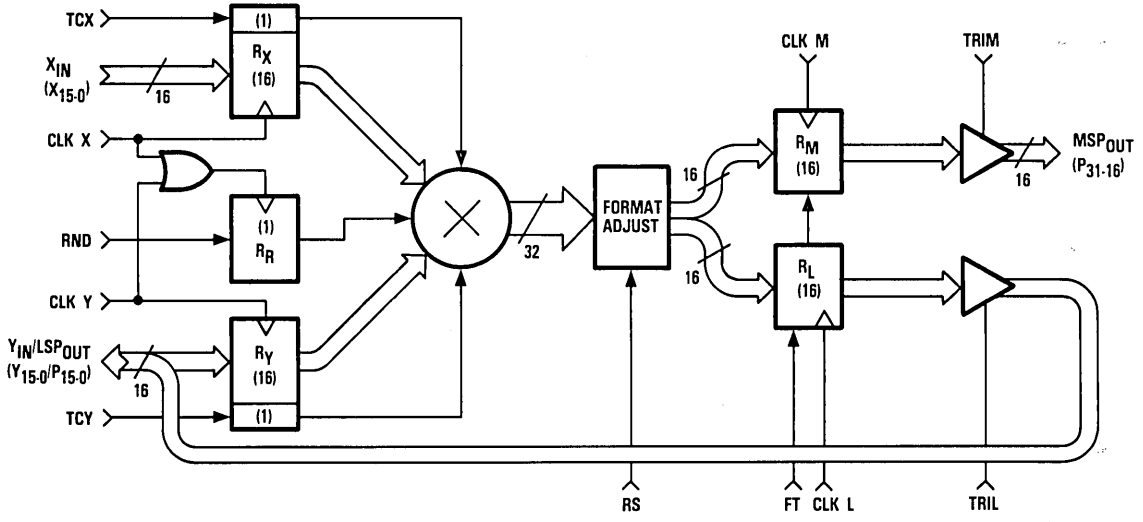
Features

- Fully TTL Compatible
- 145ns Multiply Time (Worst Case)
- Low Power CMOS Technology
- Single +5V Power Supply
- Pin And Function Compatible With TRW MPY016H
- Output Registers Can Be Made Transparent
- Three-State Outputs
- Two's Complement, Unsigned Magnitude, Or Mixed Mode Multiplication
- Available In 64 Lead DIP, 68 Contact Chip Carrier, Or 68 Leaded Chip Carrier

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



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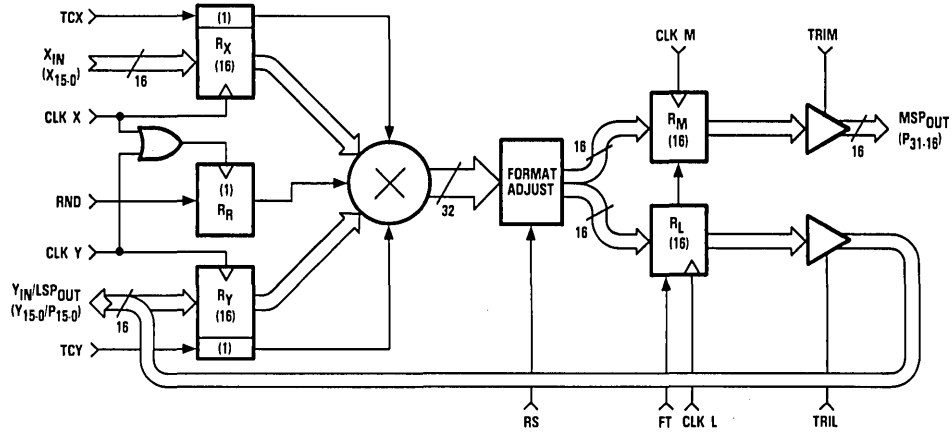
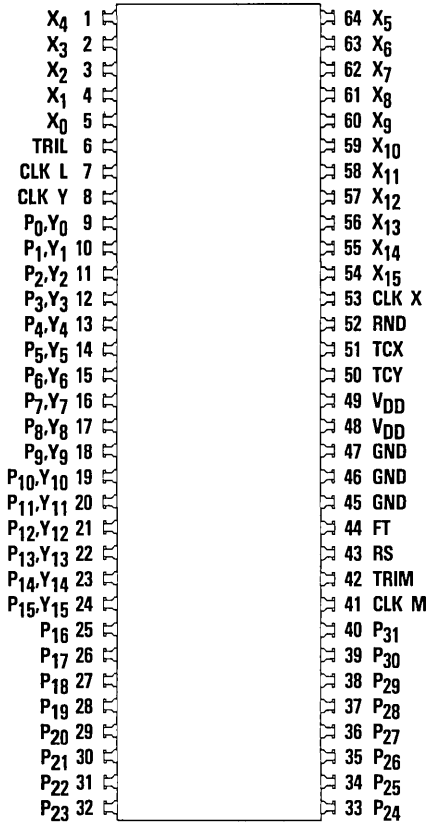
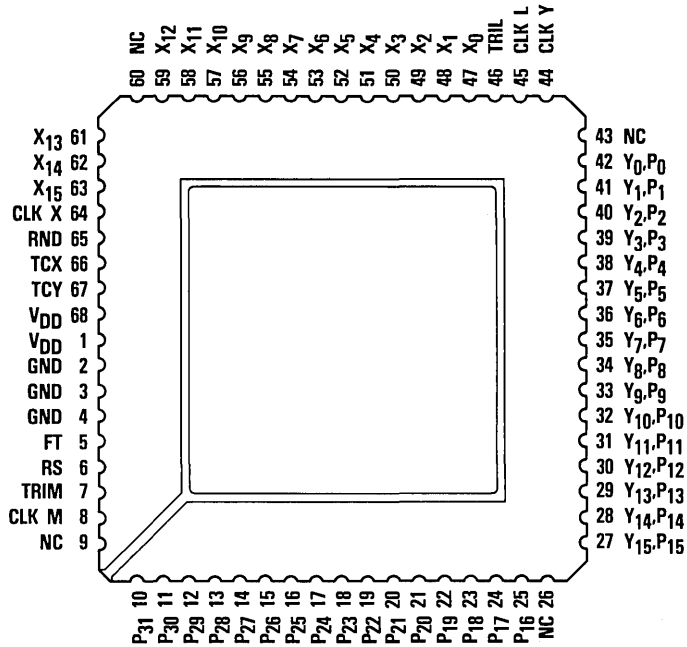
Functional Block Diagram



Pin Assignments



64 Lead DIP – J3 Package



68 Contact Or Leaded Chip Carrier – C1, L1 Package

Functional Description

General Information

The TMC216H has three functional sections: Input registers, an asynchronous multiplier array, and output registers. The input registers store the two 16-bit numbers which are to be multiplied and the instruction which controls the output rounding. The rounding control is used when a single-word output is desired. Each input operand is stored independently, simplifying multiplication by a constant. The asynchronous multiplier array is a network of AND gates and adders, designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 16-bit words, the Most Significant Product (MSP) and the Least Significant Product (LSP). Three-state output drivers allow the TMC216H to be used on a bus, or allow the Y input, least and most significant outputs to be multiplexed over the same 16-bit input/output lines. The Least Significant Product (LSP) is multiplexed with the Y input.

Power

The TMC216H operates from a single +5 Volt supply. All power and ground lines must be connected. Note that the device is pin and function compatible with the MPY016H.

Name	Function	Value	J3 Package	C1, L1 Package
V_{DD}	Positive Supply Voltage	+5.0V	Pins 48, 49	Pins 1, 68
GND	Ground	0.0V	Pins 45, 46, 47	Pins 2, 3, 4

Data Inputs

The TMC216H has two 16-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_{15} and Y_{15}, carry the sign information for the two's complement notation. The remaining bits are denoted X_0 through X_{14} and Y_0 through Y_{14} (with X_0 and Y_0 the Least Significant Bits). The input and output formats for fractional two's complement, fractional unsigned magnitude, fractional mixed mode, integer two's complement, integer unsigned magnitude, and integer mixed mode notation are shown in Figures 1 through 6, respectively. The Y inputs are multiplexed with the LSP outputs, and hence can only be used when the TRIL control is in a HIGH state.

Name	Function	Value	J3 Package	C1, L1 Package
X_{15}	X Data MSB	TTL	Pin 54	Pin 63
X_{14}		TTL	Pin 55	Pin 62
X_{13}		TTL	Pin 56	Pin 61
X_{12}		TTL	Pin 57	Pin 59
X_{11}		TTL	Pin 58	Pin 58
X_{10}		TTL	Pin 59	Pin 57
X_9		TTL	Pin 60	Pin 56
X_8		TTL	Pin 61	Pin 55
X_7		TTL	Pin 62	Pin 54
X_6		TTL	Pin 63	Pin 53
X_5		TTL	Pin 64	Pin 52
X_4		TTL	Pin 1	Pin 51
X_3		TTL	Pin 2	Pin 50
X_2		TTL	Pin 3	Pin 49
X_1		TTL	Pin 4	Pin 48
X_0	X Data LSB	TTL	Pin 5	Pin 47

Data Inputs (Cont.)

Name	Function	Value	J3 Package	C1, L1 Package
Y_{15}	Y Data MSB	TTL	Pin 24	Pin 27
Y_{14}		TTL	Pin 23	Pin 28
Y_{13}		TTL	Pin 22	Pin 29
Y_{12}		TTL	Pin 21	Pin 30
Y_{11}		TTL	Pin 20	Pin 31
Y_{10}		TTL	Pin 19	Pin 32
Y_9		TTL	Pin 18	Pin 33
Y_8		TTL	Pin 17	Pin 34
Y_7		TTL	Pin 16	Pin 35
Y_6		TTL	Pin 15	Pin 36
Y_5		TTL	Pin 14	Pin 37
Y_4		TTL	Pin 13	Pin 38
Y_3		TTL	Pin 12	Pin 39
Y_2		TTL	Pin 11	Pin 40
Y_1		TTL	Pin 10	Pin 41
Y_0	Y Data LSB	TTL	Pin 9	Pin 42

Data Outputs

The TMC216H has a 32-bit two's complement or unsigned magnitude output which is the product of the two input data values. This output is divided into two 16-bit output words, the Most Significant Product (MSP) and Least Significant Product (LSP). The Most Significant Bit (MSB) of both the MSP and the LSP is the sign bit if fractional two's complement notation is used (TCX=TCY=1, RS=0). The input and output formats for fractional two's complement, fractional unsigned magnitude, fractional mixed mode, integer two's complement, integer unsigned magnitude, and integer mixed mode notation are shown in Figures 1 through 6, respectively.

The LSP output can be taken from the Y input pins only when TRIL is LOW. Care must be taken to enable these shared input lines only at the proper time. For an output from the MSP lines to be read, the TRIM control must be LOW.

RS is an output format control. A HIGH on RS deletes the sign bit from the LSP and shifts the MSP down one bit. This is mandatory for unsigned magnitude, mixed mode, or integer two's complement operation.

Name	Function	Value	J3 Package	C1, L1 Package
P_{31}	Product MSB	TTL	Pin 40	Pin 10
P_{30}		TTL	Pin 39	Pin 11
P_{29}		TTL	Pin 38	Pin 12
P_{28}		TTL	Pin 37	Pin 13
P_{27}		TTL	Pin 36	Pin 14
P_{26}		TTL	Pin 35	Pin 15
P_{25}		TTL	Pin 34	Pin 16
P_{24}		TTL	Pin 33	Pin 17
P_{23}		TTL	Pin 32	Pin 18
P_{22}		TTL	Pin 31	Pin 19
P_{21}		TTL	Pin 30	Pin 20
P_{20}		TTL	Pin 29	Pin 21
P_{19}		TTL	Pin 28	Pin 22
P_{18}		TTL	Pin 27	Pin 23
P_{17}		TTL	Pin 26	Pin 24
P_{16}		TTL	Pin 25	Pin 25

Data Outputs (Cont.)

Name	Function	Value	J3 Package	C1, L1 Package
P_{15}		TTL	Pin 24	Pin 27
P_{14}		TTL	Pin 23	Pin 28
P_{13}		TTL	Pin 22	Pin 29
P_{12}		TTL	Pin 21	Pin 30
P_{11}		TTL	Pin 20	Pin 31
P_{10}		TTL	Pin 19	Pin 32
P_9		TTL	Pin 18	Pin 33
P_8		TTL	Pin 17	Pin 34
P_7		TTL	Pin 16	Pin 35
P_6		TTL	Pin 15	Pin 36
P_5		TTL	Pin 14	Pin 37
P_4		TTL	Pin 13	Pin 38
P_3		TTL	Pin 12	Pin 39
P_2		TTL	Pin 11	Pin 40
P_1		TTL	Pin 10	Pin 41
P_0	Product LSB	TTL	Pin 9	Pin 42

Clocks

The TMC216H has four clock lines, one for each input register and one for each product register. Data and two's complement instructions present at the inputs of these registers are loaded into the registers at the rising edge of the appropriate clock. The RND input is registered and clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with loading this control signal can be avoided by the use of normally LOW clocks.

Name	Function	Value	J3 Package	C1, L1 Package
CLK X	Clock Input Data X	TTL	Pin 53	Pin 64
CLK Y	Clock Input Data Y	TTL	Pin 8	Pin 44
CLK L	Clock LSP Register	TTL	Pin 7	Pin 45
CLK M	Clock MSP Register	TTL	Pin 41	Pin 8

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Controls

The TMC216H has seven control lines:

FT — Feedthrough. A control line which makes the output register transparent if it is HIGH.

TRIM, TRIL — Three-state enable lines for the MSP and the LSP. The output driver is in the high-impedance state when TRIM or TRIL is HIGH, and enabled when the appropriate control is LOW.

RS — Register Shift. RS is an output format control. A HIGH level on RS deletes the sign bit from the LSP and shifts the MSP down one bit. This is mandatory for unsigned magnitude, mixed mode, and two's complement integer operations.

RND — Round. When RND is HIGH, a one is added to the MSB of the LSP. Note that this bit depends on the state of the RS control. If RS is LOW when RND is HIGH, a one will be added to the 2^{-16} bit (P_{14}). If RS is HIGH when RND is HIGH, a one will be added to the 2^{-15} bit (P_{15}). In either case, the LSP output will reflect this addition when RND is HIGH. Note also that rounding always occurs in the positive direction; in some systems this may introduce a systematic bias.

TCX, TCY — Control how the device interprets data on the X and Y inputs. A HIGH on TCX or TCY forces the TMC216H to consider the appropriate input as a two's complement number, while a LOW forces the TMC216H to consider the appropriate input as a magnitude only number.

FT, RS, TRIM, and TRIL are not registered. The TCX input is registered, and clocked in at the rising edge of the X clock signal, CLK X. The TCY input is also registered, and clocked in at the rising edge of the Y clock signal, CLK Y. The RND input is registered, and clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with loading these control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J3 Package	C1, L1 Package
RND	Round Control Bit	TTL	Pin 52	Pin 65
TCX	X Input Two's Complement	TTL	Pin 51	Pin 66
TCY	Y Input Two's Complement	TTL	Pin 50	Pin 67
FT	Output Register Feedthrough	TTL	Pin 44	Pin 5
RS	Output Register Shift	TTL	Pin 43	Pin 6
TRIM	MSP Three-State Control	TTL	Pin 42	Pin 7
TRIL	LSP Three-State Control	TTL	Pin 6	Pin 46

No Connects

The contact and leaded versions of the TMC216H have four pins which are not connected internally. These should be left unconnected.

Name	Function	Value	J3 Package	C1, L1 Package
NC	No Connection	Open	None	Pins 9, 26, 43, 60

Figure 1. Fractional Two's Complement Notation

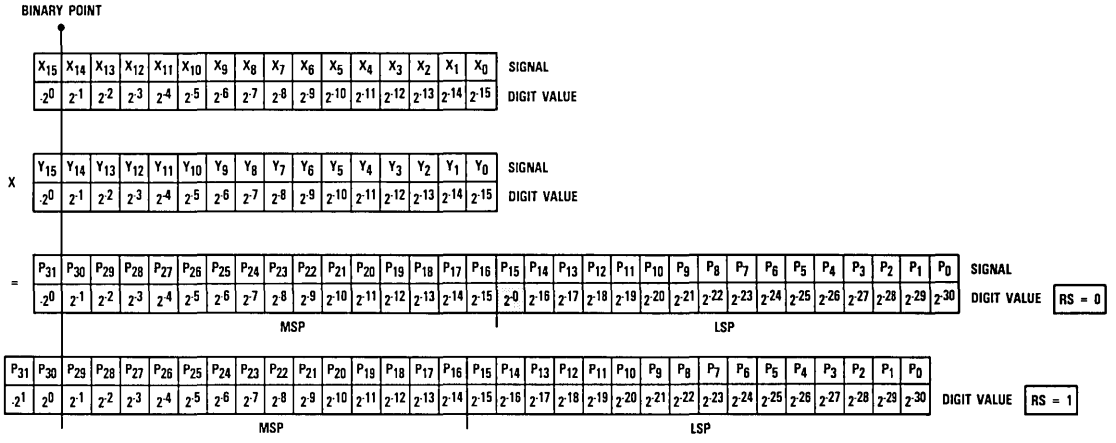

Figure 2. Fractional Unsigned Magnitude Notation

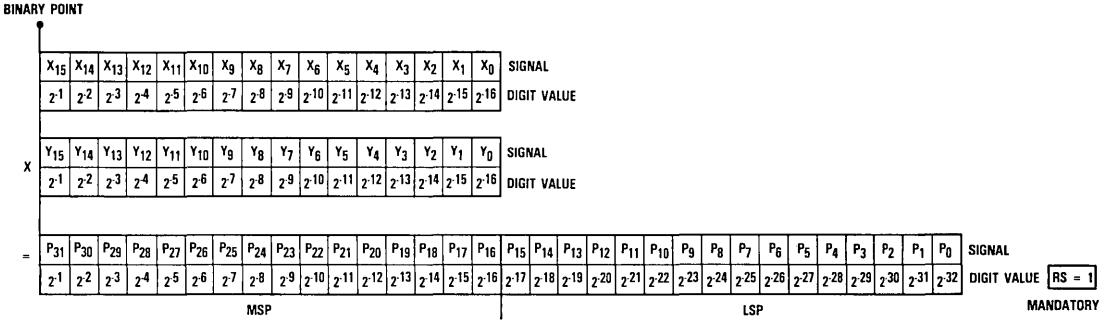

Figure 3. Fractional Mixed Notation

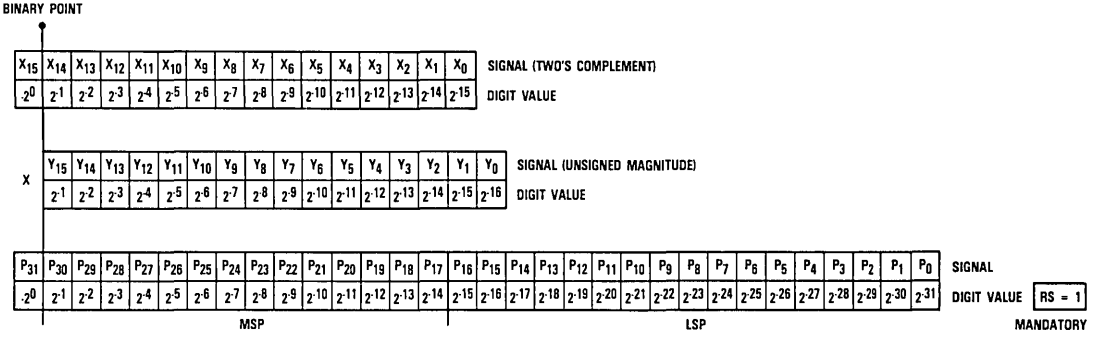

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Figure 4. Integer Two's Complement Notation

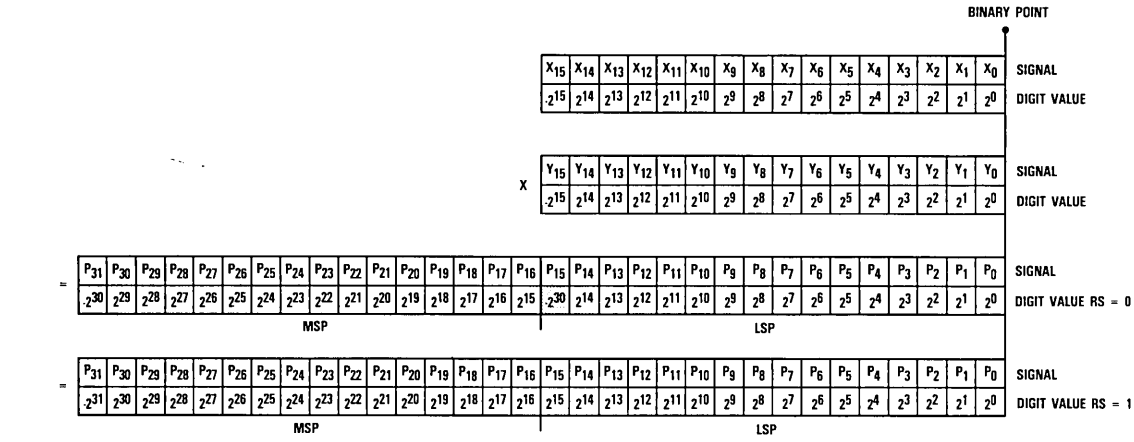

Figure 5. Integer Unsigned Magnitude Notation

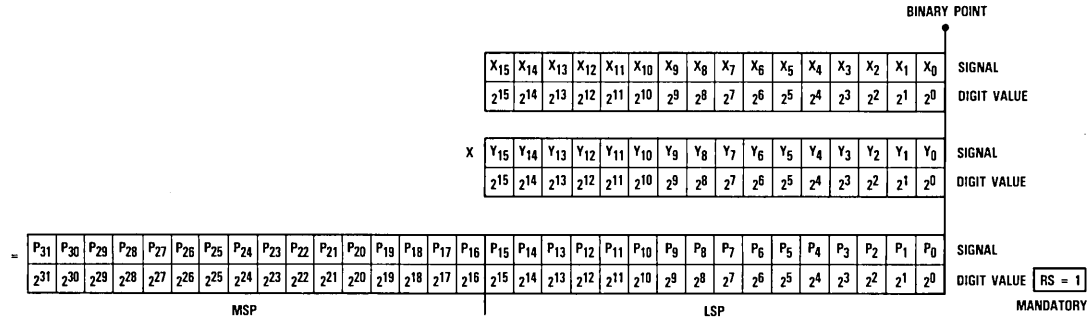

Figure 6. Integer Mixed Mode Notation

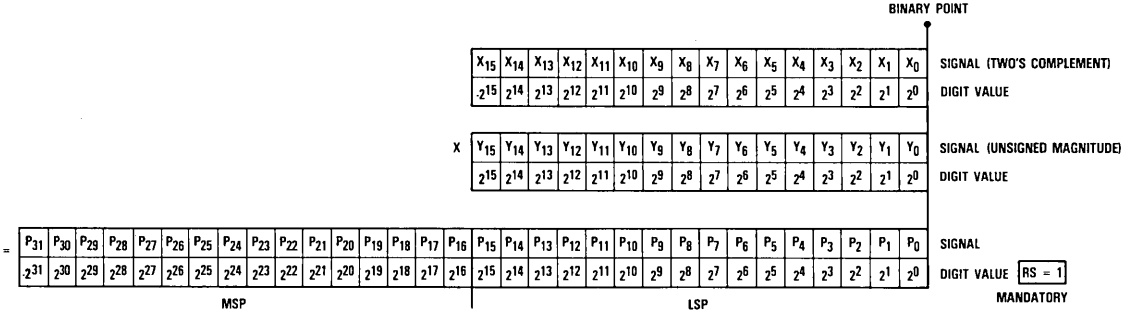

Figure 7. Timing Diagram, Clocked Mode

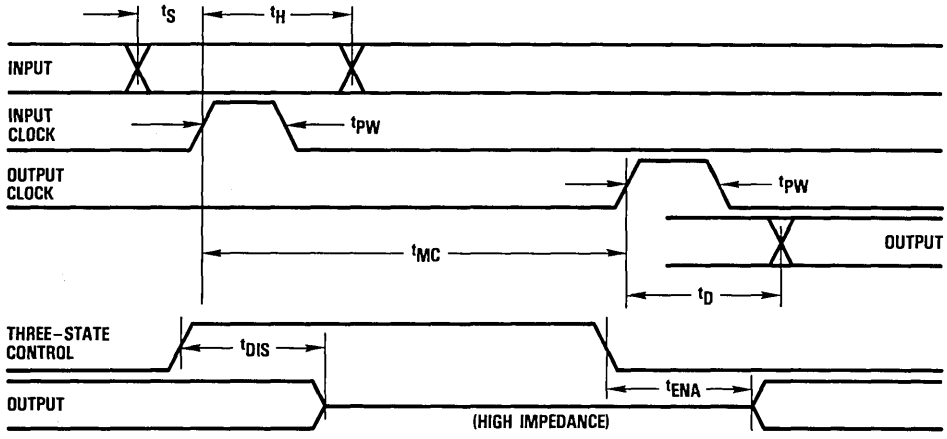

Figure 8. Timing Diagram, Unclocked Mode

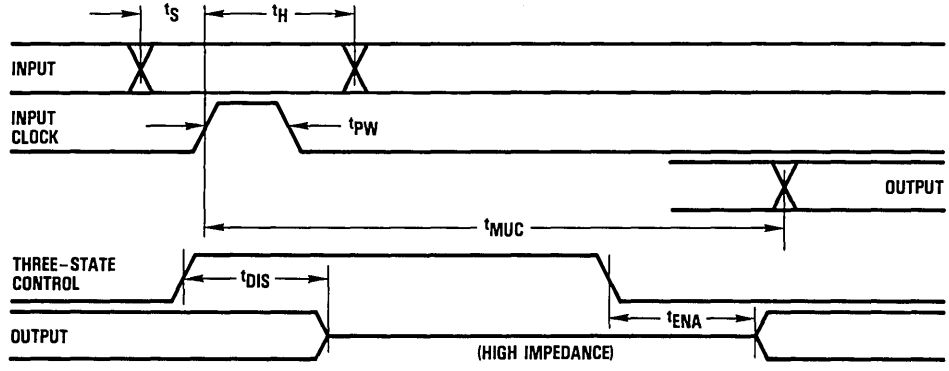

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Figure 9. Equivalent Input Circuit

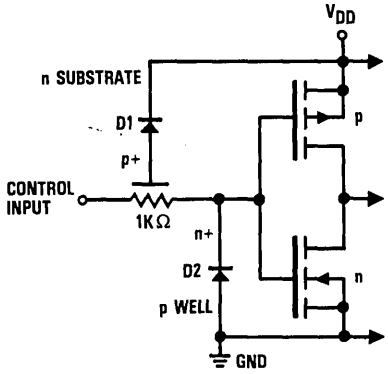


Figure 10. Equivalent Output Circuit

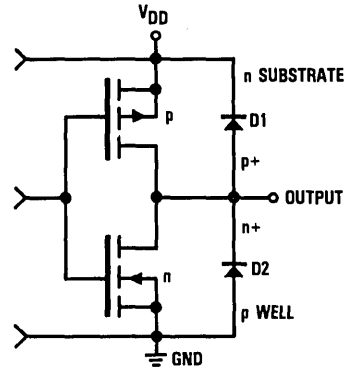


Figure 11. Test Load

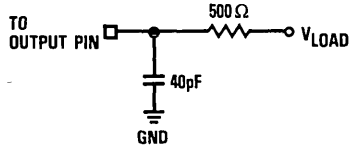
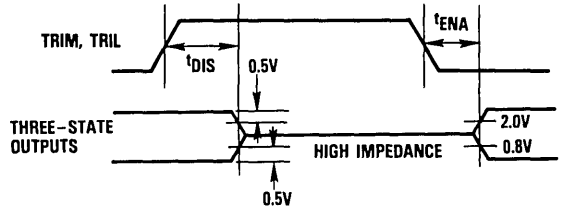


Figure 12. Transition Levels For Three-State Measurements



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} +0.5V)
Output	
Applied voltage	−0.5 to (V_{DD} +0.5V)[2]
Forced current	−1.0 to +6.0mA[3,4]
Short-circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PWL}	Clock Pulse Width, LOW	25			30			ns
t_{PWH}	Clock Pulse Width, HIGH	25			30			ns
t_S	Input Setup Time	25			30			ns
t_H	Input Hold Time	3			3			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		+125	°C

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Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
I_{DDQ}	Supply Current, Quiescent	V_{DD} = MAX, V_{IN} = 0V TRIM, TRIL = 5.0V		5		10	mA
I_{DDU}	Supply Current, Unloaded [1]	V_{DD} = MAX, F = 6.8MHz TRIM, TRIL = 5.0V		70		70	mA
I_{DDL}	Supply Current, Loaded [1, 2]	V_{DD} = MAX, F = 6.8MHz TRIM, TRIL = 0V Test Load: V_{LOAD} = V_{DD} MAX		180		180	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = MAX, V_I = 0.4V					
		X_{IN}, Controls, Clocks	−10	+10	−10	+10	μA
		Y_{IN}	−75	+75	−75	+75	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = MAX, V_I = 2.4V					
		X_{IN}, Controls, Clocks	−10	+10	−10	+10	μA
		Y_{IN}	−75	+75	−75	+75	μA
I_I	Input Current, Max Input Voltage	V_{DD} = MAX, V_I = V_{DD}		+75		+75	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = MIN, I_{OL} = MAX		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = MAX, V_I = 0.4V	−75	+75	−75	+75	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = MAX, V_I = 2.4V	−75	+75	−75	+75	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = MAX, Output HIGH, one pin to ground, one second duration max		−80		−80	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		10		10	pF

Notes:

1. Guaranteed to maximum clock rate, tested at 2MHz.
2. Worst case, all inputs and outputs toggling at maximum rate.

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
t_{MC}	Multiply Time, Clocked	V_{DD} = MIN		145		185	ns
t_{MUC}	Multiply Time, Unclocked	V_{DD} = MIN, Test Load: V_{LOAD} = 2.2V		185		230	ns
t_D	Output Delay	V_{DD} = MIN, Test Load: V_{LOAD} = 2.2V		40		45	ns
t_{ENA}	Three-State Output Enable Delay	V_{DD} = MIN, Test Load: V_{LOAD} = 1.5V		40		45	ns
t_{DIS}	Three-State Output Disable Delay	V_{DD} = MIN, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1} [2]		40		45	ns

Notes:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in figure 12.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

Application Notes

Mixed Mode Multiplication

There are several applications in which mixed mode multiplication may be advantageous. For example, inputs to a digital signal processor are often generated as unsigned magnitude numbers (e.g., data from an analog-to-digital converter). These numbers are effectively all positive values. In contrast, filter coefficients must often be negative. As a result, either the unsigned magnitude data must be converted to two's complement notation (which requires an additional bit), or the multiplier must be capable of mixed mode operation. The TMC216H provides this capability by independently specifying the mode of the multiplicand (X) and the multiplier (Y) on the TCX and TCY pins. No additional circuitry is required and the resulting product is in two's complement notation.

Multiplication by a Constant

Multiplication by a constant only requires that the constant be loaded into the desired input register, and that the selected register not be loaded again until a new constant is desired. The multiply cycle then consists simply of loading new data and strobing the output register.

Selection of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the TMC216H does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64.$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 6.

Register Shift (RS) Control

In two's complement notation, the acceptable range of values for a given word size is not the same for positive and negative numbers. The largest negative number is one LSB larger than the largest positive number. This is true for either fractional or integer notation. A problem can arise when the largest representable negative number is multiplied by itself. This should give a positive number of the same magnitude. However, the largest representable positive number is one LSB less than this value. As a result, this product cannot be correctly represented without using one additional output bit. The TMC216H has a Register Shift (RS) control that permits shifting of the result to provide a correct answer for every two's complement multiplication. When RS is active, the value of all bits in the MSP is doubled (i.e. shifted left one position), which provides the capability to represent the largest possible product. The MSB of the Least Significant Product is changed from a duplicate of the sign bit to the necessary bit to fill in the output word. The effects of this control are illustrated in Figures 1 and 4. Note that for unsigned magnitude operation, the RS control must be HIGH.

Output Register Transparent Mode

If the FT input is HIGH, the output register is made transparent: i.e., the product will appear at the output drivers as it is generated internally. The clock for the product register (CLK P) is not required in this mode of operation. The transparent mode is rarely used as it is much slower than the registered mode. It is essentially a special-purpose mode of operation.

Ordering Information[1]

Product Number	Temperature Range	Screening	Package	Package Marking
TMC216HJ3C	STD - T_A = 0°C to 70°C	Commercial	64 Lead DIP	216HJ3C
TMC216HJ3G	STD - T_A = 0°C to 70°C	Commercial With Burn-In	64 Lead DIP	216HJ3G
TMC216HJ3F	EXT - T_C = -55°C to 125°C	Commercial	64 Lead DIP	216HJ3F
TMC216HJ3A	EXT - T_C = -55°C to 125°C	High Reliability[2]	64 Lead DIP	216HJ3A
TMC216HC1C	STD - T_A = 0°C to 70°C	Commercial	68 Contact Chip Carrier	216HC1C
TMC216HC1G	STD - T_A = 0°C to 70°C	Commercial With Burn-In	68 Contact Chip Carrier	216HC1G
TMC216HC1F	EXT - T_C = -55°C to 125°C	Commercial	68 Contact Chip Carrier	216HC1F
TMC216HC1A	EXT - T_C = -55°C to 125°C	High Reliability[2]	68 Contact Chip Carrier	216HC1A
TMC216HL1C	STD - T_A = 0°C to 70°C	Commercial	68 Leaded Chip Carrier	216HL1C
TMC216HL1G	STD - T_A = 0°C to 70°C	Commercial With Burn-In	68 Leaded Chip Carrier	216HL1G
TMC216HL1F	EXT - T_C = -55°C to 125°C	Commercial	68 Leaded Chip Carrier	216HL1F
TMC216HL1A	EXT - T_C = -55°C to 125°C	High Reliability[2]	68 Leaded Chip Carrier	216HL1A

Notes:

1. Contact factory for availability.
2. Per TRW document 70Z01757.

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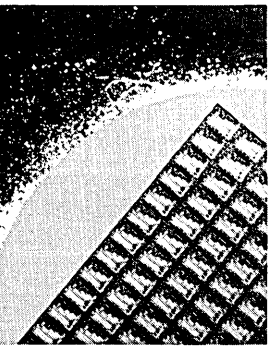
Preliminary Information describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact TRW for current information.

G

V L S I

D A T A

B O O K



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Application Notes And Reprints (Listings)

Multiplier-Accumulators

Multiplier-accumulators perform the sum of products operation found in most digital signal processing algorithms. TRW LSI offers a family of multiplier-accumulators in a variety of word sizes (8, 12, 16 bits) and speeds (100ns to 165ns multiply-accumulate time).

The multiplier-accumulator is an extension of the multiplier. The operation of addition/subtraction has been included, along with a feedback path for accumulation and a preload path for initializing the accumulator. With the accumulator adder embedded in the multiplier array, the product and sum are generated in only slightly more time than is required to derive the product alone. Clearing the accumulator is accomplished simultaneously with computation of the first product, and the accumulator may be disabled for operation as a multiplier. All TRW multiplier-accumulators are TTL compatible, and have full precision outputs (except as noted), plus three extended bits.

Multiplier-accumulators consist of three functional sections: an input section, the multiply-accumulate array, and the output section. The input section has two independently clocked n-bit input registers for the operands, comprised of positive-edge-triggered D-type flip-flops. Four mode controls (ACCumulate, SUBtract, RouND, and Two's Complement) are also registered.

The multiply-accumulate array is an asynchronous group of AND gates and adders which generates the product of the two input operands and, if desired, adds or subtracts the current contents of the product register (the result of the previous calculation). The ACCumulate control (ACC) determines whether the feedback path from the product register to the multiply-accumulate array is enabled. The SUBtract control (SUB) determines whether to add or subtract the product register contents from the new product. The input operands may be interpreted as two's complement or unsigned magnitude. User selectable rounding is available.

The output section includes the product registers and the three-state output ports. The product register receives the accumulated result from the multiply-accumulate array. Accumulation can generate word growth; in addition to the n-bit Most Significant Product (MSP) and the Least Significant Product (LSP), there is an additional three bits of eXTended Product (XTP) in the product register. The output pins are bidirectional ports through which the product register may be preloaded by coordinating the PRELoad control (PREL) with the three-state controls.

Bipolar Multiplier-Accumulators

The TDC1008, TDC1009, TDC1010 (8, 12 and 16 bits, respectively) and the TDC1043 (16 bits) are triple-diffused bipolar devices. The TDC1043 is similar to the TDC1010; however, there is no preload function, and the LSP, though internally used, is not output.

CMOS Multiplier-Accumulators

The TMC2009 (12-bit) and the TMC2010 (16-bit) devices are pin and function compatible with the TDC1009 and the TDC1010, respectively. They are fabricated using a two-micron CMOS process and operate at comparable speeds with reduced power consumption as compared to the bipolar devices. The TMC2110 (16-bit) multiplier-accumulator is fabricated using OMICRON-C™, TRW's state-of-the-art one-micron CMOS process. It is pin and function compatible with the industry standard TDC1010, yet operates at more than 50% greater speed.

Product	Size	Multiplication Time[1] (ns)	Power Dissipation[2] (Watts)	Package	Notes
TDC1008	8x8	100	2.4	J4, C1, L1	
TDC1009	12x12	135	3.9	J1, C1, L1	
TDC1010	16x16	165	5.8	J1, C1, L1	
TDC1043	16x16	100	1.2	J3, C1, L1	19-Bit Output
TMC2009	12x12	135	.32	J3, C1, L1	CMOS
TMC2010	16x16	160	.32	J3, C1, L1	CMOS
TMC2110	16x16	100	.53	J3, C1, L1	CMOS

Notes:

1. Guaranteed, Worst Case, T_A = 0°C to 70°C.
2. Bipolar: Worst Case, T_A = 0°C to 70°C.
   CMOS: All inputs toggling at MAX clock rate, unloaded. T_A = 0°C to 70°C.

TDC1008

VLSI Multiplier–Accumulator
8 X 8 bit, 100ns

The TDC1008 is a high-speed 8 x 8 bit parallel multiplier-accumulator which operates at a 100 nanosecond cycle time (10MHz multiply-accumulate rate). The input data may be specified as two's complement or unsigned magnitude, yielding a full-precision 16-bit product. Products may be accumulated to a 19-bit result.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The result is divided into a 3-bit eXTended Product (XTP), an 8-bit Most Significant Product (MSP), and an 8-bit Least Significant Product (LSP). Individual three-state output ports are provided for the XTP, LSP and MSP. The output register can be preloaded directly via the output ports.

Built with TRW's 2-micron bipolar process, the TDC1008 is a uniquely powerful LSI signal processing device.

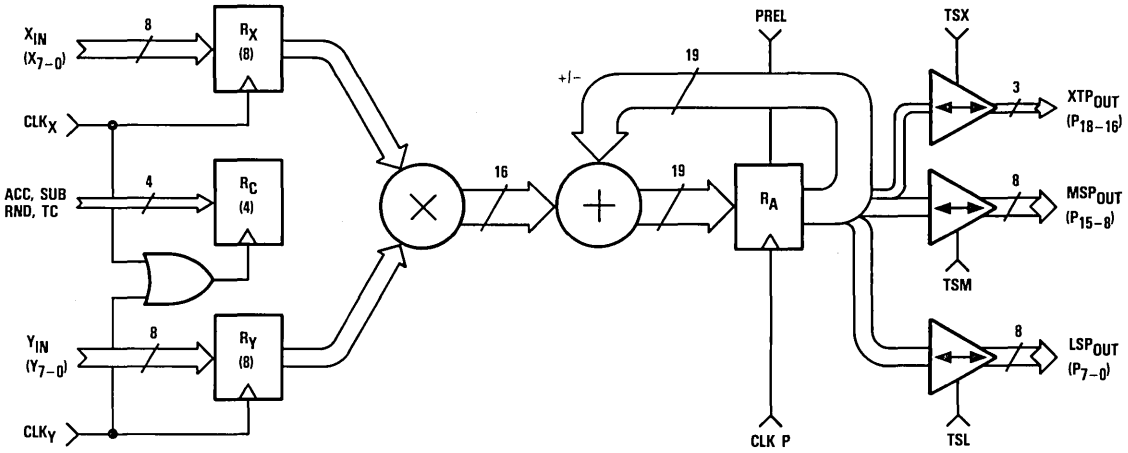
Features

- 100ns Multiply-Accumulate Time (Worst Case)
- 8 x 8 Bit Parallel Multiplication With Accumulation To 19-Bit Result
- Selectable Accumulation, Subtraction, Rounding, And Preloading
- All Inputs And Outputs Are Registered TTL Compatible
- Three-State Outputs
- Two's Complement Or Unsigned Magnitude Operation
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In 48 Lead Ceramic DIP, 68 Contact Chip Carrier, Or Leaded Chip Carrier

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



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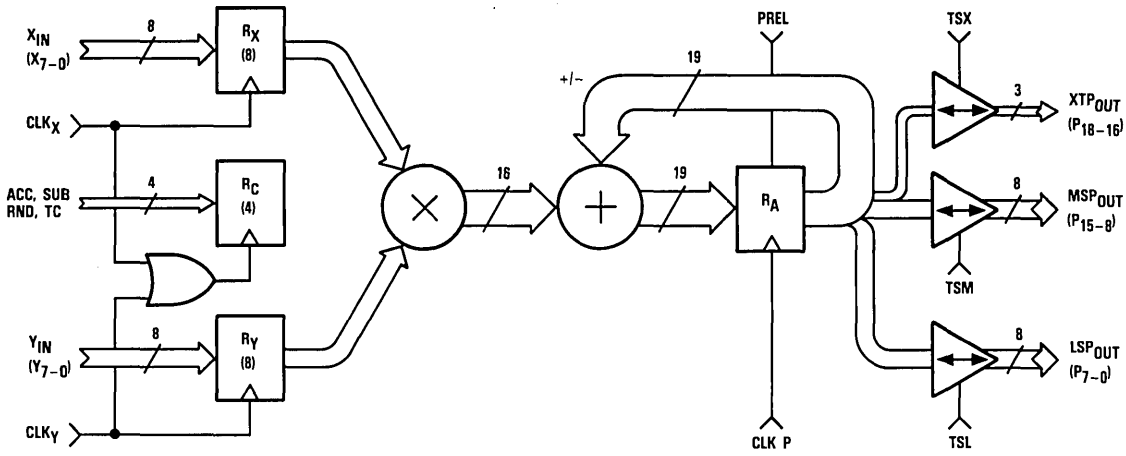
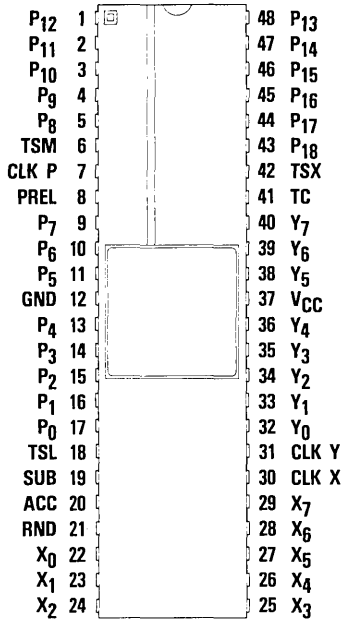
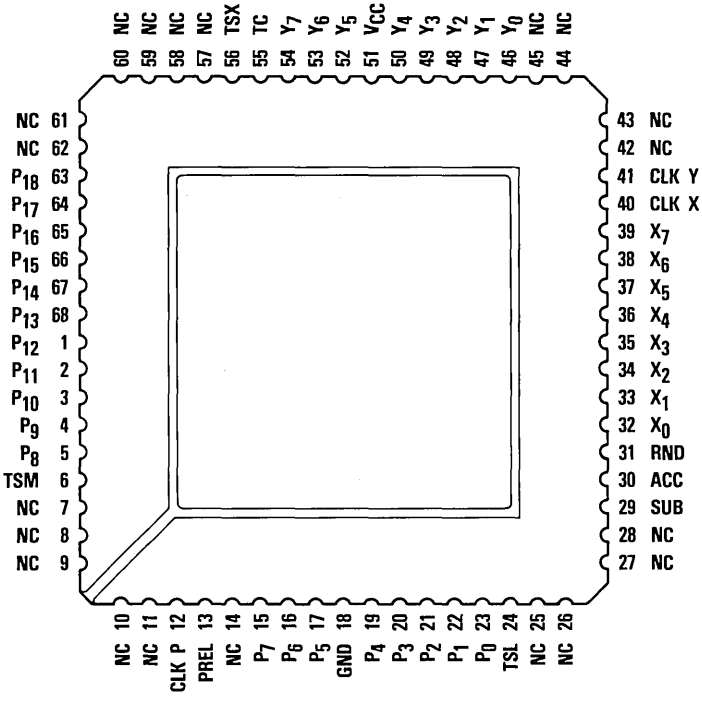
Functional Block Diagram



Pin Assignments



48 Lead DIP – J4 Package



68 Contact Or Leaded Chip Carrier – C1, L1 Package

Functional Description

General Information

The TDC1008 consists of four functional sections: Input registers, an asynchronous multiplier array, an adder, and output registers. The input registers store the two 8-bit numbers which are to be multiplied, and the control lines which control the input numerical format (two's complement or unsigned magnitude), output rounding, accumulation, and subtraction. The round control is used when a single-word output is desired. Each input is independently stored, simplifying multiplication by a constant. The output registers can be preloaded with a constant to provide the sum of products plus a constant. The asynchronous multiplier array is a network of AND gates and adders, which has been designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 8-bit words and one 3-bit word: the Most Significant Product (MSP), the Least Significant Product (LSP), and the eXTended Product (XTP). Three-state output drivers permit the TDC1008 to be used on a bus, or allow the outputs to be multiplexed over the same 8-bit output lines.

Power

The TDC1008 operates from a single +5 Volt supply. All power and ground lines must be connected.

Name	Function	Value	J4 Package	C1, L1 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pin 37	Pin 51
GND	Ground	0.0V	Pin 12	Pin 18

Data Inputs

The TDC1008 has two 8-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_7 and Y_7, carry the sign information for the two's complement notation. The remaining bits are denoted X_0 through X_6 and Y_0 through Y_6 (with X_0 and Y_0 the Least Significant Bits). Data present at the X and Y inputs are clocked into the input registers at the rising edge of the appropriate clock. The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

Name	Function	Value	J4 Package	C1, L1 Package
X_7	X Data MSB	TTL	Pin 29	Pin 39
X_6		TTL	Pin 28	Pin 38
X_5		TTL	Pin 27	Pin 37
X_4		TTL	Pin 26	Pin 36
X_3		TTL	Pin 25	Pin 35
X_2		TTL	Pin 24	Pin 34
X_1		TTL	Pin 23	Pin 33
X_0	X Data LSB	TTL	Pin 22	Pin 32
Y_7	Y Data MSB	TTL	Pin 40	Pin 54
Y_6		TTL	Pin 39	Pin 53
Y_5		TTL	Pin 38	Pin 52
Y_4		TTL	Pin 36	Pin 50
Y_3		TTL	Pin 35	Pin 49
Y_2		TTL	Pin 34	Pin 48
Y_1		TTL	Pin 33	Pin 47
Y_0	Y Data LSB	TTL	Pin 32	Pin 46

Data Outputs

The TDC1008 has a 19-bit two's complement or unsigned magnitude result that is the sum of the products of the two input data values and the previous products which have been accumulated. The output is divided into two 8-bit output words, the Most Significant Product (MSP) and Least Significant Product (LSP), and one 3-bit output word, the eXTended Product (XTP). The Most Significant Bit (MSB) of the XTP is the sign bit if two's complement notation is used. The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

Name	Function	Value	J4 Package	C1, L1 Package
P_{18}	Product MSB	TTL	Pin 43	Pin 63
P_{17}		TTL	Pin 44	Pin 64
P_{16}		TTL	Pin 45	Pin 65
P_{15}		TTL	Pin 46	Pin 66
P_{14}		TTL	Pin 47	Pin 67
P_{13}		TTL	Pin 48	Pin 68
P_{12}		TTL	Pin 1	Pin 1
P_{11}		TTL	Pin 2	Pin 2
P_{10}		TTL	Pin 3	Pin 3
P_9		TTL	Pin 4	Pin 4
P_8		TTL	Pin 5	Pin 5
P_7		TTL	Pin 9	Pin 15
P_6		TTL	Pin 10	Pin 16
P_5		TTL	Pin 11	Pin 17
P_4		TTL	Pin 13	Pin 19
P_3		TTL	Pin 14	Pin 20
P_2		TTL	Pin 15	Pin 21
P_1		TTL	Pin 16	Pin 22
P_0	Product LSB	TTL	Pin 17	Pin 23

Clocks

The TDC1008 has three clock lines, one for each of the input registers and one for the product register. Data present at the inputs of these registers is loaded into the registers at the rising edge of the appropriate clock. The RouND (RND), Two's Complement (TC), ACCumulate (ACC), and SUBtract (SUB) inputs are registered, with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J4 Package	C1, LI Package
CLK X	Clock Input Data X	TTL	Pin 30	Pin 40
CLK Y	Clock Input Data Y	TTL	Pin 31	Pin 41
CLK P	Clock Product Register	TTL	Pin 7	Pin 12

Controls

The TDC1008 has eight control lines. TSX, TSM, and TSL are three-state enable lines for the XTP, the MSP, and the LSP respectively. The output driver is in the high-impedance state when TSX, TSM, or TSL is HIGH, and enabled when the appropriate control is LOW, and PRELoad is LOW.

PRELoad (PREL) is an active-HIGH control which has several effects when active (see Table 1). First, all output buffers are forced into the high-impedance state. Second, when any or all of TSX, TSM, and TSL are also HIGH, external data present at the output pins will be preloaded into the corresponding section of the output register on the rising edge of CLK P. Normal data setup and hold times apply both to the logical AND of PREL and the relevant three-state control (TSX, TSM, TSL), and to the data being preloaded. These setup and hold times are with respect to the rising edge of CLK P.

RouND (RND) controls the addition of a 1 to the MSB of the LSP for rounding. When RND is HIGH, a 1 is added to the MSB of the LSP for rounding the product in the MSP and XTP (if appropriate) rather than truncating it.

Two's Complement (TC) controls how the device interprets data on the X and Y inputs. TC HIGH makes both inputs two's complement inputs, while TC LOW makes both inputs unsigned magnitude only inputs.

When ACCumulate (ACC) is HIGH, the content of the output register is added to or subtracted from the next product generated, and their sum is stored back into the output registers at the next rising edge of CLK P. When ACC is LOW, multiplication without accumulation is performed, and the next product generated is stored into the output registers directly. This operation is used for the first term in a summation to avoid a separate "clear" operation.

The SUBtract (SUB) control is used in conjunction with the ACC control. When both the ACC and SUB controls are HIGH, the content of the output register is subtracted from the next product generated and the difference is stored back into the output register. Note that the previous output is subtracted from the product, not the product from the previous output.

The RND, TC, ACC, and SUB inputs are registered, with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J4 Package	C1, LI Package
TSX	XTP Three-State Control	TTL	Pin 42	Pin 56
TSM	MSP Three-State Control	TTL	Pin 6	Pin 6
TSL	LSP Three-State Control	TTL	Pin 18	Pin 24
PREL	Preload Control	TTL	Pin 8	Pin 13
RND	Round Control Bit	TTL	Pin 21	Pin 31
TC	Two's Complement Control	TTL	Pin 41	Pin 55
ACC	Accumulate Control	TTL	Pin 20	Pin 30
SUB	Subtract Control	TTL	Pin 19	Pin 29

H

Preload Truth Table 1

PREL[1]	TSX[1]	TSM[1]	TSL[1]	XTP	MSP	LSP
L	L	L	L	Register→ Output pin	Register→ Output pin	Register→ Output pin
L	L	L	H	Register→ Output pin	Register→ Output pin	Hi-Z
L	L	H	L	Register→ Output pin	Hi-Z	Register→ Output pin
L	L	H	H	Register→ Output pin	Hi-Z	Hi-Z
L	H	L	L	Hi-Z	Register→ Output pin	Register→ Output pin
L	H	L	H	Hi-Z	Register→ Output pin	Hi-Z
L	H	H	L	Hi-Z	Hi-Z	Register→ Output pin
L	H	H	H	Hi-Z	Hi-Z	Hi-Z
H[2]	L	L	L	Hi-Z	Hi-Z	Hi-Z
H[2]	L	L	H	Hi-Z	Hi-Z	Hi-Z Preload
H[2]	L	H	L	Hi-Z	Hi-Z Preload	Hi-Z
H[2]	L	H	H	Hi-Z	Hi-Z Preload	Hi-Z Preload
H[2]	H	L	L	Hi-Z Preload	Hi-Z	Hi-Z
H[2]	H	L	H	Hi-Z Preload	Hi-Z	Hi-Z Preload
H[2]	H	H	L	Hi-Z Preload	Hi-Z Preload	Hi-Z
H[2]	H	H	H	Hi-Z Preload	Hi-Z Preload	Hi-Z Preload

Notes:

1. PREL, TSX, TSM, and TSL are not registered.
2. PREL Hi inhibits any change of output register for those outputs in which the three-state control is LOW.

Figure 1. Fractional Two's Complement Notation

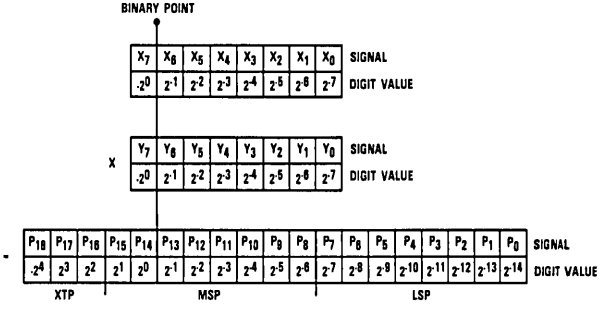


Figure 2. Fractional Unsigned Magnitude Notation

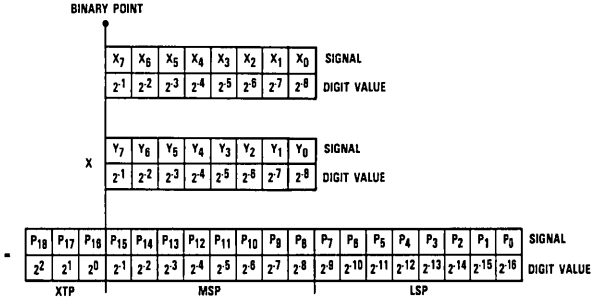


Figure 3. Integer Two's Complement Notation

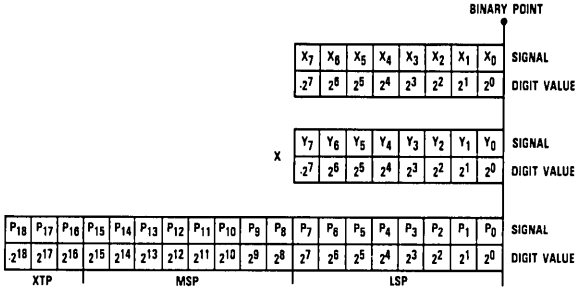
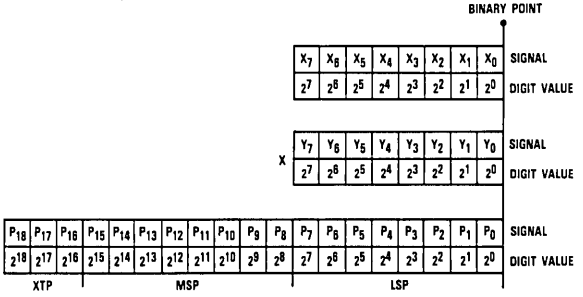


Figure 4. Integer Unsigned Magnitude Notation



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−6.0 to + 6.0mA
Output	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−1.0 to +6.0mA [3,4]
Short-circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, case	−55 to +125°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PW}	Clock Pulse Width	25			30			ns
t_S	Input Setup Time (Except PREL)	25			30			ns
t_S	Input Setup Time (PREL)	40			45			ns
t_H	Input Hold Time	0			3			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		+125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = MAX, Static[1]		450		525	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V					
		Data, Registered Controls		-0.4		-0.4	mA
		Clocks, Unregistered Controls		-1.0		-1.0	mA
		CLK P		-2.0		-2.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V					
		Data, Registered Controls		75		100	μA
		Clocks, Unregistered Controls		75		100	μA
		CLK P		150		200	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{CC} = MAX, V_I = 0.4V		-400		-400	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{CC} = MAX, V_I = 2.4V		75		100	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = MAX, Output HIGH, one pin to ground, one second duration		-50		-50	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		10		10	pF

Note:

1. Worst case, all inputs and outputs LOW.

Switching characteristics within specified operating conditions[1]

Parameter		Test Conditions	*Temperature Range*				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MA}	Multiply-Accumulate Time	V_{CC} = MIN		100		125	ns
t_D	Output Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V		40		45	ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 1.8V		40		45	ns
t_{DIS}	Three-State Output Disable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1}[2]		40		45	ns

Notes:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in Figure 9.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

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Figure 5. Timing Diagram

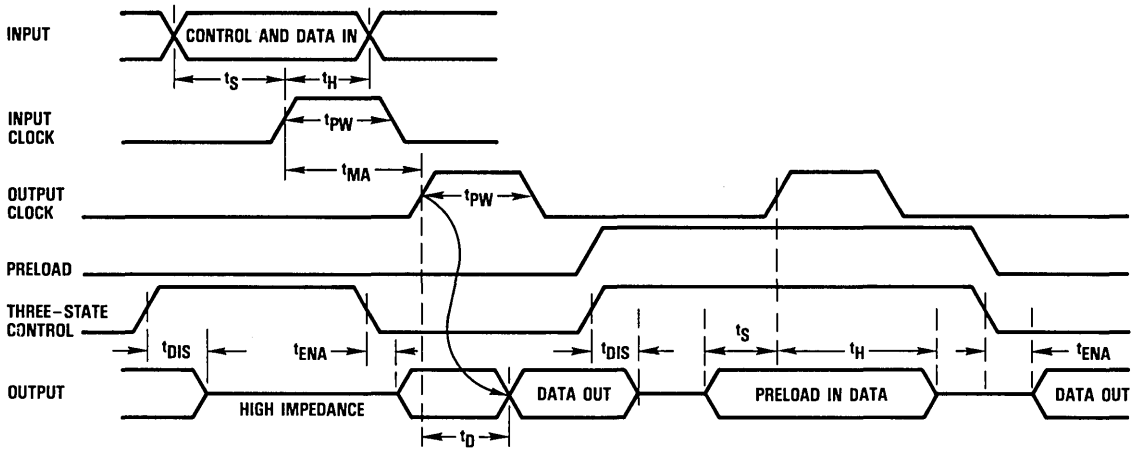
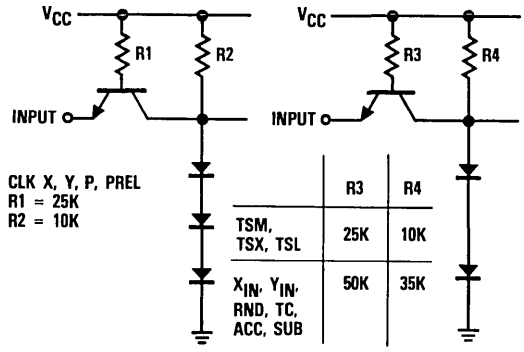


Figure 6. Equivalent Input Circuit



	R3	R4
TSM, TSX, TSL	25K	10K
X_{IN}, Y_{IN}, RND, TC, ACC, SUB	50K	35K

Figure 7. Equivalent Output Circuit

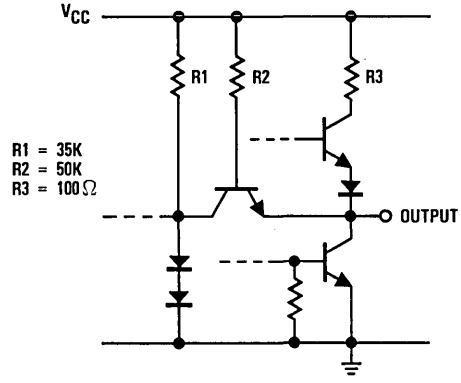


Figure 8. Test Load

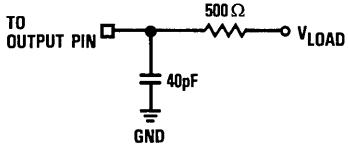
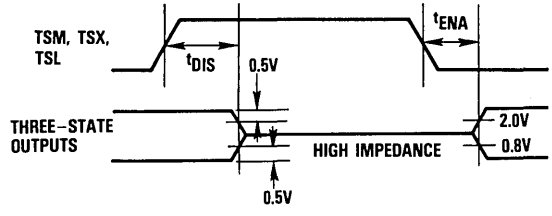


Figure 9. Transition Levels For Three-State Measurements



Application Notes

Multiplication by a Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and the desired register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the TDC1008 does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 4.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1008J4C	STD-T_A = 0°C to 70°C	Commercial	48 Lead DIP	1008J4C
TDC1008J4G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	48 Lead DIP	1008J4G
TDC1008J4F	EXT-T_C = -55°C to 125°C	Commercial	48 Lead DIP	1008J4F
TDC1008J4A	EXT-T_C = -55°C to 125°C	High Reliability[2]	48 Lead DIP	1008J4A
TDC1008C1F	EXT-T_C = -55°C to 125°C	Commercial	68 Contact Chip Carrier	1008C1F
TDC1008C1A	EXT-T_C = -55°C to 125°C	High Reliability[2]	68 Contact Chip Carrier	1008C1A
TDC1008L1F[1]	EXT-T_C = -55°C to 125°C	Commercial	68 Leaded Chip Carrier	1008L1F
TDC1008L1A[1]	EXT-T_C = -55°C to 125°C	High Reliability[2]	68 Leaded Chip Carrier	1008L1A

Notes:

1. Contact factory for availability.
2. Per TRW document 70Z1757.

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TDC1009

VLSI Multiplier–Accumulator
12 X 12 bit, 135ns

The TDC1009 is a high-speed 12 x 12 bit parallel multiplier-accumulator which operates at a 135 nanosecond cycle time (7.4MHz multiply-accumulate rate). The input data may be specified as two's complement or unsigned magnitude, yielding a full-precision 24-bit product. Products may be accumulated to a 27-bit result.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The result is divided into a 3-bit eXTended Product (XTP), a 12-bit Most Significant Product (MSP), and a 12-bit Least Significant Product (LSP). Individual three-state output ports are provided for the XTP, the MSP, and the LSP. The output register can be preloaded directly via the output ports.

Built with TRW's 2-micron bipolar process, the TDC1009 is a uniquely powerful LSI signal processing device.

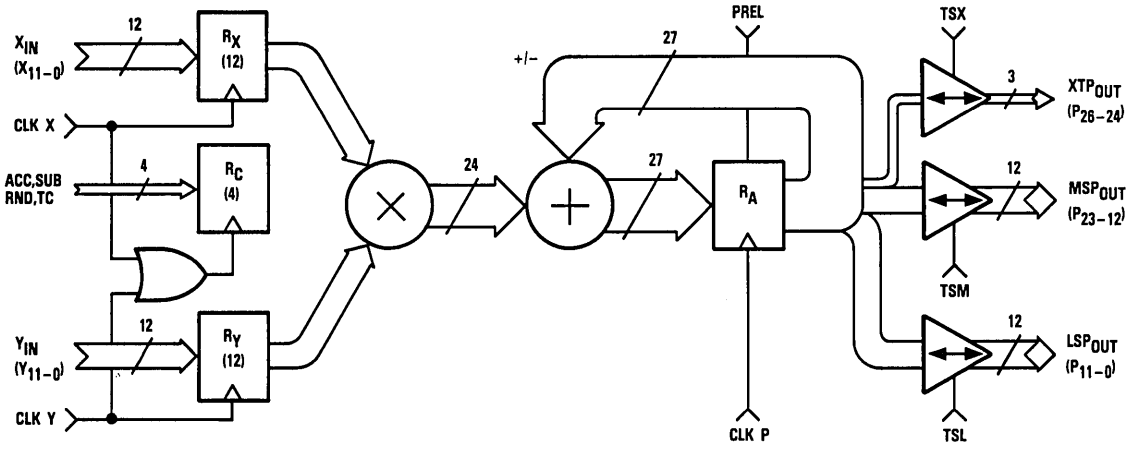
Features

- 135ns Multiply-Accumulate Time (Worst Case)
- 12 x 12 Bit Parallel Multiplication With Accumulation To 27-Bit Result
- Selectable Accumulation, Subtraction, Rounding, And Preloading
- All Inputs And Outputs Are Registered TTL Compatible
- Three-State Output
- Two's Complement Or Unsigned Magnitude Operation
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In 64 Lead Ceramic DIP, 68 Contact Chip Carrier, Or 68 Leaded Chip Carrier

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



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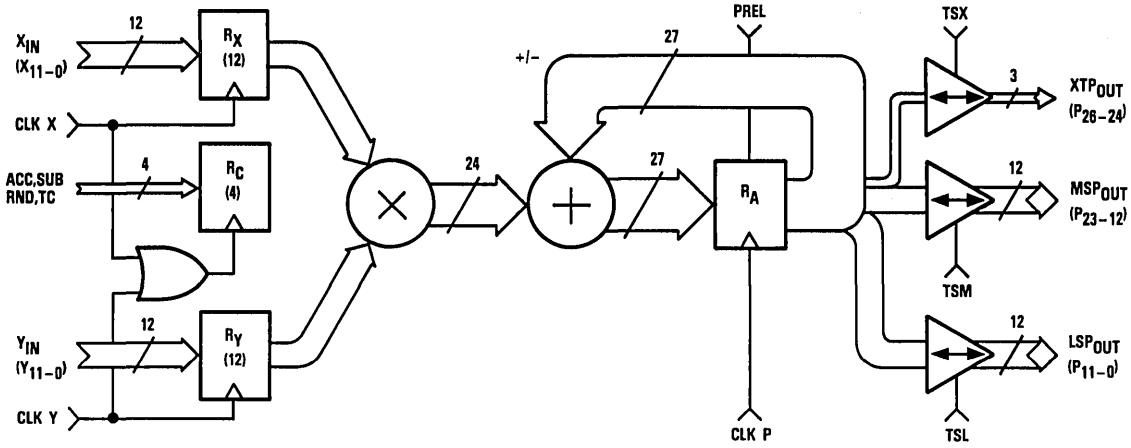
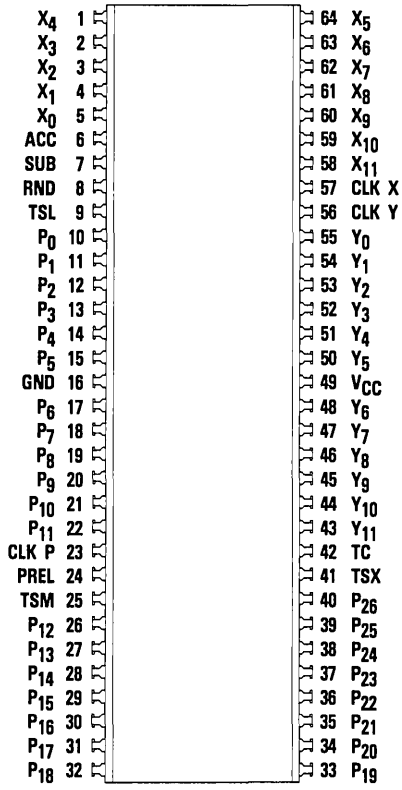
Functional Block Diagram

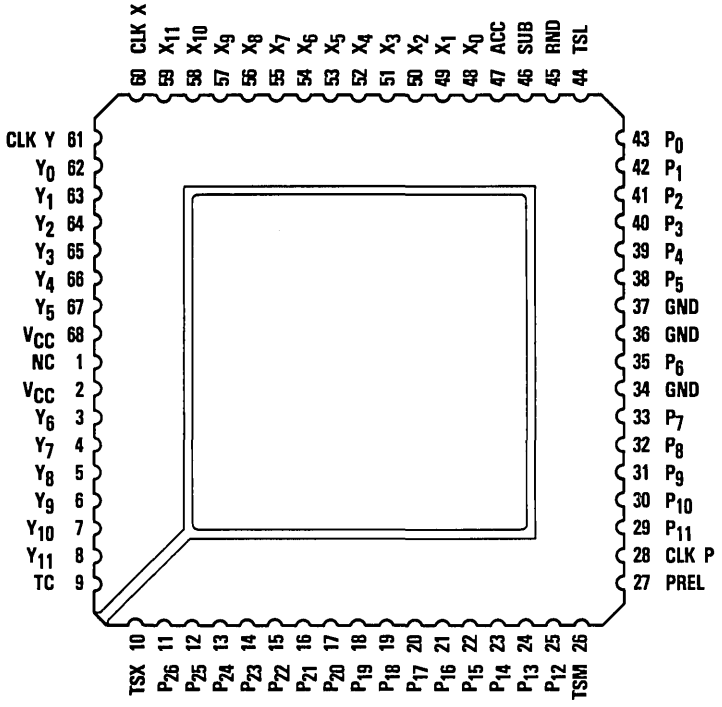


Pin Assignments



64 Lead DIP – J1 Package

Pin Assignments



68 Contact or Leaded Chip Carrier – C1, L1 Package

Functional Description

General Information

The TDC1009 consists of four functional sections: Input registers, an asynchronous multiplier array, an adder, and output registers. The input registers store the two 12-bit numbers which are to be multiplied, and the control lines which control the input numerical format (two's complement or unsigned magnitude), output rounding, accumulation, and subtraction. The round control is used when a single-word output is desired. Each input is independently stored, simplifying multiplication by a constant. The output registers can be preloaded with a constant to provide the sum of products plus a constant. The asynchronous multiplier array is a network of AND gates and adders, which has been designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 12-bit words and one 3-bit word: the Most Significant Product (MSP), the Least Significant Product (LSP), and the eXTended Product (XTP). Three-state output drivers permit the TDC1009 to be used on a bus, or allow the outputs to be multiplexed over the same 12-bit output lines.

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Power

The TDC1009 operates from a single +5 Volt supply. All power and ground lines must be connected.

Name	Function	Value	J1 Package	C1, LI Package
V_{CC}	Positive Supply Voltage	+5.0V	Pin 49	Pins 68, 2
GND	Ground	0.0V	Pin 16	Pins 34, 36, 37

Data Inputs

The TDC1009 has two 12-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_{11} and Y_{11}, carry the sign information for the two's complement notation. The remaining bits are denoted X_0 through X_{10} and Y_0 through Y_{10} (with X_0 and Y_0 the Least Significant Bits). Data present at the X and Y inputs are clocked into the input registers at the rising edge of the appropriate clock. The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

Name	Function	Value	J1 Package	C1, LI Package
X_{11}	X Data MSB	TTL	Pin 58	Pin 59
X_{10}		TTL	Pin 59	Pin 58
X_9		TTL	Pin 60	Pin 57
X_8		TTL	Pin 61	Pin 56
X_7		TTL	Pin 62	Pin 55
X_6		TTL	Pin 63	Pin 54
X_5		TTL	Pin 64	Pin 53
X_4		TTL	Pin 1	Pin 52
X_3		TTL	Pin 2	Pin 51
X_2		TTL	Pin 3	Pin 50
X_1		TTL	Pin 4	Pin 49
X_0	X Data LSB	TTL	Pin 5	Pin 48
Y_{11}	Y Data MSB	TTL	Pin 43	Pin 8
Y_{10}		TTL	Pin 44	Pin 7
Y_9		TTL	Pin 45	Pin 6
Y_8		TTL	Pin 46	Pin 5
Y_7		TTL	Pin 47	Pin 4
Y_6		TTL	Pin 48	Pin 3
Y_5		TTL	Pin 50	Pin 67
Y_4		TTL	Pin 51	Pin 66
Y_3		TTL	Pin 52	Pin 65
Y_2		TTL	Pin 53	Pin 64
Y_1		TTL	Pin 54	Pin 63
Y_0	Y Data LSB	TTL	Pin 55	Pin 62

Data Outputs

The TDC1009 has a 27-bit two's complement or unsigned magnitude result that is the sum of the products of the two input data values and the previous products which have been accumulated. The output is divided into two 12-bit output words, the Most Significant Product (MSP) and Least Significant Product (LSP), and one 3-bit output word, the eXTended Product (XTP). The Most Significant Bit (MSB) of the MSP is the sign bit if two's complement notation is used. The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

Name	Function	Value	J1 Package	C1, LI Package
P_{26}	Product MSB	TTL	Pin 40	Pin 11
P_{25}		TTL	Pin 39	Pin 12
P_{24}		TTL	Pin 38	Pin 13
P_{23}		TTL	Pin 37	Pin 14
P_{22}		TTL	Pin 36	Pin 15
P_{21}		TTL	Pin 35	Pin 16

Data Outputs (Cont.)

Name	Function	Value	J1 Package	C1, LI Package
P_{20}		TTL	Pin 34	Pin 17
P_{19}		TTL	Pin 33	Pin 18
P_{18}		TTL	Pin 32	Pin 19
P_{17}		TTL	Pin 31	Pin 20
P_{16}		TTL	Pin 30	Pin 21
P_{15}		TTL	Pin 29	Pin 22
P_{14}		TTL	Pin 28	Pin 23
P_{13}		TTL	Pin 27	Pin 24
P_{12}		TTL	Pin 26	Pin 25
P_{11}		TTL	Pin 22	Pin 29
P_{10}		TTL	Pin 21	Pin 30
P_9		TTL	Pin 20	Pin 31
P_8		TTL	Pin 19	Pin 32
P_7		TTL	Pin 18	Pin 33
P_6		TTL	Pin 17	Pin 35
P_5		TTL	Pin 15	Pin 38
P_4		TTL	Pin 14	Pin 39
P_3		TTL	Pin 13	Pin 40
P_2		TTL	Pin 12	Pin 41
P_1		TTL	Pin 11	Pin 42
P_0	Product LSB	TTL	Pin 10	Pin 43

Clocks

The TDC1009 has three clock lines, one for each of the input registers and one for the product register. Data present at the inputs of these registers is loaded into the registers at the rising edge of the appropriate clock. The RouND (RND), Two's Complement (TC), ACCumulate (ACC), and SUBtract (SUB) inputs are registered, with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J1 Package	C1, LI Package
CLK X	Clock Input Data X	TTL	Pin 57	Pin 60
CLK Y	Clock Input Data Y	TTL	Pin 56	Pin 61
CLK P	Clock Product Register	TTL	Pin 23	Pin 28

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Controls

The TDC1009 has eight control lines. TSX, TSM, and TSL are three-state enable lines for the XTP, the MSP, and the LSP respectively. The output driver is in the high-impedance state when TSX, TSM, or TSL is HIGH, and enabled when the appropriate control is LOW.

PRELoad (PREL) is an active-HIGH control which has several effects when active (see Table 1). First, all output buffers are forced into the high-impedance state. Second, when any or all of TSX, TSM, and TSL are also HIGH, external data present at the output pins will be preloaded into the corresponding section of the output register on the rising edge of CLK P. Normal data setup and hold times apply both to the logical AND of PREL and the relevant three-state control (TSX, TSM, TSL), and to the data being preloaded. These setup and hold times are with respect to the rising edge of CLK P.

Controls (Cont.)

RouND (RND) controls the addition of a 1 to the MSB of the LSP for rounding. When RND is HIGH, a 1 is added to the MSB of the LSP for rounding the product in the MSP and XTP (if appropriate) rather than truncating it.

Two's Complement (TC) controls how the device interprets data on the X and Y inputs. TC HIGH makes both inputs two's complement inputs, while TC LOW makes both inputs unsigned magnitude only inputs.

When ACCumulate (ACC) is HIGH, the content of the output register is added to or subtracted from the next product generated, and their sum is stored back into the output registers at the next rising edge of CLK P. When ACC is LOW, multiplication without accumulation is performed, and the next product generated is stored into the output registers directly.

This operation is used for the first term in a summation to avoid a separate "clear" operation.

The SUBtract (SUB) control is used in conjunction with the ACC control. When both the ACC and SUB controls are HIGH, the content of the output register is subtracted from the next product generated and the difference is stored back into the output register. Note that the previous output is subtracted from the product, not the product from the previous output.

The RND, TC, ACC, and SUB inputs are registered, with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J1 Package	C1, LI Package
TSX	XTP Three-State Control	TTL	Pin 41	Pin 10
TSM	MSP Three-State Control	TTL	Pin 25	Pin 26
TSL	LSP Three-State Control	TTL	Pin 9	Pin 44
PREL	Preload Control	TTL	Pin 2	Pin 27
RND	Round Control Bit	TTL	Pin 8	Pin 45
TC	Two's Complement Control	TTL	Pin 42	Pin 9
ACC	Accumulate Control	TTL	Pin 6	Pin 47
SUB	Subtract Control	TTL	Pin 7	Pin 46

Preload Truth Table 1

PREL[1]	TSX[1]	TSM[1]	TSL[1]	XTP	MSP	LSP
L	L	L	L	Register→ Output pin	Register→ Output pin	Register→ Output pin
L	L	L	H	Register→ Output pin	Register→ Output pin	Hi-Z
L	L	H	L	Register→ Output pin	Hi-Z	Register→ Output pin
L	L	H	H	Register→ Output pin	Hi-Z	Hi-Z
L	H	L	L	Hi-Z	Register→ Output pin	Register→ Output pin
L	H	L	H	Hi-Z	Register→ Output pin	Hi-Z
L	H	H	L	Hi-Z	Hi-Z	Register→ Output pin
L	H	H	H	Hi-Z	Hi-Z	Hi-Z
H[2]	L	L	L	Hi-Z	Hi-Z	Hi-Z
H[2]	L	L	H	Hi-Z	Hi-Z	Hi-Z Preload
H[2]	L	H	L	Hi-Z	Hi-Z Preload	Hi-Z
H[2]	L	H	H	Hi-Z	Hi-Z Preload	Hi-Z Preload
H[2]	H	L	L	Hi-Z Preload	Hi-Z	Hi-Z
H[2]	H	L	H	Hi-Z Preload	Hi-Z	Hi-Z Preload
H[2]	H	H	L	Hi-Z Preload	Hi-Z Preload	Hi-Z
H[2]	H	H	H	Hi-Z Preload	Hi-Z Preload	Hi-Z Preload

Notes:

1. PREL, TSX, TSM, and TSL are not registered.
2. PREL Hi inhibits any change of output register for those outputs in which the three-state control is LOW.

Figure 1. Fractional Two's Complement Notation

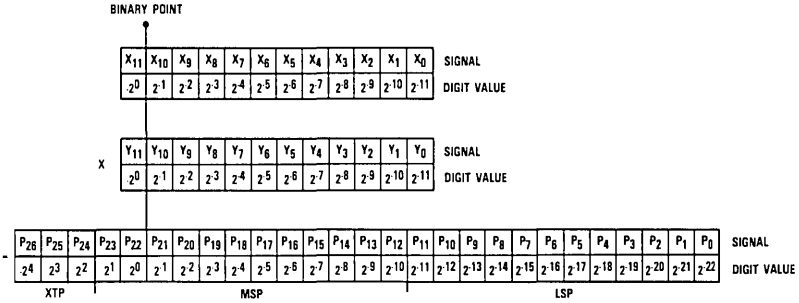


Figure 2. Fractional Unsigned Magnitude Notation

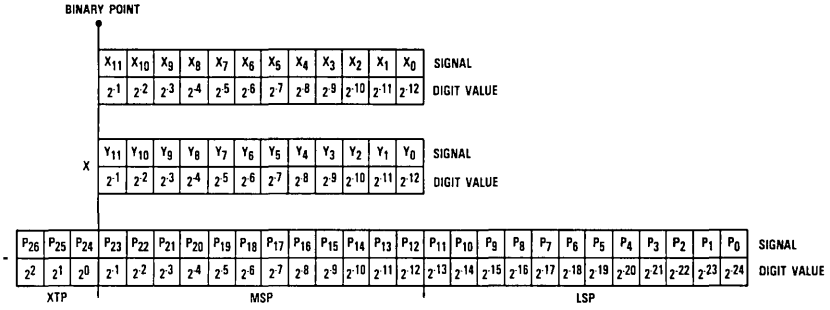


Figure 3. Integer Two's Complement Notation

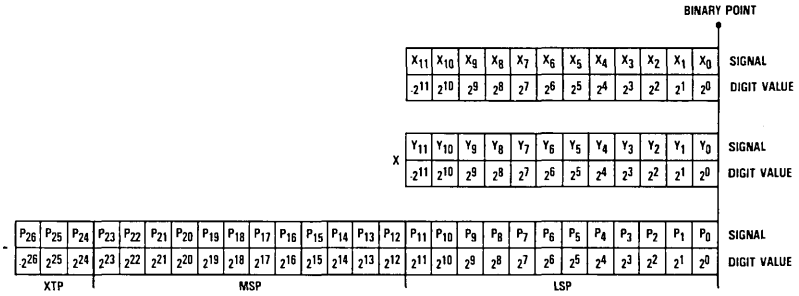
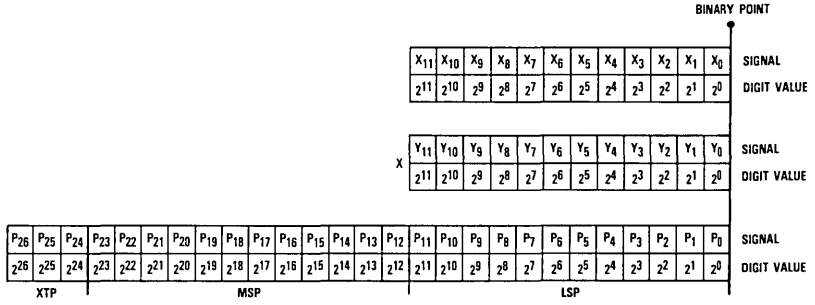


Figure 4. Integer Unsigned Magnitude Notation



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Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−6.0 to +6.0mA
Output	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−1.0 to +6.0mA [3,4]
Short-circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, case	−55 to +125°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PW}	Clock Pulse Width	25			30			ns
t_S	Input Setup Time (Except PREL)	25			30			ns
t_S	Input Setup Time (PREL)	40			45			ns
t_H	Input Hold Time	0			3			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		+125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = MAX, Static[1]		750		850	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V					
		X_{IN}, Y_{IN}, RND, ACC, SUB, TC		−0.4		−0.4	mA
		CLK Y, P, PREL		−2.0		−2.0	mA
		CLK X, TSL, TSM, TSX		−1.0		−1.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V					
		X_{IN}, Y_{IN}, RND, ACC, SUB, TC		75		100	μA
		CLK Y, P, PREL		150		200	μA
		CLK X, TSL, TSM, TSX		75		100	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{CC} = MAX, V_I = 0.4V		−400		−400	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{CC} = MAX, V_I = 2.4V		75		100	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = MAX, output HIGH, one pin to ground, *one second duration*		−50		−50	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		10		10	pF

Note:

1. Worst case, all inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MA}	Multiply-Accumulate Time	V_{CC} = MIN		135		170	ns
t_D	Output Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V		40		45	ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 1.8V		40		45	ns
t_{DIS}	Three-State Output Disable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1}[2]		40		45	ns

Notes:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in Figure 7.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

H

Figure 5. Timing Diagram

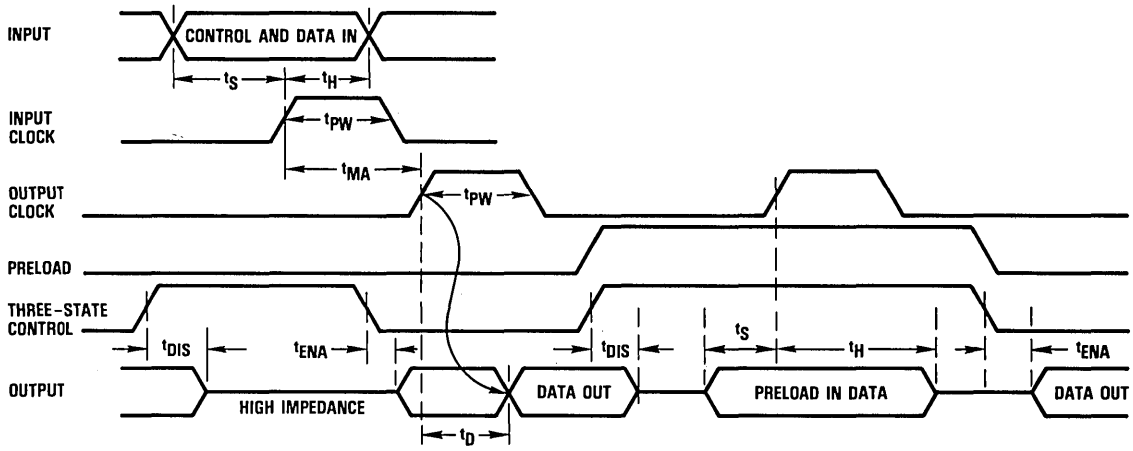
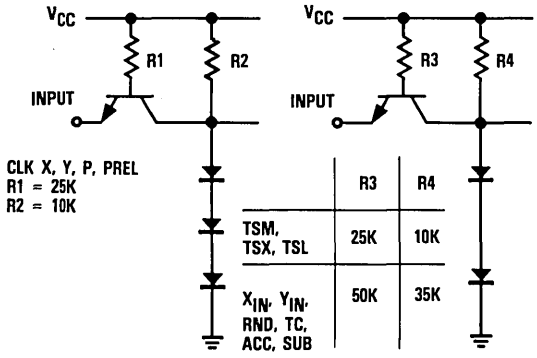


Figure 6. Equivalent Input Circuit



	R3	R4
TSM, TSX, TSL	25K	10K
X_{IN}, Y_{IN}, RND, TC, ACC, SUB	50K	35K

Figure 7. Transition Levels For Three-State Measurements

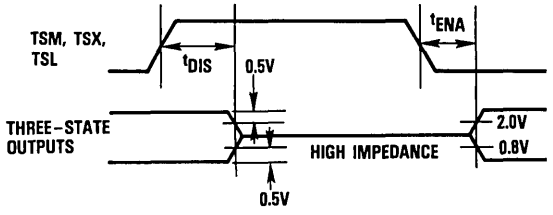
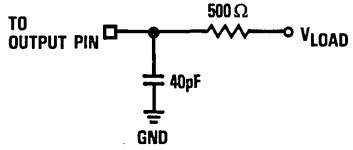


Figure 8. Test Load



Application Notes

Multiplication by a Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and the desired register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the TDC1009 does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 4.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1009J1C	STD-T_A = 0°C to 70°C	Commercial	64 Lead DIP	1009J1C
TDC1009J1G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	64 Lead DIP	1009J1G
TDC1009J1F	EXT-T_C = -55°C to 125°C	Commercial	64 Lead DIP	1009J1F
TDC1009J1A	EXT-T_C = -55°C to 125°C	High Reliability[2]	64 Lead DIP	1009J1A
TDC1009C1F	EXT-T_C = -55°C to 125°C	Commercial	68 Contact Chip Carrier	1009C1F
TDC1009C1A	EXT-T_C = -55°C to 125°C	High Reliability[2]	68 Contact Chip Carrier	1009C1A
TDC1009L1F[1]	EXT-T_C = -55°C to 125°C	Commercial	68 Leaded Chip Carrier	1009L1F
TDC1009L1A[1]	EXT-T_C = -55°C to 125°C	High Reliability2	68 Leaded Chip Carrier	1009L1A

Notes:

1. Contact factory for availability.
2. Per TRW document 70Z1757.

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TDC1010

VLSI Multiplier–Accumulator
16 X 16 bit, 165ns

The TDC1010 is a high-speed 16 x 16 bit parallel multiplier-accumulator which operates at a 165 nanosecond cycle time (6MHz multiply-accumulate rate). The input data may be specified as two's complement or unsigned magnitude, yielding a full-precision 32-bit product. Products may be accumulated to a 35-bit result.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The result is divided into a 3-bit eXTended Product (XTP), a 16-bit Most Significant Product (MSP), and a 16-bit Least Significant Product (LSP). Individual three-state output ports are provided for the XTP and the MSP; the LSP is multiplexed with the Y input. The output register can be preloaded directly via the output ports.

Built with TRW's 2-micron bipolar process, the TDC1010 is a uniquely powerful LSI signal processing device.

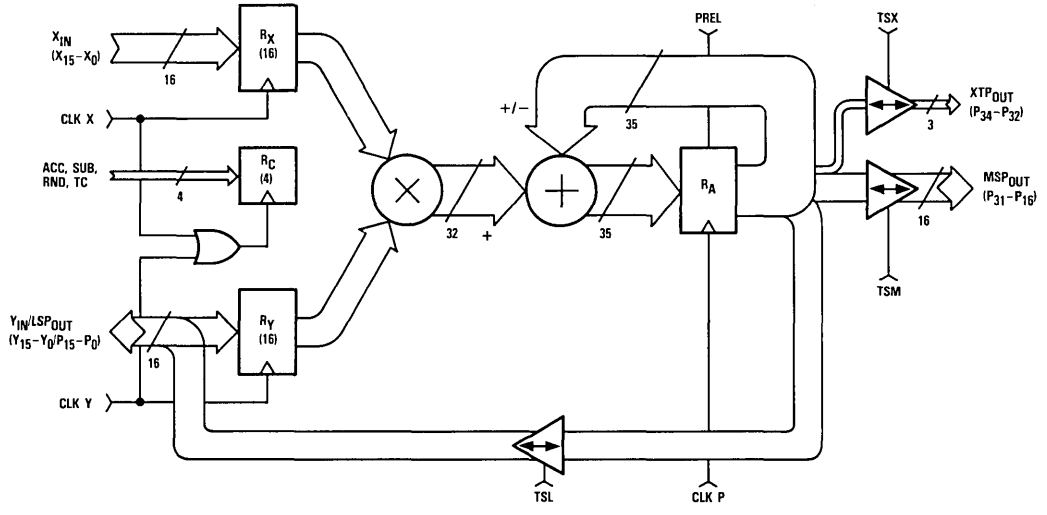
Features

- 165ns Multiply-Accumulate Time (Worst Case)
- 16 x 16 Bit Parallel Multiplication With Accumulation to 35-Bit Result
- Selectable Accumulation, Subtraction, Rounding, And Preloading
- All Inputs And Outputs Are Registered TTL Compatible
- Three-State Outputs
- Two's Complement Or Unsigned Magnitude Operation
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In 64 Lead Ceramic DIP, 68 Contact Chip Carrier Or 68 Leaded Chip Carrier

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



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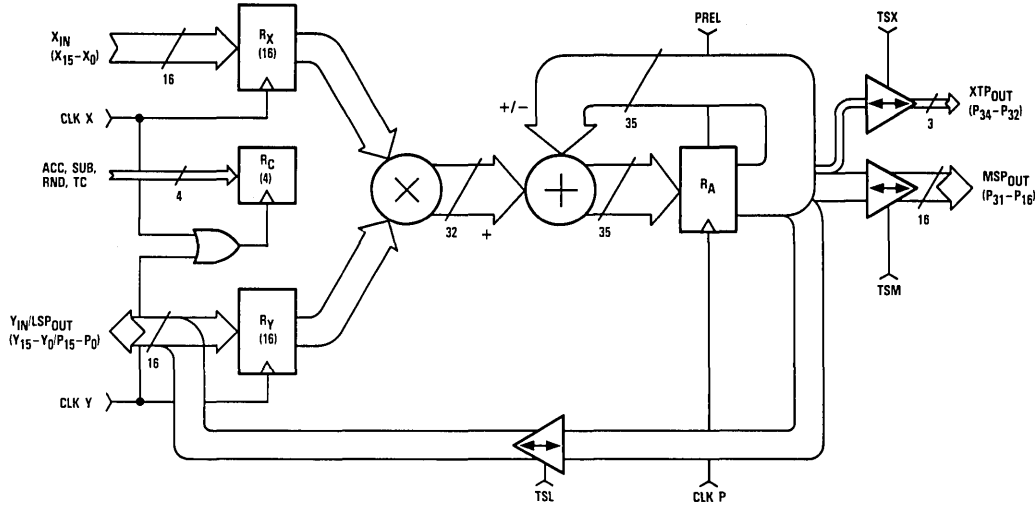
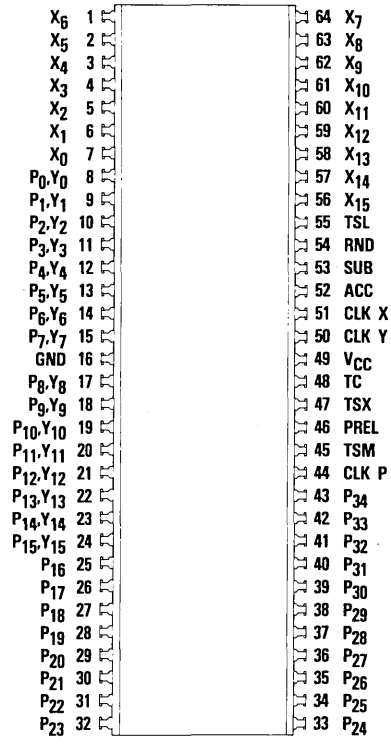
Functional Block Diagram

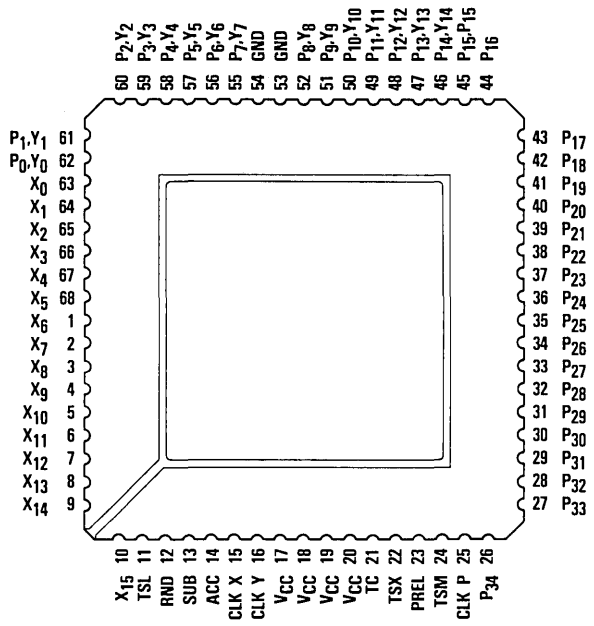


Pin Assignments



64 Lead DIP – J1 Package

Pin Assignments



68 Contact Or Leaded Chip Carrier – C1, L1 Package

Functional Description

General Information

The TDC1010 consists of four functional sections: Input registers, an asynchronous multiplier array, an adder, and output registers. The input registers store the two 16-bit numbers which are to be multiplied, and the control lines which control the input numerical format (two's complement or unsigned magnitude), output rounding, accumulation, and subtraction. The round control is used when a single-word output is desired. Each number is independently stored, simplifying multiplication by a constant. The output registers can be preloaded with a constant to provide the sum of products plus a constant. The asynchronous multiplier array is a network of AND gates and adders, which has been designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 16-bit words and one 3-bit word: the Most Significant Product (MSP), the Least Significant Product (LSP), and the eXTended Product (XTP). Three-state output drivers permit the TDC1010 to be used on a bus, or allow the outputs to be multiplexed over the same 16-bit output lines. The Least Significant Product (LSP) is multiplexed with the Y input.

H

Power

The TDC1010 operates from a single +5 Volt supply. All power and ground lines must be connected.

Name	Function	Value	J1 Package	C1, LI Package
V_{CC}	Positive Supply Voltage	+5.0V	Pin 49	Pins 17, 18, 19, 20
GND	Ground	0.0V	Pin 16	Pins 53, 54

Data Inputs

The TDC1010 has two 16-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_{15} and Y_{15}, carry the sign information for the two's complement notation. The remaining bits are denoted X_{14} through X_0 and Y_{14} through Y_0 (with X_0 and Y_0 the Least Significant Bits). Data present at the X and Y inputs are clocked into the input registers at the rising edge of the appropriate clock. The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

Name	Function	Value	J1 Package	C1, LI Package
X_{15}	X Data MSB	TTL	Pin 56	Pin 10
X_{14}		TTL	Pin 57	Pin 9
X_{13}		TTL	Pin 58	Pin 8
X_{12}		TTL	Pin 59	Pin 7
X_{11}		TTL	Pin 60	Pin 6
X_{10}		TTL	Pin 61	Pin 5
X_9		TTL	Pin 62	Pin 4
X_8		TTL	Pin 63	Pin 3
X_7		TTL	Pin 64	Pin 2
X_6		TTL	Pin 1	Pin 1
X_5		TTL	Pin 2	Pin 68
X_4		TTL	Pin 3	Pin 67
X_3		TTL	Pin 4	Pin 66
X_2		TTL	Pin 5	Pin 65
X_1		TTL	Pin 6	Pin 64
X_0	X Data LSB	TTL	Pin 7	Pin 63
Y_{15}	Y Data MSB	TTL	Pin 24	Pin 45
Y_{14}		TTL	Pin 23	Pin 46
Y_{13}		TTL	Pin 22	Pin 47
Y_{12}		TTL	Pin 21	Pin 48
Y_{11}		TTL	Pin 20	Pin 49
Y_{10}		TTL	Pin 19	Pin 50
Y_9		TTL	Pin 18	Pin 51
Y_8		TTL	Pin 17	Pin 52
Y_7		TTL	Pin 15	Pin 55
Y_6		TTL	Pin 14	Pin 56
Y_5		TTL	Pin 13	Pin 57
Y_4		TTL	Pin 12	Pin 58
Y_3		TTL	Pin 11	Pin 59
Y_2		TTL	Pin 10	Pin 60
Y_1		TTL	Pin 9	Pin 61
Y_0	Y Data LSB	TTL	Pin 8	Pin 62

Data Outputs

The TDC1010 has a 35-bit two's complement or unsigned magnitude result that is the sum of the products of the two input data values and the previous products which have been accumulated. The output is divided into two 16-bit output words, the Most Significant Product (MSP) and Least Significant Product (LSP), and one 3-bit output word, the eXTended Product (XTP). The Most Significant Bit (MSB) of the XTP is the sign bit if two's complement notation is used. The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

Name	Function	Value	J1 Package	C1, L1 Package
P_{34}	Product MSB	TTL	Pin 43	Pin 26
P_{33}		TTL	Pin 42	Pin 27
P_{32}		TTL	Pin 41	Pin 28
P_{31}		TTL	Pin 40	Pin 29
P_{30}		TTL	Pin 39	Pin 30
P_{29}		TTL	Pin 38	Pin 31
P_{28}		TTL	Pin 37	Pin 32
P_{27}		TTL	Pin 36	Pin 33
P_{26}		TTL	Pin 35	Pin 34
P_{25}		TTL	Pin 34	Pin 35
P_{24}		TTL	Pin 33	Pin 36
P_{23}		TTL	Pin 32	Pin 37
P_{22}		TTL	Pin 31	Pin 38
P_{21}		TTL	Pin 30	Pin 39
P_{20}		TTL	Pin 29	Pin 40
P_{19}		TTL	Pin 28	Pin 41
P_{18}		TTL	Pin 27	Pin 42
P_{17}		TTL	Pin 26	Pin 43
P_{16}		TTL	Pin 25	Pin 44
P_{15}		TTL	Pin 24	Pin 45
P_{14}		TTL	Pin 23	Pin 46
P_{13}		TTL	Pin 22	Pin 47
P_{12}		TTL	Pin 21	Pin 48
P_{11}		TTL	Pin 20	Pin 49
P_{10}		TTL	Pin 19	Pin 50
P_9		TTL	Pin 18	Pin 51
P_8		TTL	Pin 17	Pin 52
P_7		TTL	Pin 15	Pin 55
P_6		TTL	Pin 14	Pin 56
P_5		TTL	Pin 13	Pin 57
P_4		TTL	Pin 12	Pin 58
P_3		TTL	Pin 11	Pin 59
P_2		TTL	Pin 10	Pin 60
P_1		TTL	Pin 9	Pin 61
P_0	Product LSB	TTL	Pin 8	Pin 62

Clocks

The TDC1010 has three clock lines, one for each of the input registers and one for the product register. Data present at the inputs of these registers is loaded into the registers at the rising edge of the appropriate clock. The RouND (RND), Two's Complement (TC), ACCumulate (ACC), and SUBtract (SUB) inputs are registered, with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J1 Package	C1, LI Package
CLK X	Clock Input Data X	TTL	Pin 51	Pin 15
CLK Y	Clock Input Data Y	TTL	Pin 50	Pin 16
CLK P	Clock Product Register	TTL	Pin 44	Pin 25

Controls

The TDC1010 has eight control lines. TSX, TSM, and TSL are three-state enable lines for the XTP, the MSP, and the LSP respectively. The output driver is in the high-impedance state when TSX, TSM, or TSL is HIGH, and enabled when the appropriate control is LOW.

PRELoad (PREL) is an active-HIGH control which has several effects when active (see Table 1). First, all output buffers are forced into the high-impedance state. Second, when any or all of TSX, TSM, and TSL are also HIGH, external data present at the output pins will be preloaded into the corresponding section of the output register on the rising edge of CLK P. Normal data setup and hold times apply both to the logical AND of PREL and the relevant three-state control (TSX, TSM, TSL), and to the data being preloaded. These setup and hold times are with respect to the rising edge of CLK P.

RouND (RND) controls the addition of a 1 to the MSB of the LSP for rounding. When RND is HIGH, a 1 is added to the MSB of the LSP for rounding the product in the MSP and XTP (if appropriate) rather than truncating it.

Two's Complement (TC) controls how the device interprets data on the X and Y inputs. TC HIGH makes both inputs two's complement inputs, while TC LOW makes both inputs magnitude only inputs.

When ACCumulate (ACC) is HIGH, the content of the output register is added to or subtracted from the next product generated, and their sum is stored back into the output registers at the next rising edge of CLK P. When ACC is LOW, multiplication without accumulation is performed, and the next product generated is stored into the output registers directly. This operation is used for the first term in a summation to avoid a separate "clear" operation.

The SUBtract (SUB) control is used in conjunction with the ACC control. When both the ACC and SUB controls are HIGH, the content of the output register is subtracted from the next product generated and the difference is stored back into the output register. Note that the previous output is subtracted from the product, not the product from the previous output.

The RND, TC, ACC, and SUB inputs are registered, with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J1 Package	C1, LI Package
TSX	XTP Three-State Control	TTL	Pin 47	Pin 22
TSM	MSP Three-State Control	TTL	Pin 45	Pin 24
TSL	LSP Three-State Control	TTL	Pin 55	Pin 11
PREL	Preload Control	TTL	Pin 46	Pin 23
RND	Round Control Bit	TTL	Pin 54	Pin 12
TC	Two's Complement Control	TTL	Pin 48	Pin 21
ACC	Accumulate Control	TTL	Pin 52	Pin 14
SUB	Subtract Control	TTL	Pin 53	Pin 13

Figure 1. Fractional Two's Complement Notation

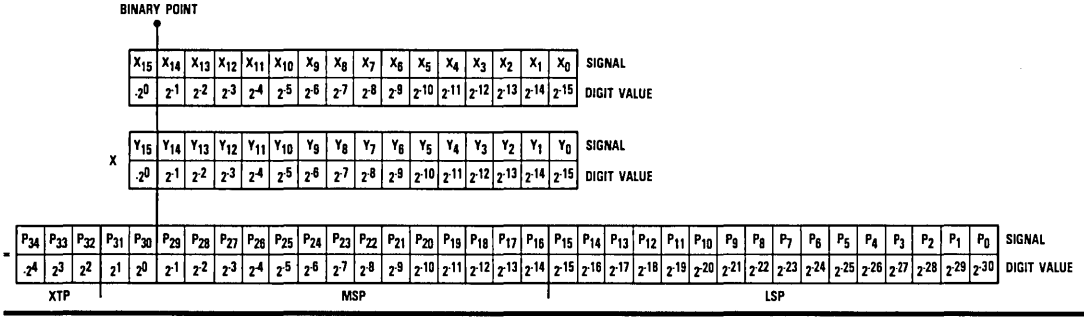


Figure 2. Fractional Unsigned Magnitude Notation

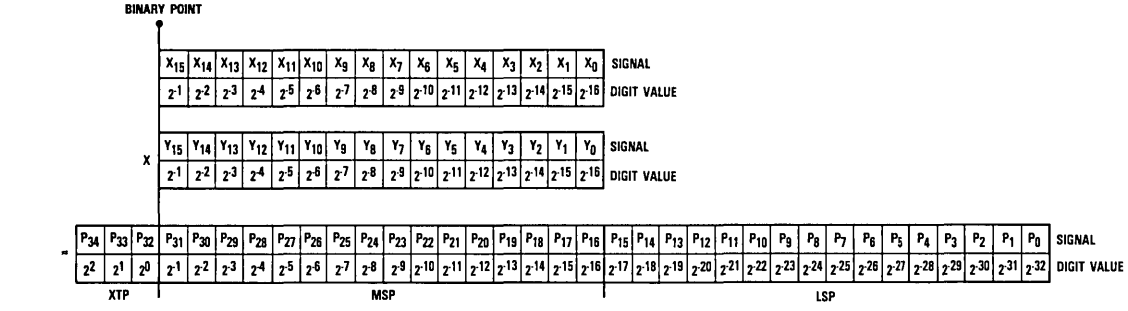


Figure 3. Integer Two's Complement Notation

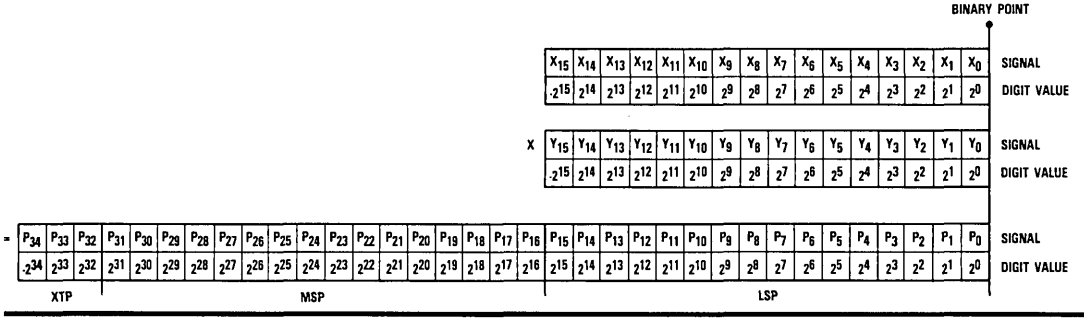
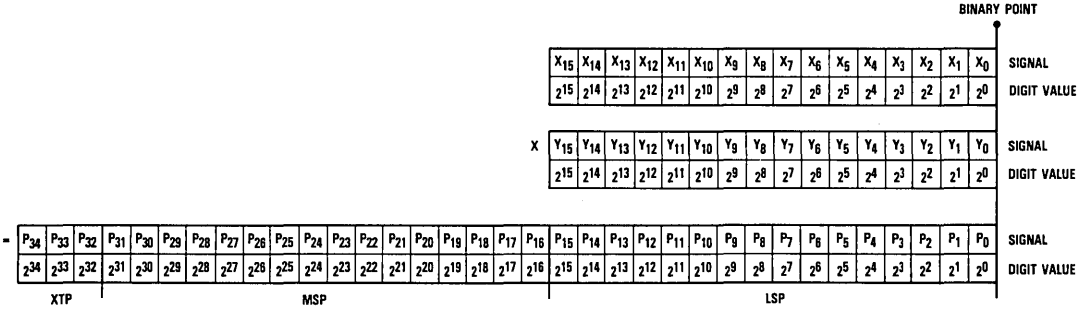


Figure 4. Integer Unsigned Magnitude Notation.



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−6.0 to +6.0mA
Output	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−1.0 to +6.0mA [3,4]
Short-circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, case	−55 to +125°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PW}	Clock Pulse Width	25			30			ns
t_S	Input Setup Time (Except PREL)	25			30			ns
t_S	Input Setup Time (PREL)	40			45			ns
t_H	Input Hold Time	0			3			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		+125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = MAX, Static[1]		1100		1250	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V					
		X_{IN}, RND, ACC, SUB, TC		−0.4		−0.4	mA
		Y_{IN}		−0.8		−0.8	mA
		CLK X, TSX, TSM, and TSL		−1.0		−1.0	mA
		CLK P, CLK Y, PREL		−2.0		−2.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V					
		X_{IN}, RND, ACC, SUB, TC		75		100	μA
		Y_{IN}		75		100	μA
		CLK X, TSX, TSM, and TSL		75		100	μA
		CLK P, CLK Y, PREL		150		200	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{CC} = MAX, V_I = 0.4V		−800		−800	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{CC} = MAX, V_I = 2.4V		75		100	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = MAX, Output HIGH, one pin to ground, one second duration		−50		−50	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:

1. Worst case, all inputs and outputs LOW.

Switching characteristics within specified operating conditions[1]

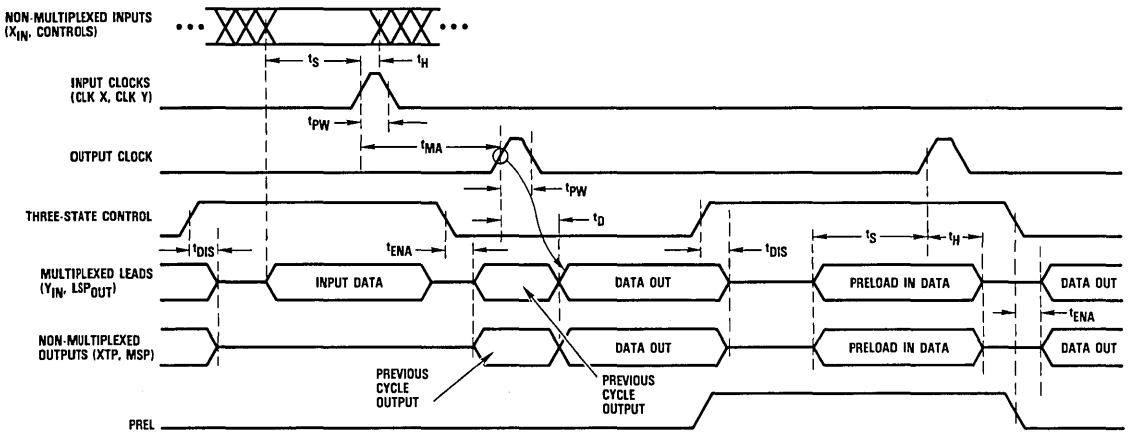
Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MA}	Multiply-Accumulate Time	V_{CC} = MIN		165		200	ns
t_D	Output Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V		40		45	ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 1.8V		40		45	ns
t_{DIS}	Three-State Output Disable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1}[2]		40		45	ns

Notes:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in Figure 9.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

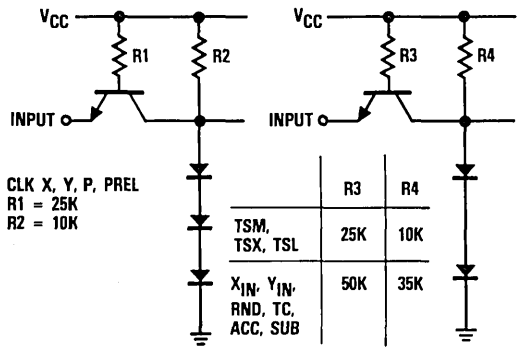
H

Figure 5. Timing Diagram



Note: On multiplexed leads, input data and preload in data are applied to the TDC1010, and data out is produced and driven by the TDC1010.

Figure 6. Equivalent Input Circuit



	R3	R4
TSM, TSX, TSL	25K	10K
X_{IN}, Y_{IN}, RND, TC, ACC, SUB	50K	35K

Figure 7. Equivalent Output Circuit

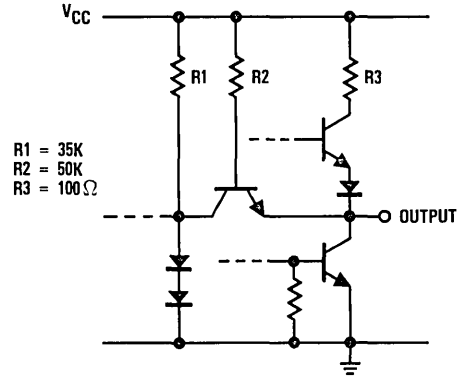


Figure 8. Test Load

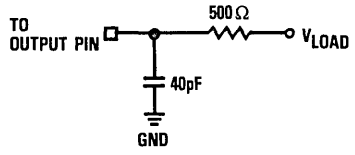
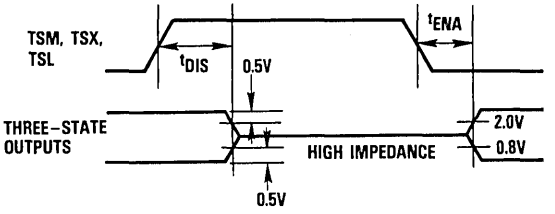


Figure 9. Transition Levels For Three-State Measurements



Preload Truth Table 1

PREL[1]	TSX[1]	TSM[1]	TSL[1]	XTP	MSP	LSP
L	L	L	L	Register→ Output pin	Register→ Output pin	Register→ Output pin
L	L	L	H	Register→ Output pin	Register→ Output pin	Hi-Z
L	L	H	L	Register→ Output pin	Hi-Z	Register→ Output pin
L	L	H	H	Register→ Output pin	Hi-Z	Hi-Z
L	H	L	L	Hi-Z	Register→ Output pin	Register→ Output pin
L	H	L	H	Hi-Z	Register→ Output pin	Hi-Z
L	H	H	L	Hi-Z	Hi-Z	Register→ Output pin
L	H	H	H	Hi-Z	Hi-Z	Hi-Z
H[2]	L	L	L	Hi-Z	Hi-Z	Hi-Z
H[2]	L	L	H	Hi-Z	Hi-Z	Hi-Z Preload
H[2]	L	H	L	Hi-Z	Hi-Z Preload	Hi-Z
H[2]	L	H	H	Hi-Z	H1-Z Preload	Hi-Z Preload
H[2]	H	L	L	Hi-Z Preload	Hi-Z	Hi-Z
H[2]	H	L	H	Hi-Z Preload	Hi-Z	Hi-Z Preload
H[2]	H	H	L	Hi-Z Preload	Hi-Z Preload	Hi-Z
H[2]	H	H	H	Hi-Z Preload	Hi-Z Preload	Hi-Z Preload

Notes:

1. PREL, TSX, TSM, and TSL are not registered.
2. PREL Hi inhibits any change of output register for those outputs in which the three-state control is LOW.

Application Notes

Multiplication by a Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and that the register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the TDC1010 does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 4.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1010J1C	STD-T_A = 0°C to 70°C	Commercial	64 Lead DIP	1010J1C
TDC1010J1G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	64 Lead DIP	1010J1G
TDC1010J1F	EXT-T_C = -55°C to 125°C	Commercial	64 Lead DIP	1010J1F
TDC1010J1A	EXT-T_C = -55°C to 125°C	High Reliability[2]	64 Lead DIP	1010J1A
TDC1010C1F	EXT-T_C = -55°C to 125°C	Commercial	68 Contact Chip Carrier	1010C1F
TDC1010C1A	EXT-T_C = -55°C to 125°C	High Reliability[2]	68 Contact Chip Carrier	1010C1A
TDC1010L1F[1]	EXT-T_C = -55°C to 125°C	Commercial	68 Leaded Chip Carrier	1010L1F
TDC1010L1A[1]	EXT-T_C = -55°C to 125°C	High Reliability[2]	68 Leaded Chip Carrier	1010L1A

Notes:

1. Contact factory for availability.
2. Per TRW document 70Z1757.

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TDC1043
Preliminary Information

VLSI Multiplier–Accumulator
16 X 16 bit, 100ns

The TRW TDC1043 is a high-speed 16 X 16 bit parallel multiplier-accumulator which operates at a 100 nanosecond cycle time (10MHz multiply-accumulate rate). The input data may be specified as two's complement or unsigned magnitude.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge triggered D-type flip-flops. All outputs are three-state.

Built with TRW's OMICRON-B™ 1-micron bipolar process, the TDC1043 is pin-compatible with the industry standard TDC1010, but does not provide the preload and Least Significant Product (LSP) output capabilities of the TDC1010. However, the LSP bits are used internally for accurate accumulation. The TDC1043 operates with almost twice the speed of the TDC1010 at less than one-third the power dissipation.

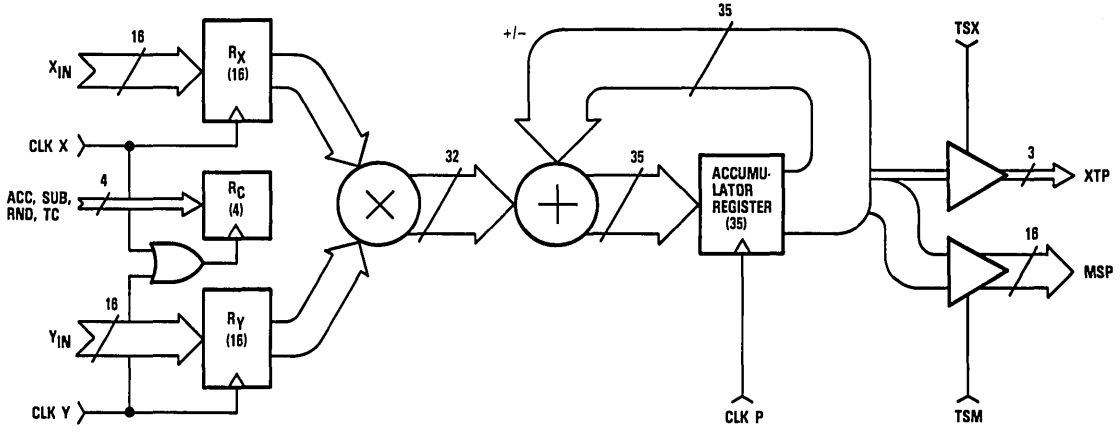
Features

- 100ns Multiply-Accumulate Time (Worst Case)
- 16 X 16 Bit Parallel Multiplication With Selectable Accumulation And Subtraction, And 19-Bit Limited Precision Output
- Pin Compatible With TRW TDC1010
- All Inputs And Outputs Are Registered TTL Compatible
- Three-State TTL Outputs
- Two's Complement Or Unsigned Magnitude Multiplication
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In 64 Lead DIP, 68 Contact Chip Carrier Or 68 Leaded Chip Carrier

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



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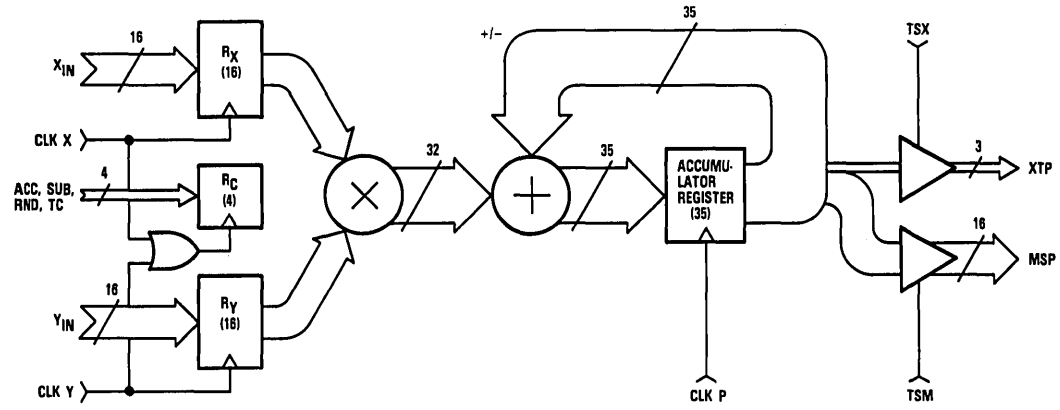
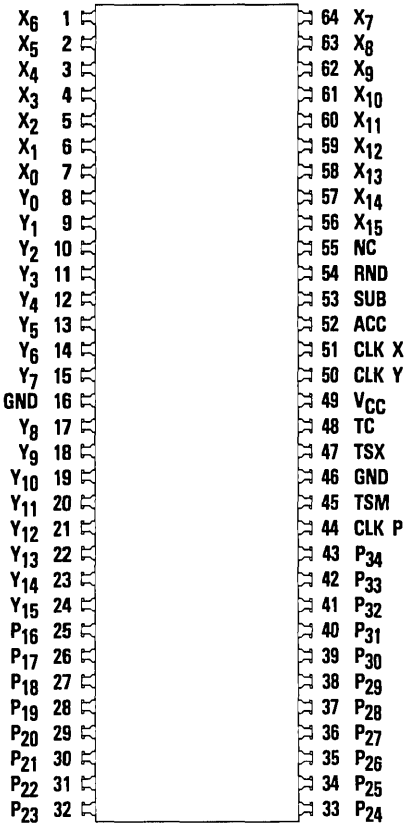
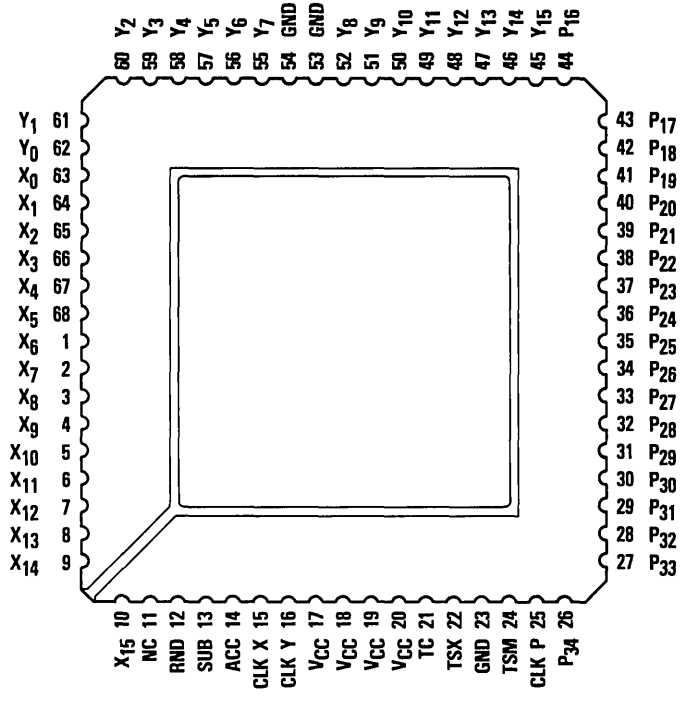
Functional Block Diagram



Pin Assignments



64 Lead DIP – J3 Package



68 Contact Or Leaded Chip Carrier – C1, L1 Package

Functional Description

General Information

The TDC1043 has four functional sections: Input registers, an asynchronous multiplier array, an adder, and output registers. The input registers store the two 16-bit numbers which are to be multiplied and the control lines which control the input numerical format (two's complement or unsigned magnitude), output roundings, accumulation and subtraction. Each number is stored independently, simplifying multiplication by a constant. The asynchronous multiplier array is a network of AND gates and adders, which has been designed to handle two's complement or unsigned magnitude numbers. The output registers hold the complete result. Three-state output drivers are provided for one 16-bit word, the Most Significant Product (MSP), and one 3-bit word, the eXTended Product (XTP). The Least Significant Product (LSP) is not available with the TDC1043. It is held internally for use in accumulation. Three-state output drivers permit the TDC1043 to be used on a bus, or allow the outputs to be multiplexed over the same 16-bit output lines. The unit is pin-compatible with the TDC1010 with the exception that there is no preload capability or least significant product output.

Power

The TDC1043 operates from a single +5 Volt supply. The voltage tolerance is different for the standard and extended temperature range parts. All power and ground lines must be connected. A good ground must be provided due to the large number of data outputs capable of changing simultaneously. A 0.1μF (minimum) bypass capacitor between V_{CC} and ground is recommended.

TDC1010 Compatibility Note: Permanently connect pin 46 (J3 package) or pin 23 (C1, L1 package) on the TDC1043 to ground. Do not leave this pin open or connected to a TTL output. (On the TDC1010, this pin is the preload pin.)

Name	Function	Value	J3 Package	C1, L1 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pin 49	Pins 17, 18, 19, 20
GND	Ground	0.0V	Pins 16, 46	Pins 23, 53, 54

Data Inputs

The TDC1043 has two 16-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_{15} and Y_{15}, carry the sign information for the two's complement notation. The remaining bits are denoted X_{14} through X_0 and Y_{14} through Y_0 (with X_0 and Y_0 the Least Significant Bits). Data present at the X and Y inputs are clocked into the input registers at the rising edge of the appropriate clock. The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

Name	Function	Value	J3 Package	C1, L1 Package
X_{15}	X Data MSB	TTL	Pin 56	Pin 10
X_{14}		TTL	Pin 57	Pin 9
X_{13}		TTL	Pin 58	Pin 8
X_{12}		TTL	Pin 59	Pin 7
X_{11}		TTL	Pin 60	Pin 6
X_{10}		TTL	Pin 61	Pin 5
X_9		TTL	Pin 62	Pin 4
X_8		TTL	Pin 63	Pin 3
X_7		TTL	Pin 64	Pin 2
X_6		TTL	Pin 1	Pin 1
X_5		TTL	Pin 2	Pin 68
X_4		TTL	Pin 3	Pin 67
X_3		TTL	Pin 4	Pin 66
X_2		TTL	Pin 5	Pin 65
X_1		TTL	Pin 6	Pin 64
X_0	X Data LSB	TTL	Pin 7	Pin 63
Y_{15}	Y Data MSB	TTL	Pin 24	Pin 45
Y_{14}		TTL	Pin 23	Pin 46
Y_{13}		TTL	Pin 22	Pin 47
Y_{12}		TTL	Pin 21	Pin 48
Y_{11}		TTL	Pin 20	Pin 49
Y_{10}		TTL	Pin 19	Pin 50
Y_9		TTL	Pin 18	Pin 51
Y_8		TTL	Pin 17	Pin 52
Y_7		TTL	Pin 15	Pin 55
Y_6		TTL	Pin 14	Pin 56
Y_5		TTL	Pin 13	Pin 57
Y_4		TTL	Pin 12	Pin 58
Y_3		TTL	Pin 11	Pin 59
Y_2		TTL	Pin 10	Pin 60
Y_1		TTL	Pin 9	Pin 61
Y_0	Y Data LSB	TTL	Pin 8	Pin 62

Data Outputs

The TDC1043 has a 35-bit two's complement or unsigned magnitude result that is the sum of the products of the two input data values and the previous products which have been accumulated. Only the most significant 19 bits are available off-chip. The output is divided into one 16-bit output word, the Most Significant Product (MSP), and one 3-bit output word, the eXTended Product (XTP). The Most Significant Bit (MSB) of the XTP is the sign bit if two's complement notation is used. The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 and 4, respectively.

Name	Function	Value	J3 Package	C1, L1 Package
P_{34}	Product MSB	TTL	Pin 43	Pin 26
P_{33}		TTL	Pin 42	Pin 27
P_{32}		TTL	Pin 41	Pin 28
P_{31}		TTL	Pin 40	Pin 29
P_{30}		TTL	Pin 39	Pin 30
P_{29}		TTL	Pin 38	Pin 31
P_{28}		TTL	Pin 37	Pin 32
P_{27}		TTL	Pin 36	Pin 33
P_{26}		TTL	Pin 35	Pin 34
P_{25}		TTL	Pin 34	Pin 35
P_{24}		TTL	Pin 33	Pin 36
P_{23}		TTL	Pin 32	Pin 37
P_{22}		TTL	Pin 31	Pin 38
P_{21}		TTL	Pin 30	Pin 39
P_{20}		TTL	Pin 29	Pin 40
P_{19}		TTL	Pin 28	Pin 41
P_{18}		TTL	Pin 27	Pin 42
P_{17}		TTL	Pin 26	Pin 43
P_{16}		TTL	Pin 25	Pin 44

Clocks

The TDC1043 has three clock lines, one for each of the input registers and one for the product register. Data present at the inputs of these registers are loaded into the registers at the rising edge of the appropriate clock. Note that the input to the output register comes only from the internal adder and multiplier array. The RouND (RND), Two's Complement (TC), ACCumulate (ACC), and SUBtract (SUB) inputs are registered, with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with the loading of these four control signals can be avoided by use of normally LOW clocks.

Name	Function	Value	J3 Package	C1, L1 Package
CLK X	Clock Input Data X	TTL	Pin 51	Pin 15
CLK Y	Clock Input Data Y	TTL	Pin 50	Pin 16
CLK P	Clock Product Register	TTL	Pin 44	Pin 25

Controls

The TDC1043 has six control lines. TSX and TSM are three-state enable lines for the XTP and the MSP. The output driver is in the high-impedance state when TSX or TSM is HIGH, and enabled when the appropriate control is LOW. TSX and TSM are not registered.

RouND (RND) controls the addition of a 1 to the MSB of the LSP for rounding. When RND is HIGH, a 1 is added to the MSB of the LSP for rounding the product in the MSP and XTP (if appropriate) rather than truncating it.

Two's Complement (TC) controls how the device interprets data on the X and Y inputs. TC HIGH makes both inputs two's complement inputs and TC LOW makes both inputs magnitude only inputs.

When ACCumulate (ACC) is HIGH, the contents of the output register are added to or subtracted from the next product generated, and their sum is stored back into the output registers at the next rising edge of CLK P. When ACC is LOW, multiplication without accumulation is performed, and the next product generated is stored into the output registers directly. This operation is used for the first term in a summation to avoid a separate "clear" operation.

The SUBtract (SUB) control is used in conjunction with the ACC control. When both the ACC and SUB controls are HIGH, the contents of the output register are subtracted from the next product generated and the difference is stored back into the output register. Note that the previous output is subtracted from the product, not the product from the previous output.

The RND, TC, ACC, and SUB inputs are registered, with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J3 Package	C1, L1 Package
TSX	XTP Three-State Control	TTL	Pin 47	Pin 22
TSM	MSP Three-State Control	TTL	Pin 45	Pin 24
RND	Round Control Bit	TTL	Pin 54	Pin 12
TC	Two's Complement Control	TTL	Pin 48	Pin 21
ACC	Accumulate Control	TTL	Pin 52	Pin 14
SUB	Subtract Control	TTL	Pin 53	Pin 13

No Connects

The TDC1043 has one pin labeled "No Connect" (NC). No connection is made between the chip and this pin.

Name	Function	Value	J3 Package	C1, L1 Package
NC	No Connection	Open	Pin 55	Pin 11

Figure 1. Fractional Two's Complement Notation

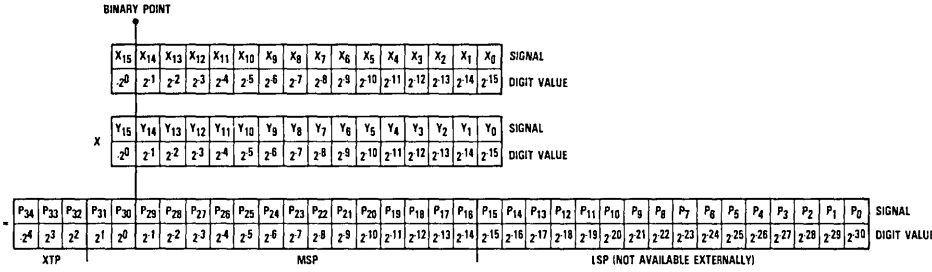


Figure 2. Fractional Unsigned Magnitude Notation

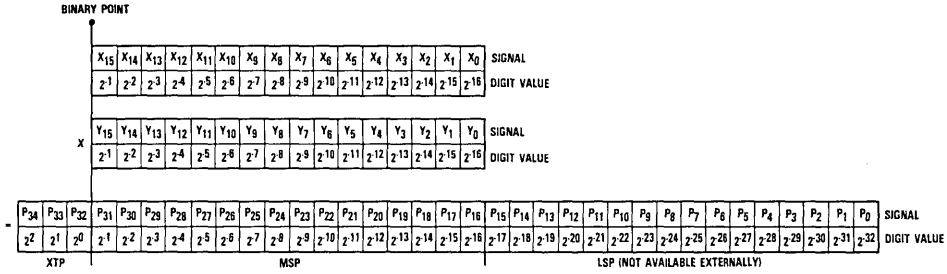


Figure 3. Integer Two's Complement Notation

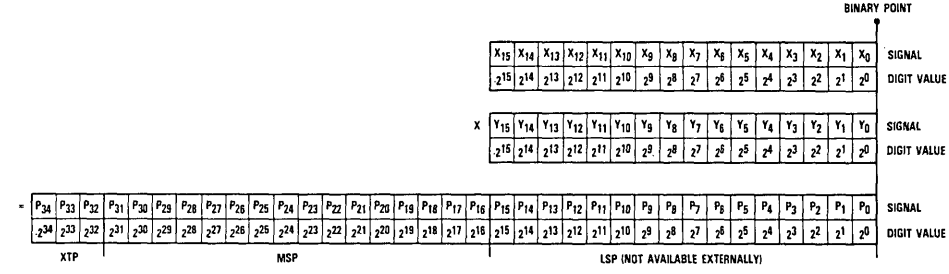
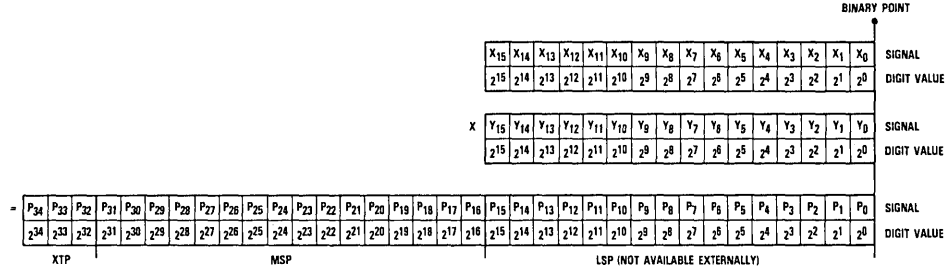


Figure 4. Integer Unsigned Magnitude Notation



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input	
Applied voltage	−0.5 to +5.5 V[2]
Forced current	−6.0 to +6.0mA
Output	
Applied voltage	−0.5 to +5.5V[2]
Forced current	−1.0 to +6.0mA[3,4]
Short−circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, case	−55 to +125°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
t_{PWL}	Clock Pulse Width, LOW	25			ns
t_{PWH}	Clock Pulse Width, HIGH	25			ns
t_S	Input Setup Time	25			ns
t_H	Input Hold Time	0			ns
V_{IL}	Input Voltage, Logic LOW			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			V
I_{OL}	Output Current, Logic LOW			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400	μA
T_A	Ambient Temperature, Still Air	0		70	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
I_{CC}	Supply Current	V_{CC} = MAX, Static [1]			
		T_A = 0°C to 70°C		220	mA
		$T_A \geq$ 25°C		200	mA
		V_{CC} = 5.0V			
		$T_A \geq$ 25°C		195	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V			
		Data Inputs, RND, ACC, SUB, TC		−0.2	mA
		TSX, TSM, CLK X, CLK Y, CLK P		−0.8	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V			
		Data Inputs, RND, ACC, SUB, TC		50	μA
		TSX, TSM, CLK X, CLK Y, CLK P		100	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{CC} = MAX, V_I = 0.4V		−20	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{CC} = MAX, V_I = 2.4V		20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, One pin to ground, one second duration, output HIGH.	−5	−50	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		15	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		15	pF

Note:

1. Worst case, all inputs and outputs LOW.

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
t_{MA}	Multiply-Accumulate Time	V_{CC} = MIN		100	ns
t_D	Output Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V		35	ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 1.8V		35	ns
t_{DIS}	Three-State Output Disable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1} [2]		35	ns

Notes:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in Figure 9.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

Figure 5. Timing Diagram

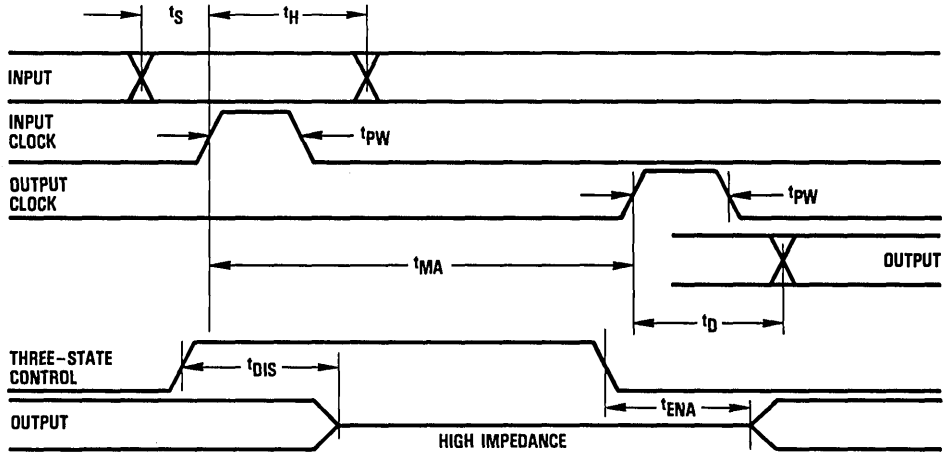
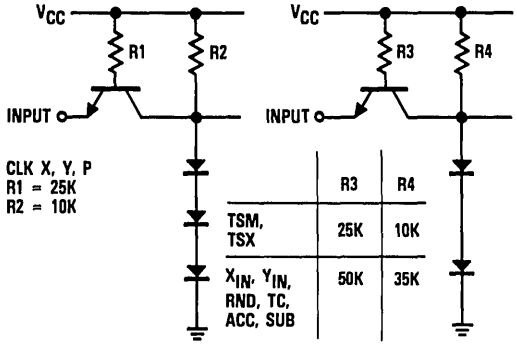


Figure 6. Equivalent Input Circuit



	R3	R4
TSM, TSX	25K	10K
X_{IN}, Y_{IN}, RND, TC, ACC, SUB	50K	35K

Figure 7. Equivalent Output Circuit

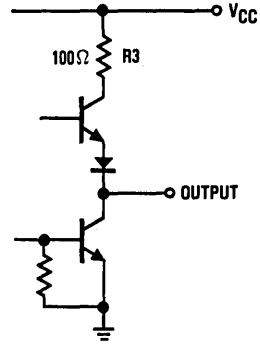


Figure 8. Test Load

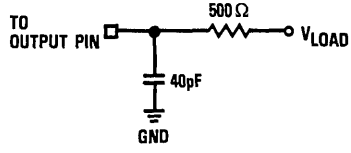
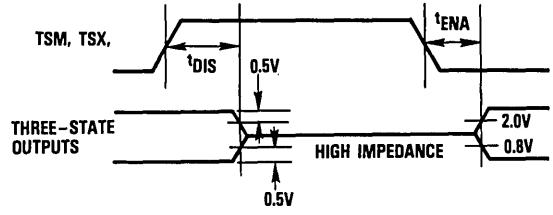


Figure 9. Transition Levels For Three-State Measurements



Application Notes

Multiplication by a Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and that the register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the TDC1043 does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64.$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 4.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1043J3C	STD-T_A = 0°C to 70°C	Commercial	64 Lead DIP	1043J3C
TDC1043J3G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	64 Lead DIP	1043J3G
TDC1043C1C[1]	STD-T_A = 0°C to 70°C	Commercial	68 Contact Chip Carrier	1043C1C
TDC1043C1G[1]	STD-T_A = 0°C to 70°C	Commercial With Burn-In	68 Contact Chip Carrier	1043C1G
TDC1043L1C[1]	STD-T_A = 0°C to 70°C	Commercial	68 Leaded Chip Carrier	1043C1C
TDC1043L1G[1]	STD-T_A = 0°C to 70°C	Commercial With Burn-In	68 Leaded Chip Carrier	1043C1G

Notes:

1. Contact factory for availability.
2. Per TRW document 70Z1757.

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Preliminary Information describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact TRW for current information.

TMC2009
Preliminary Information

CMOS Multiplier–Accumulator
12 x 12 bit, 135ns

The TMC2009 is a high-speed 12 x 12 bit parallel multiplier-accumulator which operates at a 135 nanosecond cycle time (7.4MHz multiply-accumulate rate). The input data may be specified as two's complement or unsigned magnitude, yielding a full-precision 24-bit product. Products may be accumulated to a 27-bit result.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The result is divided into a 3-bit eXTended Product (XTP), a 12-bit Most Significant Product (MSP), and a 12-bit Least Significant Product (LSP). Individual three-state output ports are provided for the XTP, the MSP, and the LSP. The output register can be preloaded directly via the output ports.

Built with TRW's state-of-the-art 2-micron CMOS process, the TMC2009 is pin and function compatible with the industry standard TDC1009 and operates with the same speed at one-fifth or less power dissipation.

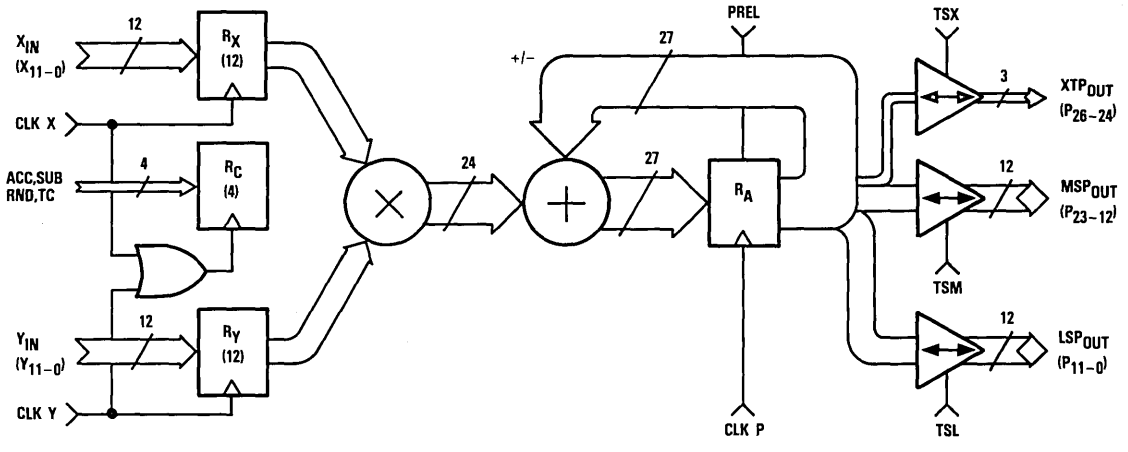
Features

- Low Power Consumption CMOS Process
- Pin And Function Compatible With TRW TDC1009
- 135ns Multiply-Accumulate Time (Worst Case)
- 12 x 12 Bit Parallel Multiplication With Accumulation To 27-Bit Result
- Selectable Accumulation, Subtraction, Rounding, And Preloading
- All Inputs And Outputs Are Registered TTL Compatible
- Three-State Output
- Two's Complement Or Unsigned Magnitude Operation
- Single +5V Power Supply
- Available In 64 Lead DIP, 68 Contact Chip Carrier, Or 68 Leaded Chip Carrier

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



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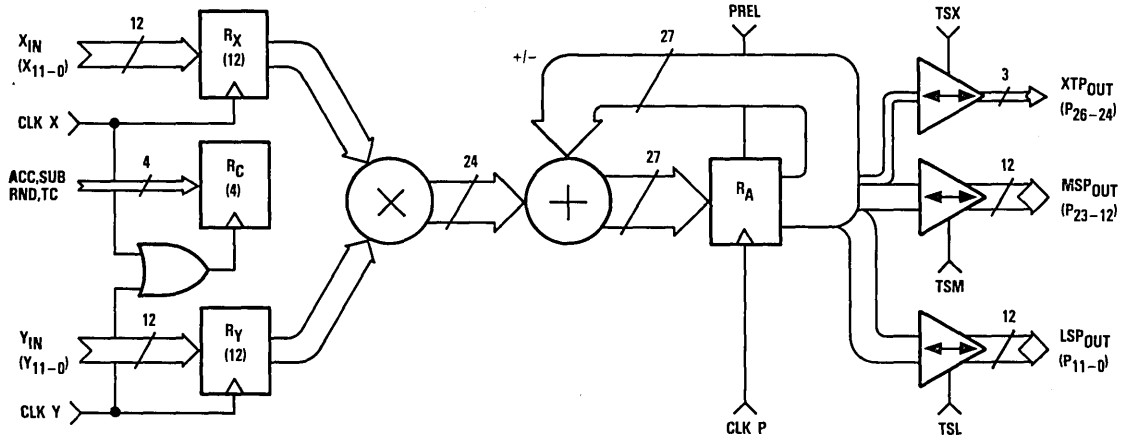
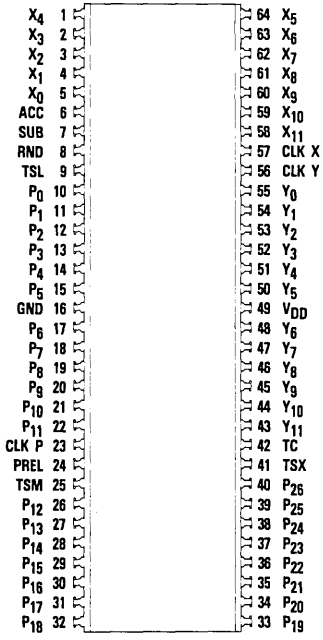
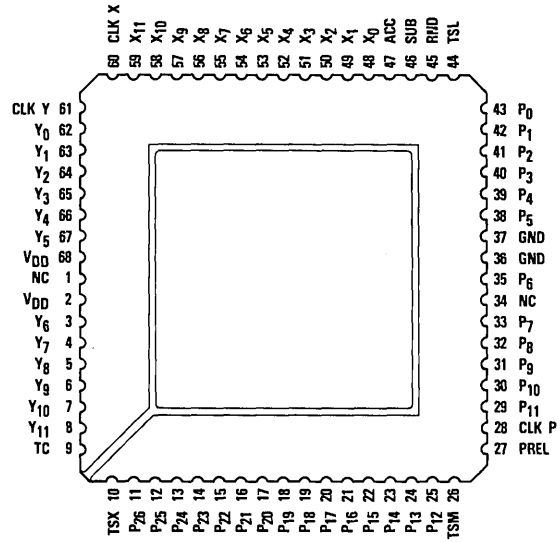
Functional Block Diagram



Pin Assignments



64 Lead DIP – J3 Package



68 Contact or Leaded Chip Carrier – C1, L1 Package

Functional Description

General Information

The TMC2009 consists of four functional sections: Input registers, an asynchronous multiplier array, an adder, and output registers. The input registers store the two 12-bit operands which are to be multiplied, and the control lines which control the input numerical format (two's complement or unsigned magnitude), output rounding, accumulation, and subtraction. The round control is used when a single-word output is desired. Each number is independently stored, simplifying multiplication by a constant. The output registers can be preloaded with a constant to provide the sum of products plus a constant. The asynchronous multiplier array is a network of AND gates and adders, which has been designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 12-bit words and one 3-bit word: the Most Significant Product (MSP), the Least Significant Product (LSP), and the eXTended Product (XTP). Three-state output drivers permit the TMC2009 to be used on a bus, or allow the outputs to be multiplexed over the same 12-bit output lines.

Power

The TMC2009 operates from a single +5 Volt supply. All power and ground lines must be connected.

Name	Function	Value	J3 Package	C1, L1 Package
V_{DD}	Positive Supply Voltage	+5.0V	Pin 49	Pins 68, 2
GND	Ground	0.0V	Pin 16	Pins 34, 36, 37

Data Inputs

The TMC2009 has two 12-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), X_{11} and Y_{11}, carry the sign information for the two's complement notation. The remaining bits are denoted X_{10} through X_0 and Y_{10} through Y_0 (with X_0 and Y_0 the Least Significant Bits). Data present at the X and Y inputs are clocked into the input registers at the rising edge of the appropriate clock. The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

Name	Function	Value	J3 Package	C1, L1 Package
X_{11}	X Data MSB	TTL	Pin 58	Pin 59
X_{10}		TTL	Pin 59	Pin 58
X_9		TTL	Pin 60	Pin 57
X_8		TTL	Pin 61	Pin 56
X_7		TTL	Pin 62	Pin 55
X_6		TTL	Pin 63	Pin 54
X_5		TTL	Pin 64	Pin 53
X_4		TTL	Pin 1	Pin 52
X_3		TTL	Pin 2	Pin 51
X_2		TTL	Pin 3	Pin 50
X_1		TTL	Pin 4	Pin 49
X_0	X Data LSB	TTL	Pin 5	Pin 48

Data Inputs (Cont.)

Name	Function	Value	J3 Package	C1, L1 Package
Y_{11}	Y Data MSB	TTL	Pin 43	Pin 8
Y_{10}		TTL	Pin 44	Pin 7
Y_9		TTL	Pin 45	Pin 6
Y_8		TTL	Pin 46	Pin 5
Y_7		TTL	Pin 47	Pin 4
Y_6		TTL	Pin 48	Pin 3
Y_5		TTL	Pin 50	Pin 67
Y_4		TTL	Pin 51	Pin 66
Y_3		TTL	Pin 52	Pin 65
Y_2		TTL	Pin 53	Pin 64
Y_1		TTL	Pin 54	Pin 63
Y_0	Y Data LSB	TTL	Pin 55	Pin 62

Data Outputs

The TMC2009 has a 27-bit two's complement or unsigned magnitude result that is the sum of the products of the two input data values and the previous products which have been accumulated. This output is divided into two 12-bit output words, the Most Significant Product (MSP) and Least Significant Product (LSP), and one 3-bit output word, the eXTended Product (XTP). The Most Significant Bit (MSB) of the XTP is the sign bit if two's complement notation is used. The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

Name	Function	Value	J3 Package	C1, L1 Package
P_{26}	Product MSB	TTL	Pin 40	Pin 11
P_{25}		TTL	Pin 39	Pin 12
P_{24}		TTL	Pin 38	Pin 13
P_{23}		TTL	Pin 37	Pin 14
P_{22}		TTL	Pin 36	Pin 15
P_{21}		TTL	Pin 35	Pin 16
P_{20}		TTL	Pin 34	Pin 17
P_{19}		TTL	Pin 33	Pin 18
P_{18}		TTL	Pin 32	Pin 19
P_{17}		TTL	Pin 31	Pin 20
P_{16}		TTL	Pin 30	Pin 21
P_{15}		TTL	Pin 29	Pin 22
P_{14}		TTL	Pin 28	Pin 23
P_{13}		TTL	Pin 27	Pin 24
P_{12}		TTL	Pin 26	Pin 25

Data Outputs (Cont.)

Name	Function	Value	J3 Package	C1, L1 Package
P_{11}		TTL	Pin 22	Pin 29
P_{10}		TTL	Pin 21	Pin 30
P_9		TTL	Pin 20	Pin 31
P_8		TTL	Pin 19	Pin 32
P_7		TTL	Pin 18	Pin 33
P_6		TTL	Pin 17	Pin 35
P_5		TTL	Pin 15	Pin 38
P_4		TTL	Pin 14	Pin 39
P_3		TTL	Pin 13	Pin 40
P_2		TTL	Pin 12	Pin 41
P_1		TTL	Pin 11	Pin 42
P_0	Product LSB	TTL	Pin 10	Pin 43

Clocks

The TMC2009 has three clock lines, one for each of the input registers and one for the product register. Data present at the inputs of these registers are loaded into the registers at the rising edge of the appropriate clock. The RouND (RND), Two's Complement (TC), ACCumulate (ACC) and SUBtract (SUB) inputs are registered, with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J3 Package	C1, L1 Package
CLK X	Clock Input Data X	TTL	Pin 57	Pin 60
CLK Y	Clock Input Data Y	TTL	Pin 56	Pin 61
CLK P	Clock Product Register	TTL	Pin 23	Pin 28

Controls

The TMC2009 has eight control lines. TSX, TSM, and TSL are three-state enable lines for the XTP, the MSP, and the LSP, respectively. The output driver is in the high-impedance state when TSX, TSM, or TSL is HIGH, and enabled when the appropriate control is LOW.

PRELoad (PREL) is an active-HIGH control which has several effects when active (see Table 1). First, all output buffers are forced into the high-impedance state. Second, when any or all of TSX, TSM, and TSL are also HIGH, external data present at the output pins will be preloaded into the corresponding section of the output register on the rising edge of CLK P. Normal data setup and hold times apply both to the logical AND of PREL and the relevant three-state control (TSX, TSM, TSL), and to the data being preloaded. These setup and hold times are with respect to the rising edge of CLK P.

RouND (RND) controls the addition of a 1 to the MSB of the LSP for rounding. When RND is high, a 1 is added to the MSB of the LSP for rounding the product in the MSP and XTP (if appropriate) rather than truncating them.

Two's Complement (TC) controls how the device interprets data on the X and Y inputs. TC HIGH makes both inputs two's complement inputs, while TC LOW makes both inputs unsigned magnitude only inputs.

When ACCumulate (ACC) is HIGH, the content of the output register is added to or subtracted from the next product generated, and the result is stored back into the output registers at the next rising edge of CLK P. When ACC is LOW, multiplication without accumulation is performed, and the next product generated is stored into the output registers directly. This operation is used for the first term in a summation to eliminate the need for a separate "clear" operation.

The SUBtract (SUB) control is used in conjunction with the ACC control. When both the ACC and SUB controls are HIGH, the content of the output register is subtracted from the next product generated and the difference is stored back into the output register. Note that the previous output is subtracted from the product, not the product from the previous output.

Controls (Cont.)

The RND, TC, ACC, and SUB inputs are registered, with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J3 Package	C1, L1 Package
TSX	XTP Three-State Control	TTL	Pin 41	Pin 10
TSM	MSP Three-State Control	TTL	Pin 25	Pin 26
TSL	LSP Three-State Control	TTL	Pin 9	Pin 44
PREL	Preload Control	TTL	Pin 2	Pin 27
RND	Round Control Bit	TTL	Pin 8	Pin 45
TC	Two's Complement Control	TTL	Pin 42	Pin 9
ACC	Accumulate Control	TTL	Pin 6	Pin 47
SUB	Subtract Control	TTL	Pin 7	Pin 46

No Connects

The contact and leaded chip carrier versions of the TMC2009 have two pins which are not connected internally. These should be left unconnected.

Name	Function	Value	J3 Package	C1, L1 Package
NC	No Connection	Open	None	Pins 1, 34

Preload Truth Table 1

PREL[1]	TSX[1]	TSM[1]	TSL[1]	XTP	MSP	LSP
L	L	L	L	Register → Output pin	Register → Output pin	Register → Output pin
L	L	L	H	Register → Output pin	Register → Output pin	Hi-Z
L	L	H	L	Register → Output pin	Hi-Z	Register → Output pin
L	L	H	H	Register → Output pin	Hi-Z	Hi-Z
L	H	L	L	Hi-Z	Register → Output pin	Register → Output pin
L	H	L	H	Hi-Z	Register → Output pin	Hi-Z
L	H	H	L	Hi-Z	Hi-Z	Register → Output pin
L	H	H	H	Hi-Z	Hi-Z	Hi-Z
H[2]	L	L	L	Hi-Z	Hi-Z	Hi-Z
H[2]	L	L	H	Hi-Z	Hi-Z	Hi-Z Preload
H[2]	L	H	L	Hi-Z	Hi-Z Preload	Hi-Z
H[2]	L	H	H	Hi-Z	Hi-Z Preload	Hi-Z Preload
H[2]	H	L	L	Hi-Z Preload	Hi-Z	Hi-Z
H[2]	H	L	H	Hi-Z Preload	Hi-Z	Hi-Z Preload
H[2]	H	H	L	Hi-Z Preload	Hi-Z Preload	Hi-Z
H[2]	H	H	H	Hi-Z Preload	Hi-Z Preload	Hi-Z Preload

Notes:

1. PREL, TSX, TSM, and TSL are not registered.
2. PREL Hi inhibits any change of output register for those outputs in which the three-state control is LOW.

Figure 1. Fractional Two's Complement Notation

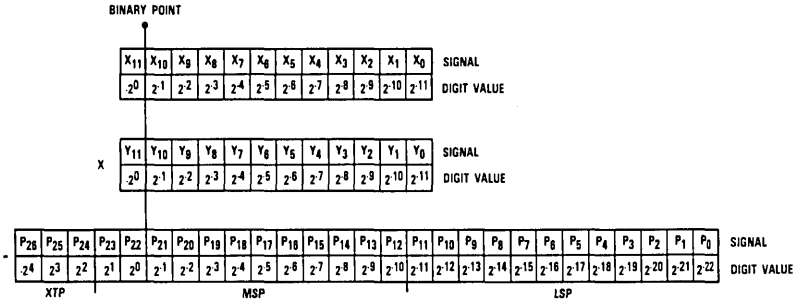


Figure 2. Fractional Unsigned Magnitude Notation

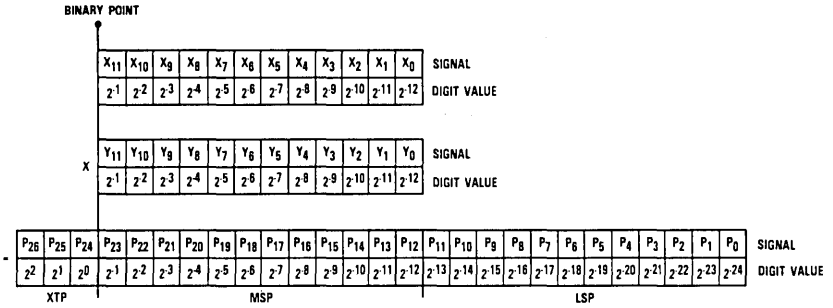


Figure 3. Integer Two's Complement Notation

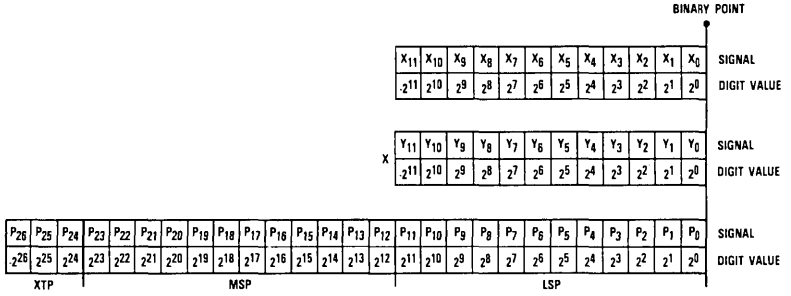
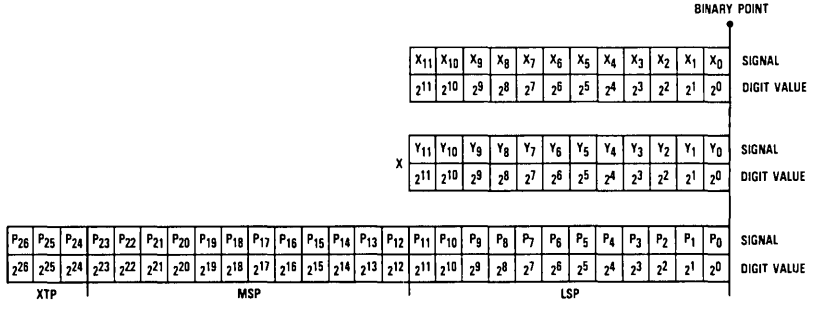


Figure 4. Integer Unsigned Magnitude Notation



H

Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} +0.5V)
Output	
Applied voltage	−0.5 to (V_{DD} +0.5V)[2]
Forced current	−1.0 to +6.0mA[3,4]
Short-circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PWL}	Clock Pulse Width, LOW	25			35			ns
t_{PWH}	Clock Pulse Width, HIGH	25			35			ns
t_S	Input Setup Time	25			30			ns
t_H	Input Hold Time	3			3			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		+125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = MAX, V_{IN} = 0V TSL, TSM, TSX = 5.0V		5		10	mA
I_{DDU}	Supply Current, Unloaded[1]	V_{DD} = MAX, F = 7.4MHz TSL, TSM, TSX = 5.0V		60		60	mA
I_{DDL}	Supply Current, Loaded[1, 2]	V_{DD} = MAX, F = 7.4MHz TSL, TSM, TSX = 0V Test Load: V_{LOAD} = V_{DD} MAX		150		170	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = MAX, V_I = 0.4V	−10	+10	−10	+10	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = MAX, V_I = 2.4V	−10	+10	−10	+10	μA
I_I	Input Current, Max Input Voltage	V_{DD} = MAX, V_I = V_{DD}		+75		+75	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = MIN, I_{OL} = MAX		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = MAX, V_I = 0.4V	−75	+75	−75	+75	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = MAX, V_I = 2.4V	−75	+75	−75	+75	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = MAX, Output HIGH, one pin to ground, one second duration max		−100		−100	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Notes:

1. Guaranteed to maximum clock rate, tested at 2MHz.
2. Worst case, all inputs and outputs toggling at maximum rate.

Switching characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MA}	Multiply-Accumulate Time	V_{DD} = MIN		135		170	ns
t_D	Output Delay	V_{DD} = MIN, Test Load: V_{LOAD} = 2.2V		40		45	ns
t_{ENA}	Three-State Output Enable Delay	V_{DD} = MIN, Test Load: V_{LOAD} = 1.5V		40		45	ns
t_{DIS}	Three-State Output Disable Delay	V_{DD} = MIN, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1}[2]		35		40	ns

Notes:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in figure 9.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

Figure 5. Timing Diagram

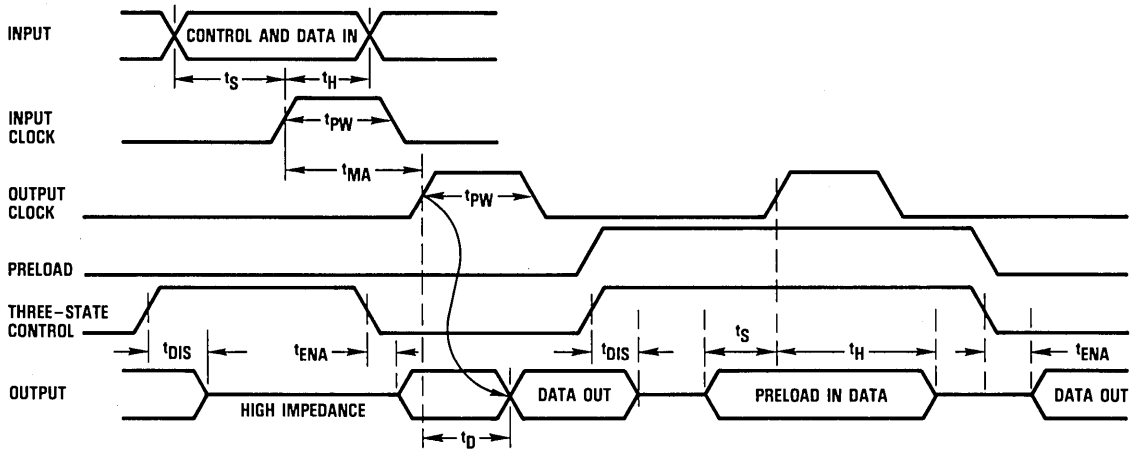


Figure 6. Equivalent Input Circuit

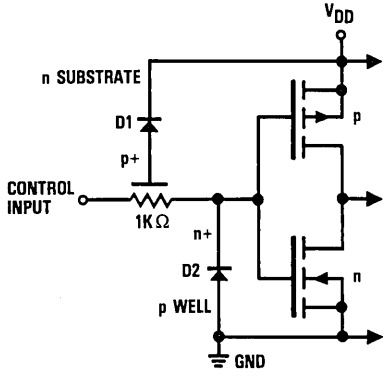


Figure 7. Equivalent Output Circuit

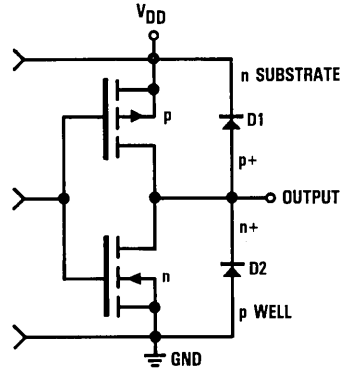


Figure 8. Test Load

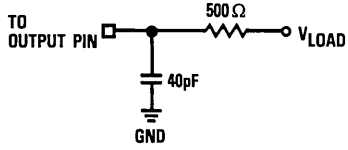
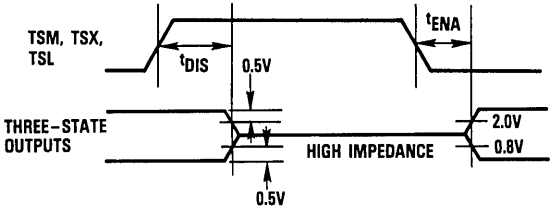


Figure 9. Transition Levels For Three-State Measurements



Application Notes

Multiplication By A Constant

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Selection Of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the TMC2009 does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 4.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2009J3C	STD – T_A = 0°C to 70°C	Commercial	64 Lead DIP	2009J3C
TMC2009J3G	STD – T_A = 0°C to 70°C	Commercial With Burn-In	64 Lead DIP	2009J3G
TMC2009J3F[1]	EXT – T_C = –55°C to 125°C	Commercial	64 Lead DIP	2009J3F
TMC2009J3A[1]	EXT – T_C = –55°C to 125°C	High Reliability[2]	64 Lead DIP	2009J3A
TMC2009C1C[1]	STD – T_A = 0°C to 70°C	Commercial	68 Contact Chip Carrier	2009C1C
TMC2009C1G[1]	STD – T_A = 0°C to 70°C	Commercial With Burn-In	68 Contact Chip Carrier	2009C1G
TMC2009C1F[1]	EXT – T_C = –55°C to 125°C	Commercial	68 Contact Chip Carrier	2009C1F
TMC2009C1A[1]	EXT – T_C = –55°C to 125°C	High Reliability[2]	68 Contact Chip Carrier	2009C1A
TMC2009L1C[1]	STD – T_A = 0°C to 70°C	Commercial	68 Leaded Chip Carrier	2009L1C
TMC2009L1G[1]	STD – T_A = 0°C to 70°C	Commercial With Burn-In	68 Leaded Chip Carrier	2009L1G
TMC2009L1F[1]	EXT – T_C = –55°C to 125°C	Commercial	68 Leaded Chip Carrier	2009L1F
TMC2009L1A[1]	EXT – T_C = –55°C to 125°C	High Reliability[2]	68 Leaded Chip Carrier	2009L1A

Notes:

1. Contact factory for availability.
2. Per TRW document 70Z01757.

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Preliminary Information describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact TRW for current information.

TMC2010
Preliminary Information

CMOS Multiplier–Accumulator
16 X 16 bit, 160ns

The TMC2010 is a high-speed 16 x 16 bit parallel multiplier-accumulator which operates at a 160 nanosecond cycle time (more than 6MHz multiply-accumulate rate). The input data may be specified as two's complement or unsigned magnitude, yielding a full-precision 32-bit product. Products may be accumulated to a 35-bit result.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The result is divided into a 3-bit eXTended Product (XTP), a 16-bit Most Significant Product (MSP), and a 16-bit Least Significant Product (LSP). Individual three-state output ports are provided for the XTP and the MSP; the LSP is multiplexed with the Y input. The output register can be preloaded directly via the output ports.

Built with TRW's state-of-the-art 2-micron CMOS process, the TMC2010 is pin and function compatible with the industry standard TDC1010 and operates with the same speed at one-sixth or less power dissipation, depending on the multiply-accumulate rate.

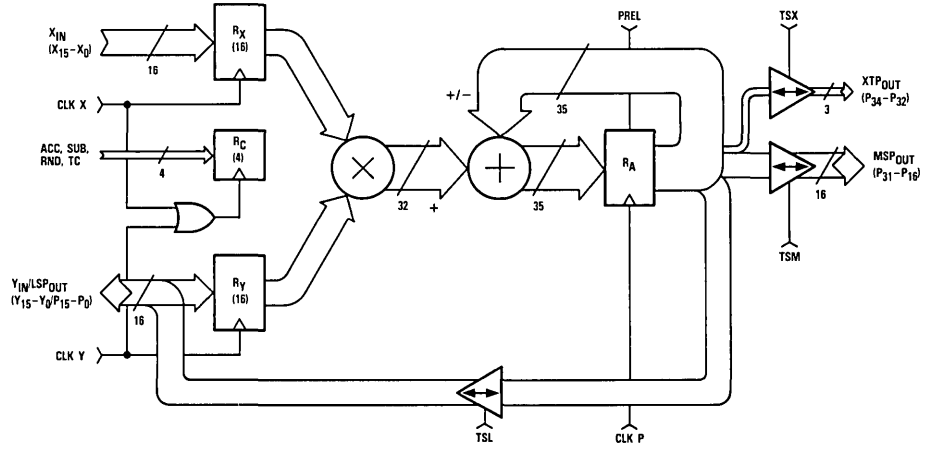
Features

- Low Power Consumption CMOS Process
- Pin And Function Compatible With TDC1010
- 160ns Multiply-Accumulate Time (Worst Case)
- 16 x 16 Bit Parallel Multiplication With Accumulation To 35-Bit Result
- Selectable Accumulation, Subtraction, Rounding, And Preloading
- All Inputs And Outputs Are Registered TTL Compatible
- Three-State Output
- Two's Complement Or Unsigned Magnitude Operation
- Single +5V Power Supply
- Available In 64 Lead DIP, 68 Contact Chip Carrier Or 68 Leaded Chip Carrier

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



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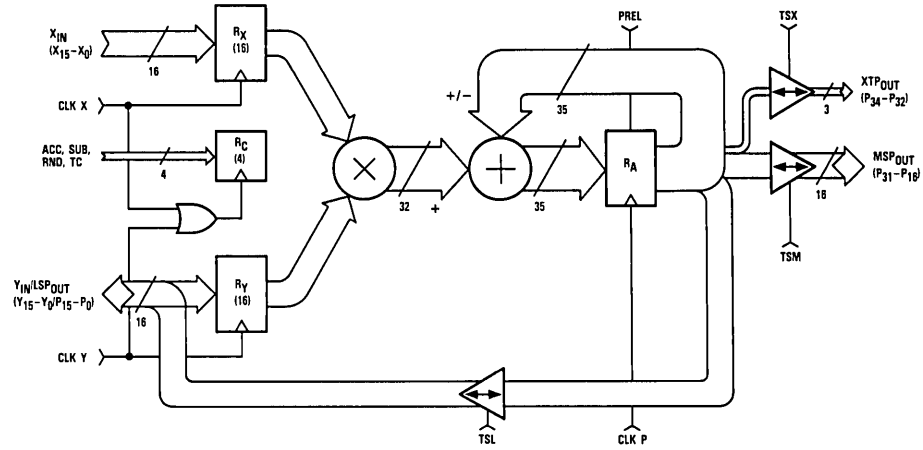
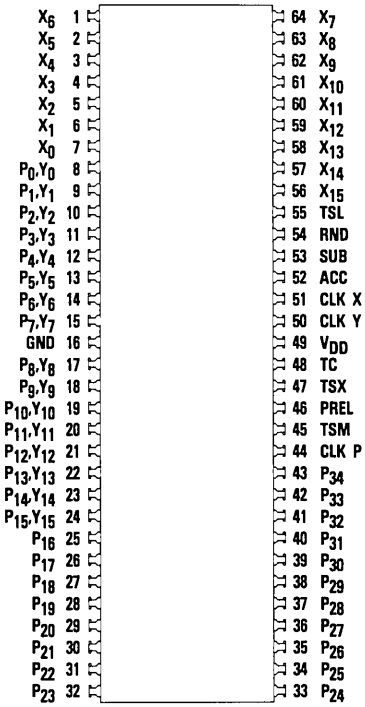
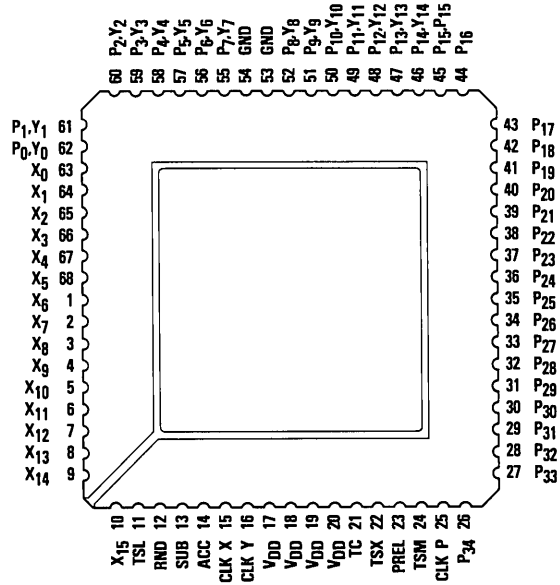
Functional Block Diagram



Pin Assignments



64 Lead DIP – J3 Package



68 Contact Or Leaded Chip Carrier – C1, L1 Package

Functional Description

General Information

The TMC2010 consists of four functional sections: Input registers, an asynchronous multiplier array, an adder, and output registers. The input registers store the two 16-bit numbers which are to be multiplied, and the control lines which control the input numerical format (two's complement or unsigned magnitude), output rounding, accumulation, and subtraction. The round control is used when a single-word output is desired. Each number is independently stored, simplifying multiplication by a constant. The output registers can be preloaded with a constant to provide the sum of products plus a constant. The asynchronous multiplier array is a network of AND gates and adders, which has been designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 16-bit words and one 3-bit word: the Most Significant Product (MSP), the Least Significant Product (LSP), and the eXTended Product (XTP). Three-state output drivers permit the TMC2010 to be used on a bus, or allow the outputs to be multiplexed over the same 16-bit output lines. The Least Significant Product (LSP) is multiplexed with the Y input.

Power

The TMC2010 operates from a single +5 Volt supply. All power and ground lines must be connected.

Name	Function	Value	J3 Package	C1, L1 Package
V_{DD}	Positive Supply Voltage	+5.0V	Pin 49	Pins 17, 18, 19, 20
GND	Ground	0.0V	Pin 16	Pins 53, 54

Data Inputs

The TMC2010 has two 16-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), X_{15} and Y_{15}, carry the sign information for the two's complement notation. The remaining bits are denoted X_{14} through X_0 and Y_{14} through Y_0 (with X_0 and Y_0 the Least Significant Bits). Data present at the X and Y inputs are clocked into the input registers at the rising edge of the appropriate clock. The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

Name	Function	Value	J3 Package	C1, L1 Package
X_{15}	X Data MSB	TTL	Pin 56	Pin 10
X_{14}		TTL	Pin 57	Pin 9
X_{13}		TTL	Pin 58	Pin 8
X_{12}		TTL	Pin 59	Pin 7
X_{11}		TTL	Pin 60	Pin 6
X_{10}		TTL	Pin 61	Pin 5
X_9		TTL	Pin 62	Pin 4
X_8		TTL	Pin 63	Pin 3
X_7		TTL	Pin 64	Pin 2
X_6		TTL	Pin 1	Pin 1
X_5		TTL	Pin 2	Pin 68
X_4		TTL	Pin 3	Pin 67
X_3		TTL	Pin 4	Pin 66
X_2		TTL	Pin 5	Pin 65
X_1		TTL	Pin 6	Pin 64
X_0	X Data LSB	TTL	Pin 7	Pin 63

Data Inputs (Cont.)

Name	Function	Value	J3 Package	C1, L1 Package
Y_{15}	Y Data MSB	TTL	Pin 24	Pin 45
Y_{14}		TTL	Pin 23	Pin 46
Y_{13}		TTL	Pin 22	Pin 47
Y_{12}		TTL	Pin 21	Pin 48
Y_{11}		TTL	Pin 20	Pin 49
Y_{10}		TTL	Pin 19	Pin 50
Y_9		TTL	Pin 18	Pin 51
Y_8		TTL	Pin 17	Pin 52
Y_7		TTL	Pin 15	Pin 55
Y_6		TTL	Pin 14	Pin 56
Y_5		TTL	Pin 13	Pin 57
Y_4		TTL	Pin 12	Pin 58
Y_3		TTL	Pin 11	Pin 59
Y_2		TTL	Pin 10	Pin 60
Y_1		TTL	Pin 9	Pin 61
Y_0	Y Data LSB	TTL	Pin 8	Pin 62

Data Outputs

The TMC2010 has a 35-bit two's complement or unsigned magnitude result that is the sum of the products of the two input data values and the previous products which have been accumulated. The output is divided into two 16-bit output words, the Most Significant Product (MSP) and Least Significant Product (LSP), and one 3-bit output word, the eXTended Product (XTP). The Most Significant Bit (MSB) of the XTP is the sign bit if two's complement notation is used. The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

Name	Function	Value	J3 Package	C1, L1 Package
P_{34}	Product MSB	TTL	Pin 43	Pin 26
P_{33}		TTL	Pin 42	Pin 27
P_{32}		TTL	Pin 41	Pin 28
P_{31}		TTL	Pin 40	Pin 29
P_{30}		TTL	Pin 39	Pin 30
P_{29}		TTL	Pin 38	Pin 31
P_{28}		TTL	Pin 37	Pin 32
P_{27}		TTL	Pin 36	Pin 33
P_{26}		TTL	Pin 35	Pin 34
P_{25}		TTL	Pin 34	Pin 35
P_{24}		TTL	Pin 33	Pin 36
P_{23}		TTL	Pin 32	Pin 37
P_{22}		TTL	Pin 31	Pin 38
P_{21}		TTL	Pin 30	Pin 39
P_{20}		TTL	Pin 29	Pin 40
P_{19}		TTL	Pin 28	Pin 41
P_{18}		TTL	Pin 27	Pin 42
P_{17}		TTL	Pin 26	Pin 43
P_{16}		TTL	Pin 25	Pin 44

Data Outputs (Cont.)

Name	Function	Value	J3 Package	C1, L1 Package
P_{15}		TTL	Pin 24	Pin 45
P_{14}		TTL	Pin 23	Pin 46
P_{13}		TTL	Pin 22	Pin 47
P_{12}		TTL	Pin 21	Pin 48
P_{11}		TTL	Pin 20	Pin 49
P_{10}		TTL	Pin 19	Pin 50
P_9		TTL	Pin 18	Pin 51
P_8		TTL	Pin 17	Pin 52
P_7		TTL	Pin 15	Pin 55
P_6		TTL	Pin 14	Pin 56
P_5		TTL	Pin 13	Pin 57
P_4		TTL	Pin 12	Pin 58
P_3		TTL	Pin 11	Pin 59
P_2		TTL	Pin 10	Pin 60
P_1		TTL	Pin 9	Pin 61
P_0	Product LSB	TTL	Pin 8	Pin 62

Clocks

The TMC2010 has three clock lines, one for each of the input registers and one for the product register. Data present at the inputs of these registers is loaded into the registers at the rising edge of the appropriate clock. The RouND (RND), Two's Complement (TC), ACCumulate (ACC) and SUBtract (SUB) inputs are registered, with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J3 Package	C1, L1 Package
CLK X	Clock Input Data X	TTL	Pin 51	Pin 15
CLK Y	Clock Input Data Y	TTL	Pin 50	Pin 16
CLK P	Clock Product Register	TTL	Pin 44	Pin 25

Controls

The TMC2010 has eight control lines. TSX, TSM, and TSL are three-state enable lines for the XTP, the MSP, and the LSP, respectively. The output driver is in the high-impedance state when TSX, TSM, or TSL is HIGH, and enabled when the appropriate control is LOW.

PRELoad (PREL) is an active-HIGH control which has several effects when active (see Table 1). First, all output buffers are forced into the high-impedance state. Second, when any or all of TSX, TSM, and TXL are also HIGH, external data present at the output pins will be preloaded into the corresponding section of the output register on the rising edge of CLK P. Normal data setup and hold times apply both to the logical AND of PREL and the relevant three-state control (TSX, TSM, TSL), and to the data being preloaded. These setup and hold times are with respect to the rising edge of CLK P.

RouND (RND) controls the addition of a 1 to the MSB of the LSP for rounding. When RND is HIGH, a 1 is added to the MSB of the LSP for rounding the product in the MSP and XTP (if appropriate) rather than truncating it.

Two's Complement (TC) controls how the device interprets data on the X and Y inputs. TC HIGH makes both inputs two's complement inputs, while TC LOW makes both inputs magnitude only inputs.

When ACCumulate (ACC) is HIGH, the content of the output register is added to or subtracted from the next product generated, and their sum is stored back into the output registers at the next rising edge of clock P. When ACC is LOW, multiplication without accumulation is performed, and the next product generated is stored into the output registers directly. This operation is used for the first term in a summation to eliminate the need for a separate "clear" operation.

The SUBtract (SUB) control is used in conjunction with the ACC control. When both the ACC and SUB controls are HIGH, the content of the output register is subtracted from the next product generated and the difference is stored back into the output register. Note that the previous output is subtracted from the product, not the product from the previous output.

The RND, TC, ACC, and SUB inputs are registered, with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J3 Package	C1, L1 Package
TSX	XTP Three-State Control	TTL	Pin 47	Pin 22
TSM	MSP Three-State Control	TTL	Pin 45	Pin 24
TSL	LSP Three-State Control	TTL	Pin 55	Pin 11
PREL	Preload Control	TTL	Pin 46	Pin 23
RND	Round Control Bit	TTL	Pin 54	Pin 12
TC	Two's Complement Control	TTL	Pin 48	Pin 21
ACC	Accumulate Control	TTL	Pin 52	Pin 14
SUB	Subtract Control	TTL	Pin 53	Pin 13

Figure 1. Fractional Two's Complement Notation

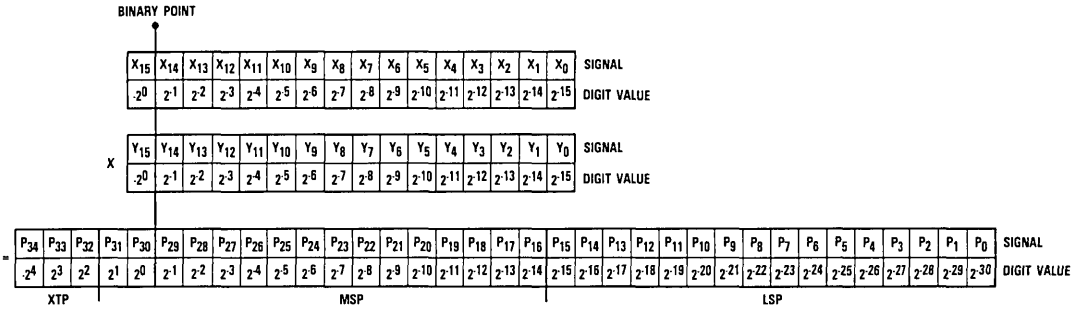


Figure 2. Fractional Unsigned Magnitude Notation

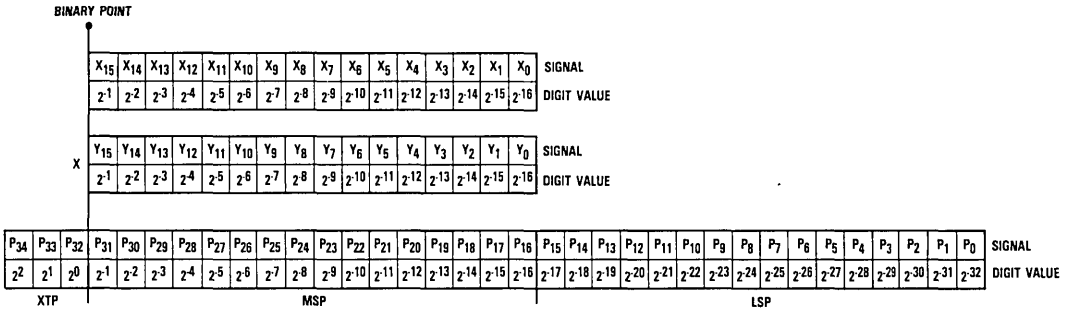


Figure 3. Integer Two's Complement Notation

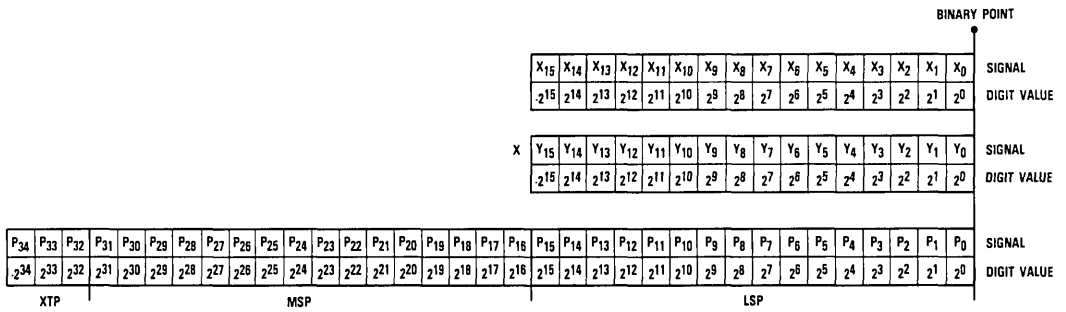
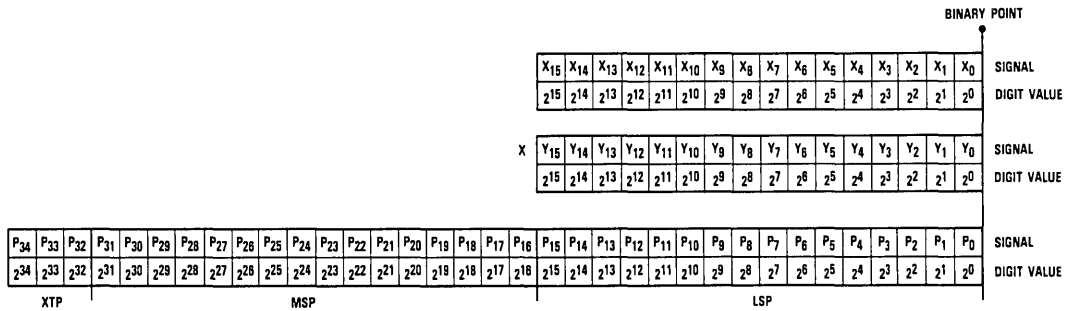


Figure 4. Integer Unsigned Magnitude Notation



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Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} +0.5V)
Output	
Applied voltage	−0.5 to (V_{DD} +0.5V)[2]
Forced current	−1.0 to +6.0mA[3,4]
Short-circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PWL}	Clock Pulse Width, LOW	25			30			ns
t_{PWH}	Clock Pulse Width, HIGH	25			30			ns
t_S	Input Setup Time	25			30			ns
t_H	Input Hold Time	3			3			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		+125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = MAX, V_{IN} = 0V TSL, TSM, TSX = 5.0V		5		10	mA
I_{DDU}	Supply Current, Unloaded[1]	V_{DD} = MAX, F = 6.2MHz TSL, TSM, TSX = 5.0V		60		60	mA
I_{DDL}	Supply Current, Loaded[1, 2]	V_{DD} = MAX, F = 6.2MHz TSL, TSM, TSX = 0V Test Load: V_{LOAD} = V_{DD} MAX		150		210	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = MAX, V_I = 0.4V					
		X_{IN}, Controls, Clocks	−10	+10	−10	+10	μA
		$\overline{Y}_{IN}$	−75	+75	−75	+75	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = MAX, V_I = 2.4V					
		X_{IN}, Controls, Clocks	−10	+10	−10	+10	μA
		$\overline{Y}_{IN}$	−75	+75	−75	+75	μA
I_I	Input Current, Max Input Voltage	V_{DD} = MAX, V_I = V_{DD}		+75		+75	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = MIN, I_{OL} = MAX		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = MAX, V_I = 0.4V	−75	+75	−75	+75	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = MAX, V_I = 2.4V	−75	+75	−75	+75	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = MAX, Output HIGH, one pin to ground, one second duration max		−100		−100	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Notes:

1. Guaranteed to maximum clock rate, tested at 2MHz.
2. Worst case, all inputs and outputs toggling at maximum rate.

Switching characteristics within specified operating conditions[1]

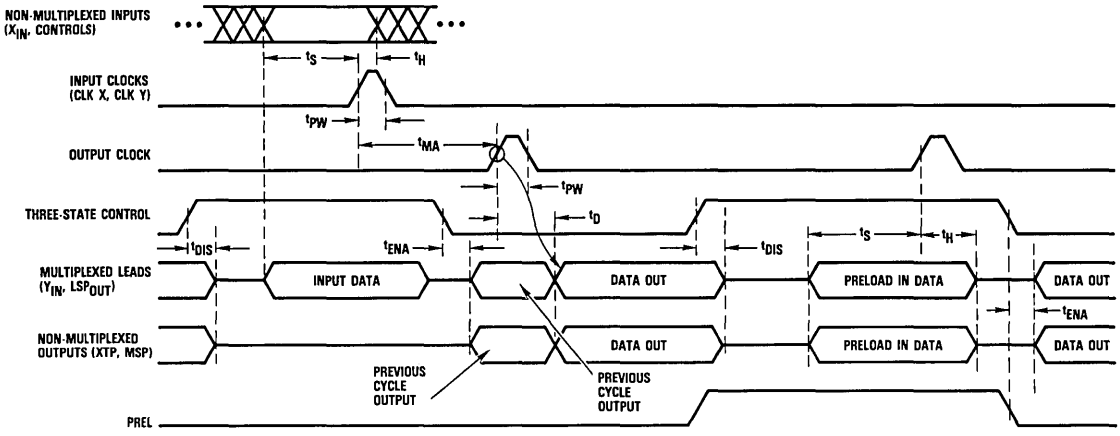
Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MA}	Multiply-Accumulate Time	V_{DD} = MIN		160		200	ns
t_D	Output Delay	V_{DD} = MIN, Test Load: V_{LOAD} = 2.2V		45		45	ns
t_{ENA}	Three-State Output Enable Delay	V_{DD} = MIN, Test Load: V_{LOAD} = 1.5V		40		45	ns
t_{DIS}	Three-State Output Disable Delay	V_{DD} = MIN, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1}[2]		35		45	ns

Notes:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in figure 9.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

H

Figure 5. Timing Diagram



Note: On multiplexed leads, input data and preload in data are applied to the TMC2010, and data out is produced and driven by the TMC2010.

Figure 6. Equivalent Input Circuit

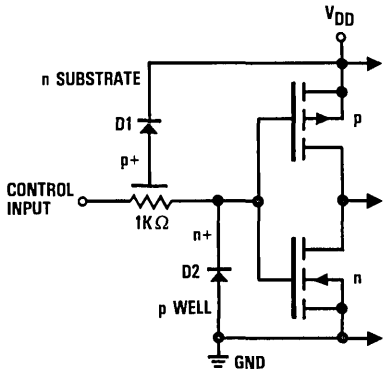


Figure 7. Equivalent Output Circuit

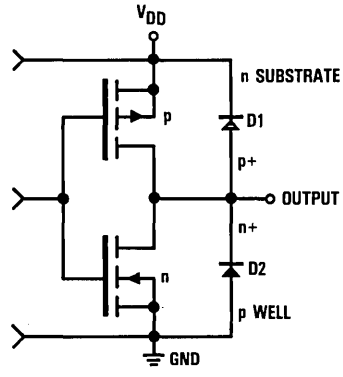


Figure 8. Test Load

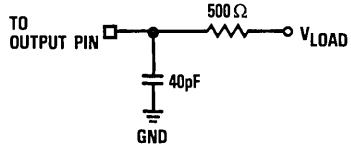
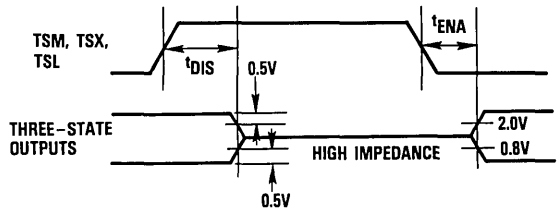


Figure 9. Transition Levels For Three-State Measurements



Preload Truth Table 1

PREL[1]	TSX[1]	TSM[1]	TSL[1]	XTP	MSP	LSP
L	L	L	L	Register→ Output Pin	Register→ Output Pin	Register→ Output Pin
L	L	L	H	Register→ Output Pin	Register→ Output Pin	Hi-Z
L	L	H	L	Register→ Output Pin	Hi-Z	Register→ Output Pin
L	L	H	H	Register→ Output Pin	Hi-Z	Hi-Z
L	H	L	L	Hi-Z	Register→ Output Pin	Register→ Output Pin
L	H	L	H	Hi-Z	Register→ Output Pin	Hi-Z
L	H	H	L	Hi-Z	Hi-Z	Register→ Output Pin
L	H	H	H	Hi-Z	Hi-Z	Hi-Z
H[2]	L	L	L	Hi-Z	Hi-Z	Hi-Z
H[2]	L	L	H	Hi-Z	Hi-Z	Hi-Z Preload
H[2]	L	H	L	Hi-Z	Hi-Z Preload	Hi-Z
H[2]	L	H	H	Hi-Z	Hi-Z Preload	Hi-Z Preload
H[2]	H	L	L	Hi-Z Preload	Hi-Z	Hi-Z
H[2]	H	L	H	Hi-Z Preload	Hi-Z	Hi-Z Preload
H[2]	H	H	L	Hi-Z Preload	Hi-Z Preload	Hi-Z
H[2]	H	H	H	Hi-Z Preload	Hi-Z Preload	Hi-Z Preload

Notes:

1. PREL, TSX, TSM, and TSL are not registered.
2. PREL Hi inhibits any change of output register for those outputs in which the three-state control is LOW.

Application Notes

Multiplication By A Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and that the desired register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection Of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the TMC2010 does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 4.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2010J3C	STD – T_A = 0°C to 70°C	Commercial	64 Lead DIP	2010J3C
TMC2010J3G	STD – T_A = 0°C to 70°C	Commercial With Burn-In	64 Lead DIP	2010J3G
TMC2010J3F[1]	EXT – T_C = -55°C to 125°C	Commercial	64 Lead DIP	2010J3F
TMC2010J3A[1]	EXT – T_C = -55°C to 125°C	High Reliability[2]	64 Lead DIP	2010J3A
TMC2010C1C[1]	STD – T_A = 0°C to 70°C	Commercial	68 Contact Chip Carrier	2010C1C
TMC2010C1G[1]	STD – T_A = 0°C to 70°C	Commercial With Burn-In	68 Contact Chip Carrier	2010C1G
TMC2010C1F[1]	EXT – T_C = -55°C to 125°C	Commercial	68 Contact Chip Carrier	2010C1F
TMC2010C1A[1]	EXT – T_C = -55°C to 125°C	High Reliability[2]	68 Contact Chip Carrier	2010C1A
TMC2010L1C[1]	STD – T_A = 0°C to 70°C	Commercial	68 Leaded Chip Carrier	2010L1C
TMC2010L1G[1]	STD – T_A = 0°C to 70°C	Commercial With Burn-In	68 Leaded Chip Carrier	2010L1G
TMC2010L1F[1]	EXT – T_C = -55°C to 125°C	Commercial	68 Leaded Chip Carrier	2010L1F
TMC2010L1A[1]	EXT – T_C = -55°C to 125°C	High Reliability[2]	68 Leaded Chip Carrier	2010L1A

Notes:

1. Contact factory for availability.
2. Per TRW document 70Z01757.

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Preliminary Information describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact TRW for current information.

TMC2110
Preliminary

CMOS Multiplier-Accumulator
16 X 16 bit, 100ns

The TMC2110 is a high-speed 16 x 16 bit parallel multiplier-accumulator which operates at a 100 nanosecond cycle time (10MHz multiply-accumulate rate). The input data may be specified as two's-complement or unsigned magnitude, yielding a full-precision 32-bit product. Products may be accumulated to a 35-bit result.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The result is divided into a 3-bit eXTended Product (XTP), a 16-bit Most Significant Product (MSP), and a 16-bit Least Significant Product (LSP). Individual three-state output ports are provided for the XTP and the MSP; the LSP is multiplexed with the Y input. The output register can be preloaded directly via the output ports.

Built with TRW's state-of-the-art 1-micron OMICRON-C™ CMOS process, the TMC2110 is pin and function compatible with the industry standard TDC1010, yet operates at more than 50% greater speed.

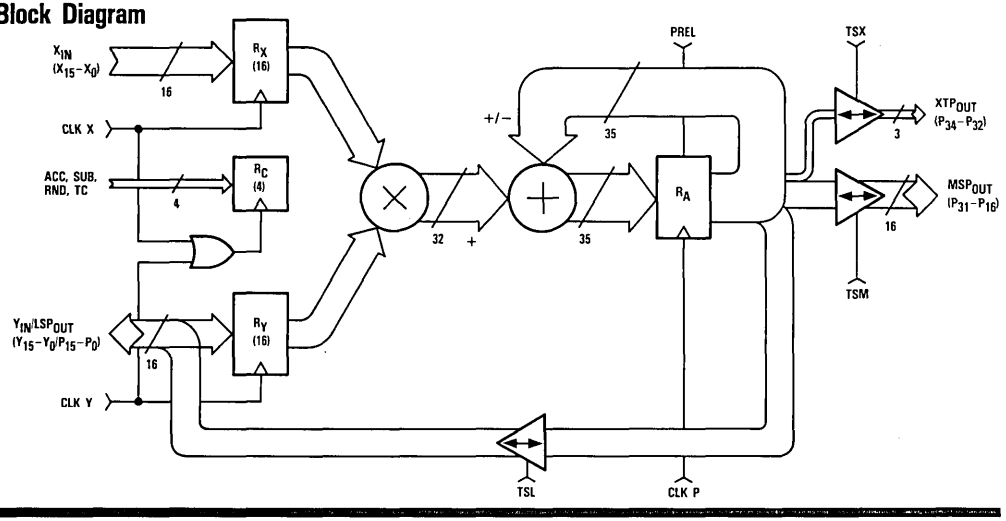
Features

- 100ns Multiply-Accumulate Time
- Pin And Function Compatible With TRW TDC1010 And TMC2010
- 16 x 16 Bit Parallel Multiplication With Accumulation To 35-Bit Result
- Selectable Accumulation, Subtraction, Rounding, And Preloading
- All Inputs And Outputs Are Registered TTL Compatible
- Three-State TTL Compatible CMOS Outputs
- Two's Complement Or Unsigned Magnitude Operation
- Low Power Consumption CMOS Process
- Single +5V Power Supply
- Available In A 64 Lead Ceramic DIP, 68 Contact Chip Carrier, Or 68 Leaded Chip Carrier

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



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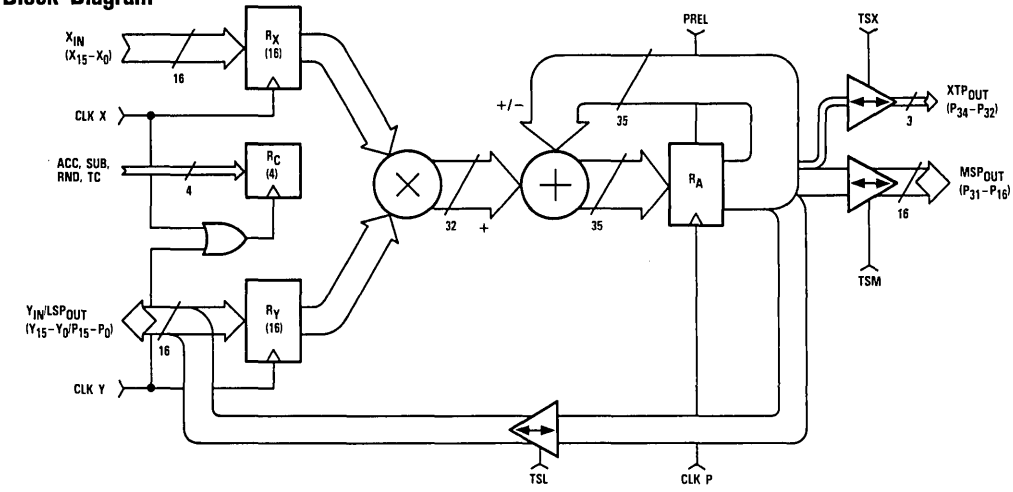
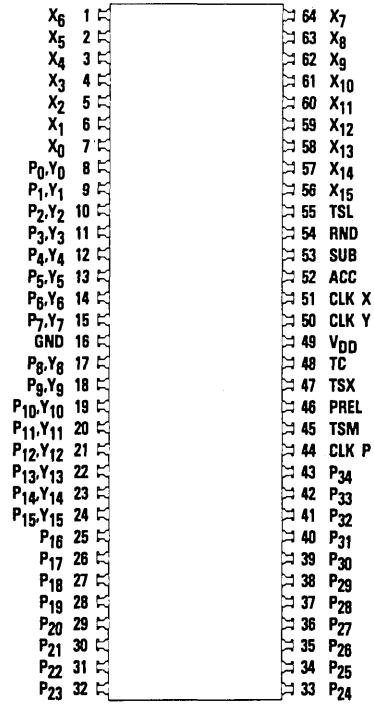
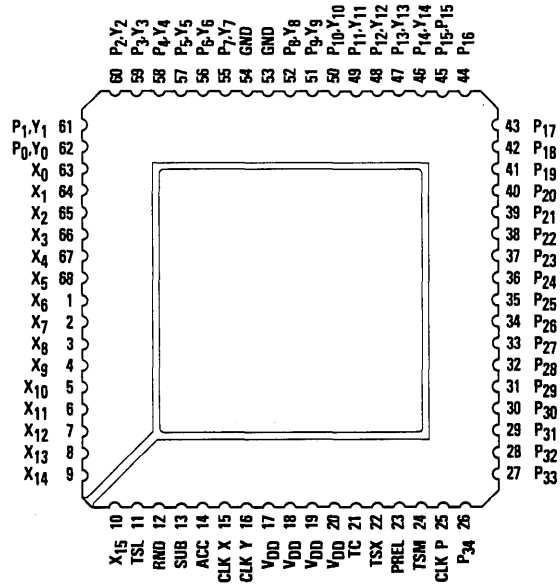
Functional Block Diagram



Pin Assignments



64 Lead DIP – J3 Package



68 Contact Or Leaded Chip Carrier – C1, L1 Package

Functional Description

General Information

The TMC2110 consists of four functional sections: input registers, an asynchronous multiplier array, an adder, and output registers. The input registers store the two 16-bit numbers which are to be multiplied, and the control lines which control the input numerical format (two's complement or unsigned magnitude), output rounding, accumulation, and subtraction. The round control is used when a single-word output is desired. Each number is independently stored, simplifying multiplication by a constant. The output registers can be preloaded with a constant to provide the sum of products plus a constant. The asynchronous multiplier array uses a modified Booth's algorithm, and has been designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 16-bit words and one 3-bit word: the Most Significant Product (MSP), the Least Significant Product (LSP), and the eXTended Product (XTP). Three-state output drivers permit the TMC2110 to be used on a bus, or allow the outputs to be multiplexed over the same 16-bit output lines. The Least Significant Product (LSP) is multiplexed with the Y input.

Power

The TMC2110 operates from a single +5 Volt supply. All power and ground lines must be connected.

Name	Function	Value	J3 Package	C1, L1 Package
V_{DD}	Positive Supply Voltage	+5.0V	Pin 49	Pins 17, 18, 19, 20
GND	Ground	0.0V	Pin 16	Pins 53, 54

Data Inputs

The TMC2110 has two 16-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_{15} and Y_{15}, carry the sign information when two's complement notation is used. The remaining bits are denoted X_{14} through X_0 and Y_{14} through Y_0 (with X_0 and Y_0 the Least Significant Bits). Data present at the X and Y inputs are clocked into the input registers at the rising edge of the appropriate clock. The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

Name	Function	Value	J3 Package	C1, L1 Package
X_{15}	X Data MSB	TTL	Pin 56	Pin 10
X_{14}		TTL	Pin 57	Pin 9
X_{13}		TTL	Pin 58	Pin 8
X_{12}		TTL	Pin 59	Pin 7
X_{11}		TTL	Pin 60	Pin 6
X_{10}		TTL	Pin 61	Pin 5
X_9		TTL	Pin 62	Pin 4
X_8		TTL	Pin 63	Pin 3
X_7		TTL	Pin 64	Pin 2
X_6		TTL	Pin 1	Pin 1
X_5		TTL	Pin 2	Pin 68
X_4		TTL	Pin 3	Pin 67
X_3		TTL	Pin 4	Pin 66
X_2		TTL	Pin 5	Pin 65
X_1		TTL	Pin 6	Pin 64
X_0	X Data LSB	TTL	Pin 7	Pin 63

Data Inputs (Cont.)

Name	Function	Value	J3 Package	C1, L1 Package
Y_{15}	Y Data MSB	TTL	Pin 24	Pin 45
Y_{14}		TTL	Pin 23	Pin 46
Y_{13}		TTL	Pin 22	Pin 47
Y_{12}		TTL	Pin 21	Pin 48
Y_{11}		TTL	Pin 20	Pin 49
Y_{10}		TTL	Pin 19	Pin 50
Y_{9}		TTL	Pin 18	Pin 51
Y_{8}		TTL	Pin 17	Pin 52
Y_{7}		TTL	Pin 15	Pin 55
Y_{6}		TTL	Pin 14	Pin 56
Y_{5}		TTL	Pin 13	Pin 57
Y_{4}		TTL	Pin 12	Pin 58
Y_{3}		TTL	Pin 11	Pin 59
Y_{2}		TTL	Pin 10	Pin 60
Y_{1}		TTL	Pin 9	Pin 61
Y_{0}	Y Data LSB	TTL	Pin 8	Pin 62

Data Outputs

The TMC2110 has a 35-bit two's complement or unsigned magnitude result that is the sum of the products of the two input data values and the previous products which have been accumulated. The output is divided into two 16-bit output words, the Most Significant Product (MSP) and Least Significant Product (LSP), and one 3-bit output word, the eXTended Product (XTP). The Most Significant Bit (MSB) of the XTP is the sign bit if two's complement notation is used. The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

Name	Function	Value	J3 Package	C1, L1 Package
P_{34}	Product MSB	TTL	Pin 43	Pin 26
P_{33}		TTL	Pin 42	Pin 27
P_{32}		TTL	Pin 41	Pin 28
P_{31}		TTL	Pin 40	Pin 29
P_{30}		TTL	Pin 39	Pin 30
P_{29}		TTL	Pin 38	Pin 31
P_{28}		TTL	Pin 37	Pin 32
P_{27}		TTL	Pin 36	Pin 33
P_{26}		TTL	Pin 35	Pin 34
P_{25}		TTL	Pin 34	Pin 35
P_{24}		TTL	Pin 33	Pin 36
P_{23}		TTL	Pin 32	Pin 37
P_{22}		TTL	Pin 31	Pin 38
P_{21}		TTL	Pin 30	Pin 39
P_{20}		TTL	Pin 29	Pin 40
P_{19}		TTL	Pin 28	Pin 41
P_{18}		TTL	Pin 27	Pin 42
P_{17}		TTL	Pin 26	Pin 43
P_{16}		TTL	Pin 25	Pin 44

Data Outputs (Cont.)

Name	Function	Value	J3 Package	C1, L1 Package
P_{15}		TTL	Pin 24	Pin 45
P_{14}		TTL	Pin 23	Pin 46
P_{13}		TTL	Pin 22	Pin 47
P_{12}		TTL	Pin 21	Pin 48
P_{11}		TTL	Pin 20	Pin 49
P_{10}		TTL	Pin 19	Pin 50
P_9		TTL	Pin 18	Pin 51
P_8		TTL	Pin 17	Pin 52
P_7		TTL	Pin 15	Pin 55
P_6		TTL	Pin 14	Pin 56
P_5		TTL	Pin 13	Pin 57
P_4		TTL	Pin 12	Pin 58
P_3		TTL	Pin 11	Pin 59
P_2		TTL	Pin 10	Pin 60
P_1		TTL	Pin 9	Pin 61
P_0	Product LSB	TTL	Pin 8	Pin 62

Clocks

The TMC2110 has three clock lines, one for each of the input registers and one for the product register. Data present at the inputs of these registers is loaded into the registers at the rising edge of the appropriate clock. The RouND (RND), Two's Complement (TC), ACCumulate (ACC), and SUBtract (SUB) inputs are registered, with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J3 Package	C1, L1 Package
CLK X	Clock Input Data X	TTL	Pin 51	Pin 15
CLK Y	Clock Input Data Y	TTL	Pin 50	Pin 16
CLK P	Clock Product Register	TTL	Pin 44	Pin 25

H

Controls

The TMC2110 has eight control lines. TSX, TSM, and TSL are three-state enable lines for the XTP, the MSP and the LSP, respectively. The output driver is in the high-impedance state when TSX, TSM, or TSL is HIGH, and enabled when the appropriate control is LOW.

PRELoad (PREL) is an active-HIGH control which has several effects when active (see Table 1). First, all output buffers are forced into the high-impedance state. Second, when any or all of TSX, TSM and TSL are also HIGH, external data present at the output pins will be preloaded into the corresponding section of the output register on the rising edge of CLK P. Normal data setup and hold times apply both to the logical AND of PREL and the relevant three-state control (TSX, TSM, TSL), and to the data being preloaded. These setup and hold times are with respect to the rising edge of CLK P.

RouND (RND) controls is the addition of a 1 to the MSB of the LSP for rounding. When RND is HIGH, a 1 is added to the MSB of the LSP for rounding the product in the MSP and XTP (if appropriate) rather than truncating it.

Two's Complement (TC) controls how the device interprets data on the X and Y inputs. TC HIGH makes both inputs two's complement inputs, while TC LOW makes both inputs unsigned magnitude only inputs. The necessary sign extension for negative two's complement numbers is provided internally.

When ACCumulate (ACC) is HIGH, the content of the output register is added to or subtracted from the next product generated, and the result is stored back into the output registers at the next rising edge of CLK P. When ACC is LOW, multiplication without accumulation is performed, and the next product generated will be stored into the output registers directly. This operation is used for the first term in a summation to eliminate the need for a separate "clear" operation.

The SUBtract (SUB) control is used in conjunction with the ACC control. When both the ACC and SUB controls are high, the content of the output register is subtracted from the next product generated and the difference is stored back into the output register. Note that the previous output is subtracted from the product, not the product from the previous output.

The RND, TC, ACC, and SUB inputs are registered, with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J3 Package	C1, L1 Package
TSX	XTP Three-State Control	TTL	Pin 47	Pin 22
TSM	MSP Three-State Control	TTL	Pin 45	Pin 24
TSL	LSP Three-State Control	TTL	Pin 55	Pin 11
PREL	Preload Control	TTL	Pin 46	Pin 23
RND	Round Control Bit	TTL	Pin 54	Pin 12
TC	Two's Complement Control	TTL	Pin 48	Pin 21
ACC	Accumulate Control	TTL	Pin 52	Pin 14
SUB	Subtract Control	TTL	Pin 53	Pin 13

Figure 1. Fractional Two's Complement Notation

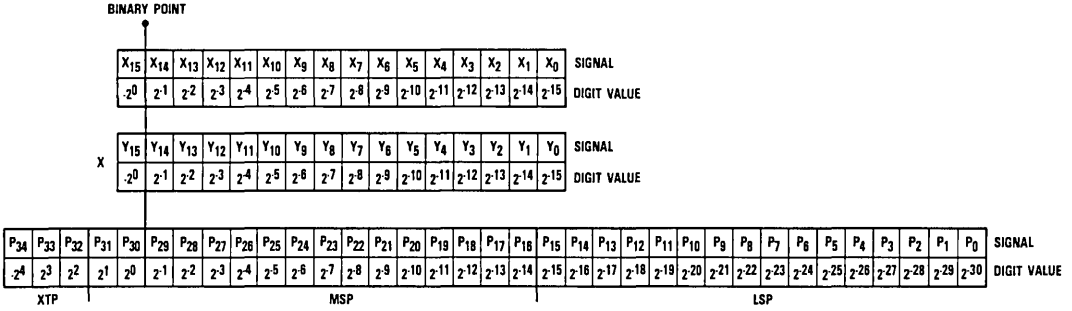


Figure 2. Fractional Unsigned Magnitude Notation

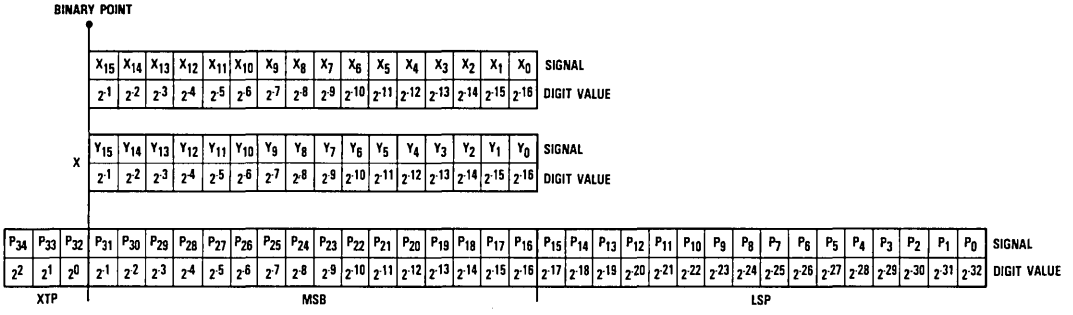


Figure 3. Integer Two's Complement Notation

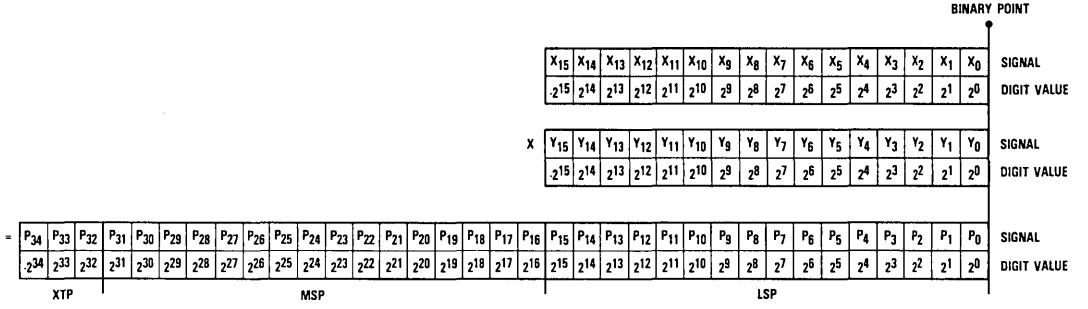
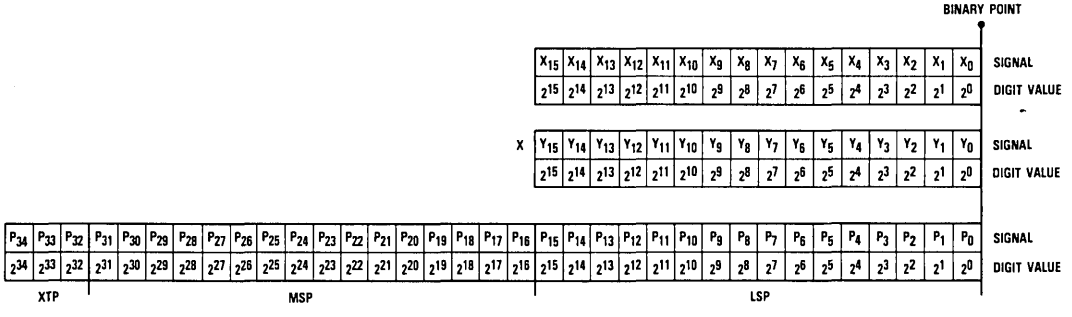


Figure 4. Integer Unsigned Magnitude Notation



Absolute maximum ratings (beyond which the device will be damaged)[1]

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5 to (V_{DD} +0.5V)

Output

Applied voltage ..... −0.5 to (V_{DD} +0.5V)[2]

Forced current ..... −1.0 to 6 mA[3,4]

Short-circuit duration (single output in high state to ground) ..... 1 sec

Temperature

Operating, case ..... −60 to +130°C

junction ..... 175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PWL}	Clock Pulse Width, LOW	25			30			ns
t_{PWH}	Clock Pulse Width, HIGH	25			30			ns
t_S	Input Setup Time	25			30			ns
t_H	Input Hold Time	0			3			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		+125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = MAX, V_{IN} = 0V TSL, TSM, TSX = 5.0V		10		10	mA
I_{DDU}	Supply Current, Unloaded[1]	V_{DD} = MAX, F = 10MHz TSL, TSM, TSX = 5.0V		100		100	mA
I_{DDL}	Supply Current, Loaded[1, 2]	V_{DD} = MAX, F = 10MHz TSL, TSM, TSX = 0V Test Load: V_{LOAD} = V_{DD} MAX		250		250	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = MAX, V_I = 0.4V					
		X_{IN}, Controls, Clocks	−10	+10	−10	+10	μA
		$\overline{Y}_{IN}$	−75	+75	−75	+75	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = MAX, V_I = 2.4V					
		X_{IN}, Controls, Clocks	−10	+10	−10	+10	μA
		$\overline{Y}_{IN}$	−75	+75	−75	+75	μA
I_I	Input Current, Max Input Voltage	V_{DD} = MAX, V_I = V_{DD}		+75		+75	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = MIN, I_{OL} = MAX		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi−Z Output Leakage Current, Output LOW	V_{DD} = MAX, V_I = 0.4V	−75	+75	−75	+75	μA
I_{OZH}	Hi−Z Output Leakage Current, Output HIGH	V_{DD} = MAX, V_I = 2.4V	−75	+75	−75	+75	μA
I_{OS}	Short−Circuit Output Current	V_{DD} = MAX, Output HIGH, one pin to ground, one second duration max		−100		−100	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		10		10	pF

Notes:

1. Guaranteed to maximum clock rate, tested at 2MHz.
2. Worst case, all inputs and outputs toggling at maximum rate.

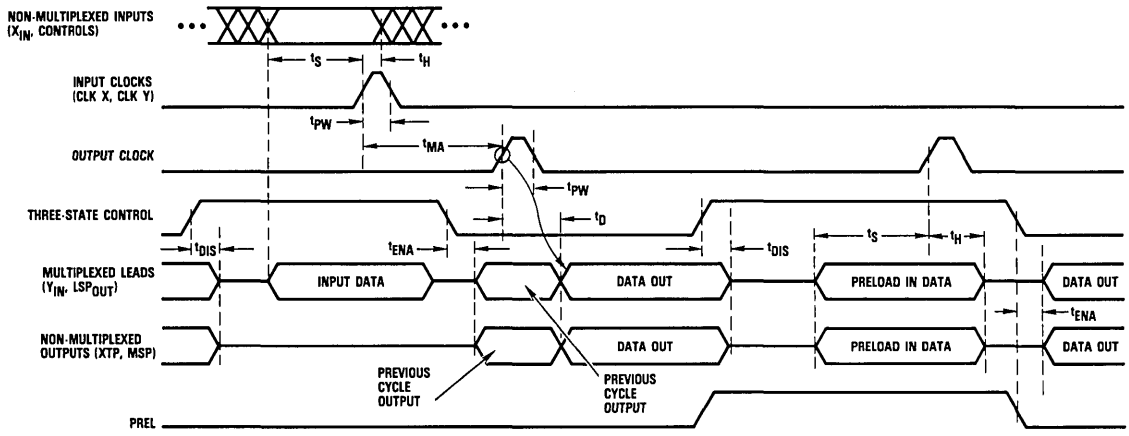
Switching characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MA}	Multiply−Accumulate Time	V_{DD} = MIN		100		120	ns
t_D	Output Delay	V_{DD} = MIN, Test Load: V_{LOAD} = 2.2V		35		40	ns
t_{ENA}	Three−State Output Enable Delay	V_{DD} = MIN, Test Load: V_{LOAD} = 1.5V		30		35	ns
t_{DIS}	Three−State Output Disable Delay	V_{DD} = MIN, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1}[2]		30		35	ns

Notes:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in figure 9.
2. t_{DIS1} denotes the transition from logical 1 to three−state.
   t_{DIS0} denotes the transition from logical 0 to three−state.

Figure 5. Timing Diagram



Note: On multiplexed leads, input data and preload in data are applied to the TMC2110, and data out is produced and driven by the TMC2110.

Figure 6. Equivalent Input Circuit

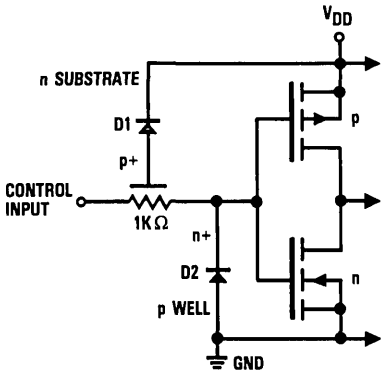


Figure 7. Equivalent Output Circuit

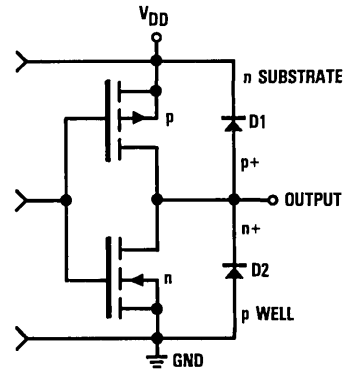


Figure 8. Test Load

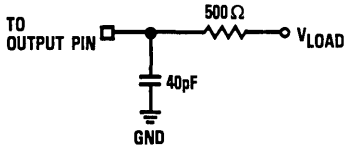
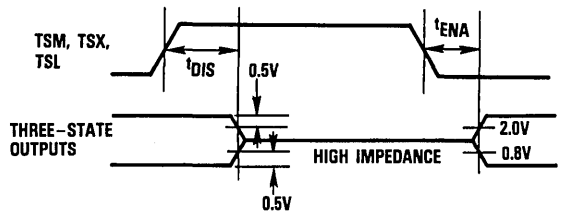


Figure 9. Transition Levels For Three-State Measurements



Preload Truth Table 1

PREL[1]	TSX[1]	TSM[1]	TSL[1]	XTP	MSP	LSP
L	L	L	L	Register-> Output Pin	Register-> Output Pin	Register-> Output Pin
L	L	L	H	Register-> Output Pin	Register-> Output Pin	Hi-Z
L	L	H	L	Register-> Output Pin	Hi-Z	Register-> Output Pin
L	L	H	H	Register-> Output Pin	Hi-Z	Hi-Z
L	H	L	L	Hi-Z	Register-> Output Pin	Register-> Output Pin
L	H	L	H	Hi-Z	Register-> Output Pin	Hi-Z
L	H	H	L	Hi-Z	Hi-Z	Register-> Output Pin
L	H	H	H	Hi-Z	Hi-Z	Hi-Z
H[2]	L	L	L	Hi-Z	Hi-Z	Hi-Z
H[2]	L	L	H	Hi-Z	Hi-Z	Hi-Z Preload
H[2]	L	H	L	Hi-Z	Hi-Z Preload	Hi-Z
H[2]	L	H	H	Hi-Z	Hi-Z Preload	Hi-Z Preload
H[2]	H	L	L	Hi-Z Preload	Hi-Z	Hi-Z
H[2]	H	L	H	Hi-Z Preload	Hi-Z	Hi-Z Preload
H[2]	H	H	L	Hi-Z Preload	Hi-Z Preload	Hi-Z
H[2]	H	H	H	Hi-Z Preload	Hi-Z Preload	Hi-Z Preload

Notes:

1. PREL, TSX, TSM, and TSL are not registered.
2. PREL Hi inhibits any change of output register for those outputs in which the three-state control is LOW.

Application Notes

Multiplication by a Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and that the register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the TMC2110 does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 4.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2110J3C	STD – T_A = 0°C to 70°C	Commercial	64 Lead DIP	2110J3C
TMC2110J3G	STD – T_A = 0°C to 70°C	Commercial With Burn-In	64 Lead DIP	2110J3G
TMC2110J3F[1]	EXT – T_C = –55°C to 125°C	Commercial	64 Lead DIP	2110J3F
TMC2110J3A[1]	EXT – T_C = –55°C to 125°C	High Reliability[2]	64 Lead DIP	2110J3A
TMC2110C1C[1]	STD – T_A = 0°C to 70°C	Commercial	68 Contact Chip Carrier	2110C1C
TMC2110C1G[1]	STD – T_A = 0°C to 70°C	Commercial With Burn-In	68 Contact Chip Carrier	2110C1G
TMC2110C1F[1]	EXT – T_C = –55°C to 125°C	Commercial	68 Contact Chip Carrier	2110C1F
TMC2110C1A[1]	EXT – T_C = –55°C to 125°C	High Reliability[2]	68 Contact Chip Carrier	2110C1A
TMC2110L1C[1]	STD – T_A = 0°C to 70°C	Commercial	68 Leaded Chip Carrier	2110L1C
TMC2110L1G[1]	STD – T_A = 0°C to 70°C	Commercial With Burn-In	68 Leaded Chip Carrier	2110L1G
TMC2110L1F[1]	EXT – T_C = –55°C to 125°C	Commercial	68 Leaded Chip Carrier	2110L1F
TMC2110L1A[1]	EXT – T_C = –55°C to 125°C	High Reliability[2]	68 Leaded Chip Carrier	2110L1A

Notes:

1. Contact factory for availability.
2. Per TRW document 70Z01757.

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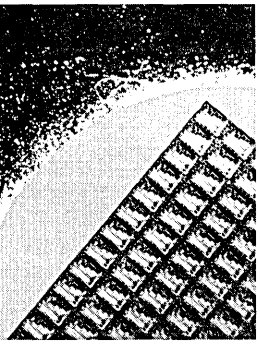
Preliminary Information describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact TRW for current information.

V L S I

D A T A

B O O K



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Product Indexes
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A/D Converters
Evaluation Boards
D/A Converters
Multipliers
Multiplier-Accumulators
Special Function Products
Memory/Storage Products
Reliability
Package Information
Glossary
Ordering Information
Application Notes And Reprints (Listings)

TRW LSI has several special function devices to address particular requirements found in digital signal processing. Floating point arithmetic has significant processing advantages over fixed point, specifically, a vastly improved dynamic range without excessive word size. Prior to the introduction of the TRW LSI floating point devices, performing floating point arithmetic required massive investments in hardware.

Correlation is a function frequently found in digital signal processing systems. Digital correlators provide a measure of the similarity between two signals.

Digital filtering often involves complex hardware; for even simple filtering functions, the sequencing of instructions can become difficult. The TDC1028 is an 8-tap finite impulse response (FIR) filter element which handles 4-bit data and coefficients and can be easily expanded in coefficient size, data size, and filter length.

The special function devices are all TTL compatible and are built using the triple-diffused bipolar technology.

Floating Point Devices

TRW LSI floating point hardware uses a 22-bit data format specifically suited to many digital signal processing applications. The 16-bit significand and 6-bit exponent are both two's complement numbers. This data format allows the full precision of the significand to be maintained over the dynamic range of the exponent (equivalent to 64 bits fixed point).

The TDC1022 floating point arithmetic unit performs the following floating point operations: addition, subtraction, normalization, and denormalization. The device has a feedback path for accumulation. Two 22-bit operands are accepted through an input port, the desired arithmetic operations are performed, and the output emerges through a three-state output port. Internal pipeline registers may be enabled to allow a 10MHz data throughput rate.

Correlators

A digital correlator is a device which measures, bit-by-bit, the congruence between two strings of bits, "reference" and "data." The output is a binary number tallying the number of matches between the two bit strings. A correlation score of zero indicates perfect anticorrelation, such that each "1" in the reference aligns with a "0" in the data stream, and vice-versa. Conversely, a maximum score indicates that each bit in the reference stream matches the corresponding bit in the data stream.

A digital correlator consists of two tapped shift registers, one for the data and one for the reference code. In the TDC1004 and TDC1023, each shift register is 64 taps long. At each tap, the contents of the reference register are exclusive-NORed with those of the data register; the 64 results are then tallied by a parallel counter. The output of the counter is the 6-bit binary-encoded correlation score, which runs between 0 and 64, inclusive.

Both correlators also include a masking function, which permits the user to eliminate any of the taps from consideration in the correlation score. For example, a 32-tap correlator can be built by masking off the last half of a TDC1004 or TDC1023, leaving only the first 32 taps active.

The TDC1023 offers the additional benefit of a reference preload/holding latch structure, in which the contents of the reference register can be stored. With the latch in this hold mode, the reference register can be preloaded with the next sequence. Returning the latch to its "track" mode reprograms the chip to correlate with the new (preloaded) reference sequence.

Digital Filter

The TDC1028 consists of eight 4-bit Multiply-ADd (MAD) cells, organized into a one-dimensional systolic array. The chip accommodates 4-bit data through its data input port, and outputs 13-bit sums at the same rate, through its SUM_{OUT} port. The TDC1028 performs the standard vector inner product or convolutional sum:

$$SUM_{OUT} = SUM_{IN} + aD(n) + bD(n\text{-}1) + \ldots + hD(n\text{-}7),$$

where a through h are the (preprogrammed) coefficients and the D(i) are the eight data values most recently clocked into the data input port.

The SUM_{IN} port permits the user to cascade the chips serially, to build either longer (more taps) or wider (greater resolution) filters from these "building block" chips. To facilitate parallel expansion, the data and coefficients have independent two's complement/unsigned magnitude controls.

Product	Description	Size	Power Clock Rate[1] (ns)	Dissipation (Watts)	Package	Notes
TDC1004	Correlator	64x1	100	0.7	J9	Analog current output
TDC1022	Floating Point Arithmetic Unit	22-Bit	100	4.7	J1	Two's complement
TDC1023	Correlator	64x1	60	1.8	J7	Binary digital output
TDC1028	FIR Filter	4x4x8	100	3.7	J4	8 Taps

Note: 1. Guaranteed, Worst Case, T_A = 0°C to 70°C.

TDC1004

Analog Output, Digital Correlator
64-bit

The TRW TDC1004 is a 64-bit digital correlator with a current source analog output. The device consists of three 64-bit, independently-clocked shift registers capable of a shift speed of 15MHz and a parallel correlation rate of 10MHz.

Correlation takes place when two binary words are serially shifted into the A and B registers. The two words are continually compared, bit for bit by exclusive-NOR (XNOR) circuits. Each XNOR circuit controls a current source. The current output of each current source is then summed to produce the correlation current that is proportional to the degree of correlation.

The third 64-bit shift register (M register) is provided to allow the user to mask or selectively choose "no compare" bit positions.

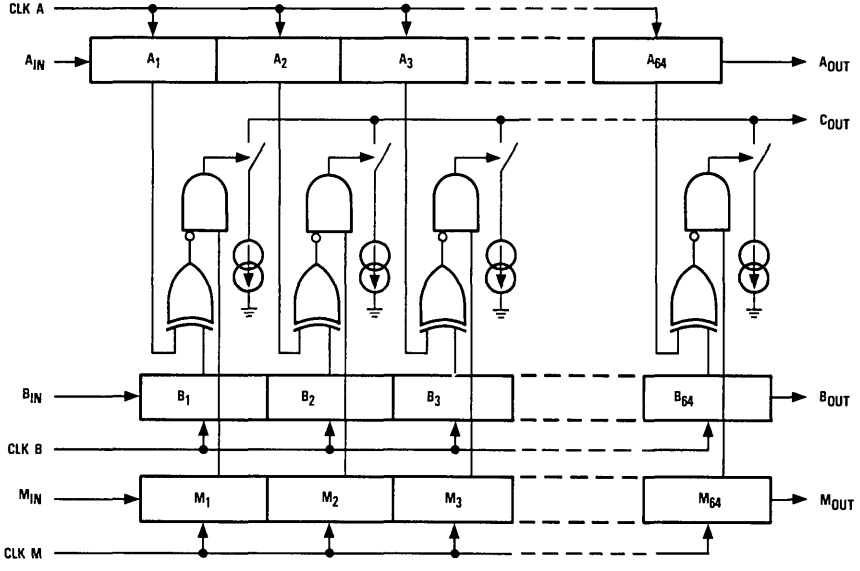
Features

- 10MHz Correlator Speed
- 15MHz Shift Speed (Static Shift Registers)
- Current Output
- Mask Register
- TTL Compatible
- Available In 16 Lead Ceramic DIP
- Radiation Hard
- 700mW Power Consumption

Applications

- Image Comparison/Recognition
- Bit/Word Synchronization
- Key Word Detection
- Error Correction Coding
- Radar And Sonar

Functional Block Diagram



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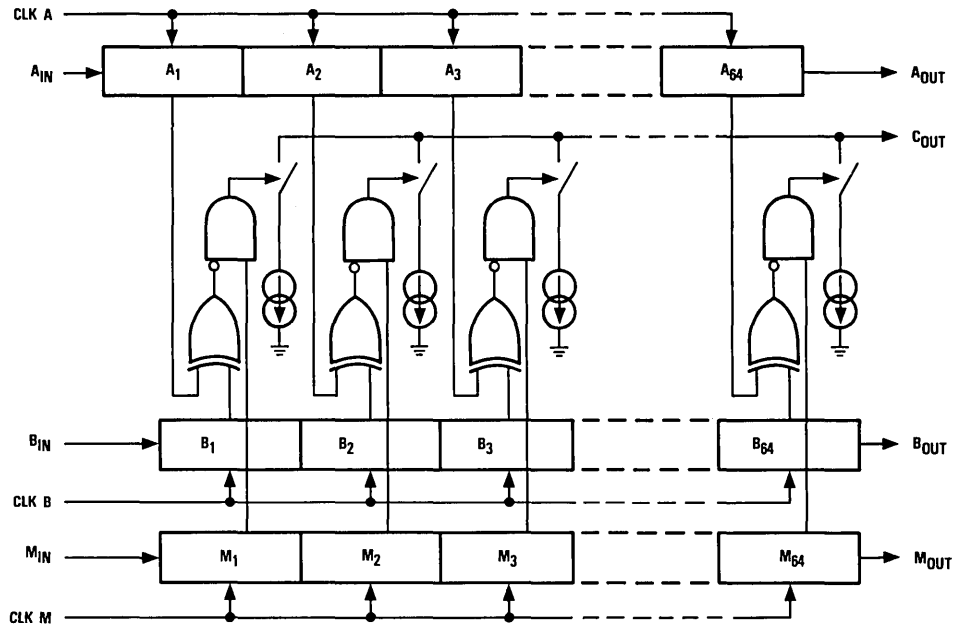
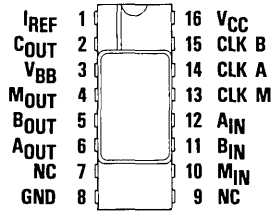
Functional Block Diagram



Pin Assignments



16 Lead DIP – J9 Package

Functional Description

General Information

The TDC1004 has three 64-bit long shift registers: A,B and M. Shift registers A and B are bit-by-bit XNORed (gate provides a true output if the two inputs are the same). The 64 results are then bit-by-bit ANDed with the M register. Each of the outputs of the AND gates are used to turn on one of the 64 equally weighted current sources whose outputs are summed to provide the analog correlation output.

Reference

The TDC1004 provides an output current of:

$I_{OUT} = N \times I_{BIT} + I_{COZ}$

where I_{BIT} is the individual bit output current, N is the number of correlating bits and I_{COZ} is the offset current.

By adjustment of I_{REF} as described in the calibration procedure, the mean bit current variation can be zeroed. I_{REF} is a current input. The voltage at this pin may vary from device to device due to input impedance variations.

Name	Function	Value	J9 Package
I_{REF}	Reference Current	350 μA	Pin 1

Correlation Output

The output of the TDC1004 is a current source at pin 2. The output stage consists of the collector of an NPN transistor whose base is connected to V_{BB}; it is therefore critical that the voltage at the output pin be kept 1.5V to 2.5V above V_{BB} to avoid saturation of this output transistor. V_{BB} should be set to a voltage level of V_{CC} + 1V ± 0.3VDC.

Name	Function	Value	J9 Package
C_{OUT}	Analog Output	300 to 3028 μA	Pin 2
V_{BB}	Base Bias Voltage	6V	Pin 3

Power

The TDC1004 operates from a +5.0V supply. A bias voltage of +6.0V is also required. Since less than 100 μA are drawn from this supply, a separate supply is not necessary and the V_{BB} can be provided by the circuit shown in Figure 6.

Name	Function	Value	J9 Package
V_{CC}	Supply Voltage	+5V	Pin 16
V_{BB}	Secondary Supply Voltage	+6V	Pin 3
GND	Electrical Ground	0V	Pin 8

Clocks

CLK A, CLK M, CLK B — Clock input pins for the A, M, and B registers, respectively. Each register may be independently clocked.

Name	Function	Value	J9 Package
CLK A	A Register Clock	TTL	Pin 14
CLK M	M Register Clock	TTL	Pin 13
CLK B	B Register Clock	TTL	Pin 15

Data Inputs

M_{IN} — Input to the M register. Allows the user to choose "no compare" bit positions. A "0" in any bit location will result in a no-compare state for that location.

A_{IN}, B_{IN} — Input to the A and B 64-bit serial shift registers.

Name	Function	Value	J9 Package
M_{IN}	Mask Register Input	TTL	Pin 10
A_{IN}	Shift Register Input	TTL	Pin 12
B_{IN}	Shift Register Input	TTL	Pin 11

Data Outputs

B_{OUT}, A_{OUT}, M_{OUT} — Outputs of the three 64-bit serial shift registers: B, A, and M, respectively.

Name	Function	Value	J9 Package
B_{OUT}	Shift Register B Output	TTL	Pin 5
A_{OUT}	Shift Register A Output	TTL	Pin 6
M_{OUT}	Shift Register M Output	TTL	Pin 4

No Connects

There are two leads labeled no connect (NC), which have no connections to the chip. These leads may be connected to ground for increased noise reduction.

Name	Function	Value	J9 Package
NC	No Connect	GND	Pins 7, 9

Figure 1. Timing Diagram

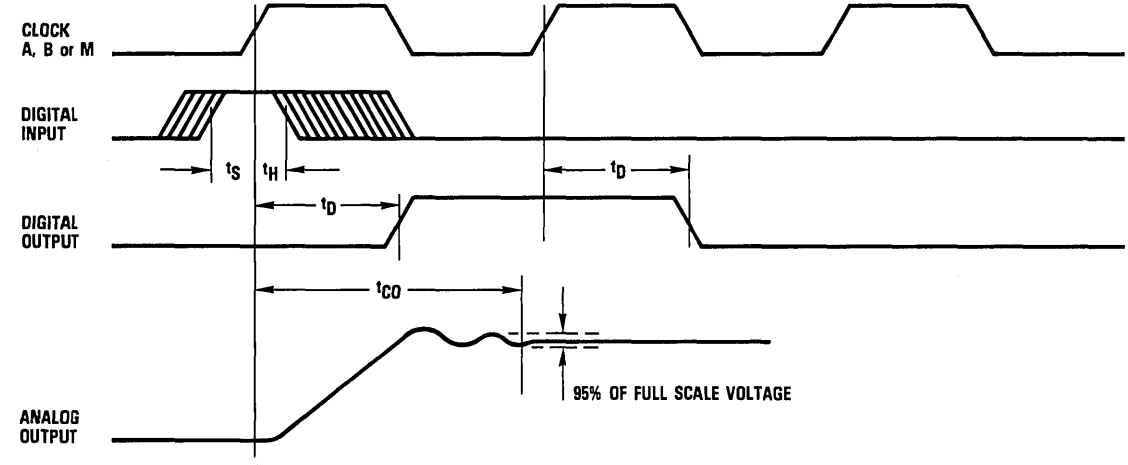


Figure 2. Analog Output Test Load

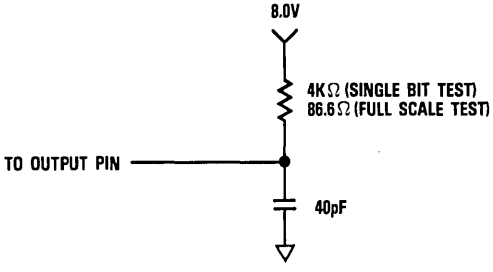
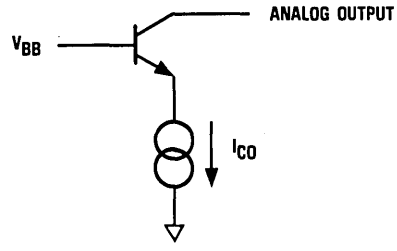


Figure 3. Analog Output Equivalent Circuit



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Current Source	
Reference signal, I_{REF}	5.0 mA
Input Voltage	
Data and Clock	0.0 to 5.5V
Output Voltage	
Digital outputs, A_{OUT}, B_{OUT}, M_{OUT}	0.0 to 5.5V
Analog output, C_{OUT}	V_{BB} to 8.5V
Applied voltage	−0.5 to 5.5V [2]
Applied current, externally forced	−1.0 to 6.0mA [3,4]
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, ambient	−55 to +150°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{BB}	Secondary Supply Voltage	5.7	6.0	6.3	5.7	6.0	6.3	V
I_{REF}	Reference Current		320	350		320	350	μA
V_{CO}	Analog Output Voltage	6.5	V_{BB}+2V	8.5	6.5	V_{BB}+2V	8.5	V
I_{COFS}	Full-Scale Analog Output Current	2.73		3.03	2.73		3.03	mA
t_{PW}	Clock Pulse Width	20			20			ns
t_S	Input Register Set-Up Time	20			20			ns
t_H	Input Register Hold Time	10			10			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
$V(I_{REF})$	Current Reference Voltage		2.2			2.2		V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Electrical characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = MAX		130		130	mA
$I(V_{BB})$	Secondary Supply Current			100		100	µA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = 4.0mA		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = −0.4mA	2.4		2.4		V
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_{IL} = 0.4V Clock		−4.0		−4.0	mA
		Data		−0.8		−0.8	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_{IH} = 2.4V Clock		200		200	µA
		Data		50		50	µA
I_{BIT}	Single-Bit Analog Output (Delta)	See Note 2	37	43	37	43	µA
I_{COZ}	Zero Correlation Analog Output (Offset)	See Note 2	300	340	300	340	µA

Notes:

1. Test conditions: V_{CC}, V_{BB}, I_{REF} = NOM, measured under DC conditions.
2. After calibration to I_{COFS} (Full-Scale Analog Output Current).

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{CO}	Analog Output Delay	See Figure 2		100		100	ns
t_D	Digital Propagation Delay	See Figure 1		65		65	ns
F_{SI}	Maximum Clock Frequency	Analog output	10		10		MHz
		Digital outputs	15		15		MHz

Application Notes

The TDC1004 is a 64-bit digital correlator with current source analog output. The device performs a bit-for-bit exclusive-OR correlation. In a mathematical sense the TDC1004 performs a convolution on 1-bit words which can be expressed in the general form:

$$y(k) = \sum_{n=1}^{N} k(n) \bullet x(n - k) \qquad \left[\begin{array}{l}\text{Logical 1} = +1 \\ \text{Logical 0} = -1\end{array}\right]$$

In some applications it may be useful to utilize the output current to generate a voltage source for threshold triggering. When converting the output to a voltage, insure that the voltage at the output pin remains above V_{BB} in order to avoid saturation of the output transistor. It is recommended that the voltage at C_{OUT} be in the range of 7.5V to 8.5V for a 6.0V V_{BB}. Two methods for achieving this are shown below:

Figure 4.

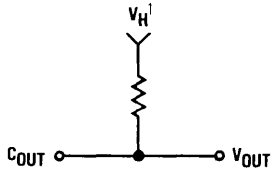
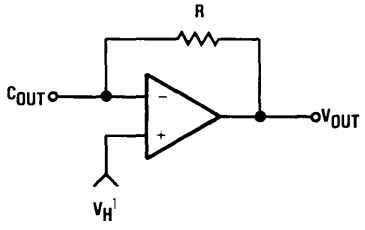


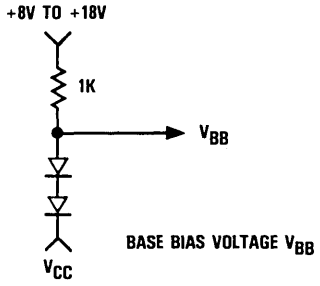
Figure 5.



Note: 1. $7.5V < V_H < 8.5V$

V_{BB} may be provided by the circuit shown below:

Figure 6.



Calibration

The TDC1004 requires two supplies (V_{BB} and V_{CC}) and a reference current source (I_{REF}) for proper operation. The voltage at the I_{REF} pin will vary from part to part due to differences in input impedance; hence, the source will be specified as a current source. The analog output current will be directly proportional to I_{REF}; therefore it is necessary to scale I_{REF} to minimize output error due to variations.

The total output current (I_{CON}) is equal to the number of correlation bits (N) times the individual bit currents (I_{BIT} = 40μA ± 3μA) plus the offset current (I_{COZ} = 320μA ± 20μA).

Therefore, the total output current can be expressed as:

$$I_{CON} = N \times I_{BIT} + I_{COZ}$$

As noted in the electrical characteristics, I_{BIT} and I_{COZ} vary separately over the temperature range; thus, by using the following procedure, I_{REF} can be adjusted to yield a statistically zero mean input current variation.

Calibrate I_{REF} as follows:

1) Set V_{BB} at V_{CC} + 1 ± 0.3V
2) Set I_{REF} to 320μA
3) Measure I_{COZ} (zero correlation analog output current)
4) Measure I_{COFS} (full scale correlation analog output)
5) Reset I_{REF} to:

$$* \text{ New } I_{REF} = \frac{2.56\text{mA}}{(I_{COFS} - I_{COZ})} \times \text{Old } I_{REF}$$

*This procedure may be done iteratively by taking the new I_{REF} and repeating steps 3 through 5.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1004J9C	STD-T_A = 0°C to 70°C	Commercial	16 Lead DIP	1004J9C
TDC1004J9G	STD-T_A = 0°C to 70°C	Commercial with Burn-In	16 Lead DIP	1004J9G
TDC1004J9F	EXT-T_C = -55°C to 125°C	Commercial	16 Lead DIP	1004J9F
TDC1004J9A	EXT-T_C = -55°C to 125°C	High Reliability[1]	16 Lead DIP	1004J9A

Note:

1. Per TRW document 70Z01757.

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TDC1022
Preliminary Information

Floating Point Arithmetic Unit
22-bit

The TDC1022 is a monolithic, 22-bit floating point arithmetic unit. Its operands are two 22-bit floating point numbers, each with a 16-bit two's complement significand and a two's complement 6-bit exponent. All data inputs and outputs, instruction bits, and controls are registered.

The TDC1022 allows parallel loading and outputting of data. Internal pipeline registers may be enabled to permit a throughput rate of 10MHz (100ns). Three-state output buffers are provided. All signals are TTL compatible.

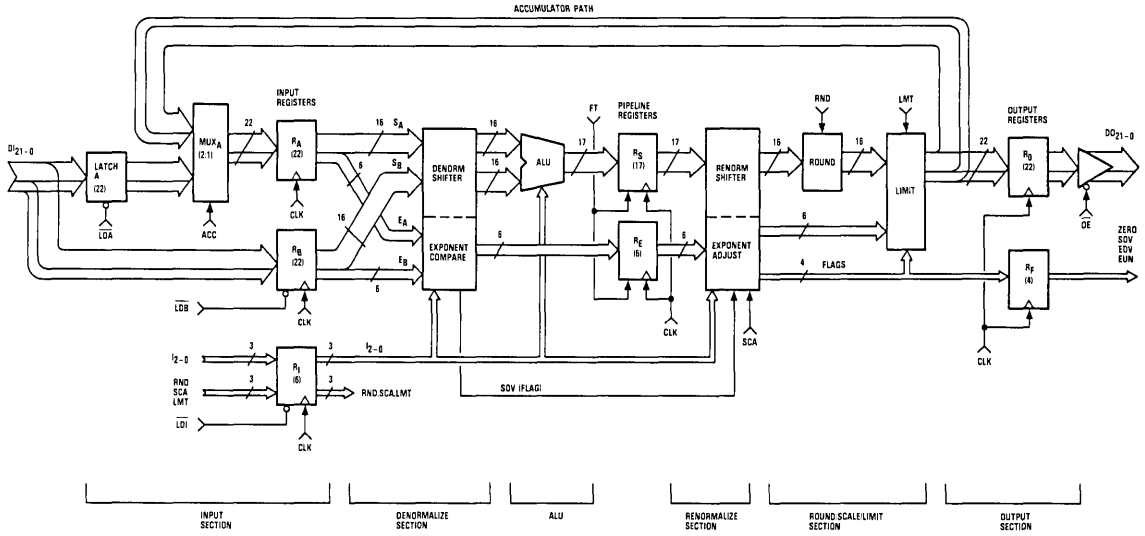
Features

- Two's Complement Floating Point Operation
- 100ns Pipelined Cycle Time
- Dynamic Range Equivalent To 64-Bit Fixed Point
- Parallel Data I/O Structure
- Selectable Pipelining
- Selectable Add/Accumulate Function
- Selectable Overflow/Underflow Characteristics
- Three-State TTL Outputs
- Available In 64 Lead DIP, 68 Contact Chip Carrier Or 68 Leaded Chip Carrier

Applications

- ALU In Array Processors
- Microprogrammed Signal Processors
- Conversion Between Fixed/Floating Point Numbers
- Floating Point Digital Filters And FFT's
- Geometric Transforms
- Image Processing

Functional Block Diagram



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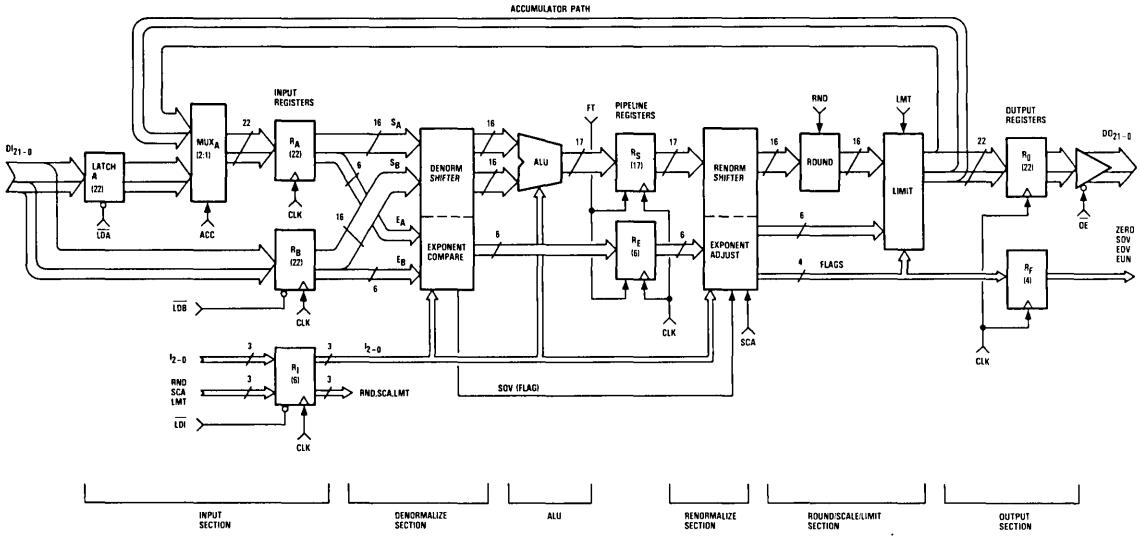
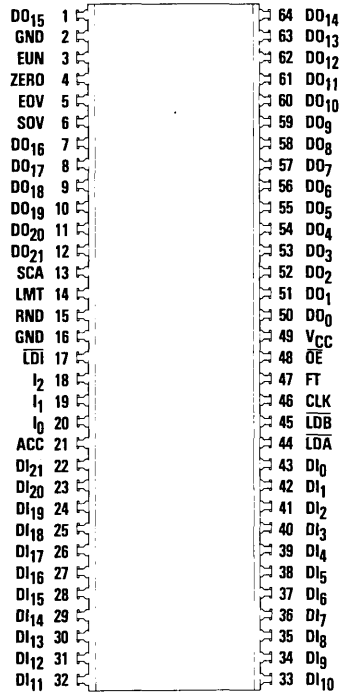
Functional Block Diagram



Pin Assignments



64 Lead DIP – J1 Package

Functional Description

General Information

The TDC1022 has six functional sections: input section, denormalizer, ALU, renormalizer, round/scale/limit section, and output section.

Two 22-bit floating point operands, along with the instructions and controls, are brought into the TDC1022 at the input section. When accumulate mode is selected, the operands are the result of the previous calculation.

The denormalizer selects the operand with the smaller exponent and downshifts its significand to compensate for the difference in exponents. The operands are then passed to the ALU.

The ALU performs the selected arithmetic function and passes its result to the renormalizer. Data pipeline registers located between the ALU and the renormalizer may be enabled to permit a throughput rate of 10MHz (100ns).

The renormalizer removes redundant leading bits (zeroes in the case of positive numbers, ones in the case of negative numbers) by upshifting the significand and decrementing the exponent accordingly. The number is normalized when the MSB and the next bit differ ($S15 \oplus S14 = 1$). Flags are generated in this section which are used by the limiter.

User selectable rounding, scaling (decrementing the exponent by one, thus performing division by two), and limiting functions are available. The adjusted result, along with the flags, then enters the output registers.

Input Section

The inputs to the TDC1022 are: data inputs DI_{21-0}, Latch A control ($\overline{LDA}$), enable signals for Registers B and I ($\overline{LDB}$, $\overline{LDI}$), mode controls ACCumulate (ACC) and Pipeline Register FeedThrough (FT), three ALU instruction bits (I_{2-0}), and three signals which control adjustment of the ALU result: RouND (RND), SCAle (SCA), and LiMiT (LMT). All inputs are registered except FT, ACC, and the register controls.

Operand Input

Input operands A and B are timeshared on one 22-bit input port. Latch A is provided before the input to Register A to allow for proper demultiplexing to Registers A and B. Latch A is transparent when $\overline{LDA}$ is low. Data A is clocked into Latch A at the rising edge of $\overline{LDA}$. MUX(A) selects between the contents of Latch A (ACC=0) and the result of the previous calculation (ACC=1) based on the state of the accumulate control, ACC. Register A is always loaded at the rising edge of CLK.

Register B inputs are also connected to the input port (DI_{21-0}). Register B is in hold mode when $\overline{LDB}$ is high, and is loaded at the rising edge of CLK when $\overline{LDB}$ is low.

Instruction and Control Input

The instruction register (Register I) accepts inputs I_{2-0}, RND, SCA, and LMT when $\overline{LDI}$ is low. When $\overline{LDI}$ is high, Register I is in hold mode. The rising edge of CLK loads Register I when $\overline{LDI}$ is low.

Denormalizer Section

Floating point addition is performed by forcing the two exponents to equal values and then adding the significands. The greatest accuracy is maintained by denormalizing the operand with the smaller exponent. This is done by right-shifting the significand n-places with sign-extension (downshifting), where n is the difference between the two exponents. The exponent of the denormalized operand is incremented by n, thereby equating the exponents. These internal operations are performed automatically by the TDC1022.

With 16-bit significands, the maximum allowable shift is 15 bits. If the exponents differ by 16 or more, the TDC1022 will yield a significand of zero (0.000 0000 0000 0000) when denormalizing a positive number and a significand of −1 LSB (1.111 1111 1111 1111) when denormalizing a negative number. All bits shifted beyond the LSB position are truncated.

After denormalization, the two significands are passed to the ALU where the selected arithmetic function is performed.

ALU Section

Operation of the ALU section is controlled exclusively by the ALU instruction microcode, I_{2-0}. The 17 bit significand emerging from the ALU (which includes one overflow bit) enters the significand pipeline register (Register S), and the exponent enters the exponent pipeline register (Register E). These registers may be made transparent by asserting the feedthrough control (FT=1); they are functional when FT=0. Note that there is no pipeline register for the instructions. Detailed discussion of the pipelined mode is provided at the end of the ALU functional description. The eight ALU instructions are described below.

ALU Instructions

Instruction	I_2	I_1	I_0	Name
0	0	0	0	ZERO
1	0	0	1	A + B
2	0	1	0	A - B
3	0	1	1	B - A
4	1	0	0	Normalize B
5	1	0	1	Normalize (-B)
6	1	1	0	Denormalize A
7	1	1	1	Denormalize (-A)

Zero

Both the A and B data fields are forced to ZERO (exponent = 100 000, significand = 0.000 0000 0000 0000). The contents of the input registers are unchanged. The ZERO flag is set high, and the final output is 0.0×2^{-32}.

A + B

The ALU adds the significands after the operand with the smaller exponent has been denormalized. Round should be enabled (RND=1) in this mode.

A−B

The operand with the smaller exponent is denormalized. Negative B is generated in two's complement form by one's complementing the B significand, then adding 1 LSB. This addition of 1 LSB is necessary due to the asymmetric nature of the two's complement number line and is called adding a "hot-one". The significands (A and −B) are then added. The rounding function must be disabled during subtraction (RND=0).

B−A

This operation is the same as A−B, except the operands are reversed. As before, the rounding function must be disabled during subtraction.

Normalize B

This function is used to normalize a number entering the B data field. The A operand is forced to ZERO (0.0 x 2^{-32}) to ensure that B passes through the denormalizer unchanged. The ALU does not affect the B operand, which is passed through to the renormalizer. Redundant leading ones (negative numbers) or leading zeroes (positive numbers) are removed by left-shifting (upshifting) the significand while decrementing the exponent, thereby normalizing the number. The number is normalized when the MSB of the significand does not match the next lower bit (see Data Format, page 315). If B is already a normalized floating point number, this instruction is effectively a "pass-through." If B is an unnormalized floating point number, the TDC1022 will attempt to normalize it, generating an Exponent UNderflow flag (EUN) if the exponent exceeds its maximum negative value. This instruction would be most frequently used to convert a fixed point number into a floating point number.

Normalize (-B)

The B significand is one's complemented and a "hot-one" is added to the LSB, generating -B in two's complement form. This result is normalized as in the preceding instruction.

Denormalize A

This is used to convert a floating point number, A, to a fixed point number scaled by B. The B significand is zeroed, but not the B exponent. If the A exponent is less than the B exponent, the denormalizer downshifts the A significand up to 15 places. Beyond shifts of 15 places, positive significands become zero and negative significands become -1 LSB. If the A exponent exceeds the B exponent, the Significand OVerflow flag (SOV) is set. In this case, the significand output remains unchanged. This instruction disables the renormalizer section.

Execution of the Denormalize instructions in pipelined mode must be handled carefully. Since the instructions are not pipelined, it is necessary to execute a "fill" instruction (e.g., same instruction repeated), prior to start of Denormalization to avoid interfering with other data going through the pipeline. The first result will be undefined; the true denormalized results start to emerge after the second result. It is also necessary to execute an extra denormalize instruction after the final desired denormalization to prevent the renormalize shifter from being enabled. The result of the calculation after the final denormalize will again be undefined. Basically, when doing the denormalize instruction n-times, n+1 denormalize instructions must be executed. Note that the SOV flag is generated before the pipeline register, and since there is no pipeline register for the flag, it will emerge one clock cycle ahead of the data it represents. This will cause improper functioning of the limit section; the result of the calculation previous to the one causing the overflow will be limited in this case (when LMT=1). Additionally, the overflow case will be passed through without being limited, since the SOV flag has already taken its effect.

Denormalize (-A)

The A significand is one's complemented and the "hot-one" is added to the LSB, creating -A in two's complement. This result is denormalized as in instruction Denormalize A. Note that the case where this instruction is executed with the A significand = 1.000 0000 0000 0000, and the A exponent = B exponent is undefined.

This is due to the fact that -(-1) = +1 is not representable in two's complement. This case will generate the SOV flag. The ZERO flag is set when Denormalize (-A) is executed with A = -1 any time the A exponent is greater than or equal to the B exponent. In these cases, a clean zero (0.0 X 2^{-32}) is the output. Attempting to Denormalize (-A) for A = -1, where the A exponent is 16 or more than the B exponent, results in the output of the B exponent, a significand of +1 LSB, and no flags are set. Use of the Denormalize (-A) in pipelined mode causes the same situations which occur when Denormalize A is executed (see above).

Operation of the TDC1022 in Pipelined Mode

There is no pipeline register for I_{2-0}, RND, SCA, and LMT. As a result, when the TDC1022 is operated in pipelined mode, the RND, SCA, and LMT functions must be delayed one clock cycle from the data and instructions (I_{2-0}) with which they are associated for proper operation. This is true since these functions take effect after the pipeline registers, which delay the data resulting from execution of ALU instructions on the input operands. RND, SCA, and LMT affect the results of the ALU output on the current clock cycle, which is the result of the previous calculation when pipeline mode is used.

Use of the Denormalize instructions in pipelined mode is covered under the description of instruction "Denormalize A," in the ALU instructions.

Changing the instructions when in pipelined mode requires consideration of all the above mentioned facts. Changing states on the FeedThrough control (FT) is not permitted.

Renormalizer Section

The significand result emerging from the ALU is examined for possible positive or negative overflow into the 17th bit. If overflow is detected, the renormalization logic downshifts the significand one bit while incrementing the exponent by one. The resulting number is then assured to be a normalized number.

If no overflow is detected, the renormalize section removes redundant leading zeroes of positive numbers (leading ones of negative numbers) by upshifting the significand and decrementing the exponent. This process is continued until the number is normalized, which means that the MSB and the next bit are different (see also Data Format, page 315).

The TDC1022 will always produce a normalized number as the final output, except when either Denormalize A or Denormalize (−A) is executed. This is true regardless of the states of RND, SCA, and LMT.

All flags except the Significand OVerflow (SOV) flag are generated in this section. Upon completion of rounding and scaling, the flags may need to be set. This is handled in the next section. The renormalized number and the flags are passed directly to the round/scale/limit section.

Flag Generation

EOV — The EOV flag is set high (EOV=1) when the exponent exceeds its maximum positive value of +31.

EUN — The EUN flag is set high (EUN=1) when the exponent drops below its maximum negative value of −32.

ZERO — The ZERO flag is set high (ZERO=1) when the significand is zero due to the subtraction of two identical significands, the execution of instruction ZERO, or Denormalization of positive numbers where the significand is shifted beyond the LSB. The ZERO flag is also set when Denormalize (−A) is executed where A = −1 and the A exponent is greater than or equal to the B exponent. When the ZERO flag is set, a clean zero is always output.

SOV — The SOV flag can only be set high (SOV=1) when either instruction Denormalize A or Denormalize (−A) is executed. If either of these instructions is executed and the A (data) exponent exceeds the B (seed) exponent, the SOV flag will go high. The only other way to set SOV high is to execute Denormalize (−A) with the A exponent greater than or equal to the B exponent, and an A significand of −1. In this case, the ZERO flag is erroneously set and the TDC1022 outputs a clean zero. In any normalized mode, the significand cannot overflow.

Round/Scale/Limit Section

The round/scale/limit section operates on the normalized floating point number passed to it from the renormalizer. The operations of rounding and scaling occur before the limit function, since it is possible for rounding and scaling to generate exponent overflows or underflows. The flags (SOV, EOV, EUN, ZERO) are used by the limit section to produce the appropriate result of maximum positive, maximum negative, or zero. In pipelined mode, the controls RND, SCA, LMT must be delayed one clock cycle from the data which they are to influence. The output of the limit section, along with the flags, goes directly to the output registers.

Rounding

When the round control is high (RND=1), the TDC1022 adds a 1 to the 1/2 LSB position. This results in a carry propagation into the LSB if there was a 1 in the 1/2 LSB position.

Scaling

When the scale (divide by two) control is high (SCA=1), the exponent is decremented by one, resulting in a division by two. Note that if the exponent is −32 and SCA=1, the EUN flag would be set and if the limiter is turned off (LMT=0), the resulting exponent is +31. This condition would produce the correct result of ZERO (0.0×2^{-32}) if the limiter is enabled (LMT=1).

Limiting

When the limit function is disabled (LMT=0), the significand and exponent retain their two's complement characteristics upon overflow; adding one to maximum positive numbers return maximum negatives, and subtracting one from maximum negative yields maximum positives.

When the limit function is enabled (LMT=1) and exponent overflow occurs, the data output is clipped. The resulting output is the maximum positive number possible (exponent = 011111, significand = 0.111 1111 1111 1111) if the significand is positive. If the significand is negative, the resulting output is the maximum negative number possible (exponent = 011111, significand = 1.000 0000 0000 0000).

When the limit function is enabled and exponent underflow occurs, the data output is forced to ZERO, regardless of the sign of the significand. This also occurs when a zero significand (denoted by the ZERO flag being set) with an exponent other than −32 exists. These cases will always be replaced with clean zeroes, regardless of the state of the LMT control.

When the limit function is enabled and significand overflow occurs, the limiter clips the emerging result to a full-scale maximum positive or negative value, as appropriate. The case of Denormalize (−A) with A = −1 and the A exponent greater than or equal to the B exponent results in the output of a clean zero, since the ZERO flag is also set.

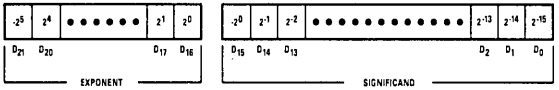
Output Section

The data and flag output registers are unconditionally loaded at the rising edge of CLK. The data output emerges through a three-state, 22-bit output port. The output format is identical to the input format. The flags are not three-stated, and the flag buffers are always enabled.

Signal Definitions

	Signal Name	Function	Value	J1 Package
Power				
	V_{CC}	Supply Voltage	+5.0V	Pin 49
	GND	Ground	0.0V	Pins 2, 16
	CLK	Clock	TTL	Pin 46
Data Input				
	$\overline{LDA}$	Latch A Control	TTL	Pin 44
	$\overline{LDB}$	Register B Load Control	TTL	Pin 45
	DI_{21-0}	Data Input	TTL	Pins 22–43
Control, Instructions				
	$\overline{LDI}$	Register I Load Control	TTL	Pin 17
	FT	Feedthrough Control	TTL	Pin 47
	ACC	Accumulate Control	TTL	Pin 21
	I_{2-0}	ALU Instructions	TTL	Pins 18–20
	RND	Round Control	TTL	Pin 15
	SCA	Scale Control	TTL	Pin 13
	LMT	Limit Control	TTL	Pin 14
Flags				
	ZERO	Zero Flag	TTL	Pin 4
	SOV	Significand Overflow Flag	TTL	Pin 6
	EOV	Exponent Overflow Flag	TTL	Pin 5
	EUN	Exponent Underflow Flag	TTL	Pin 3
Data Output				
	$\overline{OE}$	Three-State Output Enable	TTL	Pin 48
	DO_{21-0}	Data Output	TTL	Pins 1, 7–12, 50–64

Floating Point Data Format



Exponent

The exponent is represented by bits D_{16} through D_{21}. It is a two's complement integer with D_{21} the two's complement sign bit. The exponent ranges from −32 to 31.

$$\text{Exponent} = D_{21} \times (-2^5) + \sum_{n=16}^{20} D_n \times 2^{(n-16)}$$

Significand

The significand (sometimes referred to as the MANTISSA) is represented by bits D_{15} through D_0. It is a fractional two's complement number with 16-bit precision: D_{15} is the two's complement sign bit. The significand ranges from −1 to $(1-2^{-15})$.

$$\text{Significand} = D_{15} \times (-1) + \sum_{n=0}^{14} D_n \times 2^{(n-15)}$$

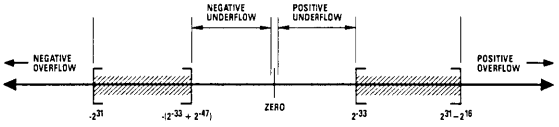
Zero

Zero is represented as follows:

Significand = 0.000 0000 0000 0000
Exponent = 100 000

Representable Floating Point (FLP) Number Range

Normalized Floating Point Range: A normalized floating point number is one for which the first two bits of the significand (D_{15} and D_{14}) are different, that is $D_{15} \oplus D_{14} = 1$.



TDC1022 Timing Diagrams

General Information

TDC1022 can be operated in any one of the following four modes:

1. Non-Accumulate without Pipelining (ACC=0, FT=1)
2. Non-Accumulate with Pipelining (ACC=0, FT=0)
3. Accumulate without Pipelining (ACC=1, FT=1)
4. Accumulate with Pipelining (ACC=1, FT=0)

In non-pipelined modes, the CLK period t_{CYN} is approximately twice as long as the CLK periods of the pipelined modes t_{CYP}.

The input register setup and hold times, the output delay time, the three-state enable and three-state disable times are the same in all four modes, thus they are only shown for the non-accumulate without pipelining mode (see below).

Figure 1. Non-Accumulate Mode Without Pipelining

The output data is available one clock cycle after the input data is entered.

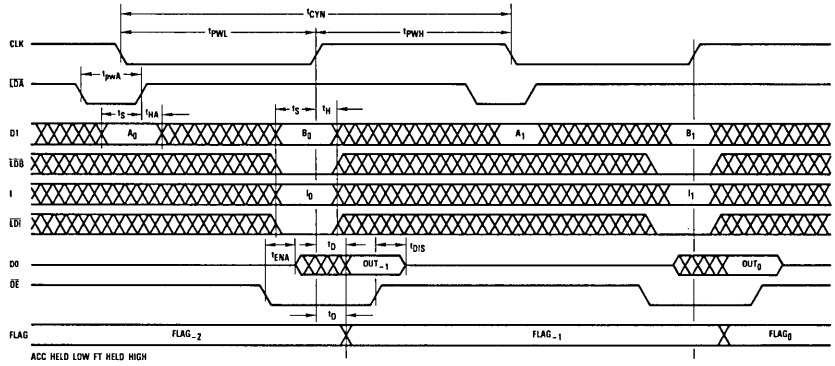
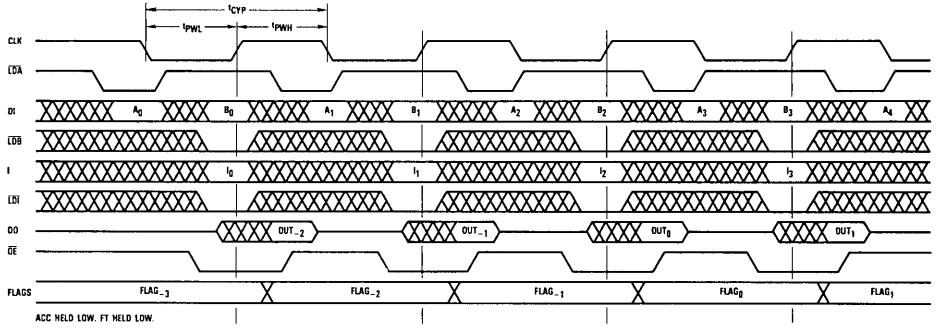


Figure 2. Non-Accumulate Mode With Pipelining [1]

The output data is available two clock cycles after the input data is entered.



Note: 1. Since RND, SCA, LMT are NOT pipelined, they must be entered one clock cycle **after** the data which they are to affect.

Figure 3. Accumulate Mode Without Pipelining

The first output data is available one clock cycle after the first input data is entered. The output is further described below:

1. The first output is the result of performing the first instruction on the first two operands.

   $OUT_0 = I_0\ (A_0, B_0)$

2. The second output is the result of performing the second instruction on the second two operands.

   $OUT_1 = I_1\ (A_1, B_1)$

3. Any subsequent output depends on the previous output and the current instruction and incoming operand.

   $OUT_n = I_n\ (OUT_{n-1}, B_n)$

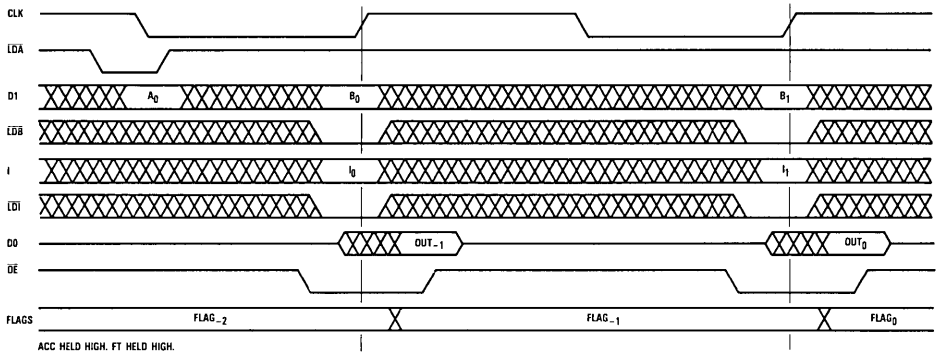


Figure 4. Accumulate Mode With Pipelining[1]

The first output data is available two clock cycles after the first input data is entered. The output is further described below:

1. The first output is the result of performing the first instruction on the first two operands.

   $OUT_0 = I_0\ (A_0, B_0)$

2. The second output is the result of performing the second instruction on the first output and the incoming operand.

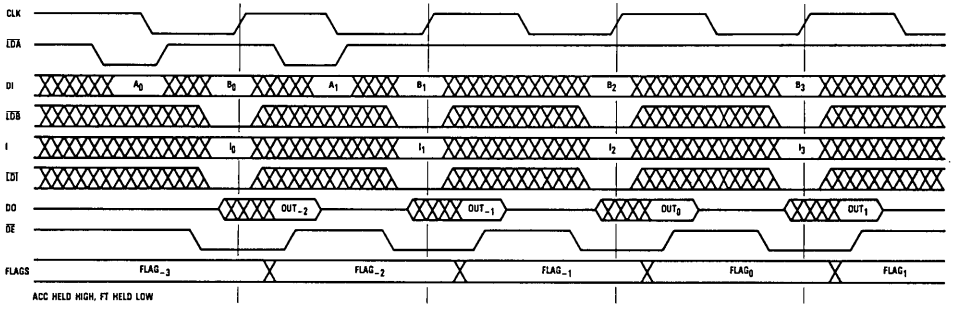
   $OUT_1 = I_1\ (OUT_0, B_1)$

3. The third output is the result of performing the third instruction on the first output and the incoming operand.

   $OUT_2 = I_2\ (OUT_0, B_2)$

4. Any subsequent output depends on the output from two cycles ago, the current instruction, and the incoming operand.

   $OUT_n = I_n\ (OUT_{n-2}, B_n)$



Note: 1. Since RND, SCA, LMT are NOT pipelined, they must be entered one clock cycle **after** the data which they are to affect.

Figure 5. Equivalent Input Circuits

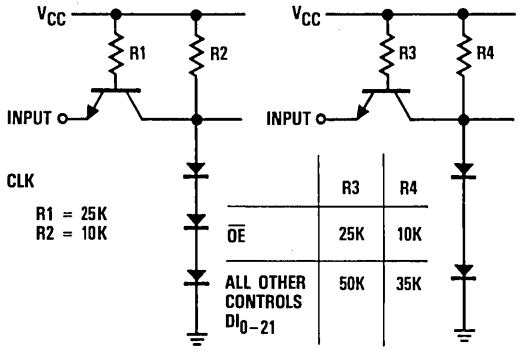


Figure 6. Equivalent Output Circuits

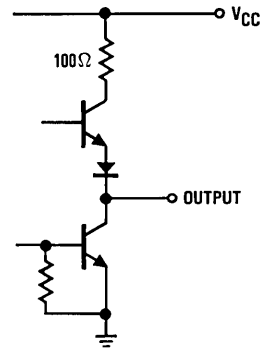


Figure 7. Test Load

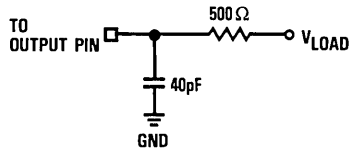
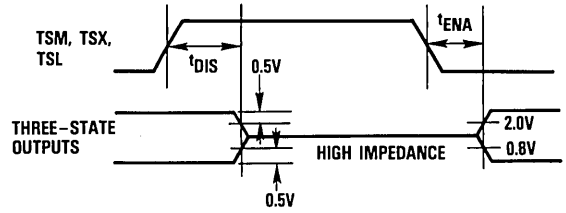


Figure 8. Transition Levels For Three–State Measurements



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to 7.0V
Input	
Applied voltage	−0.5 to 5.5V [2]
Forced current	−6.0 to +6.0mA
Output	
Applied voltage	−0.5 to 5.5V [2]
Forced current	−1.0 to 6.0mA [3,4]
Short circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating case	−55 to 125°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to 150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
t_{PWL}	Clock Pulse Width (LOW)	25			ns
t_{PWH}	Clock Pulse Width (HIGH)	25			ns
t_{PWA}	Clock Pulse Width (LDA)	35			ns
t_S	Input Setup Time	30			ns
t_H	Input Hold Time	3			ns
t_{HA}	Input Hold Time (Latch A)	4			ns
V_{IL}	Input Voltage, Logic LOW			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			V
I_{OL}	Output Current, Logic LOW			4.0	mA
I_{OH}	Output Current, Logic HIGH			−0.4	mA
T_C	Case Temperature	20		100	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
I_{CC}	Power Supply Current	V_{CC} = MAX, static		900	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_{IL} = 0.4V			
		(all inputs except CLK, $\overline{OE}$)		−0.4	mA
		CLK, $\overline{OE}$		−0.8	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_{IH} = 2.4V		75	μA
I_I	Input Current, MAX Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = 4.0mA		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = −0.4mA	2.4		V
I_{OZL}	HIGH-Z Output Leakage Current, Output LOW	V_{CC} = MAX, V_I = 0.4V		−40	μA
I_{OZH}	HIGH-Z Output Leakage Current, Output HIGH	V_{CC} = MAX, V_I = 2.4V		40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, One pin to ground, one second duration, output HIGH		−40	mA
C_I	Input Capacitance	T_A = 25°C, F = 1.0MHz		15	pF
C_O	Output Capacitance	T_A = 25°C, F = 1.0MHz		15	pF

Switching characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
t_{CYP}	Cycle Time, Pipelined	V_{CC} = MIN		100	ns
t_{CYN}	Cycle Time, Non-pipelined	V_{CC} = MIN		200	ns
t_D	Output Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V		40	ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 1.8V		35	ns
t_{DIS}	Three-State Output Disable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1}[2]		35	ns

Notes:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in Figure 8.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1022J1C	STD-T_C = 20°C to 100°C	Commercial	64 Lead DIP	1022J1C
TDC1022J1G	STD-T_C = 20°C to 100°C	Commercial With Burn-In	64 Lead DIP	1022J1G

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Preliminary Information describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact TRW for current information.

TDC1023

Digital Output Correlator
64-bit

The TRW TDC1023 is a monolithic, all-digital 64-bit correlator with a 7-bit three-state buffered digital output. This device consists of three 64-bit independently clocked shift registers, one 64-bit reference holding latch, and a 64-bit independently clocked digital summing network. The device is capable of a 17MHz parallel correlation rate.

The 7-bit threshold register allows the user to preload a binary number from 0 to 64. Whenever the correlation is equal to or greater than the number in the threshold register, the threshold flag goes HIGH.

The 64-bit mask shift register (M register) allows the user to mask or selectively choose "no compare" bit positions enabling total word length flexibility.

The reference word is serially shifted into the B register. By clocking the R latch, the data is parallel-loaded into the R reference latch. This allows the user to serially load a new reference word into the B register while correlation is taking place between the A register and R latch. The two words are continually compared bit-for-bit by exclusive-OR circuits. Each exclusive-OR provides one bit to the digital summer. The output is a 7-bit word representing the sum of positions which agree at any one time between the A register and R latch.

A control provides either true or inverted binary output formats.

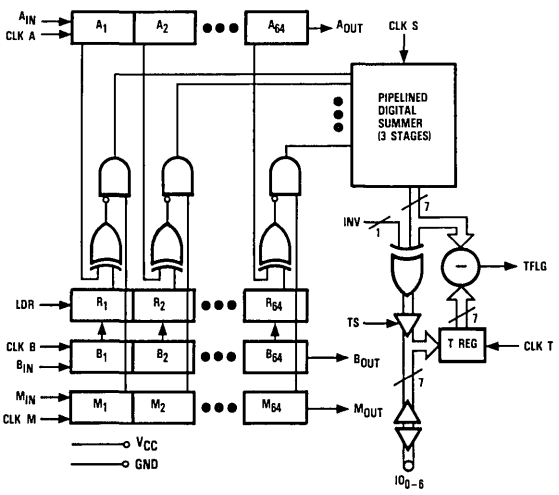
Features

- 17MHz Correlation Rate
- TTL Compatible
- All Digital
- Single +5V Power Supply
- Serial Data Input, Parallel Correlation Output
- Programmable Word Length
- Independently Clocked Registers
- Available In 24 Lead DIP
- Output Format Flexibility
- Three-State Outputs

Applications

- Check Sorting Equipment
- High-Density Recording
- Bar Code Identification
- Radar Signature Recognition
- Video Frame Synchronization
- Electro-Optical Navigation
- Pattern And Character Recognition
- Cross-Correlation Control Systems
- Error Correction Coding
- Asynchronous Communication

Functional Block Diagram



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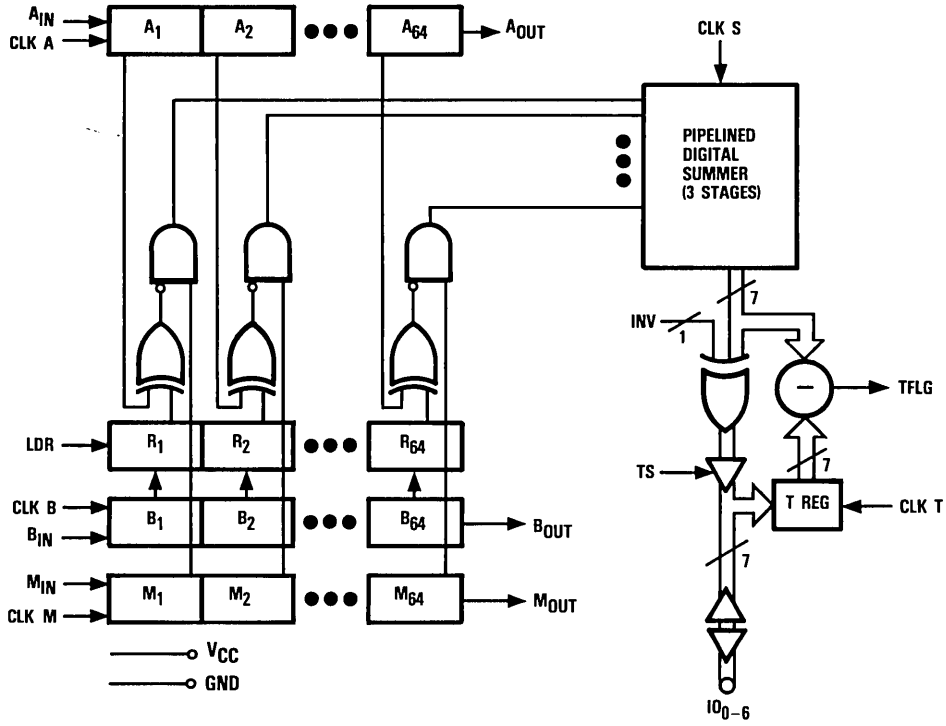
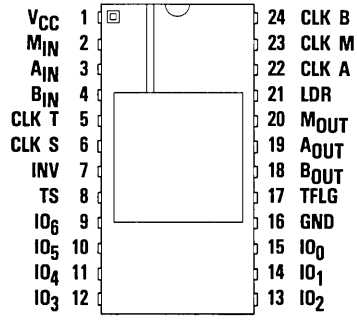
Functional Block Diagram



Pin Assignments



24 Lead DIP – J7 Package

Functional Description

General Information

The TDC1023 consists of an input section and an output section. The input section contains A, B, and M registers, an R latch, XOR/AND logic and a pipelined summer. The output section consists of threshold, inversion and three-state logic.

Power

The TDC1023 operates from a single +5 Volt supply.

Name	Function	Value	J7 Package
GND	Ground	0.0V	Pin 16
V_{CC}	Supply Voltage	+5.0V	Pin 1

Control

INV — Control that inverts the 7-bit digital output. When a HIGH level is applied to this pin, the outputs IO_{0-6} are logically inverted.

TS — Control that enables the three-state output buffers. A HIGH level applied to this pin forces outputs into the high-impedance state.

LDR — Control that allows parallel data to be loaded from the B register into the reference R latch for correlation. If LDR is held HIGH, the R latch is transparent.

Name	Function	Value	J7 Package
INV	Invert Output	TTL	Pin 7
TS	Three-State Enable	TTL	Pin 8
LDR	Load Reference	TTL	Pin 21

Clocks

CLK A, CLK M, CLK B — Input clocks. Clock input pins for the A, M, and B registers, respectively. Each register may be independently clocked.

CLK T — Threshold register clock. Clock input pin for T register.

CLK S — Digital summer clock. Clock input which allows independent clocking of pipelined summer network.

Name	Function	Value	J7 Package
CLK A	A Register Clock	TTL	Pin 22
CLK M	M Register Clock	TTL	Pin 23
CLK B	B Register Clock	TTL	Pin 24
CLK T	Threshold Register Clock	TTL	Pin 5
CLK S	Digital Summer Clock	TTL	Pin 6

Data Inputs

M_{IN} Allows the user to choose "no compare" bit positions. A "0" in any bit location will result in a no-compare state for that location.

A_{IN}, B_{IN} Shift register inputs to the A and B 64-bit serial registers.

Name	Function	Value	J7 Package
M_{IN}	Mask Register Input	TTL	Pin 2
A_{IN}	Shift Register Input	TTL	Pin 3
B_{IN}	Shift Register Input	TTL	Pin 4

Data Outputs

IO_{0-6} Bidirectional data pins. When outputs are enabled (TS LOW), data is a 7-bit binary representation of the correlation between the unmasked positions of the R latch and the A register. IO_6 is the MSB. These pins also serve as parallel inputs to load the threshold register. Data present one setup time before CLK T goes HIGH will be latched into the threshold register.

TFLG TFLG output goes HIGH whenever the correlation score is equal to or greater than the number loaded into the T register (0 to 64).

B_{OUT}, A_{OUT}, M_{OUT} Shift register outputs of the three 64-bit serial shift registers: B, A, and M, respectively.

Name	Function	Value	J7 Package
IO_6	MSB	TTL	Pin 9
IO_5		TTL	Pin 10
IO_4		TTL	Pin 11
IO_3		TTL	Pin 12
IO_2		TTL	Pin 13
IO_1		TTL	Pin 14
IO_0	LSB	TTL	Pin 15
TFLG	Threshold Flag	TTL	Pin 17
B_{OUT}	Shift Register B	TTL	Pin 18
A_{OUT}	Shift Register A	TTL	Pin 19
M_{OUT}	Shift Register M	TTL	Pin 20

TDC1023 Timing Diagrams

1. Continuous Correlation

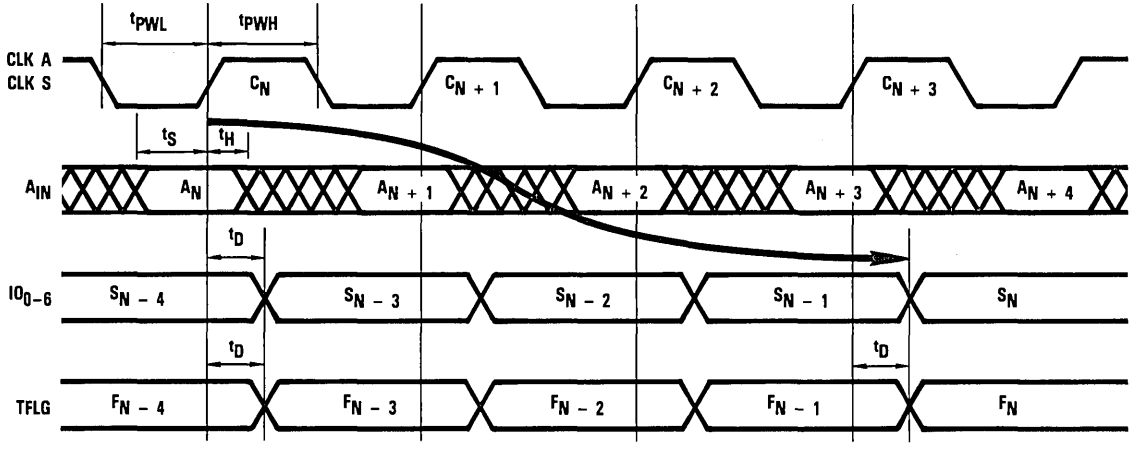
The TDC1023 contains three 1 X 64 serial shift registers (A, B, and M). The operation of these registers is identical and each has its own TTL-compatible input, output, and clock. As shown in the timing diagram (Figure 1), valid data is loaded into register A (B, M) on the rising edge of CLK A (CLK B, CLK M). Data is valid if present at the input for a setup time of a least t_S (ns) before and a hold time t_H (ns) after the rising clock edge.

The summing process is initiated when the comparison result between the A register and R latch is clocked into the summing network by a rising edge of CLK S. Typically, CLK A and CLK S are tied together so that a new correlation score is computed for each new alignment of the A register and R latch. When LDR goes HIGH, the contents of register B are copied into the R latch. With LDR LOW, a new template may be entered serially into register B, while parallel correlation takes place between register A and the R latch. In the case of continuous correlation, LDR is held HIGH so that the R latch contents continuously track those of the B register.

The summing network consists of three pipelined stages. Therefore, the total correlation score for a given set of A and B register contents appears at the summer output three CLK S cycles later. Data on the output pins IO_{0-6} is available after an additional propagation delay, denoted t_D on the timing diagram.

The correlation result is compared with the contents of the threshold register. TFLG goes HIGH if the correlation equals or exceeds the threshold value. TFLG is valid after a delay of t_D (ns) from the third CLK S rising edge.

Figure 1. Continuous Correlation



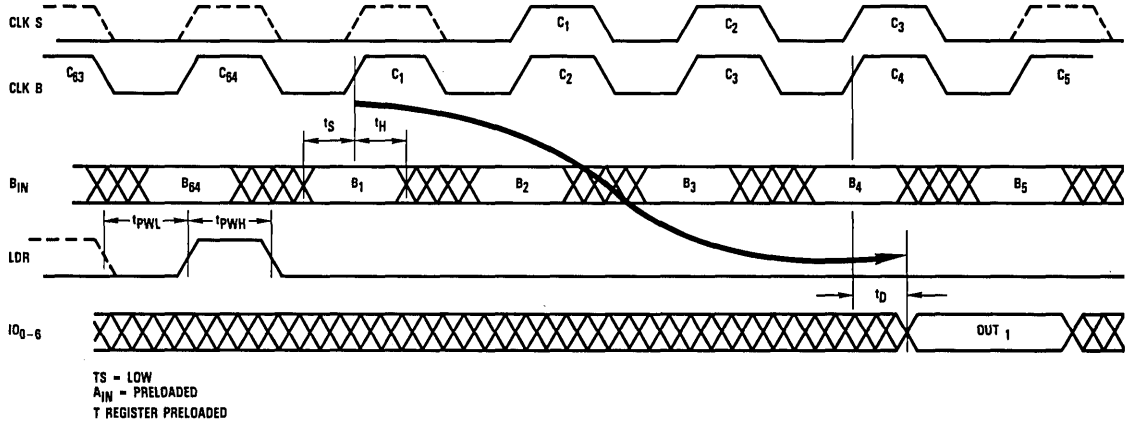
LDR = HIGH
TS = LOW
B_{IN} = REFERENCE
T REGISTER PRELOADED

2. Cross–Correlation

When LDR goes HIGH, the B register contents are copied into the reference latch (R latch). This useful feature allows correlation to take place between data in the R latch and the A register while a new reference is being serially clocked into the B register. If the new reference is n bits long, it requires n rising edges of CLK B to load this data into the B register. For the timing diagram (see Figure 2), n = 64. LDR is set HIGH during the final (n^{th}) CLK B cycle, so that the new reference word is copied into the R latch. The minimum low and high level pulse widths for LDR are shown as t_{PWL} (ns) and t_{PWH} (ns), respectively.

After the new reference is loaded, the data to be correlated is clocked through the A register. Typically, CLK A and CLK S can be tied together. This allows a new correlation score to be computed for each shift of the A register data relative to the fixed reference word in the R latch. The digital summer is internally partitioned into three pipelined stages. Therefore, a correlation score for a particular alignment of the A register data and the R latch reference appears at the summer output three CLK S cycles later. After an additional output delay of t_D (ns), the correlation data is valid at the output pins (IO_{0-6}). If this correlation result is equal to or exceeds the value in the threshold register, then TFLG goes HIGH. TFLG is valid t_D (ns) after the third rising edge of CLK S.

Figure 2. Cross–Correlation



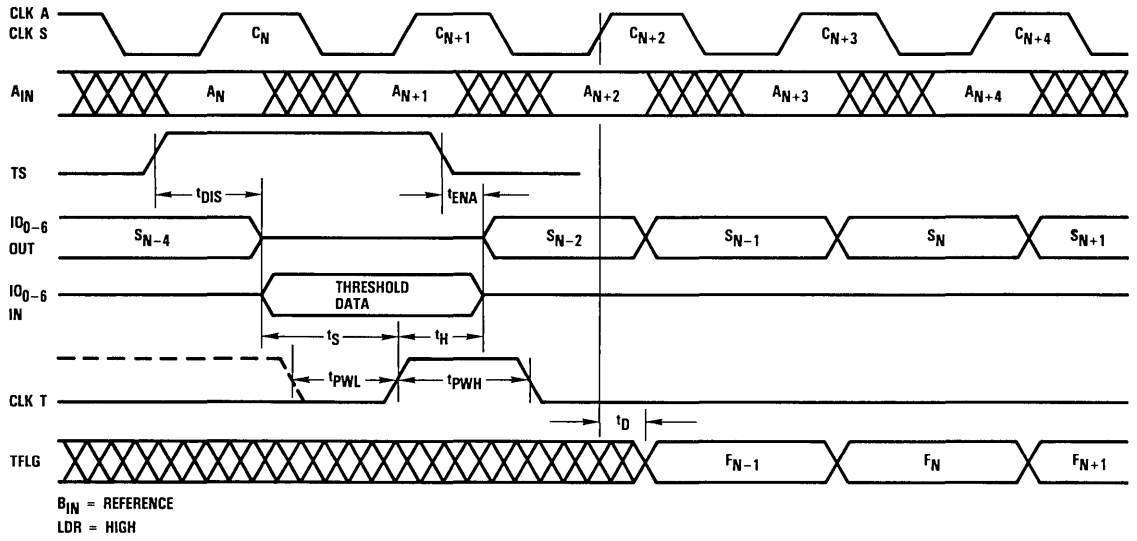
3. Threshold Register Load

The timing sequence for loading the threshold (T) register is shown in Figure 3. The T register holds the 7-bit threshold value to be compared with each correlation result. The rising edge of CLK T loads the data present on the IO_{0-6} pins into the T register.

The output buffers must be in a high-impedance state (disabled) when the T register is programmed from an external source. After a delay of t_{DIS} (ns) from the time TS goes HIGH, the output buffers are disabled. The data pins IO_{0-6} may then be driven externally with the new threshold data. The data must be present for a setup time of t_S (ns) before and t_H (ns) after the rising edge of CLK T to be correctly registered. The minimum low and high level pulse widths for CLK T are shown below as t_{PWL} (ns) and t_{PWH} (ns), respectively.

After TS is set LOW, there is an enable delay of t_{ENA} (ns) before the internal correlation data is available at pins IO_{0-6}.

Figure 3. Threshold Register Load



4. Mask Register

In addition to the A and B shift registers, the TDC1023 has another independently clocked register – the M, or mask register. The M register functions identically to the A and B registers, except that its parallel outputs are ANDed with the exclusive-ORed outputs from the A register and R latch.

Many uses of the TDC1023 digital correlator require disabling the correlation between certain bit positions (A_i and R_i) of input words A and R. While correlation data is being clocked into the A and/or B register, a mask word may be entered into the M register. Where no comparison is to be made, zeroes are entered in those M register positions. The exclusive-OR result between each bit position is ANDed with a bit from the M register. Thus, if a particular mask bit (M_i) is zero, the output correlation between A and B for that bit position will be disabled. Consequently, a zero correlation is presented to the digital summer for each masked bit position.

The mask register is useful for changing correlation word length and location within the registers. Where a word is undefined or no correlation is to take place, the M register should contain zeroes.

The M register is useful for building logic functions. Note that for each bit A_i and R_i, the correlation logic is:

$A_i \oplus R_i \equiv A_i\overline{R_i} + \overline{A_i}R_i$ (A_i exclusive-OR R_i)

This result is complemented at the input of the AND gates and ANDed with the mask bit (M_i) resulting in:

$$\overline{[A_i\overline{R_i} + \overline{A_i}R_i]} \bullet M_i$$

The last step, performed in the digital summer, is to sum the above result over all bit positions simultaneously for a correlation at time K:

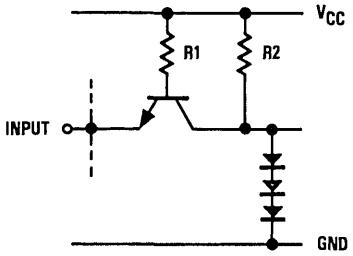
$$C(K) = \sum_{i=1}^{n} \overline{[A_i\,\overline{R_i} + \overline{A_i}\,R_i\,]} \bullet M_i$$

where,

i = 1, 2, 3...

n = correlation word length

Figure 4. Equivalent Input Schematic



PIN	VALUES R1	R2	NUMBER OF INTERNAL CIRCUITS LOADING PIN
A_{IN}, B_{IN}, M_{IN}	50K	35K	1
CLK A, B, M	35K	20K	2
LDR	35K	20K	2
CLK S	35K	20K	3
CLK T, INV	35K	20K	1

Figure 5. Equivalent Circuit for IO_{0-6}, A_{OUT}, B_{OUT}, M_{OUT} and TFLG.

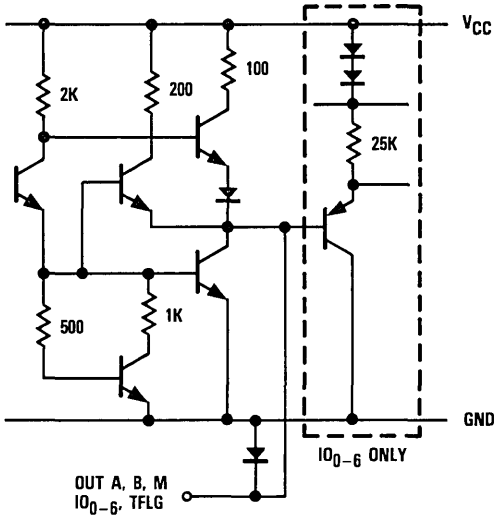


Figure 6. Equivalent Circuit for Three-State (TS) Input.

The circuitry to the right of dashed line is repeated 7 times.

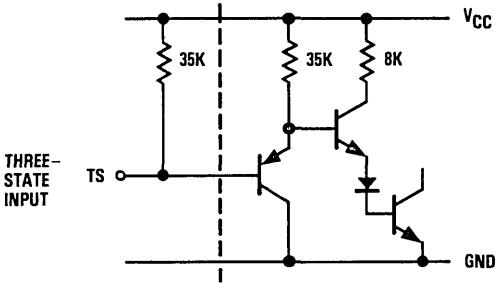


Figure 7. Test Load

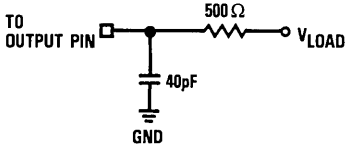
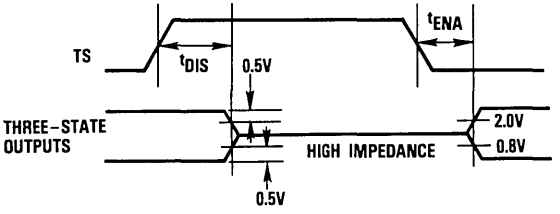


Figure 8. Transition Levels For Three-State Measurements



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−6.0 to +6.0mA
Output	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−1.0 to +6.0mA [3,4]
Short circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, ambient	−60 to 135°C
junction	+175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to 150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter			Temperature Range						Units
			Standard			Extended			
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PWL}	Clock Pulse Width, LOW	CLK A, CLK B, CLK M, CLK S, LDR	20			20			ns
		CLK T	25			30			ns
t_{PWH}	Clock Pulse Width, HIGH	Clocks	25			30			ns
		LDR	30			35			ns
t_S	Data Input Setup Time	A_{IN}, B_{IN}, M_{IN}	20			22			ns
		$\overline{IO}_{0-6}$	45			50			ns
t_H	Data Input Hold Time	A_{IN}, B_{IN}, M_{IN}	3			3			ns
		$\overline{IO}_{0-6}$	0			3			ns
V_{IL}	Input Voltage, Logic LOW				0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH		2.0			2.0			V
I_{OL}	Output Current, Logic LOW				4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH				−400			−400	μA
T_A	Ambient Temperature, Still Air		0		70				°C
T_C	Case Temperature					−55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
I_{CC}	Supply Current	V_{CC} = MAX, static[1]					
		T_A = 0°C to 70°C		335			mA
		T_A = 70°C		295			mA
		T_C = −55°C to 125°C				395	mA
		T_C = 125°C				275	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V					
		IO_{0-6}, TS, Data, INV		−350		−400	μA
		Clocks, LDR		−1.0		−1.3	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V					
		IO_{0-6}, TS, INV, Data		50		50	μA
		Clocks, LDR		100		100	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		500		500	μA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	High-Z Output, Leakage Current[2]	V_{CC} = MAX, V_I = 0.4V		−350		−400	μA
I_{OZH}	High-Z Output, Leakage Current[2]	V_{CC} = MAX, V_I = 2.4V		50		50	μA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz					
		Clocks		10		10	pF
		IO_{0-6}, Controls		5		5	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Notes:

1. Worst case, all digital inputs and outputs LOW.
2. Due to the IO_{0-6} and T registernnection, these values are the I_{IH} and I_{IL} of the T register.

Switching characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
F_{SH}	Shift-In Clock Rate	V_{CC} = MIN	20		17		MHz
F_C	Correlation Rate	V_{CC} = MIN[2]	17		15		MHz
t_D	Digital Output Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V					
		IO_{0-6}		45		50	ns
		A_{OUT}, B_{OUT}, M_{OUT}		35		40	ns
		TFLG		40		45	ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 1.8V		40		45	ns
t_{DIS}	Three-State Output Disable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1}[3]		35		35	ns

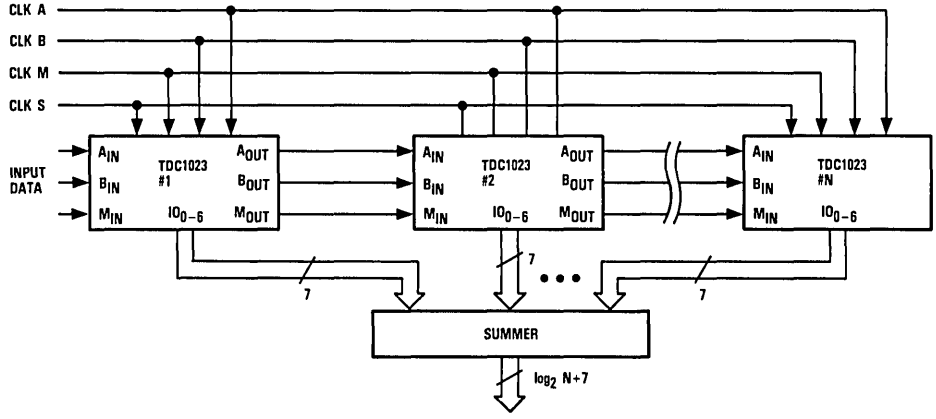
Notes:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in Figure 8.
2. Synchronous clocking: CLK A = CLK B = CLK M = CLK S.
3. t_{DIS1} *denotes the transition from logical 1 to three-state.*
   t_{DIS0} denotes the transition from logical 0 to three-state.

Application Notes

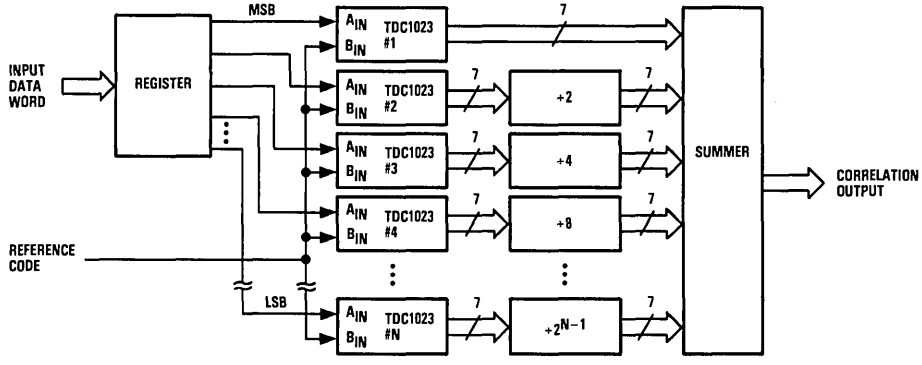
1. The TDC1023 can be cascaded to implement correlations of more than 64 bits. Typically, all clocks are tied together and the A, B, and M outputs of preceding stages are connected to the respective inputs of subsequent stages. An external summer is required to generate the composite correlation score. Use of the T register and TFLG require additional hardware in this configuration.

Figure 9. Cascading For Extended–Length Correlation



2. When comparing a multi-bit word to a single-bit reference, the outputs from the individual correlators must be appropriately weighted. This weighting reflects the relative importance of the different bit positions. Normally, simple shifts (+ 2, 4, 8,...) provide the required weighting.

Figure 10. Multi–Bit x 1 Bit Correlation



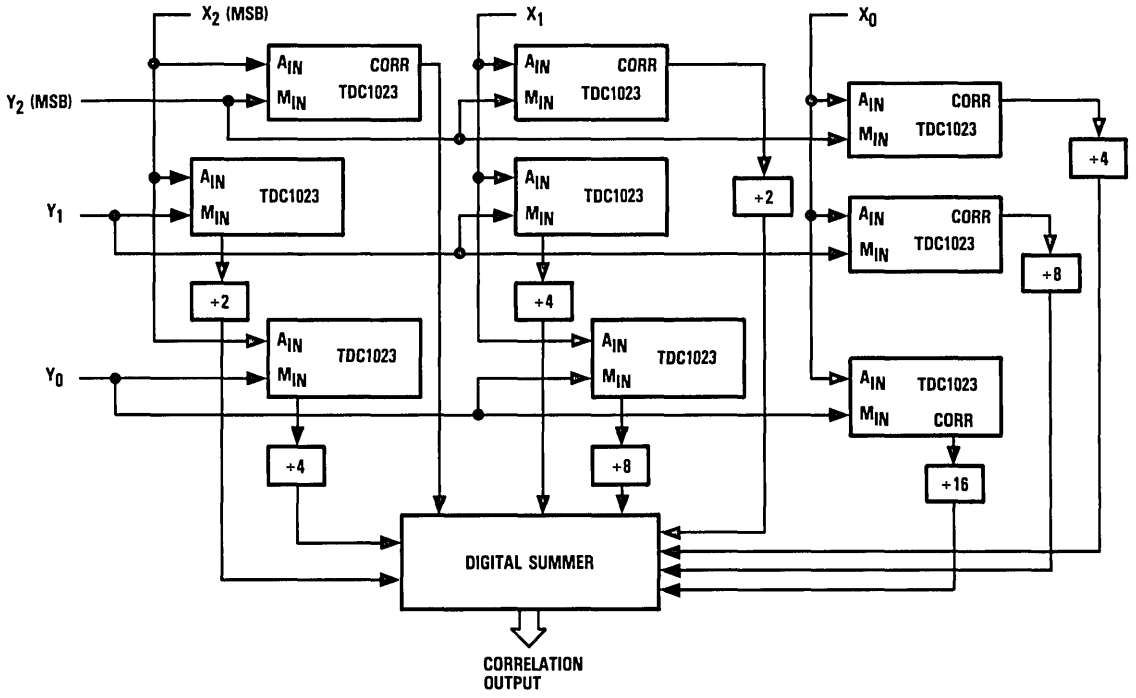
3. The correlation of two multi-bit words requires evaluating the term:

$$R(M) = \sum_{n=1}^{N} h(n) \times (M+n)$$

An example of two 3-bit words is shown below.

For additional TDC1023 Digital Output Correlator applications, see Application Note TP-17, "Correlation - A Powerful Technique for Digital Signal Processing." This application note is available upon request from TRW LSI Products.

Figure 11. Multi-Bit Correlation



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1023J7C	STD-T_A = 0°C to 70°C	Commercial	24 Lead DIP	1023J7C
TDC1023J7G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	24 Lead DIP	1023J7G
TDC1023J7F	EXT-T_C = -55°C to 125°C	Commercial	24 Lead DIP	1023J7F
TDC1023J7A	EXT-T_C = -55°C to 125°C	High Reliability[1]	24 Lead DIP	1023J7A

Note:
1. Per TRW document 70Z01757.

TDC1028
Preliminary Information

Digital Filter/Correlator
Building Block, 10MHz

The TDC1028 is a video-speed, TTL compatible bit-slice building block for Finite Impulse Response (FIR) digital filters and multi-bit digital correlators. It is used independently in the coefficient and signal data word dimensions as a bit-slice processor. Word lengths can be multiples of four bits. Two's complement or unsigned magnitude operation is independently selectable for both coefficients and signal data words.

The TDC1028 provides eight delay stages, eight multipliers, and eight adders in a single integrated circuit. Eight coefficient storage registers are also provided for ease in programming filter characteristics and to make correlation possible. One coefficient may be changed every clock cycle. The delay registers and the adder pipeline registers have been merged for efficiency.

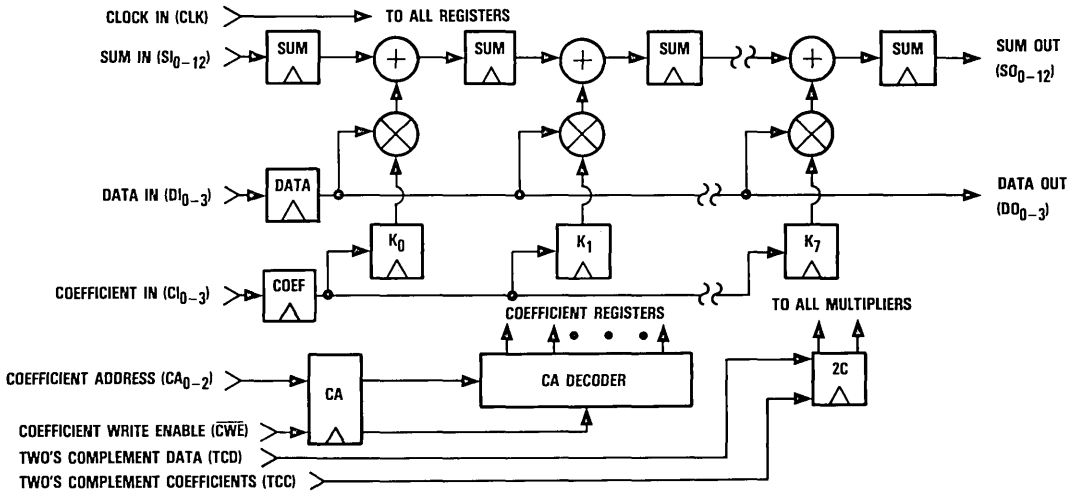
Features

- 10MHz Throughput Rate
- Eight Coefficients
- Cascadable (To > 36 Taps) Without External Components
- 4-Bit Coefficient And Signal Data Words
- Independently Expandable Coefficient And Signal Word Length
- Independently Selectable Format For Coefficients And Signal Data Words (Two's Complement or Unsigned Magnitude)
- Available In 48 Lead DIP
- Radiation Hard Bipolar Process
- Single +5V Power Supply
- TTL Compatible

Applications

- Digital Video Filters
- Matched Filters
- Pulse Compression
- Multi-Bit Correlation
- Waveform Synthesis
- Adaptive Filters

Functional Block Diagram



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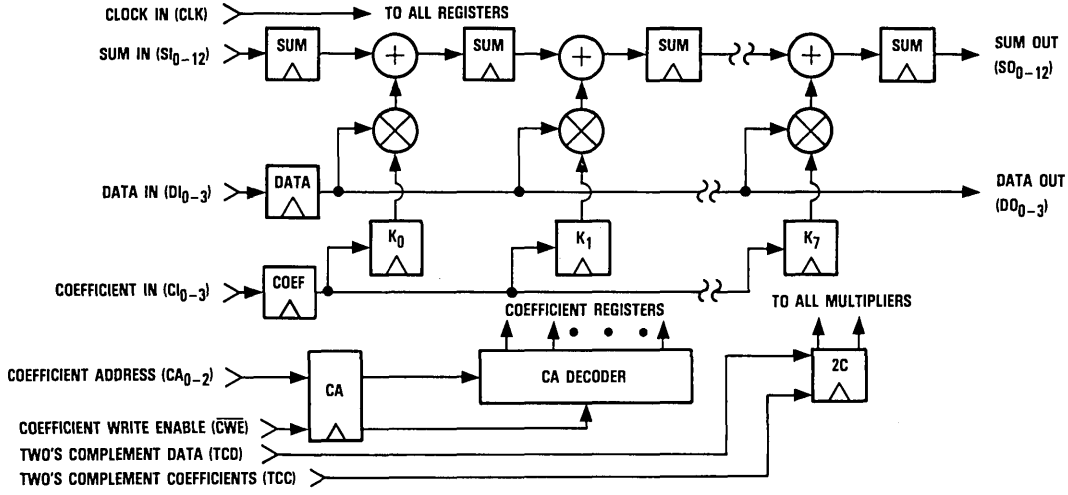
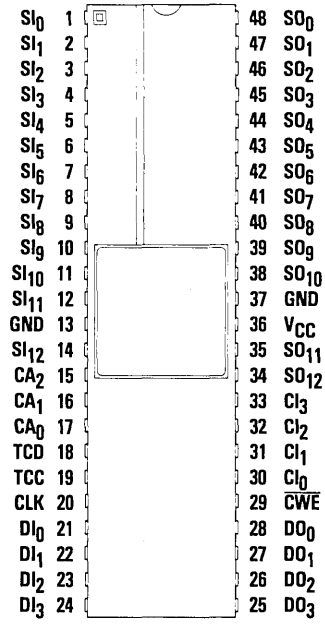
Functional Block Diagram



Pin Assignments



48 Lead DIP – J4 Package

Functional Description

General Information

The TDC1028 has four internal functions: delay, multiplication, addition, and coefficient storage. These functions are connected to form a building block for finite impulse response filters or correlators. Cascading inputs are provided to allow the construction of filters or correlators of arbitrary length. The basic word size for coefficients and data is four bits. The order of the operations has been changed from the canonical form to permit the merging of delay and pipelining registers (see Figure 1).

Power

The TDC1028 operates from a single +5 Volt supply. All power and ground lines must be connected.

Name	Function	Value	J4 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pin 36
GND	Ground	0.0V	Pins 13,37

Inputs

The TDC1028 has three types of inputs: signal data, coefficients, and sum (cascading) inputs.

Name	Function	Value	J4 Package
DI_3	Signal Data Input MSB	TTL	Pin 24
DI_2		TTL	Pin 23
DI_1		TTL	Pin 22
DI_0	Signal Data Input LSB	TTL	Pin 21
CI_3	Coefficient Input MSB	TTL	Pin 33
CI_2		TTL	Pin 32
CI_1		TTL	Pin 31
CI_0	Coefficient Input LSB	TTL	Pin 30
SI_{12}	Cascading Sum Input MSB	TTL	Pin 14
SI_{11}		TTL	Pin 12
SI_{10}		TTL	Pin 11
SI_9		TTL	Pin 10
SI_8		TTL	Pin 9
SI_7		TTL	Pin 8
SI_6		TTL	Pin 7
SI_5		TTL	Pin 6
SI_4		TTL	Pin 5
SI_3		TTL	Pin 4
SI_2		TTL	Pin 3
SI_1		TTL	Pin 2
SI_0	Cascading Sum Input LSB	TTL	Pin 1

Data Outputs

The TDC1028 has two outputs: a sum output and a data output. The data output is used to connect one TDC1028 to the next (cascading) for greater filter or correlation length. The sum output is used both for cascading and signal output.

Name	Function	Value	J4 Package
SO_{12}	Sum Output MSB	TTL	Pin 34
SO_{11}		TTL	Pin 35
SO_{10}		TTL	Pin 38
SO_9		TTL	Pin 39
SO_8		TTL	Pin 40
SO_7		TTL	Pin 41
SO_6		TTL	Pin 42
SO_5		TTL	Pin 43
SO_4		TTL	Pin 44
SO_3		TTL	Pin 45
SO_2		TTL	Pin 46
SO_1		TTL	Pin 47
SO_0	Sum Output LSB	TTL	Pin 48
DO_3	Data Output MSB	TTL	Pin 25
DO_2		TTL	Pin 26
DO_1		TTL	Pin 27
DO_0	Data Output LSB	TTL	Pin 28

Clocks

The TDC1028 operates synchronously from a single master clock, which can be clocked at up to 10MHz. All internal circuitry is static; there is no minimum clock frequency required. The rising edge of CLK latches the Coefficient Input (CI_{3-0}), the Coefficient Address (CA_{2-0}), and the Coefficient Write Enable control ($\overline{CWE}$). If $\overline{CWE}$ is LOW, a new coefficient will be loaded into the selected coefficient register at the next rising edge of CLK, as shown in Figure 4.

Name	Function	Value	J4 Package
CLK	Clock	TTL	Pin 20

Controls

The TDC1028 has six control inputs. TCC and TCD control the interpretation of the data and coefficients as two's complement or unsigned magnitude numbers. These inputs provide two's complement operation for the respective input when a logic HIGH is applied, and unsigned magnitude operation when a logic LOW is applied. One active LOW input ($\overline{CWE}$) controls the writing of a coefficient, and three inputs (CA_{2-0}) control the selection of which coefficient is to be written.

Name	Function	Value	J4 Package
TCC	Two's Complement Coefficients	TTL	Pin 19
TCD	Two's Complement Data	TTL	Pin 18
$\overline{CWE}$	Coefficient Write Enable	TTL	Pin 29
CA_2	Coefficient Address MSB	TTL	Pin 15
CA_1		TTL	Pin 16
CA_0	Coefficient Address LSB	TTL	Pin 17

Figure 1.

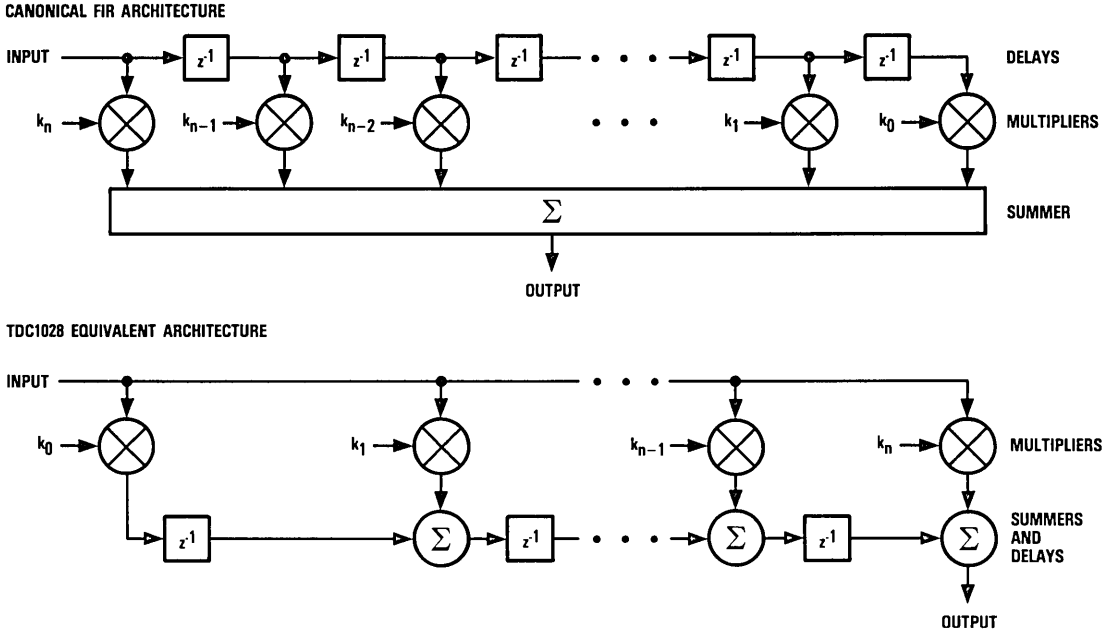


Figure 2.

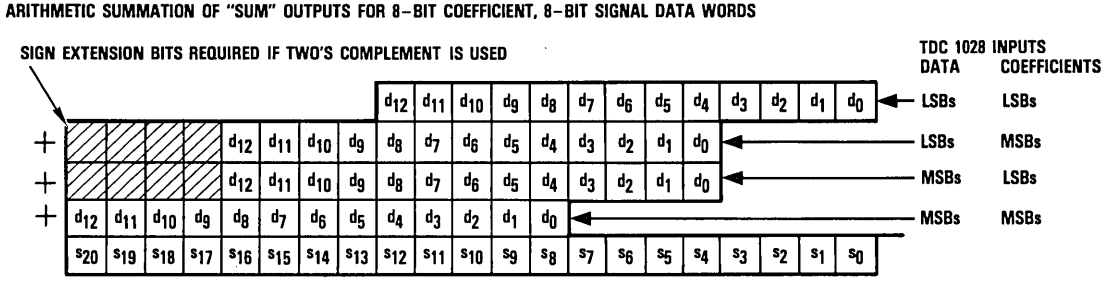


Figure 3.

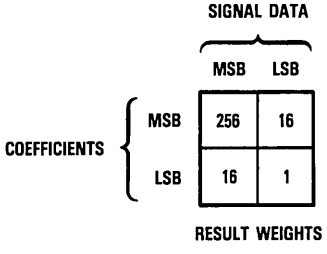


Figure 4.

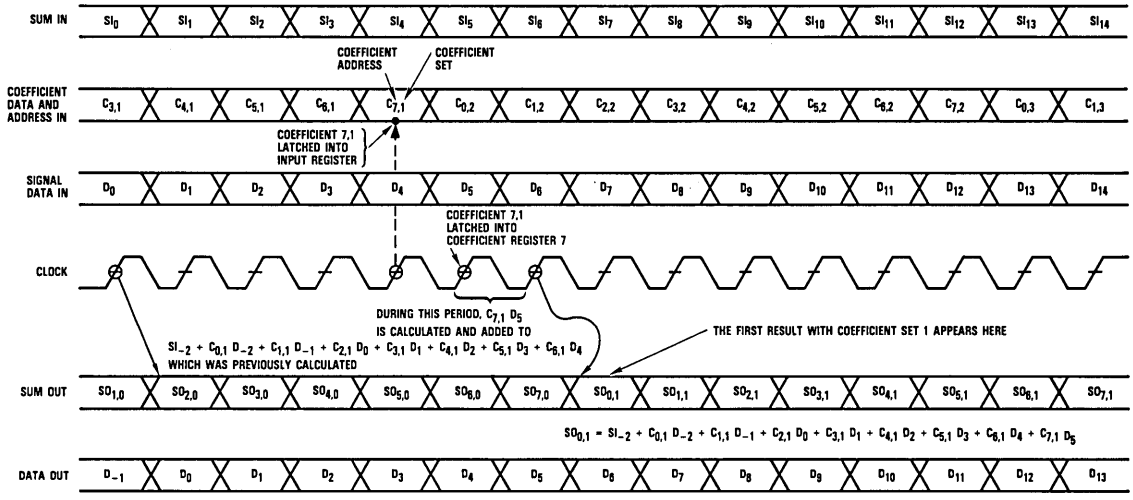


Figure 5.

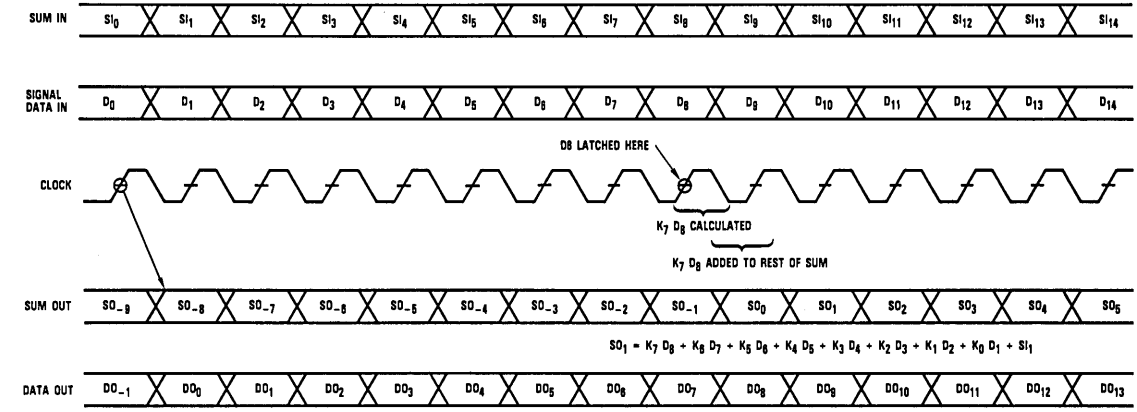


Figure 6. Equivalent Input Circuit

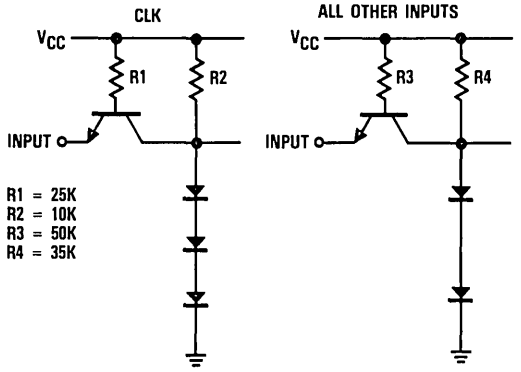


Figure 7. Equivalent Output Circuit

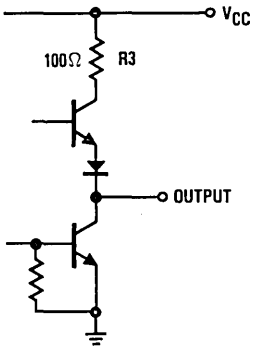
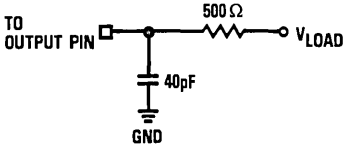


Figure 8. Test Load



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−6.0 to +6.0mA
Output	
Applied voltage (measured to D_{GND})	−0.5 to +5.5V [2]
Applied current, externally forced	−1.0 to +6.0mA [3,4]
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	−55 to +125°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to 150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	v
t_{PWL}	Clock Pulse Width, LOW	48			65			ns
t_{PWH}	Clock Pulse Width, HIGH	48			65			ns
t_{CY}	Clock Cycle Time	100			135			ns
t_S	Input Setup Time							
	Data In, Sum In	15			15			ns
	Coefficient In, Coefficient Address In	25			25			ns
	Coefficient Write Enable	30			30			ns
t_H	Input Hold Time (All inputs)	5			5			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		+125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = MAX, Static[1]					
		T_A = 0°C to 70°C		700			mA
		T_A = 70°C		550			mA
		T_C = −55°C to 125°C				800	mA
		T_C = 125°C				500	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V					
		Data Inputs		−0.4		−0.4	mA
		Clock Input		−1.0		−1.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V					
		Data Inputs		75		75	μA
		Clock Input		75		75	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OS}	Short-Circuit Output Current	V_{CC} = MAX, Output HIGH, one pin to ground, one second duration		−50		−50	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:
1. Worst case, all inputs and outputs LOW.

Switching characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{CY}	Cycle Time	V_{CC} = MIN		100		135	ns
t_D	Output Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 1.8V		30		35	ns

Note:
1. All transitions are measured at a 1.5V level.

Application Notes

More than one TDC1028 may be connected together to form filters of greater length, greater signal data resolution, and/or greater coefficient resolution.

The simplest form of expansion is length. Each TDC1028 has a data and a sum input, and a data and a sum output. To make a filter of greater length, connect the data and sum outputs to the data and sum inputs of the next device, as shown in Figures 2 and 3. This procedure is used for each section of a filter built with higher resolution for signal data and coefficients. Note that the sum inputs of the first device in a series (the one to which signal data is directly applied) must be supplied with a "zero" input (that is, all sum input pins must be grounded). This form of expansion is also used in combination with increased resolution, and is directly applicable to those cases.

Two options are available for increased resolution. The first method uses external adders and pipeline registers, the second uses the internal adders and pipeline registers of the TDC1028. Block diagrams of these methods are shown in Figures 9 and 10. The second method significantly increases latency; the output experiences a significant delay with respect to that of an ideal but causal Finite Impulse Response filter.

This section discusses the increasing of signal data and coefficient resolution when both signal data and coefficients are given in two's complement notation. For additional information, refer to TRW LSI Products Application Note TP-22.

The basic approach is to divide the word that requires greater resolution into two or more parts of four bits each. A separate section will be needed for every four bits or fraction thereof. Usually, both signal data words and coefficients will be divided. Next, a filter section is assigned to each possible combination of non-overlapping 4-bit groups of signal data with 4-bit groups of coefficients. (A filter section is assigned for each element in the cross-product of the signal data and coefficient data word spaces.) This process is shown in Figure 3, which illustrates division into 4-bit segments, used with both options for increasing resolution.

The choice is made between the adder option and the no-adder option. If the adder option is chosen, a pipelined adder must be designed using MSI components. A complete 16-tap filter using 8-bit signal data words and 8-bit coefficients is shown in Figure 9. Care must be taken to assure that the outputs of each of the sections are properly weighted. Note that the Two's Complement Data (TCD) pin should be active only in the sections which have the MSD of the data word as the input. Likewise, the Two's Complement Coefficient (TCC) pin should be active only on the sections which have the MSD of the coefficient word as the input.

However, another approach is possible. The TDC1028 has internal adders which are not used in the above configuration. Those are the adders in the first device in each section. By introducing suitable delays, these adders can be used to increase resolution without using external adders. A sample circuit, a complete 16-tap filter using 8-bit signal data words and 8-bit coefficients, is shown in Figure 10. Notice that this introduces an eighteen sample delay in the signal path. The necessary 8-bit wide by 9 or 18 stage long shift registers are provided by TRW's TDC1011.

Figure 9.

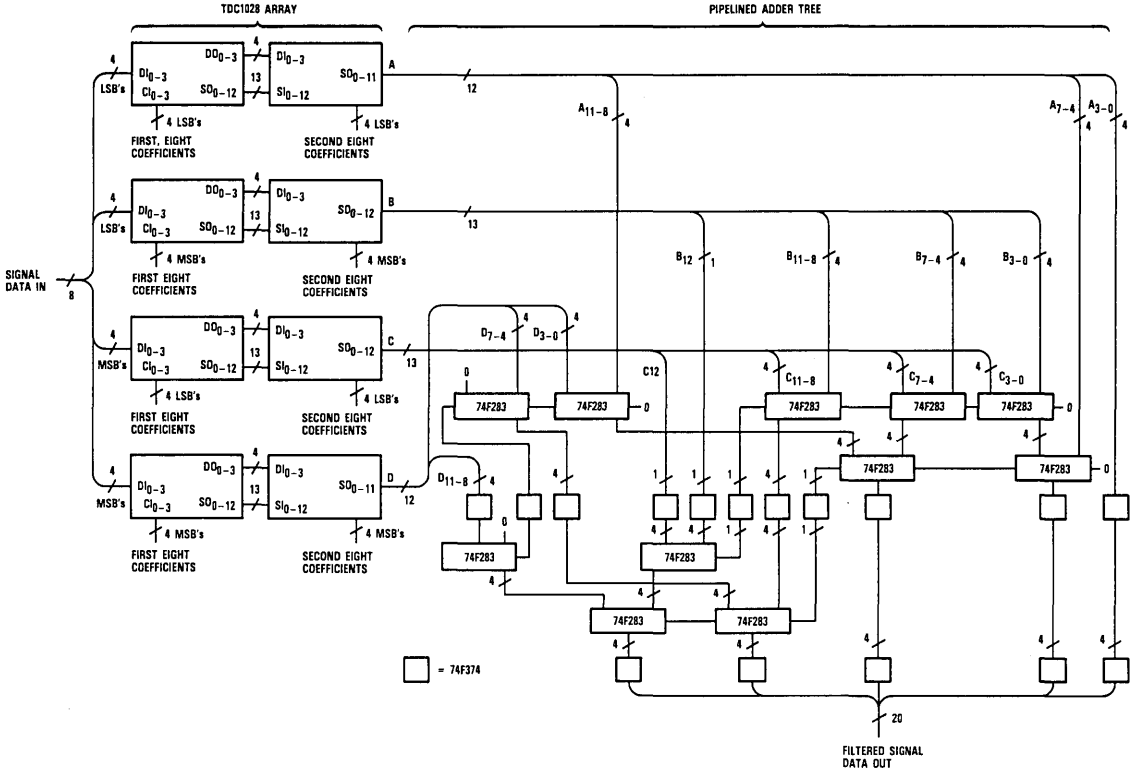
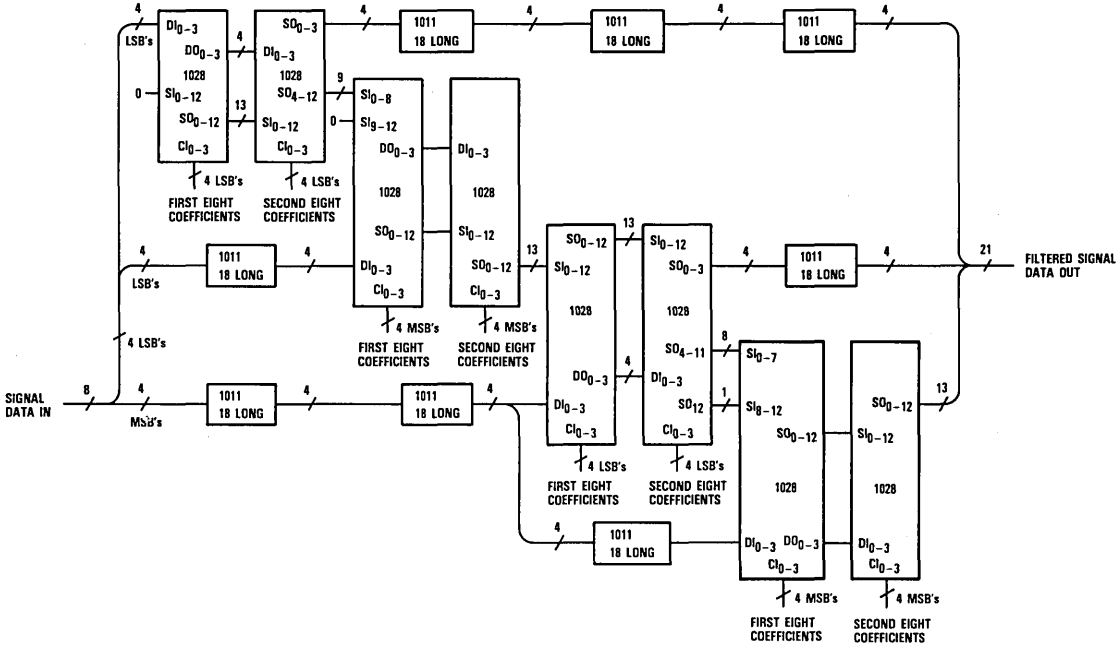

TDC1028 ARRAY
PIPELINED ADDER TREE
SIGNAL DATA IN
LSB's
MSB's
FIRST, EIGHT COEFFICIENTS
SECOND EIGHT COEFFICIENTS
FIRST EIGHT COEFFICIENTS
SECOND EIGHT COEFFICIENTS
74F283
= 74F374
FILTERED SIGNAL DATA OUT

Figure 10.



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1028J4C	STD-T_A = 0°C to 70°C	Commercial	48 Lead DIP	1028J4C
TDC1028J4G	STD-T_A = 0°C to 70°C	Commercial with Burn-In	48 Lead DIP	1028J4G
TDC1028J4F[1]	EXT-T_C = -55°C to 125°C	Commercial	48 Lead DIP	1028J4F
TDC1028J4A[1]	EXT-T_C = -55°C to 125°C	High Reliability[2]	48 Lead DIP	1028J4A

Notes:

1. Contact factory for availability.
2. Per TRW document 70Z1757.

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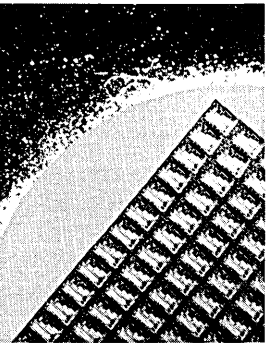
Preliminary Information describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact TRW for current information.

V L S I

D A T A

B O O K



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Application Notes And Reprints (Listings)

Shift Registers

The TDC1005 and TDC1006 are very high-speed, synchronous shift registers. Both devices are TTL compatible and support 20MHz clock rates. The TDC1006 stores a serial string of 256 bits, while the TDC1005 stores two parallel 64-bit strings.

Designed as a companion for the TDC1028 FIR filter chip, the TDC1011 byte wide programmable shift register can be used for delays from 3 to 18 stages. Both the registers and controls can be clocked at 18MHz. A 4-bit synchronous instruction controls the length to provide variable-delay capabilities at video speeds. A special split-word mode (two 4-bit words) is also provided for use with the TDC1028. The device is expandable in both the bit and word direction, and is fully TTL compatible.

FIFO

To help interface systems with differing instantaneous clock rates, TRW has introduced the TDC1030, a first-in first-out memory. The device accommodates up to 64 nine-bit words and is fully TTL compatible. Data may be written into and read out from the device asynchronously, using the TDC1030's input and output handshaking ports. Two or more TDC1030s can be cascaded serially to facilitate storage of longer data sequences. The maximum shift-in and shift-out rate is 15MHz for individual devices, and 13MHz for cascaded parts. The device may be used without the control flags up to 18MHz.

Product	Description	Size	Shift Rate[1] (MHz)	Power Dissipation[1] (Watts)	Package	Notes
TDC1005	Shift Register	64x2	25	0.6	J9	Expandable/Cascadable
TDC1006	Shift Register	256x1	25	0.7	J9	Expandable/Cascadable
TDC1011	Programmable Shift Register	18x8	18	0.8	J7, B7	Expandable/Cascadable
TDC1030	FIFO	64x9	15	1.8	J6, B6, C3	Expandable/Cascadable

Note: 1. Guaranteed, Worst Case, T_A = 0°C to 70°C.

J

TDC1005

Serial Shift Register
Dual 64-bit

The TRW TDC1005 is a dual 64-bit positive-edge-triggered serial shift register which operates at 25MHz. This device is cascadable in the number of words and the word size.

Complementary TTL outputs Q and $\overline{Q}$ are provided. The two data inputs in each shift register, D0 and D1, are controlled by a data select input, DS. This provides on-chip recirculate gating when the true output is hard-wired to one of the inputs.

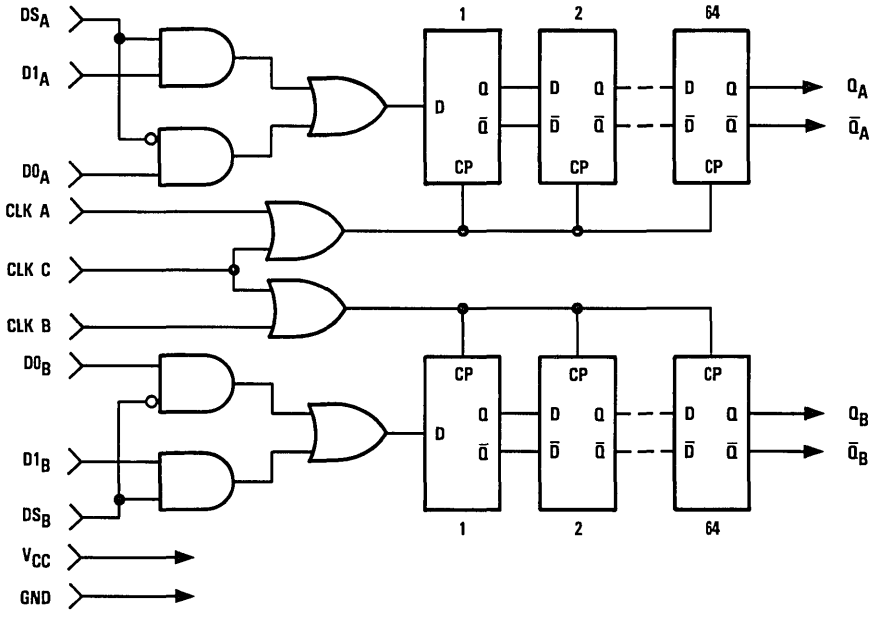
Features

- 25MHz Guaranteed Clock Frequency
- Fully TTL Compatible
- True and Complementary Outputs
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In 16 Lead Ceramic DIP
- Horizontal And Vertical Cascadability

Applications

- High-Speed Data Acquisition
- First-In First-Out Data Buffers
- Coefficient Storage For FIR Filters
- Digital Delay Lines
- Local Storage Registers

Functional Block Diagram



J

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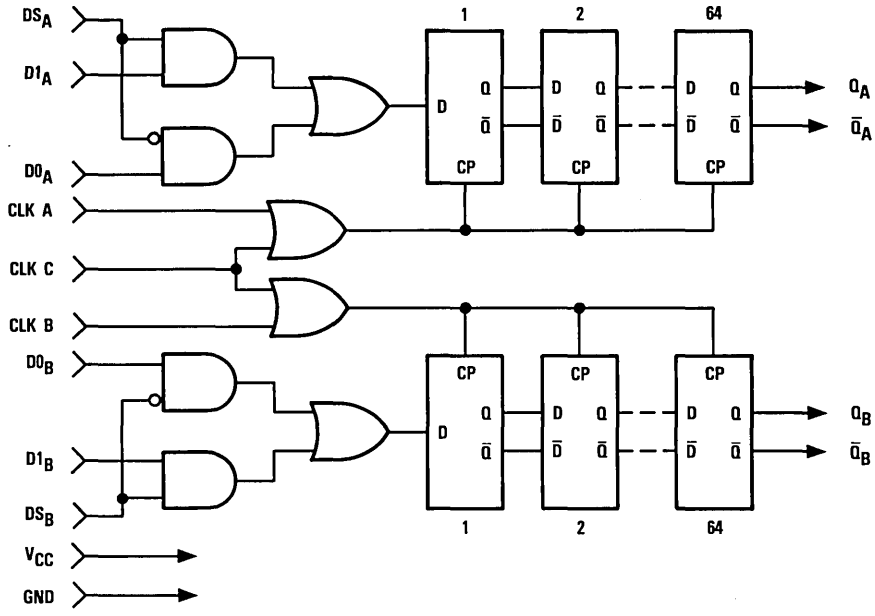
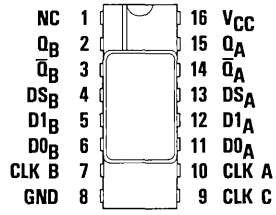
Functional Block Diagram



Pin Assignments



16 Lead DIP – J9 Package

Functional Description

General Information

The TDC1005 is a positive-edge-triggered dual 64-bit serial shift register. One of two data inputs (D0 and D1) is selected by the Data Select control (DS). Complementary outputs Q and $\overline{Q}$ are available.

Power

The TDC1005 operates from a single +5 Volt power supply.

Name	Function	Value	J9 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pin 16
GND	Ground	0.0V	Pin 8

Data Inputs

The TDC1005 has two data inputs per block, ($D0_A$ and $D0_B$, $D1_A$ and $D1_B$).

Name	Function	Value	J9 Package
$D0_A$	Data Input 0, Block A	TTL	Pin 11
$D1_A$	Data Input 1, Block A	TTL	Pin 12
$D0_B$	Data Input 0, Block B	TTL	Pin 6
$D1_B$	Data Input 1, Block B	TTL	Pin 5

Data Select

Two data select controls, one for Block A (DS_A) and one for Block B (DS_B), are provided to select between inputs 0 and 1. The 0 input is selected when DS is LOW; the 1 input is selected when DS is HIGH.

Name	Function	Value	J9 Package
DS_A	Block A Data Select	TTL	Pin 13
DS_B	Block B Data Select	TTL	Pin 4

Data Outputs

Complementary outputs Q and $\overline{Q}$ are provided for the TDC1005.

Name	Function	Value	J9 Package
QA	Data Output Block A	TTL	Pin 15
$\overline{QA}$	Data Output (Inv.) Block A	TTL	Pin 14
QB	Data Output Block B	TTL	Pin 2
$\overline{QB}$	Data Output (Inv.) Block B	TTL	Pin 3

J

Clocks

The TDC1005 has three clock inputs (CLK A, CLK B, CLK C) which are combined to provide the clock signals for the two blocks. Block A is clocked by the logical OR of CLK A and CLK C. Block B is clocked by the logical OR of CLK B and CLK C. This allows the two blocks to be clocked either independently or simultaneously.

Name	Function	Value	J9 Package
CLK A	Clock A	TTL	Pin 10
CLK B	Clock B	TTL	Pin 7
CLK C	Clock C	TTL	Pin 9

No Connects

Pin 1 on the TDC1005 is not connected internally. This pin may be left unconnected.

Name	Function	Value	J9 Package
NC	No connection	Open	Pin 1

Figure 1. Timing Diagram

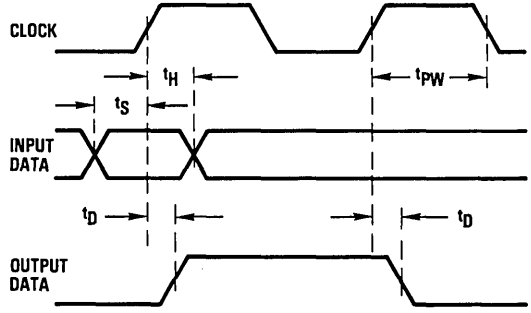


Figure 2. Input/Output Schematics

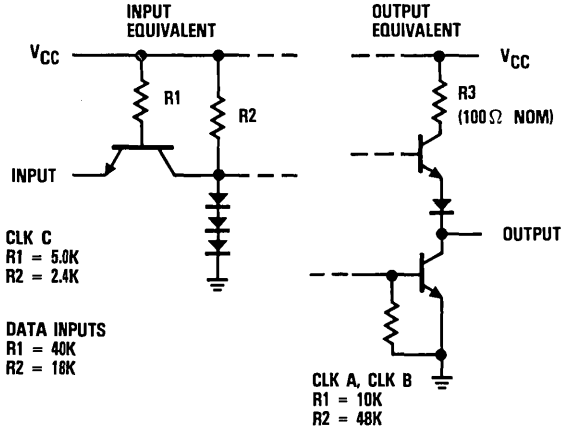
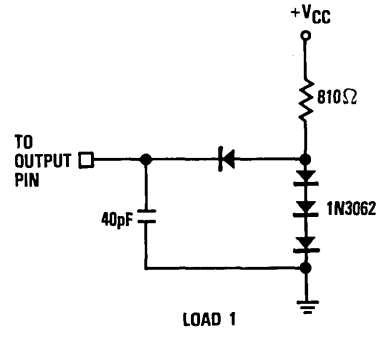


Figure 3. Test Load for Delay Measurement (Typical)



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	0 to +5.5V
Output	
Applied voltage (measured to GND)	0 to +5.5V [2]
Applied current, externally forced	−1.0 to 6.0ma [3,4]
Short circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, ambient	−55 to +150°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PW}	Clock Pulse Width	15			15			ns
t_S	Input Register Setup Time	4			4			ns
t_H	Input Register Hold Time	10			10			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

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Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = MAX		105		120	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{IL}	Input Current, Logic LOW[1]	V_{CC} = MAX, V_{IL} = 0.4V		−0.5		−0.8	mA/load
I_{IH}	Input Current, Logic HIGH[1]	V_{CC} = MAX, V_{IH} = 2.4V		20		50	μA/load

Note:

1. CLK C: Eight equivalent loads
   CLK A, CLK B: Four equivalent loads

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_C	Clock Frequency	(See Figure 3)	25		25		MHz
t_D	Output Delay	(See Figure 3)		30		30	ns

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1005J9C	STD–T_A = 0°C to 70°C	Commercial	16 Lead DIP	1005J9C
TDC1005J9G	STD–T_A = 0°C to 70°C	Commercial with Burn-In	16 Lead DIP	1005J9G
TDC1005J9F	EXT–T_C = −55°C to 125°C	Commercial	16 Lead DIP	1005J9F
TDC1005J9A	EXT–T_C = −55°C to 125°C	*High Reliability*[1]	16 Lead DIP	1005J9A

Note:

1. *Per TRW document 70Z01757.*

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TDC1006

Serial Shift Register
256-bit

The TRW TDC1006 is a positive-edge-triggered serial shift register which operates at 25MHz. The device is cascadable in the number of words and the word size.

Complementary TTL outputs Q and $\overline{Q}$ are provided. Two data inputs, D0 and D1, are controlled by a data select input, DS. This provides on-chip recirculate gating when the true output is hard-wired to one of the inputs.

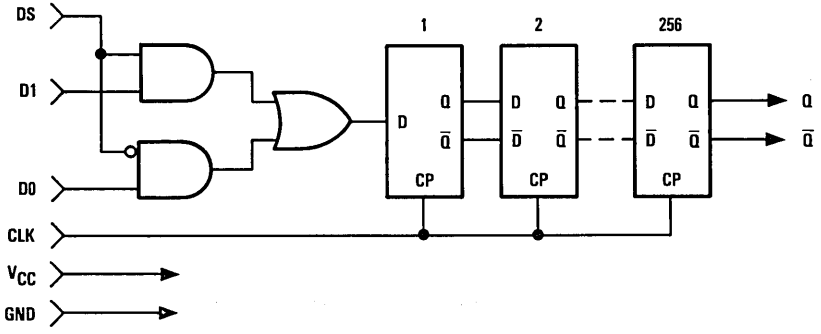
Features

- 25MHz Guaranteed Clock Frequency
- Fully TTL Compatible
- True and Complementary Outputs
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available in 16 Lead Ceramic DIP
- Horizontal and Vertical Cascadability

Applications

- High-Speed Data Acquisition
- First-In First-Out Data Buffers
- Coefficient Storage for FIR Filters
- Digital Delay Lines
- Local Storage Registers

Functional Block Diagram



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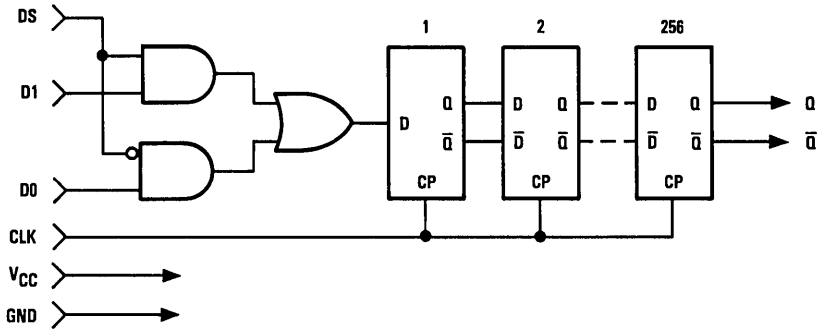
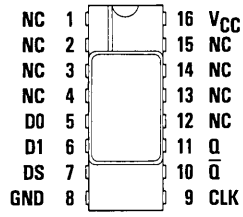
Functional Block Diagram



Pin Assignments



16 Lead DIP – J9 Package

Functional Description

General Information

The TDC1006 is a 256-bit positive-edge-triggered serial shift register. One of two data inputs (D0 and D1) is selected by the Data Select control DS. Complementary outputs Q and $\overline{Q}$ are available.

Power

The TDC1006 operates from a single +5 Volt power supply.

Name	Function	Value	J9 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pin 16
GND	Ground	0.0V	Pin 8

Data Inputs

The TDC1006 is a single 256-bit shift register with two data inputs D0 and D1.

Name	Function	Value	J9 Package
D0	Data Input 0	TTL	Pin 5
D1	Data Input 1	TTL	Pin 6

Data Select

The TDC1006 has one data select control (DS) to select between inputs D0 and D1. Input D1 is selected when DS is HIGH, D0 is selected when DS is LOW.

Name	Function	Value	J9 Package
DS	Data Select	TTL	Pin 7

Data Outputs

Complementary outputs Q and $\overline{Q}$ are provided for the TDC1006.

Name	Function	Value	J9 Package
Q	Data Output	TTL	Pin 11
$\overline{Q}$	Data Output Inverted	TTL	Pin 10

Clocks

The TDC1006 has one clock signal, CLK.

Name	Function	Value	J9 Package
CLK	Clock	TTL	Pin 9

No Connects

There are several pins on the TDC1006 which are not connected internally. These pins may be left unconnected.

Name	Function	Value	J9 Package
NC	No Connect	Open	Pins 1-4, 12-15

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Figure 1. Timing Diagram

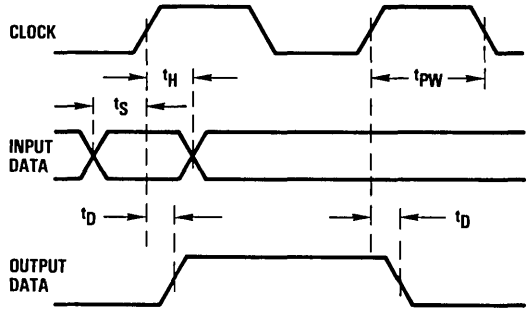


Figure 2. Equivalent Input/Output Schematics

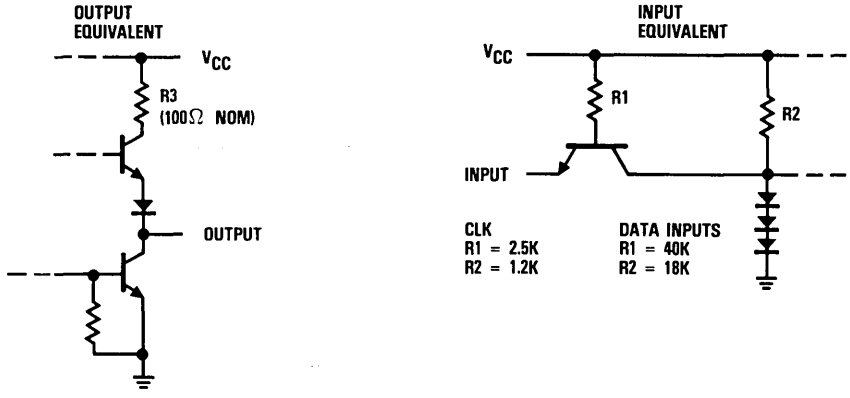
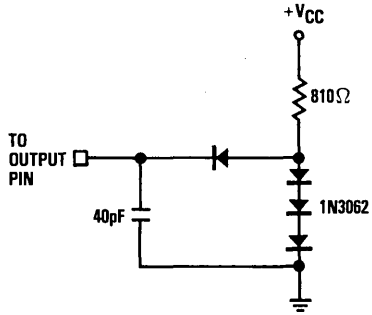


Figure 3. Test Load



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0 V
Input Voltage	0 to +5.5V
Output	
Applied voltage (measured to GND)	0 to +5.5V [2]
Applied current, externally forced	−1.0 to +6.0mA [3,4]
Short circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, ambient	−55 to +150°C
junction	+175°C
Lead, soldering (10 sec.)	+300°C
Storage	−65 to +160°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PW}	Clock Pulse Width	15			15			ns
t_S	Input Register Setup Time	4			4			ns
t_H	Input Register Hold Time	10			10			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

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Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = MAX		135		155	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{IL}	Input Current, Logic LOW[1]	V_{CC} = MAX, V_{IL} = 0.4V		-0.5		-0.8	mA/load
I_{IH}	Input Current, Logic HIGH[1]	V_{CC} = MAX, V_{IH} = 2.4V		20		50	μA/load

Note:
1. CLK: Sixteen equivalent loads.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_C	Clock Frequency	(See Figure 1)	25		25		MHz
t_D	Output Delay	(See Figure 1)		30		30	ns

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1006J9C	STD-T_A = 0°C to 70°C	Commercial	16 Lead DIP	1006J9C
TDC1006J9G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	16 Lead DIP	1006J9G
TDC1006J9F	EXT-T_C = -55°C to 125°C	Commercial	16 Lead DIP	1006J9F
TDC1006J9A	EXT-T_C = -55°C to 125°C	High Reliability[1]	16 Lead DIP	1006J9A

Note:
1. Per TRW document 70Z01757.

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TDC1011
Preliminary Information

Variable-Length Shift Register
8-bit, 18MHz

The TRW TDC1011 is a high-speed, byte-wide shift register which can be programmed to any length between 3 and 18 stages. It operates at a 56 nanosecond cycle time (18MHz shift rate). A special split-word mode is provided for use with the TRW TDC1028.

The TDC1011 is fully synchronous, with all operations controlled by a single master clock. Input and output registers are positive-edge-triggered D-type flip-flops. The length control inputs are also registered.

Built with TRW's OMICRON-B™ 1-micron bipolar process, the TDC1011 provides the system designer with a unique variable-delay capability at video speeds.

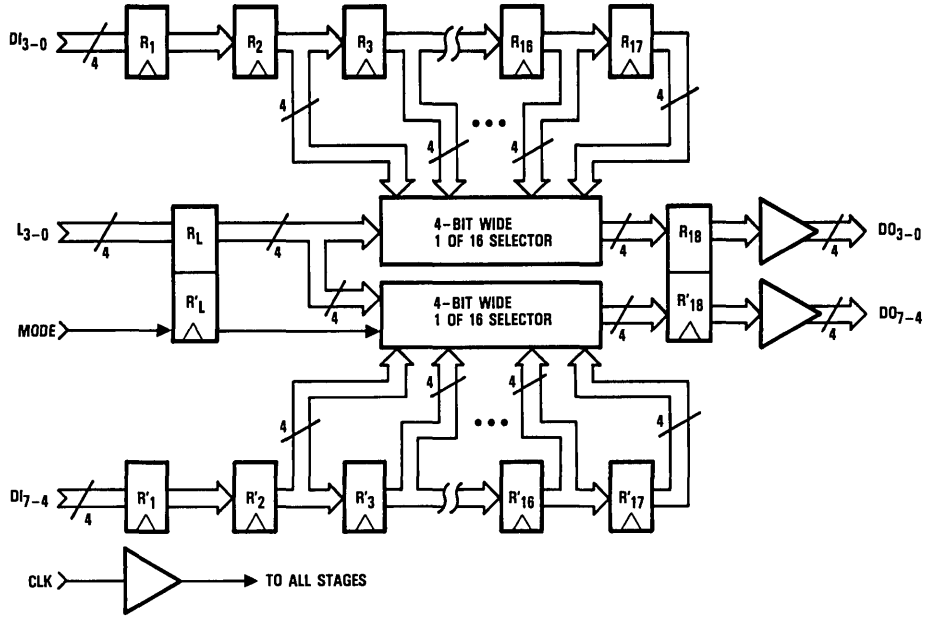
Features

- 56ns Cycle Time (Worst Case)
- Single +5V Power Supply
- TTL Compatible
- Selectable Length From 3 To 18 Stages
- Special 4-Bit Wide Mixed-Delay Mode
- Available In 24 Lead DIP and CERDIP

Applications

- Word Size Expansion Of TDC1028
- Video Filtering
- *High-Speed Data Acquisition*
- Local Storage Registers
- Digital Delay Lines
- Television Special Effects

Functional Block Diagram



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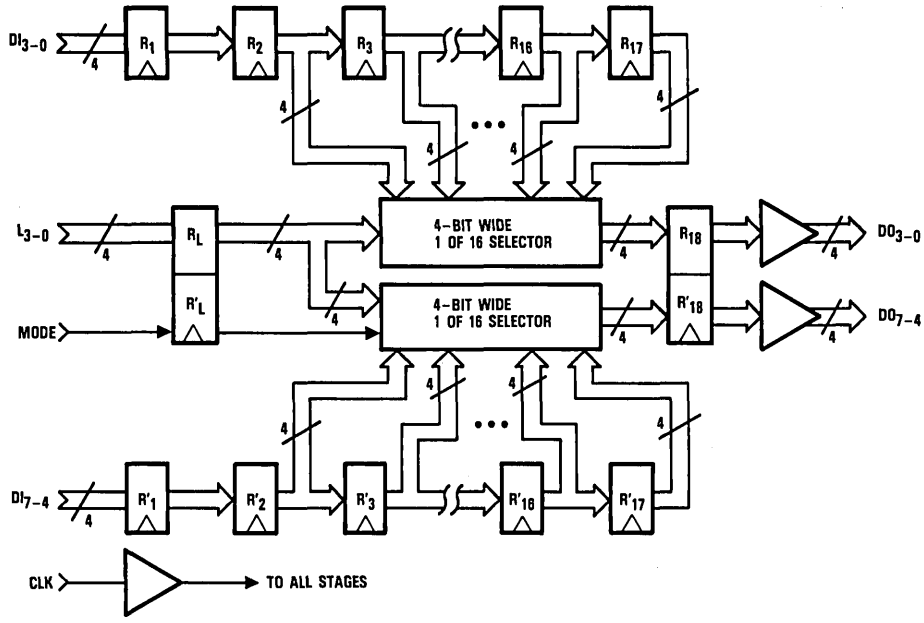
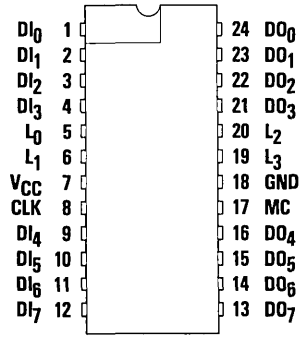
Functional Block Diagram



Pin Assignments



24 Lead DIP – J7 Package
24 Lead CERDIP – B7 Package

Functional Description

General Information

The TDC1011 consists of two 4-bit wide, adjustable length shift registers. These registers share control signals and a common clock.

Power

The TDC1011 operates from a single +5 Volt supply.

Name	Function	Value	J7, B7 Package
V_{CC}	Positive Supply Voltage	5.0V	Pin 7
GND	Ground	0.0V	Pin 18

Inputs

The eight inputs to the TDC1011 are divided into two groups of four, and are intended to support the TDC1028, which has inputs in groups of four bits. The lengths of these two groups are different when the Mode Control (MC) is HIGH (refer to Controls Section). The incoming data is unchanged by the TDC1011. All inputs are fully TTL compatible and all internal circuitry is static.

Name	Function	Value	J7, B7 Package
DI_0	Data Input	TTL	Pin 1
DI_1		TTL	Pin 2
DI_2		TTL	Pin 3
DI_3		TTL	Pin 4
DI_4		TTL	Pin 9
DI_5		TTL	Pin 10
DI_6		TTL	Pin 11
DI_7	Data Input	TTL	Pin 12

Outputs

The outputs of the TDC1011 are delayed relative to the input signals. The amount of the delay is programmable (refer to Controls Section). The outputs remain valid for a minimum of t_{HO} nanoseconds after the leading edge of CLK. This allows the data to be latched into circuits with non-zero hold time requirements.

Name	Function	Value	J7, B7 Package
DO_0	Data Output	TTL	Pin 24
DO_1		TTL	Pin 23
DO_2		TTL	Pin 22
DO_3		TTL	Pin 21
DO_4		TTL	Pin 16
DO_5		TTL	Pin 15
DO_6		TTL	Pin 14
DO_7	Data Output	TTL	Pin 13

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Clock

The TDC1011 operates synchronously from a single master clock line, which can be clocked up to 18MHz. All operations occur at the rising edge of the master clock. Since the internal circuitry is static, the clock can be gated if desired.

Name	Function	Value	J7, B7 Package
CLK	Clock	TTL	Pin 8

Controls

The TDC1011 has four length selection controls and one mode selection control. The operation of these controls is shown in Table I.

Name	Function	Value	J7, B7 Package
L_0	Length Select LSB	TTL	Pin 5
L_1	Length Select	TTL	Pin 6
L_2	Length Select	TTL	Pin 20
L_3	Length Select MSB	TTL	Pin 19
MC (Mode)	Mode Control	TTL	Pin 17

Length Programming Table I

Input Code				Mode (MC) = 0		Mode (MC) = 1	
L_3	L_2	L_1	L_0	DO_{3-0} Length	DO_{7-4} Length	DO_{3-0} Length	DO_{7-4} Length
0	0	0	0	3	3	3	18
0	0	0	1	4	4	4	18
0	0	1	0	5	5	5	18
0	0	1	1	6	6	6	18
0	1	0	0	7	7	7	18
0	1	0	1	8	8	8	18
0	1	1	0	9	9	9	18
0	1	1	1	10	10	10	18
1	0	0	0	11	11	11	18
1	0	0	1	12	12	12	18
1	0	1	0	13	13	13	18
1	0	1	1	14	14	14	18
1	1	0	0	15	15	15	18
1	1	0	1	16	16	16	18
1	1	1	0	17	17	17	18
1	1	1	1	18	18	18	18

Figure 1. Timing Diagram (Preset Length Controls)

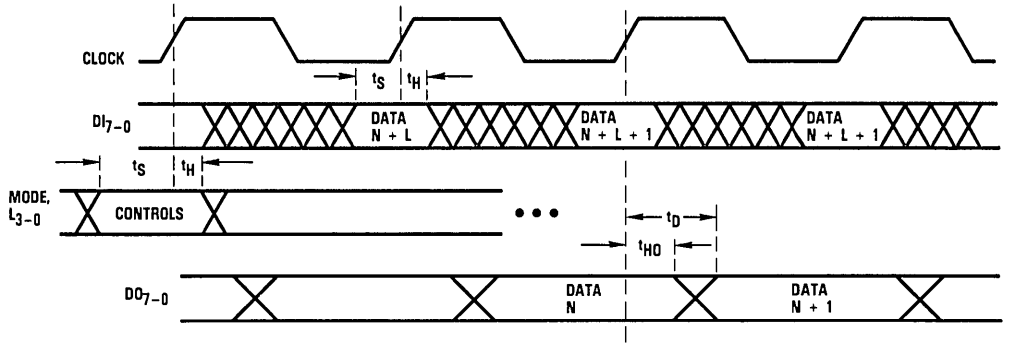


Figure 2. Length Control Operation

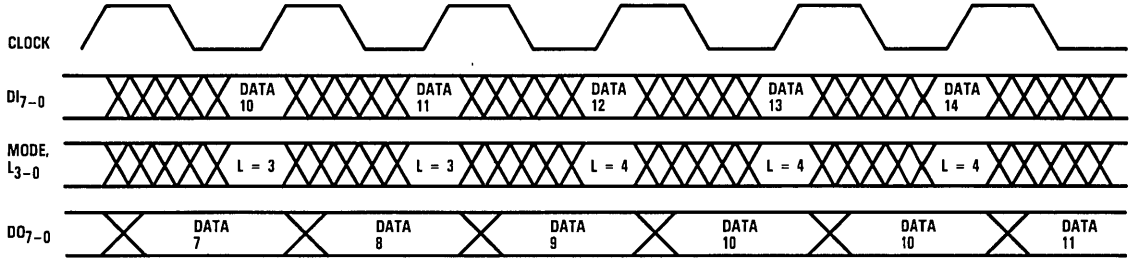
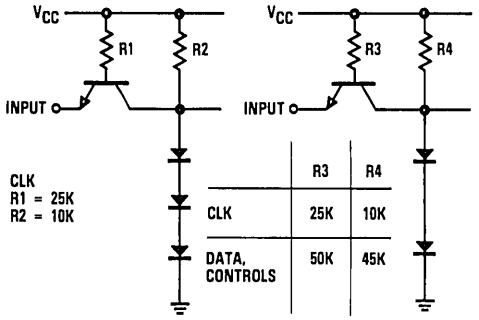


Figure 3. Equivalent Input Circuit



	R3	R4
CLK	25K	10K
DATA, CONTROLS	50K	45K

Figure 4. Equivalent Output Circuit

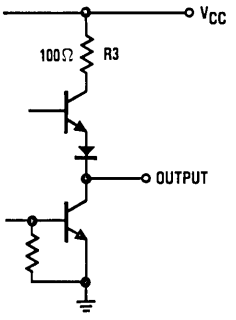
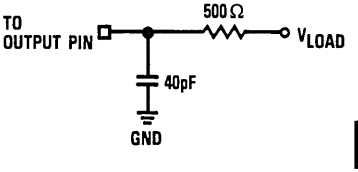


Figure 5. Test Load



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Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage ..... −0.5 to +7.0V

Input

Applied voltage ..... −0.5 to +5.5V[2]

Forced current ..... −6.0 to +6.0mA

Output

Applied voltage ..... −0.5 to +5.5V[2]

Forced current ..... −1.0 to +6.0mA[3,4]

Short circuit duration (single output in high state to ground) ..... 1 sec

Temperature

Operating, case ..... −55 to +125°C

junction ..... 175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PWL}	Clock Pulse Width, LOW	15			15			ns
t_{PWH}	Clock Pulse Width, HIGH	15			15			ns
t_S	Input Setup Time	20			25			ns
t_H	Input Hold Time	0			2			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = MAX, Static[1]		150		200	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V					
		Data Inputs		-0.4		-0.4	mA
		Clock		-1.0		-1.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V		75		75	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OS}	Short-Circuit Output Current	V_{CC} = MAX, One pin to ground, one second duration max, output HIGH	-5	-40	-5	-40	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:
1. Worst case, all inputs and outputs LOW.

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
f_{CLK}	Clock Rate	V_{CC} = MIN					
		Static Length Controls	18		15		MHz
		Dynamic Length Controls	15		10		MHz
t_D	Output Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V		25		30	ns
t_{HO}	Output Hold Time[2]	V_{CC} = MAX, Test Load: V_{LOAD} = 2.2V	5		5		ns

Notes:
1. All transitions are measured at a 1.5V level.
2. Guaranteed, not tested.

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Application Notes

The TDC1011 has two types of applications: as a support device for the TDC1028, and as a general variable-length shift register.

To support the TDC1028, the lengths will be set to one of the following:

1. Both sections 9 stages long.
2. One section 9 stages long, the other section 18 stages long.
3. Both sections 18 stages long.

The sections are interchangeable only if the lengths are identical.

Further description of the use of the TDC1011 to support the TDC1028 is given in TRW LSI Products Application Note TP-22.

For general use, it is important to note that the length control inputs are registered. There are no constraints on the use of the control leads other than the operational requirements shown in the Operating Conditions table. Specifically, the length can be increased from one clock period to another and proper operation will occur; no data is lost, except the eighteenth stage.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1011J7C	STD-T_A = 0°C to 70°C	Commercial	24 Lead DIP	1011J7C
TDC1011J7G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	24 Lead DIP	1011J7G
TDC1011J7F	EXT-T_C = -55°C to 125°C	Commercial	24 Lead DIP	1011J7F
TDC1011J7A	EXT-T_C = -55°C to 125°C	High Reliability[1]	24 Lead DIP	10llJ7A
TDC1011B7C	STD-T_A = 0°C to 70°C	Commercial	24 Lead CERDIP	1011B7C
TDC1011B7G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	24 Lead CERDIP	1011B7G

Note:

1. Per TRW document 70Z01757.

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Preliminary Information describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact TRW for current information.

TDC1030
Preliminary Information

First-In First-Out Memory
64 words by 9 bits cascadable

The TRW TDC1030 is an expandable, First-In First-Out (FIFO) memory organized as 64 words by 9 bits. A 15MHz data rate makes it ideal in high-speed applications. Burst data rates of 18MHz can be obtained in applications where the device status flags are not used.

With separate Shift-In (SI) and Shift-Out (SO) controls, reading and writing operations are completely independent, allowing synchronous and asynchronous data transfers. Additional controls include a Master Reset ($\overline{MR}$), and Output Enable ($\overline{OE}$). Input Ready (IR) and Output Ready (OR) flags are provided to indicate device status.

Devices can be easily interconnected to expand word and bit dimensions. The device has all output pins directly opposite the corresponding input pins, facilitating board layouts in expanded format. All inputs and outputs are TTL compatible.

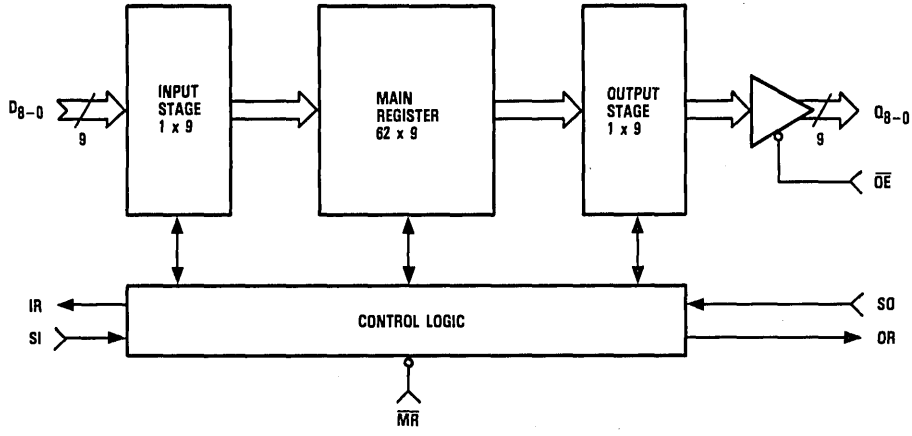
Features

- 64 Words By 9 Bits Organization
- 15MHz Shift-In, Shift-Out Rates With Flags
- 18MHz Burst-In, Burst-Out Rates Without Flags
- Cascadable To 13MHz
- Readily Expandable In Word And Bit Dimension
- TTL Compatible
- Asynchronous Or Synchronous Operation
- Three-State Outputs
- Master Reset Input To Clear Control
- Output Pins Directly Opposite Corresponding Input Pins For Easy Board Layout
- Available in 28 Lead Ceramic DIP, CERDIP, or Contact Chip Carrier

Applications

- High-Speed Disk Or Tape Controller
- Video Time Base Correction
- A/D Output Buffers
- Voice Synthesis
- Input/Output Formatter For Digital Filters and FFTs

Functional Block Diagram



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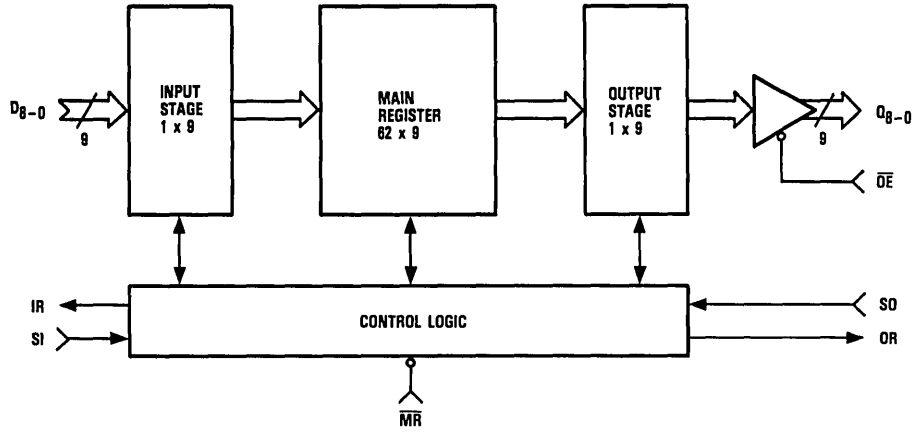
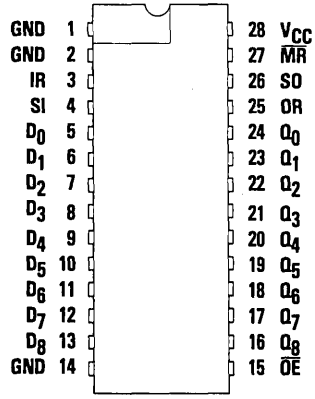
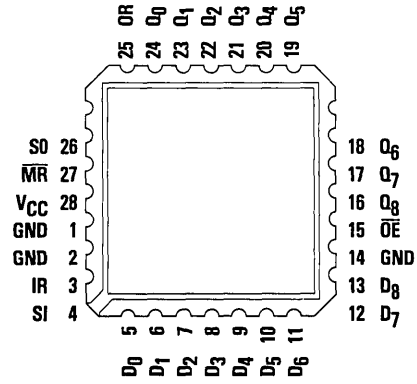
Functional Block Diagram



Pin Assignments



28 Lead DIP – J6 Package
28 Lead CERDIP – B6 Package



28 Contact Chip Carrier – C3 Package

Functional Description

Data Input (Figure 1)

Following power up, the Master Reset ($\overline{MR}$) is pulsed LOW to clear the FIFO (Figure 2). The Input Ready (IR) flag HIGH indicates that the FIFO input stage is empty and available to receive data. When IR is valid (HIGH), Shift-In (SI) may be asserted, thus loading the data present at D_0 through D_8 into the FIFO. Bringing the SI signal HIGH causes IR to drop LOW. The data remains at the first location until SI is set LOW. With SI LOW, the data then propagates to the second location and continues to "fall through" to the output stage or last empty location. If the FIFO is not full after the SI pulse, IR will again be valid (HIGH), indicating that there is space available in the FIFO. If the memory is full, the IR flag remains invalid (LOW).

With the FIFO full, the SI can be held HIGH until a Shift-Out (SO) occurs (Figure 3). Following the SO pulse, the empty location "bubbles up" to the input stage. This results in an Input Ready (IR) pulse HIGH and awaiting data is shifted in. The SI must be brought LOW before additional data can be shifted in.

Data Transfer

After data has been transferred into the second location by bringing SI LOW, the data continues to "fall through" the FIFO in an asynchronous manner. The data stacks up at the end of the device, leaving the empty locations up front.

Data Output (Figure 4)

The Output Ready (OR) flag HIGH indicates that there is valid data at the output stage (pins Q_0-Q_8). An initial Master Reset ($\overline{MR}$) pulse LOW at power up sets the Output Ready LOW (Figure 2). Although the internal control circuitry is cleared, random data remains on the output pins. Data shifted into the FIFO (after $\overline{MR}$) "falls through" to the output stage, causing OR to go HIGH, and replaces the random data with valid data.

When the OR flag is valid (HIGH), data can be transferred out via the Shift-Out (SO) control. An SO HIGH results in a "busy" (LOW) signal at the OR flag. When SO is brought LOW, data is shifted to the output stage, and the empty location "bubbles up" to the input stage. At the completion of the SO pulse, OR goes HIGH. If the last valid piece of data has been shifted out, leaving the memory empty, the OR flag remains invalid (LOW). With the FIFO empty, the last word shifted out remains on the output pins Q_0-Q_8.

With the FIFO empty, the SO can be held HIGH until a SI occurs (Figure 5). Following the SI pulse, the data "falls through" to the output stage. This results in an OR pulse HIGH and data is shifted out. The SO must be brought LOW before additional data can be shifted out.

Data Inputs

The nine data inputs of the TDC1030 are TTL compatible. There is no weighting to the inputs, and any one of them can be assigned as the MSB. The memory size of the FIFO can be reduced from the 9 x 64 configuration by leaving open unused data input pins (i.e., 8 x 64, 7 x 64 . . . 1 x 64). In the reduced format, the unused data output pins must also be left open.

Name	Function	Value	J6, C3, B6 Package
D_0	Data Input	TTL	Pin 5
D_1		TTL	Pin 6
D_2		TTL	Pin 7
D_3		TTL	Pin 8
D_4		TTL	Pin 9
D_5		TTL	Pin 10
D_6		TTL	Pin 11
D_7		TTL	Pin 12
D_8	Data Input	TTL	Pin 13

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Data Outputs

The nine data outputs of the TDC1030 are TTL compatible, capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. There is no weighting to the outputs, and any one of them can be assigned as the MSB.

The memory size of the FIFO can be reduced from the 9 x 64 configuration by leaving open unused data output pins (i.e., 8 x 64, 7 x 64 . . . 1 x 64). In the reduced format, the unused data input pins must also be left open.

Name	Function	Value	J6, C3, B6 Package
Q_0	Data Output	TTL	Pin 24
Q_1		TTL	Pin 23
Q_2		TTL	Pin 22
Q_3		TTL	Pin 21
Q_4		TTL	Pin 20
Q_5		TTL	Pin 19
Q_6		TTL	Pin 18
Q_7		TTL	Pin 17
Q_8	Data Output	TTL	Pin 16

Controls

SI — The rising edge loads data into the input stage. The falling edge triggers the automatic data transfer process.

SO — The rising edge causes OR to go LOW. The falling edge moves upstream data into the output stage and triggers the "bubble up" process of empty locations.

$\overline{MR}$ — $\overline{MR}$ LOW clears all data and control within the FIFO: Input Ready flag is set HIGH, Output Ready flag is set LOW, and the FIFO is cleared. The output stage remains in the state of the last word shifted out, or in the random state of power up.

$\overline{OE}$ — With the $\overline{OE}$ LOW, the outputs of the FIFO are TTL compatible. When disabled ($\overline{OE}$ HIGH), the outputs go into their high-impedance state.

Name	Function	Value	J6, C3, B6 Package
SI	Shift-In	TTL	Pin 4
SO	Shift-Out	TTL	Pin 26
$\overline{MR}$	Master Reset	TTL	Pin 27
$\overline{OE}$	Output Enable	TTL	Pin 15

Power

The TDC1030 operates from a single +5.0V supply. All power and ground pins must be connected.

Name	Function	Value	J6, C3, B6 Package
V_{CC}	Supply Voltage	+5.0	Pin 28
GND	Digital Ground	0.0	Pins 1, 2, 14

Status Flags

Input Ready (IR) and Output Ready (OR) flags are provided to indicate the status of the FIFO. Operation with use of the flags is explained in the Functional Description. In this mode of operation, the Shift-In and Shift-Out rates are determined by the status flags. It is assumed that a Shift-In or Shift-Out pulse is not applied until the respective flag (IR, OR) is valid (Figures 1 and 4).

The IR and OR flags are not required to operate the device. A high-speed burst mode is achievable when operating without the flags. Refer to the High-Speed Burst Mode section for a complete description.

IR — An IR flag HIGH indicates that the input stage is empty and ready to accept valid data. An IR LOW indicates that the FIFO is full or that a previous SI operation is not complete.

OR — An OR flag HIGH assures valid data at the output stage (pins Q_0-Q_8). However, the OR flag does not indicate whether or not there is any new data awaiting transfer into the output stage. An OR LOW indicates that the output stage is "busy", or that there is no valid data.

Name	Function	Value	J6, C3, B6 Package
IR	Input Ready Flag	TTL	Pin 3
OR	Output Ready Flag	TTL	Pin 25

Application Notes

Expanded Format

The TDC1030 is easily cascaded to increase word capacity without any external circuitry. Word capacity can be expanded beyond the 128 words X 9 bits configuration shown in Figure 6. In the cascaded format, all necessary communications and timing are handled by the FIFOs themselves. The intercommunication speed is controlled by the minimum flag pulse widths and the flag delays. (See Figures 7 and 8.)The maximum data rate when cascading devices is 13MHz.

With the addition of a logic gate, the FIFO is easily expanded to increase word length (Figure 9). The basic operation and timing are identical to a single FIFO, with the exception of an additional gate delay on the flags. Word length can be expanded beyond the 18 bits X 64 words configuration shown in Figure 9.

High-Speed Burst Mode

Burst rates of 18MHz can be obtained for applications in which the device status flags are not used. In this mode of operation, the Burst-In and Burst-Out rates are determined by the minimum Shift-In Pulse Widths, and Shift-Out Pulse Widths (See Figures 10 and 11). With the Input Ready and Output Ready flags not monitored, a shift pulse can be applied without regard to the status flag. However, a Shift-In pulse which would overflow the storage capacity of the FIFO is not permitted.

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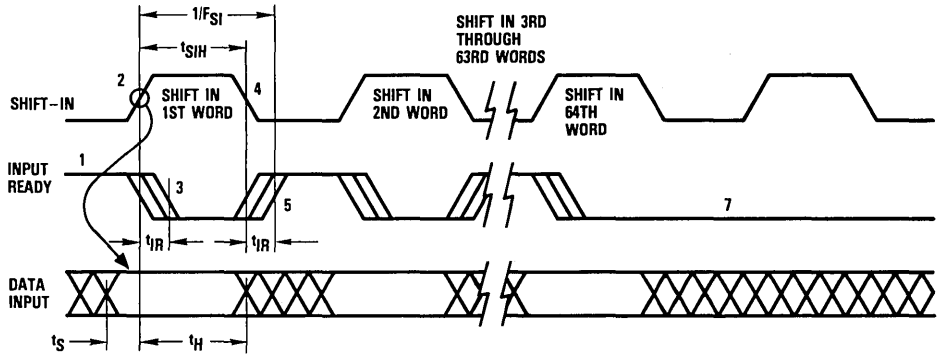
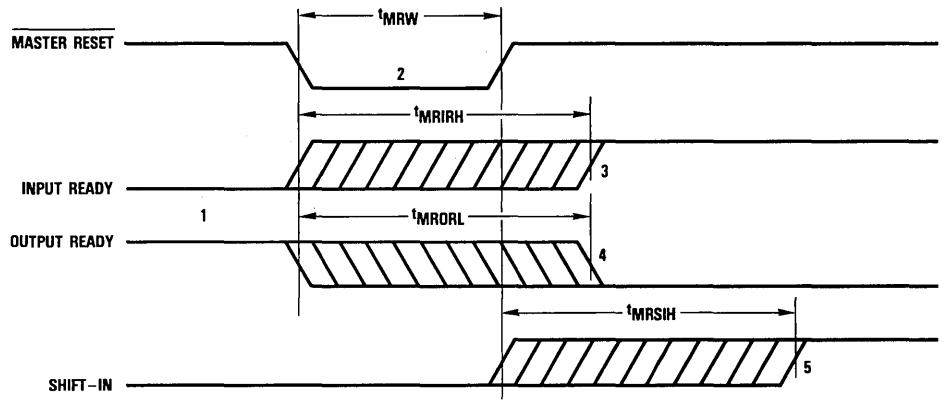
TDC1030 Timing Diagrams

Figure 1. Shifting In Sequence, FIFO Empty To FIFO Full



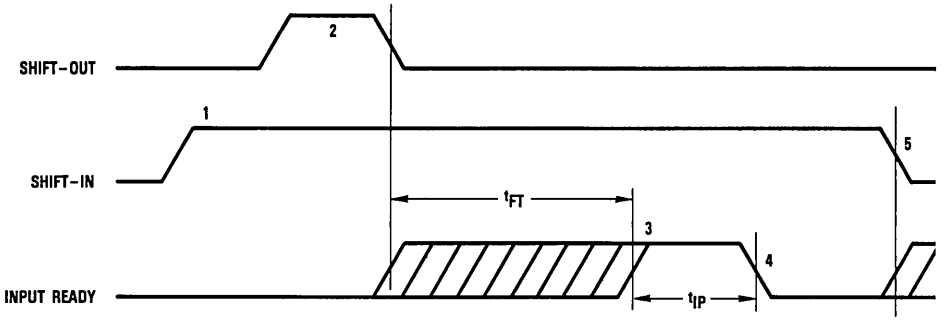
1. Input Ready initially HIGH – FIFO is prepared for valid data.
2. Shift-In set HIGH – data loaded into input stage.
3. Input Ready drops LOW (t_{IR} delay after SI HIGH) – input stage "busy."
4. Shift-In set LOW – data from first location "falls through."
5. Input Ready goes HIGH (t_{IR} delay after SI LOW) – status flag indicates FIFO prepared for additional data.
6. Repeat process to load 2nd through 64th word into FIFO.
7. Input Ready remains LOW – with attempt to shift into full FIFO, no data transfer occurs.

Figure 2. Master Reset Applied With FIFO Full



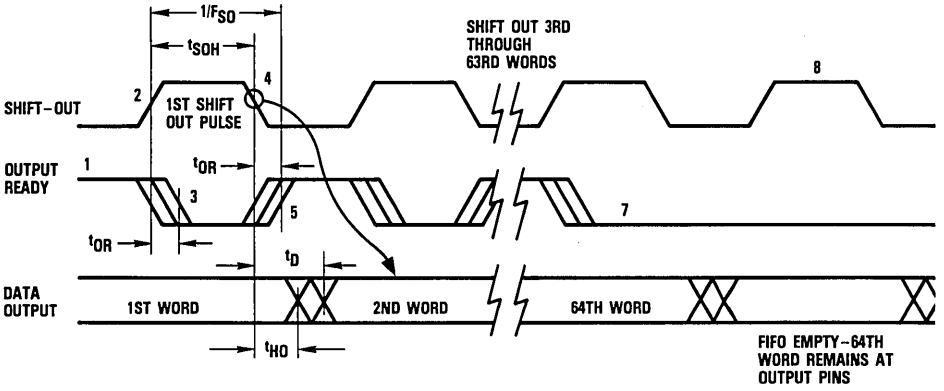
1. Input Ready LOW, Output Ready HIGH – assume FIFO is full.
2. Master Reset pulse LOW – clears FIFO.
3. Input Ready goes HIGH (t_{MRIRH} delay after $\overline{MR}$) – flag indicates input prepared for valid data.
4. Output Ready drops LOW (t_{MRORL} delay after $\overline{MR}$) – flag indicates FIFO empty.
5. Shift-In HIGH (t_{MRSI} delay after $\overline{MR}$) – clearing process complete, move new data into FIFO.

Figure 3. With FIFO Full, Shift–In Held High In Anticipation Of Empty Location



1. FIFO is initially full, Shift–In is held HIGH.
2. Shift–Out pulse – data in the output stage is unloaded, "bubble up" process of empty location begins.
3. Input Ready HIGH (t_{FT} fallthrough delay after SO pulse) – when empty location reaches input stage, flag indicates FIFO is prepared for data input.
4. Input Ready returns LOW – data Shift–In to empty location is complete, FIFO is again full.
5. SI brought LOW – necessary to complete Shift–In process, allows data "fall through" if additional empty location "bubbles up."

Figure 4. Shifting Out Sequence, FIFO Full to FIFO Empty



1. Output Ready HIGH – no data transferring in progress, valid data is present at output stage.
2. Shift–Out set HIGH – results in OR LOW.
3. Output Ready drops LOW (t_{OR} delay after SO HIGH) – output stage "busy."
4. Shift–Out set LOW – data in the input stage is unloaded, and new data replaces it as empty location "bubbles up" to input stage.
5. Output Ready goes HIGH – transfer process completed, valid data present at output.
6. Repeat process to unload the 3rd through 64th word from FIFO.
7. Output Ready remains LOW – FIFO is empty.
8. Shift–Out pulse asserted – with attempt to unload from empty FIFO, no data transfer occurs.

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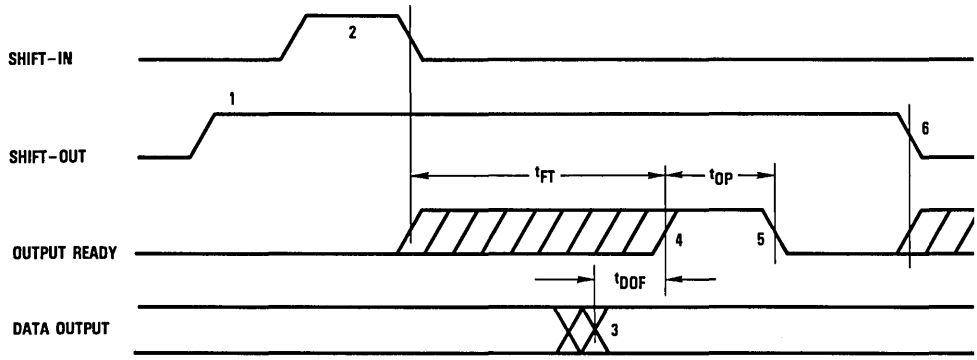
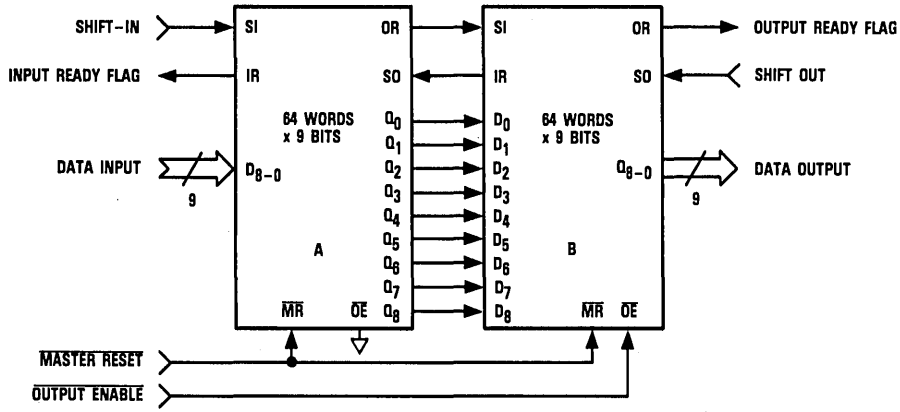
Figure 5. With FIFO Empty Shift Out Is Held High In Anticipation Of Data



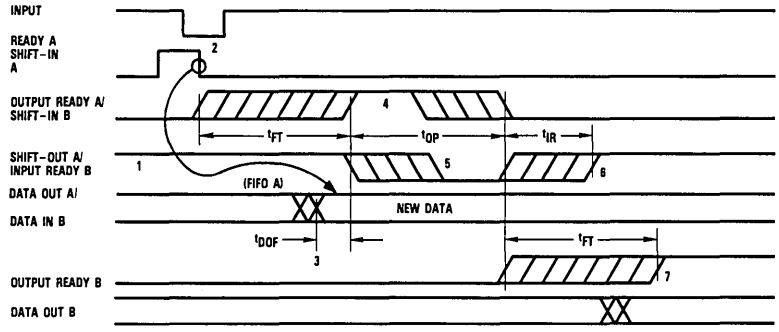
1. FIFO is initially empty, Shift-Out is held HIGH.
2. Shift-In pulse - loads data into FIFO and initiates "fall through" process.
3. Data Output transition - (t_{DOF} delay before OR HIGH), valid data arrives at output stage.
4. Output Ready HIGH - (t_{FT} fallthrough delay after SI pulse), OR flag signals the arrival of valid data at the output stage.
5. Output Ready goes LOW - data Shift-Out is complete, FIFO is again empty.
6. Shift-Out set LOW - necessary to complete Shift-Out process, allows "bubble up" of empty location as data "falls through."

Figure 6. Cascading For Increased Word Capacity - 128 Words X 9 Bits



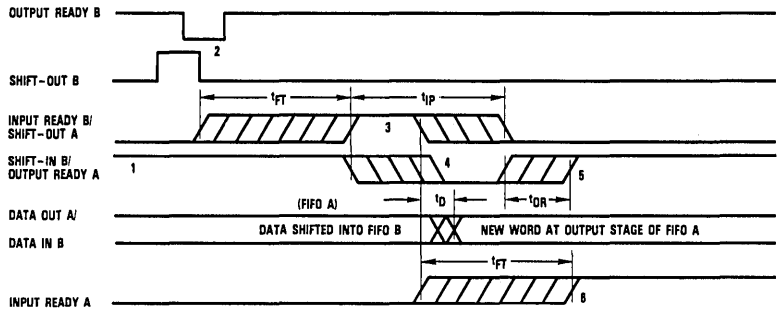
The TDC1030 is easily cascaded to increase word capacity without any external circuitry. In the cascaded format, all necessary communications are handled by the FIFOs themselves. Figures 7 and 8 demonstrate the intercommunication timing between FIFO A and FIFO B.

Figure 7. FIFO – FIFO Communication: Input Timing Under Empty Condition



1. FIFO A and B initially empty, SO (A) held HIGH in anticipation of data.
2. Load one word into FIFO A – SI pulse applied, IR pulse results.
3. Data Out A/Data In B transition – (t_{DOF} delay before OR (A) HIGH), valid data arrives at FIFO A output stage prior to OR flag, meeting data input setup requirements of FIFO B.
4. OR (A) and SI (B) pulse HIGH – (t_{FT} delay after SI (A) LOW), data is unloaded from FIFO A as a result of the Output Ready Pulse (T_{OP}), data is shifted into FIFO B.
5. IR (B) and SO (A) go LOW – (t_{IR} delay after SI (B) HIGH), flag indicates input stage of FIFO B is "busy," Shift-Out of FIFO A is complete.
6. IR (B) and SO (A) go HIGH – (t_{IR} delay after SI (B) LOW), input stage of FIFO B is again available to receive data, SO is held HIGH in anticipation of additional data.
7. OR (B) goes HIGH – (t_{FT} delay after SI (B) LOW), valid data is present at the FIFO B output stage.

Figure 8. FIFO – FIFO Communication: Output Timing Under Full Condition



1. FIFO A and B initially full, SI (B) held HIGH in anticipation of shifting in new data as empty location "bubbles up."
2. Unload one word from FIFO B – SO pulse applied, OR pulse results.
3. IR (B) and SO (A) pulse HIGH – (t_{FT} delay after SO (B) LOW), data is loaded into FIFO B as a result of the Input Ready Pulse (tIP), data is shifted out of FIFO A.
4. OR (A) and SI (B) go LOW – (t_{OR} delay after SO (A) HIGH), flag indicates the output stage of FIFO A is "busy," Shift-In to FIFO B is complete.
5. OR (A) and SI (B) go HIGH – (t_{OR} delay after SO (A) LOW), flag indicates valid data is again available at the FIFO A output stage, SI (B) is held HIGH, awaiting "bubble up" of empty location.
6. IR (A) goes HIGH – (t_{FT} delay after SO (A) LOW), an empty location is present at input stage of FIFO A.

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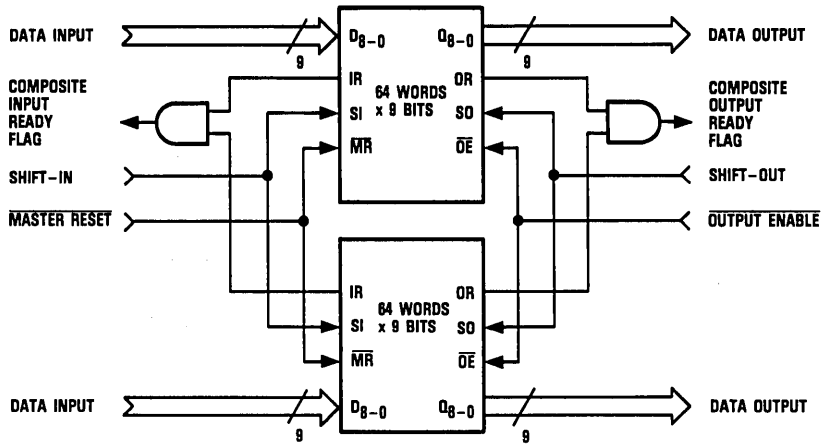
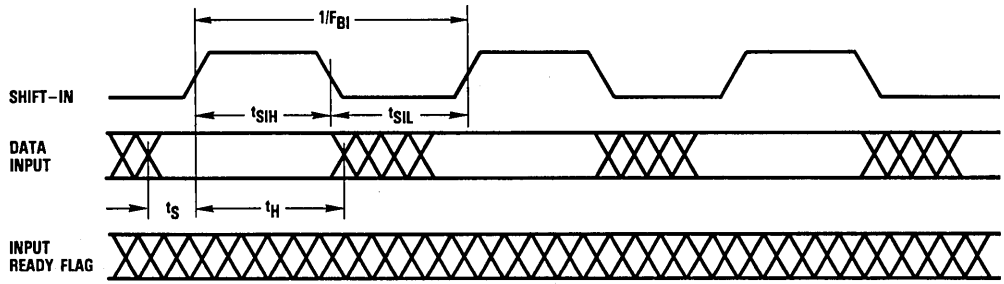
Figure 9. Expanded FIFO for Increased Word Length – 64 Words X 18 Bits



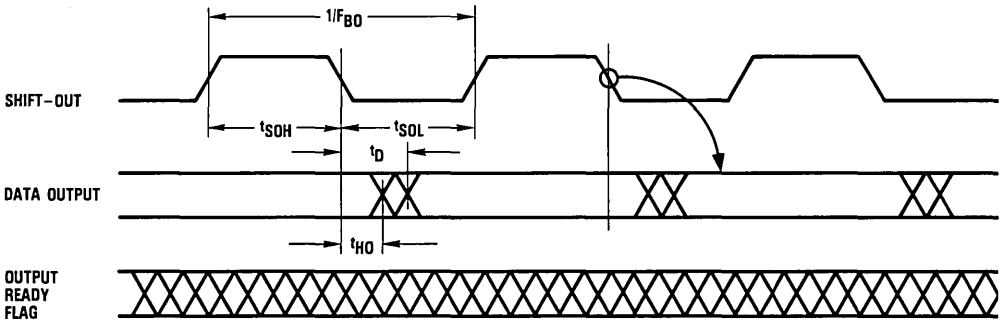
The TDC1030 is easily expanded to increase word length. Composite Input Ready and Output Ready flags are formed with the addition of an AND logic gate. The basic operation and timing are identical to a single FIFO, with the exception of an added gate delay on the flags.

Figure 10. Shift–In Operation In High–Speed Burst Mode



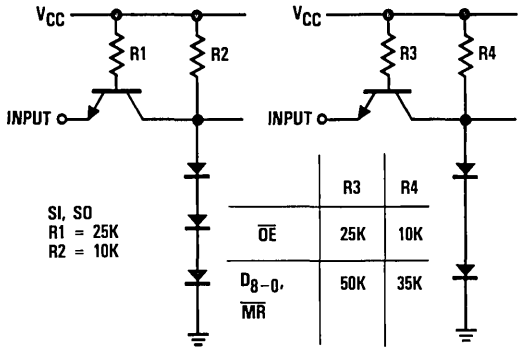
In the high–speed mode, the Burst–In rate is determined by the minimum Shift–In HIGH and Shift–In LOW specifications. The IR status flag is a "don't care" condition, and a Shift–In pulse can be applied without regard to the flag. A Shift–In pulse which would overflow the storage capacity of the FIFO is not permitted.

Figure 11. Shift-Out Operation In High-Speed Burst Mode



In the high-speed mode, the Burst-Out rate is determined by the minimum Shift-Out HIGH and Shift-Out LOW specifications. The OR flag is a "don't care" condition, and a Shift-Out pulse can be applied without regard to the flag.

Figure 12. Equivalent Input Circuit



	R3	R4
$\overline{OE}$	25K	10K
D_{8-0}, $\overline{MR}$	50K	35K

Figure 13. Equivalent Output Circuit

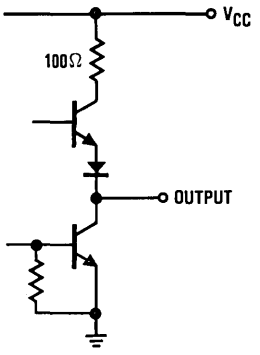


Figure 14. Test Load

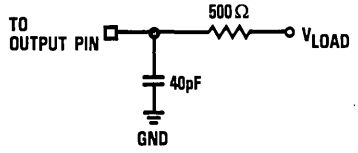
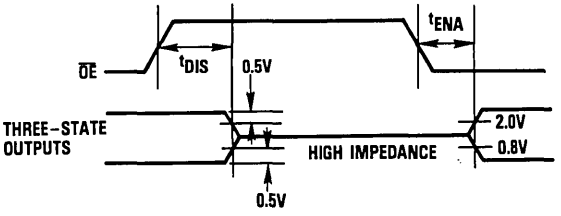


Figure 15. Transition Levels For Three-State Measurements



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Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−6.0 to +6.0mA
Output	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−1.0 to +6.0mA [3,4]
Short circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, case	−60 to +140°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{SIL}	Shift-In Pulse Width, LOW	20			20			ns
t_{SIH}	Shift-In Pulse Width, HIGH	15			18			ns
t_S	Input Setup Time	0			0			ns
t_H	Input Hold Time	25			30			ns
t_{SOL}	Shift-Out Pulse Width, LOW	20			20			ns
t_{SOH}	Shift-Out Pulse Width, HIGH	15			18			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = MAX, static[1]					
		T_A = 0°C to 70°C		350			mA
		T_A = 70°C		280			mA
		T_C = -55°C to 125°C				400	mA
		T_C = 125°C				260	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V					
		D_{8-0}, MR		-0.4		-0.4	mA
		SI, SO, $\overline{OE}$		-1.0		-1.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V		75		75	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	HIGH-Z Output, Leakage Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V		-40		-40	μA
I_{OZH}	HIGH-Z Output, Leakage Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V		40		40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, One pin to ground, one second duration, output HIGH.		-40		-40	mA
C_I	Input Capacitance	T_A = 25°C, F = 1.0MHz		15		15	pF
C_O	Output Capacitance	T_A = 25°C, F = 1.0MHz		15		15	pF

Note:

1. Worst case, all digital inputs and outputs LOW, OE HIGH.

TRW reserves the right to change products and specifications without notice. This information does not convey any license under patent rights of TRW Inc. or others.

Preliminary Information describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact TRW for current information.

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Switching characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_{SI}	Shift-In Clock Rate	V_{CC} = MIN	18		16		MHz
F_{BI}	Burst-In Clock Rate	V_{CC} = MIN	20		18		MHz
t_{IR}	Input Ready Delay	V_{CC} = MIN		40		50	ns
t_{FT}	Fallthrough Time	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V		1.6		1.8	μs
F_{SO}	Shift-Out Clock Rate	V_{CC} = MIN	15		13		MHz
F_{BO}	Burst-Out Clock Rate	V_{CC} = MIN	18		16		MHz
t_{OR}	Output Ready Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V		51		65	ns
t_{D}	Data Output Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V		50		65	ns
t_{HO}	Data Output Hold Time	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V	15		15		ns
t_{MRW}	Master Reset Pulse Width	V_{CC} = MIN	20		25		ns
t_{MRORL}	Master Reset to OR LOW	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V		60		80	ns
t_{MRIRH}	Master Reset to IR HIGH	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V		45		65	ns
t_{MRSI}	Master Reset to SI	V_{CC} = MIN	55		65		ns
t_{IP}	Input Ready Pulse	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V	40		45		ns
t_{OP}	Output Ready Pulse	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V	45		50		ns
t_{DOF}	Data To Output Flag Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V	1		1		ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 1.8V		35		45	ns
t_{DIS}	Three-State Output Disable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1}[2]		30		40	ns

Notes:

1. All transitions are measured at a 1.5 level except for t_{DIS} and t_{ENA}, which are shown in Figure 15.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1030J6C	STD-T_A = 0°C to 70°C	Commercial	28 Lead DIP	1030J6C
TDC1030J6G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	28 Lead DIP	1030J6G
TDC1030J6F	EXT-T_C = -55°C to 125°C	Commercial	28 Lead DIP	1030J6F
TDC1030J6A	EXT-T_C = -55°C to 125°C	High Reliability[2]	28 Lead DIP	1030J6A
TDC1030C3C	STD-T_A = 0°C to 70°C	Commercial	28 Contact Chip Carrier	1030C3C
TDC1030C3G[1]	STD-T_A = 0°C to 70°C	Commercial With Burn-In	28 Contact Chip Carrier	1030C3G
TDC1030C3F	EXT-T_C = -55°C to 125°C	Commercial	28 Contact Chip Carrier	1030C3F
TDC1030C3A	EXT-T_C = -55°C to 125°C	High Reliability[2]	28 Contact Chip Carrier	1030C3A
TDC1030B6C	STD-T_A = 0°C to 70°C	Commercial	28 Lead CERDIP	1030B6C
TDC1030B6G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	28 Lead CERDIP	1030B6G

Notes:

1. Contact factory for availability.
2. Per TRW document 70Z01757.

V L S I

D A T A

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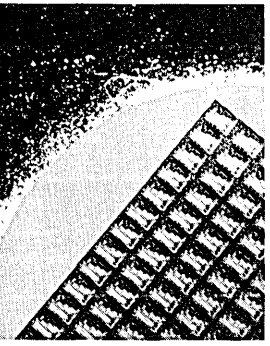

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The ability to produce integrated circuits to high reliability specifications cannot be learned overnight. It takes years to develop such capability with special attention given to manufacturing processes and circuit design techniques.

TRW has been in the forefront of the development and production of high reliability integrated circuits. Following the small-scale integration afforded by the first TTL gates, TRW moved to medium and large-scale integration.

TRW LSI Products' movement from SSI to VLSI has been centered around the use of a triple diffusion (3D) bipolar process. This process was developed by TRW in the early 1960s and has been consistently improved to give superior producibility, performance and reliability. Recently a bulk 1μ CMOS process has been developed and has demonstrated excellent reliability.

The 3D process meets the stringent requirements of MIL-M-38510 and MIL-STD-883, as well as those requirements of other high performance commercial and industrial applications. Development of the process was only one of the steps required to produce high reliability VLSI. Circuit design must also be directed toward the same goal. Reliability cannot be added at a later stage in the development process. It must be included in the initial design of each device.

Another aspect of reliability is the control of the assembly process, which is necessary to obtain the desired results. Here again, there is no substitute for experience. Each step in the TRW LSI assembly process is controlled within narrow limits to produce high-yield devices of proven reliability. Testing verifies that high reliability VLSI has been achieved. TRW performs unique, product-oriented accelerated life tests in addition to tests that are in accordance with MIL-M-38510 and MIL-STD-883.

Demonstrated VLSI Reliability

Reliability is expressed in terms of failure units, or FITs, which are defined as failures per 10^9 device-hours. VLSI devices from TRW LSI Products exhibit a failure rate many times better than that obtainable from SSI or MSI logic.

An example of the reliability possible from VLSI is evidenced by tests performed on the MPY016H multiplier. The MPY016H contains 14,000 components (transistors and resistors) configured into 888 Current Mode Logic (CML) gates. Eighteen of these devices were operated for 2,000 hours at 290°C junction temperature, and a median life of 8.0 x 10^6 hours at Tj=125°C was demonstrated. This corresponds to a mean time to failure (MTTF) of 3.39 x 10^7 hours or a failure rate of 29.5 FITs.

Accelerated life testing at elevated temperatures is used to reduce testing hours to a practical number. The theoretical basis for accelerated temperature testing is the Arrhenius equation that relates failure rate to temperature:

$$\frac{1}{t_f} = A \exp\left(\frac{-E_a}{kT}\right)$$

where: tf = time to failure

A = a constant

E_a = activation energy (approx. 1.02 eV)

k = Boltzmann's constant (8.61 x 10^{-5} ev/°K)

T = absolute temperature (°K=°C+273°)

A graphical solution of the Arrhenius equation can be performed. The first step in the evaluation of the test results is to plot the cumulative percent of failures vs. the hours to failure, as shown in Figure 1. Then, the best straight line fit for these points is drawn to represent the failure distribution. The intersection of this line with the 50% failure line is the median lifetime, t_m, which in this case is 1500 hours.

An activation energy of 1.02eV was used for the example in Figure 2. From this data point (a junction temperature of 290°C and median lifetime of 1500 hours), a median lifetime of 8 x 10^6 hours at 125°C is extrapolated. This corresponds to a mean time to failure (MTTF) of 3.39 x 10^7 hours, or a failure rate of 29.5 FITs.

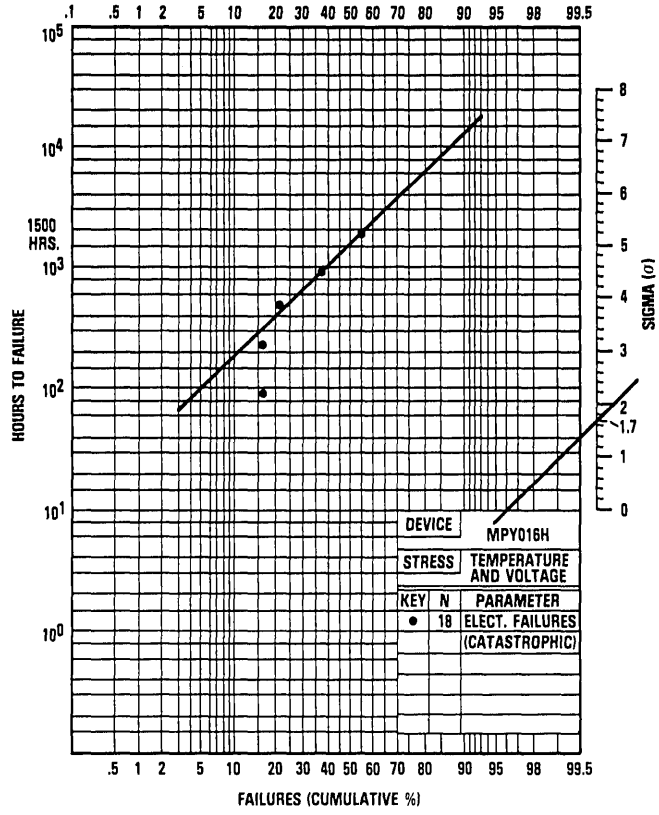

Figure 1. Median lifetime, t_m, is 1500 hours for 18 samples of the MPY016H multiplier operating at 290°C junction temperature.

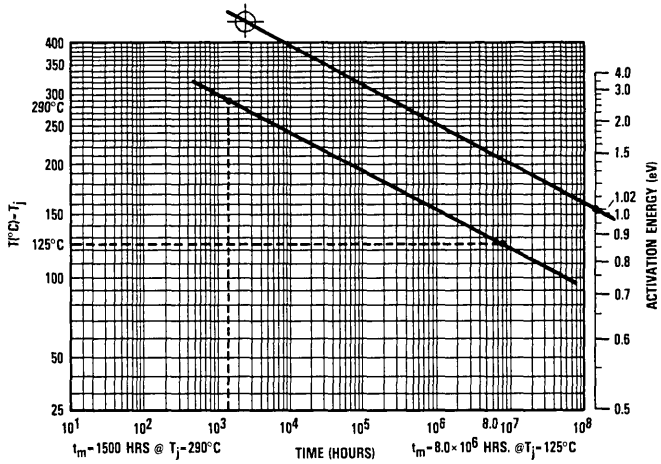

Figure 2. Median Lifetime is 8.0 x 10^6 hours for the MPY016H at 125°C, as determined by accelerated reliability testing at 290°C.

Inherent Radiation Hardness

Radiation Source	Radiation Level (Device Fully Functional)
Gamma Rays	10^6 rads (Si)
Neutrons	10^{14} n/cm^2
X-Ray (Upset)	2.9 x 10^8 rads/sec
X-Ray (Burnout)	1.3 x 10^{12} rads/sec

Table 1. Radiation Resistance Levels

As shown in Table 1, TRW's 3D bipolar process is inherently radiation resistant. High energy radiation excites and ionizes the semiconductor materials and displaces atoms from normal crystal sites, thus, it has a profound effect on device parameters. These effects result from damage induced by neutrons, X-rays, and gamma rays. The damage can change AC and DC parameters, affect functional performance, and in some cases even destroy the device. Often, these effects are temporary, lasting only microseconds, but in some cases they cause permanent damage.

The small geometries and 3D bipolar fabrication process make TRW LSI Products' VLSI devices inherently radiation-hard. This hardness is obtained by structural perfection and cleanliness of the silicon-silicon dioxide interface. As a result, these devices outperform many of the MOS and bipolar devices exposed to similar radiation environments. TRW's multipliers have been found fully functional after an absorbed dose of 10^6 rads (Si) from a gamma ray source.

Neutron damage also causes a change in device characteristics by reducing h_{fe}, the current gain of the transistor. The 3D transistors are inherently resistant to neutron damage because their narrow base region and low transmit time provide an f_t of about 300MHz for 2-micron geometries; thus, any small change in h_{fe} has little effect on performance. VLSI multipliers fabricated with the 3D process have survived a dose of 10^{14} n/cm^2 without functional failures.

Another source of potential radiation problems comes from X-rays, which can cause circuit upsets or burnouts. An upset can produce permanent effects in regenerative circuits by causing latch-up conditions or changes in logic states.

VLSI multipliers fabricated with 3D technology have experienced no functional failures or latch-ups when subjected to 2.9 x 10^8 rads/sec of X-ray upset. The high upset tolerance is again due to small geometries and fast recovery time constants inherent in the 3D process. The resistance to latch-up is also due to the low inverse betas of the NPN and PNP transistors.

The same VLSI multipliers that passed 2.9 x 10^8 rads/sec were tested for X-ray burnout with a dose of 1.3 x 10^{12} rads/sec. There were no functional failures, latch-ups or burnouts in the samples.

Reliability by Design

Fabrication

Matching the fabrication process to both semiconductor and circuit design, TRW LSI Products achieves optimum performance from VLSI. As a result, both high reliability and good yields are available.

An example of the reliability designed into our bipolar and CMOS processes is the use of a composite metallization system consisting of titanium and aluminum. This technique virtually eliminates electromigration, which causes voids or hillocks in metallization. Elimination of electromigration is achieved because titanium reduces residual silicon dioxide in the contact windows, providing improved ohmic contact and excellent mechanical adhesion.

Accurate Masks Lead to Reliable Devices
The final physical layout of the chip is stored on magnetic tape and applied to a pattern generator which automatically draws the device on a glass reticle. Manual steps are eliminated, thus ensuring accurate masks for device production. The first output from the pattern generator is a glass reticle containing the layout of a single chip that is several times actual size.

The reticle is accurately aligned and the image is reproduced repeatedly to produce the master mask. This mask is less susceptible to plate defects (small pinholes in chrome) than an actual size mask. Projection printing and wafer stepper aligners are used in the wafer fabrication process. In contrast with contact printing, projection masks have a longer useful lifetime because they encounter essentially no physical wear. On the other hand, most contact masks must be discarded after one hundred (or less) operations. Projection masks also provide better results than contact masks because minor defects are less likely to occur.

Controlling Production to Assure Reliability
Once the design is completed, fabrication of the VLSI die can begin. This involves tightly-controlled steps with appropriate levels of inspection, testing and screening.

The fabrication process begins with a silicon wafer. Before any work is done on the wafer, it is inspected for visible surface defects.

Next, the wafer's thickness, flatness and resistivity are measured. A thin wafer can be excessively brittle, whereas a thick wafer is more difficult to cut into individual dice. Flatness is important in obtaining an accurate projection of the artwork contained on the production masks. Resistivity affects the electrical parameters of the semiconductor devices on the wafer.

After a blank wafer passes inspection, it is processed through many steps. These include diffusion, ion implantation, etching, coating with photoresist, metallization, etc. The masks are aligned within very tight tolerances to ensure proper registration between elements on each die. To protect the finished surface of the wafer against contaminants, silicon dioxide or nitride (glass passivation) is deposited over the entire wafer. Gold is then evaporated onto the back of the wafer to provide a good electrical contact to the substrate. The gold-silicon back contact not only provides good electrical contact to the substrate ground, it also simplifies later attachment of the VLSI die to its package and enhances thermal conduction.

The next step involves computer-controlled testing of each die on the wafer. Known as "die probe," this is an electrical function check for correct operation. If a die is found to be non-functional, a drop of ink is automatically placed on it so it can be discarded after die separation.

Figure 3 traces the path of each wafer as it passes through the assembly process that ends with a completely packaged device. Note that each production step has an inspection, screening or test function associated with it.

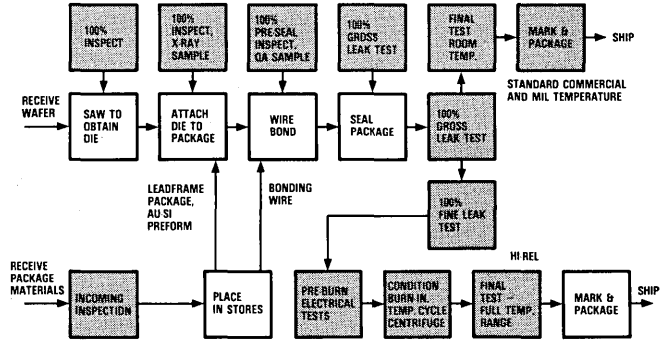

Figure 3. Inspection, screening or testing (shown in gray) accompanies each assembly step to ensure the reliability of the finished device.

Controlled Assembly Steps
The first step in the assembly process is die separation. This is accomplished with an automated diamond saw that slices the wafer. The saw technique produces a smoother edge and results in higher yields than other die separation methods.

Now the dice are ready to be mounted within the device package. Each die is accurately positioned within the package and a gold-silicon solder preform is placed between the bottom of the die and the package. The combination is heated within very close temperature tolerances, attaching the die to the package.

One of the checks on the die-attach step is temperature calibration of the heating equipment, which is done every four hours. Another check is die shear testing of samples of attached die from each production lot, and is done to detect voids between the die and the package.

After the die is attached to the package, 1.25mil wires are bonded from pads on the die to package pads that connect to the external pins of the device. To ensure reliable bonds, each bonding machine is monitored every four hours.

To check the wire bonds, device samples are removed from each production lot and subjected to a wire-bond pull test. This is accomplished by specialized equipment that pulls bonding wires until they separate from the die. Control charts are maintained to provide trend analysis.

Inspection Enhances Product Quality
After wire bonding, the device goes through a pre-seal microscopic inspection to ensure that it is internally correct and that the workmanship meets all requirements. After passing this inspection, the package is sealed. In sealing, the package moves through a special furnace where a lid is attached to the package.

The sealed package is then gross-leak tested to verify a good hermetic seal. Commercial parts receive complete electrical testing at 25°C and then are marked and packaged.

For high reliability parts, military or customer-specified screens and other tests are performed. These are followed by complete electrical testing over the recommended operating temperature range. Next, the devices are appropriately marked and packaged. Then data are reviewed for acceptability and if requested, a certificate of conformance is generated.

Electrical testing of devices is performed on automated VLSI testers that are programmed to provide unique signal patterns for each of the VLSI circuits. A full-time programming staff is responsible for the maintenance of all test programs.

Mil Spec Testing
TRW LSI Products' high reliability devices are all produced in accordance with customer or military specifications and standards, notably MIL-STD-883, "Test Methods and Procedures for Microelectronics," and MIL-M-38510, "General Specifications for Microcircuits."

These military documents categorize microcircuits into two product assurance classes related to the reliability requirements of the application. Class S requirements are the most stringent because they cover critical applications and Class B requirements are intended for less critical applications and are the most widely used.

MIL-STD-883 contains test methods and procedures for various electrical, mechanical and environmental tests as well as requirements for screening, qualification and quality conformance inspection. Table 2, taken from Method 5004 of MIL-STD-883, lists the 100% screening tests required for these three devices. TRW LSI Products typically screens high reliability devices to the Class B requirements.

Following device screening, samples are removed from the lot(s) as part of our ongoing Quality Conformance Inspection (QCI) program. This testing is divided into four inspection groups: A, B, C, and D.

Group A electrical inspection involves dynamic, static, functional and switching tests at maximum, minimum and ambient operating temperatures. Sample sizes and specified tests depend on the product assurance class.

Assurance of the absence of lot-to-lot fabrication related errors is covered by Group B inspection, which includes tests for marking permanency, internal visual and mechanical correctness, bond strength, and solderability.

For the remaining two inspection groups, Group C is oriented toward die integrity and Group D covers package integrity. Among the Group C tests are steady state life, temperature cycling and constant acceleration. Group D includes lead integrity, hermeticity, and thermal and mechanical shock.

The combination of these 100% and sample tests assures that all TRW LSI Products are capable of meeting their specified requirements, and that reliability will meet or exceed customer requirements.

TRW LSI Products has received facilities certification from the Defense Electronics Supply Center of the Department of Defense. This certification is the first step in obtaining MIL-M-38510 QPL (JAN) approval for LSI Products devices (which is expected during 1985) and demonstrates TRW's commitment and capability to perform accurate testing.

Screen	Class S Method	Requirement	Class B Method	Requirement
1. Wafer lot acceptance	5007	All lots		–
2. Nondestructive bond pull	2023	100%		
3. Internal Visual	2010, condition A	100%	2010, condition B	100%
4. Stabilization bake (no end point measurement required)	1008, condition C (min.), 24 hrs. min.	100%	1008, condition C (min.), 24 hrs. min.	100%
5. Temperature cycling	1010, condition C	100%	1010, condition C	100%
6. Constant acceleration	2001, condition C (min.) Y1 orientation only	100%	2001, condition E (min.) Y1 orientation only	100%
7. Visual inspection		100%		100%
8. Seal a) Fine b) Gross	1014	100%	1014	100%
9. Particle impact noise detection (PIND)	2020, condition A or B	100%		
10. Interim (pre-burn-in) electrical parameters	Per applicable device specification	100%	Per applicable device specification	
11. Burn-in test	1015-240 hrs. @ 125°C min.	100%	1015-160 hrs. @ 125°C min.	100%
12. Interim (post-burn-in) electrical parameters	Per applicable device specification	100%		
13. Reverse bias burn-in	1015, condition A or C 72 hrs. @ 150°C min.	100%		
14. Interim (post-burn-in) electrical parameters	Per applicable device specification (Read and Record)	100%	Per applicable device specification	100%
15. Percent defective allowable calculation	5% over subgroup 1 3% functional parameters @ 25°C	All lots	5% over subgroup 1 @ 25°C	All lots
16. Seal 12 a) Fine b) Gross	1014	100%		
17. Final electrical test a) Static tests 1) 25°C (subgroup 1, Table 1, 5005) 2) Maximum & minimum rated operating temp (subgroups 2, 3, Table 1, 5005) b) Dynamic tests and switching test 25°C (subgroups 4, 9, Table 1, 5005) c) Functional tests 25°C (subgroup 7, Table 1, 5005)	Per applicable device specification	 100% 100% 100% 100%	Per applicable device specification	 100% 100% 100% 100%
18. Radiographic	2012 two views	100%		–
19. Qualification or quality conformance inspection test sample selection		Sample 1	Sample	Sample 1
20. External visual	2009	100%		100%

Table 2. 100% Screening Tests (Method 5004)

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V L S I

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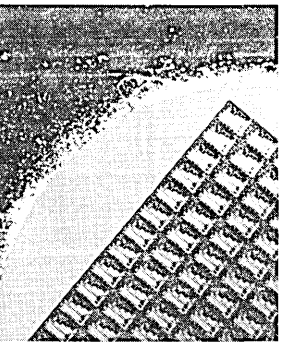

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Package Information

At TRW LSI Products, packaging is designed to meet the thermal, mechanical, and electrical needs of the circuit and the customer. TRW LSI Products offers a wide range of package designs to accommodate these requirements. The High Rel user has the option of 16-64 lead fully gold plated DIPs, flat packs and chip carriers.

Two types of chip carriers are included within this wide variety of packages: contact (also known as terminal or leadless) chip carriers, and leaded chip carriers. TRW chip carriers and their equivalent DIP configurations are indicated below:

Chip Carrier I/O	Equivalent DIP Package I/O
68 Contact or Leaded Chip Carrier	48 Lead, 64 Lead Top Brazed DIP (also 64 Leaded Flatpack)
44 Contact Chip Carrier	40 Lead DIP
28 Contact Chip Carrier	24 or 28 Lead DIP
20 Contact Chip Carrier	16 or 18 Lead DIP

Contact chip carriers conform to the JEDEC type C outline with 0.050 inch contact spacing located on plane 1 (heat dissipating side only). The body construction consists of multilayer ceramic with a metallized seal ring for gold solder lid seal. Contact chip carriers are used for mother board leaded conversions of ceramic/compliant PCB attachments by means of surface solder mounting techniques.

Leaded chip carriers are available in the 68 I/O configuration. The body is constructed identically to the 68 Contact Chip Carrier, however the contacts are located on plane 2 (side opposite the heat dissipating side). Gold plated "Kovar" leads, (0.018 inch wide x 0.006-0.010 inch thick x 0.400 inch long nominal) brazed to the contacts complete the package. This type of chip carrier is used for surface and through hole PCB attachments, and when external heat sinks are required.

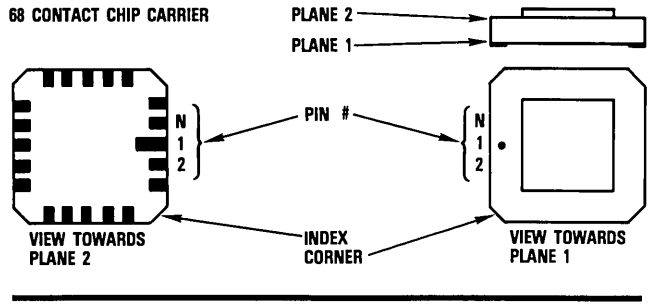
There are three major advantages to using chip carriers over standard DIP packages. First and foremost is the economy of chip carrier size (see the chart below for approximate area differences in square inches).

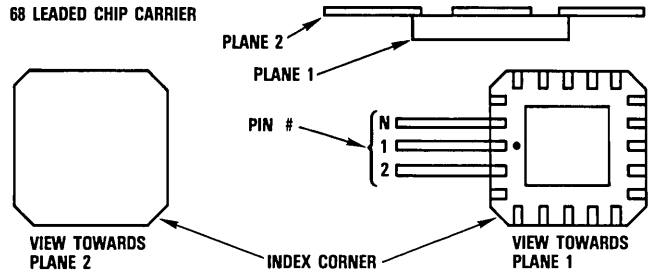
I/O Count	Chip Carrier Area[1]	DIP Area[1]	Ratio: CC to DIP
68	0.903	2.560	0.353
44	0.432	1.200	0.353
28	0.203	0.840	0.242
20	0.123	0.270	0.456

1. Square Inches

Secondly, chip carriers offer a reasonable size package for present and future high pin count circuits. For example, a 68 Contact Chip Carrier is only .965 inches per side and occupies a 0.93 square inch area, which is approximately the equivalent of a 48 Lead DIP (1.440 square inches). When considering the difficulties of handling and inserting a 48 Lead DIP into a PCB, the impracticality of a 68 Lead DIP (3.4 inches x 1.2 inches, if available) is evident. The third advantage is that chip carriers optimize electrical and thermal characteristics. Shorter leads of approximately equal length reduce lead resistance, inductance and capacitance. The longest trace on a 64 Lead DIP is almost eight times that of the longest trace on a 68 Contact Chip Carrier. In addition, the thermal impedance characteristics of the chip carrier are approximately equal to those of a DIP. The leaded chip carrier also provides the external heat sink option, allowing the heat generated by the device to be dissipated through the PCB or to the surrounding environment.

L





Chip carriers can typically reduce board space requirements as much as three to one over dual-in-line packages.

Cerdip packages provide similar mechanical, and identical electrical configurations as the dual-in-line packages without the full gold solder seal and lead finish, making them more economical. The body construction consists of two single layer ceramic pieces that "sandwich" an aluminized Kovar lead frame. The leads are matte tin finished for easy solderability.

Thermal considerations are important aspects of package design. Much computer modeling of die/package relationships is required to ensure the integrity of the products over all temperature ranges. A list of thermal resistivity (Θjc), which is material and geometry dependent, is listed for all products in Table 1. This list reflects the relationship of the die and the package only. Θja, a relationship between die, package and outside environment, is dependent on the particular application.

Product/ Package	Maximum Calculated Θjc
MPY008HJ5	9.557°C/W
MPY008HC2	7.183
MPY08HUJ5	9.557
MPY012HJ1, C1, L1	5.877
MPY012HF1	3.631
MPY016HJ1, C1	7.908
MPY016HF1	4.956
MPY016KJ1	6.753
MPY112KJ4	10.438
TDC1001/1002J8	22.869
TDC1004J9	9.908
TDC1005J9	12.544
TDC1006J9	11.075
TDC1007J1, C1	3.671
TDC1008J4, C1	7.908
TDC1009J1, C1	5.428
TDC1010J1, C1	3.382
TDC1011J7	15.297
TDC1011B7	19.996

Table 1 Continues on following page.

Product/ Package	Maximum Calculated Θjc
TDC1014J7	9.804
TDC1014C3	6.335
TDC1014B7	13.130
TDC1016J7	13.985
TDC1016J5	13.985
TDC1016C2	10.781
TDC1016B7	18.139
TDC1018J7	20.140
TDC1018B7	25.240
TDC1018C3	11.897
TDC1019C1, L1, J1	3.404
TDC1021J9	23.884
TDC1022J1	5.178
TDC1023J7	5.906
TDC1025C1, L1	7.814
TDC1027J7	8.411
TDC1027B7	11.411
TDC1028J4	5.142
TDC1029J7	18.548
TDC1030J6	10.740
TDC1030C3	6.952
TDC1030B6	14.289
TDC1043J3	11.364
TDC1048J6	7.752
TDC1048C3	5.008
TDC1048B6	10.566

Table 1

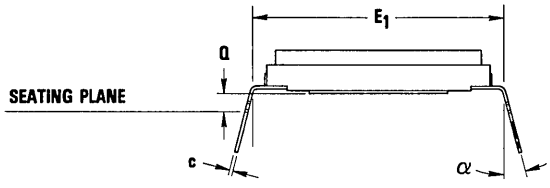
The following codes, one of which is stamped on the back of each TRW LSI device, identify the "country of origin" in which the device was manufactured.

Code	Country of Origin
K	Korea
HK	Hong Kong, BCC
P	Philippines
CP	San Diego, CA, U.S.A.
U.S.A.	U.S.A. (used for JAN products only)
SJ	San Jose, CA, U.S.A.
ES	El Segundo, CA, U.S.A.

L

J1 Package

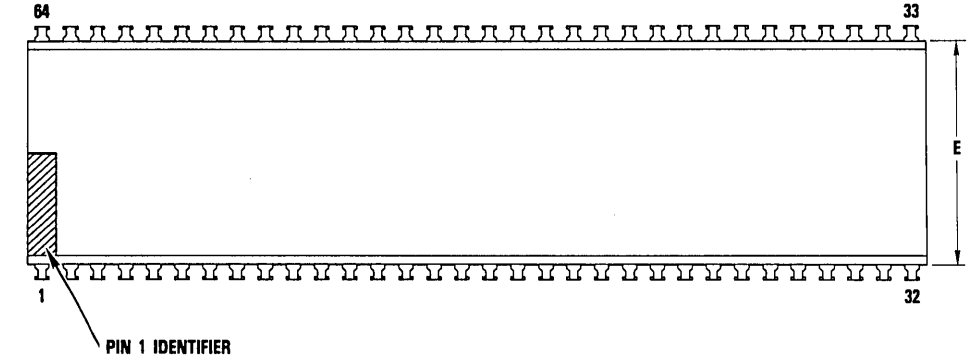
64 Lead Hermetic Ceramic DIP

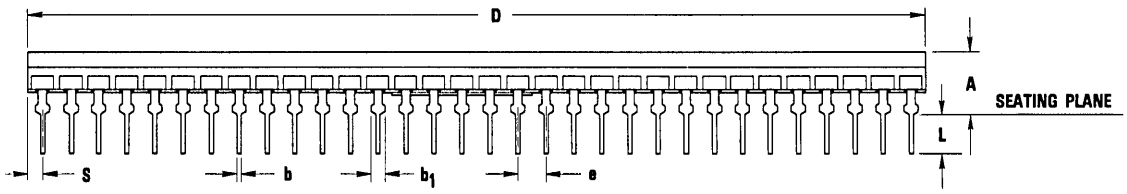


Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Nom ± Tol.
A	.206 (5.23)	.267 (6.78)	
b	.015 (0.38)	.019 (0.48)	
b_1	.045 (1.14)	.055 (1.40)	
c	.009 (0.23)	.012 (0.30)	
D			3.200 ± .030 (81.28 ± 0.76)
E			.800 ± .010 (20.32 ± 0.25)
E_1			.900 ± .010 (22.86 ± 0.25)
e			.100 ± .005 (2.54 ± 0.13)
L	.125 (3.18)	.160 (4.06)	
Q	.070 (1.78)	.085 (2.16)	
S	.030 (0.76)	.070 (1.78)	
α	0°	15°	

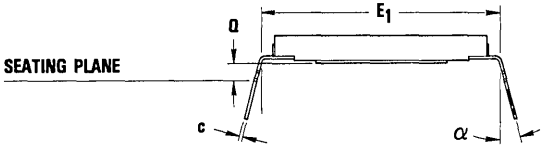
Ref. 90X00181





J3 Package

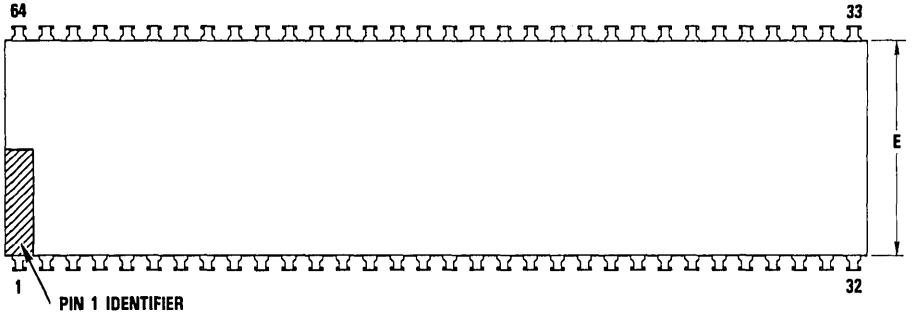
64 Lead Hermetic Ceramic DIP

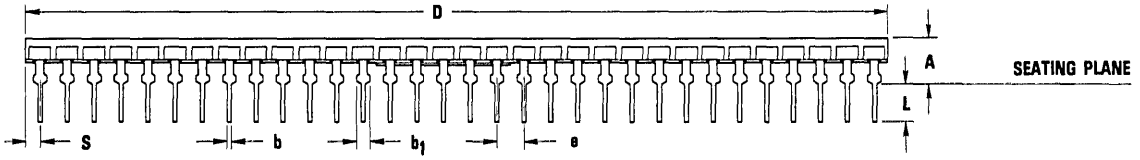


Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Nom ± Tol.
A	.153 (3.89)	.186 (4.72)	
b	.015 (0.38)	.019 (0.48)	
b_1	.045 (1.14)	.055 (1.40)	
c	.009 (0.23)	.012 (0.30)	
D			3.200 ± .030 (81.28 ± 0.76)
E			.800 ± .010 (20.32 ± 0.25)
E_1			.900 ± .010 (22.86 ± 0.25)
e			.100 ± .005 (2.54 ± 0.13)
L	.125 (3.18)	.160 (4.06)	
Q	.070 (1.78)	.085 (2.16)	
S	.030 (0.76)	.070 (1.78)	
α	0°	15°	

Ref. 90X00181





L

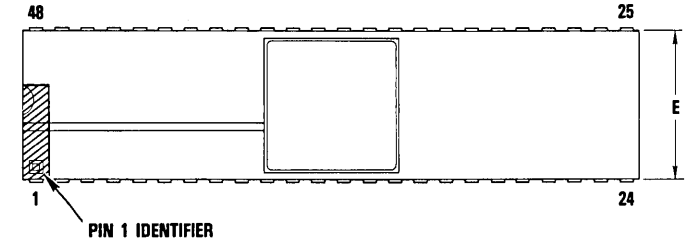
J4 Package

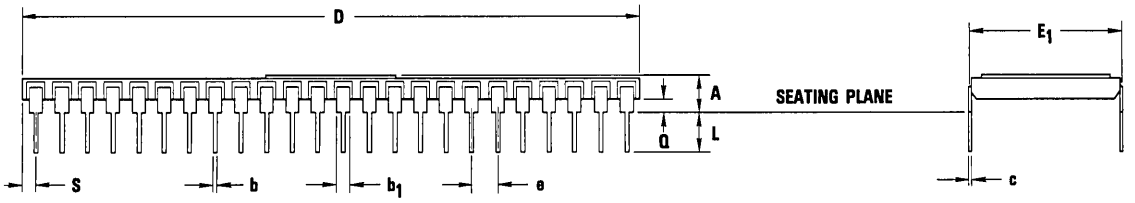
48 Lead Hermetic Ceramic DIP

Dimensions

Sym	Inches (Millimeters) Min	Max	Nom ± Tol.
A	.126 (3.20)	.166 (4.22)	
b	.016 (0.41)	.020 (0.51)	
b_1	.045 (1.14)	.055 (1.40)	
c	.009 (0.23)	.012 (0.30)	
D			2.400 ± .024 (60.96 ± 0.61)
E			.595 ± .010 (15.11 ± 0.25)
E_1			.600 ± .010 (15.24 ± 0.25)
e			.100 ± .005 (2.54 ± 0.13)
L	.125 (3.18)	.175 (4.45)	
Q	.040 (1.02)	.060 (1.52)	
S	.043 (1.09)	.057 (1.45)	

Ref. 90X00181



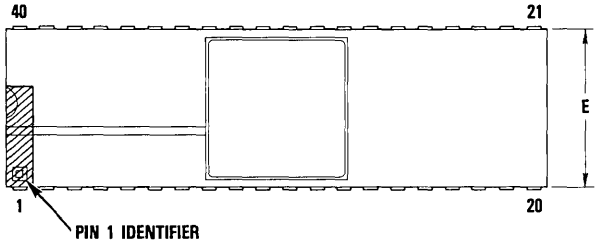


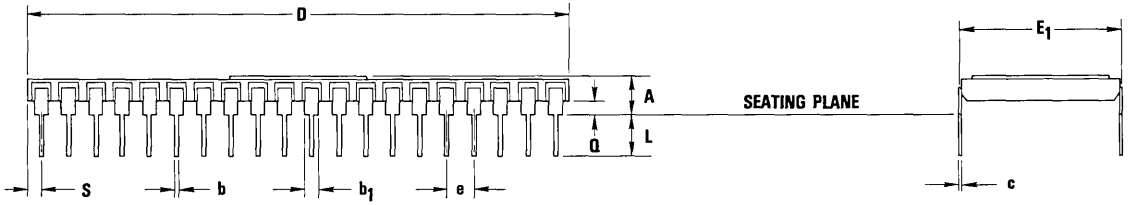
J5 Package
40 Lead Hermetic Ceramic DIP

Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Nom ± Tol.
A	.126 (3.20)	.166 (4.22)	
b	.016 (0.41)	.020 (0.51)	
b_1	.035 (0.89)	.045 (1.14)	
c	.009 (0.23)	.012 (0.30)	
D			2.000 ± .020 (50.80 ± 0.51)
E			.590 ± .010 (14.99 ± 0.25)
E_1			.600 ± .010 (15.24 ± 0.25)
e			.100 ± .005 (2.54 ± 0.13)
L	.125 (3.18)	.175 (4.45)	
Q	.040 (1.02)	.060 (1.52)	
S	.043 (1.09)	.059 (1.50)	

Ref. 90X00181

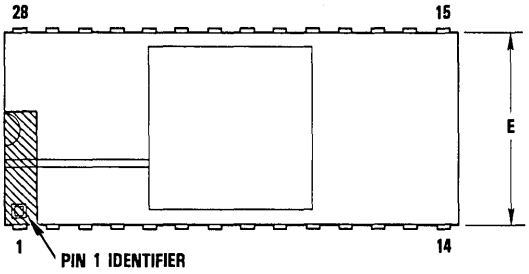




L

J6 Package

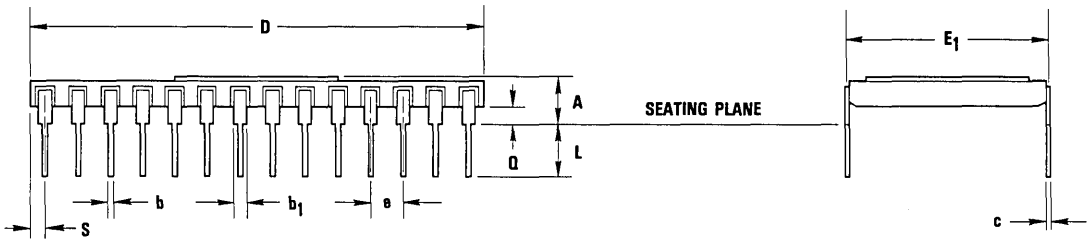
28 Lead Hermetic Ceramic DIP



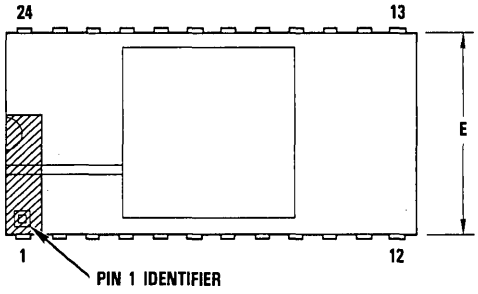
Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Nom ± Tol.
A	.126 (3.20)	.166 (4.22)	
b	.016 (0.41)	.020 (0.51)	
b_1	.045 (1.14)	.055 (1.40)	
c	.009 (0.23)	.012 (0.30)	
D			1.400 ± .014 (35.56 ± 0.36)
E			.590 ± .010 (14.99 ± 0.25)
E_1			.600 ± .010 (15.24 ± 0.25)
e			.100 ± .005 (2.54 ± 0.13) O.C.
L	.125 (3.18)	.175 (4.45)	
Q	.040 (1.02)	.060 (1.52)	
S	.043 (1.09)	.059 (1.50)	

Ref. 90X00181



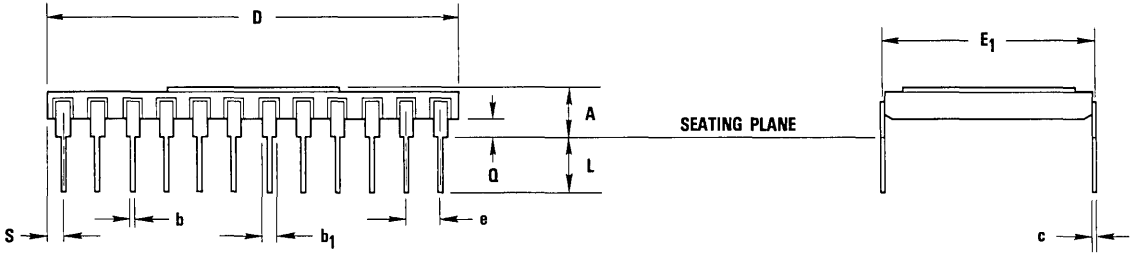
J7 Package
24 Lead Hermetic Ceramic DIP



Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Nom ± Tol.
A	.126 (3.20)	.166 (4.22)	
b	.016 (0.41)	.020 (0.51)	
b_1	.035 (0.89)	.045 (1.14)	
c	.009 (0.23)	.012 (0.30)	
D			1.200±.012 (30.48±0.30)
E			.590±.010 (14.99±0.25)
E_1			.600±.010 (15.24±0.25)
e			.100±.005 (2.54±0.13) O.C.
L	.125 (3.18)	.175 (4.45)	
Q	.040 (1.02)	.060 (1.52)	
S	.043 (1.09)	.057 (1.45)	

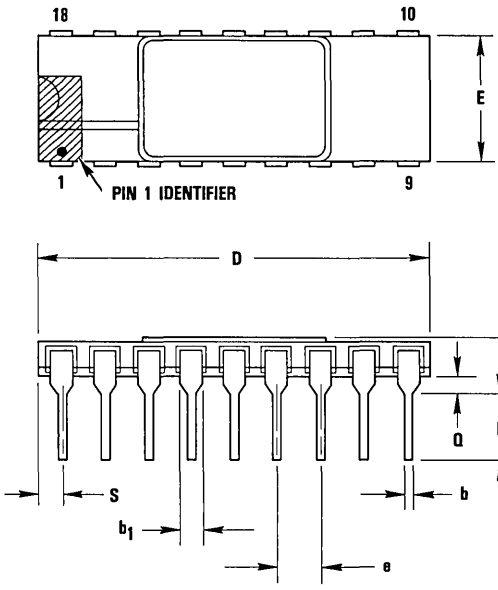
Ref. 90X00181



L

J8 Package

18 Lead Hermetic Ceramic DIP



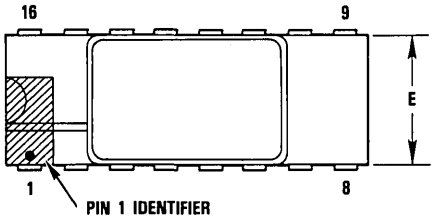
Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Nom ± Tol.
A	.110 (2.79)	.150 (3.81)	
b	.016 (0.41)	.020 (0.51)	
b_1	.049 (1.24)	.059 (1.50)	
c	.009 (0.23)	.012 (0.30)	
D			.900 ± .010 (22.86 ± 0.25)
E			.295 ± .008 (7.49 ± 0.20)
E_1			.300 ± .010 (7.62 ± 0.25)
e			.100 ± .005 (2.54 ± 0.13)
L	.125 (3.18)	.170 (4.32)	
Q	.025 (0.64)	.045 (1.14)	
S	.043 (1.09)	.057 (1.45)	

Ref. 90X00181

J9 Package

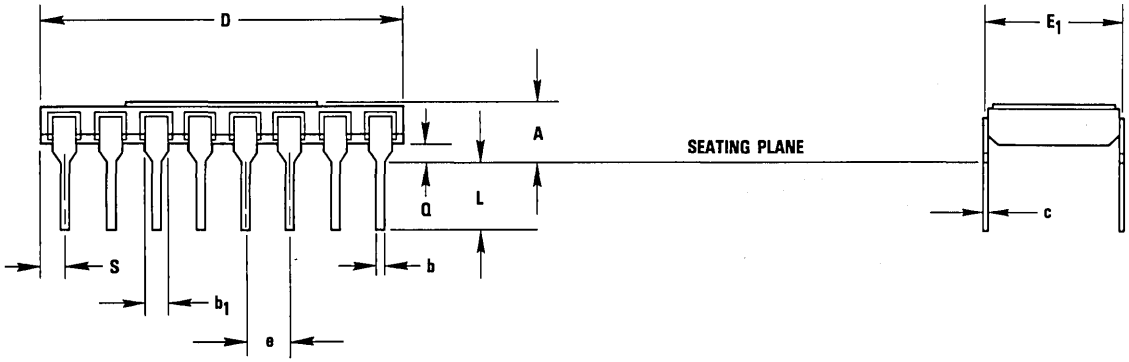
16 Lead Hermetic Ceramic DIP



Dimensions

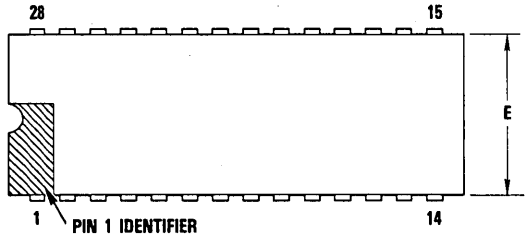
	Inches (Millimeters)		
Sym	Min	Max	Nom ± Tol.
A	.110 (2.79)	.150 (3.81)	
b	.016 (0.41)	.020 (0.51)	
b_1	.049 (1.24)	.059 (1.50)	
c	.009 (0.23)	.012 (0.30)	
D	.792 (20.12)	.808 (20.52)	
E			.295 ± .008 (7.50 ± .205)
E_1			.300 ± .010 (7.62 ± 0.25)
e			.100 ± .005 (2.54 ± 0.13)
L	.125 (3.18)	.170 (4.32)	
Q	.025 (0.64)	.045 (1.14)	
S	.043 (1.09)	.057 (1.45)	

Ref. 90X00181



L

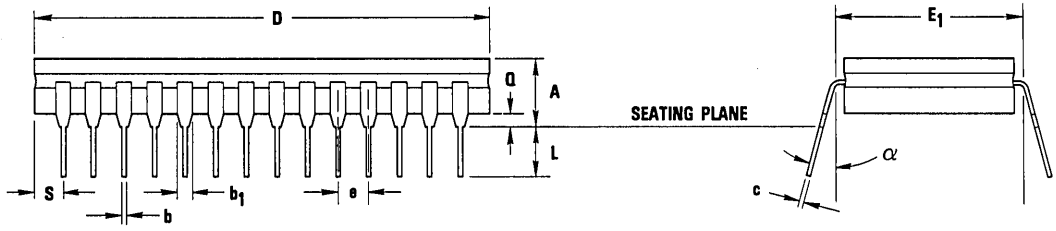
B6 Package
28 Lead CERDIP



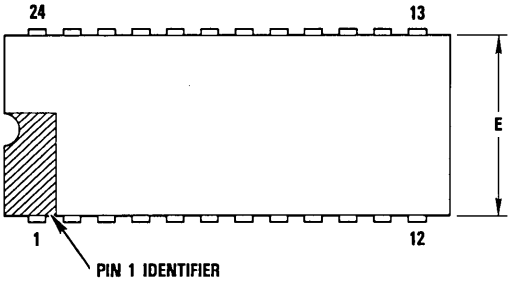
Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Nom±Tol.
A		.255 (5.72)	
b	.014 (0.36)	.023 (0.58)	
b_1	.030 (0.76)	.070 (1.78)	
c	.008 (0.30)	.015 (0.38)	
D			1.465 ± .025 (37.21 ± 0.64)
E	.510 (12.95)	.590 (14.99)	
E_1			.600 ± .010 (15.24 ± 0.25)
e			.100 ± .005 (2.54 ± 0.13)
L	.125 (3.18)	.200 (5.08)	
Q	.015 (0.38)	.075 (1.91)	
S		.098 (2.49)	
α	0°	15°	

Ref. 90X00181



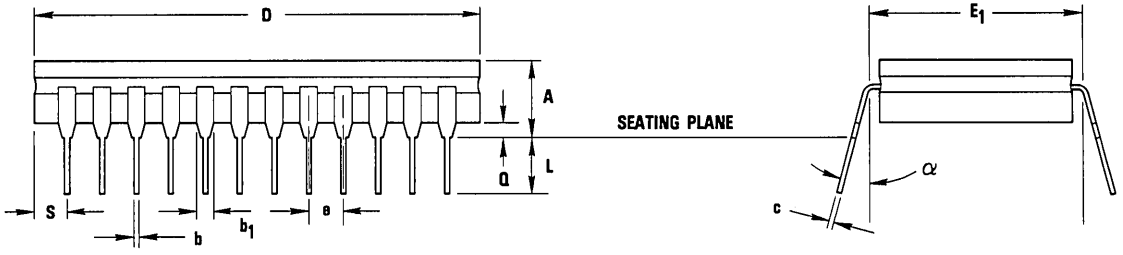
B7 Package
24 Lead CERDIP



Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Nom ± Tol.
A		.225 (5.72)	
b	.014 (0.36)	.023 (0.58)	
b_1	.030 (0.76)	.070 (1.78)	
c	.008 (0.20)	.015 (0.38)	
D			1.267 ± .023 (32.18 ± 0.58)
E	.510 (12.95)	.610 (15.49)	
E_1			.605 ± .015 (15.37 ± 0.38)
e			.100 ± .005 (2.54 ± 0.13)
L	.125 (3.18)	.200 (5.08)	
Q	.015 (0.38)	.075 (1.91)	
S		.098 (2.49)	
α	0°	15°	

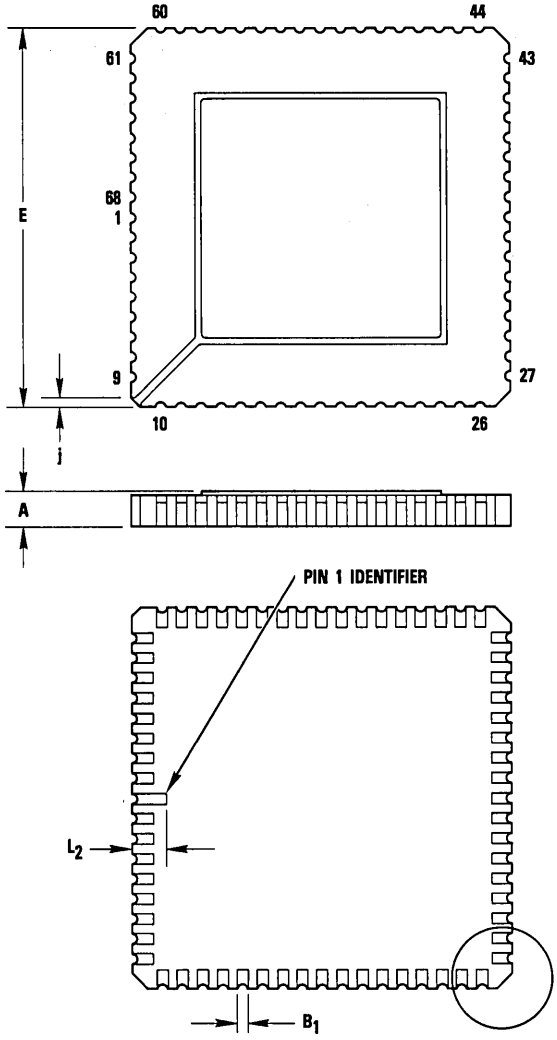
Ref. 90X00181

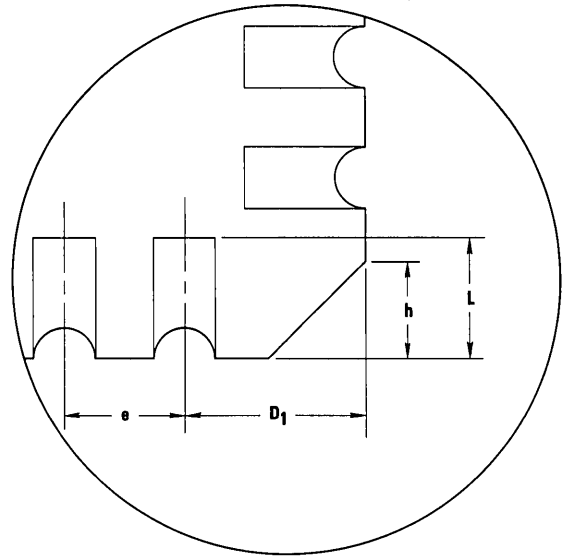


L

C1 Package

68 Contact Hermetic Ceramic Chip Carrier





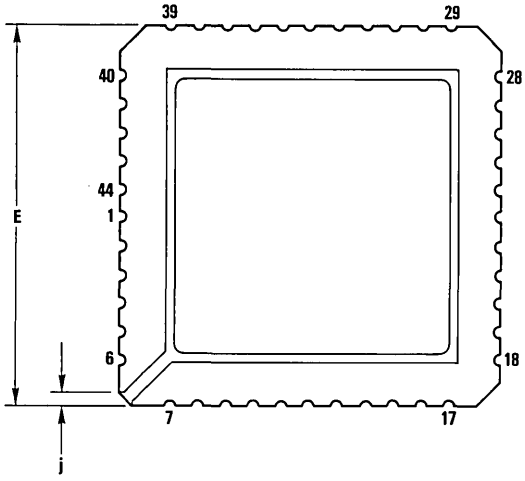
Dimensions

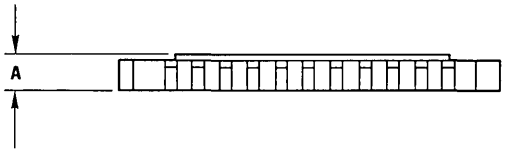
	Inches (Millimeters)		
Sym	Min	Max	Nom ± Tol.
A	.082 (2.08)	.100 (2.54)	
B_1	.020 (0.51)	.030 (0.76)	
D_1	.070 (1.78)	.080 (2.03)	
E			.9525 ± .0125 (24.19 ± .3175) sq.
e			.050 ± .005 (1.27 ± 0.13) O.C.
h			.040 ± .005 (1.02 ± 0.13) 3 PLCS
j			.020 ± .005 (0.51 ± 0.13) 3 PLCS
L	.042 (1.07)	.058 (1.47)	
L_2	.080 (2.03)	.090 (2.29)	

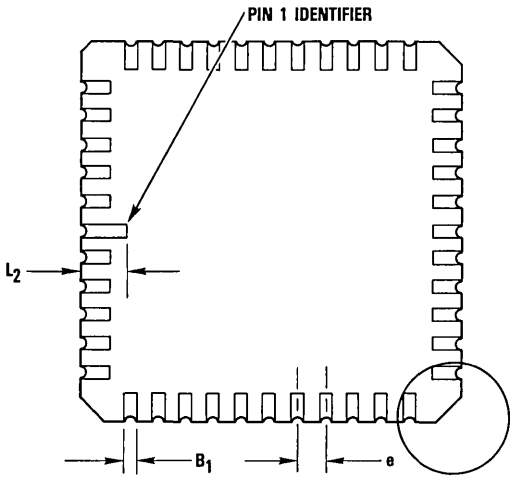
Ref. 90X00181

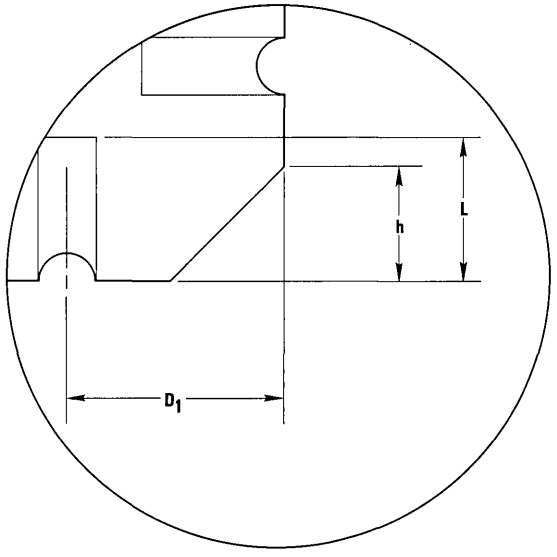
C2 Package

44 Contact Hermetic Ceramic Chip Carrier









Dimensions

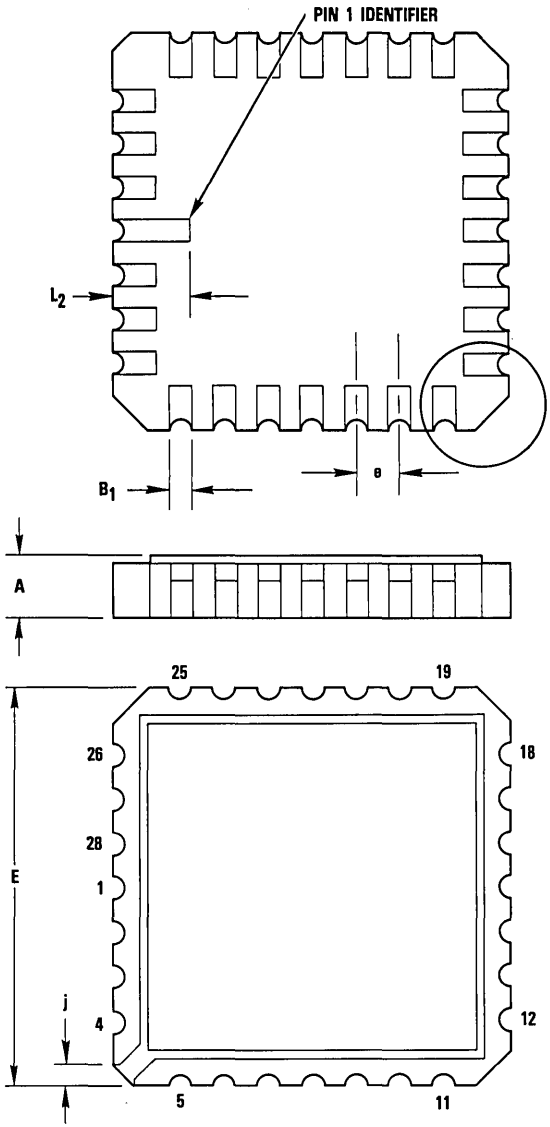
	Inches (Millimeters)		
Sym	Min	Max	Nom ± Tol.
A	.068 (1.73)	.084 (2.13)	
B_1	.020 (0.51)	.030 (0.76)	
D_1	.070 (1.78)	.080 (2.03)	
E			.652 ± .010 (16.56 ± 0.25) sq.
e			.050 ± .005 (1.27 ± 0.13) O.C.
h			.040 ± .005 (1.02 ± 0.13) 3 PLCS
j			.020 ± .005 (0.51 ± 0.13) 3 PLCS
L	.042 (1.07)	.058 (1.47)	
L_2	.080 (2.03)	.090 (2.29)	

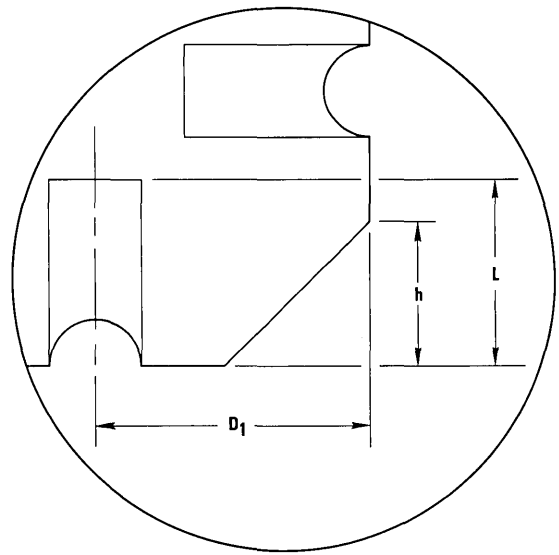
Ref. 90X00181

L

C3 Package

28 Contact Hermetic Ceramic Chip Carrier





Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Nom ± Tol.
A	.064 (1.63)	.078 (1.98)	
B_1	.020 (0.51)	.030 (0.76)	
D_1	.070 (1.78)	.080 (2.03)	
E			.450 ± .008 (11.43 ± .020) sq.
e			.050 ± .005 (1.27 ± 0.13) O.C.
h			.040 ± .005 (1.02 ± 0.13) x 45°, 3 PLCS
j			.020 ± .005 (0.51 ± 0.13) x 45°, 3 PLCS
L	.045 (1.14)	.055 (1.40)	
L_2	.080 (2.03)	.090 (2.29)	

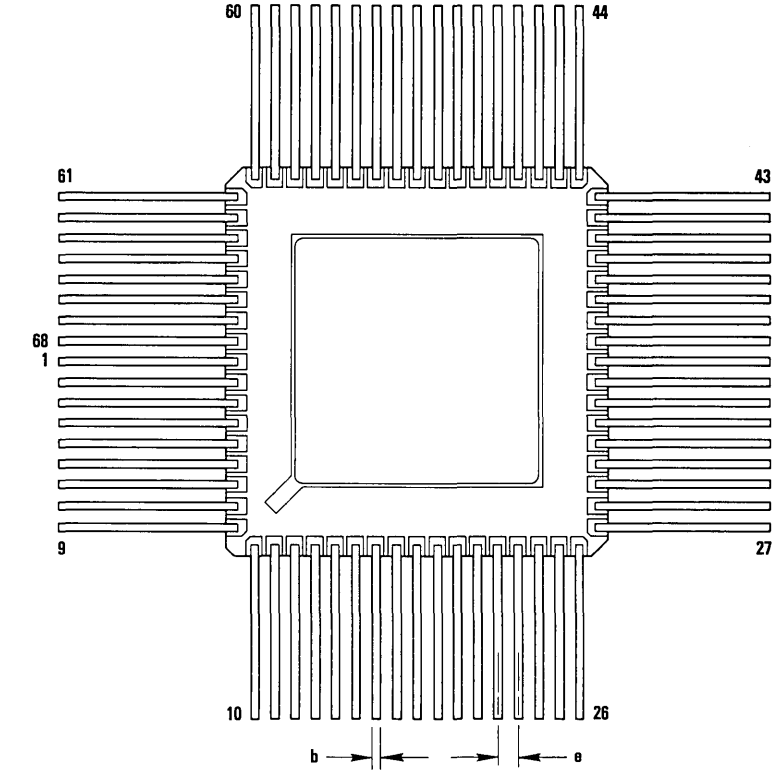
Ref: 90X00181

L1 Package
68 Leaded Hermetic Ceramic Chip Carrier

Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Nom ± Tol.
A	.082 (2.08)	.100 (2.54)	
b	.016 (0.41)	.020 (0.51)	
c	.008 (0.20)	.012 (0.30)	
E			.9525 ± .0125 (24.19 ± .3175) sq.
e			.050 ± .005 (1.27 ± 0.13) O.C.
L	.350 (8.89)	.400 (10.16)	

Ref. 90X00181



L

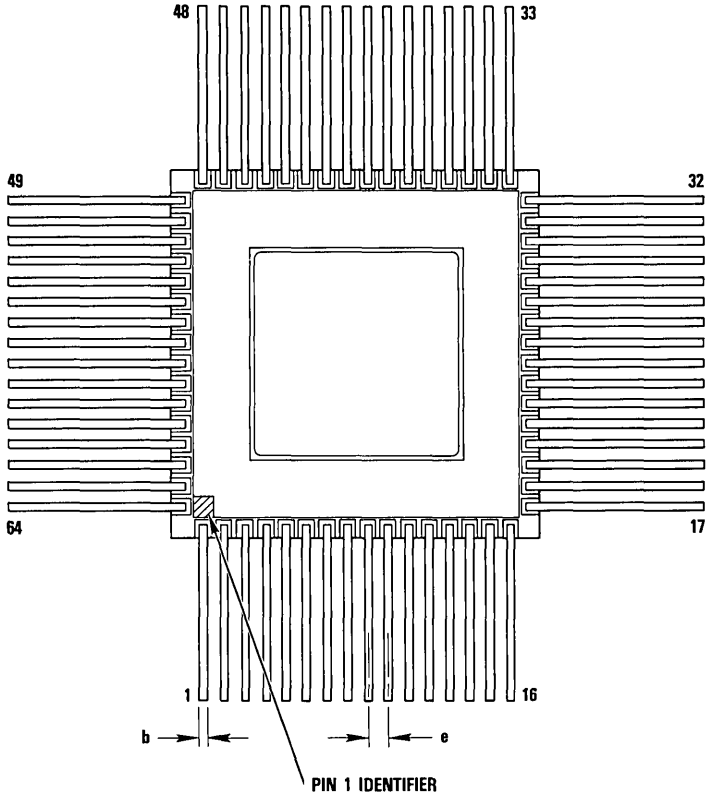
F1 Package

64 Leaded Hermetic Ceramic Flatpack

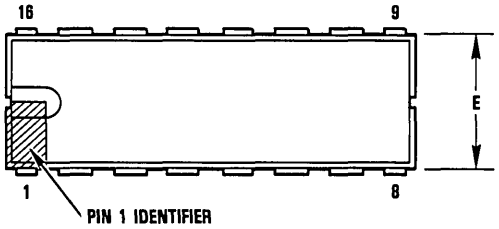
Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Nom ± Tol.
A	.064 (1.63)	.079 (2.01)	
b	.016 (0.41)	.020 (0.51)	
c	.007 (0.18)	.010 (0.25)	
E			.900 ± .009 (22.86 ± 0.23)
E_2			.800 ± .008 (20.32 ± 0.20)
e			.050 ± .005 (1.27 ± 0.13)
L	.350 (8.89)	.400 (10.16)	

Ref. 90X00181



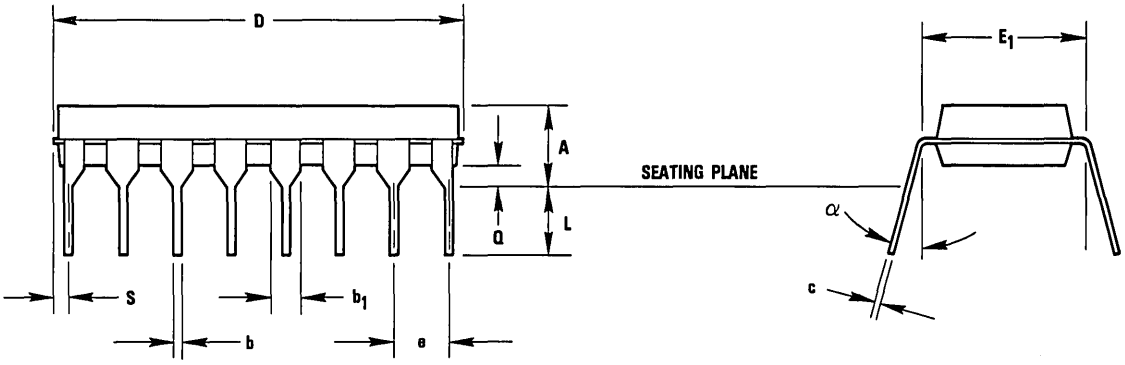
N9 Package
16 Lead Plastic DIP



Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Nom ± Tol.
A		.149 (3.78)	
b	.016 (0.41)	.020 (0.51)	
b_1	.058 (1.47)	.062 (1.57)	
c	.011 (0.28)	.013 (0.33)	
D			.757 ± .003 (19.23 ± 0.76)
E	.244 (6.20)	.252 (6.40)	
E_1			.300 ± .005 (7.62 ± 0.13)
e			.100 ± .005 (2.54 ± 0.13)
L	.125 (3.18)	.130 (3.30)	
Q	.011 (0.28)	.013 (0.33)	
S		.030 (0.76)	
α	0°	16°	

Ref. 90X00181

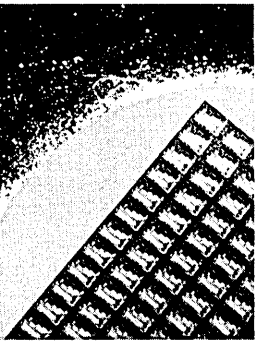


L

V L S I

D A T A

B O O K



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ACC Accumulate (Control)

An active-HIGH control signal which causes the contents of the product register to be added to (or subtracted from) the output of the multiplier in a multiplier-accumulator.

A_{GND} Analog Ground

Ground reference point for analog power supply and analog circuitry.

BW Full Power Bandwidth

Bandwidth specified for a flash Analog-to-Digital (A/D) converter is different from the bandwidth specification given for a purely analog device. Before attenuation becomes a significant factor in the performance of the converter, other problems may arise, leading to degraded performance. Spurious and missing codes might be encountered when the analog input frequency exceeds the bandwidth specification. Bandwidth for an A/D converter is the maximum frequency full-scale input sinewave that can be accurately quantized by the A/D converter without spurious or missing codes. A spurious code is a code which is grossly inaccurate, such as when the input signal is near mid-scale and an output code which is a full-scale output is generated. When the signal is reconstructed with a D/A converter, this spurious code looks like a glitch, and is therefore sometimes referred to as a glitch. Bandwidth is measured with worst case power supply conditions and sampling at the maximum sampling rate. (F_S).

The test used to determine the bandwidth of an A/D converter is the "Beat Frequency Test." The principle behind this test is to use "aliasing" to convert a high-frequency input signal to a low-frequency output signal which is easier to analyze. This is done by providing the A/D converter with a high-frequency sine wave input, and then sampling the input at a rate offset by a small delta in frequency from an integral (N) multiple of the input frequency. A D/A converter is given every Nth A/D output; this produces an output signal of the A/D which is an aliased version of the input. This is shown in figure 1, where the upper high frequency input is sampled at a rate slightly faster than three times its frequency (A/D samples are taken at the locations of the upper bars), every third A/D sample (lower bars) is presented to a D/A converter, and the resultant output signal is the bottom low frequency signal. In a typical set-up, the analog reconstruction (D/A output) is examined on an oscilloscope

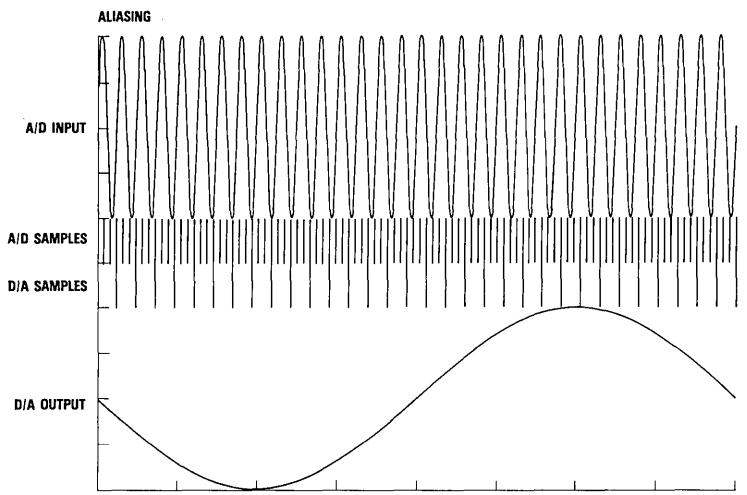

Figure 1. Beat Frequency Test

for spurious and missing codes. Figure 2 shows a typical test set-up. A spurious code is defined as a non-continuous change in the output of the A/D which is not reflected in the input signal. Figure 3 shows an example of a spurious code in the reconstructed output of an A/D converter. A missing code is defined as a code which has a code size less than the minimum specified (see definition for Q, code size). Figure 4 shows an example of the output of an A/D which has missing codes. The photographs for figures 3 and 4 were both obtained with a beat frequency test.

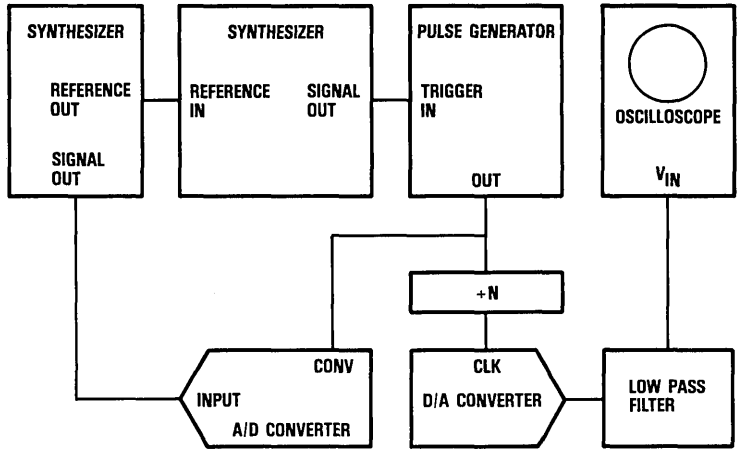

Figure 2. Beat Frequency Test Set-Up

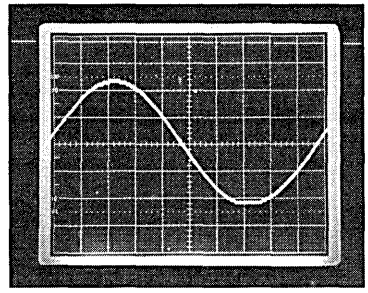

Figure 3. Spurious Code

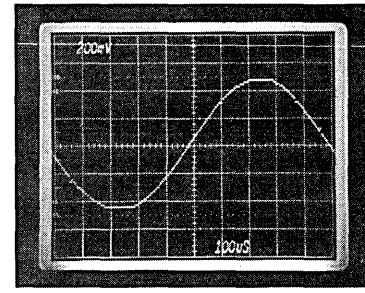

Figure 4. A/D Converter With Missing Codes

BWR Bandwidth, Reference

BWR specifies the maximum frequency at which the reference (V_{REF}) may be exercised. It is a small signal parameter since in many cases the reference may only be varied by a small portion of its full-scale value. Exceeding the BWR specification may result in the same types of coding errors encountered when the BW specification is violated.

C_I Digital Input Capacitance

The amount of capacitive loading present at a digital input. Digital input capacitance is measured with a capacitance bridge, applying a 1MHz signal to the input.

C_{IN} Input Equivalent Capacitance

C_{IN} is an approximation of the largely capacitive input impedance of a flash A/D converter. The input capacitance is slightly dependent upon the DC level of the analog input voltage and the input frequency. The input equivalent capacitance must be taken into account

when designing a buffer to drive a flash A/D.

The method used to test input capacitance involves sending a high-frequency signal through a transmission line to the analog input, and determining the input impedance by analysis of the reflected wave. This type of test is performed by an R.F. impedance analyzer.

C_O Output Capacitance

Parasitic capacitance between the output terminal of a device and ground.

CONV Convert (Input)

An input signal whose rising edge initiates sampling in a flash analog-to-digital converter. The input signal is quantized after a delay of t_{STO}.

C_{REF} Input Capacitance, Reference

Parasitic capacitance between the reference input terminal and analog ground.

DG Differential Gain

Differential Gain is defined as "The difference between (1) the ratio of the output amplitudes of a small high-frequency sine wave signal at two stated levels of a low frequency signal on which it is superimposed and (2) unity" [1]. Distortion-free processing of a color television signal demands that the amplitude of the chrominance signal not be affected by the luminance function. This is a relevant specification for the video industry since the saturation of the color being shown is represented by the amplitude of a small signal superimposed upon another signal which determines the brightness of the color. The standard method for measuring the differential gain of a device is by using a standardized test signal, known as a modulated ramp (refer to figure 5). The output of the A/D is then reconstructed by a reference D/A and low pass filter; the resultant signal is displayed on a vectorscope which is defined in reference [2]. During DG measurements the vectorscope display will be fuzzy due to quantizing errors in the A/D and D/A. The measurement requires interpretation of the peak-to-peak curvature of the center of the waveform. Figure 6 shows a vectorscope photo with DG testing in progress. The center line is indicated with a dashed line. There are theoretical bounds on differential gain performance described in [3]. The number specified on an A/D converter data sheet is the difference between the actual differential gain of the device and the theoretical performance. Figure 7 shows the typical test set-up that might be used in Differential Gain testing, which is described in more detail in reference [2].

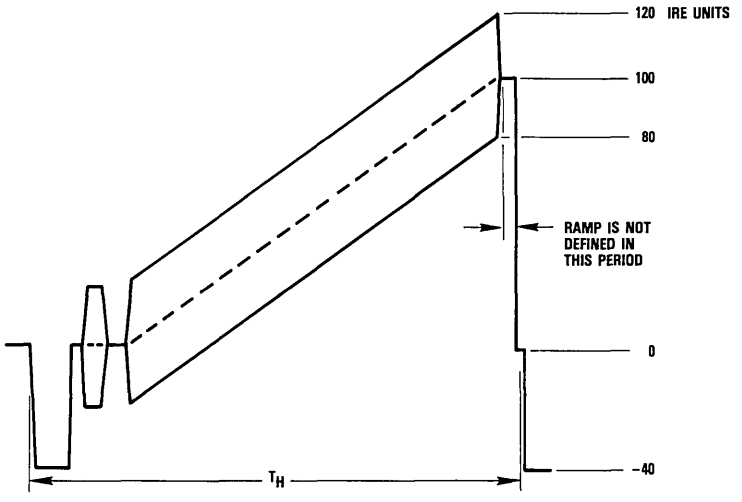

Figure 5. Modulated Ramp Test Signal

M

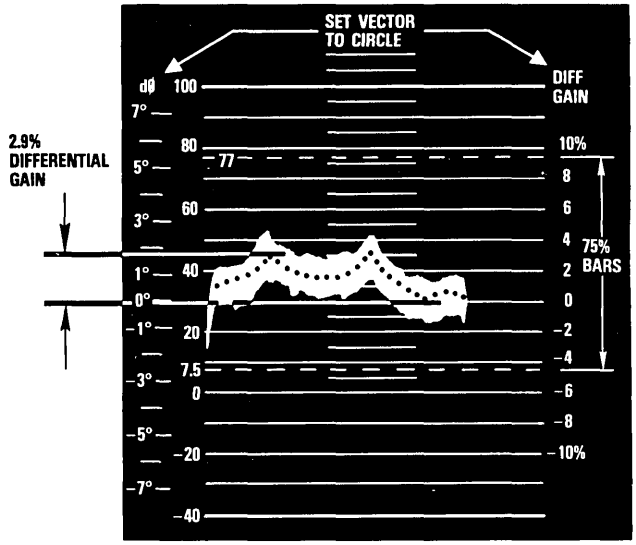

Figure 6. Differential Gain, Example Results

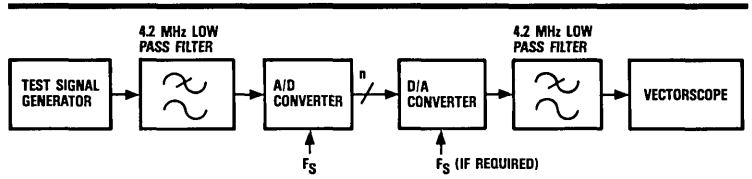

Figure 7. Differential Gain And Phase, Test Set-Up

D_{GND} Digital Ground

Ground reference point for digital power supply and digital circuitry.

DP Differential Phase

Differential Phase is defined as "the difference in output phase of a small, high-frequency, sine wave signal at the two stated levels of a low frequency signal on which it is superimposed" [1]. Distortion-free processing of a color television signal demands that the phase of the chrominance signal not be affected by the luminance function.

Differential phase errors appear on the T.V. screen as changes in the hue of the colors (tint) as the brightness changes. Differential phase testing is very similar to differential gain testing. The equipment shown in figure 7 is identical, and the display shown in figure 8 is similar to that of figure 6. The results are analyzed in the same manner as Differential Gain, taking the center line of the fuzzy line and finding its maximum peak-to-peak deviation. Reference [2] also describes differential phase testing of A/D converters.

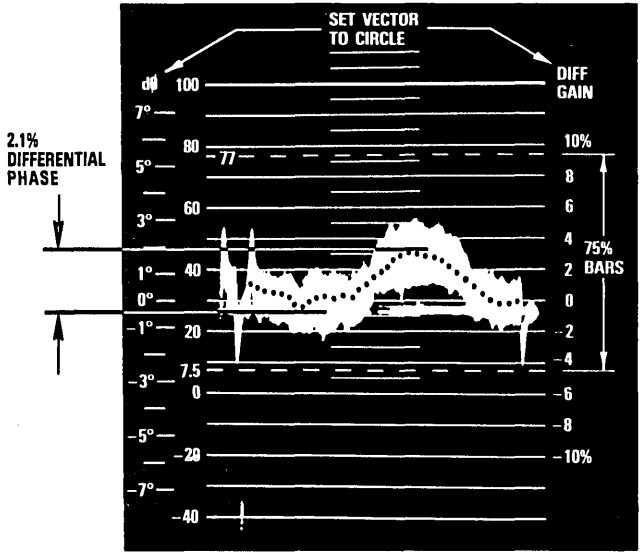

Figure 8. Differential Phase, Example Results

E_{AP} Aperture Error

Since there is an aperture of non-zero duration during which the A/D looks at a signal before conversion, there are errors introduced in the conversion. These errors are the effect of: aperture time (the amount of time during which the input signal is considered before conversion), aperture time uncertainty (the variation in aperture time) and aperture jitter which is the uncertainty in the starting instant of the aperture time. All of these effects are combined in a single parameter, Aperture Error (E_{AP}). Aperture errors cause a degradation of the SNR of the A/D converter with higher analog input frequencies and are estimated based upon this SNR degradation.

E_G Absolute Gain Error

The variation in the slope (gain) of the transfer function of a converter with respect to an established ideal transfer function. This error may be eliminated by adjusting the reference voltage or current applied to the device.

E_{LD} Linearity Error, Differential

Differential non-linearity is a measure of the uniformity of the code midpoint spacing. Differential linearity is defined as the maximum of the difference between adjacent code midpoints and the width of one Least Significant Bit (LSB), divided by the width of an ideal LSB (all units are in LSBs). If there is a missing code, the center of that code is considered to be the transition which skips that code. A differential non-linearity calculation is shown in figure 9. Another method that can be used to determine differential non-linearity is by a subtractive ramp test which examines the difference between adjacent quantization levels (see E_{LI}). This method is shown in figure 10. Differential non-linearity is sometimes measured with a statistical (histogram) test. In the histogram test the A/D converter is provided a full-scale sinusoidal analog input, and a large number of output samples are collected. The probability of obtaining each code is then calculated and the actual ratio of number of samples at that code to total number of samples is compared to this ideal probability. The differential linearity is then estimated, with the assumption that an increase in code width would result in a corresponding increase in the number of occurrences of that particular code.

M

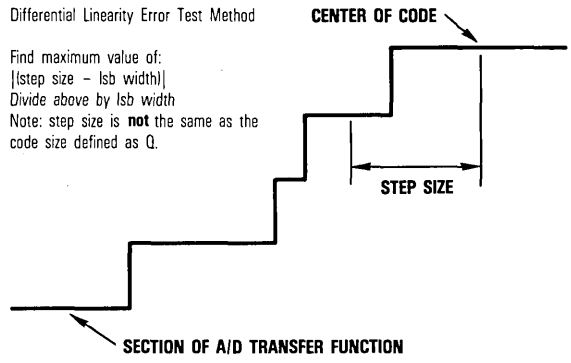

Figure 9. Differential Linearity Error

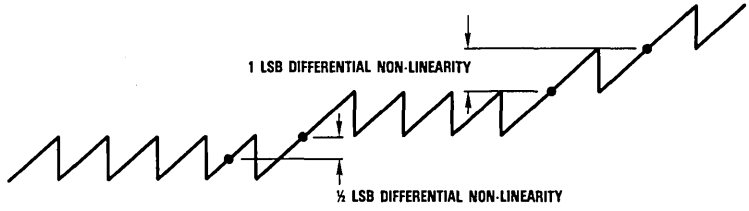

Figure 10. Differential Non-Linearity Measurement

E_{LI} Integral Linearity Error

Integral linearity is a measure of how the ideal and actual transfer functions of the A/D compare. The integral linearity error is the maximum difference between the actual and ideal quantization levels (the midpoint between adjacent threshold levels). A typical A/D transfer function showing different types of linearity errors is shown in figure 11. There are several methods for measuring integral linearity. Zero-based linearity is used mainly in bipolar systems with adjustments that allow the user to null any errors at the origin (the center of the transfer function). To measure zero-based integral linearity, a "straight line of best fit" is drawn through the origin. Then the maximum deviation of the actual transfer function from this line is determined. Terminal-based linearity measurements are similar to the zero-based; however the line is drawn between the two end points of the transfer function. The same difference signal is generated, and the same method is used for interpreting the results. The last common method for measuring independent-based integral linearity involves drawing the "straight line of best fit" through the transfer function, independent of the mid or end points, then calculating the error. When measuring integral linearity, a common test is the subtractive ramp test. A low-frequency ramp is digitized by the A/D converter, then the signal is reconstructed with a D/A converter. The reconstructed signal is now subtracted from the original ramp with a differential amplifier and the difference (error signal) is displayed on an oscilloscope. The sawtooth wave displayed on the oscilloscope can now be examined for integral non-linearities. Figure 12 shows the test set-up for the subtractive ramp test, and figure 13 is a photo of the oscilloscope screen during such a test. Figures 14, 15 and 16 show the measurement of zero-based, terminal-based and independent-based linearity error using the subtractive ramp test.

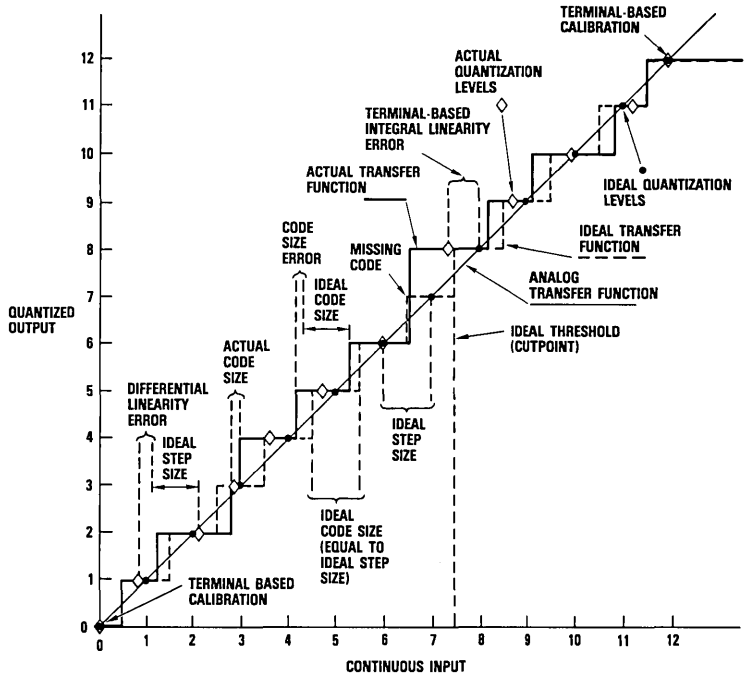

Figure 11. A/D Converter Transfer Function

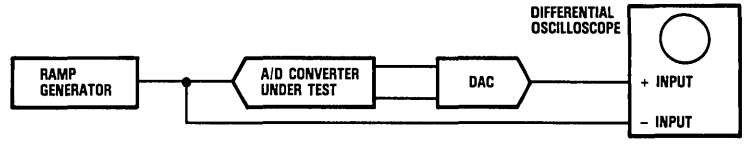

Figure 12. Subtractive Ramp Test Set-Up

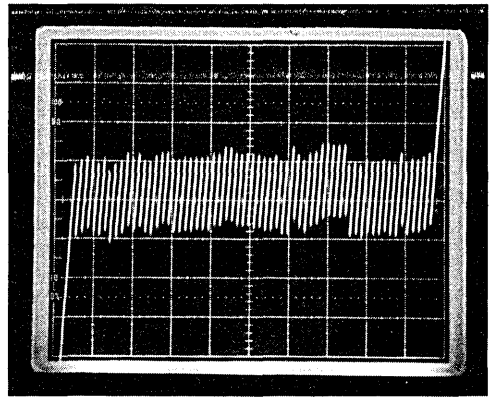

Figure 13. Subtractive Ramp, Example Results

M

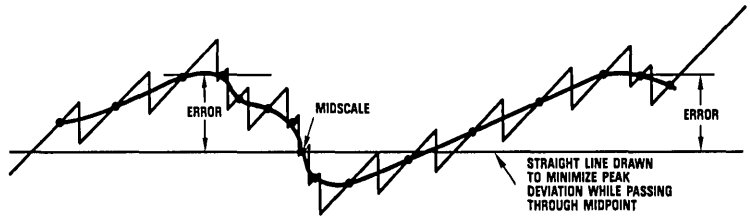

Figure 14. Zero-Based Linearity Measurement

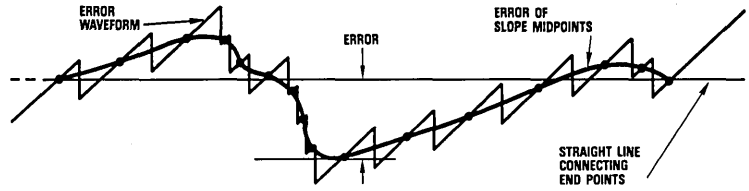

Figure 15. Terminal-Based Linearity Measurement

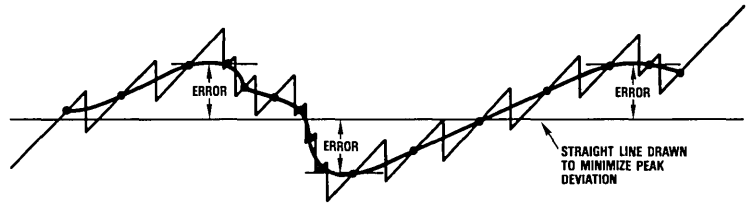

Figure 16. Independent-Based Linearity Measurement

E_{LI} Integral Linearity Error (Terminal-Based)
The maximum difference between the actual transfer characteristics of a converter and the straight line that passes through the end-points (terminals) of that data.

E_{OB}, E_{OT} Offset Voltage Bottom, Offset Voltage Top
Figure 17 shows the block diagram for a typical 6-bit flash A/D converter. There is a parasitic (R_P) resistance between the R_T lead and the first resistor. The voltage drop across this resistor is an offset voltage between the first code quantization level and the voltage applied to R_T. This offset is referred to as E_{OT}. The similar offset voltage at the bottom of the resistor chain is E_{OB}. E_{OT} and E_{OB} are measured by applying a known voltage to R_T and R_B and measuring the difference between these voltages and the voltages of the first and last code transitions of the A/D converter. In an ideal A/D, the first transition occurs at a point 1/2 LSB more negative than the top of the range. Therefore, if the input voltage to the device is set 1/2 LSB closer to R_B than zero, and V_{RT} is adjusted to get toggling between codes 0 and 1, then the voltage on R_T will be E_{OT}.

E_{OBS}, E_{OTS} Offset Errors, Sense Connected
To minimize the effect of offset errors, some A/D converters have sense outputs. These allow the use of a sense pin, which carries minimal current to close a feedback path around the reference input, resulting in lower offset errors. Figure 18 shows a block diagram for an A/D converter which has sense connections. Figure 19 shows how a feedback path is closed around an operational amplifier to make use of the offset sense point. E_{OBS} and E_{OTS} are the residual offset errors when the sense leads are used.

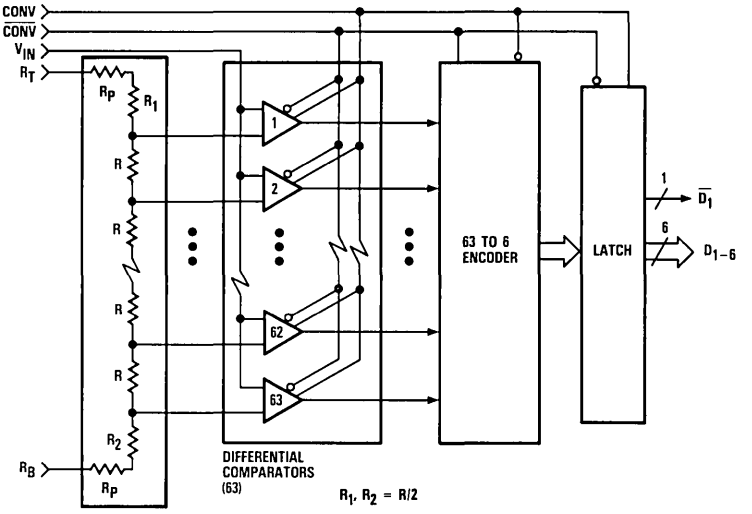

Figure 17. 6-Bit Flash A/D Block Diagram

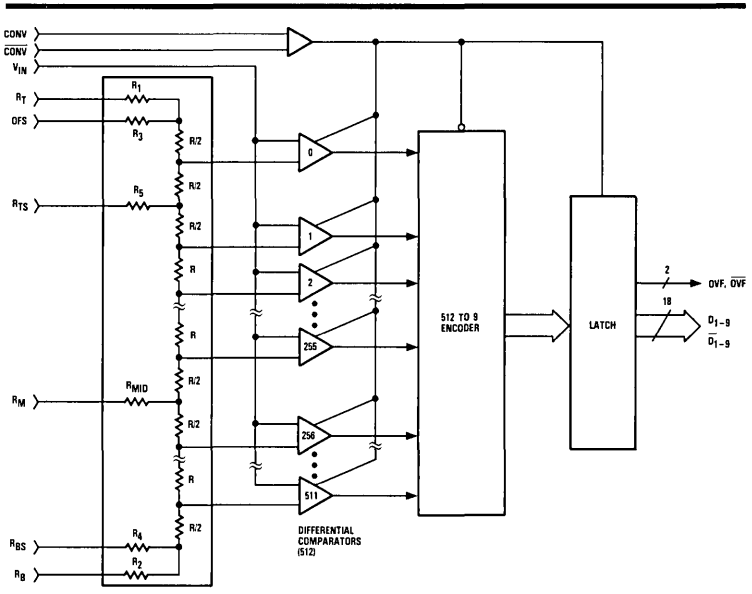

Figure 18. 9-Bit Flash A/D Block Diagram

M

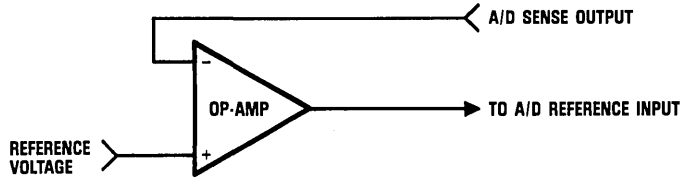

Figure 19. Driving A Reference With The Sense Connection

F_S Maximum Sampling Rate

F_S is a sampling rate (samples per second) at which the converter is guaranteed to operate. Most flash A/D converters will operate reliably at any rate up to the maximum sampling rate, which is measured with worst case supply, worst case duty cycle conditions, and maximum full-power input frequency.

FT_C, FT_D, FT_R Feedthrough -clock, -data, -reference

A measure of unwanted leakage from an input port of a device to another port (e.g., the analog output of a D/A converter), which is expressed in decibels relative to the full-scale value of the output. Clock and data feedthrough refer to spurious output noise arising from logic transitions at the clock and data inputs. Reference feedthrough relates to output variation as a function of reference variation in a D/A converter when data inputs correspond to a zero output.

G_C Peak Glitch Charge

The maximum product of the glitch current and the duration of the glitch; usually given in units of picoCoulombs (pC). Since glitches tend to be symmetric, the average glitch charge is usually much less than the peak glitch charge.

G_E Peak Glitch "Energy" (Area)

The maximum product of the glitch voltage and the duration of the glitch; usually given in units of picoVolt-seconds (pV-sec). Since glitches tend to be symmetric, the average glitch area is usually much less than the peak glitch area.

G_I Peak Glitch Current

The transient current deviation from the ideal output current during an input code transition.

G_V Peak Glitch Voltage

The transient voltage deviation from the ideal output voltage during an input code transition.

I_{CB} Input Current, Constant Bias[1]

The current drawn by the input of the A/D converter is dependent upon frequency and voltage level of the analog input. The current is sometimes also dependent upon the phase of the convert signal. This dependence is explained under I_{SB}, synchronous bias current; however, neglecting all of these second order effects, the current drawn by the input of the A/D is I_{CB}. This can be thought of as the sum of the comparator input bias currents which is dependent upon the input voltage level.

I_{CC} Supply Current[1]

I_{CC} is the current drawn by the device from the V_{CC} supply. I_{CC} is a positive valued parameter. I_{CC} decreases with increasing temperatures in bipolar devices and is measured with V_{CC} at the maximum rated value.

I_{DDL} Loaded Supply Current

Current flowing into the positive power supply terminals with all inputs and outputs toggling at the maximum clock rate, and an output test load of 500 Ohms and 40pF for CMOS devices. I_{DDL} is the current measurement under worst case conditions. In addition to the internal or unloaded supply current, the output buffer now requires current to charge and discharge the load capacitance. This parameter is frequency-dependent. (See I_{DDQ} and I_{DDU} for CMOS supply current under different measurement conditions.)

I_{DDQ} Quiescent Supply Current

Current flowing into the positive power supply terminals under quiescent conditons for CMOS devices. If the inputs are tied LOW, and the outputs are in a high-impedance state, no gates

Note: 1. All currents are defined as positive when flowing into the device.

are switching. As a result, the p-channel and n-channel transistors that compose the basic CMOS gate are neither charging nor discharging stray capacitance, and only leakage current flows into the positive supply. (See I_{DDU} and I_{DDL} for CMOS supply current under different measurement conditions.)

I_{DDU} Unloaded Supply Current

Current flowing into the positive power supply terminals of a CMOS device with all inputs toggling at the maximum clock rate, and the outputs in a high-impedance state. With the device unloaded, I_{DDU} includes only the components that contribute to the internal current: the leakage current when the gate is in a "0" or "1" state, and the current drawn during a gate transition. An increase in average gate switching frequency will lead to an increase in current. (See I_{DDQ} and I_{DDL} for CMOS supply current under different measurement conditions.)

I_{EE} Supply Current[1]

I_{EE} is the current drawn by the device from the V_{EE} supply. Since I_{EE} is referenced to a negative supply, it is a negative valued parameter (current flows out of the device). In TRW bipolar devices, I_{EE} decreases with increasing temperatures and is measured with the maximum (most negative) rated V_{EE}.

I_I Input Current, Maximum Input Voltage[1]

Current flowing into a digital input under worst-case power supply and input voltage conditions.

I_{IH} Input current, Logic HIGH[1]

I_{IH} is the current drawn by a digital input to the device when the potential of the terminal is in the logic HIGH state.

I_{IL} Input Current, Logic LOW[1]

I_{IL} is the current drawn by a digital input to the device when the potential of the terminal is in the logic LOW state.

I_{OF} Output Offset Current[1]

The residual output current of a D/A converter that flows when all internal current sinks are switched off.

I_{OH} Output Current, Logic HIGH[1]

I_{OH} is the maximum current that can be forced into (this is a negative value, therefore current flow is out of the device) an output terminal in the HIGH state, while potential at the terminal remains within the V_{OH} specification.

I_{OL} Output Current, Logic LOW[1]

I_{OL} is the maximum current that can be forced into an output terminal on the LOW state, while the potential at the terminal remains within the V_{OL} specification.

I_{ON} Maximum Current, - Output[1]

The maximum current that flows into the "OUT-" output of a D/A converter.

I_{OP} Maximum Current, + Output[1]

The maximum current that flows into the "OUT+" output of a D/A converter.

I_{OS} Output Short Circuit Current[1]

The current flowing from an output when the output is short circuited to ground while in the logic high state. This specification is usally indicated only on TTL compatible devices.

I_{REF} Reference Current

Current Flowing into or out of the reference input terminals of an A/D or D/A converter.

I_{SB} Input Current, Synchronous Bias

In some flash converters, the current flowing into the analog input varies slightly depending upon the state of the CONV signal. If the comparators are in the track mode (CONV LOW), then the input current is greater, and the amount of this current change is ISB, synchronous bias current.

MSPS Megasamples Per Second

The abbreviation for the conversion rate (clock or convert frequency) at which an A/D or D/A converter is operating.

NPR Noise Power Ratio

"NPR is the decibel ratio of the noise level in a measuring channel with the baseband fully noise loaded to the level in that channel with all of the baseband noise loaded except the measuring channel: [4]. To test NPR, the input of

Note: 1. All currents are defined as positive when flowing into the device.

the A/D converter is presented with white noise having a frequency spectrum from low frequencies up to 1/2 the sampling rate. The power of the input noise is adjusted so that the converter is fully loaded, but not clipping excessively. The output of the A/D converter is then converted back into an analog signal with a D/A. The D/A output is passed through a very narrow band pass filter, and the output power of the signal is measured. The process is now repeated, but with a notch filter at the input of the A/D converter. The ratio of the two measured powers is the Noise Power Ratio, and is often expressed in dB:

$$NPR = 10 \log_{10}(ratio)$$

NPR is often used to determine how much noise will "bleed" into one channel from other channels in a broadband, frequency domain multiplexed system.

PREL Preload (Control)

A control signal which determines (in conjunction with the three-state control pins) which of three signals is to be loaded into the output register at the rising edge of the product clock: the result of the calculations which were just performed, the present contents of the output register, or a value applied to the output port by external circuitry.

PSS Power Supply Sensitivity

A measure of DC variation of an output under consideration (e.g., the analog output of a D/A converter) as the power supply voltage is varied around the nominal value. PSS is specified in milliAmps or milliVolts of output change per Volt of supply change.

PSRR Power Supply Rejection Ratio

A measure of high-frequency noise rejection from the power supply inputs of a device to the output under consideration (e.g., the analog output of a D/A converter). Expressed in decibels relative to full-scale output. Generally, PSRR decreases with increasing frequency and for this reason is often specified at more than one frequency.

Q, CS Code Size

Code size is the size of the individual codes, from code transition to code transition. It is often expressed as a percentage of the ideal code size. The ideal code size is given by:

$$\frac{\text{Input Voltage Range}}{2^N}$$

Where N is the number of bits of resolution of the A/D converter.

Q is also defined as the total number of quantizing levels or codes output by a converter (2^N) with N being the number of bits of resolution provided by the A/D.

RES Resolution

The smallest level separation (input level of A/Ds and output level for D/As) that is unambiguously distinguishable over the full-scale range of a converter. It is expressed as a percentage of full-scale or as an equivalent number of bits, usually the number of data inputs of a D/A or data outputs of an A/D converter.

R_{IN} Analog Input Impedance

Although the input impedance of a flash A/D converter is largely capacitive, it does have a resistive component which is approximated with R_{IN} the input resistance. R_{IN} varies with the input voltage.

R_O Equivalent Output Resistance

The effective equivalent resistance between an analog output terminal of a D/A converter and analog ground.

R_{REF} Reference Resistance

R_{REF} is the total resistance of the entire reference resistor chain, including parasitics. It can be measured directly between R_T and R_B. Another method of testing R_{REF} is to calculate it from I_{REF} and (V_{RT} - V_{RB}).

R_S Register Shift (Control)

A control signal which changes the output format to permit a valid result for the product of two most negative numbers.

SNR Signal-To-Noise Ratio

The signal-to-noise ratio is the ratio of the value of the signal to that of the noise. The values of the signal and of the noise are usually RMS, but for some signals such as video, it is defined as peak-to-peak signal vs RMS noise, because it is difficult to

determine the RMS value of a video signal, and the meaning of peak-to-peak noise is not a useful parameter. The signal-to-noise ratio of an A/D converter provides a good figure of merit for the dynamic accuracy of the device. To test SNR, the A/D converter is given a high purity sine wave input. This is sampled at a non-harmonic sampling rate and the output of the A/D converter is stored in memory. The data from the A/D are then transformed into the frequency domain with a Fast Fourier Transform (FFT) and analyzed to determine the SNR. When analyzing the data most of the "noise" will be located at the harmonic frequencies; therefore the SNR is a good estimate of total harmonic distortion. The analysis method takes the RMS or peak-to-peak voltage of the signal, and divides it by the RMS value of the noise. SNR is usually expressed in dB with the formula below:

$$SNR = 20 \log_{10} \frac{\text{Signal}}{\text{Noise}}$$

SUB Subtract (Control)

A control signal which determines whether the present contents of the output register is added to (SUB = LOW) or subtracted from (SUB = HIGH) the product at the output.

T_A Ambient Temperature

For standard temperature range devices, the temperature range is specified in terms of the ambient temperature (still air) surrounding the converter.

T_C Case Temperature

For extended temperature range devices, the temperature range is specified in terms of the case temperature.

TC Two's Complement (General Definition)

Two's complement is a binary numbering system in which the Most Significant Bit (MSB) carries the sign information by virtue of a negative place value. In two's complement, an MSB of ZERO signifies a positive number, a ONE denotes a negative number, and the negative number order is reversed from straight binary. That is, the number which consists of all ONEs is the least negative number, and the number which consists of a ONE and all ZEROs is the most negative number.

TC Two's Complement (Control)

An active HIGH signal which designates one or both inputs as two's complement numbers. If TC is LOW, unsigned magnitude processing will be used. Note that some parts allow independent designation of each input as two's complement or unsigned magnitude, and other parts do not.

TC_G Gain Error Tempco

The factor which linearly approximates the variation with temperature of Absolute Gain Error, E_G.

T_{CO} Temperature Coefficient

T_{CO} is the factor which linearly approximates the variation with temperature of Offset Errors (E_{OT}, E_{OB}). This is a first order approximation and the actual temperature coefficient is a function of temperature which may exceed the maximum of T_{CO} in some temperature ranges.

t_D Output Delay

t_D is the time between the rising edge of the CONV signal and the time at which the output data from the A/D is guaranteed to be stable. On many TTL flash A/D converters, this delay can be reduced by the addition of pull-up resistors from the data outputs of the device to the V_{CC} supply. This output delay is measured with the test load specified in the corresponding data sheet.

t_H Hold Time

The time period after the operative edge of CLK signal during which input data must be constant in order to be correctly registered.

t_{HO} Output Hold Time

The time from the rising edge of the convert signal to the time when the output data lines begin to change.

t_{PW} Pulse Width

The time period between consecutive edges of a logic pulse.

M

t_{PWH} Pulse Width High

t_{PWH} is the minimum width high CONV pulse with which the A/D will accurately operate if all other specifications are met. t_{PWH} is measured from the 1.3 Volt level of the rising edge of the CONV signal to the 1.3 Volt level of the falling edge of the CONV signal on TTL compatible devices. If the CONV signal has a low portion of t_{PWL}, and a high portion of t_{PWH}, the device may be exceeding F_S in which case it may not operate properly. The performance of many A/D converters performance can be improved by making t_{PWH} as long as possible.

t_{PWL} Pulse Width Low

t_{PWL} is the minimum width low CONV pulse with which the A/D will accurately operate if all other specs are met. t_{PWL} is measured from the 1.3 Volt level of the falling edge of the CONV signal to the 1.3 Volt level of the rising edge of the CONV signal on TTL compatible devices.

TRIL Three-State Least Significant Product (Control)

A control which enables the output state for the least significant product when in the LOW state, and places the output stage for the least significant product in the high-impedance state when HIGH.

TRIM Three-State Most Significant Product (Control)

A control which enables the output stage for the most significant product when in the LOW state, and places the output stage for the most significant product in the high-impedance state when HIGH.

t_S Setup Time

The time period prior to the operative edge of the clock signal during which input data must be stable in order to be correctly registered.

TSL Three-State Least Significant Product (Control)

A control which enables the output stage for the least significant product when in the LOW state, and places the output stage for the least significant product in the high-impedance state when HIGH. A HIGH on this control also forces the most significant product section of the output register to be preloaded at the rising edge of the product clock when PREL is active.

TSM Three-State Most Significant Product (Control)

A control which enables the output stage for the most significant product when in the LOW state, and places the output stage for the most significant product in the high-impedance state when HIGH. A HIGH on this control also forces the most significant product section of the output register to be preloaded at the rising edge of the product clock when PREL is active.

t_{STO} Sampling Time Offset

Sampling time offset is the time interval between the rising edge of the CONV signal and the actual instant at which the A/D samples the input signal.

TSX Three-State Extended Product (Control)

A control which enables the output stage for the extended product when in the LOW state, and places the output stage for the extended product in the high-impedance state when HIGH. A HIGH on this control also forces the extended product section of the output register to be preloaded at the rising edge of the product clock when PREL is active.

t_{TR} Transient Response

t_{TR} is the amount of time required for the converter to recover from a fullscale input transition, before valid data can be produced. The comparators in a flash A/D converter have a finite slew rate and a finite settling time. If a device is presented with a full-scale input change (which exceeds that slew rate), it takes t_{TR} for the input circuit to recover and provide accurate data.

V_{AGND} Analog Ground Voltage

Potential of the analog ground terminal with respect to the digital ground terminal.

V_{CC} Positive Supply Voltage

The positive power supply voltage required for operation of a device.

V_{EEA}, V_{EED}, V_{EE} Supply Voltage

V_{EE} is the negative supply voltage. On converters with both digital and analog

negative supplies, the analog supply is denoted $V_{EE}A$, and the digital supply is $V_{EE}D$.

V_{ICM} Input Voltage, Common Mode Range
The operational limit over which a differential logic input voltage may be varied.

V_{IDF} Input Voltage, Differential
The voltage difference between a logic input and its complementary input.

V_{IH} Input Voltage, Logic HIGH
The voltage required on a digital input in order for that input to be forced to a valid logic HIGH state.

V_{IL} Input Voltage, Logic LOW
The voltage required on a digital input in order for that input to be forced to a valid logic LOW state.

V_{OCN} Voltage Compliance, - Output
A measure of the range over which the output voltage of a current generator may be varied. V_{OCN} is the voltage compliance of the - output of a D/A converter.

V_{OCP} Voltage Compliance, + Output
V_{OCP} is the voltage compliance of the + output of a D/A converter. See V_{OCN}.

V_{OH} Output High Voltage
The potential at an output terminal in the high state with respect to digital ground, when loaded with the test load defined in the data sheet. V_{OH} is measured with V_{CC} at a minimum.

V_{OL} Output Low Voltage
The potential at an output terminal in the low state with respect to digital ground, when loaded with the test load defined in the data sheet. V_{OL} is measured with V_{CC} set to the maximum value.

V_{OZS} Output Voltage, Zero Scale
The residual output voltage of a D/A converter that appears at its output when all internal current sinks are switched off.

V_{RB} Reference Bottom Voltage
The potential of the R_B terminal with respect to analog ground.

V_{RM} Reference Middle Voltage
The potential of the R_M terminal with respect to analog ground.

V_{RT} Reference Top Voltage
The potential of the R_T terminal with respect to analog ground.

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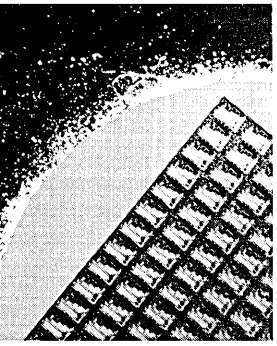

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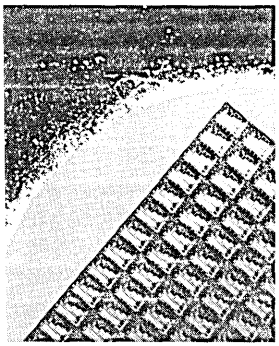

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Application Notes And Reprints (Listings)

Application Notes

TP-1 "Multiplier-Accumulator Application Notes" by L. Schirm IV.
Covers the use of multiplier-accumulators including an explanation of the clock, input and output controls. Other discussions include: larger word accumulations, multiplication plus a constant, operation with microprocessors, digital filters and complex multiplication.

TP-2 "Monolithic Bipolar Circuits for Video Speed Data Conversion" by W. Bucklen.
Describes the "flash" A/D converter, TDC1007J, and the TDC1016J, D/A converter. Also included are approaches for extending the performance of the TDC1007J.

TP-4 "Digital Signal Processing for Radar Systems" by W. Finn.
Describes how VLSI multipliers and multiplier-accumulators can be used in a radar signal processor to achieve data rate reduction, by means of predictive mechanization; pulse compression, utilizing an FIR matched filter; maximum computational capabilities, via pipelining; and high-speed convolution, using 2-point DFTs and a complete FFT processor.

TP-5 "An LSI Approach to Digital Signal Processing Enhances Telemetry Systems" by W. Finn.
All aspects of Telemetry have one thing in common: an increasing need for high-speed digital signal processing. The impact of large scale integrated (LSI) circuitry on telemetry systems is a topic of increasing importance. Dependency of real-time digital signal processors on LSI circuitry is largely due to the advantages they afford: smaller size, faster speed, lower power consumption, more reliability and less cost. These advantages are over and above those which can be achieved by SSI, MIS, or even analog circuitry.

TP-6 "Introduction to the Z-Transform and its Derivation" by R. Karwoski.
A tutorial discussion of LaPlace and Z-transforms and their use in sampled data systems. Application of the Z-transform to filter synthesis is also treated.

TP-7A "Hardware Development for a General Purpose Digital Filter Computing Machine" by R. Karwoski.
This paper describes the hardware for a flexible, fast, digital filter computing machine that can be easily programmed. Emphasis is on real-time signal processing, particularly in the area of digital filtering.

TP-8 "Second Order Recursive Digital Filter Design with the TRW Multiplier-Accumulators" by R. Karwoski.
Develops the fundamental concepts for second order recursive digital filters and describes some efficient hardware implementations using the TDC1010J multiplier-accumulator.

TP-9 "A Four-Cycle Butterfly Arithmetic Architecture" by R. Karwoski.
Explains the background of the FFT and the computational element called the butterfly. A block diagram of the FFT processor is presented and the DAU (Data Arithmetic Unit) architecture is described in detail. The text's description of the four FFT instructions is supplemented by computational diagram, block diagrams, a data flowchart and a timing diagram.

TP-10 "An Introduction to Digital Spectrum Analysis Including a High-Speed FFT Processor Design" by R. Karwoski.
Develops the DFT using well-known continuous Fourier Transform and series concepts. Common spectrum analysis terms are defined with respect to the DFT, and the decimation in time FFT is derived in detail. Describes the design of a high-speed FFT processor, particularly the architecture and address generation. Also included is an explanation of the use of bit-slice microprocessors as FFT sequencers.

TP-16 "An LSI Digital Signal Processor for Airborne Applications" by L. Schirm IV.
Discusses the background of digital signal processing with emphasis on radar processors. Described is a digital signal processing board, employing a multiplier-accumulator IC, which includes the basic processor, address generators, controller and system interface.

TP-17 "Correlation–A Powerful Technique for Digital Signal Processing" by J. Eldon.
Correlation techniques find use in communications, instrumentation, computers, telemetry, sonar, radar, medical, and other signal processing systems. Electronic systems that perform correlation have been around for years, but they have been bulky and inefficient. The development of a new VLSI chip from TRW LSI Products has changed this; now correlation can be performed efficiently with a minimum number of components.

TP-18 "LSI Multipliers Application Notes."
Describes larger and smaller word multiplication, higher speed multiplication and division using multiplication.

TP-19 "Non-Linear A/D Conversion" by B. Friend.
Describes the quantization process necessary to produce a non-linear transfer function. TRW LSI Products offers A/D converters which can be used in place of more expensive or impractical methods to achieve this result with a minimum of cost and effort.

A discussion of a typical TRW A/D converter includes information on the internal circuitry of the device and provides diagrams of circuit modifications to use with the A/D converter to improve performance.

TP-22 "A Guide to the Use of the TDC1028; a Digital Filter Building Block" by F. Williams.
Discusses word and length sizing of Finite Impulse Response (FIR) digital filters, and implementation of filters with different lengths and word sizes. A circuit to autoload coefficients in stand-alone applications is also provided.

TP-23 "A 22-Bit Floating Point Registered Arithmetic Logic Unit" by J. Eldon.
Introduces the TDC1022, a registered arithmetic logic unit (RALU), built with TRW's dual layer metal, one micron bipolar process (OMICRON-B ™). Emphasis is on RALU architecture, and the instruction microcode. Block diagrams and ALU function control chart are provided.

TP-24 "A Single Board Floating Point Signal Processor" by G. Winter and B. Yamashita.
Floating point arithmetic offers many advantages to the field of digital signal processing (DSP). This article describes the realization of a Finite Impulse Response (FIR) filter using a family of floating point devices; the TDC1022 Floating Point Adder, the TDC1033 Floating Point Registered ALU, and the TDC1042 Floating Point Multiplier.

TP-25 "Floating Point Hardware for Digital Signal Processing" by J. Haight.
Recent advances in VLSI circuitry make high-speed digital signal processing (DSP) with wide dynamic range possible without significant penalties in cost or hardware overhead. The architectures of the TDC1022, TDC1033 and TDC1042 are discussed, as well as their applications in some designs.

TP-26 "Floating Point, the Second Generation for Digital Signal Processing" by J. Haight.
High-speed digital signal processing (DSP) has recently progressed to a widely used real or near real-time field. Today, a new generation of 22-bit floating point integrated circuits (TDC1022, TDC1033 and TDC1042) makes it possible to build circuitry to handle signals with wide dynamic range at high speeds and reasonable cost. This article discusses the architecture of these ICs and the motivations behind them.

TP-27 "Components For Instruments That Employ Digital Signal Processing Techniques" by D. Watson.
Applications of fast analog-to-digital (A/D) converters are expanding into the measurement and analytical instrument marketplace. This article discusses A/D converters as they are used in digital instruments, reviews "flash" A/D technology, and presents future directions of A/D design.

TP-28 "A Floating Point ALU for Digital Signal Processing" by R. Sierra and G. Covert.
Discusses applications of the TRW LSI TDC1022, Floating Point Arithmetic Unit. The architecture of the TDC1022 is discussed, together with several application examples in the areas of filtering and spectrum analysis.

TP-29 "The Use of Floating Point Arithmetic in Digital Filters and Equalizers" by F. Williams.
Digital Audio, a high-performance technology, has undergone rapid growth during the last few years. This article describes TRW LSI floating point processors and how they are used in digital audio systems to provide noise control, accurate response control, and maintenance of effective SNR. Frequency response high and low filter graphs are provided.

TP-30 "Understanding Flash A/D Converter Terminology" by M. Sauerwald.
A comprehensive list of parameter definitions that TRW LSI Products uses in flash A/D converter data sheets.

TP-31 "An Introduction To Two Different Finite Impulse Response Structures by F. Williams.
Digital filtering is a rapidly expanding field, and the design process is not dramatically different from design techniques for high-performance analog filters. However, due to the flexibility of the digital approach, additional design decisions are necessary. This application note presents two different forms for Finite Impulse Response (FIR) digital filters. Theoretical discussion is included.

TP-32 "The TDC1048, A New Low Power 8-Bit A/D Converter" by Dr. D. Packard.
For video speed flash converters, significant improvements in packaging, cost, and ease of use can be obtained by emphasizing low power in the converter design rather than ultimate speed. The TRW TDC1048 8-bit flash converter uses TRW's OMICRON-B ™ 1-micron bipolar process to create a 20MSPS device with dynamic performance equal to or better than any comparable speed converter with low enough power to allow a compact easy-to-use package. Discussion includes design and process features as well as performance characteristics.

TP-33 "Using the TDC1018 and TDC1034 in a TTL Environment" by D. Watson.
The TDC1018 and TDC1034 digital-to-analog converters (D/A) were designed for operation in systems that employ ECL logic families. However, there are many TTL systems that require the use of high-speed D/A converters but have only +5 Volt power supplies available. The TDC1018 and TDC1034 can easily be used in a TTL environment; this application note discusses practical circuits and clarifies some of the issues.

TP-35 "High-Speed Color Palette Memory For The TDC1034 Graphics Ready DAC" by Dan Watson.
Design of a Color-Palette Memory for 4 and 8-bit "Graphics-Ready" A/D converters is described herein. Included are a block diagram and detailed schematic for 3 x 256 x 4 Color-Palette. Other related information is given for CRT graphics applications.

Article Reprints

R-1 "Packing a Signal Processor onto a Single Digital Board," by L. Schirm IV, **Electronics**, December 20, 1979.

Discusses general applications of multiplier-accumulators and the design of a single-board FFT processor.

R-2 "Microprocessor Compatible Recursive Digital Filters," by Ford, Youseff-Digaleh and Current (UC Davis); **Proceedings of the IEEE**, April 1979.

Describes the implementation of recursive digital filters through time-shared use of a single multiplier-accumulator.

R-3 "A Radix-4 FFT Processor for Application in a 60-Channel Transmultiplexer Using TTL Technology," by Roste, Haaberg and Ramstad; **IEEE Transactions on Acoustics, Speech and Signal Processing**; Vol. ASSP-27, No. 6, December 1979.

Presents a hardware solution for the two 128-point DFT processors with a transform time of 125 sec needed in a 60-channel transmultiplexer for conversion between FDM and TDM signals.

"Design of a 24-Channel Transmultiplexer," by M. Narashima; **IEEE Transactions on Acoustics, Speech and Signal Processing**; Vol. ASSP-27, No. 6, December 1979.

Discusses the design of a transmultiplexer capable of performing the bilateral conversion between 1544 kbits/sec digital signal and two analog group signals.
Note: Both articles are included in the same reprint.

R-4 "Television Gathers Speed On its Way from A to D," **Broadcast Communications**, September 1979.

Explains the ways in which the TV broadcast studio is evolving towards digital implementations. Discusses the advantages of the digital vs the analog approach.

R-5 "Get to know the FFT and take advantage of speedy LSI building blocks," by L. Schirm IV; **Electronic Design**, April 26, 1979.

Explains the use of the FFT (Fast Fourier Transform) and how to implement an FFT processor board using a multiplier-accumulator.

R-6 "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform," by F. Harris, **Proceedings of the IEEE**, January 1978.

A comprehensive discussion of data windows and their effect on the spectrum analysis problem. Key parameters are identified, and window options are compared. Applications are discussed in detail.

R-7 "Floating-point chips carve out FFT systems," by J. Eldon and G. Winter; **Electronic Design**, August 4, 1983.

Describes the implementation of real-time signal processing using a set of three floating point ICs: the TDC1033, an arithmetic logic unit with registers; the TDC1042, a floating point multiplier; and the TDC1022, a floating point arithmetic unit.

R-8 "Quantization Effects on Differential Phase and Gain Measurements," by F. Williams and R. Olsen; **SMPTE Journal**, November, 1982.

Discusses absolute performance standards as a means of characterizing television systems. Equations are provided which are used to obtain Differential Phase and Differential Gain limits for use in the evaluation and diagnosis of television equipment.

R-9 "High speed FIFO memory: theory and applications," by E. Chocheles and R. Sierra, **Electronic Products**, March 28, 1983.

A comprehensive study of the TDC1030, a First-In First-Out (FIFO) memory buffer (fixed or variable-length storage) used in data transfer elements. Extensive timing analysis is covered in the article.

R-10 "One-chip DAC delivers composite video signal," by R. Castleberry and C. Robertson; **Electronic Design**, September 1, 1983.

Describes the TDC1018, a low-cost, digital-to-analog converter that delivers a composite video signal, capable of driving high-resolution graphics displays. Device architecture and performance specifications are included.

R-11 "Single-chip Flash A/D Converters With Evaluation Boards," by J. Eldon and R. Olsen; **Proceedings IEEE 1982 Region 6 Conference.**

Describes TRW LSI Products' A/D Converters and optional evaluation boards. The boards may be used to evaluate the ICs, or as models for individual circuit design effects.

R-12 "6-bit a-d chip steps up the pace of signal processing," by J. Muramatsu and R. Olsen; **Electronic Design**, September 16, 1982.

Describes the TRW LSI TDC1029, a 6-bit analog-to-digital converter that samples broadband signals at 100 MegaSamples Per Second (MSPS). This device increases the real-time performance of military, medical and industrial systems.

R-13 "Video-speed filtering gets its own digital IC," by F. Williams; **Electronics**, October 20, 1983.

Describes the TRW LSI TDC1028, a single-chip filter that is paving the way to video-speed fixed and adaptive filter implementations in design processes.

R-14 "One-Micron VLSI Chips for Military Systems," by Dr. J. Eldon, M. Gagnon and F. Williams; **Defense Electronics**, November 1983.

Describes TRW's one-micron VLSI chips and their applications for military systems. The article also discusses the bipolar 3-D process used in fabricating the devices, VLSI reliability, and other topics related to implementation of these chips.

R-15 "Using high speed multipliers for real time signal processing," by R. Sierra; **Electronic Products**, February 7, 1984.

Complex signal processing can now be implemented with the precision and accuracy of digital arithmetic logic components. This article describes TRW LSI Multipliers and their usefulness in filtering and spectrum analysis.

R-16 "CMOS comes to high speed digital signal processing," by J. Haight; **Electronic Products**, February 1984.

Discusses the possibilities for CMOS: as geometries continue to shrink, the improved performance and reduced power of CMOS make possible a much greater number of devices on a chip. This opens up many exciting possibilities in the digital signal processing market.

R-17 "Digital correlator defends signal integrity with multibit precision" by Dr. J. Eldon; **Electronic Design**, May 1984.

Correlation serves as the most effective means of measuring time delays or detecting weak signals in the presence of interference. Single-bit digital correlator chips excel in applications such as continuous-wave radar, but often lack precision needed for matching optical patterns or measuring ultrasonic time delays. The demand for greater quantization precision is satisfied by TRW's multibit TMC2220, a general-purpose digital correlator. Theory and practical applications presented with applicable diagrams.

R-18 "High-speed video D/A converters simplify graphics-display designs" by R. Castleberry; **Electronic Design News**, May 1984.

This article discusses some of the main features of a graphics-display system and the resulting tradeoffs, design parameters and architectures, with special emphasis on the D/A conversion process, and the use of the TRW TDC1018.

R-19 "Digital Signal Processing in Radar" by J. Haight; **Defense Electronics**, May 1984.

VLSI adds new dimensions to radar and EW signal processing. Much of the current work in radar consists of implementing ideas formulated right after World War II. As technology grows, so does the potential performance of radar, especially as related to digital signal processing, which has made the biggest difference in radar performance in the last decade. This article discusses the benefits of using DSP components with respect to radar. Detailed diagrams accompany the text.

R-21 "Multiplier-accumulator derives high performance from 1-micron CMOS" by F. Williams; **Electronic Design**, October 1984.

This discussion of 1-micron CMOS technology includes background information on the TRW TMC2160, a CMOS multiplier-accumulator. Topics covered are: choosing a number format, flexible control structure, slowing down word growth, and rounding for precision. In-depth diagrams accompany the text.

R-22 "Digital correlators suit military applications" by Dr. J. Eldon; **Electronic Design News**, August 1984.

This article presents the theory behind correlation and how it can serve applications ranging from spread-spectrum communications to optical alignment. With the advent of high-speed, low-power digital correlators such as the TRW CMOS TMC2220, which can overcome the calibration drift that analog correlators can exhibit when exposed to varying operating temperatures and voltages, digital correlators seem to be the direction of the future.

The Application Notes and Article Reprints listed above are available upon request from TRW LSI Products.

R-23 "DSP ICs – A Look Ahead" by Robert R. Yamashita; **Integrated Circuits Magazine**, October 1984.

The author examines how the evaluation of IC fabrication has brought about changes in the field of DSP. The advent of improved CMOS technology coupled with substantially more sophisticated CAE now affords revolutionary new product designs for DSP chips.

R-24 "Increased A/D Resolution Improves Image Processing" by Ellen Chocheles; **Electronic Products Magazine** October 15, 1984.

The article describes the benefits of utilizing a TDC1048 as a low-cost 8-bit flash converter for improved systems performance without extensive design overhead.

R-25 "High-Speed D/A Converters Yield Precision Graphics" by Randel Castleberry; **Computer Design** November 1984.

Megasample-per-second chips improve resolution, precision and flexibility of computer system displays.

The Application Notes and Article Reprints listed above are available upon request from TRW LSI Products.

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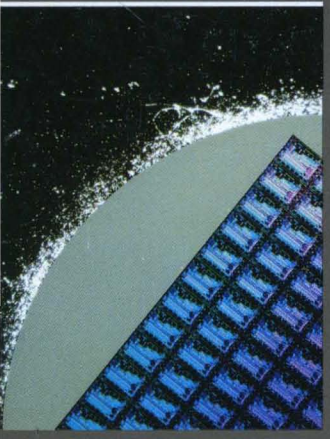

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