Linear Integrated Circuits DATABOOK

UNITRODE

IC500

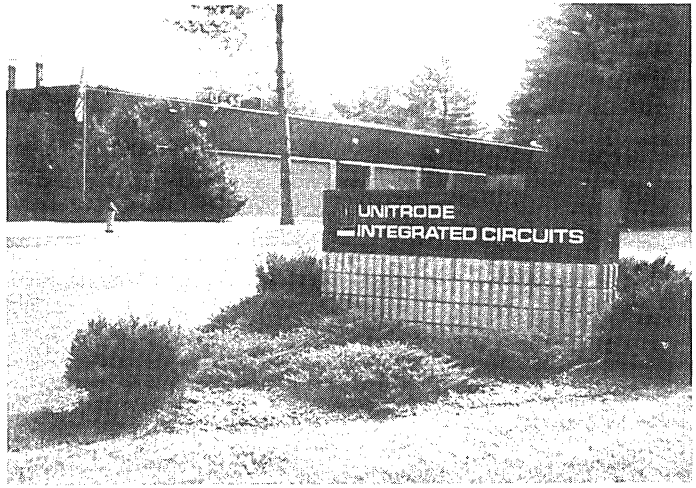
Unitrode Linear IC DATABOOK 1987-1988

IC

INTRODUCTION

Unitrode Integrated Circuits Corporation is a recognized leader in the development and manufacture of high performance circuits for power management. The company provides significant IC products for switching power supplies, motor drives and special function circuits, optimized for smart-power applications.

We are committed to the creation of new and innovative circuits to serve unique and valuable functions. To achieve this goal, we take a totally integrated approach to definition, development and production. Design and process engineers work together, often directly with customers, so that users can maximize their impact on product development.



Unitrode's state-of-the art manufacturing facility in Merrimack, New Hampshire, has been awarded JAN Microcircuit Certification. The facility includes 65,000 square feet dedicated to engineering, wafer fabrication, assembly and testing. Volume assembly operations take place at other facilities in the United States and the Far East.

We are also committed to objectives of the Unitrode Corporation described in its Mission Statement:

"We will continuously improve our techniques for understanding the needs of our customers and fulfilling their high value-added requirements. We will deliver quality products of superior performance. They will be supplied on time and at a fair price. By matching our capabilities and customer needs, we will best achieve our profit-growth objective."

It is this approach, carried out by dedicated personnel working in the most modern facilities, that makes the Unitrode difference — that makes it possible for us to offer the best in cost-performance integrated circuits.

This databook describes our current IC product lines. We welcome your inquiries about these devices, or about the development of new ones to meet your specific needs.

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Unitrode Corporation makes no representation that the use or interconnection of the circuits described herein will not infringe on existing or future patent rights, nor do the descriptions contained herein imply the granting of licenses to make, use or sell equipment constructed in accordance therewith.

NOTE: The information presented in this section is believed to be accurate and reliable. However, no responsibility is assumed by Unitrode Corporation for its use.

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6-8	UCOP02BJ	High Speed Op-Amp; Ceramic Dip
6-8	UCOP02CN	High Speed Op-Amp; Plastic Dip
6-8	UCOP02DN	High Speed Op-Amp; Plastic Dip
6-8	UCOP02EN	High Speed Op-Amp; Plastic Dip

* Contact Unitrode

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GENERAL INFORMATION

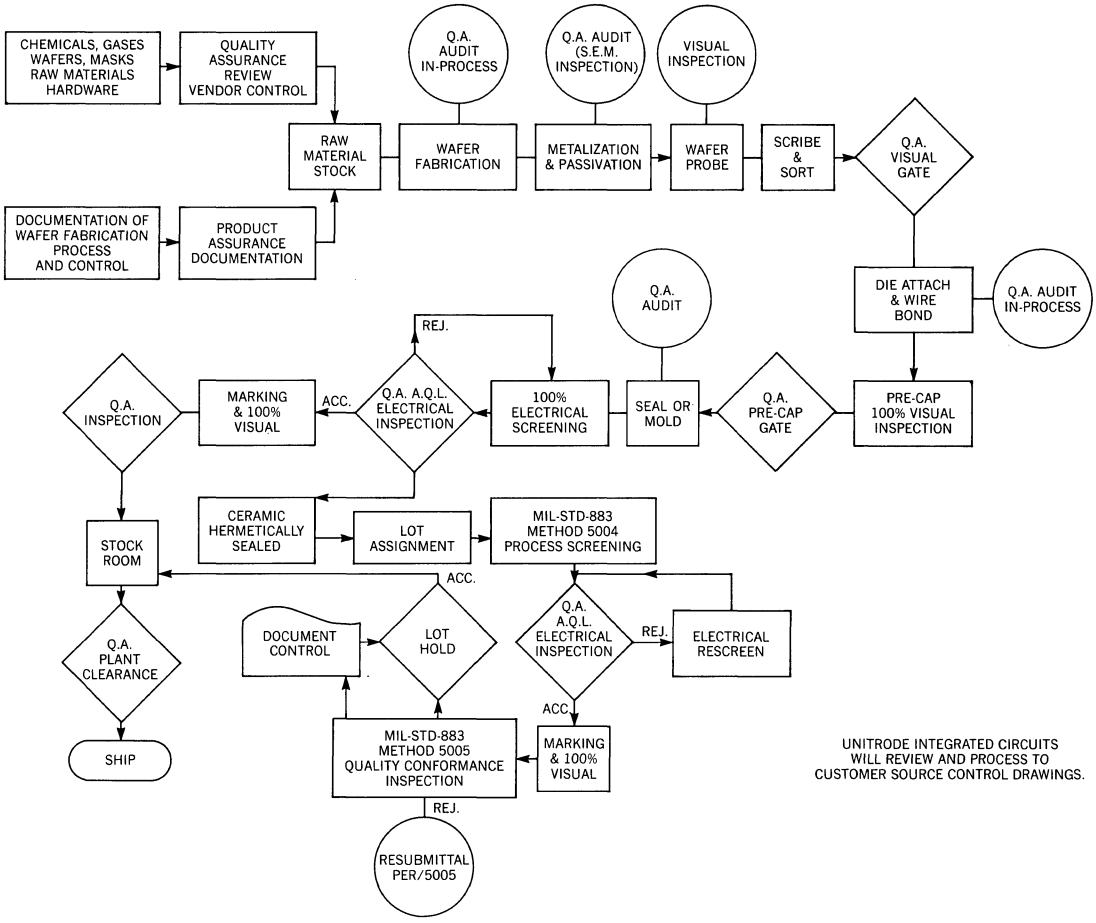
QUALITY STATEMENT

To become the recognized leader in the areas of quality and reliability, Unitrode Integrated Circuits Corporation has established and will continue to maintain high standards of design and workmanship that equal or surpass those sustained within our industry.

Further, it is our intent to consistently demonstrate quality conformance through professional leadership, technological commitment, and dedicated human resource.

To this end, Unitrode Integrated Circuits will continue to assure ongoing customer satisfaction.

UNITRODE INTEGRATED CIRCUITS PROCESS FLOW



UNITRODE INTEGRATED CIRCUITS WILL REVIEW AND PROCESS TO CUSTOMER SOURCE CONTROL DRAWINGS.

UNITRODE ASSEMBLY PACKAGE CODE	ASSEMBLY LOCATION CLASS B PRODUCT
K	Korea
B	Thailand
P	Philippines — S.D.P.I.
T	Philippines — Telefunken
I	U.S.A. — Indy
P	Singapore

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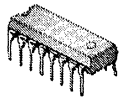
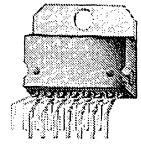
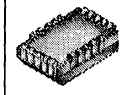
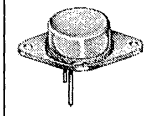
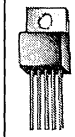
GENERAL INFORMATION

PACKAGE CROSS REFERENCE

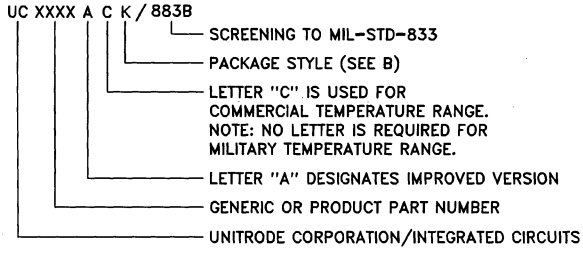
2

	 PLASTIC DIP	 CERAMIC DIP	 MULTIWATT®	 PLCC	 LCC	 SOIC	 TO-3	 TO-220
UNITRODE	N	J	V	Q	L	D	K	T
Linear Tech	N, N8	J, J8	—	—	L	5, 58	K	T
Integrated Power	N	J, L	—	—	L	D	K	T
SGS	B, N, P	—	V	—	—	—	K	—
Silicon General	M, N	J, Y	—	—	L	—	K	P
Texas Instruments	P, N	J, JG	—	FN	FC	D, DW	K	KC
Signetics	N	F	—	—	—	D	—	U
National	N	J	—	—	—	—	K, KC	T
Motorola	P	U	—	FN	—	D	K, KC	T
Fairchild	T, P	D, R	—	—	L	—	K	U
Sprague	A, M, B	R	—	E	—	L	V	T

GENERAL INFORMATION

ORDERING INFORMATION

A. PART NUMBER DESIGNATORS



0022-1

B. PACKAGE SUFFIXES

LETTER DESIGNATOR	PACKAGE TYPE
N	—Plastic Molded DIP
J	—Glass-Sealed Ceramic DIP
S	—Side-Braized Ceramic DIP
D	—SO Surface Mount
L	—Ceramic Leadless Chip Carrier
Q	—Plastic Molded Quad PLCC
V	—Multiwatt® Vertical Mount
VH	—Multiwatt® Horizontal Mount
H	—TO-5 Metal Can
K	—TO-3 Steel-Base Power
T	—TO-220 Plastic Power
P	—Ceramic Power

JAN Part Numbering System

J	M38510/	117	04	B	Y	C
JAN Designator Cannot be marked with "J" unless qualified on Part I or Part II of the QPL	**General Procurement Spec**	**Refers to Detail Spec** 101 Op Amps 102 Voltage Regulators 103 Comparators 104 Interface 105 733 106 Voltage Followers 107 Positive Fixed Voltage Regulators 108 Transistor Arrays 109 Timers 110 Quad Op Amps 112 Voltage Comparator 113 D to A Converter 114 Bi-Fet Op Amps 115 Negative Fixed Voltage Regulators 117 Positive Adjustable Voltage Regulators 118 Negative Adjustable Voltage Regulators 119 Bi-Fet Op Amps	**Defines Device Type**	**Processing Level** S B C	**Package Type** A 14-lead 1/4 × 1/4 Flatpak B 14-lead 1/4 × 1/8 Flatpak C 14-lead 1/4 × 3/4 Dip D 14-lead 1/4 × 3/8 Flatpak E 16-lead 1/4 × 7/8 Dip F 16-lead 1/4 × 3/8 Flatpak G 8-lead Can H 10-lead 1/4 × 1/4 Flatpak I 10-lead Can' J 24-lead 1/2 × 1 1/4 Dip K 24-lead 3/8 × 5/8 Flatpak P 8-lead 1/4 × 3/8 Dip X 3-lead Can Y 2-lead TO-3 Can Z 24-lead 1/4 × 3/8 Flatpak	**Lead Finish** A Hot Solder Dip B Tin Plate C Gold Plate X Any Finish

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POWER SUPPLY CIRCUITS

Switching Regulator Control ICs

Note: Most series available screened to /883B Rev. C.

TYPE	Voltage Reference ±4%	Voltage Reference ±1%	Soft Start	PWM Latch	Under-Voltage Lockout	Pulse-by-Pulse Current Limiting	Shutdown Terminal	Output Current	Feed Forward	Maximum Frequency Oscillator	Dual Outputs	Single-Ended Output	Totem Pole Outputs	Separate Oscillator Sync Terminal	Adjustable Deadtime Control	Latch Off or Continuous Retry Mode	Double Pulse Suppression	Low Current Start Up	Package
Regulating PWMs UC1524/2524/3524	X						X	100mA		300kHz	X								16 Pin DIP
Advanced Regulating PWMs UC1524A/2524A/3524A		X		X	X	X	X	200mA		500kHz	X						X		16 Pin DIP
Advanced Regulating PWMs UC1525A/2525A/3525A UC1527A/2527A/3527A		X	X	X	X		X	100mA 0.4A Pulse		500kHz			X	X	X				16 Pin DIP
Regulating PWM UC1526/2526/3526		X	X	X	X	X	X	100mA		400kHz			X	X	X		X		18 Pin DIP
Advanced Regulating PWMs UC1526A/2526A/3526A		X	X	X	X	X	X	100mA		550kHz			X	X	X		X		18 Pin DIP
Regulating PWMs UC493/UC494/	X							200mA		300kHz	X				X		X		16 Pin DIP
UC495																			18 Pin DIP
Advanced Regulating PWMs UC493A/UC493AC UC494A/UC494AC		X			X			200mA		300kHz	X				X		X		16 Pin DIP
UC495A/UC495AC UC495B/UC495BC																			18 Pin DIP
Current Mode PWM Controllers UC1846/2846/3846 UC1847/2847/3847		X	X	X	X	X	X	200mA	X	500kHz			X	X	X	X	X		16 Pin DIP
Programmable Primary Side PWMs UC1840/2840/3840		X	X	X	X	X	X	200mA	X	500kHz		X			X	X	N/A	X	18 Pin DIP
Programmable Primary Side PWMs UC1841/2841/3841		X	X	X	X	X	X	200mA	X	500kHz		X			X	X	N/A	X	18 Pin DIP
Economy Primary Side PWMs UC1842/2842/3842 UC1843/2843/3843 UC1844/2844/3844 UC1845/2845/3845		X		X	X	X		100mA 1A Pulse	X	500kHz		X			X		N/A	X	8 Pin DIP
High Frequency PWM Controllers UC1823/2823/3823		X	X	X	X	X		500mA 1.5A Pulse	X	2MHz		X	X	X	X		X	X	16 Pin DIP
UC1825/2825/3825		X	X	X	X	X					X		X	X	X		X	X	
Power Supply Control System UC2850/3850	X		X	X	X	X	X	50mA		200kHz	X			X	X		X		24 Pin DIP
High Current Buck Regulator L296		X	X	X		X	X	4A		200kHz		X					X		15 Pin Multiwatt®
Resonant Mode Controller UC1860/2860/3860		X	X		X		X	1.5A		3MHz	X		X	X	X	X	X		24 Pin DIP

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Power Supply Support Functions

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC1543/2543/3543 UC1544/2544/3544	Power Supply Supervisory Circuit, Monitors and Controls Power Supply Output	• Over/Under-Voltage, and Current Sensing Circuits • Programmable Time Delays • SCR "Crowbar" Drive of 300mA • Optional Over-Voltage Latch • Internal 1% Accurate Reference • Remote Activation Capability • Uncommitted Comparator • Inputs for Low Voltage Sensing (UC1544 Series only)	16 Pin DIL (1543 Series) 18 Pin DIL (1544 Series)
UC1705/2705/3705 UC1706/2706/3706 UC1707/2707/3707	See Power Driver & Interface Circuit Section		
UC1834/2834/3834	High Efficency Linear Regulator, Low Input-Output Differential	• Minimum V_{IN}—V_{OUT} less than 0.5V at 5A Load with External Pass Device • Equally Usable for either Positive or Negative Regulator Design • Adjustable Low Threshold Current Sense Amplifier • Under- and Over-Voltage Fault Alert with Programmable Delay • Over-Voltage Fault Latch with 100mA Crowbar Drive Output	16 Pin DIL
UC1835/2835/3835 UC1836/2836/3836	High Efficiency Regulator Controllers 5V Fixed (1835 Series) Adjustable (1836 Series)	• Complete Control for High Current Low Dropout Linear Regulator • Accurate 2.5A Current Limiting with Foldback • Internal Current Sense • External Shutdown	8 Pin DIL
UC1838/2838/3838	Magnetic Amplifier Controller	• Independent 1% Reference • Two Uncommitted, Identical Op Amps • 100mA Reset Current Source	16 Pin DIL Power Pkg.
UC1901/2901/3901	Isolated Feedback Generator Stable and Reliable Alternative to an Optical Coupler	• An Amplitude-Modulation System for Transformer Coupling an Isolated Feedback Error Signal • Internal 1% Reference and Error Amplifier • Loop Status Monitor • Low-Cost Alternative to Optical Couplers • Internal Carrier Oscillator Usable to 5MHz • Modulator Synchronizable to an External Clock	14 Pin DIL
UC1903/2903/3903	Quad Supply and Line Monitor Precision System	• Monitor Four Power Supply Output Voltage Levels • Both Over- and Under-Voltage Indicators • Internal Inverter for Negative Level Sense • Adjustable Fault Window • Additional Input for Early Line Fault Sense • On Chip, High-Current General Purpose OP-AMP	18 Pin DIL

Product Applications Circuits

PRODUCT SERIES	TYPICAL APPLICATIONS
UC1611/2611/3611 Quad Schottky Array	• Matched, Four Diode Monolithic Array • High Peak Current • Low Cost MINIDIP Package • Low Forward Voltage • Parallelable for Lower V_F or Higher V_F • Fast Recovery Time • Military Temperature Range
UC1704/3704 Bridge Transducer Switch	Any Analog to Digital monitoring system; coupled with any of a wide range of sensors almost any type of physical phenomena may be monitored. Samples: • Air-Flow Sensor Circuits • Liquid or Gas Flow Circuits • Passing Object Circuits
UC1906/2906 Lead-Acid Battery Charger	"IC Circuitry that results in optimized charge cycles for specific battery applications." • Uninterruptable Power Supplies • Portable Electrical Equipment • Emergency Power and Light Systems • Volatile Data Handling Computers—Power Back-Up
UC1730/2730/3730 Temperature and Air Flow Sensor	By combining a temperature monitor and heater, this IC permits airflow velocity past the IC package to be monitored. • On-Chip Temperature Transducer • Temperature Comparator Gives Thresold Temp-Airflow Alarm • Low 2.5mA Quiescent Current

POWER SUPPLY CIRCUITS

3 Terminal Fixed and Adjustable Regulators

Three Terminal Voltage Regulators, Adjustable

TYPE	OUTPUT CURRENT (A)	POLARITY	REGULATED OUTPUT VOLTAGE (V)	PACKAGE
†*UC117K/LM117K				TO-3
UC217K/LM217K	1.5A	Pos.	Adjustable from 1.2V to 37V	TO-3
UC317K/LM317K	1.5A	Neg.		TO-3
*UC137K/LM137K				TO-3
UC237K/LM237K	1.5A	Neg.	Adjustable from −1.2V to −37V	TO-3
UC337K/LM337K				TO-3
*UC150K/LM150K				TO-3
UC250K/LM250K	3.0A	Pos.	Adjustable from 1.2V to 33V	TO-3
UC350K/LM350K				TO-3

Three Terminal Voltage Regulators, Fixed, Positive

TYPE	OUTPUT CURRENT (A)	POLARITY	REGULATED INPUT VOLTAGE (V)			PACKAGE
*UC7800AK/LM140AK SERIES	1.5A	Pos.	5V ± 1%	12V ± 1%	15V ± 1%	TO-3
UC7800ACK/LM340AK SERIES						TO-3
*UC7800K/LM140K SERIES	1.5A	Pos.	5V ± 4%	12V ± 4%	15V ± 4%	TO-3
UC7800CK/LM340K SERIES						TO-3

Three Terminal Voltage Regulators, Fixed, Negative

TYPE	OUTPUT CURRENT (A)	POLARITY	REGULATED INPUT VOLTAGE (V)			PACKAGE
*UC7900AK/LM120K SERIES	1.5A	Neg.	−5V ± 1%	−12V ± 1%	−15V ± 1%	TO-3
UC7900ACK SERIES						TO-3
*UC7900K SERIES	1.5A	Neg.	−5V ± 4%	−12V ± 4%	−15V ± 4%	TO-3
UC7900CK/LM320K SERIES						TO-3

*All TO-3 Fixed and Adjustable Regulators available in /883B screened versions.

PACKAGE NOTE: Both Plastic or Ceramic Surface Mount Packaging are available. Contact factory for details.

† Available in /38510 version. Contact factory for details.

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LINEAR INTEGRATED CIRCUITS

High Current Switching Regulator

FEATURES

- 4A Output Current
- 5.1V to 40V Output Voltage Range
- 0 to 100% Duty Cycle Range
- Precise (±2%) On-Chip Reference
- Switching Frequency up to 200KHz
- Very High Efficiency (Up to 90%)
- Very Few External Components
- Soft Start
- Reset Output
- Control Circuit for Crowbar SCR
- Input for Remote Inhibit and Synchronous PWM
- Thermal Shutdown

DESCRIPTION

The L296 is a stepdown power switching regulator delivering 4A at voltages from 5.1V to 40V. The device features programmable current limiting, remote inhibit, soft start, thermal protection, reset output for microprocessors, and a PWM comparator input for synchronization in multichip configurations. The L296 is offered in a 15-lead Multiwatt® plastic power package and requires very few external components. Efficient operation at switching frequencies up to 200KHz allows reduction, in size and cost, of external filter components. A voltage sense input and SCR drive output are provided for optical crowbar over-voltage protection with an external SCR.

ABSOLUTE MAXIMUM RATINGS

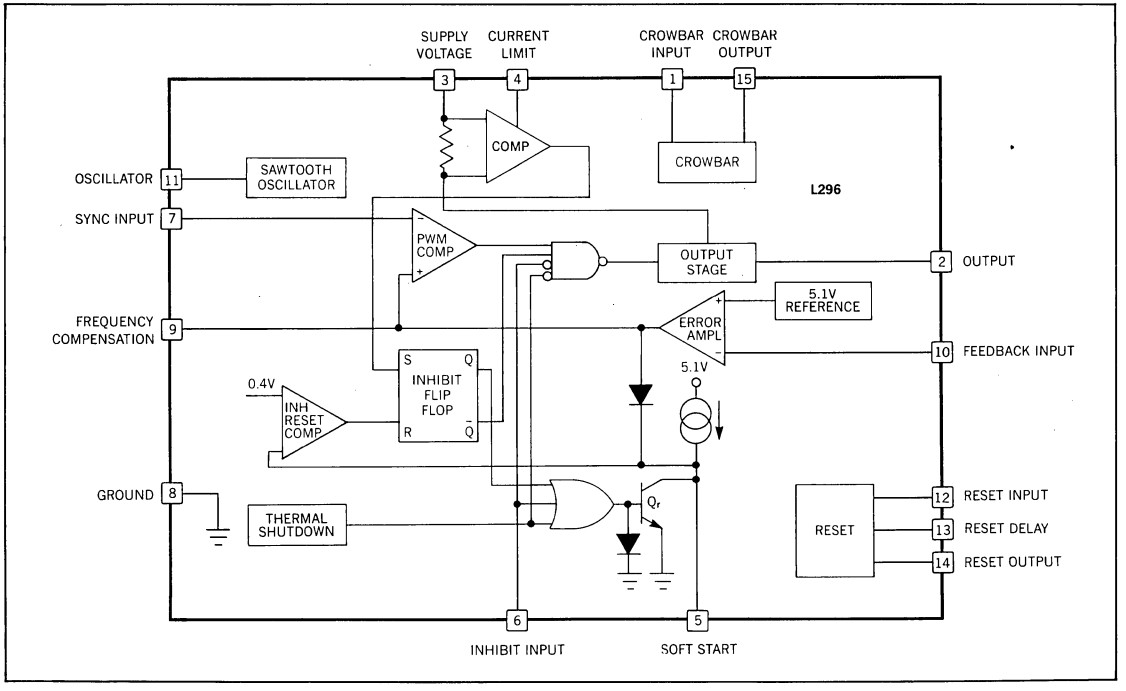
Supply Voltage, V_3 ..... 50V
Input to Output Voltage Difference, $V_3 - V_2$ 50V
Output DC Voltage, V_2 ..... −1V
Output Peak Voltage at t = 0.1μsec, f = 200KHz ..... −7V
Voltage at Pins 1 and 12, V_1, V_{12} 10V
Voltage at Pins 6 and 15, V_6, V_{15} 15V
Voltage at Pins 4, 5, 7 and 9, V_4, V_5, V_7, V_9 ..... 5.5V
Voltage at Pins 10 and 6, V_{10}, V_6 ..... 7V
Voltage at Pin 14 ($I_{14} \leq 1mA$), V_{14} ..... V_3
Pin 9 Sink Current, I_9 ..... 1mA
Pin 11 Source Current, I_{11} ..... −20mA
Pin 14 Sink Current ($V_{14} < 5V$), I_{14} 50mA
Power Dissipation at $T_{case} \leq 90°C$, P_{tot} 20W
Junction and Storage Temperature, T_j, T_{stg} .. −40°C to +150°C

THERMAL DATA

Thermal Resistance Junction-Case, θ_{JC} ..... 3°C/W max.
Thermal Resistance Junction-Ambient, θ_{JA} ..... 35°C/W max.

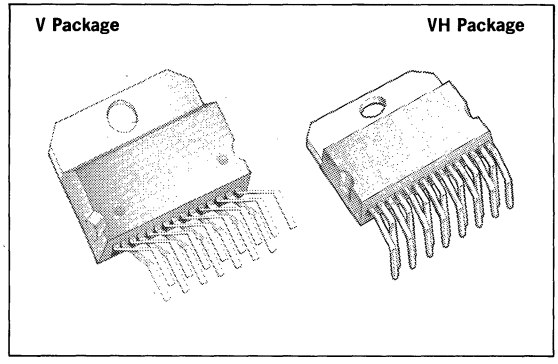
Note: Currents into the device (sink) are positive value. Currents out of the device (source) are negative value.

BLOCK DIAGRAM

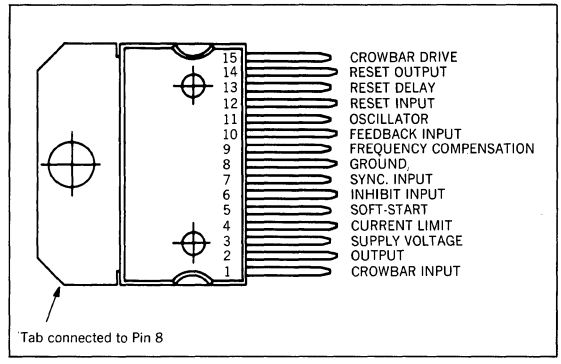


UNITRODE

LEAD FORM OPTIONS



CONNECTION DIAGRAM (TOP VIEW)



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_j = 25°C, V_3 = 35V, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
Dynamic Characteristics (Pin 6 to GND unless otherwise specified)							
Output Voltage Range	V_o	V_3 = 46V, I_o = −1A		V_{REF}		40	V
Supply Voltage Range	V_3	V_o = V_{REF} to 36V, I_o = −4A		9		46	V
Line Regulation	ΔV_o	V_3 = 10V to 40V, V_o = V_{REF}, I_o = −2A			15	50	mV
Load Regulation	ΔV_o	V_o = V_{REF}	I_o = −2A to −4A		10	30	mV
			I_o = −0.5A to −4A		15	45	
Internal Reference Voltage (Pin 10)	V_{REF}	V_3 = 9V to 46V, I_o = −2A		5	5.1	5.2	V
Average Temperature Coefficient of Reference Voltage*	$\frac{\Delta V_{REF}}{\Delta T}$	T_j = 0°C to 125°C, I_o = −2A			0.4		mV/°C
Dropout Voltage (Between Pin 2 and Pin 3)	V_d	I_o = −4A			2	3.2	V
		I_o = −2A			1.3	2.1	V
Maximum Operating Load Current	I_{om}	V_3 = 9V to 46V, V_o = V_{REF} to 36V		−4			A
Current Limiting Threshold (Pin 2)	I_{2L}	V_3 = 9V to 46V, V_o = V_{REF} to 40V	Pin 4 Open			−8	A
			R_{lim} = 33KΩ		−2.5		A
Input Average Current	I_{SH}	V_3 = 46V, Output Short-Circuited			60	100	mA
Efficiency	η	I_o = −3A	V_o = V_{REF}		75		%
			V_o = 12V		85		%
Supply Voltage Ripple Rejection	SVRR	ΔV_3 = $2V_{rms}$, f_{ripple} = 120Hz, V_o = V_{REF}, I_o = −2A		50	56		dB
Switching Frequency	f			85	100	115	KHz
Voltage Stability of Switching Frequency		V_3 = 9V to 46V			0.5		%
Temperature Stability of Switching Frequency*		T_j = 0°C to 125°C			1		%
Maximum Operating Switching Frequency	f_{max}	V_o = V_{REF}, I_o = −1A, R = 1.75KΩ, C = 2.2nF		200			KHz
Thermal Shutdown Junction Temperature*	T_{jsd}			135	150		°C

* Guaranteed by design; not 100% tested.

ELECTRICAL CHARACTERISTICS(Refer to the test circuit, T_j = 25°C, V_3 = 35V, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
DC Characteristics							
Quiescent Drain Current	I_{3Q}	V_3 = 46V, V_7 = 0V, V_{10} = 0V, Pin 11: Open	V_6 = 0V		66	85	mA
			V_6 = 3V		30	40	
Output Leakage Current	I_{2L}		V_6 = 3V			−2	mA
Soft Start							
Source Current	I_5	V_6 = 0V, V_5 = 3V		−100	−130	−160	μA
Sink Current	I_5	V_6 = 3V, V_5 = 3V		50	70	120	μA
Inhibit							
Low Input Voltage	V_{6L}	V_3 = 9V to 46V, V_7 = 0V, V_{10} = 0V, Pins 2, 11: Open		−0.3		0.8	V
High Input Voltage	V_{6H}			2		5.5	V
Input Current with Low Input Voltage	I_{6L}		V_6 = 0.8V			−10	μA
Input Current with High Input Voltage	I_{6H}		V_6 = 2V			−3	μA
Error Amplifier							
High Level Output Voltage	V_{9H}	$V_{10} = V_{REF}$ − 400mV, I_9 = +100μA		3.5			V
Low Level Output Voltage	V_{9L}	$V_{10} = V_{REF}$ + 400mV, I_9 = −100μA				0.5	V
Sink Output Current	I_9	$V_{10} = V_{REF}$ + 400mV		100	150		μA
Source Output Current	I_9	$V_{10} = V_{REF}$ − 400mV		−100	−150		μA
Input Bias Current	I_{10}	V_{10} = 5.2V			2	10	μA
DC Open Loop Gain	G_V	V_9 = 1V to 3V		46	55		dB
Oscillator and PWM Comparator							
Input Bias Current of PWM Comparator	I_7	V_7 = 0.5V to 3.5V				−5	μA
Oscillator Source Current	I_{11}	V_{11} = 2V, Pin 2: Open		−5			mA
Reset							
Rising Threshold Voltage	V_{12R}	V_3 = 9V to 46V, I_{14} = 16mA, Pin 13: Open		V_{REF} −150mV	V_{REF} −100mV	V_{REF} −50mV	V
Falling Threshold Voltage	V_{12F}			4.75	V_{REF} −150mV	V_{REF} −100mV	V
Delay Threshold Voltage	V_{13D}	V_{12} = 5.3V, I_{14} = 16mA		4.3	4.5	4.7	V
Delay Threshold Voltage Hysteresis	V_{13H}	V_{12} = 5.3V, I_{14} = 16mA			100		mV
Output Saturation Voltage	V_{14S}	I_{14} = 16mA, V_{12} = 4.7V, Pin 13: Open				0.4	V
Input Bias Current	I_{12}	V_{12} = 0V to V_{REF}, I_{14} = 16mA, Pin 13: Open			1	3	μA
Delay Source Current	I_{13}	V_{13} = 3V, I_{14} = 16mA, V_{12} = 5.3V		−70	−110	−140	μA
Delay Sink Current	I_{13}	V_{13} = 3V, I_{14} = 16mA, V_{12} = 4.7V		10			mA
Output Leakage Current	I_{14}	V_3 = 46V, V_{12} = 5.3V, Pin 13: Open				+100	μA
Crowbar							
Input Threshold Voltage	V_1	V_{15} = 2V		5.5	6	6.4	V
Output Saturation Voltage	V_{15}	V_3 = 9V to 46V, V_1 = 5.4V, I_{15} = 5mA			0.2	0.4	V
Input Bias Current	I_1	V_1 = 6V, V_{15} = 2V				10	μA
Output Source Current	I_{15}	V_3 = 9V to 46V, V_1 = 6.5V, V_{15} = 2V		−70	−100		mA

* Guaranteed by design; not 100% tested.

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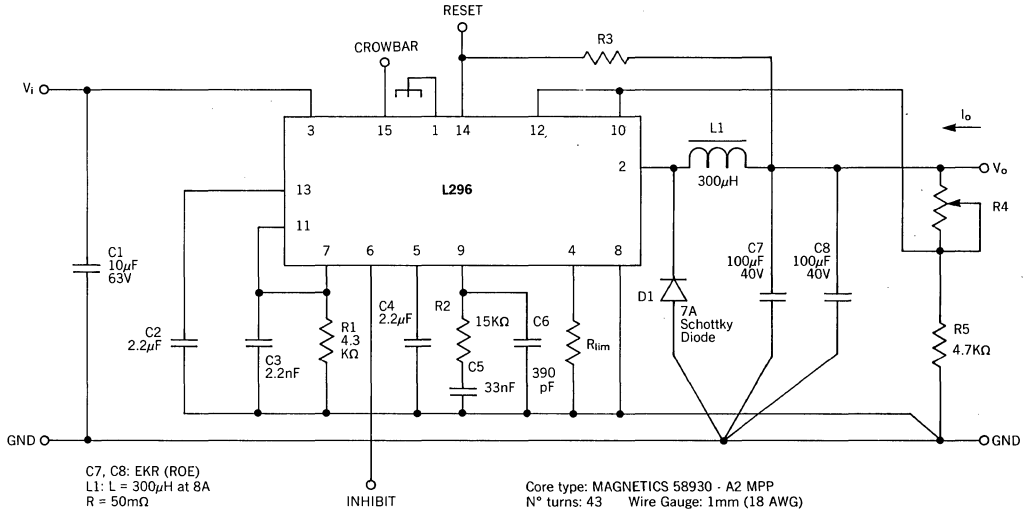
DYNAMIC TEST CIRCUIT



APPLICATION INFORMATION

Choosing the Inductor and Capacitor

The input and output capacitors of the L296 must have a low ESR and low inductance at high current ripple.

Saturation must not occur at current levels below 1.5 times the current limiter level.

$$L = \frac{(V_3 - V_o)\, V_o}{V_3\, f\, \Delta I_L}$$

$$C = \frac{(V_3 - V_o)\, V_o}{8L\, f^2\, \Delta V_o}$$

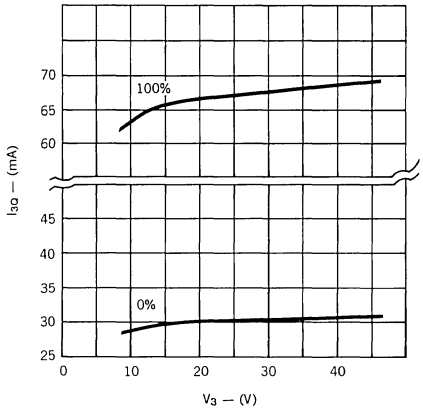
f = frequency

ΔI_L = Inductance current ripple

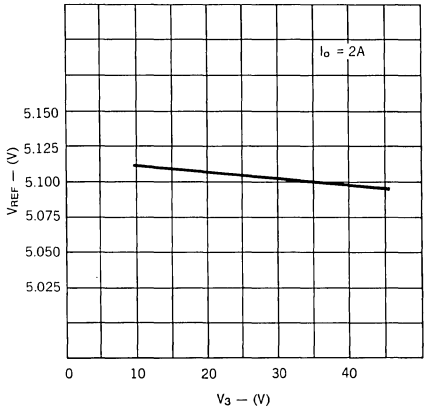
ΔV_O = Output ripple voltage

Resistor Values for Standard Output Voltages		
V_o	R_5	R_4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

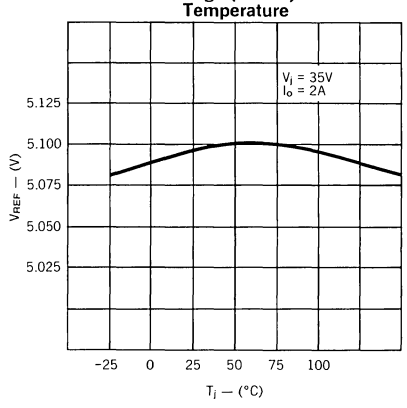
Quiescent Drain Current vs Supply Voltage (0% + 100% Duty Cycle)



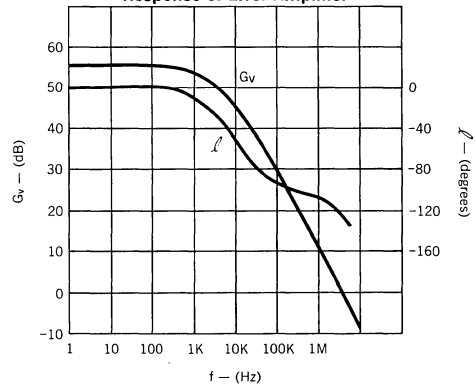
Reference Voltage (Pin 10) vs V_i



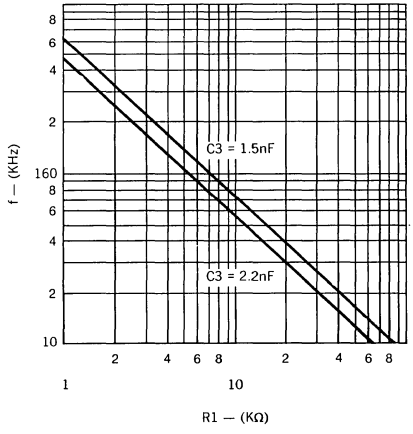
Reference Voltage (Pin 10) vs Junction Temperature



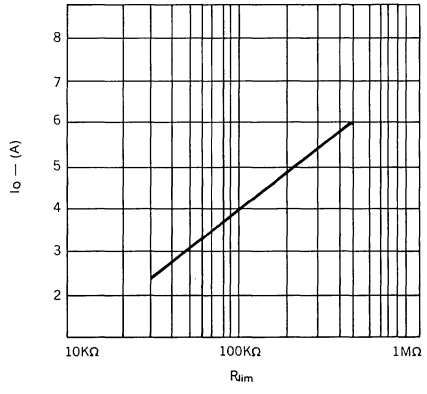
Open Loop Frequency and Phase Response of Error Amplifier



Switching Frequency vs R1



Maximum C/L Thresholds



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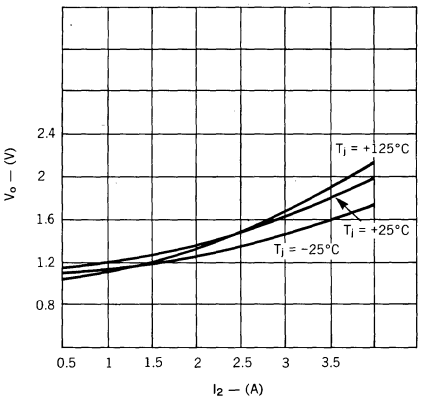
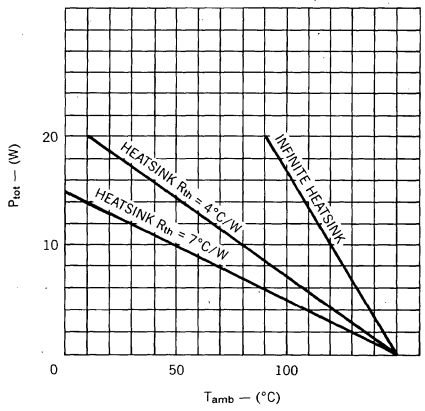
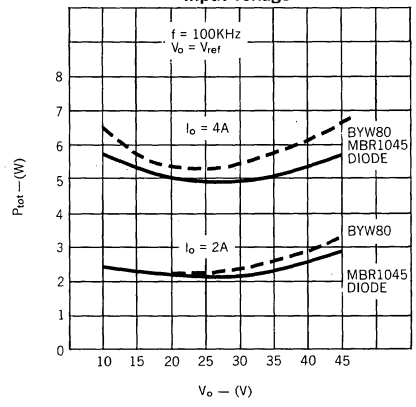
Dropout Voltage Between Pin 3 and Pin 2 vs Current at Pin 2



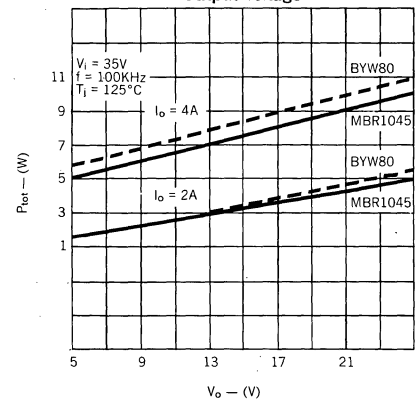
Power Dissipation Derating Curve



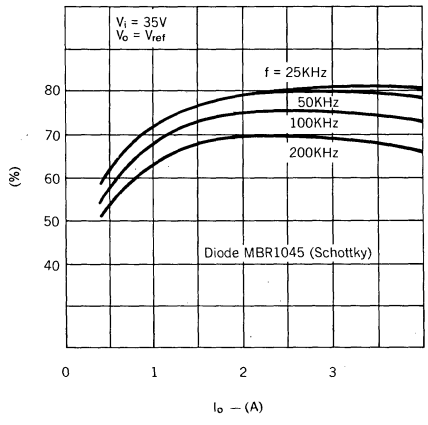
Power Dissipation (L296 only) vs Input Voltage



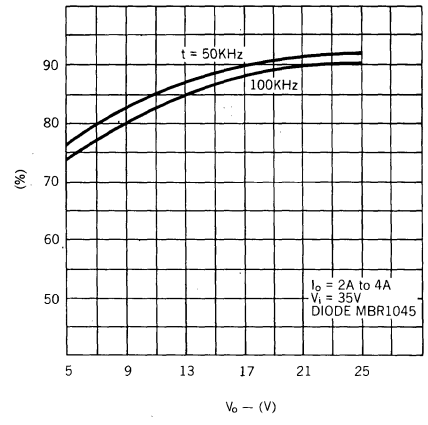
Power Dissipation (L296 only) vs Output Voltage



Efficiency vs Output Current



Efficiency vs Output Current



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CIRCUIT OPERATION

Figure 1. Reset Output Waveforms

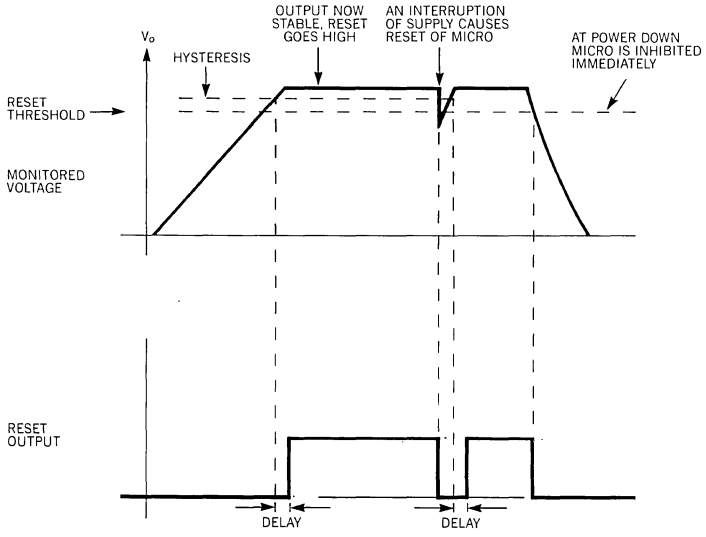


Figure 2. Soft Start Waveforms

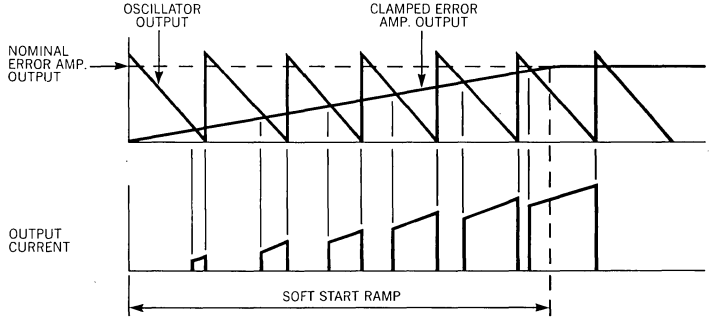
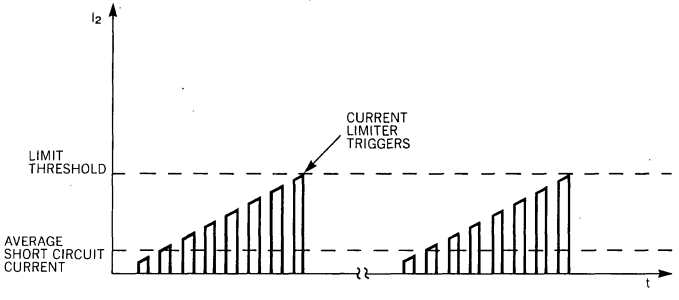


Figure 3. Current Limiter Waveforms



CIRCUIT OPERATION (continued)
(refer to the block diagram)

The L296 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 4A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (trimmed to ±2%). This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage. The gain and frequency stability of the loop can be adjusted by an external RC network connected to Pin 9. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source.

Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V. The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network.

The reset circuit generates an output signal when the supply voltage exceeds a threshold programmed by an external divider. The reset signal is generated with a delay time programmed by an external capacitor. When the supply falls below the threshold the reset output goes low immediately. The reset output is an open collector.

The crowbar circuit senses the output voltage and the crowbar output can provide a current of 100mA to switch on an external SCR. This SCR is triggered when the output voltage exceeds the nominal by 20%. There is no internal connection between the output and crowbar sense input; therefore the crowbar can monitor either the input or the output.

PIN FUNCTIONS

NO.	NAME	FUNCTION
1.	CROWBAR INPUT	Voltage sense input for crowbar over-voltage protection. Normally connected to the feedback input thus triggering the SCR when V_{OUT} exceeds nominal by 20%. May also monitor the input and a voltage divider can be added to increase the threshold. Connected to ground when SCR not used.
2.	OUTPUT	Regulator output.
3.	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the L296's internal logic.
4.	CURRENT LIMIT	A resistor connected between this terminal and ground sets the current limiter threshold. If this terminal is left unconnected the threshold is internally set (see electrical characteristics).
5.	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
6.	INHIBIT INPUT	TTL - level remote inhibit. A logic high level on this input disables the L296.
7.	SYNC INPUT	Multiple L296s are synchronized by connecting the Pin 7 inputs together and omitting the oscillator RC network on all but one device.
8.	GROUND	Common ground terminal.
9.	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
10.	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
11.	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. This pin must be connected to Pin 7 input when the internal oscillator is used.
12.	RESET INPUT	Input of the reset circuit. The threshold is roughly 5V. It may be connected to the feedback point or via a divider to the input.
13.	RESET DELAY	A capacitor connected between this terminal and ground determines the reset signal delay time.
14.	RESET OUTPUT	Open collector reset signal output. This output is high when the supply is safe.
15.	CROWBAR OUTPUT	SCR gate drive output of the crowbar circuit.

A TTL - level inhibit input is provided for applications such as remote on/off control. This input is activated by high logic level and disables circuit operation. After an inhibit the L296 restarts under control of the soft start network.

The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

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LINEAR INTEGRATED CIRCUITS

1.5A, Three Terminal Adjustable Positive Voltage Regulators

UC117
UC217
UC317

3

FEATURES

- Output voltage adjustable from 1.2 to 37V
- Guaranteed 1.5A output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Temperature-independent current limit
- Standard 3-lead transistor packages (TO-3, TO-220)

DESCRIPTION

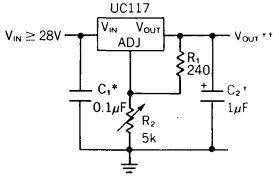
This monolithic integrated circuit is an adjustable 3-terminal positive voltage regulator designed to supply more than 1.5A of load current with an output voltage adjustable over a 1.2 to 37V range. Although ease of setting the output voltage to any desired value with only two external resistors is a major feature of this circuit, exceptional line and load regulation are also offered. In addition, full overload protection consisting of current limiting, thermal shutdown and safe-area control are included in this device which is packaged in TO-3 and TO-220 packages. The UC117 is rated for operation from −55°C to +150°C, the UC217 from −25°C to +150°C and the UC317 from 0°C to +125°C.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation ..... Internally limited
Input—Output Voltage Differential 40V
Operating Junction Temperature Range
UC117 ..... −55°C to +150°C
UC217 ..... −25°C to +150°C
UC317 ..... 0°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

TYPICAL APPLICATIONS

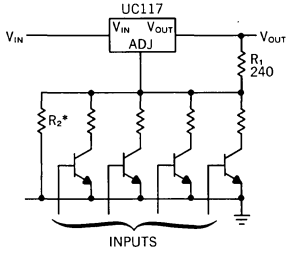
1.2V—25V Adjustable Regulator



*Needed if device is far from filter capacitors
†Optional—improves transient response

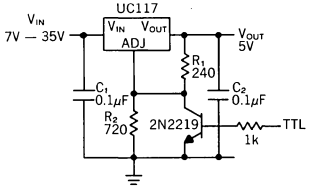
†† $V_{OUT} = 1.25V \left(1 + \frac{R_2}{R_1}\right)$

Digitally Selected Outputs



*Value determines maximum V_{OUT}

5V Logic Regulator with Electronic Shutdown*



*Min output ≃ 1.2V

UNITRODE

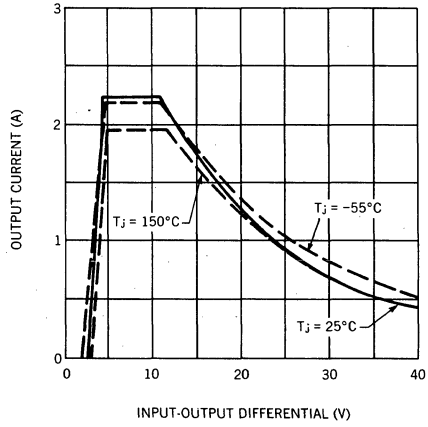
ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	TEST CONDITIONS	UC117/UC217			UC317			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Line Regulation	T_A = 25°C, 3V ≤ (V_{IN} − V_{OUT}) ≤ 40V, (Note 2)		0.01	0.02		0.01	0.04	%/V
Load Regulation	T_A = 25°C, 10mA ≤ I_{OUT} ≤ I_{MAX} V_{OUT} ≤15V, (Note 2) V_{OUT} ≥ 5V, (Note 2)		 5 0.1	 15 0.3		 5 0.1	 25 0.5	 mV %
Thermal Regulation	T_A = 25°C, 20ms Pulse		0.03	0.07		0.04	0.07	%/W
Adjustment Pin Current			50	100		50	100	μA
Adjustment Pin Current Change	10mA ≤ I_L ≤ I_{MAX} 2.5V ≤ (V_{IN} − V_{OUT}) ≤ 40V		0.2	5		0.2	5	μA
Reference Voltage	3 ≤ (V_{IN} − V_{OUT}) ≤ 40V 10mA ≤ I_{OUT} ≤ I_{MAX}, P ≤ P_{MAX}	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation	3 ≤ (V_{IN} − V_{OUT}) ≤ 40V, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	10mA ≤ I_{OUT} ≤ I_{MAX}, (Note 2) V_{OUT} ≤ 5V V_{OUT} ≥ 5V		 20 0.3	 50 1		 20 0.3	 70 1.5	 mV %
Temperature Stability	T_{MIN} ≤ T_j ≤ T_{MAX}		1			1		%
Minimum Load Current	V_{IN} − V_{OUT} = 40V		3.5	5		3.5	10	mA
Current Limit	(V_{IN} − V_{OUT}) ≤15V K Package T Package (V_{IN} − V_{OUT}) = 40V K Package T Package	 1.5 1.5 	 2.2 2.2 0.4 0.4	 	 1.5 1.5 	 2.2 2.2 0.4 0.4	 	 A A A A
RMS Output Noise	T_A = 25°C, 10Hz ≤ f ≤ 10kHz		0.003			0.003		%
Ripple Rejection Ratio	V_{OUT} = 10V, f = 120Hz C_{ADJ} = 10μF	 66	65 80	 	 66	65 80	 	dB dB
Long Term Stability	T_A = 125°C, 1000 Hrs.		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	K Package T Package		2.3	3		2.3 4	3	°C/W °C/W

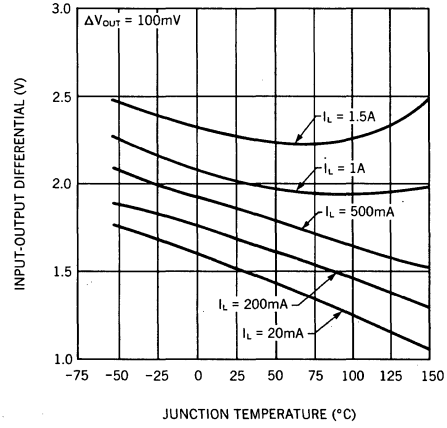
Notes: 1. Unless otherwise noted, the above specifications apply over the following conditions:
UC117: −55°C ≤ T_j ≤ 150°C
UC217: −25°C ≤ T_j ≤ 150°C
UC317: 0°C ≤ T_j ≤ 125°C
(V_{IN} − V_{OUT}) = 5V, I_O = 0.5A, I_{MAX} =1.5A
2. All regulation specifications are measured at constant junction temperatures using low duty-cycle pulse testing.

TYPICAL PERFORMANCE CHARACTERISTICS

Current Limit

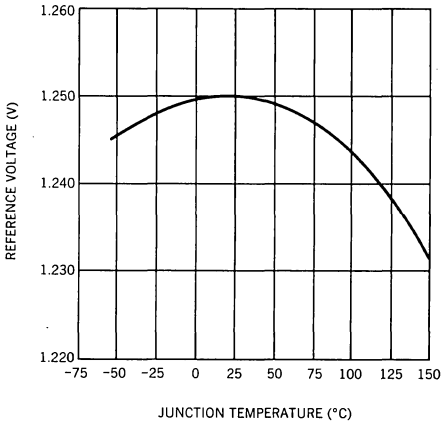


Dropout Voltage

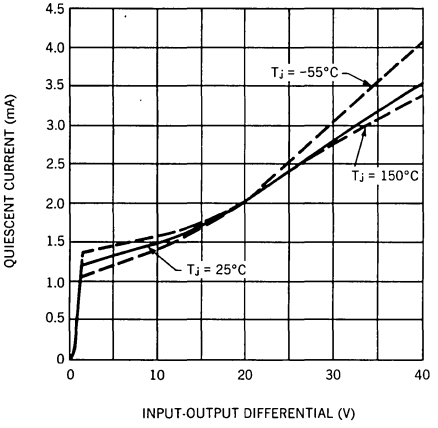


TYPICAL PERFORMANCE CHARACTERISTICS

Temperature Stability



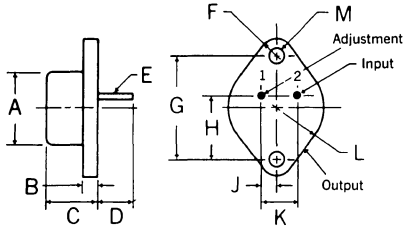
Minimum Operating Current



3

MECHANICAL SPECIFICATIONS AND CONNECTION DIAGRAMS

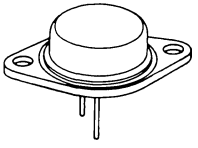
UC117 UC217 UC317



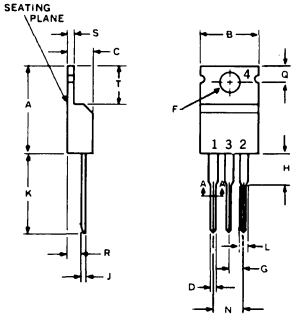
Bottom View

	INCHES	MILLIMETERS
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	.250-.450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	.188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655-.675	16.64-17.15
J	.205-.225	5.21-5.72
K	.420-.440	10.67-11.18
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.

TO-204AA K(TO-3)



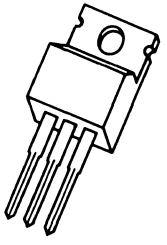
UC317



1-Adjustment
2-Input
3-Output
4-Output

	INCHES		MILIMETERS	
	MIN	MAX	MIN	MAX
A	0.560	0.625	14.23	15.87
B	0.380	0.420	9.66	10.66
C	0.140	0.190	3.56	4.82
D	0.020	0.045	.0.51	1.14
F	0.139	0.147	3.531	3.733
G	0.090	0.110	2.29	2.79
H	—	0.250	—	6.35
J	0.015	0.025	0.38	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.070	1.14	1.77
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.115	2.04	2.92
S	0.045	0.055	1.14	1.39
T	0.230	0.270	5.85	6.85

T(TO-220)



Note: When ordering, add suffix "K" (for TO-3 package) or "T" (for TO-220 package) to the Part Number.

APPLICATION HINTS

In operation, the UC117 develops a nominal 1.25V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R_1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R_2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}R_2$$

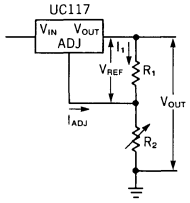


Figure 1

Since the 100μA current from the adjustment terminal represents an error term, the UC117 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

External Capacitors

An input bypass capacitor is recommended. A 0.1μF disc or 1μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the UC117 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10μF bypass capacitor 80 dB ripple rejection is obtainable at any output level.

In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25μF in aluminum electrolytic to equal 1μF solid tantalum at high frequencies.

Although the UC117 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500pF and 5000pF. A 1μF solid tantalum (or 25μF aluminum electrolytic) on the output swamps this effect and insures stability.

Load Regulation

The UC117 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation.

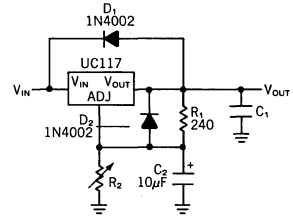
With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor by using 2 separate leads to the case. The ground of R_2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

Protection Diodes

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the UC117, this discharge path is through a large junction that is able to sustain 15A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25μF or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the UC117 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10μF capacitance. *Figure 2* shows a UC117 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.



$$V_{OUT} = 1.25V\left(1 + \frac{R_2}{R_1}\right) + R_2I_{ADJ}$$

D_1 protects against C_1
D_2 protects against C_2

Figure 2. Regulator with Protection Diodes

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LINEAR INTEGRATED CIRCUITS

1.5A, Three Terminal Adjustable Negative Voltage Regulators

UC137
UC237
UC337

3

FEATURES

- Output voltage adjustable from −1.2 to −37V
- Guaranteed 1.5A output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Excellent thermal regulation, 0.002%/W
- 77 dB ripple rejection
- Excellent rejection of thermal transients
- 50 ppm/°C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- Standard 3-lead transistor packages (TO-3, TO-220)

DESCRIPTION

The UC137/UC237/UC337 are adjustable 3-terminal negative voltage regulators capable of supplying in excess of −1.5A over an output voltage range of −1.2V to −37V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the UC137 series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

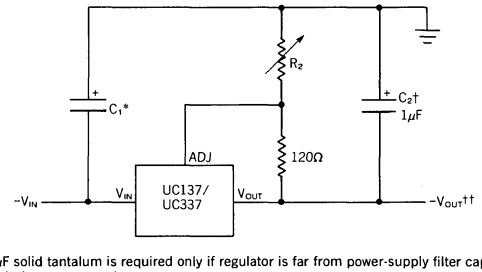
The UC137/UC237/UC337 serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The UC137/UC237/UC337 are ideal complements to the UC117/UC217/UC317 adjustable positive regulators. These devices are available in TO-3 and TO-220 packages. The UC137 is rated for operation from −55°C to +150°C, the UC237 from −25°C to +150°C and the UC337 from 0°C to +125°C.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation	Internally limited
Input—Output Voltage Differential	40V
Operating Junction Temperature Range	
UC137	−55°C to +150°C
UC237	−25°C to +150°C
UC337	0°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

TYPICAL APPLICATION

Adjustable Negative Voltage Regulator



*C_1 = 1μF solid tantalum is required only if regulator is far from power-supply filter capacitor.
†Optional—improves transient response
†† $-V_{OUT} = -1.25V\left(1 + \frac{R_2}{120\Omega}\right)$

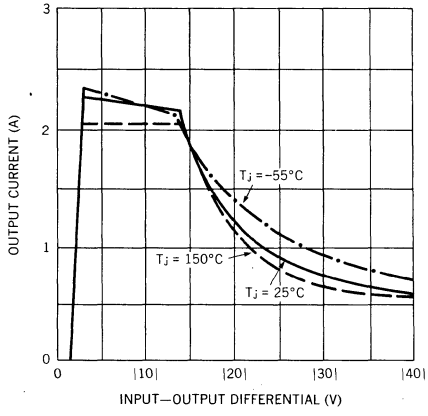
UNITRODE

ELECTRICAL CHARACTERISTICS (Note 1)

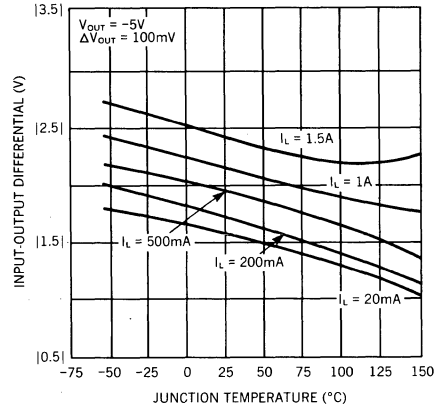
PARAMETER	TEST CONDITIONS	UC137/UC237			UC337			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Line Regulation	$T_A = 25°C$, $3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$ (Note 2)		0.01	0.02		0.01	0.04	%/V
Load Regulation	$T_A = 25°C$, $10mA \le I_{OUT} \le I_{MAX}$							
	$\lvert V_{OUT} \rvert \le 5V$, (Note 2)		15	25		15	50	mV
	$\lvert V_{OUT} \rvert \ge 5V$, (Note 2)		0.3	0.5		0.3	1.0	%
Thermal Regulation	$T_A = 25°C$, 10ms Pulse		0.002	0.02		0.003	0.04	%/W
Adjustment Pin Current			65	100		65	100	μA
Adjustment Pin Current Change	$10mA \le I_L \le I_{MAX}$		2	5		2	5	μA
	$2.5V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, $T_A = 25°C$							
Reference Voltage	$T_A = 25°C$							
	$3 \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$	-1.225	-1.250	-1.275	-1.213	-1.250	-1.287	V
	$10mA \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$	-1.200	-1.250	-1.300	-1.200	-1.250	-1.300	V
Line Regulation	$3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	$10mA \le I_{OUT} \le I_{MAX}$, (Note 2)							
	$\lvert V_{OUT} \rvert \le 5V$		20	50		20	70	mV
	$\lvert V_{OUT} \rvert \ge 5V$		0.3	1		0.3	1.5	%
Temperature Stability	$T_{MIN} \le T_j \le T_{MAX}$		0.6			0.6		%
Minimum Load Current	$\lvert V_{IN} - V_{OUT} \rvert \le 40V$		2.5	5		2.5	10	mA
	$\lvert V_{IN} - V_{OUT} \rvert \le 10V$		1.2	3		1.5	6	mA
Current Limit	$\lvert V_{IN} - V_{OUT} \rvert \le 15V$							
	K Package	1.5	2.2		1.5	2.2		A
	T Package	1.5	2.2		1.5	2.2		A
	$\lvert V_{IN} - V_{OUT} \rvert = 40V$							
	K Package		0.4			0.4		A
	T Package		0.4			0.4		A
RMS Output Noise	$T_A = 25°C$, $10Hz \le f \le 10kHz$		0.003			0.003		%
Ripple Rejection Ratio	$V_{OUT} = -10V$, f = 120Hz		60			60		dB
	$C_{ADJ} = 10\mu F$	66	77		66	77		dB
Long Term Stability	$T_A = 125°C$, 1000 Hours		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	K Package		2.3	3		2.3	3	°C/W
	T Package					4		°C/W

Notes: 1. Unless otherwise noted, the above specifications apply over the following conditions:
UC137: $-55°C \le T_j \le 150°C$
UC237: $-25°C \le T_j \le 150°C$
UC337: $0°C \le T_j \le 125°C$
$\lvert V_{IN} - V_{OUT} \rvert = 5V$, $I_O = 0.5A$, $I_{MAX} = 1.5A$
2. All regulation specifications are measured at constant junction temperatures using low duty-cycle pulse testing.

Current Limit



Dropout Voltage



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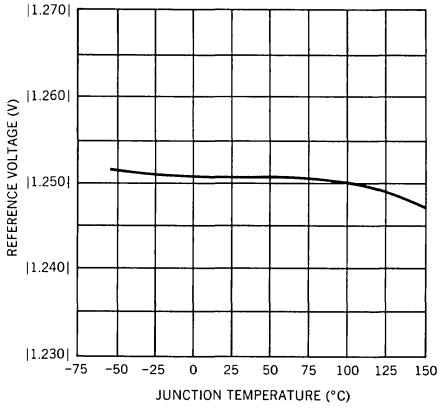
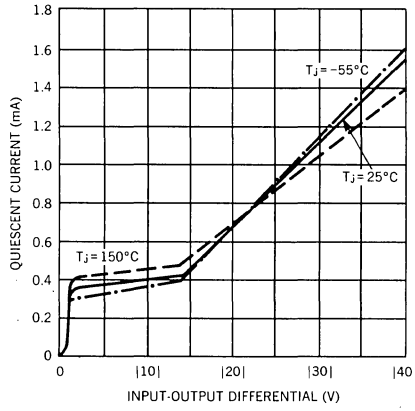
TYPICAL PERFORMANCE CHARACTERISTICS

Temperature Stability



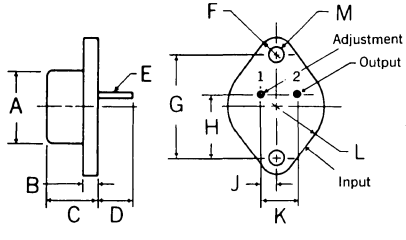
Minimum Operating Current



3

MECHANICAL SPECIFICATIONS AND CONNECTION DIAGRAMS

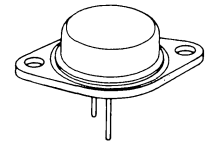
UC137 UC237 UC337



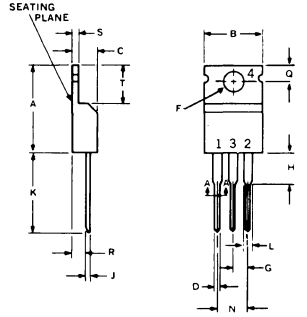
Bottom View

	INCHES	MILLIMETERS
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	.250-.450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	.188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655-.675	16.64-17.15
J	.205-.225	5.21-5.72
K	.420-.440	10.67-11.18
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.

TO-204AA K(TO-3)



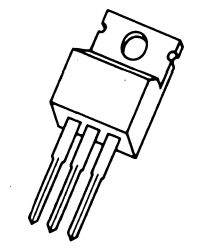
UC337



1-Adjustment
2-Output
3-Input
4-Input

	INCHES		MILIMETERS	
	MIN	MAX	MIN	MAX
A	0.560	0.625	14.23	15.87
B	0.380	0.420	9.66	10.66
C	0.140	0.190	3.56	4.82
D	0.020	0.045	0.51	1.14
F	0.139	0.147	3.531	3.733
G	0.090	0.110	2.29	2.79
H	—	0.250	—	6.35
J	0.015	0.025	0.38	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.070	1.14	1.77
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.115	2.04	2.92
S	0.045	0.055	1.14	1.39
T	0.230	0.270	5.85	6.85

T(TO-220)



Note: When ordering, add suffix "K" (for TO-3 package) or "T" (for TO-220 package) to the Part Number.

LINEAR INTEGRATED CIRCUITS

3A, Three Terminal Adjustable Positive Voltage Regulators

UC150
UC250
UC350

FEATURES

- Output voltage adjustable from 1.2V to 33V
- Guaranteed 3A output current
- Line regulation typically 0.005%/V
- Load regulation typically 0.1%
- Guaranteed thermal regulation
- Current limit constant with temperature
- Standard 3-lead transistor package

DESCRIPTION

The UC150/UC250/UC350 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 3A over a 1.2V to 33V output range. They require only 2 external resistors to set the output voltage. Further, both line and load regulation are comparable to discrete designs.

In addition to higher performance than fixed regulators, the UC150 series offers full overload protection. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is accidentally disconnected.

Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded.

Supplies requiring electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

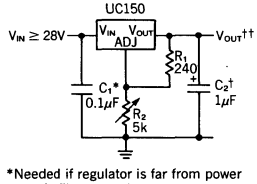
The UC150/UC250/UC350 are packaged in standard TO-3 transistor packages. The UC150 is rated for operation from −55°C to +150°C, the UC250 from −25°C to +150°C and the UC350 from 0°C to +125°C.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation ..... Internally limited
Input—Output Voltage Differential 35V
Operating Junction Temperature Range
UC150 ..... −55°C to +150°C
UC250 ..... −25°C to +150°C
UC350 ..... 0°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

TYPICAL APPLICATIONS

1.2V—25V Adjustable Regulator

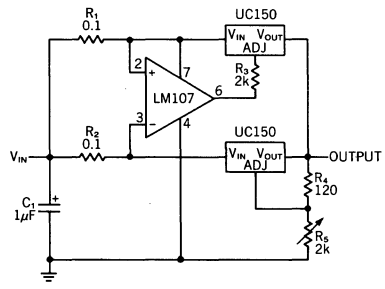


*Needed if regulator is far from power supply filter capacitor
†Optional—improves transient response

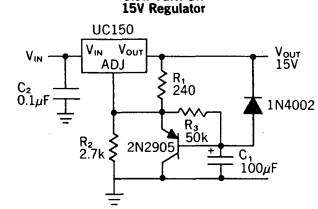
†† $V_{OUT} = 1.25V \left(1 + \frac{R_2}{R_1}\right)$

Note: Usually R_1 = 240Ω for UC150 and UC250 and R_1 = 120Ω for UC350

6A Regulator



Slow Turn-On 15V Regulator



UNITRODE

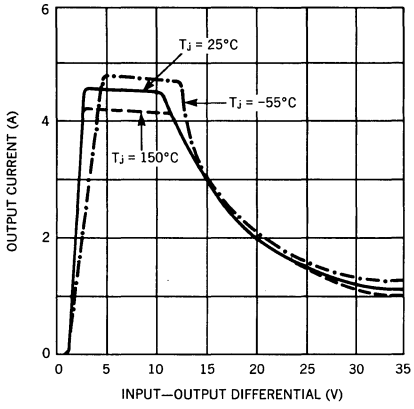
ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	TEST CONDITIONS	UC150/UC250			UC350			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Line Regulation	T_A = 25°C, 3V ≤ (V_{IN} — V_{OUT}) ≤ 35V, (Note 2)		0.005	0.01		0.005	0.03	%/V
Load Regulation	T_A = 25°C, 10mA ≤ I_{OUT} ≤ 3A V_{OUT} ≤5V, (Note 2) V_{OUT} ≥ 5V, (Note 2)		 5 0.1	 15 0.3		 5 0.1	 25 0.1	 mV %
Thermal Regulation	Pulse = 20ms		0.002	0.01		0.002	0.03	%/W
Adjustment Pin Current			50	100		50	100	μA
Adjustment Pin Current Change	10mA ≤ I_L ≤ 3A 3V ≤ (V_{IN} — V_{OUT}) ≤ 35V		0.2	5		0.2	5	μA
Reference Voltage	3 ≤ (V_{IN} — V_{OUT}) ≤ 35V, 10mA ≤ I_{OUT} ≤ 3A, P ≤ 30W	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation	3 ≤ (V_{IN} — V_{OUT}) ≤ 35V, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	V_{OUT} ≤ 5V 10mA ≤ I_{OUT} ≤ 3A, (Note 2) V_{OUT} ≥ 5V		20 0.3	50 1		20 0.3	70 1.5	mV %
Temperature Stability	T_{MIN} ≤ T_j ≤ T_{MAX}		1			1		%
Minimum Load Current	(V_{IN} — V_{OUT}) = 35V		3.5	5		3.5	10	mA
Current Limit	(V_{IN} — V_{OUT}) ≤10V (V_{IN} — V_{OUT}) = 30V	3.0	4.5 1		3.0	4.5 1		A A
RMS Output Noise	T_A = 25°C, 10Hz ≤ f ≤ 10kHz		0.003			0.003		%
Ripple Rejection Ratio	V_{OUT} = 10V, f = 120Hz C_{ADJ} = 10μF	 66	65 86		 66	65 86		dB dB
Long Term Stability	T_A = 125°C, 1000 Hrs.		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case				1.5			1.5	°C/W

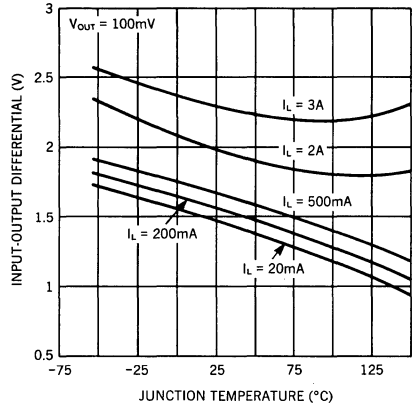
Notes: 1. Unless otherwise noted, the above specifications apply over the following conditions:
UC150: −55°C ≤ T_j ≤ 150°C
UC250: −25°C ≤ T_j ≤ 150°C
UC350: 0°C ≤ T_j ≤ 125°C
(V_{IN} — V_{OUT}) = 5V, I_{OUT} = 1.5A
2. All regulation specifications are measured at constant junction temperatures using low duty-cycle pulse testing.

TYPICAL PERFORMANCE CHARACTERISTICS

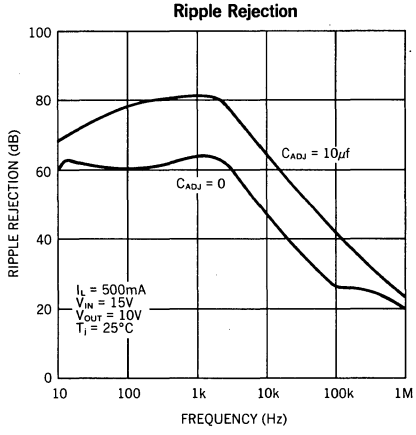
Current Limit



Dropout Voltage

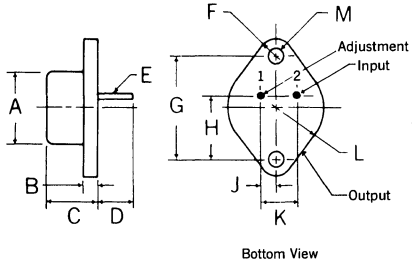


Ripple Rejection



MECHANICAL SPECIFICATIONS AND CONNECTION DIAGRAM

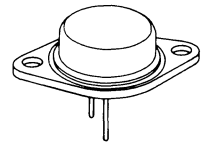
UC150 UC250 UC350



Bottom View

	INCHES	MILLIMETERS
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	.250-.450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	.188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655-.675	16.64-17.15
J	.205-.225	5.21-5.72
K	.420-.440	10.67-11.18
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.

TO-204AA K(TO-3)



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APPLICATION HINTS

In operation, the UC150 develops a nominal 1.25V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R_1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R_2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}R_2$$

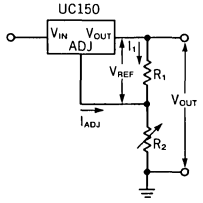


Figure 1

Since the 50μA current from the adjustment terminal represents an error term, the UC150 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

External Capacitors

An input bypass capacitor is recommended. A 0.1μF disc or 1μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the UC150 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10μF bypass capacitor 86 dB ripple rejection is obtainable at any output level.

In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25μF in aluminum electrolytic to equal 1μF solid tantalum at high frequencies.

Although the UC150 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500pF and 5000pF. A 1μF solid tantalum (or 25μF aluminum electrolytic) on the output swamps this effect and insures stability.

Load Regulation

The UC150 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation.

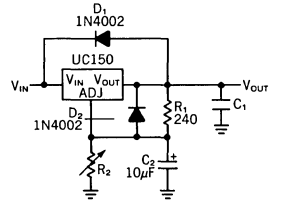
With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor by using 2 separate leads to the case. The ground of R_2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

Protection Diodes

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharged current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the UC150, this discharge path is through a large junction that is able to sustain 25A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25μF or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the UC150 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10μF capacitance. *Figure 2* shows a UC150 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.



$$V_{OUT} = 1.25V\left(1 + \frac{R_2}{R_1}\right) + R_2I_{ADJ}$$

Figure 2. Regulator with Protection Diodes

LINEAR INTEGRATED CIRCUITS

Advanced Regulating Pulse Width Modulators

UC493A UC493AC
UC494A UC494AC
UC495A UC495AC
UC495B UC495BC

FEATURES

- Dual uncommitted 40V, 200mA output transistors
- 1% accurate 5V reference
- Dual error amplifiers
- Wide range, variable deadtime
- Single-ended or push-pull operation
- Under-voltage lockout with hysteresis
- Double pulse protection
- Master or slave oscillator operation
- UC493A/UC495B: Built in 80mV threshold for current limiting
- UC495A/UC495B: Internal 39V zener diode
- UC495A/UC495B: Buffered steering control

DESCRIPTION

This entire series of PWM modulators each provide a complete pulse width modulation system in a single monolithic integrated circuit. These devices include a 5V reference accurate to ±1%, two independent amplifiers usable for both voltage and current sensing, an externally synchronizable oscillator with its linear ramp generator, and two uncommitted transistor output switches. These two outputs may be operated either in parallel for single-ended operation or alternating for push-pull applications with an externally controlled dead-band. These units are internally protected against double-pulsing of a single output or from extraneous output signals when the input supply voltage is below minimum.

The UC495A and UC495B also contain an on-chip 39V zener diode for high-voltage applications where V_{CC} would be greater than 40V, and a buffered output steering control that overrides the internal control of the pulse steering flip-flop.

UC493A and UC494A are packaged in a 16-pin DIP, while the UC495A and UC495B are packaged in an 18-pin DIP. The UC493A, UC494A, UC495A and UC495B are specified for operation over the full military temperature range of −55°C to +125°C, while the UC493AC, UC494AC, UC495AC and UC495BC are designed for industrial applications from 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS (Note 1)

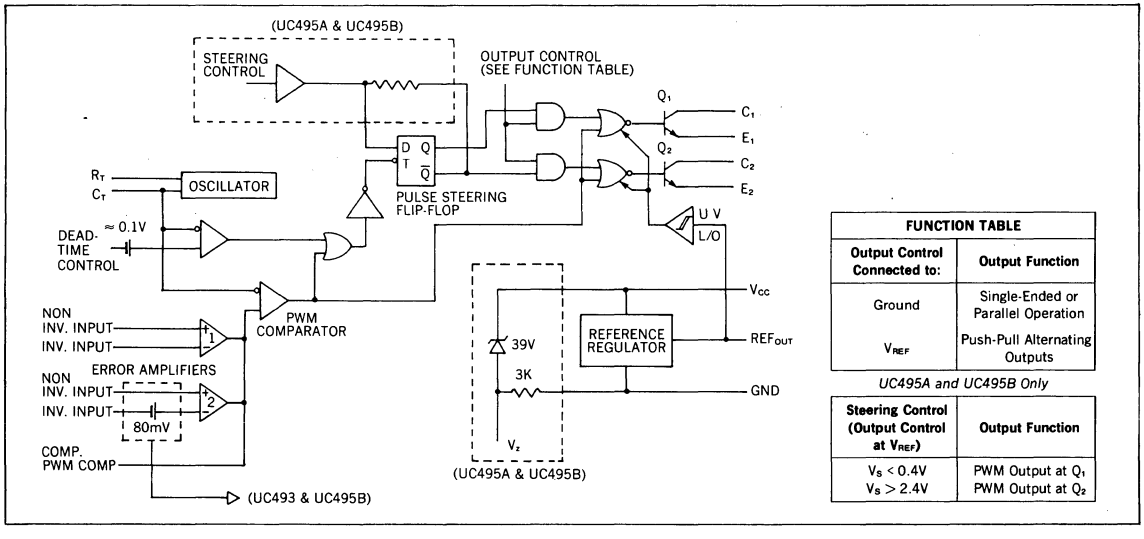
Supply Voltage, V_{CC} (Note 2) 45V
Amplifier Input Voltages ..... V_{CC} + 0.3V
Collector Output Voltage 41V
Collector Output Current 250mA
Continuous Total Dissipation 1000mW
@ (or below) 25°C free air temperature range (Note 3)
Storage Temperature Range ..... −65° to +150°C
Lead Temperature 1/16" (1.6mm) from case for 60 seconds,
J Package ..... 300°C
Lead Temperature 1/16" (1.6mm) from case for 10 seconds,
N Package ..... 260°C

Notes: 1. Over operating free air temperature range unless otherwise noted.
2. All voltage values are with respect to network ground terminal.
3. For J package, derate at 8.2mW/°C for ambient temperature above +28°C. For N package, derate at 9.2mW/°C for ambient temperature above +41°C.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{CC} ..... 7V to 40V
Error Amplifier Input Voltages ..... −0.3V to V_{CC}−2V
Collector Output Voltage 40V
Collector Output Current (each transistor) 200mA
Current into Feedback Terminal 0.3mA
Timing Capacitor, C_T ..... 0.47nF to 10,000nF
Timing Resistor, R_T ..... 1.8KΩ to 500KΩ
Oscillator Frequency ..... 1kHz to 300kHz
Operating Free Air Temperature
UC493A, UC494A, UC495A, UC495B ..... −55°C to +125°C
UC493AC, UC494AC, UC495AC, UC495BC ..... 0°C to +70°C

BLOCK DIAGRAM



FUNCTION TABLE	
Output Control Connected to:	**Output Function**
Ground	Single-Ended or Parallel Operation
V_{REF}	Push-Pull Alternating Outputs

UC495A and UC495B Only

Steering Control (Output Control at V_{REF})	**Output Function**
$V_S < 0.4V$	PWM Output at Q_1
$V_S > 2.4V$	PWM Output at Q_2

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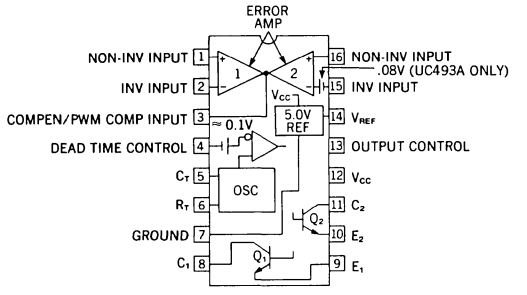
CONNECTION DIAGRAMS

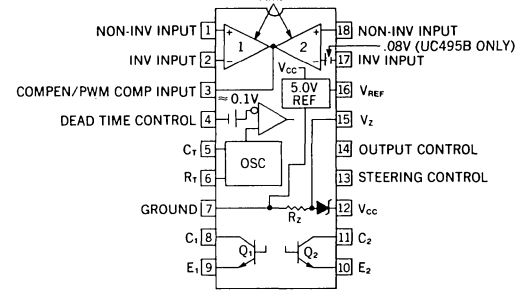
DIL-16 (Top View)
J or N Package

UC493A/UC493AC
UC494A/UC494AC



DIL-18 (Top View)
J or N Package

UC495A/UC495AC
UC495B/UC495BC



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, over recommended operating free-air temperature range, V_{CC} = 15V, f = 10kHz.)

PARAMETER		TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Reference Section						
Output Voltage (V_{REF})		I_O = 1mA, T_A = 25°C	4.95	5	5.05	V
Input Regulation		V_{CC} = 7V to 40V		2	25	mV
Output Regulation		I_O = 1mA to 10mA		1	15	mV
Output Voltage over Temperature		Δ T_A = Min. to Max.	4.90		5.10	V
Short Circuit Output Current (Note 1)		V_{REF} = 0, T_A = 25°C	10	35	50	mA
Oscillator Section						
Frequency (Note 2)		C_T = 0.01μF, R_T = 12kΩ		10		kHz
Standard Deviation of Frequency (Note 3)		All values of V_{CC}, C_T, R_T, T_A constant		10		%
Frequency Change with Voltage		V_{CC} = 7V to 40V, T_A = 25°C		0.1		%
Frequency Change with Temperature		C_T = 0.01μF, R_T = 12kΩ Δ T_A = Min. to Max.			2	%
Deadtime Control Section (Output Control connected to V_{REF})						
Input Bias Current (Pin 4)		$V_{(PIN\ 4)}$ = 0V to 5.25V		-2	-10	μA
Maximum Duty-Cycle (Each Output)		$V_{(PIN\ 4)}$ = 0V	45			%
Input Threshold Voltage (Pin 4)		Zero Duty-Cycle		3	3.3	V
		Maximum Duty-Cycle	0			
Amplifier Section (Current Limit specifications apply to UC493A and UC495B only)						
Input Offset Voltage	Error	$V_{O\ (PIN\ 3)}$ = 2.5V		2	10	mV
	Current Limit		70	80	90	
Input Offset Current		$V_{O\ (PIN\ 3)}$ = 2.5V		25	250	nA
Input Bias Current	Error	$V_{O\ (PIN\ 3)}$ = 2.5V		-0.2	-1	μA
	Current Limit			-1	-2	
Common-Mode Input Voltage Range		V_{CC} = 7V to 40V	0.3 to V_{CC} -2			V
Open Loop Voltage Gain	Error	Δ V_O = 3V, V_O = 0.5V to 3.5V	70	95		dB
	Current Limit		66	90		
Unity Gain Bandwidth				800		kHz
Common-Mode Rejection Ratio	Error	V_{CC} = 40V, T_A = 25°C	65	80		dB
	Current Limit		50	70		
Output Sink Current (Pin 3)		V_{ID} = -15mV to -5V, $V_{(PIN\ 3)}$ = 0.7V	0.3	0.7		mA
Output Source Current (Pin 3)		V_{ID} = 15mV to 5V, $V_{(PIN\ 3)}$ = 3.5V	-2			mA

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ELECTRICAL CHARACTERISTICS (Unless otherwise stated, over recommended operating free-air temperature range, V_{CC} = 15V, f = 10kHz.)

PARAMETER		TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Section						
Collector Off-State Current		V_{CE} = 40V, V_{CC} = 40V		2	100	μA
Emmitter Off-State Current		V_{CC} = V_C = 40V, V_E = 0			-100	μA
Collector-Emitter Saturation Voltage	Common-Emitter	V_E = 0, I_C = 200mA		1.1	1.3	V
	Emitter-Follower	V_C = 15V, I_E = -200mA		1.5	2.5	
Output Control Input Current		V_I = V_{REF}			3.5	mA
PWM Comparator Section						
Input Threshold Voltage (Pin 3)		Zero Duty-Cycle		4	4.5	V
Input Sink Current (Pin 3)		$V_{(PIN\ 3)}$ = 0.7V	0.3	0.7		mA
Steering Control (UC495A and UC495B only, see Function Table)						
Input Current		$V_{(PIN\ 13)}$ = 0.4V, Q_1 active			-200	μA
		$V_{(PIN\ 13)}$ = 2.4V, Q_2 active			300	
Deadband				500		mV
Zener Diode Circuit (UC495A and UC495B only)						
Breakdown Voltage		V_{CC} = 45V, I_Z = 2mA	36	39	45	V
Sink Current		$V_{(PIN\ 15)}$ = 1V	0.2	0.3	0.6	mA
Total Device						
Standby Supply Current		Pin 6 at V_{REF}. All other V_{CC} = 15V		6	10	mA
		inputs and outputs open. V_{CC} = 40V		9	15	
Under-Voltage Lockout			3.5		6.5	V
Hysteresis				300		mV
Switching Characteristics (T_A = 25°C)						
Output Voltage Rise Time		Common-Emitter Configuration		100	200	ns
Output Voltage Fall Time		R_L = 68Ω, C_L = 15pF		25	100	ns
Output Voltage Rise Time		Emitter-Follower Configuration		100	200	ns
Output Voltage Fall Time		R_L = 68Ω, C_L = 15pF		40	100	ns

Notes: 1. Duration of the short circuit should not exceed one second.

2. Frequency for other values of C_T and R_T is approximately $f = \frac{1.1}{R_T C_T}$

3. Standard deviation is a measure of the statistical distribution about the mean as derived from the formula $\sigma = \sqrt{\frac{\sum_{n=1}^{n} (x_n - x)^2}{n-1}}$

Figure 1. Slaving Two or More Control Circuits

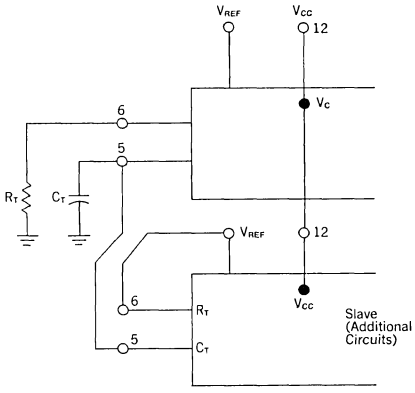
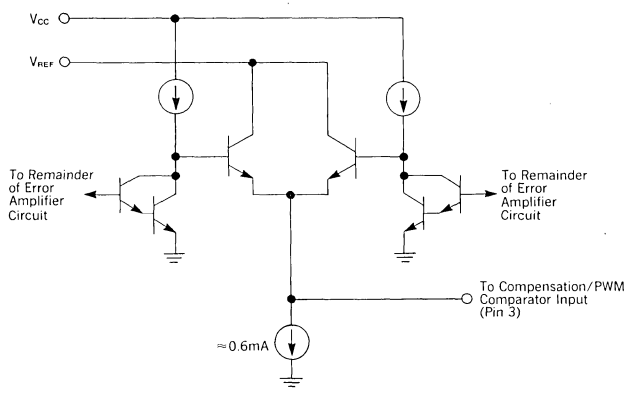


Figure 2. Output Circuit of Error Amplifiers



3

Figure 3. Output Connections for Single-Ended and Push-Pull Configurations

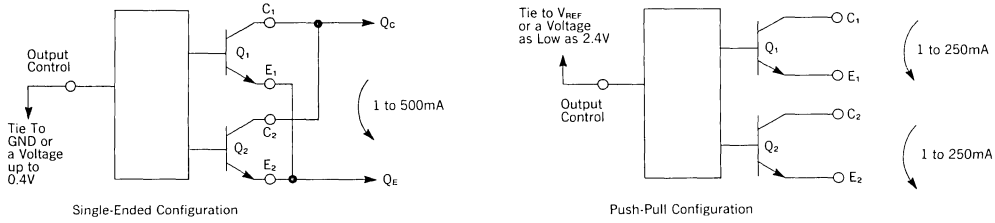


Figure 4. Internal Buffer with Deadband for Steering Control on UC495A and UC495B

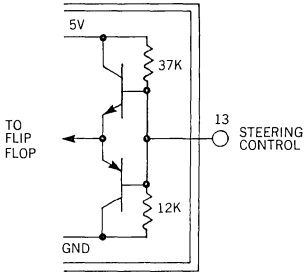


Figure 5. Operation with $V_{IN} > 40V$ Using Internal Zener (UC495A and UC495B Only)

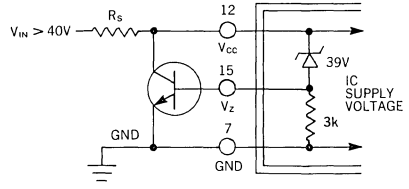
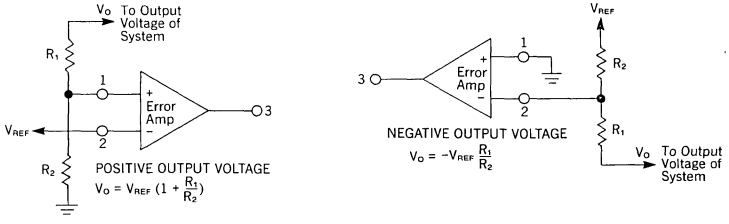


Figure 6. Error Amplifier Sensing Techniques



LINEAR INTEGRATED CIRCUITS

Advanced Regulating Pulse Width Modulators

UC1524A
UC2524A
UC3524A

FEATURES

- Fully interchangeable with standard UC1524 family
- Precision reference internally trimmed to ±1%
- High-Performance current limit function
- Under-voltage lockout with hysteretic turn-on
- Start-up supply current less than 4mA
- Output current to 200mA
- 60V output capability
- Wide common-mode input range for both error and current limit amplifiers
- PWM latch insures single pulse per period
- Double pulse suppression logic
- 200ns shutdown through PWM latch
- Guaranteed frequency accuracy
- Thermal shutdown protection

DESCRIPTION

The UC1524A family of regulating PWM ICs has been designed to retain the same highly versatile architecture of the industry standard UC1524 (SG1524) while offering substantial improvements to many of its limitations. The UC1524A is pin compatible with "non-A" models and in most existing applications can be directly interchanged with no effect on power supply performance. Using the UC1524A, however, frees the designer from many concerns which typically had required additional circuitry to solve.

The UC1524A includes a precise 5V reference trimmed to ±1% accuracy, eliminating the need for potentiometer adjustments; an error amplifier with an input range which includes 5V, eliminating the need for a reference divider; a current sense amplifier useful in either the ground or power supply output lines; and a pair of 60V, 200mA uncommitted transistor switches which greatly enhance output versatility.

An additional feature of the UC1524A is an under-voltage lockout circuit which disables all the internal circuitry, except the reference, until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifying the design of low power, off-line supplies. The turn-on circuit has approximately 600mV of hysteresis for jitter-free activation.

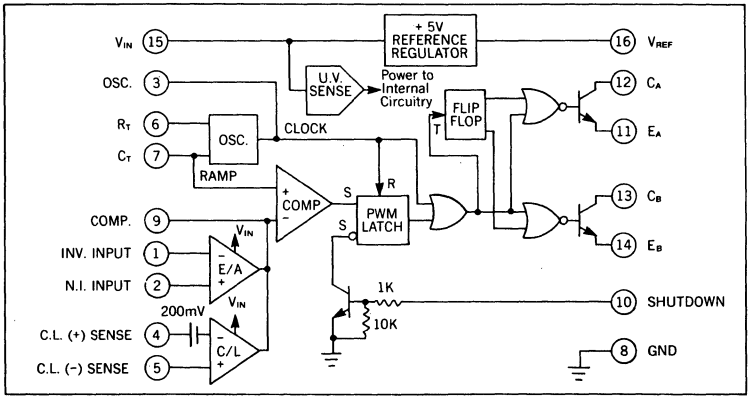
Other product enhancements included in the UC1524A's design include a PWM latch which insures freedom from multiple pulsing within a period, even in noisy environments, logic to eliminate double pulsing on a single output, a 200ns external shutdown capability, and automatic thermal protection from excessive chip temperature. The oscillator circuit of the UC1524A is usable beyond 500kHz and is now easier to synchronize with an external clock pulse.

The UC1524A is packaged in a hermetic 16-pin DIP and is rated for operation from −55°C to +125°C. The UC2524A and UC3524A are available in either ceramic or plastic packages and are rated for operation from −25°C to +85°C and 0°C to 70°C, respectively.

ABSOLUTE MAXIMUM RATINGS

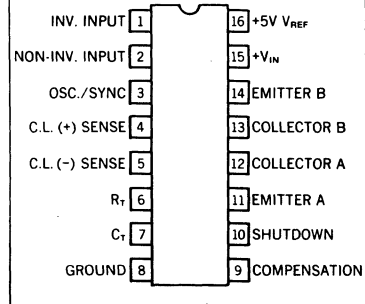
Supply Voltage (V_{IN})	40V
Collector Supply Voltage (V_C)	60V
Output Current (Each Output)	200mA
Reference Output Current	50mA
Oscillator Charging Current	5mA
Power Dissipation at T_A = +25°C	1000mW
Derate above +50°C	10mW/°C
Power Dissipation at T_C = +25°C	2000mW
Derate for Case Temperature above +25°C	16mW/°C
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

BLOCK DIAGRAM



CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N Package



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ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1524A, −25°C to +85°C for the UC2524A, and 0°C to +70°C for the UC3524A; V_{IN} = V_C = 20V.)

PARAMETER	TEST CONDITIONS	UC1524A UC2524A			UC3524A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Turn-on Characteristics								
Input Voltage	Operating Range after Turn-on	8		40	8		40	V
Turn-on Threshold		5.5	7.5	8.5	5.5	7.5	8.5	V
Turn-on Current	V_{IN} = 6V		2.5	4		2.5	4	mA
Operating Current	V_{IN} = 8 to 40V		5	10		5	10	mA
Turn-on Hysteresis*			0.6			0.6		V
Reference Section								
Output Voltage	T_j = 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	V_{IN} = 10 to 40V		10	20		10	30	mV
Load Regulation	I_L = 0 to 20mA		20	50		20	50	mV
Temperature Stability*	Over Operating Range*		20	50		20	50	mV
Short Circuit Current	V_{REF} = 0, T_j = 25°C		80	100		80	100	mA
Output Noise Voltage*	10hz ≤ f ≤ 10kHz, T_j = 25°C		40			40		μVrms
Long Term Stability*	T_j = 125°C, 1000 Hrs.		20	50		20	50	mV
Oscillator Section (Unless otherwise specified, R_T = 2700Ω, C_T = 0.01 mfd)								
Initial Accuracy	T_j = 25°C	41	43	45	39	43	47	kHz
Temperature Stability	Over Operating Temperature Range		1	2		1	2	%
Minimum Frequency*	R_T = 150kΩ, C_T = 0.1 mfd			140			120	Hz
Maximum Frequency	R_T = 2.0kΩ, C_T = 470 pF	500			500			kHz
Output Amplitude*	T_j = 25°C		3.5			3.5		V
Output Pulse Width*	T_j = 25°C		0.5			0.5		μs
Ramp Peak		3.3	3.5	3.7	3.3	3.5	3.7	V
Ramp Valley	T_j = 25°C	0.7	0.8	0.9	0.7	0.8	0.9	V
Ramp Valley T.C.			−1.0			−1.0		mV/°C
Error Amplifier Section (Unless otherwise specified, V_{CM} = 2.5V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	5		1	10	μA
Input Offset Current			.05	1		0.5	1	μA
Common Mode Rejection Ratio	V_{CM} = 1.5 to 5.5V	60	75		60	75		dB
Power Supply Rejection Ratio	V_{IN} = 10 to 40V	50	60		50	60		dB
Output Swing	Minimum Total Range	0.5		5.0	0.5		5.0	V
Open Loop Voltage Gain	ΔV_O = 1 to 4V, $R_L \geq$ 10 Meg Ω	72	80		60	80		dB
Gain-Bandwidth*	T_j = 25°C, A_V = 0dB	1	3		1	3		MHz
DC Transconductance*†	T_j = 25°C, 30kΩ ≤ R_L ≤ 1MΩ	1.7	2.3		1.7	2.3		mS

* These parameters are guaranteed by design but not 100% tested in production.

† DC transconductance (g_M) relates to DC open-loop voltage gain according to the following equation: $A_V = g_M R_L$ where R_L is the resistance from pin 9 to ground.

The minimum g_M specification is used to calculate minimum A_V when the error amplifier output is loaded.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1524A, −25°C to +85°C for the UC2524A, and 0°C to +70°C for the UC3524A; V_{IN} = V_C = 20V.)

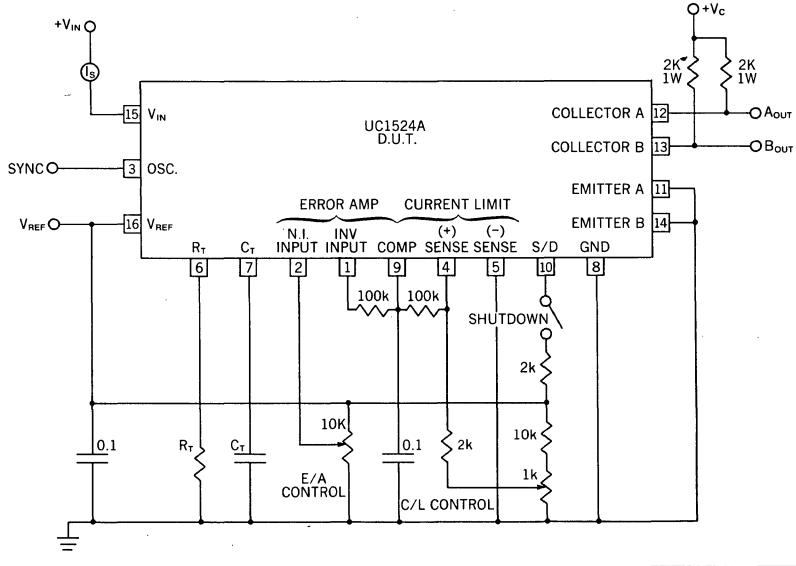
PARAMETER	TEST CONDITIONS	UC1524A UC2524A			UC3524A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Current Limit Amplifier (Unless otherwise specified, Pin 5 = 0V)								
Input Offset Voltage	T_j = 25°C, E/A Set for Maximum Output	190	200	210	180	200	220	mV
Input Offset Voltage	Over Operating Temperature Range	180		220	170		230	mV
Input Bias Current			−1	−10		−1	−10	μA
Common Mode Rejection Ratio	$V_{(Pin\ 5)}$ = −0.3V to +5.5V	50	60		50	60		dB
Power Supply Rejection Ration	V_{IN} = 10 to 40V	50	60		50	60		dB
Output Swing	Minimum Total Range	0.5		5.0	0.5		5.0	V
Open-Loop Voltage Gain	ΔV_O = 1 to 4V, $R_L \geq$ 10 Meg Ω	70	80		70	80		dB
Delay Time*	Pin 4 to Pin 9, ΔV_{IN} = 300mV		300			300		ns
Output Section (Each Output)								
Collector Emitter Voltage	I_C = 100μA	60	80		60	80		V
Collector Leakage Current	V_{CE} = 50V		.1	20		.1	20	μA
Saturation Voltage	I_C = 20mA I_C = 200mA		.2 1	.4 2.2		.2 1	.4 2.2	V V
Emitter Output Voltage	I_E = 50mA	17	18		17	18		V
Rise Time*	T_j = 25°C, R = 2K Ω		200			200		ns
Fall Time*	T_j = 25°C, R = 2K Ω		100			100		ns
Comparator Delay*	T_j = 25°C, Pin 9 to output		300			300		ns
Shutdown Delay*	T_j = 25°C, Pin 10 to Output		200			200		ns
Shutdown Threshold	T_j = 25°C, R_C = 2K Ω	0.6	.7	1.0	0.6	.7	1.0	V
Thermal Shutdown*			165			165		°C

* These parameters are guaranteed by design but not 100% tested in production.

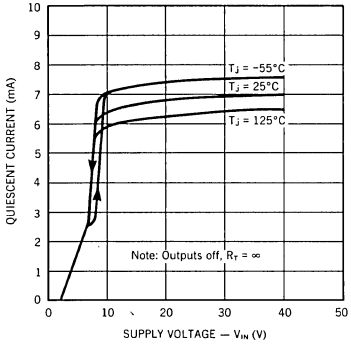
OPEN-LOOP TEST CIRCUIT

Note: The UC1524A should be able to be tested in any 1524 test circuit with two possible exceptions:
1. The higher gain-bandwidth of the current limit amplifier in the UC1524A may cause oscillations in an uncompensated 1524 test circuit.
2. The effect of the shutdown, pin 10, cannot be seen at the compensation terminal, pin 9, but must be observed at the outputs.

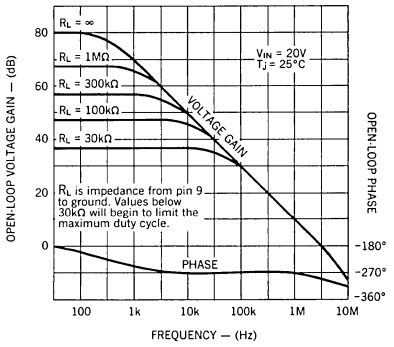
The circuit below will allow all UC1524A functions to be evaluated.



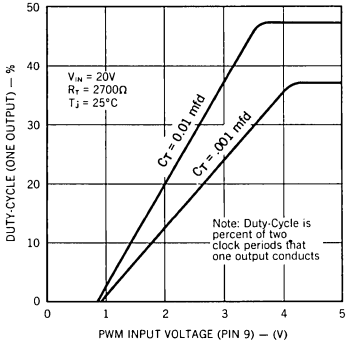
Supply Current vs Voltage



Error Amplifier Voltage Gain and Phase vs Frequency



Pulse Width Modulator Transfer Function



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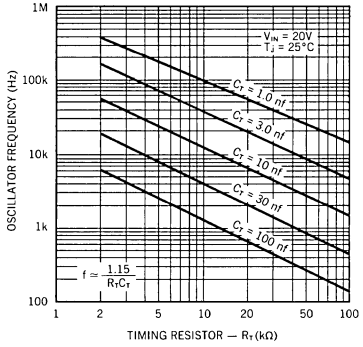
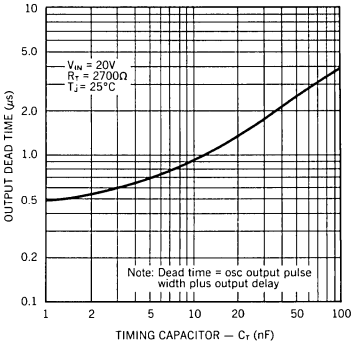
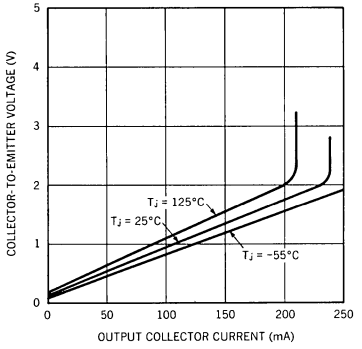
Oscillator Frequency vs Timing Components



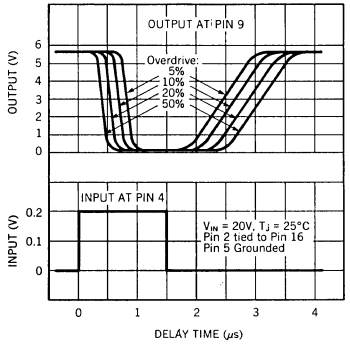
Output Dead Time vs Timing Capacitor Value



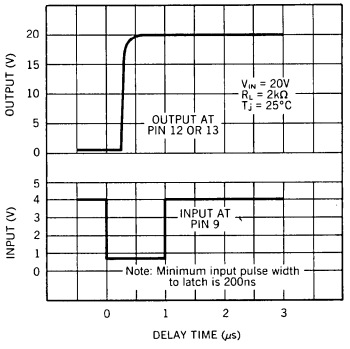
Output Saturation Voltage



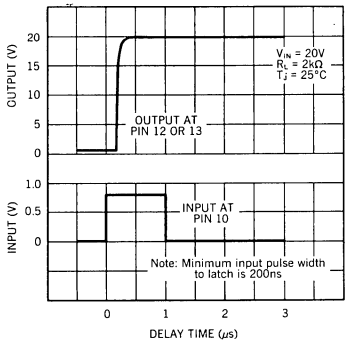
Current Limit Amplifier Delay



Shutdown Delay From PWM Comparator — Pin 9



Turn-Off Delay From Shutdown — Pin 10



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LINEAR INTEGRATED CIRCUITS

Regulating Pulse Width Modulators

UC1524
UC2524
UC3524

FEATURES

- Complete PWM Power control circuitry
- Uncommitted outputs for single-ended or push-pull applications
- Low standby current ... 8mA typical
- Interchangeable with SG1524, SG2524 and SG3524, respectively

DESCRIPTION

The UC1524, UC2524 and UC3524 incorporate on a single monolithic chip all the functions required for the construction of regulating power supplies inverters or switching regulators. They can also be used as the control element for high-power-output applications. The UC1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allow either single-ended or push-pull applications. Each device includes an on-chip reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry. The UC1524 is characterized for operation over the full military temperature range of −55°C to +125°C. The UC2524 and UC3524 are designed for operation from −25°C to +85°C and 0°C to +70°C, respectively.

ABSOLUTE MAXIMUM RATINGS (Note 1)

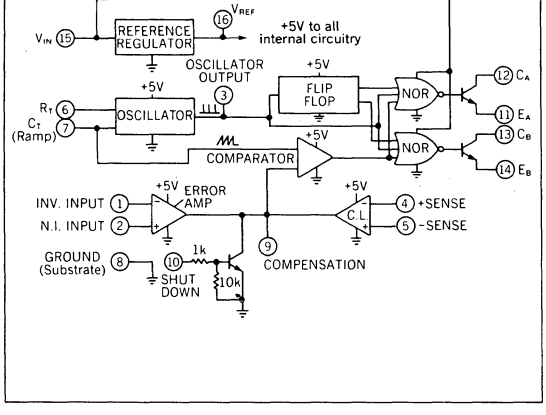
Supply Voltage, V_{CC} (Notes 2 and 3) 40V
Collector Output Current 100mA
Reference Output Current 50mA
Current Through C_T Terminal ..... −5mA
Power Dissipation at T_A = +25°C (Note 4) 1000mW
Thermal Resistance, Junction to Ambient ..... 100°C/W
Power Dissipation at T_C = +25°C (Note 5) 2000mW
Thermal Resistance, Junction to Case ..... 60°C/W
Operating Junction Temperature Range ..... −55°C to +150°C
Storage Temperature Range ..... −65°C to +150°C

Notes: 1. Over operating free-air temperature range unless otherwise noted.
2. All voltage values are with respect to the ground terminal, pin 8
3. The reference regulator may be bypassed for operation from a fixed 5V supply by connecting the V_{CC} and reference output pins both to the supply voltage. In this configuration the maximum supply voltage is 6V.
4. Derate at 10mW/°C for ambient temperatures above +50°C
5. Derate at 16mW/°C for case temperatures above +25°C

RECOMMENDED OPERATING CONDITIONS

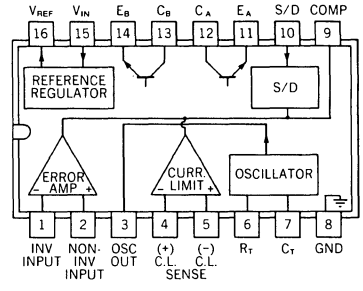
Supply Voltage, V_{CC} ..... 8V to 40V
Reference Output Current ..... 0 to 20mA
Current through C_T Terminal ..... −0.03mA to −2mA
Timing Resistor, R_T ..... 1.8KΩ to 100KΩ
Timing Capacitor, C_T ..... 0.001μF to 0.1μF
Operating Ambient Temperature Range
UC1524 ..... −55°C to +125°C
UC2524 ..... −25°C to +85°C
UC3524 ..... 0°C to +70°C

BLOCK DIAGRAM



CONNECTION DIAGRAM

DIL-16
J or N Package



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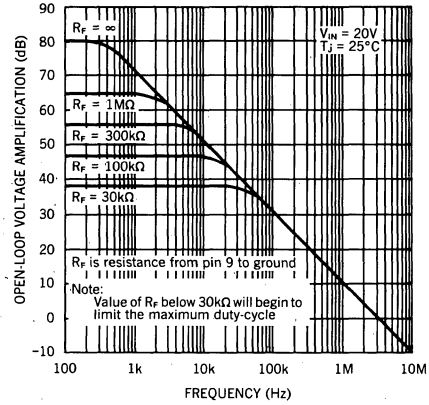
ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1524, −25°C to +85°C for the UC2524, and 0°C to +70°C for the UC3524, V_{IN} = 20V, and f = 20kHz)

PARAMETER	TEST CONDITIONS	UC1524/UC2524			UC3524			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage		4.8	5.0	5.2	4.6	5.0	5.4	V
Line Regulation	V_{IN} = 8 to 40V		10	20		10	30	mV
Load Regulation	I_L = 0 to 20mA		20	50		20	50	mV
Ripple Rejection	f = 120Hz, T_j = 25°C		66			66		dB
Short Circuit Current Limit	V_{REF} = 0, T_j =25°C		100			100		mA
Temperature Stability	Over Operating Temperature Range		0.3	1		0.3	1	%
Long Term Stability	T_j = 125°C, t = 1000 Hrs.		20			20		mV
Oscillator Section								
Maximum Frequency	C_T = .001mfd, R_T = 2kΩ		300			300		kHz
Initial Accuracy	R_T and C_T Constant		5			5		%
Voltage Stability	V_{IN} = 8 to 40V, T_j = 25°C			1			1	%
Temperature Stability	Over Operating Temperature Range			2			2	%
Output Amplitude	Pin 3, T_j =25°C		3.5			3.5		V
Output Pulse Width	C_T = .01mfd, T_j = 25°C		0.5			0.5		μs
Error Amplifier Section								
Input Offset Voltage	V_{CM} = 2.5V		0.5	5		2	10	mV
Input Bias Current	V_{CM} = 2.5V		2	10		2	10	μA
Open Loop Voltage Gain		72	80		60	80		dB
Common Mode Voltage	T_j = 25°C	1.8		3.4	1.8		3.4	V
Common Mode Rejection Ratio	T_j = 25°C		70			70		dB
Small Signal Bandwidth	A_V = 0dB, T_j = 25°C		3			3		MHz
Output Voltage	T_j = 25°C	0.5		3.8	0.5		3.8	V
Comparator Section								
Duty-Cycle	% Each Output On	0		45	0		45	%
Input Threshold	Zero Duty-Cycle		1			1		V
Input Threshold	Maximum Duty-Cycle		3.5			3.5		V
Input Bias Current			1			1		μA
Current Limiting Section								
Sense Voltage	Pin 9 = 2V with Error Amplifier Set for Maximum Out, T_j = 25°C	190	200	210	180	200	220	mV
Sense Voltage T.C.			0.2			0.2		mV/°C
Common Mode Voltage		−1		+1	−1		+1	V
Output Section (Each Output)								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	V_{CE} = 40V		0.1	50		0.1	50	μA
Saturation Voltage	I_C = 50mA		1	2		1	2	V
Emitter Output Voltage	V_{IN} = 20V	17	18		17	18		V
Rise Time	R_C = 2K ohm, T_j = 25°C		0.2			0.2		μs
Fall Time	R_C = 2K ohm, T_j = 25°C		0.1			0.1		μs
Total Standby Current (Excluding oscillator charging current, error and current limit dividers, and with outputs open)	V_{IN} = 40V		8	10		8	10	mA

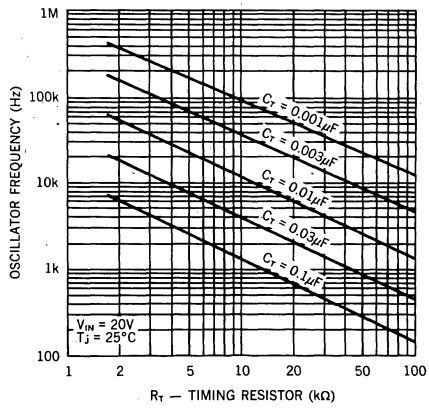
3

TYPICAL CHARACTERISTICS

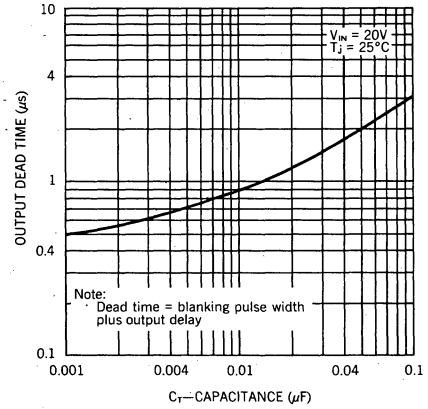
Open-Loop Voltage Amplification of Error Amplifier vs Frequency



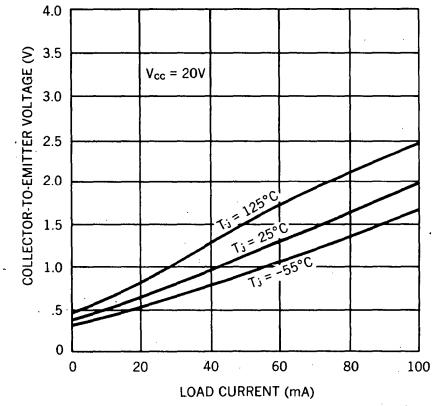
Oscillator Frequency vs Timing Components



Output Dead Time vs Timing Capacitance Value



Output Saturation Voltage vs Load Current



PRINCIPLES OF OPERATION

The UC1524 is a fixed-frequency pulse-width-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor (R_T) and one timing capacitor (C_T). R_T establishes a constant charging current for C_T. This results in a linear voltage ramp at C_T, which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The UC1524 contains an on-board 5V regulator that serves as a reference as well as powering the UC1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generate a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at C_T. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistor (Q_1 or Q_2) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the value of C_T. The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier, or to provide additional control to the regulator.

3

TYPICAL APPLICATIONS DATA

Oscillator

The oscillator controls the frequency of the UC1524 and is programmed by R_T and C_T according to the approximate formula:

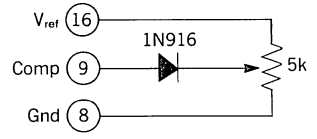
$$f \approx \frac{1.18}{R_T C_T}$$

where R_T is in kilohms
C_T is in microfarads
f is in kilohertz

Practical values of C_T fall between 0.001 and 0.1 microfarad. Practical values of R_T fall between 1.8 and 100 kilohms. This results in a frequency range typically from 120 hertz to 500 kilohertz.

Blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of C_T. If small values of C_T are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit below:

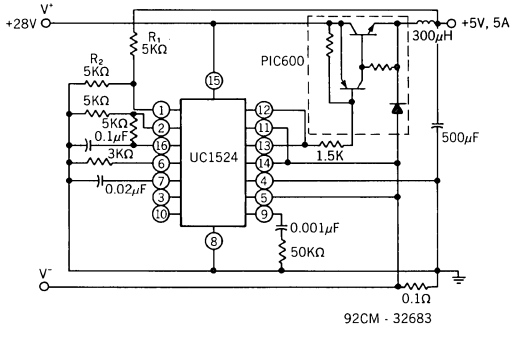


Synchronous Operation

When an external clock is desired, a clock pulse of approximately 3V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 kilohms. In this configuration R_T C_T must be selected for a clock period slightly greater than that of the external clock.

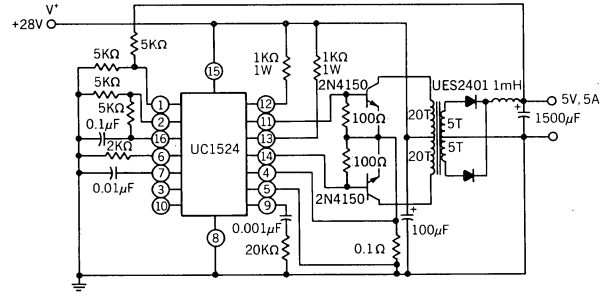
If two or more UC1524 regulators are to be operated synchronously, all oscillator output terminals should be tied together, all C_T terminals connected to a single timing capacitor, and the timing resistor connected to a single R_T terminal. The other R_T terminals can be left open or shorted to V_{REF}. Minimum lead lengths should be used between the C_T terminals.

Single-Ended LC Switching Regulator Circuit

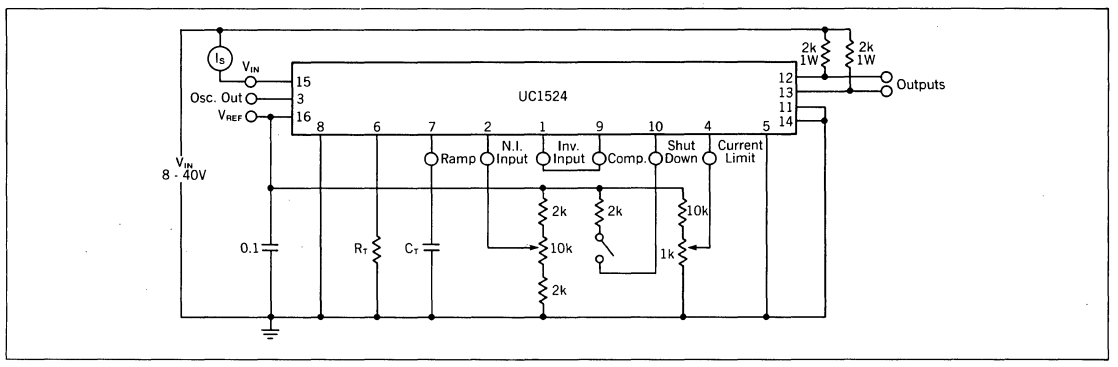


92CM - 32683

Push-Pull Transformer-Coupled Circuit

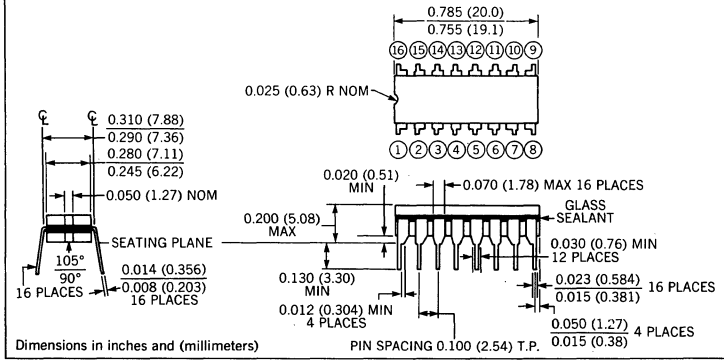


OPEN LOOP TEST CIRCUIT



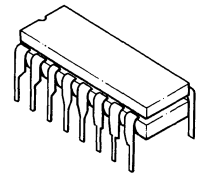
MECHANICAL SPECIFICATIONS

UC1524 UC2524 UC3524

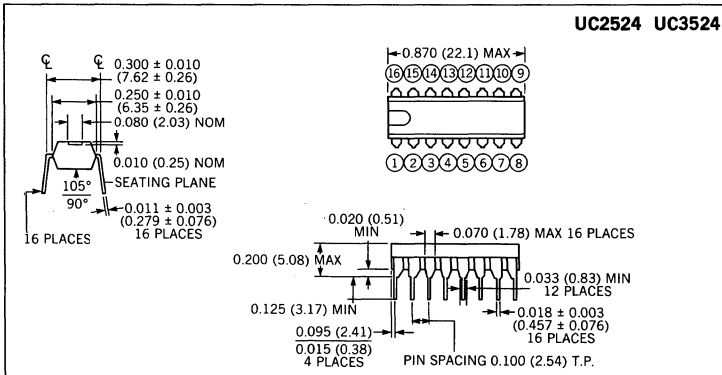


Dimensions in inches and (millimeters)

16-PIN J CERAMIC

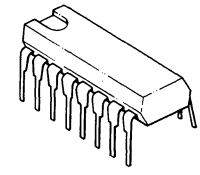


UC2524 UC3524



Dimensions in inches and (millimeters)

16-PIN N PLASTIC



Note: When ordering, add suffix "J" (for 16 pin ceramic package) or "N" (for 16 pin plastic package) to the part number.

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LINEAR INTEGRATED CIRCUITS
Regulating Pulse Width Modulators

UC1525A UC1527A
UC2525A UC2527A
UC3525A UC3527A

FEATURES
- 8 to 35V operation
- 5.1V reference trimmed to ±1%
- 100Hz to 500kHz oscillator range
- Separate oscillator sync terminal
- Adjustable deadtime control
- Internal soft-start
- Pulse-by-pulse shutdown
- Input undervoltage lockout with hysteresis
- Latching PWM to prevent multiple pulses
- Dual source/sink output drivers

DESCRIPTION
The UC1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip +5.1V reference is trimmed to ±1% and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the C_T and the discharge terminals provide a wide range of dead time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The UC1525A output stage features NOR logic, giving a LOW output for an OFF state. The UC1527A utilizes OR logic which results in a HIGH output level when OFF.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, ($+V_{IN}$)	+40V
Collector Supply Voltage (V_C)	+40V
Logic Inputs	-0.3V to +5.5V
Analog Inputs	-0.3V to $+V_{IN}$
Output Current, Source or Sink	500mA
Reference Output Current	50mA
Oscillator Charging Current	5mA
Power Dissipation at T_A= +25°C (Note 2)	1000mW
Thermal Resistance, Junction to Ambient	100°C/W
Power Dissipation at T_C = +25°C (Note 3)	2000mW
Thermal Resistance, Junction to Case	60°C/W
Operating Junction Temperature	-55°C to +150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

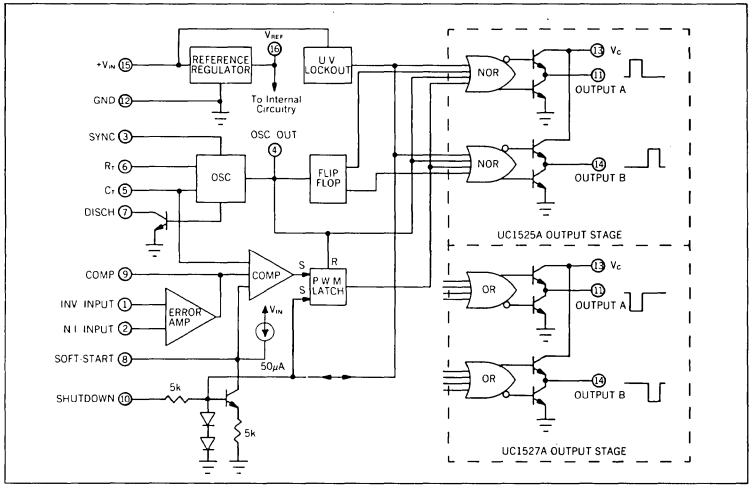
Notes: 1. Values beyond which damage may occur.
2. Derate at 10mW/°C for ambient temperatures above +50°C.
3. Derate at 16mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS (Note 4)

Input Voltage ($+V_{IN}$)	+8V to +35V
Collector Supply Voltage (V_C)	+4.5V to +35V
Sink/Source Load Current (steady state)	0 to 100mA
Sink/Source Load Current (peak)	0 to 400mA
Reference Load Current	0 to 20mA
Oscillator Frequency Range	100Hz to 400kHz
Oscillator Timing Resistor	2kΩ to 150kΩ
Oscillator Timing Capacitor	.001μF to 0.1μF
Dead Time Resistor Range	0 to 500Ω
Operating Ambient Temperature Range	
UC1525A, UC1527A	-55°C to +125°C
UC2525A, UC2527A	-25°C to +85°C
UC3525A, UC3527A	0°C to +70°C

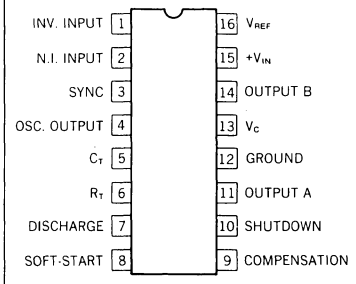
Notes: 4. Range over which the device is functional and parameter limits are guaranteed.

BLOCK DIAGRAM



CONNECTION DIAGRAM

DIL-16 (Top View)
J or N Package



ELECTRICAL CHARACTERISTICS (+V_{IN} = 20V, and over operating temperature, unless otherwise specified)

PARAMETER	TEST CONDITIONS	UC1525A/UC2525A UC1527A/UC2527A			UC3525A UC3527A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_j = 25°C	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V_{IN} = 8 to 35V		10	20		10	20	mV
Load Regulation	I_L = 0 to 20mA		20	50		20	50	mV
Temperature Stability (Note 5)	Over Operating Range		20	50		20	50	mV
Total Output Variation (Note 5)	Line, Load, and Temperature	5.00		5.20	4.95		5.25	V
Short Circuit Current	V_{REF} = 0, T_j =25°C		80	100		80	100	mA
Output Noise Voltage (Note 5)	10Hz ≤ 10kHz, T_j = 25°C		40	200		40	200	μVrms
Long Term Stability (Note 5)	T_j = 125°C		20	50		20	50	mV
Oscillator Section (Note 6)								
Initial Accuracy (Notes 5 & 6)	T_j = 25°C		±2	±6		±2	±6	%
Voltage Stability (Notes 5 & 6)	V_{IN} = 8 to 35V		±0.3	±1		±1	±2	%
Temperature Stability (Note 5)	Over Operating Range		±3	±6		±3	±6	%
Minimum Frequency	R_T = 200kΩ, C_T = 0.1μF			120			120	Hz
Maximum Frequency	R_T = 2kΩ, C_T = 470pF	400			400			kHz
Current Mirror	I_{RT} = 2mA	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude (Notes 5 & 6)		3.0	3.5		3.0	3.5		V
Clock Width (Notes 5 & 6)	T_j = 25°C	0.3	0.5	1.0	0.3	0.5	1.0	μs
Sync Threshold		1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V		1.0	2.5		1.0	2.5	mA
Error Amplifier Section (V_{CM} = 5.1V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	10		1	10	μA
Input Offset Current				1			1	μA
DC Open Loop Gain	R_L ≥ 10 Meg Ω	60	75		60	75		dB
Gain-Bandwidth Product (Note 5)	A_V = 0dB, T_j = 25°C	1	2		1	2		MHz
DC Transconductance (Notes 5 & 7)	T_j = 25°C, 30kΩ ≤ R_L ≤ 1MΩ	1.1	1.5		1.1	1.5		mS
Output Low Level			0.2	0.5		0.2	0.5	V
Output High Level		3.8	5.6		3.8	5.6		V
Common Mode Rejection	V_{CM} = 1.5 to 5.2V	60	75		60	75		dB
Supply Voltage Rejection	V_{IN} = 8 to 35V	50	60		50	60		dB

Notes: 5. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

6. Tested at f_{OSC} = 40KHz (R_T = 3.6kΩ, C_T = .01μF, R_D = 0Ω). Approximate oscillator frequency is defined by: $f = \frac{1}{C_T(0.7R_T + 3R_D)}$

7. DC transconductance (g_M) relates to DC open-loop voltage gain (A_V) according to the following equation: $A_V = g_M R_L$ where R_L is the resistance from pin 9 to ground.
The minimum g_M specification is used to calculate minimum A_V when the error amplifier output is loaded.

ELECTRICAL CHARACTERISTICS (+V_{IN} = 20V, and over operating temperature, unless otherwise specified)

PARAMETER	TEST CONDITIONS	UC1525A/UC2525A UC1527A/UC2527A			UC3525A UC3527A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
PWM Comparator								
Minimum Duty-Cycle				0			0	%
Maximum Duty-Cycle		45	49		45	49		%
Input Threshold (Note 6)	Zero Duty-Cycle	0.7	0.9		0.7	0.9		V
Input Threshold (Note 6)	Maximum Duty-Cycle		3.3	3.6		3.3	3.6	V
Input Bias Current (Note 5)			.05	1.0		.05	1.0	μA
Shutdown Section								
Soft Start Current	V_{SD} = 0V, V_{SS} = 0V	25	50	80	25	50	80	μA
Soft Start Low Level	V_{SD} = 2.5V		0.4	0.7		0.4	0.7	V
Shutdown Threshold	To outputs, V_{SS} = 5.1V, T_j = 25°C	0.6	0.8	1.0	0.6	0.8	1.0	V
Shutdown Input Current	V_{SD} = 2.5V		0.4	1.0		0.4	1.0	mA
Shutdown Delay (Note 5)	V_{SD} = 2.5V, T_j = 25°C		0.2	0.5		0.2	0.5	μS
Output Drivers (Each Output) (V_C = 20V)								
Output Low Level	I_{SINK} = 20mA		0.2	0.4		0.2	0.4	V
	I_{SINK} = 100mA		1.0	2.0		1.0	2.0	V
Output High Level	I_{SOURCE} = 20mA	18	19		18	19		V
	I_{SOURCE} = 100mA	17	18		17	18		V
Under-Voltage Lockout	V_{COMP} and V_{SS} = High	6	7	8	6	7	8	V
V_C OFF Current (Note 7)	V_C = 35V			200			200	μA
Rise Time (Note 5)	C_L = 1nF, T_j = 25°C		100	600		100	600	ns
Fall Time (Note 5)	C_L = 1nf, T_j =25°C		50	300		50	300	ns
Total Standby Current								
Supply Current	V_{IN} = 35V		14	20		14	20	mA

Notes: 5. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
6. Tested at f_{OSC} = 40KHz (R_T =3.6kΩ, C_T = 0.1μF, R_D = 0Ω).
7. Collector off-state quiescent current measured at pin 13 with outputs low for UC1525A and high for UC1527A.

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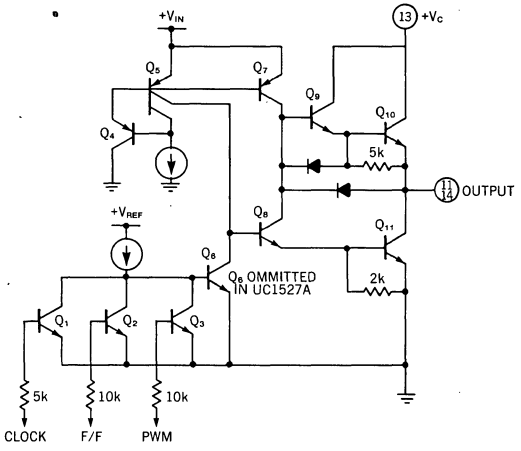
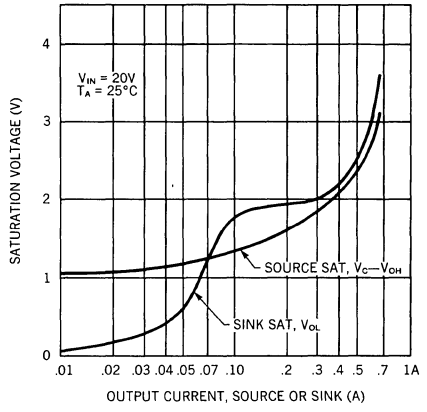
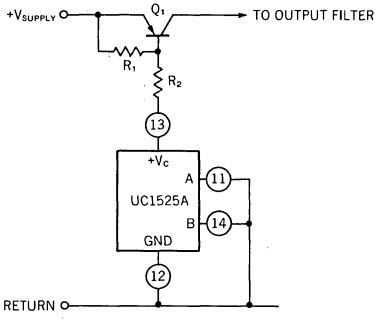
PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

UC1525A Output Circuit
(½ Circuit Shown)

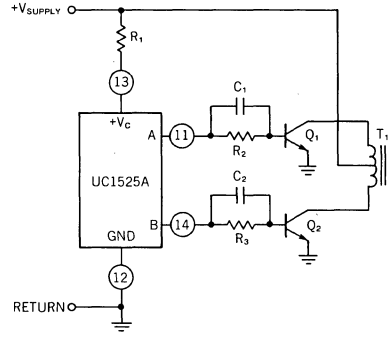


UC1525A Output Saturation Characteristics

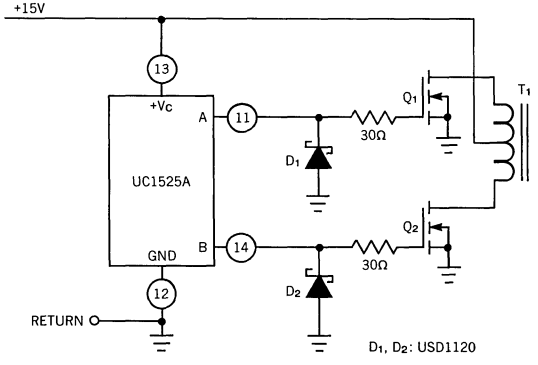




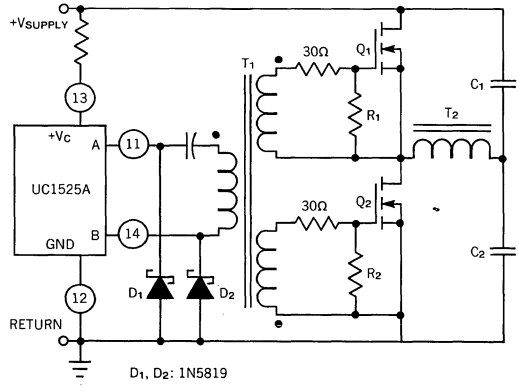
For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.



In conventional push-pull bipolar designs, forward base drive is controlled by R_1-R_3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C_1 and C_2.



The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.



Low power transformers can be driven by the UC1525A. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

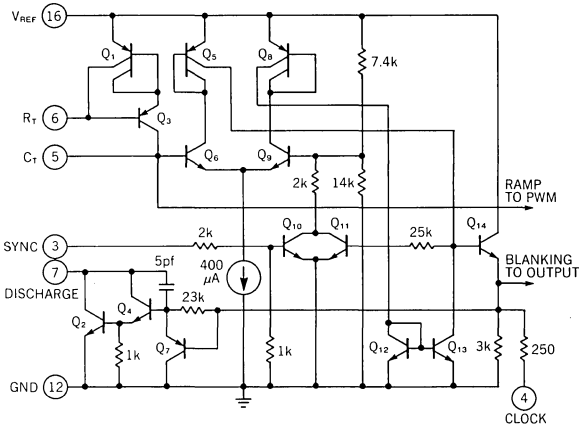
SHUTDOWN OPTIONS (See Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

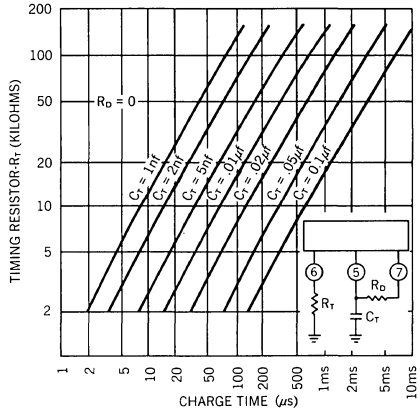
An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn-off signal to the outputs; and a 150μA current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

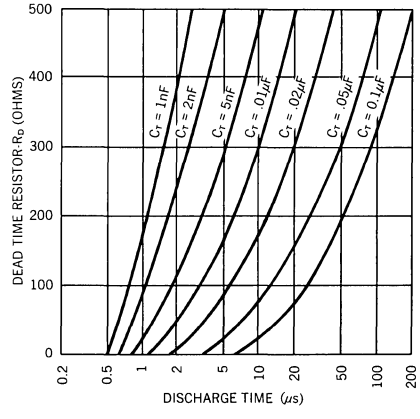
UC1525A Oscillator Schematic



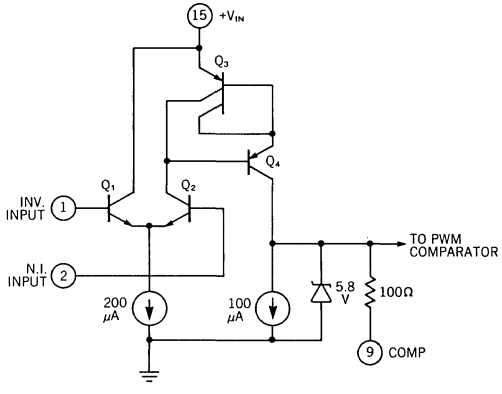
Oscillator Charge Time vs. R_T and C_T



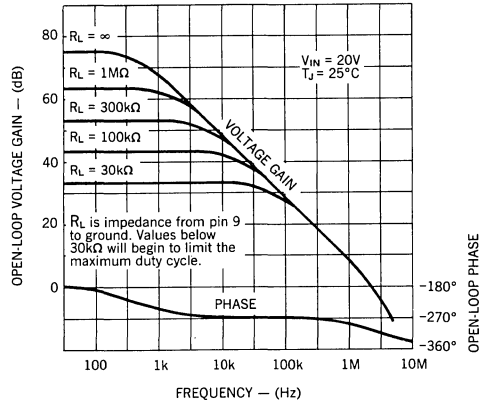
Oscillator Discharge Time vs. R_D and C_T



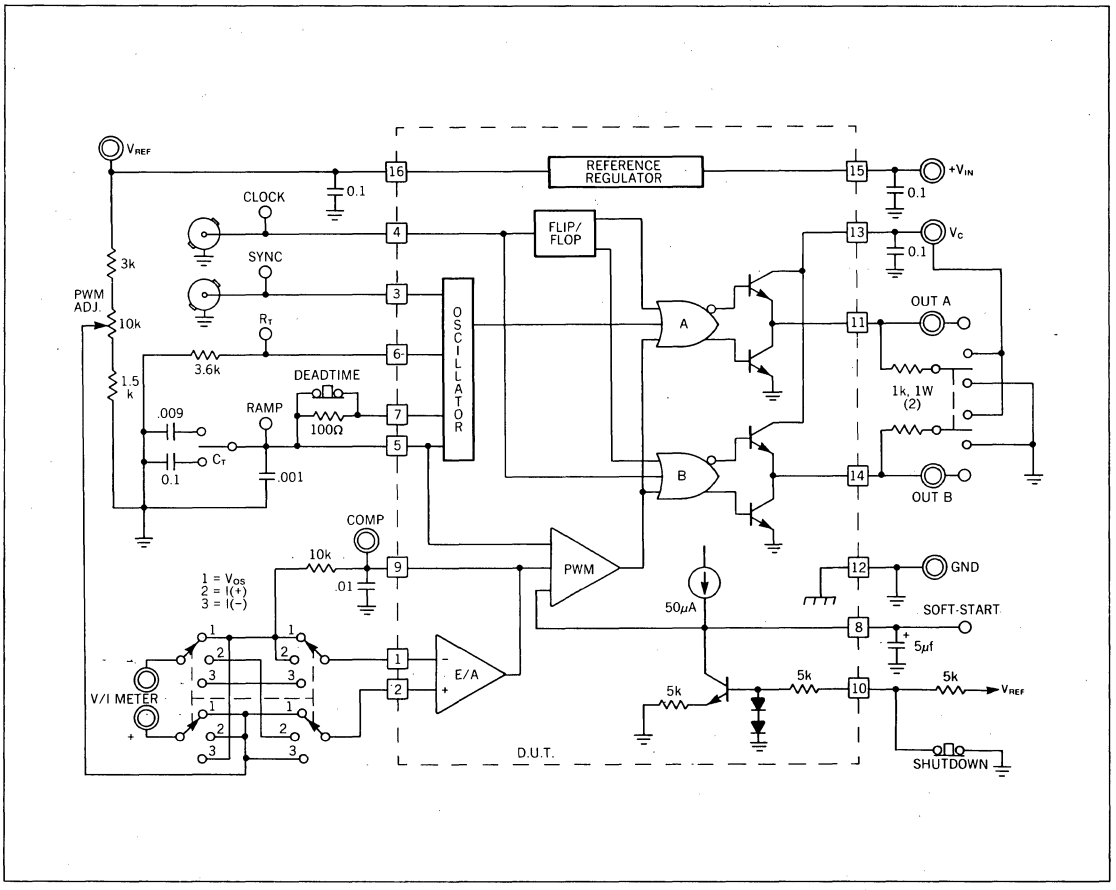
UC1525A Error Amplifier



Error Amplifier Voltage Gain and Phase vs Frequency

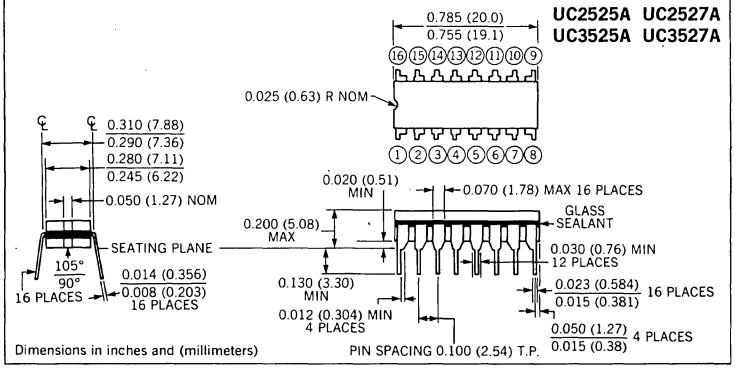


LAB TEST FIXTURE



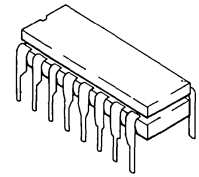
MECHANICAL SPECIFICATIONS

UC1525A UC1527A
UC2525A UC2527A
UC3525A UC3527A

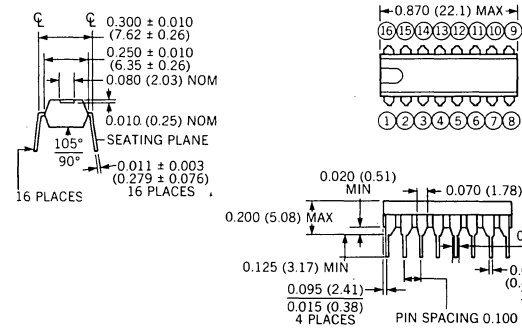


Dimensions in inches and (millimeters)

DIL-16 J CERAMIC

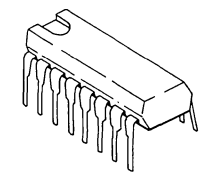


UC2525A UC2527A
UC3525A UC3527A



Dimensions in inches and (millimeters)

DIL-16 N PLASTIC



Note: When ordering, add suffix "J" (for 16 pin ceramic package) or "N" (for 16 pin plastic package) to the part number.

LINEAR INTEGRATED CIRCUITS

Regulating Pulse Width Modulator

UC1526A
UC2526A
UC3526A

FEATURES

- Reduced Supply Current
- Oscillator Frequency to 600KHz
- Precision Band-Gap Reference
- 7 to 35V Operation
- Dual 100mA Source/Sink Outputs
- Minimum Output Cross-Conduction
- Double-Pulse Suppression Logic
- Under-Voltage Lockout
- Programmable Soft-Start
- Thermal Shutdown
- TTL/CMOS Compatible Logic Ports

DESCRIPTION

The UC1526A Series are improved-performance pulse-width modulator circuits intended for direct replacement of equivalent non-"A" versions in all applications. Higher frequency operation has been enhanced by several significant improvements including: a more accurate oscillator with less minimum dead time, reduced circuit delays (particularly in current limiting), and an improved output stage with negligible cross-conduction current. Additional improvements include the incorporation of a precision, band-gap reference generator, reduced overall supply current, and the addition of thermal shutdown protection.

Along with these improvements, the UC1526A Series retains the protective features of under-voltage lockout, soft-start, digital current limiting, double pulse suppression logic, and adjustable deadtime. For ease of interfacing, all digital control ports are TTL compatible with active low logic.

These versatile devices may be used to implement single-ended or push-pull switching regulators of all topologies.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage ($+V_{IN}$) ..... +40V
Collector Supply Voltage ($+V_C$) ..... +40V
Logic Inputs ..... -0.3V to +5.5V
Analog Inputs ..... -0.3V to $+V_{IN}$
Source/Sink Load Current (each output) 200mA
Reference Load Current 50mA
Logic Sink Current 15mA
Power Dissipation at T_A = +25°C (Note 2) 1000mW
Thermal Resistance, Junction to Ambient ..... 100°C/W
Power Dissipation at T_C = +25°C (Note 3) 3000mW
Thermal Resistance, Junction to Case ..... 42°C/W
Operating Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

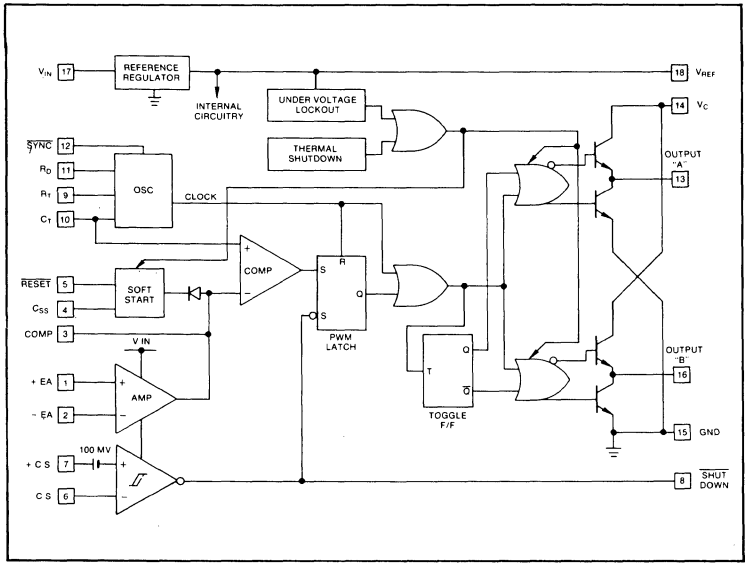
Notes: 1. Values beyond which damage may occur.
2. Derate at 10mW/°C for ambient temperatures above +50°C.
3. Derate at 24mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS (Note 4)

Input Voltage ..... +7V to +35V
Collector Supply Voltage ..... +4.5V to +35V
Sink/Source Load Current (each output) ..... 0 to 100mA
Reference Load Current ..... 0 to 20mA
Oscillator Frequency Range ..... 1Hz to 600kHz
Oscillator Timing Resistor ..... 2kΩ to 150kΩ
Oscillator Timing Capacitor ..... 400pF to 20μF
Available Deadtime Range at 40kHz ..... 1% to 50%
Operating Ambient Temperature Range
UC1526A ..... -55°C to +125°C
UC2526A ..... -25°C to +85°C
UC3526A ..... 0°C to +70°C

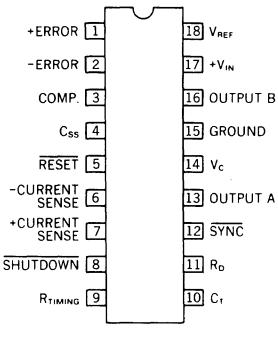
Note: 4. Range over which the device is functional and parameter limits are guaranteed.

BLOCK DIAGRAM



CONNECTION DIAGRAM

DIL-18 (TOP VIEW)
J or N PACKAGE



ELECTRICAL CHARACTERISTICS (+V_{IN} = 15V, and over operating ambient temperature, unless otherwise specified)

PARAMETER	TEST CONDITIONS	UC1526A/UC2526A			UC3526A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section (Note 5)								
Output Voltage	T_J = +25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	+V_{IN} = 7 to 35V		2	10		2	15	mV
Load Regulation	I_L = 0 to 20mA		5	20		5	20	mV
Temperature Stability	Over Operating T_J (Note 6)		15	50		15	50	mV
Total Output Voltage Range	Over Recommended Operating Conditions	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	V_{REF} = 0V	25	50	100	25	50	100	mA
Under-Voltage Lockout								
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 3.8V		0.2	0.4		0.2	0.4	V
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 4.7V	2.4	4.7		2.4	4.8		V
Oscillator Section (Note 7)								
Initial Accuracy	T_J = +25°C		±3	±8		±3	±8	%
Voltage Stability	+V_{IN} = 7 to 35V		0.5	1		0.5	1	%
Temperature Stability	Over Operating T_J (Note 6)		2	6		1	3	%
Minimum Frequency	R_T = 150kΩ, C_T = 20μF (Note 6)			1			1	Hz
Maximum Frequency	R_T = 2kΩ, C_T = 470pF	550			650			kHz
Sawtooth Peak Voltage	+V_{IN} = 35V		3.0	3.5		3.0	3.5	V
Sawtooth Valley Voltage	+V_{IN} = 7V	0.5	1.0		0.5	1.0		V
$\overline{\text{SYNC}}$ Pulse Width	T_J = 25°C, R_L = 2.7kΩ to V_{REF}		1.1			1.1		μs
Error Amplifier Section (Note 8)								
Input Offset Voltage	$R_S \leq$ 2kΩ		2	5		2	10	mV
Input Bias Current			-350	-1000		-350	-2000	nA
Input Offset Current			35	100		35	200	nA
DC Open Loop Gain	$R_L \geq$ 10 Meg Ω	64	72		60	72		dB
HIGH Output Voltage	Vpin1-Vpin2≥150mV, I_{source} = 100μA	3.6	4.2		3.6	4.2		V
LOW Output Voltage	Vpin2-Vpin1≥150mV, I_{sink} = 100μA		0.2	0.4		0.2	0.4	V
Common Mode Rejection	$R_S \leq$ 2kΩ	70	94		70	94		dB
Supply Voltage Rejection	+V_{IN} = 12 to 18V	66	80		66	80		dB
PWM Comparator (Note 7)								
Minimum Duty Cycle	$V_{compensation}$ = +0.4V			0			0	%
Maximum Duty Cycle	$V_{compensation}$ = +3.6V	45	49		45	49		%
Digital Ports ($\overline{\text{SYNC}}$, $\overline{\text{SHUTDOWN}}$, and $\overline{\text{RESET}}$)								
HIGH Output Voltage	I_{source} = 40μA	2.4	4.0		2.4	4.0		V
LOW Output Voltage	I_{sink} = 3.6mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	V_{IH} = +2.4V		-125	-200		-125	-200	μA
LOW Input Current	V_{IL} = +0.4V		-225	-360		-225	-360	μA
Shutdown Delay	From Pin 8, T_J = 25°C		160			160		ns

Notes: 5. I_L = 0mA.
6. Guaranteed by design, not 100% tested in production.
7. F_{OSC} = 40kHz (R_T = 4.12kΩ ± 1%, C_T = 0.01μF ± 1%, R_D = 0Ω)
8. V_{CM} = 0 to +5.2V

UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • TELEX 95-3040

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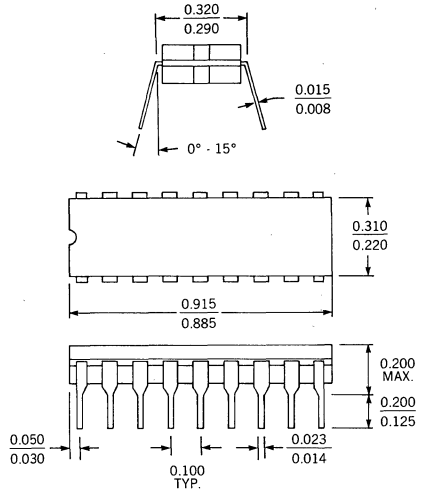
ELECTRICAL CHARACTERISTICS ($+V_{IN}$ = 15V, and over operating ambient temperature, unless otherwise specified)

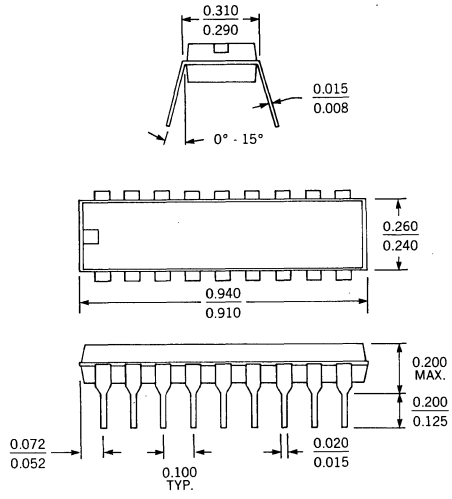
PARAMETER	TEST CONDITIONS	UC1526A/UC2526A			UC3526A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Current Limit Comparator (Note 9)								
Sense Voltage	$R_S \leq 50\Omega$	90	100	110	80	100	120	mV
Input Bias Current			-3	-10		-3	-10	μA
Shutdown Delay	From Pin 7, 100mV Overdrive, T_J = 25°C		260			260		nS
Soft-Start Section								
Error Clamp Voltage	$\overline{RESET}$ = +0.4V		0.1	0.4		0.1	0.4	V
C_S Charging Current	$\overline{RESET}$ = +2.4V	50	100	150	50	100	150	μA
Output Drivers (Each Output) (Note 10)								
HIGH Output Voltage	I_{source} = 20mA	12.5	13.5		12.5	13.5		V
	I_{source} = 100mA	12	13		12	13		V
LOW Output Voltage	I_{sink} = 20mA		0.2	0.3		0.2	0.3	V
	I_{sink} = 100mA		1.2	2.0		1.2	2.0	V
Collector Leakage	V_C = 40V		50	150		50	150	μA
Rise Time	C_L = 1000pF (Note 6)		0.3	0.6		0.3	0.6	μs
Fall Time	C_L = 1000pF (Note 6)		0.1	0.2		0.1	0.2	μs
Cross-Conduction Charge	Per cycle, T_J = 25°C		8			8		nC
Power Consumption (Note 11)								
Standby Current	$\overline{SHUTDOWN}$ = +0.4V		14	20		14	20	mA

Notes: 9. V_{CM} = 0 to +12V
10. V_C = +15V
11. $+V_{IN}$ = +35V, R_T = 4.12kΩ

PACKAGE DIMENSIONS



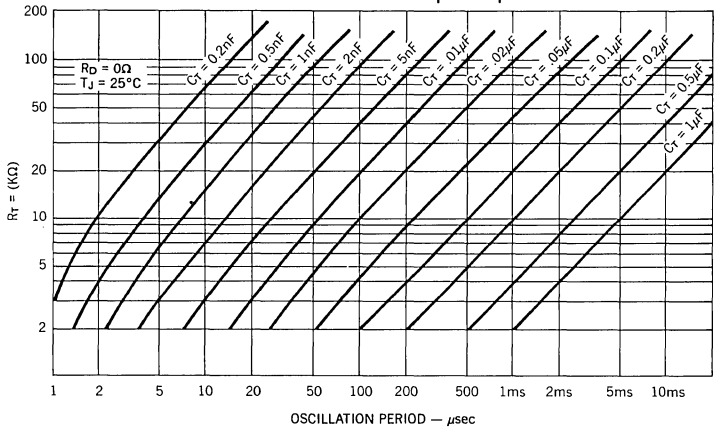
J Package
18-Pin Cerdip
Alloy 42 Leadframe



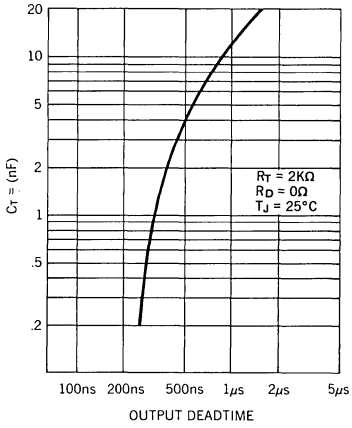
N Package
18-Pin Plastic Dip
Copper Alloy Leadframe

TYPICAL CHARACTERISTICS

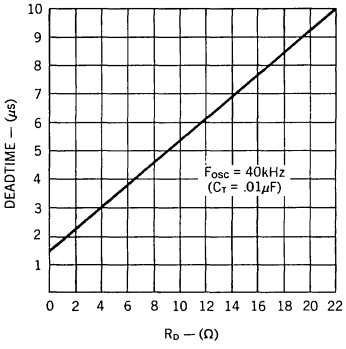
Oscillator Period vs R_T and C_T



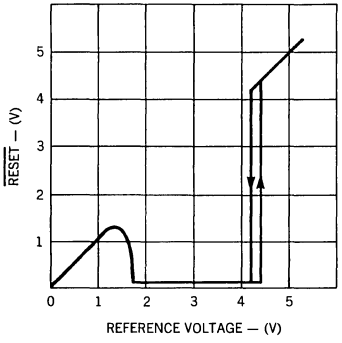
Output Blanking



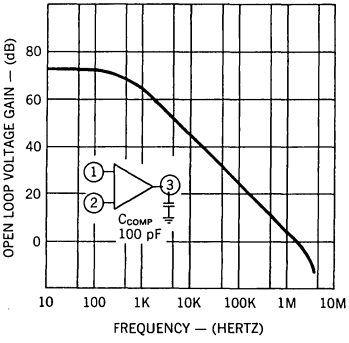
Output Driver Deadtime vs R_D Value



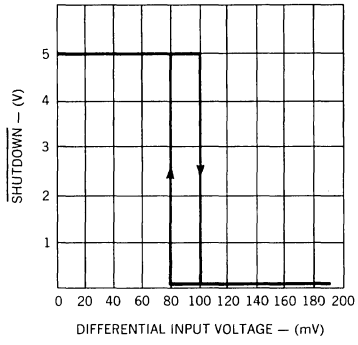
Under-Voltage Lockout Characteristic



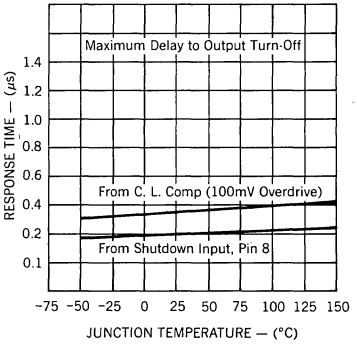
Error Amplifier Open Loop Gain vs Frequency



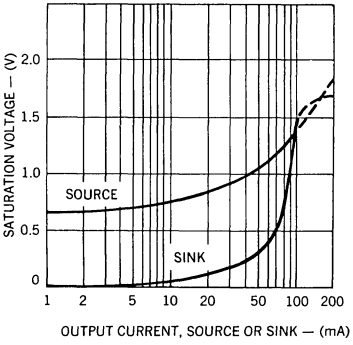
Current Limit Transfer Function



Shutdown Delay



Output Driver Saturation Voltage



APPLICATIONS INFORMATION

Voltage Reference

The reference regulator of the UC1526A is based on a precision band-gap reference, internally trimmed to ±1% accuracy. The circuitry is fully active at supply voltages above +7V, and provides up to 20mA of load current to external circuitry at +5.0V. In systems where additional current is required, an external PNP transistor can be used to boost the available current. A rugged low frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillations. Even so, some types of transistors may require collector-base capacitance for stability. Up to 1 amp of load current can be obtained with excellent regulation if the device selected maintains high current gain.

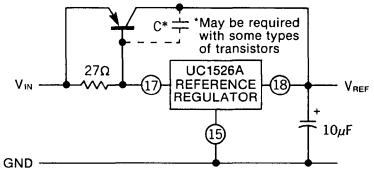


Figure 1. Extending Reference Output Current

Under-Voltage Lockout

The under-voltage lockout circuit protects the UC1526A and the power devices it controls from inadequate supply voltage. If $+V_{IN}$ is too low, the circuit disables the output drivers and holds the $\overline{RESET}$ pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a +1.2V bandgap reference and comparator circuit which is active when the reference voltage has risen to $3V_{BE}$ or +1.8V at 25°C. When the reference voltage rises to approximately +4.4V, the circuit enables the output drivers and releases the $\overline{RESET}$ pin, allowing a normal soft-start. The comparator has 350mV of hysteresis to minimize oscillation at the trip point. When $+V_{IN}$ to the PWM is removed and the reference drops to +4.2V, the under-voltage circuit pulls $\overline{RESET}$ LOW again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The UC1526A can operate from a +5V supply by connecting the V_{REF} pin to the $+V_{IN}$ pin and maintaining the supply between +4.8 and +5.2V.

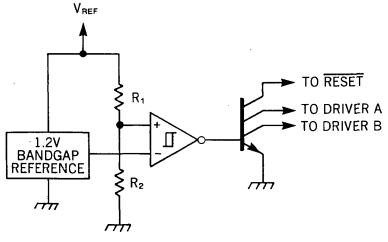


Figure 2. Under-Voltage Lockout Schematic

Soft-Start Circuit

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the UC1526A, the under-voltage lockout circuit holds $\overline{RESET}$ LOW with Q_3. Q_1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q_1 clamps the output of the error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, $\overline{RESET}$ will go HIGH. Q_1 turns off, allowing the internal 100μA current source to charge C_S. Q_2 clamps the error amplifier output to $1V_{BE}$ above the voltage on C_S. As the soft-start voltage ramps up to +5V, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for an error null.

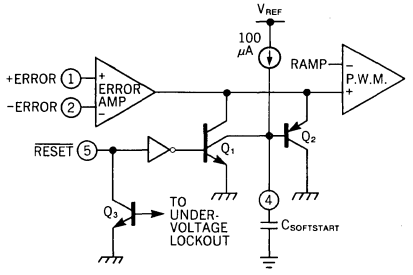


Figure 3. Soft-Start Circuit Schematic

Digital Control Ports

The three digital control ports of the UC1526A are bi-directional. Each pin can drive TTL and 5V CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector TTL, open-drain CMOS, and open-collector voltage comparators; fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is pulled LOW to activate the particular function. Driving $\overline{SYNC}$ LOW initiates a discharge cycle in the oscillator. Pulling $\overline{SHUTDOWN}$ LOW immediately inhibits all PWM output pulses. Holding $\overline{RESET}$ LOW discharges the soft-start capacitor. The logic threshold is +1.1V at +25°C. Noise immunity can be gained at the expense of fan-out with an external 2K pull-up resistor to +5V.

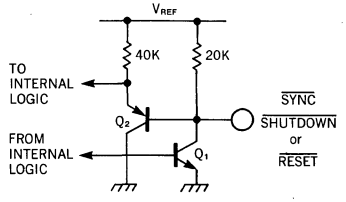


Figure 4. Digital Control Port Schematic

Oscillator

The oscillator is programmed for frequency and dead time with three components: R_T, C_T and R_D. Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With $R_D = 0\Omega$ (pin 11 shorted to ground) select values for R_T and C_T from the graph on page 4 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the $+V_C$ terminal is the same as the oscillator frequency.
2. If more dead time is required, select a larger value of R_D. At 40kHz dead time increases by 400ns/Ω.
3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of R_T slightly to bring the frequency back to the nominal design value.

The UC1526A can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the sync frequency. A periodic LOW logic pulse approximately 0.5μs wide at the $\overline{SYNC}$ pin will then lock the oscillator to the external frequency.

Multiple devices can be synchronized together by programming one master unit for the desired frequency, and then sharing its sawtooth and clock waveforms with the slave units. All C_T terminals are connected to the C_T pin of the master, and all $\overline{SYNC}$ terminals are likewise connected to the $\overline{SYNC}$ pin of the master. Slave R_T terminals are left open or connected to V_{REF}. Slave R_D terminals may be either left open or grounded.

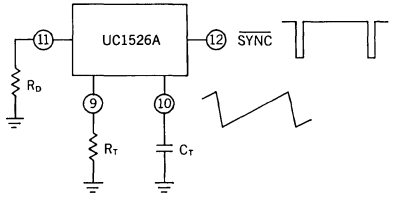


Figure 5. Oscillator Connections and Waveforms

Error Amplifier

The error amplifier is a transconductance design, with an output impedance of 2MΩ. Since all voltage gain takes place at the output pin, the open-loop gain/frequency characteristics can be controlled with shunt reactance to ground. When compensated for unity-gain stability with 100pF, the amplifier has an open-loop pole at 800Hz.

The input connections to the error amplifier are determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0V and the feedback connections in Figure 6A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0V reference voltage, as shown in Figure 6B.

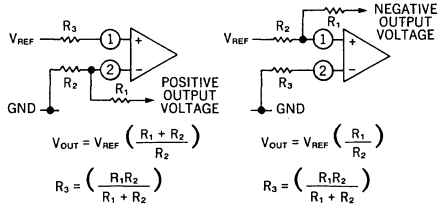


Figure 6. Error Amplifier Connections

Output Drivers

The totem-pole output drivers of the UC1526A are designed to source and sink 100mA continuously and 200mA peak. Loads can be driven either from the output pins 13 and 16, or from the $+V_C$, as required.

Since the bottom transistor of the totem-pole is allowed to saturate, there is a momentary conduction path from the $+V_C$ terminal to ground during switching; however, improved design has limited this cross-conduction period to less than 50ns. Capacitor decoupling at V_C is recommended and careful grounding of Pin 15 is needed to insure that high peak sink currents from a capacitive load do not cause ground transients.

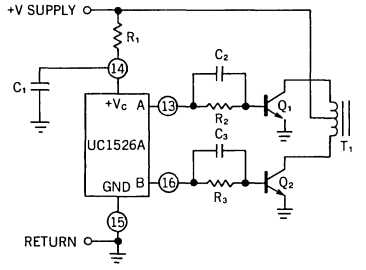


Figure 7. Push-Pull Configuration

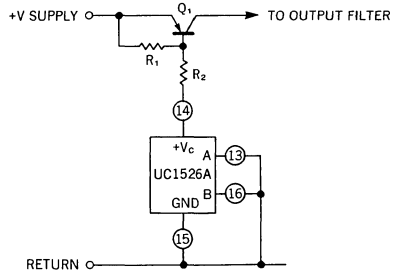


Figure 8. Single-Ended Configuration

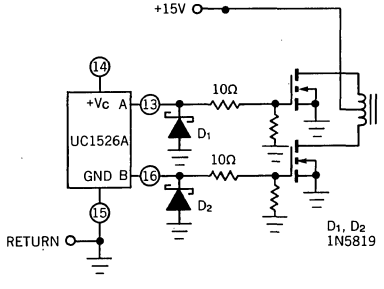


Figure 9. Driving N-Channel Power Mosfets

LINEAR INTEGRATED CIRCUITS

Regulating Pulse Width Monitor

UC1526
UC2526
UC3526

FEATURES

- 8 to 35V operation
- 5V reference trimmed to ±1%
- 1Hz to 400kHz oscillator range
- Dual 100mA source/sink outputs
- Digital current limiting
- Double pulse suppression
- Programmable deadtime
- Under-voltage lockout
- Single pulse metering
- Programmable soft-start
- Wide current limit common mode range
- TTL/CMOS compatible logic ports
- Symmetry correction capability
- Guaranteed 6 unit synchronization

DESCRIPTION

The UC1526 is a high performance monolithic pulse width modulator circuit designed for fixed-frequency switching regulators and other power control applications. Included in an 18-pin dual-in-line package are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two low impedance power drivers. Also included are protective features such as soft-start and under-voltage lockout, digital current limiting, double pulse inhibit, a data latch for single pulse metering, adjustable deadtime, and provision for symmetry correction inputs. For ease of interface, all digital control ports are TTL and B-series CMOS compatible. Active LOW logic design allows wired-OR connections for maximum flexibility. This versatile device can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer coupled. The UC1526 is characterized for operation over the full military temperature range of −55°C to +125°C. The UC2526 is characterized for operation from −25°C to +85°C, and the UC3526 is characterized for operation from 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage ($+V_{IN}$) ..... +40V
Collector Supply Voltage ($+V_C$) ..... +40V
Logic Inputs ..... −0.3V to +5.5V
Analog Inputs ..... −0.3V to $+V_{IN}$
Source/Sink Load Current (each output) 200mA
Reference Load Current 50mA
Logic Sink Current 15mA
Power Dissipation at T_A = +25°C (Note 2) 1000mW
Thermal Resistance, Junction to Ambient ..... 100°C/W
Power Dissipation at T_C = +25°C (Note 3) 3000mW
Thermal Resistance, Junction to Case ..... 42°C/W
Operating Junction Temperature ..... +150°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

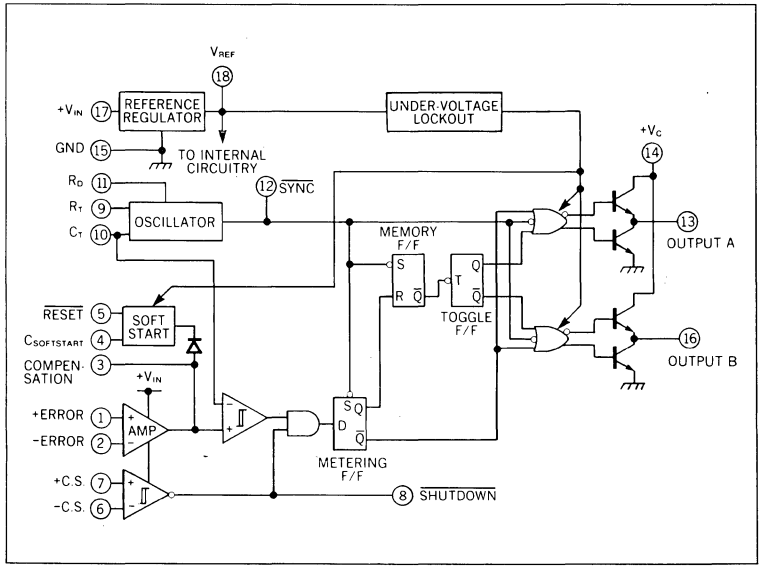
Notes: 1. Values beyond which damage may occur.
2. Derate at 10mW/°C for ambient temperatures above +50°C.
3. Derate at 24mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS (Note 4)

Input Voltage ..... +8V to +35V
Collector Supply Voltage ..... +4.5V to +35V
Sink/Source Load Current (each output) ..... 0 to 100mA
Reference Load Current ..... 0 to 20mA
Oscillator Frequency Range ..... 1Hz to 400kHz
Oscillator Timing Resistor ..... 2kΩ to 150kΩ
Oscillator Timing Capacitor ..... 1nF to 20μF
Available Deadtime Range at 40kHz ..... 3% to 50%
Operating Ambient Temperature Range
UC1526 ..... −55°C to +125°C
UC2526 ..... −25°C to +85°C
UC3526 ..... 0°C to +70°C

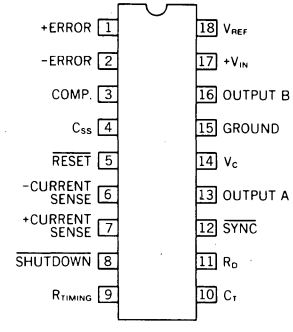
Note: 4. Range over which the device is functional and parameter limits are guaranteed.

BLOCK DIAGRAM



CONNECTION DIAGRAM

DIL-18 (TOP VIEW)
J or N PACKAGE



ELECTRICAL CHARACTERISTICS (+V_{IN} = 15V, and over operating ambient temperature, unless otherwise specified)

PARAMETER	TEST CONDITIONS	UC1526/UC2526			UC3526			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section (Note 5)								
Output Voltage	T_J = +25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	+V_{IN} = 8 to 35V		10	20		10	30	mV
Load Regulation	I_L = 0 to 20mA		10	30		10	50	mV
Temperature Stability	Over Operating T_J		15	50		15	50	mV
Total Output Voltage Range	Over Recommended Operating Conditions	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	V_{REF} = 0V	25	50	100	25	50	100	mA
Under-Voltage Lockout								
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 3.8V		0.2	0.4		0.2	0.4	V
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 4.8V	2.4	4.8		2.4	4.8		V
Oscillator Section (Note 6)								
Initial Accuracy	T_J = +25°C		±3	±8		±3	±8	%
Voltage Stability	+V_{IN} = 8 to 35V		0.5	1		0.5	1	%
Temperature Stability	Over Operating T_J		7	10		3	5	%
Minimum Frequency	R_T = 150kΩ, C_T = 20μF			1			1	Hz
Maximum Frequency	R_T = 2kΩ, C_T = 1.0nF	400			400			kHz
Sawtooth Peak Voltage	+V_{IN} = 35V		3.0	3.5		3.0	3.5	V
Sawtooth Valley Voltage	+V_{IN} = 8V	0.5	1.0		0.5	1.0		V
Error Amplifier Section (Note 7)								
Input Offset Voltage	$R_S \leq$ 2kΩ		2	5		2	10	mV
Input Bias Current			-350	-1000		-350	-2000	nA
Input Offset Current			35	100		35	200	nA
DC Open Loop Gain	$R_L \geq$ 10 Meg Ω	64	72		60	72		dB
HIGH Output Voltage	Vpin1−Vpin2≥150mV, I_{source} = 100μA	3.6	4.2		3.6	4.2		V
LOW Output Voltage	Vpin2−Vpin1≥150mV, I_{sink} = 100μA		0.2	0.4		0.2	0.4	V
Common Mode Rejection	$R_S \leq$ 2kΩ	70	94		70	94		dB
Supply Voltage Rejection	+V_{IN} = 12 to 18V	66	80		66	80		dB
PWM Comparator (Note 6)								
Minimum Duty Cycle	$V_{compensation}$ = +0.4V			0			0	%
Maximum Duty Cycle	$V_{compensation}$ = +3.6V	45	49		45	49		%
Digital Ports ($\overline{\text{SYNC}}$, $\overline{\text{SHUTDOWN}}$, and $\overline{\text{RESET}}$)								
HIGH Output Voltage	I_{source} = 40μA	2.4	4.0		2.4	4.0		V
LOW Output Voltage	I_{sink} = 3.6mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	V_{IH} = +2.4V		-125	-200		-125	-200	μA
LOW Input Current	V_{IL} = +0.4V		-225	-360		-225	-360	μA

Notes: 5. I_L = 0mA.
6. F_{OSC} = 40kHz (R_T = 4.12kΩ ± 1%, C_T = .01μF ± 1%, R_D = 0Ω
7. V_{CM} = 0 to +5.2V

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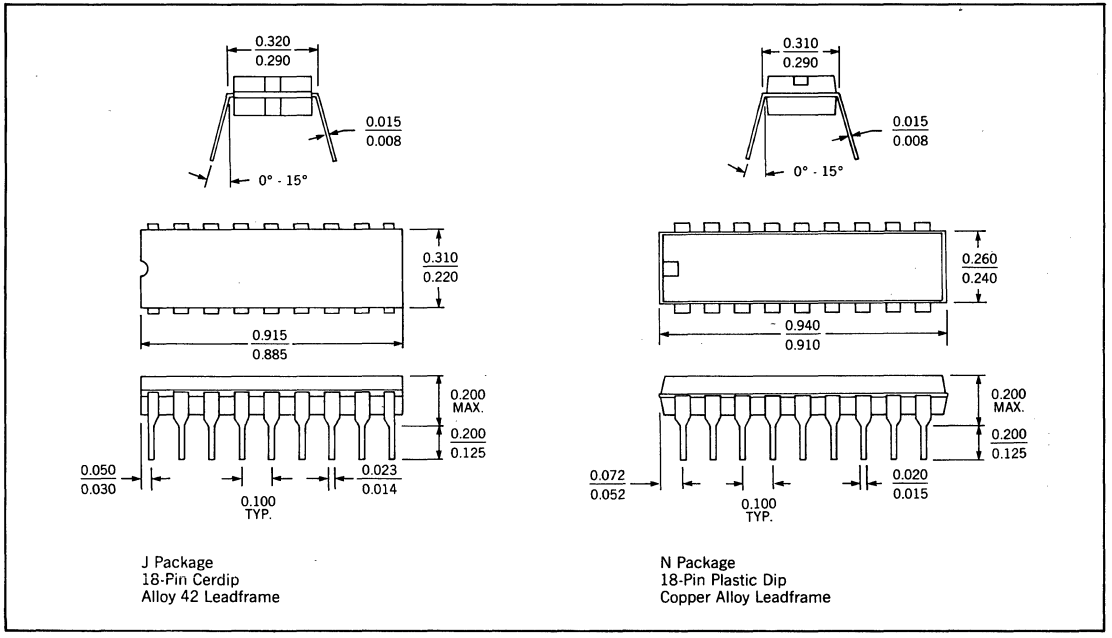
ELECTRICAL CHARACTERISTICS ($+V_{IN}$ = 15V, and over operating ambient temperature, unless otherwise specified)

PARAMETER	TEST CONDITIONS	UC1526/UC2526			UC3526			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Current Limit Comparator (Note 8)								
Sense Voltage	$R_S \leq 50\Omega$	90	100	110	80	100	120	mV
Input Bias Current			-3	-10		-3	-10	μA
Soft-Start Section								
Error Clamp Voltage	$\overline{RESET}$ = +0.4V		0.1	0.4		0.1	0.4	V
C_S Charging Current	$\overline{RESET}$ = +2.4V	50	100	150	50	100	150	μA
Output Drivers (Each Output) (Note 9)								
HIGH Output Voltage	I_{source} = 20mA	12.5	13.5		12.5	13.5		V
	I_{source} = 100mA	12	13		12	13		V
LOW Output Voltage	I_{sink} = 20mA		0.2	0.3		0.2	0.3	V
	I_{sink} = 100mA		1.2	2.0		1.2	2.0	V
Collector Leakage	V_C = 40V		50	150		50	150	μA
Rise Time	C_L = 1000pF		0.3	0.6		0.3	0.6	μs
Fall Time	C_L = 1000pF		0.1	0.2		0.1	0.2	μs
Power Consumption (Note 10)								
Standby Current	$\overline{SHUTDOWN}$ = +0.4V		18	30		18	30	mA

Notes: 8. V_{CM} = 0 to +12V
9. V_C = +15V
10. $+V_{IN}$ = +35V, R_T = 4.12kΩ

PACKAGE DIMENSIONS



J Package
18-Pin Cerdip
Alloy 42 Leadframe

N Package
18-Pin Plastic Dip
Copper Alloy Leadframe

APPLICATIONS INFORMATION

Voltage Reference

The reference regulator of the UC1526 is based on a temperature compensated zener diode. The circuitry is fully active at supply voltages above +8V, and provides up to 20mA of load current to external circuitry at +5.0V. In systems where additional current is required, an external PNP transistor can be used to boost the available current. A rugged low frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillations. Even so, some types of transistors may require collector-base capacitance for stability. Up to 1 amp of load current can be obtained with excellent regulation if the device selected maintains high current gain.

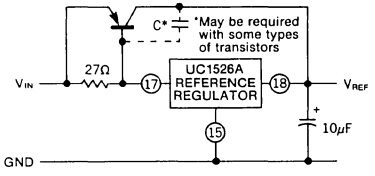


Figure 1. Extending Reference Output Current

Under-Voltage Lockout

The under-voltage lockout circuit protects the UC1526 and the power devices it controls from inadequate supply voltage. If $+V_{IN}$ is too low, the circuit disables the output drivers and holds the $\overline{RESET}$ pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a +1.2V bandgap reference and comparator circuit which is active when the reference voltage has risen to $3V_{BE}$ or +1.8V at 25°C. When the reference voltage rises to approximately +4.4V, the circuit enables the output drivers and releases the $\overline{RESET}$ pin, allowing a normal soft-start. The comparator has 200mV of hysteresis to minimize oscillation at the trip point. When $+V_{IN}$ to the PWM is removed and the reference drops to +4.2V, the under-voltage circuit pulls $\overline{RESET}$ LOW again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The UC1526 can operate from a +5V supply by connecting the V_{REF} pin to the $+V_{IN}$ pin and maintaining the supply between +4.8 and +5.2V.

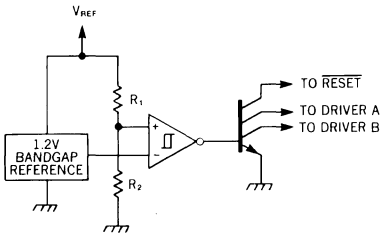


Figure 2. Under-Voltage Lockout Schematic

Soft-Start Circuit

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the UC1526, the under-voltage lockout circuit holds $\overline{RESET}$ LOW with Q_3. Q_1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q_1 clamps the output of the error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, $\overline{RESET}$ will go HIGH. Q_1 turns off, allowing the internal 100μA current source to charge C_S. Q_2 clamps the error amplifier output to $1V_{BE}$ above the voltage on C_S. As the soft-start voltage ramps up to +5V, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for an error null.

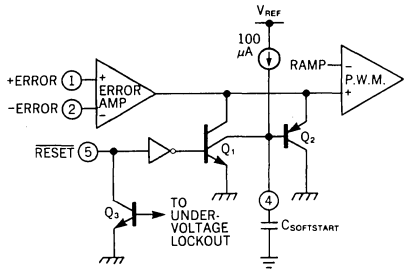


Figure 3. Soft-Start Circuit Schematic

Digital Control Ports

The three digital control ports of the UC1526 are bi-directional. Each pin can drive TTL and 5V CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector TTL, open-drain CMOS, and open-collector voltage comparators; fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is pulled LOW to activate the particular function. Driving $\overline{SYNC}$ LOW initiates a discharge cycle in the oscillator. Pulling $\overline{SHUTDOWN}$ LOW immediately inhibits all PWM output pulses. Holding $\overline{RESET}$ LOW discharges the soft-start capacitor. The logic threshold is +1.1V at +25°C. Noise immunity can be gained at the expense of fan-out with an external 2K pull-up resistor to +5V.

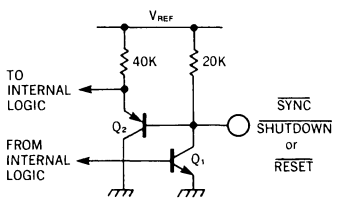


Figure 4. Digital Control Port Schematic

Oscillator

The oscillator is programmed for frequency and dead time with three components: R_T, C_T and R_D. Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With $R_D = 0\Omega$ (pin 11 shorted to ground) select values for R_T and C_T from Figure 7 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the $+V_C$ terminal is the same as the oscillator frequency.
2. If more dead time is required, select a large value of R_D. At 40kHz dead time increases by 400nS/Ω.
3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of R_T slightly to bring the frequency back to the nominal design value.

The UC1526 can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the sync frequency. A periodic LOW logic pulse approximately 0.5μs wide at the $\overline{SYNC}$ pin will then lock the oscillator to the external frequency.

Multiple devices can be synchronized together by programming one master unit for the desired frequency, and then sharing its sawtooth and clock waveforms with the slave units. All C_T terminals are connected to the C_T pin of the master, and all $\overline{SYNC}$ terminals are likewise connected to the $\overline{SYNC}$ pin of the master. Slave R_T terminals are left open or connected to V_{REF}. Slave R_D terminals may be either left open or grounded.

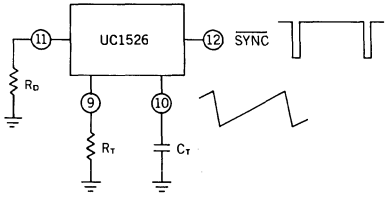


Figure 5. Oscillator Connections and Waveforms

Error Amplifier

The error amplifier is a transconductance design, with an output impedance of 2MΩ. Since all voltage gain takes place at the output pin, the open-loop gain/frequency characteristics can be controlled with shunt reactance to ground. When compensated for unity-gain stability with 100pF, the amplifier has an open-loop pole at 800Hz.

The input connections to the error amplifier are determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0V and the feedback connections in Figure 6A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0V reference voltage, as shown in Figure 6B.

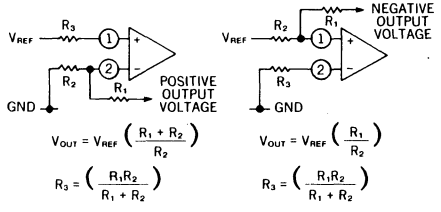


Figure 6. Error Amplifier Connections

Output Drivers

The totem-pole output drivers of the UC1526 are designed to source and sink 100mA continuously and 200mA peak. Loads can be driven either from the output pins 13 and 16, or from the $+V_C$, as required.

Since the bottom transistor of the totem-pole is allowed to saturate, there is a momentary conduction path from the $+V_C$ terminal to ground during switching. To limit the resulting current spikes a small resistor in series with pin 14 is always recommended. The resistor value is determined by the driver supply voltage, and should be chosen for 200mA peak currents.

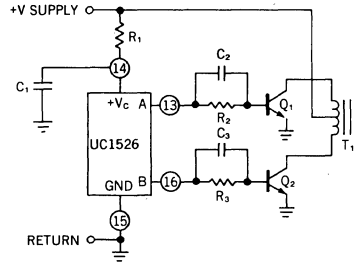


Figure 7. Push-Pull Configuration

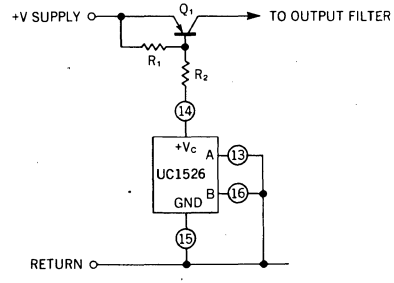


Figure 8. Single-Ended Configuration

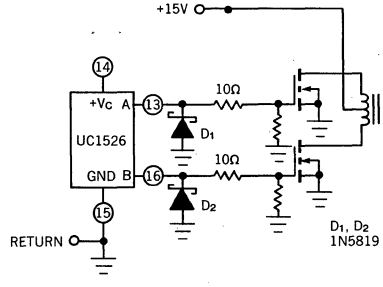


Figure 9. Driving N-Channel Power Mosfets

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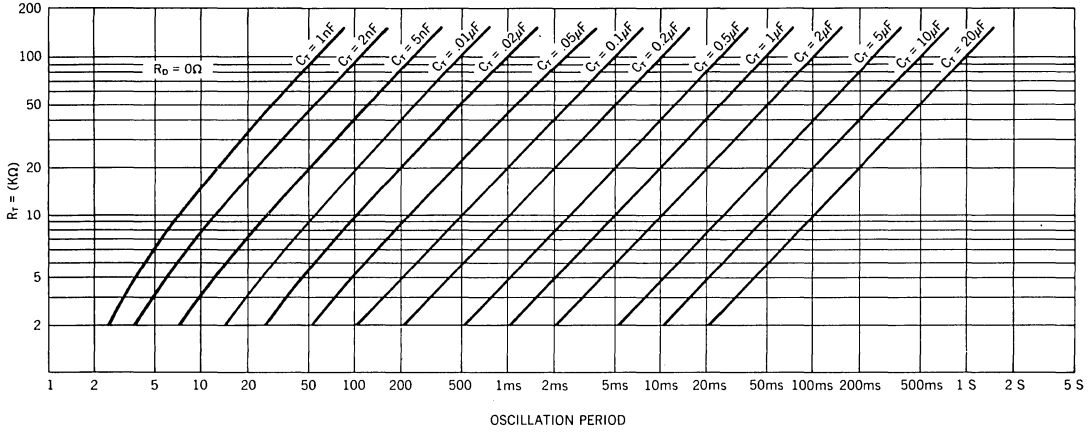
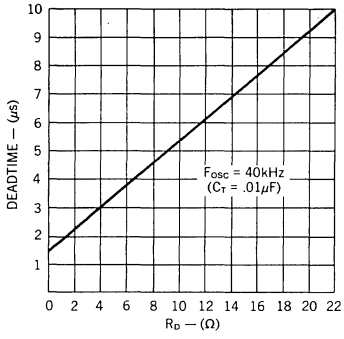
TYPICAL CHARACTERISTICS

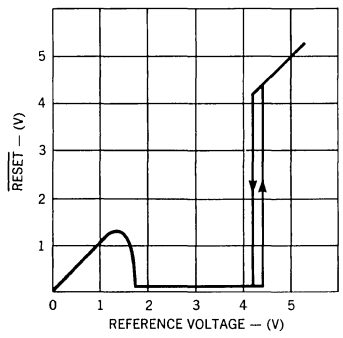
Oscillator Period vs R_T and C_T



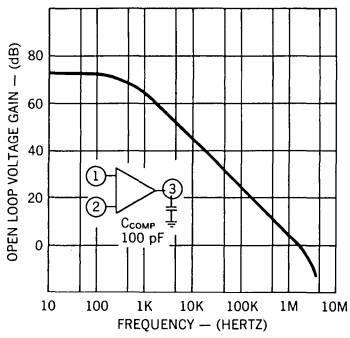
Output Driver Deadtime vs R_D Value



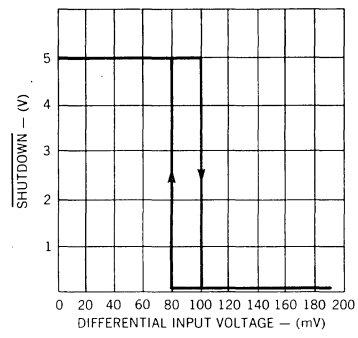
Under-Voltage Lockout Characteristic



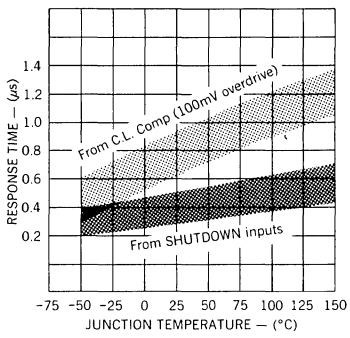
Error Amplifier Open Loop Gain vs Frequency



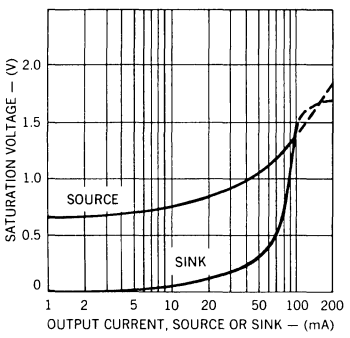
Current Limit Transfer Function



Shutdown Delay



Output Driver Saturation Voltage



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LINEAR INTEGRATED CIRCUITS

Power Supply Supervisory Circuit

UC1543 UC1544
UC2543 UC2544
UC3543 UC3544

FEATURES

- Includes over-voltage, under-voltage, and current sensing circuits
- Internal 1% accurate reference
- Programmable time delays
- SCR "crowbar" drive of 300mA
- Remote activation capability
- Optional over-voltage latch
- Uncommitted comparator inputs for low voltage sensing (UC1544 series only)

DESCRIPTION

These monolithic integrated circuits contain all the functions necessary to monitor and control the output of a sophisticated power supply system. Over-voltage (O.V.) sensing with provision to trigger an external SCR "crowbar" shutdown; an under-voltage (U.V.) circuit which can be used to monitor either the output or to sample the input line voltage; and a third op amp/comparator usable for current sensing (C.L.) are all included in this IC, together with an independent, accurate reference generator.

Both over- and under-voltage sensing circuits can be externally programmed for minimum time duration of fault before triggering. All functions contain open collector outputs which can be used independently or wire-or'ed together, and although the SCR trigger is directly connected only to the over-voltage sensing circuit, it may be optionally activated by any of the other outputs, or from an external signal. The O.V. circuit also includes an optional latch and external reset capability.

The UC1544/2544/3544 devices have the added versatility of completely uncommitted inputs to the voltage sensing comparators so that levels less than 2.5V may be monitored by dividing down the internal reference voltage.

The current sense circuit may be used with external compensation as a linear amplifier or as a high-gain comparator. Although nominally set for zero input offset, a fixed threshold may be added with an external resistor. Instead of current limiting, this circuit may also be used as an additional voltage monitor.

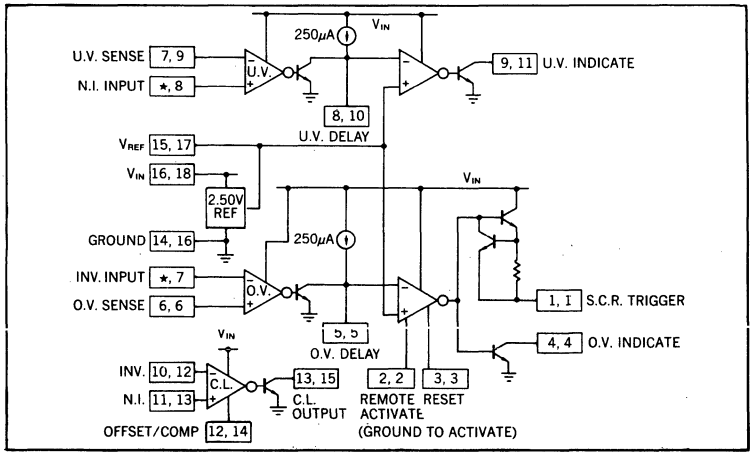
The reference generator circuit is internally trimmed to eliminate the need for external potentiometers and the entire circuit may be powered directly from either the output being monitored or from a separate bias voltage.

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, V_{IN} 40V
Sense Inputs, Voltage Range ..... 0 to V_{IN}
SCR Trigger Current ..... -600mA*
Indicator Output Voltage 40V
Indicator Output Sink Current 50mA
Power Dissipation (Package Limitation) 1000mW
Derate Above 25°C ..... 8.0mW/°C
Operating Temperature Range
UC1543, UC1544 ..... -55°C to +125°C
UC2543, UC2544 ..... -25°C to +85°C
UC3543, UC3544 ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C

*At higher input voltages, a dissipation limiting resistor, R_G, is required.
Note: Currents are positive-into, negative-out of the specified terminal.

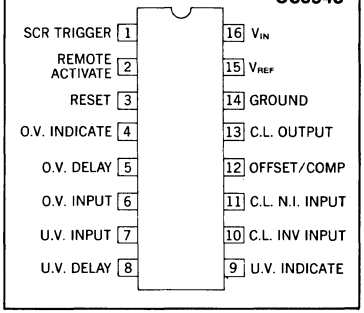
BLOCK DIAGRAM



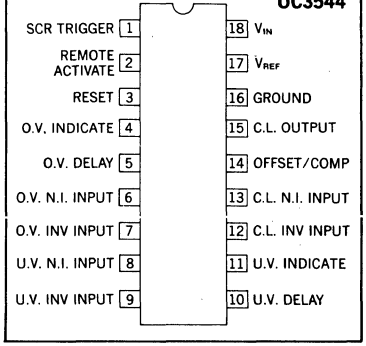
Note: For each terminal, first number refers to 1543 series, second to 1544 series.
★ On 1543 series, this function is internally connected to V_{REF}.

CONNECTION DIAGRAMS

DIL-16 (TOP VIEW) **UC1543**
J or N PACKAGE **UC2543**
UC3543



DIL-18 (TOP VIEW) **UC1544**
J or N PACKAGE **UC2544**
UC3544



UNITRODE

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1543 & UC1544; −25°C to +85°C for the UC2543 & UC2544; and 0°C to +70°C for the UC3543 & UC3544; and for V_{IN} = 5 to 35V. Electrical tests are performed with V_{IN} = 10V and 2kΩ pull-up resistors on all indicator outputs. All electrical ratings and specifications for the UC1544, UC2544 & UC3544 devices are tested with the inverting over-voltage input and the non-inverting under-voltage input externally connected to the 2.5V reference.)

PARAMETER	TEST CONDITIONS	UC1543/UC2543 UC1544/UC2544			UC3543 UC3544			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Voltage Range	T_J = 25°C to T_{MAX}	4.5		40	4.5		40	V
Input Voltage Range	T_{MIN} to T_{MAX}	4.7		40	4.7		40	V
Supply Current	V_{IN} = 40V, Outputs Open		7	10		7	10	mA
Reference Section								
Output Voltage	T_J = 25°C	2.48	2.50	2.52	2.45	2.50	2.55	V
Output Voltage	Over Temperature Range	2.45		2.55	2.40		2.60	V
Line Regulation	V_{IN} = 5 to 30V		1	5		1	5	mV
Load Regulation	I_{REF} = 0 to 10mA		1	10		1	10	mV
Short Circuit Current	V_{REF} = 0	−12	−20	−40	−12	−20	−40	mA
Temperature Stability			50			50		ppm/°C
SCR Trigger Section								
Peak Output Current	V_{IN} = 5V, R_G = 0, V_O = 0	−100	−300	−600	−100	−300	−600	mA
Peak Output Voltage	V_{IN} = 15V, I_O = −100mA	12	13		12	13		V
Output Off Voltage	V_{IN} = 40V		0	0.1		0	0.1	V
Remote Activate Current	R/A Pin = Gnd		−0.4	−0.8		−0.4	−0.8	mA
Remote Activate Voltage	R/A Pin Open		2	6		2	6	V
Reset Current	Reset = Gnd, R/A = Gnd		−0.4	−0.8		−0.4	−0.8	mA
Reset Voltage	Reset Open, R/A = Gnd		2	6		2	6	V
Output Current Rise Time	R_L = 50Ω, T_J = 25°C, C_D = 0		400			400		mA/μs
Prop. Delay from R/A			300			300		ns
Prop. Delay from O/V input			500			500		ns
Comparator Sections								
Input Threshold (Input voltage rising on O.V. and falling on U.V.)	T_J = 25°C	2.45	2.50	2.55	2.40	2.50	2.60	V
	Over Temperature Range	2.40		2.60	2.35		2.65	V
Input Hysteresis			25			25		mV
Input Bias Current	Sense Input = 0V		−0.3	−1.0		−0.3	−1.0	μA
Delay Saturation			0.2	0.5		0.2	0.5	V
Delay High Level			6	7		6	7	V
Delay Charging Current	V_D = 0	−200	−250	−300	−200	−250	−300	μA
Indicate Saturation	I_L = 10mA		0.2	0.5		0.2	0.5	V
Indicate Leakage	V_{IND} = 40V		.01	1.0		.01	1.0	μA
Propagation Delay	Input Overdrive = 200mV, T_J = 25°C, C_D = 0		400			400		ns
	Input Overdrive = 200mV, T_J = 25°C, C_D = 1μF		10			10		ms
Current Limit Section								
Input Voltage Range		0		(V_{IN}−3V)	0		(V_{IN}−3V)	V
Input Bias Current	Offset Pin Open, V_{CM} = 0		−0.3	−1.0		−0.3	−1.0	μA
Input Offset Voltage	Offset Pin Open, V_{CM} = 0		0	10		0	10	mV
Input Offset Voltage	10kΩ from Offset Pin to Gnd	80	100	120	80	100	120	mV
CMRR	0 ≤ V_{CM} ≤ 12V, V_{IN} = 15V	60	70		60	70		dB
AVOL	Offset Pin Open, V_{CM} = 0V	72	80		72	80		dB
Output Saturation	I_L = 10mA		0.2	0.5		0.2	0.5	V
Output Leakage	V_{IND} = 40V		.01	1.0		.01	1.0	μA
Small Signal Bandwidth	A_V = 0dB, T_J = 25°C		5			5		MHz
Propagation Delay	$V_{overdrive}$ = 100mV, T_J = 25°C		200			200		ns

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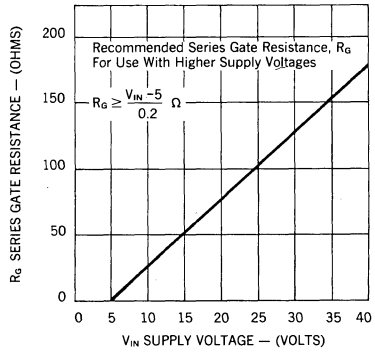
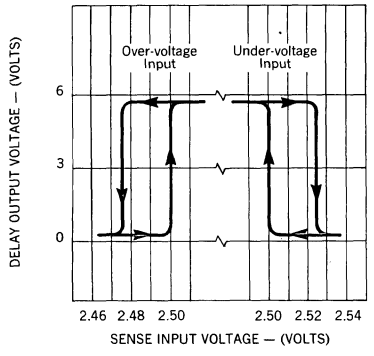
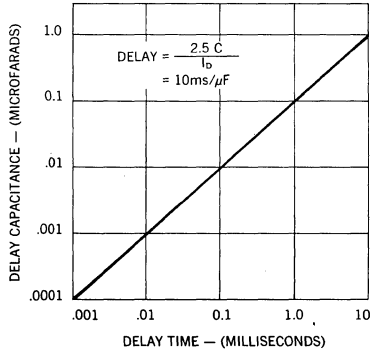
SCR Trigger Power Limiting



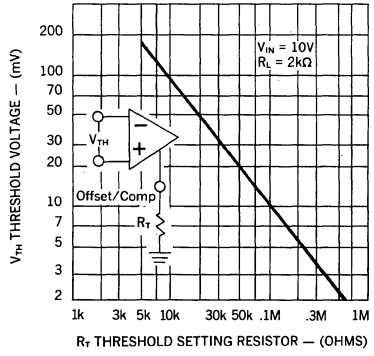
Comparator Input Hysteresis



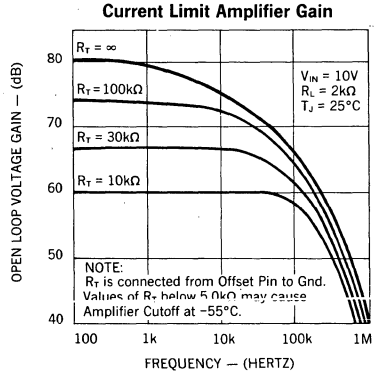
Activation Delay vs Capacitor Value



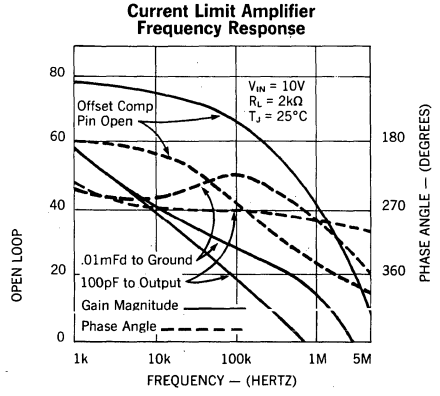
Current Limit Input Threshold



Current Limit Amplifier Gain



Current Limit Amplifier Frequency Response



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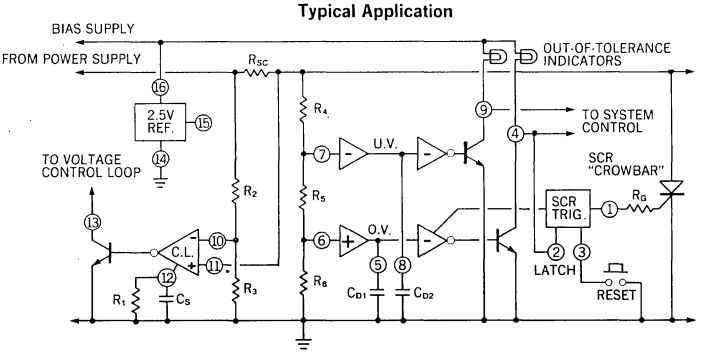
APPLICATIONS (Pin Numbers given for UC1543 series devices)

Typical Application



The values for the external components are determined as follows:

Current limit input threshold, $V_{th} \approx \frac{1000}{R_1}$

C_s is determined by the current loop dynamics

Peak current to load, $Ip \cong \frac{V_{th}}{R_{SC}} + \frac{V_O}{R_{SC}} \left(\frac{R_2}{R_2 + R_3} \right)$

Short circuit current, $Isc = \frac{V_{th}}{R_{SC}}$

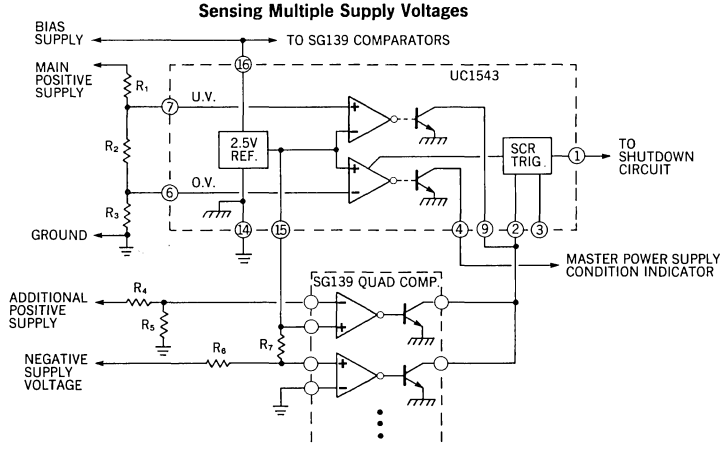
Low output voltage limit, $V_O\,(Low) = \frac{2.5\,(R_4 + R_5 + R_6)}{R_5 + R_6}$

High output voltage limit $V_O\,(High) = \frac{2.5\,(R_4 + R_5 + R_6)}{R_6}$

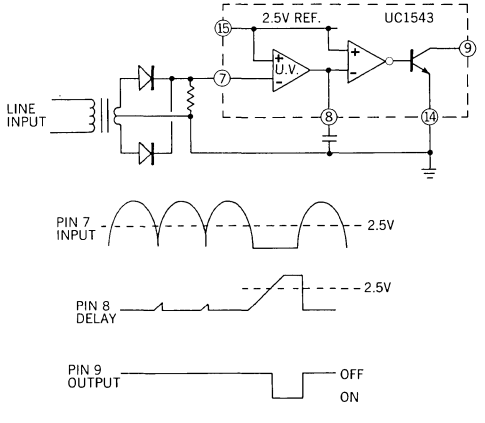
Voltage sensing delay, $t_d = 10{,}000\ Cd$

SCR trigger power limiting resistor, $R_G > \frac{V_{IN} - 5}{0.2}$

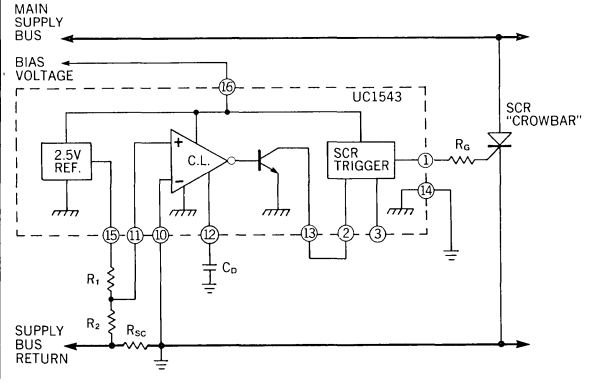
Sensing Multiple Supply Voltages



Input Line Monitor



Overcurrent Shutdown



LINEAR INTEGRATED CIRCUITS

Quad Schottky Diode Array

UC1611
UC3611

FEATURES

- Matched, Four-Diode Monolithic Array
- High Peak Current
- Low-Cost MINIDIP Package
- Low Forward Voltage
- Parallelable for Lower V_F or Higher I_F
- Fast Recovery Time
- Military Temperature Range Available

DESCRIPTION

This four-diode array is designed for general purpose use as individual diodes or as a high-speed, high-current bridge. It is particularly useful on the outputs of high-speed power MOSFET drivers where Schottky diodes are needed to clamp any negative excursions caused by ringing on the driven line.

These diodes are also ideally suited for use as voltage clamps when driving inductive loads such as relays and solenoids, and to provide a path for current free-wheeling in motor drive applications.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

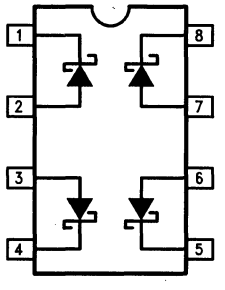
This single monolithic chip is fabricated in both hermetic CERDIP and copper-leaded plastic MINIDIP packages. The UC1611 in ceramic is designed for −55°C to +125°C environments but with reduced peak current capability: while the UC3611 in plastic has higher current rating over a 0°C to +70°C ambient temperature range.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage (per Diode) 50V
Diode-to-Diode Voltage..... 80V
Peak Forward Current
  UC1611 ..... 1A
  UC3611 ..... 3A
Power Dissipation at T_A = +70°C..... 1W
  Derate 12.5 mW/°C above +70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

CONNECTION DIAGRAM

DIL-8 (TOP VIEW)
J or N PACKAGE



0001-1

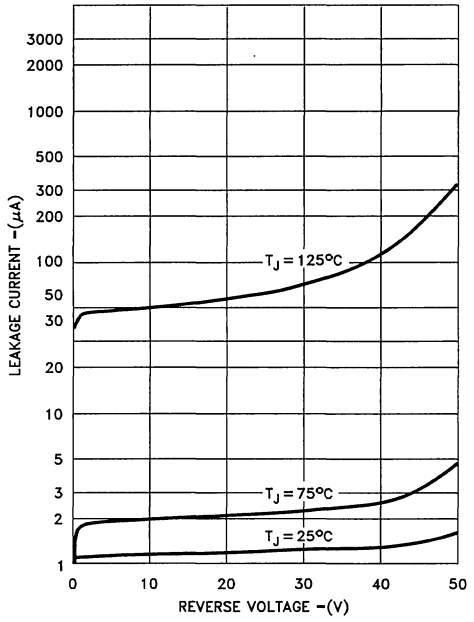
ELECTRICAL CHARACTERISTICS (All specifications apply to each individual diode. T_J = +25°C except as noted.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage Drop	I_F = 100 mA I_F = 1A	0.4	0.5 0.9	0.7 1.2	V
Leakage Current	V_R = 40V V_R = 40V, T_J = +100°C		0.01 0.1	0.1 1.0	mA
Reverse Recovery	0.5A Forward to 0.5A Reverse		20		ns
Forward Recovery	1A Forward to 1.1V Recovery		40		ns
Junction Capacitance	V_R = 5V		100		pF

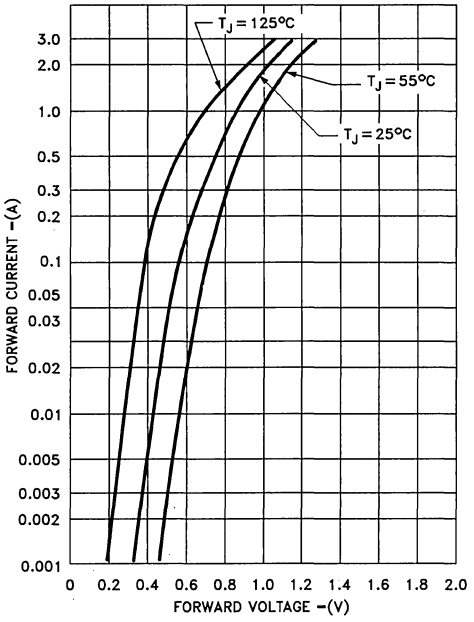
Note: At forward currents of greater than 1.0A, a parasitic current of approximately 10 mA may be collected by adjacent diodes.

3

Reverse Current vs Voltage

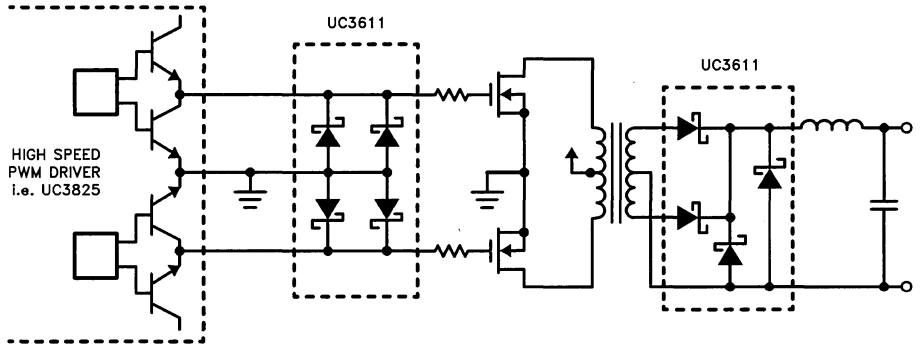


Forward Voltage vs Current



0004-2

TYPICAL APPLICATIONS



0004-3

LINEAR INTEGRATED CIRCUITS

Thermal Monitor

UC1730
UC2730
UC3730

FEATURES

- On-Chip Temperature Transducer
- Temperature Comparator Gives Threshold Temperature Alarm
- Power Reference Permits Airflow Diagnostics
- Precision 2.5V Power Reference Permits Airflow Diagnostics
- Transducer Output is Easily Scaled for Increased Sensitivity
- Low 2.5 mA Quiescent Current

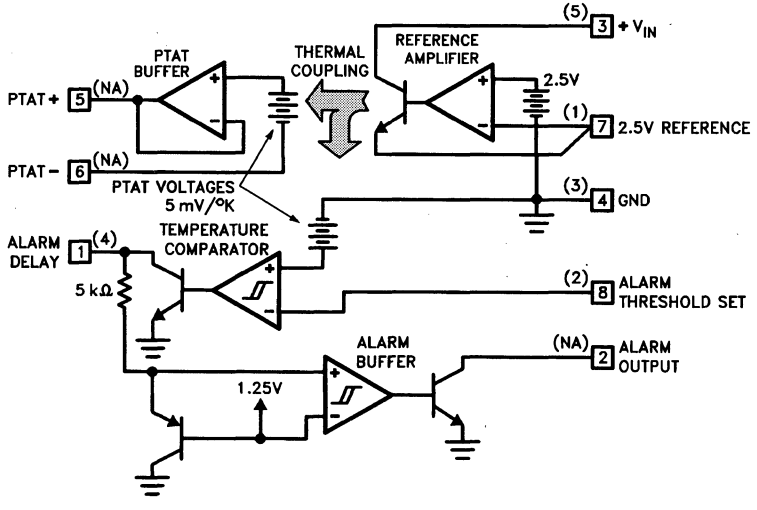
DESCRIPTION

The UC1730 family of integrated circuit devices are designed to be used in a number of thermal monitoring applications. Each IC combines a temperature transducer, precision reference, and temperature comparator allowing the device to respond with a logic output if temperatures exceed a user programmed level. The reference on these devices is capable of supplying in excess of 250 mA of output current—by setting a level of power dissipation the rise in die temperature will vary with airflow past the package, allowing the IC to respond to airflow conditions.

These devices come in an 8-Pin DIP, plastic or ceramic, or a 5-Pin TO-220 version. In the 8-pin version, a PTAT (proportional to absolute temperature) output reports die temperature directly. This output is configured such that its output level can be easily scaled up with two external gain resistors. A second PTAT source is internally referenced to the temperature comparator. The other input to this comparator can then be externally programmed to set a temperature threshold. When this temperature threshold is exceeded an alarm delay output is activated. Following the activation of the delay output, a separate open collector output is turned on. The delay pin can be programmed with an external RC to provide a time separation between the activation of the delay pin and the alarm pin, permitting shutdown diagnostics in applications where the open collector outputs of multiple parts are wire OR'ed together.

The 5-pin version in the TO-220 package is well suited for monitoring heatsink temperatures. Enhanced airflow sensitivities can be obtained with this package by mounting the device to a small heatsink in the airstream. This version of the device does not include the PTAT output or the open collector alarm output.

BLOCK DIAGRAM

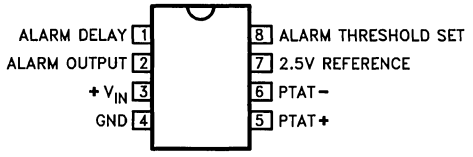


0008-9

Pin numbers shown for 8-Pin DIP, ( ) number for 5-Pin TO-220.

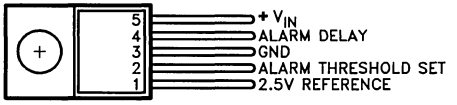
CONNECTION DIAGRAMS

DIL-8 (TOP VIEW)
N or J PACKAGE



0008-1

5-PIN TO-220 (TOP VIEW)
T PACKAGE



0008-2

3

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, (+V_{IN}) 40V
Alarm Output Voltage (8-Pin Version Only) 40V
Alarm Delay Voltage 10V
Alarm Threshold Set Voltage 10V
2.5V Reference Output Current ..... −400 mA
Alarm Output Current (8-Pin Version Only) ..... 20 mA
Power Dissipation at T_A = 25°C ..... 1000 mW
  Derate at 10 mW/°C Above 25°C
Power Dissipation at T_C = 25°C ..... 2000 mW
  Derate at 16 mW/°C Above 25°C

Thermal Resistance Junction to Ambient
  N, 8-Pin Plastic DIP ..... 110°C/W
  J, 8-Pin Ceramic DIP ..... 110°C/W
  T, 5-Pin Plastic DIP TO-220 ..... 65°C/W
Thermal Resistance Junction to Case
  N, 8-Pin Plastic DIP ..... 60°C/W
  J, 8-Pin Ceramic DIP ..... 40°C/W
  T, 5-Pin Plastic TO-220 ..... 5°C/W
Operating Junction Temperature ..... −55°C to +150°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note: 1. Voltages are referenced to ground. Currents are positive into, negative out of, the specified terminals.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, specifications hold for T_j = 0°C to +100°C for the UC3730, −25°C to +100°C for the UC2730 and −55°C to +125°C for the UC1730, +V_{IN} = +5V, and PTAT− = 0V.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY					
Supply Current	+V_{IN} = 35V		2.8	4.0	mA
	+V_{IN} = 5V		2.3	3.5	mA
REFERENCE					
Output Voltage	T_J = 25°C	2.475	2.5	2.525	V
	Over Temperature	2.46		2.54	V
Load Regulation	I_{OUT} = 0 to 250 mA		8.0	25	mV
Line Regulation	+V_{IN} = 5 to 25V		1.0	5.0	mV
TEMPERATURE COMPARATOR					
Temperature Comparator Threshold	at 300°K (26.85°C), Nominally 5 mV/°K, V_{INPUT} High to Low	1.475	1.50	1.525	V
Temperature Error		−10		10	°C
Threshold Line Regulation	+V_{IN} = 5 to 25V		0.005	0.02	%/V
Temperature Linearity	Note 2		2.0	5.0	°C
Threshold Hysteresis		3.0	8.0	15	mV
Input Bias Current	V_{INPUT} at 1.5V	−0.5	−0.1		μA
Max Output Current	V_{OUT} = 1V	1.2	3.0		mA
Output Sat Voltage	I_{OUT} = 100 μA		0.05	0.25	V
Output Leakage Current	V_{OUT} = 1V		0.01	1.0	μA

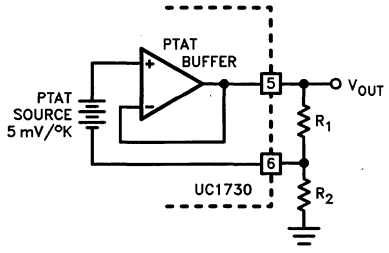
ELECTRICAL CHARACTERISTICS (Continued) (Unless otherwise stated, specifications hold for T_j = 0°C to +100°C for the UC3730, −25°C to +100°C for the UC2730 and −55°C to +125°C for the UC1730, $+V_{IN}$ = +5V, and PTAT− = 0V.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PTAT BUFFER (8-Pin N, or J Version Only)					
Output Voltage	at 300°K (26.85°C), Nominally 5 mV/°K	1.460	1.50	1.54	V
	In 10X Config. $+V_{IN}$ = 25V	14.6	15	15.4	V
Temperature Error		−12		12	°C
Temperature Linearity (Note 2)			2.0	5.0	°C
Line Regulation	$+V_{IN}$ = 5 to 25V		0.02	0.04	%/V
Load Regulation	I_{OUT} = 0 to 2 mA		1.0	3.0	mV
Dropout Voltage	PTAT+ TO $+V_{IN}$		1.9	2.5	V
Input Bias Current at PTAT− Input		−3.0	−1.0		µA
ALARM BUFFER COMPARATOR (8-Pin N, or J, Version Only)					
Threshold Voltage (V_{th})	Alarm Delay Input Low to High	1.1	1.2	1.3	V
Threshold Hysteresis Voltage	Alarm Delay Voltage > V_{th}		100	250	mV
Input Bias Current	Alarm Delay Voltage < V_{th}		0.1	0.5	µA
Max Output Current	V_{OUT} = 1V	7.0	15		mA
Output Sat Voltage	I_{OUT} = 3 mA		0.25	0.45	V
Output Leakage	V_{OUT} = 35V		0.1	2.0	µA

Note: 2. This parameter is guaranteed by design and is not tested in production.

APPLICATION AND OPERATION INFORMATION

Scaling the PTAT Output (8-Pin Version Only)

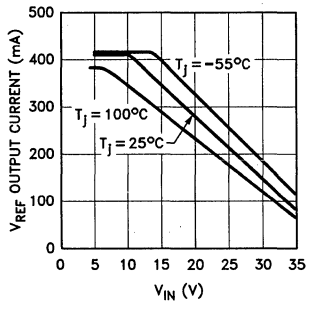


$$V_{OUT} = 5 \times \left(1 + \frac{R_2}{R_1}\right) \text{mV/°K}$$

(Recommended Range for R_1 is 2K to 4K)

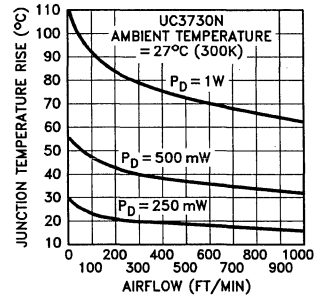
0008-3

V_{REF} Maximum Output Current vs Input Supply



0008-4

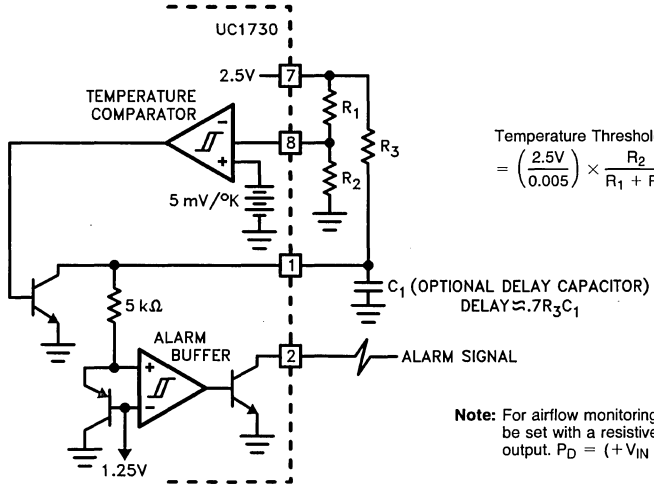
Junction Temperature Rise vs Airflow UC3730N (8-Pin Plastic Dip)



0008-5

APPLICATION AND OPERATION INFORMATION (Continued)

Setting a Temperature Threshold



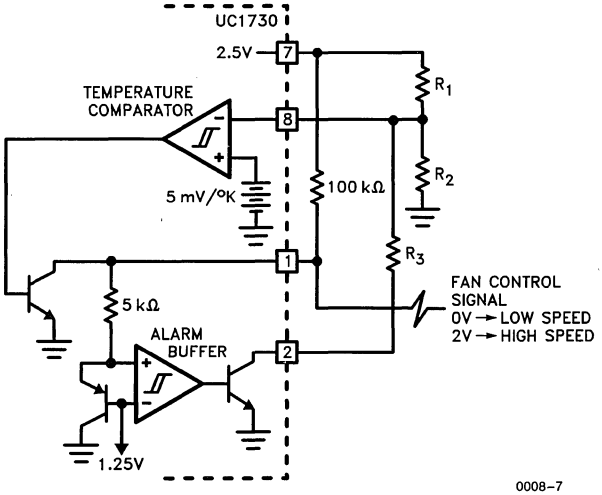
Temperature Threshold (°C)

$$= \left(\frac{2.5V}{0.005}\right) \times \frac{R_2}{R_1 + R_2} - 273.15$$

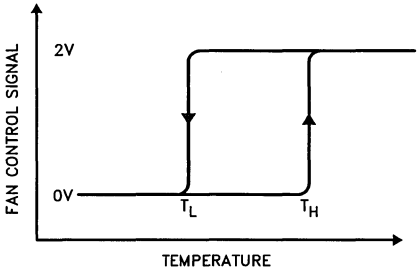
Note: For airflow monitoring a power dissipation level can be set with a resistive load, R_L, on the reference output. $P_D = (+V_{IN} - 2.5V)^2/R_L$.

0008-6

Dual Speed Fan Control



0008-7



0008-8

$$T_H\,(°C) = \frac{2.5V}{0.005} \times \frac{R_2}{R_1 + R_2} - 273.15$$

$$T_L\,(°C) = \frac{2.5V}{0.005} \times \frac{R_X}{R_1 + R_X} - 273.15$$

Where: $R_X = \frac{R_2 R_3}{R_2 + R_3}$

LINEAR INTEGRATED CIRCUITS
High Speed PWM Controller

UC1823
UC2823
UC3823

FEATURES

- Compatible with Voltage or Current-Mode Topologies
- Practical Operation @ Switching Frequencies to 1.0MHz
- 50ns Propagation Delay to Output
- High Current Totem Pole Output (1.5A peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start/Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1mA)
- Trimmed Bandgap Reference (5.1V +/- 1%)

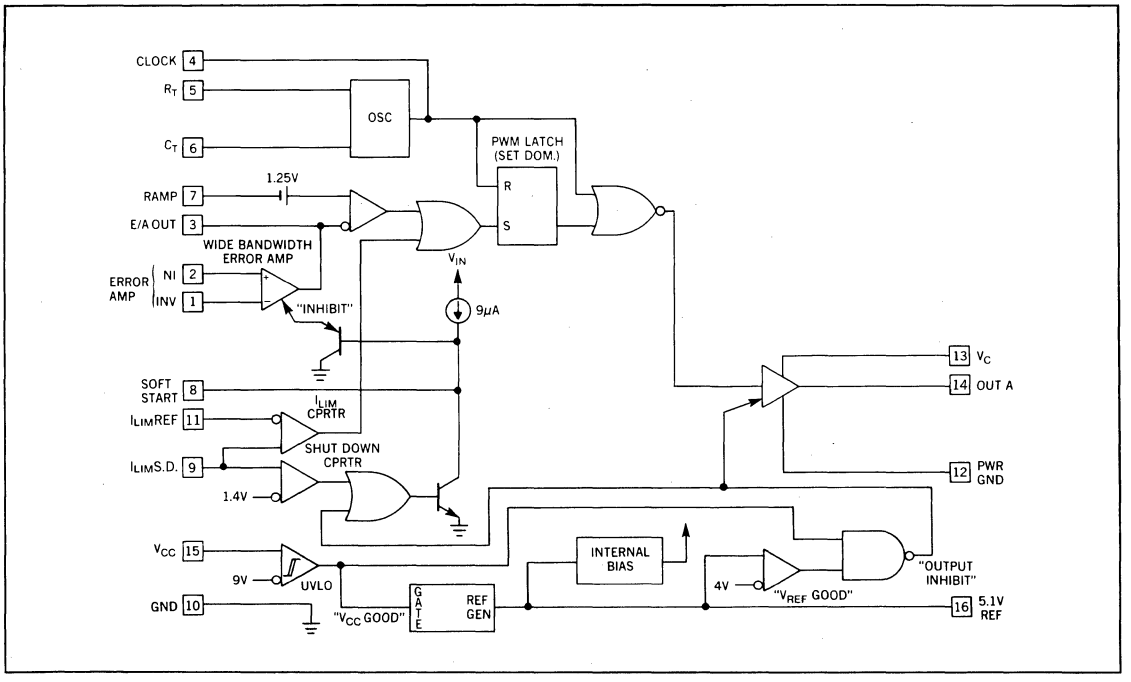
DESCRIPTION

The UC1823 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at the output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the output is high impedance.

These devices feature a totem pole output designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is defined as a high level.

BLOCK DIAGRAM



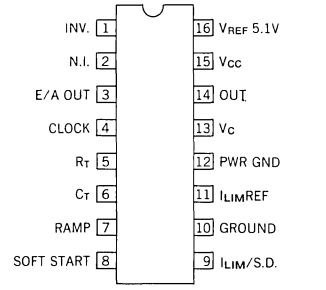
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 15, 13) 30V
Output Current, Source or Sink (Pins 11, 14)
DC 0.5A
Pulse (0.5μs) 2.0A
Analog Inputs (Pins 1, 2, 7, 8, 9) ..... −0.3V to +6V
Clock Output Current (Pin 4) ..... −5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) ..... −5mA
Power Dissipation at T_A = 60°C 1W
Derate 11mW/°C for T_A > 60°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

NOTE: All voltages are with respect to ground, Pin 10.
Currents are positive into the specified terminal.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



3

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, these specifications apply for R_T = 3.65K, C_T = 1nF, V_{CC} = 15V, 0°C < T_A < +70°C for the UC3823, −25°C < T_A < +85°C for the UC2823, and −55°C < T_A < +125°C for the UC1823.)

PARAMETERS	TEST CONDITIONS	UC1823 UC2823			UC3823			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_j = 25°C, I_O = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	10 < V_{CC} < 30V		2	20		2	20	mV
Load Regulation	1 < I_O < 10mA		5	20		5	20	mV
Temperature Stability*	T_{MIN} < T_A < T_{MAX}		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation*	Line, Load, Temp.	5.00		5.20	4.95		5.25	V
Output Noise Voltage	10Hz < f < 10KHz		50			50		μV
Long Term Stability*	T_j = 125°C, 1000 hrs.		5	25		5	25	mV
Short Circuit Current	V_{REF} = 0V	−15	−50	−100	−15	−50	−100	mA
Oscillator Section								
Initial Accuracy*	T_j = 25°C	360	400	440	360	400	440	KHz
Voltage Stability*	10 < V_{CC} < 30V		0.2	2		0.2	2	%
Temperature Stability*	T_{MIN} < T_A < T_{MAX}		5			5		%
Total Variation*	Line, Temp.	340		460	340		460	KHz
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V

* This parameter not 100% tested in production but guaranteed by design.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, these specifications apply for R_T = 3.65K, C_T = 1nF, V_{CC} = 15V, $0°C < T_A < +70°C$ for the UC3823, $-25°C < T_A < +85°C$ for the UC2823, and $-55°C < T_A < +125°C$ for the UC1823.)

PARAMETERS	TEST CONDITIONS	UC1823 UC2823			UC3823			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Error Amplifier Section								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	μA
Input Offset Current			0.1	1		0.1	1	μA
Open Loop Gain	$1 < V_O < 4V$	60	95		60	95		dB
CMRR	$1.5 < V_{CM} < 5.5V$	75	95		75	95		dB
PSRR	$10 < V_{CC} < 30V$	85	110		85	110		dB
Output Sink Current	$V_{PIN\ 3}$ = 1V	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/μs
PWM Comparator Section								
Pin 7 Bias Current	$V_{PIN\ 7}$ = 0V		-1	-5		-1	-5	μA
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero D.C. Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
Soft-Start Section								
Charge Current	$V_{PIN\ 8}$ = 0.5V	3	9	20	3	9	20	μA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			1			mA
Current Limit/Shutdown Section								
Pin 9 Bias Current	$0 < V_{PIN\ 9} < 4V$			±10			±10	μA
Current Limit Offset	$V_{PIN\ 11}$ = 1.1V			15			15	mV
Current Limit Common Mode Range ($V_{PIN\ 11}$)		1.0		1.25	1.0		1.25	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output*			50	80		50	80	ns
Output Section								
Output Low Level	I_{OUT} = 20mA		0.25	0.40		0.25	0.40	V
	I_{OUT} = 200mA		1.2	2.2		1.2	2.2	
Output High Level	I_{OUT} = -20mA	13.0	13.5		13.0	13.5		V
	I_{OUT} = -200mA	12.0	13.0		12.0	13.0		
Collector Leakage	V_C = 30V		100	500		100	500	μA
Rise/Fall Time*	CL = 1nF		30	60		30	60	ns
Under-Voltage Lockout Section								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
Supply Current								
Start Up Current	V_{CC} = 8V		1.1	2.5		1.1	2.5	mA
I_{CC}	$V_{PIN\ 1}$, $V_{PIN\ 7}$, $V_{PIN\ 9}$ = 0V $V_{PIN\ 2}$ = 1V		22	33		22	33	mA

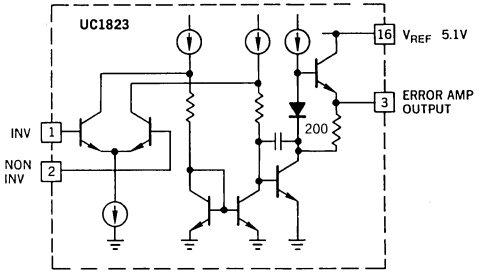
* This parameter not 100% tested in production but guaranteed by design.

UC1823 PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

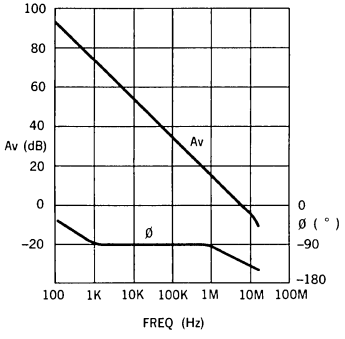
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1823, follow these rules. 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFET. Don't allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve this purpose. 3) Bypass V_{CC}, V_C, and V_{REF}. Use 0.1μF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, C_T, like a bypass capacitor.

ERROR AMPLIFIER CIRCUIT

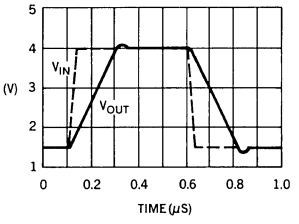
Simplified Schematic



Open Loop Frequency Response

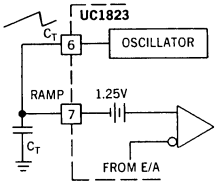


Unity Gain Slew Rate

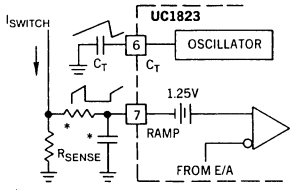


PWM APPLICATIONS

Conventional (Voltage Mode)

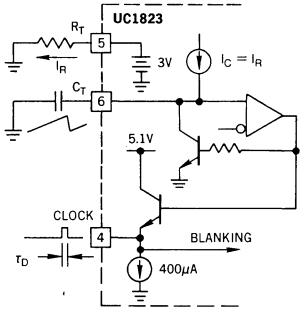


Current-Mode

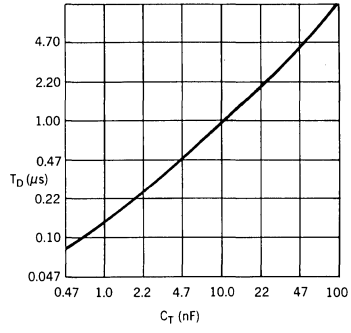


* A SMALL FILTER MAY BE REQUIRED TO SUPPRESS SWITCH NOISE

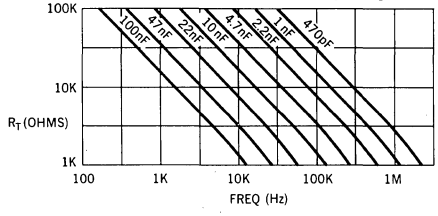
OSCILLATOR CIRCUIT



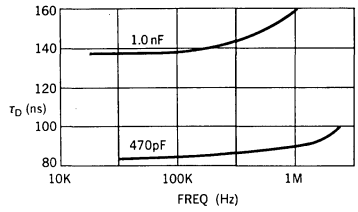
Deadtime vs C_T ($3 \leq R_T \leq 100K$)



Timing Resistance vs Frequency

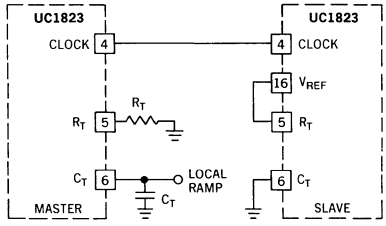


Deadtime vs Frequency

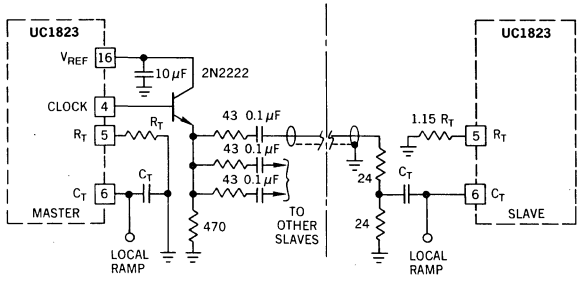


SYNCHRONIZED OPERATION

Two Units in Close Proximity:

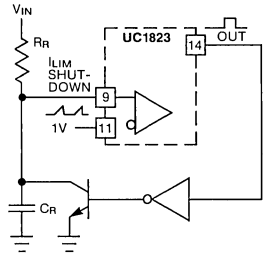


Generalized Synchronization:



Constant Volt-Second Clamp Circuit

The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, R_T and C_R are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the inverter must be such that the ramp capacitor can be completely discharged during the minimum deadtime.



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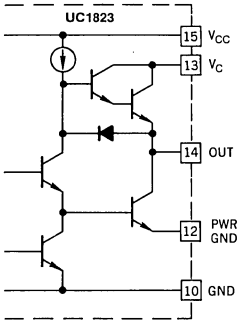
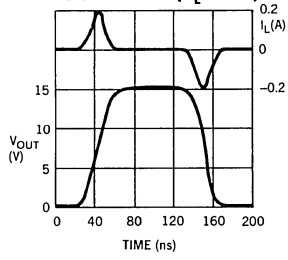
OUTPUT SECTION

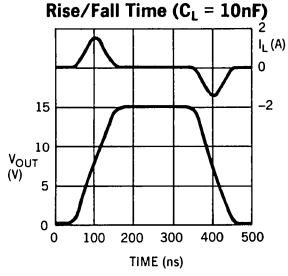
Simplified Schematic



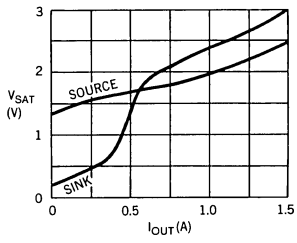
Rise/Fall Time (C_L = 1nF)



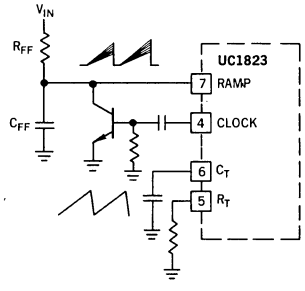
Rise/Fall Time (C_L = 10nF)



Saturation Curves



FEED FORWARD TECHNIQUE FOR OFF-LINE VOLTAGE MODE APPLICATION



LINEAR INTEGRATED CIRCUITS
High Speed PWM Controller

UC1825
UC2825
UC3825

FEATURES

- Compatible with Voltage or Current-Mode Topologies
- Practical Operation @ Switching Frequencies to 1.0MHz
- 50ns Propagation Delay to Output
- High Current Dual Totem Pole Outputs (1.5A peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start/Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1mA)
- Trimmed Bandgap Reference (5.1V +/- 1%)

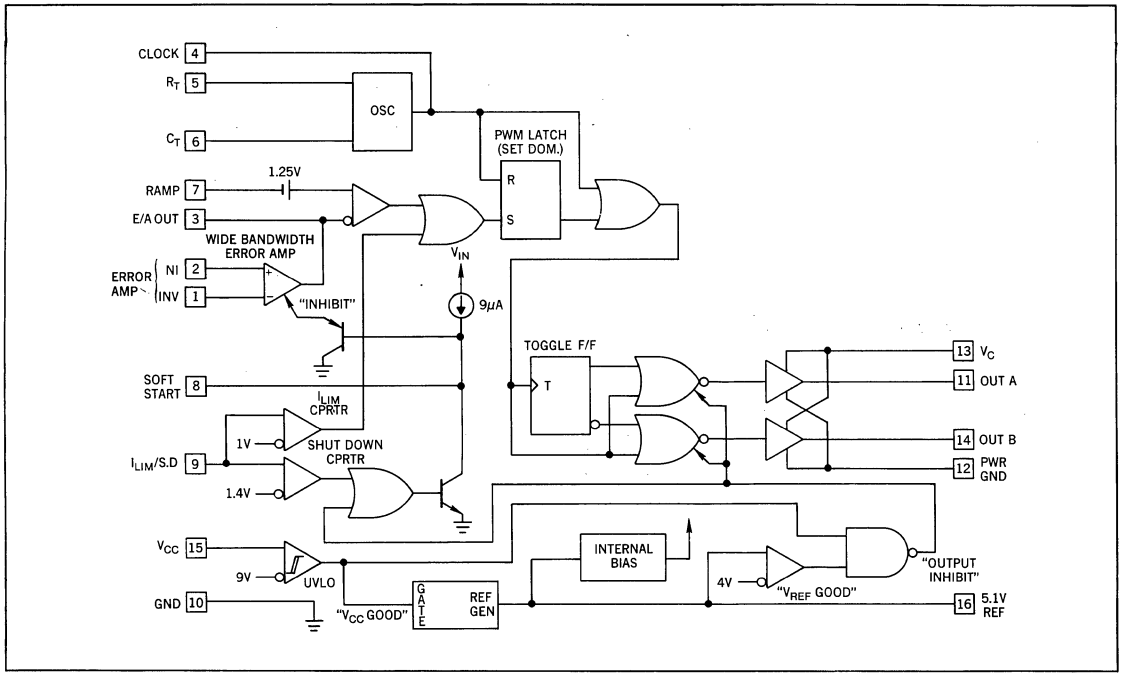
DESCRIPTION

The UC1825 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the outputs are high impedance.

These devices feature totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is defined as a high level.

BLOCK DIAGRAM



UNITRODE

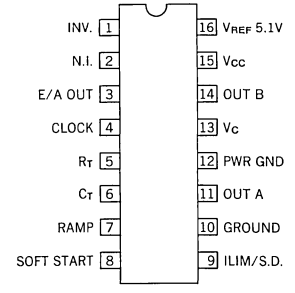
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 15, 13) 30V
Output Current, Source or Sink (Pins 11, 14)
DC 0.5A
Pulse (0.5μs) 2.0A
Analog Inputs
(Pins 1, 2, 7) ..... -0.3V to 7V
(Pin 9, 8) ..... -0.3V to 6V
Clock Output Current (Pin 4) ..... -5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) ..... -5mA
Power Dissipation at T_A = 60°C 1W
Derate 11mW/°C for T_A > 60°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

NOTE: All voltages are with respect to ground, Pin 10.
Currents are positive into the specified terminal.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



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ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, these specifications apply for R_T = 3.65K, C_T = 1nF, V_{CC} = 15V, 0 < T_A < 70°C for the UC3825, -25°C < T_A < 85°C for the UC2825, and -55°C < T_A < 125°C for the UC1825.)

PARAMETERS	TEST CONDITIONS	UC1825 UC2825			UC3825			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_j = 25°C, I_O = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	10 < V_{CC} < 30V		2	20		2	20	mV
Load Regulation	1 < I_O < 10mA		5	20		5	20	mV
Temperature Stability*	T_{MIN} < T_A < T_{MAX}		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation*	Line, Load, Temp.	5.00		5.20	4.95		5.25	V
Output Noise Voltage	10Hz < f < 10KHz		50			50		μV
Long Term Stability*	T_j = 125°C, 1000 hrs.		5	25		5	25	mV
Short Circuit Current	V_{REF} = 0V	-15	-50	-100	-15	-50	-100	mA
Oscillator Section								
Initial Accuracy*	T_j = 25°C	360	400	440	360	400	440	KHz
Voltage Stability*	10 < V_{CC} < 30V		0.2	2		0.2	2	%
Temperature Stability*	T_{MIN} < T_A < T_{MAX}		5			5		%
Total Variation*	Line, Temp.	340		460	340		460	KHz
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V

* This parameter not 100% tested in production but guaranteed by design.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, these specifications apply for R_T = 3.65K, C_T = 1nF, V_{cc} = 15V, $0 < T_A < 70°C$ for the UC3825, $-25°C < T_A < 85°C$ for the UC2825, and $-55°C < T_A < 125°C$ for the UC1825.)

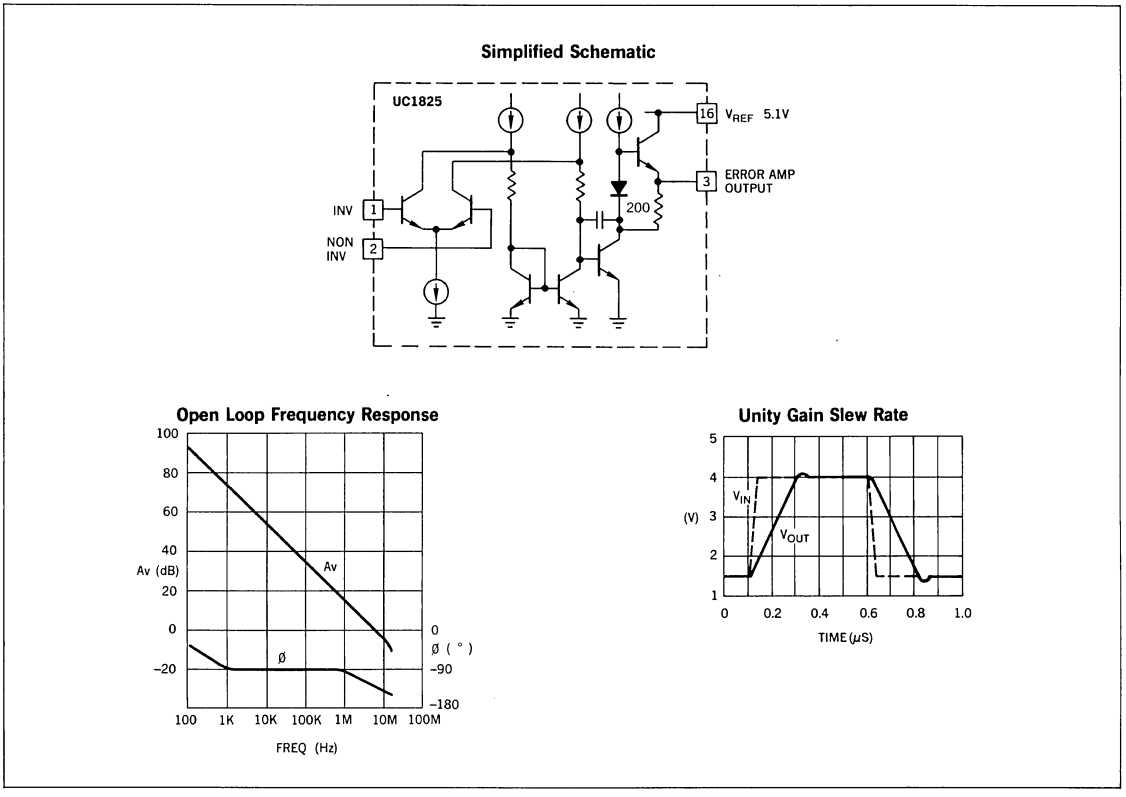
PARAMETERS	TEST CONDITIONS	UC1825 UC2825			UC3825			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Error Amplifier Section								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	μA
Input Offset Current			0.1	1		0.1	1	μA
Open Loop Gain	$1 < V_O < 4V$	60	95		60	95		dB
CMRR	$1.5 < V_{CM} < 5.5V$	75	95		75	95		dB
PSRR	$10 < V_{CC} < 30V$	85	110		85	110		dB
Output Sink Current	$V_{PIN\ 3}$ = 1V	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/μs
PWM Comparator Section								
Pin 7 Bias Current	$V_{PIN\ 7}$ = 0V		-1	-5		-1	-5	μA
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero D.C. Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
Soft-Start Section								
Charge Current	$V_{PIN\ 8}$ = 0.5V	3	9	20	3	9	20	μA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			1			mA
Current Limit/Shutdown Section								
Pin 9 Bias Current	$0 < V_{PIN\ 9} < 4V$			±15			±10	μA
Current Limit Threshold		0.9	1.0	1.1	0.9	1.0	1.1	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output*			50	80		50	80	ns
Output Section								
Output Low Level	I_{OUT} = 20mA		0.25	0.40		0.25	0.40	V
	I_{OUT} = 200mA		1.2	2.2		1.2	2.2	
Output High Level	I_{OUT} = -20mA	13.0	13.5		13.0	13.5		V
	I_{OUT} = -200mA	12.0	13.0		12.0	13.0		
Collector Leakage	V_C = 30V		100	500		100	500	μA
Rise/Fall Time*	CL = 1nF		30	60		30	60	ns
Under-Voltage Lockout Section								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
Supply Current								
Start Up Current	V_{CC} = 8V		1.1	2.5		1.1	2.5	mA
I_{CC}	$V_{PIN\ 1}$, $V_{PIN\ 7}$, $V_{PIN\ 9}$ = 0V $V_{PIN\ 2}$ = 1V		22	33		22	33	mA

* This parameter not 100% tested in production but guaranteed by design.

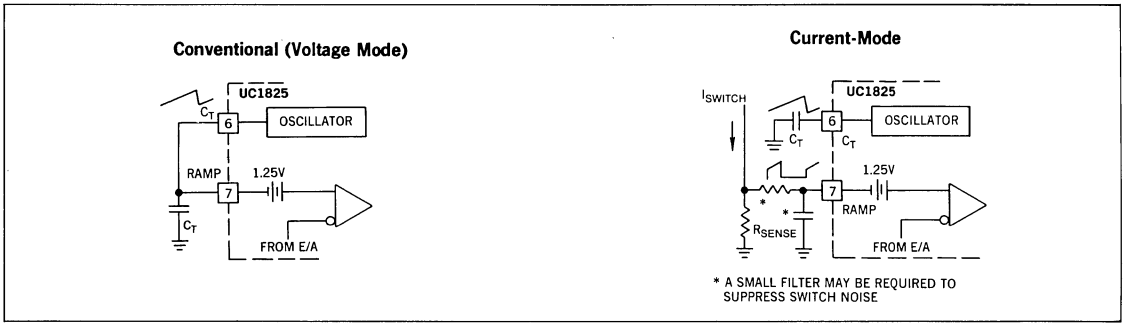
UC1825 PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1825, follow these rules. 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFETs. Don't allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve this purpose. 3) Bypass V_{CC}, V_C, and V_{REF}. Use 0.1μF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, C_T, like a bypass capacitor.

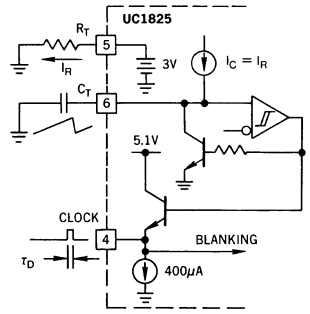
ERROR AMPLIFIER CIRCUIT



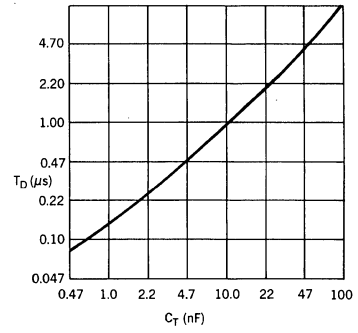
PWM APPLICATIONS



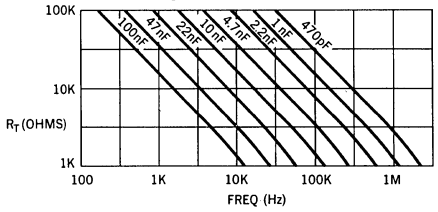
OSCILLATOR CIRCUIT



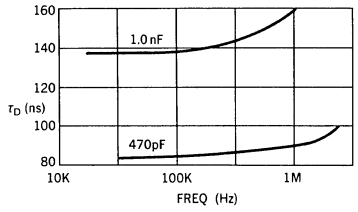
Deadtime vs C_T ($3 \leq R_T \leq 100K$)



Timing Resistance vs Frequency

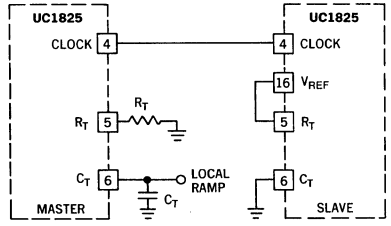


Deadtime vs Frequency

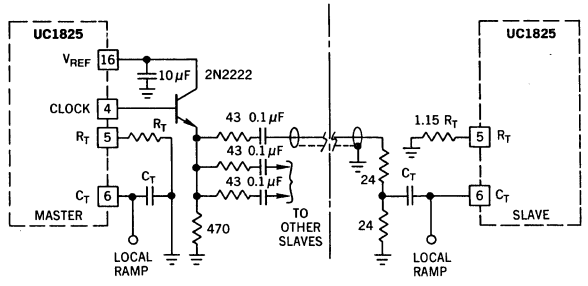


SYNCHRONIZED OPERATION

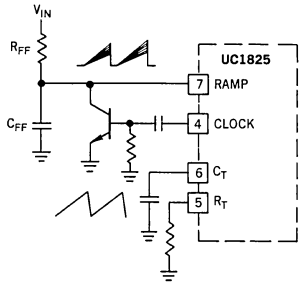
Two Units in Close Proximity:



Generalized Synchronization:

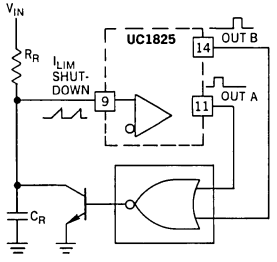


FEED FORWARD TECHNIQUE FOR OFF-LINE VOLTAGE MODE APPLICATION



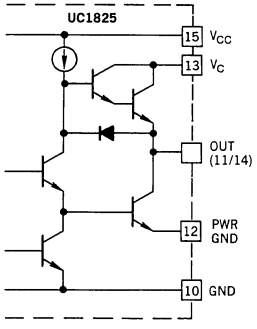
Constant Volt-Second Clamp Circuit

The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, R_T and C_R are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional nor block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

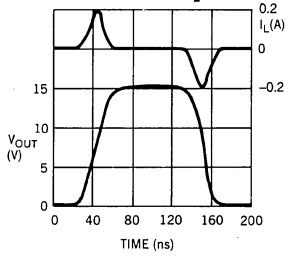


OUTPUT SECTION

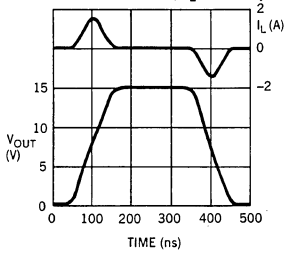
Simplified Schematic



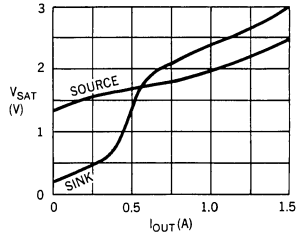
Rise/Fall Time (C_L = 1nF)



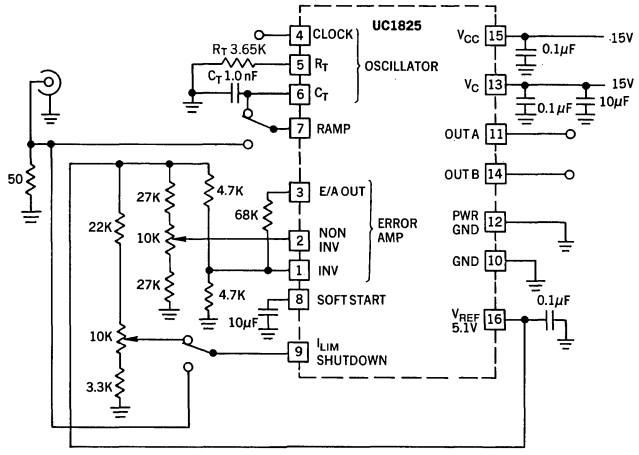
Rise/Fall Time (C_L = 10nF)



Saturation Curves



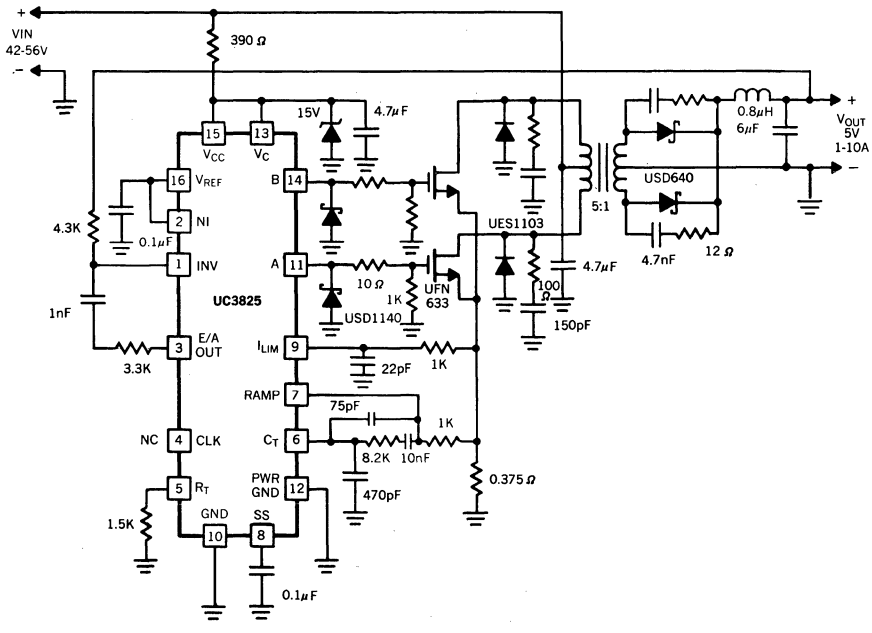
OPEN LOOP LABORATORY TEST FIXTURE



This test fixture is useful for exercising many of the UC1825's functions and measuring their specifications.

As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.

DESIGN EXAMPLE: 50W, 48V to 5V DC TO DC CONVERTER — 1.5MHz CLOCK FREQUENCY



LINEAR INTEGRATED CIRCUITS

High Efficiency Linear Regulator

UC1834
UC2834
UC3834

3

FEATURES

- Minimum V_{IN} - V_{OUT} less than 0.5V at 5A load with external pass device
- Equally usable for either positive or negative regulator design
- Adjustable low threshold current sense amplifier
- Under and over-voltage fault alert with programmable delay
- Over-voltage fault latch with 100mA crowbar drive output

DESCRIPTION

The UC1834 family of integrated circuits is optimized for the design of low input-output differential linear regulators. A high gain amplifier and 200mA sink or source drive outputs facilitate high output current designs which use an external pass device. With both positive and negative precision references, either polarity of regulator can be implemented. A current sense amplifier with a low, adjustable, threshold can be used to sense and limit currents in either the positive or negative supply lines.

In addition, this series of parts has a fault monitoring circuit which senses both under and over-voltage fault conditions. After a user defined delay for transient rejection, this circuitry provides a fault alert output for either fault condition. In the over-voltage case, a 100mA crowbar output is activated. An over-voltage latch will maintain the crowbar output and can be used to shutdown the driver outputs. System control to the device can be accommodated at a single input which will act as both a supply reset and remote shutdown terminal. These die are protected against excessive power dissipation by an internal thermal shutdown function.

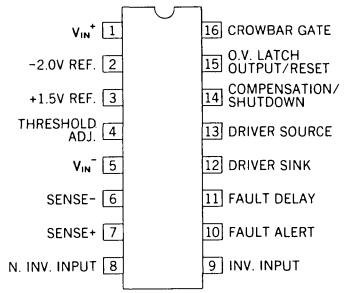
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage, V_{IN}^+	40V
Driver Current	400mA
Driver Source to Sink Voltage	40V
Crowbar Current	-200mA
+1.5V Reference Output Current	-10mA
Fault Alert Voltage	40V
Fault Alert Current	15mA
Error Amplifier Inputs	-0.5V to 35V
Current Sense Inputs	-0.5V to 40V
O.V. Latch Output Voltage	-0.5V to 40V
O.V. Latch Output Current	15mA
Power Dissipation at T_A = 25°C	1000mW
Derate at 10mW/°C above T_A = 50°C	
Power Dissipation at T_C = 25°C	2000mW
Derate at 16mW/°C above T_C = 25°C	
Thermal Resistance, Junction to Ambient	100°C/W
Thermal Resistance, Junction to Case	60°C/W
Operating Junction Temperature	-55°C to +150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C

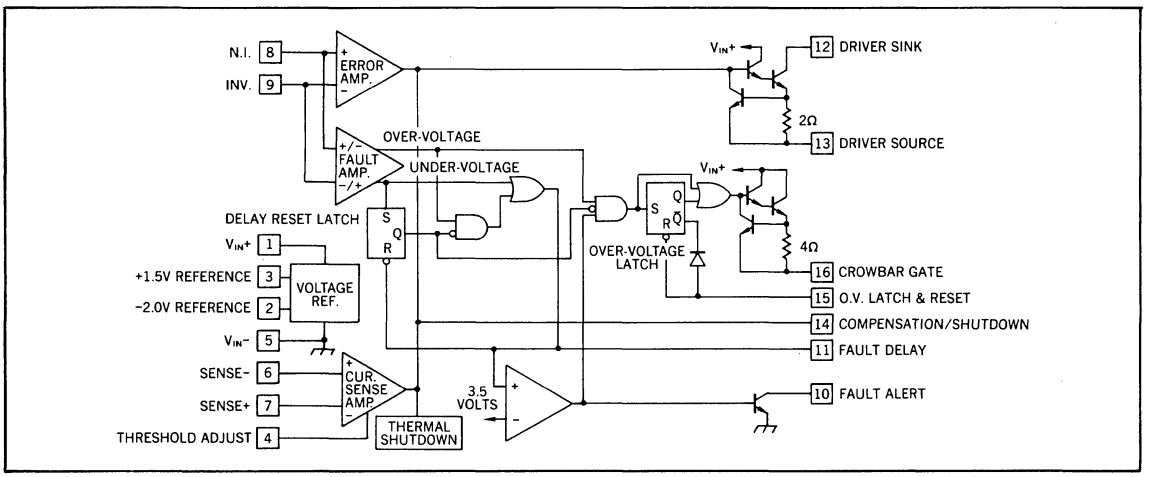
Note: 1. Voltages are reference to V_{IN}^-, Pin 5.
Currents are positive into, negative out of the specified terminals.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



BLOCK DIAGRAM



UNITRODE

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1834; −25°C to +85°C for the UC2834; and 0°C to +70°C for the UC3834; V_{IN}^+ = 15V, V_{IN}^- = 0V.)

PARAMETER	TEST CONDITIONS	UC1834/UC2834			UC3834			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Standby Supply Current			5.5	7		5.5	10	mA
+1.5 Volt Reference								
Output Voltage	T_j = 25°C	1.485	1.5	1.515	1.47	1.5	1.53	V
	$T_{j(MIN)} \le T_j \le T_{j(MAX)}$	1.47		1.53	1.455		1.545	
Line Regulation	V_{IN}^+ = 5 to 35V		1	10		1	15	mV
Load Regulation	I_{OUT} = 0 to 2mA		1	10		1	15	mV
−2.0 Volt Reference (Note 2)								
Output Voltage (Referenced to V_{IN}^+)	T_j = 25°C	2.04	−2	1.96	2.06	−2	1.94	V
	$T_{j(MIN)} \le T_j \le T_{j(MAX)}$	2.06		1.94	2.08		1.92	
Line Regulation	V_{IN}^+ = 5 to 35V		1.5	15		1.5	20	mV
Output Impedance			2.3			2.3		kΩ
Error Amplifier Section								
Input Offset Voltage	V_{CM} = 1.5V		1	6		1	10	mV
Input Bias Current	V_{CM} = 1.5V		−1	−4		−1	−8	μA
Input Offset Current	V_{CM} = 1.5V		0.1	1		0.1	2	μA
Small Signal Open Loop Gain	Output @ Pin 14, Pin 12 = V_{IN}^+ Pin 13, 20Ω to V_{IN}^-	50	65		50	65		dB
CMRR	V_{CM} = 0.5 to 33V, V_{IN}^+ = 35V	60	80		60	80		dB
PSRR	V_{IN}^+ = 5 to 35V, V_{CM} = 1.5V	70	100		70	100		dB
Driver Section								
Maximum Output Current		200	350		200	350		mA
Saturation Voltage	I_{OUT} = 100mA		0.5	1.2		0.5	1.5	V
Output Leakage Current	Pin 12 = 35V, Pin 13 = V_{IN}^-, Pin 14 = V_{IN}^-		0.1	50		0.1	50	μA
Shutdown Input Voltage at Pin 14	$I_{OUT} \le 100\mu A$, Pin 13 = V_{IN}^-, Pin 12 = V_{IN}^+	0.4	1		0.4	1		V
Shutdown Input Current at Pin 14	Pin 14 = V_{IN}^-, Pin 12 = V_{IN}^+, $I_{OUT} \le 100\mu A$, Pin 13 = V_{IN}^-		−100	−150		−100	−150	μA
Thermal Shutdown (Note 3)			165			165		°C
Fault Amplifier Section								
Under- and Over- Voltage Fault Threshold	V_{CM} = 1.5V, @ E/A Inputs	120	150	180	110	150	190	mV
Common Mode Sensitivity	V_{IN}+ = 35V, V_{CM} = 1.5 to 33V		−0.4	−0.8		−0.4	−1.0	%/V
Supply Sensitivity	V_{CM} =1.5V, V_{IN}^+ = 5 to 35V		−0.5	−1.0		−0.5	−1.2	%/V
Fault Delay		30	45	60	30	45	60	ms/μF
Fault Alert Output Current		2	5		2	5		mA
Fault Alert Saturation Voltage	I_{OUT} =1mA		0.2	0.5		0.2	0.5	V
O.V. Latch Output Current		2	4		2	4		mA
O.V. Latch Saturation Voltage	I_{OUT} = 1mA		1.0	1.3		1.0	1.3	V
O.V. Latch Output Reset Voltage		0.3	0.4	0.6	0.3	0.4	0.6	V
Crowbar Gate Current		−100	−175		−100	−175		mA
Crowbar Gate Leakage Current	V_{IN}^+ = 35V, Pin 16 = V_{IN}^-		−0.5	−50		−0.5	−50	μA

Note: 2. When using both the 1.5V and −2.0V references the current out of Pin 3 should be balanced by an equivalent current into Pin 2. The −2.0V output will change −2.3mV per μA of inbalance.

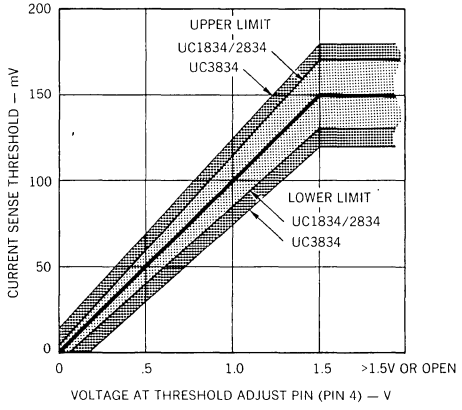
3. Thermal shutdown turns off the driver. If Pin 15 (O.V. Latch Output) is tied to Pin 14 (Compensation/Shutdown), the O.V. Latch will be reset.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1834; −25°C to +85°C for the UC2834; and 0°C to +70°C for the UC3834; V_{IN}^+ = 15V, V_{IN}^- = 0V.)

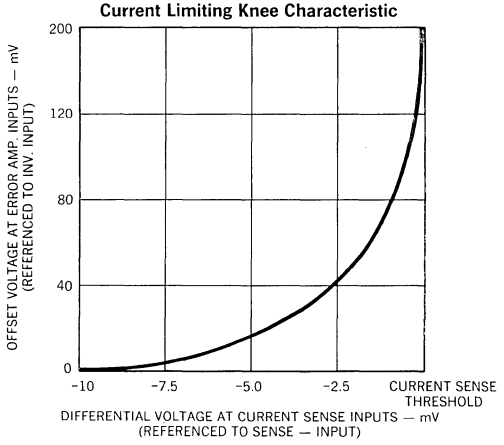
PARAMETER	TEST CONDITIONS	UC1834/UC2834			UC3834			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Current Sense Amplifier Section								
Threshold Voltage	Pin 4 Open, $V_{CM} = V_{IN}^+$ or V_{IN}^-	130	150	170	120	150	180	mV
	Pin 4 = 0.5V, $V_{CM} = V_{IN}^+$ or V_{IN}^-	40	50	60	30	50	70	
Threshold Supply Sensitivity	Pin 4 Open, $V_{CM} = V_{IN}^-$, V_{IN}^+ = 5 to 35V		−0.1	−0.3		−0.1	−0.5	%/V
Adj. Input Current	Pin 4 = 0.5V		−2	−10		−2	−10	μA
Sense Input Bias Current	$V_{CM} = V_{IN}^+$		100	200		100	200	μA
	$V_{CM} = V_{IN}^-$		−100	−200		−100	−200	

3

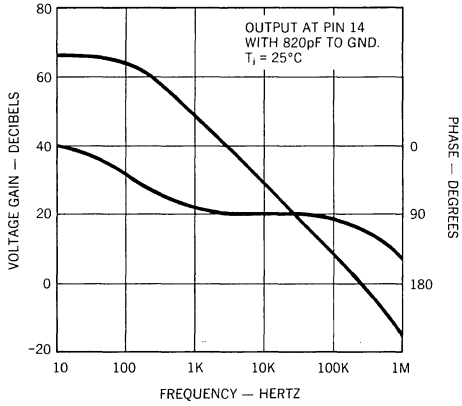
Current Sense Threshold Adjustment



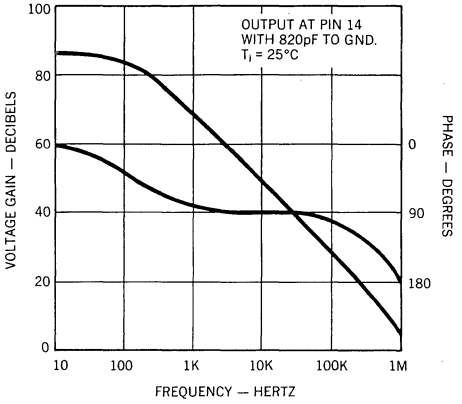
Current Limiting Knee Characteristic



Error Amplifier Gain and Phase Frequency Response

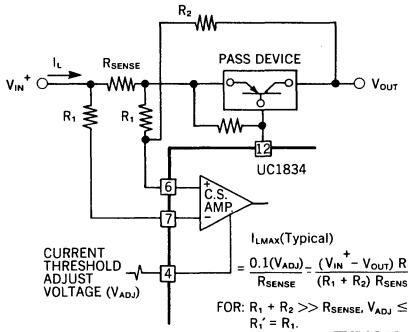


Current Sense Amplifier Gain and Phase Frequency Response

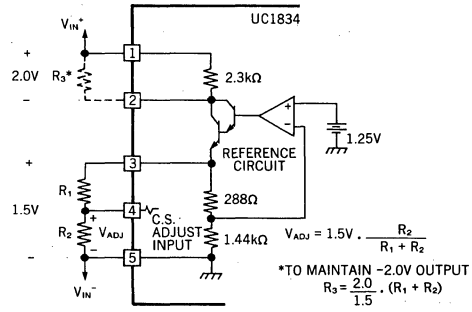


APPLICATION INFORMATION

Foldback Current Limiting



Setting The Threshold Adjust Voltage (V_{ADJ})



TYPICAL APPLICATIONS

Both the current sense and error amplifiers on the UC1834 are transconductance type amplifiers. As a result, their voltage gain is a direct function of the load impedence at their shared output pin, Pin 14. Their small signal voltage gain as a function of load and frequency is nominally given by;

$$A_{V\ E/A} = \frac{Z_L(f)}{700\Omega} \text{ and } A_{V\ C.S./A} = \frac{Z_L(f)}{70\Omega}$$

for: $f \leq 500kHz$ and $|Z_L(f)| \leq 1M\Omega$,

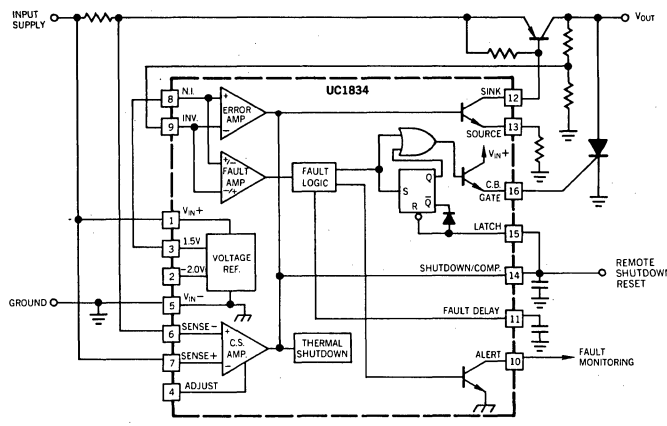
where:

A_V = small signal voltage gain to Pin 14,
$Z_L(f)$ = load impedence at Pin 14.

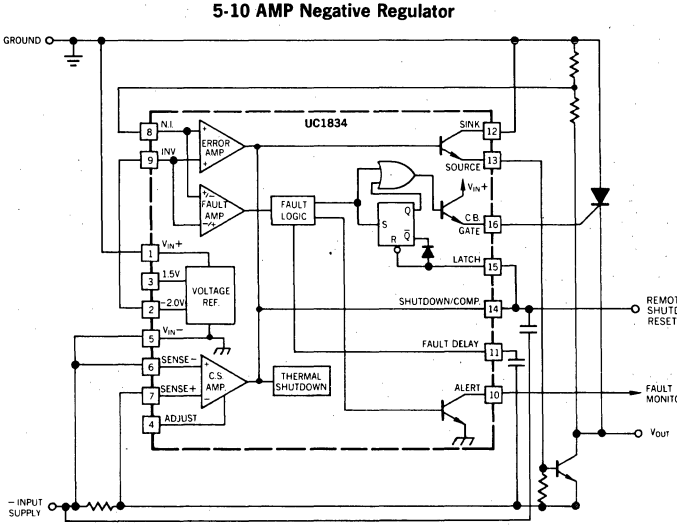
The UC1834 fault delay circuitry prevents the fault outputs from responding to transient fault conditions. The delay reset latch insures that the full, user defined, delay passes before an over-voltage fault response occurs. This prevents unnecessary crowbar, or latched-off conditions, from occurring following sharp under-voltage to over-voltage transients.

The crowbar output on the UC1834 is activated following a sustained over-volatge condition. The crowbar output remains high as long as the fault condition persists, or, as long as the over-voltage latch is set. The latch is set with an over-voltage fault if the voltage at Pin 15 is above the latch reset threshold, typically 0.4V. When the latch is set, its $\overline{Q}$ output will pull Pin 15 low through a series diode. As long as a nominal pull-up load exists, the series diode prevents $\overline{Q}$ from pulling Pin 15 below the reset threshold. However, Pin 15 is pulled low enough to disable the driver outputs if Pins 15 and 14 are tied together. With Pin 15 and 14 common, the regulator will latch off in response to an over-voltage fault. If the fault condition is cleared and Pins 14 and 15 are momentarily pulled below the latch reset threshold, the driver outputs are re-enabled.

5-10 AMP Positive Regulator



5-10 AMP Negative Regulator



LINEAR INTEGRATED CIRCUITS
High Efficiency Regulator Controller

UC1835 UC1836
UC2835 UC2836
UC3835 UC3836

FEATURES
- Complete Control for a High Current, Low Dropout, Linear Regulator
- Fixed 5V or Adjustable Output Voltage
- Accurate 2.5A Current Limiting with Foldback
- Internal Current Sense Resistor
- Remote Sense for Improved Load Regulation
- External Shutdown
- Under-Voltage Lockout and Reverse Voltage Protection
- Thermal Shutdown Protection
- Packaged in an 8-Pin Mini-Dip

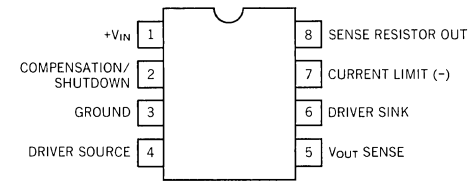
DESCRIPTION
The UC1835/6 families of linear controllers, packaged in 8-pin mini-dips, are optimized for the design of low cost, low dropout, linear regulators. Using an external pass element, dropout voltages of less than 0.5V are readily obtained. These devices contain a high gain error amplifier, a 250mA output driver, and a precision reference. In addition, current sense with foldback provides for a 2.5A peak output current dropping to less than 0.5A at short circuit.

These devices are available in fixed, 5V, (UC1835), or adjustable, (UC1836), versions. In the fixed 5 volt version, the only external parts required are an external pass element, an output capacitor, and a compensation capacitor. On the adjustable version the output voltage can be set anywhere from 2.5V to 35V with two external resistors.

Additional features of these devices include under-voltage lockout for predictable start-up, thermal shutdown and short circuit current limiting to protect the driver device. On the fixed voltage version, a reverse voltage comparator minimizes reverse load current in the event of a negative input to output differential.

CONNECTION DIAGRAM

DIL-8 (TOP VIEW)
N or J PACKAGE

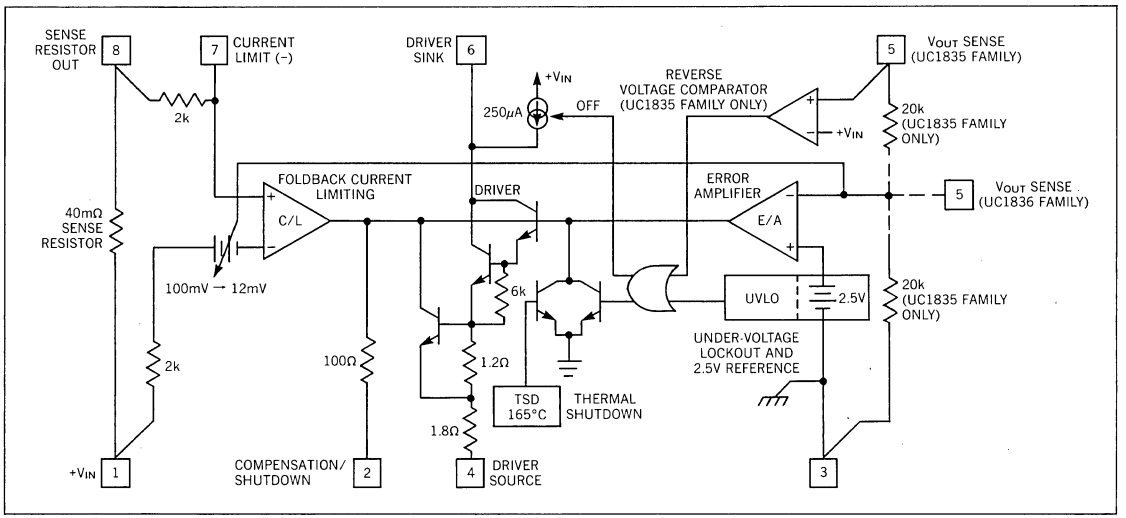


ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage ($+V_{IN}$) ..... -1.0V to +40V
Driver Output Current (Sink or Source) 600mA
Driver Source to Sink Voltage ..... +40V
Maximum Current Through Sense Resistor 4A
V_{OUT} Sense Input Voltage ..... -.3V to +40V
Power Dissipation at T_A = 25°C 1000mW
Derate at 10mW/°C above 25°C
Power Dissipation at T_C = 25°C 2000mW
Derate at 16mW/°C above 25°C
Thermal Resistance Junction to Ambient ..... 100°C/W
Thermal Resistance Junction to Case ..... 60°C/W
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note: 1. Voltages are referenced to ground, (Pin 16). Currents are positive into, negative out of, the specified terminals.

BLOCK DIAGRAM



UNITRODE

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, specifications hold for T_A = 0°C to +70°C for the UC3835/6, −25°C to +85°C for the UC2835/6 and −55°C to +125°C for the UC1835/6, $+V_{IN}$ = 6V, Driver source = 0V, Driver sink = 5V.)

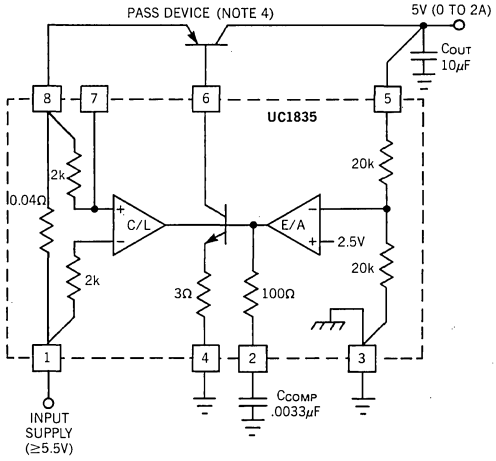
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Supply					
Supply Current	$+V_{IN}$ = 6V		2.75	4.0	mA
	$+V_{IN}$ = 40V		3.75	6.0	mA
UVLO Threshold	$+V_{IN}$ Low to High, V_{OUT} Sense = 0V	3.9	4.4	4.9	V
Threshold Hysteresis			0.1	0.35	V
Reverse Current	$+V_{IN}$ = −1.0V, Driver Sink Open		6.0	20	mA
Regulating Voltage and Error Amplifier (UC1835 Family Only)					
Regulating Level at V_{OUT} Sense (V_{REG})	Driver Current = 10mA, T_J = 25°C	4.94	5.0	5.06	V
	Over Temperature	4.9		5.1	V
Line Regulation	$+V_{IN}$ = 5.2V to 35V		15	40	mV
Load Regulation	Driver Current = 0 to 250mA		6.0	25	mV
Bias Current at V_{OUT} Sense	V_{OUT} Sense = 5.0V	75	125	210	µA
Error Amp Transconductance	±100µA at Compensation/Shutdown Pin	0.8	1.3	2.0	mS
Maximum Compensation Output Current	Sink or Source, Driver Source Open	90	200	260	µA
Regulating Voltage and Error Amplifier (UC1836 Family Only)					
Regulating Level at V_{OUT} Sense (V_{REG})	Driver Current = 10mA, T_J = 25°C	2.47	2.5	2.53	V
	Over Temperature	2.45		2.55	V
Line Regulation	$+V_{IN}$ = 5.2V to 35V		6.0	20	mV
Load Regulation	Driver Current = 0 to 250mA		3.0	15	mV
Bias Current at V_{OUT} Sense	V_{OUT} Sense = 2.5V	−1.0	−0.2		µA
Error Amp Transconductance	±100µA at Compensation/Shutdown Pin	0.8	1.3	2.0	mS
Maximum Compensation Output Current	Sink or Source, Driver Source Open	90	200	260	µA
Driver					
Maximum Current		250	500		mA
Saturation Voltage	Driver Current = 250mA, Driver Sink		2.0	2.8	V
Pull-Up Current at Driver Sink	Compensation/Shutdown = 0.45V	140	250	300	µA
Driver Sink Leakage	In UVLO			10	µA
	In Reverse Voltage (UC1835 Family Only)			10	µA
Thermal Shutdown			165		°C
Foldback Current Limit					
Current Limit Levels at Sense Resistor Out	V_{OUT} Sense = (0.99) V_{REG}	2.2	2.5	2.8	A
	V_{OUT} Sense = (0.5) V_{REG}	1.3	1.5	1.7	A
	V_{OUT} Sense = 0V	0.25	0.4	0.55	A
Current Limit Amp Transconductance	±100µA at Compensation/Shutdown, V_{OUT} Sense = (0.9) V_{REG}	12	24	42	mS
Limiting Voltage at Current Limit (−) (Note 2)	V_{OUT} Sense = (0.9) V_{REG} Volts Below $+V_{IN}$, T_J = 25°C	80	100	140	mV
Sense Resistor Value (Note 3)	V_{OUT} Sense = (0.9) V_{REG} I_{OUT} = 1A, T_J = 25°C		40		mΩ

Note: 2. This voltage has a positive temperature coefficient of approximately 3500ppm/°C.

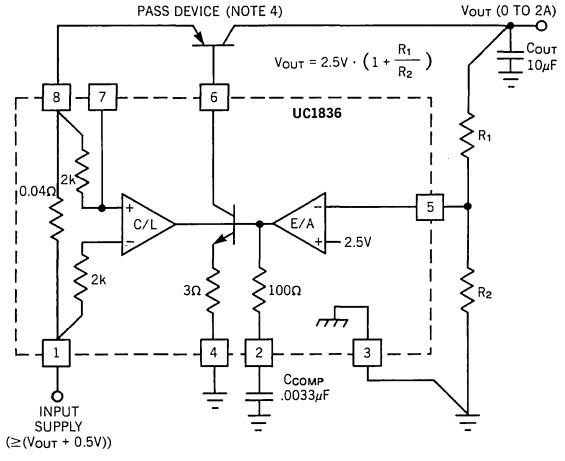
3. This resistance has a positive temperature coefficient of approximately 3500ppm/°C. The total resistance from Pin 1 to Pin 8 will include an additional 60 to 100mΩ of package resistance.

APPLICATION AND OPERATION INFORMATION

UC1835 — Typical Configuration for a 2A, Low Dropout 5V Regulator

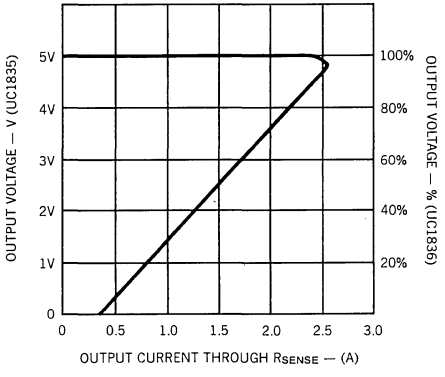


UC1836 — Typical Configuration for a 2A, Low Dropout Adjustable Regulator



Note: 4. Suggested pass devices are TIP32B, (Dropout Voltage ≤ 0.75V) or, D45H, (Dropout Voltage ≤ 0.5V), or equivalents.

UC1835/6 Foldback Current Limiting



LINEAR INTEGRATED CIRCUITS
Magnetic Amplifier Controller

UC1838
UC2838
UC3838

FEATURES
- Independent 1% Reference
- Two Uncommitted, Identical Operational Amplifiers
- 100mA Reset Current Source with −100V Capability
- 5V to 40V Analog Operation
- 5W DIL Package

DESCRIPTION
The UC1838 family of magnetic amplifier controllers contains the circuitry to generate and amplify a low-level analog error signal along with a high voltage-compliant current source. This source will provide the reset current necessary to enable a magnetic amplifier to regulate and control a power supply output in the range of 2A to 20A.

By controlling the reset current to a magnetic amplifier, this device will define the amount of volt-seconds the magnetic amplifier will block before switching to the conducting state. Magnetic amplifiers are ideal for post-regulators for multiple-output power supplies where each output can be independently controlled with efficiencies up to 99%. With a square or pulse-width-modulated input voltage, a magnetic amplifier will block a portion of this input waveform, allowing just enough to pass to provide a regulated output. With the UC1838, only the magnetic amplifier coil, three diodes, and an output L-C filter are necessary to implement a complete closed-loop regulator.

The UC1838 contains a precision 2.5V reference, two uncommitted high-gain op amps and a high-gain PNP-equivalent current source which can deliver up to 100mA of magnetic amplifier reset current.

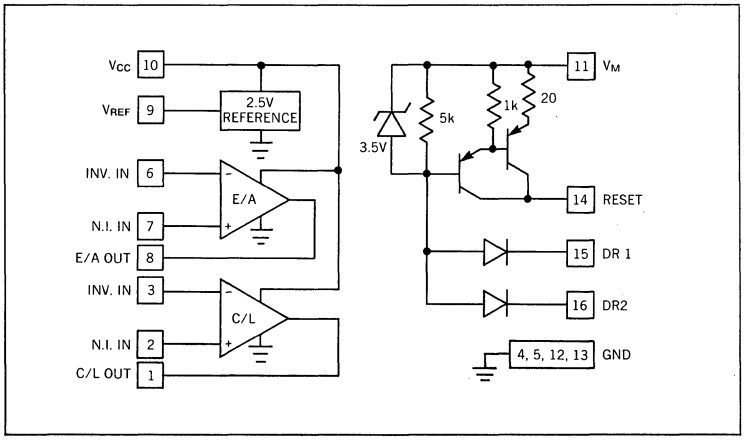
These devices are available in a plastic "bat-wing" DIP for operation over a −20°C to +85°C temperature range and, with reduced power, in a hermetically sealed cerdip for −55°C to +125°C operation.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	40V	
Magnetic Amp. Source Voltage, V_M	40V	
Reset Output Voltage, V_R	−80V	
Total Current Source Voltage, $V_M - V_R$	100V	
Amplifier Input Range	−.3V to V_{CC}	
Reset Input Current, I_{DR}	−10mA	
	Plastic	**Cerdip**
Power Dissipation at T_A = 25°C	2W	1W
Derate Above 50°C	20mW/°C	10mW/°C
Power Dissipation at T (leads/case) = 25°C	5W	2W
Derate for Ground Lead Temperature Above 70°C	70mW/°C	—
Derate for Case Temperature Above 25°C	—	16mW/°C
Operating Temperature Range	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	
Lead Temperature (Soldering, 10 sec)	300°C	

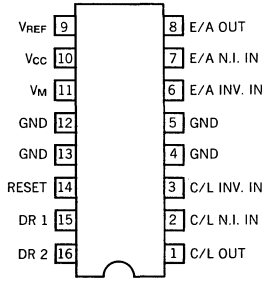
NOTE: All voltages are with respect to ground pins.
All currents are positive into the specified terminal.

BLOCK DIAGRAM



CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



NOTE: All four ground pins must be connected to a common ground.

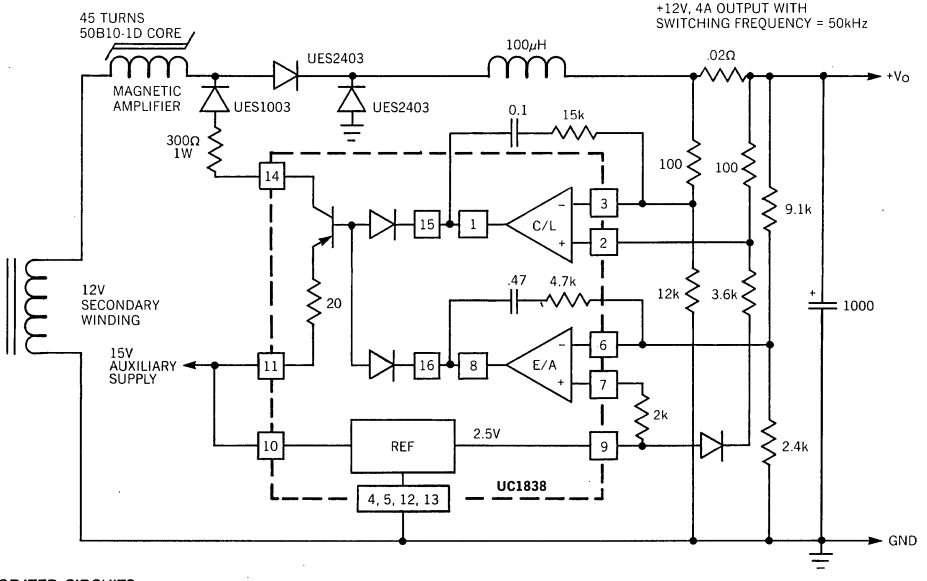
UNITRODE

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1838, −20°C to +85°C for the UC2838, and 0°C to +70°C for the UC3838; V_{CC} = 20V, V_M = 5V.)

PARAMETER	TEST CONDITIONS	UC1838/UC2838			UC3838			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Supply Current	V_{CC} = V_M = 40V	—	6	8	—	6	8	mA
Reference Output	T_A = 25°C	2.47	2.5	2.53	2.45	2.5	2.55	V
Line Regulation	V_{CC} = 5 to 30V	—	1	5	—	1	10	mV
Load Regulation	I_O = 0 to −2mA	—	15	25	—	15	25	mV
Short Circuit Current	V_{REF} = 0V	—	−30	−60	—	−30	−60	mA
Temperature Stability*	Over Operating Temp. Range	—	15	25	—	10	25	mV
Amplifier Section (Each Amplifier)								
Offset Voltage	V_{CM} = 2.5V	—	—	5	—	—	10	mV
Input Bias Current	V_{IN} = 0V	—	—	−1	—	—	−1	μA
Input Offset Current		—	—	100	—	—	100	nA
Minimum Output Swing		0.4	—	18	0.4	—	18	V
Output Sink Current	V_O = 5V	1	10	30	1	10	30	mA
Output Source Current	V_O = 0V	−1	−10	−20	−1	−10	−20	mA
A_{VOL}	V_O = 1 to 11V	100	120	—	100	120	—	dB
CMRR	V_{IN} = 1 to 11V	70	80	—	70	80	—	dB
PSRR	V_{CC} = 10 to 20V	70	100	—	70	100	—	dB
Gain Bandwidth*		0.6	0.8	—	0.6	0.8	—	MHz
Reset Drive Section								
Input Leakage	V_{DR} = 30V	—	—	10	—	—	10	μA
Output Leakage	V_R = −80V	—	—	−100	—	—	−100	μA
Input Current	I_R = −50mA, V_R = 0	—	−1	−2	—	−1	−2	mA
Maximum Reset Current	I_{DR} = −3mA, V_R = 0	−90	−120	−200	−90	−120	−200	mA
Transconductance	I_R = −10 to −50mA	.03	.04	.05	.03	.04	.05	A/V

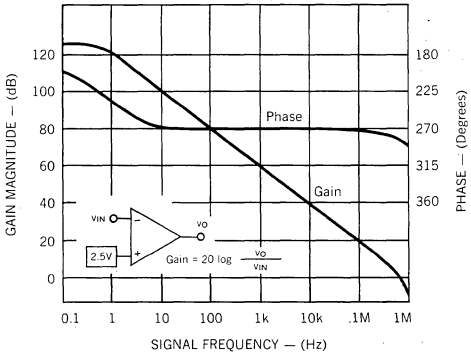
NOTE: These parameters guaranteed by design and not 100% tested in production.

TYPICAL APPLICATION

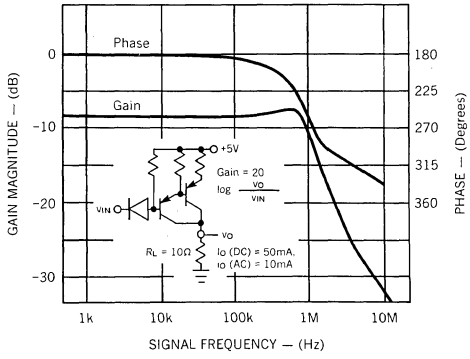


UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • TELEX 95-3040

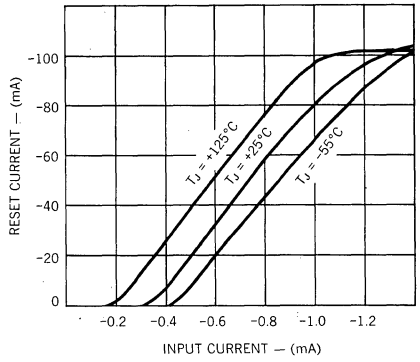
Amplifier Open-Loop Response



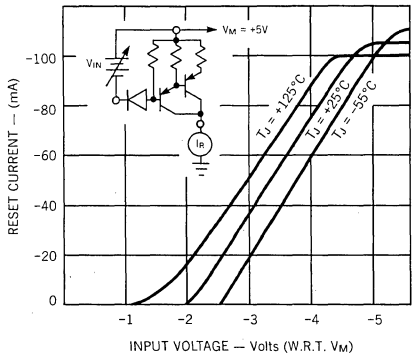
Reset Driver Response



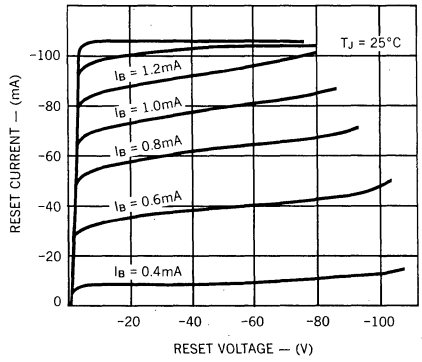
Reset Driver — Input Current



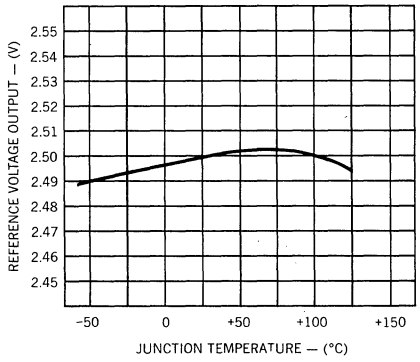
Reset Driver — Input Voltage



Reset Driver — Output Impedance



Reference Temperature Coefficient



LINEAR INTEGRATED CIRCUITS
Programmable, Off-Line, PWM Controller

UC1840
UC2840
UC3840

3

FEATURES
- All control, driving, monitoring, and protection functions included
- Low-current, off-line start circuit
- Feed-forward line regulation over 4 to 1 input range
- PWM latch for single pulse per period
- Pulse-by-pulse current limiting plus shutdown for over-current fault
- No start-up or shutdown transients
- Slow turn-on and maximum duty-cycle clamp
- Shutdown upon over- or under-voltage sensing
- Latch off or continuous retry after fault
- Remote, pulse-commandable start/stop
- PWM output switch usable to 1A peak current
- 1% reference accuracy
- 500kHz operation
- 18-pin DIL package

DESCRIPTION
Although containing most of the features required by all types of switching power supply controllers, the UC1840 family has been optimized for highly-efficient boot-strapped primary-side operation in forward or flyback power converters. Two important features for this mode are a starting circuit which requires little current from the primary input voltage and feed-forward control for constant volt-second operation over a wide input voltage range.

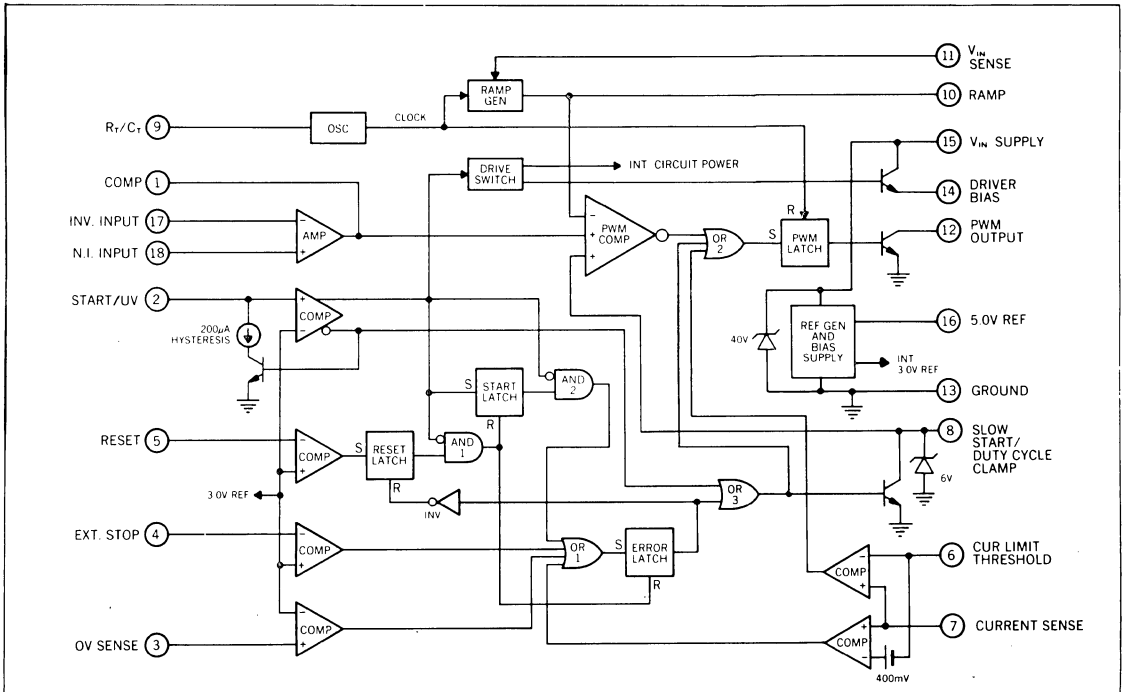
In addition to startup and normal regulating PWM functions, these devices offer built-in protection from over-voltage, under-voltage, and over-current fault conditions. This monitoring circuitry contains the added features that any fault will initiate a complete shutdown with provisions for either latch off or automatic restart. In the latch-off mode, the controller may be started and stopped with external pulsed or steady-state commands.

Other performance features of these devices include a 1% accurate reference, provision for slow-turn-on and duty-cycle limiting, and high-speed pulse-by-pulse current limiting in addition to current fault shutdown.

The UC1840's PWM output stage includes a latch to insure only a single pulse per period and is designed to optimize the turn off of an external switching device by conducting during the "OFF" time with a capability for both high peak current and low saturation voltage. These devices are available in an 18-pin dual-in-line plastic or ceramic package.

The UC1840 is characterized for operation over the full military temperature range of −55°C to +125°C. The UC2840 and UC3840 are designed for operation from −25°C to +85°C and 0°C to +70°C, respectively.

BLOCK DIAGRAM



Note: Positive true logic, latch outputs high with set, reset has priority.

UNITRODE

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, $+V_{IN}$ (Pin 15)
- Voltage Driven ..... +32V
- Current Driven, 100mA maximum ..... Self-limiting

PWM Output Voltage (Pin 12) 40V
PWM Output Current, Steady-State (Pin 12) 400mA
PWM Output Peak Energy Discharge 20μJoules
Driver Bias Current (Pin 14) ..... -200mA
Reference Output Current (Pin 16) ..... -50mA
Slow-Start Sink Current (Pin 8) 20mA
V_{IN} Sense Current (Pin 11) 10mA
Current Limit Inputs (Pins 6 & 7) ..... -0.5 to +5.5V
Comparator Inputs (Pins 2, 3, 4, 5, 17, 18) ..... -0.3 to +32V
Power Dissipation at T_A = 25°C 1000mW
- Derate at 10 mW/°C for T_A above 50°C

Power Dissipation at T_C = 25°C 2000mW
- Derate at 16 mW/°C for T_C above 25°C

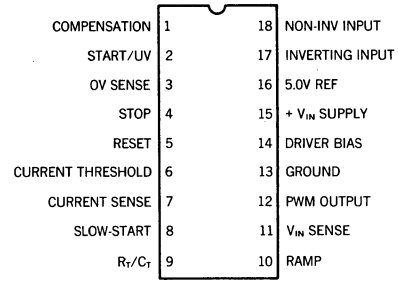
Thermal Resistance, Junction to Ambient ..... 100°C/W
Thermal Resistance, Junction to Case ..... 60°C/W
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Notes: 1. All voltages are with respect to ground, Pin 13.
Currents are positive-into, negative-out of the specified terminal.

CONNECTION DIAGRAM

DIL-18 (TOP VIEW)
J or N PACKAGE

UC1840
UC2840
UC3840



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1840, -25°C to +85°C for the UC2840, and 0°C to 70°C for the UC3840; V_{IN} = 20V, R_T = 20k, C_T = .001mfd, C_R = .001mfd, Current Limit Threshold = 200mV)

PARAMETER	TEST CONDITIONS	UC1840 UC2840			UC3840			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Power Inputs								
Start-Up Current	V_{IN} = 30V, Pin 2 = 2.5V, T_J = 25°C		4	5.5		4	5.5	mA
Start-Up Current T.C.*	V_{IN} = 30V, Pin 2 = 2.5V		-0.1	-0.2		-0.1	-0.2	%/°C
Operating Current	V_{IN} = 30V, Pin 2 = 3.5V	5	10	15	5	10	15	mA
Supply OV Clamp	I_{IN} = 20mA	33	40	45	33	40	48	V
Reference Section								
Reference Voltage	T_J = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	V_{IN} = 8 to 30V		10	15		10	20	mV
Load Regulation	I_L = 0 to 20mA		10	20		10	30	mV
Temperature Coefficient*	Over operating temperature range			±0.4			±0.4	mV/°C
Short Circuit Current	V_{REF} = 0, T_J = 25°C		-80	-100		-80	-100	mA
Oscillator								
Nominal Frequency	T_J = 25°C	47	50	53	45	50	55	kHz
Voltage Stability	V_{IN} = 8 to 30V		0.5	1		0.5	1	%
Temperature Coefficient*	Over operating temperature range			±.08			±.08	%/°C
Maximum Frequency	R_T = 2kΩ, C_T = 330pF	500			500			kHz
Ramp Generator								
Ramp Current, Minimum	I_{SENSE} = -10μA		-11	-14		-11	-14	μA
Ramp Current, Maximum	I_{SENSE} = 1.0mA	-0.9	-.95		-0.9	-.95		mA
Ramp Valley		0.3	0.5	0.7	0.3	0.5	0.7	V
Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	V

*Guaranteed by design. Not 100% tested in production.

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ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1840, −25°C to +85°C for the UC2840, and 0°C to 70°C for the UC3840; V_{IN} = 20V, R_T = 20k, C_T = .001mfd, C_R = .001mfd, Current Limit Threshold = 200mV)

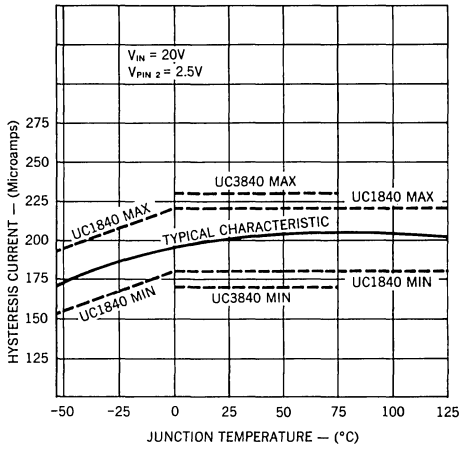
PARAMETER	TEST CONDITIONS	UC1840 UC2840			UC3840			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Error Amplifier								
Input Offset Voltage	V_{CM} = 5.0V		0.5	5		2	10	mV
Input Bias Current			0.5	2		1	5	μA
Input Offset Current				0.5			0.5	μA
Open Loop Gain	ΔV_O = 1 to 3V	60	66		60	66		dB
Output Swing (Max. Output ≤ Ramp Peak − 100mV)	Minimum Total Range	0.3		3.5	0.3		3.5	V
CMRR	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
PSRR	V_{IN} = 8 to 30V	40	50		40	50		dB
Short Circuit Current	V_{COMP} = 0V		−4	−10		−4	−10	mA
Gain Bandwidth*	T_J = 25°C, A_{VOL} = 0dB	1	2		1	2		MHz
Slew Rate*	T_J = 25°C, A_{VCL} = 0dB		0.8			0.8		V/μs
PWM Section								
Continuous Duty Cycle Range* (other than zero)	Minimum Total Continuous Range Ramp Peak < 4.2V	5		95	5		95	%
Output Saturation	I_{OUT} = 20mA		0.2	0.4		0.2	0.4	V
Output Saturation	I_{OUT} = 200mA		1.7	2.2		1.7	2.2	V
Output Leakage	V_{OUT} = 40V		0.1	10		0.1	10	μA
Comparator Delay*	Pin 8 to Pin 12 T_J = 25°C, R_L = 1kΩ		300	500		300	500	ns
Sequencing Functions								
Comparator Thresholds	Pins 2, 3, 4, 5	2.8	3.0	3.2	2.8	3.0	3.2	V
Input Bias Current	Pins 3, 4, 5 = 0V		−1.0	−3.0		−1.0	−3.0	μA
Start/UV Hysteresis Current	Pin 2 = 2.5V, T_J = 25°C	180	200	220	170	200	230	μA
Input Leakage	Input V = 20V		0.1	10		0.1	10	μA
Driver Bias Saturation Voltage, $V_{IN} - V_{OH}$	I_B = −50mA		2	3		2	3	V
Driver Bias Leakage	V_B = 0V		−0.1	−10		−0.1	−10	μA
Slow-Start Saturation	I_S = 2mA		0.2	0.5		0.2	0.5	V
Slow-Start Leakage	V_S = 4.5V		0.1	2.0		0.1	2.0	μA
Current Control								
Current Limit Offset			0	5		0	10	mV
Current Shutdown Offset		370	400	430	360	400	440	mV
Input Bias Current	Pin 7 = 0V		−2	−5		−2	−5	μA
Common Mode Range*		−0.4		3.0	−0.4		3.0	V
Current Limit Delay*	T_J = 25°C, Pin 7 to 12, R_L = 1k		200	400		200	400	ns

*Guaranteed by design. Not 100% tested in production.

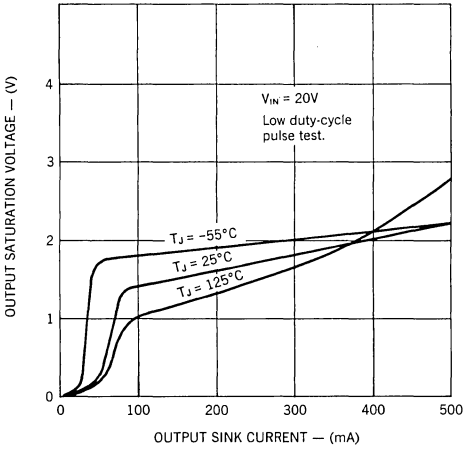
FUNCTIONAL DESCRIPTION

PWM CONTROL	
1. Oscillator:	Generates a fixed-frequency internal clock from an external R_T and C_T. Frequency $= \frac{K_c}{R_T C_T}$ where K_c is a first-order correction factor $\approx 0.3 \log (C_T \times 10^{12})$.
2. Ramp Generator:	Develops a linear ramp with a slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R C_R}$ C_R is normally selected $\leq C_T$ and its value will have some effect upon valley voltage. C_R terminal can be used as an input port for current mode control.
3. Error Amplifier:	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance; unity-gain stable.
4. Reference Generator:	Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of $\pm$ 2%. 40V clamp zener for chip OV protection, 100mA maximum current.
5. PWM Comparator:	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
6. PWM Latch:	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets with each internal clock pulse.
7. PWM Output Switch:	Transistor capable of sinking current to ground which is off during the PWM on-time and turns on to terminate the power pulse. Current capacity is 400mA saturated with peak capacitance discharge in excess of one amp.
SEQUENCING FUNCTIONS	
1. Start/UV Sense:	This comparator performs three functions— With an increasing voltage, it generates a turn-on signal at a start threshold. With a decreasing voltage, it generates a UV fault signal at a lower level separated by a 200μA hysteresis current. At the UV threshold, it also resets the Error Latch if the Reset Latch has been set.
2. Drive Switch:	Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
3. Driver Bias:	Supplies drive current to external power switch to provide turn-on bias.
4. Slow Start:	Clamps low to hold PWM OFF. Upon release, rises with rate controlled by $R_S C_S$ for slow increase of output pulse width. Also used to clamp maximum duty cycle with divider R_S R_{DC}.
5. Start Latch:	Keeps low input voltage at initial turn-on from being defined as a UV fault. Sets at start level to monitor for UV fault.
6. Reset Latch:	When reset, this latch insures no reset signal to either Start or Error latches so that first fault will lock the PWM off. When set, this latch resets the Start and Error latches at the UV low threshold, allowing a restart.
PROTECTION FUNCTIONS	
1. Error Latch:	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. UV low (after turn-on) b. OV high c. Stop low d. Current Sense 400mV over threshold. Error Latch resets at UV threshold if Reset Latch is set.
2. Current Limiting:	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400mV above threshold, a shutdown signal is sent to Error Latch.

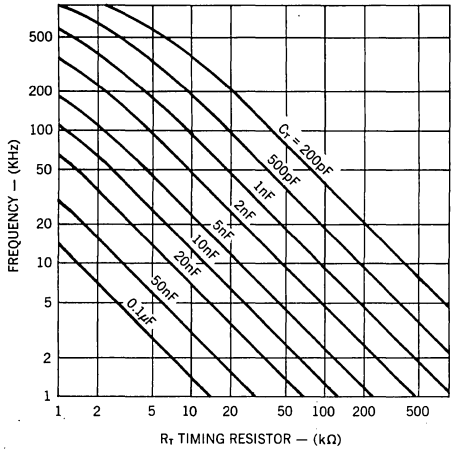
Start/UV Hysteresis Current



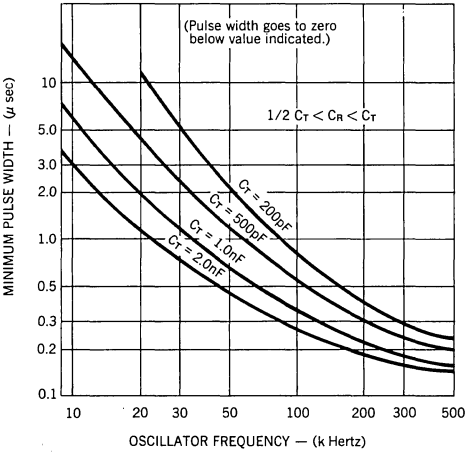
PWM Output Saturation Voltage



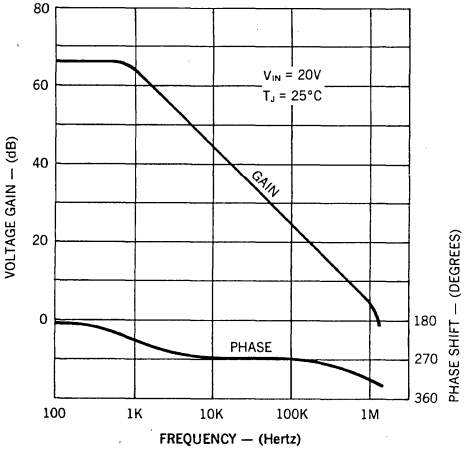
Oscillator Frequency



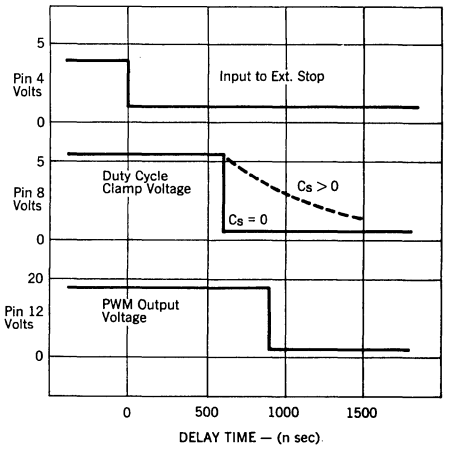
PWM Output Minimum Pulse Width



Error Amplifier Open-Loop Gain and Phase



Shutdown Timing



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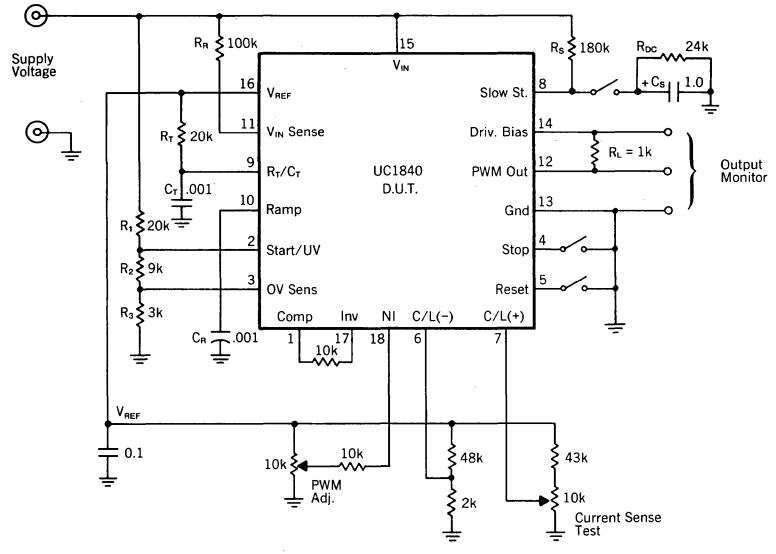
OPEN-LOOP TEST CIRCUIT



Nominal Frequency = $\frac{1}{R_T C_T}$ = 50kHz

Start Voltage = $3\left(\frac{R_1 + R_2 + R_3}{R_2 + R_3}\right) + 0.2R_1 = 12V$

UV Fault Voltage = $3\left(\frac{R_1 + R_2 + R_3}{R_2 + R_3}\right) = 8V$

OV Fault Voltage = $3\left(\frac{R_1 + R_2 + R_3}{R_3}\right) = 32V$

Current Limit = 200mV
Current Fault Voltage = 600mV
Duty Cycle Clamp = 50%

FLYBACK APPLICATION (A)

In this application (see Figure A, next page), complete control is maintained on the primary side. Control power is provided by R_{IN} and C_{IN} during start-up, and by a primary-referenced low voltage winding, N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling — a task made even easier with the UC1840's feed-forward line regulation.

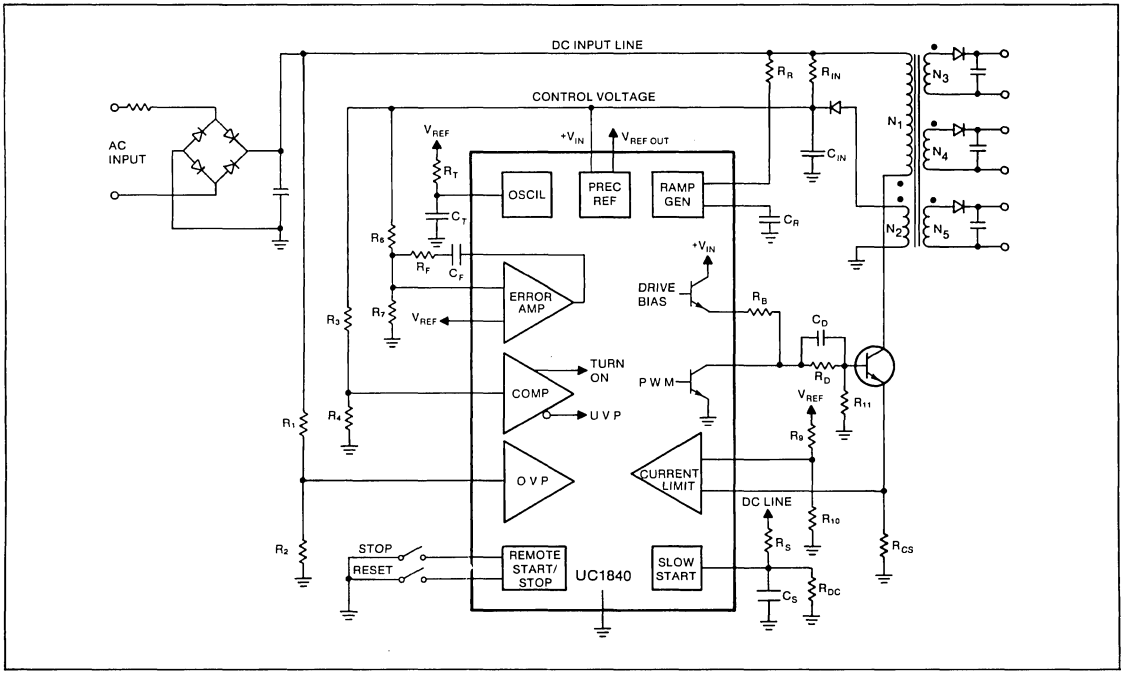
An extension to this application for more precise regulation would be the use of the UC1901 Isolated Feedback Generator for direct closed-loop control to an output. The UC1840 will readily accept digital start/stop commands transmitted from the secondary side by means of optical couplers.

Not shown are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Qs, or the application.

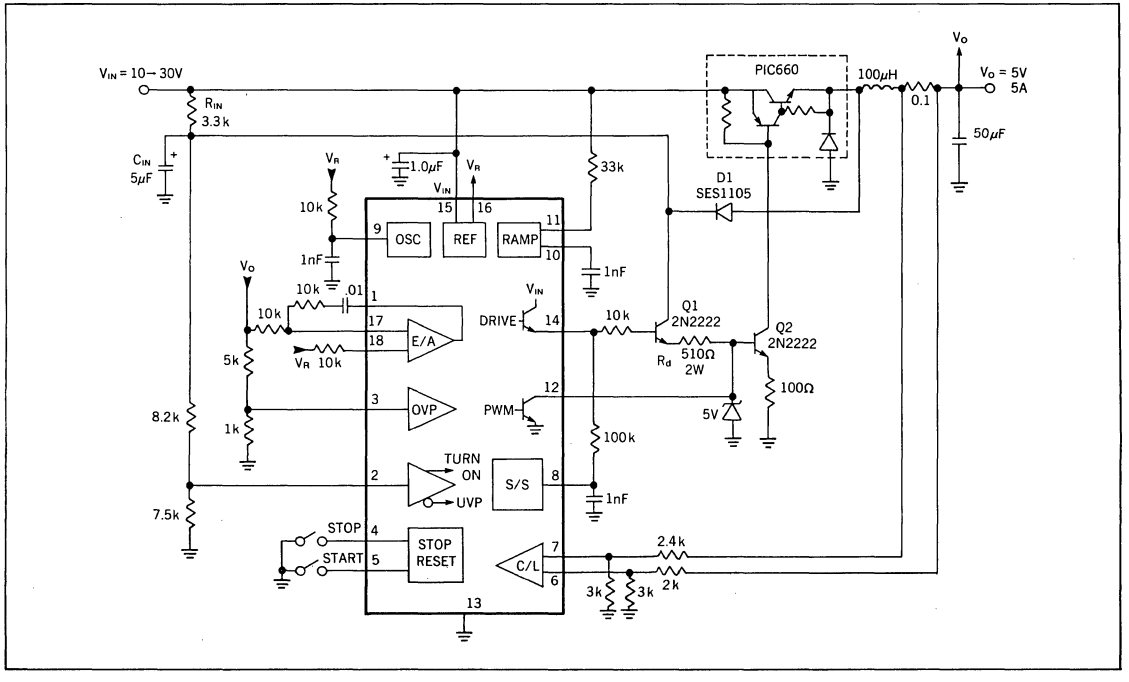
REGULATOR APPLICATION (B)

Although primarily intended for transformer-coupled power systems, the UC1840's advantages of feed-forward for high ripple-rejection, a fully contained fault monitoring system and remote start/stop capability make it worth considering for other types of regulators. Since the fault logic within the UC1840 requires recycling the voltage sensed by the Start/UV Comparator to reset the error latch, a need for automatic restart must be addressed in a manner similar to that shown in Figure B (next page). In this simple, non-isolated, buck regulator; diode D1 provides a low-impedence bootstrapped drive power source after start-up is achieved through R_{IN} and C_{IN}. When a fault shutdown terminates switching action, the loading of Q1 and R_d will lower the voltage on pin 2 to effect an automatic re-start attempt which will continuously recycle until the fault is removed.

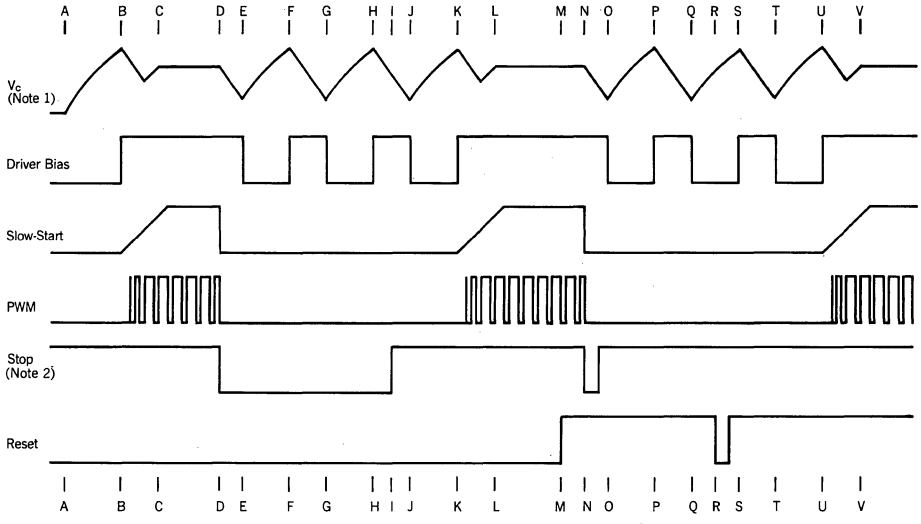
UC1840 PROGRAMMABLE PWM CONTROLLER IN A SIMPLIFIED FLYBACK REGULATOR (A)



UC1840 CONTROLS A HIGH-CURRENT NON-ISOLATED BUCK REGULATOR (B)



UC1840 POWER SEQUENCING FUNCTIONS



Notes: 1. VC represents an analog of the output voltage generated by a primary-referenced secondary winding on the power transformer. It is the voltage monitored by the start/UV comparator and, in most cases, is the supply voltage, V_{IN}, for the UC1840.

2. Although input to External Stop, Pin 4, is shown, results are the same for any fault input which sets the Error Latch.

UC1840 POWER SEQUENCING FUNCTIONS

TIME	EVENT
A	Initial turn-on, V_C rises with light load
B	Start threshold. Driver Bias loads V_C
C	Operating PWM regulates V_C
D	Stop input sets Error Latch turning off PWM
E	UV low threshold, Error Latch remains set
F	Start turns on Driver Bias but Error Latch still set
G, H	V_C and Driver Bias continue to cycle
I	Stop command removed
J	Error Latch reset at UV low threshold
K	Start threshold now removes slow-start clamp
L	Return to normal run state
M	Reset Latch set signal removed
N	Error Latch set with momentary fault
O	Error Latch does not reset as Reset Latch is reset
P, Q	V_C and Driver Bias recycle with no turn-on.
R	Reset Latch set is set with momentary Reset signal
S	V_C must complete cycle to turn-on
T	Start and Error Latches reset
U	Normal start initiated
V	Return to normal run state

LINEAR INTEGRATED CIRCUITS

Programmable, Off-Line, PWM Controller

UC1841
UC2841
UC3841
PRELIMINARY

3

FEATURES

- All control, driving, monitoring, and protection functions included
- Low-current, off-line start circuit
- Voltage feed forward or current mode control
- Guaranteed duty cycle clamp
- PWM latch for single pulse per period
- Pulse-by-pulse current limiting plus shutdown for over-current fault
- No start-up or shutdown transients
- Slow turn-on both initially and after fault shutdown
- Shutdown upon over- or under-voltage sensing
- Latch off or continuous retry after fault
- PWM output switch usable to 1A peak current
- 1% reference accuracy
- 500kHz operation
- 18-pin DIL package

DESCRIPTION

The UC1841 family of PWM controllers has been designed to increase the level of versatility while retaining all of the performance features of the earlier UC1840 devices. While still optimized for highly-efficient boot-strapped primary-side operation in forward or flyback power converters, the UC1841 is equally adept in implementing both low and high voltage input DC to DC converters. Important performance features include a low-current starting circuit, linear feed-forward for constant volt-second operation, and compatibility with either voltage or current mode topologies.

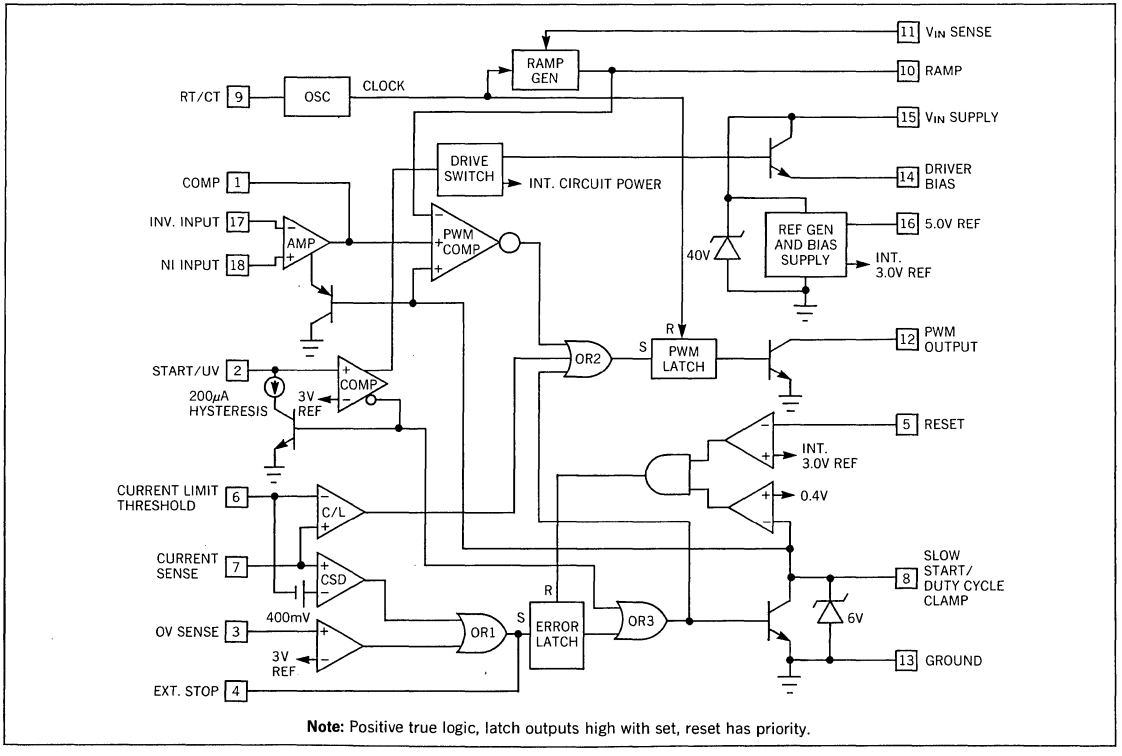
In addition to start-up and normal regulating PWM functions, these devices include built in protection from over-voltage, under-voltage, and over-current fault conditions with the option for either latch-off or automatic restart.

While pin compatible with the UC1840 in all respects except that the polarity of the External Stop has been reversed, the UC1841 offers the following improvements:

1. Fault latch reset is accomplished with slow start discharge rather than recycling the input voltage to the chip.
2. The External Stop input can be used for a fault delay to resist shutdown from short duration transients.
3. The duty-cycle clamping function has been characterized and specified.

These devices are packaged in 18-pin plastic or ceramic dual-in-line packages with the UC1841 characterized for −55°C to +125°C operation while the UC2841 and UC3841 are designed for −25°C to +85°C and 0°C to +70°C, respectively.

BLOCK DIAGRAM (Pin numbers shown for DIL-18 package)



Note: Positive true logic, latch outputs high with set, reset has priority.

UNITRODE

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, $+V_{IN}$ (Pin 15)
- Voltage Driven ..... +32V
- Current Driven, 100mA maximum ..... Self-limiting

PWM Output Voltage (Pin 12) 40V
PWM Output Current, Steady-State (Pin 12) 400mA
PWM Output Peak Energy Discharge 20μJoules
Driver Bias Current (Pin 14) ..... -200mA
Reference Output Current (Pin 16) ..... -50mA
Slow-Start Sink Current (Pin 8) 20mA
V_{IN} Sense Current (Pin 11) 10mA
Current Limit Inputs (Pins 6 & 7) ..... -0.5 to +5.5V
Stop Input (Pin 4) ..... -0.3 to +5.5V
Comparator Inputs
- (Pins 2, 3, 5, 17, 18) ..... Internally clamped at 12V

Power Dissipation at T_A = 25°C 1000mW
- Derate at 10mW/°C for T_A above 50°C

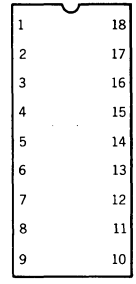
Power Dissipation at T_C = 25°C 2000mW
- Derate at 16mW/°C for T_C above 25°C

Thermal Resistance, Junction to Ambient ..... 100°C/W
Thermal Resistance, Junction to Case ..... 60°C/W
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

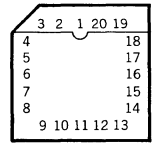
Notes: 1. All voltages are with respect to ground, Pin 13.
Currents are positive-into, negative-out of the specified terminal.
2. All pin numbers are referenced to DIL-18 package.

CONNECTION DIAGRAMS

TOP VIEWS
DIL-18, J or N PACKAGE



PLCC-20
Q PACKAGE



PACKAGE PIN FUNCTIONS

FUNCTION	DIL	PLCC
COMP	1	1
START/UV	2	2
OV SENSE	3	3
STOP	4	4
RESET	5	5
CUR THRESH	6	7
CUR SENSE	7	8
SLOW START	8	9
RT/CT	9	10
RAMP	10	11
V_{IN} SENSE	11	12
PWM OUT	12	13
GROUND	13	14
DRIV BIAS	14	15
$+V_{IN}$ SUPPLY	15	17
5.0V REF	16	18
INV INPUT	17	19
N.I. INPUT	18	20

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1841, -25°C to +85°C for the UC2841, and 0°C to 70°C for the UC3841; V_{IN} = 20V, R_T = 20kΩ, C_T = .001mfd, R_R = 10kΩ, C_R = .001mfd, Current Limit Threshold = 200mV)

PARAMETER	TEST CONDITIONS	UC1841 UC2841			UC3841			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Power Inputs								
Start-Up Current	V_{IN} = 30V, Pin 2 = 2.5V,		4	5		4	5	mA
Operating Current	V_{IN} = 30V, Pin 2 = 3.5V		9	12		9	12	mA
Supply OV Clamp	V_{IN} = 20mA	33	40	45	33	40	45	V
Reference Section								
Reference Voltage	T_J = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	V_{IN} = 8 to 30V		10	15		10	20	mV
Load Regulation	I_L = 0 to 10mA		10	20		10	30	mV
Temperature Coefficient*	Over operating temperature range			±0.4			±0.4	mV/°C
Short Circuit Current	V_{REF} = 0, T_J = 25°C		-80	-100		-80	-100	mA
Oscillator								
Nominal Frequency	T_J = 25°C	47	50	53	45	50	55	kHz
Voltage Stability	V_{IN} = 8 to 30V		0.5	1		0.5	1	%
Temperature Coefficient*	Over operating temperature range			±.08			±.08	%/°C
Maximum Frequency	R_T = 2kΩ, C_T = 330pF	500			500			kHz
Ramp Generator								
Ramp Current, Minimum	I_{SENSE} = -10μA		-11	-14		-11	-14	μA
Ramp Current, Maximum	I_{SENSE} = 1.0mA	-0.9	-.95		-0.9	-.95		mA
Ramp Valley		0.3	0.4	0.6	0.3	0.4	0.6	V
Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	V

*Guaranteed by design. Not 100% tested in production.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1841, −25°C to +85°C for the UC2841, and 0°C to 70°C for the UC3841; V_{IN} = 20V, R_T = 20kΩ, C_T = .001mfd, R_R = 10kΩ, C_R = .001mfd, Current Limit Threshold = 200mV)

PARAMETER	TEST CONDITIONS	UC1841 UC2841			UC3841			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Error Amplifier								
Input Offset Voltage	V_{CM} = 5.0V		0.5	5		2	10	mV
Input Bias Current			0.5	2		1	5	μA
Input Offset Current				0.5			0.5	μA
Open Loop Gain	ΔV_O = 1 to 3V	60	66		60	66		dB
Output Swing (Max. Output ≤ Ramp Peak − 100mV)	Minimum Total Range	0.3		3.5	0.3		3.5	V
CMRR	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
PSRR	V_{IN} = 8 to 30V	40	50		40	50		dB
Short Circuit Current	V_{COMP} = 0V		−4	−10		−4	−10	mA
Gain Bandwidth*	T_J = 25°C, A_{VOL} = 0dB	1	2		1	2		MHz
Slew Rate*	T_J = 25°C, A_{VCL} = 0dB		0.8			0.8		V/μs
PWM Section								
Continuous Duty Cycle Range* (other than zero)	Minimum Total Continuous Range Ramp Peak < 4.2V	4		95	4		95	%
50% Duty Cycle Clamp	R_{SENSE} to V_{REF} = 10k	42	47	52	42	47	52	%
Output Saturation	I_{OUT} = 20mA		0.2	0.4		0.2	0.4	V
Output Saturation	I_{OUT} = 200mA		1.7	2.2		1.7	2.2	V
Output Leakage	V_{OUT} = 40V		0.1	10		0.1	10	μA
Comparator Delay*	Pin 8 to Pin 12 T_J = 25°C, R_L = 1kΩ		300	500		300	500	ns
Sequencing Functions								
Comparator Thresholds	Pins 2, 3, 5	2.8	3.0	3.2	2.8	3.0	3.2	V
Input Bias Current	Pins 3, 5 = 0V		−1.0	−4.0		−1.0	−4.0	μA
Input Leakage	Pins 3, 5 = 10V		0.1	2.0		0.1	2.0	μA
Start/UV Hysteresis Current	Pin 2 = 2.5V,	170	200	220	170	200	230	μA
Ext. Stop Threshold	Pin 4	0.8	1.2	2.4	0.8	1.2	2.4	V
Error Latch Activate Current	Pin 4 = 0V, Pin 3 > 3V		−120	−200		−120	−200	μA
Driver Bias Saturation Voltage, V_{IN} − V_{OH}	I_B = −50mA		2	3		2	3	V
Driver Bias Leakage	V_B = 0V		−0.1	−10		−0.1	−10	μA
Slow-Start Saturation	I_S = 10mA		0.2	0.5		0.2	0.5	V
Slow-Start Leakage	V_S = 4.5V		0.1	2.0		0.1	2.0	μA
Current Control								
Current Limit Offset			0	5		0	10	mV
Current Shutdown Offset		370	400	430	360	400	440	mV
Input Bias Current	Pin 7 = 0V		−2	−5		−2	−5	μA
Common Mode Range*		−0.4		3.0	−0.4		3.0	V
Current Limit Delay*	T_J = 25°C, Pin 7 to 12, R_L = 1k		200	400		200	400	ns

*Guaranteed by design. Not 100% tested in production.

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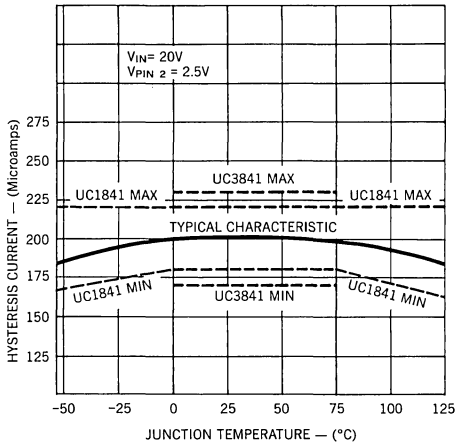
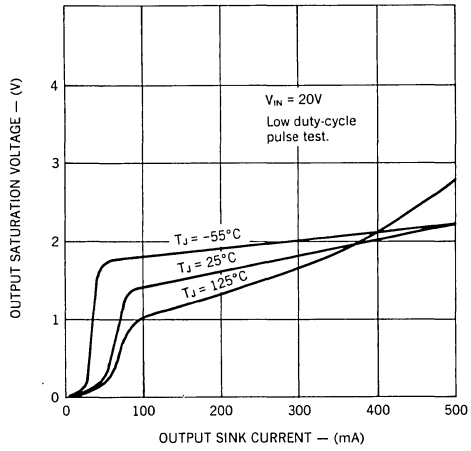
FUNCTIONAL DESCRIPTION

PWM CONTROL	
1. Oscillator:	Generates a fixed-frequency internal clock from an external R_T and C_T. Frequency = $\frac{K_c}{R_T C_T}$ where K_c is a first-order correction factor $\approx 0.3 \log (C_T \times 10^{12})$.
2. Ramp Generator:	Develops linear ramp with slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R C_R}$ C_R is normally selected $\leq C_T$ and its value will have some effect upon valley voltage. Limiting the minimum value for I_{SENSE} into pin 11 will establish a maximum duty cycle clamp. C_R terminal can be used as an input port for current mode control.
3. Error Amplifier:	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance; unity-gain stable. The output is held low by the slow start voltage at turn on in order to minimize overshoot.
4. Reference Generator:	Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of $\pm$ 2%. 40V clamp zener for chip OV protection, 100mA maximum current.
5. PWM Comparator:	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
6. PWM Latch:	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets with each internal clock pulse.
7. PWM Output Switch:	Transistor capable of sinking current to ground which is off during the PWM on-time and turns on to terminate the power pulse. Current capacity is 400mA saturated with peak capacitance discharge in excess of one amp.
SEQUENCING FUNCTIONS	
1. Start/UV Sense:	With an increasing voltage, this comparator generates a turn-on signal and releases the slow-start clamp at a start threshold. With a decreasing voltage, it generates a turn-off command at a lower level separated by a 200μA hysteresis current.
2. Drive Switch:	Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
3. Driver Bias:	Supplies drive current to external power switch to provide turn-on bias.
4. Slow Start:	Clamps low to hold PWM OFF. Upon release, rises with rate controlled by $R_S C_S$ for slow increase of output pulse width. Can also be used as an alternate maximum duty cycle clamp with an external voltage divider.
PROTECTION FUNCTIONS	
1. Error Latch:	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. OV > 3.0V b. Stop > 1.2V c. Current Sense 400mV over threshold. Error Latch resets when slow start voltage falls to 0.4V if Reset Pin 5 < 3.0V. With Pin 5 > 3.0V, Error Latch will remain set.
2. Current Limiting:	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400mV above threshold, a shutdown signal is sent to Error Latch.
3. Ext. Stop:	A voltage over 1.2V will set the Error Latch and hold the output off. A voltage less than 0.8V will defeat the error latch and prevent shutdown. A capacitor here will slow the action of the error latch for transient protection by providing a delay of 10ms/μF.

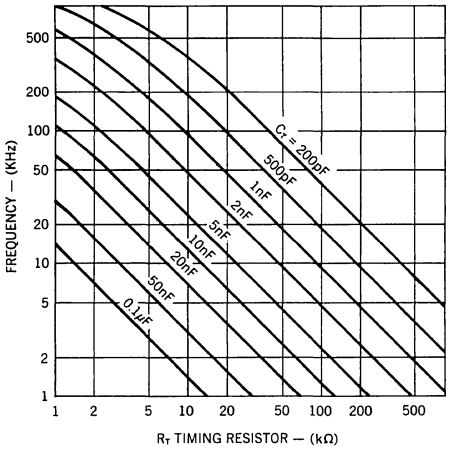
Start/UV Hysteresis Current



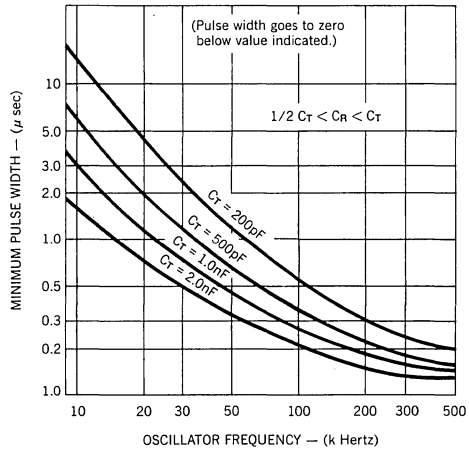
PWM Output Saturation Voltage



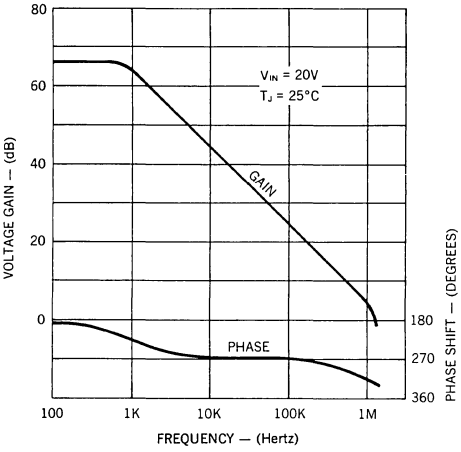
Oscillator Frequency



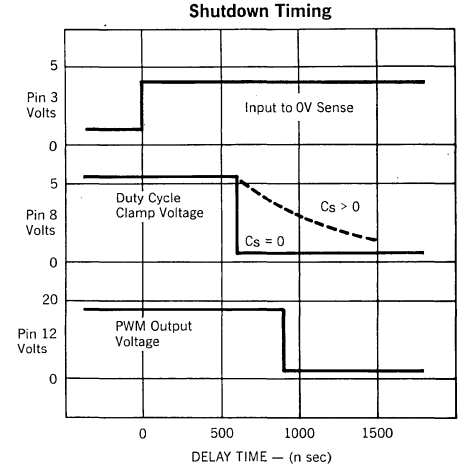
PWM Output Minimum Pulse Width



Error Amplifier Open-Loop Gain and Phase



Shutdown Timing



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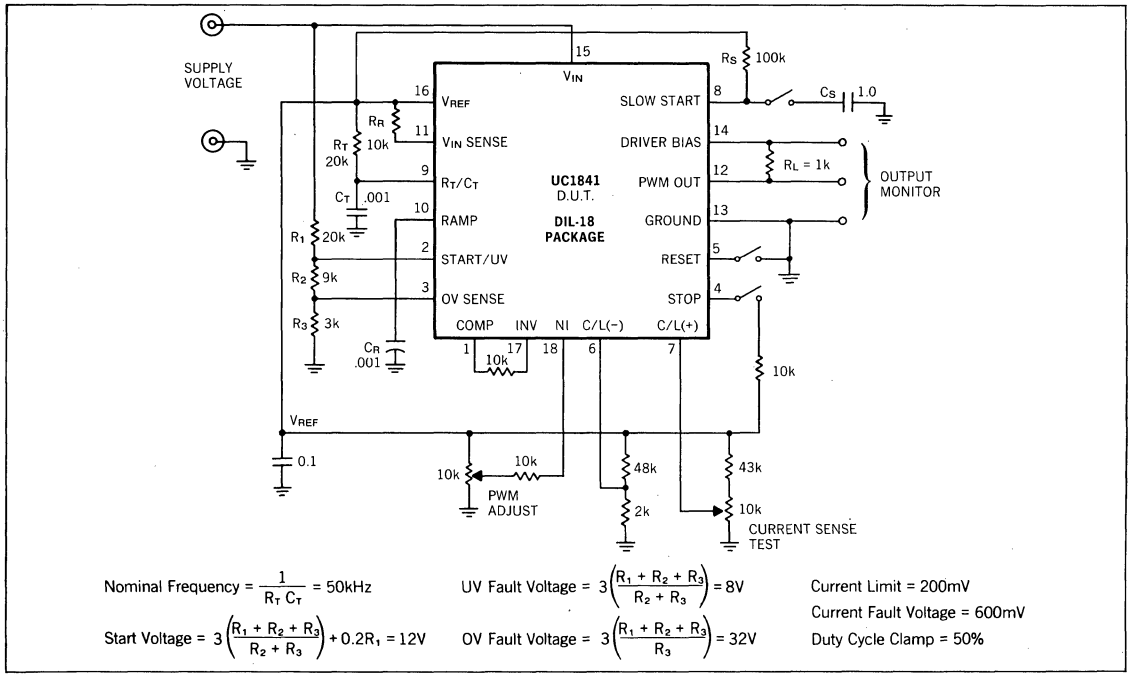
OPEN-LOOP TEST CIRCUIT



FLYBACK APPLICATION (A)

In this application (see Figure A, next page), complete control is maintained on the primary side. Control power is provided by R_{IN} and C_{IN} during start-up, and by a primary-referenced low voltage winding, N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling — a task made even easier with the UC1841's feed-forward line regulation.

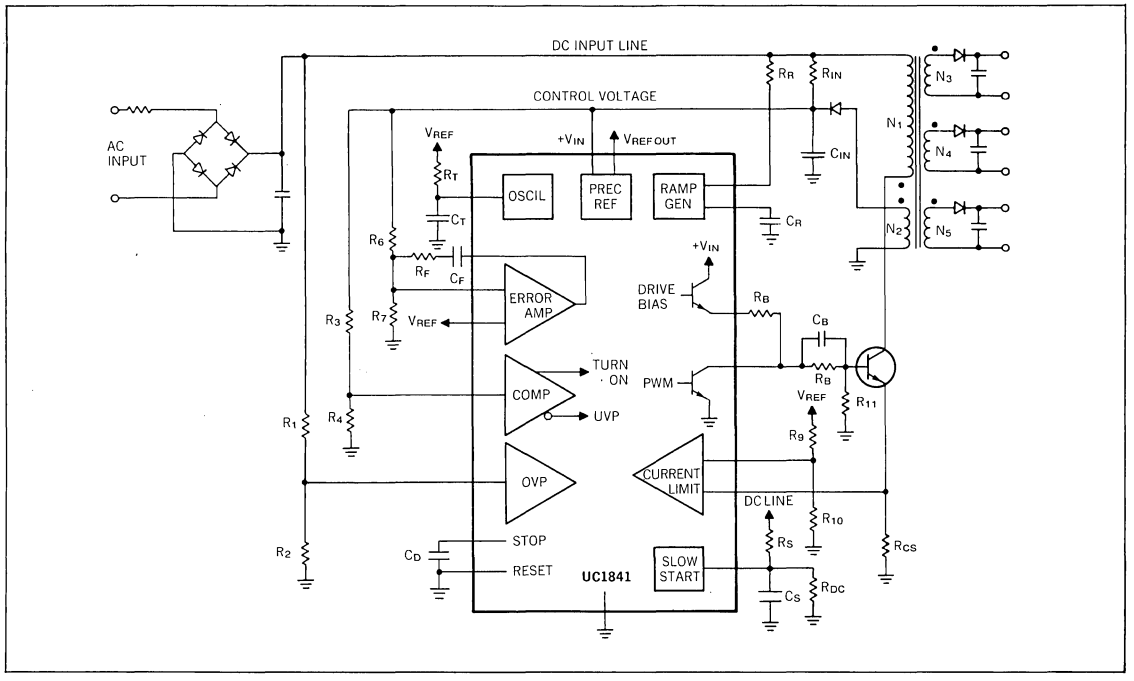
An extension to this application for more precise regulation would be the use of the UC1901 Isolated Feedback Generator for direct closed-loop control to an output.

Not shown, are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Qs, or the application; however, one example of power transistor interfacing is provided on the following page.

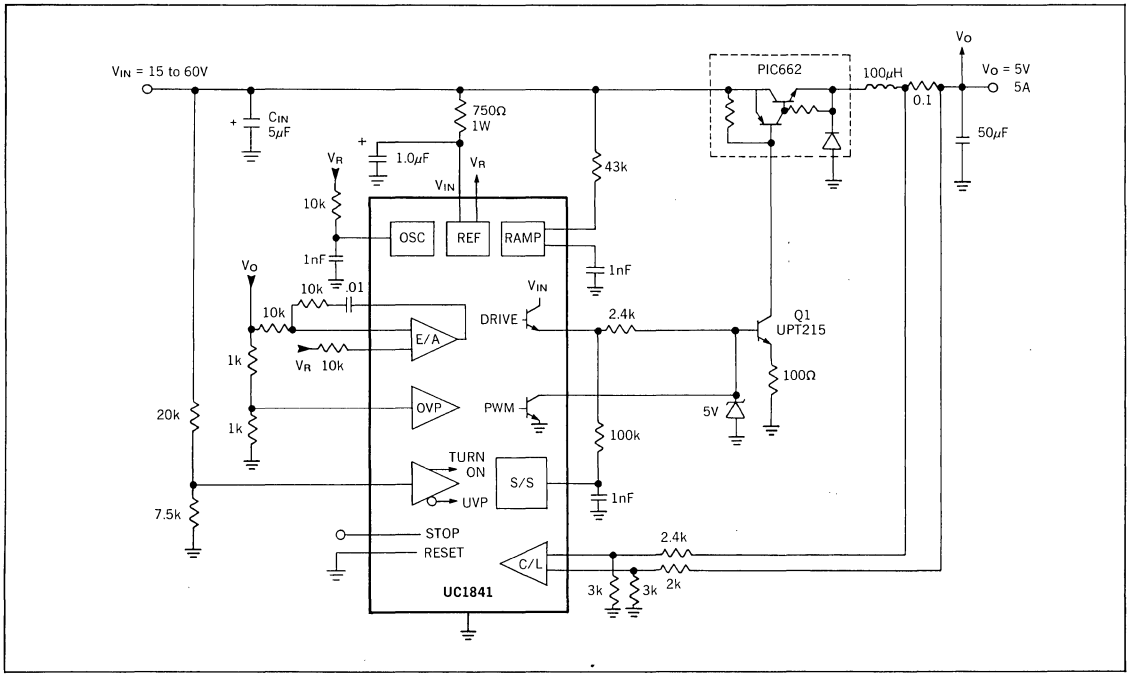
REGULATOR APPLICATION (B)

With the addition of a level shifting transistor, Q1, the UC1841 is an ideal control circuit for DC to DC converters such as the buck regulator shown in Figure B opposite. In addition to providing constant current drive pulses to the PIC661 power switch, this circuit has full fault protection and high speed dynamic line regulation due to its feed-forward capability. An additional feature is the ability to work with high input line voltages — in this case, up to 60V — with internal protective clamping.

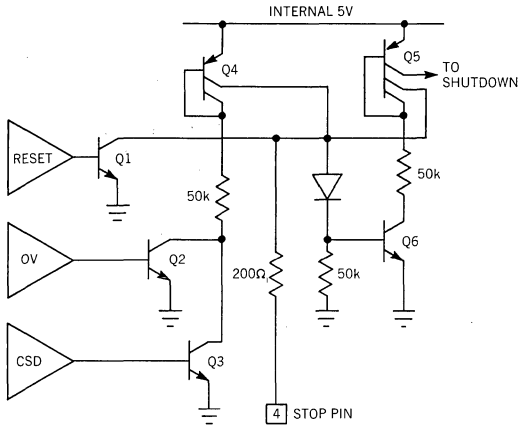
UC1841 PROGRAMMABLE PWM CONTROLLER IN A SIMPLIFIED FLYBACK REGULATOR (A)



UC1841 CONTROLS A HIGH-CURRENT, HIGH-INPUT VOLTAGE BUCK REGULATOR (B)

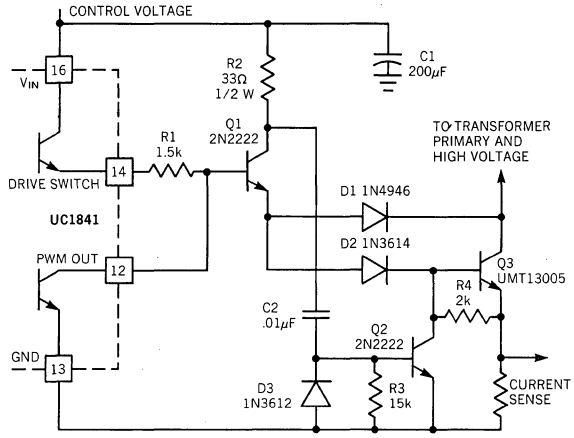


ERROR LATCH INTERNAL CIRCUITRY



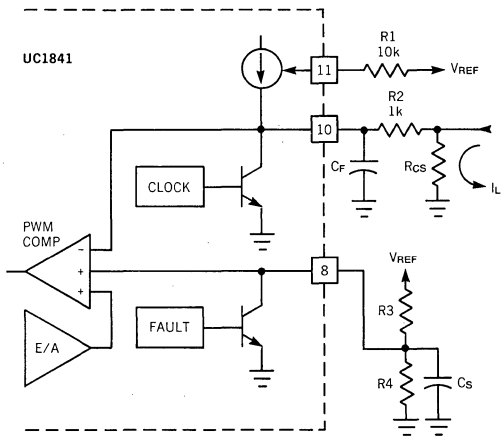
The Error Latch consists of Q5 and Q6 which, when both on, turns off the PWM Output and pulls the Slow-Start pin low. This latch is set by either the Over-Voltage or Current Shutdown comparators, or by a high signal on Pin 4. Reset is accomplished by either the Reset comparator or a low signal on Pin 4. An activation time delay can be provided with an external capacitor on Pin 4 in conjunction with the ≈ 100μA collector current from Q4.

INTERFACING HIGH-VOLTAGE BIPOLAR TRANSISTORS



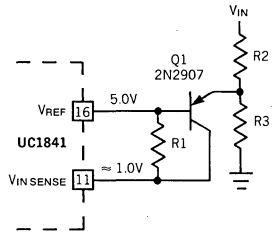
Most high voltage transistors trade both current gain and speed for voltage capability. This circuit provides both high turn-on and turn-off pulse base currents into Q3 as well as a Baker clamp saturation control. This entire drive circuit is held off by the UC1841's Drive Switch for low current drain while the control voltage is rising.

CURRENT MODE CONTROL



Since Pin 10 is a direct input to the PWM comparator, this point can also serve as a current sense port for current mode control. In this application, current sensing is ground referenced through R_{CS}. Resistor R1 sets a 400mV offset across R2 (assuming $R2 \gg R_{CS}$) so that both the Error Amplifier and Fault Shutdown can force the current completely to zero. R2 is also used along with C_F as a small filter to attenuate leading-edge spikes on the load current waveform. In this mode, current limiting can be accomplished by divider R3/R4 which forms a clamp overriding the output of the Error Amplifier.

VOLTAGE FEED-FORWARD COMBINED WITH MAXIMUM DUTY-CYCLE CLAMP



In this circuit, R1 is used in conjunction with C_R (not shown) to establish a minimum ramp charging current such that the ramp voltage reaches 4.2V at the required maximum output pulse width.

The purpose of Q1 is to provide an increasing ramp current above a threshold established by R2 and R3 such that the duty cycle is further reduced with increasing V_{IN}.

The minimum ramp current is:

$$I_R\,(MIN) = \frac{V_{REF} - V_{IN\,SENSE}}{R1} \approx \frac{4V}{R1}$$

The threshold where V_{IN} begins to add extra ramp current is:

$$V_{IN} \approx 5.6V \left(\frac{R2 + R3}{R3}\right)$$

Above the threshold, the ramp current will be:

$$I_R\,(VARIAB) \approx \frac{4}{R1} + \frac{V_{IN} - 5.6}{R2} - \frac{5.6}{R3}$$

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LINEAR INTEGRATED CIRCUITS

Current Mode PWM Controller

UC1842/3/4/5
UC2842/3/4/5
UC3842/3/4/5

FEATURES

- Optimized for off-line and DC to DC converters
- Low start up current (<1mA)
- Automatic feed forward compensation
- Pulse-by-pulse current limiting
- Enhanced load response characteristics
- Under-voltage lockout with hysteresis
- Double pulse suppression
- High current totem pole output
- Internally trimmed bandgap reference
- 500KHz operation
- Low R_O error amp

DESCRIPTION

The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N Channel MOSFETs, is low in the off state.

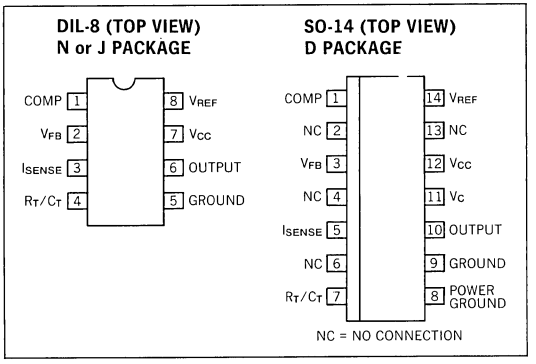
Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.5V and 7.9V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to < 50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

ABSOLUTE MAXIMUM RATINGS (Note 1)

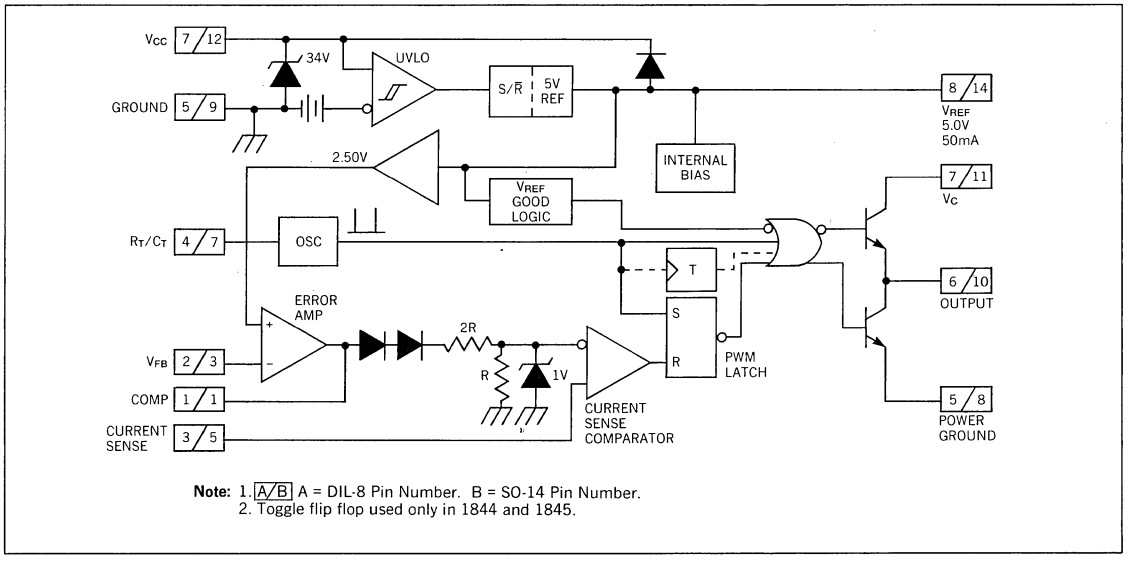
Supply Voltage (Low Impedence Source) 30V
Supply Voltage (I_{CC} < 30mA) ..... Self Limiting
Output Current ..... ±1A
Output Energy (Capacitive Load) 5µJ
Analog Inputs (Pins 2, 3) ..... -0.3V to +6.3V
Error Amp Output Sink Current 10mA
Power Dissipation at $T_A \leq 25°C$ (DIL-8) 1W
Derate 8mW/°C for $T_A > 25°C$
Power Dissipation at $T_A \leq 25°C$ (SO-14) 725mW
Derate 5.8mW/°C for $T_A > 25°C$
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note: 1. All voltages are with respect to Pin 5.
All currents are positive into the specified terminal.

CONNECTION DIAGRAM



BLOCK DIAGRAM



Note: 1. A/B A = DIL-8 Pin Number. B = SO-14 Pin Number.
2. Toggle flip flop used only in 1844 and 1845.

ELECTRICAL SPECIFICATIONS (Unless otherwise stated, these specifications apply for $-55 \leq T_A \leq 125°C$ for UC184X; $-25 \leq T_A \leq 85°C$ for UC284X; $0 \leq T_A \leq 70°C$ for UC384X; V_{CC} = 15V (Note 5); R_T = 10K; C_T = 3.3nF.)

PARAMETER	TEST CONDITIONS	UC184X UC284X			UC384X			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_j = 25°C, I_O = 1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	$12 \leq V_{IN} \leq 25V$		6	20		6	20	mV
Load Regulation	$1 \leq I_O \leq 20mA$		6	25		6	25	mV
Temp. Stability	(Note 2)		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp. (Note 2)	4.9		5.1	4.82		5.18	V
Output Noise Voltage	$10Hz \leq f \leq 10KHz$, T_j = 25°C (Note 2)		50			50		μV
Long Term Stability	T_A = 125°C, 1000 Hrs. (Note 2)		5	25		5	25	mV
Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
Oscillator Section								
Initial Accuracy	T_j = 25°C (Note 6)	47	52	57	47	52	57	KHz
Voltage Stability	$12 \leq V_{CC} \leq 25V$		0.2	1		0.2	1	%
Temp. Stability	$T_{MIN} \leq T_A \leq T_{MAX}$ (Note 2)		5			5		%
Amplitude	$V_{PIN\ 4}$ peak to peak		1.7			1.7		V
Error Amp Section								
Input Voltage	$V_{PIN\ 1}$ = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	-2	μA
A_{VOL}	$2 \leq V_O \leq 4V$	65	90		65	90		dB
Unity Gain Bandwidth	(Note 2)	0.7	1		0.7	1		MHz
PSRR	$12 \leq V_{CC} \leq 25V$	60	70		60	70		dB
Output Sink Current	$V_{PIN\ 2}$ = 2.7V, $V_{PIN\ 1}$ = 1.1V	2	6		2	6		mA
Output Source Current	$V_{PIN\ 2}$ = 2.3V, $V_{PIN\ 1}$ = 5V	-0.5	-0.8		-0.5	-0.8		mA
V_{OUT} High	$V_{PIN\ 2}$ = 2.3V, R_L = 15K to ground	5	6		5	6		V
V_{OUT} Low	$V_{PIN\ 2}$ = 2.7V, R_L = 15K to Pin 8		0.7	1.1		0.7	1.1	V
Current Sense Section								
Gain	(Notes 3 & 4)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	$V_{PIN\ 1}$ = 5V (Note 3)	0.9	1	1.1	0.9	1	1.1	V
PSRR	$12 \leq V_{CC} \leq 25V$ (Note 3)		70			70		dB
Input Bias Current			-2	-10		-2	-10	μA
Delay to Output			150	300		150	300	ns
Output Section								
Output Low Level	I_{SINK} = 20mA		0.1	0.4		0.1	0.4	V
	I_{SINK} = 200mA		1.5	2.2		1.5	2.2	V
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
	I_{SOURCE} = 200mA	12	13.5		12	13.5		V
Rise Time	T_j = 25°C, C_L = 1nF (Note 2)		50	150		50	150	ns
Fall Time	T_j = 25°C, C_L = 1nF (Note 2)		50	150		50	150	ns

Notes: 2. These parameters, although guaranteed, are not 100% tested in production.
3. Parameter measured at trip point of latch with $V_{PIN\ 2}$ = 0.
4. Gain defined as:

$$A = \frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}}; 0 \leq V_{PIN\ 3} \leq 0.8V.$$

5. Adjust V_{CC} above the start threshold before setting at 15V.
6. Output frequency equals oscillator frequency for the UC1842 and UC1843. Output frequency is one half oscillator frequency for the UC1844 and UC1845.

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7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
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ELECTRICAL SPECIFICATIONS (Unless otherwise stated, these specifications apply for $-55 \leq T_A \leq 125°C$ for UC184X; $-25 \leq T_A \leq 85°C$ for UC284X; $0 \leq T_A \leq 70°C$ for UC384X; V_{CC} = 15V (Note 5); R_T = 10K; C_T = 3.3nF.)

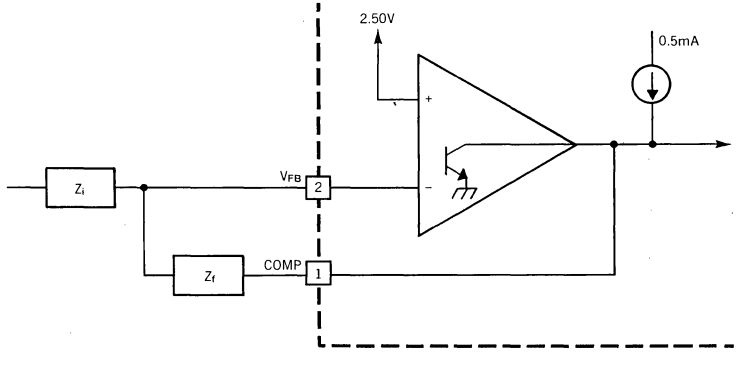
PARAMETER	TEST CONDITIONS	UC184X UC284X			UC384X			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Under-Voltage Lockout Section								
Start Threshold	X842/4	15	16	17	14.5	16	17.5	V
	X843/5	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operating Voltage After Turn On	X842/4	9	10	11	8.5	10	11.5	V
	X843/5	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section								
Maximum Duty Cycle	X842/3	95	97	100	95	97	100	%
	X844/5	46	48	50	46	48	50	%
Minimum Duty Cycle				0			0	%
Total Standby Current								
Start-Up Current			0.5	1		0.5	1	mA
Operating Supply Current	$V_{PIN\ 2} = V_{PIN\ 3}$ = 0V		11	17		11	17	mA
V_{CC} Zener Voltage	I_{CC} = 25mA		34			34		V

Notes: 2. These parameters, although guaranteed, are not 100% tested in production.
3. Parameter measured at trip point of latch with $V_{PIN\ 2} = 0$.
4. Gain defined as:

$$A = \frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}}; 0 \leq V_{PIN\ 3} \leq 0.8V.$$

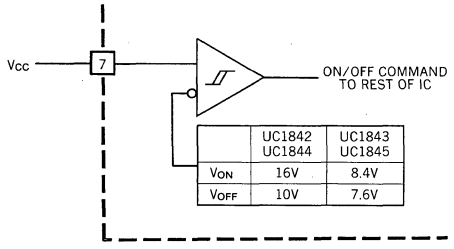
5. Adjust V_{CC} above the start threshold before setting at 15V.
6. Output frequency equals oscillator frequency for the UC1842 and UC1843. Output frequency is one half oscillator frequency for the UC1844 and UC1845.

ERROR AMP CONFIGURATION

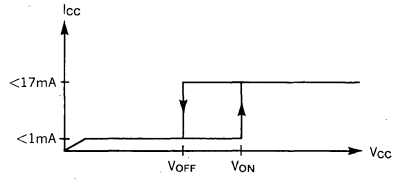


ERROR AMP CAN SOURCE OR SINK UP TO 0.5mA

UNDER-VOLTAGE LOCKOUT

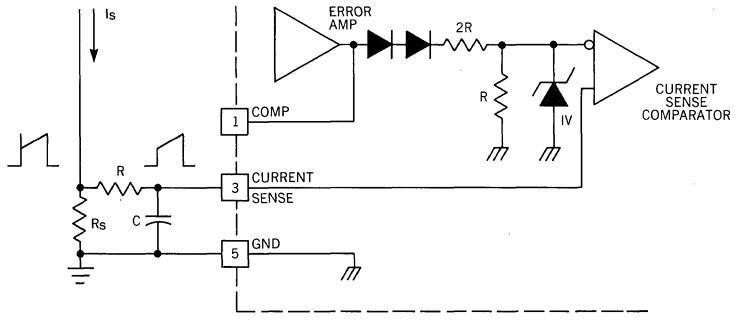


	UC1842 UC1844	UC1843 UC1845
V_{ON}	16V	8.4V
V_{OFF}	10V	7.6V



During Under-Voltage Lockout, the output driver is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.

CURRENT SENSE CIRCUIT

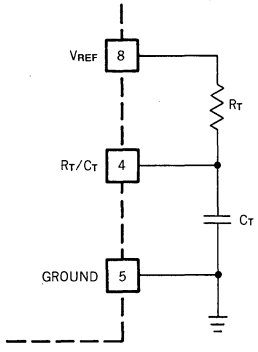


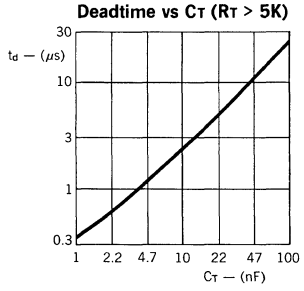
PEAK CURRENT (I_S) IS DETERMINED BY THE FORMULA:

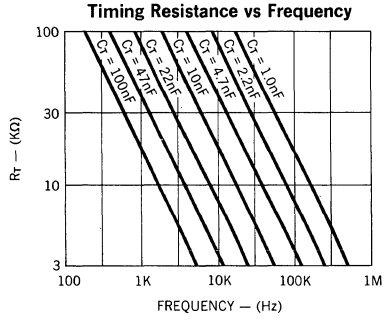
$$I_{smax} \approx \frac{1.0V}{R_S}$$

A SMALL RC FILTER MAY BE REQUIRED TO SUPPRESS SWITCH TRANSIENTS.

OSCILLATOR SECTION

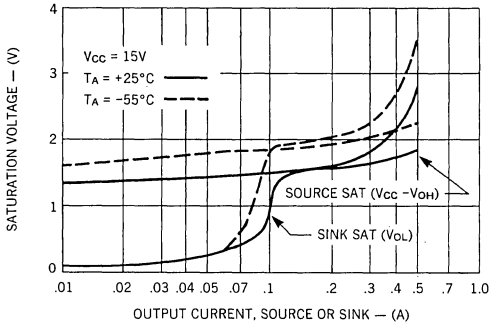




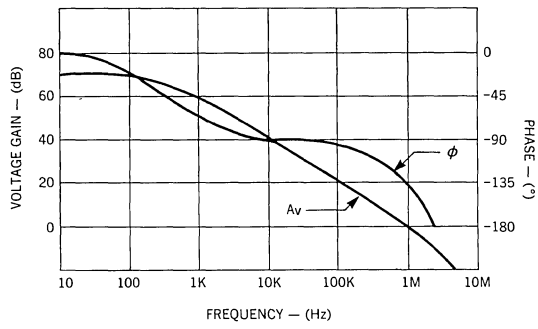


For $R_T > 5K$ $f \approx \frac{1.72}{R_T C_T}$

Output Saturation Characteristics

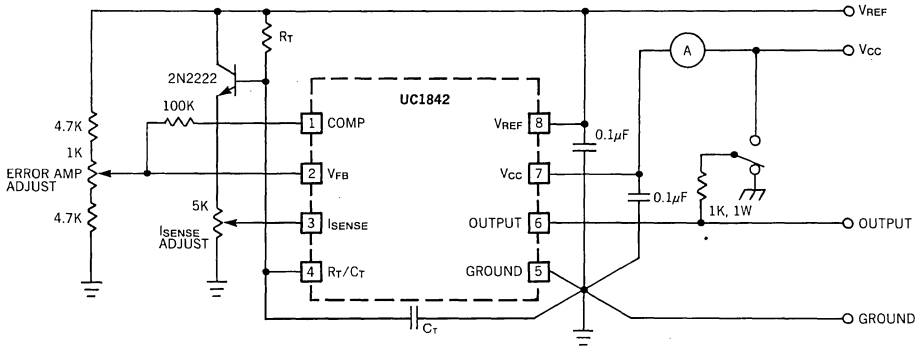


Error Amplifier Open-Loop Frequency Response



3

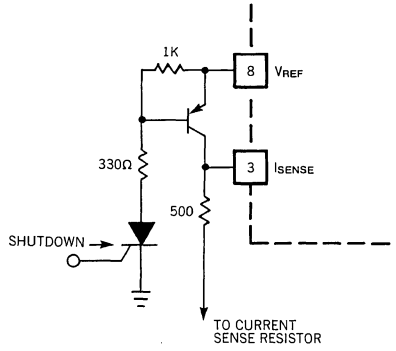
OPEN-LOOP LABORATORY TEST FIXTURE



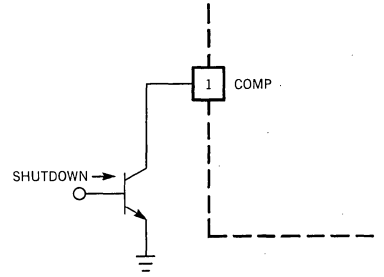
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground.

The transistor and 5K potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

SHUTDOWN TECHNIQUES

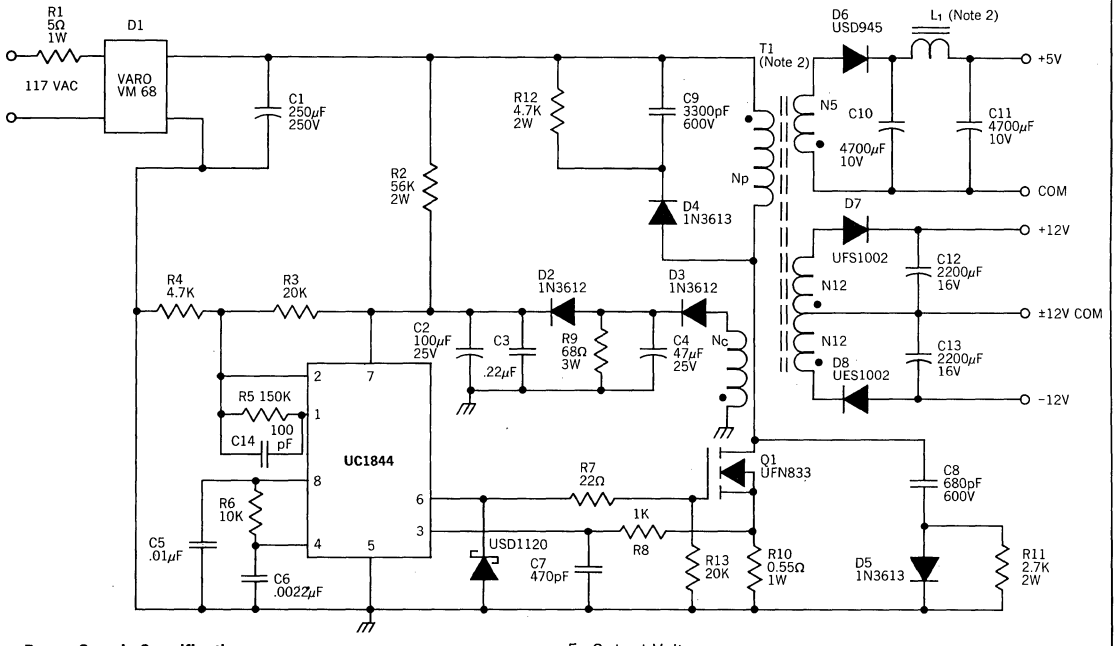


Shutdown of the UC1842 can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below a voltage two diode drops above ground. Either method causes the output of the PWM



comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling Vcc below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

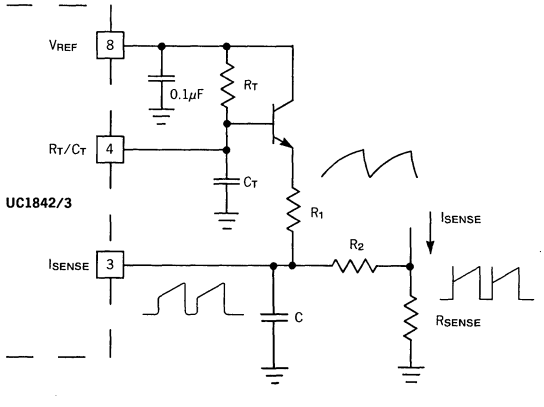
OFFLINE FLYBACK REGULATOR



Power Supply Specifications

1. Input Voltage: 95VAC to 130VAC (50Hz/60Hz)
2. Line Isolation: 3750V
3. Switching Frequency: 40KHz
4. Efficiency @ Full Load: 70%
5. Output Voltage:
   - A. +5V, ±5%: 1A to 4A load
     Ripple voltage: 50mV P-P Max.
   - B. +12V, ±3%: 0.1A to 0.3A load
     Ripple voltage: 100mV P-P Max.
   - C. −12V, ±3%: 0.1A to 0.3A load
     Ripple voltage: 100mV P-P Max.

SLOPE COMPENSATION



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.

Note that capacitor, C, forms a filter with R_2 to suppress the leading edge switch spikes.

LINEAR INTEGRATED CIRCUITS

Current Mode PWM Controller

UC1846 UC1847
UC2846 UC2847
UC3846 UC3847

3

FEATURES

- Automatic feed forward compensation
- Programmable pulse by pulse current limiting
- Automatic symmetry correction in push-pull configuration
- Enhanced load response characteristics
- Parallel operation capability for modular power systems
- Differential current sense amplifier with wide common mode range
- Double pulse suppression
- 200mA totem-pole outputs
- ±1% bandgap reference
- Under-voltage lockout
- Soft start capability
- Shutdown terminal
- 500kHz operation

DESCRIPTION

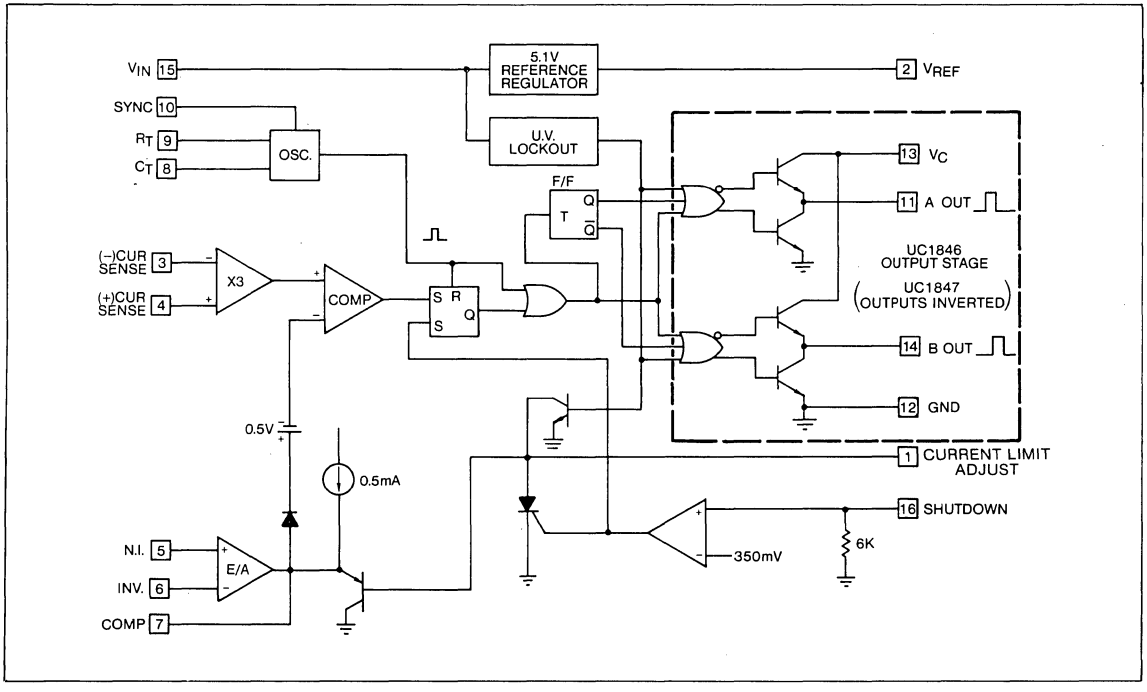
The UC1846/1847 family of control ICs provides all of the necessary features to implement fixed frequency, current mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel "power modules" while maintaining equal current sharing.

Protection circuitry includes built-in under-voltage lockout and programmable current limit in addition to soft start capability. A shutdown function is also available which can initiate either a complete shutdown with automatic restart or latch the supply off.

Other features include fully latched operation, double pulse suppression, deadtime adjust capability, and a ±1% trimmed bandgap reference.

The UC1846 features low outputs in the OFF state, while the UC1847 features high outputs in the OFF state.

BLOCK DIAGRAM



UNITRODE

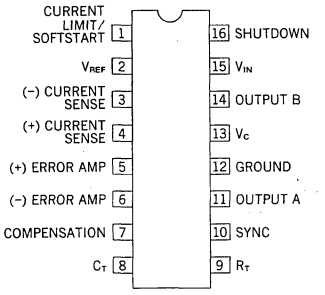
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Pin 15) ..... +40V
Collector Supply Voltage (Pin 13) ..... +40V
Output Current, Source or Sink (Pins 11, 14) 500mA
Analog Inputs (Pins 3, 4, 5, 6, 16) ..... −0.3V to +V_{IN}
Reference Output Current (Pin 2) ..... −30mA
Sync Output Current (Pin 10) ..... −5mA
Error Amplifier Output Current (Pin 7) ..... −5mA
Soft Start Sink Current (Pin 1) 50mA
Oscillator Charging Current (Pin 9) 5mA
Power Dissipation at T_A = 25°C 1000mW
Derate at 10mW/°C for T_A above 50°C
Power Dissipation at T_C = 25°C 2000mW
Derate at 16mW/°C for T_C above 25°C
Thermal Resistance, Junction to Ambient ..... 100°C/W
Thermal Resistance, Junction to Case ..... 60°C/W
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

Note: 1. All voltages are with respect to Ground, Pin 13.
Currents are positive into, negative out of the specified terminal.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for UC1846/UC1847; −25°C to +85°C for the UC2846/UC2847; and 0°C to +70°C for the UC3846/UC3847; V_{IN} =15V, R_T = 10k, C_T = 4.7nF)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_j = 25°C, I_O = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V_{IN} = 8 to 40V		5	20		5	20	mV
Load Regulation	I_L = 1mA to 10mA		3	15		3	15	mV
Temperature Stability	Over Operating Range, (Note 2)		0.4			0.4		mV/°C
Total Output Variation	Line, Load, and Temperature (Note 2)	5.00		5.20	4.95		5.25	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, T_j = 25°C (Note 2)		100			100		μV
Long Term Stability	T_j =125°C, 1000Hrs., (Note 2)		5			5		mV
Short Circuit Output Current	V_{REF} = 0V	−10	−45		−10	−45		mA
Oscillator Section								
Initial Accuracy	T_j = 25°C	39	43	47	39	43	47	kHz
Voltage Stability	V_{IN} = 8 to 40V		−1	2		−1	2	%
Temperature Stability	Over Operating Range (Note 2)		−1			−1		%
Sync Output High Level		3.9	4.35		3.9	4.35		V
Sync Output Low Level			2.3	2.5		2.3	2.5	V
Sync Input High Level	Pin 8 = 0V	3.9			3.9			V
Sync Input Low Level	Pin 8 = 0V			2.5			2.5	V
Sync Input Current	Sync Voltage = 3.9V, Pin 8 = 0V		1.3	1.5		1.3	1.5	mA
Error Amp Section								
Input Offset Voltage			0.5	5		0.5	10	mV
Input Bias Current			−0.6	−1		−0.6	−2	μA
Input Offset Current			40	250		40	250	nA
Common Mode Range	V_{IN} = 8 to 40V	0		V_{IN}−2V	0		V_{IN}−2V	V
Open Loop Voltage Gain	ΔV_O = 1.2 to 3V, V_{CM} = 2V	80	105		80	105		dB
Unity Gain Bandwidth	T_j = 25°C (Note 2)	0.7	1.0		0.7	1.0		MHz
CMRR	V_{CM} = 0 to 38V, V_{IN} = 40V	75	100		75	100		dB
PSRR	V_{IN} = 8 to 40V	80	105		80	105		dB
Output Sink Current	V_{ID} = −15mV to −5V, $V_{Pin\ 7}$ = 1.2V	2	6		2	6		mA
Output Source Current	V_{ID} = 15mV to 5V, $V_{Pin\ 7}$ = 2.5V	−0.4	−0.5		−0.4	−0.5		mA

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for UC1846/UC1847; −25°C to +85°C for the UC2846/UC2847; and 0°C to +70°C for the UC3846/UC3847; V_{IN} =15V, R_T = 10k, C_T = 4.7nF)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Error Amp Section (continued)								
High Level Output Voltage	R_L = (Pin 7) 15kΩ	4.3	4.6		4.3	4.6		V
Low Level Output Voltage	R_L = (Pin 7) 15kΩ		0.7	1		0.7	1	V
Current Sense Amplifier Section								
Amplifier Gain	$V_{Pin\ 3}$ = 0V, Pin 1 Open (Notes 3 & 4)	2.5	2.75	3.0	2.5	2.75	3.0	V
Maximum Differential Input Signal ($V_{Pin\ 4}$-$V_{Pin\ 3}$)	Pin 1 Open (Note 3) R_L (Pin 7) = 15kΩ	1.1	1.2		1.1	1.2		V
Input Offset Voltage	$V_{Pin\ 1}$ = 0.5V Pin 7 Open (Note 3)		5	25		5	25	mV
CMRR	V_{CM} = 1 to 12V	60	83		60	83		dB
PSRR	V_{IN} = 8 to 40V	60	84		60	84		dB
Input Bias Current	$V_{Pin\ 1}$ = 0.5V, Pin 7 Open (Note 3)		−2.5	−10		−2.5	−10	μA
Input Offset Current	$V_{Pin\ 1}$ = 0.5V, Pin 7 Open (Note 3)		0.08	1		0.08	1	μA
Input Common Mode Range		0		V_{IN}−3	0		V_{IN}−3	V
Delay to Outputs	T_j = 25°C, (Note 2)		200	500		200	500	ns
Current Limit Adjust Section								
Current Limit Offset	$V_{Pin\ 3}$ = 0V, $V_{Pin\ 4}$ = 0V, Pin 7 Open (Note 3)	0.45	0.5	0.55	0.45	0.5	0.55	V
Input Bias Current	$V_{Pin\ 5}$ = V_{REF}, $V_{Pin\ 6}$ = 0V		−10	−30		−10	−30	μA
Shutdown Terminal Section								
Threshold Voltage		250	350	400	250	350	400	mV
Input Voltage Range		0		V_{IN}	0		V_{IN}	V
Minimum Latching Current ($I_{Pin\ 1}$)	(Note 6)	3.0	1.5		3.0	1.5		mA
Maximum Non-Latching Current ($I_{Pin\ 1}$)	(Note 7)		1.5	0.8		1.5	0.8	mA
Delay to Outputs	T_j = 25°C (Note 2)		300	600		300	600	ns
Output Section								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	V_C = 40V (Note 5)			200			200	μA
Output Low Level	I_{SINK} = 20mA		0.1	0.4		0.1	0.4	V
	I_{SINK} = 100mA		0.4	2.1		0.4	2.1	
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
	I_{SOURCE} = 100mA	12	13.5		12	13.5		
Rise Time	C_L = 1nF, T_j = 25°C (Note 2)		50	300		50	300	ns
Fall Time	C_L = 1nF, T_j = 25°C (Note 2)		50	300		50	300	ns
Under-Voltage Lockout Section								
Start-Up Threshold			7.7	8.0		7.7	8.0	V
Threshold Hysteresis			0.75			0.75		
Total Standby Current								
Supply Current			17	21		17	21	mA

Notes:
2. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
3. Parameter measured at trip point of latch with $V_{Pin\ 5}$ = V_{REF}, $V_{Pin\ 6}$ = 0V.
4. Amplifier gain defined as:
$$G = \frac{\Delta V_{Pin\ 7}}{\Delta V_{Pin\ 4}}\ ;\ \Delta V_{Pin\ 4} = 0 \text{ to } 1.0V$$
5. Applies to UC1846/UC2846/UC3846 only due to polarity of outputs.
6. Current into Pin 1 guaranteed to latch circuit in shutdown state.
7. Current into Pin 1 guaranteed not to latch circuit in shutdown state.

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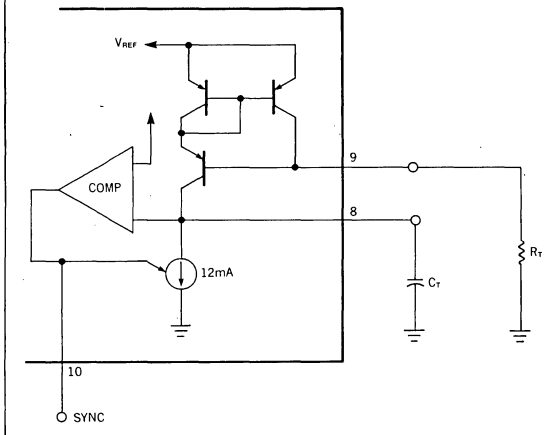
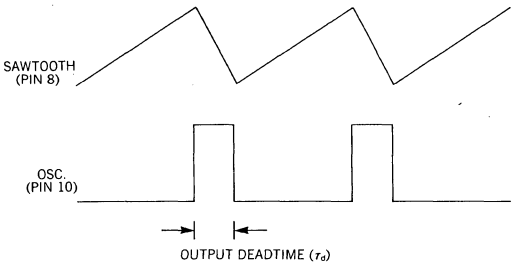
APPLICATIONS DATA

Oscillator Circuit



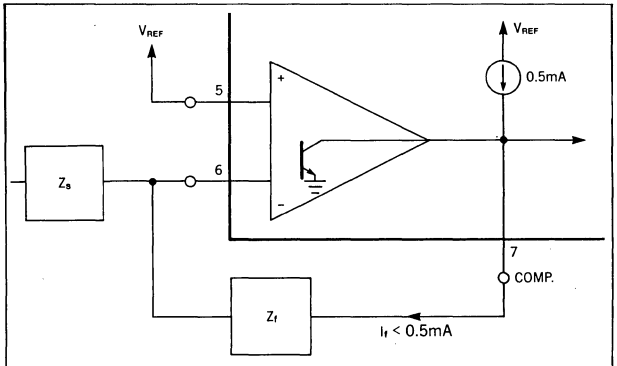


Output deadtime is determined by the external capacitor, C_T, according to the formula: $\tau_d\ (\mu s) = 145 C_T\ (\mu f) \left(\frac{12}{12 - \frac{3.6}{R_T\ (k\Omega)}} \right)$

For large values of R_T: $\tau_d\ (\mu s) \approx 145 C_T\ (\mu f)$

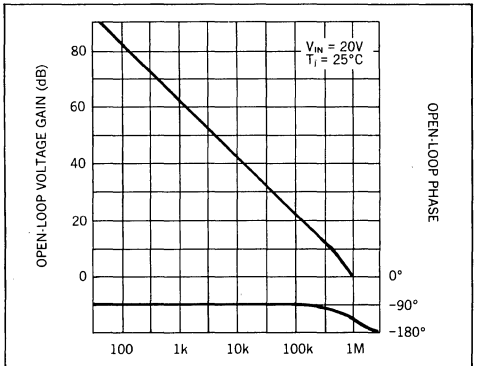
Oscillator frequency is approximated by the formula: $f_T\ (kHz) \approx \frac{2.2}{R_T\ (k\Omega)\ C_T\ (\mu f)}$

Error Amp Output Configuration

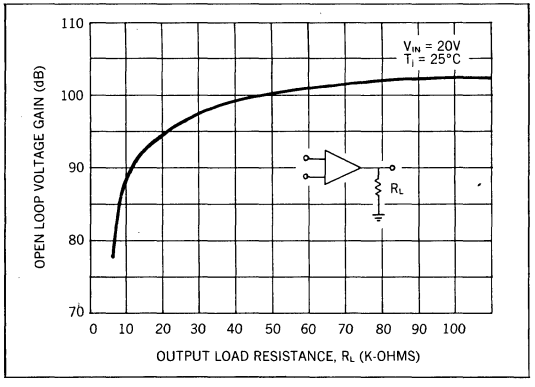


Error Amplifier can source up to 0.5mA.

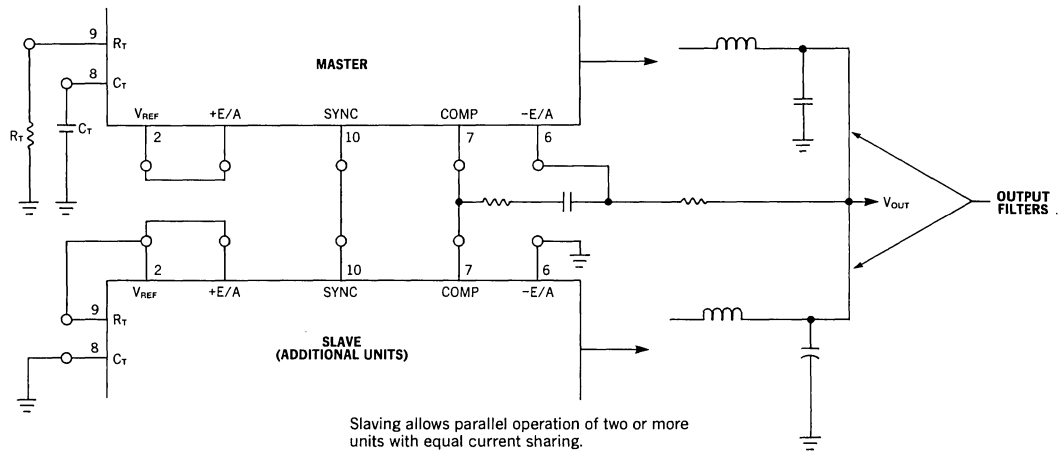
Error Amp Gain and Phase vs Frequency



Error Amp Open-Loop D.C. Gain vs Load Resistance

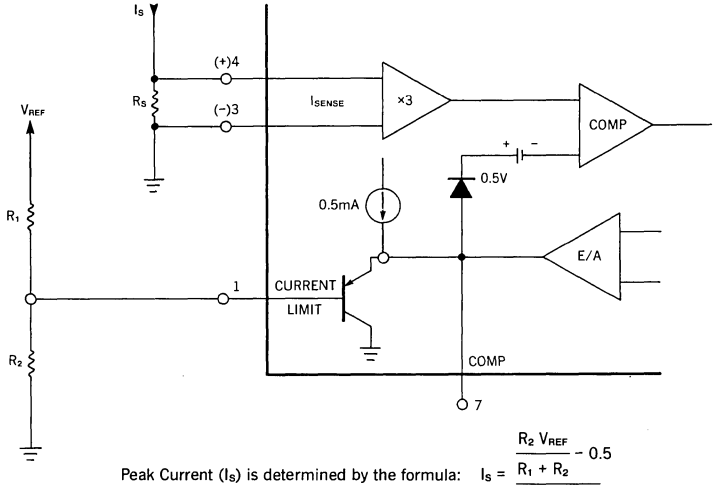


Parallel Operation



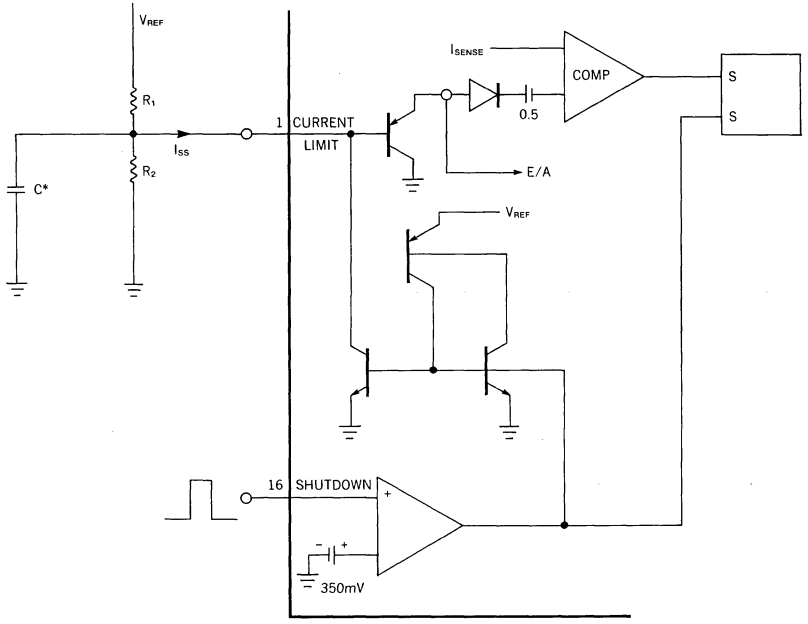
Slaving allows parallel operation of two or more units with equal current sharing.

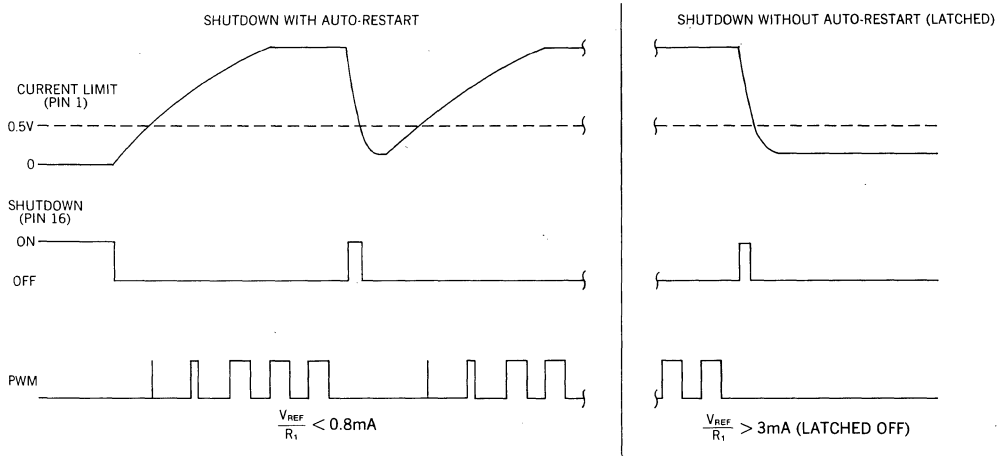
Pulse by Pulse Current Limiting



Peak Current (I_S) is determined by the formula: $I_S = \dfrac{\dfrac{R_2 V_{REF}}{R_1 + R_2} - 0.5}{3R_S}$

Soft Start and Shutdown/Restart Functions

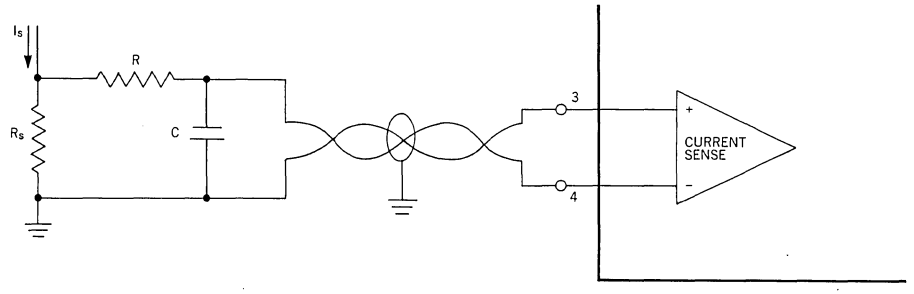




If $\frac{V_{REF}}{R_1} < 0.8mA$, the shutdown latch will commutate when I_{ss} = 0.8mA and a restart cycle will be initiated.

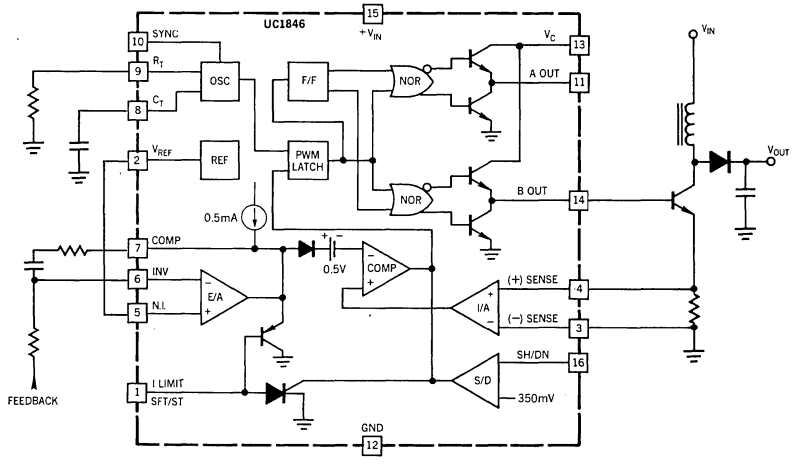
If $\frac{V_{REF}}{R_1} > 3mA$, the device will latch off until power is recycled.

Current Sense Amp Connections

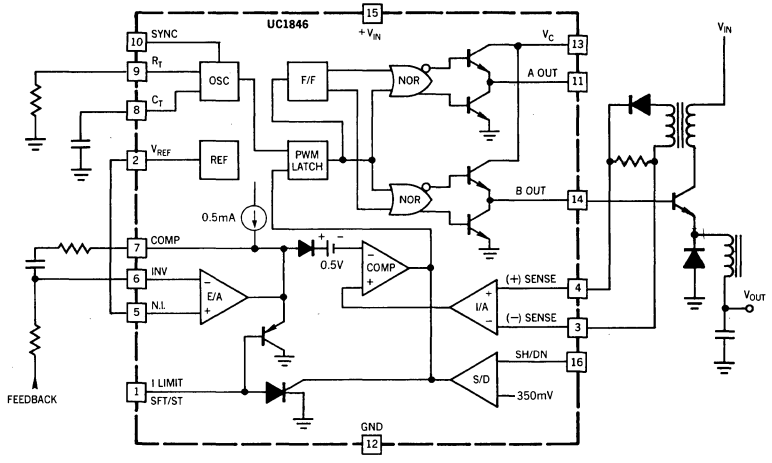


A small RC filter may be required in some applications to reduce switch transients. Differential input allows remote, noise free sensing.

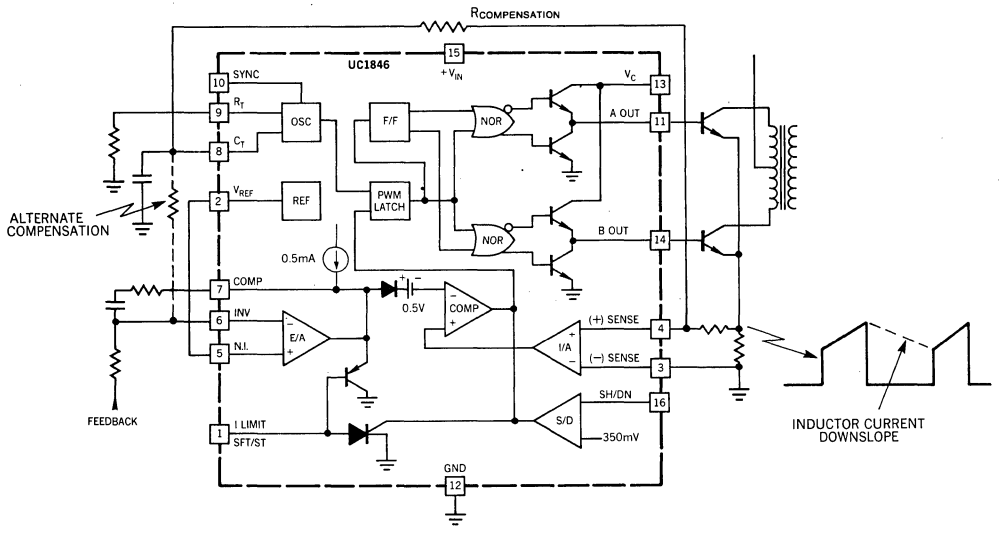
Single Ended Boost Configuration



Buck Converter with Current Sense Winding



Push/Pull Converter with Slope Compensation



Current loop instability above 50% duty cycle can be corrected using slope compensation derived from the sawtooth oscillator. Compensation magnitude should be greater than ½ of the downslope of the inductor current waveform as shown. Alternatively, the compensation signal can be summed into the negative input of the error amplifier.

LINEAR INTEGRATED CIRCUITS

Resonant Mode Power Supply Controller

UC1860
UC2860
UC3860

ADVANCED PRODUCT INFORMATION

3

FEATURES

- Variable Oscillator from 1 kHz to 3 MHz
- 2 MHz Error Amplifier with Controlled Output Swing
- Programmable One Shot Timer—300 ns
- Precision 5V Reference—1%
- Dual Output Stage—2A Peak
- Programmable Under Voltage Lockout
- Programmable Dual or Single Output Mode
- Programmable Restart Delay/Fault Latch
- Uncommitted Open Collector Comparator

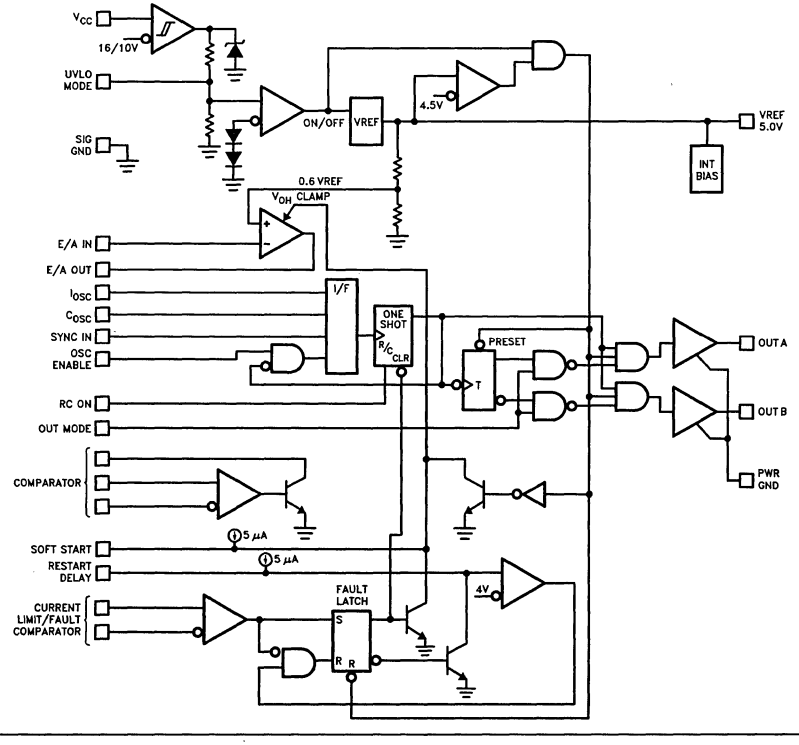
DESCRIPTION

The UC1860 family of control ICs is specifically intended for resonant mode power supply control applications. The control philosophy employed is fixed on-time, variable frequency. The fundamental control blocks include a reference and a wide band, high gain error amplifier which controls a variable frequency oscillator up to 3 MHz. The error amplifier controls oscillator frequency via a resistor into the I_{OSC} pin which is 2 diodes above ground. The error amplifier is clamped so that its output swing is limited from 2 diodes above ground to 2V plus 2 diodes, thus allowing minimum and maximum frequencies to be programmed. A temperature stable one shot timer, triggered by the oscillator, generates pulses as low as 300 ns defining on-time for the output drivers. Each output is capable of driving transient currents up to 2A making them ideal for power MOSFET gates. The mode of the toggle flip-flop is programmable for alternate or unison operation of the outputs.

Additional blocks reside in the chip to facilitate more control capability. An uncommitted open collector comparator can be used to shorten the on-time pulse during start-up or under low load conditions. A fast comparator with a common mode range from −0.3 to +3V is available to sense over current fault conditions. The chip is versatile in fault disposition with several soft start and restart delay options. The restart delay pin can be used to permanently shut the supply down after a fault, restart after a delay, or restart immediately after the fault indication has been removed. A programmable under voltage lockout rounds out the chip. It allows off line operation with a 16V start threshold and 6V of V_{CC} hysteresis or operation directly from a DC supply from 5 to 20V. The UVLO Mode pin can also be used as a port for gating the entire supply on and off. During under voltage lockout, the output stages are actively driven low, and supply current is kept to a minimum.

BLOCK DIAGRAM

UC 1860



UNITRODE

LINEAR INTEGRATED CIRCUITS
Isolated Feedback Generator

UC1901
UC2901
UC3901

FEATURES
- An amplitude-modulation system for transformer coupling an isolated feedback error signal
- Low-cost alternative to optical couplers
- Internal 1% reference and error amplifier
- Internal carrier oscillator usable to 5MHz
- Modulator synchronizable to an external clock
- Loop status monitor

DESCRIPTION
The UC1901 family is designed to solve many of the problems associated with closing a feedback control loop across a voltage isolation boundary. As a stable and reliable alternative to an optical coupler, these devices feature an amplitude modulation system which allows a loop error signal to be coupled with a small RF transformer or capacitor.

The programmable, high-frequency oscillator within the UC1901 series permits the use of smaller, less expensive transformers which can readily be built to meet the isolation requirements of today's line-operated power systems. As an alternative to RF operation, the external clock input to these devices allows synchronization to a system clock or to the switching frequency of a SMPS.

An additional feature is a status monitoring circuit which provides an active-low output when the sensed error voltage is within ±10% of the reference.

Since these devices can also be used as a DC driver for optical couplers, the benefits of 4.5 to 40V supply operation, a 1% accurate reference, and a high gain general purpose amplifier offer advantages even though an AC system may not be desired.

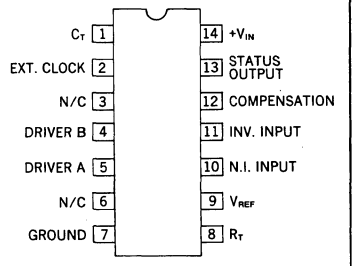
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage, V_{IN}	40V
Reference Output Current	-10mA
Driver Output Currents	-35mA
Status Indicator Voltage	40V
Status Indicator Current	20mA
Ext. Clock Input	40V
Error Amplifier Inputs	-0.5V to +35V
Power Dissipation at T_A = 25°C	
Derate at 10mW/°C above T_A = 50°C	1000mW
Power Dissipation at T_C = 25°C	
Derate at 16mW/°C above T_A = 25°C	2000mW
Thermal Resistance, Junction to Ambient	100°C/W
Thermal Resistance, Junction to Case	60°C/W
Operating Junction Temperature	-55°C to +150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

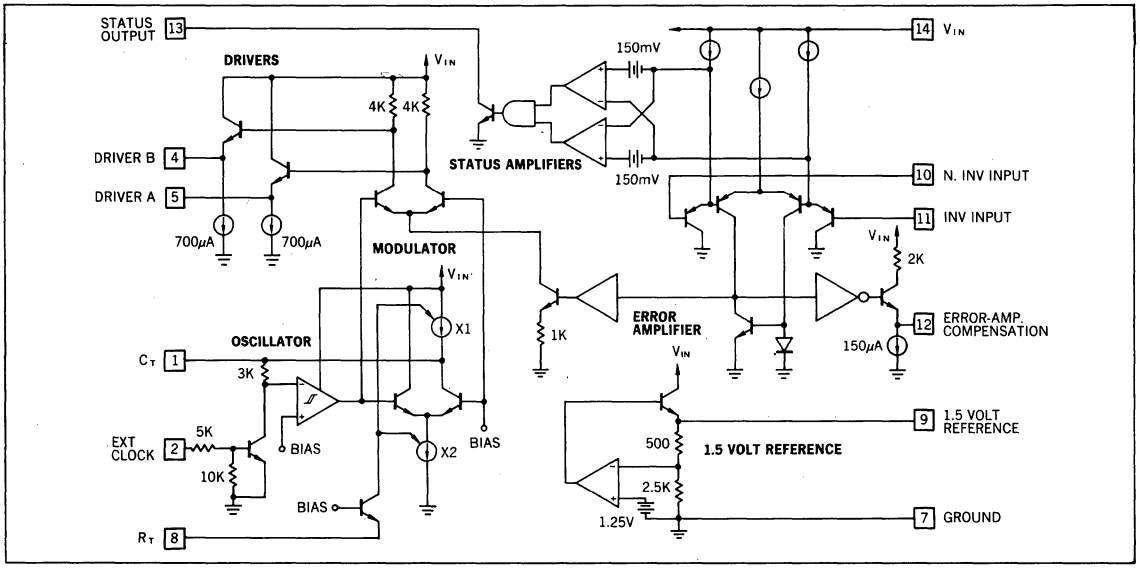
Note 1: Voltages are referenced to ground, Pin 7.
Currents are positive into, negative out of the specified terminal.

CONNECTION DIAGRAM

DIL-14 (TOP VIEW)
J or N PACKAGE



UC1901 SIMPLIFIED SCHEMATIC



UNITRODE

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1901; −25°C to +85°C for the UC2901; and 0°C to +70°C for the UC3901; V_{IN} = 10V, R_T = 10kΩ, C_T = 820pF)

PARAMETER	TEST CONDITIONS	UC1901/UC2901			UC3901			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_j = 25°C	1.485	1.5	1.515	1.47	1.5	1.53	V
	$T_{MIN} \leq T_j \leq T_{MAX}$	1.470	1.5	1.530	1.455	1.5	1.545	
Line Regulation	V_{IN} = 4.5 to 35V		2	10		2	15	mV
Load Regulation	I_{OUT} = 0 to 5mA		4	10		4	15	mV
Short Circuit Current	T_j = 25°C		−35	−55		−35	−55	mA
Error Amplifier Section (To Compensation Terminal)								
Input Offset Voltage	V_{CM} = 1.5V		1	4		1	8	mV
Input Bias Current	V_{CM} = 1.5V		−1	−3		−1	−6	μA
Input Offset Current	V_{CM} = 1.5V		0.1	1		0.1	2	μA
Small Signal Open Loop Gain		40	60		40	60		dB
CMRR	V_{CM} = 0.5 to 7.5V	60	80		60	80		dB
PSRR	V_{IN} = 5 to 25V	80	100		80	100		dB
Output Swing, Δ V_O		0.4	0.7		0.4	0.7		V
Maximum Sink Current		90	150		90	150		μA
Maximum Source Current		−2	−3		−2	−3		mA
Gain Band Width Product			1			1		MHz
Slew Rate			0.3			0.3		V/μs
Modulator/Drivers Section (From Compensation Terminal)								
Voltage Gain		11	12	13	10	12	14	dB
Output Swing		±1.6	±2.8		±1.6	±2.8		V
Driver Sink Current		500	700		500	700		μA
Driver Source Current		−15	−35		−15	−35		mA
Gain Band Width Product			25			25		MHz
Oscillator Section								
Initial Accuracy	T_j = 25°C	140	150	160	130	150	170	kHz
	$T_{MIN} \leq T_j \leq T_{MAX}$	130		170	120		180	kHz
Line Sensitivity	V_{IN} = 5 to 35V		.15	.35		.15	.60	%/V
Maximum Frequency	R_T = 10K, C_T = 10pF		5			5		MHz
Ext. Clock Low Threshold	Pin 1 (C_T) = V_{IN}	0.5			0.5			V
Ext. Clock High Threshold	Pin 1 (C_T) = V_{IN}			1.6			1.6	V
Status Indicator Section								
Input Voltage Window	@ E/A Inputs, V_{CM} = 1.5V	±135	±150	±165	±130	±150	±170	mV
Saturation Voltage	E/A Δ Input = 0V, I_{SINK} = 1.6mA			0.45			0.45	V
Max. Output Current	Pin 13 = 3V, E/A Δ Input = 0.0V	8	15		8	15		mA
Leakage Current	Pin 13 = 40V, E/A Δ Input = 0.2V		.05	1		.05	5	μA
Supply Current	V_{IN} = 35V		5	8		5	10	mA

UNITRODE INTEGRATED CIRCUITS
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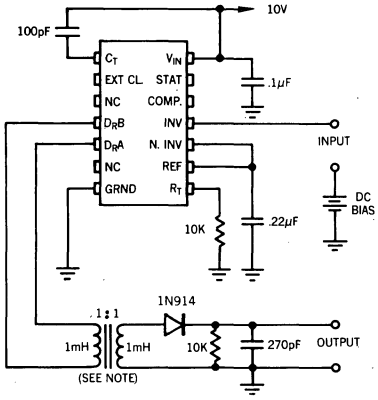
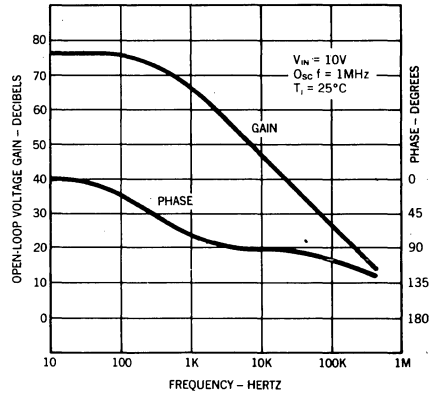
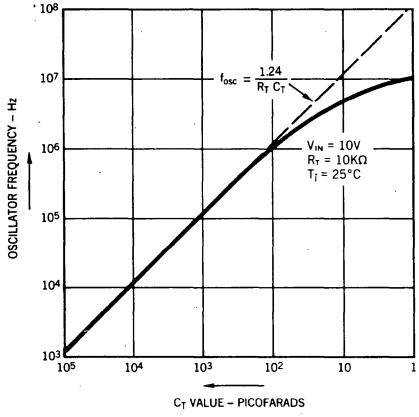
Transformer Coupled Open Loop Transfer Function



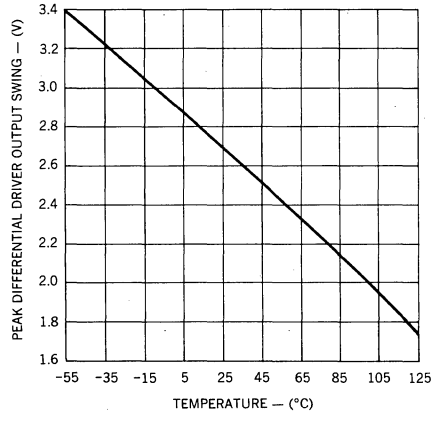


Transformer Data: N1 = N2 = 20T AWG 26
Core = Ferroxcube 3E2A Ferrite, 0.5" O.D. toroid
Carrier Frequency = 1MHz

Oscillator Frequency



Typical Driver Output Swing vs Temperature



APPLICATION INFORMATION

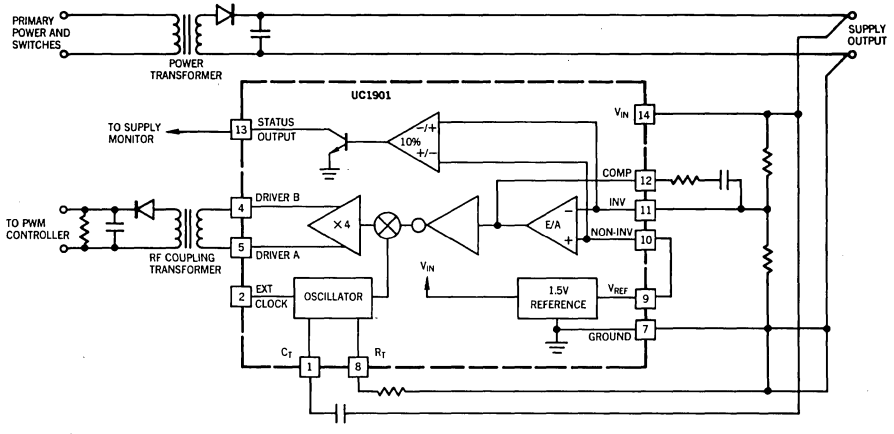
The error amplifier compensation terminal, Pin 12, is intended as a source of feedback to the amplifier's inverting input at Pin 11. For most applications, a series DC blocking capacitor should be part of the feedback network. The amplifier is internally compensated for unity feedback.

The waveform at the driver outputs is a squarewave with an amplitude that is proportional to the error amplifier input signal. There is a fixed 12dB of gain from the error amplifier compensation pin to the modulator driver outputs. The frequency of the output waveform is controlled by either the internal oscillator or an external clock signal. With the internal oscillator the squarewave will have a fixed 50% duty cycle. If the internal oscillator is disabled by connecting Pin 1, C_T, to V_{IN} then the frequency and duty cycle of the output will be determined by the input clock waveform at Pin 2. If the oscillator remains disabled and there is no clock input at Pin 2, there will be a linear 12dB of signal gain to one or the other of the driver outputs depending on the DC state of Pin 2.

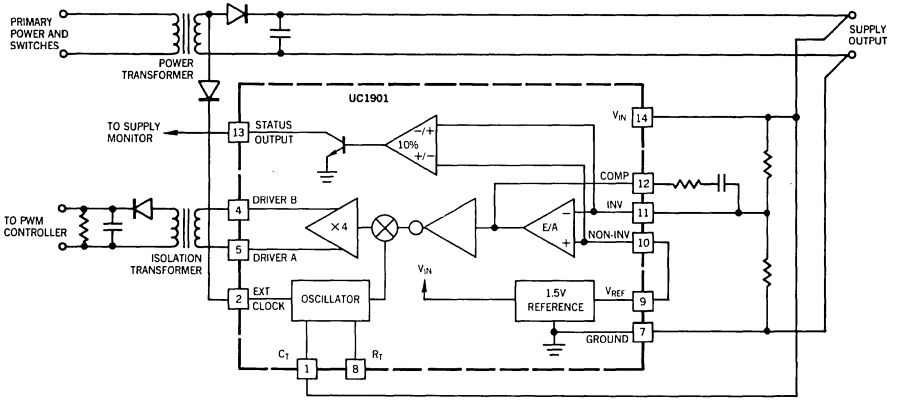
The driver outputs are emitter followers which will source a minimum of 15mA of current. The sink current, internally limited at 700μA, can be increased by adding resistors to ground at the driver outputs.

TYPICAL APPLICATIONS

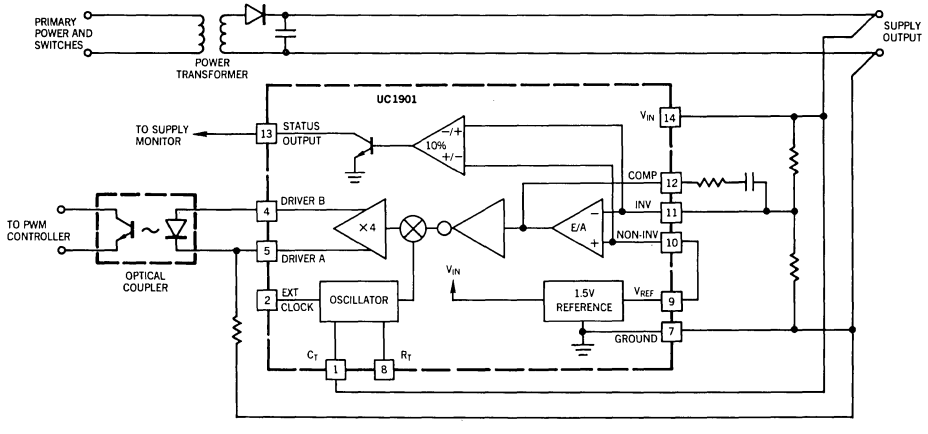
R.F. Transformer Coupled Feedback



Feedback Coupled at Switching Frequency



Optically Coupled DC Feedback



LINEAR INTEGRATED CIRCUITS

Quad Supply and Line Monitor

UC1903
UC2903
UC3903

FEATURES

- Inputs for monitoring up to four separate supply voltage levels
- Internal inverter for sensing a negative supply voltage
- Line/switcher sense input for early power source failure warning
- Programmable under- and over-voltage fault thresholds with proportional hysteresis
- A precision 2.5V reference
- General purpose op-amp for auxillary use
- Three high current, >30mA, open-collector outputs indicate over-voltage, under-voltage and power OK conditions
- Input supply under-voltage sensing and start-latch eliminate erroneous fault alerts during start-up
- 8-40V supply operation with 7mA stand-by current

DESCRIPTION

The UC1903 family of quad supply and line monitor integrated circuits will respond to under- and over-voltage conditions on up to four continuously monitored voltage levels. An internal op-amp inverter allows at least one of these levels to be negative. A separate line/switcher sense input is available to provide early warning of line or other power source failures.

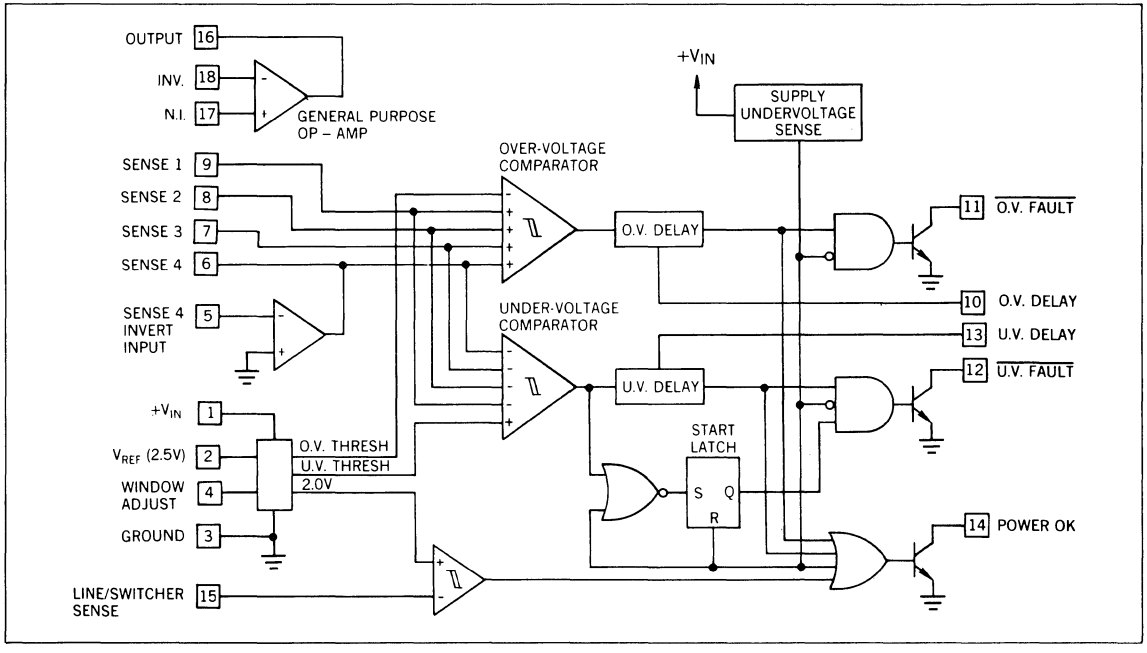
The fault window adjustment circuit on these devices provides easy programming of under- and over-voltage thresholds. The thresholds, centered around a precision 2.5V reference, have an input hysteresis that scales with the window width for precise, glitch-free operation. A reference output pin allows the sense input fault windows to be scaled independently using simple resistive dividers.

The three open collector outputs on these devices will sink in excess of 30mA of load current when active. The under- and over-voltage outputs respond after separate, user defined, delays to respective fault conditions. The third output is active during any fault condition including under- and over-voltage, line/switcher faults, and input supply under-voltage. The off state of this output indicates a "power OK" situation.

An additional, uncommitted, general purpose op-amp is also included. This op-amp, capable of sourcing 20mA of output current, can be used for a number of auxiliary functions including the sensing and amplification of a feedback error signal when the 2.5V output is used as a system reference.

In addition, these ICs are equipped with a start-latch to prevent erroneous under-voltage indications during start-up. These parts operate over an 8-40V input supply range and require a typical stand-by current of only 6mA.

BLOCK DIAGRAM



UNITRODE

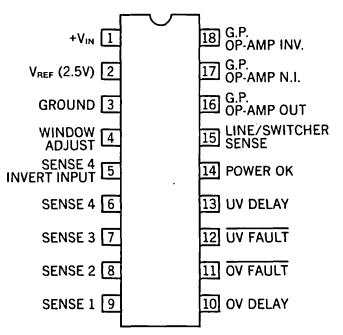
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ($+V_{IN}$) ..... +40V
Open Collector Output Voltages ..... +40V
Open Collector Output Currents 50mA
Sense 1-4 Input Voltages ..... -0.3V to +20V
Line/Switcher Sense Input Voltage ..... -0.3V to +40V
Op-Amp and Inverter Input Voltages ..... -0.3V to +40V
Op-Amp and Inverter Output Currents ..... -40mA
Window Adjust Voltage ..... 0.0V to +10V
Delay Pin Voltages ..... 0.0V to +5V
Reference Output Current ..... -40mA
Power Dissipation at T_A = 25°C 1000mW
  Derate at 10mW/°C above T_A = 25°C
Power Dissipation at T_C = 25°C 2000mW
  Derate at 16mW/°C above T_C = 25°C
Thermal Resistance, Junction to Ambient ..... 100°C/W
Thermal Resistance, Junction to Case ..... 60°C/W
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note: 1. Voltages are referenced to ground (Pin 3). Currents are positive into, negative out of, the specified terminals.

CONNECTION DIAGRAM

DIL-18 (Top View)
J or N Package



3

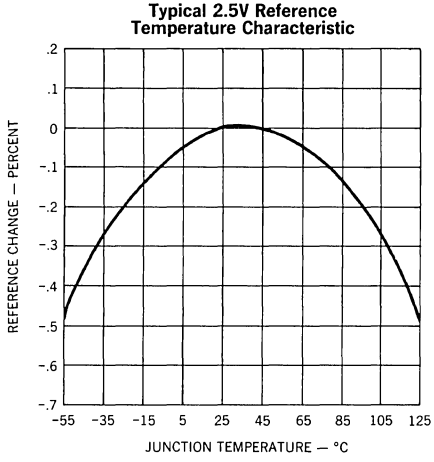
ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1903; -25°C to +85°C for the UC2903; and 0°C to +70°C for the UC3903; $+V_{IN}$ = 15V; Sense Inputs (Pins 6-9 and Pin 15) = 2.5V; $V_{PIN\ 4}$ = 1.0V.)

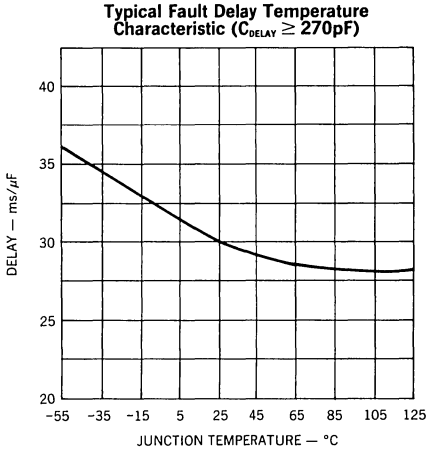
PARAMETER	TEST CONDITIONS	UC1903/UC2903			UC3903			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply								
Input Supply Current	No Faults	—	7	9	—	7	11	mA
	UV, OV and Line Fault	—	10	15	—	10	18	mA
Supply Under Voltage Threshold (V_{SUV})	Fault Outputs Enabled	6.0	7.0	7.5	5.5	7.0	8.0	V
Minimum Supply to Enable Power OK Output		—	3.0	4.0	—	3.0	4.0	V
Reference								
Output Voltage (V_{REF})	T_j = 25°C	2.485	2.5	2.515	2.470	2.5	2.530	V
	Over Temperature	2.465	—	2.535	2.465	—	2.535	V
Load Regulation	I_L = 0 to 10mA	—	1	10	—	1	15	mV
Line Regulation	$+V_{IN}$ = 8 to 40V	—	1	4	—	1	8	mV
Short Circuit Current	T_j = 25°C	—	40	—	—	40	—	mA
Fault Thresholds								
OV Threshold Adj.	Offset from V_{REF} as a function of V_{PIN4} Input = Low to High, .5V ≤ $V_{PIN\ 4}$ ≤ 2.5V	.230	.25	.270	.230	.25	.270	V/V
UV Threshold Adj.	Offset from V_{REF} as a function of V_{PIN4} Input = High to Low, .5V ≤ $V_{PIN\ 4}$ ≤ 2.5V	-.270	-.25	-.230	-.270	-.25	-.230	V/V
OV & UV Threshold Hyst.	.5V ≤ $V_{PIN\ 4}$ ≤ 2.5V	10	20	30	10	20	30	mV/V
OV & UV Threshold Supply Sensitivity	$+V_{IN}$ = V_{SUV} +0.1V to 40V	—	.002	.01	—	.002	.02	%/V
Adjust Pin (Pin 4) Input Bias Current	.5V ≤ $V_{PIN\ 4}$ ≤ 2.5V	—	±1	±10	—	±1	±12	μA/V
Line Sense Threshold	Input = High to Low	1.94	2.0	2.06	1.9	2.0	2.1	V
Line Sense Threshold Hyst.		125	175	225	100	175	250	mV

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1903; −25°C to +85°C for the UC2903; and 0°C to +70°C for the UC3903; $+V_{IN}$ = 15V; Sense Inputs (Pins 6-9 and Pin 15) = 2.5V; $V_{PIN\ 4}$ = 1.0V.)

PARAMETER	TEST CONDITIONS	UC1903/UC2903			UC3903			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Sense Inputs								
Sense 1-4 Input Bias Current	Input = 2.8V (Note 2)	—	1	3	—	1	6	μA
	Input = 2.2V (Note 2)	—	-1	-3	—	-1	-6	μA
Line Sense Input Bias Current	Input = 2.3V (Note 2)	—	1	3	—	1	6	μA
OV and UV Fault Delay								
Charging Current		—	60	—	—	60	—	μA
Threshold Voltage	Delay Pin = Low to High	—	1.8	—	—	1.8	—	V
Threshold Hysteresis	T_j = 25°C	—	250	—	—	250	—	mV
Delay	Ratio of Threshold Voltage to Charging Current	20	30	50	20	30	50	ms/μF
Fault Outputs ($\overline{OV}$, $\overline{UV}$, & Power OK)								
Maximum Current	V_{OUT} = 2V	30	70	—	30	70	—	mA
Saturation Voltage	I_{OUT} = 12mA	—	.25	.40	—	.25	.40	V
Leakage Current	V_{OUT} = 40V	—	3	25	—	3	25	μA
Sense 4 Inverter								
Input Offset Voltage		—	2	8	—	2	10	mV
Input Bias Current		—	.1	2	—	.1	4	μA
Open Loop Gain		65	80	—	65	80	—	dB
PSRR	$+V_{IN}$ = 8 to 40V	65	100	—	65	100	—	dB
Unity Gain Frequency		—	1	—	—	1	—	MHz
Slew Rate		—	.4	—	—	.4	—	V/μs
Short Circuit Current	T_j = 25°C	—	40	—	—	40	—	mA
G.P. Op-Amp								
Input Offset Voltage		—	1	5	—	1	8	mV
Input Bias Current		—	.1	2	—	.1	4	μA
Input Offset Current		—	.01	.5	—	.01	1.0	μA
Open Loop Gain		65	120	—	65	120	—	dB
CMRR	V_{CM} = 0 to $+V_{IN}$ −2.0V	65	100	—	65	100	—	dB
PSRR	$+V_{IN}$ = 8 to 40V	65	100	—	65	100	—	dB
Unity Gain Frequency		—	1	—	—	1	—	MHz
Slew Rate		—	.4	—	—	.4	—	V/μs
Short Circuit Current	T_j = 25°C	—	40	—	—	40	—	mA

Note: 2. These currents represent maximum input bias currents required as the sense inputs cross appropriate thresholds.





3

OPERATION AND APPLICATION INFORMATION

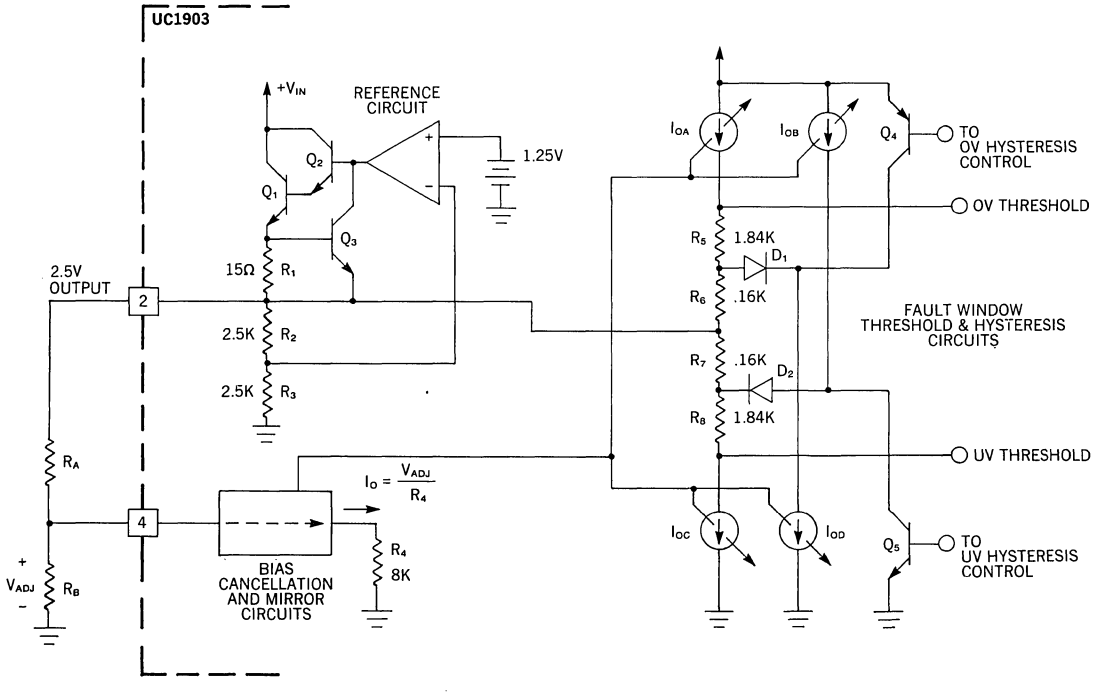


Figure 1. The UC1903 fault window circuitry generates OV and UV thresholds centered around the 2.5V reference. Window magnitude and threshold hysteresis are proportional to the window adjust input voltage at Pin 4.

OPERATION AND APPLICATION INFORMATION (continued)

Setting a Fault Window

The fault thresholds on the UC1903 are generated by creating positive and negative offsets, equal in magnitude, that are referenced to the chip's 2.5V reference. The resulting fault window is centered around 2.5V and has a magnitude equal to that of the applied offsets. Simplified schematics of the fault window and reference circuits are shown in Figure 1 (see previous page). The magnitude of the offsets is determined by the voltage applied at the window adjust pin, Pin 4. A bias cancellation circuit keeps the input current required at Pin 4 low, allowing the use of a simple resistive divider off the reference to set the adjust pin voltage.

The adjust voltage at Pin 4 is internally applied across R_4, an 8K resistor. The resulting current is mirrored four times to generate current sources I_{OA}, I_{OB}, I_{OC}, and I_{OD}, all equal in magnitude. When all four of the sense inputs are inside the fault window, a no-fault condition, Q_4 and Q_5 are turned on. In combination with D_1 and D_2 this prevents I_{OB} and I_{OD} from affecting the fault thresholds. In this case, the OV and UV thresholds are equal to $V_{REF} + I_{OA}(R_5 + R_6)$ and $V_{REF} - I_{OC}(R_7 + R_8)$ respectively. The fault window can be expressed as:

(1) $$2.5V \pm \frac{V_{ADJ}}{4}$$

In terms of a sensed nominal voltage level, V_S, the window as a percent variation is:

(2) $$V_S \pm (10 \cdot V_{ADJ})\%$$

When a sense input moves outside the fault window given in equation (1), the appropriate hysteresis control signal turns off Q_4 or Q_5. For the under-voltage case, Q_5 is disabled and current source I_{OB} flows through D_2. The net current through R_7 becomes zero as I_{OB} cancels I_{OC}, giving an 8% reduction in the UV threshold offset. The over-voltage case is the same, with Q_4 turning off, allowing I_{OD} to cancel the current flow, I_{OA}, through R_6. The result is a hysteresis at the sense inputs which is always 8% of the window magnitude. This is shown graphically in Figure 2.

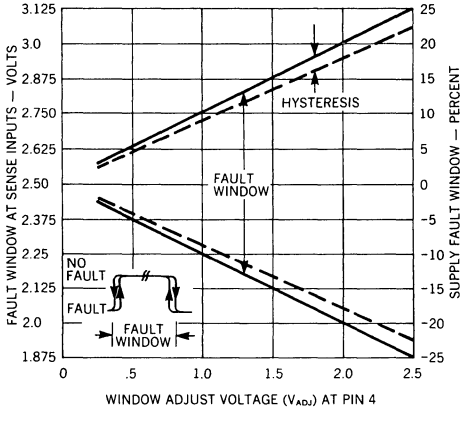


Figure 2. The fault window and threshold hysteresis scale as a function of the voltage applied at Pin 4, the window adjust pin.

Fault Windows Can be Scaled Independently

In many applications, it may be desirable to monitor various supply voltages, or voltage levels, with varying fault windows. Using the reference output and external resistive dividers this is easily accomplished with the UC1903. Figures 3 and 4 illustrate how the fault window at any sense input can be scaled independently of the remaining inputs.

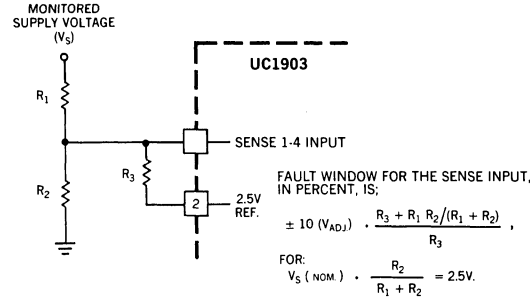


Figure 3. Using the reference output and a resistive divider, a sense input with an independently wider fault window can be generated.

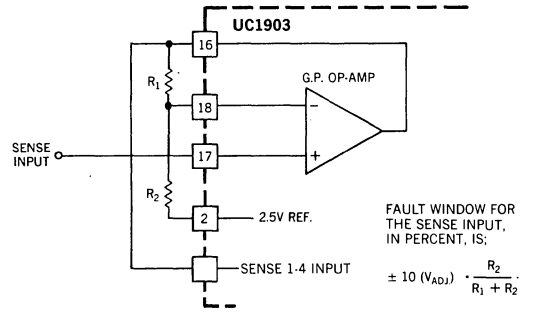


Figure 4. The general purpose op-amp on the UC1903 can be used to create a sense input with an independently tighter fault window.

Figure 4 demonstrates one of many auxillary functions that the uncommitted op-amp on the UC1903 can be used for. Alternatively, this op-amp can be used to buffer high impedence points, perform logic functions, or for sensing and amplification. For example, the G.P. op-amp, combined with the 2.5V reference, can be used to produce and buffer an optically coupled feedback signal in isolated supplies with primary side control. The output stage of this op-amp is detailed in Figure 5. The NPN emitter follower provides high source current capability, ≥20mA, while the substrate device, Q_3, provides good transient sinking capability.

OPERATION AND APPLICATION INFORMATION (continued)

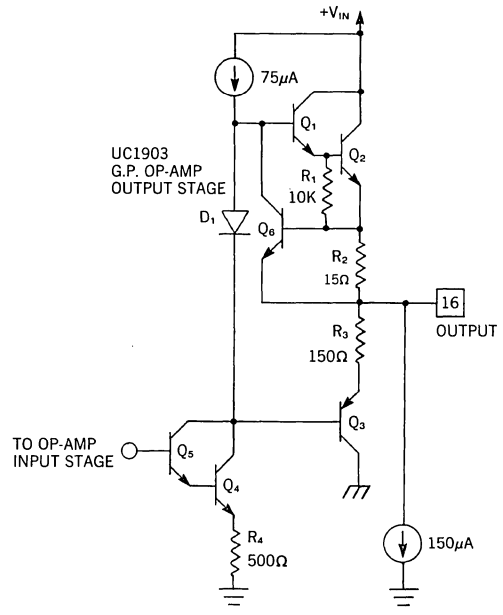


Figure 5. The G.P. op-amp on the UC1903 has a high source current (≥20mA) capability and enhanced transient sinking capability through substrate device Q_3.

Sensing a Negative Voltage Level

The UC1903 has a dedicated inverter coupled to the sense 4 input. With this inverter, a negative voltage level can be sensed as shown in Figure 6. The output of this inverter is an unbiased emitter follower. By tying the inverting input, Pin 5, high the output emitter follower will be reverse biased, leaving the sense 4 input in a high impedence state. In this manner, the sense 4 input can be used, as the remaining sense inputs would be, for sensing positive voltage levels.

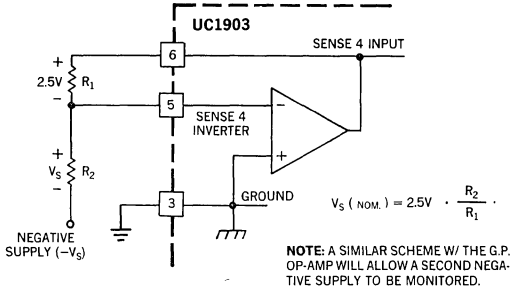


Figure 6. Inverting the sense 4 input for monitoring a negative supply is accommodated with the dedicated inverter.

Using The Line/Switcher Sense Output

The line switcher sense input to the UC1903 can be used for early detection of line, switcher, or other power source, failures. Internally referenced to 2.0V, the line sense comparator will cause the POWER OK output to indicate a fault (active low) condition when the LINE/SWITCHER SENSE input goes from above to below 2.0V. The line sense comparator has approximately 175mV of hysteresis requiring the line/switcher input to reach 2.175V before the POWER OK output device can be turned-off, allowing a no-fault indication. In Figure 7 an example showing the use of the LINE/SWITCHER SENSE input for early switcher-fault detection is detailed. A sample signal is taken from

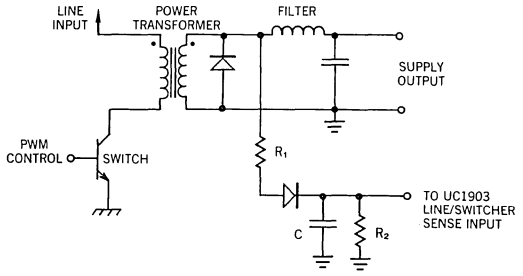


Figure 7. The line/switcher sense input can be used for an early line or switcher fault indication.

the output of the power transformer, rectified and filtered, and used at the line/switcher input. By adjusting the R_2C time constant with respect to the switching frequency of the supply and the hold up time of the output capacitor, switcher faults can be detected before supply outputs are significantly affected.

OV and UV Comparators Maintain Accurate Thresholds

The structure of the $\overline{OV}$ and $\overline{UV}$ comparators, shown in Figure 8 results in accurate fault thresholds even in the case where multiple sense inputs cross a fault threshold simultaneously. Unused sense inputs can be tied either to the 2.5V reference, or to another, utilized, sense input. The four under- and over-voltage sense inputs on the UC1903 are clamped as detailed on the Sense 1 input in Figure 8. The series 2K resistor, R_1, and zener diode, Z_1, prevent extreme under- and over-voltage conditions from inverting the outputs of the fault comparators. A parasitic diode, D_1, is present at the inputs as well. Under normal operation it is advisable to insure that voltage levels at all of the sense inputs stay above −0.3V. The same type of input protection exists at the line sense input, Pin 15, except a 5K series resistor is used.

The fault delay circuitry on the UC1903 is also shown in Figure 8. In the case of an over-voltage condition at one of the sense inputs Q_{20} is turned off, allowing the internal 60μA current source to charge the user-selected delay capacitor. When the capacitor voltage reaches 1.8V, the $\overline{OV}$ and POWER OK outputs become active low. When the fault condition goes away Q_{20} is turned back on, rapidly discharging the delay capacitor. Operation of the under-voltage delay is, with appropriate substitutions, the same.

OPERATION AND APPLICATION INFORMATION (continued)

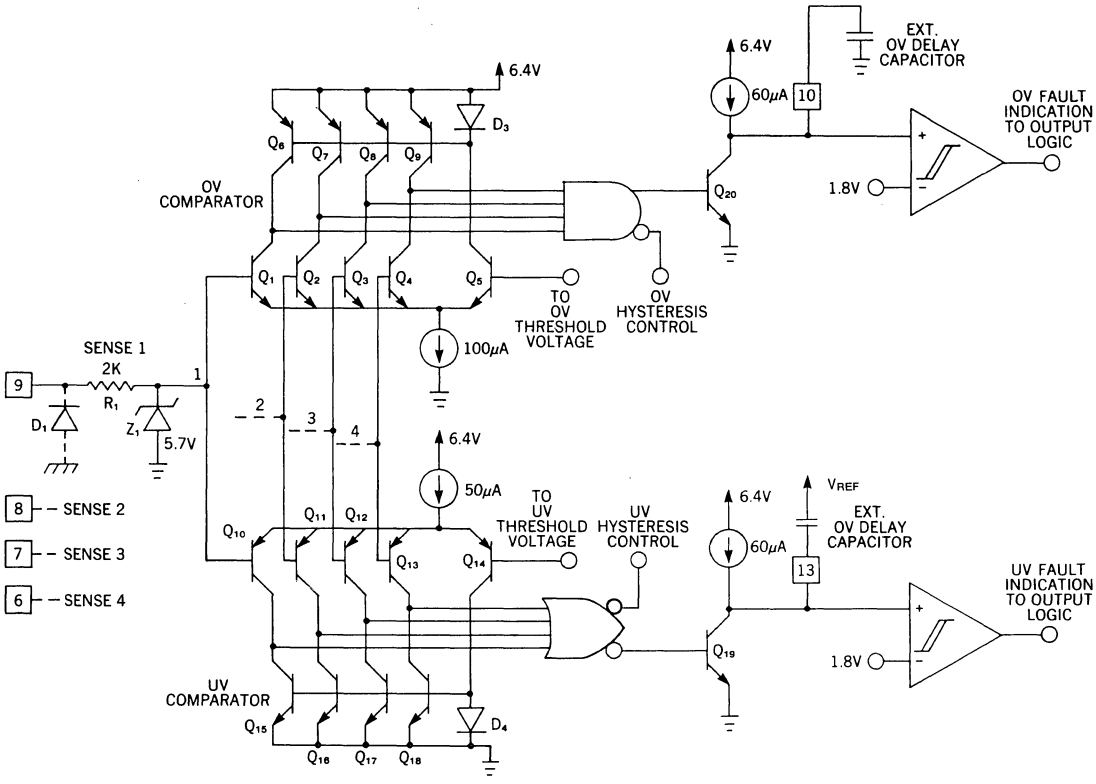


Figure 8. The OV and UV comparators on the UC1903 trigger respective fault delay circuits when one or more of the sense inputs move outside the fault window. Input clamps insure proper operation under extreme fault conditions.

Start Latch and Supply Under-Voltage Sense Allow Predictable Power-Up

The supply under-voltage sense and start-latch circuitry on the UC1903 prevents fault indications during start-up or low input supply ($+V_{IN}$) conditions. When the input supply voltage is below the supply under-voltage threshold the $\overline{OV}$ and $\overline{UV}$ fault outputs are disabled and the POWER OK output is active low. The POWER OK output will remain active until the input supply drops below approximately 3.0V. With $+V_{IN}$ below this level, all of the open collector outputs will be off.

When the input supply is low, the under-voltage sense circuitry resets the start-latch. With the start-latch reset, the UV fault output will remain disabled until the input supply rises to its normal operating level (8-40V), and all of the sense inputs are above the under-voltage threshold. This allows slow starting, or supply sequencing, without an artificial under-voltage fault indication. Once the latch is set, the UV fault output will respond if any of the sense inputs drop below the under-voltage threshold.

LINEAR INTEGRATED CIRCUITS

Sealed Lead-Acid Battery Charger

UC2906
UC3906

3

FEATURES

- Optimum control for maximum battery capacity and life
- Internal state logic provides three charge states
- Precision reference tracks battery requirements over temperature
- Controls both voltage and current at charger output
- System interface functions
- Typical standby supply current of only 1.6mA

DESCRIPTION

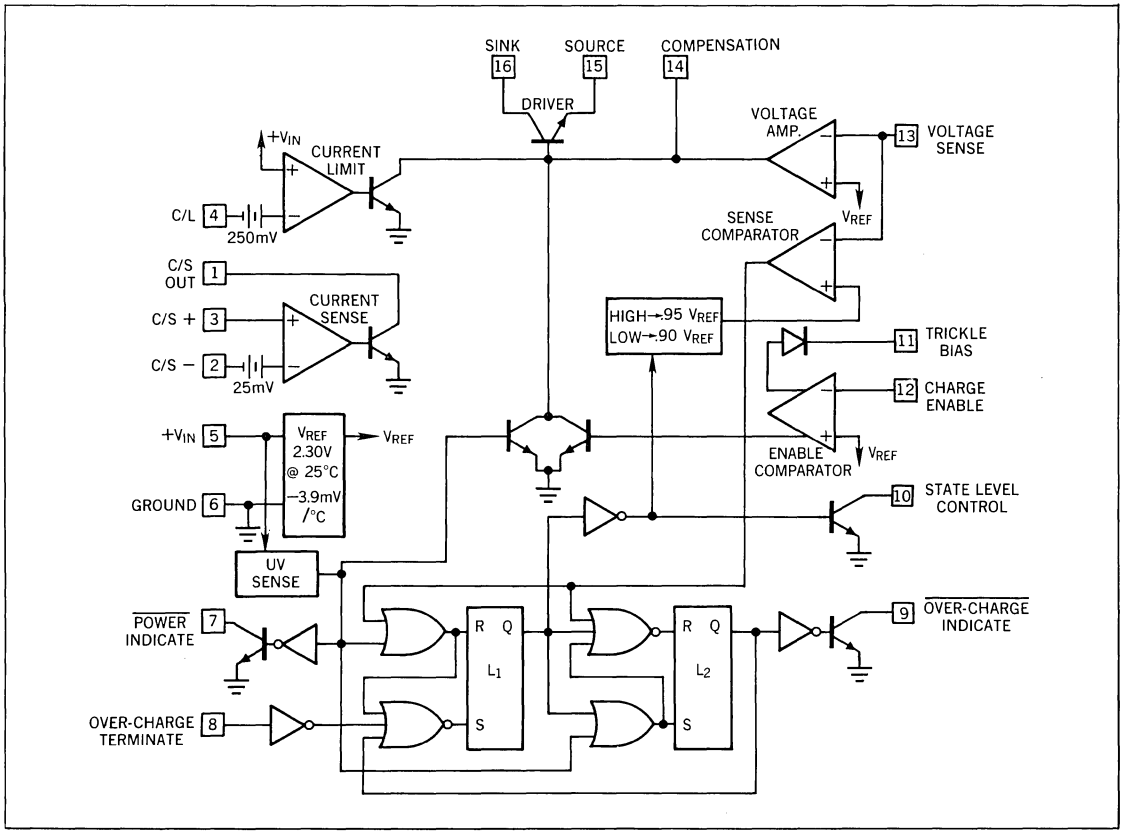
The UC2906 series of battery charger controllers contains all of the necessary circuitry to optimally control the charge and hold cycle for sealed lead-acid batteries. These integrated circuits monitor and control both the output voltage and current of the charger through three separate charge states; a high current bulk-charge state, a controlled over-charge, and a precision float-charge, or standby, state.

Optimum charging conditions are maintained over an extended temperature range with an internal reference that tracks the nominal temperature characteristics of the lead-acid cell. A typical standby supply current requirement of only 1.6mA allows these ICs to predictably monitor ambient temperatures.

Separate voltage loop and current limit amplifiers regulate the output voltage and current levels in the charger by controlling the onboard driver. The driver will supply up to 25mA of base drive to an external pass device. Voltage and current sense comparators are used to sense the battery condition and respond with logic inputs to the charge state logic. A charge enable comparator with a trickle bias output can be used to implement a low current turn-on mode of the charger, preventing high current charging during abnormal conditions such as a shorted battery cell.

Other features include a supply under-voltage sense circuit with a logic output to indicate when input power is present. In addition the over-charge state of the charger can be externally monitored and terminated using the over-charge indicate output and over-charge terminate input.

UC2906 BLOCK DIAGRAM



UNITRODE

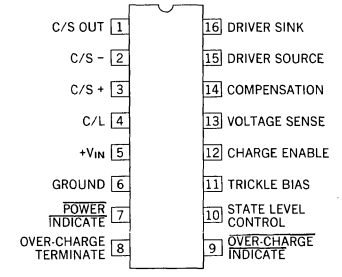
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ($+V_{IN}$) 40V
Open Collector Output Voltages 40V
Amplifier and Comparator Input Voltages ..... -0.3V to +40V
Over-Charge Terminate Input Voltage ..... -0.3V to +40V
Current Sense Amplifier Output Current 40mA
Other Open Collector Output Currents 5mA
Trickle Bias Output Current ..... -40mA
Driver Current 40mA
Power Dissipation at T_A = 25°C
  Derate at 10mW/°C Above T_A = 25°C 1000mW
Power Dissipation at T_C = 25°C
  Derate at 16mW/°C Above T_C = 25°C 2000mW
Thermal Resistance, Junction-to-Ambient ..... 100°C/W
Thermal Resistance, Junction-to-Case ..... 60°C/W
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65° to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note: 1. Voltages are referenced to ground (Pin 6).
Currents are positive into, negative out of, the specified terminals.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = -40°C to +70°C for the UC2906 and 0°C to +70°C for the UC3906, $+V_{IN}$ = 10V.)

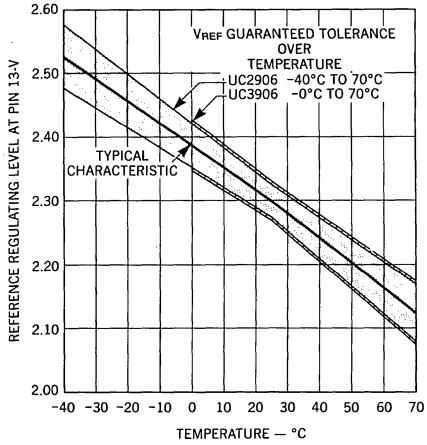
PARAMETER	TEST CONDITIONS	2906			3906			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Supply								
Supply Current	$+V_{IN}$ = 10V		1.6	2.5		1.6	2.5	mA
	$+V_{IN}$ = 40V		1.8	2.7		1.8	2.7	mA
Supply Under-Voltage Threshold	$+V_{IN}$ = Low to High	4.2	4.5	4.8	4.2	4.5	4.8	V
Supply Under-Voltage Hysteresis			.20	.30		.20	.30	V
Internal Reference (V_{REF})								
Voltage Level (Note 2)	Measured as Regulating Level At Pin 13 w/ Driver Current = 1mA, T_j = 25°C	2.275	2.3	2.325	2.270	2.3	2.330	V
Line Regulation	$+V_{IN}$ = 5 to 40V		3	8		3	8	mV
Temperature Coefficient			-3.9			-3.9		mV/°C
Voltage Amplifier								
Input Bias Current	Total Input Bias at Regulating Level	-.5	-.2		-.5	-.2		μA
Maximum Output Current	Source	-45	-30	-15	-45	-30	-15	μA
	Sink	30	60	90	30	60	90	μA
Open Loop Gain	Driver Current = 1mA	50	65		50	65		dB
Output Voltage Swing	Volts Above GND or Below $+V_{IN}$		.2			.2		V
Driver								
Minimum Supply to Source Differential	Pin 16 = $+V_{IN}$, I_O = 10mA		2.0	2.2		2.0	2.2	V
Maximum Output Current	Pin 16 to Pin 15 = 2V	25	40		25	40		mA
Saturation Voltage	Driver Current = 10mA		.2	.45		.2	.45	V
Current Limit Amplifier								
Input Bias Current			.2	1.0		.2	1.0	μA
Threshold Voltage	Offset Below $+V_{IN}$	225	250	275	225	250	275	mV
Threshold Supply Sensitivity	$+V_{IN}$ = 5 to 40V		.03	.25		.03	.25	%/V

Note: 2. The reference voltage will change as a function of power dissipation on the die according to the temperature coefficient of the reference and the thermal resistance, junction-to-ambient.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −40°C to +70°C for the UC2906 and 0°C to +70°C for the UC3906, $+V_{IN}$ = 10V.)

PARAMETER	TEST CONDITIONS		2906			3906			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Voltage Sense Comparator									
Threshold Voltage	As a Function of V_{REF}	L_1 = RESET	.945	.95	.955	.945	.95	.955	V/V
		L_1 = SET	.895	.90	.905	.895	.90	.905	V/V
Input Bias Current	Total Input Bias at Thresholds		−.5	−.2		−.5	−.2		μA
Current Sense Comparator									
Input Bias Current				.1	.5		.1	.5	μA
Input Offset Current				.01	.2		.01	.2	μA
Input Offset Voltage	Referenced to Pin 2, I_{OUT} = 1mA		20	25	30	20	25	30	mV
Offset Supply Sensitivity	$+V_{IN}$ = 5 to 40V			.05	.35		.05	.35	%/V
Offset Common Mode Sensitivity	CMV = 2V to $+V_{IN}$			.05	.35		.05	.35	%/V
Maximum Output Current	V_{OUT} = 2V		25	40		25	40		mA
Output Saturation Voltage	I_{OUT} = 10mA			.2	.45		.2	.45	V
Enable Comparator									
Threshold Voltage	As a Function of V_{REF}		.99	1.0	1.01	.99	1.0	1.01	V/V
Input Bias Current			−.5	−.2		−.5	−.2		μA
Trickle Bias Maximum Output Current	V_{OUT} = $+V_{IN}$ − 3V		25	40		25	40		mA
Trickle Bias Maximum Output Voltage	Volts Below $+V_{IN}$, I_{OUT} = 10mA			2.0	2.6		2.0	2.6	V
Trickle Bias Reverse Hold-Off Voltage	$+V_{IN}$ = 0V, I_{OUT} = −10μA		6.3	7.0		6.3	7.0		V
Over-Charge Terminate Input									
Threshold Voltage			.7	1.0	1.3	.7	1.0	1.3	V
Internal Pull-Up Current	At Threshold			10			10		μA
Open Collector Outputs (Pins 7, 9 and 10)									
Maximum Output Current	V_{OUT} = 2V		2.5	5		2.5	5		mA
Saturation Voltage	I_{OUT} = 1.6mA			.25	.45		.25	.45	V
	I_{OUT} = 50μA			.03	.05		.03	.05	V
Leakage Current	V_{OUT} = 40V			1	3		1	3	μA

Internal Reference Temperature Characteristic and Tolerance



OPERATION AND APPLICATION INFORMATION

Dual Level Float Charger Operation

The UC2906 is shown configured as a dual level float charger in Figure 1. All high currents are handled by the external PNP pass transistor with the driver supplying base drive to this device. This scheme uses the TRICKLE BIAS output and the charge enable comparator to give the charger a low current turn-on mode. The output current of the charger is limited to a low level until the battery reaches a specified voltage, preventing high current charging if a battery cell is shorted. Figure 2 shows the state diagram of the charger. Upon turn-on the UV sense circuitry puts the charger in state 1, the high rate bulk-charge state. In this state, once the enable threshold has been exceeded, the charger will supply a peak current that is determined by the 250mV offset in the C/L amplifier and the sensing resistor R_S.

To guarantee full re-charge of the battery, the charger's voltage loop has an elevated regulating level, V_{OC}, during state 1 and state 2. When the battery voltage reaches 95% of V_{OC}, the charger enters the over-charge state, state 2. The charger stays in this state until the OVER-CHARGE TERMINATE pin goes high. In Figure 1, the charger uses the current sense amplifier to generate this signal by sensing when the charge current has tapered to a specified level, I_{OCT}. Alternatively the over-charge could have been controlled by an external source, such as a timer, by using the $\overline{\text{OVER-CHARGE INDICATE}}$ signal at Pin 9. If a load is applied to the battery and begins to discharge it, the charger will contribute its full output to the load. If the battery drops 10% below the float level, the charger will reset itself to state 1. When the load is removed a full charge cycle will follow. A graphical representation of a charge, and discharge, cycle of the dual level float charger is shown in Figure 3.

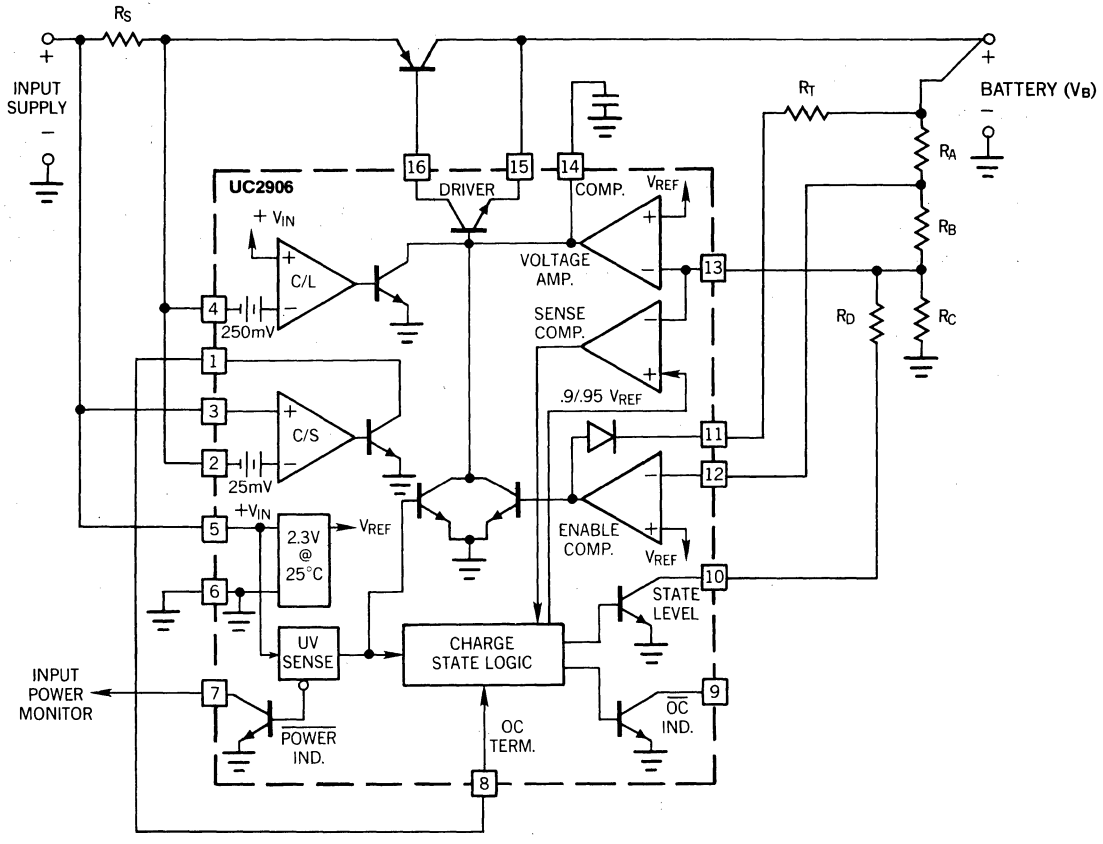
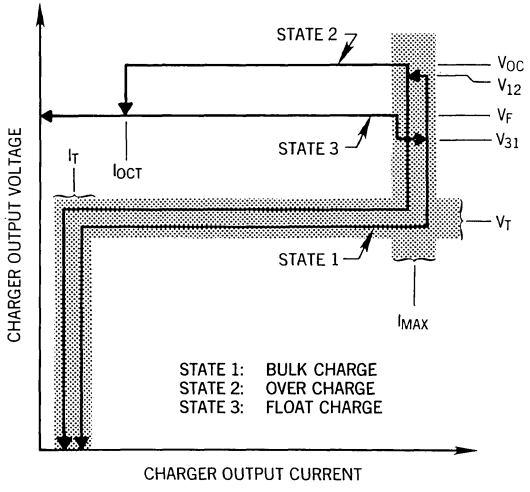


Figure 1. The UC2906 in a Dual Level Float Charger



1.) $V_T = V_{REF}\ (1 + \frac{R_A}{R_B + R_X})$ Where: $R_X = \frac{R_D\ R_C}{R_D + R_C}$

2.) $V_{OC} = V_{REF}\ (1 + \frac{R_A + R_B}{R_C} + \frac{R_A + R_B}{R_D})$

3.) $V_F = V_{REF}\ (1 + \frac{R_A + R_B}{R_C})$

4.) $V_{12} = .95\ V_{OC}$

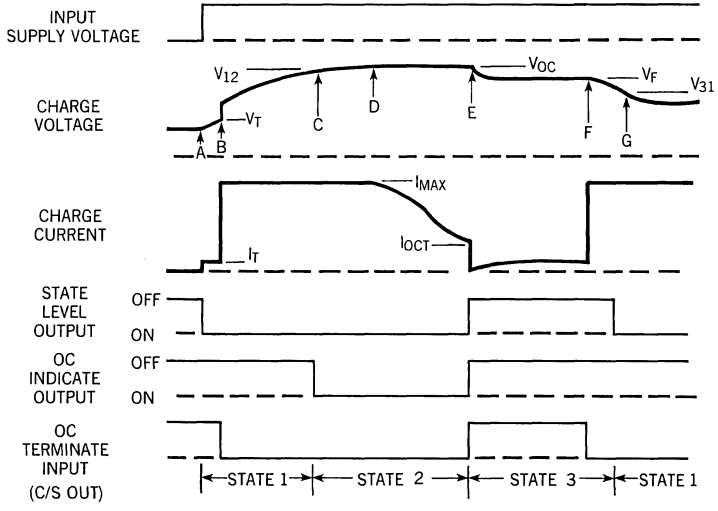
5.) $V_{31} = .9\ V_F$

6.) $I_{MAX} = \frac{.25V}{R_S}$

7.) $I_{OCT} = \frac{.025V}{R_S}$

8.) $I_T = \frac{V_{IN} - V_B - 2.5V}{R_T}$

Figure 2. State Diagram and Design Equations For the Dual Level Float Charger



Explanation: Dual Level Float Charger

A. Input power turns on, battery charges at trickle current rate.

B. Battery voltage reaches V_T enabling the driver and turning off the trickle bias output, battery charges at I_{MAX} rate.

C. Transition voltage V_{12} is reached and the charger indicates that it is now in the over-charge state, state 2.

D. Battery voltage approaches the over-charge level V_{OC} and the charge current begins to taper.

E. Charge current tapers to I_{OCT}. The current sense amplifier output, in this case tied to the OC TERMINATE input, goes high. The charger changes to the float state and holds the battery voltage at V_F.

F. Here a load ($>I_{MAX}$) begins to discharge the battery.

G. The load discharges the battery such that the battery voltage falls below V_{31}. The charger is now in state 1, again.

Figure 3. Typical Charge Cycle: UC2906 Dual Level Float Charger

Compensated Reference Matches Battery Requirements

When the charger is in the float state, the battery will be maintained at a precise float voltage, V_F. The accuracy of this float state will maximize the standby life of the battery while the bulk-charge and over-charge states guarantee rapid and full re-charge. All of the voltage thresholds on the UC2906 are derived from the internal reference. This reference has a temperature coefficient that tracks the temperature characteristic of the optimum charge and hold levels for sealed lead-acid cells. This further guarantees that proper charging occurs, even at temperature extremes.

Dual Step Current Charger Operation

Figures 4, 5 and 6 illustrate the UC2906's use in a different charging scheme. The dual step current charger is useful when a large string of series cells must be charged. The holding-charge state maintains a slightly elevated voltage across the batteries with the holding current, I_H. This will tend to guarantee equal charge distribution between the cells. The bulk-charge state is similar to that of the float charger with the exception that when V_{12} is reached, no over-charge state occurs since Pin 8 is tied high at all times. The current sense amplifier is used to regulate the holding current. In some applications a series resistor, or external buffering transistor, may be required at the current sense output to prevent excessive power dissipation on the UC2906.

A PNP Pass Device Reduces Minimum Input to Output Differential

The configuration of the driver on the UC2906 allows a good bit of flexibility when interfacing to an external pass transistor. The two chargers shown in Figures 1 and 4 both use PNP pass devices, although an NPN device driven from the source output of the UC2906 driver can also be used. In situations where the charger must operate with low input to output differentials the PNP pass device should be configured as shown in Figure 4. The PNP can be operated in a saturated mode with only the series diode and sense resistor adding to the minimum differential. The series diode, D1, in many applications, can be eliminated. This diode prevents any discharging of the battery, except through the sensing divider, when the charger is attached to the battery with no input supply voltage. If discharging under this condition must be kept to an absolute minimum, the sense divider can be referenced to the $\overline{\text{POWER INDICATE}}$ pin, Pin 7, instead of ground. In this manner the open collector off state of Pin 7 will prevent the divider resistors from discharging the battery when the input supply is removed.

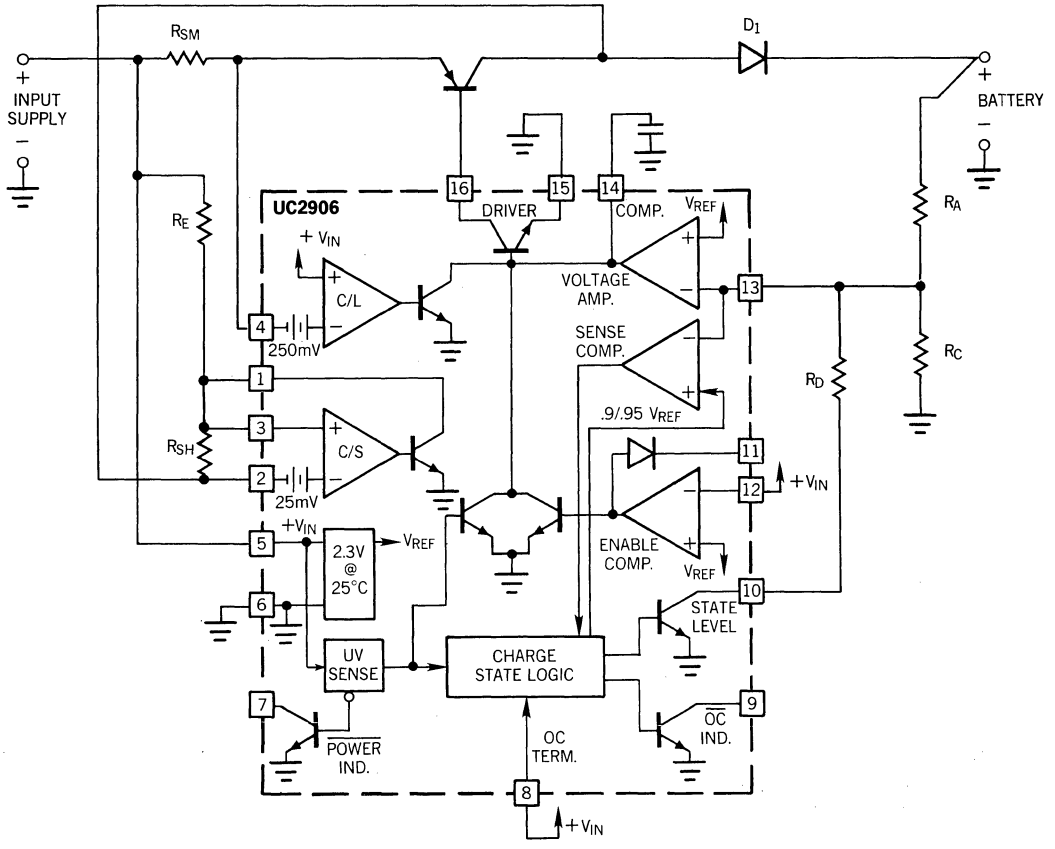
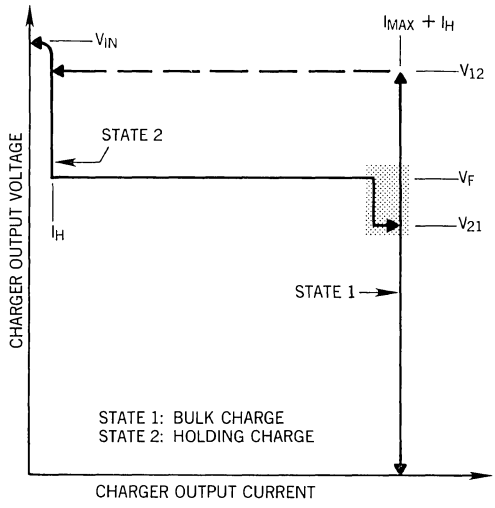


Figure 4. The UC2906 in a Dual Step Current Charger



1.) $V_{12} = .95\ V_{REF}\ (1 + \frac{R_A}{R_C} + \frac{R_A}{R_D})$

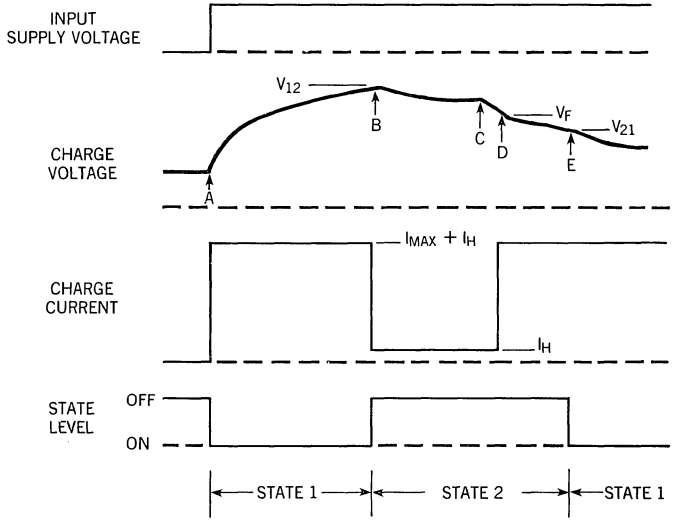
2.) $V_F = V_{REF}\ (1 + \frac{R_A}{R_C})$

3.) $V_{21} = .9\ V_F$

4.) $I_{MAX} = \frac{.25V}{R_{SM}}$

5.) $I_H = \frac{.025V}{R_{SH}}$

Figure 5. State Diagram and Design Equations for the Dual Step Current Charger



Explanation: Dual Step Current Charger

A. Input power turns on, battery charges at a rate of $I_H + I_{MAX}$.

B. Battery voltage reaches V_{12} and the voltage loop switches to the lower level V_F. The battery is now fed with the holding current I_H.

C. An external load starts to discharge the battery.

D. When V_F is reached the charger will supply the full current $I_{MAX} + I_H$.

E. The discharge continues and the battery voltage reaches V_{21} causing the charger to switch back to state 1.

Figure 6. Typical Charge Cycle: UC2906 Dual Step Current Charger

LINEAR INTEGRATED CIRCUITS

UC3850

Switching Power Supply Control System

FEATURES

- Single Chip PWM Control System
- Programmable Under-Voltage Sense
- Remote Enable with Soft-Start
- Adjustable Deadtime
- Over-Voltage Shutdown Latch
- Dual Uncommitted Output Transistors
- Double-Pulse Suppression Logic
- High-Gain, High-Output Error Amplifier
- Controlled-Gain Current Limit Amplifier
- Oscillator Disable for Current-Mode Control
- "Power Good" Logic Indication
- Internal 5V Reference Generator
- 24-Pin DIP Configuration

DESCRIPTION

The UC3850 device provides a complete control system for high-performance switching power supplies. In addition to a fixed-frequency, dual-output, pulse width modulator, these chips also contain full programming and protection circuitry. While the output of the error amplifier provides the normal regulating input to the PWM comparator, this signal may be overridden with two other comparator inputs. One is a dead-band control which serves to limit the maximum duty cycle, and the other is a protection bus activated by any of several functions. These include a current limit amplifier, an over-voltage shutdown latch, an under-voltage sense comparator and the remote enable input. These last two functions activate a soft-start with an external capacitor.

Additional features included in these devices are logic signal outputs for input "power good" and an indicator when the OVP latch is set. The internal oscillator can be disabled allowing compatability with external frequency sources, voltage feed-forward, or current-mode control.

The PWM output transistors have uncommitted collectors and emitters and have 40V, 100mA capability. The logic arrangement prevents multiple pulses per period and repetitive pulses on one output.

Packaged in a 24-pin DIP, the UC3850 is intended for operation from 0°C to +70°C and is available in either a plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS

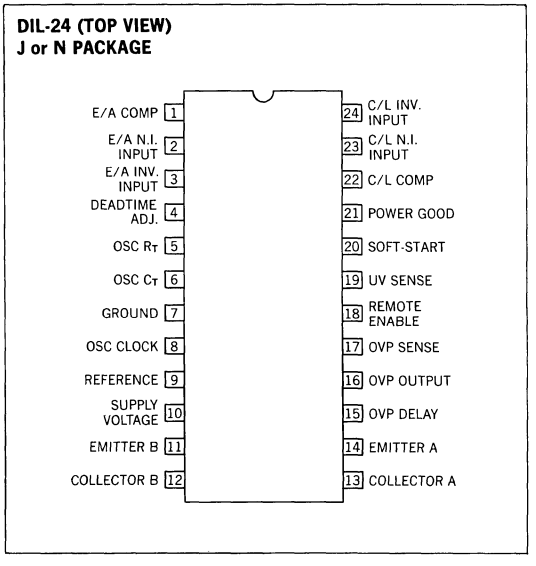
Supply Voltage (V_{IN}) 40V
Collector Voltage (V_C) 40V
Output Current (each output) 100mA
Reference Output Current 20mA
Logic Output Current Sink 10mA
Oscillator Charging Current 5mA
Input Voltage Ranges:
a. Remote Enable ..... -0.3V to V_{REF}
b. Error Amplifier ..... -0.3V to +7V
c. Current Limit Amplifier ..... -0.3V to +7V
d. Under-Voltage Sense ..... -0.3V to $+V_{IN}$
e. Over-Voltage Sense ..... -0.3V to +7V
Power Dissipation at T_A = 25°C 800mW
Derate Above 50°C ..... 8mW/°C
Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{IN} ..... 11V to 36V
Oscillator Frequency ..... 10KHz to 200KHz
Timing Resistor, R_T ..... 3KΩ to 20KΩ
Timing Capacitor, C_T ..... .001μF to 1.0μF
Error Amp Input Range ..... 1.5V to 5.5V
Current Amp Input Range ..... 0V to 5.5V

CONNECTION DIAGRAM

DIL-24 (TOP VIEW)
J or N PACKAGE



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ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = 0°C to +70° for the UC3850; V_{IN} = 24V, F_{OSC} = 40KHz.)

PARAMETERS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Reference Section					
Output Voltage	T_J = 25°C	4.8	5.0	5.2	V
Line Regulation	V_{IN} = 11V to 36V	—	0.10	0.33	mV/V
Load Regulation	I_L = 1mA to 10mA	—	10	30	mV
Temperature Stability*	Over Operating Range	—	20	50	mV
Short Circuit Current	V_{REF} = 0, T_J = 25°C	—	55	100	mA
Oscillator Section					
Nominal Frequency	R_T = 11.5K, C_T = 2.2nF	35	40	45	KHz
Temperature Stability*	Over Operating Range	—	2.5	5	%
Output Pulse Amplitude*		2.0	3.3	4.5	V
Output Pulse Width*		—	0.4	0.8	μS
Maximum Frequency	R_T = 3K, C_T =1.0nF	200	—	—	KHz
Oscillator Output Impedance		—	300	—	Ω
Error Amplifier (V_{CM} = 2.5V)					
Input Offset Voltage		—	5	10	mV
Input Bias Current		—	.05	2	μA
Input Offset Current		—	—	0.1	μA
Open Loop Voltage Gain	$R_L > 50K\Omega$	70	100	—	dB
Gain Bandwidth*	T_J = 25°C, A_V = 0dB	—	0.7	—	MHz
Common-Mode Rejection Ratio	V_{CM} = 0.3V to 5.5V	50	70	—	dB
Output Sink Current	V_O = 0.5V	0.2	0.4	1.0	mA
Output Source Current	V_O = 0V	5.0	7.0	10	mA
Output Swing	Minimum Total Range	0.5	—	4.5	V
Current Limit Amplifier (V_{CM} = 1V)					
Input Offset Voltage		—	—	30	mV
Input Bias Current		—	1	3	μA
Input Offset Current		—	—	0.2	μA
Open Loop Voltage Gain		35	40	—	dB
Output Load Resistance		32	44	56	KΩ
Response Time*		—	0.2	0.4	μS
Deadtime Control					
Nominal Deadtime	Pin 4 = Open	12	16	20	%
Minimum Deadtime	Pin 4 = V_{REF}	—	—	5	%
Control Gain	Pin 4 = 0.5V to 4.5V	—	25	—	%/V
Current to Disable Oscillator*	Pin 4 > 6V	—	—	1	mA

* These parameters although guaranteed over the recommended operating conditions, are not 100% tested in production.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = 0°C to +70° for the UC3850; V_{IN} = 24V, F_{OSC} = 40KHz.)

PARAMETERS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Under-Voltage Sense					
Lower Trip Point Threshold		4.53	4.78	5.02	V
UVS Hysteresis		—	0.25	—	V
UVS Input Current		—	-2	-10	μA
Soft-Start Charge Current	Pin 20 = 0V	56	70	84	μA
Soft-Start Discharge	Pin 20 = 4.7V	200	250	300	μA
Power Good On Threshold		4.8	5.0	5.2	V
Power Good Hysteresis		—	0.7	—	V
Remote Enable Threshold		0.8	1.6	2.0	V
Power Good Off Current	Pin 21 = 5V	—	—	10	μA
Power Good On Voltage	I_{21} = 5mA	—	0.3	0.4	V
Over-Voltage Sense					
OVS Threshold		1.9	2.0	2.1	V
OVS Input Current		—	—	10	μA
Delay Charge Current	Pin 15 = 0V	44	55	66	μA
OVP Off Current	Pin 16 = 5V	—	—	10	μA
OVP On Voltage	I_{16} = 5mA	—	.3	.4	V
Output Switches					
Collector-Emitter Voltage		—	—	20	V
Collector Leakage Current	V_{CE} = 20V	—	—	100	μA
C-E Saturation Voltage	I_C = 50mA	—	1.2	2	V
Emitter Output Voltage	V_C = 11V, I_E = 50mA	8	—	—	V
Short Circuit Current	V_{cc} = 36V	—	200	—	mA
Supply Current					
Standby	V_{cc} = 40V	—	8	12	mA
Operating	V_{cc} = 30V	—	9	14	mA

FUNCTIONAL DESCRIPTION

1. **Reference Regulator:** The regulator supplies several internal reference levels as well as a 5.0V source for external use up to 20mA.

2. **Oscillator:** An external resistor establishes a constant charging current into an external capacitor. In addition to a fixed frequency clock output, the voltage across C_T forms a sawtooth waveform for the PWM comparator. This oscillator may be synchronized to an external source with a positive input into the clock terminal. Alternatively, it may be completely disabled by raising pin 4 above V_{REF} with a source able to provide 1-10mA. In this application, pin 6 is a high impedance input into the PWM comparator and an external blanking pulse must be applied to pin 8 for latch reset and deadtime control.

3. **PWM Comparator:** The output of this comparator will go from low to high — setting the PWM Latch high — when the ramp input on pin 6 rises above the voltage level at its inverting input. This inverting input will follow the lowest of three levels — Deadtime, Error amplifier output, or the Fault line. The comparator will accept inputs down to 0V and once set, the PWM latch requires a clock signal before the next pulse can begin.

4. **Deadtime Adjust:** An internal divider establishes a nominal output duty cycle clamp at 84% but by setting pin 4 to a voltage between 0 and 5V, the duty cycle limit can be set from 0 to 95%. This pin can also be used to disable the oscillator (see above).

5. **Error Amplifier:** This amplifier provides the normal means of controlling pulse width with its gain and frequency response a function of external feedback. The amplifier is stable with closed-loop gains of 10 or above and its output cannot rise above the soft-start voltage on pin 20.

6. **Current Limit:** This amplifier takes control away from the Error amplifier when load current is excessive. The gain characteristics are non-linear to provide a rapid response to an over-current condition, but lower gain for stable current regulation after the initial transient period. Compensation of the current loop can be effected at the Fault line, pin 22.

7. **Fault Line:** Pin 22 is normally pulled to V_{REF} through an internal 44K resistor, but will be held low for any of the following conditions:
   a. Current limit amplifier active
   b. Under-voltage sense low
   c. Over-voltage sense high
   d. Remote enable low

   When the fault cause is removed, the Fault line will go high at a rate determined by the soft-start voltage on pin 20.

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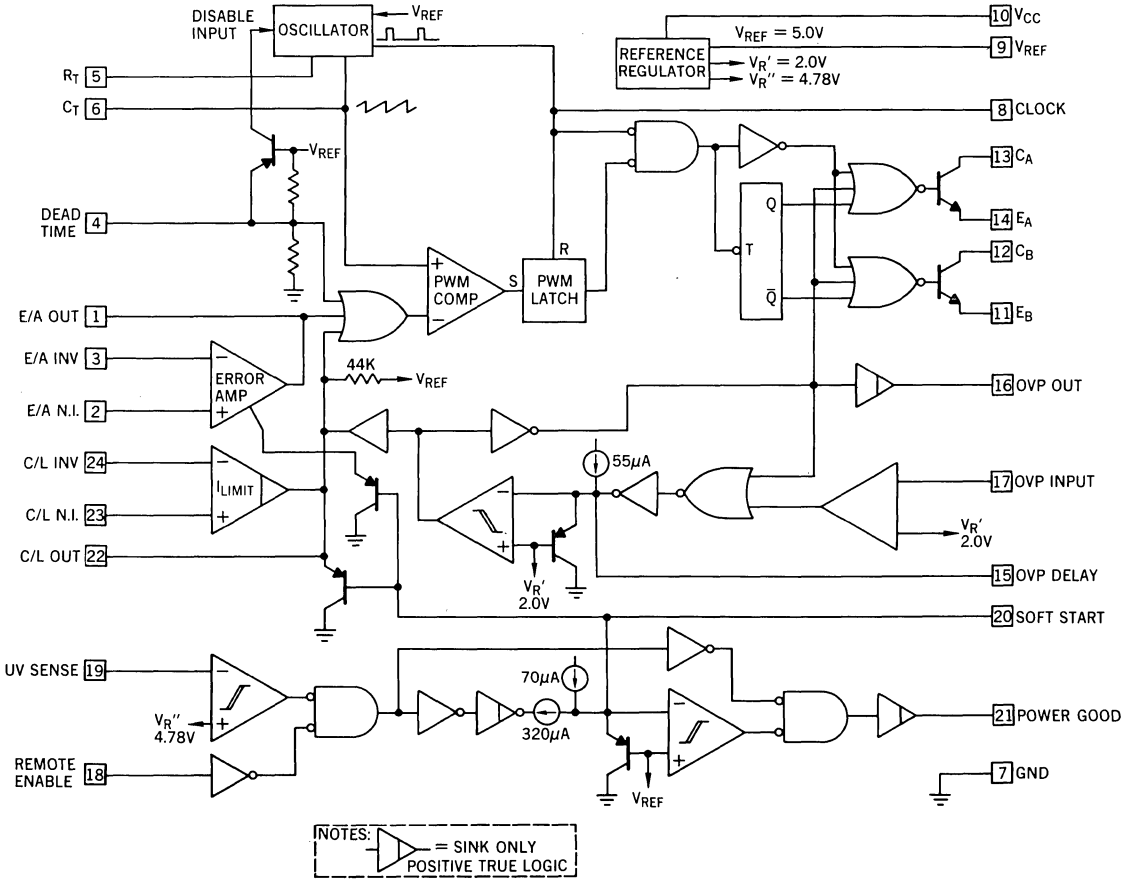
8. **Under-Voltage/Remote Sense:** The regulator will be active only when both the Under-Voltage Sense and Remote Enable inputs are high. When this occurs, a "soft-start" is effected with the internal 70μA current source and an external capacitor on pin 20. Should either input fall below its threshold, the Power Good output on pin 21 will immediately go to an active low, followed by regulator shutdown after a delay controlled by the soft-start capacitor and the net pull-down current of 250μA.

9. **Over-Voltage Sense:** When this comparator senses a voltage in excess of its threshold, with a duration longer than an interval established by the 55μA current source and an external capacitor on pin 15, the circuit will latch, terminate the PWM output signal, pull the fault line low, and indicate with a high level on pin 16, the OV shutdown state. Once latched, the circuit may be restarted by recycling the input V_{CC} voltage, momentarily lowering the Remote Enable input, or discharging the OVP delay capacitor on pin 15.

10. **Output Switches:** The switches will operate alternately with logic to insure that once a given pulse is terminated, the same output cannot reactivate during the remainder of that period or in any succeeding period until after a pulse has been delivered by the other output. The output transistors may be operated in either common emitter or common collector configuration.

3850 BLOCK DIAGRAM



LINEAR INTEGRATED CIRCUITS

Three Terminal Fixed Voltage Positive Regulators

UC7800A
UC7800AC
UC7800
UC7800C

FEATURES

- ±1% Output Voltage on 7800A, AC Series
- Complete Specifications at 1A Load
- No External Components
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe Area Compensation
- Available in TO-3 and TO-220 Packages
- Output Voltages of 5V, 12V and 15V (For Other Voltages, Please Contact the Factory)

DESCRIPTION

These three terminal monolithic positive voltage regulators employ internal current limiting, thermal shutdown and safe area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A of output current. They are intended as fixed voltage regulators in a wide range of applications including local (on card) regulation for elimination of distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents. The 7800 and 7800C series have output tolerances of ±4%. The 7800A and 7800AC series offer ±1% tolerances on initial output voltage and, in addition, are specified to provide better regulator performance.

ABSOLUTE MAXIMUM RATINGS

Input Voltage 35V
Power Dissipation ..... Internally limited
Operating Junction Temperature Range
- UC7800A SERIES ..... -55°C to +150°C
- UC7800AC SERIES ..... 0°C to +125°C
- UC7800 SERIES ..... -55°C to +150°C
- UC7800C SERIES ..... 0°C to +125°C

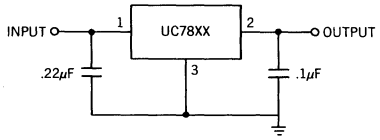
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds)
- K (TO-3) package ..... 300°C
- T (TO-220) package ..... 230°C

Power/Thermal Characteristics

	K (TO-3) Package	T (TO-220) Package
Rated Power @ 25°C		
T_C	20W	15W
T_A	4.3W	2W
Thermal Resistance		
θ_{JC}	3°C/W	3°C/W
θ_{JA}	35°C/W	60°C/W

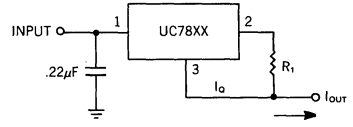
TYPICAL APPLICATIONS

Fixed Output Regulator



Notes: 1. To specify an output voltage, substitute voltage value for "XX".
2. Although no output capacitor is needed for stability, it does improve transient responses.
3. Input capacitor required if regulator is located an appreciable distance from power supply filter.

Current Regulator



$I_{OUT} = \frac{V_{OUT}}{R_1} + I_Q$

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ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	UC7805A			UC7805AC			UC7805			UC7805C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	T_j = 25°C, V_{IN} = 10V, I_O = 1A	4.95		5.05	4.95		5.05	4.8		5.2	4.8		5.2	V
	T_j = 25°C, 7.5V ≤ V_{IN} ≤ 20V 5mA ≤ I_{OUT} ≤ 1A, P_D ≤ 15W	4.9		5.1	4.87		5.13	4.8		5.2	4.77		5.23	V
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$	4.85		5.15	4.85		5.15	4.75		5.25	4.75		5.25	V
Line Regulation	T_j = 25°C, 7.5V ≤ V_{IN} ≤ 20V, I_O = 500mA			5			6			25			35	mV
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$		3	10		3	10		10	50		10	50	mV
Load Regulation	T_j = 25°C, V_{IN} = 10V, 5mA ≤ I_O ≤ 1.5A		10	12		10	17		20	26		20	40	mV
	V_{IN} = 10V, 5mA ≤ I_O ≤ 1A Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			25			25			50			50	mV
Quiescent Current	T_j = 25°C, V_{IN} = 10V, I_O = 1A		4.5	6		4.5	6		4.5	6		4.5	6	mA
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			6.5			6.5			6.5			6.5	mA
Quiescent Current Change	T_j = 25°C, V_{IN} = 10V, 5mA ≤ I_O ≤ 1A			.4			.4			.4			.4	mA
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			.5			.5			.5			.5	mA
	T_j = 25°C, 7.5V ≤ V_{IN} ≤ 20V, I_O = 500mA			.6			.6			.8			.8	mA
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			.8			.8			1.0			1.0	mA
Ripple Rejection	T_j = 25°C, 8V ≤ V_{IN} ≤ 18V, I_O = 500mA	69			69			63			63			dB
Output Noise Voltage	T_j = 25°C, V_{IN} = 10V, I_O = 1A		40			40			40			40		μV
Dropout Voltage	T_j = 25°C, I_O = 1A		2			2			2			2		V
Short Circuit Current	T_j = 25°C, V_{IN} = 10V		2.1			2.1			2.1			2.1		A
Peak Output Current	T_j = 25°C		2.4			2.4			2.4			2.4		A
Avg. Temp. Variation of V_{OUT}	0°C ≤ T_j ≤ T_{MAX}, V_{IN} = 10V, I_O = 5mA		-.4			- 4			-.4			-.4		mV/°C
Long Term Stability	1000 Hrs. @ T_j = 125°C, V_{IN} = 10V, I_O = 5mA		20			20			20			20		mV
Thermal Shutdown	V_{IN} = 10V, I_O = 5mA		175			175			175			175		°C
	T_{MAX}		150			125			150			125		°C
	T_{MIN}		-55			0			-55			0		°C

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \le 10ms$, duty-cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

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7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • TELEX 95-3040

ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	UC7812A			UC7812AC			UC7812			UC7812C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	T_j = 25°C, V_{IN} = 19V, I_O = 1A	11.88		12.12	11.88		12.12	11.52		12.48	11.52		12.48	V
	T_j = 25°C, 14.5V ≤ V_{IN} ≤ 27V 5mA ≤ I_{OUT} ≤ 1A, P_D ≤ 15W	11.76		12.24	11.70		12.30	11.52		12.48	11.46		12.54	V
	Over Temperature, T_{MIN} ≤ T_j ≤ T_{MAX}	11.64		12.36	11.64		12.36	11.40		12.60	11.40		12.60	V
Line Regulation	T_j = 25°C, 14.5V ≤ V_{IN} ≤ 27V, I_O = 500mA			12			15			60			84	mV
	Over Temperature, T_{MIN} ≤ T_j ≤ T_{MAX}		4	18		4	18		20	120		20	120	mV
Load Regulation	T_j = 25°C, V_{IN} = 19V, 5mA ≤ I_O ≤ 1.5A		12	32		12	50		50	64		50	100	mV
	V_{IN} = 19V, 5mA ≤ I_O ≤ 1A Over Temperature, T_{MIN} ≤ T_j ≤ T_{MAX}			60			60			120			120	mV
Quiescent Current	T_j = 25°C, V_{IN} = 19V, I_O = 1A		4.5	6		4.5	6		4.5	7		4.5	7	mA
	Over Temperature, T_{MIN} ≤ T_j ≤ T_{MAX}			6.5			6.5			6.5			6.5	mA
Quiescent Current Change	T_j = 25°C, V_{IN} = 19V, 5mA ≤ I_O ≤ 1A			.4			.4			.4			.4	mA
	Over Temperature, T_{MIN} ≤ T_j ≤ T_{MAX}			.5			.5			.5			.5	mA
	T_j = 25°C, 14.5V ≤ V_{IN} ≤ 27V, I_O = 500mA			.6			.6			.8			.8	mA
	Over Temperature, T_{MIN} ≤ T_j ≤ T_{MAX}			.8			.8			1.0			1.0	mA
Ripple Rejection	T_j = 25°C, 15V ≤ V_{IN} ≤ 25V, I_O = 500mA	62			62			56			56			dB
Output Noise Voltage	T_j = 25°C, V_{IN} = 19V, I_O = 5mA		75			75			75			75		μV
Dropout Voltage	T_j = 25°C, I_O = 1A		2			2			2			2		V
Short Circuit Current	T_j = 25°C, V_{IN} = 19V		1.5			1.5			1.5			1.5		A
Peak Output Current	T_j = 25°C		2.4			2.4			2.4			2.4		A
Avg. Temp. Variation of V_{OUT}	0°C ≤ T_j ≤ T_{MAX}, V_{IN} = 19V, I_O = 5mA		-.8			-.8			-.8			-.8		mV/°C
Long Term Stability	1000 Hrs. @ T_j = 125°C, V_{IN} = 19V, I_O = 5mA		50			50			50			50		mV
Thermal Shutdown	V_{IN} = 19V, I_O = 5mA		175			175			175			175		°C
	T_{MAX}		150			125			150			125		°C
	T_{MIN}		-55			0			-55			0		°C

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques (t_w ≤ 10ms, duty-cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

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ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	UC7815A			UC7815AC			UC7815			UC7815C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	T_j = 25°C, V_{IN} = 23V, I_O = 1A	14.85		15.15	14.85		15.15	14.4		15.6	14.4		15.6	V
	T_j = 25°C, 17.5V ≤ V_{IN} ≤ 30V 5mA ≤ I_{OUT} ≤ 1A, P_D ≤ 15W	14.7		15.3	14.60		15.40	14.4		15.6	14.3		15.7	V
	Over Temperature, T_{MIN} ≤ T_j ≤ T_{MAX}	14.55		15.45	14.55		15.45	14.25		15.75	14.25		15.75	V
Line Regulation	T_j = 25°C, 17.5V ≤ V_{IN} ≤ 30V, I_O = 500mA			15			19			75			100	mV
	Over Temperature, T_{MIN} ≤ T_j ≤ T_{MAX}		4	22		4	22		22	150		22	150	mV
Load Regulation	T_j = 25°C, V_{IN} = 23V, 5mA ≤ I_O ≤ 1.5A		12	35		12	50		50	80		50	120	mV
	V_{IN} = 23V, 5mA ≤ I_O ≤ 1A Over Temperature, T_{MIN} ≤ T_j ≤ T_{MAX}			75			75			150			150	mV
Quiescent Current	T_j = 25°C, V_{IN} = 23V, I_O = 1A		4.5	6		4.5	6		4.5	7		4.5	7	mA
	Over Temperature, T_{MIN} ≤ T_j ≤ T_{MAX}			6.5			6.5			6.5			6.5	mA
Quiescent Current Change	T_j = 25°C, V_{IN} = 23V, 5mA ≤ I_O ≤ 1A			.4			.4			.4			.4	mA
	Over Temperature, T_{MIN} ≤ T_j ≤ T_{MAX}			.5			.5			.5			.5	mA
	T_j = 25°C, 17.5V ≤ V_{IN} ≤ 30V, I_O = 500mA			.6			.6			.8			.8	mA
	Over Temperature, T_{MIN} ≤ T_j ≤ T_{MAX}			.8			.8			1.0			1.0	mA
Ripple Rejection	T_j = 25°C, 18.5V ≤ V_{IN} ≤ 28.5V, I_O = 500mA	60			60			54			54			dB
Output Noise Voltage	T_j = 25°C, V_{IN} = 23V, I_O = 5mA		90			90			90			90		μV
Dropout Voltage	T_j = 25°C, I_O = 1A		2			2			2			2		V
Short Circuit Current	T_j = 25°C, V_{IN} = 23V		1.2			1.2			1.2			1.2		A
Peak Output Current	T_j = 25°C		2.4			2.4			2.4			2.4		A
Avg. Temp. Variation of V_{OUT}	0°C ≤ T_j ≤ T_{MAX}, V_{IN} = 23V, I_O = 5mA		-1.0			-1.0			-1.0			-1.0		mV/°C
Long Term Stability	1000 Hrs. @ T_j = 125°C, V_{IN} = 23V, I_O = 5mA		60			60			60			60		mV
Thermal Shutdown	V_{IN} = 23V, I_O = 5mA		175			175			175			175		°C
	T_{MAX}		150			125			150			125		°C
	T_{MIN}		-55			0			-55			0		°C

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques (t_w ≤ 10ms, duty-cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

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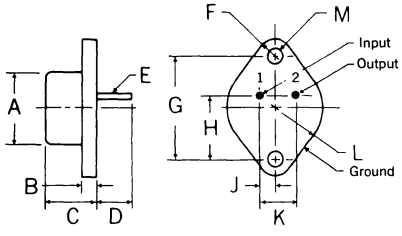
MECHANICAL SPECIFICATIONS AND CONNECTION DIAGRAMS

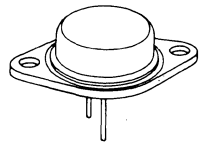
UC7800AC UC7800A SERIES
UC7800C UC7800 SERIES

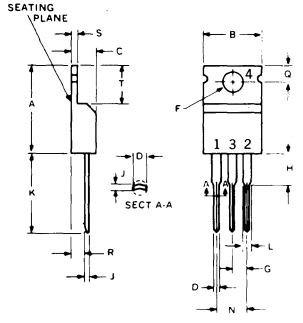


Bottom View

	INCHES	MILLIMETERS
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	.250-.450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	.188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655-.675	16.64-17.15
J	.205-.225	5.21-5.72
K	.420-.440	10.67-11.18
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.

TO-204AA K(TO-3)



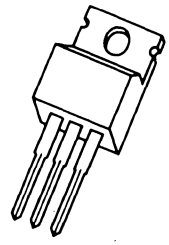


1-Input
2-Output
3-Ground
4-Ground

UC7800C UC7800AC SERIES

	INCHES		MILIMETERS	
	MIN	MAX	MIN	MAX
A	0.560	0.625	14.23	15.87
B	0.380	0.420	9.66	10.66
C	0.140	0.190	3.56	4.82
D	0.020	0.045	0.51	1.14
F	0.139	0.147	3.531	3.733
G	0.090	0.110	2.29	2.79
H	—	0.250	—	6.35
J	0.015	0.025	0.38	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.070	1.14	1.77
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.115	2.04	2.92
S	0.045	0.055	1.14	1.39
T	0.230	0.270	5.85	6.85

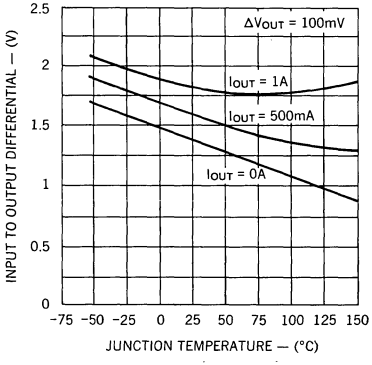
T(TO-220)



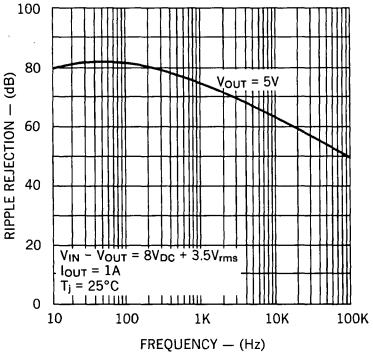
ORDERING INFORMATION

OUTPUT VOLTAGE	PACKAGE SUFFIX			
	K(TO-3)		T(TO-220)	
5V	UC7805AK UC7805ACK	UC7805K UC7805CK	— UC7805ACT	— UC7805CT
12V	UC7812AK UC7812ACK	UC7812K UC7812CK	— UC7812ACT	— UC7812CT
15V	UC7815AK UC7815ACK	UC7815K UC7815CK	— UC7815ACT	— UC7815CT

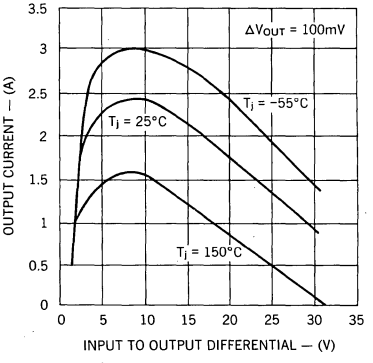
Dropout Voltage



Ripple Rejection



Peak Output Current



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LINEAR INTEGRATED CIRCUITS

Three Terminal Fixed Voltage Negative Regulators

UC7900A
UC7900AC
UC7900
UC7900C

3

FEATURES

- ±1% Output Voltage on 7900A, AC Series
- Output Current to 1.5A
- One External Component
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe Area Compensation
- Available in TO-3 and TO-220 Packages
- Output Voltages of −5V, −12V and −15V (For Other Voltages, Please Contact the Factory)

DESCRIPTION

These three terminal monolithic negative voltage regulators employ internal current limiting, thermal shutdown and safe area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A of output current. They are intended as fixed voltage regulators in a wide range of applications including local (card) regulation for elimination of distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents. The 7900 and 7900C series have output tolerances of ±4%. The 7900A and 7900AC series offer ±1% tolerances on initial output voltage and, in addition, are specified to provide better regulator performance.

ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... −35V
Input-Output Voltage Differential 30V
Power Dissipation ..... Internally limited
Operating Junction Temperature Range
  UC7900A SERIES ..... −55°C to +150°C
  UC7900AC SERIES ..... 0°C to +125°C
  UC7900 SERIES ..... −55°C to +150°C
  UC7900C SERIES ..... 0°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 seconds)
  K (TO-3) package ..... 300°C
  T (TO-220) package ..... 230°C
Power/Thermal Characteristics

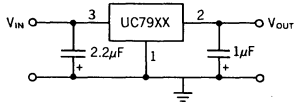
	K (TO-3) Package	T (TO-220) Package
Rated Power @ 25°C		
T_C	20W	15W
T_A	4.3W	2W
Thermal Resistance		
θ_{JC}	3°C/W	3°C/W
θ_{JA}	35°C/W	60°C/W

TYPICAL APPLICATIONS

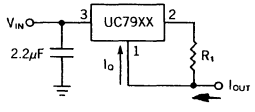
Input bypass capacitors are recommended for stable operation of the UC7900 series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

The bypass capacitors, (2.2μF on the input, 1μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10μF or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

Fixed Output Regulator



Basic Current Regulator



$$I_{OUT} = \frac{V_{OUT}}{R_1} + I_Q$$

UNITRODE

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ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	UC7905A			UC7905AC			UC7905			UC7905C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	T_j = 25°C, V_{IN} = −10V, I_O = 5mA	−5.05		−4.95	−5.05		−4.95	−5.20		−4.80	−5.20		−4.80	V
	T_j = 25°C, −25V ≤ V_{IN} ≤ −8V 5mA ≤ I_{OUT} ≤ 1.0A, P ≤ P_D	−5.10		−4.90	−5.13		−4.87	−5.20		−4.80	−5.23		−4.77	V
	Over Temperature, T_{MIN} ≤ T_j ≤ T_{MAX}	−5.15		−4.85	−5.15		−4.85	−5.25		−4.75	−5.25		−4.75	V
Line Regulation	T_j = 25°C, −25V ≤ V_{IN} ≤ −7V, I_O = 5mA		10	15		10	25		25	50		25	50	mV
Load Regulation	T_j = 25°C, V_{IN} = −10V, 5mA ≤ I_O ≤ 1.5A		20	50		20	100			50			100	mV
Quiescent Current	T_j = 25°C, V_{IN} = −10V, I_O = 500mA		1	2		1	2		1	2.5		1	2.5	mA
	Over Temperature, T_{MIN} ≤ T_j ≤ T_{MAX}			2.5			2.5			3			3	mA
Quiescent Current Change	T_j = 25°C, V_{IN} = −10V, 5mA ≤ I_O ≤ 1.5A			.4			.4			1.0			1.0	mA
	T_j = 25°C, −25V ≤ V_{IN} ≤ −8V, I_O = 500mA			.4			.4			.5			.5	mA
Ripple Rejection	T_j = 25°C, −18V ≤ V_{IN} ≤ −8V, I_O = 500mA	54			54			54			54			dB
Output Noise Voltage	f = 10Hz to 100KHz, C_L = 1μf T_j = 25°C, V_{IN} = −10V, I_O = 500mA		100			100			100			100		μV
Dropout Voltage	T_j = 25°C, I_O = 1A		2.0			2.0			2.0			2.0		V
Short Circuit Current	T_j = 25°C, V_{IN} = −10V		1.8			1.8			1.8			1.8		A
Peak Output Current	T_j = 25°C		2.0			2.0			2.0			2.0		A
Avg. Temp. Variation of V_{OUT}	0°C ≤ T_j ≤ T_{MAX}, V_{IN} = −10V, I_O = 5mA		−.4			−.4			−.4			−.4		mV/°C
Long Term Stability	1000 Hrs. @ T_j = 125°C, V_{IN} = −10V, I_O = 5mA		20			20			20			20		mV
Thermal Shutdown	V_{IN} = −10V, I_O = 5mA		175			175			175			175		°C
	T_{MAX}		150			125			150			125		°C
	T_{MIN}		−55			0			−55			0		°C

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques (t_w ≤ 10ms, duty-cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately. P_D = 20W for TO-3 (K) and 15W for TO-220 (T); Min $|V_O - V_{IN}|$ @ −55°C = 2.5V.

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ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	UC7912A			UC7912AC			UC7912			UC7912C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	T_j = 25°C, V_{IN} = −17V, I_O = 5mA	−12.12		−11.88	−12.12		−11.88	−12.48		−11.52	−12.48		−11.52	V
	T_j = 25°C, −32V ≤ V_{IN} ≤ −14V 5mA ≤ I_{OUT} ≤ 1.0A, P ≤ P_D	−12.24		−11.76	−12.30		−11.70	−12.48		−11.52	−12.54		−11.46	V
	Over Temperature, T_{MIN} ≤ T_j ≤ T_{MAX}	−12.36		−11.64	−12.36		−11.64	−12.60		−11.40	−12.60		−11.40	V
Line Regulation	T_j = 25°C, −32V ≤ V_{IN} ≤ −14V, I_O = 5mA		10	20		10	30		30	80		30	80	mV
Load Regulation	T_j = 25°C, V_{IN} = −17V, 5mA ≤ I_O ≤ 1.5A		40	80		40	80			120			240	mV
Quiescent Current	T_j = 25°C, V_{IN} = −17V, I_O = 500mA		3			3			3			3		mA
	Over Temperature, T_{MIN} ≤ T_j ≤ T_{MAX}			4			4			4			4	mA
Quiescent Current Change	T_j = 25°C, V_{IN} = −17V, 5mA ≤ I_O ≤ 1.5A			.4			.4			.8			.8	mA
	T_j = 25°C, −32V ≤ V_{IN} ≤ −14V, I_O = 500mA			.4			.4			.5			.5	mA
Ripple Rejection	T_j = 25°C, −25V ≤ V_{IN} ≤ −15V, I_O = 500mA	56			56			56			56			dB
Output Noise Voltage	f = 10Hz to 100KHz, C_L = 1μf T_j = 25°C, V_{IN} = −17V, I_O = 500mA		200			200			200			200		μV
Dropout Voltage	T_j = 25°C, I_O = 1A		1.1			1.1			1.1			1.1		V
Short Circuit Current	T_j = 25°C, V_{IN} = −17V		1.3			1.3			1.3			1.3		A
Peak Output Current	T_j = 25°C		2.0			2.0			2.0			2.0		A
Avg. Temp. Variation of V_{OUT}	0°C ≤ T_j ≤ T_{MAX}, V_{IN} = −17V, I_O = 5mA		−.9			−.9			−.9			−.9		mV/°C
Long Term Stability	1000 Hrs. @ T_j = 125°C, V_{IN} = −17V, I_O = 5mA		48			48			48			48		mV
Thermal Shutdown	V_{IN} = −17V, I_O = 5mA		175			175			175			175		°C
	T_{MAX}		150			125			150			125		°C
	T_{MIN}		−55			0			−55			0		°C

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques (t_w ≤ 10ms, duty-cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately. P_D = 20W for TO-3 (K) and 15W for TO-220 (T).

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ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	UC7915A			UC7915AC			UC7915			UC7915C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	T_j = 25°C, V_{IN} = −20V, I_O = 5mA	−15.15		−14.85	−15.15		−14.85	−15.60		−14.40	−15.60		−14.40	V
	T_j = 25°C, −35V ≤ V_{IN} ≤ −17V 5mA ≤ I_{OUT} ≤ 1.0A, P ≤ P_D	−15.30		−14.70	−15.38		−14.63	−15.60		−14.40	−15.68		−14.32	V
	Over Temperature, T_{MIN} ≤ T_j ≤ T_{MAX}	−15.45		−14.55	−15.45		−14.55	−15.75		−14.25	−15.75		−14.25	V
Line Regulation	T_j = 25°C, −35V ≤ V_{IN} ≤ −17V, I_O = 5mA		10	20		10	30		35	100		35	100	mV
Load Regulation	T_j = 25°C, V_{IN} = −20V, 5mA ≤ I_O ≤ 1.5A		50	80		50	80			150			300	mV
Quiescent Current	T_j = 25°C, V_{IN} = −20V, I_O = 500mA		3			3			3			3		mA
	Over Temperature, T_{MIN} ≤ T_j ≤ T_{MAX}			4			4			4			4	mA
Quiescent Current Change	T_j = 25°C, V_{IN} = −20V, 5mA ≤ I_O ≤ 1.5A			.4			.4			.8			.8	mA
	T_j = 25°C, −35V ≤ V_{IN} ≤ −17V, I_O = 500mA			.4			.4			.5			.5	mA
Ripple Rejection	T_j = 25°C, −28V ≤ V_{IN} ≤ −18V, I_O = 500mA	56			56			56			56			dB
Output Noise Voltage	f = 10Hz to 100KHz, C_L = 1μf T_j = 25°C, V_{IN} = −17V, I_O = 500mA		250			250			250			250		μV
Dropout Voltage	T_j = 25°C, I_O = 1A		1.1			1.1			1.1			1.1		V
Short Circuit Current	T_j = 25°C, V_{IN} = −20V		1.1			1.1			1.1			1.1		A
Peak Output Current	T_j = 25°C		2.0			2.0			2.0			2.0		A
Avg. Temp. Variation of V_{OUT}	0°C ≤ T_j ≤ T_{MAX}, V_{IN} = −20V, I_O = 5mA		−1.0			−1.0			−1.0			−1.0		mV/°C
Long Term Stability	1000 Hrs. @ T_j = 125°C, V_{IN} = −20V, I_O = 5mA		60			60			60			60		mV
Thermal Shutdown	V_{IN} = −20V, I_O = 5mA		175			175			175			175		°C
	T_{MAX}		150			125			150			125		°C
	T_{MIN}		−55			0			−55			0		°C

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques (t_w ≤ 10ms, duty-cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately. P_D = 20W for TO-3 (K) and 15W for TO-220 (T).

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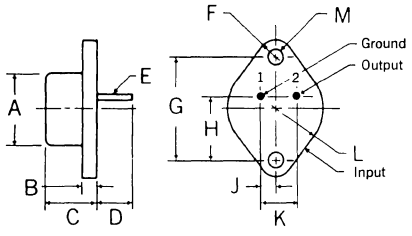
MECHANICAL SPECIFICATIONS AND CONNECTION DIAGRAMS

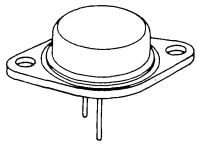
UC7900A UC7900AC SERIES
UC7900 UC7900C SERIES

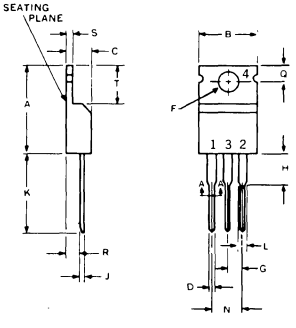


Bottom View

	INCHES	MILLIMETERS
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	.250-.450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	.188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655-.675	16.64-17.15
J	.205-.225	5.21-5.72
K	.420-.440	10.67-11.18
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.

TO-204AA K(TO-3)



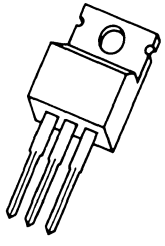


1-Ground
2-Output
3-Input
4-Input

UC7900AC UC7900C SERIES

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.560	0.625	14.23	15.87
B	0.380	0.420	9.66	10.66
C	0.140	0.190	3.56	4.82
D	0.020	0.045	0.51	1.14
F	0.139	0.147	3.531	3.733
G	0.090	0.110	2.29	2.79
H	—	0.250	—	6.35
J	0.015	0.025	0.38	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.070	1.14	1.77
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.115	2.04	2.92
S	0.045	0.055	1.14	1.39
T	0.230	0.270	5.85	6.85

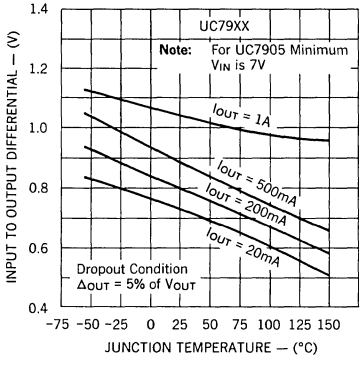
T(TO-220)



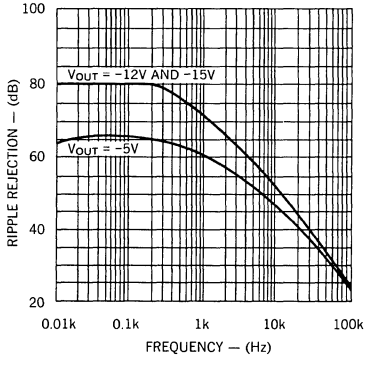
ORDERING INFORMATION

OUTPUT VOLTAGE	PACKAGE SUFFIX			
	K(TO-3)		T(TO-220)	
-5V	UC7905AK UC7905ACK	UC7905K UC7905CK	— UC7905ACT	— UC7905CT
-12V	UC7912AK UC7912ACK	UC7912K UC7912CK	— UC7912ACT	— UC7912CT
-15V	UC7915AK UC7915ACK	UC7915K UC7915CK	— UC7915ACT	— UC7915CT

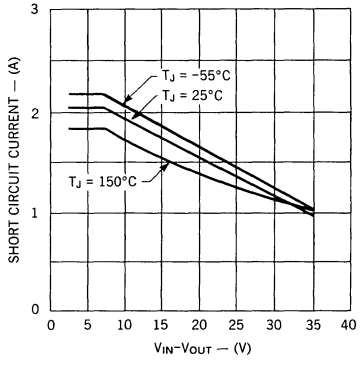
Dropout Voltage as a Function of Junction Temperature



Ripple Rejection as a Function of Frequency



Peak Output Current



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MOTION CONTROL CIRCUITS

Unitrode produces a variety of industry standard motor drivers and actuator circuits. Unitrode also has introduced many new and innovative circuits of its own offering you, the designer, with the technological difference, the best in cost performance integrated circuits.

UNITRODE DEVICE	Brush-Type Motor	Two-Phase Stepper	Micro-Stepping	Three-Phase Brushless	Solenoid Driver	Voice Coil
L292	■		■		■	■
L293	■	■				
L293D	■	■				
L295					■	
L298, L298D	■	■				■
UC3517		■				
UC3610	■	■			■	■
UC3620				■		
UC3622				■		
UC3633/3634	■			■		
UC3637	■		■			■
UC3705	■	■			■	
UC3707	■	■			■	
UC3717		■	■			
UC3717A		■	■			
UC3657				■		
UC2950	■	■		■	■	
UC3716	■		■		■	■

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MOTION CONTROL CIRCUITS

TYPE	DESCRIPTION	TYPICAL APPLICATION	V_C	V_{SS}	I_{OUT}	P_D	f_c	θ_{JC}	PACKAGE
L292	H-Bridge Transconductance amplifier with PWM current control.	DC Motors, torque control, stepping motors, microstepping solenoid controlled valves.	18 to 36 Volts		2.0 Amp Cont.	25 Watts MAX	30 kHz MAX	3.0 °C/W	15 Pin Power Tab
L293	Four Totem-Pole Drivers	DC Motors Stepping Motors	36 Volts	4.5 to 36 Volts	1.0 Amp Cont.	5.0 Watts MAX		14.0 °C/W	16 Pin DIP "BATWING"
L293D	L293 with eight bridge diodes; reduced I_{OUT}	DC Motors Stepping Motors	36 Volts	4.5 to 36 Volts	0.6A Amp Cont.	5.0 Watts MAX		14.0 °C/W	16 Pin DIP "BATWING"
L295	Dual solenoid driver with current control.	Hammer driver in matrix printers Solenoid drivers Motors	See Power Driver & Interface Circuits.						
L298 L298D	Dual Full-Bridge with individual logic inputs for each bridge. (L298D has on board diodes)	Power stage for motor and solenoid drivers. Low standby power drain makes it ideal for battery operated equipment.	V_{SS} to 46 Volts	4.5 to 7.0 Volts	2.0 Amp Cont. 1.0A Cont.	25 Watts MAX		3.0 °C/W	15 Pin Power Tab
UC1610 UC3610	Dual diode bridge with eight Schottky diodes. (V_f = 1V @ 2A)	Use as circulating diodes with motor or solenoid drivers.	40 Volts MAX		3.0 Amp MAX				8 Pin DIP
UC3620	Brushless DC motor with switching current control.	Drive brushless DC motors. Includes Hall decode logic and fixed off-time current control switching.	40 Volts MAX		2.0 Amp Cont.	25 Watts MAX	30 kHz	3.0 °C/W	15 Pin Power Tab
UC3622	Brushless DC motor with voltage mode control.	Drives brushless DC motors in fast responding, position feedback systems.	40 Volts MAX		2.0 Amp Cont.	25 Watts	30 kHz	30 °C/W	15 Pin Power Tab
UC1633 UC1634	Phase Locked Controller	Speed control for DC motors with crystal oscillator, phase detector and lock indicator.	8 to 15 Volts		16mA	1 Watt			16 Pin DIP
UC1637 UC2637 UC3637	PWM Driver for DC Servomotors; Current Limit, Under-Voltage Lock-Out.	Drive Bipolar or MOSFET Power H-Bridge in DC Velocity and Position Servo-Loops.	40 Volts MAX		500mA Peak	2.0W MAX			18 Pin DIP
UC1705* UC3705* UC1706 UC3706 UC1707 UC3707	Dual driver for power MOSFETs; 40nS into 1000pF, 1.5A peak. TTL compatible inputs.	Interface between low-level control functions and high power control devices, particularly power MOSFETs.	See Power Driver & Interface Circuits.						
UC1717 UC3717 UC3717A	Stepping motor phase driver; TTL compatible inputs. Pulse-by-pulse current control, and full output H-Bridge with diodes.	Stepping motor driver in full-step, half-step, or microstep mode. Separate digital control sets current at 100%, 60%, 19%, or zero Bipolar operation.	10 to 40 Volts	4.75 to 5.25 Volts	1.0 Amp Peak	2.0 Watts MAX	30 kHz Typ.	11.0 °C/W	16 Pin DIP "BATWING"
UC3517	Stepping modor driver, unipolar, bilevel. Minimal RFI. Activates both motor phases.	Driver for stepping motors in applications requiring least possible RFI. Internal logic for STEP, FWD/REV, and FULL STEP/HALF STEP. High voltage pulse width set by single RC.	10 to 40 Volts	4.75 to 5.25 Volts	350 mA Cont.	1.6 Watts MAX			16 Pin DIP
UC2950	Half Bridge Bipolar Switch	2-Phase Steppers Brush Type Motors 3-Phase Brushless	See Power Driver & Interface Circuits.						
UC1657 UC3657	Triple Half Bridge Power Driver	3-Phase Brushless Motors	40 Volts MAX		2.0 Amp Cont.	2.5 Watts	30 kHz	3.0 °C/W	15 Pin Power Tab
UC3176	Voice-Coil Driver	Head Positioning	25 Volts MAX		3.0 Amp MAX				15 Pin Power Tab
UC3720	Smart Switch	Any Load Switching Feedback System	See Power Driver & Interface Circuits.						

*UC1705/3705 are single drivers.

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LINEAR INTEGRATED CIRCUITS

Switchmode Driver for DC Motors

FEATURES

- Driving capability: 2A, 36V, 30KHz
- Two logic chip enable inputs
- External loop gain adjustment
- Single power supply (18 to 36V)
- Input signal symmetric to ground
- Thermal protection

DESCRIPTION

The L292 is a monlithic LSI circuit in a 15-lead Multiwatt® package. It is intended to drive DC motors controlling positioning devices such as used in typewriters, printers, plotters and other computer peripherals.

The device contains a level shifter, triangle waveform oscillator, error amplifier, PWM comparator, current sensing amplifier, H-bridge output stage with a 2A, 36V driving capability and two output enable inputs. Protection circuitry includes under-voltage output inhibit and thermal protection.

4

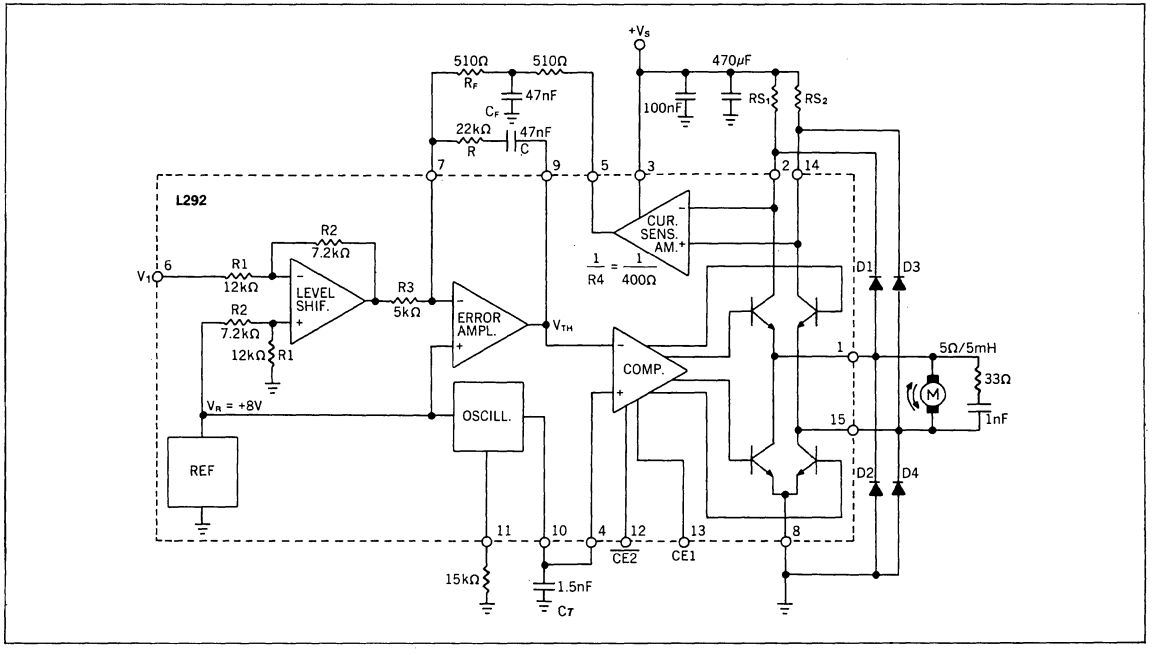
ABSOLUTE MAXIMUM RATINGS

Power Supply, V_s 36V
Input Voltage, V_1 ..... −15 to $+V_s$V
Inhibit Voltage, $V_{inhibit}$ ..... 0 to V_sV
Output Current, I_o 2.5A
Total Power Dissipation (T_{case} = 75°C) 25W
Storage and Junction Temperature, T_{stg} .....−40 to +150°C
Thermal Resistance Junction-Case, θ_{JC} ..... 3°C/W

THERMAL DATA

Thermal Resistance Junction-Case, θ_{JC} ..... 3°C/W max

BLOCK DIAGRAM



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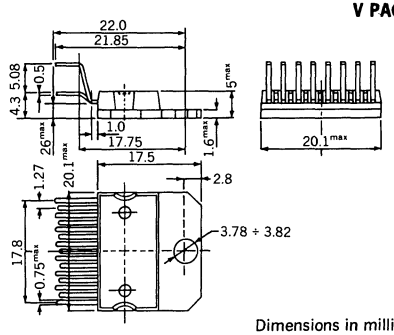
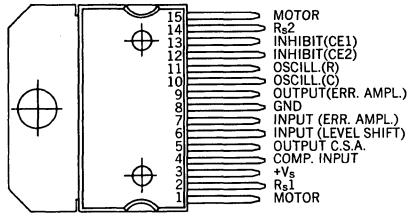
MECHANICAL DATA

V PACKAGE



Dimensions in millimeters

CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS (T_A = 25°C; f_{osc} = 20KHz unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_s			18		36	V
Quiescent Drain Current	I_d	V_s = 20V (offset null)			30	50	mA
Input Offset Voltage (Pin 6)	V_{os}	V_s = 36V, I_o = 0				±350	mV
Inhibit Input Voltage (Pin 12, 13)	$V_{inh.}$ L					2	V
	$V_{inh.}$ H			3.2			V
Inhibit Input Current	$I_{inh.}$ L	$V_{inh.}$ (L) = 0.4V				-100	μA
	$I_{inh.}$ H	$V_{inh.}$ (H) = 3.2V				10	μA
Input Current (Pin 6)	I_i		V_I = -8.8V			-1.8	mA
			V_I = +8.8V			0.5	mA
Input Voltage (Pin 6)	V_i	R_{S1} = R_{S2} = 0.2Ω	I_o = 2A		9.1		V
			I_o = -2A		-9.1		V
Output Current	I_o	V_I ± 9.8V, R_{S1} = R_{S2} = 0.2Ω		±2			A
Total Drop Out Voltage	V_D	(including sensing resistors)	I_o = 2A			5	V
			I_o = 1A			3.5	V
Sensing Resistor Voltage Drop	V_{RS}	T_j = 150°C, I_o = 2A				0.44	V
Transconductance	$\frac{I_o}{V_i}$	R_{S1} = R_{S2} = 0.2Ω		220	240	260	mA/V
		R_{S1} = R_{S2} = 0.4Ω			120		mA/V
Frequency Range (Pin 10)	f_{osc}			1		30	KHz

TRUTH TABLE

$V_{inhibit}$		Output Stage Condition
Pin 12	Pin 13	
L	L	Disabled
L	H	Normal Operation
H	L	Disabled
H	H	Disabled

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FUNCTIONAL DESCRIPTION

The error signal input has been designed to accept a bidirectional error signal symmetrical to ground. The level shifter converts the ± error signal into a single positive signal with the aid of an internally generated 8V reference. This same reference voltage supplies the triangle wave oscillator whose frequency is fixed by the external RC network (R_T, C_T - pins 11 and 10) where:

$$f_{osc} = \frac{1}{2RC} \text{ (with } R \geq 8.2K\Omega)$$

The oscillator determines the switching frequency of the output stage and should be in the range 1 to 30KHz.

Motor current is regulated by an internal loop in the L292 which is performed by the resistors R_{S1}, R_{S2} and the differential current sense amplifier, the output of which is filtered by an external RC network and fed back to the error amplifier.

The choice of the external components in this RC network (pins 5, 7, 9) is determined by the motor type and the bandwidth requirements. The values shown in the diagram are for a 5Ω, 5mH motor. (See L292 Transfer Function Calculation in Application Information).

The error signal obtained by the addition of the input and the current feedback signals (pin 7) is used to pulse width modulate the oscillator signal by means of the comparator. The pulse width modulated signal controls the duty cycle of the H-bridge to give an output current corresponding to the L292 input signal.

The interval between one side of the bridge switching off and the other switching on, τ, is programmed by C_τ in conjunction with an internal resistor R_τ.

This can be found from:

$\tau = R_\tau \cdot C_{PIN\ 10}$ (C_τ in the diagram)

Since R_τ is approximately 1.5 KΩ and the recommended τ to avoid simultaneous conduction is 2.5μS, $C_{PIN\ 10}$ should be around 1.5nF.

The current sense resistors R_{S1} and R_{S1} should be high precision types (maximum tolerance ±2%) and the recommended value is given by:

$R_{max} \cdot I_{o\ max} \leq 0.44V$

It is possible to synchronize two L292s, if desired, using the network shown in Figure 1.

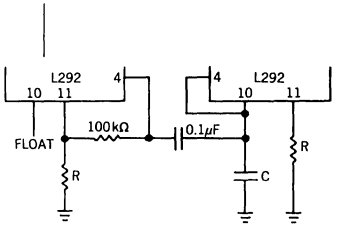


Figure 1.

Finally, two enable inputs are provided on the L292 (pins 12 and 13-active low and high respectively). Thus the output stage may be inhibited by taking pin 12 high or by taking pin 13 low. The output will also be inhibited if the supply voltage falls below 18V.

The enable inputs were implemented in this way because they are intended to be driven directly by a microprocessor. Currently available microprocessors may generate spikes as high as 1.5V during power-up. These inputs may be used for a variety of applications such as motor inhibit during reset of the logical system and power-on reset (see Figure 2).

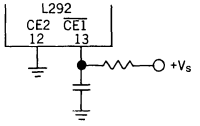


Figure 2.

APPLICATION INFORMATION

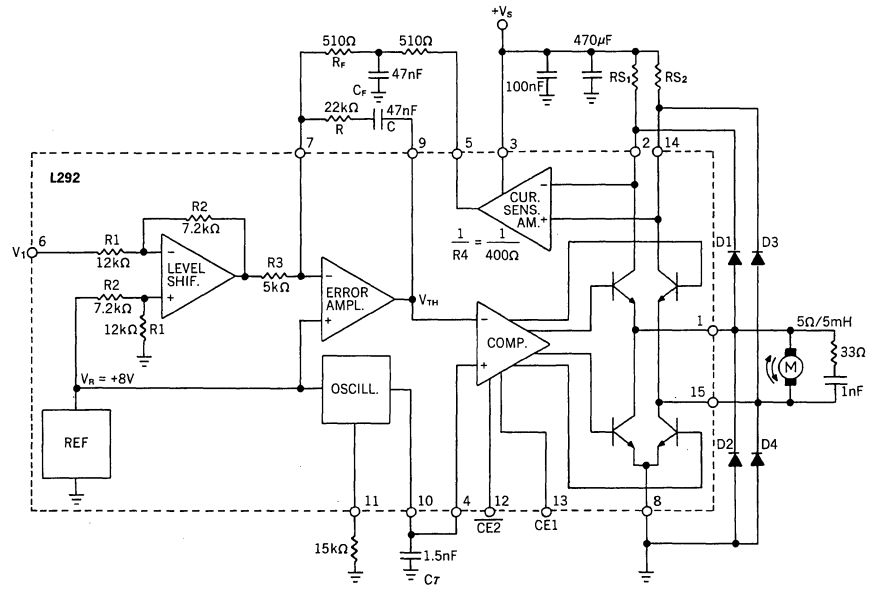
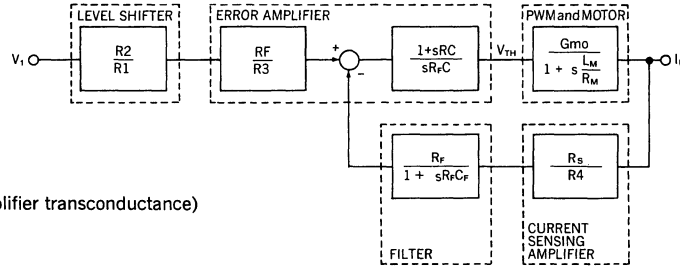


Figure 3.

The schematic diagram used for the Laplace analysis of the system is shown in Figure 4.



$R_{S1} = R_{S2} = R_S$ (sensing resistors)

$\frac{1}{R_4} = 2.5 \cdot 10^{-3}\,\Omega$ (current sensing amplifier transconductance)

L_M = Motor inductance

R_M = Motor resistance

I_M = Motor current

$G_{mo} = \frac{I_M}{V_{TH}}\Big|_{s=0}$ (DC transfer function from the input of the comparator (V_{TH}) to the motor current (I_M)).

Figure 4.

APPLICATION INFORMATION (continued)

Neglecting the $V_{CE\ sat}$ of the bridge transistor and the V_{BE} of the diodes:

$$G_{mo} = \frac{1}{R_M}\ \frac{2V_S}{V_R} \quad \text{where: } V_S = \text{supply voltage} \quad (1)$$

V_R = 8V (reference voltage)

DC Transfer Function

In order to be sure that the current loop is stable the following condition is imposed:

$$1 + sRC = 1\ s\ \frac{L_M}{R_M} \quad \text{(pole cancellation)} \quad (2)$$

from which $RC = \frac{L_M}{R_M}$ (Note that in practice R must be greater than 5.6KΩ)

The transfer function is then, (3)

$$\frac{I_M}{V_i}(s) = \frac{R_2R_4}{R_1R_3}\ G_{mo}\ \frac{1 + sR_FC_F}{G_{mo}R_s + s\ R_4C + s^2\ R_FC_FR_4C}$$

In DC condition, this is reduced to

$$\frac{I_M}{V_i}(o) = \frac{R_2R_4}{R_1R_3} \cdot \frac{1}{R_s} = \frac{0.048}{R_s}\ \left[\frac{A}{V}\right]$$

Open-Loop Gain and Stability Criterion

For $RC = L_M/R_M$, the open loop gain is: (5)

$$A\beta = \frac{1}{sR_FC} \cdot G_{mo}\ \frac{R_s}{R_4}\ \frac{R_F}{1 + sR_FC_F} = \frac{G_{mo}\ R_s}{R_4C}\ \frac{1}{s\ (1 + sR_FC_F)}$$

In order to achieve good stability, the phase margin must be greater than 45°C when $|A\beta| = 1$.

That means that, at $f_F = \frac{1}{2\pi R_FC_F}$, $|A\beta|$ must be < 1 (see Figure 5), that is:

$$|A\beta|\ f = \frac{1}{2\pi R_FC_F} = \frac{G_{mo}R_s}{R_4C}\ \frac{R_FC_F}{\sqrt{2}} < 1 \quad (6)$$

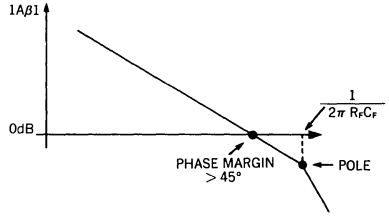


Figure 5. Open-Loop Frequency Response

Closed-Loop System Step Response

a) Small-signals analysis

The transfer function (3) can be written as follows:

$$\frac{I_M}{V_i}(s) = \frac{0.048}{R_s}\ \frac{1 + \frac{s}{2\ \xi\ \omega_o}}{1 + \frac{2\xi s}{\omega_o} + \frac{s^2}{\omega_o^2}} \quad (7)$$

where: $\omega_o = \sqrt{\frac{G_{mo}R_s}{R_4C\ R_FC_F}}$ is the cutoff frequency

where: $\xi = \sqrt{\frac{R_4C}{4\ R_FC_F\ G_{mo}\ R_s}}$ is the damping factor

By choosing the ξ value, it is possible to determine the system response to an input step signal. Examples:

1) $\xi = 1$ from which

$$I_M(t) = \frac{0.048}{R_s}\ [1 - e^{-\frac{t}{2R_FC_F}}\ (1 + \frac{t}{4\ R_FC_F})\ ] \cdot V_i$$

(where V_i is the amplitude of the input step).

2) $\xi = \frac{1}{\sqrt{2}}$ from which

$$I_M(t) = \frac{0.048}{R_s}\ (1 - \cos\ \frac{t}{2R_FC_F}\ e^{-\frac{t}{2R_FC_F}})\ V_i$$

From Figure 7 it is possible to verify that the L292 works in "closed-loop" conditions during the entire motor current rise-time: the voltage at pin 7 (inverting input of the error amplifier is locked to the reference voltage V_R, present at the non-inverting input of the same amplifier.

The previous linear analysis is correct for this example.

Decreasing the ξ value, the rise-time of the current decreases. But for a good stability, from relationship (6), the minimum value of ξ is:

$$\xi_{min} = \frac{1}{2\sqrt[4]{2}} \quad \text{(phase margin = 45°)}$$

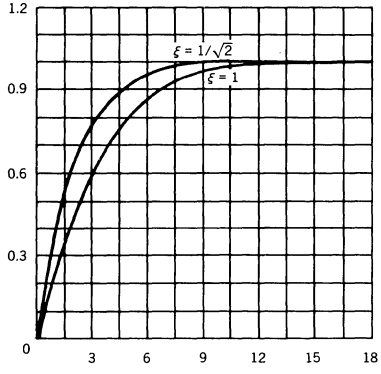
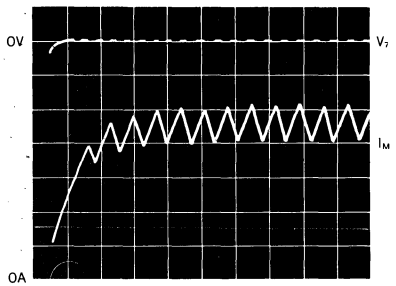


Figure 6. Small Signal Step Response (Normalized Amplitude vs t/R_FC_F)

APPLICATION INFORMATION (continued)

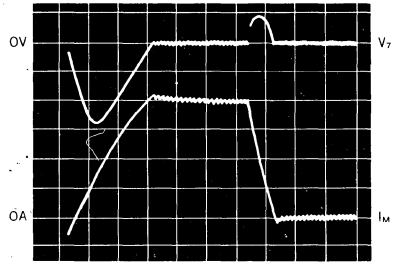


V_7 = 200mV/div.
I_M = 100mA/div.
t = 100μs/div.
with V_1 = 1.5 Vp.

Figure 7. Motor Current and Pin 7 Voltage Waveforms (Application of Figure 3). Small Signal Response

b) Large signal response

The large step signal response is limited by slew-rate and inductive load. In this case, during the rise-time of the motor current, the L292 works in open-loop condition, as can be seen from Figure 8.



V_7 = 1V/div.
I_M = 0.5A/div.
t = 500μs/div.

Figure 8. Motor Current and Pin 7 Voltage Waveforms (Application of Figure 3). Large Signal Response

The voltage at pin 7 (inverting input of the error amplifier) departs from the reference voltage V_R present at the non-inverting input and the feedback loop is open.

The feedback loop is on when the motor current reaches its steady-state value (2A).

Closed Loop System Bandwidth

A good choice for ξ is the value $1/\sqrt{2}$. In this case:

$$\frac{I_M}{V_i}(s) = \frac{0.048}{R_s} \cdot \frac{1 + s\,R_F C_F}{1 + 2s\,R_F C_F + 2s^2 R_F^2 C_F^2} \qquad (8)$$

The module of the transfer function is: (9)

$$\left|\frac{I_M}{V_i}\right| = \frac{0.048}{R_s} \cdot \frac{2\sqrt{1 + \omega^2 R_F^2 C_F^2}}{\sqrt{[(1 + 2\omega R_F C_F)^2 + 1] \cdot [(1 - 2\omega R_F C_F)^2 + 1]}}$$

The cutoff frequency is derived from expression (9) by putting

$$\left|\frac{I_M}{V_i}\right| = 0.707 \cdot \frac{0.048}{R_s} \text{ (-3dB);}$$

from which:

$$\omega_T = \frac{0.9}{R_F C_F} \qquad f_T = \frac{0.9}{2\pi R_F C_F} \qquad (10)$$

Note that R_F must be less than 1.5KΩ in order to have the maximum current swing at the output of current sensing amplifier.

Working Frequency and Motor Current Ripple

For a value of rotation speed ω the e.m.f. E is equal to $K_E\omega$, where K_E is the motor speed constant.

Neglecting the motor resistance R_M, the V_{CEsat} of the bridge transistors and the V_{BE} of the diodes, we have:

$$\Delta t_1 = \frac{\Delta I_M}{V_s - E} L_M \quad \text{(transistors conduction period)} \qquad (11)$$

$$\Delta t_2 = \frac{\Delta I_M}{V_s + E} L_M \quad \text{(diodes conduction period)}$$

Where ΔI_M is the current ripple in the motor (see Figure 9).

The working frequency is:

$$f = \frac{1}{2\,R_T C_T} = \Delta t_1 = \Delta t_2 \qquad (12)$$

where R_T is the resistance at pin 11 and C_T the capacitor at pin 10. R_T must be ≥8.2KΩ due to the output current capability at pin 11.

If we consider E = 0 (ω = 0; motor stopped) we have:

$$\Delta t_1 = \Delta t_2 = \frac{\Delta I_M}{V_s} L_M \qquad (13)$$

from this formula we can write

$$\Delta I_M = \frac{V_s}{L_M} \frac{T}{2} \qquad \left(\frac{T}{2} = \Delta t_1 = \Delta t_2 = \text{half period}\right) \qquad (13 \text{ bis})$$

The motor current ripple ΔI_M must be limited in order to reduce dissipation in the motor and the peak output current of the L292.

ΔI_{Mmax} should be less than 10% of I_{Mmax} (see Figure 9).

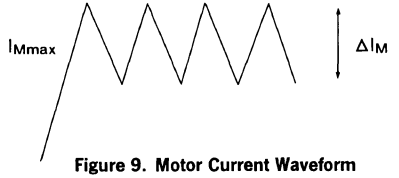


Figure 9. Motor Current Waveform

From the equation (13 bis) and considering $\Delta I_M = 0.1\, I_{M\,max}$ we have:

$$0.1\, I_{Mmax} = \frac{V_s}{2f\, L_{Mmin}} \qquad (14)$$

from which:

$$L_{Mmin} = \frac{5\, V_s}{f\, I_{Mmax}} \qquad (15)$$

The switching characteristics of the L292 demand that the working frequency f is less than 30KHz.

If for f = 30KHz, L_M is less than $L_{M\,min}$, an external inductor should be put in series with the motor.

From relationship (15) we have:

$$L_{series} = \frac{5\ V_s}{f\ I_{M\,max}} - L_M \qquad (16)$$

Deadtime

A problem associated with the system used in the L292 is the danger of simultaneous conduction in both legs of the output bridge which, if it were allowed to occur would damage them. To overcome this the comparator that drives the final stage in effect consists of two separate comparators (Figure 10): both receive the same Vt signal but on opposite inputs. The other two inputs are driven by V_{TH} shifted by plus or minus $R_T I'$. This voltage shift when compared with Vt results in a delay in switching from one comparator to the other. In this way there will always be a delay between switching off one leg of the bridge and switching on the other. The delay τ is a function of the integrated resistor R_T (1.5K) and an external capacitor C_T connected to pin 10 which also fixes oscillator frequency.

It is: $\tau = R_T C_T$

In a typical application, a capacitor of 1.5nF is used to give a switching delay of 2.25μs, a more than adequate time when you consider that the switch-off delay of the integrated transistors is only 0.5μs.

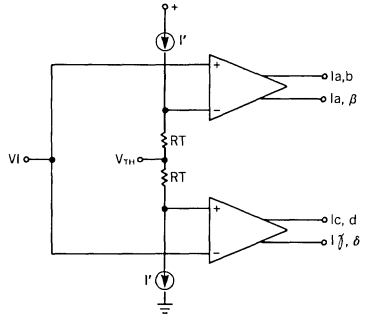


Figure 10. L292 Deadtime Control

Efficiency and Power Dissipation

The expression for the bridge efficiency, independently of the losses due to the switching times and neglecting the dissipation due to the motor current ripple, is:

$$\eta = 1 - \frac{\Delta t_1}{\Delta t_1 + \Delta t_2} \cdot \frac{V_{sat}}{V_s} - \frac{\Delta t_2}{\Delta t_1 + \Delta t_2} \cdot \frac{V_{over}}{V_s} \qquad (17)$$

where $V_{over} \cong 2V\ (2V_{BE} + R_s I_M)$
$V_{sat} \cong 4V\ (2V_{CE\,sat} + 3V_{BE})$
Δt_1 = transistors conduction period.
Δt_2 = diodes conduction period.

If $\Delta t_1 \gg \Delta t_2$ and $V_s = 20V$, we obtain:

$$\eta = 1 - \frac{4}{20} = 80\% \qquad (18)$$

In practice, the efficiency will be slightly lower due to the signal circuit dissipation (1W @ 20V) and the finite switching times (about 1W). If we transfer to the motor a power of 40W the bridge power dissipation from (18) is 10W and the total dissipation is 12W. This is an actual efficiency of 77%. Considering a maximum dissipation equal to 20W for the L292 (Multiwatt package), it is possible to handle continuous powers greater than 60W.

EXAMPLE

a) Data
- Motor characteristics: $L_M = 5mH$, $R_M = 5\Omega$, $L_M/R_M = 1msec$
- Voltage and current characteristics: $V_s = 20V$ $I_M = 2A$ $V_i = 8.3V$
- Closed loop bandwidth: 3kHz.

b) Calculation
- From relationship (4):

$$R_s = \frac{0.048}{I_M} V_i = 0.2\Omega$$

and from (1):

$$G_{mo} = \frac{2V_s}{R_M V_R} 1\Omega^{-1}$$

- RC = 1msec [from expression (2)].
- Assuming $\xi = 1/\sqrt{2}$; from (7) follows:

$$\xi^2 = \frac{1}{2} = \frac{400\ C}{4\ R_F C_F \cdot 0.2}$$

The cutoff frequency is:

$$f_T = \frac{143 \cdot 10^{-3}}{R_F C_F} = 3kHz$$

c) Summarizing
- $RC = 1 \cdot 10^{-3}$ sec
- $\frac{1000\ C}{R_F C_F} = 1$
- $R_F C_F \cong 47\mu s$

} C = 47nF, R = 22KΩ

For $R_F = 510\Omega$ → $C_F = 92nF$

LINEAR INTEGRATED CIRCUITS

Push-Pull Four Channel Driver

L293
L293D

FEATURES

- Output current 1A per channel (600mA for L293D)
- Peak output current 2A per channel (1.2A for L293D)
- Inhibit facility
- High noise immunity
- Separate logic supply
- Over-temperature protection

DESCRIPTION

The L293 and L293D are quad push-pull drivers capable of delivering output currents to 1A or 600mA per channel respectively. Each channel is controlled by a TTL-compatible logic input and each pair of drivers (a full bridge) is equipped with an inhibit input which turns off all four transistors. A separate supply input is provided for the logic so that it may be run off a lower voltage to reduce dissipation.

Additionally the L293D includes the output clamping diodes within the IC for complete interfacing with inductive loads.

Both devices are packaged in 16-pin plastic DIPs; both use the four center pins to conduct heat to the printed circuit boards.

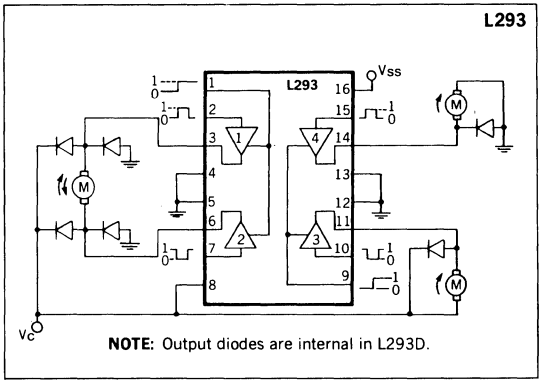
ABSOLUTE MAXIMUM RATINGS

Collector Supply Voltage, V_c 36V
Logic Supply Voltage, V_{ss} 36V
Input Voltage, V_i 7V
Inhibit Voltage, V_{inh} 7V
Peak Output Current (Non-Repetitive), I_{out} (L293) 2A
I_{out} (L293D) 1.2A
Total Power Dissipation at $T_{ground-pins}$ = 80°C, P_{tot} 5W
Storage and Junction Temperature, T_{stg}, T_j .....-40 to +150°C

THERMAL DATA

Thermal Resistance Junction-Case, θ_{JC} ..... 14°C/W max
Thermal Resistance Junction-Ambient, θ_{JA} ..... 80°C/W max

BLOCK DIAGRAM



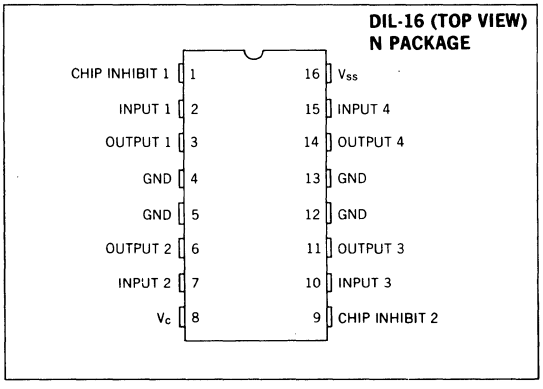
NOTE: Output diodes are internal in L293D.

TRUTH TABLE

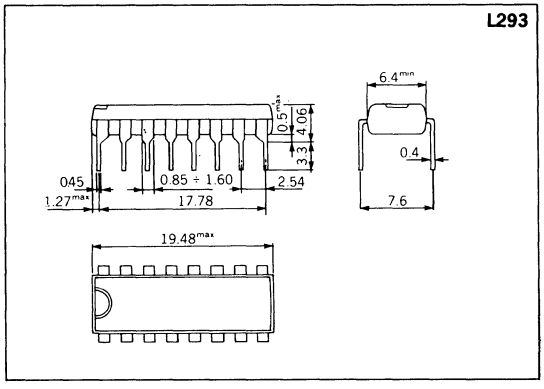
V_i (each channel)	V_{inh}.*	V_o
H	H	H
L	H	L
H	L	X**
L	L	X**

*Relative to the considered channel.
**High output impedance.

CONNECTION DIAGRAM



MECHANICAL DATA



UNITRODE

ELECTRICAL CHARACTERISTICS (For each channel, V_c = 24V, V_{ss} = 5V, T_{amb} = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Collector Supply Voltage	V_c				36	V
Logic Supply Voltage	V_{ss}		4.5		36	V
Collector Supply Current	I_c	V_i = L, I_o = 0, $V_{inh.}$ = H		2	6	mA
		V_i = H, I_o = 0, $V_{inh.}$ = H		16	24	
		$V_{inh.}$ = L			4	
Total Quiescent Logic Supply Current	I_{ss}	V_i = L, I_o = 0, $V_{inh.}$ = H		44	60	mA
		V_i = H, I_o = 0, $V_{inh.}$ = H		16	22	
		$V_{inh.}$ = L		16	24	
Input Low Voltage	V_{iL}		-0.3		1.5	V
Input High Voltage	V_{iH}	$V_{ss} \leq 7V$	2.3		V_{ss}	V
		$V_{ss} > 7V$	2.3		7	
Low Voltage Input Current	I_{iL}	V_i = L			-10	μA
High Voltage Input Current	I_{iH}	V_i = H		30	100	μA
Inhibit Low Voltage	$V_{inh.L}$		-0.3		1.5	V
Inhibit High Voltage	$V_{inh.H}$	$V_{ss} \leq 7V$	2.3		V_{ss}	V
		$V_{ss} > 7V$	2.3		7	
Low Voltage Inhibit Current	$I_{inh.L}$			-30	-100	μA
High Voltage Inhibit Current	$I_{inh.H}$				10	μA
Source Output Saturation Voltage	V_{CEsatH}	I_o = -1A (-0.6A for L293D)		1.4	1.8	V
Sink Output Saturation Voltage	V_{CEsatL}	I_o = 1A (0.6A for L293D)		1.2	1.8	V
Clamp Diode Forward Voltage (L293D only)	V_F	I_F = 0.6A		1.3		V
Rise Time	t_r	0.1 to 0.9 V_o (See Figure 1)		250		ns
Fall Time	t_f	0.9 to 0.1 V_o (See Figure 1)		250		ns
Turn-On Delay	t_{ON}	0.5 V_i to 0.5 V_o (See Figure 1)		450		ns
Turn-Off Delay	t_{OFF}	0.5 V_i to 0.5 V_o (See Figure 1)		200		ns

SCHEMATIC DIAGRAM

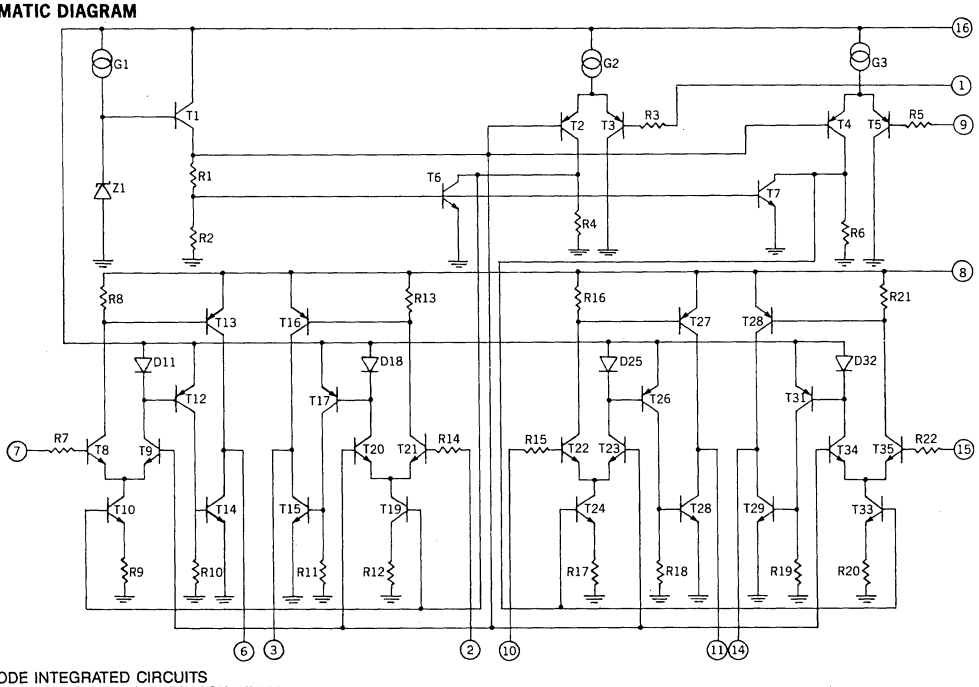


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Figure 1. Switching Times

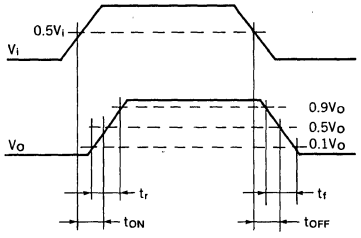


Figure 2. Quiescent Logic Supply Current vs Logic Supply Voltage

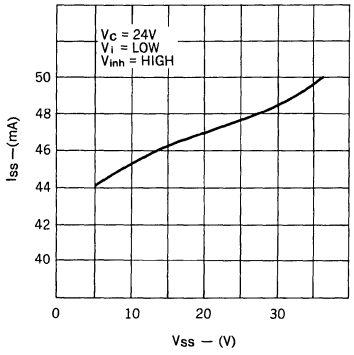


Figure 3. Output Voltage vs Input Voltage

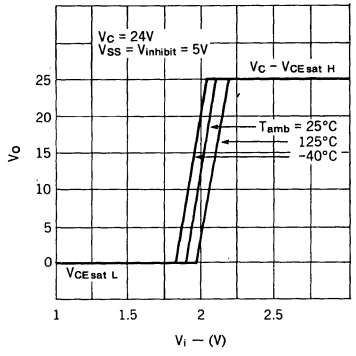


Figure 4. L293 Saturation vs Output Current

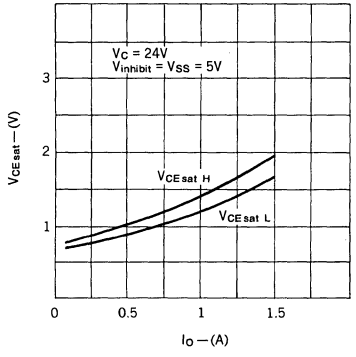


Figure 5. L293 Source Saturation vs Ambient Temperature

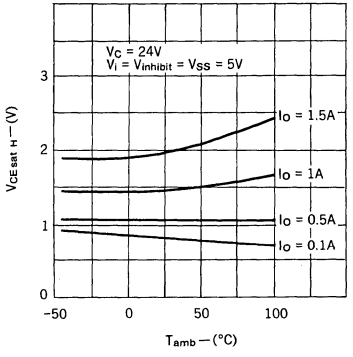
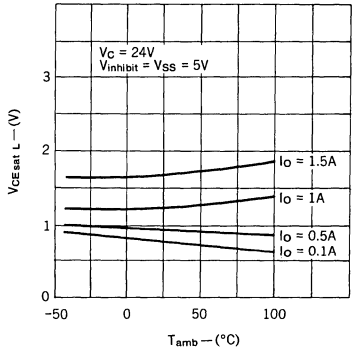


Figure 6. L293 Sink Saturation Voltage vs Ambient Temperature



NOTE: For L293D curves, multiply output current by 0.6

Figure 7. DC Motor Controls (with Connection to Ground and to the Supply Voltage)

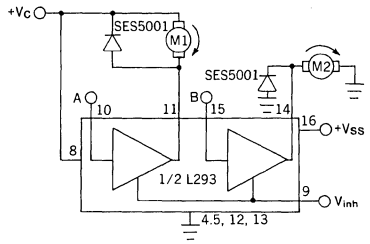
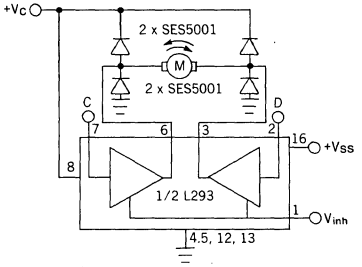


Figure 8. Bidirectional DC Motor Control



Vinh.	A	M1	B	M2
H	H	Fast Motor Stop	H	Run
H	L	Run	L	Fast Motor Stop
L	X	Free Running Motor Stop	X	Free Running Motor Stop

L = Low H = High X = Don't care

INPUTS		FUNCTION
Vinh. = H	C = H; D = L	Turn Right
	C = L; D = H	Turn Left
	C = D	Fast Motor Stop
Vinh. = L	C = X; D = X	Free Running Motor Stop

L = Low H = High X = Don't care

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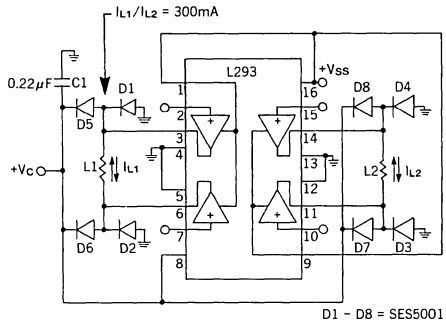


Figure 9. Bipolar Stepping Motor Control

MOUNTING INSTRUCTIONS

The $R_{thj-amp}$ of the L293 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heatsink.

The diagram of Figure 13 shows the maximum package power P_{tot} and the θ_{JA} as a function of the side " ℓ " of two equal square copper areas having a thickness of 35μ (see Figure 12). In addition, it is possible to use an external heatsink (see Figure 14).

During soldering the pins' temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 10. Example of P.C. Board Copper Area which is used as Heatsink

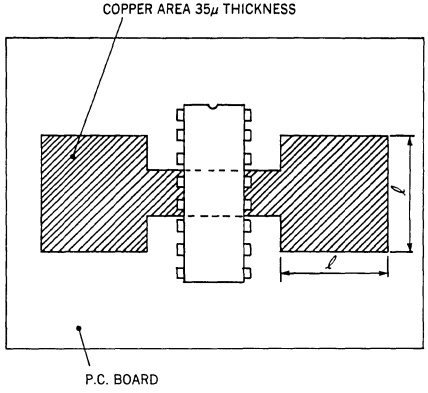


Figure 11. External Heatsink Mounting Example (θ_{JA} = 25°C/W)

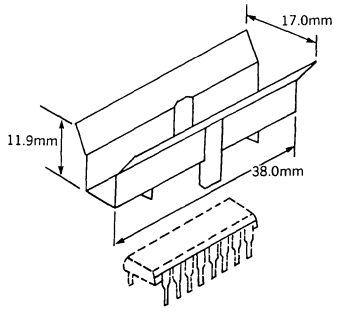


Figure 12. Maximum Package Power and Junction to Ambient Thermal Resistance vs Size " ℓ "

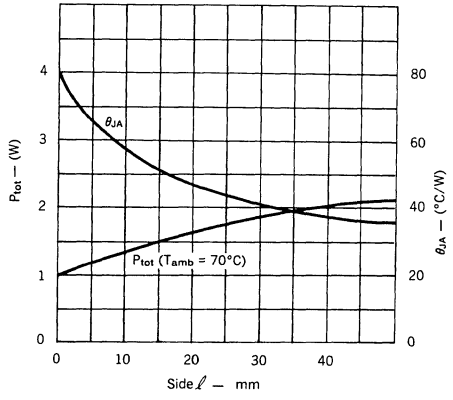
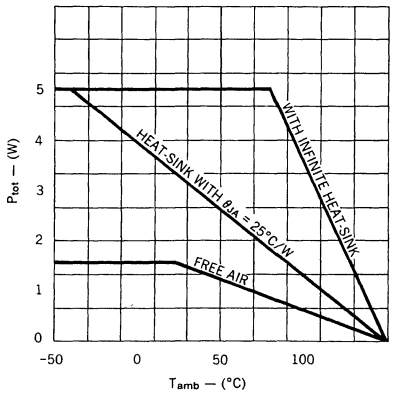


Figure 13. Maximum Allowable Power Dissipation vs Ambient Temperature



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LINEAR INTEGRATED CIRCUITS

Dual Full-Bridge Driver Power

FEATURES

- Operating Supply Voltage up to 46V
- Total Saturation Voltage 3.4V max at 1A
- Overtemperature Protected
- Operates in Switched and Linear Regulation Modes
- 25W Power-Tab Package for Low Installed Cost
- Individual Logic Inputs for Each Driver
- Channel-Enable Logic Inputs for Driver Pairs

DESCRIPTION

The L298 is a power integrated circuit usable for driving resistive and inductive loads. This device contains four push-pull drivers with separate logic inputs. Two enable inputs are provided for power down and chopping. Each driver is capable of driving loads up to 2A continuously.

Logic inputs to the L298 have high input thresholds (1.85V) and hysteresis to provide trouble-free operation in noisy environments normally associated with motors and inductors. The L298 input currents and thresholds allow the device to be driven by TTL and CMOS systems without buffering or level shifting.

The emitters of the low-side power drivers are separately available for current sensing. Feedback from the emitters can be used to control load current in a switching mode, or can be used to detect load faults.

Separate logic and load supply lines are provided to reduce total IC power consumption. Power consumption is reduced further when the enable inputs are low. This makes the L298 ideal for systems that require low standby current, such as portable or battery-operated equipment.

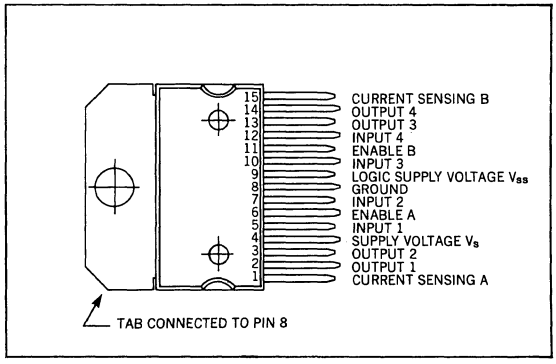
ABSOLUTE MAXIMUM RATINGS

Power Supply, V_s 50V
Logic Supply Voltage, V_{ss} 7V
Input and Inhibit Voltage, V_i, $V_{inhibit}$ ..... -0.3V to +7V
Peak Output Current (each channel), I_o
  Non-Repetitive (t = 100μs) 3A
  Repetitive (80% on - 20% off; t_{ON} = 10ms) 2.5A
  DC Operation 2A
Sensing Voltage, V_{sens} ..... -1V to +2.3V
Total Power Dissipation (T_{case} = 75°C), P_{tot} 25W
Storage and Junction Temperature, T_{stg}, T_j ..... -40°C to +150°C

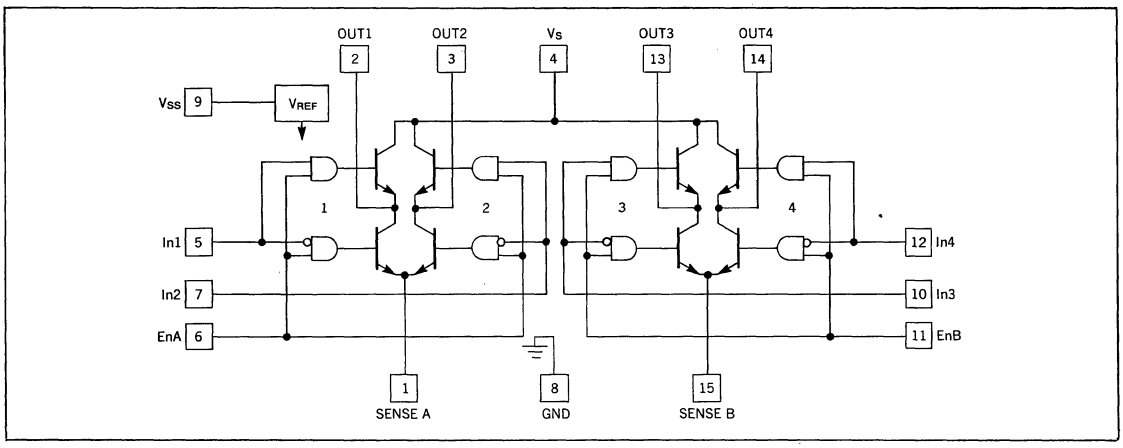
THERMAL DATA

Thermal Resistance Junction-Case, $R_{th\ j\text{-}case}$ ..... 3°C/W max.
Thermal Resistance Junction-Ambient, $R_{th\ j\text{-}amb}$ ..... 35°C/W max.

CONNECTION DIAGRAM



BLOCK DIAGRAM



UNITRODE

ELECTRICAL CHARACTERISTICS (for each channel, V_s = 42V, V_{ss} = 5V, T_j = 25°C)

PARAMETERS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage (Pin 4), V_s	Operative Condition	V_{IH}+2.5		46	V
Logic Supply Voltage (Pin 9), V_{ss}		4.5		7	V
Quiescent Supply Current (Pin 4), I_s	$V_{inh.}$ = H V_i = L		3	7	mA
	I_L = 0 V_i = H		15	20	
	$V_{inh.}$ = L			1	
Quiescent Current from V_{ss} (Pin 9), I_{ss}	$V_{inh.}$ = H V_i = L		5	10	mA
	I_L = 0 V_i = H		1.5	3	
	$V_{inh.}$ = L		1	1.5	
Input Low Voltage (Pins 5, 7, 10, 12), $V_{i\ L}$		-0.3		1.5	V
Input High Voltage (Pins 5, 7, 10, 12), $V_{i\ H}$		2.3		V_{ss}	
Low Voltage Input Current (Pins 5, 7, 10, 12), $I_{i\ L}$	V_i = L			-10	μA
High Voltage Input Current (Pins 5, 7, 10, 12), $I_{i\ H}$	V_i = H		30	100	
Inhibit Low Voltage (Pins 6, 11), $V_{inh.\ L}$		-0.3		1.5	V
Inhibit High Voltage (Pins 6, 11), $V_{inh.\ H}$		2.3		7	
Low Voltage Inhibit Current (Pins 6, 11), $I_{inh.\ L}$	$V_{inh.}$ = L			-10	μA
High Voltage Inhibit Current (Pins 6, 11), $I_{inh.\ H}$	$V_{inh.}$ = H ≤ V_{ss} -0.6V		30	100	
Source Saturation Voltage, $V_{CE\ sat(H)}$	I_L = 1A		1.2	1.8	V
	I_L = 2A		1.8	2.8	
Sink Saturation Voltage, $V_{CE\ sat(L)}$	I_L = 1A		1.2	1.8	V
	I_L = 2A		1.7	2.6	
Total Drop, $V_{CE\ sat}$	I_L = 1A			3.4	V
	I_L = 2A			5.2	
Sensing Voltage (Pins 1, 15), V_{sens}		-1 (1)		2	V
Source Current Turn-Off Delay, $T_1(V_i)$	0.5 V_i to 0.9 I_L (2)		1.7		μs
Source Current Fall Time, $T_2(V_i)$	0.9 I_L to 0.1 I_L (2)		0.2		μs
Source Current Turn-On Delay, $T_3(V_i)$	0.5 V_i to 0.1 I_L (2)		2.5		μs
Source Current Rise Time, $T_4(V_i)$	0.1 I_L to 0.9 I_L (2)		0.35		μs
Sink Current Turn-Off Delay, $T_5(V_i)$	0.5 V_i to 0.9 I_L (3)		0.7		μs
Sink Current Fall Time, $T_6(V_i)$	0.9 I_L to 0.1 I_L (3)		0.2		μs
Sink Current Turn-On Delay, $T_7(V_i)$	0.5 V_i to 0.1 I_L (3)		1.5		μs
Sink Current Rise Time, $T_8(V_i)$	0.1 I_L to 0.9 I_L (3)		0.2		μs
Commutation Frequency, f_c	I_L = 2A		25	40	KHz

1) Sensing voltage can be -1V for t ≤ 50μS; in steady state V_{sens} min ≥ -0.5V.
2) See figure 1a.
3) See figure 2a.

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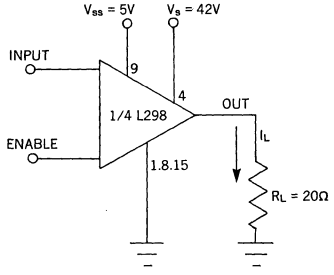
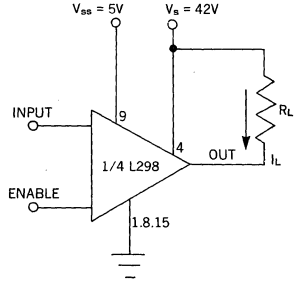
SWITCHING CHARACTERISTICS

Figure 1. Switching times test circuits.



NOTE: For INPUT chopper, set EN = H.

Figure 2. Switching Times Test Circuits.



NOTE: For INPUT chopper, set EN = H.

Figure 1a. Source Current Delay Times vs. Input or Enable Chopper.

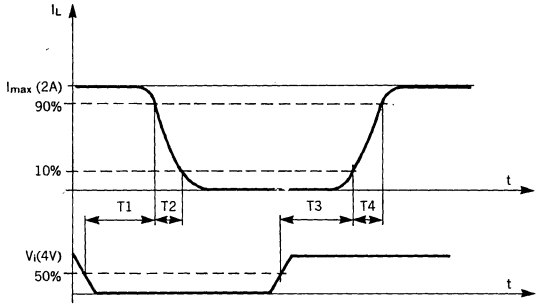
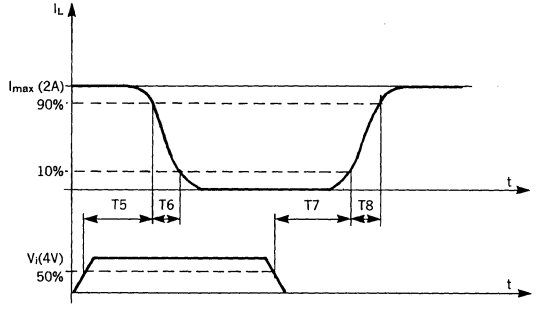
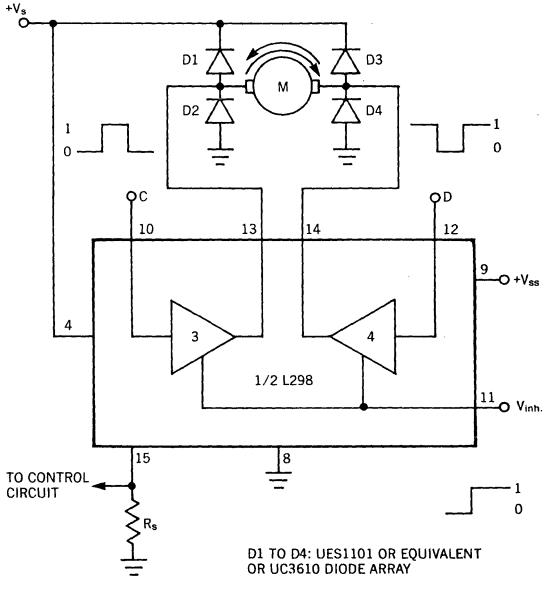


Figure 2a. Sink Current Delay Times vs. Input or Enable Chopper.



APPLICATIONS

Figure 3. Bi-Directional DC Motor Control.



	INPUTS	FUNCTION
$V_{inh.}$ = H	C = H; D = L	Turn right
	C = L; D = H	Turn left
	C = D	Fast motor stop
$V_{inh.}$ = L	C = X; D = C	Free running motor stop

L = Low
H = High
X = Don't Care

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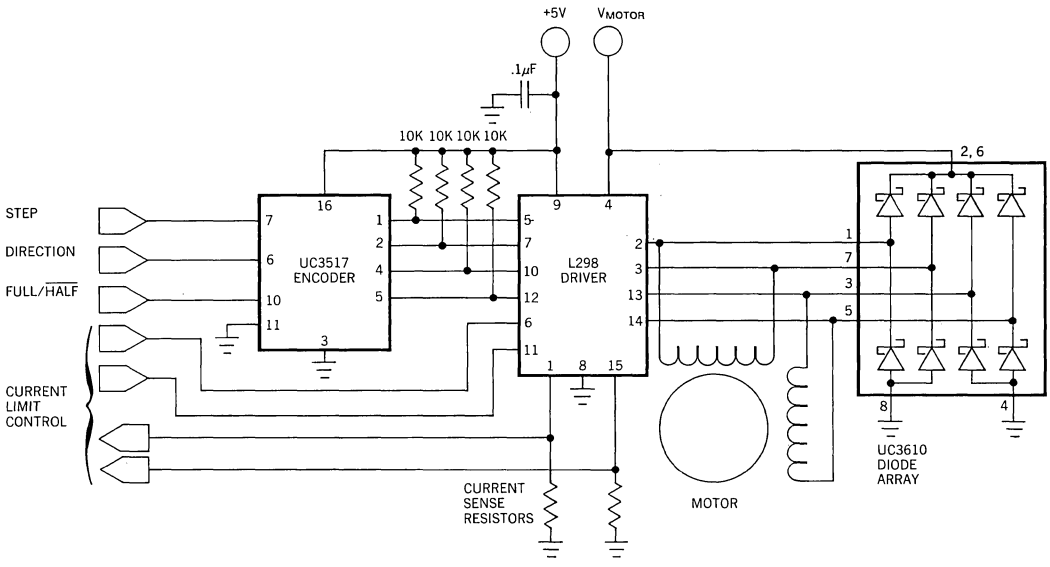
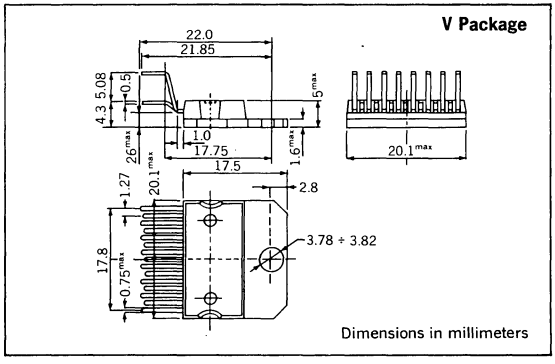
Figure 4. Bipolar Step Motor Driver.



MECHANICAL DATA



LINEAR INTEGRATED CIRCUITS

L298D

Dual Full-Bridge Driver Power

FEATURES

- Operating Supply Voltage up to 46V
- Overtemperature Protected
- Operates in Switched and L/R Current Regulation Modes
- 25W Power-Tab Package for Low Installed Cost
- Individual Logic Inputs for Each Driver
- Channel-Enable Logic Inputs for Driver Pairs
- Internal Diodes Minimize Parts Count

DESCRIPTION

The L298D is a power integrated circuit usable for driving resistive and inductive loads. This device contains four push-pull drivers with separate logic inputs. Two enable inputs are provided for power down and chopping. Each driver is capable of driving loads up to 1A continuously.

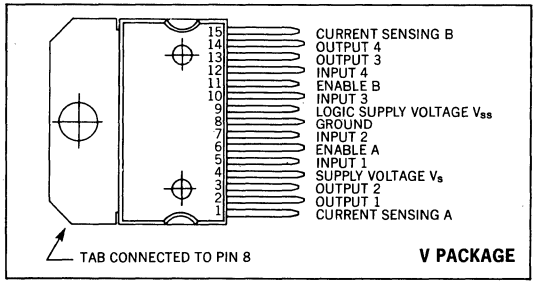
The L298D features internal diodes for clamping output excursions when driving inductive loads, such as motors and transmission lines. For most applications, these diodes can completely replace all external clamp diodes. In certain cases, however, additional output catch diodes may be valuable for reducing recovery time or power dissipation.

Logic inputs to the L298D have high input thresholds (1.85V) and hysteresis to provide trouble-free operation in noisy environments normally associated with motors and inductors. The L298D input currents and thresholds allow the device to be driven by TTL and CMOS systems without buffering or level shifting.

The emitters of the low-side power drivers are available in pairs for current sensing. Feedback from the emitters can be used to control load current in a switching mode, or can be used to detect load faults.

Separate logic and load supply lines are provided to reduce total IC power consumption. Power consumption is reduced further when the enable inputs are low. This makes the L298D ideal for systems that require low standby current, such as portable or battery-operated equipment.

CONNECTION DIAGRAM (TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

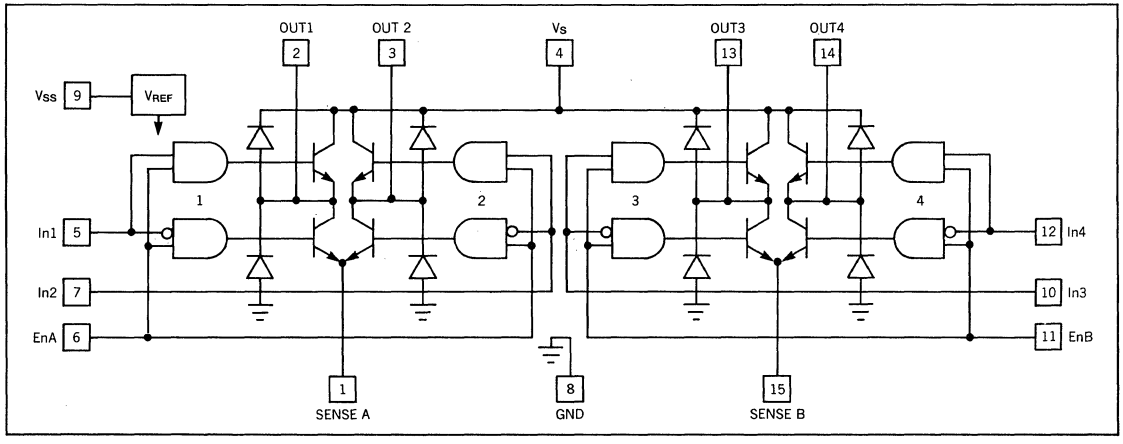
Power Supply, V_s 50V
Logic Supply Voltage, V_{ss} 7V
Input and Enable Voltage, V_i, V_{En} ..... -0.3V to +7V
Peak Output Current (each channel), I_o
- Non-Repetitive (t = 100μs) 1.5A
- Repetitive (80% on - 20% off; t_{ON} = 10ms) 1.2A
- DC Operation 1A

Sensing Voltage, V_{sens} ..... -1V to +2.3V
Total Power Dissipation (T_{case} = 75°C), P_{tot} 25W
Storage and Junction Temperature, T_{stg}, T_j ..... -40°C to +150°C

THERMAL DATA

Thermal Resistance Junction-Case, $R_{th\ j\text{-}case}$ ..... 3°C/W max.
Thermal Resistance Junction-Ambient, $R_{th\ j\text{-}amb}$ ..... 35°C/W max.

BLOCK DIAGRAM



UNITRODE

ELECTRICAL CHARACTERISTICS (for each channel, V_s = 42V, V_{ss} = 5V, T_j = 25°C)

PARAMETERS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage (Pin 4), V_s	Operative Condition	V_{IH}+2.5		46	V
Logic Supply Voltage (Pin 9), V_{ss}		4.5		7	V
Quiescent Supply Current (Pin 4), I_s	V_{En} = H V_i = L		3	7	mA
	I_L = 0 V_i = H		15	20	
	V_{En} = L			1	
Quiescent Current from V_{ss} (Pin 9), I_{ss}	V_{En} = H V_i = L		5	10	mA
	I_L = 0 V_i = H		1.5	3	
	V_{En} = L		1	1.5	
Input Low Voltage (Pins 5, 7, 10, 12), $V_{i\ L}$		-0.3		1.5	V
Input High Voltage (Pins 5, 7, 10, 12), $V_{i\ H}$		2.3		V_{ss}	
Low Voltage Input Current (Pins 5, 7, 10, 12), $I_{i\ L}$	V_i = L			-10	μA
High Voltage Input Current (Pins 5, 7, 10, 12), $I_{i\ H}$	V_i = H		30	100	
Enable Low Voltage (Pins 6, 11), $V_{En\ L}$		-0.3		1.5	V
Enable High Voltage (Pins 6, 11), $V_{En\ H}$		2.3		7	
Low Voltage Enable Current (Pins 6, 11), $I_{En\ L}$	V_{En} = L			-10	μA
High Voltage Enable Current (Pins 6, 11), $I_{En\ H}$	V_{En} = H ≤ V_{ss} -0.6V		30	100	
Source Saturation Voltage, $V_{CE\ sat(H)}$	I_L = 1A		1.2	2.2	V
Sink Saturation Voltage, $V_{CE\ sat(L)}$	I_L = 1A		1.4	2.2	V
Total Drop, $V_{CE\ sat}$	I_L = 1A		2.6	4.2	V
High-Side Diode Voltage, $V_{D(H)}$	I_L = 1A		1.6	2.1	V
Low-Side Diode Voltage, $V_{D(L)}$	I_L = 1A		1.6	2.1	V
Sensing Voltage (Pins 1, 15), V_{sens}		-1 (1)		2	V
Source Current Turn-Off Delay, $T_1(V_i)$	0.5 V_i to 0.9 I_L (2)		1.7		μs
Source Current Fall Time, $T_2(V_i)$	0.9 I_L to 0.1 I_L (2)		0.2		μs
Source Current Turn-On Delay, $T_3(V_i)$	0.5 V_i to 0.1 I_L (2)		2.5		μs
Source Current Rise Time, $T_4(V_i)$	0.1 I_L to 0.9 I_L (2)		0.35		μs
Sink Current Turn-Off Delay, $T_5(V_i)$	0.5 V_i to 0.9 I_L (3)		0.7		μs
Sink Current Fall Time, $T_6(V_i)$	0.9 I_L to 0.1 I_L (3)		0.2		μs
Sink Current Turn-On Delay, $T_7(V_i)$	0.5 V_i to 0.1 I_L (3)		1.5		μs
Sink Current Rise Time, $T_8(V_i)$	0.1 I_L to 0.9 I_L (3)		0.2		μs
Commutation Frequency, f_c	I_L = 1A		25	40	KHz

1) Sensing voltage can be -1V for t ≤ 50μS; in steady state V_{sens} min ≥ -0.5V.
2) See figure 1a.
3) See figure 2a.

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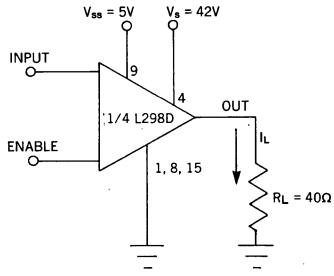
SWITCHING CHARACTERISTICS

Figure 1. Switching times test circuits.



NOTE: For INPUT chopper, set EN = H.

Figure 1a. Source Current Delay Times vs. Input.

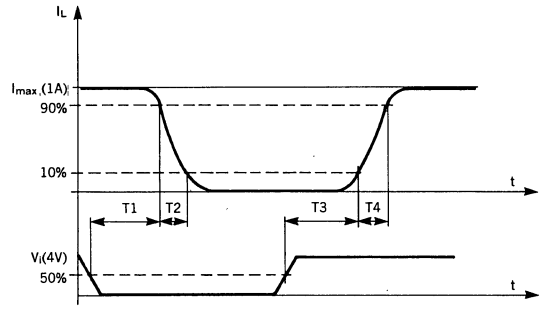
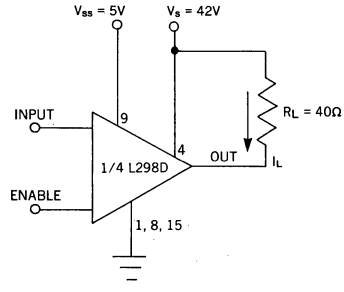
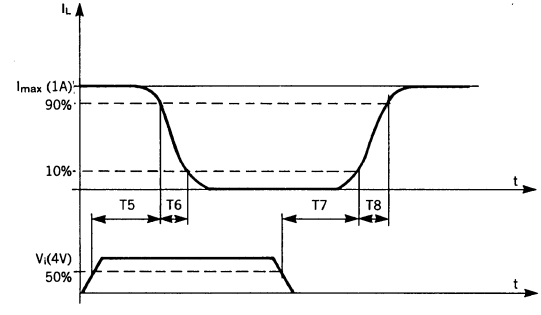


Figure 2. Switching Times Test Circuits.



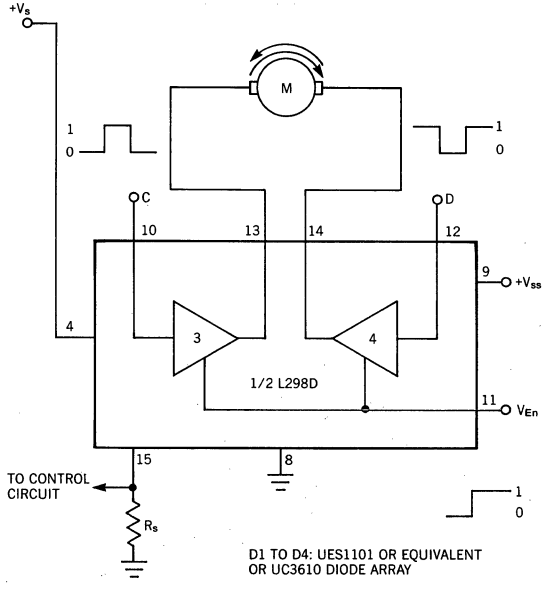
NOTE: For INPUT chopper, set EN = H.

Figure 2a. Sink Current Delay Times vs. Input.



APPLICATIONS

Figure 3. Bi-Directional DC Motor Control.



	INPUTS	FUNCTION
V_{En} = H	C = H; D = L	Turn right
	C = L; D = H	Turn left
	C = D	Fast motor stop
V_{En} = L	C = X; D = C	Free running motor stop

L = Low
H = High
X = Don't Care

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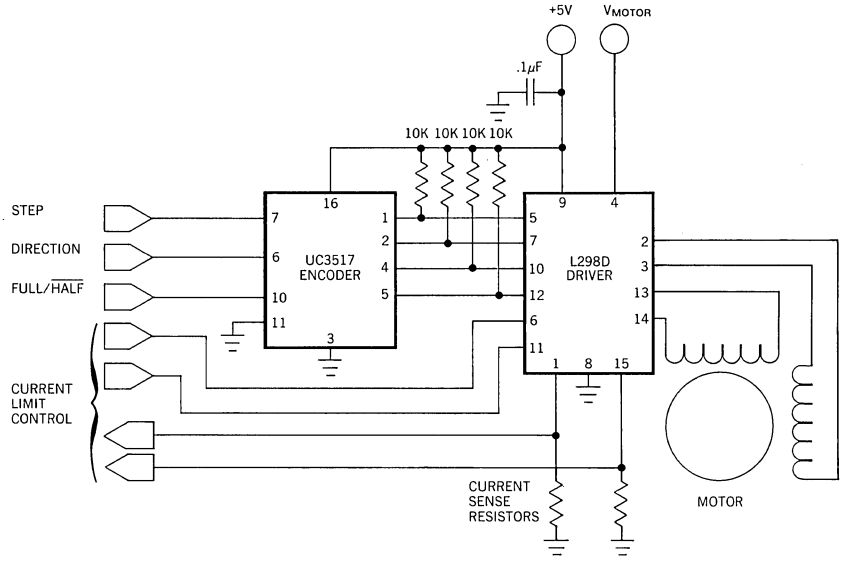
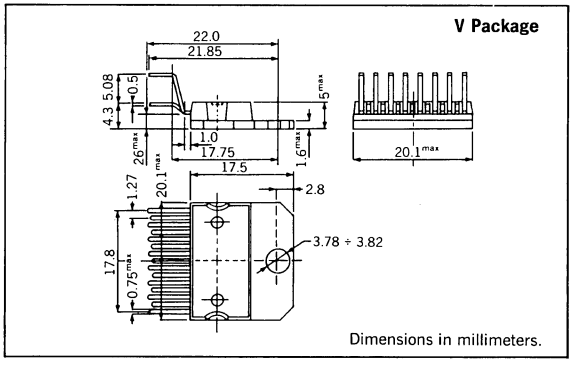
Figure 4. Bipolar Step Motor Driver.



MECHANICAL DATA



LINEAR INTEGRATED CIRCUITS

Stepper Motor Drive Circuit

UC1517
UC3517

FEATURES

- Complete Motor Driver and Encoder
- Continuous Drive Capability 350mA per Phase
- Contains all Required Logic for Full and Half Stepping
- Bilevel Operation for Fast Step Rates
- Operates as a Voltage Doubler
- Useable as a Phase Generator and/or as a Driver
- Power-On Reset Guarantees Safe, Predictable Power-Up
- Monolithic Construction
- 16 Lead Plastic or Hermetic DIL Package

DESCRIPTION

The UC3517 contains four NPN drivers that operate in two-phase fashion for full-step and half-step motor control. The UC3517 also contains two emitter followers, two monostables, phase decoder logic, power-on reset, and low-voltage protection, making it a versatile system for driving small stepper motors or for controlling large power devices.

The emitter followers and monostables in the UC3517 are configured to apply higher-voltage pulses to the motor at each step command. This drive technique, called "**Bilevel**," allows faster stepping than common resistive current limiting, yet generates less electrical noise than chopping techniques.

ORDERING INFORMATION

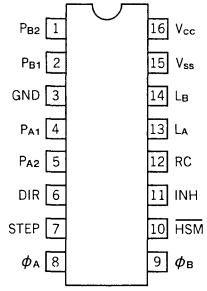
	Operating Temperature Range
UC1517J, CERDIP	-55°C to +125°C
UC3517J, CERDIP	0°C to +70°C
UC3517N, Plastic Package	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

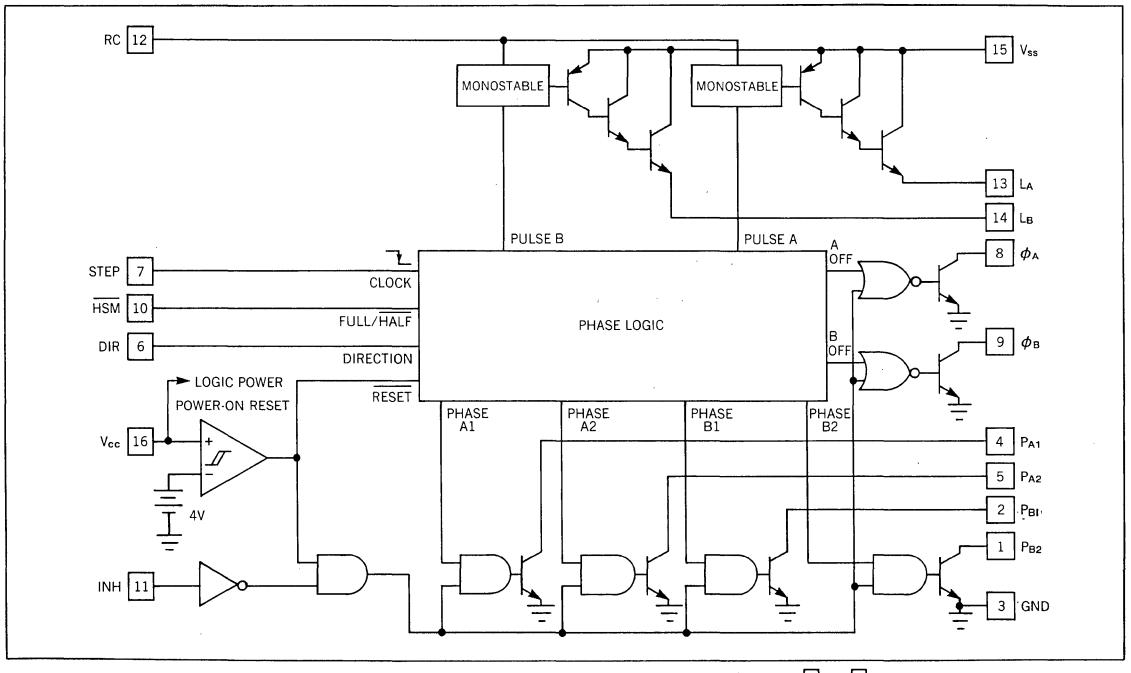
Second Level Supply, V_{ss} 40V
Phase Output Supply, V_{mm} 40V
Logic Supply, V_{cc} 7V
Logic Input Voltage, V_{in} ..... -.3V to +7V
Logic Input Current, I_{in} ..... ±10mA
Output Current, Each Phase, I_{phase} 500mA
Output Current, Emitter Follower, I_{second} ..... -500mA
Power Dissipation, 50°C, CERDIP, P_{diss} 1W
Derate 10mW/°C Above 50°C
Power Dissipation, 25°C, Plastic Package, P_{diss} 2W
Derate 10mW/°C above 25°C
Junction Temperature, T_{junct} ..... 150°C
Ambient Temperature, UC1517, $T_{ambient}$ ..... -55°C to +125°C
Ambient Temperature, UC3517, $T_{ambient}$ ..... 0°C to +70°C
Storage Temperature, $T_{storage}$ ..... -55°C to +150°C

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



BLOCK DIAGRAM



UNITRODE

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1517 and 0°C to +70°C for the UC3517; V_{cc} = 5V; V_{ss} = 20V.)

PARAMETER	TEST CONDITIONS	UC1517 UC3517			UNITS
		MIN.	TYP.	MAX.	
Logic Supply, V_{cc}	Pin 16	4.75		5.25	V
Second Supply, V_{ss}	Pin 15	10		40	V
Logic Supply Current	V_{INH} = 0.4V		45	60	mA
Logic Supply Current	V_{INH} = 4.0V		12		mA
Input Low Voltage	Pins 6, 7, 10, 11			0.8	V
Input High Voltage	Pins 6, 7, 10, 11	2.0			V
Input Low Current	Pins 6, 7, 10, 11; V = 0V			−400	μA
Input High Current	Pins 6, 7, 10, 11; V = 5V			20	μA
Phase Output Saturation Voltage	Pins 1, 2, 4, 5; I = 350mA		0.6	0.85	V
Phase Output Leakage Current	Pins 1, 2, 4, 5; V = 39V			500	μA
Follower Saturation Voltage to V_{ss}	Pins 13, 14; I = 350mA			−2	V
Follower Leakage Current	Pins 13, 14; V = 0V			500	μA
Output Low Voltage, ϕ_A, ϕ_B	Pins 8, 9; I = 1.6mA		0.1	0.4	V
Phase Turn-On Time	Pins 1, 2, 4, 5		2		μS
Phase Turn-Off Time	Pins 1, 2, 4, 5		1.8		μS
Second-Level On Time, t_{mono}	Pins 13, 14; Figure 3 Test Circuit	275	325	375	μS
Logic Input Set-Up Time, t_s	Pins 6, 10; Figure 4	400			nS
Logic Input Hold Time, t_h	Pins 6, 10; Figure 4	0			nS
STEP Pulse Width, t_p	Pin 7; Figure 4	800			nS
Timing Resistor Value	Pin 12	1K		100K	Ω
Timing Capacitor Value	Pin 12	0.1		500	nF
Power-On Threshold	Pin 16		4.3		V
Power-Off Threshold	Pin 16		3.8		V
Power Hysteresis	Pin 16		0.5		V

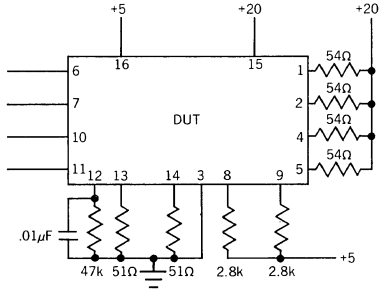


Figure 3. Test Circuit

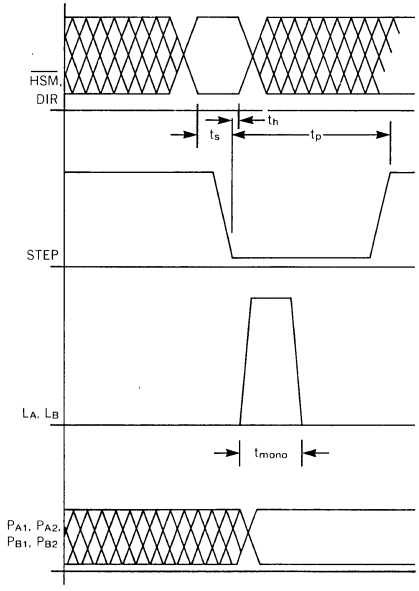


Figure 4. Timing Waveforms

UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • TELEX 95-3040

PIN DESCRIPTIONS

V_{cc}: V_{cc} is the UC3517's logic supply. Connect to a regulated 5VDC, and bypass with a 0.1μF ceramic capacitor to absorb switching transients.

V_{mm}: V_{mm} is the primary motor supply. It connects to the UC3517 phase outputs through the motor windings. Limit this supply to less than 40V to prevent breakdown of the phase output transistors. Select the nominal V_{mm} voltage for the desired continuous winding current.

V_{ss}: V_{ss} is the secondary motor supply. It drives the L_A and L_B outputs of the UC3517 when a monostable in the UC3517 is active. In the bilevel application, this supply is applied to the motor to charge winding inductance faster than the primary supply could. Typically, V_{ss} is higher in voltage than V_{mm}, although V_{ss} must be less than 40V. The V_{ss} supply should have good transient capability.

GROUND: The ground pin is the common reference for all supplies, inputs, and outputs.

RC: RC controls the timing functions of the monostables in the UC3517. It is normally connected to a resistor (R_T) and a capacitor (C_T) to ground, as shown in Figure 3. Monostable on time is determined by the formula: $T_{ON} \approx 0.69\ R_T\ C_T$. To keep the monostable on indefinitely, pull RC to V_{cc} through a 50k resistor. The UC3517 contains only one RC pin for two monostables. If step rates comparable to T_{ON} are commanded, incorrect pulsing can result, so consider maximum step rates when selecting R_T and C_T. Keep $T_{ON} \leq T_{STEP\ MAX}$.

ϕ_A and ϕ_B: These logic outputs indicate half-step position. These outputs are open-collector, low-current drivers, and may directly drive TTL logic. They can also drive CMOS logic if a pull-up resistor is provided. Systems which use the UC3517 as an encoder and use a different driver can use these outputs to disable the external driver, as shown in Figure 8. The sequencing of these outputs is shown in Figure 5.

P_{A1}, P_{A2}, P_{B1}, and P_{B2}: The phase outputs pull to ground sequentially to cause motor stepping, according to the state diagram of Figure 5. The sequence of stepping on these lines, as with the L_A and L_B lines is controlled by the STEP input, the DIR input, and the $\overline{HSM}$ input. Caution: If these outputs or any other IC pins are pulled too far below ground either continuously or in a transient, step memory can be lost. It is recommended that these pins be clamped to ground and supply with high-speed diodes when driving inductive loads such as motor windings or solenoids. This clamping is very important because one side of the winding can "kick" in a direction opposite the swing of the other side.

L_A and L_B: These outputs pull to V_{ss} when their corresponding monostable is active, and will remain high until the monostable on time elapses. Before and after, these outputs are high-impedance. For detailed timing information, consult Figure 5.

STEP: This logic input clocks the logic in the UC3517 on every falling edge. Like all other UC3517 inputs, this input is TTL/CMOS compatible, and should not be pulled below ground.

DIR: This logic input controls the motor rotation direction by controlling the phase output sequence as shown in Figure 5. This signal must be stable 400nS before a falling edge on STEP, and must remain stable through the edge to insure correct stepping.

$\overline{HSM}$: This logic input switches the UC3517 between half-stepping ($\overline{HSM}$ = low) and full-stepping ($\overline{HSM}$ = high) by controlling the phase output sequence as shown in Figure 5. This line requires the same set-up time as the DIR input, and has the same hold requirement.

INH: When the inhibit input is high, the phase and ϕ outputs are inhibited (high-impedance). STEP pulses received while inhibited will continue to update logic in the IC, but the states will not be reflected at the outputs until inhibit is pulled low. In stepper motor systems, this can be used to save power or to allow the rotor to move freely for manual repositioning.

OPERATING MODES

The UC3517 is a system component capable of many different operating modes, including:

Unipolar Stepper Driver: In its simplest form, the UC3517 can be connected to a stepper motor as a unipolar driver. L_A, L_B, RC and V_{ss} are not used, and may be left open. All other system design considerations mentioned above apply, including choice of motor supply V_{mm}, undershoot diodes, and timing considerations.

Unipolar Bilevel Stepper Driver: If increased step rates are desired, the application circuit of Figure 6 makes use of the monostables and emitter followers as well as the configuration mentioned above to provide high-voltage pulses to the motor windings when any phase is turned on. For a given dissipation level, this mode offers faster step rates, and very little additional electrical noise.

The choice of monostable components can be estimated based on the timing relationship of motor current and voltage: $V = L dI/dt$. Assuming a fixed secondary supply voltage (V_{ss}), a fixed winding inductance (L_m), a desired winding peak current (I_w), and no back EMF from the motor, we can estimate that $R_T\ C_T = 1.449\ I_w L_m / V_{ss}$. In practice, these calculations should be confirmed and adjusted to accommodate for effects not modeled.

Voltage-Doubler Mode: The UC3517 can also be used to generate higher voltages than available with system power supplies using capacitors and diodes. Figure 9 shows how this might be done, and gives some estimates for component values.

Higher-Current Operation: For systems requiring more than 350mA of drive per phase the UC3517 can be used in conjunction with discrete power transistors or power driver ICs, like the L298. These can be connected as current gain devices that turn on when the phase outputs turn on.

Bipolar Motor Driver: Bipolar motors can be controlled by the UC3517 with the addition of bipolar integrated drivers such as the UC3717A (Figure 8) and the L298, or discrete devices. Care should be taken with discrete devices to avoid potential cross-conduction problems.

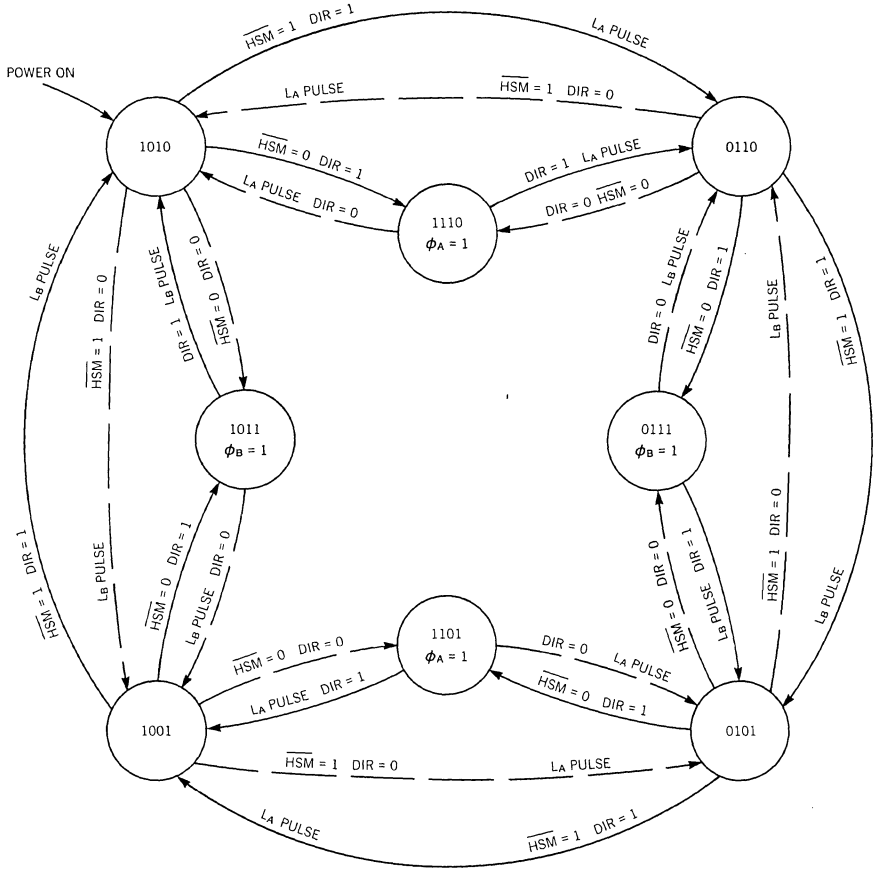


Figure 5. Logic Flow Graph

LOGIC FLOW GRAPH

The UC3517 contains a bidirectional counter which is decoded to generate the correct phase and ϕ outputs. This counter is incremented on every falling edge of the STEP input. Figure 5 shows a graph representing the counter sequence, inputs that determine the next state (DIR and $\overline{HSM}$), and the outputs at each state. Each circle represents a unique logic state, and the four inside circles represent the half-step states.

The four bits inside the circles represent the phase outputs in each state (P_{A1}, P_{A2}, P_{B1}, and P_{B2}). For example, the circle labeled 1010 is immediately entered when the device is powered up, and represents P_{A1} off ("1" or high), P_{A2} on ("0" or low), P_{B1} off ("1" or high), and P_{B2} on ("0" or low). The ϕ_A and ϕ_B outputs are both low (unidentified).

The arrows in the graph show the state changes. For example, if the IC is in state 0110, DIR is high, $\overline{HSM}$ is high, and STEP falls, the next state will be 0101, and a pulse will be generated on the L_B line by the monostable.

Inhibit will not effect the logic state, but it will cause all phase outputs and both ϕ outputs to go high (off). A falling edge on STEP will still cause a state change, but inhibit will have to toggle low for the state to be apparent.

A falling edge on STEP with $\overline{HSM}$ high will cause the counter to advance to the next full step state regardless of whether or not it was in a full step state previously.

No L_A or L_B pulses are generated entering half-states.

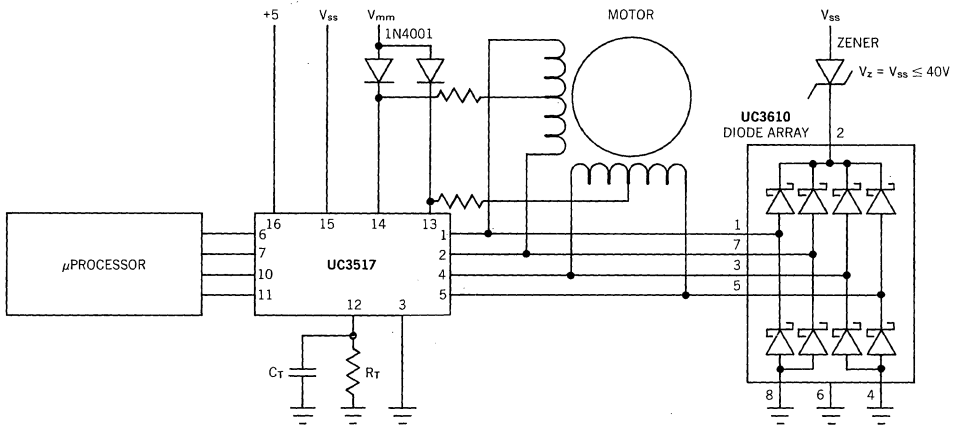


Figure 6. Bilevel Motor Driver

For applications requiring very fast step rates, a zener diode permits windings to discharge at higher voltages, and higher rates. Driver transistor breakdown must be considered when selecting V_{ss} and zener voltage to insure that the outputs will not overshoot past 40V. If the zener diodes are not used and UC3610 pin 2 is connected directly to V_{ss}, then higher V_{ss} can be used.

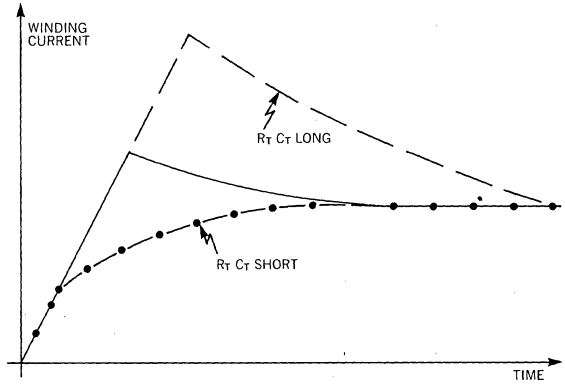


Figure 7. Effects of Different R_T & C_T on Bilevel Systems

Experimental selection of R_T and C_T allow the designer to select a small amount of winding current overshoot, as shown above. Although the overshoot may exceed the continuous rated current of the winding and the drive transistors, the duration can be well controlled. Average power dissipation for the driver and motor must be considered when designing systems with intentional overshoot, and must stay within conservative limits for short duty cycles.

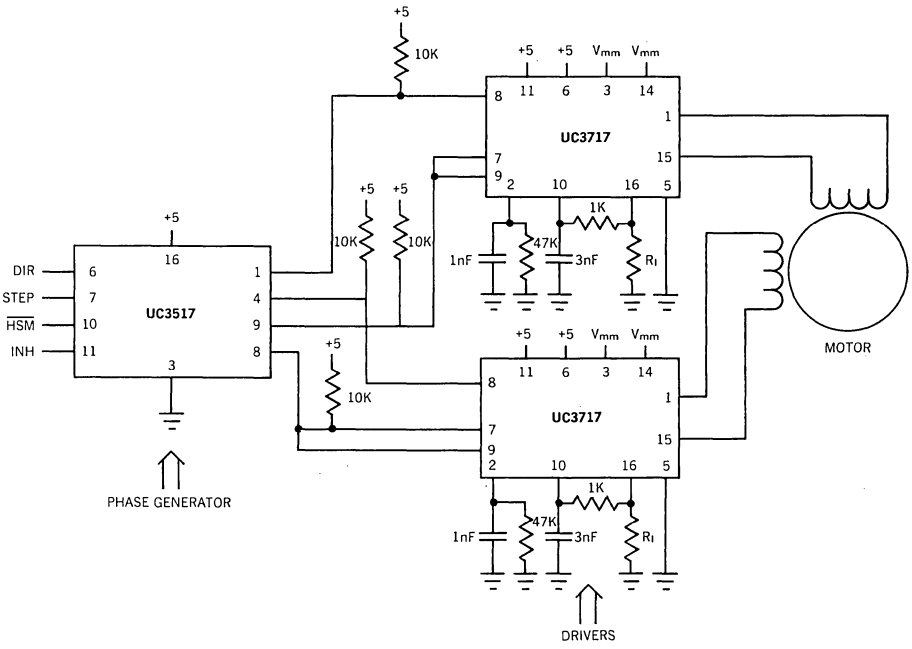


Figure 8. Interface to UC3717 Bipolar Driver

In this application, the ϕ_A and ϕ_B outputs of the UC3517 are connected to the current program inputs of the UC3717. This allows the UC3517 inhibit signal to inhibit the UC3717, and also allows half-step operation of the UC3717. Peak motor winding current will be limited to approximately $.42V/R_I$ by chopping.

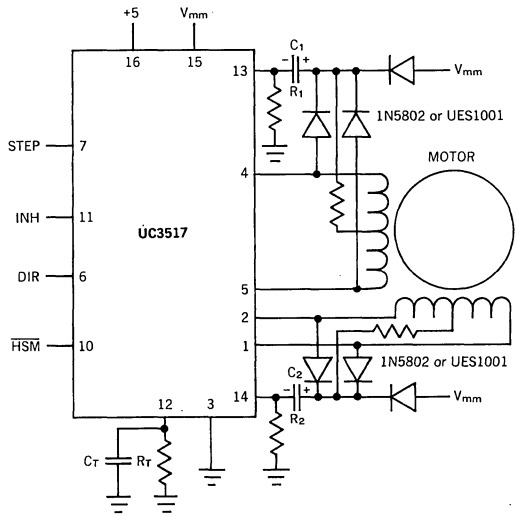


Figure 9. Using the UC3517 as a Voltage Doubler

Although component values can be best optimized experimentally, good starting values speed development. For this design, start with:

$R_T C_T = 3 L_W/R_W$
$C_1 = C_2 = L_W I_r/R_W$
$R_1 = R_2 = 2.9 T_{min}/C_1$

where:
L_W is winding inductance,
R_W is winding resistance,
I_r is rated winding current, and
T_{min} is minimum step period expected.

UNITRODE INTEGRATED CIRCUITS

UC1610
UC3610

DUAL Schottky Diode Bridge

FEATURES

- Monolithic Eight-Diode Array
- Exceptional Efficiency
- Low Forward Voltage
- Fast Recovery Time
- High Peak Current
- Small Size

DESCRIPTION

This eight-diode array is designed for high-current, low duty-cycle applications typical of flyback voltage clamping for inductive loads. The dual bridge connection makes this device particularly applicable to bipolar driven stepper motors.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

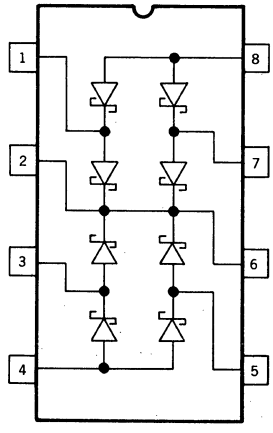
This single monolithic chip is fabricated in both hermetic cerdip and copper-leaded plastic minidip packages. The UC1610 in ceramic is designed for −55°C to +125°C environments but with reduced peak current capability; while the UC3610 in plastic has higher current rating over a 0°C to 70°C ambient temperature range.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage (per diode) 50V
Peak Forward Current
  UC1610 ..... 1A
  UC3610 ..... 3A
Power Dissipation at T_A = 70°C 1W
  Derate 12.5mW/°C above 70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

CONNECTION DIAGRAM

DIL-8 (TOP VIEW)
N or J PACKAGE



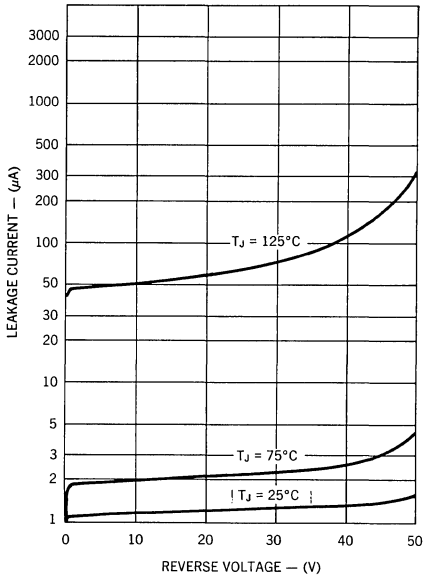
UNITRODE

ELECTRICAL CHARACTERISTICS (All specifications apply to each individual diode. T_J = 25°C except as noted.)

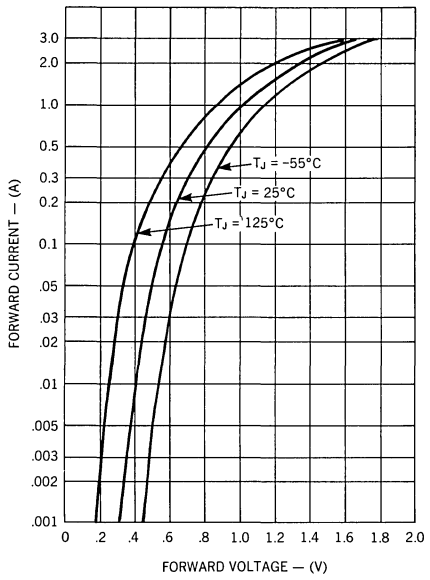
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Forward Voltage Drop	I_F = 100mA I_F = 1A	0.4 0.8	0.5 1.0	0.7 1.3	V
Leakage Current	V_R = 40V V_R = 40V, T_J = 100°C		.01 0.1	0.1 1.0	mA
Reverse Recovery	.5A Forward to .5A Reverse		15		nSec
Forward Recovery	1A Forward to 1.1V Recovery		30		nSec
Junction Capacitance	V_R = 5V		70		pF

Note: At forward currents of greater than 1.0A, a parasitic current of approximately 10mA may be collected by adjacent diodes.

Reverse Current vs Voltage



Forward Voltage vs Current



4

LINEAR INTEGRATED CIRCUITS

Phase Locked Frequency Controller

UC1633
UC2633
UC3633

FEATURES

- Precision Phase Locked Frequency Control System
- Crystal Oscillator
- Programmable Reference Frequency Dividers
- Phase Detector with Absolute Frequency Steering
- Digital Lock Indicator
- Double Edge Option on the Frequency Feedback Sensing Amplifier
- Two High Current Op-Amps
- 5V Reference Output

DESCRIPTION

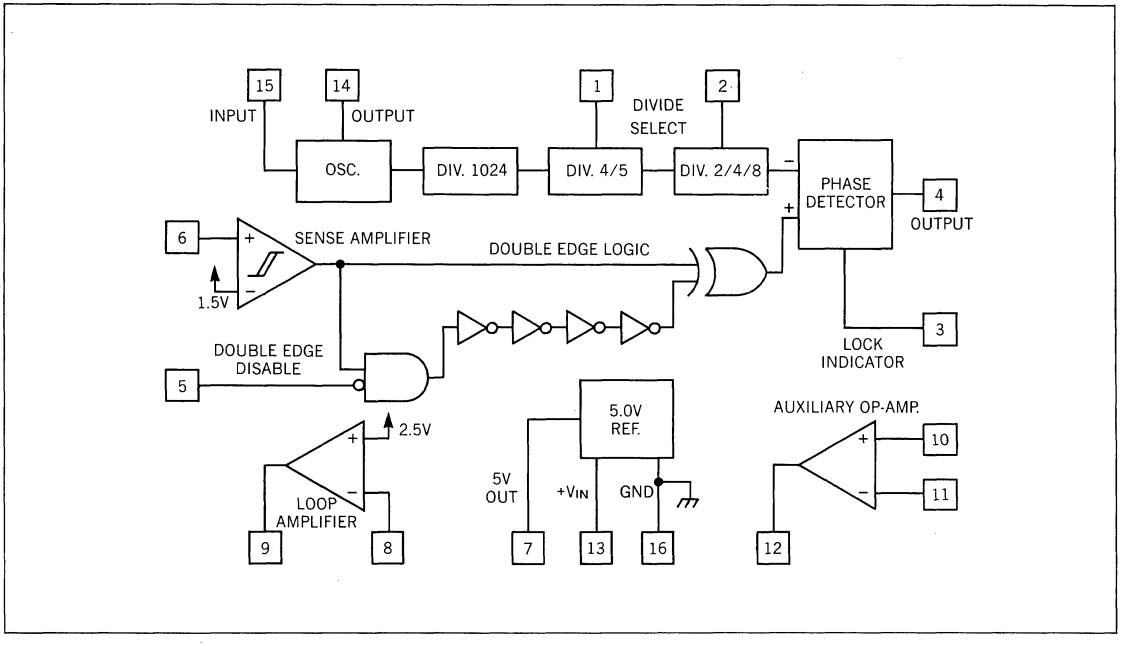
The UC1633 family of integrated circuits was designed for use in phase locked frequency control loops. While optimized for precision speed control of DC motors, these devices are universal enough for most applications that require phase locked control. A precise reference frequency can be generated using the device's high frequency oscillator and programmable frequency dividers. The oscillator operates using a broad range of crystals, or, can function as a buffer stage to an external frequency source.

The phase detector on these integrated circuits compares the reference frequency with a frequency/phase feedback signal. In the case of a motor, feedback is obtained at a hall output or other speed detection device. This signal is buffered by a sense amplifier that squares up the signal as it goes into the digital phase detector. The phase detector responds proportionally to the phase error between the reference and the sense amplifier output. This phase detector includes absolute frequency steering to provide maximum drive signals when any frequency error exists. This feature allows optimum start-up and lock times to be realized.

Two op-amps are included that can be configured to provide necessary loop filtering. The outputs of these op-amps will source or sink in excess of 16mA, so they can provide a low impedance control signal to driving circuits.

Additional features include a double edge option on the sense amplifier that can be used to double the loop reference frequency for increased loop bandwidths. A digital lock signal is provided that indicates when there is zero frequency error, and a 5V reference output allows DC operating levels to be accurately set.

BLOCK DIAGRAM



UNITRODE

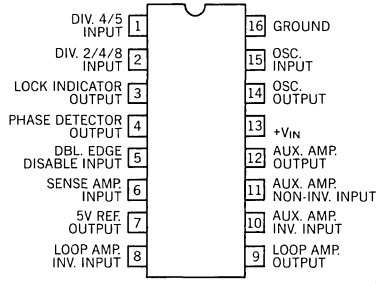
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage ($+V_{IN}$) ..... +20V
Reference Output Current ..... -30mA
Op-Amp Output Currents ..... ±30mA
Op-Amp Input Voltages ..... -.3V to +20V
Phase Detector Output Current ..... ±10mA
Lock Indicator Output Current ..... +15mA
Lock Indicator Output Voltage ..... +20V
Divide Select Input Voltages ..... -.3V to +10V
Double Edge Disable Input Voltage ..... -.3V to +10V
Oscillator Input Voltage ..... -.3V to +5V
Sense Amplifier Input Voltage ..... -.3V to +20V
Power Dissipation at T_A = 25°C 1000mW
Derate at 10mW/°C above 25°C
Power Dissipation at T_C = 25°C 2000mW
Derate at 16mW/°C above 25°C
Thermal Resistance Junction to Ambient ..... 100°C/W
Thermal Resistance Junction to Case ..... 60°C/W
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note: 1. Voltages are referenced to ground, (Pin 16). Currents are positive into, negative out of, the specified terminals.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



4

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, specifications hold for T_A = 0°C to +70°C for the UC3633, -25°C to +85°C for the UC2633 and -55°C to +125°C for the UC1633, $+V_{IN}$ = 12V.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$+V_{IN}$ = 15V		20	28	mA
Reference					
Output Voltage (V_{REF})		4.75	5.0	5.25	V
Load Regulation	I_{OUT} = 0 to 7mA		5.0	20	mV
Line Regulation	$+V_{IN}$ = 8 to 15V		2.0	20	mV
Short Circuit Current	V_{OUT} = 0V	12	30		mA
Oscillator					
DC Voltage Gain	Oscillator Input to Oscillator Output	12	16	20	dB
Input DC Level (V_{IB})	Oscillator Input Pin Open, T_J = 25°C	1.15	1.3	1.45	V
Input Impedance (Note 2)	$V_{IN} = V_{IB} \pm 0.5V$, T_J = 25°C	1.3	1.6	1.9	kΩ
Output DC Level	Oscillator Input Pin Open, T_J = 25°C	1.2	1.4	1.6	V
Maximum Operating Frequency		10			MHz
Dividers					
Maximum Input Frequency	Input = $1V_{PP}$ at Oscillator Input	10			MHz
Div. 4/5 Input Current	Input = 5V (Div. by 4)		150	500	μA
	Input = 0V (Div. by 5)	-5.0	0.0	5.0	μA
Div. 4/5 Threshold		0.5	1.6	2.2	V
Div. 2/4/8 Input Current	Input = 5V (Div. by 8)		150	500	μA
	Input = 0V (Div. by 2)	-500	-150		μA
Div. 2/4/8 Open Circuit Voltage	Input Current = 0μA (Div. by 4)	1.5	2.5	3.5	V
Div. by 2 Threshold		0.35	0.8		V
Div. by 4 Threshold		1.5		3.5	V
Div. by 8 Threshold	Volts Below V_{REF}	0.35	0.8		V

Note: 2. These impedance levels will vary with T_J at about 1700ppm/°C.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, specifications hold for T_A = 0°C to +70°C for the UC3633, −25°C to +85°C for the UC2633 and −55°C to +125°C for the UC1633, $+V_{IN}$ = 12V.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Sense Amplifier					
Threshold Voltage	Percent of V_{REF}	27	30	33	%
Threshold Hysteresis			10		mV
Input Bias Current	Input = 1.5V	−1.0	−0.2		μA
Double Edge Disable Input					
Input Current	Input = 5V (Disabled)		150	500	μA
	Input = 0V (Enabled)	−5.0	0.0	5.0	μA
Threshold Voltage		0.5	1.6	2.2	V
Phase Detector					
High Output Level	Positive Phase/Freq. Error, Volts Below V_{REF}		0.2	0.5	V
Low Output Level	Negative Phase/Freq. Error		0.2	0.5	V
Mid Output Level	Zero Phase/Freq. Error, Percent of V_{REF}	47	50	53	%
High Level Maximum Source Current	V_{OUT} = 4.3V	2.0	8.0		mA
Low Level Maximum Sink Current	V_{OUT} = 0.7V	2.0	5.0		mA
Mid Level Output Impedance (Note 2)	I_{OUT} = −200 to +200μA, T_J = 25°C	4.5	6.0	7.5	kΩ
Lock Indicator Output					
Saturation Voltage	Freq. Error, I_{OUT} = 5mA		0.3	0.45	V
Leakage Current	Zero Freq. Error, V_{OUT} = 15V		0.1	1.0	μA
Loop Amplifier					
NON INV. Reference Voltage	Percent of V_{REF}	47	50	53	%
Input Bias Current	Input = 2.5V	−0.8	−0.2		μA
AVOL		60	75		dB
PSRR	$+V_{IN}$ = 8 to 15V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA
Auxiliary Op-Amp					
Input Offset Voltage	V_{CM} = 2.5V			8	mV
Input Bias Current	V_{CM} = 2.5V	−0.8	−0.2		μA
Input Offset Current	V_{CM} = 2.5V		.01	0.1	μA
AVOL		70	120		dB
PSRR	$+V_{IN}$ = 8 to 15V	70	100		dB
CMRR	V_{CM} = 0 to 10V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA

Note: 2. These impedance levels will vary with T_J at about 1700ppm/°C.

APPLICATION AND OPERATION INFORMATION

Determining The Oscillator Frequency

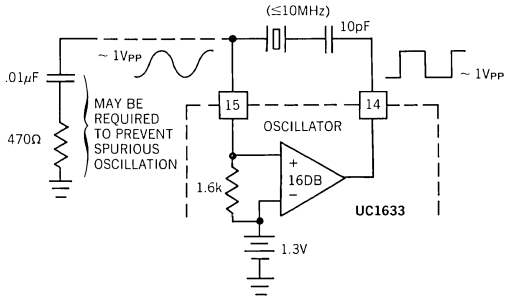
The frequency at the oscillator is determined by: the desired RPM of the motor, the divide ratio selected, the number of poles in the motor, and the state of the double edge select pin.

f_{OSC}(Hz) = (Divide Ratio) · (Motor RPM) · (1/60 SEC/MIN) ·

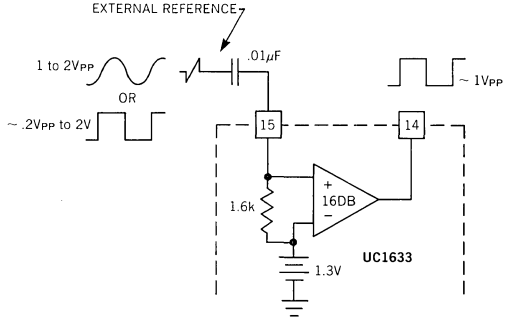
(No. of Rotor Poles/2) · (× 2 if Pin 5 Low)

The resulting reference frequency appearing at the phase detector inputs is equal to the oscillator frequency divided by the selected divide ratio. If the double edge option is used, (Pin 5 low), the frequency of the sense amplifier input signal is doubled by responding to both the rising and falling edges of the input signal. Using this option the loop reference frequency can be doubled for a given motor RPM.

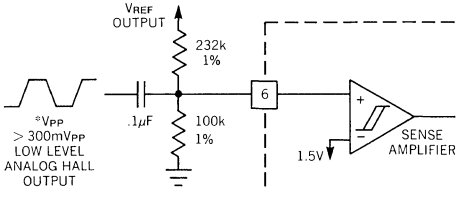
Recommended Oscillator Configuration Using AT Cut Quartz Crystal



External Reference Frequency Input



Method For Deriving Rotation Feedback Signal From Analog Hall Effect Device



*This signal may require filtering if chopped mode drive scheme is used.

APPLICATION AND OPERATION INFORMATION

Phase Detector Operation

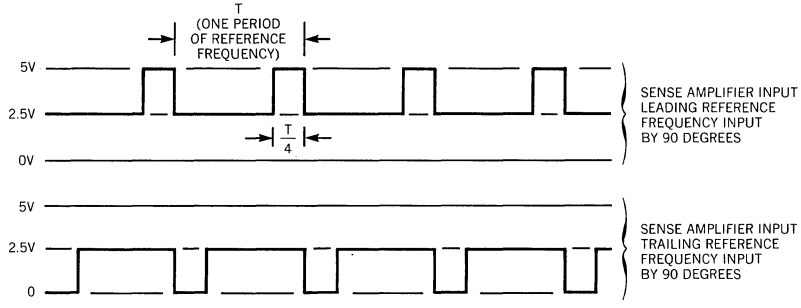
The phase detector on these devices is a digital circuit that responds to the rising edges of the detector's two inputs. The phase detector output has three states: a high, 5V state, a low, 0V state, and a middle, 2.5V state. In the high and low states the output impedance of the detector is low, the middle state output impedance is high, typically 6.0kΩ. When there is any static frequency difference between the inputs the detector output is fixed at its high level if the +input (the sense amplifier signal) is greater in frequency, and fixed at its low level if the −input (the reference frequency signal) is greater in frequency.

When the frequencies of the two inputs to the detector are equal the phase detector switches between its middle state and either the high or low states, depending on the relative phase of the two signals. If the +input is leading in phase then, during each period of the input frequency, the detector output will be high for a time equal to the time difference between the rising edges of the inputs, and will be at its middle level the remainder of the period. If the phase relationship is reversed then the detector will go low for a time proportional to the phase difference of the inputs. The resulting gain of the phase detector, $K\phi$, is $5V/4\pi$ radians, or about 0.4V/radian. The dynamic range of the detector is $\pm 2\pi$ radians.

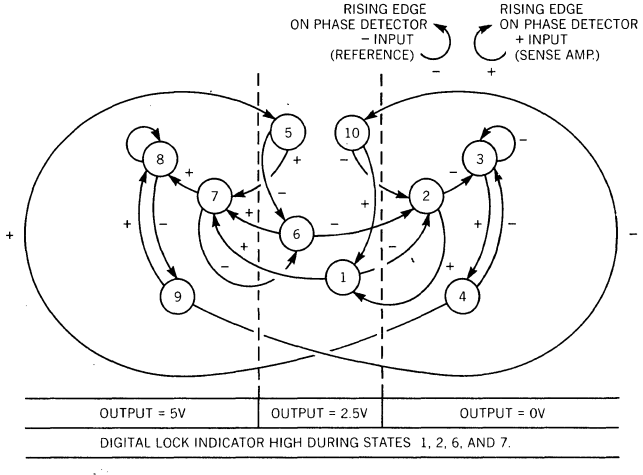
The operation of the phase detector is illustrated in the figures below. The upper figure shows typical voltage waveforms seen at the detector output for leading and lagging phase conditions. The lower figure is a state diagram of the phase detector logic. In this figure, the circles represent the 10 possible states of the logic and the connecting arrows the transition events/paths to and from these states. Transition arrows that have a clockwise rotation are the result of a rising edge on the +input, and conversely, those with counter-clockwise rotation are tied to the rising edge on the −input signal.

The normal operational states of the logic are 6 and 7 for positive phase error, 1 and 2 for a negative phase error. States 8 and 9 occur during positive frequency error, 3 and 4 during negative frequency error. States 5 and 10 occur only as the inputs cross over from a frequency error to a normal phase error only condition. The level of the phase detector output is determined by the logic state as defined in the state diagram figure. The lock indicator output is high, off, when the detector is in states 1, 2, 6, or 7.

TYPICAL PHASE DETECTOR OUTPUT WAVEFORMS

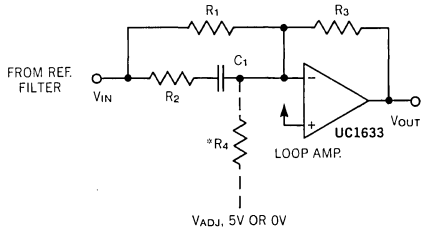


PHASE DETECTOR STATE DIAGRAM



APPLICATION AND OPERATION INFORMATION

Suggested Loop Filter Configuration



$$\frac{\nu_{OUT}}{\nu_{IN}}(s) = \frac{R_3}{R_1} \cdot \frac{1 + s/\omega_Z}{1 + s/\omega_P}$$

$$\omega_P = \frac{1}{R_2 C_1}$$

$$\omega_Z = \frac{1}{(R_1 + R_2)\, C_1}$$

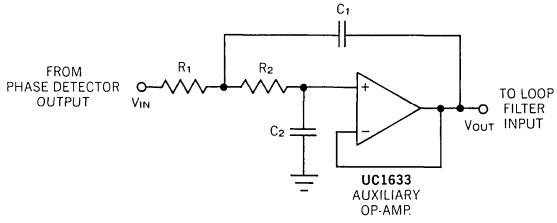
* The static phase error of the loop is easily adjusted by adding resistor, R_4, as shown. To lock at zero phase error R_4 is determined by:

$$R_4 = \frac{2.5V \cdot R_3}{|\Delta V_{OUT}|}$$

Where: $|\Delta V_{OUT}| = |V_{OUT} - 2.5V|$
and V_{OUT} = DC Operating Voltage At Loop Amplifier Output During Phase Lock

If: $(V_{OUT} - 2.5) > 0$ R_4 Goes To 0V
$(V_{OUT} - 2.5) < 0$ R_4 Goes To 5.0V

Reference Filter Configuration



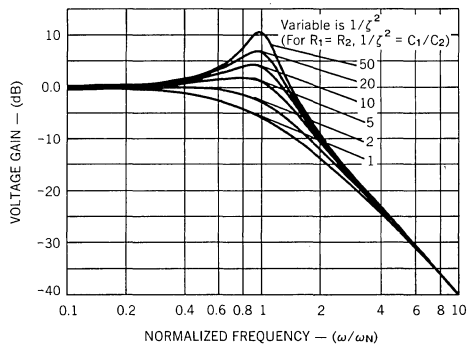
$$\frac{\nu_{OUT}}{\nu_{IN}}(s) = \frac{1}{1 + \frac{s2\zeta}{\omega_N} + \frac{s^2}{\omega_N^2}}$$

$$\omega_N = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

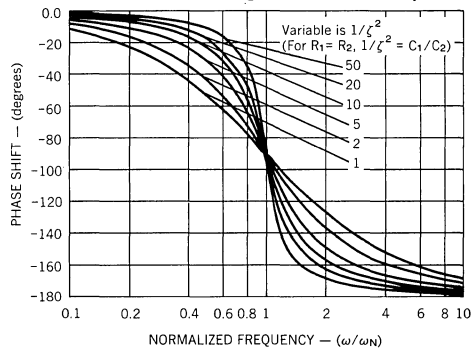
$$\zeta = \frac{1}{2Q} = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}\ \frac{R_1 + R_2}{\sqrt{R_1 R_2}}$$

Note: with $R_1 = R_2$, $\zeta = \sqrt{\frac{C_2}{C_1}}$

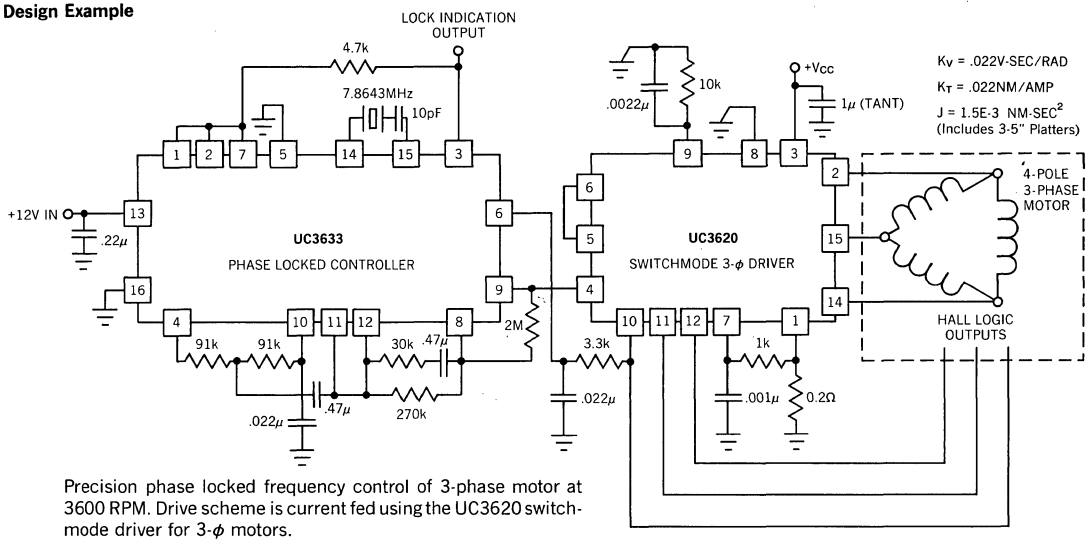
Reference Filter Design Aid — Gain Response



Reference Filter Design Aid — Phase Response

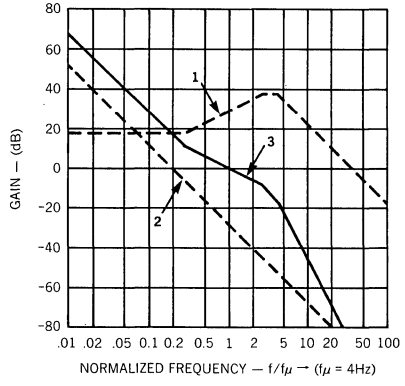


Design Example



Precision phase locked frequency control of 3-phase motor at 3600 RPM. Drive scheme is current fed using the UC3620 switch-mode driver for 3-ϕ motors.

Bode Plots — Design Example Open Loop Response



1 — $K_{LF}(s) \cdot K_{RF}(s)$

2* — $\dfrac{N \cdot K\phi \cdot G_{PD} \cdot K_T}{s^2 \cdot J}$

3 — Combined Overall Open Loop Response

Where:

$K_{LF}(s)$ = Loop Filter Response

$K_{RF}(s)$ = Reference Filter Response

N = 4 (Using Double Edge Sensing With 4 Pole Motor)

$K\phi$ = Phase Detector Gain (.4V/RAD)

G_{PD} = Power Stage Transconductance (1A/V)

K_T = Motor Torque Constant (.022NM/A)

J = Motor Moment of Inertia (.0015NM - SEC^2)

$s = 2\pi jf$

*Note: For a current mode driver the electrical time constant, L_M/R_M, of the motor does not enter into into the small signal response. If a voltage mode drive scheme is used, then the asymptote, plotted as **2** above, can be approximated by:

$$\frac{N \cdot K\phi \cdot K_{PD} \cdot K_T}{s^2 \cdot J \cdot R_M} \quad \text{if: } R_M \gg K_T \sqrt{\frac{L_M}{J}} \quad \text{and,} \quad \frac{K_T^2}{2\pi \cdot J \cdot R_M} < f < \frac{R_M}{2\pi \cdot L_M}$$

Here: K_{PD} = Voltage Gain of Driver Stage

R_M = Motor Winding Resistance

L_M = Motor Winding Inductance

LINEAR INTEGRATED CIRCUITS
Phase Locked Frequency Controller

UC1634
UC2634
UC3634

4

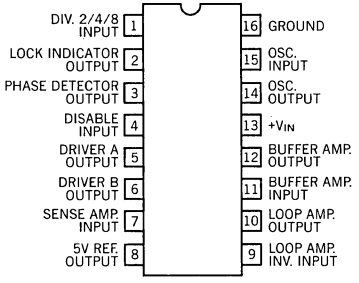
FEATURES
- Precision Phase Locked Frequency Control System
- Commutation Logic for 2-Phase Motors
- Disable Input for Motor Inhibit
- Crystal Oscillator
- Programmable Reference Frequency Dividers
- Phase Detector with Absolute Frequency Steering
- Digital Lock Indicator
- Two High Current Op-Amps
- 5V Reference Output

DESCRIPTION
The UC1634 series of devices is optimized to provide precision phase locked frequency control for two phase DC brushless motors. These devices include most of the features of the general purpose UC1633 Phase Locked Control family and also provide the out-of-phase commutation signals required for driving two phase brushless motors. Only an external power booster stage is required for a complete drive and control system.

The two commutation outputs are open collector devices that can sink in excess of 16mA. A disable input allows the user to simultaneously force both of these outputs to an active low state. Double edge logic, following the sense amplifier, doubles the reference frequency at the phase detector by responding to both edges of the input signal at Pin 7.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE

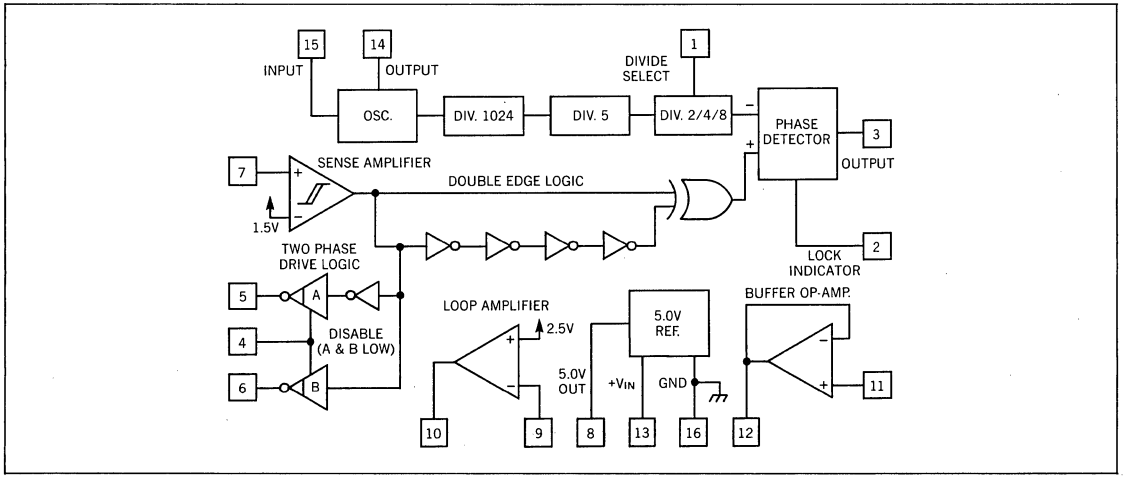


ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage ($+V_{IN}$) ..... +20V
Reference Output Current ..... −30mA
Op-Amp Output Currents ..... ±30mA
Op-Amp Input Voltages ..... −.3V to +20V
Phase Detector Output Current ..... ±10mA
Lock Indicator Output Current ..... +15mA
Lock Indicator Output Voltage ..... +20V
Divide Select Input Voltage ..... −.3V to +10V
Disable Input Voltage ..... −.3V to +10V
Oscillator Input Voltage ..... −.3V to +5V
Sense Amplifier Input Voltage ..... −.3V to +20V
Driver Output Currents ..... +30mA
Driver Output Voltages ..... +20V
Power Dissipation at T_A = 25°C 1000mW
Derate at 10mW/°C above 25°C
Power Dissipation at T_C = 25°C 2000mW
Derate at 16mW/°C above 25°C
Thermal Resistance Junction to Ambient ..... 100°C/W
Thermal Resistance Junction to Case ..... 60°C/W
Operating Junction Temperature ..... −55°C to +150°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note: 1. Voltages are referenced to ground, (Pin 16). Currents are positive into, negative out of, the specified terminals.

BLOCK DIAGRAM



UNITRODE

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, specifications hold for T_A = 0°C to +70°C for the UC3634, −25°C to +85°C for the UC2634 and −55°C to +125°C for the UC1634, $+V_{IN}$ = 12V.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$+V_{IN}$ = 15V		20	29	mA
Reference					
Output Voltage (V_{REF})		4.75	5.0	5.25	V
Load Regulation	I_{OUT} = 0 to 7mA		5.0	20	mV
Line Regulation	$+V_{IN}$ = 8 to 15V		2.0	20	mV
Short Circuit Current	V_{OUT} = 0V	12	30		mA
Oscillator					
DC Voltage Gain	Oscillator In to Oscillator Out	12	16	20	dB
Input DC Level (V_{IB})	Oscillator In Pin Open, T_J = 25°C	1.15	1.3	1.45	V
Input Impedance (Note 2)	$V_{IN} = V_{IB} \pm 0.5V$, T_J = 25°C	1.3	1.6	1.9	kΩ
Output DC Level	Oscillator In Pin Open, T_J = 25°C	1.2	1.4	1.6	V
Maximum Operating Frequency		10			MHz
Dividers					
Maximum Input Frequency	Input = $1V_{PP}$ at Oscillator In	10			MHz
Div. 4/5 Input Current (Q Package Only, Note 3)	Input = 5V (Div. by 4)		150	500	μA
	Input = 0V (Div. by 5)	−5.0	0.0	5.0	μA
Div. 4/5 Threshold (Q Package Only, Note 3)		0.5	1.6	2.2	V
Div. 2/4/8 Input Current	Input = 5V (Div. by 8)		150	500	μA
	Input = 0V (Div. by 2)	−500	−150		μA
Div. 2/4/8 Open Circuit Voltage	Input Current = 0μA (Div. by 4)	1.5	2.5	3.5	V
Div. by 2 Threshold		0.35	0.8		V
Div. by 4 Threshold		1.5		3.5	V
Div. by 8 Threshold	Volts Below V_{REF}	0.35	0.8		V
Sense Amplifier					
Threshold Voltage	Percent of V_{REF}	27	30	33	%
Threshold Hysteresis			10		mV
Input Bias Current	Input = 1.5V	−1.0	−0.2		μA
Two Phase Drive Outputs, A and B					
Saturation Voltage	I_{OUT} = 16mA		0.3	0.6	V
Leakage Current	V_{OUT} = 15V		0.1	5.0	μA
Disable Input					
Input Current	Input = 5V (Disabled, A and B Outputs Active Low)		150	500	μA
	Input = 0V (Enabled)	−5.0	0.0	5.0	μA
Threshold Voltage		0.5	1.6	2.2	V
Phase Detector					
High Output Level	Positive Phase/Freq. Error, Volts Below V_{REF}		0.2	0.5	V
Low Output Level	Negative Phase/Freq. Error		0.2	0.5	V
Mid Output Level	Zero Phase/Freq. Error, Percent of V_{REF}	47	50	53	%
High Level Maximum Source Current	V_{OUT} = 4.3V	2.0	8.0		mA
Low Level Maximum Sink Current	V_{OUT} = 0.7V	2.0	5.0		mA
Mid Level Output Impedance (Note 2)	I_{OUT} = −200 to +200μA, T_J = 25°C	4.5	6.0	7.5	kΩ

Note: 2. These impedance levels will vary with T_J at about 1700ppm/°C.
3. This part is also available in a 20 pin plastic leadless chip carrier, Q designator, where a divide by 4/5 select pin is available. Consult factory for details.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, specifications hold for T_A = 0°C to +70°C for the UC3634, −25°C to +85°C for the UC2634 and −55°C to +125°C for the UC1634, $+V_{IN}$ = 12V.)

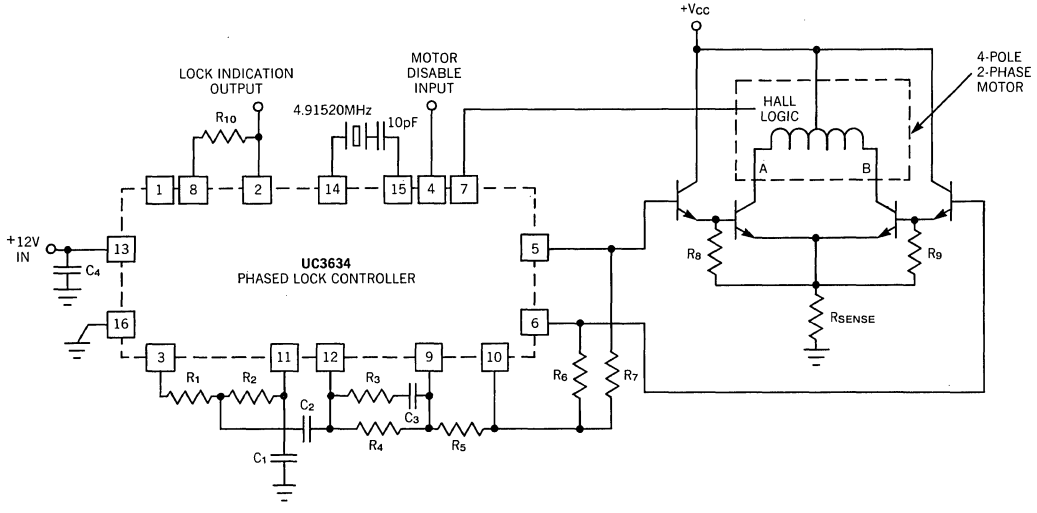
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Lock Indicator Output					
Saturation Voltage	Freq. Error, I_{OUT} = 5mA		0.3	0.45	V
Leakage Current	Zero Freq. Error, V_{OUT} = 15V		0.1	1.0	μA
Loop Amplifier					
N INV. Reference Voltage	Percent of V_{REF}	47	50	53	%
Input Bias Current	Input = 2.5V	−0.8	−0.2		μA
AVOL		60	75		dB
PSRR	$+V_{IN}$ = 8 to 15V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA
Buffer Op-Amp					
Input Offset Voltage	V_{CM} = 2.5V			8	mV
Input Bias Current	V_{CM} = 2.5V	−0.8	−0.2		μA
PSRR	$+V_{IN}$ = 8 to 15V	70	100		dB
CMRR	V_{CM} = 0 to 10V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA

4

APPLICATION AND OPERATION INFORMATION (For additional information see UC1633 data sheet)

Design Example:

Precision phased locked frequency control of a 2-phase motor at 3600 RPM. Using the commutation logic on the UC3634, a simple discrete drive scheme is possible.



LINEAR INTEGRATED CIRCUITS

Switched Mode Controller for DC Motor Drive

UC1637
UC2637
UC3637

FEATURES

- Single or dual supply operation
- ± 2.5V to ± 20V input supply range
- ± 5% initial oscillator accuracy; ± 10% over temperature
- Pulse-by-pulse current limiting
- Under-voltage lockout
- Shutdown input with temperature compensated 2.5V threshold
- Uncommitted PWM comparators for design flexibility
- Dual 100mA, source/sink output drivers

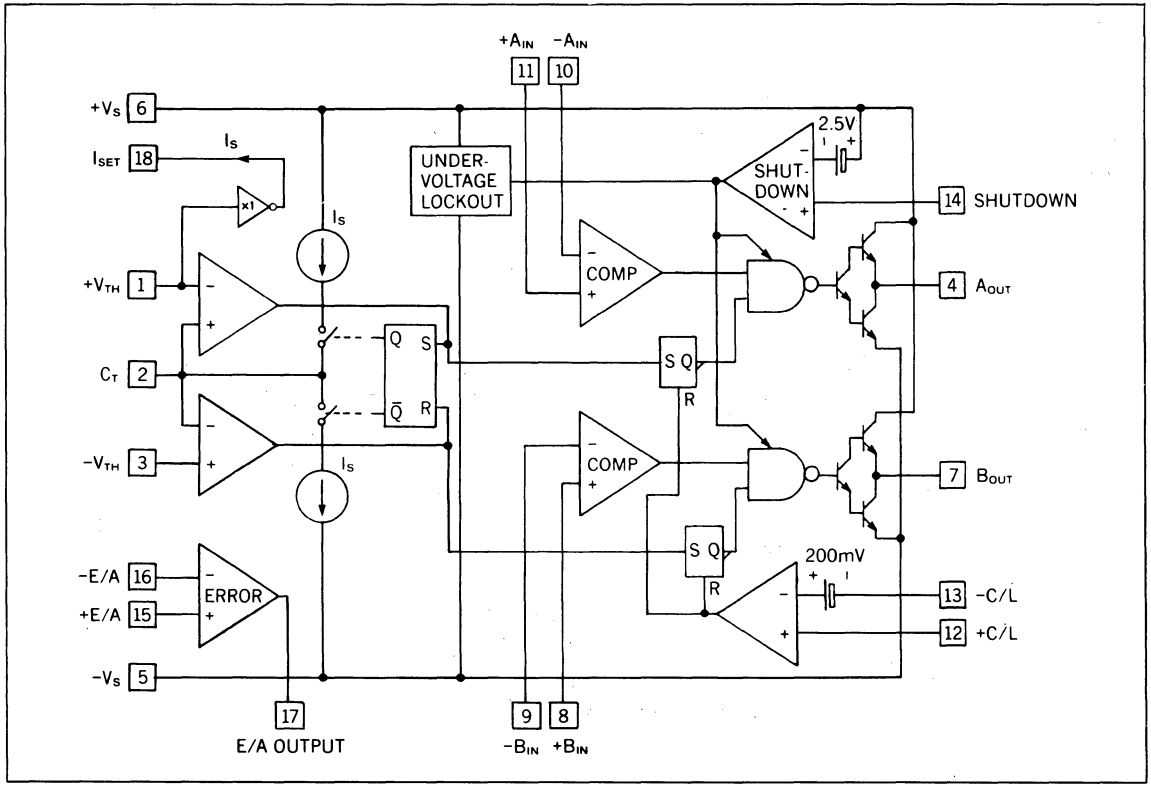
DESCRIPTION

The UC1637 is a pulse width modulator circuit intended to be used for a variety of PWM motor drive and amplifier applications requiring either uni-directional or bi-directional drive circuits. When used to replace conventional drivers, this circuit can increase efficiency and reduce component costs for many applications. All necessary circuitry is included to generate an analog error signal and modulate two bi-directional pulse train outputs in proportion to the error signal magnitude and polarity.

This monolithic device contains a sawtooth oscillator, error amplifier, and two PWM comparators with ± 100mA output stages as standard features. Protection circuitry includes under-voltage lockout, pulse-by-pulse current limiting, and a shutdown port with a 2.5V temperature compensated threshold.

The UC1637 is characterized for operation over the full military temperature range of −55°C to +125°C, while the UC2637 and UC3637 are characterized for −25°C to +85°C and 0°C to +70°C, respectively.

BLOCK DIAGRAM



UNITRODE

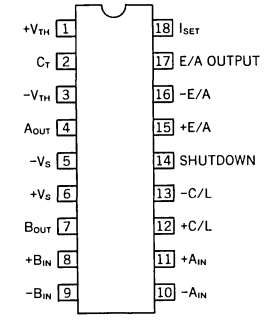
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ($\pm V_S$) ..... ±20V
Output Current, Source/Sink (Pins 4, 7) 500mA
Analog Inputs (Pins 1, 2, 3, 8, 9, 10, 11, 12, 13, 14, 15, 16) ..... $\pm V_S$
Error Amplifier Output Current (Pin 17) ..... ±20mA
Oscillator Charging Current (Pin 18) ..... -2mA
Power Dissipation at T_A = 25°C 1000mW
Derate at 10mW/°C For T_A above 50°C
Power Dissipation at T_C = 25°C 2000mW
Derate at 16mW/°C for T_C above 25°C
Thermal Resistance, Junction to Ambient ..... 100°C/W
Thermal Resistance, Junction to Case ..... 60°C/W
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

Note: 1. Currents are positive into, negative out of the specified terminal.

CONNECTION DIAGRAM

DIL-18 (TOP VIEW)
J or N PACKAGE



4

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for UC1637; -25°C to +85°C for the UC2637; and 0°C to +70°C for the UC3637; $+V_S$ = +15V, $-V_S$ = -15V, $+V_{TH}$ = 5V, $-V_{TH}$ = -5V, R_T = 16.7kΩ, C_T = 1500pF)

PARAMETER	TEST CONDITIONS	UC1637/UC2637			UC3637			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Oscillator								
Initial Accuracy	T_j = 25°C	9.4	10	10.6	9	10	11	kHz
Voltage Stability	V_S = ± 5V to ± 20V, $V_{PIN\ 1}$ = 3V $V_{PIN\ 3}$ = -3V		5	7		5	7	%
Temperature Stability	Over Operating Range		0.5	2		0.5	2	%
$+V_{TH}$ Input Bias Current	$V_{PIN\ 2}$ = 6V	-10	0.1	10	-10	0.1	10	µA
$-V_{TH}$ Input Bias Current	$V_{PIN\ 2}$ = 0V	-10	-0.5		-10	-0.5		µA
$+V_{TH}$, $-V_{TH}$ Input Range		$+V_S$-2		$-V_S$+2	$+V_S$-2		$-V_S$+2	V
Error Amplifier								
Input Offset Voltage	V_{CM} = 0V		1.5	5		1.5	10	mV
Input Bias Current	V_{CM} = 0V		0.5	5		0.5	5	µA
Input Offset Current	V_{CM} = 0V		0.1	1		0.1	1	µA
Common Mode Range	V_S = ± 2.5 to 20V	$-V_S$+2		$+V_S$	$-V_S$+2		$+V_S$	V
Open Loop Voltage Gain	R_L = 10K	75	100		80	100		dB
Slew Rate			15			15		V/µs
Unity Gain Bandwidth								
CMRR	Over Common Mode Range	75	100		75	100		dB
PSRR	V_S = ± 2.5V to ± 20V	75	110		75	110		dB
Output Sink Current	$V_{PIN\ 17}$ = 0V		-50	-20		-50	-20	mA
Output Source Current	$V_{PIN\ 17}$ = 0V	5	11		5	11		mA
High Level Output Voltage		13	13.6		13	13.6		V
Low Level Output Voltage			-14.8	-13		-14.8	-13	V
PWM Comparators								
Input Offset Voltage	V_{CM} = 0V		20			20		mV
Input Bias Current	V_{CM} = 0V		2	10		2	10	µA
Input Hysteresis	V_{CM} = 0V		10			10		mV
Common Mode Range	V_S = ± 5 to ± 40V	$-V_S$+1		$+V_S$-2	$-V_S$+1		$+V_S$-2	V

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for UC1637; −25°C to +85°C for the UC2637; and 0°C to +70°C for the UC3637; $+V_S$ = +15V, $-V_S$ = −15V, $+V_{TH}$ = 5V, $-V_{TH}$ = −5V, R_T = 16.7kΩ, C_T = 1500pF)

PARAMETER	TEST CONDITIONS	UC1637/UC2637			UC3637			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Current Limit								
Input Offset Voltage	V_{CM} = 0V, T_j = 25°C	190	200	210	180	200	220	mV
Input Offset Voltage T.C.			−0.2			−0.2		mV/°C
Input Bias Current		−10	−1.5		−10	−1.5		μA
Common Mode Range	V_S = ± 2.5V to ± 20V	$-V_S$		$+V_S$−3	$-V_S$		$+V_S$ −3	V
Shutdown								
Shutdown Threshold	(Note 3)	−2.3	−2.5	−2.7	−2.3	−2.5	−2.7	V
Hysteresis			40			40		mV
Input Bias Current	$V_{PIN\ 14}$ = $+V_S$ to $-V_S$	−10	−0.5		−10	−0.5		μA
Under-Voltage Lockout								
Start Threshold	(Note 4)		4.15	5.0		4.15	5.0	V
Hysteresis			0.25			0.25		mV
Total Standby Current								
Supply Current			8.5	15		8.5	15	mA
Output Section								
Output Low Level	I_{SINK} = 20mA		−14.9	−13		−14.9	−13	V
	I_{SINK} = 100mA		−14.5	−13		−14.5	−13	
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
	I_{SOURCE} = 100mA	12	13.5		12	13.5		
Rise Time	(Note 2) C_L = 1nf, T_j = 25°C		100	600		100	600	ns
Fall Time	(Note 2) C_L = 1nf, T_j = 25°C		100	300		100	300	ns

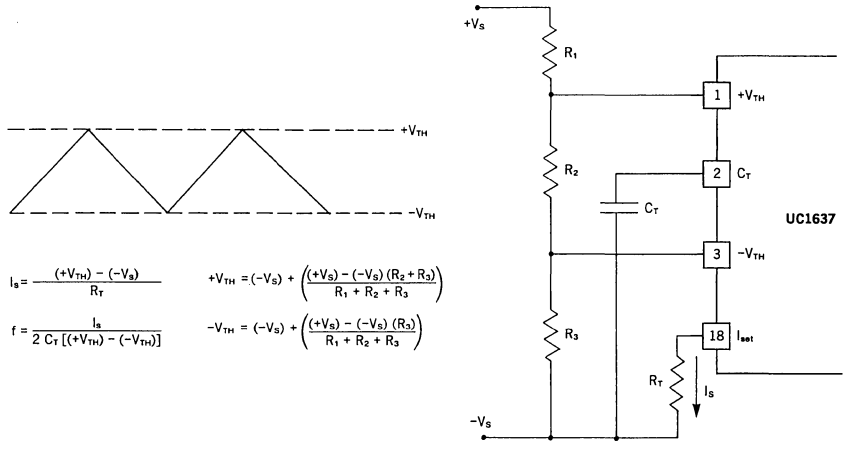
Notes: 2. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
3. Parameter measured with respect to $+V_S$ (Pin 6).
4. Parameter measured at $+V_S$ (Pin 6) with respect to $-V_S$ (Pin 5).

FUNCTIONAL DESCRIPTION

Following is a description of each of the functional blocks shown in the Block Diagram.

Oscillator

The oscillator consists of two comparators, a charging and discharging current source, a current source set terminal, I_{set}, and a flip-flop. The upper and lower threshold of the oscillator waveform is set externally by applying a voltage at pins $+V_{TH}$ and $-V_{TH}$ respectively. The $+V_{TH}$ terminal voltage is buffered internally and also applied to the I_{set} terminal to develop the capacitor charging current through R_T. If R_T is referenced to $-V_S$ as shown in Figure 1, both the threshold voltage and charging current will vary proportionally to the supply differential, and the oscillator frequency will remain constant. The triangle waveform oscillators frequency and voltage amplitude is determined by the external components using the formulas given in Figure 1.



$$I_s = \frac{(+V_{TH}) - (-V_S)}{R_T} \qquad +V_{TH} = (-V_S) + \left(\frac{(+V_S) - (-V_S)(R_2 + R_3)}{R_1 + R_2 + R_3}\right)$$

$$f = \frac{I_s}{2\,C_T\,[(+V_{TH}) - (-V_{TH})]} \qquad -V_{TH} = (-V_S) + \left(\frac{(+V_S) - (-V_S)(R_3)}{R_1 + R_2 + R_3}\right)$$

Figure 1. Oscillator Set Up

PWM Comparators

Two comparators are provided to perform pulse width modulation for each of the output drivers. Inputs are uncommitted to allow maximum flexability. The pulse width of the outputs A and B is a function of the sign and amplitude of the error signal. A negative signal at Pin 10 and 8 will lengthen the high-state of output A and shorten the high-state of output B. Likewise, a positive error signal reverses the procedure. Typically, the oscillator waveform is compared against the summation of the error signal and the level set on Pin 9 and 11.

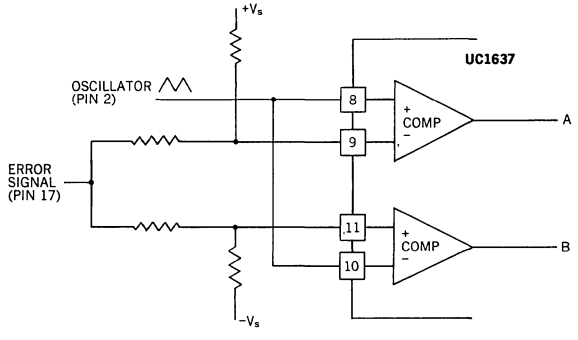


Figure 2. Comparator Biasing

MODULATION SCHEMES

Case A Zero Deadtime (Equal voltage on Pin 9 and Pin 11)

In this configuration, maximum holding torque or stiffness and position accuracy is achieved. However, the power input into the motor is increased. Figure 3A shows this configuration.

Case B Small Deadtime (Voltage on Pin 9 > Pin 11)

A small differential voltage between Pin 9 and 11 provides the necessary time delay to reduce the chances of momentary short circuit in the output stage during transitions, especially where power-amplifiers are used. Refer to Figure 3B.

Case C Increased Deadtime and Deadband Mode
(Voltage on Pin 9 > Pin 11)

With the reduction of stiffness and position accuracy, the power input into the motor around the null point of the servo loop can be reduced or eliminated by widening the window of the comparator circuit to a degree of acceptance. Where position accuracy and mechanical stiffness is unimportant, deadband operation can be used. This is shown in Figure 3C.

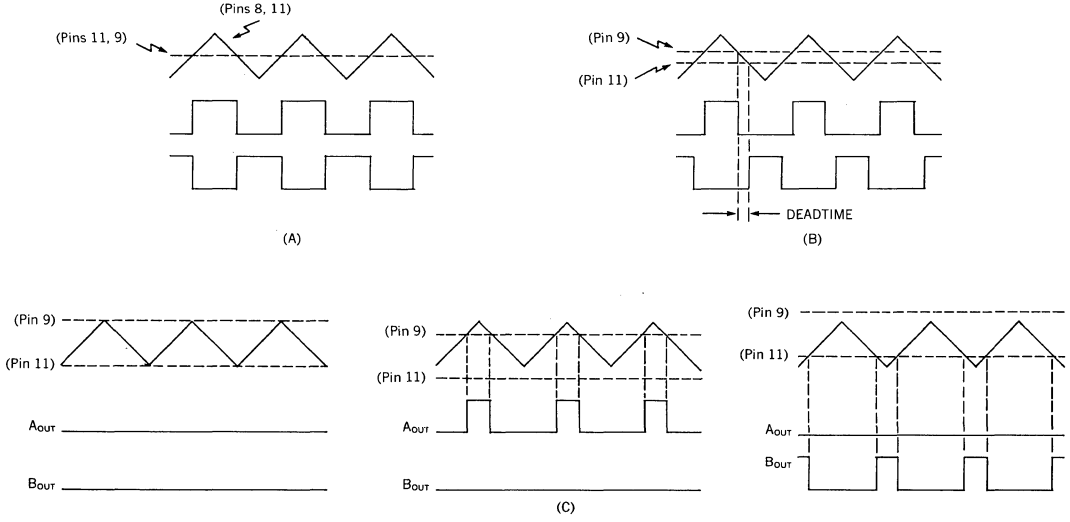


Figure 3. Modulation Schemes Showing (A) Zero Deadtime (B) Deadtime and (C) Deadband Configurations.

Output Drivers

Each output driver is capable of both sourcing and sinking 100mA steady state and up to 500mA on a pulsed basis for rapid switching of either POWERFET or bipolar transistors. Output levels are typically $-V_S$ +0.2V @ 50mA low level and $+V_S$ — 2.0V @ 50mA high level.

Error Amplifier

The error amplifier consists of a high slew rate (15V/μs) op-amp with a typical 1MHz bandwidth and low output impedance. Depending on the $\pm V_S$ supply voltage, the common mode input range and the voltage output swing is within 2V of the V_S supply.

Under-Voltage Lockout

An under-voltage lockout circuit holds the outputs in the low state until a minimum of 4V is reached. At this point, all internal circuitry is functional and the output drivers are enabled. If external circuitry requires a higher starting voltage, an over-riding voltage can be programmed through the shutdown terminal as shown in Figure 4.

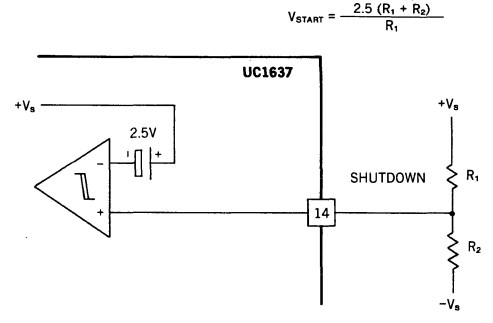


Figure 4. External Under-Voltage Lockout

Shutdown Comparator

The shutdown terminal may be used for implementing various shutdown and protection schemes. By pulling the terminal more than 2.5V below V_{IN}, the output drivers will be enabled. This can be realized using an open collector gate or NPN transistor biased to either ground or the negative supply. Since the threshold is temperature stabilized, the comparator can be used as an accurate low voltage lockout (Figure 4) and/or delayed start as in Figure 5. In the shutdown mode the outputs are held in the low state.

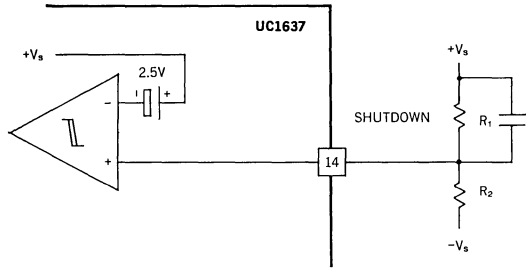


Figure 5. Delayed Start-Up

Current Limit

A latched current limit amplifier with an internal 200mV offset is provided to allow pulse-by-pulse current limiting. Differential inputs will accept common mode signals from $-V_S$ to within 3V of the $+V_S$ supply while providing excellent noise rejection. Figure 6 shows a typical current sense circuit.

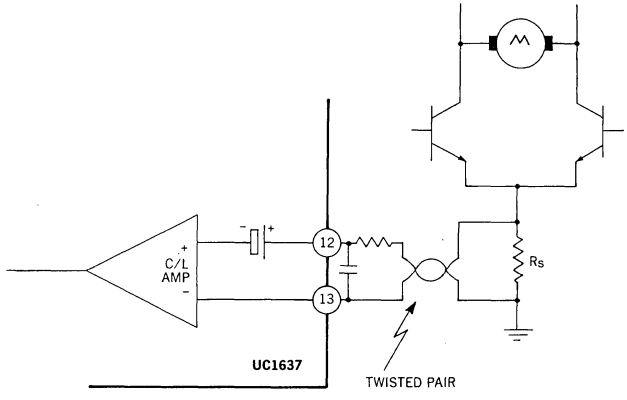


Figure 6. Current Limit Sensing

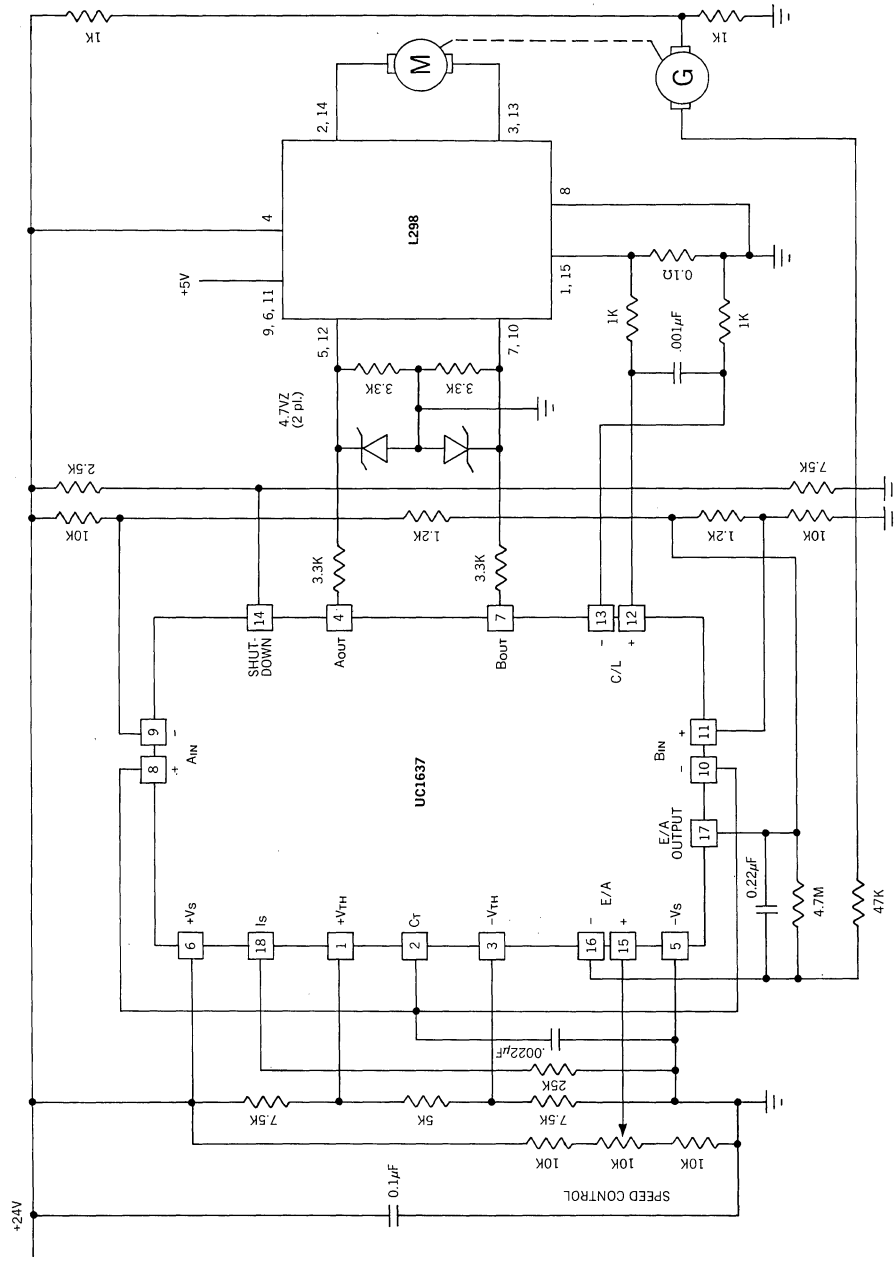


Figure 7. Bi-Directional Motor Drive with Speed Control and Power-Amplifier

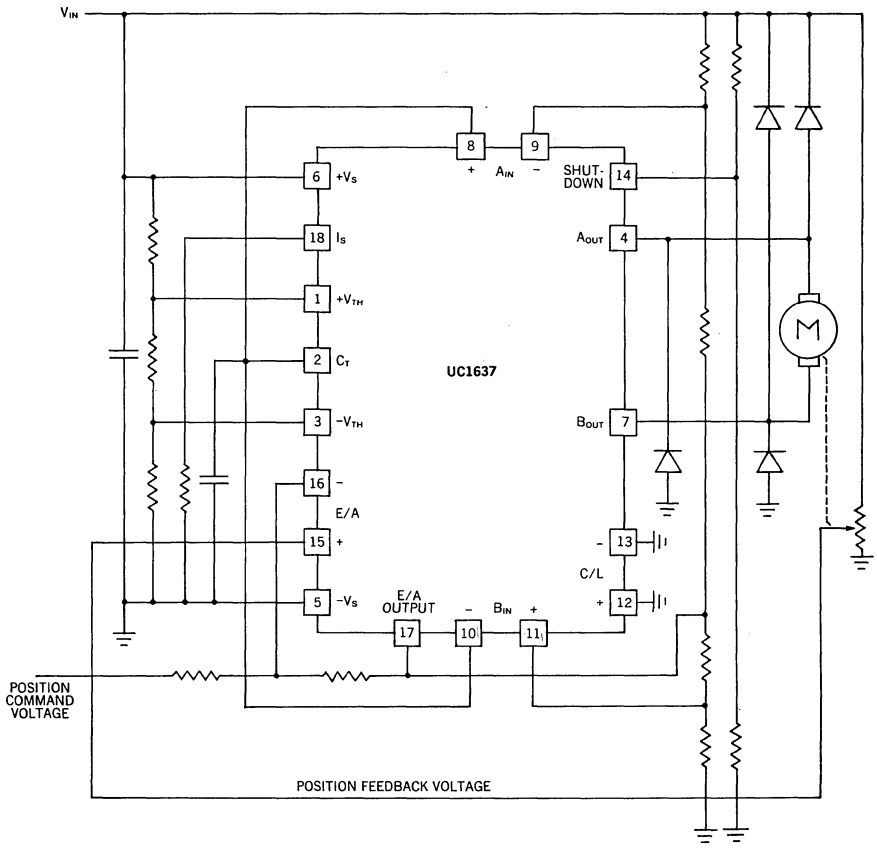


Figure 8. Single Supply Position Servo Motor Drive

LINEAR INTEGRATED CIRCUITS

Stepper Motor Drive Circuit

UC1717
UC3717

FEATURES

- Half-step and full-step capability
- Bipolar constant current motor drive
- Built-in fast recovery Schottky commutating diodes
- Wide range of current control 5-1000mA
- Wide voltage range 10-45V
- Designed for unregulated motor supply voltage
- Current levels can be selected in steps or varied continuously
- Thermal overload protection

DESCRIPTION

The UC3717 has been designed to control and drive the current in one winding of a bipolar stepper motor. The circuit consists of an LS-TTL-compatible logic input, a current sensor, a monostable and an output stage with built-in protection diodes. Two UC3717s and a few external components form a complete control and drive unit for LS-TTL or micro-processor controlled stepper motor systems.

The UC1717 is characterized for operation over the full military temperature range of -55°C to +125°C, while the UC3717 is characterized for 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage
- Logic Supply, V_{CC} 7V
- Output Supply, V_m 45V

Input Voltage
- Logic Inputs (Pins 7, 8, 9) 6V
- Analog Input (Pin 10) ..... V_{CC}
- Reference Input (Pin 11) 15V

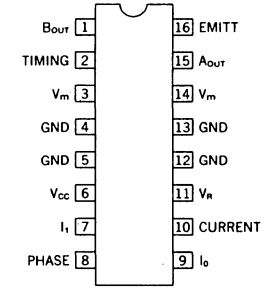
Input Current
- Logic Inputs (Pins 7, 8, 9) ..... -10mA
- Analog Inputs (Pins 10, 11) ..... -10mA

Output Current (Pins 1,15) ..... ±1A
Junction Temperature, T_j ..... +150°C
Thermal Resistance, Junction to Ambient (NE Package) ..... 45°C/W
Thermal Resistance, Junction to Case (NE Package) ..... 11°C/W
Thermal Resistance, Junction to Ambient (J Package) ..... 100°C/W
Thermal Resistance, Junction to Case (J Package) ..... 60°C/W
Storage Temperature Range, T_S ..... -55°C to +150°C

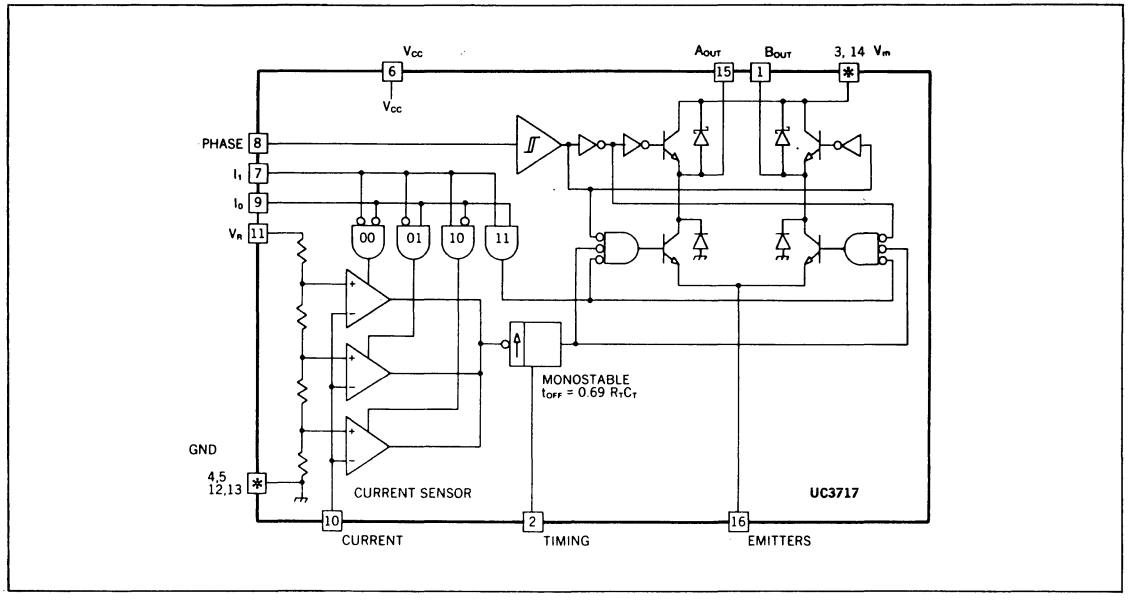
Note: 1. All voltages are with respect to ground, Pins 4, 5, 12, 13. Currents are positive into, negative out of the specified terminal.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or NE PACKAGE



BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN.	TYP.	MAX.	UNITS
Supply Voltage, V_{CC}	4.75	5	5.25	V
Supply Voltage, V_m	10		40	V
Output Current, I_m	20		800	mA
Rise Time Logic Inputs, t_r			2	μs
Fall Time Logic Inputs, t_f			2	μs
Ambient Temperature, t_a				
UC1717	−55		125	°C
UC3717	0		70	°C

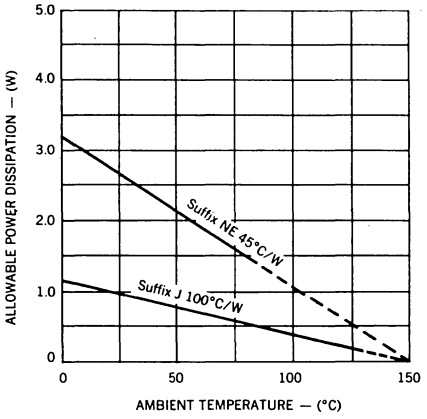


Figure 1.

4

ELECTRICAL CHARACTERISTICS (Over recommended operating conditions unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, I_{CC}				25	mA
High-Level Input Voltage, Pins 7, 8, 9		2.0			V
Low-Level Input Voltage, Pins 7, 8, 9				0.8	V
High-Level Input Current, Pins 7, 8, 9	V_I = 2.4V			20	μA
Low-Level Input Current, Pins 7, 8, 9	V_I = 0.4V	−0.4			mA
Comparator Threshold Voltage	I_0 = 0, I_1 = 0, V_R = 5.0V	390	420	440	mV
	I_0 = 1, I_1 = 0, V_R = 5.0V	230	250	270	mV
	I_0 = 0, I_1 = 1, V_R = 5.0V	65	80	90	mV
Comparator Input Current		−20		20	μA
Output Leakage Current	I_0 = 1, I_1 = 1, T_A = + 25°C			100	μA
Total Saturation Voltage Drop	I_m = 500mA			4.0	V
Total Power Dissipation	I_m = 500mA, f_s = 30kHz		1.4	2.1	W
	I_m = 800mA, f_s = 30kHz		2.9	3.1	W
Cut Off Time, t_{OFF}	See Figure 5 and 6, V_m = 10V, $t_{ON} \geqq 5\mu$s	25	30	35	μs
Turn Off Delay, t_d	See Figure 5 and 6, T_A = +25°C; $dV_C/dt \geqq 50mV/\mu s$		1.6	2.0	μs
Thermal Shutdown Junction Temperature		+160		+180	°C

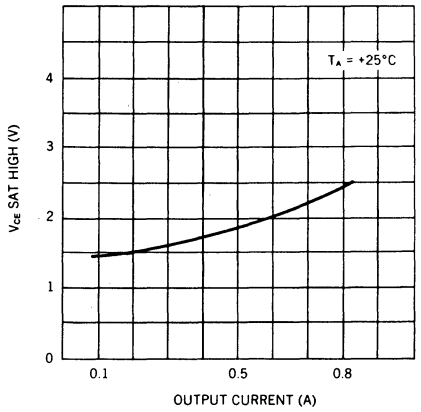


Figure 2. Typical Source Saturation Voltage vs Output Current

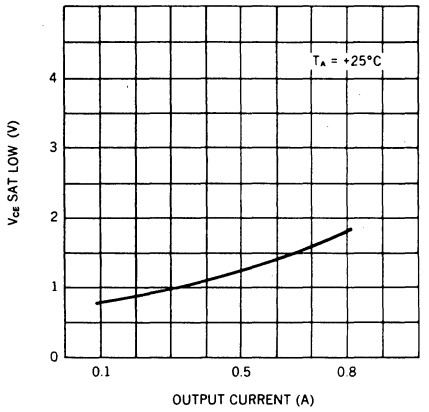


Figure 3. Typical Sink Saturation Voltage vs Output Current

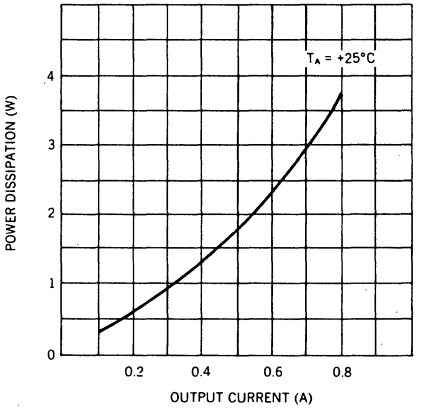


Figure 4. Typical Power Losses vs Output Current

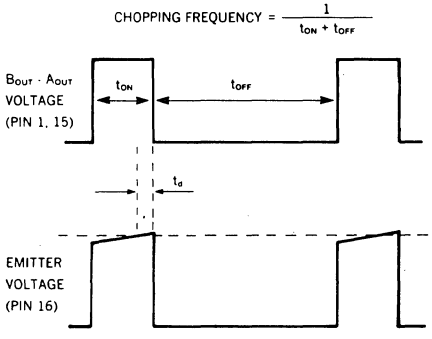


Figure 5. Connections and Component Values as in Figure 6

FUNCTIONAL DESCRIPTION

The UC3717 drive circuit shown in the block diagram includes the following functions.

(1) Phase Logic and H-Bridge Output Stage
(2) Voltage Divider with three Comparators for current control
(3) Two Logic inputs for Digital current level select
(4) Monostable for off time generation

Input Logic
If any of the logic inputs are left open, the circuit will treat it as a high level input.

Phase Input
The phase input terminal, pin 18, controls the direction of the current through the motor winding. The Schmidt-Trigger input coupled with a fixed time delay assures noise immunity and eliminates cross conduction in the output stage during phase changes. A low level on the phase input will turn Q2 on and enable Q3 while a high level will turn Q1 on and enable Q4. (See Figure 7).

Output Stage
The output stage consists of four Darlington transistors and associated diodes connected in an H-Bridge configuration. The diodes are needed to provide a current path when the transistors are being switched. For fast recovery, Schottky diodes are used across the source transistors. The Schottky diodes allow the current to circulate through the winding while the sink transistors are being switched off. The diodes across the sink transistors in conjunction with the Schottkys provide the path for the decaying current during phase reversal. (See Figure 7).

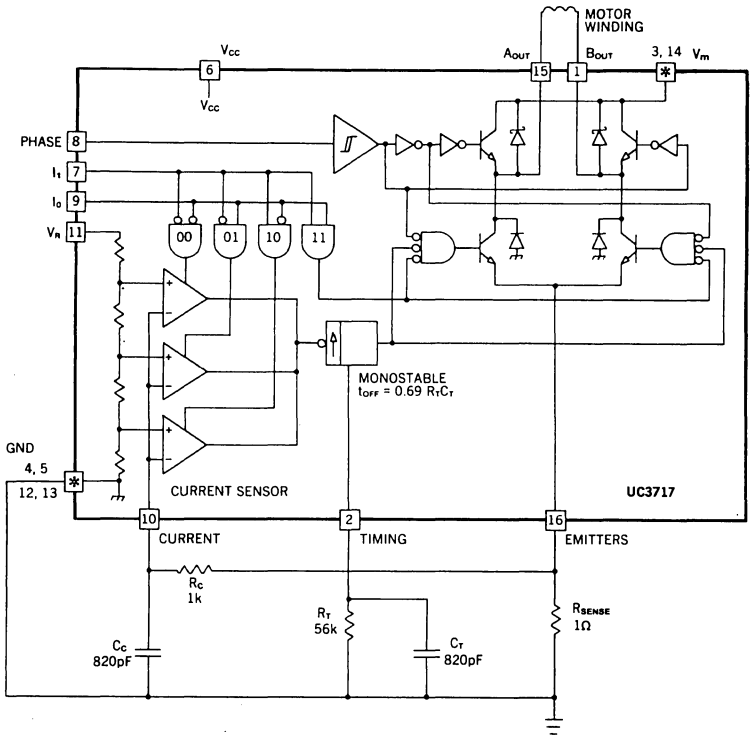


Figure 6.

PHASE INPUT	Q1, Q4	Q2, Q3
LOW	OFF	ON
HIGH	ON	OFF

TABLE 1

I_0	I_1	CURRENT LEVEL
0	0	100%
1	0	60%
0	1	19%
1	1	CURRENT INHIBIT

Current Control

The voltage divider, comparators and monostable provide a means for current sensing and control. The two bit input (I_0, I_1) logic selects the desired comparator. The monostable controls the off time and therefore the magnitude of the current decrease. The time duration is determined by R_T and C_T connected to the timing terminal (pin 2). The reference terminal (pin 11) provides a means of continuously varying the current for situations requiring half-stepping and micro-stepping. The relationship between the logic input signals at pin 7 and 9 in reference to the current level is shown in Table 1. The values of the different current levels are determined by the reference voltage together with the value of the external sense resistor R_s (pin 16).

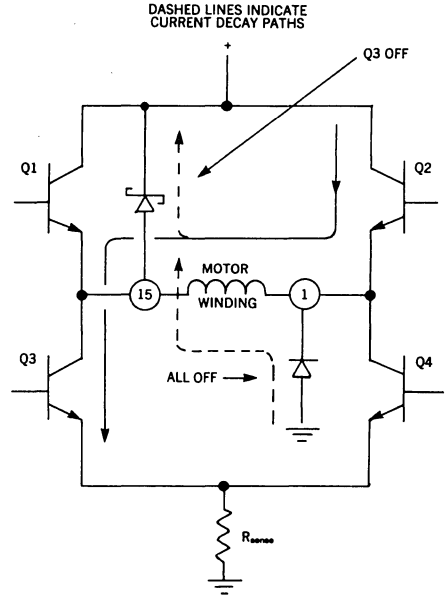


Figure 7. Simplified Schematic of Output Stage

Single-Pulse Generator

The pulse generator is a monostable triggered on the positive going edge of the comparator. Its output is high during the pulse time and this pulse switches off the power feed to the motor winding causing the current to decay. The time is determined by the external timing components R_T and C_T as:

$$t_{OFF} = 0.69\ R_T C_T$$

If a new trigger signal should occur during t_{OFF}, it is ignored.

Overload Protection

The circuit is equipped with a thermal shutdown function, which will limit the junction temperature by reducing the output current. It should be noted however, that a short circuit of the output is not permitted.

Operation

When the voltage is applied across the motor winding the current rises linearly and appears across the external sense resistor as an analog voltage. This voltage is fed through a low-pass filter R_C, C_C to the the voltage comparator (pin 10). At the moment the voltage rises beyond the comparator threshold voltage the monostable is triggered and its output turns off the sink transistors. The current then circulates through the source transistor and the appropriate Schottky diode. After the one shot has timed out, the sink transistor is turned on again and the procedure repeated until a current reverse command is given. By reversing the logic level of the phase input (pin 8), both active transistors are being turned off and the opposite pair turned on. When this happens the current must first decay to zero before it can reverse. The current path then provided is through the two diodes and the power-supply. Refer to Figure 7. It should be noticed at this time that the slope of the current decay is steeper, and this is due to the higher voltage build up across the winding. For better speed performance of the stepping motor at half step mode, the phase logic level should be changed the same time the current inhibit is applied. A typical current wave form is shown in Figure 8.

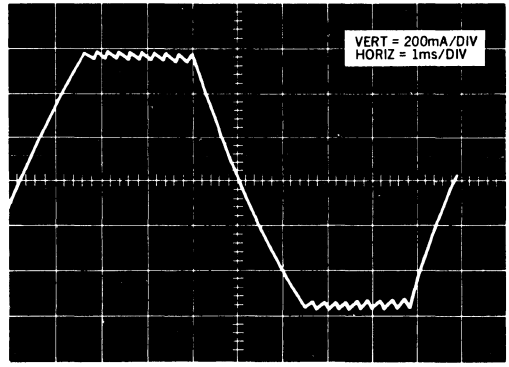


Figure 8.

APPLICATIONS

A typical chopper drive for a two phase bipolar permanent magnet or hybrid stepping motor is shown in Figure 9. The input can be controlled by a microprocessor, TTL, LS or CMOS logic.

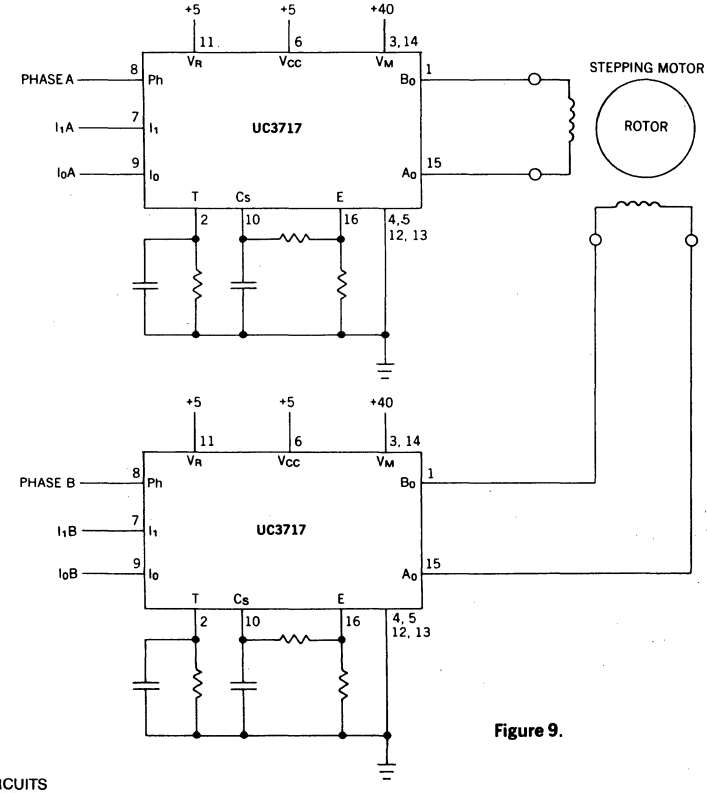


Figure 9.

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The timing diagram in Figure 10 shows the required signal input for a two phase, full step, stepping sequence. Figure 11 shows a one phase, full step, stepping sequence, commonly referred to as wave drive. Figure 12 shows the required input signal for a one phase-two phase stepping sequence called half-stepping.

The circuit of Figure 13 provides the signal shown in Figure 10, and in conjunction with the circuit shown in Figure 9, will implement a pulse-to-step two phase, full step, bidirectional motor drive.

The schematic of Figure 14 shows a pulse to half step circuit generating the signal shown in Figure 12. Care has been taken to change the phase signal the same time the current inhibit is applied. This will allow the current to decay faster and therefore enhance the motor performance at higher step rates.

The UC3717 can also be used to drive an external high power output stage such as the Unitrode PIC900 hybrid circuit in an 18-Pin dual-in-line package. The 5A output of the PIC900 can be controlled with as little as 5mA base drive. Using the UC3717 to drive the PIC900 provides a uniquely packaged state-of-the-art high power stepper motor control and drive. See Figure 15.

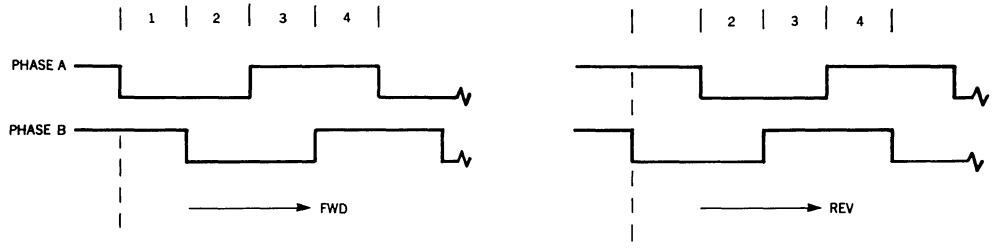

Figure 10. Phase Input Signal for Two Phase Full Step Drive (4 Step Sequence)

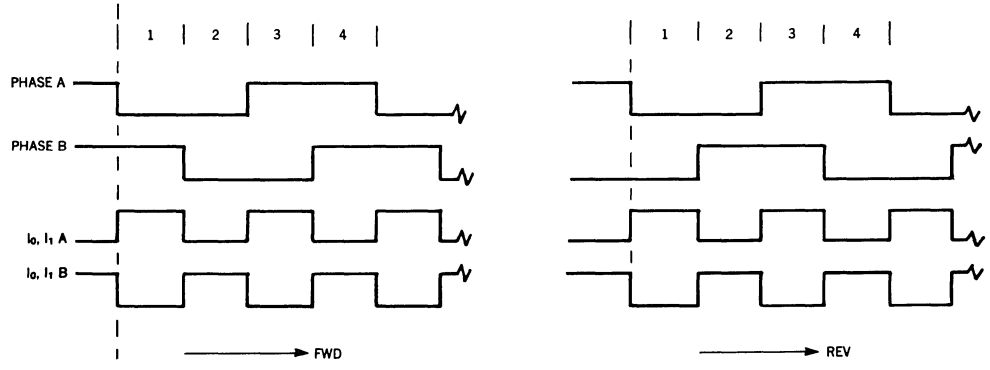

Figure 11. Phase and Current-Inhibit Signal for Wave Drive (4 Step Sequence)

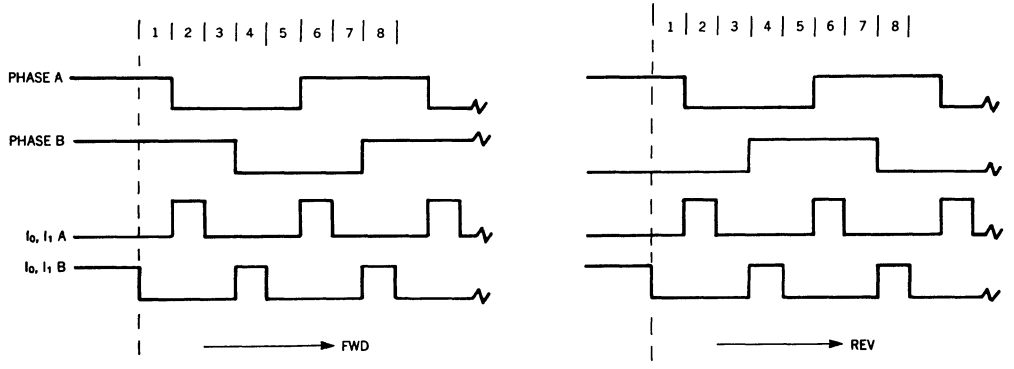

Figure 12. Phase and Current-Inhibit Signal for Half-Stepping (8 Step Sequence)

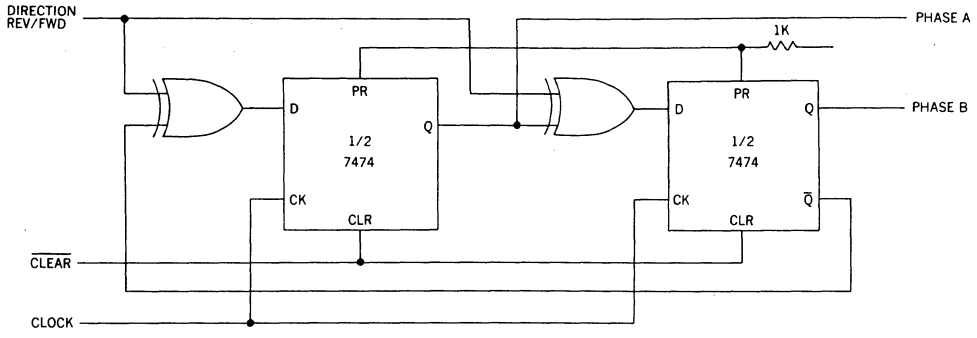

Figure 13. Full Step, Bidirectional Two Phase Drive Logic

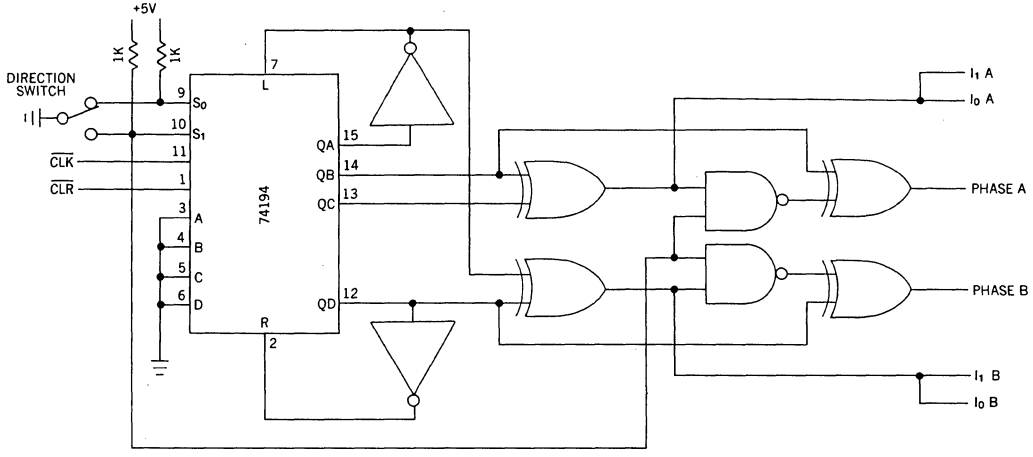

Figure 14. Half Step, Bidirectional Drive Logic

CONSIDERATION

Half-Stepping

In the half step sequence the power input to the motor alternates between one or two phases being energized. In a two phase motor the electrical phase shift between the windings is 90 degrees. The torque developed is the vector sum of the two windings energized. Therefore when only one winding is energized the torque of the motor is reduced by approximately 30%. This causes a torque ripple and if it is necessary to compensate for this, the V_R input can be used to boost the current of the single energized winding.

Ramping

Every drive system has inertia and must be considered in the drive scheme. The rotor and load inertia plays a big role at higher speeds. Unlike the DC motor the stepping motor is a synchronous motor and does not change its speed due to load variations. Examining typical stepping motors torque vs. speed curves indicates a sharp torque drop off for the start-stop without error curve, even with a constant current drive. The reason for this is that the torque requirements increase by the square of the speed change, and the power need increases by the cube of the speed change. As it can be seen, for good motor performance controlled acceleration and deceleration should be considered.

Iron Core Losses

Some motors, especially the Tin-Can type, exhibit high iron losses mostly due to eddy currents which rise in an exponental matter as the frequency or step rate is increased. The power losses can not be calculated by I^2R where I is the chopping current level and R the DC resistance of the coil. Actual measurements indicate the effective resistance may be many times larger. Therefore, for 100% duty cycle the current must be limited to a value which will not overheat the motor. This may not be necessary for lower duty cycle operation.

Interference

Electrical noise generated by the chopping action can cause interference problems, particularly in the vicinity of magnetic storage media. With this in mind, printed circuit layouts, wire runs and decoupling must be considered. 0.01 to 0.1μF ceramic capacitors for high frequency bypass located near the drive package across V+ and ground might be very helpful. The connection and ground leads of the current sensing components should be kept as short as possible.

Ordering Information

UNITRODE TYPE NUMBER
UC3717NE — 16 Pin Dual-in-line (DIL) "Bat Wing" Package
UC3717J — 16 Pin Dual-in-line Ceramic Package
UC1717J — 16 Pin Dual-in-line Ceramic Package

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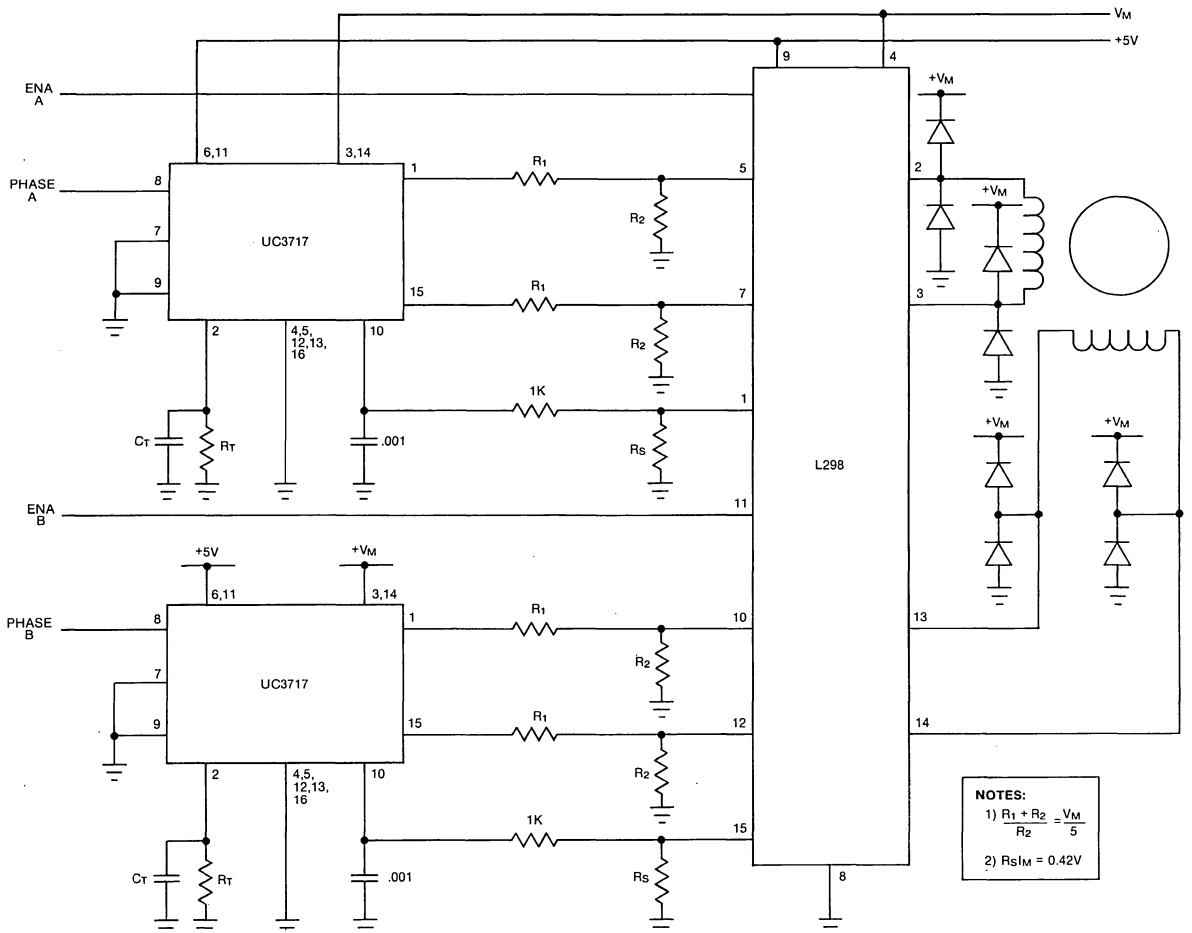


Figure 15 - UC3717 with L298 Power Amplifier.

LINEAR INTEGRATED CIRCUITS

Full Bridge Power Amplifier

FEATURES

- Dual Power Operational Amplifiers
- ±2A Output Current Guaranteed
- Precision Current Sense Amplifier
- Two Supply Monitoring Inputs
- Parking Function and Under-Voltage Lockout
- Typical Total V_{SAT} of 3V @ 2A
- Safe Operating Area Protection
- 5V to 35V Operation

DESCRIPTION

The UC3176 contains two power operational amplifiers that are rated for a continuous output current of 2A. Intended for use in precision servo applications such as disk head positioning, these Op-Amps can be used in a standard voltage feedback mode, or the IC's current sense amplifier can be used to obtain precision control of the load current in a bridge configuration. Output stage protection includes foldback current limiting and thermal shutdown.

Auxiliary functions on this device include a dual input under-voltage comparator that can be programmed to respond to low voltage conditions on two independent supplies. In response to an under-voltage condition the power Op-Amps are inhibited and a high current, 100 mA, drive output is activated. A separate logic level input is also available to force this state. The above functions are easily combined to provide a head parking function in disc drive applications.

The devices are operational over a 5V–35V supply range. Internal under-voltage lockout provides predictable power-up and power-down characteristics. The parts are packaged in the 15-Pin Multiwatt package with a maximum θ_{jc} of 3°C/W.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage, ($+V_{IN}$) 40V
Other Input Voltages ..... −0.3V to $+V_{IN}$
AI_{SINK} and BI_{SINK} Voltages ..... −0.3V to +6V
Parking Drive Output Voltage ..... −0.3V to +40V
A and B Output Currents (Continuous)
Source ..... Internally Limited
Sink 2.5A
Total Supply Current (Continuous) 4A
Parking Drive Output Current (Continuous) ..... 150 mA
Operating Junction Temperature ..... −55°C to +150°C
Power Dissipation at T_C = +75°C 25W
Storage Temperature ..... −65°C to +150°C

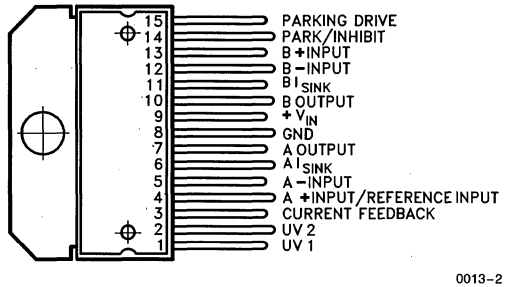
Note: 1. Voltages are referenced to ground, PIN 8. Currents are positive into, negative out of, the specified terminals.

Thermal Data

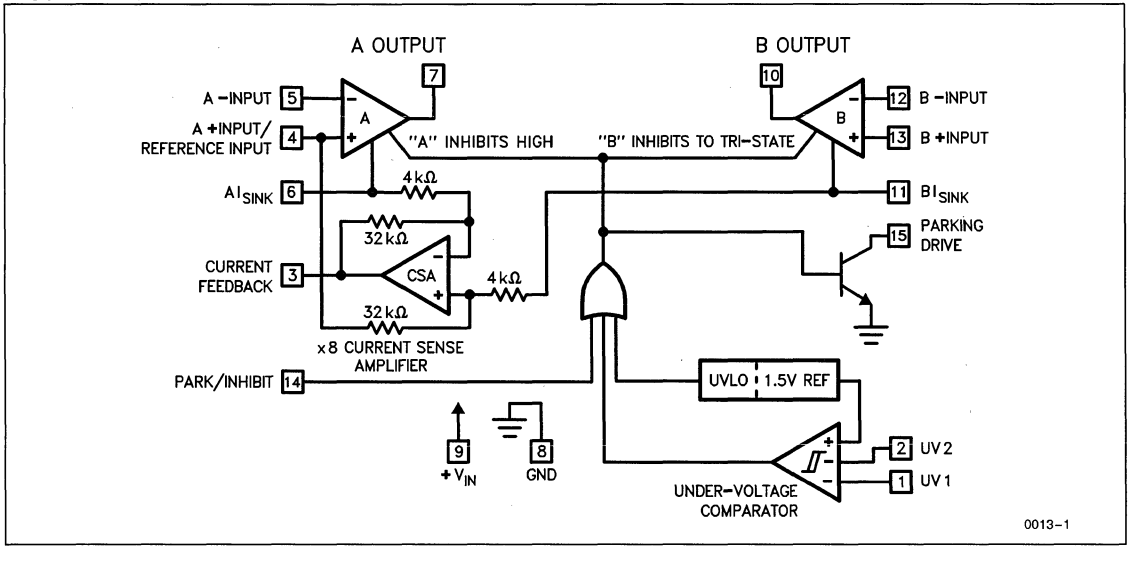
Thermal Resistance Junction to Case, θ_{jc} ..... 3°C/W
Thermal Resistance Junction to Ambient, θ_{ja} ..... 35°C/W

CONNECTION DIAGRAM

MULTIWATT 15-PIN V PACKAGE
(TOP VIEW)



BLOCK DIAGRAM



UNITRODE

ELECTRICAL CHARACTERISTICS Unless otherwise stated, specifications hold for T_j = 0°C to +70°C, $+V_{IN}$ = 12V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY					
Supply Current	$+V_{IN}$ = 12V		21		mA
	$+V_{IN}$ = 35V		25		mA
UVLO Threshold	$+V_{IN}$ Low to High		2.8		V
	Threshold Hysteresis		150		mV
POWER AMPLIFIERS, A and B					
Input Offset Voltage	I_{OUT} = 0, V_{CM} = 6V, V_{OUT} = 6V				mV
Input Bias Current	V_{CM} = 6V, Except A+ Input		1		µA
Input Bias Current at A+/Reference Input	(A+/Ref − BI_{SINK})/36 kΩ		28		µA/V
Input Offset Current	V_{CM} = 6V, B Amp Only		50		nA
CMRR	V_{CM} = 1 to 33V, $+V_{IN}$ = 35V, V_{OUT} = 6V, I_{OUT} = 0A		100		dB
PSRR	$+V_{IN}$ = 5 to 35V, V_{CM} = 2.5V, I_{OUT} = 0A		100		dB
Thermal Feedback	$+V_{IN}$ = 20V, P_D = 20W				µV/W
Saturation Voltage	I_{OUT} = −2A, High Side		1.7		V
	I_{OUT} = 2A, Low Side		1.1		V
Unity Gain Bandwidth			1		MHz
Slew Rate			2		V/µs
Differential I_{OUT} Sense Error Current in Bridge Configuration	$\lvert I_{OUT}\rvert - \lvert AI_{SINK} - BI_{SINK}\rvert$, 0A < $\lvert I_{OUT}\rvert$ < 2A, $AI_{OUT} = -BI_{OUT}$		3		mA
Thermal Shutdown	Tri-States A & B Outputs		165		°C
CURRENT SENSE AMPLIFIER					
Input Offset Voltage	V_{CM} = 0V, A+/Ref at 6V			2.0	mV
	A+/Ref = 2V to 20V, $+V_{IN}$ = 35, as Percent of A+/Ref Voltage			0.06	%
Thermal Gradient Sensitivity	$+V_{IN}$ = 20V, A+/Ref = 10V P_D = 20W				mV/W
Gain	$\lvert AI_{SINK} - BI_{SINK}\rvert$ < 0.5V		8		V/V
Slew Rate			4		V/µs
3 dB Bandwidth			1		MHz
Max Output Current	I_{SOURCE}, $+V_{IN} - V_{OUT}$ = 0.5V		3.0		mA
Output Saturation Voltage	I_{SOURCE} = 1.5 mA, High Side		0.3		V
	I_{SINK} = 5 mA, Low Side		1.0		V
UNDER-VOLTAGE COMPARATOR					
Threshold Voltage	High to Low, Other Input at 5V		1.425		V
	Low to High, Other Input at 5V		1.50		V
Input Bias Current	Input = 1V, Other Input at 5V		0.25	1	µA
PARK/INHIBIT					
Park/Inhibit Threshold			1.3		V
Park/Inhibit Input Current	At Threshold		70		µA
Park Drive Sat V	I_{OUT} = 100 mA		0.7		V
Parking Drive Leakage	V_{OUT} = 35V			50	µA

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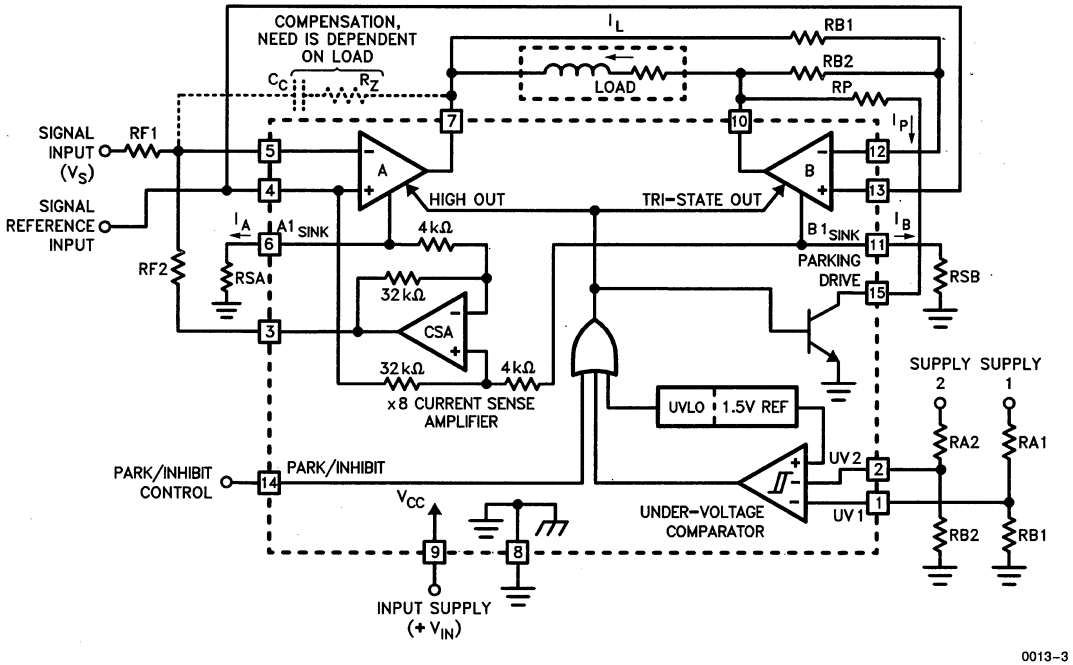
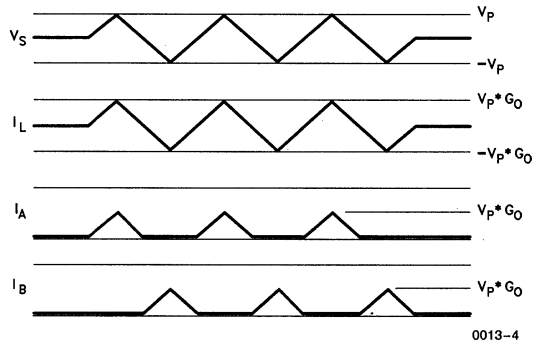
APPLICATION AND OPERATION INFORMATION

The UC3176 in a Full Bridge Transconductance Amplifier



0013-3

Waveforms for Above Application



0013-4

Design Equations

Transconductance $(G_O) = \frac{I_L}{V_S} = \frac{R_{F2}}{R_{F1}} \frac{1}{8 * R_S}$

With: $R_{SA} = R_{SB} = R_S$, and $R_{B1} = R_{B2}$

Parking Current $(I_P) = (+V_{IN} - 1.5V)/(R_P + R_L)$

Where: R_L = Load DC Impedence

Under-Voltage Thresholds, at Supplies

High to Low Threshold, $(V_{LH}) = 1.425\ (R_A + R_B)/R_B$

Low to High Threshold, $(V_{HL}) = 1.5\ (R_A + R_B)/R_B$

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LINEAR INTEGRATED CIRCUITS

Switchmode Driver For 3-ϕ Brushless DC Motors

FEATURES

- 2A Continuous, 3A Peak Output Current
- 8V to 40V Operation
- Internal High Gain Amplifier for Servo Applications
- TTL Compatible Hall Inputs
- Mask Programmable Decode Logic
- Pulse-by-Pulse Current Limiting
- Internal Thermal Shutdown Protection
- Under-Voltage Lockout
- 15 Lead, 25W Multiwatt® Package

DESCRIPTION

The UC3620 is a brushless DC motor driver capable of decoding and driving all 3 windings of a 3-phase brushless DC motor. In addition, an on-board current comparator, oscillator, and high gain Op-Amp provide all necessary circuitry for implementing a high performance, chopped mode servo amplifier. Full protection, including thermal shutdown, pulse-by-pulse current limiting, and under-voltage lockout aid in the simple implementation of reliable designs. Both conducted and radiated EMI have been greatly reduced by limiting the output dv/dt to 150V/μs for any load condition.

The UC3620 offers standard 60 mechanical degree, four-pole, hall decoding per Table 1. Other decoding options are available via mask programming at the factory.

4

ABSOLUTE MAXIMUM RATINGS (Note 1)

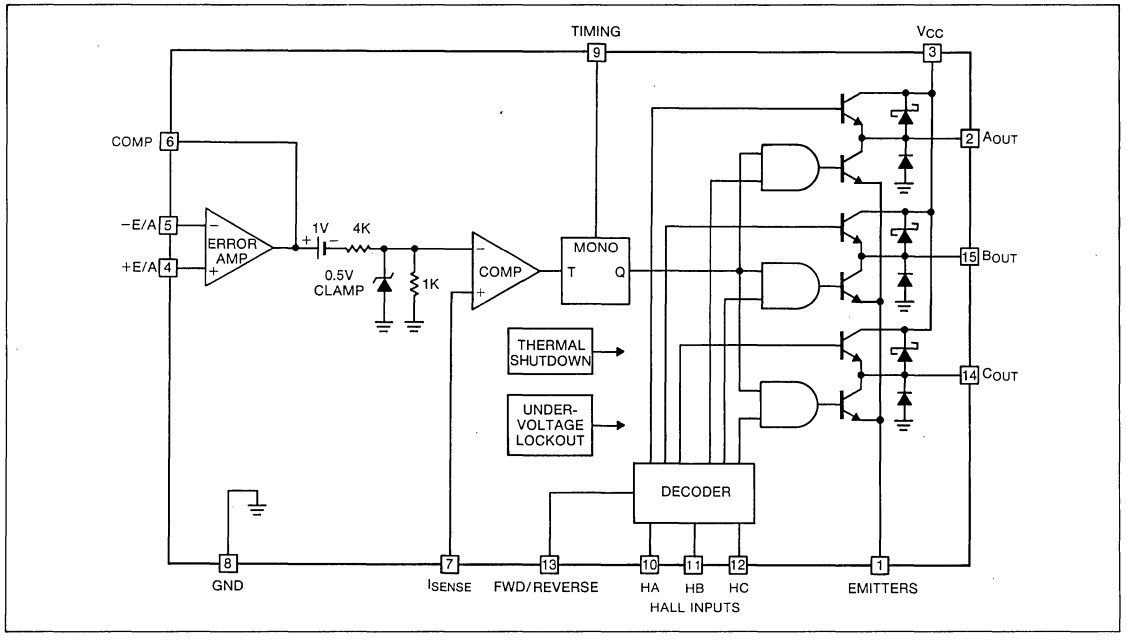
Supply Voltage, V_{cc} 40V
Output Current, Source or Sink
  Non-Repetitive (t = 100μsec), I_O 3A
  Repetitive (80% on - 20% off; t_{ON} = 10ms) 2.5A
  DC Operation 2A
Analog Inputs..... -0.3 to $+V_{cc}$
Logic Inputs ..... -0.3 to $+V_{cc}$
Total Power Dissipation (at T_{CASE} = 75°C) 25W
Storage and Junction Temperature..... -40°C to +150°C

Note: 1. All voltages are with respect to ground, pin 8. Currents are positive into, negative out of the specified terminal.

THERMAL DATA

Thermal Resistance Junction-Case, θ_{jc} ..... 3°C/W Max
Thermal Resistance Junction-Ambient, θ_{ja} ..... 35°C/W Max

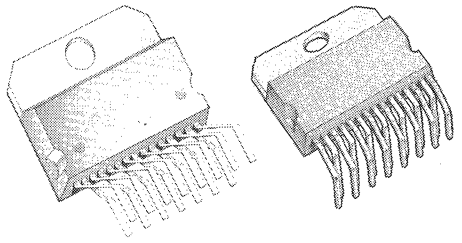
BLOCK DIAGRAM



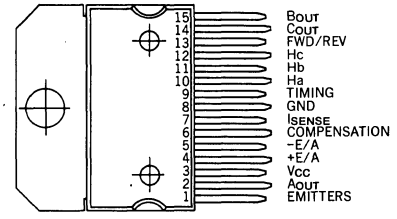
UNITRODE

MECHANICAL DATA

V Package **VH Package**



CONNECTION DIAGRAM (TOP VIEW)



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C; $V_{cc(PIN\ 3)}$ = 20V, R_T = 10k, C_T = 2.2nF)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Error Amplifier Section					
Input Offset Voltage			1.5	10	mV
Input Bias Current			−.25	−2.0	μA
Input Offset Current			15	250	nA
Common Mode Range	V_{cc} = 8V to 40V	0		V_{IN}-2	V
Open Loop Gain	$\Delta V_{PIN\ 6}$ = 1V to 4V	80	100		dB
Unity Gain Bandwidth	T_j = 25°C, Note 2		0.8		MHz
Output Sink Current	$V_{PIN\ 6}$ = 1V		2		mA
Output Source Current	$V_{PIN\ 6}$ = 4V		8		mA
Current Sense Section					
Input Bias Current			−2.0	−5	μA
Internal Clamp		.425	0.5	.575	V
Divider Gain		.180	0.2	.220	V/V
Internal Offset Voltage		.8	1.0	1.2	V
Timing Section					
Output Off Time		18	20	22	μs
Upper Mono Threshold			5.0		V
Lower Mono Threshold			2.0		V
Decoder Section					
High-Level Input Voltage		2.2			V
Low-Level Input Voltage				0.8	V
High-Level Input Current				10	μA
Low-Level Input Current		−10			μA
Output Section					
Output Leakage Current	V_{cc} = 40V			500	μA
V_F, Schottky Diode	I_o = 2A		1.5	2.0	V
V_F, Substrate Diode	I_o = 2A		2.2	3.0	V
Total Output Voltage Drop	I_o = 2A, Note 3		3.0	3.6	V
Output Rise Time	I_o = 2A		150		ns
Output Fall Time	I_o = 2A		150		ns

Notes: 2. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
3. The total voltage drop is defined as the sum of both top and bottom side driver.

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ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C; $V_{cc(PIN\ 3)}$ = 20V, R_T = 10k, C_T = 2.2nF)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Under-Voltage Lockout					
Start-Up Threshold				8.0	V
Threshold Hysteresis			0.5		V
Thermal Shutdown					
Junction Temperature		150		180	°C
Total Standby Current					
Supply Current				55	mA

TABLE 1

STEP	FWD/ REV	Ha	Hb	Hc		AOUT	BOUT	COUT
1	1	1	0	1		H	L	0
2	1	1	0	0		H	0	L
3	1	1	1	0		0	H	L
4	1	0	1	0		L	H	0
5	1	0	1	1		L	0	H
6	1	0	0	1		0	L	H
1	0	1	0	1		L	H	0
2	0	1	0	0		L	0	H
3	0	1	1	0		0	L	H
4	0	0	1	0		H	L	0
5	0	0	1	1		H	0	L
6	0	0	0	1		0	H	L

H = HIGH OUTPUT
L = LOW OUTPUT
O = OPEN OUTPUT

4

CIRCUIT DESCRIPTION

The UC3620 is designed for implementation of a complete 3-Φ brushless DC servo drive using a minimum number of external components. Below is a functional description of each major circuit feature.

DECODER

Table 1 shows the decoding scheme used in the UC3620 to decode and drive each of three high current totem pole output stages. A forward/reverse signal, pin 13, is used to provide direction. At any point in time, one driver is sourcing, one driver is sinking, and the remaining driver is off or tri-stated. Pulse width modulation is accomplished by turning the sink driver off during the monostable reset time, producing a fixed off-time chop mode. Controlled output rise and fall times help reduce electrical switching noise while maintaining relatively small switching losses.

CURRENT SENSING

Referring to Figure 1, emitter current is sensed across R_S and fed back through a low pass filter to the current sense pin 7. This filter is required to eliminate false triggering of the monostable due to leading edge current spikes. Actual filter values, although somewhat dependent on external loads, will generally be in the 1KΩ and 1000pF range.

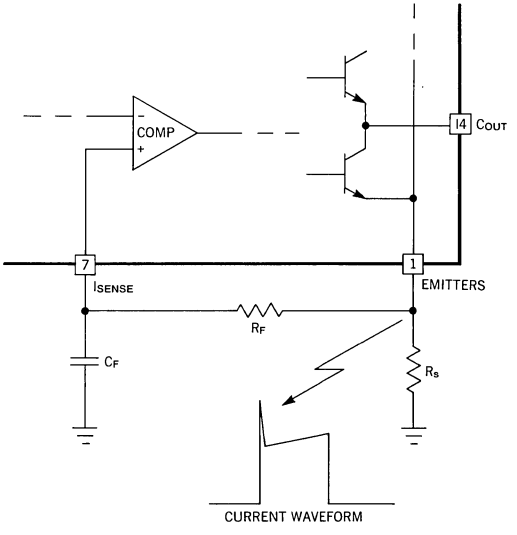


Figure 1. Current Sense Filter

TIMING

An R-C time constant on pin 9 is used by the monostable to generate a fixed off time at the outputs according to the formula:

$T_{OFF} = .916\ R_T C_T$

As the peak current in the emitters approaches the value at the minus (−) input of the on-board comparator, the monostable is triggered, causing the outputs to be turned off. On time is determined by the amount of time required for motor current to increase to the value required to re-trip the monostable. A timing sequence of these events is shown in Figure 2.

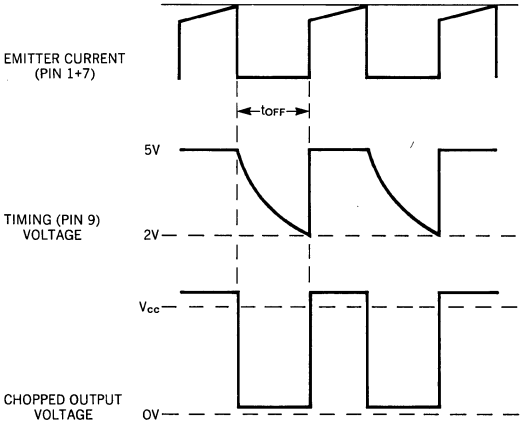


Figure 2. Chopped Mode Timing Diagram

CURRENT LIMIT

Since peak current is being controlled at all times by the internal comparator, a simple voltage clamp at its negative (−) input will limit peak current to a maximum value. A fixed 0.5V internal clamp has been included on the UC3620, and any current spike in the output which generates a sensed voltage greater than 0.5V will immediately shut down the outputs. Actual peak current values may be programmed by selecting the appropriate value of R_S according to the formula:

$$R_S = 0.5/I_{CURRENT\ LIMIT}$$

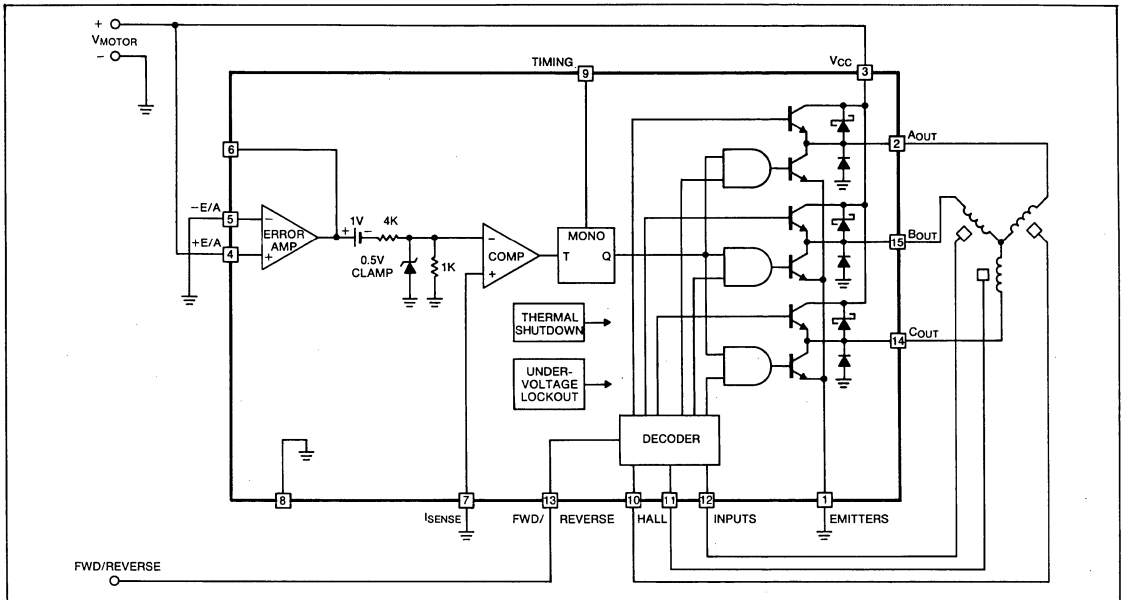
ERROR AMPLIFIER

A high performance, on-board error amplifier is included to facilitate implementing closed loop motor control. Error voltage generation and loop compensation are easily accomplished by appropriately configuring the gain and feedback of this amplifier. To provide a larger dynamic signal range at the output of the error amplifier, a divide by 5 resistor network is used to reduce the error signal level before applying to the internal comparator. In addition, a one volt offset has been introduced at the output of the error amplifier to guarantee control down to zero current in the output stages. Since this offset is divided by the open loop gain of the feedback loop, it has virtually no effect on closed loop performance.

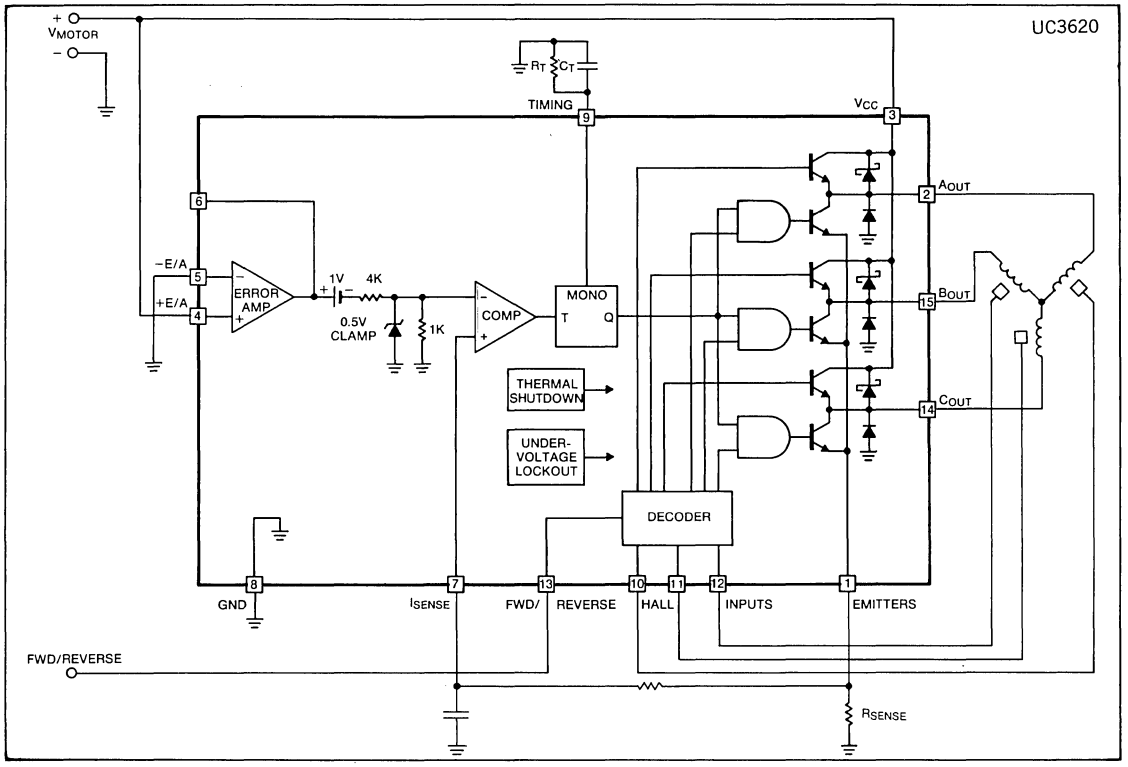
PROTECTION FUNCTIONS

Protective functions including under-voltage lockout, peak current limiting, and thermal shutdown, provide an extremely rugged device capable of surviving under many types of fault conditions. Under-voltage lockout guarantees the outputs will be off or tri-stated until V_{CC} is sufficient for proper operation of the chip. Current limiting limits the peak current for a stalled or shorted motor, whereas thermal shutdown will tri-state the outputs if a temperature above 150°C is reached.

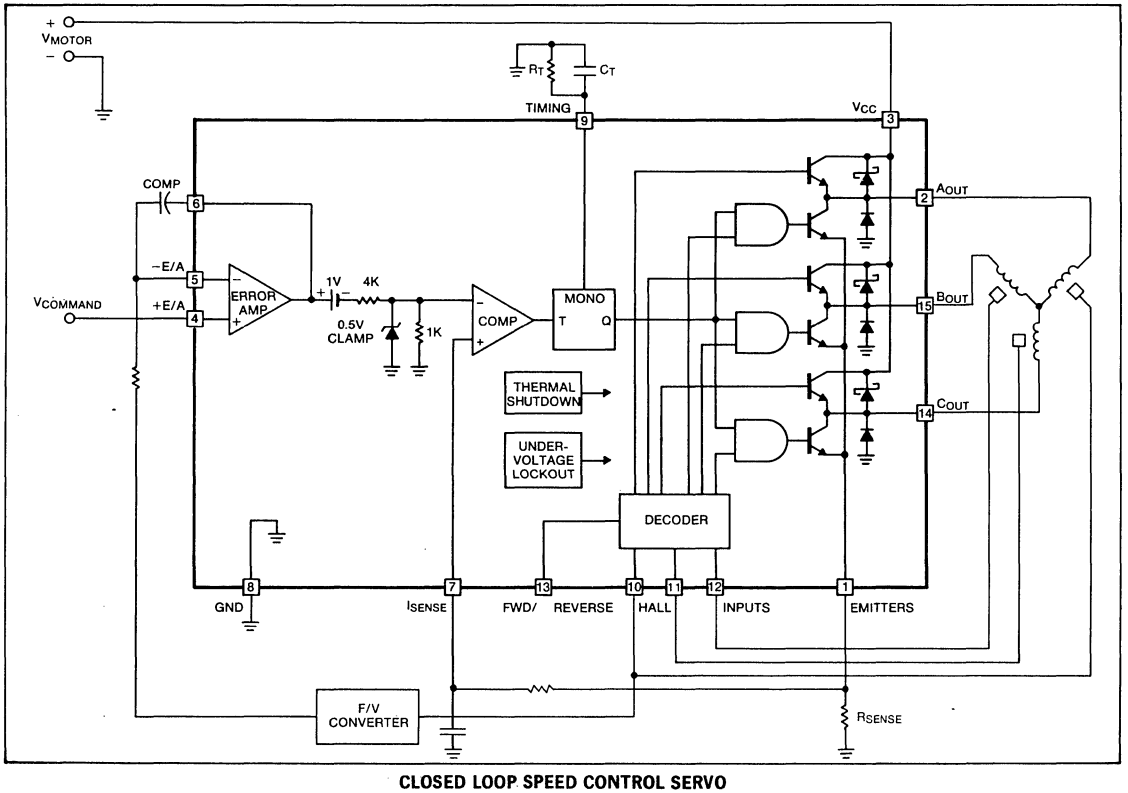
TYPICAL APPLICATIONS



3-ϕ BRUSHLESS DC OPEN LOOP MOTOR DRIVE



3-ϕ BRUSHLESS DC OPEN LOOP MOTOR DRIVE WITH CURRENT LIMIT



CLOSED LOOP SPEED CONTROL SERVO

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LINEAR INTEGRATED CIRCUITS

Switchmode Driver For 3-ϕ Brushless DC Motors

FEATURES

- 2A Continuous, 3A Peak Output Current
- 8V to 40V Operation
- Fixed-Frequency Pulse-Width Modulation for Servo Applications
- TTL Compatible Hall Inputs
- Pulse-by-Pulse Current Limiting
- Internal Thermal Shutdown Protection
- Under-Voltage Lockout
- 15 Lead, 25W Multiwatt® Package

DESCRIPTION

The UC3622 is a brushless DC motor driver capable of decoding and driving all 3 windings of a 3-phase brushless DC motor. In addition, an on-board oscillator and latched PWM comparator provide the necessary circuitry for implementing a fixed-frequency, pulse width modulated servo amplifier. Full protection, including thermal shutdown, pulse-by-pulse current limiting, and under-voltage lockout aid in the simple implementation of reliable designs. Both conducted and radiated EMI have been reduced by limiting the output dv/dt to 150μs for any load condition.

The UC3622 will decode and drive all 3-phase motors with hall decode schemes compatible with Table 1. All other schemes can be decoded with the addition of a single external inverter.

ABSOLUTE MAXIMUM RATINGS (Note 1)

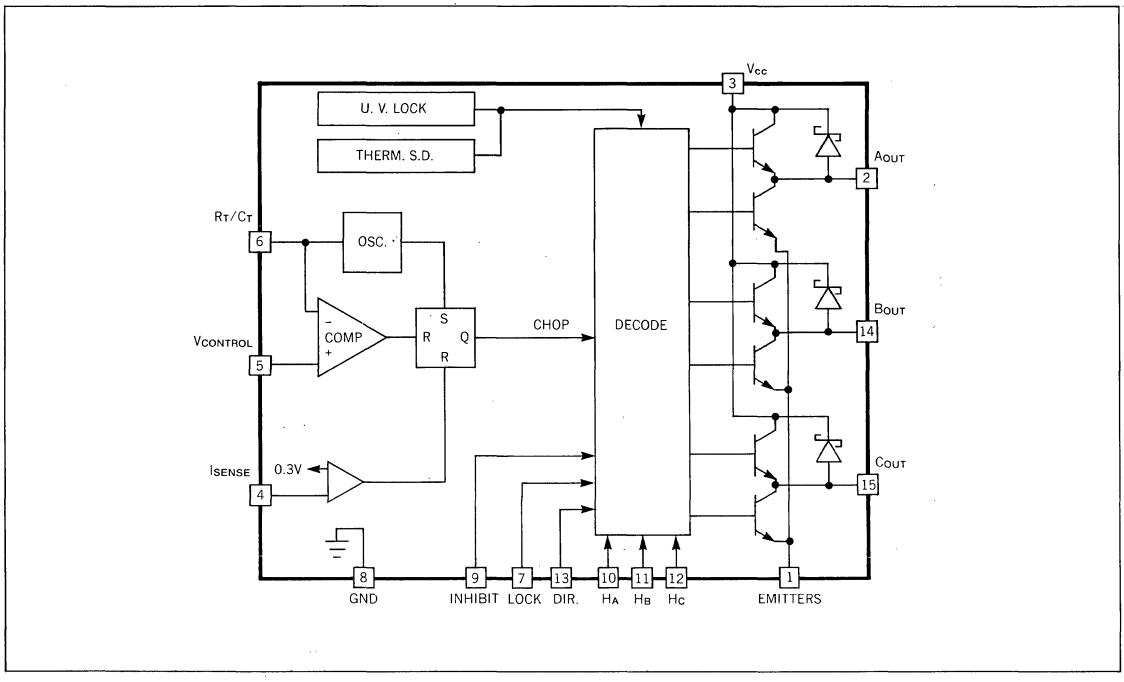
Supply Voltage, V_{cc} 40V
Output Current, Source or Sink
  Non-Repetitive (t = 100μsec), I_O 3A
  Repetitive (80% on - 20% off; t_{ON} = 10ms) 2.5A
  DC Operation 2A
Analog Inputs ..... −0.3 to +V_{cc}
Logic Inputs ..... −0.3 to +V_{cc}
Total Power Dissipation (at T_{CASE} = 75°C) 25W
Storage and Junction Temperature ..... −40°C to +150°C

Note: 1. All voltages are with respect to ground, pin 8. Currents are positive into, negative out of the specified terminal.

THERMAL DATA

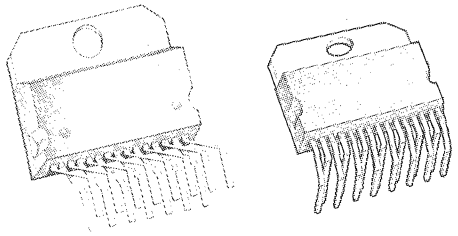
Thermal Resistance Junction-Case, θ_{jc} ..... 3°C/W Max
Thermal Resistance Junction-Ambient, θ_{ja} ..... 35°C/W Max

BLOCK DIAGRAM

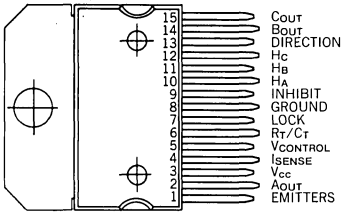


MECHANICAL DATA

V Package **VH Package**



CONNECTION DIAGRAM (TOP VIEW)



4

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C; $V_{cc(PIN\ 3)}$ = 20V, R_T = 47k, C_T = .015μF)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
PWM Comparator Section					
Input Offset Voltage				10	mV
Input Bias Current				5	μA
Current Sense Section					
Input Bias Current				5	μA
Internal Offset Voltage		.25	0.3	.35	V
Oscillator Section					
Initial Accuracy	T_j = 25°C	9	10	11	kHz
Temperature Stability	Over Operating Range		2		%
Ramp Peak			3.3		V
Ramp Valley			1.3		V
Decoder Section					
High-Level Input Voltage		2.5			V
Low-Level Input Voltage				0.8	V
High-Level Input Current				10	μA
Low-Level Input Current		−10			μA
Output Section					
Output Leakage Current	V_{cc} = 40V			500	μA
V_F, Schottky Diode	I_o = 2A		1.5	2.0	V
Total Output Voltage Drop	I_o = 2A, Note 3		3.0	3.6	V
Output Rise Time	I_o = 2A		150		ns
Output Fall Time	I_o = 2A		150		ns
Under-Voltage Lockout					
Start-Up Threshold				8.0	V
Threshold Hysteresis			0.5		V
Thermal Shutdown					
Junction Temperature		150		180	°C
Total Standby Current					
Supply Current				55	mA

Notes: 2. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
3. The total voltage drop is defined as the sum of both top and bottom side driver.

TABLE 1

STEP	INHIBIT	DIR	H_a	H_b	H_c	LOCK		A_{OUT}	B_{OUT}	C_{OUT}
1	0	1	1	0	0	1		ϕ	H	L
2	0	1	1	1	0	1		L	H	ϕ
3	0	1	1	1	1	1		L	ϕ	H
4	0	1	0	1	1	1		ϕ	L	H
5	0	1	0	0	1	1		H	L	ϕ
6	0	1	0	0	0	1		H	ϕ	L
1	0	0	1	1	1	1		H	ϕ	L
2	0	0	1	1	0	1		H	L	ϕ
3	0	0	1	0	0	1		ϕ	L	H
4	0	0	0	0	0	1		L	ϕ	H
5	0	0	0	0	1	1		L	H	ϕ
6	0	0	0	1	1	1		ϕ	H	L
—	1	X	X	X	X	X		ϕ	ϕ	ϕ
—	0	X	X	X	X	0		H	ϕ	L

H = HIGH OUTPUT L = LOW OUTPUT ϕ = OPEN (TRISTATE) OUTPUT

CIRCUIT DESCRIPTION

The UC3622 is designed for implementation of a complete 3-phase brushless DC servo drive using a minimum number of external components. Below is a functional description of each major circuit feature.

DECODER

Table 1 shows the logic scheme employed to decode and drive each of three high current, totem pole, output stages. A forward/reverse signal, Pin 13, is used to provide direction. At any time, one driver is sourcing, one driver is sinking, and the remaining driver is off or tri-stated. Pulse width modulation is accomplished by chopping all drivers during current control (fixed-frequency PWM), producing a four-quadrant, regenerative mode drive. Controlled output rise and fall times help reduce electrical switching noise while maintaining relatively small switching losses.

HALL INPUTS

The Hall input pins (#10, 11, 12) are not provided with internal pull-up resistors. If these are required for the Hall devices, they must be added externally.

CURRENT LIMIT

Referring to Figure 1, emitter current is sensed across R_{LIMIT} and fed back through a low pass filter to the current sense, Pin 4. This filter is required to eliminate false triggering of the monostable due to leading edge current spikes. Actual filter values, although somewhat dependent on external loads, will generally be in the 1k and 1000pF range. An internal 0.3V reference voltage limits the motor current to

$$I_{max} = \frac{0.3}{R_{LIMIT}}$$

TIMING

An RC circuit at Pin 6 is used to set the PWM frequency, as shown in Figure 2. The frequency is determined by the formula

$$f \approx \frac{V_{OSC} - 2.37}{2.4\ R_T\ C_T}\ [\text{Hz}]$$

Note: R_T should be chosen so that

$$50\mu A < \frac{V_{OSC} - 2.4}{R_T} < 1mA$$

INHIBIT

The INHIBIT input (Pin 9) must be low during normal operation. A high level at this pin forces all three outputs to the open state, and can be used to allow the motor to coast.

LOCK

A low level at LOCK (Pin 7), together with a low level at INHIBIT, sets the following output condition:

A_{OUT} _ _ _ _ _ _ _ HIGH
B_{OUT} _ _ _ _ _ _ _ OPEN
C_{OUT} _ _ _ _ _ _ _ LOW

This can be used as part of a circuit intended to force the motor shaft to a desired parking position.

PROTECTION FUNCTIONS

Protective functions including under-voltage lockout, peak current limiting, and thermal shutdown, provide an extremely rugged device capable of surviving under many types of fault conditions. Under-voltage lockout guarantees the outputs will be off or tri-stated until V_{CC} is sufficient for proper operation of the chip. Current limiting limits the peak current for a stalled or shorted motor, whereas thermal shutdown will tri-state the outputs if a temperature above 150°C is reached.

APPLICATION MATERIAL

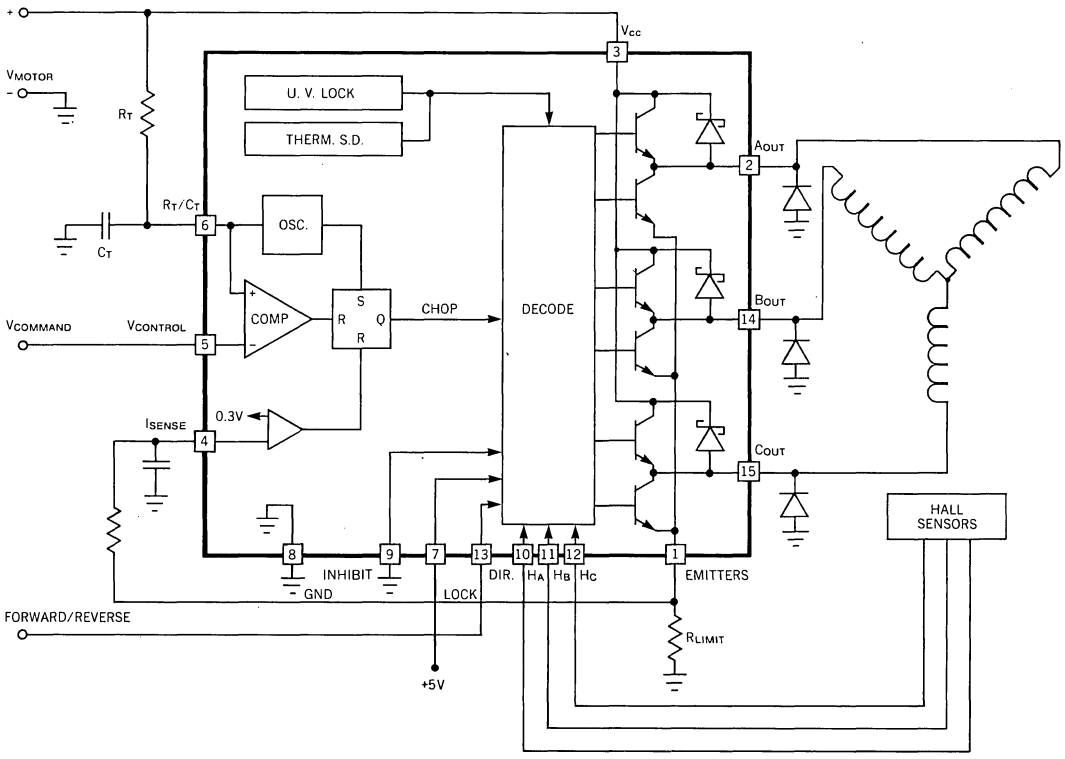


Figure 1. Open Loop Speed Control with Current Limiting

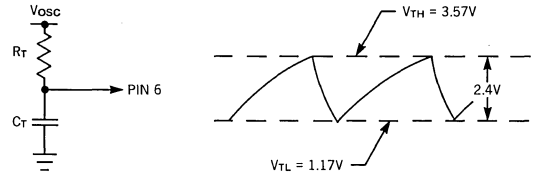


Figure 2. PWM Oscillator Waveform

LINEAR INTEGRATED CIRCUITS

UC3657

Triple Tri-State Power Driver

PRELIMINARY

FEATURES

- Operating Supply Voltage to 32V
- Load Current Capability to 3A
- Built-In Thermal Protection
- Clamp Diodes Included for Driving Inductive Loads
- 25W Multiwatt® Power-Tab Package
- Individual Logic Inputs for Each Driver
- Master Inhibit Input for Power-Down and Coast
- TTL/CMOS Compatible Inputs

DESCRIPTION

The UC3657 triple power driver integrated circuit is well suited to driving three-phase motors, stepper motors, brush motors, inductors, incandescent lamps, resistive loads and long lines with controlled voltage slew rates. The UC3657 features minimum saturation voltage with light loads as well as low saturation voltage for loads in excess of 2A.

Each output contains two clamp diodes to conduct transient currents from inductive loads. The diode to V_{CC} is a fast, low voltage-drop Schottky type, while the diode to ground is a slower P-N junction device.

The UC3657 is completely safe from destruction due to incorrect combinations of logic inputs. For best performance, however, it is recommended that the inputs are driven with logic signals that have transition times faster than 100nS.

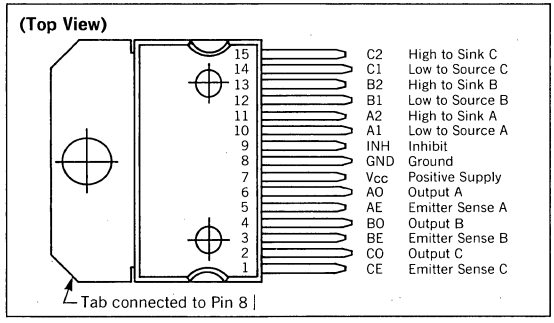
ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage 35V
Logic Input Voltage ..... -0.3 to +35V
Peak Output Current (each channel)
  Non-Repetitive 100μS 3A
  Repetitive, 8mS on, 2mS off 2.5A
  Continuous 2A
Total Power Dissipation, T_{TAB} = 75°C 25W
Derate for T_{TAB} > 75°C ..... 0.3W/°C
Storage and Junction Temperature ..... -40°C to +150°C

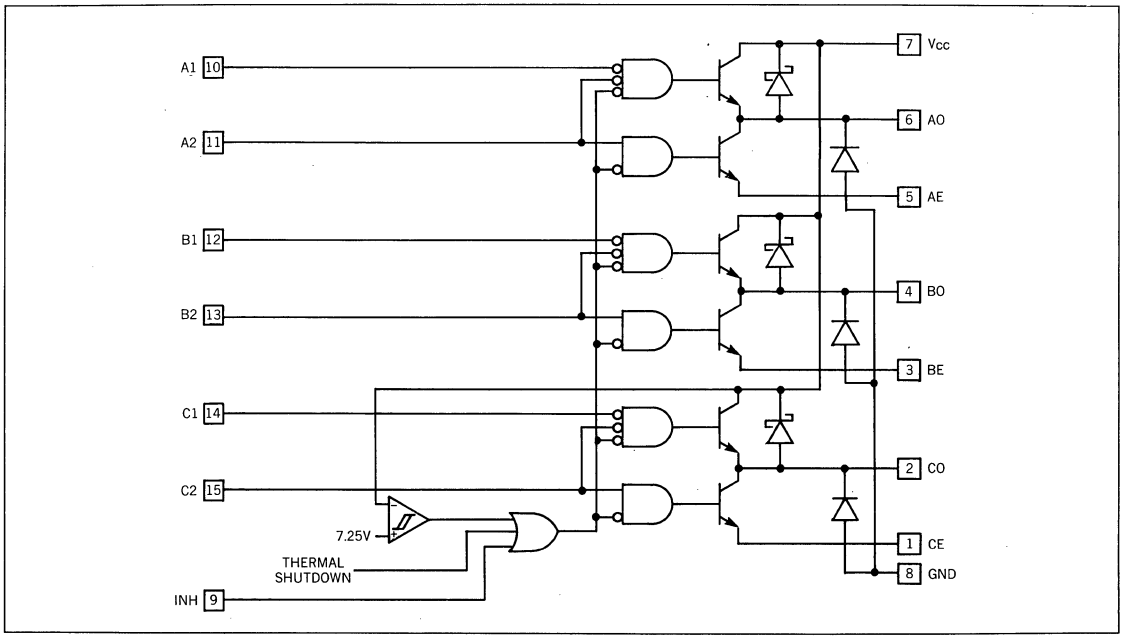
THERMAL DATA

Thermal Resistance, Junction to Case ..... 3°C/W
Thermal Resistance, Junction to Ambient ..... 35°C/W

CONNECTION DIAGRAM



BLOCK DIAGRAM



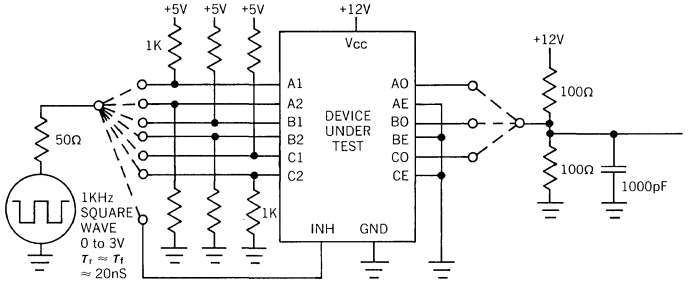
UNITRODE

ELECTRICAL CHARACTERISTICS (0°C < T_A < 70°C, V_{CC} = 12V unless otherwise noted.)

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
I_{CC}, Outputs Off	A1, B1, C1 = H A2, B2, C2 = L INH = L			10	25	mA
I_{CC}, Outputs High	A1, B1, C1 = L A2, B2, C2 = L INH = L			10	28	mA
I_{CC}, Outputs Low	A1, B1, C1 = L A2, B2, C2 = H INH = L			40	70	mA
I_{CC}, Chip Inhibited	INH = H			0.5	5	mA
I_{CC}, One Output Low 2A	A2, B2, C2 = H INH = L			100		mA
V_{CC} Range, Operating			8		32	V
Turn-On Threshold				7.5	8	V
Turn-Off Threshold				7.0		V
Thermal Shutdown Temperature				170		°C
Thermal Recovery Temperature				160		°C
Logic Input Threshold			0.8		2.0	V
Input Low Current; A1, A2, B1, B2, C1, C2	at 0.0V			4	20	μA
Inhibit Low Current; INH	at 0.0V				20	μA
Input High Current; A1, A2, B1, B2, C1, C2	at 3.0V				10	μA
Inhibit High Current; INH	at 3.0V			0.2	1	mA
Output Low Voltage	A2, B2, C2 = H INH = L	100mA		.07	.12	V
	AE, BE, CE Grounded	1A		.37	.75	V
		2A		.7	1.25	V
Output High Voltage, to V_{CC}	A1, B1, C1 = L INH = L	100mA		−.9	−1.3	V
	A2, B2, C2 = L	1A		−1.2	−1.5	V
		2A		−1.5	−1.9	V
Propagation Delay, Off-High	Test Circuit, Drive A1, B1, or C1			.1		μS
Propagation Delay, Off-Low	Test Circuit, Drive A2, B2, or C2			3.2		μS
Propagation Delay, High-Low	Test Circuit, Drive A1+A2, B1+B2, or C1+C2			.25		μS
Propagation Delay, Low-High	Test Circuit, Drive A1+A2, B1+B2, or C1+C2			.51		μS
Propagation Delay, High-Off	Test Circuit, Drive A1, B1, or C1			.4		μS
Propagation Delay, Low-Off	Test Circuit, Drive A2, B2, or C2			.35		μS
Propagation Delay, Low-Inhibit	Test Circuit, Drive INH			1.5		μS
Propagation Delay, Inhibit-Low	Test Circuit, Drive INH			.6		μS
Propagation Delay, High-Inhibit	Test Circuit, Drive INH			2.5		μS
Propagation Delay, Inhibit-High	Test Circuit, Drive INH			.5		μS
Output Slew Rate, Output Rising	100Ω Load to GND; Drive A1+A2, B1+B2, or C1+C2			50		V/μS
Output Slew Rate, Output Falling	100Ω Load to V_{CC}; Drive A1+A2, B1+B2, or C1+C2			50		V/μS
Output Leakage Current	INH = H, V_{CC} = 32V, 0V < V_{OUT} < 32V		−250		250	μA
High-Side Diode 2A Drop	INH = H			1.3	2	V
Low-Side Diode 2A Drop	INH = H			1.6	3	V

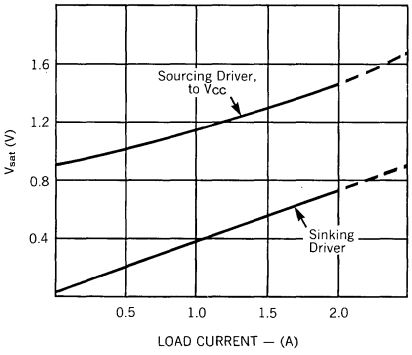
PROPAGATION DELAY TEST CIRCUIT

Connect only one channel at a time.

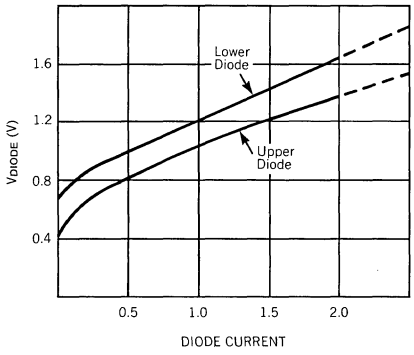


TYPICAL CHARACTERISTICS, 25°C, 12V

Saturation Voltage



Diode Voltage

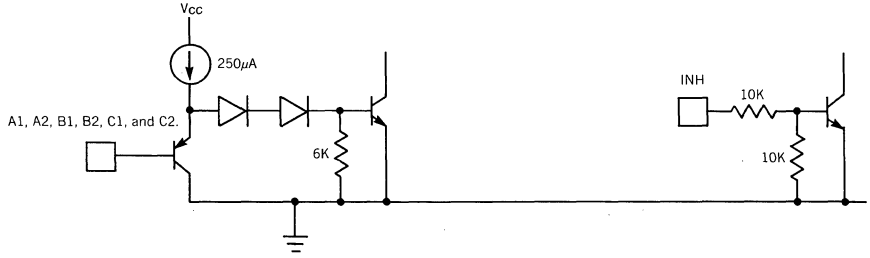


LOGIC TRUTH TABLE

Input 1	Input 2	INH	Output
X	X	H	Off
H	L	X	Off
L	L	L	High
X	H	L	Low

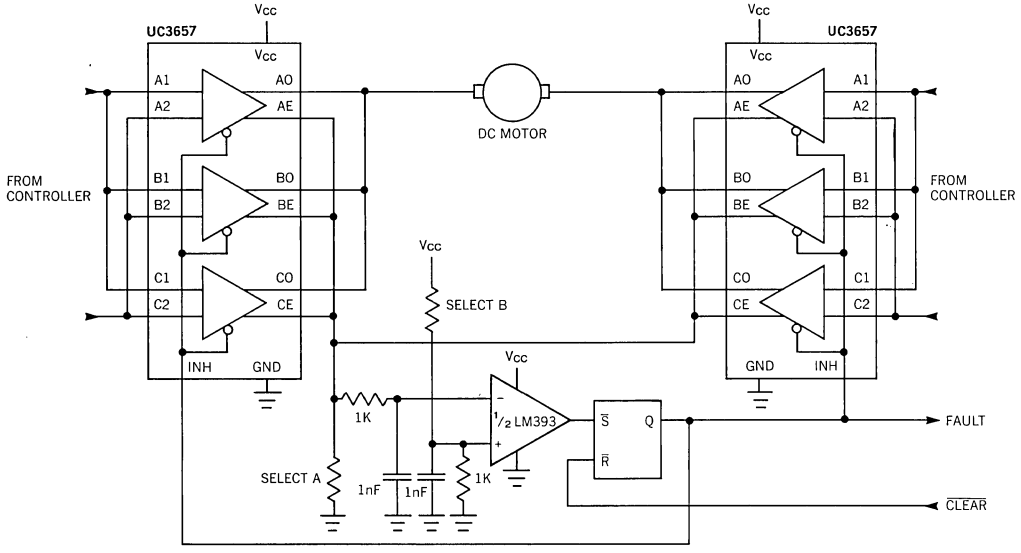
L means input voltage < 0.8V.
H means input voltage > 2.0V.
Off means output is high impedance.
Low means output is low impedance to "E."
High means output is low impedance to "V_{CC}."
X means input voltage will not affect the output (don't care).

EQUIVALENT INPUT CIRCUIT



TYPICAL APPLICATIONS

DC BRUSH MOTOR DRIVER WITH FAULT LATCH

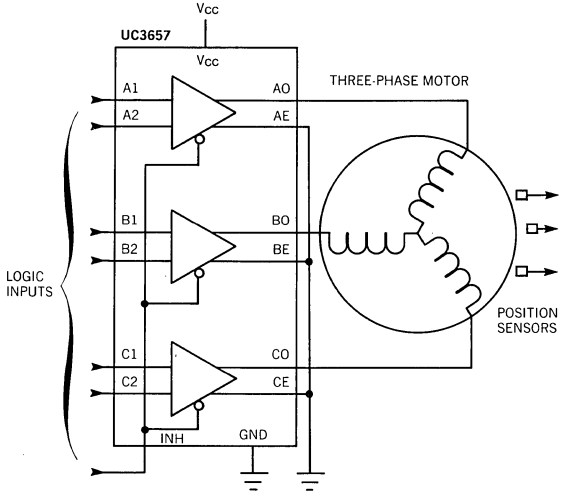


DC Brush Motor Driver with Fault Latch

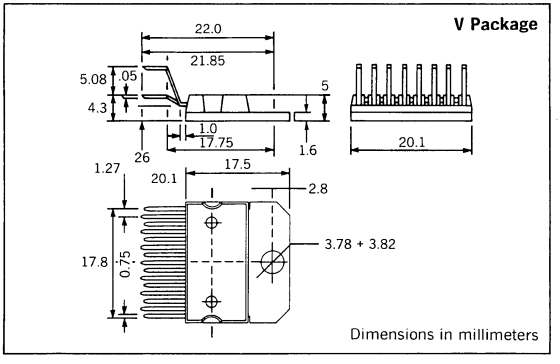
This application features a fault latch to detect a shorted wire, stuck rotor, or other problem that can cause current to exceed some threshold. A single sense resistor is used with a voltage comparator to detect this fault. Emitter resistor "A" is used to sense total low-side current, and inhibit all devices in the event that current exceeds a threshold. Resistor "B" sets the comparator threshold, and a set-reset flip-flop latches the error signal to prevent oscillation. Matched RC filters on the comparator inputs allow operation close to threshold with good supply-noise rejection.

To achieve high currents, UC3657 outputs have been paralleled. This is practical within the device current and power ratings, according to the derating specification for the package.

BRUSHLESS MOTOR DRIVER



MECHANICAL DATA



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LINEAR INTEGRATED CIRCUITS

Stepper Motor Drive Circuit

FEATURES

- Full-Step, Half-Step and Micro-Step Capability
- Bipolar Output Current up to 1A
- Wide Range of Motor Supply Voltage 10-46V
- Low Saturation Voltage with Integrated Bootstrap
- Built-In Fast Recovery Commutating Diodes
- Current Levels Selected in Steps or Varied Continuously
- Thermal Protection with Soft Intervention

DESCRIPTION

The UC3717A is an improved version of the UC3717, used to switch drive the current in one winding of a bipolar stepper motor. The UC3717A has been modified to supply higher winding current, more reliable thermal protection, and improved efficiency by providing integrated bootstrap circuitry to lower recirculation saturation voltages. The diagram shown below presents the building blocks of the UC3717A. Included are an LS-TTL compatible logic input, a current sensor, a monostable, a thermal shutdown network, and an H-bridge output stage. The output stage features built-in fast recovery commutating diodes and integrated bootstrap pull up. Two UC3717As and a few external components form a complete control and drive unit for LS-TTL or micro-processor controlled stepper motor systems.

The UC3717A is characterized for operation over the temperature range of 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage
- Logic Supply, V_{CC} 7V
- Output Supply, V_m 50V

Input Voltage
- Logic Inputs (Pins 7, 8, 9) 6V
- Analog Input (Pin 10) ..... V_{CC}
- Reference Input (Pin 11) 15V

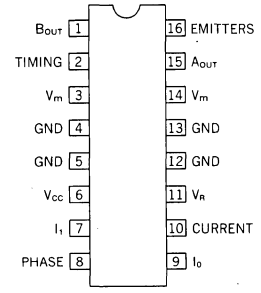
Input Current
- Logic Inputs (Pins 7, 8, 9) ..... -10mA
- Analog Inputs (Pins 10, 11) ..... -10mA

Output Current (Pins 1, 15) ..... ±1.2A
Junction Temperature, T_j ..... +150°C
Thermal Resistance, Junction to Ambient (NE Package) ..... 45°C/W
Thermal Resistance, Junction to Case (NE Package) ..... 11°C/W
Thermal Resistance, Junction to Ambient (J Package) ..... 100°C/W
Thermal Resistance, Junction to Case (J Package) ..... 60°C/W
Storage Temperature Range, T_S ..... -55°C to +150°C

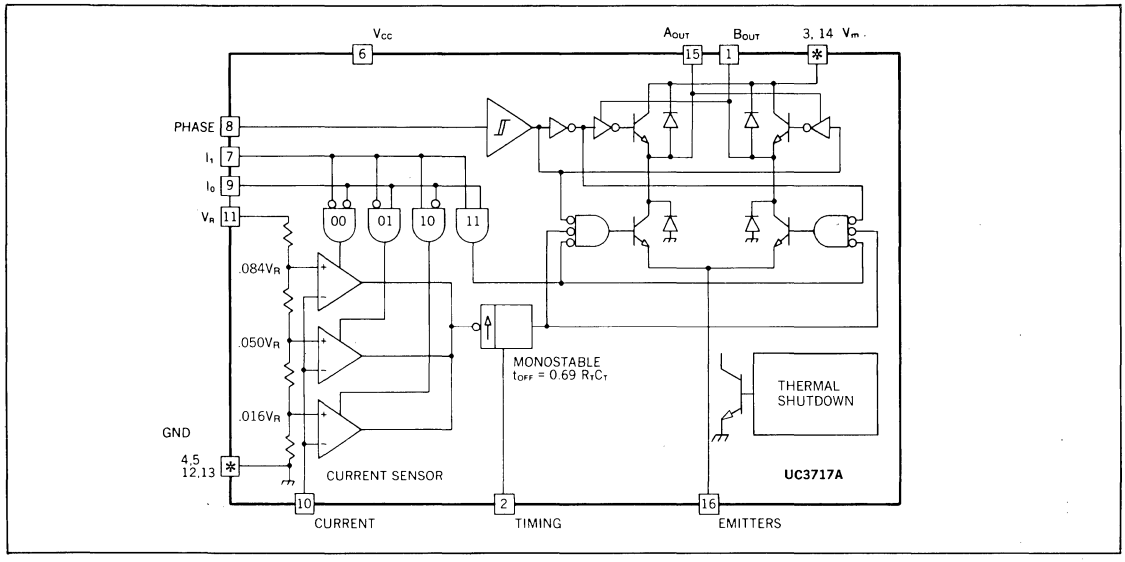
Note: 1. All voltages are with respect to ground, Pins 4, 5, 12, 13. Currents are positive into, negative out of the specified terminal.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or NE PACKAGE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, Figure 6. V_m = 36V, V_{CC} = 5V, V_R = 5V, T_A = 0°C to +70°C, unless otherwise stated).

PARAMETERS	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
Supply Voltage, V_m (Pins 3, 14)			10		46	V
Logic Supply Voltage, V_{CC} (Pin 6)			4.75		5.25	V
Logic Supply Current, I_{CC} (Pin 6)	$I_0 = I_1 = 0$			7	15	mA
Thermal Shutdown Temperature			+160		+180	°C
Logic Inputs						
Input Low Voltage (Pins 7, 8, 9)					0.8	V
Input High Voltage (Pins 7, 8, 9)			2		V_{CC}	V
Low Voltage Input Current (Pins 7, 8, 9)	V_i = 0.4V	Pin 8			-100	µA
		Pins 7, 9			-400	
High Voltage Input Current (Pins 7, 8, 9)	V_i = 2.4V				10	µA
Comparators						
Comparator Low Threshold Voltage (Pin 10)	V_R = 5V	I_0 = L, I_1 = H	66	80	90	mV
Comparator Medium Threshold Voltage (Pin 10)	V_R = 5V	I_0 = H, I_1 = L	236	250	266	mV
Comparator High Threshold Voltage (Pin 10)	V_R = 5V	I_0 = L, I_1 = L	396	420	436	mV
Comparator Input Current (Pin 10)					±20	µA
Cutoff Time, t_{OFF}	R_T = 56KΩ	C_T = 820pF	25		35	µs
Turn Off Delay, t_d	(See Figure 5)				2	µs
Source Diode-Transistor Pair						
Saturation Voltage, V_{sat} (Pins 1, 15)	I_m = -0.5A	Conduction Period		1.7	2.1	V
	(See Figure 5)	Recirculation Period		1.1	1.35	
Saturation Voltage, V_{sat} (Pins 1, 15)	I_m = -1A	Conduction Period		2.1	2.8	V
	(See Figure 5)	Recirculation Period		1.7	2.5	
Leakage Current	V_m = 40V				300	µA
Diode Forward Voltage V_F	I_m = -0.5A			1	1.25	V
	I_m = -1A			1.3	1.7	
Sink Diode-Transistor Pair						
Saturation Voltage, V_{sat} (Pins 1, 15)	I_m = 0.5A			1.1	1.35	V
	I_m = 1A			1.6	2.3	
Leakage Current	V_m = 40V				300	µA
Diode Forward Voltage V_F	I_m = 0.5A			1.1	1.5	V
	I_m = 1A			1.4	2	

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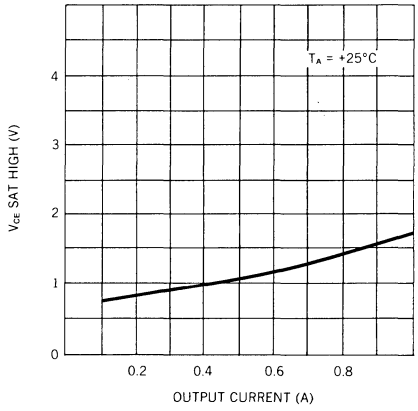

Figure 1. Typical Source Saturation Voltage vs Output Current (Recirculation Period)

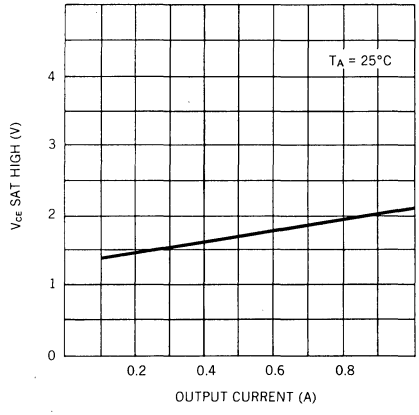

Figure 2. Typical Source Saturation Voltage vs Output Current (Conduction Period)

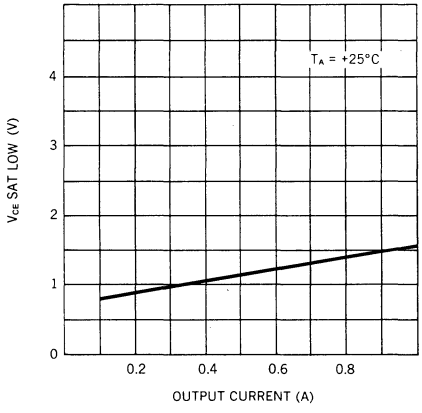

Figure 3. Typical Sink Saturation Voltage vs Output Current

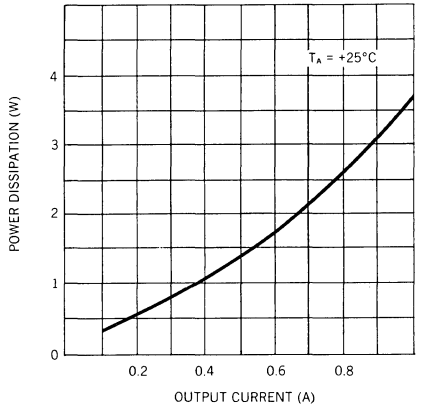

Figure 4. Typical Power Dissipation vs Output Current

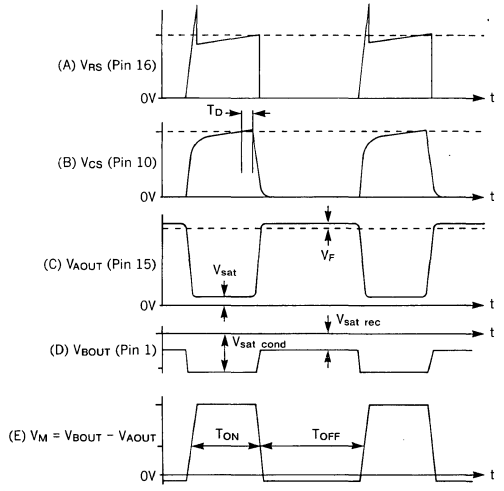

Figure 5. Typical Waveforms with MA Regulating (phase = 0)

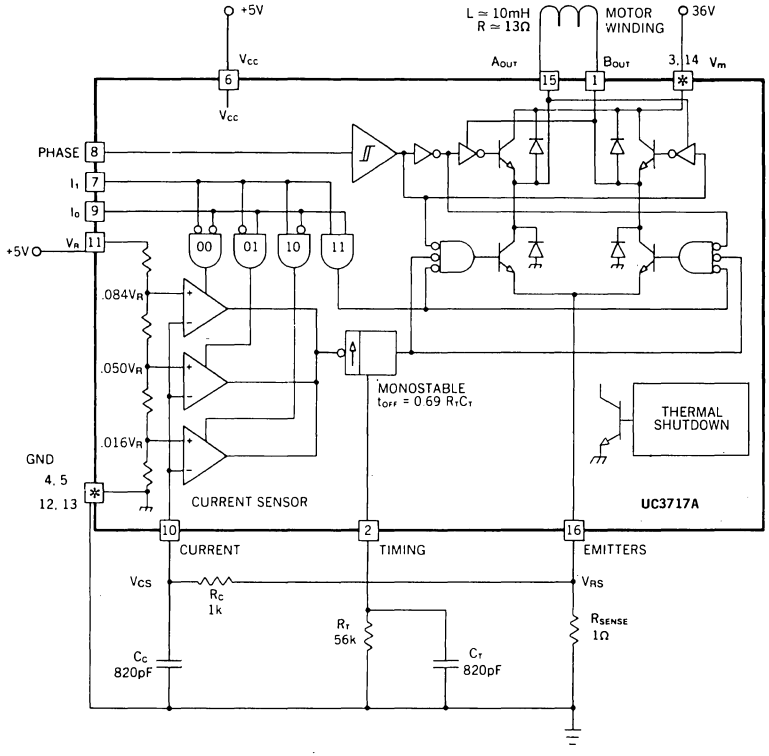

Figure 6. UC3717A Test Circuit

FUNCTIONAL DESCRIPTION

The UC3717A's drive circuit shown in the block diagram includes the following components:

(1) H-bridge output stage
(2) Phase polarity logic
(3) Voltage divider coupled with current sensing comparators
(4) Two-bit D/A current level select
(5) Monostable generating fixed off-time
(6) Thermal protection

OUTPUT STAGE

The UC3717A's output stage consists of four Darlington power transistors and associated recirculating power diodes in a full H-bridge configuration as shown in Figure 7. Also presented, is the new added feature of integrated bootstrap pull up, which improves device performance during switched mode operation. While in switched mode, with a low level phase polarity input, Q2 is on and Q3 is being switched. At the moment Q3 turns off, winding current begins to decay through the commutating diode pulling the collector of Q3 above the supply voltage. Meanwhile, Q6 turns on pulling the base of Q2 higher than its previous value. The net effect lowers the saturation voltage of source transistor Q2 during recirculation, thus improving efficiency by reducing power dissipation.

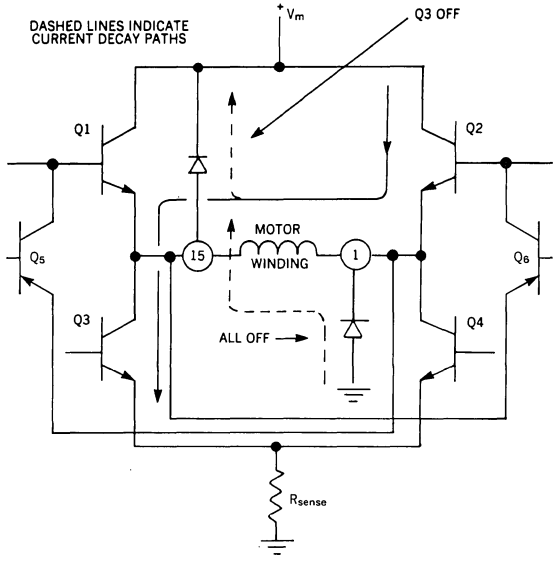

Figure 7. Simplified Schematic of Output Stage

PHASE POLARITY INPUT

The UC3717A phase polarity input controls current direction in the motor winding. Built-in hysteresis insures immunity to noise, something frequently present in switched-drive environments. A low level phase polarity input enables Q2 and Q3 as shown in Figure 7. During phase reversal, the active transistors are both turned off while winding current decays through the commutating diodes shown. As winding current decays to zero, the inactive transistors Q1 and Q4 turn on and charge the winding with current of the reverse direction. This delay insures noise immunity and freedom from power supply current spikes caused by overlapping drive signals.

PHASE INPUT	Q1, Q4	Q2, Q3
LOW	OFF	ON
HIGH	ON	OFF

CURRENT CONTROL

The voltage divider, comparators, monostable, and two-bit D/A provide a means to sense winding peak current, select winding peak current, and disable the winding sink transistors.

The UC3717A switched driver accomplishes current control using an algorithm referred to as "fixed off-time." When a voltage is applied across the motor winding, the current through the winding increases exponentially. The current can be sensed across an external resistor as an analog voltage proportional to instantaneous current. This voltage is normally filtered with a simple RC low-pass network to remove high-frequency transients, and then compared to one of the three selectable thresholds. The two-bit D/A input signal determines which one of the three thresholds is selected, corresponding to a desired winding peak current level. At the moment the sense voltage rises above the selected threshold, the UC3717A's monostable is triggered and disables both output sink drivers for a fixed off-time. The winding current then circulates through the source transistor and appropriate diode. The reference terminal of the UC3717A provides a means of continuously adjusting the current threshold to allow microstepping. Table 1 presents the relationship between the two-bit D/A input signal and selectable current level.

TABLE 1

I_0	I_1	CURRENT LEVEL
0	0	100%
1	0	60%
0	1	19%
1	1	CURRENT INHIBIT

OVERLOAD PROTECTION

The UC3717A is equipped with a new, more reliable thermal shutdown circuit which limits the junction temperature to a maximum of 180°C by reducing the winding current.

PERFORMANCE CONSIDERATIONS

In order to achieve optimum performance from the UC3717A careful attention should be given to the following items.

External Components

The UC3717A requires a minimal number of external components to form a complete control and switch drive unit. However, proper selection of external components is necessary for optimum performance. The timing pin, (pin 2) is normally connected to an RC network which sets the off-time for the sink power transistor during switched mode. As shown in Figure 8, prior to switched mode, the winding current increases exponentially to a peak value. Once peak current is attained the monostable is triggered which turns off the lower sink drivers for a fixed off-time. During off-time winding current decays through the appropriate diode and source transistor. The moment off-time times out, the motor current again rises exponentially producing the ripple waveform shown. The magnitude of winding ripple is a direct function of off-time. For a given off-time t_{OFF}, the values of R_T and C_T can be calculated from the expression:

$$T_{OFF} = 0.69 R_T C_T$$

with the restriction that R_T should be in the range of 10-100k. As shown in Figure 5, the switch frequency F_S is a function of T_{OFF} and T_{ON}. Since T_{ON} is a function of the reference voltage, sense resistor, motor supply, and winding electrical characteristics, it generally varies during different modes of operation. Thus, F_S may be approximated nominally as:

$$F_S = 1 / 1.5 (T_{OFF})$$

Normally, switch frequency is selected greater than 20kHz to prevent audible noise, and lower than 100kHz to limit power consumed during the switching cycle.

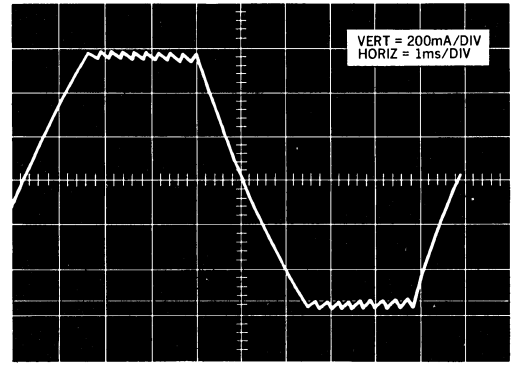

Figure 8. A typical winding current waveform. Winding current rises exponentially to a selected peak value. The peak value is limited by switched mode operation producing a ripple in winding current. A phase polarity reversal command is given and winding current decays to zero, then increases exponentially in the reverse direction.

Low-pass filter components R_C C_C should be selected so that all switching transients from the power transistors and commutating diodes are well smoothed, but the primary signal, which can be in the range of $1/T_{OFF}$ or higher must be passed. Figure 5a shows the waveform which must be smoothed, Figure 5b presents the desired waveform that just smooths out overshoot without radical distortion.

The sense resistor should be chosen as small as practical to allow as much of the winding supply voltage to be used as overdrive to the motor winding. V_{RS}, the voltage across the sense resistor, should not exceed 1.5V.

Voltage Overdrive

In many applications, maximum speed or step rate is a desirable performance characteristic. Maximium step rate is a direct function of the time necessary to reverse winding current with each step. In response to a constant motor supply voltage, the winding current changes exponentially with time, whose shape is determined by the winding time constant and expressed as:

$$I_m = V_m/R\ [1\text{-}EXP(-RT/L)]$$

as presented in Figure 9. With rated voltage applied, the time required to reach rated current is excessive when compared with the time required with over-voltage applied, even though the time constant L/R remains constant. With over-voltage however, the final value of current is excessive and must be prevented. This is accomplished with switch drive by repetitively switching the sink drivers on and off, so as to maintain an average value of current equal to the rated value. This results in a small amount of ripple in the controlled current, but the increase in step rate and performance may be considerable.

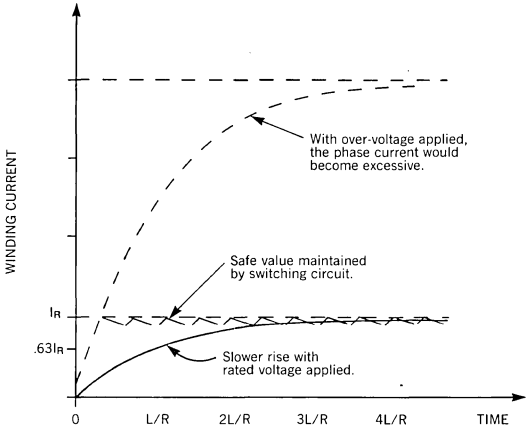

Figure 9. With rated voltage applied, winding current does not exceed rated value, but takes L/R seconds to reach 63% of its final value—probably too long. Increased performance requires an increase in applied voltage, or overdrive, and therefore a means to limit current. The UC3717A motor driver performs this task efficiently.

Interference

Electrical noise generated by the chopping action can cause interference problems, particularly in the vicinity of magnetic storage media. With this in mind, printed circuit layouts, wire runs and decoupling must be considered. 0.01 to 0.1μF ceramic capacitors for high frequency bypass located near the drive package across V+ and ground might be very helpful. The connection and ground leads of the current sensing components should be kept as short as possible.

Half-Stepping

In half step sequence the power input to the motor alternates between one or two phases being energized. In a two phase motor the electrical phase shift between the windings is 90°. The torque developed is the vector sum of the two windings energized. Therefore when only one winding is energized the torque of the motor is reduced by approximately 30%. This causes a torque ripple and if it is necessary to compensate for this, the V_R input can be used to boost the current of the single energized winding.

MOUNTING INSTRUCTIONS

The $R_{thj\text{-}amb}$ of the UC3717A can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heat sink.

The diagram of Figure 11 shows the maximum package power P_{tot} and the θ_{ja} as a function of the side " ℓ " of two equal square copper areas having a thickness of 35μ (see Figure 10).

During soldering the pins' temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The printed circuit copper area must be connected to electrical ground.

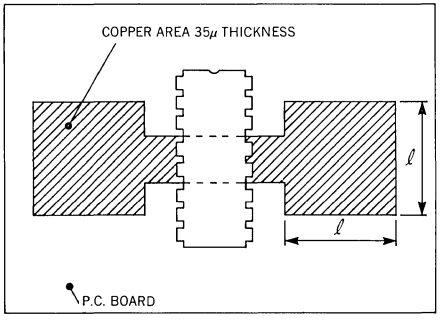

Figure 10. Example of P.C. Board Copper Area which is used as Heatsink

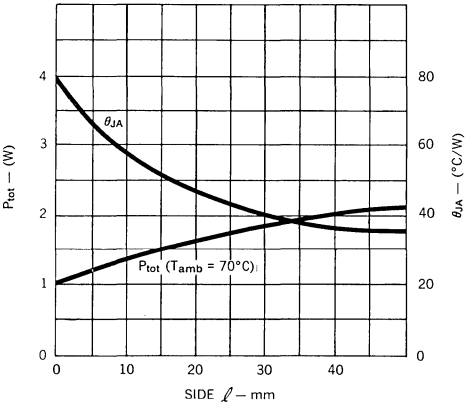

Figure 11. Maximum Package Power and Junction to Ambient Thermal Resistance vs Side " ℓ "

APPLICATIONS

A typical chopper drive for a two phase bipolar permanent magnet or hybrid stepping motor is shown in Figure 12. The input can be controlled by a microprocessor, TTL, LS, or CMOS logic.

The timing diagram in Figure 13 shows the required signal input for a two phase, full step stepping sequence. Figure 14 shows the requred input signal for a one phase-two phase stepping sequence called half-stepping.

The circuit of Figure 15 provides the signal shown in Figure 13, and in conjunction with the circuit shown in Figure 12 will implement a pulse-to-step two phase, full step, bidirectional motor drive.

The schematic of Figure 16 shows a pulse to half step circuit generating the signal shown in Figure 14. Care has been taken to change the phase signal the same time the current inhibit is applied. This will allow the current to decay faster and therefore enhance the motor performance at high step rates.

Ordering Information

UNITRODE TYPE NUMBER

UC3717ANE — 16 Pin Dual-in-line (DIL) "Bat Wing" Package

UC3717AJ — 16 Pin Dual-in-line Ceramic Package

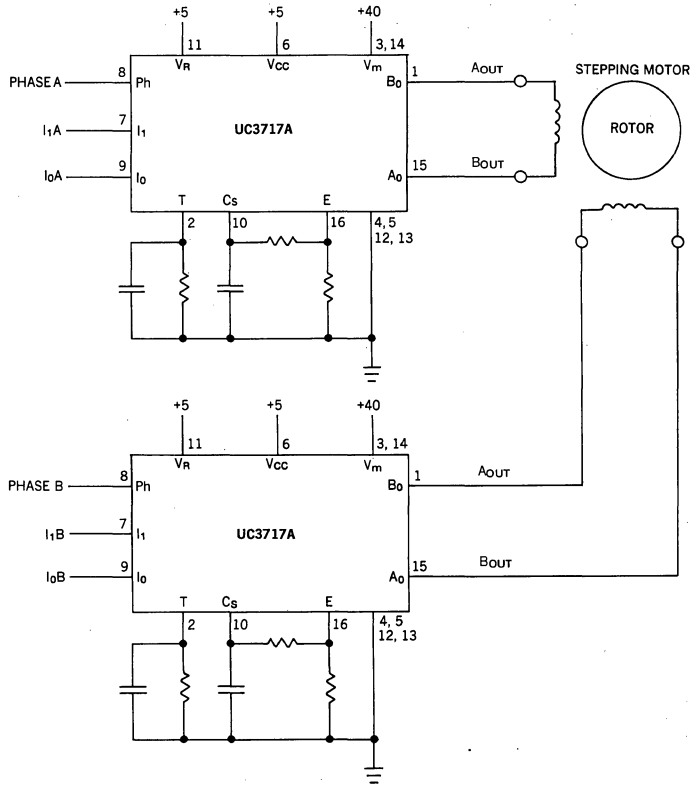

Figure 12. Typical Chopper Drive for a Two Phase Permanent Magnet Motor

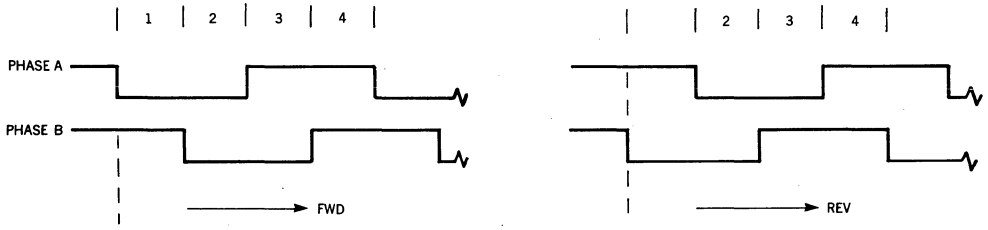

Figure 13. Phase Input Signal for Two Phase Full Step Drive (4 Step Sequence)

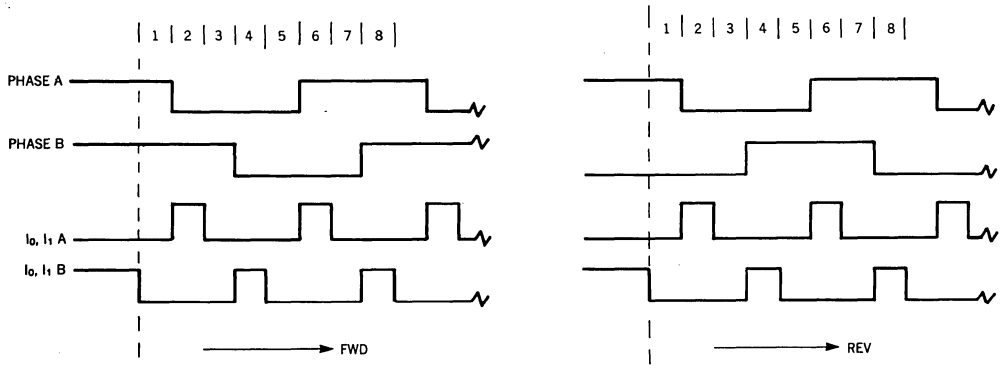

Figure 14. Phase and Current-Inhibit Signal for Half-Stepping (8 Step Sequence)

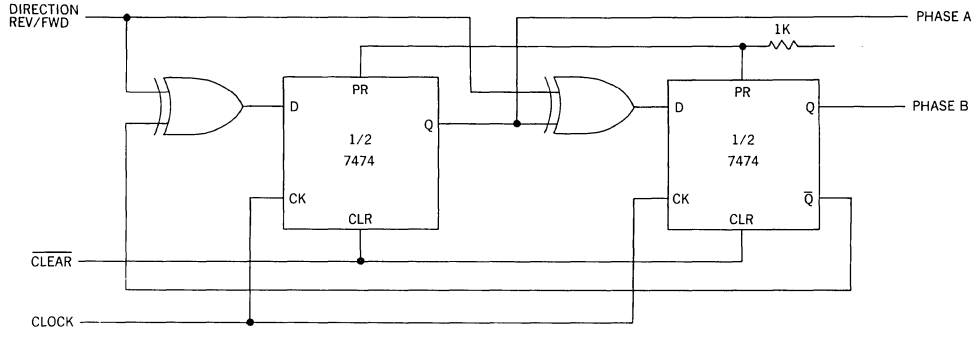

Figure 15. Full Step, Bidirectional Two Phase Drive Logic

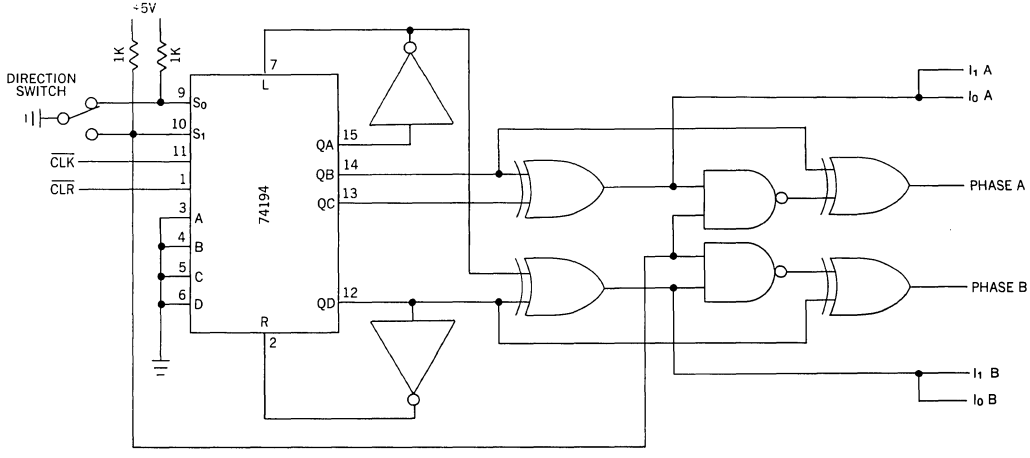

Figure 16. Half Step, Bidirectional Drive Logic

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POWER DRIVER & INTERFACE CIRCUITS 5

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POWER DRIVER & INTERFACE CIRCUITS

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
L295	Dual Solenoid Driver with Current Control	• High Current Capability (Up to 2.5A per channel) • High Voltage Operation (Up to 46V for Power Stage) • High Efficiency Switchmode Operation • Regulated Output Current (Adjustable) • Few External Components • Separate Logic Supply • Thermal Protection	15 Pin Power Tab
UC195/295/395	Smart Power Switch	The UC195/395 family of devices are ultra reliable, fast, monolithic power transistors with complete overload protection. These devices act as high gain power transistors and have on-chip, current limiting, power limiting, and thermal overload protection, making them virtually impossible to destroy. The UC195/395 offers a significant increase in reliability and simplifies power circuitry designs. • Greater than 1.0A Output • 3.0μA Typical Base Current • 500ns Switching Time • 2.0V Saturation Voltage • Directly Interfaces with CMOS or TTL • Internal Thermal Limiting	TO-5 TO-220
UC1704/3704	Bridge Transducer Switch	• Dual Matched Current Sources • High-Gain Differential Sensing Circuit • Wide Common-Mode Input Capability • Complimentary Digital Open-Collector Outputs • Externally Programmable Time Delay • Optional Output Latch with Reset • Built-In Diagnostic Activation • Wide Supply Voltage Range • High Current Heater Power Source Driver	16 Pin DIL
UC1705/3705	High Speed Power Driver (Single ended)	• 1.5A Totem Pole Output • High Speed MOSFET Compatible • Low Quiescent Current • Low Cost Package	8 Pin DIL 5 Pin TO-220
UC1706/3706 UC1707/3707	Dual High Current MOSFET Compatible Output Driver Dual Uncommitted High Current MOSFET Compatible Output Driver	• Dual, 1.5A, Totem Pole Outputs • Parallel or Push-Pull Operations • Single-Ended to Push-Pull Conversion (1706 Series) • Internal Overlap Protection • Analog, Latched Shutdown • High-Speed, Power MOSFET Compatible • Thermal Shutdown Protection • 5 to 40V Operation • Low Quiescent Current	16 Pin DIL "Batwing"
UC1728/3728	PWM Dual Driver	Load Control and Status monitoring for two inductive loads) up to 1 amp each. • PWM Current Control • Dual, Floating Switches • Supply Voltage up to 60V • Tri-State Status Outputs • 60V Operation	28 Pin DIL 28 PLCC
UC2950	Half-Bridge Bipolar Switch	• Source or Sink 4.0A • Supply Voltage to 35V • High-Current Output Diodes • Tri-State Operation • TTL and CMOS Input Compatibility • Thermal Shutdown Protection • 300kHz Operation	5 Pin TO-220

5

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POWER DRIVER & INTERFACE CIRCUITS (cont.)

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC3657	Triple Half Bridge Power Driver	See Motor Control Section	15 Pin Power Tab
UC3720	Smart Switch	Independent high and low side switching, up to 2.5A capability. • Full Protection • Over- and Under-Current Fault Indication • 50V Operation	15 Pin Power Tab
UC3722	Five Channel Programmable Current Switch	• Five Current-Sinking Switches • Programmable Currents from .5 to 2.5A • Internal Current Sensing • 40V Operation • Protection Features	15 Pin Power Tab
UC5170	Octal Single Ended Line Driver	Suited for data transmission systems. • Eight Driver in One Package • Meets EIA Standards • Single External Resistor Controls Slew Rate • Tri-State Outputs • Low Power Consumption • TTL Compatible	28 Pin DIL 28 PLCC
UC5180/5181	Octal Line Receiver	Suited for digital communication requirements. • Eight Receivers in One Package • Meets EIA Standards • Single 5V Supply • Differential Inputs Withstand ±25V • Low Noise Filter (5180 Only)	28 Pin DIL 28 PLCC

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LINEAR INTEGRATED CIRCUITS

Dual Switchmode Solenoid Driver

FEATURES

- High current capability (up to 2.5A per channel)
- High voltage operation (up to 46V for power stage)
- High efficiency switchmode operation
- Regulated output current (adjustable)
- Few external components
- Separate logic supply
- Thermal protection

DESCRIPTION

The L295 is a monolithic integrated circuit in a 15 lead MULTIWATT® package; it incorporates all the functions for direct interfacing between digital circuitry and inductive loads. The L295 is designed to accept standard microprocessor logic levels and drive 2 independent solenoids. The output current is completely controlled by means of a switching technique allowing very efficient operation. Furthermore, it includes an enable input and separate power supply inputs for bilevel operation such as interfacing with peripherals running at higher voltage levels.

The L295 is particularly suitable for applications such as hammer driving in matrix printers, step motor driving and electromagnet controllers.

ABSOLUTE MAXIMUM RATINGS

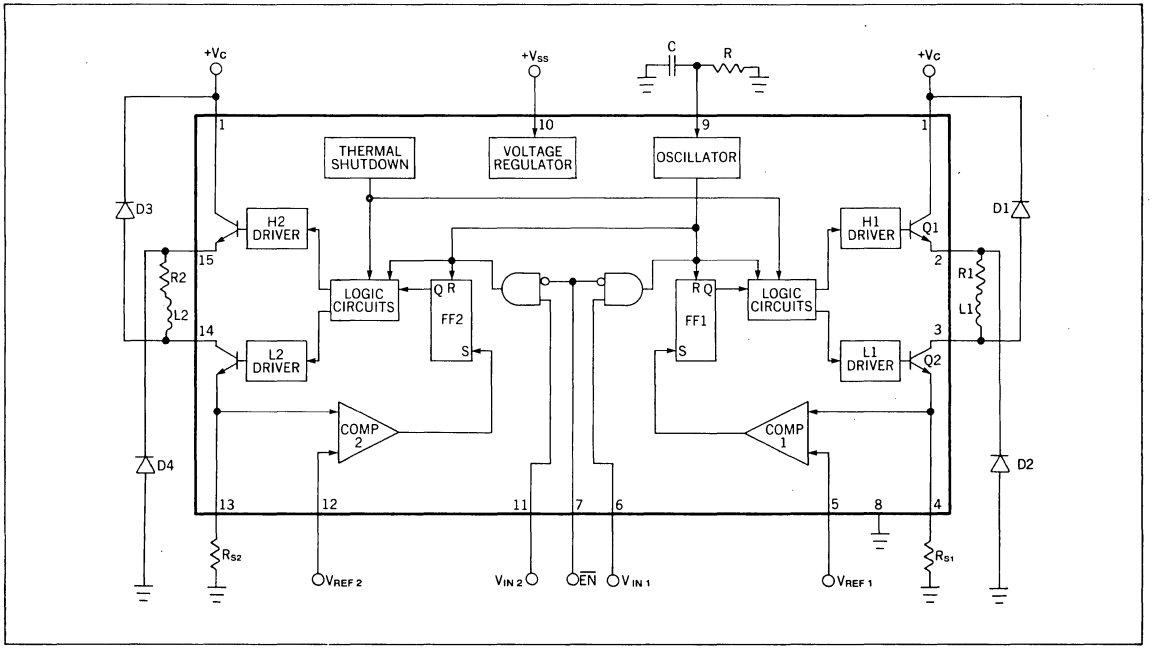
Collector Supply Voltage, V_C 50V
Logic Supply Voltage, V_{SS} 12V
Enable and Input Voltage, V_{EN}, V_i 7V
Reference Voltage, V_{REF} 7V
Peak Output Current (each channel)
Non-Repetitive, (t = 100μsec), I_o 3A
Repetitive (80% on −20% off; t_{ON} = 10ms) 2.5A
DC Operation 2A
Total Power Dissipation (at T_{case} = 75°C) 25W
Storage and Junction Temperature ..... −40 to +150°C

THERMAL DATA

Thermal Resistance Junction-Case, θ_{JC} ..... 3°C/W max
Thermal Resistance Junction-Ambient, θ_{JA} ..... 35°C/W max

5

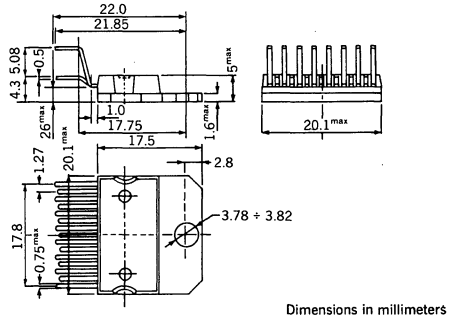
BLOCK DIAGRAM



UNITRODE

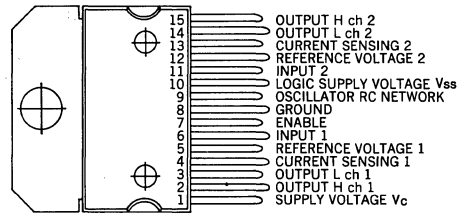
MECHANICAL DATA

V Package



Dimensions in millimeters

CONNECTION DIAGRAM (TOP VIEW)



ELECTRICAL CHARACTERISTICS (Refer to the application circuit, V_{SS} = 5V, V_C = 36V, T_j = 25°C; unless otherwise specified, L = Low; H = High)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_C		12		46	V
Logic Supply Voltage	V_{SS}		4.75		10	V
Quiescent Drain Current (from V_C)	I_C	V_C = 46V; V_{i1} = V_{i2} = V_{EN} = L			4	mA
Quiescent Drain Current (from V_{SS})	I_{SS}	V_{SS} = 10V			46	mA
Low Input Voltage	V_{i1}L, V_{i2}L		-0.3		0.8	V
High Input Voltage	V_{i1}H, V_{i2}H		2.2		7	V
Low Enable Input Voltage	V_{EN}L		-0.3		0.8	V
High Enable Input Voltage	V_{EN}H		2.2		7	V
Input Current	I_{i1}, I_{i2}	V_{i1} = V_{i2} = L			-100	μA
		V_{i1} = V_{i2} = H			10	
Enable Input Current	I_{EN}	V_{EN} = L			-100	μA
		V_{EN} = H			10	
Input Reference Voltage	V_{REF1}, V_{REF2}		0.2		2	V
Input Reference Current	I_{REF1}, I_{REF2}				-5	μA
Oscillation Frequency	f_{osc}	C = 3.9nF, R = 9.1KΩ		25		KHz
Transconductance (each channel)	$\frac{I_p}{V_{REF}}$	V_{REF} = 1V, R_s = 0.5Ω	1.9	2	2.1	A/V
Total Output Voltage Saturation (each channel)*	V_{sat}	I_o = 2A		2.8	3.6	V
External Sensing Resistors Voltage Drop	$V_{sens\ 1}$, $V_{sens\ 2}$				2	V

*V_{sat} = $V_{CEsatQ1}$ + $V_{CEsatQ2}$.

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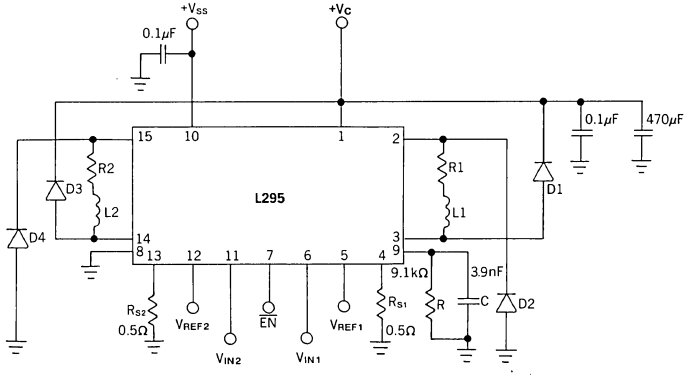
APPLICATION CIRCUIT



D1, D4 = 2A HIGH SPEED DIODES (SES5001, or equivalent)

FUNCTIONAL DESCRIPTION

The L295 incorporates two independent driver channels with separate inputs and outputs, each capable of driving an inductive load (see block diagram).

The device is controlled by three microprocessor compatible digital inputs and two analog inputs. These inputs are;

$\overline{EN}$ chip enable (digital input, active low), enables both channels when in the low state.

V_{IN1},
V_{IN2} channel inputs (digital inputs, active high), enable each channel independently. A channel is activated when both $\overline{EN}$ and the appropriate channel input are active.

V_{REF1},
V_{REF2} reference voltages (analog inputs), used to program the peak load currents. Peak load current is proportional to V_{REF}.

Since the two channels are identical, only channel one will be described. The following description applies equally to channel two, replacing FF2 for FF1, V_{REF2} for V_{REF1} etc. When the channel is activated by a low level on the $\overline{EN}$ input and a high level on the channel input V_{IN1}, the output transistors Q1 and Q2 switch on and current flows in the load according to the exponential law:

$$I = \frac{V}{R1}\left(1 - e^{\frac{-R1t}{L1}}\right)$$

where: R1 and L1 are the resistance and inductance of the load and V is the voltage available on the load

The current increases until the voltage on the external sensing resistor, R_{S1}, reaches the reference voltage, V_{REF1}. This peak current, I_{p1}, is given by:

$$I_{p1} = \frac{V_{REF1}}{R_{S1}}$$

At this point the comparator output, Comp 1, sets the RS flip-flop, FF1, that turns off the output transistor, Q1. The load current flowing through D2, Q2, R_{S1}, decreases according to the law:

$$I = \left(\frac{V_A}{R1} + I_{P1}\right) e^{\frac{-R1\,t}{L1}} - \frac{V_A}{R1}$$

where: $V_A = V_{CEsat\ Q2} + V_{sense\ 1} + V_{D2}$

If the oscillator pin (9) is connected to ground the load current falls to zero as shown in Figure 1.

At time t_2, channel 1 is disabled by taking the inputs V_{IN1} low and/or $\overline{EN}$ high, and the output transistor Q2 is turned off. The load current flows through D2 and D1 according to the law:

$$I = \left(\frac{V_B}{R1} + I_{T2}\right) e^{\frac{-R1t}{L1}} - \frac{V_B}{R1}$$

where: $V_B = V_C + V_{D1} + V_{D2}$
I_{T2} = current value at the time t_2.

Figure 2 shows the current waveform obtained with an RC network connected between pin 9 and ground. From t_o to t_1 the current increases as in Figure 1. A difference exists at the time t_2 because the current starts to increase again. At this time a pulse is produced by the oscillator circuit that resets the flip flop, FF1, and switches on the output transistor, Q1. The current increases until the drop on the sensing resistor R_{s1} is equal to V_{REF1} (t_3) and the cycle repeats.

The switching frequency depends on the values of R and C, as shown in Figure 4 and must be chosen in the range 10 to 30KHz.

It is possible with external hardware to change the reference voltage V_{REF} in order to obtain a high peak current I_p and a lower holding current I_h (see Figure 3).

The L295 is provided with a thermal protection that switches off all the output transistors when the junction temperature exceeds 150°C. The presence of a hysteresis circuit makes the IC work again after a fall of the junction temperature of about 20°C.

The analog input pins (V_{REF1}, V_{REF2}) can be left open or connected to V_{ss}; in this case the circuit works with an internal reference voltage of about 2.5V and the peak current in the load is fixed only by the value of R_s:

$$I_p = \frac{2.5}{R_s}$$

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SIGNAL WAVEFORMS

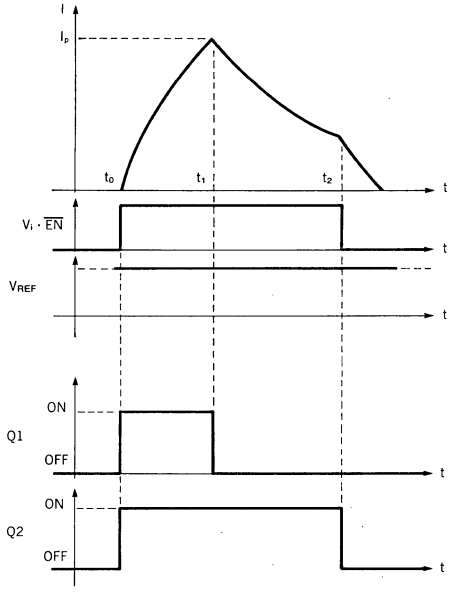


Figure 1. Load current waveform with pin 9 connected to GND

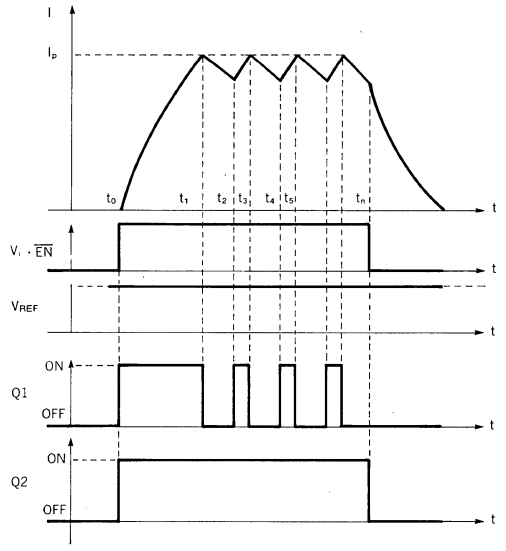


Figure 2. Load current waveform with external R-C network connected between pin 9 and ground

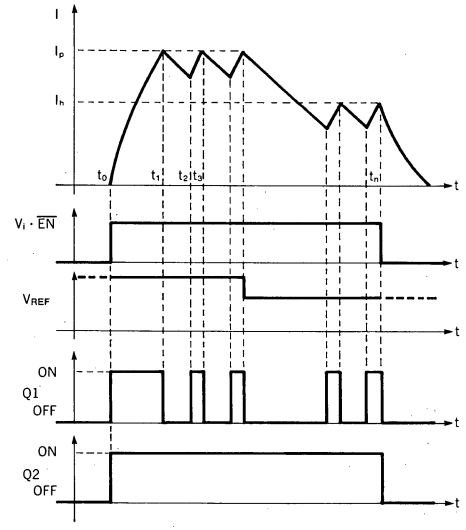


Figure 3. With V_{REF} changed by hardware

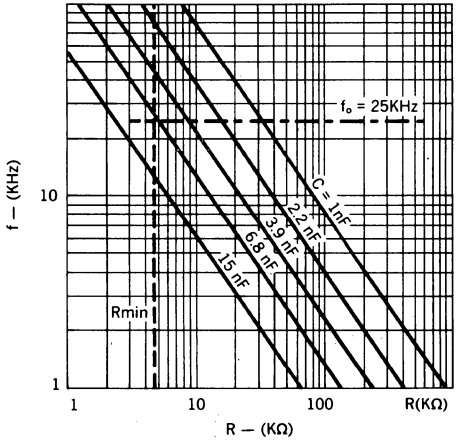


Figure 4. Switching frequency vs values of R and C

Smart Power Transistor

FEATURES

- Greater Than 1.0A Output
- 3.0μA Typical Base Current
- 500ns Switching Time
- 2.0V Saturation
- Directly Interfaces with CMOS or TTL
- Internal Thermal Limiting

DESCRIPTION

The UC195/UC395 family of devices are ultra reliable, fast, monolithic power transistors with complete overload protection. These devices act as high gain power transistors and have on chip, current limiting, power limiting, and thermal overload protection, making them virtually impossible to destroy. The UC195/UC395 offers a significant increase in reliability and simplifies power circuitry designs.

The UC195/UC395 are available in standard TO-3 power packages and solid Kovar TO-5. The UC195 is rated for operation from −55°C to +150°C, the UC295 is rated from −25°C to +125°C, and the UC395 is rated from 0°C to +125°C.

ABSOLUTE MAXIMUM RATINGS

Collector to Emitter Voltage
- UC195, UC295 ..... 42V
- UC395 ..... 36V

Collector to Base Voltage
- UC195, UC295 ..... 42V
- UC395 ..... 36V

Base to Emitter Voltage (Forward)
- UC195, UC295 ..... 42V
- UC395 ..... 36V

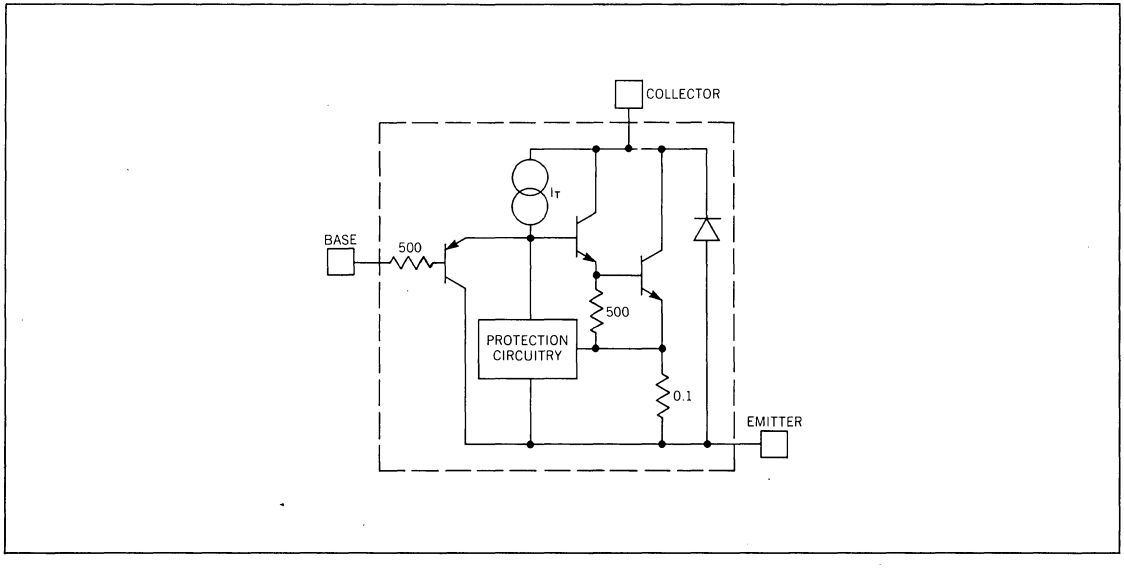
Base to Emitter Voltage (Reverse) 20V
Collector Current ..... Internally Limited
Power Dissipation ..... Internally Limited
Operation Temperature Range
- UC195 ..... −55°C to +150°C
- UC295 ..... −25°C to +125°C
- UC395 ..... 0°C to +125°C

Storage Temperature Range ..... −65°C to +150°C
Lead Soldering Temperature (10 seconds) ..... 300°C

THERMAL DATA

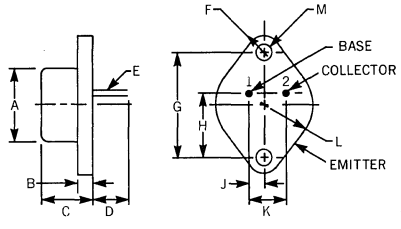
TO-3 ..... θ_{ja} = 35°C/W
TO-5 ..... θ_{ja} = 150°C/W

BLOCK DIAGRAM



UNITRODE

MECHANICAL SPECIFICATIONS



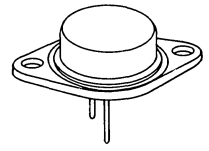
BOTTOM VIEW

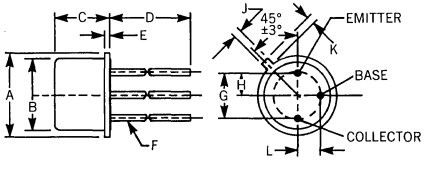
CASE: EMITTER

	INCHES	MILLIMETERS
A	.875 MAX.	22.23 MAX.
B	.135 MAX.	3.43 MAX.
C	.250-.450	6.35-11.43
D	.312 MIN.	7.92 MIN.
E	.038-.043 DIA.	0.97-1.09 DIA.
F	.188 MAX. RAD.	4.78 MAX. RAD.
G	1.177-1.197	29.90-30.40
H	.655-.675	16.64-17.15
J	.205-.225	5.21-5.72
K	.420-.440	10.67-11.18
L	.525 MAX. RAD.	13.34 MAX. RAD.
M	.151-.161 DIA.	3.84-4.09 DIA.

CONNECTION DIAGRAMS

TO-3

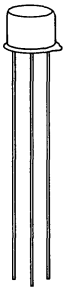




CASE: EMITTER

	INCHES	MILLIMETERS
A	.335-.370	8.51-9.40
B	.305-.335	7.75-8.51
C	.240-.260	6.09-6.60
D	1.5 MIN.	38.10 MIN.
E	.010-.030	.254-.762
F	.017 ± .002 .001	.432 ± .051 .025
G	.200	5.08
H	.100	2.54
J	.028-.034	.711-.864
K	.029-.045	.736-1.14
L	.100	2.54

TO-5



ELECTRICAL CHARACTERISTICS (Unless otherwise specified these specifications apply for $-55°C \leq T_j \leq +150°C$ for the UC195, $-25°C \leq T_j \leq +125°C$ for the UC295, and $0°C \leq T_j \leq +125°C$ for the UC395.)

PARAMETERS	SYMBOL	CONDITIONS	UC195, UC295			UNITS
			MIN.	TYP.	MAX.	
Collector-Emitter Operating Voltage	V_{ce}	$I_q \leq I_c \leq I_{c\,max}$			42	V
Base to Emitter Breakdown Voltage	BV_{be}	$0 \leq V_{ce} \leq V_{ce\,max}$	42			V
Collector Current	I_c					
TO-3		$V_{ce} \leq 15V$	1.2	2.2		A
TO-5		$V_{ce} \leq 7.0V$	1.2	1.8		A
Saturation Voltage	V_{sat}	$I_c \leq 1.0A$, $T_A = 25°C$		1.8	2.0	V
Base Current	I_b	$0 \leq I_c \leq I_{max}$ $0 \leq V_{ce} \leq V_{ce\,max}$		3.0	5.0	μA
Quiescent Current	I_q	$V_{be} = 0V$ $0 \leq V_{ce} \leq V_{ce\,max}$		2.0	5.0	mA
Base-Emitter Voltage	V_{be}	$I_c = 1.0A$, $T_A = 25°C$		0.9		V
Switching Time	t_s	$V_{ce} = 36V$, $R_L = 36\Omega$ $T_A = 25°C$		500		ns
Thermal Resistance Junction to Case	θ_{jc}	TO-3 Package		2.3	3.0	°C/W
		TO-5 Package		12	15	°C/W

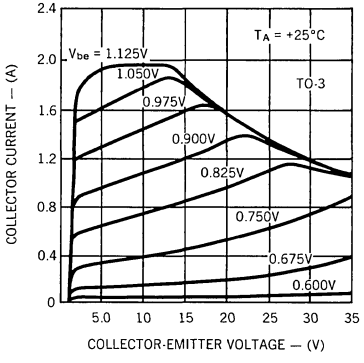
ELECTRICAL CHARACTERISTICS (Unless otherwise specified these specifications apply for $-55°C \leq T_j \leq +150°C$ for the UC195, $-25°C \leq T_j \leq +125°C$ for the UC295, and $0°C \leq T_j \leq +125°C$ for the UC395.)

PARAMETERS	SYMBOL	CONDITIONS	UC395			UNITS
			MIN.	TYP.	MAX.	
Collector-Emitter Operating Voltage	V_{ce}	$I_q \leq I_c \leq I_{c\,max}$			36	V
Base to Emitter Breakdown Voltage	BV_{be}	$0 \leq V_{ce} \leq V_{ce\,max}$	36	60		V
Collector Current TO-3 TO-5	I_c	 $V_{ce} \leq 15V$ $V_{ce} \leq 7.0V$	 1.0 1.0	 2.2 1.8		 A A
Saturation Voltage	V_{sat}	$I_c \leq 1.0A$, $T_A = 25°C$		1.8	2.2	V
Base Current	I_b	$0 \leq I_c \leq I_{max}$ $0 \leq V_{ce} \leq V_{ce\,max}$		3.0	10.0	μA
Quiescent Current	I_q	$V_{be} = 0V$ $0 \leq V_{ce} \leq V_{ce\,max}$		2.0	10.0	mA
Base-Emitter Voltage	V_{be}	$I_c = 1.0A$, $T_A = 25°C$		0.9		V
Switching Time	t_s	$V_{ce} = 36V$, $R_L = 36\Omega$ $T_A = 25°C$		500		ns
Thermal Resistance Junction to Case	θ_{jc}	TO-3 Package TO-5 Package		2.3 12	3.0 15	°C/W °C/W

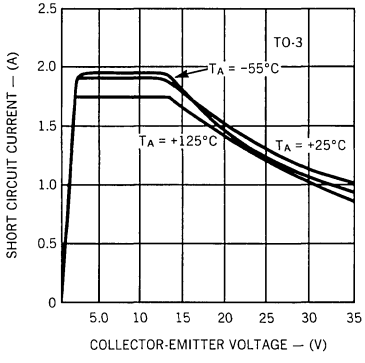
5

TYPICAL PERFORMANCE CHARACTERISTICS

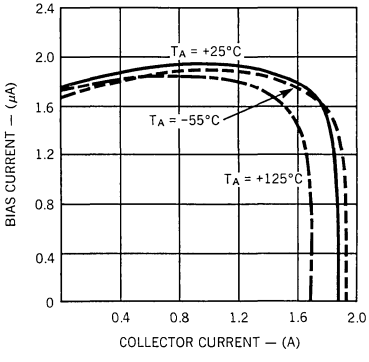
Collector Characteristics



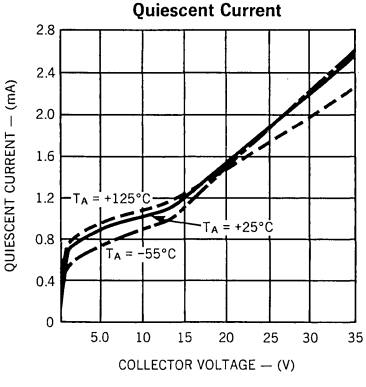
Short Circuit Current



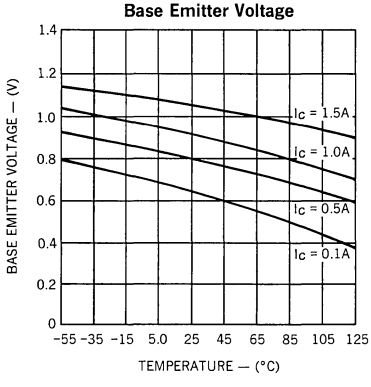
Bias Current



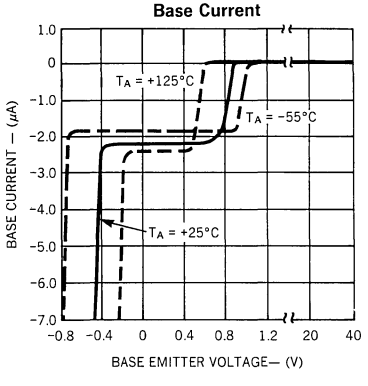
Quiescent Current



Base Emitter Voltage



Base Current



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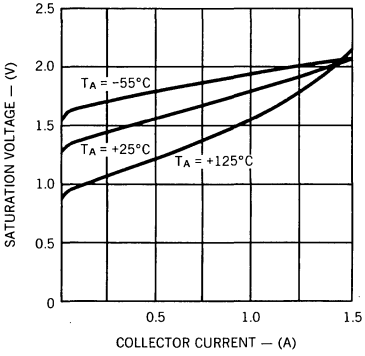
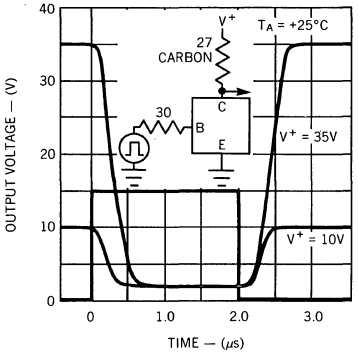
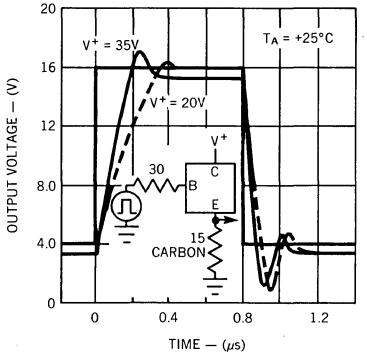
Saturation Voltage



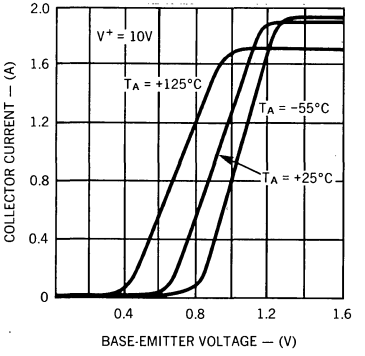
Response Time



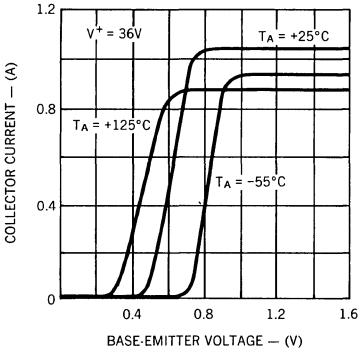
Response Time



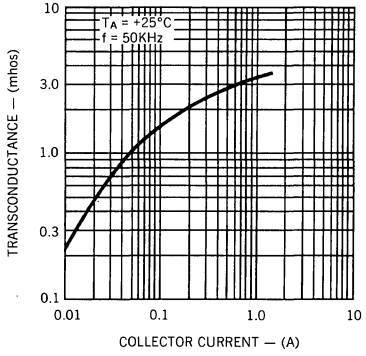
10V Transfer Function



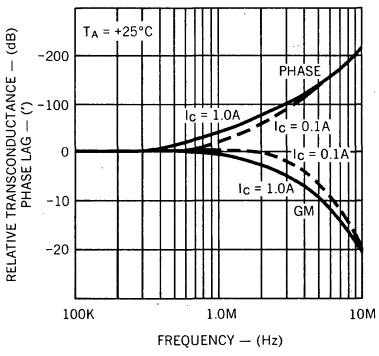
36V Transfer Function



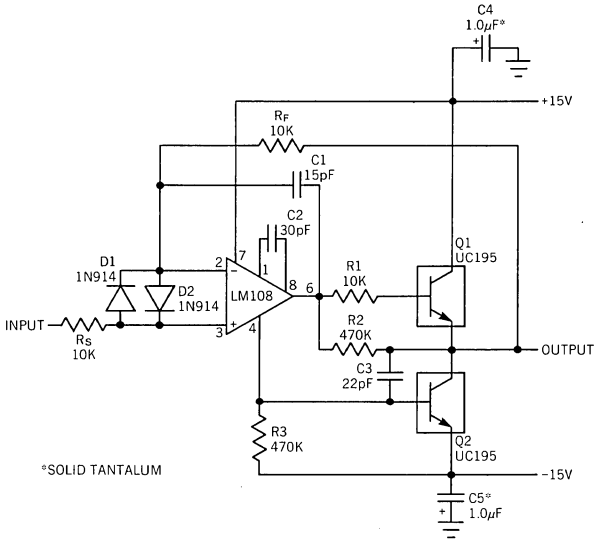
Transconductance



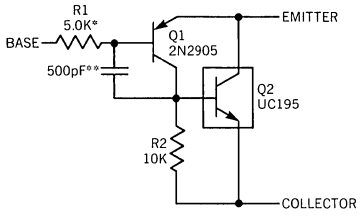
Small Signal Frequency Response



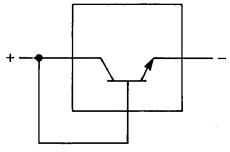
TYPICAL APPLICATIONS



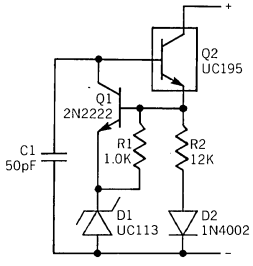
1.0A Voltage Follower



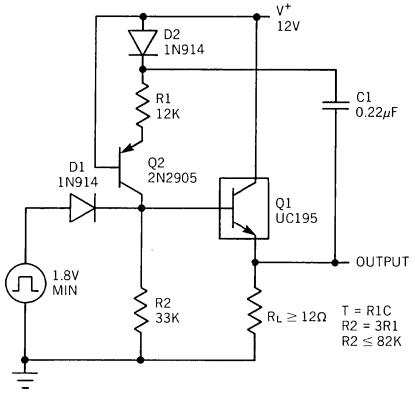
Power PNP



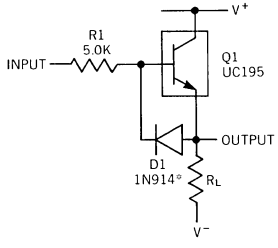
Two Terminal Current Limiter



Two Terminal 100mA Current Regulator



Power One-Shot



Fast Follower

LINEAR INTEGRATED CIRCUITS
Bridge Transducer Switch

UC1704
UC3704

UC1704 COMPATIBLE SENSORS

SENSOR TYPE	ACTIVATION SOURCE						
	Temperature	Pressure	Force	Position	Displacement	Velocity	Shock
Thermistor	X					X	
Sensistor	X					X	
Thermocouple	X						
Semiconductor	X	X	X				
Photo Voltaic				X	X	X	
Photo Resistive				X	X	X	
Strain Gage		X	X	X	X	X	X
Piezoelectric		X	X		X	X	X
Magneto Resistive				X	X		
Inductive				X	X	X	X
Hall Effect				X	X		
Capacitive							X

FEATURES

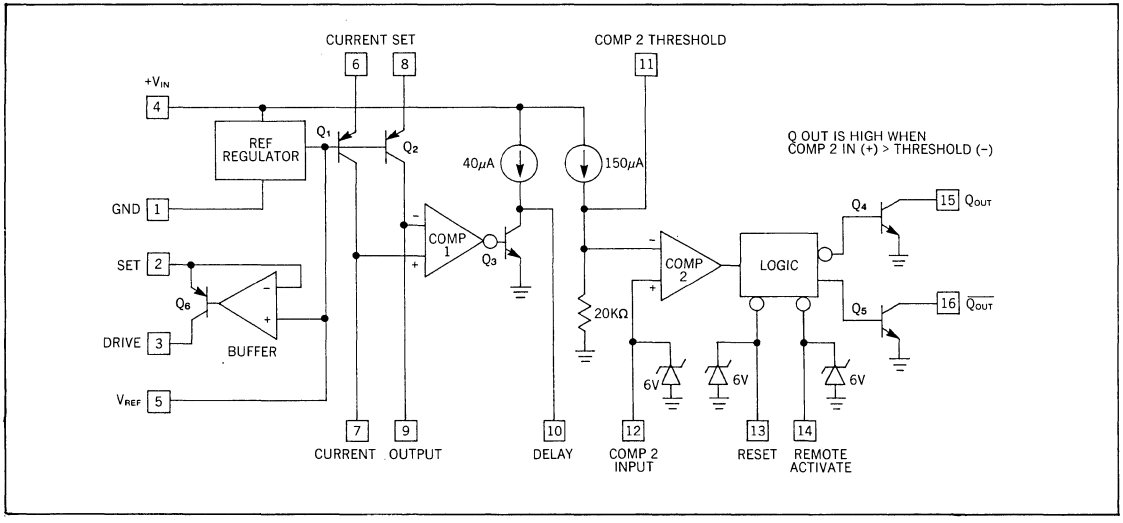
- Dual matched current sources
- High-gain differential sensing circuit
- Wide common-mode input capability
- Complimentary digital open-collector outputs
- Externally programmable time delay
- Optional output latch with reset
- Built-in diagnostic activation
- Wide supply voltage range
- High current heater power source driver

DESCRIPTION

This integrated circuit contains a complete signal conditioning system to interface low-level variable impedance transducers to a digital system. A pair of matched, temperature-compensated current sources are provided for balanced transducer excitation followed by a precision, high-gain comparator. The output of this comparator can be delayed by a user-selectable duration, after which a second comparator will switch complimentary outputs compatible with all forms of logic. This output section can be separately activated for diagnostic operation and has an optional latch with external reset capability. An added feature is a high current power source useful as a heater driver in differential temperature sensing applications.

The UC1704 is characterized for operation over the full military temperature range of −55°C to +125°C while the UC3704 is designed for 0°C to +70°C environments.

BLOCK DIAGRAM



UNITRODE

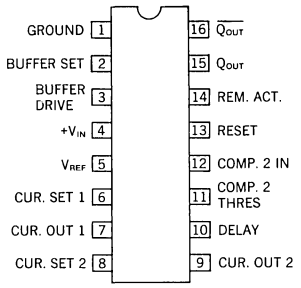
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($+V_{IN}$) 40V
Output Current (each output) 50mA
Buffer Power Source Current 200mA
Comparator 1 Inputs ..... -0.5V to V_{REF}
Comparator 2 Inputs ..... 0 to 5.5V
Remote Activation and Reset Inputs ..... 0 to 5.5V
Power Dissipation at T_A = 25°C 1000mW
Derate at 10mW/°C for T_A > 50°C
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

NOTE: Unless otherwise specified, all voltages are with respect to ground (Pin 1). Currents are positive into, negative out of the specified terminal.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



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ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1704 and 0°C to +70°C for the UC3704; V_{IN} = 15V)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Power Inputs					
Supply Voltage Range	T_A > 0°C	4.2		36	V
Supply Current	V_{IN} = 36V		5	10	mA
Reference Section (with respect to V_{IN})					
V_{REF} Value $\lvert V_{IN} - V_{REF} \rvert$	T_J = 25°C	2.1	2.2	2.3	V
V_{REF} Temperature Coefficient	Note 1	-1	-2	-3	mV/°C
Line Regulation	ΔV_{IN} = 4.2 to 25V		2	10	mV
Load Regulation	ΔI_O = 0 to 4mA		2	10	mV
Short Circuit Current	V_{IN} = 36V V_{REF} = V_{IN} or Ground			±25	mA
Current Sources (Q_1 and Q_2)					
Output Current (Note 2)	Current Set = 10μA	-9	-9.5	-10	μA
	Current Set = 200μA	-180	-195	-200	μA
Output Offset Current	R_{E6} = R_{E8} = 20KΩ		0	±1	μA
Comparator One					
Input Offset Voltage			±1	±4	mV
Input Bias Current			-100	-300	nA
Input Offset Current				±60	nA
CMRR	V_{CM} = 0 to 12V	60	70		dB
Voltage Gain	R_L > 150KΩ	70	85		dB
Delay Current Source		34	40	52	μA
Output Rise Time	Overdrive = 10mV, C_D = 15pF, T_J = 25°C		2		V/μs

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1704 and 0°C to +70°C for the UC3704; V_{IN} = 15V)

PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
Comparator Two (Q_{OUT} and $\overline{Q_{OUT}}$)						
Threshold Voltage			2.2	3.0	3.8	V
Threshold Resistance	To Ground		14	20	24	KΩ
Input Bias Current	V_{IN} (Pin 12) = 5V			1	3	μA
Remote Activate Current	Pin 14 = 0V			0.2	0.5	mA
Reset Current	Pin 13 = 0V			0.2	0.5	mA
Remote Activate Threshold	T_A = 25°C		0.8	1.2		V
Reset Threshold	T_A = 25°C		0.8	1.2		V
Output Saturation	I_{OUT} = 16mA			0.2	0.5	V
	I_{OUT} = 50mA			0.7	2.0	V
Output Leakage	V_{OUT} = 40V			0.2	10	μA
Output Response	Comp. Overdrive = 1V, R_L = 5K to V_{IN}	Turn-on		0.4		μs
		Turn-off		1.0		
Buffer						
Set Voltage (V_{IN} − V_S)	T_J = 25°C, I_S = 100mA		1.9	2.1	2.3	V
Drive Current	T_J = 25°C, R_S = 200Ω, V_D = 0V		90	100	120	mA

Note: 1. Parameter guaranteed by design, not tested in production.

2. Collector output current = $\frac{V_{IN} - V_{REF} - V_{BE}}{R_E} \approx \frac{1.5V}{R_E}$

APPLICATIONS INFORMATION

Sensor Section

The input portion of the UC1704 provides both excitation and sensing for a low-level, variable impedance transducer. This circuitry consists of a pair of highly matched PNP transistors biased for operation as constant current sources followed by a high gain precision comparator.

The reference voltage at the bases of the PNP transistors has a TC to offset the base-emitter voltage variation of these transistors resulting in a constant voltage across the external emitter resistors and correspondingly constant collector currents. With the emitter resistors external, the user has the option of tailoring the collector currents for balancing, offsetting, or to provide a unique temperature characteristic.

With the PNP transistors' optimum current ranging from 10 to 200μA, and the common-mode input voltage of the comparator usable from ground to (V_{IN} − 3V), a wide range of transducer impedance levels is possible.

The sensor comparator has a current source pull-up at the output so that an external capacitor from this point to ground can be used to provide a programmable delay before reaching the second comparator's threshold. The low-impedance on-state of Comp 1's output provides quick reset of this capacitor. This programmable delay function is useful for providing transient protection by requiring that Comp 1 remain activated for a finite period of time before Comp 2 triggers. Another application is in counting repetitive pulses where a missing pulse will allow Comp 1's output to rise to Comp 2's threshold. This time delay function is:

$$\text{Delay} = \frac{\text{Comp 2 Threshold}}{\text{Delay Current}} \times C_D \approx 175\ \text{ms}/\mu\text{F}$$

If hysteresis is desired for Comparator 1, it may be accommodated by applying positive feedback from the delay terminal to the non-inverting input on Pin 7. This will aid in providing oscillation-free transitions for very slowly changing inputs.

Output Section

The output portion of the UC1704 is basically a second comparator with complimentary, open-collector outputs. This comparator has a built-in, ground-referenced threshold implemented with a high-impedance current source and resistor so that it may be easily overridden with an external voltage source if desired. Comp 2's input transistors are NPN types which require at least 1V of common-mode voltage for accurate operation and should not see a differential input voltage greater than 6V.

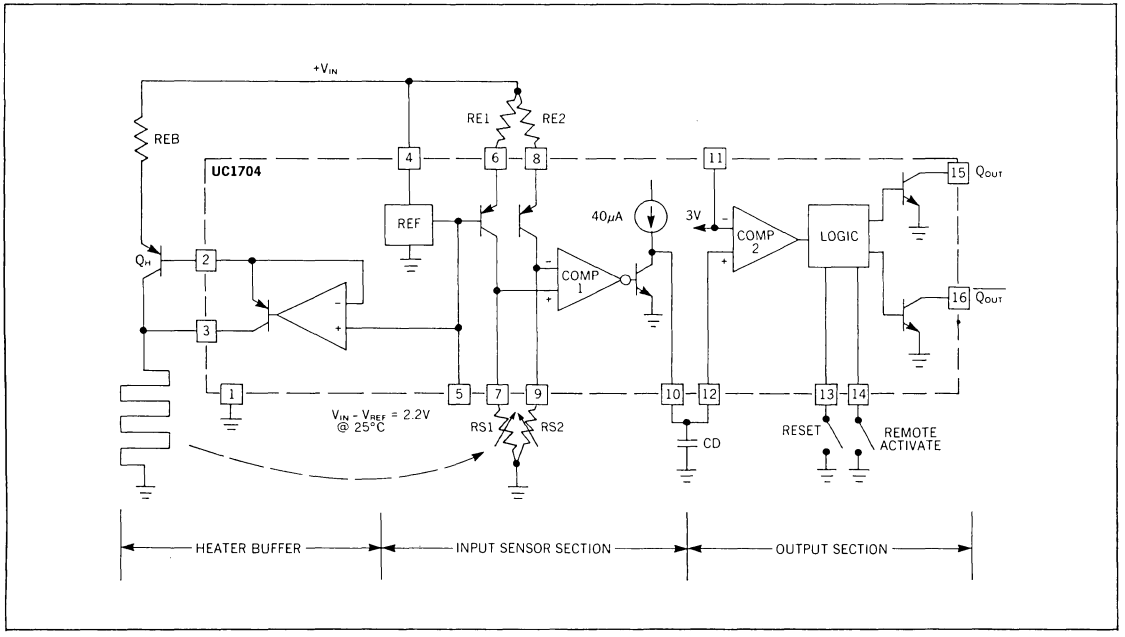
For diagnostic or latching purposes, the output logic is equipped with a Remote Activate and Reset function. These pins have internal pull-ups and are only active when pulled low below a threshold of approximately 1V. A low signal at the Remote Activate Pin causes the outputs to change state in exactly the same manner as if Comp 2's input is raised above the threshold on Pin 11. If Pin 16 is connected to Pin 14, positive feedback results and the outputs will latch once triggered by Comp 2's input. Pulling the Reset terminal low overrides the Remote Activate Pin releasing the latch.

Reference Buffer

This circuit is designed to provide up to 100mA to drive a high-current external PNP transistor useful for powering a heater for differential temperature measurements. Care must be taken that power dissipation in Q_6 does not cause excessive thermal gradients which will degrade the accuracy of the sensing circuitry.

Using a heating element attached to a temperature sensitive resistor, RS1, in one leg of the input bridge implements a flow sensor for either gasses or liquids. As long as there is flow, heat from the element is carried away and the sensor voltage remains below threshold. Using an identical sensor, RS2, without a heater to establish this threshold compensates for the ambient temperature of the flow.

Typical Application For Monitoring Liquid or Gas Flow



5

LINEAR INTEGRATED CIRCUITS
High Speed Power Driver

UC1705
UC3705

FEATURES
- 1.5A Source/Sink Drive
- 100 nsec Delay
- 40 nsec Rise and Fall into 1000pF
- Inverting and Non-Inverting Inputs
- Low Cross-Conduction Current Spike
- Low Quiescent Current
- 5V to 40V Operation
- Thermal Shutdown Protection
- MINIDIP and Power Packages

DESCRIPTION

The UC1705 family of power drivers is made with a high speed Schottky process to interface between low-level control functions and high-power switching devices — particularly power MOSFETs. These devices are also an optimum choice for capacitive line drivers where up to 1.5 amps may be switched in either direction. With both Inverting and Non-Inverting inputs available, logic signals of either polarity may be accepted, or one input can be used to gate or strobe the other.

Supply voltages for both V_S and V_C can independently range from 4.5V to 40V. In the MINIDIP package, V_S can also be used to gate the output as when V_S is less than 4V, the output is held in the high impedence state and no current is drawn from V_C.

For additional application details, see the UC1707/3707 data sheet.

The UC1705 is packaged in an 8-pin hermetically sealed CERDIP for −55°C to +125°C operation. The UC3705 is specified for a temperature range of 0°C to +70°C and is available in either a plastic minidip or a 5-pin, power TO-220 package.

TRUTH TABLE

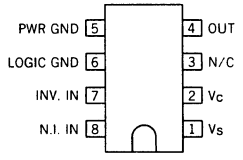
INV	N.I.	OUT
H	H	L
L	H	H
H	L	L
L	L	L

OUT = $\overline{\text{INV}}$ and N.I.

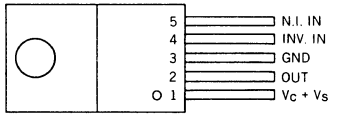
$\overline{\text{OUT}}$ = INV or $\overline{\text{N.I.}}$

CONNECTION DIAGRAMS

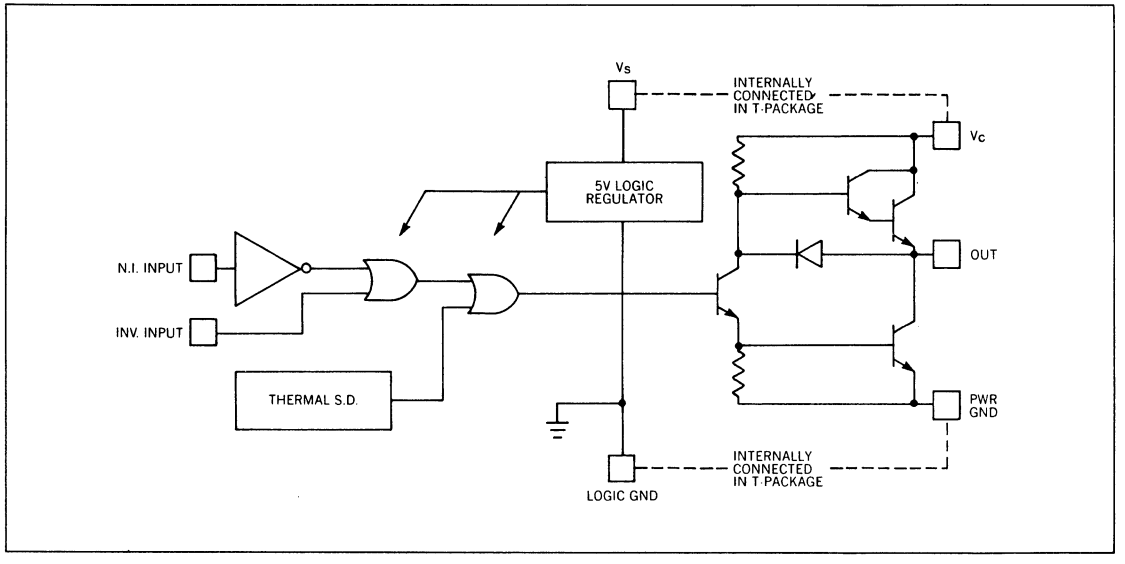
DIL-8 MINIDIP
N or J Package
Top View



5-Pin TO-220
T Package
Top View



BLOCK DIAGRAM



UNITRODE

ABSOLUTE MAXIMUM RATINGS	N-Pkg	J-Pkg	T-Pkg
Supply Voltage, V_{IN}	40V	40V	40V
Collector Supply Voltage, V_C	40V	40V	40V
Output Current (Source or Sink)			
Steady-State	±500mA	±500mA	±1.0A
Peak Transient	±1.5A	±1.0A	±2.0A
Capacitive Discharge Energy	20μJ	15μJ	50μJ
Digital Inputs (see note)	5.5V	5.5V	5.5V
Power Dissipation at T_A = 25°C	1W	1W	3W
Derate above 50°C	10mW/°C	10mW/°C	25mW/°C
Power Dissipation at T (Leads/Case) = 25°C	3W	2W	25W
Derate for Ground Lead Temperature above 25°C	25mW/°C	—	—
Derate for Case Temperature above 25°C	—	16mW/°C	200mW/°C
Operating Temperature Range	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C	-65°C to +150°C
Load Temperature (Soldering, 10 seconds)	300°C	300°C	300°C

NOTE: All currents are positive into, negative out of the specified terminal.
Digital Drive can exceed 5.5V if input current is limited to 10mA.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1705 and 0°C to +70°C for the UC3705; V_S = V_C = 20V.)

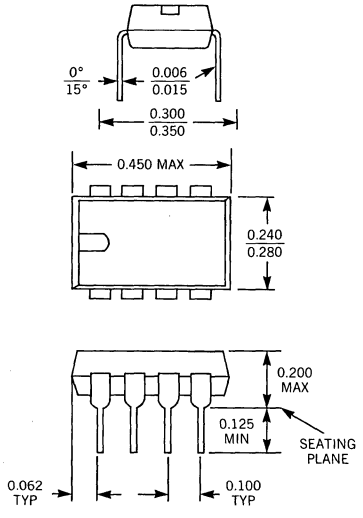
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
V_S Supply Current	V_S = 40V		6	8	mA
V_C Supply Current	V_C = 40V, Outputs Low		2	4	mA
V_C Leakage Current	V_S = 0, V_C = 30V		.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	V_I = 0		-0.6	-1.0	mA
Input Leakage	V_I = 5V		.05	0.1	mA
Output High Sat., V_C-V_O	I_o = -50mA			2.0	V
Output High Sat., V_C-V_O	I_o = -500mA			2.5	V
Output Low Sat., V_O	I_o = 50mA			0.4	V
Output Low Sat., V_O	I_o = 500mA			2.5	V
Thermal Shutdown			155		°C

TYPICAL SWITCHING CHARACTERISTICS (V_S = V_C = 20V, T_A = 25°C. Delays measured to 10% output change.)

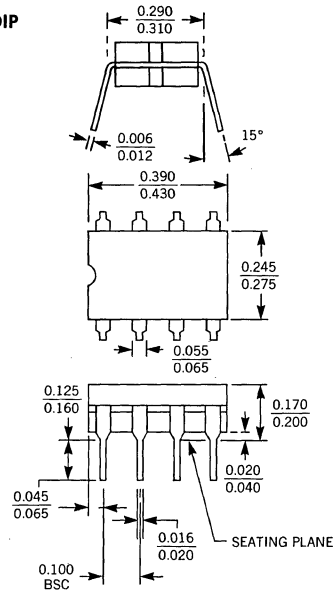
PARAMETER	TEST CONDITIONS	OUTPUT C_L =			UNITS
From Inv. Input to Output:		open	1.0	2.2	nF
Rise Time Delay		60	60	60	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		60	60	60	ns
90% to 10% Fall		25	40	50	ns
From N.I. Input to Output:					
Rise Time Delay		90	90	90	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		60	60	60	ns
90% to 10% Fall		25	40	50	ns
V_C Cross-Conduction Current Spike Duration	Output Rise	25			ns
	Output Fall	0			ns

MECHANICAL SPECIFICATIONS

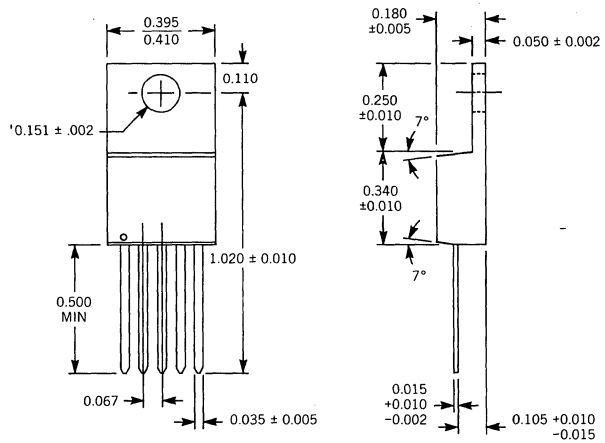
N-Package
8-Pin MINIDIP



J-Package
8-Pin CERDIP



T-Package
TO-220



FEATURES
- Dual, 1.5A Totem Pole Outputs
- 40nsec Rise and Fall into 1000pF
- Parallel or Push-Pull Operation
- Single-Ended to Push-Pull Conversion
- High-Speed, Power MOSFET Compatible
- Low Cross-Conduction Current Spike
- Analog, Latched Shutdown
- Internal Deadband Inhibit Circuit
- Low Quiescent Current
- 5 to 40V Operation
- Thermal Shutdown Protection
- 16-Pin Dual-In-Line Package

DESCRIPTION

The UC1706 family of output drivers are made with a high-speed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFET's. These devices implement three generalized functions as outlined below:

First: They accept a single-ended, low-current digital input of either polarity and process it to activate a pair of high-current, totem pole outputs which can source or sink up to 1.5A each.

Second: They provide an optional single-ended to push-pull conversion through the use of an internal flip-flop driven by double-pulse-suppression logic. With the flip-flop disabled, the outputs work in parallel for 3.0A capability.

Third: Protection functions are also included for pulse-by-pulse current limiting, automatic deadband control, and thermal shutdown.

These devices are available in a two-watt plastic "bat-wing" DIP for operation over a 0° to +70°C temperature range and, with reduced power, in a hermetically sealed cerdip for −55°C to +125°C operation.

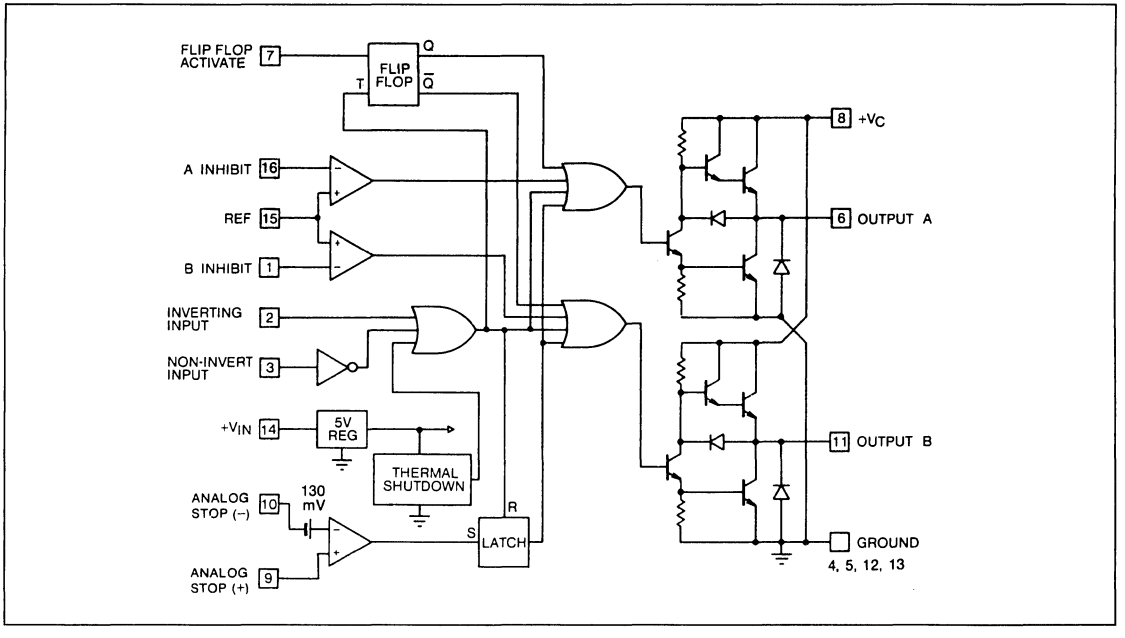
TRUTH TABLE

INV.	N.I.	OUT
H	H	L
L	H	H
H	L	L
L	L	L

OUT = $\overline{INV}$ and N.I.

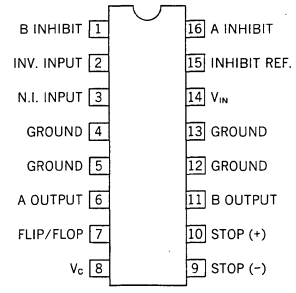
$\overline{OUT}$ = INV or $\overline{N.I.}$

BLOCK DIAGRAM



CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



Note: All four ground pins must be connected to a common ground.

ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg
Supply Voltage, V_{IN}	40V	40V
Collector Supply Voltage, V_C	40V	40V
Output Current (Each Output, Source or Sink)		
Steady-State	±500mA	±500mA
Peak Transient	±1.5A	±1.0A
Capacitive Discharge Energy	20μJ	15μJ
Digital Inputs	5.5V	5.5V
Inhibit Inputs	5.5V	5.5V
Stop Inputs	V_{IN}	V_{IN}
Power Dissipation at T_A = 25°C	2W	1W
Derate above 50°C	20mW/°C	10mW/°C
Power Dissipation at T (Leads/Case) = 25°C	5W	2W
Derate for Ground Lead Temperature above 25°C	40mW/°C	—
Derate for Case Temperature above 25°C	—	16mW/°C
Operating Temperature Range	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	
Load Temperature (Soldering, 10 Seconds)	300°C	

Note: All voltages are with respect to the four ground pins which must be connected together. All currents are positive into, negative out of the specified terminal.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55° to +125°C for the UC1706 and 0°C to +70°C for the UC3706; V_{IN} = V_C = 20V.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
V_{IN} Supply Current	V_{IN} = 40V		8	10	mA
V_C Supply Current	V_C = 40V, Outputs Low		4	5	mA
V_C Leakage Current	V_{IN} = 0, V_C = 30V		.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	V_I = 0		−0.6	−1.0	mA
Input Leakage	V_I = 5V		.05	0.1	mA
Output High Sat., V_C−V_O	I_o = −50mA			2.0	V
Output High Sat., V_C−V_O	I_o = −500mA			2.5	V
Output Low Sat., V_O	I_o = 50mA			0.4	V
Output Low Sat., V_O	I_o = 500mA			2.5	V
Inhibit Threshold	V_{REF} = 0.5V	0.4		0.6	V
Inhibit Threshold	V_{REF} = 3.5V	3.3		3.7	V
Inhibit Input Current	V_{REF} = 0		−10	−20	μA
Analog Threshold	V_{CM} = 0 to 15V	100	130	150	mV
Input Bias Current	V_{CM} = 0		−10	−20	μA
Thermal Shutdown			155		°C

UNITRODE INTEGRATED CIRCUITS
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TYPICAL SWITCHING CHARACTERISTICS (V_{IN} = V_C = 20V, T_A = 25°C. Delays measured 50% in to 50% out.)

PARAMETER	TEST CONDITIONS	OUTPUT C_L=			UNITS
From Inv. Input to Output:		open	1.0	2.2	nF
Rise Time Delay		110	130	140	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		80	90	110	ns
90% to 10% Fall		25	30	50	ns
From N.I. Input to Output:					
Rise Time Delay		120	130	140	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		100	120	130	ns
90% to 10% Fall		25	30	50	ns
V_C Cross-Conduction Current Spike Duration	Output Rise	25			ns
	Output Fall	0			ns
Inhibit Delay	Inhibit Ref. = 1V Inhibit = 0.5 to 1.5V	250			ns
Analog Shutdown Delay	Stop (+) Ref. = 0 Stop (−) Input = 0 to 0.5V	180			ns

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CIRCUIT DESCRIPTION

Outputs

The totem-pole outputs have been designed to minimize cross-conduction current spikes while maximizing fast, high-current rise and fall times. Current limiting can be done externally either at the outputs or at the common V_C pin. The output diodes included have slow recovery and should be shunted with high-speed external diodes when driving high-frequency inductive loads.

Flip/Flop

Grounding pin 7 activates the internal flip-flop to alternate the two outputs. With pin 7 open, the two outputs operate simultaneously and can be paralleled for higher current operation. Since the flip-flop is triggered by the digital input, an off-time of at least 200nsec must be provided to allow the flip/flop to change states. Note that the circuit logic is configured such that the "OFF" state is defined as the outputs low.

Digital Inputs

With both an inverting and non-inverting input available, either active-high or active-low signals may be accepted. These are true TTL compatible inputs — the threshold is approximately 1.2V with no hysteresis; and external pull-up resistors are not required.

Inhibit Circuit

Although it may have other uses, this circuit is included to eliminate the need for deadband control when driving relatively slow bipolar power transistors. A diode from each inhibit input to the opposite power switch collector will keep one output from turning-on until the other has turned-off. The threshold is determined by the voltage on pin 15 which can be set from 0.5 to 3.5V. When this circuit is not used, ground pin 15 and leave 1 and 16 open.

Analog Shutdown

This circuit is included to get a latched shutdown as close to the outputs as possible, from a time standpoint. With an internal 130mV threshold, this comparator has a common-mode range from ground to (V_{IN} − 3V). When not used, both inputs should be grounded. The time required for this circuit to latch is inversely proportional to the amount of overdrive but reaches a minimum of 180nsec. As with the flip-flop, an input off-time of at least 200nsec is required to reset the latch between pulses.

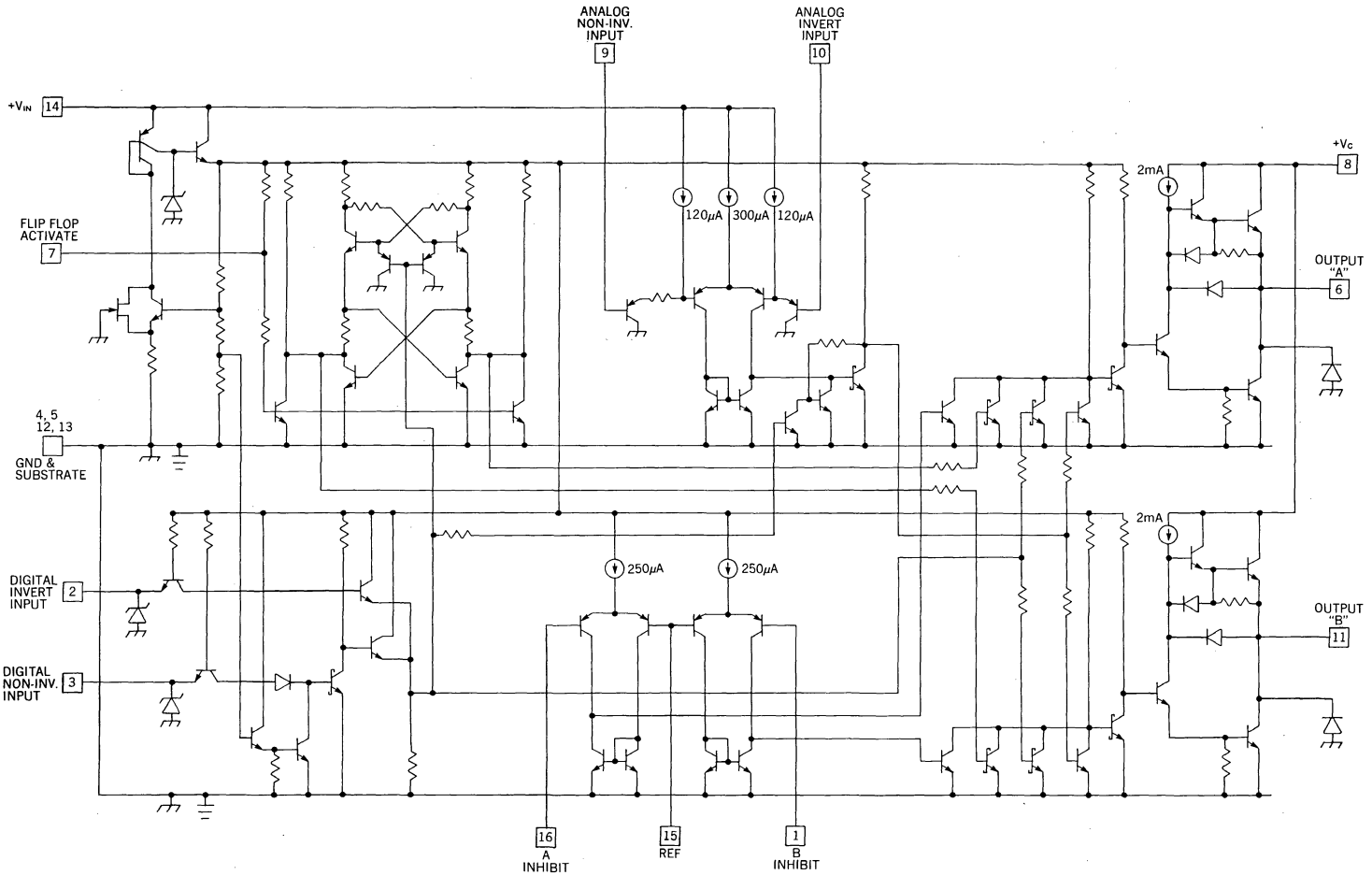
Supply Voltage

With an internal 5V regulator, this circuit is optimized for use with a 7 to 40V supply; however, with some slight response time degradation, it can also be driven from 5V. When V_{IN} is low, the entire circuit is disabled and no current is drawn from V_C. When combined with a UC1840 PWM, the Driver Bias switch can be used to supply V_{IN} to the UC1706. V_{IN} switching should be fast as if V_C is high, undefined operation of the outputs may occur with V_{IN} less than 5V.

Thermal Considerations

Should the chip temperature reach approximately 155°C, a parallel, non-inverting input is activated driving both outputs to the low state.

SIMPLIFIED SCHEMATIC DIAGRAM



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LINEAR INTEGRATED CIRCUITS

Dual Channel Power Driver

UC1707
UC3707

FEATURES

- Two Independent Drivers
- 1.5A Totem Pole Outputs
- Inverting and Non-Inverting Inputs
- 40ns Rise and Fall into 1000pF
- High-Speed, Power MOSFET Compatible
- Low Cross-Conduction Current Spike
- Analog Shutdown with Optional Latch
- Low Quiescent Current
- 5V to 40V Operation
- Thermal Shutdown Protection
- 16-Pin Dual-In-Line Package

DESCRIPTION

The UC1707 family of power drivers is made with a high-speed Schottky process to interface between low-level control functions and high-power switching devices — particularly power MOSFETs. These devices contain two independent channels, each of which can be activated by either a high or low input logic level signal. Each output can source or sink up to 1.5A as long as power dissipation limits are not exceeded.

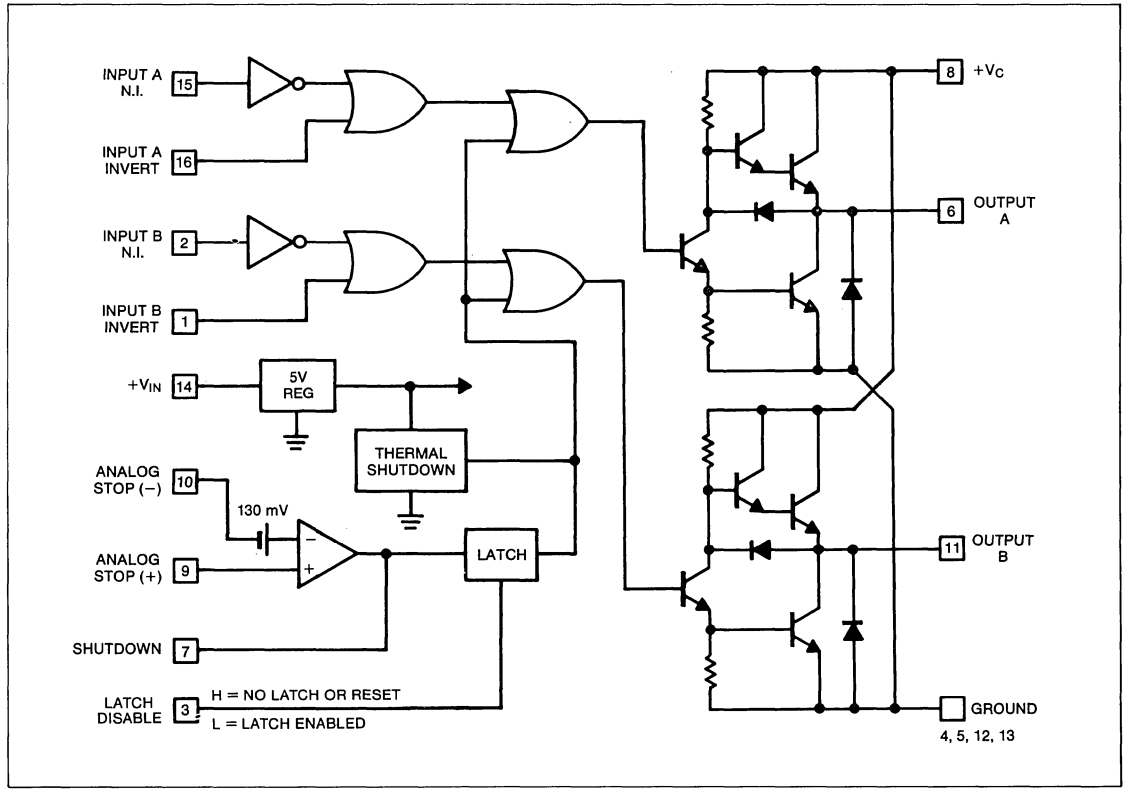
Although each output can be activated independently with its own inputs, it can be forced low in common through the action either of a digital high signal at the Shutdown terminal or a differential low-level analog signal. The Shutdown command from either source can either be latching or not, depending on the status of the Latch Disable pin.

Supply voltage for both V_{IN} and V_C can independently range from 4.5V to 40V. V_{IN} can also be used to gate the outputs as when V_{IN} is less than 4V, both outputs are held in the high impedance state and no current is drawn from V_C.

These devices are available in a two-watt plastic "bat-wing" DIP for operation over a 0°C to +70°C temperature range and, with reduced power, in a hermetically sealed cerdip for −55°C to +125°C operation.

5

BLOCK DIAGRAM



UNITRODE

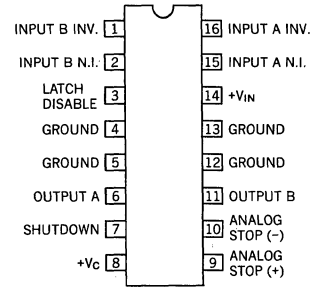
ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg
Supply Voltage, V_{IN}	40V	40V
Collector Supply Voltage, V_C	40V	40V
Output Current (Each Output, Source or Sink)		
Steady-State	±500mA	±500mA
Peak Transient	±1.5A	±1.0A
Capacitive Discharge Energy	20μJ	15μJ
Digital Inputs (see note)	5.5V	5.5V
Analog Stop Inputs	V_{IN}	V_{IN}
Power Dissipation at T_A = 25°C	2W	1W
Derate above 50°C	20mW/°C	10mW/°C
Power Dissipation at T (Leads/Case) = 25°C	5W	2W
Derate for Ground Lead Temperature above 25°C	40mW/°C	—
Derate for Case Temperature above 25°C	—	16mW/°C
Operating Temperature Range	-55°C to +125°C	
Storage Temperature Range	-65°C to +150°C	
Load Temperature (Soldering, 10 seconds)	300°C	

NOTE: All voltages are with respect to the four ground pins which must be conected together.
All currents are positive into, negative out of the specified terminal.
Digital Drive can exceed 5.5V if input current is limited to 10mA.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J OR N PACKAGE



NOTE: All four ground pins must be connected to a common ground.

TRUTH TABLE (Each Channel)

INV.	N.I.	OUT
H	H	L
L	H	H
H	L	L
L	L	L

OUT = $\overline{\text{INV.}}$ and N.I.

$\overline{\text{OUT}}$ = INV. or $\overline{\text{N.I.}}$

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1707 and 0°C to +70°C for the UC3707; V_{IN} = V_C = 20V.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
V_{IN} Supply Current	V_{IN} = 40V		10	12	mA
V_C Supply Current	V_C = 40V, Outputs Low		4	5	mA
V_C Leakage Current	V_{IN} = 0, V_C = 30V		.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	V_I = 0		-0.6	-1.0	mA
Input Leakage	V_I = 5V		.05	0.1	mA
Output High Sat., V_C-V_O	I_o = -50mA			2.0	V
Output High Sat., V_C-V_O	I_o = -500mA			2.5	V
Output Low Sat., V_O	I_o = 50mA			0.4	V
Output Low Sat., V_O	I_o = 500mA			2.5	V
Analog Threshold	V_{CM} = 0V to 15V	100	130	150	mV
Input Bias Current	V_{CM} = 0		-10	-20	μA
Thermal Shutdown			155		°C
Shutdown Threshold	Pin 7 Input	0.4	1.0	2.2	V
Latch Disable Threshold	Pin 3 Input	0.8	1.2	2.2	V

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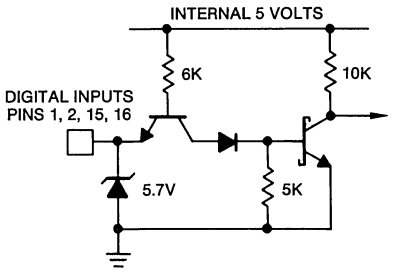
TYPICAL SWITCHING CHARACTERISTICS (V_{IN} = V_C = 20V, T_A = 25°C. Delays measured to 10% output change.)

PARAMETER	TEST CONDITIONS	OUTPUT C_L =			UNITS
From Inv. Input to Output:		open	1.0	2.2	nF
Rise Time Delay		60	60	60	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		60	60	60	ns
90% to 10% Fall		25	40	50	ns
From N.I. Input to Output:					
Rise Time Delay		90	90	90	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		60	60	60	ns
90% to 10% Fall		25	40	50	ns
V_C Cross-Conduction Current Spike Duration	Output Rise	25			ns
	Output Fall	0			ns
Analog Shutdown Delay	Stop (+) Ref. = 0 Stop (−) Input = 0V to 0.5V	160			ns
Digital Shutdown Delay	2V Input on Pin 7	50			ns

5

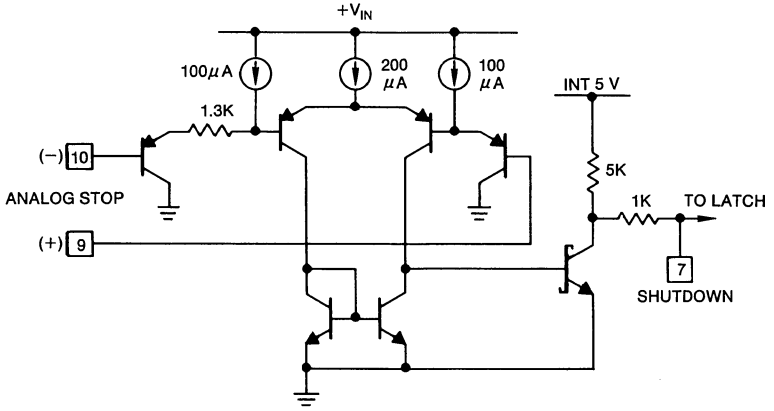
SIMPLIFIED INTERNAL CIRCUITRY

Typical Digital Input Gate



The input zener may be used to clamp input signal voltages higher than 5V as long as the zener current is limited to 10mA max. External pull-up resistors are not required.

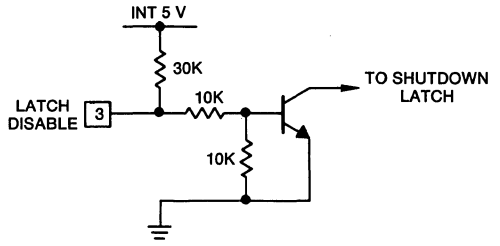
Analog Shutdown Comparator Circuit



The input common-mode voltage range is from ground to (V_{IN}−3V). When not used both inputs should be grounded. Activate time is a function of overdrive with a minimum value of 160ns. Pin 7 serves both as a comparator output and as a common digital shutdown input. A high signal here will accomplish the fastest turn off of both outputs. Note that "OFF" is defined as the outputs low.

SIMPLIFIED INTERNAL CIRCUITRY (continued)

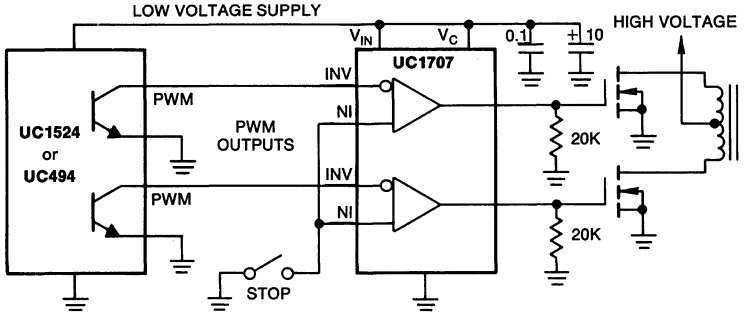
Latch Disable



The Shutdown latch is disabled when pin 3 is open. An impedance of 4KΩ or less from pin 3 to ground will allow a shutdown signal to set the latch which can then be reset by either recycling the V_{IN} supply or by momentarily (>200ns) raising pin 3 high.

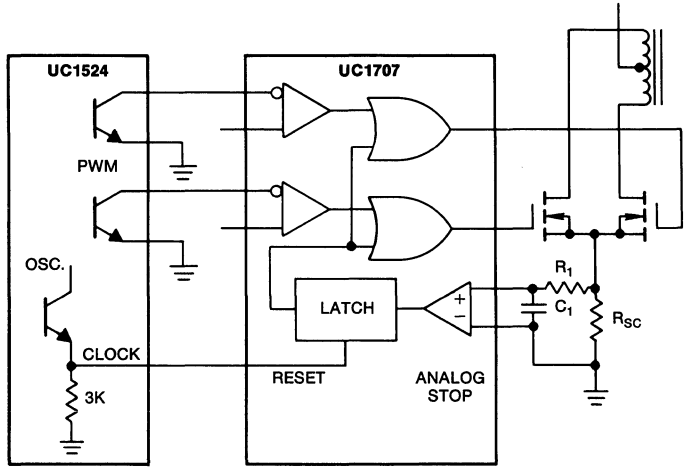
APPLICATIONS

Conventional Dual-Output Drive



Driving the inverting inputs from open-collector, dual-output PWM Controllers. If unneeded for programming functions, the non-inverting inputs can be left open. Note that the high peak current drive for MOS gates requires good supply decoupling at V_C. V_{IN} and V_C need not be at the same levels. The 20K resistors hold the FETs off during startup when the UC1707 output impedance is high.

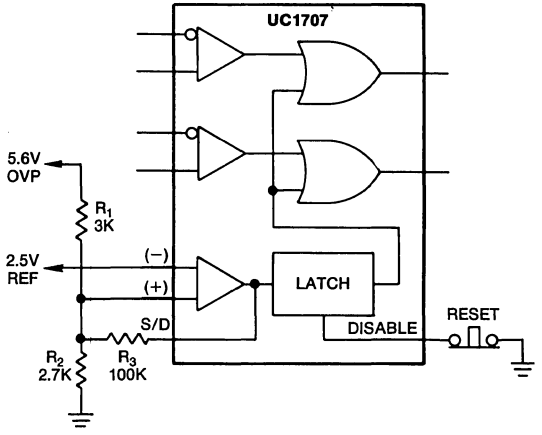
Current Limiting



The Analog shutdown can give pulse-by-pulse current limiting with a reset pulse from the clock output of the UC1524. R_1C_1 is used to filter leading edge spikes.

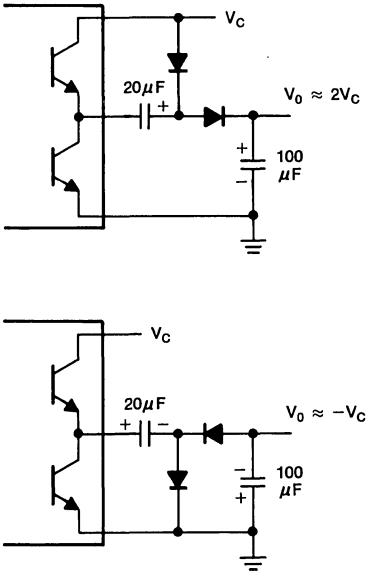
APPLICATIONS (continued)

Over-Voltage Protection



With an external reference, the shutdown comparator can be used for over-voltage protection. R_1 and R_2 set the shutdown level while R_3 adds positive feedback for hysteresis.

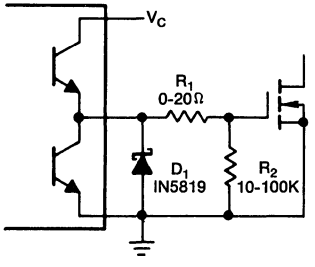
Voltage Multipliers



When driven with a TTL square wave drive, the low output impedance of the UC1707 allows ready implementation of charge pump voltage converters.

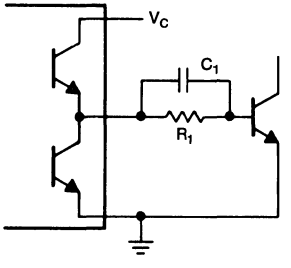
OUTPUT STAGE COUPLING

Power MOSFET



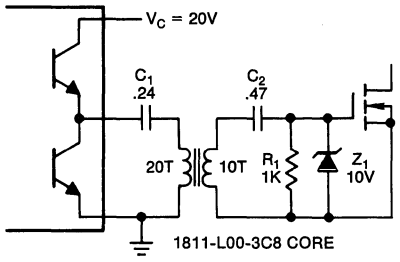
Simple direct drive to gate requires close coupling:
- R_1 adds damping at the expense of gate rise time.
- R_2 insures against turn on with leakage currents.
- D_1 is necessary if ringing would drive output pin negative.

Bipolar Power Transistor

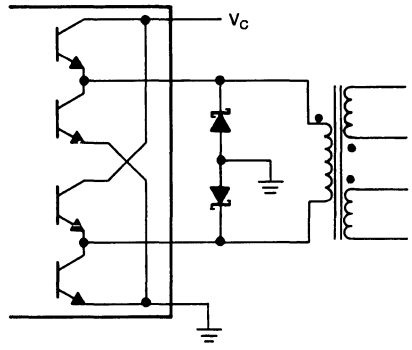


Fast turn-off bipolar switch drive:
- Charge on C_1 will drive base negative at turn-off.
- For large V_C, clamping to prevent E-B breakdown may be necessary.
- V_{OL} at low current will keep bipolar switch off.

TRANSFORMER COUPLING



Single-ended transformer drive:
C_1 blocks DC.
Z_1 clamps gate voltage, both positive and negative.



Balanced Transformer Drive:
With no net DC in primary, capacitors are unnecessary.
Clamp diodes necessary if leakage inductance drives outputs negative.
May require secondary snubbing circuitry.

LINEAR INTEGRATED CIRCUITS

Dual Smart Switch

UC1728
UC3728

FEATURES

- Independent Floating Switches
- PWM Current Control
- Supply Voltages to 46V
- Load Currents to 1A
- Transparent Input Latches
- Programmable Current Level
- Three-State Status Outputs
- Over-Current Latch
- Under-Voltage Lockout
- Thermal Shutdown

DESCRIPTION

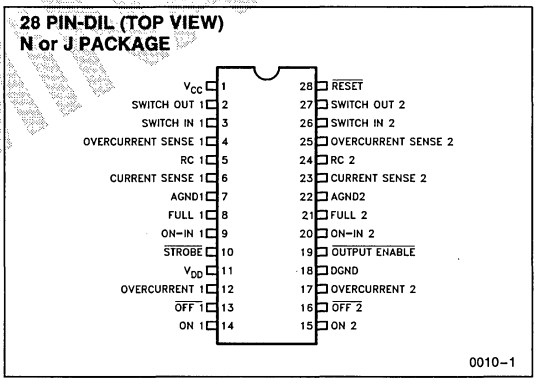
This IC performs load control and status monitoring for two inductive loads up to 1 amp each. Loads can be ground referenced, positive supply referenced, or floating, depending on the control and monitoring desired. Load current regulation is provided by fixed off-time pulse-width modulation, so that efficient use of low-voltage inductive loads from higher supplies is practical. Digital status outputs indicate load off, load on, and overload conditions. Latching over-current detection circuitry protects the system from shorts to ground and shorted loads. These parts are available in ceramic or plastic dual-inline packages and heremetic surface-mount chip carriers.

ABSOLUTE MAXIMUM RATINGS

V_{DD} Voltage 7V
V_{CC} Voltage 50V
Switch Input Voltage ..... V_{CC} +0.3V
Logic Input Voltage ..... V_{DD} +0.3V
Switch Current, Per Channel 1.5A
Operating Temperature,
UC1728 ..... −55°C to +125°C
UC3728 ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Power Dissipation at T_C = 70°C 1W

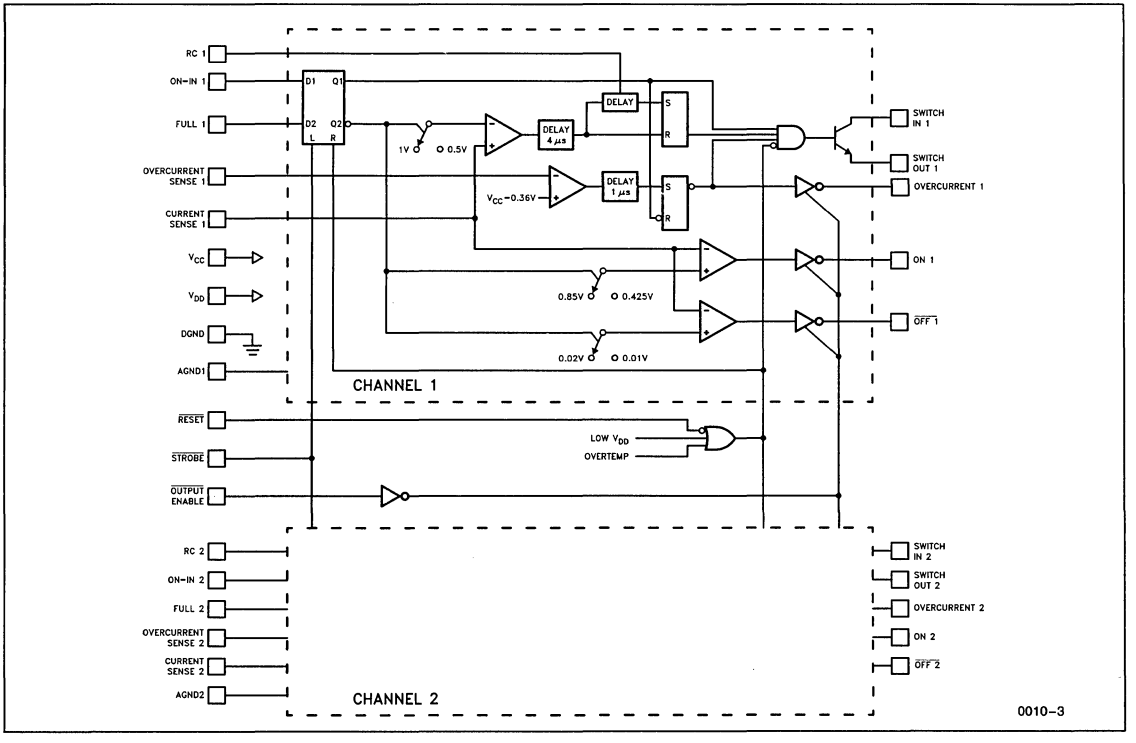
CONNECTION DIAGRAMS

28 PIN-DIL (TOP VIEW)
N or J PACKAGE



0010-1

BLOCK DIAGRAM



0010-3

5

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply over $-55°C < T_A < +125°C$ for the UC1728 and $0°C < T_A < +70°C$ for the UC3728. Unless otherwise stated, $V_{DD} = +5V$, $V_{CC} = +32V$.)

PARAMETER	TEST CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
V_{DD} Enable Threshold		3.5	4	4.5	V
V_{DD} Operating Range		4.5		5.5	V
V_{DD} Current	$V_{DD} = 5.5V$		12	30	mA
V_{CC} Current	$V_{CC} = 46V$		1.5	6	mA
Logic Input Current	$V_{IN} = 0V$	−50	−5		µA
Current Sense Input Current	$V_{CS} = 0V$	−15	−3		µA
Overcurrent Sense Input Current	$V_{OCS} = V_{CC}$	−10	−1		µA
Logic Input Threshold	$4.5 < V_{DD} < 5.5$	0.8	1.4	2	V
Fault Threshold Overcurrent Sense Input	$13 < V_{CC} < 46$ Measured to V_{CC}	−0.4	−0.36	−0.32	V
PWM Threshold Current Sense Input	FULL = 1	0.92	1	1.08	V
	FULL = 0	0.45	0.5	0.55	V
ON Threshold Current Sense Input	FULL = 1	780	850	890	mV
	FULL = 0	390	425	450	mV
OFF Threshold Current Sense Input	FULL = 1	10	20	30	mV
	FULL = 0	5	10	15	mV
Switch Drop	I = 200 mA		0.95	1.4	V
	I = 1A		1.05	1.8	V
Switch Leakage	$S_I = 32V$, $S_O = 0V$			200	µA
Logic Output Low	$I_{LOGIC} = 4$ mA		0.2	0.45	V
Logic Output High	$I_{LOGIC} = -4$ mA	2.4	3.3		V
Logic Output Leakage	$0 < V_{LOGIC} < 5V$	−10		10	µA
OFF Time	$R_T = 36k$, $C_T = 1$ nF	15	25	35	µs
Current Sense Delay			4		µs
Overcurrent Sense Delay			1		µs

APPLICATION INFORMATION

In the adjoining figure, one half of the UC1728 is shown in a typical application driving a solenoid. The solenoid current is set by current sense resistor R_S, and programmed by the FULL input as per the following:

FULL = 1 $I_{PEAK} = 1V/R_S$

FULL = 0 $I_{PEAK} = 0.5V/R_S$

The solenoid current will charge up to the programmed peak current at a rate approximately equal to:

$dI/dt = V_{CC}/L$, where L is the load inductance

and coast down at a slower rate for a fixed off-time of about:

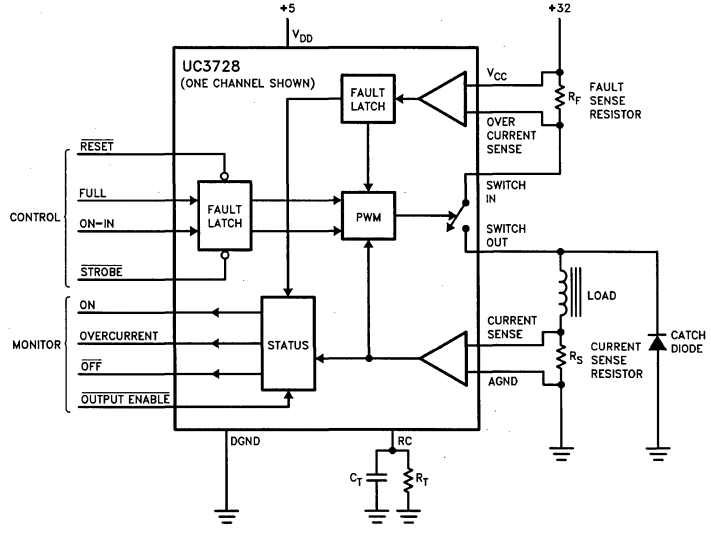
$T_{OFF} = 0.69\ R_T\ C_T$

The slower rate is determined by the series voltage drop in the current sense resistor, the drop in the load resistance, and the Catch Diode voltage working with the load inductance. Typical designs target the PWM frequency over 20 kHz to avoid audible noise. If the duty cycle is less than 50%, the PWM frequency will be controlled by the off time, and an appropriate off time will be around 20 µs.

The overcurrent threshold is set by the fault resistor, R_F. The fault latch will trip when the current in that resistor reaches:

$$I_{FAULT} = 0.36V/R_F$$

The catch diode should be returned to ground rather than R_S so that load current always flows through R_S, making the status information continuously valid through the PWM cycle. Returning the catch diode to ground also produces a more smooth voltage waveform on R_S, which lessens the potential of false triggering the PWM.



0010-4

LINEAR INTEGRATED CIRCUITS
Half-Bridge Bipolar Switch

FEATURES
- Source or Sink 4.0A
- Supply Voltage to 35V
- High-Current Output Diodes
- Tri-State Operation
- TTL and CMOS Input Compatibility
- Thermal Shutdown Protection
- 300kHz Operation
- Low-Cost TO-220 Package

DESCRIPTION

This device is a monolithic integrated circuit designed to provide high-current switching with low saturation voltages when activated by low-level logic signals. Source and sink switches may be independently activated without regard to timing as a built-in interlock will keep the sink off if the source is on.

This driver has the high-current capability to drive large capacitive loads with fast rise and fall times; but with high-speed internal flyback diodes, it is also ideal for inductive loads. Two UC2950s can be used together to form a full bridge, bipolar motor driver compatible with high frequency chopper current control.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_C ..... 8V to 35V
Output Voltage Range, V_O ..... -3.0V to V_C+3V
Input Voltage Range, V_{IN} ..... -0.3V to +7.0V
Peak Output Current (100ms, 10% DC) ..... ±4.0A
Continuous Output Current ..... ±2.0A
Power Dissipation with Heat Sink 15W
  Derate for tab T_C > 75°C ..... 0.2W/°C
Power Dissipation in Free Air 2W
  Derate for T_A > 75°C ..... 30mW/°C
Operating Temperature Range, T_A ..... -20°C to +100°C
Storage Temperature Range, T_S ..... -55°C to +125°C

TRUTH TABLE

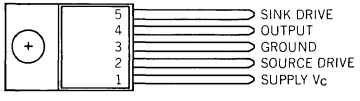
Source Drive Pin 2	Sink Drive Pin 5	Output Pin 4
Low	Low	Low
Low	High	OFF
High	Low	High
High	High	High

Note: With no load, output voltage will be HIGH in the OFF state.

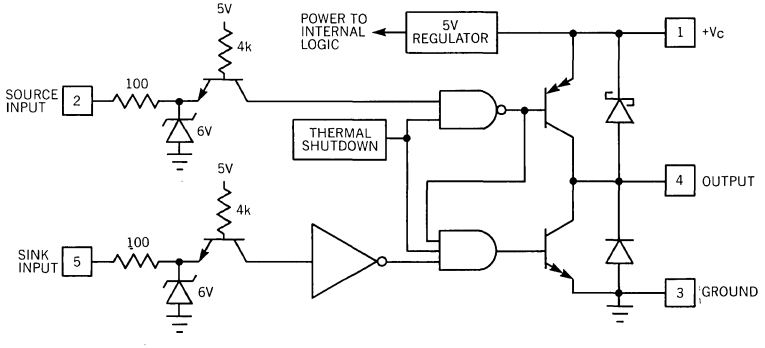
5

CONNECTION DIAGRAM

5-PIN TO-220 (TOP VIEW)
T PACKAGE



SIMPLIFIED SCHEMATIC



UNITRODE

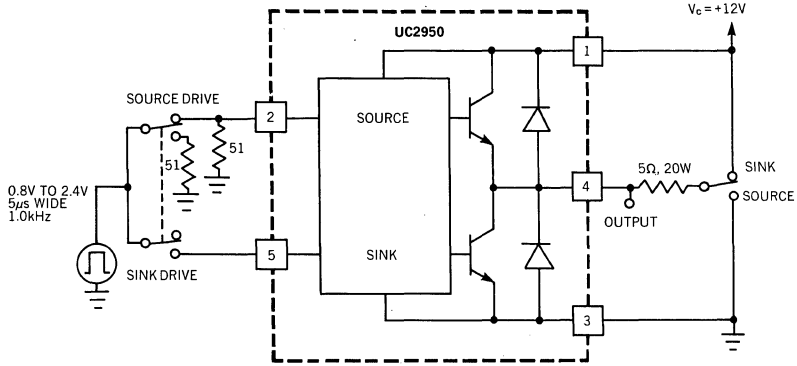
ELECTRICAL CHARACTERISTICS (Unless otherwise stated, V_C = 35V, T_A = −20°C to +100°C, V_{IL} = 0.8V, V_{IH} = 2.4V for either input.)

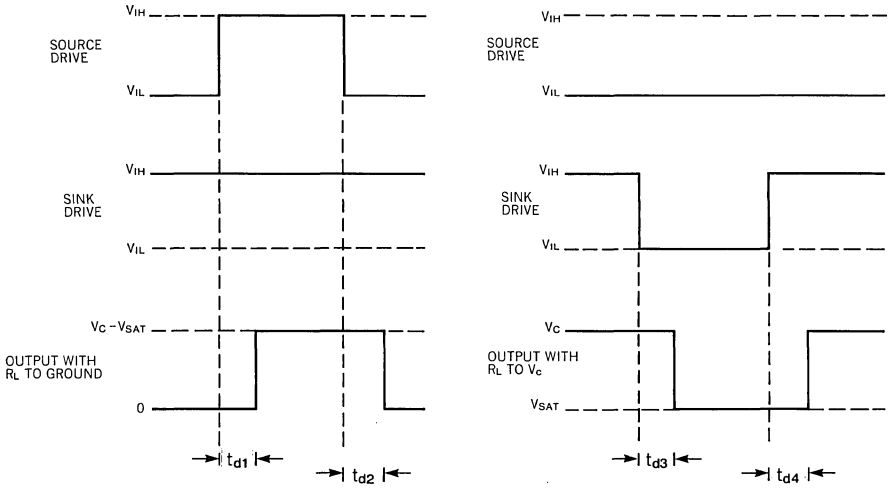
PARAMETERS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Leakage to V_C	Output Off		20	500	μA
Output Leakage to Ground	Output Off		−200	−500	μA
Output Sink Saturation	V_{OL}, I_L = 2.0A		1.2	2.0	V
Output Source Saturation	(V_C−V_{OL}), I_L = −2.0A		1.2	2.0	V
Sink Diode Forward Voltage	I_D = −2.0A		1.4	2.0	V
Source Diode Forward Voltage	I_D = 2.0A		1.4	2.0	V
Input Current	Either Input, V_I = 5V		20	100	μA
Input Current	Either Input, V_I = 0V		−1.0	−1.6	mA
Supply Current	Output High		20	30	mA
Supply Current	Output Low		10	20	mA

SWITCHING CHARACTERISTICS (See Test Circuit. V_C = 12V, R_L = 5Ω, T_A = 25°C. Guaranteed by design, not 100% tested in production.)

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Source Turn-On Delay, t_{d1}		300	500	ns
Source Turn-Off Delay, t_{d2}		1.0	2.0	μs
Sink Turn-On Delay, t_{d3}		200	400	ns
Sink Turn-Off Delay, t_{d4}		100	300	ns
Cross-Conduction Current Spike When Source and Sink are Activated Together		0.6	1.0	μs

SWITCHING TEST CIRCUIT

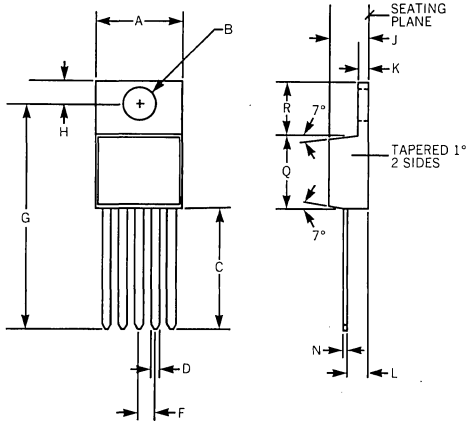




5

MECHANICAL SPECIFICATIONS

T-Package
5-Pin TO-220



	INCHES	MILLIMETERS
A	0.395–0.420	10.03–10.67
B	0.151±0.002 DIA.	3.835±0.051 DIA.
C	0.540±0.015	13.716±0.381
D	0.035±0.005 TYP.	0.889±0.127 TYP.
F	0.067±0.005 TYP.	1.702±0.127 TYP.
G	1.020±0.015	25.91±0.381
H	0.110±0.010	2.794±0.254
J	0.180±0.005	4.572±0.127
K	0.050±0.002	1.270±0.051
L	$0.105^{+0.010}_{-0.015}$	$2.667^{+0.254}_{-0.381}$
N	$0.015^{+0.010}_{-0.002}$	$0.381^{+0.254}_{-0.051}$
Q	0.340±0.010	8.636±0.254
R	0.250±0.010	6.350±0.254

LINEAR INTEGRATED CIRCUITS

Smart Switch

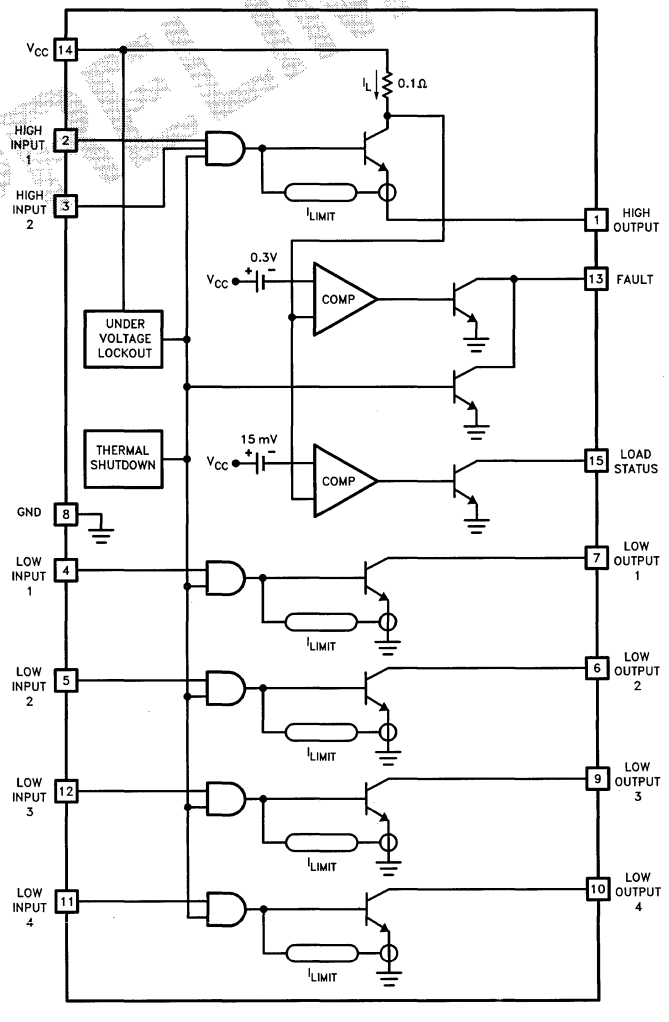
FEATURES

- 60V Operation
- 4 Independent Low Side Switches with 1A Capability
- 4.5A High Side Switch Capability
- Over and Under Current Fault Indication
- Short Circuit and Thermal Shutdown Protection
- Under-Voltage Lockout
- 15 Lead, 25W Multiwatt Package

DESCRIPTION

The UC3720 Smart Switch contains a fully protected 4.5A high side switch along with four 1A low side switches. This device allows for the control of up to four separate loads while monitoring for both shorted or open conditions at the point of load. A full range of protection circuitry including instantaneous current limit, under-voltage lockout, hiccup mode current limit, and thermal shutdown allow for safe reliable operation.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage V_{CC} 60V

Output Current, High Side Switch (pin 1)
Non-Repetitive ($t \leq 50\ \mu s$) ..... −8A
DC Operation ..... −4.5A

Output Current, Low Side Switches (pins 6, 7, 9, 10)
Non-Reptitive ($t = 50\ \mu s$) 1.5A
DC Operation 1A

Logic Inputs ..... −0.3 to 7V

Total Power Dissipation (at $T_{CASE} = 75°C$) 25W

Storage and Junction Temperature ..... −40°C to +150°C

THERMAL DATA

Thermal Resistance Junction-Case, θ_{jc} ..... 3°C/W Max

Thermal Resistance Junction-Ambient, θ_{ja} ..... 35°C/W Max

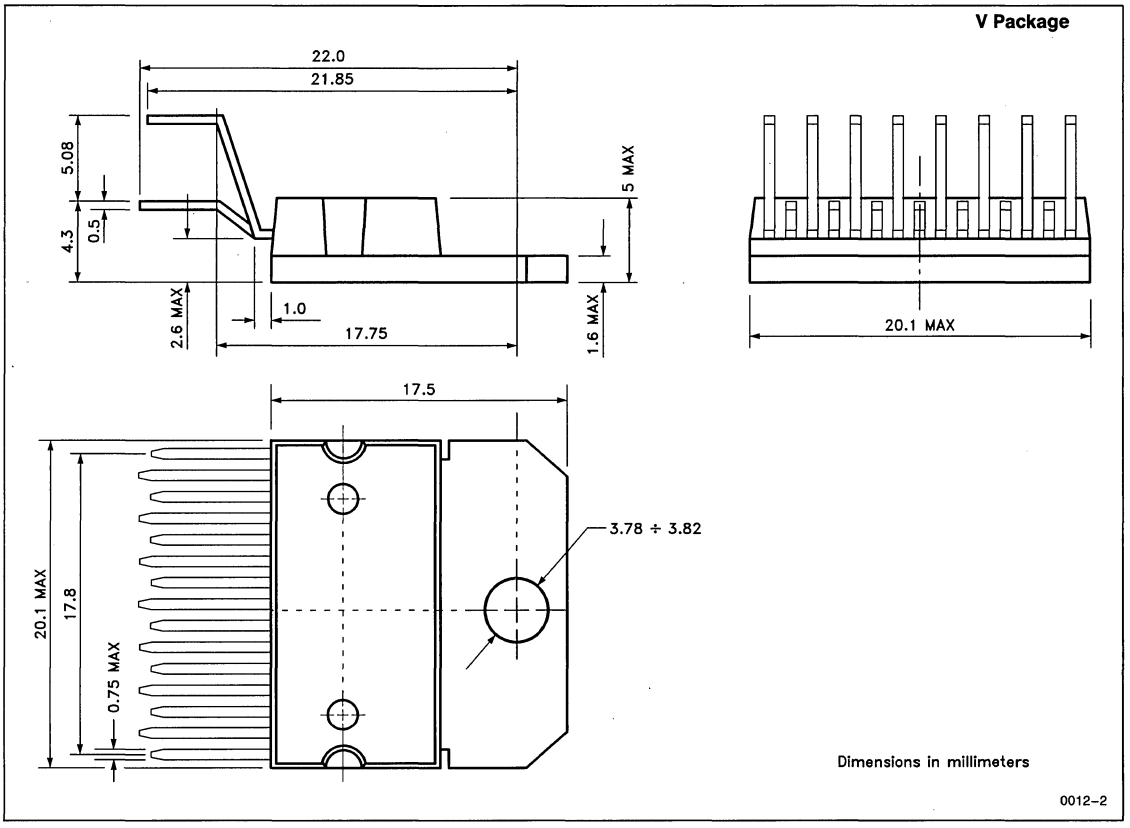
Note: 1. All voltages are with respect to ground, pin 8. Currents are positive into, negative out of the specified terminal.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = 0°C$ to $+70°C$; $V_{IN} = 28$ VDC)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Voltage		8		40	V
Supply Current	$V_{PIN1} = V_{PIN2} = 0V$			20	mA
LOGIC INPUTS					
High-Level Input Voltage		3.0			V
Low-Level Input Voltage				0.8	V
High-Level Input Current	$V_{IN} = 5.5V$			250	μA
Low-Level Input Current	$V_{IN} = 0.4V$	−160			μA
LOAD STATUS					
Output Sink Current	$V_{OUT} = 0.4V$	0.5			mA
Current Detect Threshold		100		200	mA
FAULT					
Output Sink Current	$V_{OUT} = 0.4V$	0.5			mA
Overcurrent Threshold		2.8	3.0	3.2	A
U.V. Lockout Threshold		6.0		8.0	V
Thermal Shutdown			160		°C
HIGH SIDE SWITCH					
V_{SAT} ($V_{PIN14} - V_{PIN1}$)	$I_{LOAD} = 3A$			2	V
Output Leakage Current				100	μA
Output Current Limit			8.0		
LOW SIDE SWITCHES					
V_{SAT} ($V_{PIN6,7,9,10}$)	$I_{LOAD} = 0.75A$			1.4	V
Output Leakage Current	$V_O = 28V$			50	μA
Output Current Limit			1.5		A

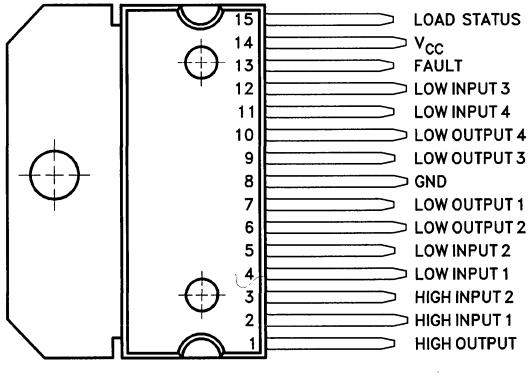
5

MECHANICAL DATA

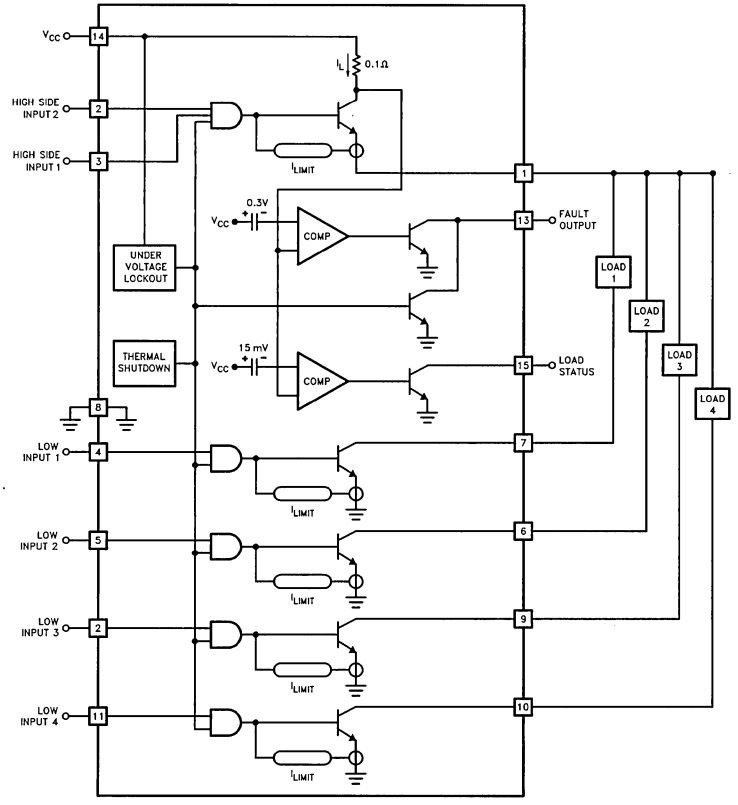


CONNECTION DIAGRAM

(TOP VIEW)



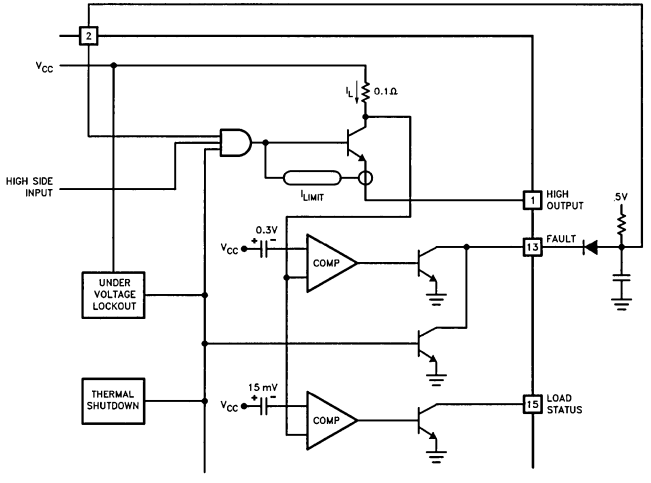
TYPICAL APPLICATIONS



0012-4

TYPICAL LOAD CONFIGURATION

Hiccup-Mode Current Limit



0012-5

Five-Channel Programmable Current Switch

FEATURES

- Five Current-Sinking Switches
- Peak Current Programmable from 0.5 to 2.5A
- Internal Current Sensing
- Low-Saturation Outputs Can Block 40V
- TTL Compatible Inputs
- Diagnostic Signal Detects Open Load or Inoperative Switch
- Thermal Sensor Detects Excessive Chip Temperature
- High Power Multiwatt® or Standard DIP Packages

DESCRIPTION

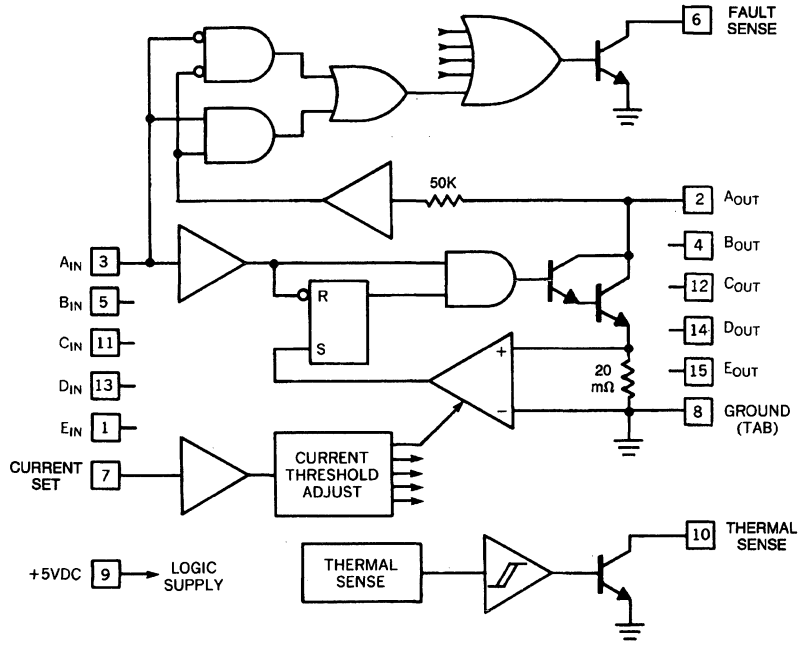
This high-power monolithic circuit consists of five identical, low-side, high-current switches plus a common programmable circuit which sets the peak current limit for all five channels. This current limit threshold—which immediately latches off the power switch when reached—can be programmed over a range of 0.5 to 2.5A. Each switch channel also contains a diagnostic circuit which compares the output response to the input command and provides, on a single fault-sense pin, an indication of a malfunction in either state of any switch. Finally, there is a temperature sensing circuit which switches on when the chip temperature exceeds a value of approximately 160°C. This circuit does not cause shutdown, but provides an indication to the user of an over-temperature condition.

Each current switch is a high-gain grounded-emitter NPN Darlington power device with internal current sensing. This switch is off with the input low and switches on with an input voltage above a two volt threshold. If the current through the switch increases to a value greater than that programmed by the current adjust pin, the switch will be immediately latched off regardless of the input command. Lowering the input signal below threshold will reset the latch allowing the switch to turn on again with the next positive excursion of the input.

The UC3722 is ideal for driving multiple inductive loads such as printer hammers or stepper motor phases to control peak current while providing maximum voltage across the coil. In the Multiwatt package, this device is able to handle up to 25W of internal power dissipation while the DIP package, with only one watt capability, should be considered only for low current and/or low duty cycle applications.

BLOCK DIAGRAM

UC3722
FIVE CHANNEL CURRENT SWITCH



Note: Pin numbers shown for Multiwatt Package

Multiwatt® is a registered trademark of SGS Corporation.

ABSOLUTE MAXIMUM RATINGS

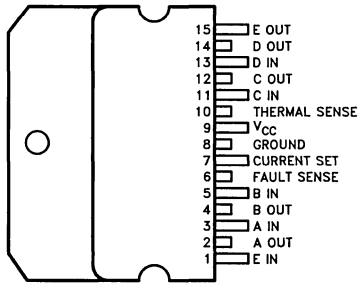
Collector Supply Voltage, V_C ..... +40V
Peak Collector Current, I_O ..... +3.0A
Logic Supply Voltage, V_{CC} ..... +7V
Fault and Thermal Sense Voltage ..... +40V
Fault and Thermal Sense Current ..... +20 mA
Input Signal Voltage, V_{IN} ..... −0.3 to +7.0V
Current Set Voltage ..... 0 to V_{CC}
Multiwatt Power Dissipation (T_{TAB} = +75°C) ..... +25W
Derate for Tab Temperature > +75°C ..... +0.3 W/°C
Dual-In-Line Power Dissipation (T_A = +25°C) ..... +1.0W
Derate for T_A > +25°C ..... +10 mW/°C
Operating Junction Temperature ..... −55°C to +150°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

THERMAL DATA

Multiwatt Thermal Resistance,
Junction to Case, θ_{JC} ..... +3°C/W
Multiwatt Thermal Resistance,
Junction to Ambient, θ_{JA} ..... +35°C/W
Plastic DIL Thermal Resistance,
Junction to Case, θ_{JC} ..... +50°C/W
Plastic DIL Thermal Resistance,
Junction to Ambient, θ_{JA} ..... +100°C/W

CONNECTION DIAGRAMS

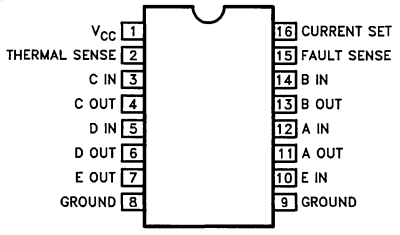
MULTIWATT (TOP VIEW)
VH PACKAGE



0003-1

Tab connected to Pin 8
Note: Power Tab must be connected to electrical ground.

DIL (TOP VIEW)
N PACKAGE



0003-3

5

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C; V_{CC} = +5V, V_C = +35V, V_{CS} = V_{CC} = +5V)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	V_{CC} = 5V		20	25	mA
Thermal Sense Leakage	V_{TS} = 40V		0.01	10	µA
Thermal Sense Saturation*	I_{TS} = 5 mA		0.1	0.4	V
Fault Sense Leakage	V_{FS} = 40V		0.01	10	µA
Fault Sense Saturation	I_{FS} = 5 mA		0.1	0.4	V
Current Set Input Bias	V_{CS} = 5V		2	10	µA
Thermal Sense Activation*			160		°C
Note: The following specifications apply to each channel tested separately					
Input Bias Current	V_{IN} = 0.4V		−0.2	−0.5	mA
Input Bias Current	V_{IN} = 4.0V		0.2	0.5	mA
Min. Input Turn-On Voltage			2.3	3.2	V
Max. Input Reset Voltage		0.8	1.7		V
Output Saturation	I_O = 1.0A		1.2	2.0	V
Output Saturation	I_O = 2.5A		1.8	2.2	V
Peak Output Current	V_{CS} = V_{CC}		2.7		A
Peak Output Current	V_{CS} = V_{CC} − 0.5V		1.5		A
Peak Output Current	V_{CS} = V_{CC} − 1.5V		0.5		A
Output Leakage	V_O = 40V		0.2	1.0	mA
Turn-On Delay*	See Test Circuit		100		ns
Turn-Off Delay*			500		ns
Current Shutdown Delay*			200		ns

*This parameter not 100% tested in production

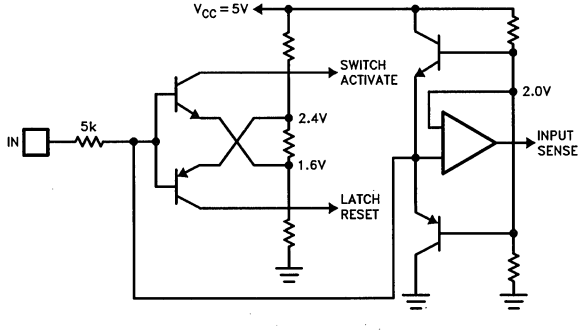
APPLICATION NOTES

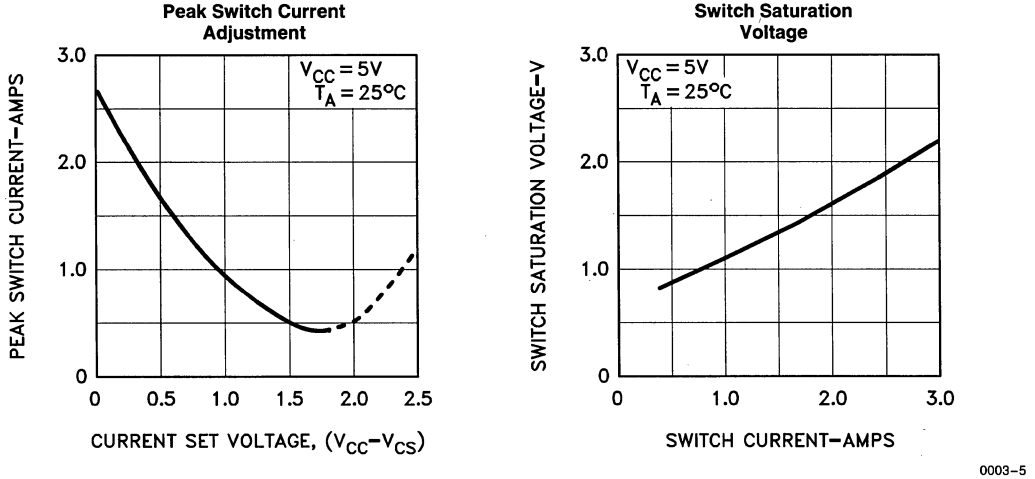
1. All threshold levels are developed from, and are therefore proportional to, V_{CC}.
2. Ground is common to all switches and the package heat sink. Switch overlap is allowable but only if the heat sink is electrically connected to a high-conduction ground. In other words, ground current above 3 amps should go through the heat sink rather than pin 8. In the DIL package, maximum peak ground current should be limited to 6 amps.
3. For efficient switching, input signals should have fast transitions (100 ns, or less).
4. The Current Set input is referenced to V_{CC} and is intended for operation with a Set voltage ranging from V_{CC} down to (V_{CC} − 1.5) volts at which point the switch current is clamped to its minimum value. Reducing V_{CS} below (V_{CC} − 1.5) volts will saturate the Current Set internal amplifier and cause the switch current clamp to increase back to its peak value.
5. The Fault Sense logic will indicate a fault by pulling low on its open-collector output. Multiple units can be wire-ORed together merely by connecting together to a common pull-up. The truth table logic is the following:

	V_C < 4V	V_C > 4V
V_{IN} > 2.7V	High (Good)	Low (Fault)
V_{IN} < 1.3V	Low (Fault)	High (Good)

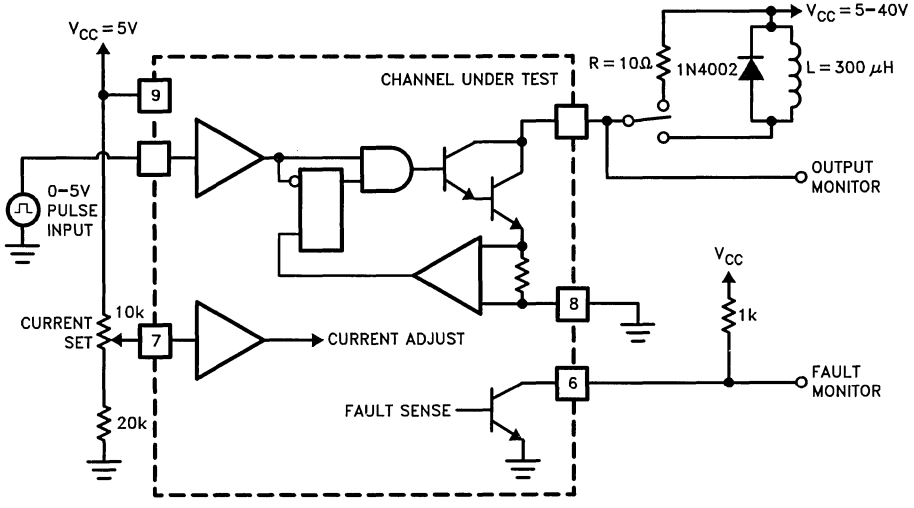
   The Fault Signal may need to be externally strobed since, due to switching delays, there will be a short fault condition with every signal transition. In addition, if the current sensing circuit latches the output off while the input remains high, this will show as a fault state.
6. The Thermal Sense output is also open-collector so it can be wire-ORed with other circuitry. The sense circuit has approximately 15° of hysteresis (switch on at approximately 160°C; off at approximately 145°C).

SIMPLIFIED INPUT CIRCUITRY (Each Channel)





TEST CIRCUIT

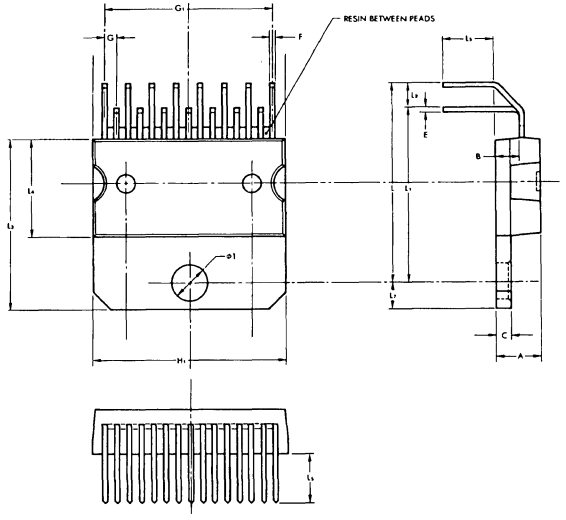


0003–2

5

MULTIWATT VH PACKAGE OUTLINE (Horizontal Lead Bend)

SYMBOL	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	.174	.177	.180	4.43	4.50	4.58
B	.096	.100	.104	2.45	2.55	2.65
C	.059	.060	.061	1.49	1.52	1.54
E	.019	.020	.021	0.50	0.52	0.54
F	.026	.028	.029	0.66	0.70	0.72
G	.046	.050	.054	1.17	1.27	1.37
G_1	.696	.700	.704	17.68	17.78	17.88
H_1	.783	.787	.791	19.90	20.00	20.10
L	.806	.810	.814	20.47	20.57	20.67
L_1	.706	.710	.714	17.93	18.03	18.13
L_2	.094	.100	.104	2.44	2.54	2.64
L_3	.685	.689	.693	17.40	17.50	17.60
L_4	.417	.421	.425	10.60	10.70	10.80
L_5	.206	.208	.210	5.23	5.28	5.33
L_7	.109	.110	.111	2.78	2.80	2.83
ϕ1	.149	.150	.151	3.78	3.80	3.82



0003–7

LINEAR INTEGRATED CIRCUITS

UC5170

Octal Line Driver

FEATURES

- Eight Single Ended Line Drivers in One Package
- Meets EIA Standards RS-232D and RS-423A and CCITT V.10/X.26
- Single External Resistor Controls Slew Rate
- Wide Supply Voltage Range
- Tri-State Outputs
- Output Short-Circuit Protection
- Low Power Consumption

DESCRIPTION

The UC5170 is a octal single ended line driver suited for use in digital data transmission systems where signal wave shaping is desired. The output slew rates are jointly controlled by a single external resistor connected between SRA (slew rate adjust) and ground. The slew rate and output levels (RS-423A mode) are independent of power supply variations.

RS-423A and RS-232C selection is easily accomplished by taking the mode select pins (M_S+ and M_S-) to ground (RS-423A) or to their respected supplies (RS-232C).

Inputs are compatible with TTL and MOS logic families and are diode-protected against negative transients.

ABSOLUTE MAXIMUM RATINGS (Note 1)

V^+ (Pin 20) 15V
V^- (Pin 11) ..... −15V
PLCC Power Dissipation, T_A = 25°C ..... 1000 mW
  Derate at 10 mW/°C for T_A above 50°C
  Thermal Resistance, Junction to Ambient ..... 100°C/W
DIP Power Dissipation, T_A = 25°C ..... 1250 mW
  Derate at 12.5 mW/°C for T_A above 50°C
  Thermal Resistance, Junction to Ambient ..... 80°C/W
Input Voltage ..... −1.5V to +7V
Output Voltage ..... −12V to +12V
Slew Rate Resistor ..... 2k to 10 kΩ
Storage Temperature ..... −65°C to +150°C

Note: 1. All voltages are with respect to ground, pin 18.

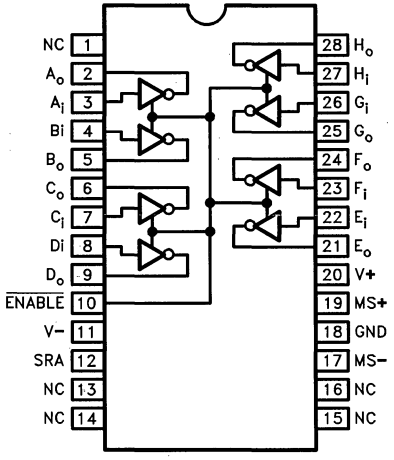
FUNCTIONAL TABLE

INPUTS		OUTPUTS	
$\overline{EN}$	DATA	RS-232C(2)	RS423A
0	0	$(V^+)-3V$	5V to 6V
0	1	$(V^-)-3V$	−5V to 6V
1	X	High Z	High Z

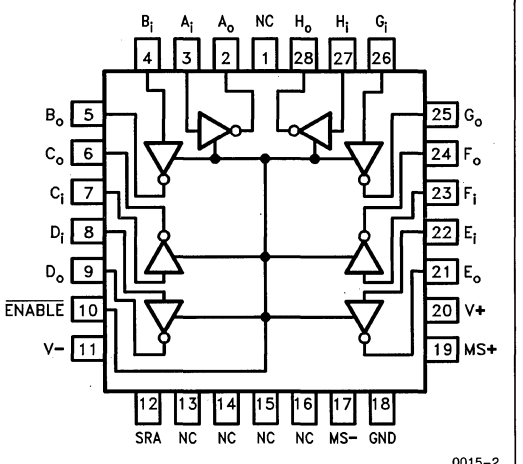
Note: 2. Minimum output swings.

CONNECTION DIAGRAMS

N PACKAGE (TOP VIEW)



Q PACKAGE (TOP VIEW)



UNITRODE

DC ELECTRICAL CHARACTERISTICS (Unless otherwise stated these specifications hold for $|V^+| = |V^-| = 10V$, $0 < T_A < +70°C$, $M_{S+} = M_{S-} = 0V$, $R_{SRA} = +10k$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS						
V^+ Range			9		15	V
V^- Range			−9		−15	V
V^+ Supply Current	I^+	R_L = Infinite $\overline{En}$ = 0V		25	37	mA
V^- Supply Current	I^-	R_L = Infinite $\overline{En}$ = 0V		−23	−35	mA
INPUTS						
High-Level Input Voltage	V_{IH}		2.0			V
Low-Level Input Voltage	V_{IL}				0.8	V
Input Clamp Voltage	V_{IK}	I_I = −15 mA		−1.1	−1.5	V
High Level Input Current	I_{IH}	V_{IH} = 2.4V		0.25	40	µA
Low Level Input Current	I_{IL}	V_{IL} = 0.4V	−200	−8.0		µA
OUTPUTS						
High Level Output Voltage (RS-423A)	V_{OH}	V_{IN} = 0.8V R_L = Inf., $\overline{En}$ = 0.8V R_L = 3k, R_L = 450	5.0 5.0 4.5	5.3 5.3 5.2	6.0 6.0 6.0	V V V
Low Level Output Voltage (RS-423A)	V_{OL}	V_{IN} = 2.0V R_L = Inf. $\overline{En}$ = 0.8V R_L = 3k R_L = 450	−5.0 −5.0 −4.5	−5.3 −5.6 −5.4	−6.0 −6.0 −6.0	V V V
Output Balance (RS-423A)	V_{BAL}	R_L = 450 $V_{OH} - V_{OL} = V_{BAL}$		0.2	0.4	V V
High Level Output Voltage (RS-232C)	V_{OH}	V_{IN} = 0.8V R_L = Inf. $\overline{En}$ = 0.8V R_L = 3k $M_{S+} = V^+, M_{S-} = V^-$	7.0 7.0	7.6 7.6	10 10	V V
Low Level Output Voltage (RS-232C)	V_{OL}	V_{IN} = 2.0V R_L = Inf. $\overline{En}$ = 0.8V R_L = 3k $M_{S+} = V^+, M_{S-} = V^-$	−7.0 −7.0	−7.7 −7.7	−10 −10	V V
Off-State Output Current	I_{OZ}	$\overline{En}$ = 2.0V, $V_O = \pm 6V$ $V^+ = 15V, V^- = -15V$	−100		100	µA
Power-Off Output Current	I_X	$V^+ = V^- = \overline{En} = 0V$ $V_O = \pm 6V$	−100		100	µA
Short-Circuit Current	I_{OS}	V_{IN} = 0V, $\overline{En}$ = 0V V_{IN} = 5V, $\overline{En}$ = 0V	25 25	50 40		mA mA

AC ELECTRICAL CHARACTERISTICS at $|V^+| = |V^-| = +10V$, $0 < T_A < +70°C$, $M_{S+} = M_{S-} = 0V$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Slew Rate	t_r t_f	R_{SRA} = 2k R_L = 450, C_L = 50 pF	8.25 8.25	9.5 10	13.25 13.25	V/µs V/µs
Output Slew Rate	t_r t_f	R_{SRA} = 10k R_L = 450, C_L = 50 pF	1.65 1.65	1.9 2.2	3.05 3.05	V/µs V/µs
Propagation Output to High Impedance	t_{Hz} t_{Lz}	R_{SRA} = 10k, R_L = 450, C_L = 50 pF		0.3 0.5	1.0 1.0	µs µs
Propagation High Impedance to Output	t_{zH} t_{zL}	R_{SRA} = 10k, R_L = 450, C_L = 50 pF		6.0 7.0	15 15	µs µs

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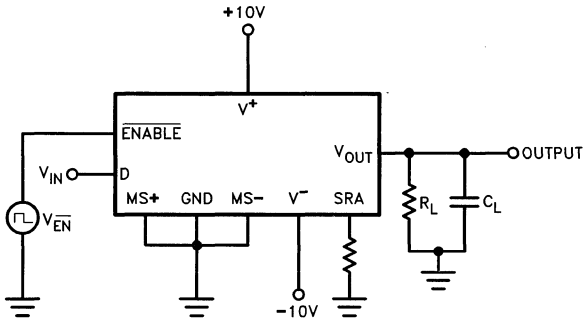
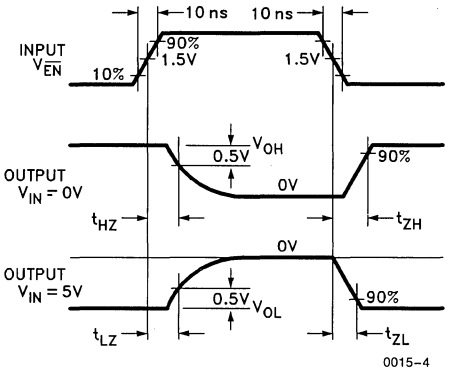
AC PARAMETER TEST CIRCUIT AND WAVEFORMS



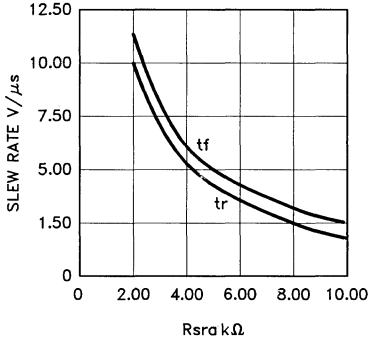
0015-3



0015-4

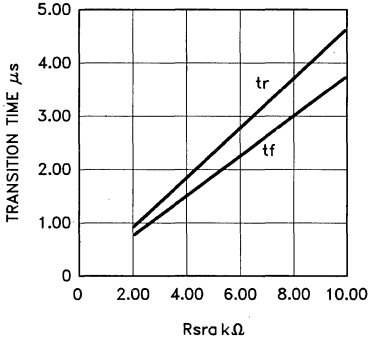
AC CHARACTERISTICS

Driver Slew Rate



0015-5

Driver t_r & t_f (10–90%) RS-423A Mode



0015-6

APPLICATIONS INFORMATION

Slew Rate Programming

Slew rate for the UC5170 is set up by a single external resistor connected between the SRA pin and ground. Slew rate adjustments can be approximated by using the following formula:

$$V/\mu s = \frac{20}{R_{SRA}} (R_{SRA} \text{ in } k\Omega)$$

The slew rate resistor can vary between 2k and 10 kΩ which allows slew rates between 10 to 22 V/µs, respectively. The relationship between slew rate and R_{SRA} is shown in the typical characteristics.

Waveshaping of the output lets the user control the level of interference (near-end crosstalk) that may be coupled to adjacent circuits in an interconnection. The recommended output characteristics for cable length and data rates can be found in EIA standard RS-423A. Approximations of these standards are given by the following equations:

Max. Data Rate = 300/t (For data rates 1k to 100k bit/s)

Max. Cable Length (feet) = 100 × t (Max. length 4000 feet)

where t is the transition time from 10% to 90% of the output swing in microseconds. For data rates below 1k bit/s t may be up to 300 microseconds.

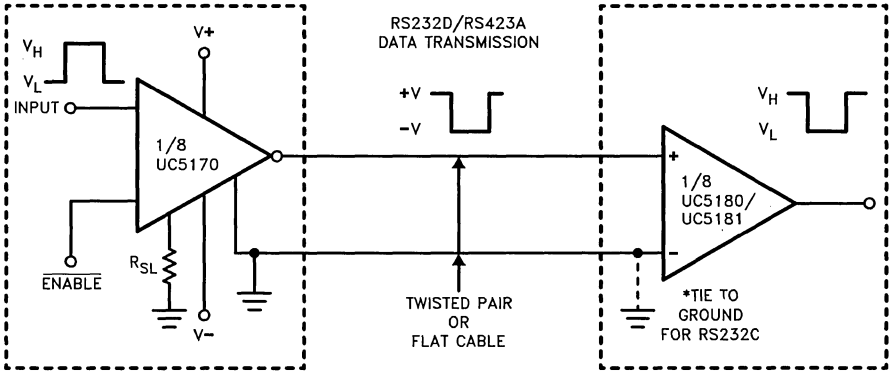
Output Voltage Programming

The UC5170 has two programmable output modes, either a low voltage mode which meets RS-423A specifications, or the high output mode which meets the RS-232C specifications.

The high output mode provides greater output swings, minimum of 3V below the supply rails, for driving higher, attenuated lines. This mode is selected by connecting the mode select pins to their respected supples, M_{S+} to V^+ and M_{S-} to V^-.

The low output mode provides a controlled output swing and is accomplished by connecting both mode select pins to ground.

APPLICATIONS



0015-7

5

LINEAR INTEGRATED CIRCUITS

UC5180/5181

Octal Line Receiver

FEATURES

- Meets EIA 232D/423A/422A and CCITT V.10, V.11, V.28
- Single +5V Supply—TTL Compatible Outputs
- Differential Inputs withstand ±25V
- Low Open Circuit Voltage for Improved Failsafe Characteristic
- Reduced Supply Current—35 mA Max
- Input Noise Filter (UC5180 only)
- Internal Hystersis

DESCRIPTION

The UC5180 and UC5181 are octal line receivers designed to meet a wide range of digital communications requirements as outlined in EIA standards 232D, RS422A, and CCITT V.10, V.11, V.28, X.26, and X.27. The UC5180 includes an input noise filter and is intended for applications employing data rates up to 200 Kb/s. The UC5181, without input filtering, covers the entire range of data rates up to 10 Mb/s. A failsafe function allows these devices to "fail" to a known state under a wide variety of fault conditions at the inputs.

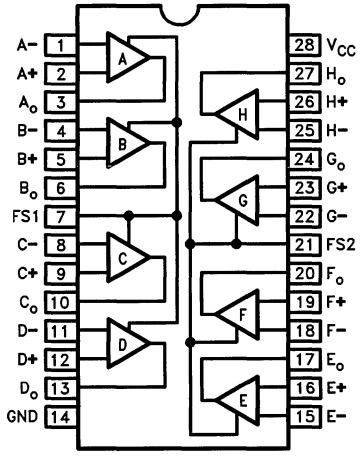
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, V_{CC} 7V
Output Sink Current ..... 50 mA
Output Short Circuit Time ..... 1 Sec
Common Mode Input Range 15V
Differential Input Range 25V
Failsafe Voltage ..... −0.3 to V_{CC}
PLCC Power Dissipation, T_A = 25°C ..... 1000 mW
  Derate at 10 mW/°C for T_A above 50°C
  Thermal Resistance, Junction to Ambient ..... 100°C/W
DIP Power Dissipation, T_A = 25°C ..... 1200 mW
  Derate at 12.5 mW/°C for T_A above 50°C
  Thermal Resistance, Junction to Ambient ..... 80°C/W
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

Note: 1. All voltages are with respect to ground, pin 8. Currents are positive into, negative out of the specified terminal.

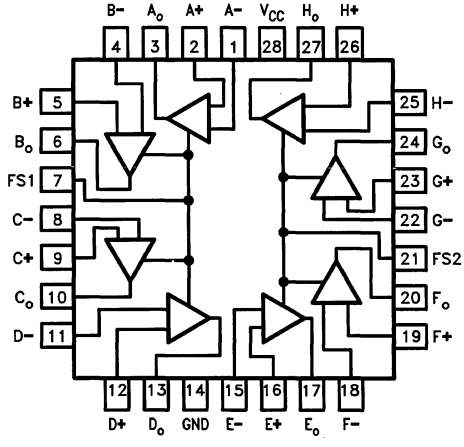
CONNECTION DIAGRAMS

28 PIN DIL



0014-1

28 PIN PLCC



0014-2

UNITRODE

DC ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C; V_{CC} = 5V ±5%, Input Common Mode Range ±7V)

PARAMETER	SYMBOL	TEST CONDITIONS		UC5180		UC5181		UNITS
				MIN	MAX	MIN	MAX	
DC Input Resistance	R_{IN}	3V ≤ $\|V_{IN}\|$ ≤ 25V		3K	7K	3K	7K	Ω
Failsafe Output Voltage	V_{OFS}	Inputs Open or Shorted Together, or One Input Open and One Grounded	0V ≤ I_{OUT} ≤ 8 mA, $V_{FAILSAFE}$ = 0V		0.45		0.45	V
			0 ≥ I_{OUT} ≥ −400 μA, $V_{FAILSAFE}$ = V_{CC}	2.7		2.7		
Differential Input High Threshold	V_{th}	V_{OUT} = 2.7V, I_{OUT} = −440 μA (See Figure 1)	R_S = 0 (Note 2)		0.2		0.2	V
			R_S = 500 (Note 2)		0.4		0.4	
Differential Input Low Threshold	V_{tl}	V_{OUT} = 0.45V, I_{OUT} = 8 mA (See Figure 1)	R_S = 0 (Note 2)	−0.2		−0.2		V
			R_S = 500 (Note 2)	−0.4		−0.4		
Hysteresis	V_H	F_S = 0V or V_{CC} (See Figure 1)		60	140	60	140	mV
Open Circuit Input Voltage	V_{IOC}				100		100	mV
Input Capacitance	C_I				100		100	pF
High Level Output Voltage	V_{OH}	V_{ID} = 1V, I_{OUT} = −440 μA		2.7		2.7		V
Low Level Output Voltage	V_{OL}	V_{ID} = −1V (Note 3)	I_{OUT} = 4 mA		0.4		0.4	V
			I_{OUT} = 8 mA		0.45		0.45	
Short Circuit Output Current	I_{OS}	Note 4		20	100	20	100	mA
Supply Current	I_{CC}	4.75V ≤ V_{CC} ≤ 5.25V			35		35	mA
Input Current	I_{IN}	Other Inputs Grounded	V_{IN} = +10V		3.25		3.25	mA
			V_{IH} = −10V	−3.25		−3.25		

Notes: **2.** R_S is a resistor in series with each input.
3. Measured after 100 ms warm up (at 0°C).
4. Only 1 output may be shorted at a time and then only for a maximum of 1 sec.

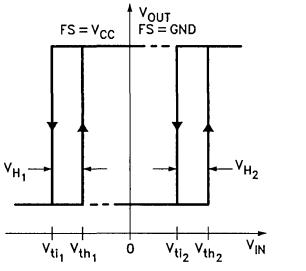
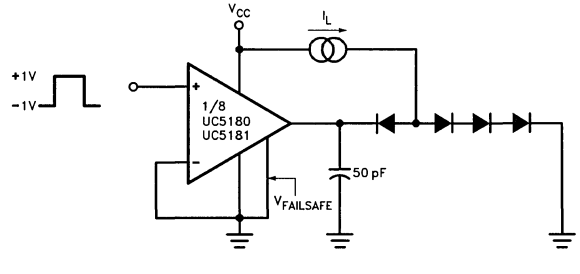


Figure 1. V_{tl}, V_{th}, V_H Definition

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±5%, T_A = 0°C to +70°C, Figure 2)

PARAMETER	SYMBOL	TEST CONDITIONS	UC5180		UC5181		UNITS
			MIN	MAX	MIN	MAX	
Propagation Delay — Low to High	t_{PLH}	C_L = 50 pF, V_{IN} = ±1V		300		70	ns
Propagation Delay — High to Low	t_{PHL}	C_L = 50 pF, V_{IN} = ±1V		300		70	ns
Acceptable Input Frequency	f_a	Unused Input Grounded, V_{IN} = ±200 mV		0.1		5.0	MHz
Rejectable Input Frequency	f_r	Unused Input Grounded, V_{IN} = ±500 mV	5.5		NA		MHz



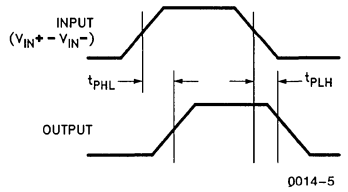


Figure 2. AC Test Circuit

APPLICATIONS INFORMATION

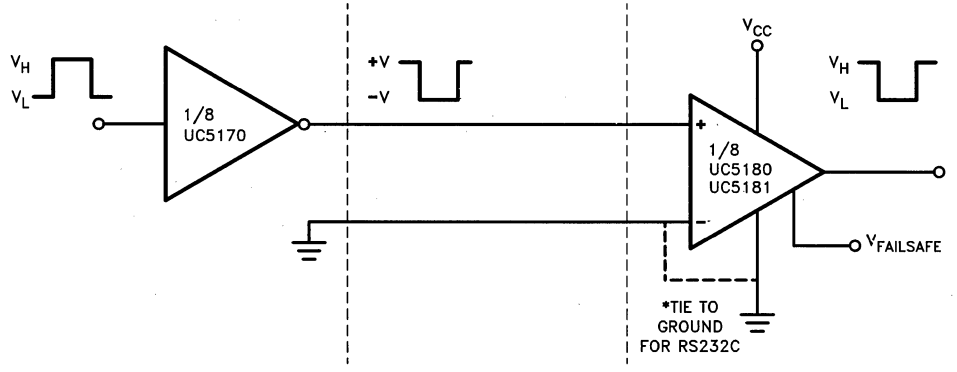
Failsafe Operation

These devices provide a failsafe operating mode to guard against input fault conditions as defined in RS422A and RS423A standards. These fault conditions are (1) driver in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to V_{CC} or ground. A connection to V_{CC} provides a logic "1" output under fault conditions, while a connection to ground provides a logic "0". There are two failsafe pins (F_{S1} and F_{S2}) on the UC5180 or UC5181 where each provides common failsafe control for four receivers.

Input Filtering (UC5180)

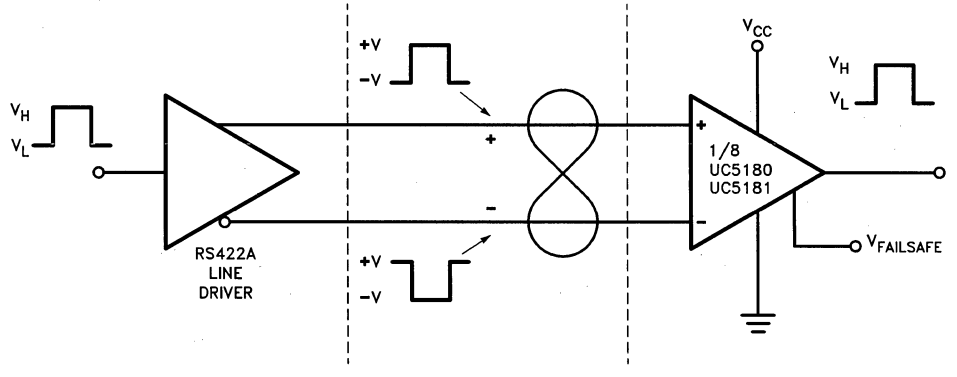
The UC5180 has input filtering for additional noise rejection. This filtering is a function of both signal level and frequency. For the specified input (5.5 MHz at ±500 mV) the input stage filter attenuates the signal such that the output stage threshold levels are not exceeded and no change of state occurs at the output.

RS232C/RS423C DATA TRANSMISSION



0014-6

RS422A DATA TRANSMISSION



0014-7

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TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UCOP01	High Speed - High Slew Rate Op Amp	• Low Power • Fast Settling Time • Internally Compensated • Pin Compatible with 741, OP01	8 Pin DIL
UCOP02	High Performance General Purpose Op Amp	• Low Power • Low Offset Voltage Drift • Internally Compensated • Pin Compatible with 741	8 Pin DIL
UC161	Quad Comparator with Programmable AC & DC Parameters	• Wide Input Common Mode Range • Low Power • Directly Compatible with CMOS Logic • Output Drive Level Programmability • Outputs Can Be Wire Or'd	16 Pin DIL
UC542	High Slew Rate Operational Amplifier	• High Slew Rate 150V/μs tvd • Fast Settling Time: 1% in 75ns • Open Loop Gain: 70dB min. • Low Offset Voltage Drift 10μV/°C max. • Wide Bandwidth: DC to 100MHz at 10dB Gain	8 Pin DIL
UC1704/3704	Bridge Transducer Switch for Monitoring Systems	See Power Driver & Interface Circuits.	

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LINEAR INTEGRATED CIRCUITS

Inverting High Speed Operational Amplifier

UCOP01
UCOP01C
UCOP01G
UCOP01H

FEATURES

- Fast Settling Time—1μsec to 0.1%
- High Slew Rate—18V/μsec Typ
- Power Bandwidth—250 kHz Typ
- Low Power Consumption—90 mW Max
- Internally Compensated
- Pin Compatible with 741, OP-01

DESCRIPTION

The UCOP-01 high speed operational amplifier features high slew rate and fast settling time. High speed capabilities are combined with excellent DC specifications, without compromising input bias current or power consumption. The feedforward frequency compensation network assures stable, high speed performance without external capacitors. The selection of the resistance seen by the inverting input lets you tailor the bandwidth to your application while assuring proper stability.

The fast output response combined with excellent settling time makes the UCOP-01 an excellent choice for a D/A converter output amplifier, or any precision application requiring enhanced speed performance.

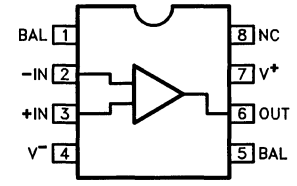
ABSOLUTE MAXIMUM RATING (Note 1)

V+ (Pin 7) ..... +22V
V− (Pin 4) ..... −22V
Power Dissipation ..... 500 mW
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range
UCOP-01, UCOP-01G ..... −55°C to +125°C
UCOP-01H, UCOP-01C ..... 0°C to +70°C

Note: 1. All voltages are with respect to ground.

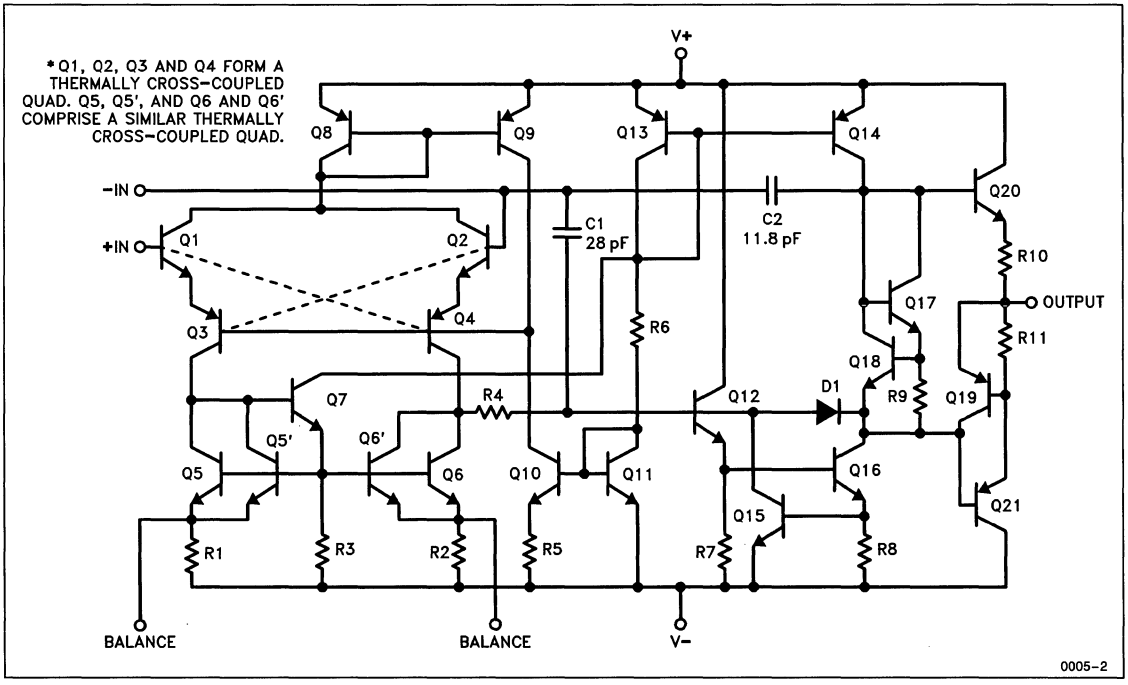
CONNECTION DIAGRAM

DIL-8 (TOP VIEW)
N or J PACKAGE



0005-1

SIMPLIFIED SCHEMATIC



0005-2

UNITRODE

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A + 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	UCOP-01 UCOP-01H			UCOP-01G UCOP-01C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20\ k\Omega$	—	0.3	0.7	—	2.0	5.0	mV
Input Offset Current	I_{OS}		—	0.5	2.0	—	2.0	20	nA
Input Bias Current	I_B		—	18	30	—	25	100	nA
Input Voltage Range	IVR		±12	±13	—	±12	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20\ k\Omega$	85	110	—	80	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20\ k\Omega$	—	10	60	—	100	150	μV/V
Output Voltage Swing	V_O	$R_L \geq 5\ k\Omega$ $R_L \geq 2\ k\Omega$	±12.5 ±12.0	±13.5 ±13.0	— —	±12.5 ±12.0	±13.5 ±13.0	— —	V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2\ k\Omega$ $V_O = \pm 10V$	50	100	—	25	75	—	V/mV
Power Consumption	P_d	$V_{OUT} = 0$	—	50	90	—	50	90	mW
Setting Time to 0.1% (Summing Node Error)	t_S	$A_V = -1$ (Notes 1, 2) $V_{IN} = 5V$	—	0.7	1.0	—	0.7	1.0	μs
Slew Rate (Notes 2, 3, 4)	SR	$A_V = -1$, $R_S = 3k$ to $5\ k\Omega$	12	18	—	12	18	—	V/μs
Large-Signal Bandwidth (Notes 3, 4)			150	250	—	150	250	—	kHz
Small-Signal Bandwidth (Notes 3, 4)			1.5	2.5	—	1.5	2.5	—	MHz
Risetime	t_r	$A_V = -1$ $V_{IN} = 50\ mV$	—	150	—	—	150	—	ns
Overshot	O_S		—	2	—	—	2	—	%

Notes: 1. $R_L = 2.5\ k\Omega$; $C_L = 50\ pF$. See Settling Time Test Circuit.
2. Sample tested.
3. See applications information.
4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C < T_A < +125°C$ for UCOP-01, UCOP-01G and $0°C < T_A + 70°C$ for UCOP-01H, UCOP-02C unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	UCOP-01 UCOP-01H			UCOP-01G UCOP-01C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20\ k\Omega$	—	0.4	1.0	—	3.0	6.0	mV
Input Offset Current	I_{OS}		—	1	4	—	4	40	nA
Input Bias Current	I_B		—	30	50	—	50	200	nA
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20\ k\Omega$	85	110	—	80	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20\ k\Omega$	—	10	60	—	100	150	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2\ k\Omega$ $V_O = \pm 10V$	30	60	—	15	50	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 5\ k\Omega$ $R_L \geq 2\ k\Omega$	±12.5 ±12.0	±13.5 ±13.0	— —	±12.5 ±12.0	±13.5 ±13.0	— —	V
Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S \leq 5\ k\Omega$	—	2	8	—	5	20	μV/°C

NOTES: 1. Sample tested.

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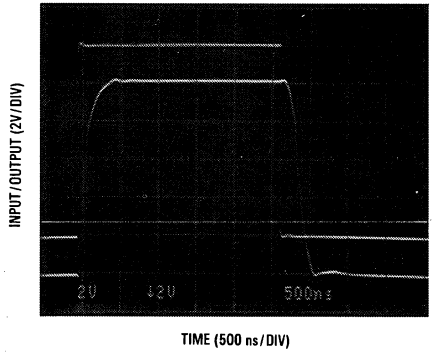
OPERATION AND APPLICATION INFORMATION

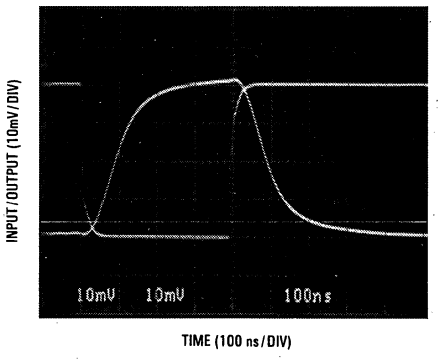
Large-Signal Pulse Response



0005-3

$V_S = \pm 15V$, $A_V = -1$, $R_S = 3.3\ k\Omega$
$V_{IN} = \pm 5V$, $R_L = 2\ k\Omega$, $C_L = 50\ pF$

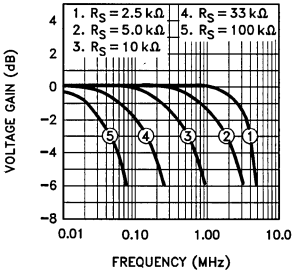
Small-Signal Pulse Response



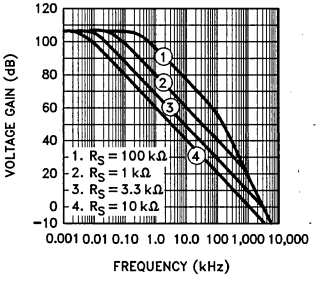
0005-4

$V_S = \pm 15V$, $A_V = -1$, $R_S = 3.3\ k\Omega$
$V_{IN} = \pm 40\ mV$, $R_L = 2\ k\Omega$, $C_L = 50\ pF$

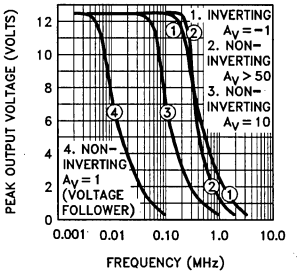
Unity-Gain Bandwidth vs Source Resistance



Open-Loop Gain vs Frequency



Large-Signal Output Swing vs Frequency

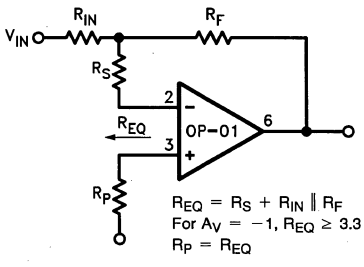


0005-5

Compensation

The UCOP-01 uses a feedforward compensation network to provide fast slewing and settling times in all inverting and moderate to high gain noninverting applications. Unity gain bandwidth is a function of the total equivalent source resistance seen by the inverting input terminal. Proper choice of this resistance will allow the user to maximize bandwidth while assuring proper stability. The equivalent inverting terminal resistance is defined as $R_{IN}||R_F$, and it must be greater than 3.3 kΩ to assure stability in all closed loop configurations including unity gain. Should this resistance become less than 3.3 kΩ, a resistor (R_S) can be placed between the inverting terminal and the summing node to provide the required resistance. (See Figure Fast Inverting Amp Diagram.) Lower values of $R_{IN}||R_F$ may be used to improve bandwidth in higher closed loop gain configurations, as shown by the open loop gain vs frequency plot.

Fast Inverting Amplifier

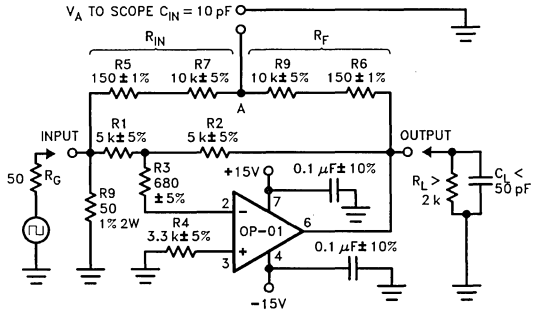


0005-6

OPERATION AND APPLICATION INFORMATION (Continued)

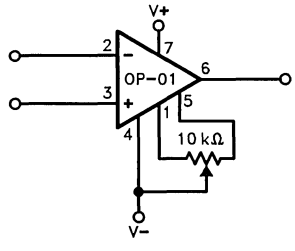
Settling Time Test Circuit

The settling time measurements have been made using the test figure shown, this circuit incorporates the "false summing node" technique to produce accurate and repeatable results. For a 5V input step, 0.1% settlings will be achieved when the false summing node settles to 2.5 mV of its final value. The scope being used should have wide bandwidth and fast overload recovery time. The capacitance at the false summing node should be minimized and R_{IN} has to equal R_F within 0.01% to be able to measure settling times within 0.1%.

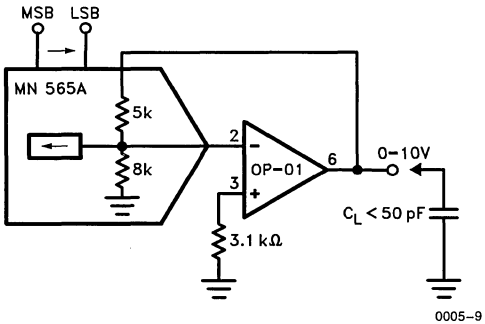


TYPICAL APPLICATIONS

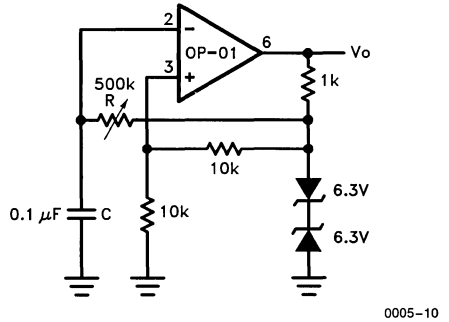
Offset Nulling Circuit



Fast Voltage-Output D/A Converter



10 Hz to 10 kHz Square Wave Generator



LINEAR INTEGRATED CIRCUITS

General Purpose Operational Amplifier

UCOP02 UCOP02A
UCOP02B UCOP02C
UCOP02D UCOP02E

FEATURES

- Excellent DC Specification
- Low Offset Voltage Drift—8 μV/°C Max
- Low Power Consumption—90 mW Max
- Internally Compensated
- Pin Compatible with 741

DESCRIPTION

The UCOP-02 high performance general purpose operational amplifier provides significant improvements over industry standard 741 types while maintaining ease of application and low cost. The UCOP-02 offers superior specifications in key areas, such as V_{OS}, I_{OS}, I_B, CMRR, PSRR, and A_{VO} which are all specified over the full operating temperature range.

The UCOP-02 is a direct replacement for the 741. It is ideal for upgrading existing designs.

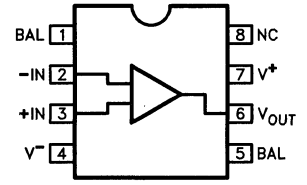
ABSOLUTE MAXIMUM RATING (Note 1)

V^+ (Pin 7) ..... +22V
V^- (Pin 4) ..... −22V
Power Dissipation ..... 500 mW
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range
UCOP-02, UCOP-02A, UCOP-02B ..... −55°C to +125°C
UCOP-02C, UCOP-02D, UCOP-02E ..... 0°C to +70°C

Note: 1. All voltages are with respect to ground.

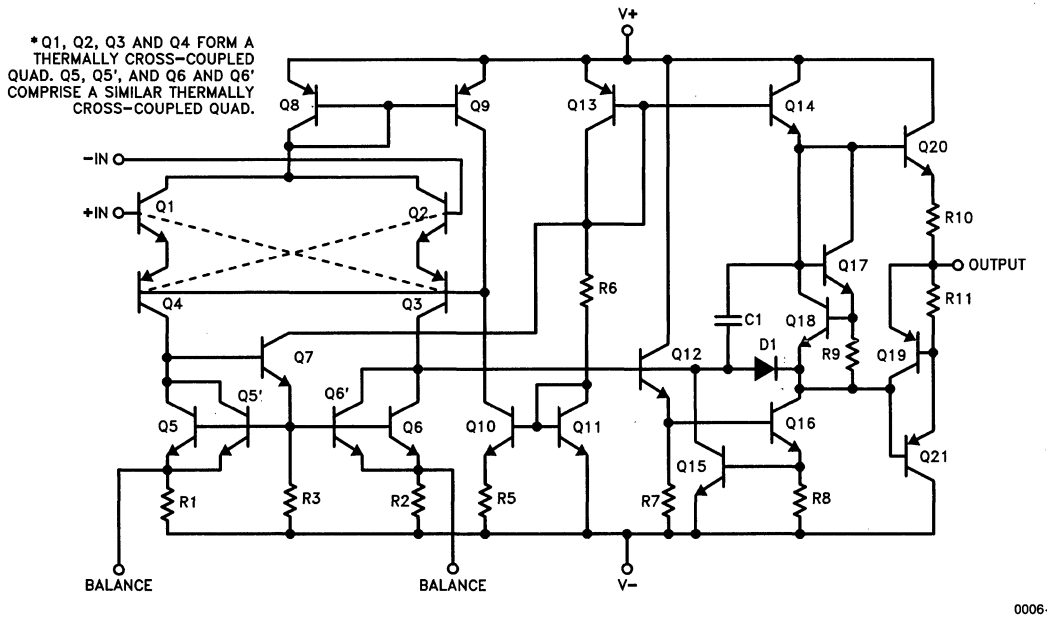
CONNECTION DIAGRAM

DIL-8 (TOP VIEW)
N or J PACKAGE



0006-1

SIMPLIFIED SCHEMATIC



0006-3

UNITRODE

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A + 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	UCOP-02A UCOP-02E			UCOP-02 UCOP-02C			UCOP-02B UCOP-02D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20\ k\Omega$	—	0.3	0.5	—	1	2	—	3	5	mV
Input Offset Current	I_{OS}		—	0.5	2	—	1	5	—	5	25	nA
Input Bias Current	I_B		—	18	30	—	20	50	—	30	100	nA
Input Resistance-Differentail-Mode	R_{IN}	(Note 2)	3.8	7.5	—	2.3	7	—	1	5	—	MΩ
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20\ k\Omega$	85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20\ k\Omega$	—	10	60	—	30	100	—	100	150	μV/V
Output Voltage Swing	V_O	$R_L \geq 2\ k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2\ k\Omega$ $V_O = \pm 10V$	100	250	—	50	200	—	25	150	—	V/mV
Power Consumption	P_d	$V_O = 0V$	—	40	70	—	50	90	—	50	90	mW
Input Noise Voltage	e_{np-p}	0.1 Hz to 10 Hz	—	0.65	—	—	0.65	—	—	0.65	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10$ Hz $f_O = 100$ Hz $f_O = 1000$ Hz	— — —	25 22 21	— — —	— — —	25 22 21	— — —	— — —	25 22 21	— — —	$nV/\sqrt{Hz}$
Input Noise Current	i_{np-p}	0.1 Hz to 10 Hz	—	12.8	—	—	12.8	—	—	12.8	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10$ Hz $f_O = 100$ Hz $f_O = 1000$ Hz	— — —	1.4 0.7 0.4	— — —	— — —	1.4 0.7 0.4	— — —	— — —	1.4 0.7 0.4	— — —	$pA/\sqrt{Hz}$
Slew Rate	SR	(Note 1)	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/μs
Large-Signal Bandwidth		$V_O = 20\ V_{p-p}$ (Note 1)	4	8	—	4	8	—	4	8	—	kHz
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 1)	0.8	1.3	—	0.8	1.3	—	0.8	1.3	—	MHz
Risetime	t_r	$A_{VCL} = +1$ $V_{IN} = 50$ mV	—	200	—	—	200	—	—	200	—	ns
Overshoot	O_S		—	5	—	—	5	—	—	5	—	%

Note: 1. Guaranteed by design.
2. Guaranteed by input bias current.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C < T_A < +125°C$ for UCOP-02A, UCOP-02, UCOP-02B and $0°C < T_A < +70°C$ for UCOP-02C, UCOP-02D, UCOP-02D unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	UCOP-02A UCOP-02E			UCOP-02 UCOP-02C			UCOP-02B UCOP-02D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20\ k\Omega$	—	0.4	1	—	1.2	3	—	3	6	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$	—	2	8	—	4	10	—	8	20	μV/°C
Input Offset Current	I_{OS}		—	0.7	4	—	1.4	10	—	5	50	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		—	7.5	120	—	15	250	—	70	500	pA/°C
Input Bias Current	I_B		—	22	50	—	25	100	—	50	200	nA
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20\ k\Omega$	80	100	—	80	90	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20\ k\Omega$	—	10	60	—	30	100	—	100	150	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2\ k\Omega$ $V_O = \pm 10V$	50	100	—	25	60	—	15	25	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2\ k\Omega$	±12	±13	—	±12	±13	—	±10	±13	—	V

Note: 1. Sample tested.
2. Guaranteed by design.

UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
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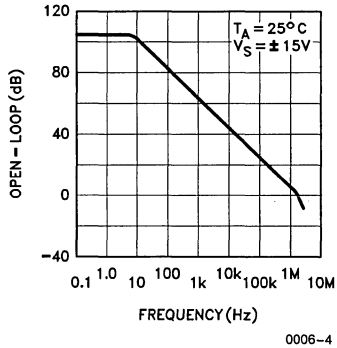
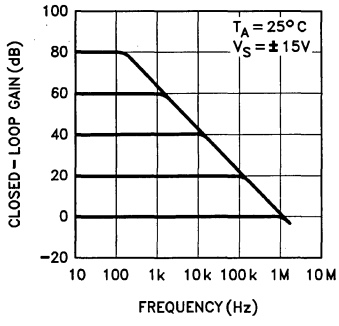
OPERATING AND APPLICATION INFORMATION

Open-Loop Frequency Response



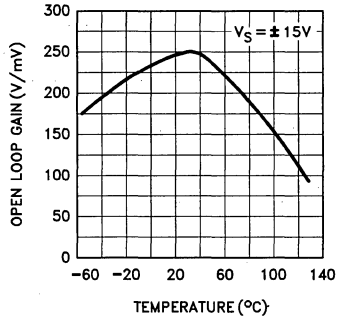
0006-4

Closed-Loop Response for Various Gain Configurations



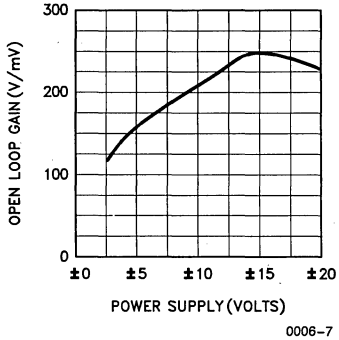
0006-5

Open-Loop Gain vs Temperature



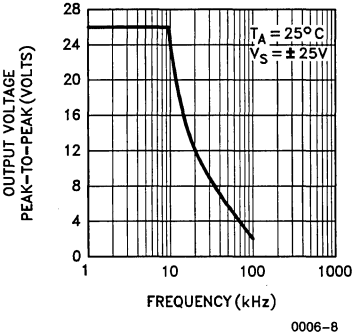
0006-6

Open-Loop Gain vs Power Supply Voltage



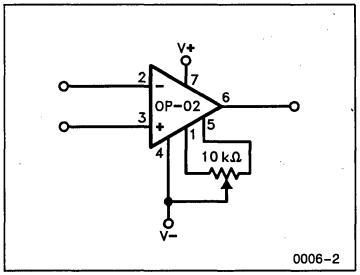
0006-7

Maximum Undistorted Output vs Frequency



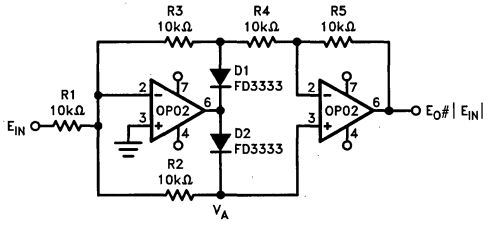
0006-8

OFFSET NULLING CIRCUIT



0006-2

ABSOLUTE VALUE CIRCUIT



0006-9

Design Equations

Positive Input

1. $V_A = 0$, D2 OFF, D1 ON
2. $E_O = \left(\frac{-E_{IN}R3}{R1}\right) \times \left(\frac{-R5}{R4}\right)$
   $= E_{IN}\frac{R3\ R5}{R1\ R4}$
3. With R1 = R3 = R4 = R5:
   $E_O = E_{IN}$
4. V_{OS} error included:
   $E_O = E_{IN} + 2V_{OS}$

Negative Input

1. D1 OFF, D2 ON
2. $\frac{-E_{IN}}{R1} = \frac{V_A}{R2} + \frac{V_A}{R3 + R4}$
3. $E_O = V_A\left(1 + \frac{R5}{R3 + R4}\right)$
4. With R3 = R4 = R5:
   $E_O = 1.5V_A$
5. $E_O = -\frac{(R2)\ (R3 + R4)\ (1.5)\ E_{IN}}{R1\ (R2 + R3 + R4)}$
6. With R1 = R2 = R3 = R4:
   $E_O = -E_{IN}$
7. V_{OS} error included:
   $E_O = -E_{IN} + 1.5V_{OS2} - 0.5V_{OS1}$
8. For both inputs: $E_O = +[E_{IN}]$

LINEAR INTEGRATED CIRCUITS

Micropower Quad Comparator

UC161A
UC161B
UC161C

FEATURES

- Programmable Output Drive Capability
- Direct CMOS Logic Compatibility
- Low Power
- Direct Wire-OR of Outputs
- Wide Input Common Mode Range

DESCRIPTION

The UC161 family of quad comparators feature programmable DC and AC parameters. A single external resistor can set the comparators to operate in the microwatt region for battery applications, or higher current levels can be set to obtain improved speed or drive capabilities. The outputs on these devices can be wire OR'd together, simplifying external logic requirements in some applications.

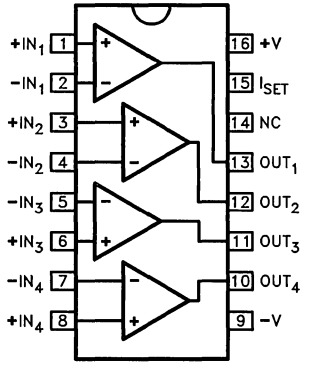
These devices are available in three temperature ranges, the UC161A is specified for the full military range, −55°C to +125°C, the UC161B for the industrial range, −25°C to +85°C, and the UC161C for the commercial range of 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (+V to −V) 36V
Differential Input Voltage ..... ±30V
Input Voltage ..... −V−0.3V to +V
Power Dissipation at T_A = 25°C ..... 1000 mW
  Derate at 10 mW/°C above 25°C
Power Dissipation at T_C = 25°C ..... 2000 mW
  Derate at 16 mW/°C above 25°C
Operating Junction Temperature ..... −55°C to +150°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 Sec.) ..... +300°C

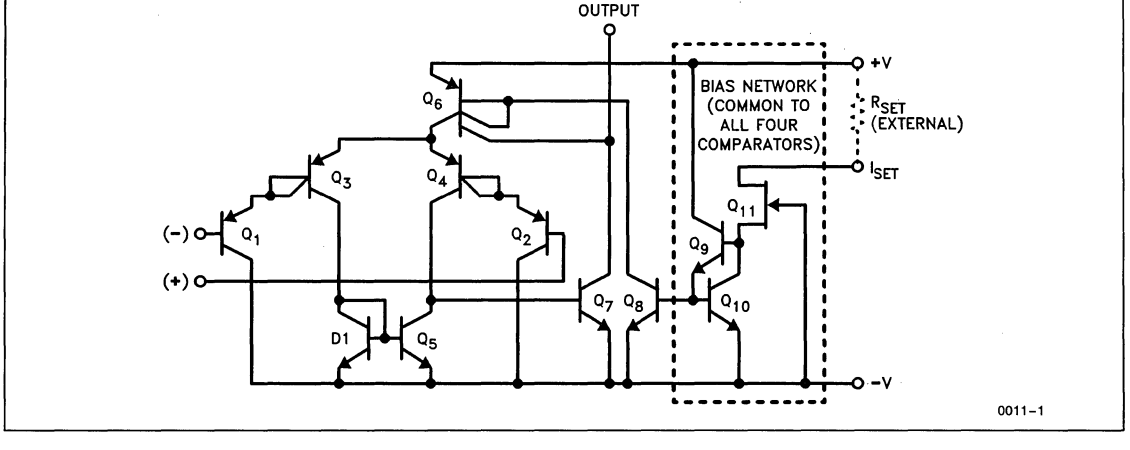
CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
N OR J PACKAGE



0011-2

SIMPLIFIED SCHEMATIC (ONE COMPARATOR)



0011-1

UNITRODE

ELECTRICAL CHARACTERISTICS Temperature range is −55° to +125°C for the UC161A, −25°C to +85°C for the UC161B, and 0°C to +70°C for the UC161C

LOW POWER ELECTRICAL CHARACTERISTICS (Unless Otherwise Stated: $V_S = \pm 3V$, I_{SET}[2] = 10 μA, R_2 = 10 MΩ, C_L = 10 pF, T_A = 25°C)

	PARAMETER	SYMBOL	TEST CONDITIONS	UC161A			UC161B/C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
INPUT	Input Offset Voltage	V_{OS}			1	3		1	6	mV
INPUT	Input Offset Current	I_{OS}			1	20		1	25	nA
INPUT	Input Bias Current	I_{BT}			20	100		20	200	nA
OUTPUT	DC Open Loop Voltage Gain	A_{VOL}		20	30		10	30		V/mV
OUTPUT	Low Output Voltage[1]	V_{OL}	R_L = 20 kΩ		−2.95	−2.6		−2.95	−2.6	V
OUTPUT	High Output Voltage[1]	V_{OH}	R_L = 200 kΩ	2.5	2.9		2.5	2.9		V
DYNAMIC	Common Mode Range	CMR			+1.3/−3			+1.3/−3		V
DYNAMIC	Response Time	t	100 mV Overdrive, C_L = 10 pF		5			5		μs
DYNAMIC	Common Mode Rejection Ratio	CMRR	V_{IN} = CMR	75	90		75	90		dB
SUPPLY	Power Supply Rejection Ratio	PSRR		65	80		65	80		dB
SUPPLY	Supply Current	I_S	All Inputs Grounded, R_L = ∞		210	300		210	300	μA
	T_A = Over Temperature Range									
	Input Offset Voltage	V_{OS}				5				mV
	DC Open Loop Voltage Gain	A_{VOL}		10			5			V/mV
	Supply Current	I_S	All Inputs Grounded, R_L = ∞			350			350	μA

HIGH POWER ELECTRICAL CHARACTERISTICS (Unless Otherwise Stated: $V_S = \pm 15V$, I_{SET}[2] = 100 μA, R_L = 2 MΩ, C_L = 10 pF, T_A = 25°C)

	PARAMETER	SYMBOL	TEST CONDITIONS	UC161A			UC161B/C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
INPUT	Input Offset Voltage	V_{OS}			1.5	3		1.5	6	mV
INPUT	Input Offset Current	I_{OS}			5	60		5	90	nA
INPUT	Input Bias Current	I_{BT}			100	400		100	800	nA
OUTPUT	DC Open Loop Voltage Gain	A_{VOL}		50	100		30	100		V/mV
OUTPUT	Low Output Voltage[1]	V_{OL}	R_L = 20 kΩ		−14.9	−14.6		−14.9	−14.6	V
OUTPUT	High Output Voltage[1]	V_{OH}	R_L = 200 kΩ	14.5	14.9		14.5	14.9		V
DYNAMIC	Common Mode Range	CMR			+13/−15			+13/−15		V
DYNAMIC	Response Time	t	100 mV Overdrive, C_L = 10 pF		1			1		μs
DYNAMIC	Common Mode Rejection Ratio	CMRR	V_{IN} = CMR	75	90		75	90		dB
SUPPLY	Power Supply Rejection Ratio	PSRR		65	80		65	80		dB
SUPPLY	Supply Current	I_S	All Inputs Grounded, R_L = ∞		2100	3500		2100	3500	μA

Notes: 1. The output current drive of the UC161 is non-symmetrical. This facilitates the wire-ORing of two comparator outputs. The output pull-down current capability is typically 75–150 times the pull-up current.

2. Set current (I_{SET}) and supply current (I_{SUPPLY}) can be determined by the following formulas:

$$I_{SET} = \frac{[(+V) - (2V_{BE}) - (-V)]}{R_{SET}}; \quad I_{SUPPLY} = 21 \times I_{SET}.$$

HIGH POWER ELECTRICAL CHARACTERISTICS (Continued) T_A = **Over Temperature Range**

	PARAMETER	SYMBOL	TEST CONDITIONS	UC161A			UC161B/C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
	Input Offset Voltage	V_{OS}				6				mV
	Input Bias Current	I_{BT}				500				nA
	DC Open Loop Voltage Gain	A_{VOL}		25			15			V/mV
	Supply Current	I_S	All Inputs Grounded, $R_L = \infty$			4000			4000	μA

Notes: 1. The output current drive of the UC161 is non-symmetrical. This facilitates the wire-ORing of two comparator outputs. The output pull-down current capability is typically 75–150 times the pull-up current.

2. Set current (I_{SET}) and supply current (I_{SUPPLY}) can be determined by the following formulas:

$$I_{SET} = \frac{[(+V) - (2V_{BE}) - (-V)]}{R_{SET}}; \quad I_{SUPPLY} = 21 \times I_{SET}.$$

APPLICATION AND OPERATION INFORMATION

DESCRIPTION

The UC161 is a monolithic quad micropower comparator with an external control for varying its AC and DC characteristics. The variation of a single programming resistor will simultaneously alter parameters such as supply current, input bias current, slew rate, output drive capability, and gain. By making this resistor large, operation at very small supply current levels and power dissipations is possible. The UC161 is therefore ideal for systems requiring minimum power drain, such as battery-powered instrumentation, aerospace systems, CMOS designs, and remote security systems.

The circuit (see Simplified Schematic) is composed of five major blocks—four comparators and a common bias network. Q_1–Q_6 and D_1 form a darlington differential amplifier with double-to-single ended conversion. Q_6 is a dual current source whose outputs are exactly twice the current flowing through Q_8. The collector current of Q_8 is a function of the current supplied externally to Q_9–Q_{10}, which in turn is known as the set current or I_{SET}. This set current is established by a resistor connected between the I_{SET} terminal and a voltage source, most commonly the positive supply. Q_{11} prevents excessive current from flowing through Q_9 and Q_{10} in the event the I_{SET} terminal is shorted to the positive supply; it has no effect on circuit operation under normal conditions.

SETTING THE SET CURRENT

The set current can be expressed as:

$$I_{SET} = \frac{[(+V) - (2\,V_{BE}) - (-V)]}{R_{SET}}$$

where $+V$ is the voltage to which the control resistor is connected, $-V$ is the negative supply voltage, V_{BE} is the base emitter drop of Q_9 or Q_{10} (about 0.7V), and R_{SET} is the value of the external control resistor or set resistor. Equation 1 is simply a derivative of ohms law. There is also an analytical relationship betwen I_{SET} and the total supply current:

I_{SUPPLY} = [I_{SET} (current sourced by Q_6 to Q_8)
+ 2 I_{SET} (current sourced to the differential amplifier by Q_6)
+ 2 I_{SET} (current sourced to the comparator output by Q_6)]
× 4 (the total numbers of comparators)
+ I_{SET} (current sourced through Q_{11}, Q_{10}, and Q_9 to $-V$)

$$= [I_{SET} + 2\,I_{SET} + 2\,I_{SET}] \times 4 + I_{SET}$$

$$= 21\,I_{SET}$$

The output current pulldown capability (I_{OL}) of the UC161 is about 2 orders of magnitude greater than the high output drive current, (I_{OH}), which allows wire-ORing the outputs. I_{OH} is simply the current sourced by Q_6:

$$I_{OH} = 2 \times I_{SET}$$

I_{OL} is found by multiplying the current sourced by the collector of Q_6 by the gain Q_7:

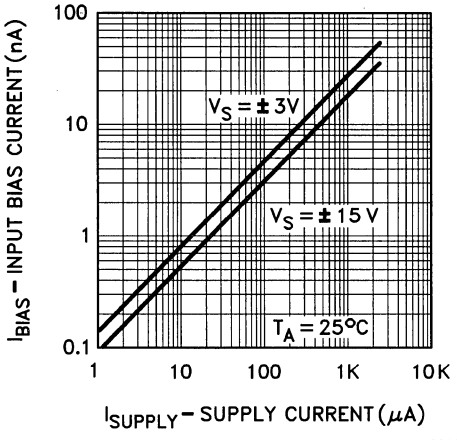
$$I_{OL} = \beta\,(Q_7) \times 2\,I_{SET}$$

The beta of Q_7 is about 75-150.

6

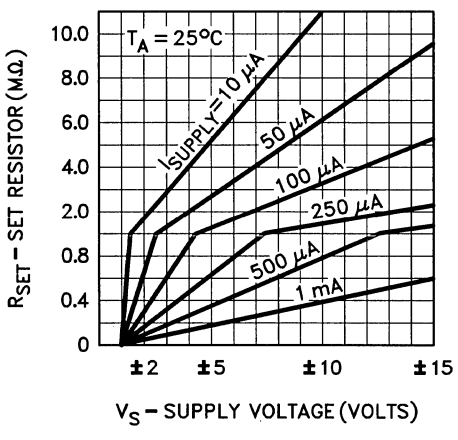
APPLICATION AND OPERATION INFORMATION (Continued)

Input Bias Current vs Supply Current



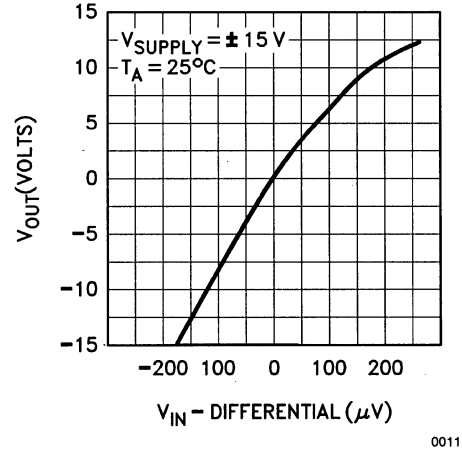
0011-3

R_{SET} vs V_{SUPPLY} for Various $I_{SUPPLIES}$



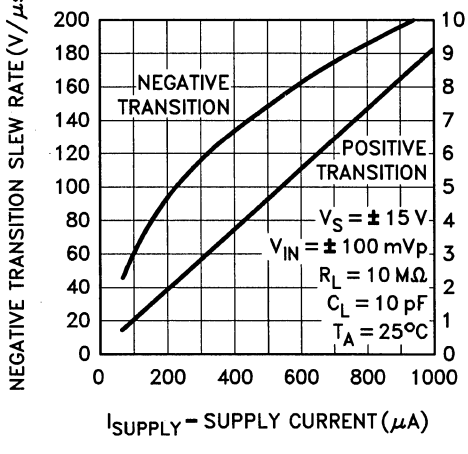
0011-4

Transfer Characteristic



0011-5

Slew Rate vs Supply Current



0011-6

LINEAR INTEGRATED CIRCUITS

High Slew Rate Operational Amplifier

UC542A
UC542B
UC542C

FEATURES

- High Slew Rate: 150V/μs typ.
- Fast Settling Time: 1% in 75 ns
- Open Loop Gain: 70 dB min.
- Low Offset Voltage Drift: 10 μV/C max.
- Wide Bandwidth: DC to 100 MHz at 10 dB Gain

DESCRIPTION

The UC542 amplifier is designed for applications requiring wide bandwidth, high slew rate and fast settling time. The amplifier has been set for optimum response at a closed loop gain of 20 dB without any additional compensation, however external frequency compensation may be added to tailor the transfer and transient response for optimum performance.

The design emphasis has been placed on obtaining high frequency performance without sacrificing key specification such as V_{OS}, I_{OS}, CMRR and PSRR.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltages

V^+ ..... +18V

V^- ..... −18V

Differential Input Voltage ..... ±7V

Input Voltage 4V

Output Short Circuit Duration ..... Indefinite

Power Dissipation, T_A = 25°C 1W
Derate 8 mW/°C for T_A > 25°C

Storage Temperature ..... −65°C to +150°C

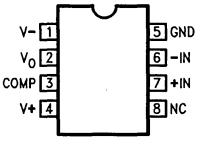
Note: All voltages are referenced to ground.

APPLICATIONS

- Wideband IF Amplifier
- Wideband Video Amplifier
- High Speed Integrator
- D/A and A/D Conversions

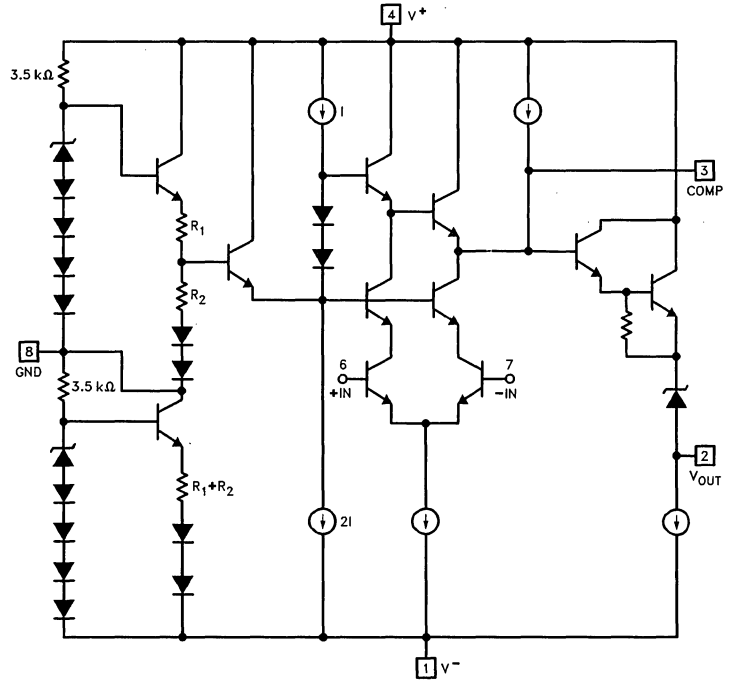
CONNECTION DIAGRAM

DIL-8 (TOP VIEW)
N or J PACKAGE



0016-1

SIMPLIFIED SCHEMATIC



0016-2

UNITRODE

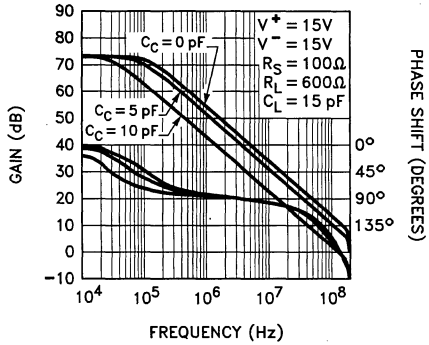
ELECTRICAL SPECIFICATIONS Unless otherwise stated, these specifications apply for $-55°C < T_A < 125°C$ for UC542A, $-25°C < T_A < 85°C$ for UC542B, $0°C < T_A < 70°C$ for UC542C, $|V+| = |V-| = 15V$ and pin 8 grounded.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS						
V+ Range			13		18	V
V− Range			−13		−18	V
V+ Supply Current	I+			15	20	mA
V− Supply Current	I−			−15	−20	mA
Power Supply Rejection	PSRR	$V_S = \pm 13V$ to $\pm 18V$			350	μV/V
INPUTS						
Input Offset Voltage	V_{OS}			2.0	5.0	mV
Input Offset Current	I_{OS}			50	200	nA
Input Bias Current	I_b			3.0	10	μA
Common Mode Rejection	CMRR	$V_{CM} = \pm 3V$	65	75		dB
Input Offset Voltage Drift	TCV_{OS}	$T_{MIN} < T_A \leq T_{MAX}$ (Note 2)		5.0	10	μV/°C
OUTPUT						
Output Voltage Swing	V_O	$R_L = 600$	±2.5			V
Output Sink Current			5	7		mA
Output Source Current			15	25		mA
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain	A_{VOL}	$R_L = 600$	70	75		dB
Open Loop Temp. Coeff.		$R_L = 600$		0.03		dB/°C
Closed Loop Bandwidth		Gain = 10 dB		100		MHz
TRANSIENT RESPONSE						
Slew Rate	SR	Gain = 20 dB (Note 2)	125	175		V/μs
Settling Time to 1%	t_S	Gain = 20 dB (Note 2)		60		ns

Note: 2. These parameters although guaranteed, are not 100% tested in production.

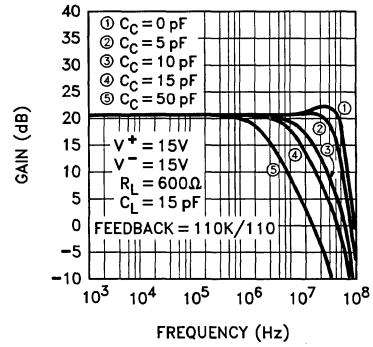
TYPICAL CHARACTERISTICS

UC542 Open Loop Gain and Phase vs Frequency



0016-3

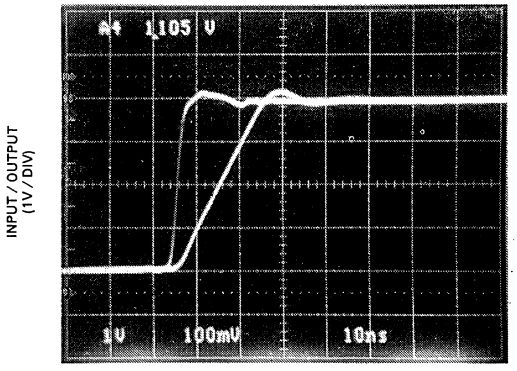
UC542 Closed Loop Gain = 20 dB Non-Inverting Amp



0016-4

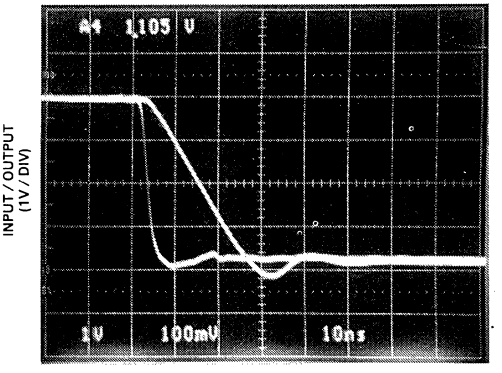
TYPICAL CHARACTERISTICS (Continued)

Large Signal Pulse Response



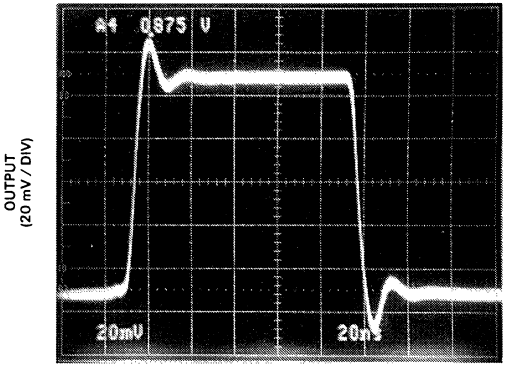
0016-5

Large Signal Pulse Response



0016-6

Small Signal Pulse Response



0016-7

Note: All pulse responses are at $|V^+| = |V^-| = 15V$, non-inverting gain of 20 dB (1k/110Ω) and $R_L = 600\Omega$; $C_L = 15$ pF.

OPERATING INSTRUCTIONS

Layout Considerations

The wide bandwidth of the UC542 necessitates that high frequency circuit layout procedures be followed. Failure to do so can result in marginal performance. A circuit board with a ground plan is recommended. Bypass capacitors (0.1 to 1.0 μF, ceramic) should be connected directly on the supply pins and lead lengths should be kept short as possible. If the compensation pin is not being used care should be taken not to add any stray capacitance to this pin. If desired the compensation pin can be cut off.

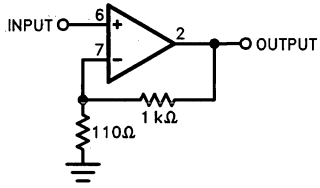
Output Level Adjustments

Pin 8 (gnd) does not need to be connected to ground unless well behave clipping levels are to be maintained. It is recommended that pin 8 be grounded at all times unless adjustments to the clipping levels are desired.

The clipping levels of the UC542 can be changed by connecting a pot between pin 4 (V+) and pin 8 (gnd). While the separations between the clipping levels remain, output swings up to 6V can be achieved. (See "Output Level Adjust" in Typical Applications.)

TYPICAL APPLICATIONS

N.I Gain of 20 dB
(Dynamic Test Circuit)



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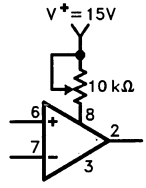
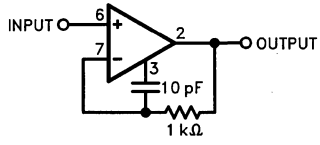
0 to 5V Output Level
Adjust Circuit



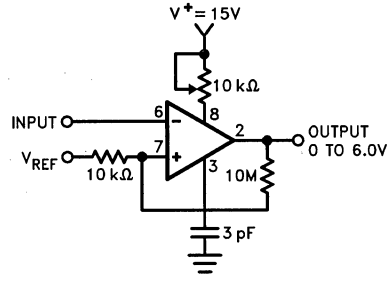
0016-9

Unity Gain Buffer
(SR ≅ 100 V/μs)



0016-10

Comparator with Hystersis



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DEVICE TEMPERATURE MANAGEMENT

All circuit components will dissipate some power while operating and this causes their temperature to rise. Unitrode integrated circuits are designed to handle a considerable range of temperatures, but there are limits. Each part is characterized for a particular temperature range, and the user must see to it that the specified limits are not exceeded. This brief note will give a few hints on how to do this.

With the power turned off, all components of a given circuit will be at the same temperature as the ambient air (assuming, of course, that sufficient time has elapsed for all differences to settle). With the power on, the various components will be warmed up due to their internal power dissipation, until a new state of equilibrium is reached. In this state, some devices may be hotter than others, and the air temperature will also be higher than before, but for each device it will be true that the amount of heat generated internally is equal to the amount of heat removed by the air. In the case of an I.C., for example, heat transfer occurs between the device's case and the air, as well as by conduction through the P.C. board, or heatsink, and from there to the air.

Since all the heat is generated at the silicon chip, it is safe to assume that the chip must be hotter than the IC case; the case must be hotter than the air, or board, or heatsink; and the board or heatsink must be hotter than the air. In short, heat flows downhill, from points of higher temperature to cooler spots.

The rate of heat flow depends on the temperature difference (ΔT) between the two end points, and also on a quantity called "thermal resistance," which is represented by the symbol θ. Heat is a form of energy, and if we choose the joule as the measuring unit, we can specify the rate of heat flow in units of joules per second. Therefore,

$$\text{Rate of heat flow} = \frac{\Delta T}{\theta} \text{ [joules per second]}$$

and since joules per second is the same as watts (W), we have

$$\theta = \frac{\Delta T}{W} \text{ [°C per watt]}$$

The quantity θ defines an important property of materials, with the better thermal conductors having the lowest θ values. Since IC chips must be protected by a variety of packages, it is important for the user to know the thermal resistance θ of each type of package, in order to make certain predictions about the thermal behavior of the device in his circuit.

UICC PACKAGE RATINGS

Package Type	Typ. θ_{JC}, °C/W	Typ. θ_{JA}, °C/W
D = 14 Pin S.O.	N/A	150
F = Ceramic Flat Pack	50	150
H = TO-39	20	130
J = Ceramic DIP		
8-Pin	40	130
14-Pin	30	80
16-Pin	30	80
18-Pin	30	75
K = TO-3	3	35
L = Ceramic Leadless Chip Carrier	15	70
N = Plastic DIP		
8-Pin	60	125
14-Pin	50	100
16-Pin	50	100
18-Pin	40	90
24-Pin	35	80
16-Pin Batwing	50	80
P = 24-Pin Power Cerdip	3	25
Q = 20-Pin PLCC	N/A	100
R = TO-66	5	40
S = Side Braised Ceramic	25	90
T = TO-220	3	60
V = 15-Pin Multiwatt®	3	35

Table 1—Thermal resistance of various Unitrode IC packages. θ_{JC} is the thermal resistance from chip to case, while θ_{JA} is the value from chip to air.

Table 1 shows the following θ values for Unitrode IC packages:

θ_{JC}: thermal resistance from chip junction to case.
θ_{JA}: thermal resistance from chip junction to air.

The values of θ_{JC} and θ_{JA} given in the table are not necessarily exact numbers, but rather conservative ones, so that by using them, you will tend to err on the side of improved reliability.

You will have noticed that Equation (1) is a sort of "thermal Ohm's law", and that if you know any two of the quantities involved, you can calculate the third. With the θ values given in Table 1, you can always calculate the junction temperature by measuring the net input power to the IC.

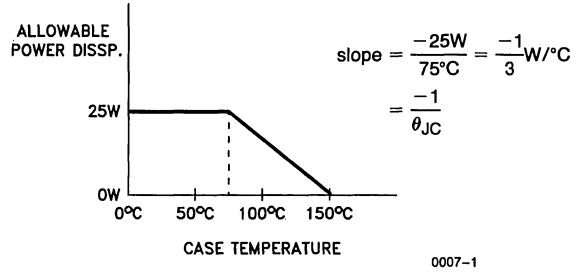
Now, consider a device such as the UC3620. The data sheet gives us the following Absolute Maximum Ratings:

Total Power Dissipation

(T_{case} = 75°C).....25W

Storage & Junction Temp .....+40°C to +150°C

We can sketch the curve below:



Although the data sheet does not specifically state the derating factor, we can calculate it from the information given; it is the slope of the line from $+75°C$ to $+150°C$. In this case, the value is $-\frac{1}{3}W/°C$ at case temperatures above $+75°C$. We note that the junction temperature anywhere along the curve is $+150°C$, and since this is the maximum allowable temperature, we must take steps to stay within the area below the curve.

The thermal resistance can be found by simply taking the reciprocal of the derating factor. In the case of our UC3620 for example:

$$\theta_{JC} = 3°C/W$$

which is also the value given in Table 1 for the 15-pin Multiwatt package.

Suppose one intends to use the UC3620 at 2A continuous output current. The data sheet states that the total voltage drop at the output stages is 3.6V maximum. At 2A, this will result in an internal dissipation of 7.2W. If the supply voltage is say, 36V, the quiescent current of 55 mA maximum gives us an additional 2W of internal heating, for a total of 9.2W. Furthermore, we decide to provide sufficient cooling to keep the junction temperature at a maximum of 100°C—for increased reliability. Suppose the ambient temperature is to be $+50°C$ maximum. Then, our ΔT is $100°C - 50°C = 50°C$, and the required thermal resistance from junction to air will be

$$\theta_{CA} = \frac{50°C}{9.2W} = 5.43°C/W$$

We know already that $\theta_{JC} = 3°C/W$. Mounting the IC to a heatsink will result in an additional thermal resistance in series. If you decide to use a mica insulator coated with thermal grease, you insert an additional 0.3°C/W (see any Semiconductor Accessories Catalog). Therefore, we need a heatsink with a θ_{CA} value of

$$\theta_{CA} = 5.43 - 3 - 0.3 = 2.13°C/W$$

This is the maximum value of thermal resistance between mounting surface and air that will keep the junction temperature at or below the chosen value of 100°C. We need only to go through a heatsink manufacturer's catalog to find a suitable part or extrusion with the required θ_{CA} value.

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PACKAGING INFORMATION
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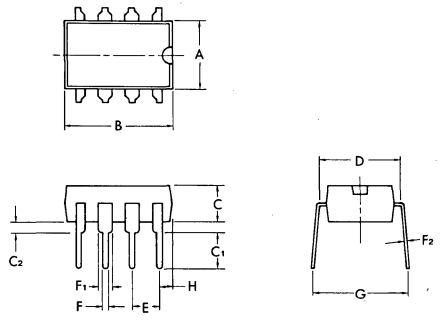
PACKAGING INFORMATION

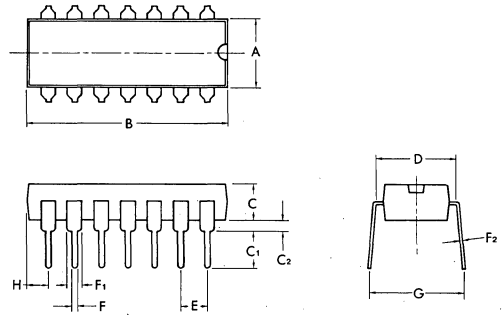
8-PIN PLASTIC
N PACKAGE

SYMBOL	DIMENSIONS.			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.245	.260	6.22	6.60
B	.370	.400	9.40	10.16
C	.125	.155	3.18	3.94
C_1	.125	.150	3.18	3.81
C_2	.015	.035	0.38	0.89
D	.290	.310	7.37	7.87
E	.090	.110	2.29	2.79
F	.015	.023	0.38	0.58
F_1	.045	.055	1.14	1.40
F_2	.008	.015	0.20	0.38
G	.300	.400	7.62	10.16
H	.025	.045	0.64	1.14



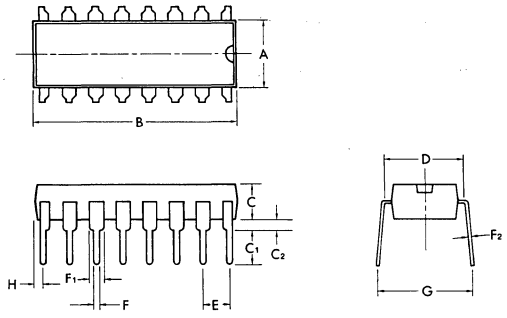
14-PIN PLASTIC
N PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.245	.260	6.22	6.60
B	.745	.810	18.92	20.57
C	.120	.140	3.05	3.56
C_1	.125	.150	3.18	3.81
C_2	.015	.035	0.38	0.89
D	.290	.310	7.37	7.87
E	.090	.110	2.29	2.79
F	.015	.023	0.38	0.58
F_1	.045	.065	1.14	1.65
F_2	.008	.015	0.20	0.38
G	.300	.400	7.62	10.16
H	.065	.085	1.65	2.16



16-PIN PLASTIC
N PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.245	.260	6.22	6.60
B	.745	.810	18.92	20.57
C	.120	.140	3.05	3.56
C_1	.125	.150	3.18	3.81
C_2	.015	.035	0.38	0.89
D	.290	.310	7.37	7.87
E	.090	.110	2.29	2.79
F	.015	.023	0.38	0.58
F_1	.045	.065	1.14	1.65
F_2	.008	.015	0.20	0.38
G	.300	.400	7.62	10.16
H	.025	.063	0.64	1.60



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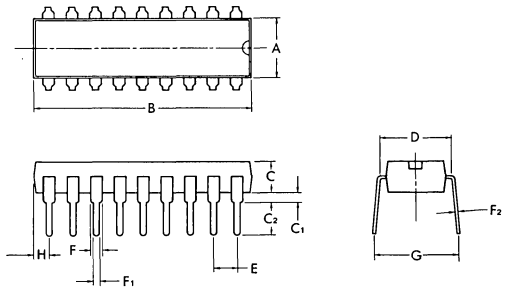
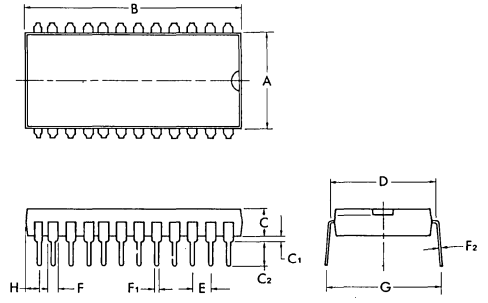
18-PIN PLASTIC
N PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.245	.260	6.22	6.60
B	.890	.920	22.61	23.39
C	.120	.140	3.05	3.56
C_1	.015	.035	0.38	0.89
C_2	.125	.150	3.18	3.81
D	.290	.310	7.37	7.87
E	.090	.110	2.29	2.79
F	.045	.065	1.14	1.65
F_1	.015	.023	0.38	0.58
F_2	.008	.015	0.20	0.38
G	.300	.400	7.62	10.16
H	.055	.080	1.40	2.03



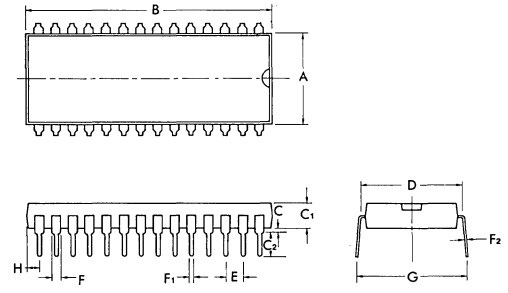
24-PIN PLASTIC
N PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.550	12.70	13.97
B	1.230	1.270	31.24	32.26
C	.150	.160	3.81	4.06
C_1	.015	.035	0.38	0.89
C_2	.125	.150	3.18	3.81
D	.590	.610	14.99	15.49
E	.090	.110	2.29	2.79
F	.040	.065	1.02	1.65
F_1	.015	.023	0.38	0.58
F_2	.006	.015	0.15	0.38
G	.500	.700	12.70	17.78
H	.065	.085	1.65	2.16



28-PIN PLASTIC
N PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.550	12.70	13.97
B	1.305	1.450	33.15	36.83
C	.015	.035	0.38	0.89
C_1	.140	.180	3.56	4.57
C_2	.125	.150	3.18	3.81
D	.590	.610	14.99	15.49
E	.090	.110	2.29	2.79
F	.040	.065	1.02	1.65
F_1	.015	.023	0.38	0.58
F_2	.008	.015	0.20	0.38
G	.700	.800	17.78	20.32
H	.065	.085	1.65	2.16



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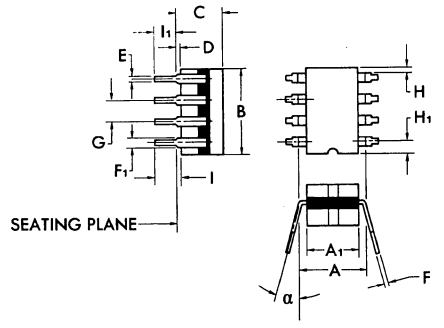
PACKAGING INFORMATION

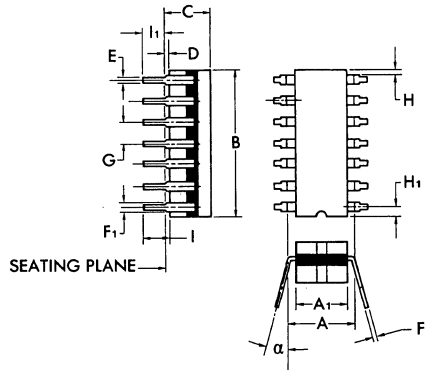
8-PIN CERAMIC
J PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.290	.320	7.37	8.13
A_1	.220	.310	5.59	7.87
B	---	.405	---	10.29
C	---	.200	---	5.08
D	.015	.060	0.38	1.52
E	.014	.023	0.36	0.58
F	.008	.015	0.20	0.38
F_1	.030	.070	0.76	1.78
G	.100 BSC		2.54 BSC	
H	.005	---	0.13	---
H_1	---	.055	---	1.35
I	.150	---	3.81	---
I_1	.125	.200	3.18	5.08
α	0°	15°	0°	15°



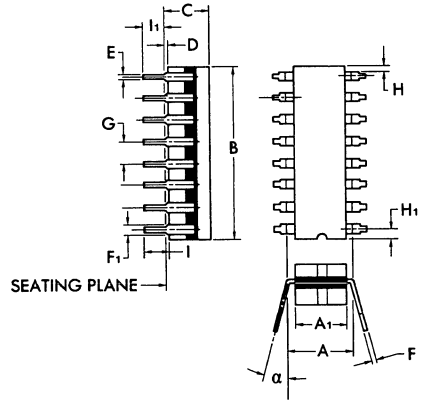
14-PIN CERAMIC
J PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.290	.320	7.37	8.13
A_1	.220	.310	5.59	7.87
B	---	.785	---	19.94
C	---	.200	---	5.08
D	.015	.060	0.38	1.52
E	.014	.023	0.36	0.58
F	.008	.015	0.20	0.38
F_1	.030	.070	0.76	1.78
G	.100 BSC		2.54 BSC	
H	.005	---	0.13	---
H_1	---	.098	---	2.49
I	.150	---	3.81	---
I_1	.125	.200	3.18	5.08
α	0°	15°	0°	15°



16-PIN CERAMIC
J PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.290	.320	7.37	8.13
A_1	.220	.310	5.59	7.87
B	---	.840	---	21.34
C	---	.200	---	5.08
D	.015	.060	0.38	1.52
E	.014	.023	0.36	0.58
F	.008	.015	0.20	0.38
F_1	.030	.070	0.76	1.78
G	.100 BSC		2.54 BSC	
H	.005	---	0.13	---
H_1	---	.080	---	2.03
I	.150	---	3.81	---
I_1	.125	.200	3.18	5.08
α	0°	15°	0°	15°



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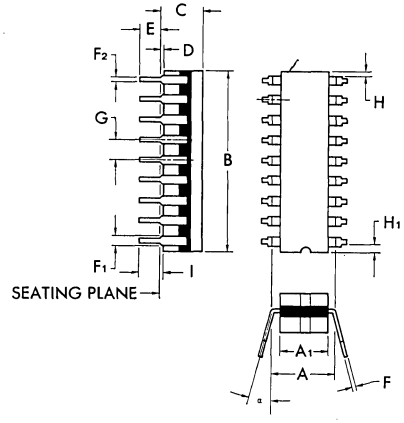
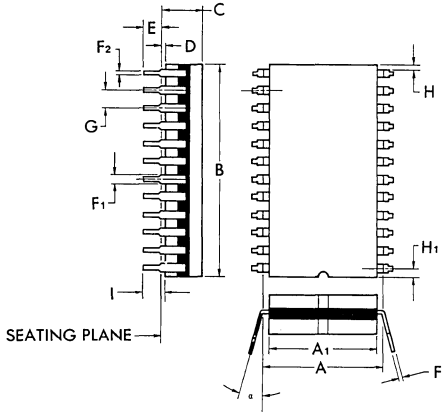
18-PIN CERAMIC J PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.290	.320	7.37	8.13
A_1	.220	.310	5.59	7.87
B	---	.960	---	24.38
C	---	.200	---	5.08
D	.015	.060	0.38	1.52
E	.125	.200	3.18	5.08
F	.008	.015	0.20	0.38
F_1	.030	.070	0.76	1.78
F_2	.014	.023	0.36	0.58
G	.100 BSC		2.54 BSC	
H	.005	---	0.13	---
H_1	---	.098	---	2.49
I	.150	---	3.81	---
α	0°	15°	0°	15°



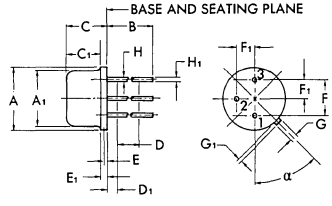
24-PIN CERAMIC J PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.620	12.70	15.75
A_1	.500	.610	12.70	15.49
B	---	1.290	---	32.77
C	---	.225	---	5.72
D	.015	.075	0.38	1.91
E	.120	.200	3.05	5.08
F	.008	.015	0.20	0.38
F_1	.030	.070	0.76	1.78
F_2	.014	.023	0.36	0.58
G	.100 BSC		2.54 BSC	
H	.005	---	0.13	---
H_1	---	.098	---	2.49
I	.150	---	3.81	---
α	0°	15°	0°	15°



3-PIN TO-5 METAL H PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
A_1	.305	.335	7.75	8.51
B	.500	---	12.70	---
C	.165	.185	4.19	4.70
C_1	.125	.155	3.18	3.94
D	.250	---	6.35	---
D_1	---	.050	---	1.27
E	.009	.041	0.23	1.04
E_1	---	.050	---	1.27
F	.200 T.P.		5.08 T.P.	
F_1	.100 T.P.		2.54 T.P.	
G	.028	.034	0.71	0.86
G_1	.029	.045	0.74	1.14
H	.016	.019	0.41	0.48
H_1	.016	.021	0.41	0.53
α	45° T.P.		45° T.P.	



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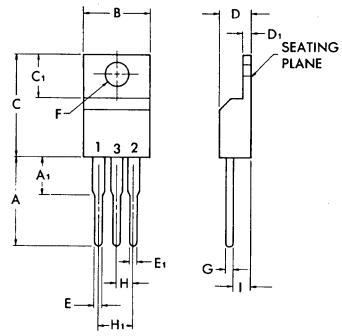
PACKAGING INFORMATION

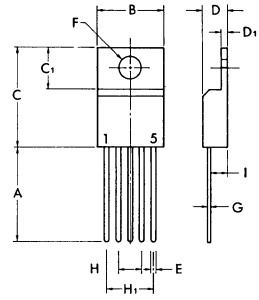
3-PIN TO-220 PLASTIC
T PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.562	12.70	14.27
A_1	---	.250	---	6.35
B	.380	.420	9.66	10.66
C	.560	.625	14.23	15.87
C_1	.230	.270	5.85	6.85
D	.140	.190	3.56	4.82
D_1	.045	.055	1.14	1.39
E	.020	.045	0.51	1.14
E_1	.045	.070	1.14	1.77
F	.139	.147	3.53	3.73
G	.015	.025	0.38	0.64
H	.090	.110	2.29	2.79
H_1	.190	.210	4.83	5.33
I	.080	.115	2.04	2.92



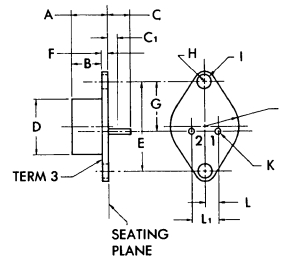
5-PIN TO-220 PLASTIC
T PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.580	12.70	14.73
B	.380	.420	9.65	10.67
C	.560	.650	14.22	16.51
C_1	.230	.270	5.84	6.86
D	.140	.190	3.56	4.83
D_1	.020	.055	0.51	1.40
E	.020	.045	0.51	1.14
F	.139	.161	3.53	4.09
G	.012	.045	0.30	1.14
H	---	.134	---	3.40
H_1	---	.268	---	6.81
I	.080	.115	2.03	2.92



2-PIN TO-3 METAL
K PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.250	.450	6.35	11.43
B	.190	.315	4.83	8.00
C	.312	.500	7.92	12.70
C_1	---	.050	---	1.27
D	---	.875	---	22.22
E	1.177	1.197	29.90	30.40
F	.060	.135	1.52	3.43
G	.655	.675	16.64	17.14
H	.131	..188	3.33	4.78
I	.151	.161	3.84	4.09
J	.495	.525	12.57	13.34
K	.038	.043	0.97	1.09
L	.205	.225	5.21	5.72
L_1	.420	.440	10.67	11.18



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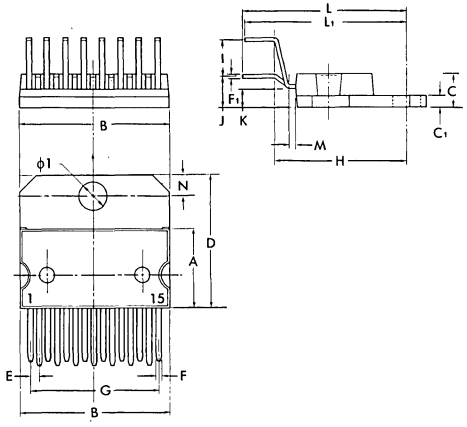
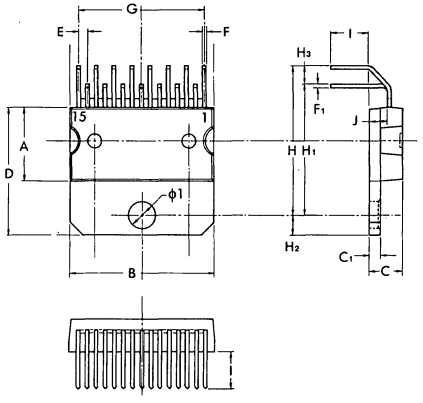
15-PIN VERTICAL MULTI WATT
V PACKAGE

SYMBOL	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	.417	.421	.425	10.60	10.70	10.80
B	.783	.787	.791	19.90	20.00	20.10
C	.174	.177	.180	4.43	4.50	4.58
C_1	.059	.060	.061	1.50	1.52	1.54
D	.685	.689	.693	17.40	17.50	17.60
E	.046	.050	.054	1.17	1.27	1.37
F	.026	.028	.029	0.66	0.70	0.72
F_1	.019	.020	.021	0.50	0.52	0.54
G	.696	.700	.704	17.68	17.78	17.88
H	.695	.699	.703	17.65	17.75	17.85
I	.196	.200	.204	4.98	5.08	5.18
J	.165	.169	.173	4.20	4.30	4.40
K	.096	.100	.104	2.45	2.55	2.65
L	.862	.873	.876	21.90	22.17	22.25
L_1	.856	.860	.864	21.75	21.85	21.95
M	---	.040	---	---	1.00	---
N	.109	.110	.111	2.78	2.80	2.83
$\phi 1$	.149	.150	.151	3.78	3.80	3.82



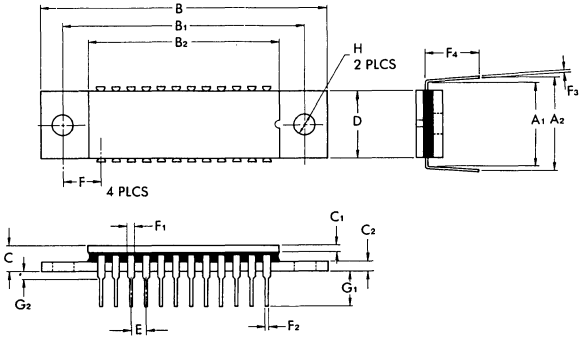
15-PIN HORIZONTAL MULTI WATT
HV PACKAGE

SYMBOL	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	.417	.421	.425	10.60	10.70	10.80
B	.783	.787	.791	19.90	20.00	20.10
C	.174	.177	.180	4.43	4.50	4.58
C_1	.059	.060	.061	1.49	1.52	1.54
D	.685	.689	.693	17.40	17.50	17.60
E	.046	.050	.054	1.17	1.27	1.37
F	.026	.028	.029	0.66	0.70	0.72
F_1	.019	.020	.021	0.50	0.52	0.54
G	.696	.700	.704	17.68	17.78	17.88
H	.806	.810	.814	20.47	20.57	20.67
H_1	.706	.710	.714	17.93	18.03	18.13
H_2	.109	.110	.111	2.78	2.80	2.83
H_3	.094	.100	.104	2.44	2.54	2.64
I	.206	.208	.210	5.23	5.28	5.33
J	.096	.100	.104	2.45	2.55	2.65
$\phi 1$	.149	.150	.151	3.78	3.80	3.82



24-PIN POWER CERAMIC
P PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A_1	.600		15.24	
A_2	.650		16.51	
B	1.900		48.26	
B_1	1.600		40.64	
B_2	1.250		31.75	
C	---	.180	---	4.57
C_1	.040		1.02	
D	.520		13.21	
E	.100		2.54	
F	.240	.260	6.10	6.60
F_1	.045	.055	1.14	1.40
F_2	.016	.020	0.41	0.51
F_3	.009	.011	0.23	0.28
F_4	.265		6.73	
G_1	.183	---	4.65	---
G_2	.015		0.38	
H	.140		3.56	



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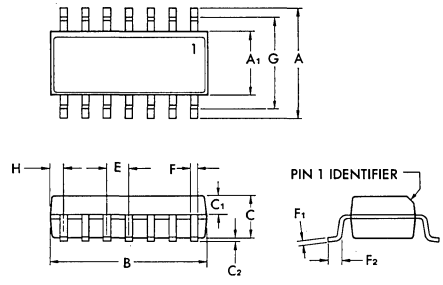
PACKAGING INFORMATION

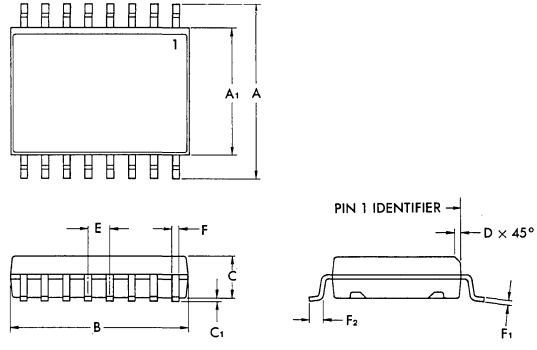
14-PIN PLASTIC SO IC SURFACE MOUNT
D PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A_1	.150	.158	3.80	4.00
B	.336	.344	8.55	8.75
C	.053	.069	1.35	1.75
C_1	.024	.031	0.61	0.78
C_2	.004	.008	0.10	0.20
D	.015 BSC		0.37 BSC	
E	.050 BSC		1.27 BSC	
F	.014	.018	0.35	0.45
F_1	.007	.009	0.19	0.22
F_2	.025	.030	0.64	0.77
G	.181	.205	4.60	5.20
H	.018	.022	0.45	0.56



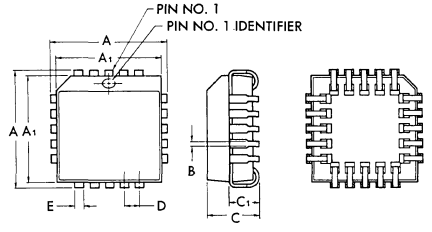
16-PIN PLASTIC SO IC SURFACE MOUNT
D PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.400	.410	10.16	10.41
A_1	.292	.299	7.42	7.59
B	.403	.413	10.24	10.49
C	.097	.104	2.46	2.64
C_1	.0055	.0115	0.140	0.292
D	.011	.016	0.28	0.41
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
F_1	.010		0.25	
F_2	.018	.035	0.46	0.89



20-PIN PLASTIC PLCC SURFACE MOUNT
Q PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.385	.395	9.78	10.03
A_1	.350	.356	8.89	9.04
B	.013	.021	0.33	0.53
C	.170	.180	4.32	4.57
C_1	.100	.110	2.54	2.79
D	.053		1.35	
E	.026	.032	0.66	0.81



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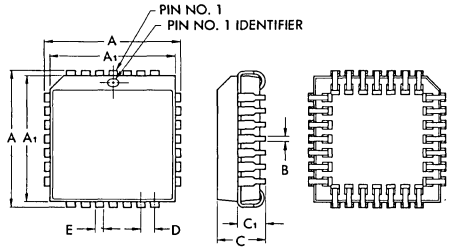
PACKAGING INFORMATION

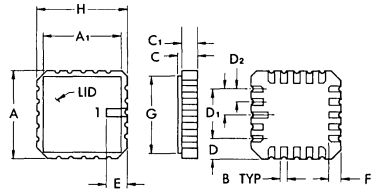
28-PIN PLASTIC PLCC SURFACE MOUNT
Q PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.485	.495	12.32	12.57
A_1	.450	.454	11.43	11.53
B	.013	.021	0.33	0.53
C	.170	.180	4.32	4.57
C_1	.100	.110	2.54	2.79
D	.053		1.35	
E	.026	.032	0.66	0.81



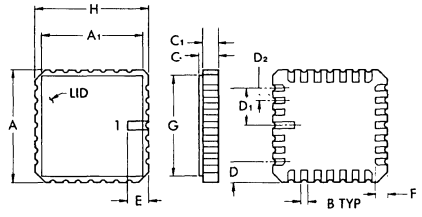
20-PIN CERAMIC LEADLESS SURFACE MOUNT
L PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.342	.358	8.69	9.09
A_1	---	.358	---	9.09
B	.022	.028	0.56	0.71
C	.064	.100	1.63	2.54
C_1	.054	.088	1.37	2.24
D	.075 REF		1.91 REF	
D_1	.100 BSC		2.54 BSC	
D_2	.050 BSC		1.27 BSC	
E	.077	.107	1.96	2.72
F	.045	.055	1.14	1.40
G	---	.358	---	9.09
H	.342	.358	8.69	9.09



28-PIN CERAMIC LEADLESS SURFACE MOUNT
L PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.442	.460	11.23	11.68
A_1	---	.460	---	11.68
B	.022	.028	0.56	0.71
C	.065	.100	1.63	2.54
C_1	.054	.088	1.37	2.24
D	.075 REF		1.91 REF	
D_1	.150 BSC		3.81 BSC	
D_2	.050 BSC		1.27 BSC	
E	.077	.107	1.96	2.72
F	.045	.055	1.14	1.40
G	---	.460	---	11.68
H	.442	.460	11.23	11.68



7

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SURFACE MOUNT CONNECTION DIAGRAMS

The following pages contain connection diagrams for either plastic or ceramic, commercial temperature range (0°C to +70°C), surface mount packages.

Mechanical drawings may be found on page 7-14 for the 20 Pin PLCC surface mount "Q" package and page 7-15 for the 20 Pin LCC surface mount "L" package. Note: The UC5170 and UC5180 are only available in the 28 Pin PLCC surface mount "Q" package (see page 7-15).

For other temperature requirements and for availability information please contact the factory.

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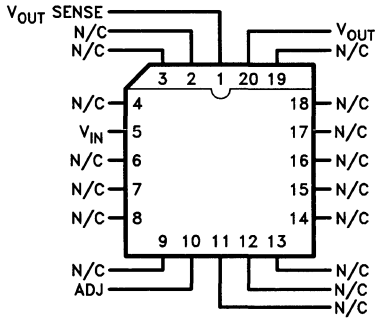
SURFACE MOUNT CONNECTION DIAGRAMS

UC317Q



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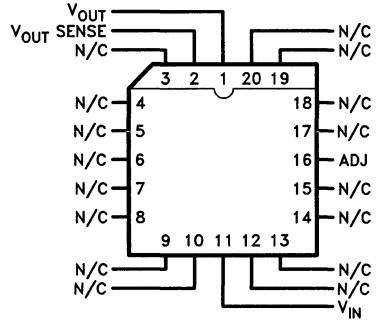

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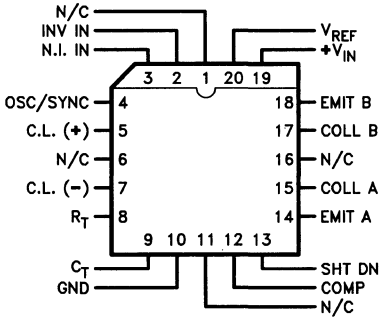

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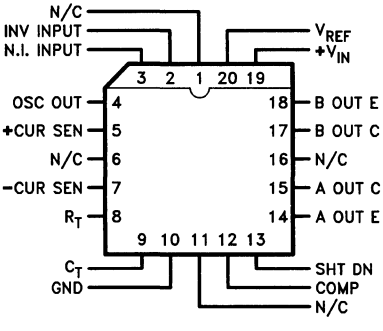

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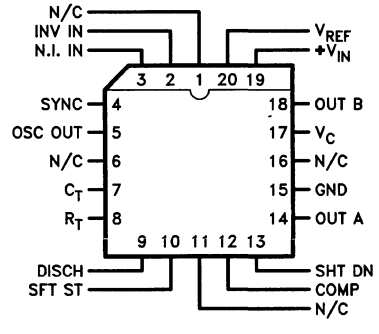

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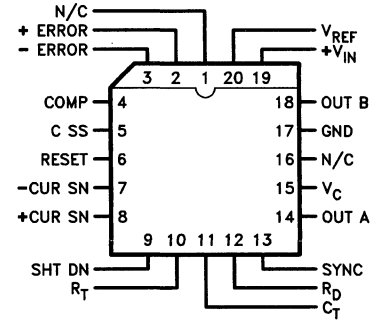

SURFACE MOUNT CONNECTION DIAGRAMS (Continued)

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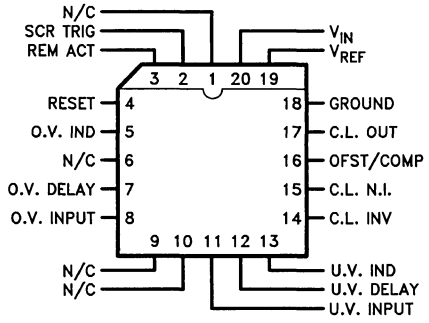

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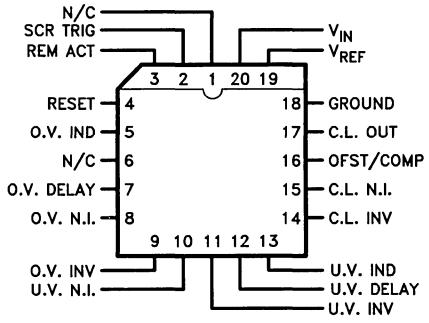

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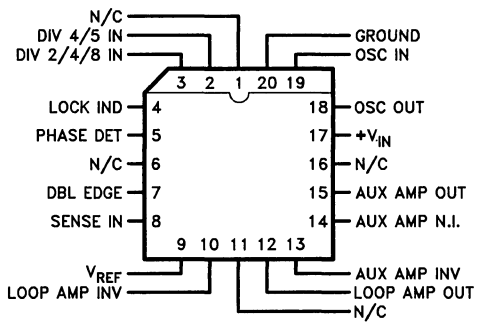

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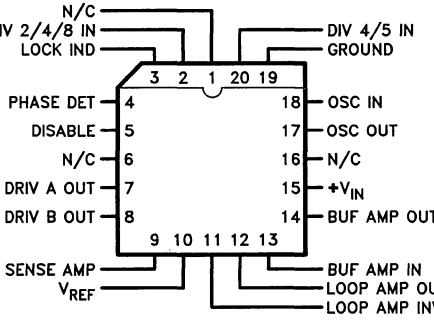

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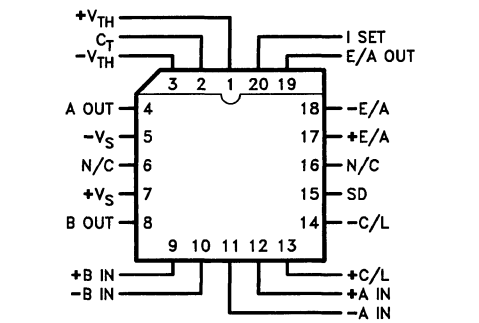

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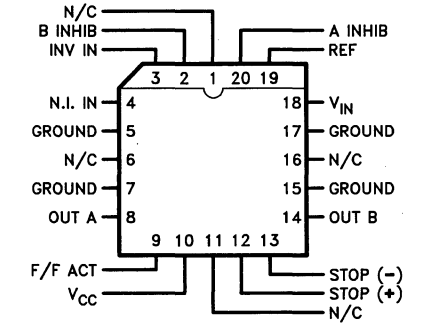

0020-2

8

SURFACE MOUNT CONNECTION DIAGRAMS (Continued)

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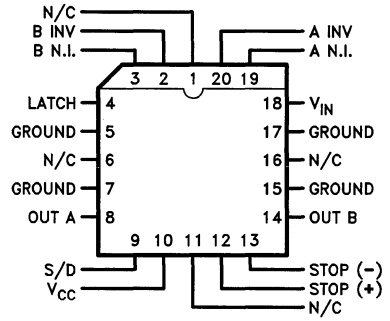

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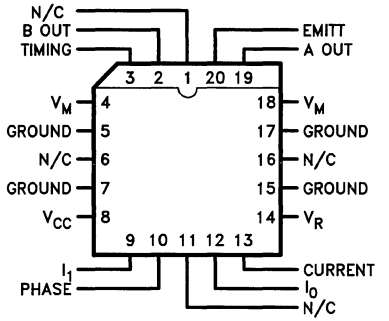

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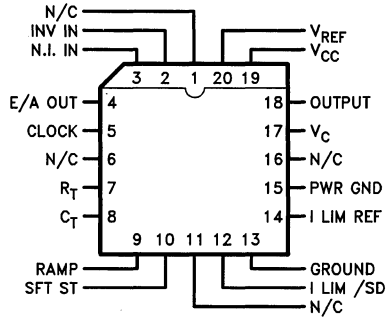

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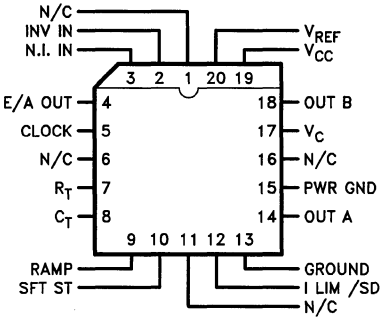

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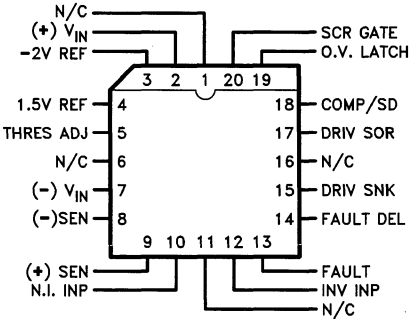

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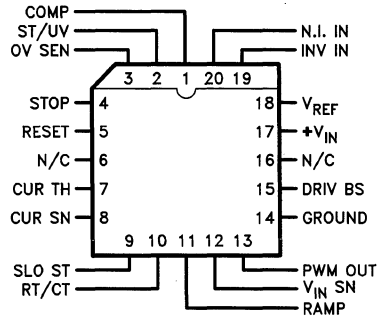

0020-20

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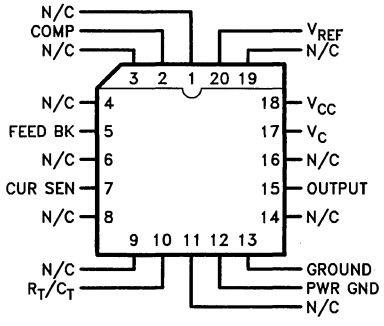
SURFACE MOUNT CONNECTION DIAGRAMS (Continued)

UC3842/43/44/45Q



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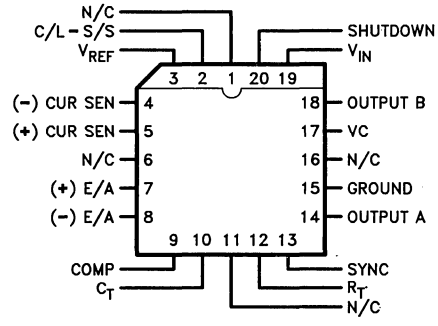

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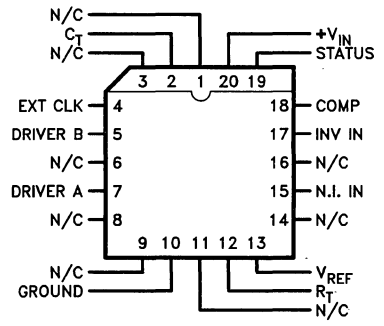

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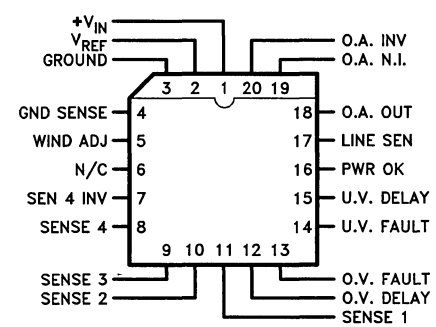

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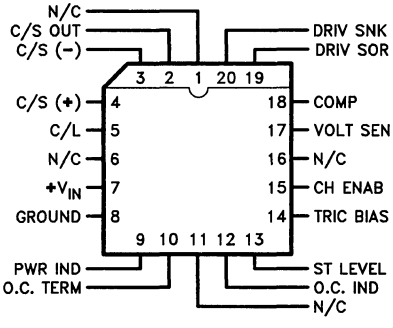

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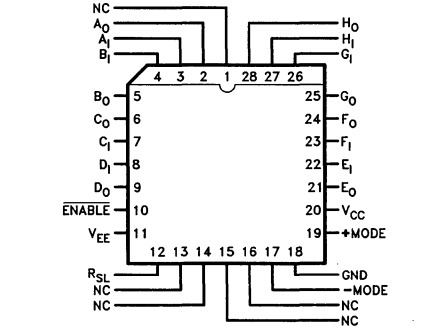

0020-26

8

SURFACE MOUNT CONNECTION DIAGRAMS (Continued)

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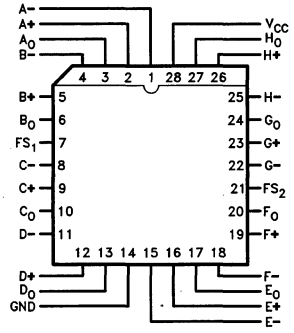

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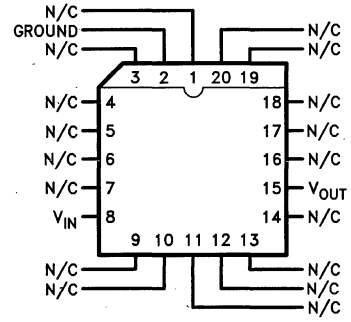
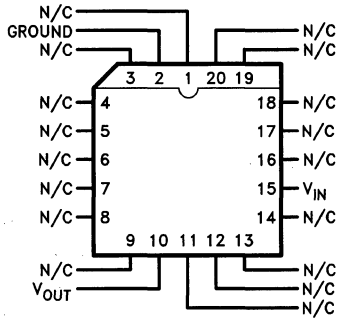


0020-11

UC7900Q



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APPLICATION NOTES
TABLE OF CONTENTS

LINEAR INTEGRATED CIRCUITS

9

CURRENT MODE — GENERAL

A SECOND-GENERATION IC SWITCH MODE CONTROLLER OPTIMIZED FOR HIGH FREQUENCY POWER MOSFET DRIVE

Introduction

Since the introduction of the SG1524 in 1976, integrated circuit controllers have played an important role in the rapid development and exploitation of high-efficiency switching power supply technology. The 1524 soon became an industry standard and was widely second-sourced (it is available from Unitrode as the UC1524). Although this device, as well as the MC3420 and TL494 which followed it, contained all the basic control elements required for switching regulator design; practical power supplies still required other functions which had to be implemented with additional external discrete circuitry.

An additional development within the semiconductor industry was the introduction of practical power FETs which offered the potential of higher efficiencies at higher speeds with resultant lower overall system costs. In order to be able to take full advantage of the speed capabilities of power FETs, it was necessary to provide high peak currents to the gate during turn-on and turn-off to quickly charge and discharge the gate capacitances of 800 to 2000pF present in higher current units.

The development of a second-generation regulating PWM IC, the UC1525A, and its complimentary output version, the UC1527A, was a direct result of the desire to add more power supply elements to the control IC, as well as to optimize the interfacing of high current power devices.

Integrating More Power Supply Functions

Having achieved the greatest level of acceptance among users of first generation control chips, the 1524 became the starting point for expanding IC controller capabilities. This early device, shown in *Figure 1*, contains a fixed-voltage reference source, an oscillator which generates both a clock signal and a linear ramp

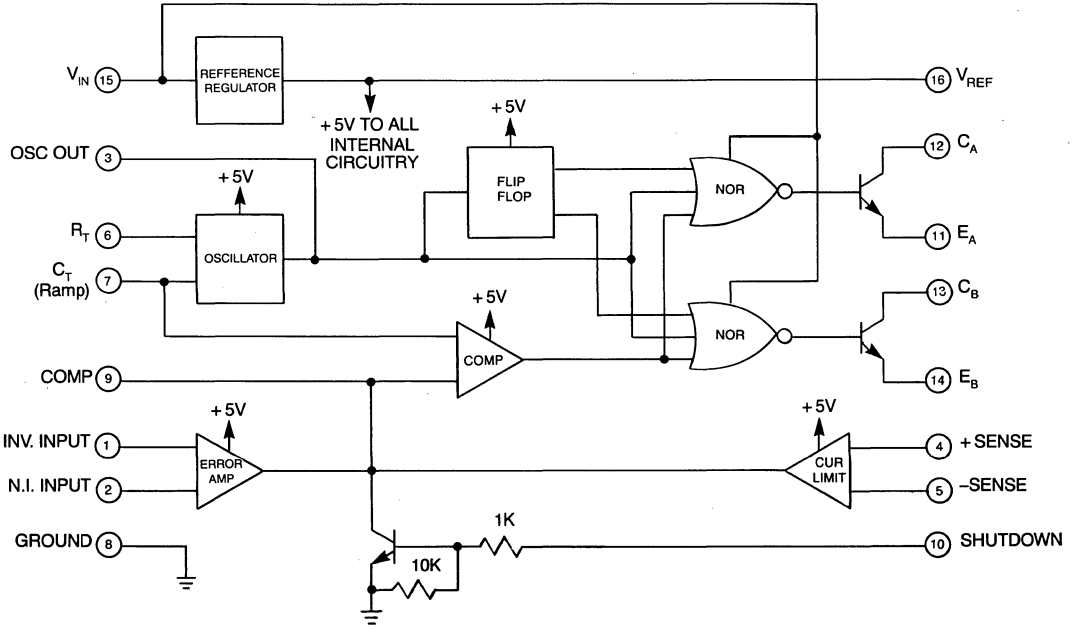

Figure 1. The UC1524 Regulating PWM Block Diagram. This design was the first complete IC control chip for switch mode power supplies.

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waveform, a PWM comparator, and a toggle flip-flop with output gating to switch the PWM signal alternately between the two outputs.

With this circuitry already defined, a two pronged development effort was initiated: 1) to add additional features required by most power supply designs and 2) to improve the utility of features already included within the 1524. The resultant block diagram for the UC1525A is shown in *Figure 2.* Two general comments should be made relative to the overall block diagram. First, in optimizing the output stage for bi-directional, low impedance switching, commitments had to be made as to whether the output should be high or low during the active, or ON state. Since this is application defined there are needs for both output states, so both were developed with the UC1525A device defined by an output configuration which is high during the ON pulse, and the UC 1527A configured to remain high during the OFF state. This difference is implemented by a mask option which eliminates inverter Q_4 (see Figure 3) for the UC1527A. In all other respects, the 1525A and 1527A are identical and any description of the 1525A characteristics apply equally to the 1527A. Second, a major difference between this new controller and the earlier 1524 is the deletion of the current limit amplifier. There are so many system considerations in providing current control that it is preferable to leave this as a user-defined external option and allocate the package pins to other, more universally requested functions. Current limiting possibilities are discussed further under shutdown options.

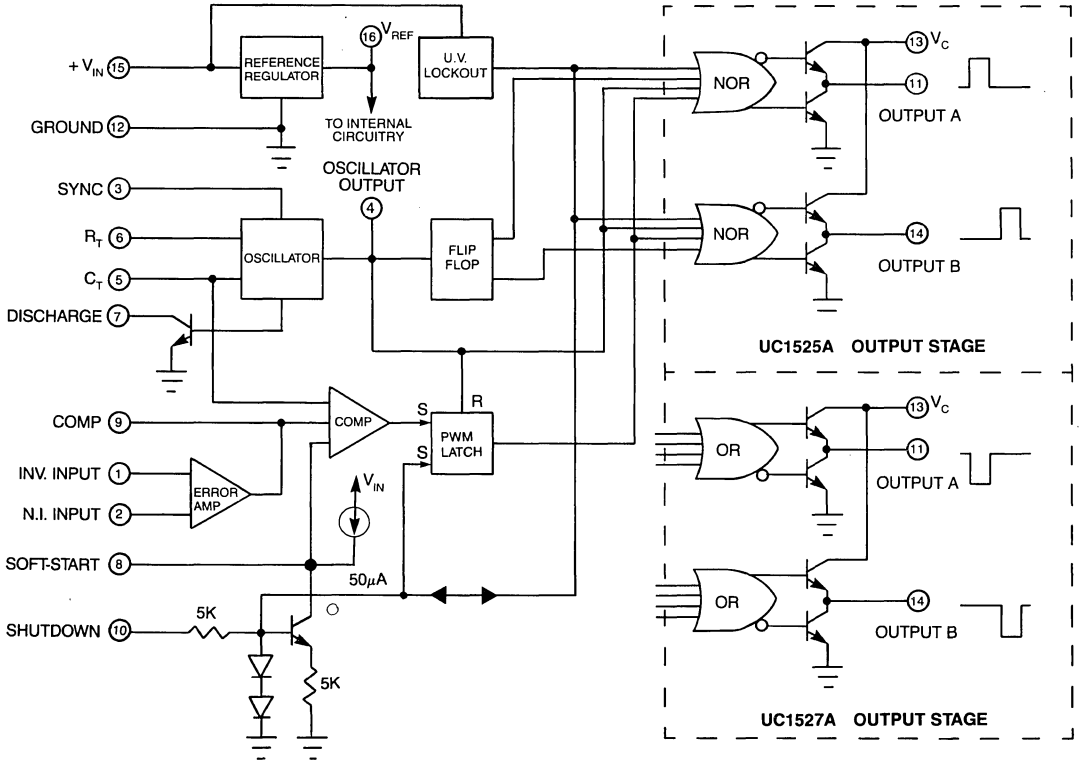

Figure 2. The UC1525A family represents a "second generation" of IC controllers.

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"Totem-Pole" Output Stage

One of the most significant benefits in using the UC1525A is its output configuration. For the first time it has been recognized in an IC controller that it is more difficult to turn a power switch off than turn it on. With the UC1525A, a high-current, fast transition, low impedance drive is provided for both turn-on and turn-off of an external power transistor or FET. The circuit schematic of one of the two output stages contained within the device is shown in *Figure 3.* This is a two-state output, either Q_8 is on, forming a low saturation voltage pull-down, or Q_7 is on, pulling the output up to V_C. Note that V_C is a separate terminal from the V_{IN} supply to the rest of the device. This offers the benefits of potentially operating the output drive from a lower supply than the rest of the circuit for power efficiencies, decoupling of drive transients from more sensitive circuits, and a third terminal for extracting a drive signal. Note that even though V_C can be set either higher or lower than V_{IN}, the output cannot rise higher than approximately 1½ volts below V_{IN}.

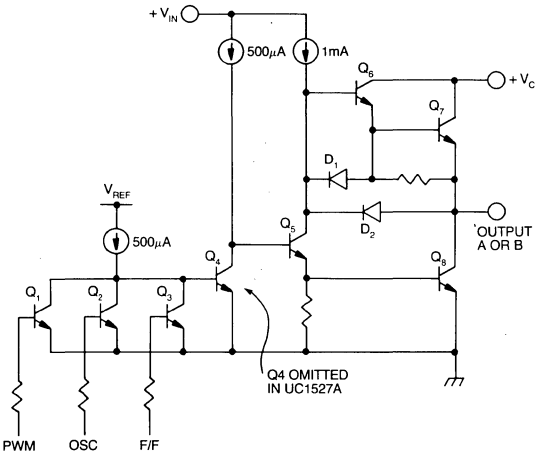

Figure 3. One of two power output stages contained within the UC1525A which conduct alternately due to the internal flip-flop.

During the transition between states, there is a slight conduction overlap between source and sink which results in a pulse of current flowing from V_C to ground. However, due to the high-speed design configuration of this stage, this current spike lasts for only about 100ns. A typical current waveform at V_C is shown in *Figure 4.* This transient will normally be decoupled from the rest of the control power by a 0.1mfd capacitor from V_C to ground but it should not, otherwise, cause a problem unless very high frequency operation is contemplated where it will contribute to overall device power dissipation, by becoming a significant portion of the total duty cycle.

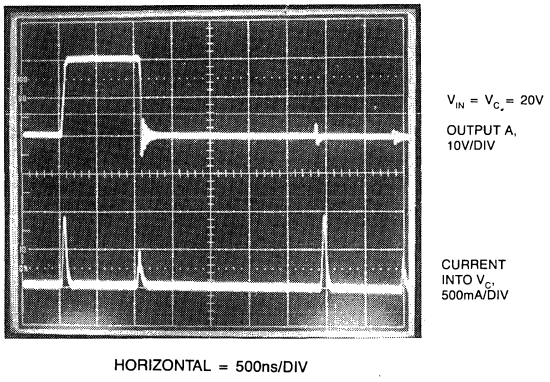

Figure 4. Current "spiking" on the V_C terminal caused by conduction overlap between source and sink is minimized by high-speed design techniques.

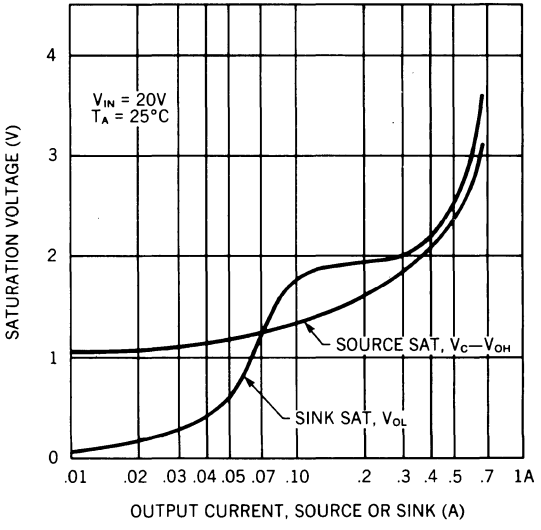

Figure 5. The ouput saturation characteristics of the UC1525A provide both high drive current and low hold-off voltage.

The output saturation characteristics of this stage are shown in *Figure 5.* The source transistor, Q_7, is a straight forward Darlington and its saturation voltage remains between 1 and 2V out to 400mA under the assumption that $V_{IN} \geq V_{CC}$. The sink transistor, Q_8, however, has a non-uniform characteristic which needs explanation. At low sink currents, the 1mA current source through Q_5 insures a very low saturation voltage at the output. As load current increases past 50mA, Q_8 begins to come out of saturation for lack of base drive but only up to about 2V. Here diode D_2 becomes forward biased shunting a portion of the load current through Q_5 to boost the base current into Q_8. With this circuit, the sink transistor can both support high peak discharge currents from a capacitive load, as well as insure the low static hold-off voltage required for bipolar transistors.

A typical output configuration for a push-pull, bipolar transistor power stage is shown in *Figure 6.* With a steady state base drive current from the UC1525A of 100mA, this stage should be able to switch 1 to 5A of transformer primary current, depending upon the choice of transistors. The sum of R_1 and R_2 determine the maximum steady state output current of the UC1525A while their ratio defines the voltage across C_2 which, at turn off, becomes the reverse V_{BE} for Q_1. With the values given, the output current and voltage waveforms are shown in *Figure 7* for a one microsecond pulse. If power FETs are used for the output switches as shown in *Figure 8,* the interfacing circuitry can become even simpler with only a small series gate resistor potentially required to damp spurious oscillations within the FET.

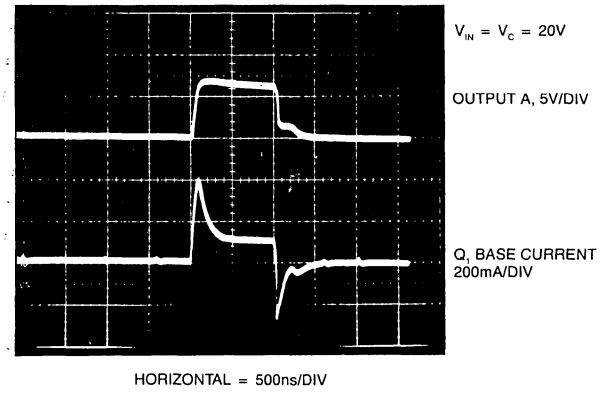

Figure 7. Base current waveforms (Figure 6 circuit) show the enhanced turn-on and turn-off current possible with the UC1525A.

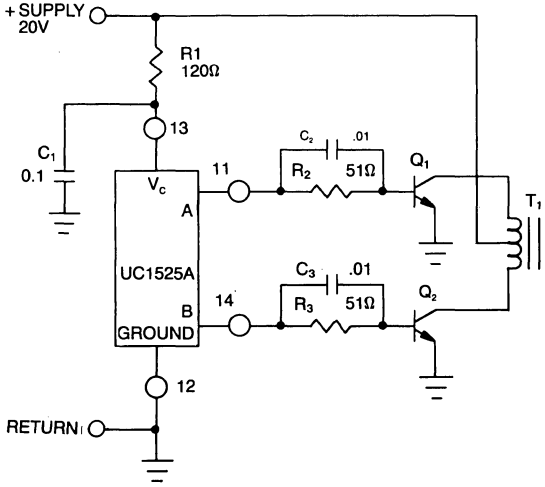

Figure 6. A typical push-pull converter power stage using external bipolar power transistor switches.

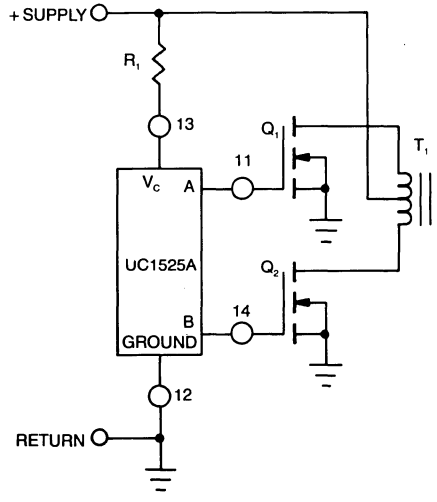

Figure 8. Replacing bipolar transistors with POWER MOSFETs provides even greater simplicity due to the low driving impedances of the UC1525A in each transition.

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Push-pull direct transformer drive is also particularly advantageous with UC1525A as shown in *Figure 9.* A version of this configuration is required for isolation when the control circuit is referenced to the secondary side of an off-line power system, and to provide level shifting of drive signals for ½ bridge and full bridge switching. The configuration of *Figure 9* has a couple of important advantages. First, by connecting the drive transformer primary directly between the outputs of the UC1525A, no center-tap is needed and the full primary is driven with opposite polarities. Secondly, between each output pulse, both outputs are pulled to ground which effectively shorts the two ends of the primary winding together coupling a low-impedance turn-off signal to the switching transistors.

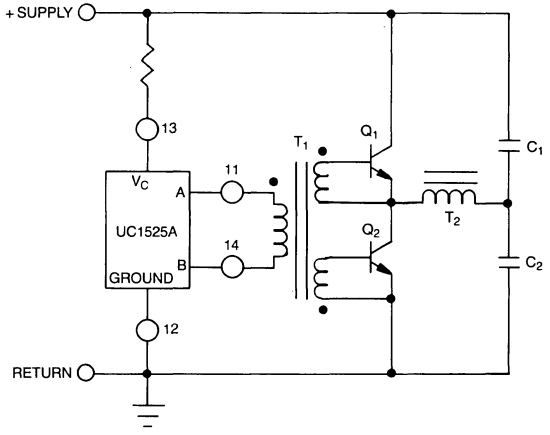

Figure 9. The UC1525A is ideally suited for driving a low-power base drive transformer and eliminates the need for a primary centertap.

A useful single-ended configuration, typical of buck regulators, is shown in *Figure 10.* Here the UC1525A outputs are grounded and the PWM signal is taken from the V_C terminal which switches close to ground during each clock period as the internal source transistors are alternately sequenced.

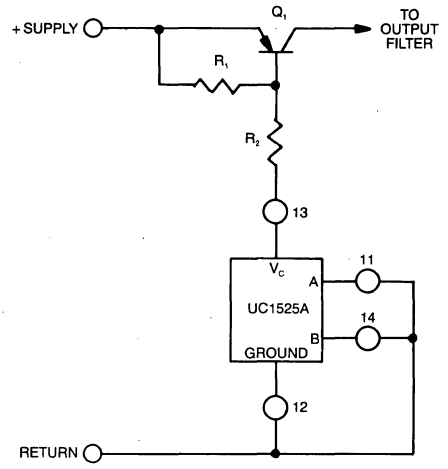

Figure 10. A single-ended, ground-referenced power stage for a flyback or boost regulator.

Controlling Power Supply Start-Up

Although the advantages of the UC1525A's output stage will often be reason enough for its selection, there are several other important and useful features incorporated within this product. One problem previously overlooked in PWM circuits is keeping the output under control as the supply voltage is turned on and off. Undefined states, particularly the possibility of turning on an output before the oscillator is running, can be quite awkward, if not catastrophic. To prevent this, the UC1525A has incorporated an under-voltage lockout circuit which effectively clamps the outputs to the off state with as little as 2½V of supply voltage which is less than the voltage required to turn the outputs on. This clamp is maintained until the supply reaches approximately 8V insuring that all the remaining UC1525A circuitry is fully operational prior to enabling the outputs. The clamp reactivates when the supply is lowered to approximately 7.5V. There is about 500mV of hysteresis built in to eliminate clamp oscillation at threshold.

Another important aspect of power sequencing is restraining the outputs from immediately commanding a 100% duty cycle when they are activated. This is accomplished by a slow turn on (soft-start) which is defined by an internal 50μA current source in conjunction with an externally applied capacitor. The details of this power sequencing system are shown in Figure 11.

Q_3 and Q_4 are the output gates normally driven by the oscillator through D_2 to provide output blanking between pulses. (One of these transistors is shown as Q_2 in Figure 3.) At low supply voltages, Q_2 conducts with base drive from the 20μA current source. Q_2 provides three functions. First, current through R_4 activates the output gates with minimum voltage drop. Second, current through R_5 activates the shutdown transistor Q_5 holding the soft-start capacitor, C_{SS}, discharged. Third, R_2 provides a small bucking voltage across R_3 for hysteresis at the switch point.

When the input voltage becomes high enough to provide a little more than one volt at the base of Q_1, that transistor turns on. This turns off Q_2, activating the outputs and allowing C_{SS} to begin to charge from the internal 50μA current source. The time to reach approximately 50% duty cycle will be

$$t = \left(\frac{2 \text{ volts}}{50\mu A} \right) Css$$

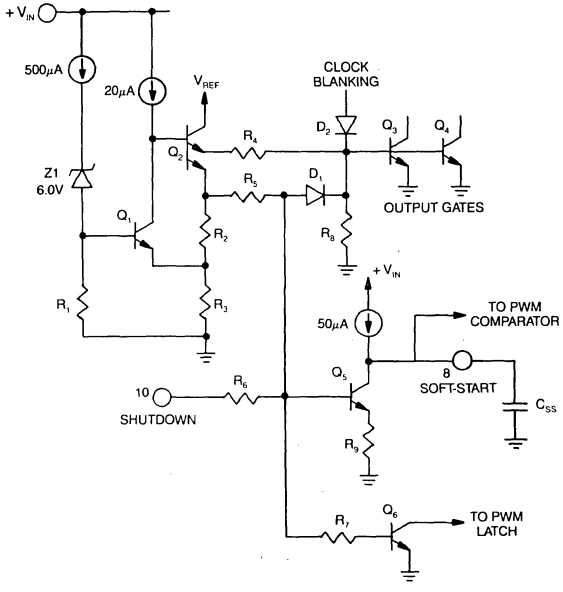

Figure 11. The internal power turn-on, soft-start, and shutdown circuitry of the UC1525A.

Power Supply Shutdown

An important part of any PWM controller is the ability to shut it down at any time for a variety of reasons, including system sequencing requirements or fault protection. Several options are available to the user of the UC1525A, which require an understanding of the capability of the shutdown terminal, pin 10. Referring to *Figure 11,* the base of Q_5 is turned on by a signal which is clamped to approximately 1.4V by the action of D_1 and the V_{BE} of gates Q_3 and Q_4. This holds the outputs off and keeps C_{SS} discharged by Q_5 which, with R9, becomes a 100μA net current sink.

If, during normal operation, pin 10 is pulled high, three things happen. First, the outputs are turned off within 200ns through D_1. Second, the PWM latch is set by Q_6 so that even if the signal at pin 10 were to disappear, the outputs would stay off for the duration of that period, being reset by the next clock pulse. Third, Q_5 is activated commencing a 100μA discharge of C_{SS}. However, if the activation pulse on pin 10 has a duration shorter than ⅓ of the clock period, the voltage on C_{SS} will remain high and soft-start will not be reactivated. Naturally, a fixed signal on pin 10 will eventually discharge C_{SS}, recycling soft-start. Thus, the shutdown pin provides both sequencing capability as well as a convenient port for protective functions, including pulse-by-pulse current limiting.

Regulating PWM Performance Improvements

The UC1525A also offers significant performance and application improvements in almost all of the additional basic functions of a PWM over those obtainable with earlier devices. A general description of these features is outlined below:

Reference Regulator: The output voltage of this regulator is internally trimmed to 5.1V ±1% during manufacture, eliminating the need for adjusting potentiomenters in most applications.

Error Amplifier: The UC1525A uses the same basic transconductance amplifier as the UC1524 with an important difference: it is powered by V_{IN} rather than V_{REF}. Now the input common-mode range includes V_{REF} eliminating the need for a voltage divider with its attendant tolerances. An additional feature relative to the error amplifier is that the shutdown circuitry feeds into a separate input to the PWM comparator allowing pulse termination without affecting the output of the error amplifier which might have a slow recovery, depending upon the external compensation network selected. An

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important benefit of a transconductance amplifier is the ease with which its current mode output can be over-ridden by other external controlling signals.

PWM Comparator: The significant benefit of the UC1525A's PWM comparator is in its following latch. A common problem with earlier devices was that any noise or ringing on the output of the error amplifier would affect multiple crossings of the oscillator ramp signal resulting in multiple pulsing at the comparator's output. The UC1525A's latch terminates the output pulse with the first signal from the comparator, insuring that there can be only a single pulse per period, removing all jitter or threshold oscillation from the system. Another important advantage of this latch is the ability to easily implement digital or pulse-by-pulse current limiting by merely momentarily activating the shutdown circuitry within the UC1525A. This could be as simple as connecting pin 10 to a ground-referenced current sensing resistor. For greater accuracy, some added gain may be advantageous. Once a current signal causes shutdown, the output will remain terminated for the duration of the period, even though the current signal is now gone. An oscillator clock signal resets the latch to start each period anew.

Oscillator: The functions of the oscillator within the UC1525A have been broadened in two important aspects. One is the addition of a synchronization terminal, pin 3, allowing much easier interfacing to an external clock signal or to synchronize multiple UC1525A's together. The other is the separation of the oscillator's discharge network from its charging current source for deadtime control. Reference should be made to the schematic of *Figure 12* for an understanding of the operation of this circuit. The heart of this oscillator is a double-threshold comparator, Q_7 and Q_8, which allows the timing capacitor to charge to an upper threshold by means of the current source defined by R_T and mirrored by Q_1 and Q_2. The comparator then switches to a lower threshold by turning on Q_{10} and discharges C_T through Q_3 and Q_4 with a rate defined by R_D. As long as C_T is discharging, the clock output is high, blanking the outputs. Since the overall oscillator frequency is defined by the sum of the charge and discharge times, there are three elements now in the frequency equation which is approximately:

$$f \approx \frac{1}{C_T\,(0.7R_T + 3R_D)}$$

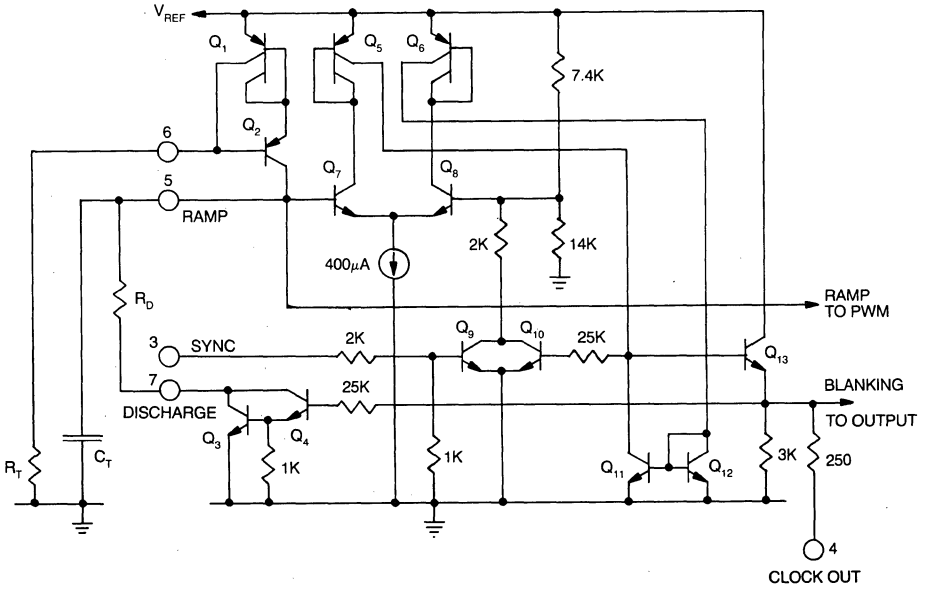

Figure 12. A simplified schematic of the UC1525A's oscillator circuitry.

External synchronization can easily be accomplished with a 2.8V positive pulse at pin 3. This will turn on Q_9, lowering the comparator threshold below wherever the voltage on C_T may happen to be. Two factors should be considered: First, the voltage on C_T determines the amplitude of the PWM ramp, and if the sync occurs too early, the loop gain will be higher and the resolution may be worse. Second, the sync circuit is regenerative within 200ns; and, while a wider pulse can be used, C_T will not begin to recharge as long as the sync pin is high. For synchronizing multiple UC1525A devices together, one need only to define a master with the correct R_TC_T time constant, connect its output pin to the slave sync pins, and set each slave R_TC_T for a time constant 10–20% longer than the master.

A 200 Watt, Off-Line, Forward Converter

The ease of interfacing the UC3525A into a practical power supply system can be illustrated by the off-line, power converter shown in *Figure 13.* This 200W supply places the control circuitry on the primary side of the power transformer where direct coupling can be used to drive the power switch. While simplifying the drive electronics, this configuration usually requires an isolated voltage feedback signal which is most easily accomplished by an optocoupler driven by some type of voltage regulator IC such as a SG723 or LM305. One other undefined block in *Figure 13* is the auxilliary power supply which suppplies the low voltage, low current bias supply for the UC1525A and the drive for Q_1, the power switch. The choice of the UFN443 POWER MOSFET

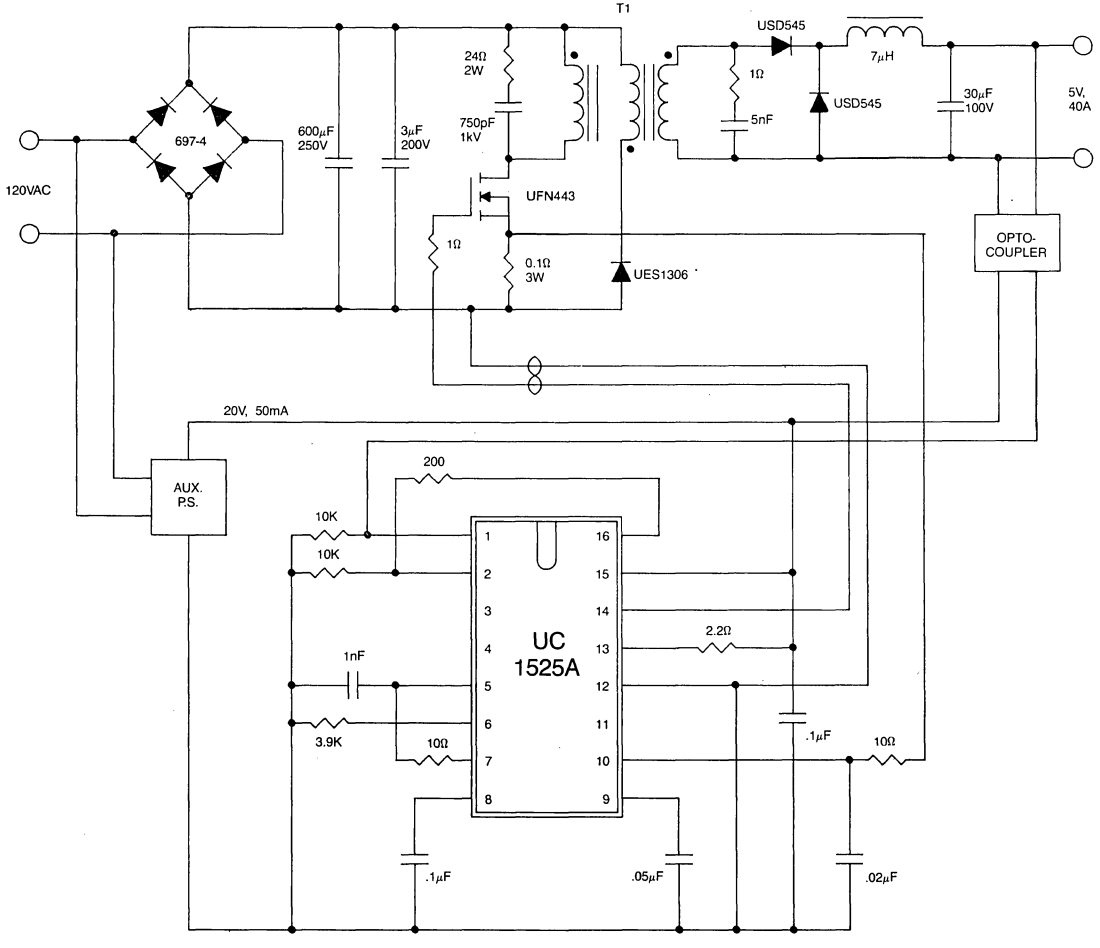

Figure 13. 200W, Off-Line Forward Converter.

for this switch keeps the total power requirements from the auxiliary supply at less than 1W; readily implemented with a small, line-driven transformer.

This converter is designed to operate at 150kHz which is accomplished by running the UC1525A at 300kHz and using only one of the outputs. This also automatically insures that the duty cycle can never be greater than 50%, a requirement of the power transformer in this configuration. The high operating frequency allows the output filter's roll-off to be set at 12kHz, greatly simplifying the overall loop stability considerations as adequate response can be achieved with only the single-pole compensation of the error amplifier provided by the .05μF capacitor on pin 9.

The totem-pole output of the UC1525A is used to advantage to drive Q_1 by providing a 400mA peak current to charge and discharge the MOSFET's gate capacitance while keeping overall power dissipation low. Waveform photographs of this operation are shown in *Figure 14.*

When operating at full load, the efficiency of this converter is 73% with by far the greatest power losses occurring in the output rectifiers—even though Schottky devices have been selected. Switching losses have been minimized by the fast current transitions, primarily defined by the leakage inductance of the transformer. Although this switching time could probably be even further reduced, there could be problems with current spikes during rise time due to Schottky rectifier capacitance.

Current limiting for this converter is provided by measuring the current in UFN443 with the 0.1Ω resistor in series with the source and using this voltage to activate the shutdown circuitry within the UC1525A. While this will provide a fast-acting short circuit protection on a pulse-by-pulse basis, a comparator may need to be added for a more accurate current limit threshold.

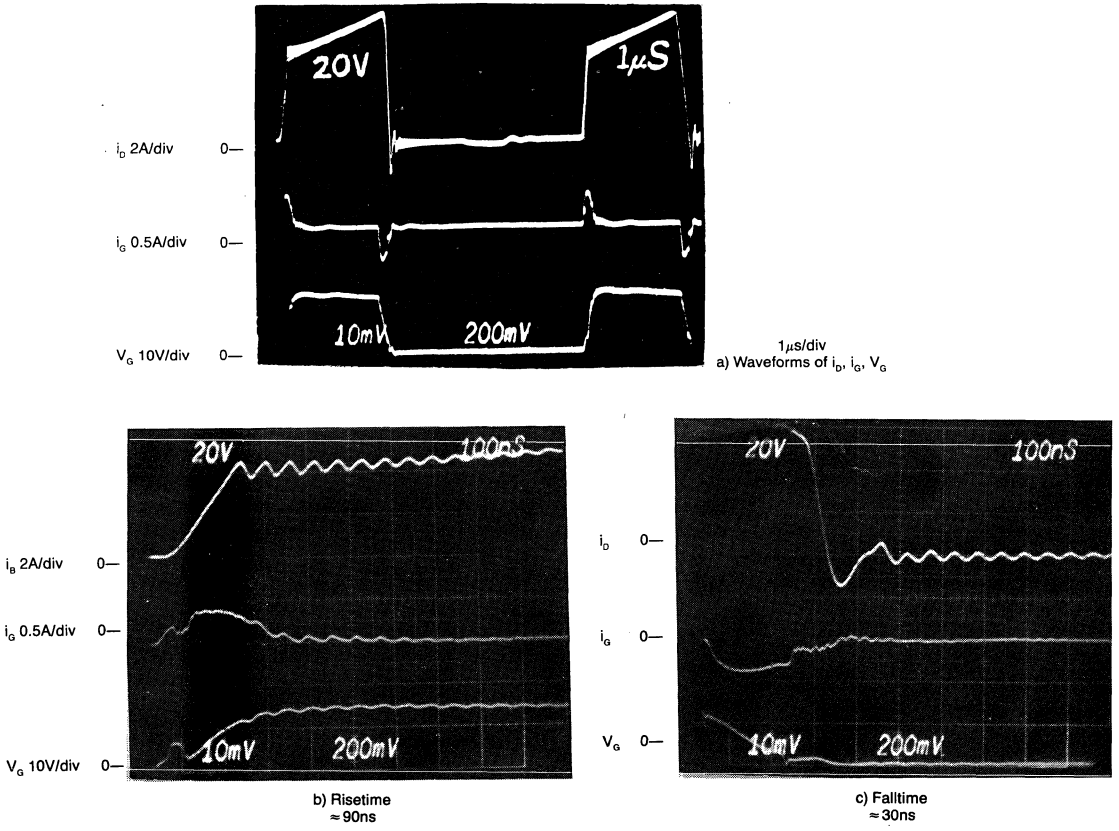

Figure 14. Current and voltage waveforms for the 200W, Off-Line Forward Converter with a UC1525A direct driven MOSFET Power switch. (Operating frequency is 150kHz with output current equal to 40A.)

Transformer Winding Data

500 Watt, 100kHz, Off-Line, Half-Bridge Converter

T1 Core: Ferrox 846T250-3C8
Pri: 14T #22AWG
Sec (2): 7T #22AWG

T2 Core: Ferrox EC52-3C8 (EE)
Pri: 14T, 2 layers, 2 #16 AWG in parallel
Sec (2): each 2T, C.T., copper strap .01″ × .8″

T3 Core: Ferrox 846T250-3C8
Pri: 1T
Sec: 20T, C.T. #22AWG

T4 117V/220V, 25V, 0.15A, 50-60Hz

L1 Core: Ferrox IF30-3C8
4 turns, 5 #12AWG in parallel

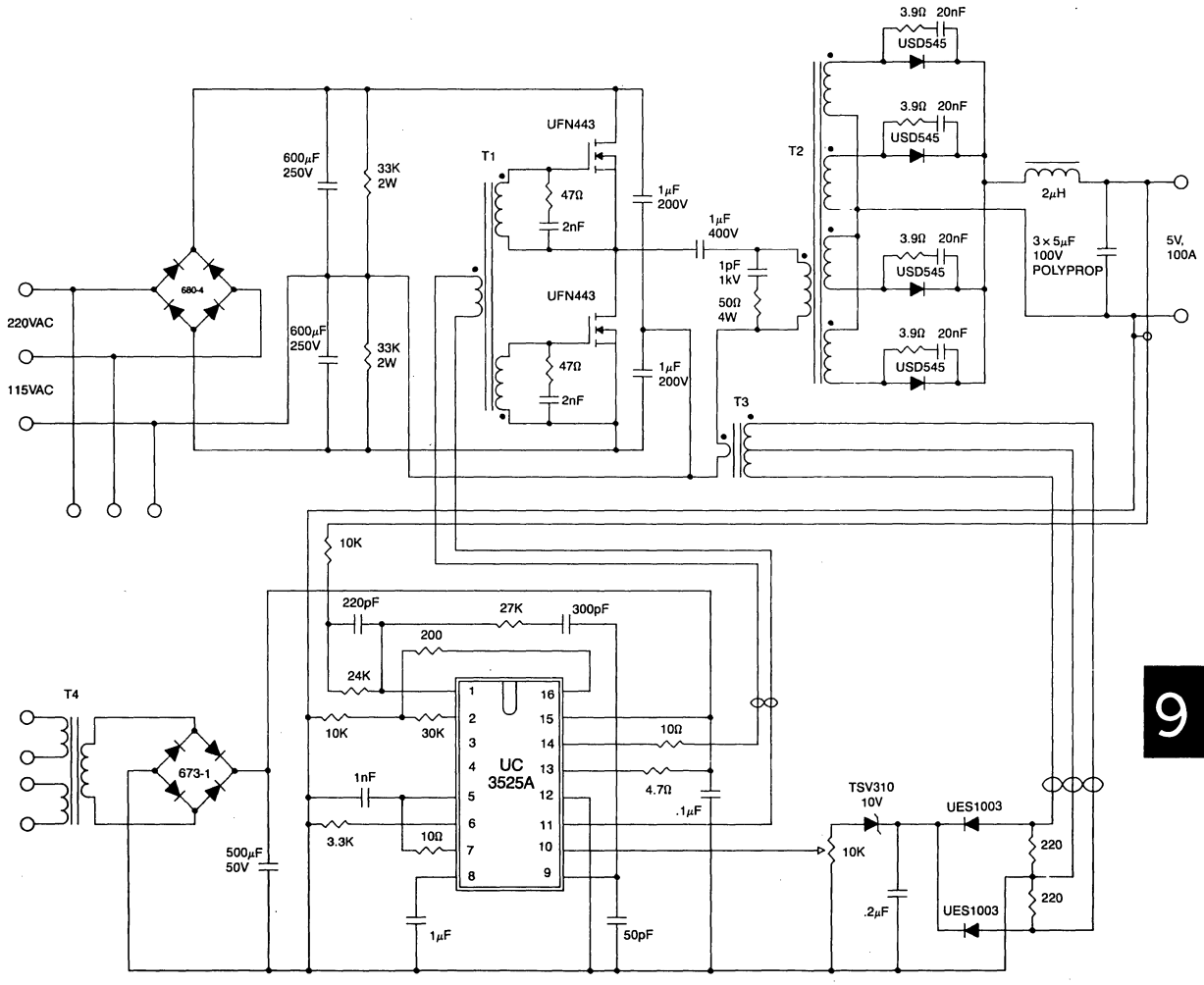

Figure 15. 500W, 100kHz Half-Bridge Schematic.

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500 Watt, Off-Line, Half-Bridge Converter

The circuit shown in *Figure 15* uses a pair of Unitrode UFN443 POWER MOSFETs in a half-bridge configuration with the UC1525A chip referenced to the secondary side of the power transformer. The MOSFET gates are driven directly from the control chip output through step down and isolation transformer T_1. The UC1525A output terminals (pins 11 and 14) provide active pull-up and pull-down (dual source/sink) for the primary of T_1. This provides the fast, high current turn-on and turn-off pulses needed for the MOSFET gates. In addition, the two ends of the primary windings are shorted to ground during deadtime, which prevents accidental turn-on by transients. Note that the current supplied by the UC1525A outputs drops to a small value when the gate capacitance has been charged or discharged to the desired gate voltage. Damping resistors with series blocking capacitors across the two secondaries of T_1 minimize ringing due to the MOSFET gate capacitance and the inductance of T_1 and lead inductance, particularly during deadtime.

Deadtime for the UC1525A is set very simply by a single resistor between pins 5 and 7. Only a small amount of deadtime is needed since the MOSFETS have no storage time and a very short delay time.

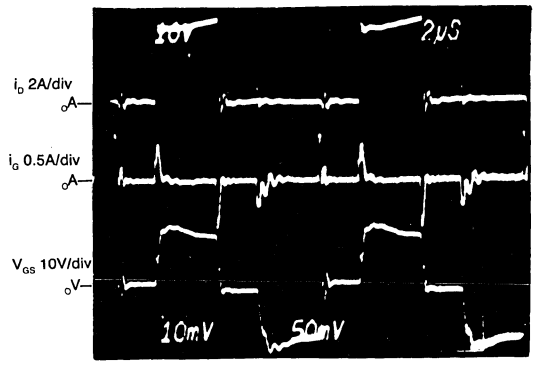
Slow turn-on is accomplished by a single capacitor at pin 8.

Current limiting is provided by current transformer T_3 in series with the primary of the power transformer T_2. The signal is rectified, threshold adjusted and sent to the shutdown terminal, pin 10, of the UC1525A.

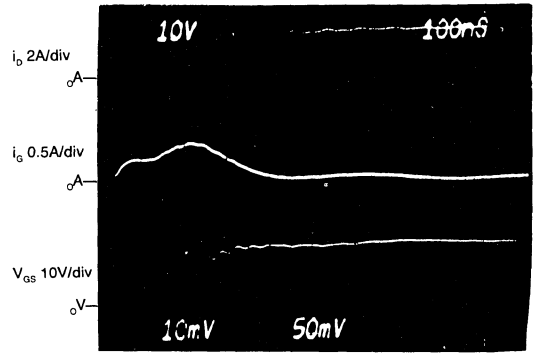
Waveforms of the converter are shown in the scope photos of *Figure 16.* Current rise and fall times are 20ns and 10ns. For additional details on this design, see Unitrode Application Note U-87, a 500W, 200kHz Off-Line Power Supply using POWER MOSFETS.

Improved Performance; Less Complexity

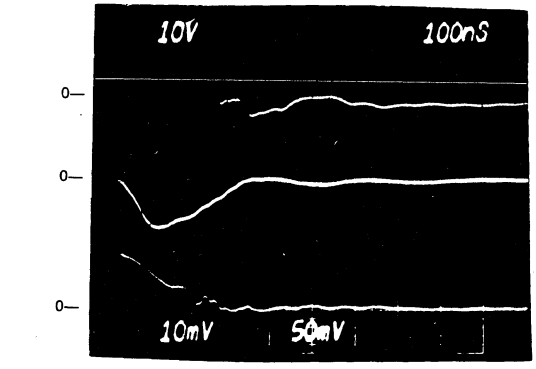
Although power supply designers for some time now have had an ever widening inventory of IC components available to ease their design tasks, the final measure of improvement has to be in terms of system performance versus cost. With fewer interface components to the power stages, freedom from potentiometer adjustments, protected start-up and shut-down, a built in soft-start network and several additional system-level features, the UC1525A provides a significant contribution to both performance and costs while simultaneously making the designer's task easier. With these accomplishments, it is clear that this device truly does represent a step-function improvement, introducing a second-generation of power control components.



2μs/div
a) Waveforms of i_D, i_G, V_G



100ns/div
b) Risetime



100ns/div
c) Falltime

Figure 16. Performance waveforms for the Half-Bridge, 500W, 100kHz Converter with output current of 80A.

THE UC1524A INTEGRATED PWM CONTROL CIRCUIT PROVIDES NEW PERFORMANCE LEVELS FOR AN OLD STANDARD

Introduction

The application of IC technology to the switching power supply really began with the introduction of the SG1524 in 1976. This device was the first IC to implement all the control blocks necessary for a wide range of PWM power systems. Its straight-forward approach to the classic PWM architecture gave it wide acceptance, and it has become the most commonly used IC controller today.

Even though the 1524 has gained great acceptance and engineers have praised its versatile and easy to understand architecture, they have many times cursed the simplistic, or idealistic, ways its individual blocks were implemented. While one would assume, at first glance, that all control functions necessary for most power supply applications are contained within the 1524, in the real world of practical power systems, additional circuitry is required to interface with the rest of the system, to protect against different types of fault conditions, to adjust for inaccuracies, or to improve control during power sequencing.

Although in the intervening years, many new IC control chips have been introduced which offer certain specialized advantages, it was found that design engineers still preferred the 1524 for its wide versatility and generalized architecture. From this understanding, it became apparent that a new design, which would improve many of the 1524's individual functions by making them more predictable and easier to apply, while retaining the same architecture, could be a winner. Thus, Unitrode undertook this task. The result is the UC1524A.

The UC1524A PWM Controller

A design goal set for the UC1524A was that it not only retain the same architecture but keep the same pin configuration as the 1524 and function equal to or better than the 1524 in most existing applications. In

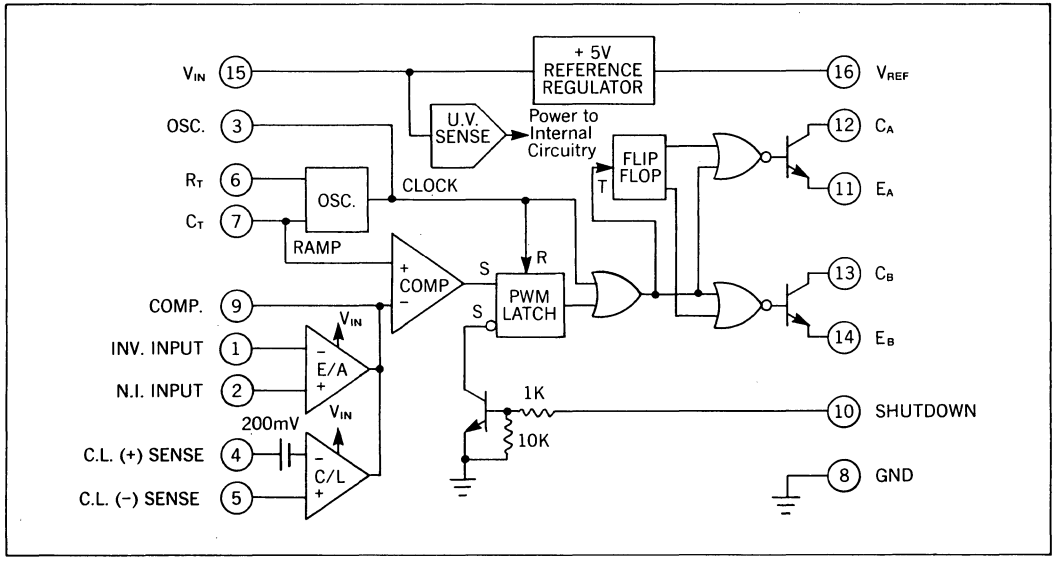


FIGURE 1 — The UC1524A Block Diagram Follows the Same Architecture As the UC1524 But With Several Significant Differences.

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this way, engineers who were familiar with the 1524 could easily understand and evaluate the UC1524A. Performance improvements had to be significant, particularly in reducing the need for discrete support circuitry, so there would be a cost advantage in using the UC1524A in new designs. The block diagram of the UC1524A is shown in Figure 1 which, by intent, appears very similar to that of the older 1524.

The list of the improvements, however, is considerable and includes the following:

1. The 5V reference is now internally trimmed to ±1% accuracy, eliminating the need for potentiometer adjustments.
2. The error amplifier's input range now extends beyond 5V, eliminating the need for a pair of dividers and their attendant tolerances.
3. A high-gain, wide-band, current sense amplifier has been included which is useful for either linear or pulse-by-pulse current limiting in the ground or power supply output lines.
4. An under-voltage lockout circuit has been added which disables all the internal circuitry except the reference until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifying the design of low-power, off-line converters. There is approximately 600mV of hysteresis included for jitter-free activation.
5. A PWM latch has been added insuring freedom from multiple pulsing within a period, even in noisy environments. In addition, the shutdown circuit feeds directly to this latch which will disable the outputs within 200ns of activation.
6. The oscillator circuit is usable to frequencies beyond 500kHz and is easier to synchronize with an external clock pulse.
7. The power capability of the output switches has been boosted by doubling the current capability to 200mA and increasing the voltage rating to 60V.

An understanding of some of these improvements is necessary for ease in application and will now be discussed in greater detail.

Internal Power Turn-on Circuit

The under-voltage lockout and turn-on hysteresis circuit is shown in Figure 2. This circuit requires approximately 2V for activation; but, since nothing else will turn on without at least 3V of supply voltage, lockout is assured. When V_{IN} rises above 2V, R_2 begins to

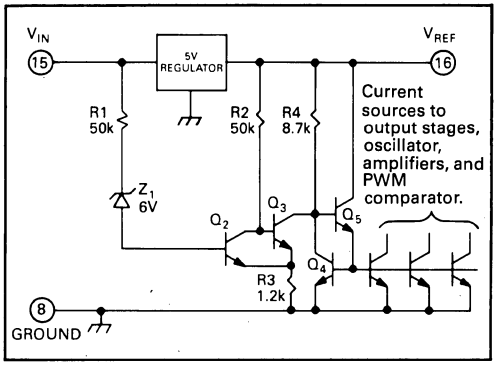

FIGURE 2 — The Under-Voltage Lockout and Power Turn-On Circuitry within the UC1524A.

conduct saturating Q_3 and holding the base of Q_5 too low to allow any of the current sources to conduct. The current through R_4 flows through Q_3 and R_3, developing a 600mV drop across R_3 when V_{REF} reaches 5V. At this level, the only current flowing is that used by the reference regulator and R_2 and R_4, a total of approximately 2.5mA at turn-on threshold.

When the input voltage reaches approximately 8V, diode, Z_1 begins to conduct turning on Q_2 which turns off Q_3 and allows the current sources to activate. Since the current through Q_2 is much less than through Q_3, the voltage across R_3 drops, providing positive feed-

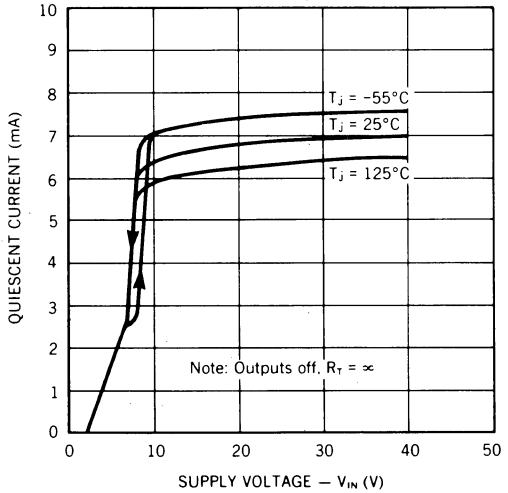

FIGURE 3 — Supply Current for the UC1524A vs. Input Voltage.

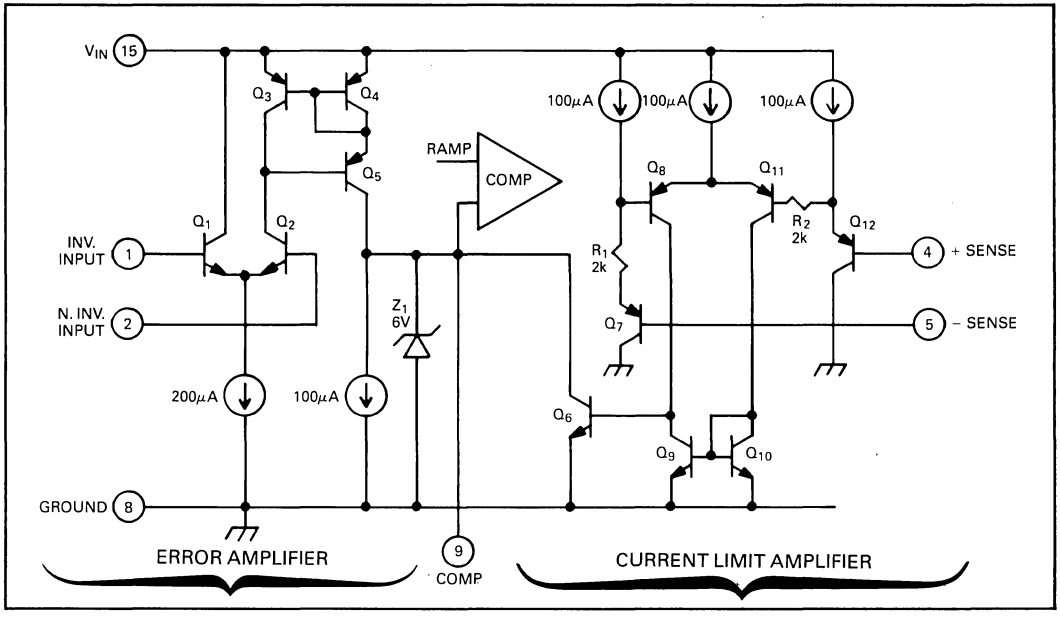

FIGURE 4 — Voltage and Current Sensing Amplifiers Have a Common Output at the Input to the PWM Comparator.

back. This gives about 600mV of hysteresis. This circuit, of course, works in reverse at turn off, insuring that the outputs can only operate when the supply is adequate for fully predictable operation. Figure 3 shows the relationship between quiescent current and input voltage. Designers should find this low current start-up characteristic quite advantageous for off-line, primary-side control with boot-strapped operation after turn on.

A New Current Limit Amplifier

Since the outputs of the current limit amplifier and the voltage-sensing error amplifier are summed at the PWM comparator input, they should be examined together as shown in Figure 4.

Since the error amplifier, consisting of transistors Q_1 through Q_5, must have the lowest priority in controlling the PWM, its output must be easily overruled by current faults or other programming functions, such as soft-start, which would hold pin 9 low. Therefore, a transconductance amplifier similar to that used in the earlier 1524 was again applied to the 1524A with one exception: it is now powered by V_{IN} instead of V_{REF}, so that the input common-mode range extends to within 2V of either rail. Zener diode, Z_1, is used on the output to keep the input level to the PWM comparator below 6 volts.

The error amplifier's output can be considered a 100μA current source or sink (0 - 200μA source with 100μA constant sink). When the current limit circuit activates, Q_6 turns on and can easily pull down pin 9 even though the error amplifier would nominally be calling for a high output at this point.

The current limit circuit consists of Q_6 through Q_{12}. Its differential PNP input stage gives it a common mode range extending from 300mV below ground to within −2V of V_{IN}. Its threshold, or offset, of 200mV is established by the 100μA current source through R_1, with R_2 added to null out the effect of any base current from Q_8.

This current sensing block within the UC1524A can actually be used either as a linear amplifier or as a comparator. The open loop small-signal gain is approximately 80dB while its transition delay with 10% overdrive is 600ns. This can be decreased substantially with additional overdrive. Use of the current sensing block as a comparator is usually preferred from a systems standpoint, since it does not have to be compensated and pin 9 can be dedicated solely to

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error amplifier compensation. Under this condition, a current signal over the threshold level will pull pin 9 low, terminating the output signal. Recovery is determined by the 100μA pull-up current from the error amplifier in conjunction with any capacitance which may be present on pin 9.

When the current limit circuit is used as a linear amplifier, stabilization is performed by feedback to the inverting input (pin 4) or by capacitance from pin 9 to ground as shown in Figure 5.

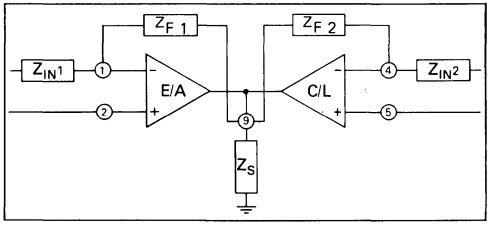

FIGURE 5 — Various Compensation Options Which Are Possible When Both Amplifiers Are Operated in the Linear Mode.

An additional feature of this circuit is its capability to perform as a duty-cycle limiting circuit in the configuration shown in Figure 6. If R_1 is made 100k, there will be minimal effect upon the error amplifier gain.

In current limiting, to achieve the fastest responding pulse-by-pulse control, consideration should be given to the use of the shutdown terminal on pin 10. While the input threshold of this circuit is not as accurately controlled as the current limit amplifier and has a negative temperature coefficient of −2mV/°C and is internally ground referenced; it does feed directly into the PWM latch with only 200ns delay from activation of pin 10 to shutdown of the outputs.

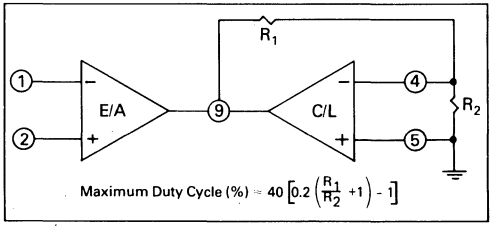

FIGURE 6 — The Fixed 200mV Threshold of the Current Limit Amplifier Can Be Multiplied to Form a Duty-Cycle Clamp or Dead-Band Control.

PWM Comparator and Latch

The PWM latch insures only a single pulse is allowed to reach the appropriate output stage within each period. The latch is reset with the oscillator clock pulse which also serves to blank the outputs. Thus, although the latch is reset at the start of the oscillator clock pulse, it is the termination of the clock pulse which initiates output conduction. The output then stays on until the latch is set, either by a signal from the PWM comparator or from a shutdown command from pin 10. Once the latch is set, it will hold the output off for the duration of the period.

There are several significant advantages to this circuit. First, the latch completely eliminates multiple outputs of the PWM comparator because of noise or ringing on the output of the error amplifier causing multiple crossings of the ramp signal. Second, current limiting can now be performed much more rapidly without instability. Without a latch, significant integration is needed to maintain a turn-off signal after the outputs have turned off. Finally, any instabilities which might potentially be present in the voltage or current loops, or the shutdown signal from pin 10, will cause much less stress on the output stages, since only two transitions through the high-dissipation active region can be made during each period.

The performance of this portion of the UC1524A can be evaluated using a triggerable pulse generator with a variable delay, set up as shown in Figure 7. R_T and C_T are selected for the desired operating frequency. The clock triggers the pulse generator, and the delay is adjusted so the generator output occurs during the PWM period. The output pulse width must be at least 200ns and the amplitude higher than the threshold of the UC1524A input being evaluated. Typical waveform photographs are shown in Figure 8.

Higher Power Output Switches

With the higher current and voltage rating of the UC1524A's output switches, significant economies can now be achieved in interfacing with higher power devices. For low power requirements, a broader range of applications may now be served by the 1524A itself without additional discrete output devices. Regardless of the power supply requirements, more current and voltage from the UC1524A will ease the design tradeoffs. Even with higher current and voltage, the UC1524A offers fast response time. Each output stage contains an anti-saturation network to keep the output transistors out of hard saturation. Although this adds

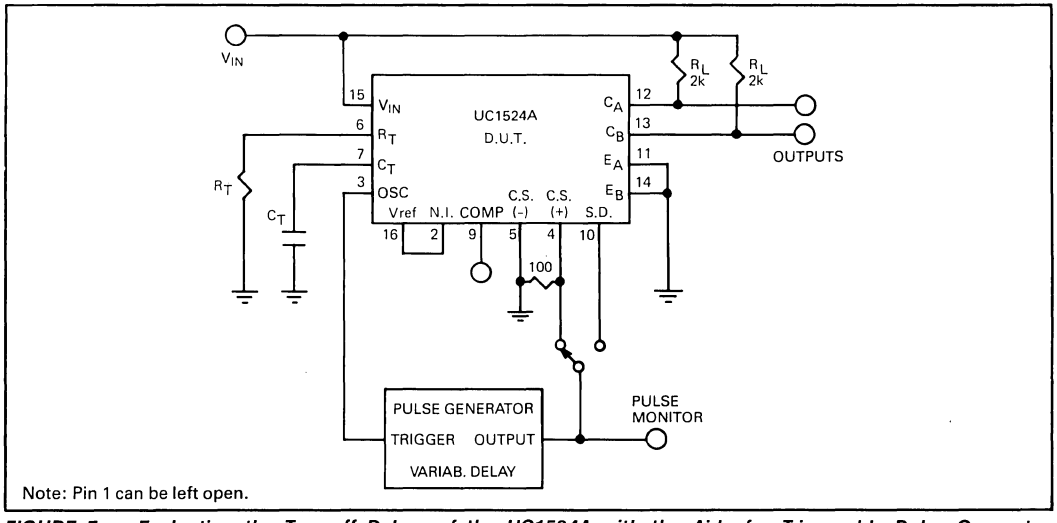

FIGURE 7 — Evaluating the Turn-off Delays of the UC1524A with the Aid of a Triggerable Pulse Generator With Variable Delay.

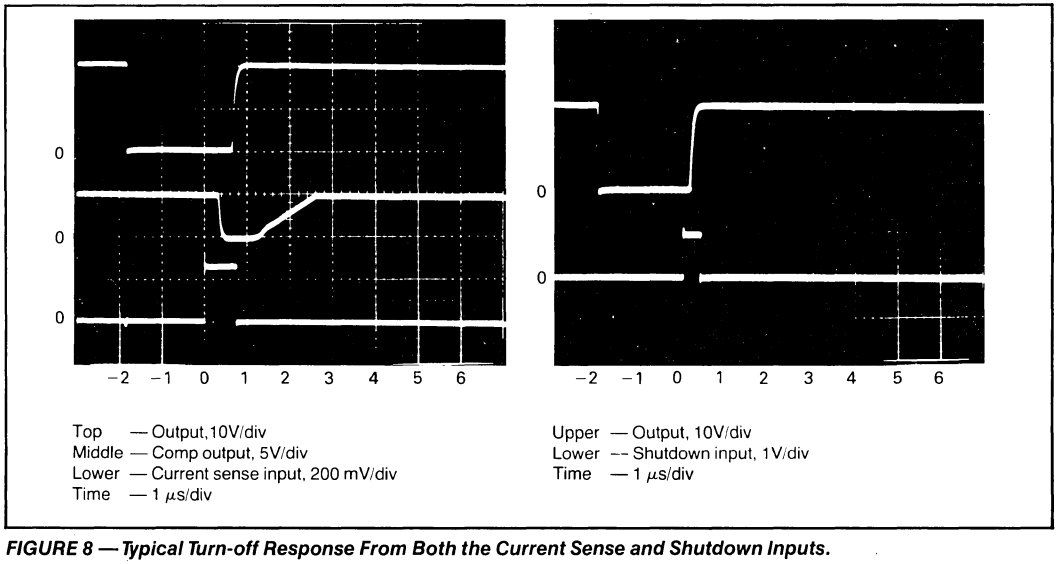

FIGURE 8 — Typical Turn-off Response From Both the Current Sense and Shutdown Inputs.

somewhat to the saturation voltage, it is more than offset by the benefits in reducing turn-off delay. Saturation voltage as a function of current is shown in Figure 9.

Since both collectors and emitters are available on the UC1524A's output transistors, many different coupling possibilities are offered. One useful configuration for enhanced turn-off is shown in Figure 10. The fast-rising signal appearing at the collector of the output transistor, Q_1, is capacitively coupled to saturate an external transistor, Q_2, greatly reducing the turn-off delay of Q_3 and allowing a much larger value to be selected for R_3. Many variations of this circuit are possible depending upon the power devices to be driven and the voltage levels required.

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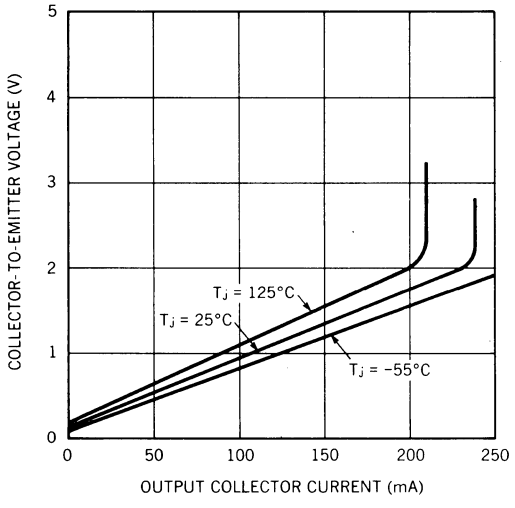

FIGURE 9 — Output Saturation Characteristics for Each of the UC1524A's Outputs.

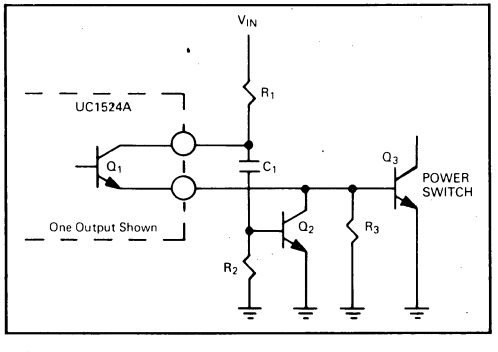

FIGURE 10 — The addition of C_1 and Q_2 Uses the Collector Signal of the UC1524A to Generate an Enhanced Turn-off Command for Q_3

Frequency Synchronization

The oscillator circuit within the UC1524A, shown in Figure 11, has been improved over that of the 1524 with the addition of C_2. Without this component, a synchronizing pulse externally applied to pin 3 had to do all the work of discharging the timing capacitor through Q_4 and Q_5. The simple addition of C_2 couples a positive pulse from pin 3 to the base of Q_{10}, momentarily reducing the threshold of comparator Q_8-Q_9 and regeneratively triggering the oscillator into its discharge state. The circuit is now leading-edge triggered and narrow pulses can be used. This is a consideration when minimum dead time is required, since the outputs are blanked off as long as pin 3 is held high.

As with the 1524, synchronization to an external clock should be done with the R_TC_T time constant set approximately 10 to 20% greater than that determined for the required clock frequency, taking into consideration the expected tolerances of the components. For synchronizing multiple UC1524A devices, all R_T, C_T, and OSC output terminals should be individually connected together and a single R_T and C_T used.

When considering blanking, the pulse on pin 3 may be extended somewhat by the addition of a capacitor of up to 100pF from pin 3 to ground. If narrower blanking pulses are required, adding a resistive load from pin 3 to ground of 1 kohm minimum will reduce the pulse width.

The best way to guarantee a large dead time is still to use a diode to clamp the peak output from the error amplifier to a divider from V_{REF}. This technique is quite accurate due to the accuracy of V_{REF} and the 100μA fixed current available from the amplifier.

A Simple Buck Regulator Circuit

The application of Figure 12 demonstrates the utility of the UC1524A used with a Unitrode PIC600 hybrid switch. This combination greatly simplifies the design of switching regulators, since the only other active device required is a small-signal 2N2222 which serves to provide a constant drive current to the output switch, regardless of the input voltage level. With the UC1524A, current sensing does not have to be done in the ground line, but will still function when the regulator output is shorted to ground.

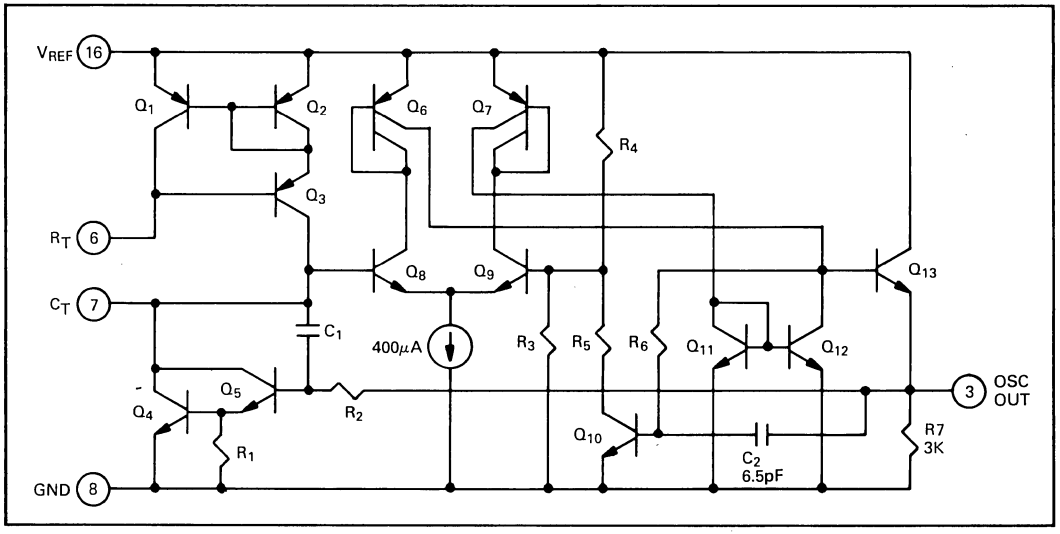

FIGURE 11 — The Oscillator Circuit of the UC1524A Allows Both High Frequency Operation and Ease of External Synchronization.

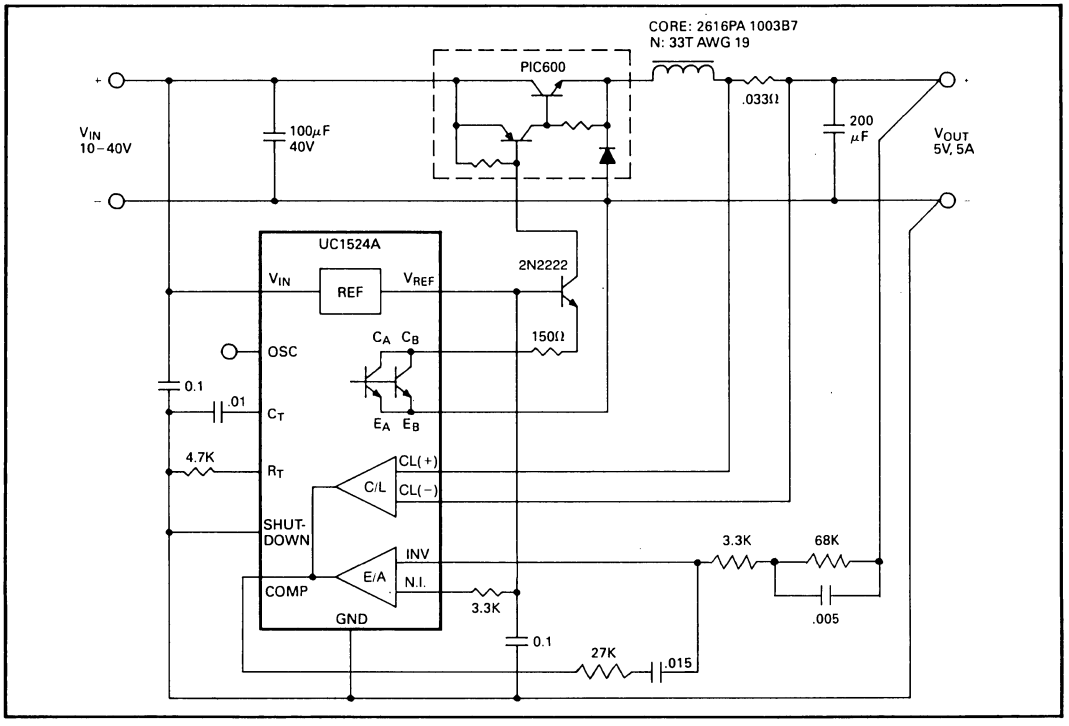

FIGURE 12 — The UC1524A Combines With the PIC 600 Hybrid Switch to Form A Simple But Powerful Buck Regulator.

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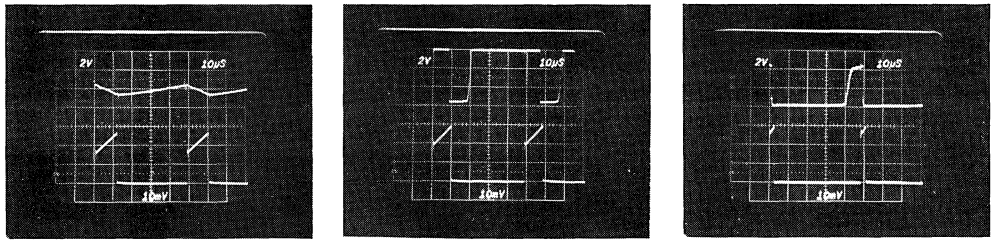
The waveforms of Figure 13 demonstrate the performance of the current limiting comparator, showing that from the onset of current limiting to a complete short circuit, the peak input current increases from 5.2A to only 5.9A.

A Complete DC-DC Converter with the UC1524A

An important attribute of the new UC1524A family is the higher voltage rating on the output transistors. This now makes it possible to implement a practical 4W DC-DC converter operating from a common 28V bus with no additional output transistors. The schematic of Figure 14 uses a push-pull configuration which imposes a voltage of twice the supply across the "OFF" transistor. This is now within the rating of the UC1524A and, thus, with a 28:7 turns ratio in the transformer, a 5V, ¾A output is achieved with 78% efficiency at a significant minimum parts count.

The fast response of the current limit amplifier within the UC1524A again keeps the device well protected as shown in the waveforms of Figure 15.



A B C

Upper trace is Comp terminal (pin 9), 2 V/div
Lower trace is input current through power switch, 0.2A/div
Time base is 10 μsec/div.

A = Onset of current limiting, I_p = 5.2A
B = Into current limiting, Comp terminal held low until inductor current falls below threshold, Ip = 5.9A
C = Output shorted to ground. Pulse width reduced to 2μs. Ip still 5.9A.

FIGURE 13 — Performance Data for Figure 13's Regulator Shows the Tight Control of Peak Current, Even Under Shorted Output Conditions.

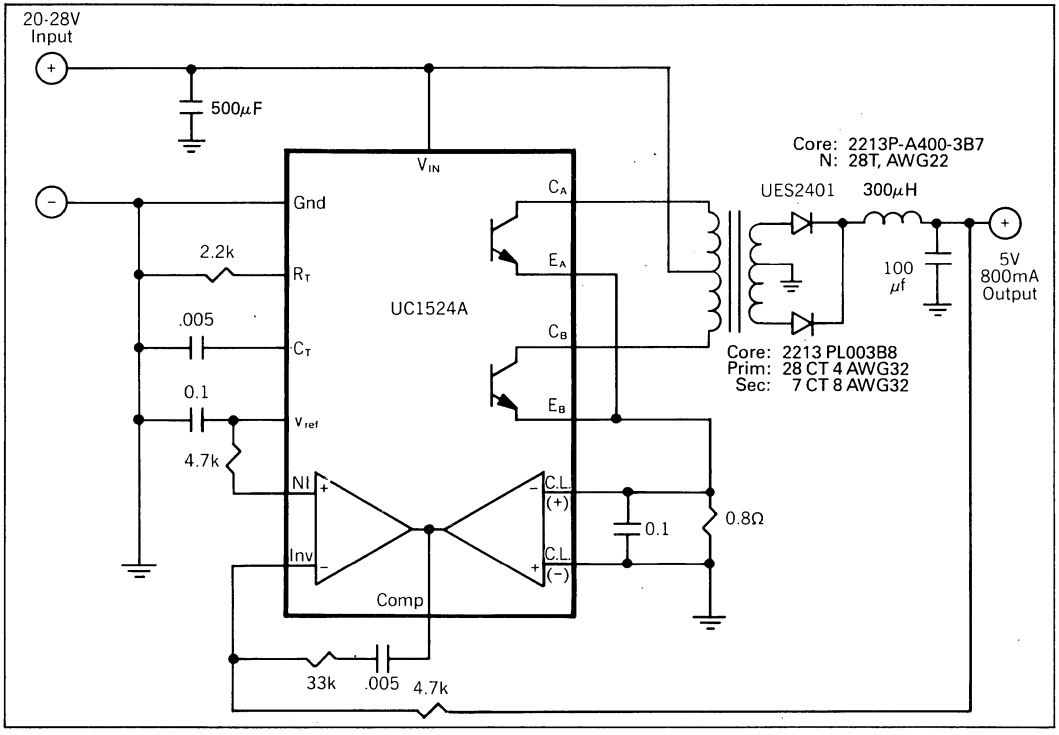


FIGURE 14 — With Higher Output Voltage Capability, the UC1524A can Implement a Complete 4 Watt DC to DC Converter with no Additional Switching Transistors.

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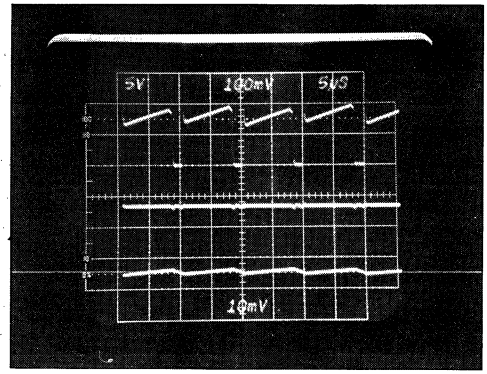
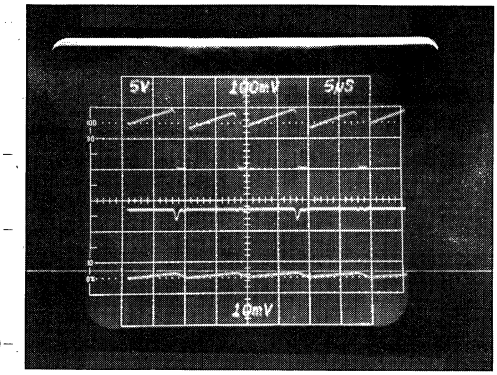
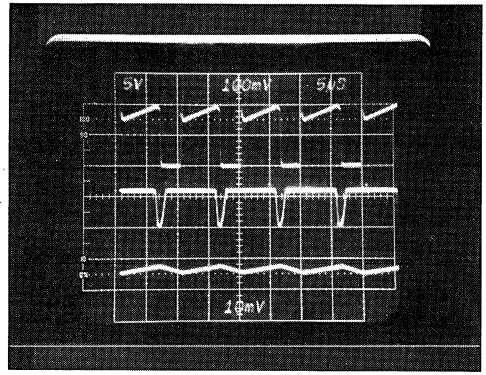


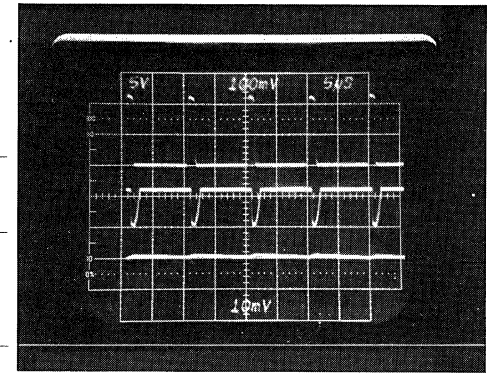
Circuit Under Normal Load



Circuit at Threshold of Current Limiting



Circuit Under Full Current Limit



Circuit Under Short Circuit Conditions

FIGURE 15 — Operating waveforms for the PWM DC-DC converter (Figure 14)
Upper trace = Primary current at 0.1 A/division
Middle trace = Pin 9 voltage at 5V/division
Lower trace = Load current at 0.5A/division
Time base = 5 µs/division

An Off-line Forward Converter

For low to medium power applications, a single-ended flyback or forward converter with all the control on the primary side of the isolation step-down transformer is usually the most economical solution. However there are two complications with this approach. The first is that although the control circuitry can easily be driven from a low-voltage winding on the power transformer, starting energy must be taken from the high-voltage rectified line where, at 170VDC, every 10mA represents a 1.7W loss. The second complication is in obtaining adequate regulation of the output while still meeting isolation requirements from output back to the line.

The 50W forward converter of Figure 16 offers innovative solutions to both these problems. In this circuit, the UC1524A provides all the control with its operating drive power coming from winding N_2. The low-current start-up characteristics of the UC1524A allow starting energy to be developed in C_2 with only approximately 8mA required through R_1.

The problem of isolated feedback control is solved in this application by sampling the 5V output level at the switching frequency by means of the 2N2222 transistor and transformer T_2. With every switching cycle, the output voltage is transferred from N_1 to N_2 where it is peak detected to generate a primary-referenced signal to drive the PWM error amplifier. Diode D_2 is used to temperature compensate for the loss in the rectifier, D_1 and the net result is better than 1% regulation with the main added cost that of a very inexpensive signal transformer.

Some of the other features of this application include a duty-cycle clamp on the PWM formed by diode D_3

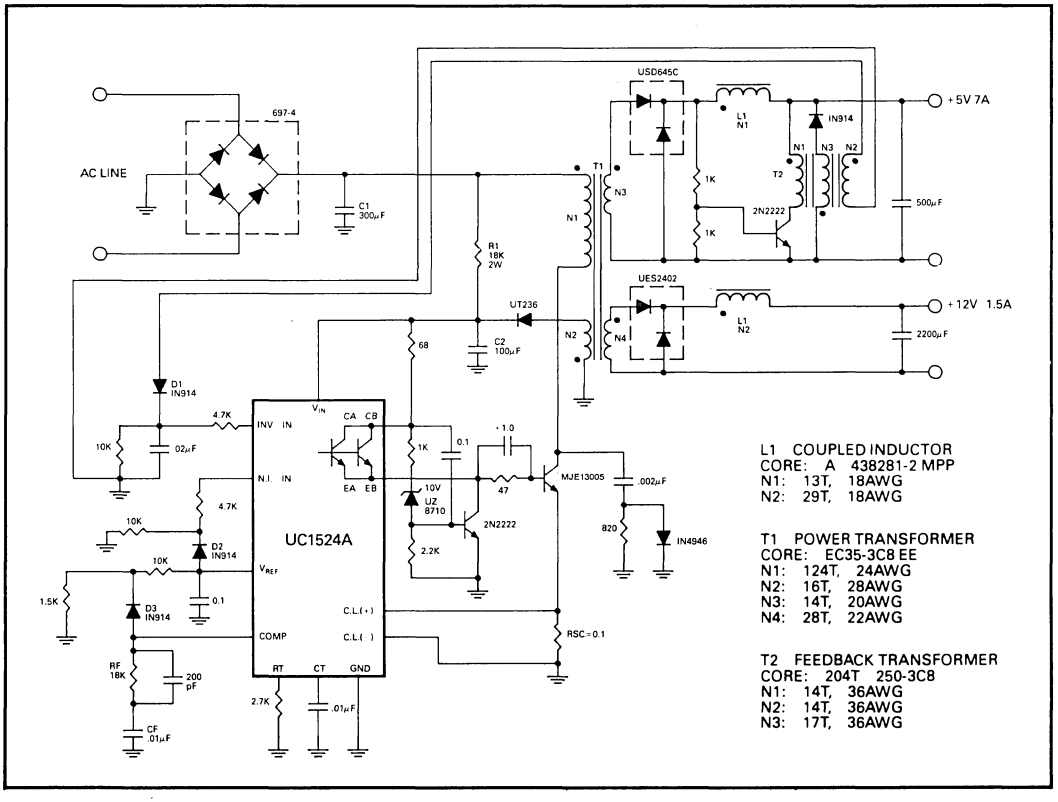


FIGURE 16 —This 50W Off-Line Forward Converter Features Both High Efficiency and Good Regulation while Maintaining Input-Output Isolation.

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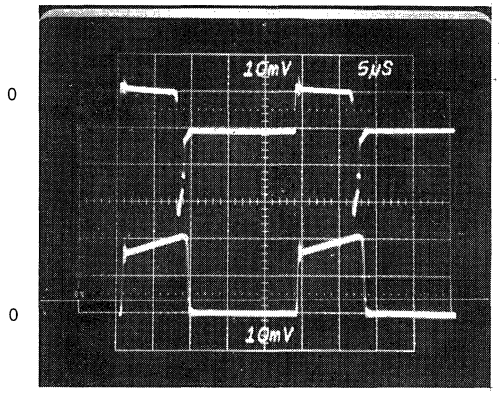
and the 10k - 1.5k divider from V_{REF}. This method of clamping is more effective with the UC1524A since the UV lockout keeps the outputs off until the reference, error amplifier, and oscillator are all operating within specification.

Drive for the UMT13005 high-voltage switch is accomplished by using the emitters of the UC1524A's output transistors for turn-on and the 2N2222 in conjunction with the 1μfd base capacitor to provide a negative base voltage for rapid turn-off as described in Figure 10.

The resultant drive signal is shown in Figure 17. Operating at 40kHz, this regulator provides an isolated 50W of power with an efficiency of 83%, a high degree of regulation, and fast overload protection.

Conclusion

Although there are now many new integrated circuits from which to choose in attempting to build more cost-effective power supplies, it always helps to review well established ideas. In the case of the UC1524A, updating and improving an earlier product has resulted in a significant advancement: providing greater performance and versatility while reducing system costs.



at Full Load (50W)

FIGURE 17 — Base Current (Upper Trace) and Collector Current for the UMT 13005 of Figure 16. The Time Base is 5μs per Division.

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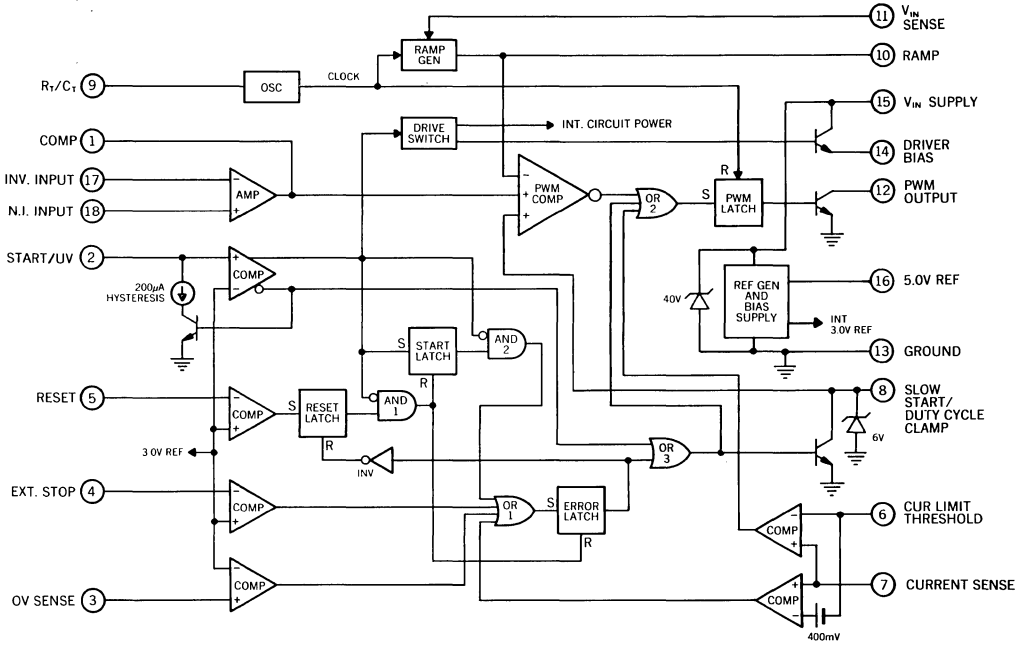
APPLYING THE UC1840 TO PROVIDE TOTAL CONTROL FOR LOW COST, PRIMARY REFERENCED SWITCHING POWER SYSTEMS

1. Introduction

There are many potential approaches to be considered in switch mode power supply design; however, the contradictory requirements of minimum cost and compatibility with ever more demanding line isolation specifications make primary control very attractive. Application of the UC1840 as a primary-side, off-line controller presents an extremely cost-effective approach to supplying isolated power from a widely varying input line while maintaining a high degree of efficiency.

Primary control means referencing all of the control electronics along with the power switching device on the input line side of an isolation transformer. An obvious advantage to this approach is the simplified interface between the control and power switch. This eliminates many of the transitions across the isolation boundary which significantly increase the cost of the magnetics portion of the power supply's budget.

There are two disadvantages to primary control: (1) operating or at least starting, the control electronics from the line voltage (typically 300 VDC), and (2) providing adequate regulation (which requires feedback from the secondary across the isolation boundary). The capability of the UC1840 Control IC to solve these problems while providing all of the regulating, sequencing, monitoring, and protection functions referenced to the primary side, makes this device very attractive.



Note: Positive true logic, latch outputs high with set, reset has priority.

FIGURE 1. THE OVERALL BLOCK DIAGRAM OF THE UC1840, AN INTEGRATED CIRCUIT OPTIMIZED FOR PRIMARY-SIDE CONTROL OF OFF-LINE SWITCHING POWER SUPPLIES.

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2. The UC1840 Controller

The overall block diagram of the UC1840, shown in Figure 1, includes the following features:

(1) Fixed-frequency operation set by user-selected components

(2) A variable-slope ramp generator for constant volt-second operation providing open-loop line regulation and minimizing, or in some cases even eliminating, the need for feedback control

(3) A drive switch for low current start-up off the high-voltage line

(4) A precision reference generator with internal over-voltage protection

(5) Complete under-voltage, over-voltage, and over-current protection including programmable shutdown and restart

(6) A high-current, single-ended PWM output optimized for fast turn-off of an external power switch

(7) Logic control for pulse-commandable or DC power sequencing

For an understanding of how these individual blocks work together in a typical, medium-power, flyback power supply, reference should be made to Figure 2 and the functional description which follows.

3. UC1840 Functional Description

3.1 Power Sequencing

A simplified schematic of the UC1840's internal power turn-on circuitry is shown in Figure 3. The key elements of this function are: (1) the Driver Bias Switch, Q3, which keeps the loading on the control voltage line, Vc, to a minimum during start up; (2) the Under-voltage Comparator which also functions as a Start Threshold Detector with programmable hysteresis; and (3) an auxiliary, primary-referenced, low-voltage winding on the main power transformer which provides normal control power after turn-on. The sequence of events is as follows:

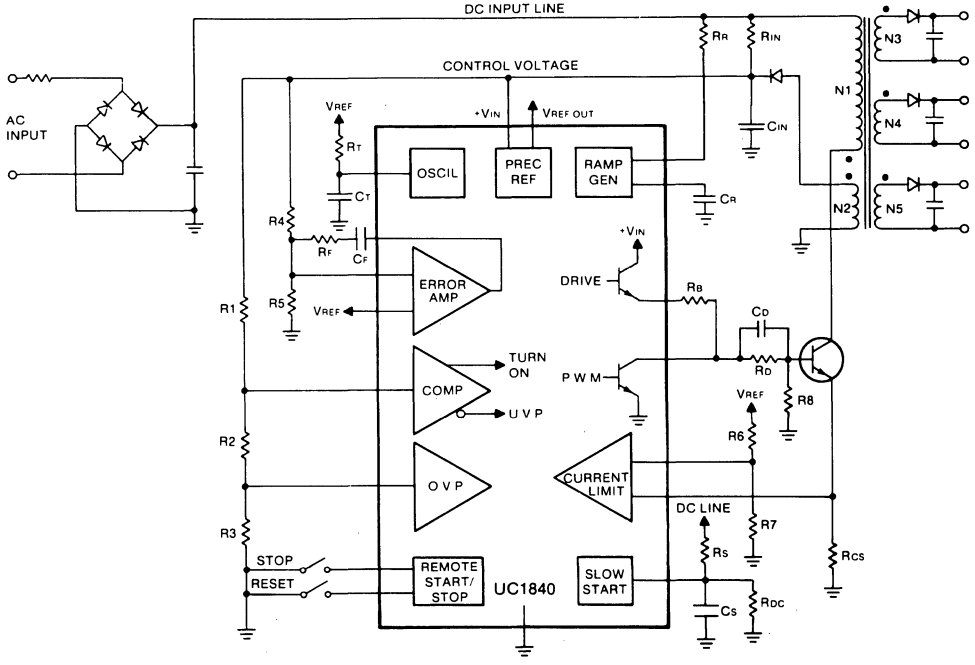

FIGURE 2. A FULLY PROTECTED, ISOLATED FLYBACK POWER SUPPLY CAN BE IMPLEMENTED WITH THE UC1840, A HIGH-VOLTAGE POWER SWITCH, THE TRANSFORMER, AND A SMALL HANDFUL OF PASSIVE COMPONENTS.

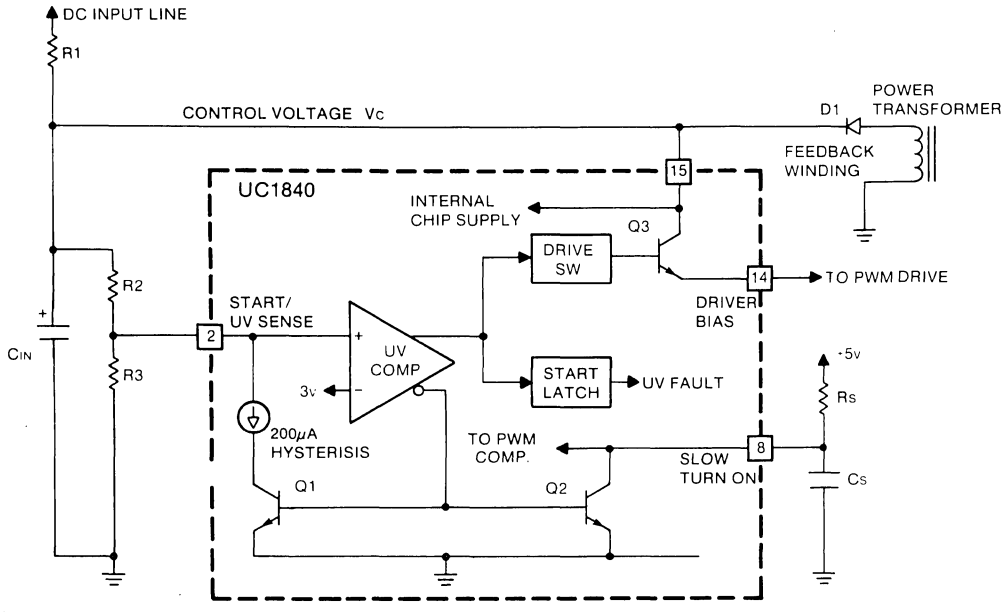

FIGURE 3. THE UC1840's START CIRCUITRY REQUIRES LOW STARTING CURRENT FROM THE DC INPUT LINE WITH NORMAL OPERATING CURRENT SUPPLIED FROM A LOW-VOLTAGE FEEDBACK WINDING ON THE POWER TRANSFORMER.

(1) While the control voltage, Vc, is low enough so that the voltage on pin 2 is less than 3V, the Start/UV Comparator does the following:

(a) A 200μA hysteresis current is flowing into pin 2 through Q1 causing an added drop across R2.

(b) The drive switch is holding the Driver Bias transistor, Q3, OFF. This insures that the only current required through R1 is the start-up current of the UC1840, plus external dividers (R2, R3, Rs, etc.).

(c) The Slow Turn-on transistor, Q2, is ON, holding pin 8 and Cs low.

(d) The Start Latch keeps the under-voltage signal from being defined as a fault.

(2) The start level is defined by:

$$Vc\ (start) = 3\left(\frac{R2 + R3}{R3}\right) + 0.2\ R2.$$

When Vc rises to this level, the Start/UV Comparator then does the following:

(a) Turns off Q1, eliminating the 200μA hysteresis current. This allows the voltage on Vc to drop before reaching the under-voltage fault level defined by:

$$Vc\ (U.V.\ fault) = 3\left(\frac{R2 + R3}{R3}\right)$$

(b) Sets the Start Latch to monitor for an under-voltage fault.

(c) Activates Q3 providing Driver Bias to the power switch, pulling the added current out of Cin.

(d) Turns off Q2 allowing for programmed slow turn-on defined by Rs and Cs.

(3) A normal start-up occurs with the control voltage, Vc, following the path shown in Figure 4. If the power supply does not start, Vc will fall to an under-voltage fault which will then either initiate a restart attempt or hold the power switch off, depending upon

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the status of the Reset terminal as defined under Fault Sequencing (Para. 3.4.2). If start-up does not occur because of some fault in the Driver Bias line, Vc will continue to rise until the 40V zener across the reference circuit conducts. This will then clamp Vc to that level, protecting the control chip.

After start-up occurs, current will continue to flow in R1 providing a power loss of:

$$Pd = \frac{(Vline - Vc)^2}{R1}$$

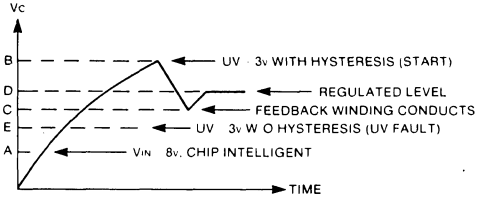

FIGURE 4. UNDER A NORMAL TURN-ON, THE SUPPLY VOLTAGE TO THE UC1840, Vc, WOULD RISE LIGHTLY LOADED TO THE START LEVEL, FALL UNDER THE TURN-ON LOAD, AND THEN REGULATE AT SOME INTERMEDIATE LEVEL.

If this loss is objectionable, it can be reduced more than an order of magnitude by the addition of a two-transistor switch shown in Figure 5. In this circuit, Q1 is initially driven on by current through R2. When the feedback winding starts to conduct through D1, however, Q2 turns on leaving only R2 conducting from the input line.

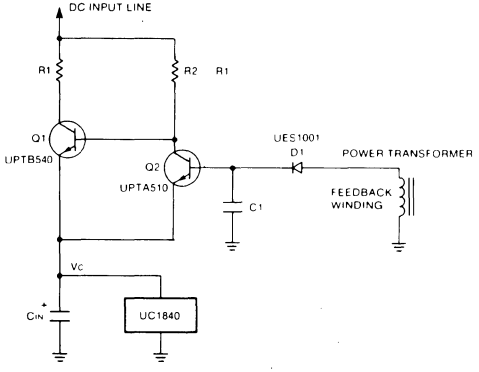

FIGURE 5. THE ADDITION OF Q1 AND Q2 CAN ELIMINATE THE STEADY-STATE CURRENT THROUGH R1 AFTER TURN-ON. Q2 IS SELECTED TO PASS ALL CONTROL CURRENT THROUGH ITS BASE-EMITTER JUNCTION.

3.2 Slow Turn-on Circuit

The PWM comparator input connected to pin 8 accommodates several programming functions, shown in Figure 6. Since this comparator will only follow the lowest positive input, holding pin 8 low will effectively eliminate a PWM signal, regardless of the status of the Error Amplifier output. Prior to turn-on, and at all times when a fault has been sensed, Q1 is ON, holding pin 8 low.

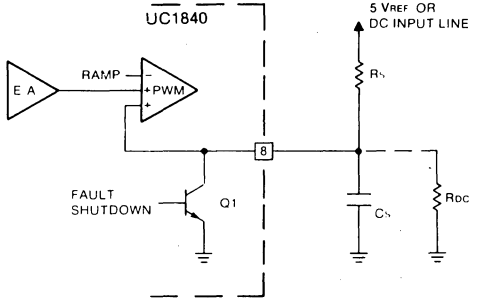

FIGURE 6. PIN 8 ON THE UC1840 CAN BE USED FOR BOTH SLOW TURN-ON AND DUTY-CYCLE LIMITING AS WELL AS A PWM SHUTDOWN PORT.

When Q1 turns off, allowing pin 8 to rise with a controlled rate will cause the output pulses to increase from zero to nominal widths at the same rate. This is accomplished by the addition of Cs and a charging source, such as Rs, to the 5V reference.

Note that where starting energy is stored in an input capacitor, the time for PWM turn-on must be less than the time required for the added Driver Bias load current to discharge the input capacitor to the under-voltage fault level. In other words, referring back to Figure 4, the slow turn-on must be faster than the time required for Vc to fall from level B to level E.

Another function of pin 8 is to establish a maximum duty cycle limit. This is achieved by clamping the voltage on pin 8 with a divider formed by adding Rdc to ground. If Rs is taken to the 5V reference, the clamp voltage will be fixed, which is desirable if the ramp slope is also fixed. If the ramp slope is varied with the input line—for constant volt-second operation—then the clamp voltage on pin 8 must also vary. This is readily accomplished by connecting Rs to the DC input line. The divider voltage:

$$VPin\ 8 = \left(\frac{Rdc}{Rs + Rdc}\right) V\ DC\ input$$

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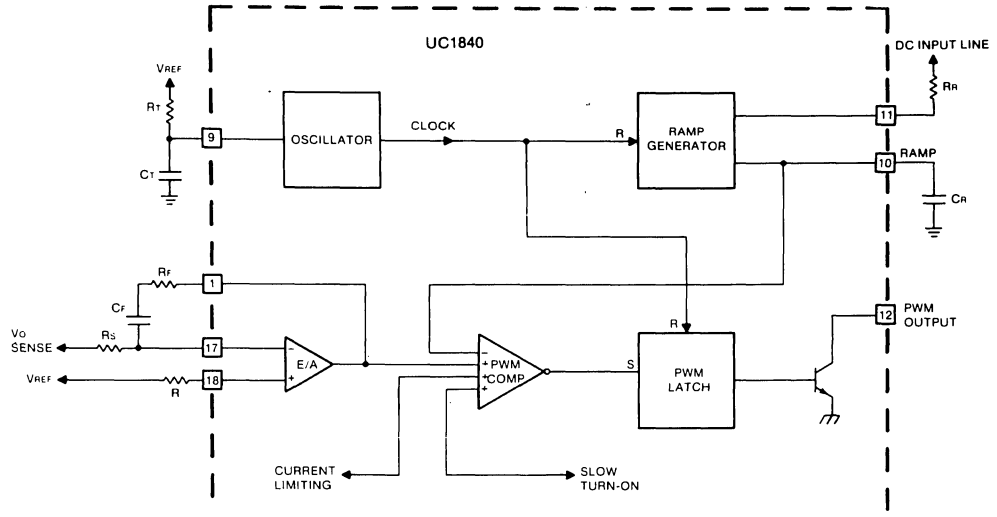

FIGURE 7 THE PULSE-WIDTH MODULATOR WITHIN THE UC1840 SEPARATES THE RAMP FUNCTION FROM THE FIXED-FREQUENCY OSCILLATOR.

should be equal to the ramp voltage level that yields the desired maximum duty cycle, at the same DC input level.

3.3 PWM Control

Pulse-Width Modulation within the UC1840 consists of the blocks shown in Figure 7. This architecture, with the possible exception of the separation between the time-base and ramp functions, is fairly conventional. It is described in greater detail in the paragraphs which follow.

3.3.1 Oscillator

A constant clock frequency is established by connecting Rt from pin 9 to the 5V reference and Ct from pin 9 to ground. The frequency is approximated by:

$$f \approx \frac{1}{Rt\ Ct}$$

where the value of Rt can range from 1kΩ to 100kΩ and Ct from 300pF to 0.1μF. The best temperature coefficients occur with Ct in the range of 1000 to 3000pF. Although the clock output pulse is not available external to the UC1840, synchronization to an external clock can still be accomplished with the circuit of Figure 8, where R1 and C1 are selected to provide a 0.5V, 200ns pulse across the 51Ω resistor, and Rt and Ct define a frequency slightly lower than the synchronizing source.

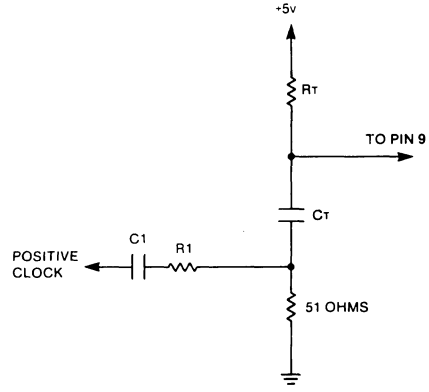

FIGURE 8. SYNCHRONIZATION TO AN EXTERNAL TIME BASE CAN BE ACCOMPLISHED BY ADDING A 51Ω RESISTOR IN SERIES WITH CT.

To achieve minimum start-up current, the oscillator is not activated until the input voltage is high enough to give a start command to the drive switch.

3.3.2. Ramp Generator

The ramp generator function of the UC1840 is shown in simplified form in Figure 9.

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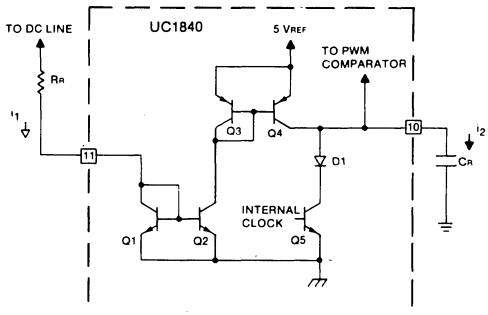

FIGURE 9. CURRENT MIRRORS Q1-Q4 ARE USED TO MAKE THE RAMP CHARGING CURRENT i2, LINEARLY PROPORTIONAL TO THE DC INPUT LINE

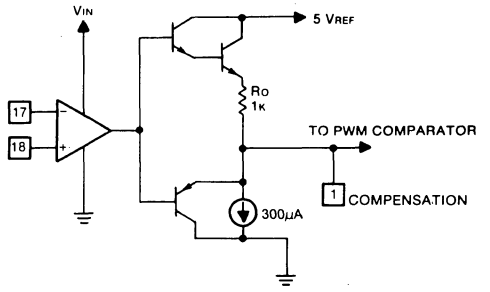

FIGURE 10. THE OUTPUT OF THE ERROR AMPLIFIER OPERATES CLASS A TO 300μA, BUT CAN SOURCE AND SINK MORE THAN 1 mA FOR FAST RESPONSE

The NPN and PNP current mirrors provide a charging current to Cr of:

$$i2 = il = \frac{Vline - 0.7V}{Rr} \simeq \frac{Vline}{Rr}$$

The current mirrors are useful over a current range of 1μA to 1mA, but optimum tracking occurs between 30μA and 300μA. Since the voltage across Q1 is very small, i2 accurately represents the input line voltage. The ramp slope, therefore, is:

$$\frac{dv}{dt} = \frac{Vline}{Rr\ Cr}$$

The peak voltage across Cr is clamped to approximately 4.2V while the valley, or low voltage, is determined by the on-voltage of the discharge network, D1 and Q5. This is typically 0.7V.

If line sensing is not required, Rr should be connected to the 5V reference for constant ramp slope.

3.3.3 Error Amplifier

This is a voltage-mode operational amplifier with an uncommitted NPN differential input stage and an output configuration as shown in Figure 10.

The 1kΩ output resistor, Ro, is used both for short circuit protection and to limit the peak output voltage to less than 4.0V so it cannot rise above the clamped ramp waveform. At sink currents less than 300μA, the low output level will be within 200mV of ground but it rises to 1V at higher current levels.

The input common mode range is from 1V to within 2V of the input supply voltage, Vin, and thus either input can be connected directly to the 5V reference.

The small signal, open-loop gain characteristics are shown in Figure 11. The amplifier is unity-gain stable and has a maximum slew rate of just under 1V/μs.

3.3.4 PWM Comparator and Latch

This comparator (see Figure 7) generates the output pulse which starts at the termination of the clock pulse and ends when the ramp waveform crosses the lowest of the three positive inputs. The clock forms a blanking pulse which keeps the maximum duty cycle less than 100%. The PWM latch insures there will be only one pulse per period and eliminates oscillation at comparator cross-over.

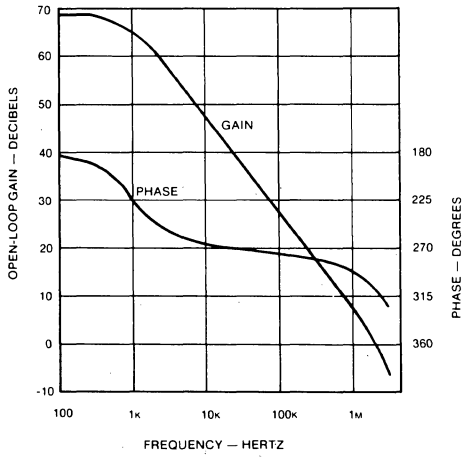

FIGURE 11. THE UC1840 ERROR AMPLIFIER HAS A DC GAIN OF 67 db, A 2 MEGAHERTZ BANDWIDTH, AND PHASE MARGIN OF APPROXIMATELY 45°

3.3.5 PWM Output Stage

In addition to the PWM output signal on pin 12, the UC1840 also includes an output gating, or arming function as Driver Bias on pin 14. Both functions should be considered together in interfacing to the external high-voltage power switch. These are illustrated in simplified form in Figure 12.

At very low input voltages (Vin < 3V), both Q2 and Q4 are OFF. This may necessitate the use of R2, but its value can be high since it does not have to turn the output switch off. It merely holds it in the off state during the early portion of start-up.

Between Vin = 3V and the start threshold (pin 2 = 3V with hysteresis on), Q2 is OFF and Q4 is ON, clamping the power switch off with a low impedance. A start command (UV high) turns on Q2, applying (Vin - 2V) to R1. This provides a source for power switch activation; however, since Q4 is still conducting, the current through R1 is shunted to ground and the power switch remains held off.

At the same time Q2 turns on, the clamping transistor at the slow-start terminal, pin 8, turns off allowing the voltage on pin 8 to rise according to the external slow-start time constant described earlier. This allows PWM pulses to begin to activate Q4—narrow at first and widening to the point where the error amplifier takes command.

The interface between the UC1840 and the primary power switch may be implemented in several different ways to meet varying system requirements. One obvious application is when the use of a bipolar transistor switch requires more drive current than the Driver Bias output can provide. Figure 13 shows a more typical bipolar drive scheme where Q5 has been added to boost the turn-on current with the UC1840 still providing the high-speed turn-off. The circuit now serves as a more efficient "totem-pole" driver since Q5 turns off when Q4 conducts. It also illustrates the use of a Baker Clamp to minimize storage time in Q6 and the capacitors for rapid turn-on and high-current pulse turn-off.

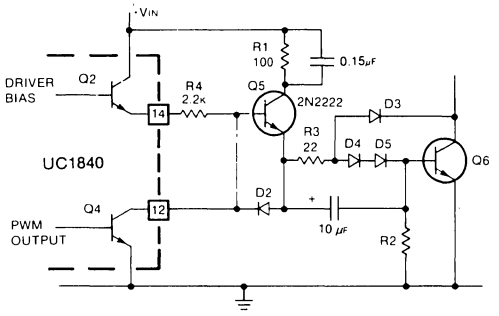

FIGURE 13. ADDING Q5 AS A SWITCHED, DRIVE-BOOST TRANSISTOR PROVIDES ADDED BASE DRIVE FOR Q6 WHILE REDUCING THE STEADY-STATE CURRENT THROUGH BOTH Q2 AND Q4.

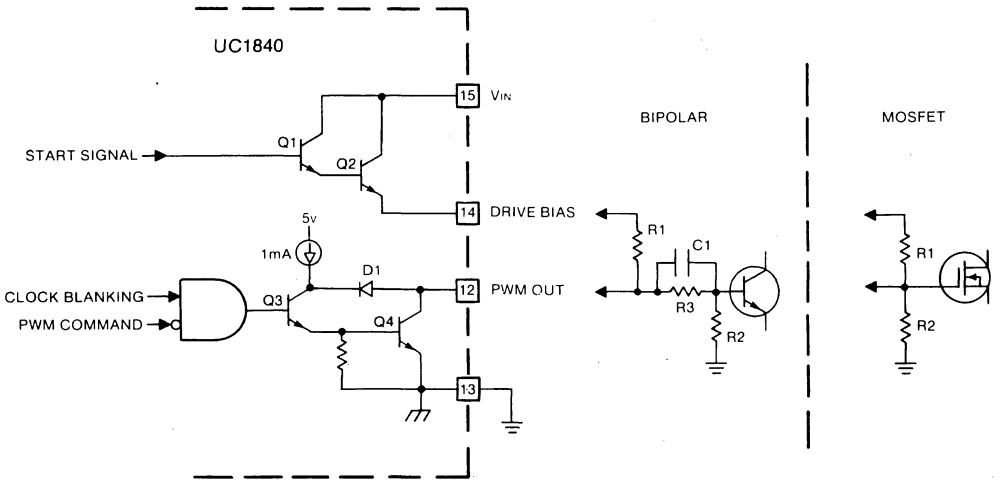

FIGURE 12. INTERFACING THE UC1840 PWM OUTPUT STAGE TO EITHER BIPOLAR OR POWER MOSFET SWITCHES.

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Another application is the two-transistor, off-line, forward converter topology shown in Figure 14. This circuit uses proportional base drive where the UC1840 need only supply a short, turn-off current pulse with transformer regeneration through T1 providing the steady-state drive. The magnetizing current is controlled by R1, with Q5 added to rapidly recharge C1 from which the turn-off current is supplied.

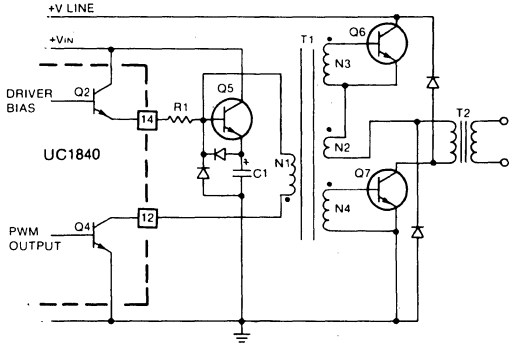

FIGURE 14. INTERFACING THE UC1840 SINGLE PWM OUTPUT TO A TWO-TRANSISTOR OFF-LINE FORWARD CONVERTER WHICH USES PROPORTIONAL BASE DRIVE.

3.4 Fault Protection

A significant benefit in using the UC1840 is the multi-faceted fault-sensing and programming capability built into the device. With the intent to provide complete control to the power system under all types of potential malfunctions, fault-sensing circuitry has been included to sense over-voltage, under-voltage, or over-current conditions. Additionally, high-speed, pulse-by-pulse digital current limiting is included as a separate function. The operation of these circuits is described below.

3.4.1 Current Limiting

The current limit comparators have differential inputs for noise rejection but are intended to be used with ground-referenced current sensing as in Figure 15. Comparator A1 is delegated to pulse-by-pulse current limiting. The output of this comparator drives the PWM comparator, where it activates the PWM latch, terminating each pulse when the current sensed by Rsc reaches a threshold defined by divider R1, R2, and the 5V reference. Since Vc is intended to track the supply's output voltage, the addition of a resistor from pin 6 to Vc will provide some foldback to the current limit characteristic. Since comparator A1 has zero offset

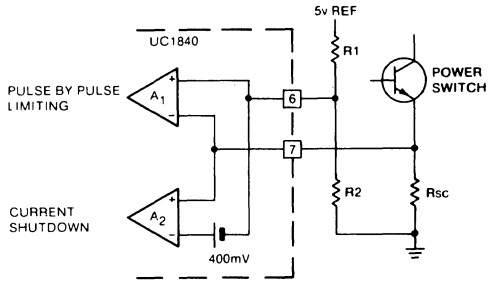

FIGURE 15. CURRENT LIMITING AND OVERCURRENT SHUTDOWN ARE IMPLEMENTED WITH COMPARATORS OF DIFFERENT THRESHOLDS AND A SINGLE CURRENT SENSE RESISTOR.

voltage, it is activated when the voltage across Rsc equals that across R2. Comparator A2, with an offset voltage of 400mV, will activate for over-current shutdown when the voltage across Rsc rises to 400mV higher than the voltage across R2. Since the input bias to both comparators is less than 5μA, a low-pass filter for noise rejection may be inserted between Rsc and the sense inputs. Activation of comparator A2 is defined as an over-current fault and it triggers the Error Latch. Its operation follows.

3.4.2 Fault Sequencing

The fault sequencing logic of the UC1840 is shown in Figure 16. Since a fault is defined by this device as an activation of the Error Latch, it makes sense to start here in an attempt to understand this portion of the circuitry. Setting the Error Latch immediately turns on Q1 and Q2, discharging the slow-start capacitor and terminating the PWM output. Note that there is an additional path from the inverted output of the Start/UV comparator through OR2 which keeps pin 8 low. This is to keep the slow-start low during initial turn-on which is not intended to be classified as a fault.

The input to the Error Latch is from OR1 which triggers on signals resulting from four possible events:

(1) A voltage less than 3V (after prior turn-on) at the Start/UV sense terminal, pin 2

(2) A voltage greater than 3V at the Over-Voltage Sense terminal, pin 3

(3) A voltage of less than 3V on the Ext. Stop terminal, pin 4

(4) An over-current signal resulting in a differential voltage between pins 7 and 6 of greater than 400mV

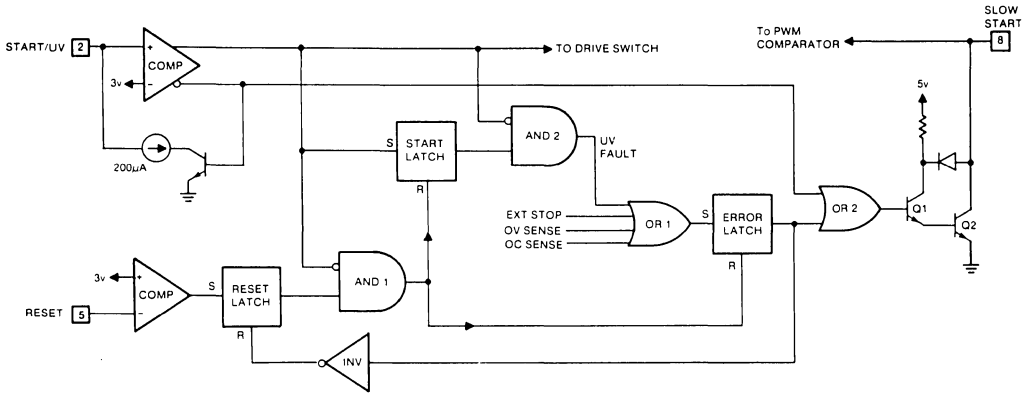

FIGURE 16. FAULT SEQUENCE LOGIC IS DESIGNED TO INSURE A COMPLETE SHUTDOWN AND FULLY CONTROLLED RESTART UPON ANY OF FOUR POSSIBLE FAULT CONDITIONS.

Any of these inputs need only be momentary to set the Error Latch. Transient protection may be necessary to eliminate false triggering, but it can be readily accomplished as all the comparator inputs are high impedances requiring less than 2μA of input current, and the 3.0V reference yields a high noise immunity.

The Start Latch can be understood by recognizing that at initial turn-on it is reset with a low output. This prevents AND2 from transmitting a UV fault signal from the Start/UV non-inverting output to the Error Latch. At the start voltage level, defined by a high level on the Start/UV non-inverting ouput, the Start Latch sets but AND2 still provides no output. Only when the Start/UV input goes low again, with the Start Latch output held high, will AND2 yield an output into the Error Latch.

The status of the Reset terminal, pin 5, determines what happens after the Error Latch is set. The choices are:

(1) Latch off and require a recycle of input voltage to restart
(2) Continuously attempt to restart
(3) Attempt some number of restarts and then latch off
(4) Latch off and await a momentary reset pulse to restart

To examine the operation of the Reset Latch, note that prior to setting the Error Latch, its low output is inverted to hold the reset input to the Reset Latch high. This forces the Reset Latch's ouput low, regardless of the voltage on pin 5, and, thus, insures no signal out of AND1. With the setting of the Error Latch, the Reset Latch is free to take the state commanded by pin 5: high if pin 5 is low and vice-versa. The latch allows merely a pulse to set the Reset Latch; the voltage on pin 5 need not be steady state.

With a high Reset Latch output, the Error Latch still does not reset until a low signal is sensed on the Start/UV sense terminal. At that point, AND1 then resets both the Error Latch and the Start Latch, re-establishing the initial conditions for a normal start after fully charging the input capacitor. Of course, if the fault is still present, when the Start/UV input reaches the start level terminating the Error Latch reset signal, this latch will immediately set again.

To aid in the understanding of this logic, Figure 17 gives a pictorial representation of its operation with both steady-state and momentary signals on both the Ext. Stop and Reset terminals.

If Driver Bias turn-on is used to pump an increment of charge into an integrating capacitor, and that capacitor voltage is applied to the Reset Terminal, some number of retrys could be programmed to take place before the Reset voltage rises to 3V, which would then lock the output OFF. Since Driver Bias continues to cycle in the latched-off state, the Reset terminal will remain high until it is either remotely pulled low or the input voltage to the controller is interrupted.

Note that an important element in any restart after a shutdown is the lowering of the voltage at the Start/UV terminal below its UV threshold. While this will occur normally in bootstrap-driven applications, this device can also be used with a con-

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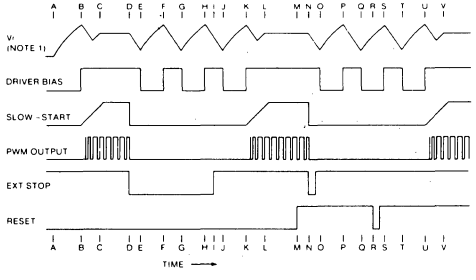
stant driving voltage by externally applying a momentary pull-down signal to the Start/UV input after a fault shutdown.

4. Conclusion

With the UC1840, power supply designers now have a device specifically developed for off-line, primary control and one which has addressed the problems of operation under less than "ideal" or normal conditions. Not only does this device make it easier to comply with stringent isolation requirements by requiring a minimum of communication between primary and secondary, but it is also ideally suited for powering systems in remote locations where only a simple transmitted pulse is available for power sequencing.



NOTE 1: Vc REPRESENTS AN ANALOG OF THE SUPPLY OUTPUT VOLTAGE GENERATED BY A PRIMARY-REFERENCED SECONDARY WINDING ON THE POWER TRANSFORMER. IT IS THE VOLTAGE MONITORED BY THE START/UV COMPARATOR AND, IN MOST CASES, IS THE SUPPLY VOLTAGE, VIN, FOR THE UC1840.

TIME	EVENT
A	INITIAL TURN-ON. Vc RISES WITH LIGHT LOAD.
B	START THRESHOLD. DRIVER BIAS LOADS Vc.
C	OPERATING PWM REGULATES Vc.
D	STOP INPUT SETS. ERROR LATCH TURNING OFF PWM.
E	UV LOW THRESHOLD. ERROR LATCH REMAINS SET.
F	START TURNS ON DRIVER BIAS BUT ERROR LATCH STILL SET.
G	Vc AND DRIVER BIAS CONTINUE TO CYCLE.
H	
I	STOP COMMAND REMOVED.
J	ERROR LATCH RESET AT UV LOW THRESHOLD.
K	START THRESHOLD NOW REMOVES SLOW-START CLAMP.
L	RETURN TO NORMAL RUN STATE.
M	RESET LATCH SET SIGNAL REMOVED.
N	ERROR LATCH SET WITH MOMENTARY FAULT.
O	ERROR LATCH DOES NOT RESET AS RESET LATCH IS RESET.
P	Vc AND DRIVER BIAS RECYCLE WITH NO TURN-ON.
Q	
R	RESET LATCH IS SET WITH MOMENTARY RESET SIGNAL.
S	Vc MUST COMPLETE CYCLE TO TURN ON.
T	START AND ERROR LATCHES RESET.
U	NORMAL START INITIATED.
V	RETURN TO NORMAL RUN STATE.

FIGURE 17. THE INTERRELATIONSHIP BETWEEN THE FUNCTIONS CONTROLLED BY THE FAULT SEQUENCE LOGIC IS ILLUSTRATED WITH BOTH STATIC AND PULSE COMMANDS ON THE EXT. STOP AND RESET TERMINALS.

A NEW INTEGRATED CIRCUIT FOR CURRENT-MODE CONTROL

Abstract

The inherent advantages of current-mode control over conventional PWM approaches to switching power converters read like a wish list from a frustrated power supply design engineer. Features such as automatic feed forward, automatic symmetry correction, inherent current limiting, simple loop compensation, enhanced load response, and the capability for parallel operation all are characteristics of current-mode conversion. This paper introduces the first control integrated circuit specifically designed for this topology, defines its operation and describes practical examples illustrating its use and benefits.

1.0 Introduction

Over the past several years an increased interest in current-mode control of switching inverters has surfaced in the literature. Originally invented in the late 1960s, this scheme was not publicly reported until 1977[1] and has seen rapid development by many authors to date.[2-6] In short, current-mode control uses an inner or secondary loop to directly control peak inductor current with the error signal rather than controlling duty ratio of the pulse width modulator as in conventional converters. Practically, this means that instead of comparing the error voltage to a voltage ramp, it is compared to an analogue of the inductor current forcing the peak current to follow the error voltage.

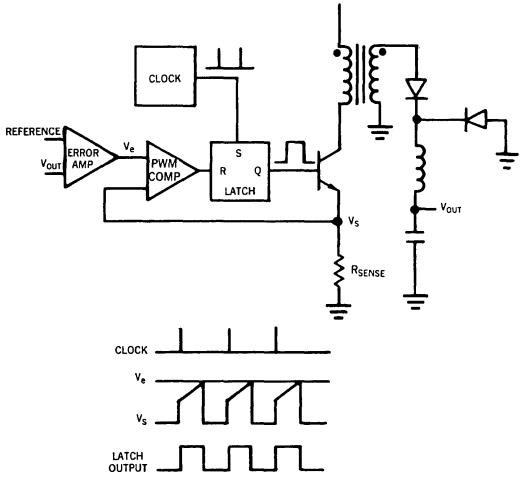


FIGURE 1. A FIXED FREQUENCY CURRENT-MODE CONTROLLED REGULATOR.

Figure 1 illustrates a simplified block diagram of a fixed frequency buck regulator employing current-mode control. As shown, the error signal, V_e, is controlling peak switch current which, to a good approximation, is proportional to average inductor current. Since the average inductor current can change only if the error signal changes, the inductor may be replaced by a current source, and the order of the system reduced by one. This results in a number of performance advantages including improved transient response, a simpler, more easily designed control loop, and line regulation comparable to conventional feed-forward schemes. Peak current sensing will automatically provide flux balancing thereby eliminating the need for complex balance schemes in push-pull systems. Additionally, by simply limiting the peak swing of the error voltage V_e, instantaneous peak current limiting is accomplished. Lastly, by feeding identical power stages with a common error signal, outputs may be paralleled while maintaining equal current sharing.

Although the advantages of current-mode control are abundant, wide acceptance of this technique has been hampered by a lack of suitable integrated circuits to perform the associated control functions. This paper introduces a new integrated circuit designed specifically for control of current-mode converters. Circuit function and features are described in detail, and a comparative design example is used to illustrate the numerous advantages of this approach.

2.0 UC1846 Chip Architecture

In addition to all the functions required of conventional PWM controllers, a current-mode controller

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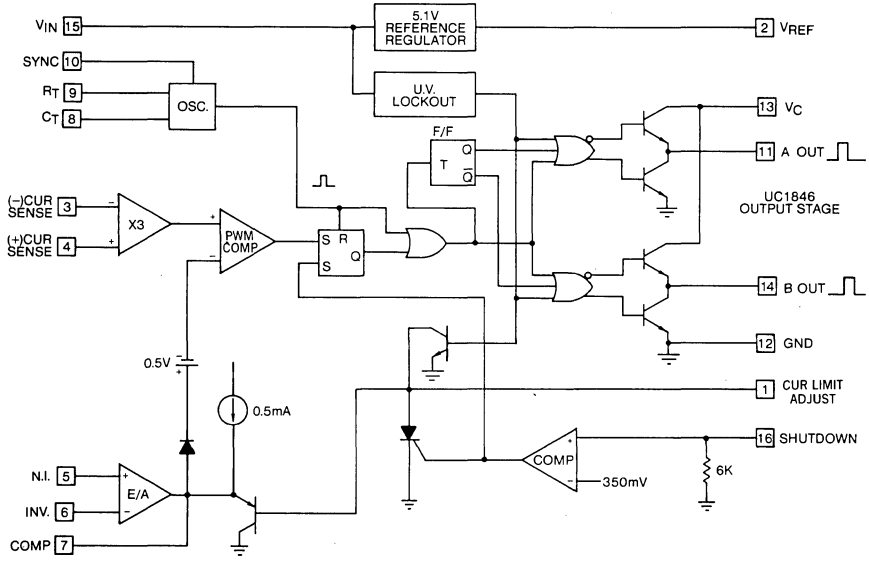


FIGURE 2. UC1846 BLOCK DIAGRAM

must be able to sense switch or inductor current and compare it on a pulse-by-pulse basis with the output of the error amplifier. As may be seen in the block diagram of Figure 2, this is accomplished in the UC1846 by using a differential current sense amplifier with a fixed gain of 3. The amplifier allows sensing of low level voltages while maintaining high noise immunity. A list of other features, while not unique to current-mode conversion, demonstrates the advanced, state-of-the-art architecture of the UC1846:

- A ± 1%, 5.1V trimmed bandgap reference used both as an external voltage reference and internal regulated power source to drive low level circuitry.
- A fixed frequency sawtooth oscillator with variable deadtime control and external synchronization capability. Circuitry features an all NPN design capable of producing low distortion waveforms well in excess of 1MHz .
- An error amplifier with common mode range from ground to V_{cc}-2V.
- Current limiting through clamping of the error signal at a user-programmed level.
- A shutdown function with built in 350mV threshold. May be used in either a latching, or non-latching mode. Also capable of initiating a "hiccup" mode of operation.
- Under-voltage lockout with hysteresis to guarantee outputs will stay "off" until reference is in regulation.
- Double pulse suppression logic to eliminate the possibility of consecutively pulsing either output.
- Totem pole output stages capable of sinking or sourcing 100mA continuous, 400mA peak currents.

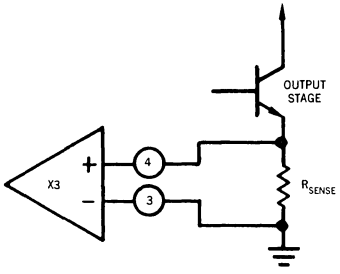
These various features, along with their interrelationships and applications to switched-mode regulators, will be further discussed in the following sections.

3.0 UC1846 Functional Description

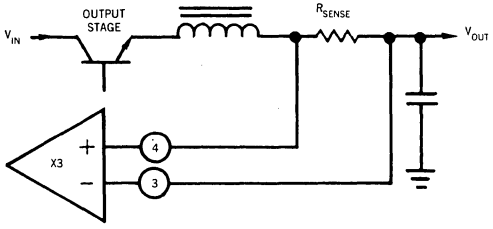
3.1 Current Sense Amplifier

The current sense amplifier may be used in a variety of ways to sense peak switch current for comparison with an error voltage. Referring to Figure 2, maximum swing on the inverting input of the PWM comparator is limited to approximately 3.5V by the internal regulated supply. Accordingly, for a fixed gain of 3, maximum differential voltages must be kept below 1.2V at the current sense inputs. Figure 3 depicts several methods of configuring sense schemes. Direct resistive sensing is simplest, however, a lower peak voltage may be required to minimize power loss in the sense resistor. Transformer coupling can provide isolation and increase effi-

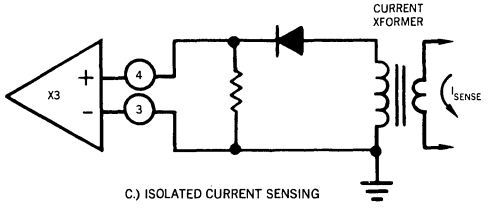
ciency at the cost of added complexity. Regardless of scheme, the largest sense voltage consistent with low power losses should be chosen for noise immunity. Typically, this will range from several hundred millivolts in some resistive sense circuits to the maximum of 1.2V in transformer coupled circuits.



A.) RESISTIVE SENSING WITH GROUND REFERENCE



B.) RESISTIVE SENSING ABOVE GROUND



C.) ISOLATED CURRENT SENSING

FIGURE 3. VARIOUS CURRENT SENSE SCHEMES

In addition, caution should be exercised when using a configuration that senses switch current (Figure 3A) instead of inductor current (Figure 3B). As the switch is turned on, a large instantaneous current spike can be generated in the sense resistor as the collector capacitance of the switch is discharged. This spike will often be of sufficient magnitude and duration to trip the current sense latch and result in erratic operation of the PWM circuit, particularly at lower duty cycles. A small RC filter (Figure 4) in series with the input is generally all that is required to reduce the spike to an acceptable level.

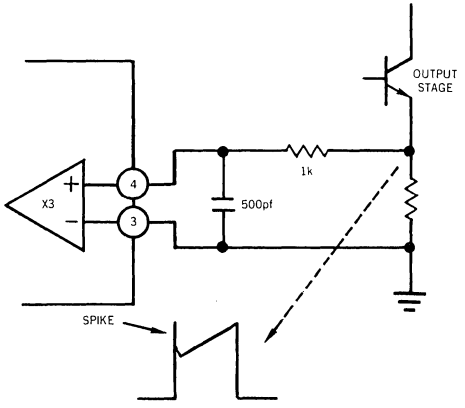


FIGURE 4. RC FILTER FOR REDUCING SWITCH TRANSIENTS

3.2 Oscillator

Although many data sheets tout 300 to 500kHz operation, virtually all PWM control chips suffer from both poor temperature characteristics and waveform distortions at these frequencies. Practical usage is generally limited to the 100 to 200kHz range. This is a direct consequence of having slow (f_t = 2MHz) PNP transistors in the oscillator signal path. By implementing the oscillator using all NPN transistors, the UC1846 achieves excellent temperature stabillity and waveform clarity at frequencies in excess of 1MHz.

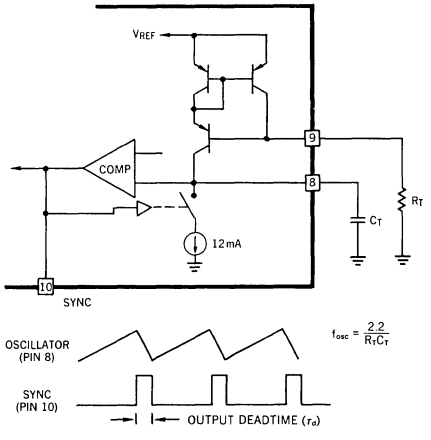


FIGURE 5. OSCILLATOR CIRCUIT

Referring to Figure 5, an external resistor R_T is used to generate a constant current into a capacitor C_T to

9

produce a linear sawtooth waveform. Oscillator frequency may be approximated by selecting R_T and C_T such that:

$$f_{osc} = \frac{2.2}{R_T C_T} \quad (1)$$

Where R_T can range from 1K to 500K and C_T is above 100pF. For quick reference a plot of frequency versus R_T and C_T is given in Figure 6.

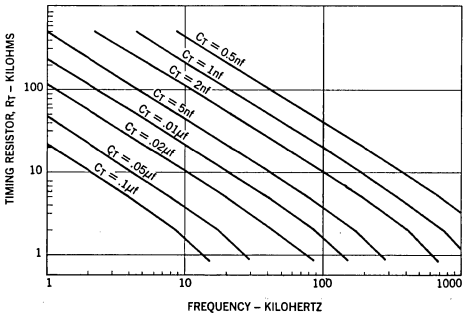


FIGURE 6. OSCILLATOR FREQUENCY AS A FUNCTION OF R_T AND C_T

Again referring to Figure 5, the oscillator generates an internal clock pulse used, among other things, to blank both outputs and prevent simultaneous cross conduction during switching transitions. This output "deadtime" is controlled by the oscillator fall time. Fall time, in turn, is controlled by C_T according to the formula:

$$\tau d = 145\ C_T \left[\frac{12}{12 - 3.6/R_T(k\Omega)}\right] \quad (2)$$

For large values of R_T:

$$\tau d = 145\ C_T \quad (3)$$

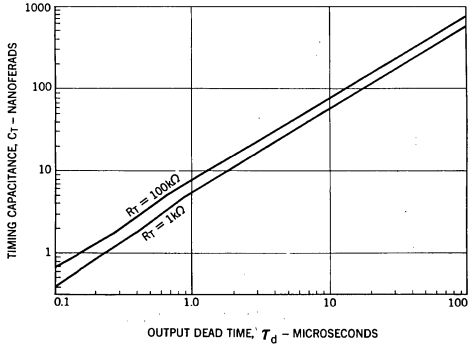


FIGURE 7. OUTPUT DEADTIME AS A FUNCTION OF TIMING CAPACITOR C_T

A plot of output deadtime versus C_T for two values of R_T is given in Figure 7.

Although timing capacitors as small as 100pF can be used successfully in low noise environments, it is generally recommended that C_T be kept above 1000pF to minimize noise effects on the oscillator frequency (see Section 4.0).

Synchronization of one or more devices to either an external time base or another UC1846 is accomplished via the bi-directional SYNC pin. To synchronize devices, first, C_T must be grounded to disable the internal oscillator on all slaved devices. Second, an external synchronization pulse must be applied to the SYNC terminal. This pulse can come directly from the SYNC terminal of a master UC1846 or, alternatively, from an external time base as shown in Figure 8.

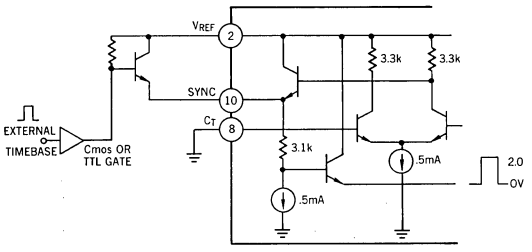


FIGURE 8. SYNCHRONIZING THE 1846 TO AN EXTERNAL TIME BASE

3.3 Current Limit

One of the most attractive features of a current-mode converter is its ability to limit peak switch currents on a pulse-by-pulse basis by simply limiting the error voltage to a maximum value. Referring to Figure 9, peak current limiting in the UC1846 is accomplished using a divider network, R_1 and R_2, to set a pre-determined voltage at pin 1.

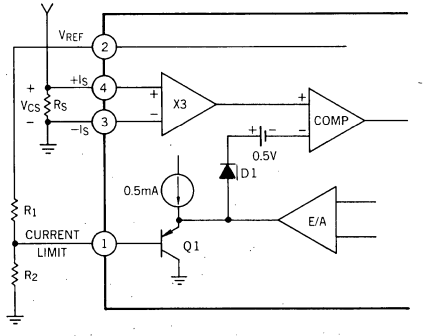


FIGURE 9. PEAK CURRENT LIMIT SET UP

This voltage, in conjunction with Q_1, acts to clamp the output of the error amplifier at a maximum value. Since the base emitter drop of Q_1 and the forward drop of diode D_1 very nearly cancel, the negative input of the comparator will be clamped at the value $V_{PIN\ 1}$ −0.5V. Following this through to the input of the current sense amplifier yields:

$$V_{cs} = \frac{V_{PIN\ 1} - 0.5}{3} \qquad (4)$$

Where V_{cs} is the differential input voltage of the current sense amplifier. Using this relationship, a value for maximum switch current in terms of external programming resistors can be derived, resulting in:

$$I_{CL} = \frac{\frac{R_2\,(V_{REF})}{R_1 + R_2} - 0.5}{3R_S} \qquad (5)$$

While still on the subject of resistor selection, it should be pointed out that R_1 also supplies holding current for the shutdown circuit, and therefore should be selected prior to selecting R_2 as outlined in the next section.

One last word on the current limit circuit. As may be seen from equation 5, any signal less than 0.5V at the current limit input will guarantee both outputs to be off, making pin 1 a convenient point for both shutting down and slow starting the PWM circuit. For example, both the under-voltage lockout and shutdown functions are connected internally to this point. If a capacitor is used to hold pin 1 low (Figure 10) then as the input voltage increases above the under-voltage lockout level, the capacitor will charge and gradually increase the PWM duty cycle to its operating point. In a similar manner if the shutdown amplifier is pulsed, the shutdown SCR will be fired and the capacitor discharged, guaranteeing a shutdown and soft restart cycle independent of input pulse width.

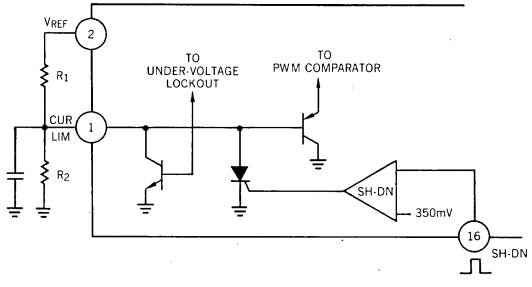


FIGURE 10. USING UNDER-VOLTAGE LOCKOUT AND SHUTDOWN TO INITIATE A SLOW START.

3.4 Shutdown

The shutdown circuit, shown in Figure 11, was designed to provide a fast acting general purpose shutdown port for use in implementing both protection circuitry and remote shutdown functions. The circuit may be divided into an input section consisting of a comparator with a 350mV temperature compensated offset, and an output section consisting of a three transistor latch. Shutdown is accomplished by applying a signal greater than 350mV to pin 16, causing the output latch to fire, and setting the PWM latch to provide an immediate signal to the outputs. At this point, several things can happen. Q_1 requires a minimum holding current, I_H, of approximately 1.5mA to remain in the latched state. Therefore, if R_1 is chosen greater than 5kΩ, Q_1 will discharge any capacitance, C_S, on pin 1 to ground and commutate the output latch, allowing C_S to recharge. If R_1 is chosen less than 2.5kΩ, Q_1 will discharge C_S and remain in the latched state until power is externally cycled off. In either case, C_S is required only if a soft-start or soft-restart function is desired.

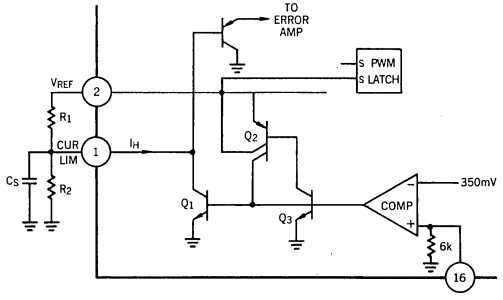


FIGURE 11. SHUTDOWN CIRCUITRY

For example, the shutdown circuit of Figure 12, operating in a nonlatched mode, will protect the supply from overcurrent fault conditions. Many times, if the output of a supply is shorted, circulating currents in the output inductor will build to dangerous levels. Pulse-by-pulse current limiting with its inherent time delay, will in general not be able to limit these currents to acceptable levels. Figure 12 details a circuit which will provide shutdown and soft-restart if the overcurrent threshold set by R_3 and R_4 is exceeded. This level should be greater than the peak current limit value determined by R_1 and R_2 (see equation 5). Sometimes called a "hiccup mode", this overcurrent function will limit both power and peak current in the output stages until the fault is removed.

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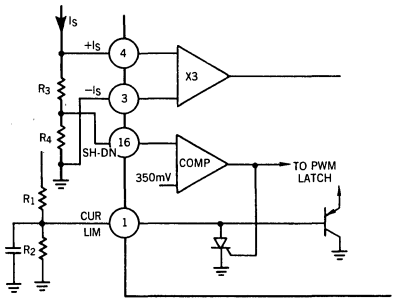


FIGURE 12. OVER CURRENT SENSING WITH THE SHUTDOWN CIRCUIT PRODUCES A SHUTDOWN — SOFT RESTART CYCLE TO PROTECT OUTPUT DRIVERS

4.0 Noise Immunity

As in all PWM circuits, some simple precautions should be observed to prevent switching noise from prematurely triggering the oscillator as it approaches its upper threshold. This is most evident when large capacitive loads — such as the gates of power FETS — are directly driven from outputs A and B. As the duty cycle approaches 100%, the current spike associated with this output capacitance can cause the oscillator to prematurely trigger with a resulting shift upward in frequency. By separating high current ground paths from low level analog grounds, using C_T values greater than 1000pF grounded directly to pin 12, and decoupling both V_{IN} and V_{REF} with good quality bypass capacitors, noise problems can be avoided.

5.0 Comparative Design Example

To more vividly illustrate the advantages of current-mode control, a relatively simple push-pull forward converter was designed using two interchangeable control sections, as shown in Figure 13. The control modules consist of (a) a UC1846 current-mode controller with associated circuitry, and (b) a conventional UC1525A PWM controller with its support circuitry. Loop compensation of the UC1525A was implemented by placing a zero in the feedback loop to cancel one of the poles in the output stage, resulting in a unity gain bandwidth of approximately 3kHz — a commonly used technique. Compensating the current-mode converter requires somewhat of a different approach. Since the output stage contains only a single pole, in theory closing the loop will produce a stable system with no additional compensation. In practice, however, it has been shown that subharmonic oscillation will result from excess gain at half the switching frequency[5]. Therefore, a pole-zero combination has been placed in the feedback loop to reduce high frequency gain and allow the output capacitor (low ESR) to roll off loop gain to 0dB at 3kHz.

While not demonstrated in Figure 13, fixed frequency current-mode converters are known to be unstable above 50% duty cycle without some form of slope compensation[4-6]. By injecting a small current from the sawtooth oscillator into the positive terminal of the current sense amplifier, slope compensation is accomplished, and the converter can be operated in excess of 50% duty cycle. An alternate, but just as effective, scheme would be to inject the signal into the negative terminal of the error amplifier.

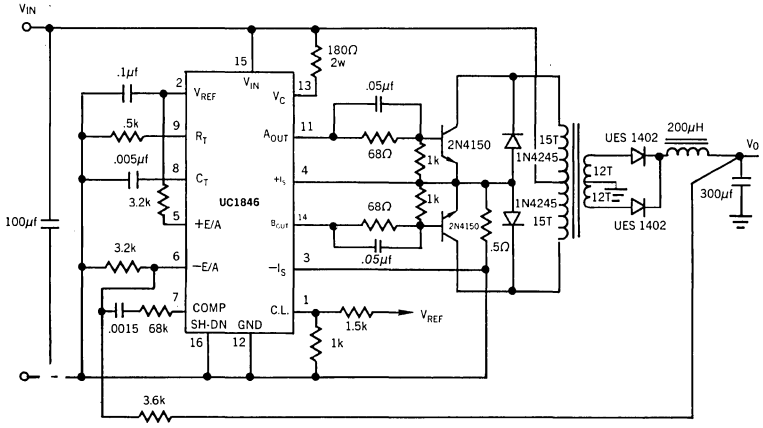
As may be seen, a similar parts count for both supplies was encountered. Topologically, using the UC1525A shutdown terminal provided only a crude current limit in contrast to the UC1846. Furthermore, internal double pulse suppression circuitry of the UC1846 gave an added level of protection against core saturation — important if your regulator is prone to subharmonic oscillations. Since both regulators were over-designed to withstand a short circuit on the output with resultant high peak currents, the shutdown-restart mode of the UC1846 was not used.

It should be pointed out at this time that one of the main features of a current-mode converter of this type is its ability to be paralleled with similar units. By disabling the oscillator and error amplifiers (C_T grounded, +E/A to V_{REF}, −E/A grounded) of one or more slave modules, and connecting SYNC and COMP pins of the slave(s) respectively, the outputs may be connected together to provide a modular approach to power supply design.

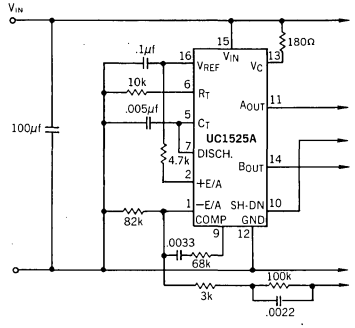
Starting with Figure 14, a comparison of line and load step responses is made between the two converters. As a result of the feed-forward effect of the current-mode converter, response to a step input change shows more than an order of magnitude improvement (Figure 14a) when compared to the conventional converter (Figure 14b). Although not as pronounced, response to a step load change leaves the UC1846 converter (Figure 15) with a clear advantage in output response — 40mV as compared to 70mV for the UC1525A.

Virtually all conventional push-pull converters are prone to flux imbalance caused by mismatched storage delays, etc., in the output stage. Figure 16 shows both converters operating with the same power stage. No effort was made to match output devices. As may be seen, there is little noticeable

difference between switch currents of the UC1846. However, the UC1525A — with identical output transistors — shows phase B driving the core close to saturation with 50% more current than phase A.

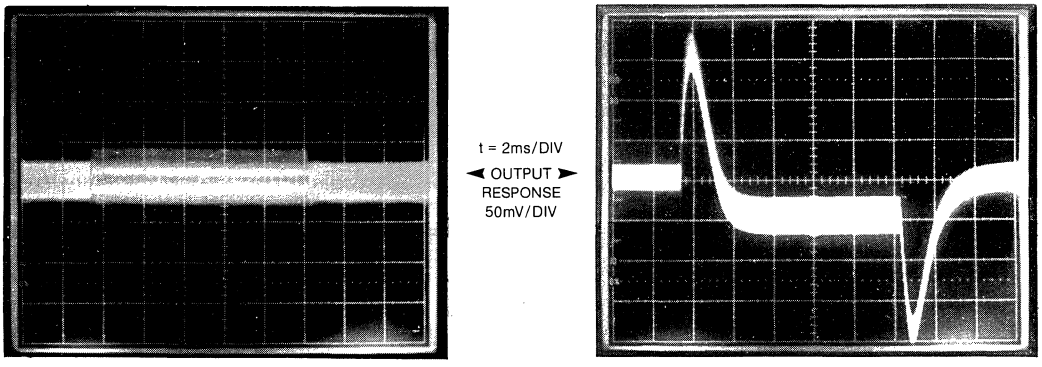


(A) UC1846 CURRENT-MODE CONTROLLED REGULATOR



(B) UC1525A VOLTAGE MODE CONTROLLER

FIGURE 13. PUSH-PULL FORWARD CONVERTER WITH (A) CURRENT-MODE CONTROL AND (B) VOLTAGE MODE CONTROL



(A) (B)

FIGURE 14. RESPONSE TO A STEP INPUT CHANGE OF 25 TO 35V BY (A) UC1846 and (B) UC1525A CONVERTERS

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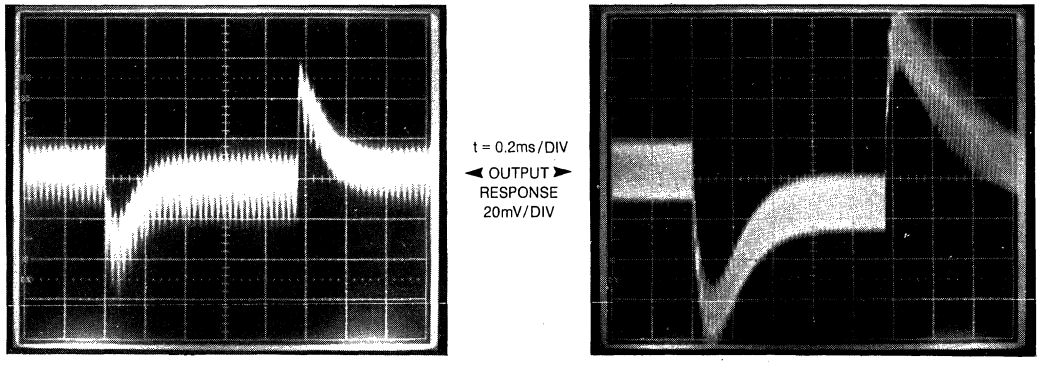

FIGURE 15. RESPONSIVE TO A STEP LOAD CHANGE OF 1 AMP BY (A) UC1846 AND (B) UC1525A CONVERTERS

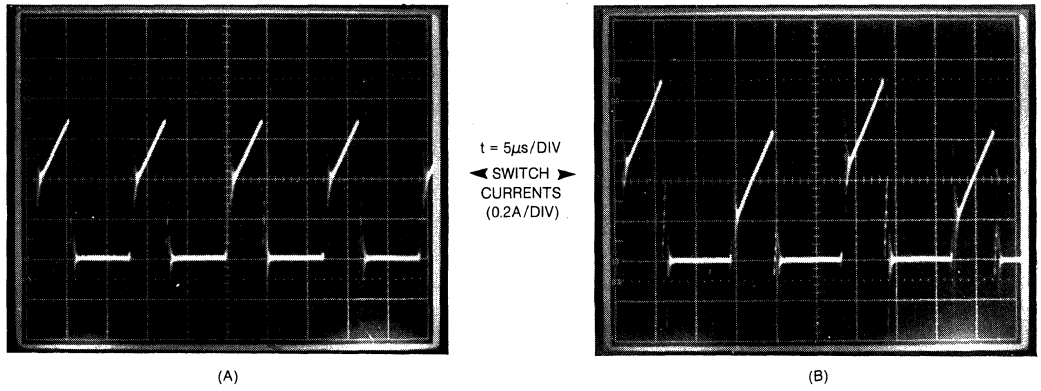

FIGURE 16. SWITCH CURRENTS SHOWING FLUX IMBALANCE IN (A) UC1846 AND (B) UC1525A CONVERTERS

6.0 Conclusion

Rarely do new design techniques evolve that can promise as much as current-mode control for the power supply engineer. We have shown this to be a simple technique easily extended from present converter topologies, that will increase dynamic performance and provide a higher degree of reliability while permitting new approaches to modular design. Until recently, current-mode converters could not compete with the economics of conventional converters designed with I.C. controllers. Now, with the UC1846 designed specifically for this task, current-mode control can provide all of the above performance advantages on a cost competitive basis.

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9

THE UC1901 SIMPLIFIES THE PROBLEM OF ISOLATED FEEDBACK IN SWITCHING REGULATORS

1. Introduction

The UC1901 simplifies the task of closing the feedback loop in isolated, primary-side control, switching regulators by combining a precision reference and error amplifier with a complete amplitude modulation system. Using the IC's amplitude modulated output, loop error signals can be transformer coupled across high voltage isolation boundaries, providing stable and repeatable closed-loop characteristics. Coupling across an isolation boundary is nothing new in transformer technology, and the UC1901's ability to generate carrier frequencies of up to 5MHz keeps the transformer size and cost at a minimum. With a secondary reference and accurate coupling path for the feedback signal, isolated off-line supplies can reliably achieve the tolerances, regulation, and transient performance of their non-isolated counter parts and still take advantage of the benefits of primary-side control.

Closing a feedback loop in a simple or complex system requires a thorough understanding of all of the loop elements. Worse case variations of each element must be taken into account when loop stability, dynamic response, and operating point are determined. Unpredictability in any of the loop components will affect the overall design by making it, necessarily, more conservative. The transient response of a control loop, for example, will usually suffer if a loop must be heavily compensated to guarantee stability with component variations.

To obtain high levels of load and line regulation, the output voltage of a power supply must be sensed and compared to an accurate reference voltage. Any error voltage must be amplified and fed back to the supply's control circuitry where the sensed error can be corrected. In an isolated supply, the control circuitry is frequently located on the primary, or line, side of the supply. As shown in Figure 1, the feedback signal in this type of supply must cross the isolation boundary. Coupling this signal requires an element that will withstand the isolation potentials and still transfer the loop error signal. Though some significant drawbacks to their use exist, optical couplers are widely used for this function due to their ability to couple DC signals. Primarily, optocouplers suffer from poor initial tolerance and stability. The gain, or current transfer ratio, through an opto-coupler is loosely specified and changes as a function of time and temperature. This variation will directly affect the overall loop gain of the system, making loop analysis more difficult and the resulting design more conservative. In addition, limited bandwidth capability prevents the use of optical couplers when an extended loop response is required.

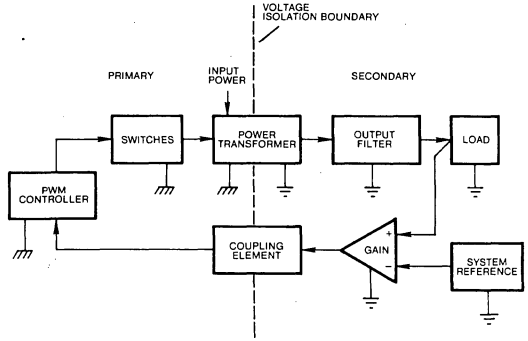

FIGURE 1: A Typical Closed-Loop Isolated Power Supply With Primary-Side Control.

With reliability firmly situated as an important aspect of electrical design, the benefits of primary-side control are increasingly attractive in off-line designs. The organization of an off-line switcher with primary-side control (See Figure 1) puts the control function on the same side of the isolation boundary as the switching elements. Not only does this simplify the interface between the controller and switches, it makes the protection of these switches much easier. Sensing of the switch currents and voltage can avoid failures and improve over-all supply performance. The argument for primary-side control has been further strengthened by the introduction of a new generation of control IC's. The controllers incorporate such features as low current start-up, high speed current sensing for pulse-by-pulse current limiting, and voltage feed-forward. Low current start-up alleviates the problem of efficiently supplying power to a line-side controller, while fast current limit circuitry and voltage feed-forward take advantage of the proximity of a primary-side controller to both the power switch(es) and the input supply voltage.

Combining all of the necessary functions to generate an AM feedback signal on the UC1901 make it the

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first IC of its type. As will be seen, the UC1901 can be used in several modes to take full advantage of its functions. Recognizing the continuing evolution of power converter technology the UC1901 is intended to simplify the design of a new era of reliable and higher performance power converters.

2. The UC1901 Functions

The operation of the UC1901 is best undestood by considering a typical application. In Figure 2, the UC1901 is shown providing the feedback signal to close the loop in an isolated switching power supply. With any feedback system it is desirable to compare the system output to the system reference with a minimum of intermediate circuitry. With the UC1901 situated on the secondary, or output side of the supply, the output voltage is simply divided down and compared to the 1.5V reference using the chip's high gain error amplifier. In this manner DC errors at the supply output are kept minimal even if significant non-linearities, or offsets, occur in the remainder of the power supply loop. Since the 1.5V output on the UC1901 is a trimmed, precision, reference, the need for a trim-pot to fine tune the output voltage is eliminated.

To make the UC1901 compatible with single output 5V power supplies it is designed to operate with input voltages as low as 4.5V. This allows the part to be powered directly from a TTL compatible 5V output. A nominal supply current of only 5mA allows the part to be easily operated at its maximum input voltage rating of 40V without worry of excessive power dissipation.

The amplified error signal at the UC1901's compensation output is internally inverted and applied to the modulator. The other input to the modulator is the carrier signal from the oscillator. The modulator combines these two signals to produce a square wave output signal with an amplitude that is directly proportional to the error signal and whose frequency is that of the oscillator input. This output is buffered and applied to the coupling transformer. With the internal oscillator, carrier frequencies into the megahertz range can be generated. Operating at high frequencies can reduce both the size and cost of the coupling transformer. The secondary winding on the coupling transformer drives a diode-capacitor peak detector. With a simple resistive load to allow discharging of the holding capacitor an effective amplitude demodulator is formed. The small signal voltage gain from the error amplifier input to the detector output is a function of the feedback network around the error-amp, the modulator gain, the turns ratio of coupling transformer, and any loss in the demodulator.

In Figure 2 the relationship of the detector output to the sense supply voltage is non-inverting. This is necessary to guarantee start-up of the supply. Since the UC1901, as shown, is powered from the supply's output, the initial feedback signal back to the PWM controller will always be zero. The required 180° of DC phase shift is easily achieved by inverting the signal with the error amplifier that is present in most any PWM controller circuit.

In some applications it may be desirable to operate the carrier frequency of the UC1901 in synchroni-

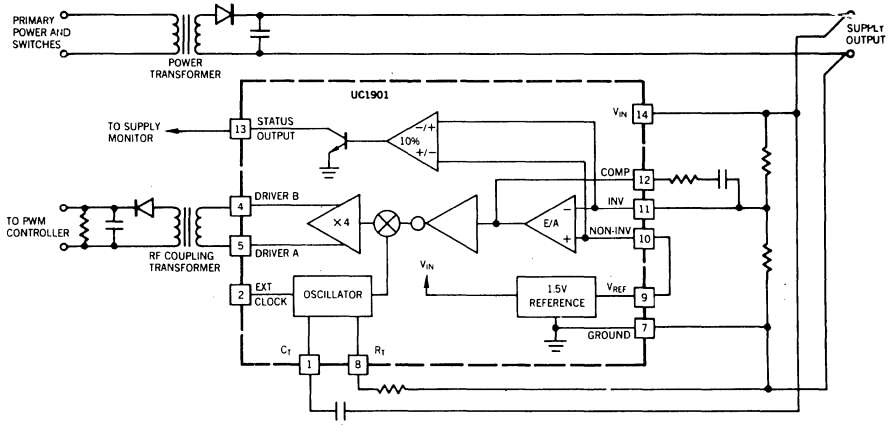


FIGURE 2: With a Precision Reference, and a Complete Amplitude Modulation System, the UC1901 Lets Isolated Feedback Loops be Closed Using a Small Signal Transformer.

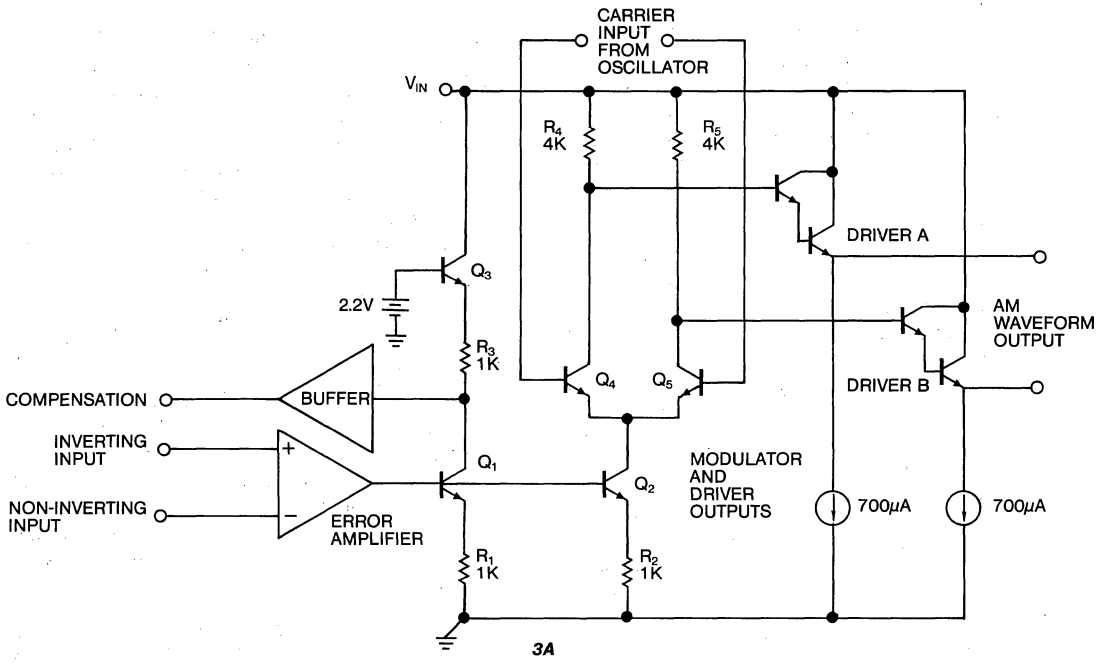


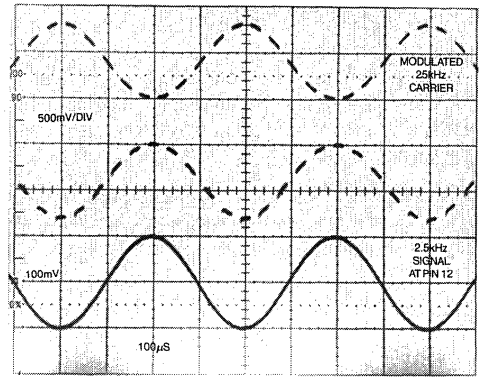
FIGURE 3: The Compensation Output on the UC1901 can be used to Accurately Control the AM Waveform Output. A Simplified Schematic, (a) Shows the internal Signal Split into the Modulator. Voltage Waveforms, (b) Across the Modulator Outputs, and at the Compensation Output show the Modulator Transfer Characteristic.

zation with a system clock, or reference frequency. In many situations, operation of the UC1901 at the switching frequency of the power supply can be beneficial. One such application is presented in this article. To accommodate this need the UC1901 has an external clock input.

One additional mode of operation is possible if the oscillator is left disabled and the external clock signal is kept low (or floated). In this condition the error amplifier can be used in a linear fashion with its output taken at the driver A output. The driver B output will be at a fixed DC voltage about 1.4V from the input supply voltage. If the external clock signal is tied high the roles of the two driver outputs are reversed. With 15mA of output current capacity, the two outputs can easily be combined to reference and drive an optical coupler. Although the instabilities of the coupler will still be present, the advantages of the UC1901's precision reference, high gain amplifier-driver, and 4.5V supply operation can be utilized.

3. A Controlled Feedback Response

There are many different topologies which can be used when implementing a switching power supply. For off-line supplies, fly-back and forward converters are often designed. In the near future current-mode control versions of these may also be widely used. Each of these converter topologies has a different forward transfer characteristic and, within each type of converter, operating point, continuous or discontinuous inductor current, and voltage or current-mode duty cycle control are a few of the factors which can alter this characteristic. In short, the task of optimally designing a feedback network for one supply must usually be repeated when the next supply is designed.



3B

Once the forward transfer function of a particular converter has been determined, various factors such as stability, line regulation, load regulation, and transient response will determine the overall loop response, and therefore feedback response, required. One of the objectives of the UC1901, in addition to allowing a controlled isolated feedback response, is to make the task of implementing a given response as easy as possible. With the compensation node on the UC1901, local R-C feedback networks can be used to shape the small signal gain and phase frequency response of the overall feedback network.

The error amplifier on the chip has a typical open loop gain of 60dB and is internally compensated to have a unity gain bandwidth of just above 1MHz. Both of these characteristics are measured with respect to the compensation node (Pin12). As shown in Figure 3a, the amplified error signal is internally split, at the collectors of Q_1 and Q_2, and fed to both the modulator and the compensation output. Applying feedback from the compensation output to the error amplifier's inverting input controls the small signal collector current through Q_1. Since Q_2 sees the same base voltage, and its emitter resistance is the same, its collector current will track that of Q_1. The collector current of Q_2 feeds the modulator and determines the amplitude of its output signal. The 4-to-1 ratio of resistors R_4 (or R_5) and R_2 results in a fixed 12dB of small signal gain measured as the ratio of the amplitude of the differential signal at the modulator outputs to the compensation mode signal. This relationship, as well as the function of the modulator, is shown in Figure 3b. The scope traces show a 200mV peak to peak sinusoid at 2.5kHz, measured at the compensation output, and the resulting 800mV variations in the peak amplitude of a 25kHz square wave carrier as measured across the modulator's differential output.

The remaining factors influencing the response of the feedback path are the signal gain through the transformer, the detector circuit, and the circuitry between the detector output and the supply's PWM. The signal gain through the transformer is simply the turns ratio of transformer. The small signal detector gain can usually be assumed to be unity as long as the AC load presented to the detector is kept small. Some load on the detector is necessary to allow its output to slew in a negative direction. Figure 4 summarizes the transfer and output characteristics of a typical transformer and detector.

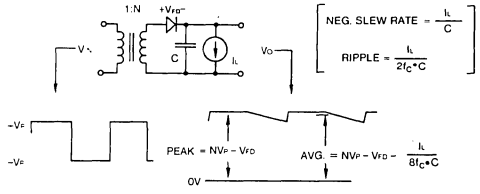


FIGURE 4: A Typical Detector Model and its Output Characteristics.

Here the load on the detector is modeled as a current source, simplifying the equations. In actual practice the operating point of the detector output will be determined by the circuitry which interfaces it with the PWM input. Since the minimum recovery from the detector is zero volts a nominal positive operating level which provides adequate dynamic range for DC and transient conditions should be chosen.

The UC1901 is specified to generate maximum carrier levels equal to or in excess of 1.6V peak. This indicates that a turns ratio of greater than one-to-one will be required for the coupling transformer if the detector output must exceed approximately 1V, (allowing for a detector diode drop of 0.6V). It should be noted that many switching power supplies now being designed include an integrated PWM control IC. A typical PWM IC includes a dedicated error amplifier which amplifies and buffers the input error voltage and applies it to the PWM ramp comparator. This amplifier can be readily used to fix a nominal detector operating point that is compatible with a one-to-one transformer. Additionally, the error amplifier on the UC1901 and the PWM's amplifier can be combined to achieve both large DC loop gains for improved load and line regulation, and the optimization of the loop gain and phase frequency response for improved transient and stability performance.

4. Transformer Requirements

The coupling transformer used with the UC1901 has two primary requirements. First, it must provide DC isolation. Secondly, it should transfer voltage information across the isolation boundary. Meeting the first requirement of DC isolation will depend on specific applications. In general, though, small signal transformers can be readily built to meet the isolation requirements of today's line-operated systems.

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For the most stringent applications, E-type cores with bobbin carried windings are inexpensively available or built. Where small size is most important, a simple toroid core can be used.

The second requirement of the transformer primarily determines the amount of magnetizing inductance it must have. The magnetizing inductance of a transformer refers to the actual inductance formed by the windings around the core material. In many classical transformer examples, the magnetizing inductance is ignored. This is a valid approximation since, in these examples, the magnetizing current required is much less than the reflected load currents. In this case, the load currents are small and, as the transformer inductance is reduced, the magnetizing currents become dominant.

The driver outputs on the UC1901 are emitter followers which are biased at 700μA. Therefore, if the drivers are operated without additional bias current the peak current through the transformer's primary winding cannot exceed this value. Figure 5a illustrates the relationship of the magnetizing current to the voltage across the transformer's input. If the reflected load currents are neglected, it can be seen that the minimum magnetizing inductance required for linear transfer of the modulator square-wave is given by:

$$(1) \qquad L_M \geq \frac{V_P}{4 f_c I_P}$$

Where:
- L_M = the magnetizing inductance,
- V_P = the peak carrier voltage across transformer inputs,
- f_C = the UC1901 operating frequency,
- I_P = the bias current of the UC1901 drivers.

As an example, consider the case where Vp is equal to 2V, f_c is 100kHz, and the drivers are operating at their internal bias levels. Using equation 1, the inductance looking into the primary winding with no secondary load must be greater than 7.1mH. Alternatively, if the carrier frequency is raised to 1MHz and the bias levels of the UC1901 drivers are increased to 3.5mA, then L_M can be as low as 150μH. Using high permeability ferrite material, this level of magnetizing inductance can be realized with as little as 10 turns on a small toroid core.

Equation 1 sets a minimum limit on the magnetizing inductance for linear transfer of the carrier wave-

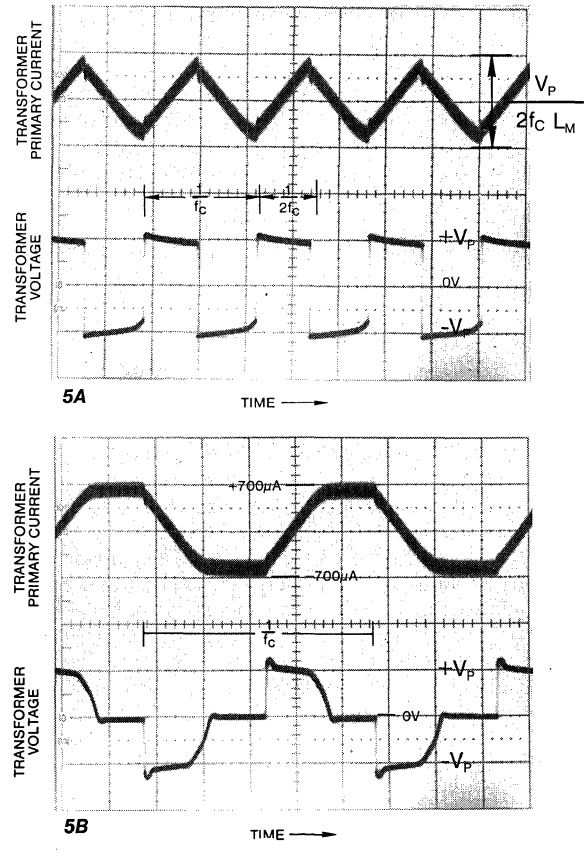

FIGURE 5: The UC1901 Driver Outputs Follow the Modulator Output Square Wave, (a.), Sourcing and Sinking Current Levels Dependent on Transformer Inductance, Carrier Frequency, and Voltage Level. When the Bias Level of the Driver Outputs, I_P, is Reached, (b.), a Tri-state Waveform is Coupled Across the Transformer, the Peak Voltage Level Though, Remains Approximately the Same. The Reflected Load Currents are Assumed Negligible.

form. Actually, the amplitude information is still coupled even when the inductance is less than this minimum. In this case, the UC1901 drivers will support the voltage across the coil until the peak current is reached. The result, illustrated in Figure 5b, is a tri-state waveform at the transformer's input and output. Peak detection of this waveform yields the same amplitude information as the linear transfer case, although detection ripple will increase. Another situation which results in a tri-state waveform exists when the carrier duty cycle is not 50%. In this case, the volt-seconds across the transformer will be balanced by an "imbalancing" of the driver

bias levels. The imbalance will be sufficient to cause the peak current to be reached during the >50% portion of the carrier waveform.

5. The High Frequency Oscillator

The oscillator circuit on the UC1901 is designed to operate at frequencies of up to 5MHz. To achieve this operating range the circuit shown in Figure 6 uses only NPN transistors in those parts of circuit which are dynamically involved in the actual oscillation. The standard bipolar process used to produce the UC1901 characteristically yields high f_T, typically 250MHz, NPN devices. Conversely, the same process has PNP structures with f_T's of only 1 to 2MHz. In the oscillator, PNP's are used only in determining quiescent operating points of the circuit.

The latched comparator formed by Q_1-Q_4, diodes D_1 and D_2, and resistors R_1 and R_2 has a controlled input hysteresis which determines the peak to peak voltage swing on the timing capacitor C_T. The timing capacitor C_T is referenced to V_{IN} since this is the reference point for the latched comparator's thresholds. The comparator's outputs at D_1 and D_2 switch the 2X current source through Q_{10} changing the net current into the timing capacitor from positive to negative, reversing the capacitor voltage's dv/dt. When the resulting ramp reaches the comparator's lower threshold, the current is switched back to Q_{11} and the ramp reverses until the upper threshold is reached and the process begins again. This results in a triangle waveform at C_T and a squarewave signal at D_1 and D_2.

The magnitude of the charging current is controlled by the external resistor, R_T and the internally generated voltage across it. This voltage is compensated to track variations in the comparator hysteresis. The tracking characteristics of this voltage stabilize the oscillation frequency over temperature and enhance the initial frequency tolerance. Typically, repeatability and temperature stability of the operating frequency are both better than 5%.

The oscillator circuit has been optimized for a nominal R_T of 10kΩ. A desired operating frequency is obtained by choosing the correct value for C_T. As shown in Figure 7, the oscillator frequency is give by the relation:

$$(2) \qquad fosc. = \frac{1.24}{R_T C_T},$$

for frequencies below 500kHz. Above 500kHz, the solid line indicates appropriate C_T values. There is

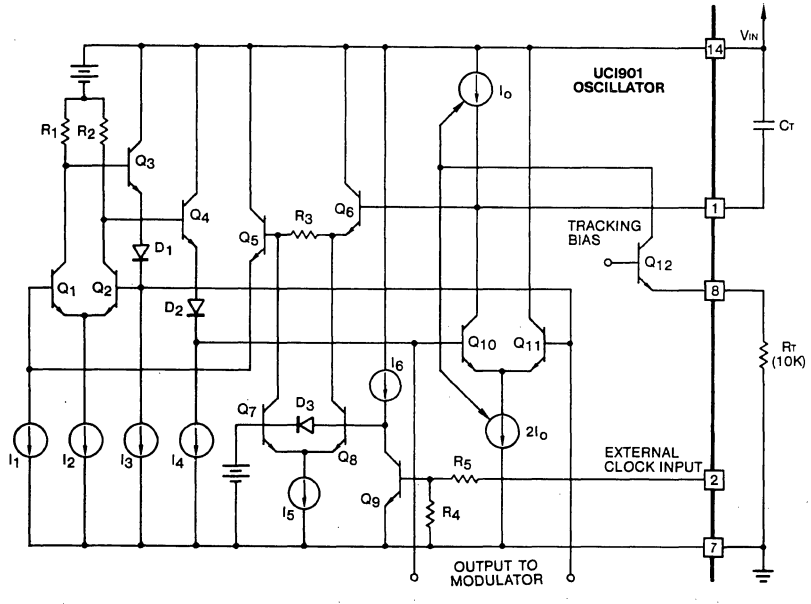

FIGURE 6: UC1901 High Frequency Oscillator Simplified Schematic.

no upper limit on the size of the capacitor used, thus allowing the oscillator to have an arbitrarily long period if desired.

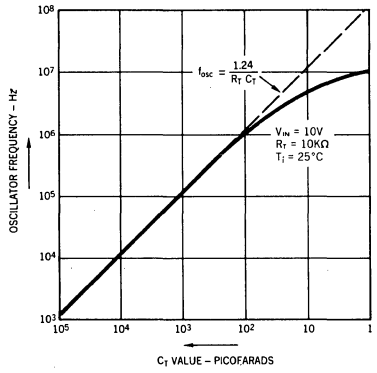

FIGURE 7: UC1901 Oscillator Frequency.

To allow operation of the modulator with a carrier frequency that is driven from a system operating frequency or clock, the oscillator can be over-ridden. Tying C_T to the input supply voltage disables the oscillator. The modulator circuit can now be switched in synchronization with a signal at the external clock input. Internally, the clock signal is applied to the latched comparator via the input device Q_9, and the differential pair Q_7 and Q_8. As the clock input goes high, Q_9 turns Q_8 off and Q_7 on, creating an offset across R_3 that is sufficient to switch the comparator. The comparator then, as before, drives the modulator. When the clock input returns low, the process is reversed. Using the external clock input, both the frequency and duty cycle of the modulator outputs are controlled.

6. A Status Output is More Than Just a Green Light

Many systems today require a monitoring function on the supply output. The status output on the UC1901 can fill this need, a green light function, and can also be used to fill some more "sophisticated" needs. The circuit in Figure 8 takes advantage of the status output in the start-up of an off-line forward converter. The UC1901 is being used in an application where the switching supply must be synchronized to a system clock. The clock signal is generated on the secondary or output side of the supply. To allow start-up, the PWM oscillator is free-running when the line voltage is applied. As the supply voltage rises, the UC1901's external clock input is driven at the switching frequency rate through resistors R_1 and R_2. When the supply output

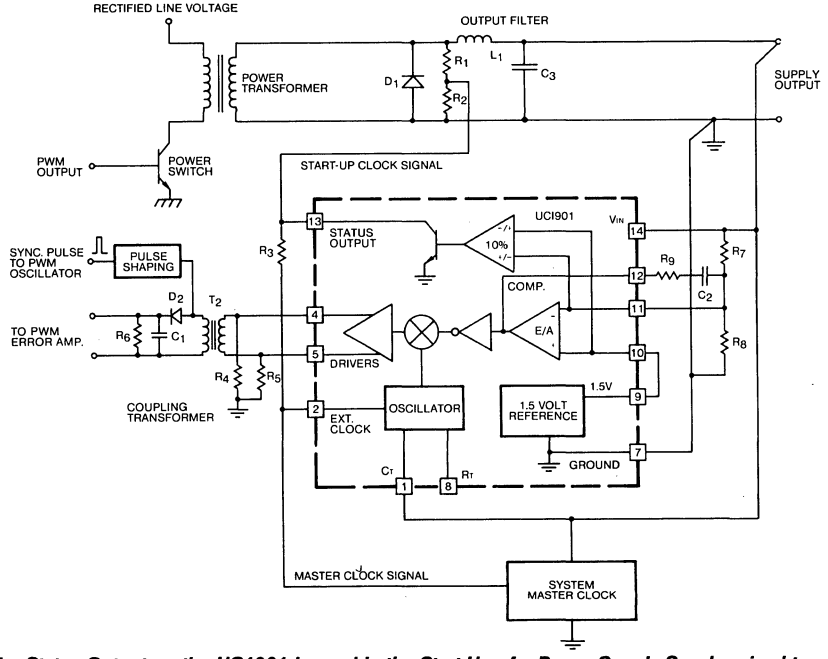

FIGURE 8: The Status Output on the UC1901 is used in the Start-Up of a Power Supply Synchronized to a Secondary Referenced Master Clock. The Coupling Transformer Carries the Feedback and Clock Signals. The Status Output is used to Sequence Clock Signals to the UC1901 External Clock Input During Start-Up.

reaches 90% of its operating level, the status output decouples the external clock input from the switcher and enables the UC1901's clock input to be driven from the now operational system clock.

On the primary side, the output of the coupling transformer is used before demodulation to provide a synchronization pulse to the PWM control oscillator. Under normal operation, the entire power supply, including the feedback system, will be synchronized to the system clock.

7. The UC1901 in an Off Line Flyback Converter

As alluded to previously, flyback converters see wide use in off-line applications. The flyback topology has some general cost benefits which have spurred its use in low cost, low power (<150W), off-line systems. Perhaps the two most significant of which are the need for only a single power magnetic element in the supply (no output filter inductor is required), and the ability to easily obtain multi-output systems by adding one additional winding to the coupling power inductor for each extra output. Also, the flyback topology, especially when used in the discontinuous mode, lends itself very well to the benefits of voltage feed-forward.

7a. 60 Watt Dual Output Converter

Shown in Figure 9 is a flyback converter designed with the UC1901 and a primary side control IC, the UC1840. The converter has two 30W outputs, one at 5V/6A, and another at 12V/2.5A. Minimum loads of 1A are specified at each output. The UC1901 is used to sense and regulate the 5V output. This output is specified at ±2 percent (untrimmed), with load and line regulation of better than 0.2 percent. Respectively, the 12V output is specified at ±5 percent with ±6 percent load and line regulation. Regulation of the 12V output relies on close coupling between the 5V and 12V output circuits.

The UC1840 controller has all of the features discussed previously for an off-line controller. In addition, it has some advanced fault protection features. Only parts of the UC1840's capabilities are discussed here. For those desiring a more complete description, it can be found in the second reference mentioned at the end of this article. In the supply, the UC1840 sequences itself through start-up using the energy stored in C_4 by the trickle resistor R_{11}. Once the supply is up and running W_4, the auxiliary winding on L_1, provides power to the controller and the switch drive circuitry. The primary winding on the coupled inductor, W_1 is applied across the rectified and filtered line voltage at a 60kHz rate via the FET switching device. L_1 is referred to as a coupled inductor, rather than as a transformer, since the primary and secondary windings do not conduct at the same time. Energy is stored in the inductor core as the switching device conducts, and then "dumped" to the secondary outputs when the device is turned off.

The converter operates in the discontinuous mode. Operating in this mode, the total current in the coupled inductor goes to zero during each cycle of operation. In other words, the energy stored in the core during the beginning of a cycle is entirely expended to the load before the end of the cycle. This allows the inductor size to be minimized since its average energy level is kept low. The price paid for discontinuous operation is higher peak currents in the switching and rectifying devices. Also, high ripple currents at the supply's output(s) make ESR, (equivalent series resistance), requirements on the output filter capacitors more stringent.

7b. Discontinuous Flyback's Forward Transfer Function

The process of designing a feedback network for the supply begins with determining the small signal transfer function of the converter's forward control path. This path can be defined as the small signal dependency of the output voltage, V_{OUT}, to, V_C, the control voltage at the input to the PWM comparator. As defined, the control voltage on the UC1840 appears at the compensation output of its internal error amplifier. The transfer function of this path for the discontinuous converter is given by equation (3).

$$(3)\quad \frac{V_{OUT}}{V_C}(s) = \frac{V_{IN}}{V_R}\sqrt{\frac{T_P R_L}{2L_M}} \cdot \frac{1 + sC_F R_S}{1 + \frac{sC_F R_L}{2}}$$

Where:

V_{IN} = level of the rectified line voltage,

V_R = The equivalent peak PWM ramp voltage-equal to the extrapolated control voltage input which would result in a 100% switch duty cycle,

T_P = One period of the switching frequency,

L_M = Magnetizing inductance of the primary winding,

C_F = A total effective output filter capacitor,

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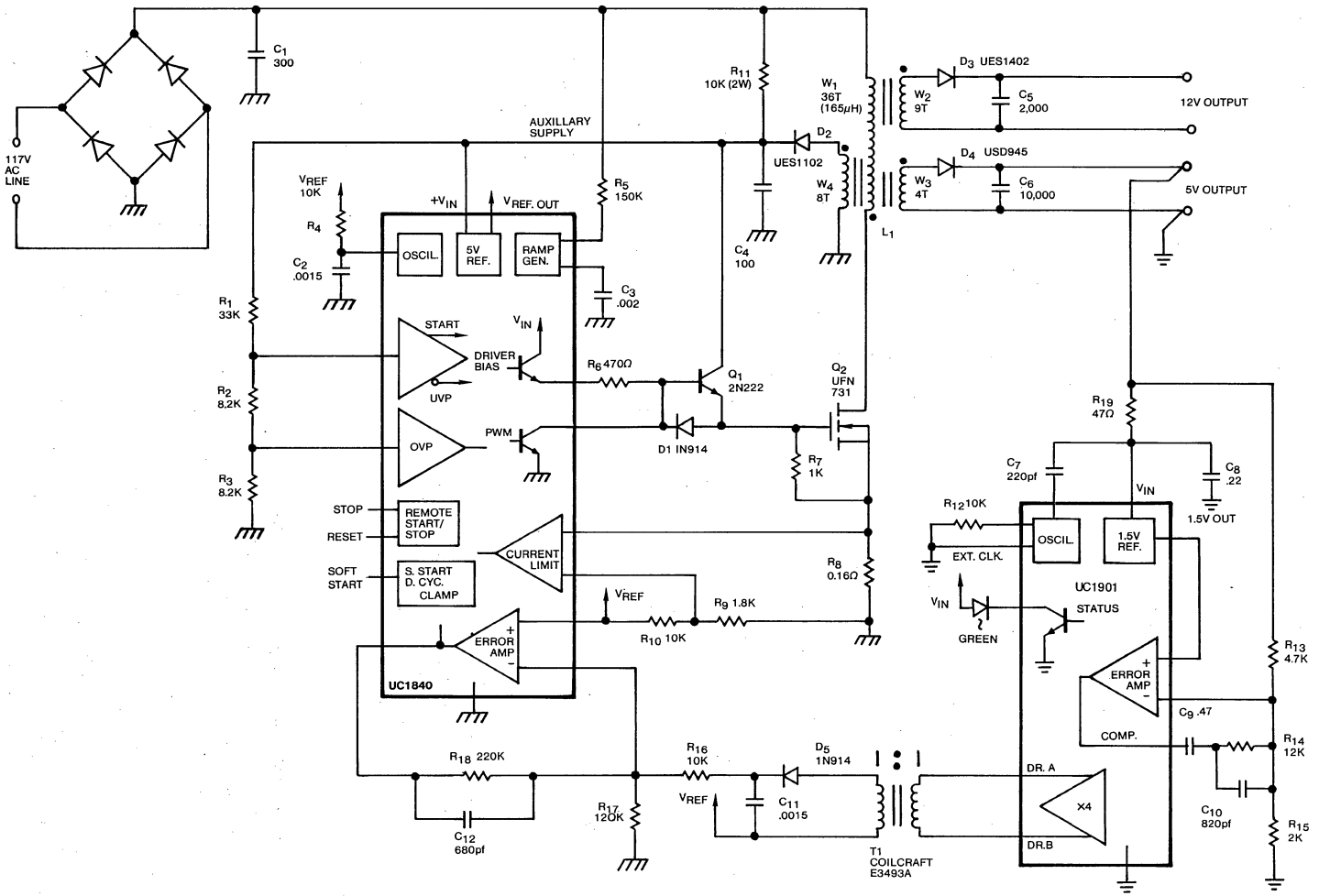

FIGURE 9: The UC1901 Combines With an Advanced PWM Controller in a 60W Off-Line Converter.

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R_L = The total effective load, (assumed resistive),
R_S = ESR of the filter capacitor,
s = $2\pi jf$, f is frequency in hertz.

The word effective is used in describing R_L and C_F since, although we are interested in calculating the response to the 5V output, the loads at the 12V and auxiliary outputs must be accounted for. This is easily done by reflecting these loads to the 5V output using the corresponding turns ratio on the inductor.

7c. Voltage Feedforward Steadies Response

Equation 3 indicates a substantial dependency of the control response to both the load R_L, and the input voltage, V_{IN}. This can slightly complicate the design of the feedback network since both the gain and phase response of the loop will vary with operating conditions.

The benefits of feed-forward are easily illustrated at this point by examining its effect in this circuit. The UC1840 controller uses resistor R_5 to sense the input voltage and proportionately scale the charging current into the PWM ramp capacitor, C_3. Scaling the ramp slope is the same as scaling V_R, the equivalent peak ramp voltage. The result is a modeled ramp voltage given by:

$$(4) \qquad V_R = \frac{V_{IN}\, T_P}{R_5\, C_3}$$

When this expression for V_R is substituted into equation 3, the result is a forward transfer function that is independent of the input voltage. Not only does this simplify the feedback analysis, it also vastly improves the supply's inherent rejection of line voltage variations.

The forward response of the converter, plotted in Figure 10, has a single pole roll-off occurring between 11Hz and 38Hz depending on the load. The single pole roll-off allows the feedback network a bit of latitude since, from a stability standpoint, the loop bandwidth can be extended by simply adding broadband gain with an appropriate roll-off frequency. No mid-band zeros or led-lag networks are necessary, as might be for converters with double pole responses. Although, the zero resulting from the ESR of the filter capacitors can, if not taken into account, appreciably extend the loop bandwidth beyond its intended value.

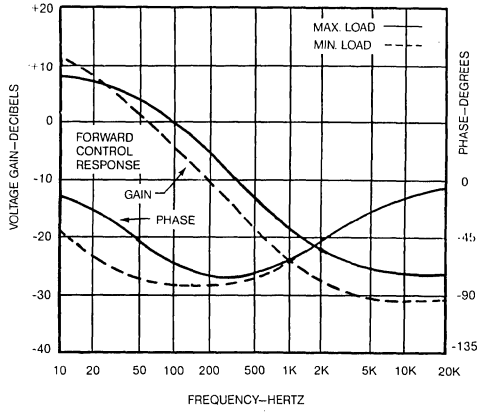

FIGURE 10: Closing the Feedback Loop is Preceeded by the Characterization of the Converter's Forward Small Signal Transfer Function.

7d. Wide Bandwidth Gives Fast Transient Response At 5V Output

This supply was designed to have a unity gain loop bandwidth of between 5 and 10kHz. With this bandwidth the supply's control response to step load and line changes occurs in fractions of a millisecond. This is only true with regard to the 5V output. There is no feedback from the 12V output therefore the output impedence of the 12V supply will be determined by IR losses, the dynamic impedence of the rectifying diodes, and the coupling efficiency between the inductor windings. This impedence is not reduced by the loop gain, as it is at the 5V output. As a result, the time constant of the response at this output will be considerably longer.

The fast response of the 5V output and the relatively slow response of the 12V output are illustrated in Figure 11 which shows three oscilliscope traces in response to a 3.0A load change at the 5V output. The upper trace is the response of the 5V output

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which has been expanded and lowpass (< 15kHz) filtered slightly so the small signal loop characteristics can be seen. The trace below this is the 12V output's deviation due to cross-regulation limitations, the longer time constants involved are obvious. Both the fast response of the 5V loop, and the longer settling time of the 12V output are apparent in the third trace. This trace is the fed back correction signal at the UC1840's error amplifier output. From the middle trace the output impedence of the 12V supply can be estimated by noting the approximate 1ms time constant and dividing it by the 2000μF value of the 12V output filter capacitor. This gives a value of 0.5Ω for the output impedence. This agrees well with actual measurements of the 12V output's load regulation.

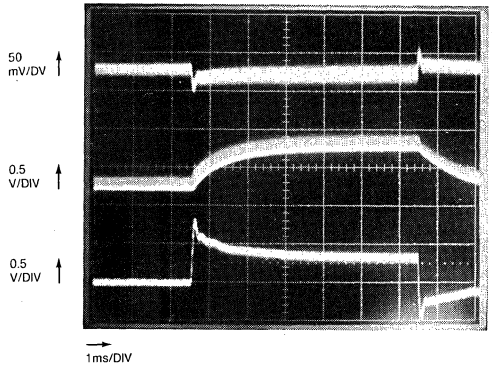

FIGURE 11: The Transient Response of the 5V Output (Top Trace), to a 3.0A Step Load Change Reflects the Extended Bandwidth of the 5V Loop. The Open-Loop 12V Output (Middle), Responds to the Effects of Cross Regulation. The Feedback Error Signal (Lower) Coupled Through the UC1901 is Measured at the UC1840 Error Amp. Output.

7e. The Feedback Response

Plotted in Figure 12 is the response of the feedback network. Also plotted are the asymptotic gain lines of the two contributing gain blocks, the UC1901 response (from 5V output to detector output) and the UC1840 error amp response (detector output to the PWM control voltage). The UC1901's error amplifier is run open loop at DC but is quickly rolled off to 8dB. With the 12dB of modulator gain, the UC1901 feedback system has a broadband gain of 20dB. A pole at 16kHz is added to reduce the gain through the UC1901 error amplifier at the 60kHz switching frequency. As mentioned earlier, excessive gain at the switching frequency can "use up" the dynamic range of the UC1901's AM output.

The UC1901 is operated with a carrier frequency of 500kHz. The coupling transformer, a Coilcraft E3493A, (double E core, bobbin wound construction), has a magnetizing inductance of 2.1mH. At 500kHz the peak current required to drive the primary winding is only 475μA per peak volt. The reflected load current is kept much smaller. This allows the transformer to be easily driven from the UC1901 driver outputs. The E3493A is widely used as a common mode line choke, and is rated for V.D.E. and U.L. isolation requirements. The transformer has a current rating of 2A, greatly exceeding the requirements of this application. Even though the device is larger than some alternatives, its availability and high volume pricing, as well as its isolation capability, make it a very suitable choice.

At the output of the transformer the diode-capacitor detector is referenced, along with the inverting input of the UC1840 error amplifier, to the UC1840's 5V reference. The operating point of the detector is fixed at 0.5V by the divider formed by R_{16} and R_{17} in Figure 9. This in turn sets the operating point of the carrier, with a detector diode drop of 0.5V, at about 1V peak. This level is reflected back through the one-to-one transformer to the UC1901 outputs. A 1V operating point is approximately at the center of the devices dynamic range.

The load current at the detector output is 50μA, set by the 0.5V operating level and R_{16}. The peak to peak detector ripple, at 500kHz, across the .0015μF holding capacitor is about 35mV. The gain through the UC1840 error amplifier at 500kHz is -26dB,

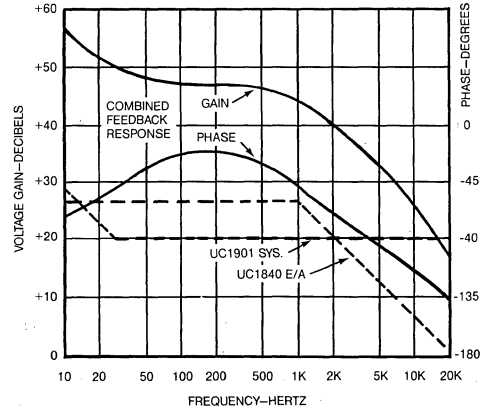

FIGURE 12: Local Feedback Around the UC1901 and 1840 Error Amplifiers is Used to Obtain the Desired Feedback Response.

attenuating the ripple to less than 2mV at the error amplifier output.

The response of the UC1840 error amplifier is flat out to 1kHz where the gain is rolled off to set the loop's 0db frequency. The DC gain is kept as high as possible, to fix the detector operating point, without actually having a series integrating capacitor in the feedback. If both the UC1901 and the UC1840 error amplifiers are run open loop at DC, with series R-C networks to set the AC gain, the total phase margin at low frequencies can become small or nonexistent. The result can be instability or, more likely, a peaked closed loop response that can increase the low frequency noise level of the supply.

The distribution of gain between the UC1901 and UC1840 error amplifiers is somewhat, although not entirely, arbitrary. Keeping the 500kHz ripple at the PWM comparator input below a certain level puts restrictions on the AC gain of the PWM's error amplifier. To much AC gain through the UC1901's amplifier can degrade the supply's transient response under large signal conditions. A suitable distribution for any application will, more than likely, be an iterative procedure. A simple computer or programmable calculator program can be a great tool when massaging these aspects of a design.

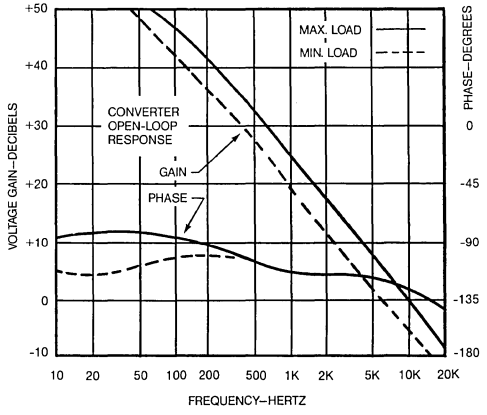

FIGURE 13: The Over-All Open-Loop Response of the Supply Will Determine the Supply's Over-All Stability and Small Signal Transient Response.

The overall open-loop responses, plotted in Figure 13, will not vary significantly except as indicated with load. The desired loop bandwidth has been achieved with an adequate phase margin of $>50°$.

The result is a supply with very repeatable, as well as stable, operating characteristics. The same type of analysis for determining the required feedback response can be used in applying the UC1901 to any type of isolated closed loop supply. The choice of coupling transformer and carrier frequency used with the UC1901 should be based on individual system requirements.

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VERSATILE UC1834 OPTIMIZES LINEAR REGULATOR EFFICIENCY

Linear voltage regulators have long been an important resource to power supply designers. Three terminal, fixed-voltage linear regulators find extensive use as "spot" regulators and as post-regulation stages fed by switched-mode supplies. However, while inexpensive and simple to use, these devices have several performance limitations.

First, three terminal regulators are inefficient power converters. Power dissipation in a linear regulator is given by the relation:

$$P = I_O \cdot (V_{IN} - V_{OUT}).$$

Most monolithic regulators now available require an input-to-output voltage differential of at least 2 to 3V. This requirement can result in substantial inefficiency, particularly in low voltage supplies. As switched-mode power technology matures, power losses incurred in linear post-regulation stages are becoming more significant in terms of overall system efficiency.

Second, fixed-voltage regulators, with fixed maximum output currents, lack versatility. The use of these devices requires that OEMs maintain large, diverse inventories in order to support a broad range of power supply requirements.

Third, fixed three-terminal devices lack the capability of remote voltage sensing, and therefore can exhibit poor load regulation.

Finally, the most common failure mechanism for linear regulators is a shorted pass transistor. All critical loads, therefore, require over-voltage protection not provided by three-terminal regulators.

IMPROVED PERFORMANCE WITH UC1834

The UC1834 is a programmable linear regulator control IC which, with an external pass transistor, forms a complete linear power supply. This IC provides solutions to all the above-mentioned drawbacks of three-terminal devices.

Figure 1 shows the basic elements of positive and negative regulators implemented with the UC1834. An error amplifier monitors the output voltage and provides appropriate bias to the pass transistor (Q1) through a driver stage. This high-gain error amplifier (E/A) allows good dynamic regulation while allowing Q1 to operate near saturation in the common-emitter mode. The circuits can achieve high efficiency by maintaining output regulation with an input-to-output voltage differential as low as 0.5V (at 5A).

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The UC1834 has both positive and negative reference voltage outputs, as well as a sink-or-source driver stage, as shown in Figure 1. These features allow implementation of either positive or negative regulators with this single IC, as shown. Output voltages from 1.5V to nearly 40V can be programmed by appropriate choice of remote sensing divider elements. Remote sensing also allows improved DC and dynamic load regulation.

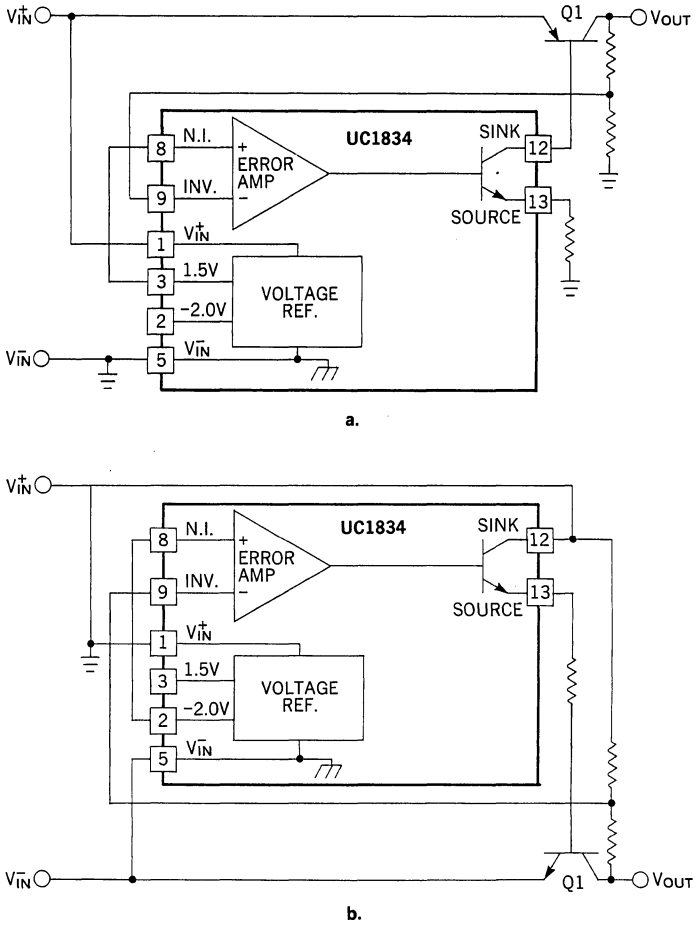

Figure 1. Basic Elements of (a.) Positive and (b.) Negative Regulators implemented with a UC1834

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The UC1834 is intended to provide a complete linear regulation system. Therefore, many auxiliary features are included on this IC which eliminate the need for additional circuit elements. Figure 2 shows a more complete block diagram including on-chip provisions for current sensing, fault monitoring, remote voltage sensing, and thermal protection.

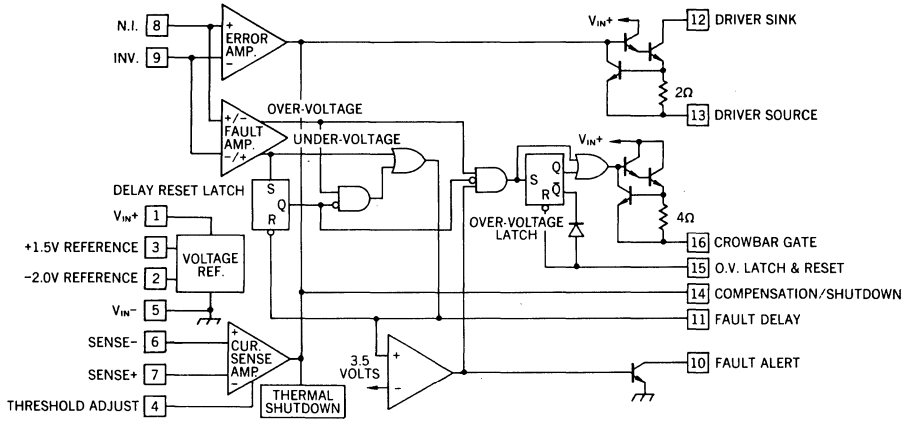

Figure 2. UC1834 Block Diagram

DRIVING THE PASS TRANSISTOR

Figure 3 shows suggested pass transistor configurations for implementing either positive or negative regulators with the UC1834. For those low current (≤200mA) applications in which efficiency is not extremely critical, the UC1834 output transistor can serve as the pass element, resulting in the simple configurations of Figure 3a. An external pass transistor is needed for output currents greater than 200mA. With the circuits of Figure 3c, the UC1834 can maintain regulation while operating the pass transistor near saturation. Operation at very high output currents (to ~30A) is possible with the Darlington pass elements of Figure 3d.

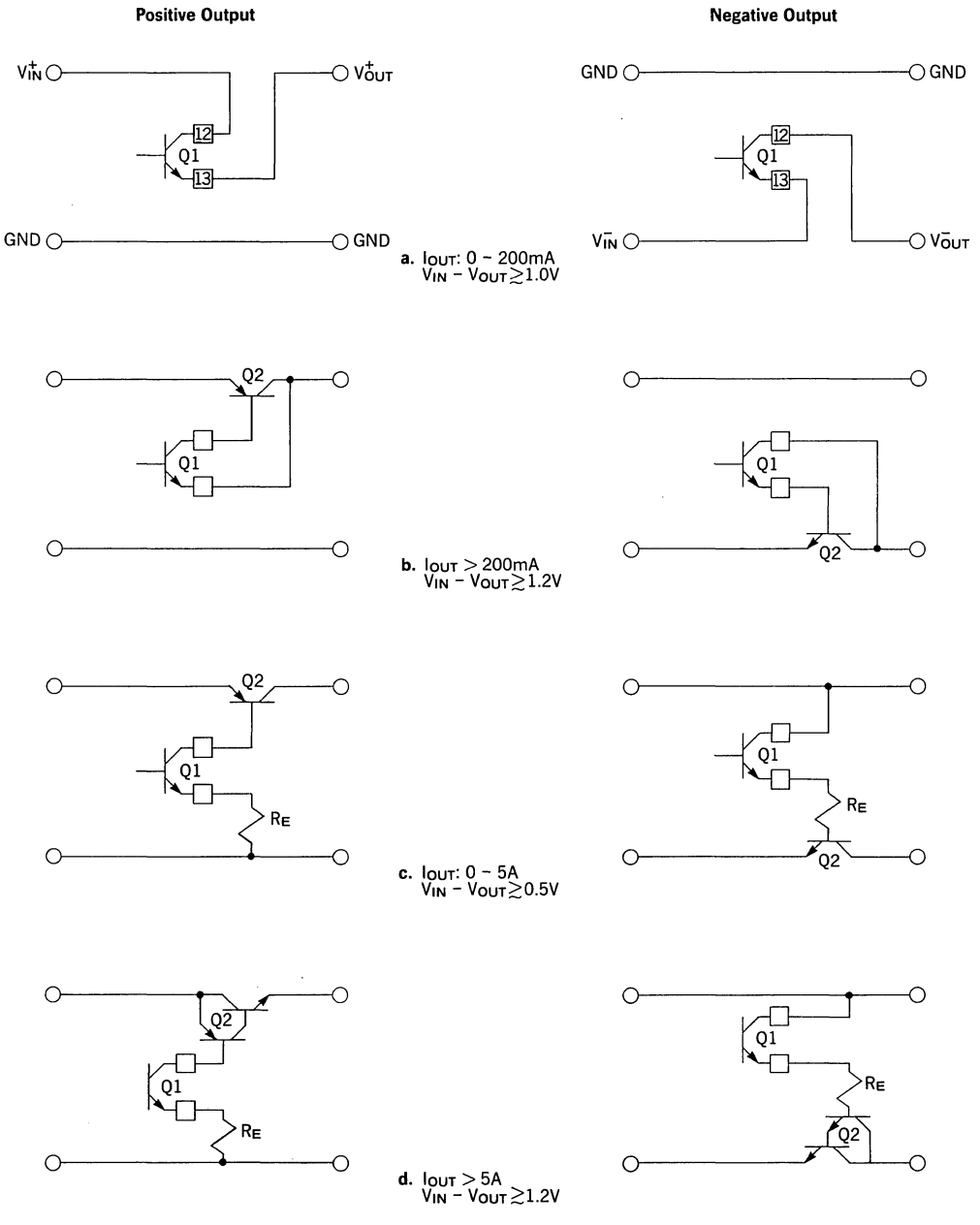

Figure 3. Pass Transistor Configurations

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Current in the UC1834 output transistor is self-limiting, for improved reliability. This limiting is achieved by Q3 and R1 in Figure 4a. The resulting maximum output current is a function of temperature as shown in Figure 4b.

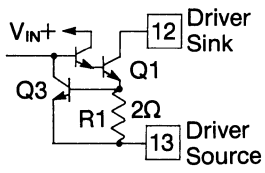
A resistor (R_E) is shown in series with the drive transistor in Figures 3c, d. This resistor shares base-drive power with the transistor, allowing cooler, more reliable operation of the IC. R_E should be as large as possible while still supporting adequate pass transistor base current under worst-case conditions of low input voltage and maximum output current:

$$V_{R_E(min)} = V_{IN(min)} - V_{BE(max)(Q2)} - V_{CE(sat)(max)(Q1)}$$
$$I_{B(max)(Q2)} = I_{O(max)} / \beta_{(min)(Q2)}$$
$$R_{E(opt)} = V_{R_E(min)} / I_{B(max)(Q2)}$$

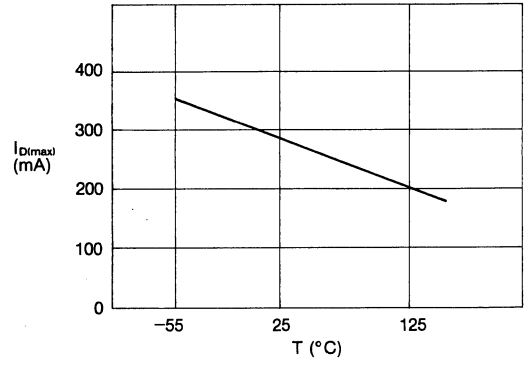
where: $V_{R_E(min)}$ is minimum voltage available to R_E
$I_{B(max)\ (Q2)}$ is maximum required base drive to Q2
$R_{E(opt)}$ is optimum value of R_E.

R_E also enhances stability by allowing operation of Q1 as an emitter-follower, thereby eliminating β_{Q1} from the loop transfer function:

$$I_{C(Q1)} \approx I_{E(Q1)} = (V_{E/A\ out} - V_{BE(Q1)} - V_{BE(Q2)}) / R_E \quad (\beta \text{ independent}).$$



a.



b.

Figure 4 a. Driver Current Limiting Circuit
b. Resulting Maximum Current vs Temperature

CURRENT SENSING

In order to protect the pass transistor from damage due to overheating, one must sense its emitter current (I_E) and then decrease the base drive if I_E is excessive. The UC1834 current sense amplifier (CS/A) accomplishes these tasks.

The UC1834 CS/A has a common mode range which includes both input supply "rails". This extended range is made possible by introducing matched voltage offsets in the differential input paths, as shown in Figure 5. Internal current sources bias the offset diodes in their appropriate direction. Which bias source (+ or -) is active is determined by whether the CS/A positive (+) input is greater or less than $V_{IN}/2$. Therefore, it is advisable to configure the sensing circuit such that the voltage at CS/A(+) will not cross $V_{IN}/2$ during operation. This precludes sensing in series with the load for most applications.

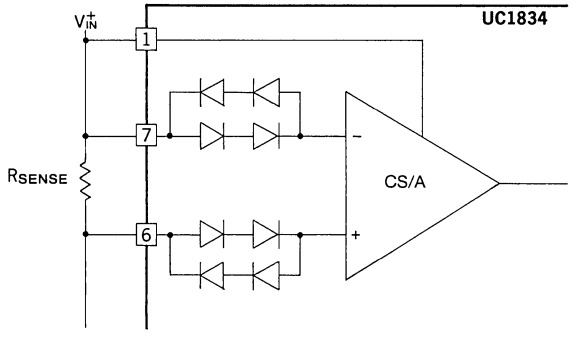


Figure 5. Two Diode-Drop Offset Allows Current Sensing at Supply Rail

The CS/A has a programmable current limit threshold which can be set between 0mV and 150mV. Programming is achieved by setting the voltage at the "Threshold Adjust" terminal (pin 4) to $10 \cdot V_{TH(desired)}$. The factor of 10 provides good noise immunity at pin 4 while allowing low power dissipation in the current sensing resistor. Figure 6 shows the guaranteed relationship between V_{PIN4} and the actual resulting threshold across the CS/A inputs. Note that the threshold is clamped at 150mV if pin 4 is open or if $V_{PIN4} > 1.5V$. The "Threshold Adjust" input is high impedance (bias current is less than $10\mu A$), allowing simple programming through a voltage divider from the 1.5V reference output. However, loading the 1.5V reference will affect the regulation of the -2.0V reference. Figure 7 shows how to compensate for this loading with a single resistor when the -2.0V reference is needed.

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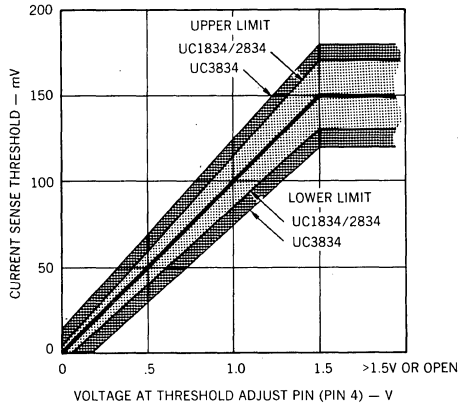

Figure 6. Guaranteed Tolerances on C/S Threshold Adjustment

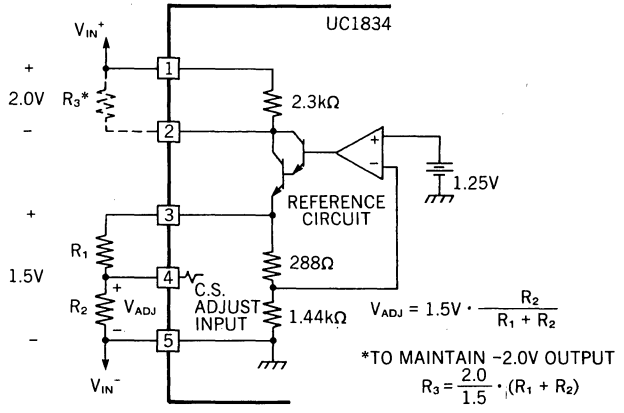

Figure 7. Setting the Current Threshold and Compensating the −2.0V Reference

The CS/A functions by pulling the E/A output low, turning off the output driver (Figure 8). As current approaches the threshold value, the E/A attempts to correct for the CS/A output, resulting in an E/A input offset voltage.The supply output voltage can decrease a proportional amount. When the CS/A input voltage differential reaches the current sense threshold, then the pass transistor is totally controlled by the CS/A. The combined CS/A and E/A gains and output configurations result in the current limit knee characteristic of Figure 9.

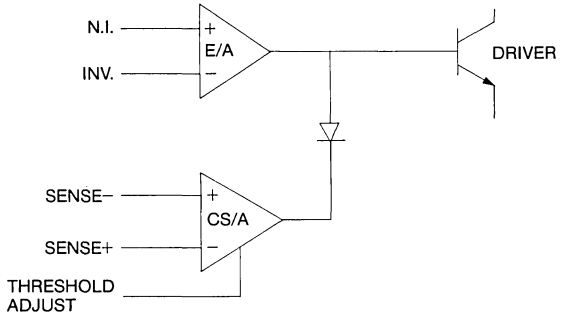

Figure 8. Current Sense Tied to E/A Output

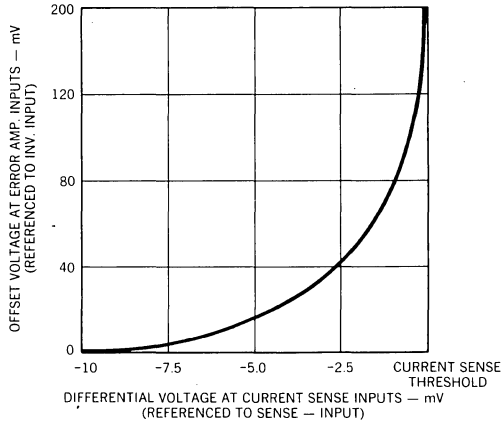

Figure 9. Current Limiting Knee Characteristic

FOLDBACK CURRENT LIMITING

It is desirable to put an upper limit on pass transistor power dissipation in order to protect that device. Ideally, for a constant power limit:

$I_{E(max)} \cdot V_{CE} \simeq K$ where K is a constant

or: $I_{E(max)} \simeq K/(V_{IN} - V_{OUT})$ (ignoring the sense resistor voltage drop).

As the input-to-out voltage differential increases, it is necessary to "fold back" the maximum allowable current. This ideal foldback characteristic is shown in Figure 10, along with a practical characteristic achievable with the circuit of Figure 11.

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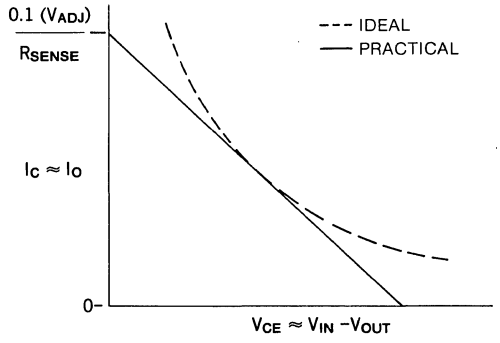

Figure 10. Ideal (Dashed Line) and Practical (Solid Line) Foldback Current Limiting Characteristics

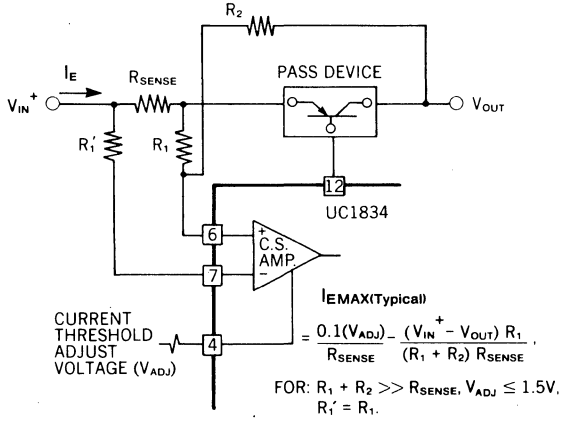

Figure 11. Foldback Current Limiting — Responds to Changes in V_{IN} or V_{OUT}

This circuit responds to changes in either V_{IN} or V_{OUT}. The voltage differential V_{IN} - V_{OUT} causes proportional current flow through R_1 and R_2. The additional drop across R_1 is interpreted by the CS/A as additional load current. The result is that the real current limit decreases linearly with V_{IN} - V_{OUT}:

$$I_{E(max)} = \frac{0.1(V_{ADJ})}{R_{SENSE}} - \frac{(V_{IN} - V_{OUT})\,R_1}{(R_1 + R_2)\,R_{SENSE}}$$

for: $R_1 + R_2 \gg R_{SENSE}$
$V_{ADJ} \leq 1.5V$
$R_1' = R_1$.

This technique can be susceptible to "latch-off". If a momentary short at the supply output causes I_E to drop to zero (pass transistor cut off), then V_{OUT} cannot recover when the short is subsequentially removed. To prevent this undesirable operation, one must ensure that $I_{E(max)} > 0$ when $V_{OUT} = 0$ and V_{IN} is at its minimum:

$$I_{E(max)} \Big|_{\substack{V_{OUT}=0 \\ V_{IN(min)}}} = \frac{0.1(V_{ADJ})}{R_{SENSE}} - \frac{(V_{IN} - V_{OUT})\,R_1}{(R_1 + R_2)\,R_{SENSE}} > 0$$

$$\frac{0.1(V_{ADJ})}{V_{IN(min)}} > \frac{R_1}{R_1 + R_2}$$

$$R_2 > \frac{V_{IN(min)}\,R_1}{0.1\,(V_{ADJ})}\left(1 - \frac{0.1\,(V_{ADJ})}{V_{IN(min)}}\right)$$

Figure 12 shows an alternative foldback current limiting scheme which responds to decreased V_{OUT} only. This circuit gives the output characteristics of Figure 13, defined by the following relation:

$$I_{E(max)} = \frac{0.1}{R_{SENSE}} \cdot \left(\frac{R_1R_2\,V_{OUT} + R_2R_3\,V_{REF}}{R_1R_2 + R_1R_3 + R_2R_3}\right)$$

This technique is immune to "latch-off" because the minimum current limit is always non-zero.

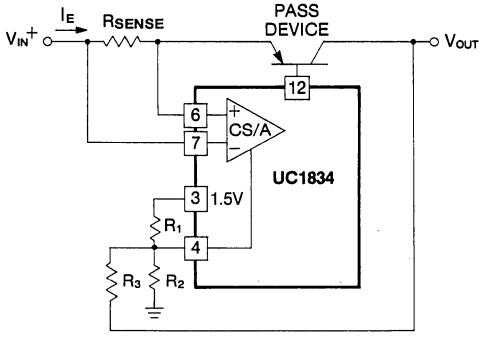

Figure 12. Foldback Current Limiting — Responds to Changes in V_{OUT} Only

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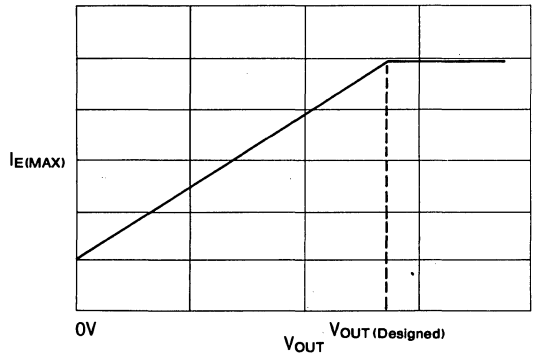

Figure 13. Foldback Current Limiting Characteristic

FAULT CIRCUITRY AND SYSTEM INTERFACING

In order to minimize the need for additional components, the UC1834 has on-chip provisions for fault detection and logic interfacing. These features are particularly useful when the linear regulator is part of a larger power supply system.

As shown in Figure 14, an internal comparator monitors the UC1834 E/A inputs. This comparator has two thresholds, for over- and under-voltage detection. Comparator thresholds are fixed at $|V_{N.I.} - V_{INV.}| = 150mV$. The resulting output voltage windows for non-fault operation are:

$$\frac{\pm .150V}{1.5V} = \pm 10\% \text{ for positive (+) supplies}$$

$$\frac{\pm .150V}{2V} = \pm 7.5\% \text{ for negative (-) supplies.}$$

A fault delay circuit prevents transient over- or under-voltage conditions (due to a rapidly changing load) being defined as faults. The delay time is programmable. An external capacitor at pin 11 is charged from an internal 75μA source. The delay period ends when the capacitor voltage reaches ~3.5V. The delay time is therefore ~47ms/μF. The fault alert output (pin 10) becomes an active low if an out-of-tolerance condition persists after the delay period. When no fault exists, this output is an open collector.

An over-voltage fault activates a 100mA crowbar gate drive output (pin 16) which can be used to switch on a shunt SCR. Such a fault also sets an over-voltage latch if the reset voltage (pin 15) is above the latch reset threshold (typically 0.4V). When the latch is set its $\overline{Q}$ output will pull pin 15 low through a series diode. As long as a nominal pull-up load exists, the series diode prevents $\overline{Q}$ from pulling pin 15 below the reset threshold. However, pin 15 is pulled low enough to disable the driver outputs if pins 15 and 14 are tied together. With pin 15 and 14 common, the regulator will latch off in response to an over-voltage fault. If the fault condition is cleared and pins 14 and 15 are momentarily pulled below the latch reset threshold, the driver outputs are re-enabled.

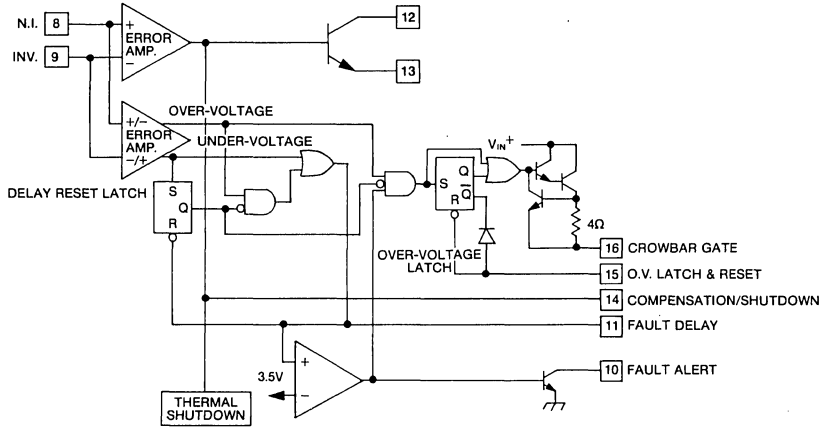

Figure 14. Fault Circuitry

An internal "delay reset latch" prevents crowbar turn-on when an under-voltage condition is immediately followed by a transient over-voltage condition. Such a situation could arise from a momentary short circuit at the supply output.

A thermal shutdown circuit pulls the E/A output low when junction temperatures reach 165°C, in order to protect the IC from excessive power dissipation in the drive transistor.

COMPENSATING THE FEEDBACK LOOP

A reliable design for any feedback system must yield a closed-loop frequency response which ensures unconditional stability. An optimum power supply response provides this stability while maximizing broadband gain for good dynamic voltage regulation with changing loads. Figure 15 illustrates such a response. The 0dB crossover frequency (f_c) should be as high as possible while maintaining phase margin above -360° at all lower frequencies (Nyquist stability criterion). In practice, this criterion dictates a single-pole response below f_c.

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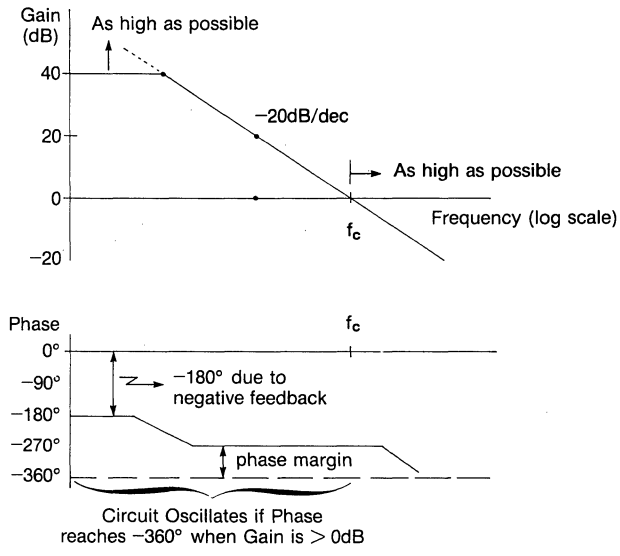

Figure 15. Desired Closed-Loop Response

Linear supplies using the UC1834 will usually have a current limiting loop in addition to the voltage control loop, as illustrated for two basic configurations* in Figure 16. Both loops must be stabilized for reliable operation. This is accomplished by appropriately compensating the E/A and CS/A at their common output (pin 14). Design of the compensation networks will often require an iterative procedure, since the compensation for one loop will affect the response of the other. A straightforward approach is outlined below:

1). Determine the frequency response of all voltage loop elements excluding the E/A. Appendix I offers guidelines for this step.

2). Design E/A compensation giving a frequency response which , when added to the response calculated in step 1, will yield a total loop characteristic consistent with the objectives outlined above. (Appendix II.)

3). Calculate the current loop response and determine whether it satisfies the Nyquist stability criterion. (Appendix III.) If not, add additional compensation and then recalculate the voltage loop response.

4). Iterate if necessary.

*All other configurations of Figure 3 are variants of these two, and can be treated in essentially the same ways.

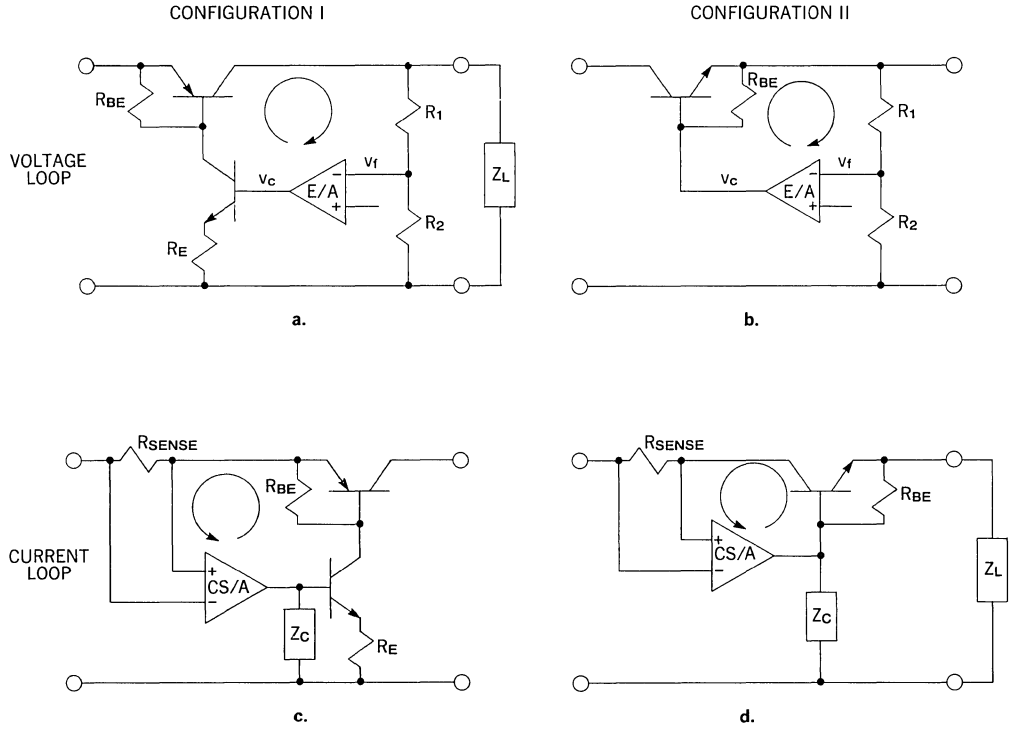

Figure 16. Voltage and Current Loops for Two Basic Configurations

EXAMPLE

Figure 17 shows a 5V, 5A (positive output) supply of the class shown in Figures 16a, c. This circuit tends toward instability when it is lightly loaded because of the high gain (β = 200) of the pass transistor at low currents. Output capacitor C_2 is needed to introduce a pole which rolls off the gain of the voltage loop to 0dB at 100kHz, avoiding instability due to the additional phase shift of a transistor pole at:

$$f = \frac{f_T}{\beta} = \frac{50\text{MHz}}{200} = 250\text{kHz}$$

Assuming a minimum load of 1A (R_L = 5Ω), the low frequency voltage loop gain, excluding the E/A, is (from Appendix I):

$$A_V = \frac{1}{15\Omega} \cdot 200 \cdot 5\Omega \cdot \frac{0.51\text{k}\Omega}{(1.7 + 0.51)\ \text{k}\Omega} = 20 = 26\text{dB}.$$

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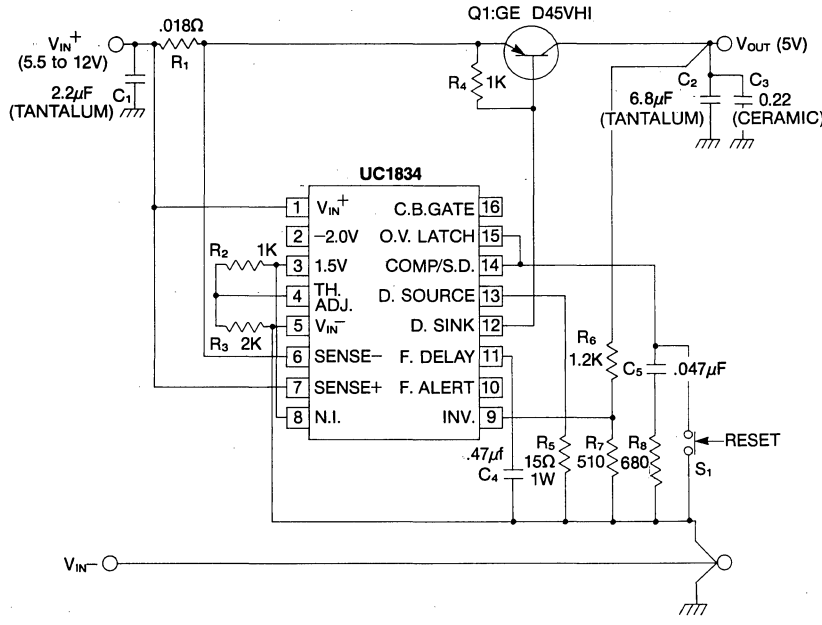

Figure 17. 0.5V Input-Output Differential 5A Positive Regulator

A pole at 5kHz is required in order to roll off from 26dB to 0dB at 100kHz. The required value of C_2 is therefore given by:

$$C_2 = \frac{1}{2\pi \cdot R_L \cdot f_p} = \frac{1}{2\pi \cdot 5\Omega \cdot 5kHz} = 6.4\mu F \text{ (6.8}\mu F \text{ used).}$$

The dashed curves of Figure 18a show the resulting voltage loop response, excluded the compensated E/A. Notice that the 5kHz pole (just added) itself introduces undesirable phase lag. This can be corrected by positioning the compensation zero (see Appendix II) at the same frequency. With $R_8 = 680\Omega$ (providing ~0dB E/A gain above 5kHz), then:

$$C_5 = \frac{1}{2\pi \cdot 680\Omega \cdot 5kHz} = .047\mu F.$$

The gain and phase of the compensated E/A (dotted lines) and complete voltage loop (solid lines) are also shown in Figure 18a.

The resulting current loop response (Figure 18b) is seen to meet the stability criterion. Gain above 5kHz is given by (from Appendix III):

$$A_I = \frac{1}{70\Omega} \cdot 680\Omega \cdot \frac{1}{15\Omega} \cdot 200 \cdot 0.018\Omega = 2.3 = 7.4dB.$$

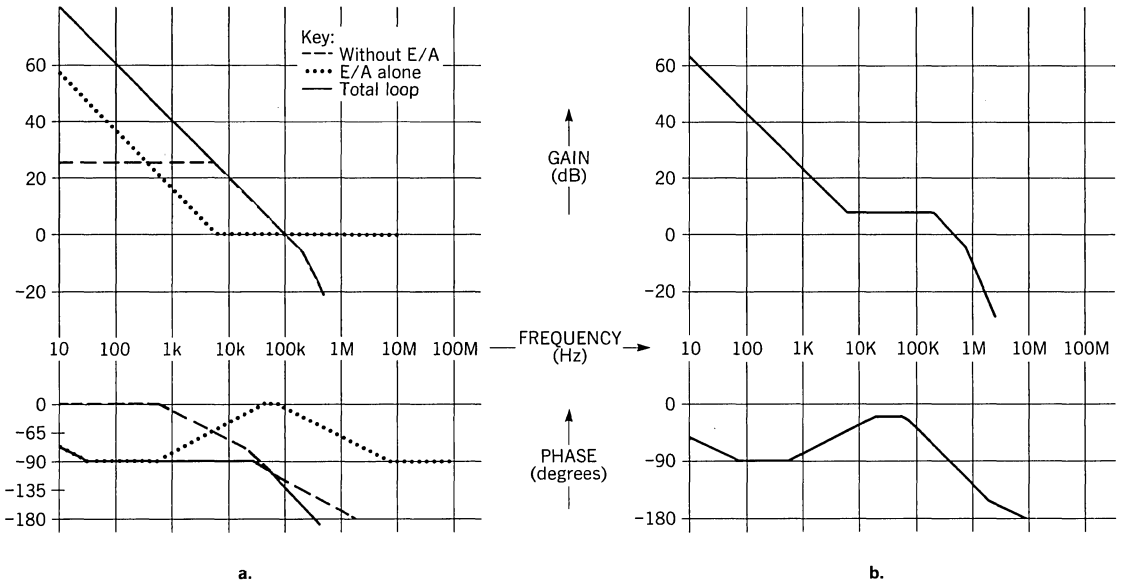

Figure 18. Loop Responses for Circuit of Figure 17
a. Voltage Loop
b. Current Loop

Reasonable phase margin (~40°) is maintained as the transistor and CS/A poles roll off this small gain to 0dB.

Figure 19 shows the UC1834 used to implement a negative output supply. A Darlington pass element provides adequate gain for operation at output current levels up to 10A.

CONCLUSION

Ever-increasing requirements for improved power supply economy and efficiency have produced a need for a versatile control IC capable of minimizing power losses in linear regulators. The UC1834 meets this need while also supporting all the auxilliary functions required of such supplies. This control circuit provides for optimized performance in a broad range of linear regulators, and in fact extends the range of applications for which such regulators are appropriate.

9

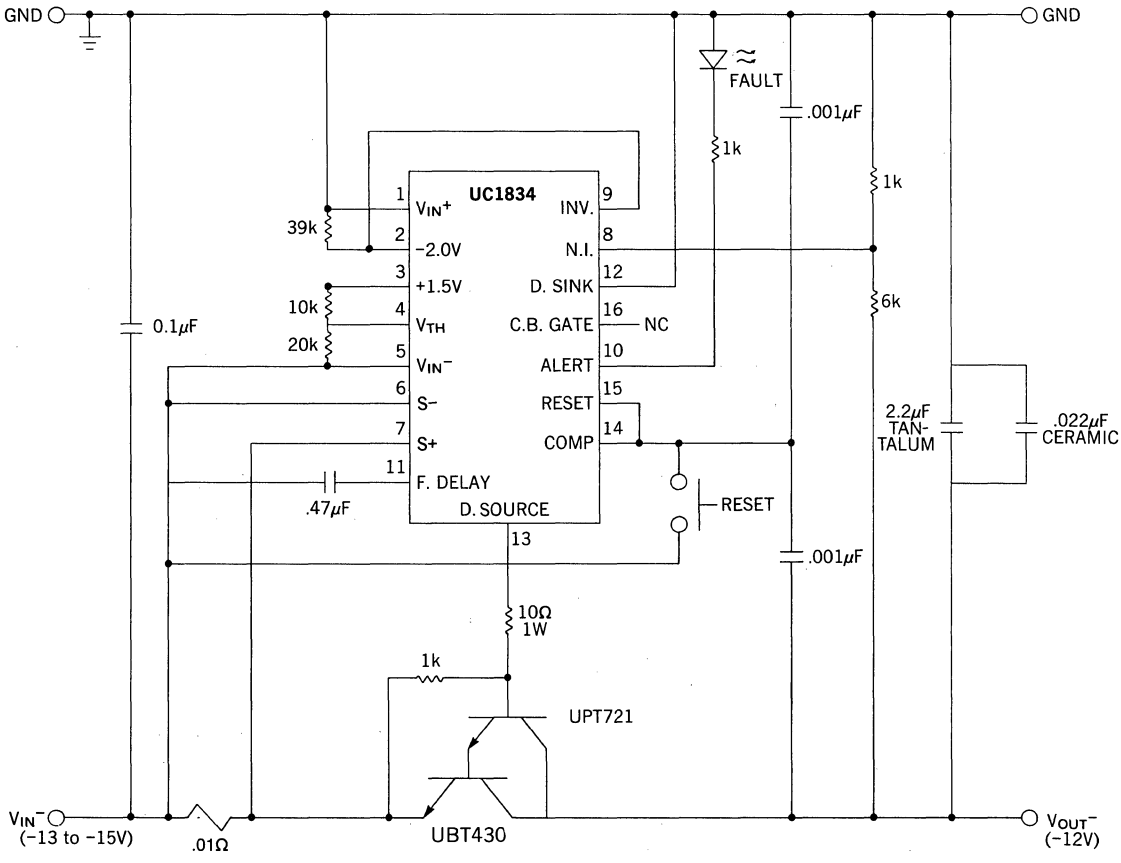

Figure 19. −12V, −10A Negative Regulator

APPENDIX I - FREQUENCY RESPONSE OF VOLTAGE LOOP ELEMENTS

A. The configuration of Figure 16a has, in addition to the compensated E/A, the following loop elements:

- **Drive Transistor** - R_E allows operation of the driver as an emitter follower. Together these elements have an effective small signal AC conductance of $1/R_E$.

- **Pass Transistor** - Low frequency gain (β) and unity-gain frequency (f_T) are usually specified. The pass transistor adds a pole to the loop transfer function at $f_p = f_T/\beta$. Therefore, in order to maintain phase margin at low frequencies, the best choice for a pass device is often a high frequency, low gain switching transistor. Further improvement can be obtained by adding a base-emitter resistor (R_{BE} in Figure 16a) which increases the pole frequency to:

$$f_p = \frac{f_T}{\beta}\left(1 + \frac{\beta \cdot r_e}{R_{BE}}\right)$$

where: $r_e = \frac{kT}{qI_C} = \frac{0.026mV}{I_C}$ (at T = 300K).

- **Load Impedance** - Load characteristics vary greatly with application and operating conditions. The most commonly used models and their respective (s domain) transfer functions are given in Table 1. Note that there are no poles in the transfer functions of those loads which lack shunt capacitance. This can result in a loop transfer function which cannot be rolled off to 0dB at a suitably low frequency using simple E/A compensation networks. For this reason a shunt output capacitor is often added to supplies which must drive loads having low or indeterminant capacitance.

- **Voltage Divider** - The output sensing network introduces a gain of $R_2/(R_1 + R_2)$.

- **Total Loop Gain,** excluding the E/A, is therefore given by:

$$A_V = \frac{v_c}{v_f} = \frac{1}{R_E} \cdot \beta_{PASS} \cdot Z_L \cdot \frac{R_2}{R_1 + R_2} \qquad \text{for } f < \frac{f_T}{\beta}\left(1 + \frac{\beta\, r_e}{R_{BE}}\right)$$

B. The circuit of Figure 16b has a more straightforward response, since the only element (other than the E/A) which introduces any gain is the voltage divider:

$$A_V = \frac{R_2}{R_1 + R_2}$$

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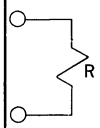
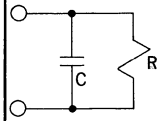
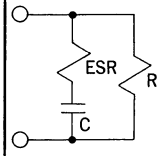
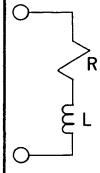
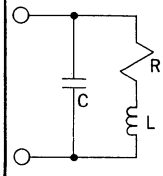
Load Model	Transfer Function	Poles @ f =	Zeros @ f =
	$Z_L(s) = R$	———	———
	$Z_L(s) = \frac{R}{1 + sRC}$	$\frac{1}{2\pi RC}$	———
	$Z_L(s) = \frac{R(1 + s(ESR)C)}{1 + s(R + ESR)C}$	$\frac{1}{2\pi(R + ESR)C}$	$\frac{1}{2\pi(ESR)C}$
	$Z_L(s) = R + sL$	———	$\frac{R}{2\pi L}$
	$Z_L(s) = \frac{s\left(s + \frac{R}{L}\right)}{s^2 + \frac{R}{L}s + \frac{1}{LC}}$	$\frac{-R/L \pm \sqrt{R^2/L^2 - 4/LC}}{4\pi}$	$0, \frac{R}{2\pi L}$

Table 1. Load Models and their Transfer Functions

APPENDIX II - ERROR AMPLIFIER RESPONSE

Figure 20 shows the open-loop gain and phase response of the UC1834 E/A when lightly loaded. The gain curve represents an upper limit on the gain available from the compensated amplifier. Note that a second-order pole occurs near 800kHz. Stable circuits will require a 0dB crossover well below this frequency ($f_c \lesssim 500kHz$).

The E/A can be compensated with or without the use of local feedback. When operated without such feedback (Figure 21a) the transconductance properties of the E/A become evident; i.e. the voltage gain in given by:

$$A_{V(E/A)} = g_M Z_C \qquad (f \lesssim 500kHz)$$

where: $g_M \approx \frac{1}{700\Omega} = 1.4mS$

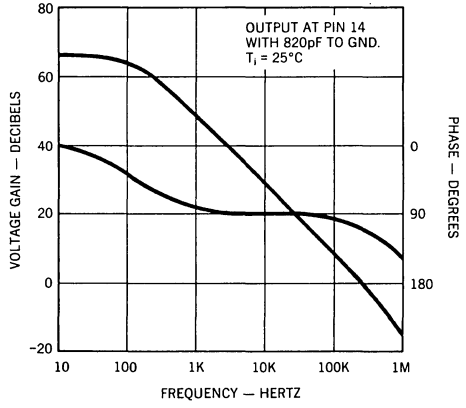


Figure 20. Error Amplifier Gain and Phase Frequency Response

When the E/A has local feedback (Figure 21b), its gain is, to a first approximation, independent of transconductance:

$$A_{V(E/A)} = \frac{Z_F}{Z_{IN}} \qquad (f \lesssim 500kHz)$$

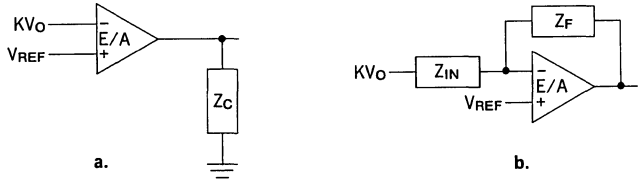


Figure 21. E/A Compensation (a.) Without and (b.) With Local Feedback

However, the use of local feedback creates an additional loop which must be independently stable. The UC1834 has no internal compensation to ensure this stability, so additional external compensation is usually required. An 820pF capacitor from the E/A output to ground will stabilize this inner voltage loop while also enhancing current loop stability.

An additional drawback to the use of local feedback is that Z_F places a DC load on the E/A output. With a transconductance amplifier this results in additional input offset voltage:

$$\Delta V_{IO} = \frac{I_{E/A\,OUT}}{g_M}$$

This offset results in degradation of DC regulation. The problem can be averted by taking local feedback from the emitter of the drive transistor if the driver is configured as an emitter-follower.

Whatever the compensation scheme, the UC1834 E/A output can sink or source a maximum of 100μA.

Table 2 shows two typical compensation schemes and the resulting E/A transfer functions. The first of these circuits is most widely used.

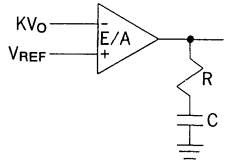
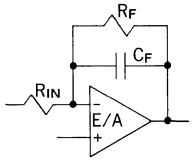
Compensation Circuit	E/A Gain ($A_{V(E/A)}(s)$)	Poles @ f =	Zeros @ f =
	$A_V = \frac{g_M(1 + sRC)}{sC}$	0	$\frac{1}{2\pi RC}$
	$A_V = \frac{R_F}{R_{IN}(1 + s\,R_F C_F)}$	$\frac{1}{2\pi\,R_F C_F}$	———

Table 2. E/A Compensation Circuits and Gain Response

APPENDIX III - FREQUENCY RESPONSE OF THE CURRENT LOOP

- **CS/A** - Figure 22 shows the open-loop gain and phase response of the UC1834 CS/A. This is also a transconductance amplifier, having $g_M \approx 1/70\Omega = 14mS$. The voltage gain is analogous to that of the E/A. The E/A compensation impedance (Z_C or $Z_{F(E/A)}$) is also seen by the CS/A output. For purposes of small signal AC analysis, the CS/A will always see this impedance as being returned to $V_{\overline{IN}}$ (as shown in Figures 16c, d) when the E/A is compensated by either of the methods shown in Table 2.

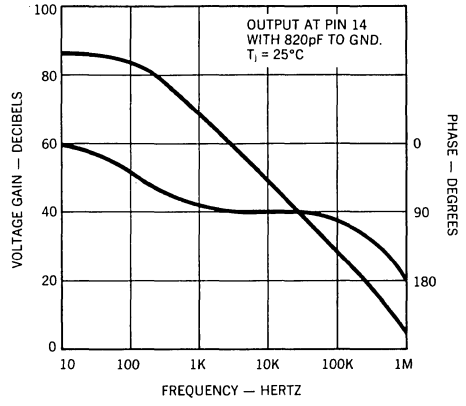


Figure 22. Current Sense Amplifier Gain and Phase Frequency Response

- **Pass Transistor** - Introduces current gain β to the loop transfer of both basic configurations (Figures 16c, d). Considerations outlined in Appendix I also apply here.

- **Sense Resistor** - Resistance value R_{SENSE} appears in transfer function for both configurations.

- **Drive Transistor** - In the circuit of Figure 16c, R_E allows operation of the driver as an emitter-follower. Effective conductance is $1/R_E$.

9

Closed-loop responses are given by the following:

for circuit of Figure 16c:

$$A_I = g_M \cdot Z_C \cdot \frac{1}{R_E} \cdot \beta \cdot R_{SENSE} \qquad \left(f < 500kHz, f < \frac{f_T}{\beta}\left(1 + \frac{\beta r_e}{R_{BE}}\right)\right)$$

for circuit of Figure 16d:

$$A_I = g_M \cdot \frac{Z_C}{Z_C + \beta Z_L} \cdot \beta \cdot R_{SENSE} \qquad \left(f < 500kHz, f < \frac{f_T}{\beta}\left(1 + \frac{\beta r_e}{R_{BE}}\right)\right)$$

A 25 WATT OFF-LINE FLYBACK SWITCHING REGULATOR

Introduction

This Application Note describes a low cost (less than $10.00) switching power supply for applications requiring multiple output voltages, e.g. personal computers, instruments, etc...The discontinuous mode flyback regulator used in this application provides good voltage tracking between outputs, which allows the use of primary side voltage sensing. This sensing technique reduces costs by eliminating the need for an isolated secondary feedback loop.

The low cost, (8 pin) UC3844 current mode control chip employed in this power supply provides performance advantages such as:

1) Fast transient response
2) Pulse by pulse current limiting
3) Stable operation

To simplify drive circuit requirements, a TO-220 power MOSFET (UFN833) is utilized for the power switch. This switch is driven directly from the output of the control chip.

Power Supply Specifications

1. Input voltage: 95VAC to 130VAC (50Hz/60Hz)
2. Output voltage:
   A. +5V, ±5%: 1A to 4A load
      Ripple voltage: 50mV P-P Max.
   B. +12V, ±3%: 0.1A to 0.3A load
      Ripple voltage: 100mV P-P Max.
   C. −12V, ±3%: 0.1A to 0.3A load
      Ripple voltage: 100mV P-P Max.
3. Line Isolation: 3750 Volts
4. Switching Frequency: 40KHz
5. Efficiency @ Full Load: 70%

Basic Circuit Operation

The 117VAC input line voltage is rectified and smoothed to provide DC operating voltage for the circuit. When power is initially applied to the circuit, capacitor C2 charges through R2. When the voltage across C2 reaches a level of 16V the output of IC1 is enabled, turning on power MOSFET Q1. During the on time of Q1, energy is stored in the air gap of transformer (inductor) T1. At this time the polarity of the output windings is such that all output rectifiers are reverse biased and no energy is transferred. Primary current is sensed by a resistor, R10, and compared to a fixed 1 volt reference inside IC1. When this level is reached, Q1 is turned off and the polarity of all transformer windings reverses, forward biasing the output rectifiers. All the energy stored is now transferred to the output capacitors. Many cycles of this store/release action are needed to charge the outputs to their respective voltages. Note that C2 must have enough energy stored initially to keep the control circuitry operating until C4 is charged to a level of approximately 13V. The voltage across C4 is fed through a voltage divider to the error amplifier (pin 2) and compared to an internal 2.5V reference.

Energy stored in the leakage inductance of T1 causes a voltage spike which will be added to the normal reset voltage across T1 when Q1 turns off. The clamp consisting of D4, C9 and R12 limits this voltage excursion from exceeding the BVDSS rating of Q1. In addition, a turn-off snubber made up of D5, C8 and R11 keeps power dissipation in Q1 low by delaying the voltage rise until drain current has decreased from its peak value. This snubber also damps out any ringing which may occur due to parasitics.

Less than 3.5% line and load regulation is achieved by loading the output of the control winding, Nc, with R9. This resistor dissipates the leakage energy associated with this winding. Note that R9 must be isolated from R2 with diode D2, otherwise C2 could not charge to the 16V necessary for initial start-up.

A small filter inductor in the 5V secondary is added to reduce output ripple voltage to less than 50mV. This inductor also attenuates any high frequency noise.

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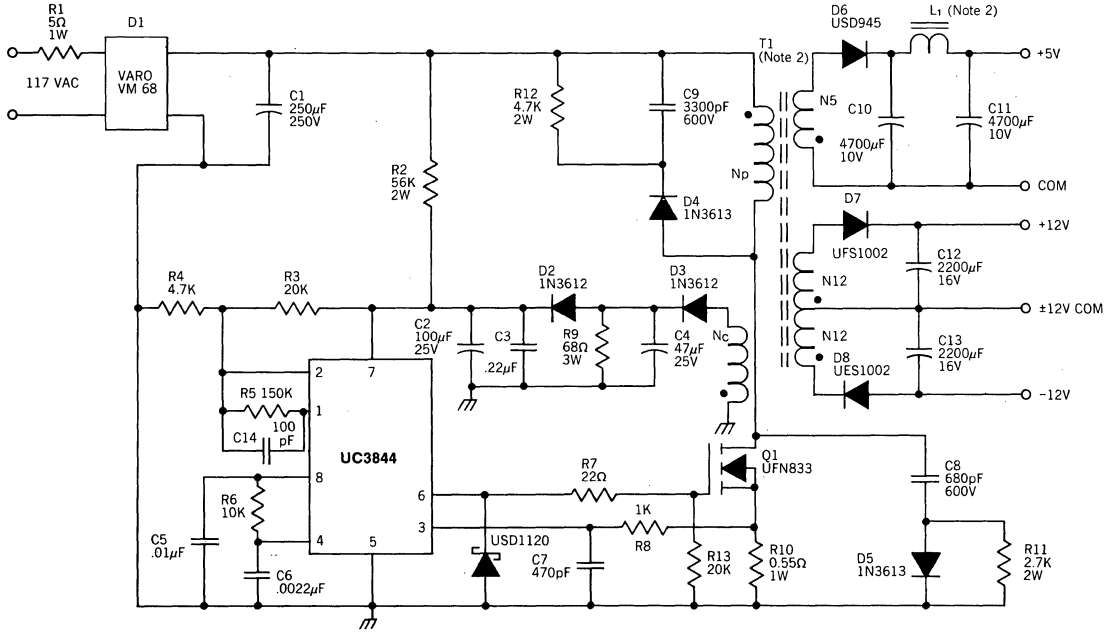
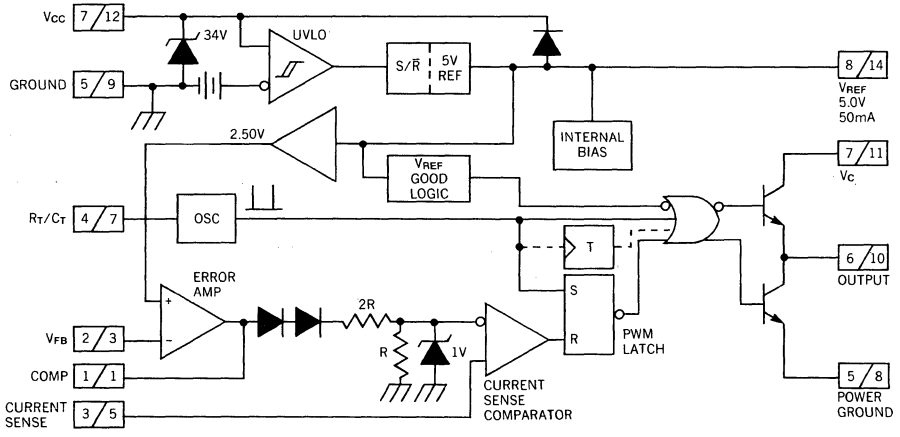
25W OFF-LINE FLYBACK REGULATOR



Notes: 1. All resistors are ¼ watt unless noted
2. See Appendix for construction details

BLOCK DIAGRAM

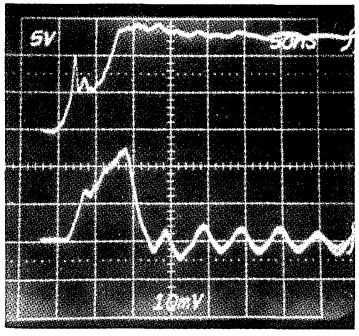


Note: 1. A/B A = DIL-8 Pin Number. B = SO-14 Pin Number.
2. Toggle flip flop used only in 1844 and 1845.

UC3842/3/4/5 CURRENT MODE PWM CONTROLLER

TYPICAL SWITCHING WAVEFORMS

T_{on} — Drive waveforms

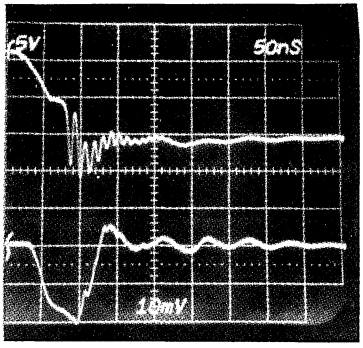


5V/DIV

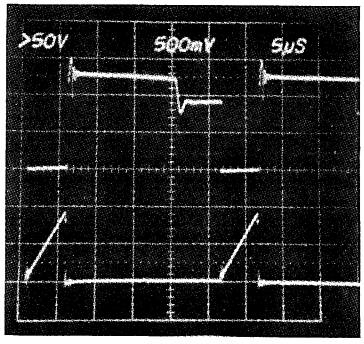
200mA/DIV

Upper trace: Q_1 — Gate to source voltage
Lower trace: Q_1 — Gate current

T_{off} — Drive waveforms



Upper trace: Q_1 — Gate to source voltage
Lower trace: Q_1 — Gate current



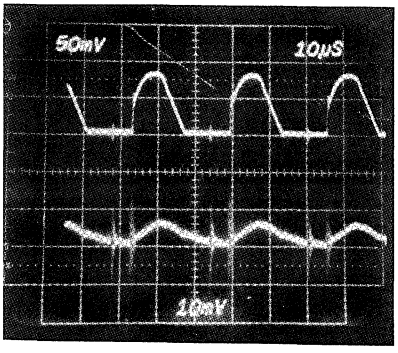
100V/DIV

0.5A/DIV

Upper trace: Q_1 — Drain to source voltage
Lower trace: Primary current — I_D

5A/DIV

50mV/DIV



Upper trace: +5V charging current
Lower trace: +5V output ripple voltage

9

PERFORMANCE DATA

CONDITIONS		5V out	12V out	−12V out
Low Line (95VAC)				
± 12 @ 100mA	+5V @ 1.0A	5.211	12.05	−12.01
	4.0A	4.854	12.19	−12.14
± 12 @ 300mA	+5V @ 1.0A	5.199	11.73	−11.69
	4.0A	4.950	11.68	−11.63
Nominal Line (120VAC)				
± 12 @ 100mA	+5V @ 1.0A	5.220	12.07	−12.03
	4.0A	4.875	12.23	−12.18
± 12 @ 300mA	+5V @ 1.0A	5.208	11.73	−11.68
	4.0A	4.906	11.67	−11.62
High Line (130VAC)				
± 12 @ 100mA	+5V @ 1.0A	5.207	12.06	−12.02
	4.0A	4.855	12.21	−12.15
± 12V @ 300mA	+5V @ 1.0A	5.200	11.71	−11.67
	4.0A	4.902	11.66	11.61
Overall Line and Load Regulation		±3.5%	±2.3%	±2.4%

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PARTS LIST

IC's	
IC1	UC3844
POWER MOSFET	
Q1	UFN833
RECTIFIERS	
D1	VM68 varo
D2, D3	1N3612
D4, D5	1N3613
D6	USD945
D7, D8	UES1002
CAPACITORS	
C1	250μF, 250V
C2	100μF, 25V
C3	0.22μF, 25V
C4	47μF, 25V
C5	.01μF, 25V
C6	.0047μF, 25V
C7	470pF, 25V
C8	680pF, 600V
C9	3300pF, 600V
C10, C11	4700μF, 10V
C12, C13	2200μF, 16V
C14	100pF, 25V
RESISTORS	
R1	5Ω, 1W
R2	56K, 2W
R3	20K
R4	4.7K
R5	150K
R6	10K
R7	22Ω
R8	1K
R9	68Ω, 3W
R10	0.55Ω, 1W
R11	2.7K, 2W
R12	4.7K, 2W
R13	20K
MAGNETICS	
T_1	see appendix
L_1	see appendix

9

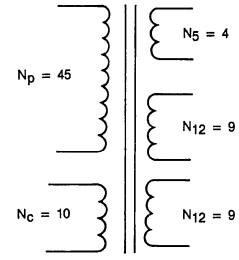
APPENDIX

POWER TRANSFORMER—T1

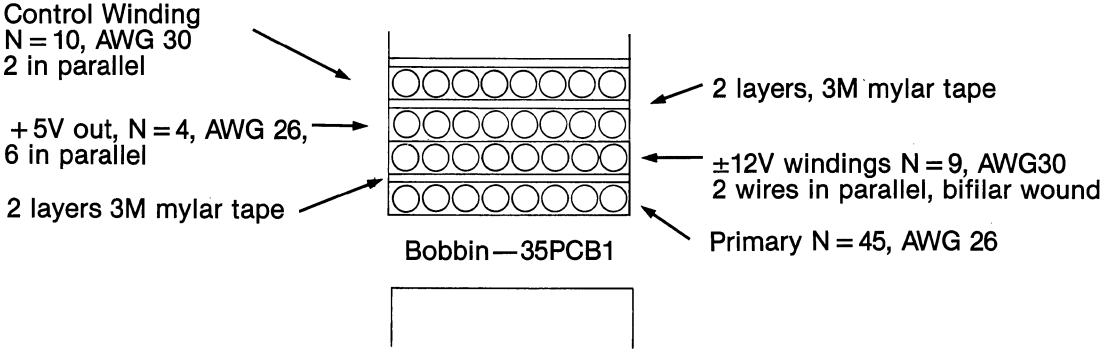
Core: Ferroxcube EC-35/3C8
Gap: 10 mil in each outer leg

NOTE: For reduced EMI put gap in center leg only. Use 20 mil.

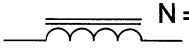
Ferroxcube
EC-35/3C8



TRANSFORMER CONSTRUCTION



5V OUTPUT INDUCTOR



Ferroxcube
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MODELLING, ANALYSIS AND COMPENSATION OF THE CURRENT-MODE CONVERTER

Abstract

As current-mode conversion increases in popularity, several peculiarities associated with fixed-frequency, peak-current detecting schemes have surfaced. These include instability above 50% duty cycle, a tendency towards subharmonic oscillation, non-ideal loop response, and an increased sensitivity to noise. This paper will attempt to show that the performance of any current-mode converter can be improved and at the same time all of the above problems reduced or eliminated by adding a fixed amount of "slope compensation" to the sensed current waveform.

1.0 INTRODUCTION

The recent introduction of integrated control circuits designed specifically for current mode control has led to a dramatic upswing in the application of this technique to new designs. Although the advantages of current-mode control over conventional voltage-mode control has been amply demonstrated [1-5], there still exist several drawbacks to a fixed frequency peak-sensing current mode converter. They are (1) open loop instability above 50% duty cycle, (2) less than ideal loop response caused by peak instead of average inductor current sensing, (3) tendency towards subharmonic oscillation, and (4) noise sensitivity, particularly when inductor ripple current is small. Although the benefits of current mode control will, in most cases, far out-weight these drawbacks, a simple solution does appear to be available. It has been shown by a number of authors that adding slope compensation to the current waveform (Figure 1) will stabilize a system above 50% duty cycle. If one is to look further, it becomes apparent that this same compensation technique can be used to minimize many of the drawbacks stated above. In fact, it will be shown that any practical converter will nearly always perform better with some slope compensation added to the current waveform.

The simplicity of adding slope compensation – usually a single resistor – adds to its attractiveness. However, this introduces a new problem – that of analyzing and predicting converter performance. Small signal AC models for both current and voltage-mode PWM's have been extensively developed in the literature. However, the slope compensated or "dual control" converter possesses properties of both with an equivalent circuit different from, yet containing elements of each. Although this has been addressed in part by several authors [1, 2], there still exists a need for a simple circuit model that can provide both qualitative and quantitative results for the power supply designer.

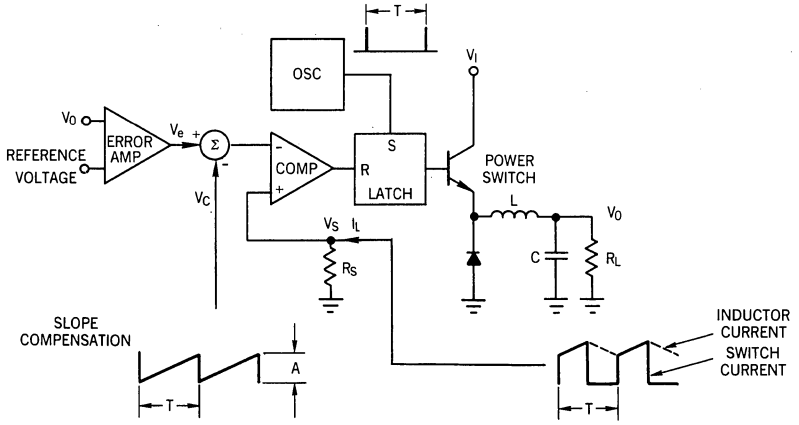

FIGURE 1 – A CURRENT-MODE CONTROLLED BUCK REGULATOR WITH SLOPE COMPENSATION.

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The first objective of this paper is to familiarize the reader with the peculiarities of a peak-current control converter and at the same time demonstrate the ability of slope compensation to reduce or eliminate many problem areas. This is done in section 2. Second, in section 3, a circuit model for a slope compensated buck converter in continuous conduction will be developed using the state-space averaging technique outlined in(1). This will provide the analytical basis for section 4 where the practical implementation of slope compensation is discussed.

2.1 OPEN LOOP INSTABILITY

An unconditional instability of the inner current loop exists for any fixed frequency current-mode converter operating above 50% duty cycle – regardless of the state of the voltage feedback loop. While some topologies (most notably two transistor forward converters) cannot operate above 50% duty cycle, many others would suffer serious input limitations if greater duty cycle could not be achieved. By injecting a small amount of slope compensation into the inner loop, stability will result for all values of duty cycle. Following is a brief review of this technique.

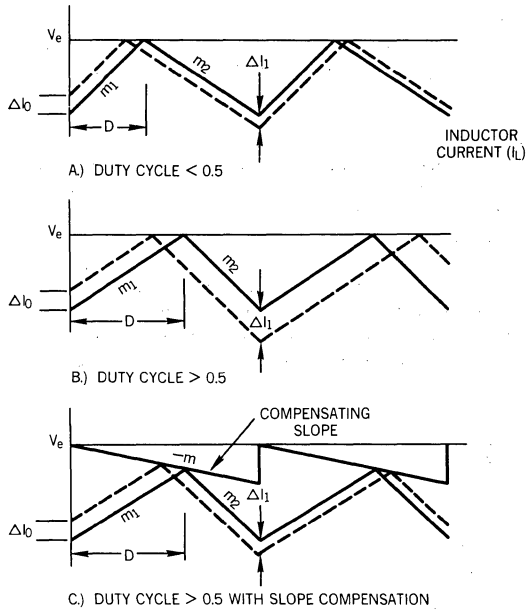

FIGURE 2 – DEMONSTRATION OF OPEN LOOP INSTABILITY IN A CURRENT-MODE CONVERTER.

Figure 2 depicts the inductor current waveform, I_L, of a current-mode converter being controlled by an error voltage V_e. By perturbing the current I_L by an amount ΔI, it may be seen graphically that ΔI will decrease with time for $D < 0.5$ (Figure 2A), and increase with time for $D > 0.5$ (Figure 2B). Mathematically this can be stated as

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2}{m_1}\right) \qquad (1)$$

Carrying this a step further, we can introduce a linear ramp of slope $-m$ as shown in Figure 2C. Note that this slope may either be added to the current waveform, or subtracted from the error voltage. This then gives

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2 + m}{m_1 + m}\right) \qquad (2)$$

Solving for m at 100% duty cycle gives

$$m > -\tfrac{1}{2} m_2 \qquad (3)$$

Therefore, to guarantee current loop stability, the slope of the compensation ramp must be greater than one-half of the down slope of the current waveform. For the buck regulator of Figure 1, m_2 is a constant equal to $\frac{V_0}{L} R_S$, therefore, the amplitude A of the compensating waveform should be chosen such that

$$A > T R_S \frac{V_0}{L} \qquad (4)$$

to guarantee stability above 50% duty cycle.

2.2 RINGING INDUCTOR CURRENT

Looking closer at the inductor current waveform reveals two additional phenomenon related to the previous instability: If we generalize equation 2 and plot I_n vs nT for all n as in Figure 3, we observe a damped sinusoidal response at one-half the switching frequency, similar to that of an RLC circuit. This ring-out is undesirable in that it (a) produces a ringing response of the inductor current to line and load transients, and (b) peaks the control loop gain at ½ the switching frequency, producing a marked tendency towards instability.

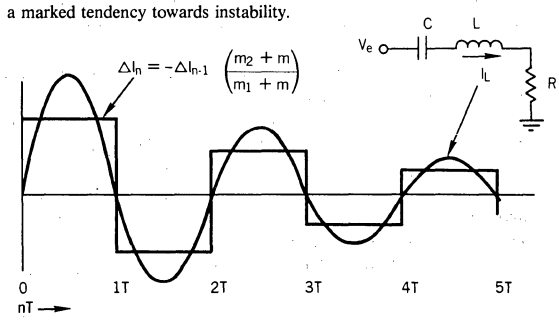

FIGURE 3 – ANALOGY OF THE INDUCTOR CURRENT RESPONSE TO THAT OF AN RLC CIRCUIT.

It has been shown in (1), and is easily verified from equation 2, that by choosing the slope compensation m to be equal to $-m_2$ (the down slope of the inductor current), the best possible transient response is obtained. This is analogous to critically damping the RLC circuit, allowing the current to correct itself in exactly one cycle. Figure 4 graphically demonstrates this point. Note that while this may optimize inductor current ringing, it has little bearing on the transient response of the voltage control loop itself.

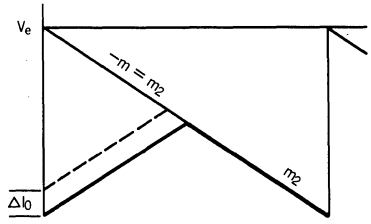

FIGURE 4 – FOR THE CASE OF $m = -m_2$, A CURRENT PERTURBATION WILL DAMP OUT IN EXACTLY ONE CYCLE.

2.3 SUBHARMONIC OSCILLATION

Gain peaking by the inner current loop can be one of the most significant problems associated with current-mode controllers. This peaking occurs at one-half the switching frequency, and – because of excess phase shift in the modulator – can cause the voltage feedback loop to break into oscillation at one-half the switching frequency. This instability, sometimes called subharmonic oscillation, is easily detected as duty cycle asymmetry between consecutive drive pulses in the power stage. Figure 5 shows the inductor current of a current-mode controller in subharmonic oscillation (dotted waveforms with period 2T).

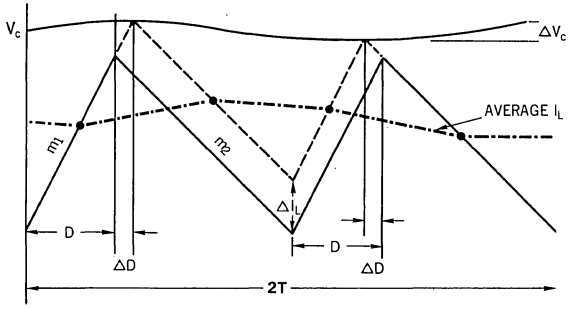

FIGURE 5 – CURRENT WAVE FORM (DOTTED) OF A CURRENT-MODE CONVERTER IN SUBHARMONIC OSCILLATION.

To determine the bounds of stability, it is first necessary to develop an expression for the gain of the inner loop at one-half the switching frequency. The technique used in (2) will be paralleled for a buck converter with the addition of terms to include slope compensation.

2.3.1 LOOP GAIN CALCULATION AT ½f_s

Referring to figures 5 and 6, we want to relate the input stimulus, ΔV_e, to an output current, ΔI_L. From figure 5, two equations may be written

$$\Delta I_L = \Delta D\, m_1\, T - \Delta D\, m_2\, T \qquad (4)$$

$$\Delta V_C = \Delta D\, m_1\, T + \Delta D\, m_2\, T \qquad (5)$$

Adding slope compensation as in figure 6 gives another equation

$$\Delta V_e = \Delta V_C + 2\Delta D\, m\, T \qquad (6)$$

Using (5) to eliminate ΔV_C from (6) and solving for $\Delta I_L/\Delta V_e$ yields

$$\frac{\Delta I_L}{\Delta V_e} = \frac{m_1 - m_2}{m_1 + m_2 + m} \qquad (7)$$

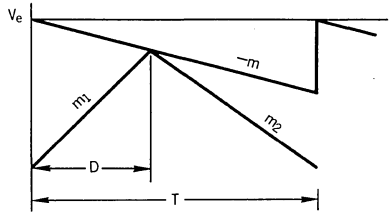

FIGURE 6 – ADDITION OF SLOPE COMPENSATION TO THE CONTROL SIGNAL

For steady state condition we can write

$$D\, m_1\, T = (1 - D)\, m_2\, T \qquad (8)$$

or

$$D = \frac{-m_2}{m_1 - m_2} \qquad (9)$$

By using (9) to reduce (7), we obtain

$$\frac{\Delta I_L}{\Delta V_e} = \frac{1}{1 - 2D\,(1 + m/m_2)} \qquad (10)$$

Now by recognizing that ΔI_L is simply a square wave of period 2T, we can relate the first harmonic amplitude to ΔI_L by the factor $4/\pi$ and write the small signal gain at $f = \frac{1}{2}f_S$ as

$$\frac{i_L}{v_e} = \frac{4\pi}{1 - 2D\,(1 + m/m_2)} \qquad (11)$$

If we assume a capacitive load of C at the output and an error amplifier gain of A, then finally, the expression for loop gain at $f = \frac{1}{2} f_S$ is

$$\text{Loop gain} = \frac{\frac{4TA}{\pi^2 C}}{1 - 2D\,(1 + m/m_2)} \qquad (12)$$

2.3.2 USING SLOPE COMPENSATION TO ELIMINATE SUBHARMONIC OSCILLATION

From equation 12, we can write an expression for maximum error amplifier gain at $f = \frac{1}{2}f_S$ to guarantee stability as

$$A_{max} = \frac{1 - 2D\,(1 + m/m_2)}{\frac{4T}{\pi^2 C}} \qquad (13)$$

This equation clearly shows that the maximum allowable error amplifier gain, A_{max}, is a function of both duty cycle and slope compensation. A normalized plot of A_{max} versus duty cycle for several values of slope compensation is shown in figure 7. Assuming the amplifier gain cannot be reduced to zero at $f = \frac{1}{2}f_S$, then for the case of m = 0 (no compensation) we see the same instability previously discussed at 50% duty cycle. As the compensation is increased to $m = -\frac{1}{2}m_2$, the point of instability moves out to a duty cycle of 1.0, however in any practical

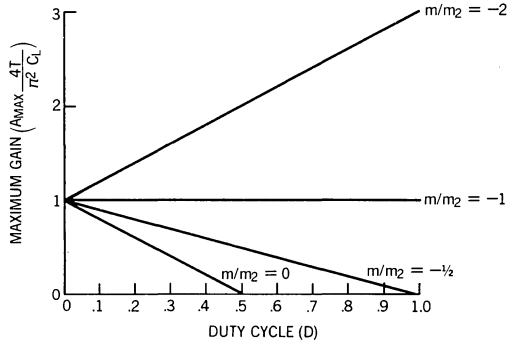

FIGURE 7 – MAXIMUM ERROR AMPLIFIER GAIN AT ½ f_s (NORMALIZED) V.S. DUTY CYCLE FOR VARYING AMOUNTS OF SLOPE COMPENSATION. REFER TO EQUATION 13.

9

system, the finite value of A_{max} will drive the feedback loop into subharmonic oscillation well before full duty cycle is reached. If we continue to increase m, we reach a point, $m = -m_2$, where the maximum gain becomes independent of duty cycle. This is the point of critical damping as discussed earlier, and increasing m above this value will do little to improve stability for a regulator operating over the full duty cycle range.

2.4 PEAK CURRENT SENSING VERSUS AVERAGE CURRENT SENSING

True current-mode conversion, by definition, should force the average inductor current to follow an error voltage – in effect replacing the inductor with a current source and reducing the order of the system by one. As shown in Figure 8, however, peak current detecting schemes are generally used which allow the average inductor current to vary with duty cycle while producing less than perfect input to output – or feedforward characteristics. If we choose to add slope compensation equal to $m = -\frac{1}{2} m_2$ as shown in Figure 9, we can convert a peak current detecting scheme into an average current detector, again allowing for perfect current mode control. As mentioned in the last section, however, one must be careful of subharmonic oscillations as a duty cycle of 1 is approached when using $m = -\frac{1}{2} m_2$.

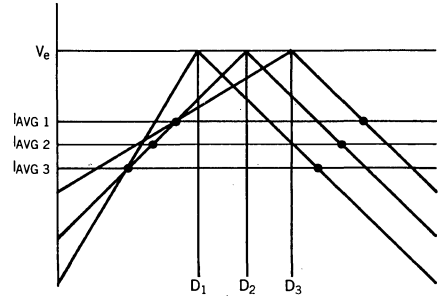

FIGURE 8 – PEAK CURRENT SENSING WITHOUT SLOPE COMPENSATION ALLOWS AVERAGE INDUCTOR CURRENT TO VARY WITH DUTY CYCLE

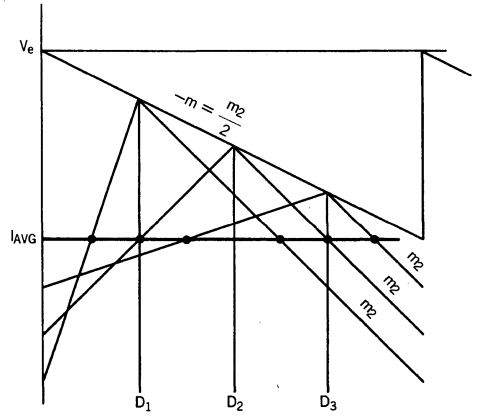

FIGURE 9 – AVERAGE INDUCTOR CURRENT IS INDEPENDENT OF DUTY CYCLE AND INPUT VOLTAGE VARIATION FOR A SLOPE COMPENSATION OF $m = -\frac{1}{2} m_2$.

2.5 SMALL RIPPLE CURRENT

From a systems standpoint, small inductor ripple currents are desirable for a number of reasons – reduced output capacitor requirements, continuous current operation with light loads, less output ripple, etc. However, because of the shallow slope presented to the current sense circuit, a small ripple current can, in many cases, lead to pulse width jitter caused by both random and synchronous noise (Figure 10). Again, if we add slope compensation to the current waveform, a more stable switchpoint will be generated. To be of benefit, the amount of slope added needs to be significant compared to the total inductor current – not just the ripple current. This usually dictates that the slope m be considerably greater than m_2 and while this is desirable for subharmonic stability, any slope greater than $m = -\frac{1}{2} m_2$ will cause the converter to behave less like an ideal current mode converter and more like a voltage mode converter. A proper trade-off between inductor ripple current and slope compensation can only be made based on the equivalent circuit model derived in the next section.

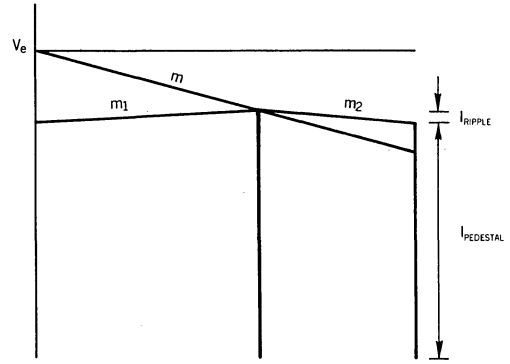

FIGURE 10 – A LARGE PEDESTAL TO RIPPLE CURRENT RATIO.

3.0 SMALL SIGNAL A.C. MODEL

As we have seen, many drawbacks associated with current-mode control can be reduced or eliminated by adding slope compensation in varying degrees to the current waveform. In an attempt to determine the full effects of this same compensation on the closed loop response, a small signal equivalent circuit model for a buck regulator will now be developed using the state-space averaging technique developed in (1).

3.1 A.C. MODEL DERIVATION

Figure 11a shows an equivalent circuit for a buck regulator power stage. From this we can write two state-space averaged differential equations corresponding to the inductor current and capacitor voltage as functions of duty cycle D

$$\dot{I}_L = \frac{(V_I - V_0)}{L} D - \frac{V_0 (1 - D)}{L} \qquad (14)$$

$$\dot{V}_0 = \frac{I_L}{C} - \frac{V_0}{R} \qquad (15)$$

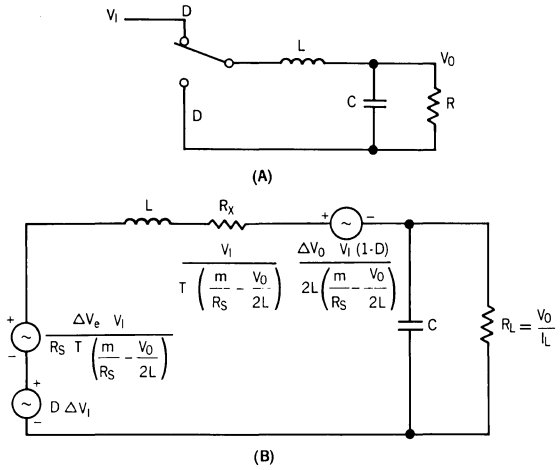

FIGURE 11 – BASIC BUCK CONVERTER (A) AND ITS SMALL SIGNAL EQUIVALENT CIRCUIT MODEL (B).

If we now perturb these equations – that in substitute $V_I + \Delta V_I$, $V_0 + \Delta V_0$, $D + \Delta D$ and $I_L + \Delta I_L$ for their respective variables – and ignore second order terms, we obtain the small signal averaged equations

$$\Delta \dot{I}_L = \frac{D\Delta I_L}{L} - \frac{\Delta V_0}{L} + \frac{V_I \Delta D}{L} \qquad (16)$$

$$\Delta \dot{V}_0 = \frac{\Delta I_L}{C} - \frac{\Delta V_0}{CR} \qquad (17)$$

A third equation – the control equation – relating error voltage, V_e, to duty cycle may be written from Figure 6 as

$$I_L R_S = V_e - mDT - \frac{(1 - D)\, V_0\, T\, R_S}{2L} \qquad (18)$$

Perturbing this equation as before gives

$$\Delta I_L = \frac{\Delta V_e}{R_S} - \Delta DT\left(\frac{m}{R_S} - \frac{V_0}{2L}\right) - \frac{T}{2L}(1 - D)\,\Delta V_0 \qquad (19)$$

By using 19 to eliminate ΔD from 16 and 17 we arrive at the state-space equations

$$\Delta \dot{I}_L = \frac{D}{L}\Delta V_I + \frac{\Delta V_e\, V_I}{R_S\, LT\left(\frac{m}{R_S} - \frac{V_0}{2L}\right)} - \frac{\Delta V_0\, V_I\,(1 - D)}{2L^2\left(\frac{m}{R_S} - \frac{V_0}{2L}\right)} - \frac{\Delta I_L V_I}{LT\left(\frac{m}{R_S} - \frac{V_0}{2L}\right)} \qquad (20)$$

$$\Delta \dot{V}_0 = \frac{\Delta I_L}{C} - \frac{\Delta V_0}{CR} \qquad (21)$$

An equivalent circuit model for these equations is shown in Figure 11B and discussed in the next section.

3.2 A.C. MODEL DISCUSSION

The model of Figure 11B can be used to verify and expand upon our previous observations. Key to understanding this model is the interaction between R_X and L as the slope compensation, m is changed. In most cases, the dependent source between R_X and C can be ignored.

If R_X is much greater than L, as is the case for little or no compensation ($m = 0$), the converter will have a single pole response and act as a true current mode converter. If R_X is small compared to $L\left(m \gg \frac{R_S V_0}{2L}\right)$, then a double pole response will be formed by the LRC output filter similar to any voltage-mode converter. By appropriately adjusting m, any condition between these two extremes can be generated.

Of particular interest is the case when $m = \frac{R_S V_0}{2L}$. Since the down slope of the inductor current (m_2 from Figure 6) is equal to $\frac{R_S V_0}{L}$, we can write $m = -\frac{1}{2}m_2$. At this point, R_X goes to infinity, resulting in an ideal current mode converter. This is the same point, discussed in section 2.4, where the average inductor current exactly follows the error voltage. Note that although this compensation is ideal for line rejection and loop response, maximum error amp gain limitations as higher duty cycles are approached (section 2.3) may necessitate using more compensation.

Having derived an equivalent circuit model, we may now proceed in its application to more specific design examples. Figure 12 plots open loop ripple rejection ($\Delta V_0/\Delta V_I$) at 120Hz versus slope compensation for a typical 12 volt buck regulator operating under the following conditions:

V_0	=	12V
V_I	=	25V
L	=	200μH
C	=	300μf
T	=	20μS
R_S	=	.5Ω
R_L	=	1Ω, 12Ω

Again, as the slope compensation approaches $-\frac{1}{2}m_2$, the theoretical ripple rejection is seen to become infinite. As larger values of m are introduced, ripple rejection slowly degrades to that of a voltage-mode converter (−6.4dB for this example).

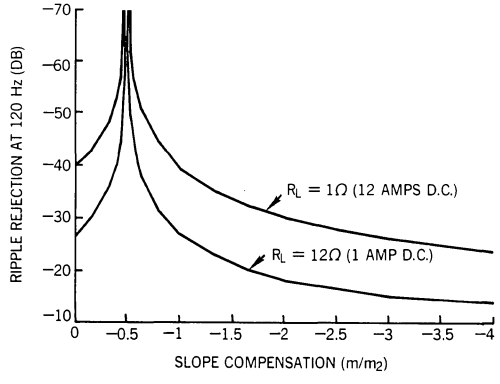

FIGURE 12 – RIPPLE REJECTION AT 120Hz V.S. SLOPE COMPENSATION FOR 1AMP AND 12AMP LOADS.

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If a small ripple to D.C. current ratio is used, as is the case for R_L = 1ohm in the example, proportionally larger values of slope compensation may be injected while still maintaining a high ripple rejection ratio. In other words, to obtain a given ripple rejection ratio, the allowable slope compensation varies proportionally to the average D.C. current, not the ripple current. This is an important concept when attempting to minimize noise jitter on a low ripple converter.

Figure 13 shows the small signal loop response ($\Delta V_0/\Delta V_e$) versus frequency for the same example of Figure 12. The gains have all been normalized to zero dB at low frequency to reflect the actual difference in frequency response as slope compensation m is varied. At m = $-\frac{1}{2}$ m_2, an ideal single-pole roll-off at 6dB/octave is obtained. As higher ratios are used, the response approaches that of a double-pole with a 12dB/octave roll-off and associated 180° phase shift.

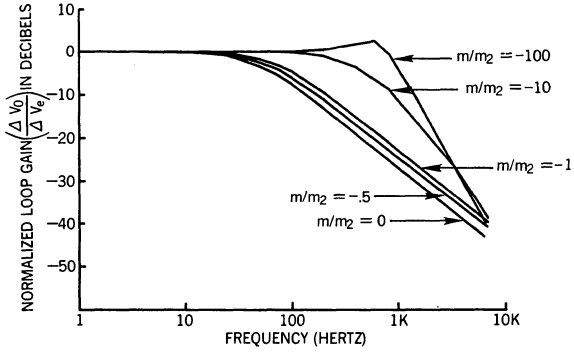
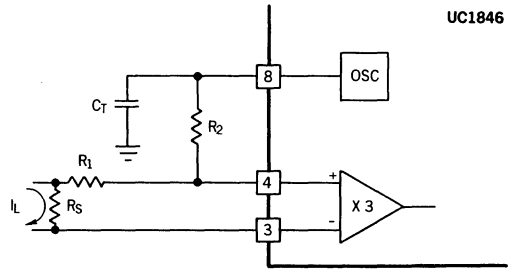
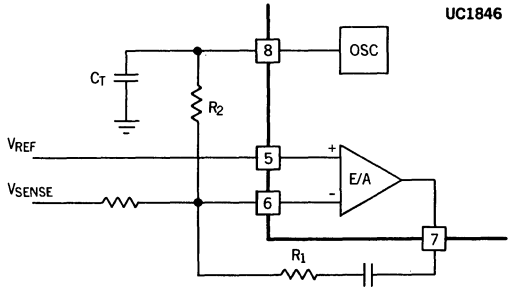


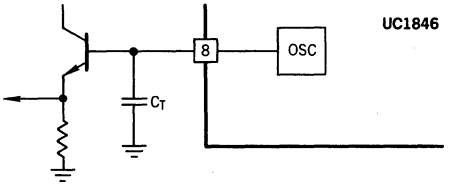
FIGURE 13 – NORMALIZED LOOP GAIN V.S. FREQUENCY FOR VARIOUS SLOPE COMPENSATION RATIO'S.



(a) SUMMING OF SLOPE COMPENSATION DIRECTLY WITH SENSED CURRENT SIGNAL



(b) SUMMING OF SLOPE COMPENSATION WITH ERROR SIGNAL



(c) EMITTER FOLLOWER USED TO LOWER OUTPUT IMPEDANCE OF OSCILLATOR.

FIGURE 14 – ALTERNATIVE METHODS OF IMPLEMENTING SLOPE COMPENSATION WITH THE UC1846 CURRENT-MODE CONTROLLER.

4.0 SLOPE COMPENSATING THE UC1846 CONTROL I.C.

Implementing a practical, cost effective current-mode converter has recently been simplified with the introduction of the UC1846 integrated control chip. This I.C. contains all of the control and support circuitry required for the design of a fixed frequency current-mode converter. Figures 14A and B demonstrate two alternative methods of implementing slope compensation using the UC1846. Direct summing of the compensation and current sense signal at Pin 4 is easily accomplished, however, this introduces an error in the current limit sense circuitry. The alternative method is to introduce the compensation into the negative input terminal of the error amplifier. This will only work if (a) the gain of the error amplifier is fixed and constant at the switching frequency (R_1/R_2 for this case) and (b) both error amplifier and current amplifier gains are taken into consideration when calculating the required slope compensation. In either case, once the value of R_2 has been calculated, the loading effect on C_T can be determined and, if necessary, a buffer stage added as in Figure 14C.

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A NEW IC OPTIMIZES HIGH SPEED POWER MOSFET DRIVE FOR SWITCHING POWER SUPPLIES

Abstract

Although touted as a high-impedance, voltage-controlled device, prospective users soon learn that it takes high drive currents to achieve high-speed switching with Power MOSFETS. This paper describes the construction techniques which lead to the parasitic effects which normally limit FET performance, and discusses several circuit approaches useful to improve switching speed. IC drivers optimized for driving FETS are compared and a new high-speed efficient driver is introduced.

INTRODUCTION

An investigation of Power MOSFET construction techniques will identify several parasitic elements which make the highly-touted "simple gate drive" of MOSFET devices less than obvious. These parasitic elements, primarily capacitive in nature, can require high peak drive currents with fast rise times coupled with care that excessive di/dt does not cause current overshoot or ringing with rectifier recovery current spikes.

This paper develops a switching model for Power MOSFET devices and relates the individual parameters to construction techniques. From this model, ideal drive characteristics are defined and practical IC implementations are discussed. Specific applications to switch-mode power systems involving both direct and transformer coupled drive are described and evaluated.

POWER MOSFET CHARACTERISTICS

The advantages which power MOSFET's have over their bipolar competitors have given them an ever-increasing utilization in power systems and, in the process, opened the way to new performance levels and new topologies.

A major factor in this regard is the potential for extremely fast switching. Not only is there no storage time inherent with MOSFET's, but the switching times can be user controlled to suit the application. This, of course, requires that the designer have an understanding of the switching dynamics inherent in these devices. Even though power MOSFET's are majority carrier devices, the speed at which they can switch is dependent upon many parameters and parasitic effects related to the device's construction.

THE POWER MOSFET MODEL

An understanding of the parasitic elements in a power MOSFET can be gained by comparing the construction details of a MOSFET with its electrical model as shown in Figure 1. This construction diagram is a simplified sketch of a single cell – a high power device such as the UFN 150 would have ≈ 20,000 of these cells all connected in parallel.

In operation, when the gate voltage is below the gate threshold, Vg(th), the drain voltage is supported by the N- drain region and its adjacent implanted P region and there is no conduction.

When the gate voltage rises above Vg(th), however, the P area under the gate inverts to N forming a conductive layer between the N+ source and the N− drain. This allows electrons to migrate from source to drain where the electric field in the drain sweeps them to the drain terminal at the bottom of the structure.

In the equivalent electrical model, the parameters are defined as follows:

1. Lg and Rg represent the inductance and resistance of the wire bonds between the package terminal and the actual gate, plus the resistance of the polysilicon gate runs.

2. C1 represents the capacitance from the gate to both the N+ source and the overlying source interconnecting metal. Its value is fixed by the design of the structure.

3. C2 + C4 represents additional gate-source capacitance into the P region. C2 is the dielectric capacitance and is fixed while C4 is

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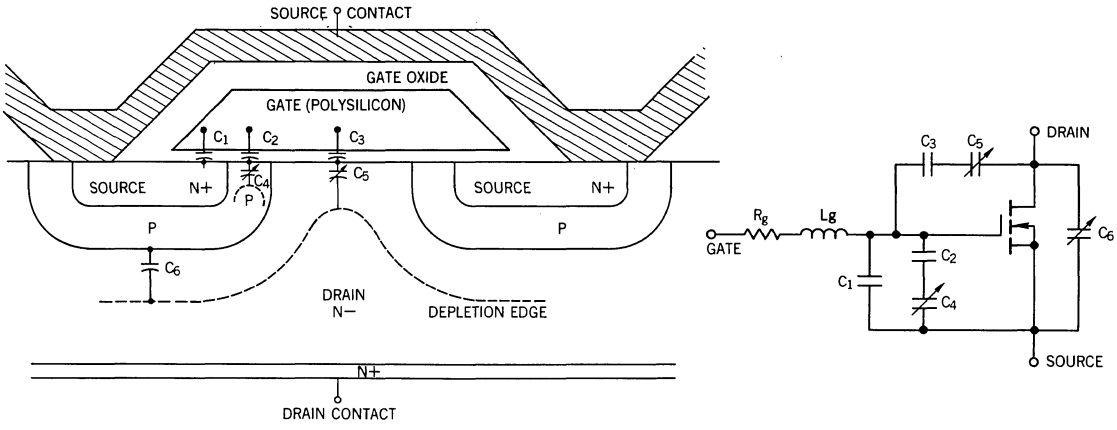

FIGURE 1 - SIMPLIFIED CROSS SECTION OF A POWER MOSFET CELL AND ITS ELECTRICAL EQUIVALENT.

due to the depletion region between source and drain and varies with the gate voltage. Its contribution causes total gate-source capacitance to increase 10-15% as the gate voltage goes from zero to Vg(th).

4. C3 + C5 is also made up of a fixed dielectric capacitance plus a value which becomes significant when the drain to gate voltage potential reverses polarity.

   C6 is the drain-source capacitance and while it also varies with drain voltage, it is not a significant factor with respect to switching times.

EVALUATING FET PARASITIC ELEMENTS

Although it is clearly not the best way to drive a power MOSFET, using a constant gate current to turn the device on allows visualization of the capacitive effects as they affect the voltage waveforms. Thus the demonstration circuit of Figure 2 is configured to show the gate dynamics in a typical buck-type switching regulator circuit. This simulates the inductive switching of a large class of applications and is implemented here with a UFN-510 FET, which is a 4 amp, 100V device with the following capacitances:

$$\left.\begin{array}{lll} Ciss \approx C1 + C4 + C5 = & 135 - 150\ pF \\ Crss \approx C5 = & 20 - 25\ pF \\ Coss \approx C5 + C6 = & 80 - 100\ pF \end{array}\right\} \quad Vgs = 0V$$

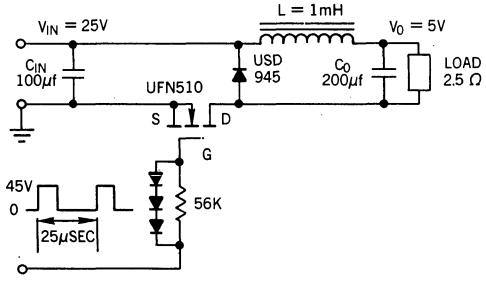

FIGURE 2 - SWITCHING TIME EVALUATION CIRCUIT.

In this illustration, the load portion of the circuit is established with Vin = 25V, Io = 2A, and f = 25Khz. The resultant turn-on waveforms are shown in Figure 3 from which the following observations may be made:

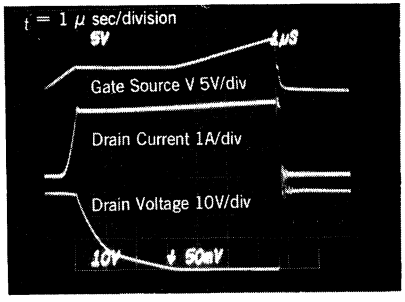

FIGURE 3 - FET TURN-ON SWITCHING CHARACTERISTICS WHEN DRIVEN WITH A CONSTANT GATE CURRENT

1. For a fixed gate drive current, the drain current rise time is 5 times faster than the voltage fall time.

2. There is a 10-15% increase in gate capacitance when the gate voltage reaches Vg(th).

3. The gate voltage remains unchanged during the entire time the drain voltage is falling because the Miller effect increases the effective gate capacitance.

4. The input gate capacitance is approximately twice as high when drain current is flowing as when it is off.

5. The drain voltage fall time has two slopes because the effective drain-gate capacitance takes a signifcant jump when the drain-gate potential reverses polarity.

6. Unless limited by external circuit inductance, the current rise time depends upon the large signal g_M and the rate of change of gate voltage as $\Delta Id = g_M \Delta Vg$

CHANGES IN EFFECTIVE CAPACITANCE

The waveform drawings of Figure 4 illustrate the dynamic effects which take place during turn-on. As the gate voltage rises from zero to threshold, C2 is not significant since C4 is very small. At threshold, the drain current rises quickly while the drain voltage is unchanged. This, of course, is due to the buck regulator circuit configuration which will not let the voltage fall until all the inductor current is transfered from the free-wheeling diode to the FET.

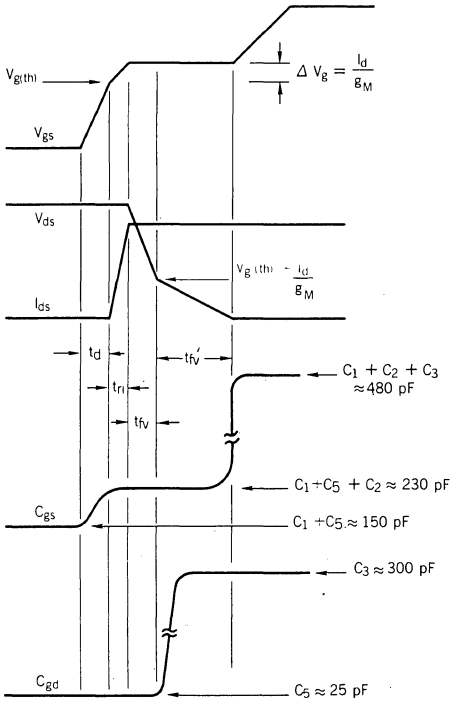

FIGURE 4 - PARASITIC CAPACITANCE VARIATION FOR A UFN510 MOS FET DURING TURN-ON

While the drain current is increasing, there is a slight increase in the gate capacitance due to the large current density underneath the gate in the N-region close to the P areas.

As the drain voltage begins to fall, its slope depends upon gate to drain capacitance and not that from gate to source. During this time, all the gate current is utilized to charge this gate to drain capacitance and no change in gate voltage is observed. This capacitance initially increases slightly as the voltage across it drops but then there is a significant jump in value when the drain voltage falls lower than the gate. When the polarity reverses from drain to gate, a surface charge accumulation takes place and the entire gate structure becomes part of the gate to drain capacitance. At this point the drain voltage fall time slows for the duration of its transition.

AN OPTIMUM GATE DRIVE

In most switching power supply applications, if a step function in gate current is provided, the drain current rise time is several times faster than the voltage fall time. This can result in substantial switching power losses which are most often combated by increasing the gate drive current. This creates a problem, however, in that it further reduces current rise time which can cause overshoot, ringing, EMI and power dissipation due to recovery time for the rectifiers which are much happier with a more slowly changing drain current.

In an effort to meet these conflicting requirements, an idealized gate current waveform was derived based upon the goal of making the voltage fall time equal to the current rise time. This optimum gate current waveform is shown in Figure 5 and consists of the following elements.

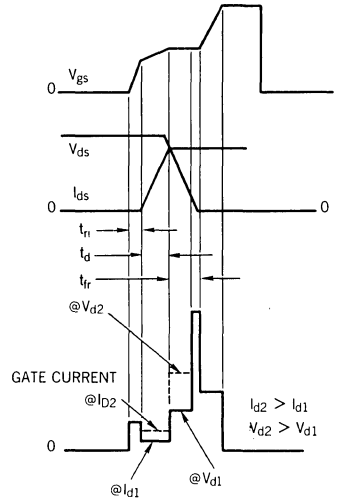

FIGURE 5 - AN "IDEAL" GATE CURRENT TURN-ON DRIVE TO PROVIDE EQUAL CURRENT RISE AND VOLTAGE FALL TIMES WITH AN INDUCTIVE LOAD

1. An initial fast pulse to get the gate voltage up to threshold.
2. A lesser amount to slow the drain current rise time. This value however, will also be a function of the required drain current.
3. Another increase to get the drain voltage to fall rapidly with a large current pulse added when the drain gate potential reverses.
4. A continued amount to allow the gate voltage to charge to its final value.

Obviously this might be a little difficult to implement in exact form, however, it can be approximated by a gate current waveform which, instead of being constant, has a rise time equal to the desired sum of the drain current rise time and the voltage fall time, and a peak value high enough to charge the large effective capacitance which appears during the switching transition. The peak current requirement can be calculated on the basis of defining the amount of charge required by the parasitic capacitance through the switching period.

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A linear current ramp will deliver a charge equal to

$$Q = \frac{Ip \cdot ton}{2} \quad \text{where we define} \quad ton = td + tri + tfv$$

The total charge required for switching is

$$Q = Ciss\,[Vg\,(th) + \frac{Id}{g_M}] + Crss\,[V_{DD} - Vg\,(th)] + Crss' Vg\,(th)$$

where Crss' is the gate-drain capacitance after the polarity has reversed during turn-on and is related to Ciss by the basic geometry design of the device. A reasonable approximation is that $Crss' \approx 1.5$ Ciss. With this assumption,

$$Ip \approx \frac{2}{ton}\,[Ciss\,(2.5\ Vg\,(th) + \frac{Id}{g_M}) + Crss\,(V_{DD} - Vg\,(th))]$$

As an example, if one were to implement a 40 V, 10A buck regulator with a UFN150, it would not be unreasonable to extend the total switching time to 50 nsec to accomodate rectifier recovery time. An optimim drive current for this application would then take 50 nsec to ramp from zero to a peak value calculated from

Ciss = 2000 pF	ton = 50 nsec
Crss = 350 pF	V_{DD} = 40 V
Vg(th) = 3 V	Id = 10 A

$$g_M = \frac{10A}{2.5\ V} = 4\ s$$

$$\text{as } Ip = \frac{2}{50 \times 10^{-9}}[2000 \times 10^{-12}(2.5 \times 3 + \frac{10}{4}) + 350 \times 10^{-12}(40 - 3)]$$

$\therefore$ Ip = 1.32 amps peak

The above has shown that while high peak currents are necessary for fast power MOSFET switching, controlling the rise time of the gate current will yield a more well-behaved system with less stress caused by rectifier recovery times and capacitance. This type of switching requirement can be fulfilled with integrated circuit technology and several IC's have been developed and applied as MOSFET drivers.

FET DRIVER IC'S

In searching for IC's capable of providing the high peak currents required by power MOSFETS, one of the first devices which became popular was DS0026 shown in Figure 6. While this IC was originally designed to be a clock driver for MOS logic, it was capable of supplying up to 1.5 amps as either a source or sink. In addition, it was made with a gold doped, all-NPN process which minimizes storage delays and, as a result, offers transition times of approximately 20 nsec. Its disadvantage is that pull-up resistors R3 and R4 require excessive supply current when the output is in the low state.

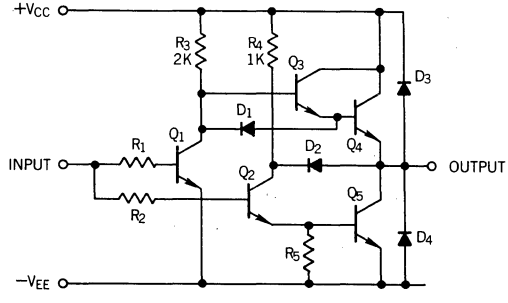

FIGURE 6 - A SIMPLIFIED SCHEMATIC OF THE DS0026 DRIVER IC

The first PWM IC's to include FET compatible output stages were the 1525A, followed by the 1526. Both of these designs feature push-pull outputs, each of which is configured as shown in Figure 7. Again with source and sink – this time driven by constant current sources – these devices can provide high FET switching drive with low stand-by current regardless of the state of the outputs. Frustratingly, these designs also suffer from some limitations. First, the maximum peak current is approximately ½ amp which is just not adequate for larger geometry FET's and, secondly, there are delays in turning off the output transistors which allow a high cross conduction current from Vc to ground as the conduction of source and sink overlap at each switch transition. This current spiking is shown in Figure 8 and while its not too much of a problem at low frequencies, at 200 KHz the internal power dissipation of the IC increases by a factor of 3 - 4.

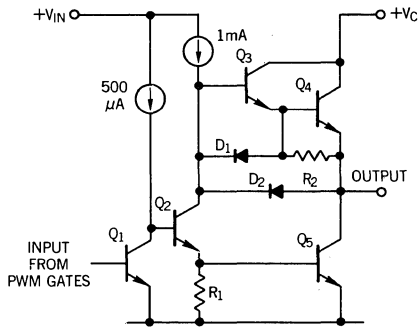

FIGURE 7 - ONE OF TWO OUTPUT STAGES FOUND IN THE 1525A and 1527A IC's

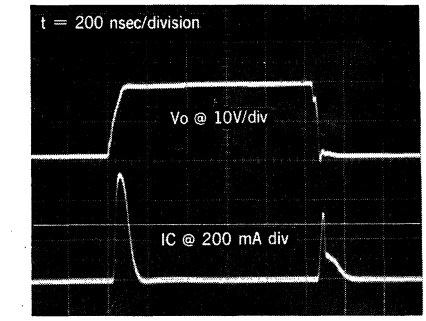

FIGURE 8 - CROSS-CONDUCTION CURRENT IN THE 1525A OUTPUT STAGE

INTRODUCING THE UC1706

This brings us to a new IC designed specifically as a power MOSFET driver compatible with PWM circuits for switching power supplies. As seen from the block diagram shown in Figure 9, this device is an interface circuit based upon the philosophy that the analog PWM control circuitry can best be done on a separate chip from the digital output driving stages. The UC1706 is made with a high-speed, high-voltage Schottky clamped process and while it isn't as fast as the DS0026, it does have delay times of only 100nsec while requiring much less supply current.

Referring again to Figure 9 it can be seen that the UC1706 is designed to provide three basic functions:

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UC1706 BLOCK DIAGRAM

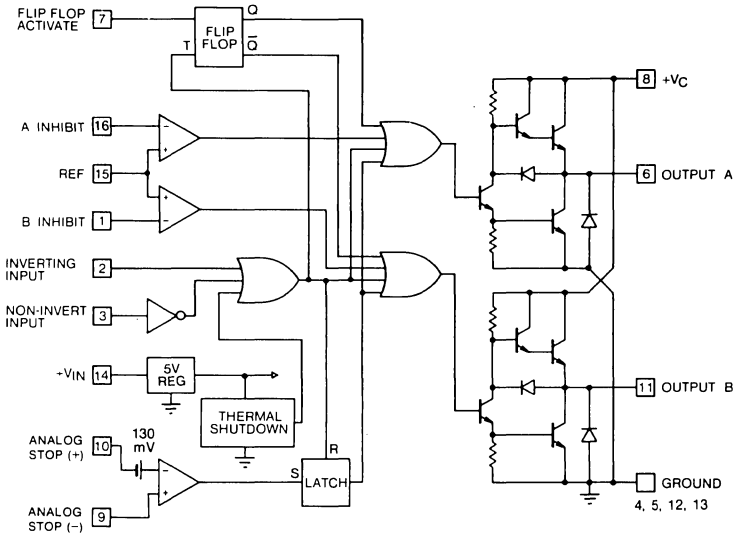

FIGURE 9 - UC1706 BLOCK DIAGRAM.

1. The main feature of this chip is a pair of totem-pole output stages, each designed to provide peak currents of 1.5 amp source or sink, with a fast turn-off optimized to minimize cross-conduction current.

2. With an internal flip-flop, the UC1706 will accept a single-ended PWM signal and drive the outputs alternately for push-pull or bridge applications. This flip-flop can be externally disabled so both outputs work in parallel. They can then be combined for 3A peak operation. Inputs can be of either polarity insuring compatibility with all available PWM chips, i.e. UC1840, UC1842, NE5560, MC30060, NE5561, etc.

3. Several protection functions associated with output drive are also included in the UC1706. These include a latching analog comparator with a 130mV threshold useful for pulse-by-pulse current limiting, an inhibit circuit designed for automatic dead-band control when slower bipolar power transistors are used as the final power switch, and thermal shutdown for it's own protection.

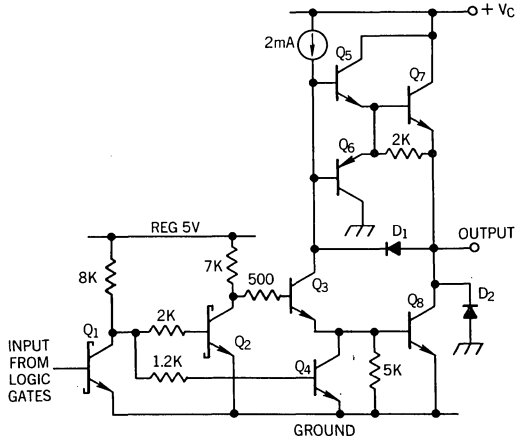

FIGURE 10- ONE OF TWO OUTPUT CIRCUITS CONTAINED WITHIN THE UC1706

INSIDE THE UC1706

The schematic of one of the output circuits in the UC1706 is shown in Figure 10. While appearing as a fairly conventional totem-pole design, the subtleties of this circuit are the slowing of the turn-off of Q3 and the addition of Q4 for rapid turn-off of Q8. The result is shown in Figure 11 where it can be seen that while maintaining fast transitions, the cross-conduction current spike has been reduced to zero when going low and only 20nsec with a high transition. This offers negligible increase in internal circuit dissipation at frequencies in excess of 500Khz.

The overall transition time through the UC1706 is shown in Figure 12 with the upper photograph recording the results with a drive to the inverting input while the lower picture is with the non-inverting input driven. Note that the only difference in speed between the two inputs is an additional 20nsec delay in turning off when the non-inverting input is used. (Note- here and in all further discussions, ON or OFF relates to the driven output power switch, i.e., ON is with the UC1706 output high and vice versa. The shutdown, blanking, and protective functions all force the UC1706 output low when active).

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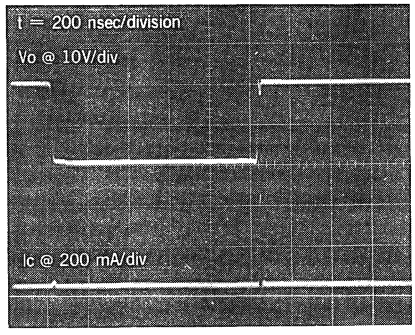

FIGURE 11- CROSS CONDUCTION CURRENT IN THE UC1706 OUTPUT STAGE

Note that the rise and fall times of the output waveform average 20nsec with no load, 40nsec with 1000pF, and 60nsec when the capacitive load is 2200 pF.

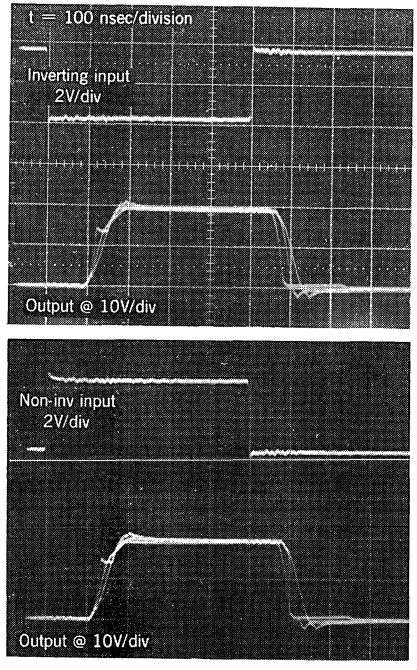

FIGURE 12- SWITCHING RESPONSE WITH OUTPUT CAPACITANCE OF 0, 1000, AND 2200 PF.

The peak output current of each output, either source or sink, is 1.5A but with the flip/flop externally disabled, the outputs may be paralled for peak currents of 3 amps as shown in Figure 13. Saturation voltage is high at this level but falls to under 2V at 500 mA per output.

It should be noted that while optimized for FET drive, the UC1706 is equally at home when driving bipolar NPN transistors. The saturation voltage in the low state, after the turn-off transient, is less than 0.4 volt at currents to 50mA.

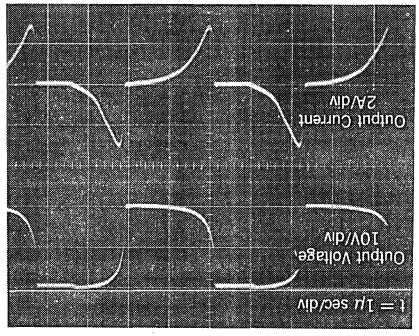

FIGURE 13- PEAK OUTPUT CURRENT WITH BOTH OUTPUTS OF THE UC1706 CONNECTED IN PARALLEL. CL = 0.1 μF

The input logic circuitry of the UC1706 is shown in Figure 14. Since it is driven from an internally regulated 5 volt supply, TTL compatibility is assured with the driving signal only required to sink less than 1.0 mA. Input Zener clamps are included so that higher driving voltages may be used as long as the current is limited to less than 10 mA. While external pull-up resistors may speed-up the drive signal, they are not required.

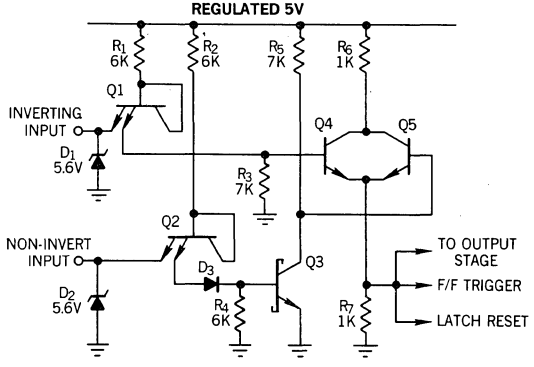

FIGURE 14- INPUT LOGIC IN THE UC1706

The logic configuration is such to favor an output low. To get the output high requires both a low Inverting input and a high N.I. input. An output low is achieved with either a high Inv. input or a low N.I. input. To put it another way: if the Inv. input is used, the N.I. input must be high or open. Using the N.I. input requires that the Inv. input be held low. Obviously, one input could be used to override the other to force a shutdown.

Note that the output from the logic gate performs three functions when going high: it blanks both output stages to OFF, changes the state of the flip-flop, and resets the internal shutdown latch. These last two functions require at least 200nsec which means the input signal must have an off-time of at least that duration. By triggering the flip-flop from the same signal that drives the outputs, double-pulsing is prevented. When one output turns off, only the other one can turn on next, regardless of the intervening time.

SUPPLYING POWER TO THE UC1706

From the block diagram of Figure 9, note that the UC1706 has two supply terminals: Vin on pin 14 and Vc on pin 8. These pins can be driven from the same or different voltages and either can range from 5 to 40 volts. Vin drives both the input logic and the current sources providing the pull-up for the outputs. Thus Vin also can be used to activate the outputs and no current is drawn from Vc when Vin is low. Thus the UC1706 interfaces conveniently with the UC1840 Off-Line PWM Controller where low-current start-up is desired. Figure 15 shows this application where Vin is powered from the Drive Bias switch in the UC1840. In this way, the UC1706 draws no supply current while C2 initally charges through R3. R3 only has to provide 5.5 mA for the UC1840 plus the start threshold divider of R1 and R2. When there is adequate charge in C2, the start command from the UC1840 activates the UC1706 which, in turn, drives Q1 bringing up sustaining low-voltage power from N2 of the power transformer.

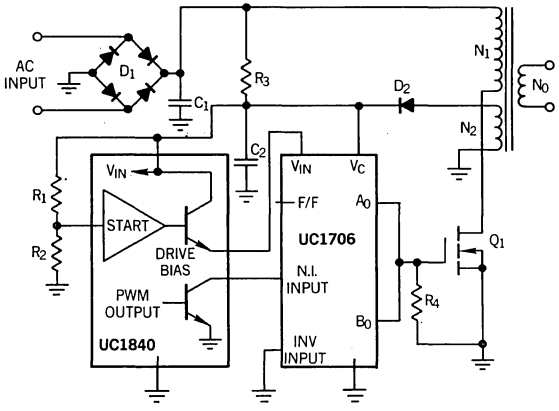

FIGURE 15- POWERING THE UC1706 FROM THE UC1840 PWM CONTROLLER

In applications where the PWM control is desired to be referenced to the load, or secondary side of the isolation transformer, the UC1706 can still be operated on the primary side for direct coupling to the power switch. With this topology, a secondary referenced auxilliary power source is necessary to operate the control circuitry whose output pulses can be either transformer or optically coupled to the input to the UC1706 on the primary side. Since only gate capacitance charging current is required from the source, at lower frequencies it is feasable to supply all the drive power directly from the line via Rin and Cin as shown in Figure 16.

In this configuration, it's still helpful to use a threshold switch with hysteresis to apply power to the UC1706 so that there is no possibility of turning on the power switch until the input voltage is adequate. Q1-Q3 implement a discrete version of such a switch.

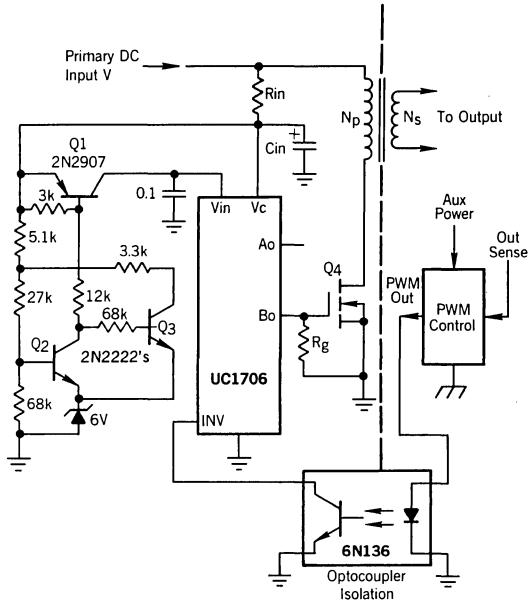

FIGURE 16- TRANSISTORS Q1 - Q3 FORM A HYSTERESIS SWITCH TO ENERGIZE THE UC1706 WHEN THE VOLTAGE ON CIN HAS CHARGED TO 15V. ISOLATED PWM DRIVE CAN BE WITH EITHER AN OPTICAL COUPLER AS SHOWN OR WITH A SMALL TRANSFORMER

DIRECT COUPLED MOSFET DRIVE

The circuit of Figure 17 shows the simplest interface to a power MOSFET - in this case the UFN 150, a large geometry 100V, 40A device with a gate capacity of typically 2000 pF. Only one output of the UC1706 was used for this demonstration and the load was the buck regulator circuit described earlier. As indicated by the use of a sense resistor in the source line, this circuit was also used to evaluate the capability of the latched shutdown comparator as a current limiter.

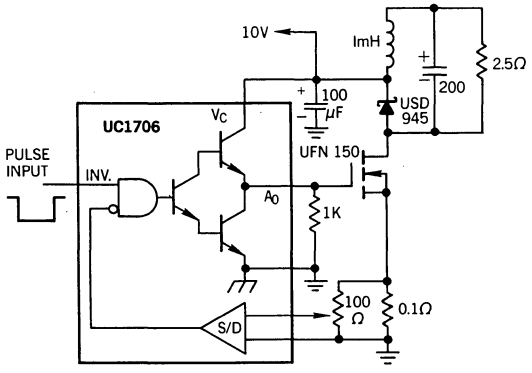

FIGURE 17 - DIRECT FET DRIVE WITH THE UC1706 WITH CURRENT SENSING IN THE SOURCE LEAD.

While directly connecting the FET gate to the output of the UC1706 is both simple and fast, it must be done with care as any wiring inductance can cause severe ringing which could take the gate voltage past its allowable limits. Usually, it merely requires some series resistance in the gate circuit to damp this ringing, but this is at the expense of switching speed as the gate resistance reacts with the input capacitance. Another justification of gate resistance is to slow switching to accommodate output rectifier recovery time as mentioned earlier in this paper.

For this example, however, maximum speed was desired and considerable care was taken to minimize lead inductance with the results as shown in Figure 18 and with an expanded time base for turn-on, in Figure 19. These photos show the requirements of this FET for one amp peak gate current at turn-on and turn-off with the hesitation in gate voltage rise time at threshold as the falling drain voltage robs gate current through the gate-drain capacitance. The drain current spike at turn-on is due to the recovery of the freewheeling diode in the output load.

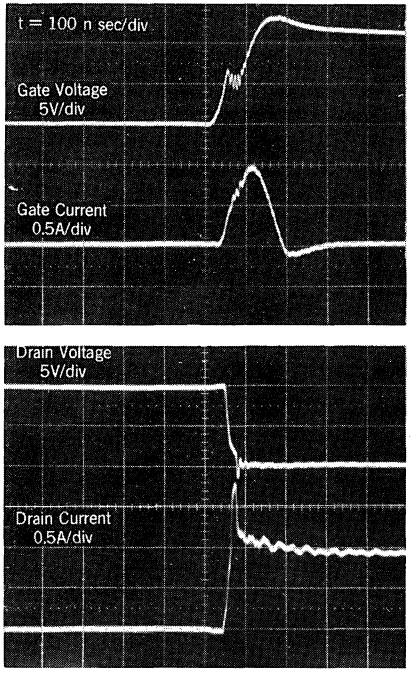

FIGURE 18- DIRECT COUPLED POWER MOS FET DRIVE

In order to evaluate the threshold of the shutdown comparator, the buck regulator circuit load on the drain was replaced with a wire wound resistor whose inductance provided a slower turn-on of drain current. Since it is a latching circuit, this comparator is another area where considerable care must be taken to eliminate the possibility of noise triggering. These problems are eased somewhat since the inputs are differential with a large common-mode range capability and the threshold of 130 mV is built in. However, these inputs should still be connected to the current sensor as a closely coupled, and perhaps even shielded pair.

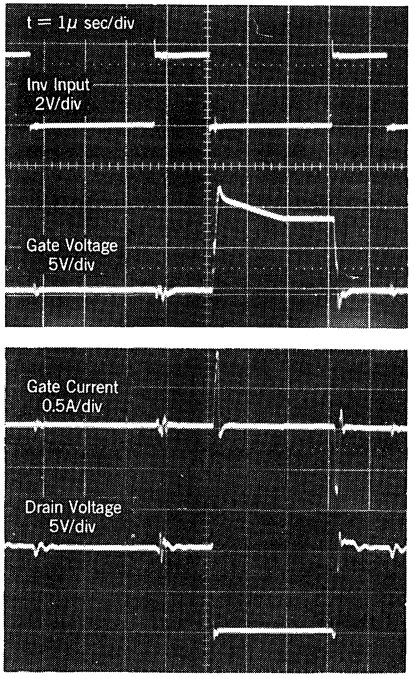

FIGURE 19- DIRECT DRIVE TURN-ON WITH EXPANDED TIME SCALE

For this example, a 0.1 ohm non-inductive resistor was used as a current sensor with a 100 ohm potentiometer used to adjust the current threshold to 2 amps. The multiple exposure print of Figure 20 shows the effect of increasing load current. At 2 amps, the comparator begins to reduce the pulse width. As current increases, the comparator is overdriven and its response time quickens to approximately 200nsec plus the turn-off time of the power switch. Beyond this point, one must rely on circuit inductance or go to more elaborate means to clamp the current.

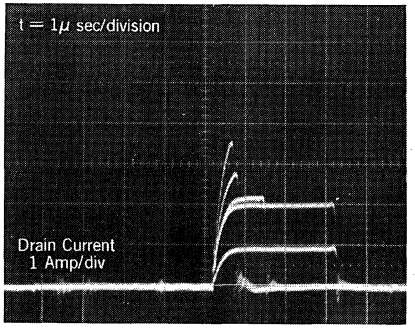

FIGURE 20- CURRENT LIMITING WITH THRESHOLD SET FOR 2 amps

ISOLATED GATE DRIVE

The single-ended transformer-coupled drive circuit shown in Figure 21 is often useful for either isolation or to optimally match the voltage and current between the driving source and the gate. In this case, outputs A and B were paralleled merely to get close to 100% modulation - the full output current capability was not required as the transformer provided additional current gain. Since this is a unipolar drive, capacitor C1 is used to block the DC voltage and provide adequate volt-seconds for core reset. C2 and the zener diode provide DC restoration and clamp the gate to only one diode drop negative. The 10V positive clamp of the zener also protects the gate from any transient overshoot.

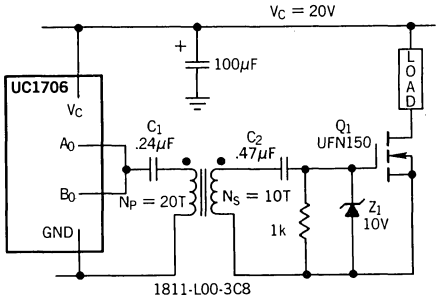

FIGURE 21 - BOTH UC1706 OUTPUTS ARE COMBINED FOR A SINGLE-ENDED TRANSFORMER-COUPLED DRIVE.*

The criteria for the transformer design was the arbitrary specification to keep the magnetization current to less than 50 mA to keep the steady-state power consumption low. Magnetization current may be made lower with more transformer turns which yields higher leakage inductance and slower response. In this circuit, with f = 100 kHz, $\tau = 10\ \mu$ sec, and Vin = 20V,

$$Lm = \frac{Vin \cdot \tau}{2\ Im} = \frac{20 \times 10 \times 10^{-6}}{2 \times 50 \times 10^{-3}} = 2\ mH$$

and since $L = A_L N^2 \times 10^{-6}$ mH, for a 1811P-L00-3C8 core

$$Np = \sqrt{\frac{Lx10^6}{A_L}} = 20\ turns$$

and Ns was made equal to 10 turns for a 10V output.

With this design, the energy stored in the core is

$$E = \tfrac{1}{2}\ Lm\ Im^2 = .05\ \mu J$$

which is considerably below the saturation level of

$$E = \frac{B^2\ Ae\ le \times 10^{-8}}{2\ \mu e} = \frac{2000^2 \times .43 \times 2.58 \times 10^{-8}}{2 \times 1930} = 11.4\ \mu J$$

The coupling capacitor value was defined by setting a requirement that it charge to no more than 10% of Vin with each pulse.

$$C_1 = \frac{Im\ \tau}{0.1\ Vin} = \frac{50 \times 10^{-3} \times 10 \times 10^{-6}}{0.1 \times 20} = .25\ \mu F$$

*Circuit design courtesy of J. Potasse, Canadair Limited.

The resultant waveforms through this circuit are shown in Figure 22. Note that when switching is complete,the gate circuit goes to a high impedance and the transformer leakage inductance causes a slight voltage over-shoot at both the gate and at the output of the UC1706. Otherwise, these waveforms should be self-explanatory.

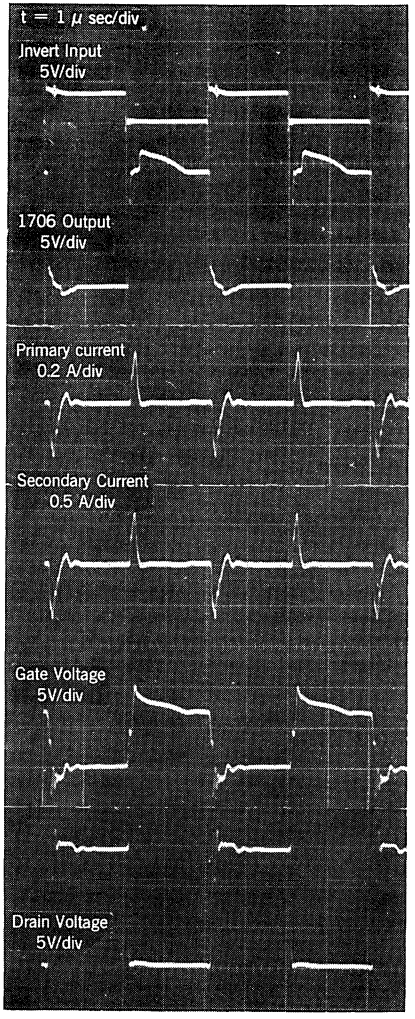

FIGURE 22 - SINGLE ENDED TRANSFORMER COUPLED PERFORMANCE

PUSH-PULL TRANSFORMER COUPLING

The totem-pole outputs of the UC1706 can easily be interfaced for balanced transformer drive as shown in Figure 23. A and B outputs are alternating now as the internal flip-flop is active and the output frequency is halved. Note that when one UC1706 output goes high, the other is held low and both are low during the dead time between output pulses.

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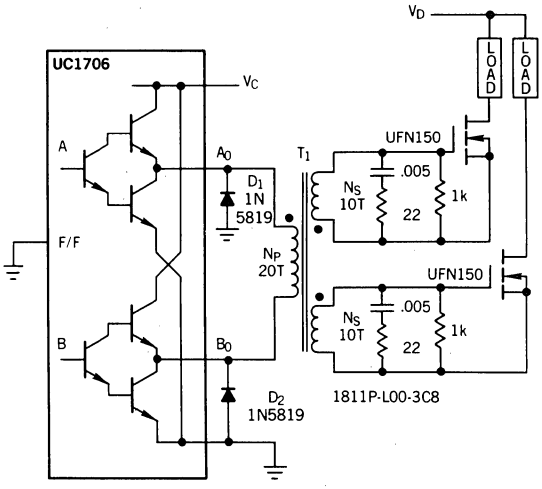

FIGURE 23 - BALANCED PUSH-PULL TRANSFORMER COUPLING

For this circuit, the same transformer as in the previous example was used except that now there are two identical secondary windings. With balanced operation, no coupling capacitor is necessary as there is no net DC current through the primary.

One precaution which must be taken however, is that transformer leakage inductance may force the output of the UC1706 negative when it turns off. If both the frequency and current are low, the output diodes in the UC1706 may suffice for clamping. Otherwise, external diodes as shown in Figure 23 should be added. An added complication of transformer leakage inductance is the requirement for snubbing circuits to keep the gate voltage ringing under control.

Again, waveforms at all significant points within this circuit are shown in Figure 24.

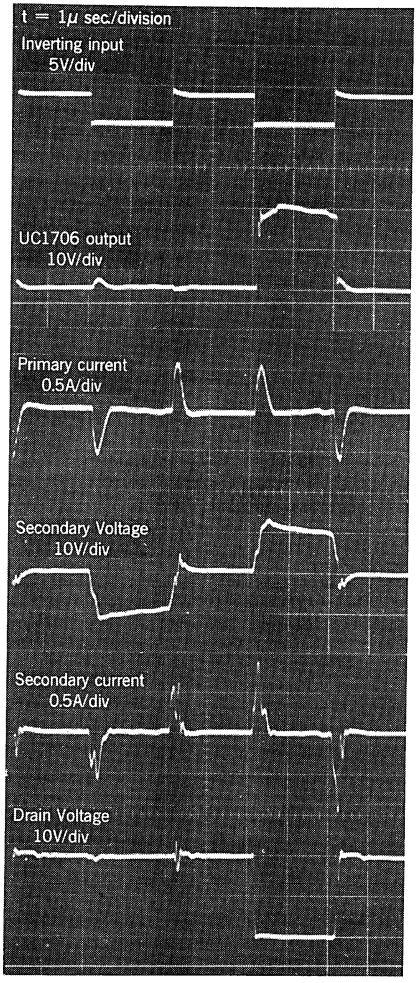

FIGURE 24 - BALANCED PUSH-PULL TRANSFORMER COUPLING PERFORMANCE.

A SQUARE WAVE INVERTER EXAMPLE

To illustrate the usage of the UC1706 as a bipolar transistor switch driver, a simple square wave generator is shown in Figure 25, with the operating

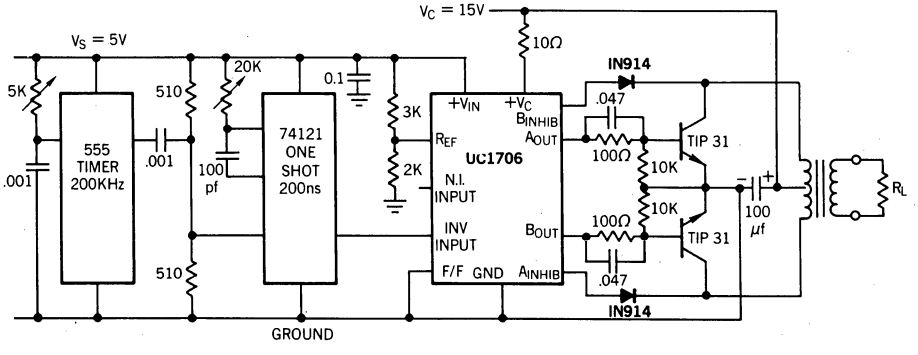

FIGURE 25 - A SQUARE WAVE INVERTER CIRCUIT USING THE UC1706 TO DRIVE BIPOLAR TRANSISTOR SWITCHES.

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circuit waveforms pitured in Figure 26. This application demonstrates the advantages in using the UC1706 to efficiently drive relatively slow transistors in high-speed applications.

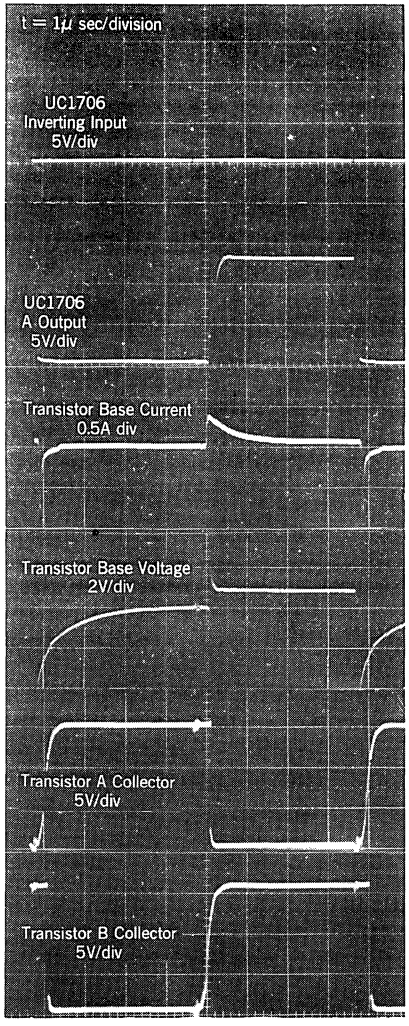

FIGURE 26- BIPOLAR SQUARE WAVE GENERATOR WAVEFORMS

This circuit starts with a 555 timer oscillating at 200 kHz to establish the operating frequency of the inverter at 100 kHz.

Its output triggers the 74121 one-shot which provides an input pulse to the UC1706. This signal is actually the off-time or blanking pulse to the outputs. For an ideal push-pull square wave generator, its pulse width should be zero. If the storage time of the power switches were a known constant, then this pulse width could be adjusted such that one switch turns on just as the other comes out of saturation. Since this is not very realistic and since the UC1706 needs 200nsec to switch from one output to the other, that's the pulse width set by the one-shot.

The high-current output from the UC1706 is utilized with .047 mfd speed-up capacitors to provide one amp of peak turn-on current, 100 mA of drive, and 1.5A turn-off, thus reducing the typical 2 micro-second turn-off time of the TIP-31 to approximately 400nsec. Since this is still longer then the blanking pulse, conduction overlap would take place were it not for the use of the inhibit circuit of the UC1706 which is connected to the outputs through the 1N914 diodes. This circuit insures that regardless of the input, side A will not turn on until the diode connected to side B's collector rises above the reference established by the 3K/2K divider. Wayeform photos of this inhibit action are shown in Figure 27. There is now a dead time resulting from the inhibit delay in the UC1706 plus the turn-on delay of the TIP-31 which can be used to advantage to allow time for the output rectifiers to recover.

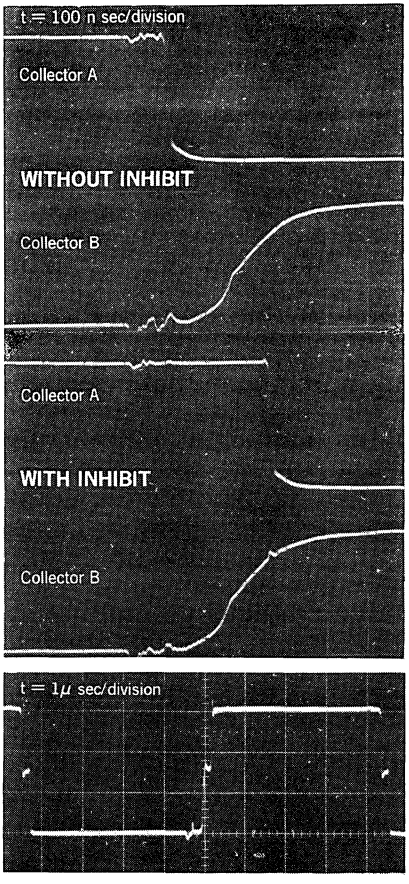

FIGURE 27- SQUARE WAVE GENERATOR OUTPUT WITH INHIBIT - CONTROLLED DEADBAND

9

SUMMARY

This paper has attempted to present an understanding of the dynamics of high-speed power MOSFET switching to aid in defining optimum gate drive signals to meet specific applications. The need for high peak gate currents with controlled rise times has led to the development of several integrated circuits aimed toward these goals. The most recent of these, the UC1706, provides high-speed response, three amps of peak current, and the ease of implementing either direct or transformer drive to a broad range of MOS FET devices. With this new device one more specialized function has been developed to further aid the power supply designer simplify his tasks.

UC3842/3/4/5 PROVIDES LOW-COST CURRENT-MODE CONTROL

INTRODUCTION

The fundamental challenge of power supply design is to simultaneously realize two conflicting objectives: good electrical performance and low cost. The UC3842/3/4/5 is an integrated pulse width modulator (PWM) designed with both these objectives in mind. This IC provides designers an inexpensive controller with which they can obtain all the performance advantages of current mode operation. In addition, the UC3842 series is optimized for efficient power sequencing of off-line converters, DC to DC regulators and for driving power MOSFETs or transistors.

This application note provides a functional description of the UC3842 family and highlights the features of each individual member, the UC3842, UC3843, UC3844 and UC3845. Throughout the text, the UC3842 part number will be referenced, however the generalized circuits and performance characteristics apply to each member of the UC3842 series unless otherwise noted. A review of current mode control and its benefits is included and methods of avoiding common pitfalls are mentioned. The final section presents designs of power supplies utilizing UC3842 control.

CURRENT-MODE CONTROL

Figure 1 shows the two-loop current-mode control system in a typical buck regulator application. A clock signal initiates power pulses at a fixed frequency. The termination of each pulse occurs when an analog of the inductor current reaches a threshold established by the error signal. In this way the error signal actually controls peak inductor current. This contrasts with conventional schemes in which the error signal directly controls pulse width without regard to inductor current.

Several performance advantages result from the use of current-mode control. First, an input voltage feed-forward characteristic is achieved; i.e., the control circuit instantaneously corrects for input voltage variations without using up any of the error amplifier's dynamic range. Therefore, line regulation is excellent and the error amplifier can be dedicated to correcting for load variations exclusively.

For converters in which inductor current is continuous, controlling peak current is nearly equivalent to controlling average current. Therefore, when such converters employ current-mode control, the inductor can be treated as an

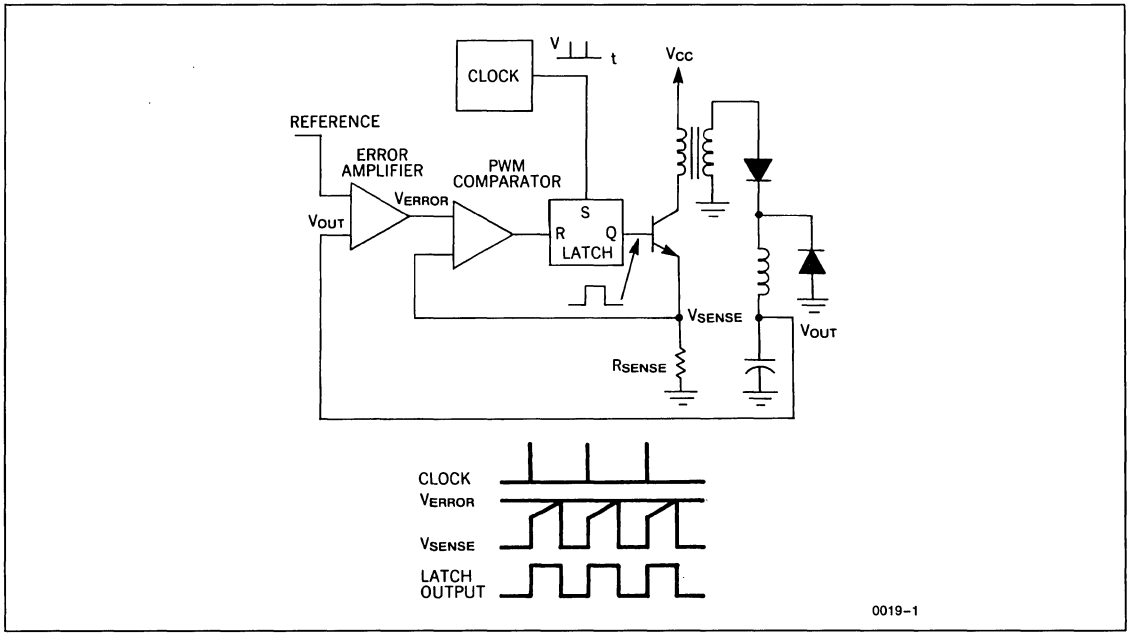

Figure 1. Two-Loop Current-Mode Control System

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error-voltage-controlled-current-source for the purposes of small-signal analysis. This is illustrated by Figure 2. The two-pole control-to-output frequency response of these converters is reduced to a single-pole (filter capacitor in parallel with load) response. One result is that the error amplifier compensation can be designed to yield a stable closed-loop converter response with greater gainbandwidth than would be possible with pulse-width control, giving the supply improved small-signal dynamic response to changing loads. A second result is that the error amplifier compensation circuit becomes simpler, as illustated in Figure 3. Capacitor C_i and resistor R_{iz} in Figure 3a add a low frequency zero which cancels one of the two control-to-output poles of non-current-mode converters. For large-signal load changes, in which converter response is limited by inductor slew rate, the error amplifier will saturate while the inductor is catching up with the load. During this time, C_i will charge to an abnormal level. When the inductor current reaches its required level, the voltage on C_i causes a corresponding error in supply output voltage. The recovery time is $R_{iz}C_i$, which may be quite long. However, the compensation network of Figure 3b can be used where current-mode control has eliminated the inductor pole. Large-signal dynamic response is then greatly improved due to the absence of C_i.

Current limiting is greatly simplified with current-mode control. Pulse-by-pulse limiting is, of course, inherent in the control scheme. Furthermore, an upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

Finally, current-mode controlled power stages can be operated in parallel with equal current sharing. This opens the possibility of a modular approach to power supply design.

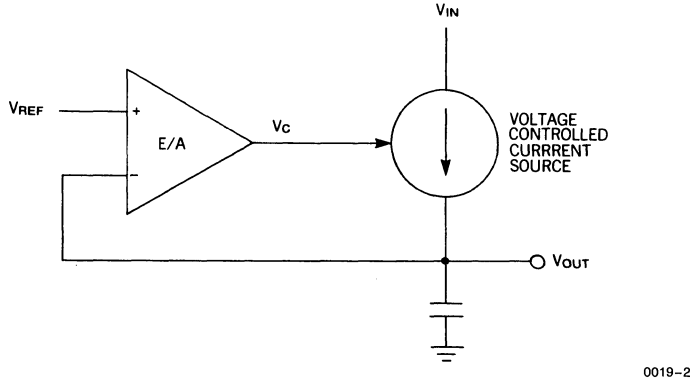
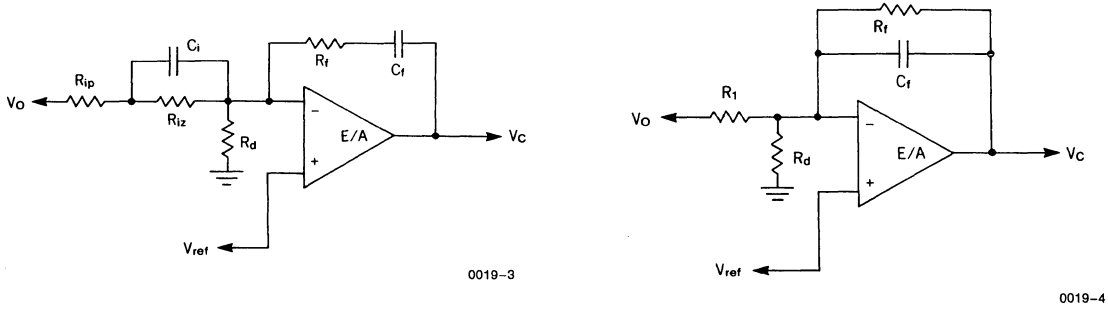


Figure 2. Inductor Looks Like a Current Source to Small Signals



A) Direct Duty Cycle Control **B) Current Mode Control**

Figure 3. Required Error Amplifier Compensation for Continuous Inductor Current Designs

THE UC3842/3/4/5 SERIES OF CURRENT-MODE PWM IC'S

DESCRIPTION

The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving either N Channel MOSFETs or bipolar transistor switches, is low in the off state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.5V and 7.9V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to <50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flip which blanks the output off every other clock cycle.

FEATURES

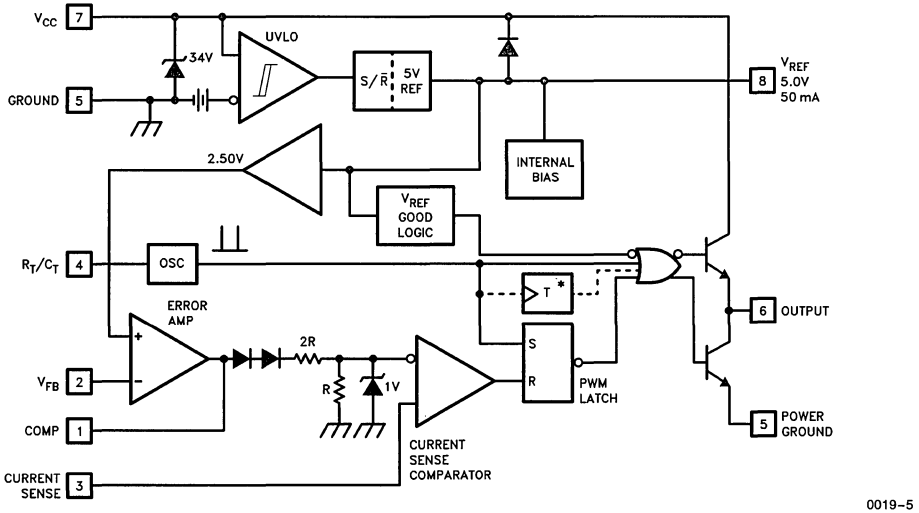
- Optimized for Off-Line and DC to DC Converters
- Low Start Up Current (<1 mA)
- Automatic Feed Forward Compensation
- Pulse-By-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-Voltage Lockout with Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500 kHz Operation
- Low R_O Error Amp

IC SELECTION GUIDE

UVLO START	MAXIMUM DUTY CYCLE	
	<50%	<100%
8.5V	UC3845	UC3843
16V	UC3844	UC3842

RECOMMENDED USAGE

APPLICATION (CIRCUIT)	POWER SUPPLY INPUT (V)	
	HIGH (OFFLINE)	LOW (DC/DC)
FLYBACK	UC3844	UC3845
FORWARD	UC3844/2	UC3845/3
BUCK/BOOST	UC3842/4	UC3843/5



*3844 and 3845 Only

Figure 4

UNDER-VOLTAGE LOCKOUT

The UVLO circuit insures that V_{CC} is adequate to make the UC3842/3/4/5 fully operational before enabling the output stage. Figure 5 shows that the UVLO turn-on and turn-off thresholds are fixed internally at 16V and 10V respectively. The 6V hysteresis prevents V_{CC} oscillations during power sequencing. Figure 6 shows supply current requirements. Start-up current is less than 1 mA for efficient bootstrapping from the rectified input of an off-line converter, as illustrated by Figure 6. During normal circuit operation, V_{CC} is developed from auxiliary winding W_{AUX} with D_1 and C_{IN}. At start-up, however, C_{IN} must be charged to 16V through R_{IN}. With a start-up current of 1 mA, R_{IN} can be as large as 100 kΩ and still charge C_{IN} when V_{AC} = 90V RMS (low line). Power dissipation in R_{IN} would then be less than 350 mW even under high line (V_{AC} = 130V RMS) conditions.

During UVLO; the output driver is in a low state. While it doesn't exhibit the same saturation characteristics as normal operation, it can easily sink 1 milliamp, enough to insure the MOSFET is held off.

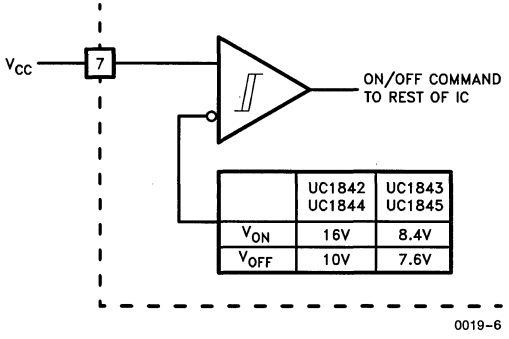


Figure 5

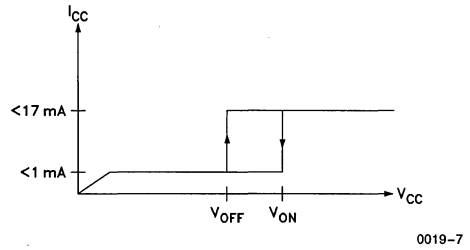


Figure 6. During Under-Voltage Lockout, the output driver is biased to sink minor amounts of current.

OSCILLATOR

The UC3842 oscillator is programmed as shown in Figure 8. Timing capacitor C_T is charged from V_{REF} (5V) through the timing resistor R_T, and discharged by an internal current source.

The first step in selecting the oscillator components is to determine the required circuit deadtime. Once obtained, Figure 9 is used to pinpoint the nearest standard value of C_T for a given deadtime. Next, the appropriate R_T value is interpolated using the parameters for C_T and oscillator frequency. Figure 10 illustrates the R_T/C_T combinations versus oscillator frequency. The timing resistor can be calculated from the following formula.

$$F_{OSC}\ (kHz) = 1.72 / (R_T\ (k) \times C_T\ (\mu f))$$

The UC3844 and UC3845 have an internal divide-by-two flip-flop driven by the oscillator for a 50% maximum duty cycle. Therefore, their oscillators must be set to run at twice the desired power supply switching frequency. The UC3842 and UC3843 oscillator runs AT the switching frequency. Each oscillator of the UC3842/3/4/5 family can be used to a maximum of 500 kHz.

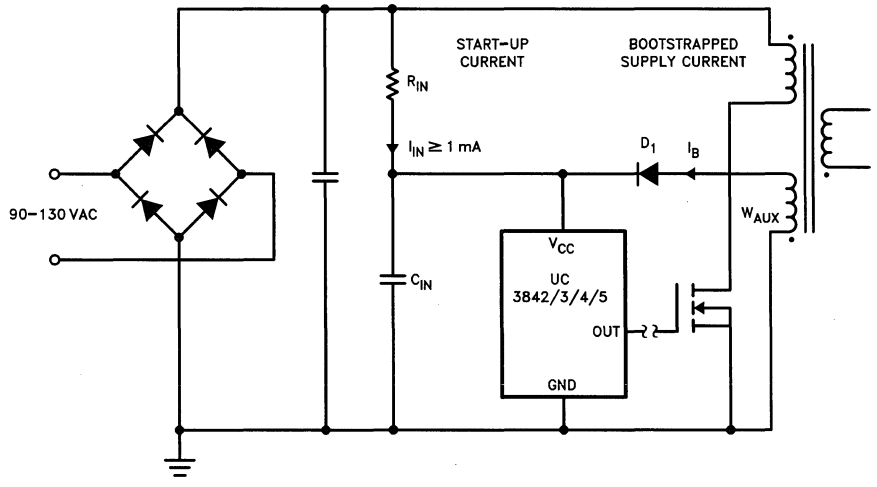


Figure 7. Providing Power to the UC3842/3/4/5

MAXIMUM DUTY CYCLE

The UC3842 and UC3843 have a maximum duty cycle of approximately 100%, whereas the UC3844 and UC3845 are clamped to 50% maximum by an internal toggle flip flop. This duty cycle clamp is advantageous in most flyback and forward converters. For optimum IC performance the deadtime should not exceed 15% of the oscillator clock period.

During the discharge, or "dead" time, the internal clock signal blanks the output to the low state. This limits the maximum duty cycle D_{MAX} to:

$D_{MAX} = 1 - (t_{DEAD} / t_{PERIOD})$ UC3842/3

$D_{MAX} = 1 - (t_{DEAD} / 2 \times t_{PERIOD})$ UC3844/5

where $T_{PERIOD} = 1 / F$ oscillator

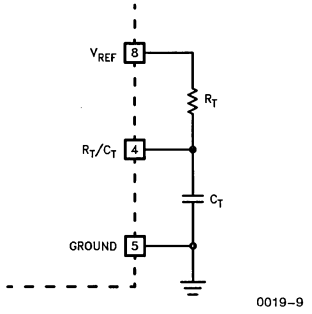


Figure 8

Deadtime vs C_T (R_T > 5k)

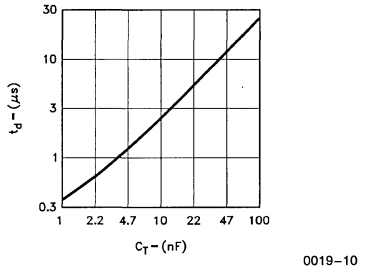


Figure 9

Timing Resistance vs Frequency

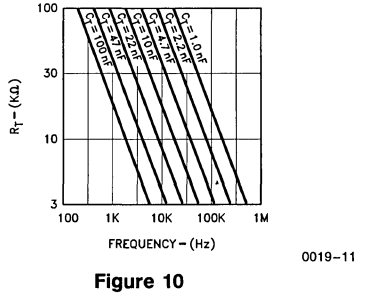


Figure 10

CURRENT SENSING AND LIMITING

The UC3842 current sense input is configured as shown in Figure 12. Current-to-voltage conversion is done externally with ground-referenced resistor R_S. Under normal operation the peak voltage across R_S is controlled by the E/A according to the following relation:

$$I_P = \frac{V_C - 1.4V}{3\,R_S}$$

where V_C = control voltage = E/A output voltage.

R_S can be connected to the power circuit directly or through a current transformer, as **Figure 11** illustrates. While a direct connection is simpler, a transformer can reduce power dissipation in R_S, reduce errors caused by the base current, and provide level shifting to eliminate the restraint of ground-referenced sensing. The relation between V_C and peak current in the power stage is given by:

$$i_{(pk)} = N\left(\frac{V_{RS(pk)}}{R_S}\right) = \frac{N}{3\,R_S}\left(V_C - 1.4V\right)$$

where: N = current sense transformer turns ratio
= 1 when transformer not used.

For purposes of small-signal analysis, the control-to-sensed-current gain is:

$$\frac{i_{(pk)}}{V_C} = \frac{N}{3\,R_S}$$

When sensing current in series with the power transistor, as shown in Figure 11, the current waveform will often have a large spike at its leading edge. This is due to rectifier recovery and/or inter-winding capacitance in the power transformer. If unattenuated, this transient can prematurely terminate the output pulse. As shown, a simple RC filter is usually adequate to suppress this spike. The RC time constant should be approximately equal to the current spike duration (usually a few hundred nanoseconds).

The inverting input to the UC3842 current-sense comparator is internally clamped to 1V (Figure 12). Current limiting occurs if the voltage at pin 3 reaches this threshold value, i.e., the current limit is defined by:

$$i_{max} = \frac{N \times 1V}{R_S}$$

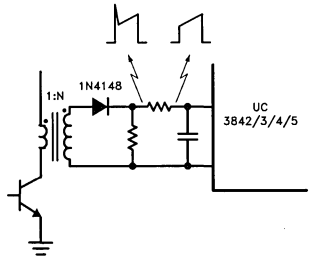


Figure 11. Transformer-Coupled Current Sensing

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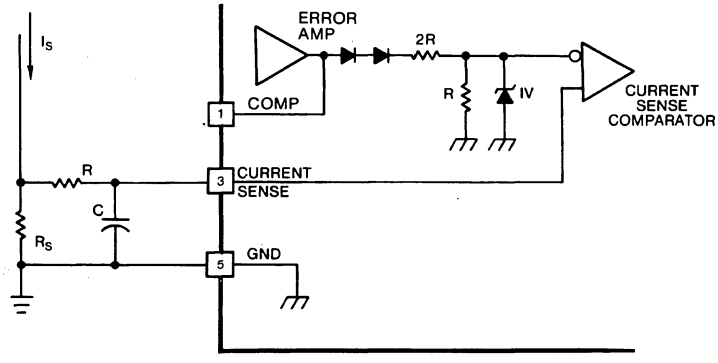

Figure 12. Current Sensing

ERROR AMPLIFIER

The error amplifier (E/A) configuration is shown in Figure 13. The non-inverting input is not brought out to a pin, but is internally biased to 2.5V ± 2%. The E/A output is available at pin 1 for external compensation, allowing the user to control the converter's closed-loop frequency response.

Figure 14 shows an E/A compensation circuit suitable for stabilizing any current-mode controlled topology except for flyback and boost converters operating with inductor current. The feedback components add a pole to the loop transfer function at $f_P = 1/2\pi R_F C_F$. R_F and C_F are chosen so that this pole cancels the zero of the output filter capacitor ESR in the power circuit. R_I and R_F fix the low-frequency gain. They are chosen to provide as much gain as possible while still allowing the pole formed by the output filter capacitor and load to roll off the loop gain to unity (0 dB) at $f \approx f_{SWITCHING}/4$. This technique insures converter stability while providing good dynamic response.

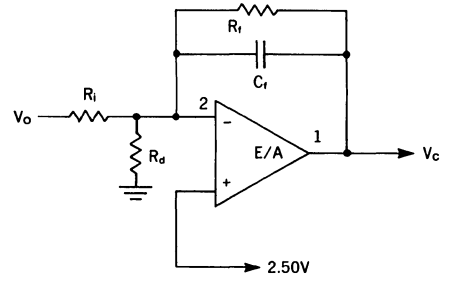

Figure 14. Compensation

The E/A output will source 0.5 mA amd sink 2 mA. A lower limit for R_F is given by:

$$R_{F(MIN)} \approx \frac{V_{EA\ OUT\ (MAX)} - 2.5V}{0.5\ mA} = \frac{6V - 2.5V}{0.5\ mA} = 7\ k\Omega.$$

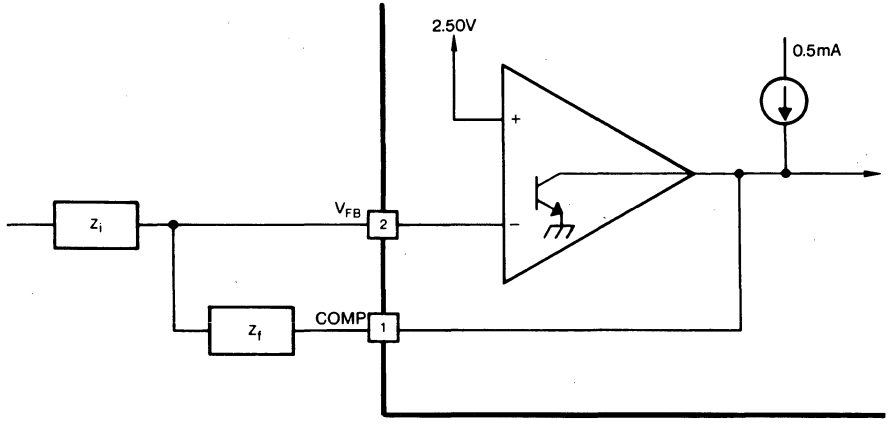

Figure 13. E/A Configuration

E/A input bias curret (2 μA max) flows through R_I, resulting in a DC error in output voltage (V_O) given by:

$\Delta V_{O(MAX)} = (2\ \mu A)\ R_I$,

It is therefore desirable to keep the value of R_I, as low as possible.

Figure 15 shows the open-loop frequency response of the UC3842 E/A. The gain represents an upper limit on the gain of the compensated E/A. Phase lag increases rapidly as frequency exceeds 1 MHz due to second-order poles at ~10 MHz and above.

Continuous-inductor-current boost and flyback converters each have a right-half-plane zero in their transfer function. An additional compensation pole is needed to roll off loop gain at a frequency less than that of the RHP zero. R_P and C_P in the circuit of Figure 16 provide this pole.

TOTEM-POLE OUTPUT

The UC3842 PWM has a single totem-pole output which can be operated to ±1 amp peak for driving MOSFET gates, and a ±200 mA average current for bipolar power transistors. Cross conduction between the output transistors is minimal, the average added power with V_{IN} = 30V is only 80 mW at 200 kHz.

Limiting the peak current through the IC is accomplished by placing a resistor between the totem-pole output and the gate of the MOSFET. The value is determined by dividing the totem-pole collector voltage V_C by the peak current rating of the IC's totem-pole. Without this resistor, the peak current is limited only by the dV/dT rate of the totem-pole switching and the FET gate capacitance.

The use of a Schottky diode from the PWM output to ground will prevent the output voltage from going excessively below ground, causing instabilities within the IC. To be effective, the diode selected should have a forward drop of less than 0.3V at 200 mA. Most 1- to 3-amp Schottky diodes exhibit these traits above room temperature. Placing the diode as physically close to the PWM as possible will enhance circuit performance. Implementation of the complete drive scheme is shown in the following diagrams. Transformer driven circuits also require the use of the Schottky diodes to prevent a similar set of circum-

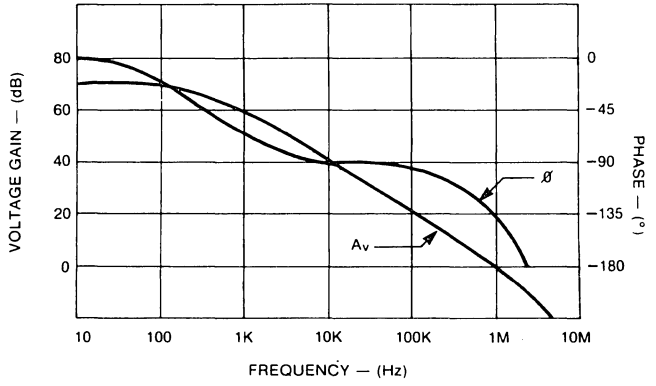

Figure 15. Error Amplifier Open-Loop Frequency Response

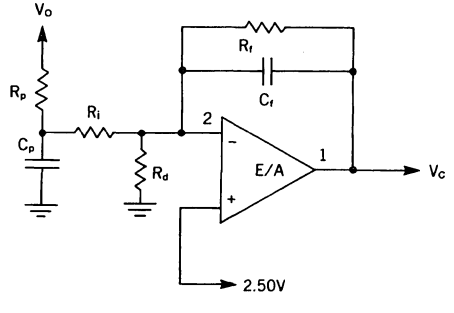

Figure 16. E/A Compensation Circuit for Continuous Boost and Flyback Topologies

9

stances from occurring on the PWM output. The ringing below ground is greatly enhanced by the transformer leakage inductance and parasitic capacitance, in addition to the magnetizing inductance and FET gate capacitance. Circuit implementation is similar to the previous example.

Figures 18, 19 and 20 show suggested circuits for driving MOSFETs and bipolar transistors with the UC3842 output. The simple circuit of Figure 18 can be used when the control IC is not electrically isolated from the MOSFET turn-on and turn-off to ±1 amp. It also provides damping for a parasitic tank circuit formed by the FET input capacitance and series wiring inductance. Schottky diode D1 prevents the output of the IC from going far below ground during turn-off.

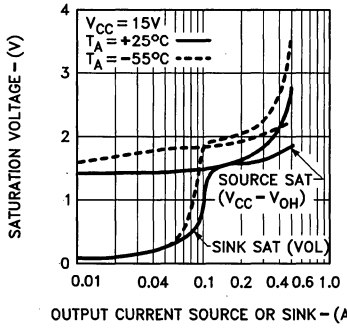

Figure 17. Output Saturation Characteristics

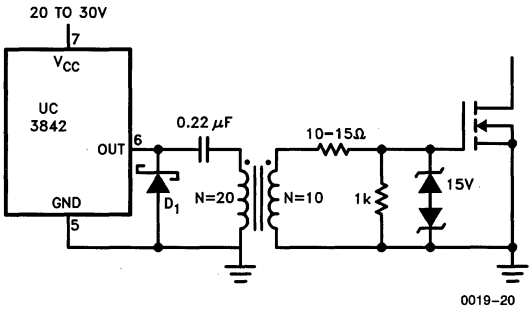

Figure 19. Isloated MOSFET Drive

Figure 19 shows an isolated MOSFET drive circuit which is appropriate when the drive signal must be level shifted or transmitted across an isolation boundary. Bipolar transistors can be driven efficiently with the circuit of Figure 20. Resistors R_1 and R_2 fix the on-state base current while capacitor C_1 provides a negative base current pulse to remove stored charge at turn-off.

Since the UC3842 series has only a single output, an interface circuit is needed to control push-pull half or full bridge topologies. The UC3706 dual output driver with internal toggle flip-flop performs this function. A circuit example at the end of this paper illustrates a typical application for these two ICs. Increased drive capability for driving numerous FETs in parallel, or other loads can be accomplished using one of the UC3705/6/7 driver ICs.

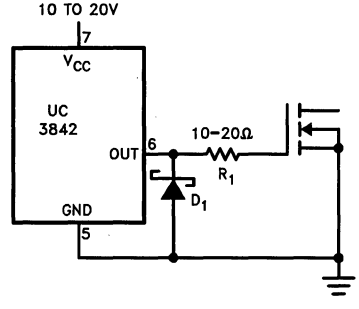

Figure 18. Direct MOSFET Drive

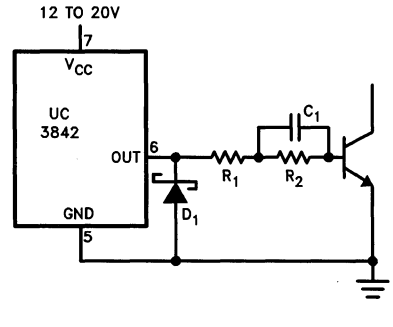

Figure 20. Bipolar Drive with Negative Turn-Off Bias

SLOPE COMPENSATION

Current mode control regulates the PEAK inductor current via the "inner" or current control loop. In a continuous mode (buck) converter, however, the output current is the AVERAGE inductor current, composed of both an AC and DC component.

AVERAGE CURRENT

At high values of V_{IN}, the AC current in both the primary and the secondary is at its maximum. This is represented graphically by duty cycle D_1, the corresponding average current I_1, and the ripple current d(I1). As V_{IN} decreases to its minimum at duty cycle, the ripple current also is at its minimum amplitude. This occurs at duty cycle D_2 of average current I_2 and ripple current d(I2). Regulating the peak primary current (current mode control) will produce different AVERAGE output currents I_1, and I_2 for duty cycles D_1 and D_2. The average current INCREASES with duty cycle when the peak current is compared to a fixed error voltage.

CONSTANT OUTPUT CURRENT

To maintain a constant AVERAGE current, independent of duty cycle, a compensating ramp is required. Lowering the error voltage precisely as a function of T_{ON} will terminate the pulse width sooner. This narrows the duty cycle creating a CONSTANT output current independent of T_{ON}, or V_{IN}. This ramp simply compensates for the peak to average current differences as a function of duty cycle. Output currents I_1 and I_2 are now identical for duty cycles D_1 and D_2.

DETERMINING THE RAMP SLOPE

Mathematically, the slope of this compensating ramp must be equal to one-half (50%) the downslope of the output inductor as seen from the control side of the circuit. This is proven in detail in "Modelling, Analysis and Compensating of the Current Mode Controller," (Unitrode publication U-97 and its references). Empirically, slightly higher values of slope compensation (75%) can be used where the AC component is small in comparison to the DC pedestal, typical of a continuous converter.

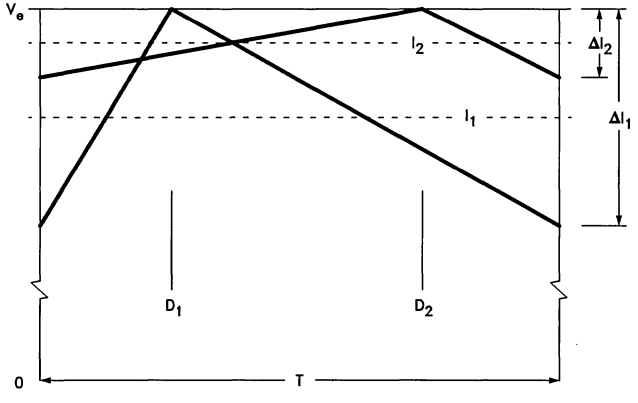

Figure 21. Average Current Error

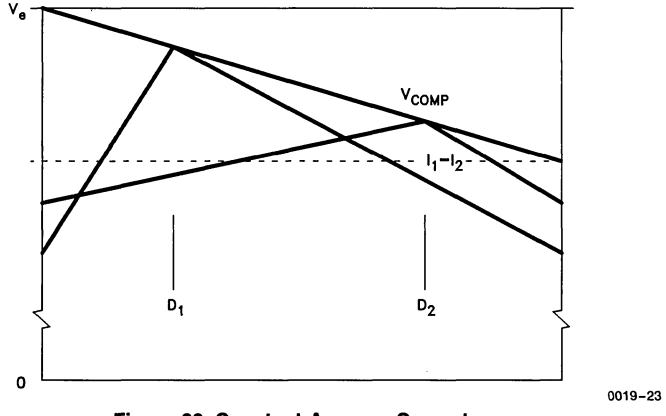

Figure 22. Constant Average Current

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CIRCUIT IMPLEMENTATION

In a current mode control PWM IC, the error voltage is generated at the output of the error amplifier and compared to the primary current at the PWM comparator. At this node, subtracting the compensating ramp from the error voltage, or adding it to the primary current sense input will have the same effect: to decrease the pulse width as a function of duty cycle (time). It is more convenient to add the slope compensating ramp to the current input. A portion of the oscillator waveform available at the timing capacitor (C_T) will be resistively summed with the primary current. This is entered to the PWM comparator at the current sense input.

PARAMETERS REQUIRED FOR SLOPE COMPENSATION CALCULATIONS

Slope compensation can be calculated after specific parameters of the circuit are defined and calculated.

SECTION	PARAMETER
Control	T on (Max) Oscillator ΔV Oscillator (PK-PK Ramp Amplitude) I Sense Threshold (Max)
Output	V Secondary (Min) L Output I AC Secondary (Secondary Ripple Current)
General	R Sense (Current Sensing Resistor) M (Amount of Slope Compensation) N Turns Ratio (N_P/N_S).

Once obtained, the calculations for slope compensation are straightforward, using the following equations and diagrams.

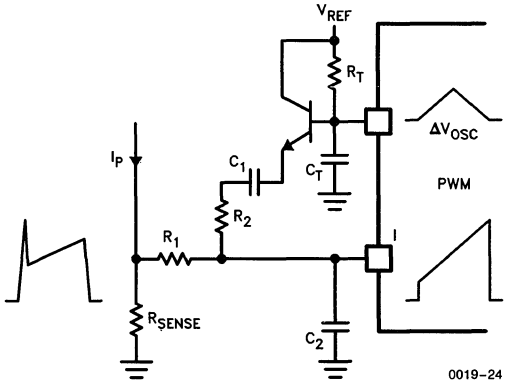


Figure 23. General Circuit

Resistors R_1 and R_2 form a voltage divider from the oscillator output to the current sense input, superimposing the slope compensation on the primary current waveform. Capacitor C_1 is an AC coupling capacitor, and allows the AC voltage swing of the oscillator to be used without adding offset circuitry. Capacitor C_2 forms an R-C filter with R_1 to suppress the leading edge glitch of the primary current wave. The ratio of resistor R_2 to R_1 will determine the exact amount of slope compensation added.

For purposes of determining the resistor values, capacitors C_T (timing), C_1 (coupling), and C2 (filtering) can be removed from the circuit schematic. The oscillator voltage (V_{OSC}) is the peak-to-peak amplitude of the sawtooth waveform. The simplified model is represented schematically in the following circuit.

These calculations can be applied to all current mode converters using a similar slope compensating scheme.

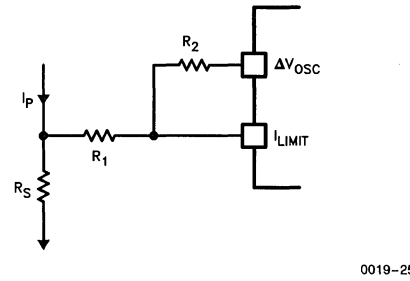


Figure 24. Simplified Circuit

Step 1. Calculate the Inductor Downslope
$S(L) = di/dt = V_{SEC}/L_{SEC}$ (Amps/Second)

Step 2. Calculate the Reflected Downslope to the Primary
$S(L)' = S(L)/N$ (Amps/Second)

Step 3. Calculate Equivalent Downslope Ramp
$V\,S(L)' = S(L)' \times R\ sense$ (Volts/Second)

Step 4. Calculate the Oscillator Charge Slope
$V\,S_{(OSC)} = d(V_{OSC})/T_{on}$ (Volts/Second)

Step 5. Generate the Ramp Equations Using superposition, the circuit can be illustrated as:

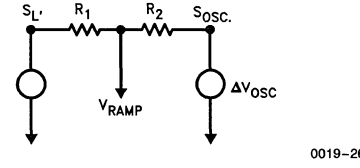


Figure 25. Superposition

$$V_{(RAMP)} = \frac{V\,S(L)' \times R_2}{R_1 + R_2} + \frac{V\,S_{(OSC)} \times R_1}{R_1 + R_2} \text{ simplifying,}$$

$$V_{(RAMP)} = V\,S(L)'' + V\,S_{(COMP)} \quad \text{where}$$

$$V\,S_{(COMP)} = \frac{V\,S_{(OSC)} \times R_1}{R_1 + R_2}, \text{ and } V\,S(L)''$$

$$= \frac{V\,S(L)' \times R_2}{R_1 + R_2}$$

Step 6. Calculate Slope Compensation
$V\,S_{(COMP)} = M \times S(L)''$ where M is the amount of inductor downslope to be introduced.

$$\text{Equating } \frac{V\,S_{(OSC)} \times R_1}{R_1 + R_2} = \frac{M \times V\,S(L)' \times R_2}{R_1 + R_2},$$

solving for R_2

$$R_2 = R_1 \times \frac{V\,S_{(OSC)}}{V\,S(L)' \times M}$$

Equating R_1 to 1 kΩ simplifies the above calculation and selection of capacitor C_2 for filtering the leading edge glitch. Using the closest standard value to the calculated value of R_2 will minimally effect the exact amount of downslope introduced. It is important that R_2 be high enough in resistance not to load down the I.C. oscillator, thus causing a frequency shift due to the slope compensation ramp to R_2. Greater flexibility can be accommodated by adding an emitter follower buffer between C_T and C_1, R_2–R_1 divider shown in Figure 23.

PWM LATCH

This flip-flop, shown in Figure 4, ensures that only a single pulse appears at the UC3842/3/4/5 output in any one oscillator period. Excessive power transistor dissipation and potential saturation of magnetic elements are thereby averted.

SHUTDOWN TECHNIQUE

Shutdown of the UC3842 can be accomplished by two methods; either raise pin 3 above 1V, Figure 26A, or pull pin 1 below 1V as shown in Figure 26B. Either method causes the output of the PWM comparator to be high (refer to block diagram, Figure 4). The PWM latch is reset dominant so that the output will remain low until the first clock pulse following removal of the shutdown signal at pin 1 or pin 3. As shown in Figure 27, an externally latched shutdown can be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower undervoltage lockout threshold (10V). At this point all internal bias is removed, allowing the SCR to reset.

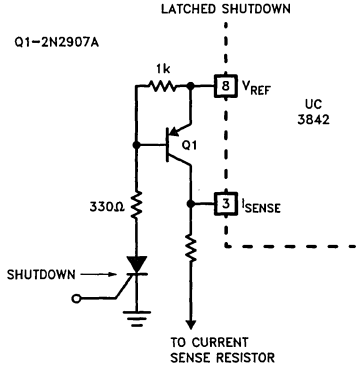
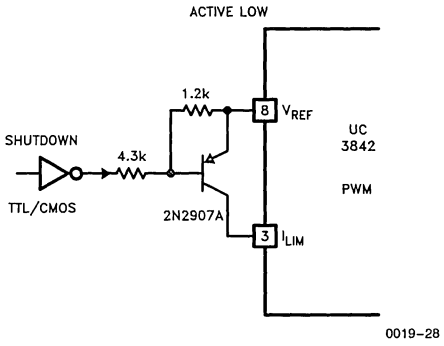
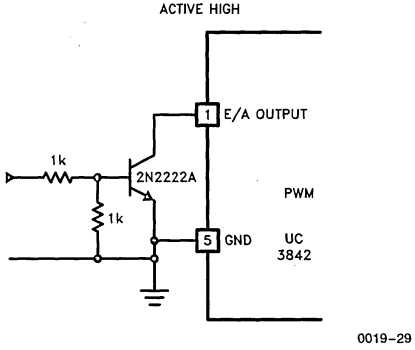


Figure 27



A. NONLATCHING

Figure 26A. PWM Shutdown Circuit



B. NONLATCHING

Figure 26B

SOFT START

Upon power-up, it is sometimes desirable to gradually widen the output pulse width beginning at zero pulse width. Since the UC3842 IC does not internally include a soft start function, it must be added externally. Using three components, an R/C network provides the time constant to control the rate of rise of the error amplifier output. A transistor is used to sink the maximum error amp output current, and isolate the R/C network during normal PWM activities.

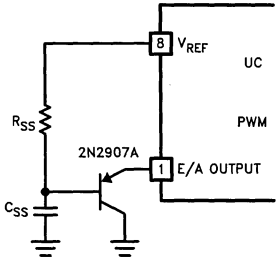


Figure 29. Soft Start Circuit

NOISE

As mentioned earlier, noise on the current sense or control signals can cause significant pulse-width jitter, particularly with continuous-inductor-current designs. While slope compensation helps alleviate this problem, a better solution is to minimize the amount of noise. In general, noise immunity improves as impedances decrease at critical points in a circuit.

One such point for a switching supply is the ground line. Small wiring inductances between various ground points on a PC board can support common-mode noise with sufficient amplitude to interfere with correct operation of the modulating IC. A copper ground plane and separate return lines for high-current paths greatly reduce common-mode noise. Note that the UC3842 has a single ground pin. High sink currents in the output therefore cannot be returned separately.

Ceramic monolythic bypass capacitors (0.1 μF) from V_{CC} and V_{REF} to ground will provide low-impedance paths for high frequency transients at those points. The input to the error amplifier, however, is a high-impedance point which cannot be bypassed without affecting the dynamic response of the power supply. Therefore, care should be taken to lay out the board in such a way that the feedback path is far removed from noise generating components such as the power transistor(s).

Figure 30 illustrates another common noise-induced problem. When the power transistor turns off, a noise spike is coupled to the oscillator R_T/C_T terminal. At high duty cycles the voltage at R_T/C_T is approaching its threshold level ($\sim$2.7V, established by the internal oscillator circuit) when this spike occurs. A spike of sufficient amplitude will prematurely trip the oscillator as shown by the dashed lines. In order to minimize the noise spike, choose C_T as large as possible, remembering that deadtime increases with C_T. It is recommended that C_T never be less than $\sim$1000 pF. Often the noise which causes this problem is caused by the output (pin 6) being pulled below ground at turn-off by external parasitics. This is particularly true when driving MOSFETs. A Schottky diode clamp from ground to pin 6 will prevent such output noise from feeding to the oscillator. If these measures fail to correct the probelm, the oscillator frequency can always be stabilized with an external clock. Using the circuit of Figure 43 results in an R_T/C_T waveform like that of Figure 30B. Here the oscillator is much more immune to noise because the ramp voltage never closely approaches the internal threshold.

SYNCHRONIZATION

The simplest method to force synchronization utilizes the timing capacitor (C_T) in near standard configuration. Rather than bring C_T to ground directly, a small resistor is placed in series with C_T to ground. This resistor serves as the input for the sync pulse which raises the C_T voltage above the oscillator's internal upper threshold. The PWM is allowed to run at the frequency set by R_T and C_T until the sync pulse appears. This scheme offers several advantages including having the local ramp available for slope compensation. The UC3842/3/4/5 oscillator

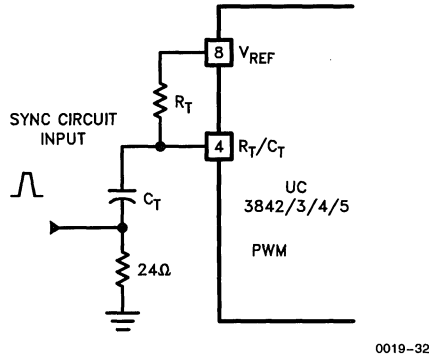


Figure 31. Sync Circuit Implementation

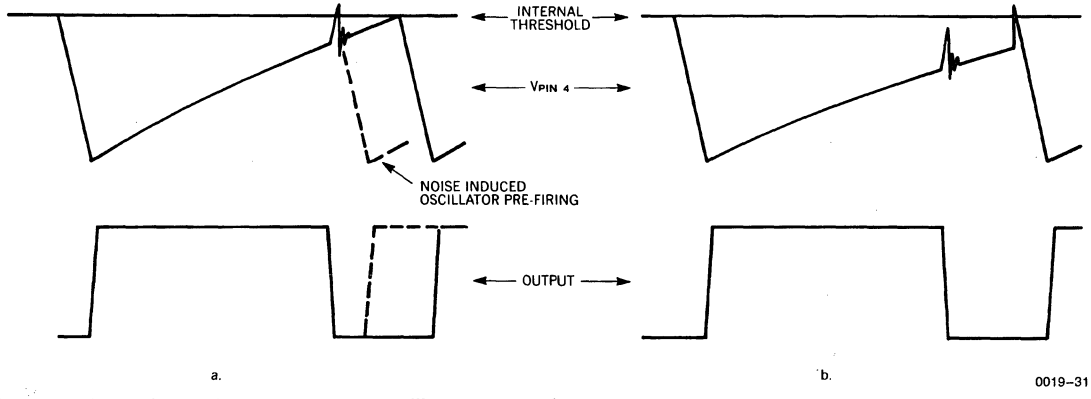


Figure 30. (a.) Noise on Pin 4 can cause oscillator to pre-trigger.
(b.) With external sync., noise does not approach threshold level.

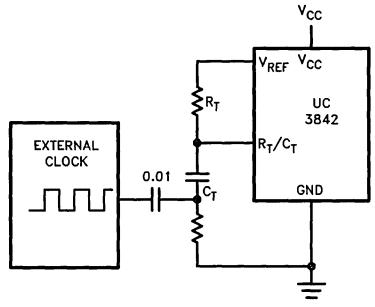
must be set to a lower frequency than the sync pulse stream, typically 20 percent with a 0.5V pulse applied across the resistor. Further information on synchronization can be found in "Practical Considerations in Current Mode Power Supplies" listed in the reference appendix.

The UC3842 can also be synchronized to an external clock source through the R_T/C_T terminal (Pin 4) as shown in Figure 32.

In normal operation, the timing capacitor C_T is charged between two thresholds, the upper and lower comparator limits. As C_T begins its charge cycle, the output of the PWM is initiated and turns on. The timing capacitor continues to charge until it reaches the upper threshold of the internal comparator. Once intersected, the discharge circuitry activates and discharges C_T until the lower threshold is reached. During this discharge time the PWM output is disabled, thus insuring a "dead" or off time for the output.

A digital representation of the oscillator charge/discharge status can be utilized as an input to the R_T/C_T terminal. In instances like this, where no synchronization port is easily available, the timing circuitry can be driven from a digital logic input rather than the conventional analog mode. The primary considerations of on-time, dead-time, duty cycle and frequency can be encompassed in the digital pulse train input.

A LOW logic level input determines the PWM maximum ON time. Conversely, a HIGH input governs the OFF, or dead time. Critical constraints of frequency, duty cycle or dead time can be acurately controlled by anything from a 555 timer to an elaborate microprocessor controlled software routine.



0019-34

$D_{Max} = t_L (t_H + t_L)$
$t_H = 0.693 (R_A + R_B) C$
$t_L = 0.693 R_B C$

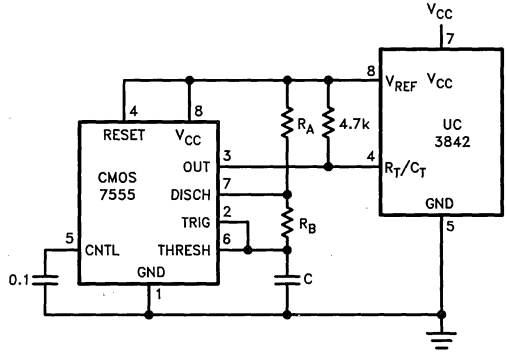


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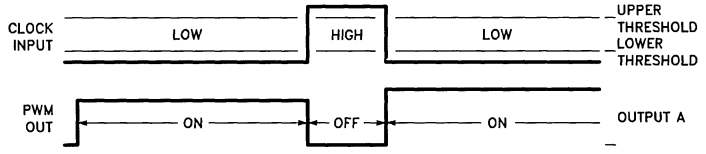
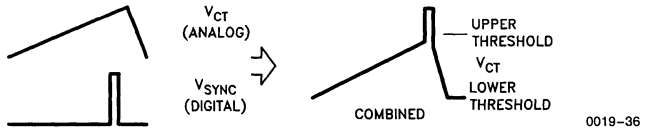
Figure 32

Synchronization to an External Clock



0019-35

Figure 33



0019-36

Figure 34

SYNC PULSE GENERATOR

The UC3842/3/4/5 oscillator can be used to generate sync pulses with a minimum of external components. This simple circuit shown in Figure 35 triggers on the falling edge of the C_T waveform, and generates the sync pulse required for the previously mentioned synchronization scheme. Triggered by the master's deadtime, this circuit is useable to several hundred kilohertz with a minimum of delays between the master and slave(s). The photos shown in Figures 36 and 37 depict the circuit waveforms of interest.

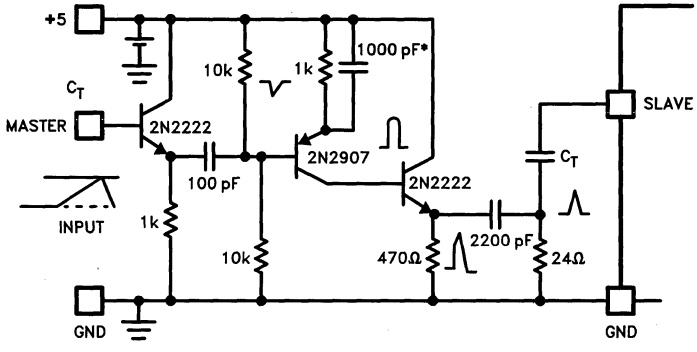
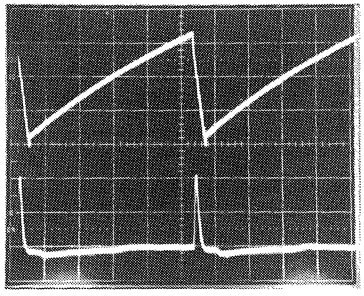


Figure 35. Sync Pulse Generator Circuit



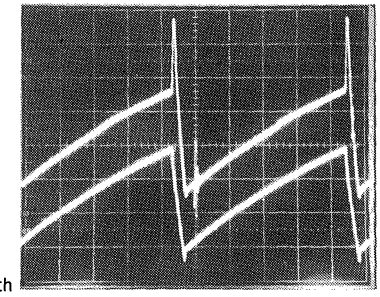
Top Trace:
Circuit Input

Bottom Trace:
Circuit Output
Across 24 Ohms

Vertical: 0.5V/CM Both
Horizontal: 0.5μS/CM

001938 0019-38

Figure 36. Operating Waveforms at 500 kHz



Top Trace:
Slave C_T

Bottom Trace:
Master C_T

Vertical: 0.5V/CM Both
Horizontal: 0.5μS/CM

001939 0019-39

Figure 37. Master/Slave Sync Waveforms at C_T

APPLICATION APPENDIX

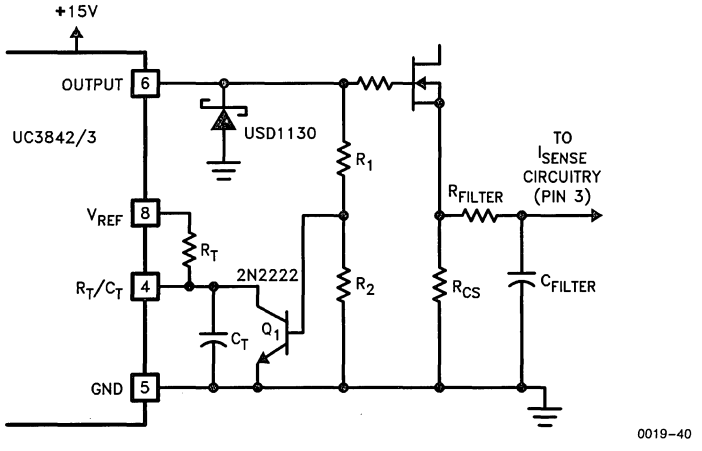
FIXED "OFF-TIME" APPLICATIONS

Obtaining a fixed "off-time" and a variable "on-time" can easily be accomplished with most current-mode PWM IC's. In these applications, the R_T/C_T timing components are used to generate the "off-time" rather than the traditional "on-time". Implementation is shown schematically in Figure 38 along with the pertinant waveforms.

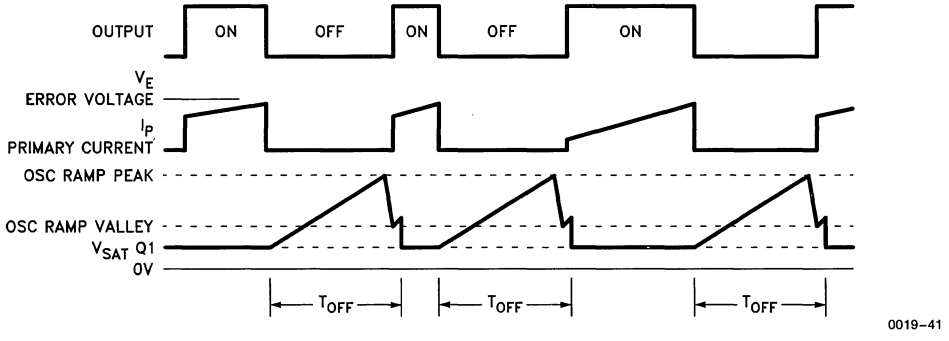
At the beginning of an oscillator cycle, C_T begins charging and the PWM output is turned on. Transistor Q_1 is driven from the output and also turns on with the PWM output, thus discharging C_T and pulling this node to ground. As this occurs, the oscillator is "frozen" with the PWM output fully ON. On-time can be controlled in the conventional manner by comparing the error amplifier output voltage with the current sense input voltage. This results in a current controlled "on-time" and fixed "off-time" mode of operation. Other variations are possible with different inputs to the current sense input.

When the PWM output goes low (off), transistor Q_1 also turns off and C_T begins charging to its upper threshold. The off-time generates by this approach will be longer for a given R_T/C_T combination than first anticipated using the oscillator "charging" equations or curves. Timing capacitor C_T now begins charging from V_{SAT} of Q_1 (approx. 0V) instead of the internal oscillator lower threshold of approximately 1V.

Fixed "Off-Time", Current Controlled "On-Time"



Schematic



Waveforms

Figure 38

CURRENT MODE ICs USED IN VOLTAGE MODE

In duty cycle control (voltage mode), pulse width modulation is attained by comparing the error amplifier output to an artificial ramp. The oscillator timing capacitor C_T is used to generate a sawtooth waveform on both current or voltage mode ICs. To utilize a current mode chip in the voltage mode, this sawtooth waveform will be input to the current sense input for comparison to the error voltage at the PWM comparator. This sawtooth will be used to determine pulse width instead of the actual primary current in this configuration.

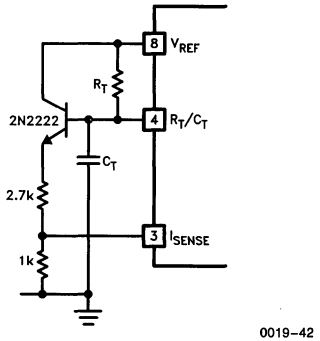


Figure 39. Current Mode PWM Used as a Voltage Mode PWM

Compensation of the loop is similar to that of voltage mode. The UC3842/3/4/5 current mode PWMs use a low output resistance (voltage) amplifier and are compensated accordingly. For further reference on topologies and compensation, consult "Closing the Feedback Loop" listed in this appendix.

FULL DUTY CYCLE (100%) APPLICATIONS

Full, or 100% duty cycle is a condition that is highly undesirable in a switch-mode power supply. Therefore, most PWM IC designs have gone to great extent to prevent 100% duty cycle from occurring. There are simple ways to over-ride these safeguards, however. One method, presented below, "freezes" the oscillator and holds the PWM output in the ON, or high state when the circuit is activated. Feedback from the output is required to guarantee that the oscillator is stopped while the output is high. Without feedback, the oscillator can be locked with the output in either state.

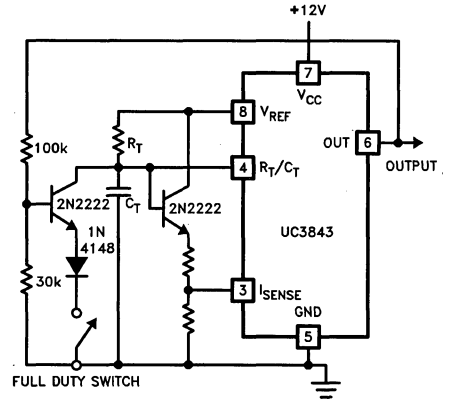


Figure 40. Full Duty Cycle Implementation

CHARGE PUMP CIRCUITS
LOW POWER DC/DC CONVERSION

Step Up

$V_O \approx 2 \times V_{IN}$

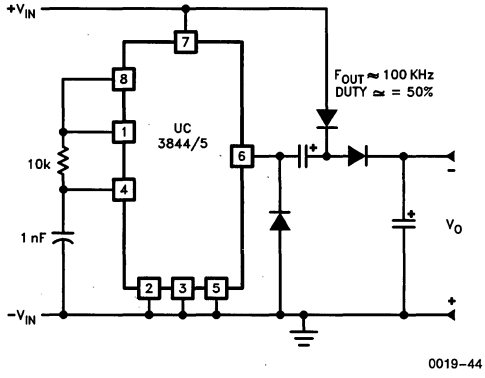


Figure 41

Inverting

$V_O \approx -V_{IN}$

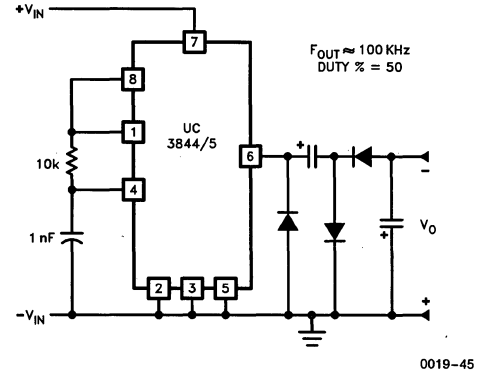


Figure 42

CIRCUIT EXAMPLES

Also consult UNITRODE application note.

1. Off-Line Flyback

Figure 43 shows a 25W multiple-output off-line flyback regulator controlled with the UC3844. This regulator is low in cost because it uses only two magnetic elements, a primary-side voltage sensing technique, and an inexpensive control circuit. Specifications are listed below.

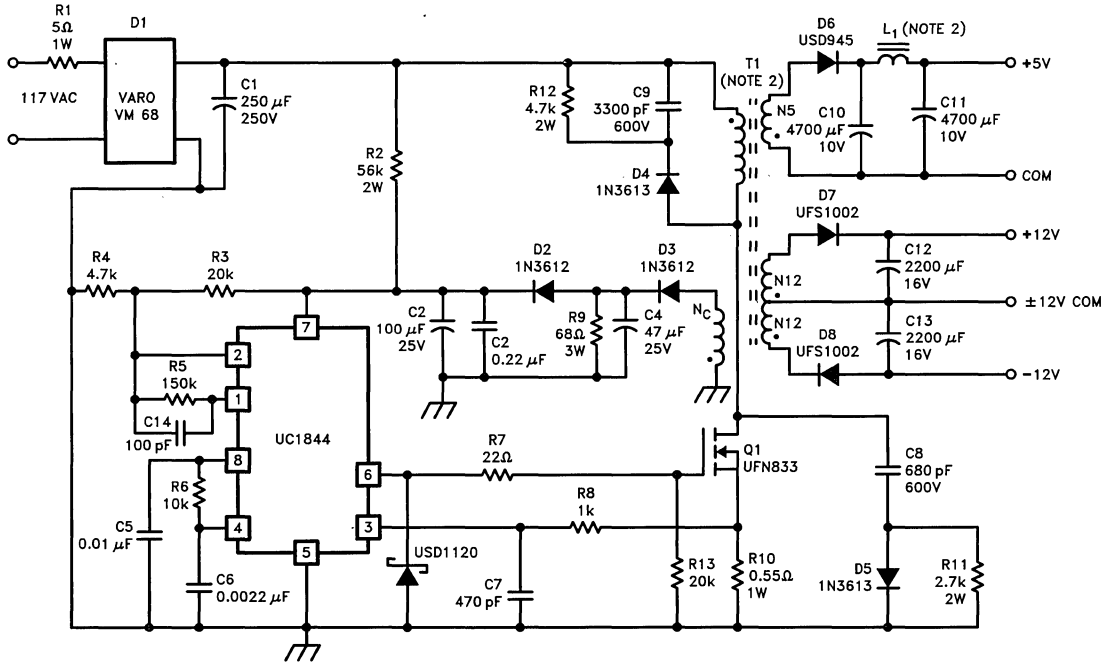


Figure 43

Power Supply Specifications

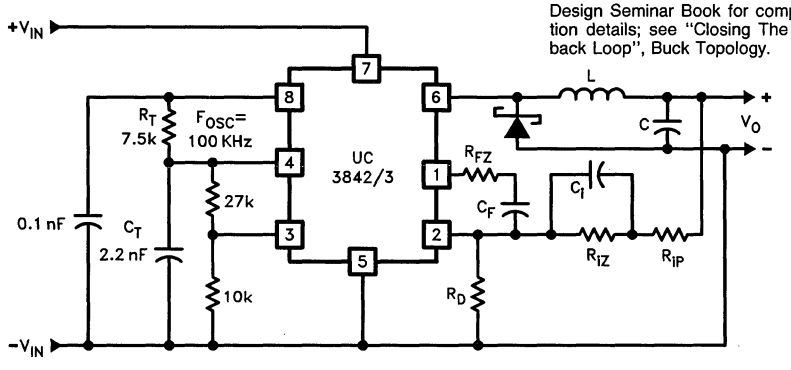
1. Input Voltage: 95 VAC to 130 VAC (50 Hz/60 Hz)
2. Line Isolation: 3750V
3. Switching Frequency: 40 kHz
4. Efficiency @ Full Load: 70%
5. Output Voltage:
   - A. +5V, ±5%: 1A to 4A load
     Ripple voltage: 50 mV P-P Max.
   - B. +12V, ±3% 0.1A to 0.3A load
     Ripple voltage: 100 mV P-P Max.
   - C. −12V ±3%, 0.1A to 0.3A load
     Ripple voltage: 100 mV P-P Max.

9

Low Power Buck Regulator—Voltage Mode

The basic buck regulator is described in the UNITRODE Applications Handbook.

*Consult UNITRODE Power Supply Design Seminar Book for compensation details; see "Closing The Feedback Loop", Buck Topology.



0019-47

Figure 44

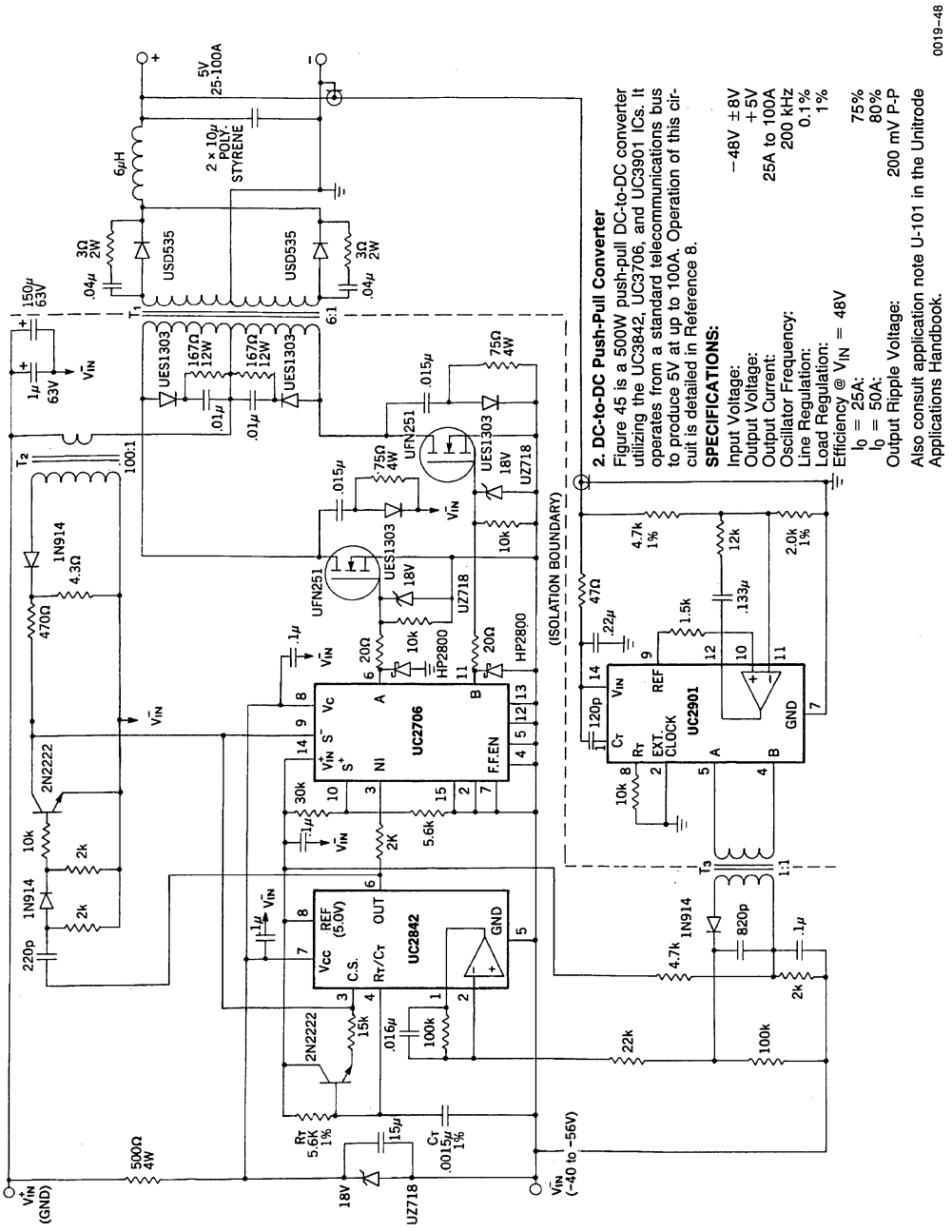


Figure 45. 500W Push-Pull DC-to-DC Converter

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200KHz CURRENT-MODE CONVERTER PROVIDES 500W

This Application Note describes a push-pull converter which develops up to 100A at 5V from a standard 48V input. It provides equations used to specify all critical components, so that a designer can adapt the circuit to meet a different set of requirements. Specifications, performance data, and waveform photographs are included. The schematic appears in Figure 1.

SPECIFICATIONS

Input Voltage ..... -48V ± 8V
Output Voltage ..... +5V
Output Current ..... 25A to 100A
Short-Circuit Current 120A
Oscillator Frequency 200KHz
Line Regulation 0.12%
Load Regulation 0.25%
Efficiency 75%
Output Ripple Voltage 300mV
Large-Signal Output Slew Rate 30A/ms

PERFORMANCE DATA

Test Conditions		Performance			
I_O	V_{IN}	V_O	I_{IN}	Efficiency	Ripple
(A)	(V)	(V)	(A)	(%)	(mV p-p)
25	40	5.002	3.9	80	50
25	56	4.996	3.0	75	75
50	40	5.000	7.8	80	100
50	56	4.995	5.8	77	150
75	40	5.000	11.8	79	200
75	56	4.996	8.6	78	220
100	40	4.990	16.7	75	250
100	56	4.990	11.8	76	300

OVERVIEW[1, 2, 3, 4]

This design utilizes a center-tap push-pull topology operating with continuous inductor current and current-mode control. This push-pull configuration optimizes transformer utilization while allowing common-source operation of the power MOSFETs.

Current-mode control was chosen for this application for several reasons. Power transformer flux balancing is achieved without the cost of added sensing circuits. The filter inductor behaves like a current source, which allows a closed-loop frequency response of greater bandwidth than would otherwise be possible for stable operation. More importantly, the error amplifier compensation becomes simpler and better behaved under conditions of large-signal load changes.[4] Finally, current-mode control provides instantaneous (single-cycle) correction for input voltage variations.

The UC2842 pulse width modulator provides all these advantages at an extremely low cost. Since this IC has only a single output, a UC2706 Dual Output Driver is used to perform a single-ended to push-pull conversion. The UC2706 provides the added advantages of rapid (180ns) current limiting and high peak current MOSFET drive needed to operate at high frequencies. Since input-to-output isolation is required, a UC2901 Isolated Feedback Generator is employed to return a feedback signal from the output to the primary-side PWM controller.

Block diagrams of these three ICs appear in Figures 2-4. Waveforms at critical circuit points are shown in Figures 5-8.

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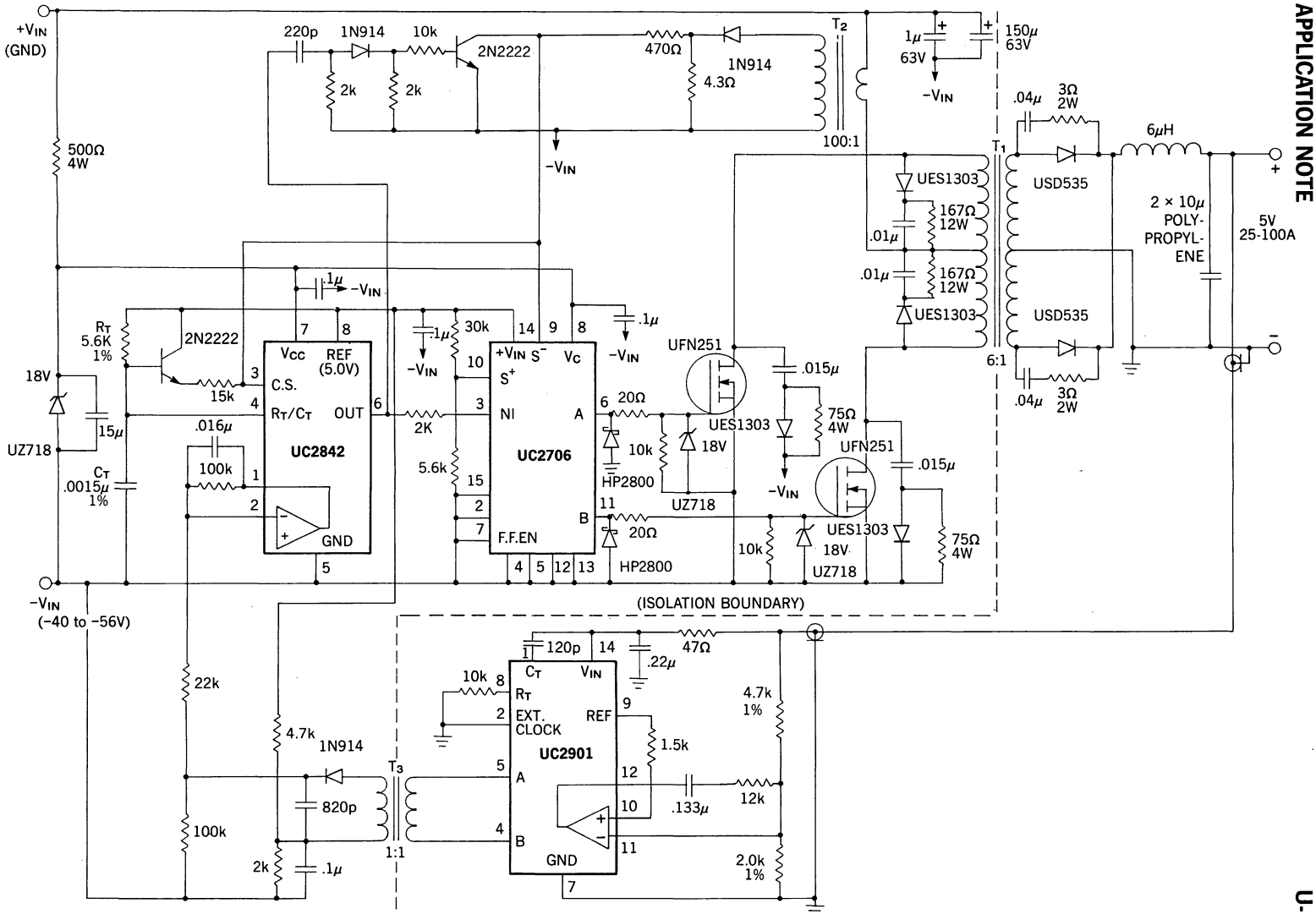

FIGURE 1. 500W PUSH-PULL DC-TO-DC CONVERTER.

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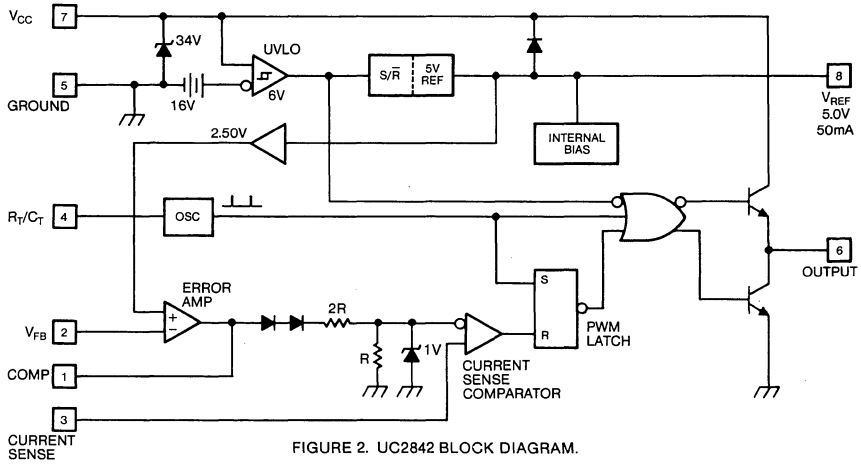

FIGURE 2. UC2842 BLOCK DIAGRAM.

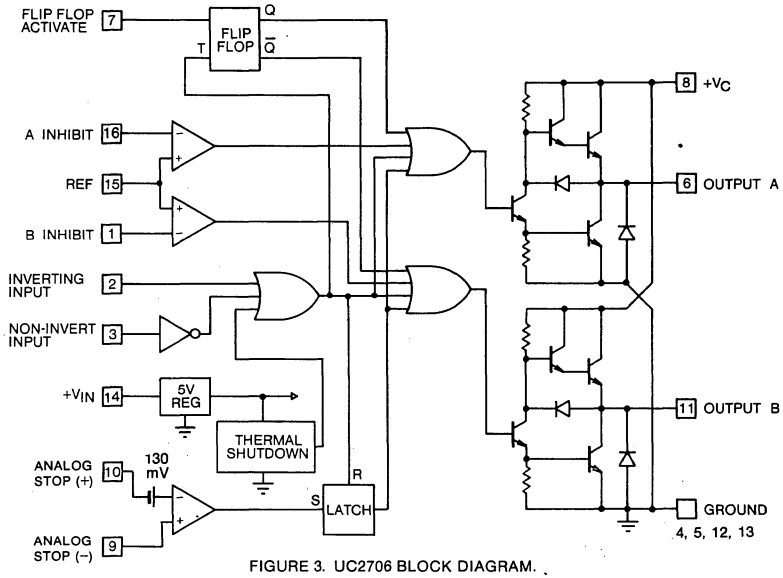

FIGURE 3. UC2706 BLOCK DIAGRAM.

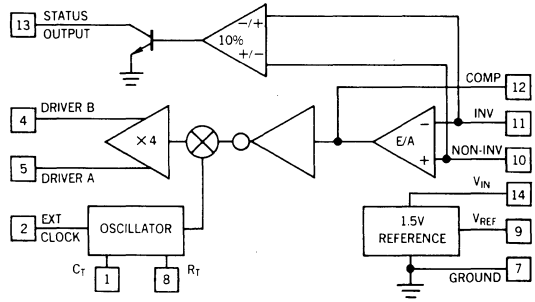

FIGURE 4. UC2901 BLOCK DIAGRAM

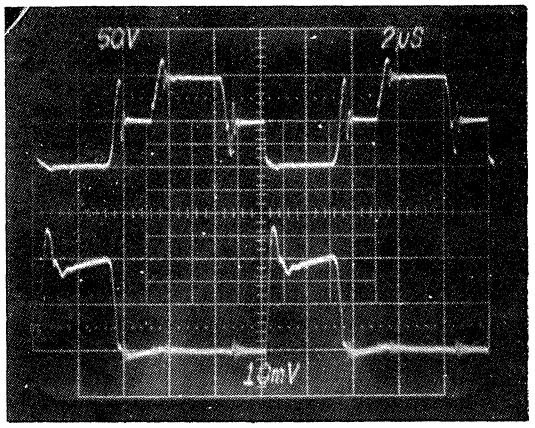

FIGURE 5. TOP: MOSFET V_{DS} @ 50V/div.
BOTTOM: MOSFET I_D @ 5A/div.
2μs/div.

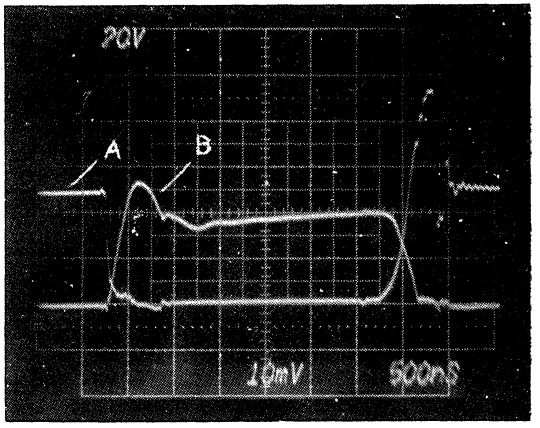

FIGURE 6. A: MOSFET V_{DS} @ 20V/div.
B: MOSFET I_D @ 5A/div.
500ns/div.

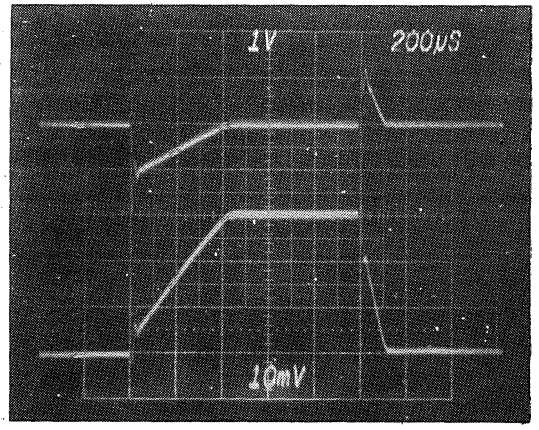

FIGURE 7. LARGE-SIGNAL OUTPUT SLEW RATE.
TOP: OUTPUT VOLTAGE @ 1V/div.
BOTTOM: OUTPUT CURRENT @ 5A/div.
200μs/div.

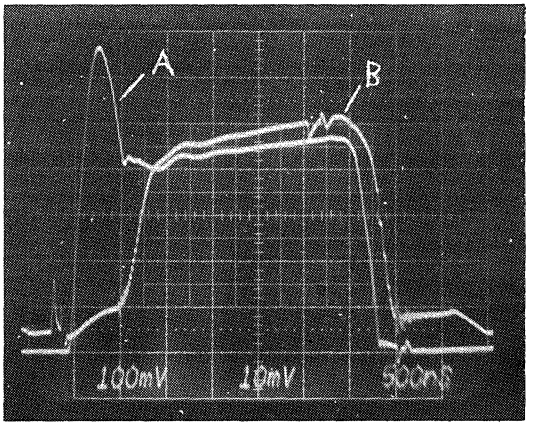

FIGURE 8. A: MOSFET I_D @ 2A/div.
B: CURRENT SENSE (UC2842 — PIN 3) @ 100mV/div.
500ns/div.

9

DESIGN EQUATIONS

Power Transformer[5]

Several design iterations resulted in the choice of a Ferroxcube EC52-3C8 ferrite core for the power transformer. This is the smallest EC core with a wire window area A_w large enough for the required high-current windings.

For this buck-derived converter, duty cycle D is given by:

$$D = \frac{(V_O + V_F)N}{V_{IN} - V_{DS(ON)}}$$

where: V_O, V_F, V_{IN} and $V_{DS(ON)}$ are defined as in Figure 9.

N = primary-to-secondary turns ratio (N_P/N_S).

This equation is used for selecting N to give an optimum range of D as V_{IN} varies from 40V to 56V. D should be as large as possible in order to minimize peak currents, but not so large that circuit delays and losses limit D when V_{IN} = 40V.

For this design, N = 5 was chosen so that:

$$D_{MAX} \approx \frac{(5V + .6V)5}{40V - 1V} = .72$$

$$D_{MIN} \approx \frac{(5V + .6V)5}{56V - 1V} = .51$$

Next, the minimum number of primary turns required to prevent core saturation is determined from the following equation:[5]

$$N_P > \frac{V_{IN(MIN)}\, t_{ON(MAX)}}{\Delta B\, A_e} \cdot 10^8$$

where: ΔB = maximum flux swing (Gauss).
A_e = effective magnetic area (cm^2).

A safe peak-operating flux density for 3C8 ferrite is ~ 2500 Gauss (saturation occurs at ~ 3000 Gauss). Therefore, B = 2 × 2500 = 5000 Gauss for push-pull operation.

$$N_P > \frac{40V \cdot 5\mu s}{5000G \cdot 1.83\ cm^2} \cdot 10^8 = 2.2$$

This design uses N_P = 5, N_S = 1.

Wire size requirements are determined by the worst-case RMS current in each winding. Refer to Figure 9.

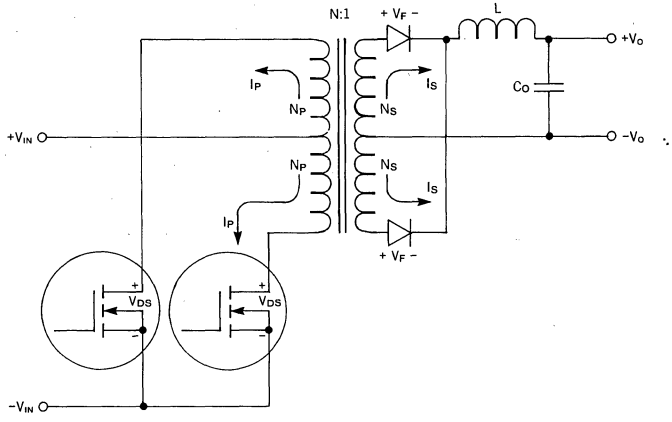

FIGURE 9. BASIC PUSH-PULL POWER CIRCUIT AND FILTER.

Primary:

$$I_{P(AVG)(MAX)} = \frac{\frac{1}{2} P_{IN(MAX)}}{V_{IN(MIN)} - V_{DS(ON)}} \approx \frac{P_{O(MAX)}}{2\eta(V_{IN(MIN)} - V_{DS(ON)})}$$

$$= \frac{500W}{2(.75)(40V - 1V)} = 8.5A$$

$$I_{P(PK)(MAX)} = \frac{I_{P(AVG)(MAX)}}{\frac{1}{2} D_{MAX}} = \frac{8.5A}{\frac{1}{2}(.72)} = 24A$$

$$I_{P(RMS)(MAX)} = I_{P(PK)(MAX)} \sqrt{\frac{1}{2} D_{MAX}} = 24A \sqrt{\frac{1}{2}(.72)}$$

$$= 14A$$

Secondary:

$$I_{S(RMS)(MAX)} = \sqrt{I^2_{O(MAX)} (\frac{1}{2} D_{MAX}) + \left(\frac{I_{O(MAX)}}{2}\right)^2 (1 - D_{MAX})}$$

$$= \sqrt{(100A)^2 (\frac{1}{2})(.72) + \left(\frac{100A}{2}\right)^2 (1 - .72)}$$

$$= 66A$$

For a core with an "area product" $AP=(A_eA_W)$, an RMS current density of:

$J = 450\ (AP)^{-.125}\ A/cm^2$

gives a core temperature rise of ~ 30°C above ambient for natural convection cooling.[5] For an EC-52, $AP = 5.7cm^4$, and:

$J = 450\ (5.7)^{-.125}\ A/cm^2 = 362\ A/cm^2$.

The required wire cross-sectional areas A_X are:

Primary:

$$A_{XP} = \frac{14A}{362A/cm^2} = .039\ cm^2$$; used 4 parallel AWG18 for $A_{XP} = .033\ cm^2$.

Secondary:

$$A_{XS} = \frac{66A}{362A/cm^2} = .18\ cm^2$$; used 3 parallel copper straps, each 20 × 400 mil, giving $A_{XS} = .16\ cm^2$.

OUTPUT FILTER

The filter capacitor (C_O) and inductor (L) are chosen to minimize output ripple voltage (v_R) while allowing fast response to a changing load. This design uses a polypropylene capacitor with extremely low ESR (7mΩ), allowing relatively high ripple currents, a small L, and therefore good large-signal dynamic response.

Maximum ripple current $i_{R(MAX)}$ occurs at minimum duty cycle and relates to $v_{R(MAX)}$ as follows:

$$i_{R(MAX)} = \frac{V_{R(MAX)}}{\frac{\tau D_{MIN}}{2C_O} + ESR} = \frac{200mV}{\frac{5\mu s(.51)}{2(20\mu F)} + 7m\Omega} = 2.8A.$$

The inductance requirement:

$$L_{MIN} = \left(\frac{V_{IN(MAX)}}{N} - V_F - V_O\right) \frac{\tau D_{MIN}}{i_{R(MAX)}}$$

$$= \left(\frac{56V}{5V} - 0.6V - 5V\right) \frac{5\mu s(.51)}{2.8A} = 5.1\mu H.$$

An Arnold A325360-2 ferrite toroid was chosen. It has an inductance index A_L of 360mH/1000 turns; the required number of turns T is:

$$T \geq \sqrt{\frac{10^6 \cdot L_{MIN(mH)}}{A_L}} = \sqrt{\frac{10^6 (.0051)}{360}} = 3.8.$$

Four turns gives L = 5.8μH. Wire size is given by:

$J_L = 450(8.64)^{-.125}\ A/cm^2 = 344\ A/cm^2$.

$$A_{XL} = \frac{100A}{344\ A/cm^2} = .29\ cm^2$$; used 12 parallel AWG14 for $A_{XL} = .25\ cm^2$.

CURRENT SENSING AND LIMITING

A current sense transformer is used to lower power dissipation in the sense resistor and to provide level shifting. A 100:1 turns ratio allows use of a 1/4 - Watt resistor. Large spikes occur at the leading edge of each current sense pulse as the junction capacitances of the secondary-side rectifiers are charged. If unattenuated, these spikes would falsely activate the current limit section of the control circuit. Therefore, the circuit of Figure 10 is used to blank the current sense signal during the first 200nS of each power pulse.

9

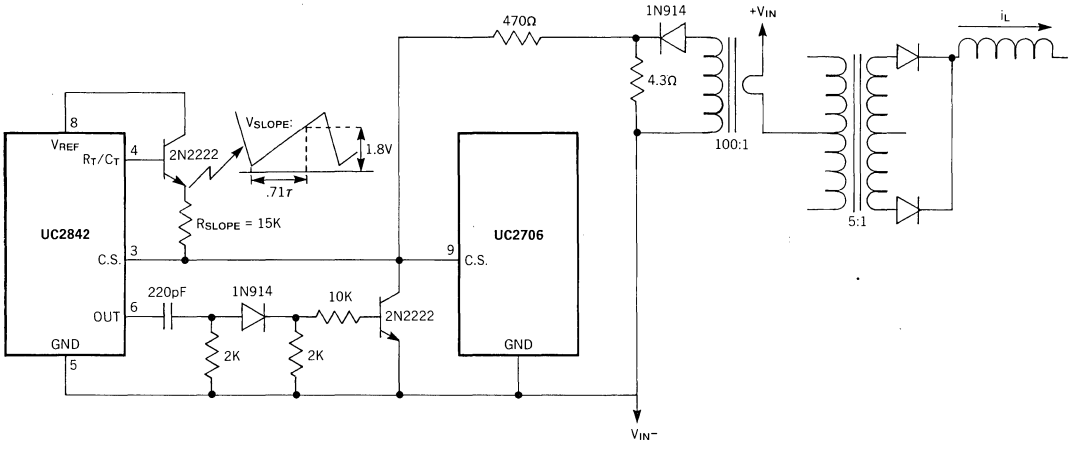

FIGURE 10. CURRENT SENSE WITH SPIKE SUPPRESSION AND SLOPE COMPENSATION.

Current limiting is performed by the UC2706 in order to achieve the fastest possible response. The UC2706 current limit threshold V_{TH} is programmed to be less than the 1 volt threshold of the UC2842.

$$V_{TH} = \frac{I_{O(MAX)}}{NN'} \cdot R_S + V_{SLOPE}\Big|_{D = .72}$$

$$= \frac{100A}{5(100)} \cdot 4.3\ \Omega + \frac{1.8V(470\Omega)}{15K\Omega + 470\Omega} = .91V$$

$$V_{PIN\ 10} = V_{TH} - .13V = .78V$$

CONTROL LOOP COMPENSATION[4]

1. Relevant Data:

f_S = 200KHz, τ = 5μs
40V ≤ V_{IN} ≤ 56V
V_O = 5V, 25A ≤ I_O ≤ 100A
0.2 Ω ≥ R_O ≥ 0.05Ω
I_{SC} = 120A

$i_{R(MAX)}$ = 2.8A
0.51 ≤ D ≤ 0.72
C_O = 20μF
ESR = 7mΩ
N = 5, N′ = 100 (transformer turns ratios)

2. Control-to-Output Response:

For the UC2842, the small signal control-to-inductor-current gain is given by:[1]

$$\frac{i_L}{V_C} = \frac{NN'}{3\ R_S}$$

The control-to-output-voltage gain is:

$$\frac{V_O}{V_C} = \frac{i_L}{V_C} \cdot R_O \cdot H_f(s)$$

$$= \frac{NN'\ R_O}{3\ R_S}\left(\frac{1 + s(2\pi \cdot ESR \cdot C_O)}{1 + s(2\pi \cdot R_O \cdot C_O)}\right)$$

Note that this response is load dependant:

a. At maximum load (minimum R_O):

$$\frac{V_O}{V_C}\Big|_{f \to o} = \frac{5(100).05\Omega}{3(4.3\Omega)} = 1.9$$

= 5.7dB (low frequency gain)

$f_P = 1/(2\pi(.05\Omega)\ 20\mu F)$
= 160KHz (filter pole frequency)

$f_Z = 1/(2\pi(7m\Omega)\ 20\mu F)$
= 1.1MHz (filter zero frequency)

b. At minimum load (maximum R_O):

$$\frac{V_O}{V_C}\Big|_{f \to o} = \frac{5(100)0.2\Omega}{3(4.3\Omega)} = 7.8 = 18dB$$

$f_P = 1/(2\pi(0.2\Omega)\ 20\mu F)$ = 40KHz

f_Z = 1.1MHz

These responses are plotted in Figure 11.

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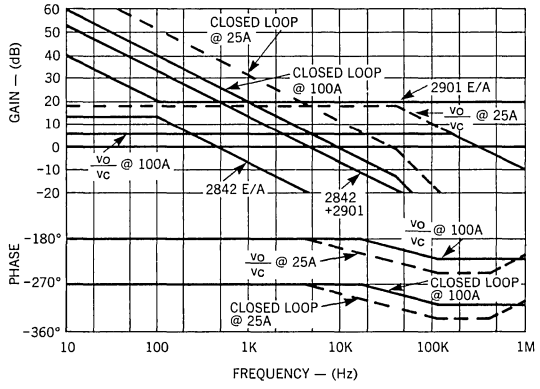

FIGURE 11. SMALL SIGNAL FREQUENCY RESPONSE.

3. Desired Closed-Loop Response:

While high gain-bandwidth is desired for fast response to dynamic loads, two stability criteria limit the achievable response characteristic. The Nyquist criterion dictates that phase margin above −360° be maintained at the frequency (f_c) at which gain crosses 0dB. Furthermore, it has been shown[6] that f_c must satisfy the following relation:

$$f_c \leq \frac{f_s}{2\pi D}$$

Using D = 0.9 to provide some margin for component tolerances,

$$f_c \approx \frac{200KHz}{2\pi(0.9)} = 35KHz.$$

4. Error Amplifier Compensation for UC2901 and UC2842:

Figure 11 shows a combined UC2901-UC2842 response curve which, when added to the control-to-output curves, yields a loop response which meets the above-mentioned stability criteria. One way of achieving this combined response is also indicated. Design equations and compensation components are shown in Figure 12.

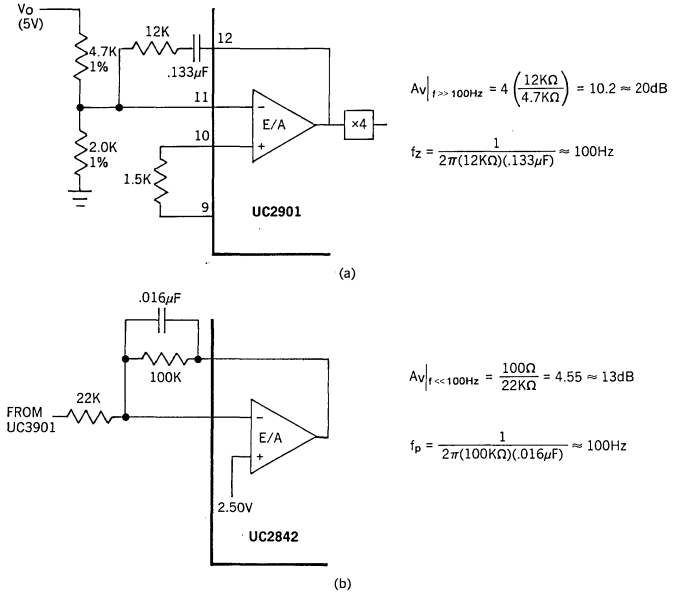

FIGURE 12. ERROR AMPLIFIER COMPENSATION FOR (a) UC2901 AND (b) UC2842.

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SLOPE COMPENSATION

Current-mode converters operated with D $\gtrsim$ 0.5 require "slope compensation" to prevent subharmonic oscillations.[7, 8, 9] In particular, if an artificial ramp is added to the current sense waveform, and if the slope magnitude of that ramp equals the deadband downslope of the inductor current (as projected to the current sense point), then any perturbations in inductor current will die out within a single cycle.[7] A resistor R_{SLOPE} connected from the timing capacitor to the current sense input can provide this ramp. Referring to Figure 10, the required value of R_{SLOPE} for the UC2842 is given by:[1]

$$R_{SLOPE} = R_f \left(\frac{(1.4V)\ NN'L}{R_S(V_O + V_F)\ T} - 1 \right)$$

$$= 470\Omega \left(\frac{1.4V(5)100(5.8\mu H)}{4.3\Omega\ (5.6V)5\mu S} - 1 \right) = 15K\Omega.$$

The emitter follower in Figure 10 prevents R_{SLOPE} from increasing the oscillator frequency.

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IMPROVED CHARGING METHODS FOR LEAD-ACID BATTERIES USING THE UC3906

ABSTRACT

This paper describes the operation and application of the UC3906 Sealed Lead-Acid Battery Charger. This IC provides reductions in the cost and design effort of implementing optimal charge and hold cycles for lead-acid batteries. Described are the design and operation of several charging circuits using this IC. The charger designs use current and voltage sensing combined with sequenced current and voltage control to maximize battery capacity and life for various applications. The presented material provides insight into expected improvements in battery performance with respect to these specific charging methods. Also presented are uses of the many auxiliary functions included on this part. The unique combination of features on this control IC has made it practical to create charge and hold cycles that truly get the most out of a battery.

AN IC FOR CHARGING LEAD-ACID BATTERIES

Battery technology has come a long way in recent years. Driven by the reduction of size and power requirements of processing functions, batteries now are used to provide portability and failsafe protection to a new generation of electronic systems. Although a number of battery technologies have evolved, the lead-acid cell remains the workhorse of the industry due to its combination of prolonged standby and cycle life with a high energy storage capacity. The makers of uninterruptible power supplies, portable equipment, and any system that requires failsafe protection are taking advantage of the improvements in this technology to provide secondary power sources to their products, for example, the sealed cell, using a trapped or gelled electrolyte, has eliminated the positional sensitivity and greatly reduced the dehydration problem.

The charging methods used to replenish or maintain the charge on a lead-acid battery have a significant effect on the performance of the cells. Building an optimum charger, one that gets the most out of a battery, is not a trivial task. Making sure that a battery undergoes the proper charge and hold cycle requires precision sensing and control of both voltage and current, logic to sequence the charger through its cycle, and temperature corrections — added to the charger's control and sensing circuits — to allow proper charging at any temperature. In the past this has required a significant number of components, and a substantial design effort as well. The UC3906 Sealed Lead-

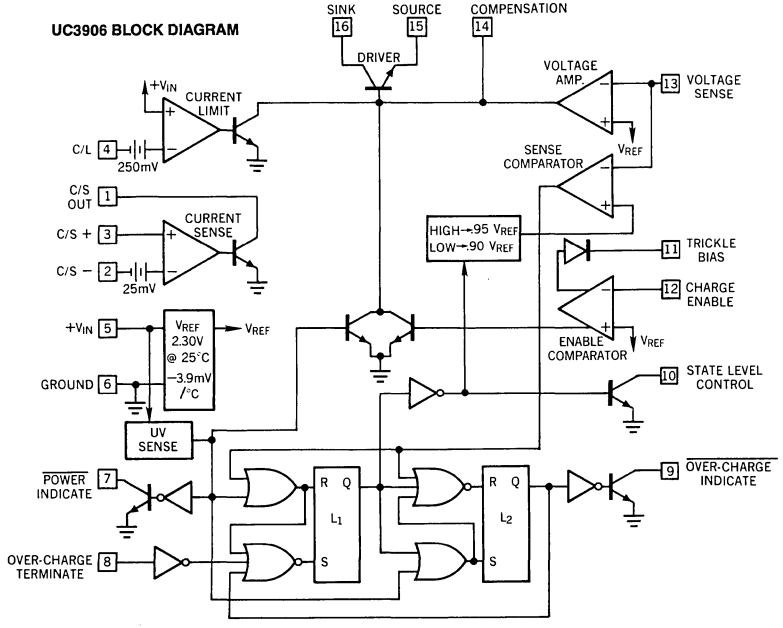

FIGURE 1. The UC3906 Sealed Lead-Acid Battery Charger combines precision voltage and current sensing with voltage and current control to realize optimum battery charge cycles. Internal charge state logic sequences the device through charging cycles. Voltage control and sensing is referenced to an internal voltage that specially tracks the temperature characteristics of lead-acid cells.

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Acid Battery Charger has all the control and sensing functions necessary to optimize cell capacity and life in a wide range of battery applications.

The block diagram for the UC3906 is shown in figure 1. Separate voltage loop and current limit amplifiers regulate the output voltage and current levels in the charger by controlling the onboard driver. The driver will supply 25mA of base drive to an external pass element. Voltage and current sense comparators are used to sense the battery condition and respond with logic inputs to the charge state logic. The charge enable comparator on this IC can be used to remotely disable the charger. The comparator's 25mA trickle bias output is active high when the driver is disabled. These features can be combined to implement a low current turn-on mode in a charger, preventing high current charging during abnormal conditions such as a shorted or reversed battery.

A very important feature of the UC3906 is its precision reference. The reference voltage is specially temperature compensated to track the temperature characteristics of lead-acid cells. The IC operates with very low supply current, only 1.7mA, minimizing on-chip dissipation and permitting the accurate sensing of the operating environmental temperature. In addition, the IC includes a supply under-voltage sensing circuit, used to initialize charging cycles at power on. This circuit also drives a logic output to indicate when input power is present. The UC3906 is specified for operation over the commercial temperature range of 0°C to 70°C. For operation over extended temperatures, −40°C to 70°C the UC2906 is available.

WHAT IS IMPORTANT IN A CHARGER?

Capacity and life are critical battery parameters that are strongly affected by charging methods. Capacity, C, refers to the number of ampere-hours that a charged battery is rated to supply at a given discharge rate. A battery's rated capacity is generally used as the unit for expressing charge and discharge current rates, i.e., a 2.5 amp-hour battery charging at 500mA is said to be charging at a C/5 rate. Battery life performance is measured in one of two ways; cycle life or stand-by life. Cycle life refers to the number of charge and discharge cycles that a battery can go through before its capacity is reduced to some threshold level. Standby life, or float life, is simply a measure of how long the battery can be maintained in a fully charged state and be able to provide proper service when called upon. The measure which actually indicates useful life expectancy in a given application will depend on the particulars of the application. In general, both aspects of battery life will be important.

During the charge cycle of a typical lead-acid cell, lead sulfate, $PbSO_4$, is converted to lead on the battery's negative plate and lead dioxide on the battery's positive plate. Once the majority of the lead sulfate has been converted, over-charge reactions begin. The typical result of over-charge is the generation of hydrogen and oxygen gas. In unsealed batteries this results in the immediate loss of water. In sealed cells, at moderate charge rates, the majority of the hydrogen and oxygen recombine before dehydration occurs. In either type of cell, prolonged charging rates significantly above C/500, will result in dehydration, accelerated grid corrosion, and reduced service life.

The onset of the over-charge reaction will depend on the rate of charge. At charge rates of >C/5, less than 80% of the cell's previously discharged capacity will be returned as the over-charge reaction begins. For over-charge to coincide with 100% return of capacity, charge rates must typically be reduced to less than C/100. Also, to accept higher rates the battery voltage must be allowed to increase as over-charge is approached. Figure 2 illustrates this phenomenon, showing cell voltage vs. percent return of previously discharged capacity for a variety of charge rates. The over-charge reaction begins at the point where the cell voltage rises sharply, and becomes excessive when the curves level out and start down again.

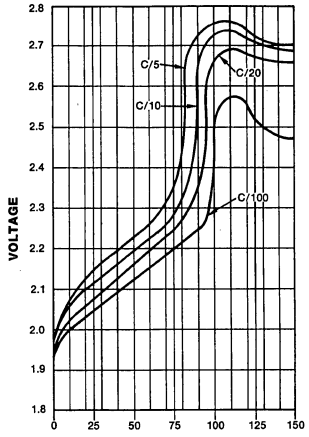

FIGURE 2. Depending on the charge rate, over-charge reactions begin, (indicated by the sharp rise in battery voltage), well below 100% return of capacity. (Reprinted with the permission of Gates Energy Products, Inc.)

Once a battery is fully charged, the best way to maintain the charge is to apply a constant voltage to the battery. This burdens the charging circuit with supplying the correct float charge level; large enough to compensate for self-discharge, and not too large to result in battery degradation from excessive overcharging. With the proper float charge, sealed lead-acid batteries are expected to give standby service for 6 to 10 years. Errors of just five percent in a float charger's characteristics can halve this expected life.

To compound the above concerns, the voltage characteristics of a lead-acid cell have a pronounced negative temperature dependence, approximately –4.0mV/°C per 2V cell. In other words, a charger that works perfectly at 25°C may not maintain or provide a full charge at 0°C and conversely may drastically over-charge a battery at +50°C. To function properly at temperature extremes a charger must have some form of compensation to track the battery temperature coefficient.

To provide reasonable re-charge times with a full 100% return of capacity, a charge cycle must adapt to the state of charge and the temperature of the battery. In sealed, or recombinate, cells, following a high current charge to return the bulk of the expended capacity, a controlled over-charge should take place. For unsealed cells the over-charge reaction must be minimized. After the over-charge, or at the onset of over-charge, the charger should convert to a precise float condition.

A DUAL LEVEL FLOAT CHARGER

A state diagram for a sealed lead-acid battery charger that would meet the above requirements is shown in figure 3.

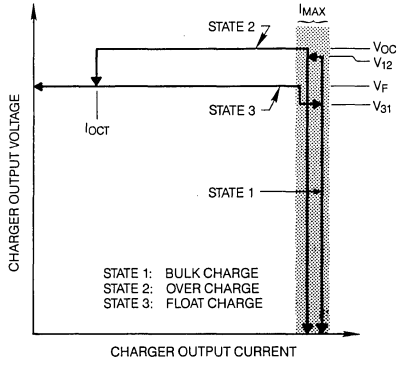

FIGURE 3. The dual level float charger has three charge states. A constant current bulk charge returns 70-90% of capacity to the battery with the remaining capacity returned during an elevated (constant) voltage over-charge. The float charge state maintains a precision voltage across the battery to optimize stand-by life.

This charger, called a dual level float charger, has three states, a high current bulk charge state, an over-charge state, and a float state. A charge cycle begins with the charger in the bulk charge state. In this state the charger acts like a current source providing a constant charge rate at I_{MAX}. The charger monitors the battery voltage and as it reaches a transition threshold, V_{12}, the charger begins its over-charge cycle. During the over-charge, the charger regulates the battery at an elevated voltage, V_{OC}, until the charge rate drops to a specified transition current, I_{OCT}. When the current tapers to I_{OCT}, with the battery at the elevated level, the capacity of the cell should be at nearly 100%. At this point the charger turns into a voltage regulator with a precisely defined output voltage, V_F. The output voltage of the charger in this third state sets the float level for the battery.

With the UC3906, this charge and hold cycle can be implemented with a minimum of external parts and design effort. A complete charger is shown in figure 4. Also shown are the design equations to be used to calculate the element values for a specific application. All of the programming of the voltage and current levels of the charger are determined by the appropriate selection the external resistors R_S, R_A, R_B, R_C.

Operation of this charger is best understood by tracing a charge cycle. The bulk charge state, the beginning, is initiated by either of two conditions. One is the cycling on of the input supply to the charger; the other is a low voltage condition on the battery that occurs while the charger is in the float state. The under-voltage sensing circuit on the UC3906 measures the input supply to the IC. When the input supply drops below about 4.5V the sensing circuit forces the two state logic latches (see figure 1) into the bulk charge condition (L1 reset and L2 set). This circuit also disables the driver output during the under-voltage condition. To enter the bulk charge state while power is on, the charger must first be in the float state (both latches set). The input to the charge state logic coming from the voltage sense comparator reports on the battery voltage. If the battery voltage goes low this input will reset L1 and the bulk charge state will be initiated.

With L1 reset, the state level output is always active low. While this pin is low the divider resistor, R_B is shunted by resistor R_C, raising the regulating level of the voltage loop. If we assume that the battery is in need of charge, the voltage amplifier will be in its stops trying to turn on the driver to force the battery voltage up. In this condition the voltage amplifier output will be over-ridden by the current limit amplifier. The current limit amplifier will control the driver, regulating the output current to a constant level. During this

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time the voltage at the internal, non-inverting, input to the voltage sense comparator is equal to 0.95 times the internal reference voltage. As the battery is charged its voltage will rise; when the scaled battery voltage at PIN 13, the inverting input to the sense comparator, reaches 0.95Vref the sense comparator output will go low. This will reset the second latch and the over-charge state will be entered. At this time the over-charge indicator output will go low. Other than this there is no externally observable change in the charger. Internally, the starting of the over-charge state arms the set input of the first latch — assuming no reset signal is present — so that when the over-charge terminate input goes high, the charger can enter the float state.

In the over-charge state, the charger will continue to supply the maximum current. As the battery voltage reaches the elevated regulating level, V_{OC}, the voltage amplifier will take command of the driver, regulating the output voltage at a constant level. The voltage at PIN 13 will now be equal to the internal reference voltage. The battery is completing its charge cycle and the charge acceptance will start to taper off.

As configured in figure 4, the current sense comparator continuously monitors the charge rate by sensing the voltage across R_S. The output of the comparator is connected to the over-charge terminate input. Whenever the charge current is less than I_{OCT}, ($25mV/R_S$), the open collector output of the comparator will be off. When this transition current is reached, as the charge rate tapers in the over-charge state, the off condition of the comparator output will allow an internal 10μA pull-up current at PIN 8 to pull that point high. A capacitor can be added from ground to this point to provide a delay to the over-charge-terminate function, preventing the charger from prematurely entering the float state if the charging current temporarily drops due to system noise or whatever. When the voltage at PIN 8 reaches its 1V threshold, latch L1 will be set, setting L2 as well, and the charger will be in the float state. At this point the state level output will be off, effectively eliminating R_C from the divider and lowering the regulating level of the voltage loop to V_F.

In the float state the charger will maintain V_F across the battery, supplying currents of zero to I_{MAX} as required. In addition, the setting of L1 switches the voltage sense comparator's reference level from 0.95 to 0.90 times the internal reference. If the battery is now discharged to a voltage level 10% below the float level, the sense comparator output will reset L1 and the charge cycle will begin anew.

The float voltage V_F, as well as V_{OC} and the transition voltages, are proportional to the internal reference on the UC3906. This reference has a temperature coefficient of

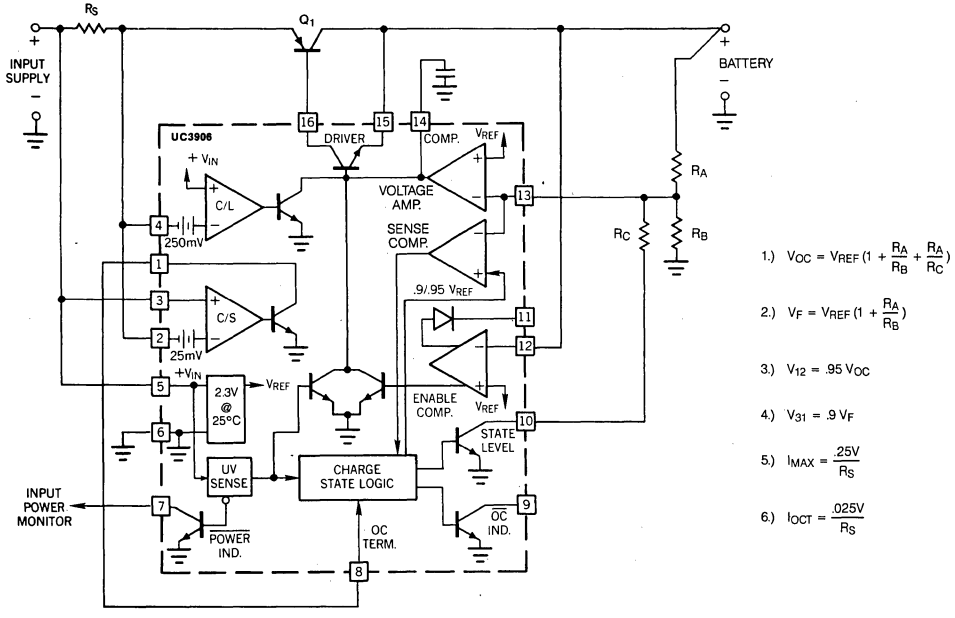

FIGURE 4. Using a few external parts and following simple design equations the UC3906 can be configured as a dual level float charger.

-3.9mV/°C. This temperature dependence matches the recommended compensation of most battery manufacturers. The importance of the control of the charger's voltage levels is reflected in the tight specification of the tolerance of the UC3906's reference and its change with temperature, as shown in figure 5.

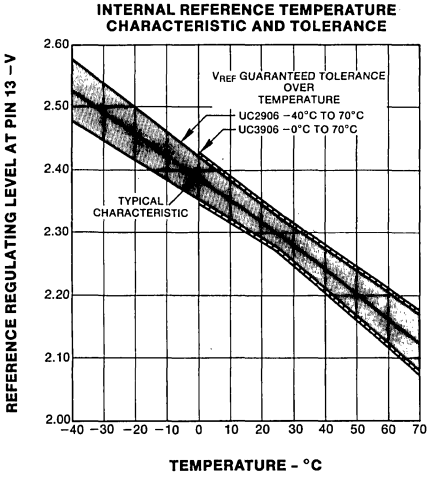

FIGURE 5. The specially temperature compensated reference on the UC3906 is tightly specified over 0 to 70°C, (-40 to 70°C for the UC2906), to allow proper charge and hold characteristics at all temperatures.

I_{MAX}, I_{OCT}, V_{OC}, and V_F can all be set independently. I_{MAX}, the bulk charge rate can usually be set as high as the available power source will allow, or the pass device can handle. Battery manufacturers recommend charge rates in the C/20 to C/3 range, although some claim rates up to and beyond 2C are OK if protection against excessive overcharging is included. I_{OCT}, the over-charge terminate threshold, should be chosen to correspond, as close as possible, to 100% recharge. The proper value will depend on the over-charge voltage (V_{OC}) used and on the cell's charge current tapering characteristics at V_{OC}.

I_{MAX} and I_{OCT} are determined by the offset voltages built into the current limit amplifier and current sense comparator respectively, and the resistor(s) used to sense current. The offsets have a fixed ratio of 250mV/25mV. If ratios other than ten are necessary separate current sensing resistors or a current sense network, must be used. The penalty one pays in doing this is increased input-to-output differential requirements on the charger during high current charging. Examples of this are shown in figure 6.

An alternative method for controlling the over-charge state is to use the over-charge indicate output, PIN 9, to initiate an external timer. At the onset of the over-charge cycle the over-charge indicate pin will go low. A timer triggered by this signal could then activate the over-charge terminate input, PIN 8, after a timed over-charge has taken place. This method is particularly attractive in systems with a centralized system controller where the controller can provide the timing function and automatically be aware of the state of charge of the battery.

The float, V_F, and over-charge, V_{OC}, voltages are set by the internal reference and the external resistor network, R_A, R_B, and R_C as shown in figure 4. For the dual level float charger the ranges at 25°C for V_F and V_{OC} are typically 2.3V-2.40V and 2.4V-2.7V, respectively. The float charge level will normally be specified very precisely by the battery manufacturer, little variation exists among most battery suppliers. The over-charge level, V_{OC}, is not as critical and will vary as a function of the charge rate used. The absolute value of the divider resistors can be made large, a divider current of 50μA will sacrifice less than 0.5% in accuracy due to input bias current offsets.

AUXILIARY CAPABILITIES OF THE CHARGER IC

Besides simply charging batteries, the UC3906 can be used to add many related auxiliary functions to the charger that would otherwise have to be added discretely. The enable comparator and its trickle bias output can be used in a number of different ways. The modification of the state diagram in figure 2 to establish a low current turn-on mode

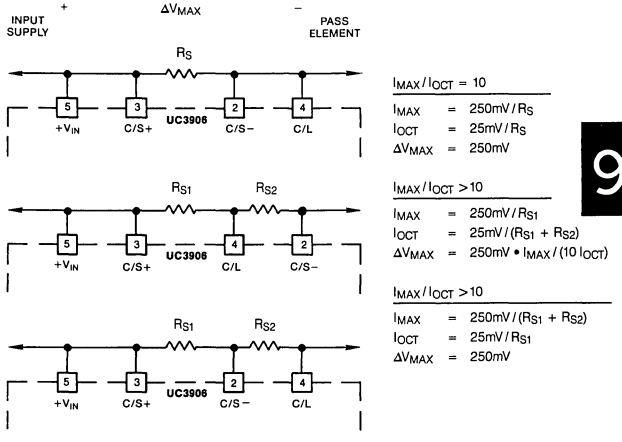

FIGURE 6. Although the ratio of input offset voltages on the current limit and current sense stages is fixed at 10, other ratios for I_{MAX}/I_{OCT} are easily obtained. Note that a penalty for ratios greater than 10 is increased voltage drop across the sensing network at I_{MAX}.

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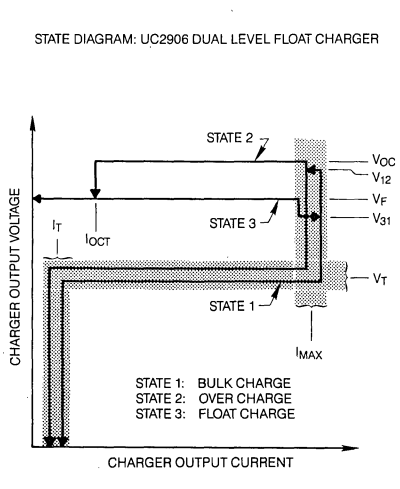
of the charger (see figure 7) is easily done. By reducing the output current of the charger when the battery voltage is below a programmable threshold, the charging system protects against: One, high current charging of a string with a shorted cell that could result in excessive outgassing from the remaining cells in the string. Two, dumping charge into a battery that has been hooked up backwards. Three, excessive power dissipation in the charger's pass element. As shown in figure 7, the enable comparator input taps off the battery sensing divider. When the battery voltage is below the resulting threshold, V_T, the driver on the UC3906 is disabled and the trickle bias output goes high. A resistor, R_T, connected to the battery from this output can then be used to set a trickle current, ($\leq$25mA) to the battery to help the charger discriminate between severely discharged cells and damaged, or improperly connected, cells.

In applications where the charger is integral to the system, i.e. always connected to the battery, and the load currents on the battery are very small, it may be necessary to absolutely minimize the load on the battery presented by the charger when input power is removed. There are two simple precautions that, when taken, will remove essentially all reverse current into the charging circuit. In figure 8 the diode in series with the pass element will prevent any reverse current through this path. The sense divider should still be referenced directly to the battery to maintain accurate control of voltage. To eliminate this discharge path, the divider in the figure is referenced to the open collector power indicate output, PIN 7, instead of ground. Connected in this manner the divider string will be in series with essentially an open when input power is removed. When power is present, the open collector device will be on, holding the divider string end at nearly ground. The saturation voltage of the open collector output is specified to be less than 50mV with a load current of 50μA.

Figure 9 illustrates the use of the enable comparator and its output to build over-discharge protection into a charger. Over-discharging a lead-acid cell, like over-charging, can severely shorten the service life of the cell. The circuit monitors the discharging of the battery and disconnects all load from the battery when its voltage reaches a specified cutoff point. The load will remain disconnected from the battery until input power is returned and the battery recharged.

This scheme uses a relay between the battery and its load that is controlled by Q1 and the presence of voltage across the load. When primary power is available Q1 is on via D5. The battery is charging, or charged, and the trickle bias output at PIN 11 is off. When input power is removed, C2 provides enough hold-up time at the load to let Q1 turn off, and the relay to close as current flows through R1. The battery is now providing power to the load and, through D1, power to the charger. The charger current draw will typically be less than 2mA. As the battery discharges, the UC3906 will continue to monitor its voltage. When the vol-



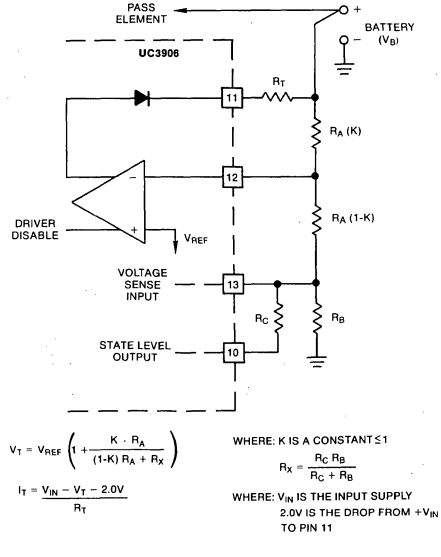


FIGURE 7. The charge enable comparator, with its trickle bias output, can be used to build protection into the charger. The current foldback at low battery voltages prevents high current charging of batteries with shorted cells, or improperly connected batteries, and also protects the pass element from excessive power dissipation.

tage reaches the cut-off level, set by the divider network, R5-R8, the trickle bias output, PIN 11, will go high. Q1 will turn back on and the relay current will collapse opening its contacts. As the load voltage drops, capacitor C1 supplies power to the UC3906 to keep Q1 on. Once the input to the charger has collapsed the power indicate pin, as shown in figure 8, will open the divider string. The battery will remain open-circuited until input power is returned. At that time the battery will begin to recharge.

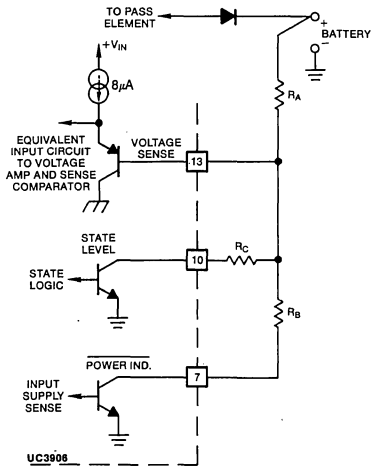


FIGURE 8. By using a diode in series with the pass element, and referencing the divider string to the power indicate pin, pin 7, reverse current into the charger, (when the charger is tied to the battery with no input power), can be eliminated.

CHARGING LARGE SERIES STRINGS OF LEAD-ACID CELLS

When large series strings of batteries are to be charged, a dual step current charger has certain advantages over the float charger of figures 3 and 4. A state diagram and circuit implementation of this type of charger is shown in figure 10. The voltage across a large series string is not as predictable as a common 3 or 6 cell string. In standby service varying self discharge rates can significantly alter the state of charge of individual cells in the string if a constant float voltage is used. The elevated voltage, low current holding state of the dual step current charger maintains full and equal charge on the cells. The holding, or trickle current, I_H, will typically be on the order of 0.005C to 0.0005C.

To give adequate and accurate recharge this charger has a bulk charge state with temperature compensated transition thresholds, V_{12}, and V_{21}. Instead of entering an elevated voltage over-charge, upon reaching V_{12} the charger switches to a constant current holding state. The holding current will maintain the battery voltage at a slightly elevated level but not high enough to cause significant overcharging. If the battery current increases, the charger will attempt to hold the battery at the V_F level as shown in the state diagram. This may happen if the battery temperature increases significantly, increasing the self-discharge rate beyond the holding current. Also, immediately following the transition from the bulk to float states, the battery will only be 80% to 90% charged and the battery voltage will drop to the V_F level for some period of time until full charging is achieved.

In this charger the current sense comparator is used to regulate the holding current. The level of holding current is determined by the sensing resistor, R_{SH}. The other series

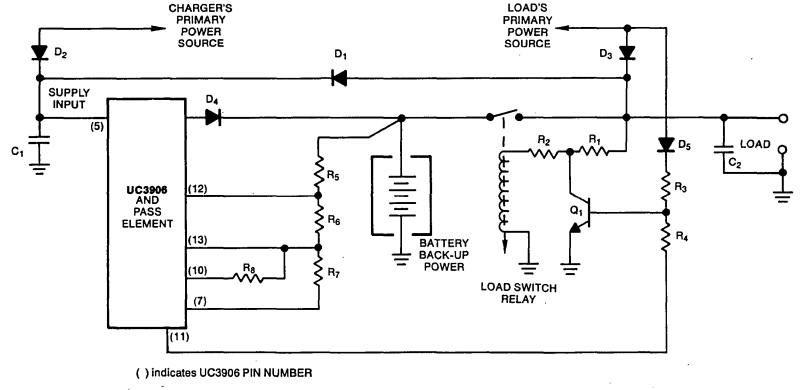


FIGURE 9. Using the enable comparator to monitor the battery voltage a precise discharge cut-off voltage can be set. When the battery reaches the cut-off threshold the trickle bial output switches off the load switch relay and the battery is left open circuited until input power is returned.

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resistor, R_E, is necessary for the current sense comparator to regulate the holding current. Its value is selected by dividing the value of I_H into the minimum input to output differential that is expected between the battery and the input supply. If the supply variation is very large, or the holding current large, (>25mA), then an external buffering element may be required at the output of the current sense comparator.

The operating supply voltage into the UC3906 should be kept less than 45V. However, the IC can be adapted to charge a battery string of greater than 45V. To charge a large series string of cells with the dual step current charger the ground pin on the UC3906 can be referenced to a tap point on the battery string as shown in figure 11. Since the charger is regulating current into the batteries, the cells will all receive equal charge. The only offset results from the bias current of the UC3906 and the divider string current adding to the current charging the battery cells below the tap point. R_B can be added to subtract the bulk of this current improving the ability of the charger to control the low level currents. The voltage trip points using this technique will be based on the sum of the cell voltages on the high side of the tap.

PICKING A PASS ELEMENT AND COMPENSATING THE CHARGER

There are four factors to consider when choosing a pass device. These are:

1. The pass device must have sufficient current and power handling capability to accommodate the desired maximum charging rate at the maximum input to output differential.
2. The device must have a high enough current gain at the maximum charge rate to keep the drive current required to less than 25mA.
3. The type of device used, (PNP, NPN, or FET), and its configuration, may be dictated by the minimum input to output differential at which the charger must operate.
4. The open loop gain of both the voltage and the current control loops are dependent on the pass element and its configuration.

Figure 12 contains a number of possible driver configurations with some rough break points on applicable current ranges as well as the resulting minimum input to output differentials. Also included in this figure are equations for the dissipation that results on the UC3906 die, equations for a resistor, R_D, that can be added to minimize this dissipation, and expressions for the open loop gains of both the voltage and current loops.

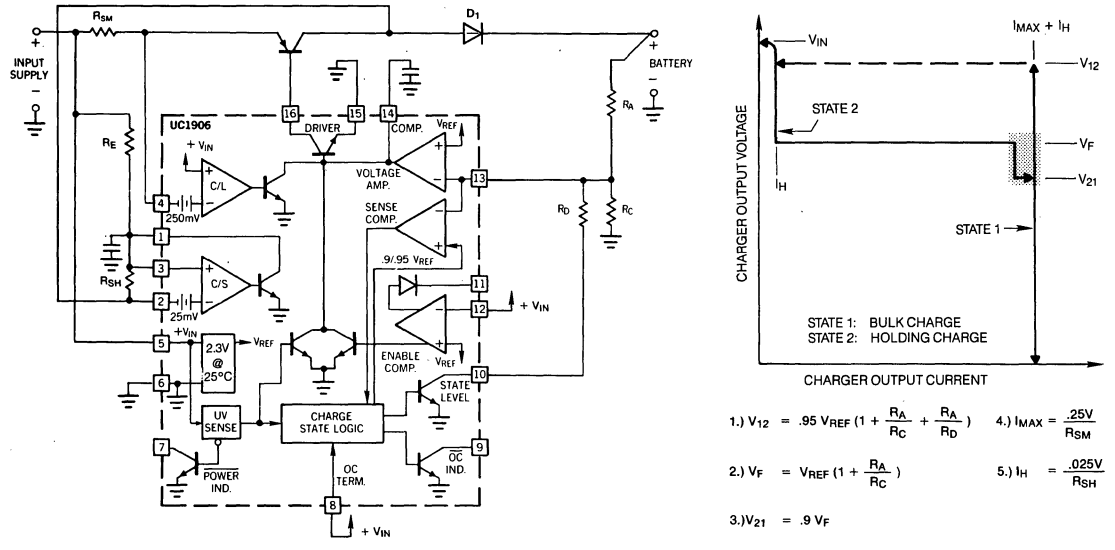


FIGURE 10. A dual step current charger has some advantages when large series strings must be charged. This type of charger maintains constant current during normal charging that results in equal charge distribution among battery cells.

As reflected in the gain expressions in figure 12, the open loop voltage gains of both the voltage and current control loops are dependent on the impedance, Z_C at the compensation pin. Both loops can be stabilized by adjusting the value of this impedance. Using the expressions given, one can go through a detailed analysis of the loops to predict respective gain and phase margins. In doing so one must not forget to account for all the poles in the open loop expressions. In the common emitter driver examples, 1 and 3, the equivalent load impedance at the output of the charger directly affects loop characteristics. In addition, a pole, or poles, will be added to the loop response due to the roll-off of the pass device's current gain, Beta. This effect will occur at approximately the rated unity gain frequency of the device divided by its low frequency current gain. The transconductance terms for the voltage and current limit amplifiers, (1/1.3K and 1/300 respectively), will start to roll off at about 500KHZ. As a rule of thumb, it is wise to kill the loop gain well below the point that any of these, not-so-predictable poles, enter the picture.

If you prefer not to go through a BODE analysis of the loops to pick a compensation value, and you recognize the fact that battery chargers do not require anything close to optimum dynamic response, then loop stability can be assured by simply oversizing the value of the capacitor used at the compensation pin. In some cases it may be necessary to add a resistor in series with the compensation capacitor to put a zero in the response. Typical values for the compensation capacitor will range from 1000pF to 0.22μF depending on the pass device and its configuration. With composite common emitter configurations, such as example 3 in figure 12, compensation values closer to

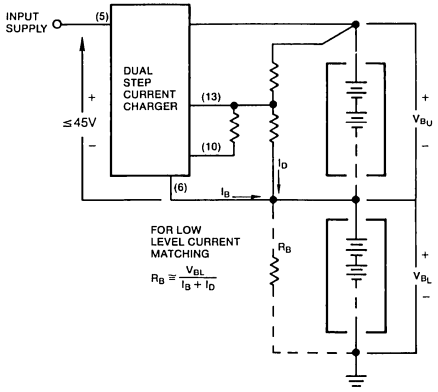
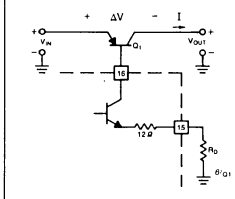
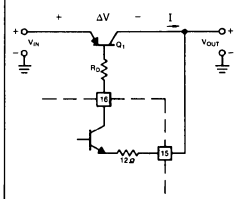
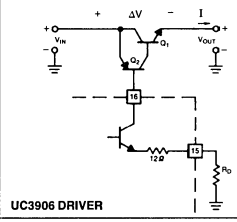
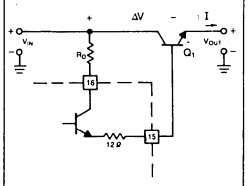


FIGURE 11. A dual step current charger can be configured to operate with input supplies of greater than 45V by using a tap on the battery to reference the UC3906. The charger uses the voltage across the upper portion of the battery to sense charging transition points. To minimize charging current offsets, R_B can be added to cancel the UC3906 bias and divider currents.

the 0.22μF value will be required to roll off the large open loop gain that results from the Beta squared term in the gain expression. Series resistance should be less than 1K, and may range as low as 100 ohms and still be effective.

The power dissipated by the UC3906 requires attention since the thermal resistance, (100°C/Watt) of the DIP package can result in significant differences in temperature between the UC3906 die and the surrounding air, (battery), temperature. Different driver/pass element configurations result in varying amounts of dissipation at the UC3906. The dissipation can be reduced by adding external dropping resistors in series with the UC3906 driver,

	COMMON EMITTER PNP	COMPOSITE FOLLOWER	COMPOSITE COMMON EMITTER	NPN EMITTER FOLLOWER
				
TOPOLOGY	UC3906 DRIVER	UC3906 DRIVER	UC3906 DRIVER	UC3906 DRIVER
CURRENT RANGE	25mA <I <1000mA	25mA <I <1000mA	600mA <I <15A	25mA <I <1000mA
MINIMUM ΔV	ΔV >0.5V	ΔV >2.0V	ΔV >1.2V	ΔV >2.7V
UC3906 DRIVER DISSIPATION	$P_D \approx \frac{V_{IN} - 0.7V}{\beta_{Q1}} \cdot I - \frac{I^2 R_D}{\beta^2_{Q1}}$	$P_D \approx \frac{V_{IN} - 0.7V - V_{OUT}}{\beta_{Q1}} \cdot I - \frac{I^2 R_D}{\beta^2_{Q1}}$	$P_D \approx \frac{V_{IN} - 0.7V}{\beta_{Q1}\beta_{Q2}} \cdot I - \frac{I^2 R_D}{\beta^2_{Q1}\beta^2_{Q2}}$	$P_D \approx \frac{V_{IN} - 0.7V - V_{OUT}}{\beta_{Q1}} \cdot I - \frac{I^2 R_D}{\beta^2_{Q1}}$
EXPRESSION FOR R_D	$R_D \approx \frac{V_{IN\,MIN} - 2.0V}{I_{MAX}} \cdot \beta_{Q1\,MIN}$	$R_D \approx \frac{V_{IN\,MIN} - V_{OUT\,MAX} - 1.2V}{I_{MAX}} \cdot \beta_{Q1\,MIN}$	$R_D \approx \frac{V_{IN\,MIN} - 0.7V}{I_{MAX}} \cdot \beta_{Q1\,MIN}\beta_{Q2\,MIN}$	$R_D \approx \frac{V_{IN\,MIN} - V_{OUT\,MAX} - 1.2V}{I_{MAX}} \cdot \beta_{Q1\,MIN}$
OPEN LOOP* GAIN OF THE VOLTAGE CONTROL LOOP	$A_{OV} \approx \frac{Z_C}{1.3K} \cdot \frac{1}{R_D + 12} \cdot \beta_{Q1} \cdot Z_O \cdot \frac{V_{REF}}{V_{OUT}}$	$A_{OV} \approx \frac{Z_C}{1.3K} \cdot \frac{V_{REF}}{V_{OUT}}$	$A_{OV} \approx \frac{Z_C}{1.3K} \cdot \frac{1}{R_D + 12} \cdot \beta_{Q1} \cdot \beta_{Q2} \cdot Z_O \cdot \frac{V_{REF}}{V_{OUT}}$	$A_{OV} \approx \frac{Z_C}{1.3K} \cdot \frac{V_{REF}}{V_{OUT}}$
OPEN LOOP* GAIN OF THE CURRENT LIMIT LOOP	$A_{OC} \approx \frac{Z_C}{300} \cdot \frac{1}{R_D + 12} \cdot \beta_{Q1} \cdot R_S$	$A_{OC} \approx \frac{Z_C}{300} \cdot \frac{1}{12/\beta_{Q1} + Z_O} \cdot R_S$	$A_{OC} \approx \frac{Z_C}{300} \cdot \frac{1}{R_D + 12} \cdot \beta_{Q1} \cdot \beta_{Q2} \cdot R_S$	$A_{OC} \approx \frac{Z_C}{300} \cdot \frac{1}{12/\beta_{Q1} + Z_O} \cdot R_S$

*Z_C = IMPEDANCE AT COMPENSATION PIN, PIN 14. Z_O = IMPEDANCE AT CHARGER OUTPUT.

FIGURE 12. There are a large number of possible driver/pass element configurations, a few are summarized here. The trade-offs are between current gain, input to output differential, and in some cases, power dissipation on the UC3906. When dissipation is a problem it can be reduced by adding a resistor in series with the UC3906 driver.

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(see figure 12). These resistors will then share the power with the die. The charger parameters most affected by increased driver dissipation are the transition thresholds, (V_{12} and V_{21}), since the charger is, by design, supplying its maximum current at these points. The current levels will not be affected since the input offset voltages on the current amplifier and sense comparator have very little temperature dependence. Also, the stand-by float level on the charger will still track ambient temperature accurately since, normally, very little current is required of the charger during this condition.

To estimate the effects of dissipation on the charger's voltage levels, calculate the power dissipated by the IC at any given point, multiply this value by the thermal resistance of the package, and then multiply this product by –3.9mV/°C and the proper external divider ratio. In most cases, the effect can be ignored, while in others the charger design must be tweaked to account for die dissipation by adjusting charger parameters at critical points of the charge cycle.

SOME RESULTS WITH THE DUAL LEVEL FLOAT CHARGER

In figure 13 the schematic is shown for a dual level, float charger designed for use with a 6V, 2.5amp-hour, sealed lead-acid battery. The specifications, at 25°C, for this charger are listed below.

Input supply voltage . . . . . 9.0V to 13V
Operating temperature range . . . . . 0°C to 70°C
Start-up trickle current (I_T) . . . . . 10mA (V_{IN} = 10V)
Start-up voltage (V_T) 5.1V
Bulk charge rate (I_{MAX}) 500mA (C/5)
Bulk to OC transition voltage (V_{12}) . . 7.125V
OC voltage (V_{OC}) 7.5V
OC terminate current (I_{OCT}) 50mA (C/50)
Float voltage (V_F) 7.0V
Float to Bulk transition voltage (V_{31}) 6.3V
Temperature coefficient on voltage levels . . . . . –12mV/°C
Reverse current at charger output with the input supply at 0.0V . . . . $\leq 5\mu A$

In order to achieve the low input to output differential, (1.5V), the charger was designed with a PNP pass device that can operate in its saturation region under low input supply conditions. The series diode, required to meet the reverse current specification, accounts for 1.0V of the 1.5V minimum differential. Keeping the reverse current under 5μA also requires the divider string to be disconnected when input power is removed. This is accomplished, as discussed earlier, by using the input power indicate pin to reference the divider string.

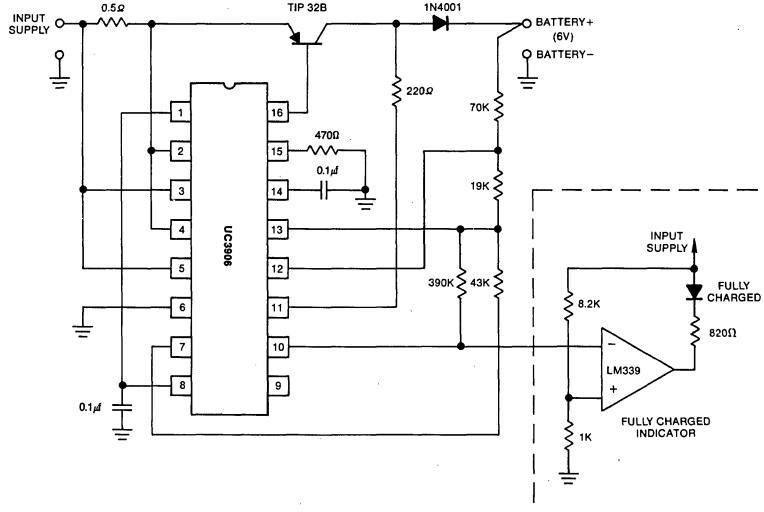

FIGURE 13. This dual level float charger was designed for a 6V (three 2V cells) 2.5AH battery. A separate "fully charged" indicator was added for visual indication of charge completion.

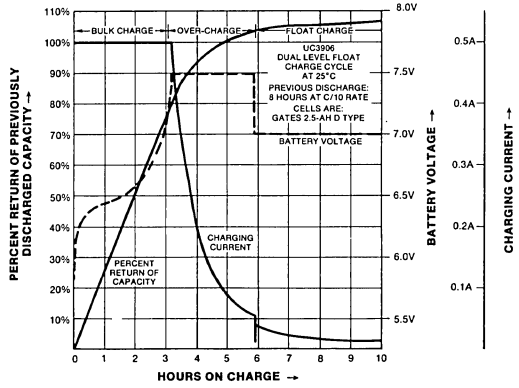

FIGURE 14. The nearly ideal characteristics of the dual level float charger are illustrated in these curves. The over-charge state is entered at about 80% return of capacity and float charging begins at just over 100% return.

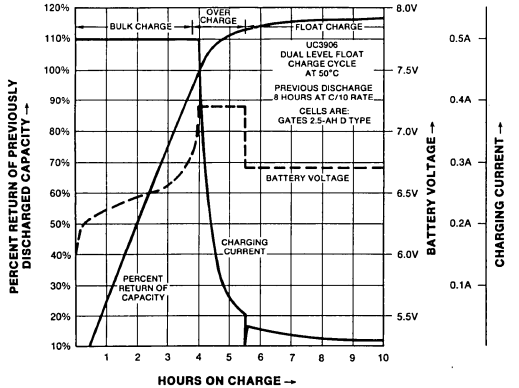

FIGURE 15. At elevated temperatures the maximum capacity of lead-acid cells is increased allowing greater charge acceptance. To prevent excessive over-charging though, the charging voltage levels are reduced.

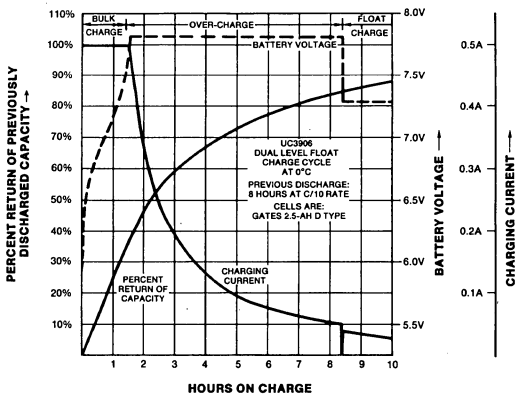

FIGURE 16. At lower temperatures the capacity of lead-acid cells is reduced as reflected by the less-than-100% return of capacity in this 0°C charge cycle, illustrating the need for elevated charging voltages to maximize returned capacity.

The driver on the UC3906 shunts the drive current from the pass device to ground. The 470ohm resistor added between PIN 15 and ground keeps the die dissipation to less than 100mW under worst case conditions, assuming a minimum forward current gain in the pass element of 35 at 500mA.

The charger in figure 13 includes a circuit to detect full charge and gives a visual indication of charge completion with an LED. This circuit turns on the LED when the battery enters the float state. Entering of the float state is detected by sensing when the state level output turns-off.

Figures 14-16 are plots of charge cycles of the circuit at three temperatures, 25°C, 50°C and 0°C. The plots show battery voltage, charge rate, and percent return of previously discharged capacity. This last parameter is the integral of the charge current over the time of the charge cycle, divided by the total charge volume removed since the last full charge. For all of these curves the previous discharge was an 80% discharge, (2amp-hours), at a C/10, (250mA), rate. The discharges were preceded by an over-night charge at 25°C.

The less than 100% return of capacity evident in the charge cycle at 0°C is the result of the battery's reduced capacity at this temperature. The tapering of the charge current in the over-charge state still indicates that the cells are being returned to a full state of charge.

REFERENCES

1. Eagle-Picher Industries, Inc., Battery Notes #200, #205A, #206, #207, #208.
2. Gates Energy Products, Inc., Battery Application Manual, 1982.
3. Panasonic, Sealed Lead-Acid Batteries Technical Handbook.
4. Yuasa Battery Co., Ltd., NP series maintenance-free rechargeable battery Application Manual.

9

NEW PULSE WIDTH MODULATOR CHIP CONTROLS 1 MHz SWITCHERS

ABSTRACT

Controversy prevails as to the benefits of pushing switched mode pulse width modulated power supplies higher and higher in frequency. Two facts are undisputed though: the industry is pushing switching frequencies up daily and no PWM control IC has been available to optimally control circuits running above several hundred kilohertz. A new IC, the UC3825, has been developed with the top end of the PWM frequency spectrum in mind to simplify high speed control problems. This chip, suitable to either voltage or current mode control, addresses the speed critical parameters that have been glossed over in the past: error amp bandwidth, output drive capability, oscillator frequency range, and propagation delay. A one megahertz, 50 watt supply has been built to demonstrate the chip.

PWM CONTROLLER REVIEW

Briefly reviewing popular control IC's on the market today should serve to illustrate one source of the headaches belonging to designers of high frequency switching power supplies. The snaggle-toothed appearance of the table illustrates the fact that high speed parameters have generally been ignored. The entries in this table represent the tried and true first and second generation standbys (1524, 1525, 494), dedicated off line control (1840), and current mode (1846). All these architectural approaches have certainly proven sufficient for numerous converter designs, but all lack the processing speed required to keep track of a 1 MHz switcher, or even 200 kHz for that matter. Many specifications in the table are missing completely, some are only typical, and the few guaranteed limits leave much room for improvement.

Of prime importance here is the delay time between fault detection and turning off the power switch – the speed critical path. When a fault occurs, either the on chip over-current sense section or an off chip fault detector plus the shutdown section of the chip must work fast enough to turn off the power switch before destructive current levels introduce an automatic (and permanent) power down feature to the supply. This feature, of course, is manifested in blown power devices. The problem is aggravated at the onset of core saturation, since switch currents then rise at much faster rates.

Also important is the drive capability of the output stage of the control chip chosen. Rise and fall times must be consistent with switching speeds or else an output buffer will have to be added. This, of course, adds delay to the speed critical path placing tighter demands on the delays through the chip or forcing the designer to over-specify the power elements to insure fault survival. Over-specifying, however, adds cost, weight and volume as transistors, heat-sinks, and transformers are beefed-up. These consequences are in direct opposition to the very motives for going to higher frequencies in the first place – reduced volume and lower cost.

On-chip error amplifiers have also been a design obstacle in the past. Why build a high frequency switcher and then over compensate the loop due to lack of error amp bandwidth? Designers have been forced to conser-

SPEED COMPARISON OF PWM CONTROLLER IC'S

	SHUT DOWN DELAY (ns)		OVER-CURRENT SENSE DELAY (ns)		ERROR AMP BANDWIDTH (MHz)		ERROR AMP SLEW RATE (V/ s)		OUTPUT RISE/FALL TIME (ns)	
	TYP	MAX	TYP	MAX	TYP	MIN	TYP	MIN	TYP	MAX
SG3524	–	–	–	–	3	–	–	–	200	–
UC3524A	200	–	600	–	3	–	–	–	200	–
UC3525A	200	500	–	–	2	1	–	–	100	600
TL494	–	–	–	–	0.8	–	–	–	200	400
UC3840	–	–	200	400	2	1	0.8	–	–	–
UC3846	300	600	200	500	1	0.7	–	–	50	300
UC3825	50	80	50	80	5.5	3	12	6	30	60

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vatively use the bandwidth available simply due to a lack of guaranteed specifications in many cases. Also, some characteristics which would prove useful haven't been specified at all. Slew rate is such a specification that has great bearing on the large signal response of the supply.

By comparison, the 3825 specifically addresses the speed critical parameters. Maximum propagation delays of 80 ns nearly belong in the "order of magnitude" improvement catagory. Slicing delays yielded a hefty output stage capable of 1.5 Amp peak currents. The guaranteed rise time is, in fact, more a function of internal slew rates than external loading in the 1000 pF range. The error amp guaranteed to 3 MHz and 6 V/μs promises ease of use when controlling wide-band loops.

UC3825 BLOCK DIAGRAM

The design philosophy for the 3825 was to build a chip faster than any other available and tailor it to fit neatly into high frequency converter designs. It includes a dual totem-pole output stage capable of driving most power mosfet gates stand-alone, and the versatility to be useful for DC to DC, off-line, bridge, flyback, push-pull, and even resonant mode converter topologies. The member of a family covering the conventional temperature ranges, the UC3825 is specified for zero to 70 degrees centigrade while the UC2825 spans −25 to 85, and the UC1825, −55 to 125.

The block diagram of the 3825 (figure 1) is architecturally similar in many respects to a number of previous PWM controllers. It includes an oscillator, under-voltage-lock-out circuit, trimmed bandgap voltage reference, wideband error amplifier, PWM comparator, PWM latch, toggle flip-flop, soft start section, comparators for over-current sensing and reinitializing soft start, and dual totem-pole outputs. The input to the PWM comparator is brought out to a separate pin so that it can be connected either to the timing capacitor for conventional PWM designs or a current sensing network for current mode control schemes.

In normal operation, the oscillator establishes a fixed clock frequency issuing blanking pulses to terminate one period and begin the next. These pulses serve to reset the PWM comparator while blanking the outputs off. After the blanking pulse, one output turns on until the ramp input (level shifted 1.25 Volts) exceeds the error amp output voltage. This sets the PWM latch which turns the output off and triggers the toggle flip-flop, selecting the other output for the next period.

THE SPEED CRITICAL PATH

The blocks that set the 3825 aside as the controller best suited for frequencies over several hundred kilohertz are those in the speed critical path (high-lighted blocks in figure 1.): the PWM comparator and current limit comparator in the front end; the PWM latch and associated internal logic; and the ouput stage. Signal

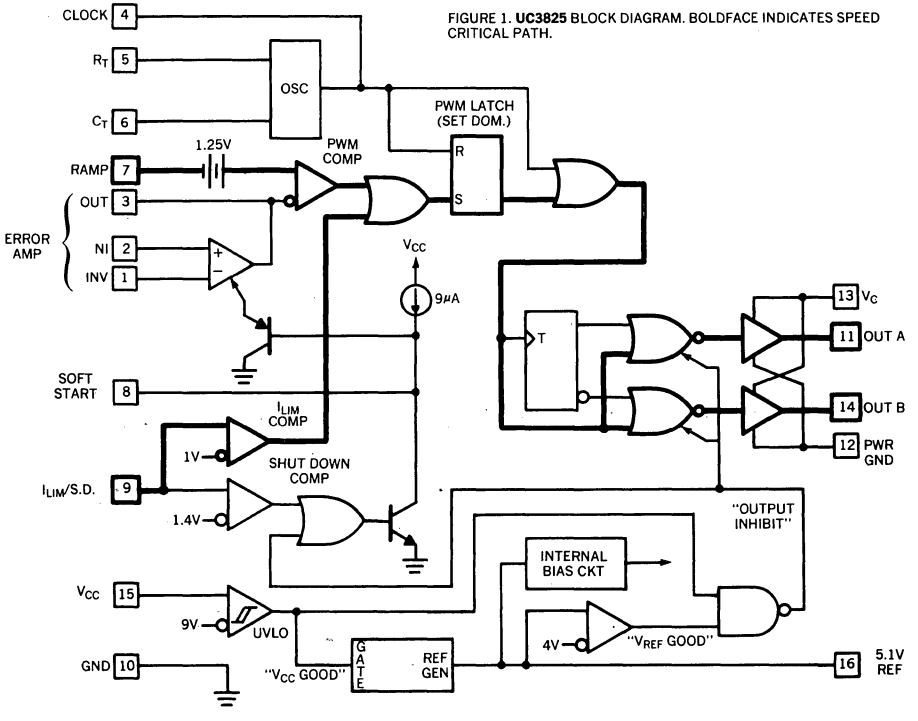


FIGURE 1. **UC3825** BLOCK DIAGRAM. BOLDFACE INDICATES SPEED CRITICAL PATH.

propagation through these subcircuits makes or breaks a design during a fault condition. In the 3825, the propagation delay from either the Ramp input or the Current-limit sense input to the output pins is typically 50ns, very much faster than any chip available today.

Comparators

The PWM comparator is basically an npn differential pair with an emitter follower output (figure 2a). The pair is biased so that the output swing is one Vbe. This guarantees none of the transistors in the comparator will saturate while providing output voltage levels compatible with the internal logic. In order to assure that the input common mode range of the comparator is not exceeded (the range of an npn input pair cannot go below approximately one Volt), a 1.25 Volt level shift is included between the non-inverting input of the comparator and the input pin of the chip. This allows the ramp input to swing from zero to approximately three Volts. The inverting input is tied directly to the output of the error amplifier.

The benefit of this approach is ease of use both in current mode and conventional PWM applications. For the older PWM circuit approach, the ramp input pin can be tied directly to the oscillator Ct pin while current mode users can simply tie a ground referenced current sense network directly to the Ramp pin.

The current limit comparator is very similar in design to the PWM comparator. Its inverting input is referenced internally to a one Volt level derived from the 5.1 Volt reference allowing the non-inverting input to be brought directly to the current limit pin. Functionally, when a fault causes the Current-limit pin to exceed one Volt, it acts just like the PWM comparator, setting the PWM latch and causing the outputs to remain off for the duration of the clock cycle.

The current-limit comparator can also be combined with the 3825 outputs and a few external components to form a constant volt-second product clamp (figure 2b). This clamp is useful in current mode systems to prevent core saturation during load transients. When either output turns on (goes high), capacitor, C, is charged from Vin through resistor, R. Normal circuit operation would turn off the outputs causing C to be discharged before it reaches one Volt. If, however, it does reach one Volt, the current-limit comparator terminates the output pulse. Since the charge rate is proportional to Vin (assuming Vin is much greater than one Volt), then a constant Volt-second product clamp of one Volt times RC is achieved.

Logic

All of the speed critical logic, including the PWM latch, the toggle flip-flop, and various gates are a cross between emitter coupled logic and emitter function logic. In either case, their speed relies on emitter coupled pairs and emitter follower buffers biased to insure that no transistor saturates. Although two OR's, a NOR and the PWM latch are directly in the critical path between the input comparators and the output drivers, they account for only twenty percent of the total delay, the remainder being shared between the comparators and the output stage.

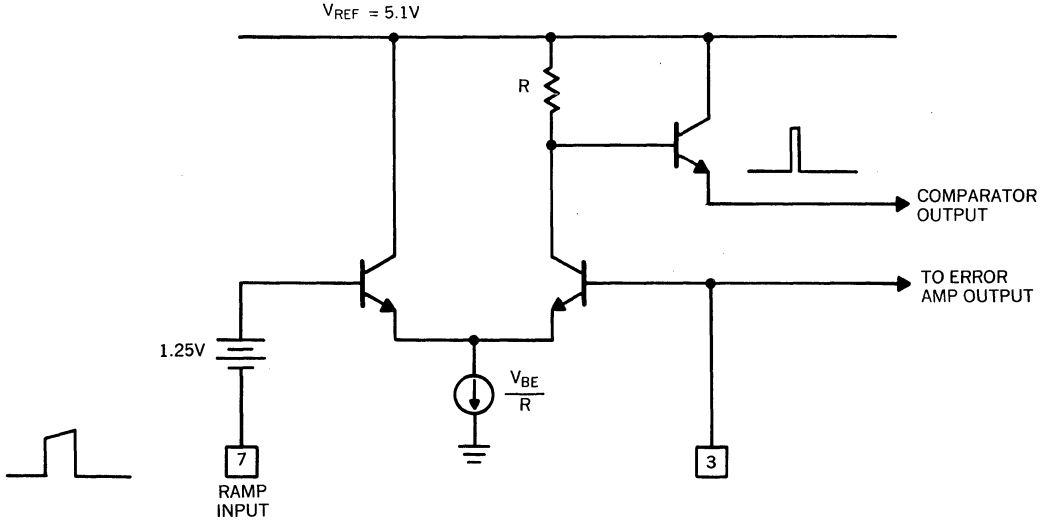
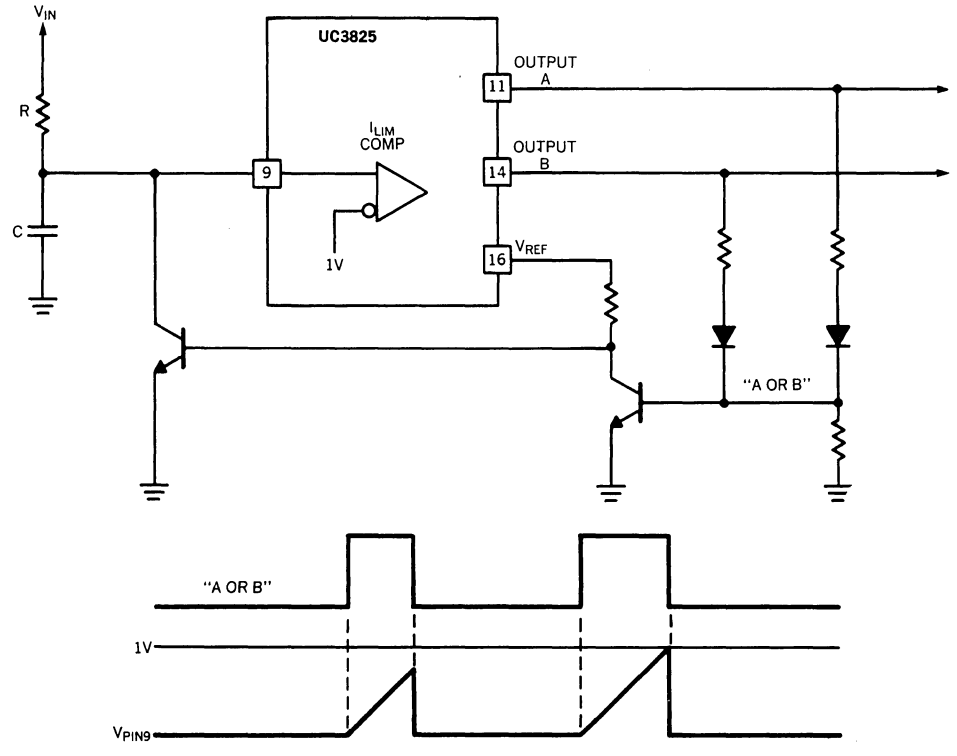


FIGURE 2a. PWM COMPARATOR SCHEMATIC.



MAXIMUM VOLT — SECOND PRODUCT = RC x 1V

FIGURE 2b. CONSTANT VOLT-SECOND PRODUCT CLAMP IMPLEMENTED USING THE CURRENT LIMIT COMPARATOR.

Outputs

Speed from one pin to another does little or no good unless the signal coming out of the chip has the strength to do its job. The dual totem-pole drivers of the 3825 are capable of driving 1000 picofarads from one rail to the other in a mere 30 nanoseconds. In fact the peak current avilable is in excess of 1.5 Amps. This kind of brute strength is sufficient for driving a wide range of power mosfet's in a variety of applications.

Some older PWM controllers with totem-pole output stages are plagued with hefty amounts of cross conducted charge during output transitions. This can result in major self heating problems especially at higher clock rates. The 3825 output stage (figure 3a) has been modeled after the successful designs of the UC3846 and UC3842. The differences are in bias values and the addition of Schottky diodes. This circuit guarantees the output transistors, Q1 and Q2, are driven with complementary signals to keep cross conducted charge under control. This approach necessarily involves a compromise since speed is of the utmost concern. Delays could be inserted to guarantee zero cross conducted charge, but that would be contrary to the required propagation delays for high speed operation. The outputs have been adjusted to yield these rise and fall times at a penalty of only 20 nanocoulombs of cross conducted charge per transition. At a clock frequency of 500 kHz, this only adds an additional 10 mA to the supply current.

Rather than dwell on cross conducted charge, which is measured with no load on the outputs, it is more appropriate to examine the performance with typical loads. The most anticipated load is a power mosfet. The impedence presented by the gate of the fet is application dependent, but is primarily capacitive. Therefore, consider the requirements of driving a capacitor with a square wave voltage. The charge required for one cycle is equal to the capacitance times the voltage. The average current taken from the supply is that charge times the switching frequency. This determines the power required from the supply to drive the cap. Since the cap is an energy storage element, all the power

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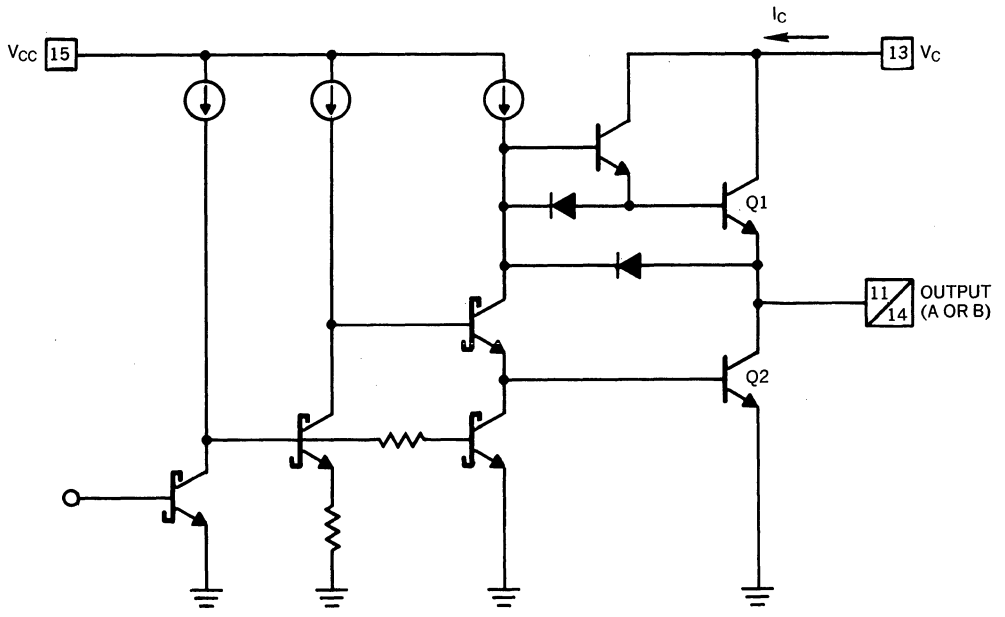
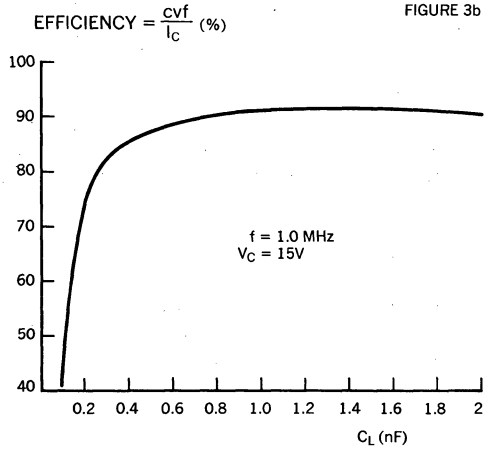


FIGURE 3a. OUTPUT STAGE SIMPLIFIED SCHEMATIC.

taken from the supply is dissipated by the chip. An efficiency figure for the chip can be defined as the ratio of the theoretical power dissipation to the actual power dissipated by the chip. This can be determined for a given frequency and supply voltage by measuring the average supply current into the Vc pin (assuming the peak output voltage is approximately equal to the supply voltage). The figure of efficiency, then, is: (CVf)/Ic. The graph of figure 3b shows the 3825 optimized to drive capacitances above 200pF. Care should always be taken when driving high capacitive loads to make sure the maximum power dissipation level of the chip is not exceeded.

FIGURE 3b



Another side effect of the output stage should be considered. Any node in a circuit capable of driving large capacitances at these rates begins quickly to resemble an LC tank. Transmission lines, even one inch in length, can become troublesome. The trouble occurs when, on the falling edge at an output, the load rings and actually pulls the output pin below ground. For years IC manufacturers have been warning users not to allow certain pins to go below ground and the 3825 output pins carry the same warning. The collector of the pull down transistor becomes a parasitic npn emitter when pulled below the chip's substrate, which is grounded (figure 4). The collector, or collectors as the case is, are every other npn collector and pnp base on the chip. The ones that are closer to the parasitic emitter collect proportionally more current than ones further away. Physical size of the parasitic collectors also plays a similar role. The results of this phenomenon can range from nonobservable to severe. Resembling leakage current internally, reference voltages can be altered, oscillator frequency can jitter, or chip temperature can be elevated. Dummy collectors tied to ground are inserted into the 3825 chip which help to attenuate this problem but the designer still needs to be aware of it. The problem's potential is not a horror story, though. Among the easiest of solutions is some form of damping in the load circuit (for example ten ohms series resistance) and a good high speed diode, Schottky if possible, to clamp the output pin's negative going excursion.

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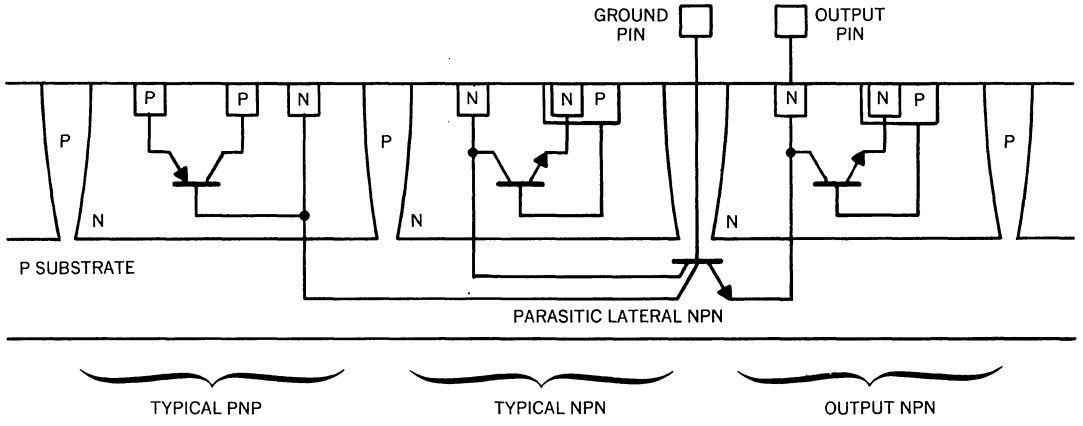

FIGURE 4. PARASITIC NPN TURNS ON WHEN SUBSTRATE – EPI JUNCTION IS FORWARD BIASED.

HIGH SPEED COMPLEMENTARY BLOCKS

An integrated circuit controller with delays of 50ns through its speed critical path is certainly a leading candidate for high frequency switcher applications. There are a few blocks just off the race path that need also to be fast in order to fully qualify the chip for such applications. The oscillator and error amplifier are two such blocks.

Oscillator

From the users point of view, the oscillator looks identical to many that have gone before it (figure 5a). Composed of an all npn comparator, this oscillator has dual thresholds – the upper at 2.8 Volts and the lower at one Volt. Charging current for the timing capacitor, Ct, is mirrored from the timing resistor, Rt. The Rt pin is held at a temperature stable 3 Volts. Temperature stability of the oscillator, then, is achieved by maintaining stable thresholds at the comparator. When Ct has charged to the upper threshold, Q3 turns on to sink a controlled current of approximately 10 mA. The effect of this action is that the discharge of Ct is done in an orderly manner allowing the comparator to reliably catch it when crossing the lower threshold. This also prevents Q3 from saturating, reducing delays in the oscillator and enabling it to operate at higher frequencies. The 3825 oscillator is nominally specified at 400kHz with an initial guaranteed accuracy of 10%. Temperature stability is typically better than 5% while voltage stability (frequency shift over supply voltage) is 0.2%. Oscillator dead time, which effects controller dynamic range, can typically be held to 100ns at 1MHz, allowing 90% duty cycles.

In applications where two 3825's are used in close proximity and synchronization is desired (figure 5b), the oscillator in one chip can be disabled by tying Rt to the reference Voltage. That chip, then, must be clocked by joining the clock pins of both chips. Multiple 3825's also can be synchronized from a master 3825 or other external sync signal. The slave chips are programmed to run at a frequency somewhat lower than the master chip. The master then inserts a sync pulse forcing each slave's Ct over the top threshold and causing discharge action to occur. This way, each chip generates its own clock pulses synchronized to a master clock.

Error Amplifier

The 3825 error amplifier is a voltage gain amp with premium bandwidth and slew rate. Again using only npn's in the signal path, a compensated unity gain bandwidth of 5.5 MHz is achieved. The simplified schematic (figure 6) shows the signal path of the amplifier. Note that while the compensation scheme is not extremely complex or brand new in nature, neither is it the simple dominant pole approach. Included are two zeros located beyond the unity gain frequency to enhance phase margin. One is created by a capacitor across the emitter degeneration resistors in the first stage and the second is formed by a resistor in series with the dominant pole capacitor.

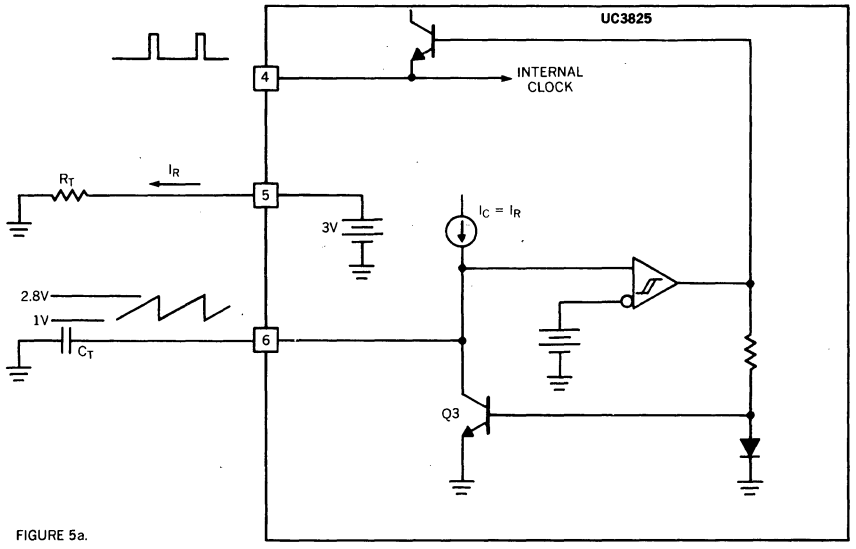

FIGURE 5a.

FIGURE 5b.

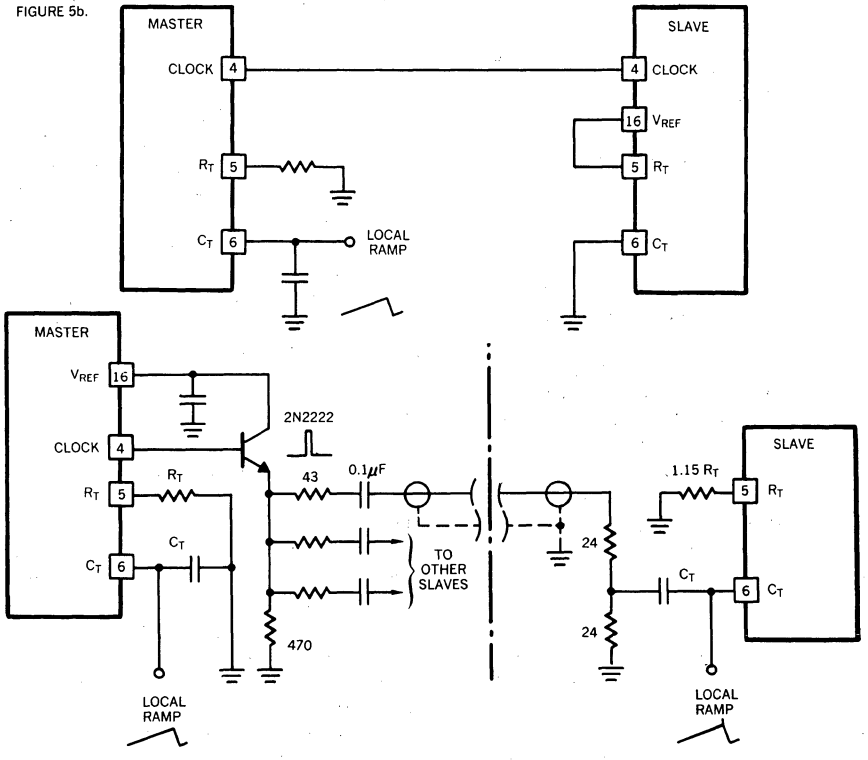

FIGURE 5. OSCILLATOR SIMPLIFIED SCHEMATIC (a) AND TWO SYNCHRONIZATION METHODS (b).

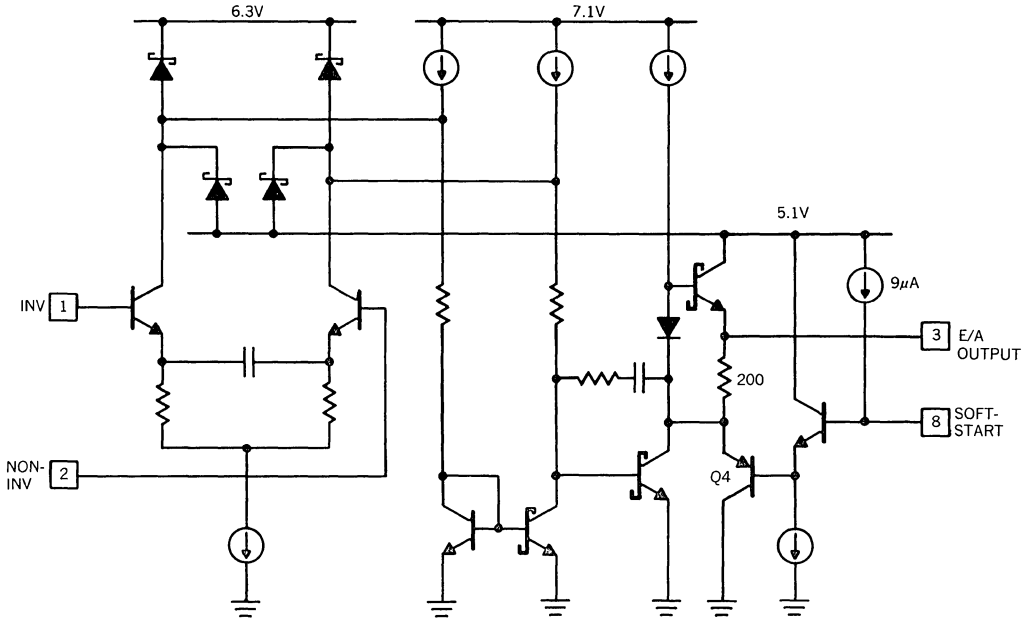

FIGURE 6. SIMPLIFIED SCHEMATIC OF WIDE BAND ERROR AMPLIFIER SHOWING SOFT START CLAMP SCHEME.

By degenerating Gm, the emitter resistors allow an increased first stage bias current level. This contributes to a 12 V/μs typical slew rate. High slew rate, while desirable for good large signal transient response, is not enough to guarantee minimal response time. Often an amplifier may have high slew rates yet exhibit long delay times coming out of saturation when it has been driven to a rail. To defeat this problem, all critical nodes within the amp have been Schottky clamped.

GLUE BLOCKS

The remaining blocks, while not speed critical, mold the 3825 into a more complete PWM controller. The reference, a time proven design, is trimmed to guarantee 5.1 Volts at better than one percent tolerance. This voltage is then held over conditions of line, load, and temperature changes to a two percent total spread.

Soft-start is very simply implemented by a pnp clamp transistor merged into the output stage of the error amp (figure 6). During soft start, while the 9 μA current source is charging the external capacitance on pin 8, Q4 actively forces pin 3 to follow pin 8. In this manner a controlled slow start can be achieved for either voltage or current mode systems. When the error amp comes into regulation, Q4's emitter-base junction is reverse biased and offers no further interference to the normal operation of the amp.

In addition to slow starts, the soft-start pin can be used to other ends. Clamping the maximum voltage this pin is allowed to rise to will then effectively clamp the maximum swing of the error amplifier. In a conventional PWM scheme this results in a duty cycle clamp while in a current mode application, it establishes the maximum peak current level.

Fault conditions are sensed by the 3825 at pin 9 which is shared by the inputs of the current limit comparator and the shut down comparator. When this pin exceeds one Volt, the current limit comparator sets the PWM latch, terminating the output for the remainder of that cycle. As with normal operation, setting the PWM latch causes the toggle flip-flop to switch states. If the pin is further raised to exceed 1.4 Volts, the shut-down comparator forces the soft-start pin to sink a guaranteed minimum of one milliampere rather than sourcing 9 microamperes. Thus the shut down comparator causes the soft start capacitor to be discharged rapidly. After the fault signal is removed the 3825 will then execute a normal soft-start sequence.

One method of combining current-limit and shut-down signals is shown in figure 7. Here, in a current mode control example, a current sense transformer is used to translate switch current to proper voltage analogs for optimal control at both the Ramp and Current-limit sense pins while the shut-down signal is inserted with a resistive summing technique.

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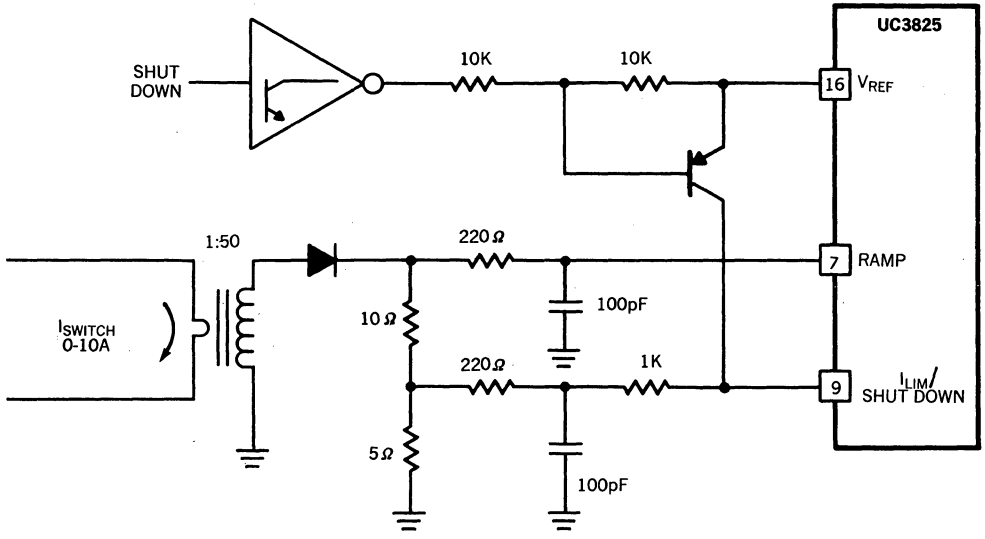

FIGURE 7. CURRENT LIMIT SENSE AND SHUT DOWN SIGNALS ARE COMBINED AT PIN 9 IN THIS CURRENT MODE EXAMPLE.

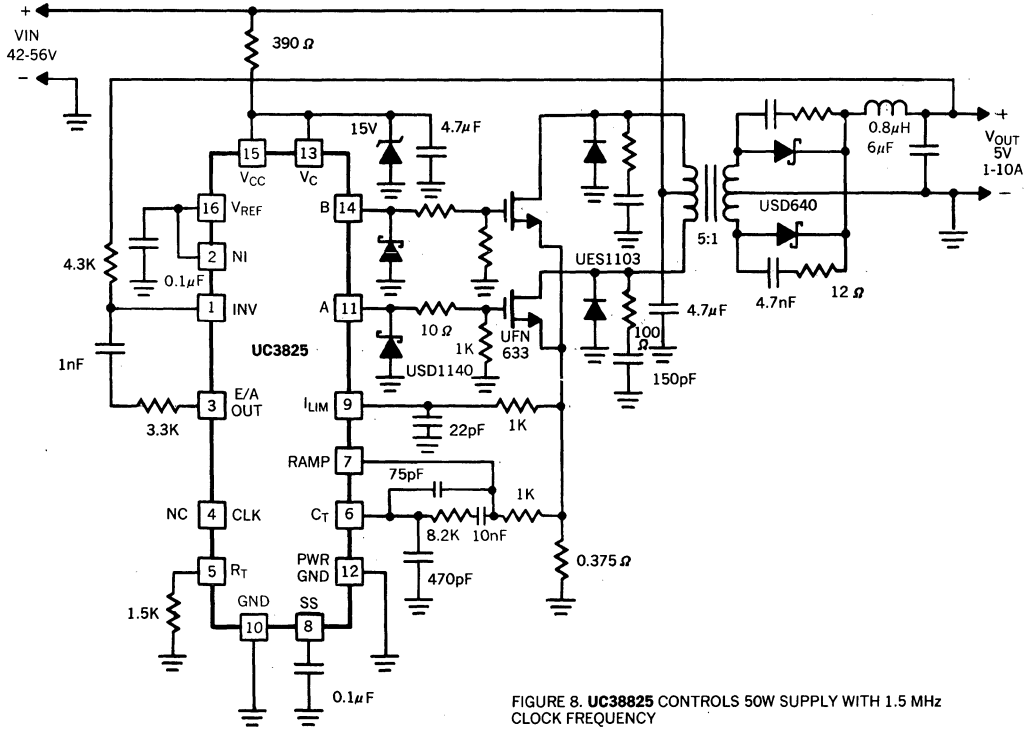

FIGURE 8. **UC38825** CONTROLS 50W SUPPLY WITH 1.5 MHz CLOCK FREQUENCY

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Starting the 3825 involves the Under-voltage lockout portion of the chip. This block acts like a comparator with it's inverting input biased to 9 Volts and having 0.8 Volts of hysteresis. If Vcc is below the UVLO threshold, the reference generator and the internal bias are turned off, Keeping Icc at a typical 1.1 mA and the outputs in a high impedence state. When Vcc exceeds the UVLO threshold, the reference is turned on and the chip comes alive. Bedlam is avoided, however, as a second comparator monitors the reference voltage and inhibits the outputs until the reference is high enough to ensure intelligent operation. This inhibit signal also holds the soft start pin at a low voltage. After the reference is sufficiently high, the chip begins a soft start sequence.

50 WATT DC-DC PUSH-PULL CONVERTER

A 48 to 5 Volt, 50 Watt converter has been built as a test vehicle for the chip (figure 8). Designed around a push pull, current mode controlled topology, the circuit runs from a 1.5 MHz clock. In the interest of simplicity, the ramp input and current limit pins were tied together underutilizing the available dynamic range of the Ramp pin by a factor of 3. A ground plane, judicious bypass capacitors and tight layout technique yielded a circuit that could be easily interrogated without significant noise interference problems.

In this simple application, the 3825 performs all the tasks required to regulate the 50 W power stage. The gate drive for the two power mosfets comes directly from the chip. Current loop slope compensation is resistively summed with the current sense signal at pin 7. Overall loop compensation is implemented with two resistors and a capacitor on the error amplifier. Taking advantage of the 1.5 MHz switching frequency and the wide bandwidth characteristics of the error amp, the control loop was compensated to zero dB at 300kHz.

CONCLUSION

Presenting an easy to use PWM architecture, the UC3825 possesses the necessary high speed characteristics to control switchers in the higher frequency ranges. This fills a void that has hindered high frequency applications in the past. A simple example running at 1.5 MHz points to a future of faster switching supplies.

USING AN INTEGRATED CONTROLLER IN THE DESIGN OF MAG-AMP OUTPUT REGULATORS

By
Robert A. Mammano, Unitrode IC Corp.
Charles E. Mullett, Mullet Associates, Inc.

Magnetic amplifier technology dates back considerably further than transistors but its wide-spread use has been slow in developing. While many factors may have been responsible for this, at least one — the high cost of tape-wound magnetic cores — has been alleviated with significant recent price reductions and the introduction of less expensive materials. And now, another one — the problems in designing effective control loops utilizing mag amps as voltage regulators — has fallen with the introduction of an IC dedicated to mag amp control — the UC1838.

While there are many types of power supply applications where mag amps may effectively be used, one of the most popular current uses is as a secondary regulator in multiple output power supplies configured as shown in Figure 1. The problem with multiple outputs stems from the fact that the open-loop output impedance of each winding, rectifier, and filter is not zero. Thus, if one assumes that the overall feedback loop holds the output of V_{01} constant, then increasing the loading on V_{01} will cause the other outputs to rise as the primary circuit compensates; similarly; increasing the loading on any of the other outputs will cause that output to droop as the feedback is not sensing those outputs. While these problems are minimized by closing the feedback loop on the highest power output, they aren't eliminated and auxiliary, or secondary regulators are the usual solution. A side benefit of secondary regulators, particularly as higher frequencies reduce the transformer turns, is to compensate for the fact that practical turns ratio may not match the ratio of output voltages. Clearly, adding any form of regulator in series with an output adds additional complexity and power loss. Mag amps are a hands down winner in both areas.

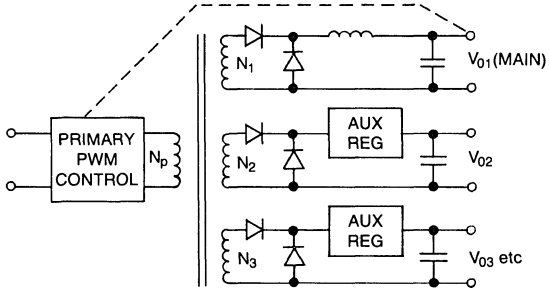

Figure 1. A typical multiple output power supply architecture with overall control from one output.

MAG AMP VOLTAGE REGULATORS

Although called a magnetic amplifier, this application really uses an inductive element as a controlled switch. A mag amp is a coil of wire wound on a core with a relatively square B-H characteristic. This gives the coil two operating modes: when unsaturated, the core causes the coil to act as a high inductance capable of supporting a large voltage with little or no current flow. When the core saturates, the impedance of the coil drops to near zero, allowing current to flow with negligible voltage drop. Thus a mag amp comes the closest yet to a true "ideal switch" with significant benefits to switching regulators.

Before discussing the details of mag amp design, there are a few overview statements to be made. First, this type of regulator is a pulse-width modulated down-switcher implemented with a magnetic switch rather than a transistor. It's a member of the buck regulator family and requires an output LC filter to convert its PWM output to DC. Instead of DC for an input, however, a mag amp works right off the rectangular waveform from the secondary winding of the power transformer. Its action is to delay the leading edge of this power pulse until the remainder of the pulse width is just that required to maintain the correct output voltage level. Like all buck regulators, it can only subtract from the incoming waveform, or, in other words, it can only lower the output voltage from what it would be with the regulator bypassed. As a leading-edge modulator, a mag amp is particularly beneficial in current mode regulated power supplied as it insures that no matter how the individual output loading varies, the maximum peak current, as seen in the primary, always occurs as the pulse is terminated.

MAG AMP OPERATION

Figure 2 shows a simplified schematic of a mag amp regulator and the corresponding waveforms. For this example, we will assume that N_S is a secondary winding driven from a square wave such that it provides a ± 10 volt waveform at v_i. At time $t = 0$, v_i switches negative. Since the mag amp, L1, had been saturated, it had been delivering $+10V$ to v_3 prior to $t = 0$ (ignoring diode drops). If we assume $v_c = -6V$, as defined by the control circuitry, when v_i goes to $-10V$, the mag amp now has four volts across it and reset current from v_c flows through D1 and the mag amp for the 10 μS that v_i is negative. This net four volts for 10 μS drives the mag amp core out of saturation and resets it by an amount equal to 40V-μS.

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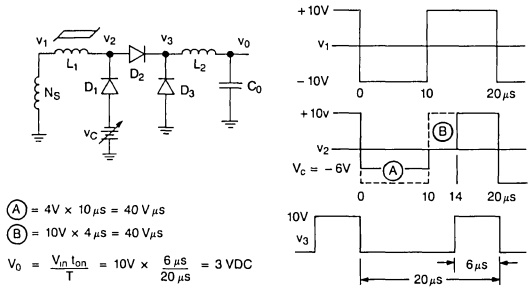

Figure 2. A simplified mag amp regulator and characteristic waveforms.

When t = 10 μS and v_1 switches back to +10V, the mag amp now acts as an inductor and prevents current from flowing, holding v_2 at 0V. This condition remains until the voltage across the core — now 10 volts — drives the core back into saturation. The important fact is that this takes the same 40 volt-μS that was put into the core during reset.

When the core saturates, its impedance drops to zero and v_1 is applied to v_2 delivering an output pulse but with the leading edge delayed by 4 μS.

Figure 3 shows the operation of the mag amp core as it switches from saturation (point 1) to reset (point 2) and back to saturation. The equations are given in cgs units as:

N = mag amp coil turns
Ae = core cross-section area, cm^2
ℓe = core magnetic path length, cm
B = flux density, gauss
H = magnetizing force, oersteads

The significance of a mag amp is that reset is determined by the core and number of turns and not by the load current. Thus a few milliamps can control many amps and the total power losses as a regulator are equal to the sum of the control energy, the core losses, and the winding I^2R loss — each term very close to zero relative to the output power.

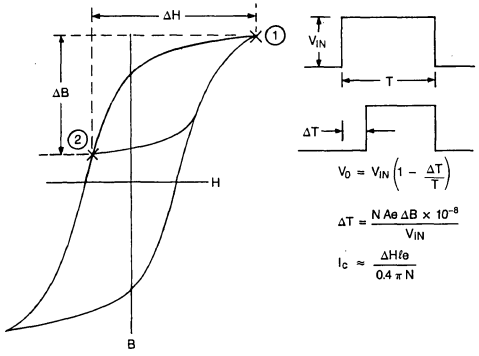

Figure 3. Operating on the B-H curve of the magnetic core.

Figure 4 shows how a mag amp interrelates in a two-output forward converter illustrating the contribution of each output to primary current. Also shown is the use of the UC1838 as the mag amp control element.

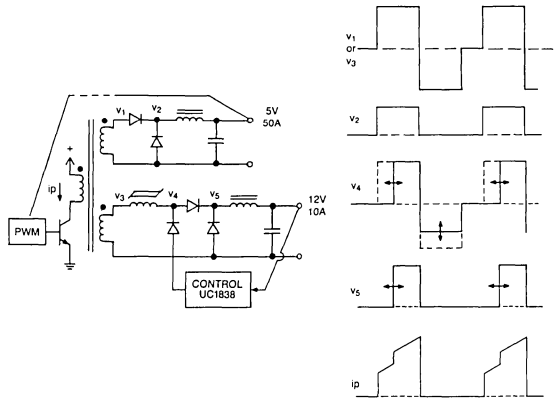

Figure 4. Control waveforms for a typical two-output, secondary regulated, forward converter.

THE UC1838 MAG AMP CONTROLLER

While bringing no major breakthroughs in either integrated circuit or power supply technology, the UC1838 provides a low-cost, easy-to-use, single-chip solution to mag amp control. The block diagrams of this device, as shown in Figure 5, includes three basic functions:

1. An independent, precise, 2.5V reference
2. Two identical, high-gain operational amplifiers
3. A high-voltage PNP reset current driver.

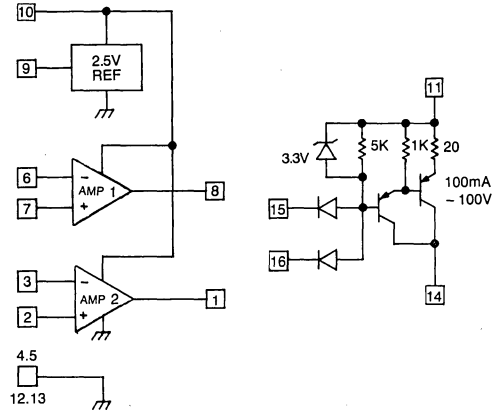

Figure 5. The block diagram of the UC1838 mag-amp control integrated circuit.

The reference is a common band-gap design, internally trimmed to 1%, and capable of operating with a supply voltage of 4.5 to 40 volts. The two op amps are identical with a structure as shown simplified in Figure 6. These amplifiers have PNP inputs for a common mode input range down to slightly below ground and have class A outputs with a 1.5 MA current sink pull down. The open loop voltage gain response, as shown in Figure 7, has a nominal 120 dB of gain at DC with a single pole roll-off to unity at 800 KHz. These amplifiers are unity-gain stable and have a slew rate of 0.3 V/μS.

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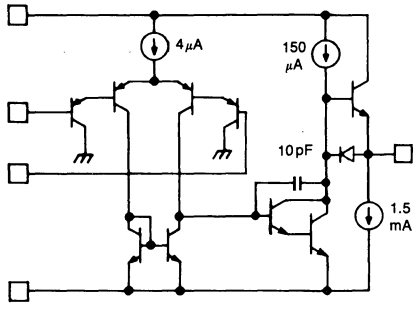

Figure 6. Simplified schematic of each of the operational amplifiers contained within the UC1838.

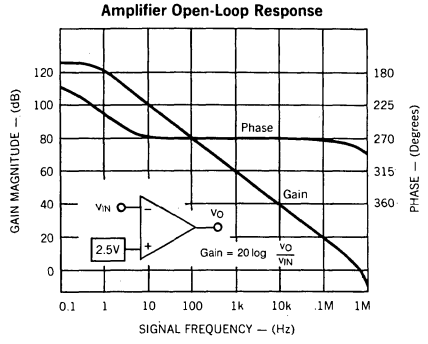

Figure 7. Open-loop gain and phase response for the UC1838 op amps.

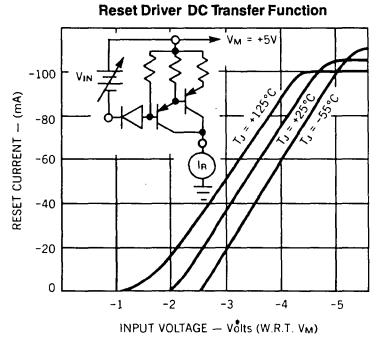

Figure 8. Transconductance characteristics of the UC1838 reset current generator.

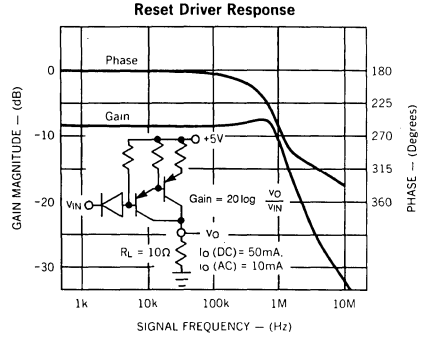

Figure 9. Reset driver frequency response.

Two op amps are included to provide several design options. For example, if one is used to close the voltage feedback loop, the other could be dedicated to some protective function such as current limiting or over-voltage shutdown. Alternatively, if greater loop gain is required, the two amplifiers could be cascaded.

The PNP output driver can deliver up to 100 MA of reset current with a collector voltage swing of as much as 80 volts negative (within the limits of package power dissipation). Remembering that the mag amp will block more volt-seconds with greater reset, pulling the input of the driver low will attempt to reduce the output voltage of the regulator. Thus, there are two inputs, diode "OR" ed to turn on the driver, turning off the supply output.

With internal emitter degeneration, this reset driver operates as a transconductance amplifier providing a reset current as a function of input voltage as shown in Figure 8. The frequency response of this circuit is plotted in Figure 9 showing flat performance out to one megahertz.

Current limiting to protect the output driver is achieved by means of the 3.5 V Zener clamp (which is temperature compensated to match two VBE's) in conjunction with the 20Ω emitter resistor. It should be noted that thermal shutdown is purposely not included since protecting the driver by turning it off would mean losing control of the power supply output. Pin 11 — the emitter of the driver — can be connected to any convenient voltage source from 5VDC to the level used to supply the op amps. Note that the op amp supply must be at least 2 volts higher than the DC level on the inputs, a point to remember when selecting a location for current sensing. One possible configuration for a complete secondary regulator with shutdown control is shown in Figure 10.

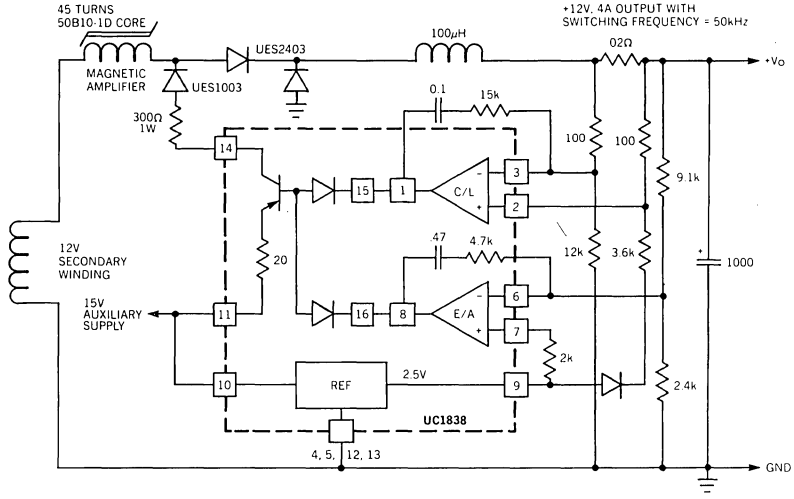

Figure 10. Using the UC1838 to provide both voltage control and over-current shutdown in a typical 12V, 4A regulator.

MAG AMP DESIGN PRINCIPLES

One of the first tasks in a mag amp design is the selection of a core material. Technology enhancements in the field of magnetic materials have given the designer many choices while at the same time, have reduced the costs of what might have been ruled out as too expensive in the past. A comparison of several possible materials is given in Figure 11. Some considerations affecting the choices could be:

1. A lower Bmax requires more turns — less important at higher frequencies since fewer turns are required.
2. Higher squareness ratios make better switches
3. Higher I_M requires more power from the control circuit
4. Ferrites are still the least expensive
5. Less is required of the mag amp if it only has to regulate and not shut down the output completely

MATERIALS

Example: Similar Toroids, 1" O.D., 0.75" I.D., 0.25" High, 25KHz, 20V.

Trade Name	Composition	Bmax (kG)	Core Loss @ Bmax	Squareness Ratio	Turns Req'd	I_M (A)
Sq. Permalloy 80	79% Ni, 17% Fe	7	1.2W	0.9	19	0.04
Supermalloy	78% Ni, 17% Fe, 5% Mo	7	1.0W	0.55	19	0.03
Orthonol	50% Ni 50% Fe	14	7.2W	0.97	10	0.39
Sq. Metglass	Fe, B	16	7.6W	0.5	9	0.06
Power Ferrites	Mn, Zn	4.7	1.8W	0.4	11	0.1
Sq. Ferrite (Fair-Rite #83)	Mn	3.9	2.8W	0.9	13	0.4

Figure 11. A comparison of several types of core materials available for mag amp usage.

In addition to selecting the core material, there are additional requirements to define, such as:

1. Regulator output voltage
2. Maximum output current
3. Input voltage waveform including limits for both voltage amplitude and pulse width
4. The maximum volt-seconds — called the "withstand area," Λ — which the mag amp will be expected to support

With these basic facts, a designer can proceed as follows:

1. Select wire size based on output current. 400 amp/cm² is a common design rule.
2. Determine core size based upon the area product:

$$AwAe = \frac{Ax \times \Lambda \times 10^8}{\Delta B \times K} \quad \text{where}$$

Aw = Window area, cm²
Ae = Effective core area, cm²
Ax = Wire area, (one conductor) cm²
Λ = Required withstand area, V-sec
ΔB = Flux excursion, gauss
K = Fill factors ≈ 0.1 to 0.3

3. Calculate number of turns from

$$N = \frac{\Lambda \times 10^8}{\Delta B \times Ae}$$

4. Estimate control current from

$$Ic \approx \frac{Hle}{0.4\,\pi\,N} \quad \text{where}$$

l_e = core path length, cm
H is taken from manufacturer's curves. Note that it increases with frequency.

5. Check the temperature rise by calculating the sum of the core loss and winding loss and using

$$\Delta T \approx \frac{P \text{ watts}^{0.8}}{A \text{ (surface) cm}^2} \times 444°C$$

6. Once the mag amp is defined, it can be used in the power supply to verify I_C and to determine the modulator gain so that the control requirements may be determined.

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COMPENSATING THE MAG AMP CONTROL LOOP

The mag amp output regulator is a buck-derived topology, and behaves exactly the same way with a simple exception. Its transfer function contains a delay function which results in additional phase delay which is proportional to frequency.

Figure 12 shows the entire regulator circuit, with the modulator, filter, and amplifier blocks identified. The amplifier, with its lead-lag network, is composed of the op-amp plus R1, R2, R3, C1, C2, and C3. The modulator, for the purpose of this discussion, includes the mag amp, the two rectifier diodes, plus the reset driver circuit which is composed of D1, Q1, and R7.

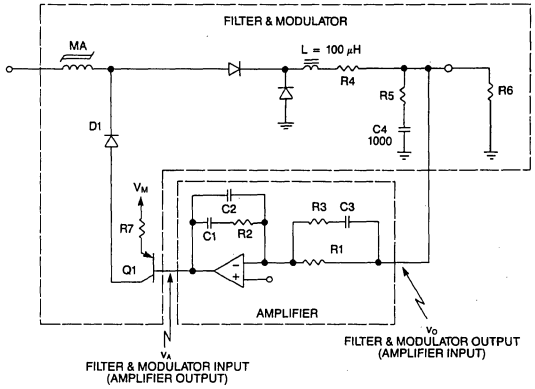

Figure 12. Schematic diagram of a typical regulator control loop.

The basic filter components are the output inductor (L) and filter capacitor (C4) and their parasitic resistances R4 and R5. For this discussion, a 20 KHz, 10 Volt, 10 Amp regulator is used. The output inductor has been chosen to be 100 μH, the capacitor is 1000 μF and each has .01 ohms of parasitic resistance. The load resistor (R6) of 1 ohm is included since it determines the damping of the filter.

The purpose of proper design of the control loop is to provide good regulation of the output voltage, not only from a dc standpoint, but in the transient case as well. This requires that the loop have adequate gain over as wide a bandwidth as practical, within reasonable economic constraints. These are the same objectives we find in all regulator designs, and the approach is also the same.

A straightforward method is to begin with the magnitude and phase response of the filter and modulator, usually by examining its Bode plot. Then we can choose a desired crossover frequency (the frequency at which the magnitude of the transfer function will cross unity gain), and design the amplifier network to provide adequate phase margin for stable operation.

Figure 13 shows a straight-line approximation of the filter response, ignoring parasitics. Note that the corner frequency is $1/(2\pi\sqrt{LC})$, or 316 Hz, and that the magnitude of the response "rolls off" at the slope of -40 dB per decade above the corner frequency. Note also that the phase lag asymptomatically approaches 180 degrees above the corner frequency.

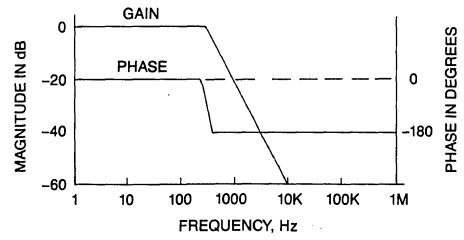

Figure 13. Output filter response.

To include the effects of the mag amp modulator, we must consider the additional phase shift inherent in its transfer function. This phase delay has two causes:

1. The output is produced after the reset is accomplished. We apply the reset during the "backswing" of the secondary voltage, and then the leading edge of the power pulse is delayed in accordance with the amount of reset which was applied.
2. The application of reset to the core is a function of the impedance of the reset circuit. In simple terms, the core has inductance during reset which, when combined with the impedance of the reset circuit, exhibits an L-R time constant. This contributes to a delay in the control function.

The sum of these two effects can be expressed as:

$$\varnothing m = -(2D + \alpha)\frac{\omega}{\omega_S}, \text{ where}$$

$\varnothing_M$ = Modulator phase shift
D = Duty ratio of the "off" time
α = resetting impedance factor: = 0 for a current source; = 1 when resetting from a low-impedance source; and somewhere in between for an imperfect current source.
ω_S = $2\pi f_S$, where f_S = the switching frequency.

When the unity-gain crossover frequency is placed at or above a significant fraction (10%) of the switching frequency, the resultant phase shift should not be neglected. Figure 14 illustrates this point. With α = 0, we insert no phase delay, and with α = 1 we insert maximum phase delay, which results from resetting from a voltage source (low impedance). The phase delay is minimized in the UC1838 by using a collector output to reset the mag amp.

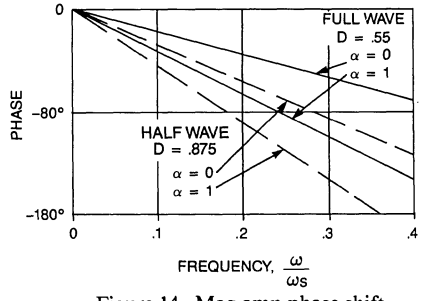

Figure 14. Mag amp phase shift.

It is difficult to include this delay function in the transfer function of the filter and modulator. A simple way to handle the problem is to calculate the Bode plot of the

filter/modulator transfer function without the delay function, and then modify the phase plot according to the modulator's phase shift.

Using this technique, the Bode plot for the modulator and output filter of this example has been calculated assuming α = 0.2 and D = 0.6 yielding the graph of Figure 15.

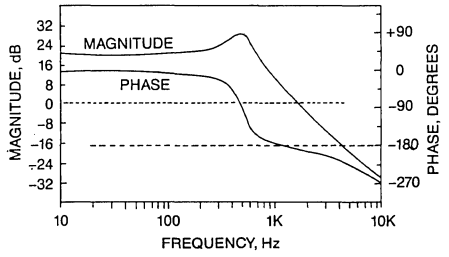

Figure 15. Filter-modulator response including the effects of mag amp phase delay.

If we now close the loop with an inverting error amplifier, introducing another 180 degrees of phase shift, and cross the unity gain axis above the corner frequency, we will have built an oscillator — unity gain and 360 degrees of phase shift.

An alternative, of course, is to close the loop in such a way as to cross the unity-gain axis at some frequency well below the corner frequency of the filter, before its phase lag has come into play. This is called "dominant pole" compensation. It will result in a stable system, but the transient response (the settling time after an abrupt change in the input or load) will be quite slow.

The amplifier network included in Figure 12 allows us to do a much better job, by adding a few inexpensive passive parts. It has the simplified response shown in Figure 16. The phase shift is shown without the lag of 180 degrees inherent in the inversion. This is a legitimate simplification, provided that we use an overall lag of 180 degrees (not 360 degrees) as our criterion for loop oscillation.

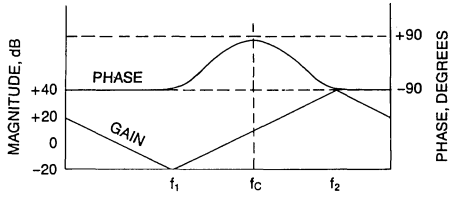

Figure 16. Compensated amplifier frequency and phase response.

The important point is that this circuit provides a phase "bump" — it can have nearly 90° of phase boost at a chosen frequency, if we provide enough separation between the corner frequencies, f1 and f2. This benefit is not free, however. As we ask for more boost (by increasing the separation between f1 and f2) we demand more gain-bandwidth of the amplifier.

DESIGN EXAMPLE

An 8V, 8A Output Derived from a 12V Output — 20 KHz Push-Pull Converter

This example uses the UC1838 to control a full-wave mag amp output regulator, with independent shutdown current limiting. Capsule specifications are as follows:

INPUT: PWM quasi-square wave which, without the magamp, produces 12 Vdc.

OUTPUT: 8.0 Vdc ±1% at load currents from 1 to 8A.

OUTPUT RIPPLE: Less than 50 mV p-p.

TRANSIENT RESPONSE: For load changes of 6 to 8 and 8 to 6A, peak excursion of the output shall be less than ±2% and settle to within 1% of the final value within 500 μS.

OUTPUT PROTECTION: The 8V output shall have independent current limiting, so as not to shut down the 12V output when the 8V output is overloaded or short-circuited. It shall recover from the overload automatically when the overload is removed.

Figure 17 shows the proposed circuit approach. A current transformer has been used to sense the overload, simply to illustrate this approach. A simple series resistor of perhaps .01 or .02 ohms would do as well here, but the current transformer is preferred for high-current outputs.

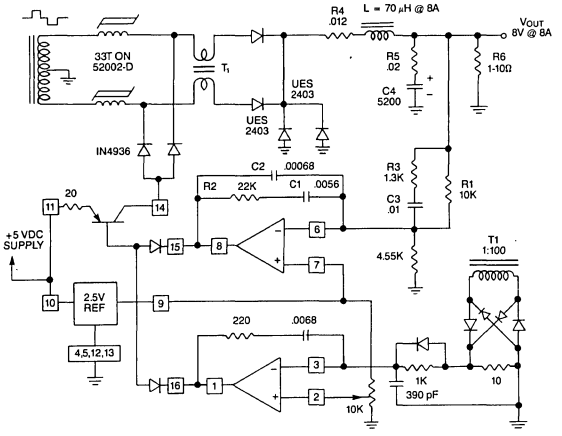

Figure 17. Control and current limiting for a 8V, 8 amp, 20 KHz push-pull converter.

DESIGN APPROACH

With the input waveform already set by the converter design, and the above specifications to define the desired output, the new output circuit will be approached as follows:

1. Draw the preliminary schematic.
2. Design the mag amp.
3. Design the feedback loop.
4. Design the current limiter.
5. Build the breadboard and test it.

PRELIMINARY SCHEMATIC

Figure 17 shows the preliminary circuit diagram. Parasitic resistance of the output filter inductor and capacitor (R4 and R5) are shown, along with the expected feedback com-

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pensation elements (R1, R2, R3, C1, C2, and C3). These will be referenced in the mag amp design.

MAG AMP DESIGN

The information necessary to the design is as follows:

1. Input pulse: nominally 32V × 9 μS, = 288 volt-microseconds.
2. Duty ratio of the "off" time: nominally (25 - 9 μS)/ 25 μS = .76, since the frequency at the output is 40 KHz.
3. Output current: 8A.
4. Regulation only, or complete shutdown required? Shutdown.

Comments on the output filter

Design of the output filter is not complicated by the presence of the mag amp. In this case, it was designed with output ripple specs, and capacitor ripple current in mind. Although this design has adequate inductance for continuous conduction of the inductor at minimum load, this is not mandatory. The mag amp, when designed for shutdown, is capable of regulating the output in the discontinuous conduction mode.

Mag amp core selection

1. Wire size: The current waveform in the magamp can be analyzed as follows: During the power pulse, the current is approximately 8A (inaccurate only due to the "tilt" of the top of the current pulse); the duty ratio of this pulse is half the ratio of the output voltage to the pulse height, or .5 × 8/30 = .12. During the dead time between pulses, the inductor current is shared by the rectifier diodes and the "catch" diode. The duty ratio is 1 - 2 × .12 = .76, and the current during this interval is 8/3A. During the remaining interval the current is zero, because the entire 8A is flowing in the other mag amp.

   The rms value of the current can now be computed:

   $$\text{Irms} = \sqrt{8^2 \times .12 + (8/3)^2 \times .76} = 3.62 \text{ A}.$$

   At 400 Amp/cm², a wire area of approx. .0091 cm² is required. 16 gauge wire has an area of .0131 and is chosen for the mag amp.
2. Core selection: An appropriate material at this frequency is square-loop 80% nickel (Square Permalloy 80 or eq.) with a tape thickness of 1 mil. The saturation flux density if this material is 7000 gauss. A fill factor of 0.2 is chosen for the winding. The required area product is:

   $$\text{AwAe} = \frac{\text{Ax} \times \Lambda \times 10^8}{\Delta B \times K} = \frac{.0131 \times 288 \times 10^{-6} \times 10^8}{2 \times 7000 \times 0.2} = .135 \text{ cm}^4$$

   which can be divided by 5.07 × 10^{-6} cm²/C.M. in order to refer to core manufacturer's tables.

   An appropriate core is the Magnetics 52002-10, which (with 1 mil tape thickness) has an area product of .026 × 10^6 C.M. cm². The core area of this core is 0.076 cm².
3. Determine the number of turns: The mag amp must be able to withstand the entire area of the input pulse, which is 288 volt-microseconds.

   $$N = \frac{\Lambda \times 10^8}{2 \times Bm \times Ac} = \frac{288 \times 10^{-6} \times 10^8}{2 \times 7000 \times .076} = 27 \text{ turns}.$$

   Allowing an extra 20% for variations in Bm, pulse dimensions, etc., the winding is chosen to be 33 turns.

FEEDBACK LOOP DESIGN

The key steps in the design of the feedback loop are as follows:

1. Determine the modulator's dc transfer function.
2. Plot the transfer function of the modulator and filter, to determine the gain and phase boost required of the feedback amplifier.
3. Design the feedback amplifier.
4. Plot the results in the form of the closed-loop transfer function.

Plotting the modulator's transfer function can be easily done experimentally with the UC1838 by opening the feedback loop at the input to the Reset Driver and driving this point (pin 15 or 16) directly. For interest, the reset current is also measured with the help of a 1 ohm resistor placed in series with the emitter of the reset transistor (pin 11 of the UC1838). The results are shown in Figure 18, with load resistors of 1 ohm and 10 ohms.

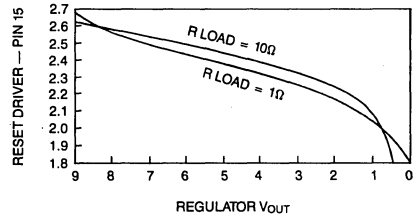

Figure 18. DC gain of the mag amp modulator.

Note that the results are practically the same at both load values. This is to be expected, since the output inductor is still in the continuous conduction mode at the minimum load.

In the region of the desired output (8V and 8A load), the modulator dc gain is approximately 12.5, or 22 dB. In addition to the phase shift of the filter, the modulator contributes additional phase lag. Assuming that we will not attempt to cross unity-gain at a frequency above one-tenth the switching frequency, we can neglect the phase lag due to the impedance of the core and the reset circuit. But we cannot neglect the phase lag resulting from the delay between the time of resetting the core and the time when the core delivers its output:

$$\varnothing_M = 2D \frac{\omega}{\omega_S}, \text{ where}$$

$\varnothing_M$ = Modulator phase shift
D = Duty ratio of the "off" time (.76 in this example)
ω_S = 2 D f_a, where f_a = the switching frequency (40 KHz)

We can use any one of the common circuit analysis programs for analyzing the filter-modulator, neglecting the modulator phase lag when running the program, and then adding it later. Or, the lag may be included in a more sophisticated analysis program. The resultant response prediction is shown in Figure 19.

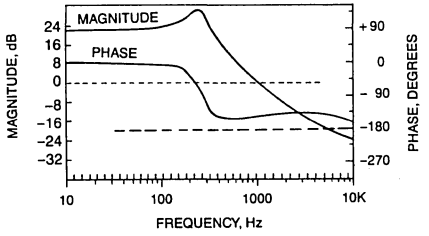

Figure 19. Calculated response plot for the modulator and filter.

Note the shape of the phase response. In the region of 2 KHz the phase lag is decreasing, due to the ESR of the output capacitor. Above 6 KHz the modulator's phase lag becomes important, and the phase lag increases.

Choosing one-tenth the switching frequency for the unity-gain crossover frequency (4 KHz), we can determine the desired gain and phase boost of the feedback amplifier. At 4 KHz, the gain of the modulator is -15 dB (a factor of .179) and the phase shift is -135 degrees. It is generally recommended that there be at least 60 degrees of phase margin at the crossover frequency. This will require reduction of the phase lag to -120 degrees.

In accordance with the design procedure of Venable[2], the required boost is:

Bc = M - P - 90, where

M = desired phase margin, and P = filter & modulator phase shift.

In this case, Bc = 60 - (-135) -90 = 105 degrees. This is comfortably within the theoretical limit of 180 degrees, inherent in the amplifier configuration shown in Figure 17. The gain required at the crossover frequency is the reciprocal of the modulator's gain, or +15dB = a gain of 5.6.

Continuing with the procedure, we can now compute the amplifier components:

$K = (\text{Tan}\ [\ (Bc/4) + 45]\ )^2 = 8.65$

$C2 = 1/(2\ \pi\ f\ G\ R1) = .00071\ \mu F$

$C1 = C2\ (K - 1) = .0055\ \mu F$

$R2 = \sqrt{K}/(2\ \pi\ f\ C1) = 21{,}485$ ohms

$R3 = R1/(K - 1) = 1{,}302$ ohms

$C3 = 1/(2\ \pi\ f\ \sqrt{K}\ R3) = .01\ \mu F$

where f = crossover frequency in Hz, G = amplifier gain at crossover (expressed as a ratio, not as dB), and K is a factor which describes the required separation of double poles and zeroes to accomplish the desired phase boost. These frequencies are:

$f1 = f/\sqrt{K}$ (double zero), and $f2 = f\sqrt{K}$ (double pole),

In this example, f1 = 1361 Hz and f2 = 11.76 KHz. With this information at hand, it is wise to check the gain-bandwidth required of the feedback amplifier to see that the circuit's needs can be met with one of the amplifers in the UC1838. Knowing that the amplifier rolloff is 20 dB per decade, we can simply calculate the required gain-bandwidth at f2 and see that it is well below the gain-bandwidth of the amplifier.

The gain at f2 is:

$Gf_2 = \sqrt{K}\ G$, and hence the required gain-bandwidth is:

$GBW = \sqrt{K}\ G\ f2 = K\ G\ f$, where G is the desired gain at crossover.

In this example, GBW = 8.65 × 5.6 × 4000 = 194 KHz. This is comfortably below the gain-bandwidth of the amplifier, which is 800 KHz.

For interest, the response of the amplifier is plotted in Figure 20. Note that the gain reaches a minimum at 1.3 KHz, and that the phase boost peaks at 4 KHz, as intended.

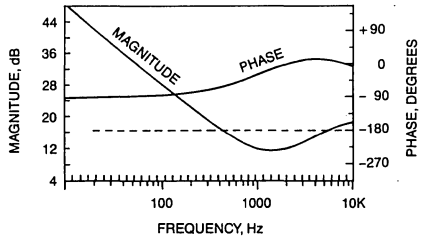

Figure 20. Compensated amplifier response.

Figure 21 shows the overall response, combining the filter-modulator's response with that of the feedback amplifier. Note the 60 degrees of phase margin at the crossover frequency.

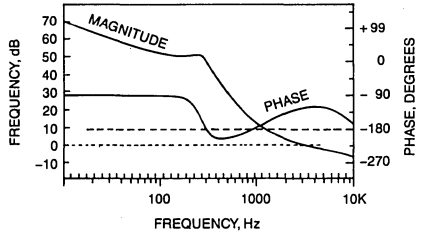

Figure 21. Total loop response with 60 degrees of phase margin at crossover.

CURRENT LIMITER DESIGN

Although a series sensing resistor might have been acceptable at this level of output current, a current transformer, T1 in Figure 17, has been used for the sake of interest. The secondary has 100 turns, and each primary winding is simply one pass through the toroid.

The amplifier performs as an integrator rather than as a comparator, the form found in many primary current limiters of switched-mode controllers. This is not an arbitrary choice. Since the current pulse occurs during the time that the core is obviously not being reset, the circuit must have "memory" — it must apply a shutdown command to the reset transistor during the next reset interval. Although many sophisticated schemes can be devised, the integrator is attractive because of its simplicity.

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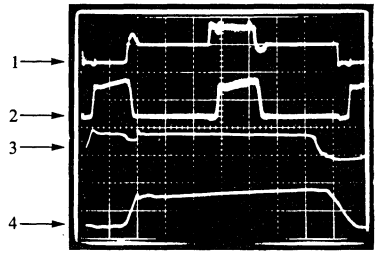
A diode is placed across the input resistor of the integrator, to force its output down quickly when receiving the narrow pulses which occur when the circuit is in current limit. The circuit of this example was developed experimentally. A future goal is to explore this in detail and develop a more rigorous approach. The performance of this circuit is illustrated with waveform photos later in the paper.

BREADBOARD TEST RESULTS

Figure 22 shows the waveform of the input voltage which is applied to the mag amp core, and the current of the two mag amps combined (by placing a current probe on the return leg of the secondary of the converter's transformer). The lower two traces are expanded versions of the top ones, and one can see clearly the effect of the transformer's leakage inductance: the voltage pulse has a "dent" in it during the rise of the current in the mag amp.

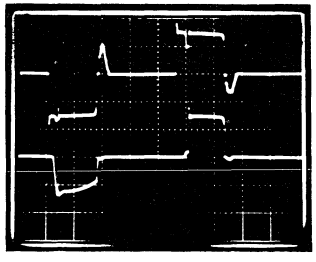


1. Secondary voltage, 50V, 5 μs/div.
2. Current in return (center tap) of secondary. 5A, 5 μs/div.
3. Secondary voltage, 50V, 1 μs/div.
4. Current in return (center tap) of secondary. 5A, 5 μs/div.

Figure 22. Input voltage and current to the mag amp.

Also note the "backswing" at the end of each voltage pulse. This is the discharge of the energy stored in the saturated inductance of the mag amp core. Finally, note the rate of rise of the current pulse, which is determined by the saturated inductance of the mag amp, in series with the leakage inductance of the transformer.

Figure 23 illustrates the operation of the mag amp in more detail. The upper trace is the input voltage of the mag amp, and the lower trace is its output. The reset volt-second product is the difference between the negative pulses of the two traces. The shape of the negative pulse in the lower trace is due to the changing impedance of the mag amp core during reset.

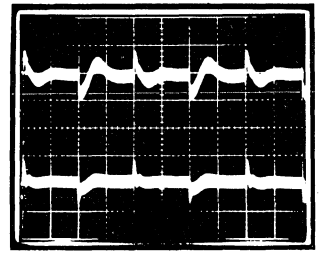


Top: Secondary voltage (into mag amp), 20V × 5 μs/div.
Bot: V_{OUT} of mag amp, 20V × 5 μs/div.

Figure 23. Mag amp operation.

Control loop transient response

To test the response of the regulator to step changes in load, an electronic load was square-wave modulated at 500 Hz, between the values of 6A and 8A. The results are shown in Figure 24. The upper trace is the regulator's output voltage, showing peak excursions of less than 50 mV, and recovery time of .5 ms. The lower trace is the reset current, measured with a current probe at the collector of the reset transistor in the IC.

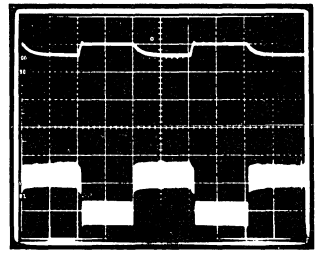


Output transient response 6-8A ΔI_{LOAD}
Top: Output voltage, 50mV × .5 ms/div.
Bot: Reset current, 20mA × .5 ms/div.
(Measured at collector of UC1838 transistor)

Figure 24. Dynamic regulator response to step change in load between 6 and 8 amps.

Response of the current limiter

To illustrate the dynamic operation of the limiter, the current limit was set at 7A, and then the electronic load was modulated between 5.7A and 8.7A at a rate of approximately 25 Hz. Figure 25 shows the output voltage in the top trace. The lower trace is the current in the output inductor. Note that the output voltage is well-behaved and that there is no overshoot of the inductor current.



Top: V_{OUT}, 2V × 20 ms/div.
Bot: Inductor current, 2A × 20 ms/div.

Figure 25. Response of current limiter with load switched between 5.7 and 8.5A; with current limit set at 7.5A.

Finally, Figure 26 shows the operation of the current-limiting amplifier. The upper trace is the inductor current, and the lower trace is the output voltage of the current-detecting amplifier. Note the output waveform of the amplifier. Although the amplifier performs as an integrator, it slews fast enough to keep up with the rate of rise of the inductor current, thus adequately protecting the converter and output rectifiers.

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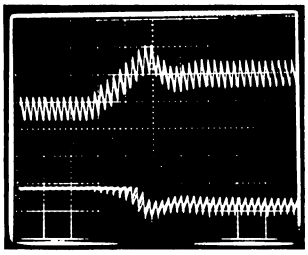

Top: Inductor current, 2A × .1 ms/div.
Bot: V_{OUT} of C.L. amp (pin 1), 2V × .1 ms/div.

Figure 26. Response time of current limit amplifier.

APPLICATIONS AT HIGHER SWITCHING FREQUENCIES

As mag amp output regulators are applied at higher and higher switching frequencies, the second-order effects, of course, become more significant.[3] Leakage inductance of the transformer and saturated inductance of the mag amp rob the circuit of its control range, since these produce additional dead time at the leading edge of the output pulse. Even without the mag amp output regulator, this can be a problem in high-frequency switched-mode converters.

Diode storage time has the same result. If the output side of the mag amp "sticks" at ground (during reverse recovery of the rectifier) while its input voltage swings negative, some unwanted reset will be applied to the mag amp. There are techniques to deal with this problem, by providing a shunt recovery path around the mag amp to remove the stored charge in the diode.[4]

The control circuit of the mag amp regulator is not involved in the cycle-by-cycle operation of the circuit; hence, the control IC is not a major barrier to raising the operating frequency. It does affect the situation in an indirect way, however. Its gain-bandwidth may limit the speed of transient response such that the loop crossover frequency cannot be raised in proportion to the switching frequency. In most applications this will not be objectionable. If it is, an outboard op amp can provide the additional gain-bandwidth. If the regulator is not required to have its own current limiter, then the second amplifier can be used in cascade with the first, to provide additional gain-bandwidth.

The integration of the circuit blocks required to implement mag amp output regulators is an important contribution. It is especially beneficial to have the reset transistor included, as this can even eliminate a small heat sink. Finally, it is helpful not only in the design process but also in production to have a single component which encompasses all of the active control functions. As more and more designers are working with the same component, the development of the technology will be more focused, and this will be universally beneficial.

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3. C. E. Mullett, "Performance of Amorphous Materials in High-Frequency Saturable Reactor Output Regulators," Proceedings of the First International High Frequency Power Conversion Conference, May, 1986, pp. 121-132.
4. C. E. Mullett and R. Hiramatsu, "An Improved Parallel Control Circuit for Saturable Reactor Output Regulators in High-Frequency Switched-Mode Converters," Proceedings of The IEEE Applied Power Electronics Conference and Exposition, April, 1986, pp. 99-106.
5. Unitrode IC Corp. acknowledges and appreciates the support and guidance given by the Power Systems Group of the NCR Corporation, Lake Mary, FL in the development of the UC1838.

1.5 MHZ CURRENT MODE IC CONTROLLED 50 WATT POWER SUPPLY

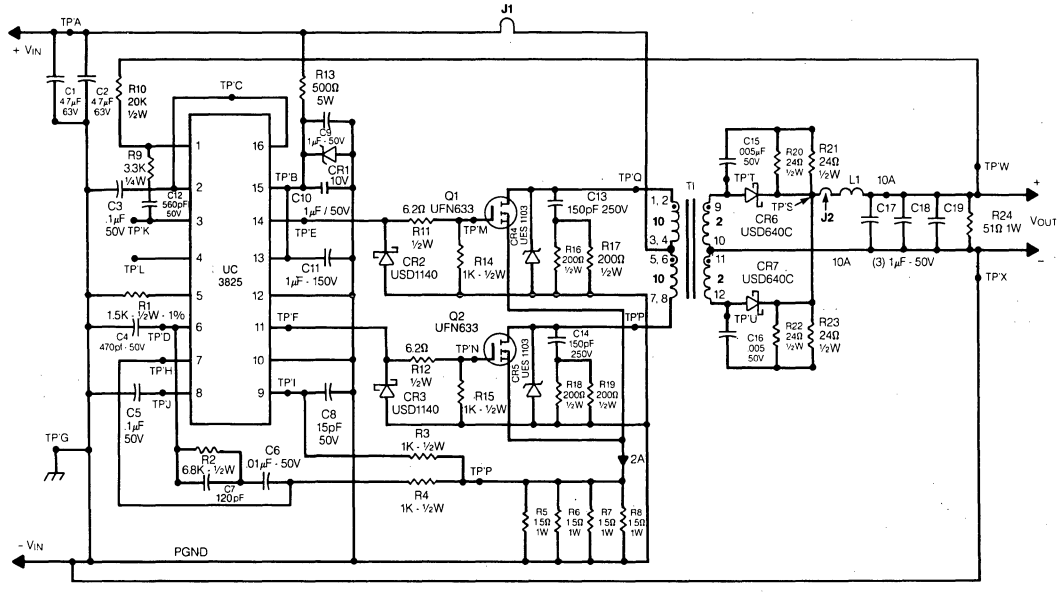
Abstract

This application note highlights the development of a 1.5 megahertz current mode IC controlled, 50 watt power supply. Push-pull topology is utilized for this DC to DC converter application of +48 volts input to +5 volts at 10 amps output. The beneficial increase in switching speed and dynamic performance is made possible by a new pulse width modulator, the Unitrode UC3825. Reductions in magnetic component sizes are realized and the selections of core geometry, ferrite material and flux density are discussed. The effects of power losses throughout the circuit on overall efficiency are also analyzed.

Introduction

The switching frequencies of power supplies have been steadily increasing since the advent of cost effective MOSFETS, used to replace the conventional bipolar devices. While the transition time in going from twenty to hundreds of kilohertz has been brief, few designers have ventured into, or beyond, the one megahertz benchmark. Until recently, those who have, had utilized discrete pulse width modulation designs due to the absence of an integrated circuit truely built for high speed. The 1.5 MHZ power supply shown schematically in figure 1 was designed to exemplify high frequency power conversion under the supervision of such an IC controller, the UC3825.[1]

Figure 1. Schematic Diagram



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II. POWER SUPPLY SPECIFICATIONS

Input Voltage Range:	42 to 56 VDC
Switching Frequency:	1.5 MHz
Output Power:	51 Watts Max.
Output Voltage:	5.1 VDC Nom.
Output Current:	2–10 ADC
Line Regulation:	5 MV
Load Regulation:	15 MV
Output Ripple:	100 MV Typ.
Efficiency:	75% Typ.

III. OPERATING PRINCIPLES

Power can efficiently be converted using any of several standard topologies. Design tradeoffs of cost, size and performance will generally narrow the field to one that is most appropriate. For this demonstration application, the center-tapped push-pull configuration has been selected.

Current mode control provides numerous advantages over conventional duty cycle control, and has been implemented as the regulation method. In review, the error amplifier output (outer control loop) defines the level at which the primary current

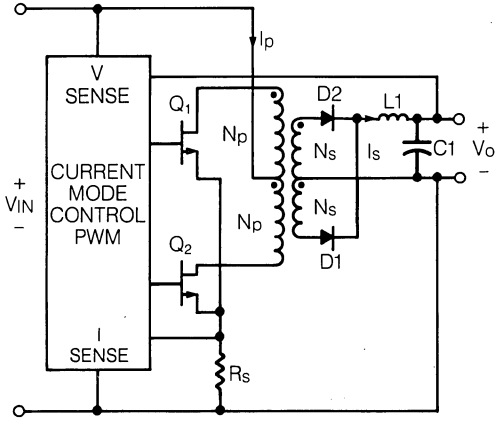

Figure 2. Basic Diagram — Push-Pull Converter Using Current Mode Control

(inner loop) will regulate the pulse width, and output voltage. Pulse-by-pulse symmetry correction (flux balancing) is inherent to current mode controllers, and essential for the push-pull topology to prevent core saturation.

A basic current mode controlled, mosfet switched push-pull converter is shown in figure 2. Transistor Q1 is turned on by a drive pulse from the PWM, causing primary current I_p to flow through the transformer primary, mosfet Q1 and sense resistor R_S. Simultaneously, diode D1 conducts current $I_p \times N_P/N_S$ in the secondary, storing energy in inductor L1 and delivering power to the output load. When Q1 receives a turn-off pulse from the PWM, it halts the current flow in the primary. Secondary current continues due to the filter inductor L1. Diodes D1 and D2 each conduct one-half the DC output current during these converter "off" times. This entire process is repeated on alternate cycles, as Q2 next is toggled on and off. The basic waveforms are shown in figure 3 for reference.

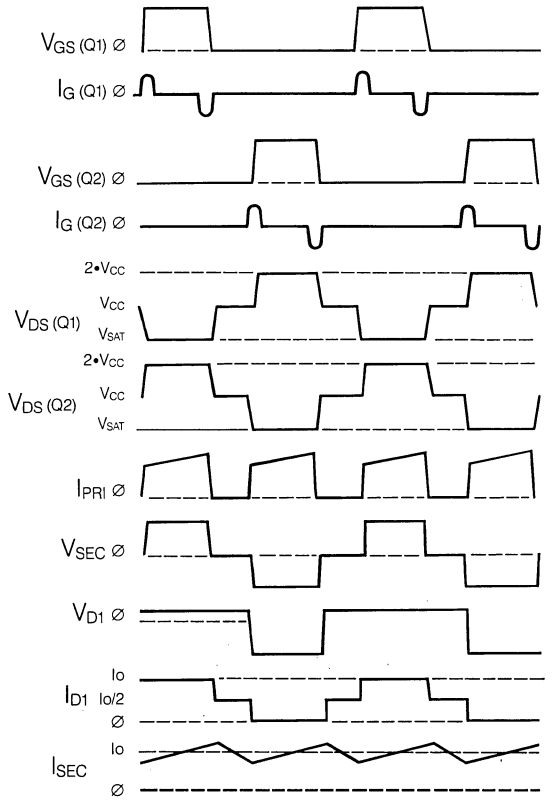

Figure 3. Basic Push-Pull Waveforms

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IV. DESIGN CONSIDERATIONS

Auxiliary Supply Voltage

The 9.2 volt minimum requirement of the UC3825 and 20 volt gate-source maximum of the mosfets imply an approximate 10 thru 18 volt range of inputs. The 10 volt value was selected to supply both V_{CC} and V_C (totem pole outputs) while keeping power dissipation in the IC low. The circuit used is a simple resistor-zener dissipative network with ample bypassing capacitors located near the IC to reduce noise.

Oscillator Frequency

The oscillator frequency selected is 1.5 MHz, resulting in a 670 nanosecond period. From the UC3825 data sheet, oscillator frequency versus R_t, C_t, and deadtime curves:

F_o = 1.5 mHz; T period = 670 ns
C_t = 470 pF
R_t = 1.5 K

Therefore; T (on) = 570 ns (max)
T (off) = 100 ns (min)

$$\text{DUTY CYCLE, d max} = \frac{\text{T (on) max}}{\text{T (period)}} = \frac{570\text{ ns}}{670\text{ ns}} = 85\%$$

NOTE: These times will determine the mosfet device selection and transformer turns ratio.

Preliminary Considerations

Prior to designing the main transformer, several parameters need to be defined and determined. Standard design procedures and for this "first cut" approximation.

Input Power

$$\text{Input power, P (in)} = \frac{\text{Output power, P (out)}}{\text{Efficiency, n}}$$

Let n = 75% for a 5 v, single output power supply.

$$\text{P (in)} = \frac{5.1\text{ v} \cdot 10\text{ a}}{0.75} = \frac{51\text{ watts}}{0.75} = 68\text{ watts}$$

Primary Current

The primary current can be approximated using the low-line constraints of 42 volts DC input:

$$\text{Primary Current (dc)} = \frac{\text{Input power P (in)}}{\text{Input voltage V (in)}} = \frac{68\text{ watts}}{42\text{ volts}} = 1.62\text{ A}$$

The primary current during the transistor on time is:

$$\text{I (p)} = \frac{\text{I (dc)}}{\text{d (max)}} = \frac{1.62\text{ A}}{0.85} = 1.9\text{ amps, or approx. 2A}$$

The RMS primary current is:

$$\text{Ip (rms)} = \frac{(\text{Ip})^2 \cdot \text{Duty (max)}}{2} = 1.24\text{A (rms)}$$

Sense Resistor R (s)

Primary current is sensed and controlled in a current mode controller by first developing a voltage proportional to the primary current, used as an input to UC3825. This is accomplished by sense resistor R (s) with a calculated value of the I limit threshold value divided by the primary current at the desired current limit point, typically 120% I (max).

$$\text{R (s)} \leq \frac{\text{V th (pin 9)}}{120\% \cdot \text{I (pri)}} = \frac{1\text{ volt}}{1.2 \cdot 2\text{ amps}} = 0.42\text{ ohm}$$

Mosfet DC Losses

A high quality mosfet is used to keep both DC and switching losses low, with an R (ds) on max of 0.8 ohms. Calculation of the voltage drops across the device are required for the transformer design.

V ds (on) = Rds (max) • I (p) = 0.8 • 2 = 1.6 v

During an overload; V ds (max) = 0.8 • 2 • 1.20 = 1.92 v (2 v)

P dc = I dc² Rds max • duty
= 2² • 0.8 • 0.85/2 = 1.35 watts

Selection of Core Material

Few manufacturers provide core loss curves for frequencies above 500 khz. To minimize power dissipation in the core, the flux density must be drastically reduced in comparison to the 20 –150 khz versions. Typical operation is at a total flux density swing, delta B, of 0.030 Tesla (300 Gauss) while approaching the 1 megahertz region. TDK's H7C4 material was selected for it's low loss, high frequency characteristics.

Main Transformer Design

The first step in transformer design is to determine the preliminary turns ratio. Once obtained, the minimum cross-sectional area core (Ae) can be calculated, and core selection made possible.

Calculation of Transformer Voltages and Turns Ratio

V pri (min) = V in (min) – V xtor (max) – V (Rs) max
V p (min) = 42 v – 2.0 v – 1 v
= 39.0 v

V sec (min) = V out (max) + V diode (max)
+ V choke (dc) + V (losses)
V sec (min) = 5.1 + 0.65 + 0.1 + 0.05 (est) = 5.9 v

$$\text{Turns ratio N} = \frac{\text{V pri (min) Duty (max)}}{\text{V sec (min)}} = \frac{39.0 \cdot 0.85}{5.9} = 5.6{:}1$$

The secondary is designed for excellent coupling using copper foil, and the primary has been rounded to the nearest lower turns.

Turns ratio: N = N pri / N sec = 5:1

The actual number of both primary and secondary turns will be determined by the ferrite core characteristics as a function of operating frequency and Gauss level.

Minimum Core Size

The minimum cross-sectional area core that can be used is calculated with the following equation for core loss limited applications.

$$Ac\ (min) = \frac{V\ (pri)\ min \cdot Duty\ (max) \cdot 10^4}{2 \cdot Freq. \cdot N\ (p) \cdot \Delta B\ (Tesla)}\ (cm^2)$$

At first it would seem that the core area required for this 1.5 MHZ switcher would be ten times smaller than that of a 150 KHZ version. This would be true if the flux density, number of turns and core losses remained constant. However, losses are a function of both frequency and frequency squared[2] and as it increases, the flux density swing (ΔB) must be drastically reduced to provide a similar core loss, hence temperature rise. In this example, an acceptable figure was selected of one percent of the total output power, or one-half watt. Empirically, this translates to a temperature rise of 25°C, at 325 Gauss (0.0325 Tesla) for cores with a cross-sectional area of 0.70 sq. cm, a ballpark estimate of the true core size.

This formula can be rewritten as:

$$Ac \cdot Np = \frac{V\ pri \cdot D\ max \cdot 10^4}{2 \cdot F \cdot \Delta B}$$

This is a more convenient formula because the right hand side of the equation contains all constants. Input voltage, frequency of operation and flux density have already been determined. The selection of core size (cross-sectional area) is inversely proportional to the number of primary turns, and vice-versa. Based on the five-to-one turns ratio, an original assumption of five turns for the primary would result in a large core size for this 50 watt application. Alternatively, a ten turn primary is used to minimize core size.

Substituting previous values for high line operation at 0.0325 Tesla (325 Gauss) and a magnetic operating frequency of 750 kHz:

$$Ac\ (min) = \frac{39 \cdot 0.85 \cdot 10^4}{2 \cdot 750{,}000 \cdot 10 \cdot 0.0325} = 0.68\ cm^2$$

Core Loss Limited Conditions

As the switching frequencies are increased, generally a reduction of core size or minimum number of turns is realized. This is true, however, but only to the point at which the increasing core losses prevent a further reduction of either size or minimum turns. This crossover point occurs at different frequencies for each individual ferrite material based upon their losses and acceptable circuit losses, or temperature rise[3]

Core Geometry Selection

A variety of standard core shapes are available in the cross-sectional area range of 0.62 to 0.84 cm^2. Considerations of safety agency spacing requirements, physical dimensions, window area and relative cost of assembly must be evaluated.

Core Style	Description	AC (cm^2)	Weight (g)
PQ	PQ 20/20	0.62	15
POT CORE	P 22/13	0.63	13
LP	LP 22/13	0.68	21
TOROID	T 28/13	0.76	26
EE	EE 35/28	0.78	28

The LP 22/13 style was selected to easily terminate (breakout) the high current output windings. For a given cross-sectional area, it occupies less PC board space, and has good shielding characteristics.

Wire Size Selection

The single, most difficult task in high frequency magnetic design is to minimize the eddy current losses, or skin effects while optimizing wire sizes. Penetration depth refers to the thickness (or depth) into a copper conductor in which a wave will penetrate for a specific frequency. For copper at 100°C:

$$d\ pen = 7.5 / (frequency^{0.5})\ (cm)$$

At 750 kHz, this corresponds to $8.66 \cdot 10^3$ cm, or about the thickness of an AWG #39 wire. Larger size wire can be used, however the AC current flows only in the depth penetrated at the switching frequency. Consult the UNITRODE DESIGN SEMINAR SEM-400 book, appendix M2 for additional information on this subject.

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For low current windings, several strands of thin wire can be paralleled, or twisted together forming a "bundle." Seven wires twisted around each other closely approximate a round conductor with a net diameter of three times the individual wire diameter. This twisting is commonly done at 10-12 turns per foot, and significantly reduces parasitics between wires at high frequencies.

Medium to high current windings require the use of Litz wire, a similar bundle of numerous conductors. Copper foil is also an excellent choice.

Industry practice is to operate at 450 amps (RMS) per centimeter squared, or $2.22 \cdot 10^{-3}$ cm²/A. This applies to windings operating at an acceptable temperature rise.

Area required = I rms / 450A / cm²

Primary area (Axp) = 1.24A / 450A / cm² = $2.75 \cdot 10^{-3}$ cm²

Calculate Secondary RMS Current.

$$\text{I rms (sec)} = \frac{\text{I sec}^2\,(\text{duty on}) + \frac{\text{I sec}^2\,(2 \cdot \text{duty off})}{2}}{2}$$

$$\text{I rms (sec)} = \frac{10^2\,(.425) + \frac{5^2\,(2 \cdot .075)}{2}}{2}$$

I rms (sec) = 4.81A

Secondary Area (Axs) = 4.81A / 450A / cm²
= $1.07 \cdot 10^{-2}$ cm²

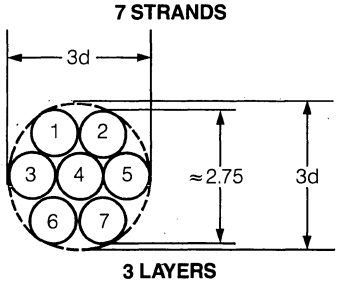

Figure 4.

For a given bundle of 7 conductors, the cross-sectional area of each conductor equals:

$$\frac{\text{Required area}}{\text{\# conductors}} = \frac{\text{Axp}}{7} = \frac{2.75 \cdot 10^{-3}}{7} = 3.93 \cdot 10^{-4}\ \text{cm}^2$$

The cross-sectional area of an AWG #36 wire is $1.32 \cdot 10^{-4}$, therefore, three bundles of seven conductors each should be used. Two bundles were utilized as a compromise between practical winding considerations and acceptable eddy current losses.

Copper foil is used for the secondary, with a required width slightly less than the bobbin width, and thickness determined by:

$$\frac{\text{Secondary area (Axs)}}{\text{Bobbin width}} = \frac{1.07 \cdot 10^{-2}\ \text{cm}}{1.40\ \text{cm}} = 7.64 \cdot 10^{-3}\ \text{cm}$$

This corresponds to 0.003″ thick foil, a standard value. In practice, slightly thicker foil (0.004″ to 0.005″) may be required to minimize power losses in the transformer.

Transformer Assembly

Standard practice to increase coupling between primary and secondary is position both as closely as possible to each other inside the transformer. In this design, the first layer wound is one primary, and the next layer is the corresponding secondary. This is again followed by the other secondary and primary. It is important to keep the secondaries in close proximity since both will be conducting simultaneously twice per period. The primaries do not conduct in this manner, so coupling from primary A to primary B is not critical, only primary A to secondary C, and primary B to secondary D.

Referring to the transformer schematic, primary A is wound closest to the bobbin. After insulation, secondaries C and D are wound bifilar and insulated. Primary B is wound last, then terminated so that primaries A and B are wired in series, likewise for secondaries C and D.

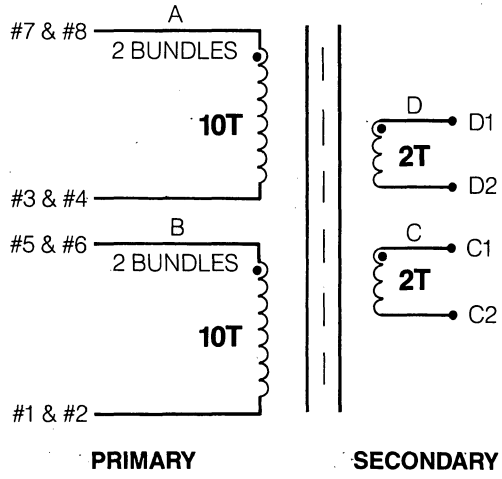

Figure 5. Transformer Schematic

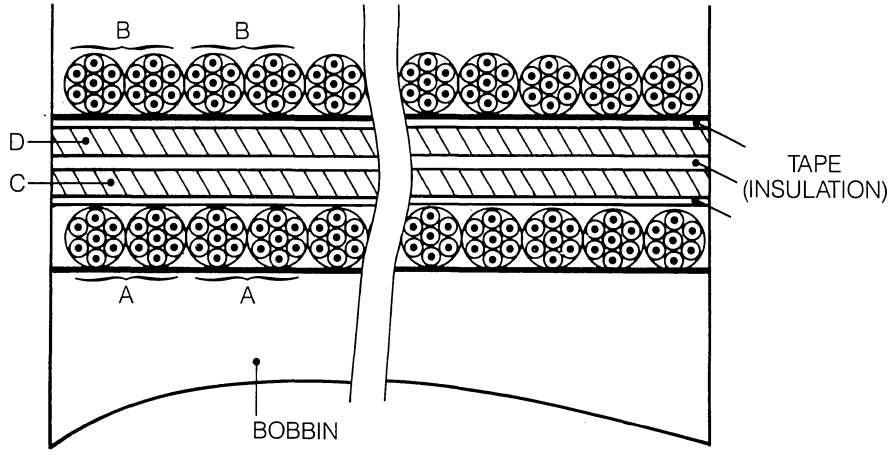

Figure 6. Transformer — Exploded View

Calculation of Winding Resistances and Losses

The mean length of turn for the bobbin can be determined from the specifications of O.D. and I.D., and for the BLP 22/13 a figure of 4.51 cm or 1.77 in. was obtained. AWG #36 wire has a resistance of $1.82 \cdot 10^{-2}$ ohms/cm at 100°C for the following:

Primary resistance can be calculated:

$$R_{pri} = \frac{R_{wire} \cdot M.L.T. \cdot \#\,turns}{\#\,wires} = \frac{0.0182 \cdot 4.51 \cdot 10}{14} = 0.0586 \text{ ohm}$$

Voltage drop and power loss in each half winding can be also calculated:

$V(R_{pri}) = I_{pri} \cdot R_{pri} = 2.0 \cdot 0.58 = 0.116$ volt (negligible)

$P(R_{pri}) = R_{pri} \cdot I_{pri}^2 \cdot duty = 0.0586 \cdot 4 \cdot 0.425$
$= 0.0996$ watts

The resistance of the secondary can be approximated by using the wire tables, and substituting the foil for wire of similar cross-sectional area. In this example, AWG #16 wire is used to obtain $R_{sec} = 1.58 \cdot 10^{-4}$ ohms/cm.

$R_{sec} = R_{foil} \cdot M.L.T. \cdot \#\,turns = 1.58 \cdot 10^{-4} \cdot 4.5 \cdot 2$
$= 0.00143$ ohm

$V(R_{sec}) = 1.43 \cdot 10^{-3} \cdot 10 = 0.0143$ volt (negligible)

$P(R_{sec}) = R_{sec}\,((I_{dc}^2 \cdot D_{on}) + ((I_{dc}/2)^2 \cdot 2 \cdot D_{off}))$

$P(R_{sec}) = 0.00143\,((10^2 \cdot 0.425) + (5^2 \cdot 0.15)) =$
0.066 watts

Transformer Power Losses

The total copper losses for two windings are then:

$P_{cu} = P(R_{pri}) + P(R_{sec}) = 2 \cdot (0.066 + 0.0996)$
$= 0.332$ watts

Estimated eddy current losses are approximately 50% of the copper losses. $P_{cu} \approx 0.50$ watts.

Given the core material type, geometry, frequency and operating Gauss level, the ferrite losses can be calculated. From the manufacturers information, the typical loss coefficient for H7C4 material operating at a flux density swing of 0.055 Tesla (550 Gauss) at 750 kHz is 0.15 watts per cubic centimeter of core volume, which is 3.327 cm^3 per LP 22/13 core set. Therefore:

$P_{core} = 3.327 \cdot 0.15 = 0.50$ watt

The total power lost is a summation of the copper and ferrite losses:

$P_{xfmr} = P_{cu} + P_{core} = 0.50 + 0.50 = 1.00$ watts

OUTPUT SECTION

Output Choke Calculations

Typically, the RMS output ripple current is less than 15% I dc, or 1.5 amps in this case. Delta I, the peak to peak ripple therefore is twice the RMS, or 3 amps.

$$V = \frac{L\,di}{dt} : L = \frac{L\,V\,dt}{di} = \frac{5.9 \text{ v } (350)\ 10^{-9} \text{ s}}{3.0 \text{ A}} = 690 \text{ nanohenries}$$

9

Due to the small value of inductance required, the conventional approach will not be used. Instead, a simple RF type wound coil will be designed using the solenoid equation found in most reference texts. A thick pencil will be utilized as the coil form with a diameter of 0.425 inches, however any similar item will suffice.

The form factor, F, is a function of the form diameter divided by the length of the wound coil, or D/L. A few gyrations will take place before the exact values are obtained, however this goes quickly. The form factor is listed below for various practical values of D/L.

Coil Dia./Length	Form Factor "F"
0.1	0.0025
0.25	0.0054
0.50	0.010
1.0	0.0173
2.0	0.026
5.0	0.040

$L\ (\mu H) = F \bullet N^2 \bullet D\ (in),\ N = (L/F \bullet D)^{1/2}$ (turns)

For D = 0.425, D/L = 1 (approx); F = 0.0173

$N = (0.690 / 0.0173 \bullet 0.425)^{1/2} = 9.76$ turns

Rounding off to the nearest next number of turns, the actual inductance for 10 turns can be calculated:

$L\ (\mu h) = 0.0173 \bullet 10^2 \bullet 0.425 = 744$ nanohenries

In an air core inductor the permeability "u" equals unity, therefore the flux density B equals the driving function H.

Output Capacitor

$$Q = \frac{I\ p\text{-}p}{2} \bullet \frac{T\ period}{2} \bullet \frac{I}{2},\ \text{Delta}\ Q = I\ p\text{-}p / 8 \bullet F$$

C = Q / dV where dV (output ripple) equals 0.100 volts.

$C = I\ p\text{-}p / 8 \bullet F \bullet dV = 3 / 8 \bullet 1.5 \bullet 10^6 \bullet 0.10 = 2.5\ \mu F$

Three 1 μf caps are used in parallel. With a typical ripple voltage of <50 mv due to ESR, the ESR each (at 1.5 mHz) must be approximately 150 milliohms. The Unitrode ceramic monolithic capacitor series was selected for their excellent high frequency characteristics.

Resonance, and its effect at these frequencies must be taken into account. In this case, the capacitor reaches resonance at 1.5 mHz, and the effective impedance is resistive.

Output Diodes

Schottky diodes were selected for their short reverse recovery times to minimize switching losses, and low forward drop for high DC efficiency. The Unitrode USD 640C is a center-tapped TO-220 type, with ample margin to safely accommodate 40 volt reverse transients and 10 amp DC output currents. Also featured is a 0.65 volt maximum drop across each diode and 1 volt per nanosecond switching rate.

UC3825 PWM CONTROL SECTION

Current Limit / Shutdown

Pulse-by-pulse current limiting is performed by the UC3825 by an input of the primary current waveform to the IC at pin 9. The small RC network of R3 and C8 are used to suppress the leading edge glitch caused by turn-on of the mosfet and transformer parasitics. The input must be below the 1 volt threshold or current limiting will occur. Once reached, an input above the threshold will narrow the pulse width accordingly. When this reaches a 1.4 volts amplitude, shutdown of the outputs will occur, and the UC3825 will initiate a soft start routine.

Ramp

The UC3825 offers the flexibility of both Current Mode Control or conventional duty cycle control via the RAMP input pin. When connected to the timing capacitor, the UC3825 operates as a duty cycle control IC. Connecting the RAMP input to the current waveform changes the control method to Current Mode. In this application, the ramp waveform is tied through a small RC filter network to the primary current waveform. This network is defined in the next section — slope compensation. The dynamic range of this input is 1-3 volts, and is generally used for introducing slope compensation to the PWM.

Slope Compensation

Slope compensation is required to compensate for the peak to average differences in primary current as a function of pulse width. Adding a minimum of 50% of the reflected downslope of the output current waveform to the primary current is required. See UNITRODE APPLICATION NOTE U-93 and U-97 for further information. Empirically, 60-75% should be used to accommodate circuit tolerances and increase stability[5]

Resistors R2 and R4 in this circuit form a voltage divider from the oscillator output to the RAMP input, superimposing the slope compensation on the primary current waveform. Capacitor C6 is an AC coupling capacitor, and allows the 1.8 volt swing of the oscillator to be used without adding offset circuitry. Capacitor C7 has a two-fold purpose. During turn on it filters the leading edge noise of the current waveform, and provides a negative going pulse across R4 to the ramp input at the end of each cycle. This overrides any parasitic capacitance at the ramp input, (pin 7), that would tend to hold it above zero volts. This insures the proper voltage input at the beginning of the next cycle.

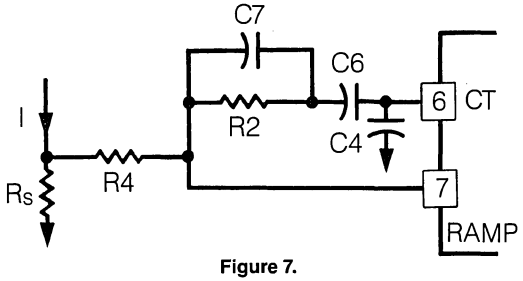

Figure 7.

For the purposes of determining the resistor values, capacitors C4 (timing), C6 (ac coupling) and C7 (filtering) can be removed from the circuit schematic. The simplified model represented in figure 8 is used for the calculations. These calculations can be applied to all Current Mode circuits using a similar scheme.

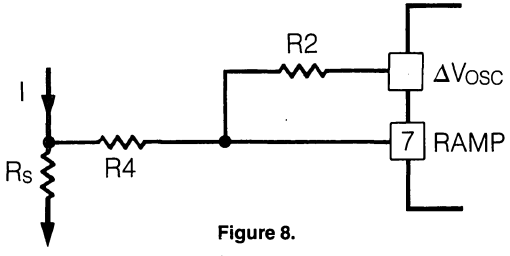

Figure 8.

STEP 1. Calculate Inductor Downslope
$S(L) = di/dt = V\,sec / L = 5.9\,V / .740\,\mu H = 8.0\,A/\mu s$ (1)

STEP 2. Calculate Reflected Downslope to Primary
$S(L)' = S(L) / N\,(turns\ ratio) = 8.0/5 = 1.6\,A/\mu S$ (2)

STEP 3. Calculate Equivalent Ramp Downslope Voltage
$V\,S(L)' = S(L)' \bullet Rsense = 1.6 \bullet 0.375 = 0.600\,V/\mu s$ (3)

STEP 4. Calculate Oscillator Slope
$V\,S\,(osc) = d\,(V\,osc) / T\,on = 1.8\,V / 570\,ns = 3.15\,V/\mu s$ (4)

STEP 5. Generate the Ramp Equations
Using superposition, the circuit can be configured as:

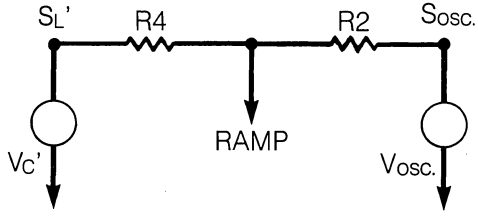

Figure 9.

$$V\,(ramp) = \frac{V\,S\,(L)' \bullet R2}{R2 + R4} = \frac{V\,S\,(osc) \bullet R4}{R2 + R4} \quad (5)$$

SUBSTITUTING,
$V\,(ramp) = V\,S\,(L)'' + V\,S\,(comp)$ (6)

WHERE

$$V\,S\,(comp) = \frac{V\,S\,(osc) \bullet R4}{R2 + R4}; \quad V\,S\,(L)'' = \frac{V\,S\,(L)' \bullet R2}{R2 + R4}$$

STEP 6. Calculate Slope Compensation
$V\,S\,(comp) = m \bullet S(L)''$ (7)

Where m equals the amount of inductor downslope to be introduced. In this example, let m = 75%, or 0.75.

$$\frac{V\,S\,(osc) \bullet R4}{R2 + R4} = \frac{m \bullet V\,S(L)' \bullet R2}{R2 + R4}$$

SOLVING FOR R2:

$$R2 = R4 \bullet \frac{V\,S\,(osc)}{V\,S\,(L)' \bullet m} = R4 \bullet \frac{3.15}{0.600 \bullet 0.75} \quad (9)$$

USING CIRCUIT VALUES,
$R2 = 7.05 \bullet R4$

For simplicity, let R4 equal 1 K ohms and R2 therefore equals 7.05 K. Using the nearest standard value resistor of 6.8 K, the exact amount of downslope is minimally affected. Important, however, is that the series combination of R2 and R4 is high enough in resistance not to load down the oscillator and cause frequency shifting.

9

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CLOSING THE FEEDBACK LOOP

Error Amplifier

Compensation of the high gain error amplifier in the UC3825 is straight forward. There is a single-pole at approximately 5 hertz. A zero will be introduced in the compensation network to provide gain once the zero db threshold is crossed. Using Current Mode control greatly simplifies the compensation task as the output choke is controlled by the inner current loop, thus making the output section appear as a single pole response with a zero at the ESR frequency[4]

Control to Output Gain

The control to output gain will vary with output loading, and as the load is increased the gain decreases. Output capacitor ESR will determine the frequency at which the zero occurs, thus changing the gain as a function of ESR. To insure stability through all combinations of load and ESR, the amplifier will be compensated to cross zero db at approximately one-fifth of the switching frequency with ample phase margin.

The output filter pole and zero occur at

$F_p = 1/2\,\pi\,R\,(load)\,C\,(output)$

$F_z = 1/2\,\pi\,R\,(esr)\,C\,(output)$

CIRCUIT PARAMETERS:

C (output) = 3 μF; ESR (each) = 0.050 min – 0.300 max

For three capacitors in parallel, ESR = 0.016 – 0.100 ohms

R (output) = 2.5 ohms at 2 A, 0.5 ohms at 10 A

Using the above equations;

$F_p\,(2A) = 1 / (2 \cdot 3.14 \cdot 2.5 \cdot 3 \cdot 10^{-6}) = 21.2$ kHz

$F_p\,(10A) = 1 / (2 \cdot 3.14 \cdot 0.5 \cdot 3 \cdot 10^{-6}) = 106.1$ kHz

$F_z\,(high) = 1 / (2 \cdot 3.14 \cdot 0.016 \cdot 3 \cdot 10^{-6}) = 3.315$ mHz

$F_z\,(low) = 1 / (2 \cdot 3.14 \cdot 0.100 \cdot 3 \cdot 10^{-6}) = 530.5$ kHz

GAIN

$$\frac{V\,(output)}{V\,(control)} = K \cdot R_o, \text{ where } K = \frac{Ipri \cdot N_p/N_s}{V\,(control)} = \frac{2 \cdot 5}{0.85} = 11.76$$

Therefore, at 2 amps and 10 amps,

$V_o/V_c = K \cdot ro = 11.76 \cdot 2.5 = 29.4$ db (2A)

$V_o/V_c = K \cdot ro + 11.76 \cdot 0.5 = 15.4$ db (10A)

Error Amplifier Compensation

The control to output gain can be plotted along with the desired zero db crossing point and an estimate of the error amplifier required compensation network can be made. The amp compensation should have a zero at approximately 100 kHz, and a gain of –16 db at this frequency. Resistor R9 has been selected to be 3.3 k ohms based on the output drive capability of the UC3825 amp. Complete specifications are contained in the UC3825 data sheet.

F zero (amp) = 1 / (2 • π • R9 • C12)

therefore, C12 = 1 / (2 • π • R9 • F zero)

C12 = 1 / (2 • 3.14 • 3300 • 100.000) = 480 pF (use 560 pF)

R10 / R9 = approx –16 db (0.16),

R10 = R9 / gain = 3.3 K / 0.16 = 20.4 K (use 20 K)

This compensated response can now be plotted, along with the control to output gain and the overall power supply response is a summation of the two curves, as seen in figures 11 and 12. Low frequency gains of 100 db at full load, and 115 db at light load are obtained, with a zero db crossing at approx. 100 kHz for both. Phase margin is generous with approx. 90 degrees for both light and 45 degrees at full load.

GAIN AND PHASE RESPONSE
UC3825 DEMO KIT

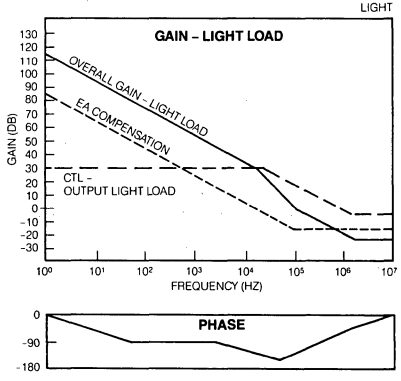


Figure 11.

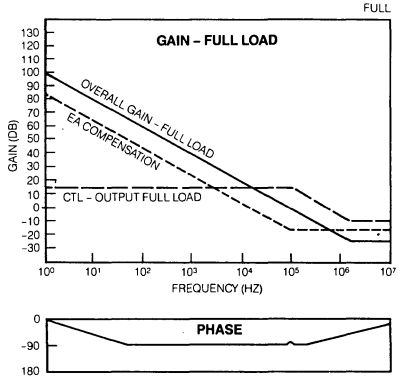


Figure 12.

LIST OF MATERIALS

REFERENCE	DESCRIPTION	
Capacitors		
C1, 2	4.7 μF, 63 VDC Electrolytic	
C3, 5	0.1 μF, 50 VDC Monolithic	
C4	470 pF, VDC Monolithic	
C6	0.01 μF, 50 VDC Monolithic	
C7	120 pF, 50 VDC Monolithic	
C8	15 pF, 50 VDC Monolithic	
C9-11, 17-19	1 μF, 50 VDC Monolithic	
C12	560 pF, 50 VDC Monolithic	
C13, 14	150 pF, 150 VDC Ceramic	
C15, 16	5000 pF, 50 VDC Ceramic	
Diodes		
CR1	1N4465	10 V, 1.5 Watt Zener
CR2, 3	USD1140	40 V, 1 Amp Schottky
CR4, 5	UES1105	150 V, 2.5 Amp Ultrafast
CR6, 7	USD640C	40 V, 12 Amp Schottky
Integrated Circuits		
U1	UC3825	Unitrode High Speed PWM
Transistors		
Q1, 2	UFN633	150 V, 8A Mosfet
Resistors		
R1	1.5 K, 1/2 W, 1%	
R2	6.8 K, 1/2 W, 5%	
R3, 4, 14, 15	1 K, 1/2 W, 5%	
R5-8	1.5 R, 1 W, 5%	
R9	3.3 K, 1/2 W, 5%	
R10	20 K, 1/2 W, 5%	
R11, 12	6.2 R, 1/2 W, 5%	
R13	500 R, 5 W, 10%	
R16-19	200 R, 1/2 W, 5%	
R20-23	24 R, 1/2 W, 5%	
R24	51 R, 1 W, 5%	
Magnetics		
L1	740 nH Wound Coil	
T1	AIE Magnetics Custom Transformer, 5:1 Turns Ratio	
Miscellaneous		
H1	Heatsink—Mosfets (AAALL #5786B)	
H2	Heatsink—Diodes (AAALL #5299B)	

Efficiency Measurements

V (In)	I (In)	P (In)	P (Loss)	Efficiency
42	1.707	71.7	20.2	71.8%
48	1.483	71.2	19.7	72.4%
56	1.331	73.2	21.7	70.4%

V (In) V	Vout (2A)	Vout (5A)	Vout (10A)	Load Reg. MV
42	5.110	5.102	5.093	17
48	5.108	5.101	5.092	16
56	5.108	5.102	5.089	19
Line	2 mv	1 mv	4 mv	

Dynamic Performance

The power supply was pulse loaded from 5 amps to 10 amps at a frequency of 100 kilohertz. Recovery to within 50 mv was less than 2 microseconds with a total excursion of less than 200 millivolts. High speed FETS were used to switch the load current with typical rise/fall times of 50 nanoseconds.

Short Circuit

The short circuit input current is approximately 0.75 amps, or an input power of 36 watts.

Circuit Power Losses

The total circuit losses are approximated using both the calculated and measured losses throughout the power supply.

Power Losses

Current Sense Circuit	1.2 W
Output Diodes	9.8 W
Switching Transistors	3.2 W
Dropping Resistor	3.0 W
Snubber Networks	1.0 W
Transformer Losses	1.0 W
Auxiliary Supply	0.8 W
Miscellaneous	0.2 W
TOTAL LOSSES	20.2 W

If a bootstrapped technique is utilized in the auxiliary supply to the IC and drive circuitry, the dropping resistor losses of three watts can be reduced to 0.1 watts in the bootstrap circuitry. In addition, the lossy resistive current sensing network can be replaced by a small current transformer, lowering the losses by a half-watt. Overall efficiency would then increase to 75%, fairly high for a five volt output application. Noteworthy is that the switching losses at this high of frequency can be minimized, and have little overall effect on circuit efficiency.

9

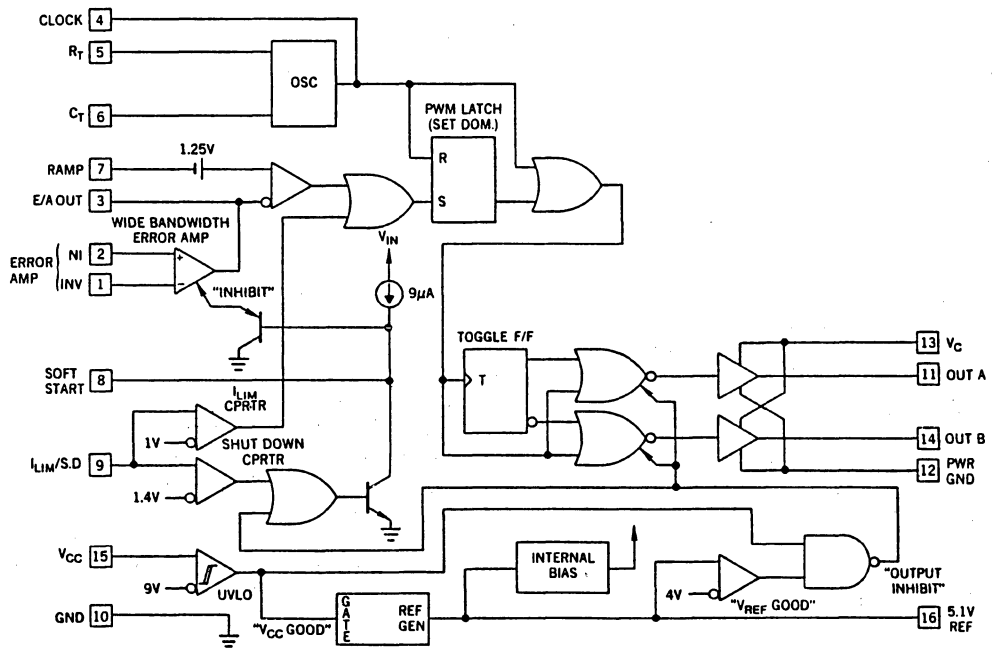
Summary

The demands of higher power densities will undoubtedly throttle many switch-mode power supply designs into and beyond the megahertz region in the near future. Designers will be facing the challenges of selecting switching devices, magnetic materials and IC controllers built exclusively for high efficiency at these frequencies. The thrust from contemporary hundreds of kilohertz designs to megahertz versions is rapidly making progress. This 1.5 MHZ current mode push-pull is an example of what can successfully be accomplished with existing high speed components and technology.

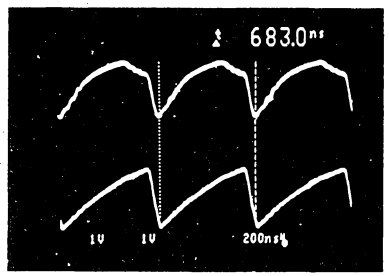
References

1. Woffard, Larry, — "New Pulse Width Modulator Chip Controls, MHZ Switchers" — U-107; Unitrode Applications Handbook 1987/88.
2. Dixon, Lloyd Jr. — "Eddy Current Losses" Section M2-4, Unitrode Power Supply Design Seminar Book, SEM-500.
3. Andreycak, Bill — "1.5 MHZ Current Mode IC Controlled 50 Watt Power Supply," Proceedings of the High Frequency Power Conversion Conference, 1986.
4. Dixon, Lloyd Jr. — "Closing the Feedback Loop" Section C1 — Unitrode Power Supply Design Seminar Book, SEM-500.
5. Andreycak, Bill "Practical Considerations in Current Mode Power Supplies" Topic 1 — Unitrode Power Supply Design Seminar Book, SEM-500.

UC3825 BLOCK DIAGRAM



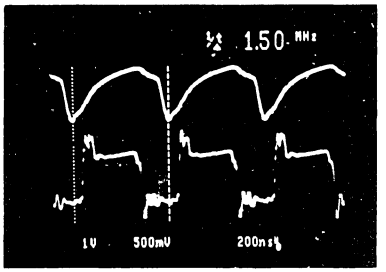
TIMING WAVEFORMS



Top Trace
Ramp Voltage
TP 'H', 1 v/cm

Bottom Trace
CT Waveform,
TP 'D', 1 v/cm

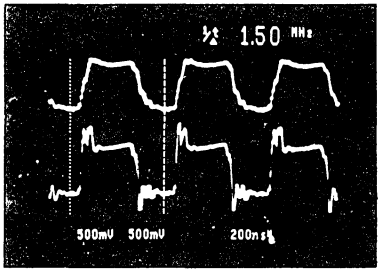
RAMP VOLTAGE



Top Trace
Filtered Ip with
Slope Compensation
TP 'H', 1 v/cm

Bottom Trace
Unfiltered Ip
TP 'P', .5 v/cm

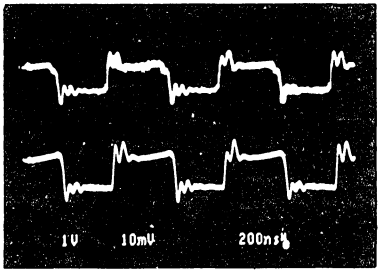
PRIMARY CURRENT



Top Trace
Filtered Ip
TP 'I', .5 v/cm

Bottom Trace
Unfiltered Ip
TP 'P', .5 v/cm

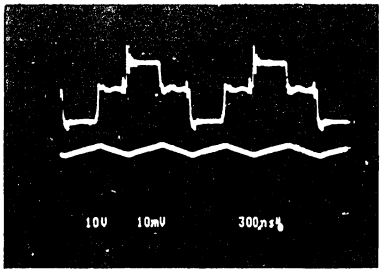
PRIMARY CURRENT



Top Trace
J1, 2 A/cm

Bottom Trace
TP 'P', 1 v/cm

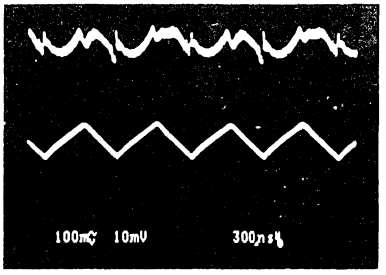
SECONDARY WAVEFORMS



Top Trace
Secondary Voltage
TP 'T', 10 v/cm

Bottom Trace
Secondary Current
J2, 5 A/cm

OUTPUT WAVEFORMS



Top Trace
Output Voltage
Ripple & Noise
TP 'W', 100 mv/cm

Bottom Trace
AC Output Current
J2, 2 A/cm

9

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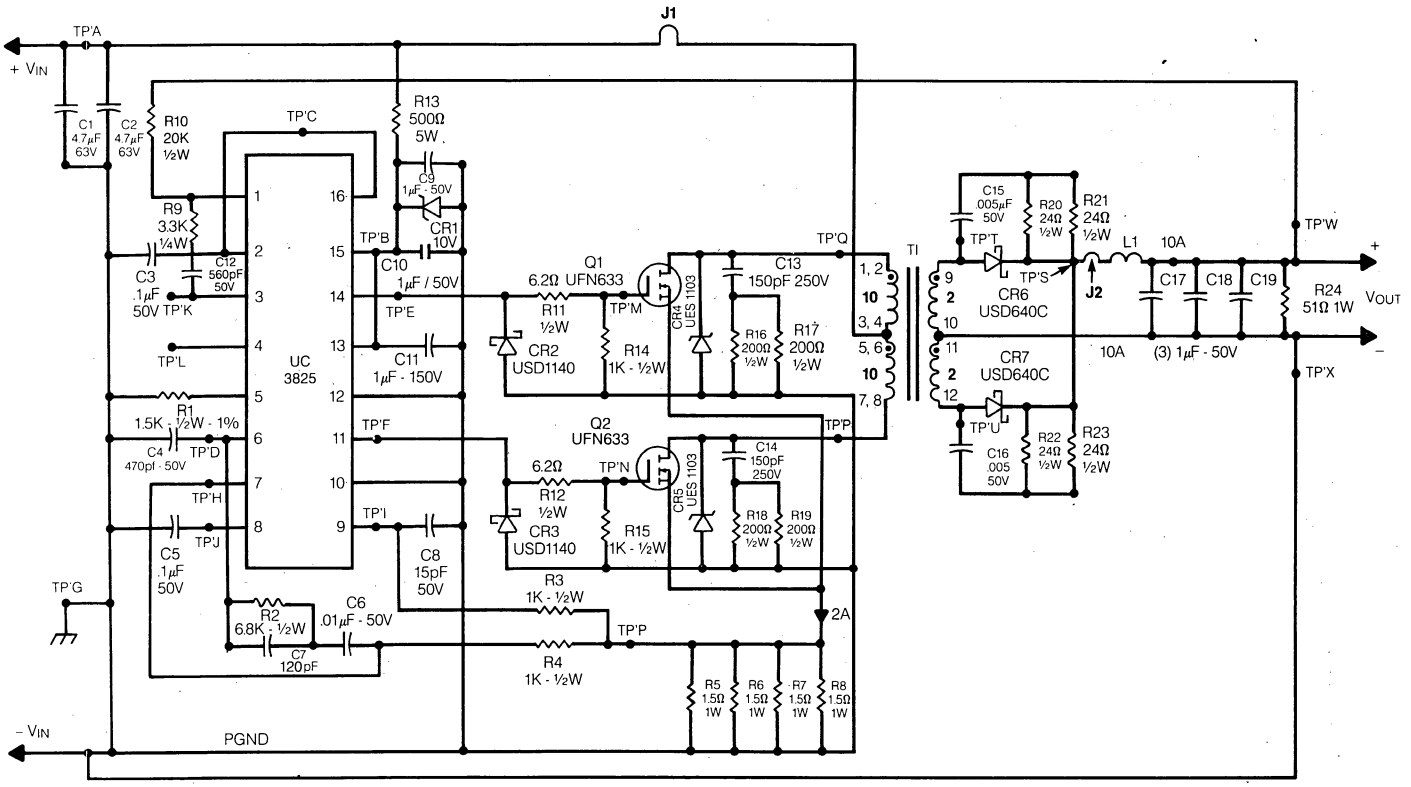

Figure 1. 1.5 MHz Push-Pull Converter Schematic Diagram

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PRACTICAL CONSIDERATIONS IN CURRENT MODE POWER SUPPLIES

Introduction

This detailed section contains an in-depth explanation of the numerous PWM functions, and how to maximize their usefulness. It covers a multitude of practical circuit design considerations, such as slope compensation, gate drive circuitry, external control functions, synchronization, and paralleling current mode controlled modules. Circuit diagrams and simplified equations for the above items of interest are included. Familiarity with these topics will simplify the design and debugging process, and will save a great deal of time for the power supply design engineer.

I. SLOPE COMPENSATION

Current mode control regulates the PEAK inductor current via the 'inner' or current control loop. In a continuous mode (buck) converter, however, the output current is the AVERAGE inductor current, composed of both an AC and DC component.

While in regulation, the power supply output voltage and inductance are constant. Therefore, V_{OUT} / L_{SEC} and dI/dT, the secondary ripple current, is also constant. In a constant volt-second system, dT varies as a function of V_{IN}, the basis of pulse width modulation. The AC ripple current component, dI, varies also as a function of dT in accordance with the constant V_{OUT} L_{SEC}.

Average Current

At high values of V_{IN}, the AC current in both the primary and the secondary is at its maximum. This is represented graphically by duty cycle D1, the corresponding average current I1, and the ripple current d(I1). As V_{IN} decreases to its minimum at duty cycle, the ripple current also is at its minimum amplitude. This occurs at duty cycle D2 of average current I2 and ripple current d(I2). Regulating the peak primary current (current mode control) will produce different AVERAGE output currents I1, and I2 for duty cycles D1 and D2. The average current INCREASES with duty cycle when the peak current is compared to a fixed error voltage.

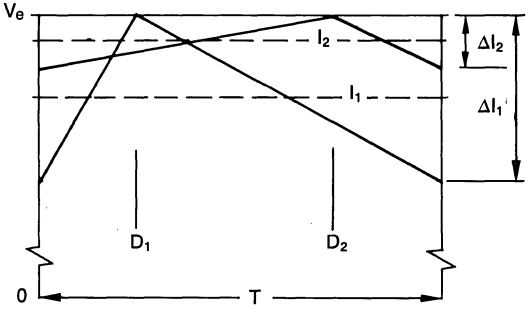

Figure 1. Average Current Error

Constant Output Current

To maintain a constant AVERAGE current, independent of duty cycle, a compensating ramp is required. Lowering the error voltage precisely as a function of T_{ON} will terminate the pulse width sooner. This narrows the duty cycle creating a CONSTANT output current independent of T_{ON}, or V_{IN}. This ramp simply compensates for the peak to average current differences as a function of duty cycle. Output currents I1 and I2 are now identical for duty cycles D1 and D2.

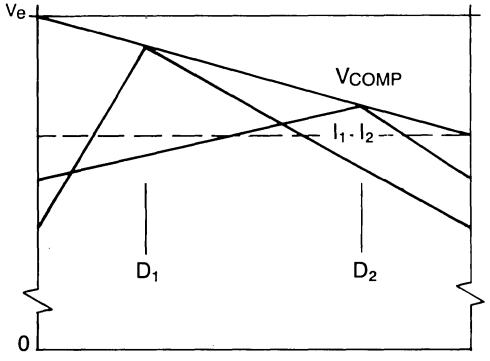

Figure 2. Constant Average Current

Determining the Ramp Slope

Mathematically, the slope of this compensating ramp must be equal to one-half (50%) the downslope of the output inductor as seen from the control side of the circuit. This is proven in detail in "Modelling, Analysis and Compensating of the Current Mode Controller," (Unitrode publication U-97 and its references). Empirically, slightly higher values of slope compensation (75%) can be used where the AC component is small in comparison to the DC pedestal, typical of a continuous converter.

Circuit Implementation

In a current mode control PWM IC, the error voltage is generated at the output of the error amplifier and compared to the primary current at the PWM comparator. At this node, subtracting the compensating ramp from the error voltage, or adding it to the primary current sense input will have the same effect: to decrease the pulse width as a function of duty cycle (time). It is more convenient to add the slope compensating ramp to the current input. A portion of the oscillator waveform available at the timing capacitor (C_T) will be resistively summed with the primary current. This is entered to the PWM comparator at the current sense input.

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Parameters Required for Slope Compensation Calculations

Slope compensation can be calculated after specific parameters of the circuit are defined and calculated.

SECTION	PARAMETER
Control	T on (Max) Oscillator
	ΔV Oscillator (PK-PK Ramp Amplitude)
	I Sense Threshold (Max)
Output	V Secondary (Min)
	L Output
	I AC Secondary
	(Secondary Ripple Current)
General	R Sense (Current Sensing Resistor)
	M (Amount of Slope Compensation)
	N Turns Ratio (N_P / N_S)

Once obtained, the calculations for slope compensation are straightforward, using the following equations and diagrams.

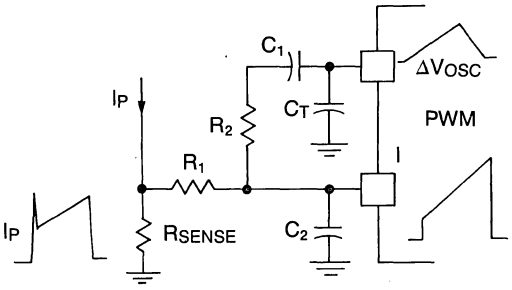

Figure 3. General Circuit

Resistors R1 and R2 form a voltage divider from the oscillator output to the current limit input, superimposing the slope compensation on the primary current waveform. Capacitor C1 is an AC coupling capacitor, and allows the AC voltage swing of the oscillator to be used without adding offset circuitry. Capacitor C2 forms an R-C filter with R1 to suppress the leading edge glitch of the primary current wave. The ratio of resistor R2 to R1 will determine the exact amount of slope compensation added.

For purposes of determining the resistor values, capacitors C_T (timing), C1 (coupling), and C2 (filtering) can be removed from the circuit schematic. The oscillator voltage (V_{OSC}) is the peak-to-peak amplitude of the sawtooth waveform. The simplified model is represented schematically in the following circuit.

These calculations can be applied to all current mode converters using a similar slope compensating scheme.

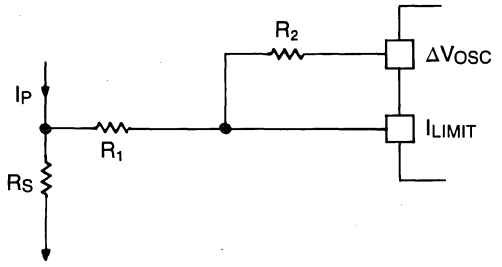

Figure 4. Simplified Circuit

Step 1. Calculate the Inductor Downslope
$S(L) = di/dt = V_{SEC}/L_{SEC}$ (Amps/Second)

Step 2. Calculate the Reflected Downslope to the Primary
$S(L)' = S(L)/N$ (Amps/Second)

Step 3. Calculate Equivalent Downslope Ramp
$V\,S(L)' = S(L)' \bullet R\ sense$ (Volts/Second)

Step 4. Calculate the Oscillator Charge Slope
$V\,S_{(OSC)} = d\,(V_{OSC}) / T\ on$ (Volts/Second)

Step 5. Generate the Ramp Equations
Using superposition, the circuit can be illustrated as:

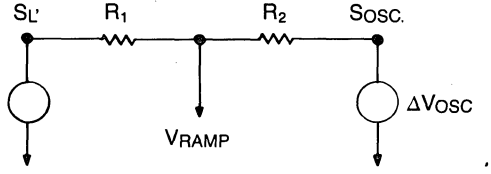

Figure 5. Superposition

$$V_{(RAMP)} = \frac{V\,S(L)' \bullet R2}{R1 + R2} + \frac{V\,S_{(OSC)} \bullet R1}{R1 + R2} \quad \text{simplifying,}$$

$$V_{(RAMP)} = V\,S(L)'' + V\,S_{(COMP)} \quad \text{where}$$

$$V\,S_{(COMP)} = \frac{V\,S_{(OSC)} \bullet R1}{R1 + R2}\ , \text{and } V\,S(L)'' = \frac{V\,S(L)' \bullet R2}{R1 + R2}$$

Step 6. Calculate Slope Compensation
$V\,S(COMP) = M \bullet S(L)''$ where M is the amount of inductor downslope to be introduced.

$$\text{Equating } \frac{V\,S_{(OSC)} \bullet R1}{R1 + R2} = \frac{M \bullet V\,S(L)' \bullet R2}{R1 + R2}$$

, solving for R2

$$R2 = R1 \bullet \frac{V\,S_{(OSC)}}{V\,S(L)' \bullet M}$$

Equating R1 to 1K ohm simplifies the above calculation and selection of capacitor C2 for filtering the leading edge glitch. Using the closest standard value to the calculated value of R2 will minimally effect the exact amount of downslope introduced. It is important that R2 be high enough in resistance not to load down the I.C. oscillator, thus causing a frequency shift due to the slope compensation ramp to R2.

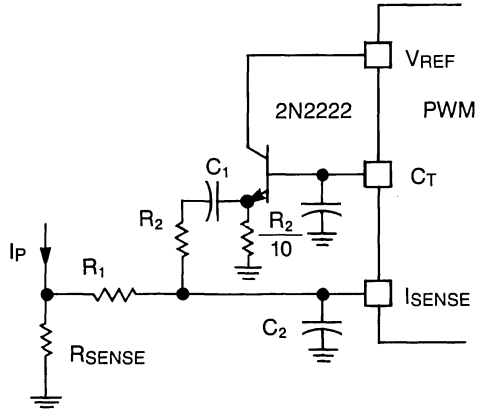

Figure 6. Emitter Follower Circuit

Design Example — Slope Compensation Calculations

Circuit Description and Parameter Listing:

Topology: Half-Bridge Converter
Input Voltage: 85-132 VAC "Doubler Configuration"
Output: 5 VDC/45 ADC
Frequency: 200 KHz, T Period = 5.0 μS
T Deadtime: 500 ns, T on Max = 4.5 μS
Turns Ratio: 15 / 1, (Np/Ns)
V Primary: 90 VDC Min, 186 Max
V Sec Min: 6 VDC
R Sense: 0.25 Ohm
I Sec Ac: 3.0 Amps (<10% I DC)
L Output: 5.16 μh

1. Calculate the Inductor Downslope on the Secondary Side

$S(L) = di/dt = V_{SEC}/L_{SEC} = 6\ v/5.16\ \mu h = 1.16\ A/\mu s$

2. Calculate the Transformed Inductor Slope to the Primary Side

$S(L)' = S(L) \bullet Ns/Np = 1.16 \bullet 1/15 = 0.0775\ A/\mu S$

3. Calculate the Transformed Slope Voltage at Sense Resistor

$V\ S(L)' = S(L)' \bullet Rsense = 7.72 \bullet 10^{-2} \bullet 0.250 = 1.94 \bullet 10^{-2}\ V/\mu S$

4. Calculate the Oscillator Slope at the Timing Capacitor

$S_{(OSC)} = d\ V\ osc/T\ on\ max = 1.8/4.5 = 0.400\ V/\mu S$

5. Let Amount of Slope Compensation (M) = 0.75 and R1 = 1K

$$R2 = R1 \bullet \frac{V\ S_{(OSC)}}{V\ S(L)' \bullet M}\ ;\ R2 = \frac{1K \bullet 0.400}{0.0192 \bullet 0.75}$$

= 27.4 K ohms

II. GATE DRIVE CIRCUITRY

The high current totem-pole outputs of most PWM ICs have greatly enhanced and simplified MOSFET gate drive circuits. Fast switching times of the high power FETs can be attained with nearly a "direct" drive from the PWM. Frequently overlooked, only two external components — a resistor and Schottky diode are required to insure proper operation of the PWM while delivering the high current drive pulses.

MOSFET Input Impedance

Typical gate-to-source input characteristics of most FETs reveal approximately 1500 picofarads of capacitance in series with 15 nanohenries of source inductance. For this example, the series gate current limiting resistor will not be used to exemplify its necessity. Also, the totem pole transistors are replaced with ideal (lossless) switches. A dV/dT rate of 0.5 volts per nanosecond is typical for most high speed PWMs and will be incorporated.

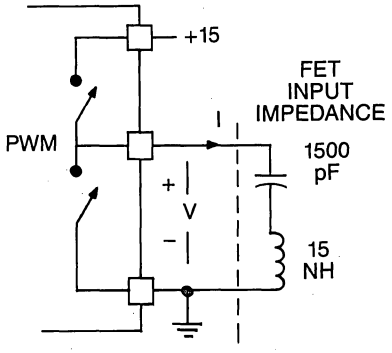

Figure 7. Ideal Circuit Gate Drive

Assuming no external circuit parasitics of R, L or C, the PWM is therefore driving an L-C resonant tank with no attenuation. The driving function is a 15 volt pulse derived from the auxiliary supply voltage. The resulting current waveform is shown in figure 8, having a peak current of approximately seven amps at a frequency of thirty-three megahertz.

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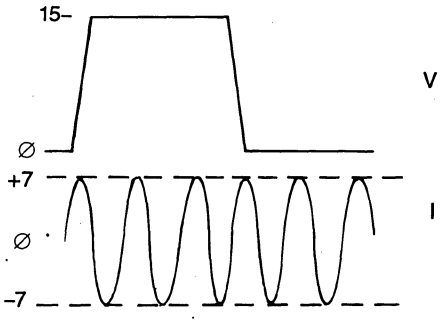

Figure 8. Voltage & Current Waveforms at Gate

In a practical application, the transistors and other circuit parameters, fortunately, are less than ideal. The results above are unlikely to happen in most designs, however they will occur at a reduced magnitude if not prevented.

Limiting the peak current through the IC is accomplished by placing a resistor between the totem-pole output and the gate of the MOSFET. The value is determined by dividing the totem-pole collector voltage (V_C) by the peak current rating of the IC's totem-pole. Without this resistor, the peak current is limited only by the dV/dT rate of the totem-pole and the FET gate capacitance.

For this example, a collector supply voltage of 10 volts is used, with an estimated totem-pole saturation voltage of approximately 2 volts. Limiting the peak gate current to 1.5 amps max requires a resistor of six ohms, and the nearest standard value of 6.2 ohms was used. Locating the resistor in series with the collector to the auxiliary voltage source will only limit the turn-on current. Therefore it must be placed between the PWM and gate to limit both turn-on and turn-off currents.

Actual circuit parasitics also play a key role in the drive behavior. The inductance of the FET source lead (15 nanohenries typical) is generally small in comparison to the layout inductance. To model this network, an approximation of 30 nanohenries per inch of PC trace can be used. In addition, the inductance between the pins of the IC and the die can be rounded off to 10 nanohenries per pin. It now becomes apparent that circuit inductances can quickly add up to 100 nanohenries, even with the best of PC layouts. For this example, an estimate of 60 nh was used to simulate the demonstration PC board. The equivalent circuit is shown in figure 10. A 10 volt pulse is applied to the network using 6.2 ohms as the current limiting resistance. Displayed is the resulting voltage and current waveform at the totem-pole output.

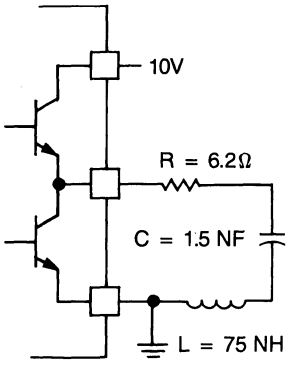

Figure 9. Circuit Parameters

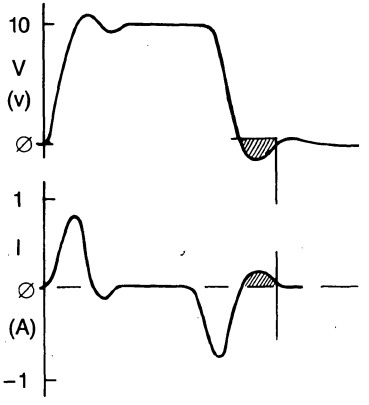

Figure 10. Circuit Response

The shaded areas of each graph are of particular interest. During this time, the lower totem-pole transistor is saturated. The voltage at its collector is negative with respect to it's emitter (ground). In addition, a positive output current is being supplied to the RLC network thru this saturated NPN transistor's collector. The IC specifications indicate that neither of these two conditions are tolerable individually, nevermind simultaneously. One approach is to increase the limiting resistance to change the response from underdamped to slightly overdamped. This will occur when:

$R\ (gate) \geq 2 \bullet \sqrt{L/C}$

Unfortunately, this also reduces the peak drive current, thus increasing the switching times of the FETS — highly undesirable. The alternate solution is to limit the peak current, and alter the circuit to accept the underdamped network.

The use of a Schottky diode from the PWM output to ground will correct both situations. Connected with the anode to ground and cathode to the output, it will prevent the output voltage from going excessively below ground, and will also provide a current path. To be effective, the diode selected should have a forward voltage drop of less than 0.3 volts at 200 milliamps. Most 1-to-3 amp diodes exhibit these traits above room temperature. The diode will conduct during the shaded part of the curve shown in figure xx when the voltage goes negative and the current is positive. The current is allowed to circulate without adversely effecting the IC performance. Placing the diode as physically close to the PWM as possible will enhance circuit performance. Circuit implementation of the complete drive scheme is shown in the schematic.

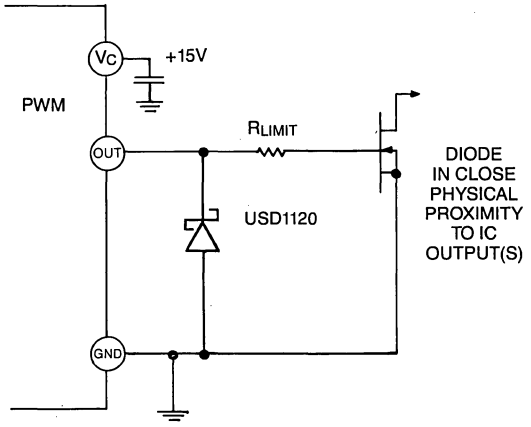

Figure 11.

Transformer driven circuits also require the use of the Schottky diodes to prevent a similar set of circumstances from occurring on the PWM outputs. The ringing below ground is greatly enhanced by the transformer leakage inductance and parasitic capacitance, in addition to the magnetizing inductance and FET gate capacitance. Circuit implementation is similar to the previous example.

Peak Gate Current and Rise Time Calculations

Several changes occur at the MOSFET gate during the turn-on period. As the gate threshold voltage is reached, the effective gate input capacitance goes up by about fifteen percent, and as the drain current flows, the capacitance will double. The gate-to-source voltage remains fairly constant while the drain voltage is decreasing. The peak gate current required to switch the MOSFET during a specified turn-on time can be approximated with the following equation.

$$I\,pk = \frac{2}{Ton}\left\{ Ciss\left[(2.5 \bullet Vgth) + \frac{Id}{gm} \right] + [Crss\,(VDD - Vgth)\,] \right\}$$

Several generalizations can be applied to simplify this equation. First, let Vgth, the gate turn-on threshold, equal 3 volts. Also, assume gm equals the drain current Id divided by the change in gate threshold voltage, dVgth. For most applications, dVgth is approximately 2.5 volts for utilization of the FET at 75% of its maximum current rating. In most off-line power supplies, the gate threshold voltage is a small percentage of the drain voltage and can be eliminated from the last part of the equation. The formulas to determine peak drive current and turn-on time using the FET parameters now simplify to:

$$I\,pk = \frac{2}{Ton} \bullet \{ (10 \bullet Ciss) + (Crss \bullet V\,drain) \}$$

$$Ton = \frac{2}{I\,pk} \bullet \{ (10 \bullet Ciss) + (Crss \bullet Vdrain) \}$$

Switching times in the order of 50 nanoseconds are attainable with a peak gate current of approximately 1.0 amps in many practical designs. Higher drive currents are obtainable using most Unitrode current mode PWMs which can source and sink up to 1.5 amps peak (UC1825). Driver ICs with similar output totem poles (UC1707) are recommended for paralleled MOSFET, high speed applications.

III. SYNCHRONIZATION

Power supplies have historically been thought of as "black boxes," an off-the-shelf commodity by most end users. Their primary function is to generate a precise voltage, independent of load current or input voltage variations, at the lowest possible cost. In addition, end users allocate a minimal amount of system real estate in which it must fit. The major task facing design engineers is to overcome these constraints while exceeding the customers' expectations, attaining high power densities and avoiding thermal management problems. It is imperative, too, that the power supply harmonize and integrate with the system rather than cause catastrophic noise problems and last minute headaches. Products that had performed to satisfaction on the lab workbench powered by well filtered linear supplies may not fare as well when driven by a noisy switcher enclosed in a small cabinet.

Basic power supply design criteria such as the switching frequency may be designated by the system clock or CPU and thus may not be up to the power supply designer's discretion. This immediately impacts the physical size of the magnetic components, hence overall supply size, and may result in less-than-optimum power density. However, for the system to function properly, the power supply must be synchronized to the system clock.

There are numerous other reasons for synchronizing the power supply to the system. Most switching power noise has a high peak-to-average ratio of short duration, generally referred to as a spike. Common mode noise generated by these pulsating currents through stray capacitance may be difficult (if not impossible) to completely eliminate after the system design is complete. Ground loop noise may also be amplified due to the interaction of changing currents through parasitic inductances, resultng in crosstalk through the system. EMI filtering to the main input line is much simpler and more repeatable when power is processed at a fixed frequency.

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In addition, multiple power stages require synchronization to reduce the differential noise generated between modules at turn-on. In unison, the converters begin their cycles at the same time, each contributing to common mode noise simultaneously, rather than randomly. This also simplifies peak power considerations and will result in predictable power distribution and losses. Compensation made for voltage drops along the bus bars, produced by both the AC and DC power current components, can be accomplished. Balancing of the loads and power bus losses also contributes to diminishing the differential noise and should be administered for optimum results.

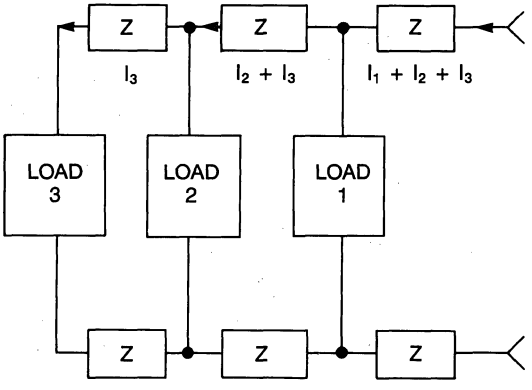


Figure 12.

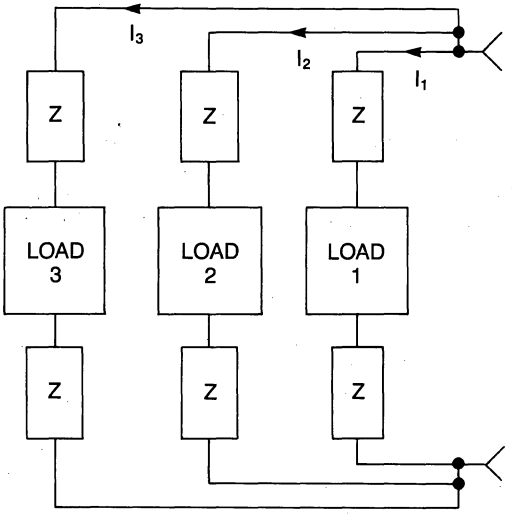


Figure 13.

Operation of the PWM Oscillator

In normal operation, the timing capacitor (Ct) is linearly charged and discharged between two thresholds, the upper and lower comparator thresholds. The charging current is determined by means of a fixed voltage across a user selected timing resistance (Rt). The resulting current is then mirrored internally to the timing capacitor Ct at the IC's Ct output. The discharge current is internally set in most PWM designs.

As Ct begins its charge cycle, the outputs of the PWM are initiated and turn on. The timing capacitor charges, and when its amplitude equals that of the error amplifier output, the PWM output is terminated and the outputs turn off. Ct continues to charge until it reaches the upper threshold of the timing comparator. Once intersected, the discharge circuitry activates and discharges Ct until the timing comparator lower threshold is reached. During this discharge time, the PWM outputs are disabled, thus insuring a "dead" time when each output is off.

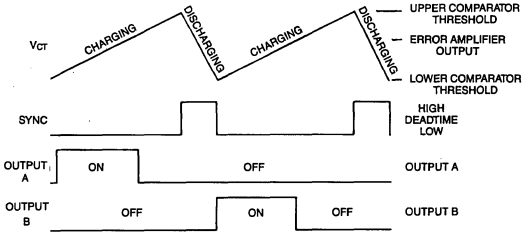


Figure 14. Voltage Mode Control – Normal Operation

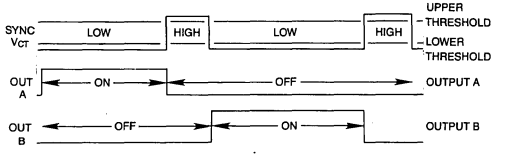


Figure 15.

The SYNC terminal provides a "digital" representation of the oscillator charge/discharge status and can be utilized as both an input or an output on most PWM's. In instances where no synchronization port is easily available, the timing circuitry (Ct) can be driven from a digital (0V, 5V) logic input rather than in the analog mode. The primary considerations of on-time, off-time, duty cycle and frequency can be encompassed in the digital pulse train. A LOW logic level input determines the PWM ON time. Conversely, a HIGH input governs the OFF time, or dead time. Critical constraints of frequency, duty cycle or dead time can be accurately controlled by a digital signal to the PWM timing cap (Ct) input. The command can be executed by anything from a simple 555 timer, to an elaborate microprocessor software controlled routine.

Not all PWM IC's have a direct synchronization input/output connection available to the internal oscillator. In these applications, the slave oscillator must be disabled and driven in a different fashion. This approach may also be required when using different PWMs amongst the slave modules with different sync characteristics, or anti-phase signals.

Unfortunately, there are several drawbacks to this method, depending on the implementation. First, the PWM error amplifier has no control over the pulse width in voltage mode control. The error amplifier output is compared to a digital signal instead of a sawtooth ramp, rendering its attempts fruitless. The conventional soft start technique of clamping the error amp output, thereby clamping the duty cycle will not function. With no local timing ramp available, the supply is completely under the direction of the sync pulse source. Should the pulse become latched or removed, the PWM outputs will either stay fully on, or fully off, depending on the sync level input (voltage mode). Also, without the local Ct ramp, the supply will not self-start, remaining off until the sync stream appears. Slope compensation for current mode controlled units requires additional components to generate the compensating ramp. Every supply must be produced as a dedicated master, or slave, and must be non-interchangeable with one another, barring modification. This is only a brief list of the numerous design drawbacks to this "open-ended" sync operation. To circumvent these shortcomings, a universal sync circuit has been developed with the following performance features and benefits:

— Sync any PWM to/from any other PWM
— Sync any PWM to/from any number of other PWMs
— Sync from digital levels for simple system integration
— Bidirectional sync signal
— Any PWM can be master or slave with no modifications
— Each control circuit will start and run independently of sync if sync signal is not present
— Localized ramp at Ct for slope compensation
— No critical frequency settings on each module
— High speed — minimum delays
— High noise immunity
— Low power requirements
— Remote off capability
— Minimal effect on frequency, duty cycle, and dead time
— Low cost and component count
— Small size

Sync Circuit Operating Principles

These optimal objectives can be obtained using a combination of both analog and digital signal inputs. The timing capacitor Ct input will be used as a summing junction for the analog sawtooth and digital sync input. The PWM is allowed to run independently using its own Rt and Ct components in standard configuration. When synchronization is required, a digital sync pulse will be superimposed on the Ct waveform.

When applied, the sync pulse quickly raises the voltage at Ct above the PWM comparator upper threshold. This forces a change in the oscillator charge/discharge status and operation. The oscillator then begins its normal discharge cycle synchronized to the sync signal. This digital sync pulse simply adds to the analog Ct waveform, forcing the Ct input voltage above the comparator upper threshold.

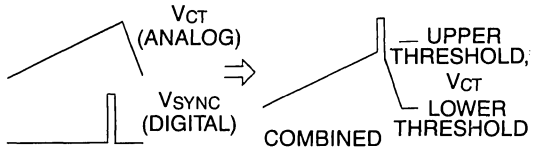


Figure 16.

In practice, this approach is best implemented by bringing Ct to ground through a small resistance, about 24 ohms. This low value was selected to have minimal offset and effects on the initial oscillator frequency. The sync pulse will be applied across the 24 ohm resistor. Since all PWMs utilize the timing capacitor in their oscillator section, it is both a convenient and universal node to work with.

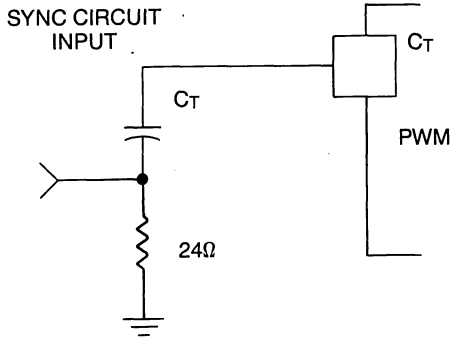


Figure 17. Sync Circuit Implementation

Oscillator Timing Equations

The oscillator timing components must be first selected to guarantee synchronization to the sync pulse. The sawtooth amplitude must be lower than the upper threshold voltage at the desired sync frequency. If not, the oscillator will run in its normal mode and cross the upper threshold first, before the sync pulse. This requirement dictates that the PWM oscillator frequency must be lower than the sync pulse frequency to trigger reliably. Typically, a ten percent reduction in free running frequency can be accommodated throughout the power supply. Adding the sync circuit will have minor effects on the PWM duty cycle, deadtime and ramp amplitude. (These will be examined in detail.)

9

The Timing Ramp

As mentioned, the timing ramp amplitude needs to be approximately ten percent lower in frequency than normal. Therefore, the MINIMUM sync pulse amplitude must fill the remaining ten percent of the peak-to-peak ramp amplitude to reach the upper threshold. Synchronization can be insured over a wide range of frequency inputs and component tolerances by supplying a slightly higher amplitude sync pulse.

Lowering the peak-to-peak charging amplitude also lowers the peak-to-peak discharge amplitude. This shortens the time required to discharge Ct since it begins at a lower potential. Consequently, this reduces the deadtime accordingly. However, the sync pulse width adds to the IC generated deadtime and increases the effective off, or deadtime due to discharge. This sync pulse width need only be wide enough to be sensed by the IC comparator, which is fairly fast. Additional sync pulse width increases deadtime which can be used to compensate for the 10% lower ramp, hence deadtime.

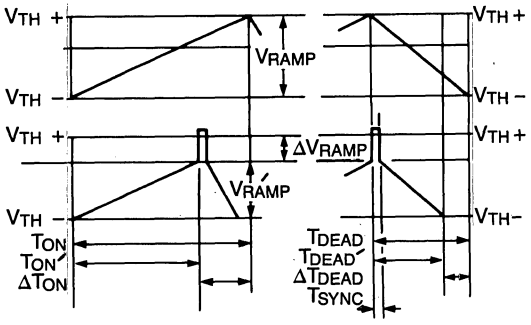


Figure 18. Oscillator Ramp Relationships

Oscillator Ramp Equations

The timing components required in the oscillator section are generally determined graphically from the manufacturers' data sheets for frequency and deadtime versus Rt and Ct. While fine for most applications, a careful examination of the equations is necessary to analyze the impacts of the additional sync circuit components on the timing relationships.

Oscillator Charging Ramp Equations

$$\Delta V\ osc = \frac{1}{Ct}\int I\ chg\ dT = \frac{I\ chg}{Ct}\Big]_0^t \quad T$$

$$T\ chg = \{\ \Delta V\ osc \bullet Ct\ \} / Ichg \quad \text{where } Ichg = Vchg / Rt$$

$$\Delta V\ osc = Vth\ upper - Vth\ lower$$

$$\Delta V\ osc' = \Delta V\ osc \frac{(tchg')}{t\ chg(o)} - V\ (24\ ohm)$$

$$V\ (24\ ohm) = I\ chg \bullet 24 = [Vchg / Rt] \bullet 24$$

These equations can be reduced if an approximation is made that the deadtime is very small in comparison to the total period. In this case, the entire effect of changing the ramp voltage is upon the charging time of the oscillator. Synchronizing to a higher frequency simply reduces the charging time of Ct, (Tchg). The new charging time (Tchg') is the original charge time multiplied by the change in frequency between F original and F sync. This relative change will be used in several equations; it is labelled P, for percentage of change.

$$\frac{T\ chg'}{T\ chg(o)} = \frac{T\ sync}{T\ orig} = \frac{F\ orig}{F\ sync} = P \text{ "relative F change"}$$

For small values of charging current, or large values of Rt, the voltage drop across the 24 ohm resistor is negligible. A current of 2 milliamps will result in a 2.5% timing error with a 2 volt peak to peak oscillator ramp at Ct. It is also preferrable to free-run the IC oscillator at about a 15% lower frequency than the synchronization frequency, where "P" = 0.85.

$$\Delta Vosc'\ (sync) = \Delta Vosc(o) \bullet P = 0.85 \bullet \Delta[Vosc]\ orig.$$

$$T\ chg' = T\ chg(o) \bullet P = 0.85\ T\ chg(o)$$

$$V\ sync\ (minimum)\ amplitude = \Delta\ [Vosc] \bullet (1\text{-}P)$$
$$= 0.15 \bullet \Delta\ [Vosc(o)]$$

With an approximate 2 volt peak to peak oscillator amplitude, the minimum sync pulse amplitude is 0.30 volts for synchronization to occur with a 15% latitude in frequencies.

Oscillator Discharge Ramp Equations

Proper deadtime control in the switching power stage is required to safeguard against catastrophic failures. Adding the sync circuit to the oscillator reduces the discharge time of the timing capacitor Ct, hence reducing the deadtime of the PWM. There are two contributing factors. First, the peak amplitude at the timing capacitor is lowered by ΔV osc(o) – ΔVosc', and the capacitor begins its discharge from a lower potential. Second, the 24 ohm resistor adds an offset voltage, dependent on its current. Typical IC discharge currents range from approximately 6 to 12 milliamps. This offset due to charging current (1-2 ma) is low in comparison to that of the discharge current (6 to 12 ma). While negligible during the charge cycle, its tenfold effects must be taken into account during the discharge, or deadtime.

The discharge time (T dchg) can be calculated knowing the discharge current of the particular IC. More convenient is to use the manufacturers' published deadtime listing for a known value of Ct, and to calculate the effects of the sync circuit. The discharge current has been averaged to 8 milliamps for brevity.

$$\Delta V\ dschg' = [\Delta Vdchg(o) \bullet P] - V\ (24\ ohm)$$
$$= [0.85 \bullet \Delta Vosc(o)] - 0.2\ volts$$

$$T\ dchg' = T\ dchg(o) - T\ loss\ (24\ ohms)$$
where T dchg(o) = initial deadtime from curve
$$= T\ dchg(o) \bullet [\Delta V\ dchg' / \Delta Vosc(o)]$$

The actual deadtime is a summation of both the discharge time of Ct and the width of the sync pulse. While being applied, the sync pulse disables the PWM outputs and must be added to the discharge time. The sync pulse width can be used to compensate for the "lost" deadtime, or as a deadtime extension.

T dead' = T dchg' + T sync pulse width

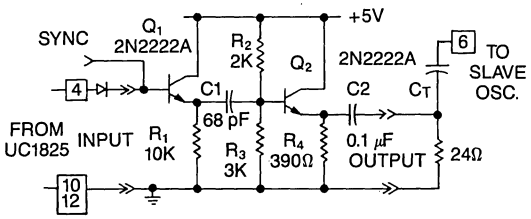
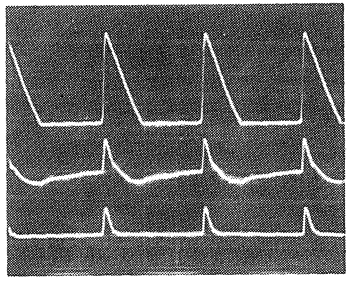


Figure 19. Sync Circuit Schematic

Operating Principles

A positive going signal is input to the base of transistor Q1 which operates as an emitter follower. The leading edge of the sync signal is coupled into the base of Q2 through capacitor C1, developing a voltage across R4 in phase with the sync input. This signal is driven through C2 to the slave timing capacitor and 24 ohm resistor network, forcing synchronization of the slave to the master. This high speed pulse amplifier circuit adds a minimum of delay (≈ 50 ns) between the master to slave timing relationship.



Top Trace:
Clock Input

Center Trace:
Base-to-Ground
Voltage at Q2

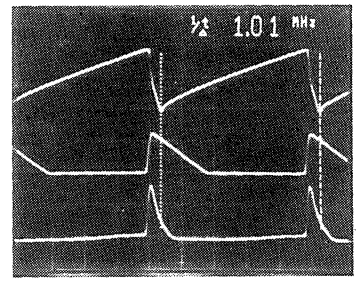
Bottom Trace:
Output Voltage
into 8 ohms

Vertical: 1 Volt/CM

Horizontal:
F OSC = 1 MHz

Figure 20. Sync Circuit Waveforms

This photo displays the waveforms of the sync circuit in operation at a clock frequency of 1 megahertz. The top trace is the circuit input, a 2.5 volt peak-to-peak clock output signal from the UC3825 PWM. Any of several other PWMs can be used as the source with similar results at lower frequencies. The center trace depicts the base to ground voltage waveform at transistor Q2, biased at 3 volts. The lower trace displays the output voltage across R4 while driving three slave modules, or about 8 ohms from the 5 volt reference.



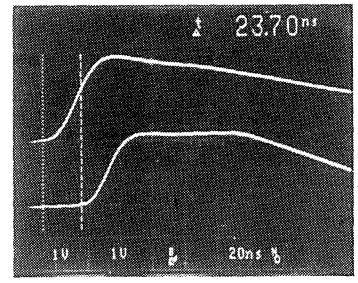
Top Trace:
Master :CT

Center Trace:
Clock Output

Bottom Trace:
V Sync Output

F OSC = 1 MHz

Figure 21. Circuit Timing Waveforms

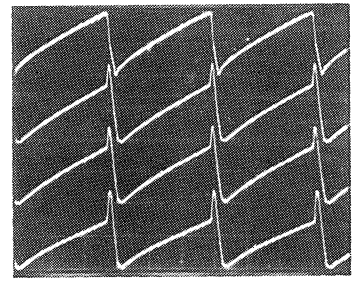


Top Trace:
Master Clock Output

Bottom Trace:
Slave Clock Output

Both: 1 V/CM, 20 ns/CM

Figure 22. Sync Circuit Delay; Input to Output



Trace 1: Master

Trace 2: Slave 1

Trace 3: Slave 2

Trace 4: Slave 3

Vertical: 1 V/CM All

Horizontal:
Fo = 1 MHz

Figure 23. Oscillator Waveforms: Master and Slaves

9

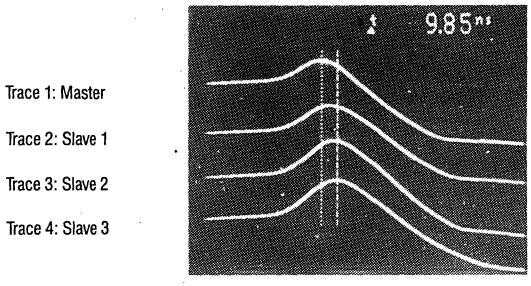


Figure 24. Typical Sync Delay at C_T: Master to Slaves

Synchronization ranges for the slaves were discussed in the previous text. The 1 volt sync pulse will accommodate most ranges in frequency due to manufacturers' tolerances. The following photo is included to display the outcome of trying to use the sync circuit on slaves with oscillator frequencies set beyond the sync circuit range. The upper trace is the master Ct waveform. The center trace is Ct of a slave free-running at approximately one half that of the master. The sync pulse alters the waveform, however does not bring it above the comparator's upper threshold to force synchronization. The lower trace shows a slave free running at approximately twice that of the master's oscillator. In this instance, the sync pulse forces synchronization at alternate cycles to the master.

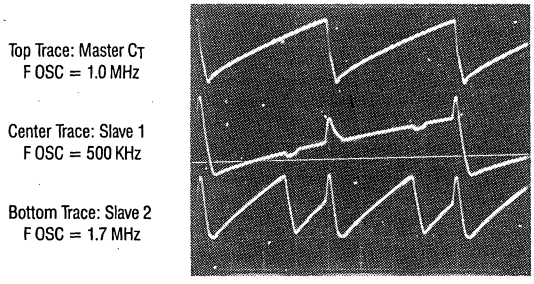


Figure 25. Nonsynchronous Operation

For voltage mode control, the free-running frequencies of the oscillator should be set as close to the master as tolerances will allow. One of the consequences of not doing so is the reduced amplitude of the Ct waveform, resulting in a lower dynamic range to compare against the error amplifier output. The top trace in the following photo shows that slave 1 has a much smaller ramp than slave 2, the lower trace. The amplitude should be made as large as possible to enhance circuit performance.

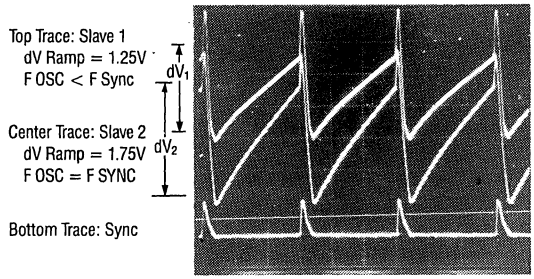


Figure 26. C_T Ramp Amplitude Waveforms

Sync Pulse Generation from the Oscillator Ct Waveform

Not every PWM IC is equipped with a sync output terminal from the oscillator. This is certainly the case with most low cost, mini-dip PWMs with a limited number of pin, like the UC1842/3/4/5. These ICs can provide a sync output with a minimum of external components.

Common to all PWMs of interest is the timing capacitor, Ct, used in the oscillator frequency generation. The universal sync circuit previously described triggers from the master deadtime, or Ct discharge time. A simple circuit will be described to detect this falling edge of the Ct waveform and generate the sync pulse required to the slave PWM(s).

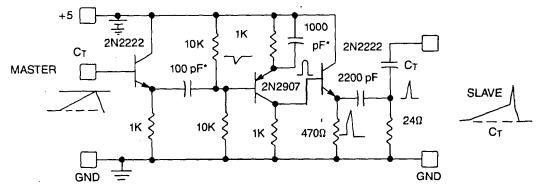


Figure 27. Sync Pulse Generator Circuit

Operating Principles

Transistor Q1 is an emitter follower to buffer the master oscillator circuit, and capacitively couples the falling edge of the timing waveform to the base of Q2. Since the rising edge of the waveform is typically ten or more times slower, it does not pass through to Q2, only the falling edge, or deadtime pulse is coupled. Transistor Q2 inverts this sync signal at its collector, which drives Q3, the power stage of this circuit. Similar to the universal sync circuit, the slave oscillator sections are driven from Q3's emitter. This circuit is useable to several hundred kilohertz with a minimum of delays between the master and slave synchronization relationship.

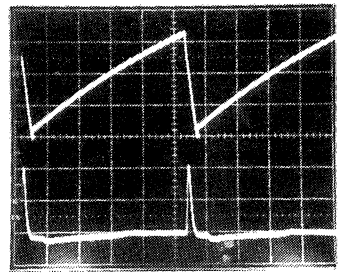


Figure 28. Operating Waveforms at 500 KHz

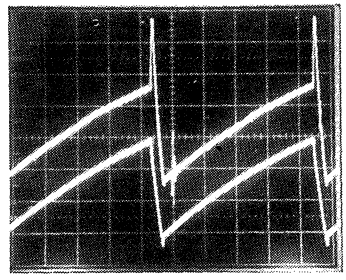


Figure 29. Master/Slave Sync Waveforms at C_T

IV. EXTERNALLY CONTROLLING THE PWM

Many of today's sophisticated control schemes require external control of the power supply for various reasons. While most of these requirements can be incorporated quite easily with a full functioned control chip, (typical of a 16 pin device), implementation may be more complex with a low cost, 8 pin PWM. Circuits to provide these functions with a minimum of external parts will be highlighted.

Shutdown

One of the most common requirements is to provide a complete shutdown of the power supply for certain situations like remote on/off, or sequencing. Typically, a TTL level input is used to disable the PWM outputs. Both voltage and current mode control ICs can perform this task by simply pulling the error amplifier output below the lower threshold of the PWM comparator of approximately 0.5 volts. This can be easily implemented via an NPN transistor placed between the E/A output and ground, used to short circuit the E/A output to zero volts. In most cases, this node is internally current limited to prevent failures.

Another scheme is to pull the current limit or current sense input above its upper threshold. A small transistor from this input to the reference voltage will fulfill this requirement.

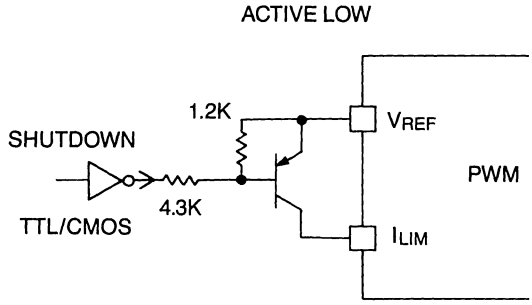


Figure 30. PWM Shutdown Circuits

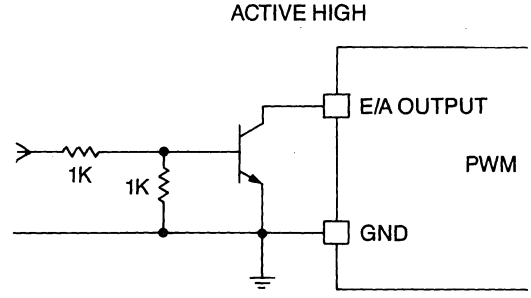
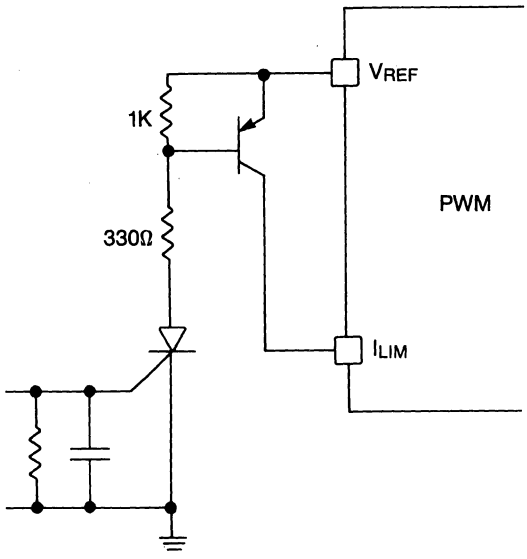


Figure 31.

Latching Shutdown

For those applications which require a latching shutdown mechanism, an SCR can be used in conjunction with the above circuits, or in lieu of them. The SCR can also be placed from the PWM E/A output to ground, provided the PWM E/A minimum short circuit current is greater than the maximum holding current of the SCR, and the voltage drop at I(hold) is less than the lower PWM threshold.

9

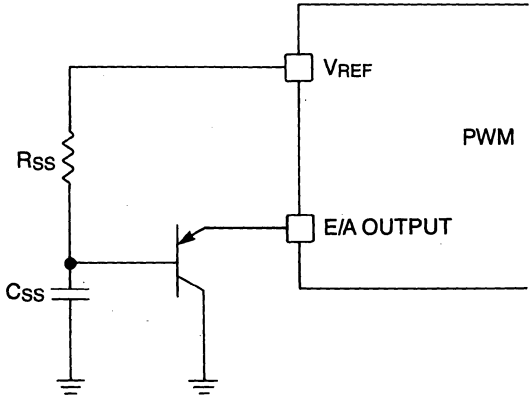


C. LATCHING

Figure 32.

Soft Start

Upon power-up, it is desirable to gradually widen the PWM pulse width starting at zero duty cycle. On PWMs without an internal soft start control, this can be implemented externally with three components. An R/C network is used to provide the time constant to control the I limit input or error amplifier output. A transistor is also used to isolate the components from the normal operation of either node. It also minimizes the loading effects on the R/C time constant by amplification through the transistors gain.



B. USING E/A

Figure 33.

Variable Frequency Operation

Certain topologies and control schemes require the use of a variable frequency oscillator in the controlling element. However, most PWMs are designed to operate in a fixed frequency mode of operation. A simple circuit is presented to disable the ICs internal oscillator between pulses, thus allowing variable frequency operation.

Internal at the ICs timing resistor (Rt) terminal is a current mirror. The current flowing through Rt is duplicated at the Ct terminal during the charge cycle, or "on" time. When the Rt terminal is raised to V ref (5 volts), the current mirror is turned off, and the oscillator is disabled. This is easily switched by a transistor and external logic as the control element, for example, a pulse generator. The PWM's timing resistor and capacitor should be selected for the maximum "ON" time and minimum "DEAD" time of the PWM output(s). The rate at which the PWM oscillator is disabled determines the frequency of the output(s).

The frequency can be varied in two distinct fashions depending on the desired control mode and trigger source. The "off" time of both outputs will occur on a pulse-by-pulse basis when the PWM outputs are OR'd to the trigger source. In this configuration either output initiates the "off" time, triggered by its falling edge. The PWM output A is activated, then both outputs A and B are low during the "off" time of the pulse generator. This is followed by output B being activated, then both outputs A and B low again during the next "off" time. This cycle repeats itself at a frequency determined by the pulse generator circuitry.

Another method is to introduce the "off" time after two (alternate A, then B) output pulses. Output A is activated, followed immediately by output B, then the desired "off" time. The pulse generator circuitry is triggered by the PWM's falling edge of output B. The specific control scheme utilized will depend on the power supply topology and control requirements.

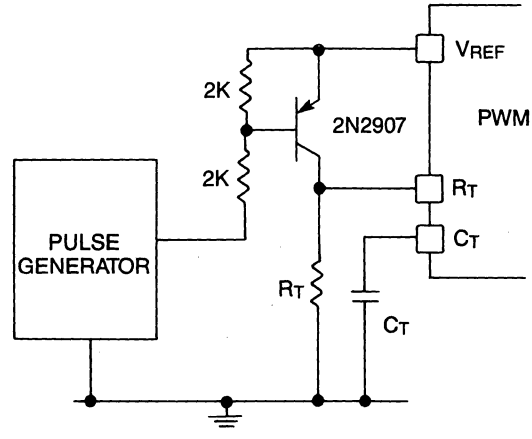


Figure 34. Oscillator Disable Circuit Variable Frequency Operation

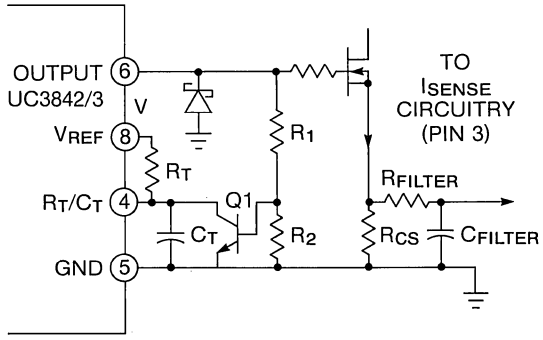
Fixed "Off-Time" Applications

Obtaining a fixed "off-time" and a variable "on-time" can easily be accomplished with most current-mode PWM IC's. In these applications, the Rt/Ct timing components are used to generate the "off-time" rather than the traditional "on-time." Implementation is shown schematically in Figure 3 along with the pertinent waveforms.

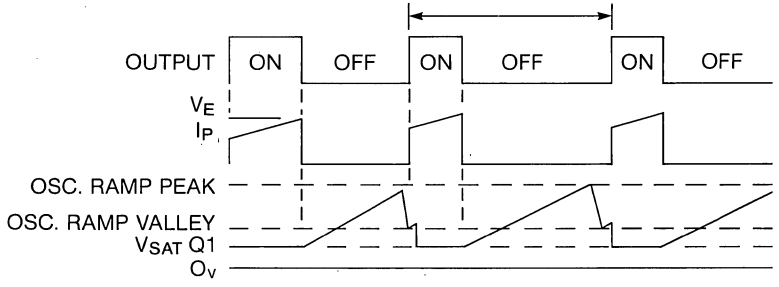
At the beginning of an oscillator cycle, Ct begins charging and the PWM output is turned on. Transistor Q1 is driven from the output and also turns on with the PWM output, thus discharging Ct and pulling this node to ground. As this occurs, the oscillator is "frozen" with the PWM output fully ON. On-time can be controlled in the conventional manner by comparing the error amplifier output voltage with the current sense input voltage. This results in a current controlled "on-time" and fixed "off-time" mode of operation. Other variations are possible with different inputs to the current sense input.

When the PWM output goes low (off), transistor Q1 also turns off and Ct begins charging to its upper threshold. The off-time generated by this approach will be longer for a given Rt/Ct combination than first anticipated using the oscillator "charging" equations or curves. Timing capacitor Ct now begins charging from Vsat of Q1 (approx. 0V) instead of the internal oscillator lower threshold of approximately 1 volt.

FIXED "OFF-TIME", CURRENT CONTROLLED "ON-TIME"



SCHEMATIC



WAVEFORMS

Figure 35.

9

Current Mode ICs Used in Voltage Mode

Most of today's current mode control ICs are second and third generation PWMs. Their features include high current output driver stages, reduced internal delays through their protection circuitry, and vast improvements in the reference voltage, oscillator and amplifier sections. In comparison to the first generation ICs (1524), numerous advantages can be obtained by incorporating a second or third generation IC (18XX) into an existing voltage mode design.

In duty cycle control (voltage mode), pulse width modulation is attained by comparing the error amplifier output to an artificial ramp. The oscillator timing capacitor Ct is used to generate a sawtooth waveform on both current or voltage mode ICs. To utilize a current mode chip in the voltage mode, this sawtooth waveform will be input to the current sense input for comparison to the error voltage at the PWM comparator. This sawtooth will be used to determine pulse width instead of the actual primary current in this method.

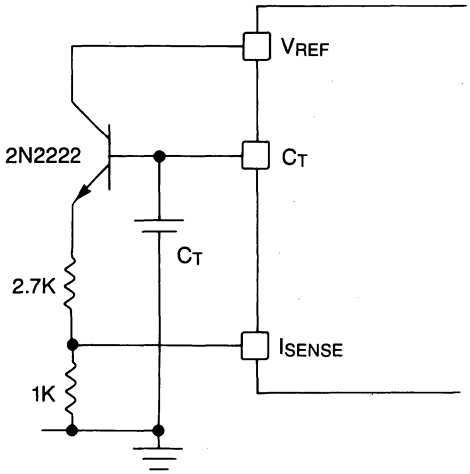


Figure 36. Current Mode PWM Used as a Voltage Mode PWM

Compensation of the loop is similar to that of voltage mode, however, subtle differences exist. Most of the earlier PWMs (15xx) incorporate a transconductance (current) type amplifier, and compensation is made from the E/A output to ground. Current mode PWMs use a low output resistance (voltage) amplifier and are compensated accordingly. For further reference on topologies and compensation, consult "Closing the Feedback Loop" listed in this appendix.

VI. FULL DUTY CYCLE (100%) APPLICATIONS

Many of the higher power (>500 watt) power supplies incorporate the use of a fan to provide cooling for the magnetic components and semiconductors. Other users locate fans throughout a computer mainframe, or other equipment to circulate the air and keep temperatures from skyrocketing. In either case, the power supply designer is usually responsible for providing the power and control.

The popularity of low voltage DC fans has increased throughout the industry due to the stringent agency safety requirements for high voltage sections of the overall circuit. In addition, it's much easier to satisfy dual AC inputs and frequency stipulations with a low cost DC fan, powered by a semi-regulated secondary output.

The most efficient way to regulate the fan motor speed (hence temperature) is with pulse width modulation. An error signal proportional to temperature can be used as the control voltage to the PWM error amplifier. While nearly full duty cycle can be easily attained, the circumstances may warrant full, or true 100% duty cycle.

This condition is highly undesirable in a switch-mode power supply, therefore most PWM IC designs have gone to great extent to prevent 100% duty cycle from occurring. There are simple ways to over-ride these safeguards, however. One method, presented below, "freezes" the oscillator and holds the PWM output in the ON, or high state when the circuit is activated. Feedback from the output is required to guarantee that the oscillator is stopped while the output is high. Without feedback, the oscillator can be nulled with the output in either state.

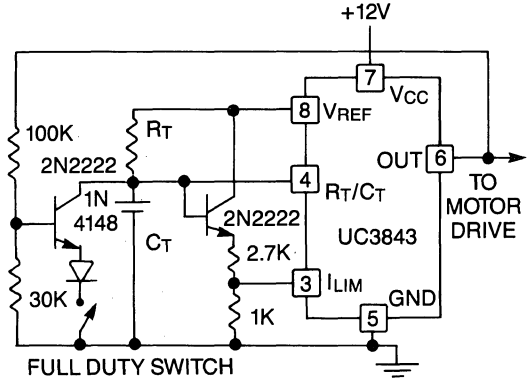


Figure 37. Full Duty Cycle Implementation

VII. HIGH EFFICIENCY START-UP CIRCUITS FOR BOOTSTRAPPED POWER SUPPLIES

Many pulse width modulator I.C.s have been optimized for offline use by incorporating an under-voltage lockout circuit. Demanding only a milliamp or two until start-up, the auxiliary supply voltage (V aux) can be generated by a simple resistor/capacitor network from the high voltage dc rail (+V dc). Once start-up is reached, the auxiliary power is supplied by means of a "boostrap" winding on the main transformer.

While the start-up requirements are quite low, losses in the resistor to the high voltage DC can be significant in steady state operation. This is especially true for low power (<35 watt) applications and circuits with high voltage rails (400 volts DC, for example). Once the main converter is running, switching the start-up resistor out of circuit would increase efficiency substantially. Circuits have been developed to use either bipolar or MOSFET transistors as the switch to lower the start-up circuit power consumption, depending on the application. Selection can be based on optimizing circuit efficiency (MOSFET) or lowest component cost (bipolar). The overall improvement in power supply efficiency suggests this circuitry is a practical enhancement.

The high efficiency start-up circuit shown in figure 1 utilizes two NPN bipolar transistors to switch the start-up resistor in and out of circuit. It can be used in a variety of applications with minor modifications, and requires a minimum of components. Figure 2 displays a similar circuit utilizing N channel MOSFET devices to perform the switching.

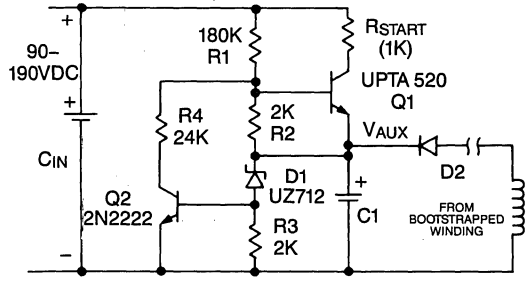


Figure 38. NPN Switches

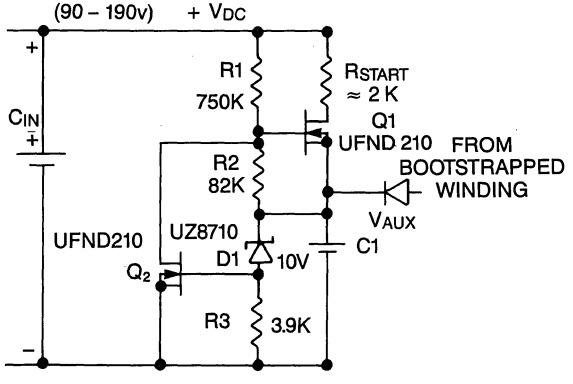


Figure 39.

Theory of Operation

Prior to applying the high voltage DC, capacitor C1 is discharged; switches Q1, Q2 and the main converter are off. As the input supply voltage (Vdc) rises, resistors R1 and R2 form a low current voltage divider. The voltage developed across R2 rises accordingly with +V dc until switch Q1 turns on, thus charging C1 thru R start-up from +V dc. This continues as the UV lockout threshold of the I.C. is reached and the main converter begins operation. Energy is delivered to C1 from the bootstrap winding in addition to that supplied through R start-up.

After several cycles, the auxiliary voltage rises with the main converters increasing pulse width, typical of a soft-start routine. Current flows through zener diode D1 and develops a voltage across the Q2's biasing resistor, R3. Transistor Q2 turns on when the auxiliary voltage reaches V zener plus Q2's turn on threshold. As this occurs, transistor Q1 is turned off, thus eliminating the start-up resistor from the circuit power losses. In most applications, the auxiliary voltage is optimized between 12 and 15 volts for driving the main power MOSFETs, while keeping power dissipation in the PWM IC low.

If the main converter is shut down for some reason, V aux will decay until Q2 turns off. Transistor Q1 then turns back on, and C1 is charged through R start-up from the high voltage DC, as during start-up.

VIII. CURRENT MODE HALF BRIDGE APPLICATIONS

As previously described (1), current mode control can cause a "runaway" condition when used with a "soft" centered primary power source. The best example of this is the half bridge converter using two storage capacitors in series from the rectified line voltage. For 110 VAC operation, the input is configured as a voltage doubler, and one of the AC inputs is tied directly to the storage capacitor's centerpoint. This is considered a "stiff" source, since the centerpoint will remain at one-half of the developed voltage between the upper and lower rail. However, during 220 VAC inputs, a bridge configuration is used for the input rectifiers, and the capacitors are placed in series with each other, across the bridge. Their centerpoint potential will vary when different amounts of charge are removed from the capacitors. This is generally caused by uneven storage times in the switching transistors Q1 and Q2.

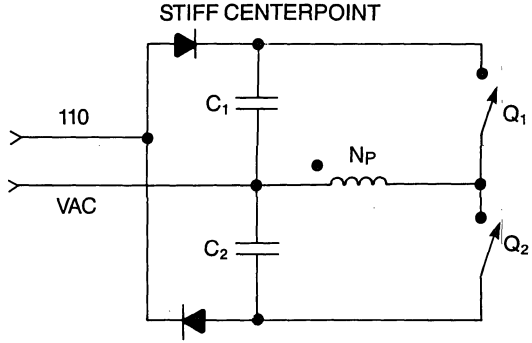


Figure 40.

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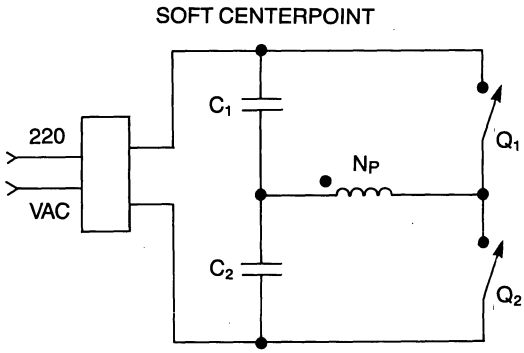

Figure 41.

The centerpoint voltage can be maintained at one-half +Vdc by the use of a balancing technique. In normal operation, transistor Q1 turns on, and the transformer primary is placed across one of the high voltage capacitors, C1 for example. On alternate cycles the transformer primary is across the other cap, C2. An additional balancing winding, equal in number in turns to the primary, is wound on the transformer. It is connected also to the capacitor centerpoint at one end and thru diodes to each supply rail at the other end. The phasing is such that it is in series with the primary winding through the ON time of either transistor Q1 or Q2.

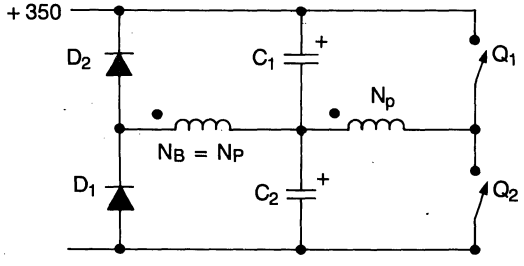

Figure 42. Schematic – Balancing Winding

In this configuration, the center point of the high voltage caps is forced to one-half of the input DC voltage by nature of the two series windings of identical turns. Should the midpoint begin to drift, current flows thru the balancing winding to compensate.

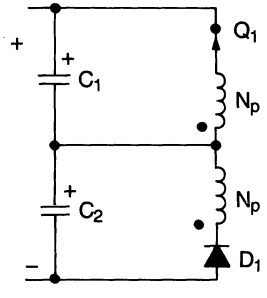

Figure 43. Transistor Q1 On

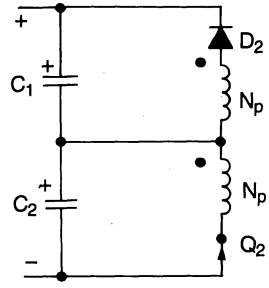

Figure 44. Transistor Q2 On

In most high frequency MOSFET designs, the FET mismatches are small, and the average current in the balancing winding is less than 50 milliamps. A small diameter wire can be wound next to the larger sized primary for the balancing winding with good results.

IX. PARALLELING CURRENT MODE MODULES

One of the numerous advantages of current mode control is the ability to easily parallel several power supplies for increased output power. This discussion is intended as a primer course to explore the basic implementation scheme and design considerations of paralleling the power modules. Redundant operation, failure modes and their considerations are not included in this text.

The prerequisites for parallel operation are few in number, but important to insure proper operation. First, each power supply module must be current mode controlled, and capable of supplying its share of the total output power. All modules must be synchronized together, and one unit can be designated as the master for the sake of simplicity. All remaining units will be configured as slaves.

The master will perform one function in addition to generating the operating frequency. It provides a common error voltage (Ve) to all modules as the input to the PWM comparator. This voltage is compared to the individual module's primary current at its PWM comparator. The slaves are utilized with their error amplifier configured in unity gain. Assume there are identical primary current sense resistors in each module, and no internal offsets in the ICs amplifiers or other circuit components. In this case, the output voltages and currents of each module would be identical, and the load would be shared equally among the modules.

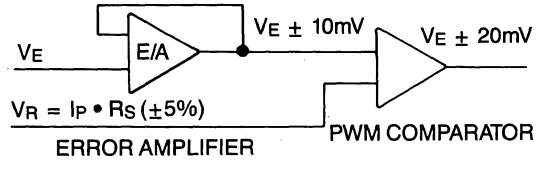

Figure 45. PWM Diagram

In reality, small offets of ±10 millivolts exist in each PWM amplifier and comparator. As the common error voltage, (Ve) traverses through the IC's circuitry, its accuracy decreases by the number and quality of gates in its path. The maximum error occurs at the lowest common mode amplifier voltage, approximately 1 volt. The ±20 millivolt offset represents a ±2% error at the PWM comparator. At higher common mode voltages, typical of full load conditions, the error voltage (Ve) is closer to its maximum of 4 volts. Here the same ±20 millivolts introduces only ±0.5% error to the signal.

The other input to the PWM comparator, Vr, is the voltage developed by the primary current flowing through the current sense resistor(s). In many applications, a 5% tolerance resistor is utilized resulting in a ±5% error at the PWM comparator's "current sense" or ramp input.

Pulse width is determined by comparing the error voltage (Ve) with the current sense voltage, (Vr). When equal, the primary current is therefore the error voltage divided by the current sense resistance; Ip = Ve/Rs. Output current is related to the primary current by the turns ratio (N) of the transformer. Sharing of the load, or total output current is directly proportional to the sharing of the total primary current. The previous equations and values can be used to determine the percentage of sharing between modules.

Primary current, Ip = Ve/Rs. Introducing the tolerances, Ip' = Ve (±2%) / Rs (±5%); therefore Ip' = Ip (±7%) The primary currents (hence output currents) will share within ±seven percent (7%) of nominal using a five percent sense resistor. Clearly, the major contribution is from the current sense circuitry, and the PWM IC offsets are minimal. Balancing can be improved by switching to a tighter tolerance resistor in the current sense circuitry.

The control-to-output gain (K) decreases with increasing load. At high loads, when primary currents are high, so is the error amplifier output voltage, (Ve). With a typical value of four volts, the effects of the offset voltages are minimized. This helps to promote equal sharing of the load at full power, which is the intent behind paralleling several modules.

For demonstration purposes, four current mode push-pull power supplies were run in parallel at full power. The primary current of each was measured (lower traces) and compared to a precision 1 volt reference (upper trace). The voltage differential between traces is displayed in the upper right hand corner of the photos. Using closely matched sense resistors, the peak primary currents varied from a low of 2.230A to 2.299 amps. Calculating a mean value of 2.270 amps, the individual primary currents shared within two percent, indicative of the sense resistor tolerances.

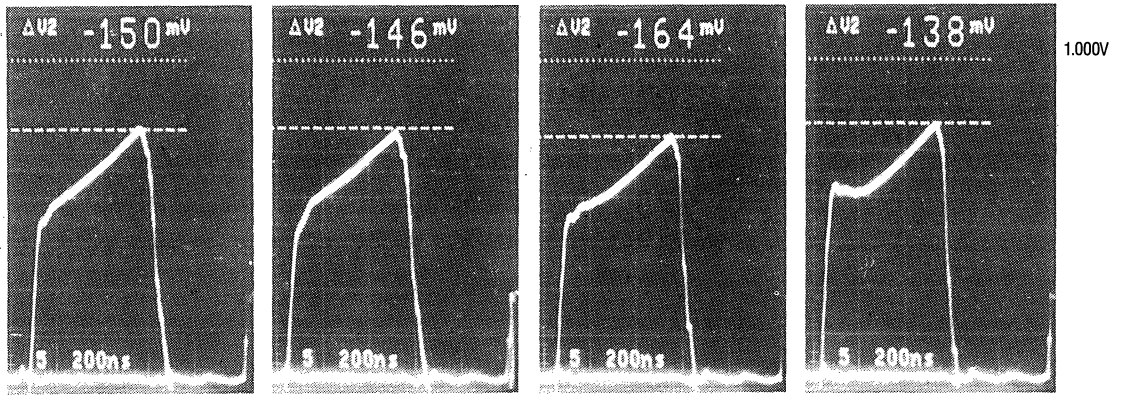

Figure 46. Primary Currents – Parallel Operation

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Other factors contributing to mismatch of output power are the individual power supply diode voltage drops. The output choke inductance reflects back to the primary current sense, and any tolerances associated with it will alter the primary current slope, hence current. In the control section, the peak-to-peak voltage swing at the timing capacitor Ct effects the amount of slope compensation introduced, along with the tolerance of the summing resistor. These must all be accounted for to calculate the actual worst case current sharing capability of the circuit.

Top Trace:
V_E: Error Voltage with Noise

Lower Trace:
V_R: Primary Current

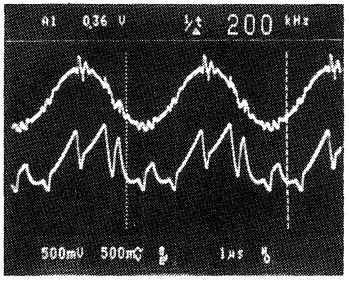

Figure 47. Noise Modulating V_E

Proper layout of all interconnecting wires is required to insure optimum performance. Shielded coax cable is recommended for distributing the error voltage among the modules. Any noise on this line will demonstrate its impact at the PWM comparator, resulting in poor load sharing, or jitter. Cables should be of equal length, originating at the master and routed away from any noise sources, like the high voltage switching section. All input and output power leads should be exactly the same length and wire gauge, connected together at ONE single point. Leads should be treated as resistors in series with the load, and deviations in length will result in different currents delivered from each module.

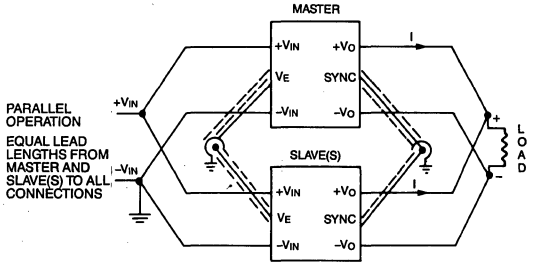

Figure 48.

A HIGH PRECISION PWM TRANSCONDUCTANCE AMPLIFIER FOR MICROSTEPPING USING UNITRODE'S UC3637

INTRODUCTION

If you ask a designer why he has chosen a stepping motor for a given application, chances are that his answer will include something about "open loop positioning." Stepping motors can provide accurate positioning without expensive position sensors and feedback loops, and this fact alone results in large savings.

But there is more: steppers are tough and durable, easy to use, and high in power rate. And if you want to close a feedback loop around them, you can do that, too.

Still, there are certain problems. Steppers are *incremental motion* machines, and as such they tend to be noisy and are prone to behave erratically under certain conditions; for example, when the stepping rate is such as to excite a mechnical or electro-mechanical resonant mode. Furthermore, although the angular increments may be small—especially when half-stepping is used—the positioning resolution is restricted to a finite number of discrete points.

Therefore, this question arises: "Is there a method of driving stepping motors such that the resulting movement is smooth and quiet—that is, essentially continuous, as opposed to incremental? And would this result in improved positioning resolution?" We will try to answer these questions here.

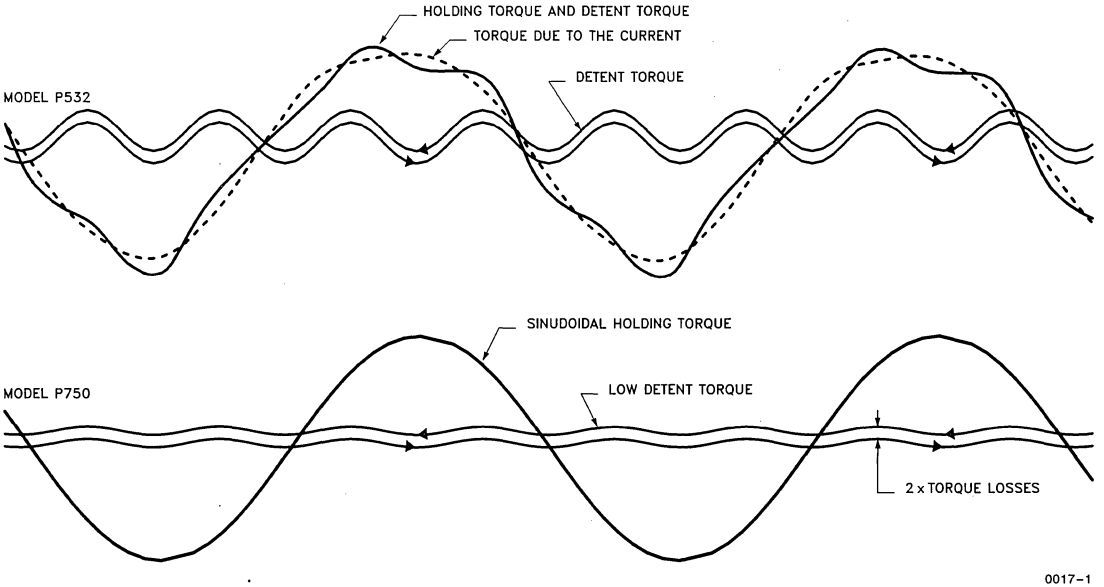

Figure 1. Static Torque Curves of Two Hybird Steppers

STATIC TORQUE CURVES

The curves in Figure 1 illustrate how a stepping motor torque behaves as a function of rotor angle. The detent torque component is a consequence of the magnetic field produced by the rotor magnet (or magnets), and is present with or without phase currents applied. It can be seen that this component contributes a fourth harmonic distortion to the static torque curves. The energized torque curves, in general, have additional harmonic components, mostly the third and fifth. Note that the two motors depicted in Figure 1 have very different characteristics in this respect. The distortion observed in the static torque characteristic is of no great consequence in the more usual applications of stepping motors, using either full step or half step sequences. It is when we start thinking about increasing the positioning resolution of these motors by some method of apportioning currents between the two phases, that we begin to be concerned about the effects of harmonic distortion. Even small amounts of added har-

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monics can have a very noticeable effect on the waveshape, as shown in Figure 2.

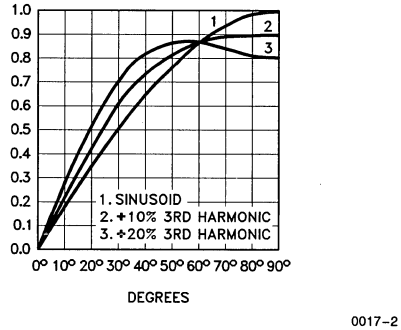

Figure 2. Effect of 10% and 20% Harmonic Content

Figure 3 shows the relationship between sine and cosine waveforms, and what it tells us is that if we can get a motor with a sinusoidal static torque characteristic—i.e., with no harmonic components—and drive phase A with a sine current function and phase B with a cosine current function, we would have smooth shaft rotation and accurate positioning at any angle.

Stepping motors having static torque curves with very low harmonic distortion are commercially available today. But most low-priced, mass produced hybrid steppers exhibit torque curves with enough harmonic components to require careful consideration in any attempt to improve resolution by what is known as *microstepping*. (The name *microstepping* originates from the fact that the required current waveforms are generated by a digital process that aproximates those waveforms incrementally. With thirty-two or sixty-four increments for an electical angle of $\pi/2$ radians, the resulting waveforms are hardly distinguishable from true sine or cosine signals.)

If the nonsinusoidal static characteristic of a given motor is known, it is possible to generate appropriate waveshapes for the phase currents so that the resulting torque curve becomes free of distortion, as required. Note that this involves no additional complexities, since it is just as easy—or difficult—to synthesize one waveform as another. Consequently, one can, in principle, linearize any motor for increased resolution and smoothness through microstepping.

Still, it should be noted that the best efficiency is obtained when the phase current waveshapes are undistorted, because of all suitable waveforms, the sine wave has the lowest form-factor.

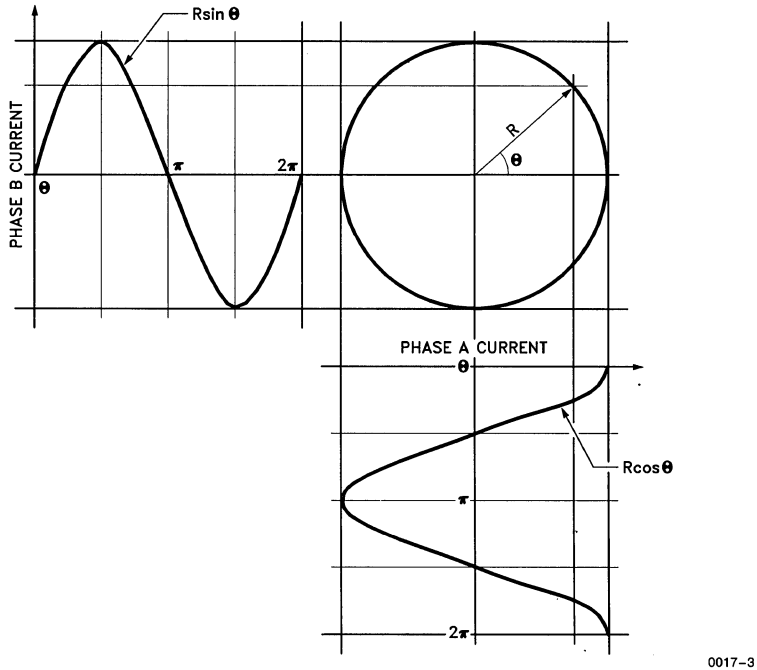

Figure 3. The sum of sine and cosine waveforms is a smoothly rotating vector.

The form-factor of a waveform is the ratio if its rms to average values. For a sine wave, this ratio is:

$$(1)\ ff_S = \frac{0.707}{0.637} = 1.111$$

Some manufacturers have used triangular waveforms—largely because they can be implemented with great simplicity—and it is interesting to note that for such a waveform, the average value is 0.5 V_{PK}, while the rms is 0.577 V_{PK}. Thus the form factor is:

$$(2)\ ff_T = \frac{0.577}{0.5} = 1.155$$

As a consequence, for the same peak power applied to the motor, the rms power of a triangular waveform is 18% less than that of a sine wave, whereas the average current is 21% less. It follows that microstepping with a triangular waveform does not use the full capabilities of the motor.

The same result is obtained with other-waveforms, as long as the peak power is limited, as it must be.

But regardless of all this, the fact remains that whether our motor has a sinusoidal torque curve or a very distorted one, the thing that will be inevitably required will be two amplifiers capable of converting the synthesized waveform into phase currents *at the required power levels*. In the next section, we will describe the design of one such amplifier, having a transconductance linearity of better than 1% and capable of delivering phase currents of up to ±6A.

UNITRODE'S UC3637 PWM CONTROLLER

Pulse width modulation (PWM) is a method of power control whose most attractive feature is the high level of efficiency that can be obtained. With careful design, and using power MOSFETs as output switches, one can easily achieve efficiencies higher than 80%.

The Unitrode UC3637 PWM controller, housed in an eighteen-pin DIL package, was originally intended to serve as a PWM amplifier for brush-type PM servomotors. But, because of its ingenious design, the device has found its way into various other uses as well, such as temperature control, uninterruptible power supplies, and even high fidelity sound reproduction. As we shall see, it can also be used in a high performance PWM transconductance amplifier.

BLOCK DIAGRAM AND LOOP EQUATIONS

A block diagram of the current feedback loop under consideration is shown in Figure 4, where the UC3637 is seen to contain the high-gain error amplifier and the main ingredients of the PWM amplifier. Since we are looking for an output of 6A, an H-bridge power stage must be added. The motor current I_M is sensed by means of a low value resistor R_S, and the derived voltage V_C is used to complete the feedback loop. Not shown in the block diagram is the back-EMF voltage, the product of motor shaft speed and K_V, the motor speed constant. Since this term does not contribute to the dynamics of the current feedback loop, it has purposely been left out.

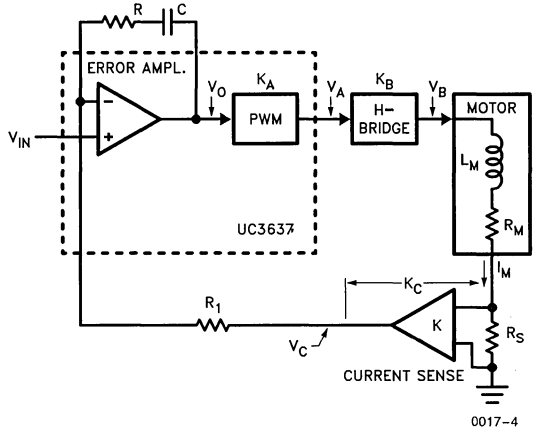

Figure 4. Block Diagram of the Complete Current-Control Loop

The transfer functions of the error amplifier and motor are as follows:

$$(3)\ \frac{V_O}{V_C} = -\frac{1 + sRC}{sR_1C}$$

$$(4)\ \frac{I_M}{V_B} = \frac{1}{R_M(1 + sTm)}$$

where $T_M = L_M/R_M$, the motor's electrical time-constant (R_S is assumed to be low compared with R_M). The forward transfer function is, then:

$$(5)\ G(s) = \frac{-K_A K_B (1 + sRC)}{sR_1R_MC(1 + sTm)}$$

For the feedback transfer functions, we have simply:

$$(6)\ H(s) = \frac{V_C}{I_M} = K_C$$

Thus, for the closed loop,

$$(7)\ \frac{I_M}{V_{IN}} = \frac{K_A K_B (1 + sRC)}{K_AK_BK_C(1 + sRC) + sR_1R_MC(1 + sTm)}$$

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If we make the time-constant RC equal to the motor's time-constant T_M, this becomes:

$$(8)\ \frac{I_M}{V_{IN}} = \frac{K_A K_B}{K_A K_B K_C + sR_1 R_M C}$$

$$(9)\ \frac{I_M}{V_{IN}} = \frac{1}{K_C(1 + sT_1)}$$

where,

$$(10)\ T_1 = \frac{R_1 R_M C}{K_A K_B K_C} = \frac{R_1 L_M}{K_A K_B K_C R}$$

By making $RC = T_M$, we have eliminated one of the transfer function poles. The resulting closed-loop response, described by (7) has a gain of $1/K_C$ from $\omega = 0$ to $\omega = 1/T_1$, and drops at -6 bd/octave thereafter.

DESIGNING THE HARDWARE

In designing circuits intended to handle power, it is customary to start with the output stage. This is surely due to the fact that the power stage is more demanding of the designer's attention and care, whereas the low level circuits are far more adaptable to the requirements of the chosen output configuration.

In the present case, power MOSFETs were chosen for the H-bridge because of their low losses, and because of their compatibility with the UC3637 outputs. Each totem-pole leg of the bridge is made up of one N-channel and one P-channel device. Such a pair can be driven in many different ways, of which several were considered for this particular design. The method that was finally chosen, shown in Figure 5, requires a few comments.

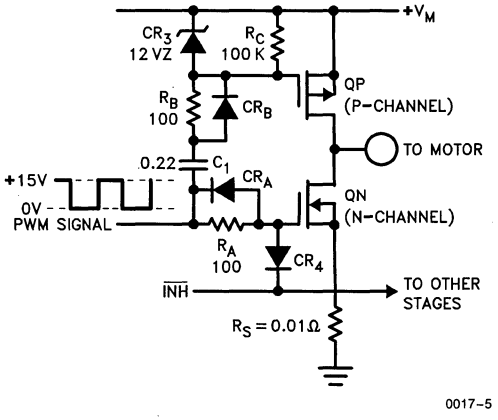

Figure 5. Totem-Pole Leg of Output H-Bridge

The first thing to notice is that the upper MOSFET, transistor QP, has its gate driven through a capacitor, C_1. This is not always practical of course, but in the case of a chopper drive combined with a stepping motor, it turns out that a driving signal is always present. At stand-still and at low speeds, it is the chopping rate that appears; at higher speeds, it is the stepping rate itself, or both. The driver is never required to deliver continuous DC (unchopped) to the motor winding, as it would to the armature of a brush-type DC motor at full speed. Consequently, QP never needs to be held in the ON state for more than a few microseconds, and for this the time constant of C1 R4 is adequate. Also, resistor R_A in parallel with CR_1, together with the gate capacitance of QN, cause this transistor to turn off faster than it turns ON. Since the same thing is done for QP, the problem of cross-conduction is neatly taken care of. The Zener diode CR3 serves as a clamp for the QP gate voltage. Finally, an inhibiting line, INH, is provided as a protection for QP and QN during the power turn-on time, when the $+V_M$ voltage is rising and C1 must be charged. An auxiliary circuit senses a positive dV_M/dt and holds the INH line low, thus keeping QN OFF during this time.

An important point in favor of this arrangement is that the gate-drive circuit losses are independent of V_M and so this voltage can be set anywhere within the Vds rating of the power MOSFETs.

We can now consider the H-bridge with its motor winding load, as shown in Figure 6. The bridge is shown schematically with its driving circuits, but the action is still as shown in Figure 5. For example, when V_{IN} is high, switch S1 is OFF and S3 is ON, and so forth. Furthermore, the opposite side of the bridge is driven by the complementary signal V_{IN}. With V_{IN} low, S1 and S4 will be conducting, and the load current I_M will increase in the positive direction (indicated by the $+I_M$ arrow). Similarly, when V_{IN} is high, both S2 and S3 conduct, causing I_M to increase in the negative direction. Remember that the load is inductive, and that inductance is an energy storing element. Therefore, if we have some positive I_M, due to S1 and S4 being closed, and we switch to S2 and S3 closed, the previous value of I_M will continue to flow "uphill," so to speak, while decreasing. At the time of switching, this current ceases to flow down through sense resistor R_{S4} to ground and starts flowing up through R_{S3} and back to the supply.

Switches S1 through S4 are able to conduct in either direction when in the ON state—a very neat feature of power MOSFETs. Furthermore, their intrinsic diode protects the devices from reverse voltage pulses during the switching no-overlap transition. Since we wish to control this current very closely in both magnitude and direction, it is

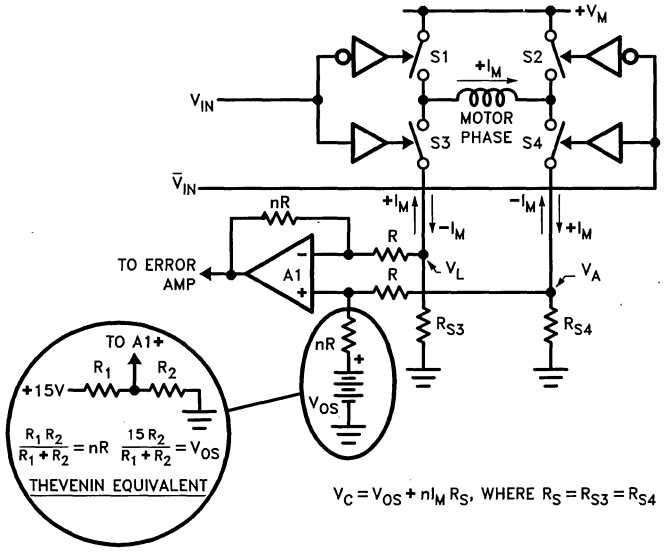

Figure 6. H-Bridge Configuration with Bidirectional Current Sensing

now necessary to generate a voltage V_C that gives an accurate indication of the current I_M over the full range from maximum positive to maximum negative. This is done by the circuit section of Figure 6 which includes the op-amp A1.

In that circuit, the voltage V_{OS} is meant to offset the output V_C of A1 to some chosen value that will correspond to $I_M = 0$. The value of V_C can be written as:

(11) $V_C = V_{CS} + nI_MR_S$

This offset is necessary when the design requires a single polarity supply, as in our case. When two supply polarities are available for the control circuit, one can simply make $V_{OS} = 0$. For the single supply case, the nR and V_{OS} combination is implemented by a simple resistor divider from $\pm V_{CC}$ to ground (a Thevenin equivalent) of the required impedance and open voltage.

To keep the circuit losses to a minimum, we should use low values for the sense resistors R_{S3} and R_{S4}. Yet, they need to be accurate and temperature-stable. In our case, having decided on a V_C scale of 0.5V per motor ampere, we have selected $R_S = 0.1\Omega$ and a current sense amplifier gain $n = 5$. We have also set $V_{OS} = V_{CC}/2 = 7.5V$, so that we will have $V_C = 7.5 + 0.5\ I_M$. This means that as the current I_M varies from $+6A$ to $-6A$, the analog voltage V_C will vary from $+10.5V$ to $+4.5V$. At $I_M = 0$, V_C will be equal to 7.5V.

SETTING UP THE PWM CONTROLLER

Having designed the power output stage (H-bridge) and the current-sense circuit, we can proceed to the PWM controller (UC3637) and its external components. The device itself has been described in great detail in its data sheet and in an application note (Publication U-102, available from Unitrode Integrated Circuits Corporation).

In the present design, we use the UC3637 to generate the two H-bridge driving signals V_{IN} and $\overline{V_{IN}}$, at the device's output pins 7 and 4, respectively.

Figure 7 shows in block form the internal workings of the device. Since operation from a single $+15V$ supply is desired, pin 5 will be GROUND and pin 6 will be $+15V$. We selected, for the ramp oscillator, a waveform as shown in Figure 8, which fits well in the $+15V$ headroom given by our V_{CC} supply. The formulas given in Figure 8 show how the various components are calculated.

Next, we set up the two PWM comparators by tying the inverting inputs (pin 10) of the A comparator, and the noninverting input (pin 8) of the B comparator together and apply the ramp (pin 2) to this line. The remaining comparator inputs (pins 9 and 11) are next connected together to become the PWM input point. It can be seen from the block diagram of Figure 7 that as the control voltage applied to this point varies from $+5V$ to $+10V$, the duty cycle of the output at pins 4 and 7 also varies. V_4 and V_7 are complementary signals; and the voltage swing of each of these signals is from a low value between 0V and $+2V$, and a high value between ($V_{CC} - 2V$) and V_{CC}.

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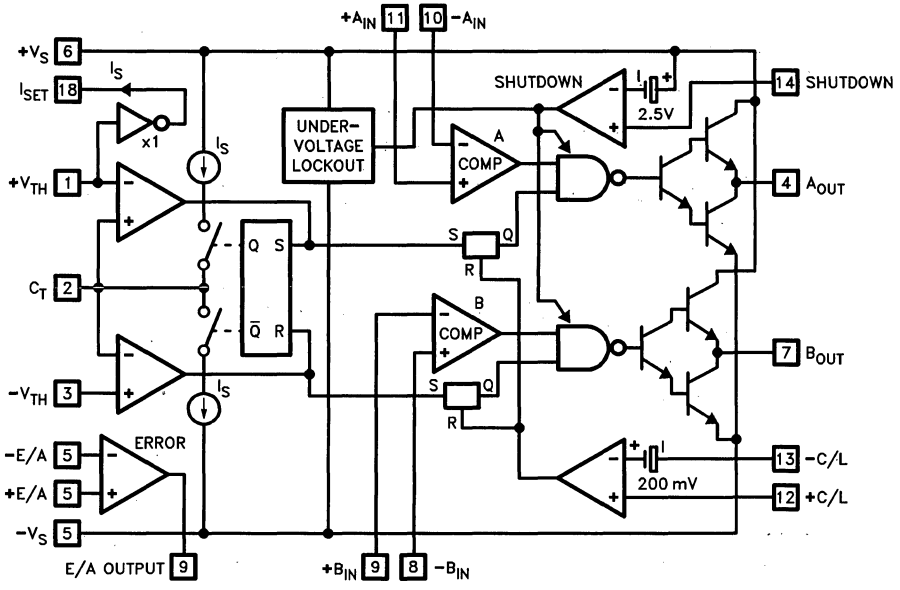
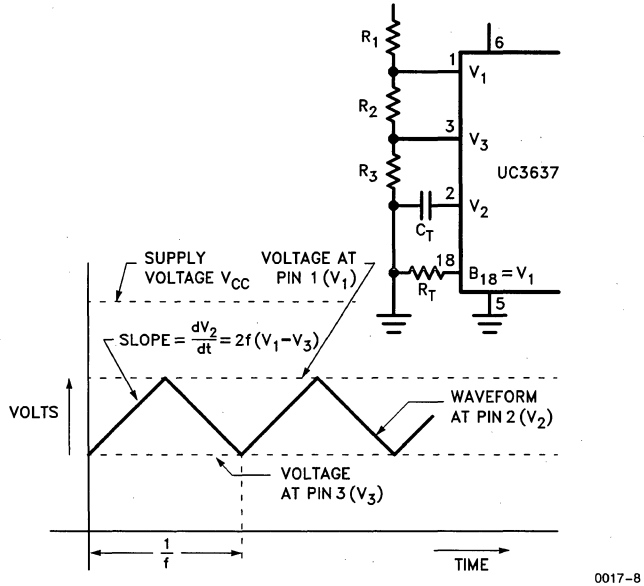


0017-7

Figure 7. Block Diagram of the UC3637. The two outputs can drive power MOSFETs directly.



0017-8

f = ramp frequency

$I_T = \frac{V_{18}}{R_T} = \frac{V_1}{R_T}$ (should be about 0.5 mA)

then, $R_T = 2000\ V_1\ (\Omega)$

$C_T = \frac{250 \times 10^{-6}}{f(V_1 - V_3)}(fd)$

Figure 8. Setting up the ramp oscillator requires only five external components.

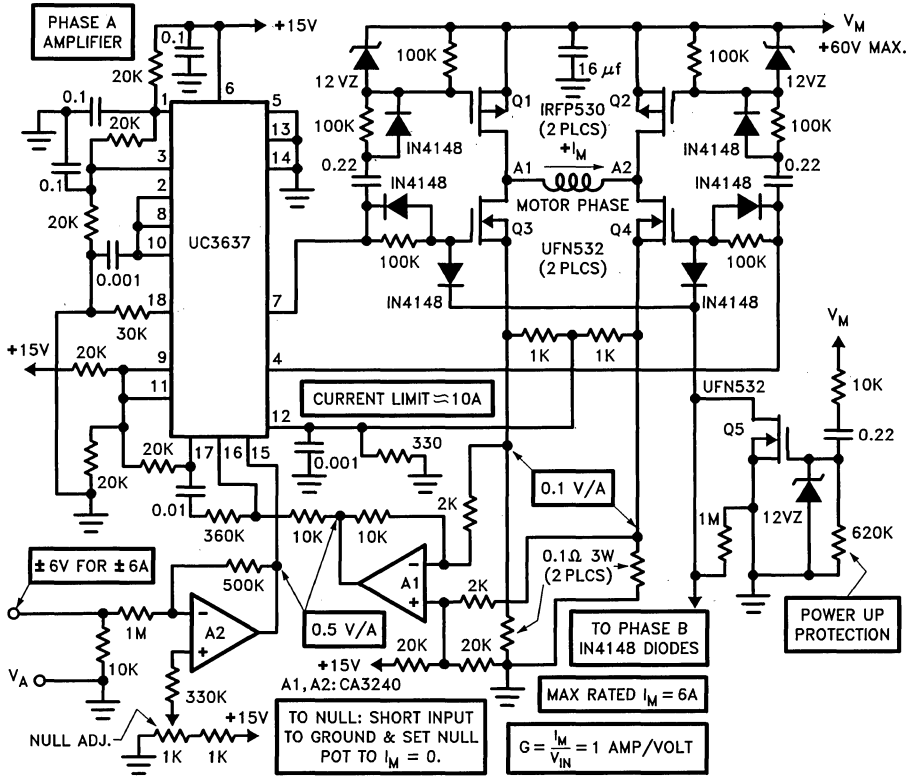


Figure 9. PWM Transconductance Amplifier UC3637

The error amplifier is used as a source for the control signal. But because its output (pin 17) has a voltage range greater than the +5V to +10V range of the V_C ramp signal, and we want to prevent the modulation range from ever reaching 0% or 100% (because of the capacitively coupled P-channel MOSFET devices) we add a simple resistive network consisting of three equal resistors to serve as an attenuator. The final result can be seen in the complete schematic of Figure 9.

CURRENT LIMIT AND CONTROL

The current limit feature of the UC3637 is used to protect the output transistors and motor from excessive current (6A in this case). As the block diagram of Figure 7 shows, the current limit comparator (pins 12 and 13) of the UC3637 is internally biased to a threshold of 200 mV. The network that connects the two sense resistors to pin 12, consisting of two 1K and one 330Ω resistors, causes a voltage of 200 mV to appear at pin 12 when the voltage at either sense resistor is about 1V, corresponding to a current of 10A. Consequently, the maximum output current will be limited to 10A. The current feedback loop is closed by feeding the output of the current sense amplifier to pin 16, the inverting input of the error amplifier of the UC3637. An RC time constant of 3.6 msec is used for the zero in this amplifier's transfer function (equations 8, 9, and 10) which is close to the effective electrical time constant of the motor. Also, a level-shift circuit is provided by means of op amp A2 to permit the use of a control input centered at zero volts, and a control range from −6A to +6A. The circuit allows this even though the op amp is powered by a single positive supply.

TEST RESULTS

The design circuit, shown in Figure 9, was breadboarded for testing at Unitrode and also at Portescap. The assembly includes two amplifiers, one for each motor phase and a "power on" auxiliary circuit for protection of the power MOSFETs. The output devices are equipped with small sheet metal heat sinks, and runs cool at all times.

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The circuit draws about 65 mA from the +15V supply. The power output section operates with a supply ranging from +20V to +60V, with no damage occurring if this voltage is lower than +20V.

The circuit performed very well, with excellent linearity and phase matching. The various plots taken, showing output current versus input voltage, are quite straight, and the transconductance is accurate to within 1%, except for a small deviation at about 3.5V, caused presumably by an instability due to the hurried breadboard layout. Furthermore, the PWM frequency was subsequently increased to slightly above 100 KHz (by reducing C_T) and the performance re-checked. The result was a marked increase in motor efficiency, due to reduced current ripple, with all other results remaining excellent.

CONCLUSION

Microstepping is a technique of considerable interest in the design of many products, particularly those in which the lower cost of open-loop positioning is an essential parameter. A motor such as Portescap's Model P-750, with its accurately sinusoidal torque curve, becomes even more attractive once its microstepping driver is shown to be fairly simple and inexpensive. The end result is not only precise open loop positioning, but quiet operation, freedom from resonance problems, and excellent electrical efficiency. Incidentally, the motor is available with two quadrature speed sensing coils that can be used for speed and position control, if desired.

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DESIGN NOTES ON PRECISION PHASE LOCKED SPEED CONTROL FOR DC MOTORS

ABSTRACT

There are a number of high volume applications for DC motors that require precision control of the motor's speed. Phase locked loop techniques are well suited to provide this control by phase locking the motor to a stable and accurate reference frequency. In this paper, the small signal characteristics, and several large signal effects, of these loops are considered. Models are given for the loop with design equations for determining loop bandwidth and stability. Both voltage and current motor drive schemes are addressed. The design of a loop for a three phase brushless motor is presented.

PHASE LOCKING GIVES PRECISION SPEED CONTROL

The precise control of motor speed is a critical function in today's disc drives. Other data storage equipment, including 9 track tape drives, precision recording equipment, and optical disc systems also require motor speed control. As the storage density requirements increase for these media, so does the precision required in controlling the speed of the media past the read/write mechanism. One of the best methods for achieving speed control of a motor is to employ a phase locked loop.

With a phase locked loop, a motor's speed is controlled by forcing it to track a reference frequency. The reference input to the phase locked loop can be derived from a precision crystal controlled source, or any frequency source with the required stability and accuracy. A block diagram of the phase locked loop is shown in Figure 1.

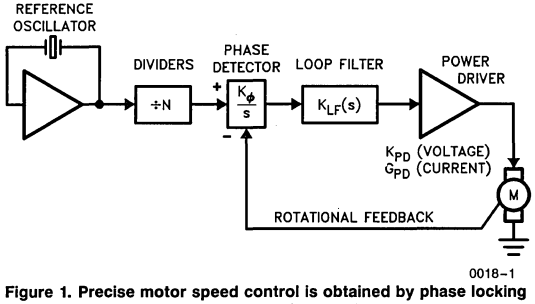

Figure 1. Precise motor speed control is obtained by phase locking the motor to a precision reference frequency.

In Figure 1, a precision crystal oscillator's frequency is digitally divided down to provide a fixed reference frequency. Alternatively, the motor could be forced to track a variable frequency source with zero frequency error. The motor speed is sensed by either a separate speed winding or, particularly in the case of the DC brushless motor, a Hall effect device. The two signals, motor speed and reference frequency, are inputs to a phase detector. The detector output is a voltage signal that is a function of the phase error between the two inputs. The transfer function of the phase detector, K_ϕ, is expressed in volts/radian. A 1/s multiplier accounts for the conversion of frequency to phase, since phase is the time integral of frequency.

Following the phase detector is the loop filter. This block contains the required gain and filtering to set the loop's overall bandwidth and meet the necessary stability criteria. The output of the loop filter is the control input to the motor drive. Depending on the type of drive used, voltage or current, the driver will have respectively, a V_{OUT}/V_{IN} transfer characteristic, or an I_{OUT}/V_{IN} transconductance.

At first glance, it seems that the motor has simply replaced the V_{CO} (voltage controlled oscillator), in the classic phase locked loop. In fact, it is a little more complicated. The mechanical and electrical time constants of the motor come into play, making the transfer function of the motor more than just a voltage-in, frequency-out block. In order to analyze the loop's small and large signal behavior it is essential to have an equivalent eletrical model for the motor.

A SIMPLE ELECTRICAL MODEL FOR A DC MOTOR

Figure 2 is an electrical representation of a DC motor. The terms used are defined here:

- L_M Motor winding inductance in henrys
- R_M Motor winding resistance in Ωs
- J Total moment of inertia of the motor in Nm-sec^2 (**Note:** 1 Nm = 141.6 oz-in)
- K_T Motor torque constant in Nm/Amp
- K_V Voltage constant (back EMF) of motor in voltage-sec/rad (**Note:** $K_V = K_T$ in SI units)

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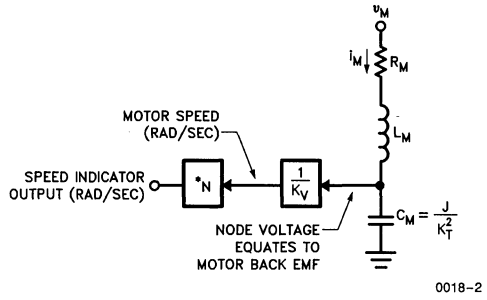


*N = Number of speed sense cycles per motor revolution

Figure 2. This simple electrical model is useful for determining the small and large signal characteristics of the motor. Capacitor, C_M is used to model the mechanical energy storage of the motor.

In this model the winding inductance and resistance elements correlate directly with the corresponding physical parameters of the motor, with values taken directly off the manufacturer's data sheet. The capacitor, C_M, models the mechanical energy storage of the motor. Current into the capacitor equates, via motor constant K_T, to motor torque, and the voltage across the capacitor is equal to the motor back EMF. The back EMF voltage equates to motor velocity through the inverse of K_V. In the model, the term N is simply a multiplier equal to the number of feedback cycles obtained per revolution of the motor. For example, in a 4 pole brushless DC motor the commutation Hall effect device outputs will be at twice the rotational frequency of the motor, making N equal to 2.

The equation for the capacitor, given in Figure 2, has the units of Farads if J and K_T are expressed in SI units. In modeling the overall transfer characteristic, it is important that the moment of inertia of the load on the motor be added to the moment of inertia of the motor itself.

It is worthwhile to note that the current into the motor, minus idling current, is proportional to acceleration of the motor. This is easily seen from the model by realizing that the time derivative of the capacitor voltage relates directly to acceleration. The effects of loads on the motor can be modeled by including a current source across the capacitor for constant torque loads, or a resistor for loads that are linearly proportional to motor speed.

TRANSFER FUNCTIONS FOR VOLTAGE AND CURRENT DRIVEN MOTORS

Using the electrical model, the small signal transfer function of the motor is easily derived. Equations 1a and 1b give the small signal frequency response for both the current and voltage driven cases respectively.

$$1a)\quad \frac{N \times \omega_M(s)}{i_M(s)} = \frac{N}{K_V} \times \frac{1}{sC_M}$$

$$1b)\quad \frac{N \times \omega_M(s)}{v_M(s)} = \frac{N}{K_V} \times \frac{1}{1 + sC_MR_M + s^2 L_MC_M}$$

The transfer function given in equation (1a) describes the small signal response of motor speed, $\omega_M(s)$, to changes in the drive current. Equation (1b) relates the dependence of motor speed to motor drive voltage.

The small signal response of the motor for the current driven case has a DC pole that results from the relationship of motor torque to velocity, that is, motor velocity is proportional to the integral of motor torque over time. In the current driven motor neither the winding resistance nor inductance appear in the transfer function. This is because these elements are in series with the current source output of the driver stage. As long as the output impedance of the driver remains large relative to the impedance of these elements, the resistance and inductance of the motor will have a negligible effect on the small signal response.

The voltage driven response has a second order characteristic that results from the interaction of the series RLC. In many cases the transfer function of the voltage driven case can be simplified. If the quality factor of the series RLC of the motor model is much less than one, as defined in equation 2, then the response of the motor can be accurately approximated by equation 3.

$$2)\quad Q_M = \frac{1}{R_M}\sqrt{\frac{L_M}{C_M}} = \frac{K_T}{R_M}\sqrt{\frac{L_M}{J}}$$

$$\therefore Q_M \ll 1 \quad \text{If } R_M \gg K_T\sqrt{\frac{L_M}{J}}$$

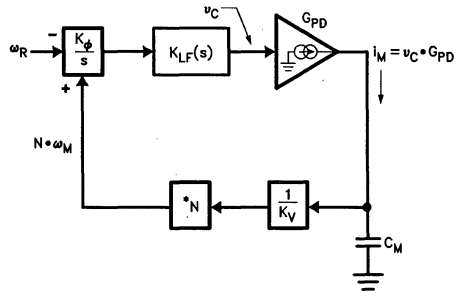
$$3)\quad \text{For } Q_M \ll 1$$

$$\frac{N \times \omega_M(s)}{v_M(s)} = \frac{N}{K_V} \times \frac{1}{(1 + sC_MR_M)(1 + sL_M/R_M)}$$

CONSIDERING THE WHOLE LOOP

Figure 3 shows the complete speed control loop for the current driven case. The overall open loop response, A_{OLC}, is easily written.

$$4)\quad A_{OLC}(s) = \frac{K_\phi \times K_{LF}(s) \times G_{PD} \times N}{s^2C_M \times K_V}$$



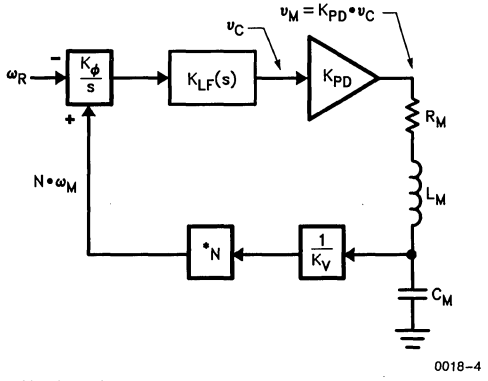
*N = Number of feedback cycles per motor revolution

Figure 3. In this phase locked loop, with current mode drive to the motor, the motor winding resistance and inductance can be ignored as long as the current driver maintains a high output impedance.

For this loop, note that there are two poles in the response at DC, i.e., s = 0. One pole is due to the response of the current driven motor, the second pole is from the frequency to phase transformation of the phase detector. The 180 degrees of phase shift this pair of poles introduce force a phase lead configuration of the loop filter in order to obtain a loop phase margin greater than zero.

The complete voltage loop is shown in Figure 4, and its open loop response, $A_{OLV}(s)$, in equation 5.

$$5)\quad A_{OLV}(s) = \frac{K_\phi \times K_F(s) \times K_{PD} \times N}{sK_V \times (1 + sC_MR_M + s^2 L_MC_M)}$$



*N = Number of feedback cycles per motor revolution

Figure 4. With voltage mode drive to the motor the electrical time constant of the motor plays a part in the small signal response of the speed control loop.

This response has only one pole at DC, although the total number of poles is three versus two for the current driven case. For most motors, particularly those used in constant velocity applications, this transfer function can be simplified by applying the results of equations 2 and 3. This is best illustrated by looking at an example. Consider the following motor, (typical 3-phase brushless for disc drive applications):

K_T ..... 1.5×10^{-2} Nm/Amp
K_V ..... 1.5×10^{-2} V-sec/rad
J (including platters) ..... 1×10^{-3} Nm-sec2
R_M 2.5Ω
L_M ..... 2 mH

For this motor, the model capacitor, C_M, is calculated using the equation in Figure 2 to be equal to 4.4 Farads. If we calculate the quality factor of the series RLC, using equation 2, we find it is equal to 42.4×10^{-3}. This is considerably less than one, and the response closely approximates the non-complex response of equation 3 with poles at 0.014 Hz and 199 Hz.

Typical loop bandwidths will fall well inside this range of frequencies. As long as this is true, the loop response with a voltage driven motor can be approximated by:

$$6)\quad A_{OLV}(s) \approx \frac{K_\phi \times K_{LF}(s) \times K_{PD}/R_M \times N}{s^2 C_M K_V}$$

$$\text{If } Q_M \ll 1 \text{ and } \frac{1}{2\pi C_M R_M} < f < \frac{R_M}{2\pi L_M} \left(f = \left|\frac{s}{2\pi}\right|\right)$$

This expression is the same as the current driven response, equation 4, with the transconductance of the current drive stage, G_{PD}, replaced by the gain of the voltage drive stage divided by the motor winding resistance, K_{PD}/R_M.

CLOSING THE LOOP

When it comes to closing the loop the goal is to have a stable loop with the required loop bandwidth. The variables that must be considered are:

1) The motor
2) The power driver, type and gain
3) The phase detector gain
4) Loop bandwidth
5) The loop filter

The first four of the above variables are usually dictated by conditions other than the stabilizing of the loop. This leaves the loop filter as the tool for achieving the small signal loop requirements.

For many cases involving constant velocity loops for DC motor speed control, the following simple Bode analysis can be applied for determining the design of the loop filter. Assuming we know, or have preliminary guesses for the first four variables listed above, we can plot the Bode asymptotes for phase and gain of the combined response of the motor and power driver. Figure 5 shows, for a typical case, such a plot on a frequency scale that has been normalized to the desired loop bandwidth, or open loop unity gain frequency. This figure illustrates the small signal open loop response for the current driven case, equation 4, minus the response of the loop filter, K_{LF}. If the previously noted assumptions hold, this plot will also apply to the voltage driven case i.e., equation 6.

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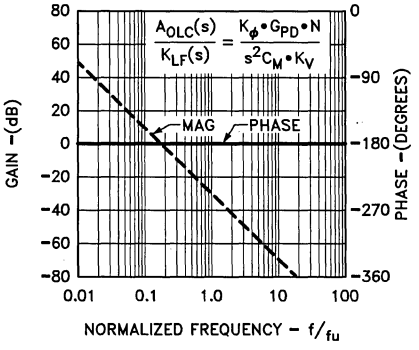


0018-5

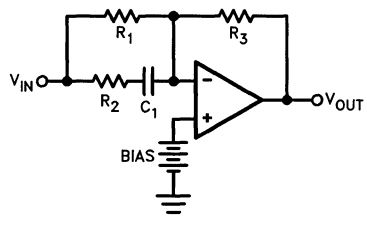
Figure 5. A Bode plot of the combined gain and phase response of the motor, motor drive, and phase dectector is useful in determining the requirements on the loop filter. This plot is normalized to the desired open loop unity gain frequency.

From Figure 5 two restrictions on the loop filter are readily apparent. First, since the remaining portion of the loop has 180° of phase shift over the entire frequency range, the loop filter must have a phase lead at the unity gain frequency and at all frequencies below the unity gain frequency. By meeting this restriction the small signal loop will be unconditionally stable.

Secondly, in order to achieve the desired loop bandwidth, the loop filter must have a voltage gain at the desired unity gain frequency of 30 dB. This level is simply the inverse of the remaining loop's voltage gain at the unity gain frequency.

A loop filter configuration that will meet these restrictions is shown in Figure 6. Also shown in this figure is the small signal response equation for the filter. The response starts out from DC with a flat inverting gain that breaks upward at the zero frequency, ω_Z, and then flattens out again at the pole, ω_P. The pole in this response is necessary to prevent excess feedthrough of residual reference frequency that is present at the outputs of many digital type phase detectors—in fact, as will be discussed in the design example, a separate reference filter is normally required.

A good choice for the relative positioning of the pole and zero of the loop filter response is to space them apart by 1 decade of frequency, and center them around the unity gain frequency. Figure 7 shows the Bode plots of this suggested positioning applied to the case illustrated in Figure 5. As shown, a phase margin of about 45° is obtained with this configuration.



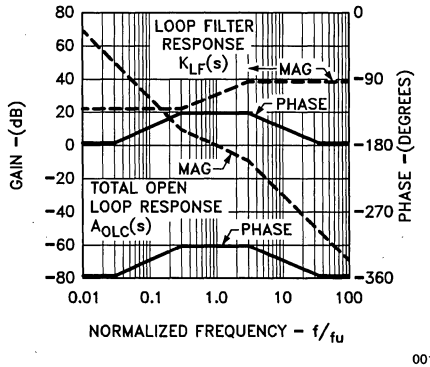
0018-6

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_3}{R_1} \times \frac{1 + s/\omega_Z}{1 + s/\omega_P}$$

$$\omega_Z = \frac{1}{(R_1 + R_2)\,C_1}$$

$$\omega_P = \frac{1}{R_2 C_1}$$

Figure 6. This loop filter configuration provides the required phase lead and gain at the loop crossover frequency.



0018-7

Figure 7. Using the criteria set forth for the design of the loop filter, the resulting Bode plot indicates a phase margin of 45°.

If the above results are acceptable, then the following simple steps can be applied to pick the loop amplifier component values. Referring to Figure 6.

1) Pick R_3 to be as high in value as acceptable for the Op-Amp and board restrictions.

2) $R_1 = (R_3 \times 3.33)/10^{X/20}$, where X is the voltage gain, in dB, required at the unity gain frequency.

3) $R_2 = R_1/9$, sets a 10:1 ratio for ω_P to ω_Z.

4) $C_1 = (2\pi \times R_2 \times 3.33 \times f_\mu)^{-1}$, where f_μ is the loop unity gain frequency.

Using this simple procedure the small signal loop is easily closed for stable static operation.

A DESIGN EXAMPLE

As an example, let us take a look at the complete design of a constant velocity speed control loop for a disc drive application. The performance characteristics for the circuit can be summarized as:

Motor speed ..... 3600 rpm ±60 ppm (0.006%)
Speed stability ..... ±50 ppm
Start-up lock time ..... 10 seconds
Input voltage ..... 12 Volts
Motor idling current ..... 0.5 Amps

The schematic for this design is shown in Figure 8. The motor is a 4 pole 3-phase brushless with the electrical and mechanical specifications given in the figure. The motor is current mode driven with the UC3620 3-phase Switchmode Driver. The speed control function is realized with the UC3633 Phase Locked Controller.

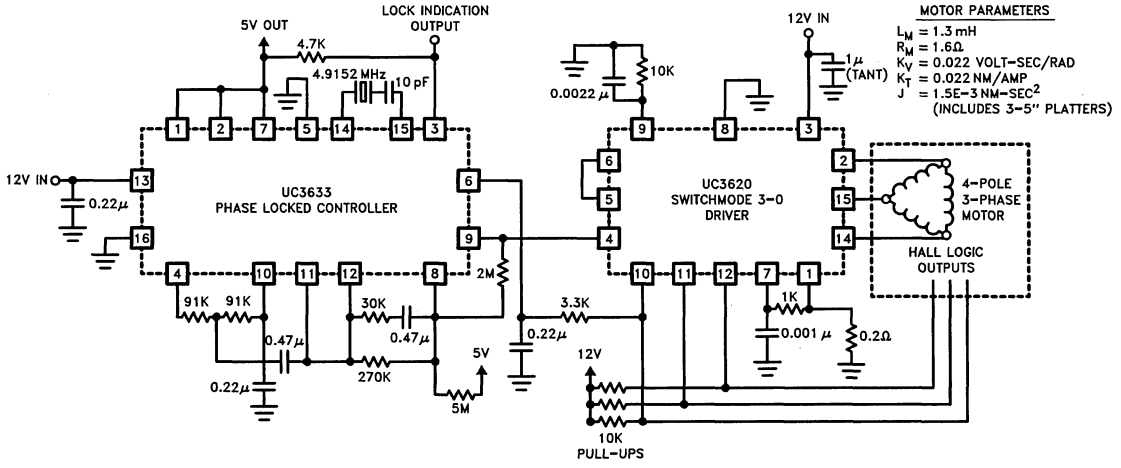


Figure 8. A precision speed control loop uses the UC3620 Switchmode 3-phase Driver and the UC3633 Phase Locked Controller to spin a DC brushless motor at 3600 rpm, ±60 ppm.

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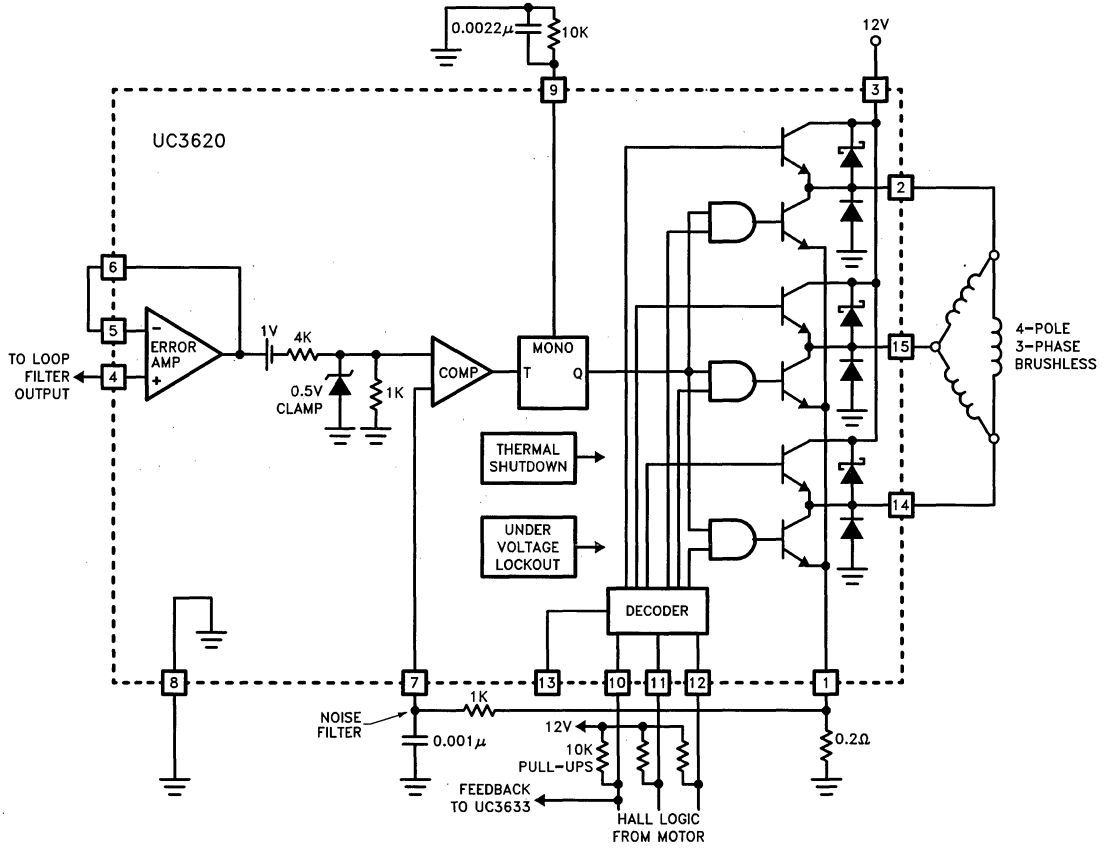
POWER DRIVER STAGE

In Figure 9 a detail of the driver IC and the associated circuitry is shown. The UC3620 is a current-mode, fixed off-time, chopper. Three 2-Amp totem pole output stages with catch diodes drive the three motor phases. The outputs are enabled by the internal commutation logic that responds to the three Hall logic signals from the motor. The motor is equipped with open collector Hall devices making the three 10k pull-up resistors on the UC3620 Hall inputs necessary.

Current is controlled by chopping the lowside drive to the phase winding under the command of the UC3620's current sense comparator. The RC combination on the timing pin of the driver sets the off-time at 22 μs. This results in a chopping frequency of well over 20 kHz under normal operating conditions.

The transconductance of the driver is set by the value of current sense resistor used at the emitter pin of the UC3620. With a value of 0.2Ω the transconductance from the error amplifier output to the driver outputs is 1 Amp/Volt. The UC3620 error amplifier is configured here as a unity gain buffer, thus the drive control signal is applied at the non-inverting error amplifier input with the same overall transconductance. An internal 0.5V clamp diode at the current sense comparator input results in a 2.5 Amp maximum drive current. There is a 1V offset internal to the UC3620 that is reflected to the drive control input at zero current. This offset combines with the 0.5 Amp idling current level of the motor to set the steady state DC voltage at the driver control input to be 1.5V.



0018-9

Figure 9. The UC3620 is a current mode fixed off-time driver. This device includes all the drive and commutation circuitry for a three phase brushless motor. The 0.2Ω current sense resistor and the internal divide by five sets the transconductance of this power stage to 1 Amp/Volt.

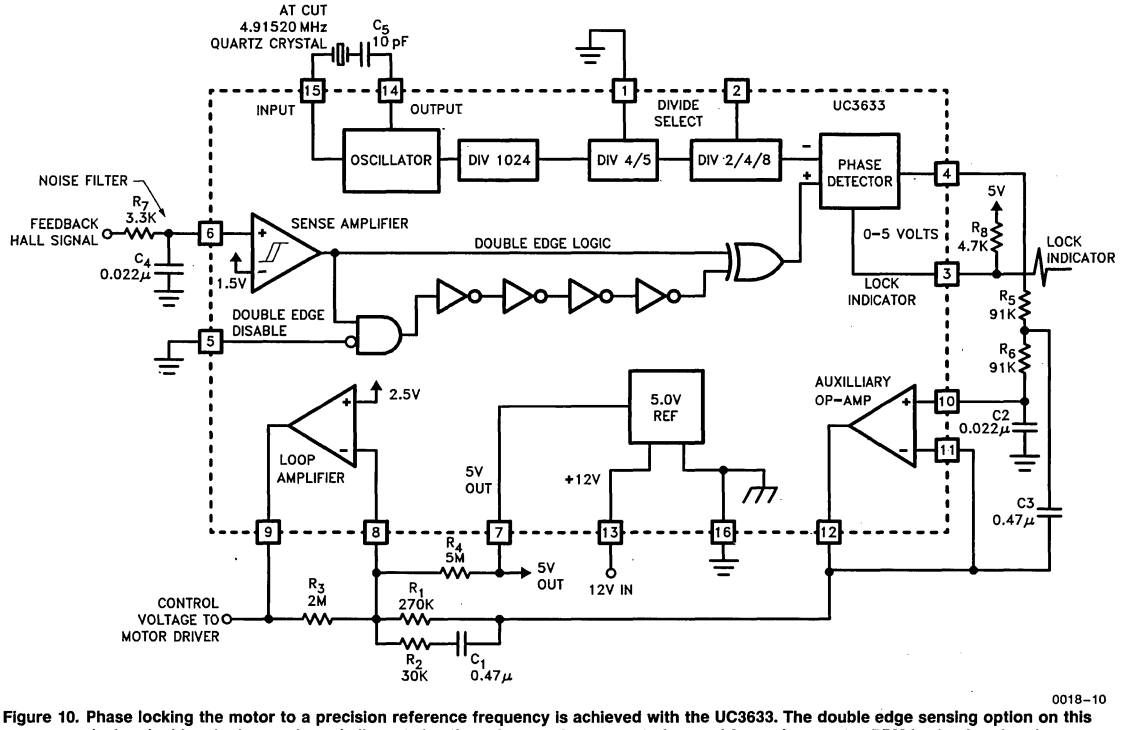


Figure 10. Phase locking the motor to a precision reference frequency is achieved with the UC3633. The double edge sensing option on this device doubles the loop gain and allows twice the reference frequency to be used for a given motor RPM by forcing the phase detector to respond to both edges of the Hall feedback signal.

PHASE LOCKED CONTROL CIRCUIT

A detail of the phase locked control portion of the design is given in Figure 10. The UC3633 contains all of the circuitry required for this function including: a crystal oscillator, programmable reference dividers, a digital phase detector, and op-amps for the required filtering. The UC3633 receives velocity feedback from the Hall signal applied at its sense amplifier input pin. The sense amplifier has a small amount of hysteresis that provides fast rising and falling input edges to the following logic. A double edge option is available on the UC3633 sense amplifier. When this option is enabled, as it is in this design, the phase detector is supplied with a short pulse on both the rising and falling edges of the feedback signal, effectively doubling the loop gain and reference frequency.

The required reference frequency for this loop is 240 Hz, given by the product of the motor rotation of 3600 rpm (60 Hz), the number of cycles/revolution at the Hall outputs (two for a 4 pole motor), and a factor of two as a result of the double edge sensing. The divider options on the UC3633 are set up such that standard microprocessor crystals can be used. In this instance, a 4.91520 MHz (±50 ppm) AT cut crystal is divided by 20,480 to realize a 240 Hz reference frequency input to the phase detector.

The phase detector on the UC3633 responds to phase differences at its two inputs with output pulses at the reference frequency rate. The width of the pulses is linearly proportional to the magnitude of the phase error present.

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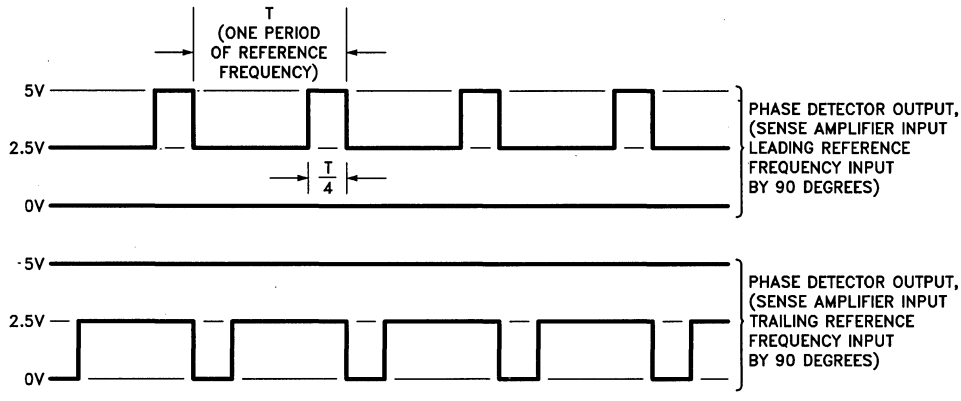


0018-11

Figure 11. The phase detector on the UC3633 is a digital circuit that responds to phase error with a pulsed output at the reference frequency rate. The width and polarity of the pulses depend respectively on the phase error magnitude and polarity. If any static frequency error is present, the detector will respond with a constant 0 Volt or 5 Volt signal depending on the sign of the error present.

The pulses are always 2.5V in magnitude and are referenced to 2.5V at the detector output. The polarity of the output pulses tracks the polarity of the input phase error. This operation is illustrated in Figure 11. The resulting phase gain of the detector is $2.5V/2\pi$ radians, or about 0.4V/rad, with a dynamic range of $\pm 2\pi$ radians.

The phase detector also has the feature of absolute frequency steering. If any static frequency error exists between the two inputs, the output of the detector will stay in a constant high, or low state; 5V, if the feedback input rate is greater than the reference frequency and 0V, if the opposite frequency relationship exists. The lock indicator output on the UC3633 provides a logic low output when any static error exists between the feedback and reference frequencies.

A unity gain bandwidth of 4 Hz was chosen for this loop. This unity gain frequency is well below the effective sampling frequency, the 240 Hz reference, and is sufficently high to not significantly affect the start-up lock time of the drive system. The design of the loop filter follows the guidelines described earlier. The magnitude of the loop gain, minus the loop filter, at 4 Hz is equal to:

$$\frac{K_\phi \times G_{PD} \times N}{(2\pi f)^2 \times C_M \times K_V} = \frac{(0.4)(1)(4)}{(2\pi 4)^2(3.1)(0.022)}$$

$= 37.2$ E-3 or -28.6 dB.

This dictates that the loop amplifier has a gain of 28.6 dB at 4 Hz. A value for the loop amplifier feedback resistor, R_3, of 2 MΩ was chosen. The values for R_1, R_2 and C_1 were calculated as follows.

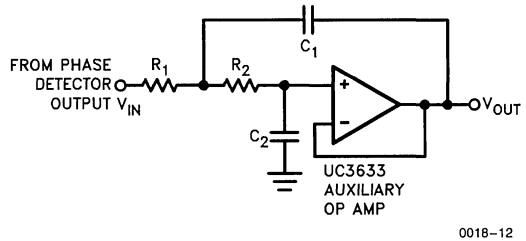
$R_1 = (2E6 \times 3.33)/10^{28.6/20} = 248$ kΩ (270 kΩ used).

$R_2 = 270/9 = 30$ kΩ

$C_1 = (2\pi \times 30E3 \times 3.33 \times 4)^{-1}$
$= 0.4\ \mu F$ ($0.47\ \mu F$ used).

The additional op-amp on the UC3633 is used to realize a second order active filter to attenuate the reference component out of the phase detector. The filter is a standard quadratic with a natural frequency of 17.2 Hz and a Q of about 2.3. This circuit provides 46 dB of attenuation at 240 Hz while adding only 5° of phase shift at the 4 Hz loop crossover frequency. In Figure 12 design guidelines and response curves for this filter are given.

Reference Filter Configuration



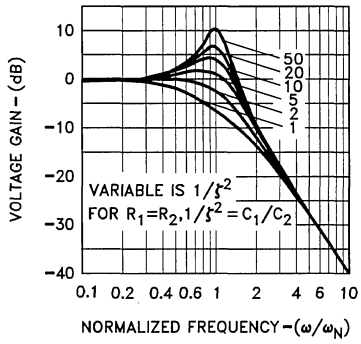
$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{1}{1 + \frac{s2\zeta}{\omega_N} + \frac{s^2}{\omega_N^2}}$$

$$\omega_N = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$\zeta = \frac{1}{2Q} = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}\ \frac{R_1 + R_2}{\sqrt{R_1 R_2}}$$

Note: with $R_1 = R_2$, $\zeta = \sqrt{\frac{C_2}{C_1}}$

Reference Filter Design Aid—Gain Response



Reference Filter Design Aid—Phase Response

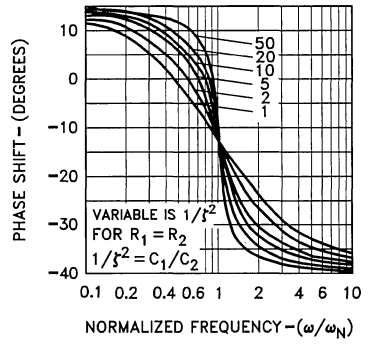


Figure 12. To keep feedthrough of the residual reference frequency at the phase detector output to a minimum, a simple quadratic filter can be used. The design of this filter is easily accomplished with the above equations and response curves.

As mentioned earlier, a separate reference filter is required in this type of phase locked loop to attenuate the reference frequency feedthrough at the output of the phase detector. With the active filter following the phase detector, the feedthrough to the loop amplifier is kept to less than $20mV_{pp}$ under the worst case condition of $\pm\pi(180°)$ phase error. This is small compared to the 1.25V DC signal out of the detector at this phase error. If the reference ripple into the loop amplifier becomes large compared to the averaged phase error term, large signal instabilities may result. These are primarily the result of the unidirectional nature of the motor drive.

The static reference ripple at the motor drive input, during phase locked conditions, can be minimized by forcing the loop to lock at zero phase error—at zero phase error there is no reference frequency component at the detector output. The finite DC gain through the loop filter, dictated by the inherent second order nature of the loop, results in a static phase error that is a function of: the DC level required at the motor drive input, the DC gain and reference voltage of the loop amplifier, and the voltage levels out the phase detector. The addition of resistor R_4, see Figure 10, from the loop amplifier's inverting input to

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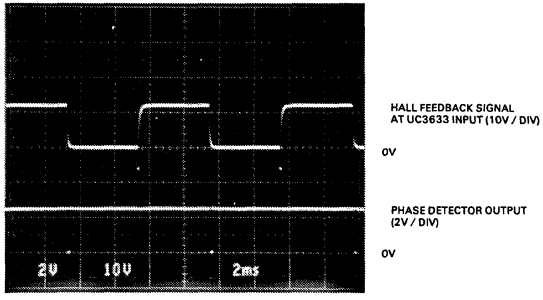
the 5V reference sets the zero phase operating voltage at the loop filter output to 1.5V. This matches the nominal operating voltage required at the UC3620 control input, taking into account the 0.5 Amp idling current of the motor and the 1V offset of the driver. This cancellation is subject to variations due to shifts in DC operating levels, so, while it does significantly reduce static reference feedthrough, it can not be expected to reliably set exactly zero phase operation.

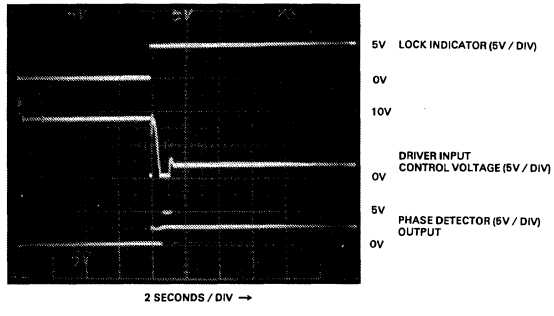
The oscilliscope traces in Figure 13 show the Hall input to the UC3633 along with the output waveform of the digital phase detector under static phase locked conditions. Notice that the phase detector output is alternating between positive and negative output pulses. This is a result of a slight asymmetry on the Hall input signal in conjunction with the use of the double edge sensing being used. In this case, the asymmetry is due to differences in the rising and falling edges of the Hall signal that result from the RC filter at the sense amplifier input. This filter is required to keep high frequency noise from the motor drive out of the phase detector.

The startup response of the motor is pictured in Figure 14. Shown are the voltage waveforms at the lock indicator output, the loop amplifier output, and the phase detector output of the UC3633. At the moment the lock indicator goes high the motor has reached its operating velocity. The absolute frequency steering of the phase detector forces a slight overshoot in frequency that delays the settling of the loop by about 1 second. Without the frequency steering feature the phase detector would command a much lower average drive signal during startup, extending the start time by over 50%.



0018-15

Figure 13. This oscilloscope trace shows the static waveforms at the Hall sensor input, and phase detector output of the UC3633. The static phase error has been adjusted, with R_4 in Figure 10, to be very small. The alternating positive and negative pulses at the output of the phase detector is due to an asymmetry in the Hall signal.



0018-16

Figure 14. The startup lock time of the motor is minimized with the absolute frequency steering feature of the phase detector, keeping lock times under 10 seconds.

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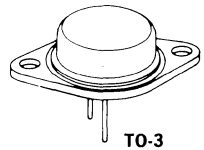
N-CHANNEL POWER MOSFETS



TO-3

V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	Part Numbers	I_D Continuous Drain Current (Amps) 100°C Case	I_D Continuous Drain Current (Amps) 25°C Case	I_{DM} Pulsed Drain Current (Amps)	$P_{D\ MAX}$ Power Dissipation (Watts)
500	0.4	2N6770*	7.75	12.0	48	150
500	0.4	UFN450	8.0	13.0	52	150
500	0.5	UFN452	7.0	12.0	48	150
500	0.85	UFN440	5.0	8.0	32	125
500	1.1	UFN442	4.0	7.0	28	125
500	1.5	2N6762*	3.0	4.5	18	75
500	1.5	UFN430	3.0	4.5	18	75
500	2.0	UFN432	3.5	4.0	16	75
500	3.0	UFN420	1.5	2.5	10	40
500	4.0	UFN422	1.0	2.0	8	40
450	0.4	UFN451	8.0	13.0	52	150
450	0.5	2N6769	7.0	11.0	44	150
450	0.5	UFN453	7.0	12.0	48	150
450	0.85	UFN441	5.0	8.0	32	125
450	1.1	UFN443	4.0	7.0	28	125
450	1.5	UFN431	3.0	4.5	18	75
450	2.0	2N6761	2.5	4.0	16	75
450	2.0	UFN433	2.5	4.0	16	75
450	3.0	UFN421	1.5	2.5	10	40
450	4.0	UFN423	1.0	2.0	8	40
400	0.3	2N6768*	9.0	14.0	56	150
400	0.3	UFN350	9.0	15.0	60	150
400	0.4	UFN352	8.0	13.0	52	150
400	0.55	UFN340	6.0	10.0	40	125
400	0.8	UFN342	5.0	8.0	32	125
400	1.0	2N6760*	3.5	5.5	22	75
400	1.0	UFN330	3.5	5.5	22	75
400	1.5	UFN332	3.0	4.5	18	75
400	1.8	UFN320	2.0	3.0	12	40
400	2.5	UFN322	1.5	2.5	10	40
350	0.3	UFN351	9.0	15.0	60	150
350	0.4	2N6767	7.75	12.0	48	150
350	0.4	UFN353	8.0	13.0	52	150
350	0.55	UFN341	6.0	10.0	40	125
350	0.8	UFN343	5.0	8.0	32	125
350	1.0	UFN331	3.5	5.5	22	75
350	1.5	2N6759	3.0	4.5	18	75
350	1.5	UFN333	3.5	4.5	18	75
350	1.8	UFN321	2.0	3.0	12	40
350	2.5	UFN323	1.5	2.5	10	40

V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	Part Numbers	I_D Continuous Drain Current (Amps) 100°C Case	I_D Continuous Drain Current (Amps) 25°C Case	I_{DM} Pulsed Drain Current (Amps)	$P_{D\ MAX}$ Power Dissipation (Watts)
200	0.085	2N6766*	19.0	30.0	120	150
200	0.085	UFN250	19.0	30.0	120	150
200	0.12	UFN252	16.0	25.0	100	150
200	0.18	UFN240	11.0	18.0	72	125
200	0.22	UFN242	10.0	16.0	64	125
200	0.4	2N6758*	6.0	9.0	36	75
200	0.4	UFN230	6.0	9.0	36	75
200	0.6	UFN232	5.0	8.0	32	75
200	0.8	UFN220	3.0	5.0	20	40
200	1.2	UFN222	2.5	4.0	16	40
150	0.085	UFN251	19.0	30.0	120	150
150	0.12	2N6765	16.0	25.0	100	150
150	0.12	UFN253	16.0	25.0	100	150
150	0.18	UFN241	11.0	18.0	72	125
150	0.22	UFN243	10.0	16.0	64	125
150	0.4	UFN231	6.0	9.0	36	75
150	0.6	2N6757	5.0	8.0	32	75
150	0.6	UFN233	5.0	8.0	32	75
150	0.8	UFN221	3.0	5.0	20	40
150	1.2	UFN223	2.5	4.0	16	40
100	0.055	2N6764*	24.0	38.0	152	150
100	0.055	UFN150	25.0	40.0	160	150
100	0.08	UFN152	20.0	33.0	132	150
100	0.085	UFN140	17.0	27.0	108	125
100	0.11	UFN142	15.0	24.0	96	125
100	0.18	2N6756*	9.0	14.0	56	75
100	0.18	UFN130	9.0	14.0	56	75
100	0.25	UFN132	8.0	12.0	48	75
100	0.3	UFN120	5.0	8.0	32	40
100	0.4	UFN122	4.0	7.0	28	40
60	0.055	UFN151	25.0	40.0	160	150
60	0.08	2N6763	20.0	31.0	124	150
60	0.08	UFN153	20.0	33.0	132	150
60	0.085	UFN141	17.0	27.0	108	125
60	0.11	UFN143	15.0	24.0	96	125
60	0.18	UFN131	9.0	14.0	56	75
60	0.25	2N6755	8.0	12.0	48	75
60	0.25	UFN133	8.0	12.0	48	75
60	0.3	UFN121	5.0	8.0	32	40
60	0.4	UFN123	4.0	7.0	28	40

* Available as JAN, JANTX, and JANTXV types.

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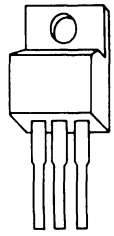

TO-220AB

V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	Part Numbers	I_D Continuous Drain Current (Amps) 100°C Case	I_D Continuous Drain Current (Amps) 25°C Case	I_{DM} Pulsed Drain Current (Amps)	$P_{D\ MAX}$ Power Dissipation (Watts)
500	0.85	UFN840	5.0	8.0	32	125
500	1.1	UFN842	4.0	7.0	28	125
500	1.5	UFN830	3.0	4.5	18	75
500	2.0	UFN832	2.5	4.0	16	75
500	3.0	UFN820	1.5	2.5	10	40
500	4.0	UFN822	1.0	2.0	8	40
450	0.85	UFN841	5.0	8.0	32	125
450	1.1	UFN843	4.0	7.0	28	125
450	1.5	UFN831	3.0	4.5	18	75
450	2.0	UFN833	2.5	4.0	16	75
450	3.0	UFN821	1.5	2.5	10	40
450	4.0	UFN823	1.0	2.0	8	40
400	0.55	UFN740	6.0	10.0	40	125
400	0.80	UFN742	5.0	8.0	32	125
400	1.0	UFN730	3.5	5.5	22	75
400	1.5	UFN732	3.0	4.5	18	75
400	1.8	UFN720	2.0	3.0	12	40
400	2.5	UFN722	1.5	2.5	10	40
400	3.6	UFN710	1.0	1.5	6	20
400	5.0	UFN712	0.8	1.3	5	20
350	0.55	UFN741	6.0	10.0	40	125
350	0.8	UFN743	5.0	8.0	32	125
350	1.0	UFN731	3.5	5.5	22	75
350	1.5	UFN733	3.0	4.5	18	75
350	1.8	UFN721	2.0	3.0	12	40
350	2.5	UFN723	1.5	2.5	10	40
350	3.6	UFN711	1.0	1.5	6	20
350	5.0	UFN713	0.8	1.3	5	20
200	0.18	UFN640	11.0	18.0	72	125
200	0.22	UFN642	10.0	16.0	64	125

V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	Part Numbers	I_D Continuous Drain Current (Amps) 100°C Case	I_D Continuous Drain Current (Amps) 25°C Case	I_{DM} Pulsed Drain Current (Amps)	$P_{D\ MAX}$ Power Dissipation (Watts)
200	0.4	UFN630	6.0	9.0	36	75
200	0.6	UFN632	5.0	8.0	32	75
200	0.8	UFN620	3.0	5.0	20	40
200	1.2	UFN622	2.5	4.0	16	40
200	1.5	UFN610	1.5	2.5	10	20
200	2.4	UFN612	1.25	2.0	8	20
150	0.18	UFN641	11.0	18.0	72	125
150	0.22	UFN643	10.0	16.0	64	125
150	0.4	UFN631	6.0	9.0	36	75
150	0.6	UFN633	5.0	8.0	32	75
150	0.8	UFN621	3.0	5.0	20	40
150	1.2	UFN623	2.5	4.0	16	40
150	1.5	UFN611	1.5	2.5	10	20
150	2.4	UFN613	1.25	2.0	8	20
100	0.085	UFN540	17.0	27.0	108	125
100	0.11	UFN542	15.0	24.0	96	125
100	0.18	UFN530	9.0	14.0	56	75
100	0.25	UFN532	8.0	12.0	48	75
100	0.3	UFN520	5.0	8.0	32	40
100	0.4	UFN522	4.0	7.0	28	40
100	0.6	UFN510	2.5	4.0	16	20
100	0.8	UFN512	2.0	3.5	14	20
60	0.085	UFN541	17.0	27.0	108	125
60	0.11	UFN543	15.0	24.0	96	125
60	0.18	UFN531	9.0	14.0	56	75
60	0.25	UFN533	8.0	12.0	48	75
60	0.3	UFN521	5.0	8.0	32	40
60	0.4	UFN523	4.0	7.0	28	40
60	0.6	UFN511	2.5	4.0	16	20
60	0.8	UFN513	2.0	3.5	14	20
50	.028	UFNZ40	32.0	51.0	160	125
50	.035	UFNZ42	29.0	46.0	145	125
50	.050	UFNZ30	19.0	30.0	80	75
50	.070	UFNZ32	16.0	25.0	60	75
50	.100	UFNZ20	10.0	15.0	60	40
50	.120	UFNZ22	9.0	14.0	56	40

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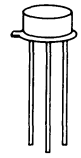
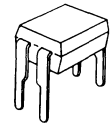


TO-39

V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	Part Numbers	I_D Continuous Drain Current (Amps) 100°C Case	I_D Continuous Drain Current (Amps) 25°C Case	I_{DM} Pulsed Drain Current (Amps)	$P_{D\ MAX.}$ Power Dissipation (Watts)
500	1.5	UFNF430	1.75	2.75	11	25
500	1.5	2N6802*	1.5	2.5	11	25
500	2.0	UFNF432	1.5	2.25	9	25
500	3.0	UFNF420	1.0	1.6	65	20
500	3.0	2N6794	0.95	1.5	6.5	20
500	4.0	UFNF422	0.9	1.4	5.5	20
450	1.5	UFNF431	1.75	2.75	11	25
450	1.5	2N6801	1.5	2.5	11	25
450	2.0	UFNF433	1.5	2.25	9	25
450	3.0	UFNF421	1.0	1.6	6.5	20
450	3.0	2N6793	0.95	1.5	6.5	20
450	4.0	UFNF423	0.9	1.4	5.5	20
400	1.0	UFNF330	2.0	3.5	14	25
400	1.0	2N6800*	1.6	3.0	14	25
400	1.5	UFNF332	1.6	3.0	12	25
400	1.8	UFNF320	1.45	2.5	10	20
400	1.8	2N6792	1.25	2.0	10	20
400	2.5	UFNF322	1.2	2.0	8	20
400	3.6	UFNF310	0.85	1.35	5.5	15
400	3.6	2N6786*	0.80	1.25	5.5	15
400	5.0	UFNF312	0.70	1.15	4.5	15
350	1.0	UFNF331	2.0	3.5	14	25
350	1.0	2N6799	1.6	3.0	14	25
350	1.5	UFNF333	1.6	3.0	12	25
350	1.8	UFNF321	1.45	2.5	10	20
350	1.8	2N6791	1.25	2.0	10	20
350	2.5	UFNF323	1.2	2.0	8	20
350	3.6	UFNF311	0.85	1.35	5.5	15
350	3.6	2N6785	0.80	1.25	5.5	15
350	5.0	UFNF313	0.70	1.15	4.5	15
200	0.4	2N6798*	3.5	5.5	22	25
200	0.4	UFNF230	3.5	5.5	22	25
200	0.6	UFNF232	2.8	4.5	18	25
200	0.8	2N6790	2.1	3.5	14	20
200	0.8	UFNF220	2.1	3.5	14	20
200	1.2	UFNF222	1.75	3.0	12	20
200	1.5	2N6784*	1.45	2.25	9	15
200	1.5	UFNF210	1.4	2.2	9	15
200	2.4	UFNF212	1.1	1.8	7.5	15
150	0.4	2N6797	3.5	5.5	22	25
150	0.4	UFNF231	3.5	5.5	22	25
150	0.6	UFNF233	2.8	4.5	18	25
150	0.8	2N6789	2.1	3.5	14	20
150	0.8	UFNF221	2.1	3.5	14	20
150	1.2	UFNF223	1.75	3.0	12	20
150	1.5	2N6783	1.45	2.25	9	15
150	1.5	UFNF211	1.4	2.2	9	15
150	2.4	UFNF213	1.1	1.8	7.5	15
100	0.18	2N6796*	5.0	8.0	32	25
100	0.18	UFNF130	5.0	8.0	32	25
100	0.25	UFNF132	4.5	7.0	28	25
100	0.3	2N6788	3.5	6.0	24	20
100	0.3	UFNF120	3.5	6.0	24	20
100	0.4	UFNF122	3.0	5.0	20	20
100	0.6	2N6782*	2.25	3.5	14	15
100	0.6	UFNF110	2.25	3.5	14	15
100	0.8	UFNF112	2.0	3.0	12	15
60	0.18	2N6795	5.0	8.0	32	25
60	0.18	UFNF131	5.0	8.0	32	25
60	0.25	UFNF133	4.5	7.0	28	25
60	0.3	2N6787	3.5	6.0	24	20
60	0.3	UFNF121	3.5	6.0	24	20
60	0.4	UFNF123	3.0	5.0	20	20
60	0.6	2N6781	2.25	3.5	14	15
60	0.6	UFNF111	2.25	3.5	14	15
60	0.8	UFNF113	2.0	3.0	12	15



DIL-4

V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	Part Numbers	I_D Continuous Drain Current (Amps) 25°C Case	I_{DM} Pulsed Drain Current (Amps)	$P_{D\ MAX.}$ Power Dissipation (Watts)
200	1.5	UFND210	0.6	2.5	1.0
200	0.8	UFND220	0.8	6.4	1.0
150	2.4	UFND213	0.45	1.8	1.0
150	1.2	UFND223	0.7	5.6	1.0
100	0.3	UFND120	1.3	5.2	1.0
100	0.6	UFND110	1.0	4.0	1.0
100	2.4	UFND1Z0	0.5	2.0	1.0
60	0.4	UFND123	1.1	4.4	1.0
60	0.8	UFND113	0.8	3.0	1.0
60	3.2	UFND1Z3	0.4	1.5	1.0

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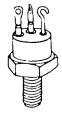
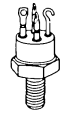
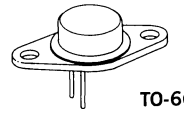
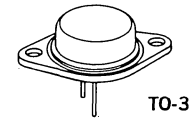
.5-30A, 60-500V


TO-59


TO-111


TO-66


TO-3

LOW VOLTAGE

Maximum Collector Current		5AMP					40AMP
Package Style		**TO-5**	**TO-59**		**TO-111**		**TO-3**
COLLECTOR-EMITTER SUSTAINING VOLTAGE $V_{CEO(SUS)}$	40V						UBT430
	60V	UPT612					
	80V	UPT613	2N2151** 2N2880* 2N3998*	2N3999*	2N3749* 2N3996*	2N3997*	
	100V	UPT614 UPT615					
h_{FE} Minimum		30 @ 1A	40 @ 1A	80 @ 1A	40 @ 1A	80 @ 1A	50 @ 20A
V_{CE}(sat) Max.		1V @ 5A	.25V @ 1A (1V @ 1A for 2N2151)				.1V @ 10A
t_f Maximum		0.1μs (typical)	0.3μs (2N2880) / 0.8μs (2N3998)	1.0μs	0.3μs (2N3749) / 0.8μs (2N3996)	1.0μs	0.12μs

HIGH VOLTAGE

Maximum Collector Current		2 AMP		3 AMP
Package Style		**TO-66**		**TO-66**
COLLECTOR-EMITTER SUSTAINING VOLTAGE $V_{CEO(SUS)}$	150V	UPT321		UPT521
	200V	UPT322	2N5660*	UPT522
	250V	UPT323		UPT523
	275V			
	300V	UPT324 UPT325	2N5661*	UPT524 UPT525
	350V			
	400V			
	500V			
h_{FE} Minimum		30 @ .5A	40 @ 5A (2N5660) / 25 @ 5A (2N5661)	25 @ 1A
V_{CE} (sat) Max.		1V @ 2A	4V @ 1A	1V @ 3A
t_r Maximum		0.3μs (typical)	0.4μs (2N5660) / 0.6μs (2N5661)	0.4μs (typical)

*Available as JAN, JANTX, JANTXV.

**Available as JAN, JANTX.

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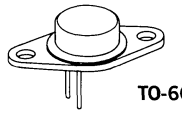
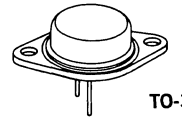
NPN BIPOLAR POWER SWITCHING TRANSISTORS

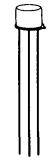
.5-30A, 60-500V



TO-66



TO-3



TO-5

LOW VOLTAGE

Maximum Collector Current		10 AMP
Package Style		**TO-5**
COLLECTOR-EMITTER SUSTAINING VOLTAGE $V_{CEO(SUS)}$	70V	2N4150*
	75V	
	80V	
	90V	
	100V	
	120V	
h_{FE} Minimum		50 @ 5A
V_{CE} (sat) Max.		0.6V @ 5A
t_f Maximum		0.5μs

HIGH VOLTAGE

Maximum Collector Current		5 AMP				
Package Style		**TO-5**		**TO-66**		
COLLECTOR-EMITTER SUSTAINING VOLTAGE $V_{CEO(SUS)}$	150V					UPT721
	200V	2N5666*		2N5664*		UPT722
	250V					UPT723
	275V					
	300V		2N5667*		2N5665*	UPT724 UPT725
	350V					
	400V					
	450V					
h_{FE} Minimum		40 @ 1A	25 @ 1A	40 @ 1A	25 @ 1A	25 @ 1A
V_{CE} (sat) Max.				0.4V @ 3A		1V @ 3A
t_f Maximum		0.8μs	1.0μs	0.8μs	1.0μs	0.5μs (typical)

*Available as JAN, JANTX, JANTXV.

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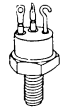
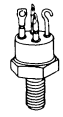
.5-30A, 60-500V



TO-59



TO-111

LOW VOLTAGE

Maximum Collector Current		10 AMP		15 AMP
Package Style		**TO-59**	**TO-111**	**TO-3**
COLLECTOR-EMITTER SUSTAINING VOLTAGE $V_{CEO\ (SUS)}$	70V			
	75V			
	80V	2N5658	2N5659	
	90V			
	100V			2N6496
	120V			
h_{FE} Minimum		50 @ 5A		12 @ 8A
V_{CE} (sat) Max.		0.5V @ 5A		1.0V @ 8A
t_f Maximum		0.5μs		0.5μs

*Available as JAN, JANTX, JANTXV.

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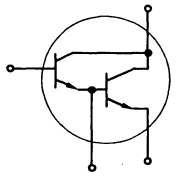
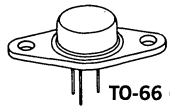


External bias types — for fast switching or other special purpose applications

TO-33



TO-66 (3-Pin)

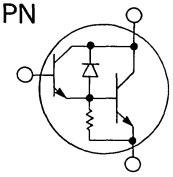
NPN Power Darlingtons

Maximum Collector Current		2A				5A			
Package Style		**TO-33**		**TO-66 (3-Pin)**		**TO-33**		**TO-66 (3-Pin)**	
COLLECTOR-EMITTER SUSTAINING VOLTAGE $V_{CEO\ (SUS)}$	60V	U2T301		U2T401					
	80V					2N6350* U2T101		2N6352* U2T201	
	150V		U2T305		U2T405		2N6351* U2T105		2N6353* U2T205
h_{FE} Minimum		1000 @ 2A		1000 @ 2A		2000 @ 5A	1000 @ 5A	2000 @ 5A	1000 @ 5A
V_{CE}(sat) Maximum		1.5V @ 2A	2.5V @ 2A	1.5V @ 2A	2.5V @ 2A	1.5V @ 5A	2.5V @ 5A	1.5V @ 5A	2.5V @ 5A
t_f Typical		0.3μs				0.5μs			

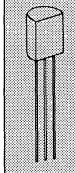
*Available as JAN, JANTX, and JANTVX types

Plastic NPN Power Darlingtons

NPN



Plastic Package types with integral bias resistance and shunt diode for maximum economy in standard applications



TO-92

Maximum Collector Current		5A (PEAK)
Package Style		**TO-92**
		NPN
COLLECTOR-EMITTER SUSTAINING VOLTAGE $V_{CEO\ (SUS)}$	60V	U2TA506
	80V	U2TA508
	100V	U2TA510
h_{FE} Minimum		500 @ 3A
V_{CE} (sat) Maximum		1.5V @ 3A
t_f Typical		0.8μs

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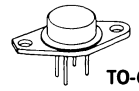
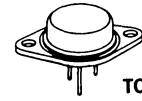
POWER HYBRIDS


TO-66


TO-3

Type	Output Current, Pk.	Input/Output Voltage	Polarity	Fall Time Volt. (ns)	Fall Time Cur. (ns)	On-State Voltage (V) @ (A)	Pkg.
PIC600	5A	60	Pos.	75	150	1.5 @ 2	**4 PIN TO-66 (Isolated)**
PIC601		80	Pos.				
PIC602		100	Pos.				
PIC610		60	Neg.				
PIC611		80	Neg.				
PIC612		100	Neg.				
PIC660	10A	60	Pos.	150	250	1.5 @ 5	**4 PIN TO-66 (Isolated)**
PIC661		80	Pos.				
PIC662		100	Pos.				
PIC670		60	Neg.	250	250		
PIC671		80	Neg.				
PIC672		100	Neg.				
PIC625	15A	60	Pos.	175	300	1.5 @ 7	**4 PIN TO-66 (Isolated)**
PIC626		80	Pos.				
PIC627		100	Pos.				
PIC635		60	Neg.	300	300		
PIC636		80	Neg.				
PIC637		100	Neg.				
PIC645	20A	60	Pos.	150	300	1.5 @ 7	**3 PIN TO-3**
PIC646		80	Pos.				
PIC647		100	Pos.				
PIC655		60	Neg.	300	300		
PIC656		80	Neg.				
PIC657		100	Neg.				

HI-REL PICS

Unitrode offers as standard parts, high reliability versions of the PIC600 series power hybrid circuit screened to Unitrode specifications UL101/102. Listed below is a part number cross reference.

Basic Device	Test Specification	Test Level T1	Test Level T2
PIC600-602	UL101	PIC7501-7503	PIC7519-7521
PIC610-612	UL101	PIC7504-7506	PIC7522-7524
PIC625-627	UL101	PIC7507-7509	PIC7525-7527
PIC635-637	UL101	PIC7510-7512	PIC7528-7530
PIC645-647	UL102	PIC7513-7515	PIC7531-7533
PIC655-657	UL102	PIC7516-7518	PIC7534-7536
PIC660-661	UL101	PIC7555-7557	PIC7561-7563
PIC670-672	UL101	PIC7558-7560	PIC7564-7566

Each PIC75XX device is 100% screened to the following requirements per specification UL101/102.

UL101/102 SCREENING TABLE

1. Hermetic Seal Test — Fine Leak
2. Hermetic Seal Test — Gross Leak
3. High Temperature Storage
4. Temperature Cycling
5. Reverse Bias Clamped Inductive Test
6. High Temperature Reverse Bias
7. Power Burn-In

Test level T1 provides "attributes" data (GO/NO-GO testing after high temperature reverse bias and power burn-in) with shipment.

Test level T2 provides "variables" data (read and record data with delta criteria before and after high temperature reverse bias and power burn-in) with shipment.

A Group A sample test of mechanical, electrical and switching speed specifications is performed on each lot.

A Certificate of Compliance is provided with each shipment.

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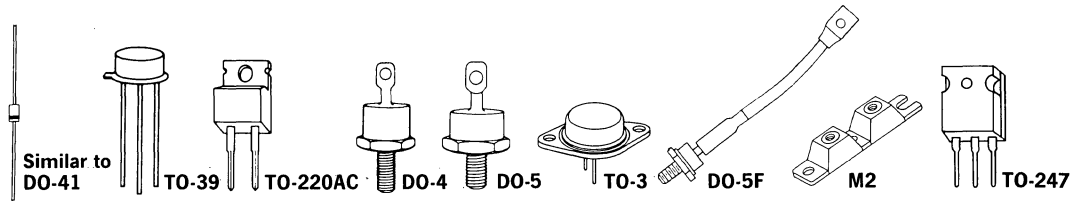

AVERAGE DC OUTPUT CURRENT		1A	1A	4A	6A	8A	12A[1]	12A
PEAK REVERSE VOLTAGE	PKG	Similar to DO-41 (ASA)	Similar to DO-41 (ASA)	TO-39 HERMETIC (3 LEAD)	TO-220 PLASTIC (2 LEAD)	TO-220 PLASTIC (2 LEAD)	TO-220 PLASTIC (3 LEAD)	TO-220 PLASTIC (2 LEAD)
20V	TYPE	1N5817	USD1120		USD620	USD720	USD620C	USD820
	V_F	.45 @ 1A	.45 @ 1A		.48 @ 6A	.48 @ 8A	.60 @ 12A	.51 @ 12A
	I_{FSM}	25A	50A		150A	200A	150A	200A
30V	TYPE	1N5818	USD1130					
	V_F	.55 @ 1A	.475 @ 1A					
	I_{FSM}	25A	50A					
35V	TYPE				USD635	USD735	USD635C	USD835
	V_F				.48 @ 6A	.48 @ 8A	.60 @ 12A	.51 @ 12A
	I_{FSM}				150A	200A	150A	200A
40V	TYPE	1N5819	USD1140		USD640	USD740	USD640C	USD840
	V_F	.60 @ 1A	.50 @ 1A		.48 @ 6A	.48 @ 8A	.60 @ 12A	.45 @ 12A
	I_{FSM}	25A	50A		150A	200A	150A	200A
45V	TYPE			USD245/R USD245C/R	USD645	USD745	USD645C	USD845
	V_F			.45 @ 2A	.48 @ 6A	.48 @ 8A	.60 @ 12A	.45 @ 12A
	I_{FSM}			80A	150A	200A	150A	200A

AVERAGE DC OUTPUT CURRENT		16A[2]	16A	16A	25A	30A	30A[3]	30A[3]
PEAK REVERSE VOLTAGE	PKG	TO-220 PLASTIC (3 LEAD)	TO-220 PLASTIC (2 LEAD)	TO-247 (2 LEAD)	DO-4 STUD	TO-247 (2 LEAD)	TO-247 (3 LEAD)	TO-3
20V	TYPE	USD720C	USD920					USD320C[6]
	V_F	.60 @ 16A	.53 @ 16A					.6 @ 20A
	I_{FSM}	200A	250A					400A
30V	TYPE			USD1630S		USD3030S	USD3030C	
	V_F			.49 @ 16A		.60 @ 30A	.65 @ 30A	
	I_{FSM}			250A		500A	300A	
35V	TYPE	USD735C	USD935					USD335C[6]
	V_F	.60 @ 16A	.53 @ 16A					.6 @ 20A
	I_{FSM}	200A	250A					400A
40V	TYPE	USD740C	USD940	USD1640S		USD3040S	USD3040C	
	V_F	.60 @ 16A	.53 @ 16A	.49 @ 16A		.60 @ 30A	.65 @ 30A	
	I_{FSM}	200A	250A	250A		500A	300A	
45V	TYPE					SD41P	SD241P	USD345C[6]
	V_F	USD745C	USD945	USD1645S	1N6391[5]	USD3045S	USD3045C	SD241[6]
	I_{FSM}	.60 @ 16A	.53 @ 16A	.49 @ 16A	.68 @ 50A	.60 @ 30A	.65 @ 30A	.6 @ 20A
		200A	250A	250A	600A	500A	300A	400A

NOTES: 1. Center-tap 6A per leg.
2. Center-tap 8A per leg.
3. Center-tap 15A per leg.
4. V_{RRM} @ 25°C is 45V, V_{RRM} @ 150°C is 35V.
5. Available as JAN, JANTX, JANTXV.
6. Available with High-Reliability (HR) Screening.
7. Center-tap 23A per leg.

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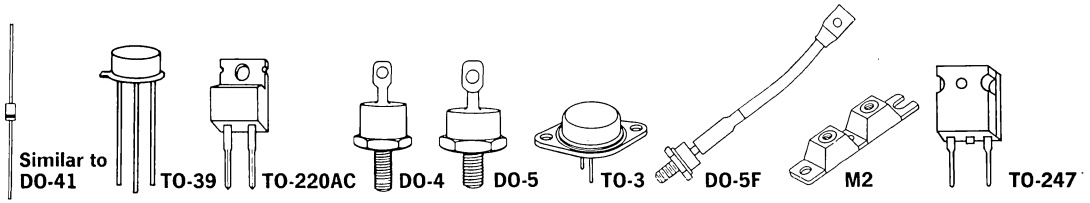

AVERAGE DC OUTPUT CURRENT		45A	45A[7]	50A	60A	75A	75A	200A
PEAK REVERSE VOLTAGE	PKG	TO-247 (2 LEAD)	TO-247 (3 LEAD)	DO-5 STUD	DO-5 DO-5F STUD	DO-5 DO-5F STUD	DO-5 STUD	POWER BLOCK M2
20V	TYPE V_F I_{FSM}					USD520 .6 @ 60A 1000A	USD7520 .425 @ 60A 1000A	
25	TYPE V_F I_{FSM}						USD7525 .425 @ 60A 1000A	
30V	TYPE V_F I_{FSM}	USD4530S .60 @ 45A 500A	USD4530C .60 @ 45A 500A	1N6097 .86 @ 157A 800A				
35V	TYPE V_F I_{FSM}					USD535 .6 @ 60A 1000A		
40V	TYPE V_F I_{FSM}	USD4540C .60 @ 45A 500A	USD4540C .60 @ 45A 500A	1N6098 .86 @ 157A 800A				USM20040C .745 @ 200A 2000A
45V	TYPE V_F I_{FSM}	USD4545S .60 @ 45A 500A	USD4545C .60 @ 45A 500A		1N6392[5] SD51[4] .6 @ 60A 800A	USD545 .6 @ 60A 1000A		USM20045C .745 @ 200A 2000A
50V	TYPE V_F I_{FSM}					USD550 .6 @ 60A 1000A		USM20050C .745 @ 200A 2000A

NOTES: 1. Center-tap 6A per leg.
2. Center-tap 8A per leg.
3. Center-tap 15A per leg.
4. V_{RRM} @ 25°C is 45V, V_{RRM} @ 150°C is 35V.
5. Available as JAN, JANTX, JANTXV.
6. Available with High-Reliability (HR) Screening.
7. Center-tap 23A per leg.

10

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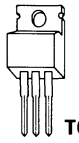
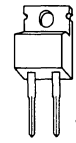


TO-220AB

A

B



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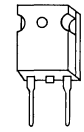
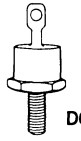


TO-247

ULTRA-FAST RECOVERY (t_{rr} — 25 to 50ns)

Average D.C. Output Current			1A	2A	2.5A	5A	6A	8A	16A	16A	16A Center-Tap
Package Style			**A**	**A**	**A**	**B**	**B**	**TO-220AC**	**TO-220AC**	**TO-247**	**TO-220AB**
Peak Inverse Voltage	50V	V_F t_{rr}	UES1001 .895 @ 1A 25ns		1N5802* UES1101 .895 @ 2A 25ns		1N5807* UES1301 .850 @ 6A 30ns	UES1401 .895 @ 8A 35ns	UES1501 .895 @ 16A 35ns	UES1605S .84 @ 16A 35ns	UES2401 .895 @ 8A 35ns
	75V	V_F t_{rr}			1N5803 .895 @ 1A 25ns		1N5808 .850 @ 6A 30ns				
	100V	V_F t_{rr}	UES1002 .895 @ 1A 25ns		1N5804* UES1102 .895 @ 2A 25ns		1N5809* UES1302 .850 @ 6A 30ns	UES1402 .895 @ 8A 35ns	UES1502 .895 @ 16A 35ns	UES1610S .84 @ 16A 35ns	UES2402 .895 @ 8A 35ns
	125V	V_F t_{rr}			1N5805 .895 @ 1A 25ns		1N5810 .850 @ 6A 30ns				
	150V	V_F t_{rr}	UES1003 .895 @ 1A 25ns		1N5806* UES1103 .895 @ 2A 25ns		1N5811* UES1303 .850 @ 6A 30ns	UES1403 .895 @ 8A 35ns	UES1503 .895 @ 16A 35ns	UES1615S .84 @ 16A 35ns	UES2403 .895 @ 8A 35ns
	200V	V_F t_{rr}		UES1104[1] 1.15 @ 1A 50ns		UES1304[1] 1.15 @ 3A 50ns		UES1404 .895 @ 8A 35ns	UES1504 .895 @ 16A 35ns	UES1620S .84 @ 16A 35ns	UES2404 .895 @ 8A 35ns
	300V	V_F t_{rr}		UES1105[1] 1.15 @ 1A 50ns		UES1305[1] 1.15 @ 3A 50ns					
	400V	V_F t_{rr}		UES1106[1] 1.15 @ 1A 50ns		UES1306[1] 1.15 @ 3A 50ns					

* Available as JAN, JANTX, JANTXV.
1. Available with High Reliability (HR) Screening. See individual datasheets.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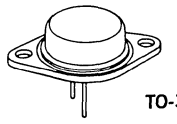
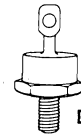

TO-3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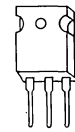
TO-247

ULTRA-FAST RECOVERY (t_{rr} — 25 to 50ns)

Average D.C. Output Current			20A	25A	30A	30A Center-Tap	30A Center-Tap	45A	45A Center-Tap	50A	50A
Package Style			**DO-4**	**DO-4**	**TO-247**	**TO-247**	**TO-3**	**TO-247**	**TO-247**	**DO-5**	**DO-5**
Peak Inverse Voltage	50V	V_F t_{rr}		1N5812* UES701 .825 @ 25A 35ns	UES3005S .95 @ 30A 35ns	UES3005C .95 @ 30A 35ns	UES2601[1] .825 @ 15A 35ns	UES4505S .90 @ 45A 50ns	UES4505C .90 @ 45A 50ns		1N6304* UES801 .84 @ 70A 50ns
	75V	V_F t_{rr}		1N5813 .825 @ 25A 35ns							
	100V	V_F t_{rr}		1N5814* UES702 .825 @ 25A 35ns	UES3010S .95 @ 30A 35ns	UES3010C .95 @ 30A 35ns	UES2602[1] .825 @ 15A 35ns	UES4510S .90 @ 45A 35ns	UES4510C .90 @ 45A 50ns		1N6305* UES802 .84 @ 70A 50ns
	125V	V_F t_{rr}		1N5815 .825 @ 25A 35ns							
	150V	V_F t_{rr}		1N5816* UES703 .825 @ 25A 35ns	UES3015S .95 @ 30A 35ns	UES3015C .95 @ 30A 35ns	UES2603[1] .825 @ 15A 35ns	UES4515S .90 @ 45A 50ns	UES4515C .90 @ 45A 50ns		1N6306* UES803 .84 @ 70A 50ns
	200V	V_F t_{rr}	UES704[1] 1.15 @ 20A 50ns				UES2604[1] 1.15 @ 15A 50ns			UES804[1] 1.15 @ 50A 50ns	
	300V	V_F t_{rr}	UES705[1] 1.15 @ 20A 50ns				UES2605[1] 1.15 @ 15A 50ns			UES805[1] 1.15 @ 50A 50ns	
	400V	V_F t_{rr}	UES706[1] 1.15 @ 20A 50ns				UES2606[1] 1.15 @ 15A 50ns			UES806[1] 1.15 @ 50A 50ns	

* Available as JAN, JANTX, JANTXV.
1. Available with High Reliability (HR) Screening. See individual datasheets.

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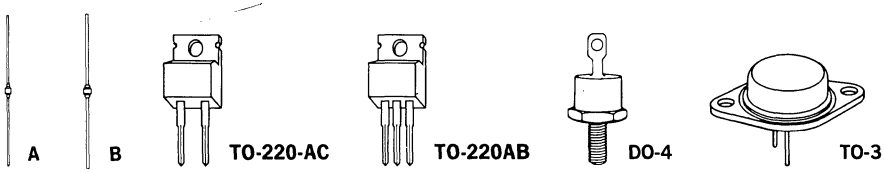

SUPER-FAST RECOVERY (t_{rr} - 75 to 100ns)

Average D.C. Output Current			1A	2A	2A	3A	4A
Package Style			**A**	**A**	**A**	**B**	**B**
Peak Inverse Voltage	50V	V_F t_{rr}	UTX105 1.00 @ .5A 75ns	UTX205 1.0V @ 1A 75ns	SES5001 .975 @ 1A 100ns	UTX3105 1V @ 2A 100ns	UTX4105 1V @ 3A 100ns
	100V	V_F t_{rr}	UTX110 1.0V @ .5A 75ns	UTX210 1.0V @ 1A 75ns	SES5002 .975 @ 1A 100ns	UTX3110 1.0V @ 2A 100ns	UTX4110 1.0V @ 3A 100ns
	150V	V_F t_{rr}	UTX115 1.00 @ .5A 75ns	UTX215 1.0V @ 1A 75ns	SES5003 .975 @ 1A 100ns	UTX3115 1.0V @ 2A 100ns	UTX4115 1.0V @ 3A 100ns
	200V	V_F t_{rr}	UTX120 1.00 @ 1A 75ns	UTX220 1.0V @ 1A 75ns		UTX3120 1.0V @ 2A 100ns	UTX4120 1.0V @ 3A 100ns
	250V	V_F t_{rr}	UTX125 1.00 @ .5A 75ns	UTX225 1.0V @ 1A 75ns			

Average D.C. Output Current			5A	8A	16A Center-Tap	16A	20A	25A Center-Tap	60A
Package Style			**B**	**TO-220AB**	**TO-220AC**	**TO-220AC**	**DO-4**	**TO-3**	**DO-5**
Peak Inverse Voltage	50V	V_F t_{rr}	SES5301 .975 @ 5A 100ns	SES5401 1.025 @ 8A 100ns	SES5401C 1.025 @ 8A 100ns	SES5501 1.025 @ 16A 100ns	SES5701 .83 @ 20A 100ns	SES5601C .83 @ 12.5A 100ns	SES5801 .85 @ 60A 100ns
	100V	V_F t_{rr}	SES5302 .975 @ 5A 100ns	SES5402 1.025 @ 8A 100ns	SES5402C 1.025 @ 8A 100ns	SES5502 1.025 @ 16A 100ns	SES5702 .83 @ 20A 100ns	SES5602C .83 @ 12.5A 100ns	SES5802 .85 @ 60A 100ns
	150V	V_F t_{rr}	SES5303 .975 @ 5A 100ns	SES5403 1.025 @ 8A 100ns	SES5403C 1.025 @ 8A 100ns	SES5503 1.02 @ 16A 100ns	SES5703 .83 @ 20A 100ns	SES5603C .83 @ 12.5A 100ns	SES5803 .85 @ 60A 100ns
	200V	V_F t_{rr}		SES5404 1.025 @ 8A 100ns	SES5404C 1.025 @ 8A 100ns	SES5504 1.02 @ 16A 100ns			

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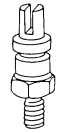
A


B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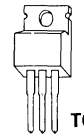
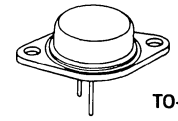

TO-220AB


TO-3

FAST RECOVERY (t_{rr} — 150 to 500ns)

Average D.C. Output Current			1A	1A	2A	3A	3A	4A	6-9A
Package Style			**A**	**A**	**A**	**B**	**B**	**B**	**C**
Peak Inverse Voltage	50V		UTR01		UTR02	UTR3305	1N5415*	UTR4305	UTR4405[1] UTR5405[1] UTR6405[1]
		V_F t_{rr}	1.1V @ .5A 250ns		1.1V @ 1A 250ns	1.1V @ 3A 250ns	1.5V @ 9A 150ns	1.1V @ 4A 250ns	1.1V @ 6A 300ns
	100V		UTR11		UTR12	UTR3310	1N5416* 1N5186**	UTR4310	UTR4410[1] UTR5410[1] UTR6410[1]
		V_F t_{rr}	1.1V @ .5A 250ns		1.1V @ 1A 250ns	1.1V @ 3A 250ns	1.5V @ 9A 150ns	1.1V @ 4A 250ns	1.1V @ 6A 300ns
	200V		UTR21	1N4942* 1N5615*	UTR22	UTR3320	1N5417* 1N5187**	UTR4320	UTR4420[1] UTR5420[1] UTR6420[1]
		V_F t_{rr}	1.1V @ .5A 250ns	1.3V @ 1A 150ns	1.1V @ 1A 250ns	1.1V @ 3A 250ns	1.5V @ 9A 150ns	1.1V @ 4A 250ns	1.1V @ 6A 400ns
	300V		UTR31		UTR32				
		V_F t_{rr}	1.1V @ .5A 300ns		1.1V @ 1A 300ns				
	400V		UTR41	1N4944* 1N5617*	UTR42	UTR3340	1N5418* 1N5188**	UTR4340	UTR4440[1] UTR5440[1] UTR6440[1]
		V_F t_{rr}	1.1V @ .5A 350ns	1.3V @ 1A 150ns	1.1V @ 1A 350ns	1.1V @ 3A 300ns	1.5V @ 9A 150ns	1.1V @ 4A 400ns	1.1V @ 6A 500ns
	500V		UTR51		UTR52	UTR3350	1N5419*	UTR4350	
		V_F t_{rr}	1.1V @ .5A 400ns		1.1V @ 1A 400ns	1.1V @ 3A 350ns	1.5V @ 9A 250ns	1.1V @ 4A 400ns	
	600V		UTR61	1N4946* 1N5619*	UTR62	UTR3360	1N5420* 1N5190**	UTR4360	
		V_F t_{rr}	1.1V @ .5A 400ns	1.3V @ 1A 250ns	1.1V @ 1A 400ns	1.1V @ 3A 400ns	1.5V @ 9A 400ns	1.1V @ 4A 400ns	

* Available as JAN, JANTX, JANTXV.
** Available as JAN, JANTX.
1. Available with High Reliability (HR) Screening. See individual datasheets.

BI-SYNCHRONOUS RECTIFIER

Continuous Forward Current	20A		40A	
Package Style	**TO-220AB**		**TO-3**	
Forward Blocking Voltage, V_{CES}	50V	UBS421	50V	UBS430
h_{FE}	80		50	
$R_{CE(ON)}$	14mΩ Typical		7mΩ Typical	
$V_{CE(SAT)}$	.95V Typical		1.2V Typical	

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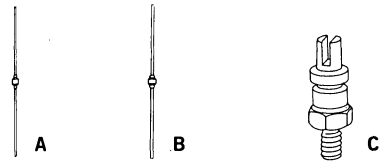

STANDARD RECOVERY

Average D.C. Output Current		1A	2A	3A	4A	7.5A	9A	12A
Package Style		**A**	**A**	**B**	**B**	**C**	**C**	**C**
Peak Inverse Voltage	50V	UR105†	UR205	UT3005	UT4005	UT5105[1]	UT6105[1]	UT8105[1]
	100V	UT236 UT110†	UT261 UT210†	UT3010	UT4010	UT5110[1]	UT6110[1]	UT8110[1]
	150V	UR115†	UR215†					
	200V	UT234 UR120† 1N4245* 1N5614*	UT262 UR220† 1N3611**	UT3020	UT4020 1N5550*	UT5120[1]	UT6120[1]	UT8120[1]
	250V	UR125†	UR225†					
	400V	UT235 1N4246* 1N5616*	UT264 1N3612**	UT3040	UT4040 1N5551*	UT5140[1]	UT6140[1]	UT8140[1]
	600V	UT238 1N4247* 1N5618*	UT267 1N3613**	UT3060	UT4060 1N5552*	UT5160[1]	UT6160[1]	UT8160[1]
	800V	UT361 1N4248* 1N5620*	UT268 1N3614**		1N5553*			
	1000V	UT347 1N4249*	UT364					

* Available as JAN, JANTX, JANTXV.
** Avalable as JAN, JANTX.
† Radiation Tolerant
1. Available with High Reliability (HR) Screening. See individual datasheets.

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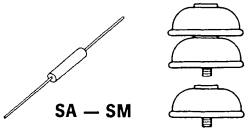

STANDARD RECOVERY

Peak Inverse Voltage	AVERAGE D.C. OUTPUT CURRENT						
	250-.50A	.50-.75A	.75-1A	1-1.5A	2.5-5A	5-6A	6-7A
1.0kV							
1.2kV				US12 **SA**			
1.5kV			US15 **SA**				
1.8kV		US18 **SA**					
2.0kV		US20 **SA**					
2.5kV		US25 **SB**		USB2.5 **DH**	UDB2.5 **DD**	UDE2.5 **DD**	UGE2.5 **DG**
3.0kV		US30 **SB**					
3.5kV	US35 **SC**						
4.0kV	US40 **SC**						
4.5kV	US45A **SD**						

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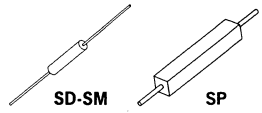

Peak Inverse Voltage	AVERAGE D.C. OUTPUT CURRENT										
	100-250A	250-50A	50-75A	.75-1A	1-1.5A	1.5-2A	2-2.5A	2.5-3A	3-4A	4-5A	5-6A
5.0kV		US50A **SD**	USB5 **DH** USS5 **DH**			UDA5 **DD** UDB5 **DD** 1N5600* **DE**				UDE5 **DG** UGB5 **DD**	UGE5 **DG** 1N5603* **DF**
6.0kV		US60A **SD**			KXS60 **SM**						
7.0kV		US70A **SD**									
7.5kV		USS7.5 **DH**	USB7.5 **DH**		UDA7.5 **DD** UDB7.5 **DD**			UGB7.5 **DG**	UGE7.5 **DG**		
8.0kV	US80A **SE**										
10kV	US100A **SE**	USB10 **DH** USS10 **DH**	688-10 **BE**	UDA10 **DD** 1N5597* **DE**			UGB10 **DG**				
12kV	US120A **SE**	688-12 **BE**									
12.5kV											

*Available as JAN

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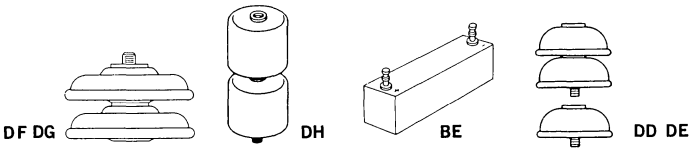

STANDARD RECOVERY

Peak Inverse Voltage	AVERAGE D.C. OUTPUT CURRENT		
	.100-.250A	.250-.50A	.50-.75A
15kV	US150A **SF** USS15 **DH**	688-15 **BE**	UDA15 **DD**
17.5kV			
18kV	US180A **SF**	688-18 **BE**	
20kV	US200A **SF**	688-20 **BE**	
22.5kV			
25kV	688-25 **BE**		

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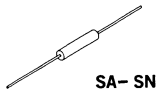

SA– SN

FAST RECOVERY

Peak Inverse Voltage	AVERAGE D.C. OUTPUT CURRENT					
	.100-.250A	.250-.50A	.50-.75A	.75-1.5A	2-2.5A	4-6A
1.0kV						
1.2kV				USR12 **SA**		
1.5kV			USR15 **SA**			
1.8kV			USR18 **SA**			
2.0kV			USR20 **SB**			
2.5kV		USR25 **SB**		UFB2.5 **DH**	UDD2.5 **DD**	UDF2.5 **DD** UGF2.5 **DG**
3.0kV		USR30 **SC**				
3.5kV		USR35 **SC**				
4.0kV		USR40A **SD**				
4.5kV	USR45A **SD**					
Reverse Recovery Time (Max.)	500ns 250ns*	500ns 250ns†	500ns 250ns*	500ns 250ns*	500ns 250ns* 150ns†	500ns

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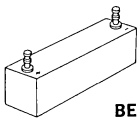
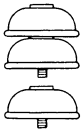
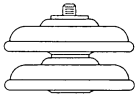
RECTIFIER MODULES


BE


DD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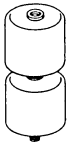
DH

FAST RECOVERY

Peak Inverse Voltage	AVERAGE D.C. OUTPUT CURRENT							
	.100-.250A	.250-.50A	.50-.75A	.75-1A	1-1.5A	1.5-2A	2-2.5A	2.5-4A
5.0kV	USR50A **SD**	UFS5 **DH**	UFB5 **DH**		UDC5 **DD** UDD5 **DD**			UDF5 **DD** UGD5 **DG** UGF5 **DG**
6.0kV	USR60A **SD**							
7.0kV	USR70A **SE**							
7.5kV		UFB7.5 **DH** UFS7.5 **DH**		UDC7.5 **DD** UDD7.5 **DD**			UGD7.5 **DG** UGF7.5 **DG**	
8.0kV	USR80A **SE**							
10kV	USR100A **SE**	UFS10 **DH**	UDC10 **DD** 688-10R **BE**			UGD10 **DG**		
12kV	USR120A **SF**	688-12R **BE**						
12.5kV								
Reverse Recovery Time (Max.)	500ns	500ns	500ns	500ns	500ns	500ns	500ns	500ns

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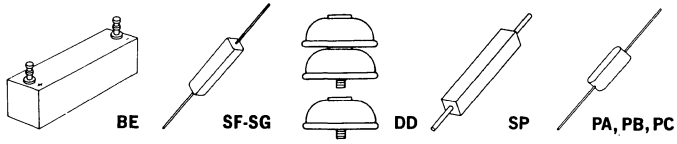
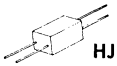


FAST RECOVERY

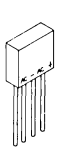
Peak Inverse Voltage	AVERAGE D.C. OUTPUT CURRENT	
	100-250A	250-75A
15kV	USR150A **SF**	UDC15 **DD** 688-15R **BE**
17.5kV		
18kV	USR180A **SF**	688-18R **BE**
20kV	688-20R **BE**	
22.5kV		
25kV	688-25R **BE**	
Reverse Recovery Time (Max.)	500ns	500ns 150ns

RECTIFIER BRIDGES

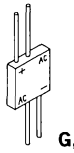
Single Phase Full-Wave Bridges



HJ, HK, HL, HM, HN, HO, HP



S



G, GA, GH

STANDARD RECOVERY

Peak Inverse Voltage Per Leg	AVERAGE D.C. OUTPUT CURRENT					
	≤.25A	.25—.75A	.75—1.5A	1.5—2.5A	4—10A	10—25A
100V			673-1 **G or S**	697-1 **GA**	680-1 **NA**	679-1 **NB** SPA25* **MC**
200V			673-2 **G or S**	697-2 **GA**	680-2 **NA** 469-1** **MD**	679-2 **NB** SPB25* **MC**
300V			673-3 **G or S**	697-3 **GA**	680-3 **NA**	679-3 **NB**
400V			673-4 **G or S**	697-4 **GA**	680-4 **NA** 469-2** **MD**	679-4 **NB** SPC25* **MC**
500V			673-5 **G or S**	697-5 **GA**	680-5 **NA**	679-5 **NB**
600V			673-6 **G or S**	697-6 **GA**	680-6 **NA** 469-3** **MD**	679-6 **NB** SPD25* **MC**
1.2kV		673-7 **GH**				
1.8kV		673-75 **HJ**				
2.4kV		673-8 **HK**				
2.5kV						
3.0kV		673-85 **HL**				
3.6kV	673-9 **HM**					
4.0kV						
4.2kV	673-10 **HN**					
4.8kV	673-11 **HO**					
5.0kV	673-12 **HO**					
7.5kV						
10kV						
15kV						

*Available as JAN
**Available as JAN, JANTX

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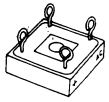
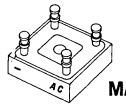
RECTIFIER BRIDGES

PRODUCT SELECTION GUIDE

Single Phase Full-Wave Bridges



NA, NB



MA, MB, MC, MD

FAST RECOVERY

Peak Inverse Voltage Per Leg	AVERAGE D.C. OUTPUT CURRENT							
	≤.25A	.25—.75A	.75—1.5A	1.5—2.5A	4—10A	10—25A		25—35A
50V							803-1 **MB**	802-1 **MA**
100V			676-1 **G or S**	698-1 **GA**	684-1 **NA**	683-1 **NB**	803-2 **MB**	802-2 **MA**
125V							803-3 **MB**	802-3 **MA**
150V							803-4 **MB**	802-4 **MA**
200V			676-2 **G or S**	698-2 **GA**	684-2 **NA**	683-2 **NB**		
300V			676-3 **G or S**	698-3 **GA**	684-3 **NA**	683-3 **NB**		
400V			676-4 **G or S**	698-4 **GA**	684-4 **NA**	683-4 **NB**		
500V			676-5 **G or S**	698-5 **GA**	684-5 **NA**	683-5 **NB**		
600V			676-6 **G or S**	698-6 **GA**	684-6 **NA**	683-6 **NB**		
1.2kV		676-12 **HJ**						
1.8kV		676-18 **HK**						
2.4kV		676-24 **HL**						
2.5kV								
3.0kV		676-30 **HM**						
3.6kV	676-36 **HN**							
4.0kV								
4.2kV	676-42 **HO**							
4.8kV	676-48 **HP**							
5.0kV	676-50 **HP**							
7.5kV								
10kV								
15kV								
Reverse Recovery Time (max.)	500ns	500ns	500ns	500ns	500ns	500ns	50ns	50ns

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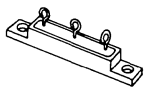
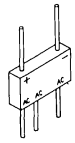
RECTIFIER BRIDGES

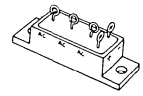
Three Phase Full-Wave Bridge



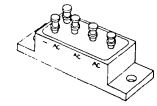
ND



F



NC



ME

STANDARD RECOVERY

Peak Inverse Voltage Per Leg	AVERAGE D.C. OUTPUT CURRENT			
	1—3A	4.5—15A	15—25A	
50V				
100V	700-1 **F**	695-1 **NC**	678-1 **NC**	
125V				
150V				
200V	700-2 **F**	695-2 **NC**	678-2 **NC**	483-1* **ME**
300V	700-3 **F**	695-3 **NC**	678-3 **NC**	
400V	700-4 **F**	695-4 **NC**	678-4 **NC**	483-2* **ME**
500V	700-5 **F**	695-5 **NC**	678-5 **NC**	
600V	700-6 **F**	695-6 **NC**	678-6 **NC**	483-3* **ME**
2.5kV				
5.0kV				
7.5kV				
10kV				

*Available as JANTX

FAST RECOVERY

Peak Inverse Voltage Per Leg	AVERAGE D.C. OUTPUT CURRENT				
	1—3A	4.5—15A	15—25A		25—40A
50V				801-1 **ME**	800-1 **ME**
100V	701-1 **F**	696-1 **NC**	682-1 **NC**	801-2 **ME**	800-2 **ME**
125V				801-3 **ME**	800-3 **ME**
150V				801-4 **ME**	800-4 **ME**
200V	701-2 **F**	696-2 **NC**	682-2 **NC**		
300V	701-3 **F**	696-3 **NC**	682-3 **NC**		
400V	701-4 **F**	696-4 **NC**	682-4 **NC**		
500V	701-5 **F**	696-5 **NC**	682-5 **NC**		
600V	701-6 **F**	696-6 **NC**	682-6 **NC**		
2.5kV					
3.0kV					
4.0kV					
5.0kV					
Reverse Recovery Time (max.)	500ns	500ns	500ns	50ns	50ns

DOUBLERS & CENTER-TAP RECTIFIERS

STANDARD RECOVERY **ND**

Peak Inverse Voltage Per Leg	Average D.C. Output Current
	2—15A
100V	681-1 **ND**
200V	681-2 **ND**
300V	681-3 **ND**
400V	681-4 **ND**
500V	681-5 **ND**
600V	681-6 **ND**

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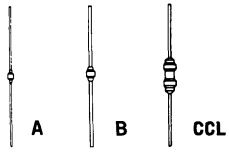
POWER ZENERS AND TRANSIENT VOLTAGE SUPPRESSORS

Transient Voltage Suppressors



Package Style	Part No.	Stand-Off Voltage V_R (V)	Min. Breakdown Voltage BV_{min} @ 1mA (V)	Max. Peak Pulse Current I_{PP} (A)	Max. Clamping Voltage* V_C @ I_{PP} (V)	Peak Power for 1mS (W)
A Body	TVS305	5.0	5.0	17	8.7	150
	TVS310	10.0	11.1	8.9	16.8	
	TVS312	12.0	13.8	7.1	21.0	
	TVS315	15.0	16.7	5.9	25	
	TVS318	18.0	20.4	4.9	31	
	TVS324	24.0	28.4	3.6	42	
	TVS328	28.0	30.7	3.2	46	
	TVS348	48.0	54	1.7	82	
	TVS360	60.0	67	1.4	105	
	TVS410	100.0	111	.91	160	
	TVS420	200.0	234	.42	360	
	TVS430	300.0	342	.28	520	
B Body	TVS505	5.0	6.0	53.7	9.3	500
	TVS510	10.0	11.1	30.3	16.5	
	TVS512	12.0	13.8	23.8	21.0	
	TVS515	15.0	16.7	19.8	25.2	
	TVS518	18.0	20.4	16.3	30.5	
	TVS524	24.0	28.4	11.9	42.0	
	TVS528	28.0	30.7	10.7	46.5	
	1N6461**	5.0	5.6 @ 25mA	56	9	500
	1N6462**	6.0	6.5 @ 20mA	46	11	
	1N6463**	12.0	13.6 @ 5mA	22	22.6	
	1N6464**	15.0	16.4 @ 5mA	19	26.5	
	1N6465**	24.0	27.0 @ 2mA	12	41.4	
	1N6466**	30.5	33.0 @ 1mA	11	47.5	
	1N6467**	40.3	43.7 @ 1mA	8	63.5	
	1N6468**	51.6	54.0 @ 1mA	6	78.5	
CCL	1N5610*		33.0	32.0	47.5	1500
	1N5611*		43.7	24.0	63.5	
	1N5612*		54.0	19.0	79.5	
	1N5613*		191.0	5.7	265.0	

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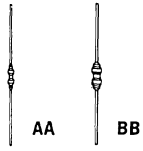
POWER ZENERS AND TRANSIENT VOLTAGE SUPPRESSORS

Bi-directional Zeners



Power		1W	3W	5W
Package Style		AA		BB
Voltage, V (10% Tolerance)	7.5	UDZ8807	UDZ807	UDZ5807
	8.2	UDZ8808	UDZ808	UDZ5808
	9.1	UDZ8809	UDZ809	UDZ5809
	10	UDZ8810	UDZ810	UDZ5810
	12	UDZ8812	UDZ812	UDZ5812
	15	UDZ8815	UDZ815	UDZ5815
	18	UDZ8818	UDZ818	UDZ5818
	20	UDZ8820	UDZ820	UDZ5820
	24	UDZ8824	UDZ824	UDZ5824
	27	UDZ8827	UDZ827	UDZ5827
	30	UDZ8830	UDZ830	UDZ5830
	33	UDZ8833	UDZ833	UDZ5833
	36	UDZ8836	UDZ836	UDZ5836
	40	UDZ8840	UDZ840	UDZ5840
	45	UDZ8845	UDZ845	UDZ5845
	60	UDZ8860	UDZ860	UDZ5860

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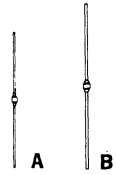
POWER ZENERS AND TRANSIENT VOLTAGE SUPPRESSORS



POWER ZENERS

Power		1W	1.5W	3W	3W	5W	5W	6W	10W
Package Style		A	A	A	A	B	B	CL	C
VOLTAGE V_Z (5% Tolerance)	5.6V						1N5968*		
	6.2V						1N5969*		
	6.8V	UZ8706	1N4461*	1N5063	UZ706[1]	UZ4706	1N4954*	UZ7706L	UZ7706[1]
	7.5V	UZ8707	1N4462*	1N5064	UZ707[1]	UZ4707	1N4955*	UZ7707L	UZ7707[1]
	8.2V	UZ8708	1N4463*	1N5065	UZ708[1]	UZ4708	1N4956*	UZ7708L	UZ7708[1]
	9.1V	UZ8709	1N4464*	1N5066	UZ709[1]	UZ4709	1N4957*	UZ7709L	UZ7709[1]
	10V	UZ8710	1N4465*	1N5067	UZ710[1]	UZ4710	1N4958*	UZ7710L	UZ7710[1]
	11V	UZ8711	1N4466*	1N5068			1N4959*	UZ7711L	UZ7711[1]
	12V	UZ8712	1N4467*	1N4883	UZ712[1]	UZ4712	1N4960*	UZ7712L	UZ7712[1]
	13V	UZ8713	1N4468*	1N5069	UZ713[1]	UZ4713	1N4961*	UZ7713L	UZ7713[1]
	14V	UZ8714		1N5070	UZ714[1]		1N5118	UZ7714L	UZ7714[1]
	15V	UZ8715	1N4469*	1N5071	UZ715[1]	UZ4715	1N4962*	UZ7715L	UZ7715[1]
	16V	UZ8716	1N4470*	1N5072	UZ716[1]	UZ4716	1N4963*	UZ7716L	UZ7716[1]
	18V	UZ8718	1N4471*	1N5073	UZ718[1]	UZ4718	1N4964*	UZ7718L	UZ7718[1]
	20V	UZ8720	1N4472*	1N4884	UZ720[1]	UZ4720	1N4965*	UZ7720L	UZ7720[1]
	22V	UZ8722	1N4473*	1N5074	UZ722[1]	UZ4722	1N4966*	UZ7722L	UZ7722[1]
	24V	UZ8724	1N4474*	1N5075	UZ724[1]	UZ4724	1N4967*	UZ7724L	UZ7724[1]
	27V	UZ8727	1N4475*	1N5076	UZ727[1]	UZ4727	1N4968*	UZ7727L	UZ7727[1]
	30V	UZ8730	1N4476*	1N5077	UZ730[1]	UZ4730	1N4969*	UZ7730L	1N7730[1]
	33V	UZ8733	1N4477*	1N5078	UZ733[1]	UZ4733	1N4970*	UZ7733L	UZ7733[1]
	36V	UZ8736	1N4478*	1N5079	UZ736[1]	UZ4736	1N4971*	UZ7736L	UZ7736[1]
	39V		1N4479*	1N5080		UZ4739	1N4972*		
	40V	UZ8740		1N5081	UZ740[1]		1N5119	UZ7740L	UZ7740[1]
	43V		1N4480*	1N5082		UZ4743	1N4973*[1]		
	45V	UZ8745		1N5083	UZ745[1]		1N5120	UZ7745L	UZ7745[1]
	47V		1N4481*	1N5084		UZ4747	1N4974*		
	50V	UZ8750		1N5085	UZ750[1]		1N5121	UZ7750L	UZ7750[1]
	51V		1N4482*	1N5086		UZ4751	1N4975*		
	56V	UZ8756	1N4483*	1N5087	UZ756[1]	UZ4756	1N4976*	UZ7756L	UZ7756[1]
	60V	UZ8760		1N5088	UZ760[1]		1N5122	UZ7760L	UZ7760[1]
	62V		1N4484*	1N5089		UZ4762	1N4977*		
	68V		1N4485*	1N5090		UZ4768	1N4978*		
PULSE POWER **		100W	140W	230W	230W	720W	900W	2000W	2000W

* Available as JAN, JANTX, & JANTXV
** For 100μs pulse width
† 10% and 20% tolerance also available
*** Pro Electron Diodes 7% tolerance
1. Available with High Reliability (HR) Screening. See individual datasheet

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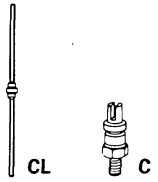
POWER ZENERS AND TRANSIENT VOLTAGE SUPPRESSORS



POWER ZENERS

Power		1W	1.5W	3W	3W	5W	5W	6W	10W
Package Style		A	A	A	A	B	B	CL	C
VOLTAGE V_Z (5% Tolerance)	70V	UZ8770		1N5091	UZ770		1N5123	UZ7770L	UZ7770[1]
	75V	UZ8775	1N4486*	1N5092	UZ775	UZ4775	1N4979*	UZ7775L	UZ7775[1]
	80V	UZ8780		1N5093	UZ780		1N5124	UZ7780L	UZ7780[1]
	82V		1N4487*	1N5094		UZ4782	1N4980*		
	90V	UZ8790		1N4096	UZ790		1N5125	UZ7790L	UZ7790[1]
	91V		1N4488*	1N4095		UZ4791	1N4981*		
	100V	UZ8110	1N4489*	1N4097	UZ110	UZ4110	1N4982*	UZ7110L	UZ7110[1]
	110V	UZ8111	1N4490*	1N5096	UZ111	UZ4111	1N4983*		
	120V	UZ8112	1N4491*	1N5097	UZ112	UZ4112	1N4984*		
	130V	UZ8113	1N4492*	1N5098	UZ113	UZ4113	1N4985*		
	140V	UZ8114		1N5099	UZ114				
	150V	UZ8115	1N4493*	1N4098	UZ115	UZ4115	1V4986*		
	160V	UZ8116	1N4494*	1N5100	UZ116	UZ4116	1V4987*		
	170V	UZ8117		1N5101	UZ117		1V5127		
	180V	UZ8118	1N4495*	1N5102	UZ118	UZ4118	1V4988*		
	190V	UZ8119		1N5103	UZ119		1N5128		
	200V	UZ8120	1N4496*	1N5104	UZ120	UZ4120	1N4989*		
	220V			1N5105	UZ122		1N4990*		
	240V			1N5106	UZ124		1N4991*		
	260V			1N5107	UZ126		1N5129		
	270V			1N5108			1N4992*		
	280V			1N5109	UZ128		1N5130		
	300V			1N5110	UZ130		1N4993*		
	320V			1N5111	UZ132		1N5131		
	330V			1N5112			1N4994*		
	340V			1N5113	UZ134		1N5132		
	360V			1N5114	UZ136		1N4995*		
	380V			1N5115	UZ138		1N5133		
	390V			1N5116			1N4996		
	400V			1N5117	UZ140		1N5134		
PULSE POWER **		100W	140W	230W	230W	720W	900W	2000W	2000W

* Available as JAN, JANTX, & JANTXV
** For 100μs pulse width
† 10% and 20% tolerance also available
*** Pro Electron Diodes 7% tolerance
1. Available with High Reliability (HR) Screening. See individual datasheet

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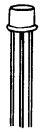
THYRISTORS (SCRs & PUTs)

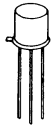
TO-18

SCR	$I_{T(RMS)}$		5A			
	V_{DRM} (V)	30		2N3027*	2N3030*	ID100
		60	AA114	2N3028*	2N3031*	ID101
		100		2N3029*	2N3032*	ID102
		150				ID103
		200	AA116			ID104
		300	AA110			ID105
		400	AA111			ID106
	I_{GT}		200μA	200μA	20μA	200μA
	I_H		2mA	5mA	4mA	5mA



TO-9

SCR	$I_{T(RMS)}$		1.25A	
	V_{DRM} (V)	30	2N1876	2N1870A**
		60	2N1877	2N1871A**
		100	2N1878	2N1872A**
		150	2N1879	2N1873A
		200	2N1880	2N1874A**
	I_{GT}		20μA	200μA
	I_H		3mA	5mA



TO-39

SCR	$I_{T(RMS)}$		1.6A				
	V_{DRM} (V)	30				2N2322	
		60	AD100	2N5724	2N2323A***	2N2323***	1D200
		100	AD101	2N5725	2N2324A***	2N2324***	ID201
		150			2N2325A	2N2325	ID202
		200	AD102	2N5726	2N2326A***	2N2326***	ID203
		300	AD103	2N5727	2N2328A***	2N2328***	ID300
		400	AD104	2N5728		2N2329***	ID301
	I_{GT}		2μA	20μA	20μA	200μA	200μA
	I_H		2mA	2mA	2mA	2mA	3mA

*Available as JAN and JANTX types.
**Available as JAN type.
***Available as JAN, JANTX, JANTXV types.
†3mA available from factory

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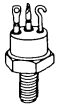
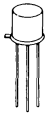
ULTRAFAST SWITCHING

 TO-18	SCR	V_{DRM} (V)	$I_{T(RMS)}$	.4A	
		60V		GA200 GA300	GA200A GA300A
		100V		GA201 GA301	GA201A GA301A
			t_{on}	20ns (TYP.)	20nS (TYP.)
			t_q	2.0μS	.5μS
 TO-59	SCR	V_{DRM} (V)	$I_{T(RMS)}$	6A	
		60V		GB200 GB300	GB200A GB300A
		100V		GB201 GB301	GB201A GB301A
			t_{on}	20ns (TYP.)	20nS (TYP.)
			t_q	2.0μS	.5μS

RADIATION HARDENED SCRs

 TO-18	On-State Current $I_{T(RMS)}$		0.4A
	Package Style		TO-18
	REPETITIVE PEAK OFF-STATE VOLTAGE, V_{DRM} and REVERSE VOLTAGE, V_{RRM}	30V	GA100
		60V	GA101
		80V	GA102
	Key Parameters		I_{GT} (Post 3X10¹⁴ NVT) 20mA
			I_H (Post 3X10¹⁴ NVT) 30mA

PUTs — PROGRAMMABLE UNIJUNCTION TRANSISTORS

 TO-18	Peak Recurrent Forward Current		8A	
	Package Style		TO-18	
	MIN. VALLEY CURRENT, I_v MAX. PEAK POINT CURRENT, I_p	$I_v = 25\mu A$ @ $R_G = 10K$ $I_p = .15\mu A$ @ $R_G = 1Meg$	U13T2	CONSULT FACTORY
		$I_v = 70\mu A$ @ $R_G = 10K$ $I_p = 2\mu A$ @ $R_G = 1Meg$	U13T1	
		$I_v = 1mA$ @ $R_G = 200\Omega$ $I_p = .15\mu A$ @ $R_G = 1Meg$	2N6120	
		$I_v = 1.5mA$ @ $R_G = 200\Omega$ $I_p = 2\mu A$ @ $R_G = 1Meg$	2N6119 2N6137*	
	Forward and Reverse Voltage; V_{AK}, V_{AKR}		40V	100V

* Available as JAN and JANTX types.

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SWITCHING, GENERAL PURPOSE AND STABISTOR DIODES

SWITCHING

Type	Reverse Breakdown Voltage (V)	Average Forward Current (mA)	Forward Voltage (V)	Reverse Recovery Time (ns)	Junction Capacitance (pF)
TID777	20	50	.52-.64 @ 0.1mA	0.75	1.3
TID700	30	50	.52-.61 @ 0.1mA	0.7	0.8
TID778	30	50	1.35 @ 50mA	0.75	1
1N4727	30	75	.79-.85 @ 10mA		4
1N4453	30	200	.51-.63 @ 0.1mA		30
1N4154	35	150	1.0 @ 30mA	2	4
1N251*	40	75	1.0 @ 5mA	150	
1N4152	40	150	.49-.52 @ 0.1mA	2	2
1N4450	40	200	.42-.54 @ 0.1mA	4	4
1N4451	40	200	.4-.5 @ 0.1mA	10	6
1N4452	40	200	.42-.54 @ 0.1mA	50	30
1N4444	70	200	.44-.55 @ 0.1mA	7	2
1N3064**	75	75	1.0 @ 10mA	4	2
1N4532***	75	125	1.0 @ 10mA	4	2
1N4534***	75	150	.74-.88 @ 20mA	4	2
1N4151	75	150	1.0 @ 50mA	2	2
1N4153***	75	150	.49-.55 @ 0.1mA	2	2
1N4305	75	150	.5-.575 @ .25mA	2	2
1N4446	75	150	1.0 @ 20mA	4	4
1N4447	75	150	1.0 @ 20mA	4	2
1N4448	75	150	1.0 @ 100mA	4	4
1N4449	75	150	1.0 @ 30mA	4	2
1N3600***	75	200	.54-.62 @ 1mA	4	2.5
1N4149	75	200	1.0 @ 10mA	4	2
1N4150***	75	200	.54-.62 @ 1mA	4	2.5
1N4454***	75	200	1.0 @ 10mA	2	2
1N4500**	80	300	.64-.72 @ 10mA	6	4
1N4607	85	400	1.1 @ 400mA	10	4
1N4608	85	500	1.1 @ 500mA	10	4
1N662*	100	40	1.0 @ 10mA	500	3
1N663*	100	40	1.0 @ 100mA	500	3
1N914**	100	75	1.0 @ 10mA	5	4
1N4531***	100	125	1.0 @ 10mA	5	4
1N4148***	100	200	1.0 @ 10mA	4	4
1N3070**	200	100	1.0 @ 100mA	50	5
1N4938**	200	150	1.0 @ 10mA	50	5

GENERAL PURPOSE

Type	Reverse Voltage (V)	Average Forward Current (mA)	Forward Voltage (V)	Reverse Recovery Time (ns)	Junction Capacitance (pF)
1N456	30	90	1.0 @ 40mA		
1N457*	70	75	1.0 @ 20mA		
1N483B**	80	200	1.0 @ 100mA		
1N458*	150	55	1.0 @ 7mA		
1N3595***	150	150	.83-1.0 @ 200mA	3μs	2.5
1N459*	200	40	1.0 @ 3mA		
1N643*	200	40	1.0 @ 10mA	300	3
1N485B**	200	200	1.0 @ 100mA		
1N645***	270	400	1.0 @ 400mA		20
1N647**	480	400	1.0 @ 400mA		20

* Available as JAN. ** Available as JAN, JANTX. *** Available as JAN, JANTX, JANTXV.

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SWITCHING, GENERAL PURPOSE AND STABISTOR DIODES

LOW LEAKAGE

Type	Reverse Breakdown Voltage (V)	Average Forward Current (mA)	Forward Voltage (V)	Reverse Leakage Current (nA)	Junction Capacitance (pF)
DE104	40	74	.61-.70 @ 0.1mA	.02 @ 20V	4
DE110	40	74	.59-.69 @ 0.1mA	2 @ 30V	4
DE111	40	74	.59-.69 @ 0.1mA	.2 @ 20V	4
DE112	40	74	1.0 @ 50mA	0.1 @ 20V	6
DE113	40	74	1.0 @ 50mA	0.25 @ 20V	6
DE114	40	74	.59-.69 @ 0.1mA		4
DE115	40	74	.59-.69 @ 0.1mA	2 @ 50V	4

STABISTOR

Type	Reverse Breakdown Voltage (V)	Forward Voltage (V)	Reverse Leakage Current (nA)	Junction Capacitance (pF)
1N4156	30	.97-1.22 @ 0.1mA	50 @ 20V	25
1N4157	30	1.52-1.77 @ 0.1mA	50 @ 20V	20
1N4453	30	.51-.63 @ 0.1mA	50 @ 20V	30
1N5179	30	1.8-2.5 @ 0.1mA	50 @ 20V	20
1N4829	30 @ 100μA	.84-1.25 @ 0.1mA	100 @ 20V	25
1N4830	30 @ 100μA	1.35-1.8 @ 0.1mA	100 @ 20V	20
MPD200	30	1.05-1.16 @ 0.1mA	30 @ 30V	15
MPD300	60	1.62-1.78 @ 0.1mA	30 @ 30V	10
MPD400	90	2.47-2.71 @ 0.1mA	30 @ 30V	7
STB567	12	1.31-1.61 @ 10mA		
STB568	12	2.09-2.31 @ 10mA		
STB569	12	2.73-3.01 @ 10mA		

PROELECTRON SWITCHING DIODES

Type	Reverse Voltage (V)	Average Forward Current (mA)	Forward Voltage (V)	Reverse Recovery Time (ns)	Reverse Current @ 25°C (μA)	Junction Capacitance (pF)
BAY60	25	115	1.0 @ 30mA	4	0.1 @ 25V	4
BAW75	35	300	1.0 @ 30mA	2	5 @ 35V	4
BAY41	40	225	1.0 @ 200mA	8.5	5 @ 40V	5
BAW24	50	600	1.0 @ 50mA	6	0.1 @ 40V	4
BAW25	50	600	0.8 @ 50mA	6	0.1 @ 40V	4
BAY42	60	225	1.0 @ 200mA	15	5 @ 60V	5
BAW26	75	600	1.0 @ 50mA	6	0.1 @ 60V	4
BAW27	75	600	1.0 @ 200mA	6	0.1 @ 40V	4
BAW76	75	300	1.0 @ 100mA	2	5 @ 75V	2
BAY43	80	225	1.0 @ 200mA	15	5 @ 80V	5
BAX12	90	400	1.25 @ 400mA	15	0.1 @ 90V	20

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PIN DIODES

For applications information, see PIN Diode Designers' Handbook and Catalog (PD-500B)

SWITCHING PIN DIODES

Type	Voltage Rating Range	Capacitance (OV, 1 GHz) C_T max.	Forward Resistance (100mA, 1 GHz) R_S max.	Parallel Resistance (100V, 1 GHz) R_p min.	Average Thermal Resistance θ_A max.	Average Power Dissipation P_A max.	Peak Power Dissipation P_p max.	Carrier Lifetime I_F = 10mA τ min.
	(V)	(pF)	(Ω)	(KΩ)	(°C/W)	(W)	(KW)	(μS)
UM4000	100-1000	3.0	0.5	2	6	25	100	5.0
UM4900	100-600	3.0	0.5	2	4	37	100	5.0
UM6000	100-1000	0.5	1.7	15	25	6	25	1.0
UM6200	100-400	1.1	0.4	10	25	6	10	0.6
UM6600	100-1000	0.4	2.5	10	35	4	13	1.0
UM7000	100-1000	0.9	1.0	10	15	10	60	2.5
UM7100	100-800	1.2	0.6	8	15	10	35	2.0
UM7200	100-400	2.2	0.25	7	15	10	20	1.5

HIGH POWER ATTENUATOR & MODULATOR PIN DIODES

Type	Voltage Ratings Range	Total Capacitance (OV, 1 GHz) C_T max.	RF Resistance (100mA, 1 GHz) R_S max.	RF Resistance (10μA, 1 GHz) R_S min.	Average Thermal Resistance θ_A max.	Average Power Dissipation P_A max.	Carrier Lifetime I_F = 10mA τ min.
	(V)	(pF)	(Ω)	(Ω)	(°C/W)	(W)	(μs)
UM4300	100-1000	2.2	1.5	1000	8	18	5.0
UM7300	100-1000	0.7	3.0	3000	20	7.5	2.5

GENERAL PURPOSE PIN DIODE

Type	Voltage Rating (I_R=10μA)	Total Capacitance (50V, 1MHz) C_T max.	RF Resistance (10μA, 100 MHz) R_S min.	RF Resistance (20mA, 100 MHz) R_S max.	RF Resistance (100mA, 100MHz) R_S max.	Carrier Lifetime (I_R = 10mA) τ min.
	(V)	(pF)	(Ω)	(Ω)	(Ω)	(μS)
1N5767	100	0.4	1000 3000 typ.	8 4 typ.	2.5 1.5 typ.	1

LOW DISTORTION ATTENUATOR PIN DIODES

Type	Voltage Rating I_R=10μA	Total Capacitance (0V, 100MHz) C_T max.	RF Resistance (100mA, 100MHz) R_S max.	RF Resistance (10μA, 100 MHz) R_S min.	Forward Current (R_S = 75Ω F = 100MHz) Typ.	Carrier Lifetime (I_F=10mA) Typ.
	(V)	(pF)	(Ω)	(Ω)	I_F (mA)	τ (μs)
1N5957	100	0.4	3.5	1500	1.0	2
UM9301	75	0.8	3.0	3000	1.1	4

TWO WAY RADIO ANTENNA SWITCHES

Type	Voltage Rating (I_R=10μA)	Total Capacitance (0V, 100MHz) C_T max.	RF Resistance (50mA, 100MHz) R_F max.	Transmit Harmonic Distortion F = 50MHz I = 20mA	Receive Third Order Distortion (Pin-10mW, 0 Bias) FA=50MHz FB=51MHz Max.	Average Power Dissipation P_A Max.
	(V)	(pF)	(Ω)	(dB)	(dB)	(W)
UM9401 and UM9402	50	1.5	1.0	−80	−60	5.5
UM9415	50	4.0	1.0	−80	60	10

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PIN DIODES

For applications information, see PIN Diode Designers' Handbook and Catalog (PD-500B)

LOW RESISTANCE ANTENNA SWITCHES

Type	Voltage Rating (I_R = 10μA)	Total Capacitance (50V, 1MHz) C_T max	RF Resistance (10mA, 100MHz) R_S max	Forward Bias Third Order I_M Distortion I = 10mA F_a = 43MHz F_b = 44MHz max	Reverse Bias Third Order I_M Distortion V = 50V F_a = 43MHz F_b = 44MHz max	Average Power Dissipation P_A max
	(V)	(pF)	(Ω)	(dB)	(dB)	(W)
UM9701	100	1.8	.8	−90	−90	2.5

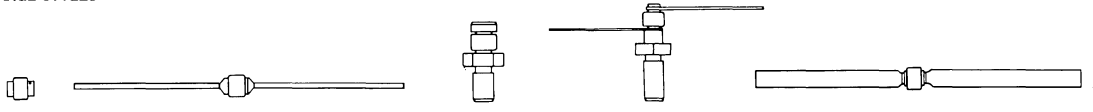
MICROSTRIP PACKAGED DIODES

Type	Series Resistance R_S max.	Parallel Resistance R_P min.	Total Capacitance C_T max.	Carrier Lifetime τ min.	Voltage Rating	Forward Voltage V_F typ.
	(Ω)	(KΩ)	(pF)	(μs)	(V)	(V)
UM9601-UM9604	0.6	5	1.2	2.0	100, 400	.85
UM9605-UM9608	1.7	7	0.5	1.0	100, 400	.95

RADIATION DETECTOR

Type	Photocurrent 10^6 Rad (Si)/s, 50V Flash X-Ray, 2.5 MeV mA min.	Maximum Photocurrent	Reverse Current 50V μA max.	Capacitance F = 1 MHz, V = 50V pF max.
UM9441	4.0	3A dc, $3A^2s$ pulsed	1.0	10

PACKAGE STYLES



A Style Basic Diode

B Style Round Axial Leads

***C Style** Stud

***D Style** Insulated Stud

E Style Ribbon Axial Leads

*Not available for UM6000, UM6600, UM6200.

For UM9600 Series

Cup UM9601/2

Cup UM9605/6

Flange UM9603/4

Flange UM9607/8

Drawings are not actual size.

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The following series are available in surface mount packaging: UM7000, UM7200, UM7300, UM9301, UM9401.

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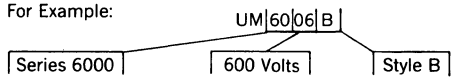
VOLTAGE RATINGS

Series	100V	200V	400V	600V	800V	1000V
UM4000	√	√		√		√
UM4300	√	√		√		√
UM4900	√	√		√		
UM6000	√	√		√		√
UM6200	√	√	√			
UM6600	√	√		√		√
UM7000	√	√		√		√
UM7100	√	√	√		√	
UM7200	√	√	√			
UM7300	√	√		√		√

ORDERING INFORMATION

Part numbers of Switching and High Power Attenuator PIN diodes consist of the letters UM followed by four digits and one or two letters. The first two digits indicate the diode series, the next two digits specify the voltage rating in hundreds of volts. The remaining letters denote the package style. Reverse polarity is available for C, and D, style and denoted by adding second letter R.

For Example:



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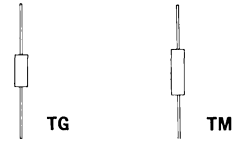

Type	Resistance Range (Ω)	Resistance Range (R25°C/R125°C)	Tolerance	Package
TG1/8-J	10-10K	0.55±15%	5%	TG
TG1/8-K	10-10K	0.55±15%	10%	TG
TM1/8-J	10-39K	0.55±15%	5%	TM
TM1/8-K	10-39K	0.55±15%	10%	TM
TM1/4-J	10-10K	0.55±15%	5%	TM
TM1/4-K	10-10K	0.55±15%	10%	TM
RTH22 ES-J	10-10K	0.55±15%	5%	TM
RTH22 ES-K	10-10K	0.55±15%	10%	TM
RTH42 ES-J	10-2.7K	0.55±15%	5%	TG
RTH42 ES-K	10-2.7K	0.55±15%	10%	TG

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TYPE NUMBER DESIGNATION **TM1/8272K**

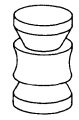
TM 1/8 272 K

STYLE	WATTAGE	RESISTANCE VALUE CODE	TOLERANCE
TM	1/8	270 = 27Ω	J = 5%
TG		271 = 270Ω	K = 10%
RTH22 ES		272 = 2,700Ω	
RTH42 ES		273 = 27,000Ω	

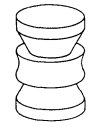
10

SURFACE MOUNT PACKAGES

Ultra-Fast & Standard Recovery Rectifiers



MELF A



MELF B

ULTRA-FAST RECTIFIERS

Average D.C. Output Current			2A	3A	4A	7A	8A
Package Style			**Melf A**	**Melf A**	**Melf A**	**Melf B**	**Melf B**
Peak Inverse Voltage	50V	t_{rr}	UES1001SM 25ns		UES1101MS 25ns		UES1301SM 30ns
	100V	t_{rr}	UES1002SM 25ns		UES1102SM 25ns		UES1302SM 30ns
	150V	t_{rr}	UES1003SM 25ns		UES1103SM 25ns		UES1303SM 30ns
	200V	t_{rr}		UES1104SM 50ns		UES1304SM 50ns	
	300V	t_{rr}		UES1105SM 50ns		UES1305SM 50ns	
	400V	t_{rr}		UES1106SM 50ns		UES1306SM 50ns	

STANDARD RECOVERY RECTIFIERS

Average D.C. Output Current		2A	4A	8A
Package Style		**Melf A**	**Melf A**	**Melf B**
Peak Inverse Voltage	200V	SM3611 SM4245	SM5614	SM5550
	400V	SM3612 SM4246	SM5616	SM5551
	600V	SM3613 SM4247	SM5618	SM5552
	800V	SM3614 SM4248	SM5620	SM5553
	1000V	SM4249		

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SURFACE MOUNT PACKAGES

Power Zeners & Transient Voltage Suppressors

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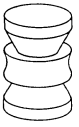

MELF B

POWER ZENERS

Power		3W	10W
Package Style		Melf A	Melf B
Voltage Vz (5% Tolerance)	5.6V		SM5968
	6.2V		SM5969
	6.8V	SM4461	SM4954
	7.5V	SM4462	SM4955
	8.2V	SM4463	SM4956
	9.1V	SM4464	SM4957
	10V	SM4465	SM4958
	11V	SM4466	SM4959
	12V	SM4467	SM4960
	13V	SM4468	SM4961
	15V	SM4469	SM4962
	16V	SM4470	SM4963
	18V	SM4471	SM4964
	20V	SM4472	SM4965
	22V	SM4473	SM4966
	24V	SM4474	SM4967
	27V	SM4475	SM4968
	30V	SM4476	SM4969
	33V	SM4477	SM4970
	36V	SM4478	SM4971
	39V	SM4479	SM4972
	43V	SM4480	SM4973
	47V	SM4481	SM4974
	51V	SM4482	SM4975
	56V	SM4483	SM4976
	62V	SM4484	SM4977

POWER ZENERS

Power		3W	10W
Package Style		Melf A	Melf B
Voltage Vz (5% Tolerance)	68V	SM4485	SM4978
	75V	SM4486	SM4979
	82V	SM4487	SM4980
	91V	SM4488	SM4981
	100V	SM4489	SM4982
	110V	SM4490	SM4983
	120V	SM4491	SM4984
	130V	SM4492	SM4985
	150V	SM4493	SM4986
	160V	SM4494	SM4987
	180V	SM4495	SM4988
	200V	SM4496	SM4989
	220V		SM4990
	240V		SM4991
	270V		SM4992
	300V		SM4993
	330V		SM4994
	360V		SM4995
	390V		SM4996

TRANSIENT VOLTAGE SUPPRESSORS

Part No.			Stand-Off Voltage V_R	Min. Breakdown Voltage $BV_{(min)}$ @ 1mA	Max. Peak Pulse Current I_{PP}	Max. Clamping Voltage V_C @ I_{PP}	Peak Power for 1mS
			(V)	(V)	(A)	(V)	(W)
Package Style	Melf B	SM6461	5.0	5.6 @ 25mA	56	9	500
		SM6462	6.0	6.5 @ 20mA	46	11	
		SM6463	12.0	13.6 @ 5mA	22	22.6	
		SM6464	15.0	16.4 @ 5mA	19	26.5	
		SM6465	24.0	27.0 @ 2mA	12	41.4	
		SM6466	30.5	33.0 @ 1mA	11	47.5	
		SM6467	40.3	43.7 @ 1mA	8	63.5	
		SM6468	51.6	54.0 @ 1mA	6	78.5	

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