VIA Technologies Incorporated

VT1612A

Stereo AC'97 Codec with S/PDIF

Features

- AC'97 2.2 compliant codec
- 18-bit stereo full-duplex ΣΔ codec
- 1Hz resolution VSR (Variable Sampling Rate)
- Integrated IEC958 line driver for S/PDIF output
- S/PDIF compressed digital or LPCM audio out
- 3D stereo expansion for simulated surround
- 18-bit independent rate stereo ADC/DAC
- Hardware VU peak meters for PCM streams
- 4 stereo, 2 mono analog line-level inputs
- Alt. line-level output with volume control, or
- Headphone Amplifier with Thermal Protection
- Low Power consumption mode
- Exceeds Microsoft® WHQL logo requirements
- 3.3V digital, 3.3 or 5V analog power supply
- 48-pin LQFP small footprint package

Description

VIA Technologies' VT1612A™ 18-bit ΣΔ audio codec conforms to the AC'97 2.2 and S/PDIF specifications. The VT1612A integrates Sample Rate Converters and can be adjusted in 1 Hz increments. The analog mixer circuitry integrates a stereo enhancement to provide a pleasing 3D surround sound effect for stereo media. Furthermore, an integrated headphone amplifier with thermal shutdown adds signal value by reducing the BOM. This codec is designed with aggressive power management to achieve low power consumption. When used with a 3.3V analog supply, power consumption is further reduced. The primary applications for this part are desktop and portable personal computers multimedia subsystems. However, it is suitable for any audio subsystem requiring stereo audio input / output with S/PDIF digital output at competitive prices.

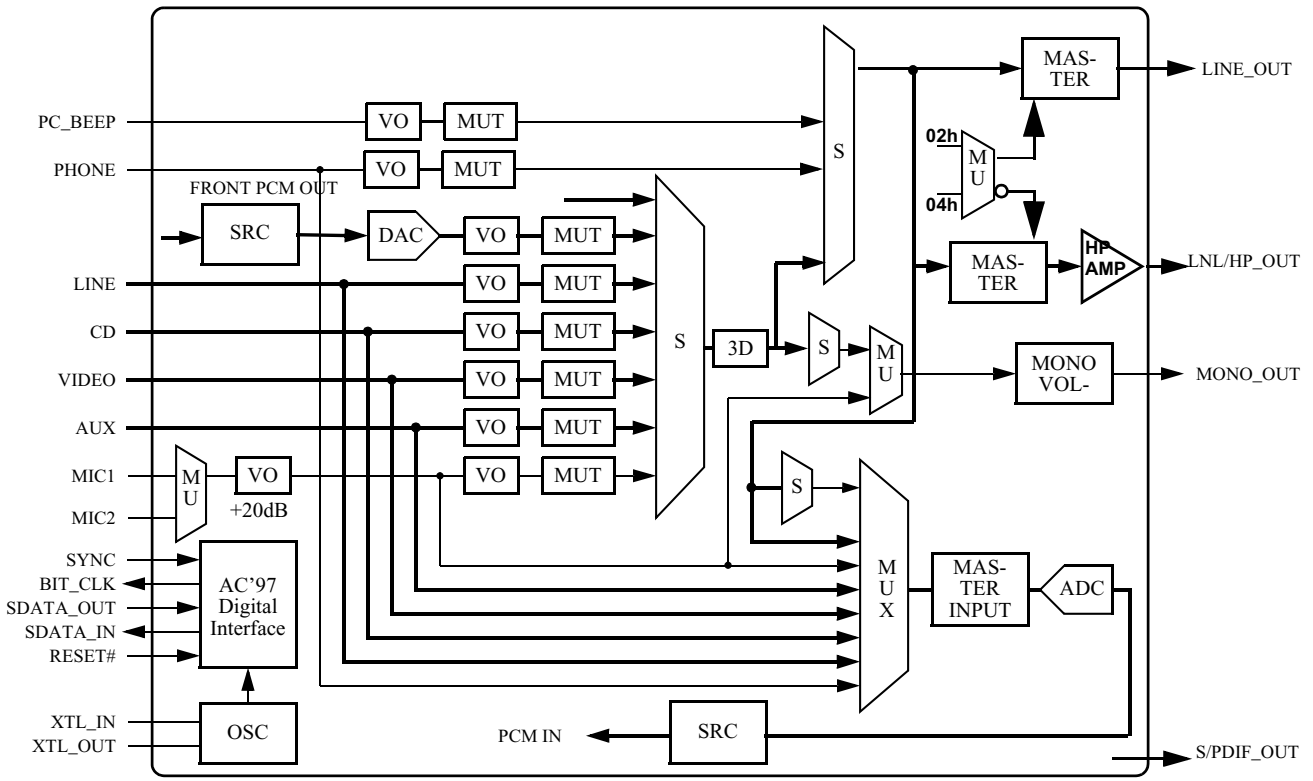

Figure 1. Functional Block Diagram

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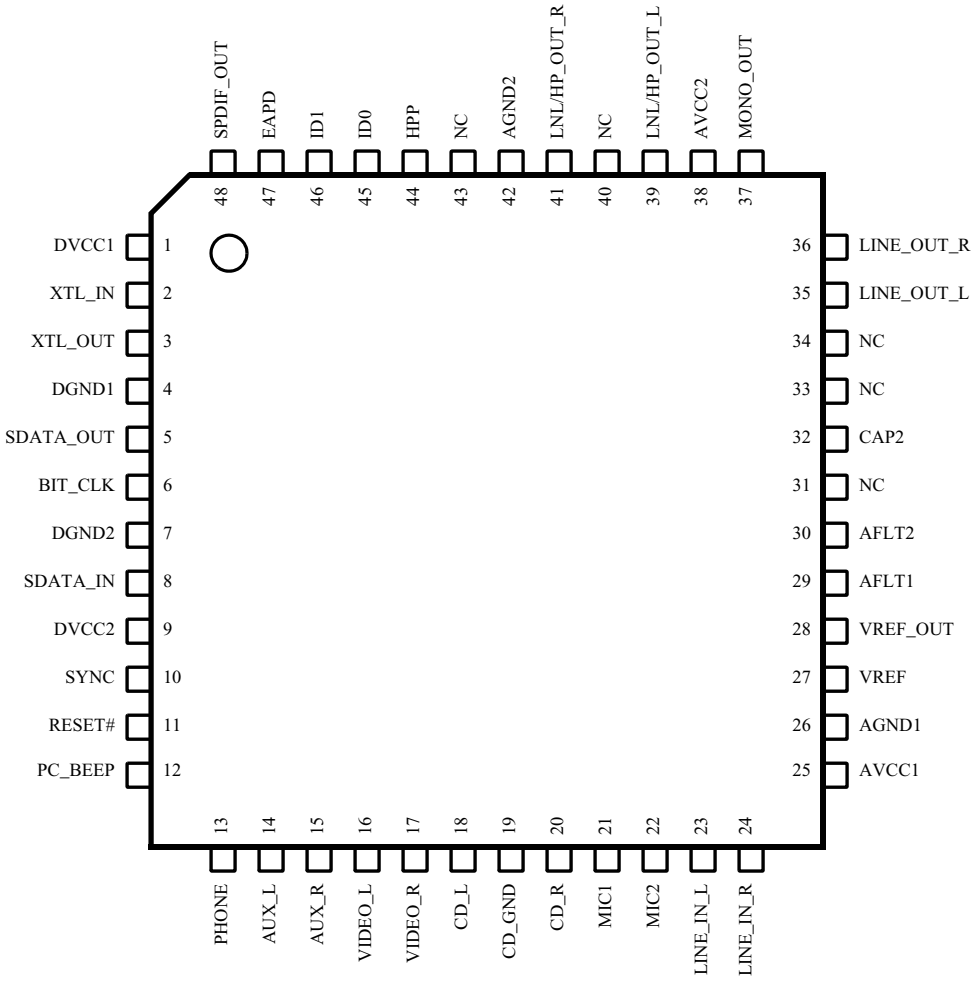


Figure 2. Pin Diagram - 48-Pin LQFP

Table 1. Pin Descriptions

Pin #	Symbol	Type	Description
1	DVCC1	P	Digital Supply Voltage, 3.3V only
2	XTL_IN	I	24.576 MHz Crystal or clock input
3	XTL_OUT	O	24.576 MHz Crystal
4	DGND1	P	Digital Ground
5	SDATA_OUT	I	AC'97 Serial Data Input Stream
6	BIT_CLK	I/O	12.288 MHz Serial Data Clock
7	DGND2	P	Digital Ground
8	SDATA_IN	O	AC'97 Serial Data Output Stream
9	DVCC2	P	Digital Supply Voltage, 3.3V only
10	SYNC	I	48 KHz Fixed Rate Sync Pulse
11	RESET#	I	AC'97 Master Reset
12	PC_BEEP	I	PC Speaker Beep Pass Through
13	PHONE	I	Telephony Subsystem Speakerphone
14	AUX_L	I	Auxiliary Audio Left Channel
15	AUX_R	I	Auxiliary Audio Right Channel
16	VIDEO_L	I	Video Audio Left Channel
17	VIDEO_R	I	Video Audio Right Channel
18	CD_L	I	CD Audio Left Channel
19	CD_GND	I	CD Audio Analog Ground
20	CD_R	I	CD Audio Right Channel
21	MIC1	I	Desktop Microphone
22	MIC2	I	Second Microphone
23	LINE_IN_L	I	Line In Left Channel
24	LINE_IN_R	I	Line In Right Channel
25	AVCC1	P	Analog Supply Voltage, 5V or 3.3V
26	AGND1	P	Analog Ground
27	VREF	I	Reference Voltage
28	VREF_OUT	O	Reference Voltage Output
29	AFLT1	O	Left Channel Anti-Aliasing Filter Capacitor
30	AFLT2	O	Right Channel Anti-Aliasing Filter Capacitor
31	NC	–	No Connect
32	CAP2	–	ADC Reference Voltage Capacitor
33	NC	–	No Connect
34	NC	–	No Connect
35	LINE_OUT_L	O	Line Out Left Channel
36	LINE_OUT_R	O	Line Out Right Channel
37	MONO_OUT	O	Mono Output
38	AVCC2	P	Analog Supply Voltage, 5V or 3.3V
39	LNL/HP_OUT_L	O	Alternate Left Line Level out or Left Headphone Output
40	NC	–	No Connect

Table 1. Pin Descriptions (*continued...*)

Pin #	Symbol	Type	Description
41	LNL / HP_OUT_R	O	Alternate Right Line Level out or Right Headphone Output
42	AGND2	P	Analog Ground
43	NC	–	No Connect
44	HPP	I	Headphone Volume Control Routing selection (Internal pull-up)
45	ID0	I	Multiple Codec Select (Internal pull-up). *Please see **Table 5**.*
46	ID1	I	Multiple Codec Select (Internal pull-up). *Please see **Table 5**.*
47	EAPD	O	External Power Amplifier Power Down
48	SPDIF_OUT	I/O	PCM/Non-Audio Sony/Philips Digital I/F Output (Internal pull-up). If left floating, S/PDIF not implemented reported on 2Ah, bit 2 = "0"

Note: The VT1612A supports +5V or +3.3V analog power supply. For best analog performance use 5V analog supply. For maximum power savings use 3.3V for both analog and digital sections. You must use 3.3V as digital supply. The digital I/Os are **NOT** 5V tolerant.

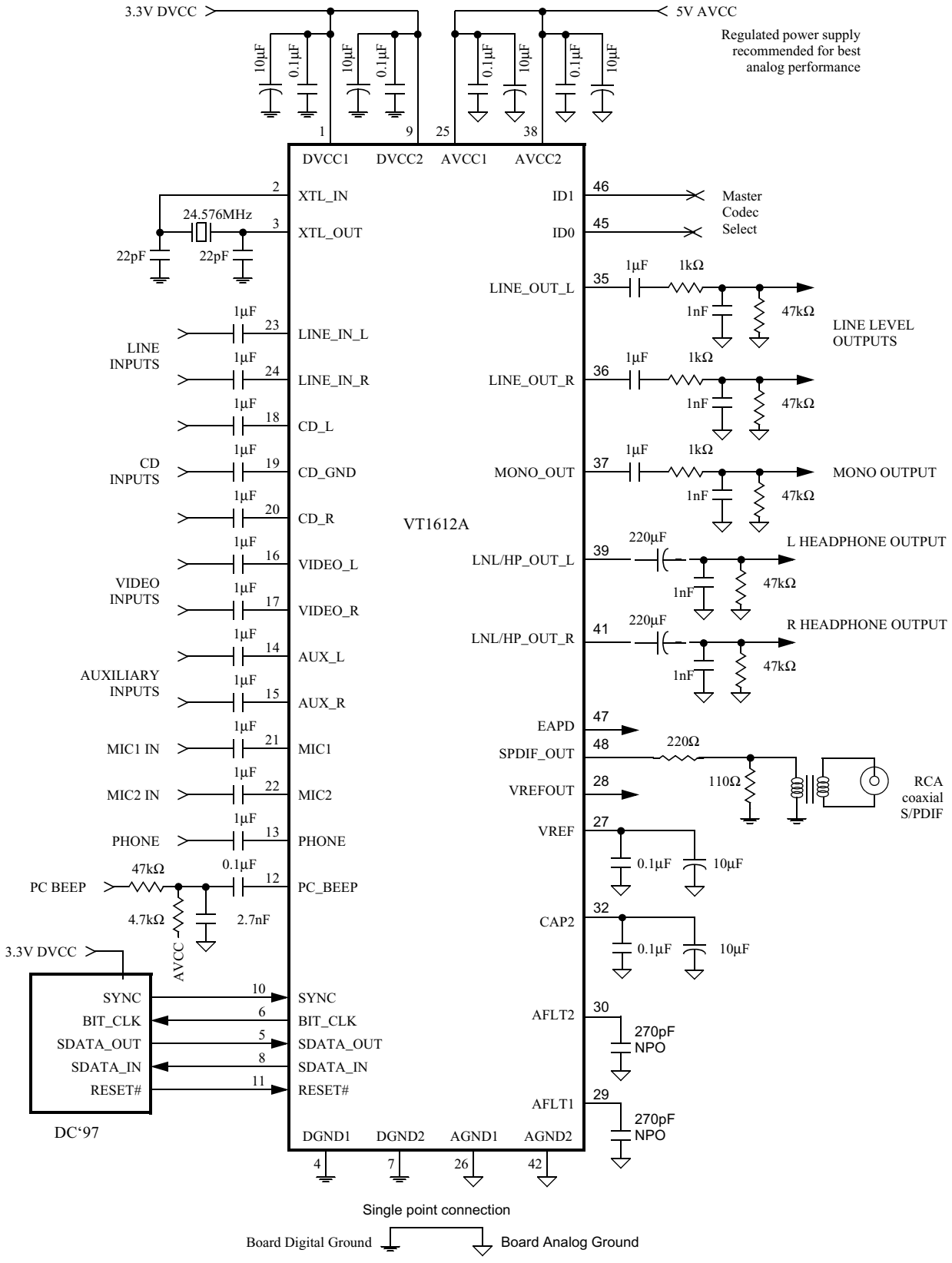


Figure 3. Typical Connection Diagram

Register Map

Index	Register Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	Reset	–	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
02h	Stereo Output Volume	Mute	–	–	ML4	ML3	ML2	ML1	ML0	–	–	–	MR4	MR3	MR2	MR1	MR0
04h	Alt. Line Output Vol.	Mute	–	–	ML4	ML3	ML2	ML1	ML0	–	–	–	MR4	MR3	MR2	MR1	MR0
06h	Mono Output Volume	Mute	–	–	–	–	–	–	–	–	–	–	MM4	MM3	MM2	MM1	MM0
0Ah	PC Beep Volume	Mute	–	–	–	–	–	–	–	–	–	–	PV3	PV2	PV1	PV0	–
0Ch	Phone Volume	Mute	–	–	–	–	–	–	–	–	–	–	GN4	GN3	GN2	GN1	GN0
0Eh	Mic In Volume	Mute	–	–	–	–	–	–	–	–	20dB	–	GN4	GN3	GN2	GN1	GN0
10h	Line In Volume	Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0
12h	CD In Volume	Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0
14h	Video In Volume	Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0
16h	Aux In Volume	Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0
18h	PCM Out volume	Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0
1Ah	Record Select	–	–	–	–	–	SL2	SL1	SL0	–	–	–	–	–	SR2	SR1	SR0
1Ch	Record Gain	Mute	–	–	–	GL3	GL2	GL1	GL0	–	–	–	–	GR3	GR2	GR1	GR0
20h	General Purpose	–	–	3D	–	–	–	MIX	MS	LPBK	–	–	–	–	–	–	–
22h	3D Control	–	–	–	–	–	–	–	–	–	–	–	–	DP3	DP2	DP1	DP0
26h	Power Down & Status	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	–	–	–	–	REF	ANL	DAC	ADC
28h	Extended Audio ID	ID1	ID0	–	–	–	–	–	LDAC	SDAC	CDAC	–	–	–	SPDIF	–	VRA
2Ah	Ext. Audio Stat/Control	–	–	PRK	PRJ	PRI	SPCV	–	LDAC	SDAC	CDAC	SSA1	SSA0	–	SPDIF	–	VRA
2Ch	PCM Front DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
32h	PCM LR ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
3Ah	S/PDIF Control	V	–	SSR1	SSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	/PCM	PRO
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
5Ah	Test Control Register	Res.	Res.	Res.	Res.	Res.	BPDC	DC	Res.	Res.	Res.	Res.	Res.	IB1	IB0	Res.	Res.
5Ch	Special Control Reg.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	HPS	HPP	SNP	Res.	DSM
5Eh	DAC VU peak meter	VDL7	VDL6	VDL5	VDL4	VDL3	VDL2	VDL1	VDL0	VDR7	VDR5	VDR5	VDR4	VDR3	VDR2	VDR1	VDR0
60h	ADC VU peak meter	VAL7	VAL6	VAL5	VAL4	VAL3	VAL2	VAL1	VAL0	VAR7	VAR6	VAR5	VAR4	VAR3	VAR2	VAR1	VAR0
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
7Ah	Vendor Reserved	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0

In compliance with the AC '97 rev. 2.2 specification, all reserved or non-implemented register bits, non-implemented addresses, odd register addresses return 0 when read. Vendor specific registers 5Ah - 7Ah are reserved for special functions, testing and similar operations.

Register Description

Reset Register (Index 00h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
–	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	6D50h

The Reset register is used to configure the hardware to a known state or to read the ID code of the part. A code was assigned to VIA Technologies (27 = 11011h) for 3D Stereo Enhancement reflected in SE[4:0]. ID8 and ID6 are set to 1b to report that the ADC and DAC are 18-bit resolution respectively. The VT1612A supports an alternate line level out with independent volume control as reflected by ID4=1b. However, since pins 39 and 41 are shared with the Surround DAC outputs, register 5Ah, bit 15, LVL has to be set to "1". Writing data to this register will set all the mixer registers to their default values. For description of the bits set to 0b, refer to AC'97 Rev. 2.1 spec.

Stereo Output Control Register (Index 02h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	ML4	ML3	ML2	ML1	ML0	–	–	–	MR4	MR3	MR2	MR1	MR0	8000h

Mute **Stereo Output Mute Control**

"1" : Mute enabled

"0" : Mute disabled

ML[4:0] **Master Output (Left Channel) Volume Control**

These five bits select the level of attenuation applied to the Left channel of the Stereo Output signal. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 2** on page 9 for details.

MR[4:0] **Master Output (Right Channel) Volume Control**

These five bits select the level of attenuation applied to the Right channel of the Stereo Output signal. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 2** on page 9 for details.

Alternate Line Output Control Register (Index 04h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	ML4	ML3	ML2	ML1	ML0	–	–	–	MR4	MR3	MR2	MR1	MR0	8000h

Mute **Stereo Output Mute Control**

"1" : Mute enabled

"0" : Mute disabled

ML[4:0] **Alternate Line Output (Left Channel) Volume Control**

These six bits select the level of attenuation applied to the Left channel of the Stereo Output signal. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 2** on page 9 for details.

MR[4:0] **Alternate Line Output (Right Channel) Volume Control**

These five bits select the level of attenuation applied to the Right channel of the Stereo Output signal. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 2** on page 9 for details.

Mono Output Control Register (Index 06h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	–	–	–	–	–	–	–	–	MM4	MM3	MM2	MM1	MM0	8000h

Mute **Mono Output Mute Control**

"1" : Mute enabled

"0" : Mute disabled

MM[4:0] **Mono Output Volume Control**

These five bits select the level of attenuation applied to the Mono Output signal. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 2** on page 9 for details.

Table 2. Stereo and Mono Output Attenuation

	M4	M3	M2	M1	M0	Level (dB)
0	0	0	0	0	0	0.0
1	0	0	0	0	1	-1.5
2	0	0	0	1	0	-3.0
3	0	0	0	1	1	-4.5
4	0	0	1	0	0	-6.0
5	0	0	1	0	1	-7.5
..	..	..	..	..	..	..
..	..	..	..	..	..	..
28	1	1	1	0	0	-42.0
29	1	1	1	0	1	-43.5
30	1	1	1	1	0	-45.0
31	1	1	1	1	1	-46.5

PC Beep Input Volume Control Register (Index 0Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	–	–	–	–	–	–	–	–	PV3	PV2	PV1	PV0	–	8000h

Mute **PC Beep Input Mute Control**

"1" : Mute enabled

"0" : Mute disabled

PV[3:0] **PC Beep Input Volume Control**

These four bits select the level of attenuation applied to the PC beep input signal. The level of attenuation is programmable from 0dB to -45dB in 3dB increments, providing a total of 16 programmable levels. The beep gain is set at 0dB when PV[3:0] = 0h. Even though the default of the input volume control is mute, as long as RESET# is active, PC Beep will be passively routed to the line outputs.

Phone Input Volume Control Register (Index 0Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	–	–	–	–	–	–	–	–	GN4	GN3	GN2	GN1	GN0	8008h

Mute **Phone Input Mute Control**

"1" : Mute enabled

"0" : Mute disabled

GN[4:0] **Phone Input Volume Control**

These five bits select the gain applied to the Phone Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 3** on page 13 for details.

Mic Input Volume Control Register (Index 0Eh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	–	–	–	–	–	–	20dB	–	GN4	GN3	GN2	GN1	GN0	8008h

Mute **Mic Input Mute Control**

"1" : Mute enabled

"0" : Mute disabled

20dB **Mic Boost Control**

"1" : Fixed 20dB gain enabled

"0" : Fixed 20dB gain disabled

GN[4:0] **Mic Input Volume Control**

These five bits select the gain applied to the Mic Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 3** on page 13 for details.

Line Input Control Register (Index 10h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0	8808h

Mute **Line Input Mute Control**

"1" : Mute enabled
"0" : Mute disabled

GL[4:0] **Left Channel Gain Control**

These five bits select the gain applied to the LEFT channel of the Line Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 3** on page 13 for details.

GR[4:0] **Right Channel Gain Control**

These five bits select the gain applied to the RIGHT channel of the Line Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 3** on page 13 for details.

CD Input Control Register (Index 12h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0	8808h

Mute **CD Input Mute Control**

"1" : Mute enabled
"0" : Mute disabled

GL[4:0] **Left Channel Gain Control**

These five bits select the gain applied to the Left channel of the CD Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 3** on page 13 for details.

GR[4:0] **Right Channel Gain Control**

These five bits select the gain applied to the Right channel of the CD Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 3** on page 13 for details.

Video Input Control Register (Index 14h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0	8808h

Mute **Video Input Mute Control**

"1" : Mute enabled "0":Mute disabled

GL[4:0] **Left Channel Gain Control**

These five bits select the gain applied to the Left channel of the Video Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 3** on page 13 for details.

GR[4:0] **Right Channel Gain Control**

These five bits select the gain applied to the Right channel of the Video Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 3** on page 13 for details.

Auxiliary Input Control Register (Index 16h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0	8808h

Mute **Auxiliary Input Mute Control**

"1" : Mute enabled "0":Mute disabled

GL[4:0] **Left Channel Gain Control**

These five bits select the gain applied to the Left channel of the Auxiliary Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 3** on page 13 for details.

GR[4:0] **Right Channel Gain Control**

These five bits select the gain applied to the Right channel of the Auxiliary Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 3** on page 13 for details.

PCM Output Control Register (Index 18h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0	8808h

Mute **PCM Output Mute Control**

"1" : Mute enabled

"0" : Mute disabled

GL[4:0] **Left Channel Gain Control**

These five bits select the gain applied to the LEFT channel of the PCM Output signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 3** on page 13 for details.

GR[4:0] **Right Channel Gain Control**

These five bits select the gain applied to the RIGHT channel of the PCM Output signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 3** (below) on page 13 for details.

Table 3. Programmable Mixer Input Gain Levels

	G4	G3	G2	G1	G0	Level (dB)
0	0	0	0	0	0	12.0
1	0	0	0	0	1	10.5
2	0	0	0	1	0	9.0
3	0	0	0	1	1	7.5
4	0	0	1	0	0	6.0
5	0	0	1	0	1	4.5
6	0	0	1	1	0	3.0
7	0	0	1	1	1	1.5
8	0	1	0	0	0	0.0
9	0	1	0	0	1	-1.5
10	0	1	0	1	0	-3.0
11	0	1	0	1	1	-4.5
12	0	1	1	0	0	-6.0
13	0	1	1	0	1	-7.5
14	0	1	1	1	0	-9.0
15	0	1	1	1	1	-10.5
16	1	0	0	0	0	-12.0
17	1	0	0	0	1	-13.5
18	1	0	0	1	0	-15.0
19	1	0	0	1	1	-16.5
20	1	0	1	0	0	-18.0
21	1	0	1	0	1	-19.5
22	1	0	1	1	0	-21.0
23	1	0	1	1	1	-22.5
24	1	1	0	0	0	-24.0
25	1	1	0	0	1	-25.5
26	1	1	0	1	0	-27.0
27	1	1	0	1	1	-28.5
28	1	1	1	0	0	-30.0
29	1	1	1	0	1	-31.5
30	1	1	1	1	0	-33.0
31	1	1	1	1	1	-34.5

Record Select Register (Index 1Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
–	–	–	–	–	SL2	SL1	SL0	–	–	–	–	–	SR2	SR1	SR0	0000h

SL[2:0] **Record Source Select (Left Channel)**

These bits determine the record source for the left channel.

SL2	SL1	SL0	Left Record Source
0	0	0	Mic
0	0	1	CD (L)
0	1	0	Video In (L)
0	1	1	Aux In (L)
1	0	0	Line In (L)
1	0	1	Stereo Mix (L)
1	1	0	Mono Mix
1	1	1	Phone

SR[2:0] **Record Source Select (Right Channel)**

These bits determine the record source for the right channel.

SR2	SR1	SR0	Right Record Source
0	0	0	Mic
0	0	1	CD (R)
0	1	0	Video In (R)
0	1	1	Aux In (R)
1	0	0	Line In (R)
1	0	1	Stereo Mix (R)
1	1	0	Mono Mix
1	1	1	Phone

Record Gain Control Register (Index 1Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	–	GL3	GL2	GL1	GL0	–	–	–	–	GR3	GR2	GR1	GR0	8000h

Mute **Record Mute Control**

"1" : Mute enabled
"0" : Mute disabled

GL[3:0] **Record Gain Control (Left Channel)**

These four bits select the gain applied to the LEFT channel recording source. The gain is programmable from 0dB to 22.5dB in 1.5dB increments, providing a total of 16 programmable levels. The gain is set at 0dB when GL[3:0] = 0h.

GR[3:0] **Record Gain Control (Right Channel)**

These four bits select the gain applied to the RIGHT channel recording source. The gain is programmable from 0dB to 22.5dB in 1.5dB increments, providing a total of 16 programmable levels. The gain is set at 0dB when GR[3:0] = 0h.

General Purpose Register (Index 20h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
–	–	3D	–	–	–	MIX	MS	LPBK	–	–	–	–	–	–	–	0000h

3D **3D Stereo Enhancement**

"1" : Enable 3D
"0" : Disable 3D

MIX **Mono Output Mode**

"1" : Mic Output
"0" : Mono mix output

MS **Microphone Select**

"1" : Microphone 2
"0" : Microphone 1

LPBK **Loopback Mode**

For this bit to be valid, 5C_0 must be set to "1". See description of LBE on page 22.
"1" : DAC/ADC Loopback enabled
"0" : DAC/ADC Loopback disabled

3D Control Register (Index 22h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
–	–	–	–	–	–	–	–	–	–	–	–	DP3	DP2	DP1	DP0	0000h

DP[3:0] **3D Depth Control**

These four bits control the linear depth control of the 3D stereo enhancement built into the codec. The gain is programmable from 0% to 100% in 6.67% increments, providing a total of 16 programmable levels. The default value corresponds to no stereo enhancement.

Table 4. 3D Depth Control

	DP3	DP2	DP1	DP0	Level (%)
0	0	0	0	0	0.0
1	0	0	0	1	6.67
2	0	0	1	0	13.33
3	0	0	1	1	20
4	0	1	0	0	26.67
5	0	1	0	1	33.33
..	..	..	..	..	..
..	..	..	..	..	..
12	1	1	0	0	80
13	1	1	0	1	86.67
14	1	1	1	0	93.33
15	1	1	1	1	100

Power Down and Status Register (Index 26h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	–	–	–	–	REF	ANL	DAC	ADC	0000h

EAPD **Enable Amplifier Power Down**

"1" : Powerdown External Power Amplifier

"0" : External Power Amplifier active

The signal polarity at pin 47, EAPD is identical to bit description.

PR[6:0] **Power Down Mode Bits**

These read/write bits are used to control the power down states of the VT1612A. Each power down function bit is enabled by setting the respective bit high. Particularly, PR5 has no effect unless PR0, PR1 and PR4 are all set to "1". This implies that the codec can be woken up by a warm reset, because warm reset clears PR4, which in turn disables the function of PR5. The register bit, however will not be cleared by a warm reset. The power down modes controlled by each bit is described in the table below:

Bit	Function
PR0	ADC and Mux Powerdown
PR1	DAC Powerdown
PR2	Mixer Powerdown (VREF on)
PR3	Mixer Powerdown (VREF off)
PR4	AC Link Powerdown (BIT_CLK off)
PR5	Internal Clock Disabled
PR6	Alternate Line Out Powerdown

REF,ANL,ADC,DACStatus (Read-Only) Bits

These bits are used to monitor the readiness of some sections of the VT1612A. Reading a "1" from any of these bits would be an indication of a "ready" state.

Bit	Status Bit
REF	VREF at nominal level
ANL	Mixer, Mux and Volume Controls ready
DAC	DAC ready to accept data
ADC	ADC ready to transmit data

Extended Audio ID Register (Index 28h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
ID1	ID0	–	–	–	–	AMAP	–	–	–	–	–	–	SPDIF	–	VRA	020xh

The Extended Audio ID is a read only register that indicates the capabilities of the VT1612A.

ID[1:0] **(See Table below)**

Table 5. Multiple Codec Mode Status Bits

ID1	ID0	Codec Mode
0	0	Primary Codec (default)
0	1	Secondary Codec 1
1	0	Secondary Codec 2
1	1	Secondary Codec 3

Note: The state of the ID pins is reported in reverse polarity on register 28h, bits D15 and D14. If you use this table to configure the codec via pins 45 and 46, use the inverse values. Please, refer to **Figure 4** on page 24. BIT_CLK is an output for the primary codec and an input pin for the controller and secondary codecs. ID[1:0] pins with internal pull-up resistors defaults codec as primary codec.

AMAP **Slot/DAC mapping based on Codec ID**

"1" : Feature applicable on VT1612A.

SPDIF **Sony/Philips Digital Audio Interface**

"1" : Feature implemented in compliance to AC '97, Rev 2.2, S/PDIF Output

"0" : Indicates that SPDIF_OUT pin 48 is left floating or pulled-high. It reflects the lack of external S/PDIF application circuitry.

VRA **Variable Sampling Rate PCM Audio**

"1" : Feature implemented in compliance to AC '97 2.1 Appendix A

Extended Audio Status/Control Register (Index 2Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
–	–	–	–	–	SPCV	–	–	–	–	SSA1	SSA0	–	SPDIF	–	VRA	0000h

SPCV **S/PDIF Configuration Valid (Read Only)**

"0" : S/PDIF configuration (SSA, SSR, DAC rate, DRS) invalid (not supported)
"1" : S/PDIF configuration (SSA, SSR, DAC rate, DRS) valid (supported)

SSA[1:0] **S/PDIF Slot Assignment**

These bits determine the S/PDIF data source from AC-link slot selection when SPDIF_OUT, pin 48 is low during reset (pulled low by external application circuit). If the S/PDIF application circuit is not implemented, these bits will return only 0. The default state reflects the pervasive design feature of common AC'97 digital controllers supporting slots 3 & 4. Slots 10 & 11 are expected to be used in the future to support concurrent 6 channels analog and 2 channel digital audio (compressed or LPCM).

SSA1	SSA0	S/PDIF Source Data
0	0	AC-link slots 3 & 4 (front stereo pair, power-up default)
0	1	AC-link slots 7 & 8 (surround pair)
1	0	AC-link slots 6 & 9 (LFE & Center pair)
1	1	AC-link slots 10 &11

SPDIF **Sony/Philips Digital Audio Interface Enable/Disable**

"1" : Set this bit to turn on the S/PDIF transmitter.
"0" : The S/PDIF transmitter is off by default.

VRA **Variable Sampling Rate Mode control**

"1" : Enable VSR
"0" : Fixed 48 KHz sampling rate

PCM DAC Sample Rate Register (Index 2Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

SR[15:0] **DAC Sample Rate (in Hz)**

16-bit unsigned value representing the sample rate in 1Hz resolution. The default value is 48 KHz (48000 = BB80h).

PCM ADC Sample Rate Register (Index 32h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

SR[15:0] **ADC Sample Rate (in Hz)**

16-bit unsigned value representing the sample rate in 1Hz resolution. The default value is 48 KHz (48000 = BB80h).

S/PDIF Control Register (Index 3Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
V	–	SSR1	SSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	/PCM	PRO	x000h

This read/write register controls the S/PDIF functionality when SPDIF bit at 28h_2 reports S/PDIF is implemented. It will return 0000h when SPDIF_OUT, pin 48 left floating or pulled high. If S/PDIF is implemented for the final product, it will read 2000h at power-up. The register manages the bit fields propagated as channel status (or subframe in the V case). With the exception of V, this register should only be written when the S/PDIF transmitter is disabled (SPDIF bit at 2Ah_2 is "0"). This ensures that control and status information start up correctly at the beginning of S/PDIF transmission.

V **Validity**

This bit affects the "Validity flag", bit 28 transmitted in each subframe and enables the S/PDIF transmitter to maintain connection during error or mute conditions.

"0" : If a valid Left/Right pair was received via AC-link and transmitted through S/PDIF, the Validity bit should be reset to "0"

"1" : Tags both samples as invalid by setting bit 28, "Validity flag" to "1"

SSR[1:0] **S/PDIF Sample Rate**

These bits declare the available S/PDIF transmitter clock rate (64*fs).

SSR1	SSR0	S/PDIF Sample Rate
0	0	Not Available
0	1	Reserved
1	0	48 KHz (default)
1	1	Not Available

L **Generation Level**

Programmed according to IEC standards.

CC[6:0] **Category Code**

Programmed according to IEC standards.

PRE **Preemphasis**

"1" : Indicates filter preemphasis is 50/15µs.

"0" : Default is no Preemphasis.

COPY **Copyright**

"1" : Indicates copyright is asserted.

"0" : Copyright is not asserted (default).

/PCM **Non-Audio Samples**

"1" : Set this bit for transmitting non-PCM audio samples such as AC-3.

"0" : Indicates samples are linear PCM suitable for direct conversion to audio playback. .

PRO **Professional**

"1" : Set Professional mode. Set this bit in conjunction with /PCM bit (above) for AC-3.

"0" : Indicates Consumer mode (default).

Vendor Reserved Register (Index 5Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Res.	Res.	Res.	Res.	Res.	BPDC	DC	Res.	Res.	Res.	Res.	Res.	IB1	IB0	Res.	Res.	8200h

Res. **Test Mode Bits**

These read/write bits are used for testing the digital modes of the audio codec. Do not access them during Normal operation.

BPDC **ADC DC-offset Removal Control**

When set to "1", the DC-offset cancellation circuit will be enabled. The default setting of "0" ensures that the circuit is disabled at power up.

DC **DC-offset Removal Capability**

This read only bit indicates that the codec incorporates DC-offset removal hardware.

IB[1:0] **Analog Current Setting Bits**

Normally these bits should be left at default when analog operating at 5V supply. The four possible settings adjust the power consumption of the analog section. The power-up default 00b sets the codec for the best overall analog performance at 5V. At 3.3V analog supply, 10b should be set for the lowest power instead of default 00b. This mode is desirable for system designs with limited power budget such as battery operated portable devices. Setting to 11b puts the codec to its best A-A mixer performance overall.

IB1	IB0	Analog Current Setting
0	0	Normal (1X)
0	1	Reduced (4/5X)
1	0	Power Miser (2/3X)
1	1	Enhanced (4/3X)

Vendor Reserved Register (Index 5Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	HPT	HPE	HPS	HPP	SNP	Res.	DSM	0018h

DSM **DAC Soft-Mute Control**

When set to "1", the DAC soft mute control is disabled. By default, when the DAC sees 4096 consecutive zeroes, its output is muted.

SNP **Register Write Cycle Snoop**

When this bit is set to '1' and the codec is set to secondary (ID = 01b, 10b or 11b), any register write cycle to the primary codec is snooped and register contents updated accordingly.

HPP **Headphone Amplifier Volume Control Toggle**

This bit reports the status of the headphone volume control register selection from pin 44, HPP. If pin 44, HPP is left floating or pulled high, the register will report '1' and the default register 04h definition will apply. If pulled low, the functionality of 02h will be transposed with 04h. This condition is overwritable by HPR bit described below.

HPS **Master Volume Control Swap**

This bit is for software override of HPP, the bit described above. If this bit is reset to '0', register 02h functionality will be transposed with 04h. Both HPP and HPS have the same priority and hence the last bit written will determine the register routing.

HPE **Headphone Amplifier Temperature Sensing Control**

This bit when set to '1' disables the built-in thermal sensor for protection of the heaphone amplifier. Default power-up state '0', thermal protection is on. If the thermal ceiling is exceeded, the heaphone output will be shut off.

HPT **Headphone Amplifier Thermal Protection Shutdown**

This read only bit gets automatically set to '1' and reports when the thermal protection threshold has been exceeded. It will be reset to '0' when the offending high temperature condition is removed and the normal operation state is re-entered.

Res. **Test Mode Bits**

These read/write bits are used for testing the digital modes of the audio codec. Do not access them during Normal operation.

DAC output PCM Peak Meter Register (Index 5Eh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
VDL7	VDL6	VDL5	VDL4	VDL3	VDL2	VDL1	VDL0	VDR7	VDR5	VDR5	VDR4	VDR3	VDR2	VDR1	VDR0	0000h

VDL[7:0] **Left Output PCM Peak Meter Value**

This byte keeps track of the largest PCM value played back on the DAC Left channel. The register is reset when the it is read. Any amplitude below -48dBFS cannot be displayed.

VDR[7:0] **Right Output PCM Peak Meter Value**

This byte keeps track of the largest PCM value played back on the DAC Right channel.

The register is reset when the it is read. Any amplitude below -48dBFS cannot be displayed.

ADC output PCM Peak Meter Register (Index 60h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
VAL7	VAL6	VAL5	VAL4	VAL3	VAL2	VAL1	VAL0	VAR7	VAR6	VAR5	VAR4	VAR3	VAR2	VAR1	VAR0	0000h

VDL[7:0] **Left Output PCM Peak Meter Value**

This byte keeps track of the largest PCM value played back on the DAC Left channel. The register is reset when the it is read. Any amplitude below -48dBFS cannot be displayed.

VDR[7:0] **Right Output PCM Peak Meter Value**

This byte keeps track of the largest PCM value played back on the DAC Right channel.

The register is reset when the it is read. Any amplitude below -48dBFS cannot be displayed.

Vendor Identification Register (Index 7Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	5649h

The upper and lower byte of this register (index 7Ch), in conjunction with the upper byte of index register 7Eh, make up the vendor identification code for the VT1612A. The Vendor ID Code (in ASCII format) is equal to "VIA", where:

F[7:0] **Upper Byte (Index 7Ch) D[15:8] = V**

S[7:0] **Lower Byte (Index 7Ch) D[7:0] = I**

T[15:8] **Upper Byte (Index 7Eh) D[15:8] = A**

Revision Identification Register (Index 7Eh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	4161h

The upper byte of this register is used in conjunction with index register 7Ch to make up the Vendor ID code for the VT1612A. The lower byte identifies VT1612A and its revision code.

T[15:8] **See description in Vendor Identification Register.**

REV[7:0] **Revision ID**

"61": VT1612A identification and revision number

Note: As a reference, other valid Rev IDs associated with VIA AC'97 products are: "01h" for the VT1611 (ICE1230), "11h" for the VT1611A (ICE1232), "51h" for the VT1616 and "41h" for the VT1612.

Multiple Codec Example

The primary codec provides the master BIT_CLK. The secondary codec, if any, and the controller, will use this clock to work in synchronous mode. Note that the ID[1:0] pins are internally pulled up; therefore, it is necessary to pull the ID[1:0] pins low to set the codec as secondary. Notice that the state of the ID[1:0] pins are reflected in reverse polarity as shown on **Table 5** on page 18. See Reg. 28h for more details.

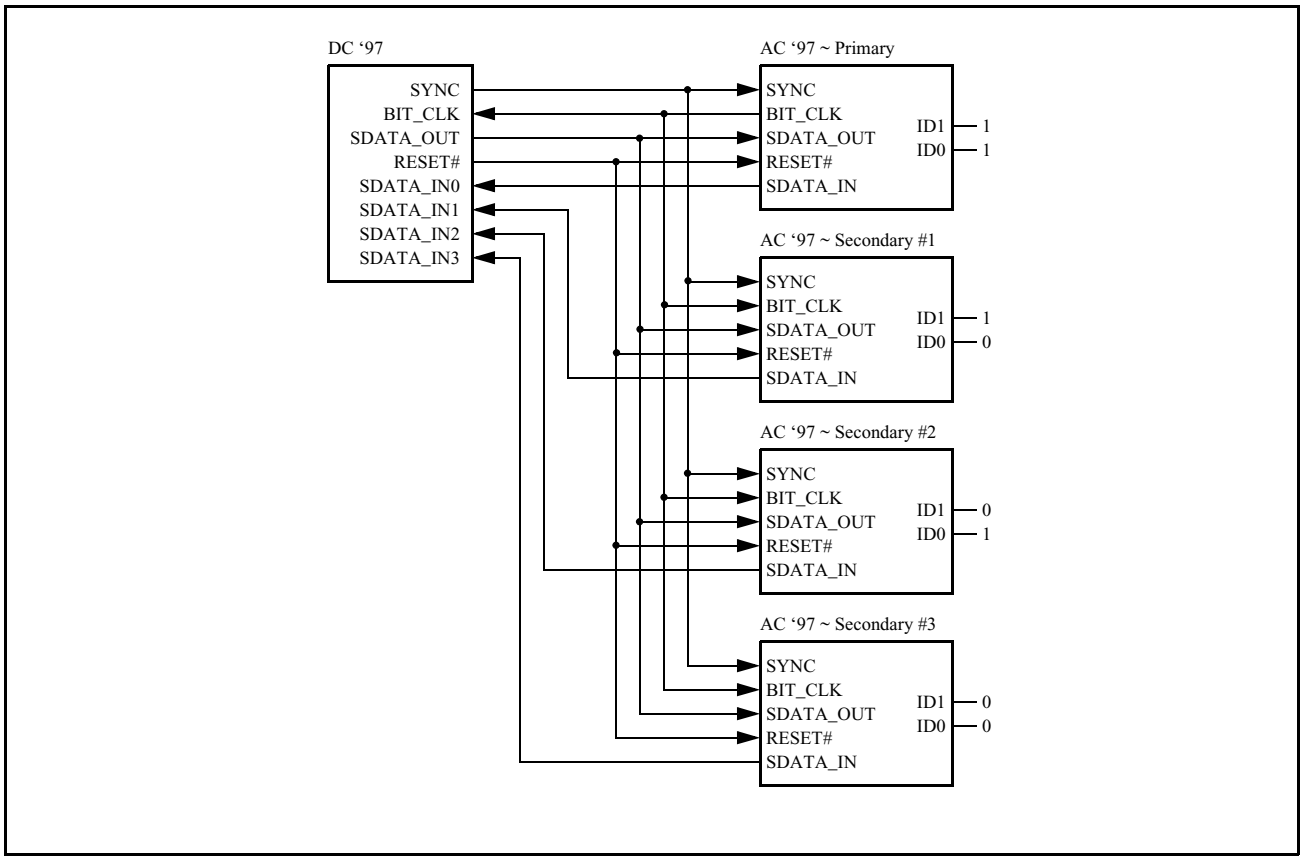


Figure 4. Multiple Codec Example

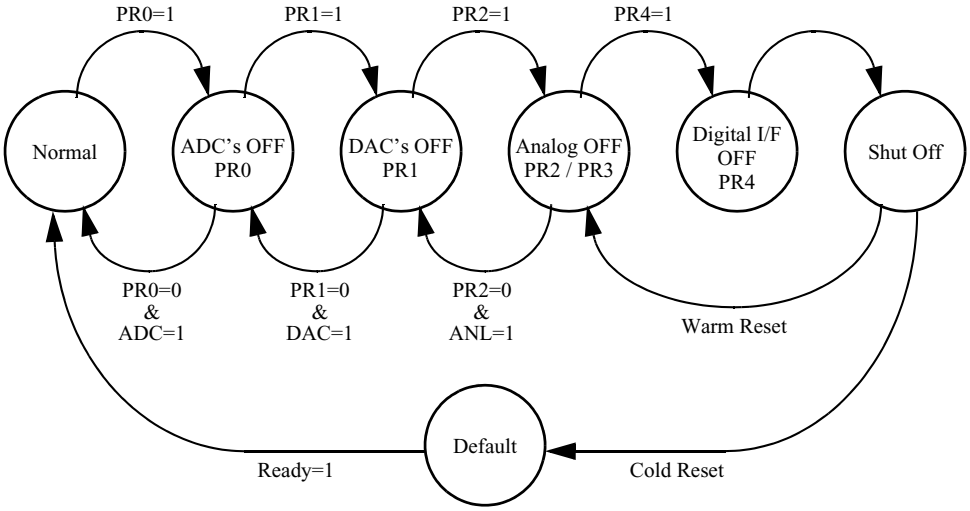
Power Management

The VT1612A may be placed in several power down states using the power down control bits located in index register 26h. **Table 6** lists the power down states accessible through this register.

Table 6. Power Down Mode Bits

Bit	Function
PR0	ADC and Mux Powerdown
PR1	DAC Powerdown
PR2	Mixer Powerdown (VREF on)
PR3	Mixer Powerdown (VREF off)
PR4	AC Link Powerdown (BIT_CLK off)
PR5	Internal Clock Disabled
PR6	Alternate Line Out Powerdown

Note: Registers maintain values in sleep mode (PR4 write) and wake up with a warm reset (register values) or a cold reset (default values). Power Down and Status register (index 26h) read action verifies stability before power down write action occurs.



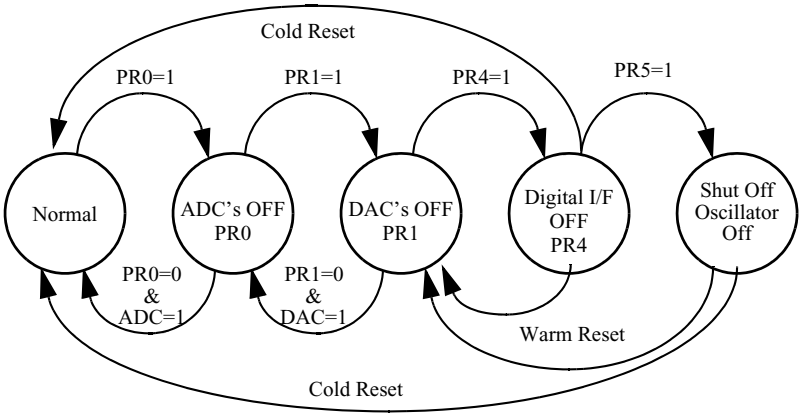
Note: In this example, the Analog Mixer has been disabled, but VREF is still on.

Figure 5. AC'97 Power Down / Power Up Procedure

Complete power down of the AC'97 device is achieved by sequential writes to the Power Down and Status Control Register (Index 26h) as follows:

Normal Operations:	PR[6:0] = 00h
ADC's and Input Mux:	PR0 = 1 (write)
DAC's:	PR1 = 1 (write)
Analog Mixer:	PR2 = 1 (write)
VREF_OUT:	PR3 = 1 (write)
AC-link:	PR4 = 1 (write)
Internal Clocks:	PR5 = 1 (write)
Alt. Line Out:	PR6 = 1 (write)

Power Management (*continued...*)



Note: To wake up the codec, a warm reset can be used; PR4 is reset to zero upon either reset. PR5 can only be cleared by a cold reset.

Figure 6. AC'97 Power Down Procedure with Analog Section Still Active

Test Mode Operation

ATE Test Mode: (PCB in-circuit Testing of the VT1612A)

ATE Test mode is entered when the SDATA_OUT signal is sampled at the rising edge of the RESET# signal. In this mode, the SDATA_IN and BIT_CLK pins are placed in a high impedance (Hi-Z) state as shown on **Table 14** on page 36. This mode of operation doesn't occur under normal operating conditions.

Vendor Test Mode:

Vendor Test mode is entered when the SYNC signal is sampled during the rising edge of the RESET# signal as shown on **Table 15** on page 36. This mode of operation doesn't occur under normal operating conditions.

Absolute Maximum Ratings

Table 7. Limits

(AGND = DGND = 0V)

Symbol	Parameter	Min	Typ	Max	Unit
–	Digital Power Supplies (DVCC)	-0.3		4.0	V
–	Analog Power Supplies (AVCC)	-0.3		6.0	V
–	Input Current per Pin	-10		10	mA
–	Output Current per Pin	-15		15	mA
–	Digital Input Voltage	-0.3		DVCC+0.3	V
–	Analog Input Voltage	-0.3		AVCC+0.3	V
–	Total Power Dissipation		290		W
–	Ambient Temperature	-55		110	°C
–	Storage Temperature	-65		150	°C

Caution: Exceeding any of these limits can cause permanent failure of the device and will void any claims against product quality.

Recommended Operating Conditions

Table 8. Limits

(AGND = DGND = 0V)

Symbol	Parameter	Min	Typ	Max	Unit
–	Digital Power Supplies (DVCC)	3.135	3.3	3.465	V
–	Analog Power Supplies (AVCC), preferred	4.75	5	5.25	V
–	Analog Power Supplies (AVCC), for low power apps	3.135	3.3	3.465	V
–	Operating Ambient Temperature	0		70	°C

Performance Specifications

Table 9. Analog Performance Characteristics (+5V Power)

TA=25°C, AVCC = 5V ± 5%, DVCC = 3.3V ± 5%; AGND = DGND = 0V; 10 KΩ / 50 pF Load; FS = 48 KHz, 0 dB = 1VRMS; BW: 20 Hz ~ 20 KHz, 0 dB Attentuation, IB[1:0]=00 (power up default), as targeted for a 2-layer PCI add-in card.

Symbol	Parameter		Min	Typ	Max	Unit
	Full Scale Input Voltage:	Line Inputs		1.0		VRMS
		Mic Inputs (20dB = 0)		1.0		VRMS
		Mic Inputs (20dB = 1)		0.1		VRMS
	Full Scale Output Voltage:	Line Outputs		1.0		VRMS
		Mono Output		1.0		VRMS
	Analog S/N:	CD to LINE_OUT		95		dB
		Other to LINE_OUT		95		dB
	Analog Frequency Response		20		20,000	Hz
	Digital S/N:	DACs	85	95		dB
		ADC	75	85		dB
	Total Harmonic Distortion:	LINE_IN to LINE_OUT		-94	-74	dB
	(DA) DAC to LINE_OUT			-85	-74	dB
	D/A and A/D Frequency Response:	DACs	20		19,200	Hz
		ADC	20		19,200	Hz
	Transition Band:	DACs	19,200		28,800	Hz
		ADC	19,200		28,800	Hz
	Stop Band:	DACs	28,800		infinity	Hz
		ADC	28,800		infinity	Hz
	Stop Band Rejection:	DACs	75			dB
		ADC	75			dB
	Out-of-Band Rejection			-40		dB
	Group Delay				1	ms
	Power Supply Rejection Ratio (1 KHz)			-40		dB
	Input Channel Crosstalk				-70	dB
	Spurious Tone Reduction			-100		dB
	Attenuation, Gain Step Size			1.5		dB
	Input Impedance		10	45		kΩ
	Input Capacitance			15		pF
	VREFOUT			2.4		V

Note: VIL = 0.8V, VIH = 2.4V
Analog Frequency Response has ±1dB limits
SNR (measured as THD+N) of rms output level with 1 KHz full-scale input to rms output level with all zeros into digital input
Measured "A wtd" over a 20 Hz ~ 20 KHz bandwidth (AES17-1991 Idle Channel Noise or EIAJ CP-307 SNR)
THD: 0 dB gain, 20 KHz BW, Fs = 48 KHz, -3 dB "large" signal
A/D and D/A Frequency Response has ±0.25 dB limits
Stop Band Rejection determines filter requirements
Out-of-Band rejection determines audible noise
Integrated Out-of-band noise generated by DAC during normal PCM audio playback over: BW = 28.8 KHz ~ 100 KHz, with respect to 1 VRMS DAC output

Performance Specifications (*continued...*)

Table 10. Analog Performance Characteristics (+3.3V Power)

TA=25°C, AVCC = DVCC = 3.3V ± 5%; AGND = DGND =0V; 10 KΩ / 50pF Load; FS = 48 KHz, 0 dB = 0.70VRMS;
BW: 20 Hz ~ 20 KHz, 0dB Attentuation, IB[1:0]=10 (set by software), as targeted for a 2-layer PCI add-in card

Symbol	Parameter		Min	Typ	Max	Unit
	Full Scale Input Voltage:	Line Inputs		0.7		VRMS
		Mic Inputs (20dB = 0)		0.7		VRMS
		Mic Inputs (20dB = 1)		0.07		VRMS
	Full Scale Output Voltage:	Line Outputs		0.70		VRMS
		Mono Output		0.07		VRMS
	Analog S/N:	CD to LINE_OUT		92		dB
		Other to LINE_OUT		92		dB
	Analog Frequency Response		20		20,000	Hz
	Digital S/N:	DACs		90		dB
		ADC		85		dB
	Total Harmonic Distortion:	Line Outputs		-70		dB
	D/A and A/D Frequency Response:	DACs	20		19,200	Hz
		ADC	20		19,200	Hz
	Transition Band:	DACs	19,200		28,800	Hz
		ADCs	19,200		28,800	Hz
	Stop Band:	DACs	28,800		infinity	Hz
		ADC	28,800		infinity	Hz
	Stop Band Rejection:	DACs	TBD			dB
		ADC	TBD			dB
	Out-of-Band Rejection			-40		dB
	Group Delay				1	ms
	Power Supply Rejection Ration (1 KHz)			-40		dB
	Input Channel Crosstalk				-70	dB
	Spurious Tone Reduction			-100		dB
	Attenuation, Gain Step Size			1.5		dB
	Input Impedance		10	50		kΩ
	Input Capacitance			15		pF
	VREFOUT			1.5		V

Note: VIL = 0.8V, VIH = 2.4V
Analog Frequency Response has ±1dB limits
SNR (measured as THD+N) of rms output level with 1 KHz full-scale input to rms output level with all zeros into digital input
Measured "A wtd" over a 20 Hz ~ 20 KHz bandwidth (AES17-1991 Idle Channel Noise or EIAJ CP-307 SNR)
THD: 0dB gain, 20 KHz BW, Fs = 48 KHz, -3dB "large" signal
A/D and D/A Frequency Response has ±0.25 dB limits
Stop Band Rejection determines filter requirements
Out-of-Band rejection determines audible noise
Integrated Out-of-band noise generated by DAC during normal PCM audio playback over: BW = 28.8 KHz ~ 100 KHz, with respect to 0.70 VRMS DAC output

Performance Specifications (*continued...*)

Table 11. Miscellaneous Analog Performance Characteristics

(TA=25°C, AVCC = 5.0V ± 5%, DVCC = 3.3V ± 5%; AGND = DGND =0V; 10kΩ / 50pF Load); FS = 48 KHz, 0dB = 1VRMS; BW: 20Hz ~ 20 KHz, 0dB Attentuation)

Symbol	Parameter	Min	Typ	Max	Unit
	Mixer Gain Range Span:				
	LINE_IN, AUX, VIDEO, MIC1, MIC2, PHONE, PC_BEEP		46.5		dB
	LINE_OUT, MONO_OUT		46.5		dB
	Mixer Step Size:				
	All Volume Controls except PC_BEEP		1.5		dB
	PC_BEEP		3.0		dB
	Mixer Mute Level		110		dB
	Mixer Gain: Interchannel Gain Mismatch	-0.5		0.5	dB
	Gain Drift		100		ppm/°C
	ADC and Analog Inputs (Rs=50Ω) Resolution			18	bits
	Gain Error		± 2	± 5	%
	Offset Error		10		mV
	Input Impedance		50		kΩ
	DAC and Analog Outputs: Resolution			18	bits
	Interchannel Isolation		80		dB
	Interchannel Gain Mismatch		0.1	0.2	dB
	Gain Error			± 5	%
	Gain Drift		60		ppm/°C

Electrical Specifications

Table 12. DC Characteristics

(TA=25°C, AVCC = 5.0V ± 5%, DVCC = 3.3V ± 5%; AGND = DGND =0V; 50pF Load)

Symbol	Parameter	Min	Typ	Max	Unit
VIN	Input Voltage Range	-0.3		VCC+0.3	V
VIL	Input Low Voltage			0.3 x VCC	V
VIH	Input High Voltage	0.7 x VCC			V
VOL	Output Low Voltage			0.4	V
VOH	Output High Voltage	2.4			V
–	Input Leakage Current (AC-Link)	-10		10	µA
–	Output Leakage Current (AC-Link and Hi-Z)	-10		10	µA
–	Output Buffer Drive Current		TBD		mA

Table 13. Power Consumption (+5V Power)

(TA=25°C, AVCC = 5.0V ± 5% DVCC = 3.3V ± 5%; AGND = DGND =0V; 50pF Load)

Symbol	Parameter	Min	Typ	Max	Unit
IVCC	*Digital Supply Current*: Power Up (default)		TBD		mA
IVCC	All active (2Ah = 0004h)		TBD		mA
IVCC	S/PDIF on (2Ah = 3804h)		TBD		mA
IVCC	All DACs off (PR1, 26h = 0200h, 2Ah = 3800h)		TBD		mA
IVCC	PR4 (26h =1F00h, 2Ah = 3800h)		TBD		mA
IVCC	Power Down (PR6, RESET# = 0)		TBD		mA
IAVCC	*Analog Supply Current*: Power Up (default)		TBD		mA
IAVCC	All active (2A = 0004h)		TBD		mA
IAVCC	PR0 (26h = 0100h, i.e. ADC off)		TBD		mA
IAVCC	All DACs off (PR1, 26h = 0200h, 2Ah = 3800h)		TBD		mA
IAVCC	PR2 (26h = 0700h)		TBD		mA
IAVCC	Power Down (PR3, 26h = 0F00h, 2Ah = 3800h)		TBD		mA

Table 14. Power Consumption (+3.3V Power)

(TA=25°C, AVCC = DVCC = 3.3V ± 5%; AGND = DGND =0V; 50pF Load)

Symbol	Parameter	Min	Typ	Max	Unit
IVCC	Digital Supply Current: Power Up		TBD		mA
IVCC	Digital Supply Current: Power Down		TBD		mA
IAVCC	Analog Supply Current: Power Up default		TBD		mA
IAVCC	Analog Supply Current: Power Up, IB[1:0]=11		TBD		mA
IAVCC	Analog Supply Current: Power Down, IB[1:0]=xx		TBD		mA

AC Timing Characteristics

(Test Conditions: TA=25°C, AVCC = 5.0V ± 5%, DVCC = 3.3V ± 5%; AGND = DGND =0V; 50pF Load)

Table 15. Cold Reset

Symbol	Parameter	Min	Typ	Max	Unit
TRST_LOW	RESET# Active Low Pulse Width	1			µs
TRST2CLK	RESET# Inactive to BIT_CLK Startup Delay	162.8			ns

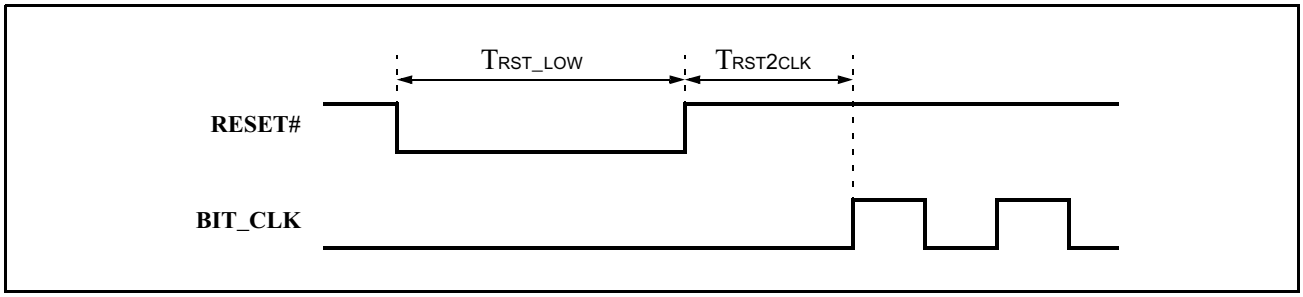


Figure 7. Cold Reset Timing

Table 16. Warm Reset

Symbol	Parameter	Min	Typ	Max	Unit
TSYNC_HIGH	Sync Active High Pulse Width		1.3		µs
TSYNC2CLK	SYNC Inactive to BIT_CLK Startup Delay	162.8			ns

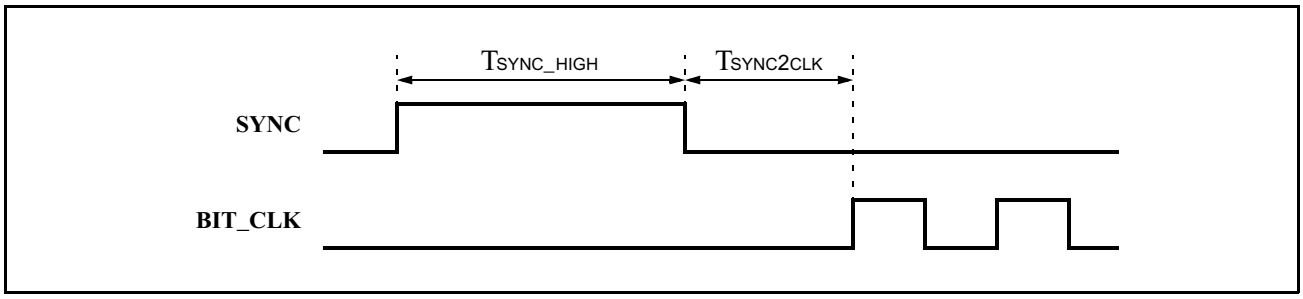


Figure 8. Warm Reset Timing

Table 17. BIT_CLK Timing

Symbol	Parameter	Min	Typ	Max	Unit
	BIT_CLK Frequency		12.288		MHz
TCLK_PERIOD	BIT_CLK Period		81.4		ns
	BIT_CLK Output Jitter			750	ps
TCLK_HIGH	BIT_CLK Pulse Width (high)	32.56	40.7	48.84	ns
TCLK_LOW	BIT_CLK Pulse Width (low)	32.56	40.7	48.84	ns
TCLK_DC	BIT_CLK Duty Cycle	40		60	%

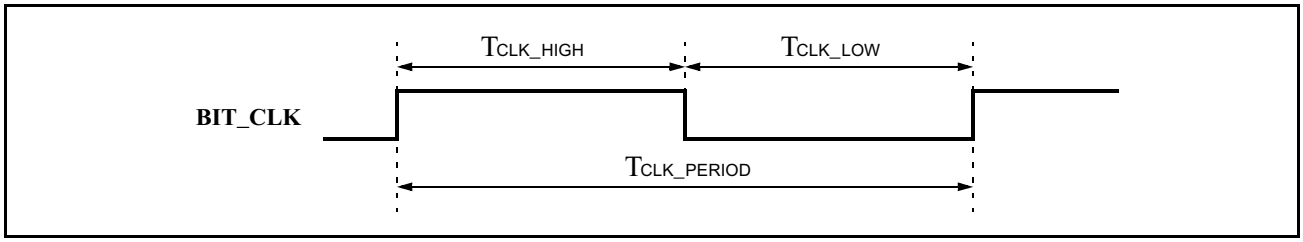


Figure 9. BIT_CLK Timing

Table 18. SYNC Timing

Symbol	Parameter	Min	Typ	Max	Unit
	SYNC Frequency		48		KHz
TSYNC_PERIOD	SYNC Period		20.8		µs
TSYNC_HIGH	SYNC Pulse Width (high)		1.3		µs
TSYNC_LOW	SYNC Pulse Width (low)		19.5		µs

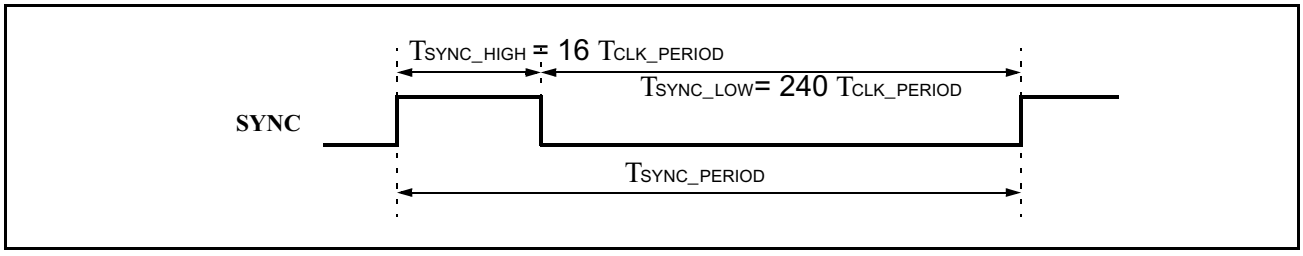


Figure 10. SYNC Timing

Table 19. Setup and Hold Timing

Symbol	Parameter	Min	Typ	Max	Unit
TSETUP1	SDATA_OUT Setup to falling edge of BIT_CLK	15			ns
THOLD1	SDATA_OUT Hold from falling edge of BIT_CLK	5			ns
TSETUP2	SYNC Setup to rising edge of BIT_CLK	15			ns
THOLD2	SYNC Hold to rising edge of BIT_CLK	5			ns

Note: SDATA_IN setup and hold calculations determined by AC'97 controller propagation delay.

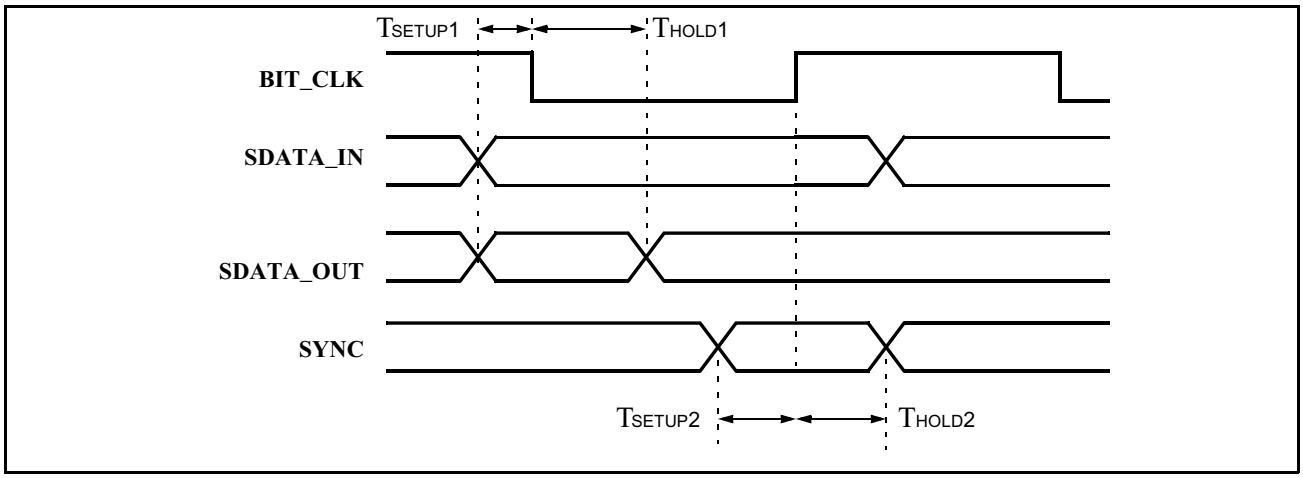


Figure 11. Setup and Hold Timing

Table 20. Rise and Fall Timing

Symbol	Parameter	Min	Typ	Max	Unit
TRISE	BIT_CLK rise time	2		6	ns
TFALL	BIT_CLK fall time	2		6	ns
TRISE	SYNC rise time	2		6	ns
TFALL	SYNC fall time	2		6	ns
TRISE	SDATA_IN rise time	2		6	ns
TFALL	SDATA_OUT fall time	2		6	ns
TRISE	SDATA_OUT rise time	2		6	ns
TFALL	SDATA_OUT fall time	2		6	ns

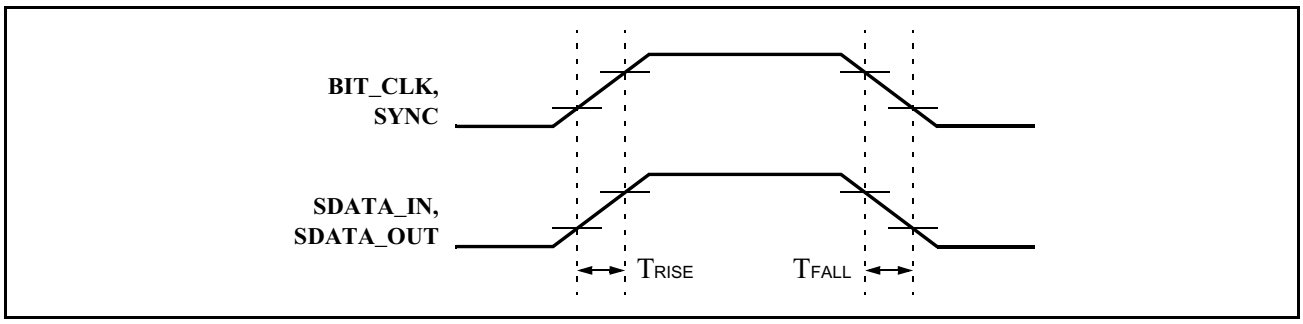


Figure 12. Rise Time and Fall Timing

Table 21. AC Link Low Power Mode

Symbol	Parameter	Min	Typ	Max	Unit
TS2_PDOWN	End of Slot 2 to BIT_CLK / SDATA_IN low			1	µs

Note: BIT_CLK not to scale.

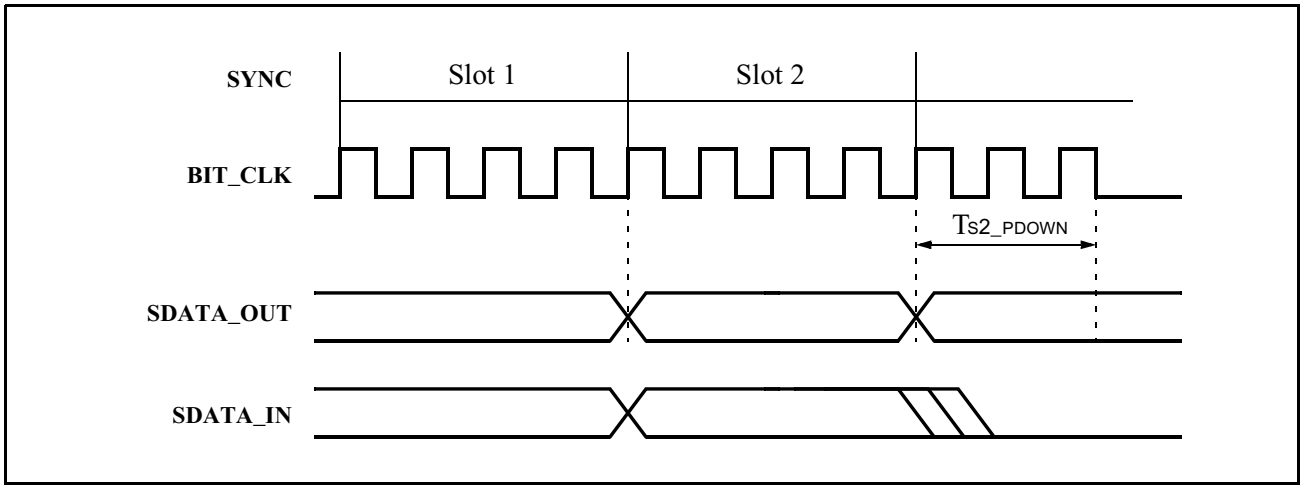


Figure 13. AC Link Power Mode Timing

Table 22. ATE Test Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit
TSETUP2RST	SDATA_OUT setup to RESET# rising edge	15			ns
TOFF	RESET# rising edge to Hi-Z state			25	ns

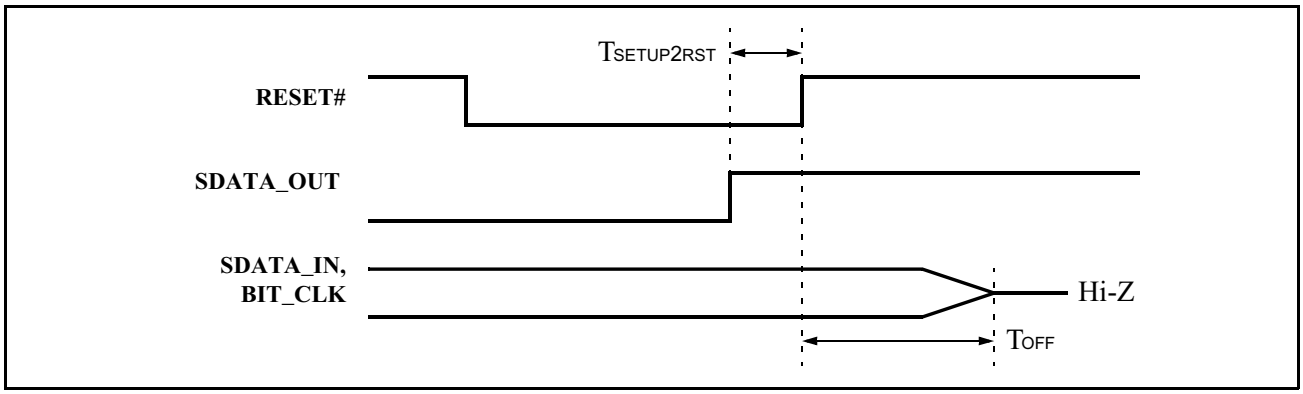


Figure 14. ATE Test Mode Timing

Table 23. Vendor Test Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit
TSETUP2RST	SYNC setup to RESET# rising edge	15			ns
TOFF	RESET# rising edge to Hi-Z state			25	ns

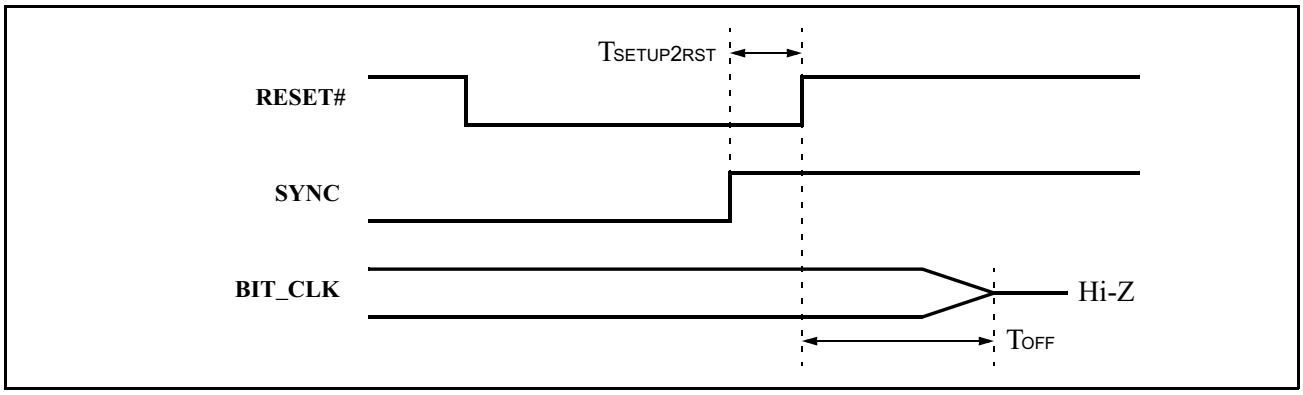
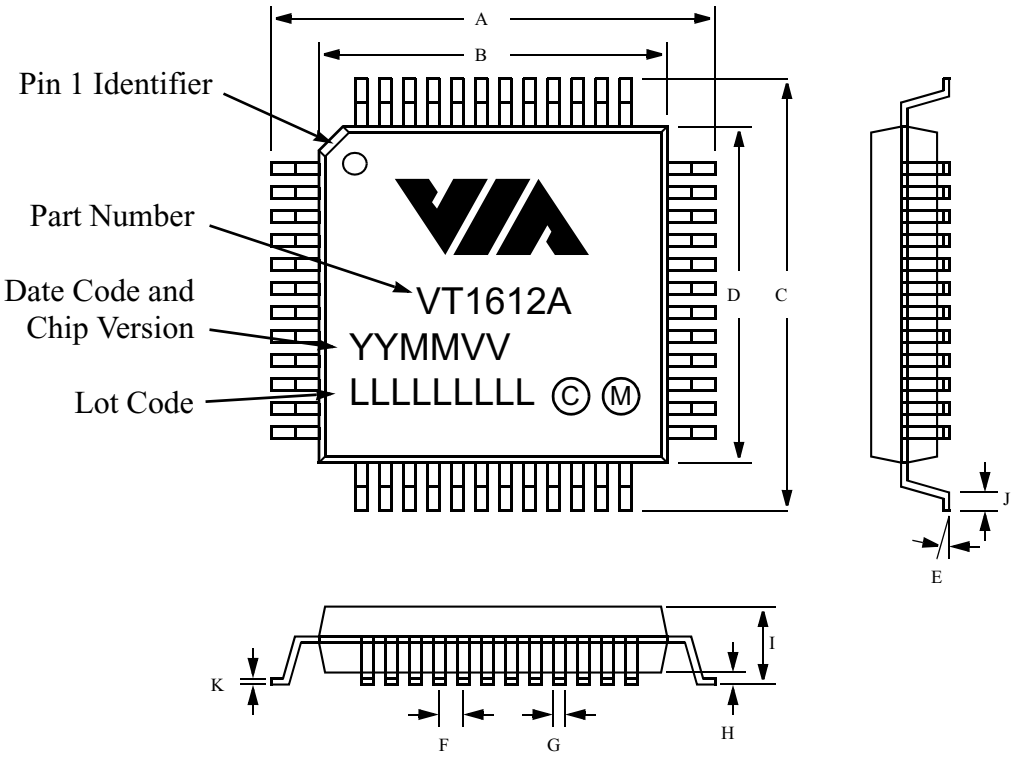


Figure 15. Vendor Test Mode Timing

Package Dimensions



Mechanical Dimensions (millimeters, unless otherwise stated)

Symbol	A	B	C	D	E	F	G	H	I	J	K
48-pin (7x7) LQFP											
minimum	8.6	6.9	8.6	6.9	0°	0.5	0.13	0.05	–	0.3	0.100
maximum	9.4	7.1	9.4	7.1	10°		0.28	0.15	1.7	0.7	0.175