VLSI TECHNOLOGY, INC.

TOPCAT HIGH-PERFORMANCE PC/AT-COMPATIBLE CHIP SET DATA MANUAL

VL82C286-SET
80286/80386SX
CHIP SET

VL82C386-SET
80386DX
CHIP SET

Logic Products Division
October 1990

$5.00

ADVANCED INFORMATION

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PREFACE

This manual provides the reader with a preliminary technical reference on the VLSI Technology, Inc., TOPCAT PC/AT-compatible chip sets. In the body of the text, all devices are treated as individuals so that the electrical characteristics of each can be clearly defined. A "Selector Guide" in the front of this manual defines which devices should be selected to form a chip set that meets the system designer's performance specifications. If you should require performance or functions not included in this manual, please contact your local VLSI Technology Design Center or Sales office. All of the devices in this manual were designed with VLSI's tools, and are available for ASIC designs of custom derivative product.

This manual contains the advance information hardware description of each device. As soon as the device characterization of all of the devices is complete, VLSI plans on publishing a definitive data manual on these devices. Further, VLSI has also scheduled publication of a separate Computer Products Applications Manual containing PC/AT-compatible system schematics and other applications information to demonstrate a typical system implementation. Since computer technology is extremely fast-moving, it is planned that VLSI's Logic Products Division will revise, update, and publish these manuals often. This will allow timely publication of data on new products, as well as improvements on existing ones. The most current information may also be obtained from your local VLSI Technology, Inc., Sales Office, Representative, or the Logic Products Division in Tempe, Arizona.

Readers are encouraged to send their comments, corrections, or suggestions to:

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VLSI Technology, Inc.
8375 South River Parkway
Tempe, AZ 85284

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VLSI TECHNOLOGY, INC.

SECTION 1

INTRODUCTION

Logic Products Division

TOPCAT PC/AT-COMPATIBLE DATA MANUAL

DATA BOOK

This data book presents a preliminary technical description of the VLSI Technology, Inc., Logic Products Division's "TOPCAT" (Two/Three-chip Optimized PC/AT-compatible) chip sets. Two chip sets are presented in this manual: the VL82C286 and VL82C386. The VL82C286 is a two-chip set designed to operate in 80286 or 80386SX microprocessor-based PC/AT-compatible systems. The VL82C386 is a three-chip set designed to operate in 80386DX microprocessor-based PC/AT-compatible systems.

In order to facilitate desktop publishing (DTP) computer generation of this data book, overbars have been replaced by a preceding minus sign on all data sheets.

GENERAL

The primary business objective of VLSI Technology, Inc., (VLSI) is to provide systems designers with total application-specific integrated circuit (ASIC) solutions. To accomplish this, it has created a unique blend of expert design tools, leading-edge process technologies, state-of-the-art fabrication facilities, and a wide range of products, including a variety of "catalog" devices.

The Logic Products Division of VLSI Technology is responsible for the manufacture and marketing of a diverse logic-based product line that encompasses both innovative and proven well established catalog devices. This line includes high-integration computer product devices, microprocessors and coprocessors, peripheral circuits, and devices for related applications.

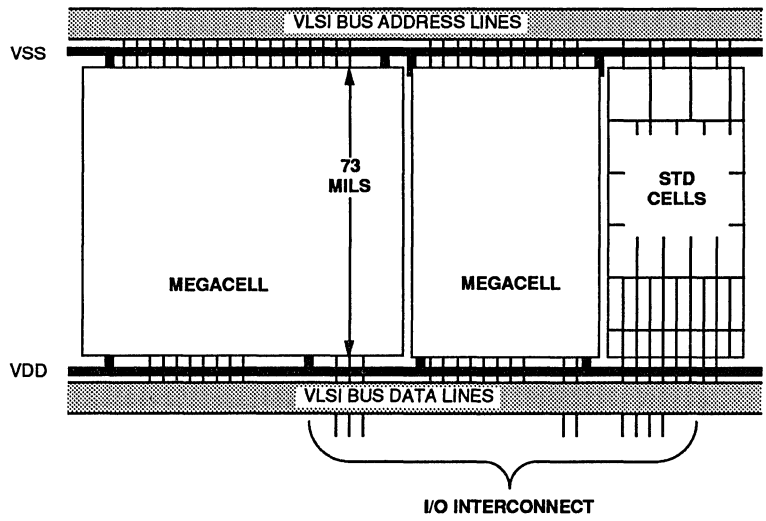
Unlike other suppliers of such devices, however, VLSI is also a recognized leader in ASICs. As such, it not only possesses the design, process, and fabrication capabilities necessary to produce the highest-quality off-the-shelf components, but is also able to treat its logic products as an integral part of a complete solution. One of the primary vehicles for accomplishing this is the megacell. The functions represented by individual devices may be implemented as megacells in VLSI's software libraries and used for semi-custom circuit design. Functions developed as megacells for specific applications can be turned into catalog products.

MEGACELLS

The megacell is a relatively new concept in the world of IC and system design. As such ASIC companies as VLSI offer better tools for IC design, simulation, and testing, it becomes necessary for systems manufacturers to design custom ICs to keep up with their competition. Megacells help decrease design time by providing large building blocks that are equivalents of standard off-the-shelf products. By using megacells and VLSI's design tools, manufacturers can have a custom IC design capability without all of the normal custom development costs.

The VLSI Technology family of megacells represents commonly used peripherals that are good candidates for integration as parts of customer-driven designs, which can be either customer-specific or market-specific. In customer-specific designs, it is possible, for example, to combine these integration elements with other megacells and logic to become single-chip equivalents of computer systems that are already in production. This increased level of integration provides cost and space reduction that can keep the system

FIGURE 1. VLSI TECHNOLOGY MEGACELLS ARE OF A FIXED HEIGHT, WITH VARIABLE WIDTHS.



designs competitive. In a market-specific design, upward-compatible enhancements that meet the needs of many customers can be added and the device offered as a new standard product.

VLSI's megacells are designed to have a fixed height and variable widths, offering the best trade-off between unusable internal space and placement ease. As shown in Figure 1, they can be configured to make a very dense final design with a minimum of wasted silicon real estate.

Of equal importance with the physical layout format of the cells is the structure of the interconnect bus. This bus must be generic enough to allow a wide variety of functions to be connected uniformly and efficiently, and must be fast enough to not itself become a limiting factor as system performance increases.

The internal structure of the bus created by VLSI for use with its megacells contains an m-bit data bus and an n-bit address bus, both of which are expandable in width to accommodate changes in system requirements. The bus operates synchronously at a rate of 3 million transfers a second, which is equivalent to the performance of a 10 MHz 8086 or 12 MHz 68000 microprocessor. The bus definition allows for internal access times of 50 ns and cycle times in the 200 ns range. With standard pad drivers, external loads can be driven while supporting a 3 MHz bus frequency; faster speeds can be obtained by using faster pad drivers. To create a standard product from a megacell, an interface circuit is incorporated that exactly matches the slower timing of the external bus to the internal bus.

MEGACELL-BASED DESIGN RATIONALE

There are many reasons why megacells make sense for new designs, including reduced board space, lower power, increased reliability and reduced design times.

Typical applications that can benefit from the use of megacells are those that contain three or four LSI components and a handful of "glue" components. All of these components can be combined into a single component if the functions can be partitioned into logical groups with a reasonable number of I/O pins. In this type of application, the total pin count might be reduced from 300 pins for a discrete solution to less than 100 pins, and the circuit board area reduced from approximately 20 square inches to 2 square inches.

The power consumption of megacell designs can be very small in comparison with the HMOS designs they replace, since all of the VLSI Technology megacell family is implemented in high speed, low power, 2-micron and 1.5-micron CMOS technology. In addition, because several functions can be put on one piece of silicon, the interconnect capacitance and inductances are minimized, thereby reducing the power to a fraction of what was needed in previous designs.

The reliability of a megacell-based design is typically better than the collection of discrete components it replaces because there are fewer pins, fewer bonding wires and lower total power consumption. In most systems, the largest contributor to reliability problems is IC pin connections, with such other factors as die temperature and die size being secondary. The more functional blocks that can be combined on a single piece of silicon, the fewer the number of interconnections that have to be bonded to package pins, resulting in higher overall reliability of the component and system using it.

Since megacells can be used as high level building blocks, overall design times can be reduced significantly by taking existing designs using standard products and integrating additional support logic directly onto the chip. An example of this technique would be the integration of a VL68C45 CRT controller with a memory interface and video shift registers to form a single-chip video adapter. An additional option might be to include character ROMs or RAM arrays, although the addition of these commodity components is not always cost effective.

CURRENT FAMILY OF MEGACELLS

Megacells are designed by very carefully studying the data sheets and systems implementations of the original part vendors, but an important part of validating a megacell design is to subject it to many different hardware and software environments. Only after a part has been tested in several applications can a vendor feel confident that the megacell exactly emulates the original function, including all of the undocumented "features". The VLSI Technology philosophy is to offer members of the megacell family as standard products as well as cells so that this validation can take place very quickly after the introduction of the standard product. Since customer-specific design times typically take from two to four months, megacell designs can be started before the standard product validation has been done. This lead time allows customers to get a head start introducing designs.

DESIGNING A CIRCUIT USING MEGACELLS

The design process is started by using a megacell schematic "icon" as part of the schematic entry of the user's design. Provided with the megacell icon is a data sheet detailing the internal timing requirements of the megacell. The designer works from this data sheet as if using an off-the-shelf standard product, except that the logic and timing of the bus are somewhat easier to use.

ADDITIONAL LOGIC FOR TEST SIMPLIFICATION

In all cases, some additional logic will be necessary to facilitate testing the megacells. This additional logic consists of multiplexers on pins to allow all of the connections of the megacell to be accessed from the periphery of the circuit. This dictates that all designs be contained in packages having at least as many pins as the most pin-intensive megacell used internally. To enable the test mode, an illegal condition on the interface is often used, such as Read Strobe and Write Strobe being asserted together while the chip is selected. This would normally never occur in an application, so it is a safe combination to use. When enabled, the I/O pads of a specific megacell are connected to the I/O pins of the component, and the standard product test program run to verify the functionality of the core.

TEST PROGRAM DEVELOPMENT

Test vectors are provided for all megacells with high fault coverage. These test programs can be integrated

with the rest of the chip's test program using VLSI vector. VLSI provides these "canned" test programs with each megacell so that it will not be necessary to spend time trying to develop a test for megacells used in the design. These test programs ensure that the megacells have been fabricated correctly and are functioning within their specifications. They are developed with a focus on very high fault coverage.

In fact, there is no need to simulate these test programs, except for a final verification that the test isolation circuitry has been properly connected. Instead designers can devote additional design verification time to the non-megacell portions of the circuit and the interfaces between the megacell and the rest of the circuit.

COMPLETING THE DESIGN

When simulation is complete and the design works satisfactorily, the layout process can begin. In most cases, designers are interested in minimizing design time and associated costs, so they pick standard cells for the additional blocks of logic that will surround the megacell cores. Cells are individually compiled, placed and routed to create blocks of logic until the entire non-megacell portion of the design is complete. For the best layout efficiency, the additional logic is either put into a block having the same height as a megacell, or it is put around the megacells to fill in the voids. When each portion of the design is completed, these blocks can be placed and interconnected using a tool called Chip Compiler, which is an automated arbitrary block place and route system. This editor assists in interconnecting blocks of cells and optimizing both the placement and interconnection of cells. The overall goal of placing blocks to form the chip is to get the ratio of the X and Y dimensions (the aspect ratio) as close to 1:1 as possible. The resulting square die gives the packaging engineer the most flexibility in package selection.

When the entire layout process is complete, a netlist of interconnections is extracted from the physical data base to allow comparison of what was intended to be with what actually was implemented. Once the extraction is complete and the netlist comparison between schematic and layout is successful, the device can be re-simulated in software with more accuracy, since values of expected capacitance are extracted along with the connectivity information. Finally, the layout is checked for design rule violations using the design rule checker (DRC) program.

When all of this has been successfully completed, the data base is sent to a design center, where the actual physical layout of the megacells is included in the data base. When everything checks out properly, a mask set is created and silicon is started. From this point, the fabrication time typically takes eight weeks for the first pass prototypes.

SUMMARY

Megacells offer a way to quickly design chips that replace today's board level function, while at the same time offering competitive costs, increased reliability, increased performance and reduced board space. The design process requires a wide range of design tools, including standard cells, cell compilers, simulators, routers, test program generators, and libraries of designs. VLSI Technology, Inc., specializes in offering these kinds of tools in addition to complete wafer services to provide a total solution to systems designers.

VLSI TECHNOLOGY, INC.

SECTION 2

ORDERING AND PACKAGING INFORMATION

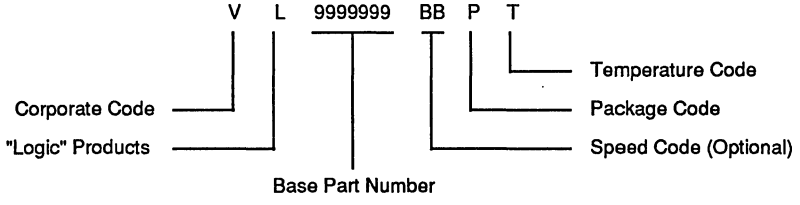
Logic Products Division

ORDERING AND PACKAGING INFORMATION

GENERAL

VLSI Technology, Inc., Logic Products devices are available in a variety of plastic packages - including flatpacks, chip carriers, and pin grid arrays - and in different temperature ranges. Specific information on the packages and temperature ranges for particular devices is coded into the part number portion of the order information included in each data sheet.

The information is organized as follows:



Package Codes:
- C - Sidebrazed Ceramic
- F - Plastic Flatpack
- G - Pin Grid Array
- L - Leadless Ceramic Chip Carrier
- P - Plastic Dual In-Line
- Q - Plastic Leaded Chip Carrier

Temperature Codes:

A - Automotive	(–40°C to +85°C)
C - Commercial	(0°C to +70°C)
I - Industrial	(refer to spec.)
M - Military	(–55°C to +125°C)

For the TOPCAT:

VL82C286-SET 2 Chip Set Consisting of:

1 - VL82C320-FC	System Controller/Data Buffer	160 PQFP
1 - VL82C331-FC	ISA Bus Controller	160 PQFP

VL82C386-SET 3 Chip Set Consisting of:

1 - VL82C330-FC	System Controller	128 PQFP
1 - VL82C331-FC	ISA Bus Controller	160 PQFP
1 - VL82C332-FC	Data Buffer	128 PQFP

ORDERING AND PACKAGING INFORMATION

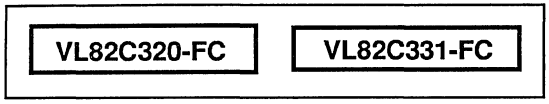
VLSI TECHNOLOGY, INC.

SECTION 3

SELECTOR GUIDE

Logic Products Division

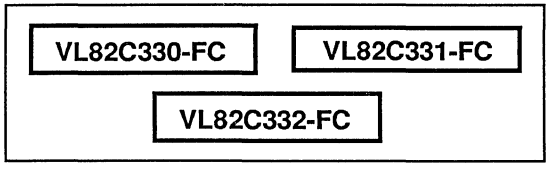
VLSI'S 286/386SX CHIP SET
VL82C286-SET



FEATURES

- 100% 286™ Based MPUPC/AT-Compatible
- Optimized Two Chip Design and Packaging Solution for 286 or 386™SX Based Systems
- Up to 25 MHz System Clock Speeds
- "Sleep" Modes Support Low-Power and Laptop Designs
- Full LIM EMS 4.0® Specification over Entire 32 Mbyte Memory Map
- Built-in Three-state Control for Board Level Testing
- Programmable DRAM and Slot Interface Drive Optimizes System for Actual Load Conditions

VLSI'S 386™DX CHIP SET
VL82C386-SET



FEATURES

- 100% 386DX Based MPU PC/AT-Compatible
- Optimized Three Chip Design and Packaging Solution for 386DX Based Systems
- Up to 33 MHz System Clock Speeds
- "Sleep" Modes Support Low-power and Laptop Designs
- Full LIM EMS 4.0 Specification over Entire 32 Mbyte Memory Map
- Built-in Three-state Control for Board Level Testing
- Programmable DRAM and Slot Interface Drive Optimizes System for Actual Load Conditions

286, 386SX, 386DX are trademarks of Intel Corporation.

LIM EMS 4.0 is a registered trademark of Lotus Development Corporation, Intel Corporation and Microsoft Corporation.

VL82C286

TOPCAT 286™/386™SX CHIP SET

FEATURES

- Two chip PC/AT-compatible chip set capable of use in 286- or 386SX-based systems up to 25 MHz
- Both chips are 160 quad flatpacks, 1.0- and 1.5-micron CMOS
- Memory control of one to four banks of 16 bit DRAM using 256K, 1M, or 4M components allowing 32M bytes on system board
- Page mode DRAM operation on any number of banks
- Two/four-way interleaving or direct access on system board memory
- Programmable option for block or word interleave
- Programmable DRAM timing parameters
- Remap option allows logical reordering of system board DRAM banks
- System board refresh optionally decoupled from slot bus refresh
- Staggered refresh minimizes power supply load variations
- Built–in "sleep" mode features, including use of slow refresh DRAMS in power critical operations
- EMS hardware supports full LIM EMS 4.0® spec over entire 32M byte memory map with backfill to 256K - includes two sets of 36 mapping registers each
- Shadow RAM support in 16K increments over entire 640K to 1M range
- Support for 287™ or 387™SX numerical coprocessors
- Software coprocessor reset can be disabled
- Internal switching and programmable CLK2 support for slow and "turbo" modes
- Programmable drive on DRAM and slot bus interface signals allows direct drive tailored to system size
- Asynchronous or synchronous slot bus operation with programmable bus clock divider
- Integrated peripheral functions:

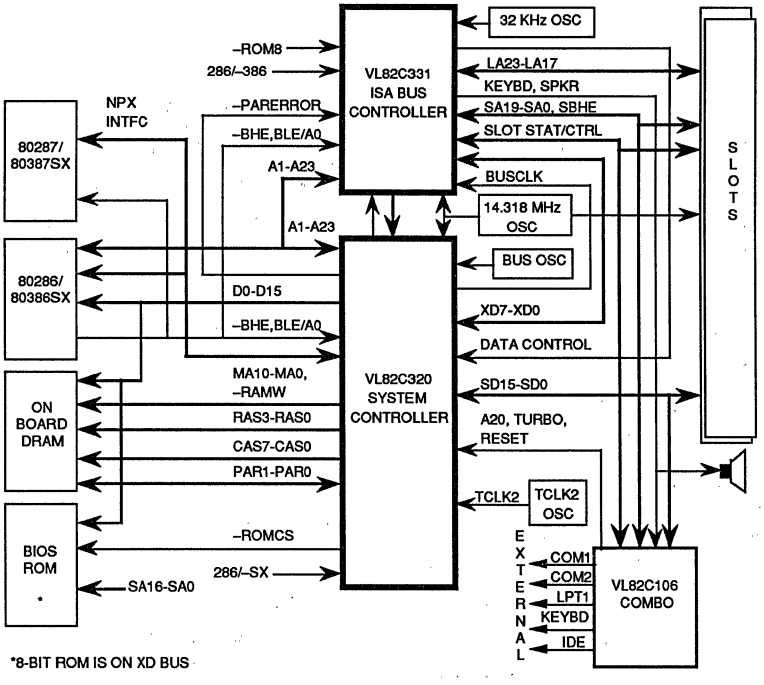
  Two 82C37A DMA controllers

  Two 82C59A interrupt controllers

  One 82C54 timer

  One 82C018 real time clock
- Supports 8- or 16-bit wide BIOS ROMs
- I/O decode programmable for 10- or 16-bit addresses
- Separate parity generators/checkers for high speed operation
- Designed for systems with up to 12 MHz backplane operation
- Three-state control pins added for board level testability
- Compatible with Lotus® 1-2-3® version 3.0 in 1M systems

BLOCK DIAGRAM



*8-BIT ROM IS ON XD BUS

ORDER INFORMATION

VL82C286/386SX Chip Set

Part Number	Package
1 - VL82C320-FC	Plastic Flatpack
1 - VL82C331-FC	Plastic Flatpack

Note: Operating temperature range is 0°C to +70°C.

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VLSI TECHNOLOGY, INC.

ADVANCE INFORMATION

VL82C386

TOPCAT 386™ DX CHIP SET

FEATURES

- Three chip PC/AT-compatible chip set capable of use in 386DX-based systems up to 33 MHz - VL82C330 System Controller, VL82C331 ISA Bus Controller, VL82C332 Data Buffer
- Two 128-pin and one 160-pin (VL82C331) quad flatpacks, 1.0- and 1.5-micron CMOS
- Memory control of one to four banks of 32-bit DRAM using 256K, 1M, or 4M components allowing 64 Mbytes on system board
- Page mode DRAM operation on any number of banks
- Two/four-way interleaving or direct access on system board memory
- Programmable option for block or word interleave
- Programmable DRAM timing parameters
- Remap option allows logical reordering of system board DRAM banks
- System board refresh optionally decoupled from slot bus refresh
- Staggered refresh minimizes power supply load variations
- Built-in "sleep" mode features, including use of slow refresh DRAMS in power critical operations
- Hardware supports full LIM EMS 4.0® spec over entire 64-Mbyte memory map
- DMA expanded to allow transfers over 64-Mbyte range
- Shadow RAM support in 16K increments over entire 640K to 1M range
- Support for 387™ DX and Weitek 3167 numerical coprocessors
- Coprocessor software reset can be disabled
- Internal switching and programmable CLK2 support for PC/AT-compatible and "turbo" modes
- Programmable drive reduces the need for external buffering on DRAM and slot bus interface signals
- ISA Bus Control of 386DX-based PC/AT-compatibles. Capable of asynchronous or synchronous bus operation to 16 MHz
- Compatible with Lotus® 1-2-3® version 3.0 in 1M systems
- Integrated Peripheral Functions:

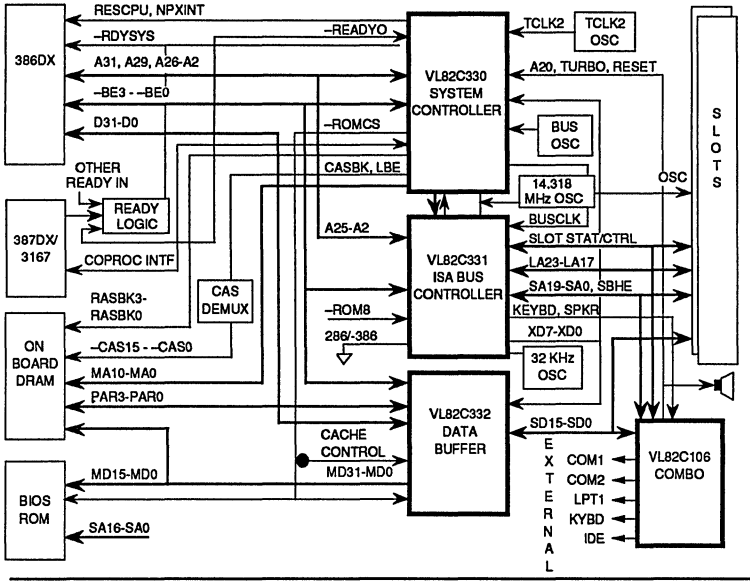
  Two 82C37A DMA Controllers with extended 74LS612 Page Register

  Two 82C59A Interrupt Controllers

  One 82C54 Timer

  One 82C018 Real Time Clock
- Additional 64 bytes of battery backed RAM in RTC provides for non-volatile storage of VL82C386 chip set configuration data and user specific information
- Supports 8- or 16-bit wide BIOS ROMs
- Cache support for posted writes
- System Memory on MD or D bus in non-cached systems
- Separate parity generation/checkers for high speed operation
- Internal I/O programmable for 10- or 16-bit decode
- Three-state control pins added for board level testability

BLOCK DIAGRAM



ORDER INFORMATION

VL82C386DX Chip Set

Part Number	Package
1 - VL82C330-FC	Plastic Flatpack
1 - VL82C331-FC	Plastic Flatpack
1 - VL82C332-FC	Plastic Flatpack

Note: Operating temperature range is 0°C to +70°C.

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VLSI TECHNOLOGY, INC.

SECTION 4

TOPCAT DEVICE DATA SHEETS

Logic Products Division

SYSTEM CONTROLLER/DATA BUFFER

DESCRIPTION

The VL82C320 contains the system control and data buffering functions in a 160-lead quad flat pack.

The VL82C320's functions are highly programmable via a set of internal configuration registers. Defaults on reset for the configuration registers allow the system to boot at the CPU's rated speed. However, operational capabilities may be temporarily reduced until the configuration registers are set to mirror the true system configuration. This normally is a function of BIOS setup.

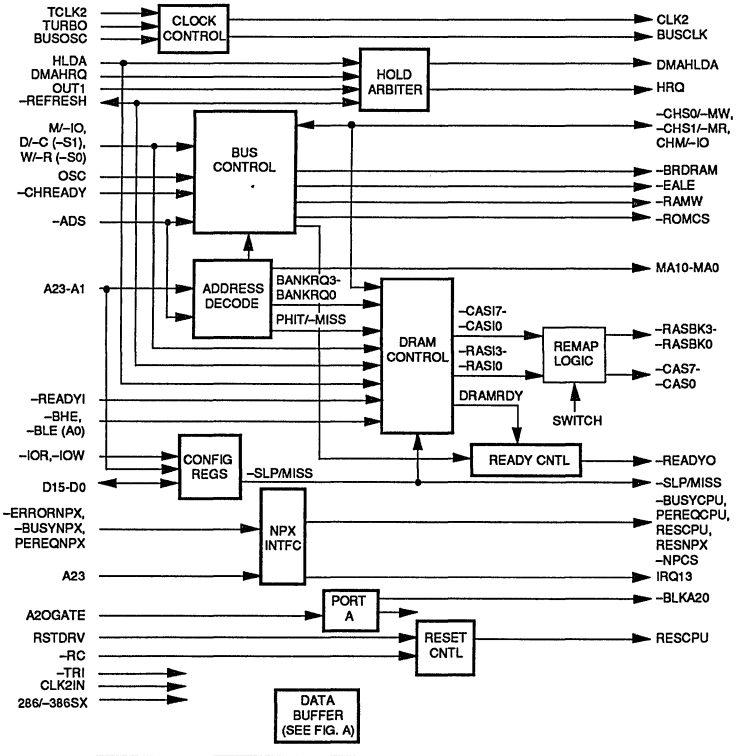
The VL82C320 is designed to perform in systems running up to 25 MHz. Built-in page mode operation, two- or four-way interleaving, and fully programmable memory timing allow the PC designer to maximize system performance using commodity DRAMs.

Programmable memory timing allows the system to be setup to match the requirements of the chosen DRAMs; standard or custom.

The system controller handles system board refresh directly and also controls the timing of slot bus refresh which is actually performed by the VL82C331 ISA Bus Controller. Refresh may be performed in coupled or decoupled mode. The former method is the standard PC/AT®-compatible mode where on- and off-board refreshes are performed synchronously. In decoupled mode, the timing of on- and off-board refreshes is independent. Both may be programmed for independent, slower than normal rates. This allows use of low power, slow refresh DRAMs. The VL82C320 controls all timing in both modes. In all cases, refreshes are staggered to minimize power supply loading and attendant noise on the VDD and ground pins. In sleep mode, –CAS before –RAS refresh may be switched for maximum power savings.

The physical banks of DRAM can be logically reordered through one of the indexed configuration registers. This DRAM remap option is useful in order to map out bad DRAM banks allowing continued use of a system until repairs are convenient. It also allows DRAM bank combinations not in the supported memory maps to be logically moved into a supported configuration without physically moving memory components. This unique, programmable function performs this task by switching the internal –RASBK and CAS signals between the external –RASBK and CAS pins. This allows internal row and

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C320-FC	Plastic Flat Pack

Note: Operating temperature range is 0°C to +70°C.

PC/AT is a registered trademark of IBM Corporation.

column address strobes generated for DRAM bank 0, for example, to be routed to any one of the four on-board DRAM banks.

The Intel 287™ numeric coprocessor is supported when the VL82C320 is strapped for 286™ mode. When strapped for 386™SX mode, the 387™SX is supported. Support is for both 8-bit wide and 16-bit wide system BIOS ROM.

EEMS support is provided in hardware for the complete LIM EMS 4.0® standard. Seventy-two mapping registers provide a standard and an alternate set of 36 registers each. The system allows backfill down to 256K for EEMS support and provides 24 mapping registers covering this space. Twelve of the 36 are page registers which cover the EMS space from C0000h to EFFFFh. These twelve registers can alternatively be mapped in the A0000-BFFFFh and D0000h-DFFFFh range by changing a configuration bit in the VL82C320. All registers are capable of translating over the complete 32 Mbyte range of on-board DRAM. Users preferring an alternate plug-in EMS solution, can disable the on-board EMS system as well as system board DRAM, as required, down to 256K.

Shadowing features are supported on all 16K boundaries between 640K and 1M. Simultaneous EMS use, shadowed ROM, and direct system board access is possible in non-overlapping fashion throughout this memory space. Control over four access options is provided.

1. Access ROM or slot bus for reads and writes.
2. Access system board DRAM for reads and writes.
3. Access system board DRAM for reads and slot bus for writes.
4. Shadow setup mode. Read ROM or slot bus, write system board DRAM.

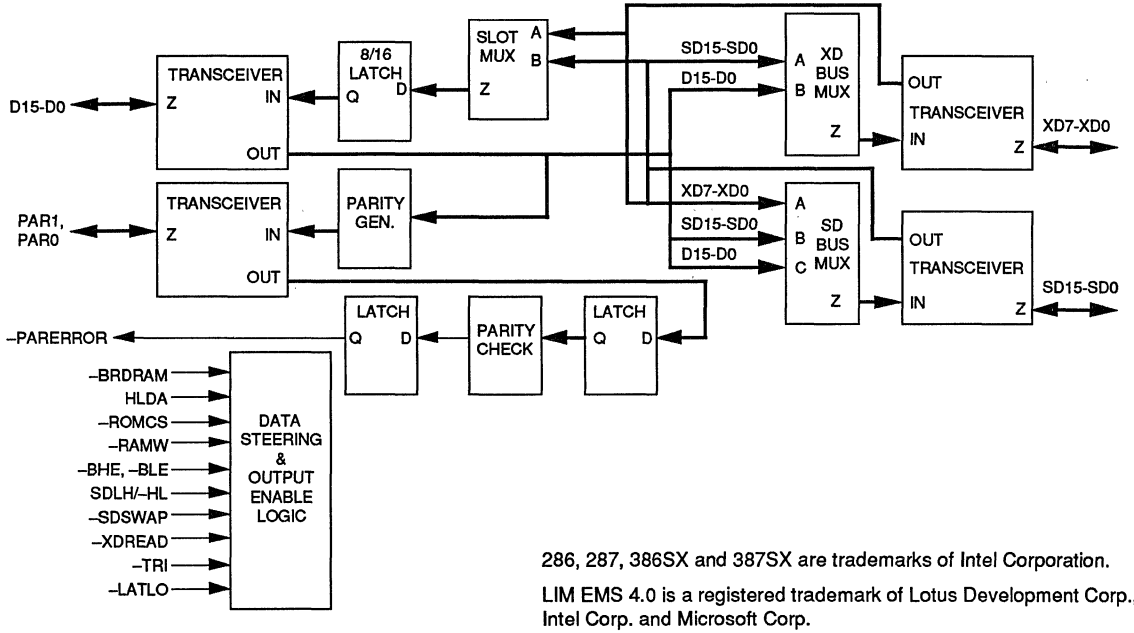
These controls are overridden by EMS in segments for which it is enabled.

The VL82C320 is used to program the desired operational mode of the AT bus. Based on this programming, it provides the bus clock and signalling interface to the Bus Controller. The bus clock may be derived from the TCLK2 or bus OSC inputs. A programmable divider conditions the selected BUSCLK source providing divide by 1, 2, 3 or 4.

The VL82C320 also performs all of the data buffering functions required for a 286- or 386SX-based PC/AT-compatible system. Under the control of the CPU, the data buffer chip routes data to and from the CPU's D bus, XD bus, and slots (SD bus). The parity is checked for D bus DRAM read operations and generated for D bus DRAM write operations. The VL82C320 provides the data conversion necessary for 16-bit accesses to 8-bit devices on the XD or SD buses. The data is latched for synchronization with the CPU.

Under the control of DMA or a bus master, the VL82C320 allows 8- or 16-bit data to be routed to and from the XD bus. The chip also is capable of performing high to low and low to high byte swaps on the SD bus. The chip also provides the feature of a single input, –TRI, to disable all of its outputs for board level testability.

DATA BUFFER FUNCTIONS BLOCK DIAGRAM



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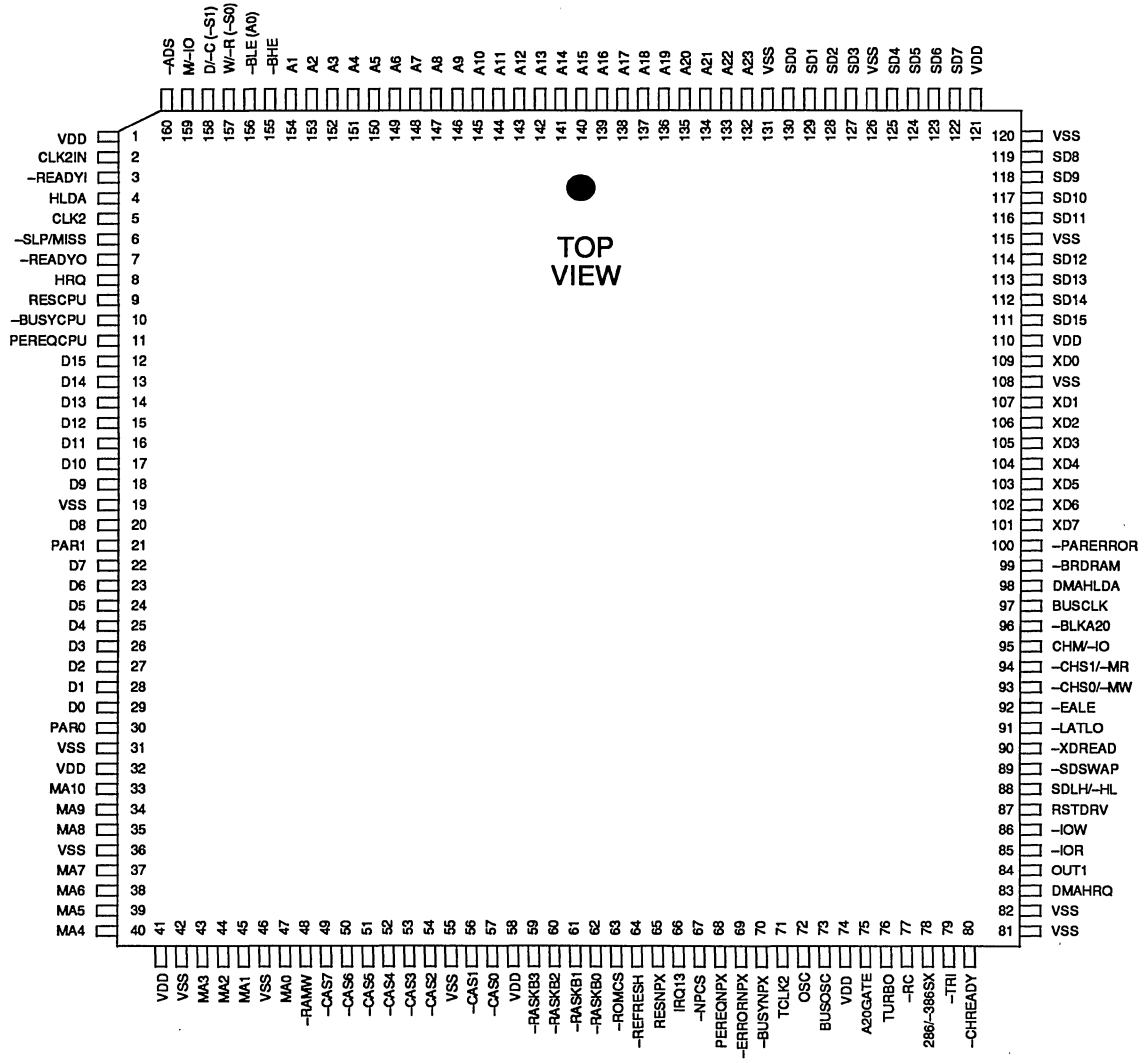
PIN DIAGRAM

VL82C320



Note: Parenthesis indicate 286 pin functions.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE SIGNALS			
A23-A1	132-154	I-TTL	Address bits 23 through 1 - When the CPU is bus master and HLDA is active, these signals are driven by the Bus Controller.
–BHE	155	I-TTL	Byte High Enable, active low - This signal is driven by the CPU or the Bus Controller. It is used to select the upper byte of a 16-bit wide memory location.
–BLE (A0)	156	I-TTL	Byte Low Enable, active low, or A0 - In 386SX mode this signal is –BLE, in 286 mode it is A0 and is driven by the CPU or the Bus Controller. It is used to select the lower byte of a 16-bit wide memory location.
W/–R (–S0)	157	I-TPU	Write or active low Read enable, or S0 - This is W/–R in 386SX mode or –S0 in 286 mode. This signal is decoded with the remaining control signals to indicate the type of bus cycle requested.
D/–C (–S1)	158	I-TPU	Data or active low Code enable, or S1 - D/–C is driven by the CPU in 386SX mode or –S1 in 286 mode. This signal is decoded with the remaining control signals to indicate the type of bus cycle requested.
M/–IO	159	I-TPU	Memory or active low I/O enable - M/–IO is decoded with the remaining control signals to indicate the type of bus cycle requested.
–ADS	160	I-TPU	Address Strobe, active low - This signal is driven by the 386SX as an indicator that the address and control signals are valid. It is used internally to indicate that the address and command are valid and determine the beginning of a bus cycle. This pin is a no connect in 286 mode.
CLK2IN	2	I-CMOS	This is the main clock input to the VL82C320 and it should be connected to the CLK2 signal that is output by the VL82C320. This signal is used internally to clock the VL82C320 logic.
TCLK2	71	I-CMOS	This input is connected to a crystal oscillator whose frequency is equal to two times the system frequency. The CMOS level is used to generate CLK2 output and optionally, bus clock.
CLK2	5	O	This output signal is CMOS level and generated from TCLK2 signal. It is output to the CPU and other on-board logic for synchronization.
–SLP/MISS	6	IT-OD	As a "power on reset" default, this signal is an output that is equal to –SLEEP[7] • –SLEEP[1]. When configuration register CTRL[0] = 1, this pin becomes a MISS input for use with a future VLSI product.
–READYO	7	O	Ready Out, active low - This signal is an indication that the current cycle is complete. It is generated from the internal DRAM controller or the synchronized version of –CHREADY for slot bus accesses. The culmination of these ORed READY signals is sent to the CPU and is also connected to the VL82C320's –READYI input. This signal may be combined externally with other READY sources.
–READYI	3	I-TTL	Ready Input, active low - This signal indicates the current bus cycle is complete.
HLDA	4	I-TTL	Hold Acknowledge, active high - This signal is issued in response to the HRQ driven by the VL82C320. When HLDA is active, the memory control is generated from –CHS1/–MR and –CHS0/–MW.
HRQ	8	O	Hold Request, active high - This signal indicates that a bus master, such as a DMA or AT channel master, is requesting control of the bus. HRQ is a result of the DMAHRQ input or a coupled refresh cycle. It is synchronized to CLK2 and internal clock.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
RESCPU	9	O	Reset CPU, active high - This signal is issued in response to the control bit for software reset located in the Port A, read from IO port EFh, RC and RSTDRV inputs and in response to VL82C320's detection of a shutdown command. In all cases it is synchronized to CLK2 and internal clock.
–BUSYCPU	10	O	Busy CPU, active low - The state of –BUSYNPX is always passed through to –BUSYCPU indicating that the NPX is processing a command. On occurrence of an –ERRORNPX signal, it is latched and held active until occurrence of a write to ports F0h, F1h, or RSTDRV.
PEREQCPU	11	O	Processor Extension Request CPU, active high - An output signal generated in response to a PEREQNPX which is issued by the coprocessor to the VL82C320. PEREQCPU is asserted on occurrence of –ERRORNPX after –BUSYNPX has gone inactive. A write to F0h returns control of the PEREQCPU signal to directly follow the PEREQNPX input.
ON-BOARD MEMORY SYSTEM INTERFACE SIGNALS			
–RAMW	48	O-TTL	RAM Write, active low - This signal is active during memory write cycles and high at all other times.
MA10-MA0	33-35, 37-40, 43-45, 47	O-TTL	Memory Addresses 10 through 0 - These address bits are the row and and column addresses sent to on-board memory. They are buffered and multiplexed versions of the CPU bus addresses.
–RASBK3- –RASBK0	59-62	O-TTL	Row Address Strobe, active low - These signals are sent to their respective RAM banks to strobe in the row address during on-board memory bus cycles. The active period for this signal is fully programmable.
–CAS7- –CAS0	49-54, 56, 57	O	Column Address, Strobe, active low - These signals are sent to their respective RAM banks to strobe in the column address during on-board memory bus cycles. There is a –CAS signal for upper and lower bytes of each of the four 16-bit DRAM memory banks. The active period for this signal is completely programmable. For clarity, alternate names may also be used for these signals as shown in the following table where the digit in the "Alternate Name" indicates the DRAM bank the signal drives, L indicates it drives the low byte, and H indicates it drives the high byte.
–REFRESH	64	IC-OD	Refresh signal, active low - This output is used by the VL82C320 to initiate an off-board DRAM refresh operation in coupled refresh mode. In decoupled mode, the Bus Controller drives refresh active to indicate to the VL82C320 that it has decoded a refresh request command and is initiating an off-board refresh cycle.
–ROMCS	63	O	ROM Chip Select - This is the on-board system BIOS ROM chip select.

Standard Name	Alternate Name
–CAS0	–CAS0L
–CAS1	–CAS0H
–CAS2	–CAS1L
–CAS3	–CAS1H
–CAS4	–CAS2L
–CAS5	–CAS2H
–CAS6	–CAS3L
–CAS7	–CAS3H

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
COPROCESSOR SIGNALS			
PEREQNPX	68	I-TPD	Coprocessor Extension Request NPX, active high - This input signal is driven by the coprocessor and indicates that it needs transfer of data operands to or from memory. For PC/AT-compatibility, this signal is also gated with the internal ERROR/BUSY control logic before being output to the CPU as PEREQCPU during NPX interrupts.
–ERRORNPX	69	I-TPU	Error NPX, active low - An input signal from the coprocessor indicating that an error has occurred in the previous instruction. This signal is internally gated and latched with –BUSYNPX to produce IRQ13.
–BUSYNPX	70	I-TPU	Busy NPX, active low - An input signal that is driven by the coprocessor to indicate that it is currently executing a previous instruction and is not ready to accept another. This signal is decoded internally to produce IRQ13 and to control PEREQCPU.
RESNPX	65	O	Reset NPX - This output is connected to the coprocessor reset input. It is triggered through an internally generated system reset or via a write to port F1h. In the case of a system reset, the RESCPU signal is also activated. Write to port F1h only resets the coprocessor. A software FINIT signal must occur after an F1h generated reset in a 386SX system, otherwise, the 387SX is not initialized to the same state that a 287 is placed in by a hardware reset alone. Optionally, the F1 reset may be disabled by setting bit 6 of the MISCSET register to 1.
IRQ13	66	O	Interrupt Request, active high - This output is driven to the Bus Controller to indicate that an error has occurred within the coprocessor. This signal is a decode of the –BUSYNPX and –ERRORNPX inputs.
–NPCS	67	O	Coprocessor Chip Select - Provides decoding of the 287 coprocessor's I/O space. This is the entire F8h to FFh region when Special Features are disabled. When Special Features are enabled, only I/O accesses to F8h, FAh, FCh, and FEh cause –NPCS to be active. This signal is a no connect pin for 387SX operation, and reserved for future use in 386SX systems.
BUS CONTROL SIGNALS			
–CHREADY	80	I-CMOS	Channel Ready, active low - An input issued by the Bus Controller as an indication that the current channel bus cycle is complete. This signal is synchronized internally then combined with READY signals from the coprocessor and DRAM controller to form the final version of –READYO which is sent to the CPU.
–CHS0/–MW	93	I-CMOS	Channel Select 0 or Memory Write, active low - This signal is a decode of the CPU's bus control signals and is sent to the Bus Controller. When combined with –CHS1 and CHM/–IO and decoded, the bus cycle type is defined for the Bus Controller. Activation of HLDA reverses this signal to become an input from the Bus Controller. It is then a –MEMW signal for the DMA or bus master to access system memory.
–CHS1/–MR	94	I-CMOS	Channel Select 1 or Memory Read, active low - This signal is a decode of the CPU's bus control signals and is sent to the Bus Controller. When combined with –CHS0 and CHM/–IO and decoded, the bus cycle type is defined for the Bus Controller. Activation of HLDA reverses this signal to become an input from the Bus Controller. It is then a –MEMR signal for the DMA or bus master to access system memory.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
CHM/–IO	95	O	Channel Memory I/O - This signal is a decode of the CPU's bus control signals and is sent to the Bus Controller. When combined with –CHS0 and CHS1 and decoded, the bus cycle type is defined for the Bus Controller. Activation of HLDA reverses this signal to become an input from the Bus Controller. It is then a –MEMR signal for the DMA or bus master to access system memory.
–BLKA20	96	O	Block A20, active low - An output driven to the Bus Controller to de-activate address bit 20. It is a decode of the A20GATE signal and Port A bit 1 indicating the dividing line of the 1 Mbyte memory boundary. Port A bit 1 may be directly written or set by a read of I/O port EEh.
BUSOSC	73	I-TTL	Bus Oscillator - This signal is supplied from an external oscillator. It is supplied to the Bus Controller when the VL82C320's internal configuration registers are set for asynchronous slot bus mode.
BUSCLK	97	O	Bus Clock - This is the source clock used by the Bus Controller to drive the slot bus. It is two times the AT bus clock (SYSCLK). It is a programmable division from TCLK2 or BUSOSC.
DMAHRQ	83	I-CMOS	DMA Hold Request, active high - This signal is an input sent by the Bus Controller. It is internally synchronized by the VL82C320 before used to generate HRQ.
DMAHLDA	98	O	DMA Hold Acknowledge - An output sent to the Bus Controller which indicates that the current hold acknowledge is in response to DMAHRQ.
–BRDRAM	99	O	Board DRAM, active low - An output to indicate that on-board DRAM is being addressed.
–EALE	92	O	Early Address Latch Enable, active low - In 286 mode, this signal is generated internally by decode of the CPU status signals. In 386SX mode, the VL82C320's –ADS input is gated directly to the –EALE output.
OUT1	84	I-CMOS	Indicates a refresh request.
PERIPHERAL INTERFACE SIGNALS			
A20GATE	75	I-TTL	Address Bit 20 Enable - An input that is used internally along with Port A bit 1 to determine if A20 is passed through or forced low. It also determines the state of –BLKA20.
TURBO	76	I-TTL	Turbo, active high - This input to the VL82C320 determines the speed at which the system board operates. It is internally ANDed with a software settable latch. When high, operation is at full speed. When low, CLK2 is divided by the value coded in configuration register MISCSET[4:3]. Turbo mode is active only when all TURBO requests are active.
–RC	77	I-TTL	Reset Control, active low - The falling edge of this signal causes a RESCPU signal.
BUS INTERFACE SIGNALS			
OSC	72	I-TTL	Oscillator - This is the buffered input of the external 14.318 MHz oscillator.
–IOR	85	I-TTL	I/O Read, active low - Indicates that an I/O read cycle is occurring on the bus.
–IOW	86	I-TTL	I/O Write, active low - Indicates that an I/O write cycle is occurring on the bus.
RSTDRV	87	I-TTL	Reset Drive, active high - This signal is used to reset internal logic and to derive RESCPU, and RESNPX.
SDLH/–HL	88	I-TTL	System Data Bus Low to High/High to Low Swap - This signal is used to establish the direction of byte swaps.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–SDSWAP	89	I-TTL	System Data Bus Byte Swap Enable - This is the qualifying signal needed for SDLH/–HL.
–XDREAD	90	I-TTL	Peripheral Data Bus (XD Bus) Read - This signal determines the direction of the XD bus data flow. When this signal is high, the XD Bus is output enabled.
–LATLO	91	I-TTL	SD Bus Low Byte Latch - This signal is needed to latch the SD bus low byte or XD bus to the local data bus until the end of the bus cycle.
D15-D0	12-18, 20, 22-29	IO-TTL	CPU Data Bus - This is the data bus directly connected to the CPU. It is also referred to as the local data bus.
SD15-SD0	111-114, 116-119, 122-125, 127-130	IO-TTL	System Data Bus - This bus connects directly to the slots. It is used to transfer data to/from the slot bus.
XD7-XD0	101-107, 109	IO-TTL	Peripheral Data Bus - This bus is connected to the Bus Controller and the VL82C320. It is used to transfer data to/from on-board 8-bit peripherals.
PAR1, PAR0	21, 30	IO-TTL	Parity Bit Bytes 1 and 0 - These bits are written to memory along with their corresponding bytes during memory write operations. During memory read operations, these bits become inputs and are used along with their respective data bytes to determine if a parity error has occurred.
–PARERROR	100	O	Parity Error, active low - This signal is the result of a parity check on all reads from on-board memory.
286/–386SX	78	I-TPU	286 or 386SX Mode - Tied high or left open for 286 mode and grounded for use in 386SX based systems.
TEST MODE PIN			
–TRI	79	I-TPU	Three-state - This pin is used to drive all outputs to a high impedance state. When –TRI is low, all outputs and bidirectional pins are high impedance.
POWER AND GROUND PINS			
VDD	1, 32, 41, 58, 74, 110, 121	PWR	Power connection, nominally +5 volts. These pins should each have 0.1 µF bypass capacitors.
VSS	19, 31, 36, 42, 46, 55, 81, 82, 108, 115, 120, 126, 131	GND	Ground connection, 0 volts.

SIGNAL TYPE LEGEND

Signal Code	Signal Type	Signal Code	Signal Type
I-TTL	TTL level input	IC-OD	Open drain output
I-TPD	Input with 30k ohm pull-down resistor	O	CMOS or TTL output
I-TPU	Input with 30k ohm pull-up resistor	O-TTL	CMOS output
I-TSPU	Schmitt-trigger input with 30k ohm pull-up resistor	O-TS	Three-state output
I-CMOS	CMOS level input	GND	Ground
IO-TTL	TTL level input/ouput	PWR	Power
IT-OD	TTL level input/open drain output		

FUNCTIONAL DESCRIPTION

DETAILED SUBSYSTEM SPECIFICATIONS

The sections that follow cover detailed operational information for the various logical groupings of VL82C320 subsystems. In most of these sections, the effect of configurable elements that can be controlled via internal I/O registers is discussed at length. Operation of the indexed I/O registers is repeated in summary form in the "Functional Summary of Indexed Registers" section. However, some lesser configurable functions are described only in that section. Do not assume that the information in that section is discussed elsewhere.

CPU INTERFACE

The VL82C320 handles the top level control interface between the synchronous local and memory data bus and the asynchronous slot data bus. It intercepts the CPU's bus status and address signals, and decodes the bus access. It then decides whether to handle the bus request itself, or send it off to the VL82C331 ISA Bus Controller.

Local Bus Accesses

The VL82C320 decodes the CPU bus signals and addresses. If the decode points to on-board memory, a bank request is issued to the on-chip DRAM controller. The DRAM controller then delivers the appropriate signals to on-board memory and returns a –READYO signal. –READYO may be combined with READY signals from the coprocessor or other external devices on the D bus to form the final –READY signal driven to the CPU.

Slot Bus Accesses

The CPU makes slot bus accesses when the VL82C320 decodes the CPU's control signals as either an I/O cycle, INTA cycle or an off-board memory access (the latter includes ROM accesses). In this case, the VL82C320 latches and decodes the CPU's control signals and sends out bus cycle status signals to the Bus Controller. The Bus Controller handles control of the slot transfer. The CPU is prevented from executing another cycle until the slot cycle is completed. During a slot cycle, the –READY signal returned to the CPU from the VL82C320 is delayed until the Bus Controller notifies the VL82C320 that it has completed the data transfer via –CHREADY.

Other CPU Interface

Bus arbitration is handled with the VL82C320's DMAHRQ, DMAHLDA, OUT1, HRQ, and HLDA signals. When the VL82C320 receives an active DMAHRQ (DMA hold request) from the Bus Controller, it synchronizes the HRQ (hold request) signal with the CPU clock and relays it to the CPU. The CPU responds with HLDA (hold acknowledge) to the VL82C320 which then delivers DMAHLDA to the Bus Controller. When the system memory refresh timer expires, HRQ is sent to the CPU and HLDA is returned to indicate the CPU has given up the bus for refresh cycles.

Reset control is supplied by the VL82C320. The VL82C320 contains the PS/2-compatible Port A. It contains a bit that can be set to cause a CPU reset. A second I/O address is provided to perform the same function. The latter option is supplied for Special Features compatibility. These two controls are combined with RC (reset control) input and a RSTDRV (reset drive) hard reset to produce the synchronized RESCPU (CPU reset) delivered to the CPU. (Refer to the section "System Reset Options" for details.)

Coprocessor interface is also supplied by the VL82C320. If the system contains a coprocessor, the interface signals (–ERRORNPX, –BUSYNPX and PEREQNPX) are sent from the coprocessor to the VL82C320 and decoded to produce the proper interface signals for the CPU. The same decode determines activation of the RESNPX output to the coprocessor. This interface provides PC/AT-compatibility for use with the 287 or 387SX.

BUS CONTROLLER/SYSTEM CONTROLLER INTERCHIP COMMUNICATION CHANNEL

The asynchronous interface to the Bus Controller is handled by a group of signals from the VL82C320. –CHS0, –CHS1, and CHM/–IO define which type of cycle is to be excuted as in the table below.

CHM/–IO	–CHS1	–CHS0	Bus Cycle
0	0	0	–INTA
0	0	1	–IOR
0	1	0	–IOW
0	1	1	Reserved
1	0	0	–REFRESH
1	0	1	–MEMR
1	1	0	–MEMW
1	1	1	Reserved

ISA Bus Clock Control

Data Port EDh (R/W)	D7	D6	D5	D4 D3	D2 D1	D0
MISCSET (14)	FX Enable	F1 Ctrl	SD Drive	Slow CLK2 Divider	**Bus Clock Divider**	**Bus Mode**

The VL82C286 chip set is capable of supporting AT slot bus operation asynchronous with respect to the CPU clock. Though the ISA Bus Controller actually drives the slot bus, the VL82C320 is programmed for the specified mode and sources the required clock to the ISA Bus Controller. Whether in synchronous or asynchronous modes, the VL82C320 synchronizes the command interface between itself and the ISA Bus Controller to BUSCLK.

BUSCLK is the AT bus clock provided to the ISA Bus Controller by the VL82C320. It runs at twice the final AT slot bus frequency. MISCSET, shown above, is one of the indexed configuration registers. The lower three bits control sourcing of BUSCLK to the ISA Bus Controller. Bit 0 sets synchronous or asynchronous mode. When set to 1, asynchronous mode is selected and the BUSOSC input is routed to the programmable divider. When set to 0, TCLK2 is output to the driver. Bits 1 and 2 of MISCSET provide for a programmable BUSCLK divider. Values of bits 1 and 2 provide for division from one to four. The programmable BUSCLK divider must be set to provide a BUSCLK of 2X the desired bus frequency. When a 16 MHz external oscillator is used, a ÷1 results in 8 MHz bus operation. Power-on reset defaults to ÷4, synchronous mode. See the section "Functional Summary of Indexed Registers" for more details.

Further programmability of bus timing is afforded by the ISA Bus Controller.

DRAM SUBSYSTEM DESCRIPTION

The VL82C320 supports up to 32 Mbyte of DRAM on the system board in four 16-bit banks. Each byte contains its own parity bit for a total of 18 bits per bank. A single bank can consist of 256K 1M or 4M DRAMs.

The parts used in multiple banks can consist of all one DRAM type or mixtures of any two types. It is not possible to use all three types in a single system simultaneously and not all combinations of any two types are supported.

The VL82C320 supports four banks by providing four –RASBK signals and eight –CAS signals. This allows direct drive with no external buffering.

Several configuration registers internal to the VL82C320 are used to control the memory map, interleaving, DRAM timing and page mode. These features are discussed in the following sections. Since interleaving requires pairs of banks, various controls described next act on memory in bank pairs. The short hand notation Bank A is used when describing something that affects DRAM banks 0 and 1 as a set. Similarly, Bank B is used to describe DRAM banks 2 and 3 as a set.

Memory Maps

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
RAMMAP (03)	1	1	1	DRAM Memory Map Code				

The VL82C320 supports 26 memory maps. These maps are shown in Table 1. The table shows the DRAM combinations that are addressable in each of four 16-bit memory banks. The memory column shows the total system memory available in each memory map. The RAMMAP (4-0) column indicates the hex value written in bits 4-0 of the RAMMAP indexed configuration register in order to select each map. It should be noted that banks 0 through 3 in Table 1 refer to the "logical" banks as internally addressed by the VL82C320. The actual system board memory banks accessed by the internal signals may differ depending on the value stored in indexed configuration register RAMMOV. See the section "DRAM Remap Options" for more details.

TABLE 1. DRAM MEMORY MAPS SUPPORTED

Bank 0	Bank 1	Bank 2	Bank 3	Memory MB	RAMMAP (4-0)
256K				0.5	0
256K	256K			(1.38)1.0	(1F*)1
256K	256K	256K		1.5	2
256K	256K	256K	256K	2.0	3
1M				(2.38) 2.0	(1E*) 4
256K	1M			2.5	5
256K	256K	1M		3.0	6
1M	1M			4.0	7
1M	1M	256K		4.5	8
256K	256K	1M	1M	5.0	9
1M	1M	1M		6.0	A
1M	1M	1M	1M	8.0	B
4M				8.0	C
256K	4M			8.5	D
256K	256K	4M		9.0	E
1M	4M			10.0	F
1M	1M	4M		12.0	10
4M	4M			16.0	11
4M	4M	256K		16.5	12
256K	256K	4M	4M	17.0	13
4M	4M	1M		18.0	14
1M	1M	4M	4M	20.0	15
4M	4M	4M		24.0	16
4M	4M	4M	4M	32.0	17

*1Fh and 1Eh are special cases where the 384K of memory above 640K is mapped as extended memory. EMS and shadow RAM are unavailable in these two modes. Memory map 1h allows EMS and shadowing, but no extended memory. Memory map 0h is the only case where there is no DRAM available for shadow, extended, or expanded memory. Memory maps other than these four can support shadow, extended, and expanded memory.

DRAM Remap Options

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
RAMMAP (04)	1	1	1	DRAM Memory Map Code				

The RAMMAP register described in the previous section shows 26 distinct memory maps that are available in a TOPCAT based system. Those are actually logical memory maps. The addition of the RAMMOV function provides 16 different ways to map the logical maps into the four possible physical DRAM banks. The combination of these two register functions provides a large number of unique ways to create a valid TOPCAT memory map. This capability provides two key features for the end user.

Easier DRAM Memory Upgrades

The physical DRAM banks need not be populated in the same order as would normally be dictated by the RAMMAP options alone. One example of when this is useful is the case where a system with one bank of 1M DRAMs is upgraded by adding a second bank of 256K DRAMs. Without the RAMMOV feature, it would be necessary to remove the 1M DRAM bank and move it to physical bank 1 then put the 256K DRAMs in physical bank 0. Using RAMMOV allows the 1M DRAMs to be left in place. The 256K DRAMs may be placed in any of the three available physical DRAM banks remaining. The proper RAMMOV code is then programmed so that the logical memory map (RAMMAP=5h) is correctly routed to the proper physical DRAM devices.

DRAM Error Recovery

In case of a partial or total DRAM bank failure, the remaining functional DRAMs can be switched into an alternate, valid logical memory map by reprogramming RAMMOV and RAMMAP together.

Table 2 shows the sixteen logical to physical mappings that are available. In the top row of this chart, the numbers 3, 2, 1 and 0 directly under "DRAM BANK MAPPING" refer to the four physical DRAM memory banks. In the sixteen rows beneath, the code that must be programmed into the RAMMOV register bits 4-0 is shown on the left side of the chart. On the right side is shown the logical bank that is mapped to the corresponding physical bank shown in the top row.

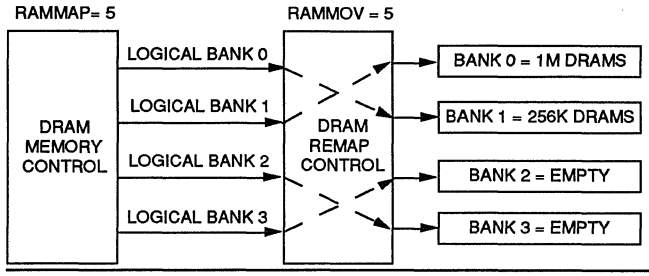
As an example, consider RAMMOV code 0001b shown in Table 2. Accesses to logical bank 3 are directed to physical bank 3. Accesses to logical bank 0 are directed to physical bank 2. Accesses to logical bank 2 are directed to physical bank 1. Accesses to logical bank 1 are directed to physical bank 0.

Note that when RAMMOV = 0000b, the default condition, the logical banks are directed to the same physical bank numbers.

TABLE 2. REMAP CONFIGURATION REGISTER CODE

RAMMOV Code				DRAM Bank Mapping				
D3	D2	D1	D0	3	2	1	0	Physical DRAM Banks
0	0	0	0	3	2	1	0	
0	0	0	1	3	0	2	1	
0	0	1	0	3	1	2	0	
0	0	1	1	3	0	1	2	
0	1	0	0	3	1	0	2	
0	1	0	1	2	3	0	1	
0	1	1	0	2	1	0	3	
0	1	1	1	2	0	1	3	Logical DRAM Banks
1	0	0	0	1	3	2	0	
1	0	0	1	1	2	3	0	
1	0	1	0	1	0	2	3	
1	0	1	1	0	3	2	1	
1	1	0	0	0	2	3	1	
1	1	0	1	0	2	1	3	
1	1	1	0	0	1	3	2	
1	1	1	1	0	1	2	3	

Example: Upgrading from one 1M DRAM bank to one 1M and one.256K bank.



Page-Mode/Interleave Subsystem Overview

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
RAMSET (05)	DRAM Drive		ESTART	1	Page Mode A	Page Mode B	Bank A Int	Bank B Int

In order to raise performance and decrease system cost, both page-mode and interleave operation are available on the system board DRAM. Interleave options are selected by the programming of the RAMSET and RAMMAP configuration registers. Page mode is enabled or disabled for each pair of DRAM banks independently. When on, it is active on all memory maps for the enabled bank pairs. Interleaving requires pairs of banks. Detailed operation of each is given in the following sections.

Interleave Operation

Two-way interleaving is automatically enabled whenever both banks of a pair are populated with like DRAM types. If all four banks are populated with like DRAMs, four-way interleaving automatically occurs when both bank pairs are programmed to interleave on the same bit. If not, two-way interleaving occurs. If the four banks are not populated with like DRAMs, two-way interleaving occurs on pairs that are of the same type. In a machine with three banks populated, the first two banks two-way interleave if they are of the same type. The third does not interleave. Table 3 shows the automatic interleaving options that occur versus the number of populated banks. All combinations not shown are unsupported. Table 3 also shows that 0, 1, 2, and 3 are the designations for each of the four DRAM banks. In the columns below these designators, "Yes" or "No", indicate whether the bank is populated. There is no configuration register programmability for enabling the interleave mode. All interleaving options (none, two-way, or four-way) occur automatically as the result of the memory map programmed into RAMMAP.

While the use of interleave is automatic and not programmable via the configuration registers, it is possible to select which bit is used for interleaving. Configuration register RAMSET bit 1 programs the Bank A interleave and bit 0 programs the Bank B interleave. When set to 0, interleave occurs on bit 1. This is called "word interleaving". When set to 1, interleave occurs on bit 10 regardless of DRAM types used. This is called "block interleaving". When all four DRAM banks are populated with like part types and bit 0 and bit 1 are set differently, two-way interleaving occurs. When they are the same, four-way interleaving occurs.

Page-Mode Operation

Interleaving operates independently of page mode. Once the desired interleave bits are set, the remaining interleave modes are automatically selected by the programmed memory map. Page-mode control is given by two configuration register bits in the RAMSET register. Bit 3 = 1 enables page-mode operation on DRAM banks 0 and 1. Bit 2 = 1 enables page-mode operation on banks 2 and 3.

When activated for a bank pair, page mode is active whether one bank or both are populated. When four-way interleaving is active it is possible to have page mode active on either, neither, or both DRAM bank pairs. This does not impact the automatic interleaving, though it impacts performance.

When pairs of banks are installed interleaving is automatically enabled. The combination of page mode with interleaving results in the best possible combination of fast system memory operation using the most cost effective DRAMs. When accesses interleaved between banks occur, CAS precharging of the next bank to be accessed occurs while CAS is active on the current bank. This has the effect of multiplying the effective page size by the number of banks being interleaved, thus increasing the odds of page hit cycles.

Tables 4, 5, and 6 show how the CPU address lines are used to accomplish the interleave options possible with the three supported DRAM types. The top portion of each table shows the CPU address lines that are strobed onto MA0-MA10 by CAS, the column address strobe. The middle portion of each table shows the CPU address lines strobed onto MA0-MA10 by –RASBK, the row address strobe. The bank select box shows the CPU address bit(s) used for interleaving. The bank enable decodes further qualify whether the CPU address is in the range of current memory map.

TABLE 3. AUTOMATIC INTERLEAVE VS. MEMORY MAP

Bank 0	Bank 1	A Bank Address Mode	Bank 2	Bank 3	B Bank Address Mode
Yes	No	Linear	No	No	N/A
Yes	Yes	2-Way Interleave	No	No	N/A
Yes	Yes	2-Way Interleave	Yes	No	Linear
Yes	Yes	2-Way Interleave 0 and 1*	Yes	Yes	2-Way Interleave 2 and 3*

*This is for the case where Banks A and B contain different types of DRAMs. For memory maps 05h, 0Bh, and 17h, all four banks contain the same DRAM type and four-way interleaving is used if both bank pairs interleave on the same bit.

TABLE 4. 256K DRAM INTERLEAVE MAPPING

	No Interleave	2-Way Block	2-Way Word	4-Way Block	4-Way Word	Memory Address
Column Address	3	3	3	3	3	0
	4	4	4	4	4	1
	5	5	5	5	5	2
	6	6	6	6	6	3
	7	7	7	7	7	4
	8	8	8	8	8	5
	9	9	9	9	9	6
	1	1	10	1	10	7
	2	2	2	2	11	8
	–	–	–	–	–	9
	–	–	–	–	–	10
Row Address	18	18	18	18	18	0
	17	17	17	17	17	1
	16	16	16	16	16	2
	15	15	15	15	15	3
	14	14	14	14	14	4
	13	13	13	13	13	5
	12	12	12	12	12	6
	11	11	11	20	20	7
	10	19	19	19	19	8
	–	–	–	–	–	9
	–	–	–	–	–	10
Interleave Bits	–	10	1	10	1	
	–	–	–	11	2	
Bank Enable Decodes	19					
	20	20	20	–	–	
	21	21	21	21	21	
	22	22	22	22	22	
	23	23	23	23	23	
	24*	24*	24*	24*	24*	

* Address line 24 is generated internally by the EMS subsystem. Memory space above 16 Mbytes can only be accessed through the EMS registers when the EMS subsystem is active.

Note: For the 256K options: CA[10]=A12 for RAMMAP=13; A11 for all others.
CA[9]=A11 for RAMMAP=9, 13; A10 for all others.
RA[10]=A22 for RAMMAP=D, E; A23 for all others.
RA[9]=A20 for RAMMAP=5, 6; A21 for all others.

TABLE 5. 1M DRAM INTERLEAVE MAPPING

	No Interleave	2-Way Block	2-Way Word	4-Way Block	4-Way Word	Memory Address
Column Address	3	3	3	3	3	0
	4	4	4	4	4	1
	5	5	5	5	5	2
	6	6	6	6	6	3
	7	7	7	7	7	4
	8	8	8	8	8	5
	9	9	9	9	9	6
	1	1	10	1	10	7
	2	2	2	2	11	8
	10	11	11	12	12	9
	–	–	–	–	–	10
Row Address	18	18	18	18	18	0
	17	17	17	17	17	1
	16	16	16	16	16	2
	15	15	15	15	15	3
	14	14	14	14	14	4
	13	13	13	13	13	5
	12	12	12	22	22	6
	11	20	20	20	20	7
	19	19	19	19	19	8
	20	21	21	21	21	9
	–	–	–	–	–	10
Interleave Bits	–	10	1	10	1	
	–	–	–	11	2	
Bank Enable Decodes	21	–	–	–	–	
	22	22	22	–	–	
	23	23	23	23	23	
	24*	24*	24*	24*	24*	

* Address line 24 is generated internally by the EMS subsystem. Memory space above 16 Mbytes can only be accessed through the EMS registers when the EMS subsystem is active.

Note: For 1 Megabyte options: CA[10]=A12 for RAMMAP=15; A11 for all others.
RA[10]=A22 for RAMMAP=F, 10; A23 for all others.

TABLE 6. 4M DRAM INTERLEAVE MAPPING

	No Interleave	2-Way Block	2-Way Word	4-Way Block	4-Way Word	Memory Address
Column Address	3	3	3	3	3	0
	4	4	4	4	4	1
	5	5	5	5	5	2
	6	6	6	6	6	3
	7	7	7	7	7	4
	8	8	8	8	8	5
	9	9	9	9	9	6
	1	1	10	1	10	7
	2	2	2	2	11	8
	10	11	11	12	12	9
	11	12	12	13	13	10
Row Address	18	18	18	18	18	0
	17	17	17	17	17	1
	16	16	16	16	16	2
	15	15	15	15	15	3
	14	14	14	14	14	4
	13	13	13	24*	24*	5
	12	22	22	22	22	6
	20	20	20	20	20	7
	19	19	19	19	19	8
	21	21	21	21	21	9
	22	23	23	23	23	10
Interleave Bits	–	10	1	10	1	
	–	–	–	11	2	
Bank Enable Decodes	23	24*	24*	–	–	
	24*	–	–	–	–	
	–	–	–	–	–	
	–	–	–	–	–	

* Address line 24 is generated internally by the EMS subsystem. Memory space above 16 Mbytes can only be accessed through the EMS registers when the EMS subsystem is active.

Programmable Memory Timing

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
RASTMA (07)	RAS ADDSEL	tRCD	1	tRP		tRAS		
CASTMA (08)	tCASW		tCST	tCP		1	tCASR	
RASTMB (09)	RAS ADDSEL	tRCD	1	tRP		tRAS		
CASTMB (0A)	tCASW		tCST	tCP		1	tCASR	

System board memory timing for this chip set is not specified in wait states. Instead, each of the critical DRAM timing parameters is specified as a number of programmable clock cycles. This allows virtually unlimited flexibility in matching DRAM specs to system CPU speed. The number of wait states for the system is whatever falls out of the programmed parameters. Banks A and B are programmed separately. This allows a user who later adds memory to maximize the speed advantage of faster parts when these chips are accessed. Conversely, a user can add slower parts for a cost savings without slowing down accesses to the entire memory system.

Four configurations registers are used to program the DRAM timing parameters. RASTMA allows programming of RAS ADDSEL delay, tRCD, tRP, and tRAS parameters for banks 0 and 1. RASTMB performs the same functions for banks 2 and 3.

CASTMA allows programming of tCST, tCP, tCASR, and tCASW for banks 0 and 1. CASTMB performs the same functions for banks 2 and 3.

The section "Functional Summary of Indexed Registers" discusses the range programmability for each parameter. Figures 2 and 3 show the relationship between these programmable timing signals for page and non-page-mode operation.

FIGURE 2. –RASBK/–CAS TIMING MODEL

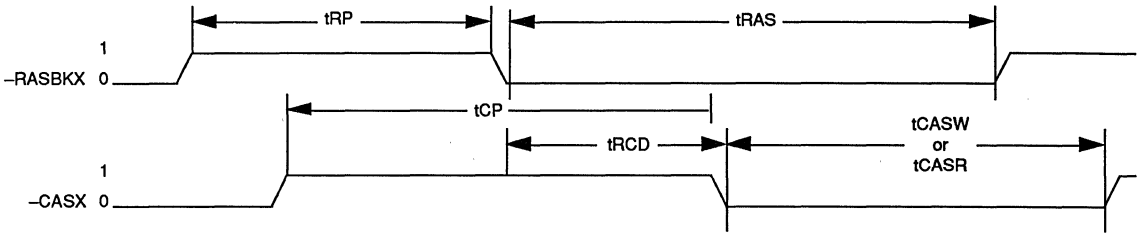
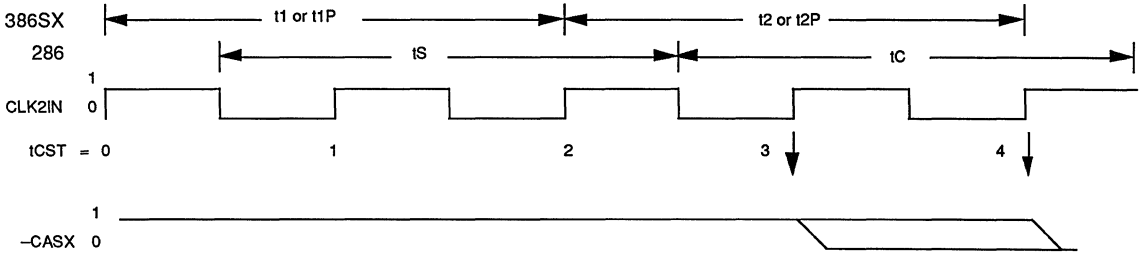
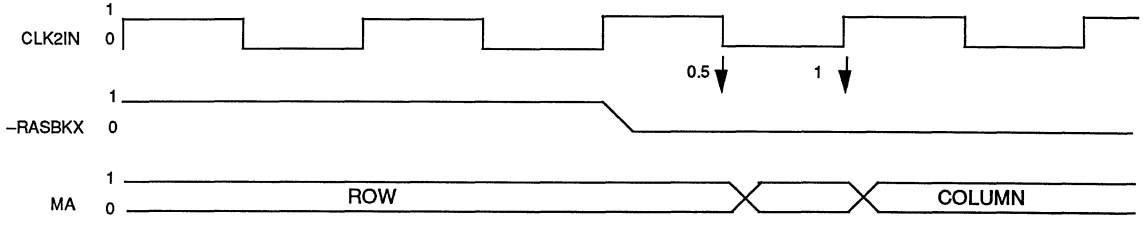


FIGURE 3. –CAS START TIME (tCST) TIMING MODEL



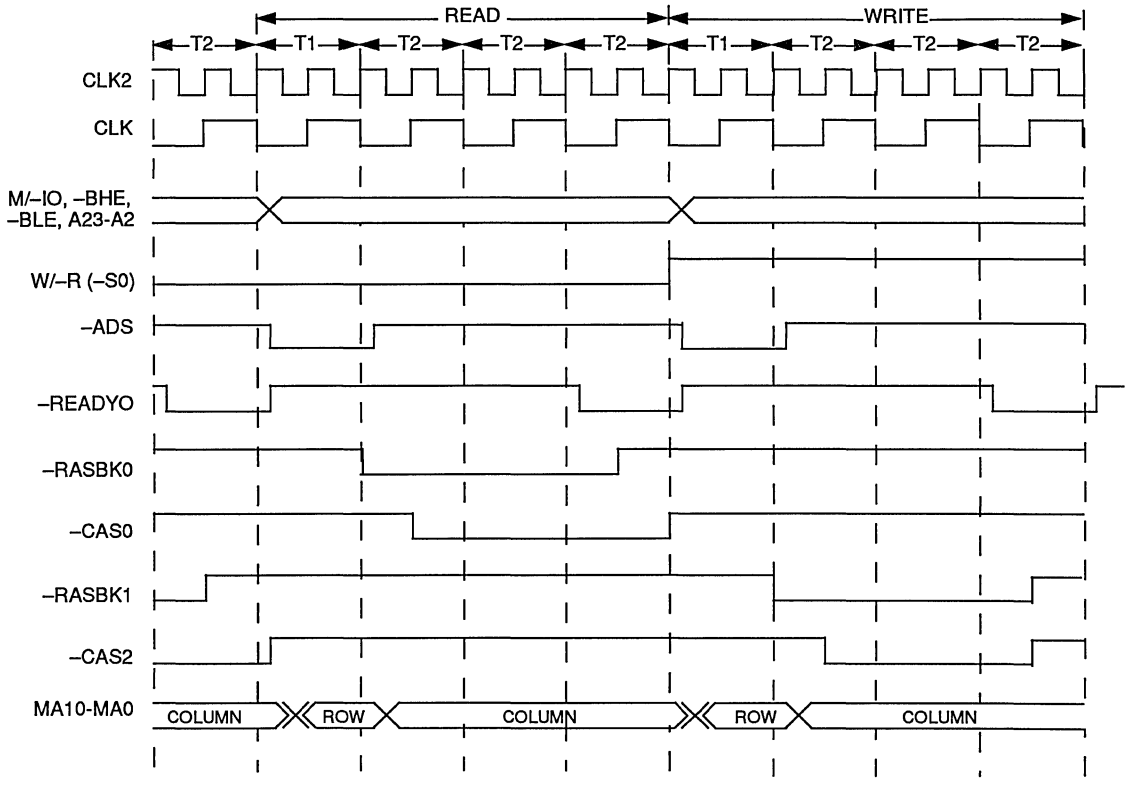
Note: tCST applies to write cycles only and equals 3 or 4. During read cycles, CAS start time defaults to zero CLK2's for pipelined or two CLK2's for non-pipelined SX or 286 mode. Iff ESTART bit in RAMSET register is programmed inactive (1), then add one to start times just mentioned for reads only. This is the earliest time –CAS can start for read cycles. Actual –CAS start time may be delayed due to –CAS pre-charge or –RASBK to –CAS delay time not yet met.

FIGURE 4. –RAS TO ADDSEL TIMING MODEL



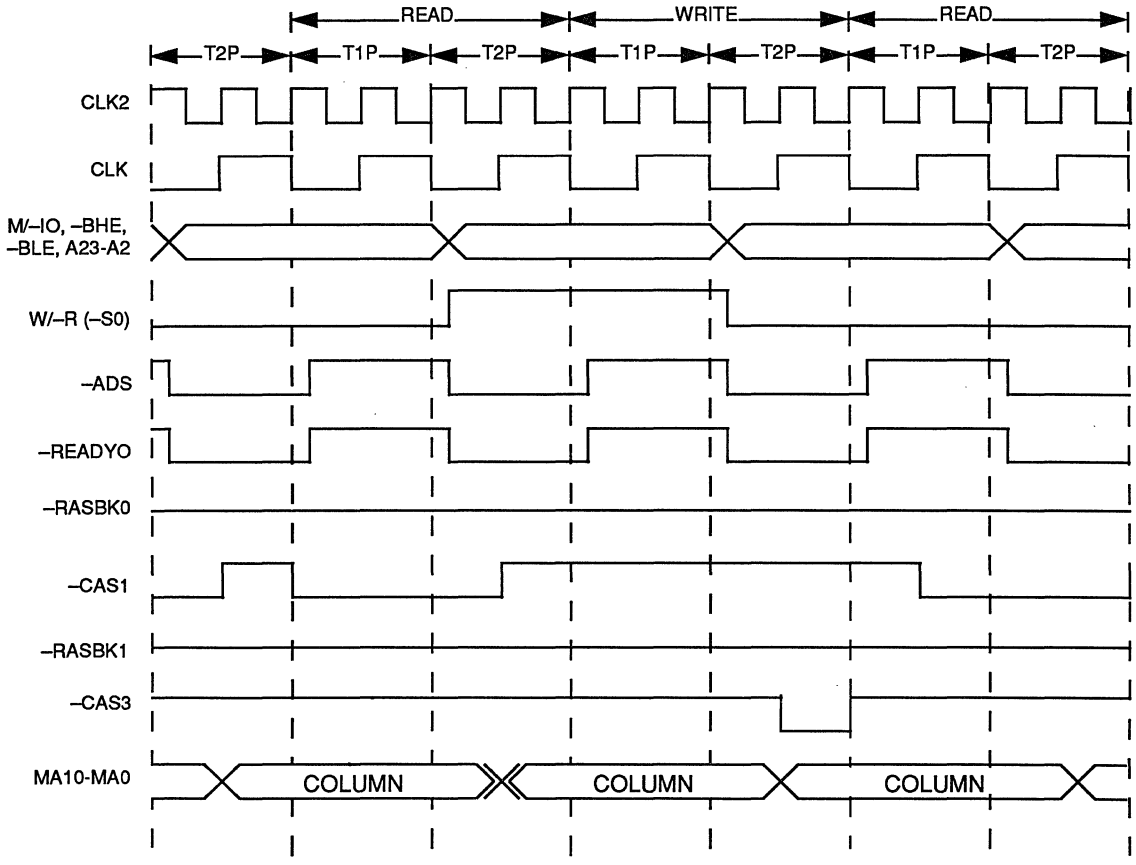
Note: Address Select can be programmed to switch MA lines 1/2 CLK2 or one CLK2 cycle after –RASBK.

FIGURE 5. NON-PAGE MODE, TWO-WAY INTERLEAVE, NON-PIPELINED



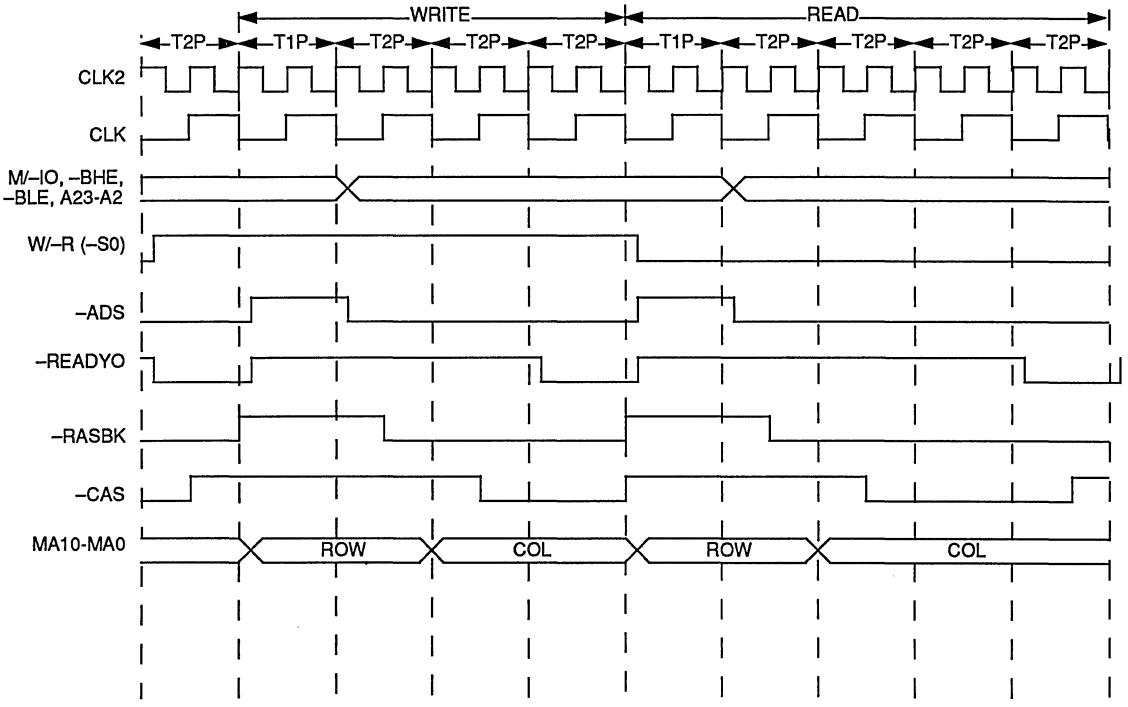
This diagram pertains to 386SX-based systems only and shows a read and write cycle with on-board memory on the D bus. Signals shown are for a two-way interleaved cycle to the first two banks (low byte) of system memory in non-pipelined mode. The –RASBK, –CAS, and MA signals can be shaped and moved in time in increments of CLK2 by varying the programmable timing values. RAMSET register bit 5 (ESTART) is active (0).

FIGURE 6. PAGE MODE, PAGE HITS, PIPELINED, TWO-WAY INTERLEAVED



This diagram pertains to 386SX-based systems only and shows read and write cycles for page mode, page hit operations. Two-way interleaving is shown on the first two memory banks for a pipelined cycle. The –RASBK and –CAS signals can be shaped and moved in time in increments of CLK2 by varying the programmable timing values. RAMSET register bit 5 (ESTART) is programmed active (0).

FIGURE 7. PAGE MODE ON (PAGE MISSES)



This diagram pertains to 386SX-based systems only and shows a read and write cycle for page mode, page miss operations. The –RASBK and –CAS signals can be shaped and moved in time in increments of CLK2 by varying the programmable timing values. RAMSET register bit 5 (ESTART) is programmed active (0).

Programmable Refresh Control

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
REFCTL (06)	Decup	Slow Refresh Divider-System Board			10/16 IO	Slow Refresh Divider-Slots		

Power-up Defaults
The DRAM system resets to a default state on power-up that allows any configuration to run, although it is a less than optimum state until BIOS or POST configures the registers with desired values. The defaults are:

- One bank of 256K DRAM
- Direct mapping from logical to physical DRAM banks
- Page mode on
- Timing for 120 ns DRAMs in 25 MHz systems

Hold Request Arbiter
The hold request arbiter is used to select between the two possible sources for a hold request to the CPU. A hold request can be generated when DMA Controller 2 in the Bus Controller issues a hold request via the DMAHRQ signal or when the output of counter 1 in the 8254 megacell of the Bus Controller makes a low to high transition. This latter signal is the OUT1 signal from the Bus Controller to the VL82C320.

At the end of a hold request from either source, the arbiter checks to see if the other source is still requesting a hold. If it is, the arbiter will give an acknowledge signal to that source and leave the HRQ line active. This will continue as long as one of the two sources is requesting a hold. Only if neither source is requesting a hold will the arbiter negate the HRQ signal and return control back to the CPU. The acknowledge to the DMA is via the VL82C320's DMAHLDA output. The acknowledge signalling for refresh is more complex due to the coupled and decoupled refresh modes. In coupled mode, an acknowledge occurs in the form of an active signal on the VL82C320's –REFRESH pin. A completely different mechanism is used in decoupled refresh mode. See the sections on "refresh" for details.

System Board DRAM Refresh
The VL82C320 performs on-board DRAM refresh and controls both on- and off-board refresh timing in all modes. Refresh may be performed in a coupled mode or decoupled mode. In coupled mode, refresh timing for both system board and slot bus refreshes is performed in a synchronous manner. In decoupled mode, the VL82C320 has complete control over the timing of on-board DRAM refresh and and off-board refresh but the timing of each is independent.

When set to coupled refresh mode (D7 = 0), the VL82C320 refresh circuitry controls system board refresh and slot bus refresh in a synchronous manner. In that mode, the division specified by bits 2-0 applies to on- and off-board refresh and bits 6-4 have no effect. Only in decoupled mode (D7 = 1), do the three bits 6-4 of the VL82C320's REFCTL register apply. In decoupled mode, the VL82C320 refreshes the on-board DRAM independent of the Bus Controller's refresh of the slot bus resident memory. It uses the division rate specified in those bits while the slot bus refresh is performed at the rate specified by the code in bits 2-0. Refer to the section "Functional Summary of Indexed Registers" for the range of refresh division mapped to the three bits 2-0 and the three bits 6-4.

Coupled Refresh Control
This is the PC/AT-compatible refresh mode. If bits 2-0 of the REFCTL register are set to their default value of 0h, the15 µsec, compatible timing is used. Other valid values, as specified in the section "Functional Summary of Indexed Registers," cause the refresh to occur at a slower rate in support of newer, low power, slow refresh DRAMs. These slower rates are all divisions of the normal 15 µsec timer provided by the Bus Controller on pin OUT1.

In sleep mode, –CAS before –RAS refresh may be used for on-board memory. This significantly reduces power requirements. The DRAMs generate their own refresh addresses internally. Therefore, the VL82C320 is not required to drive the memory address bus during refresh. When not in sleep mode, –RAS only refresh mode is used.

Decoupled Refresh Control
Decoupled refresh mode provides advantages to the user. It allows system board memory and slot memory to be refreshed at different rates. This is useful if slow refresh DRAMs are used in one location and not the other. System board refreshes are performed during slot bus cycles. Therefore, it is not necessary to add refresh cycles and their attendant overhead. Similarly, when the VL82C320 instructs the Bus Controller to perform a slot bus refresh, it can then allow the CPU to continue execution. Only if the CPU requires a slot bus access during this time, will refresh overhead occur.

SLTPTR - Critical Memory Control Element

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
SLTPTR	A23	A22	A21	A20	A19	A18	A17	A16

SLTPTR is a pointer to a 64K memory boundary between 256K and 16M. Eight bits are required to specify this range. They are used to compare to address lines A16-A23. SLTPTR sets the 64K boundary above which CPU addresses are directed to the AT slot bus. Any system board memory from 1 Mbyte up to SLTPTR is accessible as on-board extended memory. From SLTPTR up to 16 Mbytes, slot bus DRAM extended memory resides.

When the on-board EMS backfill system is disabled, SLTPTR can also be set below 1 Mbyte. At least one bank of 256K RAMs must be on the system board on reset for a physical memory size of 512K. The minimum valid value for SLTPTR is 04h to allow slot memory cards, especially EEMS capable boards, to backfill down to 256K. This capability is provided for any users who prefer to not use the built-in EEMS system. Any value between 04h and 09h makes the portion of system board DRAM from that address to A0000H inaccessible when the on-board EMS system is inactive. The set of usable values for SLTPTR is 04h to FDh. A value of FEh or FFh results in no off-board accesses since CPU accesses in the FE0000h and FF0000h segments always result in ROM chip selects. Any out of range value is treated the same as FFh.

Exceptions to the above are SLTPTR values 000Ah through 000Fh whose access is determined by the configuration of indexed registers AAXS, BAXS, CAXS, DAXS, EAXS, and FAXS described in the "EMS Subsystem" sections. Therefore, setting SLTPTR between 0Ah and 0Fh is treated the same as if the value were 10h. Default = FFh. Also see the description of the additional memory control feature provided by CTRL1 bits 7-6.

Note: The slot pointer must point to 1M or higher (≥10h) if use of the EMS backfill registers is required. Pointing SLTPTR below 640K and using the backfill registers is incompatible. Therefore, any time the SLTPTR is set between 00h and 09h the EMS backfill register enable bit in configuration register EMSEN1 is cleared. A smart BIOS setup routine does not allow this condition in actual operation.

TABLE 7. SLTPTR WITH EMS SYSTEM ENABLED

Slot Pointer Location	Effect
256K-640K	EMS backfill register automatically disabled. EMS page registers remain operational.
	CPU addresses 0 to SLTPTR are on-board DOS memory accesses.
	CPU addresses SLTPTR to 16M are slot memory accesses.
	On-board memory > SLTPTR = EMS /Shadow memory.
640K-1M 000Ah-000Fh	Respond as if SLTPTR = 0010h. (See next case.)
1M-16M 0010h-0100h	CPU addresses 0 to 640K is system board DOS memory if backfill is not enabled, otherwise, CPU addresses 0 to 256K is system board memory.
	CPU addresses 1M to SLTPTR are system board extended memory accesses.
	CPU addresses from SLTPTR to 16M accesses slot bus extended memory.
	EMS translation accesses system board RAM from SLTPTR to RAM top. Also system board RAM from 256K to 640K if backfill EMS is enabled.

Note: Table 7 does not mention what occurs for accesses between A0000h and FFFFFh. When EMS is off, the result of CPU accesses to this memory region is determined solely by configuration of registers AAXS, BAXS, CAXS, DAXS, EAXS, and FAXS. When the EMS system is enabled, the active EMS registers between CXXXXh and EXXXXh override the settings in any areas that overlap the configurations in CAXS, DAXS, and EAXS. CPU addresses that fall in the realm of EMS register control are not directly passed to the slots or the system board. The addresses are translated and access reserved areas of system board DRAM above SLTPTR or unused areas below 1 Mbyte. Table 8 summarizes the rules that are followed for all cases.

EMS Subsystem

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
EMSEN1	EMS Enable	BF Enable	Reserved	EMS MAP	B/EC000	BE/8000	B/E4000	B/E0000
EMSEN2	DC000	D8000	D4000	D0000	A/CC000	A/C8000	A/C4000	A/C0000

The EMS system consists of 72 mapping registers. They are split into a standard and alternate set of 36 registers each. The VL82C286 chip set supports the full LIM EMS 4.0 specification with any of the valid memory maps of 1 Mbyte and higher. The alternate register set allows rapid hardware context switching. Note that the VL82C286 chip set is capable of translating addresses via the EMS registers over the entire 32 Mbyte range of possible system board memory.

The EMS system is split into two parts, the 12 EMS page registers which cover the range from C0000h to EFFFFh and the 24 backfill registers that cover 40000h to 9FFFFh. Bit D7 of configuration register EMSEN1 is a global enable for the EMS page registers. Each of the 12 registers can then be individually disabled if there are system address conflicts. Bits 0 through 7 of EMSEN2 and bits 0 through 3 of EMSEN1 provide this function. The 24 EMS backfill registers are enabled by setting bit 6 of EMSEN1. These registers are all enabled or all disabled. No individual control is provided. If a full LIM EMS 4.0 system is desired, both bits 6 and 7 of EMSEN1 are set as are the desired EMS page register enable bits. Note that when EMS enable, bit 7 = 0, the state of BF enable, bit 6, has no effect on the system.

The normal EMS page register mapping to C0000h-EFFFFh can be altered by changing EMSEN1 bit 4 from 0 to 1. In this case, the 12 page registers map to AXXXXh, DXXXXh and BXXXXh in that order. In this case, EMSEN1 bits 3 through 0 work to enable or disable the BXXXXh registers rather than the EXXXXh registers. Similarly, EMSEN2 bits 3 through 0 work to enable or disable the AXXXXh registers rather than the CXXXXh registers.

When the backfill EMS registers are not used, the EMS driver allocates all memory above SLTPTR for EMS page memory. It also can use the system board memory at the same addresses as the enabled EMS page registers and any other 16K segments in the A0000h to BC000h and F0000h to FC000h areas for which the shadow code is 00b as set in configuration registers AAXS, BAXS, and FAXS. When the backfill registers are active, EMS pages can also be allocated for all system board memory from 40000h to 9FFFFh. There is no wasted DRAM in a VL82C286-based system. All memory not allocated for other purposes can be used as expanded memory.

The SLTPTR has critical effects on the EMS system. Only one effect is hardware related. When SLTPTR is set to a value from 0004h to 0009h, bit 6 of EMSEN1 is cleared. This disables the EMS backfill registers. Placement of SLTPTR is otherwise used by the EMS driver to determine the area of memory that can be allocated for use as EMS pages. Table 7 summarizes the effect of SLTPTR on the EMS system.

The EMS driver also interacts with the shadow control system through configuration registers AAXS through FAXS. Any enabled EMS page registers override the shadow control in their respective 16 Kbyte ranges. System board memory at the same address range as the EMS page registers can be allocated to the EMS memory pool by the EMS driver software. In addition, other non-EMS 16K segments can be allocated to the pool if they are not shadowed or otherwise in use. This is determined by the two shadow control bits for a specific segment. When the bits are 00b, the system board memory may be allocated to the pool. Table 8 summarizes the interaction between EMS and shadow control.

TABLE 8. INTERACTION BETWEEN EMS AND SHADOW CONTROL

EMS Enable (Bit 7)	EMS Page Enable	Shadow Control		Effect
0	Don't Care	0	0	R/W slot bus or ROM chip selects.
		1	0	Read system board or write slot (shadow).
		1	1	R/W system board.
		0	1	Read slot or ROM chip selects, write system board.
1	0 (Note 1)	0	0	CPU accesses slots, EMS may access on-board DRAM.
		1	0	Shadowed, EMS does not use.
		1	1	Used by other resource, EMS driver does not allocate.
		0	1	Setup mode active. EMS driver does not allocate (Note 2).
1	1 (Note 3)	X	X	EMS overrides use of this area.
				CPU accesses translated by EMS. System board DRAM used by EMS system for EMS memory pages.

Note 1: This case not only applies to the areas from C0000h to EFFFFh for which the EMS enable bit is turned off, but also to the A0000h to BFFFFh and F0000h to FFFFFh areas of memory. This information is supplied for use by the EMS driver code developers. Hardware operation in this mode is the same as the first case listed in Table 7.

Note 2: When an EMS driver is installed, this case should not exist. A shadow setup routine uses this code. It then changes it to 10b to enable the shadow feature. However, if an EMS driver sees this code, it may allocate the system board DRAM in this area.

Note 3: In the areas where active EMS registers reside in the CXXXXh to EXXXXh area, the control bits are overridden. Any CPU accesses to this memory space are translated and the system board memory at these addresses is allocated to the EMS page memory pool.

TABLE 9. EMS INDEX REGISTER AND DATA PORT MAP

E8h Index Port	D7	D6	D5	D4	D3	D2	D1	D0
	Set #	Auto-Inc	A5	A4	A3	A2	A1	A0
	0 = Std 1 = Alt	0 = Off 1 = On						

Data Port	Page Segment	Data Port EBh								Data Port EAh							
		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	C0/A0	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1	C4/A4	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
2	C8/A8	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
3	CC/AC	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
4	D0000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
5	D4000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
6	D8000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
7	DC000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
8	E0/B0	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
9	E4/B4	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
A	E8/B8	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
B	EC/B8	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
C	40000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
D	44000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
E	48000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
F	4C000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
10	50000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
11	54000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
12	58000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
13	5C000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
14	60000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
15	64000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
16	68000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
17	6C000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
18	70000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
19	74000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1A	78000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1B	7C000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1C	80000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1D	84000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1E	88000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1F	8C000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
20	90000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
21	94000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
22	98000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
23	9C000	1	1	1	1	1	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14

Note: A 1 indicates reserved bits that read back as logic 1.

Table 9 shows a programmer's model of the register set. Registers 0h to Bh are called the EMS page registers. Registers Ch to 23h are the backfill registers. The register set is accessed by writing a command byte to the index register located at I/O address E8h. Bits D0 through D5 contain the address of the desired EMS register from 0 to 35. Setting bit D6 to a 1 activates auto-increment. This feature is described in detail below. Bit D7 contains the desired register set to be accessed; the standard or the alternate set. I/O port addresses EAh and EBh then provide a window into the page register specified in the index register. Address EAh allows access to A14-A21. EBh allows access to A22-A24. Sixteen-bit I/O reads and writes can be used to gain access to A14-A24 in one operation via address EAh.

After initial accesses to port addresses at EAh and EBh, subsequent accesses are to the same page segment register until a new register number is written to the lower six bits of the index port at port address E8h or unless bit D6 of the index port was previously set to a logic 1. In this case, any access to port address EBh increments the page register number. (This new value is seen by a read to the index register port E8h.) The next read or write is to the next sequential page register. This feature allows the entire register set to be changed with a single access to the index register with either byte or word I/O access. For byte accesses, the lower byte at port address EAh must be written first. The access to the upper byte at EBh causes an auto-increment. Since all word accesses are made to port EAh, each one causes an auto-increment. This is due to the fact that the chip set actually breaks the word into two byte chunks, writing EAh followed by EBh.

The auto-increment feature speeds the already fast hardware driven context switching capability by minimizing the number of software instructions and, therefore, machine cycles required to read and save one context of the EMS registers, then retrieve and write another.

Configuration Enable/Disable
Ports 0F9h and 0FBh control access to the configuration registers. A write to 0FBh enables access. A write to 0F9h disables access. Since the EMS driver does not know the state of this feature when it wishes to access the configuration registers it writes 0FBh first, then writes 0F9h after its accesses are complete. This applies to all VL82C320 configuration and control registers and also to all EMS page registers discussed in this document. All such registers are mapped between I/O addresses E8h and EFh. This aids in preventing someone other than the EMS driver from inadvertently changing the EMS registers. More infomation on this feature is available in the "Dedicated Internal Control Registers" section.

Shadow RAM Ssubsystem

Data Port EDh (R/W)	D7 D6	D5 D4	D3 D2	D1 D0
AAXS	AC000 Access	A8000 Access	A4000 Access	A0000 Access
BAXS	BC000 Access	B8000 Access	B4000 Access	B0000 Access
CAXS	CC000 Access	C8000 Access	C4000 Access	C0000 Access
DAXS	DC000 Access	D8000 Access	D4000 Access	D0000 Access
EAXS	EC000 Access	E8000 Access	E4000 Access	E0000 Access
FAXS	FC000 Access	F8000 Access	F4000 Access	F0000 Access

Six indexed configuration registers are provided to give complete control over each of the 64K memory segments between 640K and 1M. The registers are called AAXS, BAXS, CAXS, DAXS, EAXS, and FAXS. Each register contains two bits for each 16K paragraph in the 64K segment controlled by that register. Refer to the section "Functional Summary of Indexed Registers" for more details.

The four modes provided are:

1. Normal PC/AT-compatible operation. This is R/W slot bus or ROM chip select depending on the memory space.
2. R/W system board DRAM. This allows complete access to DRAM in the given 16 Kbyte region.
3. Read-only DRAM. This is the normal shadow operational mode though it could be used to protect data previously written to a memory area while configured for mode 2. In this mode, writes are directed to the slot bus.
4. Shadow setup mode. In the E000 and F000 segments, reads cause on-board ROM chip selects and writes to the same address are to system board DRAM. In the segments A000 to D000 reads are from the slot bus and writes are to the system board DRAM. This allows shadowing of system board ROM as well as ROMs on a slot card.
5. Shadow RAM areas are only accessible from the CPU, not from DMAS or Masters.

NUMERICAL PROCESSOR INTERFACE

The VL82C320 supports either the Intel 287 or 387SX numeric coprocessors (NPX) for use in high performance floating point math applications. In a 286-based system, only the 287 may be used. Similarly, a 386SX-based system requires a 387SX coprocessor. It is not possible to mix CPUs and coprocessors.

The VL82C320 contains several dedicated pins in order to provide the interface between the NPX and CPU. The following sections describe the interface logic broken into several parts.

System Reset Logic

System reset is an internally generated signal caused by a reset signal to the VL82C320 (RSTDRV), usually in response to the POWERGOOD signal. This signal initiates a reset to the CPU and to the NPX.

CPU-only Reset Logic

A CPU reset without a coprocessor reset can occur for one of two reasons. The first is usually done in order to switch from real to protected mode. The signal which causes it is shown as "Hot" reset. It is triggered by setting bit 0 of I/O port 92h to a 1, by a read of I/O port EFh, or by receipt of an external –RC signal. The latter signal causes a CPU-only reset as soon as received. There is a 6.72 µsec delay between the occurrence of either of the first two events and activation of the RESCPU signal.

Internal detection of a shutdown command from the CPU also triggers a CPU-only reset.

In both of the above cases, reset is also synchronized to CLK2 and lasts for 16 CLK2 cycles.

NPX-only Reset Logic

For PC/AT-compatibility, NPX-only reset is provided via a I/O write to F1h. This action provides a reset to the NPX synchronized to CLK2 of 80 CLK2 cycles duration. –READYO does not go active after the write to F1h for 80 CLK2 cycles after the falling edge of RESNPX. There may be incompatibility with some software due to the fact that a hardware reset does not put a 387SX into the same internal state as does a reset of the 287. For this reason, the F1h reset function may be disabled by setting configuration register MISCSET[6] = 1.

Error/Interrupt Logic

For PC/AT-compatibility, –ERRORNPX active generates interrupt 13. It also latches –BUSYCPU active. This later action is required in order to prevent the CPU from attempting to use the coprocessor until the error handling interrupt routine is executed. The interrupt handler clears the latched –BUSYCPU by performing a write to I/O port F0h.

Busy Logic

The –BUSYCPU signal can be produced from three sources. It always occurs in response to the –BUSYNPX input. It also occurs as latched by the –ERRORNPX signal as previously described. Busy test logic is invoked only on system reset. At this time the 386SX self-test mode is triggered. This adds 33 ms at 16 MHz and 21 ms at 25 MHz to the CPU reset time. At the end of the self-test the BIOS can read the CPU self-test result register and perform whatever function is desired on failure. Note that when a CPU-only reset is invoked, this self-test is not performed. Therefore, "Hot" resets are performed as fast as possible.

PEREQ Logic

The PEREQNPX signal is always passed directly to the PEREQCPU pin. In addition, PEREQCPU is driven and held active as soon as –BUSYNPX goes inactive after occurrence of an active –ERRORNPX signal. The PEREQCPU signal returns to following the PEREQNPX signal after a write to I/O port F0h is performed by the NPX interrupt 13 service routine.

CPU Ready Control

On reads or writes to the 387SX, the VL82C320 automatically asserts –READYO after one wait state time-out unless the –READYI line to the VL82C320 is asserted. This prevents a system hang when a coprocessor is not present.

DEDICATED INTERNAL CONTROL REGISTERS

All Special Features (SF) decodes are between E8h and FFh as shown in Table 10. While the IBM Technical Reference Manual considers F8h to FFh reserved for coprocessor use, only F8h, FAh, FCh, and FEh are actually used. SF sandwiches some registers in this region. The recommended method is to decode the F8h to FFh range then AND with address bit –A0. This properly maps only the even addresses in this range to the coprocessor. I/O ports F0h and F1h are fully decoded due to the presence of other ports at F4h and F5h. It is possible to disable the SF functions mapped in the FXh range if they conflict with a specific design implementation. This feature is described later in this specification.

Note: The dedicated I/O registers at E8h, EAh, and E9h are described separately in the "EMS Subsystem" section. The dedicated I/O registers at ECh and EDh are described in the "Functional Summary of Indexed Registers" section.

TABLE 10. DEDICATED I/O CONTROL REGISTERS

Port Address	Function
E8h	EMS Index Register
E9h	EMS Active Set
EAh	EMS Data Port Low Byte
EBh	EMS Data Port High Byte
ECh	Configuration Index Register
EDh	Configuration Data Port
EEh	Fast A20*
EFh	Fast Reset*
F0h	Coprocessor Busy Clear
F1h	Coprocessor Reset
F4h	Slow CPU**
F5h	Fast CPU**
F8h	Coprocessor
F9h	Configuration Disable**
FAh	Coprocessor
FBh	Configuration Enable**
FCh	Coprocessor
FEh	Coprocessor

*Also can be activated through port 92h for PS/2-compatibility.

**These decodes can be disabled in case of conflict.

Note: All I/O accesses to the above registers must be byte size except the EMS data port at EAh and EBh which may be either byte or word operations.

EMS Register Set (I/O Address E9h)

E9h	D7	D6	D5	D4	D3	D2	D1	D0
EMS Register Set	X	X	X	X	X	X	X	X

A read of this address returns FFh. A read of this register activates the standard EMS register set. A write activates the alternate EMS register set. Neither of these actions has any effect if the EMS subsystem has not been enabled by setting the EMS enable bits in the EMSEN registers described in the "EMS Subsystem" and "Functional Summary of Indexed Registers" sections. Default on reset is the standard register set.

Note that this function has no relationship and is totally independent of the control afforded by bit 7 of register E8h. Bit 7 controls which register set is selected for updates to the base addresses for the EMS translation. It is possible to select and update either the standard or alternate EMS register set independent of which set is currently active.

Fast A20 (I/O Address EEh or 92h)

EEh	D7	D6	D5	D4	D3	D2	D1	D0
Fast A20	X	X	X	X	X	X	X	X

92h	D7	D6	D5	D4	D3	D2	D1	D0
Port A	1	1	1	1	1	1	CTRL	Reset

A read of I/O port EEh enables Fast A20 and returns a value of FFh. A write disables Fast A20. This method provides a fast, parallel alternative to the standard PC/AT-compatible method of using the keyboard controller to control A20. Internally, this signal and A20GATE are ORed so that either event controls the A20 address line and generates –BLKA20. Default on reset is internal A20 control disabled. While disabled, A20 is solely controlled by the A20 input for strict PC/AT-compatibility.

Fast A20 is also controlled via bit 1 of I/O register 92h for PS/2-compatibility. This register is known as Port A. When bit 1 = 1, A20 is active. When bit 1 = 0, A20 always = 0. This feature is fully integrated with the Fast A20 control achieved through EEh, i.e. a read of EEh followed by a read of bit 1 of port 92h returns a logic 1.

If bit 7 of the MISCSET register = 1, the fast A20 feature at EEh is disabled.

FAST CPU Reset (I/O Address EFh or 92h)

EFh	D7	D6	D5	D4	D3	D2	D1	D0
Fast Reset	1	1	1	1	1	1	1	1

92h	D7	D6	D5	D4	D3	D2	D1	D0
Port A	1	1	1	1	1	1	A20	Reset

This register provides an alternative to use of the –RC input in order to reset the processor. A read of EFh resets the processor. This reset signal must be ORed internally with the –RC input so that either event invokes a reset. This may provide a faster way for the system to jump between real and protected mode. Reset timing is the same as described below for the Port A reset.

Fast CPU reset can also be controlled via bit 0 of I/O register 92h for PS/2-compatibility. This register is known as Port A. When bit 0 = 1, a reset operation is triggered. Reset pulses are high for 16 CLK2s. This latch remains set until written again or until the VL82C320 is externally reset.

If bit 7 of the MISCSET register = 1, the fast CPU reset feature at EFh is disabled.

Note that in order to successfully reset a PC/AT-compatible system, A20 must be gated through and not held low, otherwise, the reset vector is not fetched and the system hangs up. Therefore, before issuing a "Hot" reset command, either via I/O port 92H or I/O port EFh as described above, one of the following must occur: 1. Set bit 1 to 1 in Port A. (Writing 03h to this register effectively accomplishes both goals with a single I/O instruction.) 2. Perform a read of EEh to enable A20.

Coprocessor Control (I/O Address 0F0h and 0F1h)

0F0h	D7	D6	D5	D4	D3	D2	D1	D0
Clear/Busy	X	X	X	X	X	X	X	X

0F1h	D7	D6	D5	D4	D3	D2	D1	D0
Reset Copro	X	X	X	X	X	X	X	X

A write to I/O port F0h clears the D-flop which holds –BUSYCPU and PEREQCPU active after an –ERRORNPX signal occurs. A write to I/O port F1h resets the NPX. This write results in a positive pulse 80 CLK2 cycles wide and is synchronized to CLK2. –READYO is held inactive during this entire period for 100 CLK2s after the falling edge of RESNPX.

Bit 6 of MISCSET must be set to 0, otherwise, a write to F1h does not cause a reset.

CPU Speed (I/O Address 0F4h and 0F5h)

0F4h	D7	D6	D5	D4	D3	D2	D1	D0
Slow CPU Speed	X	X	X	X	X	X	X	X

0F5h	D7	D6	D5	D4	D3	D2	D1	D0
Fast CPU Speed	X	X	X	X	X	X	X	X

A write to port 0F5H causes the CPU to run at normal "fast" speed. A write to port 0F4H invokes the CLK2 divider circuit. This is selected by writing the appropriate code to the MISCSET register described later in this document. The programmable range provided allows 12 to 25 MHz systems to run at or below 8 MHz. Default on reset is "fast" speed.

If bit 7 of the MISCSET register = 1, this CPU speed feature is disabled. See the description under MISCSET in the section "Functional Summary of Indexed Registers" for more details. The speed control activated by the BIOS through the keyboard controller is always available to access this function.

Configuration Enable/Disable Registers (I/O Addresses 0FBh and 0F9h)

0FBh	D7	D6	D5	D4	D3	D2	D1	D0
Config Enable	X	X	X	X	X	X	X	X

0F9h	D7	D6	D5	D4	D3	D2	D1	D0
Config Disable	X	X	X	X	X	X	X	X

When enabled and used as described above, the configuration registers are protected from unauthorized accesses that might garble the system configuration and either crash the system or change its operational characteristics in an unwanted manner. A write to 0FBh enables the configuration registers. A write to 0F9h disables the configuration registers. When disabled, the system is locked out from any access to the configuration and control ports from address E8h through EFh. This includes the registers previously described in this section, the EMS registers described in "Shadow RAM Subsystem" section and the indexed configuration registers described in the "Functional Summary of Indexed Registers" section.

If bit 7 of the MISCSET register = 1, the configuration enable/disable feature is disabled. See the description under MISCSET in the section "Functional Summary of Indexed Registers" for more details.

Sleep Mode Control Subsystem

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
SLEEP (13)	Enable	Power Down CLK2 Divider			Reserved	Reserved	Ext Ctrl 1	SYSCLK

Sleep mode operation is provided for battery operated laptop microcomputer support. The sleep indexed configuration register is provided to control this function. Bits 0 and 4 through 6 are set with the desired values by the BIOS during POST. Only bit 7 needs to be toggled to get in and out of sleep mode during operation. For maximum power savings, it is recommended that a halt instruction be executed immediately after setting bit 7.

Bit 7 is set to 1 to invoke all chip set sleep functions. When set, CLK2 is divided by the value coded in bits 4 through 6 of the sleep register except during HLDA cycles. These bits provide a code used to divide the CLK2 input for generation of CLK2 output during sleep mode. Division from 1 to 1024 is programmable. The range is specified in the "Functional Summary of Indexed Registers" section.

When used with non-static CPU's the greatest division is selected that allows CLK2 to remain above the minimum operational frequency.

Normally, –RAS-only refresh is performed. This requires driving the memory address lines and power is consumed. When bit 7 =1, the refresh controller may switch to –CAS before –RAS refresh. If –CAS before –RAS refresh is not desired while in sleep mode, setting CTRL1 bit 6 to 1 maintains standard refresh operation.

The VL82C320 is brought out of sleep mode by resetting bit 7 to a logic 0. This is done by providing a CPU write of 0 to bit 7. A hardware reset or an INTA cycle of the VL82C320 also resets this bit.

Bits 3-2 are reserved for use by external sleep control circuitry that wishes to use the same port address for logical consistency. The internal bits are read/write, but perform no other function at the present time.

Bit 0 - The sleep register is "shadowed" in the Bus Controller. That is, it exists at the same address as a write-only register in the Bus Controller. However, only bits 0 and 7 are valid in the Bus Controller. See the VL82C331 ISA Bus Controller data sheet for more details. In the VL82C320, bit 0 is a read/write bit without function. This bit is provided so that software can detect the last state written to it in the Bus Controller.

When CTRL1 bit 1 = 0, the –SLP/MISS (pin 6) provides an external indication of the inverse state of the SLEEP bit 7. That is, when pin 6 is low, sleep mode is active. This can be used as an external indicator of sleep mode or as an external sleep mode activation signal for other devices.

See the section "Sleep Mode Operation" in the VL82C331 ISA Bus Controller data sheet and the section "Functional Summary of Indexed Registers" in this data sheet for additional information.

TURBO/Slow CPU Control Subsystem

Data Port EDh (R/W)	D7	D6	D5	D4 D3	D2 D1	D0
MISCSET (14)	FX Enable	F1 Ctrl	SD Drive	**Slow CLK2 Divide**	Bus Clock Divider	Bus Mode

It has become standard for fast PC/AT-compatibles to provide means to slow operation of older, speed sensitive software. This is especially true for graphics intensive entertainment software which may otherwise operate much too fast on a high speed machine. Bits 3-4 of the MISCSET indexed configuration register are used to specify a CLK2 divider that is active when the slow CPU mode is activated. This range provides the capability to operate at 8 MHz or under, for any actual CPU speed from 12 to 33 MHz.

One way this mode may be toggled on and off is by external control of the TURBO input pin. When TURBO is low, the slow mode is activated and the CLK2 divider is in effect. When TURBO is high or during HLDA cycles, CLK2 runs at the same speed as TCLK2 (only if the SF TURBO request is also active, see above). The TURBO pin is normally connected to the keyboard controller and triggered by the BIOS via detection of a "hot key" combination such as Ctrl Alt +. This input is often externally ANDed with a mechanical turbo switch on the front panel.

For SF compatibility, another method is provided if separately enabled. A write to I/O port 0F4h also selects the CLK2 divider circuit for slow operation. A write to 0F5h returns to full speed operation. The SF must be enabled (bit 7 of MISCSET = 0) for the latter mechanism to be active. The SF internal speed control mechanism is ANDed with the TURBO input pin. In this way, any single request for slow operation causes it to occur.

Note: The state of TURBO has no impact on the slot clock frequency. See the sections "Functional Summary of Indexed Registers" and "Dedictated Internal Control Registers" for additional data.

SPECIAL CYCLES

HALT/SHUTDOWN DETECTION

The VL82C320 detects and responds as described below to halt and shutdown operations from the 286 and 386SX processors.

The chip set detects halt only to differentiate it from the shutdown cycle. No further action is taken in response to halt except to acknowledge it by asserting –READYO after two wait states.

Shutdown is handled differently. This bus cycle is executed by the CPU in response to a critical internal processing error. The VL82C320 responds by asserting –READYO after two wait states then issuing a CPU Only Reset for 16 CLK2 cycles.

COPROCESSOR CYCLES

The VL82C320 generates a –READYO signal in one wait state if the –READYI is not activated prior to this when it is in the 386SX mode. In 286 mode, coprocessor cycles are run as on-board slot bus cycles under control of the ISA Bus Controller. See Coprocessor Controller Subsection for more details.

SYSTEM RESET OPTIONS

This section describes all reset modes of the VL82C320 based on their activating signal. They have been discussed in other applicable sections of this document and are summarized as an aid to the reader.

RSTDRV: Hardware reset pin from the Bus Controller. This signal causes all internal state machines to be reset. The internal configuration registers are reset to their default values shown in Table 15. Resets are issued to the CPU and the NPX. The –BUSYCPU signal is active for at least eight CLK2 cycles before and after the falling edge of the RESCPU signal. This invokes the self-test mode of the 386SX. Systems that desire to use this feature can then read the result of this test in the 386SX's EAX register and decide what to do based on the result. Otherwise, it can be ignored. This has no effect on 286-based systems.

–RC: When active, a CPU-only reset is issued immediately on RESCPU for 16 CLK2 cycles synchronous with CLK2.

REG_92: Setting bit 0 of I/O port 92h causes a CPU-only reset. After approximately 6.75 µsec, a RESCPU is activated for 16 CLK2 cycles. See the section "Dedicated Internal Control Register" for more details.

REG_EF: A read of I/O port EFh causes a CPU-only reset. After approximately 6.75 µsec a RESCPU is activated for 16 CLK2 cycles. SF must be enabled for this feature to function. See the section "Dedicated Internal Control Register" for more details.

OUT_F1: A write to I/O port F1h causes an NPX-only reset. RESNPX is activated for 80 CLK2 cycles. Ready assertion is held off for another 100 CLK2 cycles. See the section "Dedicated Internal Control Registers" for details.

SHUTDOWN: Detection of the shutdown condition causes a CPU-only reset for 16 CLK2 cycles. See the section "Halt/Shutdown Detection" for additional information.

DATA BUFFER OPERATION

The VL82C320 data buffer functions separates the data bus into three buses, D bus, SD bus and the XD bus. The D bus is the CPU's local data bus. The VL82C320 and numeric coprocessor are connected to the D bus. BIOS ROMs are connected to the D Bus (16-bit) or the XD bus (8-bit). The SD bus is the 16-bit slot bus and the XD bus is an 8-bit bus for on-board peripherals such as the VL82C320 registers and the ISA Bus Controller. These buses can be controlled by either the CPU, a DMA controller or a bus master. Table 13 shows the source and destination buses for all possible steering functions.

In addition, the VL82C320 provides a D bus latching mechanism. The read data from the appropriate bus (D, SD, SC) is latched and re-driven to the D bus from the end of the controlling strobe (CAS, IOR, MEMR) to the point at which the CPU samples the data.

TABLE 11. 286 HALT/SHUTDOWN DETECTION

M/–IO	–S1	–S0	A1	Mode
1	0	0	1	Halt
1	0	0	0	Shutdown

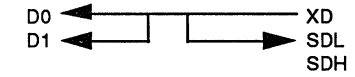
TABLE 12. 386SX HALT/SHUTDOWN DETECTION

M/–IO	D/–C	W/–R	A1	Mode
1	0	1	1	Halt
1	0	1	0	Shutdown

TABLE 13. DATA BUFFER MODE SUMMARY

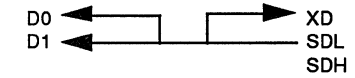
		TO D BUS		TO S BUS		
		D0	D1	XD	SDL	SDH
FROM D BUS	D0	F		D	D	
	D1		F	E	E	D E
FROM S BUS	XD	A	A		G	G
	SDL	B C	B	H	F	H
	SDH		C	I	I	F

A

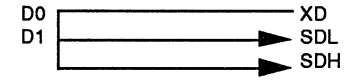


F

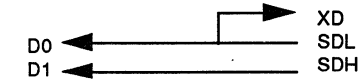
B



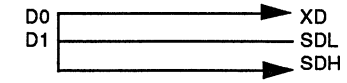
G



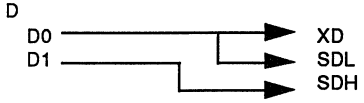
C



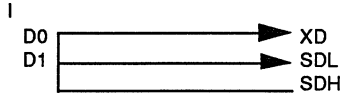
H



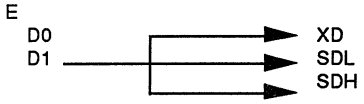
D



I



E



PARITY GENERATION AND DETECTION CIRCUIT

System board memory write cycles generate two parity bits, one for each byte of the 16-bit word bank. These bits are written out coincident with the data write. On CPU reads both system board DRAM bytes feed the parity checker. In case of a parity error, the –PARERROR line is activated to the Bus Controller.

IN-CIRCUIT TEST LOGIC

The VL82C320 is designed to make system board testing as easy as possible. The –TRI input causes all pins on the VL82C320 go to a high impedance state. This can be used to isolate the VL82C320 so other components in the system can be tested.

The –TRI input can also be used to put the VL82C320 into a special test mode called In-Circuit Test (ICT). The purpose of ICT is not to functionally test the VL82C320 while it is inserted in a circuit board, but to test that the part is connected correctly and all the pins can be toggled high and low in a predictable pattern.

During in-circuit test (ICT), each output may be toggled by one or more of the inputs. This allows for a board level tester to chek the solder connection of each pin. The sequence for enabling ICT is as follows:

1. Tester drives –TRI pin low.
2. Tester drives XD0 with a value of 1.
3. Tester simultaneously pulses –IOR and –IOW low for at least 100 ns.
4. Tester drives –TRI pin high.
5. VL82C320 remains in ICT mode until the RSTDRV pin is activated or until steps 1-4 are repeated with XD0=0.

IN-CIRCUIT TEST DESCRIPTION

ICT INPUT		ICT OUTPUT	
Signal Name	Pin #	Signal Name	Pin #
CLK2IN	2	D13	14
–READYI	3	HRQ	8
HLDA	4	PEREQCPU	11
–READYO	7	D15	12
RESCPU	8	D14	13
PAR1	21	D0	29
PAR0	30	D1	28
PEREQNPX	68	–ROMCS	63
ERRORNPX	69	–REFRESH	64
–BUSYNPX	70	IRQ13	66
TCLK2	71	–NPCS	67
286/–386SX	78	XD5	103
–CHREADY	80	XD6	102
DMAHRQ	83	–BRDRAM	99
OUT1	84	BUSCLK	97
–IOR	85	CHM/–IO	95
–IOW	86	–CHS0/–MW	93
SDLH/–HL	88	XD7	101
–SDSWAP	89	–CHS1/–MR	94
–XDREAD	90	–BLKA20	96
–LATLO	91	DMAHLDA	98
–EALE	92	–PARERROR	100
A16	139	SD6	123
A17	138	SD4	125
A18	137	SD2	128
A19	136	SD1	129
A20	135	SD0	130
A21	134	SD3	127
A22	133	SD5	124
A23	132	SD7	122
–ADS	160	CLK2	5
M/–IO	159	–BUSYCPU	10
D/–C (–S1)	158	–SLP/MISS	6

ICT INPUT		ICT INPUT		ICT OUTPUT	
Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
MA10	33	–RAMW	48	D12	15
MA9	3	–RASBK3	59	D11	16
MA8	35	–RASBK2	60	D10	17
MA7	37	–CAS7	49	D9	18
MA6	38	–CAS6	50	D8	20
MA5	39	–CAS5	51	D7	22
MA4	40	–CAS4	52	D6	23
MA3	43	–CAS3	53	D5	24
MA2	44	–CAS2	54	D4	25
MA1	45	–CAS1	56	D3	26
MA0	47	–CAS0	57	D2	27
A1	154	A15	140	SD8	119
A2	153	A14	141	SD9	118
A3	152	A13	142	SD10	117
A4	151	A12	143	SD11	116
A5	150	W/–R (–S0)	157	SD12	114
A6	149	–BLE (A0)	156	SD13	113
A7	148	–BHE	155	SD14	112
A8	147	–RASBK1	61	SD15	111
A9	146	–RASBK0	62	XD0	109
A10	145	RESNPX	65	XD1	107
A11	144	OSC	72	XD2	106
BUSOSC	73	TURBO	76	XD3	105
A20GATE	75	–RC	77	XD4	104

CONFIGURATION REGISTER SET
Software Access
Index Registers (I/O Address ECh)
The value written to this register is the 8-bit address of the data port which is accessed through the data port register at I/O address EDh. All subsequent data port reads and writes accesses the register at this address until the index register is written with a new 8-bit address. This register is readable. It always returns the last value written to it.

The Configuration Registers can only be accessed via the CPU and are limited to byte reads and writes.

Data Port Register (I/O Address EDh)
Each register accessible through I/O address EDh is functionally described below. It is accessed first by writing its address to the index register at I/O address ECh, then by accessing the data port at I/O address EDh.

FUNCTIONAL SUMMARY OF INDEXED REGISTERS
Version (00h) (Read-only)
D2-D7 contains a read-only code which indicates that this part is a VLSI Technology PC/AT-compatible System Controller/Data Buffer (VL82C320). D0 and D1 contain the version number of this chip. The first version of this chip uses the code E0h. Breaking the code into two bit pieces reveals it to be "320" Rev "0."

COMPAT (01h)
Bits 7-0 are read-only and always return logic 1's. This register is included for compatibility with the Bus Controller.

SLTPTR (02H) (Default = FFh)
The SLTPTR register represents the upper address bits of the base address where off-board (slot) memory accesses begin. It contains a full 8 bits corresponding to A16-A23. (For more details, see SLTPTR - Critical Memory Control Element Section.)

RAMMAP (03h) (Default = E0h)
Bit 7 in conjunction with the EAXS register determines system response to memory accesses between 0E0000h-0EFFFFh. When set to a logic 1 and the EAXS code for the specific 16K segment is 00b, reads generate a –ROMCS and a ROM access is performed from either the D or XD bus depending on whether 8-or 16-bit ROM BIOS is used. When set to logic 0 and the EAXS code for the specific 16K segment is 00b, reads and writes are performed to the slot bus. This feature allows systems not using a 128K BIOS to access memory devices on the slot bus in the 0E0000h-0EFFFFh area. See EAXS below for further details. Accesses to the area between FE0000h-FEFFFFh also respond in the above manner except that EAXS has no control over this memory space.

Bits 4-0 specify one of the valid memory maps as shown Table 1. Note that not all possible 5-bit codes are assigned to valid memory maps.

RAMMOV (04H) (Default = F0h)
Bits 3-0 specify a switching function which determines which internal –RASBK3 - –RASBK0 signals drive which external –RASBK3 - –RASBK0 pins.

Refer to Table 2 for the REMAP configuration register code mapping.

RAMSET (05h) (Default = 3Ch)
Bits 7-6 program the drive current on lines MA0-MA10 and on –RAMW according to the following codes:
00 = 150 pF drive (Default)
01 = 300 pF drive
10 = 450 pF drive
11 = 600 pF drive

Bit 5 is set to 0 in order to allow a cycle to begin one CLK2 earlier. This provides extra access time. (Default = 1 Early Start Disable) Early Start may be enabled in systems running at 16 MHz or below.

Bit 3 indicates whether page mode is active on Bank A.
0 = disabled
1 = enabled (Default)

Bit 2 indicates whether page mode is active on Bank B.
0 = disabled
1 = enabled (Default)

Bit 1 indicates the interleave mode for Bank A.

0 = Interleave on bit 1 for all DRAMs (Default)
1 = Interleave on bit 10 for all DRAMs

Bit 0 indicates the interleave mode for Bank B.

0 = Interleave on bit 1 for all DRAMs (Default)
1 = Interleave on bit 10 for all DRAMs

REFCTL (06h) (Default = 00h)
Bit 7 is 0 for coupled refresh mode and 1 for decoupled refresh mode. (Default = 0.)

Bits 6-4 provide three bits to specify a divider for on-board refresh.
000 = + 1 (Default)
001 = + 2
010 = + 4
011 = + 8
100 = + 16

Bit 3 controls internal I/O decode. When bit 3 = 0, full 16-bit decode is performed. When bit 3 = 1, 10-bit decode is performed. (Default = 0.)

Bits 2-0 provide three bits which specify a divider for off-board refresh.
000 = + 1 (Default)
001 = + 2
010 = + 4
011 = + 8
100 = + 16

RASTMA - RAS Timing for DRAM Banks 0 and 1 (07h) (Default = FFh)
Bit 7 indicates the –RAS to Column Address delay.
0 = 1/2 CLK2
1 = 1 CLK2 (Default)
Refer to Figure 4.

Bit 6 indicates number of clock delays between –RAS and –CAS (tRCD). Actual clock delays encoded by this bit are:
0 = 1 CLK2
1 = 2 CLK2s (Default)
Refer to Figure 2.

Bits 4-3 indicate the number of clock periods of –RAS precharge time (tRP). Bit encoding relative to the number of clocks is:
00 = 2 CLK2s
01 = 3 CLK2s
10 = 4 CLK2s
11 = 5 CLK2s (Default)
Refer to Figure 2.

Note: In 286 mode, these times may be one half CLK2 longer than programmed.

Bits 2-0 indicate the number of clock periods of –RASBK active time (tRAS). Bit encoding relative to the number of clocks is:

010 = 2 CLK2s
011 = 3 CLK2s
100 = 4 CLK2s
101 = 5 CLK2s
110 = 6 CLK2s
111 = 7 CLK2s (Default)
Refer to Figure 2.

Note: In 286 mode, these times may be one half CLK2 shorter than programmed.

CASTMA - CAS Timing for DRAM Banks 0 and 1 (08h) (Default = B7h)
Bits 7-6 indicate the number of clock cycles of –CAS active time during memory writes (tCASW):
00 = 1 CLK2
01 = 2 CLK2s
10 = 3 CLK2s (Default)
11 = 4 CLK2s
Refer to Figure 2.

Note: In 286 mode, these times may be on half CLK2 shorter than programmed.

Bit 5 indicates the number of CLK2s of delay that occur before –CAS goes active after the start of the status cycle (tCST). This parameter is applicable to write operations only.
0 = 3 CLK2s
1 = 4 CLK2s (Default)
Refer to Figure 3.

Bits 4-3 indicate the number of clock cycles of –CAS precharge time (tCP). Bit encoding relative to the number of clocks is:
00 = 1 CLK2
01 = 2 CLK2s
10 = 3 CLK2s (Default)
Refer to Figure 2.

Note: In 286 mode, these times may be one half CLK2 longer than programmed.

Bits 1-0 indicate the number of clock cycles of –CAS active time during memory reads (tCASR). Bit encoding relative to the number of clocks is:
01 = 2 CLK2s
10 = 3 CLK2s
11 = 4 CLK2s (Default)
00 = 5 CLK2s
Refer to Figure 2.

Note: In 286 mode, these times may be on half CLK2 shorter than programmed.

RASTMB - RAS Timing for DRAM Banks 2 and 3 (09h) (Default = FFh)
See RASTMA for bit definitions.

CASTMB - CAS Timing for DRAM Banks 2 and 3 (0Ah) (Default = B7h)
See CASTMA for bit definitions.

EMSEN1 (0Bh) (Default = 00h)
Bit 7 is set as global enable for the EMS translation registers from C0000h to EC000h.
0 = EMS disable (Default)
1 = EMS enable

Bit 6 is set as the global enable for the EMS backfill translation registers from 40000 to 9C000h.
0 = Backfill Disable (Default)
1 = Backfill Enable

Bit 4 determines the EMS window range.
0 = EMS Map 0
1 = EMS Map 1

Each bit below is associated with one of the EMS registers. A 0 indicates that the associated page register is disabled. A 1 indicates that it is enabled.

Page Controlled by each bit:

Bit 0	EMS Page 8
Bit 1	EMS Page 9
Bit 2	EMS Page 10
Bit 3	EMS Page 11

EMSEN2 (0Ch) (Default = 00h)
Each bit is associated with one of the EMS registers. A 0 indicates that the associated page register is disabled. A 1 indicates that it is enabled.

Page Controlled by each bit:

Bit 0	EMS Page 0
Bit 1	EMS Page 1
Bit 2	EMS Page 2
Bit 3	EMS Page 3
Bit 4	EMS Page 4
Bit 5	EMS Page 5
Bit 6	EMS Page 6
Bit 7	EMS Page 7

SHADOW CONTROLLER REGISTERS (Default = 00h)
The following registers provide control over the memory range from 640K to 1 Mbyte. Each pair of bits control one 16K page as defined below:
00 = Read (Default), Write Slot Bus
01 = Read (Default), Write System Board
10 = Read System Board, Write Slot Bus
11 = Read/Write System Board

*In the address space F0000h to FFFFFh, Default means accesses are from on-board ROM space. Default accesses in areas from A0000h-DFFFFh are from the slot bus. Default in the area from E0000h-EFFFFh can be either on-board ROM or slot bus accesses depending on the state of RAMMAP bit 7.

AAXS (0Dh) *Default is always the slot bus.
Bits 6-7 - segment at AC000h.
Bits 4-5 - segment at A8000h.
Bits 2-3 - segment at A4000h.
Bits 0-1 - segment at A0000h.

BAXS (0Eh) *Default is always the slot bus.
Bits 6-7 - segment at BC000h.
Bits 4-5 - segment at B8000h.
Bits 2-3 - segment at B4000h.
Bits 0-1 - segment at B0000h.

CAXS (0Fh) *Default is always the slot bus.
Bits 6-7 - segment at CC000h.
Bits 4-5 - segment at C8000h.
Bits 2-3 - segment at C4000h.
Bits 0-1 - segment at C0000h.

DAXS (10h) *Default is always the slot bus.
Bits 6-7 - segment at DC000h.
Bits 4-5 - segment at D8000h.
Bits 2-3 - segment at D4000h.
Bits 0-1 - segment at D0000h.

EAXS (11h) *Default may be on-board BIOS ROM access or slot bus access.
This memory space is a special case in that "default" can be one of two locations depending on the state of the RAMSET bit 7.
Bits 6-7 - segment at EC000h.
Bits 4-5 - segment at E8000h.
Bits 2-3 - segment at E4000h.
Bits 0-1 - segment at E0000h.

FAXS (12h) *Default is always on-board BIOS ROM access.
Bits 6-7 - segment at FC000h.
Bits 4-5 - segment at F8000h.
Bits 2-3 - segment at F4000h.
Bits 0-1 - segment at F0000h.

SLEEP (13h) (Default = 01h)
Bit 7 - Power-down enable.

0 = Default operational setting. Normal clock speed.
1 = Invokes clock divider set in bits 4 through 6.

This bit is reset to 0 and normal operation resumes when rewritten or when the VL82C320 receives a hardware reset.

Bits 6-4 - Power-down CLK2 divider. These bits provide a code used to divide the CLK2 down for sleep mode. The codes are:
000 = ÷1 (Default /1 clock)
001 = ÷4
010 = ÷8
011 = ÷16
100 = ÷32
101 = ÷64
110 = ÷256
111 = ÷1024

Bit 1 - External Control 1
Bit 1 along with Bit 7 control the –SLP/MISS pin.

Bit 0 is a simple latch that provides no functionality in the VL82C320. However, a read always reflects the last write to this bit.

MISCSET (14h) (Default = 06h)
Bit 7 is used to enable or disable the SF options mapped into the coprocessor chip set I/O space between F0h and FFh.
0 = enabled (Default)
1 = disabled

Bit 6 controls coprocessor software reset.
0 = enabled (Default)
1 = disabled

Bit 5 is SD high drive enable.
0 = 24 mA drive (Default)
1 = 12 mA drive

Bits 4-3 specify the CLK2 divider that is invoked when the TURBO input pin is low or when a write to port F4h is performed.
00 = CLK2 ÷1 (Default)
01 = CLK2 ÷2
10 = CLK2 ÷3
11 = CLK2 ÷4

Bits 2-1 are the value used for division of TCLK2 or BUSOSC to generate BUSCLK.
00 = ÷ 1
01 = ÷ 2
10 = ÷ 3
11 = ÷ 4 (Default)

Bit 0 indicates the BUSCLK divider source.
0 = TCLK2 (Default)
1 = BUSOSC

TEST (15h) (Default = 00h)
This register is reserved for "to be determined" factory test functions. It must never be written during normal operation.

CTRL1(16h) (Default = 00h)
This register contains additional system functional controls.

Bit 7 provides for disk controller compatibility. With fast CPUs, some disks can be overrun by programmed I/O. This bit provides a way to compensate by forcing the first memory cycle after an I/O cycle to be executed at non-turbo speed.
0 = slow programmed I/O (Default)
1 = normal programmed I/O

Bit 6 selects the sleep mode refresh option.
0 = CAS before RAS refresh
1 = normal refresh

Bits 5-4 are used to open a 64K or 128K window at the top of DOS memory for access by slot bus cards. This allows accesses to be directed off-board in this region, then come back on-board in order to access on-board extended memory. The slot pointer (SLTPTR) cannot be used to provide this function because all accesses above slot pointer are off-board. There is no way to gain access to on-board memory above this pointer except through the EMS hardware. These bits affect only the CPU address space from 512K-640K.

00 - 512K-640K on-board access
10 - 576K-640K accesses slot bus
512K-576K on-board accesses
11 - 512K-640K accesses slot bus

Special cases: This feature is inactive when EMS backfill is enabled. An attempt to set a code other than 00b with EMS backfill enabled will fail to change the code. If this feature is activated with codes 1Xb and EMS backfill is later activated, the code will automatically change to 00b disabling slot bus accesses in this region.

Use of SLTPTR in the same range is totally compatible. SLTPTR rules. If SLTPTR=576K or 512K, the setting of CTRL1 bits 5-4 doesn't matter. Accesses will be directed to the slot bus in this region and will also remain off-board above 640K.

Bit 2 programs the drive current on outputs RASBK3-RASBK0
0 = 24 mA (Default)
1 = 12 mA

Bit 1 is read/write and reserved for future use. Do not write 1's to these bits.

Bit 0 will also be used for this future circuit but it also controls a function in this version of the VL82C320.

Bit 0 - –SLP/MISS pin
0 = –SLP (Default)
1 = MISS input

TABLE 14. INDEXED CONFIGURATION REGISTER MAP

Index Port	D7	D6	D5	D4	D3	D2	D1	D0
ECh (R/W)	A7	A6	A5	A4	A3	A2	A1	A0

	Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
00	VER (R-O)	1	1	1	0	0	0	0	0
01	COMPAT	1	1	1	1	1	1	1	1
02	SLTPTR	A23	A22	A21	A20	A19	A18	A17	A16
03	RAMMAP	ROMSLOT	1	1	DRAM Memory Map Code				
04	RAMMOV	1	1	1	1	RASBK - CAS Swap Code			
05	RAMSET	DRAM Drive		ESTART	1	Page Md A	Page Md B	Bank A Int	Bank B Int
06	REFCTL	Decup	Slow Refresh Divider - System Board			10/16 IO	Slow Refresh Divider - Slots		
07	RASTMA	RAS ADDSEL	tRCD	1	tRP		tRAS		
08	CASTMA	tCASW		tCST	tCP		1	tCASR	
09	RASTMB	RAS ADDSEL	tRCD	1	tRP		tRAS		
0A	CASTMB	tCASW		tCST	tCP		1	tCASR	
0B	EMSEN1	EMS Enable	BF Enable	Reserved	EMSMAP	B/EC000	B/E8000	B/E4000	B/E0000
0C	EMSEN2	DC000	D8000	D4000	D0000	A/CC000	A/C8000	A/C4000	A/C0000
0D	AAXS	AC000 Access		A8000 Access		A4000 Access		A0000 Access	
0E	BAXS	BC000 Access		B8000 Access		B4000 Access		B0000 Access	
0F	CAXS	CC000 Access		C8000 Access		C4000 Access		C0000 Access	
10	DAXS	DC000 Access		D8000 Access		D4000 Access		D0000 Access	
11	EAXS	EC000 Access		E8000 Access		E4000 Access		E0000 Access	
12	FAXS	FC000 Access		F8000 Access		F4000 Access		F0000 Access	
13	SLEEP	Enable	Power Down CLK2 Divider			Ext Ctrl 3	Ext Ctrl 2	Ext Ctrl 1	SYSCLK
14	MISCSET	FX Enable	F1 Ctrl	High Drive	Slow CLK2 Divider		Slot Bus Divider		Bus Mode
15	TEST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
16	CTRL1	DSKTMG	SLPREF	512-640K Access		Reserved	RASDRV	Reserved	PRESNT

Note: A 1 indicates currently unused bits that read back as logic 1. It is recommended that they be written as a "1" to ensure future compatibility.

TABLE 15. DEFAULT CONFIGURATION VALUES AFTER RESET

Data Port EDh (R/W)		D7	D6	D5	D4	D3	D2	D1	D0
00	VER (R-O)	1R	1R	1R	0R	0R	0R	0R	0R
01	COMPAT	1R	1R	1R	1R	1R	1R	1R	1R
02	SLTPTR	1	1	1	1	1	1	1	1
03	RAMMAP	1	1R	1R	0	0	0	0	0
04	RAMMOV	1R	1R	1R	1R	0	0	0	0
05	RAMSET	0	0	1	1R	1	1	0	0
06	REFCTL	0	0	0	0	0	0	0	0
07	RASTMA	1	1	1R	1	1	1	1	1
08	CASTMA	1	0	1	1	0	1R	1	1
09	RASTMB	1	1	1R	1	1	1	1	1
0A	CASTMB	1	0	1	1	0	1R	1	1
0B	EMSEN1	0	0	0	0	0	0	0	0
0C	EMSEN2	0	0	0	0	0	0	0	0
0D	AAXS	0	0	0	0	0	0	0	0
0E	BAXS	0	0	0	0	0	0	0	0
0F	CAXS	0	0	0	0	0	0	0	0
10	DAXS	0	0	0	0	0	0	0	0
11	EAXS	0	0	0	0	0	0	0	0
12	FAXS	0	0	0	0	0	0	0	0
13	SLEEP	0	0	0	0	0	0	0	1
14	MISCSET	0	0	0	0	0	1	1	0
15	TEST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
16	CTRL1	0	0	0	0	0	0	0	0

Note: Values followed by "R" are read-only and have no logical function. Reserved bits in the Test register are for factory test.

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
t1	TCLK2 Period	25		ns	
t2	TCLK2 High Time	8		ns	1.5 V
t3	TCLK2 Low Time	8		ns	1.5 V
t4	BUSOSC Period	20		ns	
t5	BUSOSC, OSC High Time	8		ns	1.5 V
t6	BUSOSC, OSC Low Time	8		ns	1.5 V
t7	CLK2IN High Time	8		ns	2.0 V
t8	CLK2IN Low Time	8		ns	2.0 V
tD9	TCLK2 to CLK2 Delay		25	ns	CL=50 pF
t10	CLK2 Fall Time		4	ns	3.6 V to 1.0 V @ CL=50
t11	CLK2 Rise Time		4	ns	1.0 V to 3.6 V @ CL=50
tD12	TCLK2 to BUSCLK Delay		25	ns	CL=50 pF
tD13	BUSOSC to BUSCLK Delay		25	ns	CL=50 pF
t14	BUSCLK Fall Time		9	ns	3.6 V to 1.0 V @ CL=50
t15	BUSCLK Rise Time		12	ns	1.0 V to 3.6 V @ CL=50
tD16	CLK2IN to RESCPU Delay	3	13	ns	CL=30 pF
tD17	CLK2IN to RESNPX Delay	3	13	ns	CL=30 pF
tD18	CLK2IN to –READYO Delay	3	19	ns	CL=30 pF
tD19	CLK2IN to HRQ Delay	3	20	ns	CL=50 pF
tSU20	–ADS to CLK2IN Setup Time	20		ns	
tH21	–ADS from CLK2IN Hold Time	4		ns	
tSU22	W/–R, M/–IO, D/–C to CLK2IN Setup Time	22		ns	
tSU22a	W/–R, M/–IO, D/–C to CLK2IN Setup Time	29		ns	
tH23	W/–R, M/–IO, D/–C from CLK2IN Hold Time	4		ns	
tSU24	A23-A1 to CLK2IN Setup Time	20		ns	
tSU25	A23-A1 to CLK2IN Setup Time	26		ns	
tH26	A23-A1 from CLK2IN Hold Time	4		ns	
tSU27	–BHE, –BLE to CLK2IN Setup Time	20		ns	
tH28	–BHE, –BLE from CLK2IN Hold Time	4		ns	
tD29	–ADS to –EALE Delay	3	17	ns	CL=200 pF
tSU30	HLDA to CLK2IN Setup Time	10		ns	
tH31	HLDA to CLK2IN Hold Time	4		ns	
tSU32	–READYIN to CLK2IN Setup Time	9		ns	
tH33	–READYIN from CLK2IN Hold Time	4		ns	
tD34	CLK2IN to –RASBK3- –RASBK0 Delay	4	20	ns	CL=150 pF
tD35	CLK2IN to –RAMW Delay	4	23	ns	CL=300 pF

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
tD36	CLK2IN to –CAS7- –CAS0 Delay	4	17	ns	CL=50 pF
tD37	CLK2IN to –BRDRAM Delay	4	20	ns	CL=50 pF
tD40	CLK2IN to –ROMCS Delay	4	22	ns	CL=50 pF
tD41	A23-A1 to MA10-MA0 Delay	4	34	ns	CL=300 pF
tD42	CLK2IN to MA10-MA0 Delay	4	25	ns	CL=300 pF
tD43	CLK2IN to MA10-MA0 Delay	4	22	ns	CL=300 pF
tD46	CLK2IN to –CHS0/–MR, –CHS1/–MW CHM/–IO Going Low Delay	3	18	ns	CL=50 pF
tD47	BUSCLK to –CHS0/–MR, –CHS1/–MW, CHM/–IO Going High Delay	3	22	ns	CL=50 pF
tSU48	–CHREADY to BUSCLK Setup Time	5		ns	
tH49	–CHREADY from BUSCLK Hold Time	3		ns	
tSU50	D15-D0 to –IOW High Setup Time	30		ns	
tH51	D15-D0 from –IOW High Hold Time	5		ns	
tD52	–IOR Low to D15-D0 Delay	5	50	ns	CL=50 pF
tD53	–IOW High to –SLP/MISS Delay	4	33	ns	CL=50 pF
tD54	A20GATE to –BLKA20 Delay	4	20	ns	CL=50 pF
tD56	–IOW or –IOR Low to –BLKA20 Delay	5	25	ns	CL=50 pF
tSU57	DMAHRQ to BUSCLK Setup Time	10		ns	
tH58	DMAHRQ from BUSCLK Hold Time	8		ns	
tD59	BUSCLK to DMAHLDA Delay	3	30	ns	CL=50 pF
tD60	CLK2IN to DMAHLDA Delay	3	26	ns	CL=50 pF
tD61	BUSCLK to –REFRESH Delay	3	32	ns	CL=200 pF
tD62	CLK2IN to –REFRESH Delay	3	32	ns	CL=200 pF
tD63	BUSCLK to –REFRESH Float Delay	3	20	ns	
tD66	–ERRORNPX Low to IRQ13 Delay	3	20	ns	CL=50 pF
tD67	–IOW Low to IRQ13 Low Delay	3	25	ns	CL=50 pF
tD68	PEREQNPX to PEREQCPU Delay	3	20	ns	CL=50 pF
tD69	–BUSYNPX High to PEREQCPU High Delay	3	20	ns	CL=50 pF
tD70	–IOW Low to PEREQCPU Low Delay	3	25	ns	CL=50 pF
tD71	–BUSYNPX to –BUSYCPU Delay	3	20	ns	CL=50 pF
tD72	–IOW Low to –BUSYCPU Delay	3	25	ns	CL=50 pF
tD73	CLK2IN to –BUSYCPU Delay	3	23	ns	CL=50 pF
tD74	CLK2IN to –NPCS Delay	3	23	ns	CL=50 pF
tSU75	RSTDRV to CLK2IN Setup Time	10		ns	
tH76	RSTDRV from CLK2IN Hold Time	5		ns	
tD77	CLK2IN to D15-D0 Driven Delay	3	25	ns	CL=50 pF

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
tD78	CLK2IN to D15-D0 Float Delay	3	20	ns	CL=50 pF
tD79	CLK2IN to PAR1-PAR0 Driven Delay	3	25	ns	CL=50 pF
tD80	CLK2IN to PAR1-PAR0 Float Delay	3	25	ns	CL=50 pF
tD81	CONTROL to SD15-SD0 Driven Delay	3	25	ns	
tD82	CONTROL to SD15-SD0 Float Delay	3	25	ns	
tD83	–XDREAD High to XD Driven Delay	3	25	ns	
tD84	–XDREAD Low to XD Float Delay	3	25	ns	
tSU85	SD7-SD0, XD7-XD0, D7-D0 to –LATLO Setup	15		ns	
tH86	SD7-SD0, XD7-XD0, D7-D0 from –LATLO Hold	5		ns	
tSU87	SD15-SD0, XD7-XD0, D15-D8 to BUSCLK Setup	8		ns	
tH88	SD15-SD0, XD7-XD0, D15-D8 from BUSCLK Hold	15		ns	
tD89	D15-D0 to SD15-SD0 Delay		30	ns	CL=200 pF
tD90	XD7-XD0 to SD15-SD0 Delay		30	ns	CL=200 pF
tD91	SD15-SD8 to SD7-SD0 Delay		30	ns	CL=200 pF
tD92	SD7-SD0 to SD15-SD8 Delay		30	ns	CL=200 pF
tD93	D15-D0 to XD7-XD0 Delay		25	ns	CL=50 pF
tD94	SD15-SD0 to XD7-XD0 Delay		25	ns	CL=50 pF
tD95	XD7-XD0 to D15-D0 Delay		25	ns	CL=50 pF
tD96	SD15-SD0 to D15-D0 Delay		25	ns	CL=50 pF
tSU97	D15-D0, PAR1-PAR0 to CLK2IN Setup	3		ns	
tD98	D15-D0, PAR1-PAR0 from CLK2IN Hold	10		ns	
tD99	CLK2IN to –PARERROR Delay	3	32	ns	CL=50 pF
tD100	D15-D0 to PAR1-PAR0 Delay	3	20	ns	CL=50 pF
	OUT1, TURBO, –RC, 286/–386SX, –TRI			ns	No AC Specs on these Pins
tSU101	–CHS0/–MW, –CHS1/–MR to CLK2IN Setup	10		ns	
tH102	–CHS0/–MW, –CHS1/–MR from CLK2IN Hold	4		ns	
tD103	–CHS0/–MW to –RAMW Delay	3	25	ns	CL=50 pF
tD104	–CHS0/–MW Low to PAR1-PAR0 Driven Delay	3	25	ns	CL=50 pF
tD105	–CHS0/–MW High to PAR1-PAR0 Float Delay	3	25	ns	CL=50 pF
tD106	SD15-SD0 to PAR1-PAR0 Delay	3	28	ns	CL=50 pF
tD107	–CHS0/–MW, –CHS1/–MR to –BRDRAM Delay	3	25	ns	CL=50 pF
tD108	A23-A1 to –BRDRAM Delay	3	42	ns	CL=50 pF
tD109	–CHS0/–MW Low to D15-D0 Driven Delay	3	25	ns	CL=50 pF
tD110	A23-A1 Valid to D15-D0 Driven Delay	3	42	ns	CL=50 pF
tD111	–CHS0/–MW High to D15-D0 Float Delay	3	25	ns	CL=50 pF
tD112	A23-A1 Invalid to D15-D0 Float Delay	3	42	ns	CL=50 pF

TIMING DIAGRAMS

FIGURE 8. CPU INTERFACE TIMING

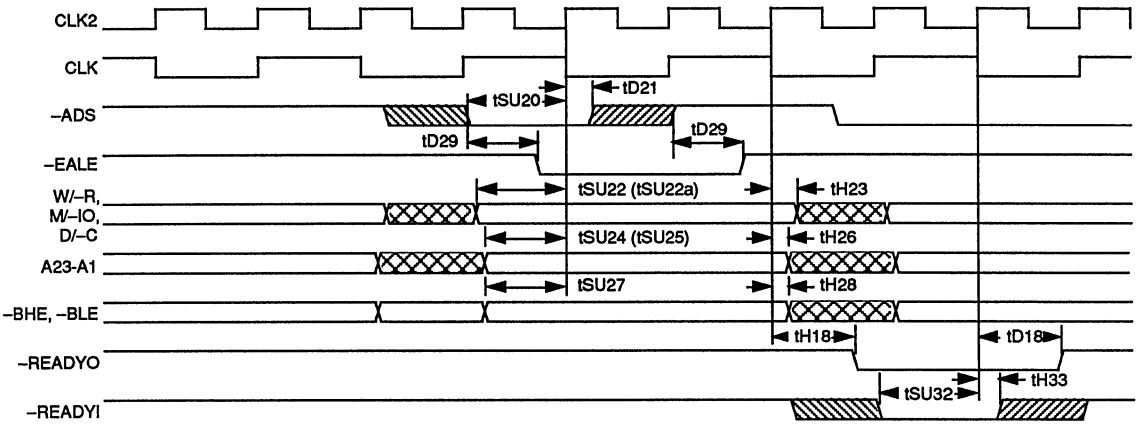


FIGURE 9. RESET AND HOLD TIMINGS

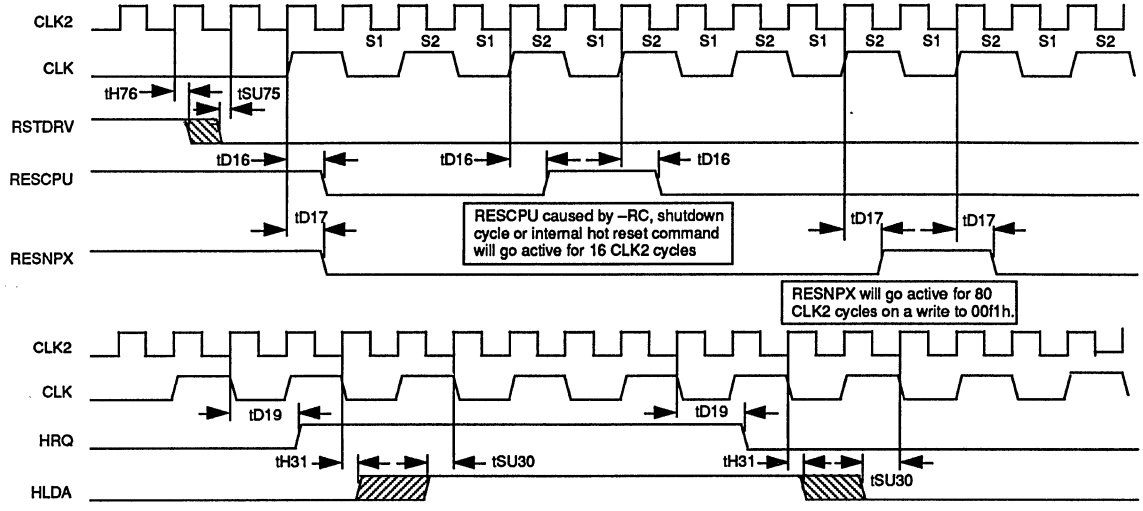


FIGURE 10. ON-BOARD MEMORY TIMING

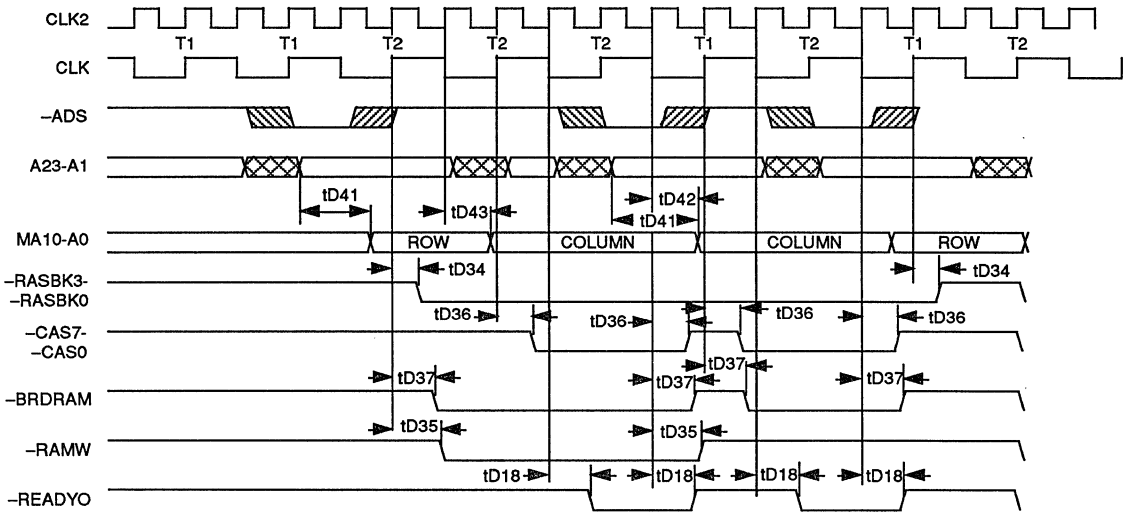


FIGURE 11. VL82C320/VL82C331 INTERFACE TIMING; A20 CONTROL TIMING

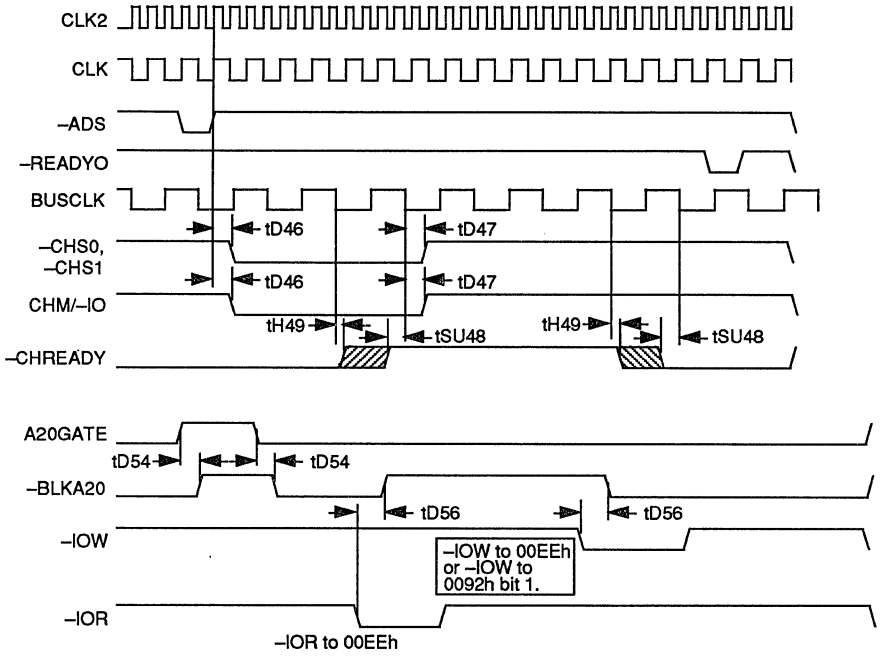


FIGURE 12. HOLD CYCLES TIMING

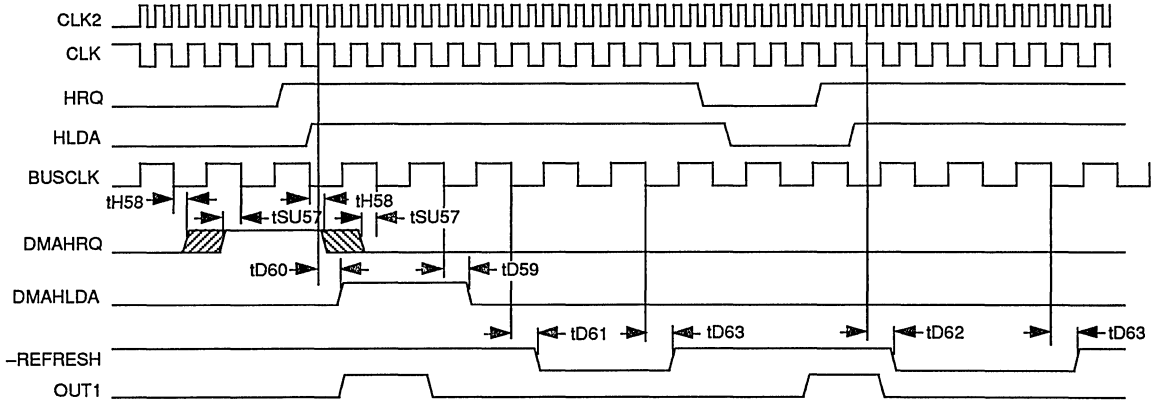


FIGURE 13. COPROCESSOR INTERFACE TIMING 386SX AND 287

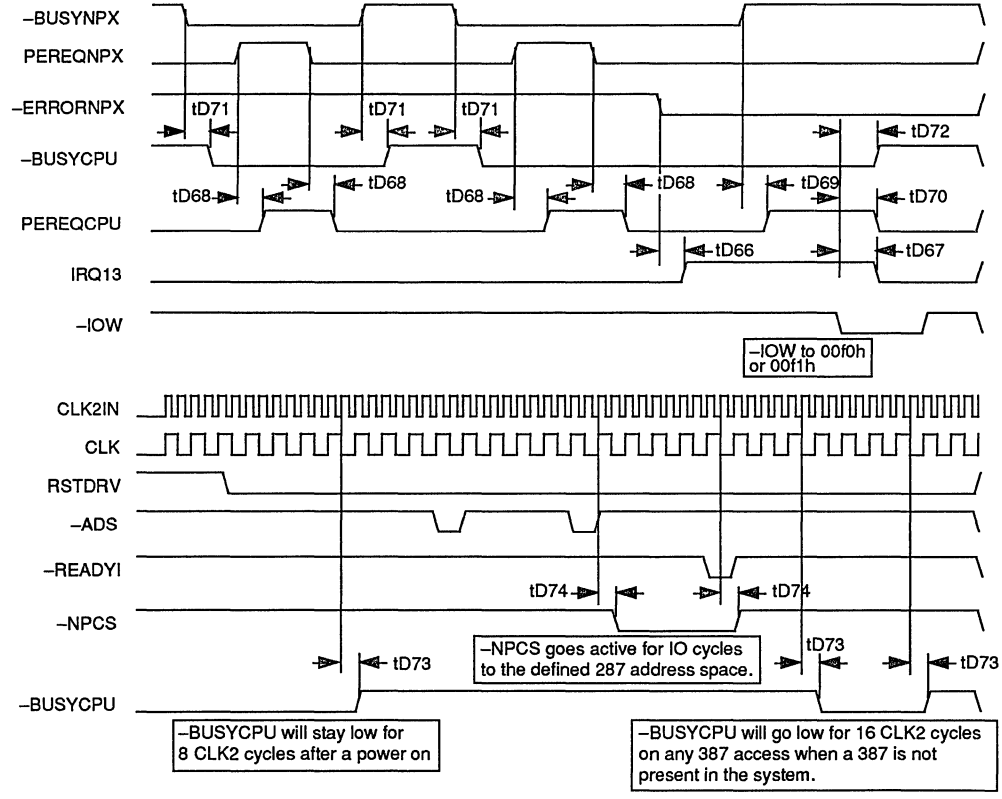
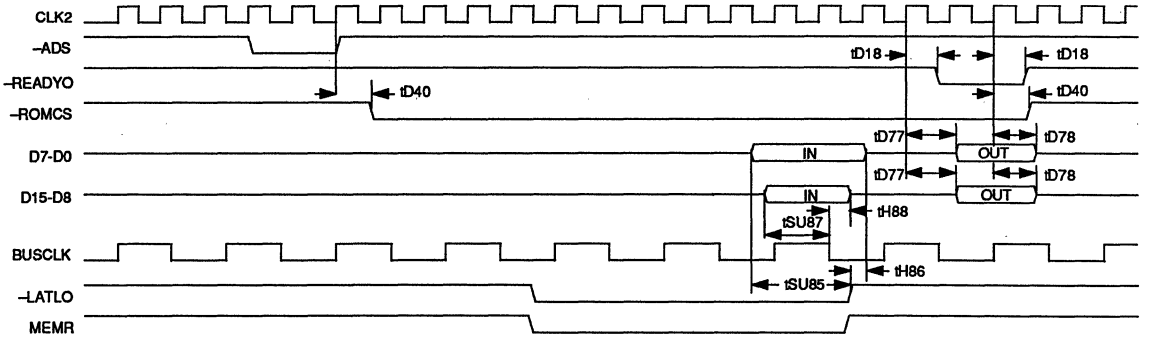


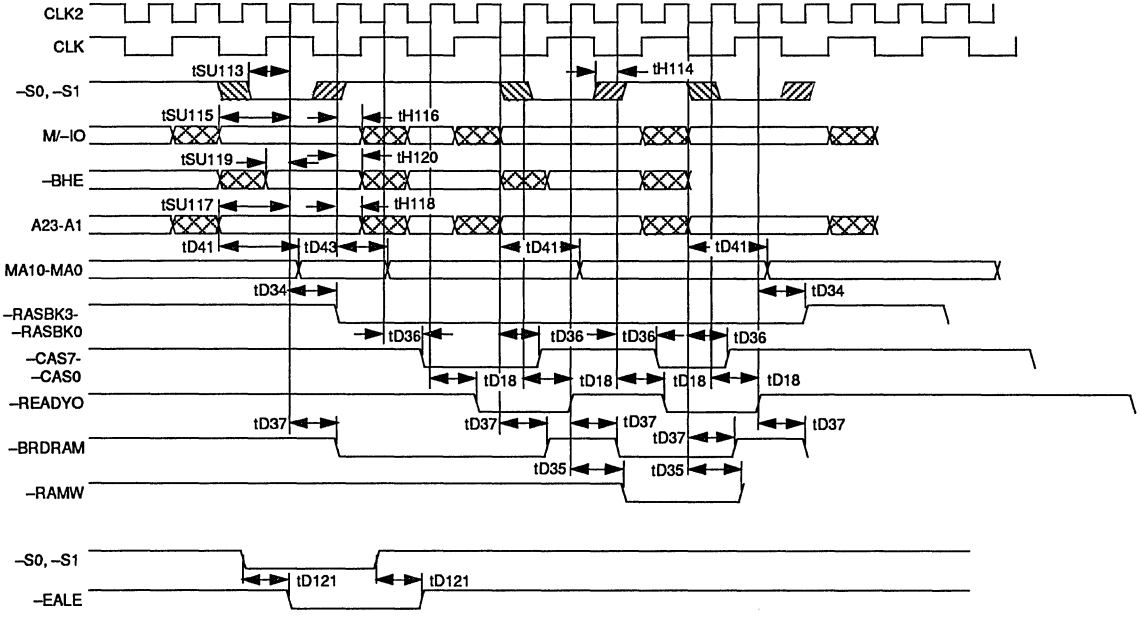
FIGURE 14. ROM CYCLE



AC CHARACTERISTICS FOR 286 MODE

Symbol	Parameter	Min	Max	Unit	Conditions
t1	TCLK2 Period	20		ns	
t7	CLK2IN High Time	8		ns	2.0 V
t8	CLK2IN Low Time	8		ns	2.0 V
tSU113	–S0, –S1 to CLK2IN Setup Time	16		ns	
tH114	–S0, –S1 from CLK2IN Hold Time	9		ns	
tSU115	M/–IO to CLK2IN Setup Time	28		ns	
tH116	M/–IO from CLK2IN Hold Time	9		ns	
tSU117	A23-A0 to CLK2IN Setup Time	28		ns	
tH118	A23-A0 to CLK2IN Hold Time	9		ns	
tSU119	–BHE to CLK2IN Setup Time	8		ns	
tH120	–BHE from CLK2IN Hold Time	9		ns	
tD121	–S0, –S1 to –EALE Delay	3	19	ns	CL=50 pF

FIGURE 15. 286 MODE TIMING



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature −10°C to +70°C

Storage Temperature −65°C to +150°C

Supply Voltage to Ground −0.5 V to VDD = 0.3 V

Applied Output Voltage −0.5 V to VDD = 0.3 V

Applied Input Voltage −0.5 V to 7.0 V

Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min.	Max.	Unit	Conditions
VIL	Input Low Voltage	−0.5	0.8	V	TTL Level Inputs
VIH	Input High Voltage	2.0	VDD +0.5	V	TTL Level Inputs
VILC	Input Low Voltage	−0.5	0.8	V	CMOS Level Inputs
VIHC	Clock Input High	VDD −0.8	VDD +0.5	V	CMOS Level Inputs
VOL1	Output Low Voltage		0.45	V	IOL = 4 mA, Note 1
VOH1	Output High Voltage	VDD −0.45	0.4	V	IOH = −1 mA, Note 1
VOL2	Output Low Voltage		0.45	V	IOL = 8 mA, Note 2
VOH2	Output High Voltage	VDD −0.45		V	IOH = −2 mA, Note 2
VOL3	Output Low Voltage		0.45	V	IOL = 20 mA, Note 3
VOH3	Output High Voltage	VDD −0.45		V	IOH = −20 mA, Note 3
VOL4	Output Low Voltage		0.45	V	IOL = 12 mA, MISCSET[5] = 1 IOL = 24 mA, MISCSET[5] = 0, Note 4
VOH4	Output High Voltage	VDD −0.45		V	IOH = −6 mA, Note 4
VOL5	Output Low Voltage		0.45	V	IOL = 12 mA, CTRL1[2] = 1 IOL = 24 mA, CTRL1[2] = 0, Note 5
VOH5	Output High Voltage	2.4		V	IOH = −6 mA, Note 5
VOL6	Output Low Voltage		0.45	V	IOL = 10 mA, RAMSET[7:6] = 00 IOL = 20 mA, RAMSET[7:6] = 01 IOL = 30 mA, RAMSET[7:6] = 10 IOL = 40 mA, RAMSET[7:6] = 11, Note 6
VOH6	Output High Voltage	2.4		V	IOH = −6 mA, RAMSET[7] = 0 IOH = −12 mA, RAMSET[7] = 1, Note 6
VOL7	Output Low Voltage		0.45	V	IOL = 8 mA, Note 7
VOL8	Output Low Voltage		0.45	V	IOL = 24 mA, Note 8
ILI	Input Leakage Current	−10	10	µA	Note 9
IIL	Input Leakage Current	−500	10	µA	Note 10
IIH	Input Leakage Current	−10	500	µA	Note 11
ILO	Output Leakage Current	−100	100	µA	

DC CHARACTERISTICS Cont.: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V Cont.

Symbol	Parameter	Min.	Max.	Unit	Conditions
IDDSB	Static Power Supply Current		3	mA	
IDDOP	Dynamic Power Supply Current		4	mA/MHz	
CI	Input or I/O Capacitance		10	pF	
CO	Output Capacitance		10	pF	

Notes:
1. Pins: –BUSYCPU, PEREQCPU, –ROMCS, IRQ13, –NPCS, –CHS0/–MW, –CHS1/–MR, CHM/–IO, –BLKA20, BUSCLK, DMAHLDA, –PARERROR, XD7-XD0
2. Pins: –READYO, HRQ, RESCPU, D15-D0, PAR1, PAR0, –CAS7- –CAS0, RESNPX, –EALE, –BRDRAM
3. Pins: CLK2
4. Pins: SD15-SD0
5. Pins: –RASBK3- –RASBK0
6. Pins: MA10-MA0, –RAMW
7. Pins –SLP/MISS
8. Pins: –REFRESH
9. All inputs except those listed in notes 10 and 11
10. Pins: –ERRORNPX, –BUSYNPX, 286/–386SX, –TRI, W/–R (–S0), D/–C (–S1), M/–IO, –ADS
11. Pins: PEREQNPX

4

NOTES:

VL82C330

SYSTEM CONTROLLER

DESCRIPTION

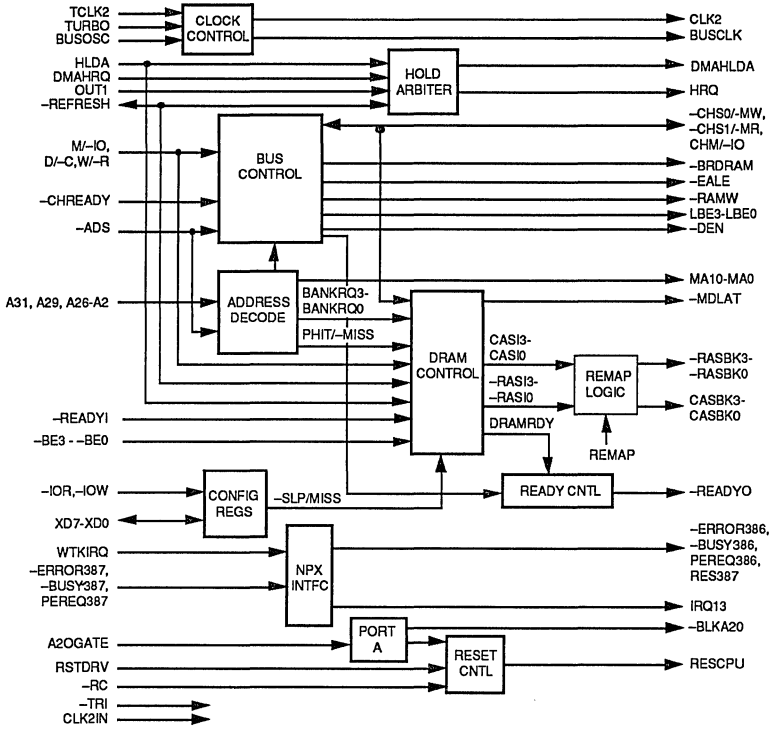
The VL82C330 System Controller is highly configurable via software. No hardware jumpers are required. Defaults on reset for the configuration registers allow the system to boot at the CPU's rated speed. However, operational capabilities are reduced until the configuration registers are set to mirror the true system configuration.

The VL82C330 is designed to perform in 386™DX systems running up to 33 MHz. Built-in page mode operation, two- or four-way interleaving and fully programmable memory timing allow the PC designer to maximize system performance using commodity DRAMs. Programmable memory timing allows the system to be setup to match the requirements of the chosen DRAMs; standard or custom.

The VL82C330 handles system board refresh directly and also controls the timing of slot bus refresh which is actually performed by the ISA Bus Controller. Refresh may be performed in coupled or decoupled mode. The former method is the standard PC/AT®-compatible mode where on- and off-board refreshes are performed synchronously. In decoupled mode, the timing of on- and off-board refreshes are independent. Both may be programmed for independent, slower than normal rates. This allows use of low power, slow refresh DRAMs. The VL82C330 controls all timing in both modes. In all cases, refreshes are staggered to minimize power supply loading and attendant noise on the VDD and ground pins.

The physical banks of DRAM can be logically reordered through one of the indexed configuration registers. This DRAM remap option is useful in order to map out bad DRAM banks allowing continued use of a system until repairs are possible. It also allows DRAM bank combinations not in the supported memory maps to be logically moved into a supported configuration without physically moving memory components. This unique, programmable function performs this task by switching the internal –RASI and CASI signals between the external –RASBK and CASBK pins. This allows internal strobes generated for DRAM bank 0, for example, to be routed to any one of the four on-board DRAM banks.

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C330-FC	Plastic Flat Pack

Note: Operating temperature range is 0°C to +70°C.

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386DX is a trademark of Intel Corp.

Active low –RASBK signals are generated to directly drive DRAM banks. Active high CASBK and LBE signals are externally decoded with NAND gates to provide 16 active low CASBK signals. This scheme provides extra timing margin and lower cost since NAND gates are cheaper and faster than equivalent OR gates.

Both the Intel 387™DX and Weitek 3167 numeric coprocessors are supported and may be used individually or in combination. Support is for both 8-bit wide and 16-bit wide system BIOS ROM.

Full EEMS support is provided in hardware for the complete full LIM EMS 4.0® standard. Seventy-two mapping registers provide a standard and an alternate set of 36 registers each. The system allows backfill to 256K for EEMS support and provides 24 mapping registers covering this space. Twelve of the 36 are page registers which cover the EMS space from C0000h to EFFFFh. These twelve registers can alternatively be mapped in the A0000-BFFFFh and D0000h-DFFFFh range by changing a configuration bit in the VL82C330. All registers are capable of translating over the complete 64 Mbyte range of on-board DRAM. Users preferring an alternate plug-in EMS solution can disable the on-board EMS system as well as system board DRAM, as required, down to 256K.

Shadowing features are supported on all 16K boundaries between 640K and 1M. EMS use, shadowed ROM, and direct system board access is possible in non-overlapping fashion throughout this memory space. Control over four access options is provided. These controls are overridden by EMS in segments for which it is enabled.

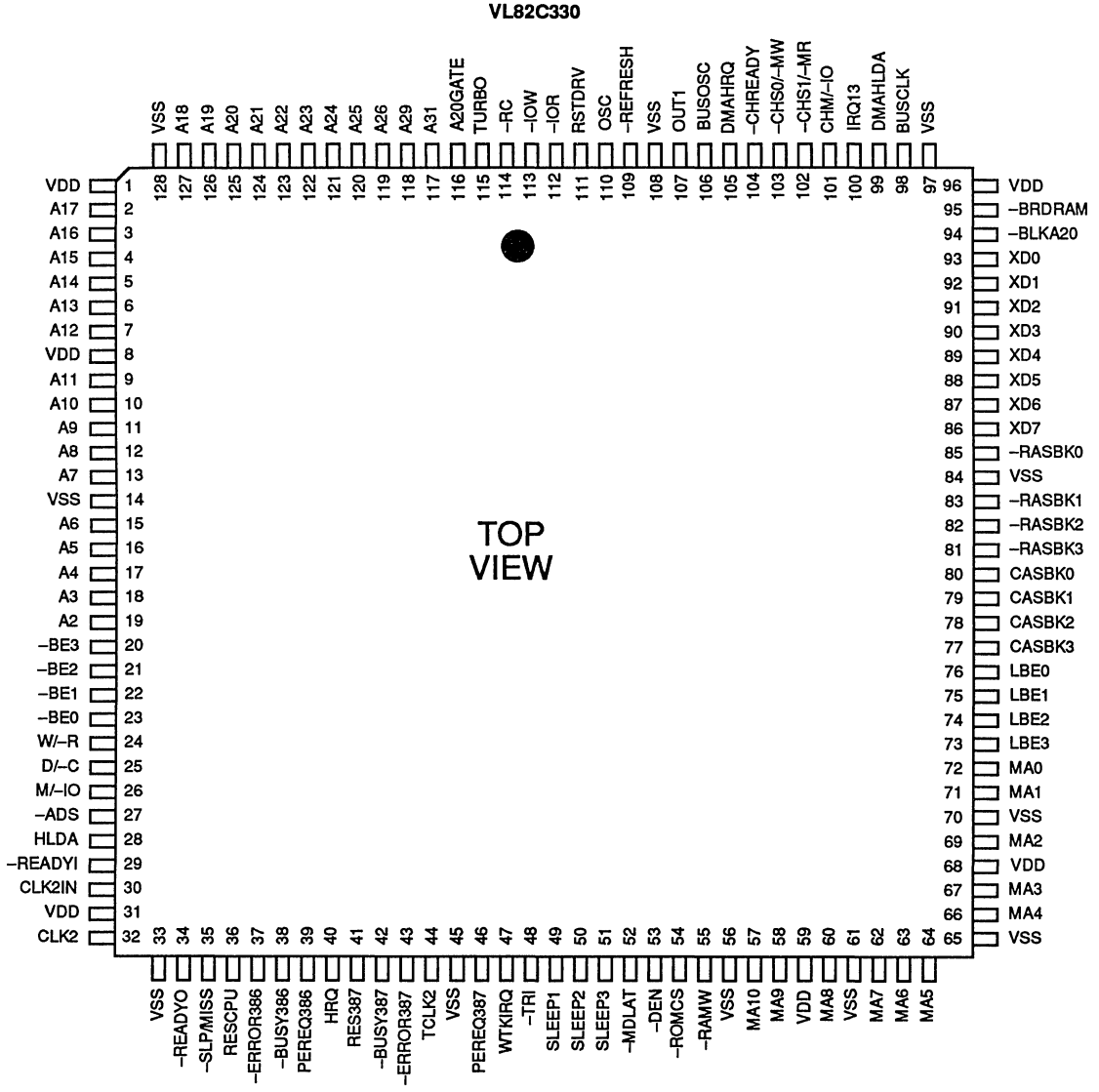
1. Access ROM or slot bus for reads and writes.
2. Access system board DRAM for reads and writes.
3. Access system board DRAM for reads and slot bus for writes.
4. Shadow setup mode. Read ROM or slot bus, write system board DRAM.

The VL82C330 is used to program the desired operational mode of the AT bus. Based on this programming, it provides the bus clock and signalling interface to the Bus Controller, which actually interfaces with the bus. The bus clock may be derived from the TCLK2 or bus OSC inputs. A programmable divider conditions the selected BUSCLK source providing divide by 1, 2, 3 or 4.

387DX is a trademark of Intel Corporation.

LIM EMS 4.0® is a registered trademark of Lotus Development Corp., Intel Corp. and Microsoft Corp.

PIN DIAGRAM


VL82C330
TOP VIEW
1 VDD
2 A17
3 A16
4 A15
5 A14
6 A13
7 A12
8 VDD
9 A11
10 A10
11 A9
12 A8
13 A7
14 VSS
15 A6
16 A5
17 A4
18 A3
19 A2
20 -BE3
21 -BE2
22 -BE1
23 -BE0
24 W/-R
25 D/-C
26 M/-IO
27 -ADS
28 HLDA
29 -READYI
30 CLK2IN
31 VDD
32 CLK2
33 VSS
34 -READYO
35 -SLP/MISS
36 RESCPU
37 -ERROR386
38 -BUSY386
39 PEREQ386
40 HRQ
41 RES387
42 -BUSY387
43 -ERROR387
44 TCLK2
45 VSS
46 PEREQ387
47 WTKIRQ
48 -TRI
49 SLEEP1
50 SLEEP2
51 SLEEP3
52 -MDLAT
53 -DEN
54 -ROMCS
55 -RAMW
56 VSS
57 MA10
58 MA9
59 VDD
60 MA8
61 VSS
62 MA7
63 MA6
64 MA5
65 VSS
66 MA4
67 MA3
68 VDD
69 MA2
70 VSS
71 MA1
72 MA0
73 LBE3
74 LBE2
75 LBE1
76 LBE0
77 CASBK3
78 CASBK2
79 CASBK1
80 CASBK0
81 -RASBK3
82 -RASBK2
83 -RASBK1
84 VSS
85 -RASBK0
86 XD7
87 XD6
88 XD5
89 XD4
90 XD3
91 XD2
92 XD1
93 XD0
94 -BLKA20
95 -BRDRAM
96 VDD
97 VSS
98 BUSCLK
99 DMAHLDA
100 IRQ13
101 CHM/-IO
102 -CHS1/-MR
103 -CHS0/-MW
104 -CHREADY
105 DMAHRQ
106 BUSOSC
107 OUT1
108 VSS
109 -REFRESH
110 OSC
111 RSTDRV
112 -IOR
113 -IOW
114 -RC
115 TURBO
116 A20GATE
117 A31
118 A29
119 A26
120 A25
121 A24
122 A23
123 A22
124 A21
125 A20
126 A19
127 A18
128 VSS

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE SIGNALS			
A31, A29, A26	117-119	I-TPU	A26 is used to prevent aliasing above 64 Mbyte. A31 and A29 are used to differentiate upper BIOS accesses, Weitek 3167 accesses, and 387DX accesses. When HLDA is active, these signals are held low internally. This is required in order to prevent errant Bus Master and DMA accesses to on-board memory.
A25-A2	120-127 2-7, 9-13, 15-19	I-TTL	Address Bits - These bits allow direct access of up to 64 Mbytes of memory.
–BE3 - –BE0	20-23	I-TTL	Byte Enables 3 through 0, active low - These signals allow 8-bit resolution during read/write accesses.
W/–R	24	I-TPU	Write or active low Read - W/–R is decoded with the remaining control signals to indicate the type of bus cycle requested.
D/–C	25	I-TPU	Data or active low Code - D/–C is decoded with the remaining control signals to indicate the type of bus cycle requested.
M/–IO	26	I-TPU	Memory or active low I/O - M/–IO is decoded with the remaining control signals to indicate the type of bus cycle requested.
–ADS	27	I-TPU	Address Strobe, active low - Indicates that the address and control signals are valid. This signal is used internally to indicate that the address and command are valid and to determine the beginning of a bus cycle.
CLK2IN	30	I-CMOS	This is the main clock input to the VL82C330 and is connected to the CLK2 signal that is output by the VL82C330. This signal is used internally to clock the VL82C330's logic.
TCLK2	44	I-CMOS	This input is connected to a crystal oscillator whose frequency is equal to two times the system frequency. The CMOS level is used to generate CLK2 output and optionally, bus clock.
CLK2	32	O	This output signal is a CMOS level converted TCLK2 signal. It is output to the CPU and other on-board logic for synchronization.
–SLP/MISS	35	IO-OD	As a "power on reset" default, this signal is an output that is equal to –SLEEP[7] • –SLEEP[1]. When configuration register CTRL[0] = 1, this pin becomes a MISS input for use with a future VLSI product.
–READYO	34	O	Ready Out, active low - This signal is an indication that the current cycle is complete. It is generated from the internal DRAM controller or the synchronized version of –CHREADY for slot bus accesses. The culmination of these ORed READY signals is sent to the CPU and is also connected to the VL82C330's –READYI input. This signal may be combined externally with other READY sources.
–READYI	29	I-TTL	Ready Input, active low - This signal indicates the current bus cycle is complete.
HLDA	28	I-TTL	Hold Acknowledge, active high - This signal is issued in response to the HRQ driven by the VL82C330. When HLDA is active, the memory control is generated from –CHS1/–MR and –CHS0/–MW.
HRQ	40	O	Hold Request, active high - Driven by the VL82C330 to the CPU, this output indicates that a bus master, such as a DMA or AT channel master, is requesting control of the bus. HRQ is a result of the DMAHRQ input or a coupled refresh cycle. It is synchronized to CLK2.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE SIGNALS (continued)			
RESCPU	36	O	Reset CPU, active high - This signal is sent to the CPU by the VL82C330. It is issued in response to the control bit for software reset located in the Port A register or a read to I/O port EFh. It is also issued in response to signals on the RSTDRV or RC inputs and in response to VL82C330 detection of a shutdown command. In all cases, it is synchronized to CLK2.
–ERROR386	37	O	Error 386, active low - On any CPU reset it is pulled low to set the 386DX to 32-bit coprocessor interface mode.
–BUSY386	38	O	Busy 386, active low - The state of –BUSY387 is always passed through to –BUSY386 indicating that the 387 is processing a command. On occurrence of an –ERROR387 signal, it is latched and held active until occurrence of a write to ports F0h, F1h, or RSTDRV.
PEREQ386	39	O	Processor Extension Request 386, active high - An output signal generated in response to a PEREQ387, which is issued by the coprocessor to the VL82C330. PEREQ386 is asserted on occurrence of –ERROR387 after –BUSY387 has gone inactive. A write to F0h returns control of the PEREQ386 signal to directly follow the PEREQ387 input.
ON-BOARD MEMORY SYSTEM INTERFACE SIGNALS			
–RAMW	55	O-TTL	RAM Write, active low - This signal is active during memory write cycles and is high at all other times.
MA10-MA0	57, 58, 60 62-64, 66, 67 69, 71, 72	O-TTL	Memory Addresses 10 through 0 - These address bits are the row and column addresses sent to on-board memory. They are buffered and multiplexed versions of the bus master addresses.
–RASBK3 - –RASBK0	81-83, 85	O	Row Address Strobe Bank 0 through 3, active low - These signals are sent to their respective RAM banks to strobe in the row address during on-board memory bus cycles. The active period for this signal is completely programmable.
CASBK3 - CASBK0	77-80	O-TTL	Column Address Strobe Bank 0 through 3 - These signals are the respective column address strobes for each of the banks. These signals are externally gated (NAND) with the LBE signals to generate the CASBK strobes for each byte of a DRAM memory bank.
LBE3-LBE0	73-76	O	Latched Byte Enable 0 through 3, active high - These signals are the latched version of the CPU's –BE3 - –BE0 signals when the CPU is bus master or is the latched version of SA1, SA0, and –BHE when the master or DMA is in control.
–REFRESH	109	IC-OD	Refresh signal, active low - This output is used by the VL82C330 to initiate an off-board DRAM refresh operation in coupled refresh mode. In decoupled mode, the Bus Controller drives refresh active to indicate to the VL82C330 that it has decoded a refresh request command and is initiating an off-board refresh cycle.
–ROMCS	54	O	ROM Chip Select - This is the on-board system BIOS ROM chip select.
COPROCESSOR SIGNALS			
PEREQ387	46	I-TPD	Coprocessor Extension Request 387, active high - This input signal is driven by the coprocessor and indicates that it needs transfer of data operands to or from memory. For PC/AT-compatibility, this signal is also gated with the internal ERROR/BUSY control logic before being output to the CPU as PEREQ386 during 387 interrupts.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
COPROCESSOR SIGNALS (continued)			
–ERROR387	43	I-TPU	Error 387, active low - An input signal from the coprocessor indicating that an error has occurred in the previous instruction. This signal is internally gated and latched with –BUSY387 to produce IRQ13.
–BUSY387	42	I-TPU	Busy 387, active low - An input signal that is driven by the coprocessor to indicate that it is currently executing a previous instruction and is not ready to accept another. This signal is decoded internally to produce IRQ13 and to control PEREQ386.
RES387	41	O	Reset 387, active high - This output is connected to the 387DX reset input. It is triggered through an internally generated system reset or via a write to port F1h. In the case of a system reset, the RESCPU signal is also activated. A write to port F1h only resets the coprocessor. A software FINIT signal must occur after an F1h generated reset before the coprocessor is reset to the same internal state that a 287™ is put into by a hardware reset alone. Optionally, the F1h reset may be disabled by setting bit 6 of MISCSET to 1.
WTKIRQ	47	I-TPD	Weitek 3167 Interrupt Request, active high.
IRQ13	100	O	Interrupt Request 13, active high - This signal is driven to the Bus Controller to indicate that an error has occurred within the coprocessor. This signal is a decode of the –BUSY387 and –ERROR387 inputs ORed with the WTKIRQ input.
BUS CONTROL SIGNALS			
–CHREADY	104	IO-CMOS	Channel Ready, active low - This signal is issued by the Bus Controller as an indication that the current channel bus cycle is complete. This signal is synchronized internally then combined with ready signals from the coprocessor and DRAM controller to form the final version of –READYO which is sent to the CPU.
–CHS0/–MW	103	IO-CMOS	Channel Select 0/Memory Write, active low - This signal is a decode of the 386DX's bus control signals and is sent to the Bus Controller. When combined with –CHS1 and CHM/–IO and decoded, the bus cycle type is defined for the Bus Controller. Activation of HLDA reverses this signal to become an input from the Bus Controller. It is then a –MEMW signal for DMA or bus master access to system memory.
–CHS1/–MR	102	I-CMOS	Channel Select 1/Memory Read, active low - This signal is a decode of the 386DX's bus control signals and is sent to the Bus Controller. When combined with –CHS0 and CHM/–IO and decoded, the bus cycle type is defined for the Bus Controller. Activation of HLDA reverses this signal to become an input from the Bus Controller. It is then a –MEMR signal for DMA or bus master access to system memory.
CHM/–IO	101	O	Channel Memory I/O - This signal is a decode of the CPU's bus control signals and is sent to the Bus Controller. When combined with –CHS0 and –CHS1 and decoded, the bus cycle type is defined for the Bus Controller. Activation of HLDA reverses this signal to become an input from the Bus Controller. It is then a –MEMR signal for the DMA or bus master to access system memory.
–BLKA20	94	O	Block A20, active low - An output driven to the Bus Controller to deactivate address bit 20. It is a decode of the A20GATE signal and Port A bit 1 indicating the dividing line of the 1 Mbyte memory boundary. Port A bit 1 may be directly written or set by a read of I/O port EEh.

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SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
BUS CONTROL SIGNALS (continued)			
BUSOSC	106	I-TTL	Bus Oscillator - This signal is supplied from an external oscillator. It is supplied to the Bus Controller when the VL82C330's internal configuration registers are set for asynchronous slot bus mode.
BUSCLK	98	O-TTL	Bus Clock - This is the source clock used by the Bus Controller to drive the slot bus. It is two times the AT bus clock (SYSCLK). It is a programmable division TCLK2 or BUSOSC.
DMAHRQ	105	I-CMOS	DMA Hold Request, active high - This signal is an input sent by the Bus Controller. It is internally synchronized by the VL82C330 before used to generate HRQ.
DMAHLDA	99	O	DMA Hold Acknowledge - An output sent to the Bus Controller that indicates that the current hold acknowledge is in response to DMAHRQ.
–BRDRAM	95	O	Board DRAM, active low - An output to indicate that on-board DRAM is being addressed.
OUT1	107	I-CMOS	Indicates a refresh request.
PERIPHERAL INTERFACE SIGNALS			
A20GATE	116	I-TTL	Address Bit 20 Enable - An input that is used internally along with Port A bit 1 to determine if A20 is passed through or forced low. It also determines the state of –BLKA20.
TURBO	115	I-TTL	Turbo, active high - This input to the VL82C330 determines the speed at which the system board operates. It is internally ANDed with a software settable latch. When high, operation is at full speed. When low, CLK2 is divided by the value coded in configuration register MISCSET. Turbo mode is active only when all TURBO requests are active.
–RC	114	I-TTL	Reset Control, active low - The falling edge of this signal causes a RESCPU signal.
SLEEP1	49	O-OD	Sleep Signal 1, active high - This pin is the logical OR of SLEEP[7] and SLEEP[1]. The pin is always active while in sleep mode but can also be controlled via software when sleep mode is inactive.
SLEEP2	50	O-OD	Sleep Signal 2, active high - This pin is the logical OR of SLEEP[7] and SLEEP[2]. The pin is always active while in sleep mode but can also be controlled via software when sleep mode is inactive.
SLEEP3	51	O-OD	Sleep Signal 3, active high - This pin is the logical OR of SLEEP[7] and SLEEP[3]. The pin is always active while in sleep mode but can also be controlled via software when sleep mode is inactive.
BUS INTERFACE SIGNALS			
XD7-XD0	86-93	IO-TTL	Peripheral Data Bus - This bus is connected to the Bus Controller and the VL82C330. It is used to transfer data to/from on-board 8-bit peripherals.
–DEN	53	O	Data Enable, active low - This signal is an output to the Data Buffer to enable data transfers on the local bus.
–IOR	112	I-TTL	I/O Read, active low - Indicates that an I/O read cycle is occurring on the bus.
–IOW	113	I-TTL	I/O Write, active low - Indicates that an I/O write cycle is occurring on the bus.
RSTDRV	111	I-TTL	Reset Drive, active high - This signal is used to reset internal logic and to derive the RES386, and RES387.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
BUS INTERFACE SIGNALS (continued)			
–MDLAT	52	O	Memory Data Bus Latch - This is an output signal to the Data Buffer. On the rising edge, the Data Buffer latches the memory data bus. –MDLAT is low anytime one of the CASBK signals is high. When low, the Data Buffer latches are transparent.
OSC	110	I-TTL	Oscillator - This is the buffered input of the external 14.318 MHz oscillator.
TEST MODE PIN			
–TRI	48	I-TPU	Three-state - This pin is used to drive all outputs to a high impedance state. When –TRI is low, all outputs and bidirectional pins are high impedance.
POWER AND GROUND PINS			
VDD	1, 8, 31, 59,	PWR	Power Connections, nominally +5 volts - These pins should each have 0.1 µF bypass capacitors.
VSS	14, 33, 45, 56, 61, 65, 70, 84, 97, 108, 128	GND	Ground Connection - 0 volts.

SIGNAL TYPE LEGEND

Signal Code	Signal Type	Signal Code	Signal Type
I-TTL	TTL level input	O	CMOS and TTL level compatible output
I-TPD	Input with 30k ohm pull-down resistor	O-OD	Open drain, output
I-TPU	Input with 30k ohm pull-up resistor	O-TTL	TTL level output
I-CMOS	CMOS level input	IO-CMOS	CMOS level input/output
IO-TTL	TTL level input/ouput	GND	Ground
IC-OD	Open drain, output or CMOS input	PWR	Power

FUNCTIONAL DESCRIPTION

DETAILED SUBSYSTEM SPECIFICATIONS

The sections that follow cover detailed operational information for the various logical groupings of VL82C330 subsystems. In most of these sections, the effect of configurable elements that can be controlled via internal I/O registers is discussed at length. Operation of the indexed I/O registers is repeated in summary form in the "Functional Summary of Indexed Registers" section. However, some lesser configurable functions are described only in that section. Do not assume that the information in that section is discussed elsewhere.

CPU INTERFACE

The VL82C330 handles the top level control interface between the synchronous local and memory data bus and the asynchronous slot data bus. It intercepts the 386DX's bus status and address signals, and decodes the bus access. It then decides whether to handle the bus request itself, or send it off to the ISA Bus Controller.

Local Bus Accesses

The VL82C330 decodes the CPU bus signals and addresses. If the decode points to on-board memory, a bank request is issued to the on-chip DRAM controller. The DRAM controller then delivers the appropriate signals to on-board memory and returns a –READYO signal. –READYO may be combined with READY signals from the coprocessor or other external devices on the D bus to form the final –READY signal driven to the CPU.

If the system includes a cache controller, the VL82C330 allows the cache controller to perform posted write cycles to on-board memory. This allows the CPU to continue with local bus cache read hits after posting a cache write through to memory. The Data Buffer latches the write data via the cache controller's posted cache write clock. The cache controller then drives the CPU control signals to the VL82C330 notifying the DRAM controller to write the data to memory.

Slot Bus Accesses

The CPU makes slot bus accesses when the VL82C330 decodes the CPU's control signals as either an I/O cycle, INTA cycle, or an off-board memory access (the latter includes ROM accesses). In this case, the VL82C330 latches and decodes the CPU's control signals and sends out bus cycle status signals to the Bus Controller. The Bus Controller handles control of the slot transfer. The CPU is prevented from executing another cycle until the slot cycle is completed. During a slot cycle, the –READY signal returned to the CPU from the VL82C330 is delayed until the Bus Controller notifies the VL82C330 that it has completed the data transfer via –CHREADY.

Other CPU Interface

Bus arbitration is handled with the VL82C330's DMAHRQ, DMAHLDA, OUT1, HRQ, and HLDA signals. When the VL82C330 receives an active DMAHRQ (DMA hold request) from the Bus Controller, it synchronizes the HRQ (hold request) signal with the CPU clock and relays it to the CPU. The CPU responds with HLDA (hold acknowledge) to the VL82C330 which then delivers DMAHLDA to the Bus Controller. When the system memory refresh timer expires, HRQ is sent to the CPU and HLDA is returned to indicate the CPU has given up the bus for refresh cycles.

Sixteen-bit transfers are handled by the Bus Controller. There is no –BS16 signal in the CPU interface. The Bus Controller decodes the –BE3- –BE0 and CPU control signals. If it detects a 32-bit read bus access to 16-bit I/O or memory, it starts an internal state machine. The state machine latches the necessary information and provides the consecutive bus cycle controls necessary to complete the 32-bit transfer. When four bytes have been delivered to the CPU's data bus, the Bus Controller notifies the VL82C330 via –CHREADY. The VL82C330 signals the CPU, which then reads its bus. For 32-bit slot bus write cycles, the Bus Controller returns –CHREADY only upon cycle completion. In this case, the CPU sees one bus cycle where there are normally two or more.

Reset control is supplied by the VL82C330. The VL82C330 contains the PS/2-compatible Port A. It contains a bit that can be set to cause a CPU reset. A second I/O address is provided to perform the same function. The latter option is supplied for Special Features compatibility. These two controls are combined with an RC (reset control) input and a RSTDRV (reset drive) hard reset to produce the synchronized RESCPU (CPU reset) delivered to the CPU. (Refer to the section "System Reset Options" for details.)

Coprocessor interface is also supplied by the VL82C330. If the system contains a coprocessor, the interface signals (–ERROR387, –BUSY387 and PEREQ387) are sent from the coprocessor to the VL82C330 and decoded to produce the proper interface signals for the CPU. This interface provides PC/AT-compatibility for use with the 387DX. This interface also supports the Weitek 3167.

BUS CONTROLLER/SYSTEM CONTROLLER INTERCHIP COMMUNICATION CHANNEL

The asynchronous interface to the ISA Bus Controller is handled by a group of signals from the VL82C330. –CHS0, –CHS1, and CHM/–IO define which type of cycle is to be excuted as in the table below.

CHM/–IO	–CHS1	–CHS0	Bus Cycle
0	0	0	–INTA
0	0	1	–IOR
0	1	0	–IOW
0	1	1	Reserved
1	0	0	–REFRESH
1	0	1	–MEMR
1	1	0	–MEMW
1	1	1	Reserved

ISA Bus Clock Control

Data Port EDh (R/W)	D7	D6	D5	D4 D3	D2 D1	D0
MISCSET (14)	FX Enable	F1 Ctrl	MBIOS	Slow CLK2 Divider	**Bus Clock Divider**	**Bus Mode**

The VL82C386 chip set is capable of supporting AT slot bus operation asynchronous with respect to the CPU clock. Though the ISA Bus Controller actually drives the slot bus, the VL82C330 is programmed for the specified mode and sources the required clock to the ISA Bus Controller. Whether synchronous or asynchronous modes, the VL82C330 synchronizes the command interface between itself and the ISA Bus Controller to BUSCLK.

BUSCLK is the AT bus clock provided to the ISA Bus Controller by the VL82C330. It runs at twice the final AT slot bus frequency. MISCSET, shown above, is one of the indexed configuration registers. The lower three bits control sourcing of BUSCLK to the ISA Bus Controller. Bit 0 sets synchronous or asynchronous mode. When set to 1, asynchronous mode is selected and the BUSOSC input is routed to the programmable divider. When set to 0, TCLK2 is output to the driver. Bits 1 and 2 of MISCSET provide for a programmable BUSCLK divider. Values of bit 1 and 2 provide for division from one to four, respectively. The programmable BUSCLK divider must be set to provide a BUSCLK of 2X the desired bus frequency. When a 16 MHz external oscillator is used, a ÷1 results in 8 MHz bus operation. Power-on reset defaults to ÷4, synchronous mode. See the section "Functional Summary of Indexed Registers" for more details.

Further programmability of bus timing is afforded by the ISA Bus Controller.

DRAM SUBSYSTEM DESCRIPTION

The VL82C330 supports up to 64 Mbyte of DRAM on the system board in four 32-bit banks. Each byte contains its own parity bit for a total of 36 bits per bank. A single bank can consist of 256K, 1M or 4M DRAMs.

The parts used in multiple banks can consist of all one DRAM type or mixtures of any two types. It is not possible to use all three types in a single system simultaneously and not all combinations of any two types are supported. The section "Page Mode/ Interleave Subsystem Overview" shows the valid options.

The VL82C330 supports four banks by providing four –RASBK signals, four CASBK signals, and four LBE lines. By applying the latter eight signals to four 74F00's, the 16 CAS lines required to drive four banks are generated.

Several configuration registers internal to the VL82C330 are used to control the memory map, DRAM timing and page mode. These features are discussed in the following sections. Since interleaving requires pairs of banks, various controls described next act on memory in bank pairs. The short hand notation Bank A is used when describing something that affects DRAM banks 0 and 1 as a set. Similarly, Bank B is used to describe DRAM banks 2 and 3 as a set.

Memory Maps

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
RAMMAP (3)	1	1	1	DRAM Memory Map Code				

The VL82C330 supports 24 memory maps and two special cases. These maps are shown in Table 1. The table shows the DRAM combinations that are addressable in each of four 32-bit memory banks. The memory column shows the total system memory available in each memory map. The RAMMAP (4-0) column indicates the hex value written in bits 0 through 4 of the RAMMAP indexed configuration register in order to select each map. It should be noted that banks 0 through 3 in Table 1 refer to the "logical" banks as internally addressed by the VL82C330. The actual system board memory banks accessed by the internal signals may differ depending on the value stored in indexed configuration register RAMMOV. See the section "DRAM Remap Options" for more details.

TABLE 1. DRAM MEMORY MAPS SUPPORTED

Bank 0	Bank 1	Bank 2	Bank 3	Memory MB	RAMMAP (4-0)
256K				(1.38) 1.00	(1F*) 0
256K	256K			(2.30) 2.00	(1E*) 1
256K	256K	256K		3.00	2
256K	256K	256K	256K	4.00	3
1M				4.00	4
256K	1M			5.00	5
256K	256K	1M		6.00	6
1M	1M			8.00	7
1M	1M	256K		9.00	8
256K	256K	1M	1M	10.00	9
1M	1M	1M		12.00	A
1M	1M	1M	1M	16.00	B
4M				16.00	C
256K	4M			17.00	D
256K	256K	4M		18.00	E
1M	4M			20.00	F
1M	1M	4M		24.00	10
4M	4M			32.00	11
4M	4M	256K		33.00	12
256K	256K	4M	4M	34.00	13
4M	4M	1M		36.00	14
1M	1M	4M	4M	40.00	15
4M	4M	4M		48.00	16
4M	4M	4M	4M	64.00	17

*1Eh and 1Fh are special case memory maps. The 384K of DRAM above 640K are accessed as extended memory. EMS and shadow RAM are unavailable in this mode. Memory map 0h allows EMS and shadowing, but no extended memory. All other memory maps can support EMS, extended, and expanded memory as desired.

DRAM Remap Options

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
RAMMOV (04)	1	1	1	1	RAS - CAS Swap Code			

The RAMMAP register described in the previous section shows 26 distinct memory maps that are available in a TOPCAT based system. Those are actually logical memory maps. The addition of the RAMMOV function provides 16 different ways to map the logical maps into the four possible physical DRAM banks. The combination of these two register functions provides a large number of unique ways to create a valid TOPCAT memory map. This capability provides two key features for the end user.

Easier DRAM Memory Upgrades

The physical DRAM banks need not be populated in the same order as would normally be dictated by the RAMMAP options alone. One example of when this is useful is the case where a system with one bank of 1M DRAMs is upgraded by adding a second bank of 256K DRAMs. Without the RAMMOV feature, it would be necessary to remove the 1M DRAM bank and move it to physical bank 1 then put the 256K DRAMs in physical bank 0. Using RAMMOV allows the 1M DRAMs to be left in place. The 256K DRAMs may be placed in any of the three available physical DRAM banks remaining. The proper RAMMOV code is then programmed so that the logical memory map (RAMMAP=5h) is correctly routed to the proper physical DRAM devices.

DRAM Error Recovery

In case of a partial or total DRAM bank failure, the remaining functional DRAMs can be switched into an alternate, valid logical memory map by reprogramming RAMMOV and RAMMAP together.

Table 2 shows the sixteen logical to physical mappings that are available. In the top row of this chart, the numbers 3,2,1 and 0 directly under "DRAM BANK MAPPING" refer to the four physical DRAM memory banks. In the sixteen rows beneath, the code that must be programmed into the RAMMOV register bits 4-0 is shown on the left side of the chart. On the right side is shown the logical bank that is mapped to the corresponding physical bank shown in the top row.

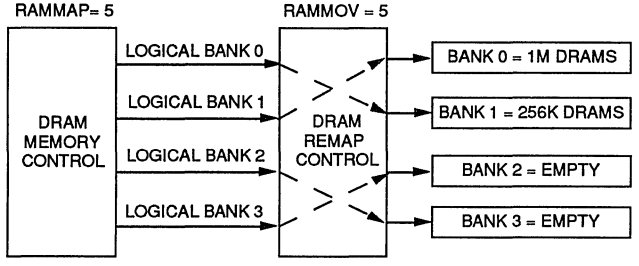
As an example, consider RAMMOV code 0001b shown in Table 2. Accesses to logical bank 3 are directed to physical bank 3. Accesses to logical bank 0 are directed to physical bank 2. Accesses to logical bank 2 are directed to physical bank 1. Accesses to logical bank 1 are directed to physical bank 0.

Note that when RAMMOV = 0000b, the default condition, the logical banks are directed to the same physical bank numbers.

TABLE 2. REMAP CONFIGURATION REGISTER CODE

RAMMOV Code				DRAM Bank Mapping				
D3	D2	D1	D0	3	2	1	0	Physical DRAM Banks
0	0	0	0	3	2	1	0	
0	0	0	1	3	0	2	1	
0	0	1	0	3	1	2	0	
0	0	1	1	3	0	1	2	
0	1	0	0	3	1	0	2	
0	1	0	1	2	3	0	1	
0	1	1	0	2	1	0	3	
0	1	1	1	2	0	1	3	Logical DRAM Banks
1	0	0	0	1	3	2	0	
1	0	0	1	1	2	3	0	
1	0	1	0	1	0	2	3	
1	0	1	1	0	3	2	1	
1	1	0	0	0	2	3	1	
1	1	0	1	0	2	1	3	
1	1	1	0	0	1	3	2	
1	1	1	1	0	1	2	3	

EXAMPLE: UPGRADING FROM ONE 1M DRAM BANK TO ONE 1M AND ONE 256K BANK



Page Mode/Interleave Subsystem Overview

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
RAMSET (05)	DRAM Drive		ESTART	1	Page Mode A	Page Mode B	Bank A Int	Bank B Int

In order to raise performance and decrease system cost, both page mode and interleave operation are available on the system board DRAM. Options are selected by programming of RAMSET and RAMMAP configuration registers. Page mode is enabled or disabled for each pair of DRAM banks independently. When on, it is active on all memory maps for the enabled bank pairs. Interleaving requires pairs of banks. Detailed operation of each is given in the following sections.

Interleave Operation

Two-way interleaving is automatically enabled whenever both banks of a pair are populated with like DRAM types. If all four banks are populated with like DRAMs, four-way interleaving automatically occurs if both bank pairs are programmed to interleave on the same bit. If not, two-way interleaving occurs. If the four banks are not populated with like DRAMs, two-way interleaving occurs on pairs that are of the same type. In a machine with three banks populated, the first two banks two-way interleave if they are of the same type. The third does not interleave. Table 3 shows the automatic interleaving options that occur versus the number of populated banks. All combinations not shown are unsupported. Table 3 also shows that 0, 1, 2, and 3 are the designations for each of the four DRAM banks. In the columns below these designators, "Yes" or "No", indicate whether the bank is populated. There is no configuration register programmability for enabling the interleave mode. All interleaving options (none, two-way, or four-way) occur automatically as the result of the memory map programmed into RAMMAP.

While the use of interleave is automatic and not programmable via the configuration registers, it is possible to select which bit is used for interleaving. Configuration register RAMSET bit 1 programs the Bank A interleave and bit 0 programs the Bank B interleave.

TABLE 3. AUTOMATIC INTERLEAVE VS MEMORY MAP

Bank 0	Bank 1	A Bank Address Mode	Bank 2	Bank 3	B Bank Address Mode
Yes	No	Linear	No	No	N/A
Yes	Yes	2-Way Interleave	No	No	N/A
Yes	Yes	2-Way Interleave	Yes	No	Linear
Yes	Yes	2-Way Interleave 0 and 1*	Yes	Yes	2-Way Interleave 2 and 3*

*This is for the case where Banks A and B contain different types of DRAMs. For memory maps 05h, 0Bh, and 17h, all four banks contain the same DRAM type and four-way interleaving is used if both bank pairs interleave on the same bit.

When set to 0, interleave occurs on bit 2. This is called "word interleaving". When set to 1, interleave occurs on bit 11 regardless of DRAM types used. This is called "block interleaving". When all four DRAM banks are populated with like part types and bit 0 and bit 1 are set differently, two-way interleaving occurs. When they are the same, four-way interleaving occurs.

Tables 4, 5, and 6 show how the CPU address lines are used to accomplish the interleave options possible with the three supported DRAM types. The top portion of each table shows the CPU address lines that are strobed onto MA0-MA10 by CASBK, the column address strobe. The middle portion of each table shows the CPU address lines strobed onto MA0-MA10 by –RASBK, the row address strobe. The bank select box shows the CPU address bit(s) used for interleaving. The bank enable decodes further qualify whether the CPU address is in the range of current memory map.

Page Mode Operation

Interleaving operates independently of page mode. Once the desired interleave bits are set, the remaining interleave modes are automatically selected by the programmed memory map. Page-mode control is given by two configuration register bits in the RAMSET register. Bit 3 = 1 enables page-mode operation on DRAM banks 0 and 1. Bit 2 = 1 enables page-mode operation on banks 2 and 3.

When activated for a bank pair, page mode is active whether one bank or both are populated. When four-way interleaving is active it is possible to have page mode active on either, neither, or both DRAM bank pairs. This does not impact the automatic interleaving, though it impacts performance.

When pairs of banks are installed, interleaving is automatically enabled. The combination of page mode with interleaving results in the best possible combination of fast system memory operation using the most cost effective DRAMs. When accesses interleaved between banks occur, CASBK precharging of the next bank to be accessed occurs while CASBK is active on the current bank. This has the effect of multiplying the effective page size by the number of banks being interleaved, thus increasing the odds of page hit cycles.

TABLE 4. 256K DRAM INTERLEAVE MAPPING

	No Interleave	2-Way Block	2-Way Word	4-Way Block	4-Way Word	Memory Address
Column Address	4	4	4	4	4	0
	5	5	5	5	5	1
	6	6	6	6	6	2
	7	7	7	7	7	3
	8	8	8	8	8	4
	9	9	9	9	9	5
	10	10	10	10	10	6
	2	2	11	2	11	7
	3	3	3	3	12	8
	–	–	–	–	–	9
	–	–	–	–	–	10
Row Address	19	19	19	19	19	0
	18	18	18	18	18	1
	17	17	17	17	17	2
	16	16	16	16	16	3
	15	15	15	15	15	4
	14	14	14	14	14	5
	13	13	13	13	13	6
	12	12	12	21	21	7
	11	20	20	20	20	8
	–	–	–	–	–	9
	–	–	–	–	–	10
Interleave Bits	–	11	2	11	2	
	–	–	–	12	3	
Bank Enable Decodes	20	–	–	–	–	
	21	21	21	–	–	
	22	22	22	22	22	
	23	23	23	23	23	
	24	24	24	24	24	
	25	25	25	25	25	

Note: For tthe 256K options:
CA[10]=A13 for RAMMAP=13; A12 for all others.
CA[9]=A11 for RAMMAP=9, 13; A10 for all others.
RA[10]=A24 for RAMMAP=D, E; A23 for all others.
RA[9]=A22 for RAMMAP=5, 6; A21 for all others.

TABLE 5. 1M DRAM INTERLEAVE MAPPING

	No Interleave	2-Way Block	2-Way Word	4-Way Block	4-Way Word	Memory Address
Column Address	4	4	4	4	4	0
	5	5	5	5	5	1
	6	6	6	6	6	2
	7	7	7	7	7	3
	8	8	8	8	8	4
	9	9	9	9	9	5
	10	10	10	10	10	6
	2	2	11	2	11	7
	3	3	3	3	12	8
	11	12	12	13	13	9
	–	–	–	–	–	10
Row Address	19	19	19	19	19	0
	18	18	18	18	18	1
	17	17	17	17	17	2
	16	16	16	16	16	3
	15	15	15	15	15	4
	14	14	14	14	14	5
	13	13	13	23	23	6
	12	21	21	21	21	7
	20	20	20	20	20	8
	21	22	22	22	22	9
	–	–	–	–	–	10
Interleave Bits	–	11	2	11	2	
	–	–	–	12	3	
Bank Enable Decodes	22	–	–	–	–	
	23	23	23	–	–	
	24	24	24	24	24	
	25	25	25	25	25	

Note: For 1 Megabyte options: CA[10]=A13 for RAMMAP=15; A112 for all others.
RA[10]=A24 for RAMMAP=F, 10; A23 for all others.

TABLE 6. 4M DRAM INTERLEAVE MAPPING

	No Interleave	2-Way Block	2-Way Word	4-Way Block	4-Way Word	Memory Address
Column Address	4	4	4	4	4	0
	5	5	5	5	5	1
	6	6	6	6	6	2
	7	7	7	7	7	3
	8	8	8	8	8	4
	9	9	9	9	9	5
	10	10	10	10	10	6
	2	2	11	2	11	7
	3	3	3	3	12	8
	11	12	12	13	13	9
	12	13	13	14	14	10
Row Address	19	19	19	19	19	0
	18	18	18	18	18	1
	17	17	17	17	17	2
	16	16	16	16	16	3
	15	15	15	15	15	4
	14	14	14	25	25	5
	13	23	23	23	23	6
	21	21	21	21	21	7
	20	20	20	20	20	8
	22	22	22	22	22	9
	23	24	24	24	24	10
Interleave Bits	–	11	2	11	2	
	–	–	–	12	3	
Bank Enable Decodes	24	–	–	–	–	
	25	25	25	–	–	

Programmable Memory Timing

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
RASTMA (07)	RAS ADDSEL	tRCD	tRP			tRAS		
CASTMA (08)	tCASW		tCST	tCP		tCASR		
RASTMB (09)	RAS ADDSEL	tRCD	tRP			tRAS		
CASTMB (0A)	tCASW		tCST	tCP		tCASR		

System board memory timing for this chip set is not specified in wait states. Instead, each of the critical DRAM timing parameters is specified as a number of programmable clock cycles. This allows virtually unlimited flexibility in matching DRAM specs to system CPU speed. The number of wait states for the system is whatever falls out of the programmed parameters. Banks A and B are programmed separately. This allows a user who later adds memory to maximize the speed advantage of faster parts when these chips are accessed. Conversely, a user can add slower parts for a cost savings without slowing down accesses to the entire memory system.

Four configurations registers are used to program the DRAM timing parameters. RASTMA allows programming of RAS ADDSEL delay, tRCD, tRP, and tRAS parameters for banks 0 and 1. RASTMB performs the same functions for banks 2 and 3.

FIGURE 2. –RASBK/CASBK TIMING MODEL

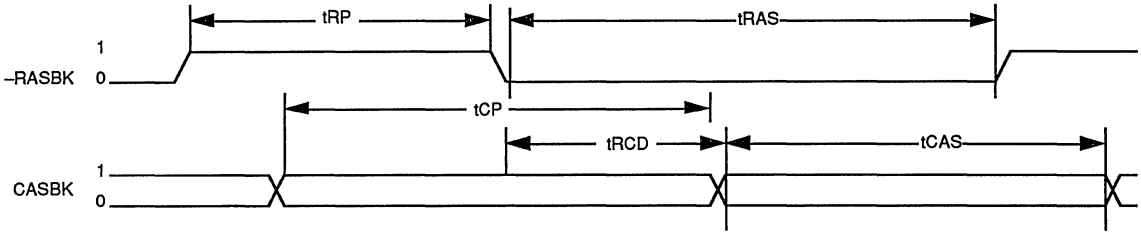
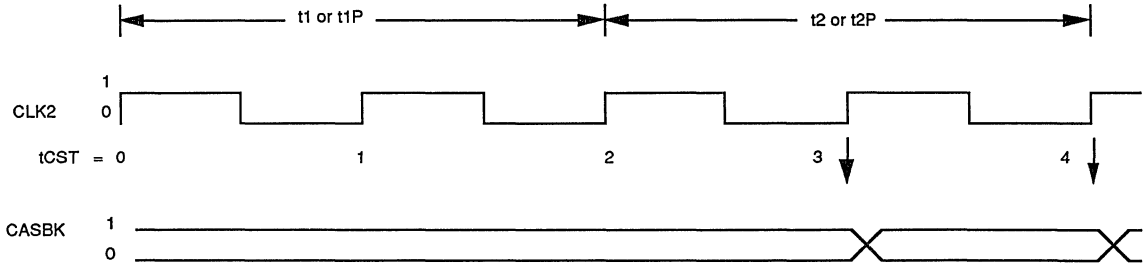
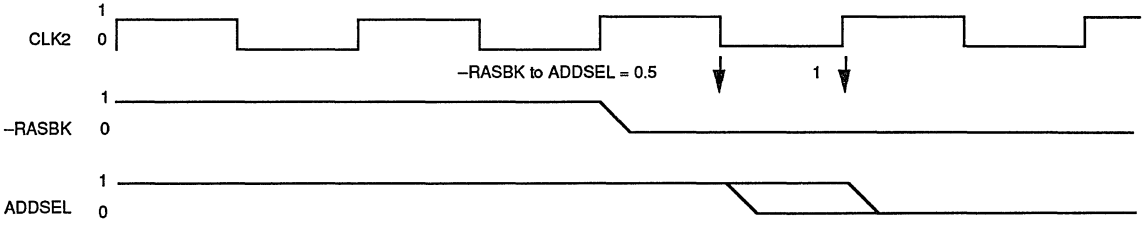


FIGURE 3. CASBK START TIME (tCST) TIMING MODEL



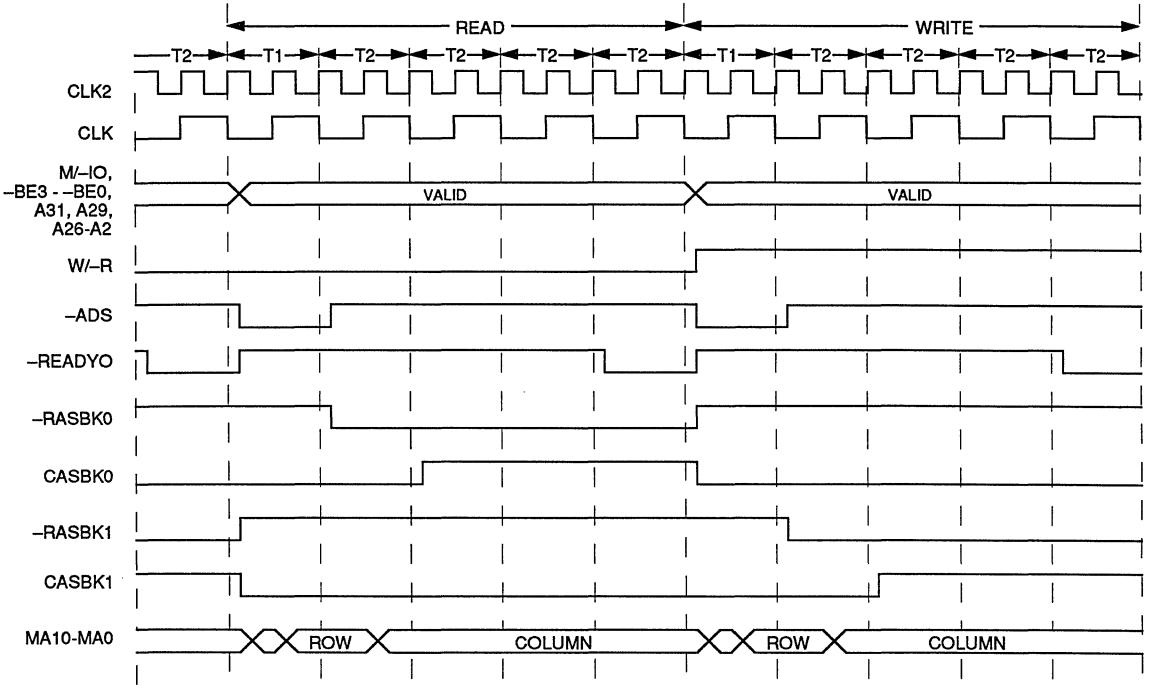
Note: tCST applies to write cycles only and always equals 3, or 4. During read cycles CASBK start time defaults to zero CLK2s if RAMSET bit 5 (ESTART) is programmed active (0) or one CLK2 if ESTART =1. This is the earliest time CASBK can start. Actual CASBK start time may be delayed due to CASBK pre-charge time or RAS to CAS delay time not yet met.

FIGURE 4. –RASBK TO ADDRESS SELECT TIMING MODEL



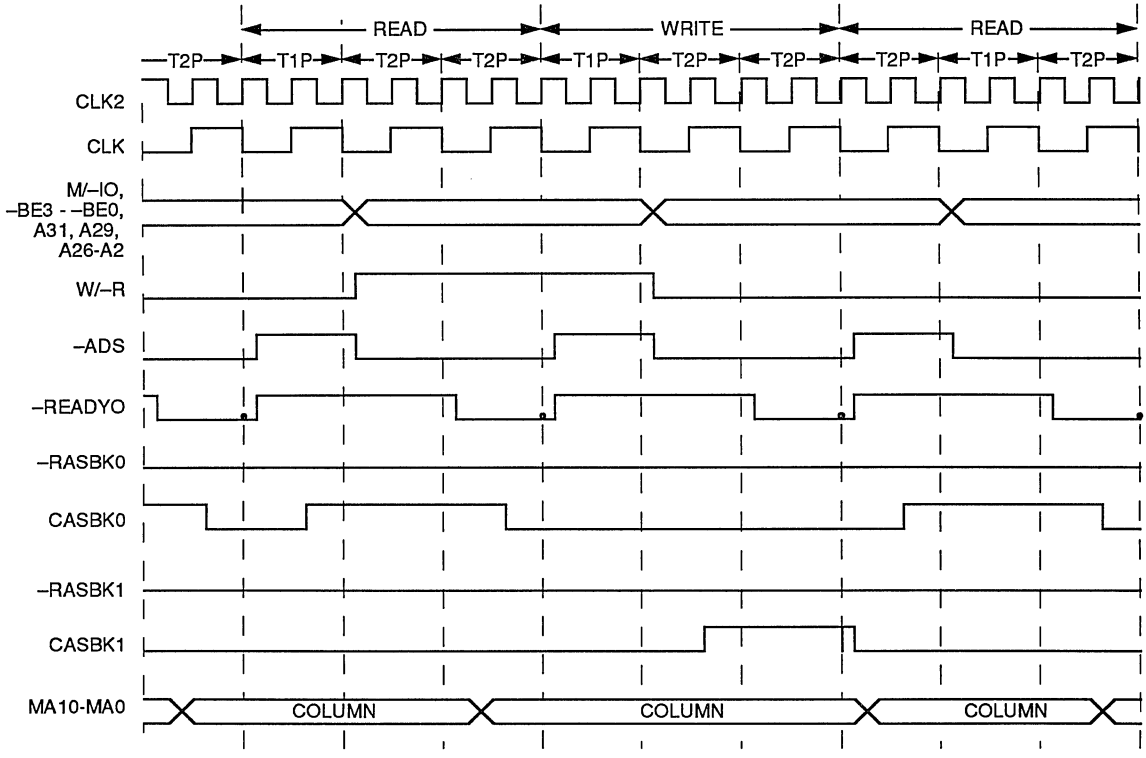
Note: Address Select can be programmed to switch MA lines 1/2 CLK2 or one CLK2 cycle after –RASBK.

FIGURE 5. NON-PAGE MODE, TWO-WAY INTERLEAVE, NON-PIPELINED



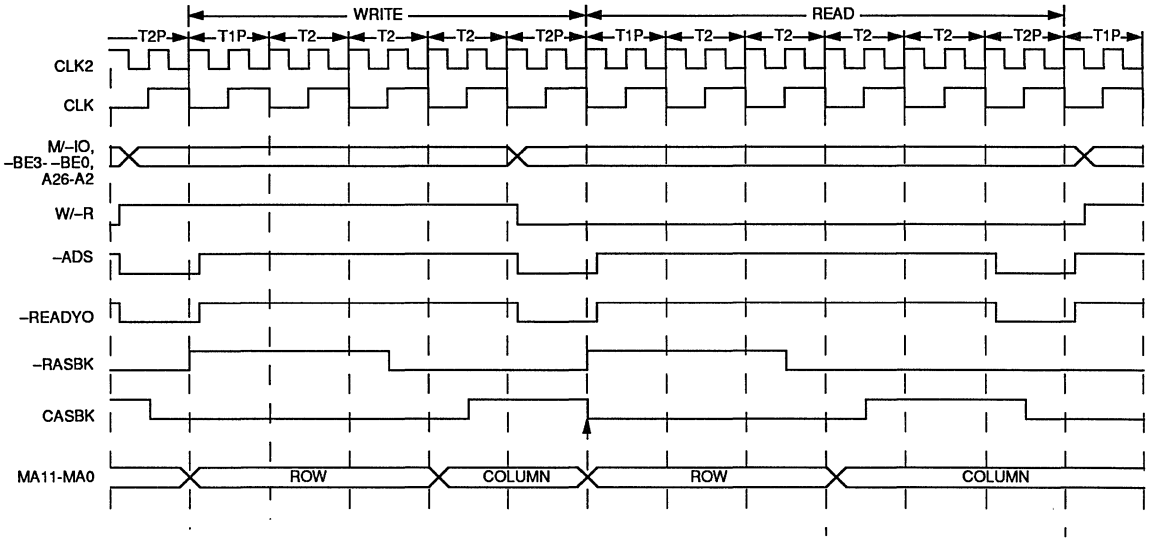
This diagram shows a read and write cycle with on-board memory on the MD bus. Signals shown are for a two-way interleaved cycle to the first two banks of system memory in non-pipelined mode. The –RASBK and CASBK signals can be shaped and moved in time in increments of CLK2 by varying the programmable timing values.

FIGURE 6. PAGEMODE, PAGE HITS, PIPELINED, TWO-WAY INTERLEAVED



This diagram shows read and write cycles for page mode, page hit operations. Two-way interleaving is shown on the first two memory banks for a pipelined cycle. The –RASBK and CASBK signals can be shaped and moved in time in increments of CLK2 by varying the programmable timing values.

FIGURE 7. DRAM BLOCK TIMING - PAGE MODE ON (PAGE MISSES)



This diagram shows a read and write cycle for page mode, page miss operations. The –RASBK and CASBK signals can be shaped and moved in time in increments of CLK2 by varying the programmable timing values.

Power-up Defaults
The DRAM system resets to a default state on power-up that allows any configuration to run, although it is a less than optimum state until BIOS or POST configures the registers with desired values. The defaults are:

- One bank of 256K DRAM
- Direct mapping from logical to physical DRAM banks
- Page mode on
- Timing for 100 ns DRAMs in 33 MHz system

Hold Request Arbiter
The hold request arbiter is used to select between the two possible sources for a hold request to the CPU. A hold request can be generated by either DMAHRQ or OUT1 going active.

At the end of a hold request from either source, the arbiter checks to see if the other source is still requesting a hold. If it is, the arbiter gives an acknowledge signal to that source and leaves the HRQ line active. This continues as long as one of the two sources is requesting a hold. Only if neither source is requesting a hold does the arbiter negate the HRQ signal and return control back to the CPU. The acknowledge to the DMA is via the VL82C330's DMAHLDA output. The acknowledge signalling for refresh is more complex due to the coupled and decoupled refresh modes. In coupled mode, an acknowledge occurs in the form of an active signal on the VL82C330's –REFRESH pin. A completely different mechanism is used in decoupled refresh mode. See the sections on "refresh" for details.

System Board DRAM Refresh
The VL82C330 performs on-board DRAM refresh and controls both on- and off-board refresh timing in all modes. Refresh may be performed in a coupled mode or decoupled mode. In coupled mode, refresh timing for both system board and slot bus refreshes is performed in a synchronous manner. In decoupled mode, the VL82C330 has complete control over the timing of on-board DRAM refresh and off-board refresh but the timing of each is independent.

Programmable Refresh Control

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
REFCTL (06)	Decup	Slow Refresh Divider-System Board			10/16 IO	Slow Refresh Divider-Slots		

When set to coupled refresh mode (D7 = 0), the VL82C330 refresh circuitry controls system board refresh and slot bus refresh in a synchronous manner. In that mode, the division specified by bits 0 to 2 applies to on- and off-board refresh and bits 4 to 6 have no effect. Only in decoupled mode (D7 = 1) do the three bits 4 to 6 of the VL82C330's REFCTL register apply. In decoupled mode, the VL82C330 refreshes the on-board DRAM independent of the Bus Controller's refresh of the slot bus resident memory. It uses the division rate specified in those bits while the slot bus refresh is performed at the rate specified by the code in bits 0 to 2. Refer to the section "Sleep Mode Control Subsystem" for the range of refresh division mapped to the three bits 0 to 2 and the three bits 4 to 6.

Coupled Refresh Control
This is the PC/AT-compatible refresh mode. If bits 0 to 2 of the REFCTL register are set to their default value of 0h, the15 µsec compatible timing is used. Other valid values, as specified in the section "Sleep Mode Control Subsystem," cause the refresh to occur at a slower rate in support of newer, low power, slow refresh DRAMs. These slower rates are all divisions of the normal 15 µsec timer provided by the Bus Controller on pin OUT1.

In sleep mode, CASBK before –RASBK refresh may be used for on-board memory. This significantly reduces power requirements. The DRAMs generate their own refresh addresses internally. Therefore, the VL82C330 is not required to drive the memory address bus during refresh. When not in sleep mode, –RASBK-only refresh mode is used.

Decoupled Refresh Control
Decoupled refresh mode provides advantages to the user. It allows system board memory and slot memory to be refreshed at different rates. This is useful if slow refresh DRAMs are used in one location and not the other. More importantly, it lowers the refresh overhead rate. System board refreshes are performed during slot bus cycles. Therefore, it is not necessary to add refresh cycles and their attendant overhead. Similarly, when the VL82C330 instructs the Bus Controller to perform a slot bus refresh, it can then allow the CPU to continue execution. Only if the CPU requires a slot bus access during this time, will refresh overhead occur.

SLTPTR - Critical Memory Control Element

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
SLOTHI (01)	1	1	1	1	1	1	A25	A24
SLOTLO (02)	A23	A22	A21	A20	A19	A18	A17	A16

The two indexed configuration registers SLOTHI and SLOTLO in combination are referred to as SLTPTR. They represent a pointer to a 64K memory boundary between 256K and 64M. Ten bits are required to specify this range. They are used to compare to address lines A16-A25. SLTPTR sets the 64K boundary above which CPU addresses are directed to the AT slot bus. Any system board memory from 1 Mbyte up to SLTPTR is accessible as on-board extended memory. Slot bus DRAM extended memory resides from SLTPTR up to 16 Mbytes. If the SLTPTR is greater than 16 Mbytes, no slot accesses are made above SLTPTR since the required address lines for this capability are not available on the slot bus in an ISA system. The VL82C330 prevents aliasing of the slot bus extended memory space for CPU addresses above 16 Mbytes.

When the on-board EMS backfill system is disabled SLTPTR can also be set below 1 Mbyte. At least one bank of 256K RAMs must be on the system board on reset for a physical memory size of 1 Mbytes. The minimum valid value for SLTPTR is 0004h to allow slot memory cards, especially EEMS capable boards, to backfill down to 256K instead of using the built-in EEMS system. However, any value between 0004h and 0009h makes the portion of system board DRAM from that address to A0000H inaccessible when the on-board EMS system is inactive. The set of valid values for slot DRAM access is 0004h-03FFh.

Exceptions to the above are SLTPTR values 000Ah through 000Fh whose access is determined by the configuration of indexed registers AAXS, BAXS, CAXS, DAXS, EAXS, and FAXS described in the "Shadow Ram Subsystem" and "Sleep Mode Control Subsystem" sections. Therefore, setting SLTPTR between 000Ah and 000Fh is treated the same as if the value were 0010h. Default = 03FFh indicates that no slot accesses occur.

Note: The slot pointer must point to 1M or higher (≥10h) if use of the EMS backfill registers is required. Pointing SLTPTR below 640K and using the backfill registers is incompatible. Therefore, any time the SLTPTR is set between 00h and 09h the EMS backfill register enable bit in configuration register EMSEN1 is cleared. A smart BIOS setup routine does not allow this condition in actual operation. See the section "Shadow Ram Subsystem" for more details. Also see the description of the additional memory control feature

TABLE 7. EFFECT OF SLTPTR WITH EMS SYSTEM ENABLED

Slot Pointer Location	Effect
256K-640K	EMS backfill register automatically disabled. EMS page registers remain operational.
	CPU addresses 0 to SLTPTR are on-board accesses.
	CPU addresses SLTPTR to 16M are slot accesses.
	On-board memory > SLTPTR = EMS page memory.
640K-1M 000Ah-000Fh	Not allowed. Respond as if Slot Pointer = 0010h. (See next case.)
1M-16M 0010h-0100h	CPU addresses 0 to 640K is system board (DOS) memory if backfill is not enabled, else 0 to 256K is system board memory.
	CPU addresses 1M to SLTPTR are system board extended memory accesses.
	CPU addresses from SLTPTR to 16M accesses slot bus, extended memory.
	EMS translation accesses system board RAM from SLTPTR to RAM top. Also system board RAM from 256 to 640K if backfill EMS is enabled.
16M-64M 0100h-03FFh	CPU addresses from 0 to SLTPTR are system board accesses.
	EMS translation accesses system board RAM from SLTPTR to RAM top. Also system board RAM from 256 to 640K if backfill EMS is enabled.

Note: Table 7 does not mention what occurs for accesses between A0000h and FFFFFh. When EMS is off, the result of CPU accesses to this memory region is determined solely by configuration of registers AAXS, BAXS, CAXS, DAXS, EAXS, and FAXS. When the EMS system is enabled, the active EMS registers between CXXXXh and EXXXXh override the settings in any areas that overlap the configurations in CAXS, DAXS, and EAXS. CPU addresses that fall in the realm of EMS register control are not directly passed to the slots or the system board. The addresses are translated and access reserved areas of system board DRAM above SLTPTR. Table 8 summarizes the rules that are followed for all cases.

EMS Subsystem

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
EMSEN1 (0B)	EMS Enable	BF Enable	Reserved	EMS MAP	B/EC000	B/E8000	B/E4000	B/E0000
EMSEN2 (0C)	DC000	D8000	D4000	D0000	A/CC000	A/C8000	A/C4000	A/C0000

The EMS system consists of 72 mapping registers. They are split into a standard and alternate set of 36 registers each. The VL82C386 chip set supports the full LIM EMS 4.0 specification with any of the valid memory maps of 1 Mbyte and higher. The alternate register set allows rapid hardware context switching. Note that the VL82C386 chip set is capable of translating addresses via the EMS registers over the entire 32 Mbyte range of possible system board memory.

The EMS system is split into two parts, the 12 EMS page registers which cover the range from C0000h to EFFFFh and the 24 backfill registers that cover 40000h to 9FFFFh. Bit D7 of configuration register EMSEN1 is a global enable for the EMS page registers. Each of the 12 registers can then be individually disabled if there are system address conflicts. Bits 0 through 7 of EMSEN2 and bits 0 through 3 of EMSEN1 provide this function. The 24 EMS backfill registers are enabled by setting bit 6 of EMSEN1. These registers are all enabled or all disabled. No individual control is provided. If a full LIM EMS 4.0 system is desired, both bits 6 and 7 of EMSEN1 are set as are the desired EMS page register enable bits.

Note that when EMS enable, bit 7 = 0, the state of BF enable, bit 6, has no effect on the system.

The normal EMS page register mapping to C0000h-EFFFFh can be altered by changing EMSEN1 bit 4 from 0 to 1. In this case, the 12 page registers map to AXXXXh, DXXXXh, and BXXXXh in that order. In this case, EMSEN1 bits 3 through 0 work to enable or disable the BXXXXh registers rather than the EXXXXh registers. Similarly, EMSEN2 bits 3 through 0 work to enable or disable the AXXXXXh registers rather than the CXXXXh registers.

When the backfill EMS registers are not used, the EMS driver allocates all memory above SLTPTR for EMS page memory. It also can use the system board memory at the same addresses as the enabled EMS page registers and any other 16K segments in the A0000h to BC000h and F0000h to FC000h areas for which the shadow code is 00b as set in configuration registers AAXS, BAXS, and FAXS. When the backfill registers are active, EMS pages can also be allocated for all system board memory from 40000h to 9FFFFh. There is no wasted DRAM in a VL82C386-based system. All memory not allocated for other purposes can be used as expanded memory.

The SLTPTR has critical effects on the EMS system. Only one effect is hardware related. When SLTPTR is set to a value from 0004h to 0009h, bit 6 of EMSEN1 is cleared. This disables the EMS backfill registers. Placement of SLTPTR is otherwise used by the EMS driver to determine the area of memory that can be allocated for use as EMS pages. Table 7 summarizes the effect of SLTPTR on the EMS system.

The EMS driver also interacts with the shadow control system through configuration registers AAXS through FAXS. Any enable EMS page registers override the shadow control in their respective 16 Kbyte ranges. System board memory at the same address range as the EMS page registers can be allocated to the EMS memory pool by the EMS driver software. In addition, other non-EMS 16K segments can be allocated to the pool if they are not shadowed or otherwise in use. This is determined by the two shadow control bits for a specific segment. When the bits are 00b, the system board memory may be allocated to the pool. Table 8 summarizes the interaction between EMS and shadow control.

TABLE 8. INTERACTION BETWEEN EMS AND SHADOW CONTROL

EMS Enable (Bit 7)	EMS Page Enable	Shadow Control		Effect
0	Don't Care	0	0	R/W slot bus or ROM chip selects.
		1	0	Read system board or write slot (shadow).
		1	1	R/W system board.
		0	1	Read slot or ROM chip selects, write system board.
1	0 (Note 1)	0	0	CPU accesses slots, EMS may access on-board DRAM.
		1	0	Shadowed, EMS does not use.
		1	1	Used by other resource, EMS driver does not allocate.
		0	1	Setup mode active. EMS driver does not allocate (Note 2).
1	1 (Note 3)	X	X	EMS overrides use of this area. CPU accesses translated by EMS. System board DRAM used by EMS memory pages.

Note 1: This case not only applies to the areas from C0000h to EFFFFh for which the EMS enable bit is turned off, but also to the A0000h to BFFFFh and F0000h to FFFFFh areas of memory.

Note 2: When an EMS driver is installed this case should not exist. A shadow setup routine uses this code. It then changes it to 10b to enable the shadow feature. However, if an EMS driver sees this code, it does not allocate the system board DRAM in this area.

Note 3: In the areas where active EMS registers reside in the CXXXXh to EXXXXh area, the control bits are overridden. Any CPU accesses to this memory space are translated and the system board memory at these addresses is allocated to the EMS page memory pool.

TABLE 9. EMS INDEX REGISTER AND DATA PORT MAP

E8h Index Port	D7	D6	D5	D4	D3	D2	D1	D0
	Set #	Auto-inc	A5	A4	A3	A2	A1	A0
	0 = Std 1 = Alt	0 = Off 1 = On						

Data Port	Page Segment	Data Port EBh								Data Port EAh							
		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	C0000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1	C4000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
2	C8000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
3	CC000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
4	D0000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
5	D4000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
6	D8000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
7	DC000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
8	E0000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
9	E4000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
A	E8000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
B	EC000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
C	40000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
D	44000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
E	48000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
F	4C000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
10	50000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
11	54000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
12	58000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
13	5C000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
14	60000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
15	64000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
16	68000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
17	6C000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
18	70000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
19	74000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1A	78000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1B	7C000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1C	80000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1D	84000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1E	88000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1F	8C000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
20	90000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
21	94000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
22	98000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
23	9C000	1	1	1	1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14

Note: A 1 indicates reserved bits that read back as logic 1.

Table 9 shows a programmer's model of the register set. The register set is accessed by writing a command byte to the index register located at I/O address E8h. Bits D0 to D5 contain the address of the desired EMS register from 0 to 35. Setting bit D6 to a 1 activates auto-increment. This feature is described in detail below. Bit D7 contains the desired register set to be accessed; the standard or the alternate set. I/O port addresses EAh and EBh then provide a window into the page register specified in the index register. Address EAh allows access to A14-A21. EBh allows access to A22-A25. Sixteen-bit I/O reads and writes can be used to gain access to A14-A25 in one operation via address EAh.

After initial accesses to port addresses at EAh and EBh, subsequent accesses are to the same page segment register until a new register number is written to the lower six bits of the index port at port address E8h or unless bit D6 of the index port was previously set to a logic 1. In this case, any access to port address EBh increments the page register number. (This new value is seen by a read to the index register port E8h.) The next read or write is to the next sequential page register. This feature allows the entire register set to be changed with a single access to the index register with either byte or word I/O access. For byte accesses, the lower byte at port address EAh must be written first. The access to the upper byte at EBh causes an auto-increment. Since all word accesses are made to port EAh, each one causes an auto-increment. This is due to the fact that the chip set actually breaks the word into two byte chunks, writing EAh followed by EBh.

The auto-increment feature speeds the already fast hardware driven context switching capability by minimizing the number of software instructions and, therefore, machine cycles required to read and save one context of the EMS registers, then retrieve and write another.

Configuration Enable/Disable

Ports 0F9h and 0FBh control access to the configuration registers. A dummy write to 0FBh enables access. A dummy write to 0F9h disables access. Since the EMS driver does not know the state of this feature when it wishes to access the configuration registers it writes 0FBh first, then writes 0F9h after its accesses are complete. This applies to all VL82C330 configuration and control registers and also to all EMS page registers discussed in this document. All such registers are mapped between I/O addresses E8h and EFh. This aids in preventing someone other than the EMS driver from inadvertently changing the EMS registers. More information on this feature is available in the "Dedicated Internal Control Registers" section.

Shadow RAM Subsystem

Data Port EDh (R/W)	D7 D6	D5 D4	D3 D2	D1 D0
AAXS	AC000 Access	A8000 Access	A4000 Access	A0000 Access
BAXS	BC000 Access	B8000 Access	B4000 Access	B0000 Access
CAXS	CC000 Access	C8000 Access	C4000 Access	C0000 Access
DAXS	DC000 Access	D8000 Access	D4000 Access	D0000 Access
EAXS	EC000 Access	E8000 Access	E4000 Access	E0000 Access
FAXS	FC000 Access	F8000 Access	F4000 Access	F0000 Access

Six indexed configuration registers are provided to give complete control over each of the 64K memory segments between 640K and 1M. The registers are called AAXS, BAXS, CAXS, DAXS, EAXS, and FAXS. Each register contains two bits for each 16K paragraph in the 64K segment controlled by that register. Refer to the section "Functional Summary of Indexed Registers" for more details.

The four modes provided are:

1. Normal PC/AT-compatible operation. This is R/W slot bus or ROM chip select depending on the memory space.
2. R/W system board DRAM. This allows complete access to DRAM in the given 16 Kbyte region.
3. Read-only DRAM. This is the normal shadow operational mode though it could be used to protect data previously written to a memory area while configured for mode 2. In this mode, writes are directed to the slot bus.
4. Shadow setup mode. In the E000 and F000 segments, reads cause on-board ROM chip selects and writes to the same address are to system board DRAM. In the segments A000 to D000 reads are from the slot bus and writes are to the system board DRAM. This allows shadowing of system board ROM as well as ROMs on a slot card.

Middle BIOS Alias Control

Data Port EDh (R/W)	D7	D6	D5	D4 D3	D2 D1	D0
MISCSET (14)	FX Enable	F1 Ctrl	MBIOS	Slow CLK2 Divider	Slot Bus Divider	Bus Mode

Bit 5 of the MISCSET indexed configuration register is used to enable the middle BIOS region (00FE0000h to 00FFFFFFFh). When the bit is a 0, this address space produces a –ROMCS. This setting is the power-on reset default. When the bit is set to logic 1, accesses to this address range are directed to the system board DRAM.

The middle and upper BIOS spaces are never shadowed.

NUMERICAL PROCESSOR INTERFACE

The VL82C330 supports both the Intel 387DX and the Weitek 3167 numeric coprocessors for use in high performance floating point math applications.

Intel 387DX

The VL82C330 contains several dedicated pins in order to provide the interface between the 387DX and the 386DX. The 386DX and 387DX are designed to interface directly without external logic. However, logic is required in order to make a system hardware compatible with the PC/AT and software compatible with the PC/AT and original IBM PC. The following sections describe the interface logic broken into several parts.

System Reset Logic

System reset is an internally generated signal caused by a reset signal to the VL82C330 (RSTDRV), usually in response to the POWERGOOD signal. This signal initiates a reset to the CPU and to the 387DX.

CPU-Only Reset Logic

A CPU reset without a coprocessor reset can occur for one of two reasons. The first is usually done in order to switch from real to protected mode. The signal which causes it is shown as "Hot" reset. It is triggered by setting bit 0 of I/O port 92h to a 1, by a read of I/O port EFh, or by receipt of an external –RC signal. The latter signal causes a CPU-only reset as soon as received. There is a 6.72 µsec delay between the occurrence of either of the first two events and activation of the RESCPU signal.

Internal detection of a shutdown command from the CPU also triggers a CPU-only reset.

In both of the above cases, reset is also synchronized to CLK2 and lasts for 16 CLK2 cycles.

387-Only Reset Logic

For PC/AT-compatibility, a 387-only reset is provided via a I/O write to F1h. This action provides a reset to the 387DX synchronized to CLK2 of 80 CLK2 cycles duration. –READYO does not go active after the write to F1h for 100 CLK2 cycles after the falling edge of RES387. There may be incompatibility with some software due to the fact that a hardware reset does not put a 387DX into the same internal state as does a reset of the 287. For this reason, the F1h reset function may be disabled by setting configuration register MISCSET[6]=1.

Error/Interrupt Logic

For PC/AT-compatibility, –ERROR387 active generates interrupt 13. It also latches –BUSY386 active. This later action is required in order to prevent the 386DX from attempting to use the coprocessor until the error handling interrupt routine is executed. The interrupt handler clears the latched –BUSY by performing a write to I/O port F0h.

Busy Logic

The –BUSY386 signal can be produced from four sources. It always occurs in response to the –BUSY387 input. It also occurs as latched by the –ERROR387 signal. In the third case, a toggle busy logic block can drive it. This block is required for compatibility with software that uses non-standard instructions to detect the presence of a coprocessor. When a coprocessor is not present, –BUSY386 is pulsed active for 16 CLK2 cycles whenever an I/O cycle is detected with A31 high.

Busy test logic is invoked only on system reset. At this time, the 386DX self-test mode is triggered. This adds 33 ms at 16 MHz and 16 ms at 33 MHz to the CPU reset time. At the end of the self-test, the BIOS can read the CPU self-test result register and perform whatever function is desired on failure. Note that when a CPU-only reset is invoked, this self-test is not performed. Therefore, "Hot" resets are performed as fast as possible.

PEREQ Logic

The PEREQ387 signal is always passed directly to the PEREQ386 pin. In addition, PEREQ386 is driven and held active as soon as –BUSY387 goes inactive after occurrence of an active –ERROR387 signal. Control of the PEREQ386 signal to follow the PEREQ387 signal is performed by a write to I/O port F0h.

387DX Ready Control

On reads or writes to the 387DX's I/O space, the VL82C330 automatically asserts –READYO to the 386DX processor after one wait state unless the –READYI line to the VL82C330 is asserted before the end of one wait state. This prevents a separate hang when a 387DX is not present.

Weitek 3167

The Weitek 3167 is a more powerful numeric coprocessor than the 387DX. It uses a superset of the 387DX pins. It is a memory mapped device and uses all 32 address lines to decode a space from C0000000h to C1FFFFFFh. The fact that it is not a standard part causes no backward compatibility issues. As such, it interfaces easily to the system. Two signals are provided on the VL82C330. WTKIRQ is used to OR this interrupt with the IRQ13 line for the 387DX. –READYI is required for any external add-in devices including a cache controller. If more than one external source of –READYI exists, they must be externally ORed.

DEDICATED INTERNAL CONTROL REGISTERS

All Special Features (SF) decodes are between E8h and FFh as shown in Table 10. While the IBM Technical Reference Manual considers F8h to FFh reserved for coprocessor use, only F8h, FAh, FCh, and FEh are actually used. SF sandwiches some registers in this region. The recommended method is to decode the F8h to FFh range then AND with address bit –A0. This properly maps only the even addresses in this range to the coprocessor. I/O ports F0h and F1h are fully decoded due to the presence of other ports at F4h and F5h. It is possible to disable the SF functions mapped in the FXh range if they conflict with a specific design implementation. This feature is described later in this specification.

Note: The dedicated I/O registers at E8h, EAh, and E9h are described separately in the "EMS Subsystem" section. The dedicated I/O registers at ECh and EDh are described in the "Functional Summary of Indexed Registers" section.

TABLE 10. DEDICATED I/O CONTROL REGISTERS

Port Address	Function
E8h	EMS Index Register
E9h	EMS Active Set
EAh	EMS Data Port Low Byte
EBh	EMS Data Port High Byte
ECh	Configuration Index Register
EDh	Configuration Data Port
EEh	Fast A20*
EFh	Fast Reset*
F0h	Coprocessor Busy Clear
F1h	Coprocessor Reset
F4h	Slow CPU**
F5h	Fast CPU**
F8h	Coprocessor
F9h	Configuration Disable**
FAh	Coprocessor
FBh	Configuration Enable**
FCh	Coprocessor
FEh	Coprocessor

* Also can be activated through port 92h for PS/2-compatibility.

** These decodes can be disabled in case of conflict.

Note: All I/O accesses to the above registers must be byte size except the EMS data port (EAh and EBh) which may be either byte or word operation.

EMS Register Set (I/O Address E9h)

E9h	D7	D6	D5	D4	D3	D2	D1	D0
EMS Register Set	1	1	1	1	1	1	1	1

A read of this address returns FFh. A read of this register also activates the standard EMS register set. A write activates the alternate EMS register set. Neither of these actions has any effect if the EMS subsystem has not been enabled by setting the EMS enable bits in the EMSEN register described in the "EMS Subsystem" and "Functional Summary of Indexed Registers" sections. Default on reset is the standard register set.

Note: This function has no relationship and is totally independent of the control afforded by bit 7 of register E8h. Bit 7 controls which register set is selected for updates to the base addresses for the EMS translation. It is possible to select and update either the standard or alternate EMS register set independent of which set is currently active.

Fast A20 (I/O Address EEh or 92h)

EEh	D7	D6	D5	D4	D3	D2	D1	D0
Fast A20	1	1	1	1	1	1	1	1

92h	D7	D6	D5	D4	D3	D2	D1	D0
Port A	1	1	1	1	1	1	A20	Reset

A read of I/O port EEh enables Fast A20 and returns a value of FFh. A write disables Fast A20. This method provides a fast, parallel alternative to the standard PC/AT-compatible method of using the keyboard controller to control A20. Internally, this signal and A20GATE are ORed so that either event controls the A20 address line and generates –BLKA20. Default on reset is internal A20 control disabled. While disabled, A20 is solely controlled by the A20 input for strict PC/AT-compatibility.

Fast A20 is also controlled via bit 1 of I/O register 92h for PS/2-compatibility. This register is known as Port A. When bit 1 = 1, A20 is active. When bit 1 = 0, A20 always = 0. This feature is fully integrated with the Fast A20 control achieved through EEh, i.e. a read of EEh followed by a read of bit 1 of port 92h returns a logic 1.

If bit 7 of MISCSET register = 1, the fast A20 feature at EEh is disabled.

Fast CPU Reset (I/O Address EFh or 92h)

EFh	D7	D6	D5	D4	D3	D2	D1	D0
Fast Reset	1	1	1	1	1	1	1	1

92h	D7	D6	D5	D4	D3	D2	D1	D0
Port A	1	1	1	1	1	1	A20	Reset

This register provides an alternative to use of the –RC input in order to reset the processor. A read of EFh resets the processor. This reset signal must be ORed internally with the –RC input so that either event invokes a reset. This may provide a faster way for the system to jump between real and protected mode. Reset timing is the same as described below for the Port A reset.

Fast CPU reset can also be controlled via bit 0 of I/O register 92h for PS/2-compatibility. This register is known as Port A. When bit 0 = 1, a reset operation is triggered. Reset pulses are high for 16 CLK2s. This latch remains set until written again or until the VL82C330 is externally reset.

If bit 7 of the MISCSET register = 1, the fast CPU reset feature at EFh is disabled.

Note that in order to successfully reset a PC/AT-compatible system, A20 must be gated through and not held low, otherwise, the reset vector is not fetched and the system hangs up. Therefore, before issuing a "Hot" reset command, either via I/O port 92H or I/O port EFh as described above, one of the following must occur: 1. Set bit 1 to 1 in Port A. (Writing 03h to this register effectively accomplishes both goals with a single I/O instruction.) 2. Perform a read of EEh to enable A20.

Coprocessor Control (I/O Address 0F0h and 0F1h)

0F0h	D7	D6	D5	D4	D3	D2	D1	D0
Clear/Busy	X	X	X	X	X	X	X	X

0F1h	D7	D6	D5	D4	D3	D2	D1	D0
Reset Copro	X	X	X	X	X	X	X	X

A write to I/O port F0h clears the D-flop which holds –BUSY386 and PEREQ386 active after an –ERROR387 signal occurs. A write to I/O port F1h resets the 387DX. This write results in a positive pulse 80 CLK2 cycles wide and is synchronized to CLK2. –READYO is held inactive during this entire period for 100 CLK2s after the falling edge of RES387.

Bit 6 of MISCSET must be set to 0, otherwise a write to F1h does not cause a reset.

CPU Speed (I/O Address 0F4h and 0F5h)

0F4h	D7	D6	D5	D4	D3	D2	D1	D0
Slow CPU Speed	X	X	X	X	X	X	X	X

0F5h	D7	D6	D5	D4	D3	D2	D1	D0
Fast CPU Speed	X	X	X	X	X	X	X	X

A write to Port 0F5H causes the CPU to run at normal "fast" speed. A write to Port 0F4H invokes the CLK2 divider circuit. This is selected by writing the appropriate code to the MISCSET register described later in this document. The programmable range provided allows 12 to 33 MHz systems to run at or below 8 MHz. Default on reset is "fast" speed.

If bit 7 of the MISCSET register = 1, this CPU speed feature is disabled. See the description under MISCSET in the section titled "Functional Summary of Indexed Registers" for more details. The speed control activated by the BIOS through the keyboard controller is always available to access this function.

Configuration Enable/Disable Registers (I/O Addresses 0FBh and 0F9h)

0FBh	D7	D6	D5	D4	D3	D2	D1	D0
Config Enable	X	X	X	X	X	X	X	X

0F9h	D7	D6	D5	D4	D3	D2	D1	D0
Config Disable	X	X	X	X	X	X	X	X

When enabled and used as described above, the configuration registers are protected from unauthorized accesses that might garble the system configuration and either crash the system or change its operational characteristics in an unwanted manner. A write to 0FBh enables the configuration registers. A write to 0F9h disables the configuration registers. When disabled, the system is locked out from any access to the configuration and control ports from address E8h through EFh. This includes the registers previously described in this section, the EMS registers described in the "Shadow RAM Subsystem" section and the indexed configuration registers described in the "Functional Summary of Indexed Registers" section.

If bit 7 of the MISCSET register = 1, the configuration enable/disable feature is disabled. See the description under MISCSET in the section "Functional Summary of Indexed Registers" for more details.

Sleep Mode Control Subsystem

Data Port EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
SLEEP (13)	Enable	Power Down CLK2 Divider			Ext Ctrl 3	Ext Ctrl 2	Ext Ctrl 1	SYSCLK

Sleep mode operation is provided for battery operated laptop microcomputer support. The sleep indexed configuration register is provided to control this function. Bits 0 and 4 through 6 are set with the desired values by the BIOS on POR. Then only bit 7 needs to be toggled to get in and out of sleep mode during operation. Bits 1 through 3 also have a special, optional function which may require control in the course of an operating session. For maximum power savings, it is recommended that a halt instruction be executed immediately after setting bit 7. Any interrupt brings the CPU out of HALT mode.

Bit 7 is set to 1 to invoke all chip set sleep functions. When set, CLK2 is divided by the value coded in bits 4 through 6 of the sleep register. These bits provide a code used to divide the CLK2 down for sleep mode. Division from 2 to 64 is programmable. The range is specified in the "Functional Summary of Indexed Registers" section.

When used with non-static CPU's the greatest division is selected that remains above the minimum operational frequency.

Normally, –RASBK-only refresh is performed. This requires driving the memory address lines and power is consumed. When bit 7 =1, the refresh controller switches to CASBK before –RASBK refresh. If CASBK before –RASBK refresh is not desired while in sleep mode, setting CTRL1[6]=1 maintains standard refresh operation.

The VL82C330 is brought out of sleep mode by resetting bit 7 to a logic 0. This can be done by providing a hardware reset to the VL82C330 or by a CPU write of 0 to bit 7. A hardware reset or an INTA cycle of the VL82C330 also resets this bit.

Bits 1 through 3 provide for software control of an external device. The state of each bit is ORed with bit 7 and the ORed output is connected to an external pin on the VL82C330. This causes the external pin to be active whenever the sleep mode is active (high) or whenever bit 1 is set high.

Bit 0 - The sleep register is "shadowed" in the Bus Controller. That is; it exists at the same address as a write-only register in the Bus Controller. However, only bits 0 and 7 are valid in the Bus Controller. See the VL82C331 ISA Bus Controller data sheet for more details. In the VL82C330, bit 0 is a read/write bit without function. This bit is provided so that software can detect the last state written to it in the Bus Controller.

When CTRL1[1]=0, the –SLP/MISS (pin 6) provides an external indication of the inverse state of the SLEEP[7] bit. That is, when pin 6 is low, sleep mode is active. This can be used as an external indicator of sleep mode or as an external sleep mode activation signal for other devices.

See sleep mode operation in the VL82C331 ISA Bus Controller data sheet and in the section "Sleep Mode Control Subsystem" in this data sheet for additional information.

Turbo/Slow CPU Control Subsystem

Data Port EDh (R/W)	D7	D6	D5	D4 D3	D2 D1	D0
MISCSET (14)	FX Enable	F1 Ctrl	MBIOS	**Slow CLK2 Divider**	Slot Bus Divider	Bus Mode

It has become standard for fast PC/AT-compatibles to provide means to slow operation for older, speed sensitive software. This is especially true for graphics intensive entertainment software which may otherwise operate much too fast on a high speed machine. Bits 3-4 of the MISCSET indexed configuration register are used to specify a CLK2 divider that is active when the slow CPU mode is activated. This range provides the capability to operate at 8 MHz or under, for any actual CPU speed from 12 to 33 MHz.

One way this mode may be toggled on and off is by external control of the TURBO input pin. When TURBO is low, the slow mode is activated and the CLK2 divider is in effect. When TURBO is high or during HLDA cycles, CLK2 runs at the same speed as TCLK2 (only if the SF TURBO request is also active, see above). The TURBO pin is normally connected to the keyboard controller and triggered by the BIOS via detection of a "hot key" combination such as Ctrl Alt +. This input is often externally ANDed with a mechanical turbo switch on the front panel.

For SF compatibility, another method is provided if separately enabled. A write to I/O port 0F4h also selects the CLK2 divider circuit for slow operation. A write to 0F5h returns to full speed operation. The SF must be enabled (bit 7 of MISCSET = 0) for the latter mechanism to be active. The SF internal speed control mechanism is ANDed with the TURBO input pin. In this way, any single request for slow operation causes it to occur.

Note: The state of TURBO has no impact on the slot clock frequency. See the sections "Functional Summary of Indexed Registers" and "Dedictated Internal Control Registers" for additional data.

SPECIAL CYCLES

Halt/Shutdown Detection

The VL82C330 detects and responds as described below to halt and shutdown operations from the CPU.

The chip set detects halt only to differentiate it from the shutdown cycle. No further action is taken in response to halt except to acknowledge it by asserting –READYO after two wait states.

Shutdown is handled differently. This bus cycle is executed by the CPU in response to a critical internal processing error. The VL82C330 responds by asserting –READYO after two wait states, then issuing a CPU-only reset for 16 CLK2 cycles.

ISA Cycles

The VL82C330 provides no time out feature for ISA bus cycles. The ISA Bus Controller performs these cycles based on the programmed number of wait states. There is no limit enforced on IOCHRDY.

Memory Cycles

Memory cycles above on-board memory below 16M are passed to the ISA bus. Cycles above on-board memory and above 16M are handled by the VL82C330 which generates a –READYO after two wait states. Memory mapped devices in the region, therefore, have two wait states to decode this cycle as their own and gate off the VL82C330's –READYO signal before it becomes the system ready signal.

Coprocessor Cycles

When the VL82C330 detects a memory access to the Weitek 3167 memory space, it generates a –READYO in approximately 7.5 µs if it does not receive a –READYI signal within this time.

When the VL82C330 detects a 387 NPX access, it generates a –READYO signal in one wait state if a –READYI signal is not received.

TABLE 11. 386 HALT/SHUTDOWN DETECTION

D/–C	W/–R	–BEO	Mode
0	1	1	Halt
0	1	0	Shutdown

SYSTEM RESET OPTIONS

This section describes all reset modes of the VL82C330 based on their activating signal. They have been discussed in other applicable sections of this document and are summarized as an aid the reader.

RSTDRV: Hardware reset pin from the ISA Bus Controller. This signal causes all internal state machines to be reset. The internal configuration registers are reset to their default values shown in Table 12. Resets are issued to the 386 and the 387. The –BUSY386 signal is active for at least eight CLK2 cycles before and after the falling edge of the RES386 signal. This invokes the self-test mode of the 386DX. Systems that desire to use this feature can then read the result of this test in the 386DX's EAX register and decide what to do based on the result. Otherwise, it can be ignored.

–RC: When active, a CPU-only reset is issued immediately on RES386 for 16 CLK2 cycles synchronous with CLK2.

REG_92: Setting bit 0 of I/O port 92h causes a 386-only reset. After approximately 6.75 µsec, a RES386 is activated for 16 CLK2 cycles. See the section "Dedicated Internal Control Register" for more details.

REG_EF: A read of I/O port EFh causes a 386-only reset. After approximately 6.75 µsec, a RES386 is activated for 16 CLK2 cycles. SF must be enabled for this feature to function. See the section "Dedicated Internal Control Register" for more details.

OUT_F1: A write to I/O port F1h causes an 387-only reset. RES387 is activated for 80 CLK2 cycles. Ready assertion is held off for another 100 CLK2 cycles. See the section "Dedicated Internal Control Registers" for details.

SHUTDOWN: Detection of the shutdown condition causes a 386-only reset for 16 CLK2 cycles. See the section "Halt/Shutdown Detection" for additional information.

IN-CIRCUIT TEST LOGIC

The VL82C330 is designed to make system board testing as easy as possible. The –TRI input causes all pins on the VL82C330 go to a high impedance state. This can be used to isolate the VL82C330 so other components in the system can be tested.

The –TRI input can also be used to put the VL82C330 into a special test mode called In-Circuit Test (ICT). The purpose of ICT is not to functionally test the VL82C330 while it is inserted in a circuit board, but to test that the part is connected correctly and all the pins can be toggled high and low in a predictable pattern.

During in-circuit test (ICT), each output may be toggled by one or more of the inputs. This allows for a board level tester to check the solder connection of each pin. The sequence for enabling ICT is as follows:

1. Tester drives –TRI pin low.
2. Tester drives XD0 with a value of 1.
3. Tester simultaneously pulses –IOR and –IOW low for at least 100 ns.
4. Tester drives –TRI pin high.
5. VL82C330 remains in ICT mode until the RSTDRV pin is activated or until steps 1-4 are repeated with XD0=0.

IN-CIRCUIT TEST DESCRIPTION

ICT INPUT		ICT INPUT		ICT INPUT		ICT INPUT		ICT OUTPUT	
Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
A17	2	A14	5	A11	9	A8	12	–REFRESH	109
A16	3	A13	6	A10	10	A7	13	–CHS0/–MW	103
A15	4	A12	7	A9	11	A6	15	–CHS1/–MR	102
A5	16	A3	18	–BE3	20	–	–	CLK2	32
A4	17	A2	19	–BE2	21	–	–	–SLP/MISS	35
–BE1	22	D/–C	25	HLDA	28	–	–	–ERROR386	37
–BE0	23	M/–IO	26	–READYI	29	–	–	–BUSY386	38
W/–R	24	–ADS	27	CLK2IN	30	–	–	PEREQ386	39
–READYO	34	RES387	41	–ERROR387	43	PEREQ387	46	HRQ	40
RESCPU	36	–BUSY387	42	TCLK2	44	WTKIRQ	47	SLEEP1	49
–MDLAT	52	MA10	57	MA7	62	–	–	SLEEP2	50
–DEN	53	MA9	58	MA6	63	–	–	SLEEP3	51
–RAMW	55	MA8	60	MA5	64	–	–	–ROMCS	54
MA4	66	LBE2	74	CASBK0	80	–	–	XD7	86
MA3	67	LBE1	75	–RASBK3	81	–	–	XD6	87
MA2	69	LBE0	76	–RASBK2	82	–	–	XD5	88
MA1	71	CASBK3	77	–RASBK1	83	–	–	XD4	89
MA0	72	CASBK2	78	–RASBK0	85	–	–	XD3	90
LBE3	73	CASBK1	79	BUSCLK	98	–	–	XD2	91
–CHREADY	104	BUSOSC	106	OSC	110	–	–	XD1	92
DMAHRQ	105	OUT1	107	–IOR	112	–	–	XD0	93
–IOW	113	TURBO	115	A31	117	–	–	–BLKA20	94
–RC	114	A20GATE	116	A29	118	–	–	–BRDRAM	95
A26	119	A23	122	A20	125	–	–	DMAHLDA	99
A25	120	A22	123	A19	126	–	–	IRQ13	100
A24	121	A21	124	A18	127	–	–	CHM/–IO	101

CONFIGURATION REGISTER SET
Software Access
Index Registers (I/O Address ECh)
The value written to this register is the 8-bit address of the data port which is accessed through the data port register at I/O address EDh. All subsequent data port reads and writes accesses the register at this address until the index register is written with a new 8-bit address. This register is readable. It always returns the last value written to it.

The Configuration Registers can only be accessed via the CPU and are limited to byte reads and writes.

Data Port Register (I/O Address EDh)
Each register accessible through I/O address EDh is functionally described below. It is accessed first by writing its address to the index register at I/O address ECh, then by accessing the data port at I/O address EDh.

FUNCTIONAL SUMMARY OF INDEXED REGISTERS
Version (00h) (Read-only)
D2-D7 contains a read-only code which indicates that this part is a VLSI Technology PC/AT-compatible VL82C330. D0 and D1 contain the version number of this chip. The first production version of this chip uses the code F2h. Breaking the code into two bit pieces reveals it to be "330" Rev "2."

SLOTHI and SLOTLO (01h and 02h) (Default = FF,FF)
These two registers represent the upper address bits of the base address where off-board (slot) memory accesses begin. In combination they are referred to as SLTPTR. (See the "SLTPTR - Critical Memory Control Element" section.) SLOTLO contains a full eight bits corresponding to A16-A23. Reading this byte returns the last value written. SLOTHI only contains two active bits corresponding to A24 and A25. Reading this register returns the last values written to bits 0 and 1 and logic 1's in all other bit positions. (Default = 03FFh, no off-board memory accesses.)

RAMMAP (03h) (Default = E0h)
Bit 7 in conjunction with the EAXS register, determines system response to memory accesses between E0000h-EFFFFh. When set to a logic 1 and the EAXS code for the specific 16K segment is 00b, reads generate a –ROMCS and a ROM access is performed from the MD bus. When set to a logic 0 and the EAXS code for the specific 16K segment is 00b, reads and writes are performed to the slot bus. This feature allows systems not using a 128K BIOS to access memory devices on the slot bus in the E0000h-EFFFFh area. See EAXS below for further details. Accesses to the area between FE0000h-FEFFFFh also respond in the above manner except that EAXS has no control over this memory space. However, in this area there is an interaction with the mid-BIOS control provided by MISCSET[5] described below.

Bits 4-0 specify one of the valid memory maps as shown Table 1. Note that not all possible 6-bit codes are assigned to valid memory maps.

RAMMOV (04H) (Default = F0h)
Bits 3-0 specify a switching function which determines which internal –RAS3- –RAS0 and CAS3-CAS0 signals drive which external –RASBK3 - –RASBK0 and CASBK3- CASBK0 pins. (Default = 0.)

Refer to Table 2 for the remap configuration register code mapping.

RAMSET (05h) (Default =7Ch)
Bits 7-6 program the drive current on lines MA0-MA10 and on –RAMW according to the following codes:
00 = 150 pF drive
01 = 300 pF drive (Default)
10 = 450 pF drive
11 = 600 pF drive

Bit 5 is set to 0 in order to allow a cycle to begin one CLK2 earlier. This provides extra access time. (Default = 1 Early Start Disable) Early Start may be enabled in systems running at 16 MHz or below.

Bit 4 programs the drive level on the –RASBK pins.
1 = 12 ma drive (Default = 1)
0 = 24 ma drive

Bit 3 indicates whether page mode is active on Bank A.
0 = Disabled
1 = Enabled (Default)

Bit 2 indicates whether page mode is active on Bank B.
0 = Disabled
1 = Enabled (Default)

Bit 1 indicates the interleave mode for Bank A. It is encoded as follows:
0 = Interleave on bit 1 for all DRAMs (Default)
1 = Interleave on bit 10 for all DRAMs

Bit 0 indicates the interleave mode for Bank B. It is encoded as follows:
0 = Interleave on bit 1 for all DRAMs (Default)
1 = Interleave on bit 10 for all DRAMs

REFCTL (06h) (Default = 00h)
Bit 7 is 0 for coupled refresh mode and 1 for decoupled refresh mode. (Default = 0.)

Bits 6-4 provide three bits to specify a divider for on-board refresh.
000 = ÷ 1 (Default)
001 = ÷ 2
010 = ÷ 4
011 = ÷ 8
100 = ÷ 16

Bit 3 controls internal I/O decode. When bit 3 = 0, full 16-bit decode is performed. When bit 3 = 1, 10-bit I/O decode is performed. (Default = 0.)

Bits 2-0 provide three bits which specify a divider for off-board refresh.
000 = ÷ 1 (Default)
001 = ÷ 2
010 = ÷ 4
011 = ÷ 8
100 = ÷ 16

RASTMA - RAS Timing for DRAM Banks 0 and 1 (07h) (Default = FFh)
Bit 7 indicates the –RASBK to column address delay:
0 = 1/2 CLK2
1 = 1 CLK2 (Default)

Bit 6 indicates number of clock delays between –RASBK and CASBK (tRCD). Actual clock delays encoded by this bit is:
0 = 1 CLK2
1 = 2 CLK2s (Default)

Bits 5-3 indicate the number of clock periods of –RASBK precharge time (tRP). Bit encoding relative to the number of clocks is:
010 = 2 CLK2s
011 = 3 CLK2s
100 = 4 CLK2s
101 = 5 CLK2s
110 = 6 CLK2s
111 = 7 CLK2s (Default)

Bits 2-0 indicate the number of clock periods of –RASBK active time (tRAS). Bit encoding relative to the number of clocks is:
000 = 2 CLK2s
001 = 3 CLK2s
010 = 4 CLK2s
011 = 5 CLK2s
100 = 6 CLK2s
101 = 7 CLK2s
110 = 8 CLK2s
111 = 8 CLK2s (Default)

CASTMA - CAS Timing for DRAM Banks 0 and 1 (08h) (Default = FFh)
Bits 7-6 indicate the number of clock cycles of CAS active time during memory writes (tCASW):
00 = 1 CLK2
01 = 2 CLK2s
10 = 3 CLK2s
11 = 4 CLK2s (Default)

Bit 5 indicates the number of CLK2s of delay that occur before CAS goes active after the start of the status cycle (tCST). This parameter is applicable during all write operations.
0 = 3 CLK2s
1 = 4 CLK2s (Default)

Bits 4-3 indicate the number of clock cycles of CAS precharge time (tCP). Bit encoding relative to the number of clocks is:
00 = 1 CLK2
01 = 2 CLK2s
10 = 3 CLK2s
11 = 4 CLK2s (Default)

Bits 2-0 indicate the number of clock cycles of CAS active time during memory reads (tCASR). Bit encoding relative to the number of clocks is:
000 = 2 CLK2s
001 = 3 CLK2s
010 = 4 CLK2s
011 = 5 CLK2s
100 = 6 CLK2s
101 = 7 CLK2s
110 = 8 CLK2s
111 = 8 CLK2s (Default)

RASTMB - RAS Timing for DRAM Banks 2 and 3 (09h) (Default = FFh)
See RASTMA for bit definitions.

CASTMB - CAS Timing for DRAM Banks 2 and 3 (0Ah) (Default = FFh)
See CASTMA for bit definitions.

EMSEN1 (0Bh) (Default = 00h)
Bit 7 is set as global enable for the EMS translation registers from C0000h to EC000h.
0 = EMS disable (Default)
1 = EMS enable

Bit 6 is set as the global enable for the EMS backfill translation registers from 40000 to 9C000h.
0 = Backfill disable (Default)
1 = Backfill enable

Bit 4 determines the EMS window range.
0 = EMS Map 0
1 = EMS Map 1

Each bit below is associated with one of the EMS registers. A 0 indicates that the associated page register is disabled. A 1 indicates that it is enabled.

Page Controlled by each bit:

Bit 0	EMS Page 8
Bit 1	EMS Page 9
Bit 2	EMS Page 10
Bit 3	EMS Page 11

EMSEN2 (0Ch) (Default = 00h)
Each bit is associated with one of the EMS registers. A 0 indicates that the associated page register is disabled. A 1 indicates that it is enabled. When disabled, an attempted access to the associated address space actually accesses that address directly. When enabled and the entire EMS system is enabled by having bit 7 of the EMSEN1 register set, an access to the associated page is redirected to the address contained in the page register concatenated with 386 address bits A0-A13. Whether bits 0-3 control the AXXXXh or CXXXXh range is determined by the state of EMSEN1[4]. Bits 4-7 control the DXXXXh range in either state of EMSEN1[4]. Bits 4-7 control the DXXXXh range in either state of EMSEN1[4]. (Default value for this register is 0; all EMS page registers are disabled.)

Page Controlled by each bit:

Bit 0	A/C0000
Bit 1	A/C4000
Bit 2	A/C8000
Bit 3	A/CC000
Bit 4	D0000
Bit 5	D4000
Bit 6	D8000
Bit 7	DC000

The following registers provide control over the memory range from 640K to 1 Mbyte.

In the registers summarized below, each pair of bits control one 16K page as defined by the following table:

	Read	Write
Slot Bus*	0	0
System Board	1	1

*In the address space F0000h to FFFFFh, default means accesses are from on-board ROM space. Default accesses in areas from A0000h-DFFFFh are from the slot bus. Default in the area from E0000h-EFFFFh can be either on-board ROM or slot bus accesses depending on the state of RAMMAP[7].

This table translates to the following four cases:
00 = Read Default, Write Slot Bus
01 = Setup Mode: Read Default, Write System Board
10 = Read System Board, Write Slot Bus
11 = Read/Write System Board

AAXS (0Dh) *Default is always the slot bus. (Default = 00h)
Bits 6-7 - segment at AC000h.
Bits 4-5 - segment at A8000h.
Bits 2-3 - segment at A4000h.
Bits 0-1 - segment at A0000h.

BAXS (0Eh) *Default is always the slot bus. (Default = 00h)
Bits 6-7 - segment at BC000h.
Bits 4-5 - segment at B8000h.
Bits 2-3 - segment at B4000h.
Bits 0-1 - segment at B0000h.

CAXS (0Fh) *Default is always the slot bus. (Default = 00h)
Bits 6-7 - segment at CC000h.
Bits 4-5 - segment at C8000h.
Bits 2-3 - segment at C4000h.
Bits 0-1 - segment at C0000h.

DAXS (10h) *Default is always the slot bus. (Default = 00h)
Bits 6-7 - segment at DC000h.
Bits 4-5 - segment at D8000h.
Bits 2-3 - segment at D4000h.
Bits 0-1 - segment at D0000h.

EAXS (11h) *Default may be on-board BIOS ROM access or slot bus access. (Default = 00h)
This memory space is a special case in that "default" can be one of two locations depending on the state of the RAMMAP[7] bit.

RAMSET[7]	EAXS	Operation
0	00	Read/Write Slot Bus
1	00	Read On-Board ROM, Write Slot Bus (–ROMCS Active)
0	01	Shadow Setup Mode: Read Slot Bus, Write System Board
1	01	Shadow Setup Mode: Read On-Bus ROM, Write System Board
X	10	Read System Board/Write Slot Bus (Shadow Active)
X	11	Read/Write System Board

FAXS (12h) *Default may be on-board BIOS ROM access. (Default = 00h)
Bits 6-7 - segment at FC000h.
Bits 4-5 - segment at F8000h.
Bits 2-3 - segment at F4000h.
Bits 0-1 - segment at F0000h.

SLEEP (13h) (Default = 01h)
Bit 7 - Power-down enable.
0 = Default operational setting. Normal clock speed.
1 = Invokes clock divider set in bits 4 through 6.

This bit is reset to 0 and normal operation resumes when rewritten or when the VL82C330 receives a hardware reset.

Bits 6-4 - Power-down CLK2 divider. These bits provide a code used to divide the CLK2 down for sleep mode. The codes are:
000 = +1 Default (/1 clock)
001 = +2
010 = +3
011 = +4
100 = +8
101 = +16
110 = +32
111 = +64

Bits 3-1 provide for software control of an external device. The state of these bits is ORed with bit 7 and the ORed output is connected to an external pin on the VL82C330. This causes the external pin to be active whenever the sleep mode is active (high) or whenever bit 1 is set high. (Default = 00b.)

Bit 0 is a simple latch that provides no functionality in the VL82C330. However, a read always reflects the last write to this bit. (Default = 1.)

MISCSET (14h) (Default = 06h)
Bit 7 is used to enable or disable the SF options mapped into the coprocessor chip set I/O space between F0h and FFh.
0 = enabled (Default)
1 = disabled

Bit 6 controls coprocessor software reset.
0 = enabled (Default)
1 = disabled

Bit 5 controls the middle BIOS space from 00FE0000h to 00FFFFFh. Two options are provided:
0 = This space mirrors the 000E0000h to 000FFFFFh space. – ROMCS is generated for this space. (Default)
1 = This space maps directly to read/write on-board DRAM.

Bits 4-3 specify the CLK2 divider that is invoked when the TURBO input pin is low or when a write to port 0F4h is performed.
00 = CLK2 +1 (Default)
01 = CLK2 +2
10 = CLK2 +3
11 = CLK2 +4

Bits 2-1 are the value used for division of TCLK2 or BUSOSC to generate BUSCLK.
00 = + 1
01 = + 2
10 = + 3
11 = + 4 (Default)

Bit 0 indicates the BUSCLK divider source.
0 = TCLK2 (Default)
1 = BUSOSC

TEST (15h) (Default = 00h)
This register is reserved for "to be determined" factory test functions. It must never be written during normal operation.

CTRL1 (16h) (Default = 00h)
This register contains additional system functional controls. Bits 1, 2, and 3 are reserved for interface to a future TOPCAT-compatible circuit. Do not write 1's to these bits. Bit 0 also will be used for this future circuit but it also controls a function in this version of the VL82C320. See below for details.

Bit 7 provides for disk controller compatibility. With fast CPUs, some disks can be overrun by programmed I/O. This bit provides a way to compensate by forcing the first memory cycle after an I/O cycle to be executive at non-turbo speed.
0 = slow programmed I/O (Default)
1 = normal programmed I/O

Bit 6 provides the option to not perform CASBK before –RASBK refresh while sleep mode is active. When set to 1, normal refresh is performed while in sleep mode. This consumes more power because the VL82C330 must drive the MA10-MA0 and –RAMW signals to all DRAM chips. When set to 0, CASBK before –RASBK refresh occurs while in sleep mode. (Default =0)

Bits 5 and 4 are used to open a 64K or 128K window at the top of DOS memory for access by slot bus cards. This allows accesses to be directed off-board in this region but then come back on-board in order to access on-board extended memory. The slot pointer (SLTPTR) cannot be used to provide this function because all accesses above slot pointer are off-board and there is no way to gain access to on-board memory above this pointer except through the EMS hardware. These bits affect only the CPU address space from 512K-640K.

0X - on-board accesses in the 512K-640K region (Default = 00)
10 - 576K-640K accesses slot bus. 512K-576K on-board accesses.
11 - 512K-640K accesses slot bus.

Special cases: This feature is inactive when EMS backfill is enabled. An attempt to set a code other than 0Xb with EMS backfill enabled will fail to change the code. If this feature is activated with codes 1Xb and EMS backfill is later activated, the code will automatically change to 00b disabling slot bus accesses in this region.

Use of SLTPTR in the same range is totally compatible. SLTPTR rules. If SLTPTR = 576K or 512K, the setting of CTRL1[5:4] doesn't matter. Accesses will be directed to the slot bus in this region and will also remain off-board above 640K.

Bit 3 is reserved. In the current generation, this bit is read/write but serves no other function. This bit will be used with CTRL1[10] which is the Cache Present bit. This will allow the cache to be present but still in either an enabled or disabled state. (Default = 0, cache disabled)

Bit 2 is a dummy stimulus bit used to test the cache input portion of the memory control state machine. Writing a one to this bit gives the memory controller a dummy indication of a cache hit. Writing a zero indicates a dummy cache miss. (Default = 0)

Bit 1 is set to 1 in systems containing a cache controller. This is used by the memory controller when page mode is enabled. It causes a –RASBK pre-charge on a page miss during a cache hit. (Default = 0)

Bit 0 changes the definition of the –SLP/MISS pin from –SLP output to MISS input when set to "1". (Default = 0)

TABLE 12. INDEXED CONFIGURATION MAP

Index Port	D7	D6	D5	D4	D3	D2	D1	D0
ECh (R/W)	A7	A6	A5	A4	A3	A2	A1	A0

Data Port EDh (R/W)		D7	D6	D5	D4	D3	D2	D1	D0
00	VER (R-O)	1	1	1	1	0	0	0	0
01	SLOTHI	1	1	1	1	1	1	A25	A24
02	SLOTLO	A23	A22	A21	A20	A19	A18	A17	A16
03	RAMMAP	ROMSLOT	1	1	DRAM Memory Map Code				
04	RAMMOV	1	1	1	1	RASBK - CAS Swap Code			
05	RAMSET	DRAM Drive		ESTART	RAS DRV	Page Md A	Page Md B	Bank A Int	Bank B Int
06	REFCTL	Decup	Slow Refresh Divider - System Board			10/16 IO	Slow Refresh Divider - Slots		
07	RASTMA	RAS ADDSEL	tRCD	tRP		tRAS			
08	CASTMA	tCASW		tCST	tCP	tCASR			
09	RASTMB	RAS ADDSEL	tRCD	tRP		tRAS			
0A	CASTMB	tCASW		tCST	tCP	tCASR			
0B	EMSEN1	EMS Enable	BF Enable	Reserved	EMSMAP	B/EC000	B/E8000	B/E4000	B/E0000
0C	EMSEN2	DC000	D8000	D4000	D0000	A/CC000	A/C8000	A/C4000	A/C0000
0D	AAXS	AC000 Access		A8000 Access		A4000 Access		A0000 Access	
0E	BAXS	BC000 Access		B8000 Access		B4000 Access		B0000 Access	
0F	CAXS	CC000 Access		C8000 Access		C4000 Access		C0000 Access	
10	DAXS	DC000 Access		D8000 Access		D4000 Access		D0000 Access	
11	EAXS	EC000 Access		E8000 Access		E4000 Access		E0000 Access	
12	FAXS	FC000 Access		F8000 Access		F4000 Access		F0000 Access	
13	SLEEP	Enable	Power Down CLK2 Divider			Ext Ctrl 3	Ext Ctrl 2	Ext Ctrl 1	SYSCLK
14	MISCSET	FX Enable	F1 Ctrl	MBIOS	Slow CLK2 Divider		Slot Bus Divider		Bus Mode
15	TEST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
16	CTRL1	DSKTMG	SLPREF	512-640K Access		KENAB	HITMISS	RASCHG	PRESNT

Note: A 1 indicates reserved bits that read back as logic 1.

TABLE 13. DEFAULT CONFIGURATION VALUES AFTER RESET

Data Port EDh (R/W)		D7	D6	D5	D4	D3	D2	D1	D0
00	VER (R-O)	1R	1R	1R	1R	0R	0R	1R	0R
01	SLOTHI	1R	1R	1R	1R	1R	1R	1	1
02	SLOTLO	1	1	1	1	1	1	1	1
03	RAMMAP	1	1R	1R	0	0	0	0	0
04	RAMMOV	1R	1R	1R	1R	0	0	0	0
05	RAMSET	0	1	1	1	1	1	0	0
06	REFCTL	0	0	0	0	0	0	0	0
07	RASTMA	1	1	1	1	1	1	1	1
08	CASTMA	1	1	1	1	1	1	1	1
09	RASTMB	1	1	1	1	1	1	1	1
0A	CASTMB	1	1	1	1	1	1	1	1
0B	EMSEN1	0	0	0	0	0	0	0	0
0C	EMSEN2	0	0	0	0	0	0	0	0
0D	AAXS	0	0	0	0	0	0	0	0
0E	BAXS	0	0	0	0	0	0	0	0
0F	CAXS	0	0	0	0	0	0	0	0
10	DAXS	0	0	0	0	0	0	0	0
11	EAXS	0	0	0	0	0	0	0	0
12	FAXS	0	0	0	0	0	0	0	0
13	SLEEP	0	0	0	0	0	0	0	1
14	MISCSET	0	0	0	0	0	1	1	0
15	TEST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
16	CTRL1	0	0	0	0	0	0	0	0

Note: Values followed by "R" are read-only and have no logical function. Reserved bits in the Test register are for factory test. Read/write results to this register are undefined.

AC CHARACTERISTICS: **TA = 0°C to +70 °C, VDD = 5 V ±5%, VSS = 0V** (The timing diagrams in this section are preliminary.)

Symbol	Parameter	Min	Max	Unit	Conditions
t1	TCLK2 Period	15		ns	
t2	TCLK2 High Time	6.5		ns	1.5 V
t3	TCLK2 Low Time	6.5		ns	1.5 V
t4	BUSOSC Period	15		ns	
t5	BUSOSC, OSC High Time	6.5		ns	1.5 V
t6	BUSOSC, OSC Low Time	6.5		ns	1.5 V
t7	CLK2IN High Time	5		ns	2.0 V
t8	CLK2IN Low Time	5		ns	2.0 V
tD9	TCLK2 to CLK2 Delay		25	ns	CL=50 pF
t10	CLK2 Fall Time		4	ns	3.7 V to 0.8 V @ CL=50
t11	CLK2 Rise Time		4	ns	0.8 V to 3.7 V @ CL=50
tD12	TCLK2 to BUSCLK Delay		25	ns	CL=50 pF
tD13	BUSOSC to BUSCLK Delay		25	ns	CL=50 pF
t14	BUSCLK Fall Time		9	ns	3.7 V to 0.8 V @ CL=50
t15	BUSCLK Rise Time		12	ns	0.8 V to 3.7 V @ CL=50
tD16	CLK2IN to RES386 Delay	3	10	ns	CL=30 pF
tD17	CLK2IN to RES387 Delay	3	10	ns	CL=30 pF
tD18	CLK2IN to –READYO Delay	3	15	ns	CL=30 pF
tD19	CLK2IN to HRQ Delay	3	18	ns	CL=50 pF
tSU20	–ADS to CLK2IN Setup Time	15		ns	
tH21	–ADS from CLK2IN Hold Time	4		ns	
tSU22	W/–R, M/–IO, D/–C to CLK2IN Setup Time	15		ns	
tSU22a	W/–R, M/–IO, D/–C to CLK2IN Setup Time	26		ns	
tH23	W/–R, M/–IO, D/–C from CLK2IN Hold Time	4		ns	
tSU24	A31,A29, A26-A2 to CLK2IN Setup Time	15		ns	
tSU25	A31, A29, A26-A2 to CLK2IN Setup Time	26		ns	
tH26	A31, A29, A25-A2 from CLK2IN Hold Time	4		ns	
tSU27a	–BE3- –BE0 to CLK2IN Setup Time	4		ns	
tH28	–BE3- –BE0 from CLK2IN Hold Time	4		ns	
tSU30	HLDA to CLK2IN Setup Time	10		ns	
tH31	HLDA to CLK2IN Hold Time	4		ns	
tSU32	–READYIN to CLK2IN Setup Time	15		ns	
tH33	–READYIN from CLK2IN Hold Time	4		ns	
tD34	CLK2IN to –RASBK3- –RASBK0 Delay	3	20	ns	CL=300 pF

Note: Minimum propogation delays noted as "tDX" are characterized but not tested.

AC CHARACTERISTICS: (Cont.)

Symbol	Parameter	Min	Max	Unit	Conditions
tD35	CLK2IN to –RAMW Delay	3	20	ns	CL=300 pF
tD36	CLK2IN to CASBK3-CASBK0 Delay	3	16	ns	CL=50 pF
tD37	CLK2IN to –BRDRAM Delay	3	18	ns	CL=50 pF
tD38	CLK2IN to –DEN Delay	3	17	ns	CL=50 pF
tD39	CLK2IN to –MDLAT Delay	3	19	ns	CL=50 pF
tD40	CLK2IN to –ROMCS Delay	3	20	ns	CL=50 pF
tD41	A31, A29, A26-A2 to MA10-MA0 Delay	3	34	ns	CL=300 pF
tD42	CLK2IN to MA10-MA0 Delay	3	24	ns	CL=300 pF
tD43	CLK2IN to MA10-MA0 Delay	3	22	ns	CL=300 pF
tD44	–BE3- –BE0 Delay	3	23	ns	CL=50 pF
tD45	CLK2IN to LBE3-LBE0 Delay	3	22	ns	CL=50 pF
tD46	CLK2IN to –CHS0/–MW, –CHS1/–MR CHM/–IO Going Low Delay	3	20	ns	CL=50 pF
tD47	BUSCLK to –CHS0/–MW, –CHS1/–MR, CHM/–IO Going High Delay	3	20	ns	CL=50 pF
tSU48	–CHREADY to BUSCLK Setup Time	8		ns	
tH49	–CHREADY from BUSCLK Hold Time	3		ns	
tSU50	XD7-XD0 to –IOW High Setup Time	30		ns	
tH51	XD7-XD0 from –IOW High Hold Time	5		ns	
tD52	–IOR Low to XD7-XD0 Delay	5	50	ns	CL=50 pF
tD53	–IOW High to SLEEP3-SLEEP1, –SLP/MISS Delay	4	25	ns	CL=50 pF
tD54	A20GATE to –BLKA20 Delay	4	20	ns	CL=50 pF
tD56	–IOW or –IOR Low to –BLKA20 Delay	5	25	ns	CL=50 pF
tSU57	DMAHRQ to BUSCLK Setup Time	10		ns	
tH58	DMAHRQ from BUSCLK Hold Time	8		ns	
tD59	BUSCLK to DMAHLDA Delay	3	25	ns	CL=50 pF
tD60	CLK2IN to DMAHLDA Delay	3	25	ns	CL=50 pF
tD61	BUSCLK to –REFRESH Low Delay	3	28	ns	CL=200 pF
tD62	CLK2IN to –REFRESH Low Delay	3	28	ns	CL=200 pF
tD63	BUSCLK to –REFRESH Float Delay	3	20	ns	
tD65	WTKIRQ to IRQ13 Delay	3	20	ns	CL=50 pF
tD66	–ERROR387 Low to IRQ13 Delay	3	25	ns	CL=50 pF
tD67	–IOW Low to IRQ13 Low Delay	3	25	ns	CL=50 pF
tD68	PEREQ387 to PEREQ386 Delay	3	20	ns	CL=50 pF
tD69	–BUSY387 High to PEREQ386 High Delay	3	20	ns	CL=50 pF

AC CHARACTERISTICS: (Cont.)

Symbol	Parameter	Min	Max	Unit	Conditions
tD70	–IOW Low to PEREQ386 Low Delay	3	25	ns	CL=50 pF
tD71	–BUSY387 to –BUSY386 Delay	3	20	ns	CL=50 pF
tD72	–IOW Low to –BUSY386 Delay	3	25	ns	CL=50 pF
tD73	CLK2IN to –BUSY386 Delay	3	20	ns	CL=50 pF
tD74	CLK2IN to –ERROR386 Delay	3	20	ns	CL=50 pF
tSU75	RSTDRV to CLK2IN Setup Time	7		ns	
tH76	RSTDRV from CLK2IN Hold Time	3		ns	
	OUT1, TURBO, –RC, –TRI			ns	No AC Specs on these Pins
tD77	–CHS0/–MW, –CHS1/–MR to CLK2IN Setup	12		ns	CL=50 pF
tD78	–CHS0/–MW, –CHS1/–MR from CLK2IN Hold	4		ns	
tD79	–CHS0/–MW to –RAMW Delay	3	25	ns	CL=50 pF
tD80	–CHS0/–MW, –CHS1/–MR to –BRDRAM Delay	3	25	ns	CL=50 pF
tD81	A23-A1 to –BRDRAM Delay	3	40	ns	CL=50 pF

FIGURE 8.

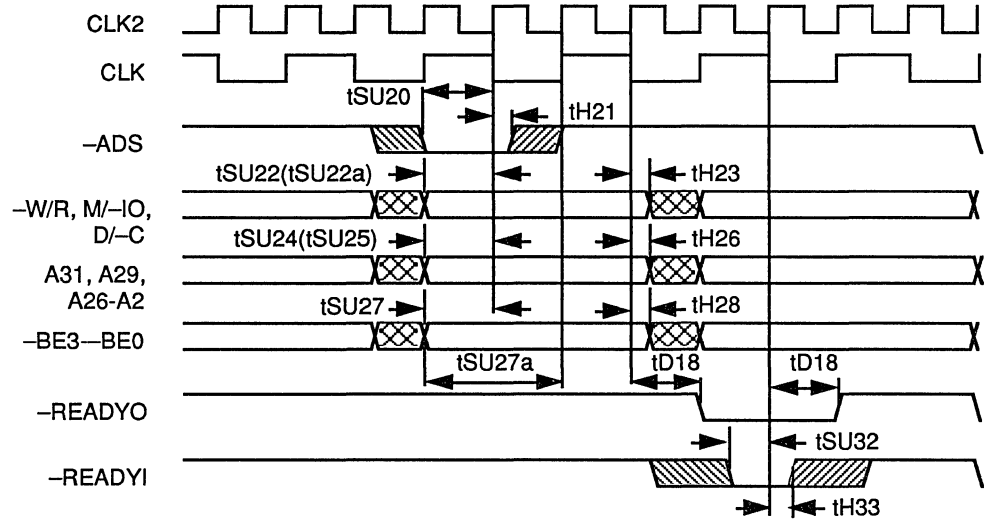


FIGURE 9.

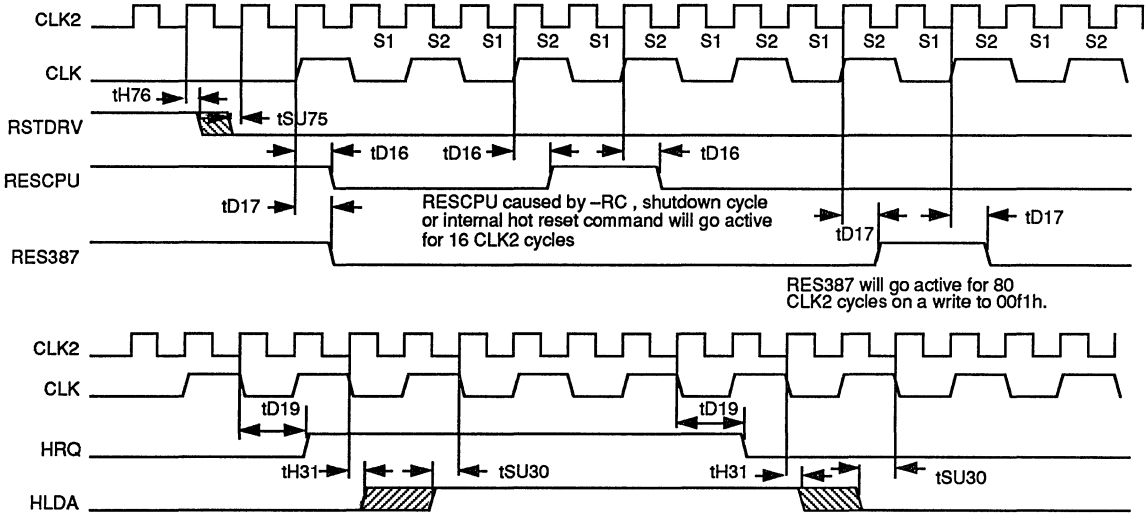


FIGURE 10.

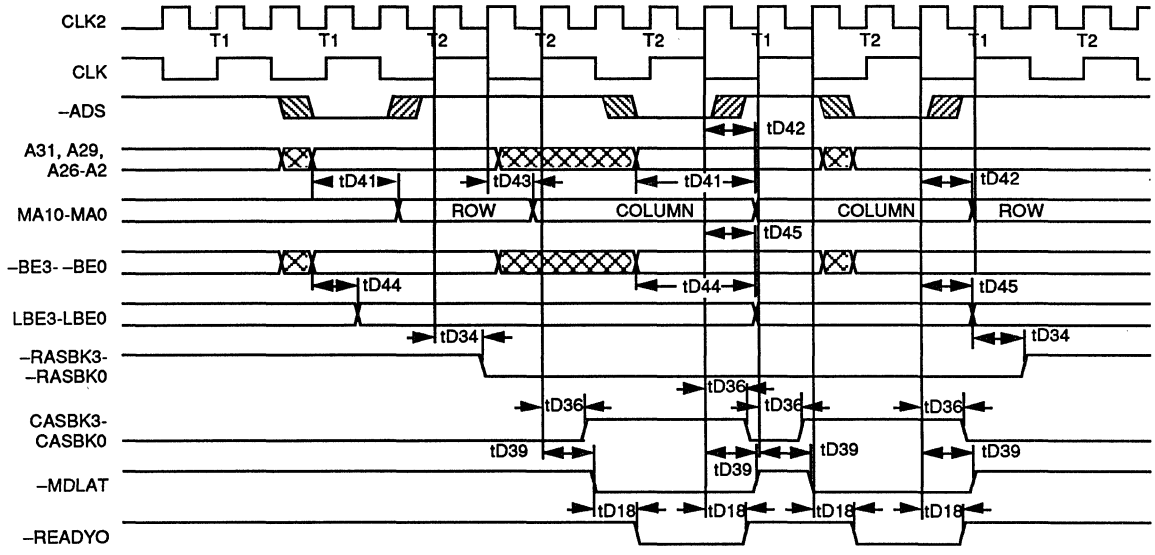
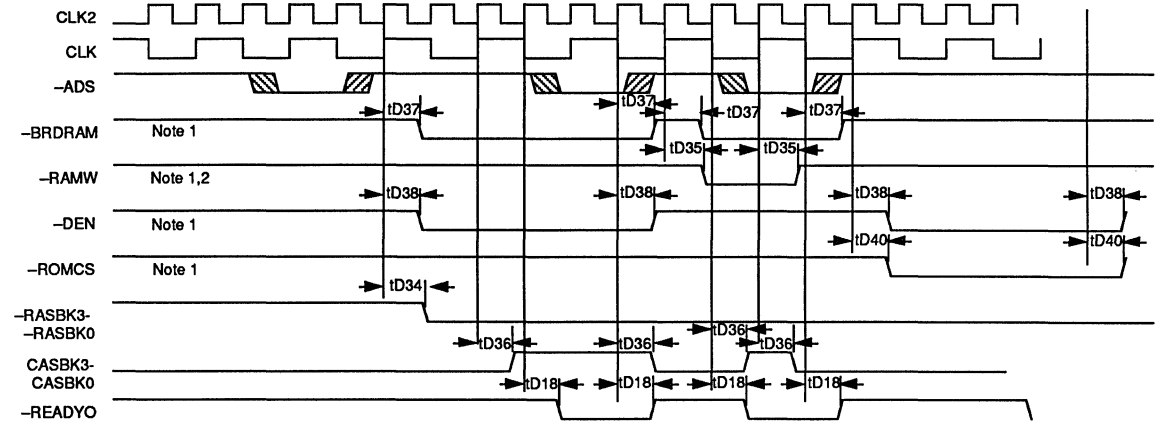


FIGURE 11.



Note: 1. –BRDRAM, –RAMW, –DEN, and –ROMCS are all shown assuming ESTART is inactive. If ESTART is active, these signals will go active one CLK2 cycle earlier. ESTART has no effect on these signals changing to the inactive state.
2. –RAMW will return in active from the same CLK2 edge when CASBK goes inactive.

FIGURE 12.

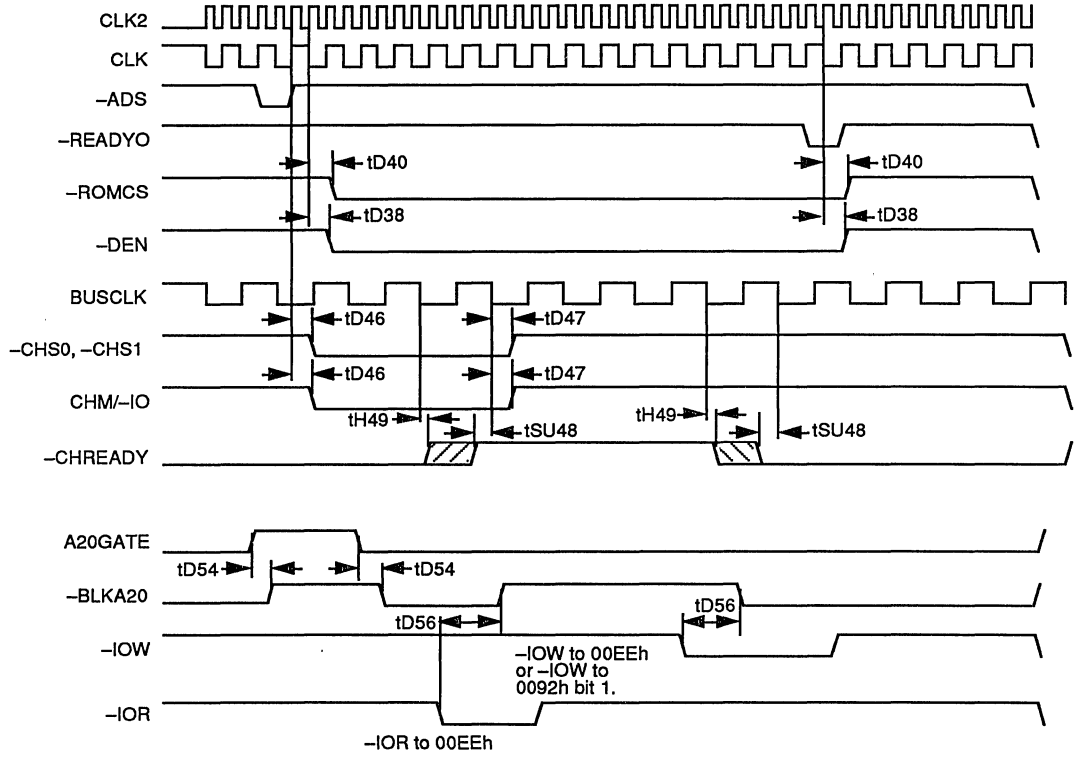


FIGURE 13.

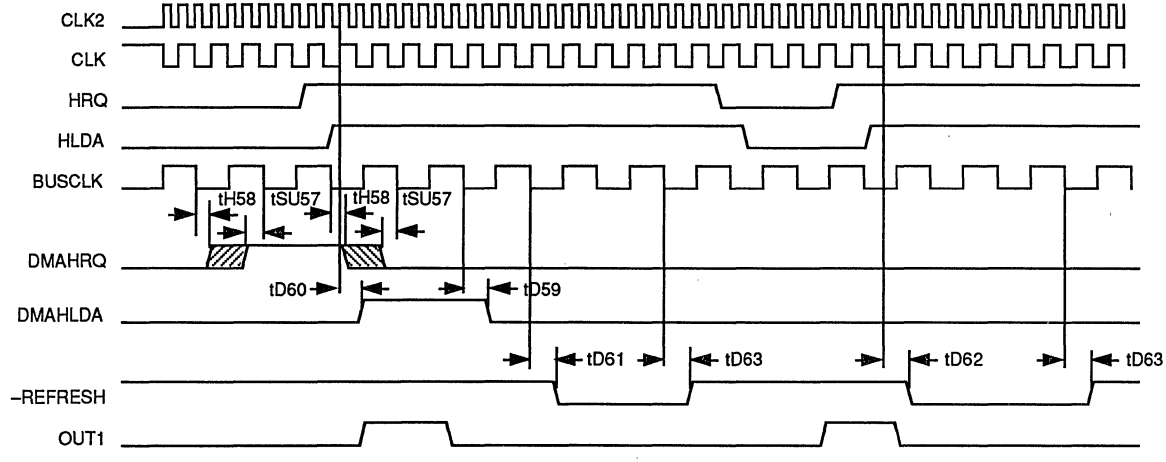
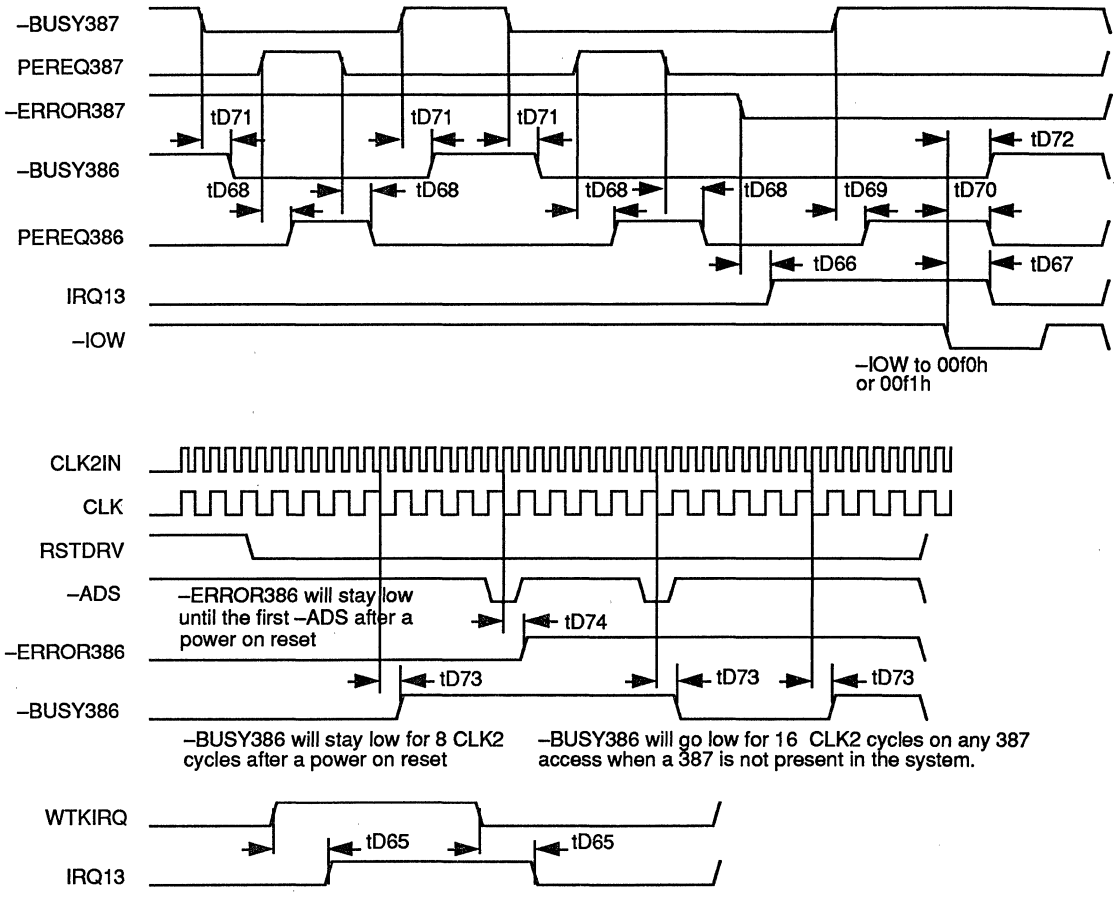


FIGURE 14.


-BUSY387
PEREQ387
-ERROR387
-BUSY386
PEREQ386
IRQ13
-IOW
tD71
tD71
tD71
tD72
tD68
tD68
tD68
tD68
tD69
tD70
tD66
tD67
-IOW to 00f0h
or 00f1h
CLK2IN
CLK
RSTDRV
-ADS
-ERROR386
-BUSY386
-ERROR386 will stay low
until the first -ADS after a
power on reset
tD74
tD73
tD73
tD73
-BUSY386 will stay low for 8 CLK2
cycles after a power on reset
-BUSY386 will go low for 16 CLK2 cycles on any 387
access when a 387 is not present in the system.
WTKIRQ
IRQ13
tD65
tD65

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature −10°C to +70°C

Storage Temperature −65°C to +150°C

Supply Voltage to Ground −0.5 V to VDD = 0.3 V

Applied Output Voltage −0.5 V to VDD = 0.3 V

Applied Input Voltage −0.5 V to 7.0 V

Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min.	Max.	Unit	Conditions
VIL	Input Low Voltage	−0.5	0.8	V	TTL Level Inputs
VIH	Input High Voltage	2.0	VDD +0.5	V	TTL Level Inputs
VILC	Input Low Voltage	−0.5	0.8	V	CMOS Level Inputs
VIHC	Input High Voltage	VDD −0.8	VDD+0.5	V	CMOS Level Inputs
VOL1	Output Low Voltage		0.45	V	IOL = 4 mA, Note 1
VOH1	Output High Voltage	VDD −0.45		V	IOH = −1 mA, Note 1
VOL2	Output Low Voltage		0.45	V	IOL = 8 mA, Note 2
VOH2	Output High Voltage	VDD −0.45		V	IOH = −2 mA, Note 2
VOL3	Output Low Voltage		0.45	V	IOL = 20 mA, Note 3
VOH3	Output High Voltage	VDD −0.45		V	IOH = −20 mA, Note 3
VOL4	Output Low Voltage		0.45	V	IOL = 12 mA, RAMSET[4] = 0 IOL = 24 mA, RAMSET[4] = 1, Note 4
VOH4	Output High Voltage	2.4		V	IOH = −6 mA, Note 4
VOL5	Output Low Voltage		0.45	V	IOL = 10 mA, RAMSET[7:6] = 00 IOL = 20 mA, RAMSET[7:6] = 01 IOL = 30 mA, RAMSET[7:6] = 10 IOL = 40 ma, RAMSET[7:6] = 11, Note 5
VOH5	Output High Voltage	2.4		V	IOH = −6 mA, RAMSET[7] = 0 IOH = −12 mA, RAMSET[7] = 1, Note 5
VOL6	Output Low Voltage		0.45	V	IOH = 8 mA, Note 6
VOL7	Output Low Voltage		0.45	V	IOH = 24 mA, Note 7
VOL8	Output Low Voltage		0.45	V	IOH = 4 mA, Note 8
ILI	Input Leakage Current	−10	10	µA	VIN = 0 V or VDD, Note 9

DC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min.	Max.	Unit	Conditions
IIL	Input Leakage Current		–500	µA	VIN = 0 V, Note 10
IIH	Input Leakage Current		500	µA	VIN = VDD, Note 11
ILO	Output Leakage Current	–100	100	µA	
IDDSB	Static Power Supply Current		3	mA	
IDDOP	Dynamic Power Supply Current		4	mA/MHz	
CI	Input or I/O Capacitance		10	pF	
CO	Output Capacitance		10	pF	

Notes:
1. Pins: –BUSY386, PEREQ386, –ERROR386, –ROMCS, IRQ13, –CHS0/–MW, –MHS1/–MR, CHM/–IO, –BLKA20, BUSCLK, DMAHLDA, XD7-XD0, SLEEP3-SLEEP1.
2. Pins: –READYO, HRQ, RESCPU, CASBK3-CASBK0, RES387, LBE3-LBE0, –BRDRAM, –DEN, –MDLAT.
3. Pins: CLK2.
4. Pins: –RASBK3- –RASBK0.
5. Pins: MA10-MA0, –RAMW.
6. Pin: –SLP/MISS is an open drain output.
7. Pin: –REFRESH is an open drain output.
8. Pins: SLEEP3-SLEEP1 are open drain outputs.
9. All inputs except those listed in notes 10 and 11.
10. Pins: –ERROR387, –BUSY387, –TRI, W/–R, D/–C, M/–IO, –ADS, A31, A29 and A26 have internal pull ups.
11. Pins: PEREQ387 and WTIRQ have internal pull downs.

VL82C331

ISA BUS CONTROLLER

DESCRIPTION

The VL82C331 ISA Bus Controller replaces several of the LSI controllers used in PC/AT®-type designs with one single 160-lead quad flat pack. The Bus Controller provides the functions of DMA, page address register, timer, interrupt control, Port B logic, slot bus refresh address generation, and real time clock.

The VL82C331 directly drives the refresh addresses onto the AT slot address bus during refresh cycles in response to a refresh cycle command from the System Controller. To avoid problems with sensitive slot bus add-in cards, the VL82C331 features "bus quiet" mode. When no valid slot bus accesses are occurring, the SA bus data and control lines do not change states. Rather, they retain their previous logic state.

Built-in sleep mode features work together with System Controller sleep features to provide a low power system idle state for extension of battery life in portable systems.

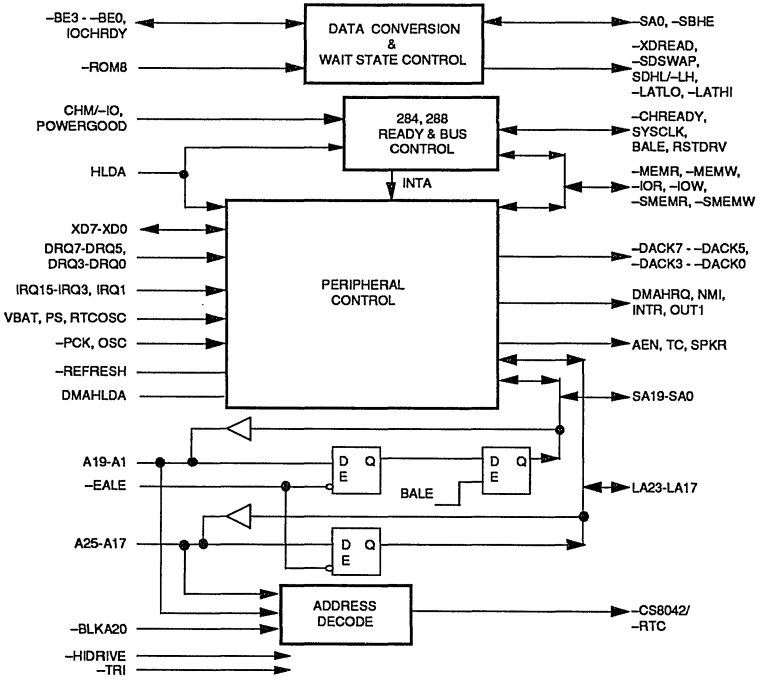
The upgraded DMA channels provide a superset of AT functionality by allowing DMA to the entire 64 Mbyte memory range of the VL82C386 chip set. Additional functionality is provided via DMA wait state, clock, and –MEMR timing programmability.

A –HIDRIVE pin can be externally strapped to provide for 12 or 24 mA drive to the slot bus. If left open, an internal pull-up causes the drive current to default to 12 mA. This allows systems designed with one to four slots to select a lower drive level and reduce bus ringing. A –ROM8 pin selects the bus and bus size to use for BIOS ROM accesses. The choices are 8- or 16-bit wide ROMs.

A three-state test control pin has been added for board level testability.

The VL82C331 features several VLSI Technology megacells, implemented in 1.5-micron CMOS technology, and is intended to work in 286™-, 386™SX-, or 386™DX-based systems with CPU clock speeds up to 33 MHz and bus speeds up to 16 MHz.

BLOCK DIAGRAM



ORDER INFORMATION

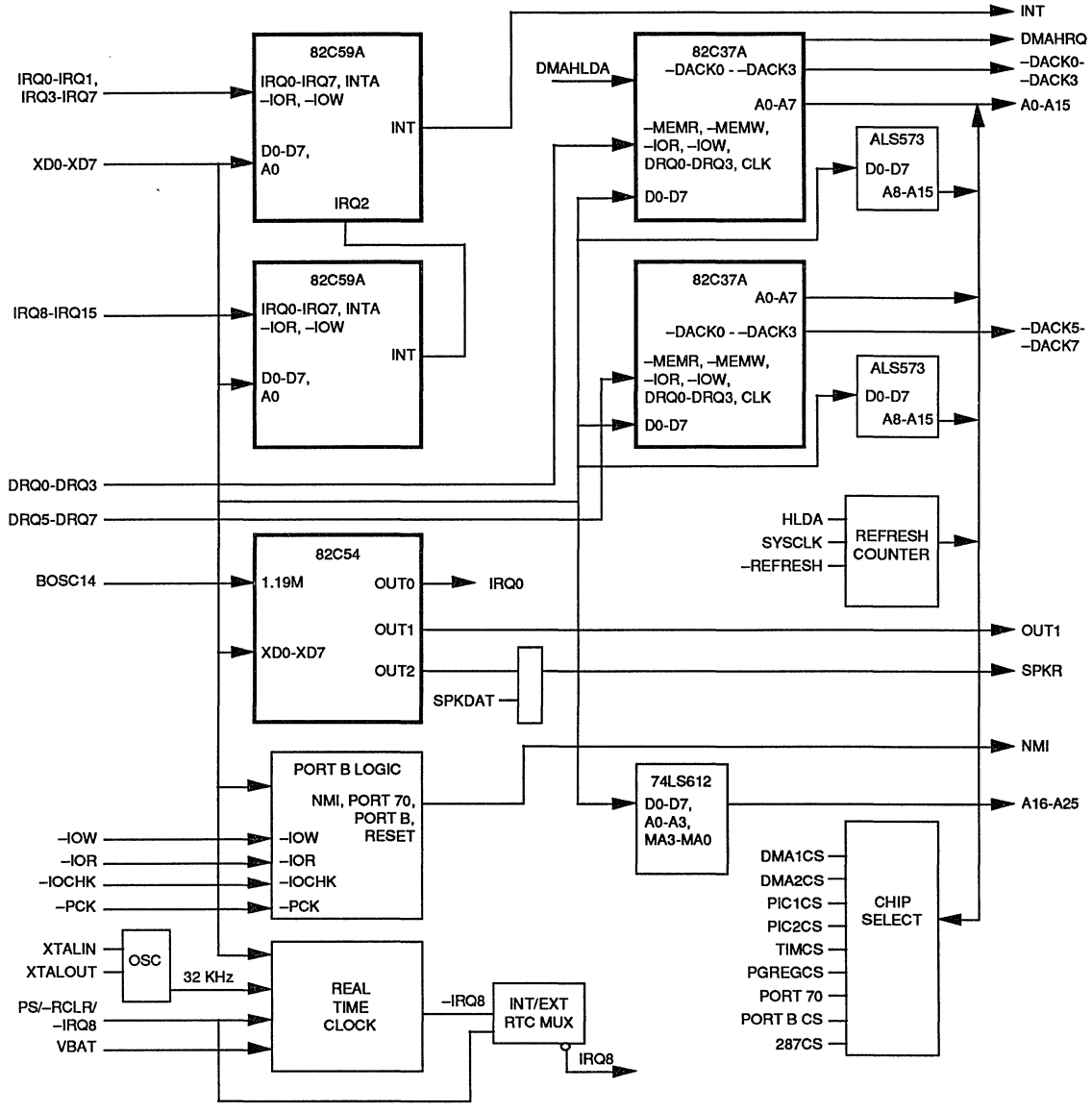
Part Number	Package
VL82C331-FC	Plastic Flat Pack

Note: Operating temperature range is 0°C to +70°C.

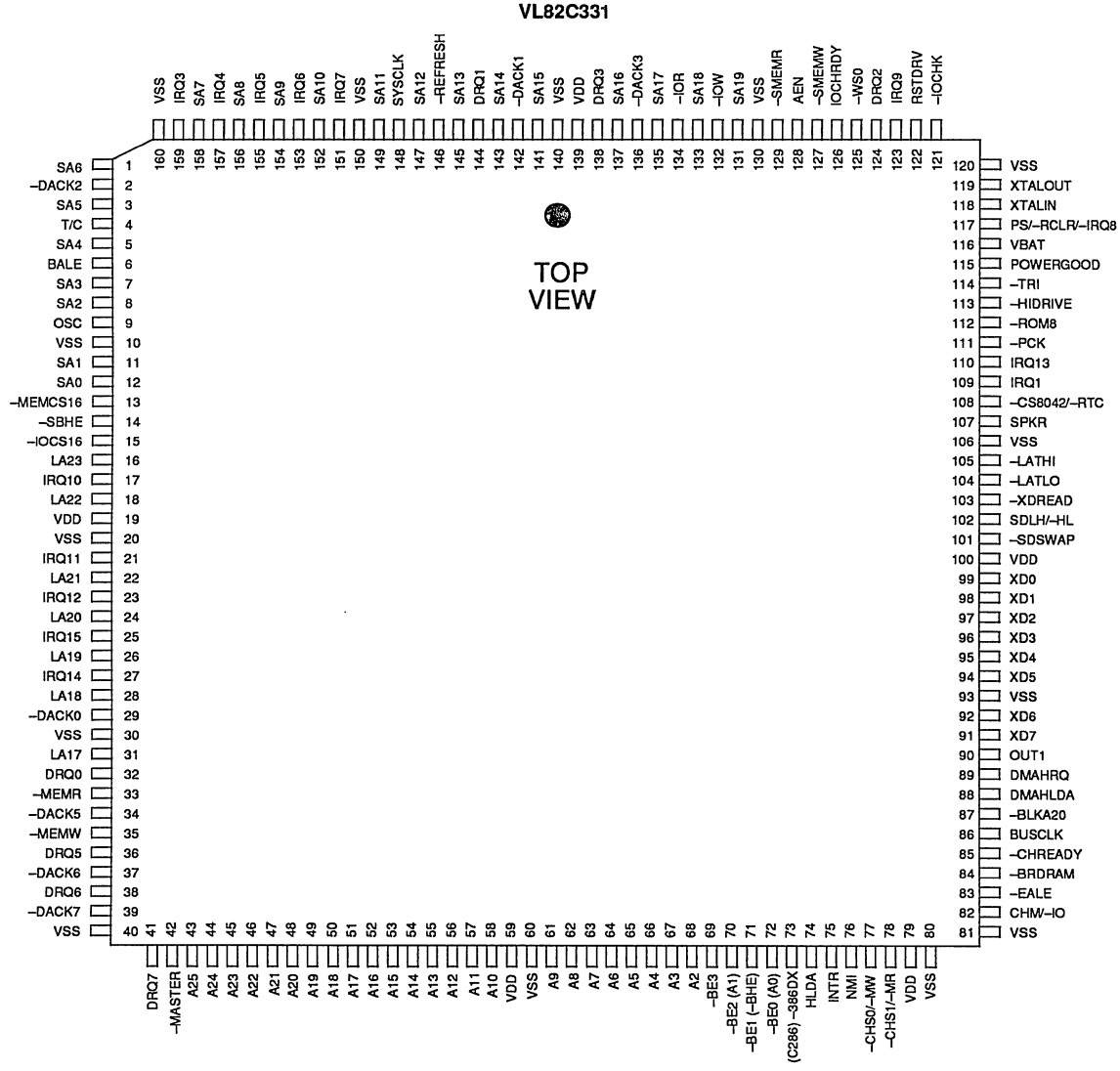
PC/AT is a registered trademark of IBM Corporation.

286, 386SX and 386DX are trademarks of Intel Corporation.

PERIPHERAL CONTROL BLOCK DIAGRAM



PIN DIAGRAM



Pin names surrounded by parenthesis indicate 286/386SX mode.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE			
A25, A24	43, 44	O-TS	Address bus - These pins are outputs during DMA, master, or standard refresh modes. They are high impedance at all other times. A25 and A24 are driven from the alternate 612 registers during DMA and refresh cycles and are driven low during master cycles.
A23-A2	45-58, 61-68	IO-TTL	Address bus - These pins are outputs during DMA, master, or standard refresh modes. They are inputs at all other times. As inputs, they are passed to the SA and LA buses and A15-A2 are used to address I/O registers internal to the bus control chip. As outputs, they are driven from different sources depending on which mode the VL82C331 is in. While in refresh mode, these pins are driven from the 612 and refresh address counter. While in DMA mode, they are driven from the 612 and DMA controller subsection. If the VL82C331 is in master mode, the pins A23-A17 are driven from the inputs LA23-LA17 and the pins A16-A2 are driven from the inputs SA16-SA2.
–BE3	69	IO-TPU	Byte Enable 3, active low - This pin is an output during DMA, master, or standard refresh modes. It is an input at all other times. As an input in 386DX mode, it is decoded along with the other byte enable signals to generate SA1, SA0 and –SBHE. As an output in 386DX mode SA1, SA0, and –SBHE are used to determine the value of –BE3. This pin should be left unconnected when using this part in 286/386SX mode.
–BE2 (A1)	70	IO-TTL	Byte Enable 2, active low, or A1 - This pin has a dual function depending on the state of the (C286) –386DX input. If (C286) –386DX is high (286/386SX mode), then the pin is treated as address bit 1. If (C286) –386DX is low (386DX mode), the pin is treated as –BE2. This pin is an output during DMA, master, or standard refresh modes. It is an input at all other times. As an input in 386DX mode, it is decoded along with the other byte enable signals to generate SA1, SA0 and –SBHE. As an output in 386DX mode, SA1, SA0, and –SBHE are used to determine the value of –BE2. When in 286/386SX mode, it is interpreted as address A1 and passed to SA1. As an output in 286/386SX mode it is driven from the SA1 input.
–BE1 (–BHE)	71	IO-TTL	Byte Enable 1 or Byte High Enable, active low - This pin has a dual function depending on the state of the (C286) –386DX input. If (C286) –386DX is high (286/386SX mode), then the pin is treated as –BHE. If (C286) –386 is low (386DX mode), the pin is treated as –BE1. This pin is an output during DMA, master, or standard refresh modes. It is an input at all other times. As an input in 386DX mode, it is decoded along with the other byte enable signals to generate SA1, SA0, and –SBHE. As an output in 386DX mode, SA1, SA0, and –SBHE are used to determine the value of –BE1. When in 286/386SX mode, it is interpreted as –BHE and passed to –SBHE. As an output in 286/386SX mode, it is driven from the –SBHE input.
–BE0 (A0)	72	IO-TTL	Byte Enable 0, active low, or A0 - This pin has a dual function depending on the state of the (C286) –386DX input. If (C286) –386DX is high (286 mode), then the pin is treated as address bit 0. If (C286) –386DX is low (386DX mode), the pin is treated as –BE0. This pin is an output during DMA, master, or standard refresh modes. It is an input at all other times. As an input in 386DX mode, it is decoded along with the other Byte Enable signals to generate SA1, SA0, and –SBHE. As an output in 386DX mode, SA1, SA0, and –SBHE are used to determine the value of –BE0. When in 286/386SX mode, it is interpreted as A0 and passed to SA0. As an output in 286/386SX mode, it is driven from the SA0 input.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
(C286)–386DX	73	I-TPU	CPU is 286/386SX or 386DX - This pin defines the type of address bus to which the bus controller chip is interfaced. If the pin is tied high, the address bus is assumed to be emulating 286/386SX signals. In this mode, A25, A24, and –BE3 would be left unconnected. The pins –BE2 (A1), –BE1 (–BHE) and –BE0 (A0) would take on the 286/386SX functions. If the pin is tied low, A25, A24 can be used to generate up to 64 Mbyte addressing for DMA, and the byte enable pins will take on the normal 386DX addressing functions. This pin has an internal pull-up to cause the chip to default to 286/386SX mode if left unconnected. This pin is a hard wiring option and must not be changed dynamically during operation. When strapped for 286/386SX mode, the VL82C331 is assumed to be interfaced to the VL82C320 System Controller which in turn may be strapped for 286 or 386SX operation.
HLDA	74	I-TTL	Hold Acknowledge - This is the hold acknowledge pin directly from the CPU. It is used to control direction on address and command pins. When HLDA is low, the VL82C331 is defined as being in the CPU mode. In the CPU mode, the local address bus (A bus) pins are inputs. The system address bus (SA and LA) pins along with the command pins (–MEMR, –MEMW, –IOR and –IOW) are outputs. When HLDA is high, the VL82C331 can be in DMA, refresh, or master modes. In both DMA and refresh modes, the commands and all address buses (A, SA and LA) are outputs. In master mode, the commands and system address bus (SA and LA) pins are inputs and the local address bus (A bus) pins are outputs. The SA bus is passed directly to the A bus except bits 17, 18, and 19 are ignored. LA23-LA17 is passed directly to A23-A17.
INTR	75	O	Interrupt Request - INTR is used to interrupt the CPU and is generated by the 8259 megacells any time a valid interrupt request input is received.
NMI	76	O	Non-Maskable Interrupt - This output is used to drive the NMI input to the CPU. This signal is asserted by either a parity error (indicated by –PCK being asserted after the ENPARCK bit in Port B has been asserted), or an I/O channel error (indicated by –IOCHCK being asserted after the ENIOCK bit in Port B has been asserted). The NMI output is enabled by writing a 0 to bit D7 of I/O port 70h. NMI is disabled on reset.
SYSTEM CONTROLLER INTERFACE			
–CHS0/–MW	77	IO-TTL	Channel Status 0 or active low Memory Write - This input is used along with –CHS1 and CHM/–IO to determine what type of bus cycle the Bus Controller is to perform. This input has the same meaning and timing requirements as the S0 signal for a 286 microprocessor. –CHS0 going active indicates a write cycle unless –CHS1 is also active. When both status inputs are active it indicates an interrupt acknowledge cycle. This input is synchronized to the BUSCLK input. Activation of CPUHLDA reverses this signal to become an output to the System Controller. It is then a –MEMW signal for DMA or bus master access to system memory.
–CHS1/–MR	78	IO-TTL	Channel Status 1 or active low Memory Read - This input is used along with –CHS0 and CHM/–IO to determine the bus cycle type. This input has the same meaning and timing requirements as the S1 signal for a 286 microprocessor. –CHS1 going active indicates a read cycle unless –CHS0 is also active. When both status inputs are active it indicates an interrupt acknowledge cycle. This input is synchronized to the BUSCLK input. Activation of CPUHLDA reverses this signal to become an output to the System Controller. It is then a –MEMR signal for DMA or bus master access to system memory.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
CHM/–IO	82	I-TTL	Channel Memory or active low I/O select - This input is used along with –CHS0 and –CHS1 to determine the bus cycle type. This input has the same meaning and timing requirements as the M/–IO signal for a 286/ 386SX microprocessor. CHM/–IO is sampled anytime –CHS0 or –CHS1 is active. If sampled high, it indicates a memory read or write cycle. If sampled low, an I/O read or write cycle should be executed. This input is synchronized to the BUSCLK input.
–EALE	83	I-TPU	Early Address Latch Enable, active low - This input is used to latch the A23-A2 and Byte Enable signals. The latches are open when –EALE is low and hold their value when –EALE is high. The latched addresses are fed directly to the LA23-LA17 bus to provide more address setup time on the bus before a command goes active. The lower latched addresses are latched again with an internal ALE signal as soon as –CHS0 or –CHS1 is sampled active and fed to the SA19-SA0 and –SBHE outputs. In a 386DX system, this input is connected directly to the –ADS output from the CPU. In a 286/386SX system, this input is connected to the –EALE output from the VL82C320 System Controller.
–BRDRAM	84	I-TTL	On-board DRAM, active low - An input from the System Controller indicating that the on-board DRAM is being addressed.
–CHREADY	85	O	Channel Ready, active low - This output is maintained in the active state when no bus accesses are active. This indicates that the VL82C331 is ready to accept a new command. During normal bus accesses, –CHREADY is negated as soon as a valid bus requested is sampled on the –CHS0 and –CHS1 inputs. It is asserted again to indicate that the VL82C331 is ready to complete the current cycle. The bus command signals are then terminated on the next falling edge of the BUSCLK input.
BUSCLK	86	I-CMOS	Bus Clock - This is the main clock input for the VL82C331. It runs at twice the frequency desired for the SYSCLK output. All inputs are synchronous with the falling edge of this input.
–BLKA20	87	I-TTL	Block A20, active low - This input is used while CPUHLDA is low to force the LA20 outputs low anytime it is active. When –BLKA20 is negated LA20 is generated from A20.
DMAHRQ	89	O	Hold Request - This output is generated by the DMA controller any time a valid DMA request is received. It is connected to the DMAHRQ pin on the System Controller.
DMAHLDA	88	I-TTL	DMA Hold Acknowledge - An input from the System Controller which indicates that the current hold acknowledge state is for the DMA controller or other bus master.
OUT1	90	O	Output 1 - Indicates a refresh request to the System Controller. This is the 15 µsec output of timer channel 1.
ROM INTERFACE			
–ROM8	112	I-TPU	8/16 bit ROM select - This input indicates the width of the ROM BIOS. If –ROM8 is low, the VL82C331 chip generates 8- to 16-bit conversions for ROM accesses. Data buffer controls are generated assuming the ROM is on the MD bus. If –ROM8 is high, data buffer controls are generated assuming 16-bit wide ROMs are on the MD bus.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
BUS INTERFACE			
–IOR	134	IO-TTL	I/O Read, active low - This signal is an input when CPUHLDA is high and –MASTER is low. It is an output at all other times. When CPUHLDA is low, –IOR is driven from the 288 bus controller megacell. When CPUHLDA is high and –MASTER is high, it is driven by the 8237 DMA controller megacells. This pin requires an external 10K ohm pull-up resistor.
–IOW	132	IO-TTL	I/O Write, active low - This signal is an input when CPUHLDA is high and –MASTER is low. It is an output at all other times. When CPUHLDA is low, –IOW is driven from the 288 bus controller megacell. When CPUHLDA is high and –MASTER is high, it is driven by the 8237 DMA controller megacells. This pin requires an external 10K ohm pull-up resistor.
–MEMR	33	IO-TTL	Memory Read, active low - This signal is an input when CPUHLDA is high and –MASTER is low. It is an output at all other times. When CPUHLDA is low, –MEMR is driven from the 288 bus controller megacell. When CPUHLDA is high and –MASTER is high, it is driven by the 8237 DMA controller megacells. This signal does not pulse low for DMA addresses above 16 Mbytes. DMA above 16 Mbytes is only performed to the system board, never to the slot bus. This pin requires an external 10K ohm pull-up resistor.
–MEMW	35	IO-TTL	Memory Write, active low - This signal is an input when CPUHLDA is high and –MASTER is low. It is an output at all other times. When CPUHLDA is low, –MEMW is driven from the 288 bus controller megacell. When CPUHLDA is high and –MASTER is high, it is driven by the 8237 DMA controller megacells. This pin requires an external 10K ohm pull-up resistor.
–SMEMR	129	O-TS	Memory Read, active low - –SMEMR is asserted on memory read cycles to addresses below 1 Mbyte and all refresh cycles. It is three stated for all addresses above 1 Mbyte. This pin requires an external 10K ohm pull-up resistor.
–SMEMW	127	O-TS	Memory Write, active low - –SMEMW is asserted on memory write cycles to addresses below 1 Mbyte. It is three stated for all addresses above 1 Mbyte. This pin requires an external 10K ohm pull-up resistor.
LA23-LA17	16, 18, 22, 24, 26, 28 31	IO-TTL	Latchable Address bus - This bus is an input when CPUHLDA is high and –MASTER is low. It is an output bus at all other times. When CPUHLDA is low, the LA bus is driven by the latched values from the A bus. When CPUHLDA is high and –MASTER is high, the LA bus is driven by the 612 memory mapper for DMA cycles and normal refresh. The LA bus is latched internally with the –EALE input.
SA19-SA17	131, 133, 135	O-TS	System Address bus - This bus is three stated when CPUHLDA is high and –MASTER is low. It is an output bus at all other times. When CPUHLDA is low, the SA bus is driven by the latched values from the A bus. When CPUHLDA is high and –MASTER is high, the SA bus is driven by the 8237 DMA controller megacells or refresh address generator. The SA bus will become valid in the middle of the status cycle generated by the –CHS0 and –CHS1 inputs. They are latched with an internally generated ALE signal.
SA16-SA0	137, 141, 143 145, 147, 149, 152, 154, 156	IO-TTL	System Address bus - This bus an input when CPUHLDA is high and –MASTER is low. It is an output bus at all other times. When CPUHLDA is low, the SA bus is driven by the latched values from the A bus. When CPUHLDA is high and –MASTER is high, the SA bus is driven by the 8237

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
	158, 1, 3, 5, 7, 8, 11, 12		DMA controller megacells or refresh address generator. The SA bus will become valid in the middle of the status cycle generated by the –CHS0 and –CHS1 inputs. They are latched with an internally generated ALE signal.
–SBHE	14	IO-TTL	System Byte High Enable, active low - This pin is controlled the same way as the SA bus. It is generated from a decode of the –BE inputs in CPU mode. It is forced low for 16-bit DMA cycles and forced to the opposite value of SA0 for 8-bit DMA cycles.
–REFRESH	146	IT-OD	Refresh signal, active low - This I/O signal is pulled low whenever a de-coupled refresh command is received from the System Controller. It is used as an input to sense refresh requests from external sources such as the System Controller for coupled refresh cycles or bus masters. It is used internally to clock the refresh address counter and select a location in the memory mapper which drives A23-A17. –REFRESH is an open drain output capable of sinking 24 mA.
SYSCLK	148	O	System Clock - This output is half the frequency of the BUSCLK input. The bus control outputs BALE and the –IOR, –IOW, –MEMR and –MEMW are synchronized to SYSCLK.
OSC	9	I-TTL	Oscillator - This is the buffered input of the external 14.318 MHz oscillator.
RSTDRV	122	O	Reset Drive, active high - This output is a system reset generated from the POWERGOOD input. RSTDRV is synchronized to the BUSCLK input.
BALE	6	O	Buffered Address Latch Enable, active high - A pulse which is generated at the beginning of any bus cycle initiated from the CPU. BALE is forced high anytime CPUHLDA is high.
AEN	128	O	Address Enable - This output goes high anytime the inputs CPUHLDA and –MASTER are both high.
T/C	4	O	Terminal Count - This output indicates that one of the DMA channels terminal count has been reached. This signal directly drives the system bus.
–DACK7- –DACK5, –DACK3 - –DACK0	39, 37, 34, 136, 2, 142, 29	O	DMA Acknowledge, active low - These outputs are the acknowledge signals for the corresponding DMA requests. The active polarity of these lines is set active low on reset. Since the 8237 megacells are internally cascaded together, the polarity of the –DACK signals must not be changed. This signal directly drives the system bus.
DRQ7-DRQ5 DRQ3-DRQ0	41, 38, 36, 138, 124, 144, 32	I-TSPU	DMA Request - These asynchronous inputs are used by an external device to indicate when they need service from the internal DMA controllers. DRQ0-DRQ3 are used for transfers from 8-bit I/O adapters to/from system memory. DRQ5-DRQ7 are used for transfers from 16-bit I/O adapters to/from system memory. DRQ4 is not available externally as it is used to cascade the two DMA controllers together.
IRQ15-IRQ9 IRQ7-IRQ3, IRQ1	25, 27, 110, 23, 21, 17, 123, 151, 153, 155, 157, 159, 109	I-TSPU	Interrupt Request - These are the asynchronous interrupt request inputs for the 8259 megacells. IRQ0 and IRQ2 are not available as external inputs to the chip, but are used internally. IRQ0 is connected to the output of the 8254 counter 0. IRQ2 is used to cascade the two 8259 megacells together. All IRQ input pins are active high.
–MASTER	42	I-TTL	Master, active low - This input is used by an external device to disable the internal DMA controllers and get access to the system bus. When asserted it indicates that an external bus master has control of the bus.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–MEMCS16	13	I-TTL	Memory Chip Select 16 bit - This input is used to determine when a 16-bit to 8-bit conversion is needed for CPU accesses. A 16 to 8 conversion is done anytime the Sytem Controller requests a 16-bit memory cycle and –MEMCS16 is sampled high.
–IOCS16	15	I-TTL	I/O Chip Select 16 bit - This input is used to determine when a 16-bit to 8-bit conversion is needed for CPU accesses. A 16 to 8 conversion is done anytime the System Controller requests a 16-bit I/O cycle and –IOCS16 is sampled high.
–IOCHK	121	I-TTL	I/O Channel Check, active low - This input is used to indicate that an error has taken place on the I/O bus. If I/O checking is enabled, an –IOCHK assertion by a peripheral device generates an NMI to the processor. The state of the –IOCHK signal is read as data bit D6 of the Port B register.
IOCHRDY	126	I-TTL	I/O Channel Ready - This input is pulled low in order to extend the read or write cycles of any bus access initiated by the CPU, DMA controllers or refresh controller. The default number of wait states for cycles initiated by the CPU are four wait states for 8-bit peripherals, one wait state for 16-bit peripherals and three wait states for ROM cycles. One DMA wait state is inserted as the default for all DMA cycles. Any peripheral that cannot present read data, or strobe-in write data in this amount of time must use –IOCHRDY to extend these cycles.
–WS0	125	I-TTL	Wait State 0, active low - This input is pulled low by a peripheral on the S bus to terminate a CPU controlled bus cycle earlier than the default values defined internally on the chip.
POWERGOOD	115	I-TSPU	System power on reset - This input signals that power to the board is stable. A Schmitt-trigger input is used. This allows the input to be connected directly to an RC network.
PERIPHERAL INTERFACE			
–CS8042/–RTC	108	O	Chip Select for 8042, active low - This output is active any time an SA address is decoded at 60h or 64h. It is intended to be connected to the chip select of the keyboard controller. If BUSCTL[6]=1, this pin is also active for RTC accesses at 70h and 71h. This is for use when the internal RTC is disabled and an external RTC is used.
XTALIN	118	I-CMOS	Crystal Input - An internal oscillator input for the real time clock crystal. It requires a 32.768 KHz external crystal or stand-alone oscillator.
XTALOUT	119	O	Crystal Output - An internal oscillator output for the real time clock crystal. See XTALIN. This pin is a no connect when an external oscillator is used.
PS/–RCLR/ –IRQ8	117	I-TSPU	Power Sense, active high - Used to reset the status of the Valid RAM and Time (VRT) bit. This bit is used to indicate that the power has failed, and that the contents of the RTC may not be valid. This pin is connected to an external RC network. When BUSCTL[6]=1, this pin becomes –IRQ8 input for use with an external RTC.
VBAT	116	I	Voltage Battery - Connected to the RTC hold-up battery.
SPKR	107	O	Speaker - This output drives an externally buffered speaker. This signal is created by gating the output of timer 2. Bit 1 of Port B, 61H, is used to enable the speaker output, and bit 0 is used to gate the output of the timer.
DATA BUFFER INTERFACE			
XD7-XD0	91, 92, 94-99	IO-TTL	Peripheral data bus - The bidirectional X data bus outputs data on an INTA cycle or I/O read cycle to any valid address within the VL82C331. It is configured as an input at all other times.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–SDSWAP	101	O	System Data Swap, active low during some 8-bit accesses - It indicates that the data on the SD bus must be swapped from low byte to high byte or vice versa depending on the state of the SDLH/–HL pin. –SDSWAP is active for 8-bit DMA cycles when an odd address access occurs for data more than one byte wide. For non-DMA accesses, –SDSWAP is active for any bus cycle to an 8-bit peripheral that is addressing the odd byte.
SDLH/–HL	102	O	System Data Low to High, or High to Low - This signal is used to determine which direction data bytes must be swapped when –SDSWAP is active. When SDLH/–HL is high, it indicates that data on the low byte must be transferred to the high byte. When SDLH/–HL is low, it indicates that data on the high byte must be transferred to the low byte. SDLH/–HL is low for 8-bit DMA memory read cycles. For non-DMA accesses, SDLH/–HL is low for any memory write or I/O write when –SBHE is low. SDLH/–HL is high at all other times.
–XDREAD	103	O	Peripheral Data Read - This output is active low any time an INTA cycle occurs or an I/O read occurs to the address space from 0000h to 00F7h, which is defined as being resident on the peripheral bus.
–LATLO	104	O	Latch Low byte - This output is generated for all I/O read and memory read bus accesses to the low byte. It is active with the same timing as the read command and returns high at the same time as the read command. This signal latches the data into the data buffer chip so that it can be presented to the CPU at a later time. This step is required due to the asynchronous interface between the System Controller and VL82C331.
–LATHI	105	O	Latch High byte - This output is generated for all I/O read and memory read bus accesses to the high byte. It is active with the same timing as the read command and returns high at the same time as the read command. This signal latches the data into the data buffer chip so that it can be presented to the CPU at a later time. This step is required due to the asynchronous interface between the System Controller and VL82C331.
–PCK	111	I-TPU	Parity Check input, active low with pull-up - Indicates that a parity error has occurred in the on-board memory array. Assertion of this signal (if enabled) generates an NMI to the processor. The state of the –PCK signal is read as data bit D7 of the Port B register.
–HIDRIVE	113	I-TPU	High Drive Enable - This pin is a wire strap option. When this input is low, all bus drivers defined with an IOL spec of 24 mA will sink the full 24 mA of current. When this input is high, all pins defined as 24 mA have the output low drive capability cut in half to 12 mA.
TEST MODE PIN			
–TRI	114	I-TPU	Three-state - This pin is used to control the three-state drive of all outputs and bidirectional pins on the chip. If this pin is pulled low, all pins on the chip except XTALOUT are in a high impedance mode. This is useful during system test when test equipment or other chips drive the signals or for hardware fault tolerant applications. –TRI has an internal pull-up.
POWER AND GROUND PINS			
VDD	19, 59, 79, 100, 139	PWR	Power connection, nominally +5 volts. These pins should each have 0.1 µF bypass capacitors.
VSS	10, 20, 30, 40, 60, 80, 81, 93, 106, 120, 130, 140, 150, 160	GND	Ground connection, 0 volts.

SIGNAL TYPE LEGEND

Signal Code	Signal Type
I-TTL	TTL level input
I-TPU	Input with 30k ohm pull-up resistor
I-TSPU	Schmitt-trigger input with 30k ohm pull-up resistor
I-CMOS	CMOS level input
IO-TTL	TTL level input/output
IO-TPU	TTL level input/output with 30k ohm pull-up resistor
IT-OD	TTL level input/open drain output
O	CMOS and TTL level compatible output
O-TS	Three-state level output
GND	Ground
PWR	Power

FUNCTIONAL DESCRIPTION

DETAILED SUBSYSTEM SPECIFICATION

The sections that follow cover detailed operational information for the various logical groupings of VL82C331 ISA Bus Controller subsystems. In most of these sections, the effect of any applicable configurable elements that can be controlled via indexed configuration registers is discussed at length. Operation of these registers is repeated in summary form in the "Configuration Register Operational Summary" section. However, some lesser configurable functions are described only in this section. Do not assume that the information in that section is discussed elsewhere.

MAJOR LOGIC BLOCK CHIP SELECT GENERATION

The VL82C331 ISA Bus Controller utilizes six VLSI Technology megacells; two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 counter/timer, and one real time clock. Programmable I/O access is required for these and other internal logic blocks. The logic block chip select subsection consists of decodes of the signals –MASTER, CPUHLDA and the address bus A15-A0. This decode is used to generate the chip select signals to each major logic block within the Bus Controller.

Data Port 00EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
ROMDMA	ROM Wait States		**8-Bit DMA Wait States**		**16-Bit DMA Wait States**		**DMA Clock**	**MEMR Timing**

The DMA subsection consists of two 8237 megacells, two 8-bit latches to hold the middle range address bits during a DMA cycle and 1.25 74LS612 page register equivalents to generate the upper range address bits during a DMA operation. The DMA subsection also has logic to allow separate programming of the number of wait states for 8- and 16-bit DMA cycles. Defaults are standard AT-compatible wait states. The timing for the leading edge of the –MEMR signal is also programmable. The DMA subsection provides a total of seven external DMA channels. Four of these channels are used for 8-bit I/O adapters and the other three are used for 16-bit I/O adapters. All channels are capable of addressing all memory locations in a 64 Mbyte address space.

The interrupt controller subsection consists of two 8259 megacells cascaded together to allow for 15 possible interrupt sources. IRQ2 is used internally. –IRQ8 is available externally only when the internal RTC is disabled.

The counter/timer subsection contains a single 8254 megacell. This megacell has three internal counters. All of the counters are driven by a common clock input. The output of counter zero is routed to the interrupt controller subsection to be used as interrupt request zero. The output from counter one drives the OUT1 pin to initiate refresh cycles. Counter two's output is gated with a signal from the Port B register and is then output as SPKR to drive the speaker.

The RTC megacell (82C018) is a direct replacement for the 146818A real time clock component. Clock functions include the following:

- Time of day clock
- Alarm function
- 100 year calendar function
- Programmable periodic interrupt output
- 114 bytes of User RAM

TABLE 1. A15-A0 ADDRESS DECODES

A15-8	A7	A6	A5	A4	A3	A2	A1	A0	Address	Chip Select Generated
0	0	0	0	0	X	X	X	X	0000-00F	DMA1 (8237)
0	0	0	1	X	X	X	X	X	0020-03F	Interrupt 1 (8259)
0	0	1	0	0	0	0	X	X	0040-043	Counter (8254)
0	0	1	1	0	X	X	X	1	0061-06F	Port B (Odd Only)
0	0	1	1	1	0	0	0	0	0070	NMI Logic
0	0	1	1	1	0	0	0	X	0070-071	Real Time Clock Access Ports
0	1	0	0	0	X	X	X	X	0080-08F	DMA Page Registers
0	1	0	0	1	0	0	1	0	0092	Port A*
0	1	0	1	X	X	X	X	X	00A0-0BF	Interrupt 2 (8259)
0	1	1	0	X	X	X	X	X	00C0-0DE	DMA2
0	1	1	1	X	X	X	X	X	00E0-0EF	Configuration Registers*
1	1	1	1	X	X	X	X	X	00F0-0FF	Coprocessor CS and RESET*
0	0	1	1	0	0	X	0	0	60, 64	–CS8042

* These entries are shown for completeness only. They are decoded and controlled by the System Controller except for ECh and EDh, which are also used by the V82C331's configuration registers.

Notes: 1. Address bits A15-A0 are used to generate chip selects for each of the individual megacells. A map of the address decode is shown in Table 1.

2. For all the address decodes shown, the inputs CPUHLDA or –MASTER must be low to generate a megacell chip select.

DMA SUBSECTION

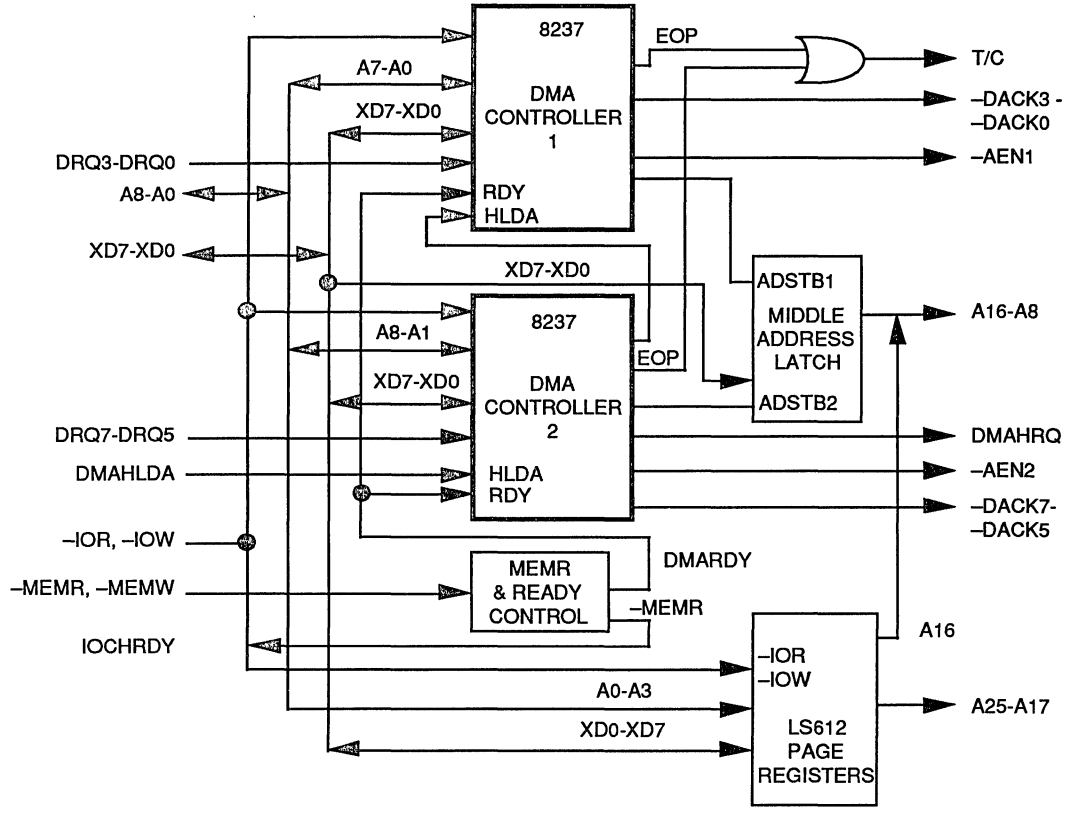
The DMA subsection controls DMA transfers between an I/O channel and on- or off-board memory. It generates a hold request to the CPU when an I/O channel requests a DMA operation. Once the hold has been acknowledged, the DMA controller will drive the CPU and the slot address buses. DMAs can occur over the full 16M range available on the slot bus and the 64M range of system board DRAM and drive the appropriate bus command signals depending on whether the DMA is a memory read or write. The DMA controllers are 8237-compatible. Internal latches are provided for latching the middle address bits output by the 8237 megacells on the data bus, and 1.25 74LS612 memory mappers are provided to generate the upper address bits. Since a single 74LS612 is only capable of accessing 16 Mbytes in an AT-compatible fashion, two additional bits are required to extend the architecture for a 64 Mbyte system. Therefore, an extra 1/4 of a 74LS612 is implemented. This is discussed in the section "Page Registers" and is functional only when used with the VL82C386 chip set.

DMA Controllers

The Bus Controller supports seven DMA channels using two 8237 equivalent megacells capable of running at SYSCLK or SYSCLK/2. This option is programmable via the indexed configuration register, ROMDMA. DMA controller 1 contains channels 0 through 3. These channels support 8-bit I/O adapters. Channels 0 through 3 are used to transfer data between 8-bit peripherals and 8- or 16-bit memory. A full 26-bit address is output for each channel so they can all transfer data throughout the entire 64 Mbyte system address space when used with the VL82C386 chip set. Each channel can transfer data in 64 kilobyte pages.

DMA controller 2 contains channels 4 through 7. Channel 4 is used to cascade DMA controller 1, so it is not available externally. Channels 5 through 7 support 16-bit I/O adapters to transfer data between 16-bit I/O adapters and 16-bit system memory. A full 26-bit address is output for each channel so they can all transfer data throughout the entire 64 Mbyte system address space. Each channel can transfer data in 128 kilobyte pages. Channels 5, 6 and 7 are meant to transfer 16-bit words only and cannot address odd bytes in system memory.

FIGURE 1. DMA SUBSECTION BLOCK DIAGRAM



DMA Controller Registers
The 8237 megacells can be programmed any time CPUHLDA is inactive. Table 2 lists the addresses of all registers which can be read or written in the 8237 megacells. Addresses under DMA2 are for the 16-bit DMA channels and DMA1 corresponds to the 8-bit channels. When writing to a channel's address or word count register, the data is written into both the base register and current register simultaneously. When reading a channel's address or word count register only, the current address or word count can be read. The base address and base word count are not accessible for reading.

The address and word count registers for each channel are 16-bit registers. The value on the data bus is written into the upper or lower byte depending on the state of the internal addressing flip-flop. This flip-flop can be cleared by the clear byte pointer flip-flop command. After this command, the first read/write to an address or word count register will read/write to the low byte of the 16-bit register and the byte pointer flip-flop will toggle to a one. The next read/write to an address or word count register will read/write to the high byte of the 16-bit register and the byte pointer flip-flop will toggle back to a zero. Refer to the 8237 data sheet for more information on programming the 8237 megacell.

The 8237 DMA controller megacells allow the user to program the active level (low or high) of the DREQ and –DACK signals. Since the two megacells are cascaded together internally on the chip, these signals should always be programmed with the DREQ signals active high and the –DACK signals active low.

When programming the 16-bit channels (channels 5, 6 and 7), the address which is written to the base address register must be the real address divided by two. Also, the base word count for the 16-bit channels is the number of 16-bit words to be transferred, not the number of bytes as is the case for the 8-bit channels.

It is recommended that all internal locations, especially the mode registers, in the 8237 megacells be loaded with some valid value. This should be done even if the channels are not used.

Middle Address Bit Latches
The middle DMA address bits are held in an internal 8-bit register. The DMA controller will drive the value to be loaded onto the internal data bus and then issue an address strobe signal to latch the data bus value into this register. An address strobe is issued at the beginning of a DMA cycle and any time the lower 8-bit address increments across the 8-bit subpage boundary during block transfers. This register cannot be written to or read externally. It is loaded only from the address strobe signals from the megacells and the outputs go only to the A16-A8 pins.

TABLE 2. 8237 READ/WRITE ADDRESS

Hex Address		
DMA2	DMA1	Register Function
00C0	0000	Channel 0 Base and Current Address Register
00C2	0001	Channel 0 Base and Current Word Count Register
00C4	0002	Channel 1 Base and Current Address Register
00C6	0003	Channel 1 Base and Current Word Count Register
00C8	0004	Channel 2 Base and Current Address Register
00CA	0005	Channel 2 Base and Current Word Count Register
00CC	0006	Channel 3 Base and Current Address Register
00CE	0007	Channel 3 Base and Current Word Count Register
00D0	0008	Read Status Register/Write Command Register
00D2	0009	Write Request Register
00D4	000A	Write Single Mask Register Bit
00D6	000B	Write Mode Register
00D8	000C	Clear Byte Pointer Flip-flop
00DA	000D	Read Temporary Register/Write Master Clear
00DC	000E	Clear Mask Register
00DE	000F	Write All Mask Register Bits

Page Registers

Data Port 0EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
612AXS (82)	Enable FF	4XX Enable	1	1	1	1	1	FF PTR

An extended 74LS612 cell is used in the Bus Controller to generate the page registers for each DMA channel. The page registers provide the upper address bits during a DMA cycle. DMA addresses do no increment or decrement across page boundaries. Page boundaries for the 8-bit channels (channels 0 through 3) are every 64 kilobytes and page boundaries for the 16-bit channels (channels 5, 6 and 7) are every 128 kilobytes. There are a total of 16 8-bit registers and eight 2-bit registers in the extended 612 megacell.

The indexed configuration register ROMDMA is used to program the extended DMA features. In addition to the description below, see the section "Configuration Register Operational Summary" for more information. Bit 7 enables the extended DMA functions. The VL82C386 chip set contains a superset of the PC/AT DMA design which allows full access to the entire 64M range of the VL82C386 chip set. In order to do this, a second 612 memory mapper subset is added to allow access to the two required upper address bits, A24 and A25. When bit 7 = 0, the extended functionality is disabled. Any previously stored values for A24 and A25 are disabled and both bits are forced to 0. This mode is fully compatible with the PC/AT-standard. When bit 7 = 1, the extended mode is enabled. A24 and A25 can be set in the memory mapper page register by setting bit 0 of this register to 1 and writing the data to the same address used for the lower page register byte. Resetting bit 0 to 0 allows access to the lower page registers. See the bit 0 discussion below for more detail. At power-on-reset, this bit defaults to 0 for complete AT-compatibility.

Bit 6 enables EISA compatibility when set to 1 by allowing access to the upper DMA page address bits at I/O addresses 4XX in accordance with Table 3. When set to 1, it also enables the extended DMA system and allows the contents of the upper page register's A24 and A25 to be used.

Bit 0 allows access to either the lower address bits, A16-A23 of the DMA page register when set to 0 or allows access to the upper address bits A24 and A25 when set to 1. The state of this bit has no effect unless bit 7 of this register has been previously set to 1. As an example, when bit 7 = 1 and bit 0 = 0, a write to address 08Ah will update A16-A23 in the lower DMA page register space. Bit 0 auto-increments on any write to the DMA register space between 0080h and 008Fh. Therefore, if the next operation is a write to 008Ah, the upper address bits A24 and A25 are updated. The next access to this register space automatically accesses the lower byte of that address. Whenever D7 = 0, this bit is reset and held at logic 0. This bit is reset to 0 on POR.

These registers must be written to select the correct page for each DMA channel before any DMA operations are performed. The other address locations between 0080h and 008Fh not shown in Table 4 and are not used by the DMA channels, but can be read or written to by the CPU. Address 008Fh (and 0048Fh) is used to drive a value onto the upper address bits A25-A17 of the CPU's address bus during a refresh cycle.

Important Difference for VL82C286 Chip Set Users

The VL82C286 chip set for use in 286- and 386SX-based systems has a 32 Mbyte limit for its largest memory map. However, only the standard DMA operation below 16 Mbytes is supported. When the Bus Controller is strapped for 286/386SX mode via no connect or external pull-up on the (C286) –386DX pin, bits 6 and 7 of the 612AXS indexed register are held low. This disables extended DMA mode. Attempts to write a 1 to these bits via software has no effect and subsequent reads of the bits will return a 0.

TABLE 3. DMA PAGE REGISTER ACCESS OPTION 1

A25-A24 Address		A23-A16 Address	DMA Channel
B6=1	B6=0	B6=X	
0487h	NA	0087h	0
0483h	NA	0083h	1
0481h	NA	0081h	2
0482h	NA	0082h	3
048Bh	NA	008Bh	5
0489h	NA	0089h	6
048Ah	NA	008Ah	7
048Fh	NA	008Fh	–REFRESH

TABLE 4. DMA PAGE REGISTER ACCESS OPTION 2

A25-A24 Address	A23-A16 Address	DMA Channel
B0=1, B7=1	B0=0, B7=1	
0087h	0087h	0
0083h	0083h	1
0081h	0081h	2
0082h	0082h	3
008Bh	008Bh	5
0089h	0089h	6
008Ah	008Ah	7
008Fh	008Fh	–REFRESH

Address Generation

The DMA addresses are set up such that there is an upper address portion, used to select a specific page, a middle address portion used to select a block within the page and a lower address portion.

The upper address portion is generated by the page registers, in the 74LS612 equivalent megacell. The page registers for each channel must be set up by the CPU before a DMA operation. DMA addresses do not increment or decrement across page boundaries. Page sizes are 64 kilobytes for 8-bit channels (channels 0 through 3) and 128 kilobytes for 16-bit channels (channels 5, 6 and 7). The DMA page register values are output on A25-A16 for 8-bit channels and A25-A17 for 16-bit channels.

The middle address portion, used to select a block within the page, is generated by the 8237 megacells at the beginning of a DMA operation and any time the DMA address increments or decrements through a block boundary. Block sizes are, 256 bytes for 8-bit channels (channels 0 through 3) and 512 bytes for 16-bit channels (channels 5, 6 and 7). This middle address portion is output by the 8237 megacells onto the internal data bus during state S1. The internal middle address bit latches will latch this value in. The middle address bit latches are output on A15-A8 for 8-bit channels and A16-A9 for 16-bit channels.

The lower address portion is generated directly by the 8237 megacells during DMA operations. The lower address bits are output on A7-A0 for 8-bit channels and A8-A1 for 16-bit channels. A0 and –SBHE are forced low during 16-bit DMA operations. –SBHE is forced to the opposite value of A0 for 8-bit DMA.

–SBHE is configured as an output during all DMA operations and will be driven as the inversion of A0 during 8-bit DMA cycles and forced low for all 16-bit DMA cycles.

TABLE 5. DMA ADDRESSING FOR SLOT BUS ACCESSES

Outputs from 74LS612 Page Registers	Outputs from Middle Address Latches	Address Outputs from 8237	8-Bit DMA Address Bits	16-Bit DMA Address Bits
M9				
M8				
M7			LA23	LA23
M6			LA22	LA22
M5			LA21	LA21
M4			LA20	LA20
M3			S/LA19	S/LA19
M2			S/LA18	S/LA18
M1			S/LA17	S/LA17
M0			SA16	
	D7		SA15	SA16
	D6		SA14	SA15
	D5		SA13	SA14
	D4		SA12	SA13
	D3		SA11	SA12
	D2		SA10	SA11
	D1		SA9	SA10
	D0		SA8	SA9
		A7	SA7	SA8
		A6	SA6	SA7
		A5	SA5	SA6
		A4	SA4	SA5
		A3	SA3	SA4
		A2	SA2	SA3
		A1	SA1	SA2
		A0	SA0	SA1
		VSS		SA0
		–A0	–SBHE	
		VSS		–SBHE

Table 5 shows the mapping from the DMA subsystem signals to slot bus signals for both the VL82C386 and VL82C286 chip sets. For the latter chip set, the equivalent signals are also driven onto the local address bus. Table 6 shows the mapping of DMA subsystem signals to local address bus signals for the VL82C386 system.

Ready Control

The ready input to each of the 8237 megacells is driven from the same source within the ready control logic. The Bus Controller ready control logic forces the preprogrammed number of wait states on every DMA transfer. POR defaults to one wait state for both 8- and 16-bit transfers. Other options can be programmed after POR in the indexed configuration register ROMDMA. The external signal IOCHRDY goes into the ready control logic to further extend transfer cycles if needed. To add extra wait states, an external device should pull IOCHRDY low within the setup time before the second phase of the internal DMA clock no later than the last forced wait state cycle. The current DMA cycle will then be extended by inserting wait states until IOCHRDY is returned high. IOCHRDY going high must meet the setup time at the beginning of a wait state cycle or an extra wait state will be inserted before the DMA controller transitions to state S4.

External Cascading

An external DMA controller or bus master can be attached to an AT-compatible design through the VL82C331's DMA controllers. To add an external DMA controller, one of the seven available DMA channels must be programmed in cascade mode. That channels DRQ signal should then be connected to the external DMA controller's HRQ output. The corresponding –DACK signal for that channel should be connected to the external DMA controller's HLDA input. When one of the seven channels is programmed in cascade mode and that channel is acknowledged, the Bus Controller will not drive the data bus, the command signals or the address bus.

TABLE 6. DMA ADDRESSING IN 386DX MODE

Outputs from 74LS612 Page Registers	Outputs from Middle Address Latches	Address Outputs from 8237	8-Bit DMA Address Bits	16-Bit DMA Address Bits
M9			A25	A25
M8			A24	A24
M7			A23	A23
M6			A22	A22
M5			A21	A21
M4			A20	A20
M3			A19	A19
M2			A18	A18
M1			A17	A17
M0			A16	
	D7		A15	A16
	D6		A14	A15
	D5		A13	A14
	D4		A12	A13
	D3		A11	A12
	D2		A10	A11
	D1		A9	A10
	D0		A8	A9
		A7	A7	A8
		A6	A6	A7
		A5	A5	A6
		A4	A4	A5
		A3	A3	A4
		A2	A2	A3
		A1	*	A2
		A0	*	**

*Byte Enables –BE0- –BE3 Controlled:

Case	A0	A1	–BE3	–BE2	–BE1	–BE0
1	0	0	High	High	High	Low
2	0	1	High	High	Low	High
3	1	0	High	Low	High	High
4	1	1	Low	High	High	High

**Byte Enables –BE0- –BE3 Controlled:

Case	A0	–BE3	–BE2	–BE1	–BE0
1	0	High	High	Low	Low
2	1	Low	Low	High	High

An external device can become a bus master and control the system address, data and command buses in much the same manner. One of the external channels must be programmed in cascade mode. The external device then asserts the DRQ line for that channel. When that channel's –DACK line goes active, the external device can then pull the –MASTER signal low. As in the DMA controller cascading, the VL82C331 does not drive the address, data and command signals while the cascaded channel's –DACK signal is active.

TABLE 7. DMA ADDRESSING SYSTEM BOARD MEMORY IN 286/386SX MODE

Outputs from 74LS612 Page Registers	Outputs from Middle Address Latches			
		Address Outputs from 8237		
			8-Bit DMA Address Bits	
				16-Bit DMA Address Bits
M9				
M8				
M7			A23	A23
M6			A22	A22
M5			A21	A21
M4			A20	A20
M3			A19	A19
M2			A18	A18
M1			A17	A17
M0			A16	
	D7		A15	A16
	D6		A14	A15
	D5		A13	A14
	D4		A12	A13
	D3		A11	A12
	D2		A10	A11
	D1		A9	A10
	D0		A8	A9
		A7	A7	A8
		A6	A6	A7
		A5	A5	A6
		A4	A4	A5
		A3	A3	A4
		A2	A2	A3
		A1	A1	A2
		A0	A0/–BLE	A1
		VSS		A0/–BLE
		–A0	–BHE	
		VSS		–BHE

Programming DMA Options

Data Port 0EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
ROMDMA (81)	ROM Wait States		8 Bit DMA Wait States		16 Bit DMA Wait States		DMA Clk	MEMR Timing

The original PC/AT DMA specification is lacking in the true speed one normally associates with DMA activity. For compatibility, the Bus Controller fully supports that specification as its POR defaults. However, a variety of programmable options are provided in order to enhance DMA performance, if desired. The extended DMA support for 64 Mbyte memory space in the VL82C386 chip set has previously been addressed in the "Page Registers" section. In the following sections, programmable wait state, DMA clock, and –MEMR timing are discussed. Actual programming of the ROMDMA registers in order to effect the desired system performance changes is covered in the "Configuration Register Operational Summary" section.

DMA Wait States
Zero, one, or two wait states can be independently programmed for 8-bit and 16-bit DMA transfers. (Default = one wait state.)

DMA Clock
The DMA clock can be programmed to occur at the normal SYSCLK/2 rate (bit 1 = 0) or at SYSCLK rate (bit 1 = 1). (Default = 0)

–MEMR Delay
To maintain an AT-compatible design, the VL82C331 POR default inserts a one DMA clock cycle delay in the falling edge of the –MEMR signal. –MEMR will go low one DMA clock later than the –MEMR signal coming out of the 8237 megacell. The rising edge is not altered and will go high at the same time the –MEMR signal from the megacell goes high. This maybe reprogrammed to remove this one clock cycle delay on the falling edge of –MEMR by setting bit 0 of ROMDMA to a 1. (Default = 0)

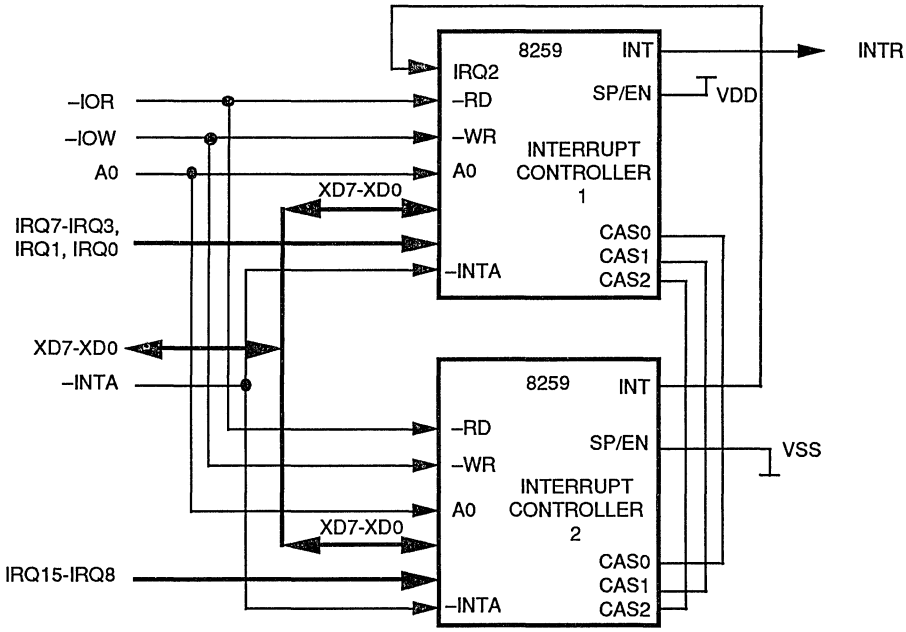
INTERRUPT CONTROLLER SUBSECTION
The interrupt controller subsection is made up of two 8259 megacells with eight interrupt request lines each for a total of 16 interrupts. The two megacells are cascaded internally on the VL82C331 and two of the interrupt request inputs are connected to internal circuitry. This nominally allows a total of 13 external interrupt requests or 14 when the internal RTC is disabled.

All external interrupt request signals have an internal pull-up resistor to eliminate noise on unconnected request pins.

The following interrupt request signals are different from the standard interrupt request in some way.

IRQ0 This interrupt is connected to the OUT0 of the 8254 megacell and is not available as an external input.

FIGURE 2. INTERRUPT CONTROLLER BLOCK DIAGRAM



IRQ2 IRQ2 is used to cascade the two 8259 megacells together and is not available as an external input.

–IRQ8 –IRQ8 input is internally connected to the real time clock megacell's interrupt pin when bit 6 of configuration register BUSCTL=0. When BUSCTL[6] is set to 1, the Interrupt Controller's –IRQ8 input pin is connected to the VL82C331's pin 117 for connection to the –IRQ pin of an external RTC.

A typical interrupt sequence would be as follows. Any unmasked interrupt will generate the INTR signal to the CPU. The interrupt controller megacells will then respond to the –INTA pulses from the CPU. On the first –INTA cycle the cascading priority is resolved to determine which of the two 8259 megacells will output the interrupt vector onto the data bus. On the second –INTA cycle the appropriate 8259 megacell will drive the data bus with the correct interrupt vector for the highest priority interrupt.

Because the two megacells are cascaded internally on the VL82C331, they should never be programmed to operate in the buffered mode. See the section "ISA Bus Controller/System Controller Interchip Communication" for special use of interrupt control during sleep mode.

Interrupt Controller Registers
The internal registers of the 8259 megacells are written to in the same way as in the standard part. Table 8 shows the correct addressing for each of the 8259 registers.

Before normal operation can begin, each 8259 megacell must follow an initialization sequence. The sequence is started by writing Initialization Command Word 1 (ICW1). After ICW1 has been written, the 8259 megacell expects the next writes to follow in the sequence ICW2, ICW3 and ICW4 if it is needed. The Operation Control Words (OCW) can be written at any time after initialization.

In the standard 8259 megacell, ICW3 is optional. But since the two 8259's in this chip are cascaded together they should always be programmed in cascade mode and ICW3 will always be needed. Refer to the 8259 data sheet for more information on programming the 8259 megacell.

When reading at address 0020h or 00A0h, the register read will depend on how Operation Control Word 3 was set up prior to the read.

TABLE 8. INTERRUPT CONTROLLER WRITE OPERATIONS

INT1	INT2	XD4	XD3	Register Function
0020h	00A0h	1	X	Write ICW1
0021h	00A1h	X	X	Write ICW2
0021h	00A1h	X	X	Write ICW3
0021h	00A1h	X	X	Write ICW4 (if needed)
0021h	00A1h	X	X	Write OCW1
0020h	00A0h	0	0	Write OCW2
0020h	00A0h	0	1	Write OCW3

TABLE 9. INTERRUPT CONTROLLER READ OPERATIONS

INT1	INT2	Register Function
0020h	00A0h	Interrupt Request Register, In-Svc Register or Poll Command
0021h	00A1h	Interrupt Mask Register

COUNTER/TIMER SUBSECTION

The timer subsection consists of one 8254 counter/timer megacell configured as shown in Figure 3. The clocks for each of the three internal counters are tied to the 14.318 MHz oscillator through a divide by 12 counter. The gate inputs of counters zero and one are tied high to enable those counters at all times. The gate input of counter two is tied to bit 0 of the Port B register inside the VL82C331.

One of the 8254 megacell counter outputs is directly available at an external pin. Counter zero's output is connected to the IRQ0 input of interrupt controller one. Counter one's output goes to the pin OUT1. Finally, counter two's output goes to an AND gate which drives the output pin SPKR. The other input on this AND gate is connected to bit 1 of the Port B register.

Counter/Timer Registers

The internal registers of the 8254 counter/timer megacell are written to in the same way as in the standard part. Table 10 shows the correct addressing for each of the 8254 registers.

The write control word at address 0043 hex could also be the counter latch command or read back command depending on the values on the data bus. Refer to the 8254 data sheet for more information on programming the 8254 megacell.

FIGURE 3. COUNTER/TIMER BLOCK DIAGRAM

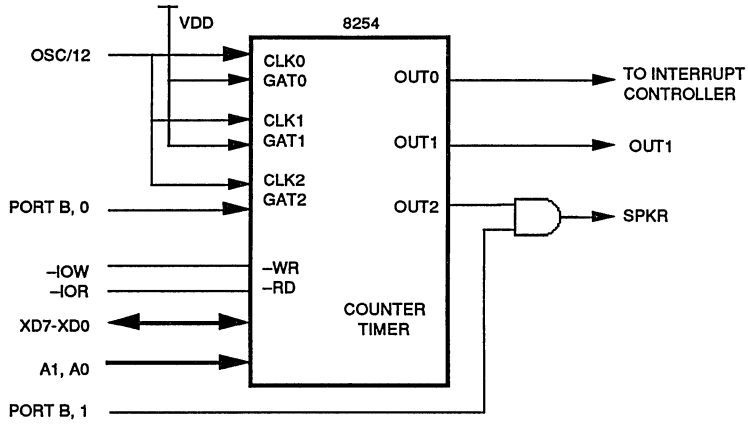


TABLE 10. COUNTER/TIMER ADDRESSING REGISTERS

Addr	–IOR	–IOW	Register Function
0040h	1	0	Write Initial Count to Counter
0040h	0	1	Read Count/Status from Counter 0
0041h	1	0	Write Initial Count to Counter 1
0041h	0	1	Read Count/Status from Counter 1
0042h	1	0	Write Initial Count to Counter 2
0042h	0	1	Read Count/Status from Counter 2
0043h	1	0	Write Control Word
0043h	0	1	No Operation

REAL TIME CLOCK

The VL82C331 contains VLSI Technology's real time clock megacell. It is 100% compatible with the 146818A and contains additional battery backed RAM within its address space in order to support non-volatile configuration register storage. Enough storage is provided to store the VL82C331's and System Controller's configuration data. Additional storage is provided in order to support future chip set enhancements and other planned VLSI Technology peripherals.

Real Time Clock Programmer's Model

The RTC memory consists of ten RAM bytes which contain the time, calendar, and alarm data, four control and status bytes, and 114 general purpose RAM bytes. The address map of the real time clock is shown in Table 11.

All 128 bytes are directly readable and writeable by the processor program except for the following:

1) Registers C and D are read-only.

2) Bit 7 of Register A is read-only.

This RTC configuration represents an extension to the 146818A architecture. An additional 64 bytes of standby RAM have been added to the RTC memory map. This area provides space to store chip set configuration data and provides ample additional storage in order to support future chip set versions and extra BIOS scratch pad memory.

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these RAM locations. The contents of the ten time, calendar, and alarm bytes may be either binary or binary-coded decimal (BCD).

Time of Day Register Descriptions

The contents of the time of day registers can be either in binary or BCD format. They are relatively straightforward, but are detailed here for completeness. The address map of these registers is shown in Table 11 and following.

TABLE 11. REAL TIME CLOCK ADDRESS MAP

Hex Addr	Function	Range
00	Seconds (Time)	0-59
01	Seconds (Alarm)	0-59
02	Minutes (Time)	0-59
03	Minutes (Alarm)	0-59
04	Hours (Time)	1-12; 12 Hour Mode
04	Hours (Time)	0-23; 24 Hour Mode
05	Hours (Alarm)	0-23
06	Day of Week	1-7
07	Date of Month	1-31
08	Month	1-12
09	Year	0-99
0A	RTC Register A	(Read/Write)
0B	RTC Register B	(Read/Write)
0C	RTC Register C	(Read-only)
0D	RTC Register D	(Read-only)
0E-7F	User RAM (Standby)	

Address 00 - Seconds:
The range of this register is 0-60 in BCD mode, and 0-3Bh in binary mode.

Address 01 - Seconds Alarm:
The range of this register is 0-60 in BCD mode, and 0-3Bh in binary mode.

Address 02 - Minutes:
The range of this register is 0-60 in BCD mode, and 0-3Bh in binary mode.

Address 03 - Minutes Alarm:
The range of this register is 0-60 in BCD mode, and 0-3Bh in binary mode.

Address 4 - Hours:
The range of this register is:

Range	Mode	Time
1-12	BCD	AM
81-92	BCD	PM
01h-0Ch	Binary	AM
81h-8Ch	Binary	PM

Address 05 - Hours Alarm:
The range of this register is:

Range	Mode	Time
1-12	BCD	AM
81-92	BCD	PM
01h-0Ch	Binary	AM
81h-8Ch	Binary	PM

Address 06 - Day of Week:
The range of this register is 1-7 in BCD mode, and 1-7h in binary mode.

Address 07 - Date:
The range of this register is 1-31 in BCD mode, and 1-1Fh in binary mode.

Address 08 - Month:
The range of this register is 1-12 in BCD mode, and 1-0Ch in binary mode.

Address 09 - Year:
The range of this register is 0-99 in BCD mode, and 0-63h in binary mode.

RTC Control Register Descriptions
The RTC megacell has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

Hex Addr	Function	Type
0A	RTC Register A	R/W
0B	RTC Register B	R/W
0C	RTC Register C	R-O
0D	RTC Register D	R-O
0E-7F	User RAM (Standby)	R/W

Register A Description
This register contains control bits for the selection of periodic interrupt, input divisor, and the update in progress status bit. The bits in the register are defined as follows:

Bit	Description	Abbr
0	Rate Select Bit 0	RS0
1	Rate Select Bit 1	RS1
2	Rate Select Bit 2	RS2
3	Rate Select Bit 3	RS3
4	Divisor Bit 0	DV0
5	Divisor Bit 1	DV1
6	Divisor Bit 2	DV2
7	Update in Progress	UIP

Bits 3-0 - The four rate selection bits (RS3 to RS0) select one of 15 taps on the 15-stage divider, or disable the divider output. The tap selected may be used to generate a periodic interrupt. These four bits are read/write bits which are not affected by RESET. The periodic interrupt rate that results from the selection of various tap values is as follows:

RS Value	Periodic Interrupt Rate
00	None
01	3.90625 ms
02	7.8125 ms
03	122.070 µs
04	244.141 µs
05	488.281 µs
06	976.562 µs
07	1.953125 ms
08	3.90625 ms
09	7.8125 ms
0Ah	15.625 ms
0Bh	31.25 ms
0Ch	62.5 ms
0Dh	125 ms
0Eh	250 ms
0Fh	500 ms

Bits 6-4 - The three divisor selection bits (DV2-DV0) are fixed to provide for only a 15-stage divider chain, which would be used with a 32 KHz external crystal. Only bit 6 of this register can be changed allowing control of the reset for the divisor chain. When the divider reset is removed, the first update cycle begins one-half second later. These bits are not affected by power-on reset (external pin).

DV Value	Condition
2	Operation Mode, Divider Running
6	Reset Mode, Divider in Reset State

Bit 7 - The update in progress (UIP) bit is a status flag that may be monitored by the program. When UIP is a 1, the update cycle is in progress or will soon begin. When UIP is a 0, the update cycle is not in progress and will not be for at least 244 µs. The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is 0. The UIP bit is a read-only bit, and is not affected by RESET. Writing the SET bit in register B to a 1 will inhibit any update cycle and then clear the UIP status bit.

Register B Description
Register B contains command bits to control various modes of operations and interrupt enables for the RTC. The bits in this register are defined as follows:

Bit	Description	Abbr
0	Daylight Savings Enable	DSE
1	24/12 Mode	24/12
2	Data Mode (Binary or BCD)	DM
3	Not Used	
4	Update End Interrupt Enable	UIE
5	Alarm Interrupt Enable	AIE
6	Periodic Interrupt Enable	PIE
7	Set Command	SET

Bit 0 - The daylight savings enable (DSE) bit is a read/write bit which allows the program to enable two special updates (when DSE is 1). On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is 0. DSE is not changed by any internal operations or reset.

Bit 1 - The 24/12 control bit establishes the format of the hours bytes as either the 24-hour mode (1) or the 12-hour mode (0). This is a read/write bit, which is affected only by software.

Bit 2 - The data mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or reset. A 1 in DM signifies binary data, while a 0 signifies BCD data.

Bit 3 - This bit is unused.

Bit 4 - The UIE (update end interrupt enable) bit is a read/write bit which enables the update-end flag (UF) bit in register C to assert an IRQ. The RESET pin being asserted or the SET bit going high, clears the UIE bit.

Bit 5 - The alarm interrupt enable (AIE) bit is a read/write bit which when set to a 1 permits the alarm flag (AF) bit in register C to assert an IRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including "don't care" alarm code of 11XXXXXXb). When the AIE bit is a 0, the AF bit does not initiate an IRQ signal. The RESET pin clears AIE to 0. The internal functions do not affect the AIE bit.

Bit 6 - The periodic interrupt enable (PIE) bit is a read/write bit which allows the periodic interrupt flag (PF) bit in register C to cause the IRQ pin to be driven low. A program writes a 1 to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3, RS2, RS1, and RS0 bits in register A. A 0 in PIE blocks IRQ from being initiated by a periodic interrupt, but the periodic flag (PF) bit is still set at the periodic rate. PIE is not modified by an internal functions, but is cleared to 0 by a reset.

Bit 7 - When the SET bit is a 0, the update cycle functions normally be advancing the counts once-per-second. When the SET bit is written to a 1, any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. Also, all time and calendar bytes should be initialized when the SET bit is written to a 1. SET is a read/write bit which is not modified by reset or internal functions.

Register C Description
Register C contains status information about interrupts and internal operation of the RTC. The bits in this register are defined as follows:

Bit	Description	Abbr
0	Not Used, Read as 0	
1	Not Used, Read as 0	
2	Not Used, Read as 0	
3	Not Used, Read as 0	
4	Update Ended Flag	UF
5	Alarm Interrupt Flag	AF
6	Periodic Interrupt Flag	PF
7	IRQ Pending Flag	IRQF

Bits 3-0 - The unused bits of status register C are read as 0's and cannot be written.

Bit 4 - The update ended interrupt flag (UF) bit is set after each update cycle. When the UIE bit is a 1, the 1 in UF causes the IRQF bit to be a 1, asserting the IRQ. UF is cleared by a register C read or a reset.

Bit 5 - A 1 in the AF (alarm interrupt flag) bit indicates that the current time has matched the alarm time. A 1 in the AF causes the IRQ pin to go low, and a 1 to appear in the IRQF bit, when the AIE bit also is a 1. A reset or a read of register C clears AF.

Bit 6 - The periodic interrupt flag (PF) is a read-only bit which is set to a 1 when a particular edge is detected on the selected tap of the divider chain. The RS3-RS0 bits establish the periodic rate. PF is set to a 1 independent of the state of the PIE bit. PF being a 1 initiates an IRQ signal and sets the IRQF bit when PIE is also a 1. The PF bit is cleared by a reset or a software read of register C.

Bit 7 - The interrupt request flag (IRQF) is set to a 1 when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1

The logic can be expressed in equation form as:

IRQF = PF • PIE + AF • AIE + UF • UIE

Any time the IRQF bit is a 1, the IRQ pin is asserted. All flag bits are cleared after register C is read by the program or when the RESET pin is asserted.

Register D Description
This register contains a bit that indicates the status of the on-chip standby RAM. The contents of the registers are described as the following:

Bit	Description	Abbr
0	Not Used, Read as 0	
1	Not Used, Read as 0	
2	Not Used, Read as 0	
3	Not Used, Read as 0	
4	Not Used, Read as 0	
5	Not Used, Read as 0	
6	Not Used, Read as 0	
7	Valid RAM Data and Time	VRT

Bits 6-0 - The remaining bits of register D are unused. They cannot be written, but are always read as 0's.

Bit 7 -

CMOS Standby RAM Description
The 114 general purpose RAM bytes are not dedicated to RTC use within the RTC. They are fully available during the update cycle.

General Operational Notes
Set Operation:
Before initializing the internal registers, the SET bit in register B should be set to a 1 to prevent time/calendar updates from occurring. The program initializes the ten locations in the selected format (binary or BCD), then indicates the format in the data mode (DM) bit of register B. All ten time, calendar, and alarm bytes must use the same data mode, either binary or BCD. The SET bit may now be cleared to allow updates. Once initialized, the RTC makes all updates in the selected data mode. The data mode cannot be changed without reinitializing the ten data bytes.

BCD VS Binary Format:
The 24/12 bit in register B establishes whether the hour locations represent 1-to-12 or 0-to-23. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected the high order bit of the hours byte represents PM when it is a 1.

Update Operation:
The time, calendar, and alarm bytes are not always accessible by the processor program. Once-per-second the ten bytes are switched to the update logic to be advanced by one second and to

check for an alarm condition. If any of the ten bytes are read at this time, the data outputs are undefined. The update lockout time is 1948 µs for the 32.768 KHz time base. The update cycle section shows how to accommodate the update cycle in the processor program.

Alarm Operation:
The three alarm bytes may be used in two ways. First, when the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second usage is to insert a "don't care" state in one or more of three alarm bytes. The "don't care" code is in any byte from C0h to FFh. An alarm interrupt each hour is created with "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

Interrupts:
The RTC plus RAM includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from one-per-second to one-a-day. The periodic interrupt may be selected for rates from half-a-second to 30.517 µs. The update ended interrupt may be used to indicate to the program that an update cycle is completed.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in register B enable the three interrupts. Writing a 1 to an interrupt enable bit permits that interrupt to be initiated when the event occurs. A 0 in the interrupt enable bit prohibits the IRQ pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enable, the IRQ pin is immediately activated, though the interrupt initiating the event may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs a flag bit is set to a 1 in register C. Each of the three interrupt sources have separate flag bits in register C, which are set independent of the state of corresponding enable bits in register B. The flag bit may be used with or without enabling the corresponding enable bits.

Divider Control
The divider control bits are fixed for only 32.768 KHz operation. The divider chain may be held reset, which allows precision setting of the time. When the divider is changed from reset to an operating time base, the first update cycle is one-half second later. The divider control bits are also used to facilitate testing the RTC.

Periodic Interrupt Selection
The periodic interrupt allows the IRQ pin to be triggered from once every 500 ms to once every 30.517 µs. The periodic interrupt is separate from the alarm interrupt which may be output from once-per-second to once-per-day.

Update Cycle
The RTC executes an update cycle one-per-second, assuming one of the proper time bases is in place, the DV2-DV0 divider is not clear, and the SET bit in register B is clear. The SET bit in the 1 state permits the program to initialize the time and calendar bytes by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the second byte, check for overflow, increment the minutes byte when appropriate and so forth through to the year of the century byte. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code (11XXXXXX) is present in all three positions.

With a 32.768 KHz time base update cycle takes 1984 µs, during which, the time, calendar, and alarm bytes are not accessible by the processor program, protecting the program from reading transitional data. This protection is provided by switching the time, calendar, and alarm portion of the RAM off the microprocessor bus during the entire update cycle. If the processor reads these RAM locations before the update is complete the output will be undefined. The update is progress (UIP) status bit is set during the interval.

Three methods of accommodating non-availablity during update are usable by the program. In discussing the three methods it is assumed that at random points user programs are able to call a subroutine to obtain the time of day.

The first method of avoiding the update cycle uses the update ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information. Before leaving the interrupt service routine, the IRQF bit in register C should be cleared.

The second method uses the update in progress bit (UIP) in register A to determine if the update cycle is in progress or not. The UIP bit will pulse once-per-second. After the UIP bit goes high, the update cycle begins 244 µs later. Therefore, if a low is a read in the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. If a 1 is read in the UIP bit, the time/calendar data may not be valid. The user should avoid interupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in register A is set high between the setting of the PF bit in register C.

To properly setup the internal counters for daylight savings time operation, the user must set the time at least two seconds before the roll-over will occur. Likewise, the time must be set at least two seconds before the end of the 29th or 30th day of the month.

Power-down Mode
The passive components that are critical for low power operation are shown in the Figure 4.

In Figure 4, the POWERGOOD signal from the power supply is used to control the power-down mode of the RTC.

When POWERGOOD is low, the RTC enters power-down mode. In this mode, all outputs are three-stated and read or write operations are inhibited. Any operation in progress (address entered but the data not yet accessed) is terminated and must restart from the

beginning of the bus cycle for proper operation. A write operation in progress is abortted and the data path is double buffered to prevent data corruption. The Power Sense signal is used to reset the state of the Valid RAM and Time (VRT) bit. This input must be asserted after power is applied to the RTC to set the state of the VRT bit properly.

With a power consumption target specification of 5 µA, and a lithium battery with a capacity of 100 mA-Hr, time will be properly kept for approximately 2.25 years.

Disabling Internal RTC

The fully compatible internal real-time clock saves the designer money and board space versus use of an external RTC. However, sometimes a stand-alone RTC is preferred. To allow this option, the internal RTC may be disabled by setting bit 6 of the configuration register BUSCTL to a logic 1. In this mode, the PS/–RCLR/–IRQ8 pin becomes the –IRQ8 input. This routes the external RTC's interrupt signal through an internal inverter to the IRQ8 input of the VL82C331's interrupt service logic. When the internal RTC is disabled by setting BUSCTL[6]=1, the VL82C331's –CS8042/–RTC output also becomes active during RTC I/O address decodes to 70h or 71h. The system designer must externally generate the required three signals for an external RTC; RTCAS, RTCDS, and RTCRW. If a stand-alone keyboard controller is used, the –CS8042/–RTC signal must also be decoded from the VL82C331's composite chip select output. These external decodes can easily be performed using the 74HC139.

BUS CONTROLLER REFRESH SUBSYSTEM

The System Controller performs on-board DRAM refresh and controls both on- and off-board refresh timing in all modes. The VL82C331 actually performs the off-board refresh when commanded by the System Controller. Refresh may be performed in a coupled or decoupled mode. In coupled mode, refresh timing for both system board and slot bus refreshes is performed in a synchronous manner. In decoupled mode, the System Controller has complete control over the timing of on-board DRAM refresh and and off-board refresh but the timing of each is independent. See the section "System Board DRAM Refresh" in the VL82C320 or VL82C330 data sheet for more information.

PORT B AND NMI LOGIC

The Bus Controller generates the Non-Maskable Interrupt (NMI) output pin for the CPU. NMI is enabled by a write to I/O address 0070h with D7 low. Once enabled, an NMI can be generated by the IOCHCK input going low or the –PARERROR input going low. Each of these NMI sources has an enable bit in the Port B register to allow these inputs to cause an NMI when set high, or ignore the input if the bit is low.

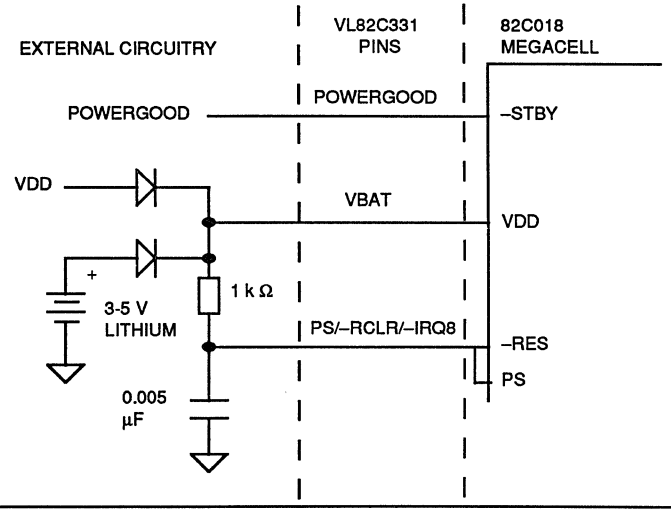
The Port B register at I/O address 0061 hex is included in the Bus Controller chip. This register contains bits to control the speaker output and NMI circuitry. Bits 3-0 are read/write bits, while bits 7-4 are read-only. Each bit of the register is defined below. Bits 3-0 are all set low by a reset.

Port B, 0 Speaker Timer 2 Gate (TIM2GAT_SPK). This bit goes to the gate 2 input on the 8254 megacell to enable counter 2 to produce a speaker frequency.

Port B, 1 Speaker Data (SPK_DAT). This bit is gated with the output of counter 2 from the 8254 megacell. When this bit is high, it allows the OUT2 frequency to be passed out on the SPKR pin. When this bit is low, the SPKR output is forced low.

Port B, 2 Enable RAM Parity Check (–ENA_RAM_PCK). When this bit is set low, it allows parity errors from the on-board RAM memory to cause an NMI. When high, on-board RAM parity errors will not cause an NMI.

FIGURE 4. RTC LOW POWER OPERATION CIRCUIT



Port B, 3 Enable I/O Check (–ENA_IO_CK). When this bit is set low, it allows an NMI to be generated if the IOCHCK input is pulled low. Otherwise, the IOCHCK input is ignored and can not generate an NMI.

Port B, 4 Refresh Detect (REFDET). This bit is tied to a toggle flip-flop which is clocked by –REFRESH. It will toggle to the opposite state every time a refresh cycle occurs.

Port B, 5 Timer Output bit 2 state (OUT2). This bit indicates the current state of the OUT2 signal from the 8254 megacell.

Port B, 6 Channel Check (CHAN_CHK). This bit indicates that a peripheral device is reporting an error. It can only be set if –ENA_IO_CK is set low. IOCHERR should be cleared by writing a high to ENA_IO_CK.

Port B, 7 Parity Check (PCK). This bit indicates that an on-board RAM parity error has occurred. It can only be set if –ENA_RAM_PCK is set 0. –PCK should be cleared by writing a 1 to –ENA_RAM_PCK.

ISA BUS INTERFACE SUBSECTION

The VL82C331 ISA Bus Interface can be controlled from four possible sources. Three of these sources are generated in the Bus Controller chip. They are CPU mode, DMA mode, and refresh mode. The fourth possible source is a bus master.

In CPU mode, the Bus Controller receives bus cycle commands from the System Controller, executes them and responds back to the System Controller when the bus cycle is complete. When in this mode, the 288 megacell is responsible for generating the command (–IOR, –IOW, –MEMR, –MEMW, –SMEMR, and –SMEMW) signals, BALE and the timing for when the SA bus will be valid. The Bus Controller samples the inputs –MEMCS16, –IOCS16, IOCHRDY, and –WS0 and combines these with internally defined definitions to determine the length in wait states of each bus cycle.

Refresh modes are initiated as described above. During refresh the bus controller will drive the –REFRESH signal, a refresh address and –MEMR command onto the bus to implement the refresh cycle. The refresh circuit samples IOCHRDY to determine if the –MEMR and –REFRESH pulses need to be extended. The outputs AEN and BALE are both driven high during the refresh cycles.

In DMA mode, the Bus Controller is driven from one of the 8237 DMA controller megacells. The DMA controllers generate the command and address signals. BALE is forced high for all DMA cycles. The bus controller asserts the AEN signal to indicate that the current address on the bus is for memory only and not to be decoded as an I/O address. The DMA section samples IOCHRDY to extend bus cycles longer than the internally defined cycle length.

Bus master mode is an extension of DMA mode. A master can get control of the bus by requesting a DMA operation. Once the DMA is acknowledged, the –MASTER signal is pulled active and the Bus Controller relinquishes control of the bus to the master. While in master mode, the Bus Controller buffers the address lines and drives them onto the local address bus (A bus) to be used to address on-board memory.

A Bus Master can perform a refresh by releasing the bus, then asserting –REFRESH. The VL82C331 will drive the refresh address and –MEMR as described above.

Extended Slot Bus Timing Options

Data Port 00EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
BUSCTL (84)	1	RTC Ctrl	1	1	ADDLY	RLX Timing	16 WS	8 WS

Four bus control options are provided and are programmable via the indexed BUSCTL register. On reset, the four control bits are reset to 0. This specifies the full PC/AT-compatibility mode.

When bit 0 = 1, an extra wait state is added for 8-bit slot bus accesses. This yields five rather than the normal four wait states. This allows slower boards to operate with equivalent performance when higher bus speeds are used.

When bit 1 = 1, an extra wait state is added for 16-bit slot bus accesses. This yields two instead of the normal one for I/O accesses and one instead of zero for memory accesses.

When bit 2 = 1, an extra command delay is added for 16-bit memory cycles.

When bit 3 = 1, an extra command delay is added for 8- and 16-bit I/O cycles and for 8-bit memory cycles.

Note: Zero wait state is possible on extremely fast boards that can pull the 0WS line fast enough and more than five wait states are possible if IOCHRDY is pulled low before the last normal wait state. However, –MEMCS16 or –IOCS16 must be pulled low before the last normal wait state even if IOCHRDY has previously been activated.

ROM ACCESS CONTROL SUBSECTION

Data Port 00EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
ROMDMA (81)	ROM Wait States		8-Bit DMA Wait States		16-Bit DMA Wait States		DMA Clock	MEMR Timing

Bits 6 and 7 of the ROMDMA configuration register allow programming the number of slot bus wait states for BIOS ROM accesses. Range is from one to three wait states. The POR default is three wait states. Shadow RAM features of the Sytem Controller are recommended to speed BIOS access. ROM decode logic in the Bus Controller provides a single ROM chip select for this BIOS region. A chip select also results from decode of the middle BIOS address space between FE0000h and FFFFFFh and also the upper BIOS space from FFFE0000h to FFFFFFFFh.

ISA BUS CONTROLLER/SYSTEM CONTROLLER INTERCHIP COMMUNICATION

The asynchronous interface to the Bus Controller is handled by a group of signals from the System Controller. –CHS0, –CHS1 and CHM/–IO define which type of cycle is to be executed as follows:

CHM/–IO	–CHS1	–CHS0	Bus Cycle
0	0	0	–INTA
0	0	1	–IOR
0	1	0	–IOW
0	1	1	Reserved
1	0	0	–REFRESH
1	0	1	–MEMR
1	1	0	–MEMW
1	1	1	Reserved

POWER SAVING SLEEP MODE

Data Port 00EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
SLEEP	Enable	1	1	1	1	1	1	SYSCLK

Bit 7 of the sleep register is set to 1 in order to enable sleep function. It is write-only at indexed register port 13h because it duplicates the address and bit position of the sleep enable function in the System Controller. (For test purposes, the Bus Controller register can be read and written at indexed location 83h.) The Bus Controller sleep mode features work together with System Controller sleep features to provide a low power system idle state for extension of battery life in portable systems. When activated by the CPU via an I/O write to bit 7 of the sleep register, the the interrupt controllers and the timers continue to operate. When an interrupt occurs due to an external source or internal timer zero, the Bus Controller passes it to the CPU. The CPU then resets bit 7 of the sleep register. This brings both the System Controller and the Bus Controller out of the sleep state.

Setting bit 0 = 0 disables the SYSCLK oscillator (BUSCLK/2) if bit 7 is set to 1. Returning bit 7 to 0 re-enables the oscillator signal. If bit 0 = 1, the oscillator is always enabled even in sleep mode.

In operation, bit 0 is set for the desired operational mode by the BIOS on power-up. Bit 7 is then controlled as required to jump in and out of sleep mode during operation.

IN-CIRCUIT TEST LOGIC

During In-Circuit Test (ICT) all of the outputs can be toggled by one or more inputs. This allows for a board level tester to test the solder connections for each signal pin.

The sequence for enabling ICT is as follows:

1) Tester drives –TRI signal to 0.
2) Tester drives XD bus to FFh.
3) Tester pulses –IOR and –IOW low for 100 ns (minimum).
4) Tester drives –TRI signal to 1 (outputs now enabled).

The sequence for disabling ICT is assertion of RESET or repeat steps 1-4 with XD bus = 00h.

ICT INPUT		ICT OUTPUT	
Signal Name	Pin #	Signal Name	Pin #
SA6	1	–DACK2	2
SA5	3	T/C	4
SA4	5	BALE	6
SA3	7	SA2	8
OSC	9	SA1	11
–MEMCS16	13	SA0	12
–IOCS16	15	–SBHE	14
IRQ10	17	LA23	16
IRQ11	21	LA22	18
IRQ12	23	LA21	22
IRQ15	25	LA20	24
IRQ14	27	LA13	26
LA18	28	–DACK0	29
DRQ0	32	LA17	31
–MEMR	33	–DACK5	34
DRQ5	36	–MEMW	35
DRQ6	38	–DACK6	37
DRQ7	41	–DACK7	39
MASTER	42	A25	43
A23	45	A24	44
A22	46	A21	47
A20	48	A19	49
A18	50	A17	51
A16	52	A15	53
A14	54	A13	55
A12	56	A11	57
A10	58	A9	61
A8	62	A7	63
A6	64	A5	65
A4	66	A3	67
A2	58	–BE3	59
–BE2 (A1)	70	–BE1 (–BHE)	71
(C286) –386DX	73	–BE0 (A0)	72
CPUHLDA	74	INTR	75

ICT INPUT		ICT OUTPUT	
Signal Name	Pin #	Signal Name	Pin #
–CHS0/–MW	77	NMI	76
–CHS1/–MR	78	CHM/–IO *	82
XD4	95	–EALE *	83
–BLKA20	87	–BRDRAM *	84
BUSCLK	86	–CHREADY	85
XD5	94	DMAHLDA *	88
XD6	92	DMAHRQ	89
XD7	91	OUT1	90
XD3	96	–LATLO	104
XD2	97	–XDREAD	103
XD1	98	SDHL/–HL	102
XD0	99	–SDSWAP	101
–PCK	111	–LATHI	105
IRQ13	110	SPKR	107
IRQ9	109	–CS8042	108
–ROM8	112	–DACK1	142
–HIDRIVE	113	SA16	137
PS/–RCLR/–IRQ8	117	SA18	133
–IOCHK	121	RSTDRV	122
IRQ9	123	SA15	131
DRQ2	124	–SMEMR	129
–WS0	125	AEN	128
IOCHDY	126	–SMEMW	127
–IOW	132	–DACK3	136
–IOR	134	SA17	135
DRQ3	138	SA15	141
DRQ1	144	SA14	143
–REFRESH	146	SA13	145
SA12	147	SYSCLK	148
IRQ7	151	SA11	149
IRQ6	153	SA10	152
IRQ5	155	SA9	154
IRQ4	157	SA8	156
IRQ3	159	SA7	158

***CAUTIONARY NOTE:** These signals are normally outputs but are mapped as inputs during ICT. Board design must take this into account if In-Circuit mode is used.

CONFIGURATION REGISTER ACCESS

CONFIGURATION ENABLE/DISABLE REGISTERS (I/O addresses 00FBh and 00F9h)

00FBh	D7	D6	D5	D4	D3	D2	D1	D0
ENABLE	X	X	X	X	X	X	X	X

00F9h	D7	D6	D5	D4	D3	D2	D1	D0
DISABLE	X	X	X	X	X	X	X	X

When enabled and used as described below, the configuration registers are protected from unauthorized accesses that might garble the system configuration and either crash the system or change its operational characteristics in an unwanted manner. A write to 00FBh enables the configuration registers. A write to 00F9h disables the configuration registers. When disabled, the system is locked out from any access to the configuration and control ports from address 00E8h through 00EFh. This includes the indexed configuration registers described in the Index Register Section.

If MISCSET=1, the Configuration Enable/Disable feature is disabled. See the description under MISCET in the Data Port Register Section.

A read operation on 00F9h or 00FBh will not cause the VL82C331 to drive the X bus. However, the VL82C331 will drive the X bus with undefined data.

CONFIGURATION REGISTER OPERATIONAL SUMMARY

Table 13 at end of this section shows a mapping of the VL82C331 ISA Bus Controller indexed configuration registers. These registers are accessed through a single port address as described in the "Index Register" section that follows.

Other configuration register sets exist in the Bus Controller. The DMA controllers, interrupt controllers, and counter/timers have separate I/O registers at the PC/AT-compatible locations.

Index Register (00ECh) (Write-Only)
The value written to this register is the 8-bit address of the data port which is accessed through the data port register at I/O address 00EDh. All subsequent data port reads and writes will access the register at this address until the index register is written with a new 8-bit address. This register is write-only. The index register and data port register, described below, share common addresses with the index and data port registers located in the System Controller. A write to the index register at 00ECh is latched into both the System Controller and Bus Controller. Only the System Controller index register is readable in order to avoid bus collisions.

Data Port Register (I/O Address 00EDh)
Each register accessible through I/O address 00EDh is functionally described next. It is accessed first by writing its address to the index register at I/O address 00ECh, then by accessing the data port at I/O address 00EDh. All data ports in the Bus Controller are located in the range 80h to FFh to avoid contention with data ports located in the System Controller. However, there is one exception. See the section "Sleep Register" for details.

Version (80h) (Read-Only) (Default = F8h)
D2-D7 will contain a code which indicates that this part is a VLSI Technology, Inc., PC/AT-compatible ISA Bus Controller. D0 and D1 contain the version number of this chip. By using this byte, a smart BIOS can compensate for "feature" differences based on the version number. The code 00F4h is used in the initial version of this chip. By breaking the code in two bit pieces, it is revealed to be "331" Rev. "0."

ROMDMA (81h) (Default = FCh)
Bits 7-6 indicate the number of ROM wait states. These wait states are timed in slot bus cycles. The valid range is 1 to 3.

00 = 3 wait states
01 = 1 wait state
10 = 2 wait states
11 = 3 wait states (Default)

Bits 5-4 are encoded with the number of clocks the command is active for 8-bit DMA cycles:

00 = 2 DMA clocks
01 = 4 DMA clocks
10 = 3 DMA clocks
11 = 3 DMA clocks (Default)

Bits 3-2 are encoded with the number of 1 clocks the command is active for 16-bit DMA cycles:
00 = 2 DMA clocks
01 = 4 DMA clocks
10 = 3 DMA clocks
11 = 3 DMA clocks (Default)

Bit 1 = 1 for DMA clock = SYSCLK. Bit 1 = 0 for SYSCLK/2. (Default = 0.)

Bit 0 specifies the delay for the –DMAMEMR signal. When bit 0=0, –DMAMEMR is active at the same time as in the original PC/AT design. This is the default case. When bit 0=1, the falling edge of –DMAMEMR occurs one DMACLK earlier. In this latter case, the –DMAMEMR timing during a memory to I/O DMA cycle is the same as that of the –IOR signal during an I/O to memory DMA cycle. (Default = 0.)

612AXS (82h) (Default = 3Eh)
Bit 7 enables the extended DMA functions when set to 1 by allowing access to the two required upper address bits, A24 and A25. When bit 7 = 0, the extended functionality is disabled. Any previously stored values for A24 and A25 are disabled and both bits are forced to 0. This latter mode is fully compatible with the PC/AT-standard. When bit 7 = 1, the extended mode is enabled. A24 and A25 can be set in the memory mapper page register by setting bit 0 of this register to 1 and writing the data to the same address used for the lower page register byte. Resetting bit 0 to 0 allows access to the lower page registers. See the bit 0 discussion below for more detail. (Default = 0.)

Bit 6 enables EISA I/O access compatibility when set to 1 by allowing access to the upper DMA page address bits at I/O addresses 4XX where XX = the same address as the lower page register byte. When set to 1, it also enables the extended DMA system and allows the contents of the upper page register's A24 and A25 to be used. (Default = 0.)

Note - When the external 286/–386 pin is not tied to ground, bits 6 and 7 are held low disabling the extended DMA mode. Attempts by software to write logic 1's to these bits has no effect and subsequent reads will return 0. The extended DMA function is not supported when the VL82C331 ISA Bus Controller is used with the VL82C320 System Controller in 286- or 386SX-based systems.

Bit 0 allows access via the same I/O addresses to the lower address bits, A16-A23 of the DMA page register when set to 0 or to the upper address bits A24 and A25 when set to 1. The state of this bit has no effect unless bit 7 of this register has been previously set to 1. (Default = 0.)

Sleep (13h) (Write-only)
SLPTST (83h) Read/Write for factory or Post test) (Default = 7Fh)
This special case register overlays the sleep register at the same indexed register location as in the VL82C320 and VL82C330 system controllers. D7 and D0 are the only active bits in the ISA Bus Controller. In standard operation, a read of indexed register 13h will return the register's contents as last written and latched into the VL82C330. For test purposes, the Bus Controller sleep register can be read and written at indexed location 83h. In normal operation, however, all reads and writes should be performed through indexed register 13h.

Bit 7- Power-down enable
0 = Default setting. Normal PC/AT-compatible operation
1 = DMA clock disabled. Bus Quiet mode active. SYSCLK stopped is bit 0=0.

This bit is reset to zero and normal operation resumes when rewritten or when a hardware reset of the Bus Controller occurs.

Bit 0 can be used to disable the SYSCLK signal to the slot bus. When set to 0 and bit 7 is set to 1, the SYSCLK signal is shut down until bit 7 is reset to 0. If bit 0 = 1, SYSCLK is enabled to the slot bus regardless of the state of bit 7. (Default = 1.)

BUSCTL (84H) (Default = B0h)
Bit 6 allows the internal RTC to be disabled if use of an external RTC is prefered. Bit 6 = 1 disables the internal RTC and redefines the PS/–RCLR/ –IRQ8 pin as –IRQ8 in. Default = 0, internal RTC is operational.

Bit 3 allows addition of one extra command delay for 8- and 16-bit I/O cycles and for 8-bit memory cycles. (Default = 0, no added command delays.)

Bit 2 determines whether to use the PC/AT-compatible zero command delays on 16-bit memory cycles or whether to add one. (Default = 0, no command delays on 16-bit memory cycles.)

Bit 1 determines whether to use zero or one wait states for 16-bit slot bus accesses. When bit 1 = 0, the PC/AT-compatible zero wait states are used. When set to 1, one wait state is used to allow robust operation of add-in cards at faster slot speeds. (Default = 0, zero wait states on 16 slot bus accesses.)

Bit 0 determines whether to use four or five wait states for 8-bit slot bus accesses. When bit 1 = 0, the PC/AT-compatible four wait states are used. When set to 1, five wait states are used to allow robust operation of add-in cards at faster slot speeds. (Default = 0; four wait states on 8-bit slot bus accesses.)

MISCSET (14h) (Write-only)
Bit 7 is used to enable or disable the SF options mapped into the coprocessor chip set I/O space between F0h and FFh. This register is used to monitor writes to MISCSET[7] in the VL82C330. When monitored in conjunction with writes to FBh and F9h, the VL82C331 can enable or disable access to these configuration registers. This is described in more detail in the Detailed Internal Control Register Section. 0=enabled, 1=disabled. (Default = 0)

RAMMAP (03h) (Write-only)
Bit 7 determines bus controller response to memory accesses between E0000h-EFFFFh and FE0000h-FEFFFFh. When set to a logic 1, a ROM access is performed for read cycles. When set to logic 0, slot bus accesses is performed for read cycles. In either case, write cycles are performed to the slot bus. This feature allows systems not using a 128K BIOS to access memory devices on the slot bus in these two areas. (Default = 1)

All other bits at data port 03h in the VL82C331 are inactive. See the definition of REGTEST (85h) that follows.

REFCTL (06h) (Write-only)
Bit 3 controls internal I/O decode. When set to 0, full 16-bit decode is performed. When set to 1, 10-bit decode is performed. The latter option provides less system flexibility but is compatible with the original PC design. This function has been restructured since the latest published specification such that a write to this single bit control both VL82C331 and Bus Controller I/O decodes. This prevents the possibility of having one component in 16-bit mode and the other in 10-bit mode. (Default = 0)

All other bits at data port 06h in the VL82C331 are inactive. An attempted read of this location will not cause the bus to be driven by the VL82C331. The System Controller will drive the bus. See the definition of REGTEST (85h) below.

REGTEST (85h) This register is intended for test purposes only. (Default = 77h)
Bit 7 is the same as MISCSET[7] at data port 14h. A write to REGTEST[7] is the same as a write to bit 7 of data port 14h in the VL82C331. However, this bit can also be read at REGTEST[7]. This allows testing of this bit at this data port address something not possible at data port 14h since the bit is write-only at that address.

Bit 6 is the same as RAMMAP[7] at data port 03h. A write to REGTEST[6] is the same as a write to bit 7 of data port 03h in the VL82C331. However, this bit can also be read at REGTEST[6]. This allows testing of this bit at this data port address; something not possible at data port 03h since the bit is write-only at that address.

Bit 3 is the same as REFCTL[3] at data port 06h. A write to REGTEST[3] is the same as a write to bit 3 of data port 06h in the VL82C331. However, this bit can also be read at REGTEST[3]. This allows testing of this bit at this data port address, something not possible at data port 06h since the bit is write-only at that address.

TABLE 13. ISA BUS CONTROLLER CONFIGURATION REGISTER MAP

Index Port	D7	D6	D5	D4	D3	D2	D1	D0
00ECh (W-O)	A7	A6	A5	A4	A3	A2	A1	A0

Data Port 00EDh		D7	D6	D5	D4	D3	D2	D1	D0
80	VER (R-O)	1	1	1	1	1	0	0	0
81	ROMDMA (R/W)	ROM Wait States		8-Bit DMA Wait States		16-Bit DMA Wait States		DMA Clock	MEMR Time
82	612AXS (R/W)	Enable FF	4XX Enable	1	1	1	1	1	FF PTR
13	SLEEP (W/O)	Enable	1	1	1	1	1	1	SYSCLK
83	SLPTST (R/W)	ENABLE	1	1	1	1	1	1	SYSCLK
84	BUSCTL (R/W)	1	RTC Ctrl	1	1	ADDLY	RLX Timing	16 WS	8 WS
14	MISCSET (W/O)	FX Enable	–	–	–	–	–	–	–
03	RAMMAP (W/O)	ROMSLOT	–	–	–	–	–	–	–
06	REFCLT (W/O)	–	–	–	–	10/16 IO	–	–	–
85	REGTEST (R/W)	FX Enable	ROMSLOT	1	1	10/16 IO	1	1	1

Note: A "1" indicates reserved register bits that read back as logic 1.
Registers containing bits with a "–" are write-only registers. The bus will not be driven during a read.

TABLE 14. CONFIGURATION REGISTER DEFAULTS ON RESET

Data Port 00EDh		D7	D6	D5	D4	D3	D2	D1	D0
80	VER (R-O)	1R	1R	1R	1R	0R	1R	0R	0R
81	ROMDMA (R/W)	1	1	1	1	1	1	0	0
82	612AXS (R/W)	0	0	1R	1R	1R	1R	1R	0
13	SLEEP (W/O)	0*	–	–	–	–	–	–	1*
83	SLPTST (R/W)	0*	1R	1R	1R	1R	1R	1R	1*
84	BUSCTL (R/W)	1R	0	1R	1R	0	0	0	0
14	MISCSET (W/O)	0+	–	–	–	–	–	–	–
03	RAMMAP (W/O)	1+	–	–	–	–	–	–	–
06	REFCTL (W/O)	–	–	–	–	0+	–	–	–
85	REGTEST (R/W)	0	1	1R	1R	0	1R	1R	1R

* These two bits are read/write at address 83H and write-only at address 13h. All other sleep register bits are inactive at 13h and read-only at 83h.

\+ These three bits are read/write at address 85h and write-only at address 03h, 06h and 14h. All other bits are inactive a 03h, 06h and 14h and read-only at 85h.

– Registers containing bits with a "–" are write-only registers. The bus will not be driven during a read.

AC CHARACTERISTICS: TA = 0°C to +70 °C, VDD = 5 V ±5%, VSS = 0V

Symbol	Parameter	Min	Max	Unit	Conditions
CPU Mode					
t1	BUSCLK Period	31		ns	
t2	BUSCLK High Time	12		ns	1.5 V (Note 1)
t3	BUSCLK Low Time	12		ns	1.5 V (Note 1)
t7	SYSCLK Fall Time		10	ns	0.8 V to 2.0 V @ CL=200 (Note 1)
t8	SYSCLK Rise Time		10	ns	0.8 V to 2.0 V @ CL=200 (Note 1)
tD9	BUSCLK to SYSCLK Delay	3	26	ns	CL=200 pF
tSU10	–CHSO, –CHS1, CHM/–IO to BUSCLK Setup Time	12		ns	(Note 2)
tH11	–CHS0, –CHS1, CHM/–IO fro BUSCLK Hold Time	4		ns	(Note 2)
tD12	BALE from BUSCLK Delay	3	28	ns	CL=200 pF
t13	BALE Pulse Width	41		ns	
tD14	–CHREADY from BUSCLK Delay	3	25	ns	CL=50 pF
tSU15	A23-A2, –BE3- –BE0 to –EALE Setup Time	12		ns	
tH16	A23-A2, –BE3- –BE0 from –EALE Hold Time	4		ns	
tD17	LA Bus Valid from A Bus	3	35	ns	Standard Bus Cycles. CL=200 pF (Note 3)
tD17a	LA Bus Valid from –EALE Delay	3	40	ns	First cycle following decoupled refresh. CL=200 pF (Note 3)
tD18	SA Bus, –SBHE Valid from BUSCLK Delay	3	40	ns	CL=200 pF (Note 4)
tD19	–CMD from BUSCLK Delay	3	35	ns	CL=200 pF (Note 5)
tSU20	–MEMCS16 to BUSCLK Setup Time	18		ns	
tH21	–MEMCS16 from BUSCLK Hold Time	5		ns	
tSU22	–WS0 to BUSCLK Setup Time	15		ns	
tH23	–WS0 from BUSCLK Hold Time	5	40	ns	
tD24	–XDREAD from BUSCLK Delay	3	40	ns	CL=50 pF
tD25	–SCMD Valid from BUSCLK Delay	3	35	ns	CL=200 pF (Note 6)
tD26	–SCMD Active from BUSCLK Delay	3		ns	CL=200 pF (Note 1)
tD27	–SCMD Float from BUSCLK Delay			ns	CL=200 pF (Note 1)
tSU28	IOCHRDY to BUSCLK Setup Time	12	40	ns	
tH29	IOCHRDY from BUSCLK Hold Time	5		ns	
tSU30	–IOCS16 to BUSCLK Setup Time	18		ns	
tH31	–IOCS16 from BUSCLK Hold Time	5		ns	
tD32	–LATLO, –LATHI Delay from BUSCLK	3	40	ns	CL=50 pF
tD33	–SDSWAP Delay from BUSCLK	3	45	ns	CL=50 pF
tD34	–SDSWAP Delay from –IOCS16	3	25	ns	Late –IOCS16. Read cycles only. CL=50 pF
tD35	SDLH/–HL Delay from BUSCLK	3	45	ns	CL=50 pF

AC CHARACTERISTICS: TA = 0°C to +70 °C, VDD = 5 V ±5%, VSS = 0V (Cont.)

Symbol	Parameter	Min	Max	Unit	Conditions
CPU Mode (Cont.)					
tD36	XD Bus Delay from BUSCLK	3	150	ns	CL=50 pF (Note 7)
tD38	XD Bus Float from BUSCLK	3	55	ns	CL=50 pF (Note 7)
tSU39	XD Bus to BUSCLK Setup Time	75	18	ns	(Note 7)
tH40	XD Bus from BUSCLK Hold Time	30	17	ns	(Note 7)
tD41	CS8042/–RTC Delay from BUSCLK	3	50	ns	CL=50 pF
tD42	SPKR, NMI Delay from BUSCLK	3	60	ns	Following write to Port B. CL=50 pF
Bus Arbitration Timing					
tD43	AEN from CPUHLDA Delay	3	35	ns	CL=200 pF
tD44	ALE from CPUHLDA Delay	3	35	ns	CL=200 pF
tD45	–MR/–MW Active from CPUHLDA Delay	3		ns	CL=50 pF (Note 1)
tD46	–MR/–MW Float from CPUHLDA Delay		30	ns	CL=50 pF (Note 1)
tD47	SA/LA Bus, –SBHE, –MEMR Active from –REFRESH	3		ns	CL=200 pF (Notes 3, 4)
tD48	SA/LA Bus, –SBHE, –MEMR Float from –REFRESH		50	ns	CL=200 pF (Notes 3, 4)
Interrupt Timing					
t50	External Interrupt Request Pulse Width Low	90		ns	
tD51	INTR Active Delay from External IRQ	3	130	ns	CL=50 pF
tD52	INTR Inactive from BUSCLK	3	110	ns	Following 2nd interrupt acknowledge pulse. CL=50 pF
Miscellaneous Timing					
tD55	NMI Delay from –PCK, –IOCHK	3	50	ns	CL=50 pF
tD56	LA20 from –BLKA20 Delay	3	35	ns	CL=200 pF
tD57	–TRI Delay (Three State All Outputs, I/Os)		150	ns	AC timing not 100% tested.
tD58	INTR Active Delay from XTALIN	3	350	ns	When source is internal IRQ8 (RTC) interrupt. CL=50 pF
tD59	PS Pulse Width	1		µs	
tH60	PS Hold Following VBAT > VBAT (min.)	1		µs	
tD61	VRT Bit Delay		1	µs	Following read of RTC register D.
tH62	POWERGOOD Active Hold from VDD > VDD (min.)	1		µs	
tH63	VDD > VDD (min.) Hold after POWERGOOD Low	1		µs	To ensure RTC data integrity.
tSU64	POWERGOOD to BUSCLK Setup Time	25		ns	(Note 2)
tH65	POWERGOOD from BUSCLK Hold Time	10		ns	(Note 2)
tD66	RSTDRV from BUSCLK Delay		35	ns	

AC CHARACTERISTICS: TA = 0°C to +70 °C, VDD = 5 V ±5%, VSS = 0V (Cont.)

Symbol	Parameter	Min	Max	Unit	Conditions
Timer/Counter Timing					
t67	OSC Period	50		ns	
t68	OSC High Time	20		ns	0.8 V to 2.0 V (Note 1)
t69	OSC Low Time	20		ns	0.8 V to 2.0 V (Note 1)
tD70	OUT1, SPKR Delay from OSC	3	120	ns	CL=50 pF
tD71	INTR Delay from OSC	3	200	ns	When source is from internal IRQ0. CL=50 pF
DMA Mode					
tSU73	DRQ to BUSCLK Setup Time	0		ns	
tD74	–DACK from BUSCLK Delay	3	100	ns	CL=100 pF
tD75	–CMD Valid from BUSCLK Delay	3	85	ns	CL=200 pF (Note 5)
tD76	–MR/–MW Valid from BUSCLK Delay	3	80	ns	CL=50 pF
tD77	A Bus, –BE3- –BE0 Valid from BUSCLK Delay	3	125	ns	CL=50 pF
tD78	A Bus, –BE3- –BE0 Active from BUSCLK Delay	3		ns	CL=50 pF (Note 1)
tD79	A Bus, –BE3- –BE0 Float from BUSCLK Delay		80	ns	CL=50 pF (Note 1)
tD80	SA, –SBHE Valid from BUSCLK Delay	3	115	ns	CL=200 pF
tD81	LA23-LA17 Valid from BUSCLK Delay	3	130	ns	CL=200 pF
tD82	DMAHRQ from BUSCLK Delay	3	70	ns	CL=50 pF
tSU83	DMAHLDA to BUSCLK Setup Time	25	85	ns	(Note 2)
tH83a	DMAHLDA from BUSCLK Hold Time	20	80	ns	(Note 2)
tD84	T/C from BUSCLK Delay	3	85	ns	CL=50 pF
tSU85	IOCHRDY to BUSCLK Setup Time	15		ns	
tH86	IOCHRDY from BUSCLK Hold Time	20		ns	
tD87	–SCMD Valid from BUSCLK Delay	3	85	ns	CL=200 pF (Note 6)
tD88	–SCMD Active from BUSCLK Delay	3		ns	CL=200 pF (Notes 1, 6)
tD89	–SCMD Float from BUSCLK Delay		135	ns	CL=200 pF (Notes 1, 6)
tD90	–SDSWAP Delay from BUSCLK	3	125	ns	CL=50 pF
tD90a	–SDSWAP Delay from –MEMCS16	3	35	ns	CL=50 pF
tD90b	–SDSWAP Delay from –BRDRAM	3	35	ns	CL=50 pF
tD91	SDLH/–HL Delay from BUSCLK	3	130	ns	CL=50 pF
tD91a	SDLH/–HL Delay from –MEMCS16	3	35	ns	CL=50 pF
tD91b	SDLH/–HL Delay from –BRDRAM	3	35	ns	CL=50 pF
tD95	–LATLO/–LATHI Delay from BUSCLK	3	115	ns	CL=50 pF

AC CHARACTERISTICS: TA = 0°C to +70 °C, VDD = 5 V ±5%, VSS = 0V (Cont.)

Symbol	Parameter	Min	Max	Unit	Conditions
Master Mode					
tD96	SA/LA Bus, –CMD Float from –MASTER Low		30	ns	CL=200 pF (Notes 1, 3, 4)
tD97	SA/LA Bus, –CMD Active from –MASTER High	3		ns	CL=200 pF (Notes 1, 3, 4)
tD98	A Bus, –BE3- –BE0 Active from –MASTER Low	3		ns	CL=50 pF (Note 1)
tD99	A Bus, –BE3- –BE0 Float from –MASTER High		25	ns	CL=50 pF (Note 1)
tD100	AEN Delay from –MASTER	3	35	ns	CL=200 pF
tSU101	LA/SA Bus, –SBHE to –CMD Setup Time	75		ns	(Notes 3, 4, 7)
tH102	LA/SA Bus, –SBHE to –CMD Hold Time	20		ns	(Notes 3, 4, 7)
t103	–CMD Pulse Width	187		ns	(Notes 5)
tD104	–MR/–MW Delay from –MEMW/–MEMR	3	25	ns	CL=50 pF
tSU105	XD to –IOW Setup Time	100		ns	(Note 7)
tH106	XD to –IOW Hold Time	20		ns	(Note 7)
tD107	XD from –IOR Delay Time	3	135	ns	CL=50 pF (Note 7)
tD108	XD Float Delay from –IOR Inactive	3	40	ns	CL=50 pF (Notes 1, 7)
tD109	LA/SA Bus, –SBHE to A Bus, –BE Delay	3	35	ns	CL=50 pF (Notes 3, 4)
tD110	–CS8042 Delay from SA, LA Bus Valid	3	40	ns	CL=50 pF (Notes 3, 4)
tD111	SPKR, NMI Delay from –IOW Inactive	3	45	ns	Following write to Port B. CL=50 pF
tD112	–XDREAD from –IOR Delay	3	30	ns	CL=50 pF
tD113	–LATLO, –LATHI Delay from –IOR/–MEMR	3	30	ns	CL=50 pF
tD114	–SDSWAP Delay from –CMD	3	35	ns	CL=50 pF (Note 5)
tD115	–SDSWAP Delay from CONTROL	3	35	ns	CL=50 pF (Note 8)
tD119	SDLH/–HL Delay from –CMD	3	35	ns	CL=50 pF (Note 5)
tD120	SDLH/–HL Delay from CONTROL	3	35	ns	CL=50 pF (Note 8)
tD124	–SCMD Valid from –MEMW/–MEMR Delay	3	30	ns	CL=200 pF (Note 6)
tD125	–SCMD Active from LA Bus Delay	3		ns	CL=200 pF (Notes 1, 3, 6)
tD126	–SCMD Float from LA Bus Delay		30	ns	CL=200 pF (Notes 1, 3, 6)
tD127	LA Bus Valid, –SBHE Low from –REFRESH	3	70	ns	CL=200 pF (Note 3)
tD128	–MEMR from BUSCLK Delay	3	50	ns	CL=200 pF (Note 9)
tD129	–MR from BUSCLK Delay	3	45	ns	CL=50 pF (Note 9)
tSU130	–REFRESH to BUSCLK Setup Time	20		ns	(Note 2)
tD131	–REFRESH from BUSCLK Delay (Release)	3	50	ns	Until refresh is no longer driven. CL=200 pF (Note 9)
tD132	–SMEMR Valid from BUSCLK Delay	3	50	ns	CL=200 pF (Note 9)
tD133	–SMEMR Active from –REFRESH Delay	3		ns	CL=200 pF (Note 1)

AC CHARACTERISTICS: TA = 0°C to +70 °C, VDD = 5 V ±5%, VSS = 0V (Cont.)

Symbol	Parameter	Min	Max	Unit	Conditions
Master Mode (Cont.)					
tD134	–SMEMR Float from BUSCLK Delay		60	ns	CL=200 pF (Notes 1 and 9)
tSU135	IOCHRDY Setup to BUSCLK	5		ns	(Note 9)
tH136	IOCHRDY Hold from BUSCLK	20		ns	(Note 9)
tD137	SA Bus Valid from BUSCLK Delay	3	60	ns	CL=200 pF (Notes 4, 9)
Decoupled REFRESH Mode					
tD138	LA Bus Valid, –SBHE Low from –BUSCLK	3	80	ns	CL=200 pF (Note 3)
tD139	–REFRESH from BUSCLK Delay (Active)	3	40	ns	CL=200 pF (Note 2)
tD140	–SCMD Active from BUSCLK Delay	3		ns	CL=200 pF (Notes 1, 6)
tD141	AEN Delay from BUSCLK	3	55	ns	CL=200 pF
tD142	ALE Delay from BUSCLK	3	55	ns	CL=200 pF

Notes:
1. Specification is characterized and guaranteed, not 100% tested.
2. Asynchronous input, for test purposes only.
3. LA bus refers to LA23-LA17.
4. SA bus refers to the signal pins SA19-SA0.
5. –CMD refers to the signals –MEMR, –MEMW, –IOR, –IOW.
6. –SCMD refers to the signals –SMEMR, –SMEMW.
7. Internal register accesses.
8. –CONTROL refers to –MEMCS16, –IOCS16, SA0, –BRDRAM.
9. Specification also applies to decoupled refresh mode cycles.

FIGURE 5. 16 TO 8 CONVERSION - I/O READS

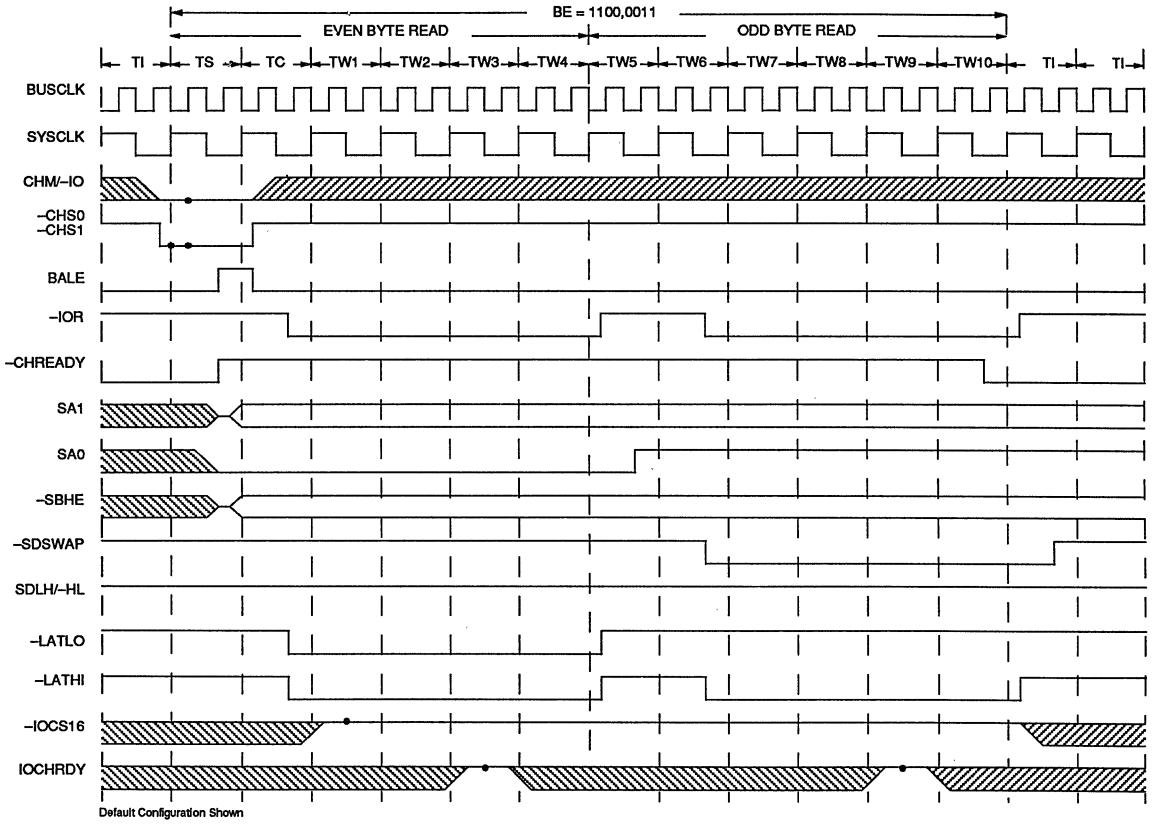


FIGURE 6. 16 TO 8 CONVERSION - I/O WRITES

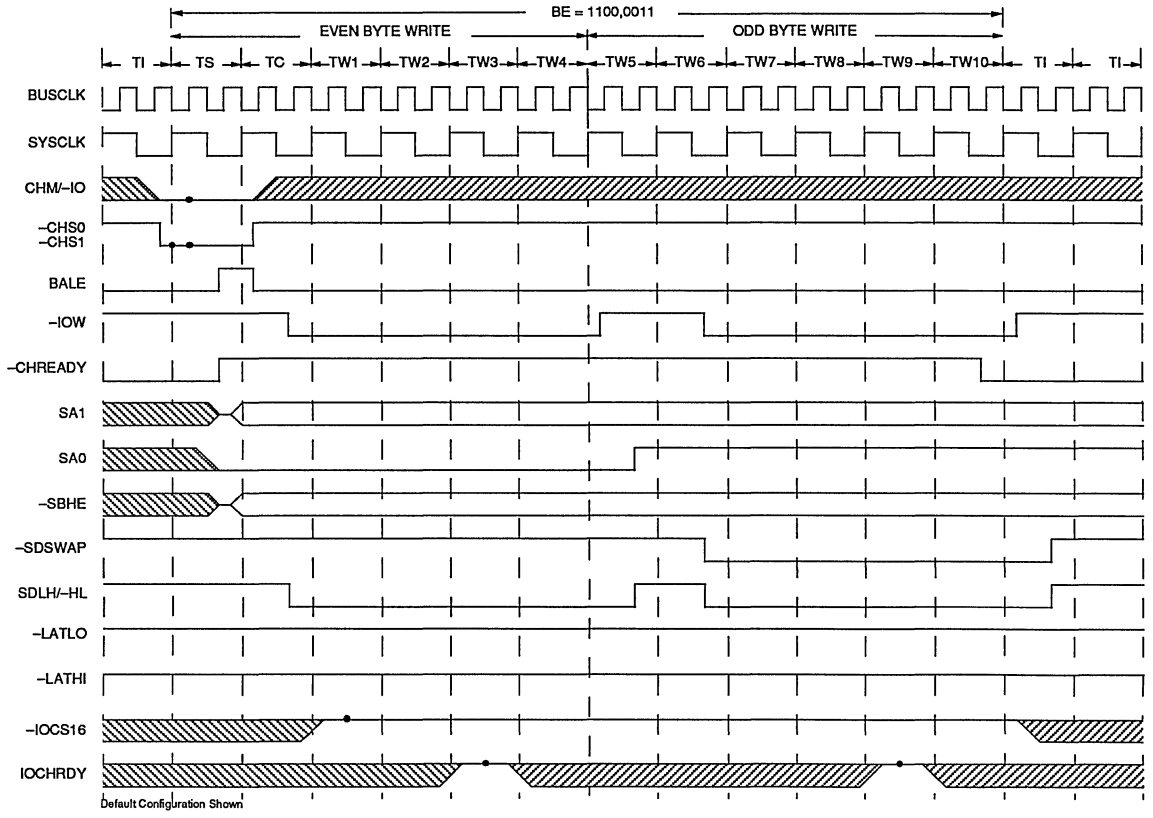


FIGURE 7. 16 TO 8 CONVERSION - MEMORY READS

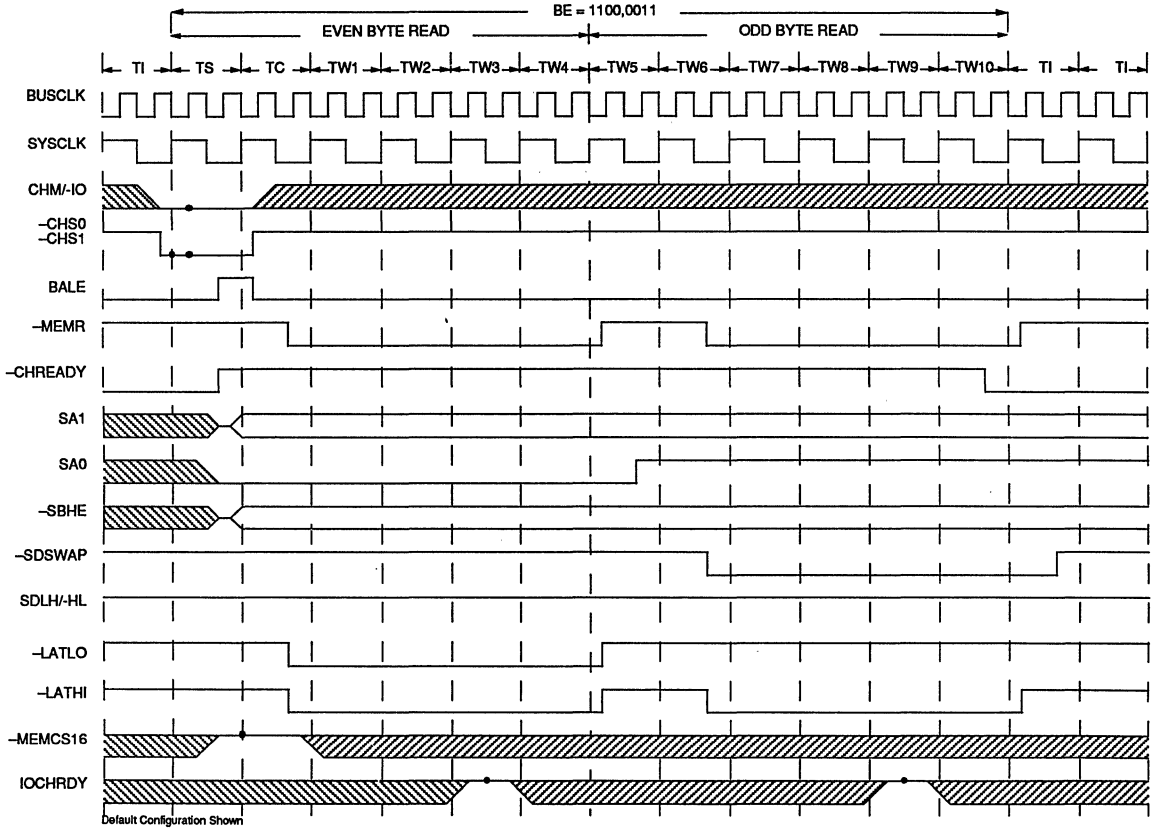


FIGURE 8. 16 TO 8 CONVERSION - MEMORY WRITES

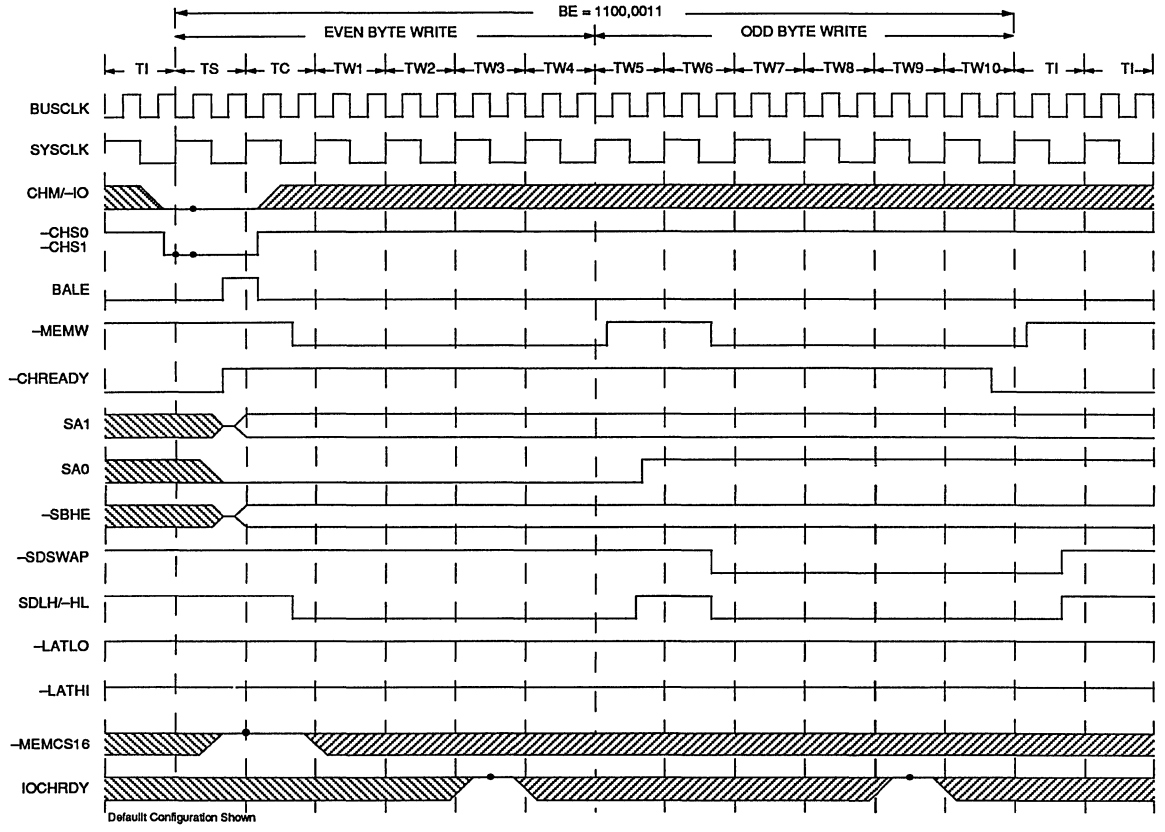


FIGURE 9. 24 TO 8 CONVERSION - I/O READ

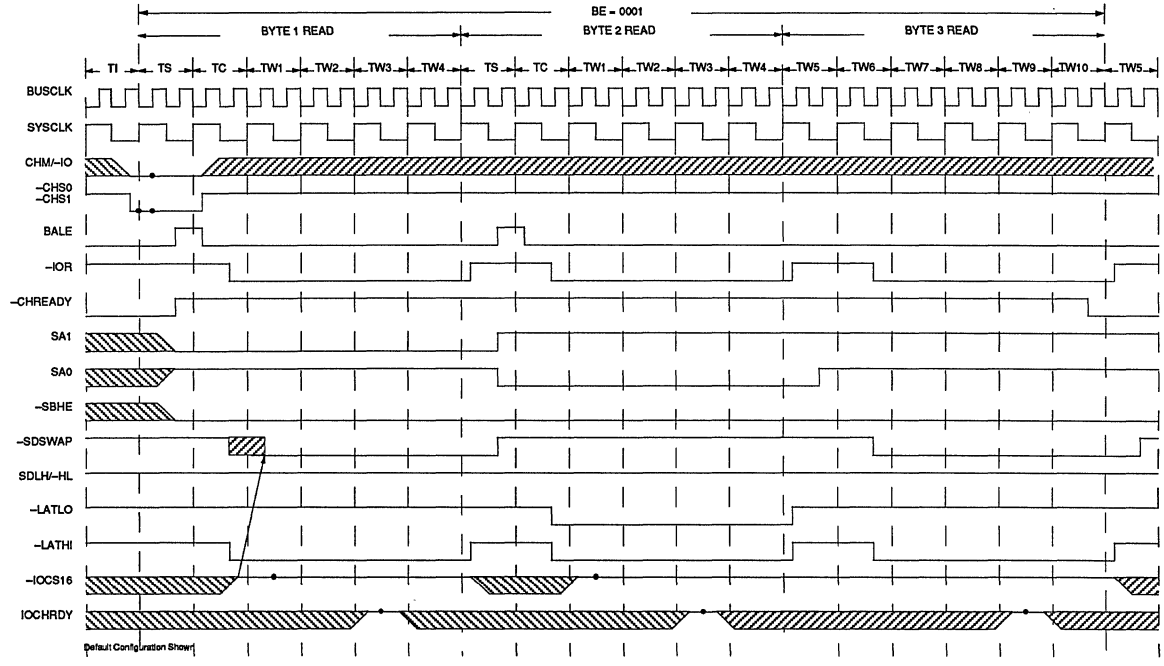


FIGURE 10. 24 TO 8 CONVERSION - I/O WRITE

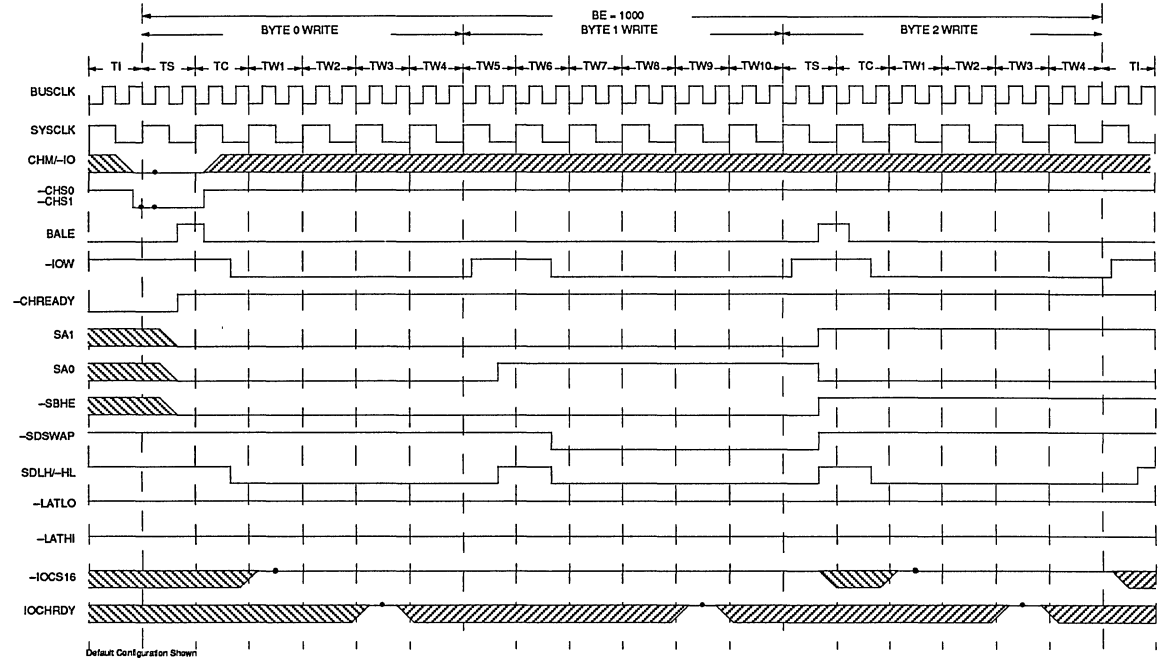


FIGURE 11. 32 TO 8 CONVERSION - MEMORY READ

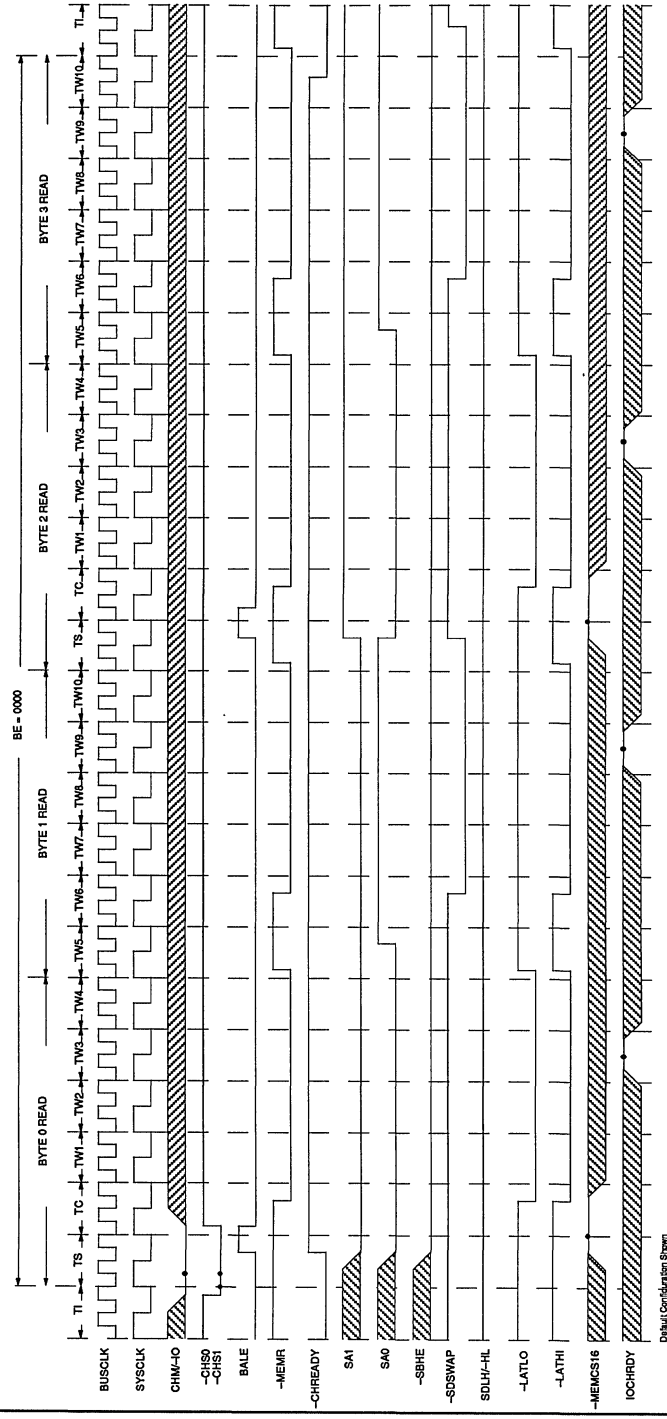


FIGURE 12. 32 TO 8 CONVERSION - MEMORY WRITE

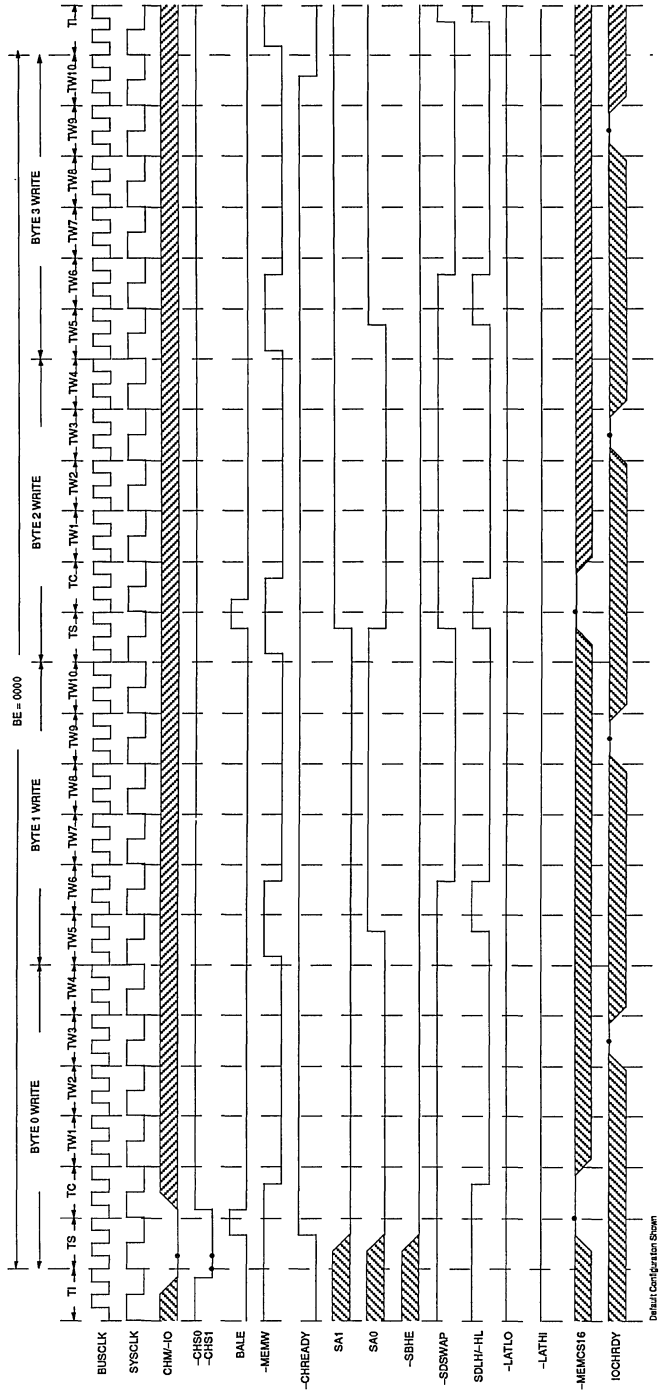


FIGURE 13. 24 TO 16 CONVERSION - MEMORY READS

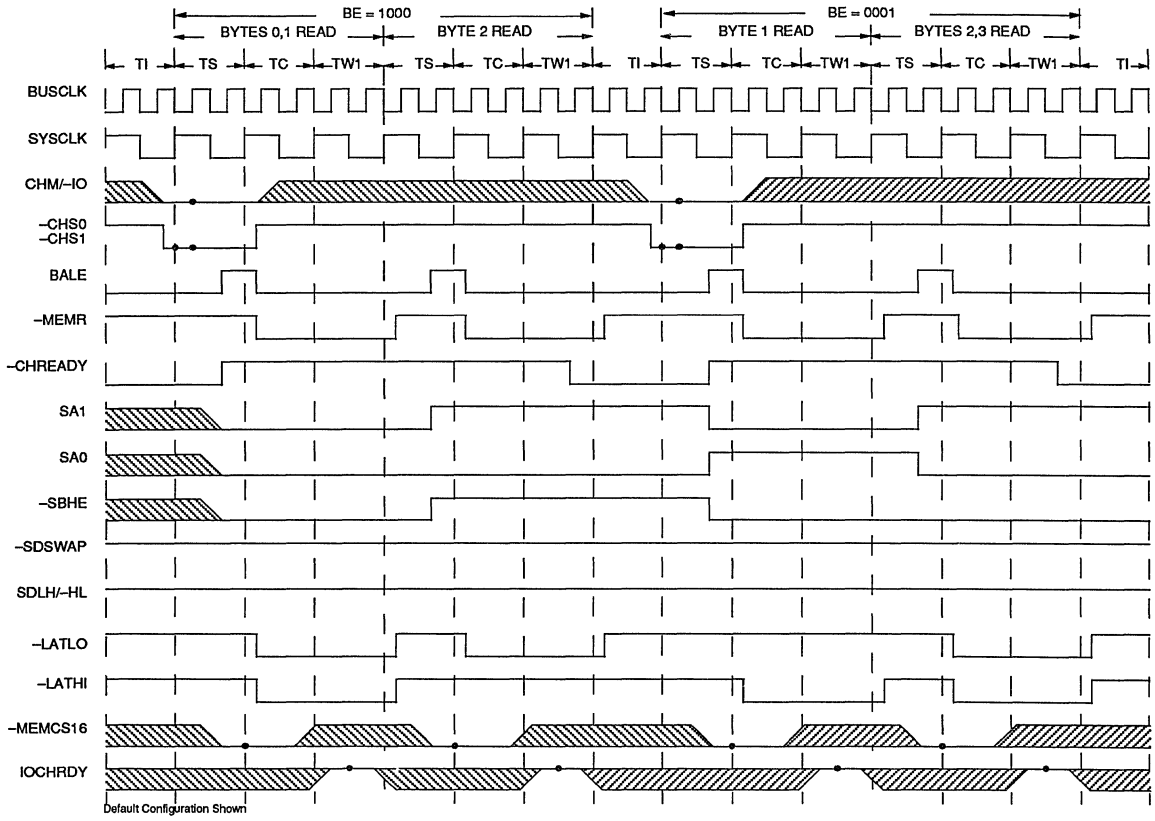
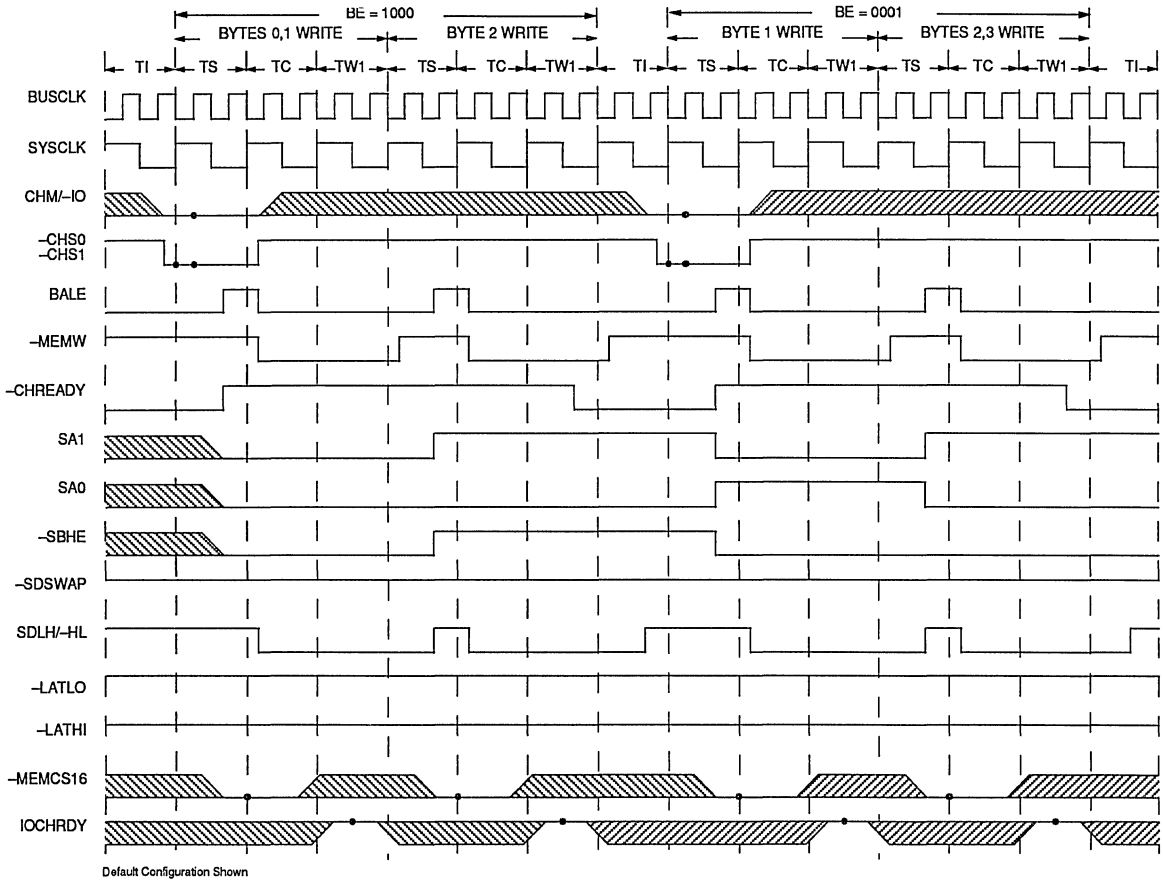


FIGURE 14. 24 TO 16 CONVERSION - MEMORY WRITES



Default Configuration Shown

FIGURE 15. 32 TO 16 CONVERSION - MEMORY READS

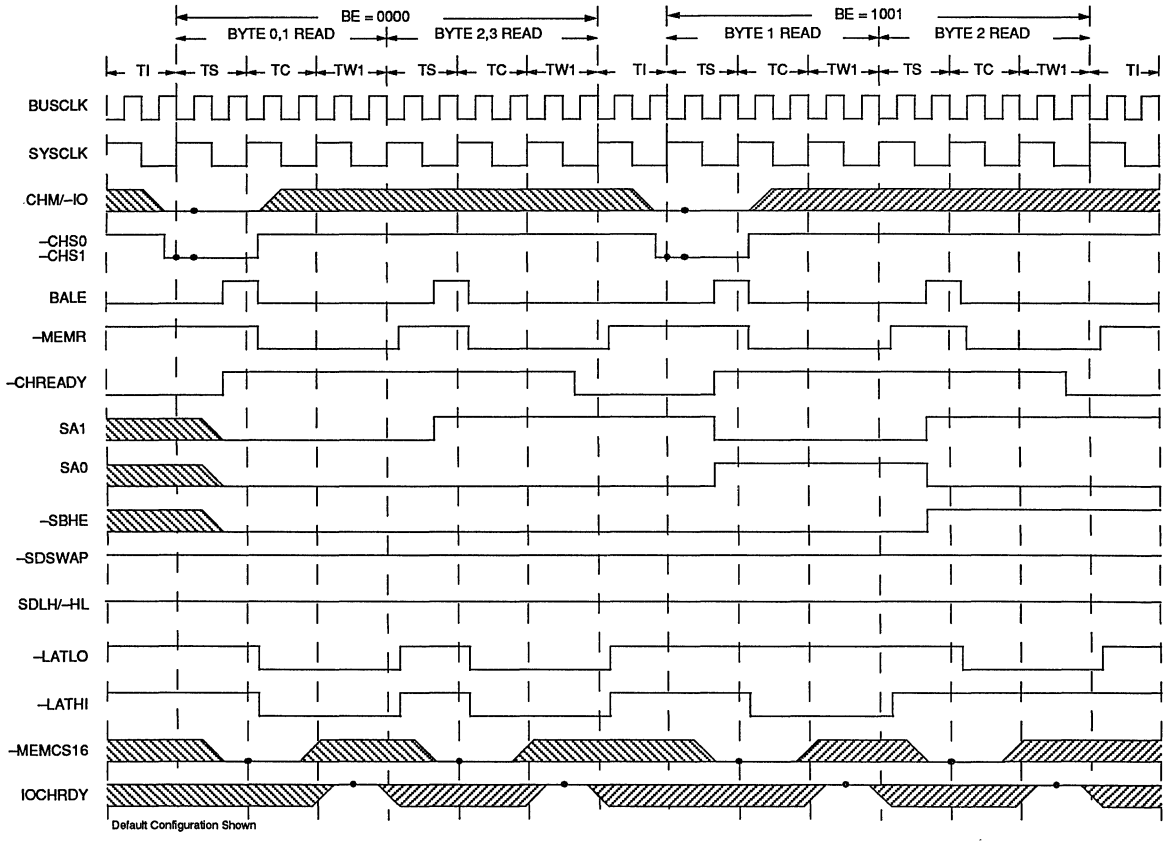


FIGURE 16. 32 TO 16 CONVERSION - MEMORY WRITES

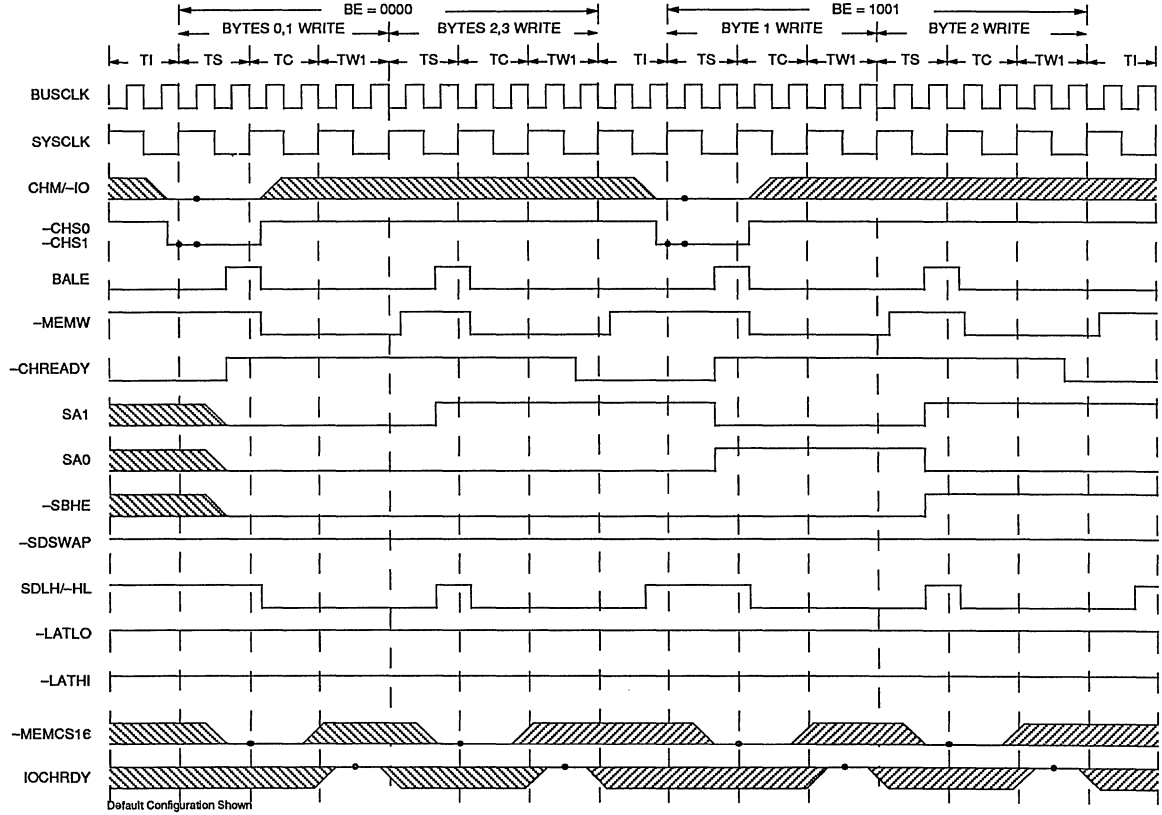


FIGURE 17. 32 TO 16 CONVERSION - I/O READS

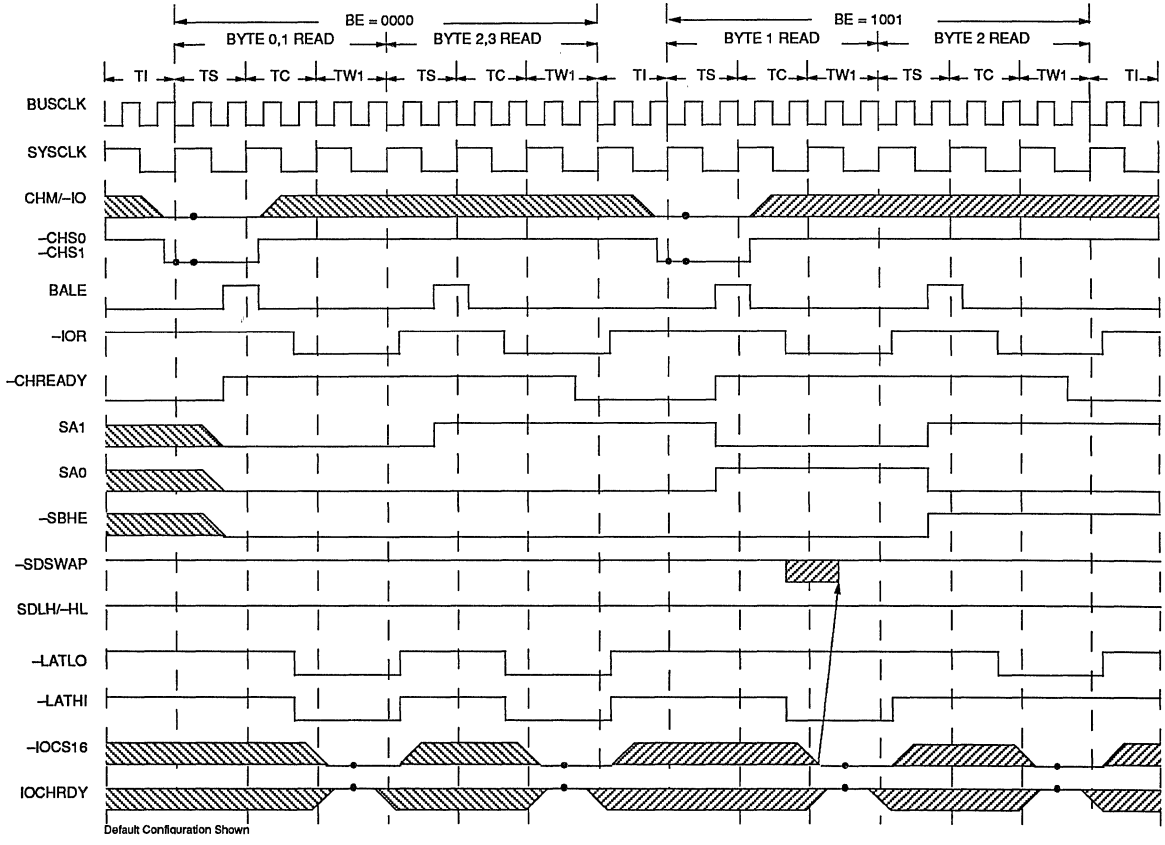


FIGURE 18. 32 TO 16 CONVERSION - I/O WRITES

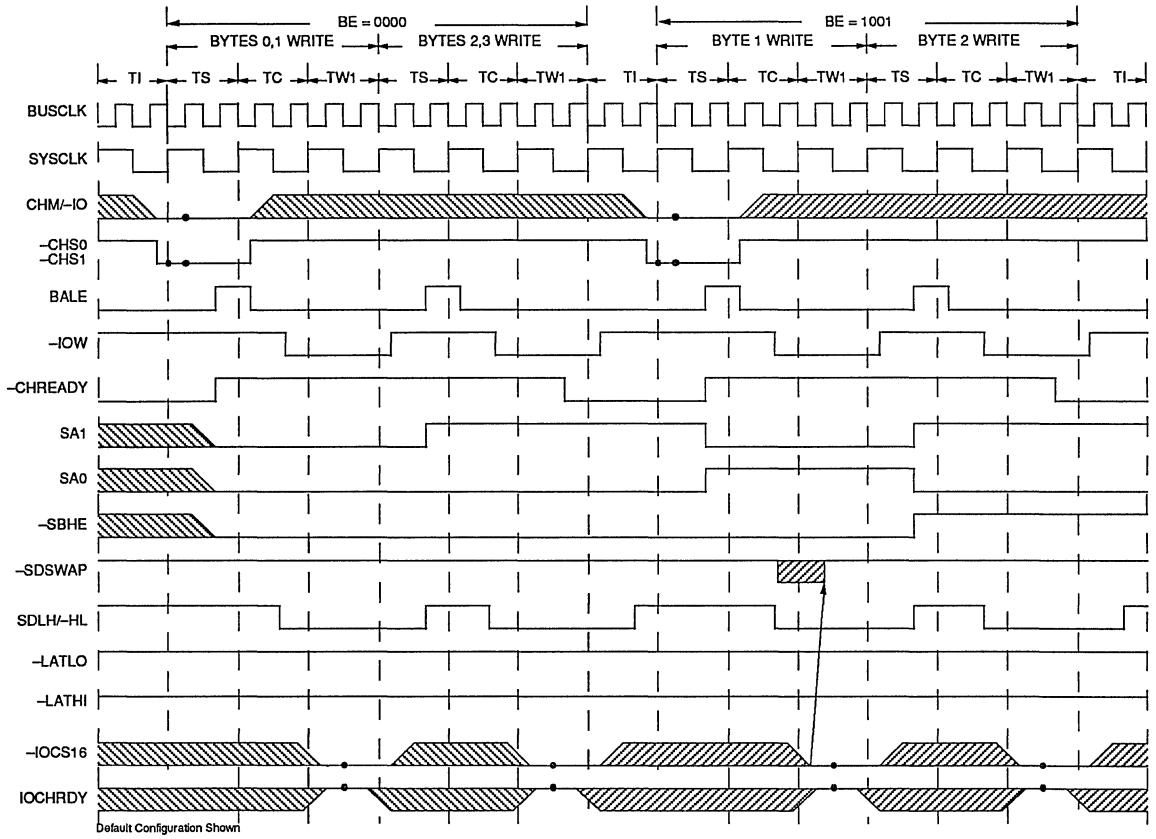
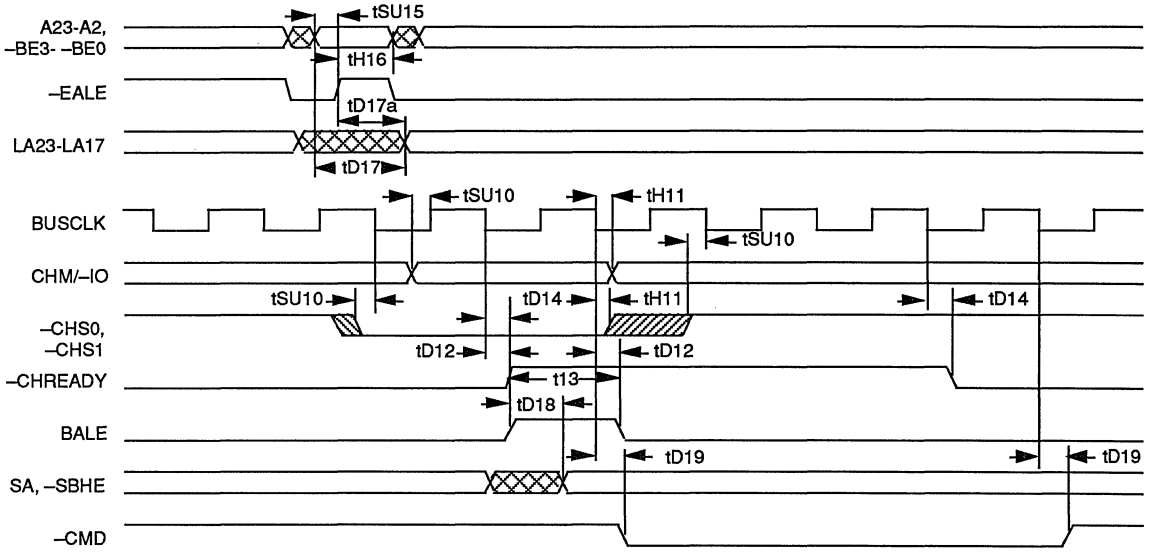


FIGURE 19. ASYNCHRONOUS BUS INTERFACE



Note: 16-bit memory cycle shown.

FIGURE 20. CPU MODE I/O CYCLE (16/8-BIT)

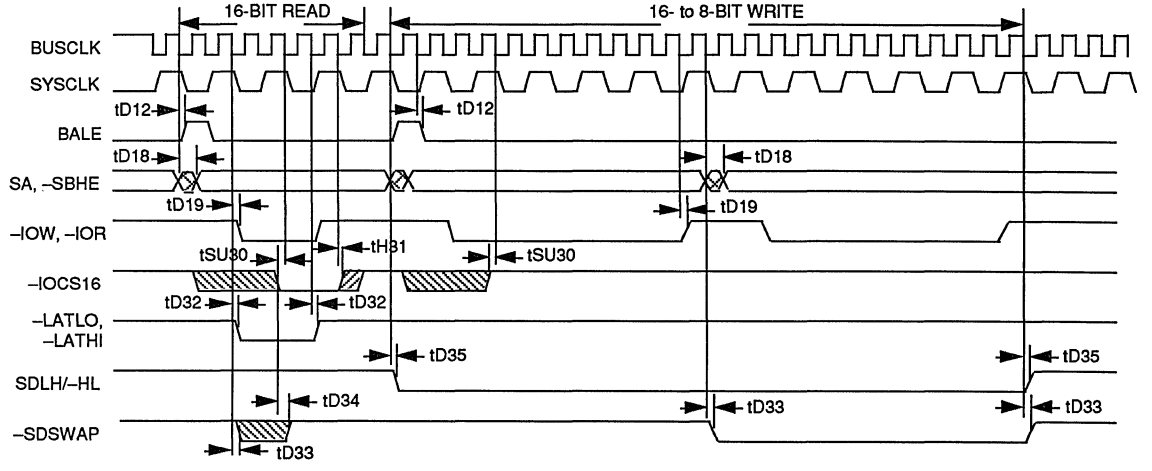
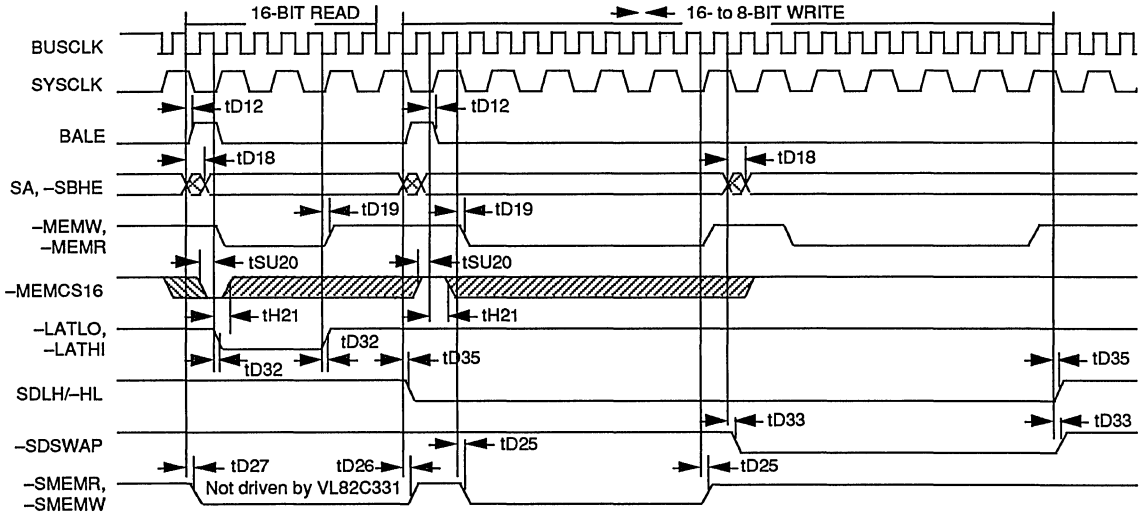
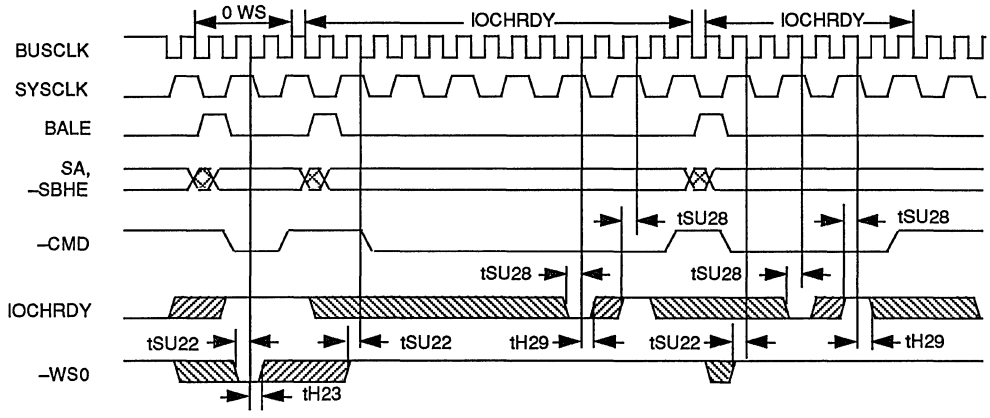


FIGURE 21. CPU MODE MEMORY CYCLE TIMING (16/8-BIT)



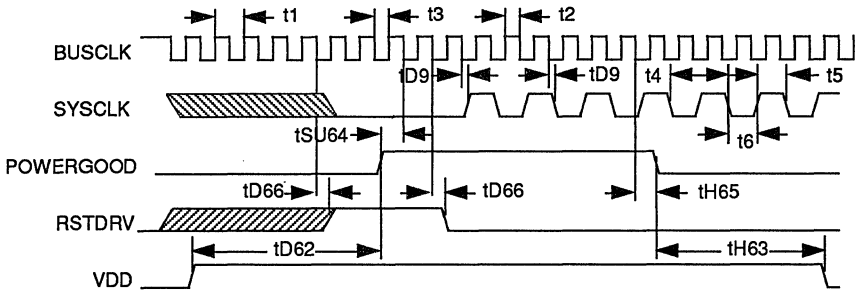
Note: -SMEMR and -SMEMW are three-stated for addresses above 1 meg. These should be pulled up externally with a 10K resistor.

FIGURE 22. CPU MODE WS0 AND IOCHRDY



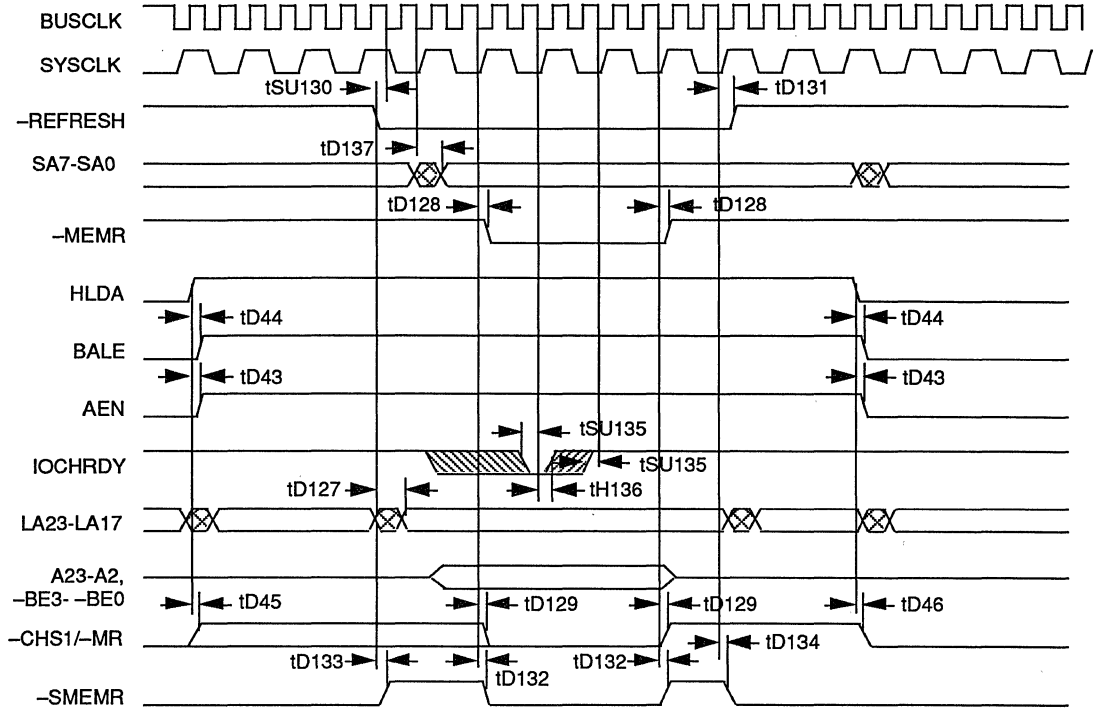
Note: 1. Zero wait state cycle shown is a 16-bit memory cycle. IOCHRDY cycles are 8-bit and 16-bit memory cycles.
2. IOCHRDY and WS0 should not be asserted at the same time. WS0 takes precedence over IOCHRDY.

FIGURE 23. CLOCK/RESET



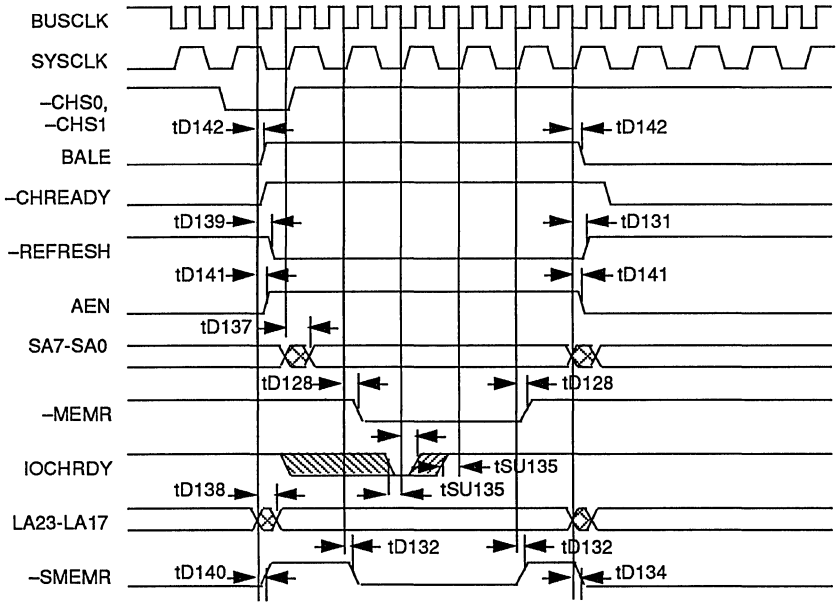
Note: POWERGOOD is an asynchronous input. This specification is given for testing purposes only. The specifications on POWERGOOD with respect to VDD are given to ensure predictable behavior. They also guarantee protection of the RTC battery-backed registers.

FIGURE 24. COUPLED REFRESH



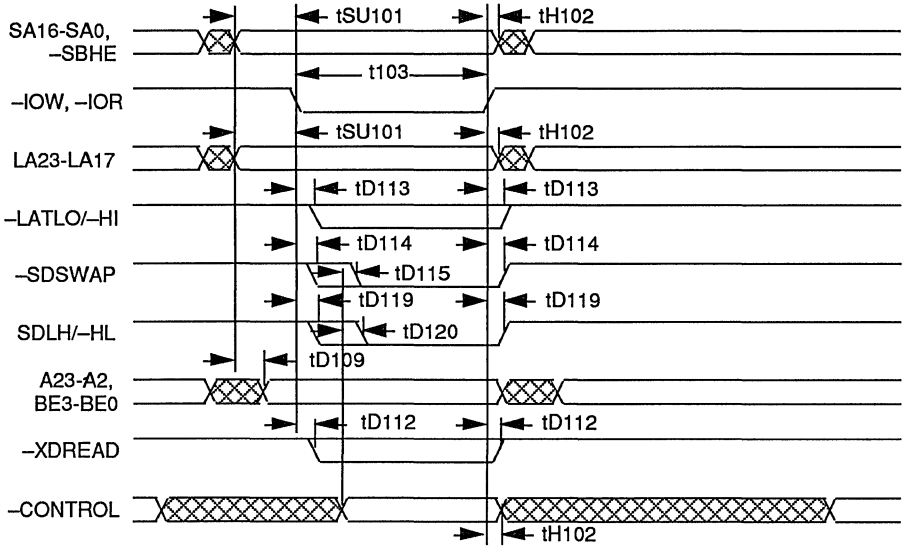
Note: –SMEMR is three-stated for addresses above 1 meg. It should be pulled up externally with a 10K resistor.

FIGURE 25. DECOUPLED REFRESH



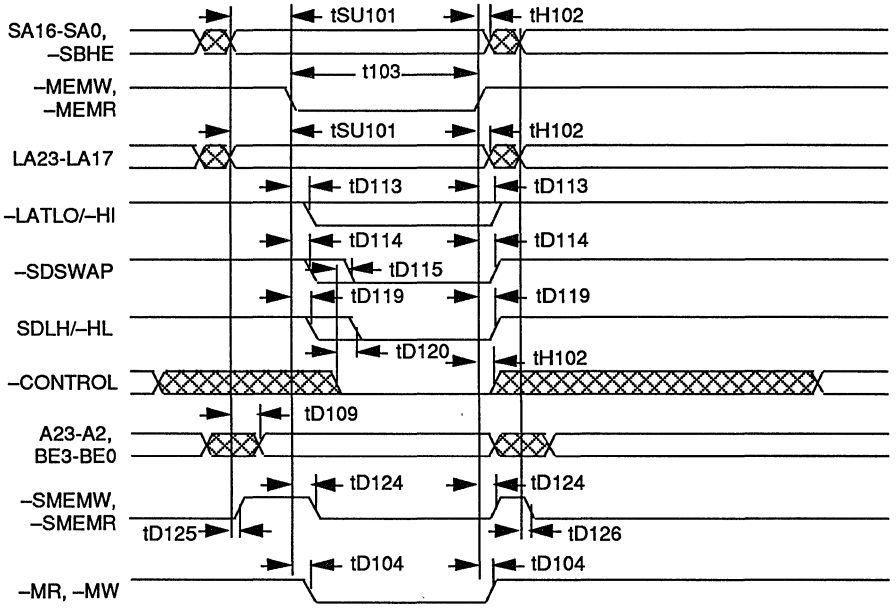
Note: -SMEMR is three stated for addresses above 1 meg. It should be pulled up externally with a 10K resistor.

FIGURE 26. MASTER MODE CYCLE (I/O ACCESS)



Note: -CONTROL refers to the signals -IOCS16, -MEMCS16, -BRDRAM and SA0.

FIGURE 27. MASTER MODE CYCLE (MEMORY ACCESS)



Note: -CONTROL refers to the signals -IOCS16, -MEMCS16, -BRDRAM and SA0.

FIGURE 28. DMA MODE CYCLE (8-BIT)

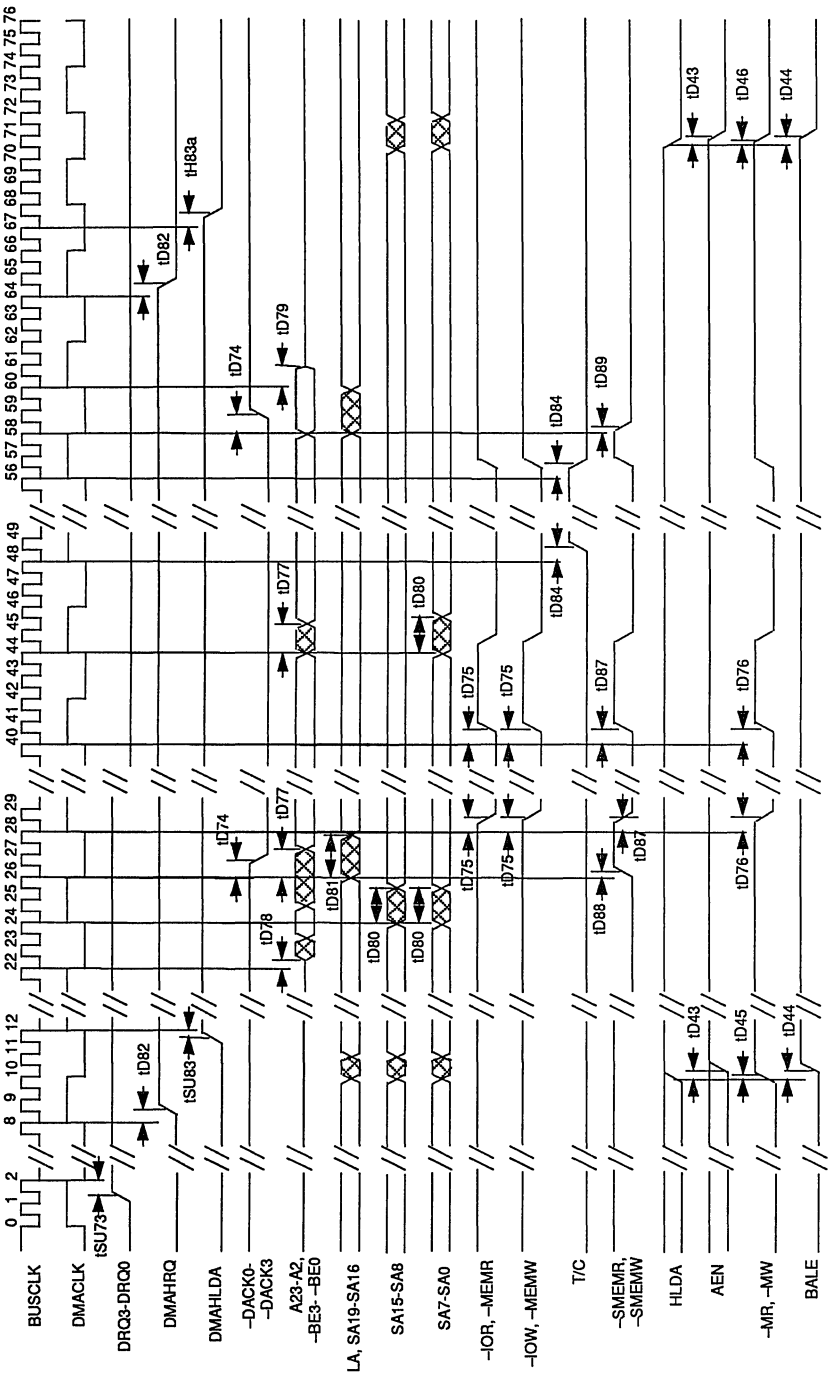


FIGURE 29. DMA MODE CYCLE (16-BIT)

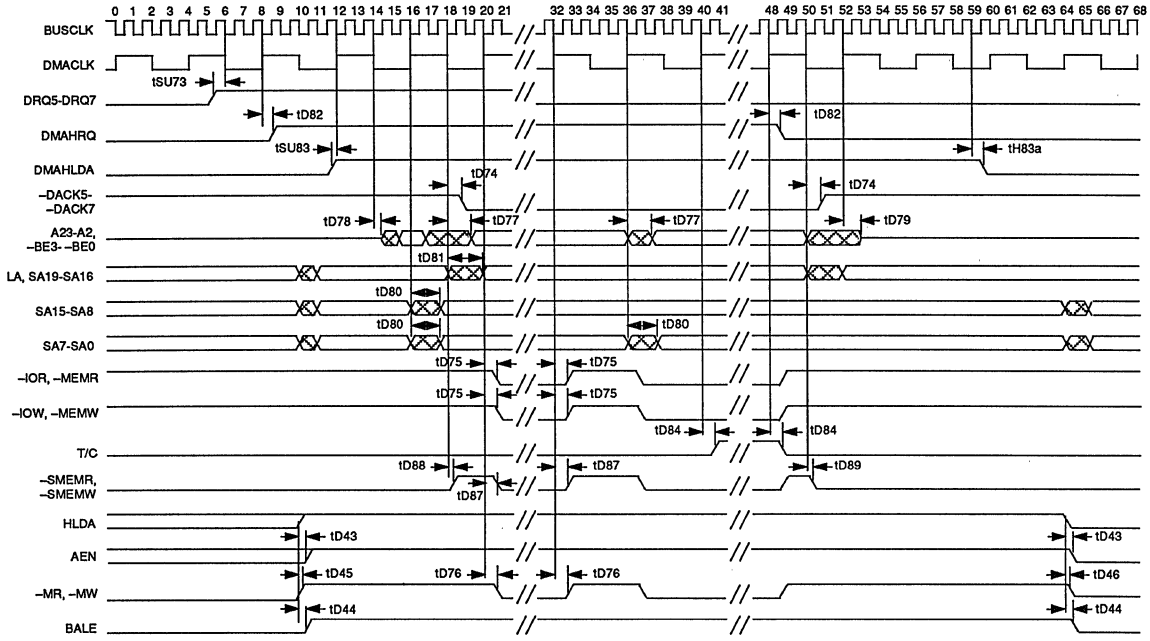


FIGURE 30. MASTER MODE ARBITRATION

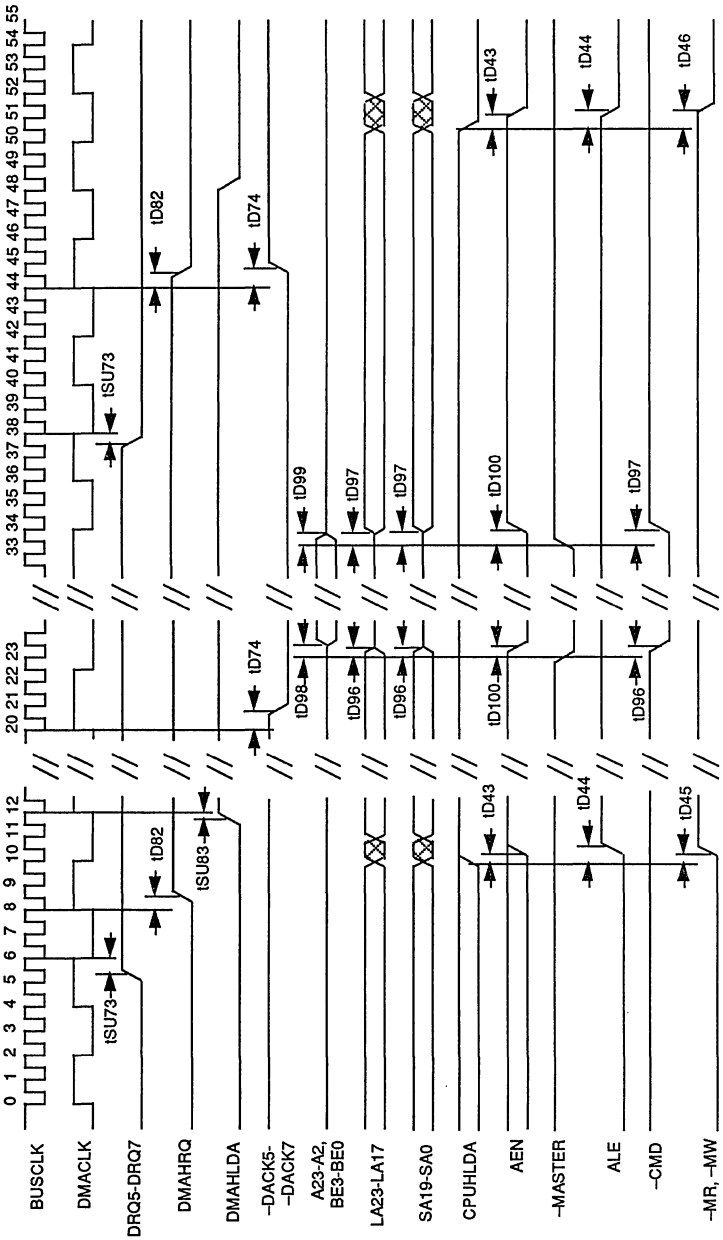


FIGURE 31. INTERRUPT/ACKNOWLEDGE CYCLE

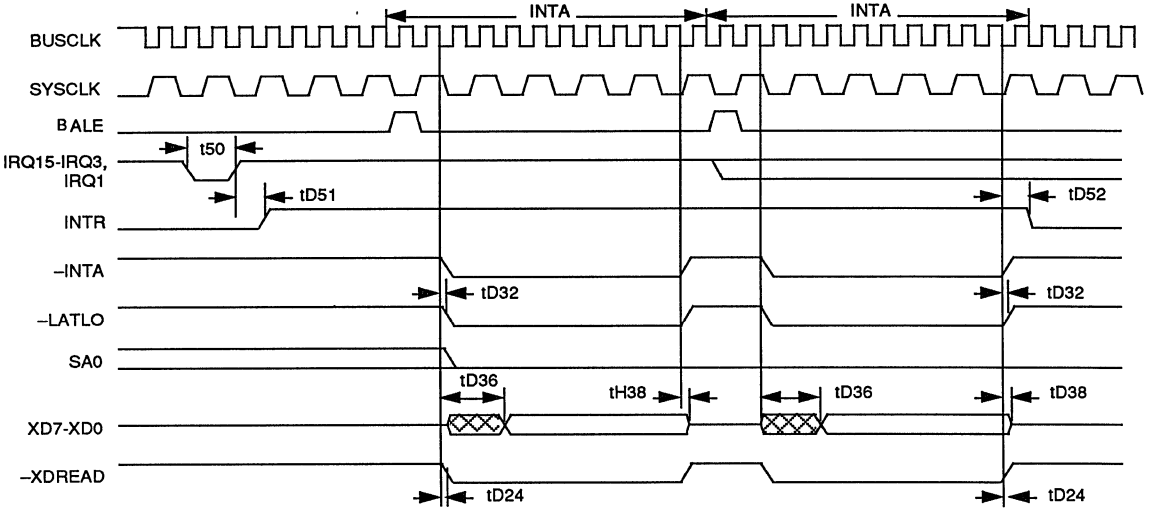
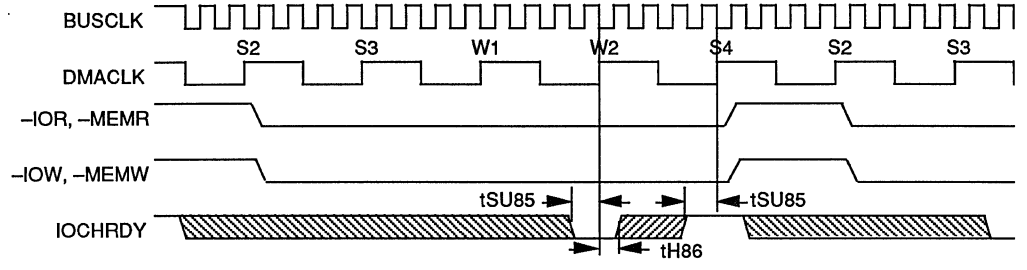


FIGURE 32. IOCHRDY (DMA CYCLES)



Note: The first wait state is automatically inserted by internal circuitry for all DMA cycles. Any additional wait states must be inserted using IOCHRDY.

FIGURE 33. CPU MODE ACCESS (INTERNAL REGISTERS)

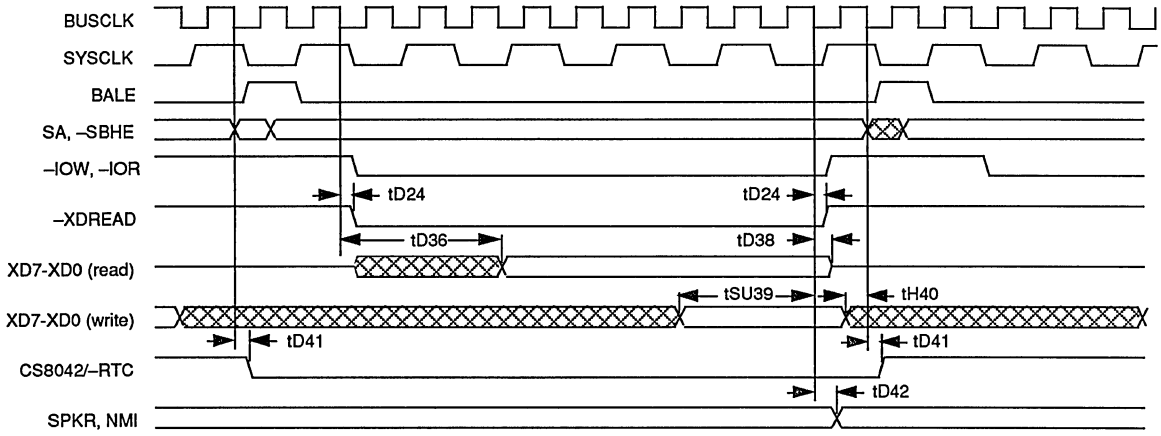


FIGURE 34. MISCELLANEOUS/PERIPHERAL

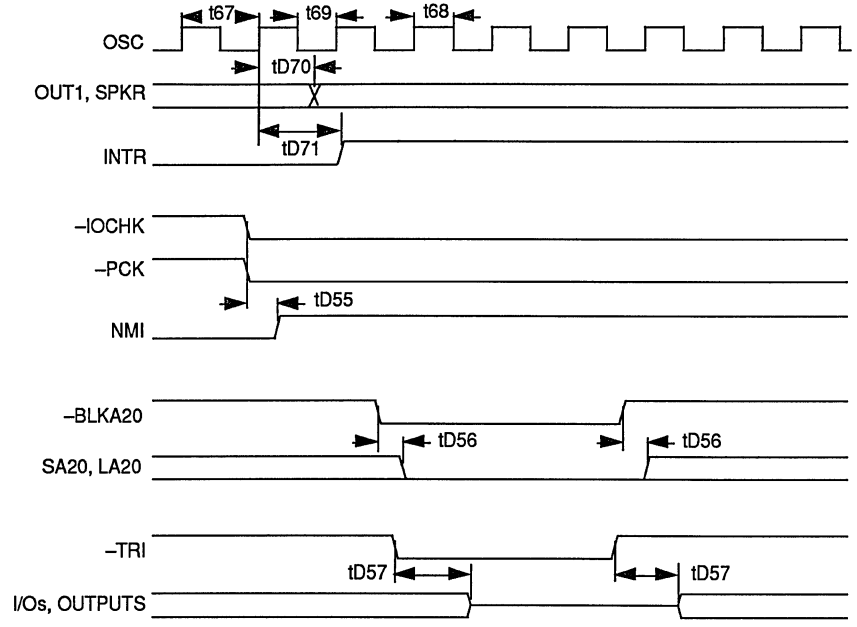
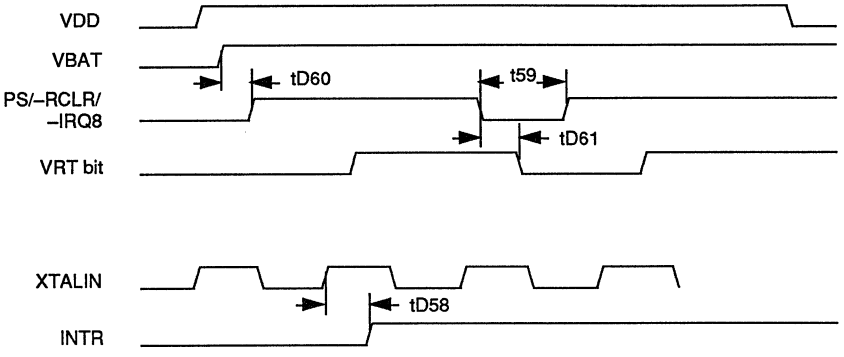


FIGURE 35. RTC INTERFACE



Note: The VRT bit is set to a "1" by reading Register D. The VRT can only be cleared by pulling the PS pin low. (See RTC description, Register D ($0D)).

FIGURE 36. MASTER MODE ACCESS (INTERNAL REGISTERS)

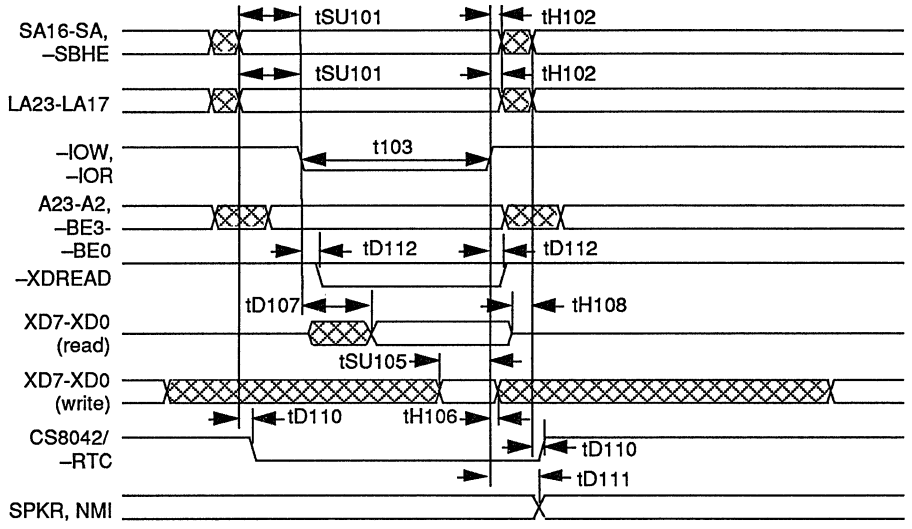


FIGURE 37. DMA MODE DATA STEERING

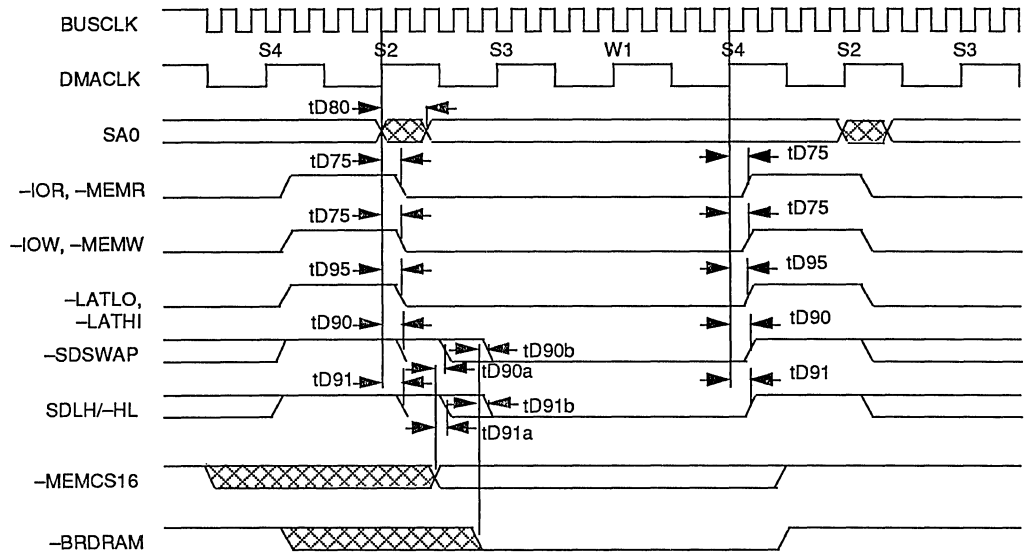
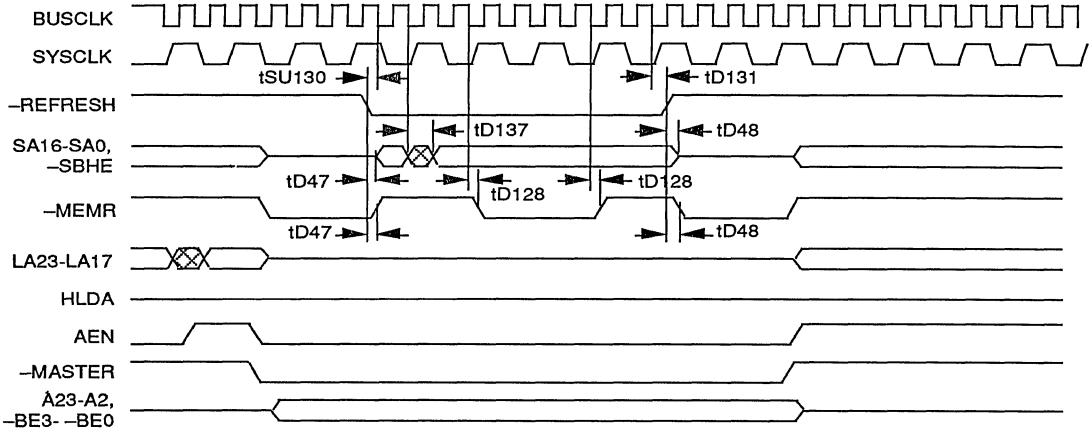


FIGURE 38. MASTER MODE REFRESH



Note: –SMEMR is three-stated for addresses above 1 meg. It should be pulled up externally with a 10K resistor.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature –10°C to +70°C

Storage Temperature –65°C to +150°C

Supply Voltage to Ground –0.5 V to VDD = 0.3 V

Applied Output Voltage –0.5 V to VDD = 0.3 V

Applied Input Voltage –0.5 V to 7.0 V

Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C TO +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min.	Max.	Unit	Conditions
VIL	Input Low Voltage	–0.5	0.8	V	TTL Level Inputs
VIH	Input High Voltage	2.0	VDD +0.5	V	TTL Level Inputs
VILC	Input Low Voltage	–0.5	0.8	V	CMOS Level Inputs
VIHC	Input High Voltage	VDD –0.8	VDD +0.5	V	CMOS Level Inputs
VOL1	Output Low Voltage		0.45	V	IOL = 4 mA, Note 1
VOH1	Output High Voltage	VDD –0.45		V	IOH = 1 mA, Note 1
VOL2	Output Low Voltage		0.45	V	IOL = 8 mA, Note 2
VOH2	Output High Voltage	VDD –0.45		V	IOH = –2 mA, Note 2
VOL3	Output Low Voltage		0.45	V	IOL = 12 mA, –HIDRIVE=1 IOL = 24 MA, –HIDRIVE=0, Note 3
VOH3	Output High Voltage	VDD –0.45		V	IOH = –6 mA, Note 3
VOL4	Output Low Voltage		0.45	V	IOL = 24 mA, Note 4
ILI	Input Leakage Current	–10	10	µA	Note 5
IIL	Input Leakage Current	–500	10	µA	Note 6
ILO	Output Leakage Current	–100	100	µA	
IDDSB	Static Power Supply Current		500	mA	
IDDOP	Dynamic Power Supply Current		4	mA/MHz	Based on BUSCLK frequency
IBAT	RTC Power Supply Current		5	µA	At VBAT=3 V, 32.768 kHz
VBAT	RTC Power Supply Voltage	2.4	5.25	V	
CI	Input or I/O Capacitance		10	pF	
CO	Output Capacitance		10	pF	

Notes appear on the following page.

NOTES FOR DC CHARACTERISTICS

Notes:
1. Pins: A25-A2, –BE3- –BE0, XD7-XD0, INTR, NMI, –CHS0, –CHS1, –CHREADY, DMAHRQ, OUT1, –SDSWAP, SDLH/–HL, –XDREAD, SPKR, –CS8042
2. Pins: –DACK7- –DACK0, T/C, –LATLO, –LATHI
3. Pins: SA19-SA0, LA23-LA17, –IOW, –IOR, –MEMW, –MEMR, –SBHE, RSTDRV, –SMEMW, –SMEMR, SYSCLK, AEN, BALE
4. Pins: –REFRESH
5. All inputs except those listed in Note 6.
6. Pins: IRQ15-IRQ9, IRQ7-IRQ3, IRQ1, DRQ7-DRQ5, DRQ3-DRQ0, –BE3, C286/–386, –EALE, –PCK, –ROM8, –HIDRIVE, –TRI, POWERGOOD, PS/–RCLR/–IRQ8

NOTES:

DATA BUFFER

DESCRIPTION

The VL82C332 Data Buffer is part of a custom, three chip set which allows extremely high performance and integration in 386™DX processor based, PC/AT®-compatible, personal computer designs. When used with VLSI Technology's VL82C330 System Controller and VL82C331 ISA Bus Controller, the set is called the VL82C386 chip set.

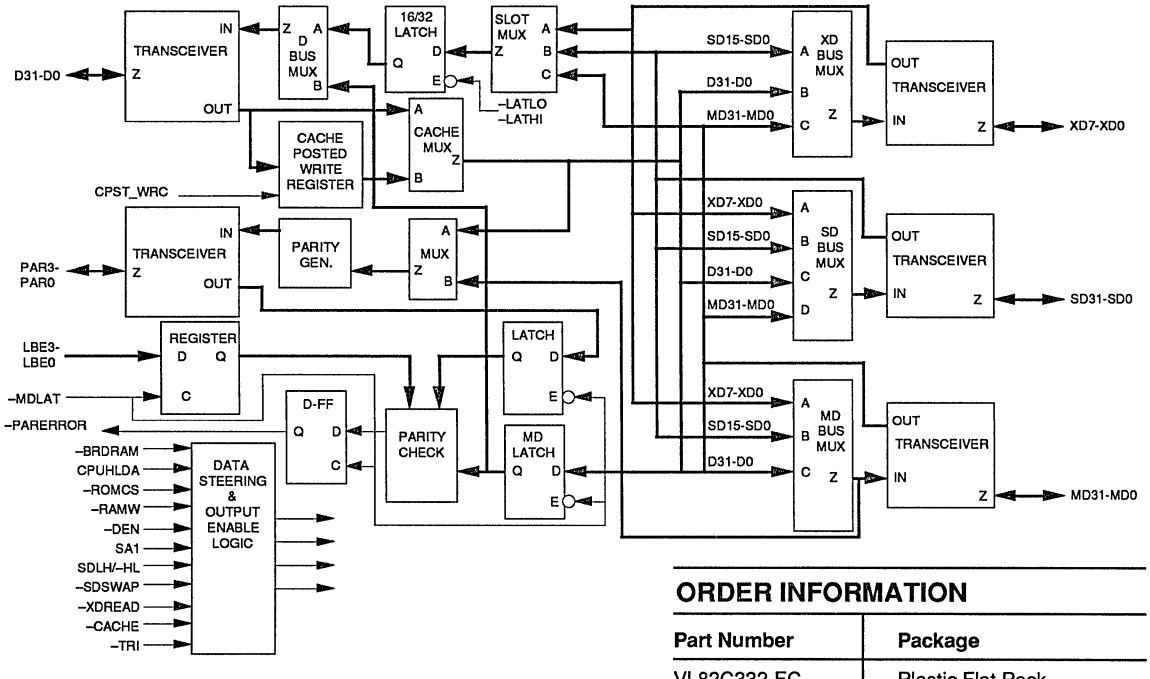
The VL82C332 performs all of the data buffering functions required for a 386DX-based PC/AT-type system. Under the control of the CPU, the data buffer chip routes data to and from the CPU bus, the MD bus, the XD bus, and the slots (SD bus). For an on-board DRAM read, the data is latched in the MD latch allowing the VL82C330 System Controller to be programmed for early CAS terminations. The parity is checked for MD bus read operations and any errors are reported during the next on-board memory read cycle. When reading from ROM, the XD bus or the SD bus, the data can be converted from 8-bits wide to 16-, 24- or 32-bits wide or from 16 bits to 32 bits at the 16/32 latch. The data is latched with –LATLO and –LATHI for synchronization with the CPU. The data conversion is accomplished without the use of the bus size 16 (–BS16) input to the 386DX allowing it to remain in pipelined mode.

CPU writes to any of the three buses are accomplished in several different ways. The VL82C332 supports posted writes from a cache controller or non-posted writes to the MD bus. Parity is generated for all data written to the MD bus. The VL82C332 provides the data conversion necessary for 32- or 16-bit writes to 16- or 8-bit devices on the XD or SD buses.

In non-cached systems, system board DRAM can be placed on the CPU's D bus. This provides extra timing margin when the MD bus delay through the VL82C332 is removed from the critical path.

Under the control of DMA or a bus master, the VL82C332 will allow 8- or 16-bit data to be routed to and from the XD and the MD buses. The chip also is capable of performing high to low and low to high byte swaps on the SD bus. For transfers between two peripherals on the slot bus, the outputs of the VL82C332 will be disabled. The chip also provides the feature of a single input, –TRI, to disable all of its outputs for board level testability.

BLOCK DIAGRAM



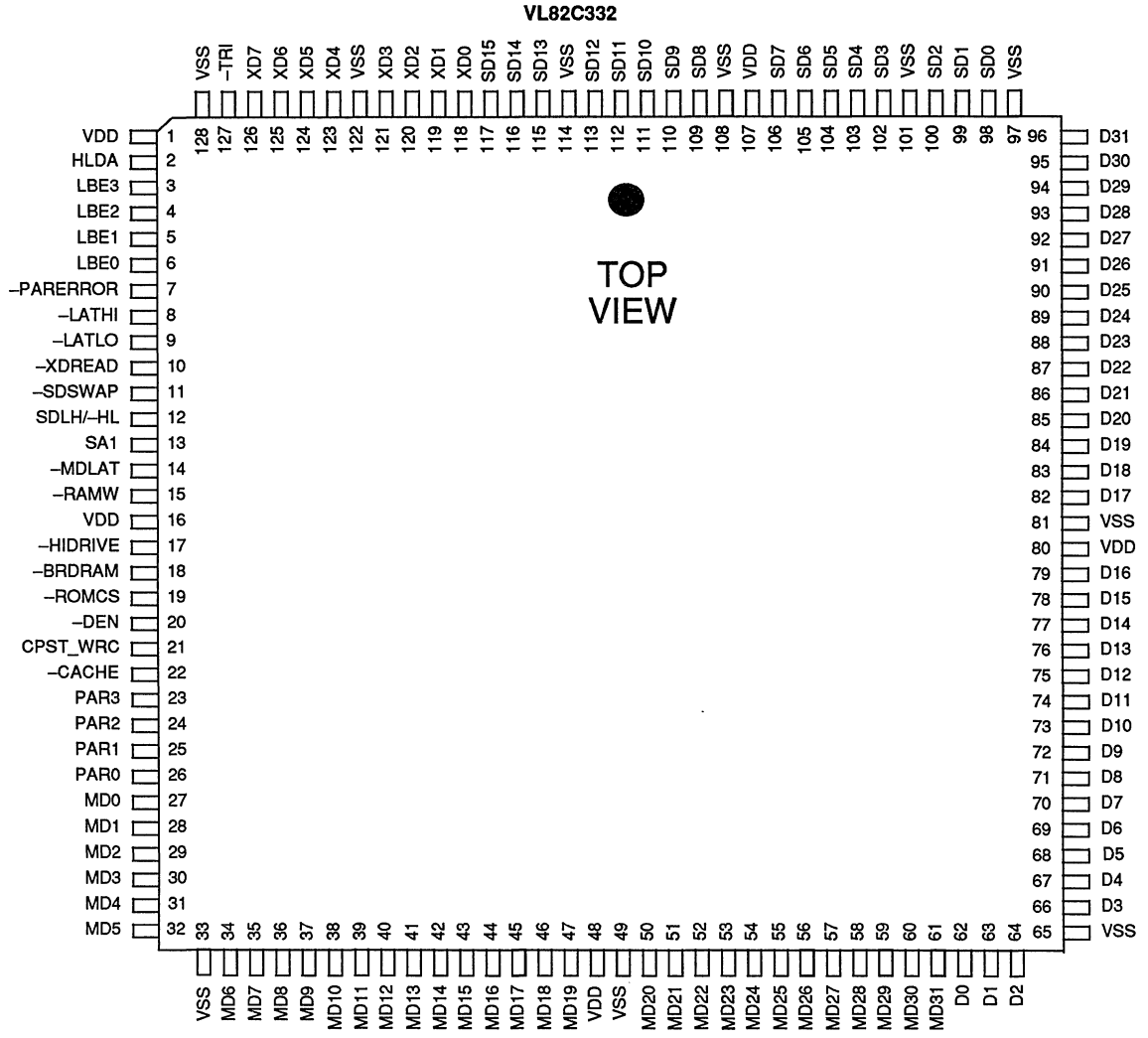
ORDER INFORMATION

Part Number	Package
VL82C332-FC	Plastic Flat Pack

Note: Operating temperature range is 0°C to +70°C.

PC/AT is a register trademark of IBM Corp.
386DX is a trademark of Intel Corp.

PIN DIAGRAM


VL82C332
TOP VIEW
1 VDD
2 HLDA
3 LBE3
4 LBE2
5 LBE1
6 LBE0
7 –PARERROR
8 –LATHI
9 –LATLO
10 –XDREAD
11 –SDSWAP
12 SDLH/–HL
13 SA1
14 –MDLAT
15 –RAMW
16 VDD
17 –HIDRIVE
18 –BRDRAM
19 –ROMCS
20 –DEN
21 CPST_WRC
22 –CACHE
23 PAR3
24 PAR2
25 PAR1
26 PAR0
27 MD0
28 MD1
29 MD2
30 MD3
31 MD4
32 MD5
33 VSS
34 MD6
35 MD7
36 MD8
37 MD9
38 MD10
39 MD11
40 MD12
41 MD13
42 MD14
43 MD15
44 MD16
45 MD17
46 MD18
47 MD19
48 VDD
49 VSS
50 MD20
51 MD21
52 MD22
53 MD23
54 MD24
55 MD25
56 MD26
57 MD27
58 MD28
59 MD29
60 MD30
61 MD31
62 D0
63 D1
64 D2
65 VSS
66 D3
67 D4
68 D5
69 D6
70 D7
71 D8
72 D9
73 D10
74 D11
75 D12
76 D13
77 D14
78 D15
79 D16
80 VDD
81 VSS
82 D17
83 D18
84 D19
85 D20
86 D21
87 D22
88 D23
89 D24
90 D25
91 D26
92 D27
93 D28
94 D29
95 D30
96 D31
97 VSS
98 SD0
99 SD1
100 SD2
101 VSS
102 SD3
103 SD4
104 SD5
105 SD6
106 SD7
107 VDD
108 VSS
109 SD8
110 SD9
111 SD10
112 SD11
113 SD12
114 VSS
115 SD13
116 SD14
117 SD15
118 XD0
119 XD1
120 XD2
121 XD3
122 VSS
123 XD4
124 XD5
125 XD6
126 XD7
127 –TRI
128 VSS

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE			
HLDA	2	I-TTL	CPU Hold Acknowledge, active high - This is the hold acknowledge pin directly from the CPU. It indicates the CPU has given up the bus for either a DMA master or a slot bus master. It is used in the steering logic to determine data routing.
D31-D0	96-82, 79-66, 64-62	IO-TTL	CPU Data Bus - This is the data bus directly connected to the CPU. It is also referred to as the local data bus. This bus is output enabled by the –DEN signal.
CACHE INTERFACE			
CPST_WRC	21	I-TTL	Posted Cache Write Clock - This clock signal is driven by the cache controller and is needed to latch the write data during a posted cache write cycle. The data is latched on the rising edge of this signal. The latch inside of the Data Buffer is bypassed if the –CACHE input is high. Also, when –CACHE is high, the state of CPST_WRC determines on which bus (D or MD) system DRAM is accessed. When high, DRAM is accessed on the D bus. When low, DRAM is accessed on the MD bus.
–CACHE	22	I-TPU	Cache Enable, active low - This signal is used to enable the cache posted write register. When there is not a cache in the system, data bypasses the register. When –CACHE is inactive (high) the state of the CPST_WRC pin determines whether the system DRAM is on the CPU's D bus or on the MD bus.
SYSTEM CONTROLLER INTERFACE			
–MDLAT	14	I-TTL	Memory Data Latch - This latching signal serves two purposes simultaneously and is only activated during on-board memory read and write cycles. As a memory data latch, this transparent low signal allows read data to flow through to the CPU's local bus. As a parity clock, it samples the byte enables, –RAMW, and parity bits to be used for parity checking. Any parity errors will be reported on the next on-board memory read cycle.
–RAMW	15	I-TTL	RAM Write, active low - This signal is supplied by the System Controller to indicate that a memory write cycle is occurring. It is used internally to direct the parity logic and to enable the MD bus outputs.
–ROMCS	19	I-TTL	ROM Chip Select - This signal tells the Data Buffer when the ROM is to be accessed so that it can latch the data and convert it from 16 or 8 bits to 32 bits. This signal is driven by the System Controller.
–BRDRAM	18	I-TTL	Board Memory Selected, active low - This signal is driven by the System Controller and indicates when on-board DRAM is being accessed.
–DEN	20	I-TTL	Data Enable, active low - This is a control signal generated by the System Controller. It is used as an output enable for the D bus.
LBE3-LBE0	3-6	I-TTL	Latch Byte Enables 3 through 0 - These signals are driven by the System Controller. They are used internally to enable the appropriate bytes for parity checking.
–PARERROR	7	O	Parity Error, active low - This signal is the result of a parity check on the appropriate bytes being read from memory. It is generated on the falling edge of –MDLAT.
BUS CONTROLLER INTERFACE			
SA1	13	I-TTL	System Address Bus bit 1 - This input will be driven by the Bus Controller or by the controlling DMA or bus master. This signal is used for 16- to 32-bit conversion. When low, this signal indicates the low word is to be used.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
SDLH/–HL	12	I-TTL	System Data Bus Low to High/High to Low Swap - This signal is driven by the Bus Controller. It is used to establish the direction of byte swaps.
–SDSWAP	11	I-TTL	System Data Bus Byte Swap Enable, active low - This signal is driven by the Bus Controller. It is the qualifying signal needed for SDLH/–HL.
–XDREAD	10	I-TTL	Peripheral Data Bus (XD Bus) Read, active low - This signal is driven by the Bus Controller and it determines the direction of the XD bus data flow. When this signal is high, the XD Bus is output enabled.
–LATHI	8	I-TTL	High Byte Latch - This signal is needed to latch the high byte to the local data bus until the CPU is ready to sample the bus. When SA1 is low, the high byte is latched into both the one byte and the three byte of the 16/32 latch. When SA1 is high, the high byte is only latched into the three byte. This signal is driven by the Bus Controller.
–LATLO	9	I-TTL	Low Byte Latch - This signal is needed to latch the low byte to the local data bus until the CPU is ready to sample the bus. When SA1 is low, the low byte is latched into both the zero byte and the two byte of the 16/32 latch. When SA1 is high, the high byte is only latched into the two byte. This signal is driven by the Bus Controller.
BUFFER INTERFACE			
MD31-MD0	61-50, 47-34, 32-27	IO-TTL	Memory Data Bus - This bus connects to the on-board DRAM and BIOS ROM. It is used to transfer data to/from memory during memory write/read bus cycles.
SD15-SD0	117-115, 103-109, 106-102, 100-98	IO-TTL	System Data Bus - This bus connects directly to the slots. It is used to transfer data to/from local and system devices.
XD7-XD0	126-123, 121-118	IO-TTL	Peripheral Data Bus - This bus is connected to the Bus Controller and the System Controller. These I/O's are used to read and write to on-board 8-bit peripherals.
PAR3-PAR0	23-26	IO-TTL	Parity Bits 3 through 0 - These bits are generated by the parity generation circuitry located on the Data Buffer chip. They are written to memory along with their corresponding bytes during memory write operations. During memory read operations, these bits become inputs and are used along with their respective data bytes to determine if a parity error has occurred. The check of each byte is enabled only when their respective LBE3-LBE0 bits are active.
–HIDRIVE	17	I-TPU	High Drive Enable - This pin is a wire option. When this pin is low, the SD bus will sink 24 mA of current. When this pin is high, the SD bus will sink 12 mA.
TEST MODE PIN			
–TRI	127	I-TPU	Three-state - This pin is used to drive all outputs to a high impedance state. When –TRI is low, all outputs and bidirectional pins are three-stated.
POWER BUS CONNECTION			
VDD	1, 16. 48, 80, 107	PWR	Power connection, nominally +5 volts. These pins should each have 0.1 µF bypass capacitors.
VSS	33, 49, 65, 81, 97, 101, 108, 114, 122, 126	GND	Ground connection, 0 volts.

SIGNAL TYPE LEGEND

Signal Code	Signal Type
I-TTL	TTL level input
I-TPU	Input with 30k ohm pull-up resistor
IO-TTL	TTL level input/ouput
O	CMOS and TTL level compatible output
GND	Ground
PWR	Power

FUNCTIONAL DESCRIPTION

BUS OPERATIONS

The VL82C332 Data Buffer separates the data bus into four distinct buses: D bus, MD bus, SD bus and the XD bus. The D bus is the CPU's data bus. The MD bus is the memory data bus which connects to the on-board DRAM and the BIOS ROM. The SD bus is the 16-bit slot bus and the XD bus is an 8-bit bus for on-board peripherals such as the VL82C330 System Controller and the VL82C331 Bus Controller. These buses can be controlled by either the CPU, a DMA controller or a bus master. Tables 1 and 2 show all possible bus steering modes provided by the VL82C332.

CACHE CONTROLLER INTERFACE

The cache controller interface is made up of a 32-bit register and a 64 to 32 MUX as shown in the block diagram. When a cache controller is not implemented, the –CACHE input pin should be tied high. This will set the MUX such that the cache posted write register is bypassed. When a cache is implemented, –CACHE should be tied low and the CPST_WRC input is used to post the write data into the register. The register latches data on the rising edge of the CPST_WRC input.

MD, D Bus System DRAM Selection

When the –CACHE input pin is tied low, system DRAM must be on the MD bus. However, when –CACHE is tied high, system DRAM may be placed on the MD bus or the CPU's D bus. The selection is made by the state of CPST_WRC. When tied low, DRAM is on the MD bus. When CPST_WRC is tied high, system DRAM is on the D bus. Since system board bus selection is hardwired on the system board, these pins can not be dynamically controlled in non-cache systems. They must be permanently tied to the proper level.

PARITY GENERATION AND DETECTION CIRCUIT

The parity check portion of the chip checks the parity of all data read from the on-board DRAM. During a DRAM read cycle, –MDLAT goes low making the MD latch transparent and latching out the parity check result, for the previous on-board memory read cycle. When –MDLAT returns high, data is latched into the MD latch. The parity check uses the Latched Byte Enable (LBE) signals from the System Controller to qualify each byte of the 32-bit word.

The parity generator provides parity generation for both CPU and DMA/master writes to on-board DRAM. A 64 to 32 MUX is used to select whether the input to the parity generator is from the CPU or from a DMA/master transfer. The result is output as one bit per data byte on the PAR3-PAR0 pins.

TABLE 1. BUS STATES WHEN PIN 21 = GROUND

Bus states for DRAM on the MD bus, ROM on the MD bus. Cache posted writes are supported.

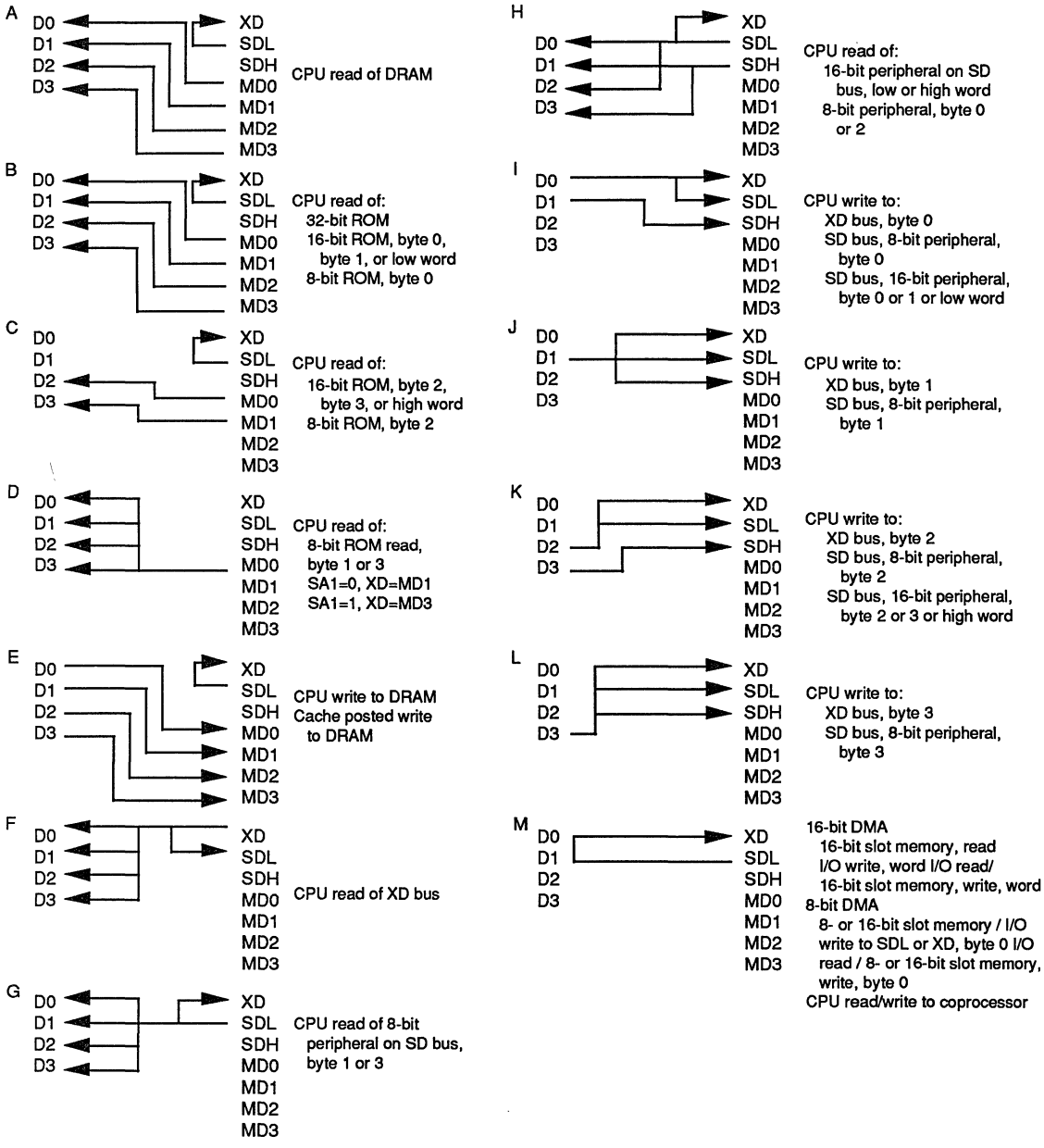
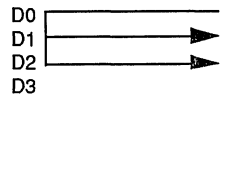


TABLE 1. BUS STATES WHEN PIN 21 = GROUND (Cont.)

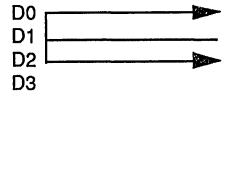
Bus states for DRAM on the MD bus, ROM on the MD bus. Cache posted writes are supported.

N



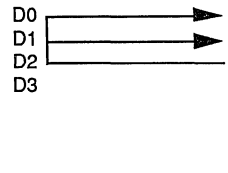
8-bit DMA
I/O read / 8- or 16-bit slot memory write, byte 0
I/O read / 16-bit slot memory write, byte 1

O



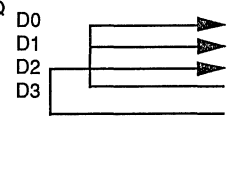
8-bit DMA
I/O read / 16-bit slot memory write, byte 1

P



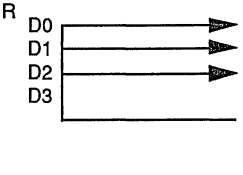
8-bit DMA
16-bit slot memory read / I/O write to SDL or XD, byte 1

Q



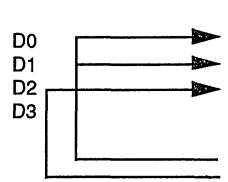
16-bit DMA
On-board memory read / I/O write, low word
8-bit DMA
On-board memory read / I/O write to SDL or XD, byte 0

R



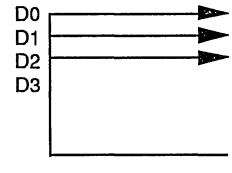
8-bit DMA
On-board memory read / I/O write to SDL or XD, byte 1

S



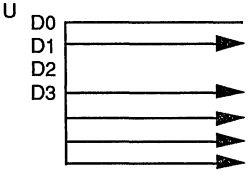
16-bit DMA
On-board memory read / I/O write, high word
8-bit DMA
On-board memory read / I/O write to SDL or XD, byte 2

T



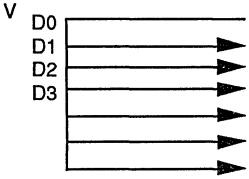
8-bit DMA
On-board memory read / I/O write to SDL or XD, byte 3

U



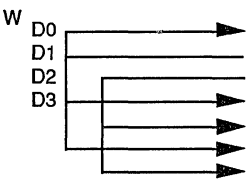
8-bit DMA
XD bus I/O read / on-board memory write, byte 0 or 2

V



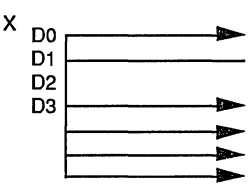
8-bit DMA
XD bus I/O read / on-board memory write, byte 1 or 3

W



16-bit DMA
SD bus I/O read / on-board memory write, low or high word
8-bit DMA
SD bus I/O read / on-board memory write, byte 0 or 2

X

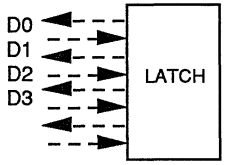


8-bit DMA
SD bus I/O read / on-board memory write, byte 1 or 3

TABLE 2. BUS STATES WHEN PIN 21 = VDD

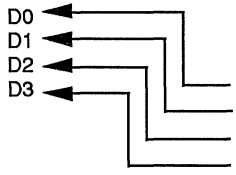
Bus states for DRAM on the D bus, ROM on the MD bus. Cache posted writes are not supported.

A



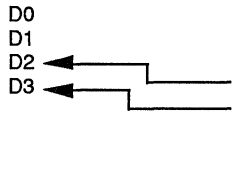
CPU read of DRAM.
D bus output enabled only after CAS goes inactive.

B



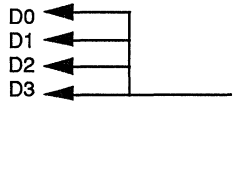
CPU read of:
- 32-bit ROM
- 16-bit ROM, byte 0, byte 1, or low word
- 8-bit ROM, byte 0

C



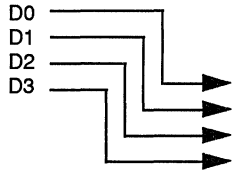
CPU read of:
- 16-bit ROM, byte 2, byte 3, or high word
- 8-bit ROM, byte 2

D



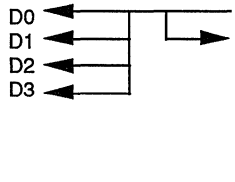
CPU read of:
- 8-bit ROM read, byte 1 or 3

E



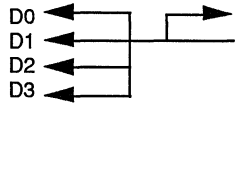
CPU write to DRAM
Cache posted write to DRAM

F U



CPU read of XD bus
8-bit DMA
- XD bus I/O read / on-board memory write, byte 0 or 2

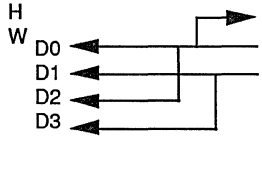
G X



CPU read of :
- 8-bit peripheral on SD bus, byte 1 or 3

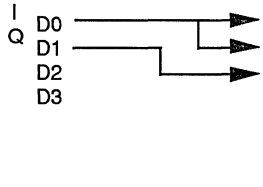
8-bit DMA
- SD bus I/O read / on-board memory write, byte1 or 3

H W



CPU read of:
- 16-bit peripheral on SD bus, low or high word
- 8-bit peripheral, byte 0 or 2
- 16-bit DMA, SD bus I/O read / on-board memory write, low or high word
- 8-bit DMA, SD bus I/O read / on-board memory write, byte 0 or 2

I Q

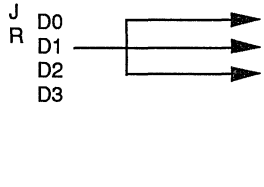


CPU write to:
- XD bus, byte 0
- SD bus, 8-bit peripheral, byte 0
- SD bus, 16-bit peripheral, byte 0 or 1 or low word

16-bit DMA
- On-board memory read / I/O write, low word

8-bit DMA
- On-board memory read / I/O write to SDL or XD, byte 0

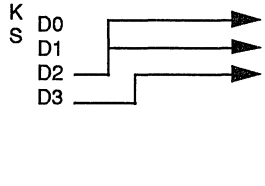
J R



CPU write to:
- XD bus, byte 1
- SD bus, 8-bit peripheral, byte 1

8-bit DMA
- On-board memory read / I/O write to SDL or XD, byte 1

K S

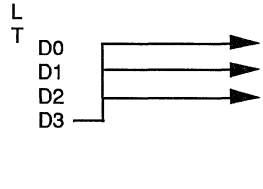


CPU write to:
- XD bus, byte 2
- SD bus, 8-bit peripheral, byte 2
- SD bus, 16-bit peripheral, byte 2 or 3 or high word

16-bit DMA
- On-board memory read / I/O write, high word

8-bit DMA
- On-board memory read / I/O write to SDL or XD, byte 2

L T



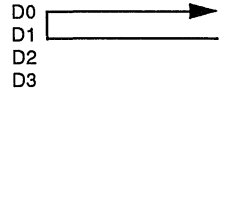
CPU write to:
- XD bus, byte 3
- SD bus, 8-bit peripheral, byte 3

8-bit DMA
- On-board memory read / I/O write to SDL or XD, byte 3

TABLE 2. BUS STATES WHEN PIN 21 = VDD (Cont.)

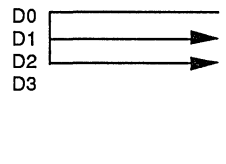
Bus states for DRAM on the D bus, ROM on the MD bus. Cache posted writes are not supported.

M



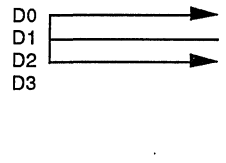
16-bit DMA
16-bit slot memory, read
I/O write, word I/O read/
16-bit slot memory, write, word
8-bit DMA
8- or 16-bit slot memory / I/O write to SDL or XD, byte 0 I/O read / 8- or 16-bit slot memory, write, byte 0
CPU read/write to coprocessor

N



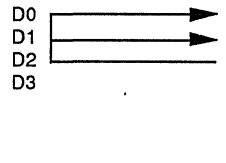
8-bit DMA
I/O read / 8- or 16-bit slot memory write, byte 0
I/O read / 16-bit slot memory write, byte 1

O



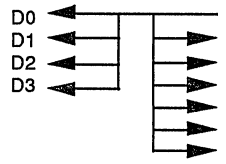
8-bit DMA
I/O read / 16-bit slot memory write, byte 1

P



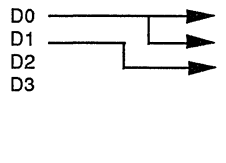
8-bit DMA
16-bit slot memory read / I/O write to SDL or XD, byte 1

V



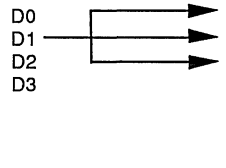
8-bit DMA
XD bus I/O read / on-board memory write, byte 1 or 3

Q



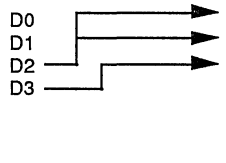
16-bit DMA
On-board memory read / I/O write, low word
8-bit DMA
On-board memory read / I/O write to SDL or XD, byte 0

R



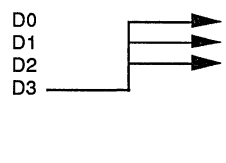
8-bit DMA
On-board memory read / I/O write to SDL or XD, byte 1

S



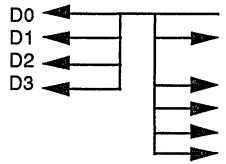
16-bit DMA
On-board memory read / I/O write, high word
8-bit DMA
On-board memory read / I/O write to SDL or XD, byte 2

T



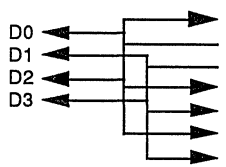
8-bit DMA
On-board memory read / I/O write to SDL or XD, byte 3

U



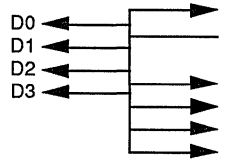
8-bit DMA
XD bus I/O read / on-board memory write, byte 0 or 2

W



16-bit DMA
SD bus I/O read / on-board memory write, low or high word
8-bit DMA
SD bus I/O read / on-board memory write, byte 0 or 2

X



8-bit DMA
SD bus I/O read / on-board memory write, byte 1 or 3

4

IN-CIRCUIT TESTING

ICT mode is not enabled in the current VL82C332 production parts. Since the VL82C332 is basically a matrix of multiplexers and I/O drivers, it is still possible to perform In-Circuit Test by application of an appropriate set of test vectors. This method is described below.

Future versions of the VL82C332 may have a true ICT mode. If so, the method described below may still be used as an option.

The values on the bidirectional buses are indicated as outputs by **boldface** type. They are inputs, otherwise. This distinction is used to tell whether to drive the indicated value on the bus or read it from the bus. A value of "u" indicates an output that is still "unknown".

BLOCK 1 -

Uses states A, C and D, and tests the following:
MD BUS (HI, LO), –ROMCS (HI, LO); D BUS (HI, LO), –BRDRAM (HI, LO); LBE BUS (HI, LO) SDLH/–HL (HI, LO); –PARERROR (HI, LO), –RAMW (HI); –MDLAT (HI, LO), –DEN (LO)

V E C T O R #	M D : : : : : : : :	D : : : : : : : :	S D H : : : : : :	S D L : : : : : :	X D : : : : : : : :	P A R : : : : : :	L B E : : : : : :	---C THCP RIAS IDCT :RH_ :IEW :V:R :E:C ::::	---- PMLL ADAA RLTT EALH RTOI R::: O::: R:::	H--- LDRB DEAR ANMD ::WR :::A ::M :::: ::::	-SS- RADS O1LD M:HS C:/W S:-A ::HP ::L: ::::	- X D R E A D : :
STATE A: VERIFY THE PARITY ERROR AND LBE SIGNALS WORK.												
1	13579BDF	**uuuuuuuu**	00	00	**00**	0	8	1010	u111	0010	1011	1
2	13579BDF	**13579BDF**	00	00	**00**	8	8	1010	u011	0010	1011	1
STATE A: LATCH IN PARITY ERROR ON BYTE 3.												
3	13579BDF	**13579BDF**	00	00	**00**	8	4	1010	u111	0010	1011	1
4	13579BDF	**13579BDF**	00	00	**00**	4	4	1010	0011	0010	1011	1
STATE A: LATCH IN PARITY ERROR ON BYTE 2.												
5	13579BDF	**13579BDF**	00	00	**00**	4	2	1010	0111	0010	1011	1
6	13579BDF	**13579BDF**	00	00	**00**	2	2	1010	0011	0010	1011	1
STATE A: LATCH IN PARITY ERROR ON BYTE 1.												
7	13579BDF	**13579BDF**	00	00	**00**	2	1	1010	0111	0010	1011	1
8	13579BDF	**13579BDF**	00	00	**00**	1	1	1010	0011	0010	1011	1
STATE A: LATCH IN PARITY ERROR ON BYTE 0.												
9	13579BDF	**13579BDF**	00	00	**00**	1	0	1010	0111	0010	1011	1
10	13579BDF	**13579BDF**	00	00	**00**	0	0	1010	0011	0010	1011	1
STATE A: LATCH IN GOOD PARITY ON ALL BYTES.												
11	13579BDF	**13579BDF**	00	00	**00**	0	F	1010	0111	0010	1011	1
12	13579BDF	**13579BDF**	00	00	**00**	0	F	1010	1011	0010	1011	1
13	13579BDF	**13579BDF**	00	00	**00**	0	F	1010	1111	0010	1011	1
STATE A: CHANGE MD BUS AND SEE THAT D BUS DOES NOT CHANGE.												
14	FDB97531	**13579BDF**	00	00	**00**	0	F	1010	1111	0010	1011	1
STATE D: –ROMCS AND SDLH/–HL BYTE OF MD BUS GO TO ALL BYTES OF D BUS.												
15	FDB97531	**31313131**	00	00	**75**	0	F	1010	1100	0011	0000	1
STATE C: RAISE SDLH/–HL, BYTES 1, 0 OF MD BUS GO TO BYTES 3, 2 OF D BUS.												
16	FDB97531	**75313131**	00	00	**00**	0	F	1010	1100	0011	0010	1
17	FDB97531	**75313131**	00	00	**00**	0	F	1010	1111	0011	0010	1

BLOCK 2 -

Uses states F, G and H, and tests the following:

SDH BUS (HI, LO) SDL BUS (HI, LO) XD BUS (HI, LO) –LATLO (HI, LO) –LATHI (HI, LO)
SA1 (HI, LO) –SDSWAP (HI, LO) –XDREAD(HI, LO) HLDA (LO)

	V	M	D	S	S	X	P	L	---C	----	H---	-SS-	-
	E	D	:	D	D	D	A	B	THCP	PMLL	LDRB	RADS	X
	C	:	:	H	L	:	R	E	RIAS	ADAA	DEAR	O1LD	D
	T	:	:	:	:	:	:	:	IDCT	RLTT	ANMD	M:HS	R
	O	:	:	:	:	:	:	:	:RH_	EALH	::WR	C:/W	E
	R	:	:	:	:	:	:	:	:IEW	RTOI	:::A	S:-A	A
		:	:	:	:	:	:	:	:V:R	R:::	:::M	::HP	D
	#	:	:	:	:	:	:	:	:E:C	O:::	::::	::L:	:
		┌──:──┐	┌──:──┐	┌:┐	┌:┐	┌:┐	┌:┐	┌:┐	::::	R:::	::::	::::	:
18		FFFFFFFF	**AA55AA55**	AA	55	**55**	0	F	1010	1100	0011	1011	1
19		FFFFFFFF	**55AA55AA**	55	AA	**AA**	0	F	1010	1100	0011	1011	1

STATE H: FORCE –LATLO, –LATHI AND SA1 HIGH.

20		FFFFFFFF	**55AA55AA**	55	AA	**AA**	0	F	1010	1111	0011	1111	1

STATE H: CHANGE SD BUSES. D BUS SHOULD NOT CHANGE.

21		FFFFFFFF	**55AA55AA**	33	CC	**CC**	0	F	1010	1111	0011	1111	1

STATE H: FORCE LATLO AND LATHI LOW. TWO HIGH BYTES OF D BUS SHOULD CHANGE.

22		FFFFFFFF	**33CC55AA**	33	CC	**CC**	0	F	1010	1100	0011	1111	1

STATE H: FORCE SA1 LOW. TWO LOW BYTES OF D BUS SHOULD CHANGE.

23		FFFFFFFF	**33CC33CC**	33	CC	**CC**	0	F	1010	1100	0011	1011	1

STATE G: FORCE –SDSWAP LOW. D BUS SHOULD CARRY SDL ON ALL BYTES.

24		FFFFFFFF	**CCCCCCCC**	33	CC	**CC**	0	F	1010	1100	0011	1010	1

STATE F: FORCE –XDREAD LOW. D BUS SHOULD CARRY XD ON ALL BYTES.

25		FFFFFFFF	**55555555**	CC	55	**55**	F	F	1010	1100	0011	1011	0

4

BLOCK 3 -

Uses state E and tests the following:

	PAR BUS (HI, LO)		–CACHE (HI, LO)		CPST_WRC (HI, LO)			–RAMW (LO)		–DEN (HI)		
	V	M	D	S	S	X	P	L	---C	----	H---	-SS-	-
	E	D	:	D	D	D	A	B	THCP	PMLL	LDRB	RADS	X
	C	:	:	H	L	:	R	E	RIAS	ADAA	DEAR	O1LD	D
	T	:	:	:	:	:	:	:	IDCT	RLTT	ANMD	M:HS	R
	O	:	:	:	:	:	:	:	:RH_	EALH	::WR	C:/W	E
	R	:	:	:	:	:	:	:	:IEW	RTOI	:::A	S:-A	A
		:	:	:	:	:	:	:	:V:R	R:::	:::M	::HP	D
	#	:	:	:	:	:	:	:	:E:C	O:::	::::	::L:	:
		┌ : ┐	┌ : ┐	┌ : ┐	┌ : ┐	┌ : ┐	┌ : ┐	┌ : ┐	::::	R:::	::::	::::	:
STATE E: TESTS MD BUS AND PAR BUSES.													
26	**55555555**	55555555	00	00	**00**	F	F	1010	1111	0100	1011	1
27	**AAAAAAAA**	AAAAAAAA	00	00	**00**	F	F	1010	1111	0100	1011	1
28	**ABAAAAAA**	ABAAAAAA	00	00	**00**	7	F	1010	1111	0100	1011	1
29	**ABABAAAA**	ABABAAAA	00	00	**00**	3	F	1010	1111	0100	1011	1
STATE E: TEST CPST_WRC AND –CACHE PINS.													
30	**uuuuuuuu**	ABABABAA	00	00	**00**	u	F	1000	1111	0100	1011	1
STATE E: RAISE CPST_WRC TO CLOCK IN DATA ON D BUS.													
31	**ABABABAA**	ABABABAA	00	00	**00**	1	F	1001	1111	0100	1011	1
STATE E: FORCE CPST_WRC LOW, CHANGE D BUS, STATE OF D BUS SHOULD NOT APPEAR ON MD BUS.													
32	**ABABABAA**	ABABABAB	00	00	**00**	1	F	1000	1111	0100	1011	1
STATE E: RAISE CPST_WRC AGAIN TO SEE NEW DATA ON MD BUS.													
33	**ABABABAB**	ABABABAB	00	00	**00**	0	F	1001	1111	0100	1011	1
34	**AAAAAAAA**	AAAAAAAA	00	00	**00**	F	F	1011	1111	0100	1011	1

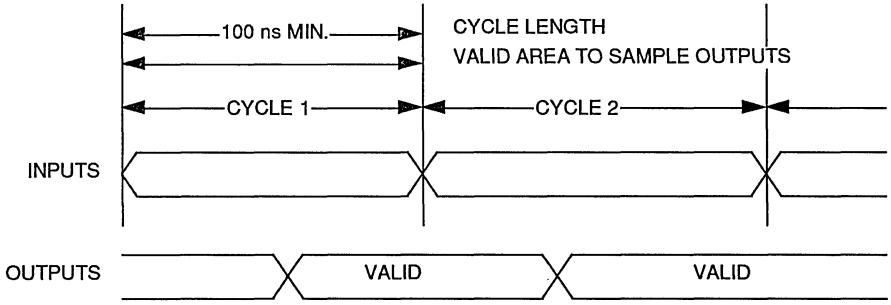
BLOCK 4 -

Uses state N and tests the following: HLDA (HI)

		V	M	D	S	S	X	P	L	---C	----	H---	-SS-	-
		E	D	:	D	D	D	A	B	THCP	PMLL	LDRB	RADS	X
		C	:	:	H	L	:	R	E	RIAS	ADAA	DEAR	O1LD	D
		T	:	:	:	:	:	:	:	IDCT	RLTT	ANMD	M:HS	R
		O	:	:	:	:	:	:	:	:RH_	EALH	::WR	C:/W	E
		R	:	:	:	:	:	:	:	:IEW	RTOI	:::A	S:-A	A
			:	:	:	:	:	:	:	:V:R	R:::	:::M	::HP	D
		#	:	:	:	:	:	:	:	:E:C	O:::	::::	::L:	:
			┌ : ┐	┌ : ┐	┌ : ┐	┌ : ┐	┌ : ┐	┌ : ┐	┌ : ┐	::::	R:::	::::	::::	:
STATE N: XD TO SDL BUS AND SDH BUS.														
35	FFFFFFFF	FFFFFFFF	**55**	**55**	55	F	F	1011	1111	1111	1001	0
36	FFFFFFFF	FFFFFFFF	**AA**	**AA**	AA	F	F	1011	1111	1111	1010	0

TEST PATTERN TIMING CONSTRAINTS

The patterns should be applied with a vector period of 100 ns. or more. with all inputs driven at the start of the cycle and all outputs sampled 60 ns or more after the beginning of the cycle, but at least 10 ns before the end of the cycle.



SPECIAL CASE SIGNALS

The only pins not tested with the test vectors described below are –TRI (low) and –HIDRIVE (high, low). The best way to test these is as follows.

–TRI (low): Force –XDREAD high and –TRI low. If the XD bus is high impedance then –TRI (low) works correctly.

–HIDRIVE (high, low): Set a current source in the range of 10 to 15 mA on one of the SD bus pins. Use a pattern that will drive a low onto the SD bus pin in question. Put a high value on the –HIDRIVE pin and test the VOL value on that SD bus pin. Then change the–HIDRIVE pin to a low. The VOL value on the SD bus pin should drop by at least 100.0 mV.

The first group of signals shown below are the buses; MD, D, SDH (SD high byte), SDL (SD low byte), XD, PAR and LBE. All these buses are shown in hexadecimal format. The next group of signals are all the individual inputs and the –PARERROR output. These signals are shown in binary format. The last group of signals, starting after –SDSWAP, are the Output Enable signals for the bidirectional buses. The two 32-bit buses have an Output Enable for each byte, but all four Output Enable (OE) signals for a given bus will transition together. The PAR bus uses the same Output Enable signals as the MD bus. All output enables are active low indicating that the VL82C332 is driving the bus anytime the Output Enable signal is low.

The values on the bidirectional buses indicate what is to be driven in if the corresponding OE signal is high, or what to sample on the outputs when the OE signal is low. A value of "u" indicates an output that is still "unknown".

AC CHARACTERISTICS: TA = 0°C to +70 °C, VDD = 5 V ±5%, VSS = 0V

Symbol	Parameter	Min	Max	Unit	Conditions
tD1	D31-D0 to MD31-MD0, PAR3-PAR0 Delay	3	20	ns	CL=50 pF
tD2	CPST_WRC to MD31-MD0, PAR3-PAR0 Delay	3	27	ns	CL=50 pF
tD3	–MDLAT Low to D31-D0 Delay	3	20	ns	CL=50 pF
tD4	–MDLAT Low to –PARERROR	3	20	ns	CL=50 pF
tD5	–LATLO, –LATHI Low to D31-D0 Delay	3	25	ns	CL=50 pF
tD6	D31-D0 to XD7-XD0 Delay	3	25	ns	CL=50 pF
tD7	D31-D0 to SD15-SD0 Delay	3	30	ns	CL=200 pF Note 1
tD8	XD7-XD0 to MD31-MD0, PAR3-PAR0 Delay	3	25	ns	CL=50 pF
tD9	XD7-XD0 to D31-D0 Delay	3	25	ns	CL=50 pF
tD10	XD7-XD0 to SD15-SD0 Delay	3	30	ns	CL=200 pF Note 1
tD11	SD15-SD0 to XD7-XD0 Delay	3	25	ns	CL=50 pF
tD12	SD15-SD0 to MD31-MD0, PAR3-PAR0 Delay	3	25	ns	CL=50 pF
tD13	SD15-SD0 to D31-D0 Delay	3	25	ns	CL=50 pF
tD14	SD15-SD8 to SD7-SD0 Delay	3	30	ns	CL=200 pF Note 1
tD15	SD7-SD0 to SD15-SD8 Delay	3	30	ns	CL=200 pF Note 1
tD16	MD31-MD0 to XD7-XD0 Delay	3	25	ns	CL=50 pF
tD17	MD31-MD0 to SD15-SD0 Delay	3	30	ns	CL=200 pF Note 1
tD18	MD31-MD0 to D31-D0 Delay	3	15	ns	CL=50 pF
tD19	MD15-MD0 to D31-D0 Delay	3	25	ns	CL=50 pF
tD20	CONTROL to SD15-SD0 Delay	3	35	ns	CL=200 pF Note 1
tD21	CONTROL to XD7-XD0 Delay	3	25	ns	CL=50 pF
tD22	CONTROL to MD31-MD0 Delay	3	20	ns	CL=50 pF
tD23	CONTROL to D31-D0 Delay	3	20	ns	CL=50 pF
tSU24	MD31-MD0 to –MDLAT Setup Time	3		ns	
tH25	MD31-MD0 from –MDLAT Hold Time	4		ns	
tSU26	D31-D0 to –MDLAT Setup Time	3		ns	
tH27	D31-D0 from –MDLAT Hold Time	4		ns	
tSU28	LBE3-LBE0, –RAMW to –MDLAT Setup TIme	–1		ns	
tH29	LBE3-LBE0, –RAMW from –MDLAT Hold TIme	8		ns	
tSU30	PAR3-PAR0 to –MDLAT Setup Time	3		ns	
tH31	PAR3-PAR0 from –MDLAT Hold Time	4		ns	
tSU32	MD15-MD0 to –LATLO, –LATHI Setup Time	10		ns	
tH33	MD15-MD0 from –LATLO, –LATHI Hold Time	2		ns	
tSU34	SD15-SD0 to –LATLO, –LATHI Setup Time	10	20	ns	

AC CHARACTERISTICS Cont.: TA = 0°C to +70 °C, VDD = 5 V

Symbol	Parameter	Min	Max	Unit	Conditions
tH35	SD15-SD0 from –LATLO, –LATHI Hold Time	2		ns	
tSU36	XD7-XD0 to –LATLO, –LATHI Setup Time	10		ns	
tH37	XD7-XD0 from –LATLO, –LATHI Hold Time	2		ns	
tSU38	D31-D0 to CPST_WRC Setup Time	5		ns	
tH39	D31-D0 from CPST_WRC Hold Time	5		ns	
t40	–MDLAT Pulse Width	10		ns	
t41	–LATLO, –LATHI Pulse Width	15		ns	
t42	CPST_WRC Pulse Width	15		ns	

Note 1: These specifications are with –HIDRIVE active.

FIGURE 1.

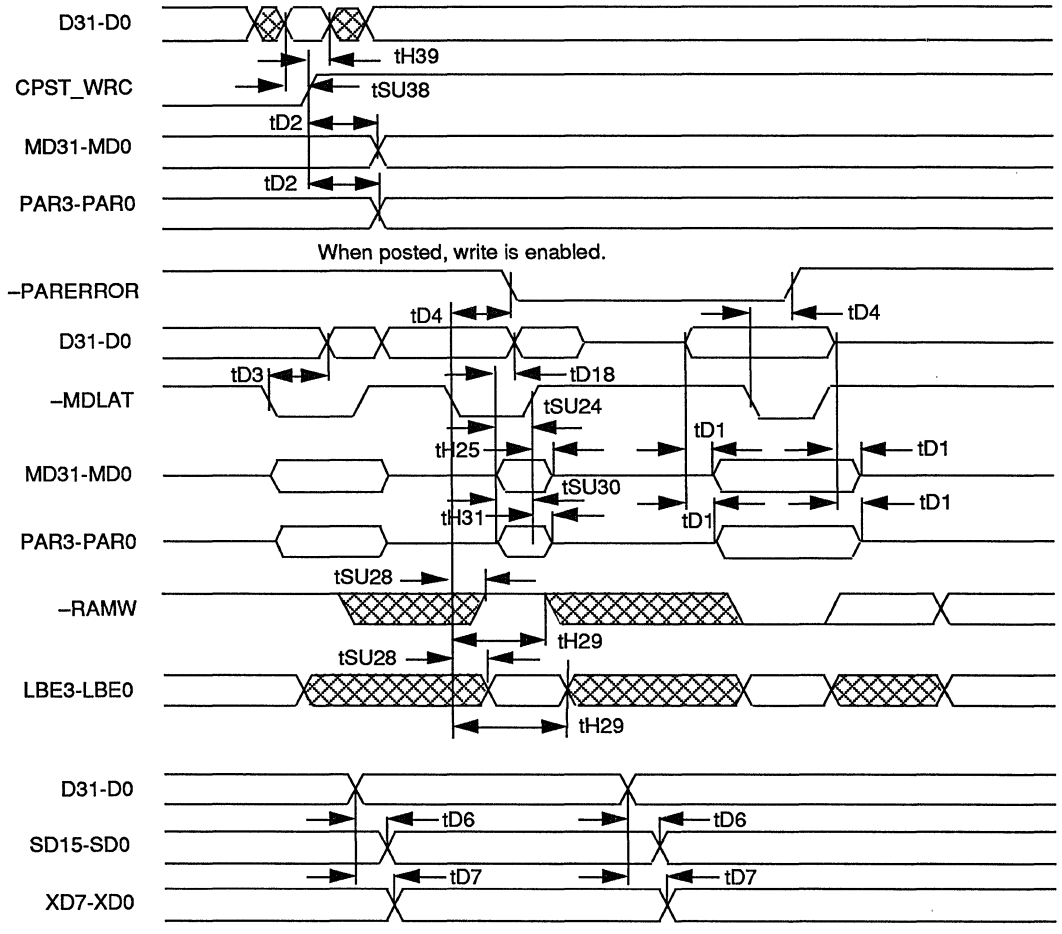

D31-D0
tH39
CPST_WRC
tSU38
tD2
MD31-MD0
tD2
PAR3-PAR0
When posted, write is enabled.
–PARERROR
tD4
tD4
D31-D0
tD3
tD18
–MDLAT
tSU24
tD1
tH25
tD1
MD31-MD0
tSU30
tD1
tH31
tD1
PAR3-PAR0
tSU28
–RAMW
tH29
tSU28
LBE3-LBE0
tH29
D31-D0
tD6
tD6
SD15-SD0
tD7
tD7
XD7-XD0

FIGURE 2.

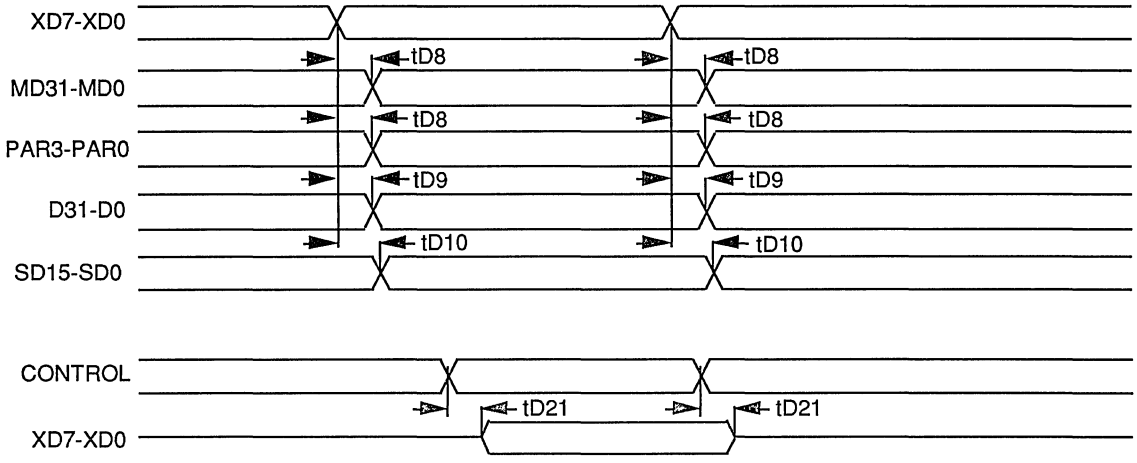


FIGURE 3.

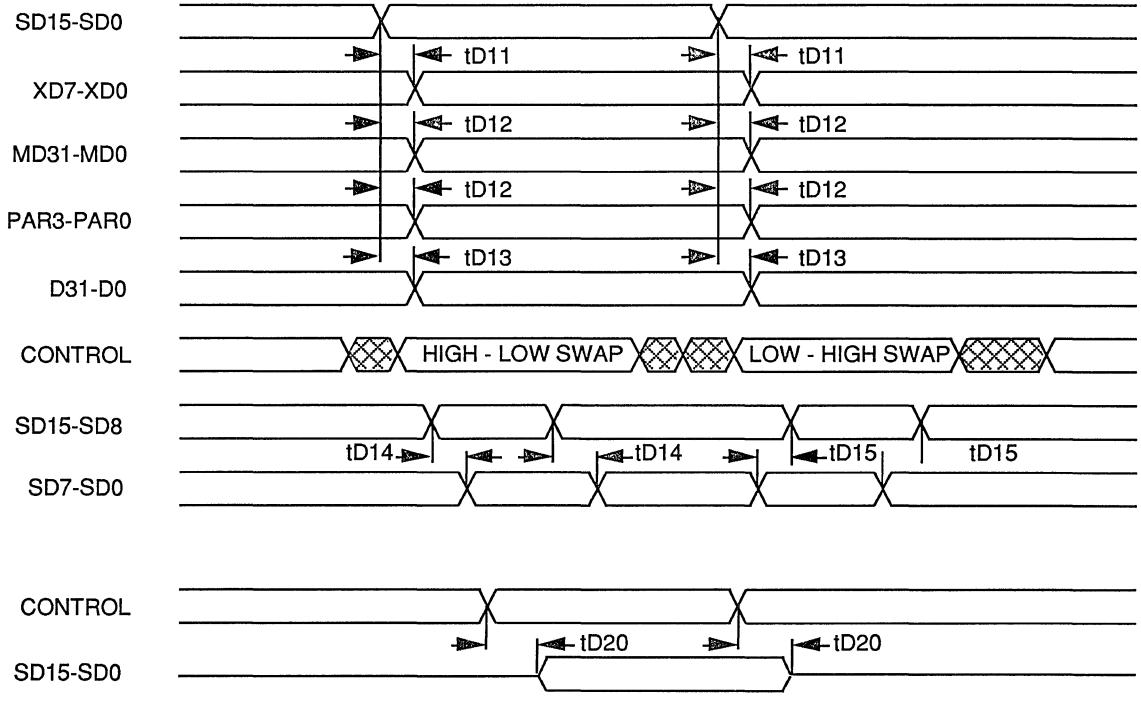
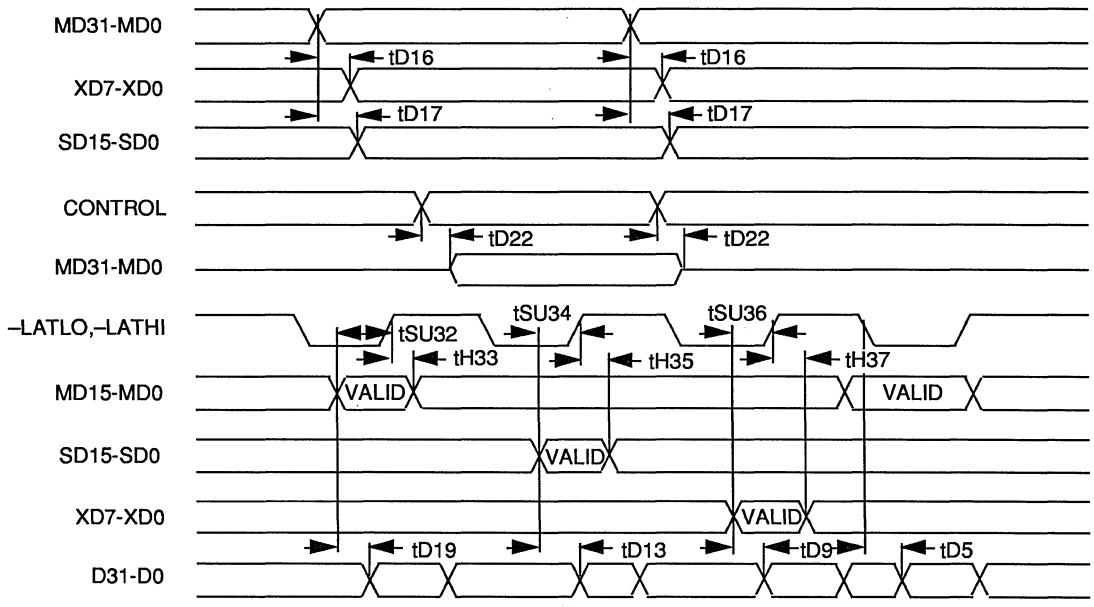


FIGURE 4.



Note: tD5 is shown with data being sourced from the MD bus. This could also be the SD or XD busses.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature –10°C to +70°C

Storage Temperature –65°C to +150°C

Supply Voltage to Ground –0.5 V to VDD = 0.3 V

Applied Output Voltage –0.5 V to VDD = 0.3 V

Applied Input Voltage –0.5 V to 7.0 V

Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C TO +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min.	Max.	Unit	Conditions
VIL	Input Low Voltage	–0.5	0.8	V	
VIH	Input High Voltage	2.0	VDD	V	
VOL	Output Low Voltage		0.4	V	
VOH	Output High Voltage	2.4		V	
IDD	Static Current		500	µA	
IDD	Dynamic Current		1.5	mA/MHz	Frequency is data dependant
IIL	Input Leakage		±10	µA	
IOZ	Three-state Leakage		±20	µA	

4

NOTES:

VLSI TECHNOLOGY, INC.

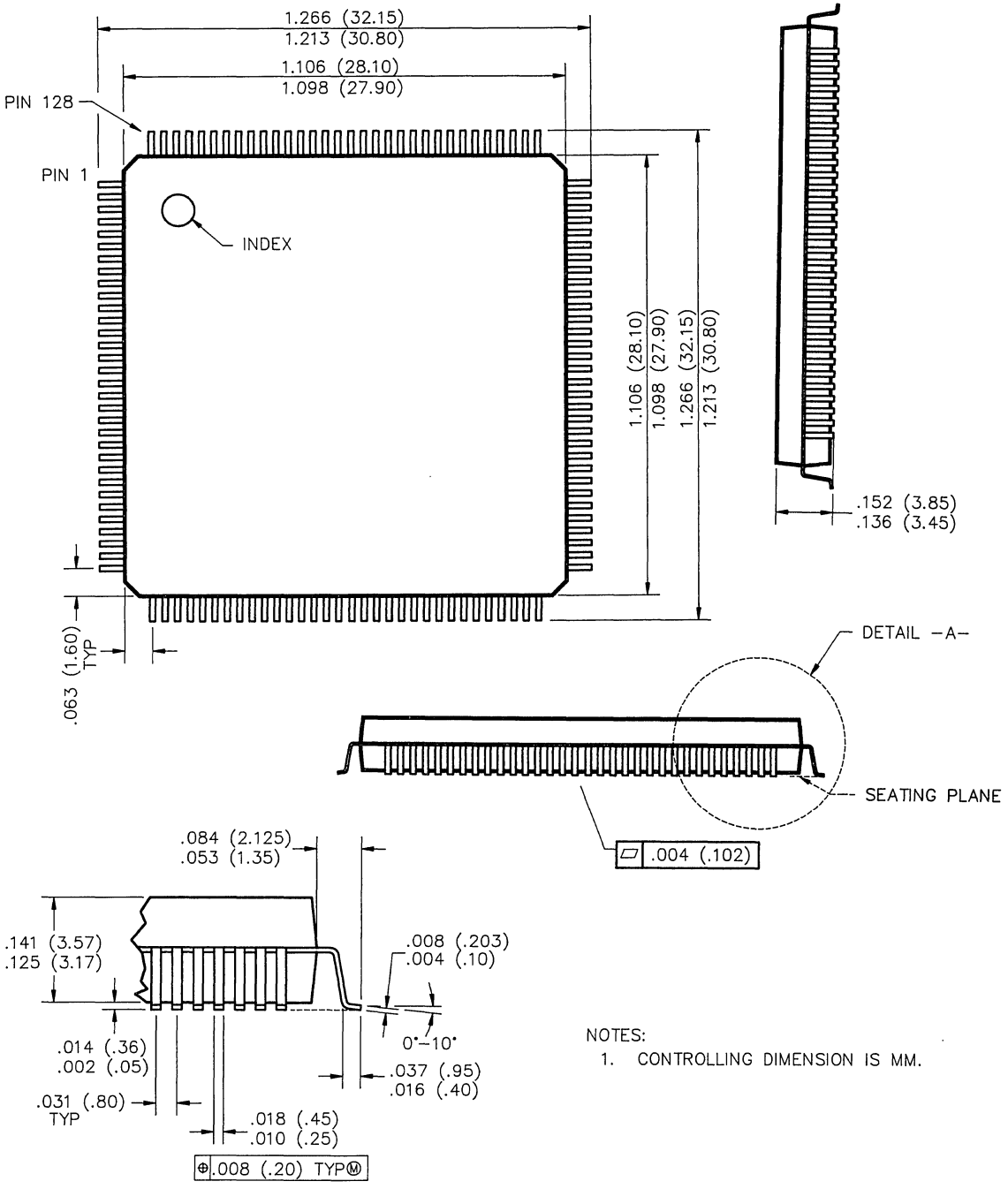
SECTION 5

PACKAGE OUTLINES

Logic Products Division


VLSI TECHNOLOGY, INC.

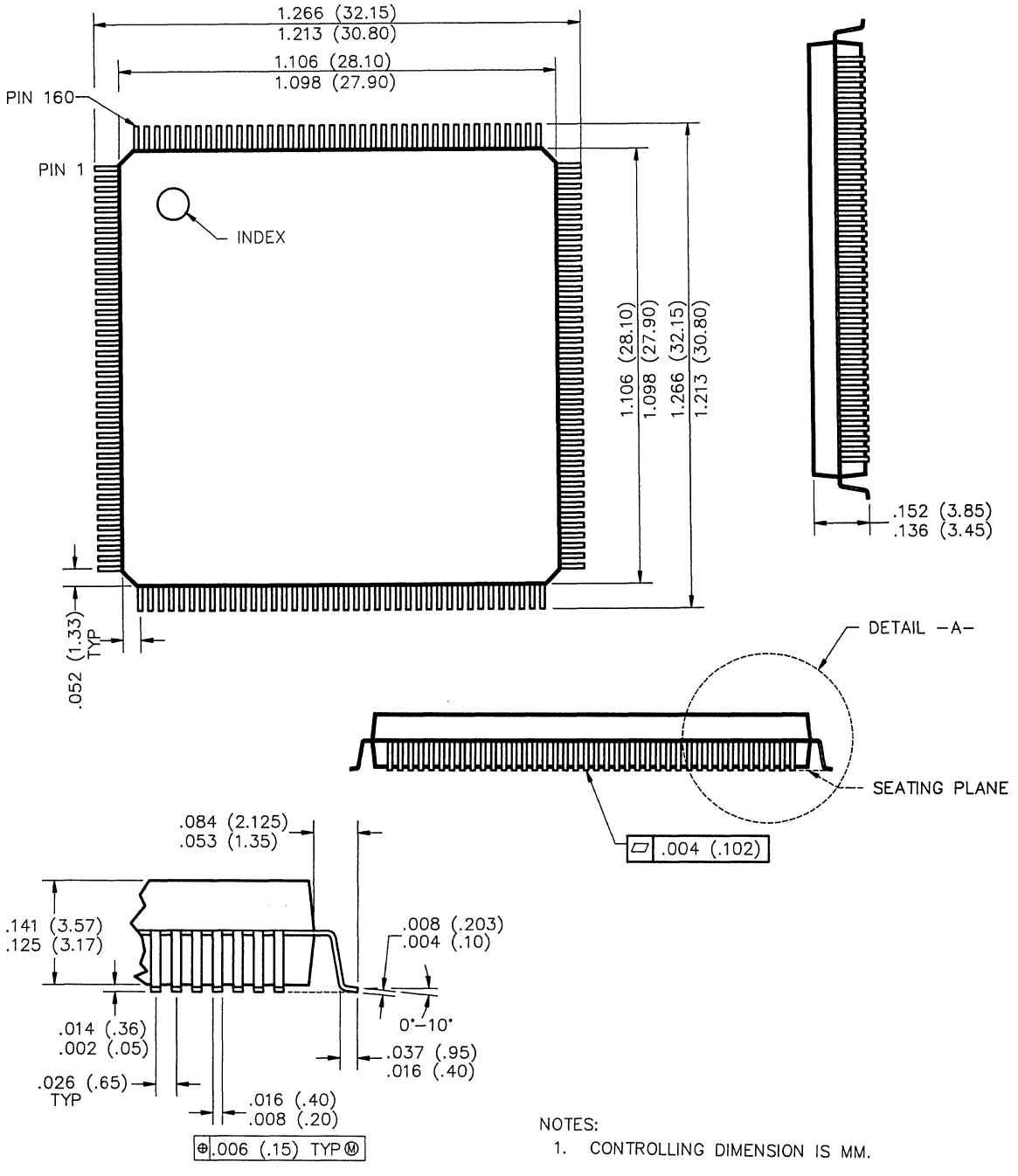
128-PIN PLASTIC FLATPACK



NOTES:

1. CONTROLLING DIMENSION IS MM.

160-PIN PLASTIC FLATPACK



NOTES:

1. CONTROLLING DIMENSION IS MM.

VLSI TECHNOLOGY, INC.

SECTION 6

BIOS


VLSI TECHNOLOGY, INC.

AMI 80286/80386SX/80386DX BIOS FOR VLSI TOPCAT CHIP SET

CPU:
Intel 80286, 80386SX, 80386DX
Auto-detect between 80386SX and 80386DX

Speed:
6 MHz to 33 MHz
BIOS is Speed independent

Coprocessor:
Intel 80287, 80387SX, 80387, and Weitek or compatible coprocessors

User Programs:

CMOS Setup Program:
Full screen edit
Full parameter display of each option
Allows user to set date and time
Allows user to set floppy drive type
(3.5" 720 KB and 1.44 MB/5.25" 360 KB and 1.2 MB)
Allows user to set fixed disk drive types (46 types)
Two user-definable fixed disk drive types
Full calendar display
Allow user to disable keyboard test, floppy test, and video test upon boot-up
Built into ROM

Extended CMOS: Setup Program (optional)
Easy Extended CMOS Setup allows the user to:
Enable Main BIOS Shadow RAM
Enable Video BIOS Shadow RAM
Select Main and Bus Clock sources
Select Main Memory Waitstates
Advanced Extended CMOS Setup allows the user to program the individual chip-set registers directly in order to achieve optimum performance from the motherboard. Each component is referred to by its chip number, and each programmable register is shown with its current value. Valid programming options are shown in a friendly pop-up window.
Both are available in ROM or on diskette

Advanced ROM: Diagnostics (optional)
Allows the user to perform extensive diagonostic tests on peripherals and to troubleshoot system errors
Test for floppy disk drive such as:
Floppy Format
Drive Speed Test
Radom R/W Test
Sequential R/W Test
Disk Change Line Test
Tests for fixed disk drives such as:
Performance Test
Seek Test
Read/Verify Test
Check Test Cylinder
Routines for fixed disk preparation routines such as:
Hard Disk format
Automatic Interleave detection
Media Analysis
Force Bad Track List
Tests for video subsystem
Test for serial and parallel ports
Tests for keyboard scan and ASCII codes
Built into ROM

POST Routines:

All IBM Standard POST Routines
Enhanced AMI POST Routines
Support for 80386's Internal Diagostics
Tests for CPU, 8259, 8253, Main Memory, Video, DMA Controller, Floppy disk drive, Fixed disk drive, Keyboard, Coprocessor, I/O Ports, etc.
AMI defined POST codes through port 80h
Easy to understand error messages appear on the screen if problems occur
Well defined error codes through speaker if there is no video system present

Main Memory:

Maximum:

64 MB on-board for 83086DX
16 MB on-board for 80386SX
16 MB on-board for 80386 (32 MB with SEEMS EMS LIM 4.0 driver)

Auto-Detect:

Automatic detection of DRAM types, number of banks and total memory size

DRAM type:

256 KB and 1 MB DRAMs

Cache Memory:

Support available for the following cache controllers:
Austek A38202, Intel 82385
BIOS can be customized for other controllers
Cache can be enabled/disabled through keyboard

Floppy Disk:

Support for 5.25" 360 KB and 1.2 MB/3.5" 720 KB and 1.44 MB disk drives
Support for two internal disk drives
Floppy POST test can be bypassed through CMOS Setup (described above)
Support for on-board floppy ports in "Combo Chip"

Fixed Disk:

Standard Drive Table of 46 drive types can be customized by OEMs and VARs using AMIGEN (described in Optional Software section below)
Support for MFM, RLL, ESDI, SCSI, and IDE fixed disk drives with up to 4096 cylinders
Two user-definable drive types in CMOS Setup
Support for on-board IDE interface in "Combo Chip"

Standard Video:

Support for MDA and CGA built into BIOS
Support for EGA, VGA, and JEGA available
Allows use of monochrome or color monitors
Video POST test can be bypassed through CMOS Setup (described above)
Optional BIOS modules can be linked into Main BIOS or can be used on a separate video adapter board

I/O Ports:

Support for four serial (COM) ports
Support for three parallel (LPT) ports
Auto-detect of all off-board serial and parallel ports
Support for on-board serial and parallel ports in "Combo Chip"

Keyboard Support:

Support for 83/84 key, 101/102 key keyboards and auto-sense keyboards
Keyboard POST test can be bypassed through CMOS Setup (see above)

Keyboard Controller:

Auto-detect between AT and PS/2 keyboard standards
Support for PS/2-style mouse with appropriate hardware
Support for on-board keyboard controller in "Combo Chip"
Controller speed ranges from 6 MHz to 12 MHz

Configurations:

Fileserver (no video or keyboard)
Workstation (no fixed or floppy disks)
Standard (video, keyboard, floppy disk exist)
All of the above can be configured through CMOS Setup described above

BIOS Format:

AMI BIOS is available in these formats:

EPROMs: 1-27512 ROMs (64 KB each)
2-27256 ROMs (32 KB each)
4-27128 ROMs (16 KB each)

Diskette: ROM files (binary format) on diskette

Source: Souce Code Modules on diskette

Optional Software:

AMICACHE: An excellent fixed disk caching program which increases data transfer rate.

AMIDISK: RAM Disk Utility. Converts RAM to Disk Space. Runs in base memory, Extended Memory, or Expanded Memory.

AMIDIAG: Award-Winning diagnostics utility based on AMI's Advanced ROM Diagonstics. Troubleshoots system components, RAM and ROM, and all peripherals.

AMI SEEMS: Software Emulated Expanded Memory System. Expanded Memory Manager which adheres to LIM 4.0 specifications.

AMIGEN: AMI BIOS modification utility used by OEMs and VARs to change sign-on message, clock and bus control methods, fixed-disk drive table, and many other features.

All company and product names are trademarks of the manufacturer respectively.

AMI
Single Source Technology™

American Megatrends, Inc., 1346 Oakbrook Drive Suite 120, Norcross, Georgia 30093
(404) 263-8181 Fax (404) 263-9381 TELEX 910-240-1527
In USA 1-800-U-BUY-AMI

AWARD MODULAR BIOS™ FOR THE VLSI TOPCAT CHIP SETS FOR 286, 386™SX, 386™DX, & 486™ PROCESSORS

Software Solutions for System Manufacturers

Award's Modular BIOS is setting the standard for Intel® microporcessor-based AT-compatible systems, with a modular architecture available for major chip platforms. The BIOS can be customized to support almost any special configuration, while providing full compatibility with the IBM AT® standard. The Award BIOS features a built-in Setup program, an enhanced Power On Self Test (POST), and the fastest character I/O available. Award's BIOS products offer the best in high performance and flexibility for all systems' requirements.

BIOS Features

47 Standard Drive Types to choose from
- Choose from a wide selection of standard drive types in Setup

User Definable Drive Tables
- In addition to the standard 47 drive types, you can define two drive types to fit the requirements of your system

Password Protection
- Protect against access to Setup or to the entire system

Extensive POST
- Test and initialize all system components

Built-In ROM Setup
- Access Setup from ROM during POST

MODBIN™ for custom changes to binary files.
- Customize the BIOS for specific needs

Chip Set Features

The VLSI TOPCAT chip sets are designed for the ISA (PC/AT bus) platform architecture for use with the Intel microprocessor family.

Multiple processor speeds
- From 12 MHz to 33 MHz for 386DX and 486
- From 12 MHz to 20 MHz for 286 and 386SX

Numeric Coprocessor
- Weitek™ 4167 for 486
- 387™DX and Weitek 3167 for 386DX
- 387SX for 386SX
- 287 for 286

Advanced Memory Configurations
- One to four banks of 32-bit DRAM for a total of 64 MB for 386DX and 486
- One to four banks of 16-bit DRAM for a total of 32 MB for 286 and 386SX
- Full LIM EMS 4.0 specification over entire memory map
- Automatic DRAM memory sizing
- Memory banks automatically remapped to allow logical re-ordering of DRAM
- Two-way and four-way page mode interleaving or direct access of on-board system memory
- Default DRAM timing parameters programmable through MODBIN

Shadow RAM
- Enable Shadow RAM in 16K increments

Extended Setup
- Available in ROM or on diskette

VLSI VL82C106 combo I/O chip
- Enable/disable of VL82C106 on-chip selects (e.g. serial port and parallel port)

Cache Support
- Selectable through Setup

Award Software, Inc.

Versatile Modular Configuration

The Award Modular BIOS is available in ready-to-install standard AT-style ROMs, in an Intel-format binary file on diskette – ready to download to a PROM burner – and also in source code modules. The BIOS configuration options make it easy for the system builder as well as the end user.

Commitment To Support

Award is committed to your success and offers everything you need to produce a compatible, trouble-free design. Award offers in-house design compatibility services, maintenance agreements, custom software development, telephone technical support, a 24-hour On-Line Support System, and a dedicated Sales and Technical Support Team. To see how you can make these advantages work for you, contact Award's corporate office or the sales office nearest you.

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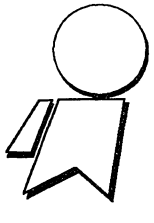

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PHOENIX 80386 ROM BIOS FOR VLSI® TOPCAT 386™ DX CHIP SET/INTEL® 82340DX

Phoenix ROM BIOS Benefits

- Superior Setup utility optimized for end-user ease-of-use.
- A greater level of compatibility through close working relationships with silicon vendors, major OEMs, and ISVs.
- A fully field-tested product. More than 200 leading OEMs ship millions of Phoenix ROM BIOS each year. In fact, more systems ship with Phoenix ROM BIOS than any other BIOS – including IBM.
- A brand name recognized, valued, and specified by end users.
- The widest array of system software products. Phoenix can provide you with a single source for your compatibility software across all your product platforms, including BIOS, utilities, and operating systems adaptation.
- Rigorously enforced legal safeguards. Phoenix pioneered the cleanroom method of compatibility product development.

Overview

Phoenix Technologies is the leading software developer that pioneered PC compatibility. By customizing its family of ROM BIOS products to support the widest variety of chip sets, processors, and bus architectures, Phoenix enables PC manufacturers to create complete product lines that offer full compatibility with industry standards.

With Phoenix ROM BIOS products, OEMs can get to market faster – without the added burden of standards-support engineering – and still be assured of full compatibility.

As part of this industry mandate to support leading standards, Phoenix now offers 80386 ROM BIOS for the VLSI TOPCAT 386DX chip set/Intel 82340DX. This Phoenix/VLSI/Intel combination is a high performance, low-cost firmware solution for i386™-based, AT®-compatible desktop, laptop, portable, and hand-held systems.

Flexible Memory Architecture

This three-component chip set features a variety of memory configuration options to suit your particular design needs, including two- or four-way interleaving of memory. This enables designers to specify less-expensive memory components. Systems employing this chip set/BIOS tandem can employ one-to-four banks of 32-bit DRAM using 256 KB, 1 MB, or 4 MB components, for a maximum of 64 MB on the system board.

Phoenix

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SPECIFICATIONS

CPU	Intel i386
Math Coprocessor Support	Intel i387
Processor Speeds	16-33 MHz
Bus Clock Speed	Adjustable bus clock speed for complete compatibility
BIOS Setup	**Choose:** • Register Control Mode (RCM) Setup for debugging and maximum configurability. Control all 26 programmable registers in the chip set. • Feature Control Mode (FCM) Setup for ease-of-use. Specify ROM shadowing in 16 KB blocks, or override dynamic memory configuration and set memory bank map.
BIOS Configuration	Code size: 64 KB or 128 KB BIOS supplied in your choice of configuration: • Two 27256 EPROMs • Four 27128 EPROMs • One 27512 EPROM • Two 27512 EPROMs (128 KB version)
Diskette Drives	5.25-inch: 160 KB, 180 KB, 320 KB, 36 KB, 1.2 MB 3.5-inch: 720 KB and 1.44 MB Support for two internal and two external diskette drives
Fixed-Disk Drives	Choose from 47 different OEM-customizable drive types in Setup Users can specify two drive types in CMOS memory ST506 (17 sectors-per-track), RLL (26 sectors-per-track), ARLL 36 sectors-per-track), and ESDI (34/36 sectors-per-track) devices supported
Keyboard Support	101/102-key and 83/84-key keyboard support Keyboard controller speeds of 6-12 MHz Keyboard-based CPU clock-speed switching (three speeds) Adjustable key-click volume (eight levels selectable from keyboard) Supports auto-sensing keyboards including Maxiswitch™ or BTC™ In addition to VLSI VL82C106/Intel 82341, the BIOS also supports Phoenix Keyboard Controller Firmware (8042-compatible) option
Standard Video Support	Software for MDA and CGA included Supports EGA and VGA BIOS options Monochrome, color direct-drive analog, and multiscan rate monitors supported
Optional Video Support	Phoenix Advanced Video BIOS (VGA-compatible) available Phoenix Enhanced Video BIOS PLUS (EGA-compatible) available Video BIOS can optionally reside in system BIOS ROMs to save cost and board space.
POST and Diagnostics	User-terminate memory test (up to 64 MB RAM) Support 80386's internal diagnostics System boot and run-time messages Beep codes identify subsystem-level problems if video fails

SPECIFICATIONS (Cont.)

Communication Device Support	Four serial ports (up to 19,200 baud) Four parallel ports with bidirectional mode support
Standard Utilities	HDFORM.EXE – low-level fixed-disk formatter EXDSKBIO.DRV – external diskette-device driver SETUP – ROM- or diskette-based system feature configurer
Standard Features	Customer sign-on message Support for hardware EMS, shadowing and fast A20 gating NMI handling to prevent system lockup after NMI Server configurations without keyboard or video Network station configurations without disk or diskette drives
Optional Features	SCSI fixed-disk drive support Phoenix EMS Driver provides full LIM 4.0 support Custom, non-standard I/O device support available PS/2®-style mouse operation and multi-level password security Laptop implementations
Deliverables	**Software:** • Object code (hex files) in EPROM and on diskette • Utility software (see above) • Serialized EPROM labels • Source code (if licensed) on diskette • Plink86 linker for source code licensees **Documentation:** • Release Notes • Guide to Features • Features Reference • User Guide • Technical Reference • Source Adaptation Guide • Application Notes

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VL82C286/VL82C386 ENHANCED 3.0 BIOS
VLSI TECHNOLOGY TOPCAT CHIP SET

Quadtel

Description

The Quadtel 286, 386/SX, 386, and 486 BIOS are IBM AT compatible BIOS products designed to operate with systems based on the VLSI Technology VL82C286/VL82C386 chip sets. These BIOS products provide the highest performance possible with the use of shadow RAM, interleaved, page mode zero wait-state memory with optional Cache Controller and intergrated Peripheral Controller at CPU speeds up to 33 MHz. Automatic memory sizing, bank reordering and configuration is provided to allow for the TOPCAT maximum amount of memory to be installed in the optimum system configuration. Using the shadow RAM logic designed into the chip sets, the ROM BIOS can be copied to RAM allowing for execution in high speed zero wait-state memory.

Extensive testing with OS/2, IBM Network and 3270 workstation program, Netware, Microsoft Windows and other BIOS-critical operating systems and applications ensure the highest degree of compatibility of any AT BIOS product available. Developed from specification with a clean-room methodology (as are all Quadtel BIOS products) legitimacy is always a standard feature.

Advanced features such as Setup in ROM, extensive directory of supported hard drives, two user configurable drive types (stored in CMOS) are all standard in this BIOS product. Custom features can be implemented for specialized hardware requirements. Most of the configuration options of the VL82C286/VL82C386 chips sets can be set with the BIOSEDIT™ program. These options include CPU speed, bus timing, DRAM timing, refresh timing, RAM/ROM configuration, address map configuration and more.

Features Summary

- Operates at CPU speeds up to 20 MHz (SX), 25 MHz (286), and 33 MHz (386/486)
- Fully compatible with OS/2, Netware, and other critical operating environments
- Automtic memory sizing, bank reordering and configuration during self-test
- Supports the maximum amount of RAM allowed by theTOPCAT chip set
- BIOSEDIT™ program allows the configuration of most BIOS options without source code
- Automatic detection and support provided for the 80287 (286), 80387SX (SX), and 80387 (386) coprocessors
- Intel 82385 and Austek 202 cache controllers supported
- ROM Setup allows configurable EMS, Extended, and Shadow RAM options
- Supports 47 fixed disk drive types
- Supports two user configurable drive types for those special one-of-a-kind drive configurations
- Supports 360K, 720K, 1.2MB, and 1.44MB diskette drive types
- Automatically supports the PC, XT, and AT keyboards with the Quadtel 8042 keyboard controller
- Keyboard selectable CPU speed switching
- Support for ESDI and RLL drives and controllers
- Compatible with the Quadtel 8042 Keyboard controller and the VL82C106 IPC internal keyboard controller
- Legitimacy assured through "clean-room" BIOS design
- Setup control of VL82C106 IPC dual serial ports, parallel port, IDE Fixed Disk and 37C65 FDC Chip Select
- EMS 4.0 Memory Manager and Productivity software (RAMDisk, Spooler and Cache) optionally available
- Optimized support for the FAST CPU RESET and GATE A20
- Diagonostics, Disk Cache, EMS, PS/2 Mouse Support and other optional BIOS Features available

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