VLSI TECHNOLOGY, INC.

486 PC/AT-COMPATIBLE SYSTEM CONTROLLER

VL82C486 DATA MANUAL

Desktop Systems Division
June 1992

ADVANCE INFORMATION

VLSI TECHNOLOGY, INC.
SC486 CONTROLLER DATA MANUAL
1992

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ADVANCE INFORMATION

PREFACE

This manual provides the reader with a preliminary technical reference for VLSI Technology, Inc.'s VL82C486 Single Chip 486 (SC486™) System Controller device for use in PC/AT-compatible applications. If you should require performance or functions not included in this manual, please contact your local VLSI Technology Design Center or Sales Office. The addresses are listed on the last page of this manual.

Since computer technology is extremely fast-moving, it is planned that VLSI's Personal Computer Products Division will revise, update, and publish this manual often. This will allow timely publication of data on new products, as well as improvements on existing ones. The most current information may also be obtained from your local VLSI Technology, Inc. Sales Office, Representative, or the Personal Computer Division in Tempe, Arizona.

Readers are encouraged to send their comments, corrections, or suggestions to:

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VLSI Technology, Inc.
8375 South River Parkway
Tempe, AZ 85284

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VL82C486

SINGLE-CHIP 486 (SC486™) CONTROLLER

FEATURES

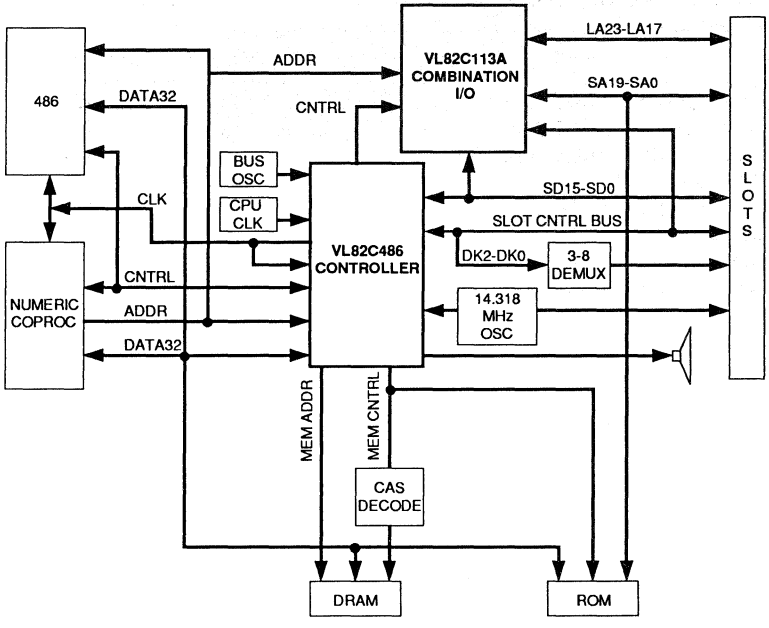
- Fully compatible 486-based PC/AT systems
- Up to 33 MHz CPU operation
- Replaces the following peripheral logic on the motherboard:
  - Two 82C37A DMA controllers
  - 74LS612 memory mapper (extended to support 64 MB)
  - Two 82C59A interrupt controllers
  - 82C54 timer
  - 82284 clock generator and ready interface
  - 82288 bus controller
- Includes:
  - Memory/refresh controller
  - Port A, B, and NMI logic
  - Bus steering logic
  - Parity generation/checking for on-board DRAM
  - Turbo Mode control
  - Hidden off-board, stolen on-board refresh
  - Staggered RAS refresh
  - Three-stateable outputs for board testing
- Memory controller features include:
  - Page Mode DRAM access
  - One to four banks 32 bits wide
  - One or two banks 64 bits wide
  - Two- or four-way interleave support
  - Programmable –RAS/CAS timing
  - Burst support
- Supports:
  - Up to 64 MB system memory
  - 256K, 1M, or 4M DRAM
  - Double-sided SIMMs
  - Secondary cache interface
  - 8- or 16-bit wide BIOS ROM
  - Shadow RAM in the 640K-1M area
  - Flash memory for BIOS ROM
  - Asynchronous ISA bus operation up to 16 MHz
  - Relocation of slot ROMs
- Power saving features include:
  - Sleep Mode
  - Slow DRAM refresh
- Other features:
  - Programmable for 10- or 16-bit internal I/O addressing
  - Programmable drive on DRAM and ISA bus signals
  - Programmable memory access to define "fast-bus", local bus, slot bus, and non-cacheable and write-protect areas
  - Input pin defines access to local bus devices
- 1.0-micron CMOS technology
- 208-lead metric quad flat pack (MQFP)

DESCRIPTION

The VL82C486 is a Single-Chip High Performance Controller for 486- and 486SX/487SX-based PC/AT systems.

The VL82C486 includes the dual 82C37A DMA controllers, dual 82C59A programmable interrupt controllers, 82C54 programmable interval timer, 82284 clock and ready generator, 82288 bus controller and the logic for address/data bus control, memory control, shutdown, refresh generation and refresh/DMA arbitration.

SYSTEM DIAGRAM (VL82C486-BASED PC/AT)



ORDER INFORMATION

Part Number	Package
VL82C486-FC	Metric Quad Flat Pack

Note: Operating temperature range is 0°C to +70°C.

SC486 is a trademark of VLSI Technology, Inc.

OVERVIEW

The VL82C486 Controller is designed to perform in 486DX- or 486SX/487SX-based PC/AT-compatible systems running up to 33 MHz. The VL82C486 replaces the following devices on the motherboard:

- Two 82C37A DMA controllers
- Two 82C59A interrupt controllers
- 82C54 timer
- 74LS612 memory mapper
- 82284 clock generator and ready interface
- 82288 bus controller

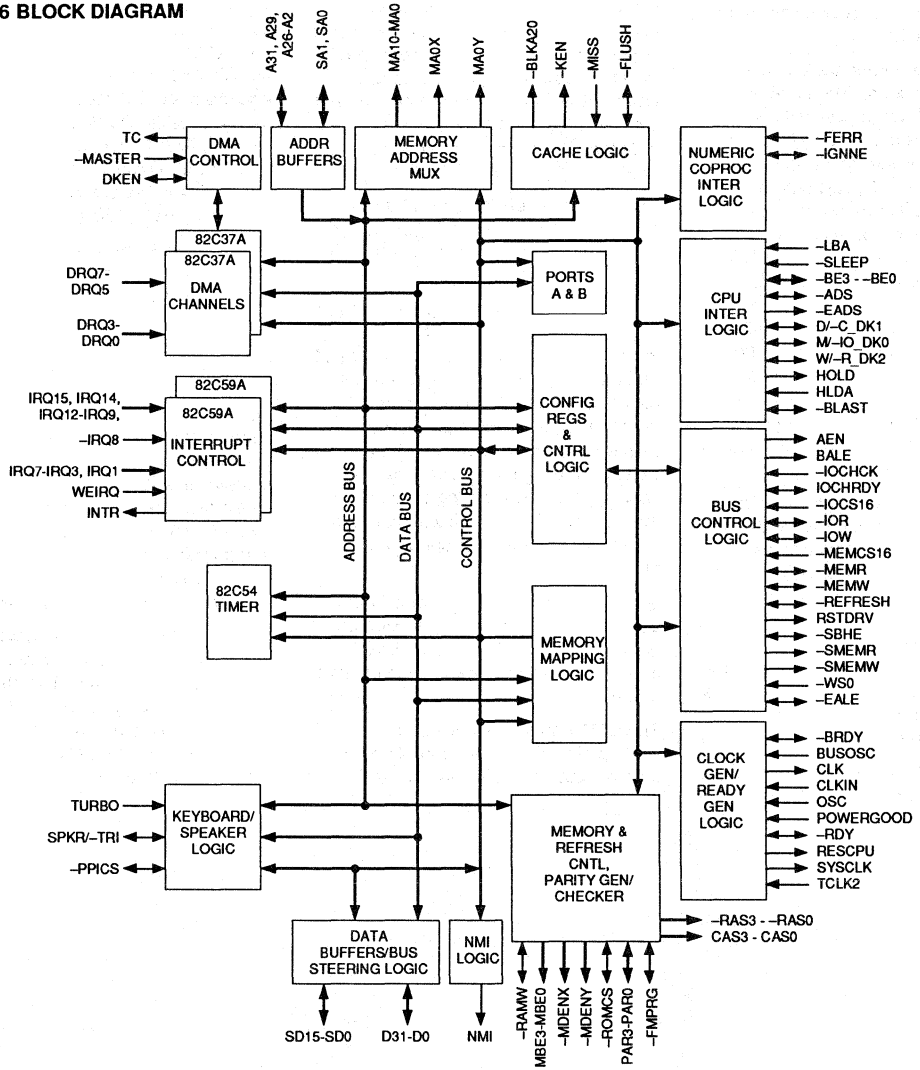
The controller also includes the following:

- Memory/refresh controller
- Port B and NMI logic
- Bus steering logic
- Turbo Mode control logic
- Parity checking logic
- Parity generation logic
- Support for Weitek numeric coprocessors

The memory controller logic is capable of accessing up to 64 MB. There can be up to four banks of 256K, 1M, or 4M DRAMs used in the system. The VL82C486 can drive four banks without external buffering. Built-in Page Mode operation and up to four-way interleaving allow the PC designer to maximize system performance using low cost DRAMs. Programmable DRAM timing is provided for RAS precharge, RAS-to-CAS delay, and CAS pulse width.

Shadowing features are supported on 16K boundaries between A0000h and FFFFFh (640 KB to 1 MB). Simultaneous use of shadowed ROM and direct system board access is possible

VL82C486 BLOCK DIAGRAM



in non-overlapping fashion throughout this memory space. Control over four access options is provided:

1. Access ROM or slot bus for reads and writes.
2. Access system board DRAM for reads and writes.
3. Access system board DRAM for reads and slot bus for writes.
4. Shadow Setup Mode. Read ROM or slot bus, write system board DRAM.

A special mode is supported for erasing and programming flash memories for the case where such devices are used as the BIOS ROMs.

Three special programmable address regions are provided. The fast-bus clock region allows accesses to certain memory regions at a faster ISA clock rate for fast on-board or off-board devices. A non-cacheable region and/or a write-protected region may be defined by a set of six registers that allow memory in the region 640 KB to 1 MB to be marked as non-cacheable and/or write-protected in increments of 16 KB. A further set of registers allows a memory range anywhere in the first 64 MB of memory to be marked as a DRAM region, an ISA bus region, or a local bus region either cacheable or non-cacheable in increments of 2 KB, 64 KB, or 1 MB.

Further support for devices that reside on the 486 local bus is provided through use of the –LBA (local bus access) input, which deselects the VL82C486 during CPU cycles. Also, a memory range anywhere in the first 64 MB of memory can be programmed via the internal Mapping Registers to make the VL82C486 access a local bus device as a 486 bus memory device during DMA or Master Mode transfers.

The VL82C486 handles system board refresh directly and also controls the timing of slot bus refresh. Refresh may be performed in Synchronous, Asynchronous, or Decoupled Mode. In Synchronous Mode, the slot bus and on-board DRAM refresh cycles proceed simultaneously and all memory cycles are held until both have completed. The Asynchronous Mode allows on- and off-board refreshes to be initiated simultaneously, but to complete asynchronously, allowing sooner access to DRAM. In Decoupled Mode, a separate refresh counter is used for slot bus refresh, allowing on-board DRAM and system refreshes to proceed independently, with DRAM refreshes initiated during bus idle cycles. CAS-before-RAS refresh is also supported. Refreshes are staggered to minimize power supply loading and attenuate noise on the VDD and ground pins. The VL82C486 supports the standard PC/AT refresh period of 15.625 µs as well as 125 µs.

Support for write-through cache controllers is provided through the use of a –MISS pin to detect cache-hits and cache-misses.

The interrupt controller logic consists of two 82C59A megacells with eight interrupt request lines each for a total of 16 interrupts. The two megacells are cascaded internally and two of the interrupt request inputs are connected to internal circuitry allowing a total of 13 external interrupt requests. There is special programmable logic included in the VL82C486 which allows deglitching of inputs on all the interrupt request pins.

The interval timer includes one 82C54 counter/timer megacell. The counter/timer has three independent 16-bit counters and six programmable counter modes.

The DMA controllers are 82C37A compatible. The DMA controllers control data transfers between an I/O channel and on- or off-board memory. DMA can transfer data over the full 64 MB range available. There are internal latches provided for latching the middle address bits output by the 82C37A megacells on the data bus, and the 74LS612 memory mappers are provided to generate the upper address bits.

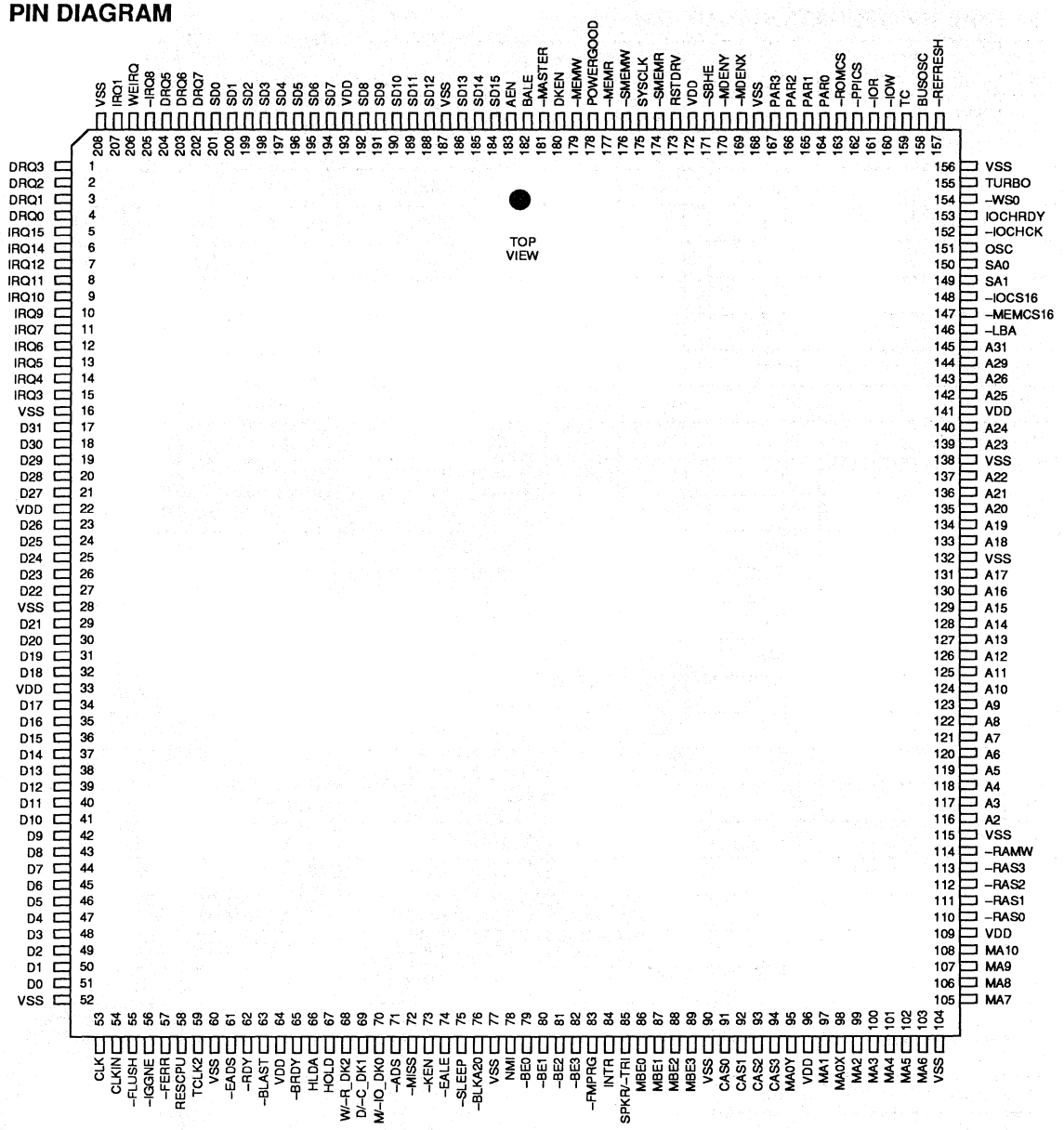
The VL82C486 can be programmed to generate the ISA bus timing from the CPU clock oscillator or a separate asyncronous oscillator.

The VL82C486 also performs all of the data buffer control functions required for a 486XX processor-based PC/AT system. Under the control of the CPU, the VL82C486 routes data to and from the CPU's D bus, the internal XD bus, and the slots (SD bus). During CPU ISA bus reads, the data is latched for synchronization with the CPU. Parity is checked for D bus DRAM read operations. The chip does not generate parity for CPU writes to DRAM.

When the DMA requestor or external bus master is the bus owner, the VL82C486 allows data transfer between the slot SD bus and the CPU local D bus. The chip also performs low-to-high and high-to-low byte swaps on the 16-bit SD bus. Parity is generated by the VL82C486 during DMA or Master writes to on-board DRAM. The chip also provides a single input, –TRI, to disable all of its outputs for board level testability. This is a dual function pin SPKR/–TRI. Care must be taken so that the pin is sampled high at the rising edge of POWERGOOD. A coupling to the speaker circuit is recommended.

The VL82C486 Controller functions are programmable via a set of internal configuration registers. The state of various interface pins on reset is used to determine the default configuration. A dip switch can be used to establish the initial configuration.

PIN DIAGRAM


TOP VIEW
1 DRQ3
2 DRQ2
3 DRQ1
4 DRQ0
5 IRQ15
6 IRQ14
7 IRQ12
8 IRQ11
9 IRQ10
10 IRQ9
11 IRQ7
12 IRQ6
13 IRQ5
14 IRQ4
15 IRQ3
16 VSS
17 D31
18 D30
19 D29
20 D28
21 D27
22 VDD
23 D26
24 D25
25 D24
26 D23
27 D22
28 VSS
29 D21
30 D20
31 D19
32 D18
33 VDD
34 D17
35 D16
36 D15
37 D14
38 D13
39 D12
40 D11
41 D10
42 D9
43 D8
44 D7
45 D6
46 D5
47 D4
48 D3
49 D2
50 D1
51 D0
52 VSS
53 CLK
54 CLKIN
55 –FLUSH
56 –IGGNE
57 –FERR
58 RESCPU
59 TCLK2
60 VSS
61 –EADS
62 –RDY
63 –BLAST
64 VDD
65 –BRDY
66 HLDA
67 HOLD
68 W/–R_DK2
69 D/–C_DK1
70 M/–IO_DK0
71 –ADS
72 –MISS
73 –KEN
74 –EALE
75 –SLEEP
76 –BLKA20
77 VSS
78 NMI
79 –BE0
80 –BE1
81 –BE2
82 –BE3
83 –FMPRG
84 INTR
85 SPKR/–TRI
86 MBE0
87 MBE1
88 MBE2
89 MBE3
90 VSS
91 CAS0
92 CAS1
93 CAS2
94 CAS3
95 MA0Y
96 VDD
97 MA1
98 MA0X
99 MA2
100 MA3
101 MA4
102 MA5
103 MA6
104 VSS
105 MA7
106 MA8
107 MA9
108 MA10
109 VDD
110 –RAS0
111 –RAS1
112 –RAS2
113 –RAS3
114 –RAMW
115 VSS
116 A2
117 A3
118 A4
119 A5
120 A6
121 A7
122 A8
123 A9
124 A10
125 A11
126 A12
127 A13
128 A14
129 A15
130 A16
131 A17
132 VSS
133 A18
134 A19
135 A20
136 A21
137 A22
138 VSS
139 A23
140 A24
141 VDD
142 A25
143 A26
144 A29
145 A31
146 –LBA
147 –MEMCS16
148 –IOCS16
149 SA1
150 SA0
151 OSC
152 –IOCHCK
153 IOCHRDY
154 –WS0
155 TURBO
156 VSS
157 –REFRESH
158 BUSOSC
159 TC
160 –IOW
161 –IOR
162 –PPICS
163 –ROMCS
164 PAR0
165 PAR1
166 PAR2
167 PAR3
168 VSS
169 –MDENX
170 –MDENY
171 –SBHE
172 VDD
173 RSTDRV
174 –SMEMR
175 SYSCLK
176 –SMEMW
177 –MEMR
178 POWERGOOD
179 –MEMW
180 DKEN
181 –MASTER
182 BALE
183 AEN
184 SD15
185 SD14
186 SD13
187 VSS
188 SD12
189 SD11
190 SD10
191 SD9
192 SD8
193 VDD
194 SD7
195 SD6
196 SD5
197 SD4
198 SD3
199 SD2
200 SD1
201 SD0
202 DRQ7
203 DRQ6
204 DRQ5
205 –IRQ8
206 WEIRQ
207 IRQ1
208 VSS

PIN TYPE BY OPERATIONAL STATE

Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pin #	Pin Name	Pin Type	Input Type	Drive (mA)
1	DRQ3	I-PU	TTL-S		33	VDD	PWR		
2	DRQ2	I-PU	TTL-S		34	D17	IO	TTL	8
3	DRQ1	I-PU	TTL-S		35	D16	IO	TTL	8
4	DRQ0	I-PU	TTL-S		36	D15	IO	TTL	8
5	IRQ15	I-PU	TTL-S		37	D14	IO	TTL	8
6	IRQ14	I-PU	TTL-S		38	D13	IO	TTL	8
7	IRQ12	I-PU	TTL-S		39	D12	IO	TTL	8
8	IRQ11	I-PU	TTL-S		40	D11	IO	TTL	8
9	IRQ10	I-PU	TTL-S		41	D10	IO	TTL	8
10	IRQ9	I-PU	TTL-S		42	D9	IO	TTL	8
11	IRQ7	I-PU	TTL-S		43	D8	IO	TTL	8
12	IRQ6	I-PU	TTL-S		44	D7	IO	TTL	8
13	IRQ5	I-PU	TTL-S		45	D6	IO	TTL	8
14	IRQ4	I-PU	TTL-S		46	D5	IO	TTL	8
15	IRQ3	I-PU	TTL-S		47	D4	IO	TTL	8
16	VSS	GND			48	D3	IO	TTL	8
17	D31	IO	TTL	8	49	D2	IO	TTL	8
18	D30	IO	TTL	8	50	D1	IO	TTL	8
19	D29	IO	TTL	8	51	D0	IO	TTL	8
20	D28	IO	TTL	8	52	VSS	GND		
21	D27	IO	TTL	8	53	CLK	O		24
22	VDD	PWR			54	CLKIN	I	CMOS	
23	D26	IO	TTL	8	55	–FLUSH	IO (Note 2)	TTL	8
24	D25	IO	TTL	8	56	–IGNNE	IO (Note 2)	TTL	8
25	D24	IO	TTL	8	57	–FERR	I-PU	TTL	
26	D23	IO	TTL	8	58	RESCPU	O		8
27	D22	IO	TTL	8	59	TCLK2	I	CMOS	
28	VSS	GND			60	VSS	GND		
29	D21	IO	TTL	8	61	–EADS	O		8
30	D20	IO	TTL	8	62	–RDY	IO-PU	TTL	8
31	D19	IO	TTL	8	63	–BLAST	IO	TTL	8
32	D18	IO	TTL	8	64	VDD	PWR		

PIN TYPE BY OPERATIONAL STATE (Cont.)

Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pin #	Pin Name	Pin Type	Input Type	Drive (mA)
65	–BRDY	IO-PU	TTL	8	97	MA1	O		12/24/36/48
66	HLDA	I	TTL		98	MA0X	O		12/24
67	HOLD	O		8	99	MA2	O		12/24/36/48
68	W/–R_DK2	IO	TTL	8	100	MA3	O		12/24/36/48
69	D/–C_DK1	IO	TTL	8	101	MA4	O		12/24/36/48
70	M/–IO_DK0	IO	TTL	8	102	MA5	O		12/24/36/48
71	–ADS	IO	TTL	8	103	MA6	O		12/24/36/48
72	–MISS	I	TTL		104	VSS	GND		
73	–KEN	O		8	105	MA7	O		12/24/36/48
74	–EALE	IO (Note 2)	TTL	8	106	MA8	O		12/24/36/48
75	–SLEEP	I	TTL		107	MA9	O		12/24/36/48
76	–BLKA20	IO (Note 2)	TTL	8	108	MA10	O		12/24/36/48
77	VSS	GND			109	VDD	PWR		
78	NMI	O		8	110	–RAS0	O		12/24
79	–BE0	IO	TTL	8	111	–RAS1	O		12/24
80	–BE1	IO	TTL	8	112	–RAS2	O		12/24
81	–BE2	IO	TTL	8	113	–RAS3	O		12/24
82	–BE3	IO	TTL	8	114	–RAMW	IO (Note 2)		12/24/36/48
83	–FMPRG	IO (Note 2)	TTL	8	115	VSS	GND		
84	INTR	O		8	116	A2	IO	TTL	8
85	SPKR/–TRI	IO-PU	TTL	24	117	A3	IO	TTL	8
86	MBE0	O		8	118	A4	IO	TTL	8
87	MBE1	O		8	119	A5	IO	TTL	8
88	MBE2	O		8	120	A6	IO	TTL	8
89	MBE3	O		8	121	A7	IO	TTL	8
90	VSS	GND			122	A8	IO	TTL	8
91	CAS0	O		12	123	A9	IO	TTL	8
92	CAS1	O		12	124	A10	IO	TTL	8
93	CAS2	O		12	125	A11	IO	TTL	8
94	CAS3	O		12	126	A12	IO	TTL	8
95	MA0Y	O		12/24	127	A13	IO	TTL	8
96	VDD	PWR			128	A14	IO	TTL	8

PIN TYPE BY OPERATIONAL STATE (Cont.)

Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pin #	Pin Name	Pin Type	Input Type	Drive (mA)
129	A15	IO	TTL	8	161	–IOR (Note 1)	IO	TTL	12/24
130	A16	IO	TTL	8	162	–PPICS	IO (Note 2)	TTL	8
131	A17	IO	TTL	8	163	–ROMCS	IO (Note 2)	TTL	8
132	VSS	GND			164	PAR0	IO	TTL	8
133	A18	IO	TTL	8	165	PAR1	IO	TTL	8
134	A19	IO	TTL	8	166	PAR2	IO	TTL	8
135	A20	IO	TTL	8	167	PAR3	IO	TTL	8
136	A21	IO	TTL	8	168	VSS	GND		
137	A22	IO	TTL	8	169	–MDENX	O		12
138	VSS	GND			170	–MDENY	O		12
139	A23	IO	TTL	8	171	–SBHE	IO	TTL	12/24
140	A24	IO	TTL	8	172	VDD	PWR		
141	VDD	PWR	TTL		173	RSTDRV	O		8
142	A25	IO	TTL	8	174	–SMEMR (Note 1)	O		12/24
143	A26	IO	TTL	8	175	SYSCLK	O		12/24
144	A29	IO	TTL	8	176	–SMEMW (Note 1)	O		12/24
145	A31	IO	TTL	8	177	–MEMR (Note 1)	IO	TTL	12/24
146	–LBA	I	CMOS		178	POWERGOOD	I-PU	TTL-S	
147	–MEMCS16	I	TTL		179	–MEMW (Note 1)	IO	TTL	12/24
148	–IOCS16	I	TTL		180	DKEN	IO (Note 2)	TTL	12/24
149	SA1	IO	TTL	12/24	181	–MASTER	I	TTL	
150	SA0	IO	TTL	12/24	182	BALE	O	TTL	12/24
151	OSC	I	TTL		183	AEN	O	TTL	12/24
152	–IOCHCK	I	TTL		184	SD15	IO	TTL	12/24
153	IOCHRDY (Note 1)	IO-OD	TTL	12	185	SD14	IO	TTL	12/24
154	–WS0	I	TTL		186	SD13	IO	TTL	12/24
155	TURBO	I	TTL		187	VSS	GND		
156	VSS	GND			188	SD12	IO	TTL	12/24
157	–REFRESH (Note 1)	IO-OD	TTL	24	189	SD11	IO	TTL	12/24
158	BUSOSC	I-PU	TTL		190	SD10	IO	TTL	12/24
159	TC	O		12/24	191	SD9	IO	TTL	12/24
160	–IOW (Note 1)	IO	TTL	12/24	192	SD8	IO	TTL	12/24

PIN TYPE BY OPERATIONAL STATE (Cont.)

Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pin #	Pin Name	Pin Type	Input Type	Drive (mA)
193	VDD	PWR			201	SD0	IO	TTL	12/24
194	SD7	IO	TTL	12/24	202	DRQ7	I-PU	TTL-S	
195	SD6	IO	TTL	12/24	203	DRQ6	I-PU	TTL-S	
196	SD5	IO	TTL	12/24	204	DRQ5	I-PU	TTL-S	
197	SD4	IO	TTL	12/24	205	–IRQ8	I-PU	TTL-S	
198	SD3	IO	TTL	12/24	206	WEIRQ	I-PD	TTL	
199	SD2	IO	TTL	12/24	207	IRQ1	I-PU	TTL-S	
200	SD1	IO	TTL	12/24	208	VSS	GND		

Notes: 1. These pins require an external pull-up resistor (10 kΩ is recommended).

2. These pins are inputs only during POR (power-on reset).

Legend:

CMOS	CMOS-compatible input
I	Input-only pin
IO	Bidirectional pin
GND	Ground pin
O	Output-only pin
OD	Open drain
PWR	Power supply pin
TTL	TTL-compatible input
-PD	Indicates a high-impedance with approximately 10 kΩ minimum resistance to VSS (internal pull-down resistor on pin).
-PU	Indicates a high-impedance with approximately 10 kΩ minimum resistance to VDD (internal pull-up resistor on pin).
-S	Indicates a Schmitt-trigger input with hystersis for noise immunity.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Pin Type	Signal Description
CPU INTERFACE SIGNALS			
A31, A29, A26-A2	145, 144, 143, 142, 140, 139, 137-133, 131-116	IO	Address bus - This bidirectional address bus is driven by the bus master. It is driven out by the VL82C486 during Non-Master Mode DMA and refresh cycles when HLDA is active and –MASTER is inactive. The signals A25-A2 allow access to 64 MB of system memory. The upper two bits of the bus, A31 and A29, are used for accessing system ROM and the Weitek numeric coprocessor A26 is used to provide a non-aliased unused address space above 64 MB to assist memory sizing routines.
–ADS	71	IO	Address Status - The active low Address Status (–ADS) signal is driven by the 486 as an indication that the address and control signals currently supplied by the CPU are valid. This signal is used internally to indicate that the data and command are valid and determine the beginning of a memory or I/O cycle. –ADS is driven by the VL82C486 when HLDA is active, and is made low for one CPU clock cycle at the beginning of DMA or Master Mode cycles when a local bus region is selected by the PMR Registers.
–BE3 - –BE0	82-79	IO	Byte Enable bits 3 through 0 - These signals are normally inputs to the VL82C486 and indicate which bytes on D31-D0 are involved in a memory or I/O access. They are ignored during all DRAM reads. –BE3 - –BE0 are driven by the VL82C486 when HLDA is active and indicate which one or two bytes are involved in an 8- or 16-bit DMA or Master Mode transfer between the slot I/O and a local bus device.
–BLAST	63	IO	Burst Last - This signal is used by the VL82C486 as an indicator of when to terminate the current burst cycle, if the length of the burst cycle is less than four double words. It is driven low by the VL82C486 when HLDA is active, since the VL82C486 does not support Burst Mode during DMA or Master Mode cycles.
–BRDY	65	IO-PU	Burst Ready - The active low ready (–BRDY) signal indicates to the 486 that the current burst cycle is complete. It is driven low when valid data has been presented to the CPU in response to a read command or when data has been accepted in response to a write command from the CPU. The VL82C486 drives –BRDY on all local bus DRAM accesses, but never drives it in response to slot bus accesses (see –RDY definition). The VL82C486 enables the –BRDY three-state output only when it needs to drive it low and leaves –BRDY enabled for just one CPU clock cycle after it has driven –BRDY high again. When HLDA is active, –BRDY is an input to the VL82C486 and may be driven by a local bus device to terminate DMA or Master Mode cycles. This pin has an internal pull-up resistor.
CLK	53	O	Clock - This output is a CMOS level signal which is normally one-half the frequency of the TCLK2 signal. It is used by the CPU and other on-board logic.
CLKIN	54	I	Input Clock - This is the fundamental clock input to the VL82C486. It must be the same clock as that supplied to the 486.
M/–IO_DK0	70	IO	Memory Input/Output or DMA Acknowledge bit 0 - When HLDA is low, M/–IO_DK0 is driven by the local bus master and is decoded with D/–C_DK1 and W/–R_DK2 to indicate the type of bus cycle requested When HLDA is high, M/–IO_DK0 is an output signal which along with D/–C_DK1 and W/–R_DK2 represents the encoded channel number being serviced at the beginning of DMA acknowledge cycles. If the VL82C486 makes –ADS active during DMA or Master Mode cycles (for local bus accesses) this signal is forced high.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Pin Type	Signal Description
D/–C_DK1	69	IO	Data Control or DMA Acknowledge bit 1 - When HLDA is low, D/–C_DK1 is driven by the local bus master and is decoded with M/–IO_DK0 and W/–R_DK2 to indicate the type of bus cycle requested. When HLDA is high, D/–C_DK1 is an output signal which along with M/–IO_DK0 and W/–R_DK2 represents the encoded channel number being serviced at the beginning of DMA acknowledge cycles. If the VL82C486 makes –ADS active during DMA or Master Mode cycles (for local bus accesses), the D/–C_DK1 signal is forced high.
W/–R_DK2	68	IO	Write/Read or DMA Acknowledge bit 2 - When HLDA is low, W/–R_DK2 is driven by the local bus master and is decoded with D/–C_DK1 and M/–IO_DK0 to indicate the type of bus cycle requested. When HLDA is high, W/–R_DK2 is an output signal which along with D/–C_DK1 and M/–IO_DK0 represents the encoded channel number being serviced at the beginning of DMA acknowledge cycles. If the VL82C486 makes –ADS active during DMA or Master Mode cycles (for local bus accesses), the W/–R_DK2 signal indicates whether a local bus read or write cycle is required.
D31-D0	17-21, 23-27 29-32, 34-51	IO	CPU Data Bus bits 31 through 0 - This is the data bus directly connected to the CPU and other external devices.
–EADS	61	O	External Address - The active low external address signal indicates a primary cache invalidation address is on the address bus. It is driven low by the VL82C486 to perform primary cache invalidations during DMA and Master Mode cycles, and is also driven low for one cycle during the first T2 of a local bus write to a write-protected memory location. It is also modulated for implementation of the Non-Turbo Mode.
–FERR	57	I-PU	Floating Point Error - This signal indicates a floating point error. When active, it generates interrupt IRQ13 internal to the VL82C486. This input pin is active low and has an internal pull-up.
HLDA	66	I	Hold Acknowledge - An active high signal that is issued by the CPU in response to the HOLD signal driven by the VL82C486. It indicates that the CPU is floating its outputs' to the high impedance state so that another master can take control of the bus.
HOLD	67	O	Hold Request - This active high output signal is driven by the VL82C486 to the CPU. It indicates that a bus master (such as a DMA or refresh controller) is requesting control of the bus. It is synchronized to CLKIN.
–IGNNE	56	IO (Note 1)	Ignore Numeric Error Output (or POR Input) - This active low output, when asserted, indicates to the CPU to ignore the present numeric error. This signal is enabled when a dummy write is performed to either Port F0h or F1h with –FERR also active. –IGNNE is an input during power-on reset to set SA1 timing.
INTR	84	O	Interrupt Request - An active high output used to interrupt the CPU. It is generated by the 82C59A megacell any time a valid interrupt request input is received.
–KEN	73	O	Cache Enable - This signal determines whether the current cycle is cacheable. It is normally low, but is driven inactive during the second and subsequent T2 cycles of all CPU memory accesses that are defined non-cacheable, except when local bus CPU cycles are selected by the PMR Registers; in this case, it is made inactive during the first subsequent T2s of the local bus cycle.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Pin Type	Signal Description
NMI	78	O	Non-Maskable Interrupt - An active high output which indicates to the CPU that an external non-maskable interrupt has been generated. This signal is asserted by either a parity error or an I/O channel error. The NMI output is enabled by resetting the MSB (most significant bit) of I/O Port 70h. NMI is disabled on reset.
–RDY	62	IO-PU	(Non-Burst) Ready - Driven by the VL82C486, this active low signal is an indication that the current memory or I/O slot bus cycle is complete. The VL82C486 enables the –RDY three-state output only when it needs to drive it low and leaves it enabled for just one CPU clock cycle after it has driven –RDY high again. When HLDA is active, –RDY is an input to the VL82C486 and may be driven by local bus devices to terminate DMA and Master Mode cycles. This pin has an internal pull-up resistor.
RESCPU	58	O	Reset CPU - This active high output resets the CPU. It is synchronous to CLKIN and is asserted in response to one of the following: 1. A dummy read from I/O Port EFh. 2. The LSB (least significant bit) of Port A is set to 1 by an active write. 3. The POWERGOOD signal changes state. 4. A Shutdown command.
TCLK2	59	I	This input is connected to a crystal oscillator that has a frequency of twice the system frequency. It is divided and sent to the CLK output.
ON-BOARD MEMORY SYSTEM INTERFACE SIGNALS			
CAS3-CAS0	94-91	O	Column Address Strobe bits 0 through 3 - These signals generate high-going column address strobes for DRAM banks during on-board memory bus cycles. The active period for these signals is determined by the number of wait states and the configuration mode.
MBE3-MBE0	89-86	O	Memory Byte Enable bits 3 through 0 - These signals are used along with the CAS3-CAS0 signals to generate independent column address strobes for each of the four DRAM banks.
MA10-MA1	108-105, 103-99, 97	O	Memory Address bus bits 10 through 1 - These address bits are the row and column addresses sent to on-board memory. They are buffered and multiplexed versions of the local CPU bus address. They allow addressing of up to 64 MB of memory by the VL82C486.
MA0X	98	O	Memory Address bus bit 0, Banks 0 and 2 - This signal is a multiplexed row/column address bit for Banks 0 and 2. It is interleaved with MA0Y to ensure that DRAM setup and hold times are met for A3 during the Fast Burst Interleave Mode.
MA0Y	95	O	Memory Address bus bit 0, Banks 1 and 3 - This signal is a multiplexed row/column address bit for Banks 1 and 3. It is interleaved with MA0X to ensure that DRAM setup and hold times are met for A3 during the Fast Burst Interleave Mode.
–MDENX, –MDENY	169, 170	O	Memory Dword Enable bits X and Y - These active low outputs select the upper and lower 32-bit double word when a 64-bit wide DRAM bank is connected in a system. –MDENX and –MDENY enable the upper and lower 32 bits of the 64-bit DRAM data bus onto the 32-bit CPU data bus. They are never enabled simultaneously during DRAM reads and are always enabled simultaneously during DRAM writes.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Pin Type	Signal Description
PAR3-PAR0	167-164	IO	Parity bits 3 through 0 - Each parity bit signal is associated with one byte of the data bus. PAR3–PAR0 are written to memory along with their corresponding bytes during DMA and Master Mode memory write operations. During memory read operations, these pins become inputs and are used along with their respective data bytes to determine if a parity error has occurred.
–RAMW	114	IO (Note 1)	RAM Write Output (or POR Input) - This active low output is sent to the DRAM memory to control the direction of data flow of the on-board memory. It is active during on-board memory write cycles and high at all other times. –RAMW is an input during power-on reset to set the BIOS ROM location.
–RAS3- –RAS0	113-110	O	Row Address Strobe bits 3 through 0 - These signals are sent to each of the four DRAM banks to strobe in the row address during on-board memory bus cycles.
CACHE CONTROLLER INTERFACE SIGNALS			
–BLKA20	76	IO (Note 1)	Block A20 Output (or POR Input) - When this signal is low, it indicates that the CPU and cache should mask address bit 20 (A20) for all operations. –BLKA20 is an input during power-on-reset to set the DRAM output drives.
–FLUSH	55	IO (Note 1)	Cache Flush Output (or POR Input) - This signal goes low for one CPU clock cycle in the second T2 of a local bus flush cycle. –FLUSH is an input during power-on reset to set DKEN polarity.
–MISS	72	I	Cache Miss - This active low input is made active by a cache controller at the start of a CPU memory read cycle if the operand is not in the secondary cache. When high in T2 of any CPU memory access, it causes the VL82C486 to cancel the requested cycle. It is tied low when no secondary cache is used. –MISS is ignored during on-board DRAM cycles for DMA/Master Mode cycles unless the –EALE pin is pulled low (for write-back cache option) during power-on reset; in which case it inhibits DMA/Master Mode DRAM read cycles if it is made high when –MEMR is active.
PERIPHERAL INTERFACE SIGNALS			
–EALE	74	IO (Note 1)	Early Address Latch Enable Output (or POR Input) - This signal is normally low. It goes high when BALE is high for all CPU slot bus cycles. During ISA bus refresh cycles –EALE goes high for 0.5 SYSCLKs before going low again. –EALE is an input during power-on reset to set the –MISS operation.
–FMPRG	83	IO (Note 1)	Flash Memory Program Output (or POR Input) - This signal is asserted when the FMPRG bit (bit 2) in the ROMSET Register is set. It may be used to gate the appropriate programming voltage to the flash memory. –FMPRG is an input during power-on reset to set the slot current drive.
–LBA	146	I	Local Bus Access - During CPU accesses, this signal must be made low by a local bus device before one half-way through the first T2 cycle of any CPU bus cycle that normally accesses on-board DRAM, or before the end of first T2 for any other type of cycle, if a CPU access is to a local bus device. It causes the VL82C486 to be deselected.
–PPICS	162	IO (Note 1)	Peripheral Chip Select Output (or POR Input) - This output signal is an active low chip select for the keyboard controller and real-time clock. It is active any time a system bus address is 60h, 64h, 70h, or 71h. –PPICS is an input during power-on reset to set the DRAM output drivers.
POWERGOOD	178	I-PU	System Power-On Reset - An active high input signal indicating that the power to the board is stable. A Schmitt-trigger input is used, thus allowing the input to be connected directly to an RC network.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Pin Type	Signal Description
–ROMCS	163	IO (Note 1)	ROM Chip Select Output (or POR Input) - This active low signal is asserted during CPU cycles that access on-board system ROM. The on-board system ROM may reside either on the local (D) bus or the ISA (SD) bus. –ROMCS is an input during power-on reset to set the DRAM configuration.
–SLEEP	75	I	Sleep Mode - A high-to-low transition on this pin puts the VL82C486 into the Sleep Mode. The Sleep Mode is when the refresh divider is active, BUSOSC is shut-off from non-essential internal circuitry, and the CPU is halted by HOLD going high.
SPKR/–TRI	85	IO-PU	Speaker or Three-State - This pin functions as the SPKR output signal and as the active low Three-State input signal. The active high SPKR output drives an externally buffered speaker. This signal is an input when the POWERGOOD input is low. If this input is sampled low, it forces the VL82C486 into the Three-State Mode where all outputs and bidirectional pins are driven to a high impedance state. This pin has an internal pull-up resistor.
TURBO	155	I	Turbo Mode - This bit determines the speed at which the CPU operates. When set low, hold signals to the 486 are continuously generated in order to slow its operation. It is also an input to the NTBREF Register from which its state may be read by software.
WEIRQ	206	I-PD	Weitek Numeric Coprocessor Interrupt - The active high WEIRQ signal indicates that an error has occurred within the Weitek numeric coprocessor. It causes an internal IRQ13 to be generated. This pin has an internal pull-down resistor.
BUS INTERFACE SIGNALS			
AEN	183	O	Address Enable - An active high output that indicates a DMA transfer cycle to the I/O resources on the bus. It is asserted only when the DMA controller is the bus owner (HLDA = 1, –MASTER = 1). The I/O resource with an active DMA Acknowledge signal should only respond to the I/O command lines and all the other I/O resources should ignore the commands.
BALE	182	O	Bus Address Latch Enable - This active high pulse is generated at the beginning of any bus cycle initiated by the CPU. It indicates when the SA19-SA0, LA23-LA17, AEN, and –SBHE signals are valid. BALE is forced high any time HLDA is high.
BUSOSC	158	I-PU	System Bus Clock - This signal is supplied by an external oscillator. It has a nominal 50% duty cycle and normally has a frequency of 16 MHz. It is used for ISA bus operations. If an oscillator is connected to this pin, SYSCLK can be programmed to be BUSOSC +2, +4, +6, or +8. If SYSCLK is to be derived from CLKIN, BUSOSC is held high or low and is used in conjunction with the CLKCTL Register to determine the clock divider value.
DKEN	180	IO (Note 1)	DMA Acknowledge Enable Input (or POR Output) - This signal enables an external 3-to-8 decoder for the generation of the DMA acknowledge signals from M/–IO_DK0, D/–C_DK1 and W/–R_DK2 when these signals are valid at the beginning of a DMA cycle. If a local bus cycle is started during a DMA cycle, then DKEN must also be used to latch the DMA acknowledges when active. It is active high when the –FLUSH signal is pulled high during power-on reset and is active low when –FLUSH is pulled low during power-on reset. DKEN is an input during power-on-reset to set the BIOS ROM width.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Pin Type	Signal Description
DRQ7-DRQ5 DRQ3-DRQ0	202-204 1-4	I-PU	DMA Request bits 7 through 5 and 3 through 0 - These asynchronous inputs are used by external devices to indicate when they need service from the internal DMA controllers. DRQ3-DRQ0 are used for transfers between 8-bit I/O adapters and system memory. DRQ7-DRQ5 are used for transfers between 16-bit I/O adapters and system memory. DRQ4 is not available externally as it is used to cascade the two DMA controllers together. All DRQ pins have internal pull-ups.
–IOCHCK	152	I	I/O Channel Check - This active low input signal indicates that an error has taken place on the I/O bus. If I/O checking is enabled, an –IOCHCK assertion by a peripheral device generates an NMI to the processor if bit 3 (ENA_IO_CHK) of Port B is set to 0. The state of the –IOCHCK signal is read as data bit 6 (CHAN_CHK) of Port B.
IOCHRDY	153	IO-OD	I/O Channel Ready - This input is pulled low in order to extend the read or write cycles of any bus access when required. The cycle can be initiated by the CPU, DMA controllers or refresh controller. The default number of wait states for cycles initiated by the CPU are four wait states for 8-bit peripherals, one wait state for 16-bit peripherals, and three wait states for ROM cycles. One DMA wait state is inserted as the default for all DMA cycles. Any peripheral that cannot present read data or strobe in write data in this amount of time must use IOCHRDY to extend these cycles. In the DMA Mode, this pin is always driven low by the VL82C486 that generates local bus cycles to allow for local bus latency. The VL82C486 never drives IOCHRDY high, but three-states it when not driven low. This pin requires an external 10 kΩ pull-up resistor.
–IOCS16	148	I	16-bit I/O Chip Select - This input signal determines when a 16-bit to 8-bit conversion is needed for CPU accesses. A conversion is done any time the VL82C486 requests a 16-bit I/O cycle and –IOCS16 is sampled high. A command delay of one BUSOSC cycle is inserted and the cycle becomes four wait states long when a conversion is needed. If sampled low, an I/O access is performed in one wait state with one command delay inserted. The –IOCS16 signal is ignored by the DMA and refresh controller for DMA transfer and refresh cycles, respectively.
–IOW –IOR	160 161	IO IO	Input/Output Write Input/Output Read –IOR and –IOW are active low inputs when an external bus master is in control (HLDA = 1, –MASTER = 0). They function as outputs at all other times. When HLDA is low, they are driven by the internal ISA bus controller. During DMA transfer cycles (HLDA = 1, –MASTER = 1), they are driven by the 82C37A DMA controller megacells. They are inactive during a refresh cycle. Both the pins require external 10 kΩ pull-up resistors.
IRQ15, IRQ14 IRQ12-IRQ9 IRQ7-IRQ3 IRQ1, –IRQ8	5, 6 7-10 11-15 207, 205	I-PU	Interrupt Requests - These are the asynchronous interrupt request inputs to the 82C59A megacells. IRQ0, IRQ2, and IRQ13 are not available as external inputs because they are used internally. All IRQ input pins except –IRQ8 are active high and have internal pull-ups. –IRQ8 is an active low input. All IRQ pins have a special programmable logic to reduce noise sensitivity. The logic is controlled by the IRQIN bit (bit 0) in the MISCSET Register. When IRQIN is set, the input to these pins must be stable for at least 105 ns to generate an interrupt.
–MASTER	181	I	Bus Master - An active low input used by an external device to get access to the system bus. When asserted, it indicates that an external bus master has control of the bus.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Pin Type	Signal Description
–MEMCS16	147	I	16-Bit Memory Chip Select - This active low input is used to determine when a 16-to-8 bit conversion is needed for CPU accesses. A conversion is done any time the VL82C486 requests a 16-bit memory cycle and –MEMCS16 is sampled high. If sampled high, a command delay of one BUSOSC cycle is inserted and the cycle becomes four wait states long. If sampled low, a memory access is performed in one wait state with no command delays inserted. The –MEMCS16 signal is ignored by the DMA and refresh controller for transfer and refresh cycles, respectively.
–MEMR –MEMW	177 179	IO IO	Memory Read Memory Write These active low signals are inputs when an external bus master is in control (HLDA = 1, –MASTER = 0). They are outputs at all other times. When HLDA is low, –MEMW is driven from the ISA bus controller. They are driven by the 82C37A DMA controllers during DMA cycles. Both pins require external 10 kΩ pull-up resistors.
OSC	151	I	Oscillator Input - The buffered input of the 14.31818 MHz oscillator with a duty cycle of 45 to 55%.
–REFRESH	157	IO-OD	Memory Refresh - Whenever a refresh cycle is initiated, this signal is pulled low. An external bus master activates this signal when it requires a refresh cycle from the refresh controller. The internal refresh controller activates this line every 15.6 µs to prevent loss of DRAM data. –REFRESH is an open drain output capable of sinking 24 mA and requires an external pull-up resistor.
RSTDRV	173	O	Reset - This active high output is system reset generated from the POWERGOOD input. RSTDRV is synchronized to the BUSOSC input. On reset, this signal remains high for at least as long as the RESCPU signal. It may therefore be used to drive the 486 AHOLD input to initiate a 486 self-test sequence on power-up reset only.
SA1, SA0	149, 150	IO	System Address bus bits 1 and 0 - These two signals represent the lower two bits of the system address bus. They act as inputs when an external bus master is in control (HLDA = 1, –MASTER = 0) and are outputs at all other times. When HLDA is low, SA1 and SA0 are generated by decoding the CPU byte enables (–BE3 - –BE0). They are driven by the 82C37A DMA controllers during DMA transfer cycles. SA0 is always connected directly to the ISA bus. SA1 is connected to the ISA bus if discrete SA buffers are used. If the VL82C113A I/O Combination chip is used, then SA1 is connected only to the A1 input of the VL82C113A (which then drives the ISA bus SA1 signal). The –IGNNE signal is used to set SA1's timing at power-on reset for use with/without the VL82C113A.
–SBHE	171	IO	System Byte High Enable - An active low signal that indicates valid data is on the upper byte of the system data bus (SD15-SD8). Its functionality is similar to that of the SA1 and SA0 signals. –SBHE is forced low during 16-bit DMA cycles and is the complement of SA0 during 8-bit DMA cycles.
SD15-SD0	184-186, 188-192, 194-201	IO	System Data Bus bits 15 through 0 - These bidirectional signals are directly connected to the slots.
–SMEMR –SMEMW	174 176	O O	System Memory Read System Memory Write These outputs are active during memory read and write cycles, respectively, when the address is below 1 MB. Both pins require an external 10 kΩ pull-up resistor.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Pin Type	Signal Description
SYSCLK	175	O	System Clock - The SYSCLK output is 1/2, 1/3, 1/4, 1/6, or 1/8 the frequency of TCLK2 or BUSOSC depending on the BUSOSC pin's status and the five lower bits in the CLKCTL Register. The bus control signals BALE, –IOR, –IOW, –MEMR and –MEMW are synchronized to SYSCLK.
TC	159	O	Terminal Count - This active high output indicates that one of the DMA channels has transferred all data.
–WS0	154	I	Wait State Terminate - An active low input that indicates a shorter access cycle. It is pulled low by a peripheral on the slot bus to terminate a CPU controlled bus cycle earlier than the default values defined internally on the chip.
POWER AND GROUND PINS			
VSS	16, 28, 52, 60, 77, 90, 104, 115, 132, 138, 156, 168, 187, 208	GND	Ground connection, 0 volts.
VDD	22, 33, 64, 96, 109, 141, 172, 193	PWR	Power connection, nominally +5 volts. These pins should each have 0.1 µF bypass capacitors.

Note 1: These pins are inputs only during POR (power-on reset.)

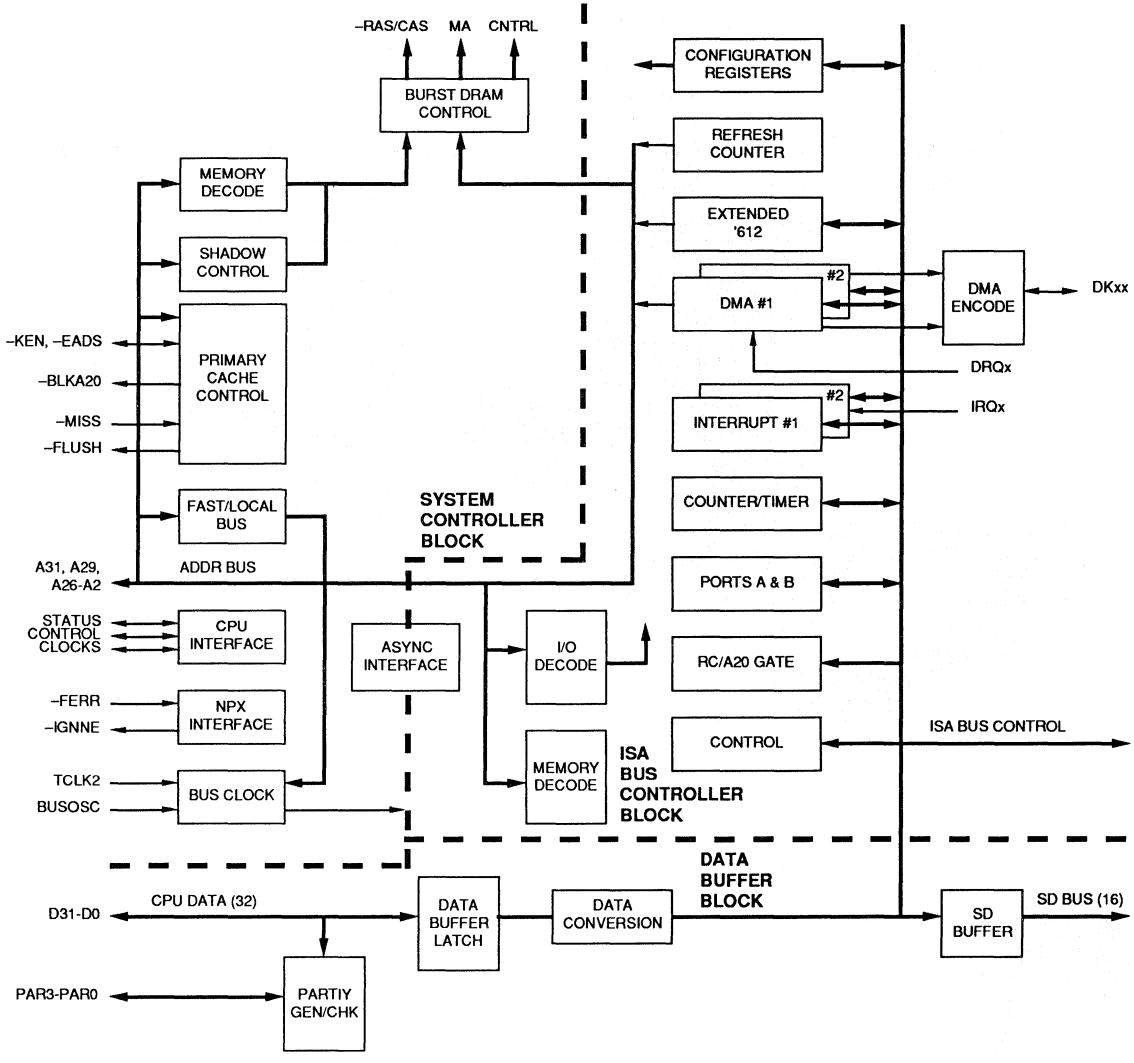
FUNCTIONAL DESCRIPTION

The VL82C486 can be divided into three main blocks:

- System Controller Block - Includes the clock generation, the CPU interface, the numeric coprocessor interface, the address decoder and the memory controller.
- ISA Bus Controller Block - Includes the dual DMA controllers (82C37A), dual programmable interrupt controllers (82C59A), the programmable interval timer (82C54), the ISA sequencer, and the logic for refresh generation and refresh/DMA arbitration.
- Data Buffer Block - Contains the latching and steering logic necessary to convert 32-bit CPU bus cycles to 8/16-bit ISA bus cycles. This block also contains the parity generation and checking logic.

The sections following cover detailed information for the various logical groupings of the VL82C486's subsystems (see Figure 1). In most cases, the effect of configurable elements that can be controlled via I/O registers is discussed at length.

FIGURE 1. VL82C486 SUBSYSTEMS



CPU INTERFACE

OVERVIEW

The VL82C486 System Controller is responsible for decoding local (486) bus requests from the CPU (or other local bus master), initiating the requested action, and responding in the manner required by the 486 bus protocol.

The VL82C486 responds to all 486 generated bus cycles except when the following conditions apply:

- The –MISS input is high during the first T2 of a memory read, indicating a cache-hit. The external cache controller then has the responsibility for completing the local bus cycle.
- The –LBA input is low during the first T2 of a memory or I/O read or write, indicating a local bus access. A local bus slave then has the responsibility for completing the local bus cycle.
- The CPU address maps to a local bus area as defined by address bits A31 and A29, or by the Programmed Memory Region Registers (PMRs). Again, a local bus slave then has the responsibility for completing the local bus cycle.

In all other cases, the VL82C486 generates either an on-board DRAM cycle, an ISA bus cycle, an interrupt acknowledge cycle, or a special bus cycle. –ADS, M/–IO, D/–C, W/–R, and the address lines are examined by the VL82C486 to determine which type of cycle to generate. All I/O accesses, and all memory accesses not directed to on-board DRAM, cause ISA bus cycles to be generated.

BUS CYCLE DECODER

Table 1 shows how the VL82C486 decodes the CPU's status signals when the CPU requests a bus cycle. The VL82C486 responds to each one of these codes according to the descriptions in the following sections.

Interrupt Acknowledge
When this cycle is detected, the VL82C486 generates a special-case ISA bus access cycle that is similar to a regular access cycle except that instead of generating an external command signal, an internal "INTA" command is sent to the on-chip 82C59A interrupt controllers. This causes them to place an interrupt vector on D7-D0 and SD7-SD0 on every second interrupt acknowledge cycle generated by the CPU. The first in a pair of interrupt acknowledge cycles is used by the 82C59As to resolve interrupt priority.

The VL82C486 asserts –RDY after the vector supplied by the 82C59As is placed on the CPU data bus.

Special Bus Cycle: Shutdown
Upon detection of a Shutdown cycle, –RDY is asserted in the second T2 of the bus cycle. Then after a delay of four bus cycles, the RESCPU signal is asserted for 16 CPU clocks.

Special Bus Cycle: Flush
Upon detection of a Flush instruction, both –FLUSH and –RDY are asserted in the second T2 cycle. No other action occurs.

Special Bus Cycle: Halt
Upon detection of a Halt cycle, –RDY is generated in the second T2 of the bus cycle. No other action occurs.

Special Bus Cycle: Write-back
Upon detection of a Write-back operation, the CPU generates –RDY in the second T2 of the bus cycle. No other action occurs.

I/O Read/Write
All I/O accesses that are not inhibited by the –LBA pin are passed to the ISA Bus Controller Block and are executed as standard ISA bus cycles. The VL82C486 steers the data between the CPU data bus and the ISA SD bus as required by each type of cycle. If the access is to an on-chip I/O location, then the VL82C486 steers data between the D bus, the SD bus, and the selected internal location as required by the cycle type.

The VL82C486 asserts –RDY on completion of all ISA bus accesses. In the case of I/O reads, valid data is placed on the CPU data bus before –RDY is asserted. The CPU is held throughout the duration of both ISA bus reads and writes.

For 32- or 24-bit CPU accesses to 16-bit ISA bus locations, or for 32-, 24-, or 16-bit CPU accesses to 8-bit ISA bus locations, the VL82C486 generates multiple ISA bus cycles for each CPU bus cycle in order to match the size of the access requested by the CPU. This process is invisible to the System Controller Block, except for the increased latency required to complete the operation.

TABLE 1. BUS CYCLE DECODE

M/–IO	D/–C	W/–R	Function
0	0	0	Interrupt Acknowledge
0	0	1	–BE3 - –BE0 = 1110 - Shutdown –BE3 - –BE0 = 1101 - Flush –BE3 - –BE0 = 1011 - Halt –BE3 - –BE0 = 0111 - Write-back
0	1	0	I/O Read
0	1	1	I/O Write
1	0	0	Code Read
1	0	1	Not Used
1	1	0	Memory Read
1	1	1	Memory Write

Code Read
Code fetches are handled exactly like any other memory read cycle (see "Memory Read/Write" below).

Memory Read/Write
Memory accesses that are not inhibited by either the –LBA pin, the –MISS pin, or the Programmed Memory Region Registers (PMRs) are directed towards either on-board DRAM or the ISA bus. Selection between on-board DRAM and the ISA bus is made by the address decoder and is described in the section titled "I/O and Memory Mapping" on page 22.

For on-board DRAM reads and writes, the VL82C486 always assumes that burst cycles are to be generated and returns –BRDY in response to each double-word (DWord) returned. –BLAST is monitored to determine when a burst read is to be terminated.

ISA bus memory read or write cycles operate in much the same way as ISA bus I/O read or write cycles (see above), with the exception that there are no on-chip ISA bus memory locations.

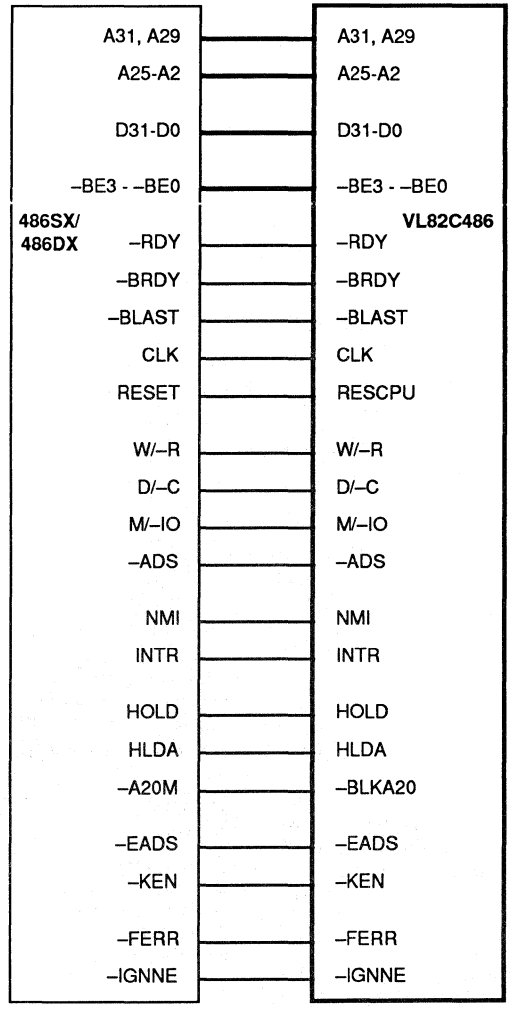
BYTE ENABLES (–BE3 - –BE0)
For all cacheable memory read cycles to both the on-board DRAM and ISA bus, the VL82C486 ignores the byte enables generated by the 486 and acts as if they were all active, thus always generating 32-bit DRAM and ISA bus read accesses. This is in accordance with the 486 cache line fill operation, which always expects 32 bits of valid data when –BRDY is asserted.

For non-cacheable memory read cycles (when –KEN is deasserted by the VL82C486), for all write cycles, and for all I/O cycles, the byte enables are used to generate an access cycle of the requested size to the ISA bus or on-board DRAM.

READY CONTROL
The VL82C486 generates –BRDY for all DRAM cycles and –RDY for all other types of cycles. The –BRDY and –RDY output buffers are normally three-stated. The output buffers are enabled only when the VL82C486 drives these signals low, and for one clock cycle after it drives them from low back to high. This protocol allows the –RDY and –BRDY signals to be driven by other local bus devices such as coprocessors and cache controllers.

–RDY and –BRDY are used as inputs to the VL82C486 whenever a CPU cycle is directed to a local bus slave instead of the VL82C486.

FIGURE 2. CPU INTERFACE



PRIMARY CACHE CONTROL
Cacheability Control
Cacheability of memory read data returned to the 486 is controlled by the –KEN signal. The –KEN output is controlled by the following factors:

- The CEN bit (bit 3) in the MISCSET Register.
- The Programmed Memory Region Registers (PMRs).
- The Segment Cacheability Registers (ACBL-FCBL).
- The CPU address.

Access to any on-board DRAM memory area always defaults to cacheable. Access to any other memory area always defaults to non-cacheable. However, default cacheability in the first 128 MB of memory can be overridden by the Segment Cacheability Registers, and the PMR Registers.

When the CEN bit in the MISCSET Register is set to 0, the –KEN output is always deasserted (set high).

When CEN is set to 1, –KEN is always asserted (low) in all CPU T1 and Ti cycles. (See Table 2.) It is deasserted during the first and subsequent T2 cycles of any memory access defined as a non-cacheable local bus access by the PMR Registers, or for any memory access where A31 and A29 = 10 or 01. It is deasserted during the second and subsequent T2 cycles of all non-cacheable ISA bus memory cycles and for on-board DRAM cycles defined as non-cacheable by the Segment Cacheability Registers.

Invalidation Control
The –EADS input to the 486 is asserted by the VL82C486 to perform primary cache invalidation cycles during DMA and Master Mode ISA bus write cycles and during attempted writes to write-protected memory regions as defined by the Segment Cacheability Registers. It is also used to generate repeated invalidations to slow the CPU when the Non-Turbo Mode is selected.

- When the CPU generates a write cycle to an area of memory defined as write-protected by the Segment Cacheability Registers, the VL82C486 asserts –EADS for one CPU clock cycle during the first T2 of the write cycle.
- During DMA or Master Mode cycles, the VL82C486 asserts –EADS for one CPU clock cycle when the ISA bus –MEMW signal is made active.

LOCAL BUS ARBITRATION
The VL82C486 requests mastership of the local bus by asserting the HOLD signal under the following circumstances:

- When an ISA bus device requests a DMA or Master Mode cycle by asserting one of the –DREQ signals.
- When the VL82C486's internal refresh counter requests a refresh cycle, and the Refresh Mode is not "decoupled".

The VL82C486 waits until the 486 asserts HLDA before taking ownership of the local bus. It deasserts HOLD at the end of the DMA, Master Mode, or refresh cycle.

NUMERIC COPROCESSOR SUPPORT
Numeric Error Reporting for 486DX and 487SX
The VL82C486 reports 486DX/487SX floating point errors through the use of two signals, –FERR and –IGNNE.

–FERR is asserted by the 486 when a floating point error is detected. A high-to-low transition on this signal causes a level-13 interrupt request to be asserted. The request is cleared on an I/O write to location xF0 (Coprocessor Busy Clear) or xF1 (Coprocessor Reset).

–IGNNE is normally inactive (high). It is made active (low) on an I/O write to location xF0 (Coprocessor Busy Clear) or xF1 (Coprocessor Reset); this allows normal execution of floating point instructions within a floating point error handling routine. –IGNNE is deactivated on a low-to-high transition of –FERR.

Weitek Coprocessor Support
The Weitek 4167 is supported via the WEIRQ input, which is connected to the INTR output of the 4167 and causes a level-13 interrupt (IRQ13) to be generated when high. The Weitek 4167 occupies the C0000000-CFFFFFFF address region; the VL82C486 therefore does not respond to accesses in this range, which it detects by looking for a high level on address input A31, and a low on address input A29.

The VL82C486 supports a –RDY time-out mechanism for accesses to the Weitek address space (A31 = 1 and A29 = 0). For the first access after power-on reset to this region, the VL82C486 asserts –RDY after 7 µs if no externally generated –RDY is detected. However, if an externally generated –RDY is detected during the first access to this address space after reset, then the time-out mechanism for this address space is disabled.

CPU RESET
The VL82C486 generates a CPU reset by asserting RESCPU in response to one of the following conditions:

- A low level on the POWERGOOD signal. RESCPU is deactivated when POWERGOOD goes high.
- When bit 0 of I/O Port 92h is set to a 1 or a dummy read of I/O Port EFh is made. In either of these two cases, the VL82C486 waits 6.72 µs from

TABLE 2. MISCSET REGISTER (07h), CACHE CONTROL BIT

Bit	Name	Function
3	CEN	Cache Enable: 0 = Primary cache is disabled, –KEN is forced inactive (high). 1 = Primary cache is selectively enabled, –KEN is controlled by PMRs, Segment Registers, and address decoder. (POR default = 0.)

completion of the I/O operation to asserting RESCPU. RESCPU is made active for 16 CPU clock cycles.

- On writing FCh or FEh to I/O Port 64h. The RESCPU signal is generated after 6.72 µs or about 50 µs, depending on the FASTRC bit of the MISCSET Register. RESCPU is made active for 16 CPU clock cycles.
- On execution of the CPU Shutdown command. RESCPU is made active for 16 CPU clock cycles.
- When the CPU clock speed is changed. RESCPU is made active for 1 ms.

On CPU reset, the VL82C486 forces the –BLKA20 signal inactive until the first memory read with A31 = 0 (this is to ensure correct reset vector operation).

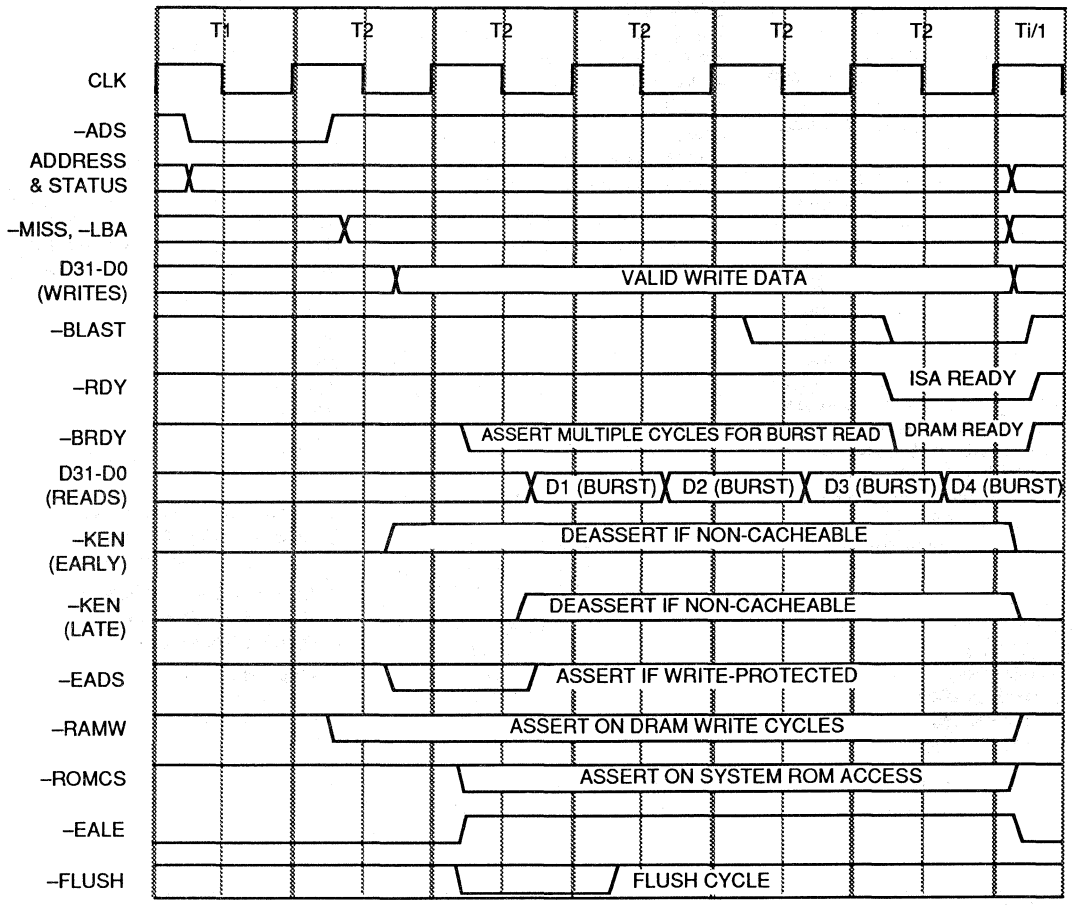
CPU SELF-TEST REQUEST

The CPU self-test request can be generated at system reset by connecting the RSTDRV signal to the AHOLD input of the 486. At the end of a system reset, the VL82C486 guarantees that RSTDRV is active for two CPU clocks longer than RESCPU, thus activating the 486's internal self-test procedure.

This adds 42 ms (at 25 MHz) to the CPU reset time. At the end of the self-test, the BIOS can read the CPU Self-Test Result Registers and perform whatever function is desired on failure.

Note that when using this method there is no self-test performed when a CPU-only reset is invoked. This results in the faster execution of a "Hot Reset".

FIGURE 3. CPU INTERFACE TIMINGS



I/O AND MEMORY MAPPING

OVERVIEW

The VL82C486 decodes CPU addresses to determine the destination of a CPU memory or I/O request. The VL82C486's address decoder distinguishes seven general regions for memory or I/O accesses. The region selected is a function of the CPU address, the CPU cycle type, and the values placed in the Configuration Registers that control memory mapping. The regions are:

- ISA Bus I/O Location, On-chip: An ISA bus I/O access cycle is generated and is responded to by the VL82C486 when it recognizes an on-chip address during the ISA bus cycle.
- ISA Bus I/O Location, Off-chip: A standard ISA bus I/O access cycle is generated. Data is passed between the local data bus (D31-D0) and the ISA data bus (SD15-SD0). –PPICS is asserted to select the keyboard controller/real-time clock if the I/O address is 60h, 64h, 70h, or 71h.
- ISA Bus Memory Location, Off-board: Standard 8- or 16-bit ISA bus cycles are generated when the VL82C486 detects a CPU memory access as being in the ISA slot bus address range. Data is passed between the local data bus (D31-D0) and the ISA data bus (SD15-SD0).
- DRAM Location, On-board: If a CPU memory access in the on-board DRAM range is detected, then the DRAM controller is selected and generates the requested DRAM cycle. The ISA bus is not affected.
- Local Bus ROM Location: Standard 8- or 16-bit ISA bus cycles are generated when the VL82C486 decodes a CPU memory access as selecting local bus ROM space. On read cycles, the VL82C486 latches ROM data from the local data bus and then redrives the data back to the CPU on the required portion of the local data bus. The –ROMCS signal is generated to enable the local bus ROM outputs. On local bus ROM writes, standard ISA bus memory write cycles are generated.
- Local Bus Peripheral Memory Location: The Programmed Memory Region Registers may be set to select local bus peripheral memory within a selected address range. In such cases, the VL82C486 is deselected to allow a local bus slave to respond to the CPU access cycle.
- Fast Bus Clock Region: If the address range falls within that defined by the Fast Bus Clock Register (FBCR) and the access is to an ISA bus memory location, then the fast bus clock divider is used to control SYSCLK speed during the ISA bus cycle.

  If the –LBA pin is assisted by a local bus device, the VL82C486 will be deselected, thus overriding any of the above memory/IO maps and allowing the local bus device to respond.

I/O MAPPING

I/O accesses are always run as ISA bus cycles, but the data steering is based on the actual I/O address depending on whether the I/O location is on-chip or off-chip. The VL82C486 provides an option in the BUSCTL Register to perform either 10- or 16-bit decodes for the resources listed in Table 4. I/O addresses explicitly decoded by the VL82C486 are shown in bold. In 10-bit mode, A15-A10 are ignored.

On-Chip I/O

For on-chip devices, the ISA bus cycle is run normally; only the data steering on read cycles is affected. bus masters have access to all on-chip registers, but DMA to on-chip I/O is not supported.

ISA Bus I/O

All I/O write cycles drive the data onto the SD bus and generate an –IOW strobe. All I/O read cycles generate an –IOR strobe and drive data onto the D bus. Data is driven onto the SD bus during all on-chip I/O reads while the SD bus sources the data for all other I/O reads.

10/16 Address Decode

The 10/16-bit I/O address decode is controlled by bit 6 (10/16IO) in the BUSCTL Register (at indexed location 09h) as shown in Table 3. See Table 25 for a complete description of the of the BUSCTL Register.

TABLE 3. BUSCTL REGISTER (09h), ADDRESS DECODE CONTROL BIT

Bit	Name	Function
6	10/16IO	10/16-Bit I/O Address Decode: When 0, full 16-bit address decode is performed. When set, 10-bit I/O decode is performed. The default value of this bit at power-on reset is 0.

TABLE 4. I/O ADDRESSING MAP

Address (Hex)	Device	Location	Address (Hex)	Device	Location
0000-00F	DMA #1	On-chip	**00C0-00DE**	DMA #2	On-chip
0020-003F	Interrupt Controller #1	On-chip	00E0-00EB	Not Used	ISA Bus
0040-0043	Counter/Timer	On-chip	**00EC**	Configuration Index	On-chip
0044-005F	Not Used	ISA Bus	**00ED**	Configuration Data	On-chip
0060	Keyboard Controller	ISA Bus, –PPICS	**00EE*+**	Fast A20	On-chip
0061	Port B	On-chip	**00EF*+**	Fast Reset	On-chip
0062-0063	Not Used	ISA Bus	**00F0****	Coprocessor Busy Clear	On-chip
0064	Keyboard Controller	ISA Bus, –PPICS	**00F1****	Coprocessor Reset	On-chip
0065-006F	Not Used	ISA Bus	00F2-00F3	Not Used	ISA Bus
0070, 0071	NMI Enable, Real-Time Clock	ISA Bus, –PPICS	**00F4+**	Slow CPU	On-chip
0072-007F	Not Used	ISA Bus	**00F5+**	Fast CPU	On-chip
0080-008F	DMA Page Registers	On-chip	00F6-00F8	Not Used	ISA Bus
0090-0091	Not Used	ISA Bus	**00F9**	Configuration Protect	On-chip
0092	Port A	On-chip	00FA+	Not Used	ISA Bus
0093-009F	Not Used	ISA Bus	**00FB+**	Configuration Unprotect	On-chip
00A0-00BF	Interrupt Controller #2	On-chip	00FC-00FF	Not Used	ISA Bus
			0100-FFFF	General I/O Locations	Local or ISA Bus

Notes: I/O addresses shown in bold are explicitly decoded by the VL82C486.
* Can also be activated via Port A.
** For compatibility, used only to set –IGNNE.
\+ Can be disabled via BUSCTL.

MEMORY MAPPING

Memory accesses are divided into on-board DRAM, local ROM, and ISA bus memory accesses. Since address bits A30, A28, and A27 are not used in the decode, many areas of the map are duplicated.

A31 and A29 are used to define four areas in the memory map. When A31 and A29 = 00, normal memory accesses are in effect. When A31 and A29 = 01 or 10, the VL82C486 is deselected and the local bus slaves may use these areas. When A31 and A29 = 11, aliased ISA bus space and BIOS ROM are selected.

A non-cached aliased ISA bus area is provided at the top of memory to allow limited access to ISA memory devices in the 1 MB to 16 MB ISA bus address range while still supporting a full 16 MB of on-board DRAM in the first 16 MB of CPU address space. However, DMA and Master Mode cycles to the ISA memory areas in such configurations are not permitted, since conflicts with on-board DRAM would arise.

TABLE 5. MEMORY ADDRESS MAPPING

Range	A31, A29	CPU Address	Destination	Comments
0-640K	0, 0	00000000-0009FFFF*	Local DRAM	Cached
640K-768K	0, 0	000A0000-000BFFFF*	ISA Memory Local DRAM	Normal Shadow
768K-832K	0, 0	000C0000-000CFFFF*	ISA Bus System ROM Local DRAM	Normal Relocated Slot ROM Shadow
832K-896K	0, 0	000D0000-000DFFFF*	ISA Bus Local DRAM	Normal Shadow
896K-1M	0, 0	000E0000-000FFFFF*	System ROM ISA Memory Local DRAM	Normal Relocated System ROM Shadow
1M-(16M-128K)	0, 0	00100000-00FDFFFF*	Local DRAM ISA Memory	Memory Map, Cached No DRAM, Non-Cached
(16M-128K)-16M	0, 0	00FE0000-00FFFFFF*	System ROM Local DRAM ISA Memory	Mid BIOS, Non-Cached No Mid BIOS, Cached No DRAM/BIOS, Non-Cached
16M-64M	0, 0	01000000-03FFFFFF*	Local DRAM Nothing Mapped	Memory Map, Cached No DRAM, 7 µs Time-Out
64M-128M	0, 0	04000000-07FFFFFF*	Nothing Mapped	No DRAM, 7 µs Time-Out
128M-0.5G	0, 0	08000000-1FFFFFFF	Alias 1st 128M x 3	Not Useful
1.0G-1.5G	0, 0	40000000-5FFFFFFF	Alias 1st 128M x 4	Not Useful
0.5G-1.0G	0, 1	20000000-3FFFFFFF	Nothing Mapped	VL82C486 Deselected, 7 µs Ready Time-Out, Non-Cached
1.5G-2.0G	0, 1	60000000-7FFFFFFF	Nothing Mapped	VL82C486 Deselected, 7 µs Ready Time-Out, Non-Cached
2.0G-2.5G	1, 0	80000000-9FFFFFFF	Nothing Mapped	VL82C486 Deselected, Conditional Ready Time-Out, Non-Cached
3.0G-3.5G	1, 0	C0000000-DFFFFFFF	Nothing Mapped	VL82C486 Deselected, Conditional Ready Time-Out, Non-Cached
2.5G-3.0G	1, 1	A0000000-BFFFFFFF	Aliased ISA Bus/ System ROM	Non-Cached
3.5G-(4.0G-16M)	1, 1	E0000000-FEFFFFFF	Aliased ISA Bus/ System ROM	Non-Cached
Top 16M	1, 1	FF000000-FFFDFFFF	Aliased ISA Bus	Non-Cached
Top 128K	1, 1	FFFE0000-FFFFFFFF	System ROM	Normal, Non-Cached

* The Programmed Memory Region Registers may be used to define any area in the lower 128 MB as local bus memory or ISA bus memory, cacheable, or non-cacheable.

Local DRAM
Memory addresses generated by the CPU are compared against the currently defined memory map. If the address is in an area defined by Table 5 and the Memory Mapping Registers as on-board DRAM, then the DRAM controller is activated and generates the requested DRAM cycle. Parity is optionally checked in this area.

Accesses to on-board DRAM areas are always cacheable unless overridden by the Segment Cacheability Registers, or the PMR Registers.

Shadow RAM
There are six Configuration Registers that allow any 16K block in the 640K-1M range to be directed to either on-board DRAM or ISA bus memory/local ROM. These registers contain two control bits for each block that allows local ROM or ISA bus ROM to be copied to local DRAM for faster access. These bits also allow a block to be defined as normal read/write DRAM. DRAM in this 384K area that is not used for Shadow RAM is not accessible to the system. Shadow RAM is also accessible by bus masters and DMA cycles. Parity is optionally generated and checked in this area only when local DRAM is accessed.

Registers AAXS, BAXS, CAXS, DAXS, EAXS, and FAXS are used to define the shadow area mapping. They are Indexed Configuration Registers and are accessed via the Index and Data Ports at I/O addresses ECh and EDh. Table 6 shows their format and index address.

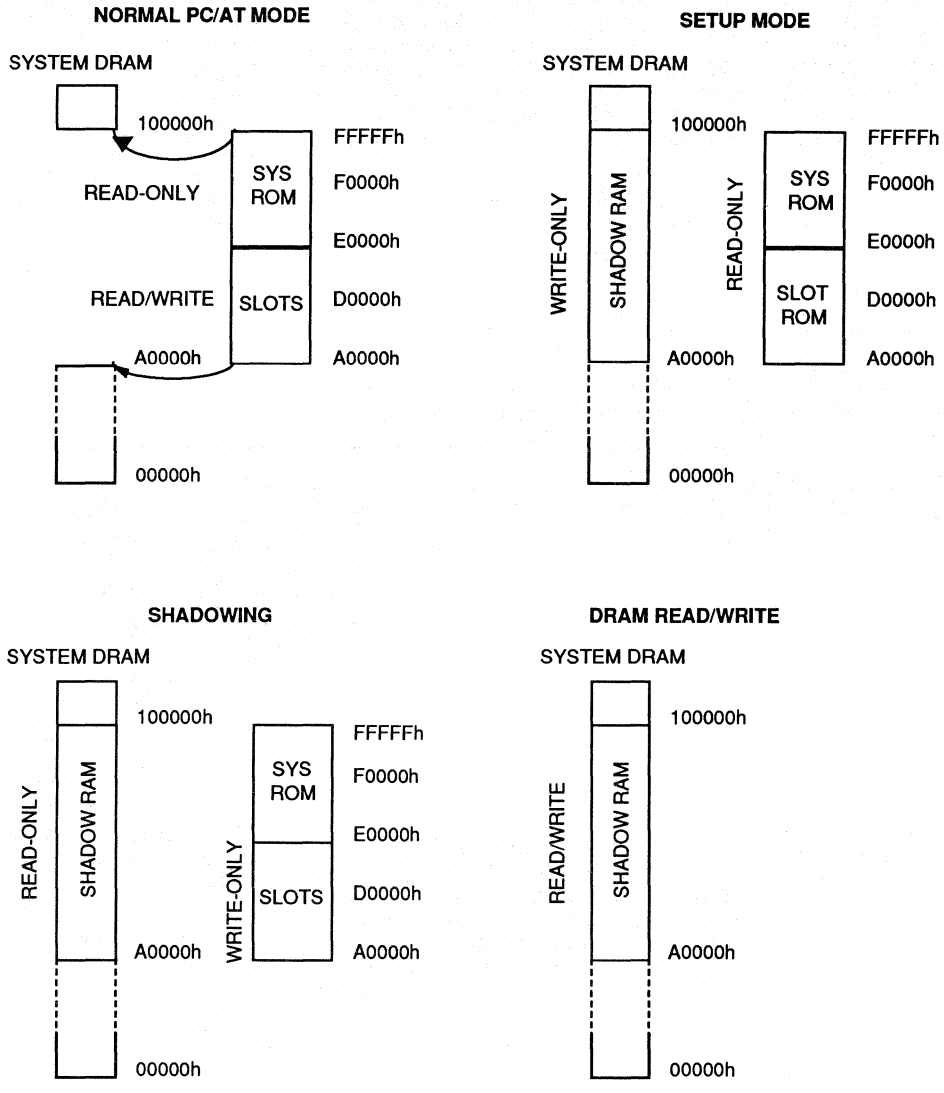
TABLE 6. SHADOW RAM SEGMENT CONTROL REGISTERS (0Dh-12h)
STARTING ADDRESS (A19-A0) OF EACH 16 KB REGION (A31, A29, A26-A20 = 0)

Data Port EDh	D7 D6	D5 D4	D3 D2	D1 D0
AAXS (0Dh)	AC000 Access	A8000 Access	A4000 Access	A0000 Access
BAXS (0Eh)	BC000 Access	B8000 Access	B4000 Access	B0000 Access
CAXS (0Fh)	CC000 Access	C8000 Access	C4000 Access	C0000 Access
DAXS (10h)	DC000 Access	D8000 Access	D4000 Access	D0000 Access
EAXS (11h)	EC000 Access	E8000 Access	E4000 Access	E0000 Access
FAXS (12h)	FC000 Access	F8000 Access	F4000 Access	F0000 Access
POR Value	0 0	0 0	0 0	0 0

The two bits for each segment select four modes as follows:

1. 00 *Read/Write Slot Bus (Default)*
   Normal PC/AT compatible operation. This may select local ROM or ISA bus ROM, depending on the memory space configuration.
2. 01 *Setup Mode: Read Slot Bus/ Write System Board*
   Shadow setup mode. In this mode, reads are from the slot bus (or local ROM) and writes are to on-board DRAM. ROM chip selects may be generated, depending on how the ROMSET Register is configured. This allows shadowing of system board ROM as well as ROMs on a slot bus card.
3. 10 *Shadow Mode: Read System Board/Write Slot Bus*
   Read-only DRAM. This is the normal shadow operational mode. In this mode, reads are from the on-board DRAM and writes are directed to the slot bus. This mode could also be used to protect data previously written to a memory area while configured for Mode 4 (below).
4. 11 *Read/Write System Board*
   Read/write System board DRAM. This allows complete access to DRAM in the given 16K region.

FIGURE 4. SHADOW RAM CONTROL



Segment Cacheability Registers
There are six Configuration Registers that allow any 16K block in the 640K-1M range to be marked as non-cacheable or write-protected. Write-protection is used to prevent the 486 from writing into its primary cache at locations defined as ROM or shadow Rom areas. It can not be used to write-protect DRAM areas - the Shadow RAM Control Registers are used for this purpose. The VL82C486 detects writes to protected areas and drives –EADS during the first T2 of the CPU write cycle to invalidate the corrupted primary cache location.

Registers ACBL, BCBL, CCBL, DCBL, ECBL, and FCBL are used to define the Segment Cacheability. They are Indexed Configuration Registers and are accessed via the Index and Data Ports at I/O addresses ECh and EDh. Table 7 shows their format and index address.

TABLE 7. SEGMENT CACHEABILITY REGISTERS (13h-18h)

STARTING ADDRESS (A19-A0) OF EACH 16 KB REGION (A31, A29, A26-A20 = 0)

Data Port EDh	D7 D6	D5 D4	D3 D2	D1 D0
ACBL (13h)	AC000 Access	A8000 Access	A4000 Access	A0000 Access
BCBL (14h)	BC000 Access	B8000 Access	B4000 Access	B0000 Access
CCBL (15h)	CC000 Access	C8000 Access	C4000 Access	C0000 Access
DCBL (16h)	DC000 Access	D8000 Access	D4000 Access	D0000 Access
ECBL (17h)	EC000 Access	E8000 Access	E4000 Access	E0000 Access
FCBL (18h)	FC000 Access	F8000 Access	F4000 Access	F0000 Access
POR Value	0 0	0 0	0 0	0 0

The two bits for each segment select four modes are as follows:

1. 00 *Not Write-protected, Cacheable*
2. 01 *Not Write-protected, Not Cacheable*
3. 10 *Write-protected, Cacheable*
4. 11 *Write-protected, Not Cacheable*

Programmed Memory Region Registers
There are two pairs of registers, (PMRA1, PMRE1 and PMRA2, PMRE2) that allow any region in the first 128 MB of memory space to be remapped from its normal default to become either ISA bus address space or local bus address space. The selected address space may also be defined as cacheable or non-cacheable, overriding the default cacheability.

Regions from 2 KB up to 8 MB in size may be selected by the PMRs.

Table 8 shows the format of the registers and the operation of each bit field.

PMRA is used to define the region type (mapping, size, and start address), and PMRE is used to divide the selected region into eight equally-sized contiguous sub-regions, each one of which can be selectively enabled for remapping.

TABLE 8. PROGRAMMED MEMORY REGION REGISTER (20h-23h)

Data Port	EDh	D7	D6	D5	D4	D3	D2	D1	D0
PMRA1	(20h)	LBA_ISA	NCBL	AX5	AX4	AX3	AX2	AX1	AX0
PMRE1	(21h)	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0
PMRA2	(22h)	LBA_ISA	NCBL	AX5	AX4	AX3	AX2	AX1	AX0
PMRE2	(23h)	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0
POR Value		0	0	0	0	0	0	0	0

PMRA

Bit	Name	Function
7	LBA_ISA	Selects the type of region: 0 = Select all memory accesses in the region to generate ISA bus cycles. 1 = Select all memory accesses in the region to access a local bus device. The VL82C486 is deselected on CPU accesses in the region, and generates local bus cycles on DMA/Master Mode accesses to the region to access the local bus device.
6	NCBL	Sets the cacheability of the region: 0 = Region is cacheable. 1 = Region is non-cacheable.
5-0	AX5-AX0	Selects the start address and size of the memory region as follows:

AX5	AX4	AX3	AX2	AX1	AX0	
0	A23	A22	A21	A20	A19	A23-A19 selects a 512 KB region in the first 16 MB of memory, aligned on a 512 KB boundary.
1	0	A26	A25	A24	A23	A26-A23 selects an 8 MB region in the first 128 MB of memory, aligned on an 8 MB boundary.
1	1	A17	A16	A15	A14	A17-A14 selects a 16 KB region in the address range C0000h-FFFFh (768K-1M) aligned on a 16 KB boundary.

PMRE

Bit	Name	Function
7-0	RE7-RE0	Sub-Region Enables: These bits enable the region selected by PMRA for remapping and/or cacheability. The region selected by PMRA is divided into eight equally sized contiguous sub-regions, each with its own enable, RE7-RE0. RE0 controls the sub-region with the lowest address. For 8 MB regions the sub-region size is 1 MB. For 512 KB regions the sub-region size is 64 KB. For 16 KB regions the sub-region size is 2 KB. Any combination of RE7-RE0 may be set. Operation is as follows: REx = 0: Default mapping/cacheability is selected. REx = 1: Sub-region mapping/cacheability is enabled as defined by PMRA.

The PMR Registers override the default mapping and cacheability of any region they select, including that set by the Segment Control Registers. If a memory region is under control of the Segment Cacheability or PMR Registers and these registers overlap, any non-cacheable region takes presedence.

Regions above 16 MB that are defined as ISA bus address space alias to the 16 MB ISA bus address space. No DMA or Master Mode cycles can be performed to aliased ISA bus areas, since the on-board DRAM and ISA memory could be mapped to the same ISA bus address space.

ISA Memory
All memory accesses below 16 MB that are not directed to local DRAM, shadowed areas, or local bus devices are directed to the ISA bus. Also, the PMR Registers may be used to define any area in the first 128 MB as mapped to the ISA bus. Standard ISA cycles are generated. The VL82C486 provides the data latching and steering logic to allow the CPU to perform 8, 16, 24, or 32 accesses to either 8- or 16-bit ISA memory devices. Parity is not generated or checked in this area.

Accesses to the ISA bus defined by the PMR Registers between 16 MB and 128 MB alias to the 24-bit ISA bus addresses. CPU accesses in this region should be performed only if no DMA or Master Mode cycles ever access the referenced locations, since if a slot bus memory device occupied the same (aliased) address as the on-board DRAM, bus contention would occur if the DMA or Master Mode cycles were attempted to that area.

Access to the full 16 MB ISA bus memory space is also provided in the CPU upper address regions (when A31 and A29 = 11). Normal ISA bus memory cycles are generated in this region. For the reasons described above, DMA or Master Mode accesses should not be made to locations referenced by the CPU in this region. Accesses in this region are always non-cacheable.

Access to system ROM is provided in the top 128K of the aliased ISA bus address space for correct reset vectoring.

Accesses to all ISA bus areas default to being non-cacheable. However, any ISA bus area may be redefined as cacheable using the PMR Registers.

SYSTEM ROM MEMORY MAPPING
Configuration
System ROM accesses are defined to be all CPU accesses in the F0000h to FFFFFh address range that are not remapped by the Segment Control or the PMR Registers. Accesses in the C0000h to CFFFFh and E0000h to EFFFFh address ranges may also be defined by the ROMSET Register as system ROM accesses (if not remapped by the Segment Control or PMR Registers).

System ROM accesses are a subset of ISA bus accesses. Standard ISA bus access cycles are generated on system ROM accesses, with the only differences being:

- –ROMCS is always asserted on system ROM accesses.
- System ROM may be selected to reside on either the local D bus or the ISA SD bus.
- Additional ISA bus wait states may be programmed for system ROM accesses via bits 1 and 0 (ROMWS1 and ROMWS0) in the ROMSET Register.

The VL82C486 provides the data latching and steering logic to allow the CPU to perform 8-, 16-, 24-, or 32-bit accesses to either 8- or 16-bit system ROMs.

In 8-bit mode, the ROM is addressed by SAxx-SA0 and the ROM physically resides on the next-to-high order byte (D23-D16) of the CPU data bus, or the low order byte of the SD bus. In 16-bit mode, ROM is addressed by SAxx-SA1 and physically resides on the high order word (D31-D16) of the CPU data bus, or all 16 bits of the SD bus.

The VL82C486 performs the required ISA bus cycles to assemble and latch the appropriate data and to present it to the CPU as requested. The DKEN pin is strobed at power-up to determine the ROM size (low = 8-bit, high = 16-bit), and the –RAMW pin is strobed at power-up to determine whether the system ROM resides on the local D or ISA SD data bus (low = D bus, high = SD bus). System ROM is also accessible by bus masters and DMA cycles. Parity is not checked in this area.

ROM Relocation
The video ROM and the fixed disk ROM, memory range C0000h to CFFFFh, can be defined to be in the system ROM range with the ROMMOV1 and ROMMOV0 bits (bits 5 and 4, respectively) in the ROMSET Register. Similarly, the memory range E0000h to EFFFFh can be defined as system ROM by the same bits. All system ROM may be defined by the ROMMOV2 bit (bit 6) of the ROMSET Register to reside either on the local D bus or ISA SD bus. Accesses to system ROM causes the –ROMCS signal to be asserted.

Table 9 shows the full decode of the ROMMOV2 through ROMMOV0 bits.

TABLE 9. RELOCATION OF SYSTEM AND SLOT ROM

ROMMOV2-ROMMOV0	000	001	010	011	100	101	110	111
E8000h-EFFFFh	D Bus, ROMCS	Slots	Slots	Slots	SD Bus, ROMCS	Slots	Slots	Slots
E0000h-E7FFFh	D Bus, ROMCS	Slots	Slots	Slots	SD Bus, ROMCS	Slots	Slots	Slots
C8000h-CFFFFh (Fixed Disk ROM)	Slots	Slots	Slots	D Bus, ROMCS	Slots	Slots	Slots	SD Bus, ROMCS
C0000h-C7FFFh (Video ROM)	Slots	Slots	D Bus, ROMCS	D Bus, ROMCS	Slots	Slots	SD Bus, ROMCS	SD Bus, ROMCS
F0000h-FFFFFh (System BIOS)	D Bus, ROMCS	D Bus, ROMCS	D Bus, ROMCS	D Bus, ROMCS	SD Bus, ROMCS	SD Bus, ROMCS	SD Bus, ROMCS	SD Bus, ROMCS

ROMCS: –ROMCS is asserted on accesses in this region.

D Bus: On-board system ROM resides on the local D bus in this region. –ROMCS is asserted. The number of waits states for ROM accesses are programmed via bits 1 and 0 (ROMWS1 and ROMWS0) of the ROMSET Register.

SD Bus: On-board system ROM resides on the ISA SD bus in this region. –ROMCS is asserted. The number of wait states for ROM acesses is programmed via the bits 1 and 0 (ROMWS1 and ROMWS0) of the ROMSET Register.

Slots: Standard off-board ISA bus cycles are generated in this region. –ROMCS is not asserted. The number of wait states for ROM accesses are programmed via bits 1 and 0 (16WS and 8WS) in the BUSCTL Register.

Note: Any region in Table 9 may be overridden by the Segment Control Registers or the PMR Registers.

Flash Memory Support
Provision is made for programming flash memory when used for the BIOS ROMs. Flash memory programming mode is set by bit 2 (FMPRG) in the ROMSET Register. When bit 2 is set, it causes the –FMPRG signal to be asserted, which may be used to gate a high voltage to the flash memory programming pin. Commands and data may then be sent to the devices to erase, program, or verify them.

System flash memory may reside on either the local data bus or the SD bus. For the case where flash memory resides on the local data bus, 8-bit flash memory can only reside on D23-D16 and 16-bit flash memory on D31-D16. –ROMCS is asserted. A special programming method is required to ensure that data is always presented on D23-D16 for 8-bit ROMs and D31-D16 for 16-bit ROMs, regardless of the state of SA1 and SA0. To guarantee this, byte/word duplication must be performed by the software programming routine as shown in Table 10.

TABLE 10. FLASH MEMORY SOFTWARE PROGRAMMING

Memory Address Conversion	Program Address (A31-A0)	–BE3 - –BE0	Converted ROM Address (SAx-SA1, SA0)	Program Operation
8-Bit ROM on D23-D16	X.....X00	0000	X.....X00	Double Word Write, 4-Byte Duplication
	X.....X01	1001	X.....X01	Word Write, 2-Byte Duplication
	X.....X10	0011	X.....X10	Word Write, Valid Least-Significant Byte
	X.....X10*	1011	X.....X11*	Byte Write
16-Bit ROM on D23-D16	X.....X0-	0000	X.....X0-	Double Word Write, 2-Word Duplication
	X.....X1-	0011	X.....X1-	Word Write

* In this special case, the VL82C486 converts a CPU byte 2 address to a ROM byte 3 address when in flash memory programming mode and the system memory resides on the local data bus. The VL82C486 internal logic provides a way of generating a ROM byte 3 address (SA1 and SA0 = 11), while still allowing the CPU to put out data on D23-D16.

When the system ROM is programmed to reside on the SD bus, normal (special programming mode is disabled) ISA bus write cycles are generated to the flash memory, and SA1 and SA0 are asserted as normal. –ROMCS is asserted if flash memory is programmed via the ROMSET Register to reside on the on-board SD bus. –ROMCS is not asserted if the flash memory is programmed to reside on the off-board slots.

Middle BIOS Switch-Out
The middle BIOS region (at the 16 MB location, 00FE0000h to 00FFFFFFh) is normally enabled. However, it may be disabled by setting bit 3 (MBIOS) in the ROMSET Register, in which case accesses to this address range are directed towards on-board DRAM or ISA bus.

ROM Control Register (ROMSET)
The ROMSET Register controls the ROM width, ROM relocation, number of ROM access wait states, and flash memory programming mode. Table 11 shows the ROMSET Register's format.

TABLE 11. ROMSET CONTROL REGISTER (0Ch) - READ/WRITE

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
ROMSET (0Ch)	ROMWID	ROMMOV2	ROMMOV1	ROMMOV0	MBIOS	FMPRG	ROMWS1	ROMWS0
POR Value	DKEN	–RAMW	0	0	0	0	0	0

Bit	Name	Function
7	ROMWID	ROM Width: Sets BIOS ROM width. 0 = 8-bit, 1 = 16-bit.
6-4	ROMMOV2-ROMMOV0	ROM Move Bits 2 through 0: ROM relocation bits as defined in Table 9 on page 29.
3	MBIOS	Middle BIOS: This bit enables the middle BIOS region (00FE0000h to 00FFFFFFh) when reset to 0. When set to 1, accesses to this range are directed to the on-board DRAM or ISA bus.
2	FMPRG	Flash Memory Program: When set, it forces the –FMPRG output low and enables the special flash memory addressing mode as defined in the section titled "Flash Memory Support" on page 30.
1, 0	ROMWS1, ROMWS0	ROM Wait States: These bits specify the number of ROM wait states defined in terms of slot bus cycles. The valid range is one to three: **Bit 1 / Bit 0 / # of WS** 0 / 0 / 3 0 / 1 / 1 1 / 0 / 2 1 / 1 / 3 These bits are set to 0 at power-on reset.

LOCAL BUS PERIPHERAL SUPPORT

CPU ACCESS TO LOCAL BUS DEVICES

CPU access to local bus devices is supported through programmable and fixed address regions at which the VL82C486 is deselected during memory accesses and by the –LBA pin which forcibly deselects the VL82C486 during memory and I/O accesses.

Fixed Local Bus Memory Regions

The VL82C486 is deselected during a memory access whenever A29 = 1, or whenever A31 and A29 = 10. Hence, local bus devices may respond to CPU memory accesses to regions that generate these A31 and A29 values without interference from the VL82C486.

The VL82C486 does, however, detect accesses to these regions in order to perform the following cacheability and time-out functions:

- –KEN is deasserted during the first and subsequent T2 cycles of accesses to these memory regions to make such accesses non-cacheable.
- For accesses to address regions where A31 and A29 = 01, the VL82C486 asserts –RDY after 7 µs from –ADS, unless before 7 µs it detects –RDY or –BRDY (generated by a local bus device).
- For accesses to address regions where A31 and A29 = 10, the VL82C486 asserts –RDY after 7 µs from –ADS, unless before 7 µs it detects –RDY or –BRDY (generated by a local bus device). If –RDY or –BRDY is detected before 7 µs, the time-out mechanism for these address regions is permanently disabled. This is intended for use with devices such as the Weitek 4167 which can generate very long access cycles, of which the first one after reset is guaranteed to be less than 7 µs and can thus be used by the VL82C486 to verify the presence of the device.

Programmable Local Bus Memory Address Regions

One or two regions in the first 128 MB of memory space may be programmed as being local bus address space by the PMR Registers. Each region may be as small as 64 KB (if it is in the first 16 MB of memory space), or as large as 8 MB. Each region may be defined as cacheable or non-cacheable.

When the VL82C486 is deselected when it detects an access to a programmed local bus memory region. The only action performed by the VL82C486 during an access to a programmed local bus region is to deassert the –KEN signal in the first and subsequent T2 cycles of the access if the region is defined as non-cacheable.

No –RDY time-out is generated for accesses to programmable memory regions.

–LBA Pin

If the –LBA input is asserted (low) during any memory or I/O access, the VL82C486 is deselected. To guarantee deselection of the VL82C486, the –LBA input must meet the following timing requirements:

- If the RAMTMG Register is set such that on-board DRAM cycles start at the beginning of the first T2, then for memory accesses that would normally select an on-board DRAM location, the –LBA pin must be asserted within a setup time to the end of T1 state.
- If the RAMTMG Register is set such that on-board DRAM cycles start in the middle of the first T2, then for memory accesses that would normally select an on-board DRAM location, the –LBA pin must be asserted within a setup time to the negative edge of the CPU clock, in the middle of the first T2.
- For all other types of accesses, the –LBA pin must be asserted within a setup time to the end of the first T2.

The VL82C486 normally forces all CPU accesses that cause the –LBA pin to be asserted to be non-cacheable by deasserting the –KEN signal in the second and subsequent T2 cycles of memory accesses. However, if the memory address that asserts –LBA also falls within the range of a PMR that is programmed to select a cacheable local bus region or a Segment Cacheablity Register that is programmed to select a cacheable region, then –KEN will remain asserted throughout the cycle.

DMA and Master Mode/Local Bus Memory Transfers

The VL82C486 supports DMA and Master Mode cycles between the ISA slot bus I/O devices and local bus memory devices. The mechanism is programmed via the PMR Registers. To support DMA transfers between a slot bus device and a local bus device, a PMR Register must be programmed to select a local bus device for the address range in which such transfers are to occur.

Whenever the HLDA input of the VL82C486 is high, it configures the –ADS, M/–IO, W/–R, D/–C, –BE3 - –BE0, A31, A29, A26-A2, and –BLAST pins as outputs. Then on detection of an active –MEMR or –MEMW signal during a DMA or Master Mode transfer cycle that falls within the range selected by a PMR for local bus accesses, the VL82C486:

- Drives IOCHRDY low on the next negative or positive edge of SYSCLK.
- Sets W/–R high on memory writes or low on memory reads, sets D/–C high, sets M/–IO high, sets –BLAST low, and sets –BE3 - –BE0 according to the decode of SA1 and SA0 and the transfer size (8 or 16 bits).
- After synchronization with the CPU clock, –ADS is asserted for 1T cycle. On memory writes, the contents of the SD bus is driven onto the selected portion of the D bus.
- Waits for –RDY or –BRDY to be returned by the local bus device. For memory reads, –RDY or –BRDY is used to strobe the data returned by the local bus device into a synchronous data register; the output of the data register is placed on the selected portion of the SD bus.
- After synchronization with SYSCLK, IOCHRDY is three-stated to terminate the cycle.

The local bus device's memory locations must be within the first 64 MB of local bus address space for DMA accesses and within the first 16 MB for Master Mode access.

When the local bus access mechanism is used in DMA transfers, the DMA Acknowledge (–DACK) signals, decoded from the M/–IO_DK0, D/–C_DK1, and W/–R_DK2, must be latched externally and enabled when DKEN is active since these signals hold a valid DMA acknowledge code only for a short time after DKEN goes active, before being multiplexed to select the local bus cycle definition.

DRAM CONTROLLER

OVERVIEW

The VL82C486 supports up to 64 MB of on-board DRAM. The DRAM is configured in one to four banks, each with its separate control signals. Each bank is 32 bits wide (without parity) or 36 bits wide (with parity). The size of each bank can be up to 16 MB.

The VL82C486 supports the use of 256Kx1, 256Kx4, 1Mx1, 1Mx4, or 4Mx1 DRAMs. Each of the four banks may consist of one or two rows of DRAMs, for support of single- or double-sided SIMMs.

The DRAMs have a separate address bus (MA10-MA0) that is generated by the VL82C486, but communicate directly with the CPU data bus (D31-D0).

The four banks of DRAMs may be configured in either a single or double memory data bus organization (referred to as Configuration A or Configuration B). Configuration B gives higher performance by permitting Column Address Strobe (CAS) signals to overlap during interleaved DRAM cycles, but require the use of ten 8-bit bidirectional buffers.

DRAM cycles for CPU accesses are generated synchronously with the CPU clock. CPU Burst Mode reads are supported; the VL82C486 is capable of performing up to four 32-bit DRAM accesses on a single CPU read request. Page Mode operation and two- or four-way interleaving are supported. Critical DRAM timing parameters are programmable via the configuration register RAMTMG. It allows the use of different speed DRAMs at various CPU clock frequencies.

DRAM cycles for DMA or Master Mode transfers are generated synchronously with the 14 MHz OSC input, have fixed timing and operate in Non-Page Mode.

Refresh cycles may be set to occur every 15.625 µs or 125 µs. They also have fixed timing and are generated synchronously with the 14 MHz OSC input.

PHYSICAL CONFIGURATIONS

Configuration A

Configuration A is the basic DRAM configuration and is shown in Figure 6. It consists of one to four banks of DRAMs. Each bank is 32 bits wide (or 36 bits wide with parity), and may consist of 256Kx1, 256Kx4, 1Mx1, 1Mx4, or 4Mx1 DRAMs. The DRAM data outputs connect directly to the CPU data bus.

The DRAM Memory Address bits MA10-MA1 connect directly to each DRAM. MA9 is used only for 1Mx1, 1Mx4, and 4Mx1 DRAMs. MA10 is used for 4Mx1 DRAMs only. MA0X is connected to an address input of each DRAM in Banks 0 and 2, while MA0Y is connected to an address input of each DRAM in Banks 1 and 3. The two versions of MA0 have different timings during Interleaved Burst Mode operation, and are necessary to meet DRAM address setup and hold specifications.

The VL82C486 supplies each bank with its own –RAS signal (–RAS3 - –RAS0). Each bank has a separate CAS signal for each byte of the bank, to allow individual byte and word writes. Each CAS3-CAS0 signal from the VL82C486 is externally NANDed with each of the MBE3-MBE0 signals to form 16 separate CAS signals, a group of four for each bank, as depicted in Figure 5.

The –RAMW signal is connected directly to the write enable (–WE) input of each DRAM.

Configuration B

Configuration B supports two 32/36-bit DRAM data buses and is shown in Figure 7. DRAM Banks 0 and 2 share one data bus, and DRAM Banks 1 and 3 share the other. Each DRAM data bus is enabled onto the 32-bit CPU data bus by a set of 74F245 buffers. The VL82C486 generates an –MDENX signal for enabling the Bank 0/2 buffers onto the CPU data bus, and an –MDENY signal for enabling the Bank 1/3 buffers onto the data bus. The –RAMW signal is used to control the direction of the bidirectional buffers.

MA, –RAS, and CAS signals are connected in the same way as for Configuration A.

Configuration B allows the CAS signals for DRAM Banks 0/2 and 1/3 to overlap without data contention, thus improving the performance of interleaved burst read cycles.

Double-Sided SIMM Support

Each of the four banks support the use of two rows of DRAMs, allowing the use of double-sided SIMMs. Each of the two rows in each bank is connected to the same CAS signal. The configuration is shown in Figures 8 and 9.

To save pins, –RAS3 - –RAS0 are shared between pairs of banks. For Banks 0 and 1, RAS0 goes to Side One of the SIMMs for each bank, and –RAS1 goes to Side Two of the SIMMs in each banks. The same applies for –RAS2 and –RAS3 for Banks 2 and 3. Since each side of the SIMMs receive the same CAS signal, to avoid data contention the VL82C486 guarantees that –RAS0 and –RAS1 are never asserted simultaneously to double-sided banks. The same applies to –RAS2 and –RAS3. The paging mechanism of the VL82C486 restricts use of double-sided SIMMs to the following configurations:

- If interleaving double-sided SIMMs between Banks 0 and 3 only (Interleave Mode 010), then Banks 1 and 2 must be unpopulated.
- If interleaving double-sided SIMMs between Banks 1 and 2 only (Interleave Mode 011), then Banks 0 and 3 must be unpopulated.

DRAM Physical Configuration Registers

Two 8-bit registers, RAMCFG0 and RAMCFG1, are used to program the physical DRAM configuration indicating the DRAM type for each bank. The registers are Indexed Configuration

Registers and are accessed via the Index and Data Ports at I/O addresses ECh and EDh. The RAMCFG0 and RAMCFG1 Registers' formats are given in Tables 12 and 13.

DRAM type may be none, 256Kx1 or 256Kx4, 1Mx1 or 1Mx4, or 4Mx1 DRAMs.

The bank type may be either single or double-sided. The bank size in bytes is thus the DRAM type multiplied by four for single-sided banks and the DRAM type multiplied by eight for double-sided banks.

TABLE 12. RAMCFG0 CONFIGURATION REGISTER (02h) - READ/WRITE

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
RAMCFG0 (02h)	1	BANK 1 DRAM SIZE 00 = None 01 = 512Kx1, or x4 10 = 1Mx1, or x4 11 = 4Mx1		BANK 1 TYPE 0 = Single 1 = Double	1	BANK 0 DRAM SIZE 00 = None 01 = 512Kx1, or x4 10 = 1Mx1, or x4 11 = 4Mx1		BANK 0 TYPE 0 = Single 1 = Double

TABLE 13. RAMCFG1 CONFIGURATION REGISTER (03h) - READ/WRITE

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
RAMCFG1 (03h)	1	BANK 3 DRAM SIZE 00 = None 01 = 512Kx1, or x4 10 = 1Mx1, or x4 11 = 4Mx1		BANK 3 TYPE 0 = Single 1 = Double	1	BANK 2 DRAM SIZE 00 = None 01 = 512Kx1, or x4 10 = 1Mx1, or x4 11 = 4Mx1		BANK 2 TYPE 0 = Single 1 = Double

DRAM MEMORY MAPS

Overview

The DRAM memory mapping (i.e., where each DRAM bank appears in the CPU address space) is determined by the RAMCFG Registers and the interleave selection set by bits 7-5 (INTLV2-INTLV0) in the RAMSET Register.

The DRAM memory map always starts at CPU address zero and is always contiguous except for "holes" created by the Segment Control and the PMR Registers. Two banks or four banks may share the same address range, depending on the interleave type selected. The two "sides" of a double-sided SIMM always occupy consecutive and contiguous address ranges.

Interleave Mode Selection

The Interleave Mode selection determines which banks occupy the same address range for two- or four-way interleave and help determine the start address of each bank. The Interleave Mode options are programmed by the INTLV2-INTLV0 bits in the RAMSET Register as follows:

INTLV2-INTLV0	Interleave Mode Selection
000	No interleave
001	Banks 0 & 1 only
010	Banks 0 & 3 only
011	Banks 1 & 2 only
100	Banks 2 & 3 only
101	Banks 0 & 1, or Banks 2 & 3
110	Banks 0 & 3, or Banks 1 & 2
111	Banks 0 & 1 and Banks 2 & 3 (four-way interleave)

Interleaved banks must be of both the same size and type. If unlike banks are programmed as interleaved, then the operation is undefined. When using double-sided SIMMs, Interleave Mode selection is restricted by the limitations (specified in the section titled "Double-Side SIMM Support" on page 34).

For two-way interleave, address bit A2 is used to select one of the banks in an interleaved pair as follows:

A2 = 0: Bank 0 or Bank 2 is selected
A2 = 1: Bank 1 or Bank 3 is selected

For four-way interleave, address bits A14 and A2 are used to select one of the banks as follows:

A14 and A2 = 00: Bank 0 is selected
A14 and A2 = 01: Bank 1 is selected
A14 and A2 = 10: Bank 2 is selected
A14 and A2 = 11: Bank 3 is selected

Note that A2 changes during a CPU burst read, therefore causing alternate interleaved banks to be accessed during a burst. However, A14 never changes during a burst read, hence only two banks can ever be active during a burst cycle.

Bank Start Address
The start address of each of the four DRAM banks is determined as shown in Table 14.

–RAS Strobe Decode
–RAS decode is performed as a function of the RAMCFG Registers, the Interleave Mode selection, and the CPU address. Each bank has an active address range which is a function of the bank size (as specified in Table 14), and the interleave information. For non-interleaved memory accesses, if the CPU address falls within the address range of a DRAM bank, then the –RAS signal for that bank is activated. For interleaved accesses, if the address falls within the range of the two selected banks, then the –RAS signals for both banks are asserted simultaneously.

For banks that have two rows of DRAMs (i.e., use double-sided SIMMs), then each half of the bank has an active address range. For Banks 0 and 1, –RAS0 is asserted for accesses to the lower half and –RAS1 is asserted for accesses to the upper half. For Banks 2 and 3, –RAS2 is asserted for accesses to the lower half and –RAS3 is asserted for accesses to the upper half.

CAS Strobe Decode
The CAS signal for each of the four banks is asserted whenever a memory address falls within the active address range for the bank, as determined by the bank size and Interleave Mode. For interleaved accesses, CAS0 or CAS2 is generated when A2 = 0, and CAS1 or CAS3 is generated when A2 = 1.

TABLE 14. DRAM BANK START ADDRESS

Inter-leave Option	Bank 0 Start Address	Bank 1 Start Address	Bank 2 Start Address	Bank 3 Start Address
000 (None)	0	Size (Bank 0)	Size (Bank 0) +Size (Bank 1)	Size (Bank 0) +Size (Bank 1) +Size (Bank 2)
001 (Banks 0, 1)	0	0	Size (Bank 0)x2	Size (Bank 0)x2 +Size (Bank 2)
010 (Banks 0, 3)	0	Size (Bank 0)x2	Size (Bank 0)x2 +Size (Bank 1)	0
010 (Banks 1, 2)	Size (Bank 2)x2	0	0	Size (Bank 0) +Size (Bank 2)x2
100 (Banks 2, 3)	Size (Bank 2)x2	Size (Bank 0) +Size (Bank 2)x2	0	0
101 (Banks 0, 1 or 2, 3)	0	0	Size (Bank 0)x2	Size (Bank 0)x2
110 (Banks 0, 3 or 1, 2)	0	Size (Bank 0)x2	Size (Bank 0)x2	0
111 (Banks 0, 1, 2, 3)	0	0	0	0

Where:

Size (Bank n) = 0 if no DRAM is programmed for that bank.
= 1 MB if 256Kx1 or 256Kx4 DRAMs are used and the bank is single-sided.
= 2 MB if 256Kx1 or 256Kx4 DRAMs are used and the bank is double-sided.
= 4 MB if 1Mx1 or 1Mx4 DRAMs are used and the bank is single-sided.
= 8 MB if 1Mx1 or 1Mx4 DRAMs are used and the bank is double-sided.
= 16 MB if 4Mx1 DRAMs are used (bank must be single-sided).

FIGURE 5. DRAM –CAS GENERATION

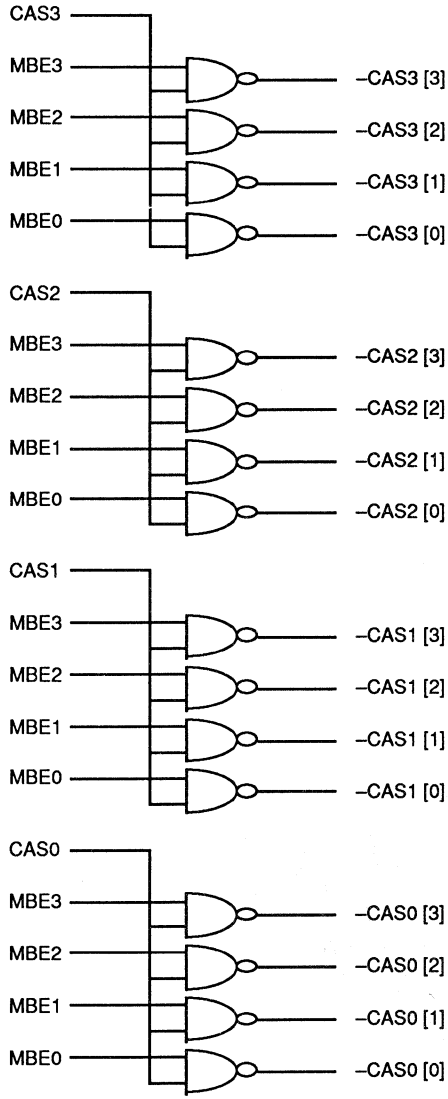


FIGURE 6. FOUR BANK DRAM SYSTEM - CONFIGURATION A

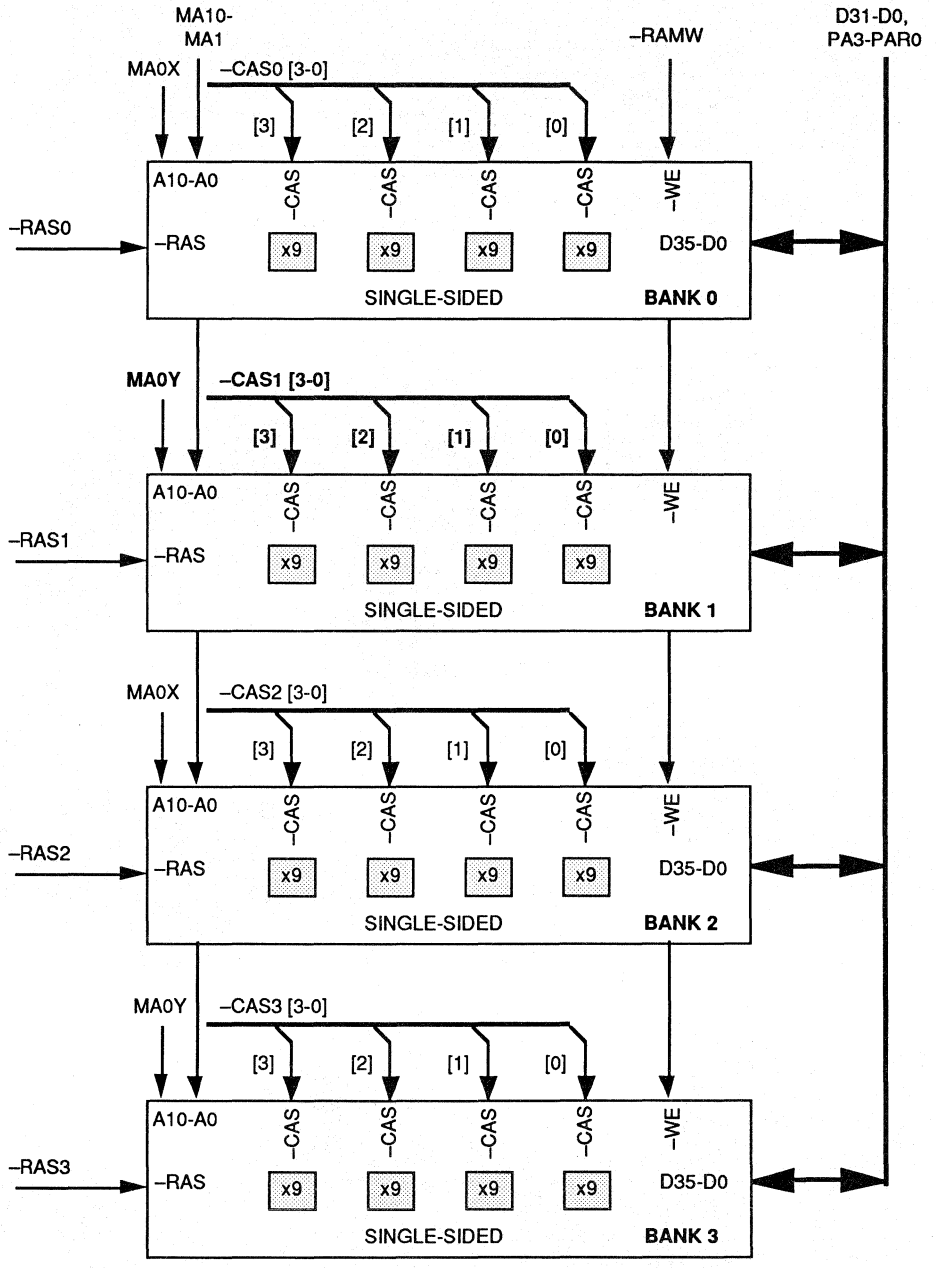


FIGURE 7. FOUR BANK DRAM SYSTEM - CONFIGURATION B

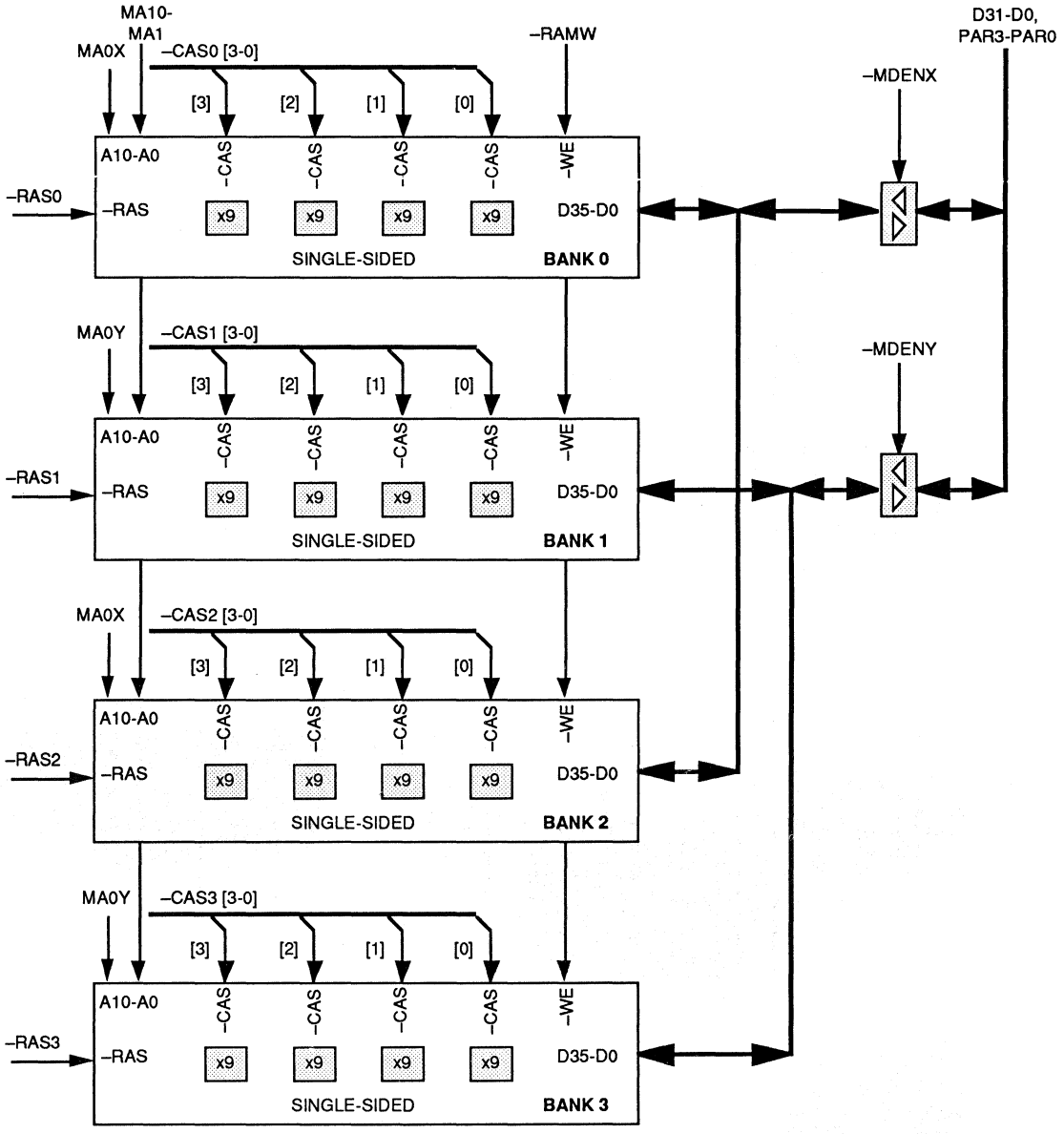


FIGURE 8. FOUR BANK DOUBLE-SIDED SIMM - CONFIGURATION A

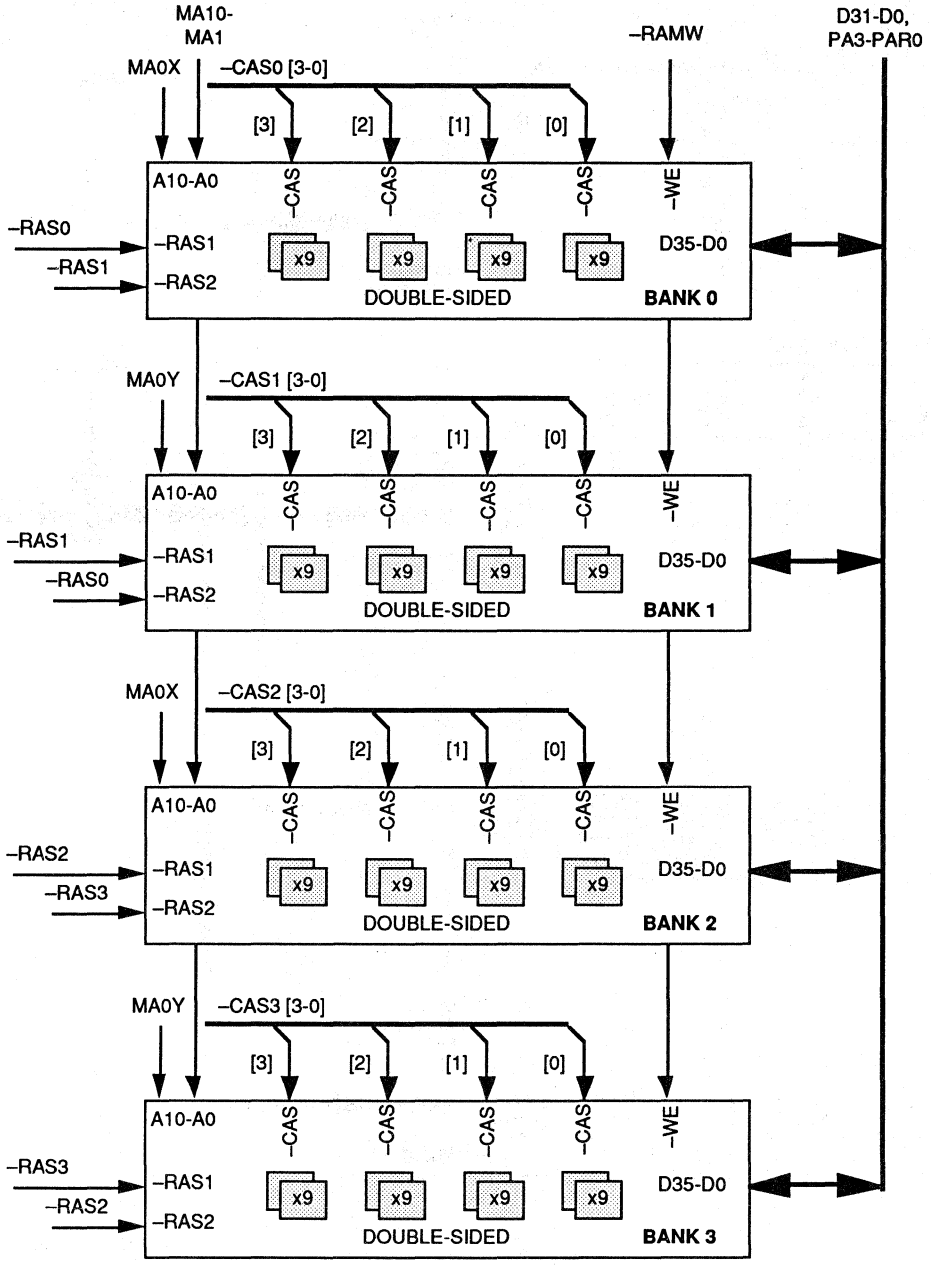
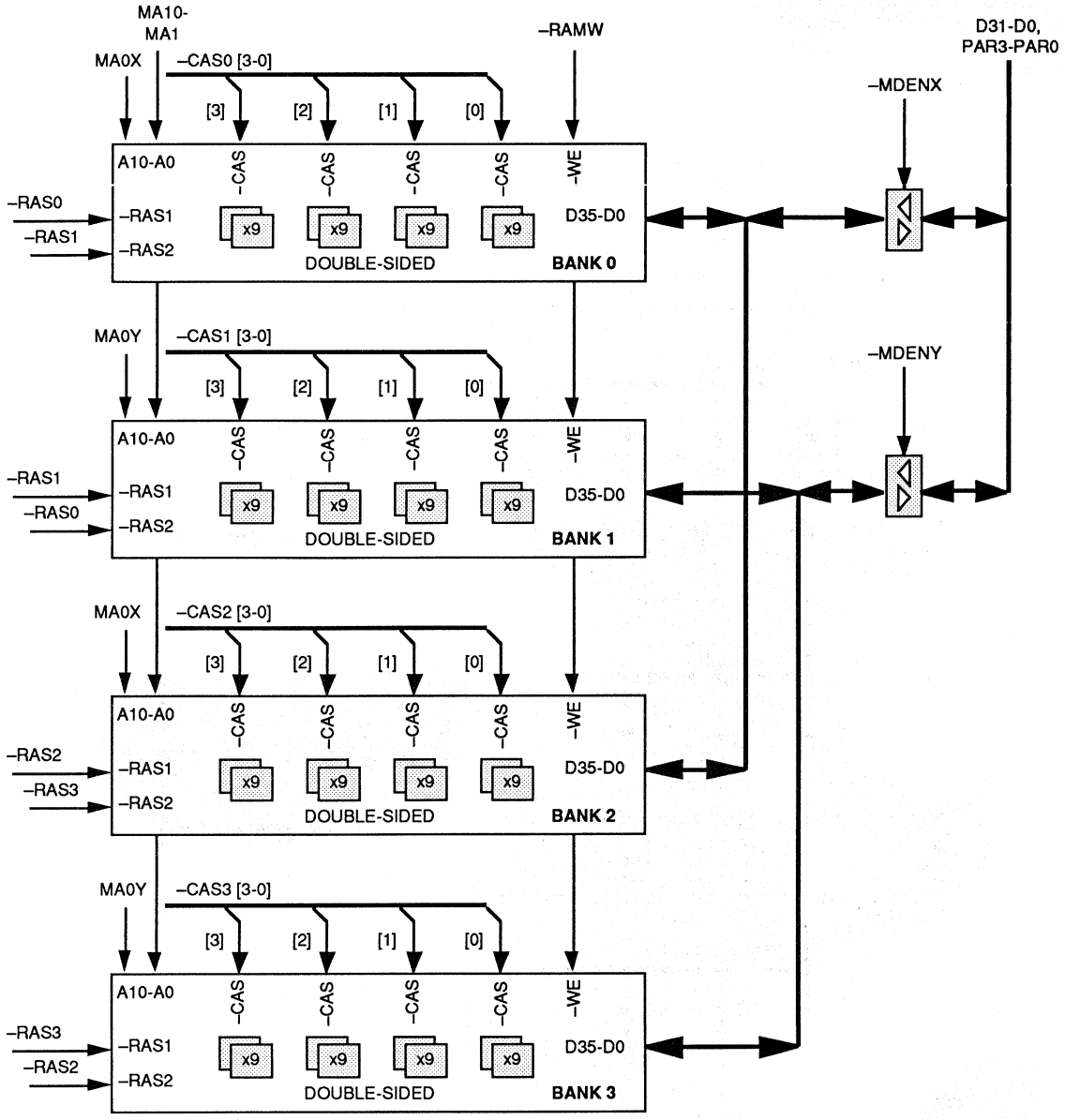


FIGURE 9. FOUR BANK DOUBLE-SIDED SIMM - CONFIGURATION B



DRAM Memory Addressing
The DRAM memory address generation is a function of the CPU memory address, the DRAM type, and the Interleave Mode selection. DRAM row and column address are multiplexed onto the same MA bus. When operating in Non-Page Mode or on page-misses, then a row address followed by a column address is generated during a DRAM access. On page-hits only a column address is generated during a DRAM access.

During CPU burst reads all column address bits except MA1, MA0X, and MA0Y remain stable throughout the burst. MA0X and MA0Y reflect the changing state of A3 during the burst. MA1 reflects the changing state of A2 during non-interleaved bursts.

Table 15 shows how the CPU memory address maps to the MA bus for row and column addresses. 0X/0Y in the table represents both MA0X and MA0Y.

TABLE 15. DRAM PAGE/INTERLEAVE MAPPING

		No Interleave			2-Way Interleave			4-Way Interleave		
	MA	256K	1M	4M	256K	1M	4M	256K	1M	4M
Column Address	10	X	X	A12	X	X	A13	X	X	A13
	9	X	A11	A11	X	A12	A12	X	A12	A12
	8	A10	A10	A10	A10	A10	A10	A10	A10	A10
	7	A9	A9	A9	A9	A9	A9	A9	A9	A9
	6	A8	A8	A8	A8	A8	A8	A8	A8	A8
	5	A7	A7	A7	A7	A7	A7	A7	A7	A7
	4	A6	A6	A6	A6	A6	A6	A6	A6	A6
	3	A5	A5	A5	A5	A5	A5	A5	A5	A5
	2	A4	A4	A4	A4	A4	A4	A4	A4	A4
	1	A2	A2	A2	A11	A11	A11	A11	A11	A11
	0X/0Y	A3	A3	A3	A3	A3	A3	A3	A3	A3

		No Interleave			2-Way Interleave			4-Way Interleave		
	MA	256K	1M	4M	256K	1M	4M	256K	1M	4M
Row Address	10	X	X	A23	X	X	A23	X	X	A23
	9	X	A21	A21	X	A21	A21	X	A21	A21
	8	A19	A19	A19	A19	A19	A19	A19	A19	A19
	7	A18	A18	A18	A18	A18	A18	A18	A18	A18
	6	A17	A17	A17	A17	A17	A17	A17	A17	A17
	5	A16	A16	A16	A16	A16	A16	A16	A16	A16
	4	A15	A15	A15	A15	A15	A15	A15	A15	A15
	3	A14	A14	A14	A14	A14	A14	A21	A23	A25
	2	A13	A13	A13	A13	A13	A24	A13	A13	A24
	1	A11	A20	A20	A20	A20	A20	A20	A20	A20
	0X/0Y	A12	A12	A22	A12	A22	A22	A12	A22	A22

DRAM INTERFACE OPERATION FOR CPU ACCESSES

Overview

This section describes the operation of the on-board DRAM interface for CPU and DMA/Master Mode accesses.

For all CPU accesses, DRAM cycles are generated synchronously with the CPU clock. DRAM signals may change on either edge of the CPU clock depending on how the RAMTMG Configuration Register is set. The timing of DRAM cycles for CPU accesses is a function of the physical configuration (Configuration A or B), the Interleave Mode selected, and the value in the RAMTMG Register.

All CPU memory cycles are assumed to be Burst Mode accesses. After a read cycle is started, up to four consecutive 32-bit DRAM accesses with incremental addresses are automatically generated. The DRAM controller terminates the burst when the CPU makes –BLAST active. The DRAM controller always asserts –BRDY (and not –RDY) on completion of DRAM cycles for both CPU reads and writes.

Cycles may operate in Page or Non-Page Mode. However, –RAS signals are always held active throughout the duration of a burst cycle; thus non-page DRAMs are not supported.

Critical DRAM timing parameters for CPU accesses are settable via the RAMTMG Register to allow the use of different speed DRAMs at various frequencies.

In the next sections, the following terminology is used to describe the starting conditions for CPU DRAM accesses:

Bank-Miss: The CPU accesses a DRAM bank that has an inactive –RAS.

Page-Hit: The CPU accesses a DRAM bank that has an active –RAS and the previous access to that bank was to the same DRAM page as the current access.

Page-Miss: The CPU accesses a DRAM bank that has an active –RAS and the previous access to the bank was not to the same DRAM page as the current access.

DRAM Programmable Timing

For CPU accesses, the timing of DRAM cycles is programmable to allow for different operating frequencies and different DRAM speeds.

The start of a DRAM cycle (the time at which –RAS or CAS is first asserted) is programmable to be the beginning of the first T2 of the CPU cycle, in the middle of the first T2, or at the beginning of the second T2. On page-hits, CAS is always asserted at the beginning of the second T2 for write cycles, but is programmable as described above for read cycles.

–RAS precharge time and –RAS to CAS delay are programmable to be from one to four CPU clocks.

CAS pulse width is programmable to be 1, 1.5, or 2 CPU clocks.

The format and function of the RAMTMG Register is given in Table 16.

Page Mode Operation

DRAM cycles normally operate in Page Mode. Each –RAS is held active after a CPU DRAM access has finished and is precharged only when a subsequent cycle to the same bank does not access the same DRAM page as the last cycle to that bank, or if an asynchronous event such as a refresh or DMA cycle causes a precharge cycle. The page size is a function of DRAM type and Interleave Mode.

In Non-Interleaved Mode, the DRAM page size is 2, 4, or 8 KB for 256K, 1M, or 4M DRAMs respectively; up to four pages may be open simultaneously (one per bank), depending on whether one, two, three, or four banks are populated. However, only one page at a time may be open for pairs of banks that employ double-sided SIMMs, since only one of the two –RAS signals used by double-sided SIMMs can be active at one time.

In Interleaved Mode, the page size is 4, 8, or 16 KB for 256K, 1M, or 4M DRAMs respectively; one or two pages may be open simultaneously depending on whether two or four banks are populated.

The DRAM controller may be configured to operate in "Burst Page Mode" by setting bit 0 (PGMD) of the RAMSET Register. In this mode, –RAS signals are always precharged at the end of each write cycle or burst read cycle. However, –RAS signals are held active through the duration of burst read cycles, so use of non-page DRAMs is not permitted. This mode is useful for applications that generate scattered memory references that would generate many DRAM page-misses and hence precharge cycles if operating in full Page Mode.

DMA/Master Mode cycles do not employ the Page Mode and always precharge the –RAS signals at the beginning and end of each access.

Page Mode –RAS Time-Out

If a –RAS signal stays active for more than 10 µs it is automatically precharged by the –RAS time-out generator to ensure that maximum DRAM –RAS active times are not violated. However, this feature may be disabled by setting bit 5 (RTODIS) of the RAMSET Register when using RAMs that have –RAS active periods of longer than 15 µs (in which case the intervention of refresh ensures that maximum –RAS active times are not violated).

–RAS Timing

Figure 10 shows all possible –RAS timings that can be generated by the VL82C486 on a CPU DRAM access.

The first group of three waveforms in Figure 10 shows how each –RAS signal is asserted on a bank-miss. –RAS is inactive at the start of the CPU access and is asserted at the beginning or middle of the first T2 or at the beginning of the second T2, depending on the values of TSTRT1 and TRST0 (bits 7 and 6) in the RAMTMG Register.

TABLE 16. RAMTMG REGISTER (01h) - READ/WRITE

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
RAMTMG (01h)	TSTRT1	TSTRT0	TRP1	TRP0	TRCD1	TRCD0	TCAS1	TCAS0
POR Value	1	1	1	1	1	1	1	1

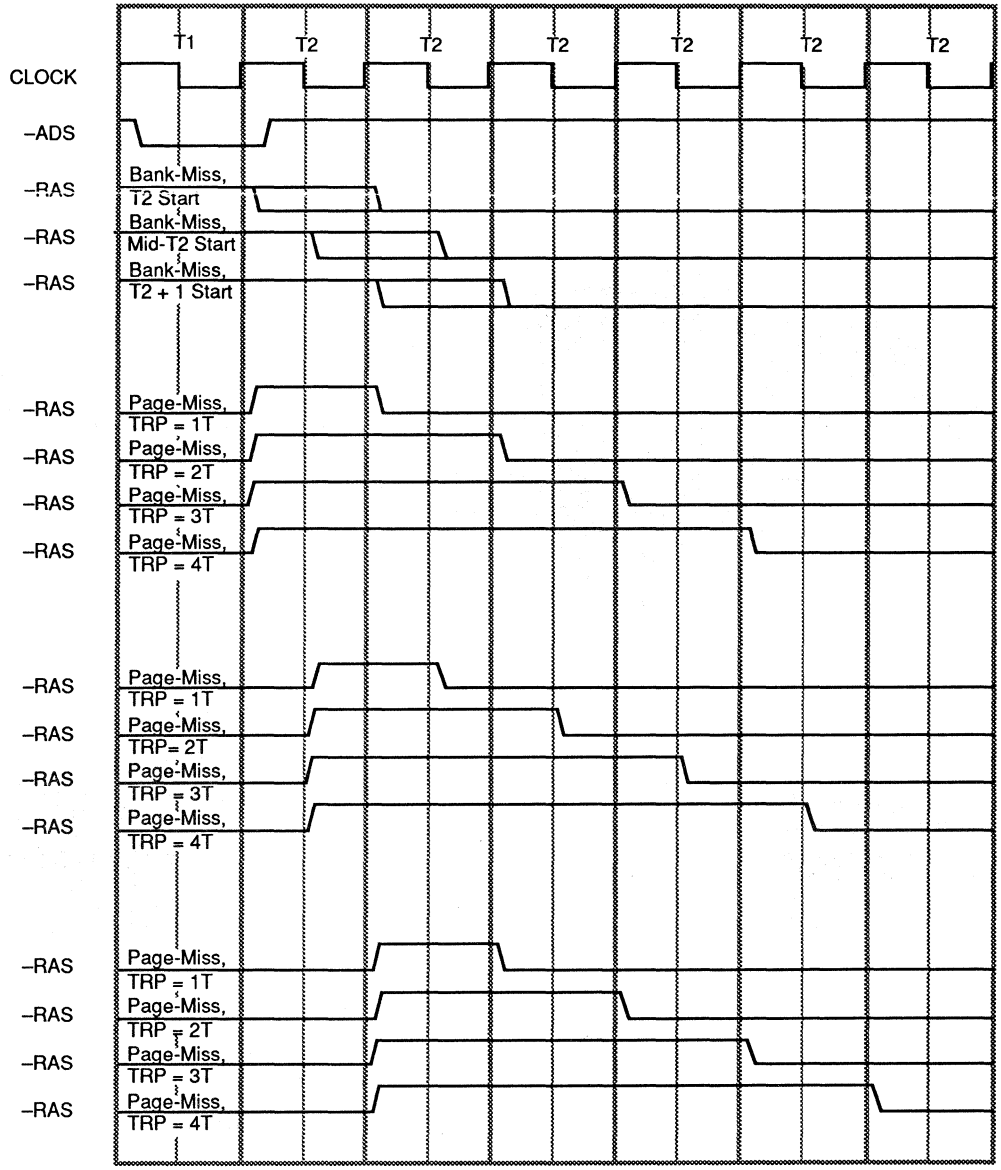
Bit	Name	Function
7, 6	TSTRT1, TSTRT0	Cycle Start: Sets start of DRAM read and write cycles: **Bit 7** **Bit 6** **Cycle Start Time** 0 0 Beginning of first T2 0 1 Middle of first T2 1 X Beginning of second T2
5, 4	TRP1, TRP0	–RAS Precharge: Sets –RAS precharge time for page-misses: **Bit 5** **Bit 4** **–RAS Precharge Time** 0 0 1 CPU Clocks 0 1 2 CPU Clocks 1 0 3 CPU Clocks 1 1 4 CPU Clocks
3, 2	TRCD1, TRCD0	RAS-CAS Delay: Sets RAS-to-CAS Delay for page/bank-misses: **Bit 3** **Bit 2** **RAS-CAS Delay Time** 0 0 1 CPU Clocks 0 1 2 CPU Clocks 1 0 3 CPU Clocks 1 1 4 CPU Clocks 0.5 CPU clock is added to above times if: • TSTRT is set for mid-T2 and TCAS is 1 or 2 clocks. • TSTRT is beginning of first/second T2 and TCAS is 1.5 clocks.
1, 0	TCAS1, TCAS0	CAS Pulse Width: Sets CAS pulse width for read and write cycles: **Bit 1** **Bit 0** **CAS Pulse Width Time** 0 0 1 (read), 1 (write) CPU Clocks 0 1 1.5 (reads), 1 (write) CPU Clocks 1 0 2 (reads), 1 (write) CPU Clocks 1 1 2 (reads), 2 (writes) CPU Clocks

The second, third, and fourth groups of waveforms in Figure 10 show how each –RAS is generated on a bank-hit/page-miss. In this case, the –RAS is deasserted for a number of T-states equal to the value set in the TRP1 and TRP0 bits of the RAMTMG Register. Each group shows the timing for one of the three different values of TSTRT (beginning, middle of first T2/beginning of second T2).

Lastly, on a page-hit, –RAS is not affected since it will already be active at the start of the cycle and will remain active.

During Non-Page Mode cycles, –RAS is deasserted at the end of the last T2 if the earliest cycle start point is the beginning of the first T2 or the end of the first T2 (i.e., TSTRT1 and TSTRT0 of the RAMTMG Register = 00 or 10). –RAS is deasserted in the middle of the next Ti or T1 cycle following the end of the Non-Page Mode cycle if the earliest cycle start point is the middle of the first T2 (i.e., TSTRT1 and TSTRT0 = 01).

FIGURE 10. DRAM CONTROLLER –RAS TIMING



–RAS Wait States
As shown by the first three waveforms in Figure 10 on bank-misses, assertion of –RAS is delayed by one wait state. Performance impact when operating in Page Mode is negligible as most accesses generate page-hits or page-misses (and not bank-misses).

–RAS wait states are disabled when bit 1 in MISCSET register is set.

RAS-to-CAS Timing
The delay from assertion of –RAS to assertion of the first CAS is programmable via the TRCD1 and TRCD0 bits (bits 3 and 2) in the RAMTMG Register. Timing for 1T, 1.5T, and 2T CAS signals are shown in Figure 11. As shown in Figure 11, an extra 0.5T RAS-to-CAS delay is added if:

- –RAS is asserted on a negative clock edge and CAS is asserted on a positive clock edge.
- –RAS is asserted on a positive clock edge and CAS is asserted on a negative clock edge.

CAS Page-Hit Timing
Figure 12 shows all the times at which the first CAS may be asserted at the beginning of a read or write cycle. CAS signals for burst reads may start at the beginning of the first T2, the middle of the first T2, or the beginning of the second T2 as shown, depending on how the TSTRT and TCAS fields in the RAMTMG Register are programmed. CAS signals for writes always start at the beginning of the second T2 (unless delayed by conditional wait states; see next section below).

CAS Conditional Wait States
On page-hits, assertion of the first CAS of a DRAM access may be delayed by one wait state as shown in Figure 12. This occurs when:

- The current access is to an interleaved bank pair and the previous access was to a non-interleaved bank.
- The current access is to a non-interleaved bank and the previous access was to an interleaved bank pair.

The extra wait state is used to hold off CAS while the MA multiplexers select a different column address MA format for interleaved or non-interleaved banks.

CAS conditional wait states are disabled when:

- All active DRAM banks operate in the Interleave Mode or all active banks operate in the Non-Interleave Mode.
- Bit 1 (SLP) in the MISCSET Register is set. For RAMTMG Register settings and clock frequencies that can tolerate the extra MA delay incurred in switching from interleaved to non-interleaved column address format without an additional wait state (see AC Timings), CAS conditional wait states may be turned off by setting bit 1 in the MISCSET Register.

CAS Burst Sequencing
Figure 13 shows all possible CAS timings that can be generated by the VL82C486 on a CPU DRAM access. CASx may be any one of the four CAS3-CAS0 signals and CASy may be the CAS for any bank that is permitted to interleave with the bank selected by CASx. Figures 14 and 15 are for write cycles; all the others are for burst reads.

All the signal timings shown assume that the access is a page-hit and that the –RAS signal for the selected bank is already active. On page-misses, the CAS signals would be asserted after the RAS-to-CAS delay as described previoulsy in the section titled "–RAS Timing" on pages 43 and 44.

For 1.5T CAS signals, the diagrams assume that the RAMTMG Register is programmed for cycles to start at the beginning or the middle of the first T2. If it is programmed for cycles to start at the end of the first T2, then the first CAS would be asserted 1T later than shown.

For 1T and 2T CAS signals, the diagrams assume that the RAMTMG Register is programmed for cycles to start at the the middle of the first T2 or the beginning of the second T2. If it is programmed for cycles to start at the beginning of the first T2, then the first CAS would be asserted 1T earlier than shown.

For Configuration B, interleaved accesses using 1.5T CAS signals, a spurious 1T CAS is generated at the end of the burst cycle as shown. This is caused by the –BLAST signal not being generated early enough by the 486 to shut-off the CAS generation mid-cycle. However, since this can only occur for read cycles, no harm results.

On write cycles, a 1T or 2T CAS is always generated as shown in the second T2 (on page-hits) of the access.

Burst writes are also supported. The DRAM controller generates BRDY after each 32-bit write to the DRAM. The DRAM controller terminates the burst write whenever the local bus master assists –BLAST. A one clock gap between successive CAS's is guaranteed to allow time for the bus master to drive new data. For correct operation of burst writes, –BE3 - –BE0 must be held active throughout the burst cycle.

–BRDY Timing
Referring to Figure 13, the VL82C486 always asserts –BRDY as follows:

- For 1T CAS signals, –BRDY is asserted at the same time as each CAS.
- For 1.5T CAS signals, –BRDY is asserted during the last whole clock cycle of each CAS (but it is inhibited during the spurious CAS generated at the end of a Configuration B interleaved access).
- For 2T CAS signals, –BRDY is asserted during the second clock cycle of each CAS.

FIGURE 11. DRAM CONTROLLER –RAS TO CAS DELAYS

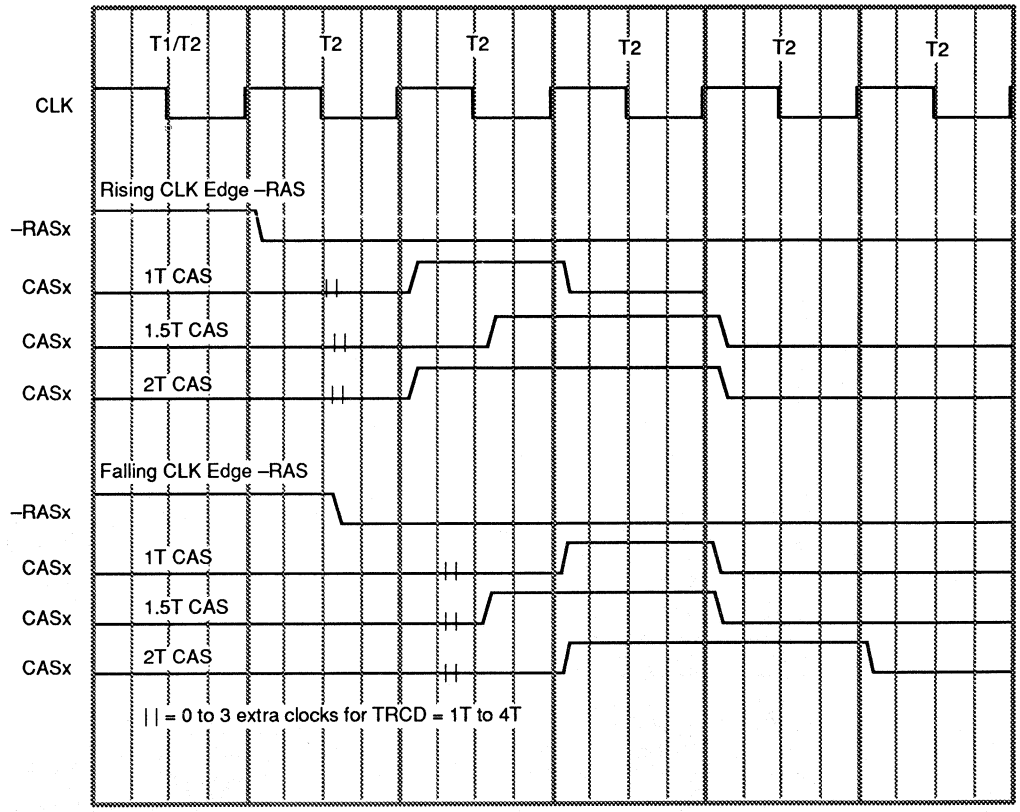


FIGURE 12. DRAM CONTROLLER PAGE-HIT CAS START TIMING

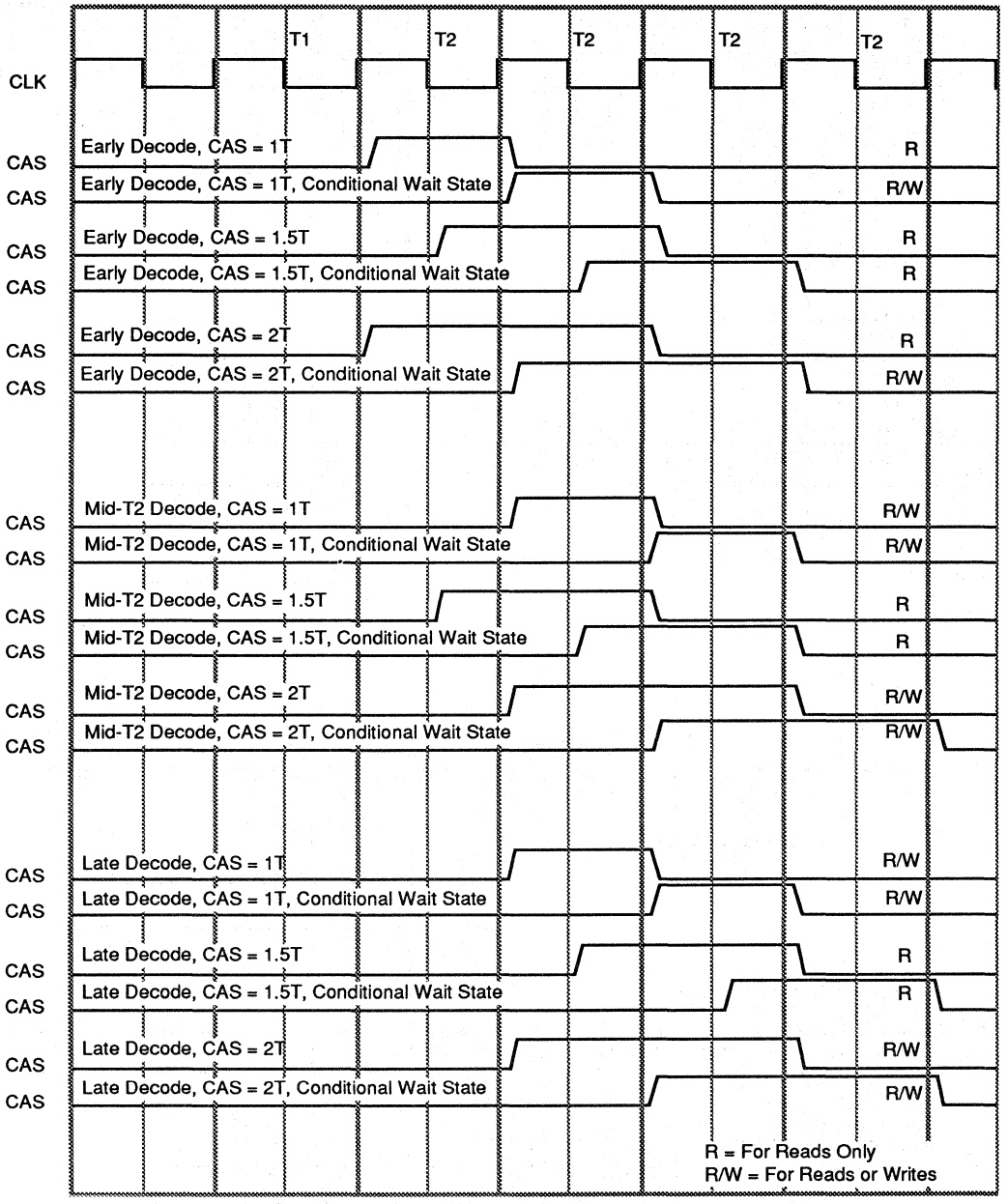


FIGURE 13. DRAM CONTROLLER READ/WRITE CAS BURST SEQUENCING

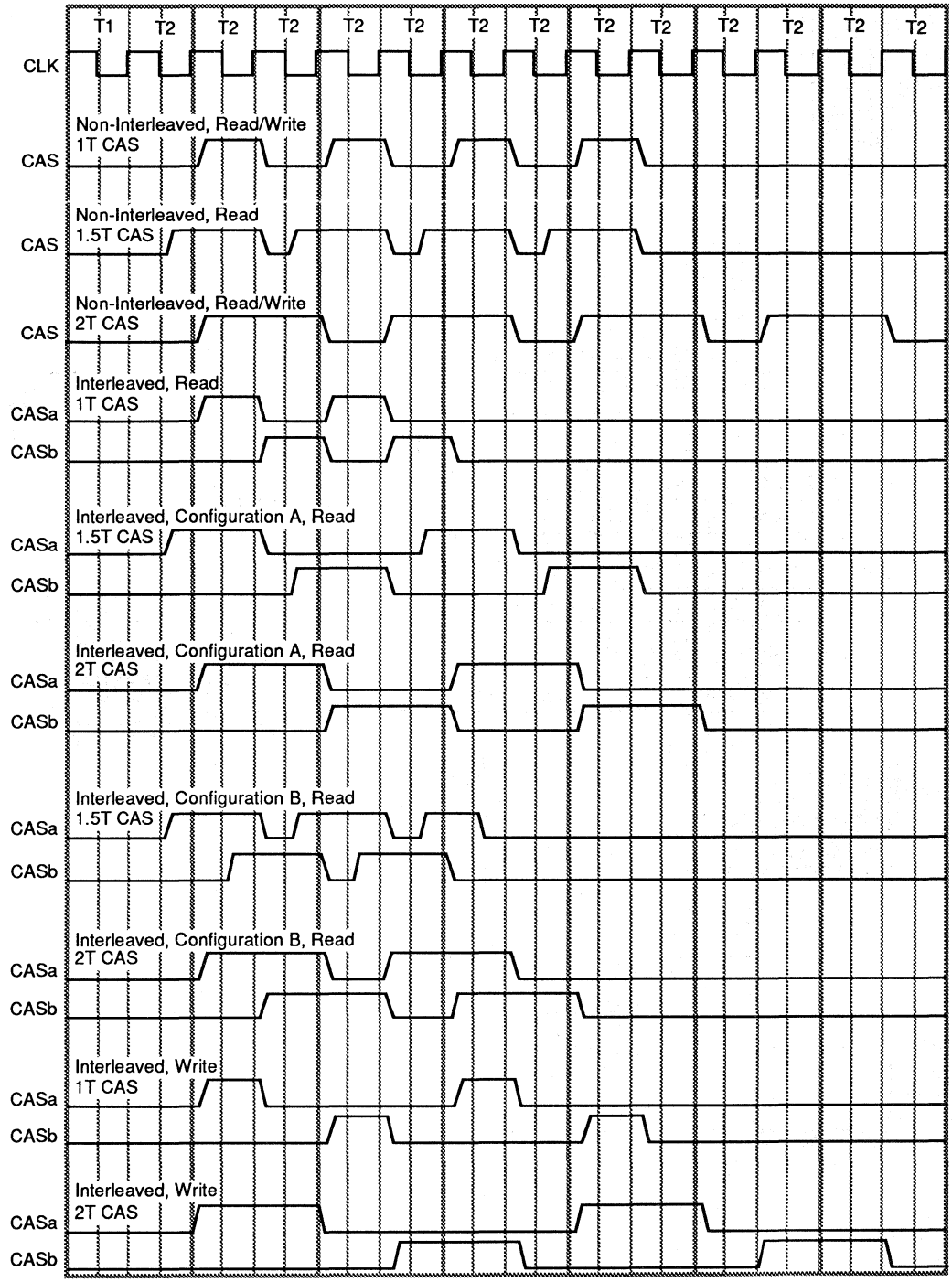


FIGURE 14. MA10-MA0 ROW/COLUMN ADDRESS SWITCHING

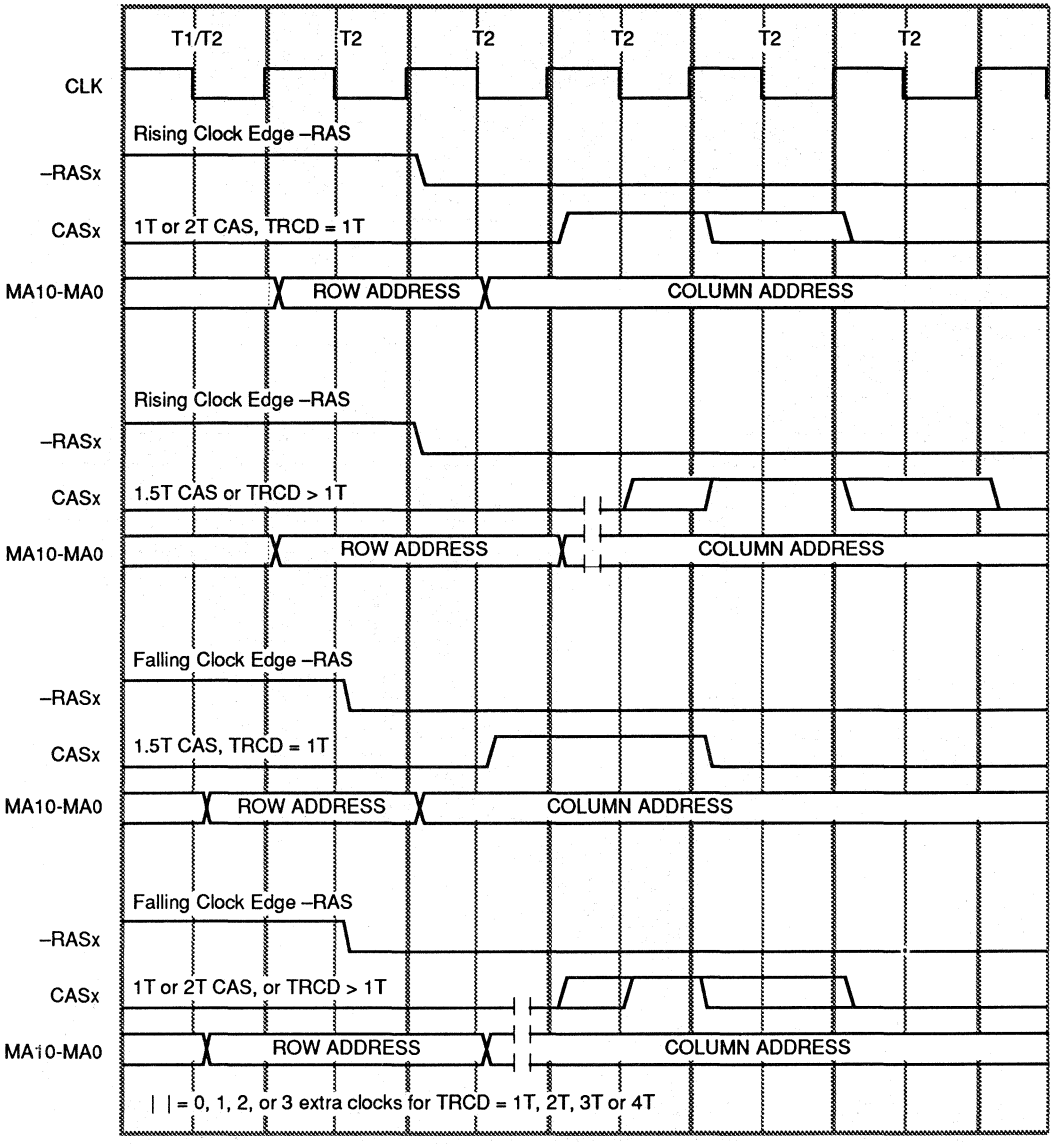
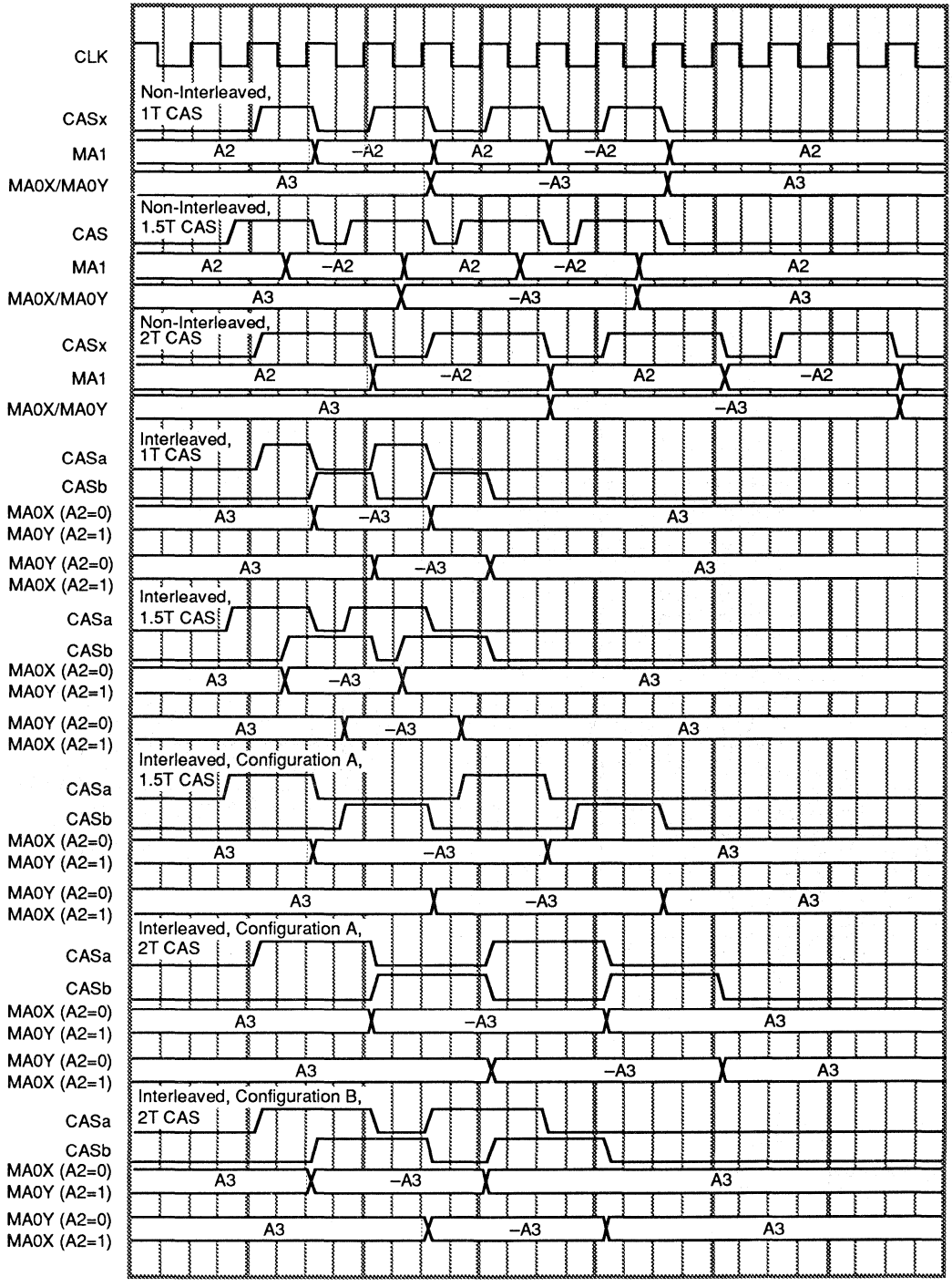


FIGURE 15. MA1, MA0X, MA0Y BURST SEQUENCING



–MDENX, –MDENY Timing
Referring to Figure 13, the VL82C486 asserts –MDENX and –MDENY during CPU reads as follows:

- For 1T CAS signals, –MDENX is asserted at the same time as CAS0 and CAS2. –MDENY is always asserted at the same time as CAS1 and CAS3.
- For 1.5T CAS signals, –MDENX is asserted during the last whole clock cycle of CAS0 and CAS2. –MDENY is always asserted during the last whole clock cycle of CAS1 and CAS3. However, both are inhibited during the spurious CAS generated at the end of a Configuration B interleaved access.
- For 2T CAS signals, –MDENX is asserted at the same time as CAS0 and CAS2. –MDENY is always asserted at the same time as CAS1 and CAS3. The only exception to this is for Configuration B interleaved cycles when –MDENX is asserted during the second clock cycle of CAS0 and CAS2, and –MDENY is asserted during the second clock cycle of CAS1 and CAS3.
- On CPU writes, both –MDENX and –MDENY are asserted throughout all the T2 cycles of the write access.

MA Bus Timing
Figure 14 shows how the MA bus is switched between selection of row or column address on CPU DRAM accesses. Selection is as follows:

- On a bank-miss or a page-miss, row address is always selected at least 1T before –RASx is asserted.
- The row address is always held for one clock cycle after –RAS is asserted and MA is then switched to select the column address. The exception to this is when there is only one clock cycle between assertion of –RASx and assertion of CASx; in this case, MA is switched to select the column address after one-half a clock cycle from assertion of –RAS, as shown in Figure 13.
- On a page-hit, the column address will already be selected since the VL82C486 defaults to selecting the column address during idle cycles if any –RASx is active.

MA0X, MA0Y, and MA1 Operation During Burst Reads and Writes
Figure 15 shows the timing of MA1, MA0X, and MA0Y. When column address is selected during a burst cycle, MA0X and MA0Y reflect the state of A3. During non-interleaved burst cycles, MA1 reflects the state of A2. The VL82C486 alters the state of these signals during a burst read cycle as follows:

- For non-interleaved cycles, MA0X and MA0Y are inverted in the clock cycle after the second CAS is deasserted. MA1 is inverted after the first, second, and third CAS signals are deasserted.
- For interleaved cycles, MA0X is inverted after the first CAS0 or CAS2 is deasserted. MA0Y is inverted after the first CAS1 or CAS3 is deasserted. MA1 does not change.

Burst Read and Write Cycle Wait States
Table 17 summarizes the number of CPU clocks required (counting from T1) for each double-word (W1-W4) transferred during a burst read for each memory configuration and timing option. The table assumes page-hits. Wait states for bank-misses and page-misses are added separately as described in the notes below the table. Also, a conditional wait state may be added to the W1 column under the conditions specified in the section titled "CAS Conditional Wait States" on page 46.

TABLE 17. CLOCK CYCLES FOR CPU DRAM READ ACCESSES

	Configuration A				Configuration B				Configuration A and B							
	Read Interleave				Read Interleave				Read No Interleave				Burst Writes			
CAS Width/Cycle Start	W1	W2	W3	W4	W1	W2	W3	W4	W1	W2	W3	W4	W1	W2	W3	W4
CAS=1T, TSTRT=00	2	1	1	1	2	1	1	1	2	2	2	2	3	2	2	2
CAS=1T, TSTRT=01/1X	3	1	1	1	3	1	1	1	3	2	2	2	3	2	2	2
CAS=1.5T, TSTRT=0X	3	2	2	2	3	1	1	1	3	2	2	2	NA	NA	NA	NA
CAS=1.5T, TSTRT=1X	4	2	2	2	4	1	1	1	4	2	2	2	NA	NA	NA	NA
CAS=2T, TSTRT=00	3	2	2	2	3	1	2	1	3	3	3	3	4	3	3	3
CAS=2T, TSTRT=01/1X	4	2	2	2	4	1	2	1	4	3	3	3	4	3	3	3

Bank-Misses: If –RAS is inactive at the start of a cycle, then TRCD (as defined by the RAMTMG Register) must be added to each of the above times for the W1 column.

Page-Misses: If –RAS is active at the start of a cycle, but the previous cycle to the DRAM bank was to a different page, then TRP plus TRCD (as defined by the RAMTMG Register) must be added to each of the above times for the W1 column.

Write Cycle Wait States
The number of clock cycles required for a write cycle is as follows:

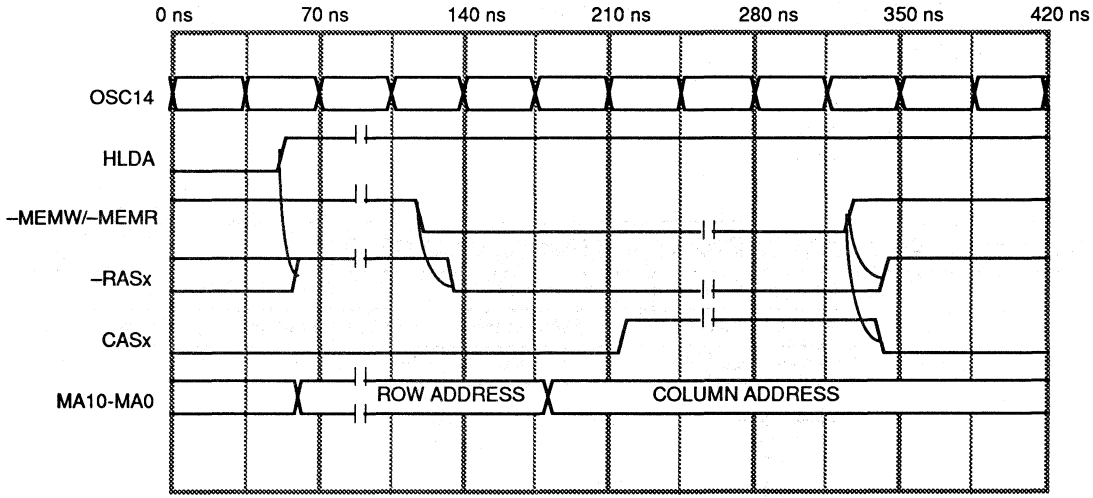
CAS=1T, Page-Hit	3T (1 ws)
CAS=1T, Bank-Miss	TRCD +3T ([TRCD+1] ws)
CAS=1T, Page-Miss	TRCD+TRP+3T ([TRCD+TRP+1] ws)
CAS=2T	Same as above, +1T

DRAM DMA/MASTER MODE CYCLE OPERATION
DMA or Master Mode accesses to on-board DRAM always generate simple non-burst cycles for both reads and writes based on the 14 MHz OSC frequency. –RAS signals are precharged at the beginning and the end of DMA cycles.

Figure 16 shows the DRAM timing for DMA and Master Mode cycles. Operation is as follows:

- When HLDA is asserted by the 486, all –RAS signals are immediately made high for precharging.
- When –MEMR or –MEMW is asserted, the selected –RAS signal is asserted (made low).
- –MEMR and –MEMW are sampled by the next positive or negative edge of the OSC 14 MHz clock. The MA bus is switched from selecting row address to selecting column address 35 ns (one-half an OSC clock) after the ISA bus command is sampled active.
- The selected CAS is asserted (made high) 70 ns (one OSC clock) after the ISA bus command is sampled active.
- The selected –CAS signal remains active for as long as –MEMR or –MEMW is active.
- When –MEMR or –MEMW goes inactive, both CAS and –RAS are deasserted.
- The above sequence is repeated if HLDA stays active and another –MEMR or –MEMW command is generated. When HLDA is removed, the DRAM controller is immediately ready to perform another CPU or DMA cycle.

FIGURE 16. DRAM TIMING FOR DMA/MASTER MODE



DRAM REFRESH

Refresh cycles occur asynchronously every 15.625 µs and like DMA/Master Mode cycles, they are timed from the 14 MHz OSC input.

In Synchronous or Asynchronous Refresh Modes, a DRAM refresh is started when the ISA bus –REFRESH signal goes active. This signal is synchronized with the 14 MHz OSC clock, and is used to generate the staggered refresh timing, as shown in Figure 17.

In Decoupled Mode, DRAM refresh is started during the first CPU T1 or Ti cycle to occur after the on-chip refresh counter has generated a refresh request. The request is synchronized with the OSC frequency and again used to generate the timing as shown below.

In both Asynchronous and Decoupled Modes, the DRAM controller is able to remember CPU DRAM requests that occur while the DRAM refresh is in progress. Such requests are executed as soon as the refresh operation is complete.

CAS3-CAS0 are asserted during refresh cycles, as shown, if the CAS-before-RAS option is selected. This is done by setting bit 1 (CASREF) in the NTBREF Register.

DRAM SPEED REQUIREMENTS

This section explains how to calculate the DRAM speed required for each programmable timing option and configuration (A or B) selected.

Estimates for critical DRAM parameters are based on the following assumptions:

- CLK to CAS (VL82C486) = 14 ns
- CAS to –CAS (74F00) = 6 ns
- CLK to –RAS (VL82C486) = 16 ns
- CLK to MA (VL82C486) = 30 ns
- Data setup time to CLK (486)= 5 ns
- Data buffer delay (Config. B only) = 7 ns
- Clock Duty Cycle = 60/40%(used to calculate delay for falling edge signals)

From the above figures:

- CAS path (Config. A) = 14 ns + 6 ns + 5 ns + CAS Access Time
- CAS path (Config. B) = 14 ns + 6 ns + 7 ns + 5 ns + CAS Access Time
- RAS path (Config. A) = 16 ns + 5 ns+ RAS Access Time
- RAS path (Config. B) = 16 ns + 7 ns + 5 ns + RAS Access Time
- MA path (Config. A) = 30 ns + 5 ns + Col. Adr. Access Time (from VL82C486)
- MA path (Config. B) = 30 ns + 5 ns + 7 ns + Col. Adr. Access Time (from VL82C486)
- MA path (Config. A) = 28/22/16 ns* + 30 ns + 5 ns + Col. Adr. Access Time (from CPU)
- MA path (Config. B) = 28/22/16 ns* + 30 ns + 5 ns + 7 ns + Col. Adr. Time (from CPU)

* for 20/25/33 MHz CPUs.

Table 18 shows the minimum speed requirements in nanoseconds for major DRAM parameters at 20, 25, and 33 MHz. Table 17 may be used to determine the length of each burst cycle generated for each of the DRAM speed options (TCAS = 1T, 1.5T, 2T / Configuration A, Configuration B) selected by Table 18.

FIGURE 17. DRAM REFRESH CYCLES

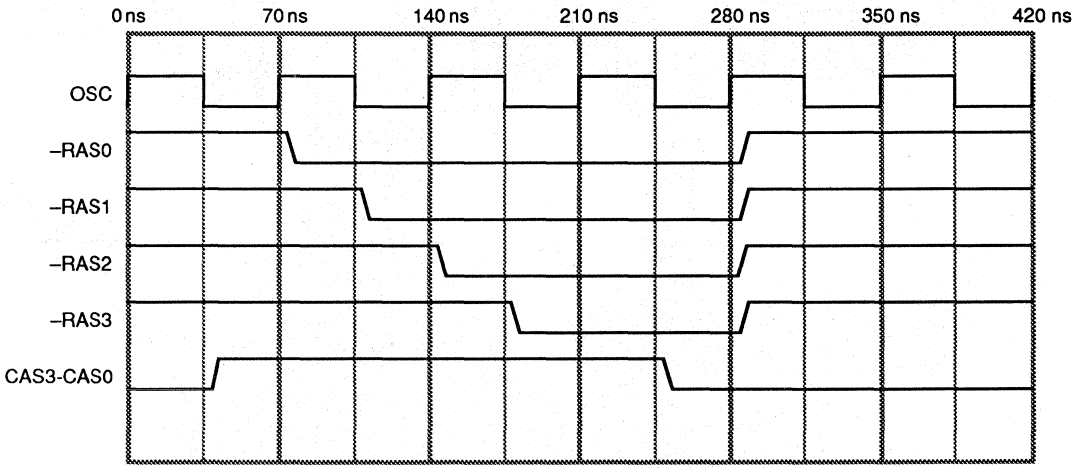


TABLE 18. CALCULATION OF DRAM SPEED REQUIREMENTS

	Configuration A (32-Bit)			Configuration B (64-Bit)		
@ 20 MHz	**TCAS = 1**	**TCAS = 1.5**	**TCAS = 2**	**TCAS = 1**	**TCAS = 1.5**	**TCAS = 2**
RAS Precharge Time	50 x TRP	–	–	–	–	–
RAS Access Time	49/29** + 50 x TRCD	–	–	–	–	–
CAS Access Time	25	–	–	–	–	–
CAS Precharge Time	50	–	–	–	–	–
Column Address Access Time	35/65†† 37†	–	–	–	–	–
@ 25 MHz						
RAS Precharge Time	40 x TRP	40 x TRP	–	–	40 x TRP	40 x TRP
RAS Access Time	35/19** + 40 x TRCD	35/59** + 40 x TRCD	–	–	28/52** + 40 x TRCD	68/52** + 40 x TRCD
CAS Access Time	15	31	–	–	24	48
CAS Precharge Time	40	16/96*	–	–	16	40
Column Address Access Time	21/45†† 23†	45/61††	–	–	38/54††	54/78††
@ 33 MHz						
RAS Precharge Time	–	30 x TRP	30 x TRP	–	30 x TRP	30 x TRP
RAS Access Time	–	21/39** + 30 x TRCD	51/39** + 30 x TRCD	–	14/32** + 30 x TRCD	44/32** + 30 x TRCD
CAS Access Time	–	17	35	–	10	28
CAS Precharge Time	–	12/72*	30/60*	–	12	30
Column Address Access Time	–	25/37††	37/55††	–	18/30††	30/48††

Where: TRP = 1, 2, 3, or 4 and TRCD = 1, 2, 3, or 4 as defined by the RAMTMG Register.

– Not a useful configuration.

* LH number is non-interleaved accesses, RH number is for interleaved accesses.

** LH number is for TSTRT = 01 (mid-T2 cycle start), RH number is for TSTRT = 00/1X (begin/end T2).

† TSTRT = 00 (begin T2).

†† LH number is for TRCD = 1, RH number is for TRCD = 2, 3, or 4 (TSTRT must be 10 or 1X in both cases).

DRAM PARITY GENERATION AND DETECTION

When the parity enable bit (–ENPAR, bit 2) in Configuration Register MISCSET is reset to 0, the VL82C486 checks parity on all on-board read DRAM accesses, whether generated by CPU, DMA or bus master. Even parity is used on a byte-by-byte basis (the sum of the number of "highs" on the eight data bits and the associated parity bit is even).

On DMA or bus master write cycles, the VL82C486 generates even parity for each byte to be written into DRAM, enabling the correct parity value onto PAR3-PAR0. On CPU writes, the parity generated by the 486 is used, thus the VL82C486 three-states its PAR3-PAR0 outputs.

When –ENPAR is set (1), parity checking is inhibited and the parity bits are driven to zero for all cycles that normally generate parity (DMA and bus master cycles). This allows bad parity to be intentionally written to memory for diagnostic purposes.

When a parity error is detected, it is reported through bit 7 (ENA_RAM_PCK) of Port B. If the bit 7 of Port B is reset to zero, then parity errors also cause a Non-maskable Interrupt (NMI) to be generated.

DRAM CONTROL REGISTERS

RAMSET Register

The RAMSET Register controls Interleave Mode, Page Mode selection, MA bus drive current, and –RAS time-out enable. Table 19 shows the RAMSET Register's format.

TABLE 19. RAMSET REGISTER (04h) - READ/WRITE

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
RAMSET (04h)	INTLV2	INTLV1	INTLV0	RTODIS	CONFB	RAMDRV1	RAMDRV0	PGMD
POR Value	0	0	0	0	–ROMCS	–PPICS	–BLKA20	1

Bit	Name	Function
7-5	INTLV2-INTLV0	DRAM Interleave: Sets DRAM interleave option: Bit 7 / Bit 6 / Bit 5 / Interleave Option 0 0 0 No interleave 0 0 1 Banks 0 and 1 only 0 1 0 Banks 0 and 3 only 0 1 1 Banks 1 and 2 only 1 0 0 Banks 2 and 3 only 1 0 1 Banks 0 and 1, or Banks 2 and 3 1 1 0 Banks 0 and 3, or Banks 1 and 2 1 1 1 Banks 0 and 1 and 2 and 3 (four-way interleave)
4	RTODIS	–RAS Time-out Disable: Disables RAS active time-out counter when set.
3	CONFB	Configuration: A read-only bit that indicates either Configuration A or B.
2, 1	RAMDRV1, RAMDRV0	RAM Drive: Sets MA10-MA0, –RAMW and –RAS3 - –RAS0 drive capability. Bit 2 / Bit 1 / Drive Time 0 0 12 mA 0 1 24 mA (MA, –RAMW), 12 mA (–RAS signals, MA0X, MA0Y) 1 0 36 mA (MA, –RAMW), 24 mA (–RAS signals, MA0X, MA0Y) 1 1 48 mA (MA, –RAMW), 24 mA (–RAS signals, MA0X, MA0Y)
0	PGMD	Page Mode: This bit controls DRAM Page Mode. When 0, Page Mode is always enable, –RAS signals are held low after any access. When 1, Page Mode is enabled only during a burst cycle; –RAS signals are held low during burst-reads, but negated at the end of the burst.

NTBREF Register
The NTBREF Register controls non-turbo speed, refresh mode, and refresh speed. Table 20 shows the NTBREF Register's format.

MISCSET Register DRAM Control Bits
The MISCSET Register has two bits that effect DRAM control which are accessed via indexed location 07h. Table 21 gives a brief description of those two bits. Refer to Table 42 for the MISCSET Register's complete format.

TABLE 20. NTBREF REGISTER (05h) - READ/WRITE

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
NTBREF (05h)	NTB2	NTB1	NTB0	TURBO	REFMD1	REFMD0	CASREF	REFSPD
POR Value	0	0	0		0	0	0	0

Bit	Name	Function
7-5	NTB2-NTB0	Non-Turbo: These bits control non-turbo CPU speed via –EADS. **Bit 7 / Bit 6 / Bit 5 / Speed** 0 0 0 Full speed (no holds/invalidates) 0 0 1 50% 0 1 0 66.6% 0 1 1 75% 1 0 0 80% 1 0 1 83.3% 1 1 0 85.7% 1 1 1 87.5%
4	TURBO	Turbo: This bit reflects the state of the TURBO pin (pin 155).
3, 2	REFMD1, REFMD0	Refresh Mode: These bits set the type of Refresh Mode. **Bit 3 / Bit 2 / Refesh Mode** 0 0 Synchronous (compatibility mode) refresh 0 1 Asynchronous refresh 1 X Decoupled refresh
1	CASREF	CAS Refresh: Enables CAS-before-RAS refresh when set to 1.
0	REFSPD	Refresh Speed: The refresh period is 15.625 µs when set to 0 and 125 µs when set to 1.

TABLE 21. MISCSET REGISTER (07h), DRAM CONTROL BITS

Bit	Name	Function
2	–ENPAR	Parity Enable: When set to 0, DRAM parity is enabled and when set to 1, it is disabled. (POR default is 0.)
1	CWE_OFF	DRAM RAS/CAS Conditional Wait States Off: When set to 0, RAS/CAS conditional wait states are enabled and when set to 1, they are disabled. (POR default is 0.)

SECONDARY CACHE SUPPORT

CACHE INTERFACE

The VL82C486 supports a simple cache interface that allows connection of several different types of cache controller. In particular, the VL82C486 is designed to work with the VL82C425 Second-Level Write-Back Cache Controller. The cache interface is comprised of the following signals:

–MISS Cache Miss - This input is made active (low) by a cache controller at the start of a CPU memory read cycle if the operand is not in secondary cache. When high at the start of any CPU memory access, it causes the VL82C486 to cancel the requested cycle. The –MISS input is tied low when no secondary cache is used. It is ignored during on-board DRAM read cycles for DMA/Master Mode cycles unless the –EALE pin is pulled low during power-on reset, in which case it inhibits DMA/Master Mode DRAM cycles if it is made high when –MEMR is active.

–MISS must be valid 13 ns before the end of T1 if TSTRT1 and TSTRT0 = 00 (bits 7 and 6 in the RAMTMG Register), or 13 ns before the middle of the first T2 if TSTRT1 and TSTRT0 = 01, or 13 ns before the end of the first T2 if TSTRT1 and TSTRT0 = 10. This last setting is used for compatibility with the VL82C425, with commodity SRAMs.

–BLKA20 This output is used to force the cache controller to deactivate A20. It is a decode of the A20GATE signal from the keyboard controller and Port A bit 1. It is also sent to the CPU –A20M input.

Figure 18 shows the VL82C486 connected with the VL82C425, SRAMs and the VL82C113A.

WRITE-THROUGH CACHE OPERATION

Write-through caches use the –MISS input. –MISS causes the VL82C486 to cancel a CPU memory read access if high in the first T2 of a CPU read cycle. The VL82C486 may be programmed to examine –MISS either in the middle of the first T2 or at the end of the first T2. The latter case allows for slow –MISS generation, but may add an extra wait state to on-board DRAM cycles.

If –MISS is high during the first T2 of a CPU memory read request, then the VL82C486 assumes a cache-hit and ignores the request. If it is low during the first T2 of a CPU memory request, then the VL82C486 performs the memory access as if there was no cache present.

On a read-miss, the cache controller loads the data from the D bus into the cache SRAMs simultaneously with the data being returned to the CPU from the DRAMs or slot bus. The cache controller must therefore monitor the –RDY and –BRDY signals to determine when the data is returned.

On a read-hit, the cache controller must perform burst or non-burst cycles, as requested by the CPU. It must therefore generate –BRDY after returning each 32-bit word and monitor –BLAST to terminate a burst cycle early at the CPU's request.

On CPU memory writes, the –MISS pin must be made low by the cache controller to make the VL82C486 perform the write to memory.

The VL82C486 does not enable its three-state –RDY and –BRDY outputs during cache-hits, allowing an external cache controller to drive these signals.

Figures 19 and 20 show functional timing diagrams for a cache-hit burst read cycles and a cache-miss non-burst read cycle, respectively.

WRITE-BACK CACHE SUPPORT

The VL82C486 is programmed by the –EALE pin during power-on reset to either ignore –MISS (–EALE high) during DMA/Master Mode on-board DRAM cycles, or inhibit on-board DRAM read cycles (–EALE low) during DMA/Master Mode cycles when –MISS is high and –MEMR is low. In the latter case, –MISS is still ignored during DMA/Master Mode on-board DRAM writes. This case is used for support of write-back secondary caches.

If –EALE is pulled low on power-on reset to select the write-back cache option, then the operation of the –MISS pin for CPU cycles also changes. When this option is selected, the –MISS signal inhibits all CPU accesses if high in T1 of any CPU cycle; it inhibits only memory cycles if low in T1 and high in T2. This feature may be used by a write-back cache controller to prevent the VL82C486 from starting any new CPU cycle when –BOFF is asserted to prepare for the write-back of dirty data. When the write-back option is not selected (–EALE high on POR), then –MISS is ignored in T1 and inhibits only memory cycles when high in T2.

The VL82C425 controls VL82C486 access to the local bus in order to perform write-back or line-swap by a serial hold request mechanism. (See Figure 18.) The HOLD output of the VL82C486 is connected to the SHOLD input of the VL82C425, rather than the HOLD input of the CPU. Similarly, the HLDA output of the CPU is connected to the CHLDA input of the VL82C425, and the SHLDA output of the VL82C425 is connected to the HLDA input of the VL82C486. When the VL82C486 asserts its HOLD output to request control of the bus, the VL82C425 clocks it in and generates the HOLD request to the CPU one cycle later via its CHOLD output.

If the VL82C425 does not have an interval HOLD request pending (in order to perform a write-back or line-swap operation), it will clock through the Hold Acknowledge from the CPU to the VL82C486 via its SHLDA output. If the VL82C425 does have a HOLD request pending, it will complete its bus operation (once it has received Hold Acknowledge from the CPU) before passing the asserting SHLDA to the VL82C486.

WRITE-BACK AND FLUSH INSTRUCTIONS

If the VL82C486 detects a write-back or flush instruction, it generates –RDY at the end of T2. No other action occurs.

FIGURE 18. CACHE CONTROLLER INTERFACE

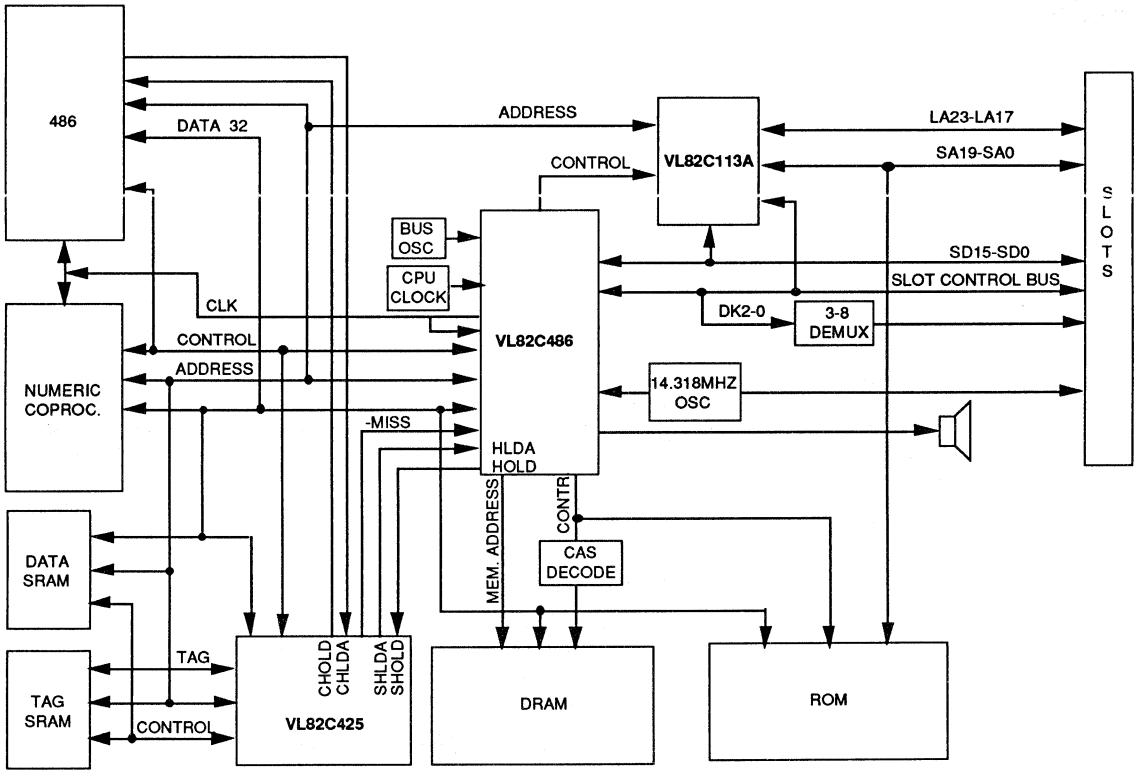


FIGURE 19. CACHE-HIT BURST-READ CYCLE

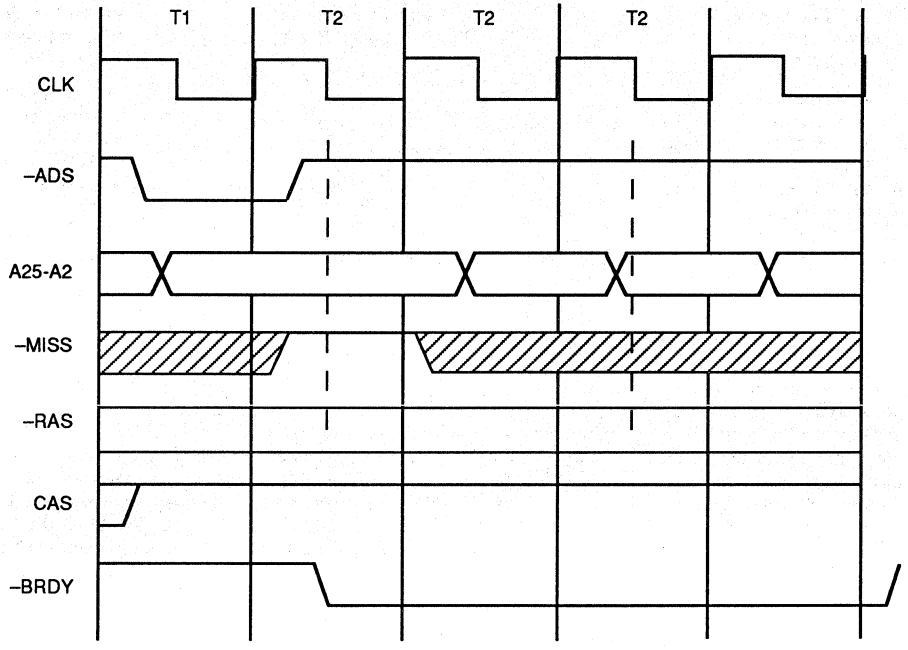
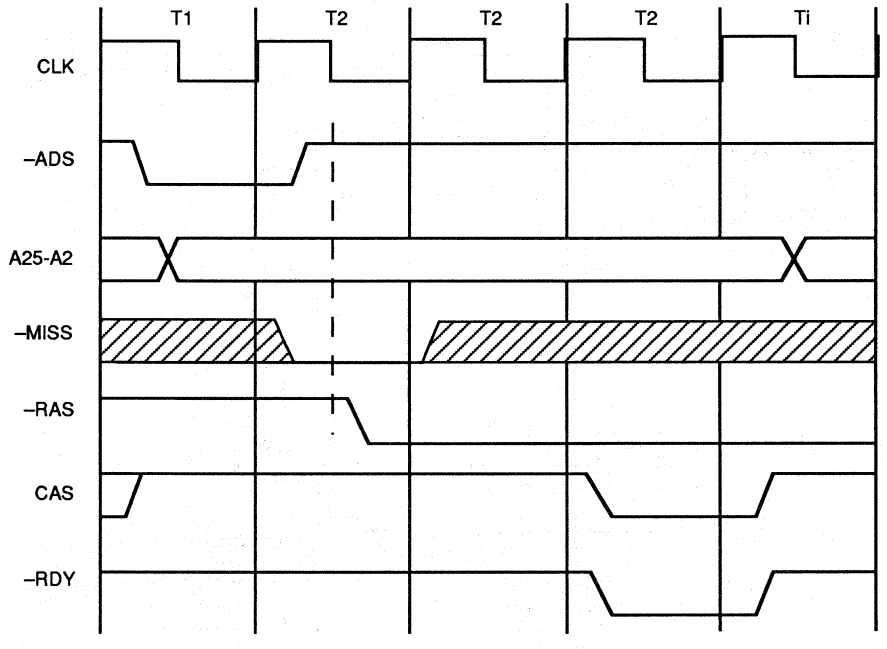


FIGURE 20. CACHE-MISS NON-BURST READ CYCLE



CLOCK GENERATION

CLOCK SIGNAL DEFINITION

The following clocks are used or generated by the VL82C486:

TCLK2 (input) — A crystal oscillator input of 2x the CPU clock frequency. In Turbo Mode, it is divided by 2 and sent to the CLK output. In Non-Turbo Mode, it is divided by 4, 6, or 8 and sent to the CLK output. A division of TCLK2 may be used to generate the ISA clock.

CLKIN (input) — The 1x 486 clock used to synchronize the interface to the CPU. It is also used to generate the DRAM strobes and timing. It is normally connected externally to the CLK output, either directly or through deskewing logic.

BUSOSC (input) — Supplied by a crystal oscillator of 2x the maximum desired frequency of the ISA bus SYSCLK signal. It may be divided by 2, 3, 4, 6, or 8 to generate SYSCLK. If SYSCLK is to be derived from TCLK2 instead of BUSOSC, then this input becomes a SYSCLK frequency-select signal as defined below.

OSC (input) — A 14.318 MHz clock common to the ISA bus signal OSC. It is divided by 12 to be used for the counter/timer clock, used by the –RAS time-out logic and "GATEA20/–RC" logic.

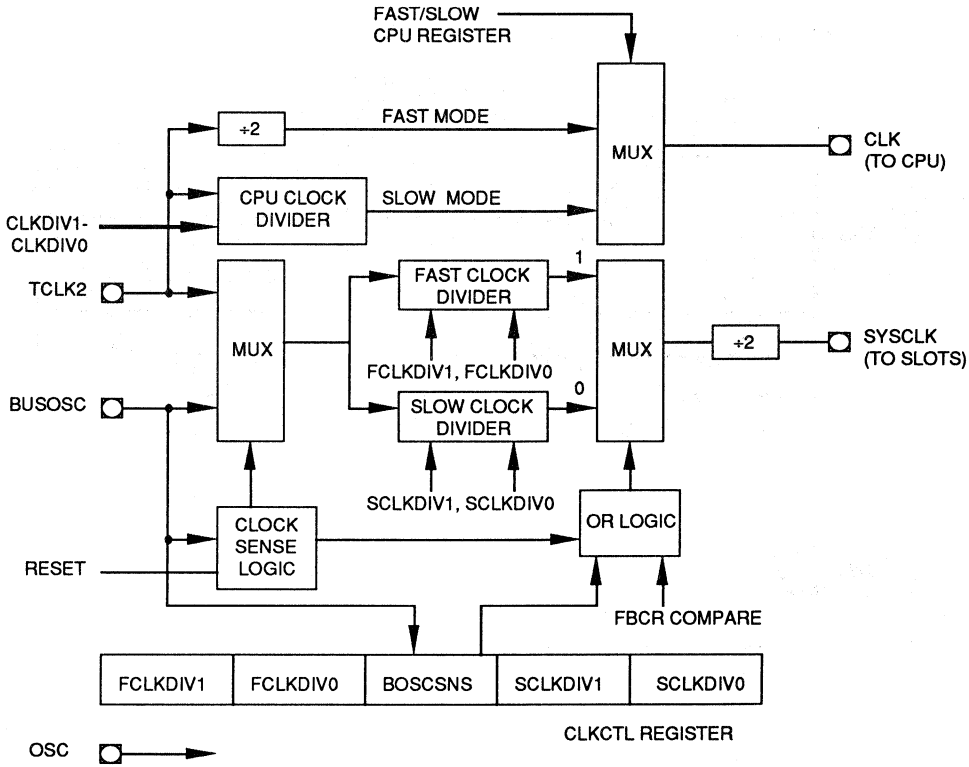
CLK (output) — The 1x CPU clock sent to the 486 and other on-board devices. Use of this signal for the system board clock is optional. However, if it is used as such, then it must also be sent to the VL82C486 CLKIN input, after appropriate deskewing if necessary.

SYSCLK (output) — The ISA bus system clock. It may be derived from a division of either TCLK2 or BUSOSC depending on the state of the BUSOSC pin and the setting of the CLKCTL Register, as described next.

PROGRAMMABLE AT BUS CLOCK

The VL82C486 provides a special feature for programming the AT bus clock, SYSCLK, for optimum performance. The frequency of SYSCLK can be varied using the BUSOSC pin, the CLKCTL Register, and the Fast Bus Clock Region (FBCR) Register. This allows different SYSCLK frequencies to be used for different peripheral accesses. The block diagram of the circuit that generates SYSCLK is shown in Figure 21.

FIGURE 21. CLOCK GENERATOR BLOCK DIAGRAM



SYSCLK Derived from BUSOSC
If the BUSOSC input is connected to a crystal oscillator, then SYSCLK is always derived from a division of BUSOSC. One of two dividers may be selected for dividing BUSOSC to derive SYSCLK: the Fast Clock Divider or the Slow Clock Divider. Selection between the Fast Divider and Slow Divider can be made by two different methods:

1) By writing a 0 to the BOSCSNS bit (bit 2) in the CLKCTL Register to select the Slow Clock Divider or by writing a 1 to BOSCSNS to select the Fast Clock Divider.
2) By making an access to a 64K block (as defined by the FBCR Register) with the FBEN bit (bit 7) in the CLKCTL Register set to 1. In this case, the Fast Clock Divider is selected regardless of the state of the BOSCSNS bit.

The division factor of the Slow Clock Divider is set by the SCLKDIV1 and SCLKDIV0 bits (bits 1 and 0) in the CLKCTL Register and may be BUSOSC ÷2, ÷4, ÷6, or ÷8. The division factor of the Fast Clock Divider is set by the FCLKDIV1 and FCLKDIV0 bits (bits 4 and 3) in CLKCTL Register and may be BUSOSC ÷2, ÷4, ÷6, or ÷8.

For example, the BUSOSC frequency may be set at 32 MHz. This would allow Slow and Fast Clock Divider frequencies of 4, 5.33, 8, and 16 MHz.

SYSCLK Derived from TCLK2
If the BUSOSC input is not connected to a crystal oscillator, then SYSCLK is always derived from a division of TCLK2. As before, either the Fast or Slow Clock Divider may be selected for dividing TCLK2 to derive SYSCLK. Selection between the Fast and Slow Clock Dividers in this case is made by the following methods:

1) By driving a 0 onto the BUSOSC pin to select the Slow Clock Divider or by driving a 1 onto the BUSOSC pin to select the Fast Clock Divider. When the BUSOSC pin is not connected to an oscillator, the BOSCSNS bit in the CLKCTL Register is no longer writeable and when read, it reflects the state of the BUSOSC pin.
2) By making an access to a 64K block (as defined by the FBCR Register) with the FBEN bit in the CLKCTL Register set to a 1. In this case, the Fast Clock Divider is selected, regardless of the state of the BUSOSC pin.

The division factor of the Slow Clock Divider is set by the SCLKDIV1 and SCLKDIV0 bits in the CLKCTL Register and may be TCLK2 ÷4, ÷6, ÷8, or ÷12. The division factor of the Fast Clock Divider is set by the FCLKDIV1 and FCLKDIV0 bits in the CLKCTL Register and may be TCLK2 ÷2, ÷4, ÷6, or ÷8.

Fast Bus Clock Region (FBCR)
The FBCR Address Register and the associated enable bit (FBEN in the CLKCTL Register) are available to allow accesses to a certain memory region to be run at a different ISA clock rate. The device must reside in a 64K block on a 64K boundary. The ISA bus cycle is run as normal except the Fast Bus Clock Divider is used during the access. Bus master and DMA accesses are not included in this function.

When enabled, address bits A23-A16 of memory accesses are compared with the address stored in the FBCR Address Register while address bits A31, A29, A25 and A24 are compared to 0. Table 22 shows the format for the FBCR Address Register.

Power-On Reset Configuration
After a power-on reset, the SYSCLK generation logic is initialized to the following state:

- The FCLKDIV1 and FCLKDIV0 bits in the CLKCTL Register are set to 11 (÷8).
- The SCLKDIV1 and SCLKDIV0 bits in the CLKCTL Register are set to 11 (÷8/12).
- If an external oscillator is connected to the BUSOSC pin, the BOSCSNS bit in the CLKCTL Register is set to 0, selecting the Slow Clock Divider value. The SYSCLK output will therefore have an initial frequency of BUSOSC ÷8.
- If no external oscillator is connected to the BUSOSC pin, the BOSCSNS bit in the CLKCTL Register will reflect the state of the BUSOSC pin, selecting the Slow Clock Divider if low or the Fast Clock Divider divider if high. The SYSCLK output will therefore have an initial frequency of TCLK2 ÷12 if the BUSOSC pin is low or TCLK2 ÷8 if the BUSOSC pin is high.
- The FBCR Address Register is disabled (the FBEN bit in the CLKCTL Register is reset to 0).

TABLE 22. FBCR ADDRESS REGISTER (0Bh) - READ/WRITE

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
FBCR (0Bh)	A23	A22	A21	A20	A19	A18	A17	A16
POR Value	0	0	0	0	0	0	0	0

AT Bus Clock Frequency Summary
Table 23 summarizes the different programming and frequency options available for SYSCLK.

CPU Clock (CLK) Frequency Control
After power-on reset the frequency of the CLK output is set to TCLK2 ÷2. However, if a dummy write to I/O Port location F4h is subsequently made (with the –VSF bit in the MISCSET Register set to 0), then Slow Clock Mode is enabled and the frequency of CLK is then controlled by the CLKDIV1 and CLKDIV0 bits (bits 6 and 5) in the CLKCTL Register, which allows CLK to be set to the frequency of TCLK2 ÷2, ÷4, ÷6, or ÷8. A dummy write to location F5h returns CLK to full speed (TCLK ÷2, Fast Clock Mode). If a write to either location F4h or F5h causes a frequency change (i.e., when the CLKDIV1 and CLKDIV0 bits are not set to 00), or if a write to the CLKCTL Register when running in Slow Mode causes a frequency change, then the VL82C486 generates a 1 ms CPU-only reset as required by the 486, starting immediately after the write is acknowledged and just before the frequency is changed. Thus, to make clock frequency switching invisible to applications programs, system software must save and restore the CPU state before and after the reset is generated.

This method of slowing the CPU's execution rate is supplied in addition to the Non-Turbo Mode of operation implemented by continuous modulation of the 486's –EADS signals. This is described in the section titled "Turbo/ Non-Turbo Mode Control" on page 65.

The TURBO pin automatically controls switching of the Turbo and Non-Turbo Modes. Using this modulation method and has no effect on CPU clock frequency. However, the state of the TURBO pin is software readable via bit 4 (TURBO) in the NTBREF Register and may be polled by system software which can then manually change the clock frequency by writing to location F4h or F5h when it senses a state change on this pin.

Note: Slow CPU Clock Mode has no impact on the synchronous slot clock frequency, which is derived from TCLK2 and is always constant.

TABLE 23. AT BUS CLOCK FREQUENCIES

BUSOSC Pin	BOSCSNS	FBCR Access	FCLKDIV1, FCLKDIV0	SCLKDIV1, SCLKDIV0	SYSCLK
Connected to Crystal Oscillator	0	No	XX	00	BUSOSC ÷2
	0	No	XX	01	BUSOSC ÷4
	0	No	XX	10	BUSOSC ÷6
	0	No	XX	11	BUSOSC ÷8
	X	Yes	00	XX	BUSOSC ÷2
	X	Yes	01	XX	BUSOSC ÷4
	X	Yes	10	XX	BUSOSC ÷6
	X	Yes	11	XX	BUSOSC ÷8
	1	X	00	XX	BUSOSC ÷2
	1	X	01	XX	BUSOSC ÷4
	1	X	10	XX	BUSOSC ÷6
	1	X	11	XX	BUSOSC ÷8
0		No	XX	00	TCLK2 ÷4
0		No	XX	01	TCLK2 ÷6
0		No	XX	10	TCLK2 ÷8
0		No	XX	11	TCLK2 ÷12
X		Yes	00	XX	TCLK2 ÷2
X		Yes	01	XX	TCLK2 ÷4
X		Yes	10	XX	TCLK2 ÷6
X		Yes	11	XX	TCLK2 ÷8
1		X	00	XX	TCLK2 ÷2
1		X	01	XX	TCLK2 ÷4
1		X	10	XX	TCLK2 ÷6
1		X	11	XX	TCLK2 ÷8

Clock Control Register (CLKCTL)
The CLKCTL Register is used to determine SYSCLK frequency (as described in the section titled "Programmable AT Bus Clock" starting on page 61), for setting CLK frequency, and for enabling SYSCLK frequency switching in the Fast Bus Clock Region (FBCR) address range.

TABLE 24. CLKCTL REGISTER (06h) - READ/WRITE

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
CLKCTL (06h)	FBEN	CLKDIV1	CLKDIV0	FCLKDIV1	FCLKDIV0	BOSCSNS	SCLKDIV1	SCLKDIV0
POR Value	0	0	0	1	1	See Descrip.	1	1

Bit	Name	Function
7	ENVDSP	Enable SYSCLK Frequency Switching in Fast Bus Clock Region Address Range: When set high, this bit selects the Fast Divider SYSCLK frequency when a memory access is made to the Fast Bus Clock Regiojn address range. When set low, FBEN disables the FBCR feature. The default value of this bit is 0.
6, 5	CLKDIV1, CLKDIV0	CLK Divider: These bits specify the CLK generated when a write to port F4h is performed. Bit 6 / Bit 5 / CLK2 0 / 0 / TCLK2 ÷2 0 / 1 / TCLK2 ÷4 1 / 0 / TCLK2 ÷6 1 / 1 / TCLK2 ÷8 The power-on reset default value of these bits is 00, selecting full speed operation.
4, 3	FCLKDIV1, FCLKDIV0	Fast Clock Divider: These bits determine the frequency of SYSCLK when an access is made to the Fast Bus Clock Region with FBEN of this register set to 1, or when BOSCNS bit reads as a 1. Bit 4 / Bit 3 / SYSCLK 0 / 0 / BUSOSC ÷2 or TCLK2 ÷2 0 / 1 / BUSOSC ÷4 or TCLK2 ÷4 1 / 0 / BUSOSC ÷6 or TCLK2 ÷6 1 / 1 / BUSOSC ÷8 or TCLK2 ÷8 Where BUSOSC is selected if connected or TCLK2 if not. The default value of these bits is 11.
2	BOSCSNS	BUSOSC Status: This bit reflects the state of the BUSOSC pin when there is no external oscillator connected to the BUSOSC pin. In that case, this bit is read-only. If an oscillator is present, this bit becomes a read/write bit that selects SCLKDIV divider when set to 0 and the FCLKDIV divider when set to 1. The default value of this bit is 0 if an external BUSOSC oscillator is present, or the BUSOSC pin state if no BUSOSC oscillator is present.
1, 0	SCLKDIV1 SCLKDIV0	Slow Clock Divider: These bits determine the frequency of SYSCLK when BOSCSNS bit reads as a 0 and an access is not in the Fast Bus Clock Region (when enabled). Bit 1 / Bit 0 / SYSCLK 0 / 0 / BUSOSC ÷2 or TCLK2 ÷4 0 / 1 / BUSOSC ÷4 or TCLK2 ÷6 1 / 0 / BUSOSC ÷6 or TCLK2 ÷8 1 / 1 / BUSOSC ÷8 or TCLK2 ÷12 Where BUSOSC is selected if an external oscillator is connected to the BUSOSC pin, or TCLK2 if not. The default value is of these bits is 11.

TURBO/NON-TURBO MODE CONTROL

It has become standard for fast PC/AT-compatibles to provide means to slow operation for older speed sensitive software. This is especially true for graphics intensive entertainment software which may otherwise operate much too fast on a high speed machine. One way this mode may be toggled on and off is by external control of the TURBO input pin. The Slow Mode is activated and the VL82C486 generates continuous invalidates (via –EADS) to the CPU when TURBO is low. When TURBO is high, the –EADS signal is not modulated (unless the VLSI Special Feature's TURBO request is not active). This feature provides the capability of emulating the effect of running at slower CPU clock frequencies even though the clock frequency is not changed. It is provided in addition to a method of actually changing the CPU clock frequency, as previously described in section titled "Clock Generation" starting on page 61.

The TURBO pin is normally connected to the keyboard controller and triggered by the BIOS via detection of a key combination such as Ctrl Alt + / Ctrl Alt -. This input is often externally ANDed with a mechanical Turbo switch on the front panel.

The VL82C486 offers a way to control –EADS modulation by software also. The –VSF bit (bit 7) in the BUSCTL Register must be enabled for software control. Slow operation can be enabled by either pulling the TURBO pin low or by performing a dummy write to I/O Port F4h. A dummy write to F5h returns to full speed operation if the TURBO pin is high. When the –VSF bit is disabled, CPU speed control is solely under control of the TURBO pin.

The Non-Turbo Mode speed is set by bits 7, 6, and 5 (NTB2-NTB0) in the NTBREF Register. The effect of these three bits ranges from no slowing (000) through to slowing by a factor of eight (111).

Note that writes to locations F4h and F5h may also be used to switch the clock frequency (refer to the section titled "CPU Clock (CLK) Frequency Control" on page 62), these locations thus performing a dual function. However, if it is desired that the operation of CPU speed be controlled only by the modulation of –EADS, then the CLKDIV1 and CLKDIV0 bits in the CLKCTL Register may be set to 0. This disables any clock frequency change when F4h is written. Similarly, if it is desired that CPU speed be controlled only by changing the clock frequency, then the NTB2-NTB0 bits (bits 7-5) in the NTBREF Register may be set to 0.

The –VSF bit in the BUSCTL Register must be enabled for software Turbo/ Slow Mode control.

The NTB bits in the NTBREF Register have the following meaning:

Bit	Name	Function
7-5	NTB2-NTB0	Sets CPU speed of operation in Non-Turbo Mode by modulation of the –EADS signal to give the following duty cycles: 000 - full speed (no holds/invalidates) 001 - 50% 010 - 66.6% 011 - 75% 100 - 80% 101 - 83.3% 110 - 85.7% 111 - 87.5%

ISA BUS INTERFACE

OVERVIEW

The ISA bus is accessed in the CPU Mode, DMA Mode, Bus Master Mode, and Refresh Mode.

In the CPU Mode, the ISA bus controller is responsible for generating the command signals –IOR, –IOW, –MEMR, –MEMW, –SMEMR and –SMEMW, and BALE. The VL82C486 samples the –MEMCS16, –IOCS16, and IOCHRDY inputs. The –WS0 signal determines the length in wait states of each bus cycle.

In the DMA Mode, the DMA controllers generate the command and address signals. BALE is forced high for all DMA cycles. The VL82C486 asserts the AEN signal to indicate that the current address on the bus is for memory only and not to be decoded as an I/O address. The DMA logic samples IOCHRDY to extend bus cycles longer than the internally defined cycle length.

The Bus Master Mode is an extension of the DMA Mode. A bus master can get control of the bus by requesting a DMA operation. Once the DMA is acknowledged, the –MASTER signal is pulled active and the VL82C486 relinquishes control of the bus to the master.

The VL82C486's SD bus output buffers will be enabled during the CPU Mode when the transfer is a write to off-board DRAM. The output buffers will also be enabled during DMA and Master Mode transfers when the transfer is a read from on-board DRAM, an on-chip I/O location, or local bus memory from a local bus device.

During the Refresh Mode, the VL82C486 drives the –REFRESH signal, a refresh address, and –MEMR command onto the bus to start the refresh cycle. The refresh circuit samples IOCHRDY to determine if the –MEMR and –REFRESH pulses need to be extended. The BALE output is driven high during refresh cycles.

ISA BUS CYCLE DESCRIPTION

CPU Access Cycles

CPU access cycles to the ISA bus are of two types: memory cycles and I/O cycles. A memory cycle may be for 8-, 16-, or 32-bit memory while an I/O cycle normally accesses 8- or 16-bit peripherals.

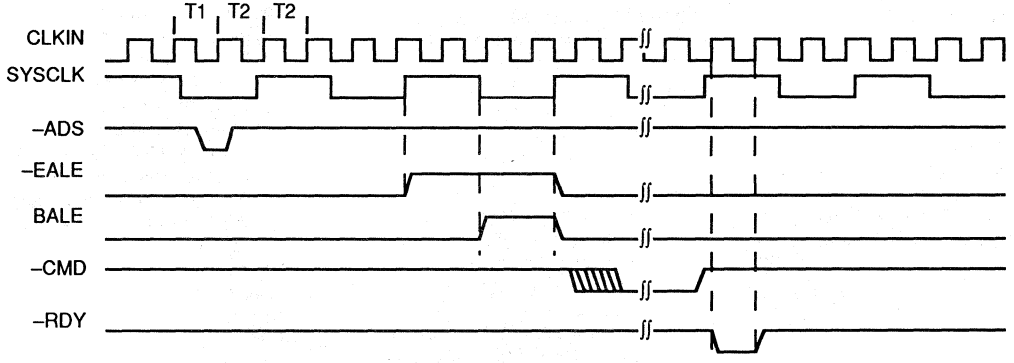
ISA bus access cycles may be synchronous with the CPU clock or may be asynchronous, depending on whether an external clock is connected to the BUSOSC pin. The bus cycles are all related to the SYSCLK clock which is derived from either BUSOSC or TCLK2.

An ISA bus cycle starts with a rising edge of –EALE coincident with the first rising edge of SYSCLK after the second T2 state. The –EALE edge is used for clocking the CPU address into the VL82C113A to generate LA23-LA17. BALE is generated at the next falling edge of SYSCLK and is one-half of a SYSCLK wide. –CMD, which may be either –MEMR, –MEMW, –IOR, or –IOW activates after BALE goes low. Deassertion of –CMD indicates the end of a bus cycle. –RDY is generated by the VL82C486 on the rising edge of CLKIN to signal the CPU the end of the current cycle. A typical CPU access cycle for the ISA bus is shown in Figure 22.

When operating in PC/AT-compatible Mode, 8-bit DRAM or I/O cycles are four SYSCLK wait states long while all 16-bit cycles are zero wait states. Eight-bit ROM cycles are three wait states long. The cycle lengths may be extended by pulling the IOCHRDY signal low.

Descriptions of 8- and 16-bit normal and ready types of cycles are detailed in the sections following.

FIGURE 22. CPU ACCESS OF ISA BUS



CPU Memory Access Cycles
The memory related control signals are –MEMR, –SMEMR, –MEMW, –SMEMW, and –MEMCS16. –SMEMR and –SMEMW are active only if the access is within the first 1 MB of memory. The state of –MEMCS16 at the beginning of the bus cycle state TC, (as shown in Figure 23) determines whether the present cycle is 8- or 16-bit. The command signals go active at the start of TC for 16-bit cycles and in the middle of TC for 8-bit cycles. The falling edge of a command signal can be delayed by one or two SYSCLKs by setting bits 2 or 3 (CMDLY1 and CMDLY2), respectively, in the BUSCTL Register as described in Table 25 (BUSCTL Register format). Under default settings, the command signals are deasserted in the beginning of TW5 for an 8-bit operation and in the beginning of TW2 for a 16-bit operation. If the SYSCLK frequency is 16 MHz, it may be necessary to delay the rising edge of the command signals by one SYSCLK. This can be achieved by setting bits 0 or 1 (8WS or 16WS) in the BUSCTL Register. For slow peripherals, additional wait states may be inserted by pulling IOCHRDY low by the middle of TW4 for an 8-bit cycle and by the beginning of TW2 for a 16-bit cycle.

The VL82C486 converts a CPU request for 16- or 32-bit data from an 8-bit memory into two 8-bit or four 8-bit cycles, respectively, as depicted in Figures 24 and 25. A cycle for 32-to-16 bit conversion is shown in Figure 26.

If the memory accessed is ROM, the timing is different for command signals. They go active at the falling edge of BALE. Both 8- and 16-bit ROM access cycles are three wait states long. They can be programmed to be one or two wait states long using bits 1 and 0 (ROMWS1 and ROMWS0) in the ROMSET Register. See Figures 27, 28, and 29.

It should be noted that SA1 timing is controlled by the state of the –IGNNE pin at power-on reset. If –IGNNE is held low, SA1 has a valid value at the rising edge of BALE. This is in accordance with the ISA bus specifications. If –IGNNE is high at power-on, SA1 is valid during state T1 of the CPU cycle. It is a direct decode of the –BE3 - –BE0 inputs from the CPU. During a conversion cycle, SA1 is valid at the rising edge of a command and remains valid until one-half a SYSCLK after the falling edge of BALE. The VL82C113A clocks in SA1 at the rising edge of –EALE.

CPU I/O Access Cycles
The I/O related control signals are –IOR, –IOW and –IOCS16. –IOR is active during an I/O read cycle and –IOW during a write cycle. –IOCS16 when low indicates a 16-bit data transfer, otherwise an 8-bit data transfer is initiated by the CPU.

The VL82C486 decodes the CPU control signals and issues a command in the middle of TC or the beginning of TW1 depending on the bit 3 (CMDLY2) of the BUSCTL Register. An 8-bit cycle is four wait states long while a 16-bit cycle has no wait states if the default configuration is used. Additional wait states may be inserted by setting bits 0 and/or bit 1 in the (8WS or 16WS) BUSCTL Register or by deasserting IOCHRDY. This is depicted in Figure 30.

The VL82C486 converts a CPU request for 16-bit data from an 8-bit peripheral into two 8-bit cycles as depicted in Figure 31.

The slot address line's (SA1) functionality is the same as mentioned earlier in the section titled "CPU Access Cycles" on page 66.

DMA Access Cycles
In the PC/AT, DMA transfers occur between peripherals and memory. The data width can be either 8 or 16 bits. Out of the seven external DMA channels available, four are used for 8-bit transfers while the remaining three are used for 16-bit transfers. One byte or word is transferred in each DMA cycle.

Normally an add-on card issues a DMA request by pulling one of DRQ7-DRQ5, DRQ3-DRQ0 signals high. When the VL82C486 detects this request, it generates HOLD to the CPU and when HLDA is received by the VL82C486, the DMA acknowledge code is issued on signals DK2-DK0. This is decoded by an external 3-to-8 decoder (as explained in the section titled "DMA Controllers" on page 80). Assertion of DKEN indicates valid data on DK2-DK0.

A typical DMA transfer cycle is shown in Figure 32. AEN and BALE go high with HLDA. The DMA address is put on A23-A2 and SA1-SA0. Two DMACLK cycles, or four SYSCLK cycles later, –MEMR and –IOW, or –IOR and –MEMW are asserted depending on the memory-to-I/O or I/O-to-memory transfer. If bit 0 (MEMTM) in the DMACTL Register is set 1, –MEMR is asserted one DMACLK cycle earlier. –EADS is also asserted for cache invalidation on writes. The command remains active for six DMACLK cycles. The data transfer takes place at the rising edge of command signals. TC is activated before the end of the command if the transfer is from one 8- or 16-bit device to another 8- or 16-bit device. If the transfer is from a 16-bit device to an 8-bit device, the command signals are again asserted after two DMACLK cycle delays and the transfer is completed.

Master Mode Cycles
Add-on cards become bus masters in the Master Mode. An add-on card issues a DMA request on the ISA bus. The VL82C486 responds with an acknowledge signal just like a DMA cycle. The add-on card then gains control of the bus by asserting the –MASTER signal. Unlike in DMA cycles, there can be multiple data transfers in the Master Mode. Figure 33 shows a Master Mode cycle.

Refresh Cycles
Data in DRAM on the ISA bus is refreshed every 15.72 µs. A refresh cycle begins with the assertion of the –REFRESH signal as shown in Figure 34. A refresh request can be generated either by the VL82C486 in the CPU Mode or by an add-on card in the Master Mode. The refresh address is put on A11-A2 and SA1-SA0 by the VL82C486 in response to a low –REFRESH signal. The page address is put on A23-A17 at the same time. A23-A17 is used to generate LA23-LA17 by external logic. The VL82C486 generates a 12-bit refresh address; however, only an 8-bit address is put on SA7-SA0 in compliance with the ISA bus requirements. –MEMR is asserted one SYSCLK cycle after –REFRESH goes active. –MEMR remains low for two SYSCLK cycles. The refresh request is removed one SYSCLK cycle after that.

FIGURE 23. ISA BUS MEMORY ACCESS CYCLE

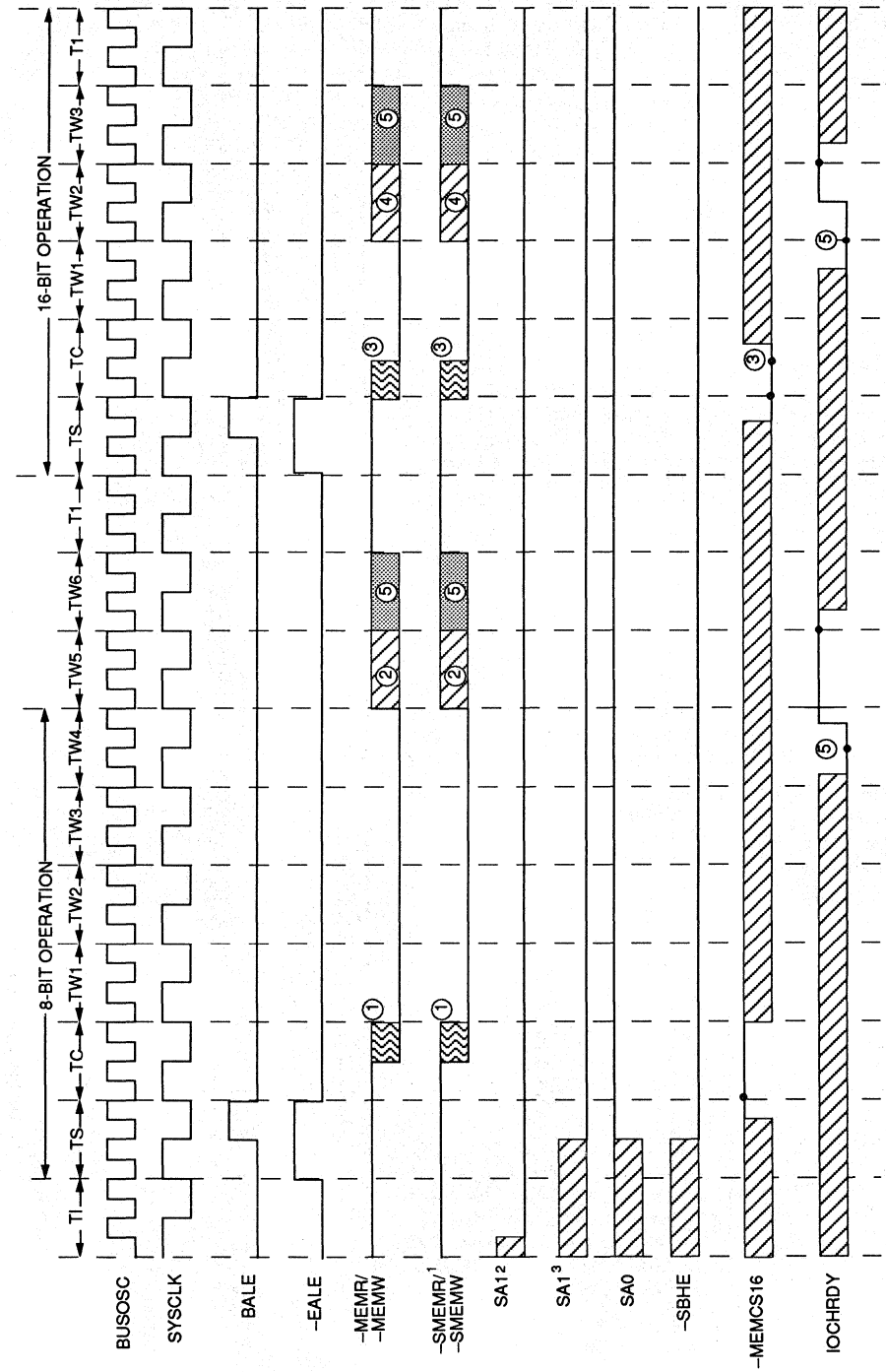


FIGURE 24. MEMORY CYCLE: 16-TO-8 BIT CONVERSION

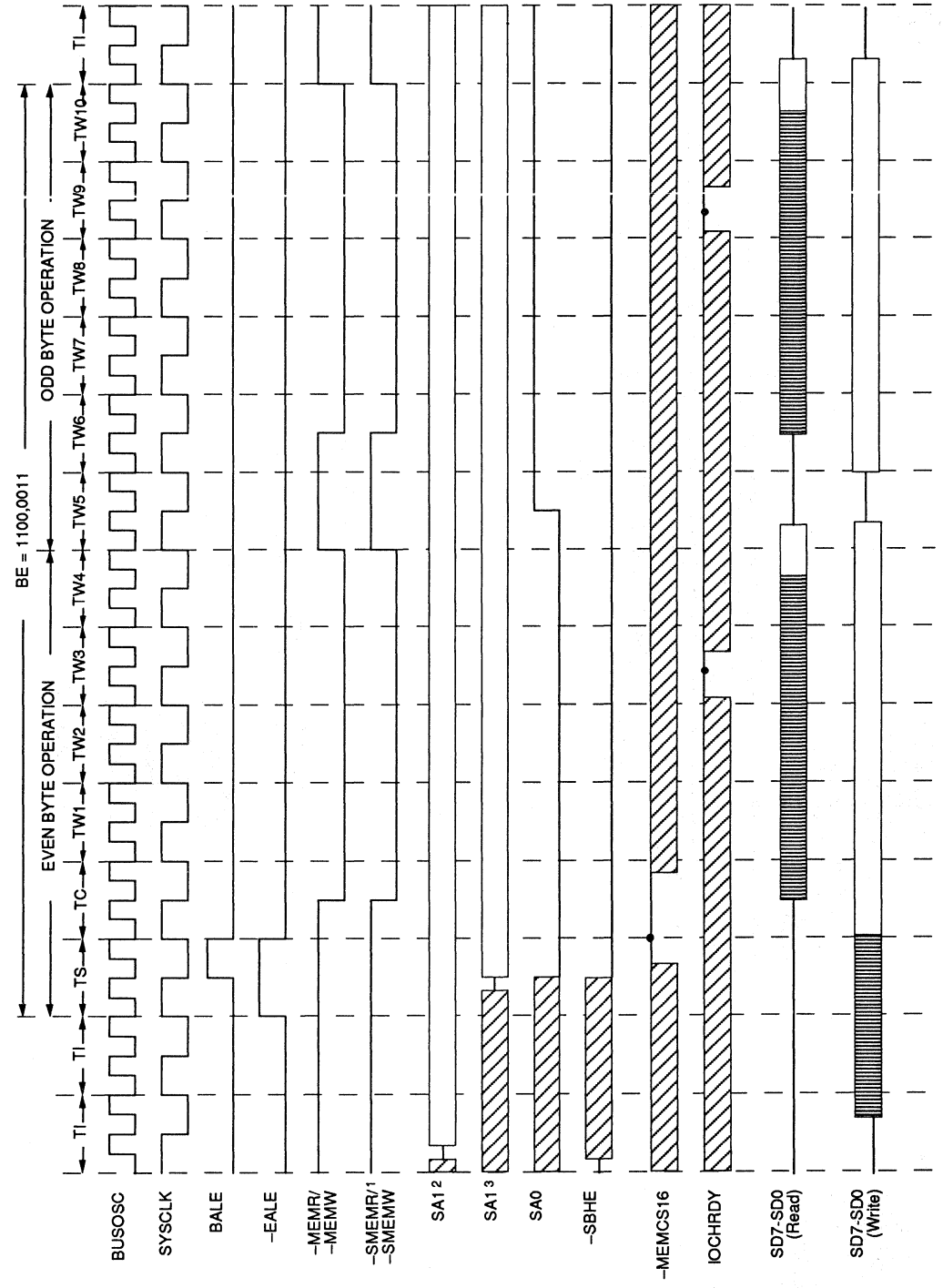


FIGURE 25. MEMORY CYCLE: 32-TO-8 BIT CONVERSION

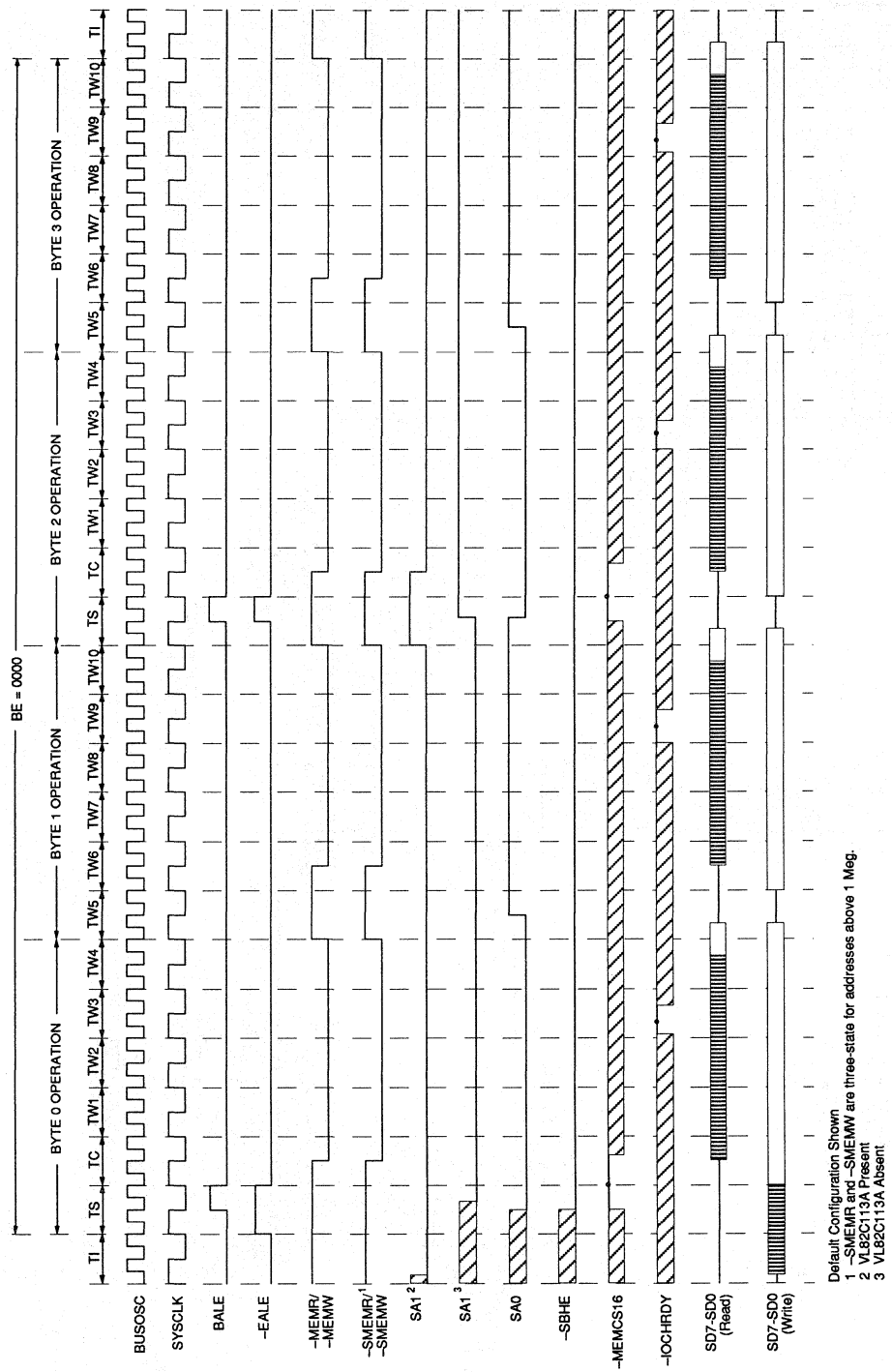


FIGURE 26. MEMORY CYCLE: 32-TO-16 BIT CONVERSION

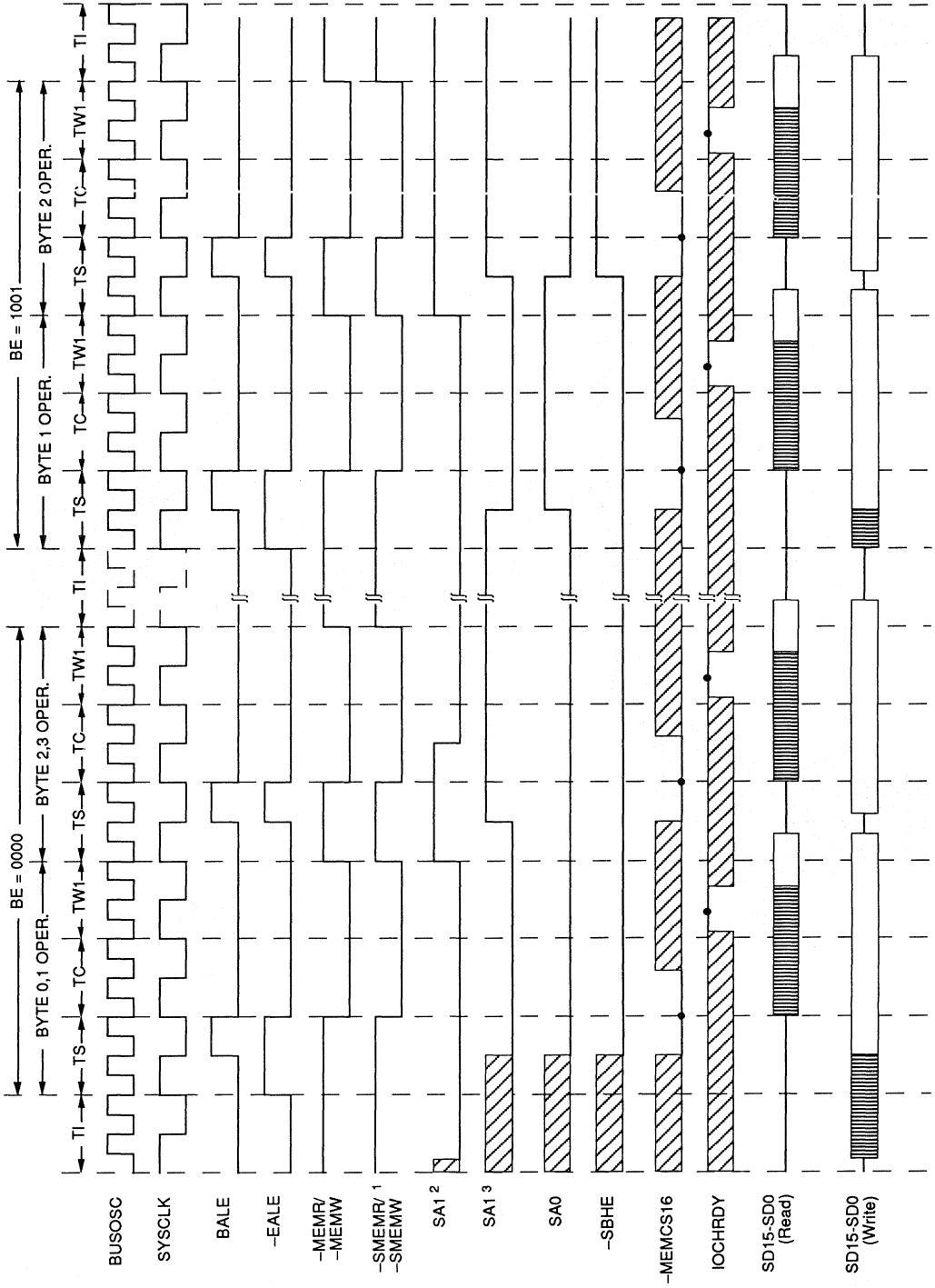


FIGURE 27. ROM ACCESS CYCLE

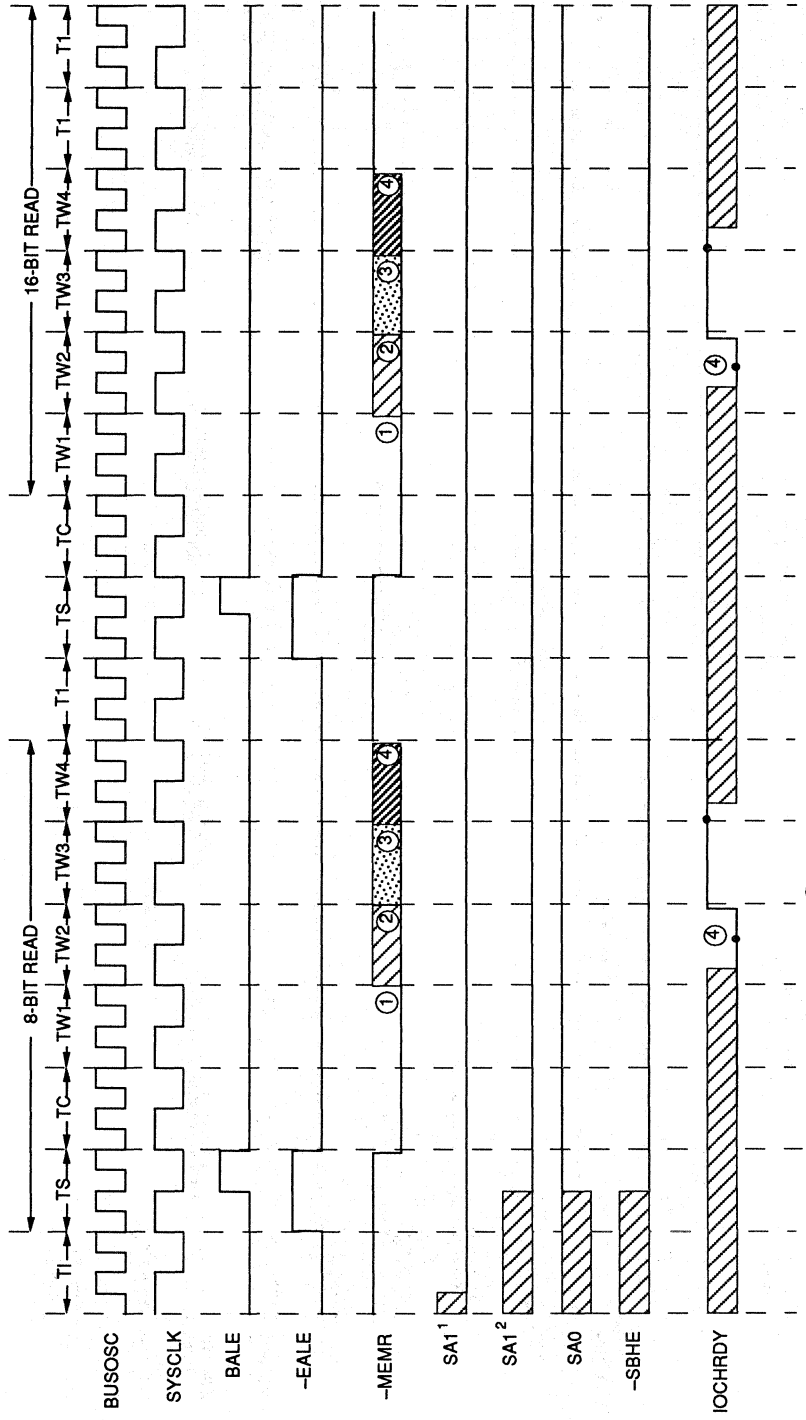


FIGURE 28. ROM CYCLE: 32-TO-8 BIT CONVERSION

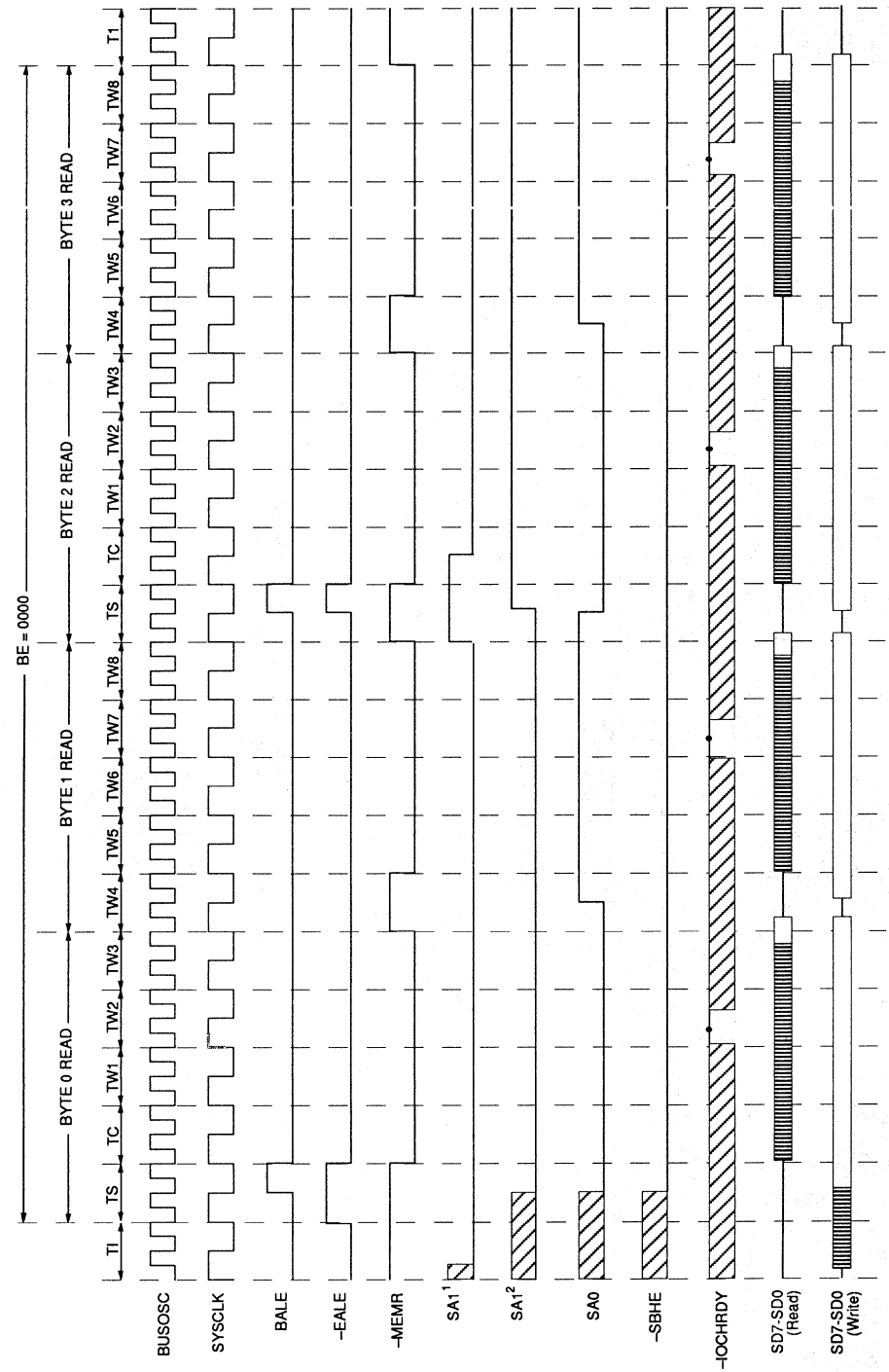


FIGURE 29. ROM CYCLE: 32-TO-16 BIT CONVERSION

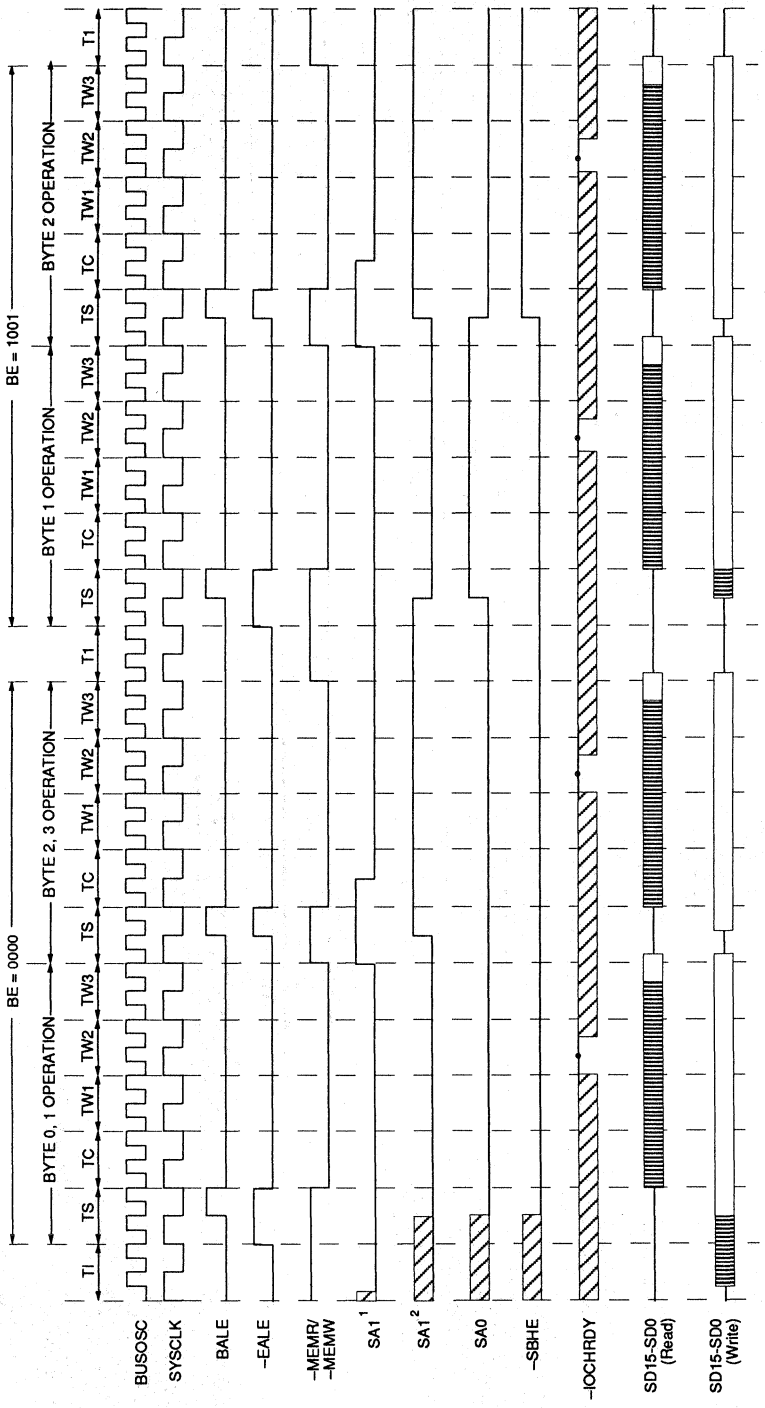


FIGURE 30. ISA BUS I/O ACCESS CYCLE

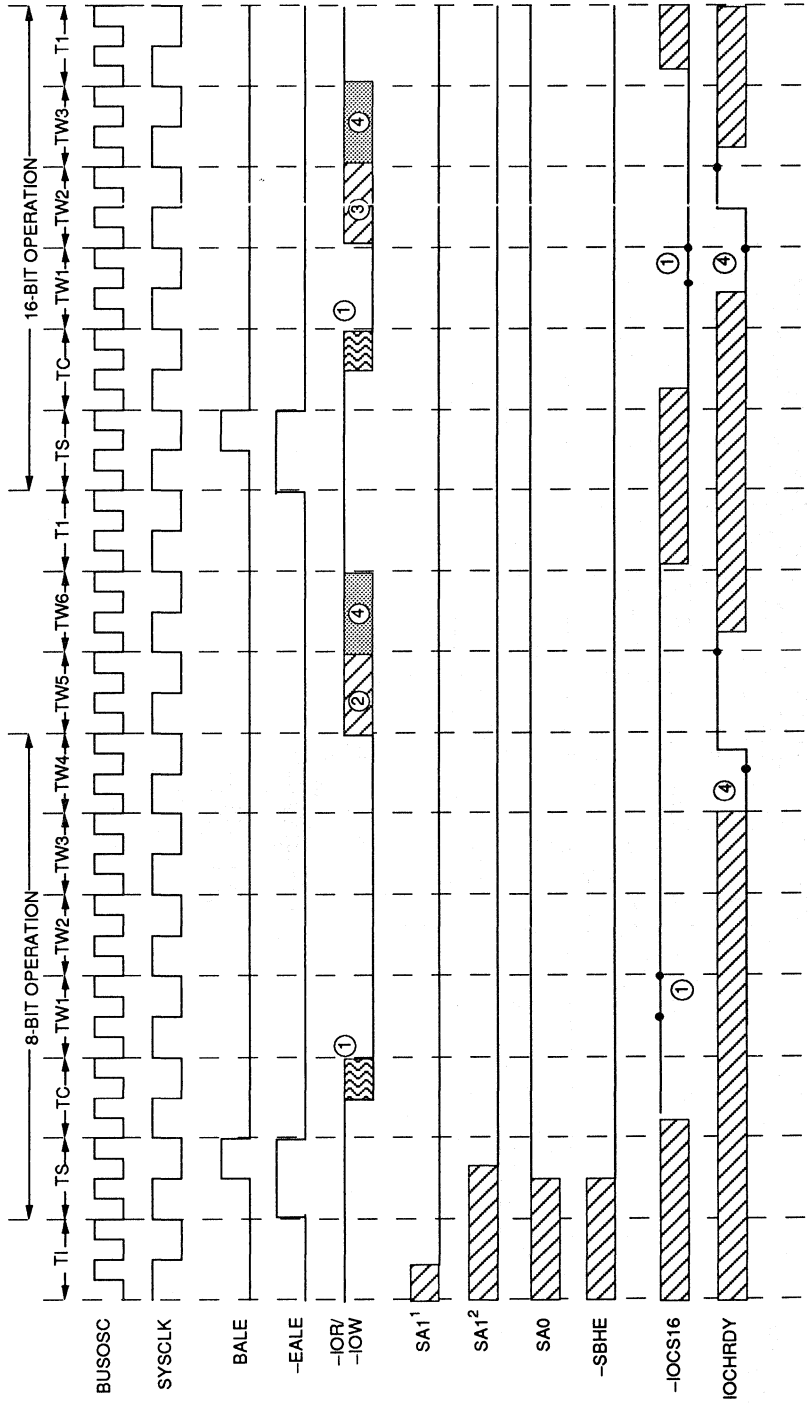


FIGURE 31. I/O CYCLE - 16-TO-8 BIT CONVERSION

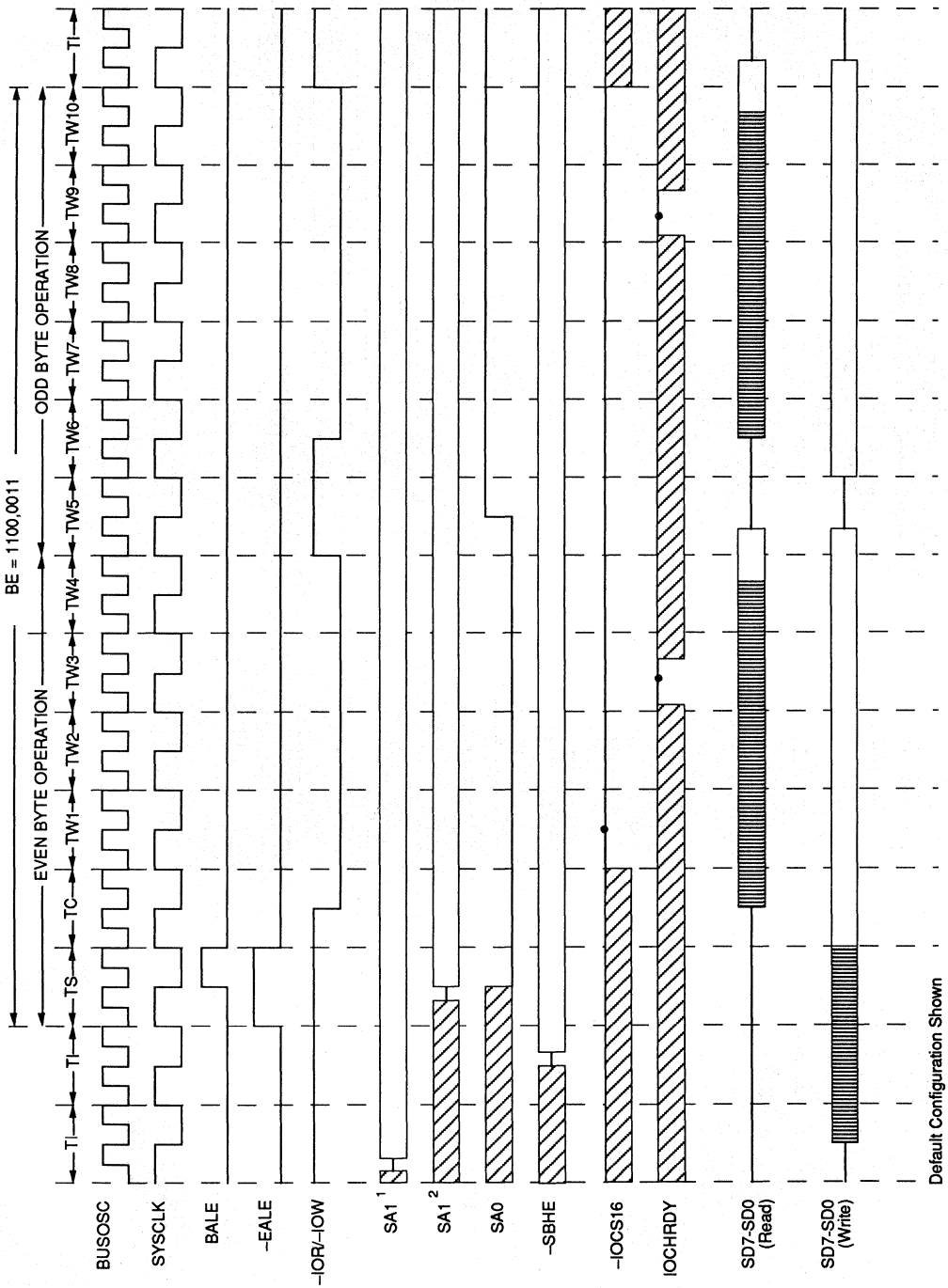
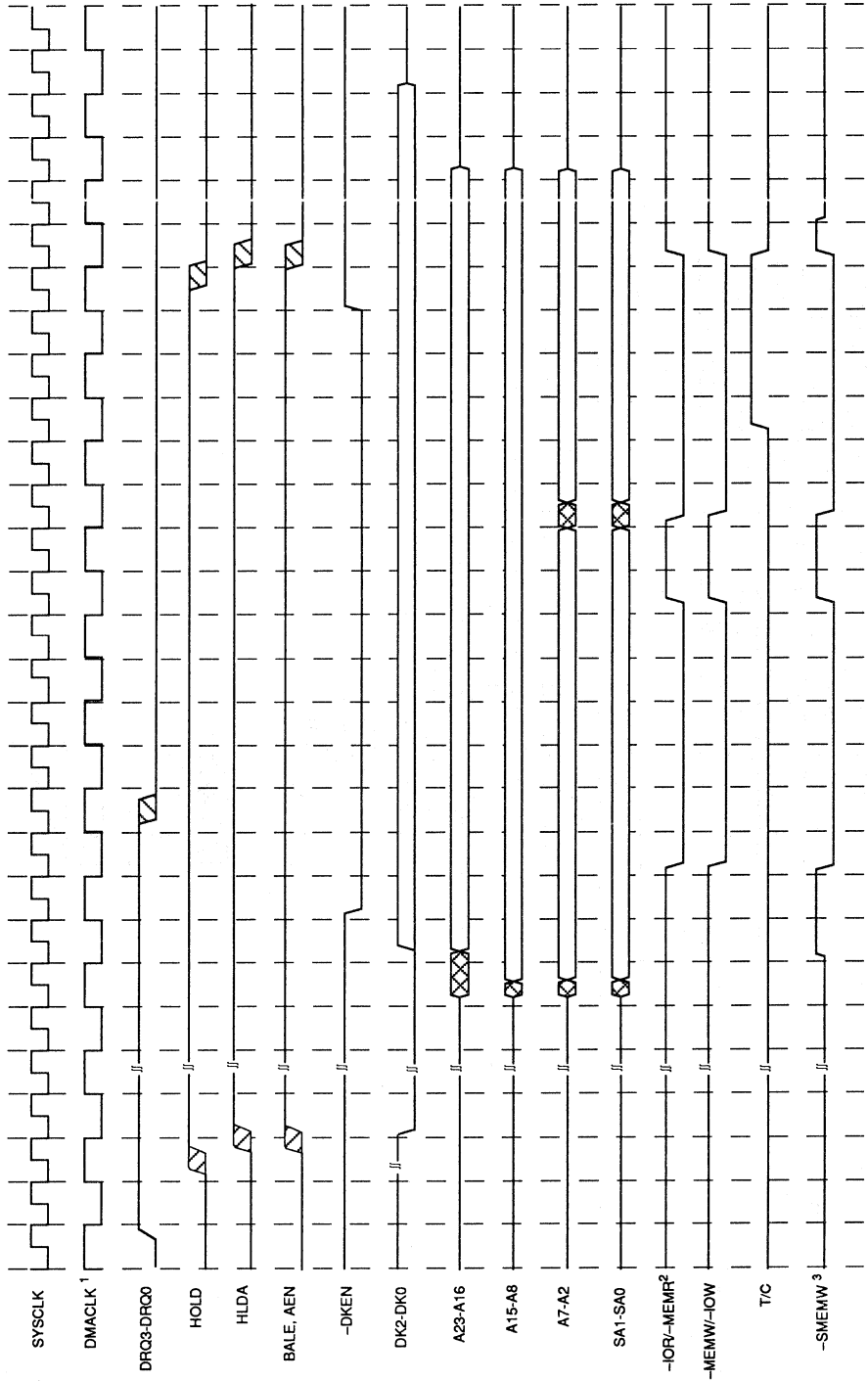


FIGURE 32. DMA TRANSFER CYCLE



1 Internal signal
2 –MEMR timing shown for when bit 0 of the DMACTL Register is 0.
3 –SMEMR/–SMEMW are three-state for addresses above 1Meg. They should be pulled up externally with a 10 kΩ resistor.

FIGURE 33. MASTER MODE CYCLE

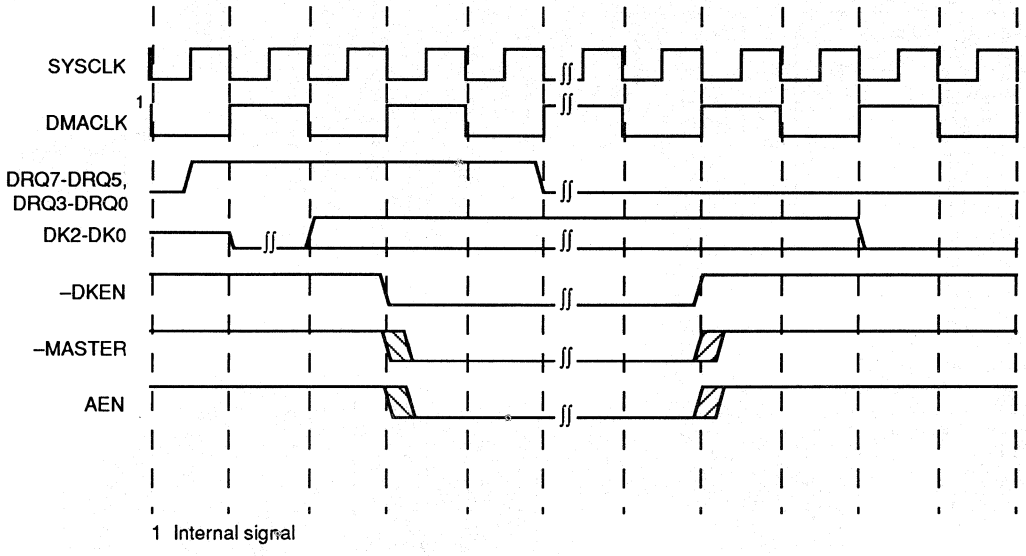
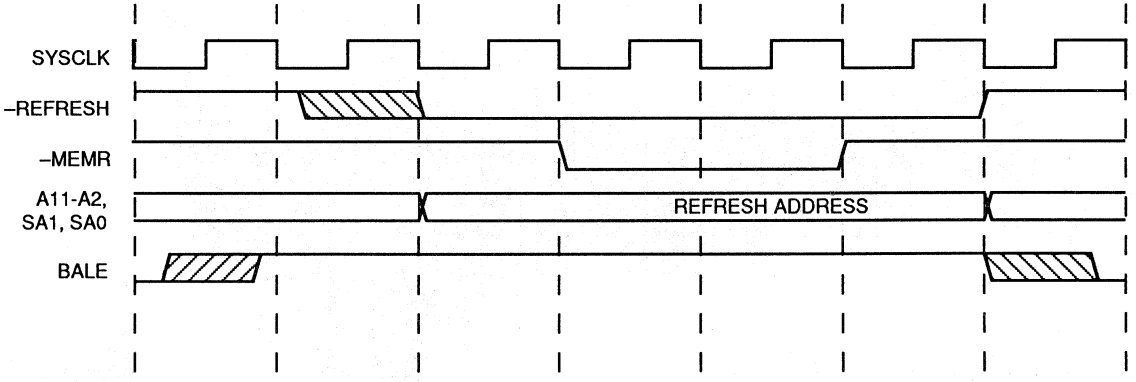


FIGURE 34. ISA BUS REFRESH CYCLE



BUS CONTROL REGISTER (BUSCTL)

Three bus control options are provided and are programmable via the indexed BUSCTL Register. The BUSCTL Register controls the number of wait states to be inserted in 8- and 16-bit slot cycles and determines the output of the slot bus buffers.

TABLE 25. BUSCTL REGISTER (09h) - READ/WRITE

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
BUSCTL (09h)	–VSF	10/16IO	SLTDRV	DSKTMG	CMDLY2	CMDLY1	16WS	8WS
POR Value	0	0	–FMPRG	0	0	0	0	0

Bit	Name	Function
7	–VSF	VLSI Special Feature Enable: Enable I/O space in the EEh to FFh region (0 = enable, 1 = disable).
6	10/16IO	10/16 Bit I/O Decode: Selects 10- or 16-bit I/O decode. 0 = 16-bit decode (default). 1 = 10-bit decode.
5	SLTDRV	Slot Current Drive: This bit selects the current drive on the slot. If low, the current drive is 12 mA, otherwise is it 24 mA. The default value of this bit is the status of the –FMPRG pin.
4	DSKTMG	Disk Timing: This bit is provided for disk controller compatibility. With fast CPUs, some disks can be overrun by programmed I/O. This bit provides a way to compensate by providing a guaranteed minimum delay of three SYSCLKs between programmed I/O cycles. 0 = slow programmed I/O (default). 1 = normal programmed I/O.
3	CMDLY2	Command Delay 2: This bit, when set, allows the addition of one extra command delay for 8-bit and 16-bit I/O cycles and for 8-bit memory cycles. When 0, there is no added command delay. The default value of this bit is 0 resulting in PC/AT compatibility.
2	CMDLY1	Command Delay 1: This bit, if 0, allows PC/AT-compatible zero command delay on 16-bit memory cycles. An extra command delay is added if set to 1. The default value of this bit is 0.
1	16WS	16-Bit Wait States: This bit determines whether to use zero or one wait state for 16-bit slot bus accesses. When 0, the PC/AT-compatible zero wait state operation is used. If set to 1, one wait state operation is used to allow robust operation of add-in cards at faster slot speeds. The default value of this bit is 0 indicating zero wait state operation for 16-bit slot accesses.
0	8WS	8-Bit Wait States: When 0, an extra wait state is added for 8-bit slot bus accesses. This yields five rather than the normal four wait states, which allows slower boards to operate with equivalent performance when high bus speeds are used. This bit is set to 0 at power-on reset initiating four wait states on 8-bit slot accesses.

Zero wait state operation is possible on extremely fast boards that can pull the –WS0 line fast enough and more than five wait states are possible if IOCHRDY is pulled low before the last normal wait state. However, –MEMCS16 or –IOCS16 must be pulled low before the last normal wait state even if IOCHRDY has previously been activated.

DIRECT MEMORY ACCESS (DMA)

The DMA controllers are 82C37A compatible, have internal latches provided for latching the middle address bits output by the 82C37A megacells on the data bus, and have 74LS612 memory mappers provided to generate the upper address bits.

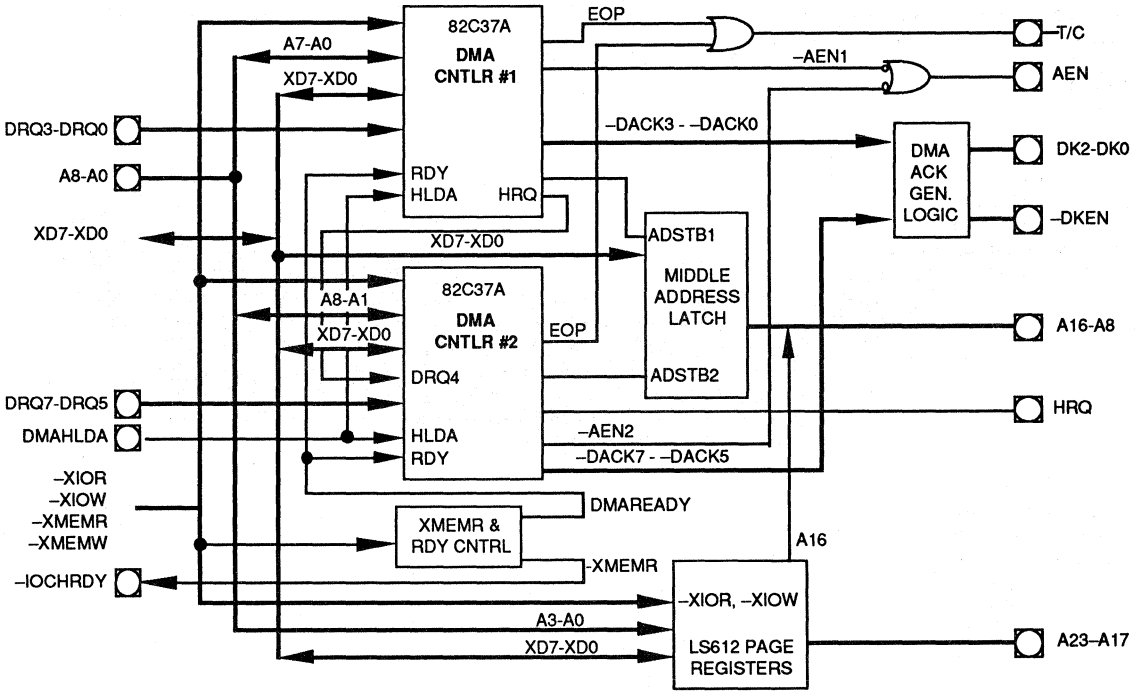
The DMA logic controls transfers between an I/O channel and on- or off-board memory. It generates a hold request to the CPU when an I/O channel requests a DMA operation. Once the hold has been acknowledged, the DMA controller drives the CPU address bus and the slot address bus. DMA transfers can occur over the full 16M range available on the slot bus and the 64M range of the system board DRAM. DMA may also be to a local bus device if a DMA transfer falls within a memory range selected as being mapped to the local bus by the PMR Registers.

DMA Controllers

The VL82C486 supports seven DMA channels using two 82C37A equivalent megacells capable of running at SYSCLK or SYSCLK ÷2. This option is programmable via the Indexed Configuration Register DMACTL. DMA Controller #1 contains channels 0 through 3. These channels support 8-bit I/O adapters. Channels 0 through 3 are used to transfer data between 8-bit peripherals and 8- or 16-bit memory. A full 26-bit address is output for each channel so they can all transfer data throughout the entire 64M system address space when used with the VL82C486. Each channel can transfer data in 64K pages.

DMA Controller #2 contains channels 4 through 7. Channel 4 is used to cascade DMA Controller #1, so it is not available externally. Channels 5 through 7 support 16-bit I/O adapters to transfer data between 16-bit I/O adapters and 16-bit system memory. A full 26-bit address is output for each channel so they can all transfer data throughout the entire 64M system address space. Each channel can transfer data in 128K pages. Channels 5, 6, and 7 are meant to transfer 16-bit words only and can not address odd bytes in system memory. Figure 35 is a block diagram of the DMA controller logic.

FIGURE 35. DMA CONTROLLER LOGIC



The seven DMA acknowledge signals are encoded within the VL82C486 to generate the external signals DK2-DK0. DK2-DK0 are decoded externally using a 3-to-8 latch/demultiplexer (74LS137). The enable signal DKEN is generated by the VL82C486 for use by the latch/demultiplexer. Figure 36 depicts the interface between the VL82C486 and 74LS137.

If a local bus device that responds to DMA cycles is selected by the PMR Registers, then the –DACKx signals must be latched when the DKEN signal is active since the encoded DK2-DK0 signals are used by the VL82C486 to drive the cycle type to the local device during a local bus memory access. However, it is not necessary to latch DK2-DK0 if the local bus DMA cycles are not programmed by the PMR Registers.

During power-on reset, DKEN may be programmed by the –FLUSH pin to be either active high or active low. When used with the VL82C107 Combination I/O it must be programmed active low (–FLUSH pulled low during power-on reset). When used with a 74LS137, it must be programmed active high (–FLUSH pulled high during power-on reset). When used with a 74LS138, it may be programmed for either polarity depending on whether it is sent to an active high or active low input of the 74LS138.

FIGURE 36A. DECODING DMA ACKNOWLEDGE SIGNALS

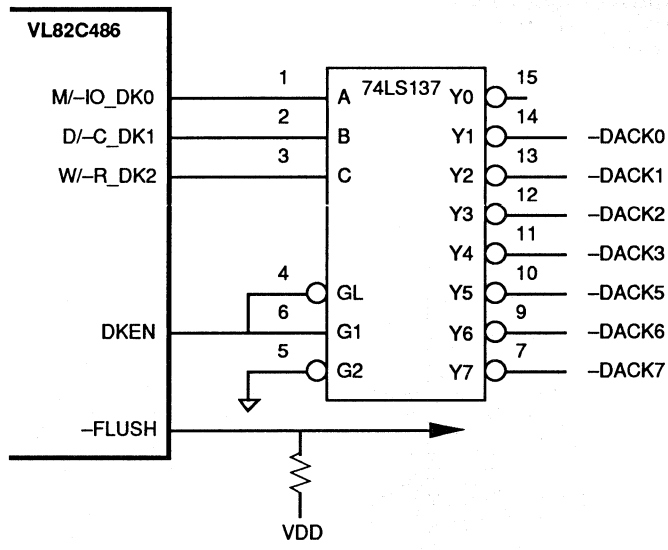
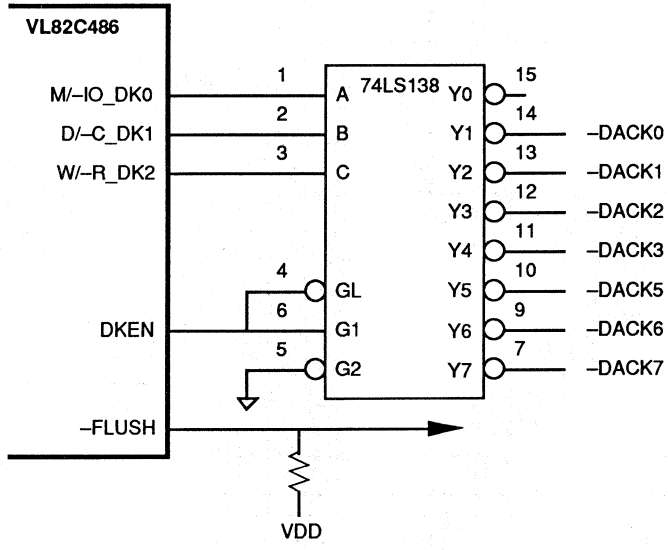


FIGURE 36B. DECODING DMA ACKNOWLEDGE SIGNALS



DMA Controller Registers

The 82C37A megacells can be programmed any time HLDA is inactive, i.e., when DMA controllers are not in operation. Table 26 lists the addresses of all registers which can be read or written in the 82C37A megacells. Addresses under the DMA2 column heading are for the 16-bit DMA channels and DMA1 corresponds to the 8-bit channels. When writing to a channel's address or word count register, the data is written into both the base register and current register simultaneously. When reading a channel's address or word count register, only the current address or word count can be read. The base address and base word count are not accessible for reading.

The address and word count registers for each channel are 16 bit-registers. The value on the data bus is written into the upper or lower byte depending on the state of the internal addressing flip-flop. This flip-flop can be cleared by the Clear Byte Pointer Flip-Flop command. After this command, the first read/write to an address or word count register will read/write to the low byte of the 16-bit register and the byte pointer flip-flop will toggle to a logic 1. The next read/write to an address or word count register will read or write to the high byte of the 16-bit register and the byte pointer flip-flop will toggle back to a logic 0. Refer to the 82C37A data sheet for more information on programming the 82C37A megacell.

The 82C37A DMA controller megacells allow the user to program the active level (low or high) of the DREQ and DACK signals. Since the two megacells are cascaded together internally on the chip, these signals should always be programmed with the DREQ signals active high and the DACK signals active low.

When programming the 16-bit channels (channels 5, 6, and 7) the address which is written to the base address register must be the real address divided by two. Also, the base word count for the 16-bit channels is the number of 16-bit words to be transferred, not the number of bytes as is the case for the 8-bit channels.

It is recommended that all internal locations, especially the Mode Registers, in the 82C37A megacells be loaded with some valid value. This should be done even if the channels are not used.

TABLE 26. DMA CONTROLLER REGISTERS

Hex Address		
DMA2	DMA1	Register Function
0C0	000	Channel 0 Base and Current Address Register
0C2	001	Channel 0 Base and Current Word Count Register
0C4	002	Channel 1 Base and Current Address Register
0C6	003	Channel 1 Base and Current Word Count Register
0C8	004	Channel 2 Base and Current Address Register
0CA	005	Channel 2 Base and Current Word Count Register
0CC	006	Channel 3 Base and Current Address Register
0CE	007	Channel 3 Base and Current Word Count Register
0D0	008	Read Status Register/Write Command Register
0D2	009	Write Request Register
0D4	00A	Write Single Mask Register Bit
0D6	00B	Write Mode Register
0D8	00C	Clear Byte Pointer Flip-Flop
0DA	00D	Read Temp Register/Write Master Clear
0DC	00E	Clear Mask Register
0DE	00F	Write All Mask Register Bits

Middle Address Bit Latches
The middle DMA address bits are held in an internal 8-bit register. The DMA controller drives the value to be loaded onto the internal data bus and then issues an address strobe signal to latch the data bus value into this register. An address strobe is issued at the beginning of a DMA cycle and any time the lower 8-bit address increments across the 8-bit subpage boundary during block transfers. This register cannot be written to or read externally. It is loaded only from the address strobe signals from the megacells and the outputs go only to the A16-A8 pins.

Page Registers and Extended Addressing
An extended 74LS612 cell is used in the VL82C486 to generate the Page Registers for each DMA channel. The Page Registers provide the upper address bits, A25-A16, during DMA cycles. DMA addresses do not increment or decrement across page boundaries. Page boundaries for the 8-bit channels (channels 0 through 3) are every 64 KB and page boundaries for the 16-bit channels (channels 5, 6, and 7) are every 128 KB. There are a total of sixteen 10-bit registers in the extended 612 megacell.

The Page Registers must be written at the addresses shown in Table 27 to select the correct page for each DMA channel before any DMA operations are performed. The other address locations between 80h and 8Fh not shown in the table are not used by the DMA channels, but can be read or written to by the CPU. Address 8Fh is used to drive a value onto the upper address bits A25-A17 of the CPU's address bus during a refresh cycle.

In normal operation, the top two bits of the 10-bit Page Registers are disabled and inaccessible, and zeros are driven onto A25 and A24 during DMA cycles. This mode is fully compatible with the PC/AT standard. In extended addressing mode, the top two bits of the Page Registers are accessible via a special programming mode, and drive their values onto A25 and A24 during DMA cycles to allow access to the full 64 MB system board memory range.

The Indexed Configuration Register DMACTL is used to program extended DMA functions. Bit 7 (ENBLFF) enables the extended addressing DMA functions. When bit 7 = 0, any previously stored values for A25 and A24 are disabled and these address bits are forced to zero during DMA cycles. When bit 7 = 1, the top two bits of the Page Registers (that supply A25 and A24 values) can be accessed by setting bit 6 (FFPTR) of the DMACTL Register, and writing data to the same address used for the lower Page Register byte. Resetting bit 6 to zero allows access to the lower Page Registers. Bit 6 is forced to zero and has no effect unless bit 7 is set to one. Bit 6 automatically toggles on any write to DMA register space between 80h and 8Fh, allowing automatic selection of the upper or lower portion of the Page Registers on consecutive writes. Both bits 6 and 7 are reset to zero on power-on reset for complete AT compatibility.

Refer to Table 28 for the DMACTL Register's format.

TABLE 27. DMA PAGE REGISTERS ACCESS

Upper Page Register Address (Sets values for A25, A24) ENBLFF = 1, FFPTR = 1	Lower Page Register Address (Sets values for A23-A16) ENBLFF = 1/0, FFPTR = 0	DMA Channel
87h	87h	0
83h	83h	1
81h	81h	2
82h	82h	3
8Bh	8Bh	5
89h	89h	6
8Ah	8Ah	7
8Fh	8Fh	Refresh

Address Generation
The DMA addresses are set up such that there is an upper address portion, a middle address portion, and a lower address portion.

The upper address portion, which selects a specific page, is generated by the Page Registers in the 74LS612 equivalent megacell. The Page Registers for each channel must be set up by the CPU before a DMA operation. DMA addresses do not increment or decrement across page boundaries. Page sizes are 64 KB for 8-bit channels (channels 0 through 3) and 128 KB for 16-bit channels (channels 5, 6, and 7). The DMA Page Register values are output on A25-A16 for 8-bit channels and A25-A17 for 16-bit channels.

The middle address portion, which selects a block within the page, is generated by the 82C37A megacells at the beginning of a DMA operation and any time the DMA address increments or decrements through a block boundary. Block sizes are 256 bytes for 8-bit channels (channels 0 through 3) and 512 bytes for 16-bit channels (channels 5, 6, and 7). This middle address portion is output by the 82C37A megacells onto the internal data bus during state S1. The value is loaded into the middle address bit latches. The middle address bit latches then are output on A15-A8 for 8-bit channels and A16-A9 for 16-bit channels.

TABLE 28. DMACTL REGISTER (08h) - READ/WRITE

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
DMACTL (08h)	ENBLFF	FF PTR	DMAWS8(1)	DMAWS8(0)	DMAWS16(1)	DMAWS16(0)	DMACLK	MEMTM
POR Value	0	0	1	1	1	0	0	0

Bit	Name	Function
7	ENBLFF	Enables extended DMA addressing and access to upper Page Register bits when set to 1. Forced to 0 on POR.
6	FFPTR	Selects upper (set to 1) or lower (set to 0) Page Register access.
5, 4	DMAWS8(1), DMAWS8(0)	8-Bit DMA Wait States: Bits 5 and 4 are encoded with the number of clocks the command is active for 8-bit DMA cycles: **Bit 5 / Bit 4 / # of DMA Clocks** 0 0 2 0 1 4 1 0 3 1 1 3
3, 2	DMAWS16(1), DMAWS16(0)	16-Bit DMA Wait States: These bits specify the number of clocks the command is active for 16-bit DMA cycles: **Bit 3 / Bit 2 / # of DMA Clocks** 0 0 2 0 1 4 1 0 3 1 1 3
1	DMACLK	DMA Clock: When set, this bit selects SYSCLK as an input clock for the DMA. When 0, the input clock to the DMA is SYSCLK ÷2. At power on, SYSCLK ÷2 is selected as the DMA clock.
0	MEMTM	–MEMR Signal Delay: This bit specifies the delay for the –MEMR signal. When 0, –MEMR is active at the same time as in the original PC/AT design. This is the default case. When 1, the falling edge of –MEMR occurs one DMACLK earlier. In this latter case, the –MEMR timing during a memory to I/O DMA cycle is the same as that of the –XIOR signal during an I/O to memory DMA cycle.

The lower address portion is generated directly by the 82C37A megacells during DMA operations. The lower address bits are output on A7-A0 for 8-bit channels and A8-A1 for 16-bit channels. The internal signals –SBHE and A0 are forced low during 16-bit DMA operations. –SBHE is forced to the opposite value of A0 for 8-bit DMA cycles.

–SBHE is configured as an output during all DMA operations and is driven as the inversion of A0 during 8-bit DMA cycles and forced low for all 16-bit DMA cycles.

Table 29 shows the mapping from the DMA subsystem signals to the slot bus signals. Table 30 shows the mapping of DMA subsystem signals to local address bus signals for a VL82C486-based system.

TABLE 29. DMA ADDRESSING FOR SLOT BUS ACCESSES

Outputs from 74LS612 Page Registers	Outputs from Middle Address Latches	Address Outputs from 82C37A	8-Bit DMA Address Bits	16-Bit DMA Address Bits
M9				
M8				
M7			LA23	LA23
M6			LA22	LA22
M5			LA21	LA21
M4			S/LA20	S/LA20
M3			S/LA19	S/LA19
M2			S/LA18	S/LA18
M1			S/LA17	S/LA17
M0			SA16	
	D7		SA15	SA16
	D6		SA14	SA15
	D5		SA13	SA14
	D4		SA12	SA13
	D3		SA11	SA12
	D2		SA10	SA11
	D1		SA9	SA10
	D0		SA8	SA9
		A7	SA7	SA8
		A6	SA6	SA7
		A5	SA5	SA6
		A4	SA4	SA5
		A3	SA3	SA4
		A2	SA2	SA3
		A1	SA1	SA2
		A0	SA0	SA1
		VSS		SA0
		–A0	–SBHE	
		VSS		–SBHE

TABLE 30. DMA ADDRESSING FOR SYSTEM BOARD MEMORY

Outputs from 74LS612 Page Registers	Outputs from Middle Address Latches	Address Outputs from 82C37A	8-Bit DMA Address Bits	16-Bit DMA Address Bits
M9			A25	A25
M8			A24	A24
M7			A23	A23
M6			A22	A22
M5			A21	A21
M4			A20	A20
M3			A19	A19
M2			A18	A18
M1			A17	A17
M0			A16	
	D7		A15	A16
	D6		A14	A15
	D5		A13	A14
	D4		A12	A13
	D3		A11	A12
	D2		A10	A11
	D1		A9	A10
	D0		A8	A9
		A7	A7	A8
		A6	A6	A7
		A5	A5	A6
		A4	A4	A5
		A3	A3	A4
		A2	A2	A3
		A1		A2
		A0		A1
		–A0		–BE1, –BE0
		A1 + A0	–BE0	–BE3, –BE2
		A1 + –A0	–BE1	
		–A1 + A0	–BE2	
		–A1 + –A0	–BE3	

Ready Control

The Ready input to each of the 82C37A megacells is driven from the same source within the Ready control logic. The VL82C486 Ready control logic forces the preprogrammed number of wait states on every DMA transfer. Power-on reset defaults to one wait state for both 8- and 16-bit transfers. Other options can be programmed after power-on reset in the Indexed Configuration Register DMACTL. The external signal IOCHRDY goes into the Ready control logic to further extend transfer cycles if needed. To add extra wait states, an external device should pull IOCHRDY low within the setup time before the second phase of the internal DMA clock no later than the last forced wait state cycle. The current DMA cycle will then be extended by inserting wait states until IOCHRDY is returned high. IOCHRDY going high must meet the setup time at the beginning of a wait state cycle or an extra wait state will be inserted before the DMA controller transitions to state S4.

External Cascading

An external DMA controller or bus master can be attached to a PC/AT-compatible design through the VL82C486's DMA controllers. To add an external DMA controller, one of the seven available DMA channels must be programmed in the Cascade Mode. That channel's DRQ signal should then be connected to the external DMA controller's HRQ output. The corresponding DACK signal for that channel should be connected to the external DMA controller's HLDA input. When one of the seven channels is programmed in the Cascade Mode and that channel is acknowledged, the VL82C486 will not drive the data bus, command signals, or address bus.

An external device can become a bus master and control the system address, data, and command buses in much the same manner. One of the external channels must be programmed in the Cascade Mode. The external device then asserts the DRQ line for that channel. When that channel's DACK line goes active, the external device can then pull the –MASTER signal low. As

in the DMA controller cascading, the VL82C486 does not drive the address, data, and command signals while the cascaded channel's DACK signal is active.

Hold Request Arbiter
The hold request arbiter is used to select between two possible sources for a hold request to the CPU. A hold request can be generated when DMA Controller #2 issues a hold request via the DMAHRQ signal or when the output of Counter #1 in the 82C54 megacell makes a low-to-high transition to indicate a need for a refresh cycle.

At the end of a hold request from either source, the arbiter checks to see if the other source is still requesting a hold. If it is, the arbiter gives an acknowledge signal to that source and leaves the HRQ line active. This continues as long as one of the two sources is requesting a hold. Only if neither source is requesting a hold will the arbiter negate the HRQ signal and return control back to the CPU.

–MEMR Delay
To maintain an AT-compatible design, the VL82C486's power-on reset default inserts one DMA clock cycle delay in the falling edge of the –MEMR signal. –MEMR will go low one DMA clock later than the –MEMR signal coming out of the 82C37A megacell. The rising edge is not altered and goes high at the same time the –MEMR signal from the megacell goes high. The VL82C486 can be reprogrammed to remove the one clock cycle delay on the falling edge of –MEMR. This done by setting the MEMTM bit (bit 0) to 1 in the DMACTL Register.

DATA STEERING
Overview
The Data Buffer Block of the VL82C486 handles data transfers between the 32-bit local CPU data bus, the 16-bit ISA slot bus, and the 8-bit on-chip I/O data bus. Connected to the local data bus is the 486, on-board DRAM, BIOS ROM, flash memory, and any other local bus devices such as the WEITEK coprocessor. Off-board memory, BIOS ROM, I/O devices, keyboard controller, real-time clock, DMA requesters, and add-on bus master cards reside on the ISA bus. Various system configuration/data registers, DMA controller registers, interrupt controller registers, and counter/timer registers lie on the on-chip I/O data bus. Either the 486, the DMA controllers, or an add-on bus master card can become the bus owner.

When the 486 is the bus owner, the VL82C486's data steering logic provides the data conversion necessary for 8/16/32-bit writes and reads to and from 8/16-bit devices on either the ISA bus, or 8-bit registers on the on-chip I/O data bus, or 8/16-bit BIOS ROM sitting on the local data bus. Data transfer between the 486 and on-board DRAM, local bus devices, and flash memory is handled directly via the local CPU data bus while slot data pads and local data bus pads of the VL82C486 are three-stated. Tables 32 and 33 show the data steering modes during CPU accesses.

When the DMA requestor or add-on bus master is the bus owner, the VL82C486 will allow 8/16-bit data transfer between the ISA bus and either the local CPU data bus or the on-chip I/O data bus. The VL82C486 is also capable of performing byte swaps between the high and low bytes of the 16-bit ISA bus. ISA bus transfers between ISA bus devices that do not require byte swaps between high and low bytes are handled directly via the ISA slot bus while the slot data pads on the VL82C486 are three-stated. Any data conversion required is handled by the DMA or add-on bus master device. Tables 34 through 38 show the data steering modes during DMA or add-on bus master accesses.

Table 31 is a glossary of terms and acronyms used in Tables 34 through 38.

TABLE 31. DATA STEERING LOGIC GLOSSARY OF TERMS AND ACRONYMS

Terms	Definition
D0, D1, D2, D3	Local CPU data bus bits 7-0, 15-8, 23-16, 31-24, respectively
DMA(8), DMA(16)	8-bit DMA device, 16-bit DMA device, respectively
DRAM(32)	32-bit on-board DRAM
ISA(8), ISA(16)	8-bit ISA bus devices and on-chip I/O devices, 16-bit ISA bus devices, respectively
LAB(32)	32-bit local bus device
MASTER(16)	16-bit add-on bus master device
ROM(8), ROM(16)	8-bit BIOS ROM, 16-bit BIOS ROM, respectively
SDL, SDH	Slot data bus low bytes 7-0 and slot data bus high bytes 15-8, respectively

TABLE 32. DATA STEERING DURING CPU WRITES

Data Type	Device Size	Data Steering	Notes
Byte, Word, Double Word	ISA(8)	D0 -> SDL or D1 -> SDL or D2 -> SDL or D3 -> SDL	• One slot access generated for byte writes • Two slot accesses generated for word writes • Four slot accesses generated for double word writes • All 8-bit on-chip I/O data bus writes performed in this data steering mode
Byte	ISA(16)	D0 -> SDL or D1 -> SDH or D2 -> SDL or D3 -> SDH	• One slot access generated for byte writes
Word, Double Word	ISA(16)	D0 -> SDL and D1 -> SDH or D2 -> SDL and D3 -> SDH	• One slot access generated for aligned word writes • Two slot accesses generated for aligned double word writes • Two slot accesses generated for misaligned word writes
Byte, Word, Double Word	DRAM(32) LBA(32) ROM(16)	N/A	• All the VL82C486's data paths (D0, D1, D2, D3, SDL, and SDH) are three-state during on-board DRAM accesses, local bus device accesses, or flash memory writes

TABLE 33. DATA STEERING DURING CPU READS

Data Type	Device Size	Data Steering	Notes
Byte, Word, Double Word	ISA(8)	SDL -> D0 or SDL -> D1 or SDL -> D2 or SDL -> D3 *On-chip bus -> D0, or D1, or, D2, or D3 and On-chip bus -> SDL, SDH	• One slot access generated for byte reads • Two slot accesses generated for word reads • Four slot accesses generated for double word reads • D0, D1, D2, and D3's data is latched before redriving onto the local data bus
Byte	ISA(16)	SDL -> D0 or SDL -> D1 or SDL -> D2 or SDL -> D3	• One slot access generated for byte reads • D0, D1, D2, and D3's data is latched before redriving onto the local data bus
Word, Double Word	ISA(16)	SDL -> D0 and SDH -> D1 or SDL -> D2 and SDH -> D3	• One slot access generated for aligned word reads • Two slot accesses generated for aligned double word reads • Two slot accesses generated for misaligned word reads • D0, D1, D2, and D3's data is latched before redriving onto the local data bus
Byte, Word, Double Word	DRAM(32) LBA(32)	N/A	• All the VL82C486's data paths (D0, D1, D2, D3, SDL, and SDH) are three-state during on-board DRAM or local bus device accesses

* For 8-bit on-chip I/O data bus reads, data is read from on-chip I/O data bus instead of SDL. Data is available on the appropriate local data bus byte D0, D1, D2, or D3, plus the SDL and SDH bus.

TABLE 34. DATA STEERING DURING BIOS ROM READS

Data Type	Device Size	Data Steering	Notes
Byte, Word, Double Word	ROM(8)	D2 -> D0 or D2 -> D1 or D2 -> D2 or D2 -> D3	• One access generated for byte reads • Two accesses generated for word reads • Four accesses generated for double word reads • D0, D1, D2, and D3's data is latched before redriving onto the local data bus
Byte	ROM(16)	D2 -> D0 or D3 -> D1 or D2 -> D2 or D3 -> D3	• One access generated for byte reads • D0, D1, D2, and D3's data is latched before redriving onto the local data bus
Word, Double Word	ROM(16)	D2 -> D0 and D3 -> D1 or D2 -> D2 and D3 -> D3	• One access generated for aligned word reads • Two accesses generated for aligned double word reads • Two accesses generated for misaligned word reads • D0, D1, D2, and D3's data is latched before redriving onto the local data bus

TABLE 35. DATA STEERING DURING DMA/MASTER READS OF ON-BOARD DRAM/LOCAL BUS DEVICES

Data Type	Device Size	Data Steering	Notes
Byte, Word	DMA(8)	D0 -> SDL or D1 -> SDL or D2 -> SDL or D3 -> SDL	• One access required for byte reads • Two accesses required for word reads • During local bus device accesses only, D0, D1, D2, and D3's data is latched before redriving onto the slot data bus
Byte	DMA(16) MASTER(16)	D0 -> SDL or D1 -> SDH or D2 -> SDL or D3 -> SDH	• One access required for byte reads • During local bus device accesses only, D0, D1, D2, and D3's data is latched before redriving onto the slot data bus
Word	DMA(16) MASTER(16)	D0 -> SDL and D1 -> SDH or D2 -> SDL and D3 -> SDH	• One access required for aligned word reads • Two accesses required for misaligned word reads • During local bus device accesses only, D0, D1, D2, and D3's data is latched before redriving onto the slot data bus

TABLE 36. DATA STEERING DURING DMA/MASTER WRITES TO ON-BOARD DRAM/LOCAL BUS DEVICES

Data Type	Device Size	Data Steering	Notes
Byte, Word	DMA(8)	SDL -> D0 or SDL -> D1 or SDL -> D2 or SDL -> D3	• One access required for byte writes • Two accesses required for word writes
Byte	DMA(16) MASTER(16)	SDL -> D0 or SDH -> D1or SDL -> D2 or SDH -> D3	• One access required for byte writes
Word	DMA(16) MASTER(16)	SDL -> D0 and SDH -> D1 or SDL -> D2 and SDH -> D3	• One access required for aligned word writes • Two accesses required for misaligned word writes

TABLE 37. DATA STEERING DURING DMA/MASTER READS OF ISA SLOT DEVICES

Data Type	Device Size	Data Steering	Notes
Byte, Word	DMA(8)	SDH -> SDL	• Byte swap required for odd byte 8-bit DMA read of 16-bit slot • One access required for byte reads
Byte	MASTER(16)	SDL -> SDH	• Byte swap required for odd byte add-on bus master read of 8-bit slot • One access required for byte reads
Byte, Word	DMA(8) DMA(16) MASTER(16)	N/A *On-chip bus -> SDL and SDH	• Except for the above two cases and bus master reads of the on-chip I/O data bus, the SDL and SDH data pads are three-state pads for all DMA or bus master reads of 8/16-bit ISA devices

* Data is available on the SDL and SDH bus for add-on bus master reads of 8-bit on-chip I/O data bus

TABLE 38. DATA STEERING DURING DMA/MASTER WRITES TO ISA SLOT DEVICES

Data Type	Device Size	Data Steering	Notes
Byte, Word	DMA(8) ISA(16)	SDH -> SDL	• Byte swap required for odd byte add-on bus master write to 8-bit slot • One access required for byte reads
Byte	MASTER(16) ISA(8)	SDL -> SDH	• Byte swap required for odd byte 8-bit slot DMA write to 16-bit slot • One access required for byte reads
Byte, Word	DMA(8) DMA(16) MASTER(16)	N/A	• Except for the above two cases, the SDL and SDH data pads are input pads for all DMA or bus master writes to 8/16-bit ISA devices • All bus master writes to 8-bit on-chip I/O data bus performed in this data steering mode

ISA BUS REFRESH CYCLE TYPES
The VL82C486 supports three modes of refresh; Synchronous, Asynchronous and Decoupled. Bits 2 and 3 (REFMD1 and REFMD0) in the NTBREF Configuration Register select the type of Refresh Mode. The PC/AT compatible refresh period of 15.625 µs and a slow refresh period of 125 µs are supported. The VL82C486 controls both the on- and off-board refresh timing. For on-board DRAM refresh, RAS-only refresh, as well as CAS-before-RAS refresh cycles are supported.

Synchronous Refresh Mode
With the Synchronous Refresh Mode, on- and off-board refreshes are initiated and completed simultaneously. When refresh is requested by the internal refresh timer, the following sequence occurs:

1) HOLD is asserted.
2) The VL82C486 waits until HLDA is asserted by the CPU.
3) The bus refresh address is placed on the A bus. The DRAM refresh address is placed on the MA bus. –EALE transitions from low-to-high to clock the ISA bus refresh address if the VL82C107 or VL82C113A Combination I/O chips are used.
4) An off-board refresh request is issued to the ISA bus controller and a refresh request to the DRAM controller is issued.
5) HOLD is released when the ISA bus cycle is complete.

Asynchronous Refresh Mode
In the Asynchronous Refresh Mode, on- and off-board refreshes are initiated simultaneously but complete independently; allowing faster refresh cycles for the on-board DRAM. For this mode, slot bus address latches are required. A refresh is requested by OUT1 (counter/timer in the Bus Controller Block) to the System Controller Block. It is arbited with the DMA request by sampling each at opposite edges of SYSCLK and synchronized to CPUCLK. When an internal refresh request is generated, the following sequence occurs:

1) HOLD is asserted.
2) The VL82C486 waits until HLDA is asserted by the CPU.
3) The bus refresh address is placed on the A bus. –EALE transitions from low-to-high to clock or latch the ISA bus refresh address. The DRAM refresh address is placed on the MA bus.
4) An off-board refresh request is issued to the ISA bus controller and a refresh request to the DRAM controller is issued.
5) HOLD is released.

Any subsequent accesses to the ISA bus or the DRAM controller are held-up until the on- or off-board refresh is completed.

Decoupled Refresh Mode
This mode is identical to the Asynchronous Refresh Mode except that HOLD is not asserted in Step 1) and the bus refresh address is not driven onto the A bus as during Step 3). An external refresh counter is therefore required to provide the refresh address to the ISA bus. An off-board refresh request is issued to the ISA bus controller and a refresh request to the DRAM controller is issued in the next CPU T1 or Ti cycle.

Any subsequent CPU request to on-board DRAM is held pending by delaying –BRDY until the on-board refresh has completed. Subsequent accesses to the ISA bus are held-up until the off-board refresh is completed by delaying –RDY until the refresh has completed.

INTERRUPT CONTROLLER

The interrupt controller logic includes two 82C59A megacells with eight interrupt request lines each for a total of 16 interrupts. The two megacells are cascaded internally and two of the interrupt request inputs are connected to the internal circuitry. This allows a total of 13 external interrupt requests. Figure 37 is a block diagram of the interrupt controller logic.

All external interrupt request signals have an internal pull-up resistor to eliminate noise on unconnected request pins. Also, all IRQ pins have a special programmable logic to reduce noise sensitivity, controlled by bit 0 (IRQIN) in the MISCSET Register (Indexed Configuration Register location 07h). The IRQIN bit is a glitch-free interrupt request pin input. If IRQIN is set to 1, glitch-free input on the IRQ pins is allowed. The input to these pins then must be stable for at least 105 ns to generate an interrupt. The IRQIN bit's default is 1.

The interrupt request signals IRQ0, IRQ2, and IRQ13 are utilized internally: Their functions are:

IRQ0 This interrupt is connected to the OUT0 of the 82C54 megacell and is not available as an external input.

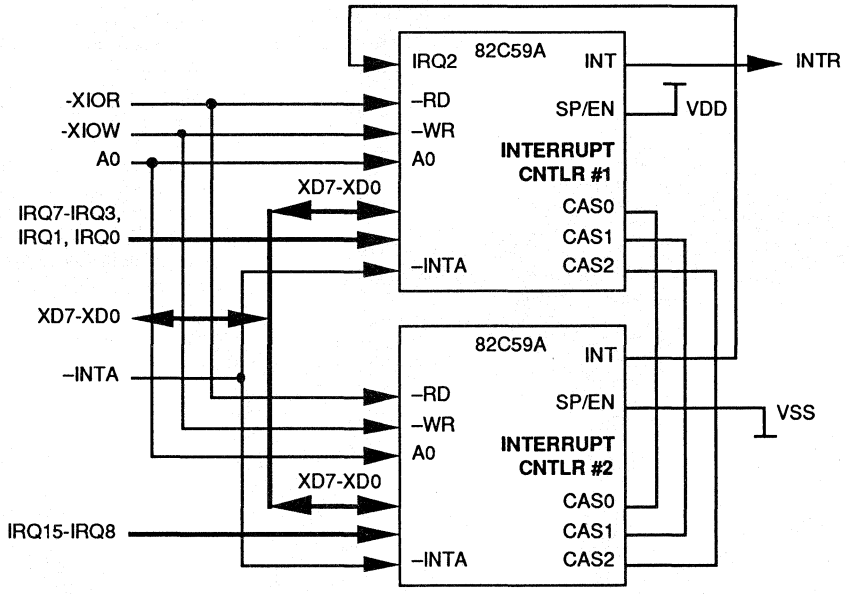
IRQ2 This interrupt is used to cascade the two 82C59A megacells together and is not available as an external input.

IRQ13 This interrupt is used for the coprocessor interface. It is generated by the coprocessor asserting the WEIRQ pin in case of an exception error.

A typical interrupt sequence is as follows. Any unmasked interrupt generates the –INTR signal to the CPU. The interrupt controller megacells then respond to the –INTA pulses from the CPU. On the first –INTA cycle, the cascading priority is resolved to determine which of the two 82C59A megacells output the interrupt vector onto the data bus. On the second –INTA cycle, the appropriate 82C59A megacell drives the data bus with the correct interrupt vector for the highest priority interrupt.

Because the two megacells are cascaded internally on the VL82C486, they should never be programmed to operate in the Buffered Mode.

FIGURE 37. INTERRUPT CONTROLLER LOGIC DIAGRAM



Interrupt Controller Registers
The internal registers of the 82C59A megacells are written to in the same way as in the standard part. Table 39 shows the correct addressing for each of the 82C59A registers.

Before normal operation can begin, each 82C59A megacell must follow an initialization sequence. The sequence is started by writing Initialization Command Word 1 (ICW1). After ICW1 has been written, the 82C59A megacell expects the next writes to follow in the sequence ICW2, ICW3, and ICW4 if it is needed. The Operation Control Words (OCW) can be written at any time after initialization.

In the standard 82C59A megacell ICW3 is optional. But since the two 82C59A's in this chip are cascaded together, they should always be programmed in the Cascade Mode and ICW3 will always be needed. Refer to the 82C59A data sheet for more information on programming the 82C59A megacell.

When reading at address 020h or 0A0h hex, the register read depends on how Operation Control Word 3 is set up prior to the read.

TABLE 39. WRITE-ONLY INTERRUPT CONTROLLER REGISTERS

INT1	INT2	D4	D3	Register Function
20h	A0h	1	X	Write ICW1
21h	A1h	X	X	Write ICW2
21h	A1h	X	X	Write ICW3
21h	A1h	X	X	Write ICW4 (if needed)
21h	A1h	X	X	Write OCW1
20h	A0h	0	0	Write OCW2
20h	A0h	0	1	Write OCW3

TABLE 40. READ-ONLY INTERRUPT CONTROLLER REGISTERS

INT1	INT2	Register Function
20h	A0h	Interrupt Request Register, In-Service Register or Poll Command
21h	A1h	Interrupt Mask Register

TIMER/COUNTER

The timer subsection consists of one 82C54 timer/counter megacell configured as shown in Figure 38. The clocks for each of the three internal counters are tied to the 14.318 MHz oscillator through a ÷12 counter. The gate inputs of Counters 0 and 1 are tied high to enable those counters at all times. The gate input of Counter 2 is tied to bit 0 (TIM2GAT_SPK) of the Port B Register inside the VL82C486.

Counter 0's output is connected to the IRQ0 input of Interrupt Controller 1. Counter 1's output is used for refresh timing. Finally, Counter 2's output goes to an AND gate which drives the output SPKR pin. The other input on this AND gate is connected to bit 1 (SPK_DAT) of the Port B Register.

Timer/Counter Registers

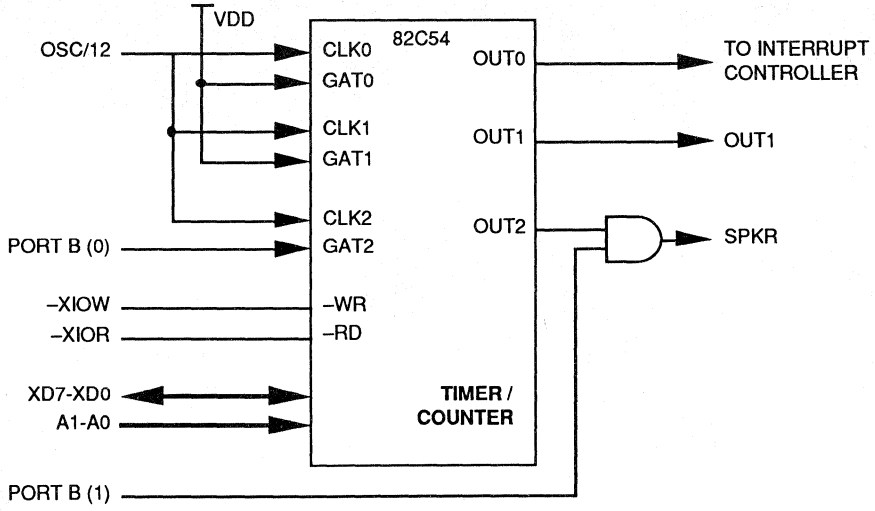
The internal registers of the 82C54 timer/counter megacell are written to in the same way as in the standard part. Table 41 shows the correct addressing for each of the 82C54 registers.

The write control word at address 43h could also be the counter latch command or read-back command depending on the values on the data bus. Refer to the 82C54 data sheet for more information on programming the 82C54 megacell.

TABLE 41. TIMER/COUNTER REGISTERS

Address	–XIOR	–XIOW	Register Function
40h	1	0	Write Initial Count to Counter
40h	0	1	Read Count/Status from Counter 0
41h	1	0	Write Initial Count to Counter 1
41h	0	1	Read Count/Status from Counter 1
42h	1	0	Write Initial Count to Counter 2
42h	0	1	Read Count/Status from Counter 2
43h	1	0	Write Control Word
43h	0	1	No Operation

FIGURE 38. TIMER/COUNTER LOGIC DIAGRAM



KEYBOARD CONTROLLER INTERFACE

The VL82C486 is connected to the keyboard controller, 8042, as shown in Figure 39. Note that there are no A20GATE and –RC pins on the VL82C486. The port pins P20 and P21 of 8042 are therefore not connected. These two signals are generated internally in the VL82C486. The data bus is checked for a particular data sequence when the keyboard controller is selected to generate A20GATE and –RC.

For hardware compatibility, the generation of –RC is delayed by about 50 µs from the issuance of the command to generate a 6 µs pulse. A delay timer is used in the internal circuit for this purpose. This timer can be disabled by the FASTRC bit (bit 4) in the MISCSET Register. When FASTRC = 1, –RC is generated with only a 6.72 µs delay. This provides an alternative for a Fast CPU Reset.

Generation of A20GATE and –RC

The keyboard controller interface signals A20GATE and –RC are generated internally in the VL82C486. These signals are generated in two ways in a PC/AT. They are as described below:

1) Data D1h is written to I/O address 64h. This is a write output port command from the CPU to the keyboard controller. The next byte written to I/O address 60h then enables or disables A20GATE and –RC. Bit 0 of this byte is propagated to –RC while bit 1 gets propagated to A20GATE. It should be noted that the I/O address 60h does not have to be written immediately after writing D1h to address 64h.

   Only A20GATE is generated in this way in the VL82C486 because generation of –RC by this method can hang-up the system. There is no delay involved in the generation of A20GATE.

2) If I/O address 64h is written with F0h-FFh, A20GATE and –RC are pulsed according to the lower two bits of the data. If bit 0 is low, –RC is pulsed and A20GATE is pulsed if bit 1 is low. Thus, a pulse appears on the –RC pin if the data is FEh or FCh and A20GATE is pulsed if it is FDh or FCh. The pulse duration is approximately 6 µs.

   The VL82C486 generates a pulsed –RC this way but there is no effect on A20GATE.

FIGURE 39. KEYBOARD CONTROLLER INTERFACE

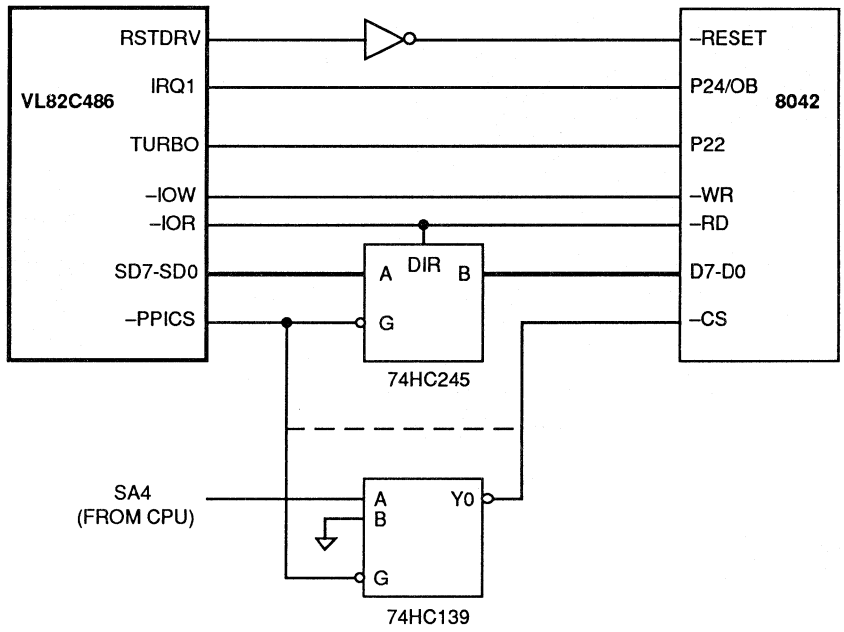


FIGURE 40. TIMING GENERATION OF A STABLE A20GATE

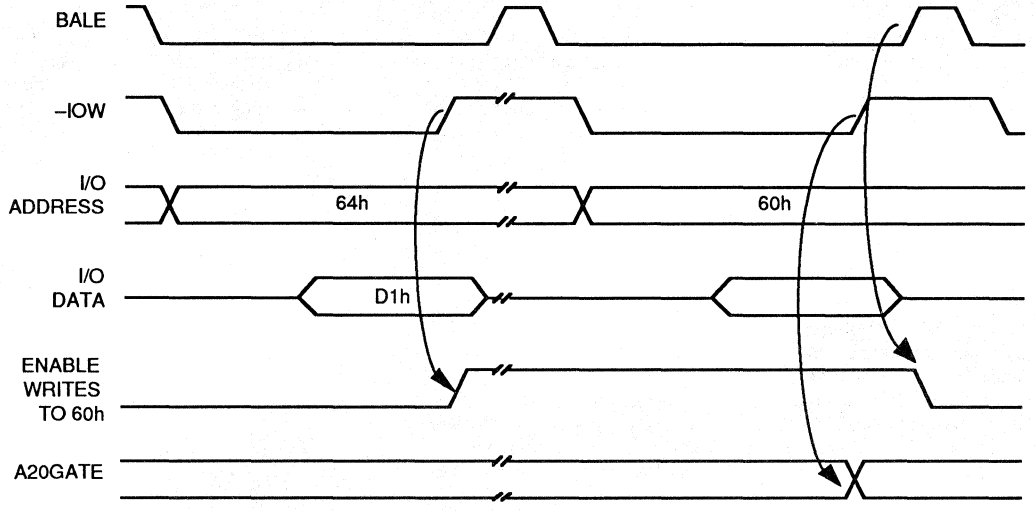
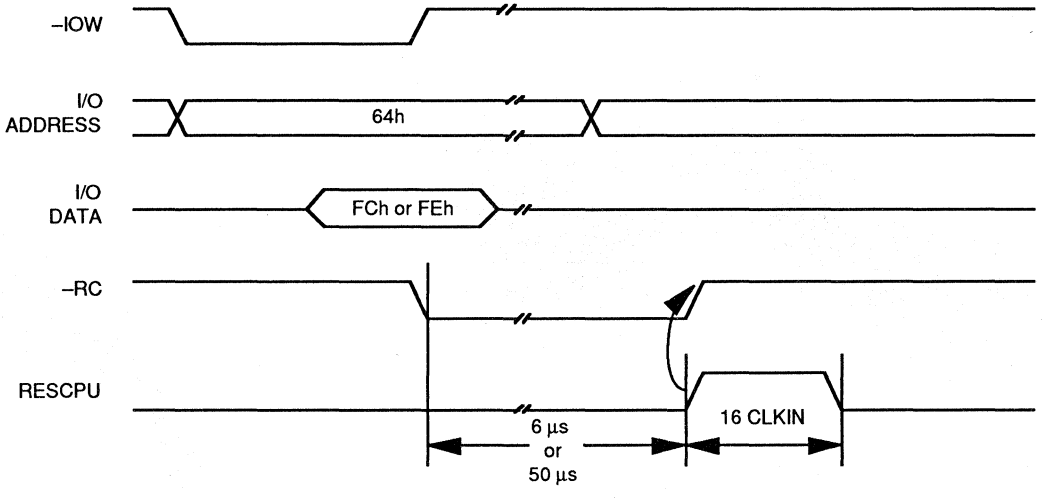


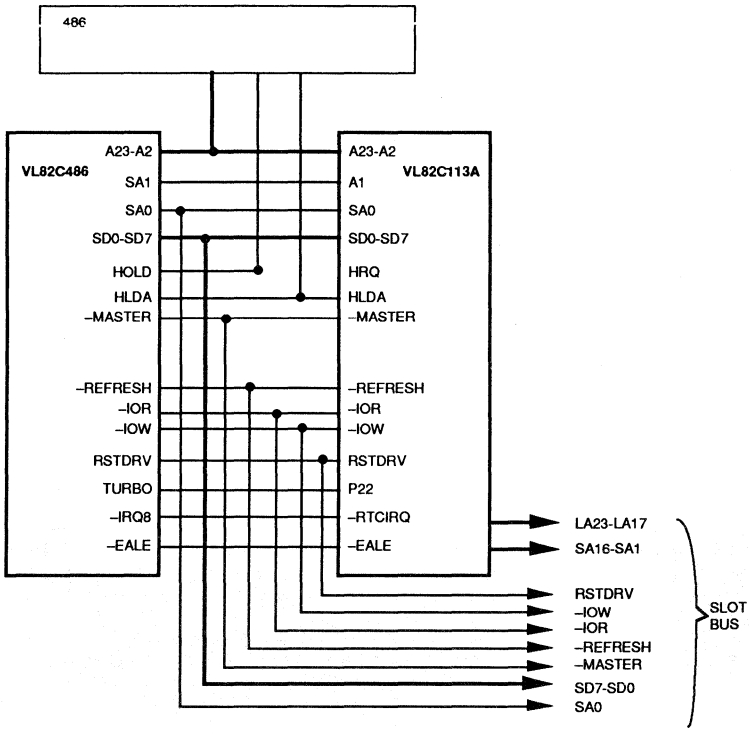
FIGURE 41. TIMING GENERATION OF A PULSED –RC



VL82C113A INTERFACE

The VL82C113A Combination I/O chip includes the glue logic required to design a PC/AT motherboard with the VL82C486. The interface between the VL82C486 and the VL82C113A is shown in Figure 42. Note that the SA1 pin of the VL82C486 is connected to the A1 pin of the VL82C113A, while the SA1 pin of the VL82C113A is connected to the slot bus. This allows the Internal Configuration Registers of the VL82C113A to be correctly addressed from the slot bus. Also, –IGNNE should be pulled high at power-on reset to select the correct timing for use with the VL82C113A.

FIGURE 42. VL82C486 INTERFACE TO THE VL82C113A COMBINATION I/O



SLEEP MODE CONTROL LOGIC

The Sleep Mode operation is provided for battery operated laptop microcomputer support. Various bits in the MISCSET Register are provided to control this function.

SLEEP MODE OPERATION

The Sleep Mode may be activated by software as well as by hardware. The external –SLEEP pin can be used to enable the Sleep Mode by hardware. A 1-to-0 transition on this pin puts the device into the Sleep Mode. For activating the Sleep Mode by software, the SLP bit (bit 7) in the MISCSET Register should be set high.

When the VL82C486 is in the Sleep Mode, the refresh divider is activated, BUSOSC is shut off from non-essential internal circuitry, and the CPU is prevented from making memory accesses by the VL82C486 making the HOLD signal active. The clocks going to the DMA circuit, interrupt controllers, and refresh logic are not shut off.

For maximum power savings, it is recommended that a halt instruction be executed immediately after setting the SLP bit. Power saving can also be accomplished by operating the CPU at the minimum allowable clock frequency (controlled by the CLKCTL Register).

The VL82C486 is brought out of the Sleep Mode in one of four ways:

1) Clearing the SLP bit in the MISCSET Register to zero by software.
2) Driving a 0-to-1 input on the –SLEEP pin.
3) Interrupting the VL82C486.
4) Resetting the VL82C486.

Normal BUSOSC routing and clock speed are resumed when the VL82C486 comes out of the Sleep Mode.

MISCSET CONTROL REGISTER
The MISCSET Register has three bits to support the Sleep Mode's functionality. Bit 6, SLPSTS, is a read-only bit. Bit 5, ENSYSCK, should be set with the desired value by the BIOS during POST. Only bit 7, SLP, needs to be toggled to get in and out of the Sleep Mode during normal operation. See Table 42 for details on the MISCSET Register.

TABLE 42. MISCSET REGISTER - READ/WRITE

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
MISCSET 07h	SLP	SLPSTS	ENSYSCK	FASTRC	CEN	–ENPAR	CWS_OFF	IRQIN
POR Value	0	–SLEEP	1	0	0	0	0	1

Bit	Name	Function
7	SLP	Sleep Mode: This bit is set to 1 to invoke all Sleep Mode functions. When set, the CPU is halted.
6	SLPSTS	–SLEEP Pin Status: This bit reflects the status of the –SLEEP pin. It is used by the software to check whether –SLEEP is active or not. The VL82C486 enters the Sleep Mode when the –SLEEP pin is pulled low. If an interrupt occurs, the VL82C486 comes out of the Sleep Mode but the pin still might be pulled low. The interrupt service routine can check this bit and activate the Sleep Mode by enabling the SLP bit. SLPSTS is a read-only bit.
5	ENSYSCK	System Clock Enable: Resetting this bit to 0 disables the SYSCLK oscillator (BUSCLK ÷2) if bit 7 is set to 1. Returning bit 7 to 0 re-enables the oscillator signal. If ENSYSCK is set to 1, the oscillator is always enabled even in the Sleep Mode. In operation, ENSYSCK is set for the desired operation mode by the BIOS on power-up. Bit 7 is then controlled as required to jump in and out of the Sleep Mode.
4	FASTRC	Fast –RC: For hardware compatibility, the internally generated –RC has a 50 µs delay from the issuance of the command to write data FCh or FEh to Port 64h (which generates a low going 6 µs pulse on –RC). This delay can be reduced by using the FASTRC bit. If set to 1, there is only a 6.72 µs delay introduced.
3	CEN	Cache Enable: When reset to 0, this bit disables the primary cache and forces the –KEN output to be deasserted (set high). When set to 1, the primary cache is selectively enabled and –KEN is controlled by PMRs, Segment Registers, and address decoder.
2	–ENPAR	Parity Enable: When reset to 0, parity generation and checking is enabled. When set to 1, parity checking is disabled.
1	CWS_OFF	DRAM CAS Conditional Wait States Off: When set to 0, CAS conditional wait states are enabled and when set to 1, they are disabled.
0	IRQIN	Glitch-free Interrupt Request Pin Input: This bit, when set to 1, allows glitch-free input on the IRQ pins. The input to these pins then should be stable for at least 105 ns to generate an interrupt.

DEDICATED INTERNAL CONTROL REGISTERS AND I/O LOCATIONS

This section describes various features of the VL82C486 available at dedicated internal I/O ports that have not been fully covered in previous sections.

VLSI SPECIAL FEATURES

The port addresses F8h-FFh are reserved for coprocessor use in an IBM PC/AT. However, only F8h, FAh, FCh, and FEh are actually used. The VLSI Special Features Mode (VSF) allows the use of unused port addresses in this range as well as special registers in the address range EEh-F7h. The F8h-FFh range is decoded and then ANDed with inverted address bit A0. This maps only the even addresses in this range to the coprocessor. The port addresses EEh, EFh, F0h, and F1h are fully decoded due to the presence of other I/O ports at F4h and F5h.

The special registers provided for VLSI Special Features are Fast A20 (EEh), Fast Reset (EFh), Slow CPU (F4h), Fast CPU (F5h), Config Disable (F9h), and Config Enable (EBh).

The VSF Mode is controlled by bit 7 (–VSF) in the BUSCTL Register. Bit 7 is used to enable or disable the VSF options mapped into the coprocessor I/O space between EEh and FFh. When bit 7 = 1, the VSF option is disabled. When bit 7 = 0, the VSF option is enabled.

DEDICATED INTERNAL CONTROL REGISTER ADDRESS

The registers and features described next are a fully compatible superset of the VLSI Special Features (VSF). All port decodes are between ECh and FFh as shown in Table 43. Refer back to Table 3 for a complete I/O map.

TABLE 43. DEDICATED I/O CONTROL REGISTERS

Port Address	Register Function	Port Address	Register Function
ECh	Config Index Register	F5h+	Fast CPU
EDh	Config Data Port	F8h	Reserved
EEh*+	Fast A20	F9h+	Config Disable
EFh*+	Fast Reset	FAh	Reserved
F0h	Coprocessor Busy Clear	FBh+	Config Enable
F1h	Coprocessor Reset	FCh	Reserved
F4h+	Slow CPU	FEh	Reserved

* Also can be activated through Port 92h (Port A) for PS/2 compatibility.
\+ These decodes can be disabled in case of conflict.

TABLE 44. CONFIGURATION INDEX REGISTER

ECh	D7	D6	D5	D4	D3	D2	D1	D0
Config Index	X	X	X	X	X	X	X	X

The value written to this register is the 8-bit address of the Indexed Configuration Register which is to be accessed through the Data Port Register at I/O address EDh. All subsequent Data Port reads and writes access the register at this address until the Index Register is written with a new address. This register is readable. It always returns the last value written to it.

TABLE 45. CONFIGURATION DATA PORT REGISTER

EDh	D7	D6	D5	D4	D3	D2	D1	D0
Config Data	X	X	X	X	X	X	X	X

The registers accessible through I/O address EDh are summarized in the section titled "Register Summary" starting on page 107. They are accessed by writing their addresses to the Index Register at I/O address ECh, then by accessing the Data Port at I/O address EDh.

TABLE 46. FAST A20 REGISTER AND PORT A

EEh (PC/AT)	D7	D6	D5	D4	D3	D2	D1	D0
Fast A20	1	1	1	1	1	1	1	1

92h (PS/2)	D7	D6	D5	D4	D3	D2	D1	D0
Port A	1	1	1	1	1	1	A20	RESET

A dummy read enables Fast A20 and returns a value of FFh. A dummy write disables Fast A20. This method provides a fast, parallel alternative to the standard PC/AT-compatible method of using the keyboard controller to control A20. It is necessary to OR this signal and the keyboard controller's A20 Enable so that either event controls the A20 address line. Default on reset is internal A20 control disabled. While disabled, A20 is solely controlled by the keyboard controller for strict PC/AT compatibility.

This register is also controlled via bit 1 of I/O Register 92h (Port A) for PS/2-compatibility. When bit 1 is high, A20 is active. When bit 1 is low, A20 is always 0. This feature is fully integrated with the Fast A20 control achieved through EEh; i.e., a dummy read of EEh followed by a read of bit 1 of Port 92h returns a logic 1.

Access at location EEh is controlled by the –VSF bit (bit 7) in the BUSCTL Register. –VSF should be 0 to access this register.

TABLE 47. FAST CPU RESET REGISTER AND PORT A

EFh (PC/AT)	D7	D6	D5	D4	D3	D2	D1	D0
Fast Reset	1	1	1	1	1	1	1	1

92h (PS/2)	D7	D6	D5	D4	D3	D2	D1	D0
Port A	1	1	1	1	1	1	A20	RESET

This register provides a fast alternative to the keyboard controller for resetting the CPU. A dummy read of EFh resets the processor and returns a value of FFh. This reset signal is internally ORed with the keyboard controller's reset signal, internal –RC, so that either event invokes a reset. This provides a much faster way for the system to jump between the Real and Protected Modes. Reset timing is the same as described below for the Port A reset.

Fast CPU Reset can also be controlled via bit 0 of I/O Register 92h (Port A) for PS/2 compatibility. When RESET (bit 0) = 1, a reset operation is triggered after a minimum 6.72 µs delay. RESET pulses high for 16 CPU clock cycles. This latch remains set until written again or until the VL82C486 is externally reset.

If the –VSF bit in the BUSCTL Register is set to 1, the Fast CPU Reset feature at EFh is disabled. The Fast Reset at 92h is always available, as is the reset activated by the BIOS through the keyboard controller.

Note: In order to successfully reset a PC/AT-compatible system, A20 must be gated through and not held low. Otherwise, the reset vector is not fetched and the system hangs up. In some existing systems a Hot Reset without controlling A20 seems to work. However, this is because an error trap occurs which eventually supplies the reset vector to the system. A large number of software instructions occurs in this case and the result is a "not very fast reset". Therefore, before issuing a Hot Reset command either via I/O Port 92h or I/O Port EFh as described above, one of the following must occur:

1) Set bit 1 in Port A to 1. (Writing 03h to this register effectively accomplishes both goals with a single I/O instruction.)
2) Perform a dummy read of EEh to enable A20.

TABLE 48. CPU SPEED CONTROL REGISTERS

F4h	D7	D6	D5	D4	D3	D2	D1	D0
Slow CPU	X	X	X	X	X	X	X	X

F5h	D7	D6	D5	D4	D3	D2	D1	D0
Fast CPU	X	X	X	X	X	X	X	X

The VL82C486 implements two methods for slowing CPU execution speed: slowing the CPU clock frequency and/or modulating the –EADS signals to the CPU. Both of these features are turned on by a dummy write to location F4h and turned off by a dummy write to location F5h. However, a write to location F5h turns off the –EADS modulation only if the TURBO pin is high. Also, if a write to either of these locations results in a CLK frequency change, then a 1 ms CPU-only reset will be issued.

CPU Speed Control Registers are controlled by the –VSF bit in the BUSCTL Register. –VSF should be 0 to enable these registers. However, if –VSF is disabled, it is still possible to control the CPU speed using the –EADS modulation with the keyboard controller if allowed by the BIOS.

An I/O read operation on these two addresses returns undefined data.

TABLE 49. CONFIGURATION ENABLE AND DISABLE REGISTERS

FBh	D7	D6	D5	D4	D3	D2	D1	D0
Config Enable	X	X	X	X	X	X	X	X

F9h	D7	D6	D5	D4	D3	D2	D1	D0
Config Disable	X	X	X	X	X	X	X	X

When enabled and used as described, the Configuration Registers are protected from unauthorized accesses that might garble the system configuration and either crash the system or change its operational characteristics in an unwanted manner. A dummy write to FBh enables the Configuration Registers and a dummy write to F9h disables them. When disabled, the system is locked out from write access to the configuration and control ports from address E8h through EFh. This includes the registers previously described in this subsection and the Configuration Indexed Registers.

If the –VSF bit in the BUSCTL Register is disabled, the Configuration Enable/Disable feature is also disabled.

An I/O read operation from these two addresses returns undefined data.

TABLE 50. NMI LOGIC

70h	D7	D6	D5	D4	D3	D2	D1	D0
NMI Enable	X	X	X	X	X	X	X	X

The VL82C486 generates the Non-Maskable Interrupt (NMI) output pin for the CPU. NMI is enabled by a write to I/O address 70h with D7 (data bit 7) low. Once enabled, an NMI can be generated by the –IOCHCK input going low or a parity error. Each of these NMI sources has an enable bit in the Port B Register.

PORT B REGISTER
The Port B Register at I/O address 61h is included in the VL82C486 chip. This register contains bits to control the speaker output and NMI circuitry. Bits 0 through 3 are read/write bits, while bits 4 through 7 are read-only bits. Each bit of the register is defined in Table 51. Bits 0 through 3 are all set low by a reset.

TABLE 51. PORT B REGISTER

61h	D7	D6	D5	D4	D3	D2	D1	D0
Port B	PCK	CHAN_CHK	OUT2	REFDET	ENA_IO_CHK	ENA_RAM_PCK	SPK_DAT	TIM2GAT_SPK

Bit	Name	Function
7	PCK	Parity Check: This bit indicates that an on-board RAM parity error has occurred. It can only be set if ENA_RAM_PCK is set to 0. PCK should be cleared by writing a 1 to ENA_RAM_PCK.
6	CHAN_CHK	Channel Check: This bit indicates that a peripheral device is reporting an error. It can only be set if ENA_IO_CHK is set low. CHAN_CHK should be cleared by writing a 1 to ENA_IO_CHK.
5	OUT2	Timer Output Bit 2 State: This bit indicates the current state of the OUT2 signal from the 82C54 megacell.
4	REFDET	Refresh Detect: This bit is tied to a toggle flip-flop which is clocked by REFRESH. It toggles to the opposite state every time a refresh cycle occurs.
3	ENA_IO_CHK	Enable I/O Check: When this bit is set low, it allows an NMI to be generated if the –IOCHCK input is pulled low. Otherwise, the -IOCHCK input is ignored and can not generate an NMI.
2	ENA_RAM_PCK	Enable RAM Parity Check: When this bit is set low, it allows parity errors from the on-board RAM memory to cause an NMI. When high, on-board RAM parity errors do not cause an NMI.
1	SPK_DAT	Speaker Data: This bit is gated with the output of Counter 2 from the 82C54 megacell. When it is high, it allows the OUT2 frequency to be passed out on the SPKR pin. When low, the SPKR output is forced low.
0	TIM2GAT_SPK	Speaker Timer 2 Gate: This bit goes to the Gate 2 input on the 82C54 megacell to enable Counter 2 to produce a speaker frequency.

IN-CIRCUIT TEST LOGIC

The VL82C486 is designed to make system board testing as easy as possible. Pulling the SPKR/–TRI input low while POWERGOOD is low causes all pins on the VL82C486 to go to a high impedance state. This mode can be used to isolate the VL82C486 so that other components in the system may be tested.

The SPKR/–TRI input can also be used to put the VL82C486 into a special test mode called In-Circuit Test (ICT) Mode. The purpose of the ICT Mode is to test that all the VL82C486's pins can be toggled high and low in a predictable pattern. It uses a type of multiplexing scheme between inputs and outputs to allow easy access and testing of each pin.

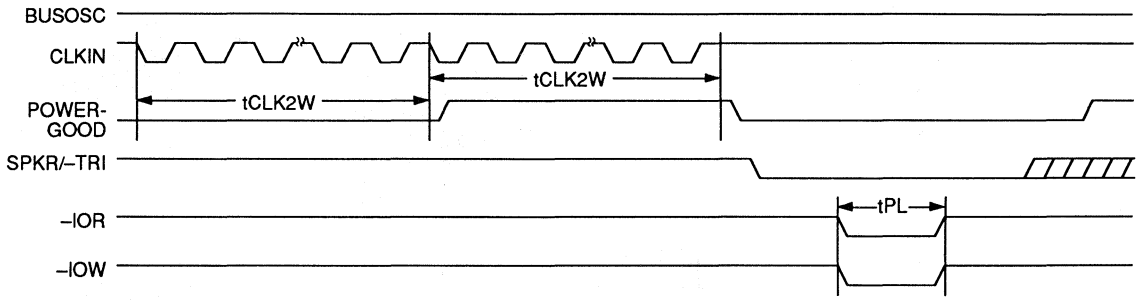
The VL82C486 has a number of internal test modes in order to completely test the functionality of the circuit. The test modes are disabled upon reset. The following procedure should be followed to place the VL82C486 into the ICT Mode (refer to Figure 43):

1) Drive the POWERGOOD pin low.
2) Drive the SPKR/–TRI pin low.
3) Invoke the ICT Mode by toggling the –IOR and –IOW pins together.
4) Release the SPKR/–TRI pin (i.e., allow it to float).
5) Return the POWERGOOD pin to high.

Note: CLKIN must initially be allowed to operate in conjunction with POWERGOOD as this is necessary to initialize internal logic. Once in the ICT Mode, CLKIN and BUSOSC must not be allowed to operate as this will cause a system reset. Also, once in the ICT Mode, the POWERGOOD and SPKR/–TRI pins should not be driven low simultaneously.

To exit the ICT Mode perform a system reset.

FIGURE 43. ICT MODE TIMING WAVEFORM



Timing Definition:

tpl	=	minimum –IOR, –IOW pulse width
tPL	=	100 ns
tCLKW	=	minimum 25 CLKINs

TABLE 52. PIN ASSIGNMENT FOR ICT MODE

ICT Input		ICT Output		ICT Input		ICT Output	
Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
DRQ3	1	D31	17	CLKIN	54	–BRDY	65
DRQ2	2	D30	18	–IGGNE	56	–FLUSH	55
DRQ1	3	D29	19	A26	143	–EADS	61
DRQ0	4	D28	20	–FERR	57	–RDY	62
IRQ15	5	D27	21	TCLK2	59	RESCPU	58
IRQ14	6	D26	23	CLK	53	–BE0	79
IRQ12	7	D25	24	–BLAST	63	HOLD	67
IRQ11	8	D24	25	HLDA	66	W/–R_DK2	68
IRQ10	9	D23	26	–ADS	71	D/–C_DK1	69
IRQ9	10	D22	27	–SLEEP	75	M/–IO_DK0	70
IRQ7	11	D21	29	MA0X	98	–EALE	74
IRQ6	12	D20	30	–MISS	72	–BLKA20	76
IRQ5	13	D19	31	A11	125	SD11	189
IRQ4	14	D18	32	A10	124	SD10	190
IRQ3	15	D17	34	A9	123	–BE2	81
A31	145	D16	35	A8	122	–BE3	82
A29	144	D15	36	A7	121	–SBHE	171
A25	142	D14	37	A6	120	–MDENY	170
A24	140	D13	38	A5	119	NMI	78
A23	139	D12	39	A4	118	TC	159
A22	137	D11	40	A3	117	–IOW	160
A21	136	D10	41	A2	116	–IOR	161
MA10	108	D0	51	–SPKR/–TRI	85	–KEN	73
A20	135	D9	42	POWERGOOD	178	–SMEMW	176
A19	134	D8	43	CAS0	91	MBE0	86
MA3	100	D7	44	CAS1	92	MBE1	87
MA4	101	D6	45	CAS2	93	MBE2	88
MA5	102	D5	46	CAS3	94	MBE3	89
MA6	103	D4	47	–LBA	146	–MDENX	169
MA7	105	D3	48	MA1	97	–FMPRG	83
MA8	106	D2	49	MA2	99	INTR	84
MA9	107	D1	50	A18	133	RSTDRV	173

TABLE 52. PIN ASSIGNMENT FOR ICT MODE (Cont.)

ICT Input		ICT Output		ICT Input		ICT Output	
Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
A17	131	–SMEMR	174	OSCIN	151	–MEMW	179
A16	130	SYSCLK	175	–IOCHCK	152	DKEN	180
A15	129	–ROMCS	163	IOCHRDY	153	BALE	182
A14	128	SD15	184	–WS0	154	AEN	183
A13	127	SD14	185	–MASTER	181	SD9	191
A12	126	SD13	186	MA0Y	95	–BE1	80
–RAMW	114	SD12	188	BUSOSC	158	–REFRESH	157
–RAS0	110	PAR0	164	TURBO	155	SD8	192
–RAS1	111	PAR1	165	DRQ7	202	SD4	197
–RAS2	112	PAR2	166	DRQ6	203	SD5	196
–RAS3	113	PAR3	167	DRQ5	204	SD3	198
–MEMCS16	147	SD7	194	–IRQ8	205	SD2	199
–IOCS16	148	SD6	195	WEIRQ	206	SD1	200
SA1	149	–PPICS	162	IRQ1	207	SD0	201
SA0	150	–MEMR	177				

VL82C486 RESET OPTIONS

RESET SEQUENCE

The VL82C486's power-on reset occurs in response to an active POWERGOOD signal.

There are two reset signals, RESCPU and RSTDRV, that are generated by the VL82C486.

The CPU reset signal, RESCPU, can be generated individually as described, or as a result of a system reset when RSTDRV is also generated. The RSTDRV signal is held active for at least two CPU clocks longer than the RESCPU signal.

The input signal POWERGOOD must be low during power-on (system) reset, but has no effect during a software reset. When a system reset is generated, the RSTDRV signal is enabled on the next high going edge of BUSOSC which in turn three-states –RAS and CAS. A system reset causes both the RESCPU and RSTDRV signals to be made active for as long as POWERGOOD is low, but also for at least 1 ms, even if POWERGOOD goes high before this time. At the end of reset, the –RAS and CAS outputs are activated on the fourth high-to-low transition of the –ADS input to allow time to transfer DRAM refresh control back to the VL82C486. This is depicted in Figure 44.

RESET MODES

This section summarizes all reset modes of the VL82C486 based on their activating signal.

POWER GOOD This signal causes all internal state machines to be reset. The Internal Configuration Registers are reset to their default values shown by the diagrams in the section titled "Register Summary" starting on page 107. Reset is issued to the CPU via the RESCPU signal. RSTDRV is generated from POWERGOOD and is synchronized with BUSOSC. The RSTDRV signal may be connected to the AHOLD input of the 486. This invokes the Self-Test Mode of the 486. Systems that desire to use this feature can then read the result of this test in the 486's Self-Test Registers and decide what to do based on the result. Otherwise, it can be ignored.

REG_{92} Setting bit 0 of I/O Port 92h causes a CPU-only reset after a 6.72 µs delay. RESCPU is activated for 16 CLKIN cycles.

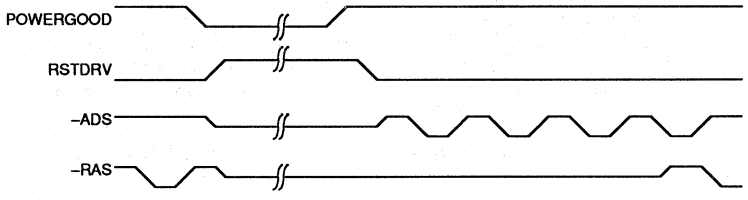
REG_{EF} A dummy read of I/O Port EFh causes a CPU-only reset after a 6.72 µs delay. RESCPU is activated for 16 CLK2 cycles. VLSI Special Features must be enabled for this feature to function.

OUT_64 The CPU is reset when I/O Port 64h is loaded with the value FCh or FEh. This generates an internal reset signal equivalent to –RC from a keyboard controller. The internal –RC is active after 6.72 µs or about 50 µs delay depending on the value of the FASTRC* bit in the MISCSET Register. The pulse width of this signal is 16 CLK cycles. It generates RESCPU.

SHUT DOWN Detection of the Shutdown condition causes a CPU-only reset for 16 CLK2 cycles. See the previous section titled "Reset Sequence" for additional information.

FASTRC BIT The FASTRC bit (bit 5) in the MISCSET Register (at indexed location 07h) can be used to remove the delay normally associated with generation of –RC. For hardware compatibility, the internally generated –RC has a 50 µs delay from the issuance of the command to write data FCh or FEh to Port 64h (which generates a low going 6 µs pulse on –RC). This delay can be reduced by using the FASTRC bit. If set to 1, there is only a 6.72 µs delay introduced. The default value is 0.

FIGURE 44. RESET SEQUENCE



REGISTER SUMMARY

SYSTEM CONFIGURATION

The VL82C486 offers hardware configureable options to ensure that it resets to a usable state with the various physical configurations available.

During reset, the output pins listed in Table 53 become inputs and their value is loaded into the Configuration Registers as shown or are used to configure the system. There is no internal default for these bits, therefore the pins shown must be set to the required value during reset. Table 53 details the mapping.

TABLE 53. SYSTEM CONFIGURATION INITIALIZATION

Pin	Register		Bit Name	Functional Description	
	Name	Bit			
–PPICS –BLKA20	RAMSET	2 1	RAMDRV1 RAMDRV0	MA10-MA0 and –RAMW Drive	00 = 12 mA 01 = 24 mA 10 = 36 mA 11 = 48 mA
–ROMCS	RAMSET	3	CONFB	DRAM Configuration	0 = Configuration A 1 = Configuration B
–RAMW	ROMSET	6	ROMMOV2	System and Slot BIOS ROM Move	
DKEN	ROMSET	7	ROMWID	ROM Width	0 = 8-bit 1 = 16-bit
–FMPRG	BUSCTL	5	SLTDRV	Slot Current Drive	0 = 12 mA 1 = 24 mA
–IGNNE				SA1 Timing during 32-bit ISA Conversion Cycles	0 = SA1 generated as normal for when it is connected directly to the ISA bus 1 = SA1 generated early in 32-to-16 bit or 32-to-8 bit conversion cycles (for VL82C107 and VL82C113A compatibility)
–FLUSH				DKEN Polarity	0 = DKEN active low 1 = DKEN active high
–EALE				–MISS Operation during DMA/Master Cycles	0 = Write-Back Cache Mode (VL82C425) 1 = Write-Through Cache Mode (Intel 485)

TABLE 54. INDEXED CONFIGURATION REGISTERS FORMAT

The following diagrams show the indexed configuration register formats. Power-on reset values are shown above the diagrams for each register or set of registers.

INDEX PORT (R/W) **ECh**

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Index Address of a Configuration Register

DATA PORT (R/W) **EDh**

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Data for a Configuration Register

VERSION (R-O) **00h**

7	6	5	4	3	2	1	0
1	0	0	1	1	0	0	0

VL82C486 Version

DRAM PROGRAMMABLE TIMING - RAMTMG (R/W) - SEE PAGE 44 **01h**

7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1
TRST1	TRST0	TRP1	TRP0	TRCD1	TRCD0	TCAS1	TCAS0

Earliest Cycle-Start Point	RAS Precharge	RAS-to-CAS Delay	CAS Width Read/Write
00 = Begin First T2	00 = 1T	00 = 1T	00 = 1T (R), 1T (W)
01 = Mid First T2	01 = 2T	01 = 2T	01 = 1.5T (R), 1T (W)
1X = End First T2	10 = 3T	10 = 3T	10 = 2T (R), 1T (W)
	11 = 4T	11 = 4T	11 = 2T (R), 2T (W)

TABLE 54. INDEXED CONFIGURATION REGISTERS FORMAT (Cont.)

DRAM CONFIGURATION REGISTER 0 - RAMCFG0 (R/W) - SEE PAGE 35 **02h**

7	6	5	4	3	2	1	0
1	0	0	0	1	0	1	0
	DRAM Bank 1 Type		S/D 1		DRAM Bank 0 Type		S/D 0

DRAM CONFIGURATION REGISTER 1 - RAMCFG1 (R/W) - SEE PAGE 35 **03h**

7	6	5	4	3	2	1	0
1	0	0	0	1	0	0	0
	DRAM Bank 3 Type		S/D 3		DRAM Bank 2 Type		S/D 2

DRAM Bank 3 Type: 00 = None, 01 = 256K, 10 = 1M, 11 = 4M

S/D 3: SIMM Type, 0 = Single-sided, 1 = Double-sided

DRAM CONTROL REGISTER - RAMSET (R/W) - SEE PAGE 56 **04h**

7	6	5	4	3	2	1	0
0	0	0	0	–ROMCS	–PPICS	–BLKA20	0
INTLV2	INTLV1	INTLV0	RTODIS	CONFB	RAMDRV1	RAMDRV0	PGMD

INTLV2, INTLV1, INTLV0: Interleave Select
000 = No Interleave, 100 = Banks 2, 3
001 = Banks 0, 1, 101 = Banks 0, 1 or 2, 3
010 = Banks 0, 3, 110 = Banks 0, 3 or 1, 2
011 = Banks 1, 2, 111 = 4-way Interleave

RTODIS: –RAS Time-Out Disable, 0 = Enable, 1 = Disable

CONFB: Configuration Bit (Read-Only), 0 = 32-bit (Config. A), 1 = 64-bit (Config. B)

RAMDRV1: MA10-MA1 & –RAMW Drive, 00 = 12 mA, 01 = 24 mA, 10 = 36 mA, 11 = 48 mA

RAMDRV0: –RAS, MA0X, & MA0Y Drive, 0X = 12 mA, 1X = 24 mA

PGMD: Page Mode, 0 = Enable, 1 = Burst-only

NON-TURBO AND REFRESH CONTROL REGISTER - NTBREF (R/W) - SEE PAGE 57 **05h**

7	6	5	4	3	2	1	0
0	0	0	TURBO	0	0	0	0
NTB2	NTB1	NTB0	TURBO	REFMD1	REFMD0	CASREF	REFSPD

NTB2, NTB1, NTB0: Non-Turbo Mode Speed
000 = Full Speed, 100 = 80%
001 = 50%, 101 = 83.3%
010 = 66.6%, 110 = 85.7%
011 = 75%, 111 = 97.5%

TURBO: State of TURBO Pin (Read-Only)

REFMD1, REFMD0: Refresh Mode, 00 = Synchronous, 01 = Asynchronous, 1X = Decoupled

CASREF: Refresh Type, 0 = Ras-Only, 1 = CAS-before -RAS

REFSPD: Refresh Period, 0 = 15.625 µs, 1 = 125 µs

TABLE 54. INDEXED CONFIGURATION REGISTERS FORMAT (Cont.)

CLOCK CONTROL REGISTER - CLKCTL (R/W) - SEE PAGE 64

06h

7	6	5	4	3	2	1	0
0	0	0	1	1	*	1	1
FBEN	CLKDIV1	CLKDIV0	FCLKDIV1	FCLKDIV0	BOSCNS	SCLKDIV1	SCLKDIV0

- **FBEN** — Enable SYSCLK Freq. Change in Fast Bus Clock Region: 0 = Disable, 1 = Enable
- **CLKDIV1, CLKDIV0** — Clock Divider in Non-Turbo Mode: 00 = CLK = TCLK2 ÷2, 01 = CLK = TCLK2 ÷4, 10 = CLK = TCLK2 ÷6, 11 = CLK = TCLK2 ÷8
- **FCLKDIV1, FCLKDIV0** — Fast Clock Divider BUSOSC / TCLK2: 00 = ÷ 2 / 2, 01 = ÷ 4 / 4, 10 = ÷ 6 / 6, 11 = ÷ 8 / 8
- **BOSCNS** — BUSCLK Pin Status: 0 = Slow Clock, 1 = Fast Clock
- **SCLKDIV1, SCLKDIV0** — Slow Clock Divider BUSOSC / TCLK2: 00 = ÷ 2 / 4, 01 = ÷ 4 / 6, 10 = ÷ 6 / 8, 11 = ÷ 8 / 12

*Reset value is 0 if an oscillator is connected to BUSOSC pin, else the state of the BUSOSC pin is reflected.

MISCELLANEOUS CONTROL REGISTER - MISCSET (R/W) - SEE PAGE 57

07h

7	6	5	4	3	2	1	0
0	–SLEEP	1	0	0	0	0	1
SLP	SLPSTS	ENSYSCK	FASTRC	CEN	–ENPAR	CWS_OFF	IRQIN

- **SLP** — Sleep Mode: 0 = Disable, 1 = Enable
- **SLPSTS** — Sleep Pin Status (Read-Only)
- **ENSYSCK** — System Clock (in Sleep Mode): 0 = Disable, 1 = Enable
- **FASTRC** — Fast Internal –RC: 0 = Disable, 1 = Enable
- **CEN** — Cache Enable: 0 = Disable, 1 = Enable
- **–ENPAR** — Enable Parity Gen/Check: 0 = Enable, 1 = Disable
- **CWS_OFF** — Conditional Wait States: 0 = Enable, 1 = Disable
- **IRQIN** — Glitch-Free Interrupt Request Input: 0 = Disable, 1 = Enable

DMA CONTROL REGISTER - DMACTL (R/W) - SEE PAGE 84

08h

7	6	5	4	3	2	1	0
0	0	1	1	1	0	0	0
ENBLFF	FFPTR	DMAWS8(1)	DMAWS8(0)	DMAWS16(1)	DMAWS16(0)	DMACLK	MEMTM

- **ENBLFF** — Enable Extended DMA Addr.: 0 = Disable, 1 = Enable
- **FFPTR** — Enable Access to Upper Page Registers: 0 = Lower, 1 = Upper
- **DMAWS8(1), DMAWS8(0)** — 8-Bit DMA Wait States: 00 = 2 WS, 01 = 4 WS, 10 = 3 WS, 11 = 3 WS
- **DMAWS16(1), DMAWS16(0)** — 16-Bit DMA Wait States: 00 = 2 WS, 01 = 4 WS, 10 = 3 WS, 11 = 3 WS
- **DMACLK** — DMA Clock: 0 = SYSCLK ÷2, 1 = SYSCLK
- **MEMTM** — DMA –MEMR Signal Delay: 0 = PC/AT -compat., 1 = 1 DMA CLK Early

TABLE 54. INDEXED CONFIGURATION REGISTERS FORMAT (Cont.)

BUS CONTROL REGISTER - BUSCTL (R/W) - SEE PAGE 79 **09h**

7	6	5	4	3	2	1	0
0	0	–FMPRG	0	0	0	0	0
–VSF	10/16IO	SLTDRV	DSKTMG	CMDLY2	CMDLY1	16WS	8WS

- –VSF: VLSI Special Features (Enable I/O Space EEh-FFh) 0 = Enable 1 = Disable
- 10/16IO: 10/16 Bit I/O Address Decode 0 = 16-bit 1 = 10-bit
- SLTDRV: Slot Drive Current 0 = 12 mA 1 = 24 mA
- DSKTMG: Disk I/O Timing 0 = Slow 1 = Fast
- CMDLY2: Command Delay for: 8-,16-Bit I/O & 8-Bit Memory Cycles 1/2 = 0 SYSCLK 1 = 1 SYSCLK
- CMDLY1: Command Delay for: 16-Bit Memory Cycles 0 = 0 SYSCLK 1/2 = 1 SYSCLK
- 16WS: 16-Bit Wait States 0 = 0 WS 1 = 1 WS
- 8WS: 8-Bit Wait States 0 = 4 WS 1 = 5 WS

FAST BUS CLOCK REGION REGISTER - FBCR (R/W) - SEE PAGE 62 **0Bh**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
A23	A22	A21	A20	A19	A18	A17	A16

Address Bits 23-16 of Memory Region Selected for Fast Bus Clock Access

ROM CONTROL REGISTER - ROMSET (RW) - SEE PAGE 32 **0Ch**

7	6	5	4	3	2	1	0
–DKEN	–RAMW	0	0	0	0	0	0
ROMWID	ROMMOV2	ROMMOV1	ROMMOV0	MBIOS	FMPRG	ROMWS1	ROMWS0

- ROMWID: BIOS ROM Width (Read-Only) 0 = 8-Bit 1 = 16-Bit
- ROMMOV2, ROMMOV1, ROMMOV0: System & Slot ROM Location Code
- MBIOS: Middle BIOS Enable 0 = Enable 1 = Disable
- FMPRG: Flash Memory Program 0 = Disable 1 = Enable
- ROMWS1, ROMWS0: ROM Wait States 00 = 3 WS 01 = 1 WS 10 = 2 WS 11 = 3 WS

TABLE 54. INDEXED CONFIGURATION REGISTERS FORMAT (Cont.)

A0000h-FFFFFh SEGMENT ACCESS CONTROL REGISTERS - SEE PAGE 25
AAXS, BAXS, CAXS, DAXS, EAXS, FAXS (R/W) **0Dh-12h**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

AC000 Access	A8000 Access	A4000 Access	A0000 Access
BC000 Access	B8000 Access	B4000 Access	B0000 Access
CC000 Access	C8000 Access	C4000 Access	C0000 Access
DC000 Access	D8000 Access	D4000 Access	D0000 Access
EC000 Access	E8000 Access	E4000 Access	E0000 Access
FC000 Access	F8000 Access	F4000 Access	F0000 Access

00 = Read/Write Slot Bus
01 = Read Slot, Write System Board
10 = Read System Board, Write Slot Bus
11 = Read/Write System Board

A0000h-FFFFFh SEGMENT CACHEABILITYCONTROL REGISTERS - SEE PAGE 27
ACBL, BCBL, CCBL, DCBL, ECBL, FCBL (R/W) **13h-18h**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

AC000 Access	A8000 Access	A4000 Access	A0000 Access
BC000 Access	B8000 Access	B4000 Access	B0000 Access
CC000 Access	C8000 Access	C4000 Access	C0000 Access
DC000 Access	D8000 Access	D4000 Access	D0000 Access
EC000 Access	E8000 Access	E4000 Access	E0000 Access
FC000 Access	F8000 Access	F4000 Access	F0000 Access

00 = Not Write-Protected, Cacheable
01 = Not Write-Protected, Not Cacheable
10 = Write-Protected, Cacheable
11 = Write-Protected, Not Cacheable

TABLE 54. INDEXED CONFIGURATION REGISTERS FORMAT (Cont.)

PROGRAMMED MEMORY REGION ADDRESS REGISTER 1 - PMRA1 (R/W) - SEE PAGE 28 **20h**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
LBA_ISA	NCBL	AX5	AX4	AX3	AX2	AX1	AX0

Select Bus
0 = ISA Bus
1 = Local Bus

Select Cacheability
0 = Cacheable
1 = Non-Cacheable

Start Address and Memory Region Size

0	A23	A22	A21	A20	A19	Start Address of a 512 KB Region in Lower 16 MB Memory
1	0	A26	A25	A24	A23	Start Address of an 8 MB Region in Lower 128 MB Memory
1	1	A17	A16	A15	A14	Start Address of a 16 KB Region in Range C0000h to FFFFFh

PROGRAMMED MEMORY REGION ENABLE REGISTER 1 - PMRE1 (R/W) - SEE PAGE 28 **21h**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0

Sub-Region Enables for Remapping and/or Cacheability

0 = Default Mapping/Cacheability
1 = Mapping and Cacheability defined by PMRA

PROGRAMMED MEMORY REGION ADDRESS REGISTER 2 - PMRA2 (R/W) - SEE PAGE 28 **22h**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
LBA_ISA	NCBL	AX5	AX4	AX3	AX2	AX1	AX0

PROGRAMMED MEMORY REGION ENABLE REGISTER 2 - PMRE2 (R/W) - SEE PAGE 28 **23h**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0

TABLE 55. INDEXED CONFIGURATION REGISTERS MAP

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
The following I/O mapped registers are used to access the Indexed Configuration Registers:									
ECh (R/W)	Index Port	A7	A6	A5	A4	A3	A2	A1	A0
EDh (R/W)	Data Port	D7	D6	D5	D4	D3	D2	D1	D0
The following registers are accessed by writing their address into the Index Port and reading/writing their data via the Data Port:									
00h (R-O)	VER	0	1	1	0	1	0	0	1
01h (R/W)	RAMTMG	TSTRT (1 & 0)		TRP (1 & 0)		TRCD (1 & 0)		TCAS (1 & 0)	
02h (R/W)	RAMCFG0	1	DRAM Bank 1 Type		S/D 1	1	DRAM Bank 0 Type		S/D 0
03h (R/W)	RAMCFG1	1	DRAM Bank 3 Type		SD 3	1	DRAM Bank 2 Type		S/D 2
04h (R/W)	RAMSET	INTLV (2-0)			RTODIS	CONFB	RAMDRV (1 & 0)		PGMD
05h (R/W)	NTBREF	NTB (2-0)			TURBO	REFMD (1 & 0)		CASREF	REFSPD
06h (R/W)	CLKCTL	FBEN	CLKDIV (1 & 0)		FCLKDIV (1 & 0)		BOSCSNS	SCLKDIV (1 & 0)	
07h (R/W)	MISCSET	SLP	SLPSTS	ENSYSCK	FASTRC	CEN	–ENPAR	CWS_OFF	IRQIN
08h (R/W)	DMACTL	ENBLFF	FFPTR	DMAWS8 (1 & 0)		DMAWS16 (1 & 0)		DMACLK	MEMTM
09h (R/W)	BUSCTL	–VSF	10/16 IO	SLTDRV	DSKTMG	CMDLY2	CMDLY1	16WS	8WS
0Bh (R/W)	FBCR	A23	A22	A21	A20	A19	A18	A17	A16
0Ch (R/W)	ROMSET	ROMWID	ROMMOV (2-0)			MBIOS	FMPRG	ROMSW (1 & 0)	
0Dh (R/W)	AAXS	AC000 Access		A8000 Access		A4000 Access		A0000 Access	
0Eh (R/W)	BAXS	BC000 Access		B8000 Access		B4000 Access		B0000 Access	
0Fh (R/W)	CAXS	CC000 Access		C8000 Access		C4000 Access		C0000 Access	
10h (R/W)	DAXS	DC000 Access		D8000 Access		D4000 Access		D0000 Access	
11h (R/W)	EAXS	EC000 Access		E8000 Access		E4000 Access		E0000 Access	
12h (R/W)	FAXS	FC000 Access		F8000 Access		F4000 Access		F0000 Access	
13h (R/W)	ACBL	AC000 Access		A8000 Access		A4000 Access		A0000 Access	
14h (R/W)	BCBL	BC000 Access		B8000 Access		B4000 Access		B0000 Access	
15h (R/W)	CCBL	CC000 Access		C8000 Access		C4000 Access		C0000 Access	
16h (R/W)	DCBL	DC000 Access		D8000 Access		D4000 Access		D0000 Access	
17h (R/W)	ECBL	EC000 Access		E8000 Access		E4000 Access		E0000 Access	
18h (R/W)	FCBL	FC000 Access		F8000 Access		F4000 Access		F0000 Access	
20h (R/W)	PMRA1	LBA_ISA	NCBL	AX5	AX4	AX3	AX2	AX1	AX0
21h (R/W)	PMRE1	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0
22h (R/W)	PMRA2	LBA_ISA	NCBL	AX5	AX4	AX3	AX2	AX1	AX0
23h (R/W)	PMRE2	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0

TABLE 56. DEDICATED I/O CONTROL REGISTERS

Port Addr.	Name	Access	Function
61h	Port B	R/W	Miscellaneous control bits.
70h	NMI Enable	W	Enables non-maskable interrupts.
92h	Port A	R/W	Fast A20 and reset control.
ECh	Configuration Index Register	R/W	Contains the address of one of the Configurations Registers noted in the "Indexed Configurations Registers Format" on page 107.
EDh	Configuration Data Port	R/W	Contains the data written to the Configuration Register selected by the Configuration Index Register.
EEH*+	Fast A20 Register	R/W	A dummy read enables Fast A20. A dummy write disables Fast A20.
EFh*+	Fast CPU Reset Register	R	A dummy read resets the CPU.
F0h	Coprocessor Busy Register	W	A dummy write clears IRQ13 and sets –IGNNE.
F1h	Coprocessor Reset Register	W	A dummy write clears IRQ13 and sets –IGNNE.
F4h+	Slow CPU Register	W	A dummy write enables Slow Clock and Non-Turbo Mode for the CPU.
F5h+	Fast CPU Register	W	A dummy write enables Fast Clock and Turbo Mode for the CPU.
F9h+	Configuration Disable Register	W	A dummy write disables access to the Configuration Registers.
FBh+	Configuration Enable Register	W	A dummy write enables access to the Configuration Registers.

* Also can be activated through Port 92h for PS/2 compatibility.
\+ Can be disabled by setting the MSB (most significant bit) of the BUSCTL Register in case of a conflict.

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Figure	Condition
Clocks						
f_TC2	TCLK2 Frequency		66	MHz		2x Processor Clock Frequency
tP_TC2	TCLK2 Period	15		ns	45	
tH_TC2	TCLK2 High Time	6		ns	45	VIL = VIH = 2.0 V
tL_TC2	TCLK2 Low Time	6		ns	45	VIL = VIH = 2.0 V
tD_CLK	TCLK2 to CLK Delay	3	35	ns		CL = 50 pF
tH_CLK	CLK High Time	13		ns	45	@ TCLK2 = 66 MHz, VOH = 2.0 V
tL_CLK	CLK Low Time	13		ns	45	@ TCLK2 = 66 MHz, VOH = 0.8 V
tR_CLK	CLK Rise Time		3	ns	45	0.8 V to 3.6 V, CL = 50 pF
tFA_CLK	CLK Fall Time		3	ns	45	3.6 V to 0.8 V, CL = 50 pF
f_CKIN	CLKIN Frequency		33	MHz		Processor Clock
tP_CKIN	CLKIN Period	30		ns	45	
tH_CKIN	CLKIN High Time	12		ns	45	VIL = VIH = 2.0 V
tL_CKIN	CLKIN Low Time	12		ns	45	VIL = VIH = 2.0 V
tP_BOSC	BUSOSC Period	20		ns	45	
tH_BOSC	BUSOSC High Time	8		ns	45	VIL = 0.8 V, VIH = 2.0 V
tL_BOSC	BUSOSC Low Time	8		ns	45	VIL = 0.8 V, VIH = 2.0 V
tR_SCK	SYSCLK Rise Time		10	ns	45	VOL = 0.8 V, VOH = 2.0 V, CL = 200 pF
tFA_SCK	SYSCLK Fall Time		10	ns	45	VOL = 0.8 V, VOH = 2.0 V, CL = 200 pF
tD1_SCK	TCLK2 to SYSCLK Delay	5	48	ns		CL = 200 pF
tD2_SCK	BUSOSC to SYSCLK Delay	5	50	ns		CL = 200 pF
tP_OSC	OSC Period	69.8		ns	45	14.31818 MHz Clock
tH_OSC	OSC High Time	20		ns	45	VIL = 0.8 V, VIH = 2.0 V
tL_OSC	OSC Low Time	20		ns	45	VIL = 0.8 V, VIH = 2.0 V
CPU Interface Synchronous Timing						
tS1_CPU	–ADS, M/–IO, W/–R, D/–C to CLKIN Setup	25		ns	46	To Rising Edge of CLKIN, RAMTMG[TSTRT1,0] = 00
tS2_CPU	–ADS, M/–IO, W/–R, D/–C to CLKIN Setup	13		ns	46	To Rising Edge of CLKIN, RAMTMG[TSTRT1,0] = 01 or 10
tS3_CPU	A26-A2, A29, A31, –BE3 - –BE0 to CLKIN Setup	25		ns	46	To Rising Edge CLKIN, end of T1, if RAMTMG[TSTRT1,0] = 00 To Falling Edge CLKIN, middle of first T2, if RAMTMG[TSTRT1,0] = 01 To Rising Edge CLKIN, end of first T2, if RAMTMG[TSTRT1,0] = 10

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Figure	Condition
CPU Interface Synchronous Timing (Cont.)						
tS4_CPU	HLDA to CLKIN Setup	6		ns	46	
tS5_CPU	–BLAST to CLKIN Setup	9		ns	46	
tS6_CPU	D31-D0, PAR3-PAR0 to CLKIN Setup	5		ns	46	For Parity Check and Local Bus DMA/Master Mode cycles
tS7_CPU	–RDY, –BRDY to CLKIN Setup	5		ns	46	Local Bus Time-out or Local Bus DMA/Master Mode cycles
tS8_CPU	–MISS, –LBA to CLKIN Setup	13		ns	46	To Rising Edge CLKIN, end of T1, if RAMTMG[TSTRT1,0] = 00 and On-board DRAM region To Falling Edge CLKIN, middle of first T2, if RAMTMG[TSTRT1,0] = 01 and On-board DRAM region To Rising Edge CLKIN, end of first T2, if RAMTMG[TSTRT1,0] = 10 or not On-board DRAM region
tH_CPU	–ADS, M/–IO, W/–R, D/–C, A31, A29, A26-A2, –BE3 - –BE0, HLDA, –FERR, –BLAST, –RDY, –BRDY, D31-D0, PAR3-PAR0, –MISS, –LBA from CLKIN Hold	3		ns	46	
tD1_CPU	CLKIN to –ADS, M/–IO, W/–R, D/–C, A31, A29, A26-A2, –BE3 - –BE0, –BLAST Delay	4	16	ns	46	CL = 50 pF HDLA Cycles T1 of Local Bus Cycles
tD2_CPU	CLKIN to –RDY, –BRDY, –FLUSH, –EADS, –KEN Delay	4	24	ns	47	CL = 50 pF
tD3_CPU	A31, A29, A26-A2 to –KEN, –EADS Delay		38	ns	47	CL = 50 pF, State Change Occurs only in T2 cycles
tD_HOLD	CLKIN to HOLD Delay	4	23	ns	47	CL = 50 pF
tD_RCPU	CLKIN to RESCPU Delay	4	24	ns	47	CL = 50 pF
tD_NMI	CLKIN to NMI Delay (Parity Error)	5	60		47	CL = 50 pF
tF1_CPU	CLKIN to –ADS, M/–IO, W/–R, D/–C, A31, A29, A26-A2, –BE3 - –BE0, –BLAST Float Delay	4	16	ns	48	CL = 50 pF HDLA Inactive Cycles
tA2_CPU	CLKIN to D31-D0 Active Delay	4	24	ns	48	CL = 50 pF, Slot Bus Reads, second T2 or Local Bus ROM Reads, last T2
tF2_CPU	CLKIN to D31-D0 Float Delay	4	24	ns	48	CL = 50 pF After Slot Bus or Local Bus ROM Read
tF3_CPU	CLKIN to –RDY, –BRDY Float Delay	4	24	ns	48	CL = 50 pF Two Clocks after driven Active

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Figure	Condition
DRAM Controller Interface Timing: CPU Cycles						
tD1_MA	A31, A29, A26-A2 to MA0X, MA0Y, MA10-MA1 Delay	4	60	ns	47	CL (MA10-MA1) = 600 pF CL (MA0X, MA0Y) = 300 pF Conditional Wait States disabled
tD2_MA	A31, A29, A26-A2 to MA0Y, MA10-MA1 Delay	4	30	ns	47	CL (MA10-MA1) = 600 pF CL (MA0X, MA0Y) = 300 pF Conditional Wait States enabled
tD3_MA	CLKIN to MA0X, MA0Y, MA10-MA1 Delay	4	28	ns	47	CL (MA10-MA1) = 600 pF CL (MA0X, MA0Y) = 300 pF
tD1_RAS	CLKIN to –RAS Delay	4	16	ns	47	CL = 150 pF
tD1_CAS	CLKIN to CAS Delay	4	14	ns	47	CL = 50 pF
tD1_MDN	CLKIN to –MDENX, –MENDY Delay	4	16	ns	47	CL = 50 pF. Read cycles, RAMTMG[TCAS] = 1T or 1.5T, or 2T 4121 Cycles
tD2_MDN	CLKIN to –MDENX, –MENDY Delay	4	23	ns	47	CL = 50 pF. Write cycles, or RAMTMG[TCAS] = 2T, non-4121 Cycles
tD1_RMW	CLKIN to –RAMW Delay Time	4	25	ns	47	CL = 600 pF. First T2 of Write Cycles
tD1_MBE	–BE3 - –BE0 to MBE3-MBE0 Delay	4	25	ns	47	CL = 50 pF
tD2_MBE	CLKIN to MBE3-MBE0 Delay	4	25	ns		CL = 50 pF. First T2 of Write and Refresh Cycles
DRAM Controller Interface Timing: HLDA / Refresh Cycles						
tD4_MA	A31, A29, A26-A2 to MA0X, MA0Y, MA10-MA1 Delay	4	60	ns	47	CL (MA10-MA1) = 600 pF, CL (MA0X, MA0Y) = 300 pF. DMA/Master Mode Cycles
tD3_MBE	–CMD to MBE3-MBE0 Vaild Delay	4	25	ns	47	CL = 50 pF DMA/Master Mode Cycles
tD2_RMW	–MEMW to –RAMW Delay	4	30	ns	47	CL = 600 pF
tD2_RAS	HLDA High to –RAS3 - –RAS0 High Delay	4	25		47	CL = 150 pF Start of HLDA Cycles
tD3_RAS	–MEMW/–MEMR to –RAS3 - –RAS0 Delay	4	25	ns	47	CL = 150 pF DMA/Master Mode Cycles
tD2_CAS	OSC to CAS3-CAS0 High Delay	4	25	ns	47	CL = 50 pF DMA/Master Mode Cycles
tD3_CAS	–MEMW/–MEMR to CAS3-CAS0 Low Delay	4	25	ns	47	CL = 50 pF DMA/Master Mode Cycles
tD5_MA	OSC to MA0X, MA0Y, MA10-MA1 Delay	4	35	ns	47	CL (MA10-MA1) = 600 pF CL (MA0X, MA0Y) = 300 pF Row to Column Address Switch
tA1_PAR	–MEMW Low to PAR3-PAR0 Valid Delay	4	25	ns	48	CL = 50 pF
tF1_PAR	–MEMW High to PAR3-PAR0 Float Delay	4	25	ns	48	CL = 50 pF

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Figure	Condition
DRAM Controller Interface Timing: HLDA / Refresh Cycles (Cont.)						
tD_PAR	SD15-SD0 to PAR3-PAR0 Delay	4	48	ns	47	CL = 50 pF
tD4_RAS	OSC to –RAS Delay	4	25	ns	47	CL = 150 pF Rising Edge OSC for –RAS0, –RAS2 Refresh Falling Edge OSC for –RAS1, –RAS3 Refresh
tD4_CAS	OSC to CAS Delay	4	25	ns	47	CL = 50 pF. CAS-before-RAS Refesh
ISA Bus Interface Timing: CPU Cycles						
tD_RMCS	CLKIN to –ROMCS Delay	4	20	ns	47	CL = 50 pF. End First T2 ROM Access
tD_EAL	SYSCLK to –EALE Delay	–6	16	ns	49	CL = 50 pF
tD_BAE	SYSCLK to BALE Delay	–6	10	ns	49	CL = 200 pF
tD_FMP	SYSCLK to –FMPRG Delay	0	50	ns	49	CL = 50 pF. Flash Memory Program Mode
tD_CMD	SYSCLK to –CMD Delay	–6	17	ns	49	CL = 200 pF. –CMD refers to signals –MEMR, –MEMW, –IOR, –IOW
tD_SCMD	SYSCLK to –SCMD Delay	–6	17	ns	49	CL = 200 pF. Addresses below 1 MB
tF_SCMD	SYSCLK to –SCMD Float Delay	–5	25	ns	50	CL = 200 pF. Addresses below 1 MB
tD1_PPS	SYSCLK to –PPICS Delay	4	40	ns		CL = 50 pF
tD1_SA	SYSCLK to SA0, SA1 Delay (Conversion Cycle)	–5	16	ns	49	CL = 200 pF
tD1_SD	SYSCLK to SD15-SD0 Valid Delay	–1	35	ns	49	CL = 200 pF. Slot write Cycles
tF1_SD	SYSCLK to SD15-SD0 Float Delay	–2	30	ns	50	CL = 200 pF. Slot write Cycles
tD1_SPKR	–IOW Inactive to –BLKA20, NMI, SPKR Delay	4	50	ns	51	CL = 50 pF. After Write Strobe to 61h (SPKR/NMI)
tD2_B20	–IOW, –IOR Low to –BLKA20 Delay	4	50	ns	51	CL = 50 pF. For Write to Port 64h or Read from EEh
tD_IGNE	–IOW Low to –IGGNE Low Delay	4	50	ns	51	CL = 50 pF. For Write to Port F0h or F1h
tS_CS16	–MEMCS16, –IOCS16 to SYSCLK Setup	35		ns	49	
tH_CS16	–MEMCS16, –IOCS16 from SYSCLK Hold	–2		ns	49	
tS_WS0	–WS0 to SYSCLK Setup	33		ns	49	
tH_WS0	–WS0 from SYSCLK Hold	–2		ns	49	
tS1_CHR	IOCHRDY to to SYSCLK Setup	33		ns	49	
tH1_CHR	IOCHRDY from SYSCLK Hold	–2		ns	49	
tS_SD	SD15-SD0 to SYSCLK Setup	35		ns	49	To Latch Data during Off-board Read Cycles
tH_SD	SD15-SD0 from SYSCLK Hold	6		ns	49	To Latch Data during Off-board Read Cycles
tS2_D	D31-D0 to SYSCLK Setup	35		ns	49	To Latch Data during Off-board Read Cycles
tH2_D	D31-D0 from SYSCLK Hold	6		ns	49	To Latch Data during Off-board Read Cycles
tD_D	SD15-SD0 to D31-D0 Delay	4	30	ns	47	CL = 50 pF. Slot bus -> On-board Writes
tD2_SD	D31-D0 to SD15-SD0 Delay	4	25	ns	47	CL = 200 pF. Slot bus <- On-board Reads

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Figure	Condition
ISA Bus Interface Timing: CPU Cycles (Cont.)						
tS_IOX	–IOCS16 to –IOR, –IOW Setup	15		ns	51	To meet Data Steering Requirements
tH_IOX	–IOCS16 from –IOR, –IOW Hold	5		ns	51	To meet Data Steering Requirements
tS_MEMX	–MEMCS16 to –MEMR, –MEMW Setup	15		ns	51	To meet Data Steering Requirements
tH_MEMX	–MEMCS16 from –MEMR, –MEMW Hold	5		ns	51	To meet Data Steering Requirements
tS_D	D31-D0 to SYSCLK Setup	75		ns	49	Internal Register Access - CPU Writes
tH_D	D31-D0 from SYSCLK Hold	30		ns	49	Internal Register Access - CPU Writes
ISA Bus Interface Timing: Master Mode						
tD_BE	SA1, SA0 to –BE3 - –BE0 Delay	3	25	ns	52	CL = 50 pF. Used to generate MBE3-MBE0
tD2_PPS	A23-A2, SA1, SA0 to –PPICS Delay	3	40	ns	52	CL = 50 pF
tD1_SCD	–MEMW, –MEMR to –SCMD Delay	3	30	ns	51	CL = 200 pF. –SCMD refers to the signals –SMEMR, –SMEMW
tA1_SCD	A23-A20 to –SCMD Active Delay	3	25	ns	52	CL = 200 pF
tF1_SCD	A23-A20 to –SCMD Float Delay	3	25	ns	52	CL = 200 pF
tS_A	A23-A2, SA1, SA0 to –CMD Setup	30		ns	51	–CMD refers to the signals –MEMR, –MEMW
tH_A	A23-A2, SA1, SA0 from –CMD Hold	20		ns	51	
tS2_SD	SD15-SD0 to –IOW Setup	55		ns	51	Internal Register Access
tH2_SD	SD15-SD0 from –IOW Hold	20		ns	51	Internal Register Access
tD3_SD	–IOR Low to SD15-SD0 Delay	5	120	ns	51	CL = 200 pF. Internal Register Access
tF2_SD	–IOR High to SD15-SD0 Float Delay	4	30	ns	51	CL = 200 pF. Internal Register Access
tA2_SD	–CMD Low to SD15-SD0 Active Delay	4	35	ns	51	CL = 200 pF. On-board Memory Read
tF3_SD	–CMD High to SD15-SD0 Float Delay	4	35	ns	51	CL = 200 pF. On-board Memory Read
tA3_SD	–CMD Low to SD7-SD0 Active Delay	4	50	ns	51	CL = 200 pF. Odd Byte Write to 8-bit Add-on Card
tF4_SD	–CMD High to SD7-SD0 Float Delay	4	35	ns	51	CL = 200 pF. Odd Byte Write to 8-bit Add-on Card
ISA Bus Interface Timing: Refresh Mode						
tL_RFSH	CLKIN to –REFRESH Low Delay	–8	13	ns	50	CL = 200 pF. Waiting for Arbiter Switch
tF_RFSH	CLKIN to –REFRESH Float Delay	–7	18	ns	50	CL = 200 pF
tD2_SA	SYSCLK to SA1, SA0 Delay	–4	40	ns	49	CL = 200 pF
tD_A	SYSCLK to A16-A2 Delay	–4	40	ns	49	CL = 50 pF
tD_MEMR	SYSCLK to –MEMR, –SMEMR Delay	–5	30	ns	49	CL = 200 pF
tS_RFSH	–REFRESH to CLKIN Setup	30		ns	49	External Bus Master Refresh
tH_RFSH	–REFRESH from CLKIN Hold	5		ns	49	External Bus Master Refresh

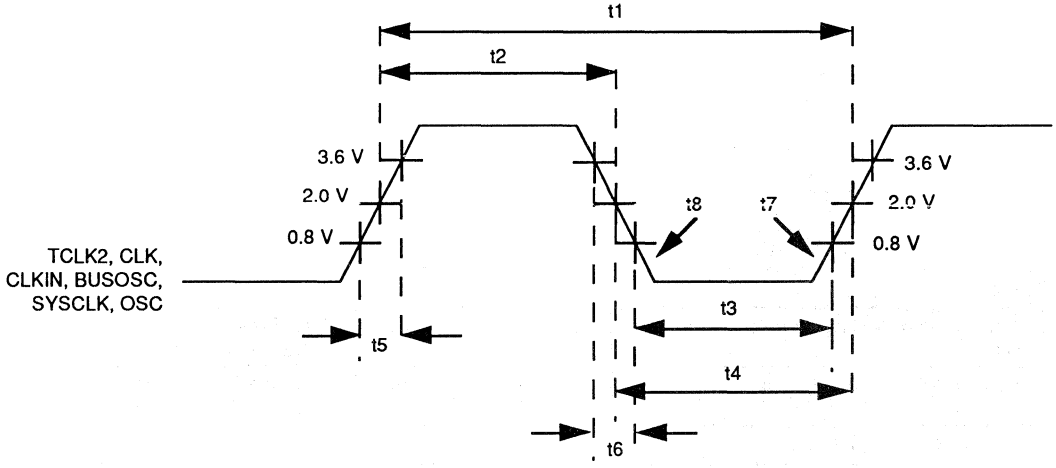
AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Figure	Condition
ISA Bus Interface Timing: Refresh Mode (Cont.)						
tS2_CHR	IOCHRDY to SYSCLK Setup	25		ns	49	
tH2_CHR	IOCHRDY from SYSCLK Hold	0		ns	49	
tD6_MA	CLKIN to MA0X, MA0Y, MA10-MA1 Delay	4	40	ns	47	CL = (MA10-MA1) = 600 pF CL = (MA0X, MA0Y) = 300 pF Generate Refresh Address
ISA Bus Interface Timing: DMA Mode						
tS_DRQ	DRQ to SYSCLK Setup	20		ns	49	External Bus Master Refresh
tD1_DK	SYSCLK to DK2-DK0 Delay	–2	70	ns	49	CL = 50 pF
tD2_DK	CLKIN to DK2-DK0 Invalid Delay	4	16	ns		CL = 50 pF. Local Bus DMA Cycles
tF_DK	SYSCLK to DK2-DK0 Float Delay	–2	70	ns	50	CL = 50 pF. End of DMA Transfer Cycle
tD_DKN	SYSCLK to DKEN Delay	–2	70	ns	49	CL = 50 pF
tD2_CMD	SYSCLK to –CMD Valid Delay	–5	60	ns	49	CL = 200 pF. –CMD refers to signals –IOW, –IOR, –MEMW, –MEMR
tD_A	SYSCLK to A26-A2, –BE3 - –BE0 Valid Delay	0	90	ns	49	CL = 50 pF
tA1_A	SYSCLK to A26-A2, –BE3 - –BE0 Active Delay	0	90	ns	50	CL = 50 pF
tF1_A	SYSCLK to A26-A2, –BE3 - –BE0 Float Delay	0	90	ns	50	CL = 50 pF
tD3_SA	SYSCLK to SA0, SA1 Valid Delay	0	95	ns	49	CL = 200 pF
tD_TC	SYSCLK to TC Delay	–5	60	ns	49	CL = 100 pF
tS3_CHR	IOCHRDY to SYSCLK Setup	45		ns	49	
tH3_CHR	IOCHRDY from SYSCLK Hold	15		ns	49	
tD2_SCD	SYSCLK to –SCMD Delay	–5	60	ns	49	CL = 200 pF. –SCMD refers to signals –SMEMW, –SMEMR
tA2_SCD	–SCMD active from SYSCLK Delay	–5	60	ns	50	CL = 200 pF
tF2_SCD	–SCMD Float from SYSCLK Delay	–5	60	ns	50	CL = 200 pF
Bus Arbitration Timing						
tD1_AEN	–MASTER to AEN Delay	3	35	ns	52	CL = 200 pF
tD2_AEN	HLDA to AEN Delay	3	35	ns	52	CL = 200 pF
tD2_BLE	HLDA to BALE Delay	3	35	ns	52	CL = 200 pF
tA_SAMR	–REFRESH to SA0, SA1, –MEMR, –SMEMR Active Delay	3	30	ns	51	CL = 200 pF Start of External Refresh Cycle
tF_SAMR	–REFRESH to SA0, SA1, –MEMR, –SMEMR Float Delay	3	30	ns	51	CL = 200 pF End of External Refresh Cycle

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

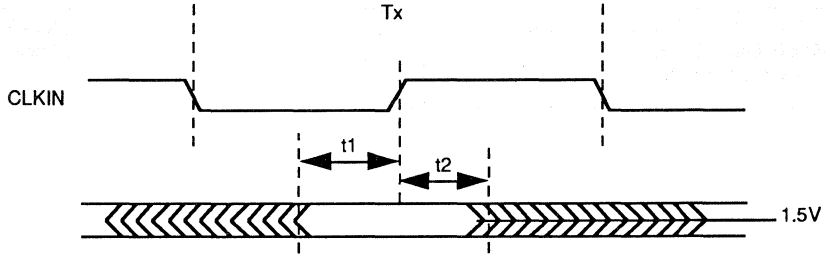
Symbol	Parameter	Min	Max	Unit	Figure	Condition
Bus Arbitration Timing (Cont.)						
tA2_A	–REFRESH to A31, A29, A26-A2, –BE3 - –BE0 Active Delay	3	30	ns	51	CL = 50 pF
tF2_A	–REFRESH to A31, A29, A26-A2, –BE3 - –BE0 Float Delay	3	30	ns	51	CL = 50 pF
tF_SACD	HLDA high to SA1, SA0, –CMD Float Delay	3	30	ns	52	CL = 200 pF
tA_SACD	HLDA high to SA1, SA0, –CMD Active Delay	3	30	ns	52	CL = 200 pF
Interrupt Timing						
tW_IRQ	External Interrupt Request Pulse Width Active	105		ns	52	Glitch-Free Circuit On Includes –FERR, WEIRQ inputs
tD1_IRQ	External IRQ to INTR High Delay	5	130	ns	52	CL = 50 pF. Glitch-Free Circuit On Includes –FERR, WEIRQ inputs
tD2_INT	OSC to INTR High Delay	5	130	ns	53	CL = 50 pF. Glitch-Free Circuit On
tD3_INT	OSC to INTR Delay	3	200	ns	54	CL = 50 pF. When Source is from Internal IRQ0 (timer interrupt)
tS_IRQ	External Interrupt to OSC Setup		15	ns	54	Glitch-Free Circuit On
tS_IRQ	External Interrupt from OSC Hold		10	ns	54	Glitch-Free Circuit On
tD_NMI	–IOCHK to NMI Delay	3	40	ns	53	CL = 50 pF
Miscellaneous Timing						
tW_IOCK	–IOCHK Pulse Width	15		ns	52	CL = 50 pF
tH_PWG	POWERGOOD from OSC Hold	10		ns	53	CL = 50 pF
tD_RSD	CLKIN to RSTDRV Delay	–10	20	ns	49	CL = 200 pF
tD2_SKR	OSC to SPKR Delay	5	120	ns	53	CL = 50 pF
tA_DRM	CLKIN to MA10-MA1, MA0X, MA0Y, –RAS3 - –RAS0, CAS3-CAS0, MBE3-MBE0, –RAMW Active Delay	4	50	ns	48	Following fourth –ADS after Power-on Reset

FIGURE 45. CLOCK WAVEFORMS



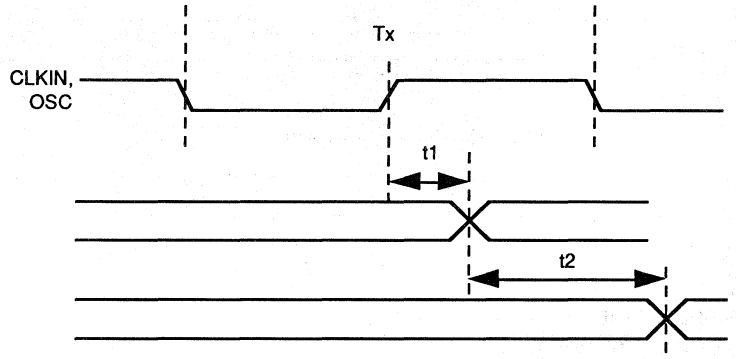
Key:
- t1 = tP_TC2, tP_CLKIN, tP_BOSC, tP_OSC
- t2 = tH_TC2, tH_CLK, tH_CLKIN, tH_BOSC, tH_OSC
- t3 = tL_CLK, tL_BOS, tL_OSC
- t4 = tL_TC2, tL_CLKIN
- t5 = tR_CLK
- t6 = tFA_CLK
- t7 = tR_SCK
- t8 = tFA_SCK

FIGURE 46. AC TIMING: CPU INTERFACE AND DRAM CONTROLLER (1)



Key:
- t1 = tS1_CPU, tS2_CPU, tS3_CPU, tS4_CPU, tS5_CPU, tS6_CPU, tS7_CPU, tS8_CPU
- t2 = tH_CPU

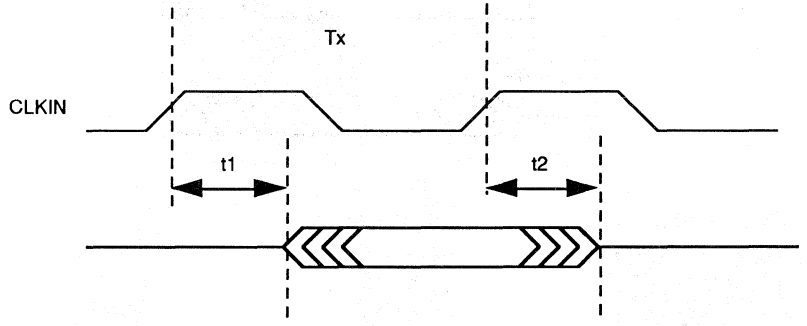
FIGURE 47. AC TIMING: CPU INTERFACE AND DRAM CONTROLLER (2)



Key: t1 = tD1_CPU, tD2_CPU, tD3_CPU, tD_HOLD, tD_RCPU, tD_NMI, tD3_MA, tD1_RAS, tD1_CAS, tD1_MDN, tD2_MDN, tD1_RMW, tD1_MBE, tD2_MBE, tD_RMCS, tD6_MA, tD4_RAS, tD4_CAS

t2 = tD3_CPU, tD1_MA, tD2_MA, tD4_MA, tD3_MBE, tD2_RMW, tD2_RAS, tD3_RAS, tD2_CAS, tD3_CAS, tD_PAR, tD5_MA

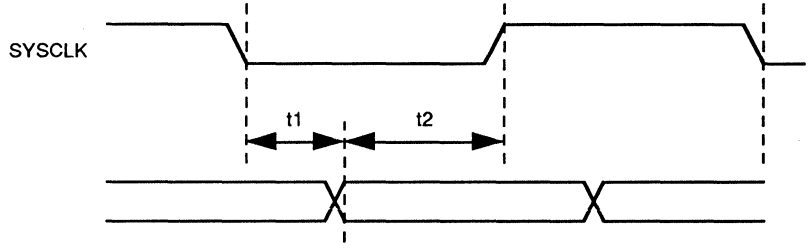
FIGURE 48. AC TIMING: CPU INTERFACE AND DRAM CONTROLLER (3)



Key: t1 = tA2_CPU, tA_DRM, tA1_PAR

t2 = tF1_CPU, tF2_CPU, tF3_CPU, tF1_PAR

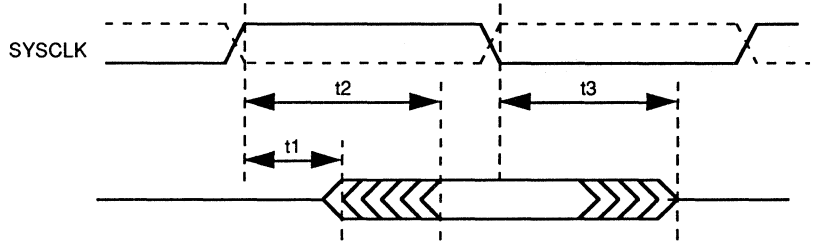
FIGURE 49. AC TIMING: ISA BUS CONTROLLER (1)



Key: t1 = tD_EAL, tD_BAE, tD_CMD, tD_SCMD, tH_CS16, tH_SW0, tH1_CHR, tH_SD, tH2_D, tL_RFSH, tD2_SA, tD_A, tD_MEMR, tH_RFSH, tH2_CHR, tD1_DK, tD_TC, tD_DKN, tD2_CMD, tD_A, tD3_SA, tH3_CHR, tD2_SCD, tH_D, tD_RSD, tD1_SA, tD1_SD

t2 = tS_CS16, tS_WS0, tS1_CHR, tS_D, tS2_D, tS_RFSH, tS2_CHR, tS_DRQ, tS3_CHR

FIGURE 50. AC TIMING: ISA BUS CONTROLLER (2)

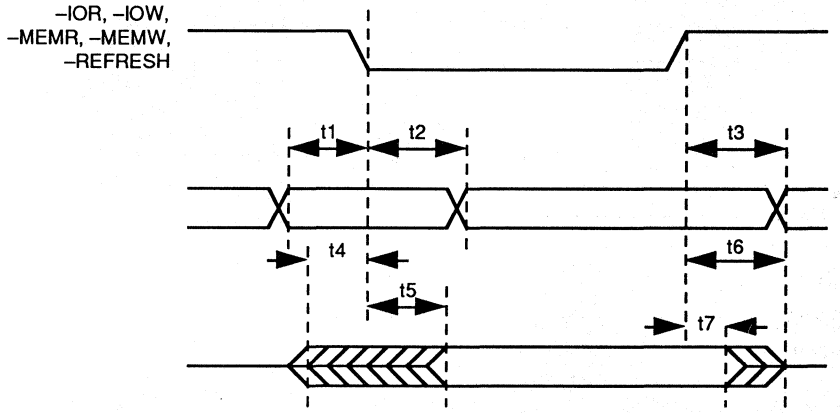


Key: t1 = tA1_A, tA_DRM, tA2_SCD

t2 = tL_RFSH,

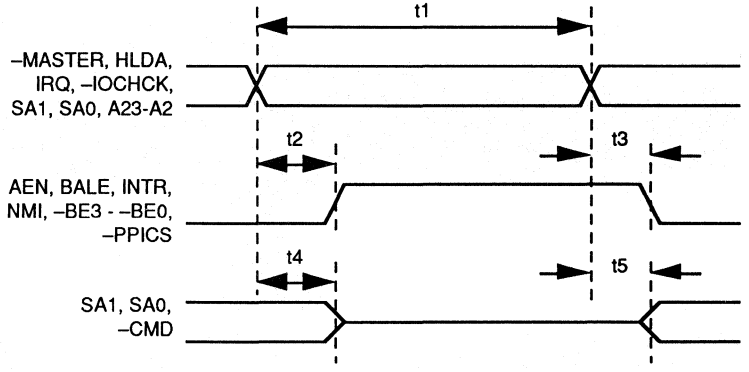
t3 = tF_SCMD, tF1_SD, tF_RFSH, tF_DK, tF1_A, tF2_SCD

FIGURE 51. AC TIMING: ISA BUS CONTROLLER (3)



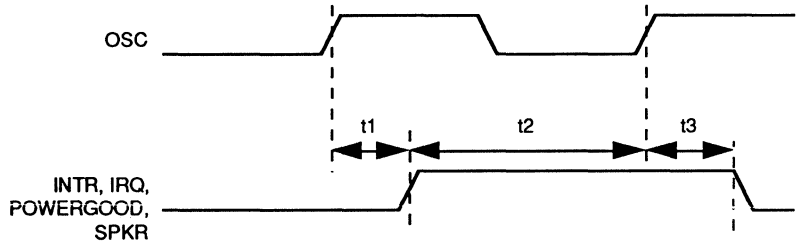
Key:
t1 = tS_IOX, tS_MEMX
t2 = tD_B20, tD_IGNE, tH_MEMX, tD1_SCD
t3 = tD1_SPKR, tH_IOX, tD1_SCD
t4 = tS2_SD, tS_A
t5 = tD3_SD, tA2_SD, tA3_SD, tA_SMR, tA_SAMR, tA2_A
t6 = tF2_SD, tF3_SD, tF4_SD, tF_SMR, tH_A, tF_SAMR, tF2_A
t7 = tH2_SD

FIGURE 52. AC TIMING: ISA BUS CONTROLLER (4)



Key:
t1 = tW_IRQ, tW_IOCK
t2 = tD1_AEN, tD2_AEN, tD2_BLE, tD1_IRQ, tD_NMI, tD_BE, tD2_PPS
t3 = tD1_AEN, tD2_AEN, tD2_BLE, tD_NMI, tD2_PPS
t4 = tF_SACD, tF_SCD
t5 = tA_SACD, tA1_SCD

FIGURE 53. AC TIMING: ISA BUS CONTROLLER (5)



Key: t1 = tD2_INT, tD3_INT, tD2_SPKR
t2 = tS_IRQ, tS_PWG
t3 = tH_IRQ, tH_PWG

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature −10°C to +70°C

Storage Temperature −65°C to +150°C

Supply Voltage to Ground Potential −0.5 V to VDD + 0.3 V

Applied Output Voltage −0.5 V to VDD + 0.3 V

Applied Input Voltage −0.5 V to +7.0 V

Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VIL	Input Low Voltage	−0.5	0.8	V	TTL Level Inputs
VIH	Input High Voltage	2.0	VDD + 0.5	V	TTL Level Inputs
VILC	Input Low Voltage	−0.5	0.8	V	CMOS Level Inputs
VIHC	Input High Voltage	VDD − 0.8	VDD + 0.5	V	CMOS Level Inputs
VOL1	Output Low Voltage		0.45	V	IOL = 4 mA, Note 1
VOH1	Output High Voltage	VDD − 0.45		V	IOH = −1 mA, Note 1
VOL2	Output Low Voltage		0.45	V	IOL = 6 mA, Note 2
VOH2	Output High Voltage	VDD − 0.45		V	IOH = −2 mA, Note 2
VOL3	Output Low Voltage		0.45	V	IOL = 12 mA, BUSCTL[5] = 0 IOL = 24 mA, BUSCTL[5] = 1 Note 3
VOH3	Output High Voltage	VDD − 0.45		V	IOH = −6 mA, Note 3
VOL4	Output Low Voltage		0.45	V	IOL = 24 mA, Note 4
VOL5	Output Low Voltage		0.45	V	IOL = 12 mA, RAMSET[2,1] = 00 IOL = 24 mA, RAMSET[2,1] = 01 IOL = 36 mA, RAMSET[2,1] = 10 IOL = 48 mA, RAMSET[2,1] = 11 Note 5
VOH4	Output High Voltage	2.4		V	IOH = −6 mA, Note 5
VOL6	Output Low Voltage		0.45	V	IOL = 24 mA, Note 6
VOH5	Output High Voltage	2.4		V	IOH = −24 mA, Note 6
VOL7	Output Low Voltage		0.45	V	IOL = 12 mA, RAMSET[2,1] = 00 IOL = 12 mA, RAMSET[2,1] = 01 IOL = 24 mA, RAMSET[2,1] = 10 IOL = 24 mA, RAMSET[2,1] = 11 Note 7
VOH7	Output High Voltage	VDD − 0.45		V	IOH = −6 mA, Note 7
VOL8	Output Low Voltage		0.45	V	IOL= −6 mA, Note 11

(Continued on next page.)

DC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5 V ±5, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
ILI	Input Leakage Current	–10	10	µA	Note 8
IIL	Input Leakage Current	–500	10	µA	Note 9
IIH	Input Leakage Current	–10	500	µA	Note 10
ILO	Output Leakage Current	–100	100	µA	
IDDSB	Static Power Supply Current		500	µA	
IDDOP	Dynamic Power Supply Current		4	mA/MHz	No DC Loads
CI	Input or I/O Capacitance		10	pF	
CO	Output Capacitance		10	pF	

Notes:
1. Pins: HOLD, INTR, NMI, –PPICS, –BLKA20, –ROMCS, –ADS
2. Pins: –BRDY, –RDY, RESCPU, PAR3-PAR0, SPKR, –EALE, A25-A2, –BE3 - –BE0, D31-D0, DKEN, W/–R_DK2, D/–C_DK1, M/–IO_DK0, CAS3-CAS0, –MDENX, –MDENY, MBE3-MBE0
3. Pins: SD15-SD0, SA1, SA0, –IOW, –IOR, –MEMW, –MEMR, RSTDRV, BALE, –SMEMW, –SMEMR, SYSCLK, AEN, TC, –SBHE
4. Pins: –REFRESH
5. Pins: MA10-MA1, –RAMW
6. Pins: CLK
7. Pins: –RAS3 - –RAS0, MA0X, MA0Y
8. All inputs excep those listed in Notes 9 and 10.
9. Pins: IRQ15, IRQ14, IRQ12-IRQ3, IRQ1, DRQ7-DRQ5, DRQ3, DRQ0, –FERR, –BRDY, –RDY, BUSOSC, POWERGOOD, SPKR
10. Pins: WEIRQ
11. Pins: IOCHRDY, –BLAST, A31, A29, A26

BIOS

The VL82C486 is supported by the following BIOS companies.

America Megatrends, Inc. (AMI)
1346 Oakbrook Drive, Suite 120
Norcross, Georgia 30093
(404) 263-8181
In U.S.A. (800) U-BUY-AMI
(404) 263-9381 Facsimile

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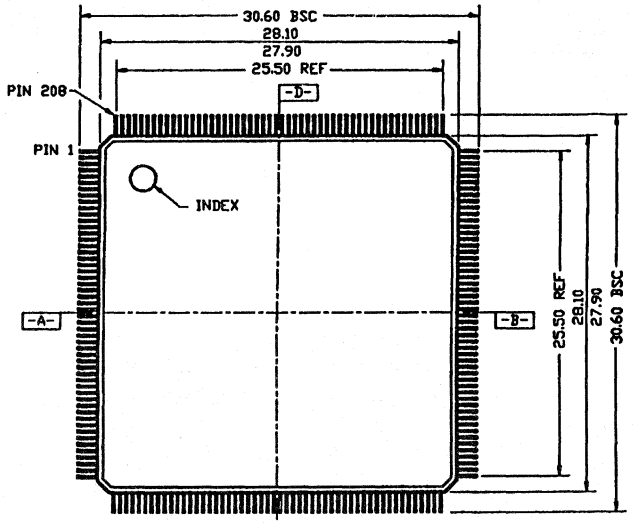
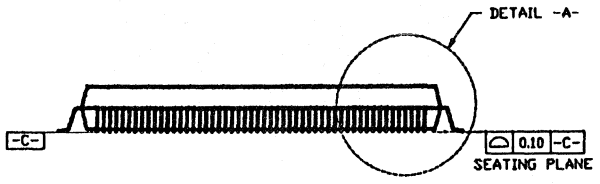
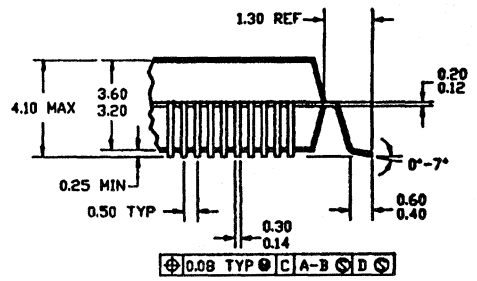
Phoenix Technologies Ltd.
846 University Ave.
Norwood, MA 02062-3950
(617) 551-4000
(617) 551-3750 Facsimile

PACKAGE OUTLINE

208-LEAD METRIC QUAD FLAT PACK (MQFP)







DETAIL -A-

Notes: 1. Dimensions are millimeters.

NOTES

NOTES

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