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1983 Components Handbook

WESTERN DIGITAL
CORPORATION

Western Digital
1983 Components
Handbook

Making The Leading Edge Work For You.

This handbook is designed for you, the design engineer. It's intended to be a useful tool, to enable you to make a preliminary evaluation of our products and, later, with samples in hand, to design our products into your own systems.

The data in these pages have been reviewed by our Marketing, Engineering, Manufacturing and Quality groups. Now we would like you to review the information we've provided and tell us how we can improve it. Please feel free to suggest any changes, additions, or clarifications that occur to you. And don't hesitate to call to our attention any sins of omission or commission we may have made.

We're eager to help upgrade the quality of information our industry provides to its customers. So, please, help us. Direct your comments to:

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Western Digital: Update '83

Western Digital is on the move, growing and expanding to meet your needs. This year's Components Handbook includes a number of significant new products. Our leadership in file management is reinforced by the many innovations this year in both floppy disk and Winchester disk controllers, and the introduction of the first LSI controller for SMD drives. We've expanded our large data communications product line with the addition of a new, ultra fast SDLC controller. And, there are a number of important introductions in our Network, Security and Special Products categories.

That's just half the story, though. This handbook is for our component products only (including board-level solutions based on our LSI disk controllers). Separate handbooks and literature are available for our systems products. We urge you to use order forms at the front of this book to order your copies of the following:

Industrial Automation Handbook: Introduces The WEDGE™, our new 100 module family of Eurocord microcomputer systems based on 8085A/8088/8086 processors and designed for command and control applications in an automated factory environment.

SuperMicro1600 Systems Brochure: Our 16-bit desktop computers, designed to improve programmer efficiency by functioning as low cost, high performance Pascal and Ada development systems, are explained in detail.

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Quality/Reliability To Leading Edge Technology

QUALITY PROGRAM DESCRIPTION

The Quality Organization shown in Figure 2 assures compliance to design control, quality and reliability specifications, pursuant to corporate policy.

CORPORATE QUALITY POLICY

It is the policy of Western Digital Corporation that every employee be committed to quality excellence in producing products/processes which conform to acceptable requirements. The total quality program is managed and monitored by the quality assurance organization. Quality assurance is chartered to review marketing product requirements, qualify hardware and software designs, certify manufacturing operations and monitor performance/control conformance to product specifications.

Primary responsibility for execution for the quality program rests with functional organizations to design, produce and market high quality and high reliability products specified to our customers.

LSI QUALITY ASSURANCE PROGRAM HIGHLIGHTS

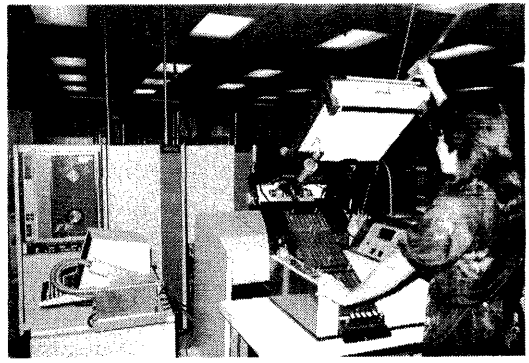
- LSI manufacturing assurance provisions are derived in part from MIL-M-38510 and MIL-STD-883B as applied to high grade commercial components.
- All process raw materials used in the Mask/Wafer fabrication and assembly operations are monitored by Material Assurance.
- Material Assurance maintains a thorough control of incoming material and has developed unique "use/stress tests" (look ahead sample build acceptance) which critical material must pass before acceptance.
- The Product Assurance Department continuously monitors the internal and external manufacturing flow (shown in Figure 1) and issues process control reports displaying detailed data and trends for the associated areas.
  - — Document control is an integral part of Product Assurance. All specifications are issued and controlled by this activity.
  - — The Western Digital Malaysian assembly operation uses specifications and quality control provisions controlled by Document Control. Indicators of Malaysia quality are reviewed weekly.
  - — Purchased FAB and assembly operations are individually qualified and are certified against standard specifications during vendor qualification and monitored against reliability criteria.
  - — Defect control within the process assures the highest levels of built-in reliability.
- Quality audits and gates are located throughout the manufacturing process in order to assure a stable process and thus, a quality product to our customers. Figure 1 illustrates the manufacturing/screening/inspection flow diagram and identifies the steps as they relate to the production of LSI devices.
- Testing assures quality margins through 100% testing by manufacturing and, in addition, all products must pass a specified AQL sample test performed by QA at maximum operating temperature as follows:

Outgoing Quality Levels

SUBGROUPS	INSPECTION LEVEL
Subgroup 1 — Final 100% Electrical Audit @ Max °C	0.5 AQL*
Subgroup 2 — Visual (Marking, Lead Integrity, Package, Verify customer shipper)	1.0 AQL
Subgroup 3 — Shipping Visual Audit	1.0 AQL

*The double sampling techniques used allow considerably better AQL's in most all cases.

- LSI devices are 100% tested on industry standard test systems like that shown below. Quality outgoing testing (auditing) is done on the Fairchild Sentry Series 20 where possible to allow better correlation with customers.



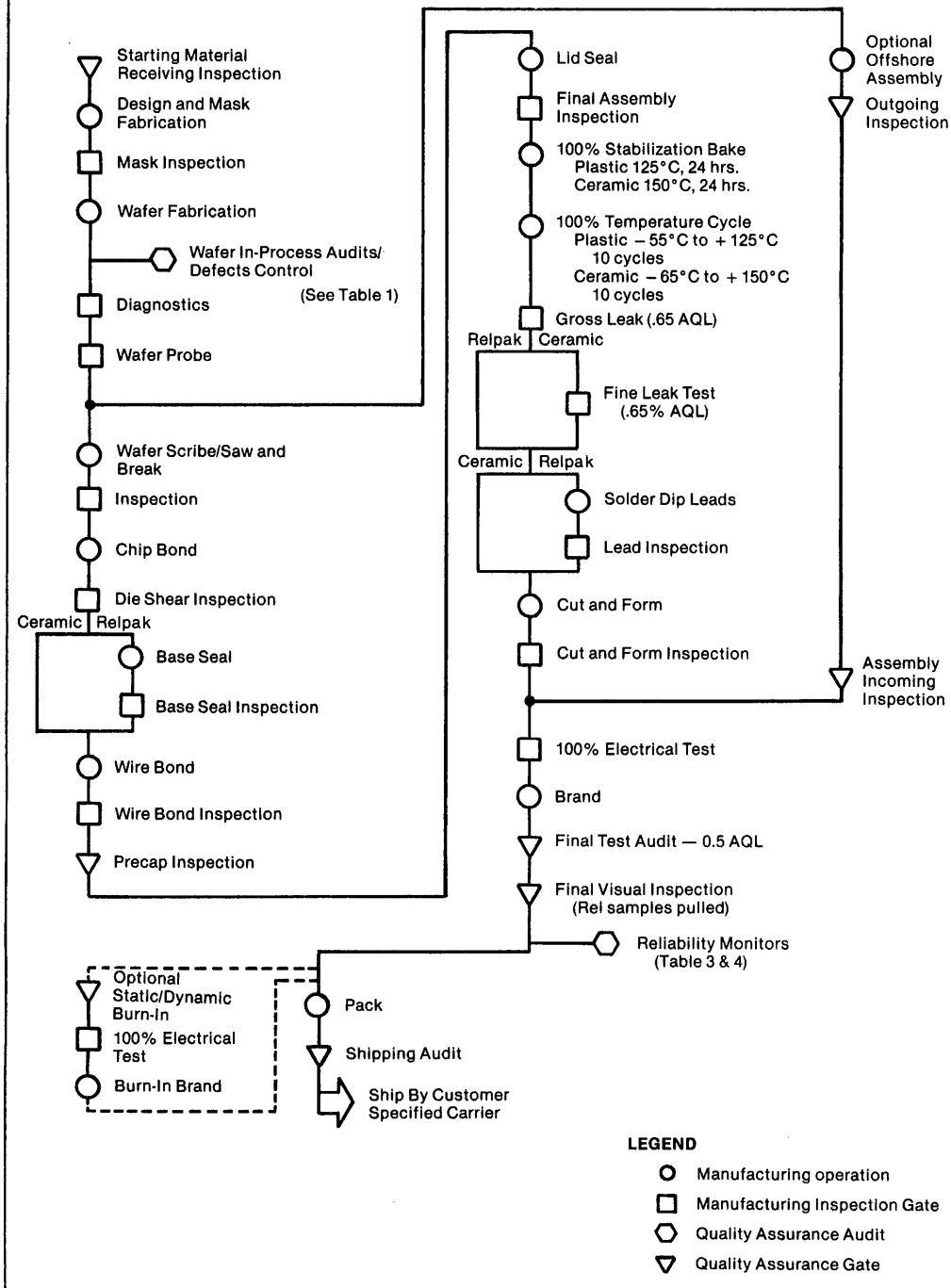


Figure 1 LSI PRODUCTION FLOW

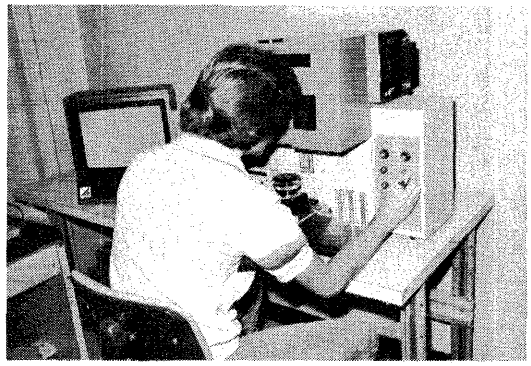
Reliability Means Lasting Value

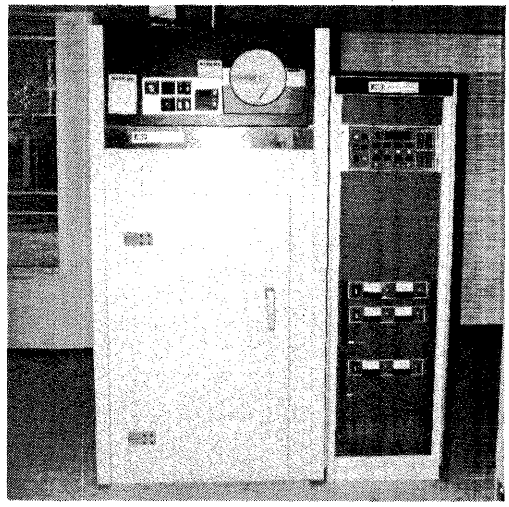
• DESIGNING FOR RELIABILITY

The production release procedure for an LSI device is designed to assure maximum reliability with a Quality checklist for:

- Test program qualifications
- Characterization report
- Field test (Beta Test) report
- Reliability Lifetest Qualifications
- Infrared Thermal Analysis
- Static Protection

All new devices and major process changes must pass reliability qualification before incorporation into production using the criteria defined in Tables 2-4. The infrared microscope shown on the right assures optimum burn-in temperatures and margins of safety. The dynamic burn-in system shown on the right is one of two custom designed systems which assure protective device isolation during burn-in.





• MAINTAINING RELIABILITY IN PRODUCTION

Process defects control are defined to continually measure built-in reliability, as measured by the following criteria:

TABLE 1

PROCESS RELIABILITY CONTROL	METHOD	CONDITION	SAMPLE*
Subgroup 1 — Defects Control			
a. Oxide Integrity	Non-destructive bubble test	Pinhole defect density	5 wafers
b. Polysilicon Integrity	SEM Analysis	Visual	5 wafers
Subgroup 2 — Electro-Migration Control			
Metal Step Coverage	MIL-STD-883 Method 2018	SEM Analysis	5 wafers
Subgroup 3 — Defect Density	Critical layers Field Gate Contact Metal	Visual of Photo defects (Defects/in^2)	8 wafers each layer
Subgroup 4 — Passivation/Insulation Integrity	MIL-STD-883 Method 2021	Visual of Pinhole defect density	Final Silox 5 wafers Intermediate 5 wafers

*Inspection intervals are defined by the in-line process control data reviewed on a lot-by-lot basis.

• PROGRAMS TO ASSURE OPTIMUM RELIABILITY

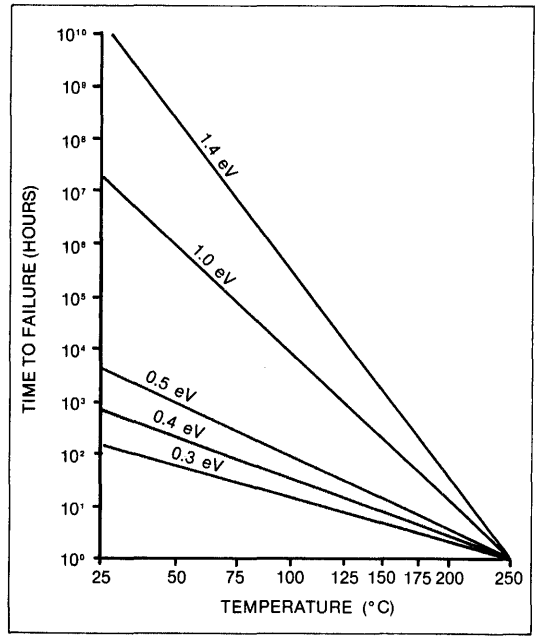
Improved levels of reliability are available under custom reliability programs using static and dynamic burn-in to further improve reliability. These programs focus on MOS failure mechanisms as follows:

FAILURE MECHANISMS IN MOS

FAILURE MECHANISM	EFFECT ON DEVICE	ESTIMATED ACTIVATION ENERGY	SCREENING METHOD
Slow Trapping	Wearout	1.0 eV	Static Burn-In
Contamination	Wearout/ Infant	1.4 eV	Static Burn-In
Surface Charge	Wearout	0.5-1.0 eV	Static Burn-In
Polarization	Wearout	1.0 eV	Static Burn-In
Electromigration	Wearout	1.0 eV	Dynamic Burn-In
Microcracks	Random	—	100% Temp. Cycling
Contacts	Wearout/ Infant	—	Dynamic Burn-In
Oxide Defects	Infant/ Random	0.3 eV	Dynamic Burn-In at max. voltage
Electron Injection	Wearout	—	Low Temp. Voltage Operating Life

Temperature Acceleration of Failure

The Arrhenius Plot defines a failure rate proportional to exp(– Ea/kt) where Ea is the activation energy for the failure mechanism. The figure on the right indicates that lower activation energy failures are **not** effectively accelerated by temperature alone; hense, maximum voltage operation is selectively applied to optimize the burn-in process.



Static Burn-In (125°C — 48 hours or 160 hours)

Provided on a sample basis for process monitor/control of 0.5 eV — 1.0 eV failure mechanisms. 100% static burn-in may be specified at an additional cost. However, static burn-in is considered only partially effective for internal LSI gates at logic "O" levels.

Dynamic Burn-In (Pattern test/125°C — 8 hours to 160 hours)

Accelerated functional dynamic operating life effectively controls internal MOS gate defects buried from external pin access. The input pattern is optionally pseudo-random or fixed pattern programmable to simulate 1000-3000 hours of field operation at maximum operating voltage(s).

High-Rel "K" Testing Program

General conformance to MIL-STD-883B method 5004.4, Class B with static Burn-In (Dynamic Burn-In may be specified as an option).

LSI RELIABILITY STANDARDS

TABLE 2 STANDARD RELIABILITY LEVELS

TEST	METHOD	CONDITION	FAILURE
Infant Mortality (see note)	Static Burn-In	125°C — 160 hrs.	<0.5%
Long Term Failure Rate	Dynamic Life Test	125°C — 1000 hrs.	<.05%/1000 hrs. @ 55°C 60% Confidence

*NOTE: Devices failing the infant mortality target remain on burn-in until acceptable failure rates are obtained.

TABLE 3 GROUP A DEVICE RELIABILITY MONITORS

TEST	METHOD	CONDITIONS	LTPD
Subgroup 1			
a. Internal Visual			15
b. Thermal Shock	1011	Test Failure Used (cond. B or C)	
c. Bond Strength	2011	Test Failures (cond. B)	
d. Die Shear Strength	2019	Test Failures	
Subgroup 2			
a. Seal — Gross Leak		Fluorocarbon detection 10^{-3} atm/cc/sec	15
b. Seal — Fine Leak	1014	Test Condition A	
Subgroup 3			
a. Rotating Steady State Life Test	1005	Static 160 hr. Burn-In 125°C plus 125°C Lifetest — 1000 hrs.	5
b. Electrical Parameters	—	Final electrical @ 25°C (with data @ 70°C)	

TABLE 4 GROUP B PACKAGE RELIABILITY MONITORS

TEST	METHOD	CONDITIONS	LTPD
Subgroup 1			
a. Thermal Shock	1011	Test Condition B or C	15
b. Temperature Cycling	1010	Test Condition B or C	
c. Seal — Gross Leak	—	Fluorocarbon detection 10^{-3} atm/cc/sec	
d. Seal — Fine Leak (ceramic)	1014	Test Condition A	
e. Electrical Parameters	—	Electrical at max -C	
f. 85/85 Moisture Resistance (plastic only)	—	85% RH/85°C for 1000 hours PDA = 10%	
g. Electrical Parameters	—	Final electrical @ 25°C	
Subgroup 2			
a. High Temp. Storage	1008	Test Condition B or C	
b. Mechanical Shock	2002	Test Condition B	15
c. Seal — Gross Leak	—	Fluorocarbon detection 10^{-3} atm/cc/sec	
d. Seal — Fine Leak (ceramic)	1014	Test Condition A	
e. Electrical Parameters	—	Final electrical @ 25°C/max. C	
Subgroup 3			
a. Lead Integrity	2004	Test Condition B2 (Lead Fatigue)	15
b. Seal — Gross Leak	—	Fluorocarbon detection 10^{-3} atm/cc/sec	
c. Seal — Fine Leak (ceramic)	1014	Test Condition A	

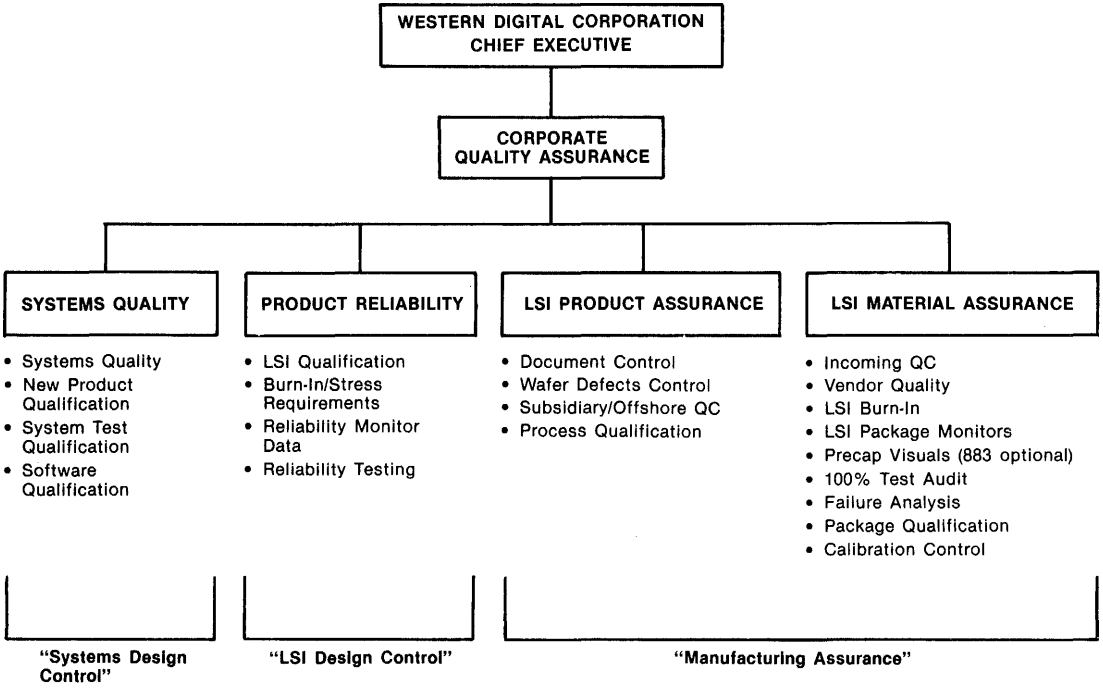


Figure 2 QUALITY ORGANIZATION

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Announcing Burn-In Program Availability/Warranties

Western Digital now supports customer burn-in requirements for both static and dynamic burn-in under the strict control of the QA-Reliability organization.

This burn-in provides high performance 125°C static and dynamic burn-in for 8-160 hours to eliminate infant mortality and improve reliability. This process is executed using custom modified 32Bit AEHR test commercial burn-in equipment which provide monitored fixed pattern or pseudorandom burn-in with power supply and resistor device pin isolation.

LSI dynamic burn-in is verified in all cases by the design engineer for proper functioning. LSI Chip sets are also individually burned-in with dynamic equivalency to assure high performance bundled reliability.

The warranty on the program will optionally provide certificate of compliance to standard or custom designed burn-in programs and guarantee <.05%/Khrs failure rate.

CAUTION

Using outside burn-in methods not certified as acceptable by Western Digital may result in voided warranty, due to mishandling, junction temperature stress, or electrical damage. Further, since most burn-in houses do not support testing, catastrophic system condition can result in substantial damage before a problem is identified.

One consistent problem experienced with outside LSI burn-in houses can cause reliability problems; namely, parallelling totem pole MOS outputs, where the output states are not predictable, can cause a single (or a few) device(s) to sink all the current from the other devices on the burn-in tray — electromigration or current zaps are both possible.

Western Digital burn-in diagrams, dated after 1/1/82, must be used exactly as shown and will be provided upon request.

SEE YOUR LOCAL REPRESENTATIVE FOR COSTS AND ORDERING INFORMATION ON THIS NEW PROGRAM.

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Hi-Rel "K" Testing Program

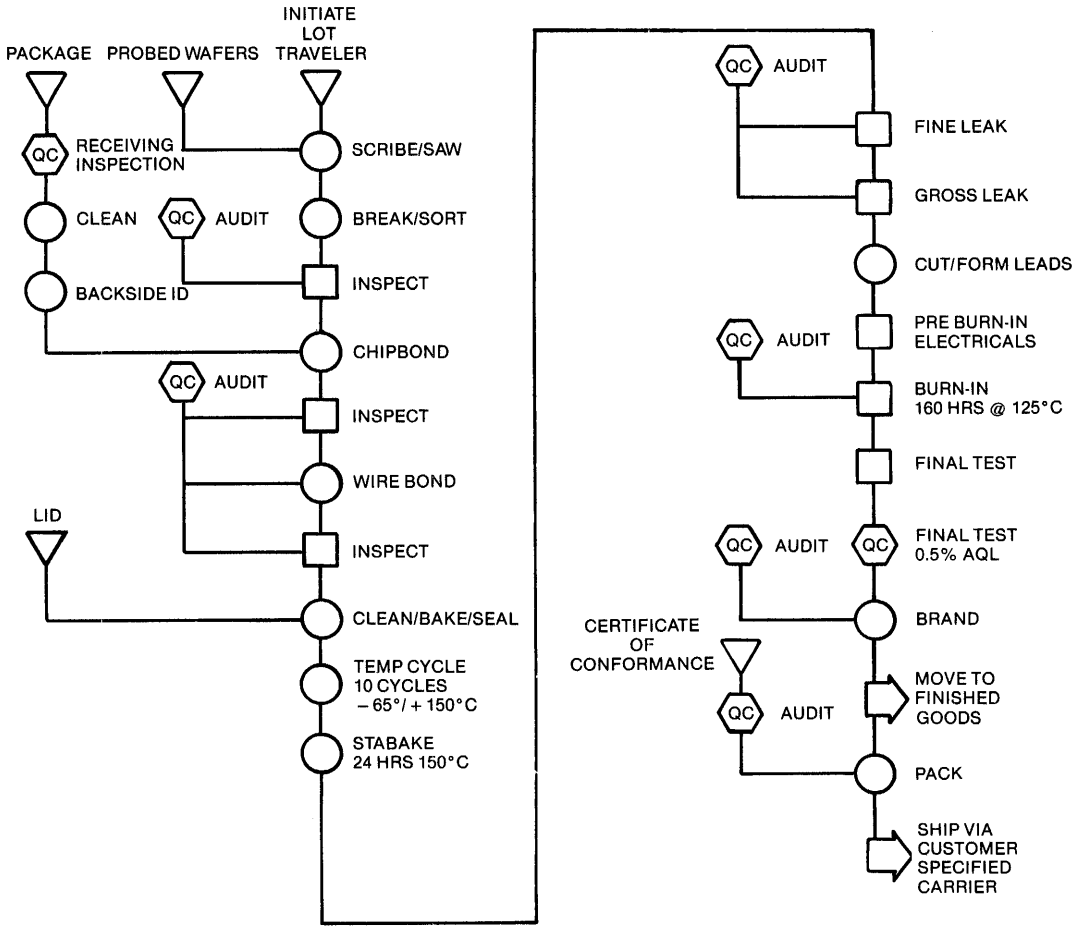
FEATURES

GENERAL CONFORMANCE TO MIL-STD-883B, METHOD 5004.4, CLASS B (SEE COMPARISON ON FOLLOWING PAGES)

- INCLUDES:
  - PRECAP VISUALS
  - SEAL INTEGRITY
  - POWER CONDITIONING
  - ENHANCEMENT OPTIONS

GENERAL DESCRIPTION

Western Digital's Hi-Rel "K" program is designed to provide high reliability devices for extended temperature environments. Individual enhancements may be specified to meet a customer's requirements.



HI-REL "K" PROGRAM FLOW DIAGRAM

COMPARISON OF MIL-STD-883 AND HI-REL "K" TEST PROGRAM

MIL-STD-883B, METHOD 5004.4, CLASS B	HI-REL "K" TEST
3.1.1 Internal Visual Method 2010.3 Test condition B	All Hi-Rel "K" devices receive 100% inspections prior to lid seal. These inspections together comprise criteria comparable to Mil-Std-883, method 2010.3, test condition B.
3.1.2 Stabilization Bake Method 1008.1 Test condition C 24 hours at 150°C	Same
3.1.3 Temperature Cycling Method 1010.2, Test condition C −65°C to 150°C for 10 cycles, with 10 minutes dwell and 5 minutes maximum transfer time	Same
3.1.4 Constant Acceleration Method 2001.2, Test condition E. 30,000 G stress level	Not Done Unless Specified
3.1.5 Visual Inspection Visual inspection for catastrophic failures after screens	Same
3.1.6 Seal Method 1014.2 (a) Helium fine leak — Test condition A_1. Bomb condition 2 hours at 60 psig. Reject limit 5×10^{-8} torr	Same
(b) Flourocarbon gross leak — Test condition C	Same
3.1.9 Interim (pre-burn-in) Electricals Per applicable device specification	Preburn-in test at 25°C. Must meet requirements of device data sheets.
3.1.10 Burn-in Test Method 1015.2 160 hours @ 125°C	Same
3.1.13 Interim (Post burn-in) electricals Per applicable device specification	Burn-in equipment isolate failures automatically to assure no harmful interaction.
3.1.15 Final Electrical Test (a) Static Tests (1) 25°C (2) Minimum and Maximum Operating Temperatures (b) Dynamic and Switching Tests at 25°C (c) Functional Tests at 25°C	Same
3.1.17 Qualification or Quality Conformance Inspection and Test Sample Selection	Not done unless defined using method 5005 as a guide.
3.1.18 External Visual Method 2009.2	Same

WESTERN DIGITAL RELIABILITY ENHANCEMENT OPTIONS

100% Temperature Testing

Level . . . . . −40° to +85°C
. . . . . −55° to +125°C

Thermal, Shock (Liquid to Liquid)

Level. . . . . 0° to +100°C, 15 cycles
. . . . . −55° to +125°C
. . . . . −65° to +150°C

Extended High Temperature Storage

+150°C for 24 hours standard, other time/temperature storage requirements available as required.

Dynamic Burn-In

Per note previously supplied.

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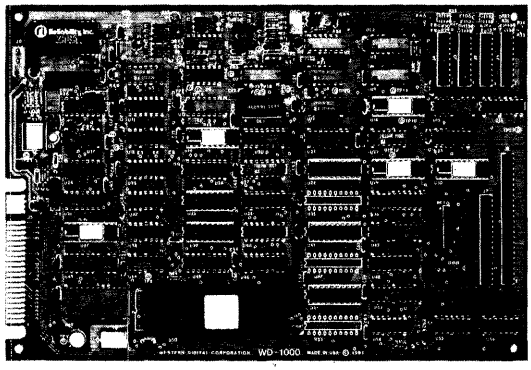
File Management Products

WD1000 Winchester Disk Controller



FEATURES

- BUILT-IN DATA SEPARATOR
- BUILT-IN WRITE PRECOMPENSATION LOGIC
- DATA RATES UP TO 5 MBITS/SEC
- CONTROL FOR UP TO 4 DRIVES
- CONTROL FOR UP TO 8 R/W HEADS
- 1024 CYLINDER ADDRESSING RANGE
- 256 SECTOR ADDRESSING RANGE
- CRC GENERATION/VERIFICATION
- AUTOMATIC FORMATTING
- 128, 256, OR 512 BYTES PER SECTOR (ROM SELECTABLE)
- UNLIMITED SECTOR INTERLEAVE CAPABILITY
- OVERLAP SEEK CAPABILITY
- IMPLIED SEEK ON ALL COMMANDS
- AUTOMATIC RETRIES ON ALL ERRORS
- AUTOMATIC RESTORE AND RE-SEEK ON SEEK ERROR
- 8-BIT HOST INTERFACE
- 0°C to 50°C OPERATION

GENERAL DESCRIPTION

The WD 1000 is a stand-alone, general purpose Winchester controller board designed to interface up to four Winchester disk drives to a host processor. The drive signals are based upon the floppy look-alike interface available on the Shugart Associates' SA 1000, the Seagate Technology ST506, the Quantum Q2000, and other compatible drives. All necessary buffers and receivers/drivers are included on the board to allow direct connection to the drive. Either a 34 pin (5¼" drive) or 50 pin (8" drive) connector is provided, as well as four 20 pin data connectors.

Communications to and from the host computer are made via a separate computer access port. This port consists mainly of an 8 bit bi-directional bus and appropriate control signals. All data to be written to or read from the disk, status information, and macro cammands are transferred via this 8 bit bus. An on board sector buffer allows data transfers to the host computer independent of the actual data transfer rate of the drive.

The WD1000 is based upon a proprietary chip set, the WD1100, specifically designed for Winchester Control.

ORGANIZATION

The WD1000 has seven on board connectors. These connectors consist of a power connector, host interface connector, drive control connector, and four high speed data cable connectors.

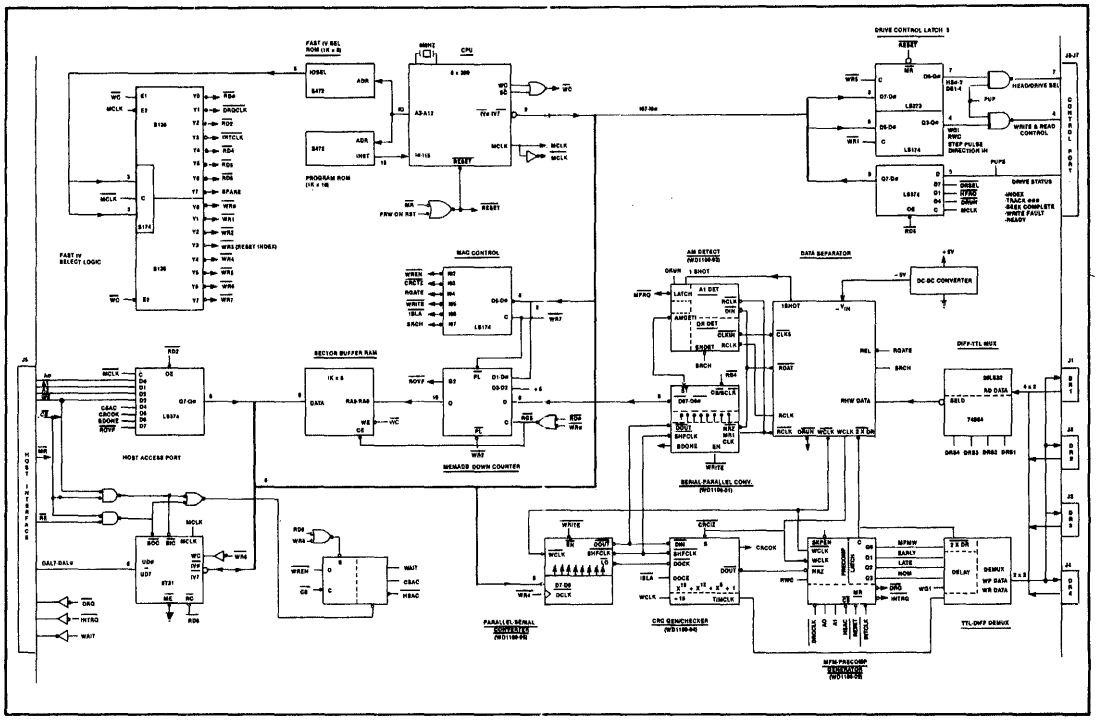
The drive control cable is daisy-chained to each of the four drives. Although there is space for two drive control connectors, only one would normally be used for any particular configuration.

The drive data connectors carry differential signals and are radially connected. Up to four drives can be accommodated by the WD1000.

The host interface connector provides interface signals that are compatible with most microprocessors and minicomputers.

WD1100

For those who want to design their own board around the WD1100 chip set, Western Digital can provide schematics, artwork, and programming information. Western Digital also has a complete staff of Applications Engineers to provide additional support. For further information please contact your local representative, or our main plant listed on page 8.



WD1000 BLOCK DIAGRAM

SPECIFICATIONS

Encoding method:	MFM
Cylinders per Head:	Up to 1024
Sectors per Track:	Up to 256 (512 byte sec)
Heads:	8
Drive Selects:	4
Step rate:	10 uS to 7.5 mS (0.5 mS increments)
Data Transfer Rate:	4.34 Mbits/sec or 5.000 Mbits/sec
Write Precomp Time:	10 nanoseconds
Sectoring:	Soft
Host Interface:	8 Bit bi-directional bus
Drive Capability:	10 "LS" Loads
Drive Cable Length:	10 ft. (3 M) max.
Host Cable Length:	3 ft. (1 M) max.
Power Requirements:	+5V ±5%, 3.0A Max. (2.5A typ.) −8 to −18V, 50 mA*
Ambient Temperature Operating:	0°C to 50°C (32 F to 122 F)
Relative Humidity:	20% to 80%
MTBF:	10,000 POH
MTTR:	30 minutes
Length:	9.9 in. (24.9 cm)
Width:	6.8 in. (17.1 cm)
Height:	0.75 in. (1.9 cm)
Mounting Centers:	6.375 x 9.375 in. (16 x 23.6 cm)

* Optional −V Supply Available.

HOST INTERFACING

The WD1000 is designed to easily interface to most micro computers and mini-computers. All interfacing is done through the Host Interface Connector (J5). The interface is very similar to Western Digital's family of Floppy Disk Controllers. The only exception is the inclusion of the $\overline{\text{WAIT}}$ line.

Waits

The $\overline{\text{WAIT}}$ control line goes true whenever either of the following are true:

- The WD1000 is accessing data internally to send to the host during a read operation
- The WD1000 has not accepted the data from the host during a write operation.

The definition of the $\overline{\text{WAIT}}$ line is very similar to the $\overline{\text{WAIT}}$ signal found on many popular processors. $\overline{\text{WAIT}}$ is also similar to the REPLY signal on Western Digital and other processors.

$\overline{\text{WAIT}}$ will not necessarily make a transition for each access to the WD1000. When the WD1000 can return the requested data within 100 nS, there will be no transition of the $\overline{\text{WAIT}}$ line. This should be interpreted as an instant REPLY on Western Digital Processors.

If the WD1000 cannot return the requested data within 100 nS, it will assert its $\overline{WAIT}$ line. The period of the $\overline{WAIT}$ signal will vary from 750 nS to 6 uS with 1.25 uS being about average. The period of the $\overline{WAIT}$ only approaches 6 uS during a read or write which happens immediately after a command is written to the command register. This means that longer waits may be encountered during the first read or write to any WD1000 register if that first read or write happens within approximately 6 uS of a command being issued.

During the time that $\overline{WAIT}$ is asserted, the host system **must** hold all of its strobe and address lines stable. On write operations, the DAL lines must also be held stable.

The user can modify the timing of the wait signal by selecting a jumper. The WD1000 is shipped with a jumper (or trace) between E4 and E5. This enables waits as soon as the $\overline{CS}$ signal is asserted. This timing is a requirement for some processors and compatible with most. If the host system requires the $\overline{WAIT}$ signal to be asserted only when $\overline{RE}$ or $\overline{WE}$ are asserted in conjunction with $\overline{CS}$, the trace at E4 and E5 should be cut and a jumper should be installed between E4 and E3.

The Host Interface connector (J5) consists of an eight bit bi-directional bus, three bit address bus, and seven control lines. All commands, status, and data are transferred over this bus. See Table 1:

HOST INTERFACE CONNECTOR **TABLE 1**

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME	DESCRIPTION
2 4 6 8 10 12 14 16	1 3 5 7 9 11 13 15	DAL0 DAL1 DAL2 DAL3 DAL3 DAL5 DAL6 DAL7	8 bit bi-directional Data Access Lines. These lines remain in a high-impedance state whenever the $\overline{CS}$ line is inactive.
18 20 22	17 19 21	A0 A1 A2	These three Address Lines are used to select one of eight registers in the Task File. They must remain stable during all read and write operations.
24	23	$\overline{CS}$	When $\overline{Card\ Select}$ is active along with $\overline{RE}$ or $\overline{WE}$, Data is read or written via the DAL bus. $\overline{CS}$ must make a transition for each byte read from or written to the task file.
26	25	$\overline{WE}$	When Write Enable is active along with $\overline{CS}$, the host may write data to a selected register of the WD1000.
28	27	$\overline{RE}$	When $\overline{Read\ Enable}$ is active along with $\overline{CS}$, the host may read data from a selected register of the WD1000.
30	29	$\overline{WAIT}$	Upon receipt of a $\overline{CS}$, the $\overline{WAIT}$ line may go active. It returns to the inactive state when the DAL lines are valid on a read, or data has been accepted on a write.
32	31	Not Connected	
34	33	−V	Optional −V input from host supplies −8 to −15V to the on-board −5 Volt regulaton (VRI). This power input is also available on J6, pin 2. −V is not required if DC/DC convertor (PSI) is used.
36	35	INTRQ	The INTerrupt ReQuest Line is activated whenever a command has been completed. It is reset to the inactive state when the Status Register is read, or a new command is loaded via the DAL lines.

HOST INTERFACE CONNECTOR (Continued)

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME	DESCRIPTION
38	37	DRQ	The Data ReQuest line is activated whenever the sector buffer contains data to be read by the host, or is awaiting data to be loaded by the host. This line is reset whenever the Data Register is read from or written to. The DRQ line will continue to toggle until the buffer is exausted or until a write or read is performed on the Cylinder Low register.
40	39	$\overline{MR}$	The Master Reset line initializes all internal logic on the logic on the WD1000. Sector Number, Cylinder Number and SDH are cleared, stepping rate is set to 7.5 mS, Write Precomp is set to cylinder 128 and Sector Count is set to 1. The DRQ line is reset and the INTRQ line is set.
	41 42	Not Connected Not Connected	
	43-50		+5V 8 power pins for regulated +5 volts. This power input is also available on J6, pin 3.
Note: Grounds			Even numbered pins (2-40) are to be used as signal grounds. Power ground is available on J6, pin 1.

DRIVE CONTROL CONNECTORS

The drive control connector is a (relatively) low speed bus that is daisy chain connected to each of the drives (up to four) in the system. To properly terminate each TTL level output signal from the WD1000, the last drive in the daisy chain should have a 220/330 ohm line termination resistor pack installed. All other drives should have no termination. See Tables 2 and 3:

34 PIN DRIVE CONTROL CONNECTOR **TABLE 2**

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2	O	$\overline{RWC}$
3	4	O	$\overline{Head\ Select\ 2}$
5	6	O	$\overline{Write\ Gate}$
7	8	I	$\overline{Seek\ Complete}$
9	10	I	$\overline{TR000}$
11	12	I	$\overline{Write\ Fault}$
13	14	O	$\overline{Head\ Select\ 0}$
15	16		NC
17	18	O	$\overline{Head\ Select\ 1}$
19	20	I	$\overline{Index}$
21	22	I	$\overline{Ready}$
23	24	O	$\overline{Step}$
25	26	O	$\overline{Drive\ Select\ 1}$
27	28	O	$\overline{Drive\ Select\ 2}$
29	30	O	$\overline{Drive\ Select\ 3}$
31	32	O	$\overline{Drive\ Select\ 4}$
33	34	O	$\overline{Direction\ In}$

50 PIN DRIVE CONTROL CONNECTOR FOR SA1000 TYPE INTERFACE **TABLE 3**

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2	O	$\overline{RWC}$
3	4	O	$\overline{Head\ Select\ 2}$
5	6		NC
7	8	I	$\overline{Seek\ Complete}$
9	10		NC
11	12		NC
13	14	O	$\overline{Head\ Select\ 0}$
15	16		NC
17	18	O	$\overline{Head\ Select\ 1}$
19	20	I	$\overline{Index}$
21	22	I	$\overline{Ready}$
23	24		NC
25	26	O	$\overline{Drive\ Select\ 1}$
27	28	O	$\overline{Drive\ Select\ 2}$
29	30	O	$\overline{Drive\ Select\ 3}$
31	32	O	$\overline{Drive\ Select\ 4}$
33	34	O	$\overline{Direction\ In}$
35	36	O	$\overline{Step}$
37	38		NC
39	40	O	$\overline{Write\ Gate}$
41	42	I	$\overline{TR000}$
43	44	I	$\overline{Write\ Fault}$
45	46		NC
47	48		NC
49	50		NC

DRIVE CONTROL SIGNAL DESCRIPTIONS

$\overline{\text{RWC}}$

When the Reduce Write Current line is activated with write gate, a lower write current is used to compensate for greater bit packing density on the inner cylinders. The RWC line is activated when the cylinder number is greater than or equal to four times the contents of the Write Precomp Register. This output is valid only during Write and Format commands.

$\overline{\text{Write Gate}}$

This output signal allows data to be written on the disk.

$\overline{\text{Seek Complete}}$

Informs the WD1000 that the head of the selected drive has reached the desired cylinder and has stabilized. Seek Complete is not checked after a SEEK command, thus allowing overlapped seeks.

$\overline{\text{Track 000}}$

Indicates that the R/W heads are positioned on the outermost cylinder. This line is sampled immediately before each step is issued.

$\overline{\text{Write Fault}}$

Informs the WD1000 that some fault has occurred on the selected drive. The WD1000 will not execute commands when this signal is true.

$\overline{\text{HS0}}$ $\overline{\text{HS2}}$

Head Select lines are used by the WD1000 to select a specific R/W head on the selected drive.

$\overline{\text{Index}}$

Is used to indicate the index point for synchronization during formatting and as a time out mechanism for retries. This signal should pulse once each rotation of the disk.

$\overline{\text{Ready}}$

Informs the WD1000 that the desired drive is selected and that its motor is up to speed. The WD1000 will not execute commands unless this line is true.

$\overline{\text{Step}}$

This line is pulsed once for each cylinder to be stepped. The direction of the step will be determined by the DIRECTION line. The step pulse period is determined by the internal stepping rate register during implied seek operations or explicitly during Seek and Restore commands. During auto restore, the step pulse period is determined by the $\overline{\text{SEEK COMPLETE}}$ time from the drive.

$\overline{\text{Direction In}}$

Determines the direction of motion of the R/W head when the step line is pulsed. A high on this line defines the direction as out and a low defines direction as in.

$\overline{\text{DS1}}$ $\overline{\text{DS4}}$

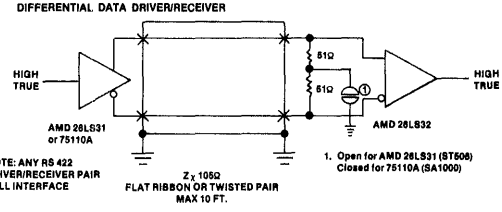
These four Drive Select lines are used to select one of four possible drives.

DRIVE DATA CONNECTOR

Four data connectors (J1-4) are provided for clock signals and data between the WD1000 and each drive. All lines associated with the transfer of data between the drive and the WD1000 system are differential in nature and may not be multiplexed. The data connectors are 20 pin vertical headers on tenth-inch centers that mate with Burndy #FRS20BS. The cable used should be flat ribbon cable or twisted pair with a length of less than 10 feet. The cable pin-outs are per Table 4:

DATA CONNECTIONS AND DESCRIPTIONS TABLE 4

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
2	1	I	– Drive Selected
4	3		NC
6	5		NC
8	7		NC
	9	O	+ Timing Clock
	10	O	– Timing Clock
11			GND
12			GND
	13	O	+ MFM Write Data
	14	O	– MFM Write Data
15			GND
16			GND
	17	I	+ MFM READ DATA
	18	I	– MFM READ DATA
19			GND
20			GND



POWER CONNECTOR

A three pin molex connector (J6) is provided for power input to the board. The customer supplied mating connector housing is Molex 03-09-1032. The pin-outs are as shown in Table 5:

TABLE 5

PIN	SIGNAL NAME
1	GROUND
2	– 8 to – 15 V unregulated
3	+ 5 V regulated

COMMANDS

The WD1000 executes five easy to use macro commands. Most commands feature automatic 'implied' seek, which means the host system need not tell the WD1000 where the R/W heads of each drive are or when to move them. The controller automatically performs all needed retries on all errors encountered including data CRC errors. If the R/W head mis-positions, the WD1000 will automatically perform a restore and a re-seek. If the error is completely unrecoverable, the WD1000 will simulate a normal completion to simplify the host system's software.

Commands are executed by loading the command byte into the Command Register while the controller is not busy. (Controller will not be busy if it has completed the previous command.) The task file must be loaded prior to issuing a command. No command will execute if the Seek Complete or Ready lines are false or if the Write Fault line is true. Normally it is not necessary to poll these signals before issuing a command. If the WD1000 receives a command that is not defined in the following table, undefined results will occur.

For ease of discussion, commands are divided into three types which are summarized in Table 6:

TABLE 6

TYPE	COMMAND	BITS 7	6	5	4	3	2	1	0
I	Restore	0	0	0	1	r_3	r_2	r_1	r_0
I	Seek	0	1	1	1	r_3	r_2	r_1	r_0
II	Read Sector	0	0	1	0	D	0	0	0
III	Write Sector	0	0	1	1	0	0	0	0
III	Format Track	0	1	0	1	0	0	0	0

r_3-r_0 — STEPPING RATE

0000 = 10uS	1000 = 4.0mS
0001 = 0.5mS	1001 = 4.5mS
0010 = 1.0mS	1010 = 5.0mS
0011 = 1.5mS	1011 = 5.5mS
0100 = 2.0mS	1100 = 6.0mS
0101 = 2.5mS	1101 = 6.5mS
0110 = 3.0mS	1110 = 7.0mS
0111 = 3.5mS	1111 = 7.5mS

D = DMA Read Mode

0 = Programmed I/O Mode
1 = DMA Mode

NOTE:

The DMA bit is used to position INTRQ in relation to DRQs during the read sector command. If the DMA bit is reset (D = 0), the interrupt will occur before the first DRQ. This allows the programmed I/O host to intervene and transfer the data from the sector buffer. If the DMA bit is set (D = 1), then the interrupt will occur only after the system DMA controller has transferred the entire buffer of data.

TYPE I COMMANDS

These commands simply position the R/W heads of the selected drive. Both commands have explicit stepping rate fields. The lower four bits of these commands form the stepping rate.

RESTORE

The Restore command is used to calibrate the position of the R/W head on each drive by stepping the head outward until the TR000 line goes true. Upon receipt of the Restore command, the Busy bit in the Status Register is set. Cylinder High and Cylinder Low Registers are cleared. The lower four bits of the command byte are stored in the stepping rate register for subsequent implied seeks. The state of $\overline{\text{Seek Complete}}$, $\overline{\text{Ready}}$ and $\overline{\text{Write Fault}}$ are sampled, and if an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an interrupt is generated and the Busy bit is reset.

If no errors are encountered thus far, the internal head position register for the selected drive is cleared. The TR000 line is sampled. If TR000 is true, an interrupt is generated and the Busy bit is reset. If TR000 is not true, stepping pulses at a rate determined by the stepping rate field are issued until the TR000 line is activated. When TR000 is activated, the Busy bit is reset and an interrupt is issued. If the TR000 line is not activated within 1023 stepping pulses, the TR000 Error bit in the Error Register and the Error bit in the Status Register are set, the Busy bit is reset and an interrupt is issued.

SEEK

The Seek command positions the R/W head to a certain cylinder. It is primarily used to start two or more concurrent seeks on drives that support buffered stepping. Upon receipt of the Seek command, the Busy bit in the Status Register is set. The lower four bits of the command byte are stored in the stepping rate register for subsequent implied seeks. The state of $\overline{\text{Seek Complete}}$, $\overline{\text{Ready}}$ and $\overline{\text{Write Fault}}$ are sampled, and if an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an interrupt is generated and the Busy bit is reset.

If no errors are encountered thus far, the internal head position register for the selected drive is updated, the direction line is set to the proper direction and a step pulse is issued for each cylinder to be read and an interrupt is issued. Note that the $\overline{\text{Seek Complete}}$ line is not sampled after the Seek command, allowing multiple seek operations to be started using drives with buffered seek capability.

TYPE II COMMANDS

This type of command is characterized by a transfer of a block of data from the WD1000 buffer to the host. This command has an implicit stepping rate as set by the last Restore or Seek command.

The Read Sector command is used to read a sector of data from the disk to the host computer. Upon receipt of the Read command, the Busy bit in the Status register is set. The state of $\overline{\text{Seek Complete}}$, $\overline{\text{Ready}}$ and $\overline{\text{Write Fault}}$ are sampled, and if an error condition exists, the Aborted Command bit in the Error Register is set, the Error bit in the Status Register is set, and a normal completion is simulated.

If no errors are encountered so far, a Seek command is executed. The Seek Complete line is sampled. If the Seek Complete line does not go true within 128 Index pulses, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, and a normal completion is simulated.

Once the head has settled over the desired cylinder, the WD1000 will attempt to read the sector. The WD1000 performs all retries necessary to recover the data during the read command. The controller attempts to read the desired sector up to 16 times. It will attempt a retry if it does not find an ID, if the ID of that sector has a bad CRC, if the Data Address Mark (DAM) couldn't be found or even if the data was actually read from the disk but incurred a data CRC error.

Every time the controller encounters an error, it records the occurance of that error in an internal register. If, after 16 retries, the controller was not able to get a match on the ID field, it assumes that the head was possibly mis-positioned and executes an auto-restore. During the auto-restore, the stepping rate is implied to be equal to the Seek Complete period. After the auto-restore has been successfully completed, the controller re-seeks and attempts to read the sector once again. An auto-restore will be performed only once per read or write sector command.

If the controller encounters a non-recoverable error, the controller examines its internal error history register. It then sets the bit in the Error Register of the highest severity error incurred. If the Data CRC Error bit is set, the data that last produced that error will be available in the sector buffer. The Error bit in the Status Register is set and a normal completion is simulated.

TYPE III COMMANDS

This type of command is characterized by a transfer of a block of data from the host to the WD1000 buffer. These commands have implicit stepping rates as set by the last Restore or Seek command.

WRITE SECTOR

The Write Sector command is used to write a sector of data from the host computer to the disk. Upon receipt of the Write command, the controller generates DRQs for each byte to be written to the buffer. (Note: It is recommended that programmed I/O transfers should take place as a block move without consulting the DRQ bit in the Status Register.)

After all data has been sent to the sector buffer, the Busy bit in the Status Register is set. The state of Seek Complete, Ready and Write Fault are sampled, and if an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an Interrupt is generated and the Busy bit is reset.

If no errors are encountered so far, a Seek command is executed. The Seek Complete line is sampled. If the Seek Complete line doesn't go true within 128 Index pulses, then the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an Interrupt is generated and the Busy bit is reset.

Once the head has settled over the desired cylinder, it will attempt to read the ID of the sector. The WD1000 performs all retries necessary to recover the ID during the write command. The controller attempts to read the ID of the desired sector up to 16 times. It will attempt a retry if it doesn't find an ID or if the ID of that sector has a bad CRC.

Every time the controller encounters an error, it records the occurrence of that error in an internal register. If, after 16 retries, the controller was not able to get a match on the ID field, it assumes that the head was possibly mis-positioned and executes an auto-restore. During the auto-restore, the stepping rate is implied to be equal to the Seek Complete period. After the auto-restore has been successfully completed, the controller re-seeks and attempts to write the sector once again.

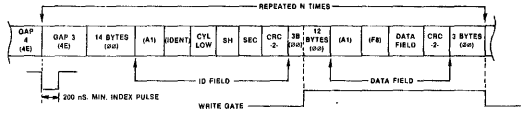
If the controller encounters a non-recoverable error, the controller examines its internal error history register. It then sets the bit in the Error Register of the highest severity error incurred. The Error bit in the Status Register is set, an Interrupt is generated and the Busy bit is reset.

If the proper sector is located, the sector buffer is written to the disk, an interrupt is generated and the Busy bit is reset.

FORMAT TRACK

The Format command is used for initializing the ID and data fields on a particular disk. Upon receipt of the Format command, the controller generates DRQs for each byte of the interleave table to be written to the buffer. In all cases, the number of bytes transferred to the buffer must correspond to the current sector size.

After all data has been sent to the buffer, the Busy bit in the Status Register is set. The state of Seek Complete, Ready and Write Fault lines are sampled. If an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an interrupt is generated and the Busy bit is reset.



NOTE:

1) When MSB of head byte = 1, bad block is detected.
2) Write Gate turn-on is 3 bytes after the ID field's CRC bytes.
3) Write Gate turn-off is 3 bytes after the Data Field's CRC bytes.
4) 12 bytes of zeroes are re-written on a Data Field update.
5) The 2 LSB's of the IDENT byte are used for Cylinder high These values are:
   - FE = 0 to 255 cylinders
   - FF = 256 to 511 cylinders
   - FC = 512 to 767 cylinders
   - FD = 768 to 1023 cylinders
6) GAP 4 values are:

SECTOR LENGTH	GAP 3	GAP 4	SECTOR COUNT
128	15	356	54
256	15	352	32
512	30	800	17

If no errors are encountered so far, a Seek command is executed. No verification of track positioning accuracy is performed because the track may not have any ID fields present. After the Seek operation has been performed, the Seek Complete line is sampled. If the Seek Complete line is not asserted within 128 Index pulses, the Aborted com-

mand bit in the Error Register is set, an Interrupt is generated and the Busy bit is reset.

Once the head has settled over the desired cylinder, the controller starts writing a pattern of 4E's until the index is encountered. Once the index is found, a number of ID fields and nulled data fields are written to the disk. The number of sectors written is equal to the contents of the Sector Count Register. As each sector is written, the Sector Count Register is decremented, and consequently, must be updated before each format operation.

After the last sector is written, the controller back-fills the track with 4E's. When the next index pulse after the last sector is written is encountered, the format operation is terminated, an Interrupt is generated and the Busy bit is reset.

SETTING UP TASK FILES

Before any of the five commands may be executed, a set of parameter registers called the Task File must be set up. For most commands, this informs the WD1000 of the exact location on the disk that the transfer should take place. For a normal read or write sector operation, the Sector Number, the Size/Drive/Head, Cylinder Number, and Command registers (usually in that order) will be written.

Note that most of these registers are readable as well as writable. These registers normally are not read from, but this feature is provided so that error reporting routines can determine physically where an error occurred without recalculating the sector, head and cylinder parameters.

Since the WD1000 can recall all the Task File parameters sent to it, it is recommended that Task File parameters be stored in the WD1000 as they are calculated. This will save the programmer a few instructions by not maintaining two copies of the same information.

Since most hard disk drives contain more than one head per positioner, it is more efficient to step the R/W head assemblies of most disk drives by cylinders, not tracks. In other words, the disk driver software should be designed to read or write all data that is directly accessable by all the heads on a positioner before stepping to a new cylinder.

REGISTER SELECTION ARRAY

$\overline{CS}$	A2	A1	A0	$\overline{RE}$	$\overline{WE}$
1	X	X	X	Deselected	Deselected
0	0	0	0	Data Register	Data Register
0	0	0	1	Error Register	Write Precomp
0	0	1	0	Sector Count	Sector Count
0	0	1	1	Sector Number	Sector Number
0	1	0	0	Cylinder Low	Cylinder Low
0	1	0	1	Cylinder High	Cylinder High
0	1	1	0	Size/Drive/Head	Size/Drive/Head
0	1	1	1	Status Register	Command Register

See page 725 for ordering information.

SDH REGISTOR

BIT	7	6 5	4 3	2 1 0
FUNCTION	0	Sec Size	Drive Select	Head Select

BIT 6	BIT 5	SECTOR SIZE
0	0	256 Bytes
0	1	512 Bytes
1	1	128 Bytes

BIT 4	BIT 3	DRIVE SELECTED
0	0	Drive Sel 0
0	1	Drive Sel 1
1	0	Drive Sel 2
1	1	Drive Sel 3

BIT 2	BIT 1	BIT 0	HEAD SELECTED
0	0	0	Head 0
0	0	1	Head 1
0	1	0	Head 2
0	1	1	Head 3
1	0	0	Head 4
1	0	1	Head 5
1	1	0	Head 6
1	1	1	Head 7

STATUS AND ERROR REGISTER BITS

BIT	STATUS REGISTER	ERROR REGISTER
7	Busy	Bad Block Detect
6	Ready	CRC Error — Data Field
5	Write Fault	CRC Error — ID Field
4	Seek Complete	ID Not Found
3	Data Request	—
2	—	Aborted Command
1	—	TR000 Error
0	Error	DAM not found

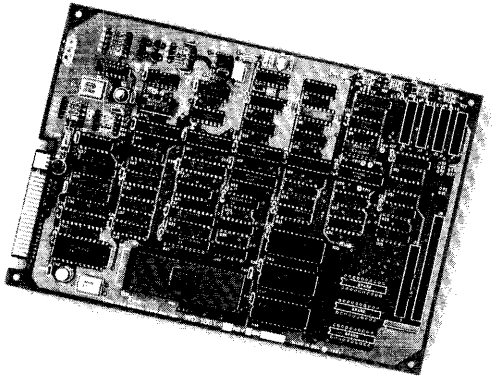
PROGRAMMING

Users familiar with floppy disk systems will find programming the WD1000 a pleasant surprise. A substantial amount of intelligence that was required by the host computer has been incorporated into the WD1000. The WD1000 performs all needed retries, even on data CRC and head positioning errors. Most commands feature automatic 'implied' seek which means that seek commands need not be issued to perform basic read/write functions. The WD1000 keeps track of the position of up to four read/write head assemblies, so the host system does not have to maintain track tables. All transfers to and from the disk are through an on-board full sector buffer. This means that data transfers are fully interruptable and can take place at any speed that is convenient to the system designer. In the event of an unrecoverable error, the WD1000 simulates a normal completion so that special error recovery software is not needed.

Printed in U.S.A.

PRELIMINARY

WD1001 Winchester Disk Controller



GENERAL DESCRIPTION

The WD 1001 is a stand-alone, general purpose Winchester controller board designed to interface up to four Winchester disk drives to a host processor. The drive signals are based upon the floppy look-alike interface available on the Shugart Associates' SA 1000, the Seagate Technology ST506, the Quantum Q2000, and other compatible drives. All necessary buffers and receivers/drivers are included on the board to allow direct connection to the drive. Either a 34 pin (5¼" drive) or 50 pin (8" drive) connector is provided, as well as four 20 pin data connectors.

Communications to and from the host computer are made via a separate computer access port. This port consists mainly of an 8 bit bi-directional bus and appropriate control signals. All data to be written to or read from the disk, status information, and macro commands are transferred via this 8 bit bus. An on board sector buffer allows data transfers to the host computer independent of the actual data transfer rate of the drive.

The WD1001 is based upon a proprietary chip series, the WD1100, specifically designed for Winchester Control.

FEATURES

- SINGLE +5V SUPPLY
- BUILT-IN DATA SEPARATOR
- BUILT-IN WRITE PRECOMPENSATION LOGIC
- DATA RATES UP TO 5 MBITS/SEC
- CONTROL FOR UP TO 4 DRIVES
- CONTROL FOR UP TO 8 R/W HEADS
- 1024 CYLINDER ADDRESSING RANGE
- 256 SECTOR ADDRESSING RANGE
- 32 BIT ECC FOR BURST ERROR CORRECTION
- ERROR CORRECTION ON DATA FIELD ERRORS
- DIAGNOSTIC READS AND WRITES FOR CHECKING ERROR CORRECTION
- BAD BLOCK MAPPING CAPABILITY
- AUTOMATIC FORMATTING
- 128, 256, OR 512 BYTES PER SECTOR (SOFTWARE SELECTABLE)
- UNLIMITED SECTOR INTERLEAVE CAPABILITY
- MULTIPLE SECTOR READS AND WRITES
- OVERLAP SEEK CAPABILITY
- IMPLIED SEEK ON ALL COMMANDS
- AUTOMATIC RETRIES ON ALL ERRORS
- AUTOMATIC RESTORE AND RE-SEEK ON SEEK ERROR
- 8-BIT HOST INTERFACE
- 0°C TO 50°C OPERATION

ORGANIZATION

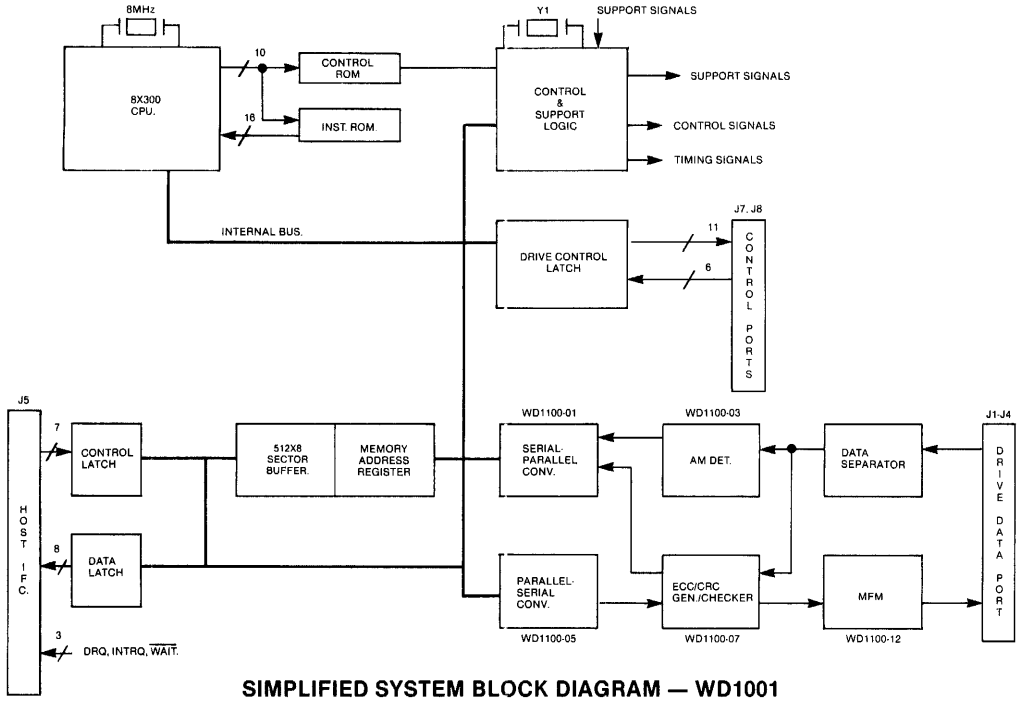
The WD1001 has seven on-board connectors. These connectors consist of a power connector, host interface connector, drive control connector, and four high speed data cable connectors.

The drive control cable is daisy-chained to each of the four drives. Although there is space for two drive control connectors, only one would normally be used for any particular configuration.

The drive data connectors carry differential signals and are radially connected. Up to four drives can be accommodated by the WD1001.

The host interface connector provides interface signals that are compatible with most microprocessors and mini-computers.

The WD1001 provides dual burst detection and single 5-bit burst correction ECC circuitry. The ECC polynomial has been computer generated for optimum error correction on Winchester Disks.



SIMPLIFIED SYSTEM BLOCK DIAGRAM — WD1001

SPECIFICATIONS

Encoding method:	MFM
Cylinders per Head:	Up to 1024
Sectors per Track:	Up to 256 (512 byte sec)
Heads:	8
Drive Selects:	4
Step rate:	10 μS to 7.5 mS (0.5 mS increments)
Data Transfer Rate:	4.34 Mbits/sec or 5.000 Mbits/sec
Write Precomp Time:	12 nanoseconds
Sectoring:	Soft
Host Interface:	8 Bit bi-directional bus
Drive Capability:	10 "LS" Loads
Drive Cable Length:	10 ft. (3M) max.
Host Cable Length:	3 ft. (1 M) max.
Power Requirements:	+5V ±5%, 3.0A Max. (2.5A typ.)
Ambient Temperature Operating:	0°C to 50°C (32 F to 122 F)
Relative Humidity:	20% to 80%
MTBF:	10,000 POH
MTTR:	30 minutes
Length:	9.9 in. (24.9 cm)
Width:	6.8 in. (17.1 cm)
Height:	0.75 in. (1.9 cm)
Mounting Centers:	6.375 x 9.375 in. (16 x 23.6 cm)

HOST INTERFACING

The WD1001 is designed to easily interface to most micro computers and mini-computers. All interfacing is done through the Host Interface Connector (J5). The interface is very similar to Western Digital's family of Floppy Disk Controllers. The only exception is the inclusion of the WAIT line.

WAITS

The $\overline{\text{WAIT}}$ control line goes true whenever either of the following are true:

- The WD1001 is accessing data internally to send to the host during a read operation.
- The WD1001 has not accepted the data from the host during a write operation.

The definition of the $\overline{\text{WAIT}}$ line is very similar to the $\overline{\text{WAIT}}$ signal found on many popular processors. $\overline{\text{WAIT}}$ is also similar to the REPLY signal on Western Digital and other processors.

$\overline{\text{WAIT}}$ will not necessarily make a transition for each access to the WD1001. When the WD1001 can return the requested data within 100 nS, there will be no transition of the $\overline{\text{WAIT}}$ line. This should be interpreted as an instant REPLY on Western Digital Processors.

If the WD1001 cannot return the requested data

within 100 nS, it will assert its $\overline{WAIT}$ line. The period of the $\overline{WAIT}$ signal will vary from 750 nS to 6 μS with 1.25 μS being about average. The period of the $\overline{WAIT}$ only approaches 6 μS during a read or write which happens immediately after a command is written to the command register. This means that longer waits may be encountered during the first read or write to any WD1001 register if that first read or write happens within approximately 6 μS of a command being issued.

During the time that $\overline{WAIT}$ is asserted, the host system **must** hold all of its strobe and address lines stable. On write operations, the DAL lines must also be held stable.

The Host Interface connector (J5) consists of an eight bit bi-directional bus, three bit address bus, and seven control lines. All commands, status, and data are transferred over this bus. See Table 1:

HOST INTERFACE CONNECTOR **TABLE 1**

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME	DESCRIPTION
2 4 6 8 10 12 14 16	1 3 5 7 9 11 13 15	DAL0 DAL1 DAL2 DAL3 DAL4 DAL5 DAL6 DAL7	8 bit bi-directional Data Access Lines. These lines remain in a high-impedance state whenever the $\overline{CS}$ line is inactive.
18 20 22	17 19 21	A0 A1 A2	These three Address Lines are used to select one of eight registers in the Task File. They must remain stable during all read and write operations.
24	23	$\overline{CS}$	When Card Select is active along with $\overline{RE}$ or $\overline{WE}$, Data is read or written via the DAL bus. $\overline{CS}$ must make a transition for each byte read from or written to the task file.
26	25	$\overline{WE}$	When Write Enable is active along with $\overline{CS}$, the host may write data to a selected register of the WD1000.
28	27	$\overline{RE}$	When Read Enable is active along with $\overline{CS}$, the host may read data from a selected register of the WD1001.
30	29	$\overline{WAIT}$	Upon receipt of a $\overline{CS}$, the $\overline{WAIT}$ line may go active. It returns to the inactive state when the DAL lines are valid on a read, or data has been accepted on a write.
32	31	Not Connected	
34	33	Not Connected	
36	35	INTRQ	The INTerrupt ReQuest Line is activated whenever a command has been completed. It is reset to the inactive state when the Status Register is read, or a new command is loaded via the DAL lines.
38	37	DRQ	The Data ReQuest line is activated whenever the sector buffer contains data to be read by the host, or is awaiting data to be loaded by the host. This line is reset whenever the Data Register is read from or written to. The DRQ line will continue to toggle until the buffer is exhausted or until a write or read is performed on the Cylinder Low register.

HOST INTERFACE CONNECTOR **TABLE 1**

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME	DESCRIPTION
40	39	MR	The Master Reset line initializes all internal logic on the logic on the WD1001. Sector Number, Cylinder Number and SDH are cleared, stepping rate is set to 7.5 mS, Write Precomp is set to cylinder 128 and Sector Count is set to 1. The DRQ and INTRQ lines are reset.
	41	Not Connected	
	42	Not Connected	
	43-50	+5V	8 power pins for regulated +5 volts. This power input is also available on J6, pin 3.
Note: Grounds			All even numbered pins (2 through 40) are to be used as signal grounds. Power ground is available on J6, pin 1.

DRIVE CONTROL CONNECTORS

The drive control connector is a (relatively) low speed bus that is daisy chain connected to each of the drives (up to four) in the system. To properly terminate each TTL level output signal from the WD1001, the last drive in the daisy chain should have a 220/330 ohm line termination resistor pack installed. All other drives should have no termination. See Tables 2 and 3:

34 PIN DRIVE CONTROL CONNECTOR **TABLE 2**

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2	O	$\overline{\text{RWC}}$
3	4	O	$\overline{\text{Head Select 2}}$
5	6	O	$\overline{\text{Write Gate}}$
7	8	I	$\overline{\text{Seek Complete}}$
9	10	I	$\overline{\text{TR000}}$
11	12	I	$\overline{\text{Write Fault}}$
13	14	O	$\overline{\text{Head Select 0}}$
15	16	I	$\overline{\text{Sector}}$
17	18	O	$\overline{\text{Head Select 1}}$
19	20	I	$\overline{\text{Index}}$
21	22	I	$\overline{\text{Ready}}$
23	24	O	$\overline{\text{Step}}$
25	26	O	$\overline{\text{Drive Select 1}}$
27	28	O	$\overline{\text{Drive Select 2}}$
29	30	O	$\overline{\text{Drive Select 3}}$
31	32	O	$\overline{\text{Drive Select 4}}$
33	34	O	$\overline{\text{Direction In}}$

50 PIN DRIVE CONTROL CONNECTOR FOR SA1000 TYPE INTERFACE **TABLE 3**

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2	O	$\overline{\text{RWC}}$
3	4	O	$\overline{\text{Head Select 2}}$
5	6		NC
7	8	I	$\overline{\text{Seek Complete}}$
9	10		NC
11	12		NC
13	14	O	$\overline{\text{Head Select 0}}$
15	16	I	$\overline{\text{Sector}}$
17	18	O	$\overline{\text{Head Select 1}}$
19	20	I	$\overline{\text{Index}}$
21	22	I	$\overline{\text{Ready}}$
23	24		NC
25	26	O	$\overline{\text{Drive Select 1}}$
27	28	O	$\overline{\text{Drive Select 2}}$
29	30	O	$\overline{\text{Drive Select 3}}$
31	32	O	$\overline{\text{Drive Select 4}}$
33	34	O	$\overline{\text{Direction In}}$
35	36	O	$\overline{\text{Step}}$
37	38		NC
39	40	O	$\overline{\text{Write Gate}}$
41	42	I	$\overline{\text{TR000}}$
43	44	I	$\overline{\text{Write Fault}}$
45	46		NC
47	48		NC
49	50		NC

DRIVE CONTROL SIGNAL DESCRIPTIONS

RWC

When the Reduce Write Current line is activated with Write Gate, a lower write current is used to compensate for greater bit packing density on the inner cylinders. The $\overline{\text{RWC}}$ line is activated when the cylinder number is greater than or equal to four times the contents of the Write Precomp Register. This output is valid only during Write and Format commands.

$\overline{\text{Write Gate}}$

This output signal allows data to be written on the disk.

$\overline{\text{Seek Complete}}$

Informs the WD1001 that the head of the selected drive has reached the desired cylinder and has stabilized. $\overline{\text{Seek Complete}}$ is not checked after a SEEK command, thus allowing overlapped seeks.

$\overline{\text{Track 000}}$

Indicates that the R/W heads are positioned on the outer-most cylinder. This line is sampled immediately before each step is issued.

$\overline{\text{Write Fault}}$

Informs the WD1001 that some fault has occurred on the selected drive. The WD1001 will not execute commands when this signal is true.

$\overline{\text{HS0}}$ $\overline{\text{HS2}}$

Head Select lines are used by the WD1001 to select a specific R/W head on the selected drive.

$\overline{\text{Index}}$

Is used to indicate the index point for synchronization during formatting and as a time out mechanism for retries. This signal should pulse once each rotation of the disk.

$\overline{\text{Ready}}$

Informs the WD1001 that the desired drive is selected and that its motor is up to speed. The WD1001 will not execute commands unless this line is true.

$\overline{\text{Step}}$

This line is pulsed once for each cylinder to be stepped. The direction of the step will be determined by the $\overline{\text{DIRECTION IN}}$ line. The step pulse period is determined by the internal stepping rate register during implied seek operations or explicitly during Seek and Restore commands. During auto restore, the step pulse period is determined by the SEEK COMPLETE time from the drive.

$\overline{\text{Direction In}}$

Determines the direction of motion of the R/W head when the step line is pulsed. A high on this line defines the direction as out and a low defines direction as in.

$\overline{\text{DS1}}$ $\overline{\text{DS4}}$

These four Drive Select lines are used to select one of four possible drives.

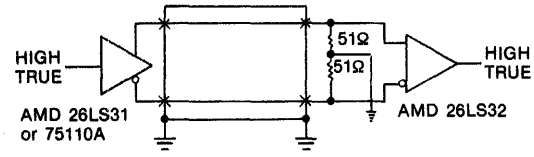
DRIVE DATA CONNECTOR

Four data connectors (J1-4) are provided for clock signals and data between the WD1001 and each drive. All lines associated with the transfer of data between the drive and the WD1001 system are differential in nature and may not be multiplexed. The data connectors are 20 pin vertical headers on tenth-inch centers that mate with Burndy #FRS20BS. The cable used should be flat ribbon cable or twisted pair with a length of less than 10 feet. The cable pin-outs are per Table 4:

DATA CONNECTIONS AND DESCRIPTIONS **TABLE 4**

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
2	1	I	– Drive Selected
4	3		NC
6	5		NC
8	7		NC
	9	O	+ Timing Clock
	10	O	– Timing Clock
11			GND
12			GND
	13	O	+ MFM Write Data
	14	O	– MFM Write Data
15			GND
16			GND
	17	I	+ MFM Read Data
	18	I	– MFM Read Data
19			GND
20			GND

DIFFERENTIAL DATA DRIVER/RECEIVER



NOTE: ANY RS 422 DRIVER/RECEIVER PAIR WILL INTERFACE

$Z_X = 105\Omega$
FLAT RIBBON OR TWISTED PAIR
MAX 10 FT.

POWER CONNECTOR

A three pin molex connector (J6) is provided for power input to the board. The customer supplied mating connector housing is Molex 03-09-1032. The pin-outs are as shown in Table 5:

TABLE 5

PIN	SIGNAL NAME
1	Ground
2	Not Connected
3	+5 V Regulated

COMMANDS

The WD1001 executes five easy to use macro commands. Most commands feature automatic 'implied' seek, which means the host system need not tell the WD1001 where the R/W heads of each drive are or when to move them. The controller automatically performs all needed retries on all errors encountered including data ECC errors. If the R/W head mis-positions, the WD1001 will automatically perform a restore and a re-seek. If the error is completely unrecoverable, the WD1001 will simulate a normal completion to simplify the host system's software.

Commands are executed by loading the command byte into the Command Register while the controller is not busy. (Controller will not be busy if it has completed the previous command.) The task file must be loaded prior to issuing a command. No command will execute if the Seek Complete or Ready lines are false or if the Write Fault line is true. Normally it is not necessary to poll these signals before issuing a command. If the WD1001 receives a command that is not defined in the following table, undefined results will occur.

For ease of discussion, commands are divided into three types which are summarized in Table 6:

TABLE 6

TYPE	COMMAND	BITS 7	6	5	4	3	2	1	0
I	Restore	0	0	0	1	r_3	r_2	r_1	r_0
I	Seek	0	1	1	1	r_3	r_2	r_1	r_0
II	Read Sector	0	0	1	0	D	M	L	0
III	Write Sector	0	0	1	1	0	M	L	0
III	Format Track	0	1	0	1	0	0	0	0

r_3-r_0 — STEPPING RATE

0000 = 10μS	1000 = 4.0mS
0001 = 0.5mS	1001 = 4.5mS
0010 = 1.0mS	1010 = 5.0mS
0011 = 1.5mS	1011 = 5.5mS
0100 = 2.0mS	1100 = 6.0mS
0101 = 2.5mS	1101 = 6.5mS
0110 = 3.0mS	1110 = 7.0mS
0111 = 3.5mS	1111 = 7.5mS

D = DMA Read Mode
0 = Programmed I/O Mode
1 = DMA Mode

L = Long Read/Write
0 = Normal Read/Write
1 = Long Read/Write

M = 1 = Multiple Sector Read/Write
0 = Single Sector Read/Write

NOTE:

The DMA bit is used to position INTRQ in relation to DRQs during the read sector command. If the DMA bit is reset (D = 0), the interrupt will occur before the first DRQ. This allows the programmed I/O host to intervene and transfer the data from the sector buffer. If the DMA bit is set (D = 1), then the interrupt will occur only after the system DMA controller has transferred the entire buffer of data.

TYPE I COMMANDS

These commands simply position the R/W heads of the selected drive. Both commands have explicit stepping rate fields. The lower four bits of these commands form the stepping rate.

RESTORE

The Restore command is used to calibrate the position of the R/W head on each drive by stepping the head outward until the $\overline{TR000}$ line goes true. Upon receipt of the Restore command, the Busy bit in the Status Register is set. Cylinder High and Cylinder Low Registers are cleared. The lower four bits of the command byte are stored in the stepping rate register for subsequent implied seeks. The state of $\overline{Seek\ Complete}$, $\overline{Ready}$ and $\overline{Write\ Fault}$ are sampled, and if an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an interrupt is generated and the Busy bit is rest.

If no errors are encountered thus far, the internal head position register for the selected drive is cleared. The $\overline{TR000}$ line is sampled. If $\overline{TR000}$ is true, an interrupt is generated and the Busy bit is reset. If $\overline{TR000}$ is not true, stepping pulses at a rate determined by the stepping rate field are issued until the $\overline{TR000}$ line is activated. When $\overline{TR000}$ is activated, the Busy bit is reset and an interrupt is issued. If the $\overline{TR000}$ line is not activated within 1023 stepping pulses, the $\overline{TR000}$ Error bit in the Error Register and the Error bit in the Status Register are set, the Busy bit is reset and an interrupt is issued.

SEEK

The Seek command positions the R/W head to a certain cylinder. It is primarily used to start two or more concurrent seeks on drives that support buffered stepping. Upon receipt of the Seek command, the Busy bit in the Status Register is set. The lower four bits of the command byte are stored in the stepping rate register for subsequent implied seeks. The state of $\overline{Seek\ Complete}$, $\overline{Ready}$ and $\overline{Write\ Fault}$ are sampled, and if an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an interrupt is generated and the Busy bit is reset.

If no errors are encountered thus far, the internal head position register for the selected drive is updated, the direction line is set to the proper direction and a step pulse is issued for each cylinder to be read

and an interrupt is issued. Note that the Seek Complete line is not sampled after the Seek command, allowing multiple seek operations to be started using drives with buffered seek capability.

TYPE II COMMANDS

This type of command is characterized by a transfer of a block of data from the WD1001 buffer to the host. This command has an implicit stepping rate as set by the last Restore or Seek command.

READ SECTOR

The Read Sector command is used to read a sector of data from the disk to the host computer. Upon receipt of the Read command, the Busy bit in the Status register is set. The state of Seek Complete, Ready and Write Fault are sampled, and if an error condition exists, the Aborted Command bit in the Error Register is set, the Error bit in the Status Register is set, and a normal completion is simulated.

If no errors are encountered so far, a Seek command is executed. The Seek Complete line is sampled. If the Seek Complete line does not go true within 128 Index pulses, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, and a normal completion is simulated.

Once the head has settled over the desired cylinder, the WD1001 will attempt to read the sector. The WD1001 performs all retries necessary to recover the data during the read command. The controller attempts to read the desired sector up to 16 times. It will attempt a retry if it does not find an ID, if the ID of that sector has a bad CRC or if the Data Address Mark (DAM) couldn't be found or even if the data was actually read from the disk but incurred an uncorrectable error.

Every time the controller encounters an error, it records the occurrence of that error in an internal register. If, after 16 retries, the controller was not able to get a match on the ID field, it assumes that the head was possibly mis-positioned and executes an auto-restore. During the auto-restore, the stepping rate is implied to be equal to the Seek Complete period. After the auto-restore has been successfully completed, the controller re-seeks and attempts to read the sector once again. An auto-restore will be performed only once per read or write sector command.

If the WD1001 encounters an ECC error, it will attempt to correct the data in its sector buffer. If it can correct the data, the Corrected bit in the Status register will be set, if not, the Uncorrectable Error bit is set.

If the controller encounters a non-recoverable error, the controller examines its internal error history register. It then sets the bit in the Error Register of the highest severity error incurred. If the Uncorrectable bit is set, the data that last produced that error will be available in the sector buffer. The Error bit in the Status Register is set and a normal completion is simulated.

READ LONG

This variation of the Read command allows the user to read the ECC check bits directly. The check bits are placed in the data buffer immediately behind the data. This increases the effective buffer length by four bytes.

TYPE III COMMANDS

This type of command is characterized by a transfer of a block of data from the host to the WD1001 buffer. These commands have implicit stepping rates as set by the last Restore or Seek command.

WRITE SECTOR

The Write Sector command is used to write a sector of data from the host computer to the disk. Upon receipt of the Write command, the controller generates DRQs for each byte to be written to the buffer. (Note: It is recommended that programmed I/O transfers should take place as a block move without consulting the DRQ bit in the Status Register.)

After all data has been sent to the sector buffer, the Busy bit in the Status Register is set. The state of Seek Complete, Ready and Write Fault are sampled, and if an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an Interrupt is generated and the Busy bit is reset.

If no errors are encountered so far, a Seek command is executed. The Seek Complete line is sampled. If the Seek Complete line doesn't go true within 128 Index pulses, then the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an Interrupt is generated and the Busy bit is reset.

Once the head has settled over the desired cylinder, it will attempt to read the ID of the sector. The WD1001 performs all retries necessary to recover the ID during the write command. The controller attempts to read the ID of the desired sector up to 16 times. It will attempt a retry if it doesn't find an ID or if the ID of that sector has a bad CRC.

Every time the controller encounters an error, it records the occurrence of that error in an internal register. If, after 16 retries, the controller was not able to get a match on the ID field, it assumes that the head was possibly mis-positioned and executes an auto-restore. During the auto-restore, the stepping rate is implied to be equal to the Seek Complete period. After the auto-restore has been successfully completed, the controller re-seeks and attempts to write the sector once again.

If the controller encounters a non-recoverable error, the controller examines its internal error history register. It then sets the bit in the Error Register of the highest severity error incurred. The Error bit in the Status Register is set, an Interrupt is generated and the Busy bit is reset.

If the proper sector is located, the sector buffer is written to the disk, an interrupt is generated and the Busy bit is reset.

WRITE LONG

This variation of the write command allows the user to introduce various error patterns to check correction capability. The check bits follow the data in the sector buffer. This increases the effective buffer length by four bytes.

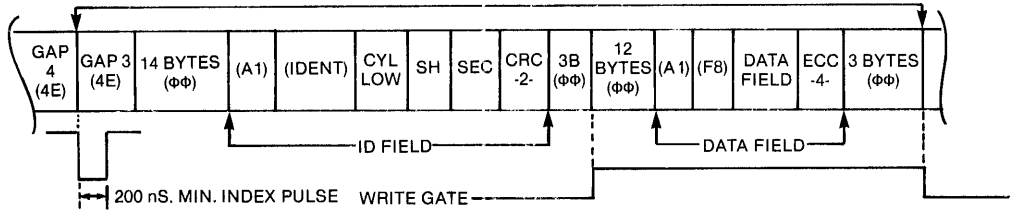
FORMAT TRACK

The Format command is used for initializing the ID and data fields on a particular disk. Upon receipt of the Format command, the controller generates DRQs for each byte of the interleave table to be written to the buffer. In all cases, the number of bytes transferred to the buffer must correspond to the current sector size.

After all data has been sent to the buffer, the Busy bit in the Status Register is set. The state of Seek Complete, Ready and Write Fault lines are sampled. If an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an interrupt is generated and the Busy bit is reset.

If no errors are encountered so far, a Seek command is executed. No verification of track positioning accuracy is performed because the track may not have any ID fields present. After the Seek operation has been performed, the Seek Complete line is sampled. If the Seek Complete line is not asserted within 128 Index pulses, the Aborted command bit in the Error Register is set, an Interrupt is generated and the Busy bit is reset.

Once the head has settled over the desired cylinder, the controller starts writing a pattern of 4E's until the index is encountered. Once the index is found, a number of ID fields and nulled data fields are written to the disk. The number of sectors written is equal to the contents of the Sector Count Register. As each sector is written, the Sector Count Register is decremented, and consequently, must be updated before each format operation.



NOTE:

1) When MSB of head byte = 1, bad block is detected.
2) Write Gate turn-on is 3 bytes after the ID field's CRC bytes.
3) Write Gate turn-off is 3 bytes after the Data Field's ECC or CRC bytes.
4) 12 bytes of zeroes are re-written on a Data Field update.
5) The 2 LSB's of the IDENT byte are used for Cylinder high These values are:
   - FE = 0 to 255 cylinders
   - FF = 256 to 511 cylinders
   - FC = 512 to 767 cylinders
   - FD = 768 to 1023 cylinders
6) GAP 3 values are:

SECTOR LENGTH	GAP 3
128	15
256	15
512	30

After the last sector is written, the controller backfills the track with 4E's. When the next index pulse after the last sector is written is encountered, the format operation is terminated, an Interrupt is generated and the Busy bit is reset.

SETTING UP TASK FILES

Before any of the five commands may be executed, a set of parameter registers called the Task File must be set up. For most commands, this informs the WD1001 of the exact location on the disk that the transfer should take place. For a normal read or write sector operation, the Sector Number, the Size/Drive/Head, Cylinder Number, and Command registers (usually in that order) will be written.

Note that most of these registers are readable as well as writable. These registers normally are not read from, but this feature is provided so that error reporting routines can determine physically where an error occurred without recalculating the sector, head and cylinder parameters.

Since the WD1001 can recall all the Task File parameters sent to it, it is recommended that Task File parameters be stored in the WD1001 as they are calculated. This will save the programmer a few instructions by not maintaining two copies of the same information.

Since most hard disk drives contain more than one head per positioner, it is more efficient to step the R/W head assemblies of most disk drives by cylinders, not tracks. In other words, the disk driver software should be designed to read or write all data that is directly accessible by all the heads on a positioner before stepping to a new cylinder.

REGISTER SELECTION ARRAY

CS	A2	A1	A0	RE	WE
1	X	X	X	Deselected	Deselected
0	0	0	0	Data Register	Data Register
0	0	0	1	Error Register	Write Precomp
0	0	1	0	Sector Count	Sector Count
0	0	1	1	Sector Number	Sector Number
0	1	0	0	Cylinder Low	Cylinder Low
0	1	0	1	Cylinder High	Cylinder High
0	1	1	0	Size/Drive/head	Size/Drive/head
0	1	1	1	Status Register	Command Register

SDH REGISTER

BIT	7	6 5	4 3	2 1 0
FUNCTION	Sec Ext	Sec Size	Drive Select	Head Select

BIT 7	SECTOR EXTENSION
0	Selects CRC for data field
1	Selects ECC for data field

BIT 6	BIT 5	SECTOR SIZE
0	0	256 Bytes
0	1	512 Bytes
1	1	128 Bytes

BIT 4	BIT 3	DRIVE SELECTED
0	0	Drive Sel 0
0	1	Drive Sel 1
1	0	Drive Sel 2
1	1	Drive Sel 3

BIT 2	BIT 1	BIT 0	HEAD SELECTED
0	0	0	Head 0
0	0	1	Head 1
0	1	0	Head 2
0	1	1	Head 3
1	0	0	Head 4
1	0	1	Head 5
1	1	0	Head 6
1	1	1	Head 7

STATUS AND ERROR REGISTER BITS

BIT	STATUS REGISTER	ERROR REGISTER
7	Busy	Bad Block Detect
6	Ready	Uncorrectable
5	Write Fault	CRC Error — ID Field
4	Seek Complete	ID Not Found
3	Data Request	—
2	Corrected	Aborted Command
1	—	TR000 Error
0	Error	DAM not found

PROGRAMMING

Users familiar with floppy disk systems will find programming the WD1001 a pleasant surprise. A substantial amount of intelligence that was required by the host computer has been incorporated into the WD1001. The WD1001 performs all needed retries, even on data ECC and head positioning errors. Most commands feature automatic 'implied' seek which means that seek commands need not be issued to perform basic read/write functions. The WD1001 keeps track of the position of up to four read/write head assemblies, so the host system does not have to maintain track tables. All transfers to and from the disk are through an on-board full sector buffer. This means that data transfers are fully interruptable and can take place at any speed that is convenient to the system designer. In the event of an unrecoverable error, the WD1001 simulates a normal completion so that special error recovery software is not needed.

See page 725 for ordering information.

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

Printed in U.S.A.

ADVANCE INFORMATION

WD1002 Winchester Disk Controller

GENERAL DESCRIPTION

The WD1002 is next generation of Winchester Controllers. It utilizes the WD1010 Winchester controller chip, and provides for floppy disk back up using the WD279X series of single chip floppy controllers.

Incorporated in this controller is all the circuitry needed for Hard disk control with floppy backup.

The firmware is incorporated in the WD1010 and the controller is compatible with previous WD1000 and WD1001. Additional software is needed for the floppy disk backup. Users of the WD1000/WD1001 need not use the floppy controller.

FEATURES

- SINGLE 5V SUPPLY
- FLOPPY DISK BACKUP
- ECC/CRC
- ST506 OR SA1000 INTERFACE
- COMPACT SIZE
- SECTOR SIZES TO 1024
- DATA RATES TO 5MBS
- AUTOMATIC FORMATTING
- WD1000 COMPATIBILITY

See page 725 for ordering information.

Printed in U.S.A.

WD1100 Series Winchester Controller Chips

DESCRIPTION

The WD1100 Chip series provides a low cost alternative for developing a Winchester Controller. These devices have been designed to read and convert an MFM data stream into 8-bit parallel bytes. During a write operation, parallel data is converted back into MFM to be written on the disk. Address Marks are generated and detected while CRC bytes can be appended and checked on the data stream. The WD1100 is fabricated in N-channel silicon gate technology and is available in a 20-pin Dual-In-Line package.

- WD1100-01 SER/PARALLEL CONVERTER
- WD1100-02 MFM GENERATOR
- WD1100-12 IMPROVED MFM GENERATOR
- WD1100-03 AM DETECTOR
- WD1100-04 CRC GENERATOR/CHECKER
- WD1100-05 PAR/SERIAL CONVERTER
- WD1100-06 ECC/CRC LOGIC
- WD1100-07 HOST INTERFACE LOGIC
- WD1100-09 DATA SEPARATION SUPPORT LOGIC

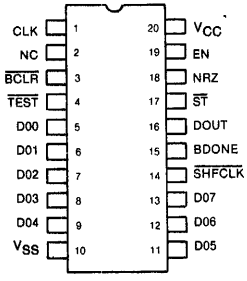
FEATURES

- SA1000/ST506 COMPATIBLE
- SINGLE 5V SUPPLY
- TRI-STATE DATA LINES
- 5 MBITS/SEC TRANSFER RATE
- SIMPLIFIED INTERCONNECT

APPLICATIONS

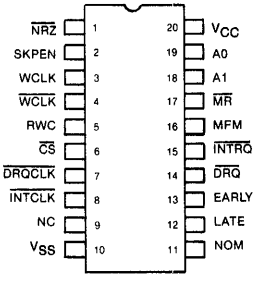
Winchester Controllers For:

- SHUGART ASSOCIATES
- SEAGATE TECHNOLOGY
- QUANTUM CORP.
- TANDON MAGNETICS
- MINISCRIBE
- RMS
- CMI . . . AND OTHERS



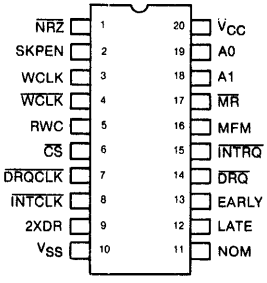
WD1100-01

SERIAL/PARALLEL CONVERTER



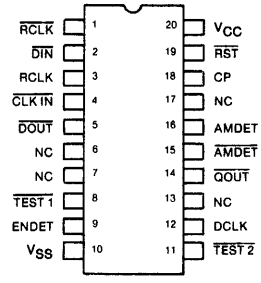
WD1100-02

MFM GENERATOR



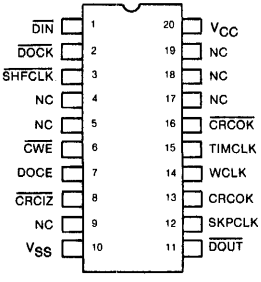
WD1100-12

IMPROVED MFM GENERATOR



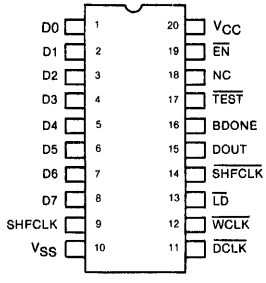
WD1100-03

AM DETECTOR



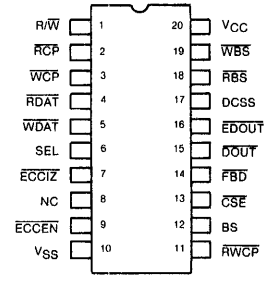
WD1100-04

CRC GENERATOR/CHECKER



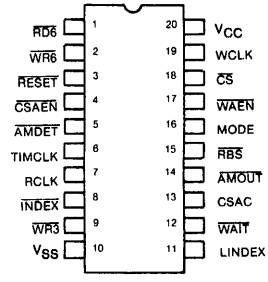
WD1100-05

PARALLEL/SERIAL CONVERTER



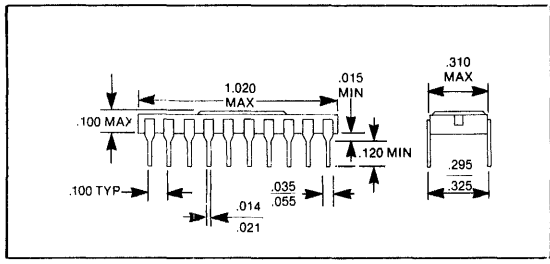
WD1100-06

ECC/CRC LOGIC

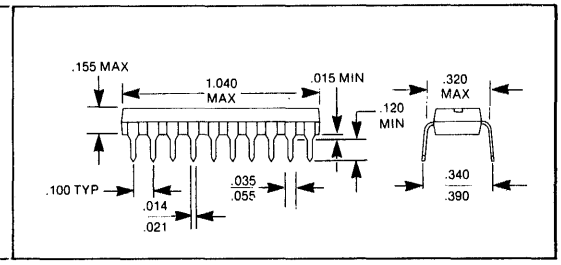


WD1100-07

HOST INTERFACE LOGIC



20 LEAD CERAMIC "U"



20 LEAD PLASTIC 'V"

See page 725 for ordering information.

Printed in U.S.A.

Western Digital
WD1100-01 Serial/Parallel Converter

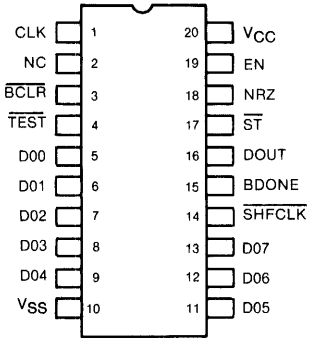
DESCRIPTION

The WD1100-01 Serial/Parallel Converter allows the user to convert NRZ (non-return to zero) data from a Winchester disk drive into 8 bit parallel form. Additional inputs are provided to signal the start of the parallel process, as well as Byte Strobes to signify the end of the conversion. The device contains two sets of 8-bit registers; one register may be read (in parallel), while data is being shifted into the other register. This double-buffering allows the Host to read data from the disk drive at one-eighth the actual data rate.

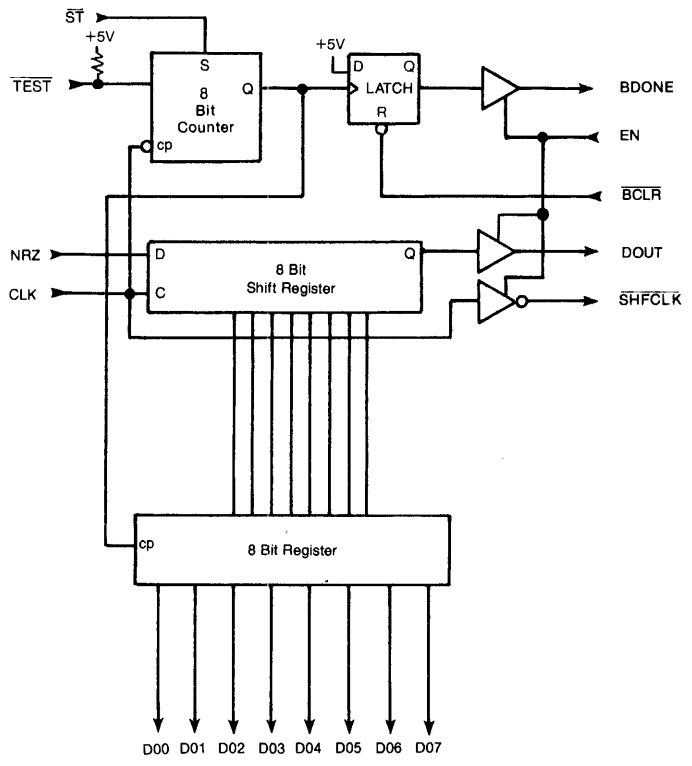
The WD1100-01 is implemented in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic dual-in-line package.

FEATURES

- SINGLE +5V SUPPLY
- DOUBLE BUFFERING
- BYTE STROBE OUTPUTS
- 5MBITS/SEC SHIFT RATE
- SERIAL IN/SERIAL-PARALLEL OUT
- 20 PIN DIP PACKAGE



WD1100-01
Figure 1. Pin Connections



WD1100-01
Figure 2. Block Diagrams

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	CLK	CLOCK	NRZ data is entered into the 8-bit shift register on the low-to-high transition of clock.
2	NC	NO CONNECTION	No connection. This pin is to be left open by the user.
3	$\overline{BCLR}$	$\overline{BYTE\ CLEAR}$	When this line is at a logic 0, the BDONE (Pin 15) line is held reset.
4	$\overline{TEST}$	$\overline{TEST\ INPUT}$	This pin must be left open by the user.
5-9, 11-13	D00-D07	DATA0-DATA7	8 bit parallel data outputs.
10	V_{SS}	GROUND	Ground.
14	$\overline{SHFCLK}$	$\overline{SHIFT\ CLOCK}$	Inverted copy of CLOCK (pin 1) which is active when EN (pin 19) is at a logic 1.
15	BDONE	BYTE DONE	This signal is forced to a logic 1 signifying 8 bits of data have been assembled. BDONE remains in a logic 1 state until reset by a logic 0 on the BCLR (pin 3) line.
16	DOUT	DATA OUT	Serial Data Output from the 8th stage of the internal shift register. DOUT is in a high impedance state whenever EN (pin 19) is at a logic 0.
17	$\overline{ST}$	$\overline{START}$	This line enables the byte counter and is used for synchronization. It must be held to a logic 1 prior to first data bit on the NRZ (Pin 18) line.
18	NRZ	NRZ DATA	NRZ serial data is entered on this pin and clocked by the low to high transition of CLK (pin 1).
19	EN	ENABLE	When this signal is at a logic 0, DOUT, $\overline{SHFCLK}$, and BDONE outputs are in a high impedance state.
20	V_{CC}	V_{CC}	+5V ± 10% power supply input.

DEVICE DESCRIPTION

Prior to shifting data through the device, the WD1100-01 must be synchronized to the data stream. The $\overline{ST}$ line (Pin 17 high) is used to hold the internal bit counter in a cleared state until valid data (NRZ) and clocks (CLK) are entered. The $\overline{ST}$ line is a synchronous input and therefore requires one full cycle of the CLK line (Pin 1) to occur in order to accept a $\overline{ST}$ condition. After this happens, the device is ready to perform serial to parallel conversions.

Data is entered on the NRZ line and clocked into the 8-bit shift register on the low-to-high transition of CLK. The $\overline{ST}$ line must be set low during the low time of CLK. Data is accepted on low-to-high transition of the clock while the high-to-low transition of CLK increments the bit counter. After 8 data bits have been entered the final high-to-low transition of CLK sets an internal latch tied to the BDONE line (Pin 15). At the same time, the contents of the shift register are parallel loaded into an 8 bit register making the parallel data available on the D00-D07 outputs. BDONE will remain in a latched state until the $\overline{BCLR}$ is set to a logic 0, clearing off the BDONE signal. $\overline{BCLR}$ is a level triggered input and must be set back to a logic 1 before the next 8 bits are shifted through the register. BCLR has no effect on the serial shifting process. When the next 8 bits are received, BDONE will again be set and the operation continues.

When interfacing to a microprocessor, BDONE is used to indicate a parallel byte is ready to be read. As the processor reads the data out of the D00-D07 lines, the $\overline{BCLR}$ line should be strobed to clear off BDONE in anticipation of the next assembled byte. An address decode signal generated at the host may be used for this purpose. During a power-up condition, the state of BDONE is indeterminant. It is recommended that $\overline{BCLR}$ be strobed low after power-up to insure that BDONE is cleared.

The serial output line from the last stage of the shift register is available on the DOUT pin. An inverted copy of CLK is available on the $\overline{SHFCLK}$ pin. Both DOUT (Pin 16) and $\overline{SHFCLK}$ (Pin 14) can be used to drive another shift register external to the device.

The three signals BDONE, DOUT, and $\overline{SHFCLK}$ can be placed in a high impedance state by setting EN (Pin 19) to a logic 0. Likewise, EN must be at a logic 1 in order for these signals to be active.

The $\overline{TEST}$ pin is internally OR'ed with the $\overline{ST}$ line to inhibit the bit counter. It is recommended that $\overline{TEST}$ be left open by the user. An internal pull-up resistor is tied to this pin to satisfy the appropriate logic level required internally for proper device operation.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . . . . 0°C to 50°C
Voltage on any pin
with respect to V_{SS} . . . . . −0.2V to +7.0V
Power Dissipation. . . . . 1 Watt
STORAGE TEMPERATURE
PLASTIC. . . . . −55°C to +125°C
CERAMIC. . . . . −55°C to +150°C

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

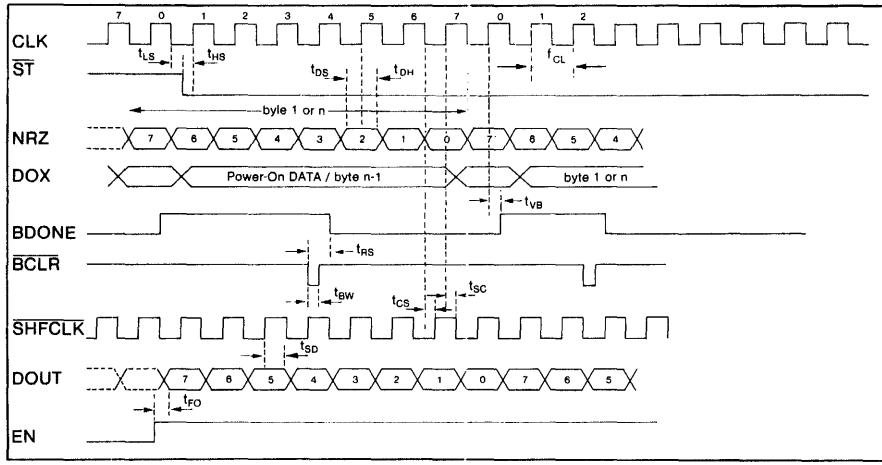
DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_O	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All Outputs Open

AC Electrical Characteristics T_A = 0° to 50°C, V_{CC} = 5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNITS	CONDITION
f_{CL}	CLK FREQUENCY	0		5.25	MHZ	
t_{LS}	↓ CLK to $\overline{ST}$	0			nsec	$\overline{ST}$ = 1 (min 200nsec)
t_{HS}	↑ CLK to $\overline{ST}$	0			nsec	$\overline{ST}$ = 1 (min 200nsec)
t_{DS}	Data set-up to ↑ CLK	15			nsec	
t_{VB}	BDONE valid from ↑ CLK	65		110	nsec	EN = 1
t_{RS}	BDONE reset from $\overline{BCLR}$			110	nsec	EN = 1
t_{BW}	$\overline{BCLR}$ Pulse Width	50			nsec	EN = 1
t_{SC}	↑ CLK to ↓ $\overline{SHFCLK}$			90	nsec	EN = 1
t_{CS}	↓ CLK to ↑ $\overline{SHFCLK}$			100	nsec	EN = 1
t_{SD}	Data delay from ↑ $\overline{SHFCLK}$			55	nsec	EN = 1
t_{FO}	Enable to DOUT ACTIVE			90	nsec	
t_{DH}	Data Hold w.r.t. ↑ CLK	25			nsec	

NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5.0V



WD1100-01
Figure 3.

See page 725 for ordering information.

Western Digital
WD1100-02 MFM Generator

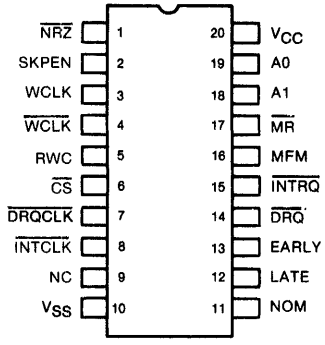
DESCRIPTION

The WD1100-02 MFM Generator converts NRZ data into an MFM (Modified Frequency Modulated) data stream. The derived MFM signal containing both clocks and data can then be used to record information on a Winchester Disk Drive utilizing this recording technique. In addition to an MFM output, the device generates first level Write Precompensation signals for use with inner track densities. A unique feature of the WD1100-02 is the ability to delete a clock pulse in the outgoing MFM stream in order to record Address Marks.

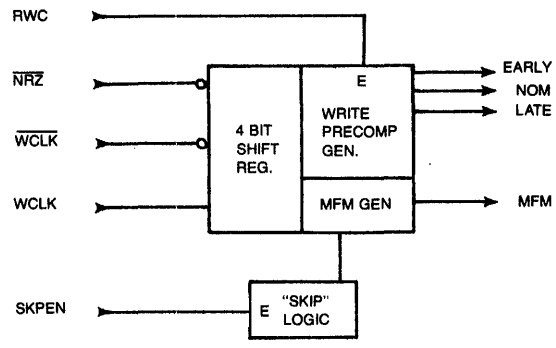
The WD1100-02 is fabricated in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic dual-in-line package.

FEATURES

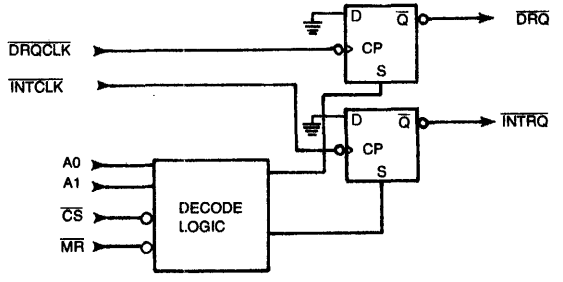
- SINGLE + 5V SUPPLY
- 5 M BIT/SEC DATA RATE
- WRITE PRECOMPENSATION
- ADDRESS MARK GENERATION
- 20 PIN DIP PACKAGE



WD1100-02
Figure 1. Pin Connections



WD1100-02
Figure 2. Block Diagram MFM Generator



WD1100-02
Figure 3. Block Diagram Interrupt Control Logic

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	$\overline{NRZ}$	$\overline{NON\text{-}RETURN\text{-}TO\ ZERO}$	NRZ data input that is strobed into the MFM generator by WCLK (↓).
2	SKPEN	SKIP ENABLE	This input arms the SKIP logic for recording Address Marks when set to a logic 1.
3	WCLK	WRITE CLOCK	Complimentary clock inputs. $\overline{NRZ}$ data is clocked into the MFM Generator on the high-to-low transition of WCLK (pin 3).
4	$\overline{WCLK}$	$\overline{WRITE\ CLOCK}$	
5	RWC	REDUCED WRITE CURRENT	This signal when high, enables EARLY, LATE and NOM outputs.
9	NC	No Connection	No Connection.
10	V_{SS}	V_{SS}	Ground.
11	NOM	NOMINAL	Output signal from the Write Precompensation Logic used to signify that data is to be written nominal.
12	LATE	LATE	Output signal from the Write Precompensation Logic used to signify that data is to be shifted LATE before writing.
13	EARLY	EARLY	Output signal from the Write Precompensation Logic used to signify that data is to be shifted EARLY before writing.
16	MFM	MFM DATA	This output contains the MFM encoded data derived from the $\overline{NRZ}$ (pin 1) line.
6	$\overline{CS}$	$\overline{CHIP\ SELECT}$	Low input signal used to enable the Address decode logic.
8	$\overline{INTCLK}$	$\overline{INTERRUPT\ REQUEST\ CLOCK}$	A high-to-low transition on this line will latch the INTRQ (pin 15) at a logic 0.
7	$\overline{DRQCLK}$	$\overline{DATA\ REQUEST\ CLOCK}$	A high-to-low transition on this line will latch the DRQ (pin 14) at a logic 0.
15	$\overline{INTRQ}$	$\overline{INTERRUPT\ REQUEST}$	This output is latched at a logic 0 when INTCLK (pin 8) makes a high-to-low transition while the decode logic is disabled.
14	$\overline{DRQ}$	$\overline{DATA\ REQUEST}$	This output is latched at a logic 0 when DRQCLK (pin 7) makes a high-to-low transition while the decode logic is disabled.
17	$\overline{MR}$	$\overline{MASTER\ RESET}$	A low level on this line causes DRQ and INTRQ to set at a logic 1.
18, 19	A_0, A_1	ADDRESS 1, 0	When CS is low and the address lines are high, INTRQ is cleared; if the address lines are low then DRQ gets cleared. (i.e. set at a logic 1).
20	V_{CC}	V_{CC}	+5V ±10% power supply input.

DEVICE DESCRIPTION

The WD1100-02 is divided into two sections: MFM Generator and Interrupt Logic. The MFM Generator converts NRZ data into MFM data and provides Write Precompensation signals. The Interrupt Logic is used specifically on the WD1000 Winchester Controller Board and may be used in similar designs to generate Interrupt signals. The two sections of the device are isolated and have no common input or output signals.

Prior to entering data, the SKPEN line must be set to a logic 0 to enable only clocks in the data stream. Data is entered on the $\overline{NRZ}$ line and strobed on the high-to-low transition of WCLK. The encoded NRZ data appears on the MFM (pin 16) output lagging by one clock cycle.

Write Precompensation signals EARLY, LATE, and NOM are generated as each data or clock pulse becomes available at the input when RWC is logic 1. The algorithm used is on Page 8.

LAST DATA SENT		SENDING	TO BE SENT NEXT	EARLY	LATE	NOM
X	1	1	0	H	L	L
X	0	1	1	L	H	L
0	0	0	1	H	L	L
1	0	0	0	L	H	L
ANY OTHER PATTERN				L	L	H

DEVICE DESCRIPTION (CONTINUED)

The SKPEN signal is used to record a unique data/clock pattern as an Address Mark, using $A1_{16}$ data with $0A_{16}$ clock. This pattern is used for synchronization prior to data or ID fields that are read from the disk.

When the SKPEN signal is set to a logic 1, the internal skip logic is enabled. As long as zeroes are being shifted into the $\overline{NRZ}$ line, the device generates normal MFM data. On receipt of the first non-zero bit (typically the MSB of the $A1_{16}$ the skip logic begins to count WCLK cycles. When the MFM generator tries to produce a clock between data bits 2 and 3, the skip logic disables the MFM generator during that time. The result for $A1_{16}$ data is a clock pattern of $0A_{16}$ instead of OE_{16}. Although other data patterns may be used, the MSB of the pattern must be a 1 (80_{16} or higher) in order to enable the skip logic at the proper time. After the skip logic has performed, it then disables itself and MFM data is recorded normally starting with the succeeding byte. To re-enable the skip logic again, the SKPEN line must be strobed.

The Interrupt Logic is used to clear Data Requests ($\overline{DRQ}$) and Interrupt Requests ($\overline{INTRQ}$) by selecting $\overline{CS}$ (pin 6) in combination with A_0 and A_1. The $\overline{MR}$ (Master Reset) signal is used to clear both $\overline{DRQ}$ and $\overline{INRQ}$ simultaneously.

$\overline{MR}$	A_1	A_0	$\overline{CS}$	$\overline{DRQ}$	$\overline{INTRQ}$
0	X	X	X	H	H
1	X	X	1	Q_N	Q_N
1	0	0	0	H	Q_N
1	1	1	0	Q_N	H
1	1	0	0	Q_N	Q_N
1	0	1	0	Q_N	Q_N

X = Don't care

Q_N = remains at previous state

$\overline{DRQ}$ and $\overline{INTRQ}$ can be set to a logic 0 only on the high-to-low transition of $\overline{DRQCLK}$ and $\overline{INTCLK}$ respectively. The signal will remain at a logic 0 until cleared by a $\overline{MR}$ or proper address selection via $\overline{CS}$, A_1, and A_0.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias..... 0°c to 50°c
Voltage on any pin with respect to V_{SS} .. −0.2V to + 7.0V
Power Dissipation..... 1 Watt

STORAGE TEMPERATURE:
PLASTIC..... −55°C to +125°C
CERAMIC..... −55°C to +150°C

NOTE: Maximum ratings indicate operation when permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

DC Electrical Characteristics T_A = 0°C to 50°C, V_{CC} = +5V ± 10%, V_{SS} = 0V

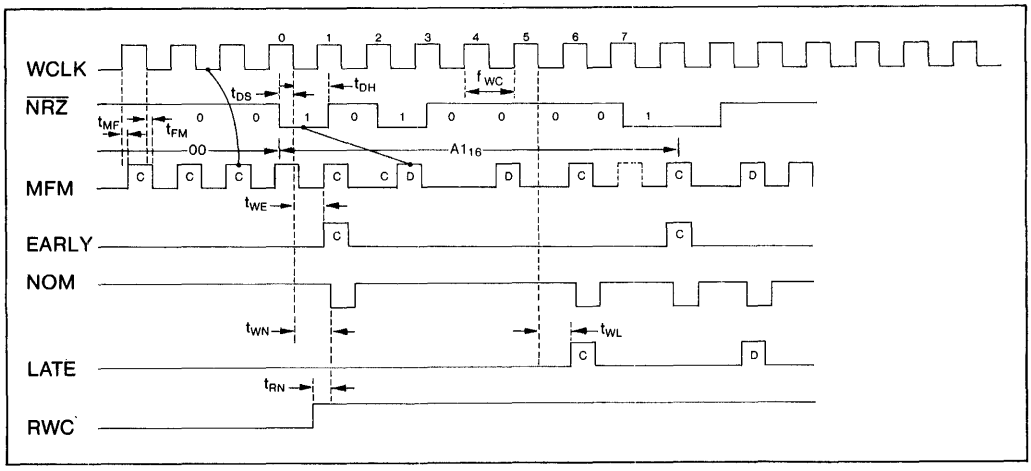
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{OC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

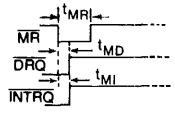
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
f_{WC}	WCLK FREQUENCY			5.25	MHZ	
t_{DS}	Data Setup w.r.t. ↓ WCLK	10			nsec	
t_{DH}	Data hold w.r.t. ↓ WCLK	25			nsec	
t_{MF}	↑ WCLK to ↑ MFM delay			160	nsec	Pin 1 LOW
t_{FM}	↓ WCLK to ↓ MFM delay			180	nsec	Pin 1 LOW
t_{WN}	Data delay to NOM from ↓ WCLK			190	nsec	Pin 4 = LOW
t_{WE}	Data delay to EARLY from ↓ WCLK			180	nsec	Pin 4 = LOW
t_{WL}	Data delay to LATE from ↓ WCLK			180	nsec	Pin 4 = LOW
t_{MR}	Master reset pulse width	50			nsec	
t_{MD}	↓ $\overline{MR}$ to ↑ $\overline{DRQ}$			150	nsec	

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{MI}	↓MR to ↑ $\overline{INTRQ}$			150	nsec	
t_{DQ}	$\overline{DRQCLK}$ pulse width	50			nsec	
t_{IQ}	$\overline{INTCLK}$ pulse width	50			nsec	
t_{DD}	↓ $\overline{DRQCLK}$ to $\overline{DRQ}$			120	nsec	
t_{II}	↓ $\overline{INTCLK}$ to $\overline{INTRQ}$			120	nsec	
t_{AD}	↓AX to ↑ $\overline{DRQ}$			145	nsec	
t_{AI}	↑AX to ↑ $\overline{INTRQ}$			160	nsec	
t_{CD}	↓ $\overline{CS}$ to ↑ $\overline{DRQ}$			145	nsec	
t_{CI}	↓ $\overline{CS}$ to ↑ $\overline{INTRQ}$			180	nsec	
t_{RN}	↑RWC to ↓NOM			115	nsec	

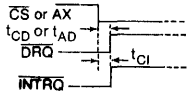
NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5.0V.



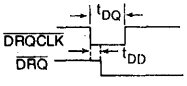
WD1100-02
Figure 4. MFM Generator Timing



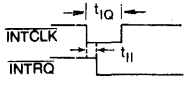
WD1100-02
Figure 5



WD1100-02
Figure 6



WD1100-02
Figure 7.



WD1100-02
Figure 8.

See page 725 for ordering information.

Printed in U.S.A

Western Digital
WD1100-12 Improved MFM Generator

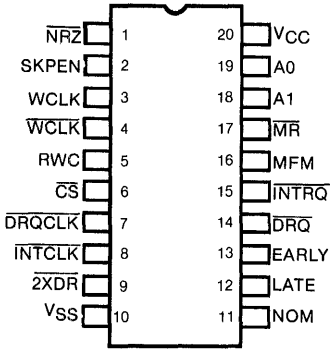
DESCRIPTION

The WD1100-12 improved MFM Generator converts NRZ data into an MFM (Modified Frequency Modulated) data stream. The derived MFM signal containing both clocks and data can then be used to record information on a Winchester Disk Drive utilizing this recording technique. In addition to an MFM output, the device generates first level Write Precompensation signals for use with inner track densities. A unique feature of the WD1100-12 is the ability to delete a clock pulse in the outgoing MFM stream in order to record Address Marks.

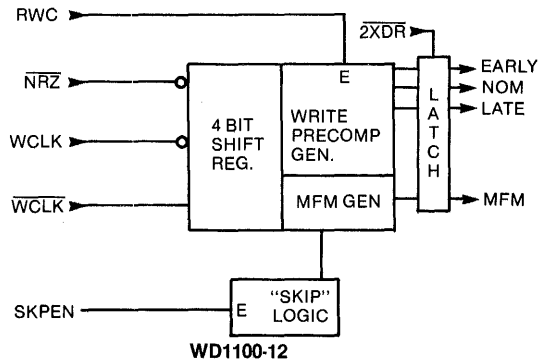
The WD1100-12 is fabricated in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic dual-in-line package.

FEATURES

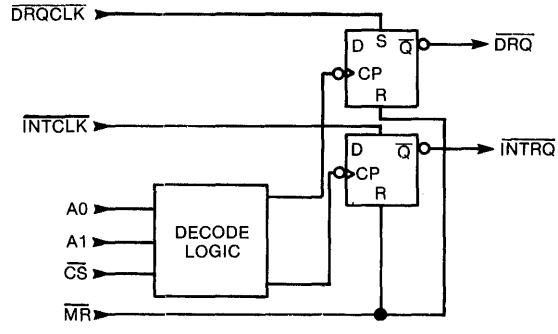
- SINGLE + 5V SUPPLY
- 5 M BIT/SEC DATA RATE
- WRITE PRECOMPENSATION
- ADDRESS MARK GENERATION



WD1100-12
Figure 1. Pin Connections



WD1100-12
*Figure 2. Block Diagram MFM Generator



WD1100-12
Figure 3. Block Diagram Interrupt Control Logic

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	$\overline{NRZ}$	$\overline{NON\text{-}RETURN\text{-}TO\ ZERO}$	NRZ data input that is strobed into the MFM generator by WCLK(↓).
2	SKPEN	SKIP ENABLE	This input arms the SKIP logic for recording Address Marks when set to a logic 1.
3	WCLK	WRITE CLOCK	Complimentary clock inputs. $\overline{NRZ}$ data is clocked into the MFM Generator on the high-to-low transition of WCLK (pin 3).
4	$\overline{WCLK}$	$\overline{WRITE\ CLOCK}$	
5	RWC	REDUCED WRITE CURRENT	This signal when high, enables EARLY, LATE and NOM outputs.
9	$\overline{2XDR}$	$\overline{2\ TIMES\ DATA\ RATE}$	This input is used to latch EARLY, LATE, NOM and MFM outputs.
10	V_{SS}	V_{SS}	Ground.
11	NOM	NOMINAL	Output signal from the Write Precompensation Logic used to signify that data is to be written nominal.
12	LATE	LATE	Output signal from the Write Precompensation Logic used to signify that data is to be shifted LATE before writing.
13	EARLY	EARLY	Output signal from the Write Precompensation Logic used to signify that data is to be shifted EARLY before writing.
16	MFM	MFM DATA	This output contains the MFM encoded data derived from the $\overline{NRZ}$ (pin 1) line.
6	$\overline{CS}$	$\overline{CHIP\ SELECT}$	Low input signal used to enable the Address decode logic.
8	$\overline{INTCLK}$	$\overline{INTERRUPT\ REQUEST\ CLOCK}$	A low on this line will latch the INTRQ (pin 15) at a logic 0.
7	$\overline{DRQCLK}$	$\overline{DATA\ REQUEST\ CLOCK}$	A low on this line will latch the DRQ (pin 14) at a logic 0.
15	$\overline{INTRQ}$	$\overline{INTERRUPT\ REQUEST}$	This output is latched at a logic 0 when INTCLK (pin 8) goes/ is low.
14	$\overline{DRQ}$	$\overline{DATA\ REQUEST}$	This output is latched at a logic 0 when DRQCLK (pin 7) goes/is low.
17	$\overline{MR}$	$\overline{MASTER\ RESET}$	A low level on this line causes DRQ and INTRQ to set at a logic 1.
18, 19	A_0,A_1	ADDRESS 0, 1	When CS is low and the address lines go high, INTRQ is cleared; if the address lines go low then DRQ gets cleared. (i.e. set at a logic 1).
20	V_{CC}	V_{CC}	+5V ± 10% power supply input.

DEVICE DESCRIPTION

The WD1100-12 is divided into two sections: MFM Generator and Interrupt Logic. The MFM Generator converts NRZ data into MFM data and provides Write Precompensation signals. The Interrupt Logic is used specifically on the WD1000 Winchester Controller Board and may be used in similar designs to generate Interrupt signals. The two sections of the device are isolated and have no common input or output signals.

Prior to entering data, the SKPEN line must be set to a logic 0 to enable only clocks in the data stream. Data is entered on the $\overline{NRZ}$ line and strobed on the high-to-low transition of WCLK. The encoded NRZ data appears on the MFM (pin 16) output lagging by one clock cycle.

Write Precompensation signals EARLY, LATE, and NOM are generated as each data or clock pulse becomes available at the input when RWC is logic 1. The algorithm used is on Page 4.

LAST DATA SENT		SENDING	TO BE SENT NEXT	EARLY	LATE	NOM
X	1	1	0	H	L	L
X	0	1	1	L	H	L
0	0	0	1	H	L	L
1	0	0	0	L	H	L
ANY OTHER PATTERN				L	L	H

DEVICE DESCRIPTION (CONTINUED)

The SKPEN signal is used to record a unique data/clock pattern as an Address Mark, using $A1_{16}$ data with $0A_{16}$ clock. This pattern is used for synchronization prior to data or ID fields that are read from the disk.

When the SKPEN signal is set to a logic 1, the internal skip logic is enabled. As long as zeroes are being shifted into the NRZ line, the device generates normal MFM data. On receipt of the first non-zero bit (typically the MSB of the $A1_{16}$ the skip logic begins to count WCLK cycles. When the MFM generator tries to produce a clock between data bits 2 and 3, the skip logic disables the MFM generator during that time. The result for $A1_{16}$ data is a clock pattern of $0A_{16}$ instead of OE_{16}. Although other data patterns may be used, the MSB of the pattern must be a 1 (80_{16} or higher) in order to enable the skip logic at the proper time. After the skip logic has performed, it then disables itself and MFM data is recorded normally starting with the succeeding byte. To re-enable the skip logic again, the SKPEN line must be strobed.

The Interrupt Logic is used to clear Data Requests ($\overline{DRQ}$) and Interrupt Requests ($\overline{INTRQ}$) by selecting $\overline{CS}$ (pin 6) in combination with A_0 and A_1. The $\overline{MR}$ (Master Reset) signal is used to clear both $\overline{DRQ}$ and $\overline{INRQ}$ simultaneously.

MR	A_1	A_0	CS	DRQ	INTRQ
0	X	X	X	H	H
1	X	X	1	Q_N	Q_N
1	0	0	0	H	Q_N
1	1	1	0	Q_N	H
1	1	0	0	Q_N	Q_N
1	0	1	0	Q_N	Q_N

X = Don't care

Q_N = remains at previous state

$\overline{DRQ}$ and $\overline{INTRQ}$ can be set to a logic 0 only by a low level or $\overline{DRQCLK}$ and $\overline{INTCLK}$ respectively. The signal will remain at a logic 0 until cleared by a $\overline{MR}$ or proper address selection via $\overline{CS}$, A_1, and A_0.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias..... 0°C to 50°C
Voltage on any pin with respect to V_{SS}... −0.2V to +7.0V
Power Dissipation..... 1 Watt

STORAGE TEMPERATURE:
PLASTIC..... −55°C to +125°C
CERAMIC..... −55°C to +150°C

NOTE: Maximum ratings indicate operation when permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

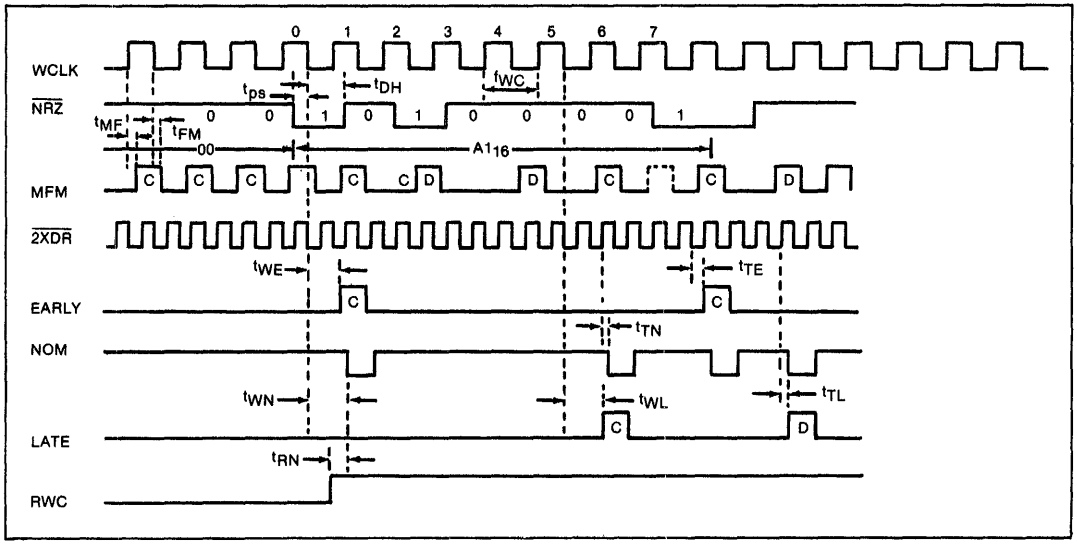
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

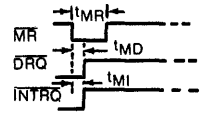
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{FR}	WCLK FREQUENCY			5.25	MHZ	
t_{DS}	Data Setup w.r.t. ↓WCLK	10			nsec	
t_{DH}	Data hold w.r.t. ↓WCLK	25			nsec	
t_{MF}	↑WCLK to ↑MFM delay			210	nsec	Pin 1 LOW
t_{FM}	↓WCLK to ↓MFM delay			230	nsec	Pin 1 LOW
t_{WN}	Data delay to NOM from ↓WCLK			240	nsec	
t_{WE}	Data delay to EARLY from ↓WCLK			230	nsec	
t_{WL}	Data delay to LATE from ↓WCLK			230	nsec	
t_{MR}	Master reset pulse width	50			nsec	
t_{MD}	↓$\overline{MR}$ to ↑$\overline{DRQ}$			150	nsec	

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{MI}	↓MR to ↑$\overline{INTRQ}$			150	nsec	
t_{DQ}	$\overline{DRQCLK}$ pulse width	50			nsec	
t_{IQ}	$\overline{INTCLK}$ pulse width	50			nsec	
t_{DD}	↓$\overline{DRQCLK}$ to $\overline{DRQ}$			120	nsec	
t_{II}	↓$\overline{INTCLK}$ to $\overline{INTRQ}$			120	nsec	
t_{AD}	↓AX to ↑$\overline{DRQ}$			145	nsec	
t_{AI}	↑AX to ↑$\overline{INTRQ}$			160	nsec	
t_{CD}	↓$\overline{CS}$ to ↑$\overline{DRQ}$			145	nsec	
t_{CI}	↓$\overline{CS}$ to ↑$\overline{INTRQ}$			180	nsec	
t_{RN}	↑RWC to ↓NOM			145	nsec	
t_{TE}	↓$\overline{2XDR}$ to ↑EARLY			75	nsec	
t_{TN}	↓$\overline{2XDR}$ to ↑NOM			75	nsec	
t_{TL}	↓$\overline{2XDR}$ to ↑LATE			75	nsec	

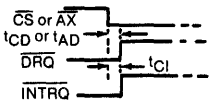
NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5.0V.



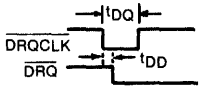
WD1100-12 Figure 4 MFM GENERATOR TIMING



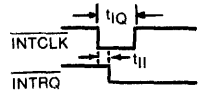
WD1100-12 Figure 5



WD1100-12 Figure 6



WD1100-12 Figure 7



WD1100-12 Figure 8

See page 725 for ordering information.

Printed in U.S.A.

Western Digital
WD1100-03 AM Detector

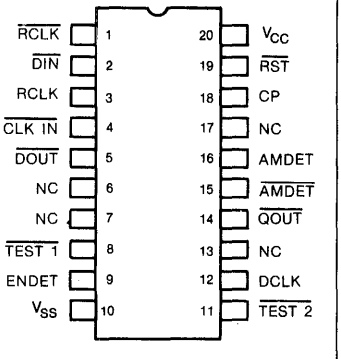
DESCRIPTION

The WD1100-03 Address Mark Detector provides an efficient means of detecting Address Mark Fields in an MFM (NRZ) data stream. MFM (NRZ) clocks and data are fed to the device along with a window clock generated by an external data separator. The WD1100-03 searches the data stream for a DATA = A1, CLK = 0A pattern and produces an AM DET signal when the pattern has been found. NRZ data is an output from the device, which can be used to drive a serial/parallel converter. An uncommitted latch is also provided for by the data separator circuitry, if required.

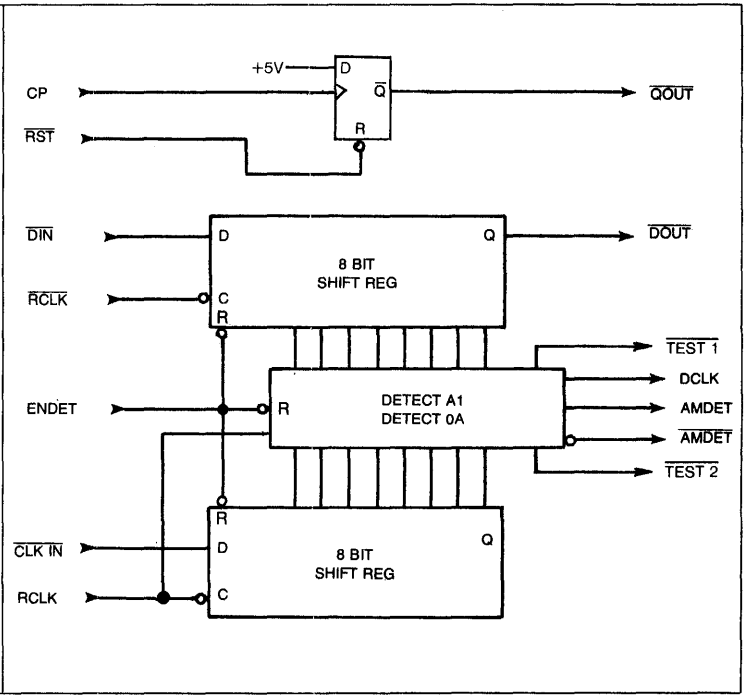
The WD1100-03 Address Mark Detector is fabricated in NMOS silicon gate technology and is available in a 20 pin dual-in-line package.

FEATURES

- SINGLE +5V SUPPLY
- 5 MBITS/SEC DATA RATE
- DECODES $A1_{16}$-$0A_{16}$
- SYNCHRONOUS CLOCK/DATA OUTPUTS
- 20 PIN DIP PACKAGE



WD1100-03
Figure 1. Pin Connections



WD1100-03
Figure 2. Block Diagram

PIN NUMBER	SYMBOL	NAME	FUNCTION
1 3	$\overline{RCLK}$ RCLK	$\overline{READ\ CLOCK}$ READ CLOCK	Complimentary clock inputs used to clock DIN and $\overline{CLK}$ IN into the AM detector.
2	$\overline{DIN}$	$\overline{DATA\ INPUT}$	MFM data pulses from the external Data Separator are connected on this line.
4	$\overline{CLK\ IN}$	$\overline{CLOCK\ INPUT}$	MFM clock pulses from the external Data Separator are connected on this line.
5	$\overline{DOUT}$	$\overline{DATA\ OUTPUT}$	Data Output from the internal Data Shift register, synchronized with DCLK.
6, 7, 13, 17	NC	No Connection	To be left open by the user
8 11	$\overline{TEST\ 1}$ $\overline{TEST\ 2}$	$\overline{TEST\ 1}$ $\overline{TEST\ 2}$	To be left open by the user.
9	ENDET	ENABLE DETECTION	A logic 1 on this line enables the detection logic to search for a data $A1_{16}$ and clock.
10	V_{SS}	V_{SS}	GROUND.
12	DCLK	DATA CLOCK	Clock output that is synchronized with $\overline{DATA\ OUT}$ (Pin 5).
14	$\overline{QOUT}$	$\overline{LATCH\ OUTPUT}$	Signal output from the uncommitted latch.
15	$\overline{AMDET}$	$\overline{ADDRESS\ MARK\ DETECT}$	Complimentary Address Mark Detector output. These signals will go active when a Data = $A1_{16}$ Clock = $0A_{16}$ pattern is detected in the data stream.
16	AMDET	ADDRESS MARK DETECT	
18	CP	CLOCK PULSE	A low-to-high transition on this line will cause the $\overline{QOUT}$ (Pin 14) to be latched at a logic 0.
19	$\overline{RST}$	$\overline{RESET}$	A logic 0 on this line will cause the QOUT (Pin 14) signal to be set at a logic 1.
20	V_{CC}	V_{CC}	+5V ± 10% power supply input.

DEVICE DESCRIPTION

Prior to shifting data through the device, the internal logic must be initialized. While the ENDET (Pin 9) line is at a logic 0, shifting of data will be inhibited and $\overline{AMDET}$, AMDET, $\overline{CLK}$, and $\overline{DATA\ OUT}$ will remain inactive.

When ENDET is at a logic 1, shifting is enabled. NRZ data is entered on the $\overline{DIN}$ line (Pin 2) and shifted on the high-to-low transition of $\overline{RCLK}$ (Pin 1). NRZ clocks are entered on the $\overline{CLK}$ IN line, and shifted on the high-to-low transition of RCLK (Pin 3). The $\overline{DOUT}$ line (Pin 5) is tied to the last stage of the internal Data Shift register and will reflect information clocked into the DIN line delayed by 8 bits.

While each bit is being shifted, a 16 bit comparator is continuously checking the parallel contents of the shift registers for the DATA = $A1_{16}$, CLK = $0A_{16}$ pattern. When this pattern is detected, AMDET will be set to a logic 0 and AMDET will be set to a logic 1. $\overline{AMDET}$ and AMDET will remain latched until the device is re-initialized by forcing ENDET to a logic 0.

When an AM is detected, DCLK will begin to toggle. Data present on the $\overline{DOUT}$ line may then be clocked into an external serial/parallel converter. DCLK will remain inactive when ENDET is held at a logic 0.

An uncommitted edge-triggered flip/flop has been provided to facilitate the detection of high frequency by the data separator, but may be used for any purpose. The low-to-high transition of CP (Pin 18) will set the $\overline{QOUT}$ (Pin 14) to a logic 0. $\overline{QOUT}$ may be reset back to a logic 1 by a low level on the $\overline{RST}$ line (Pin 19).

$\overline{TEST1}$ and $\overline{TEST2}$ are output lines. $\overline{TEST1}$ is an active low pulse when an $A1_{16}$ is detected, and $\overline{TEST2}$ is active low pulse when a $0A_{16}$ is detected. These signals are used for test points and therefore should be left open by the user if not required.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under bias ..... 0°C to 50°C
Voltage on any pin with respect to V_{SS} ... −0.2V to +7.0V
Power dissipation ..... 1 Watt

STORAGE TEMPERATURE
PLASTIC ..... −55°C to +125°C
CERAMIC ..... −55°C to +150°C

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

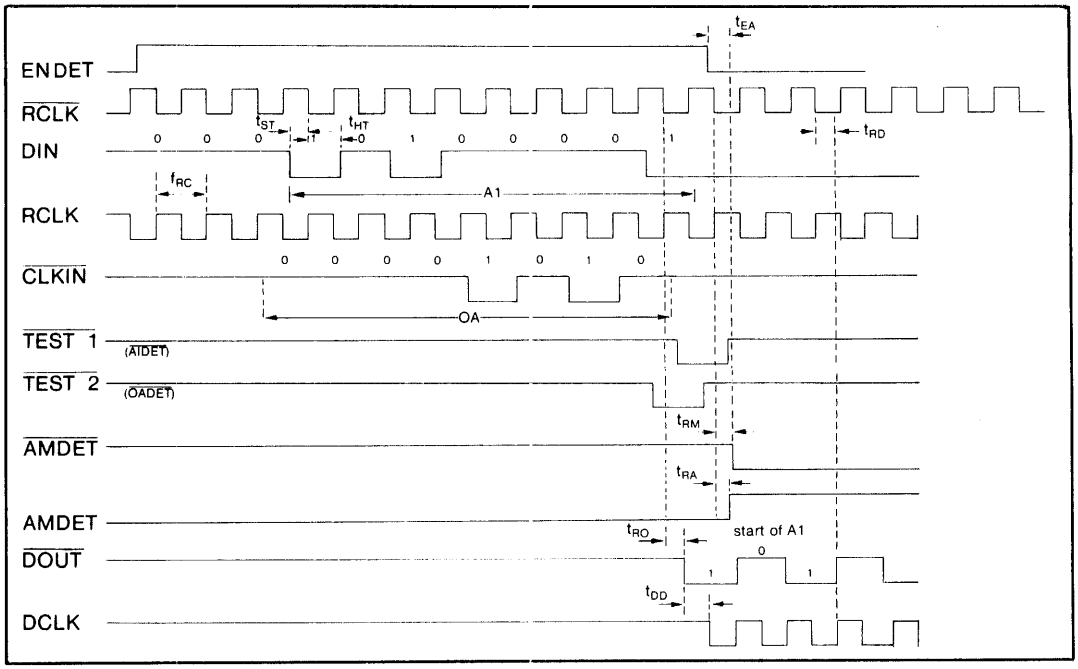
DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.7	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
f_{RC}	RCLK Frequency			5.25	MHZ	
t_{ST}	Data Setup time	40			nsec	
t_{HT}	Data Hold time	10			nsec	
t_{DD}	$\overline{DOUT}$ to DCLK DELAY			110	nsec	
t_{RD}	↓$\overline{RCLK}$ to ↑ DCLK			120	nsec	
t_{RA}	↓$\overline{RCLK}$ to ↑ AMDET			115	nsec	
t_{RM}	↓$\overline{RCLK}$ to ↓$\overline{AMDET}$			125	nsec	
t_{RO}	↓$\overline{RCLK}$ to $\overline{DOUT}$			135	nsec	
t_{EA}	↓ ENDET to ↓ AMDET			130	nsec	
t_{RQ}	↓$\overline{RST}$ to ↑$\overline{QOUT}$			110	nsec	
t_{RW}	Pulse width of $\overline{RST}$	50			nsec	
t_{CW}	CP Pulse width	90			nsec	
t_{CQ}	↑ CP to ↓$\overline{QOUT}$			106	nsec	

NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5V.



WD1100-03
Figure 3. Functional Timing

See page 725 for ordering information.

Printed in U.S.A.

Western Digital
WD1100-04 CRC Generator/Checker

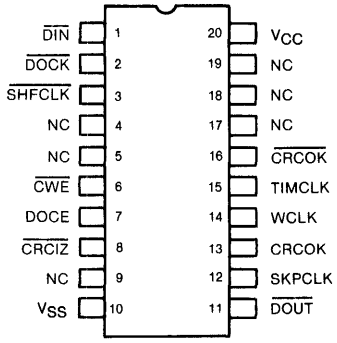
DESCRIPTION

The WD1100-04 CRC Generator/Checker is designed to generate a Cyclic Redundancy Checkword from a serial data stream, and to check a data stream against a known CRC word. Complimentary latched "CRCOK" outputs are provided to indicate CRC errors in check mode. Additional logic has been included to shift the CRC checkword out of the device by signals generated on other WD1100 family devices.

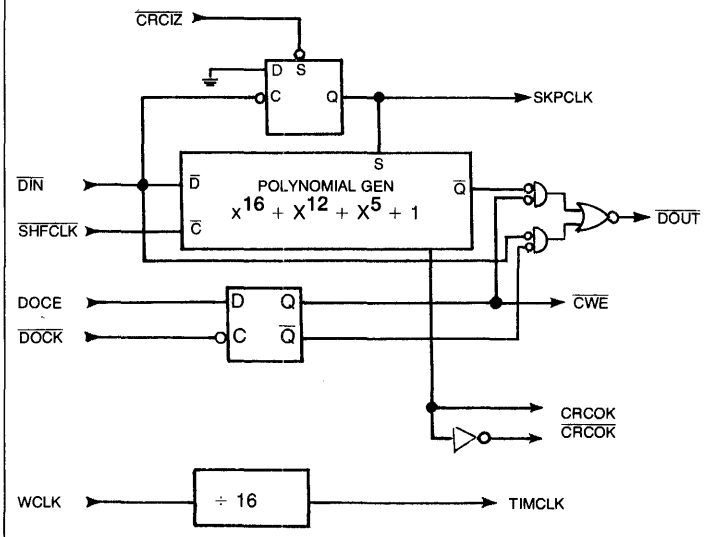
The WD1100-04 is fabricated in NMOS silicon gate technology and is available in a 20 pin dual-in-line package.

FEATURES

- GENERATES/CHECKS CRC
- SINGLE +5V SUPPLY
- LATCHED ERROR OUTPUTS
- $X^{16} + X^{12} + X^5 + 1$ (CCITT-16)
- AUTOMATIC PRESET
- 20 PIN DIP PACKAGE



WD1100-04
Figure 1. Pin Connections



WD1100-04
Figure 2. Block Diagram

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	$\overline{DIN}$	$\overline{DATA\ INPUT}$	Active low serial input data stream is used to generate/check the 2 byte CRC word.
2	$\overline{DOCK}$	$\overline{DATA\ OR\ CRC\ WORD\ CLOCK}$	After a byte of data has been transferred in, this input signal is used to latch the state of DOCE in an internal D flop with a high to low transition.
3	$\overline{SHFCLK}$	$\overline{SHIFT\ CLOCK}$	The falling edge shifts data bits into the CRC generator/checker. It also transfers the CRC check word to $\overline{DOUT}$ in the write mode (DOCE = LOW). The rising edge also activates the CRCOK lines in the read mode when no error is found.
4, 5	N.C.	NO CONNECTION	
6	$\overline{CWE}$	$\overline{CHECK\ WORD\ ENABLE}$	This active low output indicates that the CRC checkword is being output on the $\overline{DOUT}$ line. When $\overline{CWE}$ is high, data is being output on $\overline{DOUT}$.
7	DOCE	DATA OR CRC ENABLE	Initially, this input line is held high to direct input data (pin 1) to the output data (pin 11). After the next to the last BYTE is transmitted but before the last BYTE occurs DOCE must be low to direct the 2 CRC check bytes to DOUT (pin 11). DOCE must be maintained low for a minimum of 2 byte times. DOCE is used only in the write mode.
8	$\overline{CRCIZ}$	$\overline{CYCLIC\ REDUNDANCY\ CHECK\ INITIALIZE}$	When this line is at a logic 0, the SKPCLK output line is held high and the CRC generator is held preset to hex "FFFF."
9	N.C.	NO CONNECTION	
10	V_{SS}	GROUND	GROUND.
11	$\overline{DOUT}$	$\overline{DATA\ OUTPUT}$	In the write mode, this line outputs the unmodified data stream along with the 2 byte CRC word appended to the end of the stream.
12	SKPCLK	SKIP CLOCK	The first high-to-low transition on $\overline{DIN}$ (pin 1) resets SKPCLK low and enables the CRC to either generate or check the CRC word.
13	CRCOK	CYCLIC REDUNDANCY CHECK OKAY	In the read mode, after the 2 byte CRC word is entered on $\overline{DIN}$ and no error has been detected, this line is set high to indicate no errors have occurred. This line will then remain high as long as $\overline{DIN}$ is maintained high.
14	WCLK	WRITE CLOCK	This input clock is divided by 16 to produce TIMCLK (pin 15) and has no effect on the rest of the internal circuitry.
15	TIMCLK	TIMING CLOCK	See above.
16	$\overline{CRCOK}$	$\overline{CYCLIC\ REDUNDANCY\ CHECK\ OKAY}$	Complementary output version of CRCOK (pin 13).
17-19	N.C.	NO CONNECTION	
20	V_{CC}	V_{CC}	+5V ± 10% power supply input.

DEVICE DESCRIPTION

Prior to shifting data thru the device (either in the read or write modes) the CRC generator/checker is initialized by strobing the $\overline{CRCIZ}$ (pin 8) low. This forces the SKPCLK (pin 12) line to the high state. The first low going transition on $\overline{DIN}$ (pin 1), namely the most significant bit of an address mark, resets the SKPCLK line. The WD1100-04 has now been properly initialized and is ready to generate/check the CRC bytes. The CRCOK and $\overline{CRCOK}$ lines should be set to their inactive states.

In the write mode, initially the DOCE (pin 7) is held high and a pseudo $\overline{DOCK}$ is produced by supplying a string of zeros before the address mark. This ensures the proper state of the internal D flip flop to gate input data to the output line $\overline{DOUT}$ (pin 11). As shown in the block diagram the $\overline{CWE}$ (pin 6) will be set high. Sometime between the next to the last and the last $\overline{DOCK}$ that indicates the end of the data stream, DOCE (pin 7) is lowered to ensure the smooth transition of the 2 byte CRC checkword to the output line $\overline{DOUT}$ (pin 11).

DOCE must be maintained low for a minimum of 2 byte times. After the CRC word is generated, $\overline{DOUT}$ will produce a string of zeros (i.e., held high). This portion of the circuitry is dormant in the read mode.

After proper initialization, input data is entered on $\overline{DIN}$ (pin 1) along with the 2 byte CRC word for the read mode of operation. At the end of the data stream, if no errors were detected the CRCOK (pin 13) is set high. Accordingly the complimentary output (pin 16) is set low. These output states will be maintained as long as $\overline{DIN}$ is held high and $\overline{CRCIZ}$ (pin 8) is not strobed. If the CRCOK lines do not become active, an error has been detected and a re-try is in order. If successive re-tries fail, an error flag may be set to determine a further course of action as desired by the user.

WCLK is divided by 16 to produce TIMCLK which may be used as a buffered step clock for SA1000 compatible drives.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . . . . 0°c to 50°c
Voltage on any pin with respect to V_{SS} . . . −0.2V to +7.0V
Power Dissipation . . . . . 1 Watt

STORAGE TEMPERATURE
PLASTIC . . . . . −55°C to +125°C
CERAMIC . . . . . −55°C to +150°C

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

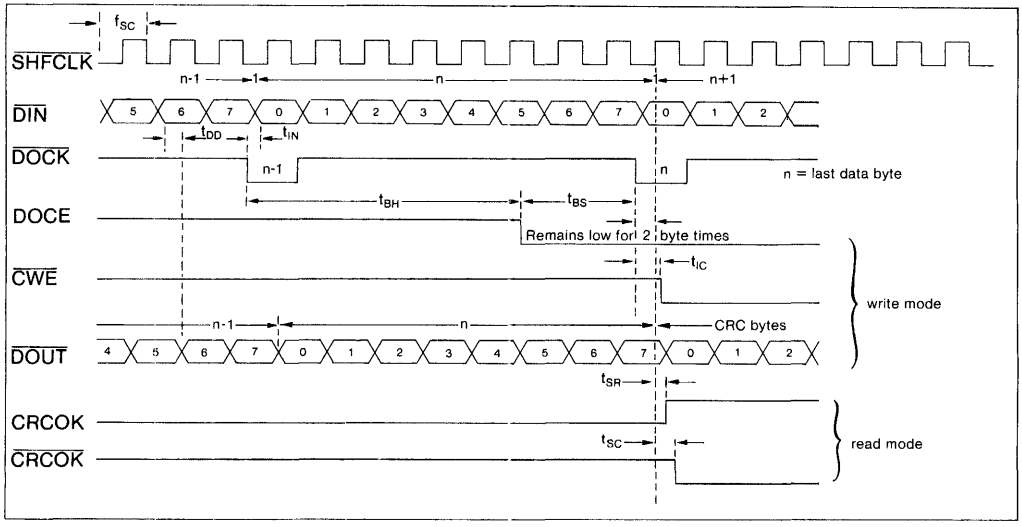
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

AC Electrical Characteristics T_A = 0° to 50°C, V_{CC} = 5V ± 10%, V_{SS} = 0V

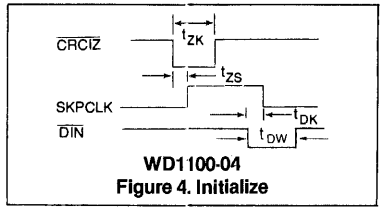
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{WT}	↑WCLK to ↓TIMCLK			95	nsec	
t_{WR}	↑WCLK to ↑TIMCLK			85	nsec	
t_{ZS}	↓$\overline{CRCIZ}$ to ↑SKPCLK			120	nsec	
t_{ZK}	$\overline{CRCIZ}$ pulse width	90			nsec	
t_{BS}	DOCE set up time w.r.t. ↓$\overline{DOCK}$	20			nsec	
t_{BH}	DOCE hold time w.r.t. ↓$\overline{DOCK}$	40			nsec	
t_{DD}	$\overline{DIN}$ to $\overline{DOUT}$ delay			105	nsec	CWE set high

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{DK}	↓$\overline{DIN}$ to ↓ SKPCLK			120	nsec	
t_{DW}	$\overline{DIN}$ P.W. to reset SKPCLK	50			nsec	
t_{IC}	↓ $\overline{DOCK}$ to ↓ $\overline{CWE}$			120	nsec	
t_{BC}	↓ $\overline{DOCK}$ to ↑ $\overline{CWE}$			120	nsec	
f_{SC}	$\overline{SHFCLK}$ frequency			5.25	MHZ	
t_{SR}	↑ $\overline{SHFCLK}$ to ↑ CRCOK			85	nsec	
t_{SC}	↑ $\overline{SHFCLK}$ to ↓ $\overline{CRCOK}$			90	nsec	
t_{IN}	↓ $\overline{DOCK}$ to ↓ $\overline{DIN}$			90	nsec	

Notes: 1. Typical values are for T_A = 25°C and V_{CC} = +5.0V



WD1100-04
Figure 3. Write Mode



WD1100-04
Figure 4. Initialize

See page 725 for ordering information.

Printed in U.S.A

Western Digital
WD1100-05 Parallel/Serial Converter

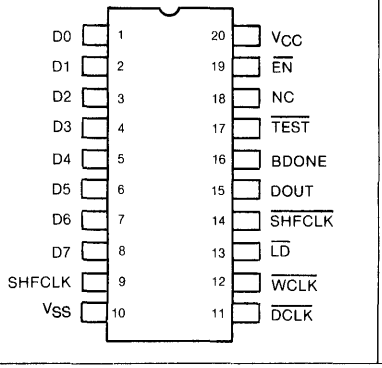
DESCRIPTION

The WD 1100-05 Parallel/Serial Converter allows the user to convert a byte of data to a serial stream when writing to a disk or any serial device. Parallel data is entered via the D0-D7 lines on the rising edge of $\overline{DCLK}$. A synchronous BYTE counter is used to signify that 8 bits of data have been shifted out and that the 8 bit latch is ready to be reloaded. The double buffering of the data permits another byte to be loaded while the previous byte is in the process of being shifted.

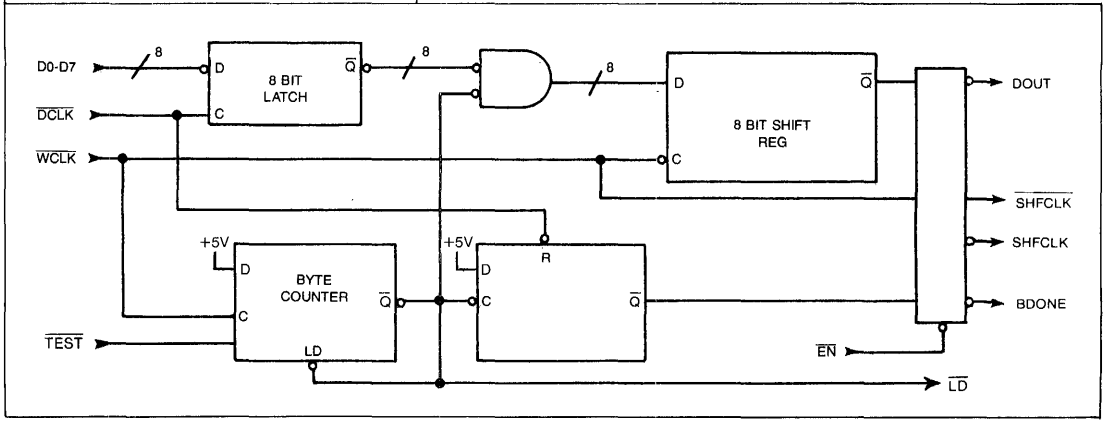
The WD1100-05 is implemented in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic dual-in-line package.

FEATURES

- SINGLE +5V SUPPLY
- DOUBLE BUFFERING
- BYTE STROBE OUTPUTS
- 5 M BITS/SEC SHIFT RATE
- TRI-STATE OUTPUT CONTROL
- PARALLEL IN/SERIAL OUT
- 20 PIN DIP PACKAGE



WD1100-05
Figure 1. Pin Connections



WD1100-05
Figure 2. Block Diagram

PIN NUMBER	SYMBOL	NAME	FUNCTION
1-8	D0-D7	DATA 0-DATA 7	8 bit parallel data inputs (bit 7 = MSB).
9	SHFCLK	SHIFT CLOCK	Inverted copy of $\overline{\text{WCLK}}$ (pin 12) which is active when ENABLE (pin 19) is at a logic 0.
10	V_{SS}	GROUND	GROUND.
11	$\overline{\text{DCLK}}$	$\overline{\text{DATA CLOCK}}$	Active low input signal resets the BDONE (pin 16) latch. The low-to-high (trailing edge) clocks the input data into the internal 8 bit latch.
12	$\overline{\text{WCLK}}$	$\overline{\text{WRITE CLOCK}}$	The high-to-low (↓) edge of this clock signal is used to shift the data out serially. The low-to-high (↑) edge is used to update the internal byte counter (module 8).
13	$\overline{\text{LD}}$	$\overline{\text{LOAD}}$	This active low signal indicates that the Byte Counter is being preset to 1. Normally left open by the user.
14	$\overline{\text{SHFCLK}}$	$\overline{\text{SHIFT CLOCK}}$	Delayed copy of $\overline{\text{WCLK}}$ (pin 12) which is active when EN (pin 19) is at a logic 0.
15	DOUT	DATA OUT	Serial data output enabled by EN (pin 19).
16	BDONE	BYTE DONE	This output signal is forced to a logic 1 whenever 8 bits of data have been shifted out. BDONE remains in this state unless reset by the loading of another byte of data.
17	$\overline{\text{TEST}}$	$\overline{\text{TEST INPUT}}$	This pin must be left open by the user.
18	NC	No Connection	
19	$\overline{\text{EN}}$	$\overline{\text{ENABLE}}$	This active low signal enables DOUT, $\overline{\text{SHFCLK}}$, SHFCLK, and BDONE outputs. When high, these output signals are in a high impedance state.
20	V_{CC}	V_{CC}	+5 ± 10% power supply input.

DEVICE DESCRIPTION

Prior to loading the WD1100-05, it is recommended that 00H (or FF) be loaded into the input buffers to ensure that DOUT is at a fixed level. $\overline{\text{EN}}$ (pin 19) is set to a logic 0 to enable the device outputs.

Data is entered on the D0-D7 input lines and is strobed into the data latches on the rising edge of $\overline{\text{DCLK}}$ (pin 11). $\overline{\text{DCLK}}$ also resets BDONE (pin 16). The first BDONE that comes up simply means that the WD1100-05 is ready to accept another byte of data and that the previous byte entered is in the process of being shifted out. If the BDONE is serviced prior to every 8th WRITE CLOCK pulse the output data will represent a contiguous block of the bytes entered. Due to the asynchronous nature of the WD1100-05, the input data will be available in serial form at the output anywhere from 8 to 16 write clock cycles later.

Data is shifted out on the high-to-low (↓) transition of the $\overline{\text{WCLK}}$ (pin 12). The low-to-high (↑) transition of $\overline{\text{WCLK}}$ increments a byte counter which in turn sets the BDONE signal high after 8 bits of data have been shifted out. The low-to-high transition of BDONE also causes the loading of the data buffer into the shift register. The data buffer is now ready to be reloaded with the next byte.

The loading of the next byte automatically clears the BDONE signal. The entire process as outlined above is repeated. BDONE always needs to be serviced within 8 $\overline{\text{WCLK}}$ cycles unless the next byte to be transmitted is the same as the previous byte.

Four signals, BDONE, DOUT, $\overline{\text{SHFCLK}}$, and SHFCLK, can be placed in a high impedance state by setting $\overline{\text{EN}}$ (pin 19) to a logic 1. Likewise, $\overline{\text{EN}}$ must be at a logic 0 in order for these signals to drive any external device.

The $\overline{\text{TEST}}$ pin is internally OR'ed with the counter output to produce the $\overline{\text{LD}}$ (pin 13) signal. This is used to inhibit the bit counter by external means for test purposes. It is recommended that $\overline{\text{TEST}}$ be left open by the user. An internal pullup register is tied to this pin to satisfy the appropriate logic level required for proper device operation.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . . . . 0°C to 50°C
Voltage on any pin with respect to V_{SS} . . . −0.2V to +7.0V
Power Dissipation. . . . . 1 Watt
STORAGE TEMPERATURE
PLASTIC. . . . . −55°C to +125°C
CERAMICS. . . . . −55°C to +150°C

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

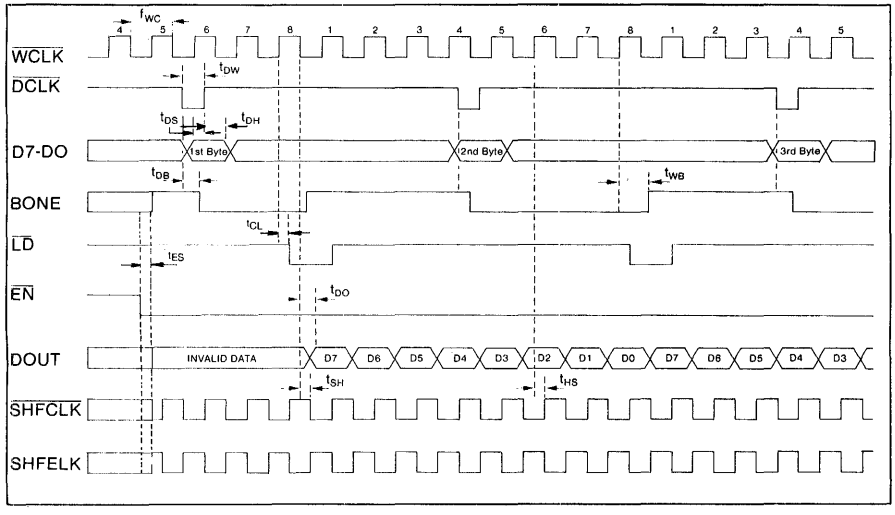
DC Electrical Characteristics: T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{OH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All Outputs Open

AC Electrical Characteristics: T_A = 0°C to 50°C; V_{CC} = +5 ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
f_{WC}	WCLK frequency			5.25	MHZ	
t_{DW}	DCLK pulse width	50			nsec	
t_{DS}	Data set-up w.r.t. ↑ DCLK	30			nsec	
t_{DH}	Data hold time w.r.t. ↑ DCLK	30			nsec	
t_{DB}	↓ DCLK to ↓ BDONE			130	nsec	EN = 0
t_{DO}	↓ WCLK to DOUT			130	nsec	EN = 0
t_{SH}	↓ WCLK to ↓ SHFCLK			75	nsec	EN = 0
t_{HS}	↑ WCLK to ↑ SHFCLK			70	nsec	EN = 0
t_{WB}	↑ WCLK to ↑ BDONE	75		180	nsec	
t_{ES}	↓ $\overline{EN}$ to BDONE, DOUT SHFCLK ACTIVE			25	nsec	
t_{CL}	↑ $\overline{WCLK}$ to ↓ $\overline{LD}$			50	nsec	

NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5.0V



WD1100-05
Figure 3. Functional Timing Diagram

Printed in U.S.A

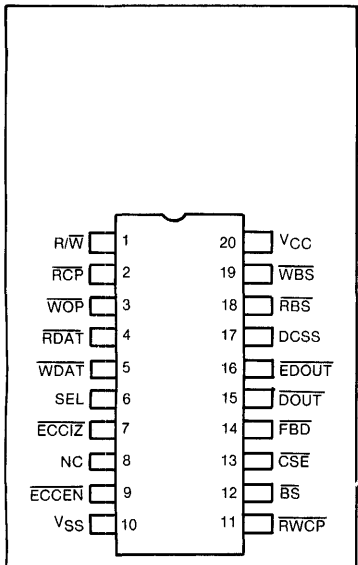
Western Digital
WD1100-06 ECC/CRC Logic

DESCRIPTION

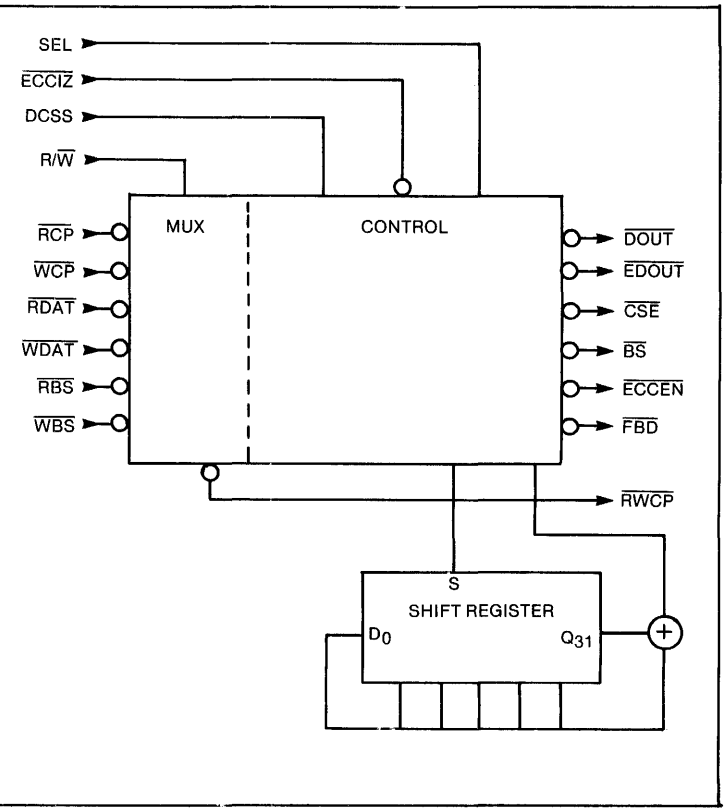
The WD1100-06 ECC/CRC logic chip gives the user of the WD1100 series of chips easy ECC or CRC implementation. With proper software, it will provide single burst correction up to 8 bits and double burst detection. The computer selected polynomial has been optimized for Winchester 5¼" and 8" drives with sector sizes up to 512 bytes.

FEATURES

- 32 bit computer selected polynomial
- Single burst correction up to 8 bits
- Multiple burst detection
- Programmable correction/detection span
- CRC or ECC software selectable
- Data transfer rates to 5.25 Mbits/sec
- Serial check/syndrome bit processing
- 128, 256, 512 byte sector sizes
- Single + 5V supply
- TTL, MOS compatible
- 20 pin DIP package



WD1100-06 Figure 1.
PIN CONNECTIONS



WD1100-06 Figure 2.
BLOCK DIAGRAM

WD1100-06 ECC/CRC DEVICE PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	READ/WRITE	R/W	Input line used to select the data, clock and CRC/ECC strobe during read/write operations. When low input signals WDAT, WCP, and WBS are selected. When high input signals RDAT, RCP, and RBS are selected.
2	READ CLOCK PULSE	RCP	Input pulse used by the internal shift registers to compute the 4 syndrome bytes.
3	WRITE CLOCK PULSE	WCP	Input pulse used by the internal shift registers to compute the 4 check bytes.
4	READ DATA	RDAT	Serial data input during a read operation.
5	WRITE DATA	WDAT	Serial data input during a write operation.
6	SELECT	SEL	This input is used to select either the CRC or the ECC polynomial for error detection/correction. SEL = 0 ECC polynomial selected. SEL = 1 CRC polynomial selected.
7	ECC INITIALIZE	ECCIZ	Input used to preset all the internal shift registers. Output lines FBD, EDOUT, DOUT, and CSE will be in their inactive high states. The first low going edge of either RDAT or WDAT signals the activation of all internal circuitry.
8	NO CONNECTION	N/C	No connection.
9	ECC ENABLE	ECCEN	When low, the ECC/CRC process is enabled. When high, this output signal indicates that the process is disabled.
10	GROUND	V_{SS}	Ground
11	READ/WRITE CLOCK PULSE	RWCP	Output clock pulse during read or write operations. The input clock pulses RCP and WCP are multiplexed on this output line for use by any support logic.
12	BYTE SYNC	BS	The input signals RBS and WBS are gated with the appropriate clocks and multiplexed as an output on the byte sync line. Normally not used by the user.
13	CLOCK SELECT ENABLE	CSE	When high, this output indicates that the device is in the process of computing the check/syndrome bytes and that EDOUT and DOUT lines contain data information. When low, the device puts CRC or ECC check/syndrome bits on the output data lines.
14	FEEDBACK	FBD	The feedback line to the shift registers is brought out as an output line for test purposes. Normally left open by the user.
15	DATA OUTPUT	DOUT	Output data line carries data or CRC/ECC information depending upon the state of DCSS.
16	EARLY DATA OUTPUT	EDOUT	Unlatched output data line available 1 clock period earlier than DOUT.

WD1100-06 ECC/CRC PIN DESCRIPTION (CONTINUED)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
17	DATA/CHECK SYNDROME SELECT	DCSS	Data or check/syndrome select input line. When high, data is output on the data lines; when low, CRC or check syndrome bits are output depending upon which polynomial is selected. DCSS goes low sometime between the last and the next to the last data byte transferred to/from the disk provided all set-up and hold-times have been met. DCSS must stay low for at least 2 byte times when the CRC polynomial selected and it must stay low for at least 4 byte times if the ECC polynomial is selected.
18	$\overline{\text{READ BYTE}}$	$\overline{\text{RBS}}$	Input used to latch the state of DCSS during the read mode.
19	$\overline{\text{WRITE BYTE}}$	$\overline{\text{WBS}}$	Input used to latch the state of DCSS during the write mode.
20	+5V	V_{CC}	+5V ± 10%

DEVICE DESCRIPTION

To ensure correct operation of the WD1100-06 device, the $\overline{\text{ECCIZ}}$ line is strobed to preset the polynomial generator shift register, and reset the Data/Check-Syndrome select flip-flop. The 32 bit shift register string is preset to avoid all zero check bytes. The DCSS line is held high and appropriate signals are then applied to the rest of the inputs. Since most disk media use an Address mark of A1 (or M.S.B. set), advantage is taken of this feature to start off the ECC/CRC calculation on the data/ID fields automatically. The first active low going edge on the input data lines releases the internal SET Flip-Flop. The $\overline{\text{ECCEN}}$ output line is set low indicating that the internal circuitry is ready to begin the computation of the ECC/CRC bytes. Immediately following the Address mark, data is supplied in a serial fashion.

Sometime before the last byte of data and after the next to the last byte of data is transferred through this device, the DCSS line is set low. Since data is generally serialized/deserialized before/after processing by the WD1100-06 device, the byte-sync pulses can be easily obtained from those devices marking the byte boundaries. The byte-sync pulses are internally ANDED with the $\overline{\text{RWCP}}$ line to ensure the smooth transition of check/syndrome bytes on the $\overline{\text{DOUT}}$ output line only after the last bit of data has been entered into the device. A one bit time delay through a D Flip-Flop has been added on the $\overline{\text{DOUT}}$ line to deglitch this output line.

During a WRITE operation, the input data stream is divided by the polynomial $X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^2 + 1$ and the 32 bit remainder obtained is used as the 4 check syndrome bytes. If the syndrome is zero, no errors occurred. Otherwise, the non-zero syndrome is used by a software algorithm to compute the displacement and the error vector within the bad sector. To protect the integrity of the ID field only a CRC check should be performed over this field. No attempt ought to be made to correct data in the ID field. The CRC polynomial implemented is the standard CCITT ($X^{16} + X^{12} + X^5 + 1$.) Although either polynomial may be used for both fields, the use of the CRC polynomial for the ID fields is recommended since it only requires 2 bytes instead of 4.

POLYNOMIAL SELECTION

For disk media, polynomial selection has a significant influence on data accuracy. Fire code polynomials have been widely used on OEM disk controllers, but provide less accuracy than properly selected computer generated codes.

For fixed, guaranteed correction and detection spans, data accuracy may be highly dependent on polynomial selection. Some polynomials, fire codes for example, are particularly susceptible to miscorrection on common disk type errors, while others, computer generated polynomials for example, can be selected to be less susceptible. Computer generated codes do not have the pattern sensitivity of the fire code and the miscorrection patterns are more random in nature.

More than 20,000 computer generated random polynomials of degree 32, each with 8 feedback terms, were evaluated in order to find the polynomial described in this specification.

SELECTING THE CORRECTION SPAN

The code described in this document can be used to correct up to 8 bits.

Any correction span from 1 to 8 may be selected. However, for best data accuracy, the lowest correction span should be used that meets the correction

requirements for the disk drives supported.

For most Winchester media, a 5 bit correction span is adequate.

The correction span may have to be longer if the drive uses a read/write modulation method that maps a single media bit in error into several decoded bits in error. Examples of read/write modulation methods of this type would be GCR and 2,7 code.

PROPERTIES OF THE POLYNOMIAL

The following polynomial was computer selected for insensitivity to short double bursts, good detection span and 8 feedback terms.

Forward polynomial is:
$X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^6 + X^2 + 0$

Reciprocal polynomial is:
$X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + x^{13} + X^6 + X^4 + X^0$

Properties*

1. Maximum record length (r) = 526x8 bits (including check bits)
2. Maximum correction span (b) = 8 bits
3. Degree of polynomial (m) = 32
4. Single burst detection span without correction = 32 bits. (Detection span when the code is used for detection only)
5. Single burst detection span with correction (d) — (Detection span when the code is used for correction)
   - = 19 bits for b = 5 and r = 526x8
   - = 14 bits for b = 8 and r = 526x8
   - = 20 bits for b = 5 and r = 270x8
   - = 14 bits for b = 8 and r + 270x8
6. Double burst detection span without correction — (Doule burst detection span when code is used for correction)
   - = 3 bits for b = 5 and r = 526x8
   - = 2 bits for b = 8 and r = 526x8
   - = 4 bits for b = 5 and r = 270x8
   - = 2 bits for b = 8 and r = 270x8
7. Non-detection probability = 2.3 E-10.
8. Miscorrection probability—
   - = 1.57 E-5 for b = 5 and r = 526x8
   - = 1.25 E-4 for b = 8 and r = 526x8
   - = 8.00 E-6 for b = 5 and r = 270x8
   - = 6.40 E-5 for b = 8 and r = 270x8

NOTE:*
You should not use this polynomial for a record length or correction span beyond the maximum specified above.

SOFTWARE REQUIREMENTS

The software algorithm, developed by the user, uses the syndrome to detect an error, generate a correction pattern and a displacement vector or to determine if uncorrectable. In the correction algorithm, a simulated shift register is used to implement the reciprocal polynomial. The simulated shift register is loaded with the syndrome and shifted until a correctable pattern is found or the error is determined to be uncorrectable. Both forward and reverse displacements are computed.

Either the serial or the parallel algorithm may be implemented by the user. In almost all cases the serial software algorithm is the most applicable. Additionally, 1K of table space is required if the parallel software algorithm is selected. It is assumed that the highest order bit of a byte is serialized and deserialized first.

CORRECTION TIME PERFORMANCE

All real time operations are performed with error correction hardware. The software algorithms used get involved only after an error has been detected.

The following correction times are for a serial type algorithm such as that used on the WD1001:

a) Standard microprocessor = 30 to 60 milliseconds
b) Bit slice = 6 to 12 milliseconds
c) 8X300 (used on WD1001) = 15 to 30 milliseconds

DATA ACCURACY

ERP (Error Recovery Procedure) strategies have a significant influence on data accuracy. An ERP strategy requires data to be re-read before applying correction and results in much better data accuracy. The WD1001 employs such a strategy. This strategy reduces the possibility of passing undetected erroneous data by rereading until the error goes away, or until there has been a consistant error syndrome over two previous rereads.

Another technique that can be used to give data a higher probability of recovery is write check: read back after write. Since write check affects performance, it should be optional. Alternate sector assignment and defect skipping are some of the other techniques that may be implemented by the user if so desired.

SELF-CHECKING WITH MICROCODE

Periodic microcode and/or software checking is another approach that can be used to limit the amount of undetected erroneous data transferred in case of an ECC circuit failure. Microcode or software diagnostics could be run on subsystem power up and during idle times. These diagnostics would force ECC errors and check for the proper syndrome and proper decoding of the syndrome by the correction routine of the operational microcode.

To do this, simply use a long bit in the READ and WRITE commands to the disk. This bit can then be used to suppress the transfer of check/syndrome bytes on the output data line by letting the DCSS line stay high during ECC TIME. The complete procedure is summarized below.

1. WRITE: Pass all data to the disk and generate 4 check bytes at the end of the data field.
2. READLONG: Do not generate the syndrome, instead copy the 4 check bytes as data and pass them unaltered to the host. Now the host may induce errors anywhere in the data stream as long as the induced error does not exceed the correction span of the polynomial generator.
3. WRITELONG: Write the data and check bytes supplied by the host to the disk. Prevent WD1100-06 from generating check bits by not asserting DCSS during transfer. No check bytes will be recorded.
4. READ: Read data and generate the syndrome in a normal manner. The software algorithm can now be invoked to correct the induced error.

To aid in detection of certain hardware failures, it is desirable to have non-zero check bytes for an all zeros record. This feature has been incorporated into the circuit defined in this specification.

SPECIFICATIONS

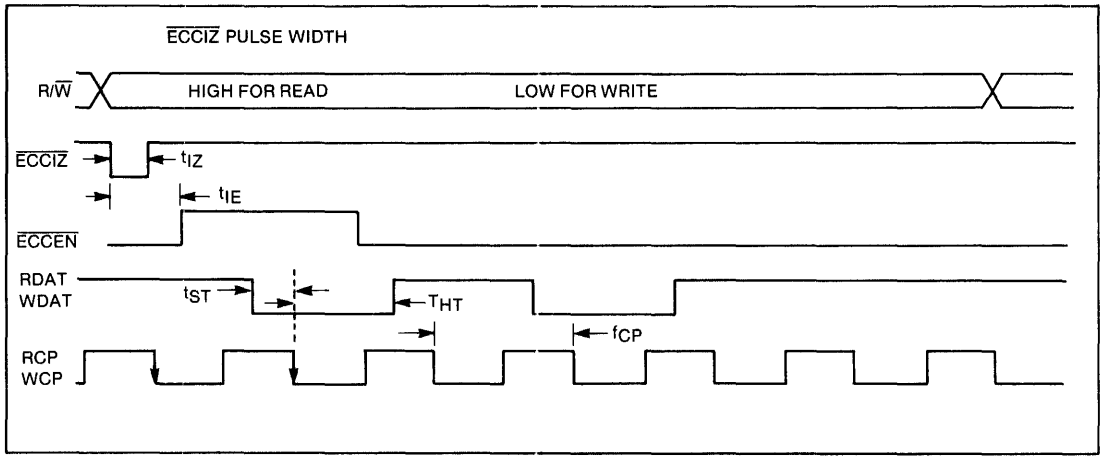
ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under bias ..... 0°C to 50°C
Voltage on any pin with
respect to V_{SS} ..... −0.2V to +7.0V
Power dissipation ..... 1 Watt
Storage Temperature
Plastic ..... −55°C to +125°C
Ceramic ..... −55°C to +150°C

NOTE:
Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current		75	150	mA	All outputs open



AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS}

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
f_{CP}	Clock Frequency			5.25	MHZ	
t_{IZ}	$\overline{ECCIZ}$ Pulse Width	50			nSec	
t_{IE}	$\overline{ECCIZ}$ ↓ to $\overline{ECCEN}$ ↑			100	nSec	
t_{ST}	R/WDAT Setup Time	50		1 Clock Period	nSec	
t_{HT}	R/WDAT Hold Time	0			nSec	

See page 725 for ordering information.

PRELIMINARY

WD1100-07

Western Digital
WD1100-07 Host Interface Logic

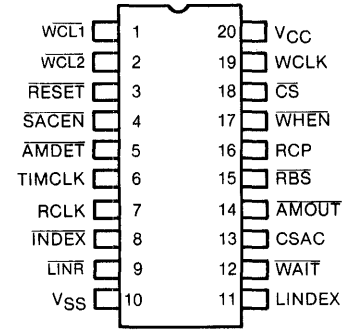
DESCRIPTION

The WD1100-07 Host Interface Logic chip simplifies the design of a Winchester Hard Disk Controller using the WD1100 chip series. It does this by performing logic functions that would otherwise require considerable discrete logic. Additionally, there are signals provided for ECC implementation.

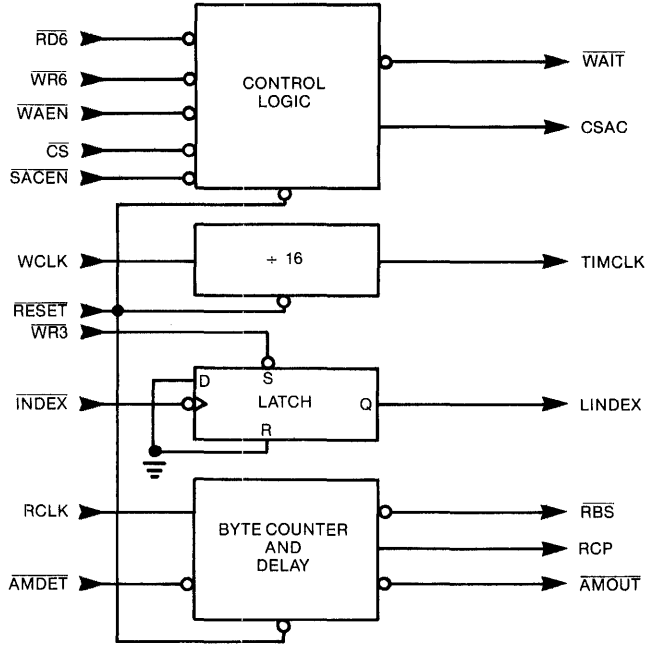
The WD1100-07 is implemented in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic Dual-in-Line package.

FEATURES

- SINGLE +5V SUPPLY
- WAIT SIGNAL GENERATION
- TIMING CLOCK GENERATION
- INDEX PROPAGATION
- CARD ACCESS CONTROL
- COMPLIMENTS ECC ARCHITECTURE
- 20 PIN DIP PACKAGE



WD1100-07 Figure 1.
PIN CONNECTIONS



WD1100-07 Figure 2.
BLOCK DIAGRAM

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	WAIT CLEAR 1	$\overline{WCL1}$	This input presets a WAIT latch to a non-WAIT condition on the falling edge.
2	WAIT CLEAR 2	$\overline{WCL2}$	This input presets a WAIT latch to a non-WAIT condition on the falling edge.
3	RESET	$\overline{RESET}$	An input used to set TIMCLK & reset $\overline{WAIT}$, $\overline{AMOUT}$ and $\overline{RBS}$.
4	SELECT ADDRESS ENABLE	$\overline{SACEN}$	This is an input signal that is used to enable card select for host access.
5	ADDRESS MARK DETECT	$\overline{AMDET}$	An input that must go active when a DATA = A1(HEX) or clock = 0A(HEX) pattern is detected in the data stream
6	TIMING CLOCK	TIMCLK	An output used to provide reference timing signals to SA100 type drives
7	READ CLOCK	RCLK	This input, the same as used to clock in data and clocks to the AM detector, is used to produce $\overline{AMOUT}$.
8	INDEX PULSE	$\overline{INDEX}$	This input is provided by the drive once each revolution of the disk
9	LINDEX RESET	$\overline{LINR}$	An input used to reset LINDEX.
10	GROUND	V_{SS}	Ground
11	LATCHED INDEX	LINDEX	An output that is $\overline{INDEX}$ delayed by one clock time.
12	WAIT	$\overline{WAIT}$	This output goes true when controller is internally accessing data or has not accepted data from the host during a WRITE.
13	CARD SELECT ADDRESS	CSAC	An output that is the result of $\overline{CS}$ qualified with $\overline{SACEN}$.
14	ADDRESS MARK DELAYED OUTPUT	$\overline{AMOUT}$	This output is a delayed version of $\overline{AMDET}$.
15	READ BYTE STROBE	$\overline{RBS}$	This output strobes once for each byte of READ data. Initialized by $\overline{AMDET}$.
16	READ CLOCK PULSE	RCP	This output is delayed from RCLK through propagation. Not normally used.
17	WAIT ENABLE	$\overline{WAEN}$	An input that is used to enable the internal WAIT circuitry.
18	CARD SELECT	$\overline{CS}$	An input from host that selects controller.
19	WRITE CLOCK	WCLK	This input is used to produce TIMCLK on low to high transitions.
20	+5VDC	V_{CC}	+5V ± 10%

DEVICE DESCRIPTION

Upon power up or reset, $\overline{WAIT}$, $\overline{AMOUT}$, and $\overline{RBS}$ are reset and TIMCLK is set. This is the only interactive signal between the four sections of the chip. Each section will be described separately.

Control Logic

This section provides $\overline{WAIT}$ (pin 12) and CSAC (pin 13). $\overline{WAIT}$ is set in its active low state when $\overline{WAEN}$ (pin 17) is active low by the falling edge of $\overline{CS}$ (pin 18). $\overline{WAIT}$ is reset by the falling edge of either $\overline{WCL1}$ or $\overline{WCL2}$ depending on whether in a read or write mode. CSAC (pin 13) is enabled by setting $\overline{SACEN}$ (pin 4) low after $\overline{WAIT}$ has been enabled. CSAC is reset by $\overline{WCL1}$ or $\overline{WCL2}$.

Timing Clock

TIMCLK (pin 6) is a divided by sixteen version of WCLK (pin 19). It is used with SA1000 type drives.

Index Pulse

Lindex (pin 11) is a delayed version of $\overline{INDEX}$ (pin 8). It remains high until reset by $\overline{LINR}$ (pin 9).

Read Byte Sync

$\overline{RBS}$ (pin 15) will go true on the eighth negative going transition of RCLK (pin 7) after $\overline{AMDET}$ (pin 5) goes true. $\overline{RBS}$ will remain true for one clock cycle.

Read Clock Pulse

RCP (pin 16) is a delayed version of RCLK and is normally left open by the user.

Address Mark Delayed Output

$\overline{AMOUT}$ (pin 14) is the same as $\overline{AMDET}$ delayed by two clock times.

These circuits were developed to work with the other chips in the WD1100 series. They are used on the WD1001 the timing relationships must be observed.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias ..... 0°C to 50°C
Voltage on any pin with
respect to V_{SS} ..... −0.2V to +7.0V
Power Dissipation..... 1 Watt
Storage Temperature Plastic −55°C to +125°C
Ceramic −55°C to +150°C

NOTE:
Maximum ratings indicate operation when permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

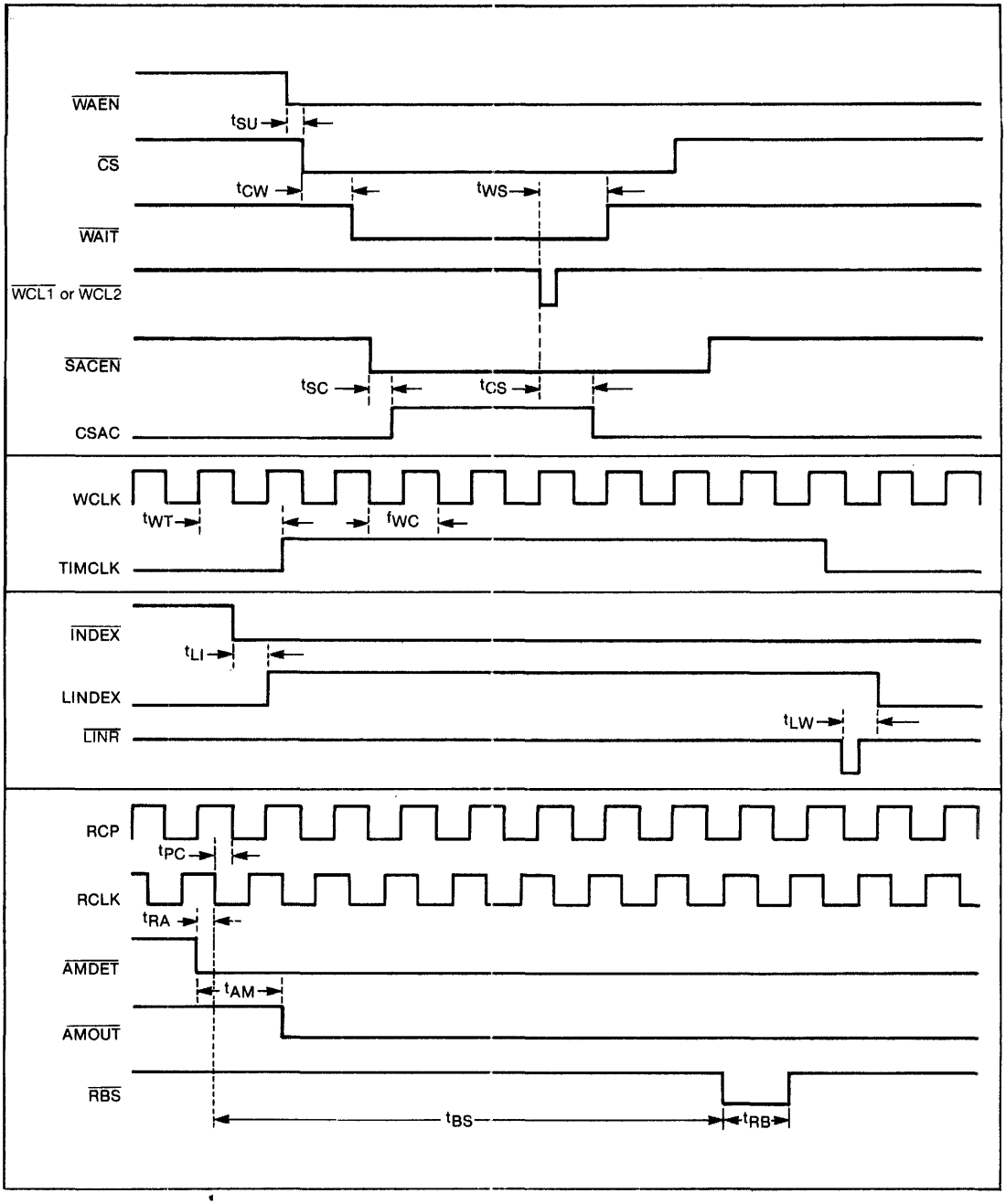
DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
f_{WC}	WCLK FREQUENCY			5.25	MHZ	
t_{CW}	CS↓ to WAIT↓		50	160	nSec	
t_{WS}	WCL1↓ or WCL2↓ to WAIT↑		170	195	nSec	
t_{SU}	$\overline{WAEN}$ Setup Time	50			nSec	
t_{SC}	SACEN↓ to CSAC↑		5	70	nSec	WAIT TRUE
t_{CS}	WCL1↓ or WCL2↓ to CSAC↓		45	155	nSec	WAIT TRUE
t_{WT}	WCLK↑ to TIMCLK↑			250	nSec	
t_{LI}	INDEX↓ to LINDEX↑		50	100	nSec	
t_{LW}	LINR↓ to LINDEX↓		30	100	nSec	
t_{PC}	RCLK↓ to RCP↓		30	75	nSec	
t_{RA}	AMDET Setup Time	30	50		nSec	
t_{AM}	AMDET↓ to AMOUT↓		2 CLOCK CYCLES	2 CLOCK CYCLES +45	nSec	
t_{BS}	RCLK↓ to RBS↓		8 CLOCK CYCLES	8 CLOCK CYCLES +165	nSec	
t_{RB}	$\overline{RBS}$ Period		1 CLOCK CYCLE			

[1] NOTE: Typical Values are for T_A = 25°C and V_{CC} = +5V



See page 725 for ordering information.

PRELIMINARY

WD1100-09

Western Digital
WD1100-09 Data Separator Support Logic

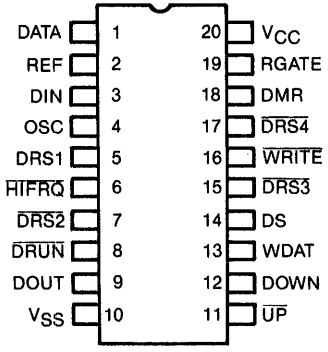
GENERAL DESCRIPTION

The WD1100-09 Data Separator Support Logic, when used with the other chips in the WD1100 series, greatly reduces the external discrete logic required to design a Winchester hard disk data separator. The chip provides the pump signals to an external error amplifier, control signals to an internal bus and a special drive selection signal also to an internal bus.

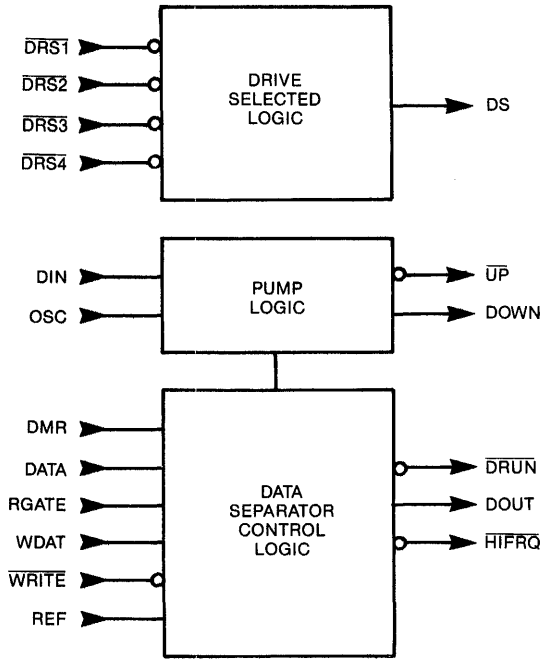
The WD1100-09 is fabricated in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic package.

FEATURES

- SINGLE +5V SUPPLY
- DRUN GENERATION
- DATA SEPARATION CONTROL SIGNALS
- 20 PIN DIP PACKAGE



WD1100-09 Figure 1.
PIN CONNECTIONS



WD1100-09 Figure 2.
BLOCK DIAGRAM

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	READ DATA	DATA	Input that is used in $\overline{\text{DRUN}}$ generation.
2	REFERENCE	REF	An input that is 2 times the data rate that keeps the VCO on center frequency during non-read times.
3	DELAYED DATA IN	DIN	This input is a delayed version of DOUT. An external delay line is used. The signals are compared to provide pumps.
4	OSCILLATOR	OSC	An input from the external VCO that is used in pump development
5, 7, 15, 17	$\overline{\text{DRIVE SELECT}}$ 1- $\overline{\text{DRIVE SELECT}}$ 4	$\overline{\text{DRS1}}$- $\overline{\text{DRS4}}$	Input signals indicating which drive has been selected.
6	$\overline{\text{HIGH FREQUENCY}}$	$\overline{\text{HIFRQ}}$	Output to controller microprocessor that indicates 16 ones or zeros have been entered on the DATA line.
8	$\overline{\text{DATA RUNNING}}$	$\overline{\text{DRUN}}$	Output that indicates to the controller microprocessor the completion of 16 ones or zeros on the data line. Used to switch from REF to DATA via firmware.
9	DATA OUT	DOUT	Output data line. Can be REF or DATA or WDATA depending on the condition of $\overline{\text{WRITE}}$, $\overline{\text{DMR}}$ and RGATE.
10	GROUND	V_{SS}	Ground
11	$\overline{\text{UP PUMP}}$	$\overline{\text{UP}}$	An output that indicates REF is leading DATA. Goes to error amp. Open collector.
12	DOWN PUMP	DOWN	An output that indicates DATA is leading REF. Goes to error amp. Open collector.
13	WRITE DATA	WDATA	MFM Write data input. Output appears at DOUT.
14	DRIVE SELECTED	DS	An output that indicates that one of four drives have been selected.
16	$\overline{\text{WRITE MODE}}$	$\overline{\text{WRITE}}$	This input is active during a write operation and enables WDAT.
18	DATA MASTER RESET	DMR	This input is used to provide time-out for $\overline{\text{DRUN}}$ and $\overline{\text{HIFRQ}}$ in the event that 16 ones or zeros are not present.
19	READ GATE	RGATE	This input, usually provided by the controller microprocessor, places chip in read mode.
20	+5VDC	V_{CC}	+5VDC ± 10%

DEVICE DESCRIPTION

The WD1100-09 is divided into three sections. Each section will be described separately.

Drive Select Logic

DS (pin 14) will go active high if any input $\overline{\text{DSR1}}$ through $\overline{\text{DRS4}}$ (pins 5, 7, 15, 17) are active low.

Pump Logic

Internal logic causes the $\overline{\text{UP}}$ (pin 11) and the DOWN (pin 12) to be set, initially to their inactive states. DIN (pin 3) is the delayed data developed by passing DOUT through a delay line. OSC (pin 4) is the output of the data separator VCO. Whichever reaches the pump logic first will determine whether UP PUMP or DOWN PUMP is produced. These signals are then sent to an external error amplifier and used for VCO correction. During a write, the DIN must be locked to a crystal oscillator clock and will hold the VCO on frequency.

Data Separator Control Logic

Read Mode

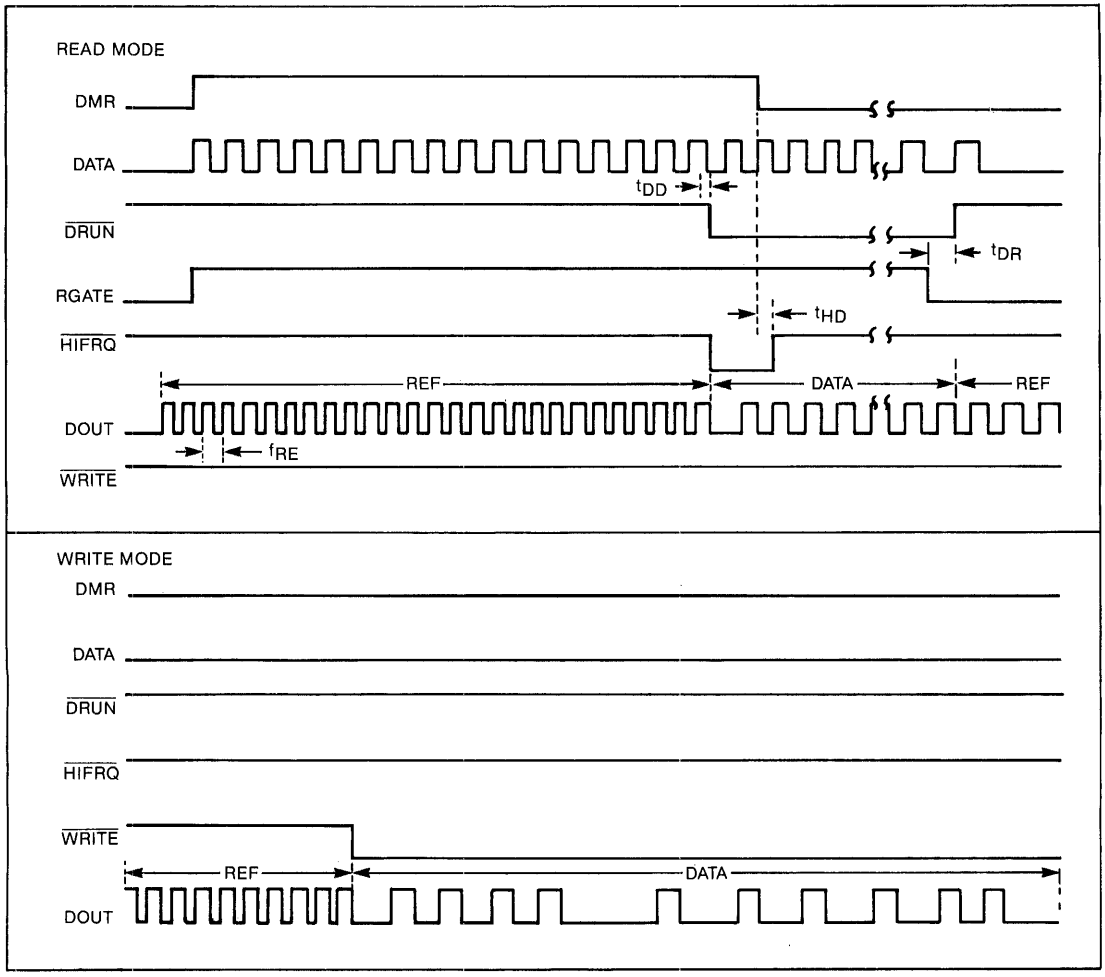
In order to prevent the external VCO from locking onto a harmonic of its operating frequency, REF (pin 2) is provided with a signal twice the data rate that is crystal controlled. With $\overline{\text{WRITE}}$ (pin 6) and RGATE (pin 19) inactive, this signal will appear at DOUT (pin 9). This signal is applied to the pump logic (see above).

The switching function is initiated immediately after RGATE goes true. DMR (pin 18) will be set active as a result of high frequency pulses applied to an external one shot whose pulse width is such that its output is a single stretched pulse. The high frequency pulses are applied to the DATA (pin 1) line and after 16 consecutive pulses, $\overline{\text{DRUN}}$ (pin 8) and $\overline{\text{HIFRQ}}$ (pin 6)

go true. At this point REF is switched out and the DATA stream is switched in and appears at DOUT. DRUN is reset when RGATE goes inactive and HIFRQ goes inactive when DMR goes inactive.

Write Mode

When WRITE (pin 16) goes active, REF is switched out and WDAT (pin 13) will appear at DOUT. Since WDAT is a crystal controlled signal (usually the MFM write data); the VCO is held locked and will not drift (see pump logic above).



AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{DD}	DATA↓ to DRUN↓			170	nSec	
t_{DR}	RGATE↓ to DRUN↑			90	nSec	
t_{HD}	DMR↓ to HIFRQ↑			90	nSec	
f_{RE}	REF frequency		2 TIMES DATA RATE	10	MHz	

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . . . . 0°C to 50°C
Voltage on any pin with
respect to V_{SS} . . . . . −0.2V to +7.0V
Power Dissipation . . . . . 1 Watt
Storage Temperature Plastic −55°C to +125°C
Ceramic −55°C to +150°C

NOTE:
Maximum ratings indicate operation when permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

NOTE: $\overline{UP}$ and DOWN are open collector outputs and provide 12mA I_{OL} @ .5V.

See page 725 for ordering information.

Printed in U.S.A.

ADVANCE INFORMATION

WD1010 Winchester Disk Controller

FEATURES

- Compatible with most 8- and 16-bit processors
- Data rate up to 5 Mbits per second
- Multiple sector read/write commands
- Unlimited interleave capability
- Automatic formatting
- Software selectable sector size (128, 256, 512, or 1024 bytes per sector)
- CRC generation/verification
- Automatic retries on all errors
- Automatic restore on seek errors
- Single +5V supply
- Provision for external ECC capability

APPLICATIONS

- Seagate ST506, ST512
- Shugart SA1000, SA1100, SA600
- Tandon 600 Series
- Texas Instruments 506
- RMS 500 Series
- Quantum Q2000 Series
- Miniscribe

. . . and others

DESCRIPTION

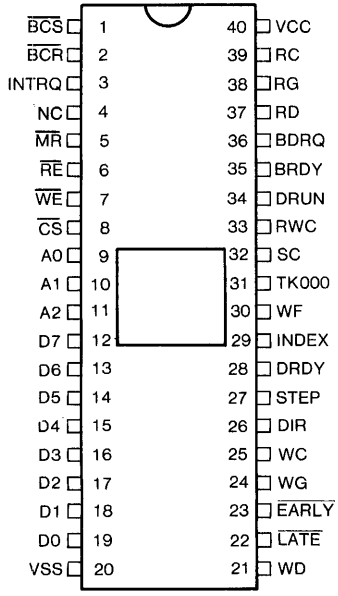
The WD1010 is a MOS/LSI device designed for use with the drives listed above as well as other drives compatible with the SA1000 or ST506 interface. The controller requires only a single +5 volts supply. It is designed to operate with an external sector buffer memory and to interface directly with TTL logic.

The WD1010 is fabricated in NMOS silicon-gate technology and is available in a 40-pin, Dual-in-line ceramic or plastic package.

FUNCTIONAL DESCRIPTION

The WD1010 is software compatible with the WD1000 controller board. Programming is very similar to that of the Western Digital FD179X floppy disk controller.

Data bytes are transferred to or from the buffer every 1.6μsec., with a 5Mbit/sec drive. The buffer may be either the Western Digital WD1510 128x9 FIFO memory (Fig. 1) or a combination of a 256x8 static RAM and a 9 bit resettable counter (Fig. 2). The WD1010 generates control signals to minimize external gating. Buffer to processor transfers are made via programmed I/O or DMA. The controller also generates handshake signals to control DMA operations for multiple sector transfers. The WD1010 interfaces to the Western Digital DM1883 and other DMA controllers.



PIN CONNECTIONS

TABLE 1. INTERFACE SIGNALS

PIN NUMBER	SYMBOL	PIN NAME	FUNCTION
12-19	D7-D0	Data 7 - Data 0	Eight bit bidirectional bus used for transfer of commands, status, and data.
6	$\overline{RE}$	READ ENABLE	Tristate bidirectional line, used as an input for reading the task register and an output when WD1010 is reading the buffer.
7	$\overline{WE}$	WRITE ENABLE	Tristate bidirectional line used as an input for writing into the task register and as an output when the WD1010 is writing to the buffer.
9-11	A0-A2	ADDRESS 0 - ADDRESS 2	These three inputs select the register to receive/transmit data on D0-D7.
8	$\overline{CS}$	CHIP SELECT	A logic low on this input enables both $\overline{WE}$ and $\overline{RE}$ signals.
3	INTRQ	INTERRUPT REQUEST	Active high output which is set to a logic high in the completion of any command.
5	$\overline{MR}$	MASTER RESET	A logic low in this input will initialize all internal logic.
1	$\overline{BCS}$	BUFFER CHIP SELECT	Active low output used to enable reading or writing of the external sector buffer.
35	BRDY	BUFFER READY	This input is used to inform the controller that the sector buffer is full or empty.
2	$\overline{BCR}$	BUFFER COUNTER RESET	Active low output that is strobed by the WD1010 prior to read/write operations.
36	BDRQ	BUFFER DATA REQUEST	This output is set to initiate data transfers to/from the sector buffer.
40	V_{CC}	+ 5 volt	$+5V \pm 5\%$ Power supply input.
20	V_{SS}	GROUND	Ground.
4	NC	NO CONNECTION	This pin must be left open by the user.
21	WD	WRITE DATA	This output contains the MFM clock and data pulses to be written on the disk.
25	WC	WRITE CLOCK	4.34 or 5.0 MHz clock input used to derive all internal write timing.
24	WG	WRITE GATE	This output is set to a logic high before writing is to be performed on the disk.
23, 22	$\overline{EARLY}$, $\overline{LATE}$	EARLY, LATE	Precompensation outputs used to delay the WD pulses externally.
37	RD	READ DATA	Data input from the Drive. Both MFM clocks and data pulses are entered on this pin.
39	RC	READ CLOCK	A normal square wave clock input derived from the external data recovery circuits.
38	RG	READ GATE	This output is set to a logic high when data is being inspected from the disk.
39	DRUN	DATA RUN	This input informs the WD1010 when a field of one's or zeroes have been detected.
27	STEP	STEP PULSE	This output generates a pulse for the stepping motor.
26	DIR	DIRECTION	This output determines the direction of the stepping motor.
28	DRDY	DRIVE READY	This input must be at a logic high in order for commands to execute.
30	WF	WRITE FAULT	An error input to the WD1010 which indicates a fault condition at the drive.
31	TK000	TRACK 000	An input to the WD1010 which indicates that the R/W heads are positioned over the outermost cylinder.

TABLE 1. INTERFACE SIGNALS

PIN NUMBER	SYMBOL	PIN NAME	FUNCTION
29	INDEX	INDEX PULSE	A logic high on this input informs the WD1010 when the index hole has been encountered.
33	RWC	REDUCED WRITE CURRENT	This output can be programmed to reduce write current on a selected starting cylinder.
32	SC	SEEK COMPLETE	This input informs the WD1010 when head settling time has expired.

PROCESSOR INTERFACE DESCRIPTION

The WD1010 controller interfaces to a host or I/O processor via an 8 bit bidirectional data bus. The buffer memory is also connected to the data bus. The WD1010 is designed for use with buffer memory and external bus transceivers. One anticipated system configuration is shown in Figure 1. In this system, the processor starts a disk operation by writing task information into the register file in the controller. The task information includes the disk cylinder, head, sector numbers, drive number, track number for start of write precompensation, sector size, and number of sectors to be transferred. After the task information has been written, the processor writes the command into the command register. In the case of a write sector command, the processor can then read the controller status register to inspect the buffer data request flag, and write data into the buffer memory. When the buffer becomes full, it activates the BRDY input of the controller. The controller then deactivates the buffer data request (BDRQ) line and activates the $\overline{BCS}$ line. The buffer chip select ($\overline{BCS}$) line is used both for buffer memory control and for disabling the data bus, $\overline{RE}$ and $\overline{WE}$ buffers. The controller thus has a direct bus to the buffer memory which is isolated from the processor data bus. When the buffered data is transferred to disk and the buffer memory is empty, the controller enables the tristate buffers, thus reconnecting the two busses. The processor can then write more data into the buffer memory.

The WD1010 disk controller generates control signals for RAM-counter control, data bus control, ECC processor and DMA control.

TABLE 2. TASK REGISTER FILE

A2	A1	A0	READ	WRITE
0	0	0	Data	Data
0	0	1	Error Flags	Write Precomp Cyl.
0	1	0	Sector Count	Sector Count
0	1	1	Sector Number	Sector Number
1	0	0	Cylinder No. Low	Cylinder No. Low
1	0	1	Cylinder No. High	Cylinder No. High
1	1	0	SDH	SDH
1	1	1	Status	Command

TABLE 3. SDH REGISTER

SECTOR EXTENSION	SECTOR SIZE		DRIVE* NUMBER		HEAD* NUMBER		
BIT 7	6	5	4	3	2	1	0
1 = ECC 0 = CRC	1 0 0 1	1 0 1 0	128 byte data field 256 byte data field 512 byte data field 1024 byte data field				

*Drive Number and Head Number must be externally decoded and latched.

DRIVE INTERFACE DESCRIPTION

The WD1010 disk controller is designed to interface to SA1000 Winchester disk drives. Winchester drives with similar interfaces, such as the Seagate Technology ST506, can also be controlled.

The WD1010 contains MFM encoder/decoder, address mark detector, and high speed shift register circuitry. Signals are provided to control write precompensation and write splice avoidance. External circuitry must provide a phase locked MFM read clock and high frequency detection. Figure 1 shows a typical controller-drive interface for a system with two Winchester disk drives.

WD1010 inputs are TTL compatible unless otherwise noted. WD1010 outputs will drive one TTL unit load.

STATUS BIT DESCRIPTION

Busy — Active when controller is accessing the disk. Activated by start of command (writing into command register). Deactivated at end of all except read sector. For read sector, Busy is deactivated when a sector of data has been transferred to buffer.

Drive Ready — Normally reflects the state of DRDY pin. After an error interrupt, the state of DRDY is frozen until the status register is read. The DRDY bit then reflects the state of the DRDY pin. An interrupt is generated when reset.

Write Fault — Reflects the state of the WF pin. An interrupt is generated when set.

Seek Complete — Reflects the state of the SC pin.

Data Request — Reflects the state of the BDRQ pin. When active, indicates that a buffer data transfer is desired. The data request flag is used for programmed I/O while the BDRQ pin is used for DMA controlled I/O.

Command in Progress — Indicates that a command is in progress.

Error — Indicates that a bit in the error register has been set.

ERROR BIT DESCRIPTION

Bad Block — A bad block address mark has been detected when trying to read or write that sector.

Data Field CRC Error — An error in the data field has been detected. The sector can be re-read to attempt recovery from a soft error. The data contained in the buffer can be read but contains errors.

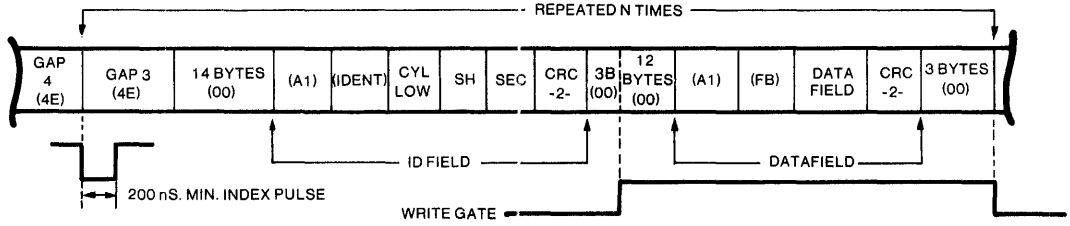
ID Not Found — Occurs when cylinder, head, sector, or size parameters cannot be found after 16 index pulses have been encountered.

TK000 Error — Occurs when track 0 not found in a Restore command after 1024 stepping pulses.

Aborted Command — Set if command was started and one of the following conditions occurred:

1. Drive not ready
2. Write fault
3. Seek complete not active within 16 index pulses
4. Illegal command code

Data AM Not Found — During a read command, the ID field for the desired sector has been found, but the data field address mark was not found. The data AM should be found within 15 bytes after the ID field. Refer to Figure 3 for track format.



NOTE:

1) When MSB of head byte = 1, bad block is detected.
2) Write Gate turn-on is 3 bytes after the ID field's CRC bytes.
3) Write Gate turn-off is 3 bytes after the Data Field's CRC bytes.
4) 12 bytes of zeroes are re-written on a Data Field update.
5) The 2 LSB's of the IDENT byte are used for Cylinder high. These values are:
   FF = 0 to 255 cylinders
   FF = 256 to 511 cylinders
   FC = 512 to 767 cylinders
   FD 768 to 1023 cylinders
6) GAP 3 length is programmable and may range from 3 bytes to 255 bytes.

FIGURE 3
TRACK FORMAT

TABLE 4. STATUS/ERROR REGISTERS

BIT	STATUS REGISTER	ERROR REGISTER
MSB 7	BUSY	Bad Block
6	DRIVE READY	Data Field CRC
5	WRITE FAULT	Reserved (= 0)
4	SEEK COMPLETE	ID Not Found
3	DATA REQUEST	Reserved (= 0)
2	RESERVED (= 0)	Aborted Command
1	COMMAND IN PROGRESS	TK000 Error
LSB 0	ERROR	Data AM Not Found

TABLE 5. COMMAND REGISTER

COMMAND	MSB 7	6	5	4	3	2	1	0
RESTORE	0	0	0	1	R3	R2	R1	R0
SEEK	0	1	1	1	R3	R2	R1	R0
READ SECTOR	0	0	1	0	D	M	0	0
WRITE SECTOR	0	0	1	1	0	M	0	0
SCAN ID	0	1	0	0	0	0	0	0
WRITE FORMAT	0	1	0	1	0	0	0	0

D = 1 for DMA; 0 for Programmed I/O
M = 1 for multiple sector read or write

R3 R2 R1 R0 =
- 0000 : Step time = 20 us
- 0001 : Step time = .5 ms
- 0010 : Step time = 1.0 ms
- 0011 : Step time = 1.5 ms
- 1111 : Step time = 7.5 ms

for 5 MHz write clock

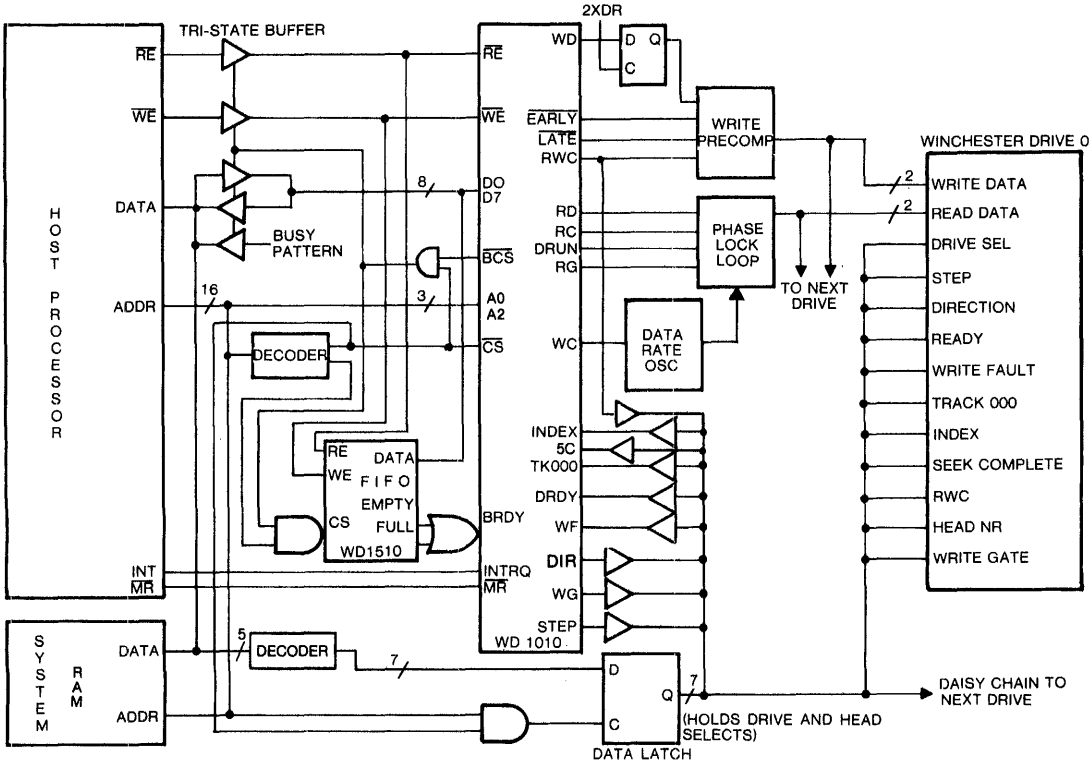


FIGURE 1.

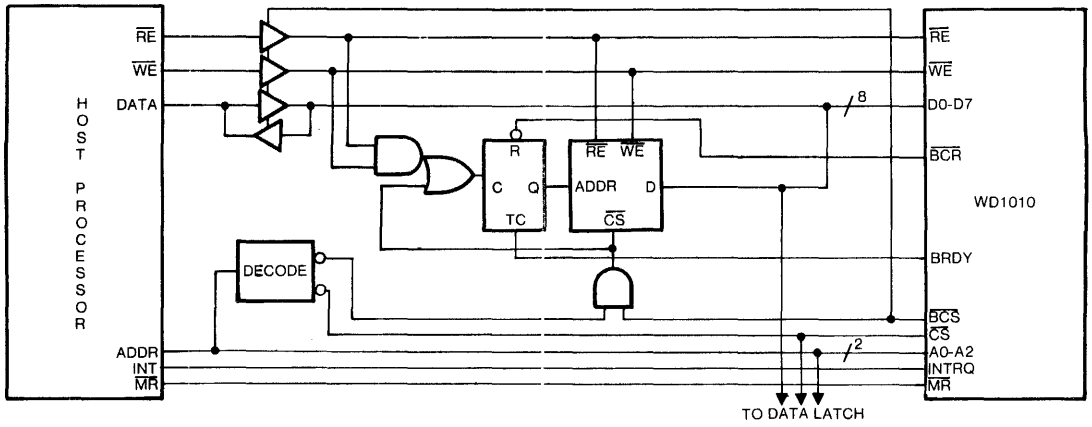


FIGURE 2.

See page 725 for ordering information.

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ADVANCE INFORMATION

WD1011 Winchester Data Separator Device

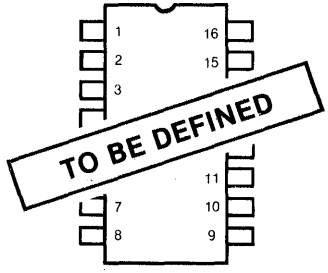
FEATURES

- 4.34 OR 5.0 MBIT/SEC DATA RATE
- INTERNAL CRYSTAL OSCILLATOR
- SINGLE +5V SUPPLY
- FM OR MFM OPERATION
- COMPATIBLE WITH THE WD1010
- WRITE CLOCK GENERATOR
- HIGH FREQUENCY DETECTION

GENERAL DESCRIPTION

The WD1011 Winchester Data Separator has been designed to replace the complex analog/digital circuitry required for data recovery by Winchester disk drives. Directly interfacing to the WD1010 Winchester Controller device, an on-chip crystal oscillator allows operation of 4.34 Mbit/sec or 5.0 Mbit/sec transfer rates. In addition to data recovery, the device provides Write Clock signals for the WD1010 as well as high frequency detection for pre-amble search. Output levels on data pins swing close to the supply rails for increased noise immunity and to minimize layout restrictions.

The WD1011 operates from a single 5 volt supply and is available in a 16 pin plastic or ceramic Dual-in-Line package.



PIN DESIGNATION

See page 725 for ordering information.

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ADVANCE INFORMATION

WD1012 Write Precompensation Device

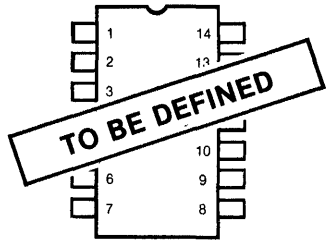
FEATURES

- DIRECT INTERFACE TO THE WD1010
- 12 NS. TYP. DELAY FROM EARLY
- PROVIDES TIMCLK FOR SA1000 TYPE DRIVES
- SINGLE +5V SUPPLY
- TTL COMPATIBLE INPUT/OUTPUTS
- COMPANION CHIP TO THE WD1011 DATA SEPARATOR

GENERAL DESCRIPTION

The WD1012 Write Precompensation device provides delayed data necessary for inner cylinder recording on Winchester disk drives. It is a companion chip to the Western Digital WD1010, utilizing signals from both the WD1010 and WD1011 data separator device. The WRITE DATA output, as well as EARLY, LATE, and RWC are applied to produce a pre-determined bit shift. Assertion of EARLY or LATE will cause a 12 ns. typ. shift of data based upon the precompensation algorithm internal to the WD1010. In addition, a divide-by-sixteen timing clock output is available for use by the SA1000 and other drives requiring a TIMCLK input.

The WD1012 operates from a single 5 volt supply and is available in a 14 pin plastic or ceramic package.



PIN DESIGNATION

See page 725 for ordering information.

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ADVANCE INFORMATION

WD1014 Buffer Manager/Error Correction Device

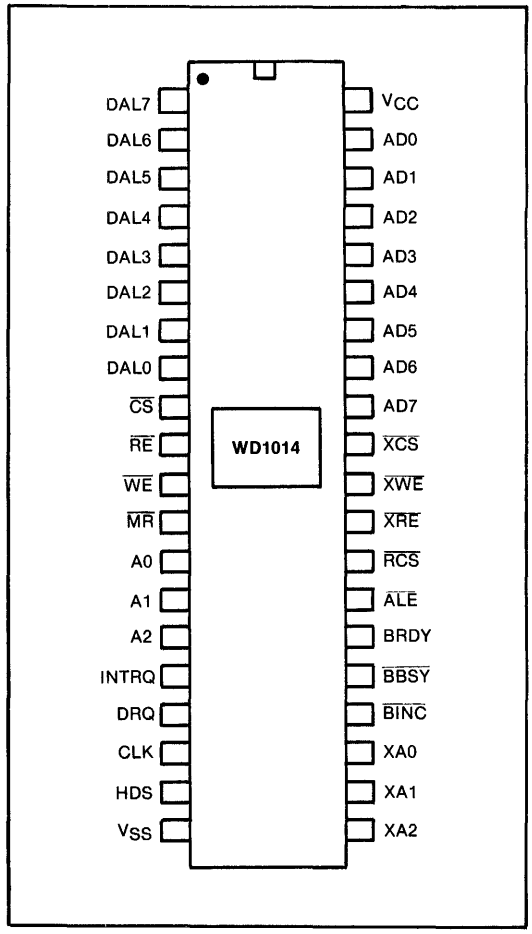
FEATURES

- DIRECT INTERFACE TO THE WD1010
- 32 AND 56 BIT ECC POLYNOMIALS
- 128, 256, 512, OR 1024 BYTE SECTORS
- BUFFER SIZE UP TO 32K BYTES
- CONTROL FOR 4 DRIVES/8 HEADS EACH
- AUTOMATIC RETRY ON ECC ERRORS
- TRANSPARENT ECC CORRECTION
- MULTI-SECTOR READ/WRITE CAPABILITY
- DMA OR PROGRAMMED I/O OPERATION
- 8-BIT TRI-STATE DATA BUS
- EXECUTES 11 MACRO-COMMANDS
- SINGLE +5V SUPPLY

GENERAL DESCRIPTION

The WD1014 is a single chip Buffer Manager/ECC device designed for use with the Western Digital Corp. WD1010 Hard Disk Controller. The device implements all of the logic required for a variable length sector buffer, ECC correction and Host interface circuitry. Use of the BMEC greatly reduces the complexity of the interface design, device count, board size requirements and increases system reliability.

The WD1014 operates from a single +5V supply and is available in a 40 pin plastic or ceramic Dual-in-Line package.



PIN DESIGNATIONS

PIN NUMBER	SYMBOL	DESCRIPTION
1-8	DAL7-0	Data Access Lines. Commands, status, and data to and from buffer are transferred over this tristate bidirectional data bus controlled by the host. DAL7 is MSB.
9	$\overline{CS}$	Chip Select must be active for all communications with the BMEC.
10	$\overline{RE}$	Read Enable. For reading data and status information from the BMEC.
11	$\overline{WE}$	Write Enable. For writing commands and data to the BMEC.
12	$\overline{MR}$	Master Reset. Initializes the BMEC and clears the status flags when activated.
13-15	A0-2	Address inputs. Used to select task file registers and data buffer. A2, A1, A0 = 000 selects buffer. A2 is MSB.
16	INTRQ	INTerrupt ReQuest. Activated whenever a command has been completed. It is reset when the status register is read, or when a new command is loaded via DAL7-0.
17	DRQ	Data ReQuest. Set whenever the buffer contains data to be read by the host or is awaiting data to be written by the host.
18	CLK	Clock signal input used for all internal timing.
19	HDS	Head & Drive Select for setting HS0-3 and DS1-4.
20	V_{SS}	GROUND
21-23	XA2-0	These address lines are used to address the disk controller when $\overline{XCS}$ = 0.
24	$\overline{BCINC}$	Buffer Counter INCrement. Increments the external buffer counter. Each negative transition is a one byte count.
25	$\overline{BBSY}$	Buffer BuSY. Signals the BMEC that the buffer is being accessed by the disk controller. It is also used to control AD0-7 bus switching and tristate $\overline{XWE}$, and $\overline{XRE}$ when it is active.
26	BRDY	Buffer ReaDY output. Signals the disk controller when the buffer memory is ready for controller data transfers. It is active when the buffer memory is full or empty.
27	$\overline{ALE}$	Address Latch Enable. Used to set the external buffer address whenever the buffer is not being accessed by the WD1010 processor.
28	$\overline{RCS}$	Ram Chip Select. Asserted when the BMEC or host accesses the external buffer.
29	$\overline{XRE}$	Tristate line activated only when $\overline{BBSY}$ = high. When $\overline{XCS}$ is low, information is read from the selected WD1010 task files registers. When $\overline{RCS}$ is low, data is read from the buffer.
30	$\overline{XWE}$	Tristate line activated only when BBSY = high. When $\overline{XCS}$ is low, command or task file information is written into the disk controller. When $\overline{RCS}$ is low data is written into the buffer.
31	$\overline{XCS}$	This Chip Select is used to access the disk controller.
32-39	AD7-0	Address or Data bus shared by the buffer, BMEC and the WD1010. While ALE is active a new buffer address is latched in an external counter, where AD7 = A14 and AD0 = A7. This allows buffer sizes from 128 bytes to 32K bytes.
40	V_{CC}	+5 ± 5% volt power supply.

FUNCTIONAL DESCRIPTION

The BMEC is designed to interface directly with industry standard static RAM chips and common TTL/LS latches and counters. The sector buffer, an integral part of the WD1010 system architecture, is addressed by a multiplexed data/address bus (AD0-7), which is also shared by the WD1010 and drive/head control latches. The WD1014 manages the external sector buffer so that it can support all WD1010 sector sizes in single and multiple sector operations. All buffer control signals required by the WD1010 are produced by the BMEC so that no external logic is required to interface the WD1010 to the BMEC.

During sector reads and writes, the BMEC produces an Error Correction Code (ECC) as data is transferred to and from the buffer. The user may select either a 32 or 56 bit polynomial depending upon his needs. Errors are detected and corrected without intervention by the host. The BMEC controls all retries on data ECC errors for the host as well. Corrected errors are reported as a status to the host. Uncorrectable errors are reported by setting the error bit in the status register with the appropriate descriptor bit set in the error register.

TASK FILE

The task file is a set of registers which contain commands, status, track, sector and other task information. Nine registers are accessed via A2 to A0 during read and write modes. Depending on the command from the host and the status of the system, the proper information is stored to or read from the task file.

A2	A1	A0	READ	WRITE
1	1	1	Status	Command
0	0	1	Error flags	Write Precomp Cylinder
0	1	0	Sector Count	Sector Count
0	1	1	Sector Number	Sector Number
1	0	0	Cylinder Number (low)	Cylinder Number (low)
1	0	1	Cylinder Number (high)	Cylinder Number (high)
1	1	0	S D H*	S D H*

*S D H bytes specifies sector size, drive number and head number.

The SDH register is coded as follows:

Bit 7 (MSB) is set for a 7 byte sector extension (used for ECC bytes).

Bits 6 and 5 contain the sector size.

The possible sector sizes and their selection codes are:

BIT 6	BIT 5	SECTOR SIZE
1	1	128 byte data field
0	0	256 byte data field
0	1	512 byte data field
1	0	1024 byte data field

Bits 4 and 3 specify Drive Number. These bits are decoded internally and latched externally to perform the select function.

Bits 2, 1 and 0 specify Head Number.

COMMAND REGISTER

The command register is accessed by writing into register 7. All other task information should be loaded into the task file before loading the command register. Command execution starts immediately after the command register is loaded and subsequent register loads are ignored until the command is done. The commands are as follows:

COMMAND	BIT CODE MSB 7	6	5	4	3	2	1	0
Restore	0	0	0	1	R3	R2	R1	R_0
Seek	0	1	1	1	R3	R2	R1	R_0
Read Sector	0	0	1	0	D	M	0	E
Write Sector	0	0	1	1	0	M	0	E
Scan ID	0	1	0	0	0	0	0	0
Write Format	0	1	0	1	0	0	0	0
Read Copy	1	0	1	0	0	M	0	E
Write Copy	1	0	1	1	0	M	0	E
Read Long	0	1	1	0	D	0	1	E
Write Long	0	1	1	1	D	0	1	E
Set Parameters	1	1	0	1	0	0	0	0

D = 1: Interrupt for DMA mode
D = 0: Interrupt for programmed I/O mode
M = 1: Multiple Sector Read or Write
E = 1: Select 56 bit ECC polynomial
E = 0: Select 32 bit ECC polynomial
R3 R2 R1 R0 = 0000 : Step time = 20μs
0001 : Step time = .5ms
0010 : Step time = 1.0ms
0011 : Step time = 1.5ms
:
:
1111 : Step time = 7.5ms for 5 MHz write clock

THE STATUS AND ERROR REGISTERS

The Status Register indicates to the host the status of the system. If the Error bit in the Status Register is set, one or more bits in the Error Register will be set. The meaning of the these bits is shown below:

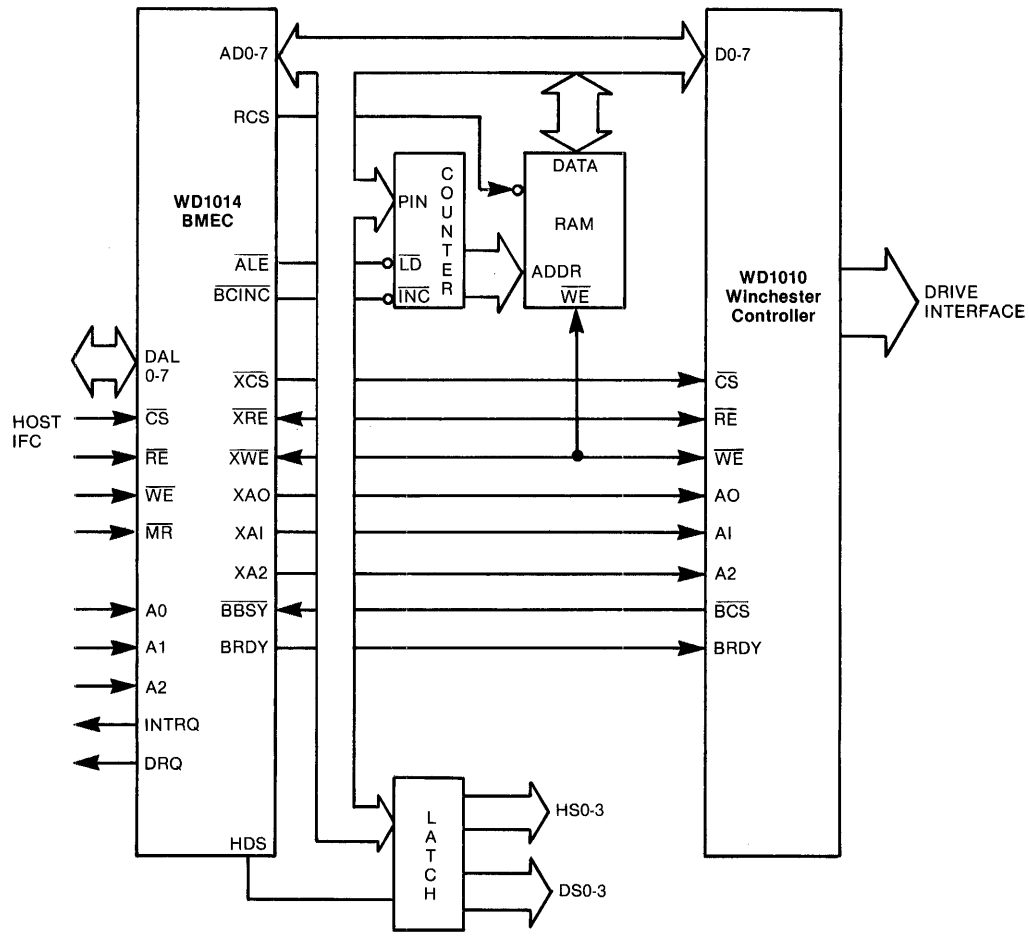
BIT	STATUS REGISTER	ERROR REGISTER
MSB 7	Busy	Bad Block Detect
6	Drive ready	Uncorrectable
5	Write fault	CRC Error — ID Field
4	Seek complete	ID Not Found
3	Data request	——
2	Data Error Corrected	Aborted Command
1	Command in progress	TR000 Error
LSB 0	Error	DAM Not Found

COMMAND DESCRIPTIONS

The BMEC passes on all information between the host and the WD1010. Some commands are modified by the BMEC and some are simply echoed. The following is a list of the commands and their formats and descriptions.

COMMAND	FORMAT	DESCRIPTION
RESTORE	0 0 0 0 R3 R2 R1 R0	Pass on task information and command and initiates a read status after the command is completed. The command is echoed. Stepping rate (R0-R3) is set.
SEEK	0 1 1 0 R3 R2 R1 R0	Pass on task information and command and initiates a read status after the command is completed. The command is echoed. Stepping rate (R0-R3) is set.
SCAN ID	0 1 0 0 0 0 0 0	Passes command to WD1010 which scans ID headers on current track. Updates cylinder number in task file and command and initiates a read status after the command is completed. The command is echoed.
READ SECTOR	0 0 1 0 D M 0 E	Write the buffer with data from WD1010. If ECC is enabled, ECC bytes are recomputed by the BMEC. After the buffer is full, the recorded ECC bytes are compared to the generated bytes to generate the syndrome bytes. If the syndrome is non-zero, errors have occurred and error correction is invoked by the BMEC. If the error is not correctable the BMEC retries the sector read. If the data is correctable the BMEC corrects the data and passes the data in the buffer to the host. Read status is requested by the BMEC and is sent from the WD1010 to the host. If, after a specified number of retries, the error is still uncorrectable, the BMEC sends an error status to the host along wtih the status from the WD1010.
WRITE SECTOR	0 0 1 1 0 M 0 E	Write the buffer with data bytes from the host. Pass the task information and command to the WD1010. The WD1010 seeks track if necessary, then writes the sector from the buffer to disk. Generate the ECC polynomial, selected by E, as the buffer is written to disc. Write the total number of sectors specified by the sector count if M = 1 in format. If M = 0 then the sector count is ignored and only one sector is written. After the sector data is written to the disc, the BMEC sends the WD1010 the ECC bytes. The BMEC requests status from the WD1010 and passes on this information to the host at the host's request.
READ LONG	0 1 1 0 D 0 1 E	Similar to Read Sector except the ECC operation producing a syndrome is inhibited in the BMEC. Instead, the BMEC copies the recorded ECC bytes from disc and passes them unaltered to the host.
WRITE LONG	0 1 1 1 D 0 1 E	The Write Long command functions similarly to the Write Sector command except the ECC operation of computing the ECC word is inhibited in the BMEC. Instead, the BMEC accepts a 32, or 56 bit appendage from the host and passes it unaltered to the WD1010 to be written on the disc after the data.
WRITE COPY	1 0 1 1 0 M 0 E	The Write Copy command is similar to the Write Sector command, except the BMEC does not send a data request (DRQ) to the host at the beginning of the command. The BMEC assumes it has a full buffer to write to the disc. The buffer could have been filled by another device other than the host, such as a back-up tape or data from another disc. This commands allows the copying of data from one disc to another with minimal host intervention.

COMMAND	FORMAT	DESCRIPTION
READ COPY	1 0 1 0 0 M 0 E	The Read Copy command is similar to the Read Sector command, except the BMEC does not send a data request (DRQ) to the host at the end of the command. This command, when used with the Write Copy command, allows the copying of data from one disk to another with minimal host intervention.
SET PARAMETERS	1 1 0 1 0 0 0 0	The buffer size parameter is specified by the value held in the sector size task register. The buffer size corresponds to the sector size task register value multiplied by 128. (E.G. if the sector size task register value = 1, then it specifies a buffer size of 128 bytes. A 32768 (32K) byte length buffer is specified by a sector size register value = 0.)



WD1010/WD1014 WINCHESTER CONTROLLER

See page 725 for ordering information.

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ADVANCE INFORMATION

WD1050 SMD Controller/Formatter

FEATURES

- 16 BIT HOST INTERFACE
- 9.677 MBITS/SEC DATA RATE
- SINGLE/MULTIPLE SECTOR TRANSFERS
- HARD SECTOR FORMAT
- TTL COMPATIBLE INPUT/OUTPUTS
- SINGLE 5V SUPPLY
- 64 PIN JEDEC CHIP CARRIER PACKAGE
- COMPATIBLE WITH SMD, MMD, FHT, LMD, AND CMD FAMILIES

DESCRIPTION

The WD1050 SMD controller/formatter is a MOS/LSI device designed to interface an SMD compatible rigid disk drive to a host processor. The device is compatible with all rigid disk drives adhering to Control Data Corporation's flat cable interface for SMD, MMD, FHT, FMD, LMD and CMD families (CDC specification 64712400 Rev H). It is TTL compatible on all inputs and outputs, with interface capability for 8 or 16 bit data busses.

The WD1050 contains a powerful set of macro-commands for read/write and control functions. An internal 16 bit task file is used to process a selected command based upon parameter information in the file.

The WD1050 operates from a single +5V supply and is available in a 64 pin JEDEC chip-carrier package.

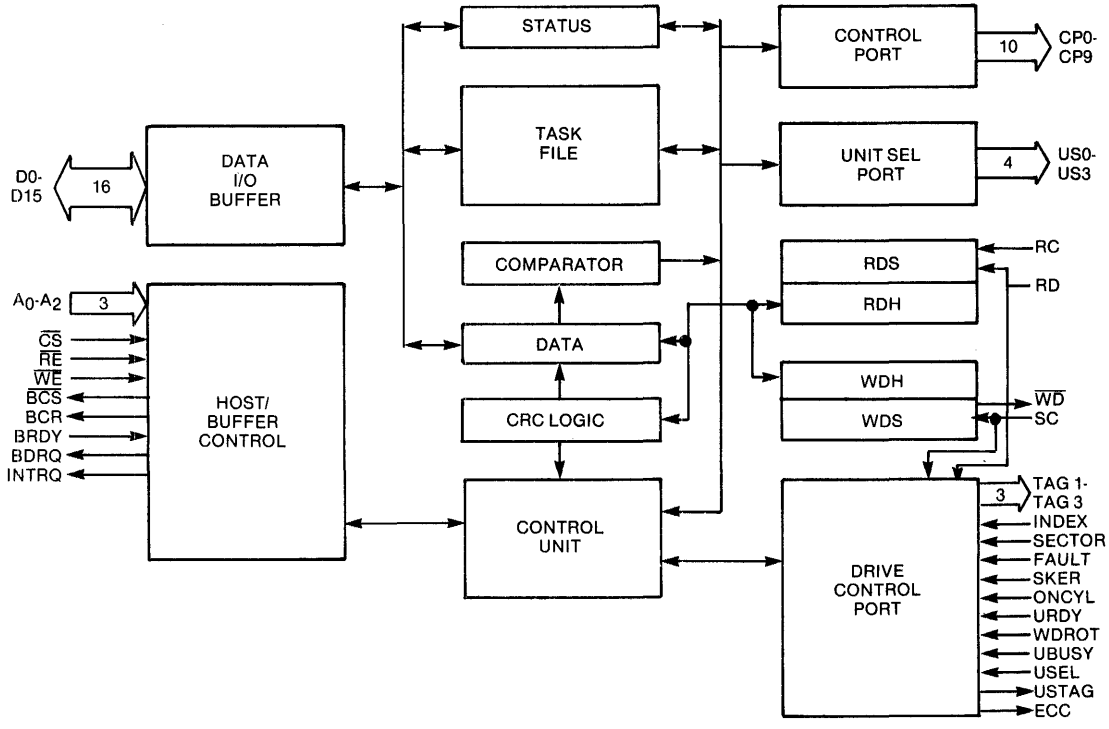


Figure 1 BLOCK DIAGRAM

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	V_{CC}	V_{CC}	+5V ± 5% power supply input
2	$\overline{\text{READ ENABLE}}$	$\overline{RE}$	Tri-state bidirectional line, used as an input when reading the task file and an output when the WD1050 is reading from the buffer.
3	$\overline{\text{WRITE ENABLE}}$	$\overline{WE}$	Tri-state bidirectional line used as an input when writing to the task file and an output when the WD1050 is writing to the buffer.
4	$\overline{\text{CHIP SELECT}}$	$\overline{CS}$	A logic low on this input enables both $\overline{WE}$ and $\overline{RE}$ signals.
5-7	ADDRESS 0→2	A0→A2	These three inputs select a task file register to receive/transmit data.
8-23	DATA BUS 0-15	D0-D15	Sixteen bit bidirectional bus used for transfer of commands, status, and data.
24	$\overline{\text{WRITE DATA}}$	$\overline{WD}$	Open Drain, NRZ data output which is synchronized to the Servo Clock input.
25	READ CLOCK	RC	Input clock from the drive which is synchronized with the Read Data Input.
26	SERVO CLOCK	SC	A nominal 9.677 MHz clock input from the drive. This clock must be valid when Unit Ready (Pin 31) is active and Fault (Pin 34) is inactive.
27	READ DATA	RD	NRZ data input from the drive which must be synchronized to the Read Clock (Pin 25) input.
28	INDEX PULSE	IP	Active high input used to monitor the Index signal from the drive.
29	SECTOR	SEC	Active high input used to monitor sector pulses from the drive.
30	UNIT SELECT	USEL	Active high output pulse used to strobe US0-US2 lines.
31	UNIT READY	URDY	Active high input used to inform the WD1050 of a READY condition on a selected drive. If this line is made inactive during any command (except RTZ or FAULT CLEAR), current command execution is terminated.
32	UNIT BUSY	UBSY	Active high input used to monitor drive status during a unit selection. If the unit had previously been selected and/or reserved prior to issuing a USTAG, the UBSY must be made active within one microsecond of the USTAG selection. This signal is used for dual-channel access applications and should be tied to ground when not used.
33	GROUND	V_{SS}	Ground.
34	FAULT	FAULT	Active high input used to detect a fault condition at the drive. Command execution is terminated if fault is made active during any command. Only the FAULT CLEAR command may be issued while this line is ascerted.
35	SEEK ERROR	SKERR	Active high input used to detect a seek error at the drive.
36	ON CYLINDER	ONCYL	Active high input used to inform the WD1050 when the heads are settled and positioned over the desired cylinder.
37	WRITE PROTECT	WPROT	Active high input used to monitor the Write Protect signal from the drive.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
38	ERROR CORRECTION	ECC	Active high output used to synchronize external ECC logic to the Data Field.
39	UNIT SELECT TAG	USTAG	Active high output used for selection of a unit on US0-US3 lines.
40-42	TAG1-TAG3	TAG1-TAG3	Active high outputs used to strobe specific data out on the Control Port Lines. Tag definitions are: TAG1 — Cylinder address TAG2 — Head/Volume select TAG3 — Control Tag
43-46	UNIT SELECT 0-3	US0-US3	These four outputs reflect the contents of the unit address field of the task file, and are used to select one of four drives.
47-56	CONTROL PORT BITS 9-0	CP9-CP0	Ten bit output bus used to issue tag parameters to the selected drive.
57	BACK-BIAS	V_{BB}	Substrate generator. Must be left open by the user.
58	BUFFER CHIP SELECT	$\overline{BCS}$	Active low output used to enable reading or writing to the external buffer.
59	BUFFER COUNTER RESET	BCR	Active low output that is strobed prior to read/write commands. Used to clear an external buffer counter.
60	BUFFER DATA REQUEST	BDRQ	This output is set to initiate data transfers to/from the external buffer.
61	BUFFER READY	BRDY	This input informs the WD1050 that the buffer is full or empty.
62	INTERRUPT REQUEST	INTRQ	Active high output which is set at the completion of any command, providing the 'I' bit is also set in the command word.
63	MASTER RESET	$\overline{MR}$	Active low input used to initialize the WD1050, usually after a power-up condition.
64	CLOCK	CLK	2 MHz Master Clock from which all timing is derived.

ORGANIZATION

The Block Diagram of the WD1050 is shown in Figure 1. Data transfers to and from the host, as well as the sector buffer, are transferred via the D0-D15 lines. An internal control unit is used to process all commands and generate drive control signals in the SMD protocol. With the use of an external sector buffer, the WD1050 directly transfers data from the buffer to the read/write lines by the host/buffer control logic. Four buffer control signals are used to manipulate the data off-line from the host processor.

TASK FILE

Inidividual registers within the task file are accessed via the A_2-A_0 lines in conjunction with either Read Enable ($\overline{RE}$) or Write Enable ($\overline{WE}$) signals. Chip Select ($\overline{CS}$) must also be made active during an $\overline{RE}$ or $\overline{WE}$ sequence.

The MSB of the address lines (A_2) can be used for 8-bit operations when interfacing to 8-bit microprocessors. When $A_2 = 0$, 16 bit programming is in effect as shown in Figure 1. When A_2 is toggled, 8-bit selection is enabled, with data entered on D8-D15 illustrated in Table 2.

TABLE 1 TASK FILE (16 BIT PROGRAMMING)

R/W		ADDRESS			TASK FILE REGISTER	
$\overline{WE}$	$\overline{RE}$	A2	A1	A0	D_{15} D_8	D_7 D_0
✓	✓	0	0	0	Head Number	Sector Address
✓	✓	0	0	1	Upper Cylinder	Lower Cylinder
✓	✓	0	1	0	Sector Count	Section Length/Unit Address
✓		0	1	1	Upper Command	Lower Command
	✓	0	1	1	Upper Status	Lower Status

TABLE 2 TASK FILE (8 BIT PROGRAMMING)

R/W		ADDRESS			TASK REGISTER
$\overline{WE}$	$\overline{RE}$	A2	A1	A0	D_7 D_0
✓	✓	1	0	0	Head Number
✓	✓	0	0	0	Sector Address
✓	✓	1	0	1	Upper Cylinder
✓	✓	0	0	1	Lower Cylinder
✓	✓	1	1	0	Sector Count
✓	✓	0	1	0	Sector Length/Unit Address
✓		1	1	1	Upper Command
✓		0	1	1	Lower Command
	✓	1	1	1	Upper Status
	✓	0	1	1	Lower Status

COMMAND SET

The WD1050 can execute eight macro-commands. The appropriate task registers are first loaded with parameter information, then the macro-command is written into the command register. Table 3 shows the eight commands, plus a summary of the various flags used to modify the execution of each command. The STATUS Register, illustrated in Table 4 allows the host to monitor key signals and command progress. Note that the status register is a "Read-Only" register, while the command register is a "Write Only" register. Both these registers share the same address, and are differentiated by the ascertion of either $\overline{RE}$ or $\overline{WE}$.

When programmed for the 8-bit mode, two consecutive reads must be accomplished to fetch the entire status word from the task file. When $A_2 = 1$, status bits D8-D15 are read; when $A_2 = 0$, status bits D0-D7 are read.

COMMAND	LSB				COMMAND REGISTER BITS										MSB	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fault Clear	0	0	0	0	0	0	0	I	0	0	0	0	U	S	E	L
Return to Zero	0	0	0	1	V	L	O	I	0	0	0	M	U	S	E	L
Seek Cylinder	0	0	1	0	V	L	O	I	Z	C	H	M	U	S	E	L
Read ID Field	0	0	1	1	0	L	O	I	Z	C	H	M	U	S	E	L
Read Sector	0	1	0	0	R	L	O	I	Z	C	H	M	U	S	E	L
Write Sector	0	1	0	1	0	L	O	I	Z	C	H	M	U	S	E	L
Format	0	1	1	0	0	P	O	I	Z	C	H	M	U	S	E	L
Verify	0	1	1	1	0	P	O	I	Z	C	H	M	U	S	E	L

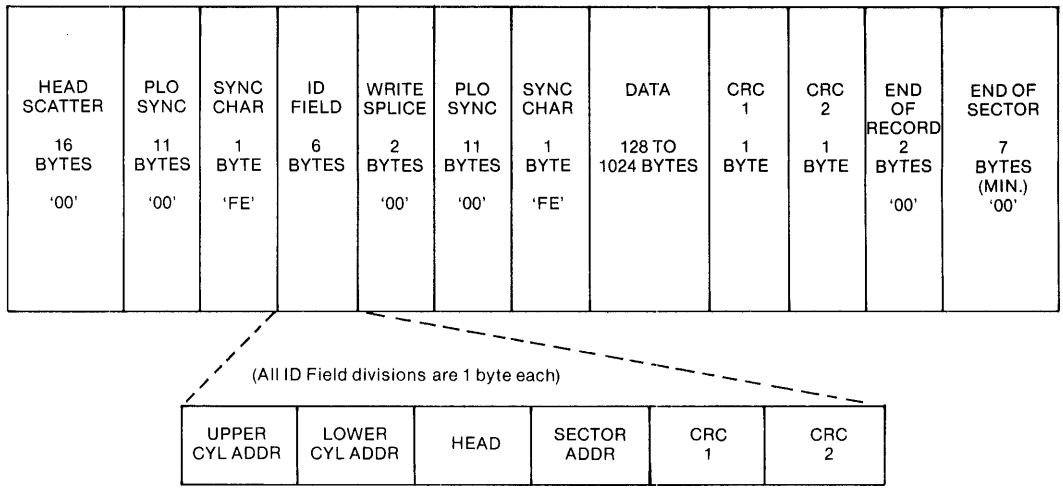
TABLE 3 COMMAND AND FLAG SUMMARY

FLAG SUMMARY	
V = Verify	I = Interrupt Enable
R = CRC Enable	Z = Volume/Head change
L = Logical Sectoring	C = Cylinder Addr
P = Programmable Sectors	H = Head selection
O = On Cylinder	M = Marginal data recovery
E = Priority Release/Early	U = Unit Sel/Servo Minus
L = Unit Deselect/Late	S = Priority Sel/Servo Plus

TABLE 4 STATUS WORD SUMMARY

	BIT	STATUS DESCRIPTION
UPPER	15	BUFFER CHIP SELECT STATUS
	14	COMMAND IN PROGRESS
	13	UNIT BUSY
	12	UNIT SELECTED
	11	WRITE PROTECT
	10	UNIT READY
	9	ON CYLINDER
	8	SEEK ERROR
LOWER	7	BUFFER CHIP SELECT STATUS
	6	FAULT CONDITION
	5	BUFFER DATA REQUEST STATUS
	4	NOT USED
	3	DATA FIELD CRC ERROR
	2	DATA SYNCH MARK NOT FOUND
	1	ID CRC ERROR
	0	ID NOT FOUND

FIXED SECTOR FORMAT



See page 725 for ordering information.

Printed in U.S.A.

WESTERN DIGITAL
CORPORATION

FD176X-02
Floppy Disk Formatter/Controller Family

FEATURES

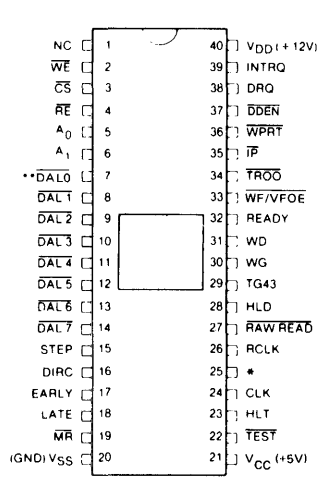
- 1 MHZ VERSION OF FD179X
- TWO VFO CONTROL SIGNALS — RG & VFOE
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY
- READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128, 256, 512 or 1024 Byte Sector Lengths
- WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-Chip Track and Sector Registers/Comprehensive Status Information
- PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- WRITE PRECOMPENSATION
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- INTERFACES TO WD1691 DATA SEPARATOR

176X-02 FAMILY CHARACTERISTICS

FEATURES	1761	1763	1765	1767
Single Density (FM)	•	•	•	•
Double Density (MFM)	•	•	•	•
True Data Bus		•		•
Inverted Data Bus	•		•	
Write Precomp	•	•	•	•
Side Selection Output			•	•

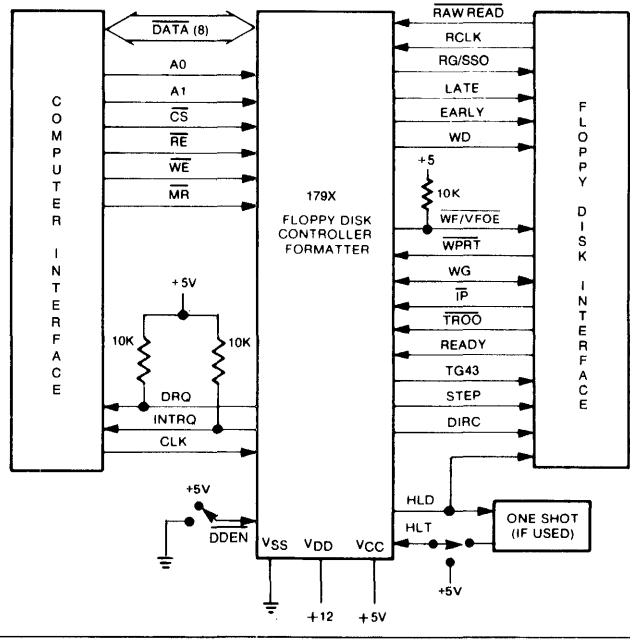
APPLICATIONS

5¼" MINI FLOPPY CONTROLLER
SINGLE OR DOUBLE DENSITY
CONTROLLER/FORMATTER



*1761/3 = RG;1765/7 = SSO
**1763/7 TRUE BUS

PIN CONNECTIONS



FD176X SYSTEM BLOCK DIAGRAM

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.
19	MASTER RESET	$\overline{MR}$	A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ±5%
40		V_{DD}	+12V ±5%
COMPUTER INTERFACE:			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control:
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit Bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by $\overline{WE}$ or transmitter enabled by $\overline{RE}$. Each line will drive 1 standard TTL load.
24	CLOCK	CLK	This input requires a free-running 1 MHZ ± 1% 50% duty cycle square wave clock for internal timing reference.
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the WRITE DATA pulse occuring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.

$\overline{CS}$	A1	A0	$\overline{RE}$	$\overline{WE}$
0	0	0	Status Reg	Command Reg
0	0	1	Track Reg	Track Reg
0	1	0	Sector Reg	Sector Reg
0	1	1	Data Reg	Data Reg

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated steppers.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD.
25	READ GATE (1761, 1763)	RG	This output is used for synchronization of external data separators. The output goes high after two Bytes of zeros in single density, or 4 Bytes of either zeros or ones in double density operation.
25	SIDE SELECT OUTPUT (1765, 1767)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the Sector I.D. Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	A 400 ns (MFM) or 1000 ns (FM) output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$ $\overline{\text{VFO ENABLE}}$	$\overline{\text{WF/VFOE}}$	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1765/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1761/3, VFOE will remain low until the end of the Data Field. This pin has an internal 100K Ohm pull-up resistor.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD176X that the Read/Write head is positioned over Track 00.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
35	INDEX PULSE	$\overline{IP}$	This input informs the FD176X when the index hole is encountered on the diskette.
36	WRITE PROTECT	$\overline{WPRT}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	DOUBLE DENSITY	$\overline{DDEN}$	This input pin selects either single or double density operation. When $\overline{DDEN}$ = 0, double density is selected. When $\overline{DDEN}$ = 1, single density is selected.

GENERAL DESCRIPTION

The FD176X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD176X is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD176X contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD176X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The FD176X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD176X is TTL compatible on all inputs and outputs. The outputs will drive ONE TTL load or three LS loads. The 1763 is identical to the 1761 except the DAL lines are TRUE for systems that utilize true data busses.

The 1765/7 has a side select output for controlling double sided drives.

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input ($\overline{RAW\ READ}$) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

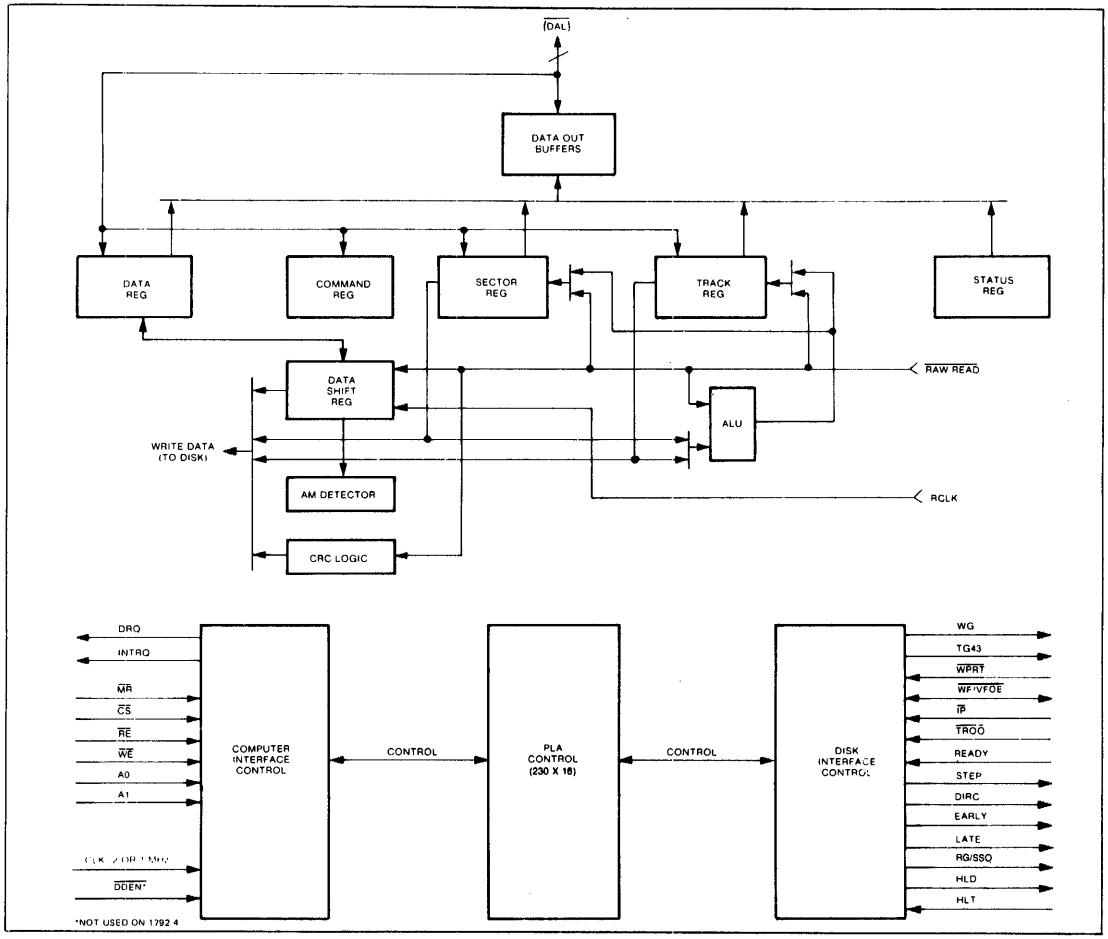
Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control — All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.



FD176X BLOCK DIAGRAM

The FD176X has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 0 double density (MFM) is assumed. When $\overline{DDEN}$ = 1, single density (FM) is assumed.

AM Detector — The address mark detector detects ID, data and index address marks during read and write operations.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{DAL}$) and associated control signals. The $\overline{DAL}$ are used to transfer Data, Status, and Control words out of, or into the FD176X. The $\overline{DAL}$ are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1	A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD176X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new

data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The 176X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input (Pin 24) is at 1 MHz.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1." For MFM formats, $\overline{DDEN}$ should be placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

Sector Length Table*	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

*1765/67 may vary — see command summary.

The number of sectors per track as far as the FD176X is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD176X is concerned is from 0 to 255 tracks.

For read operations in 5¼" double density the FD176X requires $\overline{RAW\ READ}$ Data (Pin 27) signal which is a 400 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) on 1761/63 which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FD176X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD176X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD176X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the $\overline{VFOE}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{VFOE}$ will go active low when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 176X is inspecting data off the disk

If $\overline{WF}/\overline{VFOE}$ is not used, this pin may be left open, as it has an internal pull-up resistor.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD176X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{Write\ Protect}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD176X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{Write\ Fault}$ input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD176X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 1000 ns pulses in FM ($\overline{DDEN}$ = 1) and 400 ns pulses in MFM ($\overline{DDEN}$ = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written EARLY. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD176X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

READY

Whenever a Read or Write command (Type II or III) is received the FD176X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

COMMAND DESCRIPTION

The FD176X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one

exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

TABLE 1. COMMAND SUMMARY

A. Commands for Models: 1761, 1763

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	I_1	I_3	I_2	I_1	I_0

B. Commands for Models: 1765, 1767

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	L	E	U	a_0
III	Read Address	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

TABLE 2. FLAG SUMMARY

FLAG SUMMARY

Command Type	Bit No(s)		Description
I	0, 1	r_1 r_0 = Stepping Motor Rate See Table 3 for Rate Summary	
I	2	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track
I	3	h = Head Load Flag	h = 1, Load head at beginning h = 0, Unload head at beginning
I	4	T = Track Update Flag	T = 0, No update T = 1, Update track register
II & III	0	a_0 = Data Address Mark	a_0 = 0, FB (DAM) a_0 = 1, F8 (deleted DAM)
II	1	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare
II & III	1	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1
II & III	2	E = 30 MS Delay	E = 0, No 30 MS delay E = 1, 30 MS delay
II	3	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1
II	3	L = Sector Length Flag	

	LSB's Sector Length in ID Field 00	01	10	11
L = 0	256	512	1024	128
L = 1	128	256	512	1024

FLAG SUMMARY

Command Type	Bit No(s)		Description
II	4	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records
IV	0-3	I_x = Interrupt Condition Flags	
		I_0 = 1 Not Ready To Ready Transition	
		I_1 = 1 Ready To Not Ready Transition	
		I_2 = 1 Index Pulse	
		I_3 = 1 Immediate Interrupt, Requires A Reset	
		I_3-I_1 = 0 Terminate With No Interrupt (INTRQ)	

*NOTE: See Type IV Command Description for further information.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field (r_0 r_1), which determines the stepping motor rate as defined in Table 3.

A 4 μs (MFM) or 8 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 24 μs before the first stepping pulse is generated.

The rates (shown in Table 3) can be applied to a Step-Direction Motor through the device interface.

TABLE 3. STEPPING RATES

$\overline{DDEN}$	0	1	X
R1 R0	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=0
0 0	6 ms	6 ms	368μs
0 1	12 ms	12 ms	380μs
1 0	20 ms	20 ms	396μs
1 1	30 ms	30 ms	416μs

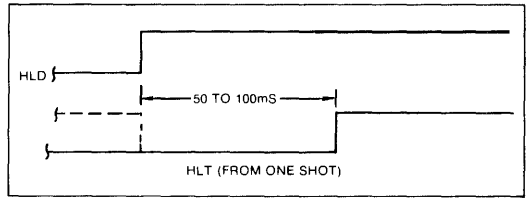
After the last directional step an additional 30 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. If $\overline{TEST}$ = 0, there is zero settling time. There is also a 30 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by settling bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 30 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

The FD176X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the FD176X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load timing (HLT) is an input to the FD176X which is used for the head engage time. When HLT = 1, the FD176X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD176X.



HEAD LOAD TIMING

When both HLD and HLT are true, the FD176X will then read from or write to the media. The "and" of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 30 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 30 ms occurs, and the FD176X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 30 ms delay occurs and the FD176X then waits for HLT to occur.

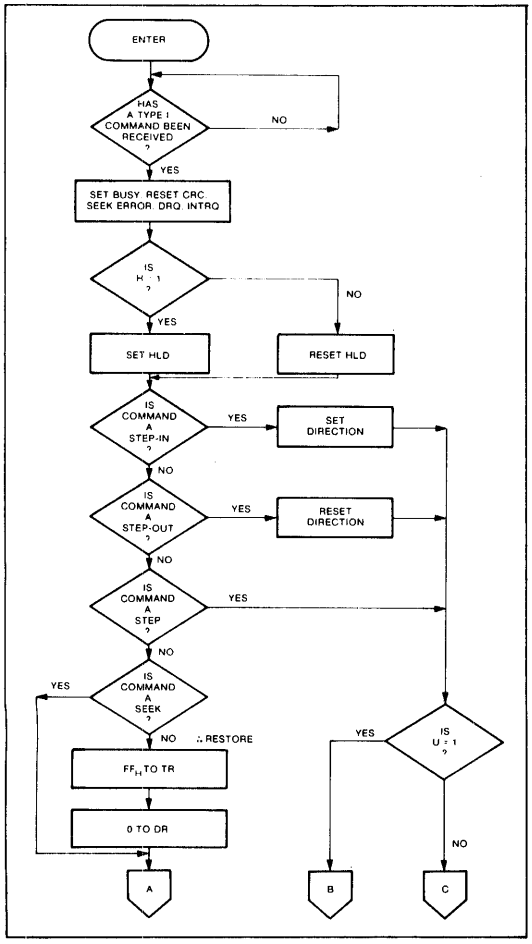
For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 30 ms delay occurs and then HLT is sampled until true.

RESTORE (SEEK TRACK 0)

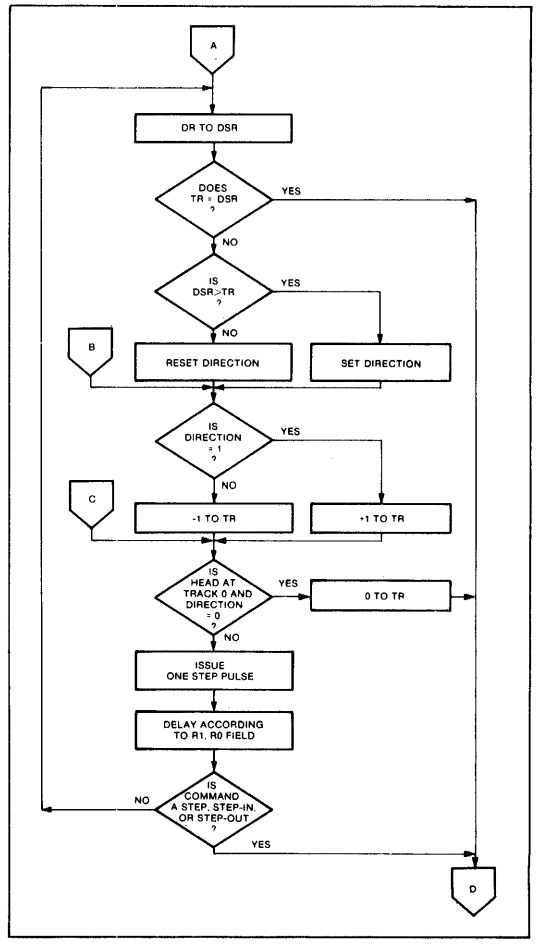
Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r1 r0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD176X terminates operation, interrupts, and sets the Seek error status bit providing the V flag is set. A verification operation also takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{MR}$ goes from an active to an inactive state and that the DRQ pin stays low.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD176X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.



TYPE I COMMAND FLOW



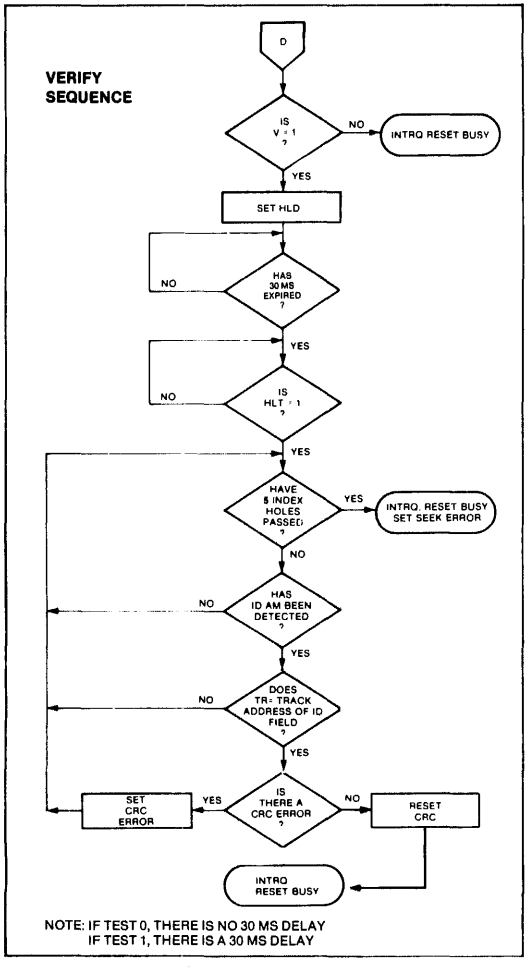
TYPE I COMMAND FLOW

STEP

Upon receipt of this command, the FD176X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the U flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD176X issues one stepping pulse in the direction towards track 80. If the U flag is on, the Track Register is incremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.



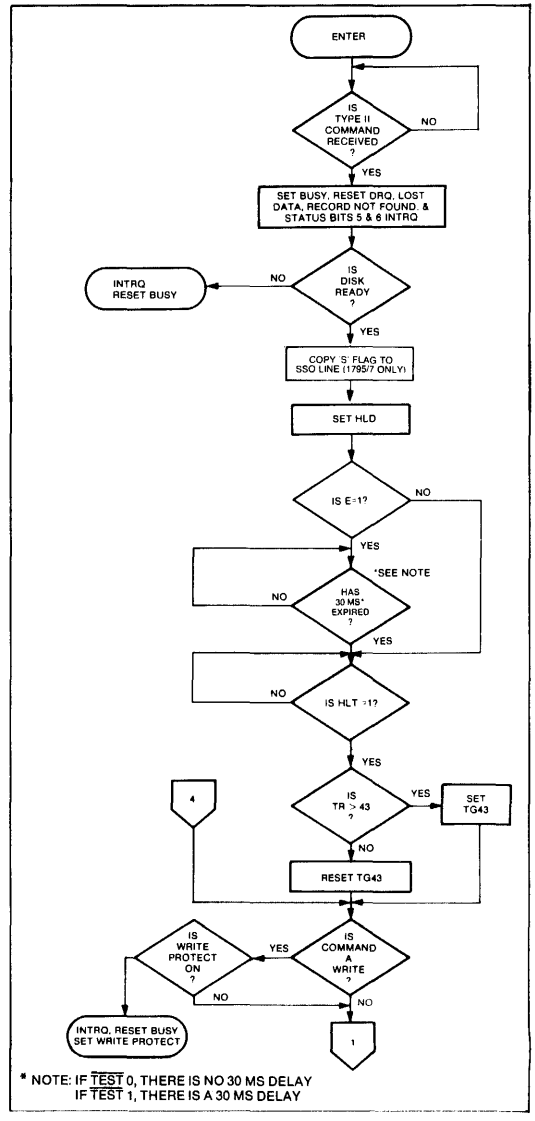
TYPE I COMMAND FLOW

STEP-OUT

Upon receipt of this command, the FD176X issues one stepping pulse in the direction towards track 0. If the U flag is on, the Track Register is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

EXCEPTIONS

On the 1765/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.



TYPE II COMMAND

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 30 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 30 msec delay. The ID field and Data Field format are shown on page 16.

When an ID field is located on the disk, the FD176X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD176X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

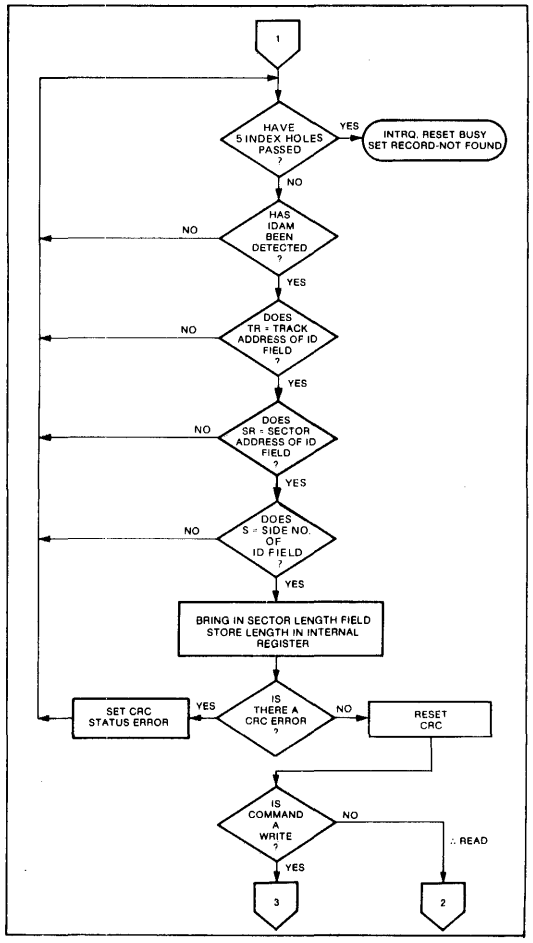
Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD176X will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the FD176X is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds the number available. The FD176X will search for 5 disk revolutions, Interrupt out, reset busy, and set the record not found status bit.

The Type II commands for 1761-63 also contain side select compare flags. When C = 0 (Bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag (Bit 3). If the S flag compares with the side number recorded in the ID field, the FD176X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The Type II and III commands for the 1765-67 contain a side select flag (Bit 1). When U = 0, SSO is updated to 0. Similarly, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions the interrupt line is made active and the RNF status bit is set.

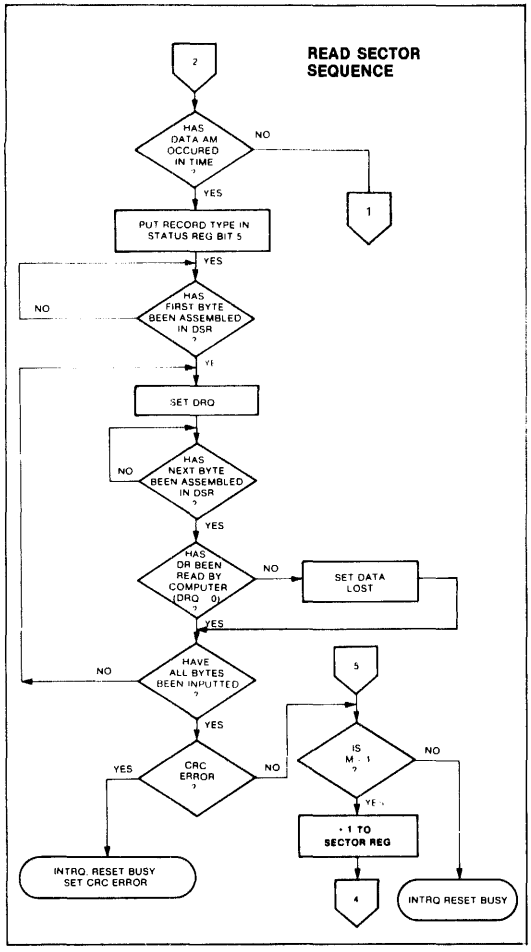
The 1765/7 READ SECTOR and WRITE SECTOR commands include a 'L' flag. The 'L' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatability, the 'L' flag should be set to a one.

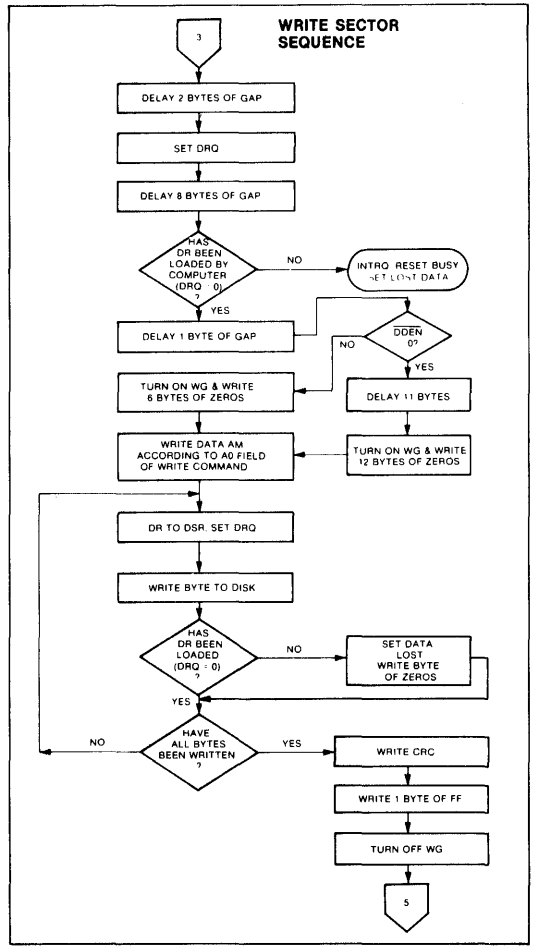


TYPE II COMMAND

READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID field is searched for and verified again followed by the Data Address Mark search. If after 5 revolutions the DAM cannot be found, the Record Not Found status bit is set and the operation is terminated.





TYPE II COMMAND

TYPE II COMMAND

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

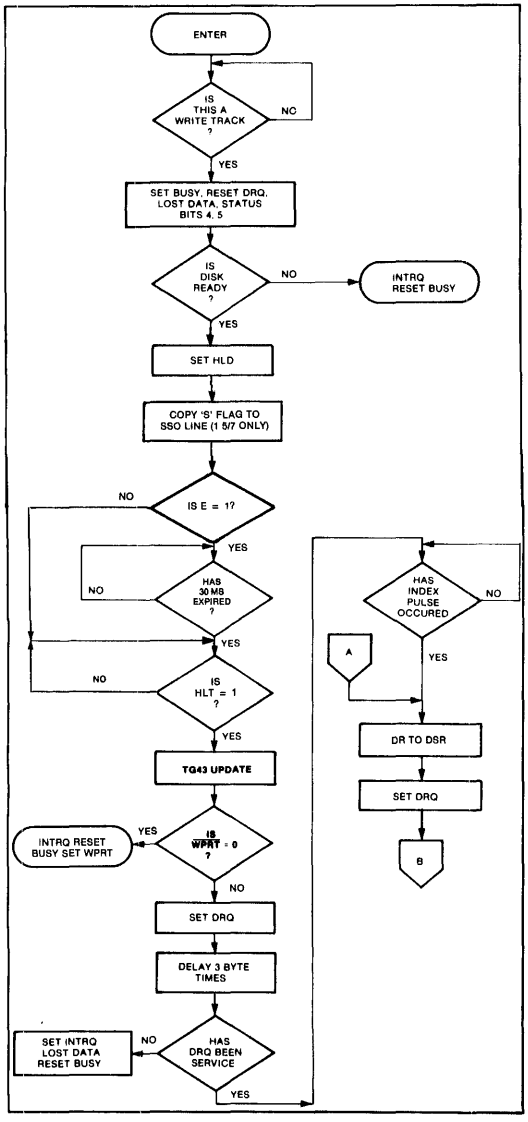
WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FD176X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The FD176X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disk.* The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated. For a 1 MHz clock the INTRQ will set 16 to 24 μsec after the last CRC byte is written.

*If partial sectors are to be written, the proper method is to write the data and fill the balance of the sector with zeroes. Do not let the chip supply the filler by not servicing the DRQs. Doing this will mask any errors by the lost data status and the CRC's may be incorrect.

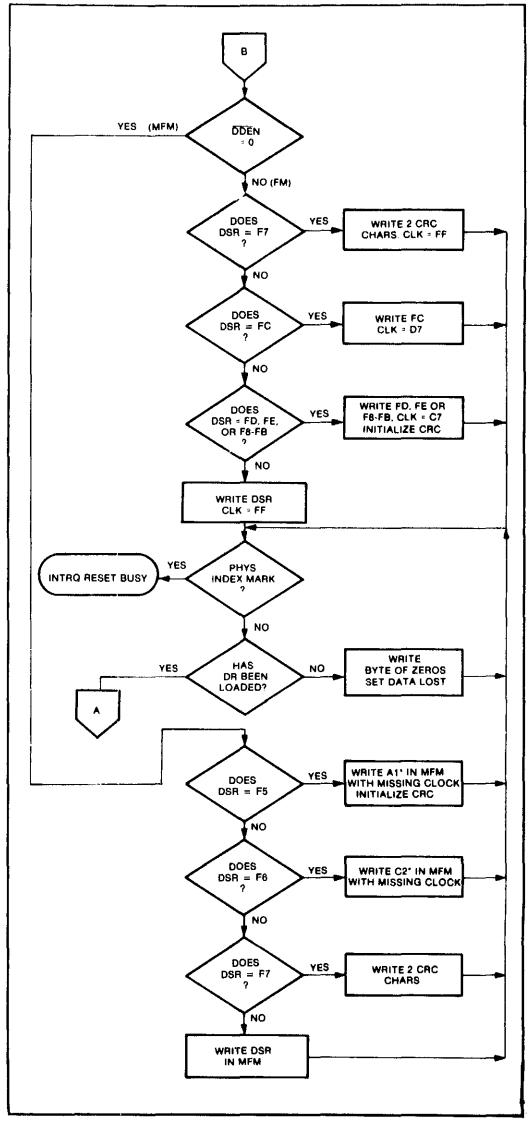


TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6



Although the CRC characters are transferred to the computer, the FD176X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the user. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: the Read Gate is not activated during the command; no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule the Lost Data status flag is set.

The ID A.M., ID field, ID CRC bytes, DAM, Data, and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

WRITE TRACK FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted. See note on page 12.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the FD176X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be tranferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

TYPE IV COMMANDS

The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to insure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

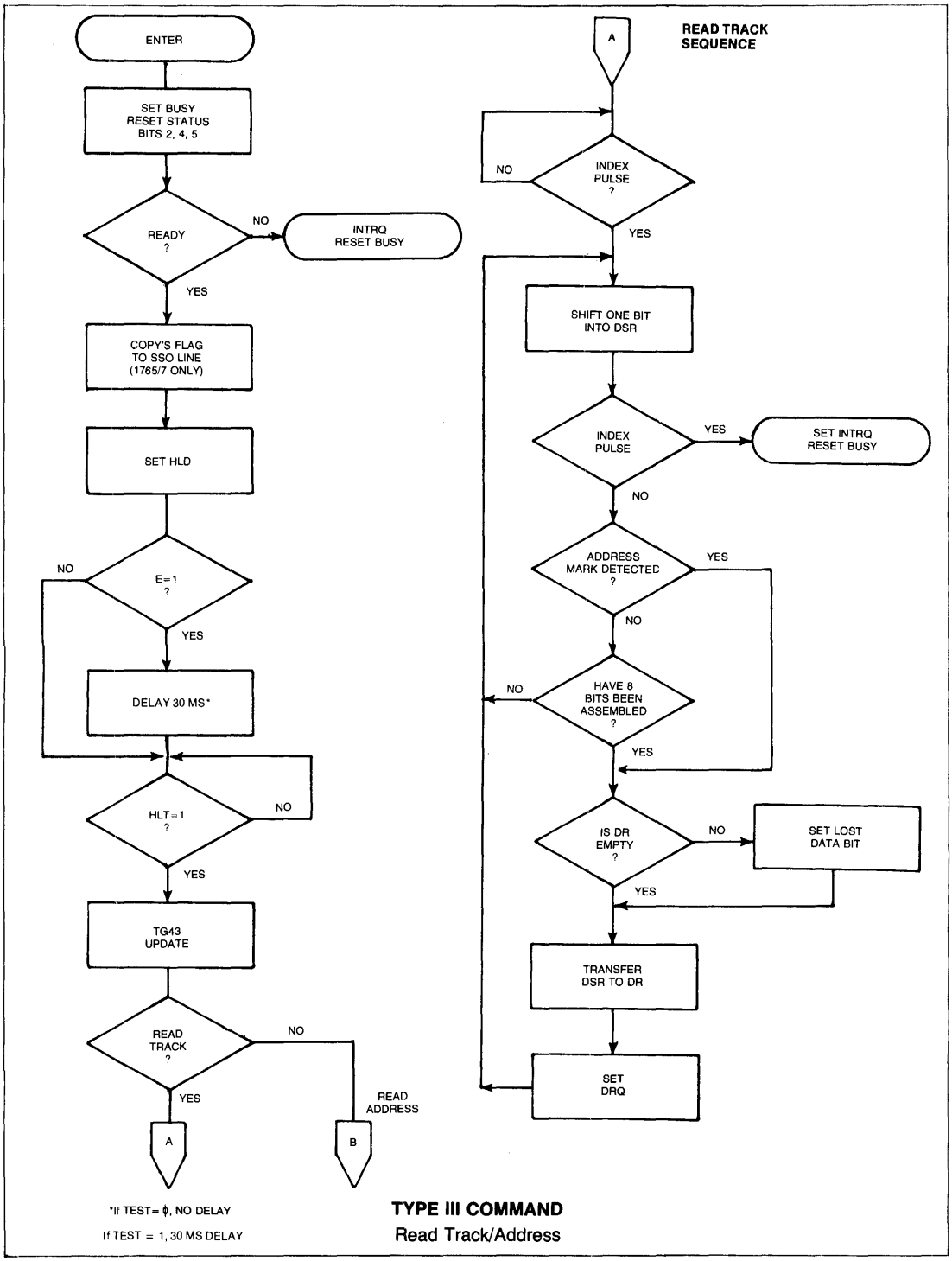
I_0 = Not-Ready to Ready Transition
I_1 = Ready to Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

CONTROL BYTES FOR INITIALIZATION

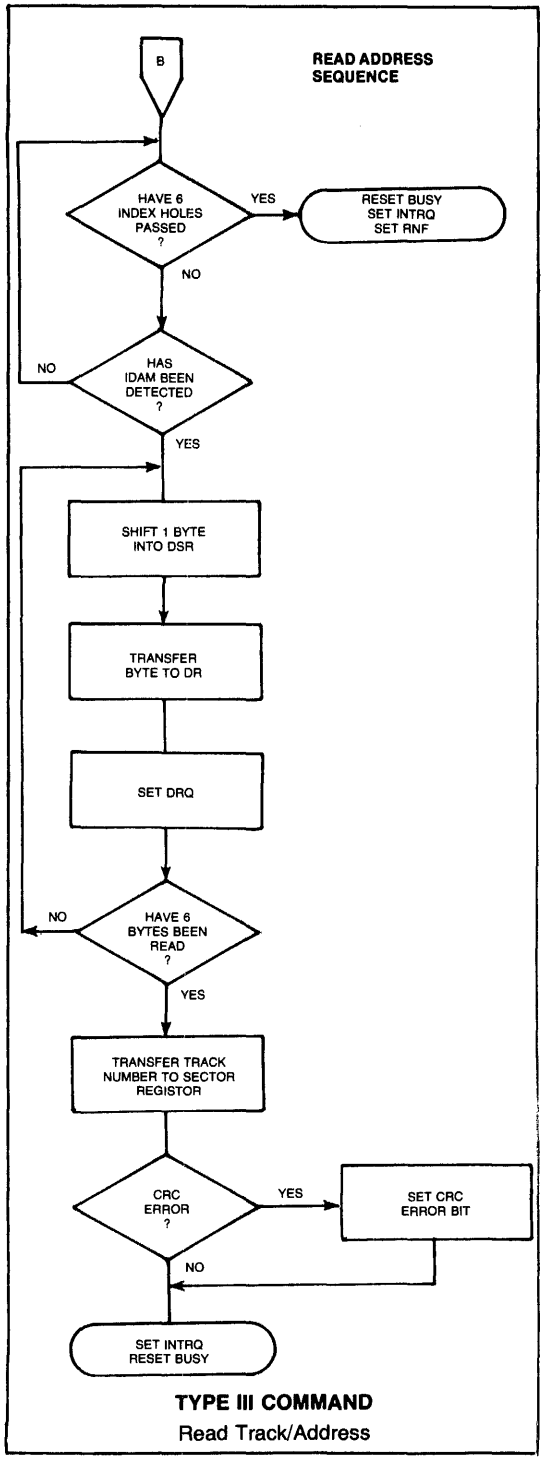
DATA PATTERN IN DR (HEX)	FD176X INTERPRETATION IN FM (DDEN = 1)	FD176X INTERPRETATION IN MFM (DDEN = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5

**Missing clock transition between bits 3 & 4



TYPE III COMMAND
Read Track/Address



TYPE III COMMAND
Read Track/Address

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3 - I_0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I_3 - I_0 are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition (I_3 = 1) an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 16 micro sec (double density) or 32 micro sec (single density before issuing a new command after issuing a forced interrupt. Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.).

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I_1 = 1) and the Every Index Pulse (I_2 = 1) are both set, the resultant command would be HEX "DA". The "OR" function is performed so that either a READY TO NOT- READY or the next Index Pulse will cause an interrupt condition.

STATUS REGISTER

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are:

Operation	Next Operation	Delay Req'd. FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	24 μs	12 μs
Write to Command Reg.	Read Status Bits 1-7	56 μs	28 μs
Write Any Register	Read From Diff. Register	0	0

RECOMMENDED — 128 BYTES/SECTOR

Shown below is the recommended single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

	NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
	40	FF (or 00)[1]
	6	00
	1	FE (ID Address Mark)
	1	Track Number
	1	Side Number (00 or 01)
	1	Sector Number (1 thru 1A)
	1	00 (Sector Length)
*	1	F7 (2 CRC's written)
	11	FF (or 00)[1]
	6	00
	1	FB (Data Address Mark)
	128	Data (IBM uses E5)
	1	F7 (2 CRC's written)
	10	FF (or 00)[1]
	369**	FF (or 00)[1]

*Write bracketed field 16 times
**Continue writing until FD176X interrupts out.
Approx. 324 bytes.
1-Optional '00' on 1765/7 only.

256 BYTES/SECTOR

Shown below is the recommended dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

	NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
	60	4E
	12	00
	3	F5 (Writes A1)
	1	FE (ID Address Mark)
	1	Track Number (0 thru 4C)
	1	Side Number (0 or 1)
	1	Sector Number (1 thru 1A)
	1	01 (Sector Length)
*	1	F7 (2 CRCs written)
	22	4E
	12	00
	3	F5 (Writes A1)
	1	FB (Data Address Mark)
	256	DATA
	1	F7 (2 CRCs written)
	24	4E
	718**	4E

*Write bracketed field 16 times
**Continue writing until FD176X interrupts out.
Approx. 668 bytes.

1. NON-STANDARD FORMATS

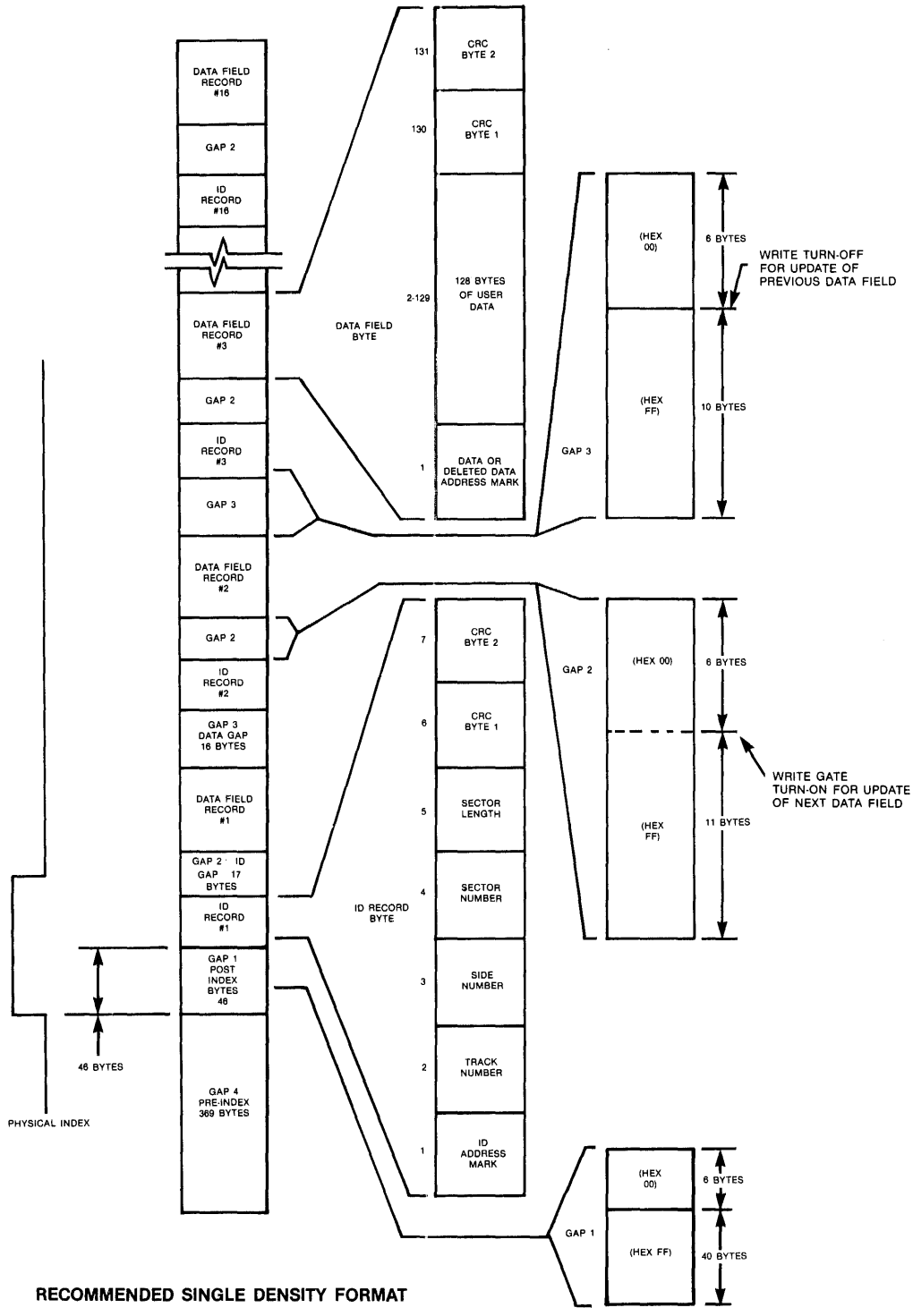
Variations in the recommended formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512 of 1024 bytes.
2) Gap 2 cannot be varied from the recommended format.
3) 3 bytes of A1 must be used in MFM.

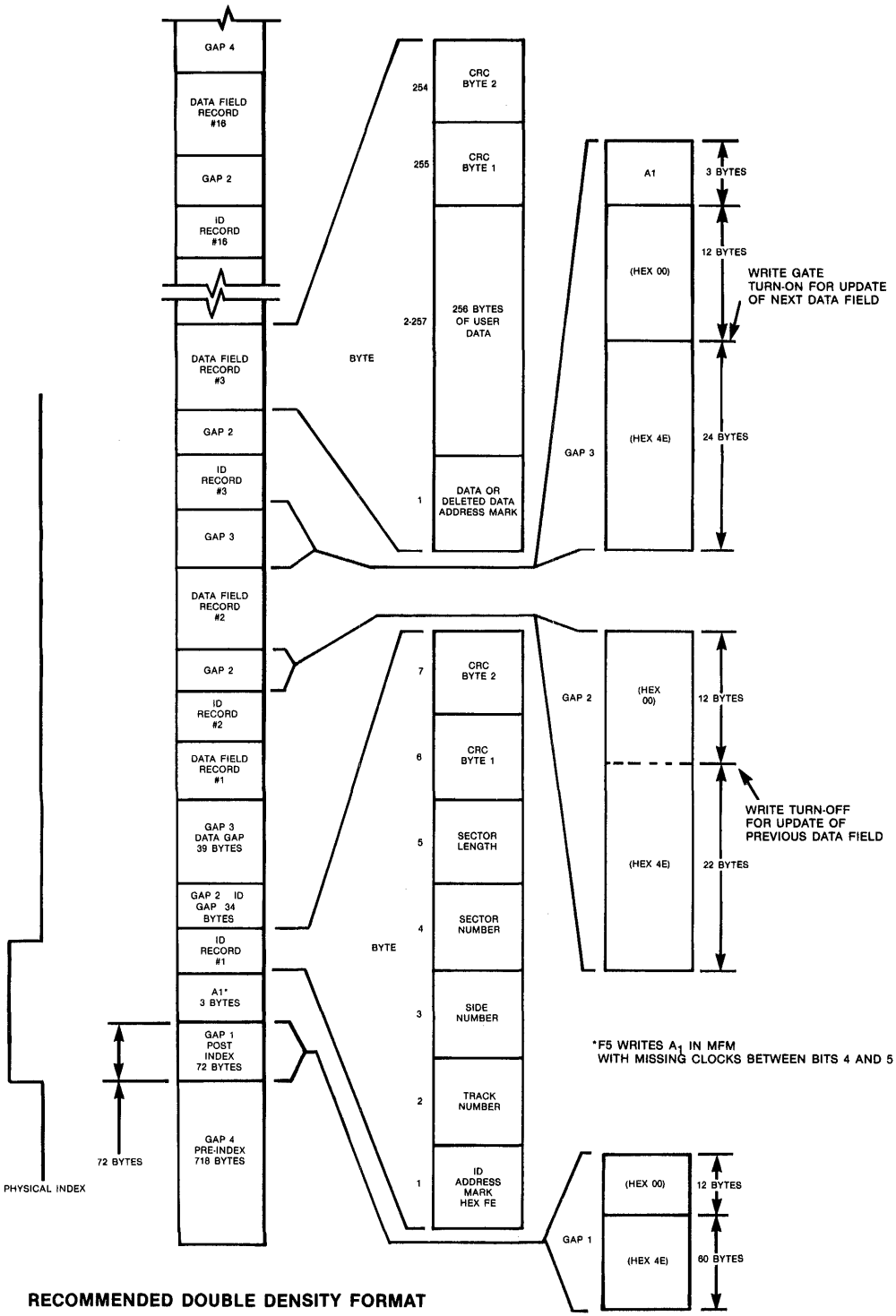
In addition, the Index Address Mark is not required for operation by the FD176X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for FD176X operation, however PLL lock up time, motor speed variation, write-splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the recommended format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.
**Byte counts are minimum, except exactly 3 bytes of A1 must be written.



RECOMMENDED SINGLE DENSITY FORMAT



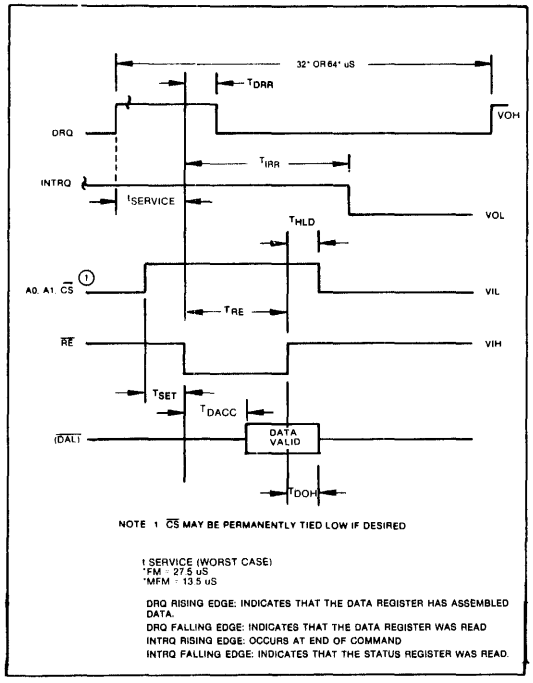
RECOMMENDED DOUBLE DENSITY FORMAT

TIMING CHARACTERISTICS

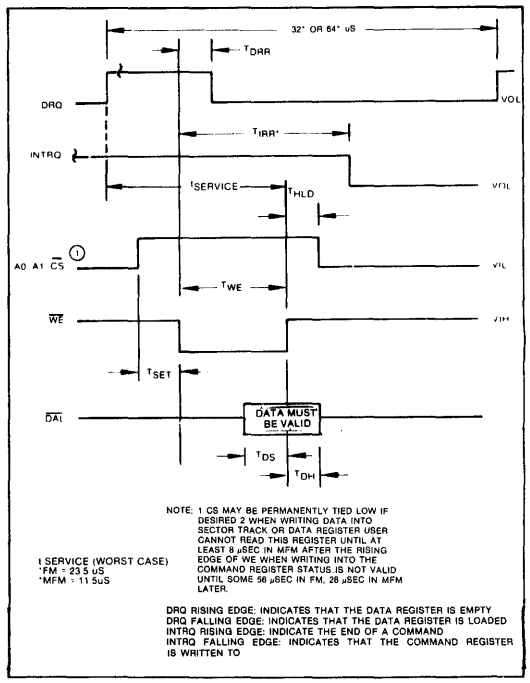
T_A = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = 0V, V_{CC} = + 5V ± .25V

READ ENABLE TIMING (See Note 4, Page 22)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	400			nsec	C_L = 50 pf
TDRR	DRQ Reset from $\overline{RE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$		1000	6000	nsec	
TDACC	Data Access from $\overline{RE}$			350	nsec	C_L = 50 pf
TDOH	Data Hold from $\overline{RE}$	50		150	nsec	C_L = 50 pf



READ ENABLE TIMING



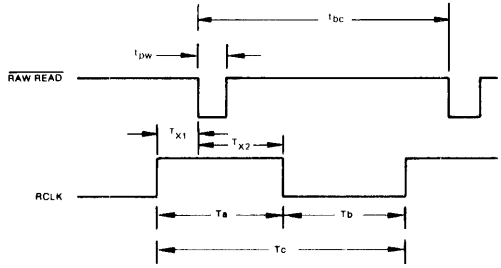
WRITE ENABLE TIMING

WRITE ENABLE TIMING (See Note 4, Page 22)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{WE}$		1000	6000	nsec	
TDS	Data Access from $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	70			nsec	

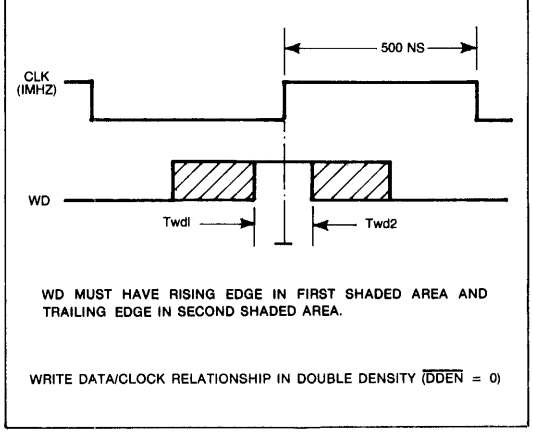
INPUT DATA TIMING (See Note 4, Page 21)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Tpw	$\overline{\text{Raw Read}}$ Pulse Width	100	200		nsec	See Note 1
tbc	$\overline{\text{Raw Read}}$ Cycle Time	3000	4000		nsec	3600 ns @ 70°C
Tc	RCLK Cycle Time	3000	4000		nsec	3600 ns @ 70°C, See Note 2
T_{X1}	RCLK hold to $\overline{\text{Raw Read}}$	40			nsec	See Note 1
T_{X2}	$\overline{\text{Raw Read}}$ hold to RCLK	40			nsec	See Note 1



			NOMINAL		
MODE	DDEN	CLK	T_a	T_b	T_c
MFM	0	1 MHz	2 μs	2 μs	4 μs
FM	1	1 MHz	4 μs	4 μs	8 μs

INPUT DATA TIMING (See Note 3, Page 22)



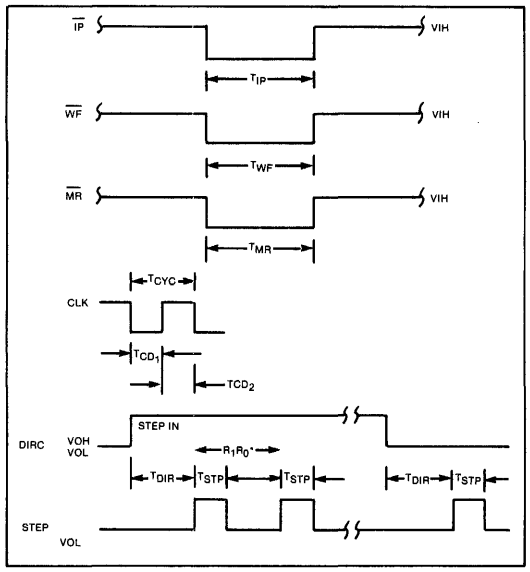
WRITE DATA TIMING

WRITE DATA TIMING (See Note 4, Page 22)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Twp	Write Data Pulse Width		1000		nsec	FM
			400		nsec	MFM
Twg	Write Gate to Write Data		4		μsec	FM
			2		μsec	MFM
Tbc	Write data cycle Time		4, 6, or 8		μsec	± CLK Error
Ts	Early (Late) to Write Data	250			nsec	MFM
Th	Early (Late) From Write Data	250			nsec	MFM
Twf	Write Gate off from WD		4		μsec	FM
			2		μsec	MFM
Twdl	WD Valid to Clk	100			nsec	
Twd2	WD Valid after CLK	100			nsec	

MISCELLANEOUS TIMING (See Note 4, Page 22)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD_1	Clock Duty (low)	460	500	20000	nsec	
TCD_2	Clock Duty (high)	400	500	20000	nsec	
TSTP	Step Pulse Output	4 or 8			μsec	
TDIR	Dir Setupt to Step		24		μsec	± CLK ERROR
TMR	Master Reset Pulse Width	50			μsec	
TIP	Index Pulse Width	10			μsec	
TWF	Write Fault Pulse Width	20			μsec	



MISCELLANEOUS TIMING

*FROM STEP RATE TABLE

NOTES:

1. Pulse width on RAW READ (Pin 27) is normally 100-300 ns. However, pulse may be any width pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 600 ns for MFM at CLK = 1 MHz and 1200 ns for FM at 1 MHz.
2. tbc should be 4 μs, nominal in MFM and 8 μs nominal in FM.
3. RCLK may be high or low during $\overline{\text{RAW READ}}$ (Polarity is unimportant).
4. All timing readings at V_{OL} = .8V & V_{OH} = 2.0V.

Table 4. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TROO}}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

V_{DD} with repect to V_{SS} (ground): + 15 to − 0.3V
Voltage to any input with respect to V_{SS} = + 15 to − 0.3V
I_{CC} = 60 MA (35 MA nominal)
I_{DD} = 15 MA (10 MA nominal)

C_{IN} & C_{OUT} = 15 pF max with all pins grounded except one under test.
Operating temperature = 0°C to 70°C
Storage temperature = − 55°C to + 125°C

OPERATING CHARACTERISTICS (DC)

TA = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = 0V, V_{CC} = + 5V ± .25V

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	CONDITIONS
I_{IL}	Input Leakage		10	μA	$V_{IN} = V_{DD}$**
I_{OL}	Output Leakage		10	μA	$V_{OUT} = V_{DD}$
V_{IH}	Input High Voltage	2.6		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.8		V	I_O = − 100 μA
V_{OL}	Output Low Voltage		0.45	V	I_O = 1.0 mA
P_D	Power Dissipation		0.6	W	

**Leakage conditions are for input pins without internal pull-up resistors. Pins 22, 23, 33, 36, and 37 have pullup resistors. See Tech Memo #115 for testing purposes.

See page 725 for ordering information.

Printed in U.S.A.

FD1771-01 Floppy Disk Formatter/Controller

FEATURES

- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- READ MODE
  Single/Multiple Sector Write with Automatic Sector Search or Entire Track Read
  Selectable 128 Byte or Variable Length Sector
- WRITE MODE
  Single/Multiple Sector Write with Automatic Sector Search
  Entire Track Write for Diskette Formatting
- PROGRAMMABLE CONTROLS
  Selectable Track-to-Track Stepping Time
  Selectable Head Settling and Head Engage Times
  Selectable Three Phase or Step and Direction and Head Positioning Motor Controls
- SYSTEM COMPATIBILITY
  Double Buffering of Data 8-Bit Bi-Directional Bus for Data, Control and Status
  DMA or Programmed Data Transfers
  All Inputs and Outputs are TTL Compatible

APPLICATIONS

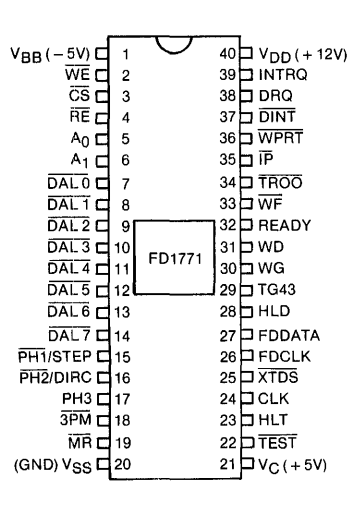
- FLOPPY DISK DRIVE INTERFACE
- SINGLE OR MULTIPLE DRIVE CONTROLLER/FORMATTER
- NEW MINI-FLOPPY CONTROLLER

GENERAL DESCRIPTION

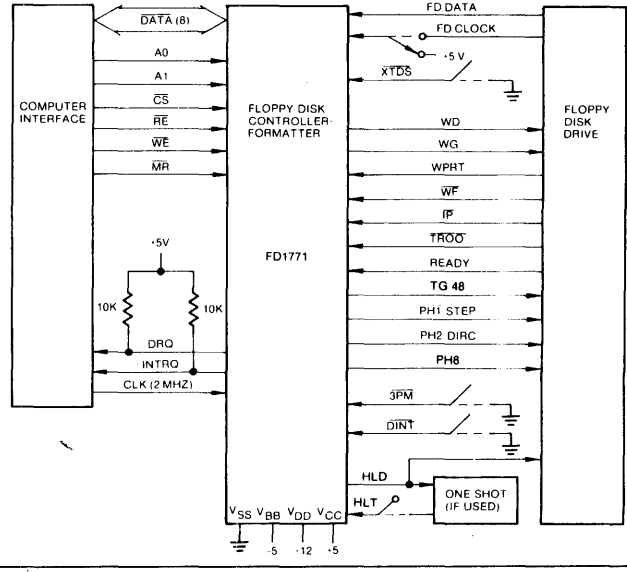
The FD1771 is a MOS/LSI device that performs the functions of a Floppy Disk Controller/Formatter. The device is designed to be included in the disk drive electronics, and contains a flexible interface organization that accommodates the interface signals from most drive manufacturers. The FD1771 is compatible with the IBM 3740 data entry system format.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The FD1771 is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD1771 is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs. The A and B suffixes are for ceramic and plastic packages, respectively.



PIN CONNECTIONS



FD1771 SYSTEM BLOCK DIAGRAM

PIN OUTS

Pin No.	Pin Name	Symbol	Function
1	Power Supplies	V_{BB}/NC	-5V
19	MASTER RESET	$\overline{MR}$	A logic low on this input resets the device and loads "03" into the command register. The Not Ready (Status bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high, a Restore Command is executed, regardless of the state of the Ready signal from the drive.
20		V_{SS}	Ground
21		V_{CC}	+5V
40		V_{DD}	+12V
Computer Interface			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5, 6	REGISTER SELECT LINES	A_0, A_1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: A_1 A_0 $\overline{RE}$ $\overline{WE}$ 0 0 Status Register Command Register 0 1 Track Register Track Register 1 0 Sector Register Sector Register 1 1 Data Register Data Register
7-14	DATA ACCESS LINES	$\overline{DAL0}$-$\overline{DAL7}$	Eight bit inverted bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by $\overline{WE}$ or a transmitter enabled by $\overline{RE}$.
24	CLOCK	CLK	This input requires a free-running 2 MHz ± 1% square wave clock for internal timing reference.
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operation, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register. Use 10K pull-up resistor to +5.
Floppy Disk Interface:			
15	Phase 1/Step	$\overline{PH1}$/STEP	If the $\overline{3PM}$ input is a logic low the three-phase motor control is selected and $\overline{PH1}$, $\overline{PH2}$, and PH3 outputs form a one active low signal out of three. $\overline{PH1}$ is active low after $\overline{MR}$. If the $\overline{3PM}$ input is a logic high the step and direction motor control is selected. The step output contains a 4 usec high signal for each step and the direction output is active high when stepping in; active low when stepping out.
16	Phase 2/Direction	$\overline{PH2}$/DIRC	
17	Phase 3	PH3	
18	3-Phase Motor Select	$\overline{3PM}$	

Pin No.	Pin Name	Symbol	Function
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user.
23	HEAD LOAD TIMING	HLT	The HLT input is sampled after 10 ms. When a logic high is sampled on the HLT input the head is assumed to be engaged.
25	$\overline{\text{EXTERNAL DATA SEPARATION}}$	$\overline{\text{XTDS}}$	A logic low on this input selects external data separation. A logic high or open selects the internal data separator.
26	FLOPPY DISK CLOCK (External Separation)	FDCLOCK	This input receives the externally separated clock when $\overline{\text{XTDS}}$ = 0. If $\overline{\text{XTDS}}$ = 1, this input should be tied to a logic high.
27	FLOPPY DISK DATA	FDDATA	This input receives the raw read disk data if $\overline{\text{XTDS}}$=1, or the externally separated data if $\overline{\text{XTDS}}$=0.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	Track Greater than 43	TG43	This output informs the drive that the Read-Write head is positioned between tracks44-76. This output is valid only during Read and Write commands.
30	WRITE GATE	WG	This output is made valid when writing is to be performed on the diskette.
31	WRITE DATA	WD	This output contains both clock and data bits of 500 ns duration.
32	Ready	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low, the Read or Write operation is not performed and an interrupt is generated. A Seek operation is performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$	$\overline{\text{WF}}$	This input detects wiring faults indications from the drive. When WG=1 and $\overline{\text{WF}}$ goes low, the current Write command is terminated and the Write Fault status bit is set. The $\overline{\text{WF}}$ input should be made inactive (high) when WG becomes inactive.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD1771 that the Read-Write head is positioned over Track 00 when a logic low.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	Input, when low for a minimum of 10 usec, informs the FD1771 when an index mark is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write command is received. A logic low terminates the command and sets the Write Protect status bit.
37	$\overline{\text{DISK INITIALIZATION}}$	$\overline{\text{DINT}}$	The iput is sampled whenever a Write Track command is received. If $\overline{\text{DINT}}$=0, the operation is terminated and the Write Protect status bit is set.

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 4. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register: This 8-bit register assembles serial data from the Read Data input (FDDATA) duriing Read operations and transfers serial data to the Write Data output during Write operations.

Data Register: This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command, the Data Register holds the address of the desired Track position. This register can be loaded from the DAL and gated onto the DAL under processor control.

Track Register: This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when this device is busy.

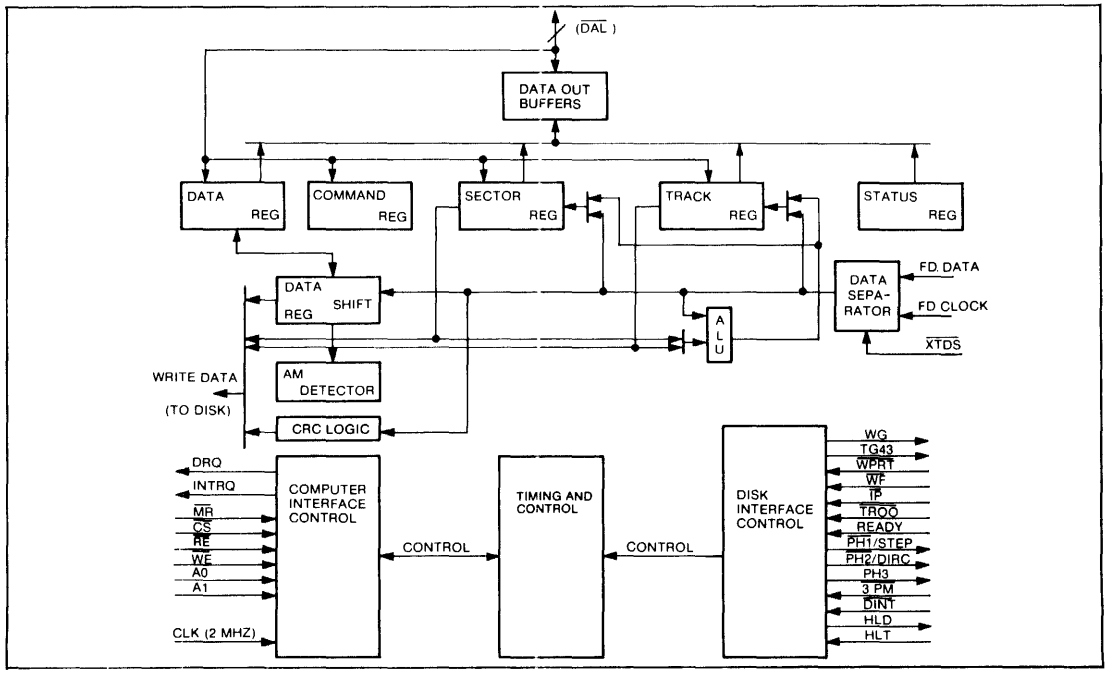
Sector Register (SR): This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR): This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the execution of the current command is to be overridden. This latter action results in an interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR): This 8-bit register holds device Status information. The meaning of the Status bits are a function of the contents of the Command Register. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic: This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.



FD1771 BLOCK DIAGRAM

Arithmetic/Logic Unit (ALU): The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

AM Detector: The Address Mark detector is used to detect ID, Data, and Index address marks during Read and Write operations.

Timing and Control: All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from a 2.0 MHz external crystal clock.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the FD1771. The DAL are three-state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable (RE) are active (low logic state) or act as input receivers when CS and Write Enable (WE) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and CS is made low. The least-significant address bits A1 and A0, combined with the signals RE during a Read operation or WE during a Write operation are interpreted as selecting the following registers:

A1	A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD1771 and the Processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

The Lost Data bit and certain other bits in the Status Register will activate the interrupt request (INTRQ). The interrupt line is also activated with normal completion or abnormal termination of all controller operations. The INTRQ signal remains active until reset by reading the Status Register to the processor or by the loading of the Command Register. In addition, the INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The Floppy Disk interface consists of head positioning controls, write gate controls, and data transfers. A 2.0 MHz ± 1% square wave clock is requred at the CLK input for internal control timing (may be 1.0 MHz for mini floppy).

HEAD POSITIONING

Four commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step, an additional 10 milliseconds of head settling time takes place. The four programmable stepping rates are tabulated below.

The rates (shown in Table 1) can be applied to a Three-Phase Motor or a Step-Direction Motor through the device interface. When the $\overline{3PM}$ input is connected to ground, the device operates with a three-phase motor control interface, with one active low signal per phase on the three output signals $\overline{PH1}$, $\overline{PH2}$, and PH3. The stepping sequence, when stepping in, is Phases 1-2-3-1, and when stepping out, Phases 1-3-2-1. Phase 1 is active low after Master Reset. Note: PH3 needs an inverter if used.

The Step-Direction Motor Control interface is activated by leaving input $\overline{3PM}$ open or connecting it to +5V. The Phase 1 pin $\overline{PH1}$ becomes a Step pulse of 4 microseconds width. The Phase 2 pin $\overline{PH2}$ becomes a direction control with a high voltage on this pin indicating a Step In, and a low voltage indicating a Step Out. The Direction output is valid a minimum of 24 μs prior to the activation of the Step pulse.

When a Seek, Step or Restore command is executed, an optional verification of Read-Write head position can be performed by setting bit 2 in the command word to a logic 1. The verification operation begins at the end of the 10 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete. If track comparison is not

made but the CRC checks, an interrupt is generated, the Seek Error status (Bit 4) is set and the Busy status bit is reset.

Table 1. STEPPING RATES

r_1 r_0	1771-X1 CLK = 2 MHz $\overline{TEST}$ = 1	1771-X1 CLK = 1 MHz $\overline{TEST}$ = 1	1771 or – X1 CLK = 2 MHz $\overline{TEST}$ = 0	1771 or – X1 CLK = 1 MHz $\overline{TEST}$ = 0
0 0	6ms	12ms	Approx. 400μs*	Approx. 800μs*
0 1	6ms	12ms		
1 0	10ms	20ms		
1 1	20ms	40ms		

*For exact times consult WDC.

The Head Load (HLD) output controls the movement of the read/write head against the disk for data recording or retrieval. It is activated at the beginning of a Read, Write (E Flag On) or Verify operation, or a Seek or Step operation with the head load bit, h, a logic one remains activated until the third index pulse following the last operation which uses the read/write head. Reading or Writing does not occur until a minimum of 10 msec delay after the HLD signal is made active. If executing the type 2 commands with the E flag off, there is no 10 msec delay and the head is assumed to be engaged. The delay is determined by sampling of the Head Load Timing (HLT) input after 10 msec. A high state input, generated from the Head Load output transition and delayed externally, identifies engagement of the head against the disk. In the Seek and Step commands, the head is loaded at the start of the command execution when the h bit is a logic one. In a verify command the head is loaded after stepping to the destination track on the disk whenever the h bit is a logic zero.

DISK READ OPERATION

The 2.0 MHz external clock provided to the device is internally divided by 4 to form the 500 kHz clock rate for data transfer. When reading data from a diskette this divider is synchronized to transitions of the Read Data (FDDATA) input. When a transition does not occur on the 500 kHz clock active state, the clock divider circuit injects a clock to maintain a continuous 500 kHz data clock. The 500 kHz data clock is further divided by 2 internally to separate the clock and information bits. The divider is phased to the information by the detection of the address mark.

In the internal data read and separation mode the Read Data input toggles from one state to the opposite state for each logic one bit of clock or information. This signal can be derived from the amplified, differentiated, and sliced Read Head signal, or by the output of a flip-flop toggling on the Read Data pulses. This input is sampled by the 2 MHz clock to detect transitions.

The chip can also operate on externally separated data, as supplied by methods such as Phase Lock loop, One Shots, or variable frequency oscillators. This is accomplished by grounding the External Data Separator ($\overline{XTDS}$) INPUT. When the Read Data input makes a high-to-low transition, the information input to the FDDATA line is clocked into the Data Shift Register. The assembled 8-bit data from the Data Shift Register are then transferred to the Data Register.

The normal sector length for read or Write operations with the IBM 3740 format is 128 bytes. This format or binary multiples of 128 bytes will be adopted by setting a logic 1 in Bit 3 of the Read and Write commands. Additionally, a variable sector length feature is provided which allows an indicator recorded in the ID Field to control the length of the sector. Variable sector lengths can be read or written in Read or Write commands, respectively, by setting a logic 0 in Bit 3 of the command word. The sector length indicator specifies the number of 16 byte groups or 16 x N, where N is equal to 1 to 256 groups. An indicator of all zeroes is interpreted as 256 sixteen byte groups.

DISK WRITE OPERATION

After data is loaded from the processor into the Data Register, and is transferred to the Data Shift Register, data will be shifted serially through the Write Data (WD) output. Interlaced with each bit of data is a positive clock pulse of 0.5 μsec duration. This signal may be used to externally toggle a flip-flop to control the direction of Write Current flow.

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing, the first data byte must be loaded into the Data Register in response to a Data Request from the FD1771 before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The $\overline{\text{Write Fault}}$ input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD1771 terminates the current command, and sets the $\overline{\text{Write Fault}}$ bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the Write Gate output becomes inactive.

Whenever a Read or Write command is received the FD1771 samples the READY input. If this input is logic low the command is not executed and an interrupt is generated. The Seek or Step commands are performed regardless of the state of the READY input.

COMMAND DESCRIPTION

The FD1771 will accept and execute eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault-free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 2.

TYPE 1 COMMANDS

The Type 1 Commands include the RESTORE, SEEK, STEP, STEP-IN, and STEP-OUT commands. Each of the Type 1 Commands contain a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 1, page 4.

The Type 1 Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h=1, the head is loaded at the beginning of the command (HLD output is made active). If h=0, HLD is deactivated.

Table 2. COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	1	0	$\bar{s}$
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_4

Note: Bits shown in TRUE form.

Table 3. FLAG SUMMARY

TYPE I

h = Head Load flag (Bit 3)
- h = 1, Load head at beginning
- h = 0, Do not load head at beginning

V = Verify flag (Bit 2)
- V = 1, Verify on last track
- V = 0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)
- Refer to Table 1 for rate summary

u = Update flag (Bit 4)
- u = 1, Update Track register
- u = 0, No update

Table 4. FLAG SUMMARY

TYPE II

m = Multiple Record flag (Bit 4)
- m = 0, Single Record
- m = 1, Multiple Records

b = Block length flag (Bit 3)
- b = 1, IBM format (128 to 1024 bytes)
- b = 0, Non-IBM format (16 to 4096 bytes)

a_1a_0 = Data Address Mark (Bits 1-0)
- a_1a_0 = 00, FB (Data Mark)
- a_1a_0 = 01, FA (User defined)
- a_1a_0 = 10, F9 (User defined)
- a_1a_0 = 11, F8 (Deleted Data Mark)

Table 5. FLAG SUMMARY

TYPE III

s = Synchronize flag (Bit 0)
- $\bar{s}$ = 0, Synchronize to AM
- $\bar{s}$ = 1, Do Not Synchronize to AM

TYPE IV

Ii = Interrupt Condition flags (Bits 3-0)
- I_0 = 1, Not Ready to Ready Transition
- I_1 = 1, Ready to Not Ready Transition
- I_2 = 1, Index Pulse
- I_3 = 1, Immediate interrupt

E = Enable HLD and 10 msec Delay
- E = 1, Enable HLD, HLT and 10 msec Delay
- E = 0, Head is assumed Engaged and there is no 10 msec Delay

Once the head is loaded, the head will remain engaged until the FD1771 receives a command that specifically disengages the head. If the FD1771 does not receive any commands after two revolutions of the disk, the head will be automatically disengaged (HLD made inactive). The Head Load Timing Input is sampled after a 10 ms delay, when reading or writing on the disk is to occur.

The Type 1 Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V=1, a verification is performed; if V=0, no verification is performed.

During verification, the head is loaded and after an internal 10 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID Field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the BUSY status bit is reset. If there is not a match but there is

valid ID CRC, an interrupt is generated, the Seek Error status bit (Status Bit 4) is set and the BUSY status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status Bit 3), and the next encountered ID Field is read from the disk for the verification operation. If an ID Field with a valid CRC cannot be found after two revolutions of the disk, the FD1771 terminates the operation and sents an interrupt (INTRQ).

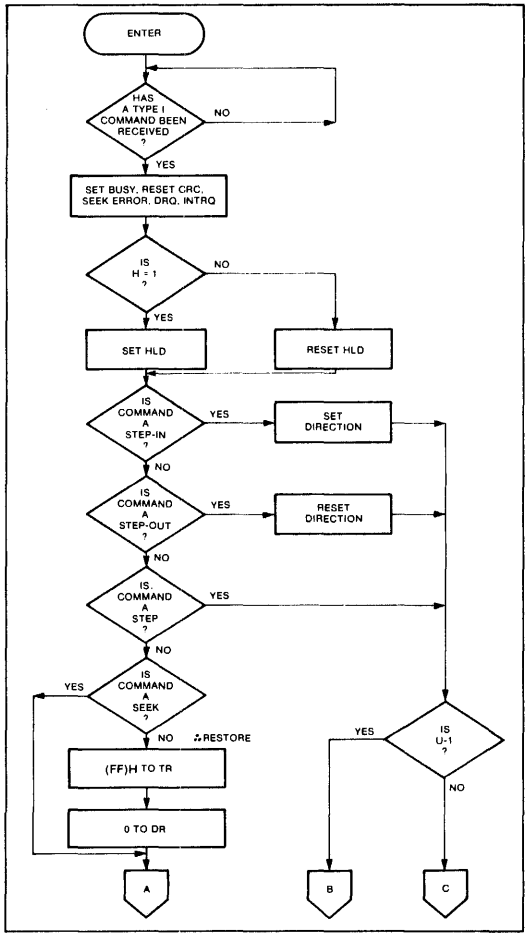
The STEP, STEP-IN, and STEP-OUT commands contain an UPDATE flag (U). When U=1, the track register is updated by one for each step. Whe U=0, the track register is not updated.

RESTORE (SEEK TRACK 0)

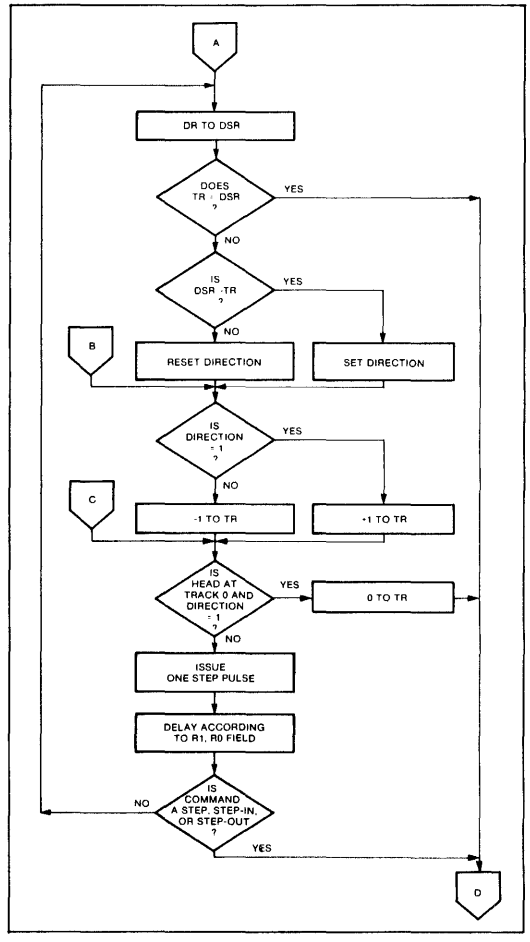
Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 17) at a rate specified by the r_1r_0 field are issued until the $\overline{TR00}$ input is activated. At this time the TR is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD1771 terminates operation, interrupts, and sets the Seek error status bit. Note that the RESTORE command is executed when $\overline{MR}$ goes from an active to an inactive state. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD1771 will update the



TYPE I COMMAND FLOW

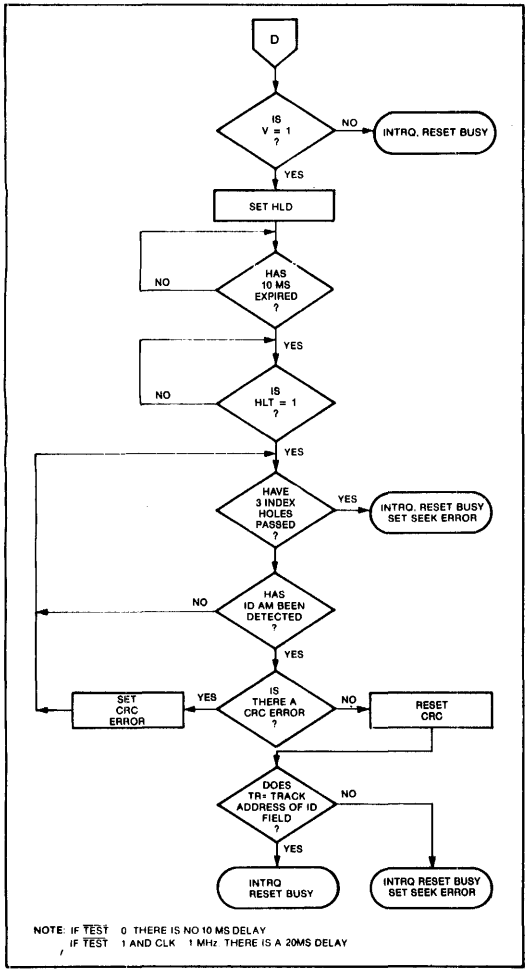


TYPE I COMMAND FLOW

Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the data register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD1771 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the u flag is on, the TR is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.



TYPE I COMMAND FLOW

STEP-IN

Upon receipt of this command, the FD1771 issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD1771 issues one stepping pulse in the direction towards track 0. If the u flag is on, the TR is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands include the Read Sector(s) and Write Sector(s) commands. Prior to loading the Type II command into the COMMAND REGISTER, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the Busy status bit is set. If the E flag=1 (this is the normal case), HLD is made active and HLT is sampled after a 10 msec delay. If the E flag is 0, the head is assumed to be engaged and there is no 10 msec delay. The ID field and the Data Field format are shown below.

When an ID field is located on the disk, the FD1771 compares the track number of the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending on the command. The FD1771 must find an ID field with a track number, Sector number, and CRC within two revolutions of the disk; otherwise, the Record Not Found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Each of the Type II Commands contain a (b) flag which in conjunction with the sector length field contents of the ID determines the length (number of characters) of the Data field.

For IBM 3740 compatibility, the b flag should equal 1. The numbers of bytes in the data field (sector) is then 128×2^n where n = 0, 1, 2, 3.

GAP	ID AM	TRACK NUMBER	ZERO	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD									DATA FIELD			

IDAM = ID Address Mark — DATA = $(FE)_{16}$ CLK = $(C7)_{16}$

Data AM = Data Address Mark — DATA = (F8, F9, FA, or FB), CLK = $(C7)_{16}$

For b = 1

Sector Length Field (Hex)	Number of Bytes in Sector (Decimal)
00	128
01	256
02	512
03	1024

When the b flag equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field as shown below.

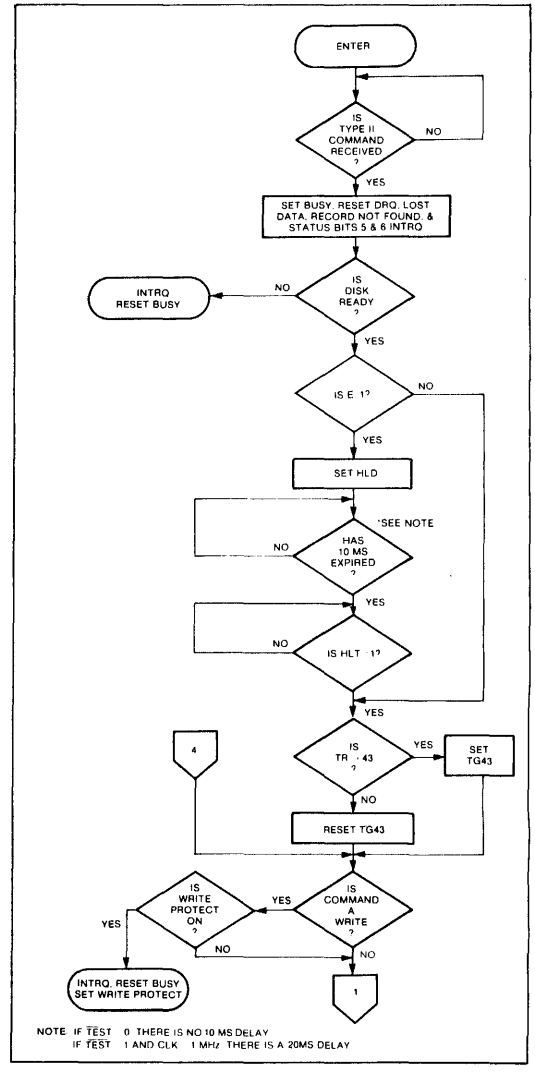
For b = 0

Sector Length Field (Hex)	Number of Bytes in Sector (Decimal)
01	16
02	32
03	48
04	64
•	•
•	•
•	•
FF	4080
00	4096

Each of the Type II commands also contain a (m) flag which determines if the multiple records (sectors) are to be read or written, depending upon the command. If m=0 a single sector is read or written and an interrupt is generated at the completion of the command. If m=1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD1771 will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the command register, which terminated the command and generates an interrupt.

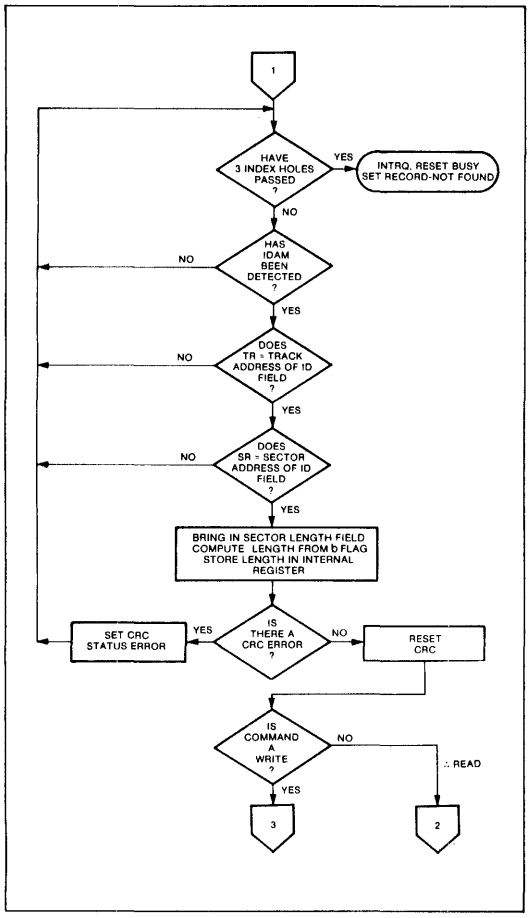
READ COMMAND

Upon receipt of the Read command, the head is loaded, the BUSY status bit set, and when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 28 bytes of the correct field; if not, the Record Not Found status bit is set and the operation is terminated. When the first character or byte of the data field has been

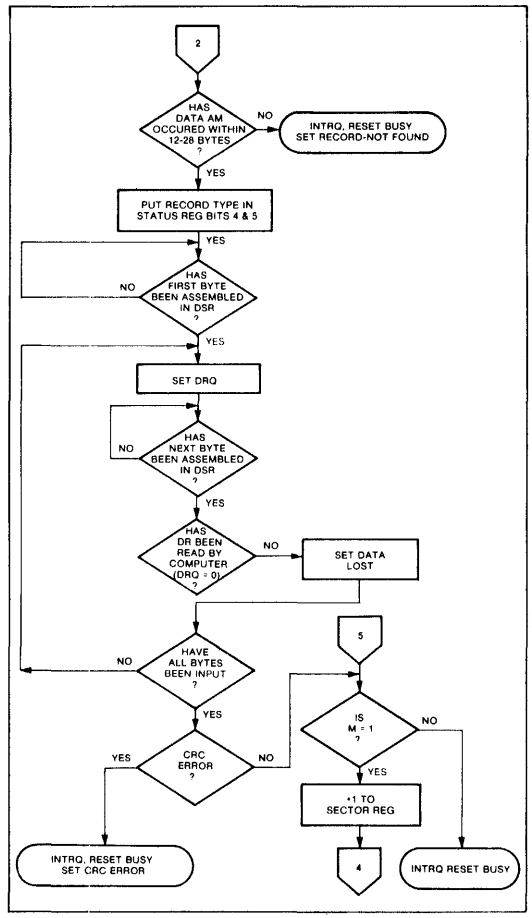


TYPE II COMMAND FLOW

shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred that character is lost and the



TYPE II COMMAND FLOW



TYPE II COMMAND FLOW

Lost Data status bit is set. This sequence continues until the complete data field has been input to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a mulltiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bits 5 and 6) as shown below.

Status Bit 6	Status Bit 5	Data AM (Hex)
0	0	FB
0	1	FA
1	0	F9
1	1	F8

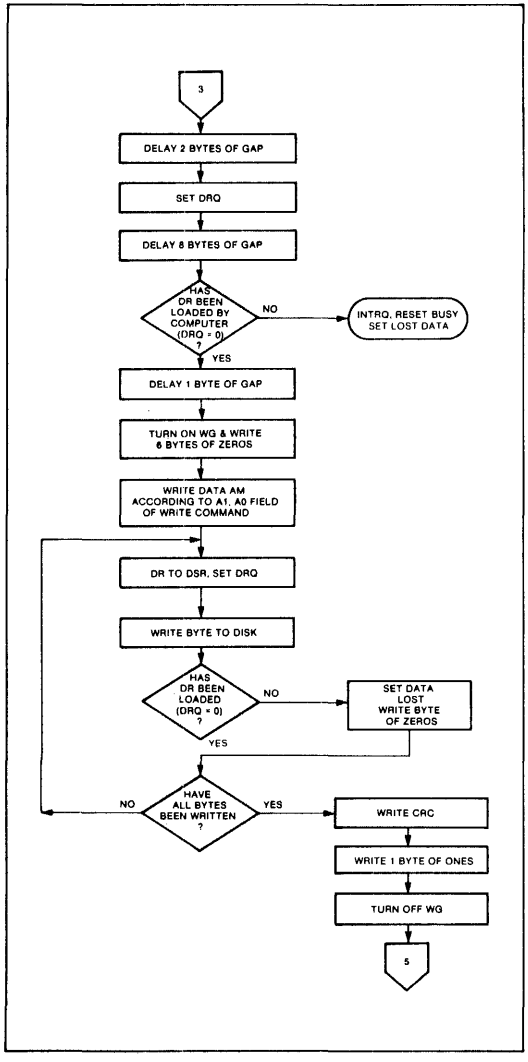
WRITE COMMAND

Upon receipt of the Write command, the head is loaded (HLD active) and the BUSY status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The FD1771 counts off 11 bytes from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the $a_1 a_0$ field of the command as shown on next page.

The FD1771 then writes the data field and generates DRQs to the computer. If the DRQ is not serviced in

a_1	a_0	Data Mark (Hex)	Clock Mark (Hex)
0	0	FB	C7
0	1	FA	C7
1	0	F9	C7
1	1	F8	C7

time for continuous writing the Lost Data status bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte gap of logic ones. The WG output is then deactivated.



TYPE II COMMAND FLOW

TYPE III COMMANDS

READ Address

Upon receipt of the Read Address command, the head is loaded and the BUSY Status bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below.

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

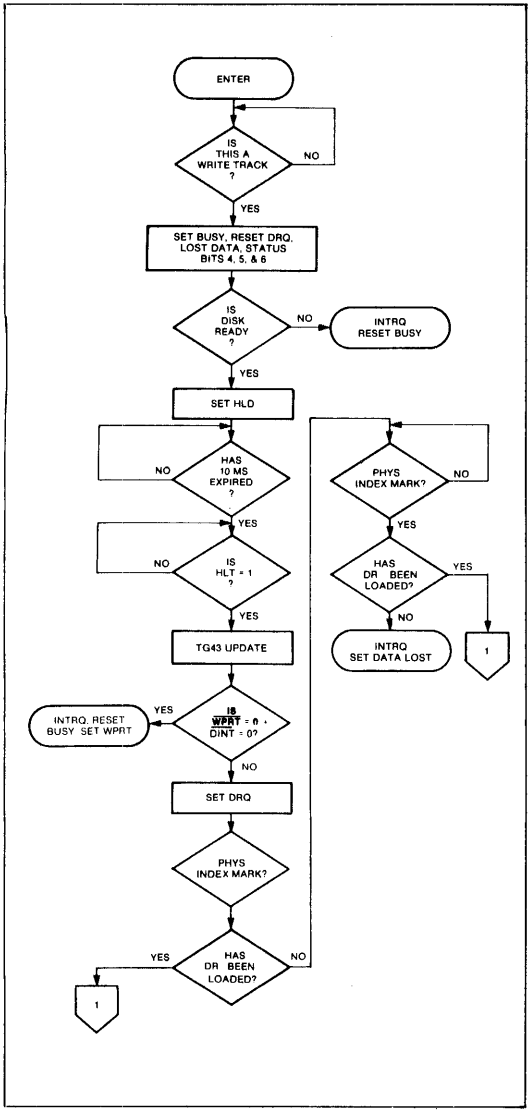
Although the CRC characters are transferred to the computer, the FD1771 checks for validity and the CRC error status bit is set if there is a CRC error. The Sector Address of the ID field is written into the Sector Register. At the end of the operation an interrupt is generated and the BUSY Status is reset.

READ TRACK

Upon receipt of the Read Track command, the head is loaded and the BUSY status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If bit 0(S) of the command is a 0, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

WRITE TRACK

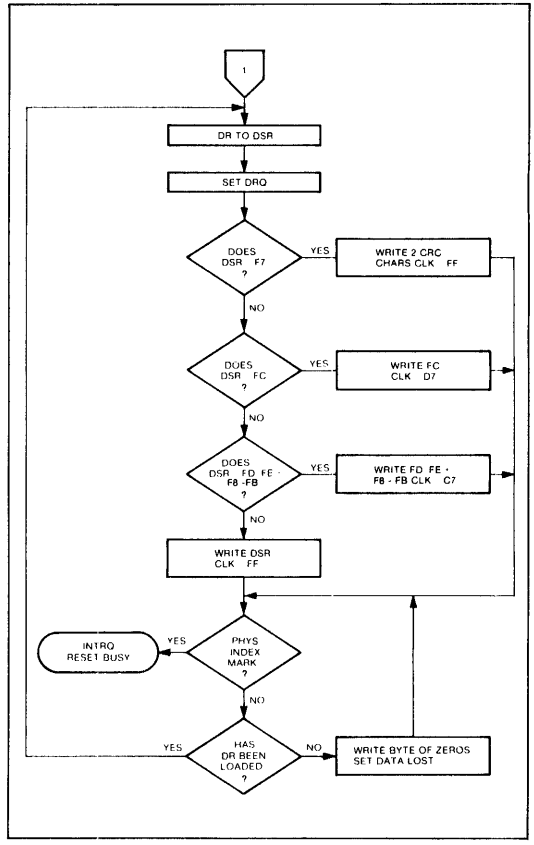
Upon receipt of the Write Track command, the head is loaded and the BUSY status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data status bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR.



TYPE III COMMAND WRITE TRACK

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN (HEX)	INTERPRETATION	CLOCK MARK (HEX)
F7	Write CRC Character	FF
F8	Data Address Mark	C7
F9	Data Address Mark	C7
FA	Data Address Mark	C7
FB	Data Address Mark	C7
FC	Index Address Mark	D7
FD	Spare	
FE	ID Address Mark	C7



TYPE III COMMAND WRITE TRACK

The Write Track Command will not execute if the $\overline{\text{DINT}}$ input is grounded; instead, the Write Protect status bit is set and the interrupt is activated. Note that one F7 pattern generates two CRC characters.

TYPE IV COMMAND

Force Interrupt

This command can be loaded into the command register at any time. If there is a current command under execution (BUSY status bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0= Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt (Requires reset, see Note)

NOTE: If I_0 - I_3 = 0, there is no interrupt generated but the current command is terminated and busy is reset. This is the only command that will clear the immediate interrupt.

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below.

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

Table 6. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	RECORD TYPE	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD ENGAGED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT	NAME	MEANING
S7	NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the READY input and logically "ored" with MR.
S6	PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{WRPT}$ input.
S5	HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4	SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3	CRC ERROR	When set, there was one or more CRC errors encountered on an unsuccessful track verification operation. This bit is reset to 0 when updated.
S2	TRACK 00	When set, indicates Read-Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{TR00}$ input.
S1	INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the IP input.
S0	BUSY	When set, command is in progress. When reset, no command is in progress.

STATUS BITS FOR TYPE II AND III COMMANDS

BIT	NAME	MEANING
S7	NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the READY input and "ored" with MR. The TYPE II and III Commands will not execute unless the drive is ready.
S6	RECORD TYPE/ WRITE PROTECT	On Read Record: It indicates the MSB of record-type code from data field address mark. On Read Track: Not Used. On any Write Track: It indicates a Write Protect. This bit is reset when updated.
S5	RECORD TYPE/WRITE FAULT	On Read Record: It indicates the LSB of record-type code from data field address mark. On Read Track: Not Used. On any Write Track: It indicates a Write Fault. This bit is reset when updated.
S4	RECORD NOT FOUND	When set, it indicates that the desired track and sector were not found. This bit is reset when updated.
S3	CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2	LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1	DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Ready operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0	BUSY	When set, command is under execution. When reset, no command is under execution.

FORMATTING THE DISK (Refer to section on Type III Commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA control with a large amount of memory. When operating under DMA with limited amount of memory, formatting is a more difficult task. This is because gaps as well as data must be provided at the computer interface.

Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the FD1771 raises the Data Request signal. At this point in time, the user loads the Data Register with desired data to be written on the disk. For every byte of information to be written on the disk, a Data Request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the Data Register is written on the disk with a clock mark of $(FF)_{16}$. However, if the FD1771 detects a data pattern on F7 through FE in the Data Register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters. As a consequence, the patterns F7 through FE must not appear in the gaps, data fields, or ID fields. Also, CRCs must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 formats with sector lengths of 128,256,512, or 1024 bytes, or may be formatted in non-IBM format with sector lengths of 16 to 4096 bytes in 16-byte increments. IBM 3740 at the present time only defines two formats. One format with 128 bytes/sector and the other with 256 bytes-/sector. The next section deals with the IBM 3740 format with 128 bytes/sector followed by a section of non-IBM formats.

IBM 3740 Formats — 128 Bytes/Sector

The IBM format with 128 bytes/sector is depicted in the Track Format figure on the following page. In order to create this format, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

	Number of Bytes	Hex Value of Byte Written
	40	00 or FF
	6	00
	1	FC (Index Mark)
*	26	00 or FF
	6	00
	1	FE (ID Address Mark)
	1	Track Number (0 through 4C)
	1	00
	1	Sector Number (1 through 1A)
	1	00
	1	F7 (two CRCs written)
	11	00 or FF
	6	00
	1	FB (Data Address Mark)
	128	Data (IBM uses E5)
	1	F7 (two CRCs written)
	27	00 or FF
	247 **	00 or FF

*Write bracketed field 26 times.
**Continue writing until FD1771 interrupts out. Approximately 247 bytes.

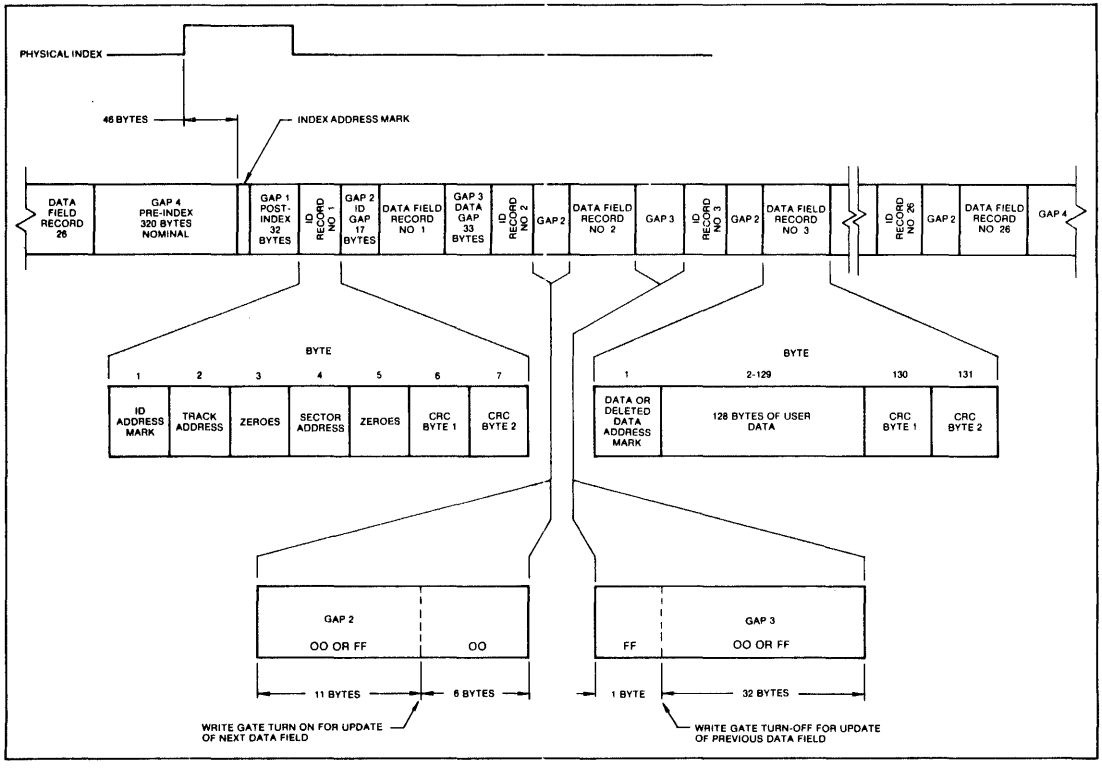
Non-IBM Formats

Non-IBM formats are very similar to the IBM formats except a different algorithm is used to ascertain the sector length from the sector length byte in the ID field. This permits a wide range of sector lengths from 16 to 4096 bytes. Refer to Section V, Type II commands with b flag equal to zero. Note that F7 through FE must not appear in the sector length byte of the ID field.

In formatting the FD1771, only two requirements regarding GAP sizes must be met. GAP 2 (i.e., the gap between the ID field and data field) must be 17 bytes of which the last 6 bytes must be zero and that every address mark be preceded by at least one byte of zeros. However, it is recommended that every GAP be at least 17 bytes long with 6 bytes of zeros. The FD1771 does not require the index address mark (i.e., DATA = FC, CLK = D7) and need not be present.

References:

1) IBM Diskette OEM Information GA21-9190-1.
2) SA900 IBM Compatibility Reference Manual — Shugart Associates.



TRACK FORMAT

ELECTRICAL CHARACTERISTICS

Maxium Ratings

V_{DD} with respect to V_{BB} (Ground)	+20 to -0.3V
Max Voltage to any input with respect to V_{BB}	+20 to -0.3V
Operating Temperature	0° C to 70° C
Storage Temperature	-55° C to +125° C

OPERATING CHARACTERISTICS (DC)

T_A = 0° C to 70° C, V_{DD} = +12.0V ± .6V,
V_{BB} = -5.0 ± .5V, V_{SS} = 0V, V_{CC} = +5V ± .25V
I_{DD} = 10 ma Nominal, I_{CC} = 30 ma Nominal,
I_{BB} = 0.4 μa Nominal

Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	μA	$V_{OUT} = V_{DD}$
V_{IH}	Input High Voltage	2.6			V	
V_{IL}	Input Low Voltage (All Inputs)			0.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = -100 uA
V_{OL}	Output Low Voltage			0.45	V	I_O = 1.0 mA

TIMING CHARACTERISTICS

TA = 0° C to 70° C, V_{DD} = +12V ± .6V,
V_{BB} = -5V ± .25V, V_{SS} = 0V, V_{CC} = +5V ± .25V

NOTE: Timings are given for 2 MHz Clock. For those timings noted, values will double when chip is operated at 1 MHz. Use 1 MHz when using mini-floppy.

Read Operations

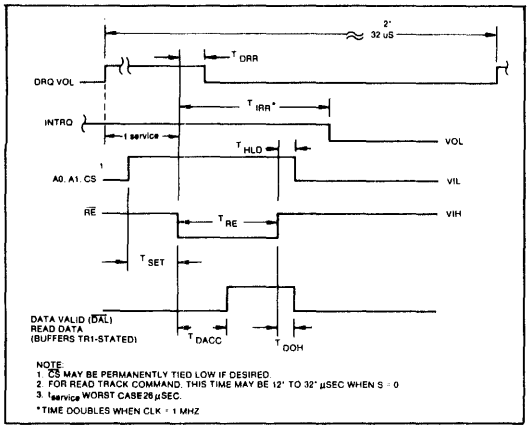
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TSET	Setup ADDR and CS to $\overline{RE}$	100			nsec	
THLD	Hold ADDR and CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	450			nsec	C_L = 25 pf
TDRR	DRQ Reset from $\overline{RE}$			750	nsec	
TIRR	INTRQ Reset from $\overline{RE}$			3000	nsec	
TDACC	Data Access from $\overline{RE}$			450	nsec	C_L = 25 pf
TDOH	Data Hold from $\overline{RE}$	50		150	nsec	C_L = 25 pf

Write Operations

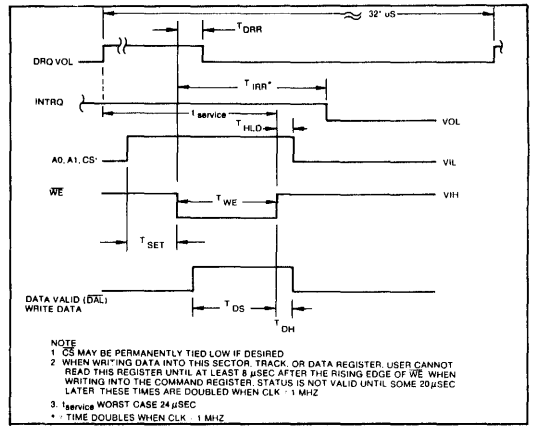
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TSET	Setup ADDR and CS to $\overline{WE}$	100			nsec	
THLD	Hold ADDR and CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	450	300		nsec	
TDRR	DRQ Reset from $\overline{WE}$			750	nsec	
TIRR	INTRQ Reset from $\overline{WE}$			3000	nsec	See Note
TDS	Data Setup to $\overline{WE}$	350			nsec	
TDH	Data Hold from $\overline{WE}$	150			nsec	

External Data Separation ($\overline{XTDS}$ = 0)

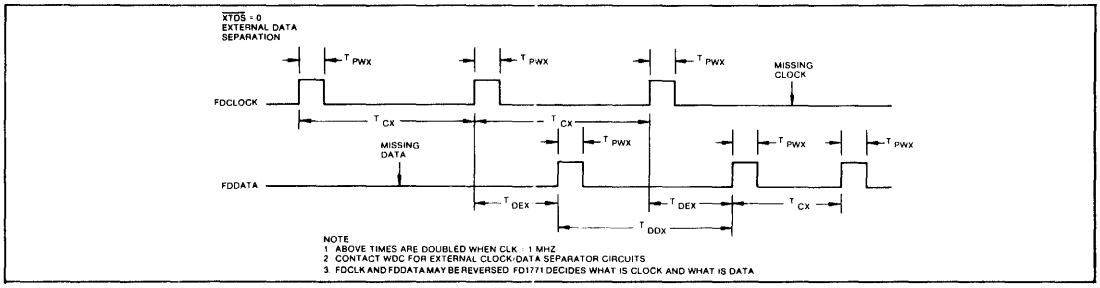
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TPWX	Pulse Width Read Data & Read Clock	150		350	nsec	
TCX	Clock Cycle External	2500			nsec	
TDEX	Data to Clock	500			nsec	
TDDX	Data to Data Cycle	2500			nsec	



READ ENABLE TIMING



WRITE ENABLE TIMING



READ TIMING ($\overline{XTDS}$ = 0)

Internal Data Separation ($\overline{XTDS}$ = 1)

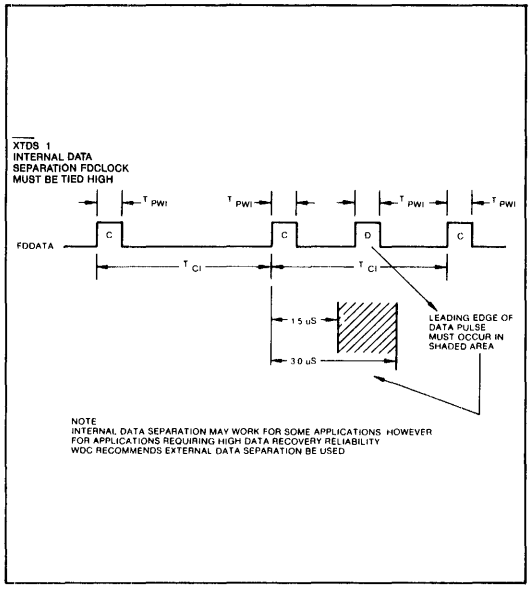
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TPWI	Pulse Width Data and Clock	150		1000	nsec	
TCI	Clock Cycle Internal	3500		5000	nsec	

Write Data Timing

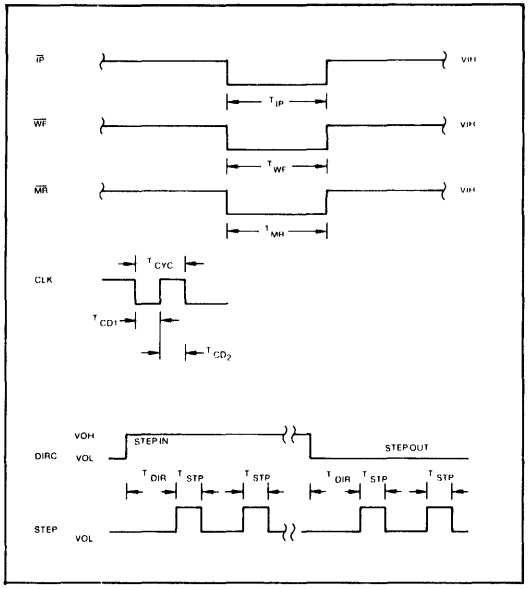
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TWGD	Write Gate to Data		1200		nsec	300 nsec ± CLK tolerance
TPWW	Pulse Width Write Data	500		600	nsec	
TCDW	Clock to Data		2000		nsec	± CLK tolerance
TCW	Clock Cycle Write		4000		nsec	± CLK tolerance
TWGH	Write Gate Hold to Data	0		100	nsec	

Miscellaneous Timing

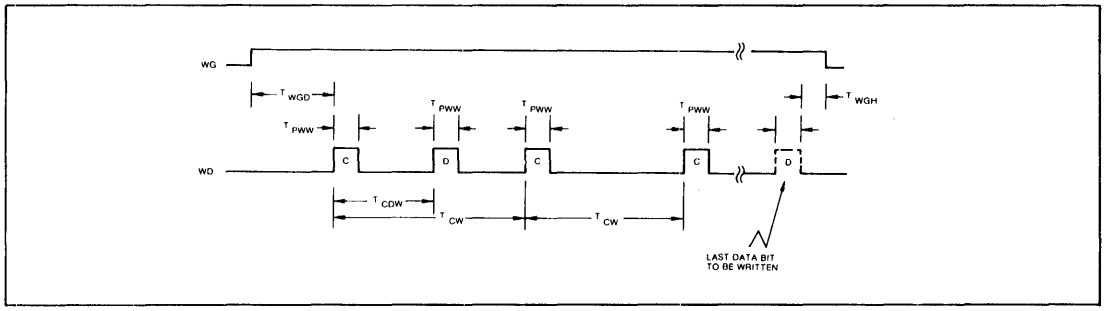
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TCD_1	Clock Duty	175			nsec	2 MHz ± 1% See Note
TCD_2	Clock Duty	210			nsec	
TSTP	Step Pulse Output	3800		4200	nsec	These times doubled when CLK = 1 MHz
TDIR	Direct Setup to Step	24			nsec	
TMR	Master Reset Pulse Width	10			nsec	
TIP	Index Pulse Width	10			nsec	
TWF	Write Fault Pulse Width	10			nsec	



READ TIMING ($\overline{XTDS}$ = 1)



MISCELLANEOUS TIMING



WRITE DATA TIMING

See page 725 for ordering information.

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1771-01 Application Notes

INTRODUCTION

The FD1771-01 Floppy Disk Formatter/Controller is a MOS/LSI device designed to ease the task of interfacing the 8" or 5¼ (mini-floppy) disk drive to a host processor. It is ideally suited for a wide range of microprocessors, providing an 8-bit bi-directional interface to the CPU for all control and data transfers. Requiring standard +12, ±5V power supplies, the 1771 is available in ceramic or plastic 40 pin dual-in-line packages.

The 1771 has been designed to be compatible with the IBM 3740 standard. This single-density Frequency Modulated (FM) recording technique, records a clock bit between a data bit serially on each track. Figure 1 illustrates how a HEX "D2" is recorded. Note that when the data bit to be written is zero, no pulse or flux transition is recorded. For the 8" drive, there are 77 tracks, with 26 sectors on each track. Each sector contains 128 bytes of data. Although there is no "standard" format for the mini-floppy, most manufacturers utilize either 35 or 40 tracks per side, wtih 16 sectors of 128 bytes each per track. Both the 8" and 5¼" formats must be soft-sectored, i.e., there are no physical holes to denote sector locations. The hard-sectored disk has been losing popularity, mainly due to the fact that the sector lengths cannot be increased.

Being soft-sector compatible, the 1771 must know where each sector begins on the track. This is performed by using Address Marks. These bytes are recorded on the disk with certain clock pulses missing, and are unique from all other data and gap bytes recorded on the track. Six distinct Address Marks can be used:

Description	Data	Clock Pattern
Index Address Mark	FC	D7
ID Address Mark	FE	C7
Data Address Mark	FB	C7
User defined	FA	C7
User Defined	F9	C7
Deleted Address Mark	F8	C7

The two "User Defined" Address Marks are unique to the 1771, and do not appear in the IBM 3740 standard. These Address Marks can be used to define the type of data i.e., "object" or "text" data, alternate sector data, or any other purpose the user chooses.

PROCESSOR INTERFACE

The 1771 contains five internal registers that can be accessed via the 8-bit DAL lines by the CPU. These registers are used to control the movement of the head, read and write sectors, and perform all other functions at the drive. Regardless of the operation performed, it must be initiated through one or more of these registers. They are selected by a proper binary code on the A0, A1 lines in conjunction with the $\overline{RE}$ and $\overline{WE}$ lines when the device is selected. The registers and their addresses are:

$\overline{CS}$	A_1	A_0	$\overline{RE}$ = 0	$\overline{WE}$ = 0
0	0	0	STATUS REG	COMMAND REG
0	0	1	TRACK REG	TRACK REG
0	1	0	SECTOR REG	SECTOR REG
0	1	1	DATA REG	DATA REG
1	X	X	Deselected	Deselected

Command Register: This is a write-only register used to send all commands to the 1771.

Status Register: This is a read-only register that must be read at the completion of every command to determine whether execution was successful. It may also be used to monitor command execution, and to sense when data is required by the drive for read or write operations.

Track Register: This R/W register holds the current position of the R/W head.

Sector Register: This R/W register holds the desired sector number for read and write commands.

Data Register: This R/W register contains the data to be read or written to a particular sector.

INTERRUPTS

There are two INTERRUPT lines for CPU use. These are the DRQ (Data Request) and INTRQ (Interrupt Request). These are active high, open drain outputs and require a pull-up resistor of 10K or greater to +5V. Both of these signals also appear in the status register as the Busy (INTRQ) and the data request (DRQ) bits. The user has the option of utilizing these hardware lines for system interrupts, or through

software by polling the status register. The choice is dependent upon the particular microprocessor and support hardware of the system.

INTRQ: This line is used to signify the completion of any command. It is reset low when a new command is loaded into the command register, or when the status register is read.

DRQ: This line is active high whenever the data register requires servicing. During a read command, it signifies that the data register contains a byte of data from the disk and may be read by the CPU. During a write command, it signifies that the data register is empty and may be loaded with the next byte to be written on the disk. The DRQ line is reset whenever the data register is read or written to. It is also reset when a new command is loaded into the command register, providing the new command is not a Forced Interrupt, and the 1771 is not busy (Busy Bit = 0).

WRITE SECTOR

With the use of the WRITE SECTOR command, the CPU can access any desired sector(s) in a track. Prior to loading this command, the R/W head of the drive must be positioned over the specific track. This can be first accomplished with the use of any of the Type I commands. Once positioned, the CPU must load the desired sector number into the sector register, then issue the command. The head will load, and the 1771 will begin searching for the correct ID field. If the correct sector and track is not found within 2 revolutions of the disk, the RECORD-NOT-FOUND bit will be set in the status register, and the command will be terminated. Once found, the 1771 will issue a DRQ in request of the first data byte to be written. Once the data register is loaded, the 1771 will issue a DRQ for each byte to be recorded, until the entire sector is written. For the 8" drive, the user must load the data register 24 microseconds after a DRQ is generated. Failure to meet this time will cause the lost data bit to be set, and a byte of zeros substituted and written on the disk.

READ SECTOR

The READ SECTOR command functions in much the same way as the WRITE SECTOR command. The sector register must again be loaded with the desired sector number, before the read command can be loaded. After the ID field has been found, the 1771 will begin generating DRQ's, with the data register being loaded with each byte of the sector field. For the 8" drive, the user must read the data register at least 26 microseconds after the DRQ is generated. Failure to meet this time will cause the lost data bit to be set in the status register, while the next assembled byte will overwrite the contents of the data register.

Both the Read and Write sector commands also contain an "m" flag for accessing multiple sectors. The sector register is incremented internally after each sector is read or written to. Eventually the sector register will exceed the physical number of sectors on the track. The user can either issue the Forced Interrupt command after the last sector, or wait for the 1771 to interrupt out. In the latter case, the RECORD-NOT-FOUND status bit will be set.

FLOPPY DISK INTERFACE

For the most part, the actual Floppy Disk Interface will consist mainly of Buffer/Drivers. Most drives manufactured today require an open collector TTL interface, with appropriate resistor terminal networks. Figure 2 shows the interface of the 1771 to a Shugart SA400 Drive. Aside from the data seperator, the interface consists mainly of 7438's and 7414 TTL gates. A 9602 one-shot is used for the desired head load delay. In this illustration, the 6800 microprocessor is used via a 6820 Peripheral Interface Adapter to control all functions of the 1771. Similarly, other parallel port devices (such as the 8255 for 8080 systems) can be used for the interface, or the 1771 may simply be tied directly to the systems data bus and control lines, providing TTL loading factors are observed.

DATA SEPERATION

The internal DATA SEPERATOR of the 1771 can be used by tying the $\overline{\text{XTDS}}$ line high, and supplying the combined clock and data pulses on the FD data line. In order to maintain an error rate better than 1 in 10^8, and external data seperator is recommended.

Since the 1771 system clock is at 2 MHz, this allows for a 500 ns resolution. The internal data window will move 500 ns with respect to the incoming data bit. On the inner tracks of the drive, the bit shift is more severe and may occasionally cause a data or clock bit to fall outside of this data window. Since the 1771 will perform up to 5 retries, this error rate may be acceptable for some applications.

When the $\overline{\text{XTDS}}$ line is forced low, the 1771 will accept seperated clock and data on the FDCLOCK and FDDATA lines. Figure 3 illustrates the timing of these signals. The actual FDCLOCK and FDDATA lines may be reversed; the 1771 will determine which line is clock and which is data when an Address Mark is detected. This feature greatly simplifies the design of the data seperator.

Figure 4 illustrates the Phase-Lock Loop method for data seperation. The circuit operates at 8 MHz, or 32 times the frequency of a received bit cell. The MC4024 VCO is used to supply the nominal clock frequency. The first 74LS161 counter provides a divide by 16 frequency and a carry to one side of the MC4044 phase detector. The other input of the MC4044 is tied to another 74LS161 counter which is affected by the incoming data stream. The output of

the phase detector is a signal proportional to the differences of the incoming pulses. This is then fed through a low pass filter, and to the input of the MC4024 to adjust the output frequency. Figures 5 thru 8 illustrate other types of data seperators. These employ the "Counter Seperator" techniques and are quite different from the Phase-Lock-Loop method. With the addition of "One-Shot" delay element or an input clock, most of the complexity of the PPL circuit can be eliminated.

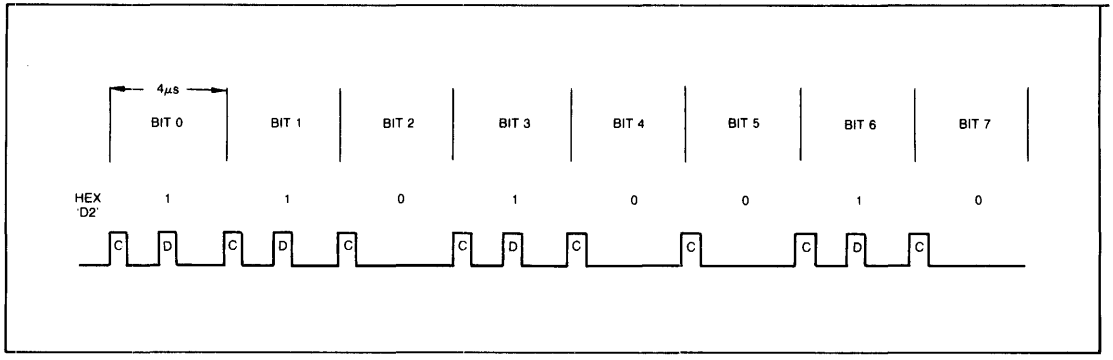


FIGURE 1. FM RECORDING.

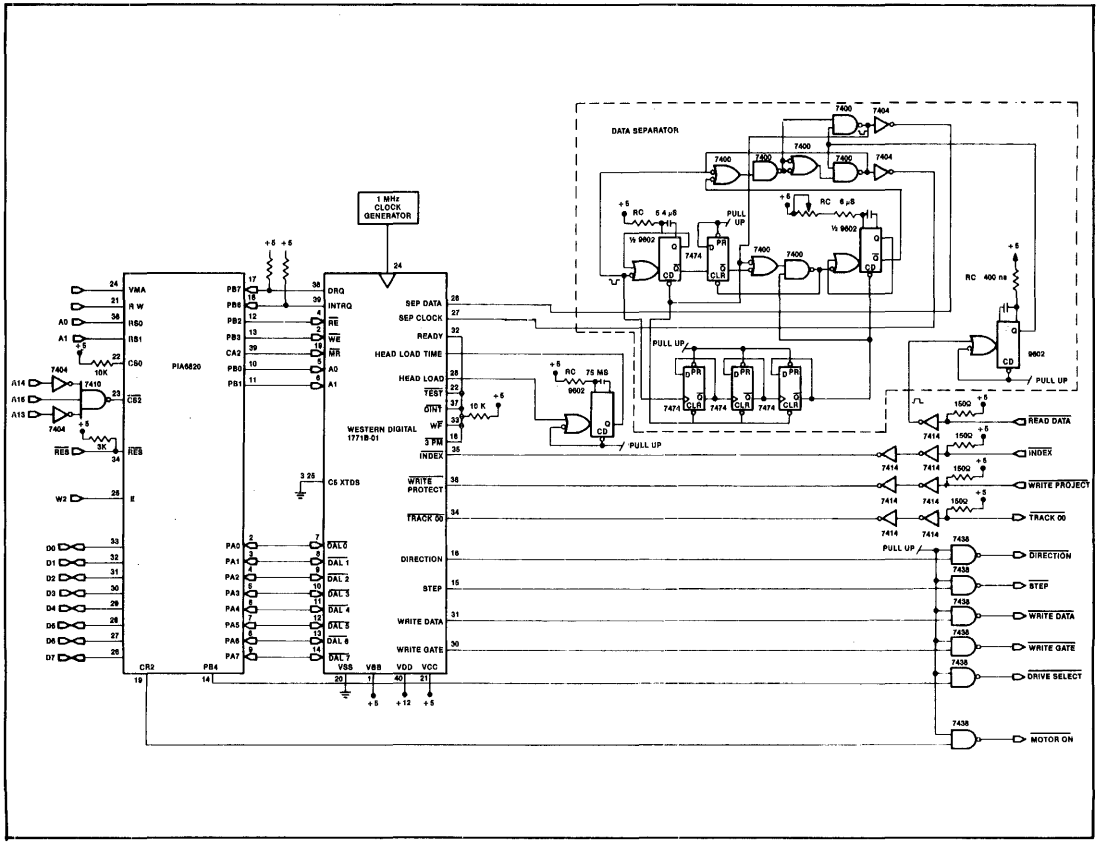


FIGURE 2. 1771 TO SHUGART SA400 DRIVE

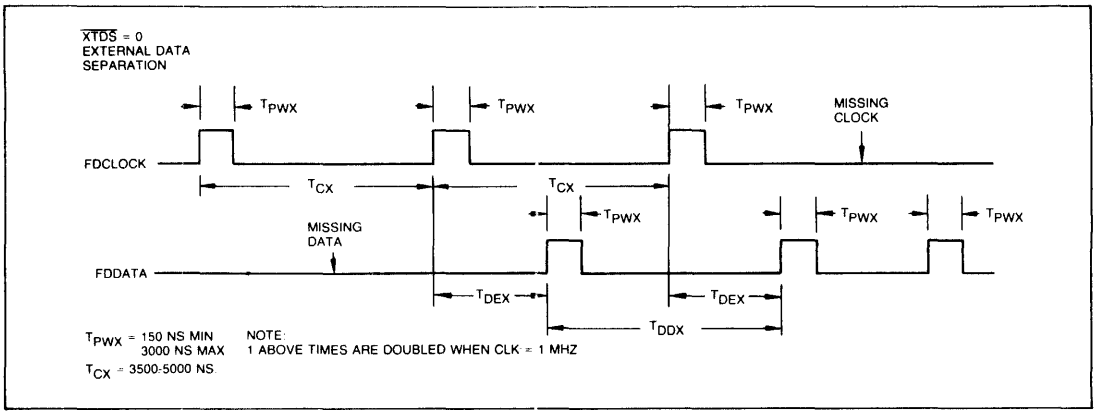


FIGURE 3. EXTERNAL DATA SEPERATOR TIMING.

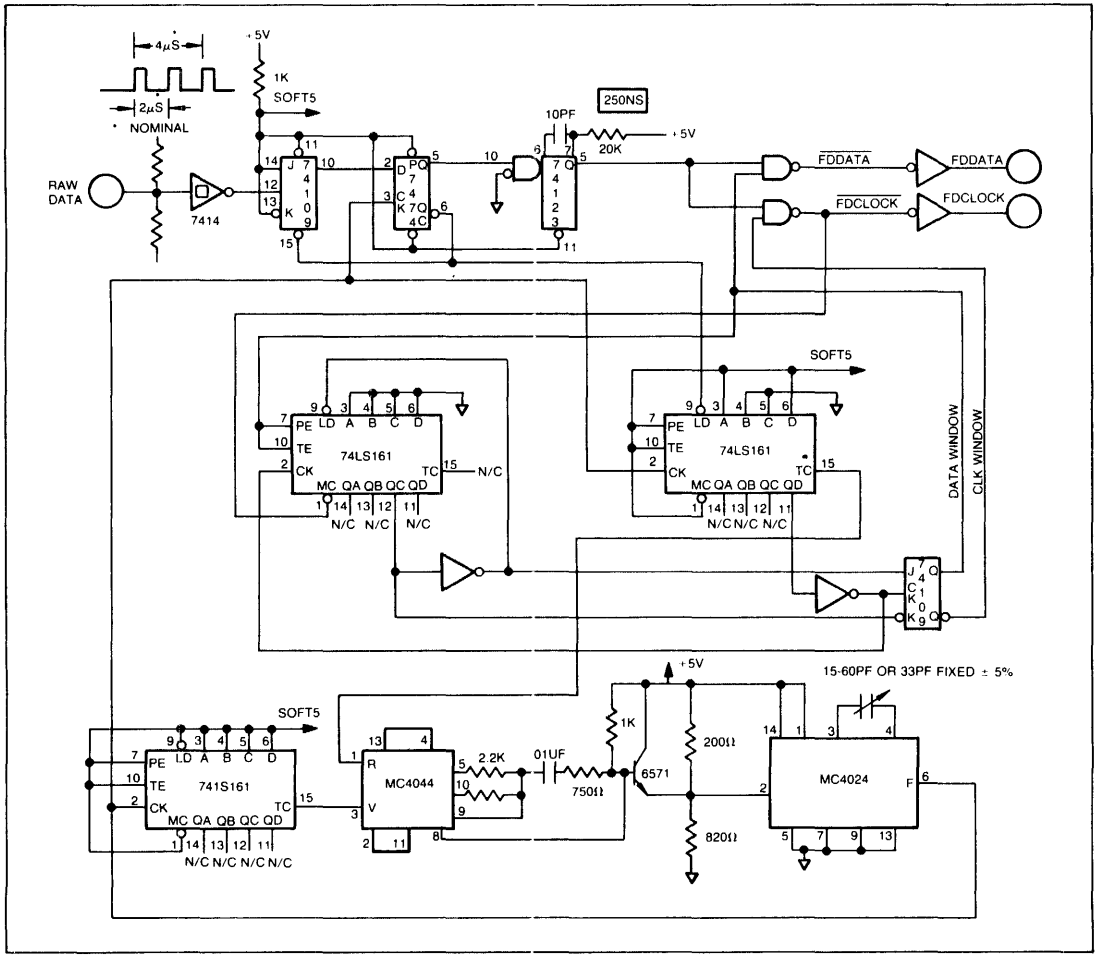


FIGURE 4. CIRCUIT PROVIDED COURTESY OF MOTOROLA AND ICOM CORPS.

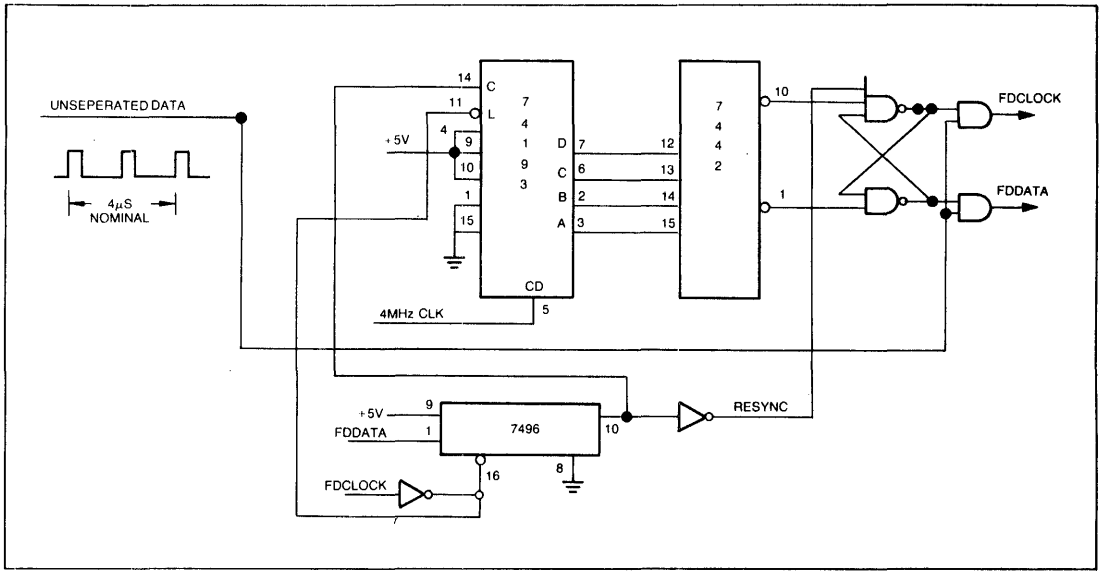


FIGURE 5. CIRCUIT PROVIDED COURTESY OF PROCESSOR APPLICATIONS LTD.

FIGURE 6.

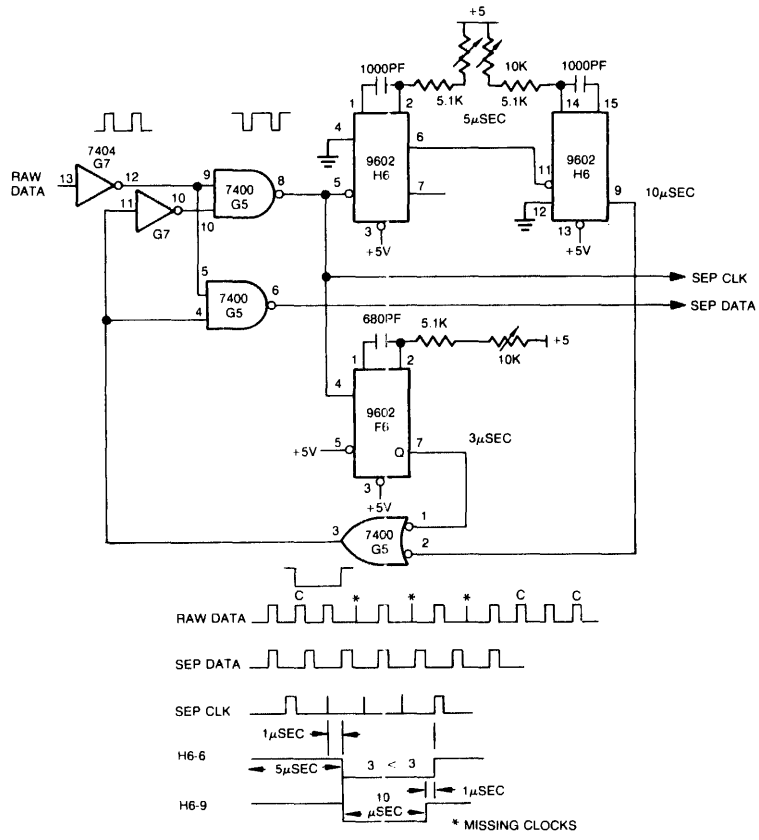
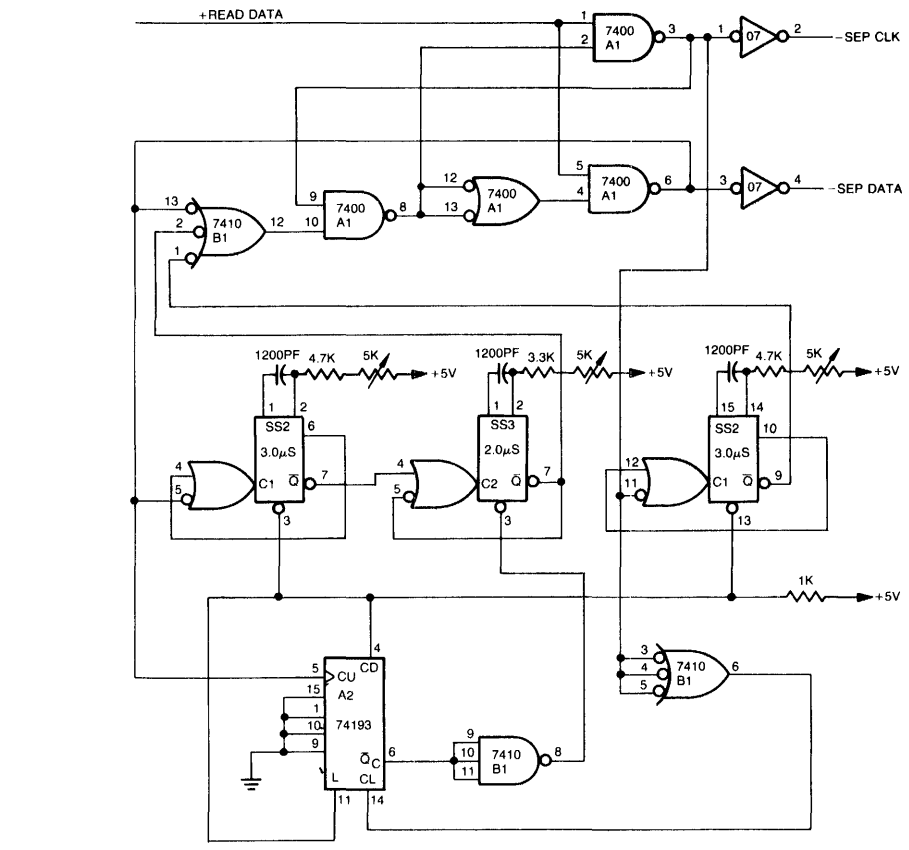


FIGURE 7. CIRCUIT PROVIDED COURTESY OF ACUTEST CORP.



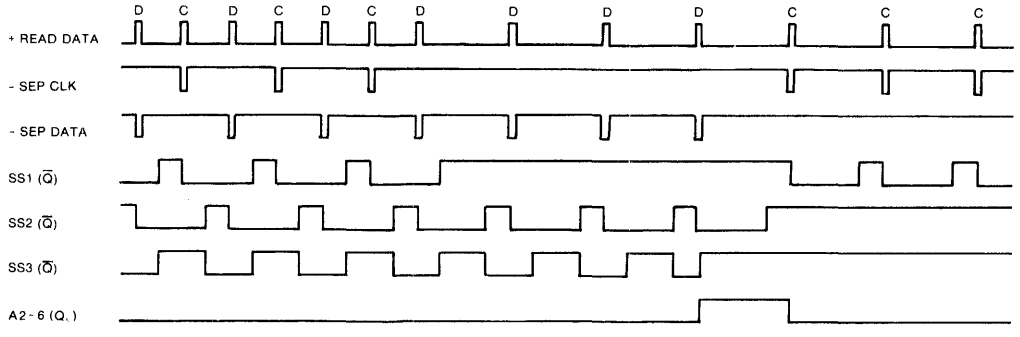


FIGURE 8. CIRCUIT PROVIDED COURTESY OF SHUGART ASSOCIATES.

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FD1781/FD1781-01 Floppy Disk Formatter/Controller

FEATURES

- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
- READ MODE
  Single/Multiple Record Read with Automatic Sector Search or Entire Track Read
  Selectable 128 Byte or Variable Length Record
- WRITE MODE
  Single/Multiple Record Write with Automatic Sector Search
  Entire Track Write for Diskette Initialization
- PROGRAMMABLE CONTROLS
  Selectable Track to Track Stepping Time
  Selectable Head Settling and Head Engage Times
- SYSTEM COMPATIBILITY
  Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  DMA or Programmed Data Transfers
  All Inputs and Outputs are TTL Compatible
  On-chip Track and Sector Registers Comprehensive Status Information

APPLICATIONS

FLOPPY DISK DRIVE INTERFACE

SINGLE OR MULTIPLE DRIVE CONTROLLER/ FORMATTER

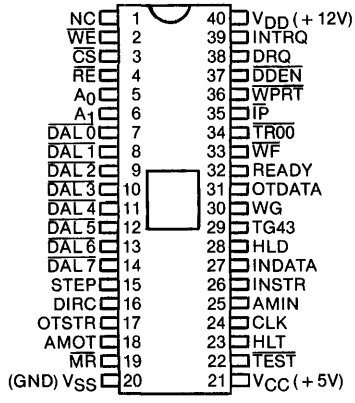
NEW MINI-FLOPPY CONTROLLER

GENERAL DESCRIPTION

The FD1781 is a MOS/LSI device that performs the functions of a Floppy Disk Controller/Formatter. The device is designed to be included in the disk drive electronics, and contains a flexible interface organization that accommodates the interface signals from most drive manufacturers. When in the single density mode the FD1781 is fully IBM-3740 compatible. In the double density mode, the type of encoding scheme is a function of the user's data recovery circuits. In this manner both M²FM or MFM is obtainable.

In Double Density Mode, the FD1781 allows 17 bytes for CAP2, while the FD1781-01 allows 34 bytes for this field. All other gap lengths can be fully defined by the user.

The FD1781 is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs.



PIN CONNECTIONS

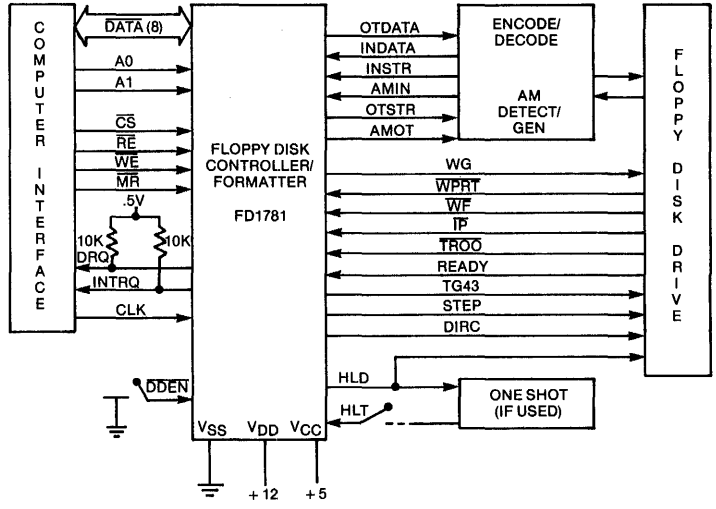


Figure 1. 1781 SYSTEM BLOCK DIAGRAM

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V
40		V_{DD}	+12V
19	MASTER RESET	$\overline{MR}$	A logic low on this input resets the device and clears the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a Restore Command is executed, regardless of the state of the Ready signal from the drive.
COMPUTER INTERFACE:			
7-14	DATA ACCESS LINES	$\overline{DAL0}$-$\overline{DAL7}$	Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by $\overline{WE}$ or a transmitter enabled by $\overline{RE}$.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
5,6	REGISTER SELECT LINES	A0,A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: A1 A0 $\overline{RE}$ $\overline{WE}$ 0 0 Status Reg Command Reg 0 1 Track Reg Track Reg 1 0 Sector Reg Sector Reg 1 1 Data Reg Data Reg
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operation, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register. Use 10K pull-up resistor to +5.
24	CLOCK	CLK	This input requires a free-running square wave clock for internal timing reference.
FLOPPY DISK INTERFACE:			
25	ADDRESS MARK DETECT IN	AMIN	Indicates to the FD1781 that an address mark has been detected. The FD1781 assumes the next three data bits defines the type of address mark encountered.
26	INPUT STROBE	INSTR	Indicates that INDATA is VALID.
27	INPUT DATA	INDATA	The external data recovery circuits present INDATA as an input to the FD1781. INDATA must be valid when INSTR is active, see timing.
31	OUTPUT DATA	OTDATA	The FD1781 presents output data and is valid when OTSTR is active.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media. The HLT

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
23	HEAD LOAD TIMING	HLT	input is sampled every 15 nsec. When a logic high is found on the HLT input the head is assumed to be engaged.
15	STEP	STEP	Step and direction motor control. The step output contains a 2 μsec high signal for each step and the direction output is active high when stepping in, active low when stepping out.
16	DIRECTION	DIRC	
17	OUTPUT STROBE	OTSTR	OTSTR when active indicates when the Output data is valid. The leading edge of OTSTR is centered about the data. (See timing) OTSTR becomes Write Data (WD) when $\overline{DDEN}$ = 1.
18	ADDRESS MARK OUT	AMOT	AMOT when active informs the external data recovery circuits to write a unique data mark in double density mode. AMOT is valid for three data bits if CLK mark = C7.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read-Write head is positioned between track 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid when writing is to be performed on the diskette.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. A Seek operation is performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{WRITE\ FAULT}$	$\overline{WF}$	This input detects writing faults indications from the drive. When WG = 1 and $\overline{WF}$ goes low the current Write command is terminated and the Write Fault status bit is set. The $\overline{WF}$ input should be made inactive (high) when WG becomes inactive.
34	$\overline{TRACK\ 00}$	$\overline{TR00}$	This input informs the FD1781 that the Read-Write head is positioned over Track 00 when a logic low.
35	$\overline{INDEX\ PULSE}$	$\overline{IP}$	Input, when low for a minimum of 10 μsec, informs the FD1781 when an index mark is encountered on the diskette.
36	$\overline{WRITE\ PROTECT}$	$\overline{WPRT}$	This input is sampled whenever a Write Command is received. A logic low terminated the command and sets the Write Protect Status bit.
37	$\overline{DOUBLE\ DENSITY}$	$\overline{DDEN}$	This pin selects either single or double density operation. When $\overline{DDEN}$ = 0, double density is selected. When $\overline{DDEN}$ = 1, single density is selected.
22	$\overline{TEST}$	$\overline{TEST}$	This input is used for testing purposes only and should be tied to +5V or left open by the user.

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated above. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input (INDATA) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register can be loaded from the DAL and gated onto the DAL under processor control.

Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when this device is busy.

Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the execution of the current command is to be overridden. This latter action results in an interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits are a function of the contents of the Command Register. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control — All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD1781 has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 0 double density is assumed. When $\overline{DDEN}$ = 1, single density is assumed. During disk read operations, the user must provide both data recovery and address mark detection circuits external to FD1781 in both single and double density modes. Thus for disk read operations, the user must provide as an input to the FD1781 Data (INDATA) a strobe to indicate when the data is valid (INSTR) and address mark detect (AMIN). During disk write operations and in the double density mode, the FD1781 provides as outputs Data (OTDATA), a strobe to indicate validity (OTSTR) and Address Mark Out (AMOT). During disk write operation and in the single density mode, OTSTR becomes Write Data (WD) which is exactly the same as in the FD1771.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the FD1781. The DAL are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The least-significant address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1	A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

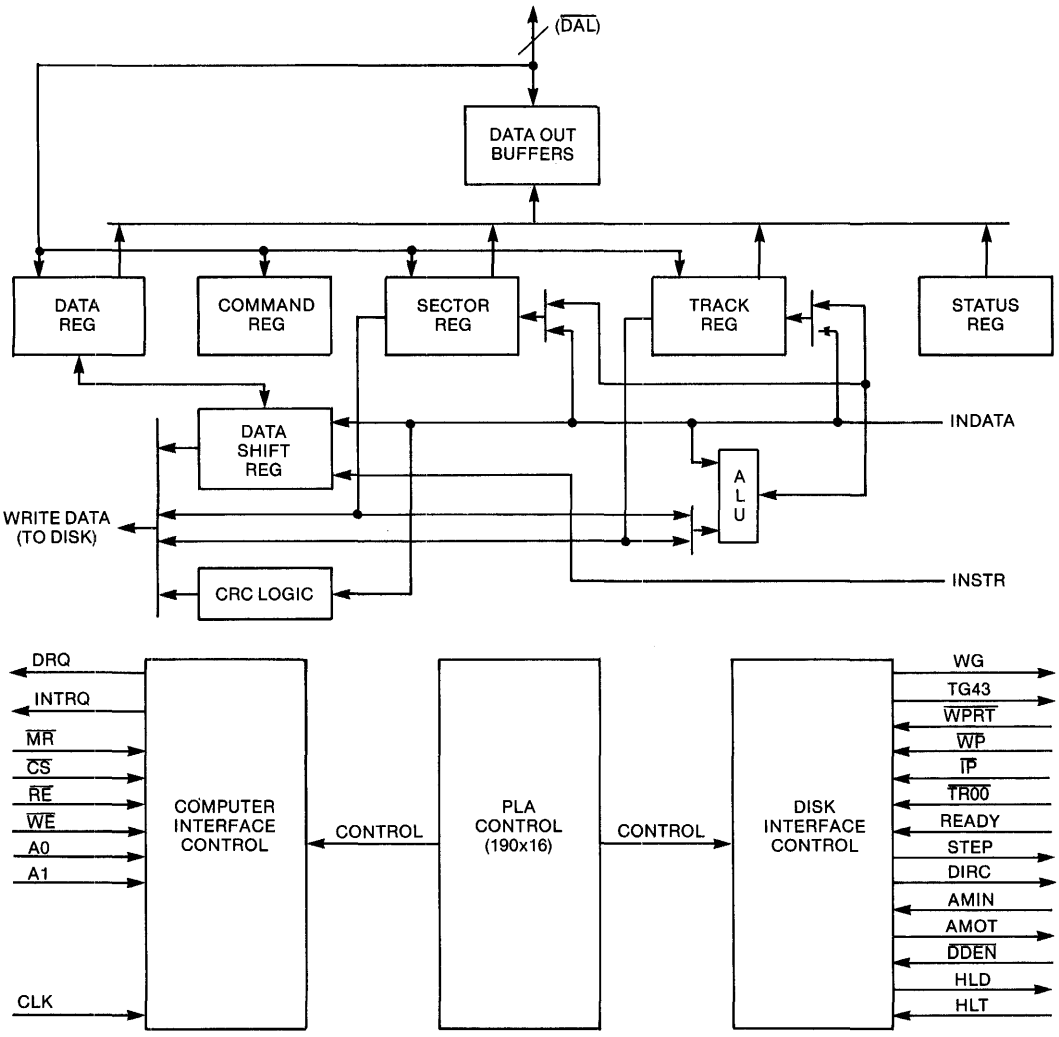


Figure 3. FD1781 BLOCK DIAGRAM

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD1781 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

The Lost Data bit and certain other bits in the Status Register will activate the interrupt request (INTRQ). The interrupt line is also activated with normal completion or abnormal termination of all controller operations. The INTRQ signal remains active until reset by reading the Status Register to the processor or by the loading of the Command Register. In addition, the INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The Floppy Disk interface consists of head positioning controls, write gate controls, and data transfers. The Clock (CLK) input is normally a free-running 2 MHz ±1% when in the double density mode and 1 MHz ±1% when in the single density mode. However when using a mini-floppy, the CLK is normally 1 MHz when in double density mode and 1/2 MHz when in the single density mode.

HEAD POSITIONING

Four commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 15 milliseconds of head settling time takes place. The four progammable stepping rates are tabulated below.

The rates (shown in Table 1) can be applied to a Step-Direction Motor through the device interface.

Step — A 2 μs pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC) — The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete. If track comparison is not made but the CRC checks, an interrupt is generated, the Seek Error status (Bit 4) is set and the Busy status bit is preset.

TABLE 1
STEPPING RATES

CLK	2 MHz	1 MHz	1 MHz	1/2 MHz	2 MHz	1 MHz
DDEN	0	1	0	1		
R1 R0	$\overline{TEST}=1$	$\overline{TEST}=1$	$\overline{TEST}=1$	$\overline{TEST}=1$	$\overline{TEST}=0$	$\overline{TEST}=0$
0 0	3 ms	3 ms	6 ms	6 ms	Approx.	Approx.
0 1	6 ms	6 ms	12 ms	12 ms	400 μs	800 μs
1 0	10 ms	10 ms	20 ms	20 ms		
1 1	20 ms	20 ms	40 ms	40 ms		

The Head Load (HDL) output controls the movement of the read/write head against the disk for data recording or retrieval. It is activated at the beginning of a Read, Write (E Flag On) or Verify Operation, or a Seek or Step operation with the head load bit, h, a logic one, and remains activated until the 15th index pulse following the last operation which uses the read/write head. Reading or Writing does not occur until a minimum of 15 msec delay after the HDL signal is made active. If executing the type 2 commands with the E flag off, there is no 15 msec delay and the head is assumed to be engaged. The delay is determined by sampling of the Head Load Timing (HLT) input every 15 msec. A high logic state input, generated from the Head Load output transition and delayed externally, identifies engagement of the head against the disk. In the Seek and Step commands, the head is loaded at the start of the command execution when the h bit is a logic one. In a verify command the head is loaded after stepping to the destination track on the disk whenever the h bit is a logic zero.

DISK READ OPERATION

The normal sector length for Read or Write operations with the IBM 3740 format is 128 bytes. This

format or binary multiples of 128 bytes will be adopted by setting a logic 1 in Bit 3 of the Read Track and Write Track commands. Additionally, a variable sector length feature is provided which allows an indicator recorded in the ID Field to control the length of the sector. Variable sector lengths can be read or written in Read or Write commands respectively by setting a logic 0 in Bit 3 of the command word. The sector length indicator specifies the number of 16 byte groups or 16 x N, where N is equal to 1 to 256 groups. An indicator of all zeroes is interpreted as 256 sixteen byte groups.

DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD1781 before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the $\overline{\text{Write Protect}}$ status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD1781 terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the Write Gate output becomes inactive.

Whenever a Read or Write command is received the FD1781 samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. The Seek or Step commands are performed regardless of the state of the Ready input.

COMMAND DESCRIPTION

The FD1781 will accept and execute eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 2.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contain a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 1, page six.

TABLE 2
COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	X	a_0
III	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	$\overline{s}$
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

X = Don't care

TABLE 3
FLAG SUMMARY

TYPE I

h = Head Load Flag (Bit 3)
- h = 1, Load head at beginning
- h = 0, Do not load head at beginning

V = Verify flag (Bit 2)
- V = 1, Verify on last track
- V = 0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)
- Refer to Table 1 for rate summary

u = Update flag (Bit 4)
- u = 1, Update Track register
- u = 0, No update

TABLE 4
FLAG SUMMARY

TYPE II

m = Multiple Record flag (Bit 4)
- m = 0, Single Record
- m = 1, Multiple Records

b = Block length flag (Bit 3)
- b = 1, IBM format (128 to 1024 bytes)
- b = 0, Non-IBm format (16 to 4096 bytes)

a_0 = Data Address Mark (Bit 0)
- a_0 = 0, FB (Data Mark)
- a_0 = 1, F8 (Deleted Data Mark)

TABLE 5
FLAG SUMMARY

TYPE III
s = Synchronize flag (Bit 0)
$\overline{s}$ = 0, Synchronize to AM
$\overline{s}$ = 1, Do Not Synchronize to AM
TYPE IV
Ii = Interrupt Condition flags (Bits 3-0)
I0 = 1, Not Ready to Ready Transition
I1 = 1, Ready to Not Ready Transition
I2 = 1, Index Pulse
I3 = 1, Immediate interrupt
E = Enable HLD and 10 msec Delay
E = 1, Enable HLD, HLT and 15 msec Delay
E = 0, Head is assumed Engaged and there is no 15 msec Delay

The Type I Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command (HLD output is made active). If h = 0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD1781 receives a command that specifically disengages the head. If the FD1781 does not receive any commands after two revolutions of the disk, the head will be automatically disengaged (HLD made inactive). The Head Load Timing Input is sampled after a 15 ms delay, when reading or writing on the disk is to occur.

The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V = 1, a verification is performed, if V = 0, no verification is performed.

During verification, the head is loaded and after an internal 15 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, the Seek Error status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the FD1781 terminates the operation and sends an interrupt, (INTRQ).

The Step, Step-In, and Step-Out commands contain an Update flag (U). When U = 1, the track register is updated by one for each step. When U = 0, the track register is not updated.

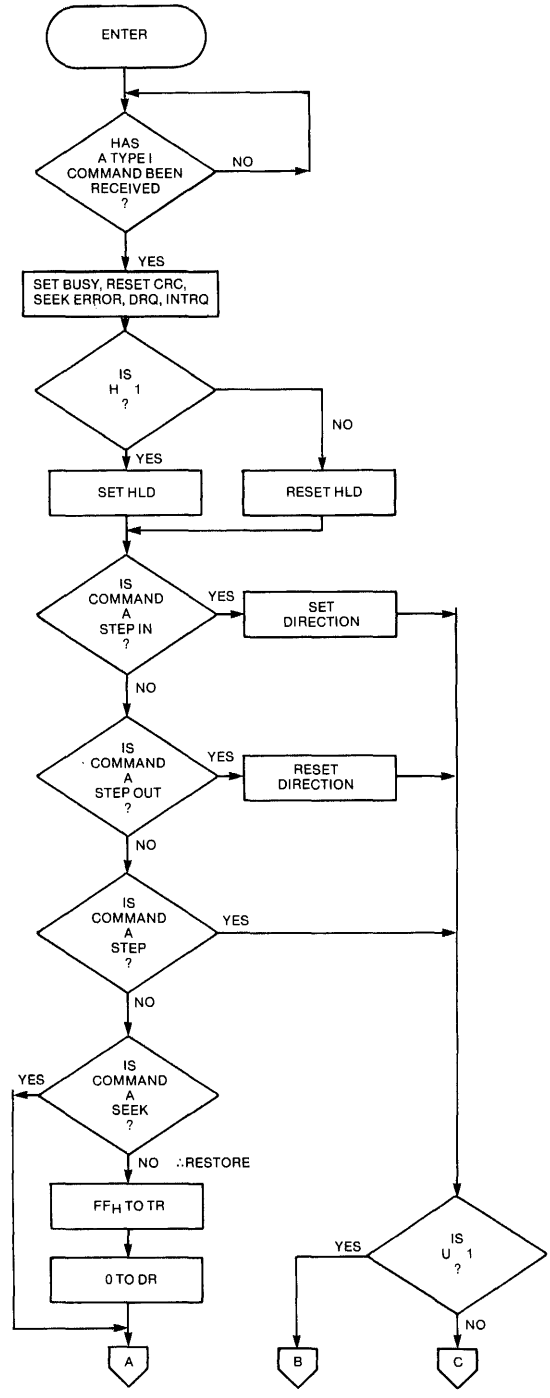


Figure 4. TYPE I COMMAND FLOW

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r_1r_0 field are issued until the $\overline{TR00}$ input is activated. At this time the TR is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD1781 terminates operation, interrupts, and sets the Seek error status bit. Note that the Restore command is executed when MR goes from an active to an inactive state. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD1781 will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the data register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD1781 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the u flag is on, the TR is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD1781 issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD1781 issues one stepping pulse in the direction towards track 0. If

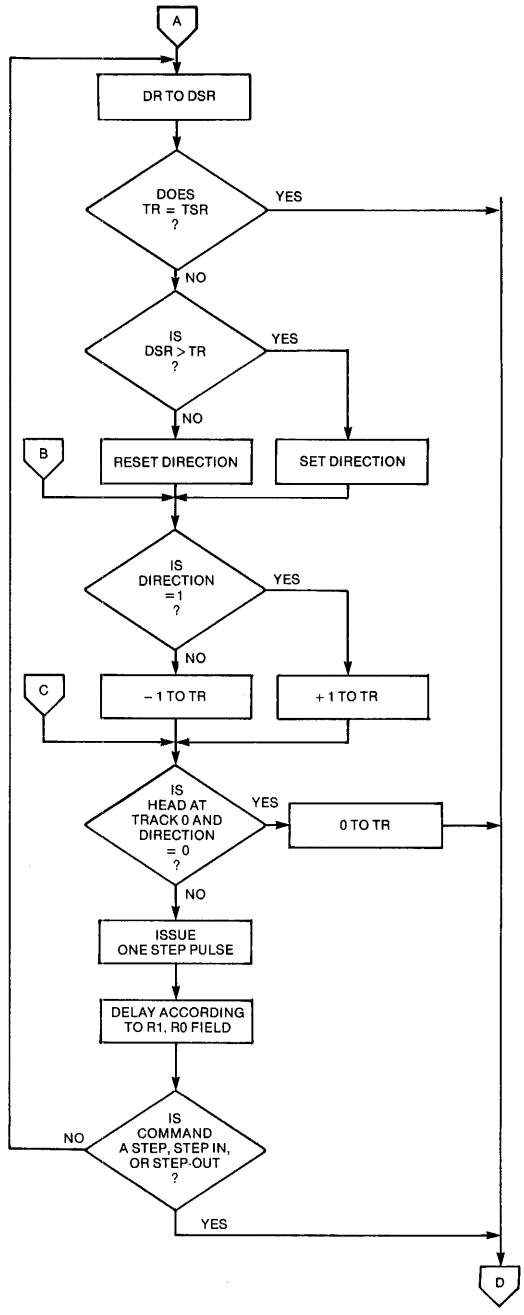


Figure 5. TYPE I COMMAND FLOW

the u flag is on, the TR is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands include the Read Sector (s) and Write Sector (s) commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II Command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is assumed to be engaged and there is no 15 msec delay. The ID field and Data Field format are shown on page 11.

When an ID field is located on the disk, the FD1781 compares the Track Number of the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD1781 must find an ID field with a Track number, Sector number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

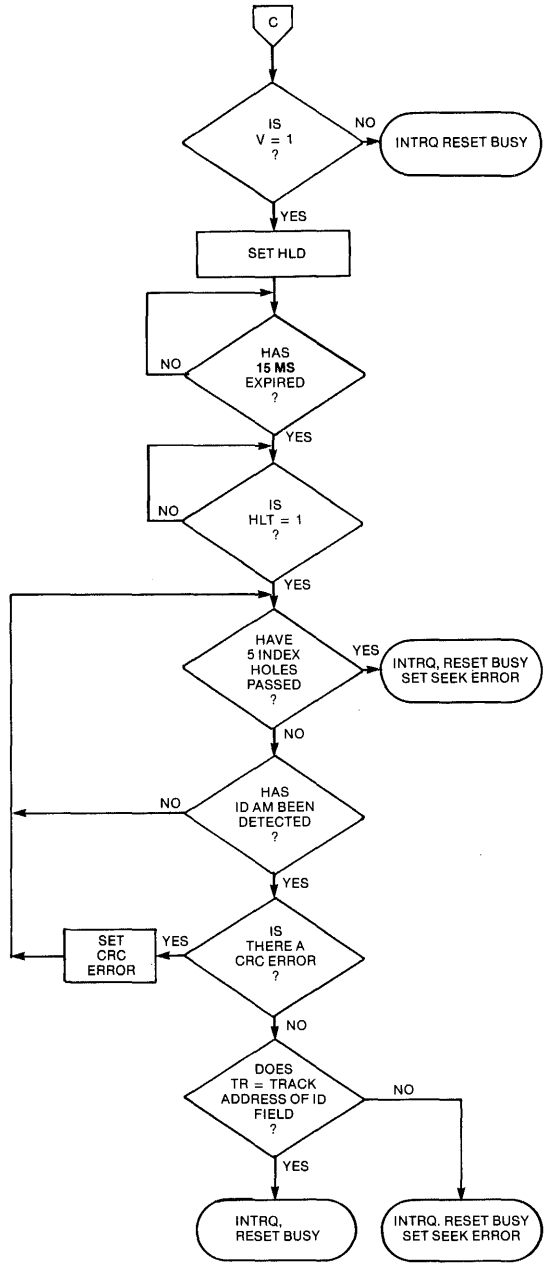
Each of the Type II Commands contain a (b) flag which in conjunction with the sector length field contents of the ID determines the length (number of characters) of the Data field.

For IBM 3740 compatibility, the b flag should equal 1. The numbers of bytes in the data field (sector) is then 128×2^n where n = 0,1,2,3.

For b = 1

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

When the b flag equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field as shown on page 11.



NOTE: IF $\overline{TEST}$-0, THERE IS NO 15MS DELAY.
IF $\overline{TEST}$-1 ANC CLK-1 MHz. THERE IS 30MS DELAY.

Figure 6. TYPE I COMMAND FLOW

For b = 0

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
01	16
02	32
03	48
04	64
•	•
•	•
•	•
FF	4080
00	4096

Each of the Type II Commands also contain a (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0 a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD1781 will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminated the command and generates an interrupt.

READ COMMAND

Upon receipt of the Read command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record Not Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bits 5) as shown below:

STATUS BIT 5	DATA 1	DATA 2	DATA 3
1	0	0	0
0	0	1	1

WRITE COMMAND

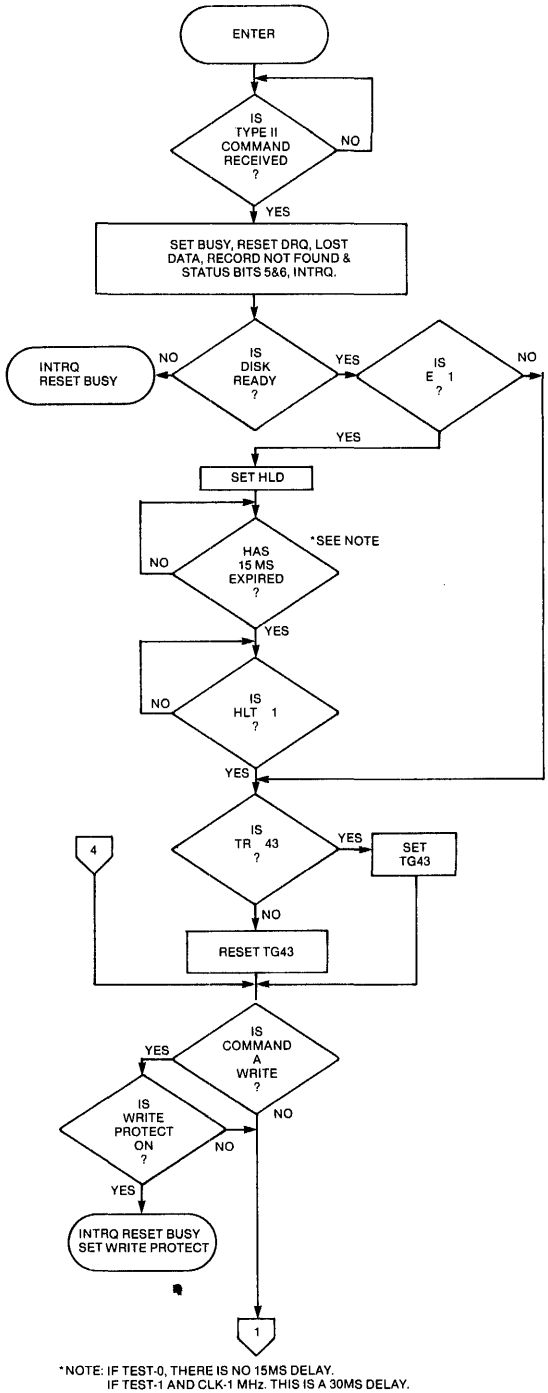
Upon receipt of the Write command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The FD1781 counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a^0 field of the command as shown below:

a^0	DATA 1	DATA 2	DATA 3
1	0	0	0
0	0	1	1

The FD1781 then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte gap of logic ones. The WG output is then deactivated.

GAP	ID AM	TRACK NUMBER	ZEROS	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP	DATA AM	DATA FIELD	1	2
ID FIELD									DATA FIELD			

IDAM = ID Address Mark – DATA = $(FE)_{16}$ CLK = $(C7)_{16}$
Data AM = Data Address Mark – DATA = (F8 or FB), CLK = $(C7)_{16}$



*NOTE: IF TEST-0, THERE IS NO 15MS DELAY.
IF TEST-1 AND CLK-1 MHz. THIS IS A 30MS DELAY.

Figure 7. TYPE II COMMAND

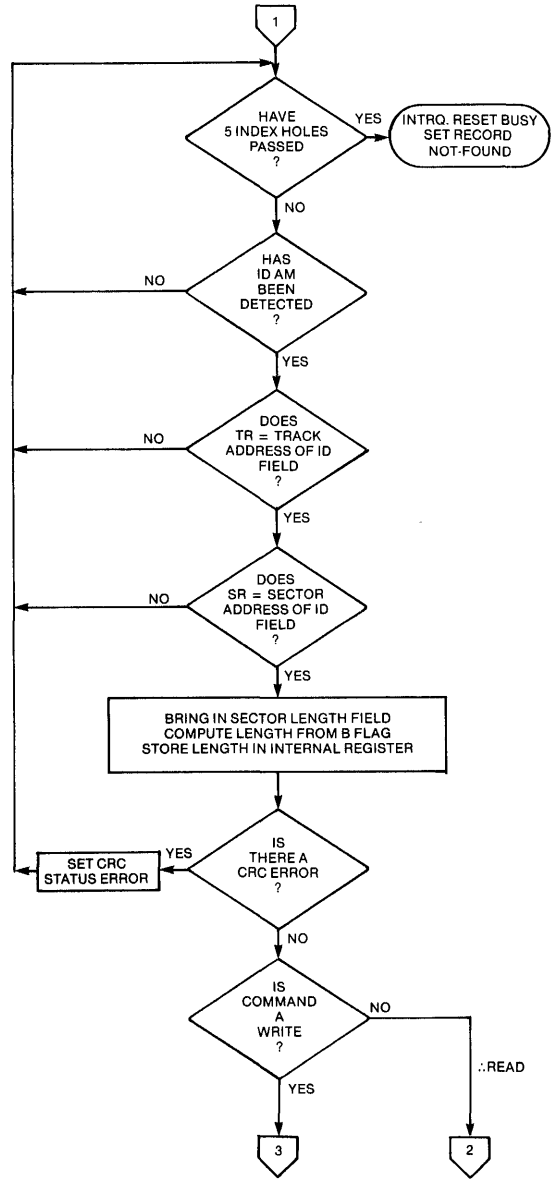


Figure 8. TYPE II COMMAND

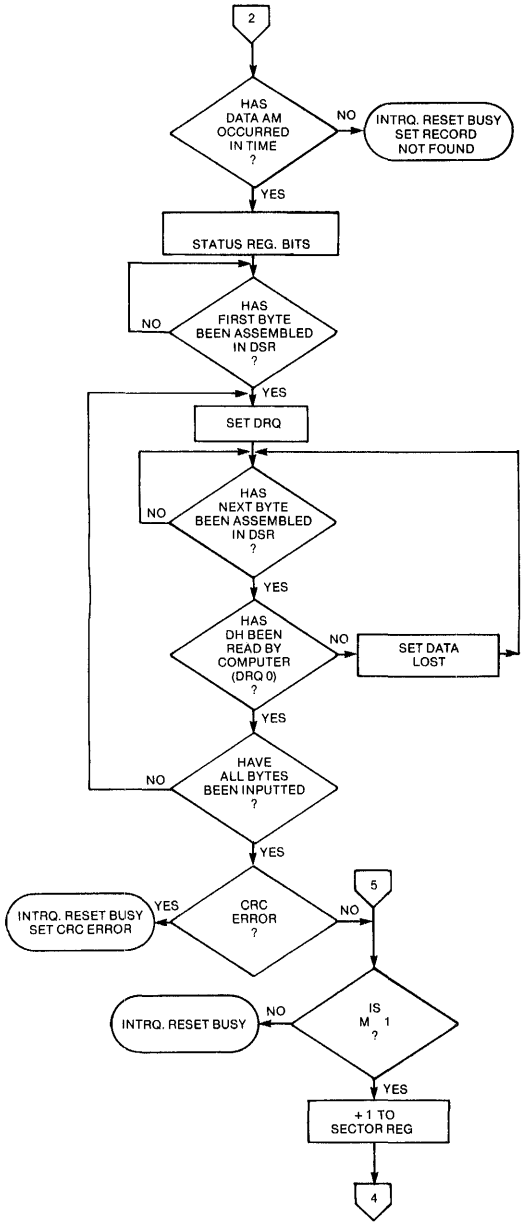


Figure 9. TYPE II COMMAND

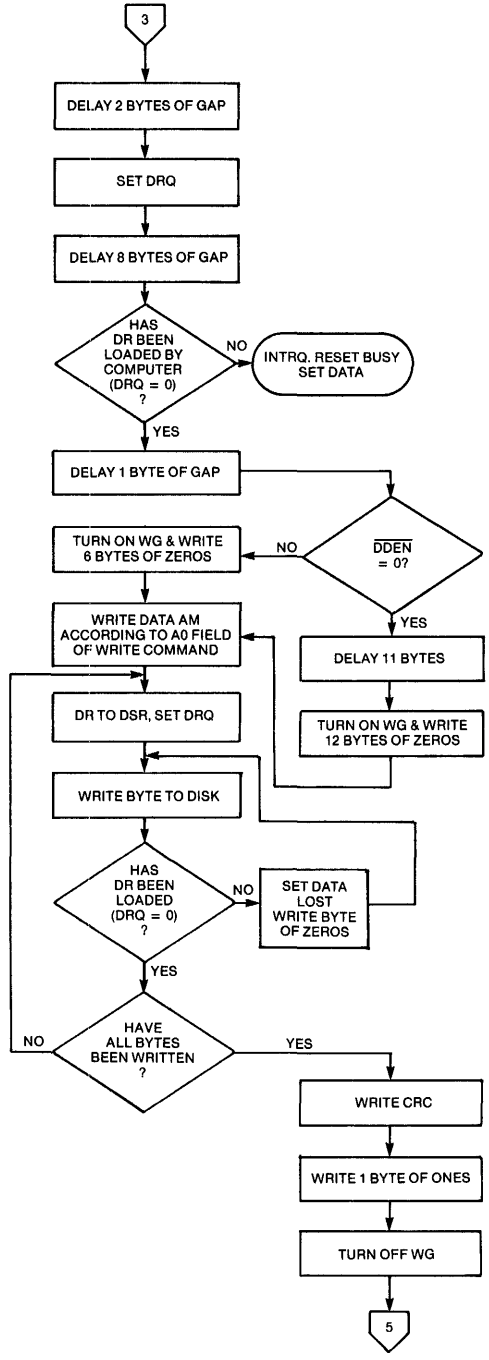
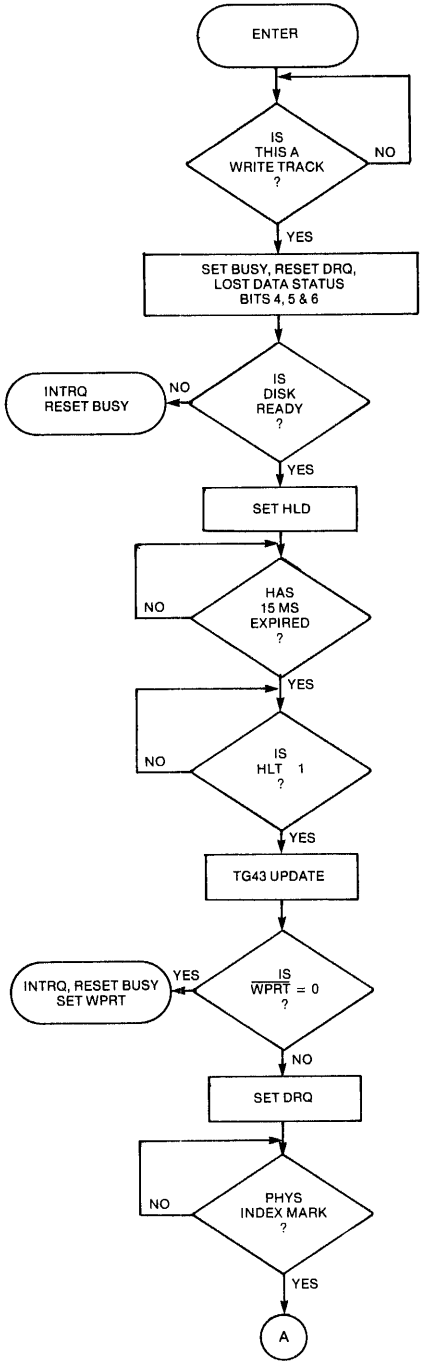
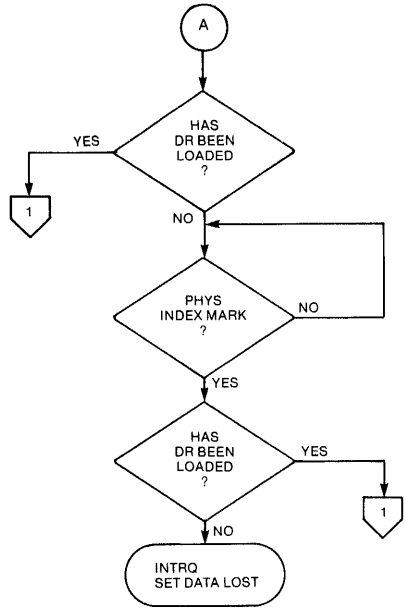


Figure 10. TYPE II COMMAND





NOTE: IF $\overline{TEST}$-0, THERE IS NO 15MS DELAY,
IF $\overline{TEST}$-1 AND CLK-1 MHz. THIS IS A 30MS DELAY.

Figure 11. TYPE III COMMAND WRITE TRACK

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	ZEROS	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FD1781 checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse.

As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If bit 0 (S) of the command is a 0, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

WRITE TRACK

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR.

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN (HEX)	INTERPRETATION	CLOCK MARK* (HEX)
F7	Write CRC Char.	FF
F8	Deleted Data Addr. Mark	C7
FB	Data Addr. Mark	C7
FC	Index Addr. Mark	D7
FD	Spare	
FE	ID Addr. Mark	C7

*Single density only

DATA 1	DATA 2	DATA 3	TYPE OF ADDRESS MARK
0	0	0	Deleted Data Mark
0	1	1	Data Mark
1	0	0	Index Address Mark
1	0	1	Undefined
1	1	0	ID Address Mark
1	1	1	Undefined

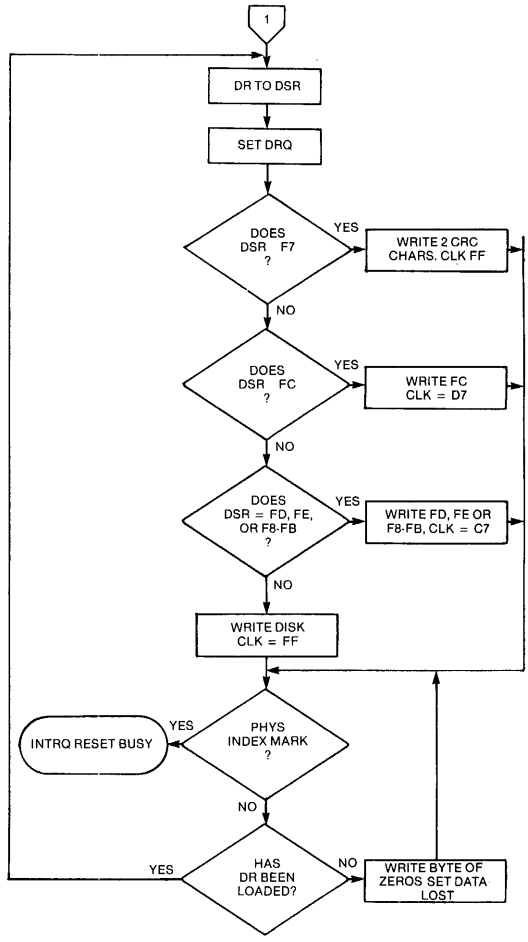


Figure 12. TYPE III COMMAND WRITE TRACK

TYPE IV COMMAND

FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0 = Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

NOTE: If I_0-I_3 = 0, there is no interrupt generated but the current command is terminated and busy is reset.

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below:

7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

TABLE 6
STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD ENGAGED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{WRPT}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	When set, there was one or more CRC errors encountered on an unsuccessful track verification operation. This bit is reset to 0 when updated.
S2 TRACK 00	When set, indicates Read Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{TR00}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{IP}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS BITS FOR TYPE II AND TYPE III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. On Read Track: Not Used. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND	When set, it indicates that the desired track and sector were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA control with a large amount of memory. When operating under DMA with limited amount of memory, formatting is a more difficult task. This is because gaps as well as data must be provided at the computer interface.

Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the FD1781 raises the data request signal. At this point in time, the user loads the data register with desired data to be written on the disk. For every byte of information to be written on the disk, a data request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a clock mark of $(FF)_{16}$. However, if the FD1781 detects a data pattern on F7 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters. As a consequence, the patterns F7 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by a F7 pattern.

Disks may be formatted in IBM 3740 formats with sector lengths of 128, 256, 512, or 1024 bytes, or may be formatted in non-IBM 3740 with sectors length of 16 to 4096 bytes in 16 byte increments. IBM 3740 at the present time only defines two formats. One format with 128 bytes/sector and the other with 256 bytes/sector. The next section deals with the IBM 3740 format with 128 bytes/sector and the following section details non-IBM formats.

IBM 3740 FORMATS — 128 BYTES/SECTOR

Shown in Figure 13, is the IBM format with 128 bytes/sector. In order to format this format, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

	NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
	40	00 or FF
	6	00
	1	FC (Index Mark)
	26	00 or FF
*	6	00
*	1	FE (ID Address Mark)
*	1	Track Number
*	1	00
*	1	Sector Number (1 thru 1A)
*	1	00
*	1	F7 (2 CRC's written)
	11	00 or FF
	6	00
	1	FB (Data Address Mark)
	128	Data (IBM uses E5)
	1	F7 (2 CRC's written)
	27	00 or FF
	247**	00 or FF

*Write bracketed field 26 times

**Continue writing until FD1781 interrupts out. Approx. 247 bytes.

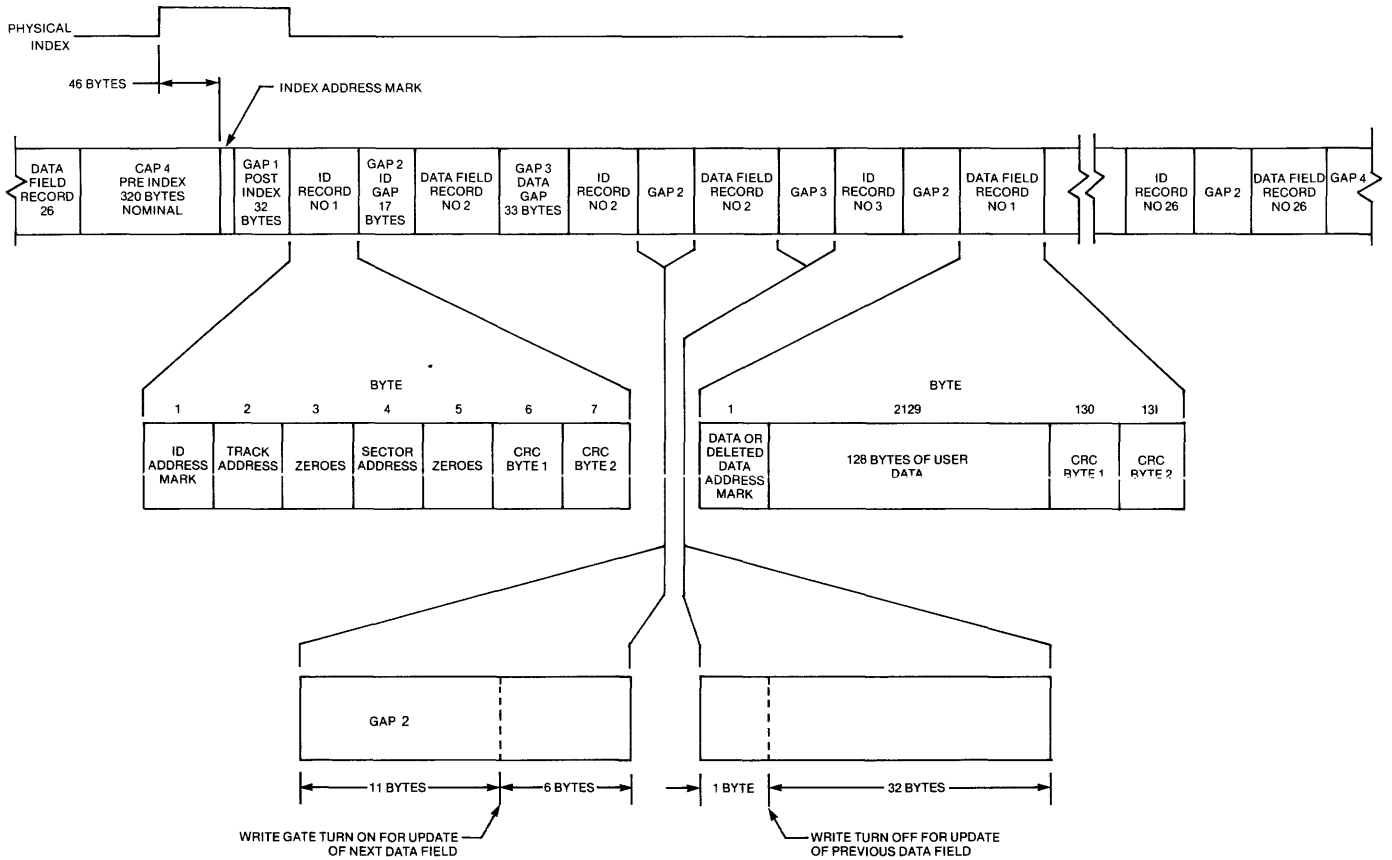


Figure 13. IBM 3740 TRACK FORMAT

NON-IBM FORMATS

Non-IBM formats are very similar to the IBM formats except a different algorithm is used to ascertain the sector length from the sector length byte in the ID field. This permits a wide range of sector lengths from 16 to 4096 bytes. Refer to Section V, Type II Commands with b flag equal to zero. Note that F7 thru FE must not appear in the sector length byte of the ID field.

In formatting the FD1781, only two requirements regarding GAP sizes must be met. GAP 2 (i.e., the gap between the ID field and data field) must be 17 bytes of which the last 6 bytes must be zeros in single density mode, and 34 bytes of which the last 12 bytes must be zeros in double density mode. For the FD1781-01, these byte counts for GAP2 are doubled.

The FD1781 does not require the index address mark (i.e., DATA = FC, CLK = D7) and it need not be present.

REFERENCES:

1. IBM Diskette OEM Information GA21-9190-1
2. SA900 IBM Compatibility Reference Manual — Shugart Associates.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{DD} With Respect to V_{SS} (Ground) . . + 15 to − 0.3V
Max. Voltage to Any Input With
Respect to V_{SS} . . . . . + 15 to − 0.3V
Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . − 55°C to + 125°C

OPERATING CHARACTERISTICS (DC)

T_A = 0°C to 70°C, V_{DD} = +12.0V ± .6V, V_{SS} = 0V, V_{CC} = +5V ± .25V
V_{DD} = 10 ma Nominal, V_{CC} = 30 ma Nominal
DC characteristics T_A = 0°C to 50°C; V_{DD} = 12V ± .6V, V_{SS} = 0V, V_{CC} = 5V ± .25V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	μA	$V_{OUT} = V_{DD}$
V_{IH}	Input High Voltage	2.6			V	
V_{IL}	Input Low Voltage (All Inputs)			0.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = − 100μA
V^*_{OL}	Output Low Voltage			0.45	V	I_O = 1.6 mA

NOTE: Vol ⩽ .4V when interfacing with low Power Schottky parts (1_O < 1 ma)
*except WG, where V_{OL} ⩽ .5 volts.

TIMING CHARACTERISTICS

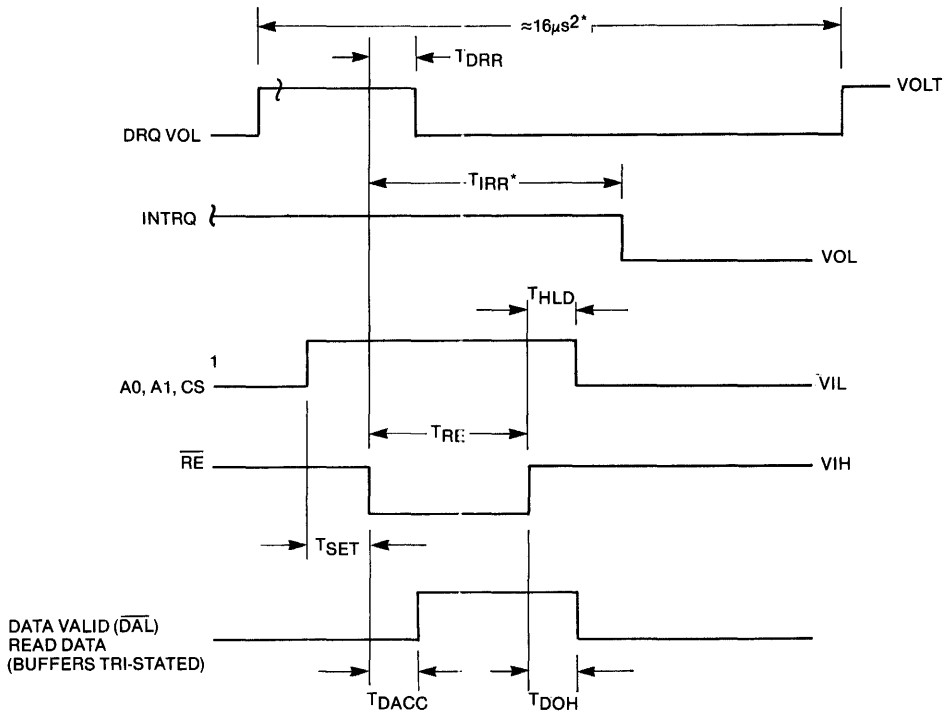
T_A = 0°C to 50°C, V_{DD} = +12V ± .6V, V_{SS} = 0V, V_{CC} = +5V ± .25V

NOTE: Timings are given for 2 MHz Clock. For those timings noted, values will double when chip is operated at 1 MHz.

READ OPERATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	100			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	500			nsec	C_L = 25 pf
TDRR	DRQ Reset from $\overline{RE}$			500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$		500	3000	nsec	
TDACC	Data Access from $\overline{RE}$			350	nsec	C_L = 25 pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	C_L = 25 pf

READ ENABLE TIMING

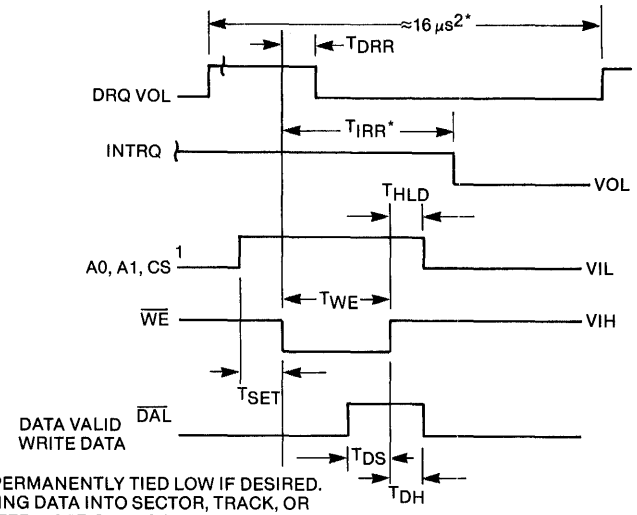


NOTE: 1. $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED.
2. FOR READ TRACK COMMAND. THIS TIME MAY BE 6* TO 16* μSEC WHEN S = 0.
*TIME DOUBLES WHEN CLK-1 MHz.

WRITE OPERATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	100			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$			500	nsec	
TIRR	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	20			nsec	

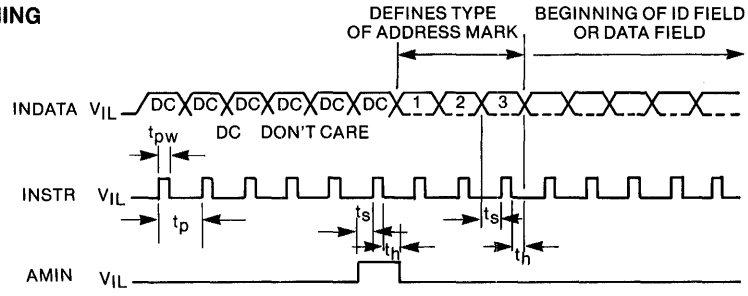
WRITE ENABLE TIMING



NOTE: 1. $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED.
2. WHEN WRITING DATA INTO SECTOR, TRACK, OR DATA REGISTER, USER CANNOT READ THIS REGISTER UNTIL AT LEAST 8 μSEC AFTER THE RISING EDGE OF $\overline{WE}$. WHEN WRITING INTO THE COMMAND REGISTER STATUS IS NOT VALID UNTIL SOME 12 μSEC LATER. THESE TIMES ARE DOUBLED WHEN CLK = 1 MHz.

*TIME DOUBLES WHEN CLOCK = 1 MHz.

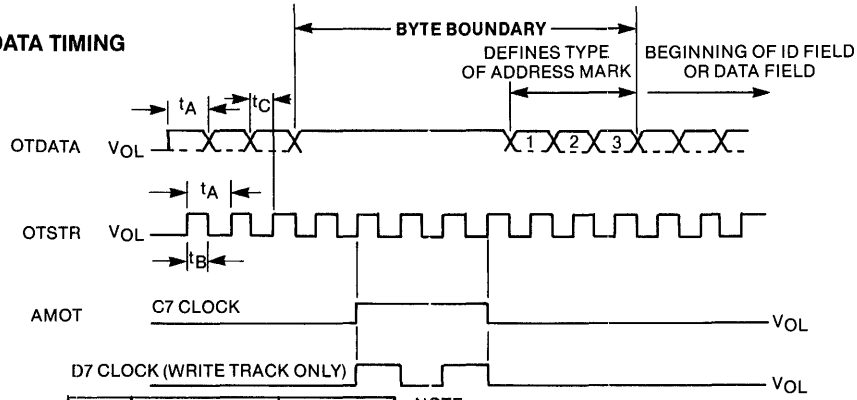
INPUT DATA TIMING



t_{pw} 500 ns = 50 ns
$t_s \geq 100$ ns
$t_h \geq 300$ ns
$1\,2\mu s < t_p < ½$ ms

NOTE: INSTR MUST BE FREE RUNNING AS INDICATED BY THE t_p SPECIFICATION. ALSO, THERE MUST BE AT LEAST 2 INSTR PULSES DURING MASTER RESET.

OUTPUT DATA TIMING



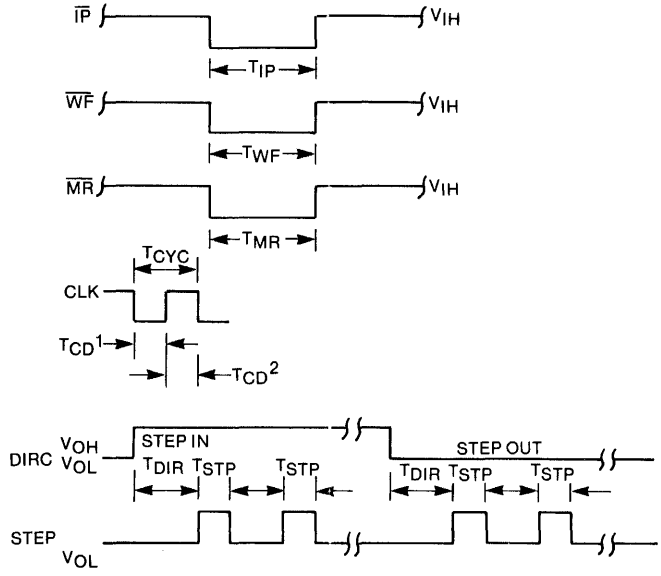
	DDEN 1	DDEN 0
t_A	SEE NOTE	2 μs
t_B		1 μs
t_C		1 μs
		CLK 2 mHz

NOTE:
WHENEVER $\overline{DDEN}$ 0. OTSTR IS FREE RUNNING AS SHOWN ABOVE.
WHEN $\overline{DDEN}$ 1 & WG 0, OTSTR IS A SERIES OF FM CLOCK PULSES.
WHEN $\overline{DDEN}$ 1 & WG 1, OTSTR BECOMES WD AS IN THE FD1771 (i.e. CONTAINS FM CLOCK & DATA PULSES).

MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TCD_1	Clock Duty	175			nsec	2 MHz ± 1% See Note
TCD_2	Clock Duty	210			nsec	
TSTP	Step Pulse Output	2000			nsec	
TDIR	Dir Setup to Step	12			μsec	These times doubled when CLK = 1 MHz
TMR	Master Reset Pulse Width	5			μsec	
TIP	Index Pulse Width	5			μsec	
TWF	Write Fault Pulse Width	5			μsec	

MISCELLANEOUS TIMING



See page 725 for ordering information.

WESTERN DIGITAL
CORPORATION

FD179X-02
Floppy Disk Formatter/Controller Family

FEATURES

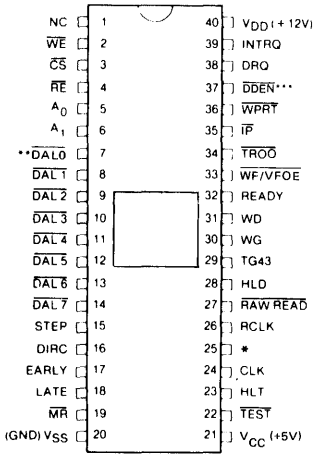
- TWO VFO CONTROL SIGNALS — RG & VFOE
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
  - Non IBM Format for Increased Capacity
- READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128, 256, 512 or 1024 Byte Sector Lengths
- WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-Chip Track and Sector Registers/Comprehensive Status Information
- PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- INTERFACES TO WD1691 DATA SEPARATOR
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- FD1792/4 IS SINGLE DENSITY ONLY
- FD1795/7 HAS A SIDE SELECT OUTPUT

179X-02 FAMILY CHARACTERISTICS

FEATURES	1791	1792	1793	1794	1795	1797
Single Density (FM)	X	X	X	X	X	X
Double Density (MFM)	X		X		X	X
True Data Bus			X	X		X
Inverted Data Bus	X	X			X	
Write Precomp	X	X	X	X	X	X
Side Selection Output					X	X

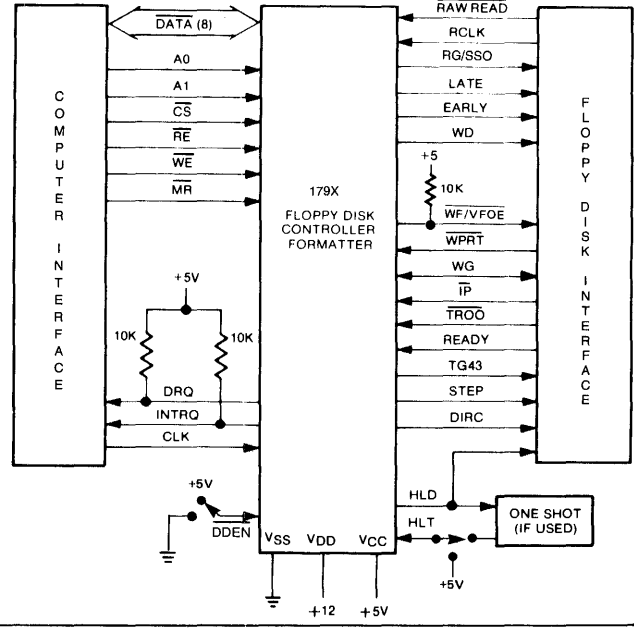
APPLICATIONS

8" FLOPPY AND 5¼" MINI FLOPPY CONTROLLER
SINGLE OR DOUBLE DENSITY
CONTROLLER/FORMATTER



*1791/3 = RG 1795/7 = SSO
**1793/7 TRUE BUS
***1792/4 OPEN

PIN CONNECTIONS



FD179X SYSTEM BLOCK DIAGRAM

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.
19	MASTER RESET	$\overline{MR}$	A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ±5%
40		V_{DD}	+12V ±5%
COMPUTER INTERFACE:			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: $\overline{CS}$ A1 A0 $\overline{RE}$ $\overline{WE}$ 0 0 0 Status Reg Command Reg 0 0 1 Track Reg Track Reg 0 1 0 Sector Reg Sector Reg 0 1 1 Data Reg Data Reg
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit Bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by $\overline{WE}$ or transmitter enabled by $\overline{RE}$. Each line will drive 1 standard TTL load.
24	CLOCK	CLK	This input requires a free-running 50% duty cycle square wave clock for internal timing reference, 2 MHz ± 1% for 8" drives, 1 MHz ±1% for mini-floppies.
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the WRITE DATA pulse occuring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated steppers.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD.
25	READ GATE (1791, 1792, 1793, 1794)	RG	This output is used for synchronization of external data separators. The output goes high after two Bytes of zeros in single density, or 4 Bytes of either zeros or ones in double density operation.
25	SIDE SELECT OUTPUT (1795, 1797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the Sector I.D. Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	A 200 ns (MFM) or 500 ns (FM) output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$ $\overline{\text{VFO ENABLE}}$	$\overline{\text{WF/VFOE}}$	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, VFOE will remain low until the end of the Data Field. This pin has an internal 100K Ohm pull-up resistor.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD179X that the Read/Write head is positioned over Track 00.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
35	INDEX PULSE	$\overline{IP}$	This input informs the FD179X when the index hole is encountered on the diskette.
36	WRITE PROTECT	$\overline{WPRT}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	DOUBLE DENSITY	$\overline{DDEN}$	This input pin selects either single or double density operation. When $\overline{DDEN}$ = 0, double density is selected. When $\overline{DDEN}$ = 1, single density is selected. This line must be left open on the 1792/4.

GENERAL DESCRIPTION

The FD179X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD179X, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD179X contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD179X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The FD179X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD179X is TTL compatible on all inputs and outputs. The outputs will drive ONE TTL load or three LS loads. The 1793 is identical to the 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The 1795/7 has a side select output for controlling double sided drives, and the 1792 and 1794 are "Single Density Only" versions of the 1791 and 1793 respectively. On these devices, DDEN must be left open.

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input ($\overline{RAW\ READ}$) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

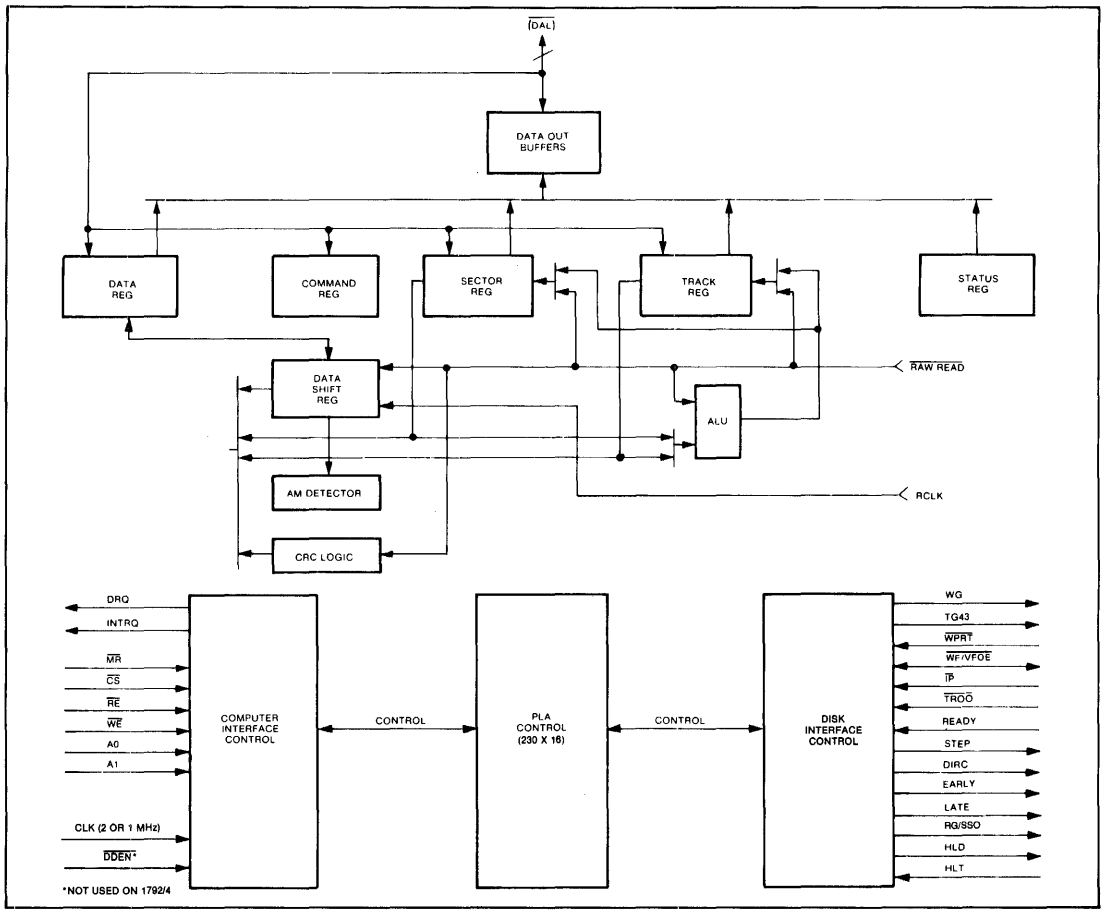
CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control — All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD179X has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 0 double density (MFM) is assumed. When $\overline{DDEN}$ = 1, single



FD179X BLOCK DIAGRAM

density (FM) is assumed. 1792 & 1794 are single density only.

AM Detector — The address mark detector detects ID, data and index address marks during read and write operations.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{DAL}$) and associated control signals. The $\overline{DAL}$ are used to transfer Data, Status, and Control words out of, or into the FD179X. The $\overline{DAL}$ are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1	A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data

Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The 179X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1." For MFM formats, $\overline{DDEN}$ should be placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

Sector Length Table*	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

*1795/97 may vary — see command summary.

The number of sectors per track as far as the FD179X is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD179X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track. (See Sector Length Table)

For read operations in 8" double density the FD179X requires $\overline{RAW\ READ}$ Data (Pin 27) signal which is a 200 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) on 1791/92/93/94 which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM. RG is made true when 2 bytes of zeroes are detected. The FD179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the $\overline{VFOE}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{VFOE}$ will go active low when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 179X is inspecting data off the disk

If $\overline{WF}/\overline{VFOE}$ is not used, leave open or tie to a 10K resistor to +5.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD179X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{Write\ Protect}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD179X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{Write\ Fault}$ input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{DDEN}$ = 1) and 200 ns pulses in MFM ($\overline{DDEN}$ = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written EARLY. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

READY

Whenever a Read or Write command (Type II or III) is received the FD179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

COMMAND DESCRIPTION

The FD179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

TABLE 1. COMMAND SUMMARY

A. Commands for Models: 1791, 1792, 1793, 1794

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

B. Commands for Models: 1795, 1797

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	L	E	U	a_0
III	Read Address	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

FLAG SUMMARY

TABLE 2. FLAG SUMMARY

Command Type	Bit No(s)		Description
I	0, 1	r_1 r_0 = Stepping Motor Rate See Table 3 for Rate Summary	
I	2	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track
I	3	h = Head Load Flag	h = 1, Load head at beginning h = 0, Unload head at beginning
I	4	T = Track Update Flag	T = 0, No update T = 1, Update track register
II	0	a_0 = Data Address Mark	a_0 = 0, FB (DAM) a_0 = 1, F8 (deleted DAM)
II	1	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare
II & III	1	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1
II & III	2	E = 15 MS Delay	E = 0, No 15 MS delay E = 1, 15 MS delay
II	3	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1
II	3	L = Sector Length Flag	LSB's Sector Length in ID Field 00: L = 0 → 256; L = 1 → 128 01: L = 0 → 512; L = 1 → 256 10: L = 0 → 1024; L = 1 → 512 11: L = 0 → 128; L = 1 → 1024
II	4	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records
IV	0-3	I_x = Interrupt Condition Flags I_0 = 1 Not Ready To Ready Transition I_1 = 1 Ready To Not Ready Transition I_2 = 1 Index Pulse I_3 = 1 Immediate Interrupt, Requires A Reset I_3-I_0 = 0 Terminate With No Interrupt (INTRQ)	

*NOTE: See Type IV Command Description for further information.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field (r_0 r_1), which determines the stepping motor rate as defined in Table 3.

A 2 μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated.

The rates (shown in Table 3) can be applied to a Step-Direction Motor through the device interface.

TABLE 3. STEPPING RATES

CLK		2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
$\overline{DDEN}$		0	1	0	1	X	X
R1	R0	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=0	$\overline{TEST}$=0
0	0	3 ms	3 ms	6 ms	6 ms	184μs	368μs
0	1	6 ms	6 ms	12 ms	12 ms	190μs	380μs
1	0	10 ms	10 ms	20 ms	20 ms	198μs	396μs
1	1	15 ms	15 ms	30 ms	30 ms	208μs	416μs

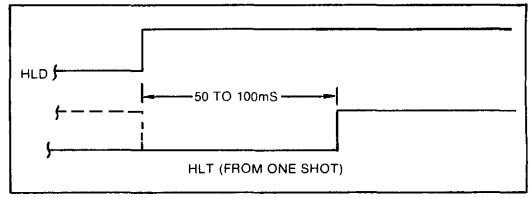
After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If $\overline{TEST}$ = 0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by settling bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

★ The FD179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the FD179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load timing (HLT) is an input to the FD179X which is used for the head engage time. When HLT = 1, the FD179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD179X.



HEAD LOAD TIMING

When both HLD and HLT are true, the FD179X will then read from or write to the media. The "and" of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the FD179X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the FD179X then waits for HLT to occur.

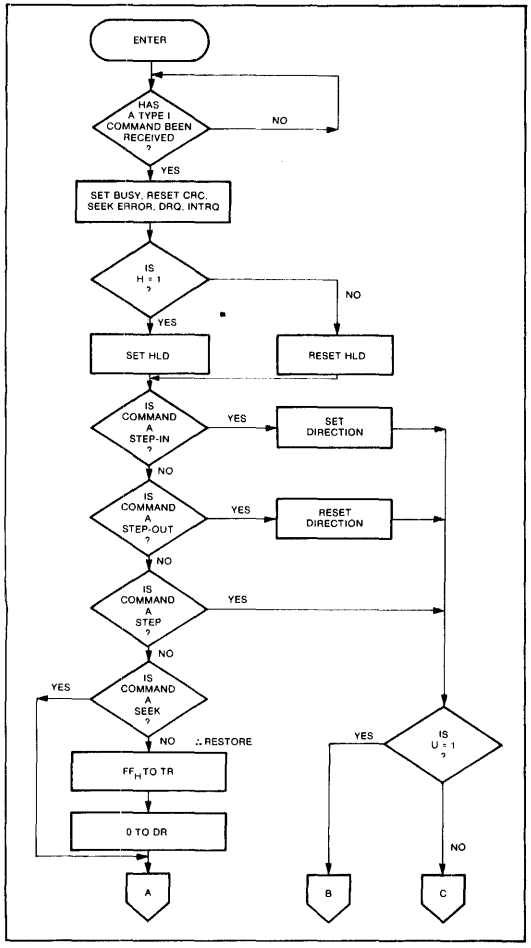
For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

RESTORE (SEEK TRACK 0)

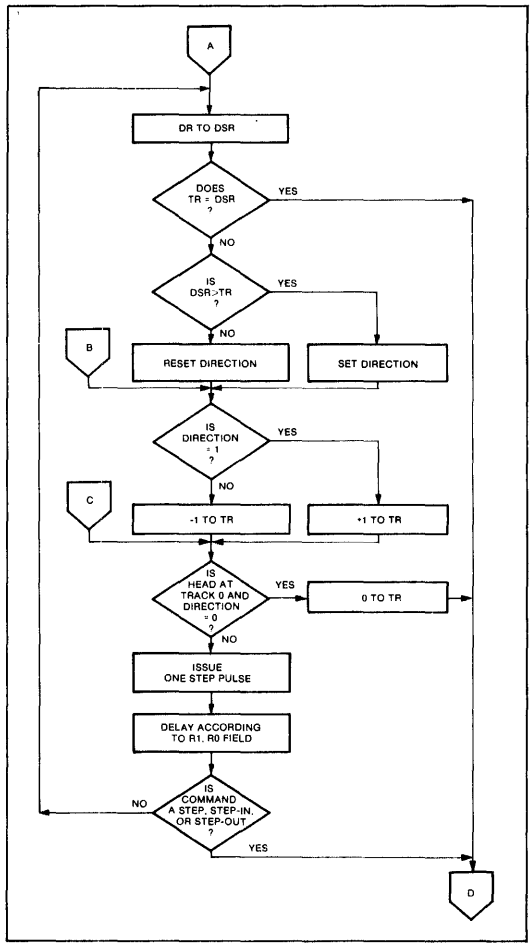
Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r_1 r_0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD179X terminates operation, interrupts, and sets the Seek error status bit, providing the V flag is set. A verification operation also takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{MR}$ goes from an active to an inactive state and that the DRQ pin stays low.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the FD179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the U flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

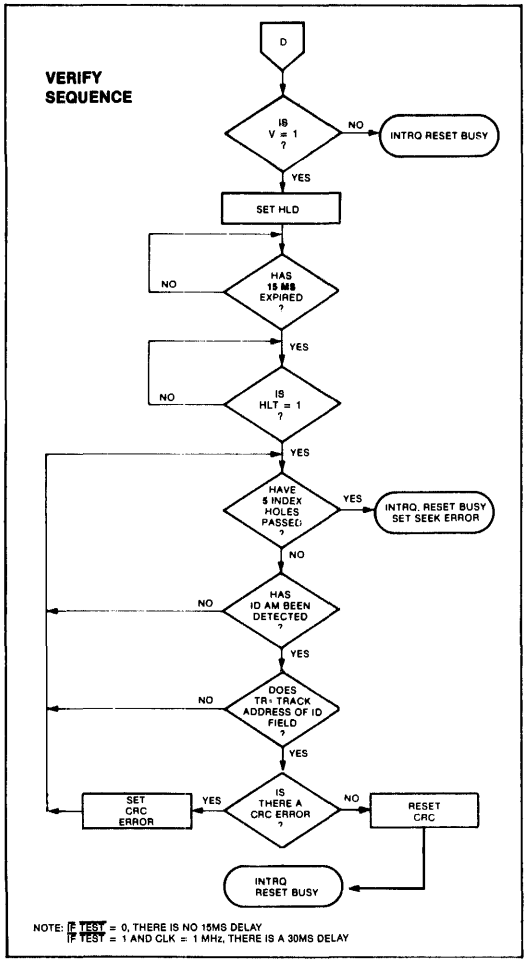
Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 76. If the U flag is on, the Track Register is incremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 0. If the U flag is on, the Track Register is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

EXCEPTIONS

On the 1795/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.

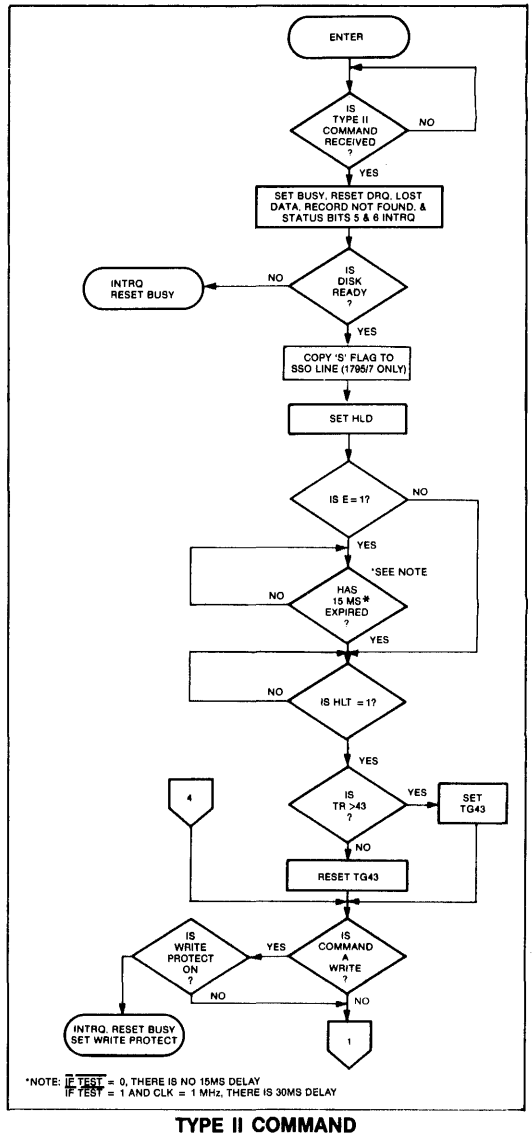


TYPE I COMMAND FLOW

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay. The ID field and Data Field format are shown on page 13.

When an ID field is located on the disk, the FD179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an Interrupt.



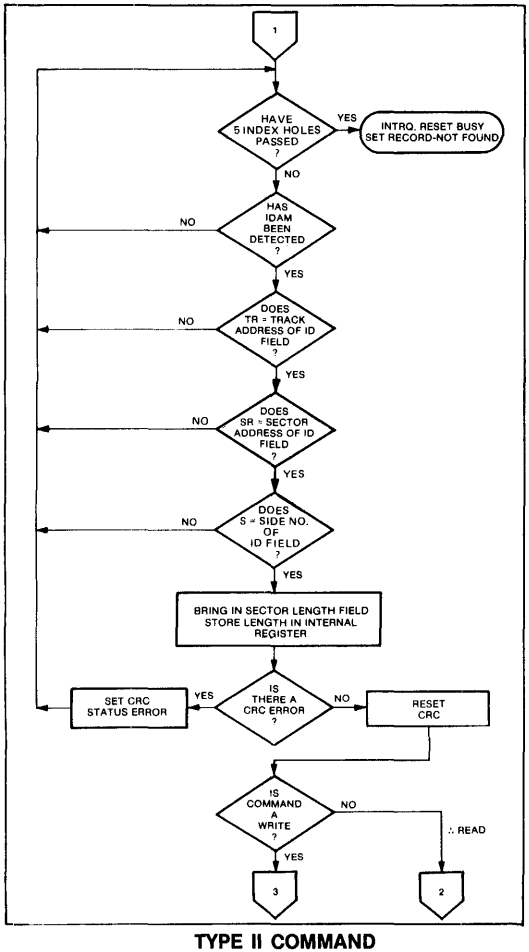
TYPE II COMMAND

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next

record. The FD179X will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the FD179X is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds the number available. The FD179X will search for 5 disk revolutions, interrupt out, reset busy, and set the record not found status bit.

The Type II commands for 1791-94 also contain side select compare flags. When C = 0 (Bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag (Bit 3). If the S flag compares with the side number recorded in the ID field, the FD179X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.



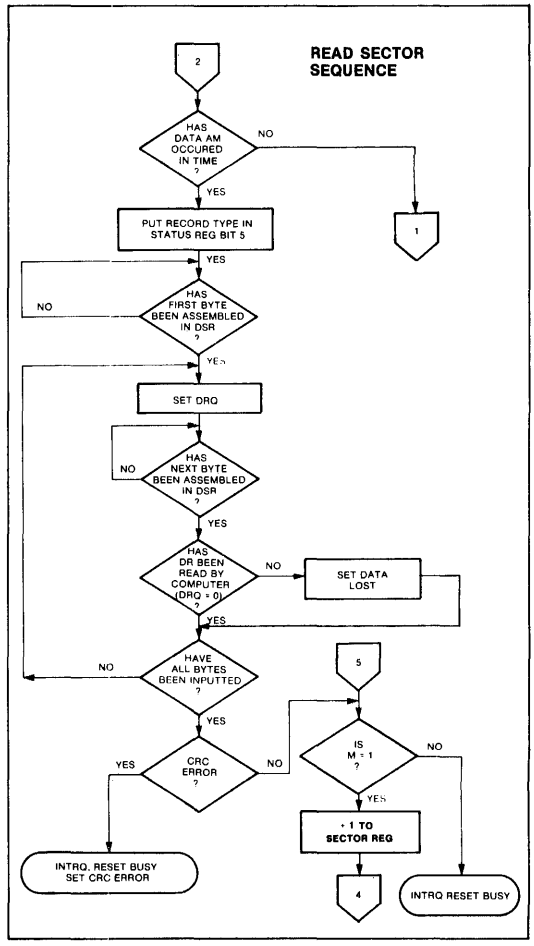
TYPE II COMMAND

The Type II and III commands for the 1795-97 contain a side select flag (Bit 1). When U = 0, SSO is updated to 0. Similarly, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions the interrupt line is made active and the RNF status bit is set.

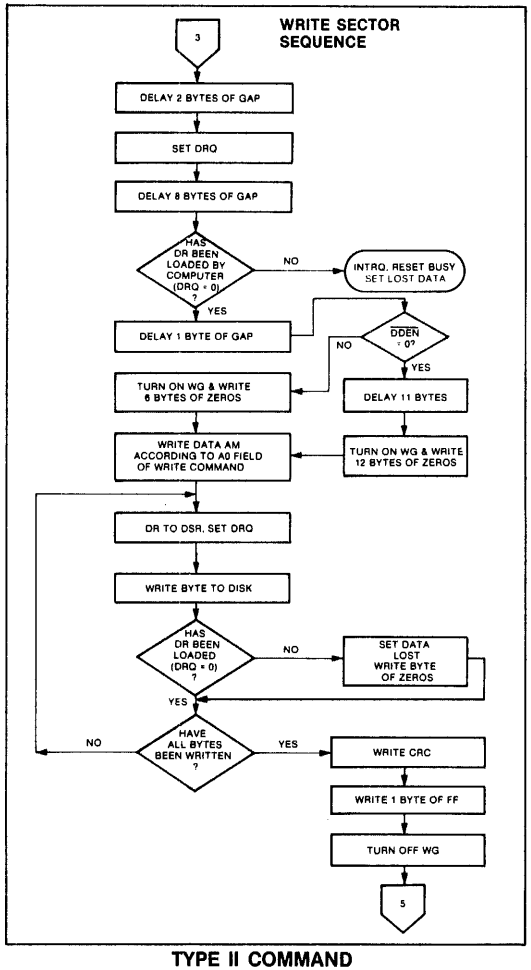
The 1795/7 READ SECTOR and WRITE SECTOR commands include a 'L' flag. The 'L' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatability, the 'L' flag should be set to a one.

READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address



TYPE II COMMAND



TYPE II COMMAND

Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID field is searched for and verified again followed by the Data Address Mark search. If after 5 revolutions the DAM cannot be found, the Record Not Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FD179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The FD179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ will set 8 to 12 μsec after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the lost data status and improper CRC Bytes.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

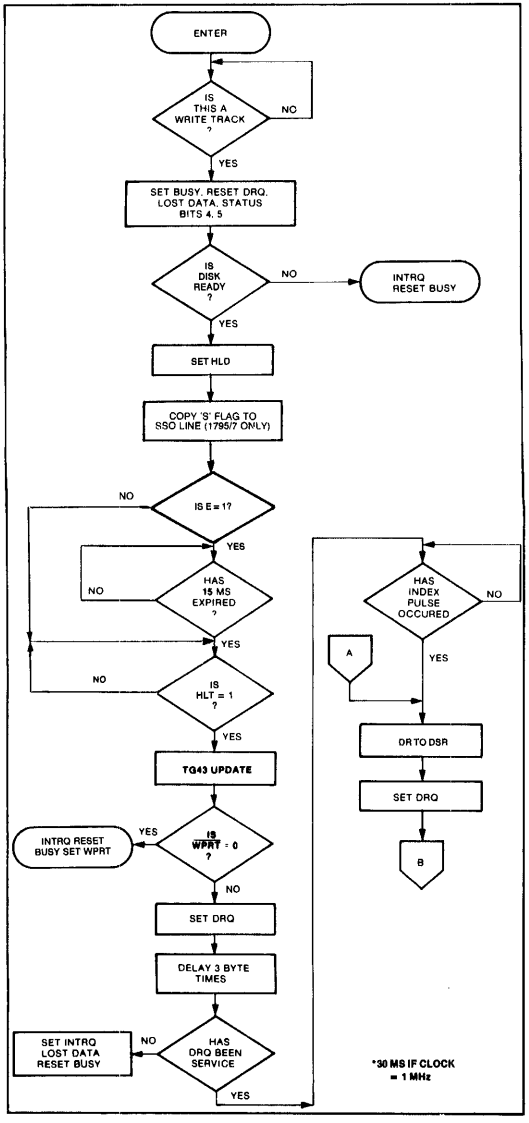
Although the CRC characters are transferred to the computer, the FD179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the user. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

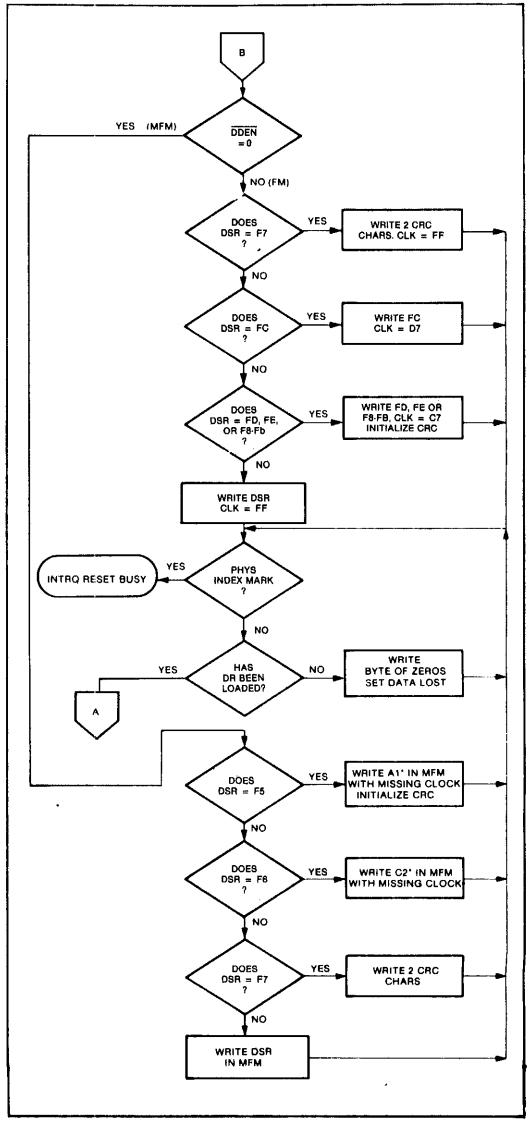
Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: the Read Gate is not activated during the command; no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule the Lost Data status flag is set.

The ID A.M., ID field, ID CRC bytes, DAM, Data, and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.



TYPE III COMMAND WRITE TRACK



TYPE III COMMAND WRITE TRACK

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	FD179X INTERPRETATION IN FM ($\overline{DDEN}$ = 1)	FD1791/3 INTERPRETATION IN MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5

**Missing clock transition between bits 3 & 4

WRITE TRACK FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the FD179X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

TYPE IV COMMANDS

The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to insure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

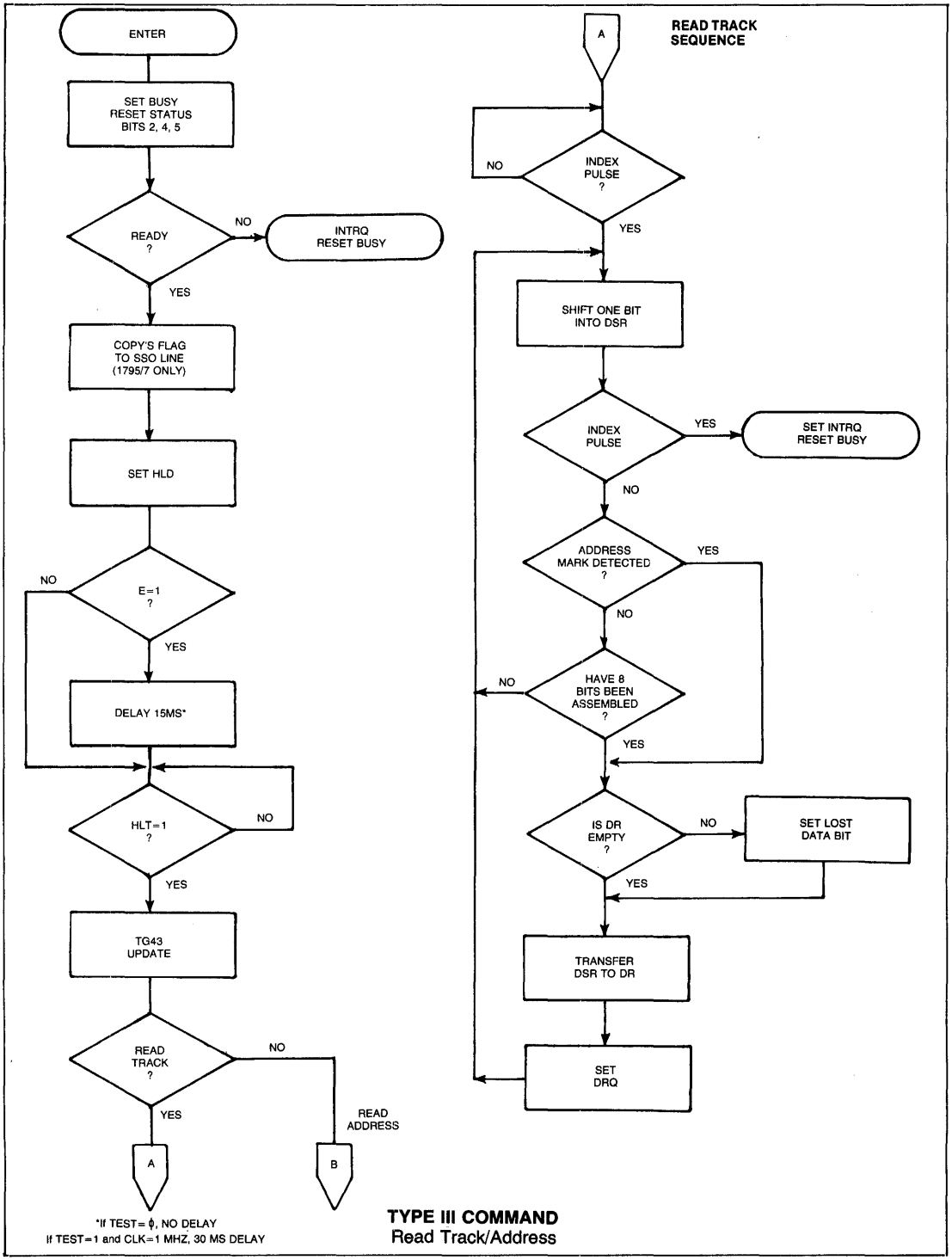
I_0 = Not-Ready to Ready Transition
I_1 = Ready to Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3 - I_0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I_3 - I_0 are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition (I_3 = 1) an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

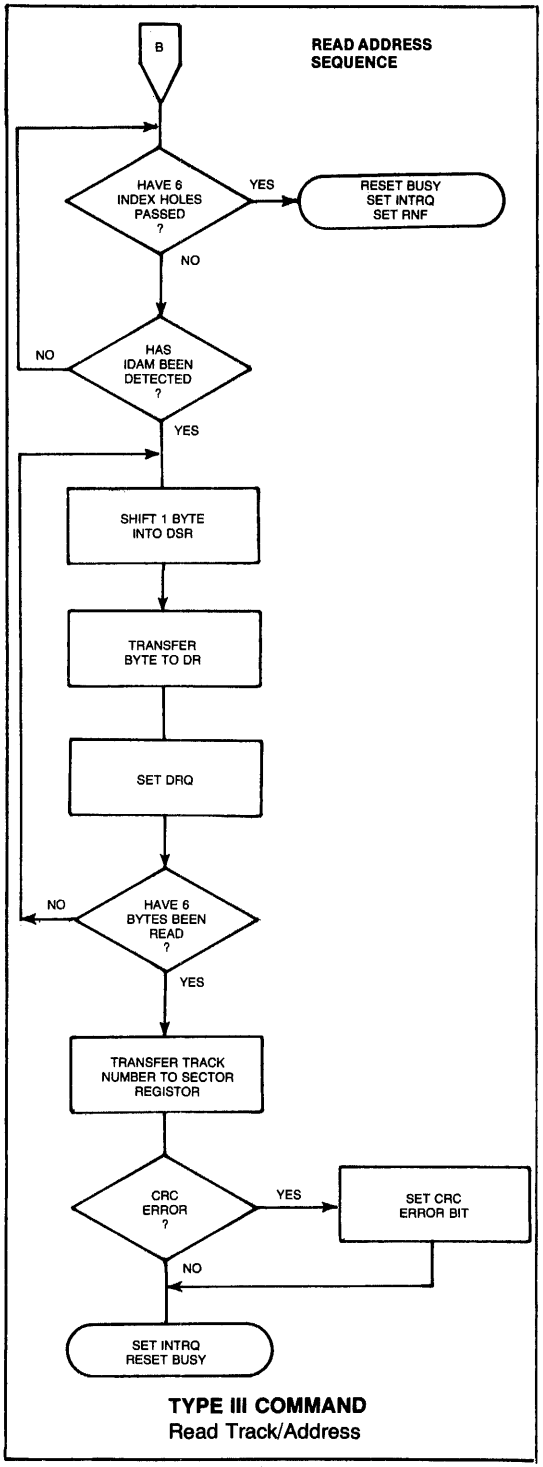
Wait 8 micro sec (double density) or 16 micro sec (single density before issuing a new command after issuing a forced interrupt (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.).

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I_1 = 1) and the Every Index Pulse (I_2 = 1) are both set, the resultant command would be HEX "DA". The "OR" function is performed so that either a READY TO NOT- READY or the next Index Pulse will cause an interrupt condition.



TYPE III COMMAND
Read Track/Address



TYPE III COMMAND
Read Track/Address

STATUS REGISTER

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are: (times double when clock = 1 MHz)

Operation	Next Operation	Delay Req'd. FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12 μs	6 μs
Write to Command Reg.	Read Status Bits 1-7	28 μs	14 μs
Write Any Register	Read From Diff. Register	0	0

IBM 3740 FORMAT — 128 BYTES/SECTOR

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

IBM 3740 FORMAT — 128 BYTES/SECTOR

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

	NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
	40	FF (or 00)[1]
	6	00
	1	FC (Index Mark)
*	26	FF (or 00)[1]
	6	00
	1	FE (ID Address Mark)
	1	Track Number
	1	Side Number (00 or 01)
	1	Sector Number (1 thru 1A)
	1	00 (Sector Length)
	1	F7 (2 CRC's written)
	11	FF (or 00)[1]
	6	00
	1	FB (Data Address Mark)
	128	Data (IBM uses E5)
	1	F7 (2 CRC's written)
	27	FF (or 00)[1]
	247**	FF (or 00)[1]

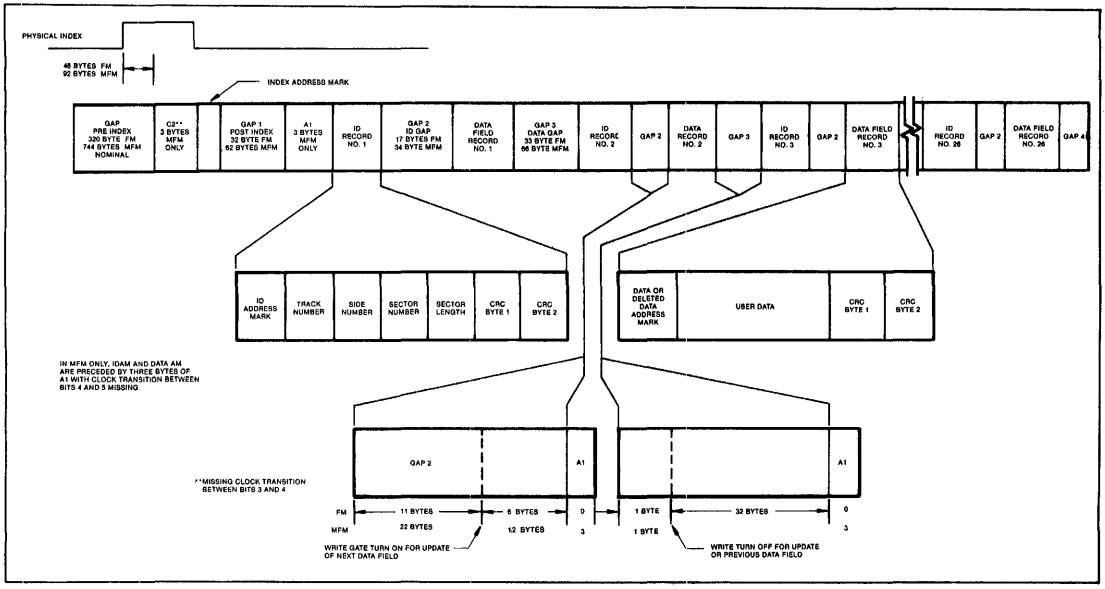
*Write bracketed field 26 times
**Continue writing until FD179X interrupts out. Approx. 247 bytes.
1-Optional '00' on 1795/7 only.

IBM SYSTEM 34 FORMAT- 256 BYTES/SECTOR

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

	NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
	80	4E
	12	00
	3	F6 (Writes C2)
	1	FC (Index Mark)
*	50	4E
	12	00
	3	F5 (Writes A1)
	1	FE (ID Address Mark)
	1	Track Number (0 thru 4C)
	1	Side Number (0 or 1)
	1	Sector Number (1 thru 1A)
	1	01 (Sector Length)
	1	F7 (2 CRCs written)
	22	4E
	12	00
	3	F5 (Writes A1)
	1	FB (Data Address Mark)
	256	DATA
	1	F7 (2 CRCs written)
	54	4E
	598**	4E

*Write bracketed field 26 times
**Continue writing until FD179X interrupts out. Approx. 598 bytes.



IBM TRACK FORMAT

1. NON-IBM FORMATS

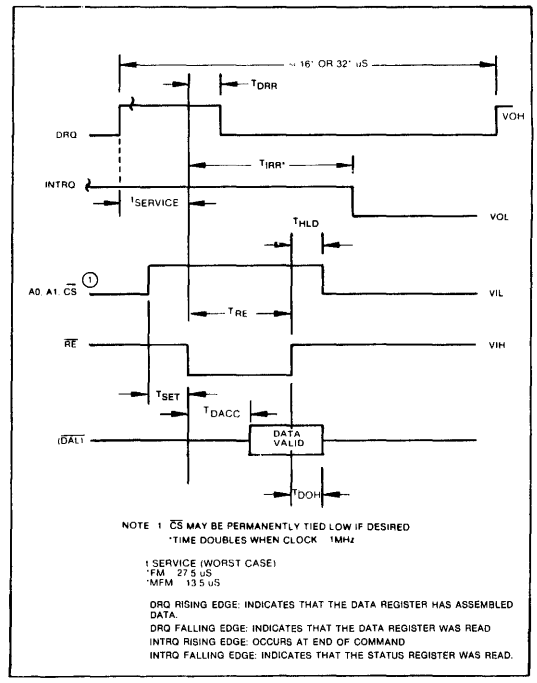
Variations in the IBM formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512 or 1024 bytes.
2) Gap 2 cannot be varied from the IBM format.
3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the FD179X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for FD179X operation, however PLL lock up time, motor speed variation, write-splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.
**Byte counts are minimum, except exactly 3 bytes of A1 must be written.



READ ENABLE TIMING

TIMING CHARACTERISTICS

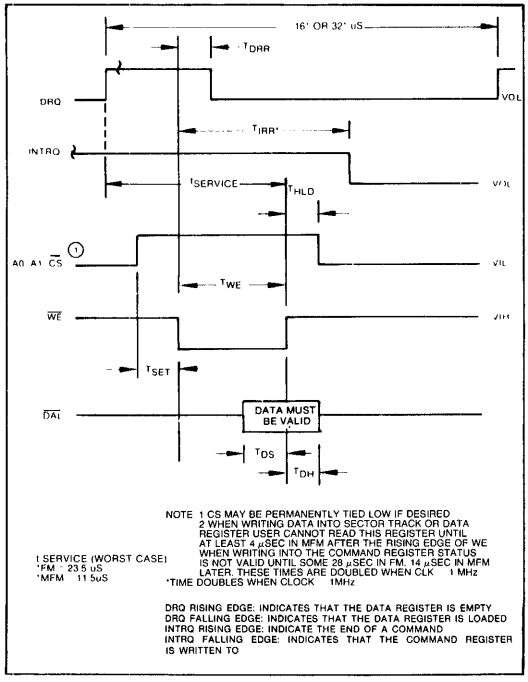
T_A = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = 0V, V_{CC} = +5V ± .25V

READ ENABLE TIMING (See Note 6, Page 21)

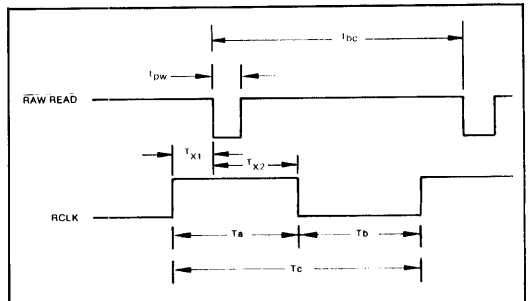
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	400			nsec	C_L = 50 pf
TDRR	DRQ Reset from $\overline{RE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$		500	3000	nsec	See Note 5
TDACC	Data Access from $\overline{RE}$			350	nsec	C_L = 50 pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	C_L = 50 pf

WRITE ENABLE TIMING (See Note 6, Page 21)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note 5
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	70			nsec	



WRITE ENABLE TIMING



				NOMINAL		
DISKETTE	MODE	DDEN	CLK	T_a	T_b	T_c
8"	MFM	0	2 MHz	1 μs	1 μs	2 μs
8"	FM	1	2 MHz	2 μs	2μs	4 μs
5"	MFM	0	1 MHz	2 μs	2μs	4 μs
5"	FM	1	1 MHz	4 μs	4 μs	8 μs

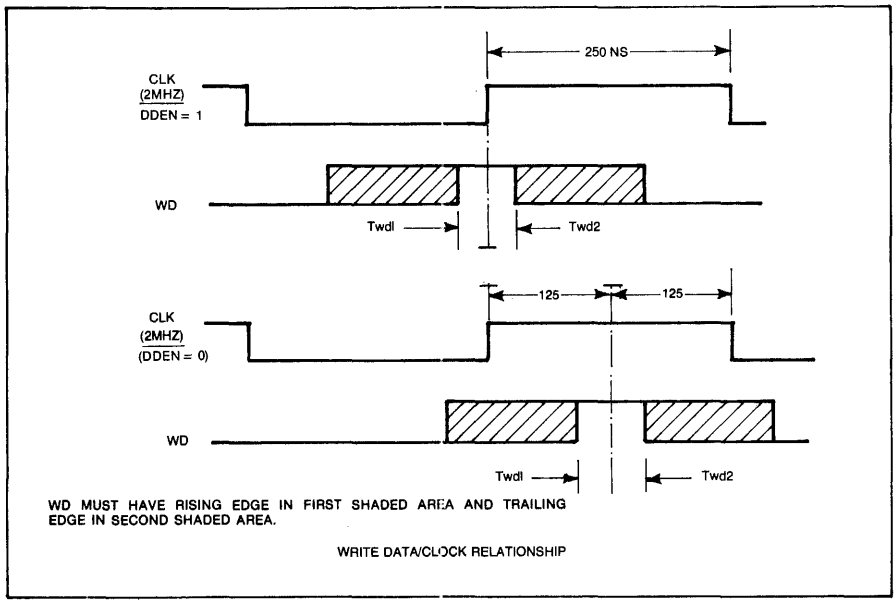
INPUT DATA TIMING

INPUT DATA TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Tpw	$\overline{\text{Raw Read}}$ Pulse Width	100	200		nsec	See Note 1
tbc	$\overline{\text{Raw Read}}$ Cycle Time	1500	2000		nsec	1800 ns @ 70°C
Tc	RCLK Cycle Time	1500	2000		nsec	1800 ns @ 70°C
T_{X1}	RCLK hold to $\overline{\text{Raw Read}}$	40			nsec	See Note 1
T_{X2}	$\overline{\text{Raw Read}}$ hold to RCLK	40			nsec	See Note 1

WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHz) (See Note 6, Page 21)

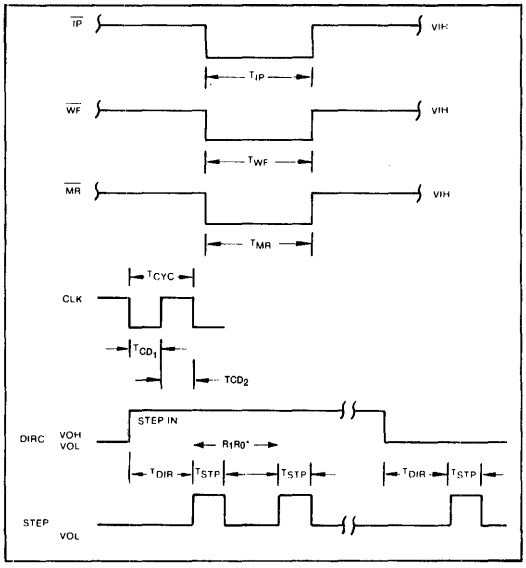
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Twp	Write Data Pulse Width		500	**650**	nsec	FM
			200	**350**	nsec	MFM
Twg	Write Gate to Write Data		2		μsec	FM
			1		μsec	MFM
Tbc	Write data cycle Time		2,3, or 4		μsec	±CLK Error
Ts	Early (Late) to Write Data	125			nsec	MFM
Th	Early (Late) From Write Data	125			nsec	MFM
Twf	Write Gate off from WD		2		μsec	FM
			1		μsec	MFM
Twd1	WD Valid to Clk	100			nsec	CLK=1 MHZ
		50			nsec	CLK=2 MHZ
Twd2	WD Valid after CLK	100			nsec	CLK=1 MHZ
		30			nsec	CLK=2 MHZ



WRITE DATA TIMING

MISCELLANEOUS TIMING: (Times Double When Clock = 1 MHz) (See Note 6, Page 21)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD_1	Clock Duty (low)	230	250	20000	nsec	
TCD_2	Clock Duty (high)	200	250	20000	nsec	
TSTP	Step Pulse Output	2 or 4			μsec	See Note 5
TDIR	Dir Setup to Step		12		μsec	± CLK ERROR
TMR	Master Reset Pulse Width	50			μsec	
TIP	Index Pulse Width	10			μsec	See Note 5
TWF	Write Fault Pulse Width	10			μsec	



MISCELLANEOUS TIMING

*FROM STEP RATE TABLE

NOTES:

1. Pulse width on RAW READ (Pin 27) is normally 100-300 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.
2. A PPL Data Separator is recommended for 8" MFM.
3. tbc should be 2 μs, nominal in MFM and 4 μs nominal in FM. Times double when CLK = 1 MHz.
4. RCLK may be high or low during $\overline{\text{RAW READ}}$ (Polarity is unimportant).
5. Times double when clock = 1 MHz.
6. Output timing readings are at V_{OL} = 0.8v and V_{OH} = 2.0v.

Table 4. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TROO}}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings
- V_{DD} with repect to V_{SS} (ground): +15 to −0.3V
- Voltage to any input with respect to V_{SS} = +15 to −0.3V
- I_{CC} = 60 MA (35 MA nominal)
- I_{DD} = 15 MA (10 MA nominal)
- C_{IN} & C_{OUT} = 15 pF max with all pins grounded except one under test.
- Operating temperature = 0°C to 70°C
- Storage temperature = −55°C to +125°C

OPERATING CHARACTERISTICS (DC)

TA = 0°C to 70°C, V_{DD} = +12V ± .6V, V_{SS} = 0V, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	CONDITIONS
I_{IL}	Input Leakage		10	μA	V_{IN} = V_{DD}**
I_{OL}	Output Leakage		10	μA	V_{OUT} = V_{DD}
V_{IH}	Input High Voltage	2.6		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.8		V	I_O = −100 μA
V_{OL}	Output Low Voltage		0.45	V	I_O = 1.6 mA*
P_D	Power Dissipation		0.6	W	

*1792 and 1794 I_O = 1.0 mA

**Leakage conditions are for input pins without internal pull-up resistors. Pins 22, 23, 33, 36, and 37 have pull-up resistors. See Tech Memo #115 for testing procedures.

See page 725 for ordering information.

FD179X Application Notes

INTRODUCTION

Over the past several years, the Floppy Disk Drive has become the most popular on-line storage device for mini and microcomputer systems. Its fast access time, reliability and low cost-per-bit ratio enables the Floppy Disk Drive to be *the* solution in mass storage for microprocessor systems. The drive interface to the Host system is standardized, allowing the OEM to substitute one drive for another with minimum hardware/ software modifications.

Since Floppy Disk Data is stored and retrieved as a self-clocking serial data stream, some means of separating the clock from the data and assembling this data in parallel form must be accomplished. Data is stored on individual Tracks of the media, requiring control of a stepper motor to move the Read/Write head to a predetermined Track. Byte sychronization must also be accomplished to insure that the parallel data is properly assembled. After all the design considerations are met, the final controller can consist of 40 or more TTL packages.

To alleviate the burden of Floppy Disk Controller design, Western Digital has developed a Family of LSI Floppy Disk controller devices. Through its own set of macro commands, the FD179X Controller Family will perform all the functions necessary to read and write data to the drive. Both the 8" standard and 5¼" minifloppy are supported with single or double density recording techniques. The FD179X is compatible with the IBM 3740 (FM) data format, or the System 34 (MFM) standards. Provisions for non-standard formats and variable sector lengths have been included to provide more storage capability per track. Requiring standard +5, +12 power supplies the FD179X is available in a standard 40 pin dual-in-line package.

The FD179X Family consists of 6 devices. The differences between these devices is summarized in Figure 1. The 1792 and 1794 are "single density only" devices, with the Double Density Enable pin (DDEN) left open by the user. Both True and inverted Data bus devices are available. Since the 179X can only drive one TTL Load, a true data bus system may use the 1791 with external inverting buffers to arrive at a true bus scheme. The 1795 and 1797 are identical to the 1791 and 1793, except a side select output has been added that is controlled through the Command Register.

SYSTEM DESIGN

The first consideration in Floppy Disk Design is to determine which type of drive to use. The choice ranges from single-density single sided mini-floppy to the 8" double-density double-sided drive. Figure 2 illustrates the various drive and data capacities associated with each type. Although the 8" double-density drive offers twice as much storage, a more complex data separator and the addition of Write Precompensation circuits are mandatory for reliable data transfers. Whether to go with 8" double-density or not is dependent upon PC board space and the additional circuitry needed to accurately recover data with extreme bit shifts. The byte transfer time defines the nominal time required to transfer one byte of data from the drive. If the CPU used cannot service a byte in this time, then a DMA scheme will probably be required. The 179X also needs a few microseconds for overhead, which is subtracted from the transfer time. Figure 3 shows the actual service times that the CPU must provide on a byte-by-byte basis. If these times are not met, bytes of data will be lost during a read or write operation. For each byte transferred, the 179X generates a DRQ (Data Request) signal on Pin 38. A bit is provided in the status register which is also set upon receipt of a byte from the Disk. The user has the option of reading the status register through program control or using the DRQ Line with DMA or interrupt schemes. When the data register is read, both the status register DRQ bit and the DRQ Line are automatically reset. The next full byte will again set the DRQ and the process continues until the sector(s) are read. The Write operation works exactly the same way, except a WRITE to the Data Register causes a reset of both DRQ's.

RECORDING FORMATS

The FD179X accepts data from the disk in a Frequency-Modulated (FM) or Modified-Frequency-Modulated (MFM) Format. Shown in Figures 4A and 4B are both these Formats when writing a Hexidecimal byte of 'D2'. In the FM mode, the 8 bits of data are broken up into "bit cells." Each bit cell begins with a clock pulse and the center of the bit cell defines the data. If the data bit = 0, no pulse is written; if the data = 1, a pulse is written in the center of the cell. For the 8" drive, each clock is written 4 microseconds apart.

In the MFM mode, clocks are decoded into the data stream. The byte is again broken up into bit cells, with the data bit written in the center of the bit cell if data = 1. Clocks are only written if both surrounding data bits are zero. Figure 4B shows that this occurs only once between Bit cell 4 and 5. Using this encoding scheme, pulses can occur 2, 3 or 4 microseconds apart. The bit cell time is now 2 microseconds; twice as much data can be recorded without increasing the Frequency rate due to this encoding scheme.

The 179X was designed to be compatible with the IBM 3740 (FM) and System 34 (MFM) Formats. Although most users do not have a need for data exchange with IBM mainframes, taking advantage of these well studied formats will insure a high degree of system performance. The 179X will allow a change in gap fields and sector lengths to increase usable storage capacity, but variations away from these standards is not recommended. Both IBM standards are soft-sector format. Because of the wide variation in address marks, the 179X can only support soft-sectored media. Hard sectored diskettes have continued to lose popularity, mainly due to the unavailability of a standard and the limitation of sector lengths imposed by the physical sector holes in the diskette.

PROCESSOR INTERFACE

The Interface of the 179X to the CPU consists of an 8-bit Bi-directional bus, read/write controls and optional interrupt lines. By selecting the device via the CHIP SELECT Line, each of the five internal registers can be accessed.

Shown below are the registers and their addresses:

PIN 3 CS	PIN 6 A_1	PIN 5 A_0	PIN 4 $\overline{RE}=\emptyset$	PIN 2 $\overline{WE}=\emptyset$
0	0	0	STATUS REG	COMMAND
0	0	1	TRACK REG	REG
0	1	0	SECTOR REG	TRACK REG
0	1	1	DATA REG	SECTOR REG
1	X	X	H1-Z	DATA REG
				H1-Z

Each time a command is issued to the 179X, the Busy bit is set and the INTRQ (Interrupt Request) Line is reset. The user has the option of checking the busy bit or use the INTRQ Line to denote command completion. The Busy bit will be reset whenever the 179X is idle and awaiting a new command. The INTRQ Line, once set, can only be reset by a READ of the status register or issuing a new command. The MR (Master Reset) Line does not affect INTRQ.

The A_0, A_1, Lines used for register selections can be configured at the CPU in a variety of ways. These lines may actually tie to CPU address lines, in which case the 179X will be memory-mapped and addressed like RAM. They may also be used under Program Control by tying to a port device such as the 8255, 6820, etc. As a diagnostic tool when checking out the CPU interface, the Track and Sector registers should respond like "RAM" when the 179X is idle (Busy = INTRQ = 0).

Because of internal synchronization cycles, certain time delays must be introduced when operating under Programmed I/O. The worst case delays are:

OPERATION	NEXT OPERATION	DELAY REQ'D
WRITE TO COMMAND REG	READ STATUS REGISTER	MFM = 14μs* FM = 28μs.
WRITE TO ANY REGISTER	READ FROM A DIFFERENT REG	NO DELAY

*NOTE: Times Double when CLK = 1MHz (5¼" drive)

Other CPU interface lines are CLK, $\overline{MR}$ and $\overline{DDEN}$. The CLK line should be 2MHz (8" drive) or 1MHz (5¼" drive) with a 50% duty cycle. Accuracy should be ±1% (crystal source) since all internal timing, including stepping rates, are based upon this clock.

The $\overline{MR}$ or Master Reset Line should be strobed a minimum of 50 microseconds upon each power-on condition. This line clears and initializes all internal registers and issues a restore command (Hex '03') on the rising edge. A quicker stepping rate can be written to the command register after a $\overline{MR}$, in which case the remaining steps will occur at the faster programmed rate. The 179X will issue a maximum of 255 stepping pulses in an attempt to expect the $\overline{TROO}$ line to go active low. This line should be connected to the drive's $\overline{TROO}$ sensor.

The $\overline{DDEN}$ line causes selection of either single density ($\overline{DDEN}$ = 1) or double density operation. $\overline{DDEN}$ should not be switched during a read or write operation.

FLOPPY DISK INTERFACE

The Floppy Disk Interface can be divided into three sections: Motor Control, Write Signals and Read Signals. All of these lines are capable of driving one TTL load and not compatible for direct connection to the drive. Most drives require an open-collector TTL interface with high current drive capability. This must be done on all outputs from the 179X. Inputs to the 179X may be buffered or tied to the Drives outputs, providing the appropriate resistor termination networks are used. Undershoot should not exceed −0.3 volts, while integrity of V_{IH} and V_{OH} levels should be kept within spec.

MOTOR CONTROL

Motor Control is accomplished by the STEP and DIRC Lines. The STEP Line issues stepping pulses with a period defined by the rate field in all Type I commands. The DIRC Line defines the direction of steps (DIRC = 1 STEP IN/DIRC = 0 STEP OUT).

Other Control Lines include the $\overline{IP}$ or Index Pulse. This Line is tied to the drives' Index L.E.D. *sensor* and makes an active transition for each revolution of the diskette. The $\overline{TROO}$ Line is another L.E.D. sensor that informs the 179X that the stepper motor is at its furthest position, over Track 00. The READY Line can be used for a number of functions, such as sensing "door open", Drive motor on, etc. Most drives provide a programmable READY Signal selected by option jumpers on the drive. The 179X will look at the ready signal prior to executing READ/WRITE commands. READY is *not* inspected during any Type I commands. All Type I commands will execute regardless of the Logic Level on this Line.

WRITE SIGNALS

Writing of data is accomplished by the use of the WD, WG, WF, TG43, EARLY and LATE Lines. The WG or Write Gate Line is used to enable write current at the drive's R/W head. It is made active prior to writing data on the disk. The WF or WRITE FAULT Line is used to inform the 179X of a failure in drive electronics. This signal is multiplexed with the VFOE Line and must be logically separated if required. Figure 5 illustrates three methods of demultiplexing.

The TG43 or "TRACK GREATER than 43" Line is used to decrease the Write current on the inner tracks, where bit densities are the highest. If not required on the drive, TG43 may be left open.

WRITE PRECOMPENSATION

The 179X provides three signals for double density Write Precompensation use. These signals are WRITE DATA, EARLY and LATE. When using single density drives (eighter 8" or 5¼"), Write Precompensation is not necessary and the WRITE DATA line is generally TTL Buffered and sent directly to the drive. In this mode, EARLY and LATE are left open.

For double density use, Write Precompensation is a function of the drive. Some manufacturers recommend Precompensating the 5¼" drive, while others do not. With the 8" drive, Precompensation may be specified from TRACK 43 on, or in most cases, all TRACKS. If the recommended Precompensation is not specified, check with the manufacturer for the proper configuration required.

The amount of Precompensation time also varies. A typical value will usually be specified from 100-300ns. Regardless of the parameters used, Write Precompensation must be done external to the 179X. When $\overline{DDEN}$ is tied low, EARLY or LATE will be activated at least 125ns. before and after the Write Data pulse. An Algorithm internal the 179X decides whether to raise EARLY or LATE, depending upon the previous bit pattern sent. As an example, suppose the recommended Precomp value has been specified at 150ns. The following action should be taken:

EARLY	LATE	ACTION TAKEN
0	0	delay WD by 150ns (nominal)
0	1	delay WD by 300ns (2X value)
1	0	do not delay WD

There are two methods of performing Write Precompensation:

1) External Delay elements
2) Digitally

Shown in Figure 6 is a Precomp circuit using the Western Digital 2143 clock generator as the delay element. The WD pulse from the 179X creates a strobe to the 2143, causing subsequent output pulses on the Ø1, Ø2 and Ø3 signals. The 5K Precomp adjust sets the desired Precomp value. Depending upon the condition of EARLY and LATE, Ø1 will be used for EARLY, Ø2 for nominal (EARLY = LATE = 0), and Ø3 for LATE. The use of "one-shots" or delay line in a Write Precompensation scheme offers the user the ability to vary the Precomp value. The Ø4 output resets the 74LS175 Latch in anticipation of the next WD pulse. Figure 7 shows the WD-EARLY/LATE relationship, while Figure 8 shows the timing of this write Precomp scheme.

Another method of Precomp is to perform the function digitally. Figure 9 illustrates a relationship between the WD pulse and the CLK pin, allowing a digital Precomp scheme. Figure 10 shows such a scheme with a preset Write Precompensation value of 250ns. The synchronous counter is used to generate 2MHz and 4MHz clock signals. The 2MHz clock is sent to the CLK input of the 179X and the 4MHz is used by the 4-bit shift register. When a WD pulse is not present, the 4MHz clock is shifting "ones" through the shift register and maintaining Q_D at a zero level. When a WD pulse is present, a zero is loaded at either A, B, or C depending upon the states of LATE, EN PRECOMP and EARLY. The zero is then shifted by the 4MHz clock until it reaches the Q_D output. The number of shift operations determines whether the WRITE DATA pulse is written early, nominal or late. If both FM and MFM operations is a system requirement, the output of this circuit should be disabled and the WD pulse should be sent directly to the drive.

DATA SEPARATION

The 179X has two inputs (RAW READ & RCLK) and one output (VFOE) for use by an external data separator. The RAW READ input must present clock and data pulses to the 179X, while the RCLK input provides a "window" or strobe signal to clock each RAW READ pulse into the device. An ideal Data Separator would have the leading edge of the RAW READ pulse occur in the exact center of the RCLK strobe.

Motor Speed Variation, Bit shifts and read amplifier recovery circuits all cause the RAW READ pulses to drift away from their nominal positions. As this occurs, the RAW READ pulses will shift left or right with respect to RCLK. Eventually, a pulse will make its transition outside of its RCLK window, causing either a CRC error or a Record-not-Found error at the 179X.

A Phase-Lock-Loop circuit is one method of achieving synchronization between the RCLK and RAW READ signals. As RAW READ pulses are fed to the PLL, minor adjustments of the free-running RCLK frequency can be made. If pulses are occurring too far apart, the RCLK frequency is *decreased* to keep synchronization. If pulses begin to occur closer together, RCLK is *increased* until this new higher frequency is achieved. In normal read operations, RCLK will be constantly adjusted in an attempt to match the incoming RAW READ frequency.

Another method of Data Separation is the Counter-Separator technique. The RCLK signal is again free-running at a nominal rate, until a RAW READ pulse occurs. The Separator then denotes the position of the pulse with respect to RCLK (by the counter value), and counts down to increase or decrease the current RCLK window. The next RCLK window will occur at a nominal rate and will continue to run at this frequency until another RAW READ pulse adjusts RCLK, but only the present window is adjusted.

Both PPL and Counter/Separator are acceptable methods of Data Separation. The PPL has the highest reliability because of its "tracking" capability and is recommended for 8" double density designs.

As a final note, the term "Data Separator" may be misleading, since the physical separation of clock and data bits are not actually performed. This term is used throughout the industry, and can better be described as a "Data Recovery Circuit" rather than a Data Separator.

The VFOE signal is an output from the 179X that signifies the head has been loaded and valid data pulses are appearing on the RAW READ line. It can be used to enable the Data Separator and to insure clean RCLK transitions to the 179X. Since some drives will output random pulses when the head is disengaged, VFOE can prevent an erratic RCLK signal during this time. If the Data Separator requires synchronization during a known pattern of one's or zero's, then RG (READ GATE) can be used. The RG signal will go active when the 179X is currently over a field of zeros or ones. RG is not available on the 1795/1797 devices, since this signal was replaced with the SSO (Side Select Output) Line.

Shown in Figure 11 is a 2½ IC Counter/Separator. The 74LS193 free runs at a frequency determined by the CRYCLK input. When a RAW READ pulse occurs, the counter is loaded with a starting count of '5'. When the RAW READ Line returns to a Logic 1, the counter counts down to zero and again free runs. The 74LS74 insures a 50% duty cycle to the 179X and performs a divide-by-two of the Q_D output.

Figure 12 illustrates another Counter/Separator utilizing a PROM as the count generator. Depending upon the RAW READ phase relationship to RCLK, the PROM is addressed and its data output is used as the counter value. A 16MHz clock is required for 8" double density, while an 8MHz clock can be used for single density.

Figure 13 shows a Phase-Lock-Loop data recovery circuit. The phase detector (U2, Figure 2) compares the phase of the SHAPED DATA pulse to the phase of VFO CLK ÷ 2. If VFO CLK ÷ 2 is lagging the SHAPED DATA pulse an output pulse on #9, U2 is generated. The filter/amplifier converts this pulse into a DC signal which increases the frequency of the VCO.

If, correspondingly, CLK ÷ 2 is leading the SHAPED DATA pulse, an output pulse on #5, U2 is generated. This pulse is converted into a DC signal which decreases the frequency of the VCO. These two actions cause the VCO to track the frequency of the incoming READ DATA pulses. This correction process to keep the two signals in phase is constantly occurring because of spindle speed variation and circuit parameter variations.

The operating specifications for this circuit are as follows:

Free Running Frequency	2MHz
Capture Range	± 15%
Lock Up Time	50 microsec. "1111" or "0000" Pattern 100 Microsec "1010" Pattern

The RAW READ pulses are generated from the falling edge of the SHAPED DATA pulses. The pulses are also reshaped to meet the 179X requirements. VFO CLK ÷ 2 OR 4 is divided by 2 once again to obtain VFO CLK OUT whose frequency is that required by the 179X RCLK input. RCLK must be controlled by VFOE so VFOE is sampled on each rising edge of VFO CLK OUT. When VFOE goes active EN RCLK goes active in synchronization with VFO CLK OUT preventing any glitches on the RCLK output. When VFOE goes inactive EN RCLK goes inactive in synchronization with VFO CLK OUT, again preventing any glitches on the RCLK output.

Figure 14 illustrates a PPL data recovery circuit using the Western Digital 1691 Floppy Support device. Both data recovery and Write Precomp Logic is contained within the 1691, allowing low chip count and PLL reliability. The 74S124 supplies the free-running VCO output. The PUMP UP and PUMP DOWN signals from the 1691 are used to control the 74S124's frequency.

COMMAND USAGE

Whenever a command is successfully or unsuccessfully completed, the busy bit of the status register is reset and the INTRQ line is forced high. Command termination may be detected either way. The INTRQ can be tied to the host processor's interrupt with an appropriate service routine to terminate commands. The busy bit may be monitored with a user program and will achieve the same results through software. Performing both an INTRQ and a busy bit check is not recommended because a read of the status register to determine the condition of the busy bit will reset the INTRQ line. This can cause an INTRQ from not occurring.

RESTORE COMMAND

On some disk drives, it is possible to position the R/W head outward past Track 00 and prevent the TROO line from going low unless a STEP IN is first performed. If this condition exists in the drive used, the RESTORE command will never detect a TROO. Issuing several STEP IN pulses before a RESTORE command will remedy this situation. The RESTORE and all other Type I commands will execute even though the READY bit indicates the drive is not ready (NOT READY = 1).

READ TRACK COMMAND

The READ TRACK command can be used to manually inspect data on a hard copy printout. Gaps, address marks and all data are brought in to the data register during this command. The READ TRACK command may be used to inspect diskettes for valid formatting and data fields as well as address marks. Since the 179X does not synchronize clock and data until the Index Address Mark is detected, data previous to this ID mark will not be valid. READ GATE (RG) is not actuated during this command.

READ ADDRESS COMMAND

In systems that use either multiple drives or sides, the read address command can be used to tell the host processor which drive or side is selected. The current position of the R/W head is also denoted in the six bytes of data that are sent to the computer.

TRACK	SIDE	SECTOR	CRS LENGTH	CRC 1	CRC 2

The READ ADDRESS command as well as all other Type II and Type III commands will not execute if the READY line is inactive (READY = 0). Instead, an interrupt will be generated and the NOT READY status bit will be set to a 1.

FORCED INTERRUPT COMMAND

The Forced Interrupt command is generally used to terminate a multiple sector command or to insure Type I status in the status register. The lower four bits of the command determine the conditional interrupt as follows:

I_0 = NOT-READY TO READY TRANSITION
I_1 = READY TO NOT-READY TRANSITION
I_2 = EVERY INDEX PULSE
I_3 = IMMEDIATE INTERRUPT

Regardless of the conditional interrupt set, any command that is currently being executed when the Forced Interrupt command is loaded will immediately be terminated and the busy bit will be reset indicating an idle condition.

Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred.

The conditional interrupt is enabled when the corresponding bit positions of the command ($I_3 - I_0$) are set to a 1. If $I_3 - I_0$ are all set to zero, no interrupt will occur, but any command presently under execution will be immediately terminated upon receipt of the Force Interrupt command (HEX DO).

As usual, to clear the interrupt a read of the status register or a write to the command register is required. The exception is when using the immediate interrupt condition (I_3 = 1). If this command is loaded into the command register, an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt; another forced interrupt command with $I_3 - I_0$ = 0 must be loaded into the command register in order to reset the INTRQ from this condition.

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I_1 = 1) and the Every Index Pulse (I_2 = 1) are both set, the resultant command would be HEX "DA". The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.

DATA RECOVERY

Occasionally, the R/W head of the disk drive may get "off track", and dust or dirt may get trapped on the media. Both of these conditions will cause a RECORD NOT FOUND and/or a CRC error to occur. This "soft error" can usually be recovered by the following procedure:

1. Issue the command again
2. Unload and load the head and repeat step
3. Issue a restore, seek the track, and repeat step 1

If RNF or CRC errors are still occurring after trying these methods, a "hard error" may exist. This is usually caused by improper disk handling, exposure to high magnetic fields, etc. and generally results in destroying portions or tracks of the diskette.

FIGURE 1. DEVICE CHARACTERISTICS

DEVICE	SNGL DENSITY	DBLE DENSITY	INVERTED BUS	TRUE BUS	DOUBLE-SIDED
1791	X	X	X		
1792	X		X		
1793	X	X		X	
1794	X			X	
1795	X	X	X		X
1797	X	X		X	X

FIGURE 2. STORAGE CAPACITIES

SIZE	DENSITY	SIDES	UNFORMATTED CAPACITY (NOMINAL)		BYTE TRANSFER TIME	FORMATTED CAPACITY	
			PER TRACK	PER DISK		PER TRACK	PER DISK
5¼″	SINGLE	1	3125	109,375*	64μs	2304**	80,640
5¼″	DOUBLE	1	6250	218,750	32μs	4608***	161,280
5¼″	SINGLE	2	3125	218,750	64μs	2304	161,280
5¼″	DOUBLE	2	6250	437,500	32μs	4608	322,560
8″	SINGLE	1	5208	401,016	32μs	3328	256,256
8″	DOUBLE	1	10,416	802,032	16μs	6656	512,512
8″	SINGLE	2	5208	802,032	32μs	3328	512,512
8″	DOUBLE	2	10,416	1,604,064	16μs	6656	1,025,024

*Based on 35 Tracks/Side
**Based on 18 Sectors/Track (128 byte/sec)
***Based on 18 Sectors/Track (256 bytes/sec)

FIGURE 3. NOMINAL VS. WORSE CASE SERVICE TIME

SIZE	DENSITY	NOMINAL TRANSFER TIME	WORST-CASE 179X SERVICE TIME	
			READ	WRITE
5¼"	SINGLE	64μs	55.0μs	47.0μs
5¼"	DOUBLE	32μs	27.5μs	23.5μs
8"	SINGLE	32μs	27.5μs	23.5μs
8"	DOUBLE	16μs	13.5μs	11.5μs

FIGURE 4A. FM RECORDING

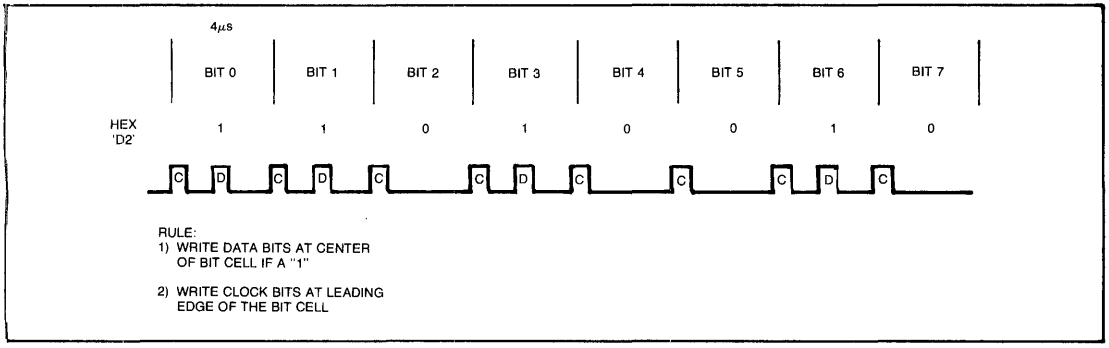


FIGURE 4B. MFM RECORDING

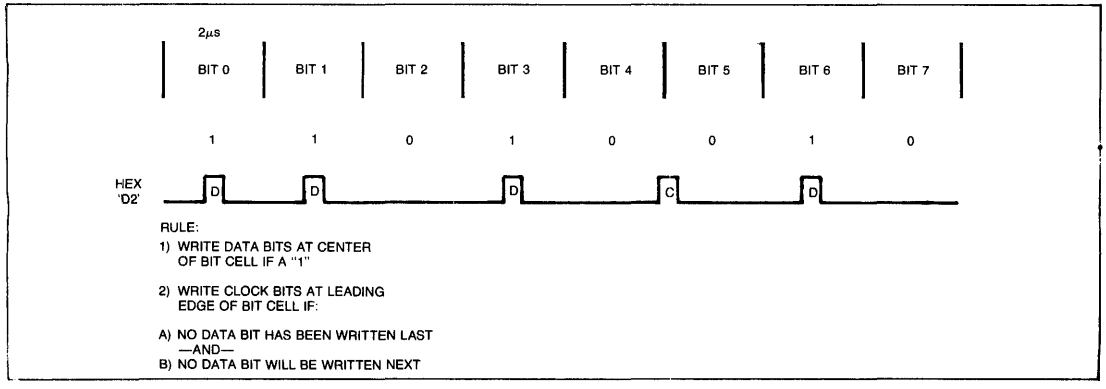
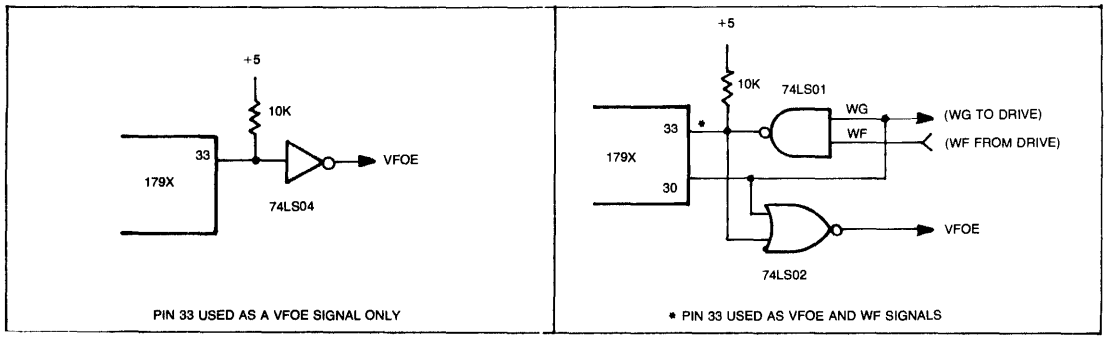


FIGURE 5. WF/VFOE DEMULTIPLEXING CIRCUITRY



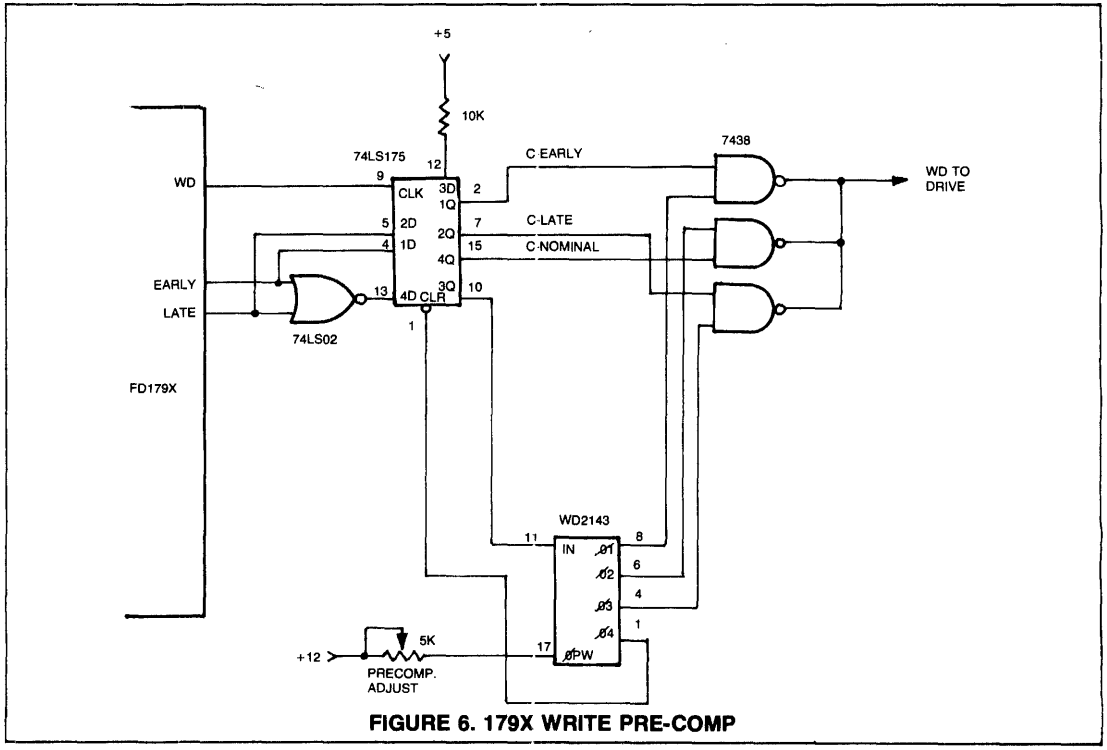


FIGURE 6. 179X WRITE PRE-COMP

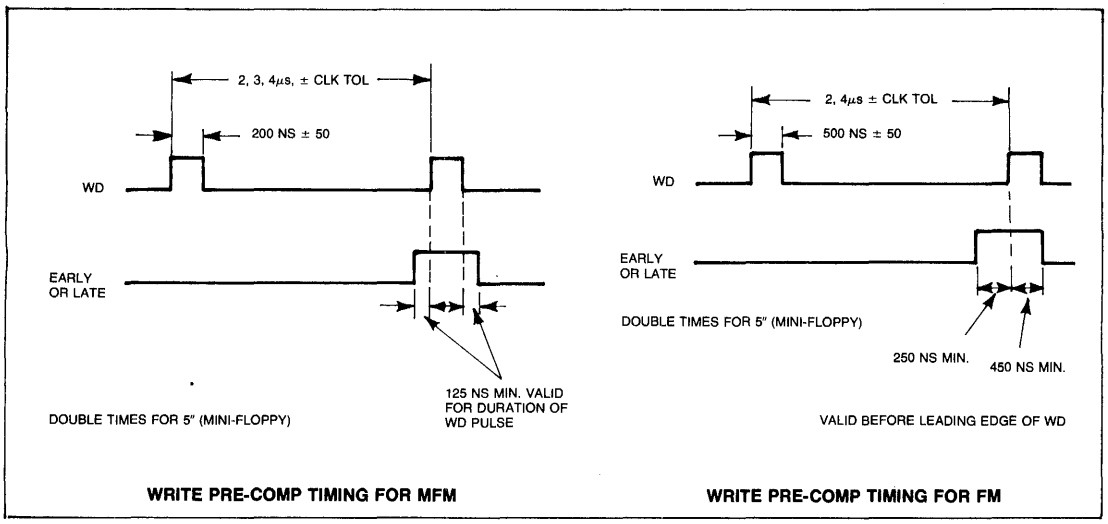


FIGURE 7. WRITE PRE-COMP TIMING

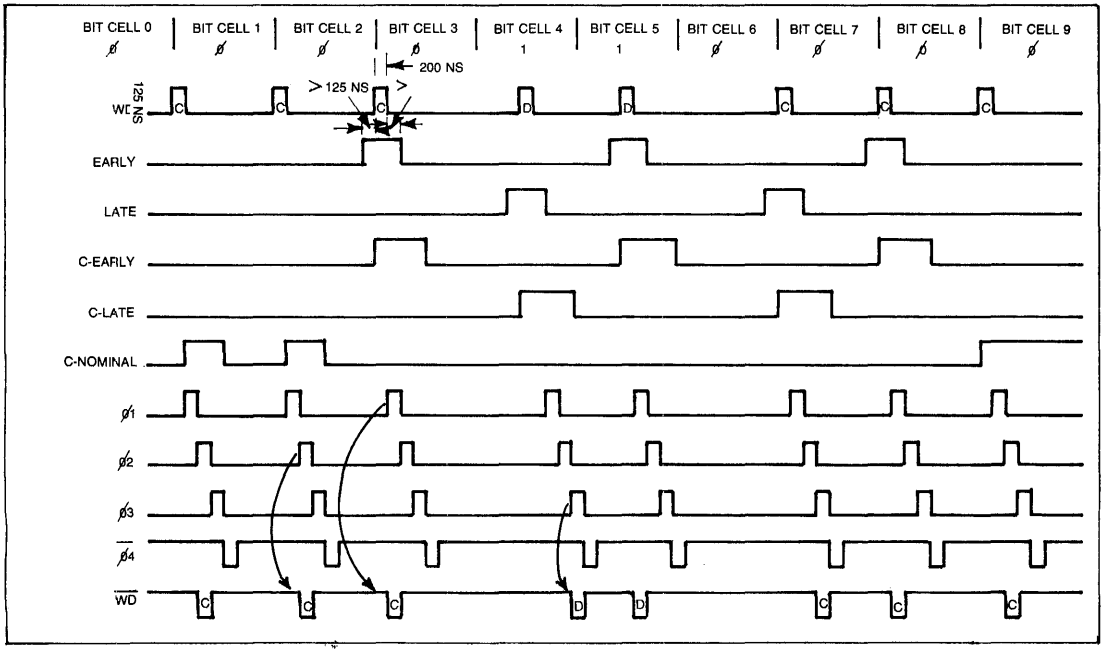


FIGURE 8. PRECOMP TIMING FOR CIRCUIT IN FIGURE 6

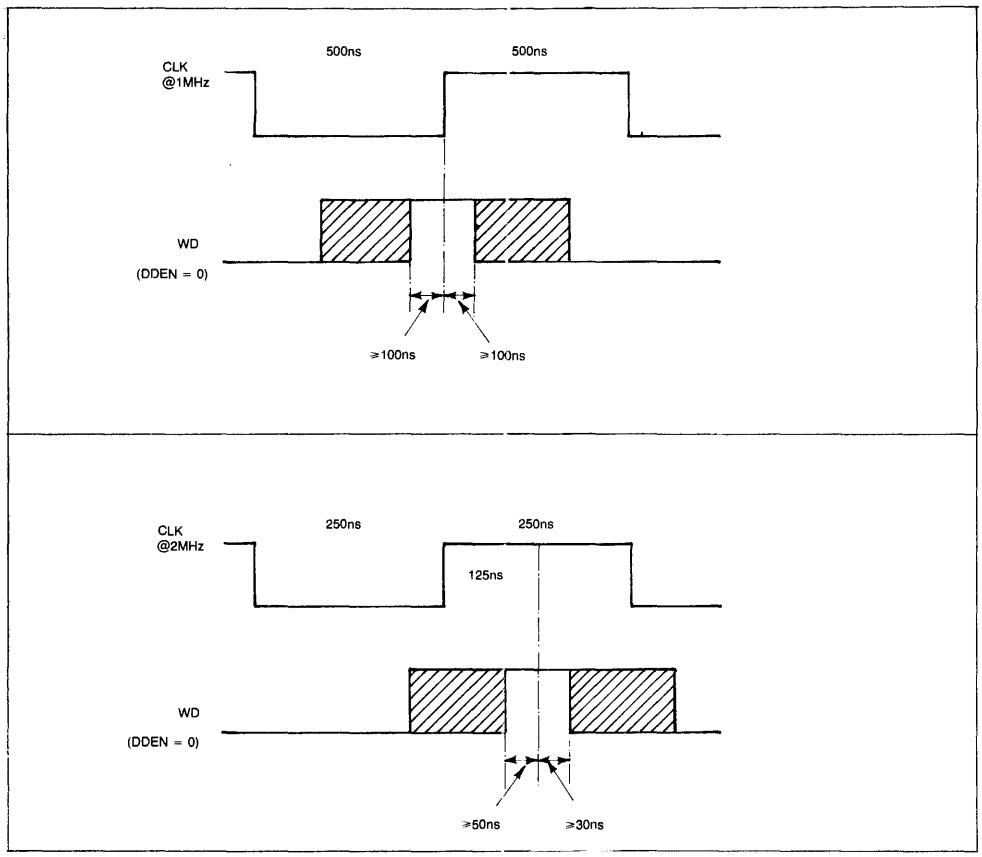


FIGURE 9. WD/CLK RELATIONSHIP FOR WRITE PRECOMP USE

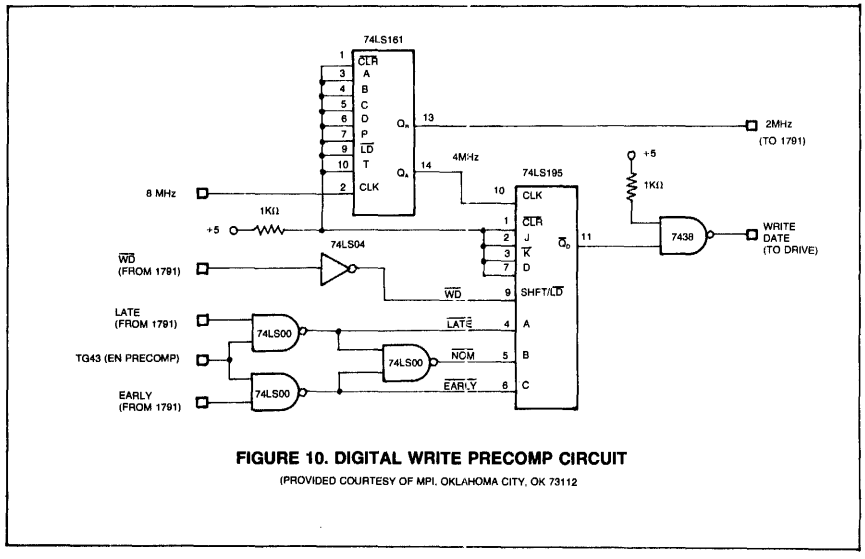
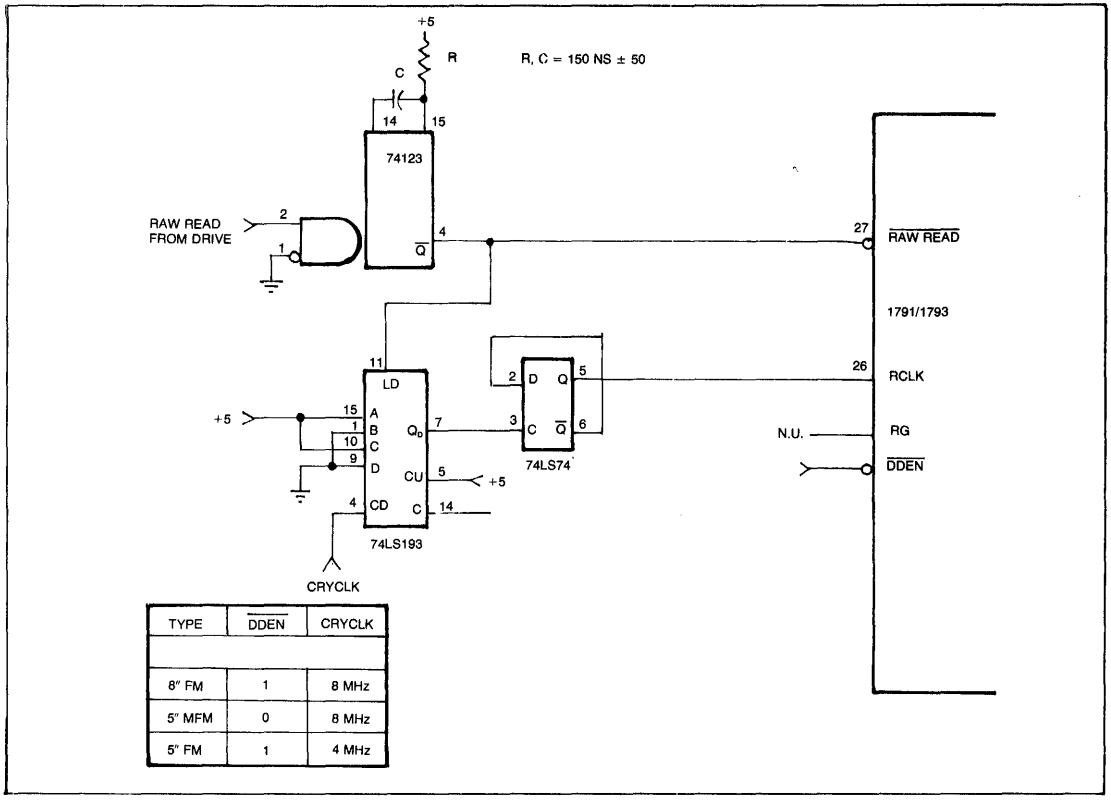


FIGURE 10. DIGITAL WRITE PRECOMP CIRCUIT

(PROVIDED COURTESY OF MPI, OKLAHOMA CITY, OK 73112



TYPE	$\overline{\text{DDEN}}$	CRYCLK
8" FM	1	8 MHz
5" MFM	0	8 MHz
5" FM	1	4 MHz

FIGURE 11. COUNTER/SEPARATOR

745288 PROGRAMMING TABLE

ADDRESS	DATA	ACTION TAKEN
00	01	NONE
01	01	RETARD BY 1 COUNT
02	02	
03	03	
04	03	RETARD BY 2 COUNTS
05	04	
06	05	
07	06	
08	0B	ADVANCE BY 2 COUNTS
09	0D	
0A	0C	
0B	0E	
0C	0F	
0D	0F	ADVANCE BY 1 COUNT
0E	00	
0F	01	
10	01	FREE RUN
11	02	
12	03	
13	04	
14	05	
15	06	
16	07	
17	08	
18	09	
19	0A	
1A	0B	
1B	0C	
1C	0D	
1D	0E	
1E	0F	
1F	00	

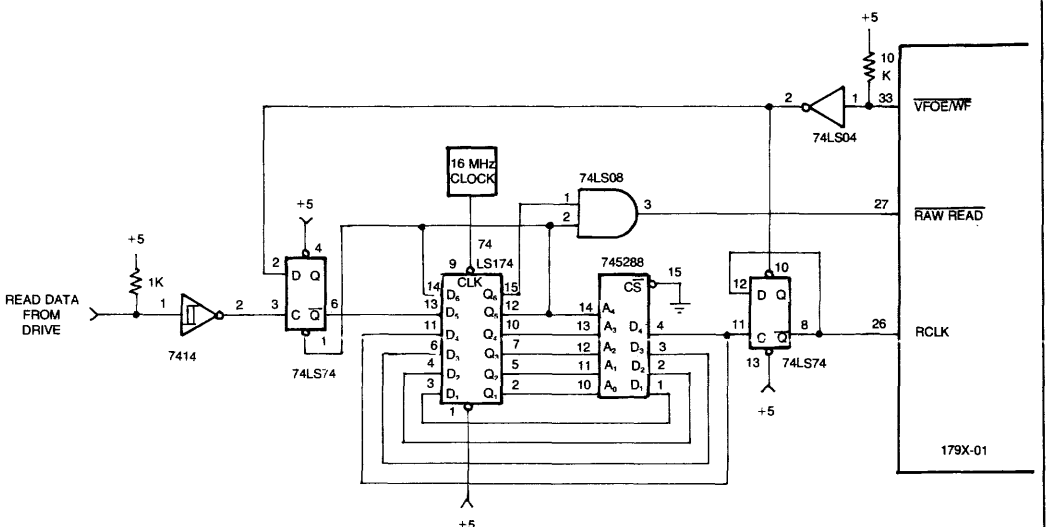


FIGURE 12. 179X DATA SEPARATOR

(PROVIDED COURTESY OF ANDROMEDA SYSTEMS, PANORAMA CITY, CA 91402)

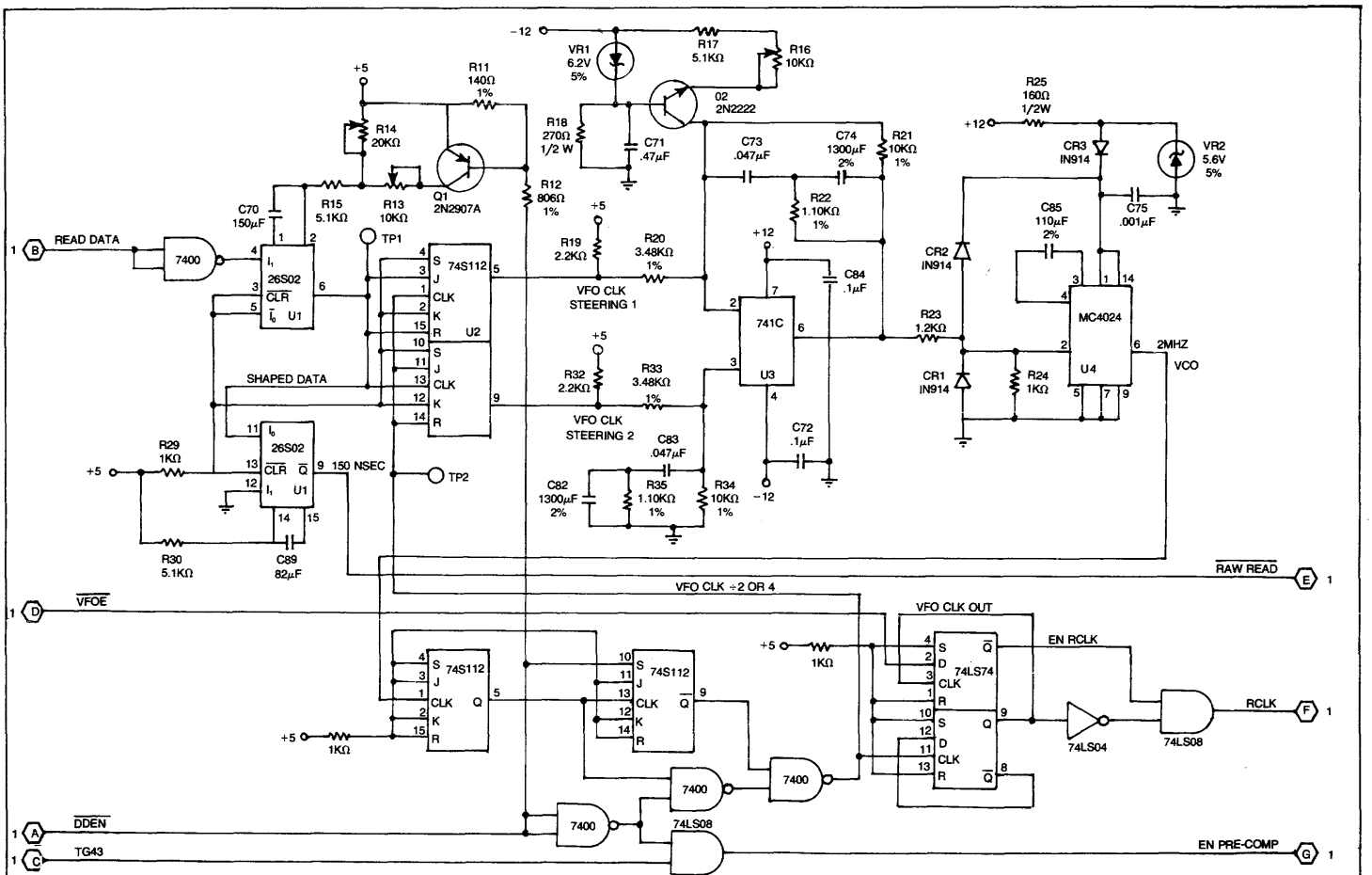


FIGURE 13. PLL DATA RECOVERY CIRCUIT

(PROVIDED COURTESY OF MPI, OKLAHOMA CITY, OK 73112)

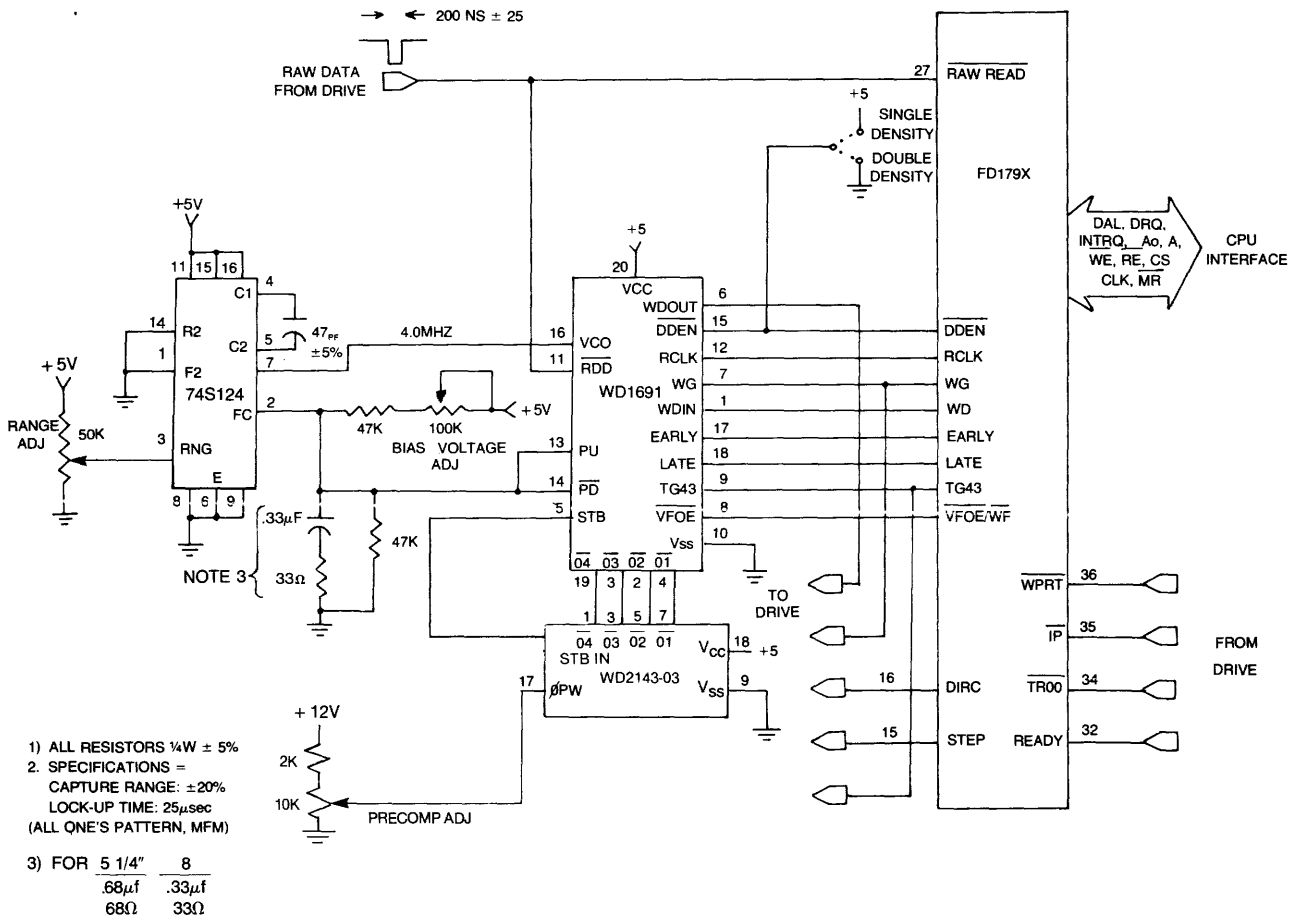


FIGURE 14. 8" SINGLE/DOUBLE DENSITY SYSTEM

Refer to 179X-02 Floppy Disk Formatter/Controller Family Data Sheet for Command, Timing and Status Information.

See page 725 for ordering information.

Printed in U.S.A.

WD279X-02 Floppy Disk Formatter/Controller Family

FEATURES

- ON-CHIP PLL DATA SEPARATOR
- ON-CHIP WRITE PRECOMPENSATION LOGIC
- SINGLE +5V SUPPLY
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 (FM)
  - IBM 34 (MFM)
- AUTOMATIC SEEK WITH VERIFY
- MULTIPLE SECTOR READ/WRITE
- TTL COMPATIBLE
- PROGRAMMABLE CONTROL
  - SELECTABLE TRACK-TO-TRACK ACCESS
  - HEAD LOAD TIMING
- SOFTWARE COMPATIBLE WITH THE FD179X SERIES
- SOFT SECTOR FORMAT COMPATIBILITY

APPLICATIONS

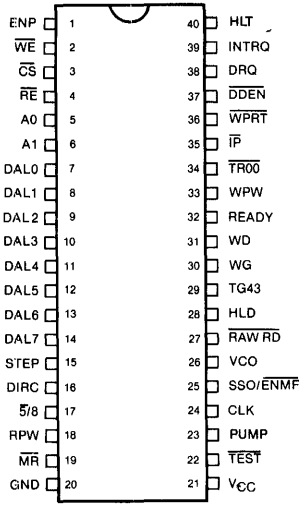
8" FLOPPY AND 5¼" MINI FLOPPY CONTROLLER
SINGLE OR DOUBLE DENSITY
CONTROLLER/FORMATTER

The WD279X Family are MOS/LSI devices which perform the functions of a Floppy Disk Controller/Formatter. Software compatible with its predecessor, the FD179X, the device also contains a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic.

When operating in Double Density mode, Write Precompensation is automatically engaged to a value programmed via an external potentiometer. An on-chip VCO and phase comparator allows adjustable frequency range for 5¼" or 8" Floppy Disk interfacing.

The WD279X is fabricated in NMOS silicon gate technology and available in a 40 pin dual-in-line ceramic or plastic package.

FEATURES	2791	2793	2795	2797
Single Density (FM)	X	X	X	X
Double Density (MFM)	X	X	X	X
True Data Bus		X		X
Inverted Data Bus	X		X	
Side Select Out			X	X
Internal CLK Divide	X	X		



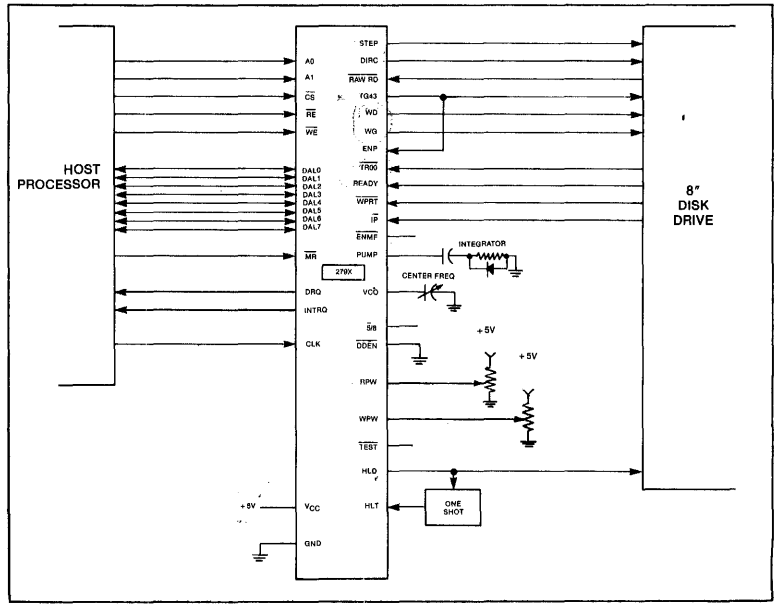


Figure 1.

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	ENABLE PRECOMP	ENP	A Logic high on this input enables write precompensation to be performed on the Write Data output.
19	MASTER RESET	$\overline{MR}$	A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during MR ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ±5%
COMPUTER INTERFACE:			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5, 6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: $\overline{CS}$ A1 A0 $\overline{RE}$ $\overline{WE}$ 0 0 0 Status Reg Command Reg 0 0 1 Track Reg Track Reg 0 1 0 Sector Reg Sector Reg 0 1 1 Data Reg Data Reg
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit bi-directional bus used for transfer of commands, status, and data. These lines are inverted (active low) on WD2791 and WD2795.
24	CLOCK	CLK	This input requires a free-running 50% duty cycle square wave clock for internal timing reference, 2 MHz ± 1% for 8" drives, 1 MHz ± 1% for mini-floppies.
38	DATA REQUEST	DRQ	This output indicates that the Data Register contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR.
39	INTERRUPT REQUEST	INTRQ	This output is set at the completion of any command and is reset when the Status register is read or the Command register is written to.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	5¼," 8" SELECT	$\overline{5}/8$	This input selects the internal VCO frequency for use with 5¼" drives or 8" drives.
18	READ PULSE WIDTH	RPW	An external potentiometer tied to this input controls the phase comparator within the data separator.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	A logic low on this input allows adjustment of external resistors by enabling internal signals to appear on selected pins.
23	PUMP	PUMP	High-Impedance output signal which is forced high or low to increase/decrease the VCO frequency.
25	ENABLE MINI-FLOPPY (2791, 2793)	$\overline{\text{ENMF}}$	A logic low on this input enables an internal ÷2 of the Master Clock when $\overline{5/8}$ is also at a logic 0. This allows both 5¼" and 8" drive operation with a single 2 MHz clock. For a 1 MHz clock on Pin 24, this line must be left open or tied to a Logic 1.
25	SIDE SELECT OUTPUT (2795, 2797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the Sector I.D. Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	VOLTAGE-CONTROLLED OSCILLATOR	VCO	An external capacitor tied to this pin adjusts the VCO center frequency.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	A 250ns (MFM) or 500 ns (FM) output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	WRITE PRECOMP WIDTH	WPW	An external potentiometer tied to this input controls the amount of delay in Write precompensation mode.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the WD279X that the Read/Write head is positioned over Track 00.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	This input informs the WD279X when the index hole is encountered on the diskette.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
36	WRITE PROTECT	$\overline{WPRT}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	DOUBLE DENSITY	$\overline{DDEN}$	This input pin selects either single or double density operation. When $\overline{DDEN}$ = 0, double density is selected. When $\overline{DDEN}$ = 1, single density is selected.
40	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD.

GENERAL DESCRIPTION

The WD279X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The WD279X, which can be considered the end result of both the FD1771 and FD179X designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The WD279X contains all the features of its predecessor the FD179X plus a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic. In Double Density mode, Write Precompensation is automatically engaged to a value programmed via an external potentiometer. In order to maintain compatibility, the FD1771, FD179X and WD279X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The WD279X is set up to operate on a multiplexed bus with other bus-oriented devices.

The WD279X is TTL compatible on all inputs and outputs. The outputs will drive one TTL load or three LS loads. The 2793 is identical to the 2791 except the DAL lines are TRUE for systems that utilize true data busses.

The 2795/7 has a side select output for controlling double sided drives.

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input ($\overline{RAW\ READ}$) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations in Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

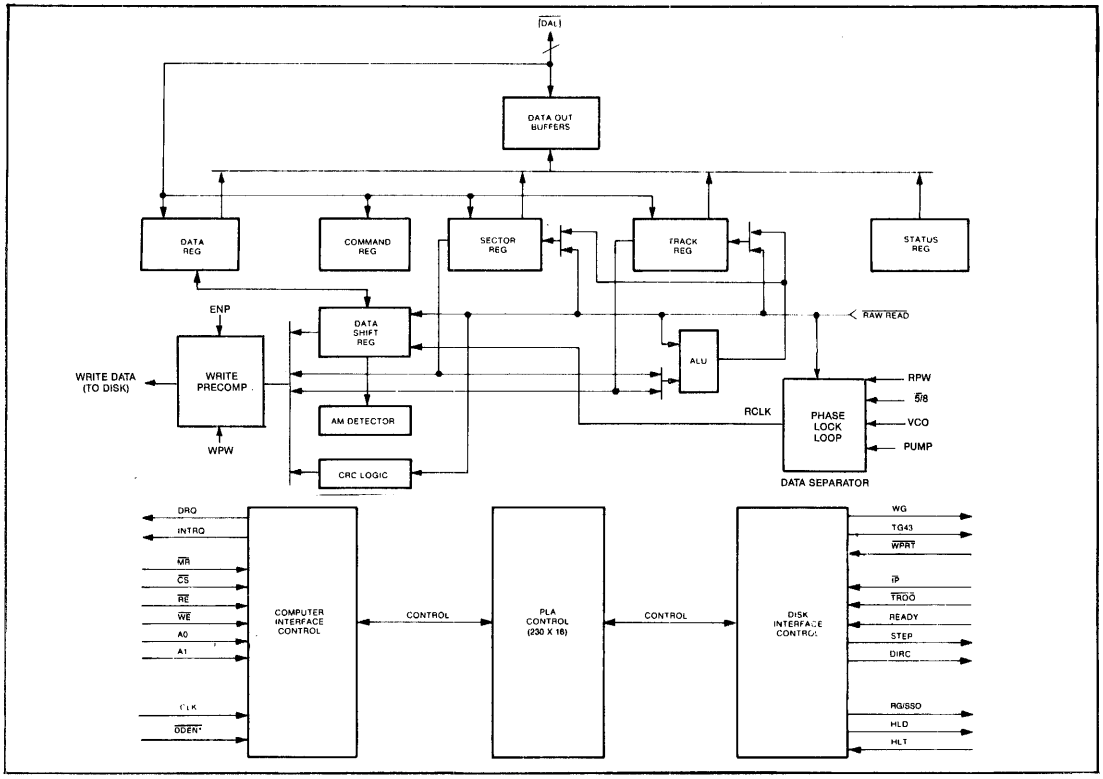
The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control — All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

AM Detector — The address mark detector detects ID, data and index address marks during read and write operations.

Write Precompensation — enables write precompensation to be performed on the Write Data output.



WD279X BLOCK DIAGRAM

Data Separator — a high performance Phase-Lock-Loop Data Separator with on-chip VCO and phase comparator allows adjustable frequency range for 5¼" or 8" Floppy Disk interfacing.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the WD279X. The DAL are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1	A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the WD279X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The 279X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, Single Density (FM) is selected. When $\overline{DDEN}$ = 0, Double Density (MFM) is selected. In either case, the CLK input (Pin 24) is set at 2 MHz for 8" drives or 1 MHz for 5¼" drives.

On the 2791/2793, the $\overline{ENMF}$ input (Pin 25) can be used for controlling both 5¼" and 8" drives with a single 2 MHz clock. When $\overline{ENMF}$ = 0, an internal ÷ 2 of the CLK is performed. When $\overline{ENMF}$ = 1, no divide takes place. This allows the use of a 2 MHz clock for both 5¼" and 8" configurations.

The internal VCO frequency must also be set to the proper value. The $\overline{5/8}$ input (Pin 17) is used to select data separator operation by internally dividing the Read Clock. When $\overline{5/8}$ = 0, 5¼" data separation is selected; when 5/8 = 1, 8" drive data separation is selected.

CLOCK (24)	$\overline{ENMF}$ (25)	$\overline{5/8}$ (17)	DRIVE
2 MHz	1	1	8"
2 MHz	0	0	5¼"
1 MHz	1	0	5¼"

Note: All other conditions invalid.

FUNCTIONAL DESCRIPTION

The WD279X-02 is software compatible with the FD179X-02 series of Floppy Disk Controllers. Commands, status, and data transfers are performed in the same way. Software generated for the 179X can be transferred to a 279X system without modification.

In addition to the 179X, the 279X contains an internal Data Separator and Write precompensation circuit. The $\overline{TEST}$ (Pin 22) line is used to adjust both data separator and precompensation. When $\overline{TEST}$ = 0, the WD (Pin 31) line is internally connected to the output of the write precomp one-shot. Adjustment of the WPW (Pin 33) line can then be accomplished. A second one-shot tracks the precomp setting at approximately 3:1 to insure adequate Write Data pulse widths to meet drive specifications.

Similarly, Data separation is also adjusted with $\overline{TEST}$ = 0. The TG43 (Pin 29) line is internally connected to the output of the read data one-shot, which is adjusted via the RPW (Pin 18) line. The DIRC (Pin 16) line contains the Read Clock output (.5 MHz for 8" drives). The VCO Trimming capacitor (Pin 26) is adjusted for center frequency.

Internal timing signals are used to generate pulses during the adjustment mode so that these adjustments can be made while the device is in-circuit. The $\overline{TEST}$ line also contains a pull-up resistor, so adjustments can be performed simply by grounding the $\overline{TEST}$ pin, overriding the pull-up. The $\overline{TEST}$ pin cannot be used to disable stepping rates during operation as its function is quite different from the 179X.

Other pins on the device also include pull-up resistors and may be left open to satisfy a Logic 1 condition. These are: ENP, $\overline{5/8}$, $\overline{ENMF}$, $\overline{WPRT}$, and $\overline{DDEN}$.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1." For MFM formats, $\overline{DDEN}$ should be placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

Sector Length Table*	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

*2795/97 may vary — see command summary.

The number of sectors per track as far as the 279X is concerned can be from 1 to 255 sectors. The number of tracks as far as the 279X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the 279X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{Write\ Protect}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.

For write operations, the 279X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of pulses set to a width approximately three times greater than the precomp adjustment. Write Data provides the unique address marks in both formats.

READY

Whenever a Read or Write command (Type II or III) is received the 297X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated. TG43 may be tied to ENP to enable write precompensation on tracks 44-76.

COMMAND DESCRIPTION

The WD279X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

TABLE 1. COMMAND SUMMARY

A. Commands for Models: 2791, 2793

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

B. Commands for Models: 2795, 2797

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	L	E	U	a_0
III	Read Address	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

TABLE 2. FLAG SUMMARY

FLAG SUMMARY

Command Type	Bit No(s)		Description
I	0, 1	r_1 r_0 = Stepping Motor Rate See Table 3 for Rate Summary	
I	2	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track
I	3	h = Head Load Flag	h = 0, Unload head at beginning h = 1, Load head at beginning
I	4	T = Track Update Flag	T = 0, No update T = 1, Update track register
II & III	0	a_0 = Data Address Mark	a_0 = 0, FB (DAM) a_0 = 1, F8 (deleted DAM)
II	1	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare
II & III	1	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1
II & III	2	E = 15 MS Delay	E = 0, No. 15 MS delay E = 1, 15 MS delay (30 MS for 1 MHz)
II	3	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1
II	3	L = Sector Length Flag	LSB's Sector Length in ID Field: 00 / 01 / 10 / 11 L = 0: 256 / 512 / 1024 / 128 L = 1: 128 / 256 / 512 / 1024
II	4	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records
IV	0-3	I_x = Interrupt Condition Flags I_0 = 1 Not Ready To Ready Transition I_1 = 1 Ready To Not Ready Transition I_2 = 1 Index Pulse I_3 = 1 Immediate Interrupt, Requires A Reset* I_3-I_0 = 0 Terminate With No Interrupt (INTRQ)	

*NOTE: See Type IV Command Description for further information.

Write Precompensation

When operating in Double Density mode ($\overline{DDEN}$ = 0), the 279X has the capability of providing a user-defined precompensation value for Write Data. An external potentiometer (10K) tied to the WPW signal (Pin 33) allows a setting of 100 to 300 ns from nominal.

Setting the Write precomp value is accomplished by forcing the $\overline{TEST}$ line (Pin 22) to a Logic 0. A stream of pulses can then be seen on the Write Data (Pin 31) line. Adjust the WPW Potentiometer for the desired pulse width. This adjustment may be performed in-circuit since Write Gate (Pin 30) is inactive while $\overline{TEST}$ = 0.

Data Separation

The 279X can operate with either an external data separator or its own internal recovery circuits. The condition of the $\overline{TEST}$ line (Pin 22) in conjunction with $\overline{MR}$ (Pin 19) will select internal or external mode.

To program the 279X for external VCO, a $\overline{MR}$ pulse must be applied while $\overline{TEST}$ = 0. A clock equivalent to eight times the data rate (e.g., 4.0 MHz for 8" Double Density) is applied to the VCO input (Pin 26). The feedback reference voltage is available on the Pump output (Pin 23) for external integration to control the VCO. $\overline{TEST}$ is returned to a Logic 1 for normal operation. Note: To maintain this mode, $\overline{TEST}$ must be held low whenever $\overline{MR}$ is applied.

For internal VCO operation, the $\overline{TEST}$ line must be high during the $\overline{MR}$ pulse, then set to a Logic 0 for the adjustment procedure.

A 50K Potentiometer tied to the RPW input (Pin 18) is used to set the internal Read Data pulse for proper phasing. With a scope on Pin 29 (TG43), adjust the RPW pulse for 1/8 of the data rate (250 ns for 8" Double Density). An external variable capacitor of 5-60 pf is tied to the VCO input (Pin 26) for adjusting center frequency. With a frequency counter on Pin 16 (DIRC) adjust the trimmer cap to yield the appropriate Data Rate (500 KHz for 8" Double Density). The $\overline{DDEN}$ line must be low while the 5/8 line is held high or the adjustment times above will be doubled.

After adjustments have been made, the $\overline{TEST}$ pin is returned to a Logic 1 and the device is ready for operation. Adjustments may be made in-circuit since the DIRC and TG43 lines may toggle without affecting the drive.

The PUMP output (Pin 23) consists of positive and negative pulses, which their duration is equivalent to the phase difference of incoming Data vs. VCO frequency. This signal is internally connected to the VCO input, but a Filter is needed to connect these pulses to a slow moving DC voltage.

The internal phase-detector is unsymmetrical for a random distribution of data pulses by a factor of two, in favor of a PUMP UP condition. Therefore, it is desirable to have a PUMP DOWN twice as responsive to prevent run-away during a lock attempt.

A first order lag-lead filter can be used at the PUMP output (Pin 23). This filter controls the instantaneous response of the VCO to bit-shifted data (jitter) as well as the response to normal frequency shift, i.e., the lock-up time. A balance must be accomplished between the two conditions to inhibit over-responsiveness to jitter and to prevent an extremely wide lock-up response, leading to PUMP run-away. The filter affects these two reactions in mutually opposite directions.

The Source Impedance for a PUMP UP/DOWN condition is 600/120 ohms, respectively, therefore the change in bias voltage for each pump can be approximated:

$$dV = \frac{dt \, \Delta V}{RC}$$

dt = 250 ns. (set by RPW)
C = 0.1μf
$R = R_S + R$
ΔV = 2.6 V for PUMP UP
0.9V for PUMP DOWN

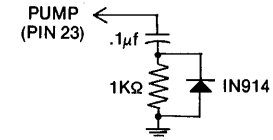
Lock
~~Lock~~-up response (T_L) is the transient time for the Loop to lock from center frequency (F_O) to maximum lock range:

$$T_L = 10\% \, F_L \times K_O \times \Delta P$$

Where:
K_O = VCO Conversion Gain = 3.7KHz/mV
F_L = Lock Range = 4.00 MHz
ΔP = Change in Bias for each Pump = 4 mV/PUMP

400 KHz x 3.7 KHz x 4 mV = 27 pumps
27 pumps = 54 μsec = 3.4 Byte times (8" Double Density)

The following Filter Circuit is recommended for 8" FM/MFM:



Since 5¼" Drives operate at exactly one-half the data rate (250 Kb/sec) the above capacitor should be doubled to .2 or .22μf.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-in, and Step-Out commands. Each of the Type I Commands contains a rate field (r_0 r_1), which determines the stepping motor rate as defined in Table 3.

A 2μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated.

The rates (shown in Table 3) can be applied to a Step-Direction Motor through the device interface.

TABLE 3. STEPPING RATES

CLK R1	CLK R0	2 MHz $\overline{TEST}$ = 1	1 MHz $\overline{TEST}$ = 1
0	0	3 ms	6 ms
0	1	6 ms	12 ms
1	0	10 ms	20 ms
1	1	15 ms	30 ms

After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for

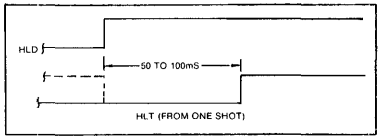
a 1 MHz clock. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

The WD279X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the 279X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load timing (HLT) is an input to the 279X which is used for the head engage time. When HLT = 1, the 279X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the 279X.



HEAD LOAD TIMING

When both HLD and HLT are true, the 279X will then read from or write to the media. The "and" of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the 279X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the 279X then waits for HLT to occur.

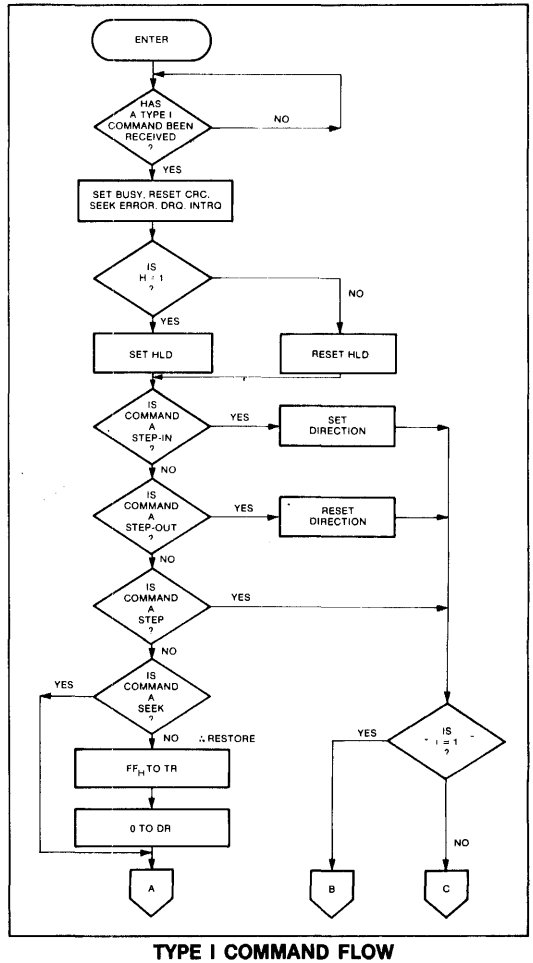
For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

RESTORE (SEEK TRACK 0)

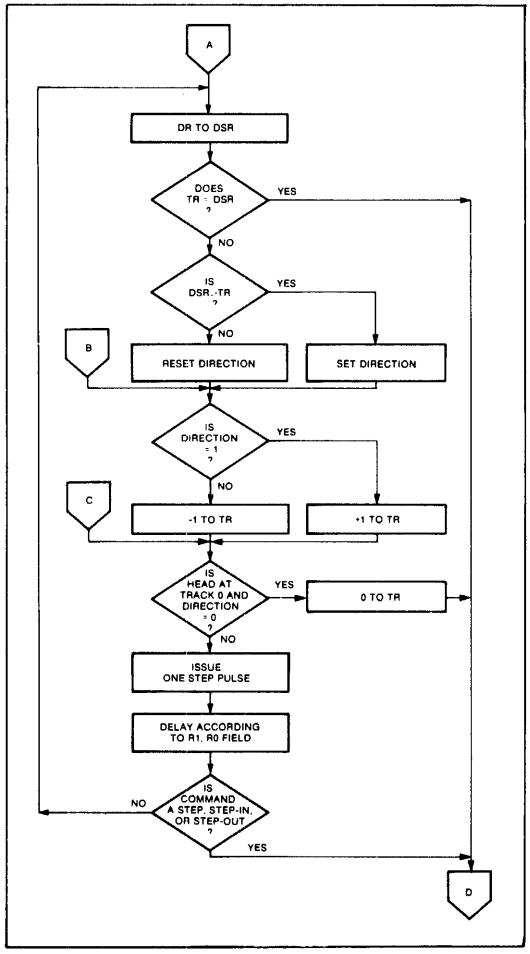
Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r_1r_0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the 279X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{MR}$ goes from an active to an inactive state.

SEEK

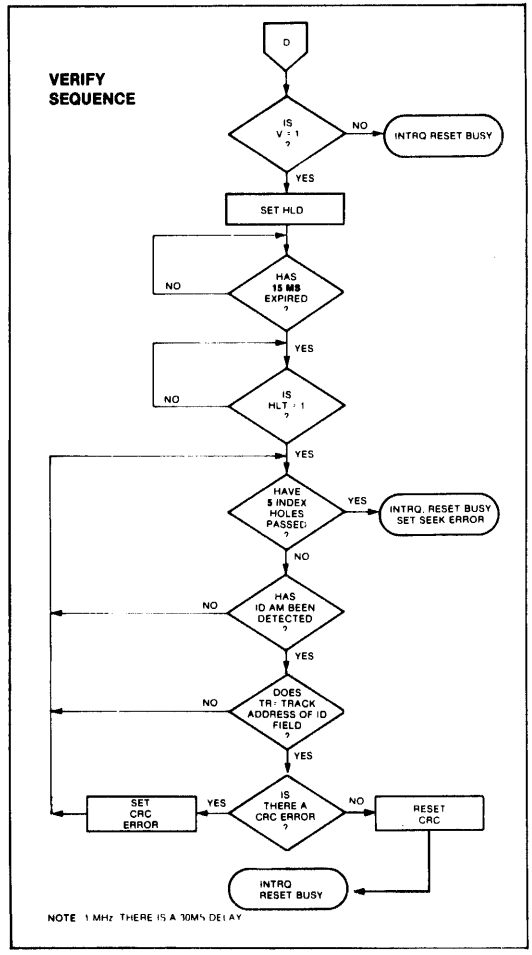
This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The WD279X will update the Track register and issue stepping pulses in the appropriate direction until the



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the 279X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the T flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the 279X issues one stepping pulse in the direction towards track 76. If the T flag is on, the Track Register is incremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the 279X issues one stepping pulse in the direction towards track 0. If the T flag is on, the Track Register is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

EXCEPTIONS

On the 2795/7 devices, the SSO output is not affected during Type I commands, and an internal side compare does not take place when the (V) Verify Flag is on.

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the

that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple sector command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The 279X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The 279X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one bye of FE in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ will set 8 to 12 μsec after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the lost data status and improper CRC Bytes.

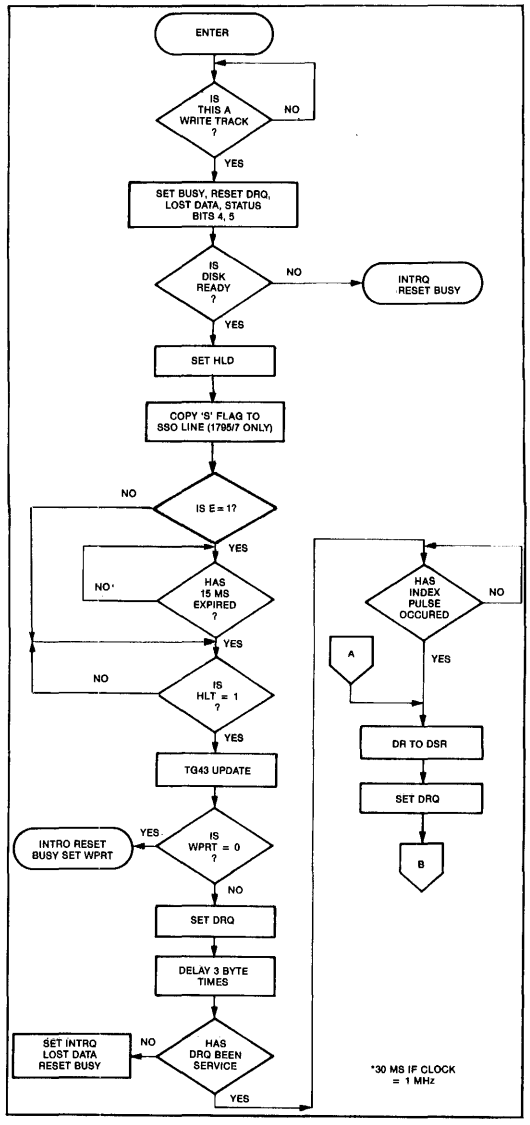
TYPES III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

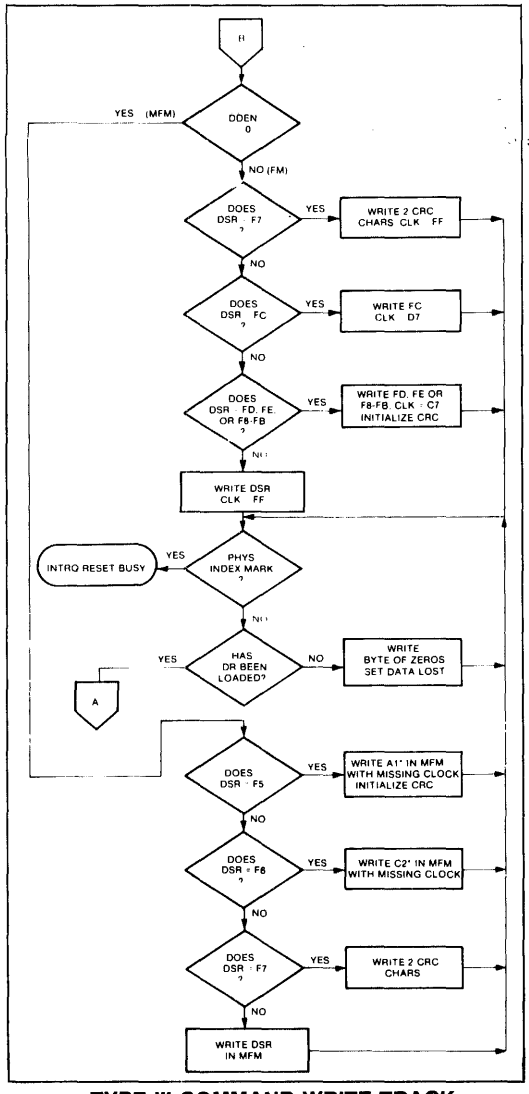
Although the CRC characters are transferred to the computer, the 279X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the host. At the end of the operation an interrupt is generated and the Busy Status is reset.



TYPE III COMMAND WRITE TRACK

READ TRACK

Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The ac-



TYPE III COMMAND WRITE TRACK

cumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule with the Lost Data status flag being set.

The ID A.M., ID field, ID CRC bytes, DAM, Data and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

WRITE TRACK FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the 279X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	WD279X INTERPRETATION IN FM ($\overline{DDEN}$ = 1)	WD279X INTERPRETATION IN MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

* Missing clock transition between bits 4 and 5

** Missing clock transition between bits 3 and 4

or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

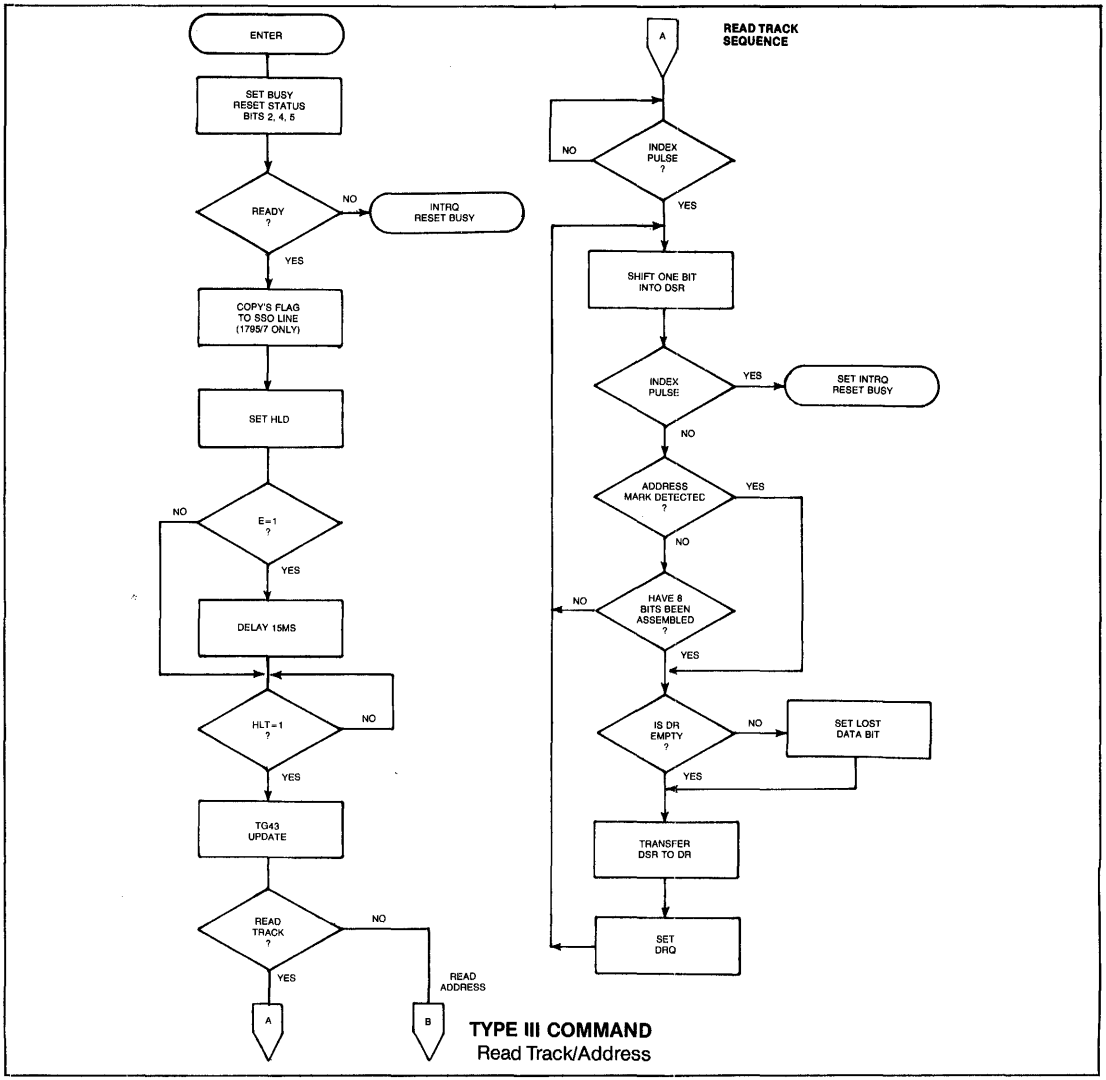
TYPE IV COMMANDS

The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to insure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

I_0 = Not-Ready to Ready Transition
I_1 = Ready to Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3 - I_0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I_3 - I_0 are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate



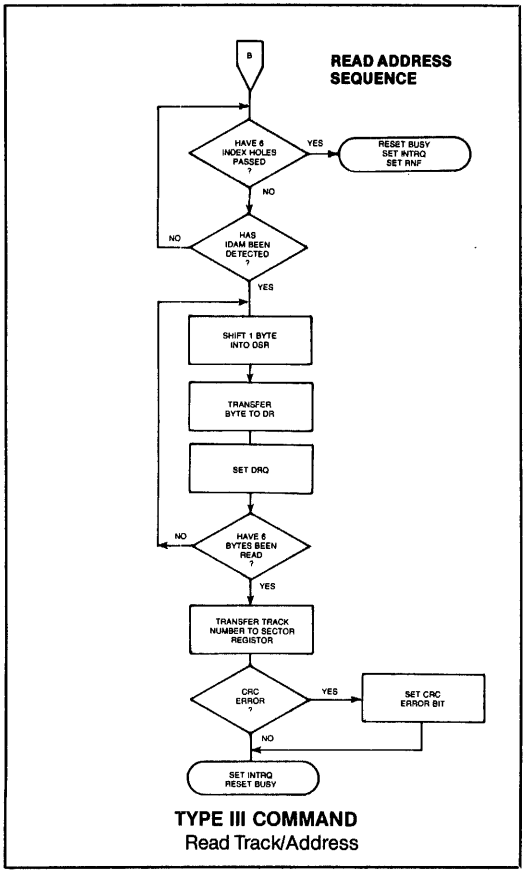
TYPE III COMMAND
Read Track/Address

interrupt condition (I_3 = 1), an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 8 micro sec (double density) or 16 micro sec (single density) before issuing a new command after issuing a forced interrupt (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.)

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I_1 = 1) and the Every Index Pulse (I_2 = 1) are both set, the resultant command would be HEX "DA." The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.



TYPE III COMMAND
Read Track/Address

STATUS REGISTER

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are: (times double when clock = 1 MHz)

Operation	Next Operation	Delay Req'd. FM	Delay Req'd. MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12μs	6μs
Write to Command Reg.	Read Status Bits 1-7	28μs	14μs
Write Any Register	Read From Diff. Register	0	0

IBM 3740 FORMAT — 128 BYTES/SECTOR

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)[3]
6	00
1	FC (Index Mark)
26	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00 (Sector Length)
1	F7 (2 CRC's written) —
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written) —
27	FF (or 00)
247[2]	FF (or 00)

1. Write bracketed field 26 times
2. Continue writing until 279X interrupts out. Approx. 247 bytes.
3. A '00' option is allowed on 2795/7 only.

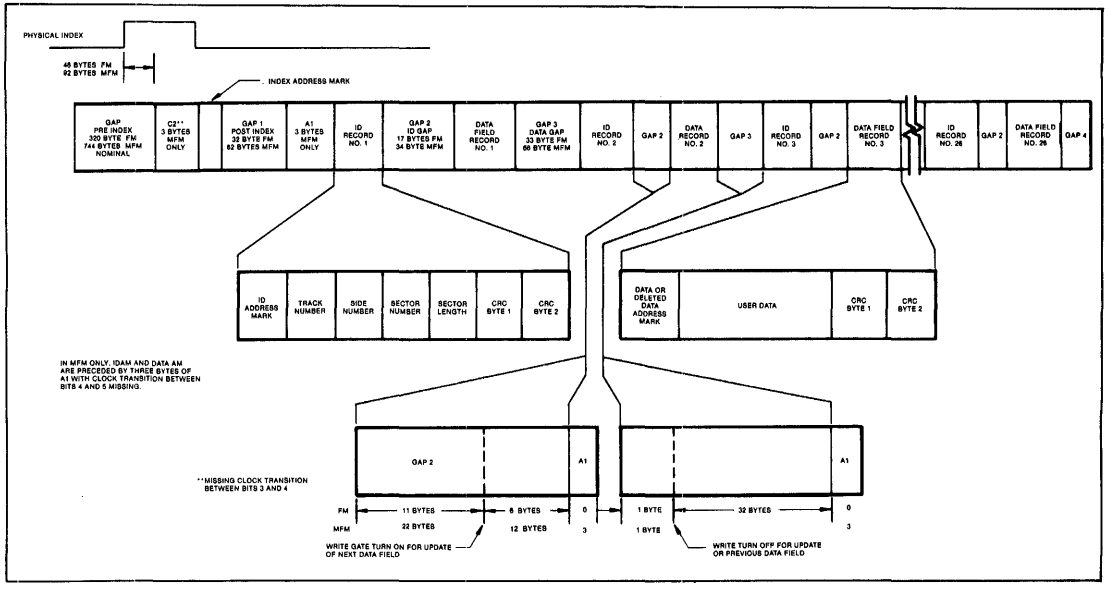
IBM SYSTEM 34 FORMAT- 256 BYTES/SECTOR

Shown below is the IBM dual-density format with 256 bytes/sector. In order for format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6 (Writes C2)
1	FC (Index Mark)
50*	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01 (Sector Length)
1	F7 (2 CRCs written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598**	4E

* Write bracketed field 26 times

** Continue writing until 279X interrupts out. Approx. 598 bytes.



IBM TRACK FORMAT

1. NON-IBM FORMATS

Variations in the IBM formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512 of 1024 bytes.
2) Gap 2 cannot be varied from the IBM format.
3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the 279X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for 279X operation, however PLL lock up time, motor speed variation, write splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

* Byte counts must be exact.
** Byte counts are minimum, except exactly 3 bytes of A1 must be written.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Voltage to any input with respect to V_{SS} = +15 to −0.3V

C_{IN} & C_{OUT} = 15 pF max with all pins grounded except one under test.
Operating temperature = 0°C to 70°C
Storage temperature = −55°C to +125°C

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

OPERATING CHARACTERISTICS (DC)

T_A = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5M ± .25V

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{IL}	Input Leakage			10	μA	$V_{IN} = V_{CC}$
I_{OL}	Output Leakage			10	μA	$V_{OUT} = V_{CC}$
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH}	Output High Voltage	2.4			V	I_O = −100μA
V_{OL}	Output Low Voltage			0.45	V	I_O = 1.6 mA
V_{OHP}	Output High PUMP	2.2			V	I_{OP} = −1.0 mA
V_{OLP}	Output Low PUMP			0.2	V	I_{OP} = +1.0 mA
P_D	Power Dissipation			.75	W	All Outputs Open
R_{PU}	Internal Pull-up*	100		1700	μA	V_{IN} = 0V
I_{CC}	Supply Current		70	150	mA	All Outputs Open

* Internal Pull-up resistors on PINS 1, 17, 22, 25, 37, and 40.

TIMING CHARACTERISTICS

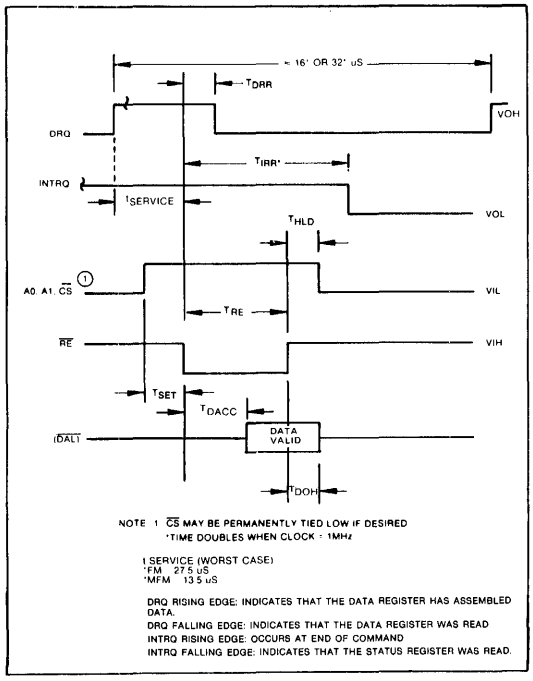
T_A = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ± .25V

READ ENABLE TIMING

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{SET}	Setup ADDR & CS to $\overline{RE}$	50			nsec	
T_{HLD}	Hold ADDR & CS from $\overline{RE}$	10			nsec	
T_{RE}	$\overline{RE}$ Pulse Width	200			nsec	C_L = 50 pf
T_{DRR}	DRQ Reset from $\overline{RE}$		100	200	nsec	
T_{IRR}	INTRQ Reset from $\overline{RE}$		500	3000	nsec	See Note
T_{DACC}	Data Valid from $\overline{RE}$		100	200	nsec	C_L = 50 pf
T_{DOH}	Data Hold From $\overline{RE}$	20		150	nsec	C_L = 50 pf

WRITE ENABLE TIMING

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{SET}	Setup ADDR & CS to $\overline{WE}$	50			nsec	
T_{HLD}	Hold ADDR & CS from $\overline{WE}$	10			nsec	
T_{WE}	$\overline{WE}$ Pulse Width	200			nsec	
T_{DRR}	DRQ Reset from $\overline{WE}$		100	200	nsec	
T_{IRR}	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note
T_{DS}	Data Setup to $\overline{WE}$	150			nsec	
T_{DH}	Data Hold from $\overline{WE}$	50			nsec	

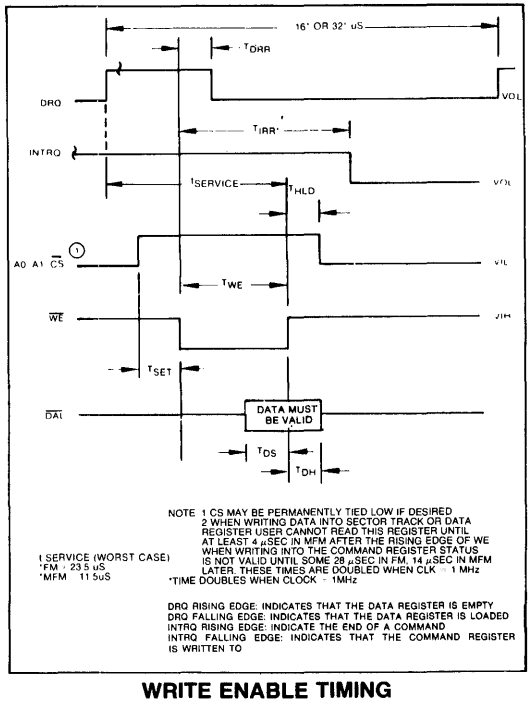


NOTE 1 $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED
*TIME DOUBLES WHEN CLOCK = 1MHz

t SERVICE (WORST CASE)
*FM 27.5 uS
*MFM 13.5 uS

DRQ RISING EDGE: INDICATES THAT THE DATA REGISTER HAS ASSEMBLED DATA.
DRQ FALLING EDGE: INDICATES THAT THE DATA REGISTER WAS READ
INTRQ RISING EDGE: OCCURS AT END OF COMMAND
INTRQ FALLING EDGE: INDICATES THAT THE STATUS REGISTER WAS READ.

READ ENABLE TIMING



NOTE 1 CS MAY BE PERMANENTLY TIED LOW IF DESIRED
2 WHEN WRITING DATA INTO SECTOR TRACK OR DATA REGISTER USER CANNOT READ THIS REGISTER UNTIL AT LEAST 4 μSEC IN MFM AFTER THE RISING EDGE OF WE WHEN WRITING INTO THE COMMAND REGISTER STATUS IS NOT VALID UNTIL SOME 28 μSEC IN FM, 14 μSEC IN MFM LATER. THESE TIMES ARE DOUBLED WHEN CLK = 1 MHz
*TIME DOUBLES WHEN CLOCK = 1MHz

t SERVICE (WORST CASE)
*FM 23.5 uS
*MFM 11.5uS

DRQ RISING EDGE: INDICATES THAT THE DATA REGISTER IS EMPTY
DRQ FALLING EDGE: INDICATES THAT THE DATA REGISTER IS LOADED
INTRQ RISING EDGE: INDICATE THE END OF A COMMAND
INTRQ FALLING EDGE: INDICATES THAT THE COMMAND REGISTER IS WRITTEN TO

WRITE ENABLE TIMING

INPUT DATA TIMING

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{PW}	$\overline{\text{Raw Read}}$ Pulse Width	100	200		nsec	
T_{BC}	$\overline{\text{Raw Read}}$ Cycle Time	1500	2000		nsec	

WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHz)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{WP}	Write Data Pulse Width	400	500	600	nsec	FM
		240		1000	nsec	MFM
T_{WG}	Write Gate to Write Data		2		μsec	FM
			1		μsec	MFM
T_{WF}	Write Gate off from WD		2		μsec	FM
			1		μsec	MFM

MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{CD_1}	Clock Duty (low)	230	250	20000	nsec	
T_{CD_2}	Clock Duty (high)	230	250	20000	nsec	
T_{STP}	Step Pulse Output	2 or 4			μsec	See Note
T_{DIR}	Dir Setup to Step		12		μsec	± CLK ERROR
T_{MR}	Master Reset Pulse Width	50			μsec	
T_{IP}	Index Pulse Width	10			μsec	See Note
RPW	Read Window Pulse Width					Input 0-5V
		120		700	nsec	MFM
		240		1400	nsec	FM ± 15%
WPW	Write Data Pulse Width					Input 0-5V
		300		1000	nsec	MFM
			500		nsec	FM
	Precomp Adjust.	100		250	nsec	MFM
RPW	Read Window Pulse Width					Input 0-5V
		120		700	nsec	MFM
		240		1400	nsec	FM ± 15%
WPW	Write Data Pulse Width					Input 0-5V
		300		1000	nsec	MFM
			500		nsec	FM
	Precomp Adjust.	100		250	nsec	MFM
VCO	Free Run Voltage Controlled	6.0			MHz	Ext. C = 0
	Oscillator. Adjustable by ext. capacitor on Pin 26		4.0		MHz	Ext. C = 35 pf
	Pump Up + 25%	5.0			MHz	PU = 2.2V Cext = 35 pf
VCO	Pump Down − 25%			3.0	MHz	$\overline{\text{PD}}$ = 0.2V Cext = 35 pf
	5% Change V_{CC}	3.8		4.2	MHz	Cext = 35 pf
VCO	T_A = 75°C	3.5			MHz	Cext = 35 pf
Cext	Necessary external capacitor	10	35	80	pf	VCO = 4.0MHz nom
RCLK	Derived read clock = VCO ÷ 8, 16, 32					VCO = 4.0MHz
			500		KHz	$\overline{\text{DDEN}}$ = 0 $\overline{5/8}$ = 1
			250		KHz	$\overline{\text{DDEN}}$ = 0 $\overline{5/8}$ = 0
			250		KHz	$\overline{\text{DDEN}}$ = 1 $\overline{5/8}$ = 1
			125		KHz	$\overline{\text{DDEN}}$ = 1 $\overline{5/8}$ = 0
PU/DON	PU/$\overline{\text{PD}}$ time on (pulse width)			250	ns	MFM
				500	ns	FM

WD1691 Floppy Support Logic (F.S.L.)

FEATURES

- DIRECT INTERFACE TO THE FD179X
- ELIMINATES EXTERNAL FDC LOGIC
- DATA SEPARATION/RCLK GENERATION
- WRITE PRECOMPENSATION SIGNALS
- VFOE/WF DEMULTIPLEXING
- PROGRAMMABLE DENSITY
- 8″ OR 5.25″ DRIVE COMPATIBLE
- ALL INPUTS AND OUTPUTS TTL COMPATIBLE
- SINGLE +5V SUPPLY

GENERAL DESCRIPTION

The WD1691 F.S.L. has been designed to minimize the external logic required to interface the 179X Family of Floppy Disk Controllers to a drive. With the use of an external VCO, the WD 1691 will generate the RCLK signal for the WD179X, while providing an adjustment pulse (PUMP) to control the VCO frequency. VFOE/WF de-multiplexing is also accomplished and Write Precompensation signals have been included to interface directly with the WD2143 Clock Generator.

The WD1691 is implemented in N-MOS silicon gate technology and is available in a plastic or ceramic 20 pin dual-in-line package.

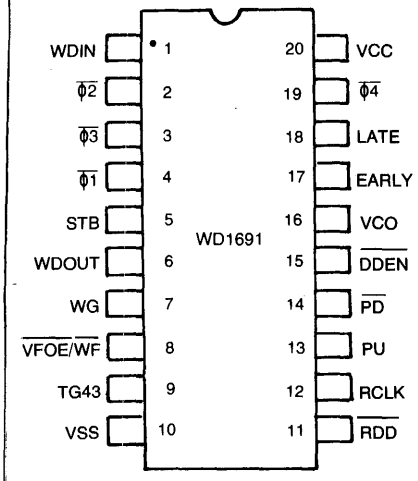


Figure 1 WD1691 PIN CONNECTIONS

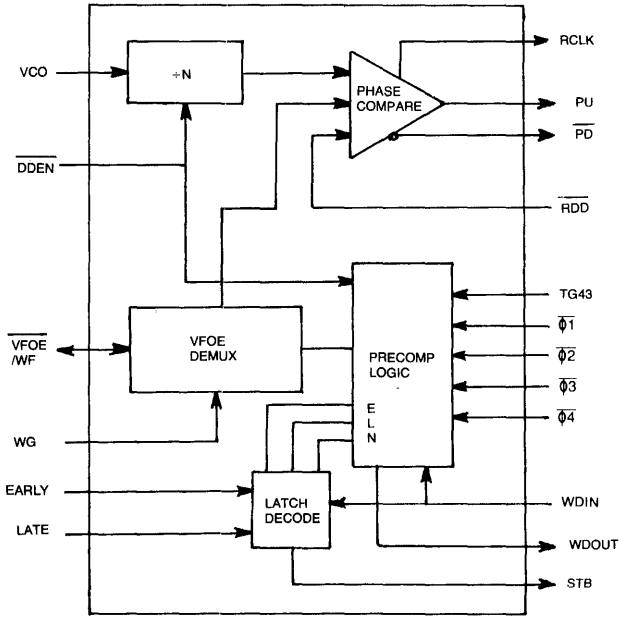


Figure 2 WD1691 BLOCK DIAGRAM

PIN	NAME	SYMBOL	FUNCTION
1	WRITE DATA INPUT	WDIN	Ties directly to the FD179X WD pin.
2, 3, 4, 19	PHASE 2, 3, 1, 4	$\overline{\Phi 2}$ $\overline{\Phi 3}$ $\overline{\Phi 1}$ $\overline{\Phi 4}$	4 Phase inputs to generate a desired Write Precompensation delay. These signals tie directly to the WD2143 Clock Generator.
5	STROBE	STB	Strobe output from the 1691. Strobe will latch at a high level on the leading edge of WDIN and reset to a low level on the leading edge of 04.
6	WRITE DATA OUTPUT	WDOUT	Serial, pre-compensated Write data stream to be sent to the disk drive's WD line.
7	WRITE GATE	WG	Ties directly to the FD179X WG pin.
8	VFO ENABLE/ WRITE FAULT	$\overline{\text{VFOE}}/\overline{\text{WF}}$	Ties directly to the FD179X $\overline{\text{VFOE}}/\overline{\text{WF}}$ pin.
9	TRACK 43	TG43	Ties directly to the FD179X TG43 pin, If Write Precompensation is required on TRACKS 44-76.
10	V_{SS}	V_{SS}	Ground
11	READ DATA	$\overline{\text{RDD}}$	Composite clock and data stream input from the drive.
12	READ CLOCK	RCLK	RCLK signal generated by the WD1691, to be tied to the FD179X RCLK pin.
13	PUMP UP	PU	Tri-state output that will be forced high when the WD1691 requires an increase in VCO frequency.
14	PUMP DOWN	$\overline{\text{PD}}$	Tri-state output that will be forced low when the WD1691 required a decrease in VCO frequency.
15	Double Density Enable	$\overline{\text{DDEN}}$	Double Density Select input. When Inactive (High), the VCO frequency is internally divided by two.
16	Voltage Controlled Oscillator	VCO	A nominal 4.0MHz (8" drive) or 2.0MHz (5.25" drive) master clock input.
17, 18	EARLY LATE	EARLY LATE	EARLY and LATE signals from the FD179X, used to determine Write Precompensation.
20	V_{CC}	V_{CC}	+ 5V ± 10% power supply

Table 1 PIN DEFINITIONS

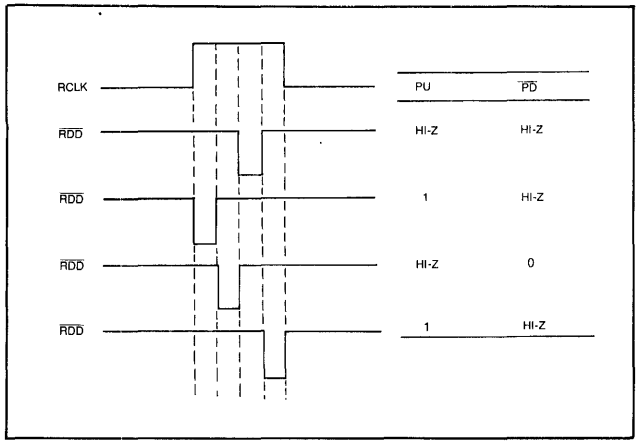


Figure 3 PUMP SIGNAL TIMING DIAGRAM

WG	VFOE/WF	RDD	PU+PD
1	X	X	HI-Z
0	1	X	HI-Z
0	0	1	HI-Z
0	0	0	Enable

Figure 4 DATA RECOVERY LOGIC

DEVICE DESCRIPTION

The WD1691 is divided into two sections:

1) Data Recovery Circuit
2) Write precompensation Circuit

The Data Separator or Recovery Circuit has four inputs: $\overline{DDEN}$, VCO, $\overline{RDD}$, and $\overline{VFOE/WF}$; and three outputs: PU, $\overline{PD}$ and RCLK. The $\overline{VFOE/WF}$ input is used in conjunction with the Write Gate signal to enable the Data recovery circuit. When Write Gate is high, a write operation is taking place, and the data recovery circuits are disabled, regardless of the state on any other inputs.

The Write Precompensation circuit has been designed to be used with the WD2143-03 clock generator. When the WD1691 is operated in a "single density only" mode, write precompensation as well as the WD2143-03 is not needed. In this case, $\overline{\phi 1}$, $\overline{\phi 2}$, $\overline{\phi 3}$, $\overline{\phi 4}$, and STB should be tied together, $\overline{DDEN}$ left open, and TG43, WDIN, Early, and Late tied to ground.

In the double-density mode ($\overline{DDEN}$=0), the signals Early and Late are used to select a phase input ($\overline{\phi 1}$ – $\overline{\phi 4}$) on the leading edge of WDIN. The STB line is latched high when this occurs, causing the WD2143-03 to start its pulse generation. $\overline{\phi 2}$ is used as the write data pulse on nominal (Early=Late=ϕ), $\overline{\phi 1}$ is used for early, and $\overline{\phi 3}$ is used for late. The leading edge of $\overline{\phi 4}$ resets the STB line in anticipation of the next write data pulse. When TG43=0 or $\overline{DDEN}$=1, Precompensation is disabled and any transitions on the WDIN line will appear on the WDout line. If write precompensation is desired on all tracks, leave TG43 open (an internal pull-up will force a Logic I) while $\overline{DDEN}$=0.

The signals, $\overline{DDEN}$, TG43, and $\overline{RDD}$ have internal pull-up resistors and may be left open if a logic I is desired on any of these lines.

When $\overline{VFOE/WF}$ and WRITE GATE are low, the data recovery circuit is enabled. When the $\overline{RDD}$ line goes Active Low, the PU or $\overline{PD}$ signals will become active. See Figure 4. If the $\overline{RDD}$ line has made its transition in the beginning of the RCLK window, PU will go from a HI-Z state to a Logic I, requesting an *increase* in VCO frequency. If the $\overline{RDD}$ line has made its transition at the end of the RCLK window, PU will remain in a HI-Z state while $\overline{PD}$ will go to a logic zero, requesting a *decrease* in VCO frequency. When the leading edge of $\overline{RDD}$ occurs in the center of the RCLK window, both PU and $\overline{PD}$ will remain tri-stated, indicating that no adjustment of the VCO frequency is needed. See Figure 3. The RCLK signal is a divide-by-16 ($\overline{DDEN}$=1) or a divide-by-8 ($\overline{DDEN}$=0) of the VCO frequency.

The minimum Voh level on PU is specified at 2.4V, sourcing 200ua. During PUMP UP time, this output will go from a tri-state to .4V minimum. By tying PU and $\overline{PD}$ together, a PUMP signal is created that will be forced low for a decrease in VCO frequency and forced high for an increase in VCO frequency. To speed up rise times and stabilize the output voltage, a resistor divider can be used to set the tristate level to approximately 1.4V. This yields a worst case swing of ± 1V; acceptable for most VCO chips with a linear voltage-to-frequency characteristic.

Both PU and $\overline{PD}$ signals are affected by the width of the RAW READ ($\overline{RDD}$) pulse. The wider the RAW READ pulse, the longer the PU or $\overline{PD}$ signal (depending upon the phase relationship to RCLK) will remain active. If the RAW READ pulse exceeds 250ns, (VCO = 4MHz, $\overline{DDEN}$ = 0) or 500ns. (VCO = 2MHz, $\overline{DDEN}$ = 1), then both a PU and $\overline{PD}$ will occur in the same window. This is undesirable and reduces the accuracy of the external integrator or low-pass filter to convert the PUMP signals into a slow moving D.C. correction voltage.

Eventually, the PUMP signals will have corrected the VCO input to exactly the same frequency multiple as the RAW READ signal. The leading edge of the RAW READ pulse will then occur in the exact center of the RCLK window, an ideal condition for the FD179X internal recovery circuits.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias ..... −25° to 70°C
Voltage on any pin with respect to Ground (vss) ..... −0.2 to +7V
Power Dissipation 1W
Storage Temp.—Ceramic—65°C to +150°C
Plastic—55°C to +125°C

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

DC ELECTRICAL CHARACTERISTICS

T_A = 0 to 70°C; V_{CC} = 5.0V ± 10%; V_{SS} = OV

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	−0.2		+0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			+0.45	V	I_{OL}=3.2MA
V_{OH}	High Level Output Voltage	2.4			V	I_{OH}= −200μa
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current		40	100	MA	All outputs open

NOTE: For AC and functional testing purposes, a Logic '0' is measured at 0.8V, and a Logic '1' at 2.0V.

AC ELECTRICAL CHARACTERISTICS

T_A = 0° to 70°C; V_{CC} = 5V ± 10%; V_{SS} = OV

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
FIN	VCO Input Frequency	.5	4	6	MHz	$\overline{DDEN}$=0
		.5	2	6	MHz	$\overline{DDEN}$=1
R_{pw}	$\overline{RDD}$ Pulse Width	100	200		ns.	
W_{el}	EARLY (LATE) to WDIN	100			ns.	
P_{on}	PUMP UP/DN Time	0		250	ns.	
W_{pi}	WDIN to WDOUT			80	ns.	$\overline{DDEN}$=1
I_{nr}	Internal Pull-up Resistor	4.0	6.5	10	KΩ	

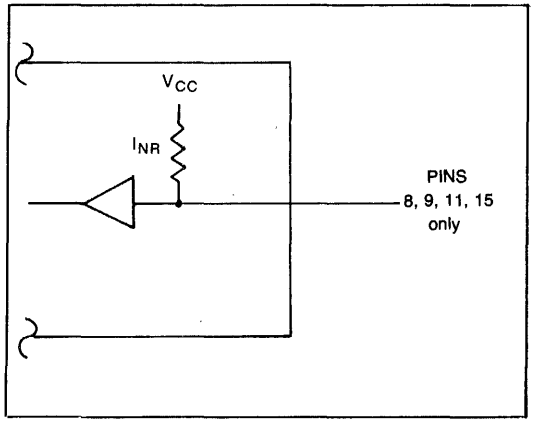


Figure 5 INTERNAL PULL-UP RESISTOR

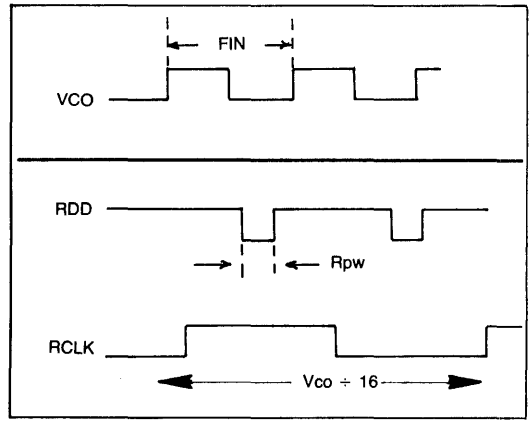


Figure 6 RDD AND RCLK PULSE DIAGRAMS

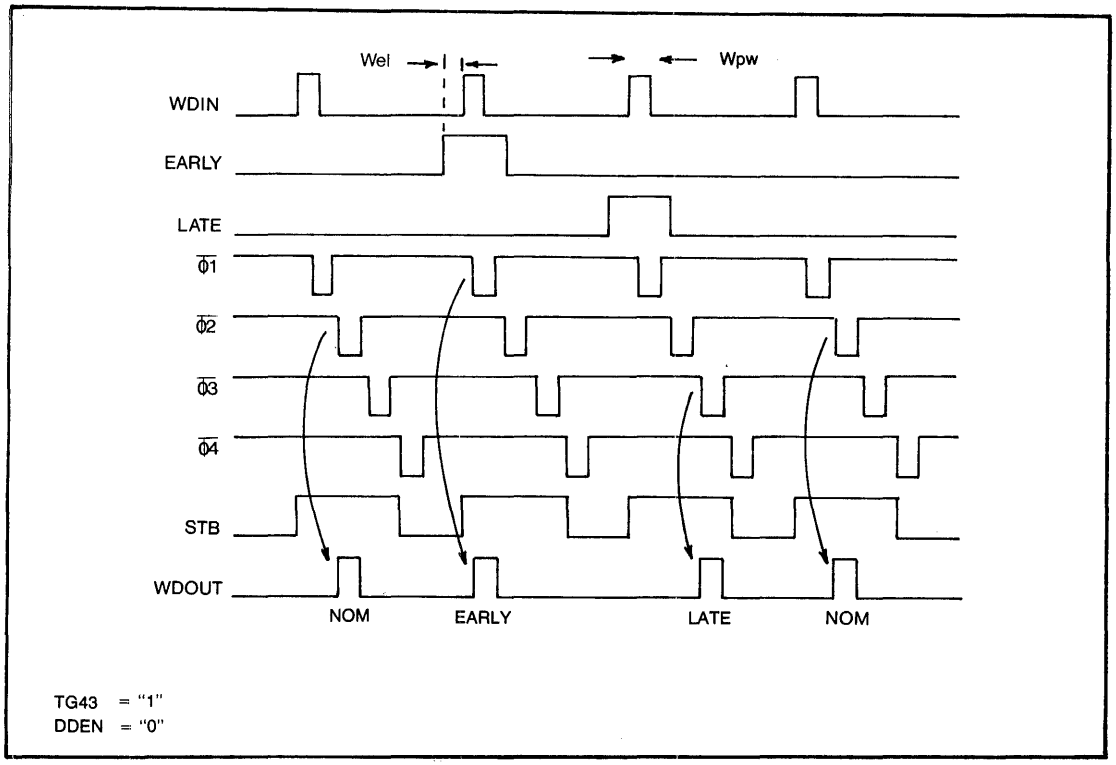


Figure 7 WRITE DATA TIMING (MFM)

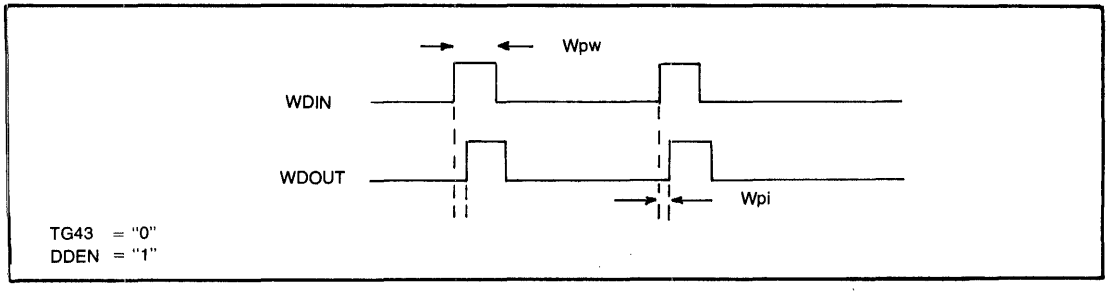


Figure 8 WRITE DATA TIMING (FM)

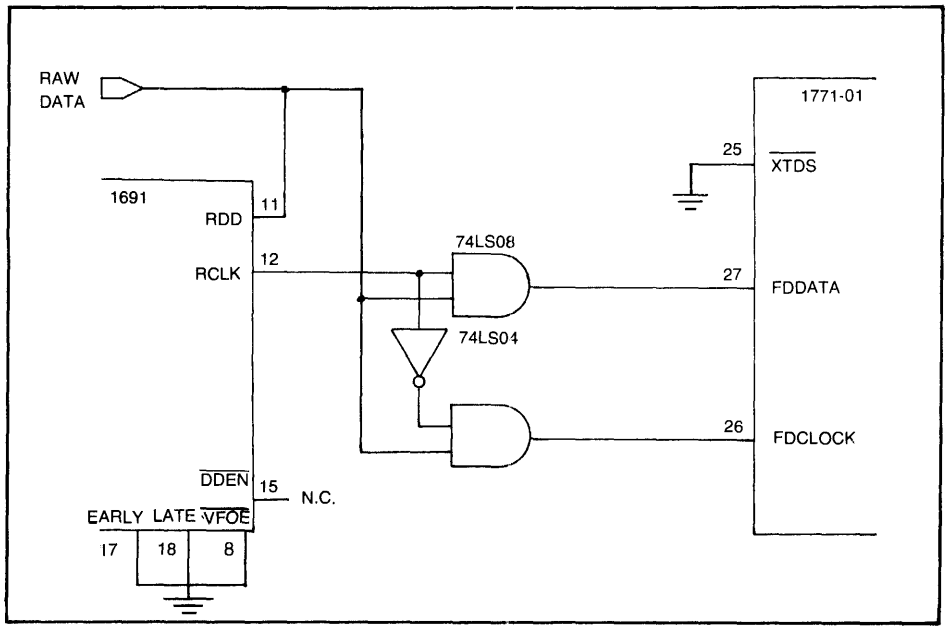


Figure 9 WD1691 to FD1771-01 INTERFACE

TYPICAL APPLICATIONS

Figure 9 illustrates the 1691 to FD1771-01 floppy disk controller. The RCLK signal is used to gate the RAW data pulses which are inverted by the 74LS04 inverter. Since RCLK will be high during data and low during clock a 74LS08 is used to switch the proper clock or data pulse to the FD1771.

Shown in Figure 10 is a Phase-Lock Loop data separator and the support logic for a single and double-density 8" drive. The raw data (Both clock and data bits) are fed to the WD1691 and FD179X. The WD1691 outputs its PU or $\overline{PD}$ signal, which is integrated by the .33uf capacitor and 33ohm resistor to form a control voltage for the 74S124 VCO device. The 4.0MHZ nominal output of the VCO then feeds back to the WD1691 completing the loop. The WD2143-03 is also used, providing write precompensation when in double-density, from tracks 44-77. The $\overline{DDEN}$ line can either be controlled by a toggle switch or a logic level from the host system.

ALIGNMENT

To adjust write precompensation, issue a command to the FD179X so that write data pulses are present. This can be done with a 'WRITE TRACK' command and the IP line open, or a continuous 'WRITE SECTOR' operation. With a scope on pin 4 of the WD1691, adjust the precomp pot for the desired value. This will range from 100 to 300 ns typically.

The pulse width set on pin 4 ($\overline{\emptyset 1}$) will be the desired precomp delay from nominal.

The data separator must be adjusted with the $\overline{RDD}$ or $\overline{VFOE}/\overline{WF}$ line at a Logic I. Adjust the bias voltage potentiometer for 1.4V on pin 2 of the 74S124. Then adjust the range control to yield 4.0MHZ on pin 7 of the 74S124.

SUBSTITUTING VCO's

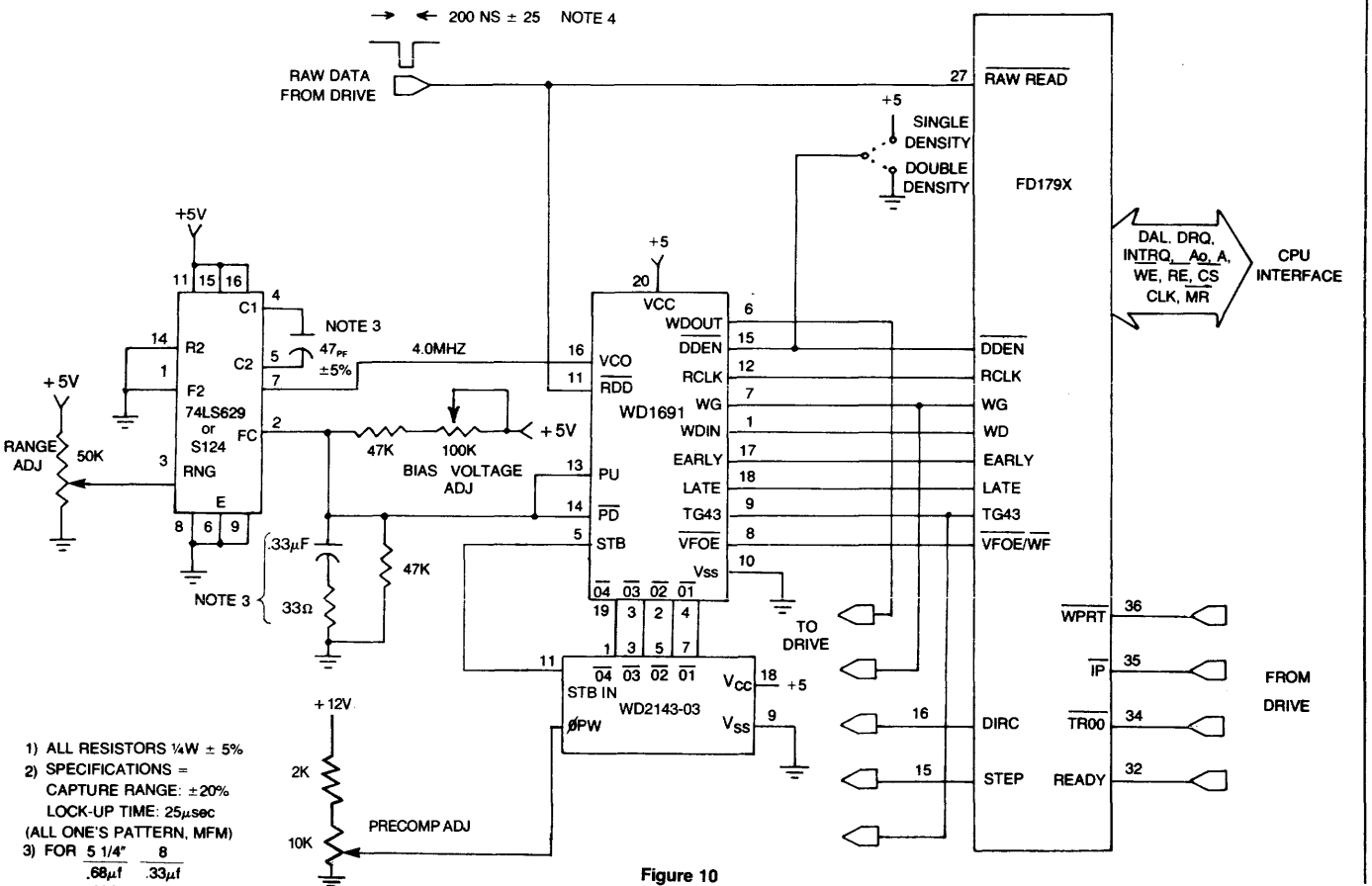
There are other VCO circuits available that may be substituted for the 74S124. The specifications required are:

1) The VCO must free run at 4.0MHz with a 1.4V control signal. The WD1691 will force this voltage 1 Volt in either direction (i.e., .4V = decrease frequency, 2.4V = increase frequency). If a ± 15% capture range is desired, then a 1 Volt change on the VCO input should change the frequency by 15%. Capture range should be limited to about ± 25%, to prevent the VCO from breaking into oscillation and/or losing lock because of noise spikes (causing abnormally quick adjustments of the VCO frequency). Jitter in the VCO output frequency may further be reduced by increasing the integration capacitor/resistor, but this will also decrease the final capture range and lock-up time.

2) The sink output current of the WD1691 is 3.2ma minimum. The source output current is −200ua. Therefore, source current is the limiting factor. Insure that the input circuitry of the VCO does not require source current in excess of −200ua.

Another alternative is to use a voltage follower/level shifter circuit to match the input requirements of the VCO chosen. A more complex filter can be used to convert the PUMP UP/PUMP DOWN pulses to the varying DC voltage signal required by the VCO, achieving an optimum condition between lock-up time and high frequency rejection.

See page 725 for ordering information.



1) ALL RESISTORS ¼W ± 5%
2) SPECIFICATIONS =
CAPTURE RANGE: ±20%
LOCK-UP TIME: 25µsec
(ALL ONE'S PATTERN, MFM)
3) FOR

5 1/4"	8
.68µf	.33µf
68Ω	33Ω
82Pf	47Pf

4) $\overline{RDD}$ = ONE EIGHTH RCLK WIDTH MAXIMUM
250ns for 4MHz
200ns for 2MHz

Figure 10
8" SINGLE/DOUBLE DENSITY FLOPPY INTERFACE

Printed in U.S.A.

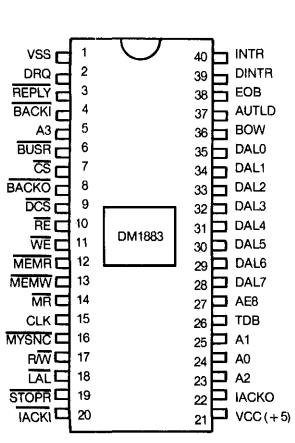
DM1883A/B Direct Memory Access Controller

FEATURES

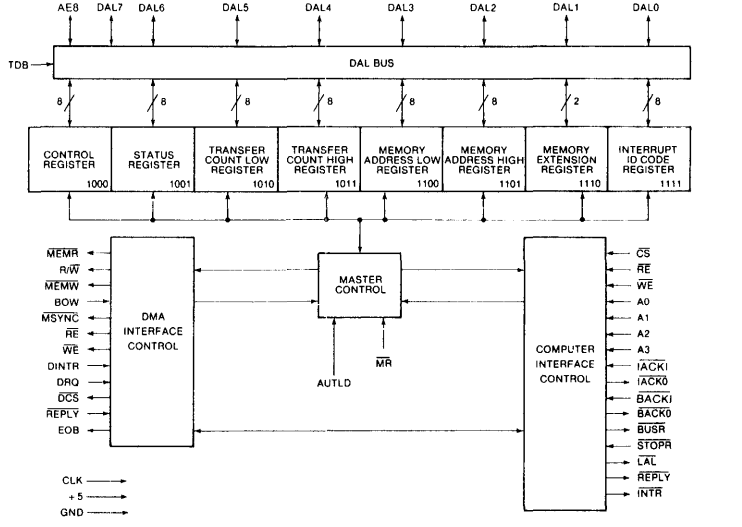
- AUTOMATIC DAISY CHAINING OF BUS AND INTERRUPT ACKNOWLEDGE SIGNALS
- AUTO LOAD OPTION
- SINGLE +5 VDC POWER SUPPLY
- 8 BIT BI-DIRECTIONAL DATA BUS
- TRUE OR COMPLEMENT DATA BUS
- 8 CPU ADDRESSABLE DMAC REGISTERS
- 8 CPU ADDRESSABLE DEVICE REGISTERS
- AUTOMATIC GENERATION OF DEVICE CS DURING DMA AND CPU DEVICE ACCESSES
- 256K MEMORY ADDRESSING
- 64K PROGRAMMABLE PAGE PROTECTION
- BYTE OR WORD DMA TRANSFERS
- INTERRUPT AND BUS REQUEST CAPABILITIES
- END-OF-BLOCK SHUT OFF BY DMAC
- TIME-OUT INTERRUPT CAPABILITY
- SINGLE CLOCK INPUT
- CS, RE, WE, A0-A3 ADDRESSING
- STOP REQUEST INPUT TO DELAY INTERRUPT OR BUS REQUESTS
- COMPATIBLE WITH OUR FLOPPY DISC CONTROLLERS
- 8 BIT PROGRAMMABLE INTERRUPT ID CODE

GENERAL DESCRIPTION

The DM1883 Direct Memory Access Controller (DMAC) is packaged in a 40 pin standard dual in-line package. The chip requires a single +5 power supply input and a single clock input. The device contains 8 CPU addressable registers, and allows for up to 8 CPU addressable device registers if the automatic device chip select feature is used. Byte or word transfers can be programmed, and all memory DMA operations are handshaked for compatibility with a variety of bus structures. Up to 256K bytes of memory can be accessed directly with 64K page protection and nonexistent memory interrupt as options. Bus and Interrupt Acknowledge signals are internally daisy chained, and a STOP REQUEST input prevents new requests while a current request is active. Device accesses are not handshaked, and a BUS HOLD feature is present for high speed devices. Device interrupt input, end-of-block output, and I/O read/write output pins simplify hardware interfacing to the device and the CPU bus. The AUTO LOAD feature allows automatic boot-loading of up to 64K bytes or words into memory starting at location zero. An 8 bit interrupt ID code is also provided.



PIN CONNECTIONS



DM1883 BLOCK DIAGRAM

INTERFACE SIGNALS DESCRIPTIONS

PIN NUMBER	SIGNAL NAME	SYMBOL	FUNCTION
1	GROUND	VSS	Ground
2	DATA REQUEST	DRQ	Data service request input from the peripheral device. A DMA transfer is initiated when this signal goes high.
3	$\overline{\text{REPLY}}$	$\overline{\text{REPLY}}$	Active low bi-directional handshake signal for both CPU and DMA transfers.
4	$\overline{\text{BACK IN}}$	$\overline{\text{BACKI}}$	Bus acknowledge in. An active low input signal from the CPU or a previous device in the $\overline{\text{BACK}}$ daisy chain. When low this signal will initiate a DMA transfer if the DMAC was requesting a DMA cycle.
5, 23, 24, 25	REGISTER SELECTS	A0-A3	These inputs select one of eight DMAC registers or one of eight device registers. When A3 is high the DMAC is selected. When A3 is low the DMAC is deselected and $\overline{\text{DCS}}$ is made low by the DMAC to activate device transfers. $\overline{\text{CS}}$ input to the DMAC must be made low before either the DMAC or the device may be selected by the CPU.
6	$\overline{\text{BUS REQUEST}}$	$\overline{\text{BUSR}}$	Active low output signal to initiate a CPU bus request and to latch A8-A15, A17 of the 18 bit DMA transfer address from DAL0-DAL7, AE8 into an external register.
7	$\overline{\text{CHIP SELECT}}$	$\overline{\text{CS}}$	Active low chip select input signal for CPU controlled operations.
8	$\overline{\text{BACK OUT}}$	$\overline{\text{BACKO}}$	Bus acknowledge out. An active low output signal used to pass $\overline{\text{BACKI}}$ along the daisy chain when the DMAC is not requesting a DMA cycle. This output is not affected by $\overline{\text{STOPR}}$.
9	$\overline{\text{DEVICE SELECT}}$	$\overline{\text{DCS}}$	Active low device chip select output signal for CPU and DMAC controlled operations.
10	$\overline{\text{READ ENABLE}}$	$\overline{\text{RE}}$	Active low bi-directional read enable for the DMAC and the device.
11	$\overline{\text{WRITE ENABLE}}$	$\overline{\text{WE}}$	Active low bi-directional write enable for the DMAC and the device. $\overline{\text{RE}}$ and $\overline{\text{WE}}$ are inputs during CPU controlled operations, and outputs to the device during DMAC controlled operations.
12	$\overline{\text{MEMORY READ}}$	$\overline{\text{MEMR}}$	Active low output to initiate a memory read during DMA transfers to the peripheral device.
13	$\overline{\text{MEMORY WRITE}}$	$\overline{\text{MEMW}}$	Active low output to initiate a memory write during DMA transfers from the peripheral device.
14	$\overline{\text{MASTER RESET}}$	$\overline{\text{MR}}$	Active low master reset signal to initialize the DMAC.
15	CLOCK	CLK	Clock input
16	$\overline{\text{MEMORY SYNC}}$	$\overline{\text{MSYNC}}$	Active low memory sync output to initiate a memory access during DMA transfers.
17	READ/$\overline{\text{WRITE}}$	R/$\overline{\text{W}}$	This output indicates the direction of transfer for the peripheral device. High for device-to-memory transfers (READ), and low for memory to device transfers (WRITE). Tied directly to Control Register bit 4.
18	$\overline{\text{LOAD ADDRESS LOW}}$	$\overline{\text{LAL}}$	Active low output signal to latch A0-A7, A16 of the 18-bit DMA transfer address from DAL0-DAL7, AE8 into an external register. $\overline{\text{BUSR}}$ and $\overline{\text{LAL}}$ are compatible with INTEL 8212 devices.

PIN NUMBER	SIGNAL NAME	SYMBOL	FUNCTION
19	$\overline{\text{STOP REQUEST}}$	$\overline{\text{STOPR}}$	Active low input that prevents $\overline{\text{INTR}}$ and $\overline{\text{BUSR}}$ from going low even if a request becomes active. An active $\overline{\text{INTR}}$ or $\overline{\text{BUSR}}$ request will not be affected by this input going low. This signal is used to speed up daisy chaining of bus and interrupt acknowledge inputs, and to prevent new requests while some other request is in the process of being serviced.
20	$\overline{\text{IACK IN}}$	$\overline{\text{IACKI}}$	Interrupt acknowledge in. An active low input signal from the CPU or a previous device in the $\overline{\text{IACK}}$ daisy chain. The DMAC is selected when $\overline{\text{INTR}}$ is low and this signal goes low. If $\overline{\text{RE}}$ also goes low while the DMAC is selected via this signal then the interrupt ID code is gated onto DAL0-DAL7.
21	POWER SUPPLY	V_{CC}	+5 VDC power supply input
22	$\overline{\text{IACK OUT}}$	$\overline{\text{IACKO}}$	Interrupt acknowledge out. An active low output signal used to pass $\overline{\text{IACKI}}$ along the daisy chain when the DMAC is not requesting an interrupt. This output is not affected by $\overline{\text{STOPR}}$.
26	TRUE DATA BUS	TDB	This input selects a true data bus on the DAL lines when high or open, and a complemented data bus on the DAL lines when low.
27	ADDRESS EXTENSION	AE8	Address extension bit output. Used during DMA operations to extend the address to 18 bits. This bit is true if TDB is high and complemented if TDB is low.
28-35	DATA ACCESS LINES	DAL0-DAL7	An 8-bit bi-directional three-state bus for CPU and DMAC controlled transfers to and from the DMAC. These signals remain in a three-state mode if the peripheral device is selected via A3 instead of the DMAC.
36	BYTE OR WORD	BOW	Byte or word DMA transfer mode input. When high memory addresses are incremented by one after every DMA transfer. When low memory addresses are incremented by two after every DMA transfer and the LSB of the memory address is forced to zero.
37	AUTO LOAD	AUTLD	Active high input to initiate a non-programmed 64K device to memory data transfer.
38	END OF BLOCK	EOB	Active high output to shut off the peripheral device when the transfer count goes to zero.
39	DEVICE INTERRUPT	DINTR	Interrupt service request input from the peripheral device. An interrupt request is generated by the DMAC if this input is high and the device interrupt enable bit in the command register is also set.
40	$\overline{\text{INTERRUPT REQUEST}}$	$\overline{\text{INTR}}$	Active low interrupt service request output. This output goes low if: 1) Any one of the three interrupt conditions is active, and 2) The $\overline{\text{STOPR}}$ input is high, and 3) The corresponding interrupt enable bit for the interrupting condition is set.

NOTE: The following pins float when not active low and require an external pull-up resistor of 10 KΩ (or greater) to +5 VDC:

$\overline{\text{INTR}}$, $\overline{\text{REPLY}}$, $\overline{\text{RE}}$, $\overline{\text{WE}}$, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{MSYNC}}$

The following pins have internal 10 KΩ pull-up resistors to +5 VDC:

TBD, DRQ, DINTR

WIRE-ORABLE SIGNALS

The following output signals can be wired together with a single common pull-up resistor if multiple DMAC chips exist on the same board:

$\overline{\text{MSYNC}}$, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{INTR}}$

REGISTER SELECTION

A 4-bit address input (A0, A1, A2, A3) is used to select one of 8 internal DMAC registers or to generate a device chip select ($\overline{\text{DCS}}$) output signal for selection of up to 8 peripheral device registers. The following table details the selection process.

INPUTS					OUTPUT	SELECTED REGISTER
$\overline{\text{CS}}$	A3	A2	A1	A0	$\overline{\text{DCS}}$	
L	L	X	X	X	L	One of 8 peripheral device registers
L	H	L	L	L	H	DMAC control register (0)
L	H	L	L	H	H	DMAC status register (1)
L	H	L	H	L	H	DMAC TC low register (2)
L	H	L	H	H	H	DMAC TC high register (3)
L	H	H	L	L	H	DMAC MA low register (4)
L	H	H	L	H	H	DMAC MA high register (5)
L	H	H	H	L	H	DMAC MA ext. register (6)
L	H	H	H	H	H	DMAC ID code register (7)

NOTE: L = Low voltage level, H = High voltage level, X = don't care.

TRANSFER COUNT REGISTER (TCR)

A 16-bit counter register that holds the two's complement of the transfer count (words or bytes) for DMA transfer operations. The low order 8 bits are in TC low, and the high order 8 bits are in TC high. The count is incremented by one after every DMA transfer. When the count reaches zero bit 3 of the Status Register is set to a one. If bit 3 in the Command Register is also a one then $\overline{\text{INTR}}$ will go low (providing $\overline{\text{STOPR}}$ is also high). TCR is set to a one on a MASTER RESET to allow a 64K transfer count during auto load.

MEMORY ADDRESS REGISTER (MAR)

An 18-bit counter register that occupies 3 DMA registers. Bits 0-7 are in MA low, bits 8-15 are in MA high, and bits 16-17 are in MA ext. The carry from bit 15 to 16 is enabled if and only if bit 6 of the Command Register is set to a one. If the BOW input pin is high then the MAR is incremented by one after every DMA transfer. If the BOW input pin is low then the MAR is incremented by two after every transfer and bit 0 is forced to a zero. This register is cleared to all zeros on a MASTER RESET.

During a DMA operation the DMA address is gated onto the DAL lines in two 9-bit bytes. The first byte out contains MAR 8-15 on DAL 0-7 and MAR 17 or AE8. The second byte out contains MAR 0-7 on DAL 0-7 and MAR 16 on AE8. The first byte is valid on the trailing edge of $\overline{\text{BUSR}}$, and the second byte is valid on the trailing edge of $\overline{\text{LAL}}$. Note that the address can easily be extended to 24 bits by decoding the address of the 2-bit extension register externally and gating the 6 unused bits into an external latch. This would give the system 16 Mbytes of addressing with either 65K or 256K bytes of paging.

REGISTER DEFINITIONS

DMAC CONTROL REGISTER (CR)

7	6	5	4	3	2	1	0
N/A	AECE	HBUS	IOM	TCIE	TOIE	DIE	RUN

BIT	SYMBOL	FUNCTION
0	RUN	Run/stop bit. A 1 places the DMAC in the run mode. A 0 terminates DMAC operation.
1	DIE	Device interrupt enable. A 1 allows a high input on DINTR to set the $\overline{\text{INTR}}$ output low.
2	TOIE	Time-out interrupt enable. A 1 allows the time-out one-shot to set the $\overline{\text{INTR}}$ output low. The time-out interrupt is set during a DMA transfer if $\overline{\text{REPLY}}$ does not go low within 5 usec of $\overline{\text{MSYNC}}$ going low.
3	TCIE	Transfer count zero interrupt enable. A 1 allows a zero in the transfer count register to set the $\overline{\text{INTR}}$ output low.
4	IOM	Input or output mode. A 1 sets READ mode (from the peripheral device to memory), and a 0 sets WRITE mode (from memory to the peripheral device). This bit also appears as an ungated output on the R/$\overline{\text{W}}$ pin.
5	HBUS	Hold bus. A 1 informs the DMAC to hold onto the bus for the entire block instead of releasing the bus after each byte or word transfer.

BIT	SYMBOL	FUNCTION
6	AECE	Address extension carry enable. A 1 allows a carry from DMA address bit 15 to propogate into bit 16.
7	N/A	Not used.

NOTE: Bits 1, 2, 3 set $\overline{\text{INTR}}$ low on an active condition if and only if the $\overline{\text{STOPR}}$ input is high.

DMAC STATUS REGISTER (SR)

7	6	5	4	3	2	1	0
BUSY	AECE	HBUS	IOM	TCZI	TOI	DINT	BOW

BIT	SYMBOL	FUNCTION
0	BOW	Byte or word data channel. A read only bit that indicates the status of the BOW input pin. A 1 bit indicates byte mode, and the DMA memory address is incremented by one after each DMA transfer. A 0 bit indicates word mode, and the DMA memory address is incremented by two (bit 0 is forced to a 0) after every DMA transfer.
1	DINT	If set a device interrupt has occurred. This is a read/write bit. Resetting this bit to a zero will reset $\overline{\text{INTR}}$.
2	TOI	If set a time-out interrupt has occurred. This is a read/write bit. Resetting this bit to a zero will reset $\overline{\text{INTR}}$.
3	TCZI	If set a transfer count equals zero interrupt has occurred. A read only bit. Sets EOB output when set.
4	IOM	Input-output mode. This bit reflects the status of bit 4 in the Command Register. A read only bit.
5	HBUS	Hold bus. This bit reflects the status of bit 5 in the Command Register. A read only bit.
6	AECE	Address extension carry enable. This bit reflects the status of bit 6 in the Command Register. A read only bit.
7	BUSY	Busy (data transfer not completed). A read only bit that reflects the status of bit 0 (RUN) in the Command Register.

NOTE: Bits 1, 2, 3 are set if the corresponding condition occurs. The enable bits in the CR affect only the $\overline{\text{INTR}}$ output, and not the Status Register.

ID CODE REGISTER (IDR)

An 8-bit programmable interrupt ID code register that gives the system an efficient way to establish a jump or vector address during a DMAC interrupt. The register is cleared to all zeros during a MASTER RESET, and must be loaded by the program during system initialization. If $\overline{\text{INTR}}$ is low, and IACKI and $\overline{\text{RE}}$ go low then the contents of this register are gated onto DAL 0-7. IACKI and $\overline{\text{CS}}$ must not be allowed to be low at the same time.

MASTER RESET

All register bits are reset to a zero during a MASTER RESET except the following which are set to ones: TCR bit 0, CR4, CR5, CR6, SR4, SR5, and SR6. This sets up the DMAC for a 64K transfer from the peripheral device to memory starting at address 0. The hold bus mode is also enabled. Execution of an Auto Load will begin DMA transfers under the above conditions.

AUTO LOAD

If the AUTLD input is made active after a MASTER RESET then bits CR3, CR1, and CR0 are also set. This places the DMAC in run mode, and enables two of the interrupt conditions. The DMAC will initiate data transfers, and will continue until either the transfer count reaches zero or a device interrupt occurs. Either event will terminate transfers and generate an interrupt.

WRITE PROTECT FEATURE

During CPU controlled transfers to the DMAC, if the RUN bit is set then any attempt to write into any of the Memory Address or Transfer Count registers will result in a NOP. $\overline{\text{REPLY}}$ will be made low in any case.

CPU CONTROLLED DATA TRANSFERS

During a CPU controlled transfer the CPU must have control of the system bus. When a CPU cycle is

initiated the system decodes the address on the bus. If the DMAC or its associated peripheral device is selected then $\overline{CS}$ to the DMAC is made low. The DMAC looks at the A3 input. If A3 is low the peripheral device is selected, and $\overline{DCS}$ is made low. The DMAC will not respond to an active $\overline{RE}$ or $\overline{WE}$ if A3 is low, and the DAL bus will stay in a high impedance state. This allows the DMAC DAL bus and the device DAL bus to be tied together if the device DAL bus is also in a high impedence state when the device is not selected.

If A3 is high when $\overline{CS}$ is low then the DMAC is selected and will respond to an active low $\overline{RE}$ or $\overline{WE}$. A0-A2 selects the DMAC as described under the REGISTER SELECTION section. If $\overline{RE}$ goes low the DMAC places the contents of the selected register on the DAL bus and activates $\overline{REPLY}$ to inform the CPU that valid data is on the bus. If $\overline{WE}$ goes low the DMAC gates the contents of the DAL bus into the selected register and activates $\overline{REPLY}$ to inform the CPU that data has been accepted.

If the peripheral device has more than 8 registers, or the device has fewer than 8 registers and there are one or more auxiliary registers external to the device, then it may be easier for the user to separate DMAC and device chip selects. In this mode $\overline{CS}$ to the DMAC is activated if and only if the DMAC is selected and A3 is tied to +5 VDC. The chip select to the device from a CPU controlled data transfer is ORed with $\overline{DCS}$ out of the DMAC. In this mode $\overline{DCS}$ will go low if and only if a DMA transfer is in effect and can be used by the controller as a "DMA ACTIVE" signal. Note that in any case actual data transfers to and from the CPU and the peripheral device are done by way of the device's DAL bus, not the DMAC's DAL bus.

DMAC CONTROLLED DATA TRANSFERS

When the DMAC is in RUN mode (CR0=1) it waits for a Data Request (DRQ) input from the peripheral device. When DRQ becomes active the DMAC requests the bus from the CPU by activating $\overline{BUSR}$. If $\overline{STOPR}$ was active when DRQ went active then the DMAC would wait until $\overline{STOPR}$ went high before activating $\overline{BUSR}$. When $\overline{BACKI}$ goes low in response to an active $\overline{BUSR}$ the request has been granted and the DMAC controls data transfers between the peripheral device and memory. The direction of the transfer is determined by the status of the READ/$\overline{WRITE}$ (R/$\overline{W}$) output pin. Note that R/$\overline{W}$ is tied directly to CR4.

1.) DEVICE-TO-MEMORY DMA TRANSFERS (CR4=1)

Once the DMAC has been granted the bus the following occurs:

A.) The DMAC places the high byte of the memory address on the DAL lines, activates $\overline{DCS}$, and then raises $\overline{BUSR}$. The trailing edge of $\overline{BUSR}$ can be used to latch the address into an external buffer.

B.) The DMAC places the low byte of the memory address on the DAL lines while activating $\overline{LAL}$, and then activates $\overline{MSYNC}$. The trailing edge of $\overline{LAL}$ can be used to latch the address into an external buffer

C.) The DAL lines are placed into a high impedence state in anticipation of a data transfer across the bus.

D.) The DMAC activates $\overline{RE}$ and then activates $\overline{MEMW}$.

E.) The DMAC waits for $\overline{REPLY}$ to go low. When $\overline{REPLY}$ is active the DMAC deactivates $\overline{MEMW}$ and then deactivates $\overline{RE}$.

F.) If the DMAC is *not* in hold bus mode (CR5=1) then the DMAC deactivates $\overline{DCS}$ and gives up control of the bus. If the DMAC is in hold bus mode then $\overline{DCS}$ remains low until after the completion of the final data transfer. Note that $\overline{BUSR}$ still cycles for every transfer.

G.) After the completion of every data transfer the memory address register is incremented by one in byte mode or two in word mode.

H.) After the completion of every data transfer the transfer count is incremented by one. Transfers are considered to be completed when the transfer count equals zero.

2.) MEMORY-TO-DEVICE DMA TRANSFERS (CR4=0)

Once the DMAC has been granted the bus it goes through the same steps as in the DEVICE-TO-MEMORY mode with the exception of steps "D" and "E" which are as follows:

D.) The DMAC activates $\overline{MEMR}$ and then activates $\overline{WE}$.

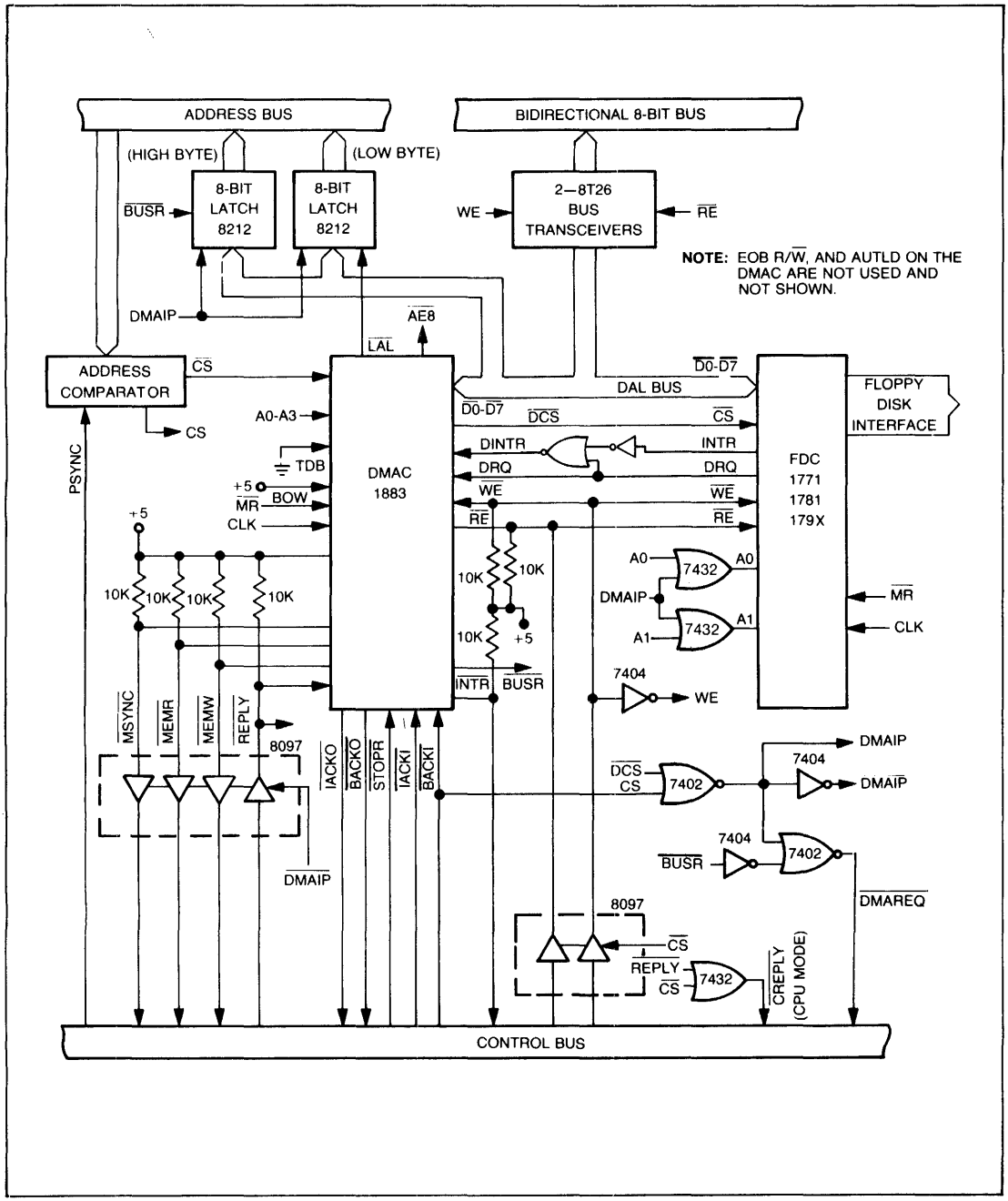
E.) The DMAC waits for $\overline{REPLY}$ to go low. When REPLY is active the DMAC deactivates $\overline{WE}$ and then deactivates $\overline{MEMR}$.

In either mode $\overline{BACKI}$ will be gated out to $\overline{BACKO}$ as soon as the DMAC deactivates $\overline{DCS}$. This allows other devices in the chain to gain access to the bus immediately.

INTERRUPTS

There are three individually enabled interrupt conditions. If any of the conditions occurs it will set its corresponding bit in the Status Register. If the

appropriate enable bit in the Command Register is set then $\overline{INTR}$ is also activated. Note that these are independent functions. When $\overline{INTR}$ is active then the DMAC can be selected by an active $\overline{IACKI}$ instead of an active $\overline{CS}$. $\overline{CS}$ and $\overline{IACKI}$ must not both be active at the same time.



TYPICAL DMAC TO FDC APPLICATION

Once an interrupt condition sets its corresponding bit in the status register the bit stays set until a CPU write to the status register occurs with a zero in the bit position.* If any one (or more) of the three interrupt condition bits in the Status Register is set then IACKI will not be gated out to IACKO even if the interrupt is *not* enabled.

NOTE: For a transfer-count-equals-zero interrupt condition to be cleared the Transfer Count Register must be loaded with a non-zero count.

The three interrupt conditions are as follows:

1.) DEVICE INTERRUPT (DINT)

A device interrupt condition occurs when the DINTR input is made high. This sets SR1 and, if CR1 is set, it activates INTR. The RUN bit is also reset thus terminating all subsequent DMA transfers. A device interrupt could be generated by a number of causes, and the program will have to test the device's Status Register to determine the cause of the interrupt. The DINT status bit in the DMAC Status Register must be cleared by the program as a part of the interrupt service routine.

2.) TRANSFER COUNT EQUALS ZERO INTERRUPT (TCZI)

When the TCR is incremented to zero after a DMA transfer the TCZI status bit (SR3) is set and the RUN bit (CR0) is reset. This terminates all DMA operations and, if CR3 is set, activates INTR. SR3 can be cleared only by loading a non-zero value into the TCR. The EOB output pin is high whenever SR3 is set.

3.) TIME-OUT INTERRUPT (TOI)

During any DMA transfer the leading edge of MSYNC triggers an internal time delay of approximately 5 microseconds. If the DMAC does not receive an active low REPLY input within that time delay then the DMA operation is terminated, the RUN bit is reset, and the TOI status bit (SR2) is set. If CR2 is set then INTR is activated. SR2 can only be cleared by writing a zero into that position of the Status Register.

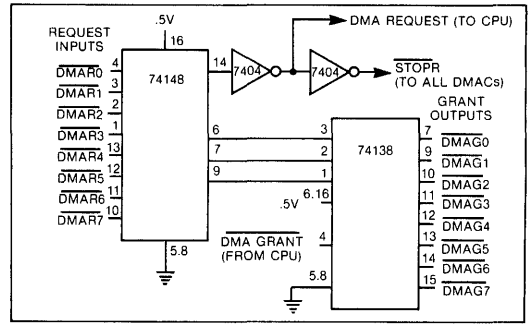
INTERRUPT OPERATION

When the DMAC activates INTR the CPU responds by activating IACKI. This signal can be daisy chained through all devices. The first device in the chain that has any bit in SR1-SR3 set will block the gating of IACKI out to IACKO. In addition, if INTR is active an IACKI will select the DMAC. An active RE after an IACKI select will gate the contents of the interrupt ID code register onto the DAL lines. The ID code stays active on the DAL lines as long as IACKI and RE are active. This code, which is cleared to zero by a MASTER RESET and loaded by the program during system initialization, can be used by the system to create a JUMP or VECTOR address for the device interrupt routine. Note that an active CS during a DMAC select via an active IACKI will cause unspecified results. Note also that no condition can activate INTR unless its corresponding enable bit is set and STOPR is high. If STOPR is active when the interrupt condition occurs then the DMAC will hold INTR inactive until STOPR goes inactive. At that time the DMAC will activate INTR automatically.

DMA PRIORITY SYSTEMS

Fixed Priority

A fixed priority can be established in two ways: through a parallel request-grant system or through a CPU controlled daisy chain system. A typical asynchronous parallel DMA priority system is shown. In this system any request generates an active STOPR, which is gated to all devices, and an active DMA request to the CPU. The CPU DMA grant generates a grant to the requesting device with the highest priority. If more than one request is received at the same time then the grants are honored from the highest to the lowest priority. In most cases, however, grants are not received simultaneously. The highest priority devices, therefore, will receive most of the immediate grants with the others being delayed by an active STOPR.



ASYNCHRONOUS PARALLEL DMA PRIORITY SYSTEM

Establishing a fixed priority system through a daisy chain approach requires the CPU monitor a "DMA IN PROGRESS" signal on the bus. This signal can be generated from DCS during a DMA transfer (i.e., DCS·CS). In this mode the CPU activates BACKI and STOPR in response to some bus request. STOPR is tied to all DMA controllers to prevent new bus requests while BACKI is propagating through all non-requesting DMAC devices. When the requesting DMAC gains control over the bus and activates DCS the CPU drops BACKI*. When DCS is deactivated the CPU deactivates STOPR to allow new requests. In this manner the device physically

closest to the CPU on the daisy chain has highest priority for all request cycles.

NOTE: $\overline{BACKI}$ and $\overline{STOPR}$ can be dropped at the same time with no effect on the priority scheme, but the CPU may have to capture new requests until $\overline{DCS}$ goes high.

Rotating Priority

This is a daisy chain approach that prevents one device from getting most of the bus grants if multiple devices are active at the same time. In this mode any device requesting the bus causes the CPU to activate $\overline{BACKI}$. This signal is tied to the $\overline{BACKI}$ and $\overline{STOPR}$ inputs of the first DMAC. The $\overline{BACKO}$ output of the first DMAC goes to the $\overline{BACKI}$ and $\overline{STOPR}$ inputs of the second DMAC, and so on. The $\overline{BACKO}$ output of the last DMAC in the chain goes back to the CPU to reset its $\overline{BACKI}$ output. In this mode the first device cannot request again until all other requesting devices in the chain have also been serviced.

In any case, if the CPU has to have the DMA request held active throughout the DMA cycle then the user will have to create this signal on the controller thusly: DMAREQ = BUSR + (DCS·$\overline{CS}$). If the device and DMAC chip selects are generated on the controller separately then the $\overline{CS}$ can be eliminated from the equation. It is needed only to distinguish a CPU chip select from a DMA cycle chip select. Note that in either case the second term in the equation is equivalent to "DMA CYCLE IN PROGRESS" (DMAIP).

SPECIFICATIONS

Absolute Maximum Ratings

Ambient Temperature Under Bias...0°C to +70°C
Voltage on Any Pin with Respect to Ground ..... -0.5V to +7V
Power Dissipation ..... 0.6 Watt

NOTE: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

DC Electrical Characteristics

T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%; GND =0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.4		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -100 µA
I_{DL}	Data Bus Leakage			-50	µA	V_{IN} = 0.45V
				10	µA	V_{IN} = V_{CC}
I_{IL}	Input Leakage			10	µA	V_{IN} = V_{CC}
I_{CC}	Power Supply Current		45	90	mA	

NOTE: VOL ≤0.4V when interfacing with low power Schottky parts (I_{OL} <1 mA).

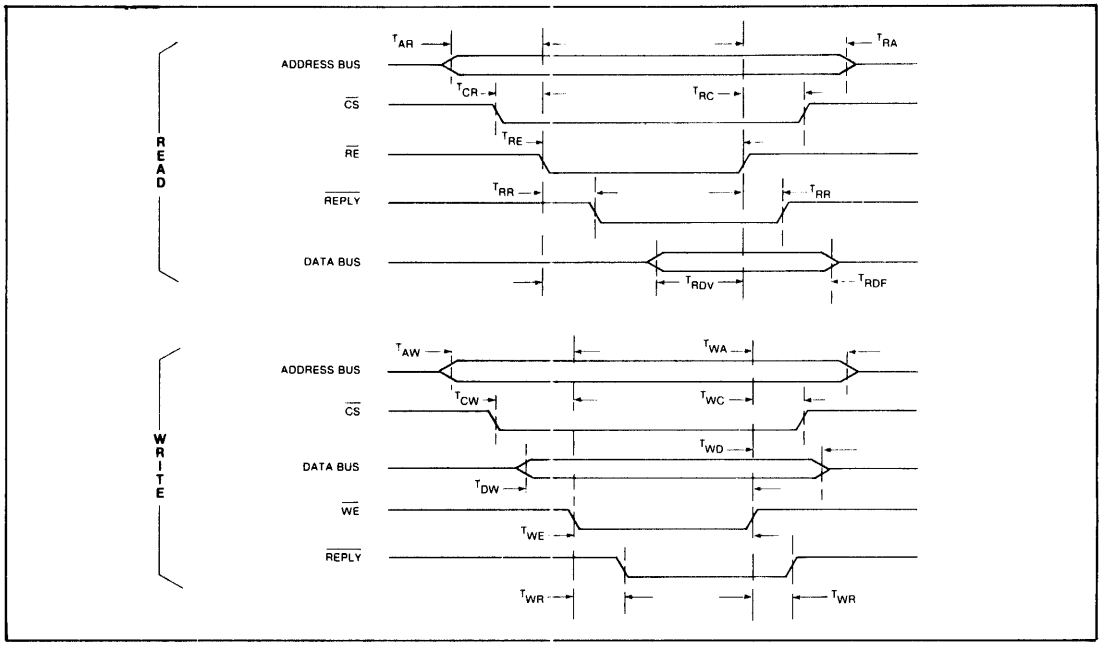
Capacitance

T_A = 25°C; V_{CC} = GND = 0V

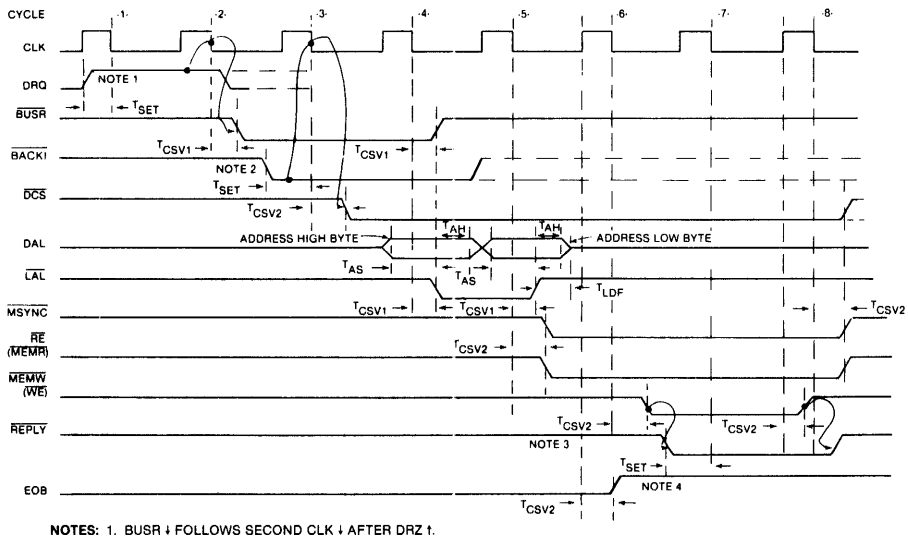
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	f_C = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND.

System Clock (CLK) Characteristics

Maximum Frequency = 2.0 MHz
Minimum Pulse Width = 250 ns
Maximum Pulse Width = 50% of duty cycle



CPU CONTROLLED TRANSFER



NOTES: 1. BUSR ↓ FOLLOWS SECOND CLK ↓ AFTER DRQ ↑.

2. a. CYCLE 2 IS SKIPPED FOR ALL SUBSEQUENT TRANSFERS WHEN IN THE HOLD MODE, I.E., DCS REMAINS LOW FOR ENTIRE BLOCK OF TRANSFERS.
   b. FOLLOWING BUSR ↓ WITH DCS HIGH (I.E., REQUESTING BUS CONTROL), THE DMA WILL ADD WAIT CYCLES BETWEEN CYCLES 2 AND 3 UNTIL BACK1 ↓ IS RECEIVED.

3. CYCLE 7 WILL BE REPEATED FOR EACH ADDITIONAL PERIOD THAT REPLY ↓ IS DELAYED TO THE DMA. CYCLE 7 WILL BE SKIPPED (I.E., MEMW (WE) PULSE WIDTH = 1/2 CLK PERIOD) IF REPLY IS MADE LOW PRIOR TO CLK ↓ OF CYCLE 6 (E.G., REPLY TIED TO GND DURING DMA TRANSFER).

4. EOB IS ACTIVATED ONLY FOR THE TRANSFER WHERE TCR INCREMENTS FROM 11 . . . 1 TO 00 . . . 0 (I.E., END OF BLOCK).

5. TO INSURE PROPER LOADING OF DAL BUS CONTENTS INTO THE CONTROLLER REGISTERS, THE WE PULSE WIDTH MUST BE GREATER THAN OR EQUAL TO ONE CLK PERIOD. THIS REQUIREMENT CAN ALSO BE SOLVED OFF CHIP BY TRIGGERING WE ↑ (TRAILING EDGE) WITH CLK ↓.

DMA CONTROLLED TRANSFER TIMING

AC Electrical Characteristics

T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%; GND = 0V

SYMBOL	DESCRIPTION	MIN	MAX.	UNIT	COND
CPU CONTROLLED TRANSFER TIMING - READ					
T_{AR}	Address Valid to $\overline{RE}$ ↓	80		ns	
T_{CR}	$\overline{CS}$ ↓ to $\overline{RE}$ ↓	0		ns	
T_{RE}	$\overline{RE}$ Pulse Width	300		ns	
T_{RDV}	$\overline{RE}$ ↓ to Data Valid		375	ns	CL = 50 pF
T_{RR}	$\overline{RE}$ ↓ (↓) to $\overline{REPLY}$ ↓ (↓)	50	350	ns	CL = 50 pF
T_{RA}	Address Hold from $\overline{RE}$ ↑	30		ns	
T_{RC}	$\overline{CS}$ Hold from $\overline{RE}$ ↑	0		ns	
T_{RDF}	Data Float from $\overline{RE}$ ↑		200	ns	
CPU CONTROLLED TRANSFER TIMING - WRITE					
T_{AW}	Address Valid to $\overline{WE}$ ↓	80		ns	
T_{CW}	$\overline{CS}$ ↓ to $\overline{WE}$ ↓	0		ns	
T_{DW}	Data Valid to $\overline{WE}$ ↑	300		ns	CL = 50 pF
T_{WE}	$\overline{WE}$ Pulse Width	300		ns	
T_{WR}	$\overline{WE}$ ↓ (↓) to $\overline{REPLY}$ ↓ (↓)	50	350	ns	CL = 50 pF
T_{WA}	Address Hold from $\overline{WE}$ ↑	30		ns	
T_{WC}	$\overline{CS}$ Hold from $\overline{WE}$ ↑	0		ns	
T_{WD}	Data Hold from $\overline{WE}$ ↑	30		ns	

SYMBOL	DESCRIPTION	MIN	TYP	MAX.	UNIT	COND
DMA CONTROLLED TRANSFER TIMING						
T_{CSV1}	Indicated CLK Edge to Indicate Signal Valid		150	250	ns	CL = 50 pF
T_{CSV2}	Indicated CLK Edge to Indicated Signal Valid		250	400	ns	CL = 50 pF
T_{AS}	DAL Set Up to $\overline{BUSR}$ ↑ or $\overline{LAL}$ ↓ (↓)	80			ns	CL = 50 pF
T_{AH}	DAL Hold from $\overline{BUSR}$ ↑ or $\overline{LAL}$ ↓ (↓)	50			ns	CL = 50 pF
T_{LDF}	$\overline{LAL}$ ↑ to DAL Float			250	ns	CL = 50 pF
T_{SET}	Indicated Signal Setup to Indicated CLK Edge	80			ns	
MISCELLANEOUS TIMING (τ = 1 CLOCK PERIOD)						
$\overline{CS}$ ↓ (↓) To $\overline{DCS}$ ↓ (↓) Propogation Delay (for A3 low)			150	250	ns	CL = 50 pF
$\overline{IACKI}$ ↓ (↓) to $\overline{IACKO}$ ↓ (↓) Propogation Delay when Not Requesting Interrupt			150	250	ns	CL = 50 pF
$\overline{BACKI}$ ↓ (↓) to $\overline{BACKO}$ ↓ (↓) Propogation Delay when Not Requesting Bus			150	250	ns	CL = 50 pF
$\overline{MR}$ Pulse Width	2τ					
DINTR, AUTLD, DRQ, $\overline{REPLY}$ Pulse Width	1τ					
BOW ↓ (↓) or TDB ↓ (↓) Set Up	500			ns		
Waiting $\overline{INTR}$ ↓ or $\overline{BUSR}$ ↓ from $\overline{STOPR}$ ↑				1τ +400	ns	CL = 50 pF
$\overline{INTR}$ ↓ from DINTR ↑				1.5τ +400	ns	CL = 50 pF

NOTE: A 1 TTL load is assumed on all output signals

See page 725 for ordering information.

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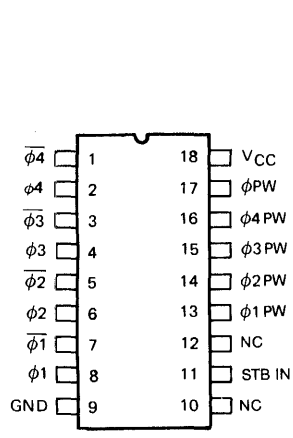
WD2143-03 Four Phase Clock Generator

FEATURES

- IMPROVED VERSION OF WD2143-01
- TRUE AND INVERTED OUTPUTS
- SINGLE 5 VOLT SUPPLY
- TTL COMPATABLE
- ON CHIP OSCILLATOR
- TTL CLOCK INPUT
- TTL CLOCK OUTPUTS
- PROGRAMMABLE PULSE WIDTHS
- PROGRAMMABLE PHASE WIDTHS
- NO EXTERNAL CAPACITOR

GENERAL DESCRIPTION

The WD2143-03 Four-Phase Clock Generator is a MOS/LSI device capable of generating four phase clocks. The output pulse widths are controlled by tying an external resistor to the proper control inputs. All pulse widths may be set to the same width by tying the ϕPW line through an external resistor. Each pulse width can also be individually programmed by tying a resistor through the appropriate ϕ1PW—ϕ4PW control inputs.



PIN CONNECTIONS

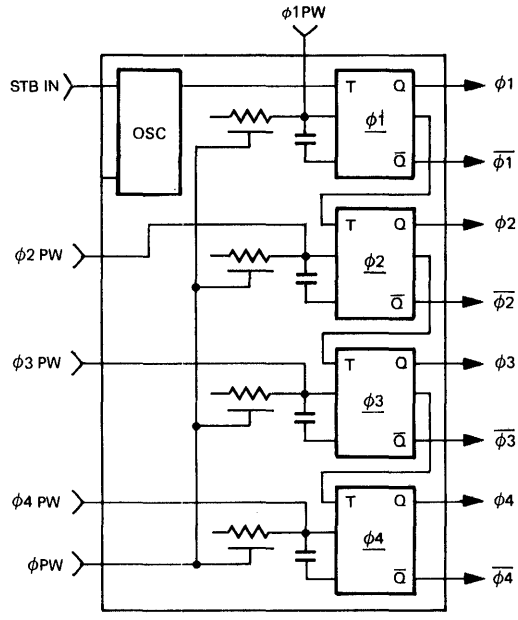


Figure 1 WD2143-03 PIN CONNECTIONS AND BLOCK DIAGRAM

DEVICE OPERATION

Each of the phase outputs can be controlled individually by typing an external resistor from ϕ1PW-ϕ4PW to a +5V supply. When it is desired to have ϕ1 through ϕ4 outputs the same width, the ϕ1PW-ϕ4PW inputs should be left open and an external resistor tied from the ϕPW (Pin 17) input to +12V.

STROBE IN (pin 11) is driven by a TTL square wave. Each of the four phase outputs provide both true and inverted signals, capable of driving 1 TTL load each.

PIN NUMBER	SYMBOL	DESCRIPTION
1, 3, 5, 7	$\overline{\phi 1}$—$\overline{\phi 4}$	Four phase clock outputs. These outputs are inverted (active low).
2, 4, 6, 8	ϕ1-ϕ4	Four Phase clock outputs. These outputs are true (active high).
9	GND	Ground
10	NC	No connection
11	STB IN	Input signal to initiate four-phase clock outputs.
12	NC	No connection
13-16	ϕ1PW-ϕ4PW	External resistor inputs to control the individual pulse widths of each output. These pins can be left open if ϕPW is used.
17	ϕPW	External resistor input to control all phase outputs to the same pulse widths.
18	V_{cc}	+5V ± 5% power supply input

Table 1 PIN DESCRIPTIONS

TYPICAL APPLICATIONS

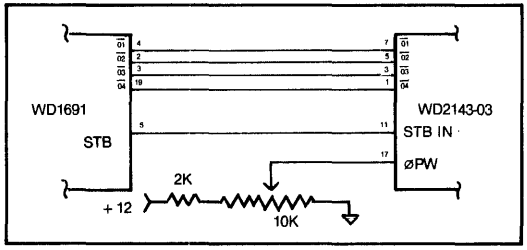


Figure 2 WRITE PRECOMP OPERATION WITH F.S.L. WD1691

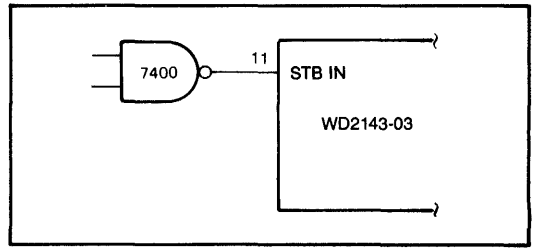


Figure 3 TTL SQUARE WAVE OPERATION

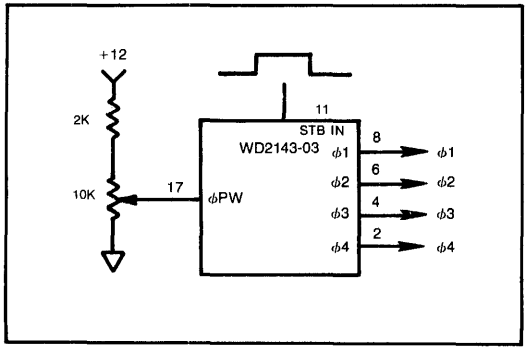


Figure 4 EQUAL PULSE WIDTH OUTPUTS

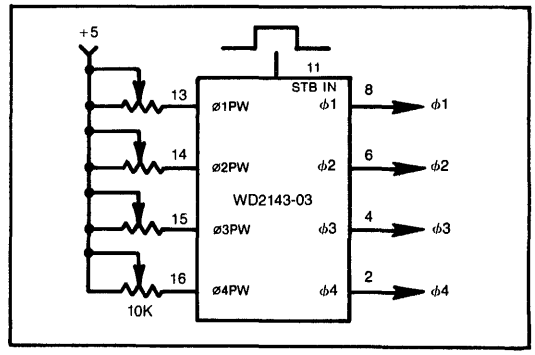


Figure 5 INDIVIDUAL PULSE WIDTH OUTPUTS

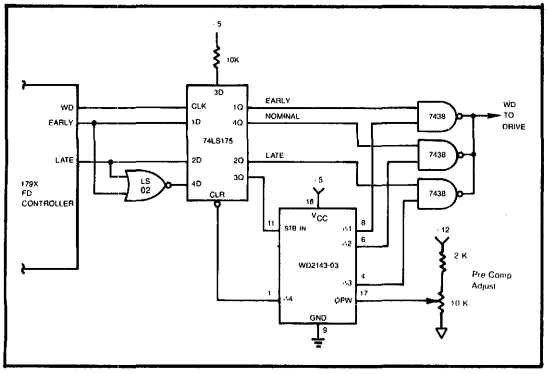


Figure 6 WRITE PRECOMP FOR FLOPPY DISK

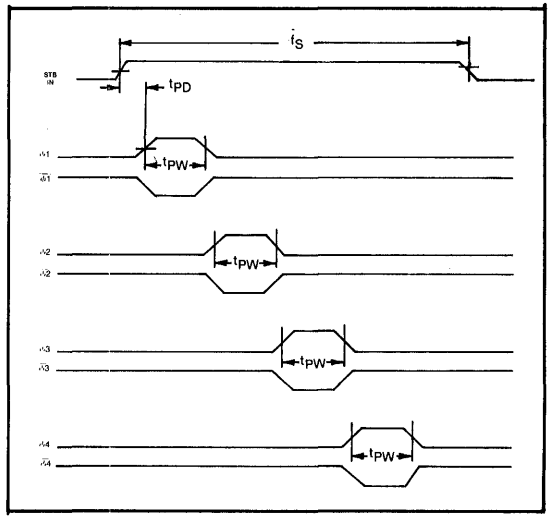


Figure 7 WD2143-03 TIMING DIAGRAM

SPECIFICATIONS

Absolute Maximum Ratings		
Operating Temperature		0° to +70° C
Voltage on any pin with respect to Ground*		−0.5 to +7V
Power Dissipation		1 Watt
Storage Temperature	plastic	−55° to +125° C
	ceramic	−65° to +150°C

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to the DC electrical characteristics specified.

*Pin 17 = −0.5V to +12V. Increasing voltage on Pin 17 will decrease T_{pw}.

DC ELECTRICAL CHARACTERISTICS

V_{cc} = 5V ±5%, GND = OV, T_A = 0° to 70°C.

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	CONDITIONS
V_{OL}	TTL low level output		0.4	V	i_{OL} = 1.6 mA
V_{OH}	TTL high level output	2.0		V	i_{OH} = −100 μA
V_{IL}	STB in low voltage		0.8	V	
V_{IH}	STB in high voltage	2.4		V	
i_{CC}	Supply Current		80	mA	All outputs open

Table 2 DC ELECTRICAL CHARACTERISTICS

SWITCHING CHARACTERISTICS

V_{CC} = 5V ± 5%, GND = 0V T_A = 0° to 70° C

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	CONDITIONS
t_{PD}	STB IN to ø1		140	ns	
t_{pw}	Pulse Width (any output)	100	300	ns	CL = 30pf
t_{PR}	Rise Time (any output)		30	ns	CL = 30pf
t_{PF}	Fall Time (any output)		25	ns	CL = 30pf
f_S	STROBE PULSE WIDTH		1.0	μs	combined t_{pw} = 400 ns
t_{DPW}	Pulse Width Differential		± 10	%	Referenced to ø1, 100-300 ns.

Table 3 SWITCHING CHARACTERISTICS

NOTE: T_{PW} measured at 50% V_{OH} Point; V_{OL} = 0.8V, V_{OH} = 2.0V.

See page 725 for ordering information.

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WESTERN DIGITAL
CORPORATION

WD9216-00/WD9216-01
Floppy Disk Data Separator — FDDS

FEATURES

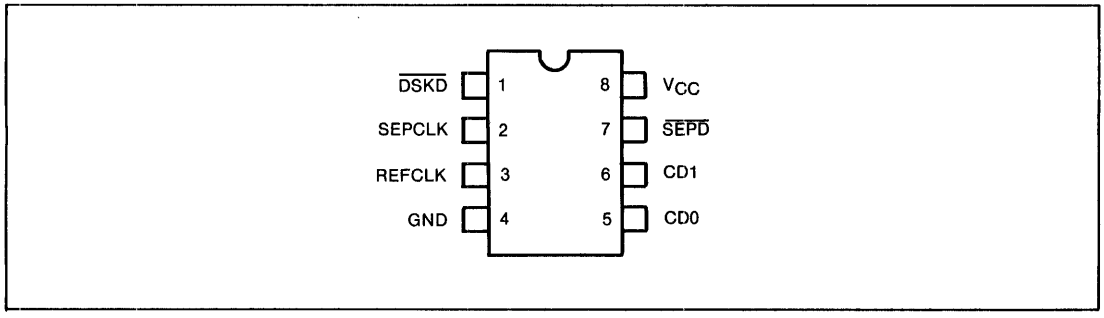
- PERFORMS COMPLETE DATA SEPARATION FUNCTION FOR FLOPPY DISK DRIVES
- SEPARATES FM OR MFM ENCODED DATA FROM ANY MAGNETIC MEDIA
- ELIMINATES SEVERAL SSI AND MSI DEVICES NORMALLY USED FOR DATA SEPARATION
- NO CRITICAL ADJUSTMENTS REQUIRED
- COMPATIBLE WITH WESTERN DIGITAL 179X, 176X AND OTHER FLOPPY DISK CONTROLLERS
- SMALL 8-PIN DUAL-IN-LINE PACKAGE
- +5 VOLT ONLY POWER SUPPLY
- TTL COMPATIBLE INPUTS AND OUTPUTS

GENERAL DESCRIPTION

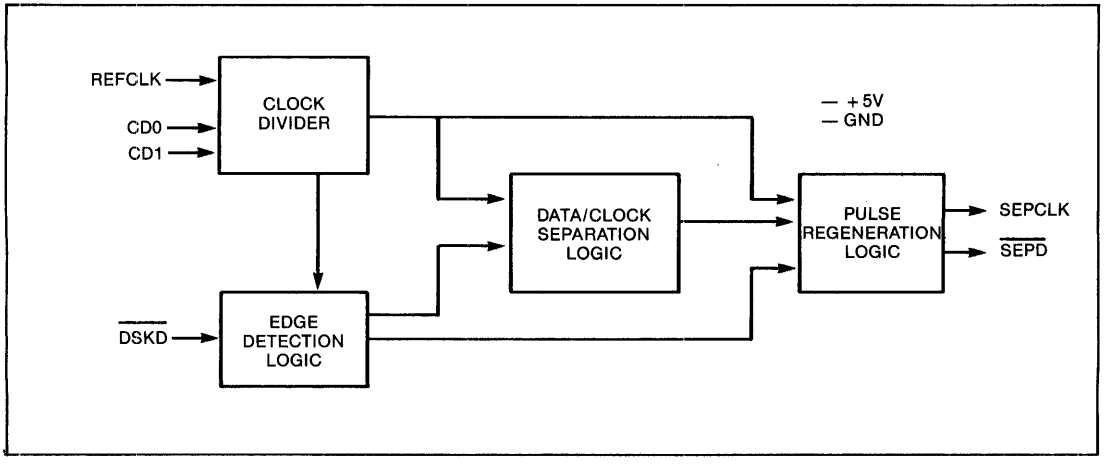
The Floppy Disk Data Separator provides a low cost solution to the problem of converting a single stream of pulses from a floppy disk drive into separate Clock and Data inputs for a Floppy Disk Controller.

The FDDS consists primarily of a clock divider, a long-term timing corrector, a short-term timing corrector, and reclocking circuitry. Supplied in an 8-pin Dual-In-Line package to save board real estate, the FDDS operates on +5 volts only and is TTL compatible on all inputs and outputs.

The WD9216 is available in two versions; the WD9216-00, which is intended for 5¼" disks and the WD9216-01 for 5¼" and 8" disks.



PIN CONFIGURATION



FLOPPY DISK DATA SEPARATOR BLOCK DIAGRAM

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

Operating Temperature Range..... 0°C to +70°C
Storage Temperature Range..... −55°C to 125°C
Positive Voltage on any Pin,
with respect to ground..... +8.0V
Negative Voltage on any Pin,
with respect to ground..... −0.3V

* Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

OPERATING CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, unless otherwise noted)

PARAMETER		MIN.	TYP.	MAX.	UNITS	COMMENTS
D.C. CHARACTERISTICS						
INPUT VOLTAGE LEVELS						
Low Level V_{IL}				0.8	V	
High Level V_{IH}		2.0			V	
OUTPUT VOLTAGE LEVELS						
Low Level V_{OL}				0.4	V	I_{OL} = 1.6mA
High Level V_{OH}		2.4			V	I_{OH} = −100μA
INPUT CURRENT						
Leakage I_{IL}				10	μA	$0 \leq V_{IN} \leq V_{DD}$
INPUT CAPACITANCE						
All Inputs				10	pF	
POWER SUPPLY CURRENT						
I_{DD}				50	mA	
A.C. CHARACTERISTICS						
Symbol						
f_{CY}	REFCLK Frequency	0.2		4.3	MHz	WD 9216-00
f_{CY}	REFCLK Frequency	0.2		8.3	MHz	WD 9216-01
t_{CKH}	REFCLK High Time	50		2500	ns	
t_{CKL}	REFCLK Low Time	50		2500	ns	
t_{SDON}	REFCLK to $\overline{SEPD}$ "ON" Delay		100		ns	
t_{SDOFF}	REFCLK to $\overline{SEPD}$ "OFF" Delay		100		ns	
t_{SPCK}	REFCLK to SEPCLK Delay	100			ns	
t_{DLL}	DSKD Active Low Time	0.1		100	μs	
t_{DLH}	DSKD Active High Time	0.2		100	μs	

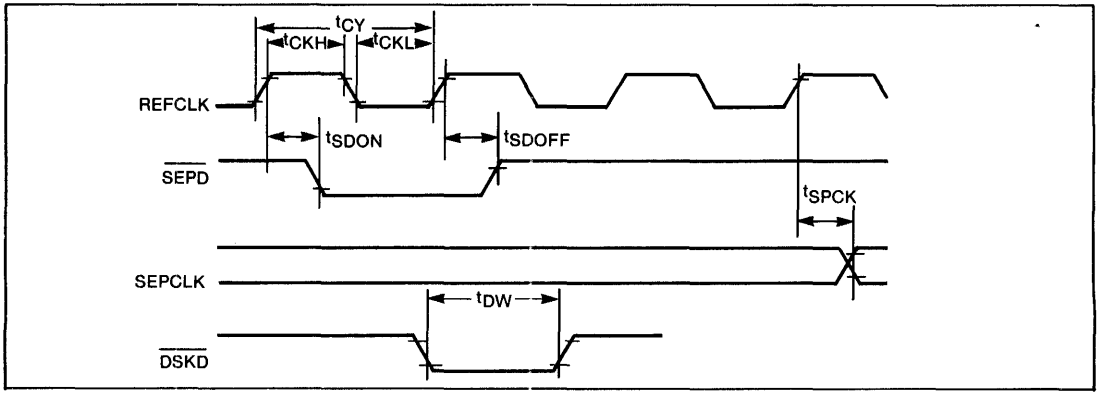


Figure 3. AC CHARACTERISTICS

DESCRIPTION OF PIN FUNCTIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	$\overline{\text{Disk Data}}$	$\overline{\text{DSKD}}$	Data input signal direct from disk drive. Contains combined clock and data waveform.
2	Separated Clock	SEPCLK	Clock signal output from the FDDS derived from floppy disk drive serial bit stream.
3	Reference Clock	REFCLK	Reference clock input.
4	Ground	GND	Ground.
5,6	Clock Divisor	CD0, CD1	CD0 and CD1 control the internal clock divider circuit. The internal clock is a submultiple of the REFCLK according to the following table: CD1 CD0 Divisor 0 0 1 0 1 2 1 0 4 1 1 8
7	$\overline{\text{Separated Data}}$	$\overline{\text{SEPD}}$	SEPD is the data output of the FDDS
8	Power Supply	V_{CC}	+5 volt power supply

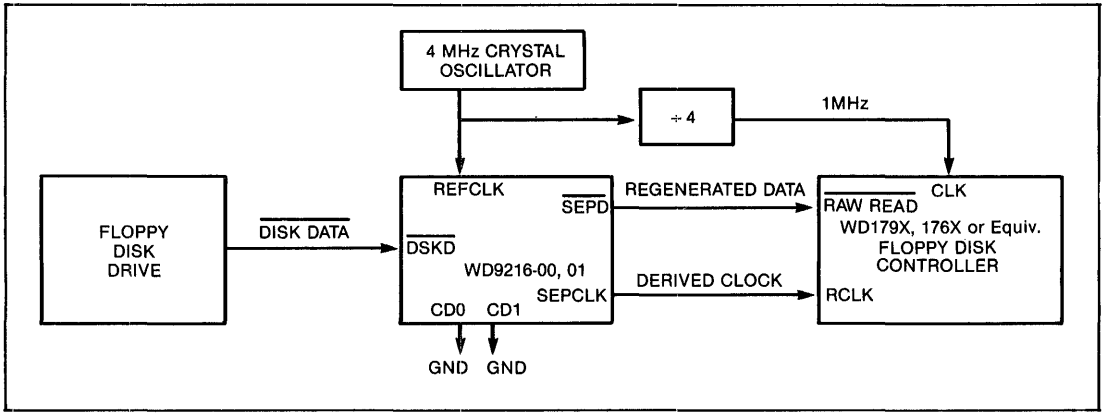


Figure 1.
TYPICAL SYSTEM CONFIGURATION
(5¼" Drive, Double Density)

OPERATION

A reference clock (REFCLK) of between 2 and 8 MHz is divided by the FDDS to provide an internal clock. The division ratio is selected by inputs CD0 and CD1. The reference clock and division ratio should be chosen per table 1.

The FDDS detects the leading edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPARATED CLOCK output.

Separate short and long term timing correctors assure accurate clock separation.

The internal clock frequency is nominally 16 times the SEPCLK frequency. Depending on the internal timing correction, the internal clock may be a minimum of 12 times to a maximum of 22 times the SEPCLK frequency.

The reference clock (REFCLK) is divided to provide the internal clock according to pins CD0 and CD1.

TABLE 1:
CLOCK DIVIDER SELECTION TABLE

DRIVE (8″ or 5¼″)	DENSITY (DD or SD)	REFCLK MHz	CD1	CD0	REMARKS
8	DD	8	0	0	Select either one
8	SD	8	0	1	
8	SD	4	0	0	
5¼	DD	8	0	1	Select either one
5¼	DD	4	0	0	
5¼	SD	8	1	0	Select any one
5¼	SD	4	0	1	
5¼	SD	2	0	0	

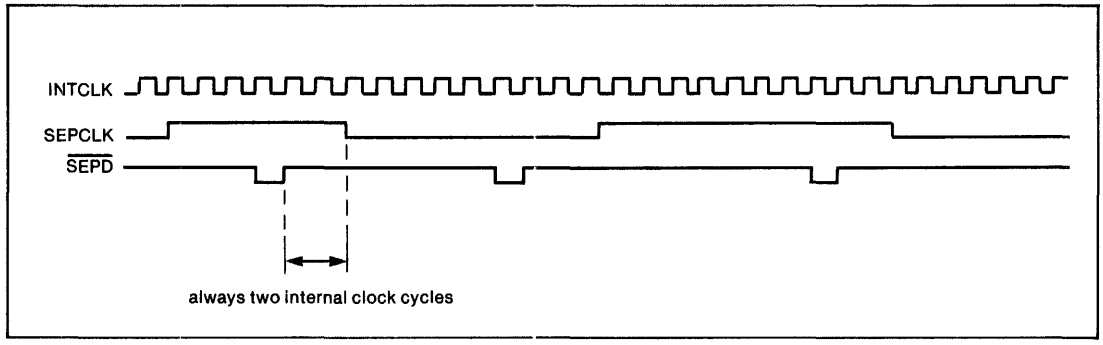


Figure 2.

See page 725 for ordering information.

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CRT Controllers

WD8275 Programmable CRT Controller

FEATURES

- PROGRAMMABLE SCREEN AND CHARACTER FORMAT
- 6 INDEPENDENT VISUAL FIELD ATTRIBUTES
- 11 VISUAL CHARACTER ATTRIBUTES (GRAPHIC CAPABILITY)
- CURSOR CONTROL (4 TYPES)
- LIGHT PEN DETECTION AND REGISTERS
- DUAL ROW BUFFERS
- PROGRAMMABLE DMA BURST MODE
- SINGLE +5V SUPPLY
- 40-PIN PACKAGE

GENERAL DESCRIPTION

The WD8275 Programmable CRT Controller is a single chip device to Interface CRT raster scan displays with microcomputer systems. Its primary function is to refresh the display by buffering the information from main memory and keeping track of the display position of the screen. The flexibility designed into the WD8275 will allow simple interface to almost any raster scan CRT display with a minimum of external hardware and software overhead.

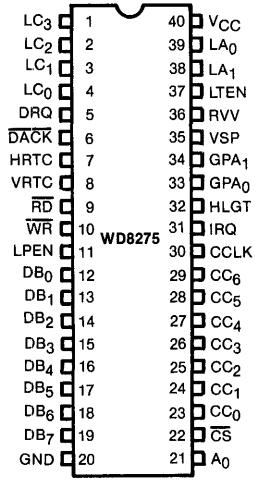


Figure 1. PIN CONFIGURATION

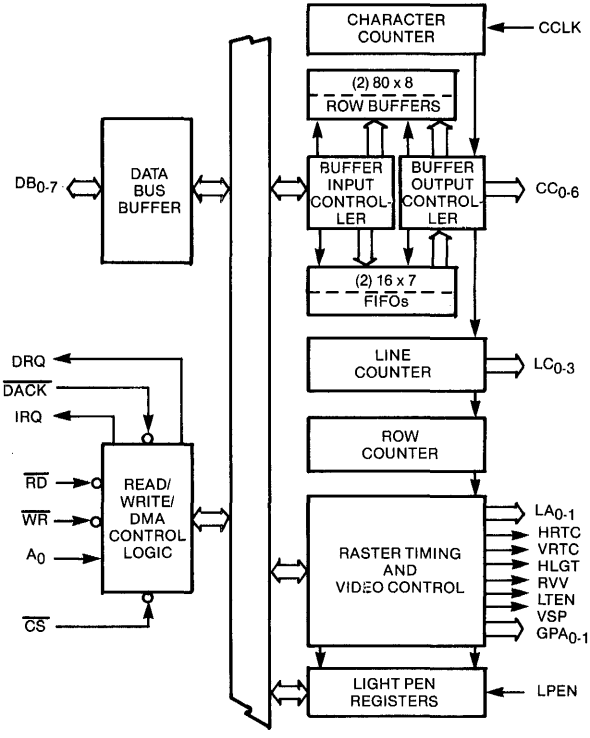


Figure 2. BLOCK DIAGRAM

TABLE 1. PIN DESCRIPTIONS

PIN NO.	TYPE	PIN NAME	SYMBOL	FUNCTION
1 2 3 4	O	LINE COUNT	LC_3 LC_2 LC_1 LC_0	Output from the line counter which is used to address the character generator for the line positions on the screen.
5	O	DMA REQUEST	DRQ	Output signal to the DMA controller requesting a DMA cycle.
6	I	DMA ACKNOWLEDGE	$\overline{DACK}$	Input signal from the DMA controller acknowledging that the requested DMA cycle has been granted.
7	O	HORIZONTAL RETRACE	HRTC	Output signal which is active during the programmed horizontal retrace interval. During this period the VSP output is high and the LTEN output is low.
8	O	VERTICAL RETRACE	VRTC	Output signal which is active during the programmed vertical retrace interval. During this period the VSP output is high and the LTEN output is low.
9	I	READ INPUT	$\overline{RD}$	A control signal to read registers.
10	I	WRITE INPUT	$\overline{WR}$	A control signal to write commands into the control registers or write data into the row buffers during a DMA cycle.
11	I	LIGHT PEN	LPEN	Input signal from the CRT system signifying that a light pen signal has been detected.
12 13 14 15 16 17 18 19	I/O	BIDIRECTIONAL THREE-STATE DATA BUS LINES	DB_0 DB_1 DB_2 DB_3 DB_4 DB_5 DB_6 DB_7	The outputs are enabled during a read of the C or P ports.
20		GROUND	Ground	
21	I	PORT ADDRESS	A_0	A high input on A_0 selects the "C" port or command registers and a low input selects the "P" port or parameter registers.
22	I	CHIP SELECT	CS	The read and write are enabled by CS.
23 24 25 26 27 28 29	O	CHARACTER CODES	CC_0 CC_1 CC_2 CC_3 CC_4 CC_5 CC_6	Output from the row buffers used for character selection in the character generator.
30	I	CHARACTER CLOCK	CCLK	From dot/timing logic.
31	O	INTERRUPT REQUEST	IRQ	Interrupt request.
32	O	HIGHLIGHT	HLGT	Output signal used to intensify the display at particular positions on the screen as specified by the character attribute codes or field attribute codes.

TABLE 1. PIN DESCRIPTIONS (Continued)

PIN NO.	TYPE	PIN NAME	SYMBOL	FUNCTION
33 34	O	GENERAL PURPOSE ATTRIBUTE CODES	GPA_1 GPA_0	Outputs which are enabled by the general purpose field attribute codes.
35	O	VIDEO SUPPRESSION	VSP	Output signal used to blank the video signal to the CRT. This output is active: —during the horizontal and vertical retrace intervals. —at the top and bottom lines of rows if underline is programmed to be number 8 or greater. —when an end of row or end of screen code is detected. —when a DMA underrun occurs. —at regular intervals (1/16 frame frequency for cursor, 1/32 frame frequency for character and field attributes) — to create blinking displays as specified by cursor, character attribute, or field attribute programming.
36	O	REVERSE VIDEO	RVV	Output signal used to indicate the CRT circuitry to reverse the video signal. This output is active at the cursor position if a reverse video block cursor is programmed or at the positions specified by the field attribute codes.
37	O	LIGHT ENABLE	LTEN	Output signal used to enable the video signal to the CRT. This output is active at the programmed underline cursor position, and at positions specified by attribute codes.
38 39	O	LINE ATTRIBUTE CODES	LA_0 LA_1	These attribute codes have to be decoded externally by the dot/timing logic to generate the horizontal and vertical line combinations for the graphic displays specified by the character attribute codes.
40		+5V POWER SUPPLY	V_{CC}	+5V power supply.

FUNCTIONAL DESCRIPTION

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the WD8275 to the system Data Bus.

This functional block accepts inputs from the System Control Bus and generates control signals for overall device operation. It contains the Command, Parameter, and Status Registers that store the various control formats for the device functional definition.

A_0	OPERATION	REGISTER
0	Read	PREG
0	Write	PREG
1	Read	SREG
1	Write	CREG

$\overline{RD}$ (READ)

A "low" on this input informs the WD8275 that the CPU is reading data or status information from the WD8275.

$\overline{WR}$ (WRITE)

A "low" on this input informs the WD8275 that the CPU is writing data or control words to the WD8275.

$\overline{CS}$ (CHIP SELECT)

A "low" on this input selects the WD8275. No reading or writing will occur unless the device is selected. When CS is high, the Data Bus in the float state and RD and WR will have no effect on the chip.

DRQ (DMA REQUEST)

A "high" on this output informs the DMA Controller that the WD8275 desires a DMA transfer.

$\overline{DACK}$ (DMA ACKNOWLEDGE)

A "low" on this input informs the WD8275 that a DMA cycle is in progress.

IRQ (INTERRUPT REQUEST)

A "high" on this output informs the CPU that the WD8275 desires interrupt service.

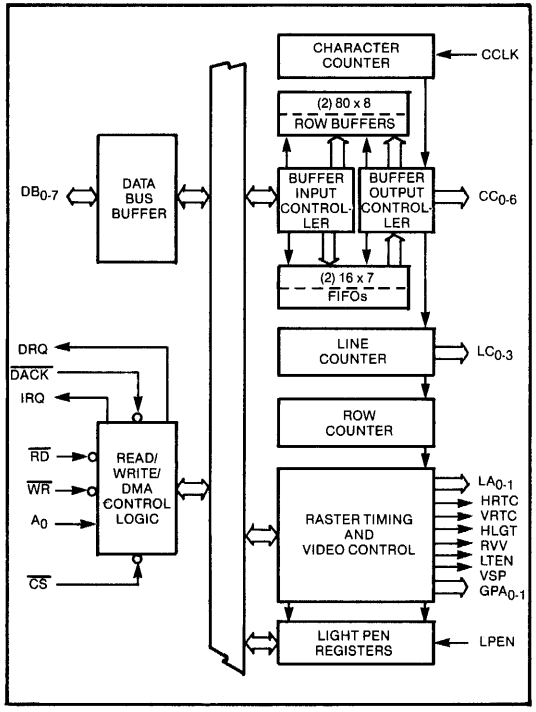


Figure 3.
WD8275 BLOCK DIAGRAM SHOWING DATA BUS BUFFER AND READ/WRITE FUNCTIONS

A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	Write WD8275 Parameter
0	1	0	0	Read WD8275 Parameter
1	0	1	0	Write WD8275 Command
1	1	0	0	Read WD8275 Status
X	1	1	0	Three-State
X	X	X	1	Three-State

Character Counter

The Character Counter is a programmable counter that is used to determine the number of characters to be displayed per row and the length of the horizontal retrace interval. It is driven by the CCLK (Character Clock) input, which should be a derivative of the external dot clock.

Line Counter

The Line Counter is a programmable counter that is used to determine the number of horizontal lines (Sweeps) per character row. Its outputs are used to address the external character generator ROM.

Row Counter

The Row Counter is a programmable counter that is used to determine the number of character rows to be displayed per frame and length of the vertical retrace interval.

Light Pen Registers

The Light Pen Registers are two registers that store the contents of the character counter and the row counter whenever there is a rising edge on the LPEN (Light Pen) input.

NOTE:
Software correction is required.

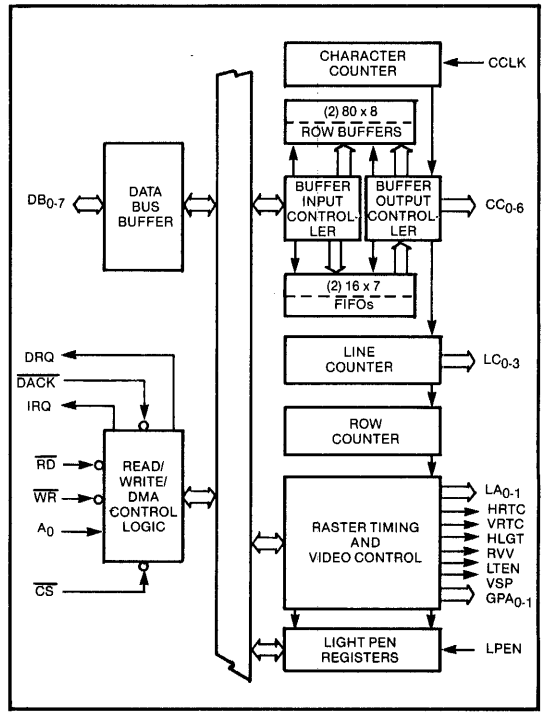


Figure 4.
WD8275 BLOCK DIAGRAM SHOWING COUNTER AND REGISTER FUNCTIONS

Raster Timing and Video Controls

The Raster Timing circuitry controls the timing of the HRTC (Horizontal Retrace) and VRTC (Vertical Retrace) outputs. The Video Control circuitry controls the generation of LA_{0-1} (Line Attribute), HGLT (Highlight), RVV (Reverse Video), LTEN (Light Enable), VSP (Video Suppress), and GPA_{0-1} (General Purpose Attribute) outputs.

Row Buffers

The Row Buffers are two 80-character buffers. They are filled from the microcomputer system memory with the character codes to be displayed. While one row buffer is displaying a row of characters, the other is being filled with the next row of characters.

FIFOs

There are two 16 character FIFOs in the WD8275. They are used to provide extra row buffer length in the Transparent Attribute Mode (see Detailed Operation section).

Buffer Input/Output Controllers

The Buffer Input/output Controllers decode the characters being placed in the row buffers. If the character is a character attribute, field attribute or special code, these controllers control the appropriate action. (Examples: An "End of Screen-Stop DMA" special code will cause the Buffer Input Controller to stop further DMA requests. A "Highlight" field attribute will cause the Buffer Output Controller to activate the HGLT output.)

SYSTEM OPERATION

The WD8275 is programmable to a large number of different display formats. It provides raster timing, display row buffering, visual attribute decoding, cursor timing, and light pen detection.

It is designed to interface with a DMA Controller and standard character generator ROMs for dot matrix decoding. Dot level timing must be provided by external circuitry.

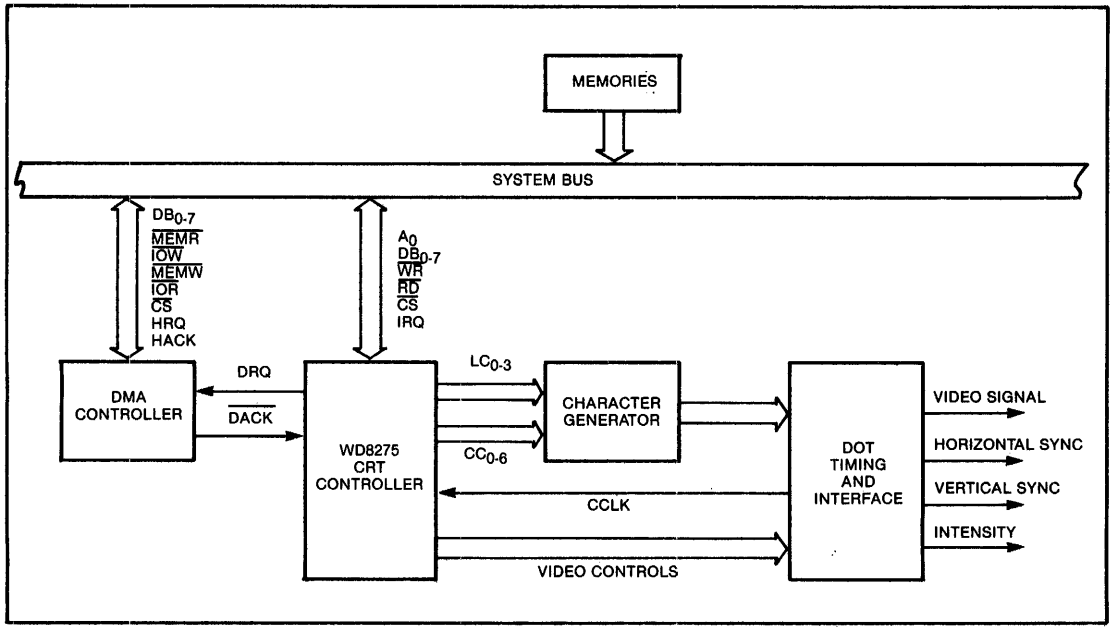


Figure 5. WD8275 SYSTEMS BLOCK DIAGRAM SHOWING SYSTEMS OPERATION

GENERAL SYSTEMS OPERATIONAL DESCRIPTION

The WD8275 provides a "window" into the microcomputer system memory.

Display characters are retrieved from memory and displayed on a row-by-row basis. The WD8275 has two row buffers. While one row buffer is being used for display, the other is being filled with the next row of characters to be displayed. The number of display characters per row and the number of character rows per frame are software programmable, providing easy interface to most CRT displays. (See Programming Section.)

The WD8275 requests DMA to fill the row buffer that is not being used for display. DMA burst length and spacing is programmable. (See Programming Section.)

The WD8275 displays character rows one line at a time.

The number of lines per character row, the underline position, and blanking of top and bottom lines are programmable. (See Programming Section.)

The WD8275 provides special Control Codes which can be used to minimize DMA or software overhead. It also provides Visual Attribute Codes to cause special action or symbols on the screen without the use of the character generator (see Visual Attributes Section).

The WD8275 also controls raster timing. This is done by generating Horizontal Retrace (HRTC) and Vertical Retrace (VRTC) signals. The timing of these signals is programmable.

The WD8275 can generate a cursor. Cursor location and format are programmable. (See Programming Section.)

The WD8275 has a light pen input and registers. The light pen input is used to load the registers. Light pen registers can be read on command. (See Programming Section.)

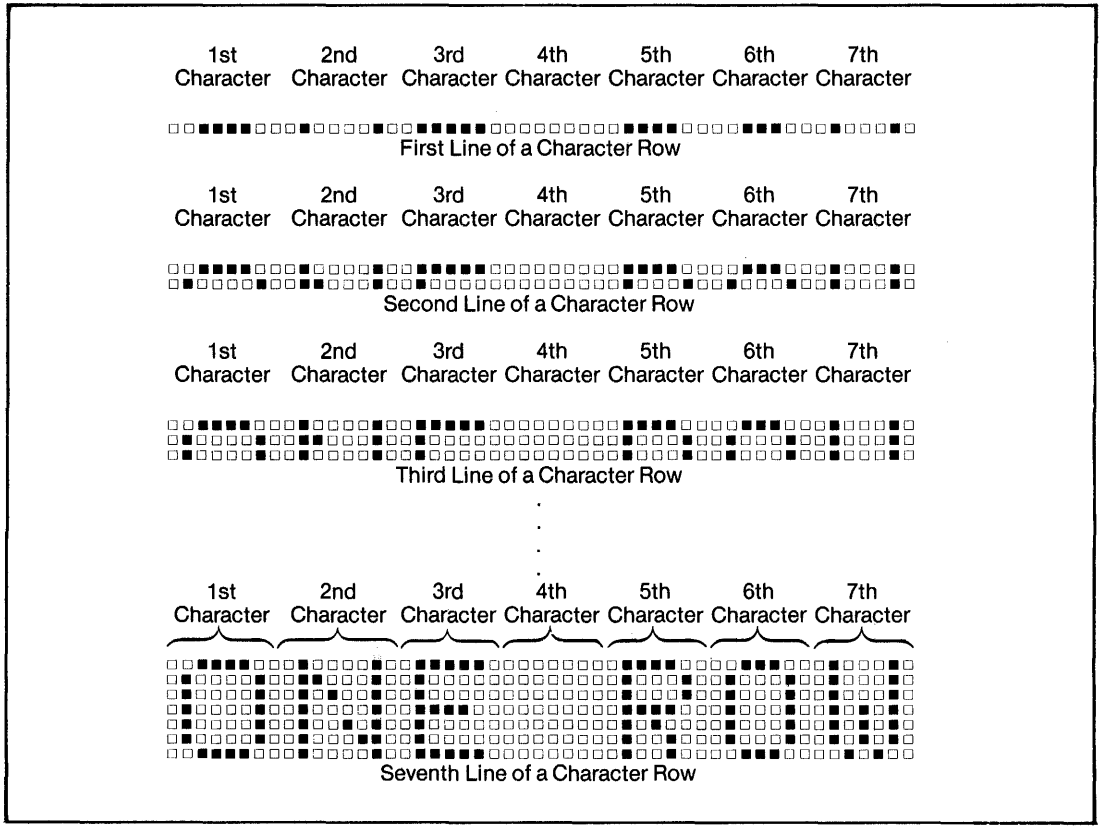


Figure 6. DISPLAY OF A CHARACTER ROW

DISPLAY ROW BUFFERING

Before the start of a frame, the WD8275 requests DMA and one row buffer is filled with characters.

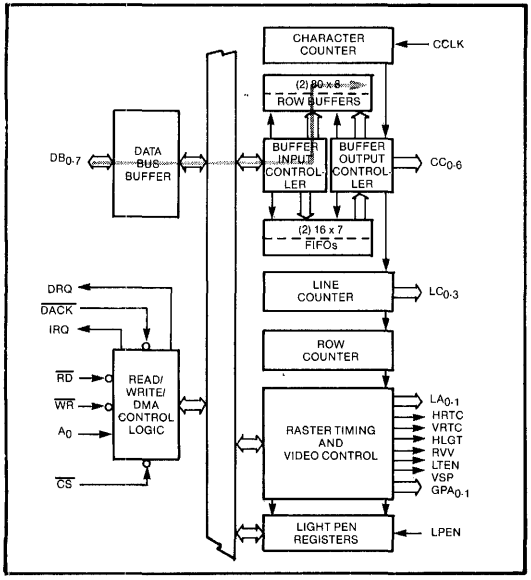


Figure 7.
FIRST ROW BUFFER FILLED

When the first horizontal sweep is started, character codes are output to the character generator from the row buffer just filled. Simultaneously, DMA begins filling the other row buffer with the next row of characters.

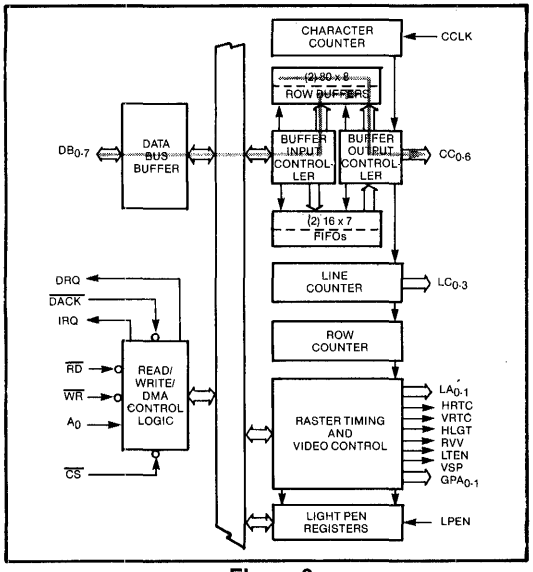


Figure 8.
SECOND BUFFER FILLED, FIRST ROW DISPLAYED

After all the lines of the character row are scanned, the roles of the two row buffers are reversed and the same procedure is followed for the next row.

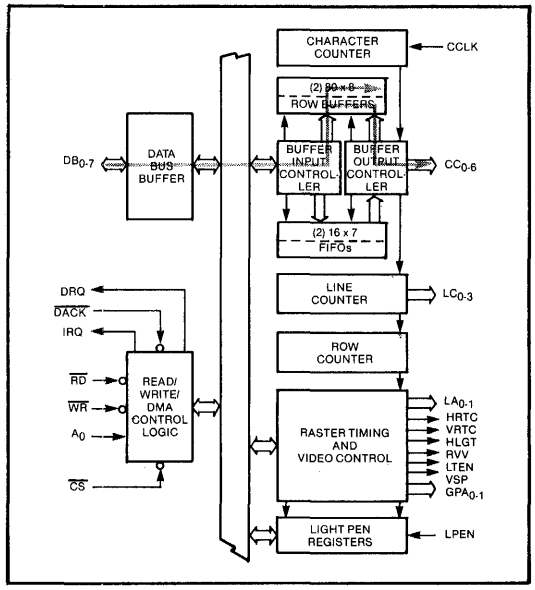


Figure 9.
FIRST BUFFER FILLED WITH THIRD ROW, SECOND ROW DISPLAYED

This is repeated until all of the character rows are displayed.

DISPLAY FORMAT

Screen Format

The WD8275 can be programmed to generate from 1 to 80 characters per row, and from 1 to 64 rows per frame.

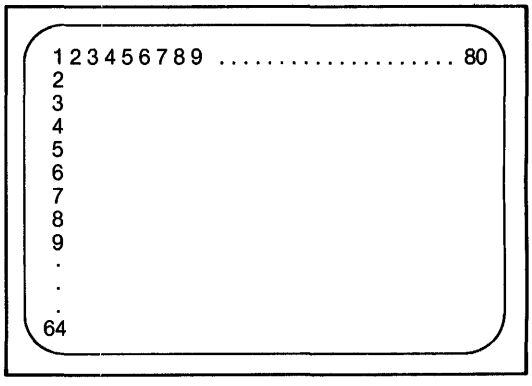


Figure 10.
SCREEN FORMAT

The WD8275 can also be programmed to blank alternate rows. In this mode, the first row is displayed, the second blanked, the third displayed, etc. DMA is not requested for the blanked rows.

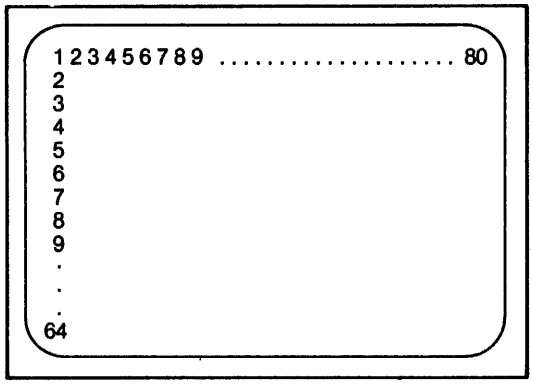


Figure 11.
BLANK ALTERNATE ROWS MODE

Row Format

The WD8275 is designed to hold the line count stable while outputting the appropriate character codes during each horizontal sweep. The line count is incremented during horizontal retrace and the whole row of character codes are output again during the next sweep. This is continued until the entire character row is displayed.

The number of lines (horizontal sweeps) per character row is programmable from 1 to 16.

The output of the line counter can be programmed to be in one of two modes.

In mode 0, the output of the line *counter* is the same as the line *number*.

In mode 1, the line *counter* is offset by one from the line *number*.

NOTE:
In mode 1, while the *first* line (line number 0) is being displayed, the *last* count is output by the line counter (see examples).

Line Number	Line Counter Mode 0	Line Counter Mode 1
0	0 0 0 0	1 1 1 1
1	0 0 0 1	0 0 0 0
2	0 0 1 0	0 0 0 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 0 1 1
5	0 1 0 1	0 1 0 0
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 1 0
8	1 0 0 0	0 1 1 1
9	1 0 0 1	1 0 0 0
10	1 0 1 0	1 0 0 1
11	1 0 1 1	1 0 1 0
12	1 1 0 0	1 0 1 1
13	1 1 0 1	1 1 0 0
14	1 1 1 0	1 1 0 1
15	1 1 1 1	1 1 1 0

Figure 12.
EXAMPLE OF A 16-LINE FORMAT

Line Number	Line Counter Mode 0	Line Counter Mode 1
0	0 0 0 0	1 0 0 1
1	0 0 0 1	0 0 0 0
2	0 0 1 0	0 0 0 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 0 1 1
5	0 1 0 1	0 1 0 0
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 1 0
8	1 0 0 0	0 1 1 1
9	1 0 0 1	1 0 0 0

Figure 13.
EXAMPLE OF A 10-LINE FORMAT

Mode 0 is useful for character generators that leave address zero blank and start at address 1. Mode 1 is useful for character generators which start at address zero.

Underline placement is also programmable (from line *number* 0 to 15). This is independent of the line *counter* mode.

If the line *number* of the underline is greater than 7 (line *number* MSB = 1), then the top and bottom lines will be blanked.

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ □ □ □ □ □ □	0 0 0 0	1 0 1 1
1	□ □ □ □ ■ □ □ □ □	0 0 0 1	0 0 0 0
2	□ □ □ ■ □ ■ □ □ □	0 0 1 0	0 0 0 1
3	□ □ ■ □ □ □ ■ □ □	0 0 1 1	0 0 1 0
4	□ ■ □ □ □ □ □ ■ □	0 1 0 0	0 0 1 1
5	□ ■ □ □ □ □ □ ■ □	0 1 0 1	0 1 0 0
6	□ ■ ■ ■ ■ ■ ■ ■ □	0 1 1 0	0 1 0 1
7	□ ■ □ □ □ □ □ ■ □	0 1 1 1	0 1 1 0
8	□ ■ □ □ □ □ □ ■ □	1 0 0 0	0 1 1 1
9	□ ■ □ □ □ □ □ ■ □	1 0 0 1	1 0 0 0
10	■ ■ ■ ■ ■ ■ ■ ■ ■	1 0 1 0	1 0 0 1
11	□ □ □ □ □ □ □ □ □	1 0 1 1	1 0 1 0

Top and Bottom Lines are Blanked

Figure 14.
UNDERLINE IN LINE NUMBER 10

If the line *number* of the underline is less than or equal to 7 (line *number* MSB = 0), then the top and bottom lines will *not* be blanked.

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ □ □ □ □ □	0 0 0 0	0 1 1 1
1	□ □ □ ■ □ □ □ □	0 0 0 1	0 0 0 0
2	□ □ ■ □ ■ □ □ □	0 0 1 0	0 0 0 1
3	□ ■ □ □ □ ■ □ □	0 0 1 1	0 0 1 0
4	□ ■ □ □ □ ■ □ □	0 1 0 0	0 0 1 1
5	□ ■ ■ ■ ■ ■ □ □	0 1 0 1	0 1 0 0
6	□ ■ □ □ □ ■ □ □	0 1 1 0	0 1 0 1
7	■ ■ ■ ■ ■ ■ ■ ■	0 1 1 1	0 1 1 0

Top and Bottom Lines are not Blanked

Figure 15.
UNDERLINE IN LINE NUMBER 7

If the line *number* of the underline is greater than the maximum number of lines, the underline will not appear.

Blanking is accomplished by the VSP (Video Suppression) signal. Underline is accomplished by the LTEN (Light Enable) signal.

Dot Format

Dot width and character width are dependent upon the external timing and control circuitry.

Dot level timing circuitry should be designed to accept the parallel output of the character generator and shift it out serially at the rate required by the CRT display.

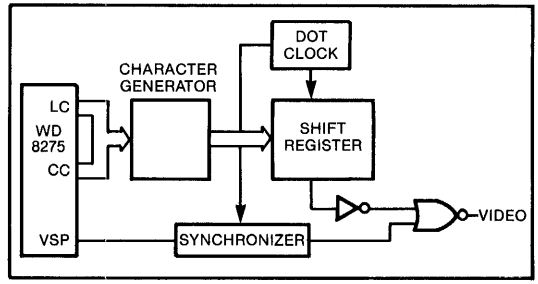


Figure 16.
TYPICAL DOT LEVEL BLOCK DIAGRAM

Dot width is a function of dot clock frequency.

Character width is a function of the character generator width.

Horizontal character spacing is a function of the shift register length.

NOTE:
Video control and timing signals must be synchronized with the video signal due to the character generator access delay.

RASTER TIMING

The character counter is driven by the character clock input (CCLK). It counts out the characters being displayed (programmable from 1 to 80). It then causes the line counter to increment, and it starts counting out the horizontal retrace interval (programmable from 2 to 32). This is constantly repeated.

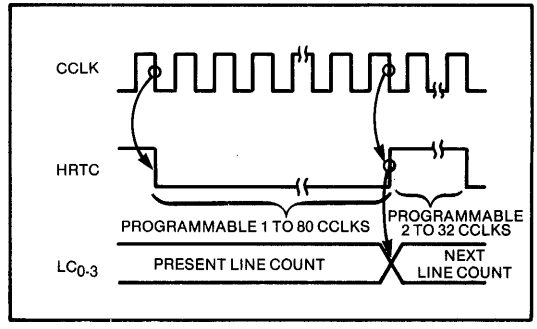


Figure 17.
LINE TIMING

The line counter is driven by the character counter. It is used to generate the line address outputs (LC_{0-3}) for the character generator. After it counts all of the lines in a character row (programmable from 1 to 16), it increments the row counter, and starts over again. (See Character Format Section for detailed description of Line Counter functions.)

The row counter is an internal counter driven by the line counter. It controls the functions of the row buffers and counts the number of character rows displayed.

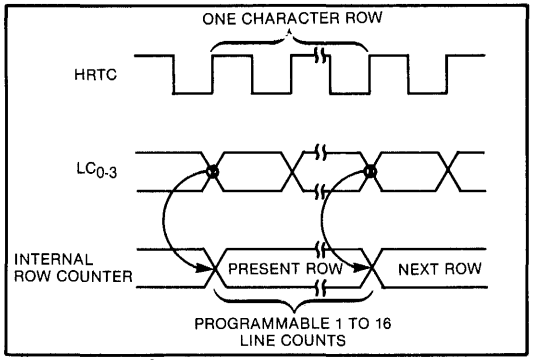


Figure 18.
ROW TIMING

After the row counter counts all of the rows in a frame (programmable from 1 to 64), it starts counting out the vertical retrace interval (programmable from 1 to 4).

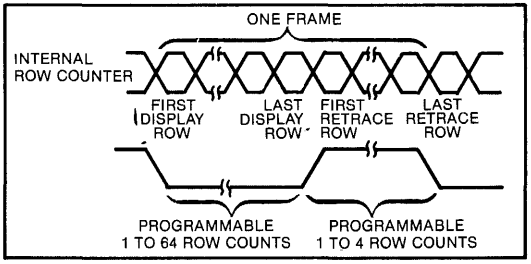


Figure 19.
FRAME TIMING

The Video Suppression Output (VSP) is active during horizontal and vertical retrace intervals.

Dot level timing circuitry must synchronize these outputs with the video signal to the CRT Display.

DMA TIMING

The WD8275 can be programmed to request burst DMA transfers of 1 to 8 characters. The interval between bursts is also programmable (from 0 to 55 character clock periods ± 1). This allows the user to tailor his DMA overhead to fit his system needs.

The first DMA request of the frame occurs one *row time* before the end of vertical retrace. DMA requests continue as programmed, until the row buffer is filled. If the row buffer is filled in the middle of a burst, the WD8275 terminates the burst and resets the burst counter. No more DMA requests will occur until the *beginning* of the *next* row. At that time, DMA requests are activated as programmed until the other buffer is filled.

The first DMA request for a row will start at the first character clock of the preceding row. If the burst mode is used, the first DMA request may occur a number of character clocks later. This number is equal to the programmed burst space.

If, for any reason, there is a DMA underrun, a flag in the status word will be set.

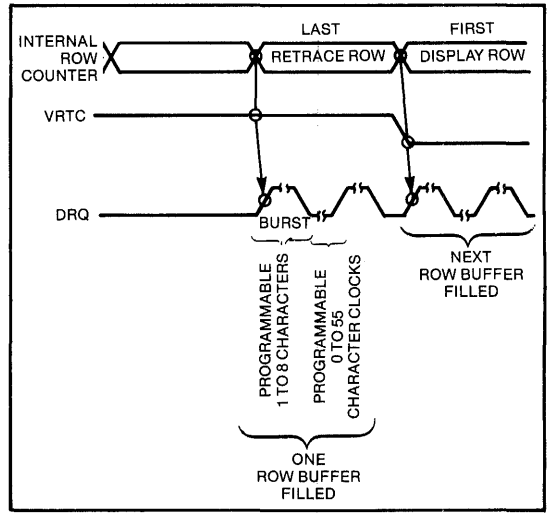


Figure 20. DMA TIMING

The DMA controller is typically initialized for the next frame at the end of the current frame.

INTERRUPT TIMING

The WD8275 can be programmed to generate an interrupt request at the end of each frame. This can be used to reinitialize the DMA controller. If the WD8275 interrupt enable flag is set, an interrupt request will occur at the *beginning* of the *last display row.*

IRQ will go inactive after the status register is read.

A reset command will also cause IRQ to go inactive, but this is not recommended during normal service.

Another method of reinitializing the DMA controller is to have the DMA controller itself interrupt on terminal count. With this method, the WD8275 interrupt enable flag should not be set.

NOTE:
Upon power-up, the WD8275 Interrupt Enable Flag may be set. As a result, the user's cold start routine should write a reset command to the WD8275 before system interrupts are enabled.

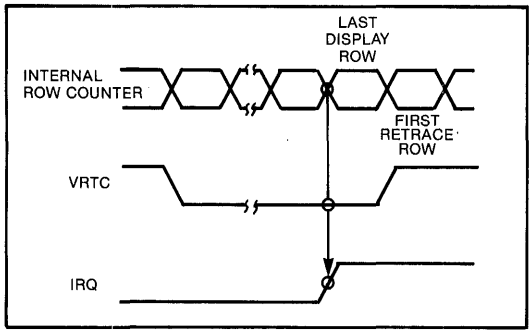


Figure 21.
BEGINNING OF INTERRUPT REQUEST

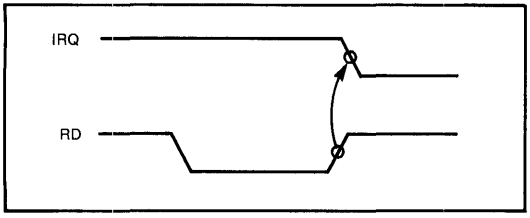


Figure 22.
END OF INTERRUPT REQUEST

VISUAL ATTRIBUTES AND SPECIAL CODES

The characters processed by the WD8275 are 8-bit quantities. The character code outputs provide the character generator with 7 bits of address. The Most Significant Bit is the extra bit and it is used to determine if it is a normal display character (MSB = 0), or if it is a Visual Attribute or Special Code (MSB = 1).

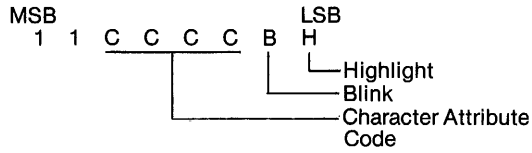
There are two types of Visual Attribute Codes. They are Character Attributes and Field Attributes.

Character Attribute Codes

Character attribute codes are codes that can be used to generate graphics symbols without the use of a character generator. This is accomplished by selectively activating the Line Attribute outputs (LA_{0-1}), the Video Suppression output (VSP), and the Light Enable output. The dot level timing circuitry can use these signals to generate the proper symbols.

Character attributes can be programmed to blink or be highlighted individually. Blinking is accomplished with the Video Suppression output (VSP). Blink frequency is equal to the screen refresh frequency divided by 32. Highlighting is accomplished by activating the Highlight output (HGLT).

Character Attributes



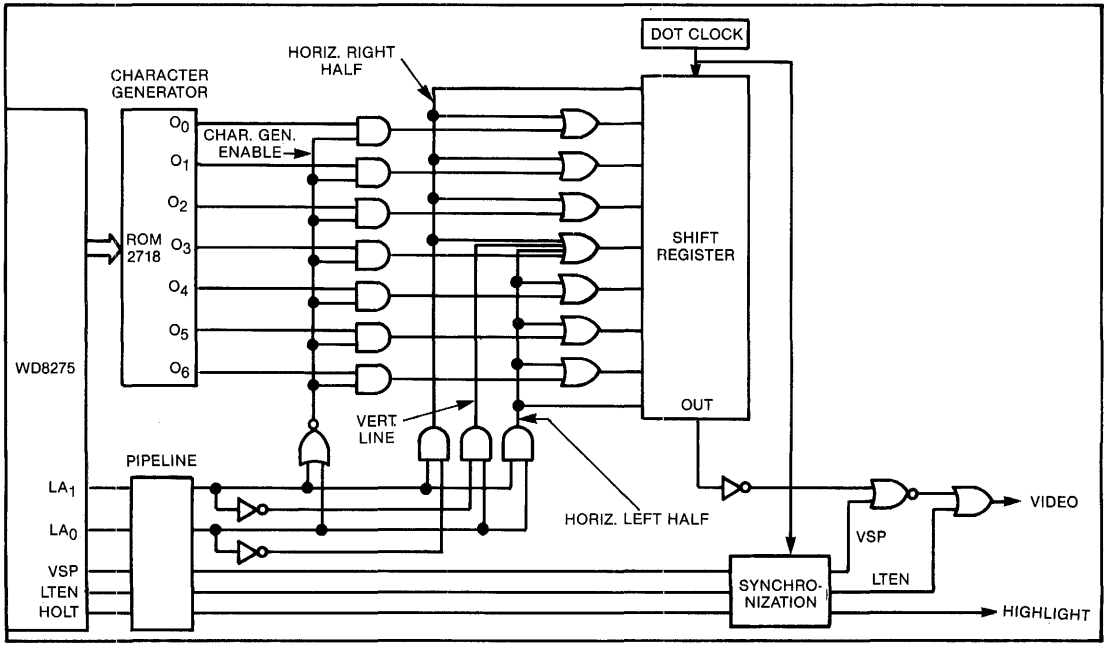
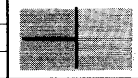
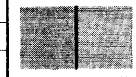


Figure 23. TYPICAL CHARACTER ATTRIBUTE LOGIC

TABLE 2. CHARACTER ATTRIBUTES

Character attributes were designed to produce the following graphics:

CHARACTER ATTRIBUTE CODE "CCCC"		OUTPUTS				SYMBOL	DESCRIPTION
		LA_1	LA_0	VSP	LTEN		
0000	Above Underline	0	0	1	0		Top Left Corner
	Underline	1	0	0	0		
	Below Underline	0	1	0	0		
0001	Above Underline	0	0	1	0		Top Right Corner
	Underline	1	1	0	0		
	Below Underline	0	1	0	0		
0010	Above Underline	0	1	0	0		Bottom Left Corner
	Underline	1	0	0	0		
	Below Underline	0	0	1	0		
0011	Above Underline	0	1	0	0		Bottom Right Corner
	Underline	1	1	0	0		
	Below Underline	0	0	1	0		
0100	Above Underline	0	0	1	0		Top Intersect
	Underline	0	0	0	1		
	Below Underline	0	1	0	0		
0101	Above Underline	0	1	0	0		Right Intersect
	Underline	1	1	0	0		
	Below Underline	0	1	0	0		
0110	Above Underline	0	1	0	0		Left Intersect
	Underline	1	0	0	0		
	Below Underline	0	1	0	0		
0111	Above Underline	0	1	0	0		Bottom Intersect
	Underline	0	0	0	1		
	Below Underline	0	0	1	0		
1000	Above Underline	0	0	1	0		Horizontal Line
	Underline	0	0	0	1		
	Below Underline	0	0	1	0		
1001	Above Underline	0	1	0	0		Vertical Line
	Underline	0	1	0	0		
	Below Underline	0	1	0	0		
1010	Above Underline	0	1	0	0		Crossed Lines
	Underline	0	0	0	1		
	Below Underline	0	1	0	0		
1011	Above Underline	0	0	0	0		Not Recommended*
	Underline	0	0	0	0		
	Below Underline	0	0	0	0		
1100	Above Underline	0	0	1	0		Special Codes
	Underline	0	0	1	0		
	Below Underline	0	0	1	0		
1101	Above Underline						Illegal
	Underline		Undefined				
	Below Underline						
1110	Above Underline						Illegal
	Underline		Undefined				
	Below Underline						
1111	Above Underline						Illegal
	Underline		Undefined				
	Below Underline						

*Character Attribute Code 1011 is not recommended for normal operation. Since none of the attribute outputs are active, the character Generator will not be disabled, and an indeterminate character will be generated.

Character Attribute Codes 1101, 1110, and 1111 are illegal.

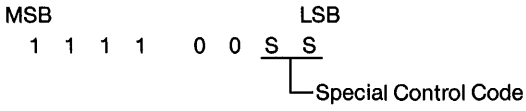
Blinking is active when B = 1.

Highlight is active when H = 1.

Special Codes

Four special codes are available to help reduce memory, software, or DMA overhead.

SPECIAL CONTROL CHARACTER



S	S	FUNCTION
0	0	End of Row
0	1	End of Row-Stop DMA
1	0	End of Screen
1	1	End of Screen-Stop DMA

The End of Row Code (00) activates VSP and holds it to the end of the line.

The End of Row-Stop DMA Code (01) causes the DMA Control Logic to stop DMA for the rest of the row when it is written into the Row Buffer. It affects the display in the same way as the End of Row Code (00).

The End of Screen Code (10) activates VSP and holds it to the end of the frame.

The End of Screen-Stop DMA Code (11) causes the DMA Control Logic to stop DMA for the rest of the frame when it is written into the Row Buffer. It affects the display in the same way as the End of Screen Code (10).

If the Stop DMA feature is not used, all characters after an End of Row character are ignored, except for the End of Screen character, which operates normally. All characters after an End of Screen character are ignored.

NOTE:
If a Stop DMA character is not the last character in a burst or row, DMA is not stopped until after the next character is read. In this situation, a dummy character must be placed in memory after the Stop DMA character.

Field Attributes

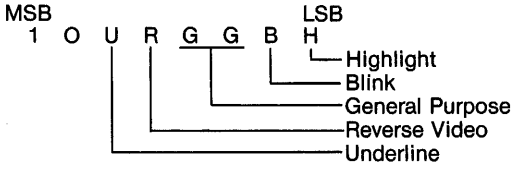
The field attributes are control codes which affect the visual characteristics for a field of characters, starting at the character following the code up to, and including, the character which precedes the *next* field attribute code, or up to the end of the frame. The field attributes are reset during the vertical retrace interval.

There are six field attributes:

1. *Blink* — Characters following the code are caused to blink by activating the Video Suppression output (VSP). The blink frequency is equal to the screen refresh frequency divided by 32.
2. *Highlight* — Characters following the code are caused to be highlighted by activating the Highlight output (HGLT).
3. *Reverse Video* — Characters following the code are caused to appear with reverse video by activating the Reverse Video output (RVV).
4. *Underline* — Characters following the code are caused to be underlined by activating the Light Enable output (LTEN).

5,6. *General Purpose* — There are two additional WD8275 outputs which act as general purpose, independently programmable field attributes. $GPA_{0\text{-}1}$ are active high outputs.

FIELD ATTRIBUTE CODE



H = 1 for highlighting
B = 1 for blinking
R = 1 for reverse video
U = 1 for underline
GG = GPA_1, GPA_0

NOTE:
More than one attribute can be enabled at the same time. If the blinking and reverse video attributes are enabled simultaneously, only the reversed characters will blink.

The WD8275 can be programmed to provide visible or invisible field attribute characters.

If the WD8275 is programmed in the visible field attribute mode, all field attributes will occupy a position on the screen. They will appear as blanks caused by activation of the Video Suppression output (VSP). The chosen visual attributes are activated after this blanked character.

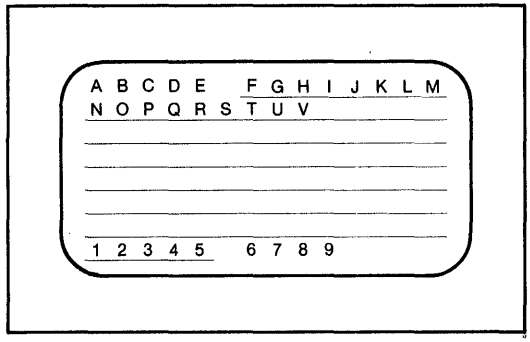


Figure 24.
EXAMPLE OF A VISIBLE FIELD ATTRIBUTE MODE (UNDERLINE ATTRIBUTE)

If the WD8275 is programmed in the invisible field attribute mode, the WD8275 FIFO is activated.

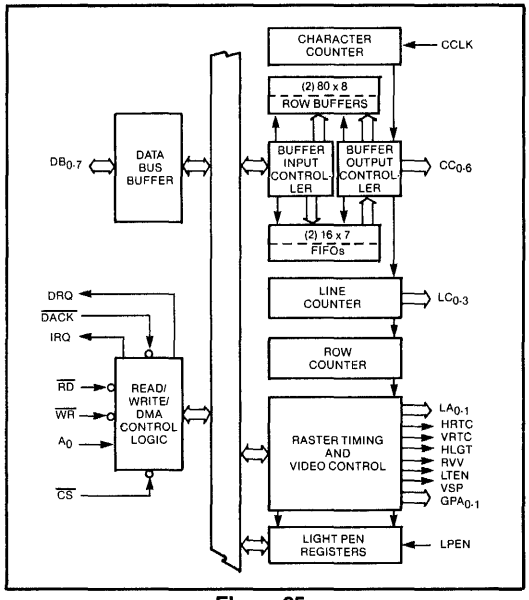


Figure 25.
BLOCK DIAGRAM SHOWING FIFO ACTIVATION

Each row buffer has a corresponding FIFO. These FIFOs are 16 characters by 7 bits in size.

When a field attribute is placed in the row buffer during DMA, the buffer input controller recognizes it and places the *next* character in the proper FIFO.

When a field attribute is placed in the Buffer Output Controller during display, it causes the controller to immediately put a character from the FIFO on the Character Code outputs (CC_{0-6}). The chosen Visual Attributes are also activated.

Since the FIFO is 16 characters long, no more than 16 field attribute characters may be used per line in this mode. If more are used, a bit in the status word is set and the first characters in the FIFO are written over and lost.

NOTE:
Since the FIFO is 7 bits wide, the MSB of any characters put in it are stripped off. Therefore, a Visual Attribute or Special Code must *not* immediately follow a field attribute code. If this situation does occur, the Visual Attribute or Special Code will be treated as a normal display character.

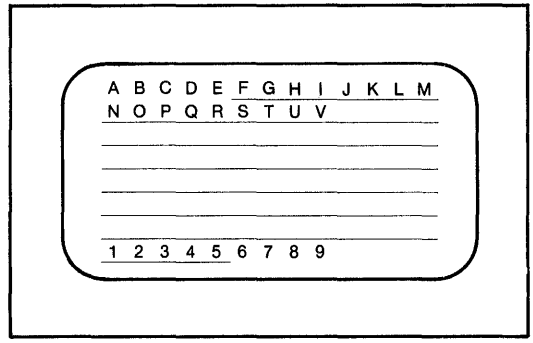


Figure 26.
EXAMPLE OF THE INVISIBLE FIELD ATTRIBUTE MODE (UNDERLINE ATTRIBUTE)

Field and Character Attribute Interaction

Character Attribute Symbols are affected by the Reverse Video (RVV) and General Purpose (GPA_{0-1}) field attributes. They are not affected by Underline, Blink or Highlight field attributes; however, these characteristics can be programmed *individually* for Character Attribute Symbols.

Cursor Timing

The cursor location is determined by a cursor row register and a character position register which are loaded by command to the controller. The cursor can be programmed to appear on the display as:

1. a blinking underline
2. a blinking reverse video block
3. a non-blinking underline
4. a non-blinking reverse video block

The cursor blinking frequency is equal to the screen refresh frequency divided by 16.

If a non-blinking reverse video *cursor* appears in a non-blinking reverse video *field*, the cursor will appear as a normal video block.

If a non-blinking underline *cursor* appears in a non-blinking underline *field*, the cursor will not be visible.

Light Pen Detection

A light pen consists of a micro switch and a tiny light sensor. When the light pen is pressed against the CRT screen, the micro switch enables the light sensor. When the raster sweep reaches the light sensor, it triggers the light pen output.

If the output of the light pen is presented to the WD8275 LPEN input, the row and character position coordinates are stored in a pair of registers. These registers can be read on command. A bit in the status word is set, indicating that the light pen signal was detected. The LPEN input must be a 0 to 1 transition for proper operation.

NOTE:
Due to internal and external delays, the character position coordinate will be off by at least three character positions. This has to be corrected in software.

Device Programming

The WD8275 has two programming registers, the Command Register (CREG) and the Parameter Register (PREG). It also has a Status Register (SREG). The Command Register can only be written into and the Status Registers can only be read from. They are addressed as follows:

A_0	OPERATION	REGISTER
0	Read	PREG
0	Write	PREG
1	Read	SREG
1	Write	CREG

The WD8275 expects to receive a command and a sequence of 0 to 4 parameters, depending on the command. If the proper number of parameter bytes are not received before another command is given, a status flag is set, indicating an improper command.

INSTRUCTION SET

The WD8275 instruction set consists of 8 commands.

COMMAND	NO. OF PARAMETER BYTES
Reset	4
Start Display	0
Stop Display	0
Read Light Pen	2
Load Cursor	2
Enable Interrupt	0
Disable Interrupt	0
Preset Counters	0

In addition, the status of the WD8275 (SREG) can be read by the CPU at any time.

1. Reset Command

	OPERATION	C/P	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Reset Command	0 0 0 0 0 0 0 0
Parameters	Write	0	Screen Comp Byte 1	S H H H H H H H
	Write	0	Screen Comp Byte 2	V V R R R R R R
	Write	0	Screen Comp Byte 3	U U U U L L L L
	Write	0	Screen Comp Byte 4	M F C C Z Z Z Z

Action

After the reset command is written, DMA requests stop, WD8275 interrupts are disabled, and the VSP output is used to blank the screen. HRTC and VRTC continue to run. HRTC and VRTC timing are random on power-up.

As parameters are written, the screen composition is defined.

Parameter—S Spaced Rows

S	FUNCTIONS
0	Normal Rows
1	Spaced Rows

Parameter—HHHHHHH Horizontal Characters/Row

H H H H H H H	NO. OF CHARACTERS PER ROW
0 0 0 0 0 0 0	1
0 0 0 0 0 0 1	2
0 0 0 0 0 1 0	3
.	.
.	.
.	.
1 0 0 1 1 1 1	80
1 0 1 0 0 0 0	Undefined
.	.
.	.
.	.
1 1 1 1 1 1 1	Undefined

Parameter—VV Vertical Retrace Row Count

V	V	NO. OF ROW COUNTS PER VRTC
0	0	1
0	1	2
1	0	3
1	1	4

Parameter—RRRRRR Vertical Rows/Frame

R	R	R	R	R	R	NO. OF ROWS/FRAME
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
			.			.
			.			.
			.			.
1	1	1	1	1	1	64

Parameter—UUUU Underline Placement

U	U	U	U	LINE NO. OF UNDERLINE
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
		.		.
		.		.
		.		.
1	1	1	1	16

Parameter—LLLL
Number of Lines per Character Row

L	L	L	L	NO. OF LINES/ROW
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
		.		.
		.		.
		.		.
1	1	1	1	16

Parameter—M Line Counter Mode

M	LINE COUNTER MODE
0	Mode 0 (Non-Offset)
1	Mode 1 (Offset by 1 Count)

Parameter—F Field Attribute Mode

F	FIELD ATTRIBUTE MODE
0	Transparent
1	Non-Transparent

Parameter—CC Cursor Format

C	C	CURSOR FORMAT
0	0	Blinking reverse video block
0	1	Blinking underline
1	0	Non-blinking reverse video block
1	1	Non-blinking underline

Parameter—ZZZZ Horizontal Retrace Count

Z	Z	Z	Z	NO. OF CHARACTER COUNTS PER HRTC
0	0	0	0	2
0	0	0	1	4
0	0	1	0	6
		.		.
		.		.
		.		.
1	1	1	1	32

NOTE:
uuuu MSB determines blanking of top and bottom lines (1 = blanked, 0 = not blanked).

2. Start Display Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Start Display	0 0 1 S S S B B
No parameters				

SSS Burst Space Code

S	S	S	NO. OF CHARACTER CLOCKS BETWEEN DMA REQUESTS
0	0	0	0
0	0	1	7
0	1	0	15
0	1	1	23
1	0	0	31
1	0	1	39
1	1	0	47
1	1	1	55

BB Burst Count Code

B	B	NO. OF DMA CYCLES PER BURST
0	0	1
0	1	2
1	0	4
1	1	8

Action
WD8275 interrupts are enabled, DMA requests begin, video is enabled, Interrupt Enable and Video Enable Status flags are set.

3. Stop Display Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Start Display	0 1 0 0 0 0 0 0
No parameters				

Action

Disables video, interrupts remain enabled, HRTC and VRTC continue to run, Video Enable status flag is reset, and the "Start Display" command must be given to re-enable the display.

4. Read Light Pen Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Read Light Pen	0 1 1 0 0 0 0 0
Parameters	Read	0	Char. Number	(Char. Position in Row)
	Read	0	Row Number	(Row Number)

Action

The WD8275 is conditioned to supply the contents of the light pen position registers in the next two read cycles of the parameter register. Status flags are not affected.

NOTE:
Software correction of light pen position is required.

5. Load Cursor Position

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Load Cursor	1 0 0 0 0 0 0 0
Parameters	Write	0	Char. Number	(Char. Position in Row)
	Write	0	Row Number	(Row Number)

Action

The WD8275 is conditioned to place the next two parameter bytes into the cursor position registers. Status flags not affected.

6. Enable Interrupt Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Enable Interrupt	1 0 1 0 0 0 0 0
No parameters				

Action

The interrupt enable flag is set and interrupts are enabled.

7. Disable Interrupt Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Disable Interrupt	1 1 0 0 0 0 0 0
No parameters				

Action

Interrupts are disabled and the interrupt enable status flag is reset.

8. Preset Counters Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Preset Counters	1 1 1 0 0 0 0 0
No parameters				

Action

The internal timing counters are preset, corresponding to a screen display position at the top left corner. Two character clocks are required for this operation. The counters will remain in this state until any other command is given.

This command is useful for system debug and synchronization of clustered CRT displays on a single CPU.

STATUS FLAGS

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Read	1	Status Word	0 IE IR LP IC VE OU FO

IE —(Interrupt Enable) Set or reset by command. It enables vertical retrace interrupt. It is automatically set by a "Start Display" command and reset with the "Reset" command.

IR —(Interrupt Request) This flag is set at the beginning of display of the last row of the frame if the interrupt enable flag is set. It is reset after a status read operation.

LP —This flag is set when the light pen input (LPEN) is activated and the light pen registers have been loaded. This flag is automatically reset after a status read.

IC —(Improper Command) This flag is set when a command parameter string is too long or too short. The flag is automatically reset after a status read.

VE —(Video Enable) This flag indicates that video operation of the CRT is enabled. This flag is set on a "Start Display" command, and reset on a "Stop Display" or "Reset" command.

DU —(DMA underrun) This flag is set whenever a data underrun occurs during DMA transfers. Upon detection of DU, the DMA operation is stopped and the screen is blanked until after the vertical retrace interval. This flag is reset after a status read.

FO —(FIFO Overrun) This flag is set whenever the FIFO is overrun. It is reset on a status read.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin
With Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 1 Watt

*NOTICE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Characteristics (T_A = 0°C to 70°C; V_{CC} = 5V ±5%)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0V
I_{CC}	V_{CC} Supply Current		160	mA	

Capacitance (T_A = 25°C; V_{CC} = GND = 0V)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance		10	pF	f_C = 1 MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to V_{SS}.

AC Characteristics (T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%; GND = 0V)

BUS PARAMETERS

Read Cycle

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
t_{AR}	Address Stable Before READ	0		ns	
t_{RA}	Address Hold Time for READ	0		ns	
t_{RR}	READ Pulse Width	250		ns	
t_{RD}	Data Delay from READ		200	ns	C_L = 150pF
t_{DF}	READ to Data Floating	20	100	ns	C_L min. = 20 pF; C_L max. = 150 pF

Write Cycle

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
t_{AW}	Address Stable Before WRITE	0		ns	
t_{WA}	Address Hold Time for WRITE	0		ns	
t_{WW}	WRITE Pulse Width	250		ns	
t_{DW}	Data Setup Time for WRITE	150		ns	
t_{WD}	Data Hold Time for WRITE	0		ns	

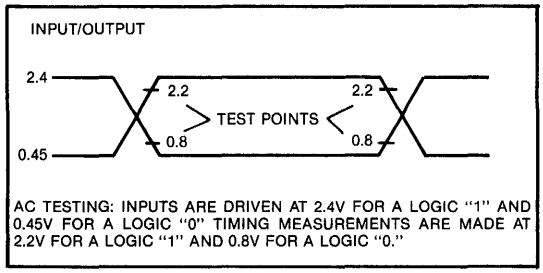
Clock Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
t_{CLK}	Clock Period	480		ns	
t_{KH}	Clock High	240		ns	
t_{KL}	Clock Low	160		ns	
t_{KR}	Clock Rise	5	30	ns	
t_{KF}	Clock Fall	5	30	ns	

Other Timing

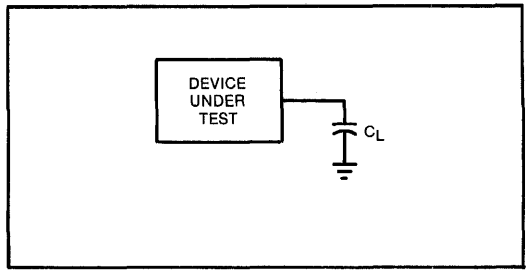
SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
t_{CC}	Character Code Output Delay		150	ns	C_L = 50 pF
t_{HR}	Horizontal Retrace Output Delay		200	ns	C_L = 50 pF
t_{LC}	Line Count Output Delay		400	ns	C_L = 50 pF
t_{AT}	Control/Attribute Output Delay		275	ns	C_L = 50 pF
t_{VR}	Vertical Retrace Output Delay		275	ns	C_L = 50 pF
t_{RI}	INT↓ from RD↑		250	ns	C_L = 50 pF
t_{WQ}	DRQ↑ from WR↑		250	ns	C_L = 50 pF
t_{RQ}	DRQ↓ from WR↓		200	ns	C_L = 50 pF
t_{LR}	DACK↓ to WR↓	0		ns	
t_{RL}	WR↑ to DACK↑	0		ns	
t_{PR}	LPEN Rise		50	ns	
t_{PH}	LPEN Hold	100		ns	

AC Testing Input, Output Wave Form



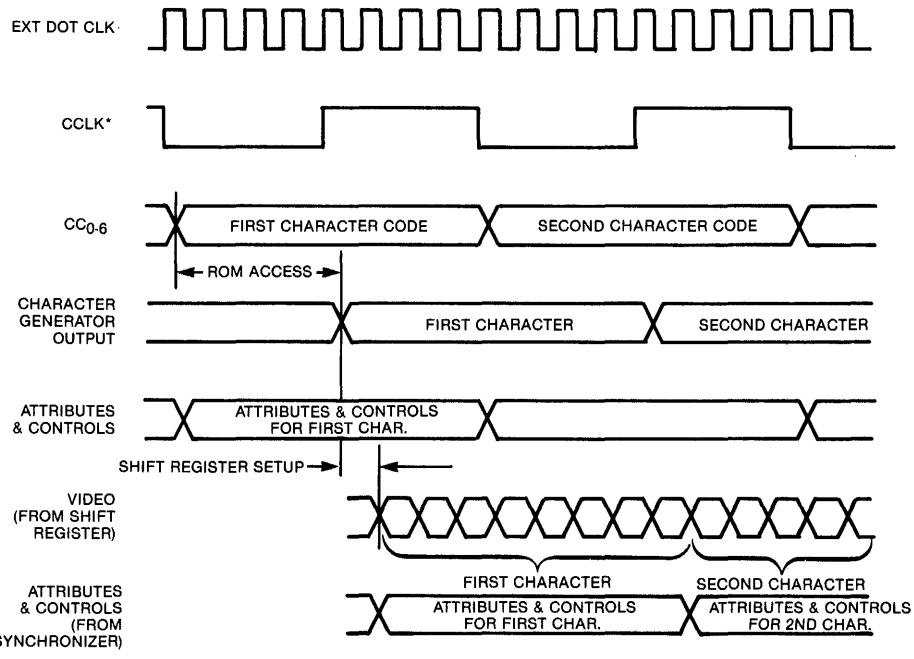
AC TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0" TIMING MEASUREMENTS ARE MADE AT 2.2V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0."

AC Testing Load Circuit



WAVEFORMS

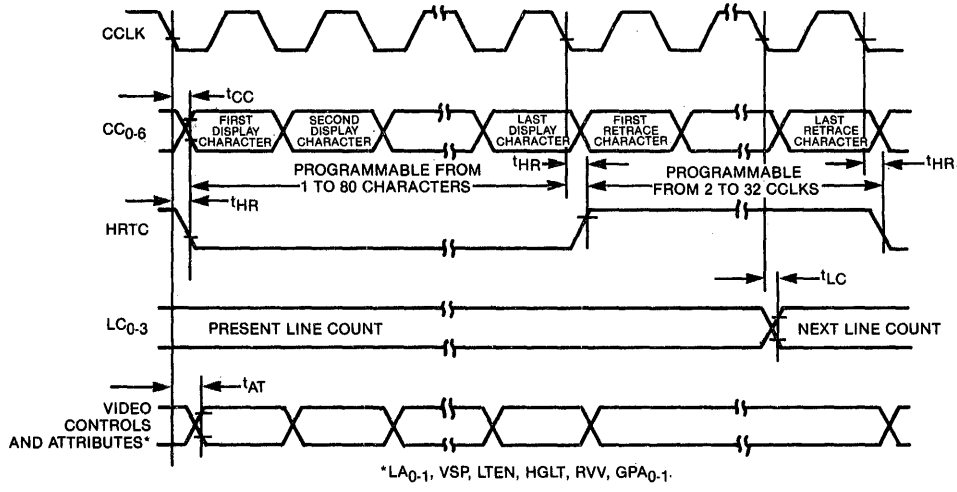
Typical Dot Level Timing



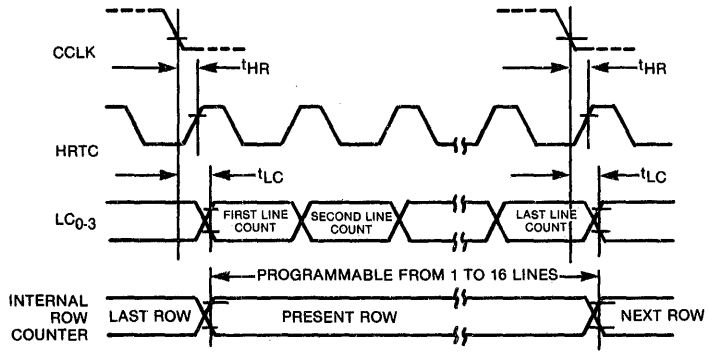
* CCLK IS A MULTIPLE OF THE DOT CLOCK AND AN INPUT TO THE 8275.

WAVEFORMS (Continued)

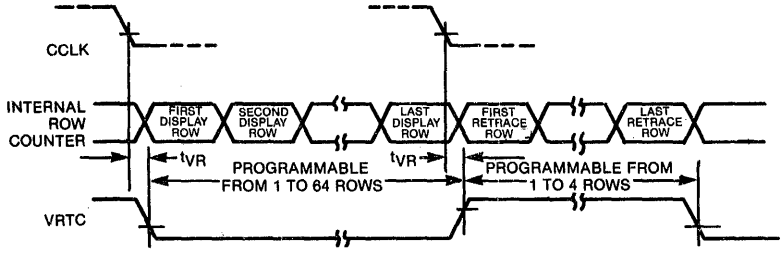
Line Timing



Row Timing

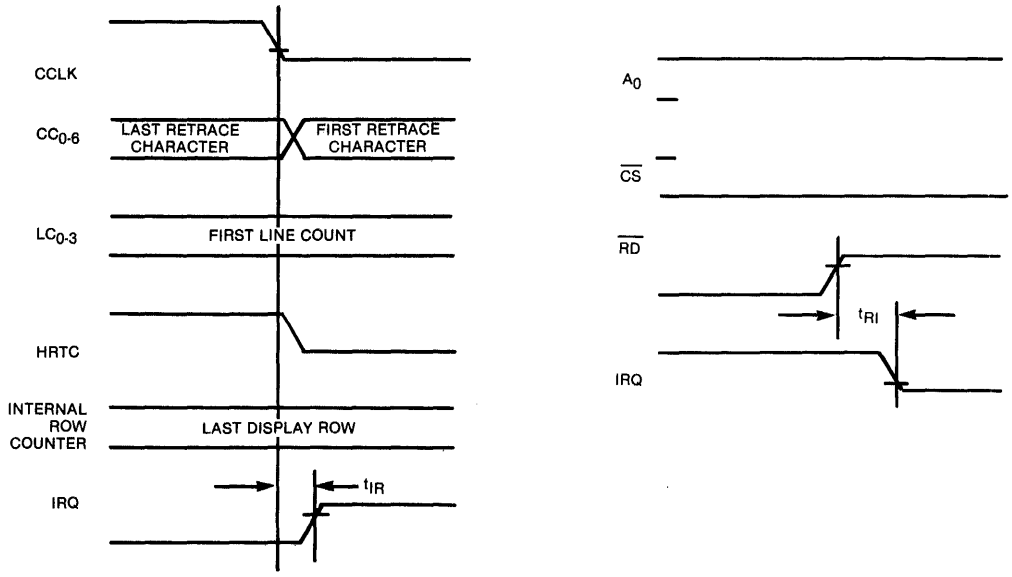


Frame Timing

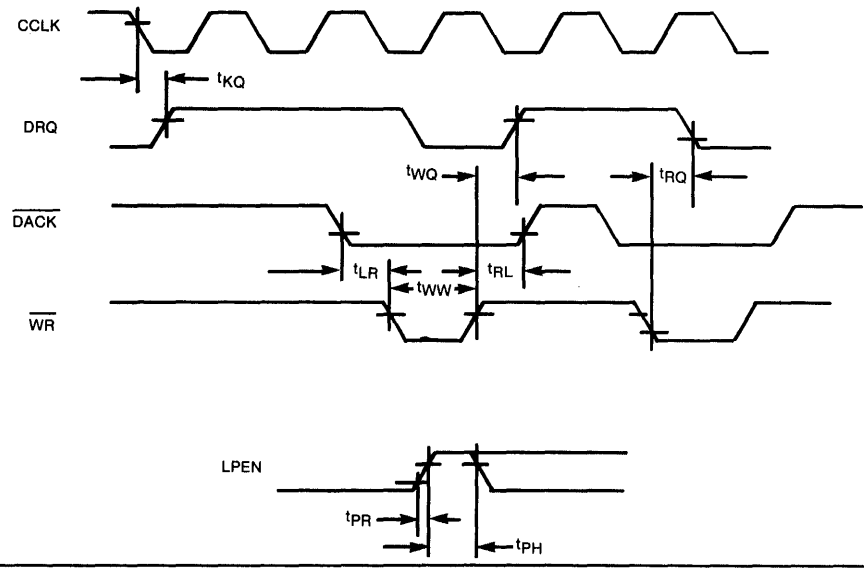


WAVEFORMS (Continued)

Interrupt Timing

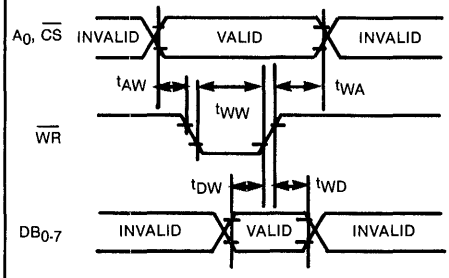


DMA Timing

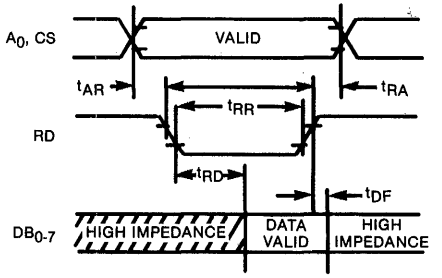


WAVEFORMS (Continued)

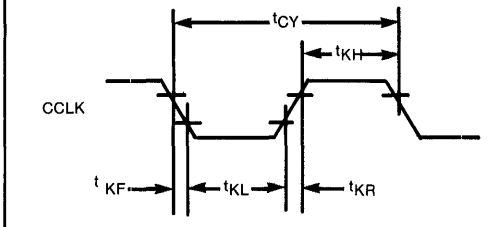
Write Timing



Read Timing



Clock Timing



See page 725 for ordering information.

Printed in U.S.A.

WD8276 Small System CRT Controller

FEATURES

- PROGRAMMABLE SCREEN AND CHARACTER FORMAT
- 6 INDEPENDENT VISUAL FIELD ATTRIBUTES
- CURSOR CONTROL (4 TYPES)
- DUAL ROW BUFFERS
- SINGLE +5V SUPPLY
- 40-PIN PACKAGE

GENERAL DESCRIPTION

The WD8276 Small System CRT Controller is a single chip device intended to interface CRT raster scan displays with Intel microcomputers in minimum device-count systems. Its primary function is to refresh the display by buffering character information from main memory and keeping track of the display position of the screen. The flexibility designed into the WD8276 will allow simple interface to almost any raster scan CRT display with a minimum system IC count.

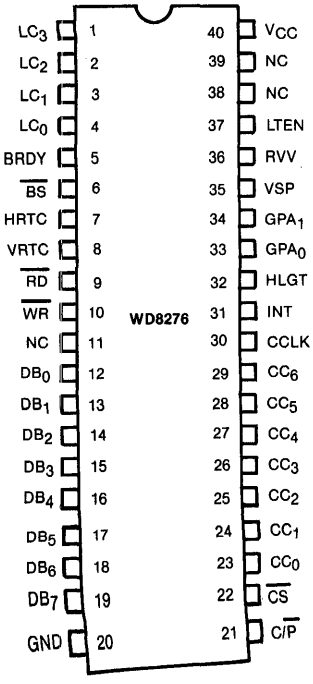


Figure 1. PIN CONFIGURATION

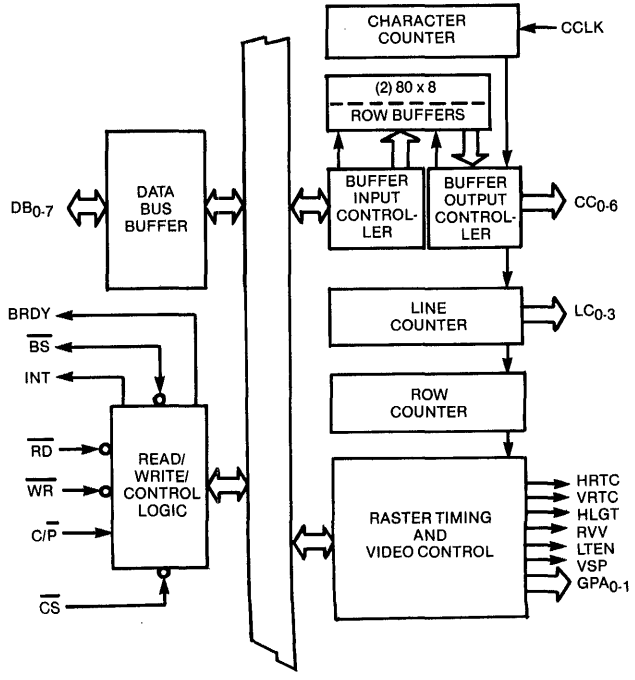


Figure 2. BLOCK DIAGRAM

TABLE 1. PIN DESCRIPTIONS

PIN NO.	TYPE	PIN NAME	SYMBOL	FUNCTION
1 2 3 4	O	LINE COUNT	LC_3 LC_2 LC_1 LC_0	Output from the line counter which is used to address the character generator for the line positions on the screen.
5	O	BUFFER READY	BRDY	Output signal indicating that a Row Buffer is ready for loading of character data.
6	I	BUFFER SELECT	$\overline{BS}$	Input signal enabling $\overline{WR}$ for character data into the Row Buffers.
7	O	HORIZONTAL RETRACE	HRTC	Output signal which is active during the programmed horizontal retrace interval. During this period the VSP output is high and the LTEN output is low.
8	O	VERTICAL RETRACE	VRTC	Output signal which is active during the programmed vertical retrace interval. During this period the VSP output is high and the LTEN output is low.
9	I	READ INPUT	$\overline{RD}$	A control signal to read registers.
10	I	WRITE INPUT	$\overline{WR}$	A control signal to write commands into the control registers or write data into the row buffers.
11		NO CONNECTION	NC	No connection
12 13 14 15 16 17 18 19	I/O	BIDIRECTIONAL DATA BUS	DB_0 DB_1 DB_2 DB_3 DB_4 DB_5 DB_6 DB_7	Three-state lines. The outputs are enabled during a read of the C or P ports.
20		GROUND	Ground	
21	I	PORT ADDRESS	$C/\overline{P}$	A high input on this pin selects the "C" port or command registers and a low input selects the "P" port or parameter registers.
22	I	CHIP SELECT	$\overline{CS}$	Enables $\overline{RD}$ of status or $\overline{WR}$ of command or parameters.
23 24 25 26 27 28 29	O	CHARACTER CODES	CC_0 CC_1 CC_2 CC_3 CC_4 CC_5 CC_6	Output from the row buffers used for character selection in the character generator.
30	I	CHARACTER CLOCK	CCLK	Character clock (from dot/timing logic).
31	O	INTERRUPT OUTPUT	INT	Interrupt output.
32	O	HIGHLIGHT	HLGT	Output signal used to intensify the display at particular positions on the screen as specified by the field attribute codes.
33 34	O	*GENERAL PURPOSE* ATTRIBUTE CODES	GPA_1 GPA_0	*Outputs which are enabled by the general purpose field attribute codes.*

TABLE 1. PIN DESCRIPTIONS

PIN NO.	TYPE	PIN NAME	SYMBOL	FUNCTION
35	O	VIDEO SUPPRESSION	VSP	Output signal used to blank the video signal to the CRT. This output is active: —during the horizontal and vertical retrace intervals. —at the top and bottom lines of rows if underline is programmed to be number 8 or greater. —when an end of row or end of screen code is detected. —when a Row Buffer underrun occurs. —at regular intervals (1/16 frame frequency for cursor, 1/32 frame frequency for attributes) — to create blinking displays as specified by cursor or field attribute programming.
36	O	REVERSE VIDEO	RVV	Output signal used to activate the CRT circuitry to reverse the video signal. This output is active at the cursor position if a reverse video block cursor is programmed or at the positions specified by the field attribute codes.
37	O	LIGHT ENABLE	LTEN	Output signal used to enable the video signal to the CRT. This output is active at the programmed underline cursor position, and at positions specified by attribute codes.
38		NO CONNECTION	NC	No connection.
39		NO CONNECTION	NC	No connection.
40		+5V POWER SUPPLY	V_{CC}	+5V power supply.

FUNCTIONAL DESCRIPTION

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the WD8276 to the system Data Bus.

This functional block accepts inputs from the System Control Bus and generates control signals for overall device operation. It contains the Command, Parameter, and Status Registers that store the various control formats for the device functional definition.

C/P	OPERATION	REGISTER
0	Read	RESERVED
0	Write	PARAMETER
1	Read	STATUS
1	Write	COMMAND

$\overline{RD}$ (READ)

A "low" on this input informs the WD8276 that the CPU is reading status information from the WD8276.

$\overline{WR}$ (WRITE)

A "low" on this input informs the WD8276 that the CPU is writing data or control words to the WD8276.

$\overline{CS}$ (CHIP SELECT)

A "low" on this input selects the WD8276 for $\overline{RD}$ or $\overline{WR}$ of Commands, Status, and Parameters.

BRDY (BUFFER READY)

A "high" on this output indicates that the WD8276 is ready to receive character data.

BS (BUFFER SELECT)

A "low" on this input enables $\overline{WR}$ of character data to the WD8276 row buffers.

INT (INTERRUPT)

A "high" on this output informs the CPU that the WD8276 needs interrupt service.

C/P	RD	WR	CS	BS	
0	0	1	0	1	Reserved
0	1	0	0	1	Write WD8276 Parameter
1	0	1	0	1	Read WD8276 Status
1	1	0	0	1	Write WD8276 Command
X	1	0	1	0	Write WD8276 Row Buffer
X	1	1	X	X	High Impedance
X	X	X	1	1	High Impedance

Character Counter

The Character Counter is a programmable counter that is used to determine the number of characters to be displayed per row and the length of the horizontal retrace interval. It is driven by the CCLK (Character Clock) input, which should be derived from the external dot clock.

Line Counter

The Line Counter is a programmable counter that is used to determine the number of horizontal lines (Raster Scans) per character row. Its outputs are used to address the external character generator.

Row Counter

The Row Counter is a programmable counter that is used to determine the number of character rows to be displayed per frame and length of the vertical retrace interval.

Raster Timing and Video Controls

The Raster Timing circuitry controls the timing of the HRTC (Horizontal Retrace) and VRTC (Vertical Retrace) outputs. The Video Control circuitry controls the generation of HGLT (Highlight), RVV (Reverse Video), LTEN (Light Enable), VSP (Video Suppress), and GPA_{0-1} (General Purpose Attribute) outputs.

Row Buffers

The Row Buffers are two 80-character buffers. They are filled from the microcomputer system memory with the character codes to be displayed. While one row buffer is displaying a row of characters,

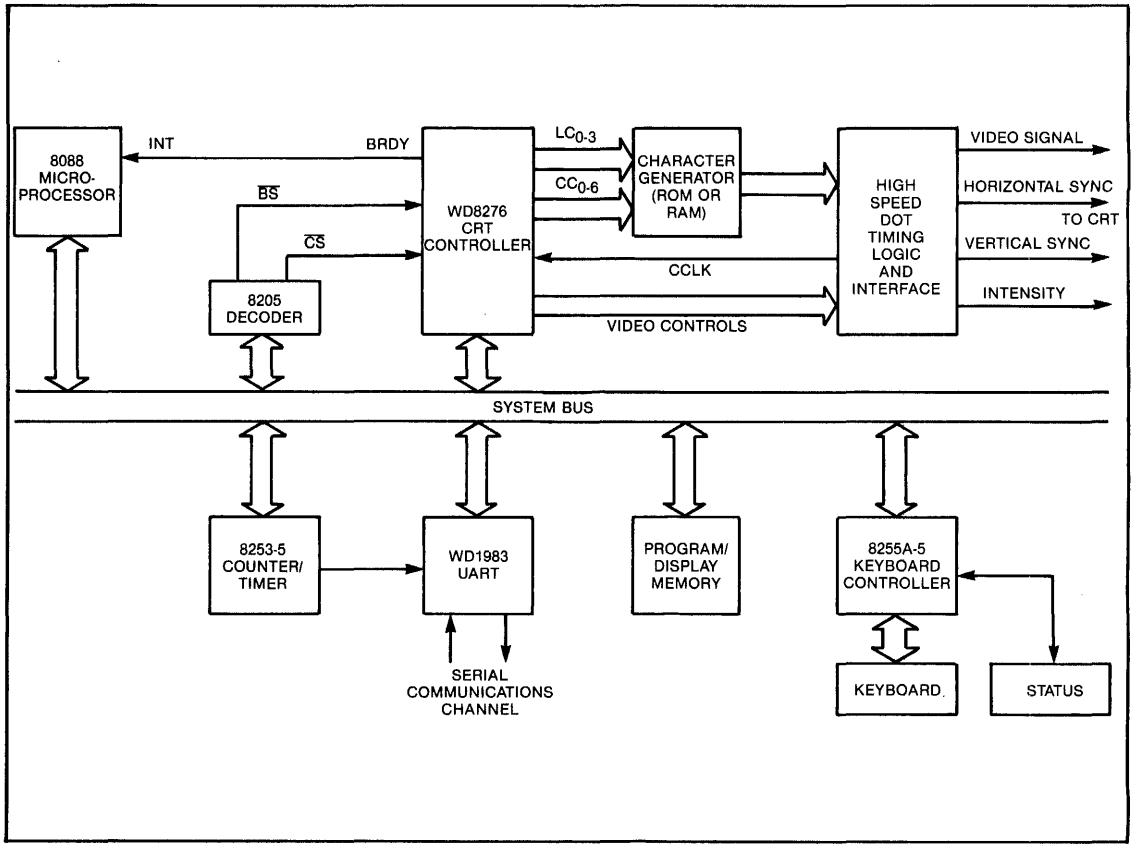


Figure 3. CRT SYSTEM BLOCK DIAGRAM

the other is being filled with the next row of characters.

Buffer Input/Output Controllers

The Buffer Input/Output Controllers decode the characters being placed in the row buffers. If the character is a field attribute or special code, they control the appropriate action. (Example: A "Highlight" field attribute will cause the Buffer Output Controller to activate the HGLT output.)

SYSTEM OPERATION

The WD8276 is programmable to a large number of different display formats. It provides raster timing, display row buffering, visual attribute decoding and cursor timing.

It is designed to interface with standard character generators for dot matrix decoding. Dot level timing must be provided by external circuitry.

GENERAL SYSTEMS OPERATIONAL DESCRIPTION

Display characters are retrieved from memory and displayed on a row-by-row basis. The WD8276 has two row buffers. While one row buffer is being used for display, the other is being filled with the next row of characters to be displayed. The number of display characters per row and the number of character rows per frame are software programmable, providing easy interface to most CRT displays. (See Programming Section.)

The WD8276 uses BRDY to request character data to fill the row buffer that is not being used for display.

The WD8276 displays character rows one scan line at a time. The number of scan lines per character row, the underline position, and blanking of top and bottom lines are programmable. (See Programming Section.)

The WD8276 provides special Control Codes which can be used to minimize overhead. It also provides Visual Attribute Codes to cause special action on the screen without the use of the character generator. (See Visual Attributes Section.)

The WD8276 also controls raster timing. This is done by generating Horizontal Retrace (HRTC) and Vertical Retrace (VRTC) signals. The timing of these signals is also programmable.

The WD8276 can generate a cursor. Cursor location and format are programmable. (See Programming Section.)

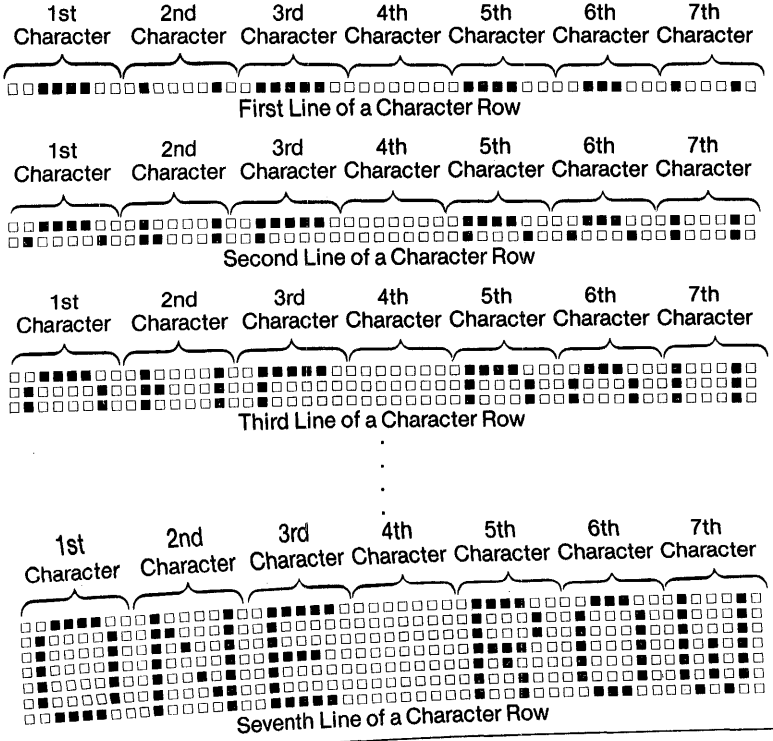


Figure 4. DISPLAY OF A CHARACTER ROW

DISPLAY ROW BUFFERING

Before the start of a frame, the WD8276 uses BRDY and $\overline{BS}$ to fill one row buffer with characters.

When the first horizontal sweep is started, character codes are output to the character generator from the row buffer just filled. Simultaneously, the other row buffer is filled with the next row of characters.

After all the lines of the character row are scanned, the buffers are swapped and the same procedure is followed for the next row.

This process is repeated until all of the character rows are displayed.

Row Buffering allows the CPU access to the display memory at all times except during Buffer Loading (about 25%). This compares favorably to alternative approaches which restrict CPU access to the display memory to occur only during horizontal and vertical retrace intervals (80% of the bus time is used to refresh the display.)

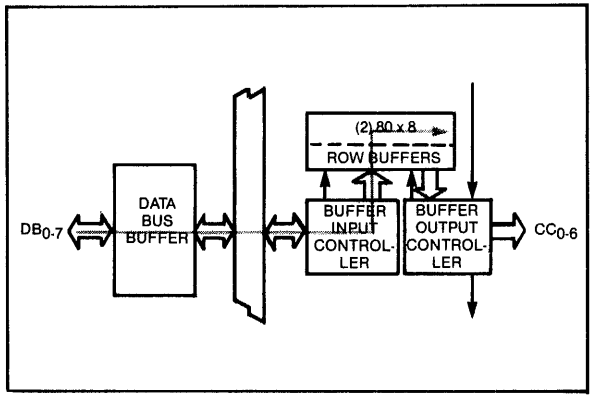


Figure 5. FIRST ROW BUFFER FILLED

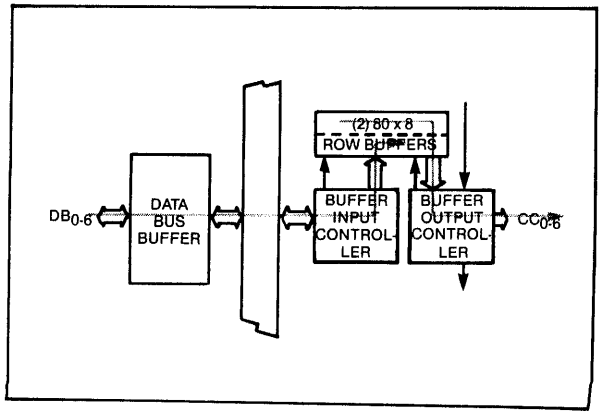


Figure 6.
SECOND ROW BUFFER FILLED, FIRST ROW DISPLAYED

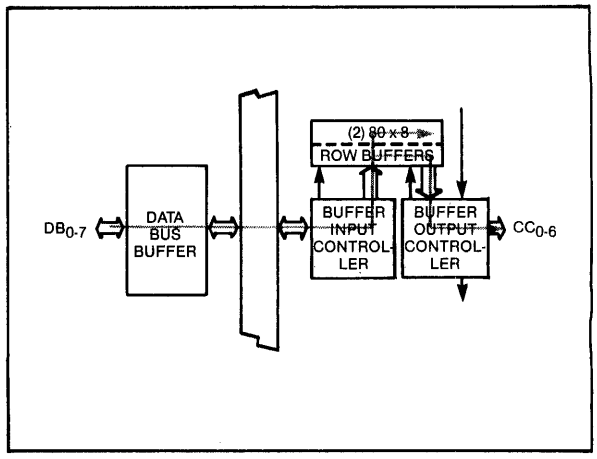


Figure 7.
FIRST ROW BUFFER FILLED WITH THIRD ROW, SECOND ROW DISPLAYED

DISPLAY FORMAT

Screen Format

The WD8276 can be programmed to generate from 1 to 80 characters per row, and from 1 to 64 rows per frame.

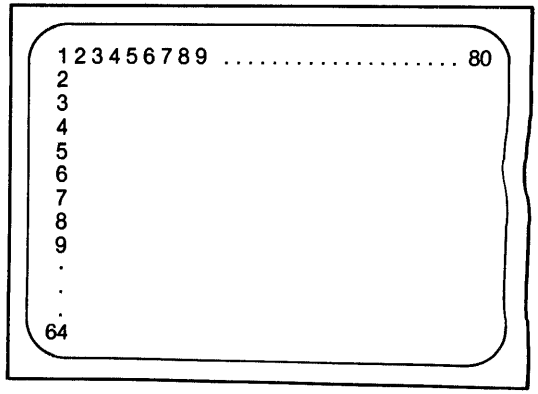


Figure 8.
SCREEN FORMAT

The WD8276 can also be programmed to blank alternate rows. In this mode, the first row is displayed, the second blanked, the third displayed, etc. Display data is not requested for the blanked rows.

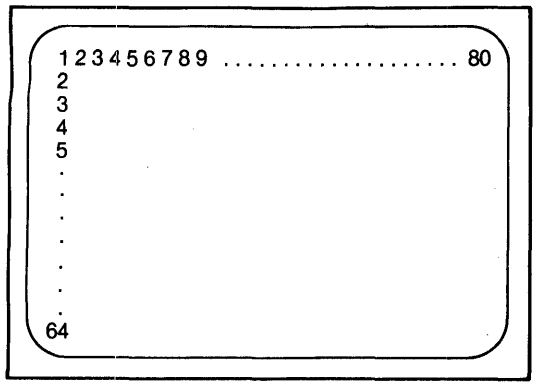


Figure 9.
BLANK ALTERNATE ROWS MODE

Row Format

The WD8276 is designed to hold the line count stable while outputting the appropriate character codes during each horizontal sweep. The line count is incremented during horizontal retrace and the whole row of character codes are output again during the next sweep. This is continued until the entire character row is displayed.

The number of lines (horizontal sweeps) per character row is programmable from 1 to 16.

The output of the line counter can be programmed to be in one of two modes.

In mode 0, the output of the line *counter* is the same as the line *number.*

Line Number	Line Counter Mode 0	Line Counter Mode 1
0	0 0 0 0	1 1 1 1
1	0 0 0 1	0 0 0 0
2	0 0 1 0	0 0 0 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 0 1 1
5	0 1 0 1	0 1 0 0
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 1 0
8	1 0 0 0	0 1 1 1
9	1 0 0 1	1 0 0 0
10	1 0 1 0	1 0 0 1
11	1 0 1 1	1 0 1 0
12	1 1 0 0	1 0 1 1
13	1 1 0 1	1 1 0 0
14	1 1 1 0	1 1 0 1
15	1 1 1 1	1 1 1 0

Figure 10.
EXAMPLE OF A 16-LINE FORMAT

In mode 1, the line *counter* is offset by one from the line *number.*

NOTE:
In mode 1, while the *first* line (line number 0) is being displayed, the *last* count is output by the line counter (see examples).

Line Number	Line Counter Mode 0	Line Counter Mode 1
0	0 0 0 0	1 0 0 1
1	0 0 0 1	0 0 0 0
2	0 0 1 0	0 0 0 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 0 1 1
5	0 1 0 1	0 1 0 0
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 1 0
8	1 0 0 0	0 1 1 1
9	1 0 0 1	1 0 0 0

Figure 11.
EXAMPLE OF A 10-LINE FORMAT

Mode 0 is useful for character generators that leave address zero blank and start at address 1. Mode 1 is useful for character generators which start at address zero.

Underline placement is also programmable (from line *number* 0 to 15). This is independent of the line *counter* mode.

If the line *number* of the underline is greater than 7 (line *number* MSB = 1), then the top and bottom lines will be blanked.

Line Number	Line Counter Mode 0	Line Counter Mode 1
0	0 0 0 0	1 0 1 1
1	0 0 0 1	0 0 0 0
2	0 0 1 0	0 0 0 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 0 1 1
5	0 1 0 1	0 1 0 0
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 1 0
8	1 0 0 0	0 1 1 1
9	1 0 0 1	1 0 0 0
10	1 0 1 0	1 0 0 1
11	1 0 1 1	1 0 1 0

Top and Bottom Lines are Blanked

Figure 12.
UNDERLINE IN LINE NUMBER 10

If the line *number* of the underline is less than or equal to 7 (line *number* MSB = 0), then the top and bottom lines will *not* be blanked.

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ □ □ □ □	0 0 0 0	0 1 1 1
1	□ □ □ ■ □ □ □	0 0 0 1	0 0 0 0
2	□ □ ■ □ ■ □ □	0 0 1 0	0 0 0 1
3	□ ■ □ □ □ ■ □	0 0 1 1	0 0 1 0
4	□ ■ □ □ □ ■ □	0 1 0 0	0 0 1 1
5	□ ■ ■ ■ ■ ■ □	0 1 0 1	0 1 0 0
6	□ ■ □ □ □ ■ □	0 1 1 0	0 1 0 1
7	■ ■ ■ ■ ■ ■ ■	0 1 1 1	0 1 1 0

Top and Bottom Lines are not Blanked

Figure 13.
UNDERLINE IN LINE NUMBER 7

If the line *number* of the underline is greater than the maximum number of lines, the underline will not appear.

Blanking is accomplished by the VSP (Video Suppression) signal. Underline is accomplished by the LTEN (Light Enable) signal.

Dot Format

Dot width and character width are dependent upon the external timing and control circuitry.

Dot level timing circuitry should be designed to accept the parallel output of the character generator and shift it out serially at the rate required by the CRT display.

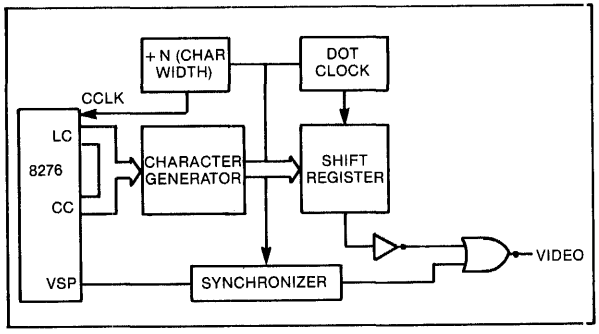


Figure 14.
TYPICAL DOT LEVEL BLOCK DIAGRAM

Dot width is a function of dot clock frequency.

Character width is a function of the character generator width.

Horizontal character spacing is a function of the shift register length.

NOTE:
Video control and timing signals must be synchronized with the video signal due to the character generator access delay.

RASTER TIMING

The character counter is driven by the character clock input (CCLK). It counts out the characters being displayed (programmable from 1 to 80). It then causes the line counter to increment, and it starts counting out the horizontal retrace interval (programmable from 2 to 32). This process is constantly repeated.

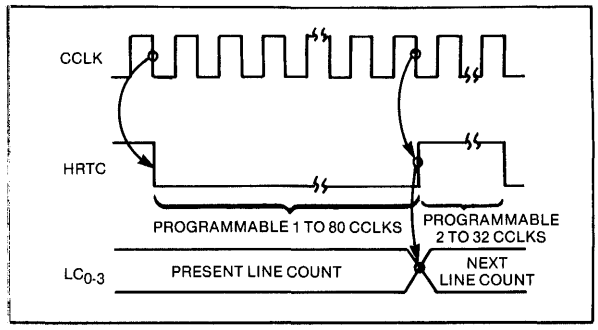


Figure 15.
LINE TIMING

The line counter is driven by the character counter. It is used to generate the line address outputs (LC_{0-3}) for the character generator. After it counts all of the lines in a character row (programmable from 1 to 16), it increments the row counter, and starts over again. (See Character Format Section for detailed description of Line Counter functions.)

The row counter is an internal counter driven by the line counter. It controls the functions of the row buffers and counts the number of character rows displayed.

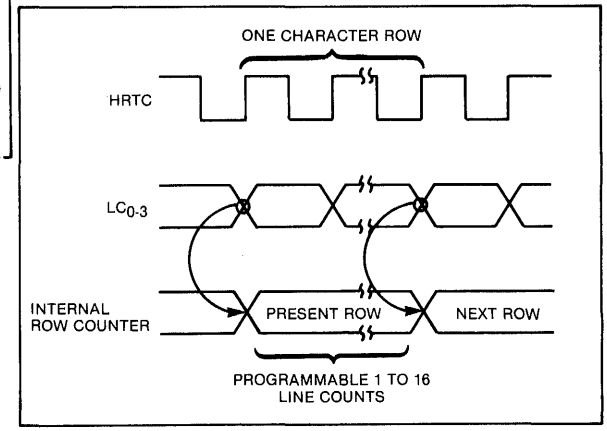


Figure 16.
ROW TIMING

After the row counter counts all of the rows in a frame (programmable from 1 to 64), it starts counting out the vertical retrace interval (programmable from 1 to 4).

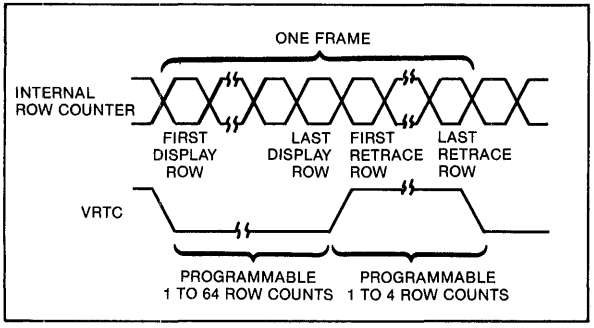


Figure 17.
FRAME TIMING

The Video Suppression Output (VSP) is active during horizontal and vertical retrace intervals.

Dot level timing circuitry must synchronize these outputs with the video signal to the CRT Display.

INTERRUPT TIMING

The WD8276 can be programmed to generate an interrupt request at the end of each frame. If the WD8276 interrupt enable flag is set, an interrupt request will occur at the *beginning* of the *last display row.*

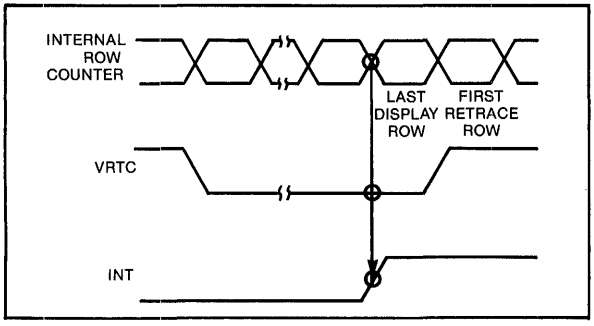


Figure 18.
BEGINNING OF INTERRUPT

INT will go inactive after the status register is read.

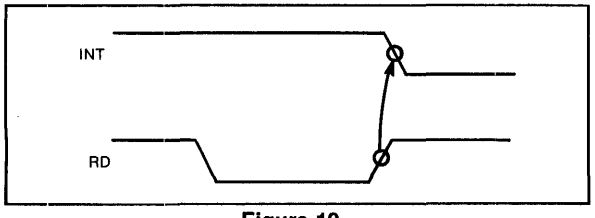


Figure 19.
END OF INTERRUPT

A reset command will also cause INT to go inactive, but this is not recommended during normal service.

NOTE:
Upon power-up, the WD8276 Interrupt Enable Flag may be set. As a result, the user's cold start routine should write a reset command to the WD8276 before system interrupts are enabled.

VISUAL ATTRIBUTES AND SPECIAL CODES

The characters processed by the WD8276 are 8-bit quantities. The character code outputs provide the character generator with 7 bits of address. The Most Significant Bit is the extra bit and it is used to determine if it is a normal display character (MSB = 0), or if it is a Field Attribute or Special Code (MSB = 1).

Special Codes

Four special codes are available to help reduce bus usage.

SPECIAL CONTROL CHARACTER

MSB LSB

1 1 1 1 0 0 S S

└ Special Control Code

S	S	FUNCTION
0	0	End of Row
0	1	End of Row-Stop Buffer Loading
1	0	End of Screen
1	1	End of Screen-Stop Buffer Loading

The End of Row Code (00) activates VSP and holds it to the end of the line.

The End of Row-Stop Buffer Loading (BRDY) Code (01) causes the Buffer Loading Control Logic to stop buffer loading for the rest of the row upon being written into the Row Buffer. It affects the display in the same way as the End of Row Code (00).

The End of Screen Code (10) activates VSP and holds it to the end of the frame.

The End of Screen-Stop Buffer Loading (BRDY) Code (11) causes the Row Buffer Control Logic to stop buffer loading for the rest of the frame upon being written. It affects the display in the same way as the End of Screen Code (10).

If the Stop Buffer Loading feature is not used, all characters after an End of Row character are ignored, except for the End of Screen character, which operates normally. All characters after an End of Screen character are ignored.

NOTE:
If a Stop Buffer Loading is not the last character in a row, Buffer Loading is not stopped until after the next character is read. In this situation, a dummy character must be placed in memory after the Stop Buffer Loading character.

Field Attributes

The field attributes are control codes which affect the visual characteristics for a field of characters, starting at the character following the code up to, and including, the character which precedes the *next* field attribute code, or up to the end of the frame. The field attributes are reset during the vertical retrace interval.

The WD8276 can be programmed to provide visible field attribute characters; all field attribute codes will occupy a position on the screen. These codes will appear as blanks caused by activation of the Video Suppression output (VSP). The chosen visual attributes are activated after this blanked character.

There are six field attributes:

1. *Blink* — Characters following the code are caused to blink by activating the Video Suppression output (VSP). The blink frequency is equal to the screen refresh frequency divided by 32.
2. *Highlight* — Characters following the code are caused to be highlighted by activating the Highlight output (HGLT).
3. *Reverse Video* — Characters following the code are caused to appear with reverse video by activating the Reverse Video output (RVV).
4. *Underline* — Characters following the code are caused to be underlined by activating the Light Enable output (LTEN).

5,6. *General Purpose* — There are two additional WD8276 outputs which act as general purpose, independently programmable field attributes. GPA_{0-1} are active high outputs.

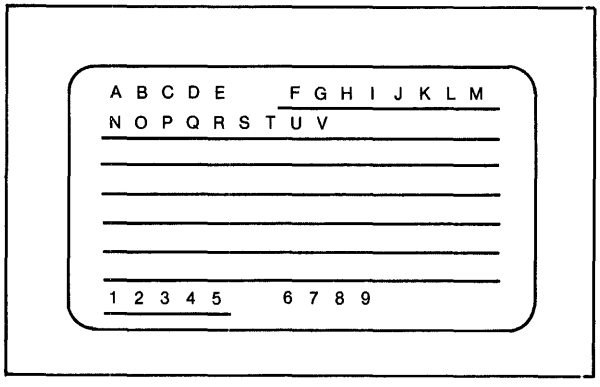
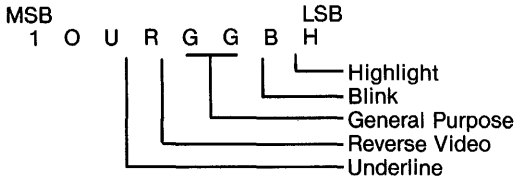


Figure 20.
EXAMPLE OF A VISIBLE FIELD ATTRIBUTE (UNDERLINE ATTRIBUTE)

FIELD ATTRIBUTE CODE



H = 1 for highlighting
B = 1 for blinking
R = 1 for reverse video
U = 1 for underline
GG = GPA_1, GPA_0

NOTE:
More than one attribute can be enabled at the same time. If the blinking and reverse video attributes are enabled simultaneously, only the reversed characters will blink.

Cursor Timing

The cursor location is determined by a cursor row register and a character position register which are loaded by command to the controller. The cursor can be programmed to appear on the display as:

1. a blinking underline
2. a blinking reverse video block
3. a non-blinking underline
4. a non-blinking reverse video block

The cursor blinking frequency is equal to the screen refresh frequency divided by 16.

If a non-blinking reverse video *cursor* appears in a non-blinking reverse video *field*, the cursor will appear as a normal video block.

If a non-blinking underline *cursor* appears in a non-blinking underline *field*, the cursor will not be visible.

Device Programming

The WD8276 has two programming registers, the Command Register and the Parameter Register. It also has a Status Register. The Command Register can only be written into and the Status Register can only be read from. They are addressed as follows:

C/$\overline{P}$	OPERATION	REGISTER
0	Read	Reserved
0	Write	Parameter
1	Read	Status
1	Write	Command

The WD8276 expects to receive a command and a sequence of 0 to 4 parameters, depending on the command. If the proper number of parameter bytes are not received before another command is given, a status flag is set, indicating an improper command.

INSTRUCTION SET

The WD8276 instruction set consists of 7 commands.

In addition, the status of the WD8276 can be read by the CPU at any time.

COMMAND	NO. OF PARAMETER BYTES
Reset	4
Start Display	0
Stop Display	0
Load Cursor	2
Enable Interrupt	0
Disable Interrupt	0
Preset Counters	0

1. Reset Command

	OPERATION	C/P	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Reset Command	0 0 0 0 0 0 0 0
Parameters	Write	0	Screen Comp Byte 1	S H H H H H H H
	Write	0	Screen Comp Byte 2	V V R R R R R R
	Write	0	Screen Comp Byte 3	U U U U L L L L
	Write	0	Screen Comp Byte 4	M 1 C C Z Z Z Z

Action

After the reset command is written, BRDY goes inactive, WD8276 interrupts are disabled, and the VSP output is used to blank the screen. HRTC and VRTC continue to run. HRTC and VRTC timing are random on power-up.

As parameters are written, the screen composition is defined.

Parameter—S Spaced Rows

S	FUNCTIONS
0	Normal Rows
1	Spaced Rows

Parameter—HHHHHHH Horizontal Characters/Row

H H H H H H H	NO. OF CHARACTERS PER ROW
0 0 0 0 0 0 0	1
0 0 0 0 0 0 1	2
0 0 0 0 0 1 0	3
.	.
.	.
.	.
1 0 0 1 1 1 1	80
1 0 1 0 0 0 0	Undefined
.	.
.	.
.	.
1 1 1 1 1 1 1	Undefined

Parameter—VV Vertical Retrace Row Count

V V	NO. OF ROW COUNTS PER VRTC
0 0	1
0 1	2
1 0	3
1 1	4

Parameter—RRRRRR Vertical Rows/Frame

R R R R R R	NO. OF ROWS/FRAME
0 0 0 0 0 0	1
0 0 0 0 0 1	2
0 0 0 0 1 0	3
.	.
.	.
.	.
1 1 1 1 1 1	64

Parameter—UUUU Underline Placement

U U U U	LINE NO. OF UNDERLINE
0 0 0 0	1
0 0 0 1	2
0 0 1 0	3
.	.
.	.
.	.
1 1 1 1	16

Parameter—LLLL
Number of Lines per Character Row

L L L L	NO. OF LINES/ROW
0 0 0 0	1
0 0 0 1	2
0 0 1 0	3
.	.
.	.
.	.
1 1 1 1	16

Parameter—M Line Counter Mode

M	LINE COUNTER MODE
0	Mode 0 (Non-Offset)
1	Mode 1 (Offset by 1 Count)

Parameter—CC Cursor Format

C	C	CURSOR FORMAT
0	0	Blinking reverse video block
0	1	Blinking underline
1	0	Non-blinking reverse video block
1	1	Non-blinking underline

NOTE:
uuuu MSB determines blanking of top and bottom lines (1 = blanked, 0 = not blanked).

Parameter—ZZZZ Horizontal Retrace Count

Z	Z	Z	Z	NO. OF CHARACTER COUNTS PER HRTC
0	0	0	0	2
0	0	0	1	4
0	0	1	0	6
		.		.
		.		.
		.		.
1	1	1	1	32

2. Start Display Command

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Start Display	0 0 1 0 0 0 0 0
No parameters				

Action

WD8276 interrupts are enabled, BRDY goes active, video is enabled, Interrupt Enable and Video Enable status flags are set.

3. Stop Display Command

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Start Display	0 1 0 0 0 0 0 0
No parameters				

Action

Disables video, interrupts remain enabled, HRTC and VRTC continue to run, Video Enable status flag is reset, and the "Start Display" command must be given to reenable the display.

4. Load Cursor Position

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Load Cursor	1 0 0 0 0 0 0 0
Parameters	Write	0	Char. Number	(Char. Position in Row)
	Write	0	Row Number	(Row Number)

Action

The WD8276 is conditioned to place the next two parameter bytes into the cursor position registers. Status flag not affected.

5. Enable Interrupt Command

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Enable Interrupt	1 0 1 0 0 0 0 0
No parameters				

Action

The interrupt enable flag is set and interrupts are enabled.

6. Disable Interrupt Command

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Disable Interrupt	1 1 0 0 0 0 0 0
No parameters				

Action

Interrupts are disabled and the interrupt enable status flag is reset.

7. Preset Counters Command

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Preset Counters	1 1 1 0 0 0 0 0
No parameters				

Action

The internal timing counters are preset, corresponding to a screen display position at the top left corner. Two character clocks are required for this operation. The counters will remain in this state until any other command is given.

This command is useful for system debug and synchronization of clustered CRT displays on a single CPU.

STATUS FLAGS

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Read	1	Status Word	0 IE IR X IC VE BU X

IE —(Interrupt Enable) Set or reset by command. It enables vertical retrace interrupt. It is automatically set by a "Start Display" command and reset with the "Reset" command.

IR —(Interrupt Request) This flag is set at the beginning of display of the last row of the frame if the interrupt enable flag is set. It is reset after a status read operation.

IC —(Improper Command) This flag is set when a command parameter string is too long or too short. The flag is automatically reset after a status read.

VE —(Video Enable) This flag indicates that video operation of the CRT is enabled. This flag is set on a "Start Display" command, and reset on a "Stop Display" or "Reset" command.

BU —(Buffer Underrun) This flag is set whenever a Row Buffer is not filled with character data in time for a buffer swap required by the display. Upon activation of this bit, buffer loading ceases, and the screen is blanked until after the vertical retrace interval.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin
With Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 1 Watt

*NOTICE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Characteristics (T_A = 0°C to 70°C; V_{CC} = 5V ±5%)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0.45V
I_{CC}	V_{CC} Supply Current		160	mA	

Capacitance (T_A = 25°C; V_{CC} = GND = 0V)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance		10	pF	f_C = 1 MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to V_{SS}

AC Characteristics (T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%; GND = 0V)

BUS PARAMETERS (Note 1)

Read Cycle

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
t_{AR}	Address Stable Before READ	0		ns	
t_{RA}	Address Hold Time for READ	0		ns	
t_{RR}	READ Pulse Width	250		ns	
t_{RD}	Data Delay from READ		200	ns	C_L = 150pF
t_{DF}	READ to Data Floating	20	100	ns	

Write Cycle

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
t_{AW}	Address Stable Before WRITE	0		ns	
t_{WA}	Address Hold Time for WRITE	0		ns	
t_{WW}	WRITE Pulse Width	250		ns	
t_{DW}	Data Setup Time for WRITE	150		ns	
t_{WD}	Data Hold Time for WRITE	0		ns	

Clock Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
t_{CLK}	Clock Period	480		ns	
t_{KH}	Clock High	240		ns	
t_{KL}	Clock Low	160		ns	
t_{KR}	Clock Rise	5	30	ns	
t_{KF}	Clock Fall	5	30	ns	

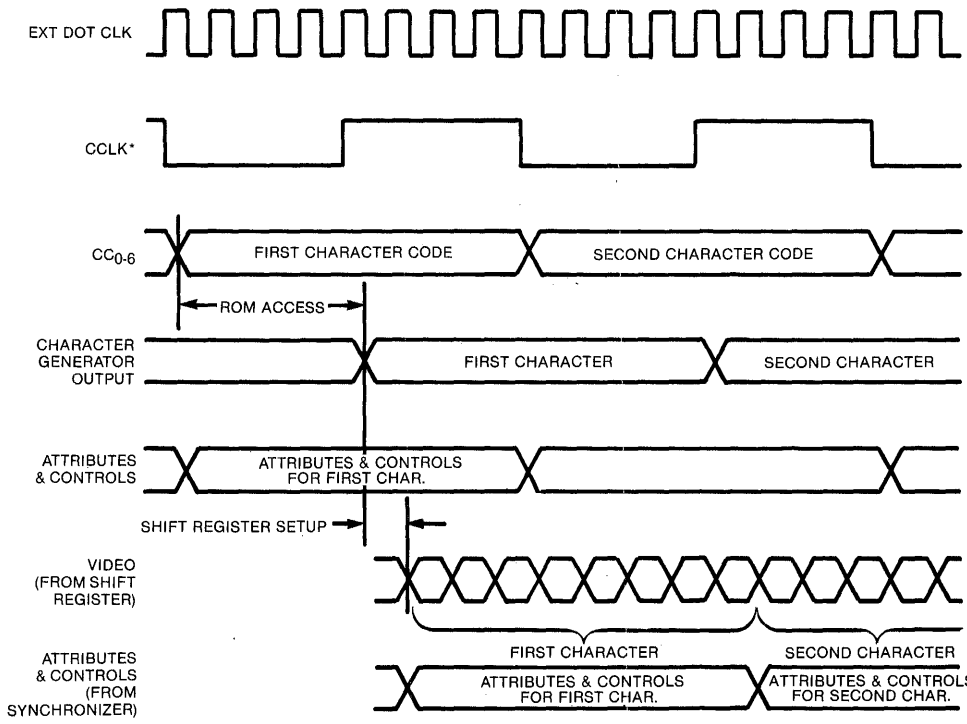
NOTE 1: AC timings measured at V_{OH} = 2.0, V_{OL} = 0.8, V_{IH} = 2.4 V_{IL} = 0.45.

Other Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
t_{CC}	Character Code Output Delay		150	ns	C_L = 50 pF
t_{HR}	Horizontal Retrace Output Delay		200	ns	C_L = 50 pF
t_{LC}	Line Count Output Delay		400	ns	C_L = 50 pF
t_{AT}	Control/Attribute Output Delay		275	ns	C_L = 50 pF
t_{VR}	Vertical Retrace Output Delay		275	ns	C_L = 50 pF
t_{RI}	INT↓ from $\overline{RD}$↑		250	ns	C_L = 50 pF
t_{WQ}	BRDY↑ from $\overline{WR}$↑		250	ns	C_L = 50 pF
t_{RQ}	BRDY↓ from $\overline{WR}$↓		200	ns	C_L = 50 pF
t_{LR}	$\overline{BS}$↓ to $\overline{WR}$↓	0		ns	
t_{RL}	$\overline{WR}$↑ to $\overline{BS}$↑	0		ns	

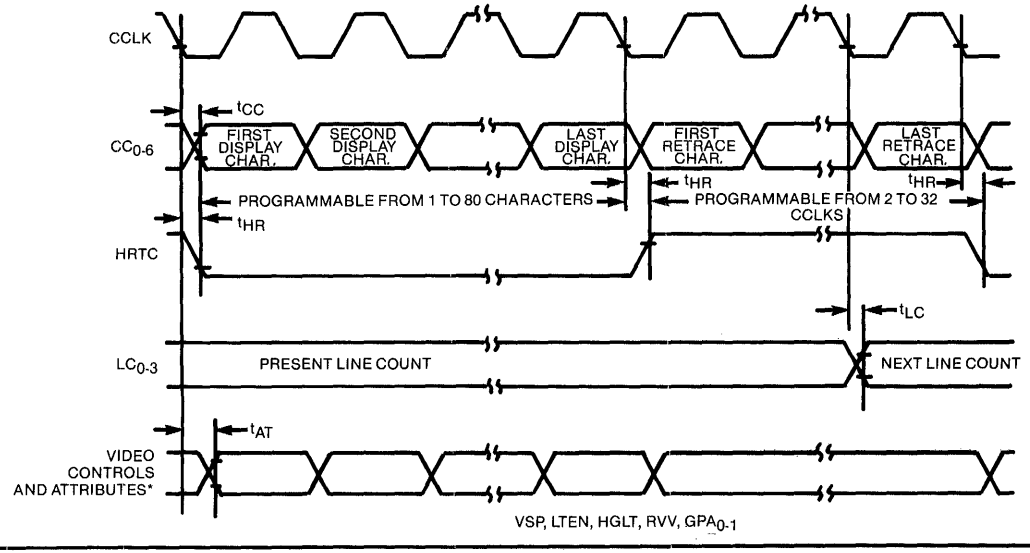
WAVEFORMS

Typical Dot Level Timing

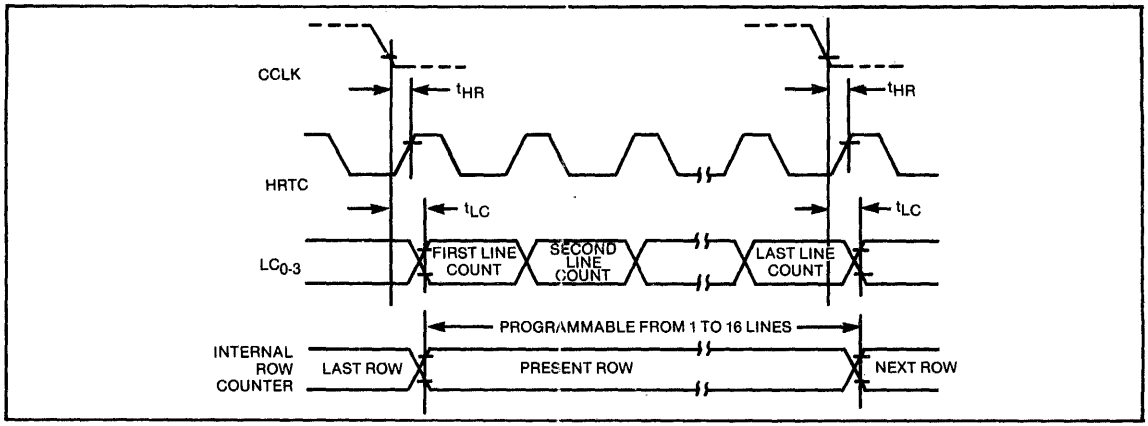


* CCLK IS A MULTIPLE OF THE DOT CLOCK AND AN INPUT TO THE 8276.

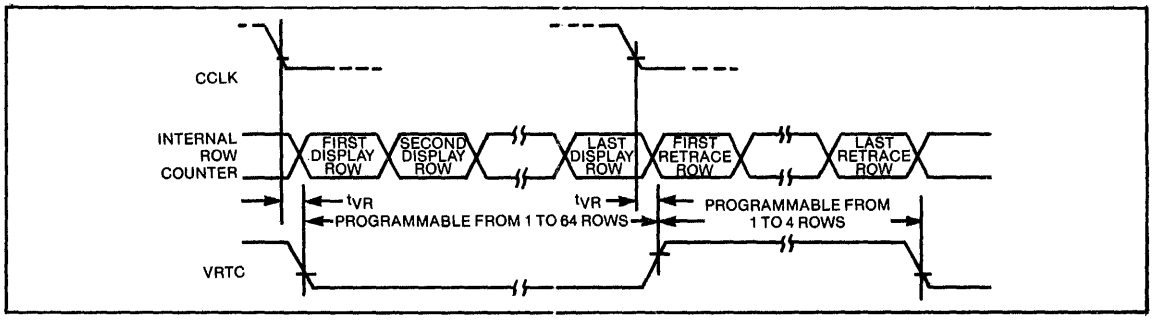
Line Timing



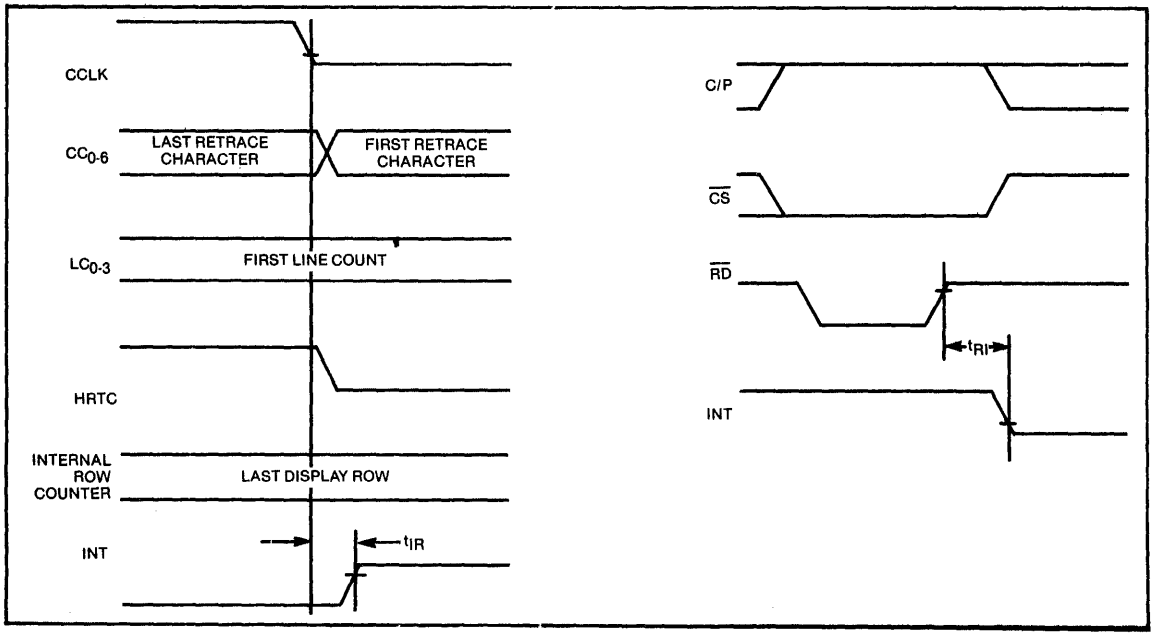
Row Timing



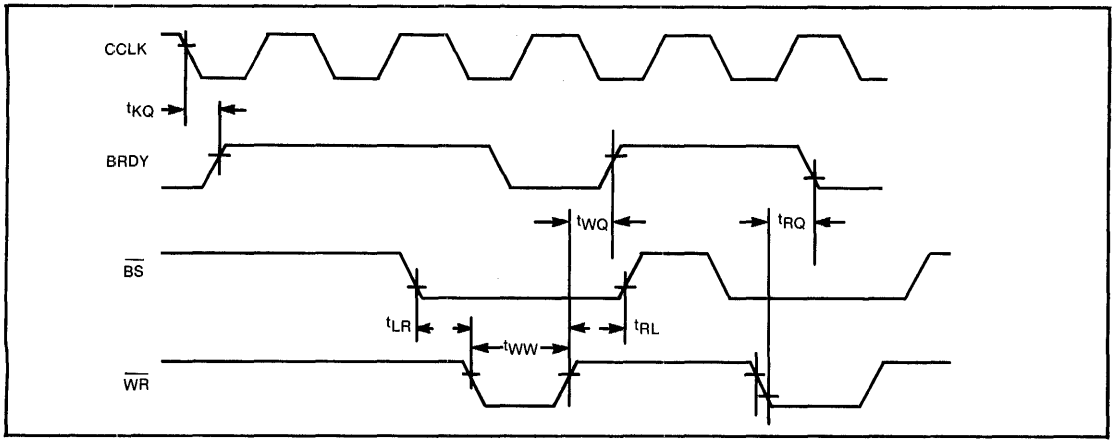
Frame Timing



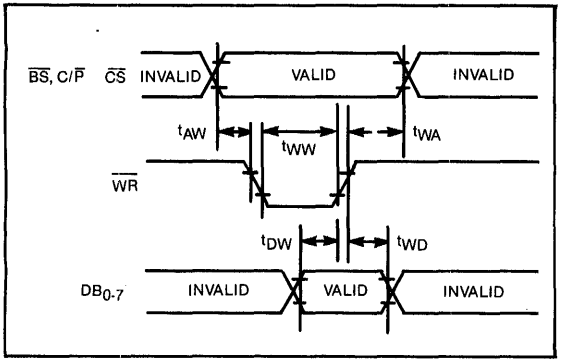
Interrupt Timing



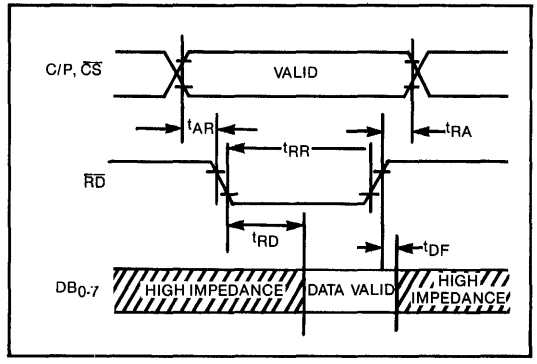
Timing for Buffer Loading



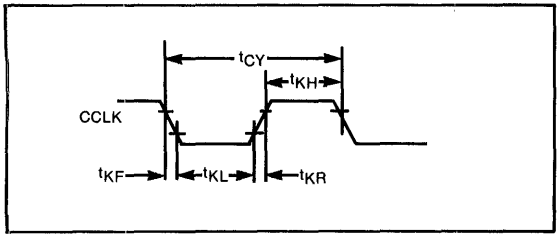
Write Timing



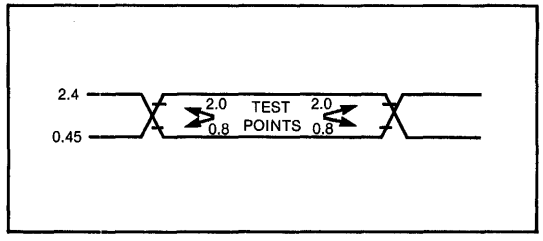
Read Timing



Clock Timing



Input and Output Waveforms for A.C. Tests



FOR A.C. TESTING, INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0." TIMING MEASUREMENTS FOR INPUT AND OUTPUT SIGNALS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0."

See page 725 for ordering information.

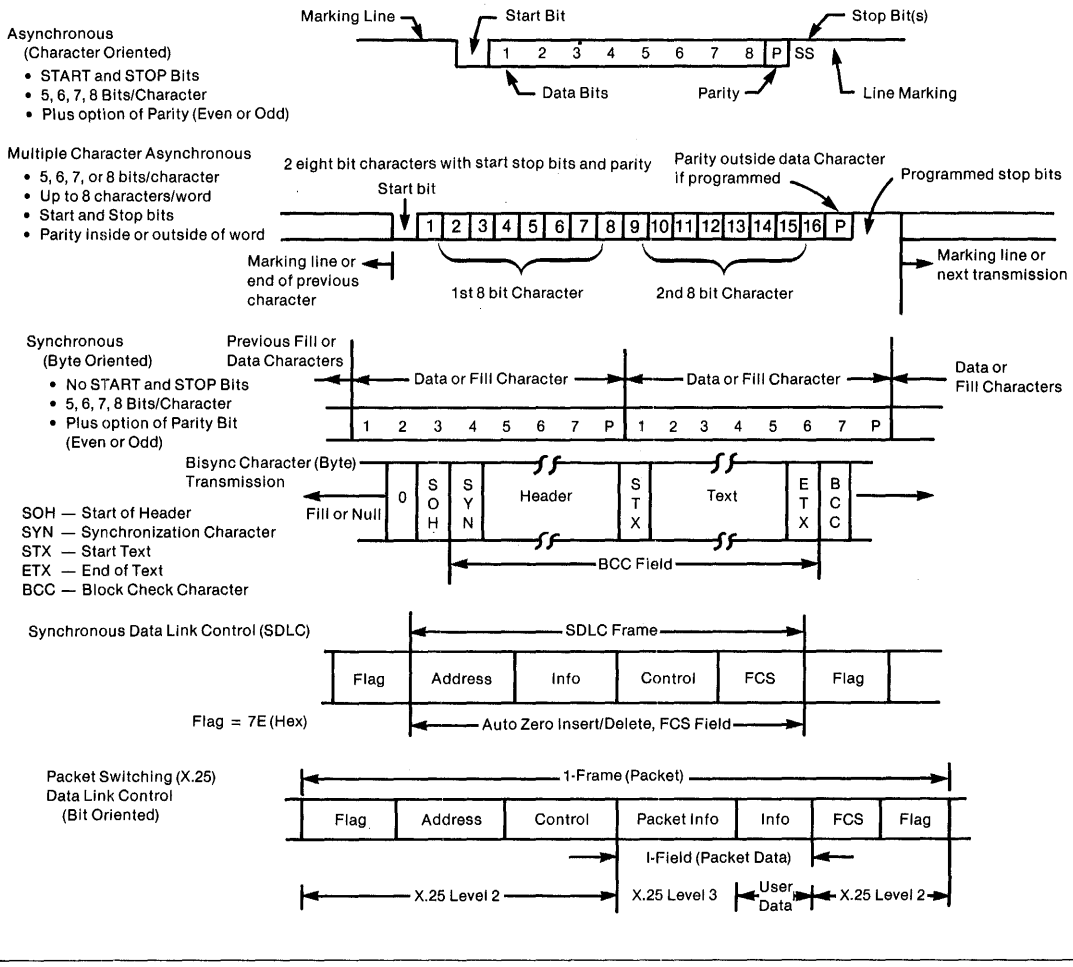
Printed in U.S.A.

Data Communications

DATA COMMUNICATION FAMILIES

UART — Universal Asynchronous Receiver-Transmitter
PSAT — Programmable Synchronous/Asynchronous Transmitter
PSAR — Programmable Synchronous/Asynchronous Receiver
USART — Universal Synchronous/Asynchronous Receiver-Transmitter
BOART — Bus Oriented Asynchronous Receiver-Transmitter
DLC — Data Link Controller

PROTOCOL DEFINITIONS



FUNCTIONALITY COMPATIBILITY GUIDE (PARTIAL LIST)

WD	SIGNETICS	FAIRCHILD	INTEL	MOTOROLA	AMI	SMC	HARRIS	ZILOG	MOSTEK
WD1931	2651 2661	6852	8251A	6852	6852	8251A		SIO	3884
WD1933	2652	6854 6856	8273	6854	6854	5025		SIO	3884
WD1993							3282		
WD2001		9414[1]	8294	6859	6894				
FR1502		33512							

PLEASE CONTACT FACTORY FOR APPLICATIONS ASSISTANCE.

NOTES: 1. Four chip set.

PIN COMPATIBLE REPLACEMENT GUIDE

WD	SMC	GI	NAT	TI	AMI	INTEL	SIGNETICS	HARRIS	INTERSIL
TR1402	COM2502 COM2502H	AY-5-1013A AY-6-1013		TMS6010[4]	S1757		2536		
TR1602	COM2017 COM2017H			TMS6011[4]					
TR1863	COM1863 COM8017	AY-3-1014A						HD6402	IM6402
TR1865	COM8018	AY-3-1015D							
PR1472		AY-3-1472B[4]							
PT1482		AY-3-1482B[4]							
UC1671	COM1671		INS1671						
WD8250			INS8250						
WD1983[1]			INS8251A			8251A			
BR1941[2]	COM5016 COM5036[3]								
WD1943	COM8116								
WD1945	COM8136								

PLEASE CONSULT FACTORY FOR MAXIMUM OPERATING FREQUENCIES AND HIGH-RELIABILITY SCREENING.

NOTES: 1. WD1983 is ASYNC only.
2. Many frequency selections available. Consult factory for details.
Frequency selection is mask programmable — consult factory for details.
3. Pin 10 on BR1941 is a "no connection".
4. Discontinued product.

PRODUCT SELECTION CHART

GENERAL DATA COMMUNICATIONS PRODUCTS		ARINC	UARTS		BOARTS				PSAR/PSAT		USART		DLC
		WD1994-3	TR1602	TR1863/5	WD1183	WD1232-3	WD1250	WD1984	PR1472	PT1482	UC1671	WD1931	WD1933/5
PROTOCOL	ARINC 429	•											
	ASYNCH		•	•	•	•	•	•	•	•	•	•	
	ISOCH		•	•	•	•	•		•	•	•		
	SYNCH (BI-SYNC)							•	•	•	•	•	
	SDLC												•
	HDLC												•
	ADCCP												•
FEATURES	FULL DUPLEX	•	•	•	•	•	•	•			•	•	•
	MAXIMUM 100 kHz												
	320 kHz		•										•
	500 kHz												
	640 kHz	•			•				•	•			
	1000 kHz			•		•	•	•			•	•	•
	1500 kHz			•									
	2500 kHz			•									•
	3500 kHz			•									
	SELECTABLE CLOCK												
	BOTH TRANSMIT AND RECEIVE		•	•									
	INDEPENDENT TRANSMIT AND RECEIVE	•			•	•	•	•	•	•	•	•	•
	1X				•	•	•	•	•	•	•	•	•
	4X	•						•					
	16X		•	•	•	•		•	•	•			•
	32X								•	•	•		•
	64X				•	•	•		•	•	•	•	
	128X										•		
	256X										•		
	WORD LENGTH SELECT 5,6,7,8 BIT	•	•	•	•	•	•	•	•	•	•	•	•
	STOP BIT SELECT 1,1.5,2		•	•	•	•	•	•	•	•	•	•	
	PARITY SELECT ODD/EVEN	•	•	•	•	•	•	•	•	•	•	•	
	MATCH/SYN GENERATE									•	•	•	•
	MATCH/SYN DETECT								•		•	•	•
	BREAK DETECT	•			•	•	•	•					
	DOUBLE BUFFERING	•	•	•	•	•	•	•	•	•	•	•	•
	TTL COMPATIBLE	•	•	•	•	•	•	•	•	•	•	•	•

PRODUCT SELECTION CHART

GENERAL DATA COMMUNICATIONS PRODUCTS		ARINC	UARTS		BOARTS				PSAR/PSAT		USART		DLC
		WD1991-3	TR1863-2	TR1881-⅜	WD1983	WD1210-3	WD2850	WD1984	PR1742	PT8872	UC1671	WD9331	WD9334-⅜
	ERROR CHECKING												
	FRAMING	•	•	•	•	•	•	•	•	•	•	•	•
	OVERRUN	•	•	•	•			•		•			•
	UNDERRUN	•						•			•	•	•
	CRC GENERATE AND CHECK												•
	PROCESSOR INTERFACE												
	UNIDIRECTIONAL		•	•					•	•			
	BIDIRECTIONAL	•			•	•	•	•			•	•	•
	CONTROL PROGRAMMING												
	DEVICE PINS		•	•					•	•			
	BIDIRECTIONAL BUS	•			•	•	•	•			•	•	•
	MODEM INTERFACE												
	NUMBER OF SIGNALS 8												•
	6						•				•	•	
	4			•									
	2					•							
	SELF LOOP TEST	•					•	•			•	•	•
SPECIAL FEATURES	NRZI OPTION												
	DIGITAL PHASE LOCK LOOP										•	•	•
	ON BOARD BAUD RATE GENERATOR					•	•						
	EXTENDED WORD SIZE	•						•					
	TWO FULL DUPLEX CHANNELS					•							

Printed in U.S.A.

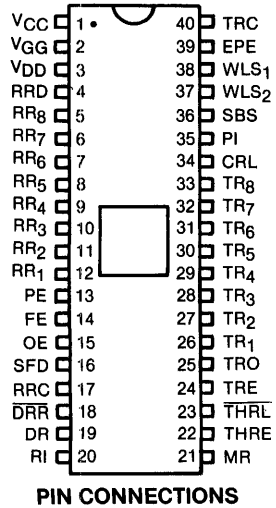
TR1402/TR1602
Universal Asynchronous Receiver/Transmitter (UART)

FEATURES

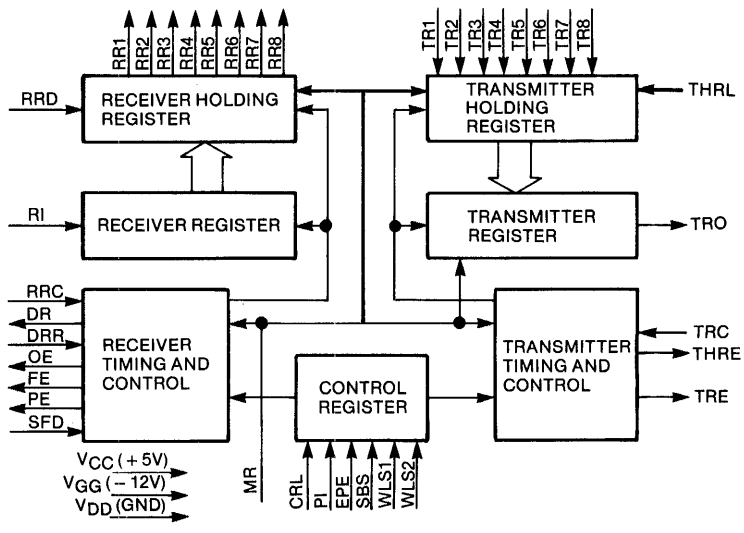
- FULL DUPLEX OR HALF DUPLEX OPERATION
- AUTOMATIC INTERNAL SYNCHRONIZATION OF DATA AND CLOCK
- AUTOMATIC START BIT GENERATION
- EXTERNALLY SELECTABLE
  Word Length
  Baud Rate
  Even/Odd Parity (Receiver/Verification — Transmitter/Generation)
  Parity Inhibit
  One, One and One-Half, or Two Stop Bit Generation (1½ at 5 Bit Level for TR1602)
- AUTOMATIC DATA RECEIVED/TRANSMITTED STATUS GENERATION
  Transmission Complete
  Buffer Register Transfer Complete
  Received Data Available
  Parity Error
  Framing Error
  Overrun Error
- BUFFERED RECEIVER AND TRANSMITTER REGISTERS
- THREE-STATE OUTPUTS
  Receiver Register Outputs
  Status Flags
- TTL COMPATIBLE
- PULL-UP RESISTORS ON ALL INPUTS

APPLICATIONS

- PERIPHERALS
- TERMINALS
- MINI COMPUTERS
- FACSIMILE TRANSMISSION
- MODEMS
- CONCENTRATORS
- ASYNCHRONOUS DATA MULTIPLEXERS
- CARD AND TAPE READERS
- PRINTERS
- DATA SETS
- CONTROLLERS
- KEYBOARD ENCODERS
- REMOTE DATA ACQUISITION SYSTEMS
- ASYNCHRONOUS DATA CASSETTES



PIN CONNECTIONS



TR1602/TR1402 BLOCK DIAGRAM

GENERAL DESCRIPTION

The Universal Asynchronous Receiver/Transmitter (UART) is a general purpose, programmable or hardwired MOS/LSI device. The UART is used to convert parallel data to a serial data format on the transmit side, and converts a serial data format to parallel data on the receive side.

The serial format in order of transmission and reception is a start bit, followed by five to eight data bits, a parity bit (if selectedl) and one, one and one-half (1602 bit data format only) or two stop bits.

Three types of error conditions are available on each received character: parity error, framing error (no valid stop bit) and overrun error.

The transmitter and receiver operate on external 16X clocks, where 16 clock times are equal to one bit time. The receiver clock is also used to sample in the center of the serial data bits to allow for line distortion.

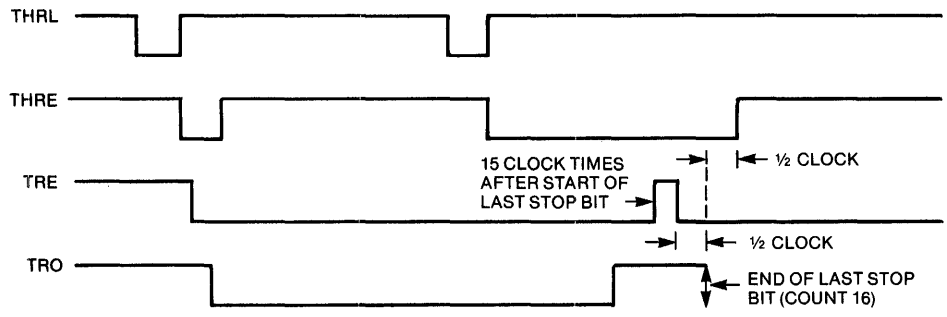
Both transmitter and receiver are double buffered allowing a one character time maximum between a data read or write. Independent handshake lines for receiver and transmitter are also included. All inputs and outputs are TTL compatible with three-state outputs available on the receiver, and error flags for bussing multiple devices.

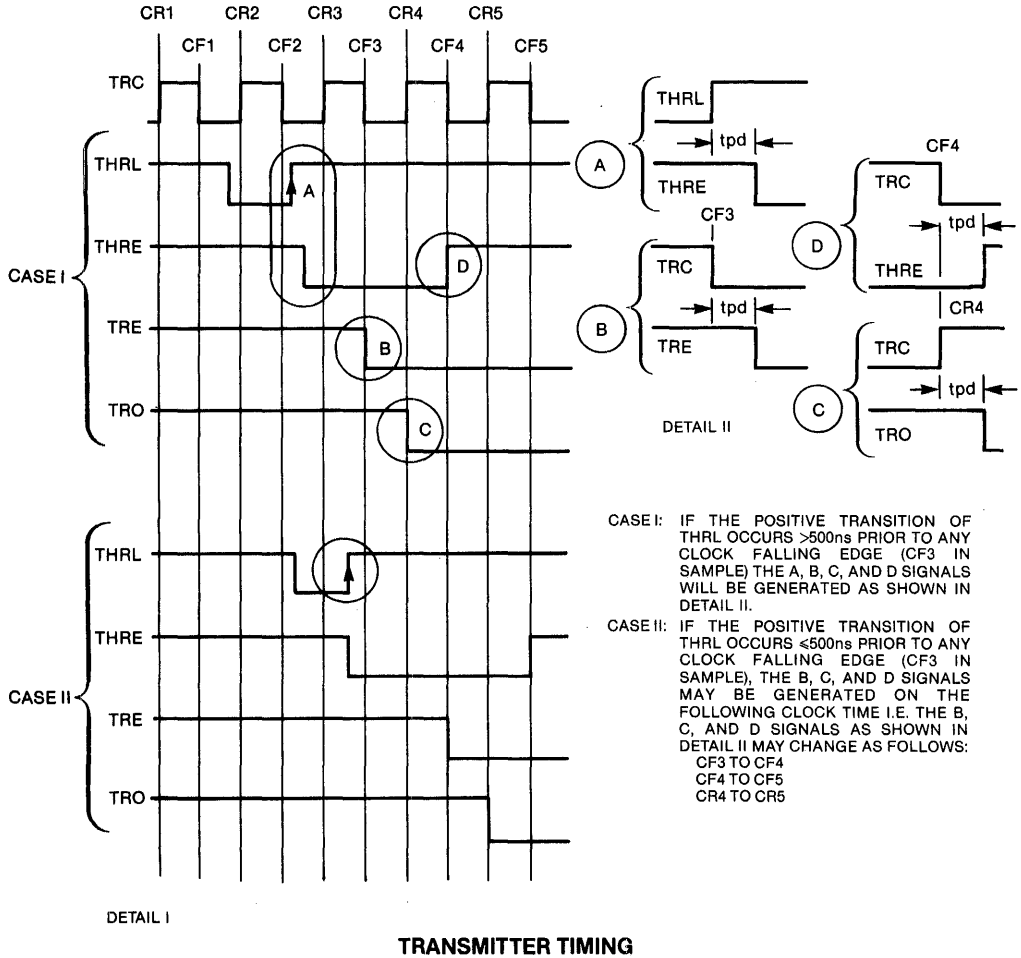
PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	POWER SUPPLY	VSS	+5 volts supply
2	POWER SUPPLY	V_{GG}	-12 volts supply
3	POWER SUPPLY	V_{DD}	Ground = 0V
4	RECEIVER REGISTER DISCONNECT	RRD	A high level input voltage, V_{IH}, applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR_{1-8} data outputs (pins 5-12).
5-12	RECEIVER HOLDING REGISTER DATA	RR_8-RR_1	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines if a low-level input voltage, V_{IL}, is applied to RRD. For character formats of fewer than eight bits received characters are right-justified with RR1 (pin 12) as the least significant bit and the truncated bits are forced to a low level output voltage, V_{OL}.
13	PARITY ERROR	PE	A high level output voltage, V_{OH}, on this line indicates that the received parity differ from that which is programmed by the EVEN PARITY ENABLE control line (pin 39). This output is updated each time a character is transferred to the RECEIVER HOLDING REGISTER. PE lines from a number of arrays can be bussed together since an output disconnect capability is provided by Status Flag Disconnect line (pin 16).
14	FRAMING ERROR	FE	A high-level output voltage, V_{OH}, on this line indicates that the received character has no valid stop bit, i.e., the bit (if programmed) is not a high level voltage. This output is updated each time a character is transferred to the Receiver Holding Register. FE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).

PIN NUMBER	NAME	SYMBOL	FUNCTION
15	OVERRUN ERROR	OE	A high-level output voltage, V_{OH}, on this line indicates that the Data Received Flag (pin 19) was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
16	STATUS FLAGS DISCONNECT	SFD	A high-level input voltage, V_{IH}, applied to this pin disconnects the PE, FE, OE, DR and THRE allowing them to be buss connected.
17	RECEIVER REGISTER CLOCK	RRC	The receiver clock frequency is sixteen (16) times times the desired receiver shift rate.
18	DATA RECEIVED RESET	$\overline{DRR}$	A low-level input voltage, V_{IL}, applied to this line resets the DR line.
19	DATA RECEIVED	DR	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.
20	RECEIVER INPUT	RI	Serial input data. A high-level input voltage, V_{IH}, must be present when data is not being received.
21	MASTER RESET	MR	This line is strobed to a high-level input voltage, V_{IH}, to clear the logic. It resets the TRANSMITTER and RECEIVER HOLDING REGISTERS, the TRANSMITTER REGISTER, FE, OE, PE, DR and sets TRO, THRE, and TRE to a high-level output voltage, V_{OH}.
22	TRANSMITTER HOLDING REGISTER EMPTY	THRE	A high-level output voltage, V_{OH}, on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.
23	TRANSMITTER HOLDING REGISTER LOAD	$\overline{THRL}$	A low-level input voltage, V_{IL}, applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.
24	TRANSMITTER REGISTER EMPTY	TRE	A high-level output voltage, V_{OH}, on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.

PIN NUMBER	NAME	SYMBOL	FUNCTION
25	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the TRANSMITTER REGISTER (START bit, DATA bits, PARITY bit, and STOP bits) are serially shifted out on this line. When no data is being transmitted, this line will remain at a h igh-level output voltage, V_{OH}. Start of transmission is defined as the transition of the START bit from a high-level output voltage VOH, to a low-level output voltage, V_{OL}.
26-33	TRANSMITTER REGISTER DATA INPUTS	TR_1-TR_8	The character to be transmitted is loaded into the TRANSMITTER HOLDING REGISTER on these lines with the THRL Strobe. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), the character is right justified to the least significant bit, TR1, and the excess bits are disregarded. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted.
34	CONTROL REGISTER LOAD	CRL	A high-level input voltage, V_{IH}, on this line loads the CONTROL REGISTER with the control bits (WLS_1, WLS_2, EPE, PI, SBS). This line may be strobed or hard wired to a high-level input voltage, V_{IH}.
35	PARITY INHIBIT	PI	A high-level input voltage, V_{IH}, on this line inhibits the parity generation and verification circuits and will clamp the PE output (pin 13) to V_{OL}. If parity is inhibited, the STOP bit(s) will immediately follow the last data bit of transmission.
36	STOP BIT(S) SELECT	SBS	This line selects the number of STOP bits to be transmitted after the parity bit. A high-level input voltage V_{IH}, on this line selects two STOP bits, and a low-level input voltage, V_{IL}, selects a single STOP bit. The TR1602 generates 1½ stop bits when word length is 5 bits and SBS is High V_{IH}.
37-38	WORD LENGTH SELECT	WLS_1-WLS_2	These two lines select the character length (exclusive of parity) as follows: WLS_2 / WLS_1 / Word Length V_{IL} / V_{IL} / 5 bits V_{IL} / V_{IH} / 6 bits V_{IH} / V_{IL} / 7 bits V_{IH} / V_{IH} / 8 bits
39	EVEN PARITY ENABLE	EPE	This line determines whether even or odd PARITY is to be generated by the transmitter and checked by the receiver. A high-level input voltage, V_{IH}, selects even PARITY and a low-level input voltage, V_{IL}, selects odd PARITY.
40	TRANSMITTER REGISTER	TRC	The transmitter clock frequency is sixteen (16) times the desired transmitter shift rate.

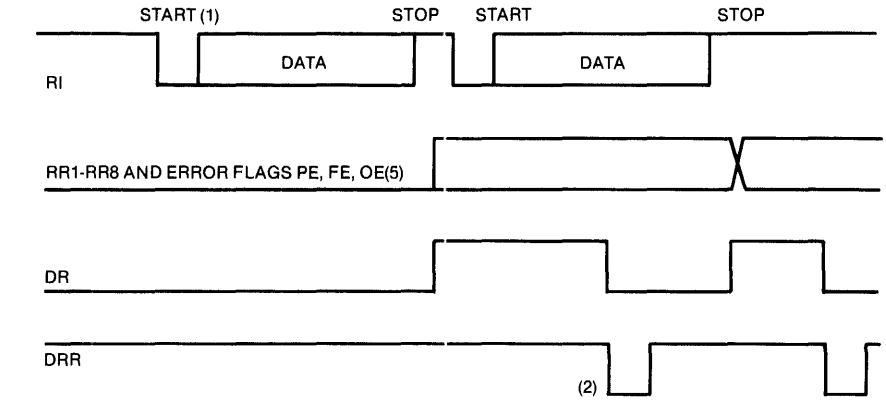




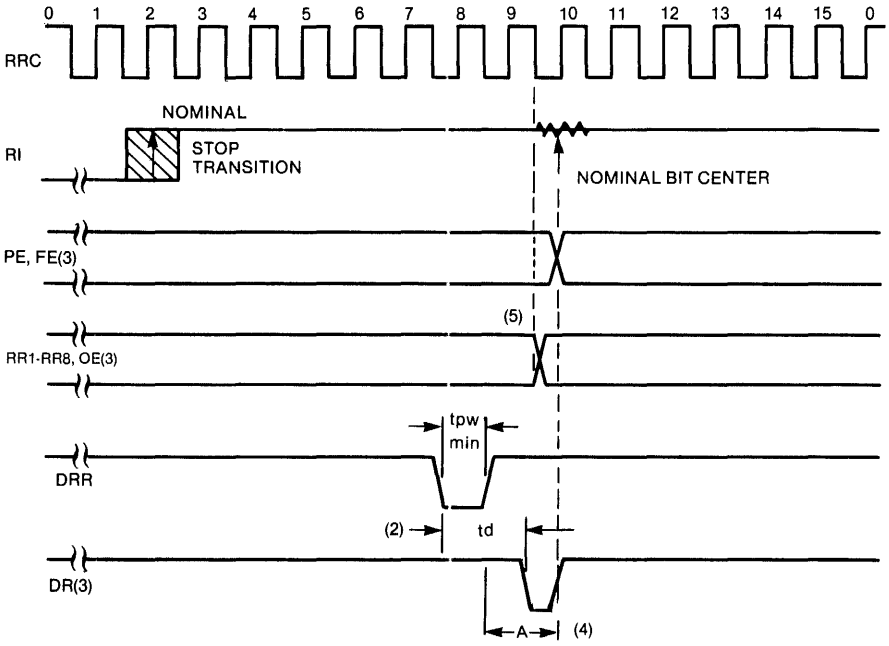
CASE I: IF THE POSITIVE TRANSITION OF THRL OCCURS >500ns PRIOR TO ANY CLOCK FALLING EDGE (CF3 IN SAMPLE) THE A, B, C, AND D SIGNALS WILL BE GENERATED AS SHOWN IN DETAIL II.

CASE II: IF THE POSITIVE TRANSITION OF THRL OCCURS ≤500ns PRIOR TO ANY CLOCK FALLING EDGE (CF3 IN SAMPLE), THE B, C, AND D SIGNALS MAY BE GENERATED ON THE FOLLOWING CLOCK TIME I.E. THE B, C, AND D SIGNALS AS SHOWN IN DETAIL II MAY CHANGE AS FOLLOWS:
- CF3 TO CF4
- CF4 TO CF5
- CR4 TO CR5

TRANSMITTER TIMING

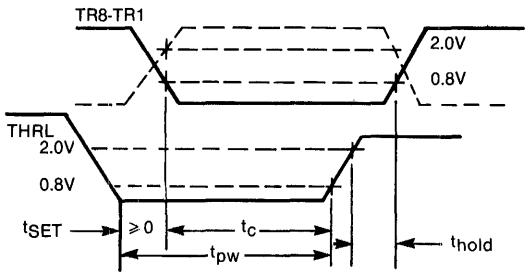


DETAIL:

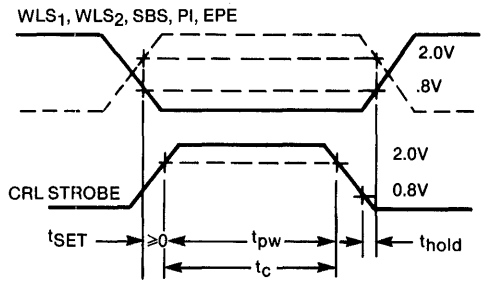


(1) SEE APPLICATION FLAGS REPORT NO. 1 FOR DESCRIPTION OF START BIT DETECTION
(2) THE DELAY BETWEEN DRR AND DR = t_d = 500 ns
(3) DR. ERROR FLAGS, AND DATA ARE VALID AT THE NOMINAL CENTER OF THE FIRST STOP BIT
(4) DRR SHOULD BE HIGH A MINIMUM OF "A" NS (ONE-HALF CLOCK TIME PLUS t_{pd}) PRIOR TO DR RISING EDGE
(5) DATA AND OE PRECEDES DR, PE, AND FE FLAGS BY ½ CLOCK
(6) DATA FLAGS WILL REMAIN SET UNTIL A GOOD CHARACTER IS RECEIVED OR MASTER RESET IS APPLIED.

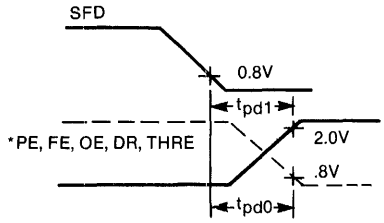
RECEIVER TIMING



DATA INPUT LOAD CYCLE

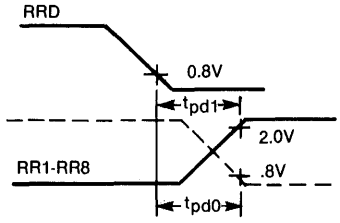


CONTROL REGISTER LOAD CYCLE



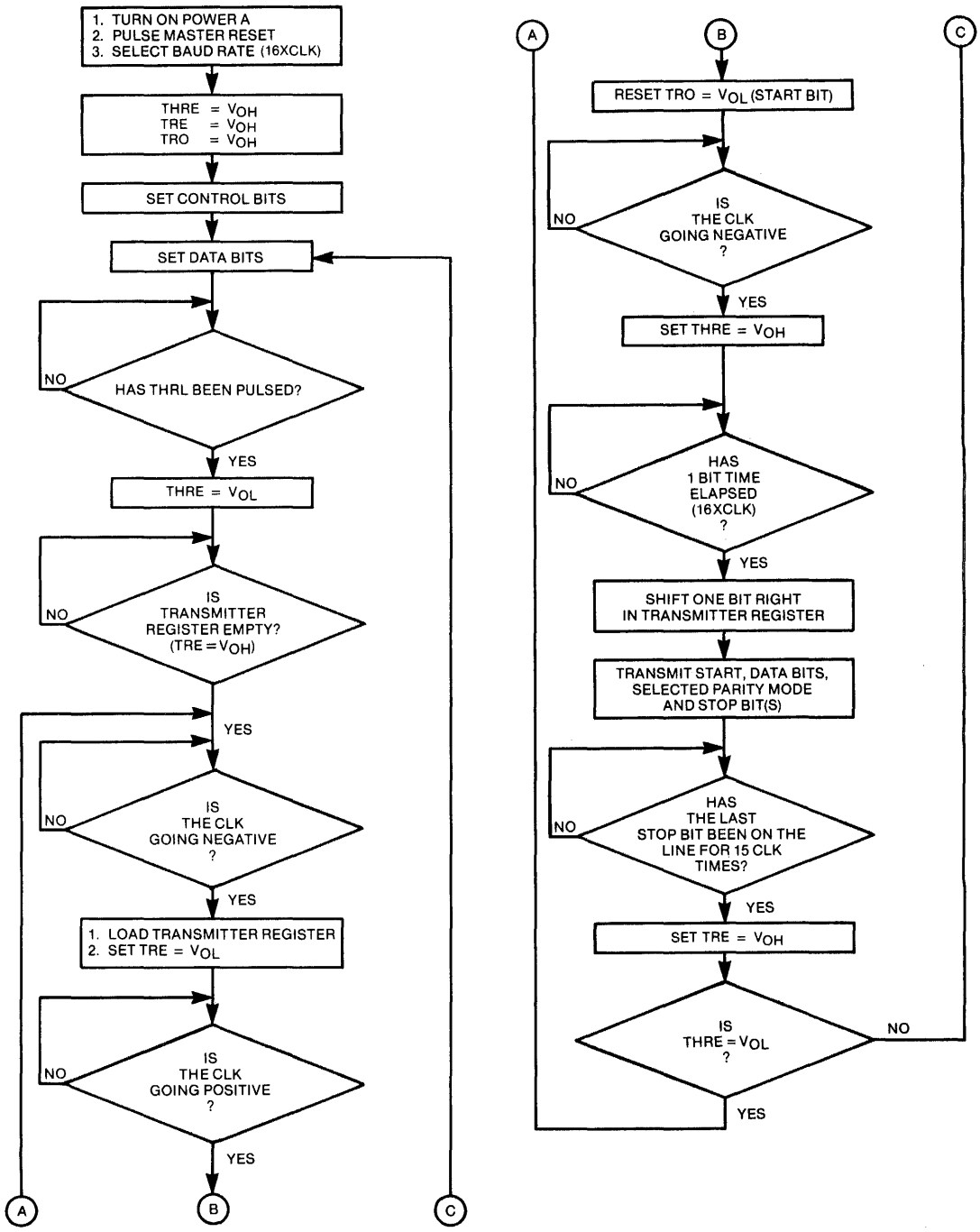
*OUTPUTS PE, FE, OE, DR, THRE ARE DISCONNECTED AT TRANSITION OF SFD FROM 0.8V TO 2.0V.

STATUS FLAG OUTPUT DELAYS

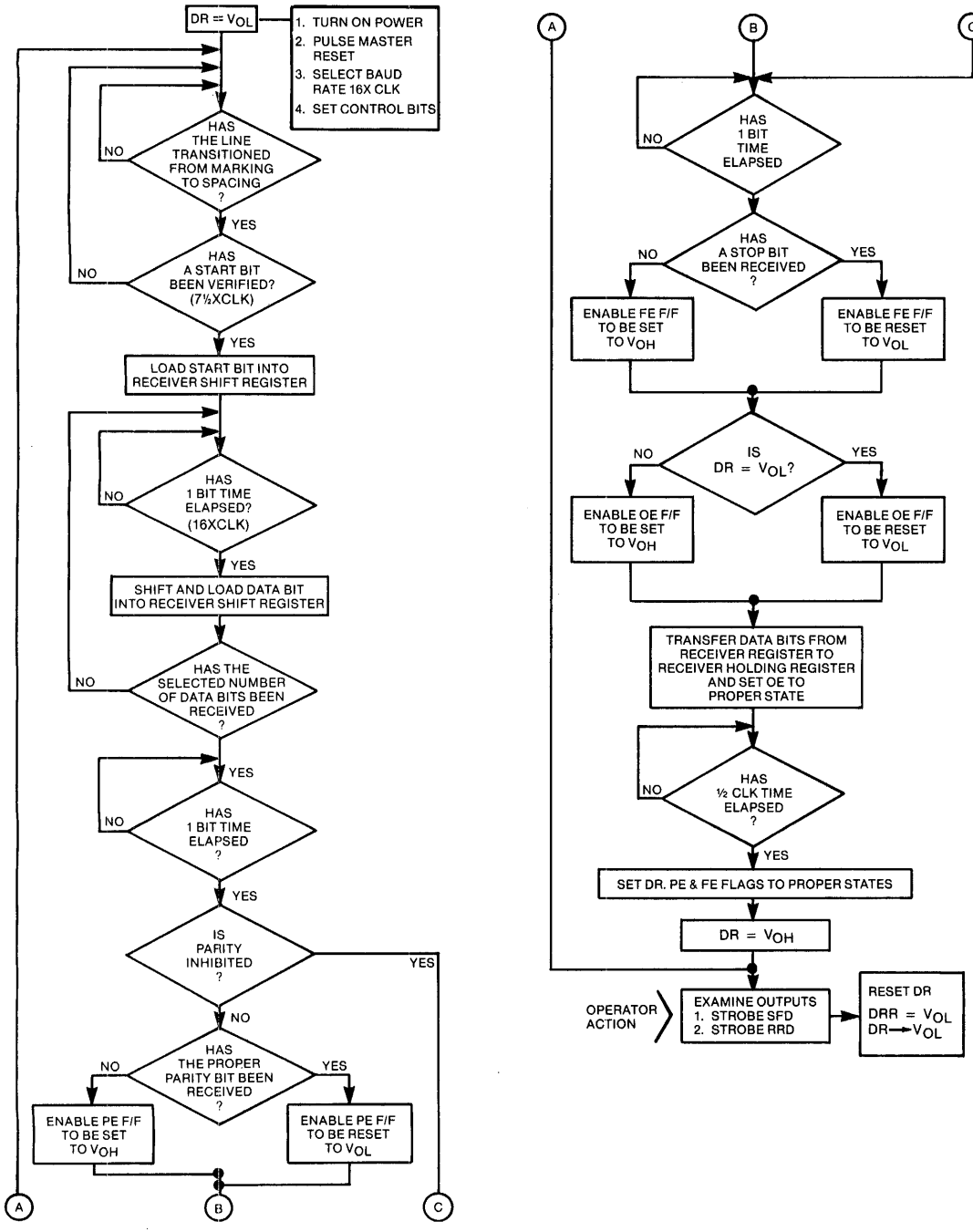


*RR_1–RR_3, ARE DISCONNECTED AT TRANSITION OF RRD FROM 0.8V TO 2.0V.

DATA OUTPUT DELAYS



TRANSMITTER FLOW CHART



RECEIVER FLOW CHART

ABSOLUTE MAXIMUM RATINGS NOTE: These voltages are measured with respect to GND

Storage Temperature
- Plastic ..... −55°C to +125°C
- Ceramic ..... −65°C to +150°C

V_{SS} Supply Voltage ..... −0.3V to +7.0V
Input Voltage at any pin ..... −0.3V to +7.0V
Operating Free-Air Temperature
- T_A Range ..... 0°C to 70°C

Lead Temperature (Soldering, 10 sec.) ..... 300°C

ELECTRICAL CHARACTERISTICS

(V_{SS} = 5V ± 5%, V_{DD} = 0V, V_{GG} = −12V ± 5%)

SYMBOL	PARAMETER	TR1602/TR1402		
	OPERATING CURRENT	MIN	MAX	CONDITIONS
I_{CC}	Substrate Supply Current		60 ma	V_{SS} = 5.25V
I_{GG}	Gate Supply Current		−10 ma	V_{GG} = −12.6V
	LOGIC LEVELS			
V_{IH}	Logic High	V_{SS} − 1.5V		
V_{IL}	Logic Low		0.8V	V_{SS} = 4.75V
	OUTPUT LOGIC LEVELS			
V_{OH}	Logic High	V_{SS} − 1.0V		V_{SS} = 4.75V, I_{OH} = 100μa
V_{OL}	Logic Low		0.4V	V_{SS} = 5.25V, I_{OL} = 1.6 ma
I_{OC}	Output Leakage (High Impedance State)		±10μa	V_{OUT} = 0V, V_{OUT} = 5V SFD = RRD = V_{IH}
I_{IL}	Low Level Input Current		1.6 ma	V_{IN} = 0.4V

SWITCHING CHARACTERISTICS
(See "Switching Waveforms")

		TR1402-* TR1602-01		TR1602-00		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	CONDITIONS
f clock	Clock Frequency	DC	320 KHz	DC	320 KHz	
tpw	Pulse Widths					
	CRL	200 ns		200 ns		
	THRL	200 ns		200 ns		
	DRR	200 ns		200 ns		
	MR	500 ns		500 ns		
tc	Coincidence Time	200 ns		200 ns		
t hold	Hold Time	20 ns		20 ns		
t set	Set-up Time	0		0		
	OUTPUT PROPAGATION DELAYS					
tpd0	To Low State		650 ns		500 ns	C_L = 20pf,
tpdl	To High State		650 ns		500 ns	plus one TTL load
	CAPACITANCE					
Cin	Inputs		20 pf		20 pf	f = 1MHz,
Co	Outputs		20 pf		20 pf	Vin = 5V

*All iterations

See page 725 for ordering information.

WESTERN DIGITAL
CORPORATION

TR1863/TR1865
Universal Asynchronous Receiver/Transmitter (UART)

FEATURES

- SINGLE POWER SUPPLY — +5VDC
- D.C. TO 1 MHZ (64 KB) (STANDARD PART) TR1863/5
- FULL DUPLEX OR HALF DUPLEX OPERATION
- AUTOMATIC INTERNAL SYNCHRONIZATION OF DATA AND CLOCK
- AUTOMATIC START BIT GENERATION
- EXTERNALLY SELECTABLE
  Word Length
  Baud Rate
  Even/Odd Parity (Receiver/Verification — Transmitter/Generation)
  Parity Inhibit
  One, One and One-Half, or Two Stop Bit Generation (1½ at 5 Bit Level)
- AUTOMATIC DATA RECEIVED/TRANSMITTED STATUS GENERATION
  Transmission Complete
  Buffer Register Transfer Complete
  Received Data Available
  Parity Error
  Framing Error
  Overrun Error
- BUFFERED RECEIVER AND TRANSMITTER REGISTERS
- THREE-STATE OUTPUTS
  Receiver Register Outputs
  Status Flags
- TTL COMPATIBLE
- TR1865 HAS PULL-UP RESISTORS ON ALL INPUTS

APPLICATIONS

- PERIPHERALS
- TERMINALS
- MINI COMPUTERS
- FACSIMILE TRANSMISSION
- MODEMS
- CONCENTRATORS
- ASYNCHRONOUS DATA MULTIPLEXERS
- CARD AND TAPE READERS
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- CONTROLLERS
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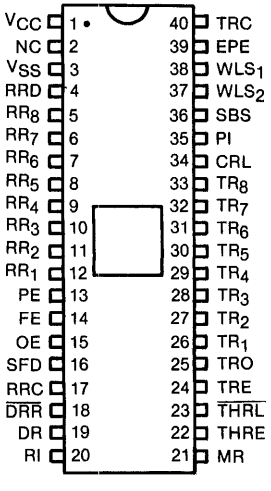
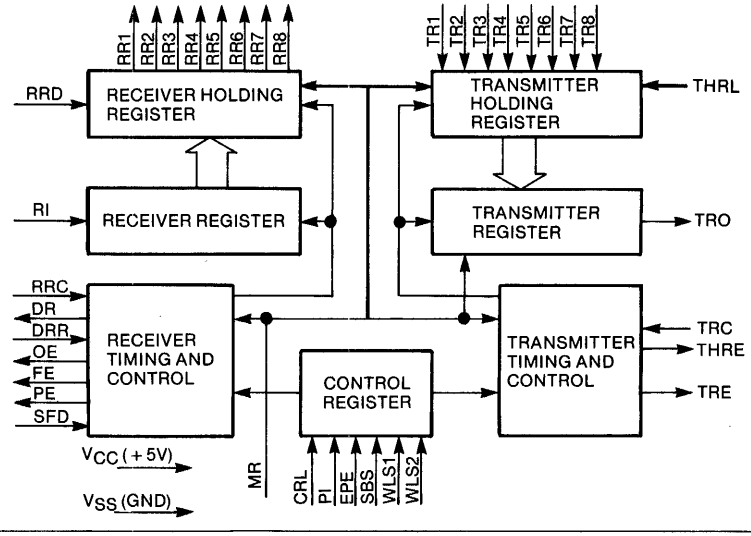
- REMOTE DATA ACQUISITION SYSTEMS
- ASYNCHRONOUS DATA CASSETTES



PIN CONNECTIONS



TR1863/TR1865 BLOCK DIAGRAM

GENERAL DESCRIPTION

The Universal Asynchronous Receiver/Transmitter (UART) is a general purpose, programmable or hardwired MOS/LSI device. The UART is used to convert parallel data to a serial data format on the transmit side, and converts a serial data format to parallel data on the receive side.

The serial format in order of transmission and reception is a start bit, followed by five to eight data bits, a parity bit (if selected) and one, one and one-half, or two stop bits.

Three types of error conditions are available on each received character: parity error, framing error (no valid stop bit) and overrun error.

The transmitter and receiver operate on external 16X clocks, where 16 clock times are equal to one bit time. The receiver clock is also used to sample in the center of the serial data bits to allow for line distortion.

Both transmitter and receiver are double buffered allowing a one character time maximum between a data read or write. Independent handshake lines for receiver and transmitter are also included. All inputs and outputs are TTL compatible with three-state outputs available on the receiver, and error flags for bussing multiple devices.

PIN DEFINITIONS

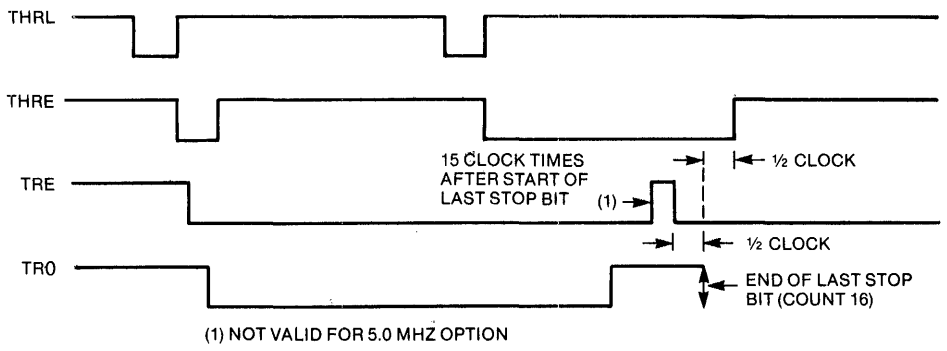
PIN NUMBER	NAME	SYMBOL	FUNCTION
1	POWER SUPPLY	V_{CC}	+5 volts supply
2	NC	NC	No Internal Connection
3	GROUND	V_{SS}	Ground = 0V
4	RECEIVER REGISTER DISCONNECT	RRD	A high level input voltage, V_{IH}, applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR_{1-8} data outputs (pins 5-12).
5-12	RECEIVER HOLDING REGISTER DATA	RR_8-RR_1	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines if a low-level input voltage, V_{IL}, is applied to RRD. For character formats of fewer than eight bits received characters are right-justified with RR1 (pin 12) as the least significant bit and the truncated bits are forced to a low level output voltage, V_{OL}.
13	PARITY ERROR	PE	A high level output voltage, V_{OH}, on this line indicates that the received parity differ from that which is programmed by the EVEN PARITY ENABLE control line (pin 39). This output is updated each time a character is transferred to the RECEIVER HOLDING REGISTER. PE lines from a number of arrays can be bussed together since an output disconnect capability is provided by Status Flag Disconnect line (pin 16).
14	FRAMING ERROR	FE	A high-level output voltage, V_{OH}, on this line indicates that the received character has no valid stop bit, i.e., the bit (if programmed) is not a high level voltage. This output is updated each time a character is transferred to the Receiver Holding Register, FE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).

PIN DEFINITIONS

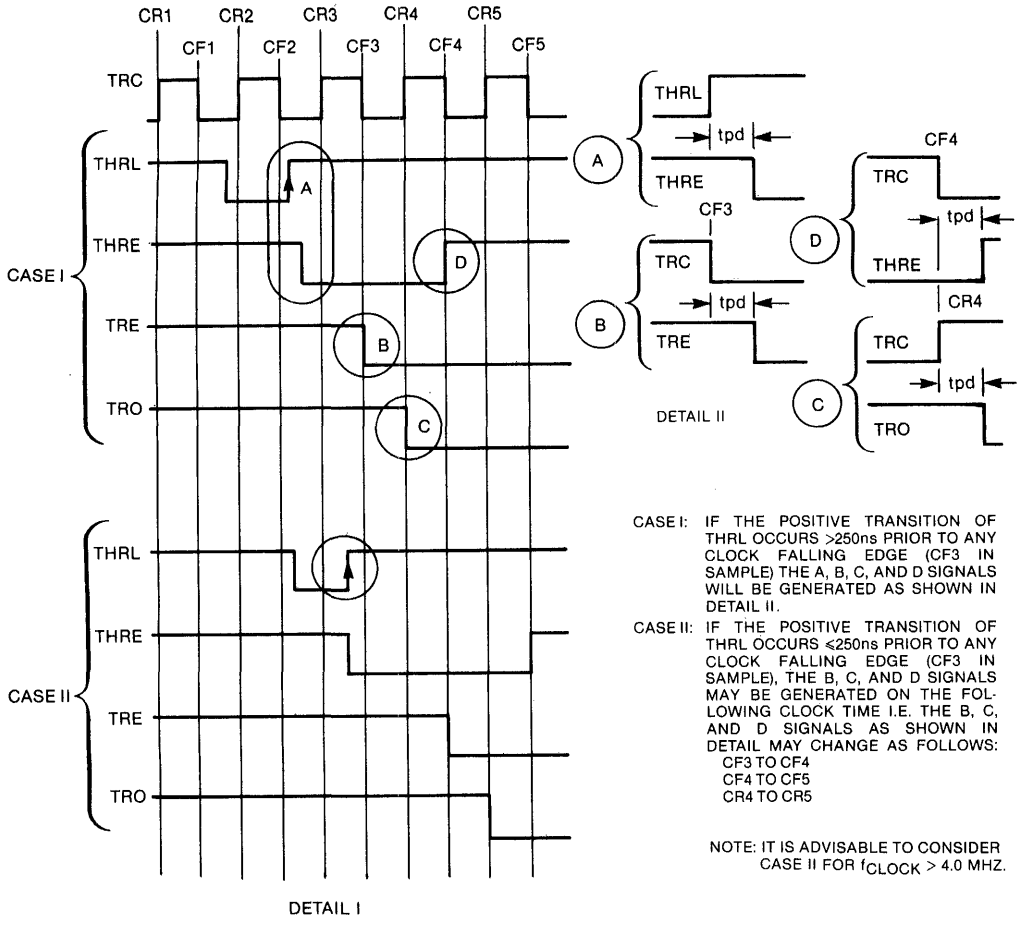
PIN NUMBER	NAME	SYMBOL	FUNCTION
15	OVERRUN ERROR	OE	A high-level output voltage, V_{OH}, on this line indicates that the Data Received Flag (pin 19) was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
16	STATUS FLAGS DISCONNECT	SFD	A high-level input voltage, V_{IH}, applied to this pin disconnects the PE, FE, OE, DR and THRE allowing them to be buss connected.
17	RECEIVER REGISTER CLOCK	RRC	The receiver clock frequency is sixteen (16) times the desired receiver shift rate.
18	DATA RECEIVED RESET	$\overline{DRR}$	A low-level input voltage, V_{IL}, applied to this line resets the DR line.
19	DATA RECEIVED	DR	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.
20	RECEIVER INPUT	RI	Serial input data. A high-level input voltage, V_{IH}, must be present when data is not being received.
21	MASTER RESET	MR	This line is strobed to a high-level input voltage, V_{IH}, to clear the logic. It resets the TRANSMITTER and RECEIVER HOLDING REGISTERS, the TRANSMITTER REGISTER, FE, OE, PE, DR and sets TRO, THRE, and TRE to a high-level output voltage, V_{OH}.
22	TRANSMITTER HOLDING REGISTER EMPTY	THRE	A high-level output voltage, V_{OH}, on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.
23	TRANSMITTER HOLDING REGISTER LOAD	$\overline{THRL}$	A low-level input voltage, V_{IL}, applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.
24	TRANSMITTER REGISTER EMPTY	TRE	A high-level output voltage, V_{OH}, on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.

PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
25	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the TRANSMITTER REGISTER (START bit, DATA bits, PARITY bit, and STOP bits) are serially shifted out on this line. When no data is being transmitted, this line will remain at a high-level output voltage, V_{OH}. Start of transmission is defined as the transition of the START bit from a high-level output voltage V_{OH}, to a low-level output voltage V_{OL}.
26-33	TRANSMITTER REGISTER DATA INPUTS	TR_1-TR_8	The character to be transmitted is loaded into the TRANSMITTER HOLDING REGISTER on these lines with the THRL Strobe. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), the character is right justified to the least significant bit, TR_1, and the excess bits are disregarded. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted.
34	CONTROL REGISTER LOAD	CRL	A high-level input voltage, V_{IH}, on this line loads the CONTROL REGISTER with the control bits (WLS_1, WLS_2, EPE, PI, SBS). This line may be strobed or hard wired to a high-level input voltage, V_{IH}.
35	PARITY INHIBIT	PI	A high-level input voltage, V_{IH}, on this line inhibits the parity generation and verification circuits and will clamp the PE output (pin 13) to V_{OL}. If parity is inhibited, the STOP bit(s) will immediately follow the last data bit of transmission.
36	STOP BIT(S) SELECT	SBS	This line selects the number of STOP bits to be transmitted after the parity bit. A high-level input voltage V_{IH}, on this line selects two STOP bits, and a low-level input voltage, V_{IL}, selects a single STOP bit. The TR1863 and TR1865 generate 1½ stop bits when word length is 5 bits and SBS is High V_{IH}.
37-38	WORD LENGTH SELECT	WLS_2-WLS_1	These two lines select the character length (exclusive of parity) as follows: WLS_2 / WLS_1 / Word Length V_{IL} / V_{IL} / 5 bits V_{IL} / V_{IH} / 6 bits V_{IH} / V_{IL} / 7 bits V_{IH} / V_{IH} / 8 bits
39	EVEN PARITY ENABLE	EPE	This line determines whether even or odd PARITY is to be generated by the transmitter and checked by the receiver. A high-level input voltage, V_{IH}, selects even PARITY and a low-level input voltage, V_{IL}, selects odd PARITY.
40	TRANSMITTER REGISTER	TRC	The transmitter clock frequency is sixteen (16) times the desired transmitter shift rate.



(1) NOT VALID FOR 5.0 MHZ OPTION

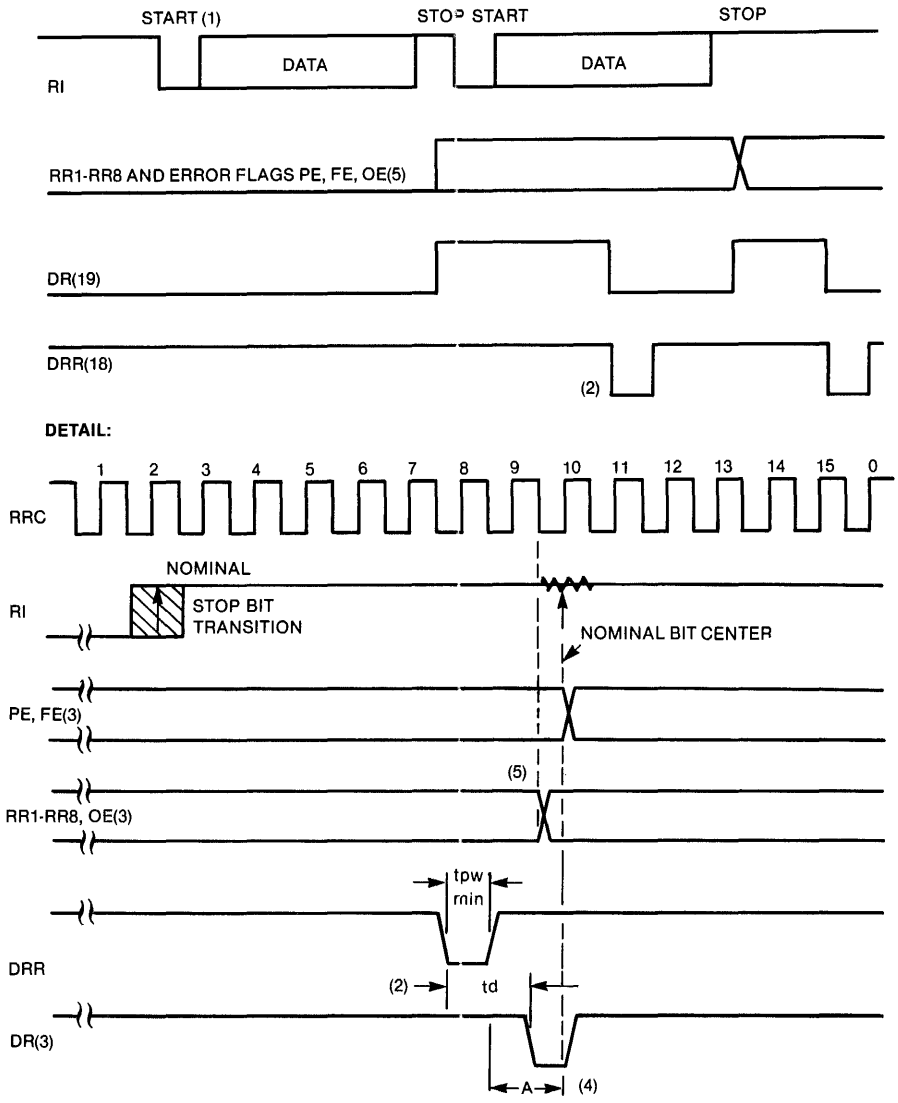


CASE I: IF THE POSITIVE TRANSITION OF THRL OCCURS >250ns PRIOR TO ANY CLOCK FALLING EDGE (CF3 IN SAMPLE) THE A, B, C, AND D SIGNALS WILL BE GENERATED AS SHOWN IN DETAIL II.

CASE II: IF THE POSITIVE TRANSITION OF THRL OCCURS ≤250ns PRIOR TO ANY CLOCK FALLING EDGE (CF3 IN SAMPLE), THE B, C, AND D SIGNALS MAY BE GENERATED ON THE FOLLOWING CLOCK TIME I.E. THE B, C, AND D SIGNALS AS SHOWN IN DETAIL MAY CHANGE AS FOLLOWS:
- CF3 TO CF4
- CF4 TO CF5
- CR4 TO CR5

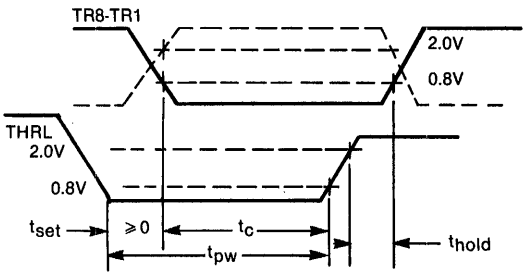
NOTE: IT IS ADVISABLE TO CONSIDER CASE II FOR f_{CLOCK} > 4.0 MHZ.

TRANSMITTER TIMING

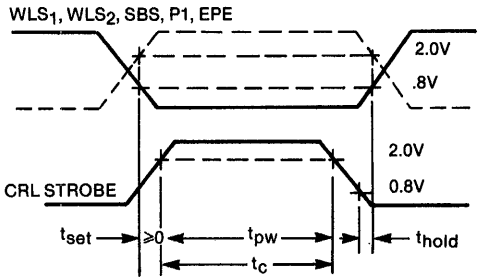


(1) SEE APPLICATION FLAGS REPORT NO. 1 FOR DESCRIPTION OF START BIT DETECTION
(2) THE DELAY BETWEEN DRR AND DR = td = 500 NS
(3) DR. ERROR FLAGS, AND DATA ARE VALID AT THE NOMINAL CENTER OF THE FIRST STOP BIT
(4) DRR SHOULD BE HIGH A MINIMUM OF "A" NS (ONE-HALF CLOCK TIME PLUS tpd) PRIOR TO THE RISING EDGE OF DR
(5) DATA AND OE PRECEDES DR, PE, AND FE FLAGS BY ½ CLOCK
(6) DATA FLAGS WILL REMAIN SET UNTIL A GOOD CHARACTER IS RECEIVED OR MASTER RESET IS APPLIED.

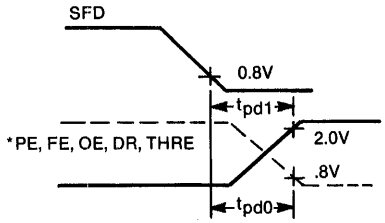
RECEIVER TIMING



DATA INPUT LOAD CYCLE

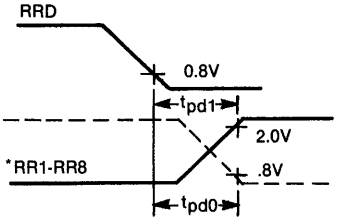


CONTROL REGISTER LOAD CYCLE



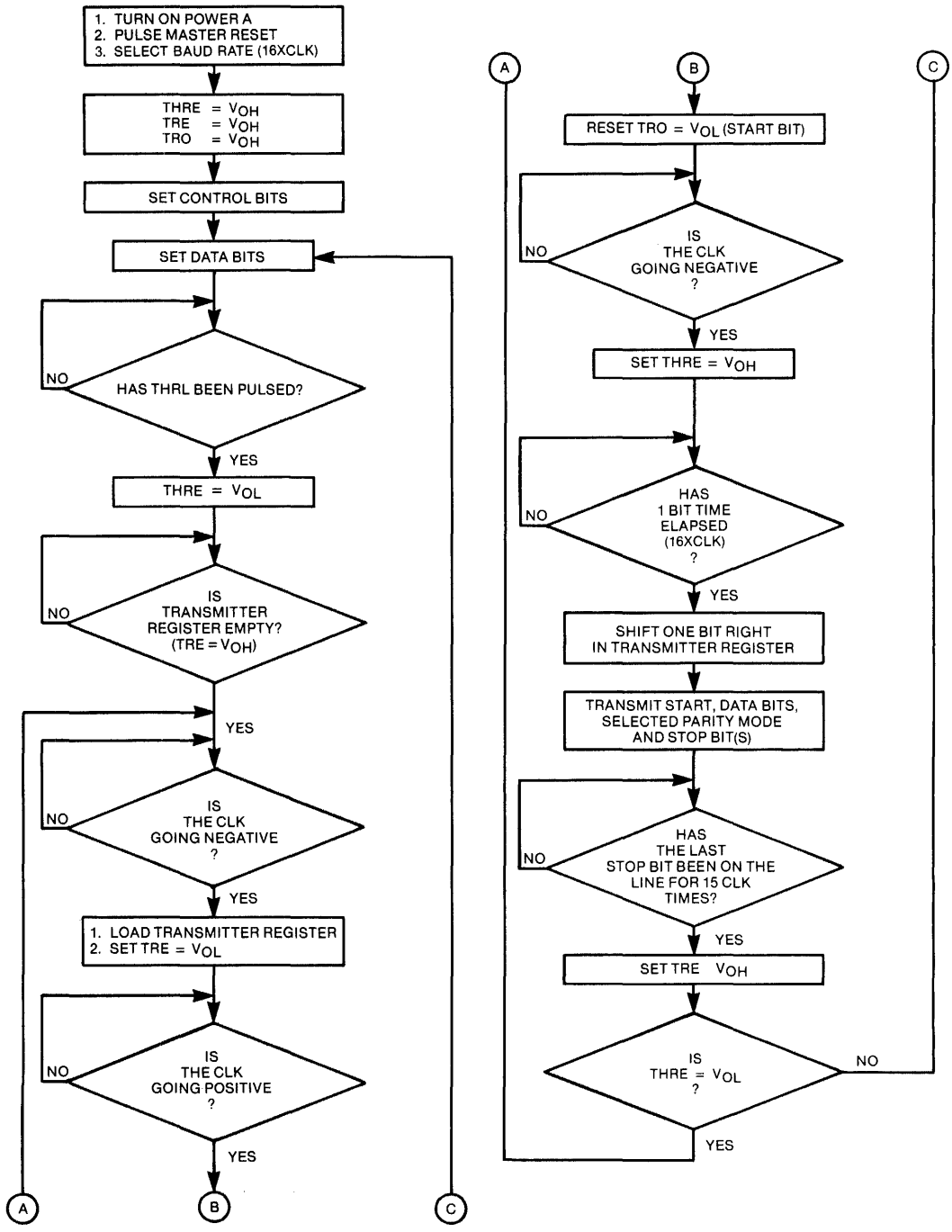
*OUTPUTS PE, FE, OE, DR, THRE ARE DISCONNECTED AT TRANSITION OF SFD FROM 0.8V TO 2.0V.

STATUS FLAG OUTPUT DELAYS

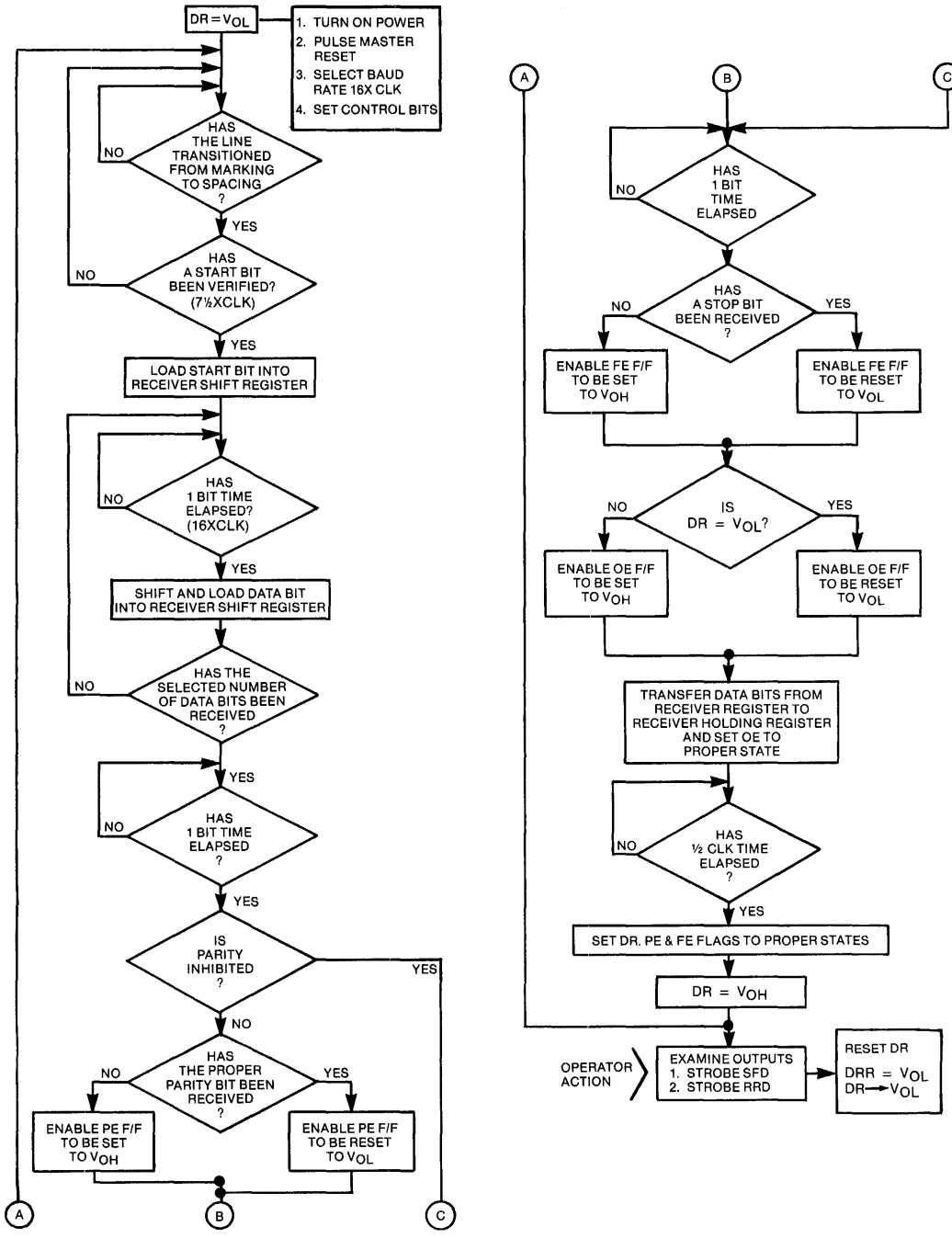


*RR_1-RR_3, ARE DISCONNECTED AT TRANSITION OF RRD FROM 0.8V TO 2.0V.

DATA OUTPUT DELAYS



TRANSMITTER FLOW CHART



RECEIVER FLOW CHART

ABSOLUTE MAXIMUM RATINGS

NOTE: These voltages are measured with respect to GND

Storage Temperature
- Plastic ..... −55°C to +125°C
- Ceramic ..... −65°C to +150°C

V_{CC} Supply Voltage ..... −0.3V to +7.0V
Input Voltage at any pin ..... −0.3V to +7.0V
Operating Free-Air Temperature
- T_A Range ..... 0°C to 70°C

Lead Temperature (Soldering, 10 sec.) ..... 300°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 5%, V_{SS} = 0V)

SYMBOL	PARAMETER	TR1863/5		
	OPERATING CURRENT	MIN	MAX	CONDITIONS
I_{CC}	Supply Current		35ma	V_{CC} = 5.25V
	LOGIC LEVELS			
V_{IH}	Logic High	2.4V		
V_{IL}	Logic Low		0.6V	V_{CC} = 4.75V
	OUTPUT LOGIC LEVELS			
V_{OH}	Logic High	2.4V		V_{CC} = 4.75V, I_{OH} = 100 μa
V_{OL}	Logic Low		0.4V	V_{CC} = 5.25V, I_{OL} = 1.6 ma
I_{OC}	Output Leakage (High Impedance State)		± 10μa	V_{OUT} = 0V, V_{OUT} = 5V SFD = RRD = V_1H
I_{IL}	Low Level Input Current	100μa	1.6ma	V_{IN} = 0.4V TR 1865 only
			10μa	V_{IN} = V_{IL}, TR 1863 only
I_{IH}	High Level Input Current		− 10μa	V_{IN} = V_{IH}, TR 1863 only

SWITCHING CHARACTERISTICS
(See "Switching Waveforms")

SYMBOL	PARAMETER	MIN	MAX	CONDITIONS
f_{clock}	Clock Frequency			V_{CC} = 4.75V
	TR1863-00	DC	1.0 MHz	
	TR1863-02	DC	2.5 MHz	
	TR1863-04	DC	3.5 MHz	
	TR1863-06	DC	5.0 MHz	
	TR1865-00	DC	1.0 MHz	with internal pull-ups on all inputs
	TR1865-02	DC	2.5 MHz	with internal pull-ups on all inputs
	TR1865-04	DC	3.5 MHz	with internal pull-ups on all inputs
	TR1865-06	DC	5.0 MHz	with internal pull-ups on all inputs
t_{pw}	Pulse Widths			
	CRL	200 ns		
	THRL	200 ns		
	DRR	200 ns		
	MR	500 ns		
t_c	Coincidence Time	200 ns		
t_{hold}	Hold Time	20 ns		
t_{set}	Set Time	0		
	OUTPUT PROPAGATION DELAYS			
t_{pd0}	To Low State		250 ns	
t_{pd1}	To High State		250 ns	C_L = 20 pf, plus one TTL load
	CAPACITANCE			
c_{in}	Inputs		20 pf	f = 1 MHz, V_{IN} = 5V
c_o	Outputs		20 pf	f = 1 MHz, V_{IN} = 5V

See page 725 for ordering information.

Printed in U.S.A.

TR1602/TR1863/TR1865 MOS/LSI Application Notes
Asynchronous Receiver/Transmitter

INTRODUCTION

The transfer of digital data over relatively long distances is generally accomplished by sending the data in serial form thru a single communications channel using one of two general transmission techniques; asynchronous or synchronous. Synchronous data transmission requires that a clock signal be transmitted with the data in order to mark the location of the data bits for receiver. A specified clock transition (either rising or falling) marks the start of each data bit interval as shown in Figure 1. In addition, special synchronization data patterns are added to the start of the transmission in order for the receiver to locate the first bit of the message. With synchronous transmission, each data bit must follow contiguously after the sync word, since one data bit is assumed for every clock period.

With asynchronous transmission, a clock signal is not transmitted with the data and the characters need not be contiguous. In order for the receiver to properly recover the message, the bits are grouped into data characters (generally from 5 to 8 bits in length) and synchronizing start and stop elements are added to each character as shown in Figure 2.

The start element is a single logic zero (space) data bit that is added to the front of each character. The stop element is a logic one (mark) that is added to the end of each character. The stop element is maintained until the next data character is ready to be transmitted. (Asynchronous transmission is often referred to as start-stop transmission for obvious reasons). Although there is no upper limit to the length of the stop element, there is a lower limit that depends on the system characteristics. Typical lower limits are 1.0, 1.42 or 2.0 data bit intervals, although most modern systems use 1.0 or 2.0. The negative going transition of the start element defines the location of the data bits in one character. A clock source at the receiver is reset by this transition and is used to locate the center of each data bit.

The rate at which asynchronous data is transmitted is usually measured in baud, where a baud is defined to be the reciprocal of the shortest signal element (usually one data bit interval). It is interesting to note that the variable stop length is what makes the baud rate differ from the bit rate. For synchronous transmission, each element is one bit in length so that the baud rate equals the bit rate. The same is true for

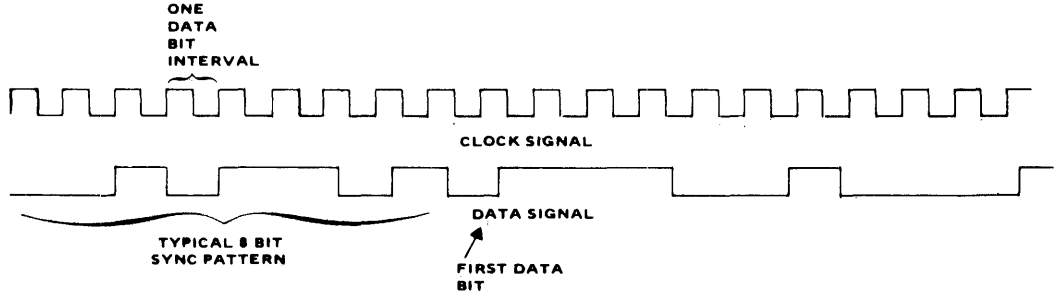


Figure 1. Synchronous Data

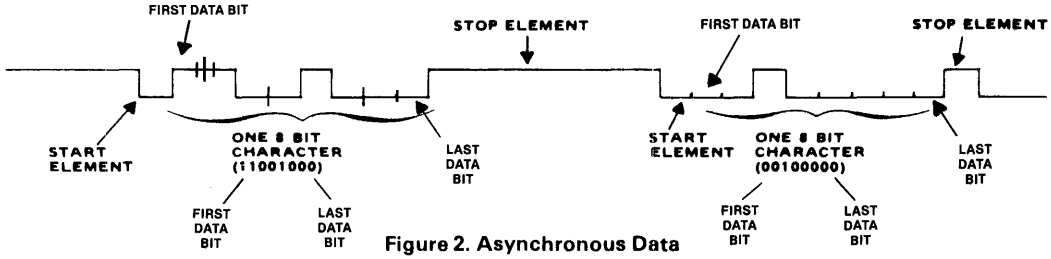


Figure 2. Asynchronous Data

asynchronous transmission if the stop element is always one bit in duration (this is referred to as *isochronous* transmission). However, when the stop code is longer than one bit, as shown in Figure 3, the baud rate differs from the bit rate.

Each character in Figure 3 is 11 data bit intervals in length, and if 15 characters are transmitted per second, then the shortest signal element (one data bit interval) is 66.6 ms/11 = 6.06 ms; giving a rate of 1/6.06 ms = 165 baud. However, since only 10 bits of information (8 data bits, one start bit and 1 stop bit) are transmitted every 66.6 msec, the bit rate is 150 bit/sec. (Even though the stop element lasts for two data intervals, it still is only one bit of information.)

There are several reasons for using asynchronous transmission. The major reason is that since a clock signal need not be transmitted with the data, transmission equipment requirements are greatly simplified. (Note, however, that an independent clock source is still required at both the transmitter and receiver). Another advantage of asynchronous transmission is that characters need not be contiguous in time, but are transmitted as they become available. This is a very valuable feature when transmitting data from manual entry devices such as a keyboard. The major disadvantage of asynchronous transmission is that it requires a very large portion of the communication channel bandwidth for the synchronizing start and stop elements (a much smaller portion of the bandwidth is required for the sync words used in synchronous transmission).

Asynchronous transmission over a simple twisted wire pair can be accomplished at moderately high baud rates (10K baud or higher depending on the length of the wire, type of line drivers, etc.) while it is generally limited to approximately 2K baud over the telephone network. When operating over the telephone network, a modem is required to convert the data pulses to tones that can be transmitted through the network.

One of the major limiting factors in the speed of asynchronous transmission is the distortion of the signal elements. Distortion is defined as the time placement between the actual signal level transition and the nominal transition (Δt), divided by the nominal data bit interval (See Figure 4).

The nominal data bit interval is equal to the reciprocal of the nominal transmission baud rate and all data transitions should ideally occur at an integer number of intervals from the start bit negative going transition. Actual data transitions may not occur at these nominal points in time as shown in the lower waveform of Figure 4. The distortion of any bit transition is equal to Δt x NOMINAL BAUD RATE.

This distortion is generally caused by frequency jitter and frequency offset in the clock source used to generate the actual waveform as well as transmission channel, noise, etc. Thus, the amount of distortion that can be expected on any asynchronous signal depends on the device used to generate the signal and the characteristics of the communication channel over which it was sent. Electronic signal generators can be held to less than 1% distortion while electromechanical devices (such as a teletype) typically generate up to 20% distortion. The transmission channel may typically add an additional 5% to 15% distortion.

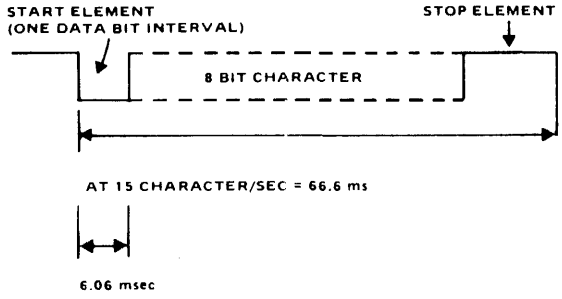


Figure 3.

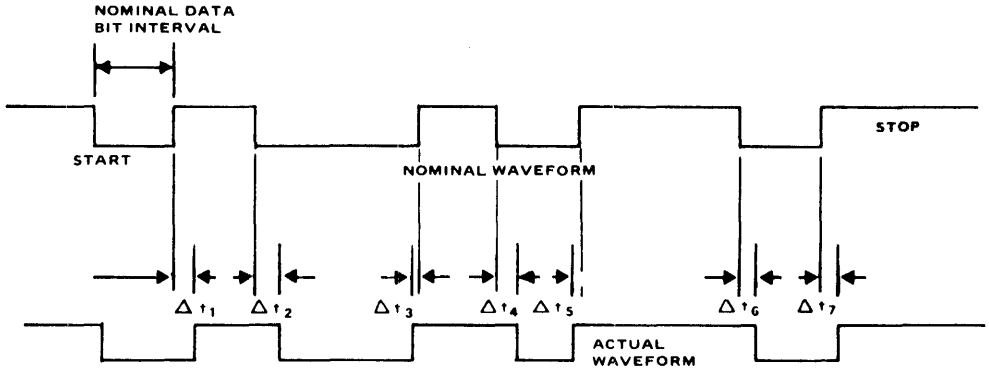


Figure 4A

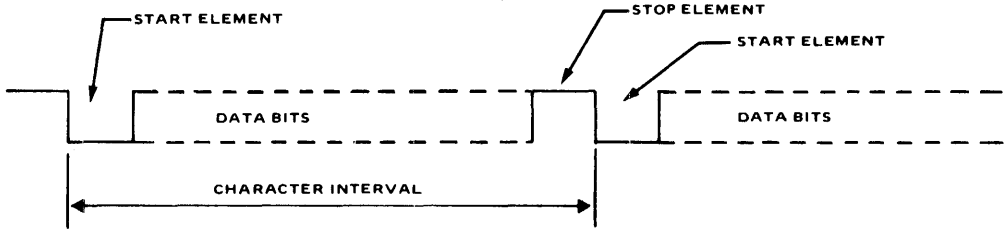


Figure 4B

The distortion previously described referred only to a single character as all measurements were referenced to the start element transition of that character. However, there may also be distortion between characters when operating at the maximum possible baud rate (i.e., stop elements are of minimum length). This type of distortion is usually measured by the minimum character interval as shown in Figure 4B.

The minimum character interval distortion is generally specified as the percentage of a nominal data bit interval that any character interval may be shortened from its nominal length. Since many of the same parameters that cause distortion of the data bits are also responsible for the character length distortion, the two distortions are often equal. However, some systems may exhibit character interval distortions of up to 50% of a data bit interval. This parameter is important when operating at the maximum baud rate since the receiver must be prepared to detect the next start bit transition after the minimum character interval.

Asynchronous receivers operate by locating the nominal center of the data bits as measured from the start bit negative going transition. However, due to receiver inaccuracies, the exact center may not be properly located. In electromechanical devices such as teletypes, the inaccuracy may be due to mechanical tolerances or variations in the power line frequency. With electronic receivers, the inaccuracies are due to frequency offset, jitter and resolution of the clock source used to find the bit centers. (The bit centers are located by counting clock pulses). For example, even if the receiver clock had no jitter or offset, and it was 16 times the baud rate, then the center of the bit could only be located within 1/16 of a bit interval (or 6.25%) due to clock resolution. However, by properly phasing the clock, this tolerance can be adjusted so that the sample will always be within ±3.125% of the bit center. Thus, signals with up to 46.875% distortion could be received. This number (the allowable receiver input distortion) is often referred to as the receiver distortion margin. Electromechanical receivers have distortion margins of 25 to 30%. The receiver must also be prepared to accept a new character after the minimum character interval. Most receivers are specified to operate with a minimum character interval distortion of 50%.

TR1602 OPERATION**

The WDC TR1602 is designed to transmit and receive asynchronous data as shown in Figure 5. Both the transmitter and the receiver are in one MOS CHIP, packaged in a 40 lead ceramic DIP. The array is capable of full duplex (simultaneous transmission and reception) or half duplex operation.

The transmitter basically disassembles parallel data characters into a serial asynchronous data system. Control lines are included so that the characters may be 5, 6, 7 or 8 bits in length, have an even or odd parity bit, and have either one or two* stop bits. Furthermore, the baud rate can be set anywhere between DC and 20K baud by providing a transmit clock at 16 times the desired baud rate.

* 1-1/2 with 5 bit code

** All references to the TR1602 operation also apply to the TR1863/TR1865 operation.

The receiver assembles the asynchronous characters into a parallel data character by searching for the start bit of every character, finding the center of every data bit, and outputting the characters in a parallel format with the start, parity and stop bits removed. Three error flags are also provided to indicate if the parity was in error, a valid stop bit was not decoded or the last character was not unloaded by the external device before the next character was received (and therefore the last character was lost). The receiver clock is set at 16 times the transmitter baud rate.

Both the transmitter and receiver have double character buffering so that at least one complete character interval is always available for exchange of the characters with the external devices. This double buffering is especially important if the external device is a computer, since this provides a much longer permissible interrupt latency time (the time required for the computer to respond to the interrupt).

The status of the transmitter buffer and the receiver buffer (empty or full) is also provided as an output.

Another feature of the TR1602 is that the control information can be strobed into the transmitter and receiver and stored internally. This allows a common bus from a computer to easily maintain the controls for a large number of transmitter/receivers.

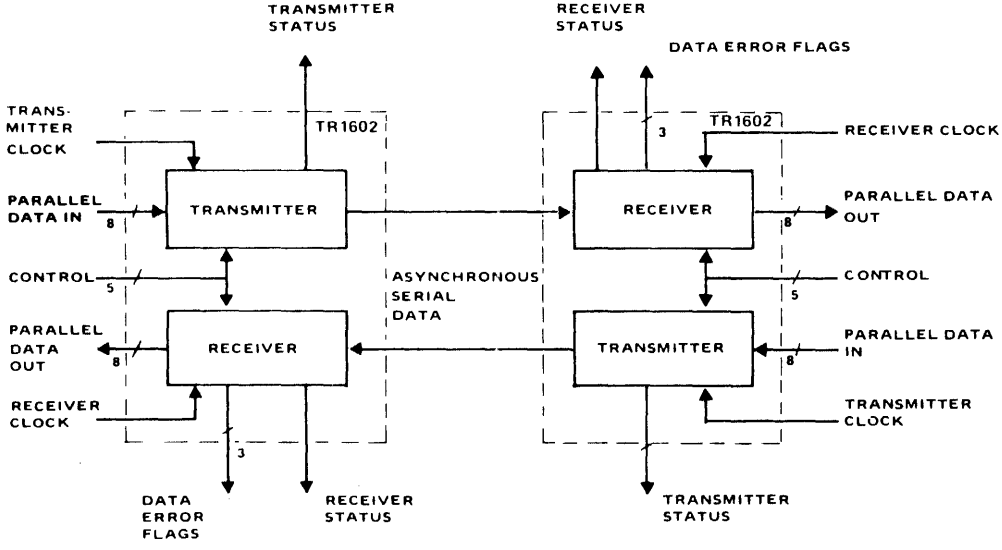


Figure 5

The TR1602 data and error flag outputs are designed for direct compatibility with bus organized systems. This feature is achieved by providing completely TTL compatible Three-state outputs (no external components are required). Three-state outputs may be set to a logic one or logic zero when enabled, or set to an open circuit (very high impedance) when disabled. A separate control line is provided to enable the data outputs and another one to enable the error flags so that the data outputs can be tied to a separate bus from the flag outputs.

The TR1602 inputs are also directly compatible with TTL logic elements without any external components. TR1863 require pullups on inputs.

TR1602 DESCRIPTION

Figure 6 is a block diagram of the transmitter portion of the TR1602. Data can be loaded into the Transmitter Holding Register whenever the Transmitter Holding Register Empty (THRE) line is at a logic one, indicating that the Transmitter Holding Register is empty. The data is loaded in by strobing the Transmitter Holding Register Load (THRL) line to a logic zero. The data is automatically transferred to the Transmitter Register as soon as the Transmitter Register becomes empty. The desired start, stop and parity bits are then added to the data and serial transmission is started. The number of stop bits and the type of parity bit is under control of the Control Register. The state of the control lines is loaded into the Control Register when the Control Register Load (CRL) line is strobed to a logic one. The 5 control lines allow 24 different character formats as shown in Table 1. These 24 formats cover almost all of the transmission schemes presently in use.

Table 1.
CONTROL DEFINITION

CONTROL WORD					CHARACTER FORMAT			
WLS2	WLS1	PI	EPE	SBS	START BIT	DATA BITS	PARITY BIT	STOP BITS
0	0	0	0	0	1	5	ODD	1
0	0	0	0	1	1	5	ODD	1.5
0	0	0	1	0	1	5	EVEN	1
0	0	0	1	1	1	5	EVEN	1.5
0	0	1	x	0	1	5	NONE	1
0	0	1	x	1	1	5	NONE	1.5
0	1	0	0	0	1	6	ODD	1
0	1	0	0	1	1	6	ODD	2
0	1	0	1	0	1	6	EVEN	1
0	1	0	1	1	1	6	EVEN	2
0	1	1	x	0	1	6	NONE	1
0	1	1	x	1	1	6	NONE	2
1	0	0	0	0	1	7	ODD	1
1	0	0	0	1	1	7	ODD	2
1	0	0	1	0	1	7	EVEN	1
1	0	0	1	1	1	7	EVEN	2
1	0	1	x	0	1	7	NONE	1
1	0	1	x	1	1	7	NONE	2
1	1	0	0	0	1	8	ODD	1
1	1	0	0	1	1	8	ODD	2
1	1	0	1	0	1	8	EVEN	1
1	1	0	1	1	1	8	EVEN	2
1	1	1	x	0	1	8	NONE	1
1	1	1	x	1	1	8	NONE	2

A Master Reset (MR) input is provided which sets the transmitter to the idle state whenever this line is strobed to a logic one. In addition, a Status Flag Disconnect (SFD) line is provided. When this signal is at a logic one, the THRE output is disabled and goes to a high impedance. This allows the THRE outputs of a number of arrays to be tied to the same data bus.

Figure 7 illustrates the relative timing of the transmitter signals. After power turn-on, the master reset should be strobed to set the circuits to the idle state. The external device can then set the transmitter register data inputs to the desired value and after the data inputs are stable, the load pulse is applied. The data is then automatically transferred to the Transmitter Register where the start, stop and parity (if required) bits are added and transmission is started. This process is then repeated for each subsequent character as they become available. The only timing requirement for the external device is that the data inputs be stable during the load pulse (and 20 nsec after).

The TR1602 Transmitter output will have less than 1% Distortion at baud rates of up to 20K baud (assuming the Transmitter Register Clock is perfect) and is, therefore, compatible with virtually all other asynchronous receivers.

Figure 8 is a block diagram of the Receiver portion of the TR1602. Serial asynchronous data is provided to the Receiver Input (RI). A start bit detect circuit continually searches for a logic one to logic zero transition while in the idle state. When this transition is located, a counter is reset and allowed to count until the center of the start bit is located. If the input is still a logic zero at the center, the signal is assumed to be a valid start bit and the counter continues to count to find the center of all subsequent data and stop bits. (Verification of the start bit prevents the receiver from assembling an erroneous data character when a logic zero noise spike is presented to the Receiver Input). The Receiver is under control of the Control Register described in the previous paragraph. This register

Figure 6. Transmitter Block Diagram

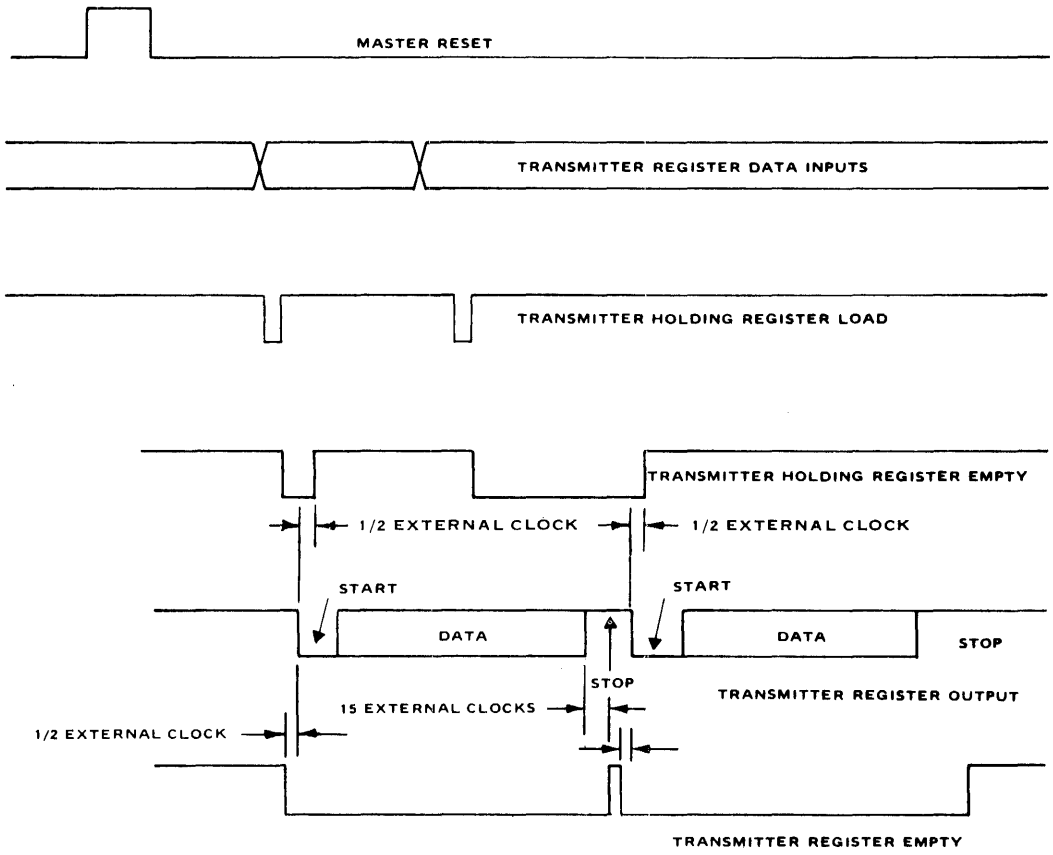


Figure 7. Transmitter Timing Diagram

controls the number of data bits, number of stop bits, and the type of parity as described in Table 1. The word length gating circuit adjusts the length of the Receiver Register to match the length of the data characters. A parity check circuit checks for even or odd parity if parity was added by the Transmitter. If parity does not check a Parity Error signal will be set to a logic one and this signal will be held until the next character is transferred to the Holding Register. A circuit is also provided that checks the first stop bit of each character. If the stop bit is not a logic one, the Framing Error line will be set to a logic one and held until the next character is transferred to the Holding Register. This feature permits easy detection of a break character (null character with no stop element).

As each received character is transferred to the Holding Register, the Data Received (DR) line is set to a logic one indicating that the external device may sample the data output. When the external device samples the output, it should strobe the Data Received Reset (DRR) line to a logic zero to reset the DR line. If the DR line is not reset before a new character is transferred to the Holding Register (i.e., a character is lost) the Overrun Error line will be set to a logic one and held until the next character is loaded into the Holding Register. The timing for all of the Receiver functions is obtained from the external Receiver Register Clock which should be set at 16 times the baud rate of the transmitter.

Figure 8. Receiver Block Diagram

Figure 9 illustrates the relative timing of the Receiver signals. A Master Reset strobe places the unit in the idle mode and the Receiver then begins searching for the first start bit. After a complete character has been decoded, the data output and error flags are set to the proper level and the Data Received (DR) line is set to a logic one. Although it is not apparent in Figure 9, the data outputs are set to the proper level one half clock period before the DR and error flags, which are set in the center of the first stop bit. The Data Received Reset pulse resets the DR line to a logic zero. Data can be strobed out at any time before the next character has been disassembled.

The TR1602 Receiver uses a 16X clock for timing purposes. Furthermore, the center of the start bit is defined as clock count 7-1/2. Therefore, if the receiver clock is a symmetrical square wave as shown in Figure 10, the center of the bits will always be located within ±3.125% (assuming a perfect input clock) thus giving a receiver margin of 46.875%.

In Figure 10, the start bit could have started as much as one complete clock period before it was detected, as indicated by the shaded area of the negative going transition. Therefore, the exact center is also unknown by the shaded area around the sample point. This turns out to be ± 1/32 = ±3.125%.

If the receiver clock is not perfect, then the receiver distortion margin must be further reduced. For example, if the clock had 1.0% jitter, 0.1% offset and the positive clock pulse was only 40% of the clock cycle; then, for a 10 element character, the clock would add:

$$1.0\% + (0.1\% \times 10) + 0.1\,(1/16) = 2.3\%\ \text{Distortion}$$

(Jitter) (Offset) (Non-symmetrical Clock)

(The frequency offset was multiplied by the number of elements per character since the offset is cumulative on each element.

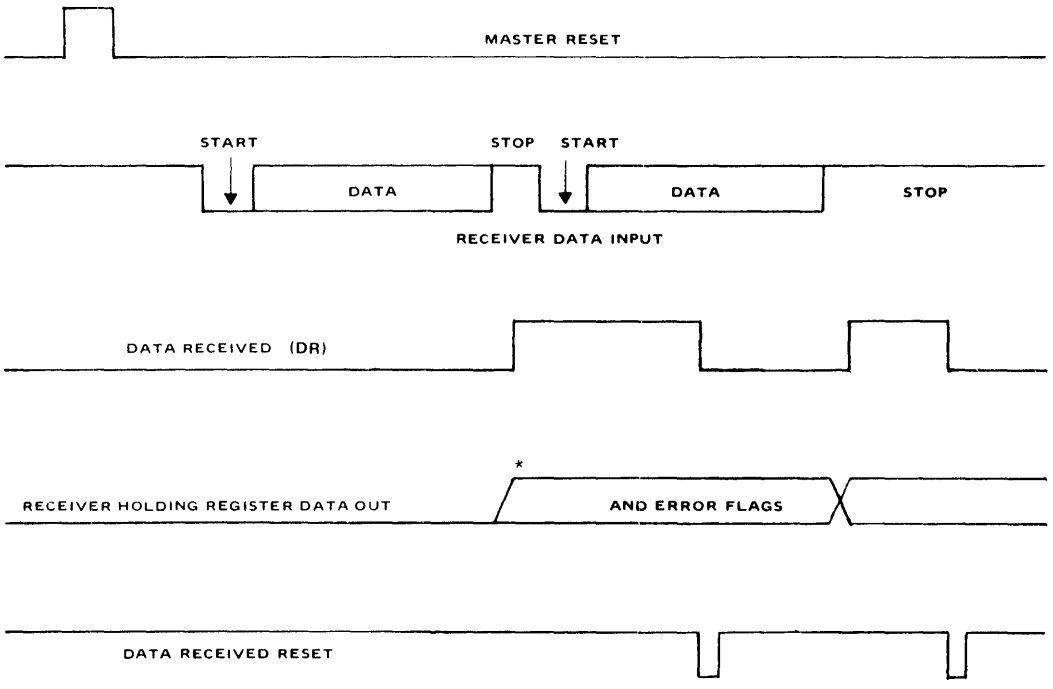


Figure 9. Receiver Timing Diagram

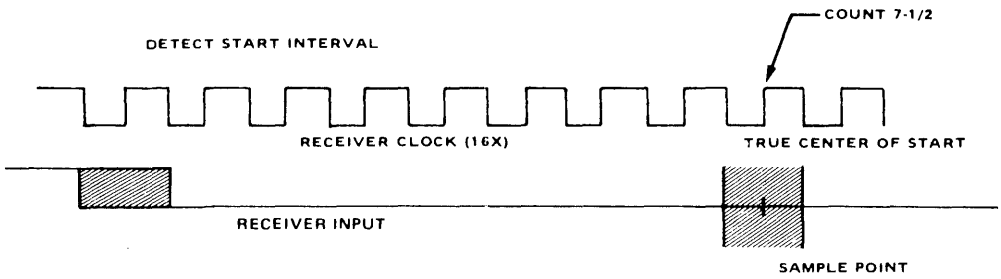


Figure 10.

Since a clock with these characteristics is very easy to obtain, it is apparent that a receiver operating margin of slightly over 45% is very easy to achieve when using the TR1602. Furthermore, this margin is sufficient for virtually all existing transmitters and modems presently in use.

The TR1602 also begins searching for the next start bit exactly in the center of the first stop bit so that minimum character distortions of up to 50% can be accepted.

A break character (null character without a stop bit) will lock the receiver up since it will not begin looking for the next start bit until a stop bit has been received.

TYPICAL TR1602 APPLICATION

The TR1602 is ideally suited for use in distributed computer networks such as is illustrated in Figure 11. One of the primary purposes of the communications controller is to assemble and disassemble the asynchronous characters (required for communication with the data terminals) to/from the parallel data format required by the host computer. Often the communications controller is a micro-computer and character assembly/disassembly is performed by the software. When this is the case, the micro-computer must be interrupted at a rate equal to 8 to 16 times the baud rate of all terminals being handled by the controller. (The actual interrupt rate depends on the amount of distortion that can be experienced on the received characters). When the number of terminals exceeds 8 to 16, even the most powerful micro-computers become overloaded due to the high interrupt rate and the complex algorithms required by the software.

The TR1602 greatly reduces this problem by performing the character assembly/disassembly functions in external hardware as shown in a typical configuration in Figure 12. This solution not only reduces the interrupt rate by a factor of up to 176, but it also greatly reduces the micro-computer load, thus freeing it for other functions.

Since the TR1602 inputs and outputs are TTL compatible, the TR1602 interfaces directly with virtually all micro-computer I/O busses. In Figure 12, the micro-computer Data Output Bus is connected to the Transmitter Register (TR) inputs and the Control Register inputs. When the micro-computer has a character to transmit, the character is placed on the Data Output bus and the address of the appropriate TR1602 is placed on the Device Address Bus. The Address Decode circuit will output a THRL load pulse under control of the Data Out Strobe from the micro-computer. When the control register should be changed, a new 5 bit control word is placed on the Data Output Bus and along with an appropriate device address which is converted to a CRL load pulse in the Address Decode circuits, again under control of the Data Out Strobe. A THRE Pulse to the Interrupt Request circuit will notify the micro-computer when a new character may be provided to the TR1602 for transmission.

When a character has been received, a DR signal to the Interrupt Request circuit will request an interrupt from the micro-computer. The micro-computer will respond by setting the proper device address and provide a Data in Strobe pulse. The Address-Decode circuit then sets the RRD line and SFD line to the appropriate receiver to enable the Data Outputs onto the mini Data Input Bus. The Data in Strobe from the micro-computer then resets the DR signal with a DRR pulse from the Address Decode circuit.

The TR1602 Transmitter Output (TRO) and Receiver Input (RI) must generally be converted to RS232 levels if they interface with a modem as shown in Figure 12. RS232 is a standard that has been established by the Electronic Industries Association for the interface between data terminals and data communications equipment. RS232-C defines a space as greater than 3 volts and a mark as less than negative 3 volts at the Receiver input. A transmitter output of between 5 and 15 volts is a space while a

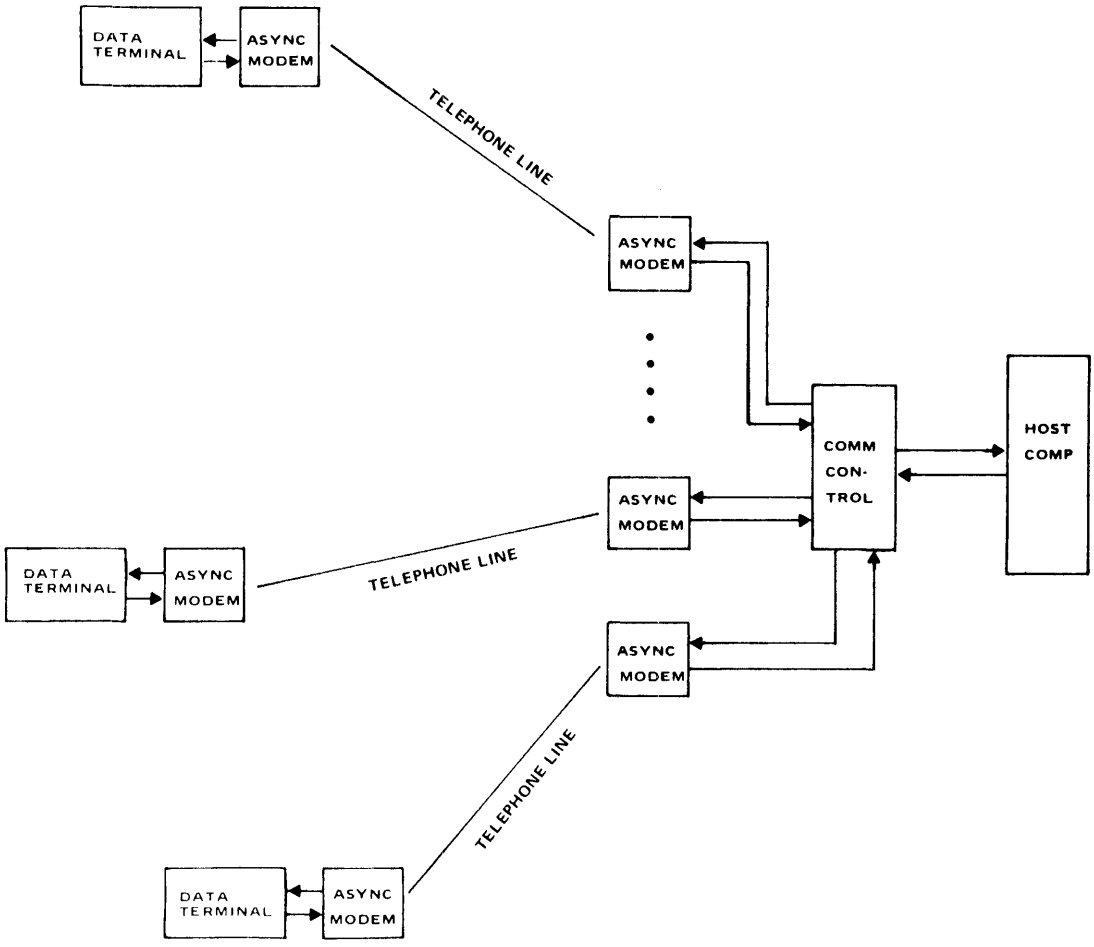


Figure 11.

level between −5 and −15 is a mark. The input/output impedances and signal rise and fall times are also specified by RS232. Fairly simple discrete level translators can be used to convert from the TTL levels to the RS232 levels, or monolithic IC's are also available.

It should be noted that the typical application illustrated in Figure 12 is only one of many and it does not take advantage of many of the TR1602 features. For example, the Status Flags could be tied to a separate interrupt request bus or the TRE output could be used to implement half-duplex operation.

See page 725 for ordering information.

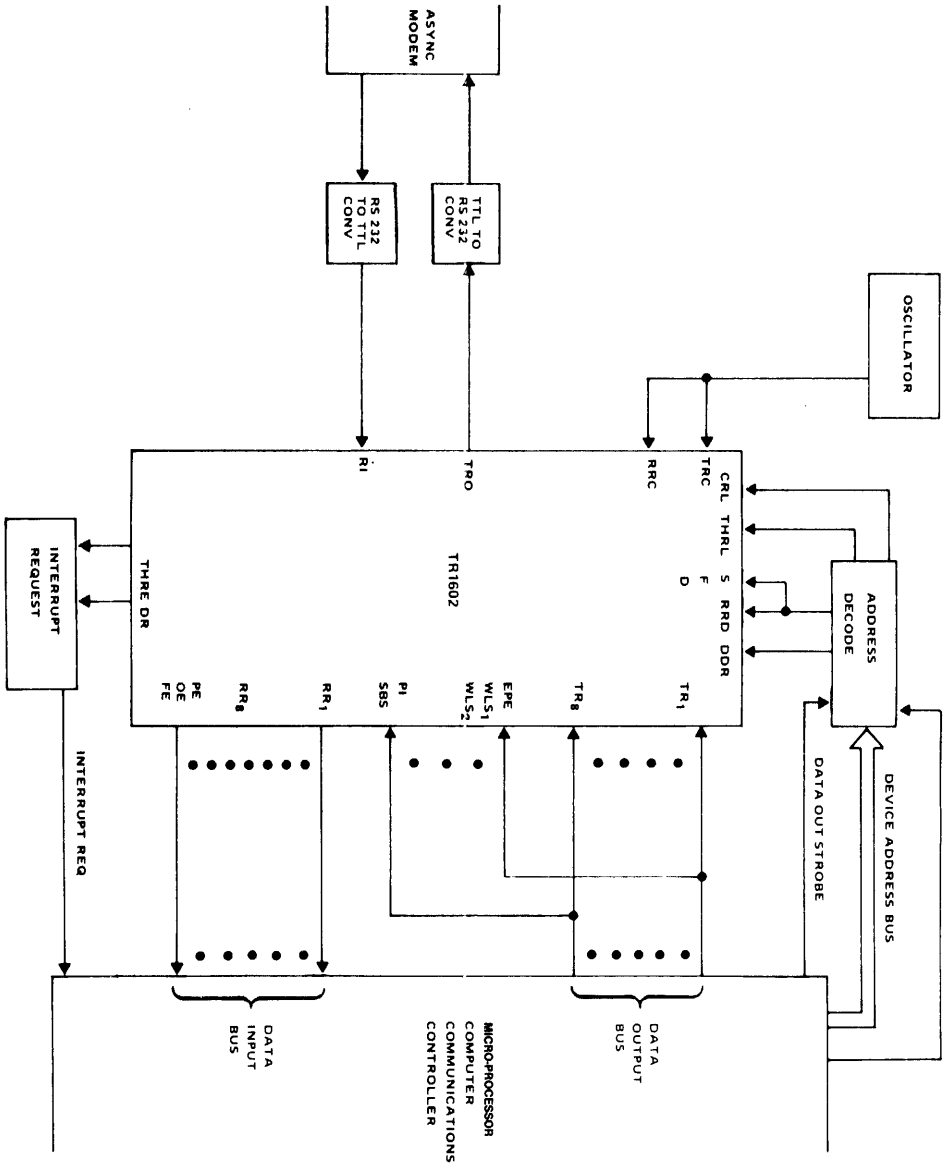


Figure 12. Typical Minicomputer Interface

Printed in U.S.A.

WD1983 (BOART)
Bus Oriented Asynchronous Receiver/Transmitter

FEATURES

ASYNCHRONOUS MODE

- FULL DUPLEX OPERATION
- SELECTABLE 5,6,7, & 8 BIT CHARACTERS
- LINE BREAK DETECTION AND GENERATION
- 1, 1½, or 2 STOP BIT SELECTION
- FALSE START BIT DETECTION
- OVERRUN AND FRAMING ERROR DETECTION
- DC TO 36K BITS/SEC (16X)
- DC TO 600K BITS/SEC (1X)
- 8251/8251A ASYNCHRONOUS ONLY REPLACEMENT
- REQUIRES NO ASYNCHRONOUS SYSTEM CLOCK
- 28 PIN PLASTIC OR CERAMIC
- +5 VOLT ONLY

SYSTEM COMPATIBILITY

- DOUBLE BUFFERING OF DATA
- 8 BIT BI-DIRECTIONAL BUS FOR DATA, STATUS, AND CONTROL WORDS
- ALL INPUTS AND OUTPUTS TTL COMPATIBLE
- CHIP SELECT, $\overline{RE}$, $\overline{WE}$, C/$\overline{D}$ INTERFACE TO CPU
- ON-LINE DIAGNOSTIC CAPABILITY
- THREE STATE DATA BUS

BAUD RATE-DC TO 36K BITS/SEC (16X)
SELECTABLE CLOCK RATES

- 1X, 16X, 64X, BAUD RATE CLOCK INPUTS
- UP TO 47% DISTORTION ALLOWANCE WITH 64X CLOCK

APPLICATIONS

ASYNCHRONOUS COMMUNICATIONS
SERIAL/PARALLEL INTERFACE

GENERAL DESCRIPTION

The WD1983 is an N channel silicon gate MOS/LSI device that interfaces a digital asynchronous channel with a parallel channel. It is available in a ceramic or plastic standard 28 pin dual in line package.

The WD1983 is a fully programmable microprocessor I/O peripheral with two control registers and a status register. It is capable of full duplex operations.

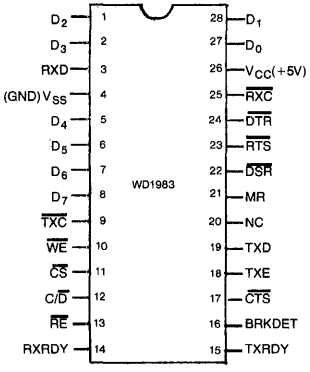


FIGURE 1 WD1983 PIN-OUT

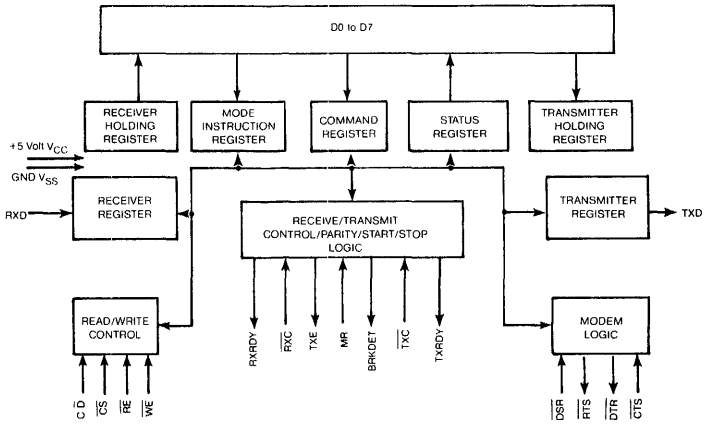


FIGURE 2 WD1983 BLOCK DIAGRAM

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1, 2, 5, 6, 7, 8, 27, 28	DATA BUS	D0 THRU D7	These are input/output pins. Data on the DATA BUS is written into the selected register during a WRITE operation. During a READ operation, the DATA BUS is driven by data in the selected register. When not selected, ($\overline{CS}$ high), these pins are in a high impedance state.
3	RECEIVE DATA	RXD	This input is the received serial data.
4	POWER GND	V_{SS}	Ground
9	TRANSMIT CLOCK	$\overline{TXC}$	This input is the source clock for transmission. MODE INSTRUCTION word bits MR0 & MR1, control 1X, 16X, or 64X, times the transmitted bit rate.
10	WRITE ENABLE	$\overline{WE}$	This input, when low, writes the data on the DATA BUS into the addressed register.
11	CHIP SELECT	$\overline{CS}$	This input, when low, enables READ or WRITE operations.
12	CONTROL/DATA	C/$\overline{D}$	This input selects the CONTROL or DATA register. It is used in conjunction with a READ or WRITE enable.
13	READ ENABLE	$\overline{RE}$	This input, when low, accesses the contents of the addressed register.
14	RECEIVER READY	RXRDY	This output is set low after MASTER RESET. When set high it indicates that the receiver has assembled a character and transferred it to the RECEIVER HOLDING REGISTER. It is automatically reset when the RECEIVER HOLDING REGISTER is read.
15	TRANSMIT READY	TXRDY	This output is set high after MASTER RESET. It indicates that the transmitter is ready to accept a character and is automatically reset whenever a character is written into the TRANSMITTER HOLDING REGISTER.
16	BREAK DETECT	BRKDET	This output is reset after MASTER RESET. It is set high when the receiver detects a string of zeros equal to the programmed character length including start, parity and stop bits. Upon detecting a valid one data bit it's reset. Assembly of the next character is begun after detecting a valid start bit.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
17	CLEAR TO SEND	$\overline{CTS}$	This input is set low to enable the transmitter. When set high it disables transmission. If the transmitter is transmitting a character, it will terminate transmission after the TRANSMITTER REGISTER is empty.
18	TRANSMIT EMPTY	TXE	This output is set high after MASTER RESET and is automatically reset when a character is written into the TRANSMITTER HOLDING REGISTER. It returns high at the end of a transmitted character indicating the end of transmission if the TRANSMIT HOLDING REGISTER has not been loaded.
19	TRANSMIT DATA	TXD	This output is the transmit serial data. When no data is being transmitted or after MASTER RESET, this output is high (a marking condition). COMMAND CONTROL word bit 3 is used to program a break condition by forcing the TXD output to a low (spacing condition).
20		NC	No internal connection, pin not used.
21	MASTER RESET	MR	This input, when high, initializes the device and clears the COMMAND and MODE REGISTERS.
22	DATA SET READY	$\overline{DSR}$	This is a general purpose input which is sensed in STATUS REGISTER bit #7.
23	REQUEST TO SEND	$\overline{RTS}$	This is a general purpose output which is set and cleared by COMMAND word bit CR5. It is reset after MASTER RESET.
24	DATA TERMINAL READY	$\overline{DTR}$	This is a general purpose output which is set and cleared by COMMAND word bit CR1. It is reset after MASTER RESET.
25	RECEIVE CLOCK	$\overline{RXC}$	This input is the receiver clock. MODE INSTRUCTION word bits MR0 & MR1 control whether this input is 1X, 16X or 64X times the received bit rate.
26	POWER SUPPLY	V_{CC}	+5 Volts

ORGANIZATION

The WD1983 Block Diagram is illustrated on Page 1. The WD1983 (BOART) is an eight bit bus-oriented device. Communication between the BOART and the controlling CPU occurs via the 8 bit DATA BUS. There are 2 accessible DATA REGISTERS, which buffer Transmit and Receive DATA. They are the TRANSMIT HOLDING REGISTER and the RECEIVE HOLDING REGISTER. There is a parallel-to-serial shift register (the TRANSMIT REGISTER) and a serial-to-parallel shift register (the RECEIVE REGISTER).

Operational control and monitoring of the BOART is performed by two CONTROL REGISTERS (the COMMAND INSTRUCTION REGISTER and the MODE INSTRUCTION REGISTER) and the STATUS REGISTER.

A READ/WRITE control circuit allows monitoring/programming or reading/loading in the CONTROL, STATUS or HOLDING REGISTERS by activating the appropriate control lines: Chip Select ($\overline{CS}$), Read Enable ($\overline{RE}$), Write Enable ($\overline{WE}$) and Control or Data Select (C/$\overline{D}$).

Internal control of the BOART is by means of two internal MICROCONTROLLERS; one for transmit and one for receive. The CONTROL REGISTERS, MODEM CONTROL LOGIC, READ/WRITE CONTROL LOGIC and various counters provide inputs to the MICROCONTROLLERS, which generate the necessary control signals to send and receive serial data according to the programmed asynchronous format.

READ/WRITE OPERATIONS

The WD1983 must be initialized after a MASTER RESET pulse by first writing the MODE INSTRUCTION word and then the COMMAND INSTRUCTION word. Thereafter, every control write to the device is interpreted as a COMMAND word. If it is desired to re-program the MODE REGISTER, a COMMAND REGISTER bit, INTERNAL RESET (CR6), allows the next control write data to be entered into the MODE REGISTER.

The WD1983 registers are accessed according to the following table:

$\overline{CS}$	C/$\overline{D}$	$\overline{RE}$	$\overline{WE}$	REGISTERS SELECTED
L	L	L	H	Read RECEIVE HOLDING REGISTER
L	L	H	L	Write TRANSMIT HOLDING REGISTER
L	H	L	H	Read STATUS REGISTER
L	H	H	L	Write CONTROL REGISTER
H	X	X	X	DATA BUS tri-stated

Note: "L" means V_{IL} at pins
"H" means V_{IH} at pins
"X" means don't care

OPERATING DESCRIPTION

The WD1983 (BOART) is primarily designed to operate in an 8 bit microprocessor environment, although other control logic schemes are easily implemented. The DATA BUS and the Interface Control Signals ($\overline{CS}$, C/$\overline{D}$, $\overline{RE}$ and $\overline{WE}$) should be connected to the microprocessor's data bus and system control bus. The appropriate $\overline{TXC}$ and $\overline{RXC}$ clock frequencies should be selected for the particular application using a programmable baud rate generator such as the BR1941.

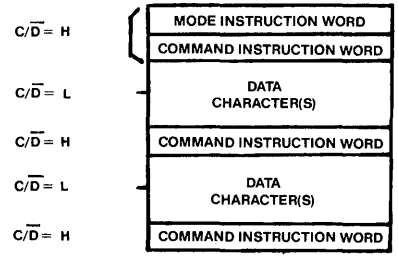
For typical data communication applications, the RXD and TXD input/outputs can be connected to RS-232C interface circuits or a modem.

The TXRDY, RXRDY, TXE and BRKDET Flags may be connected to the microprocessor system as interrupt inputs or the STATUS REGISTER can be periodically read in a polled environment to support BOART operations.

MODEM CONTROL SIGNALS can be configured several ways as the $\overline{DTR}$, $\overline{RTS}$ and $\overline{DSR}$ signals are controlled and sensed by the CPU through the COMMAND and STATUS REGISTERS. The $\overline{CTS}$ input is used to synchronize the transmitter to external events.

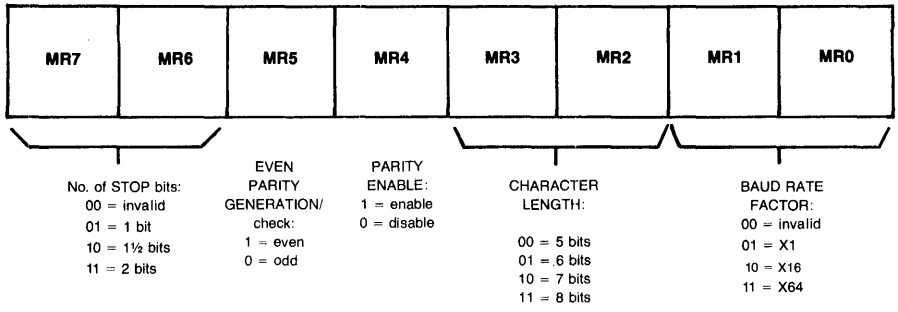
The SBRK bit of the COMMAND REGISTER (CR3) is used to send a Break Character. (A break character is defined as a start bit, and all zero data, parity and stop bits). When the CR3 bit is set to a "1", it causes the transmitter output, TXD, to be forced low after the last word is transmitted.

The receiver is equipped with logic to look for a break character. When a break character is received, the BREAK DETECT (BRKDET) FLAG and STATUS bit are set to logic "1". When the receiver input line goes high again for the least "one data bit time," the receiver resets the BREAK DETECT FLAG and resumes its search for a start bit.



TYPICAL DATA BLOCK TRANSFER

MODE INSTRUCTION CONTROL WORD FORMAT



COMMAND INSTRUCTION CONTROL WORD FORMAT

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
DON'T CARE	INTERNAL RESET (IR): 1 = returns WD1983 to mode instruction word format	REQUEST TO SEND ($\overline{RTS}$): 1 = forces $\overline{RTS}$ output low 0 = forces $\overline{RTS}$ output high	ERROR RESET (ER): 1 = resets PE, OE & FE error flags 0 = normal operation	SEND BREAK CHARACTER (SBRK): 1 = forces TXD output low 0 = normal operation	RECEIVE ENABLE (RXE): 1 = enable receiver 0 = disable receiver	DATA TERMINAL READY ($\overline{DTR}$): 1 = forces $\overline{DTR}$ output low 0 = forces $\overline{DTR}$ output	TRANSMIT ENABLE TXEN: 1 = enable transmitter 0 = disable transmitter

STATUS WORD FORMAT

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
$\overline{DSR}$ (SEE NOTE)	BRKDET (SEE NOTE)	FRAMING ERROR (FE): 1 = invalid stop bit detected at the end of the character 0 = No framing error detected (Reset by CR4)	OVERRUN ERROR (OE): 1 = CPU did not read the character before the next one became available 0 = No overrun error detected (Reset by CR4)	PARITY ERROR (PE): 1 = parity error detected 0 = No Parity error detected (Reset by CR4)	TXE (SEE NOTE)	RXRDY (SEE NOTE)	TXRDY (SEE NOTE)

FE, OE & PE FLAGS DO NOT INHIBIT OPERATION. THESE FLAGS ARE STATUS ONLY.

NOTE:
SR0, SR1, SR2, SR6, and SR7 HAVE IDENTICAL MEANINGS AS THE EXTERNAL OUTPUT PINS.

ABSOLUTE MAXIMUM RATINGS

V_{DD} with Respect to V_{SS} (Ground) + 15 to −0.3V
Max. Voltage to any Input with Respect to V_{SS} + 20 to −0.3V
Power Dissipation 1000 MW

Storage Temp.
Ceramic -65°C to +150°C ('E' Package)
Plastic -55°C to +125°C ('F' Package)

OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = + 5.0V ± .25V, V_{SS} = 0V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{CC}$
I_{DL}	Data Bus Leakage			50	μA	Data Bus is in high impedence state
ICC_{AVE}	V_{CC} Supply Current		45	80	mA	5.25 VDC/f_{CLK} = 600 kHz No Loads.
V_{IH}	Input High Voltage	2.4		0.8	V	
V_{IL}	Input Low Voltage (All Inputs)	−0.3			V	
V_{OH}	Output High Voltage	2.4			V	I_O = − 100μA (source)
V_{OL}	Output Low Voltage			0.45	V	I_O = 1.6 mA (sink)

TABLE 1 WD1983 DC CHARACTERISTICS

FIGURE 3 INPUT WAVEFORMS FOR AC TESTS

NOTE: ALL WAVEFORMS ARE MEASURED AT 2.0V IF RISING EDGE, AND 0.8V IF FALLING EDGE.

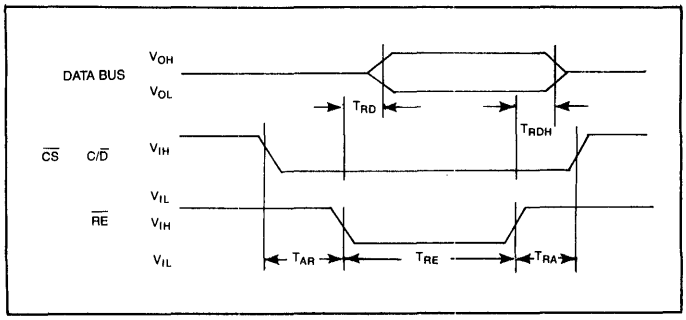


FIGURE 4 READ TIMING

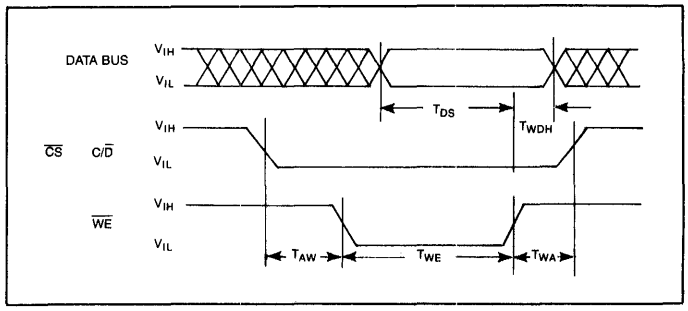


FIGURE 5 WRITE TIMING

NOTE:

8251A COMPATIBILITY

The WD1983 (BOART) is an asynchronous only device, which is compatible with the 8251A. However, in test evaluation and application, the following differences should be noted:

(1) The WD1983 utilizes the transmit and receive baud clocks in their respective internal logic sections instead of the system clock normally applied to Pin 20 on the 8251A. This Pin on the WD1983 is not used.

(2) As a result of the above condition, timings referenced to the system clock period in the 8251A specification are now specified in absolute time units or with respect to the transmit or receive baud clock.

AC Electrical Characteristics
T_A = 0°C to + 70°C; V_{CC} = 5.0 V ± 5%; GND = 0 V

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
BUS PARAMETERS READ CYCLE					
t_{AR}	Address Stable Before $\overline{RE}$ ($\overline{CS}$,C/$\overline{D}$)	50		ns	
t_{RA}	Address Hold Time for $\overline{RE}$ ($\overline{CS}$,C/$\overline{D}$)	5		ns	
t_{RE}	$\overline{RE}$ Pulse Width	350		ns	
t_{RD}	Data Delay from $\overline{RE}$		200	ns	C_L = 50pF
t_{RDH}	$\overline{RE}$ to Data Floating	25	200	ns	C_L (Max) = 50pF C_L (Min) = 15pF
WRITE CYCLE					
t_{AW}	Address Stable Before $\overline{WE}$	20		ns	
t_{WA}	Address Hold Time for $\overline{WE}$	20		ns	
t_{WE}	$\overline{WE}$ Pulse Width	350		ns	
t_{DS}	Data Set-Up Time for $\overline{WE}$	200		ns	
t_{WDH}	Data Hold Time for $\overline{WE}$	40		ns	
OTHER TIMINGS					
t_{DTX}	TXD Delay from Falling Edge of TXC		200	ns	C_L = 100pF
t_{SRX}	RX Data Set-Up Time to Sampling Pulse	200		ns	C_L = 100pF
t_{HRX}	RX Data Hold Time to Sampling Pulse	100		ns	C_L = 100pF
f_{TX} [1]	Transmitter Input Clock Frequency				
	1X Baud Rate	DC	500	kHz	
	16X and 64X Baud Rate	DC	600	kHz	
t_{TPW}	Transmitter Input Clock Pulse Width				
	1X Baud Rate	1.0		μs	
	16X and 64X Baud Rate	500		ns	

TABLE 2 WD1983 AC CHARACTERISTICS (CONTINUED)

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1X Baud Rate	1.0		μs	
	16X and 64X Baud Rate	800		ns	
f_{RX}	Receiver Input Clock Frequency				
	1X Baud Rate	DC	500	kHz	
	16X and 64X Baud Rate	DC	600	kHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1X Baud Rate	1.0		μs	
	16X and 64X Baud Rate	500		ns	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1X Baud Rate	1.0		μs	
	16X and 64X Baud Rate	800		ns	
t_{TX}	TXRDY Delay from Center of Data Bit		8	t_{RXC}	C_L = 50pF (16X)
t_{RX}	RXRDY Delay from Center of Data Bit		1/2	t_{RXC}	
t_{IS}	Internal BRKDET Delay from Center of Data Bit		1	t_{RXC}	
t_{TRD}	TXRDY Delay from Falling Edge of $\overline{WE}$		1	t_{TXC}	
t_{TOD}	TXD Output from Falling Edge of $\overline{WE}$		2	t_{TXC}	
t_{WC}	Control Delay from Rising Edge of $\overline{WE}$ ($\overline{DTR}$, $\overline{RTS}$)		400	ns	
t_{CR}	Control to $\overline{RE}$ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)		500	ns	

TABLE 2 WD1983 AC CHARACTERISTICS

At f_{TX} (max), the duty cycle should be 50%. At less than f_{TX} (max), the minimum pulse width for the high or low half is $\frac{1}{2 \bullet f_{TX}(max)}$.
Hence, at frequencies less than f_{TX} (max), the required duty cycle will be less stringout than 50%.

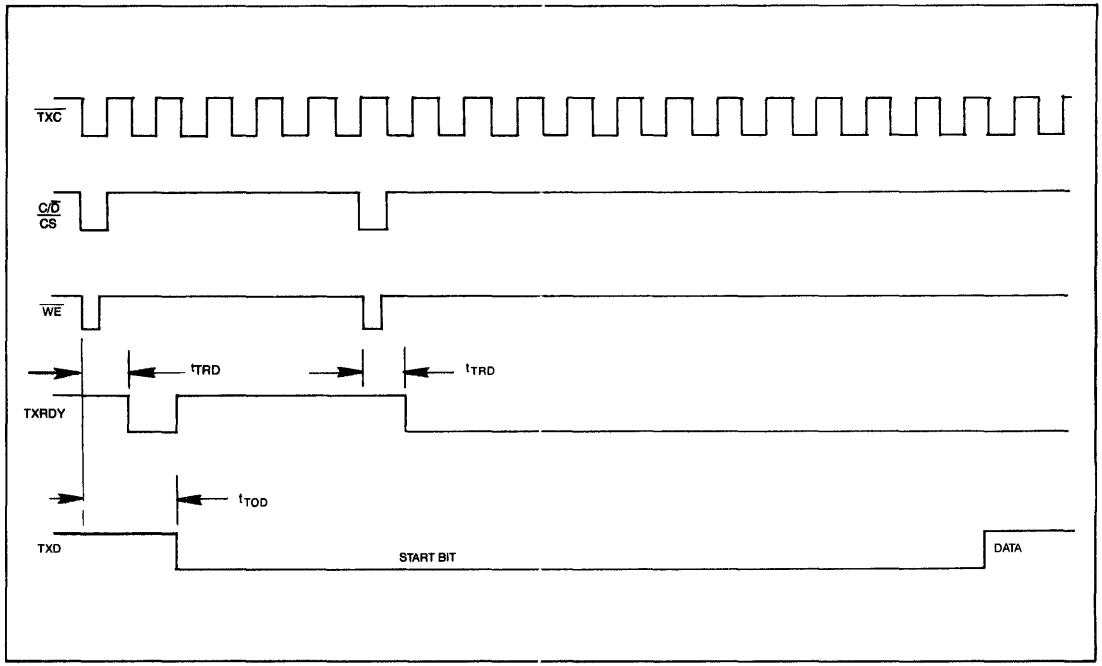


FIGURE 6

TRANSMITTER OUTPUT TIMINGS WITH RESPECT TO TRANSMIT CLOCK

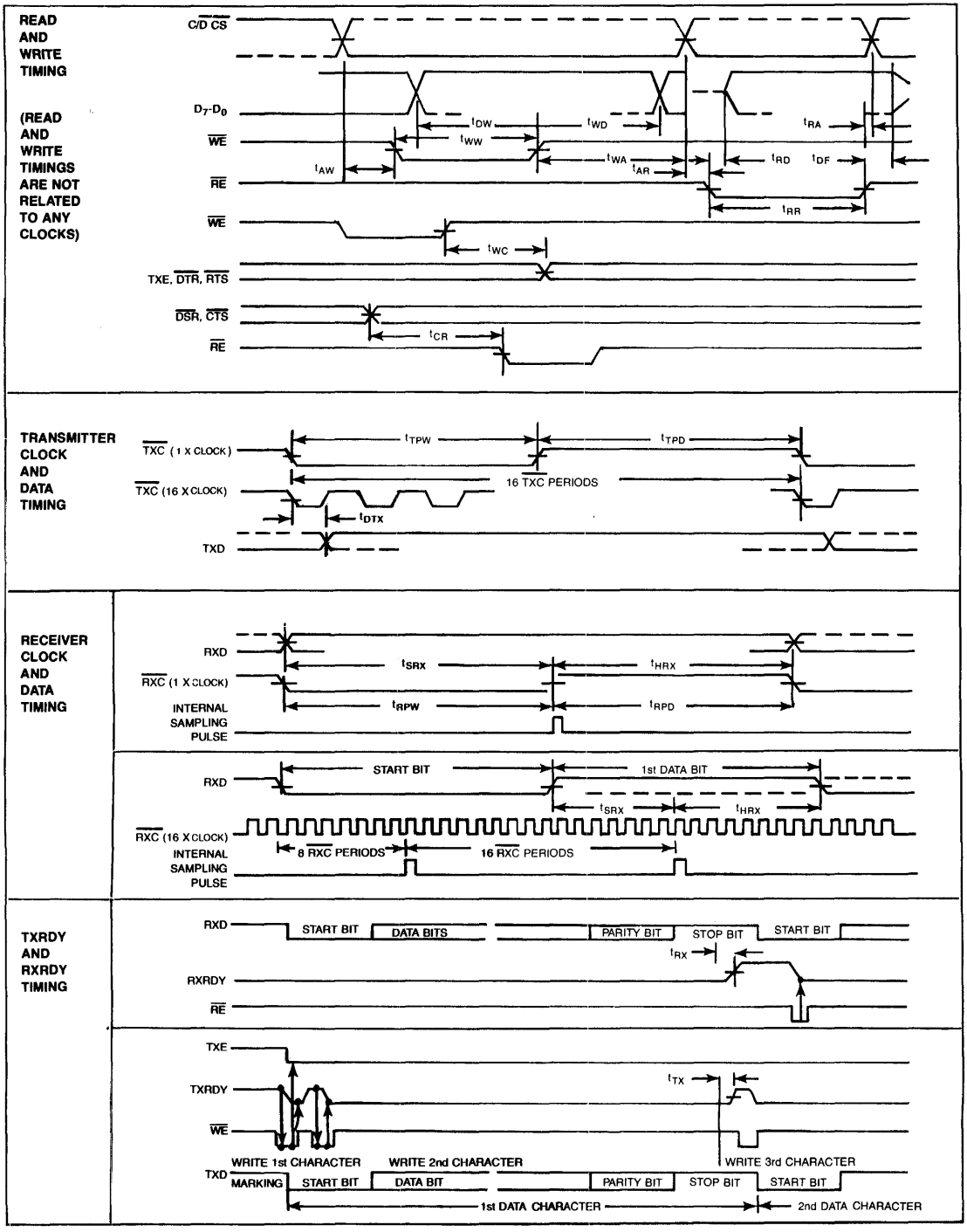


FIGURE 7 SYSTEM TIMING DIAGRAMS

See page 725 for ordering information.

Printed in U.S.A.

WD8250 Asynchronous Communications Element

FEATURES

- Designed to be Easily Interfaced to Most Popular Microprocessors (Z-80, 8080A, 6800, etc.)
- Full Double Buffering
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Programmable Baud Rate Generator Allows Division of Any Input Clock by 1 to (2^{16} - 1) and Generates the Internal 16x Clock
- Independent Receiver Clock Input
- Fully Programmable Serial-Interface Characteristics
  - —5-, 6-, 7-, or 8-Bit Characters
  - —Even, Odd, or No-Parity Bit Generation and Detection
  - —1-, 1½-, or 2-Stop Bit Generation
  - —Baud Rate Generation (DC to 56K Baud)
- False Start Bit Detector
- Complete Status Reporting Capabilities
- THREE-STATE TTL Drive Capabilities for Bi-directional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities
  - —Loopback Controls for Communications Link Fault Isolation
  - —Break, Parity, Overrun, Framing Error Simulation
- Full Prioritized Interrupt System Controls
- Single +5-Volt Power Supply

GENERAL DESCRIPTION

The WD8250 is a programmable Asynchronous Communication Element (ACE) in a 40-pin package. The device is fabricated in N/MOS silicon gate technology.

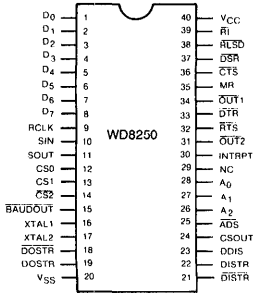
The ACE is a software-oriented device using a three-state 8-bit bi-directional data bus.

The ACE is used to convert parallel data to a serial format on the transmit side, and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and one half (five bit format only) or two stop bits. The maximum recommended data rate is 56K baud.

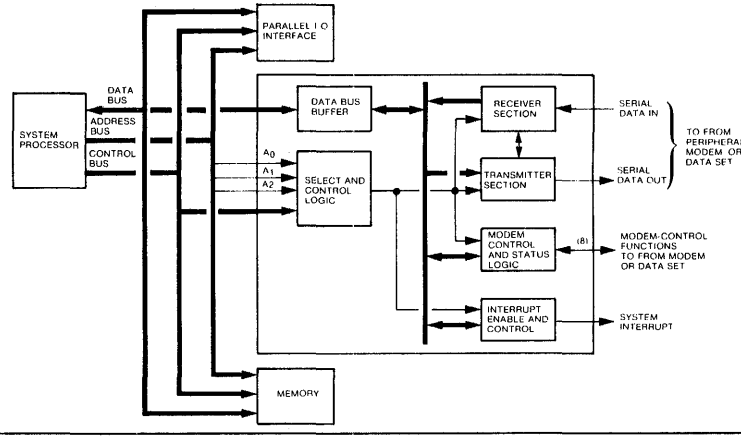
Internal registers enable the user to program various types of interrupts, modem controls, and character formats. The user can read the status of the ACE at any time monitoring word conditions, interrupts and modem status.

An additional feature of the ACE is a programmable baud rate generator that is capable of dividing an internal XTAL or TTL signal clock by a division of 1 to 2^{16} – 1.

The ACE is designed to work in either a polling or interrupt driven system, which is programmable by users software controlling an internal register.



PIN CONNECTIONS



WD8250 GENERAL SYSTEM CONFIGURATION

PIN DEFINITIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1-8	DATA BUS	D0-D7	3-state input/output lines. Bi-directional communication lines between WD8250 and Data Bus. All assembled data TX and RX, control words, and status information are transferred via the D0-D7 data bus.
9	RECEIVE CLK.	RCLK	This input is the 16X baud rate clock for the receiver section of the chip (may be tied to BAUDOUT pin 15).
10	SERIAL INPUT	SIN	Received Serial Data In from the communications link (Peripheral device, modem or data set).
11	SERIAL OUTPUT	SOUT	Transmitted Serial Data Out to the communication link. The SOUT signal is set to a (logic 1) marking condition upon a MASTER RESET.
12 13 14	CHIP SELECT CHIP SELECT CHIP SELECT	CS0 CS1 $\overline{CS2}$	When CS0 and CS1 are high, and $\overline{CS2}$ is low, chip is selected. Selection is complete when the address strobe $\overline{ADS}$ latches the chip select signals.
15	BAUDOUT	$\overline{BAUDOUT}$	16X clock signal for the transmitter section of the WD8250. The clock rate is equal to the oscillator frequency divided by the divisor loaded into the divisor latches. The BAUDOUT signal may be used to clock the receiver by tying to (pin 9) RCLK.
16 17	EXTERNAL CLOCK IN EXTERNAL CLOCK OUT	XTAL 1 XTAL 2	These pins connect the crystal or signal clock to the WD8250 baud rate divisor circuit. See Fig. 3 and Fig. 4 for circuit connection diagrams.
18 19	DATA OUT STROBE DATA OUT STROBE	$\overline{DOSTR}$ DOSTR	When the chip has been selected, a low $\overline{DOSTR}$ or high DOSTR will latch data into the selected WD8250 register (a CPU write). Only one of these lines need be used. Tie unused line to its inactive state. $\overline{DOSTR}$ — high or DOSTR — low.
20	GROUND	V_{SS}	System signal ground.
21 22	DATA IN STROBE DATA IN STROBE	$\overline{DISTR}$ DISTR	When chip has been selected, a low $\overline{DISTR}$ or high DISTR will allow a read of the selected WD8250 register (a CPU read). Only one of these lines need be used. Tie unused line to its inactive state. $\overline{DISTR}$ — high or DISTR — low.
23	DRIVER DISABLE	DDIS	Output goes low whenever data is being read from the WD8250. Can be used to reverse data direction of external transceiver.
24	CHIP SELECT OUT	CSOUT	Output goes high when chip is selected. No data transfer can be initiated until CSOUT is high.
25	ADDRESS STROBE	$\overline{ADS}$	When low, provides latching for register. Select (A0, A1, A2) and chip select (CS0, CS1, $\overline{CS2}$) NOTE: An active $\overline{ADS}$ signal is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, the $\overline{ADS}$ input can be tied permanently low.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
26 27 28	REGISTER SELECT A2 REGISTER SELECT A1 REGISTER SELECT A0	A2 A1 A0	These three inputs are used to select a WD8250 internal register during a data read or write. See Table below.
29	NO CONNECT	NC	No Connect
30	INTERRUPT	INTRPT	Output goes high whenever an enabled interrupt is pending.
31	OUTPUT 2	$\overline{OUT2}$	User-designated output that can be programmed by Bit 3 of the modem control register = 1, causes $\overline{OUT2}$ to go low.
32	REQUEST TO SEND	$\overline{RTS}$	Output when low informs the modem or data set that the WD8250 is ready to transmit data. See Modem Control Register.
33	DATA TERMINAL READY	$\overline{DTR}$	Output when low informs the modem or data set that the WD8250 is ready to communicate.
34	OUTPUT 1	$\overline{OUT1}$	User designated output can be programmed by Bit 2 of Modem Control Register = 1 causes $\overline{OUT1}$ to go low.
35	MASTER RESET	MR	When high clears the registers to states as indicated in Table 1.
36	CLEAR TO SEND	$\overline{CTS}$	Input from DCE indicating remote device is ready to transmit. See Modem Control Register.
37	DATA SET READY	$\overline{DSR}$	Input from DCE used to indicate the status of the local data set. See Modem Control Register.
38	RECEIVED LINE SIGNAL DETECT	$\overline{RSLD}$	Input from DCE indicating that it is receiving a signal which meets its signal quality conditions. See Modem Control Register.
39	RING INDICATOR	$\overline{RI}$	Input, when low, indicates that a ringing signal is being received by the modem or data set. See Modem Control Register.
40	+5V	V_{CC}	+5 Volt Supply.

CHIP SELECTION AND REGISTER ADDRESSING

Address Strobe (ADS pin 25): When low provides latching for register select (A0, A1, A2) and chip select (CS0, CS1, $\overline{CS2}$).

NOTE: An active $\overline{ADS}$ input is required when register select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If $\overline{ADS}$ is not required for latching, tie this input permanently low.

Chip Select (CS0, CS1, $\overline{CS2}$) pins 12-14: The definition of chip selected is CS0, CS1 both high and $\overline{CS2}$ is low. Chip selection is complete when latched by $\overline{ADS}$ or $\overline{ADS}$ is tied low.

Register Select (A0, A1, A2) pins 26-28: To select a register for read or write operation, see Register Table.

NOTE: (DLAB) Divisor Latch access bit is the MSB of the Line Control Register. DLAB must be programmed high logic 1 by the system software to access the Baud Rate Generator Divisor Latches.

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	None
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

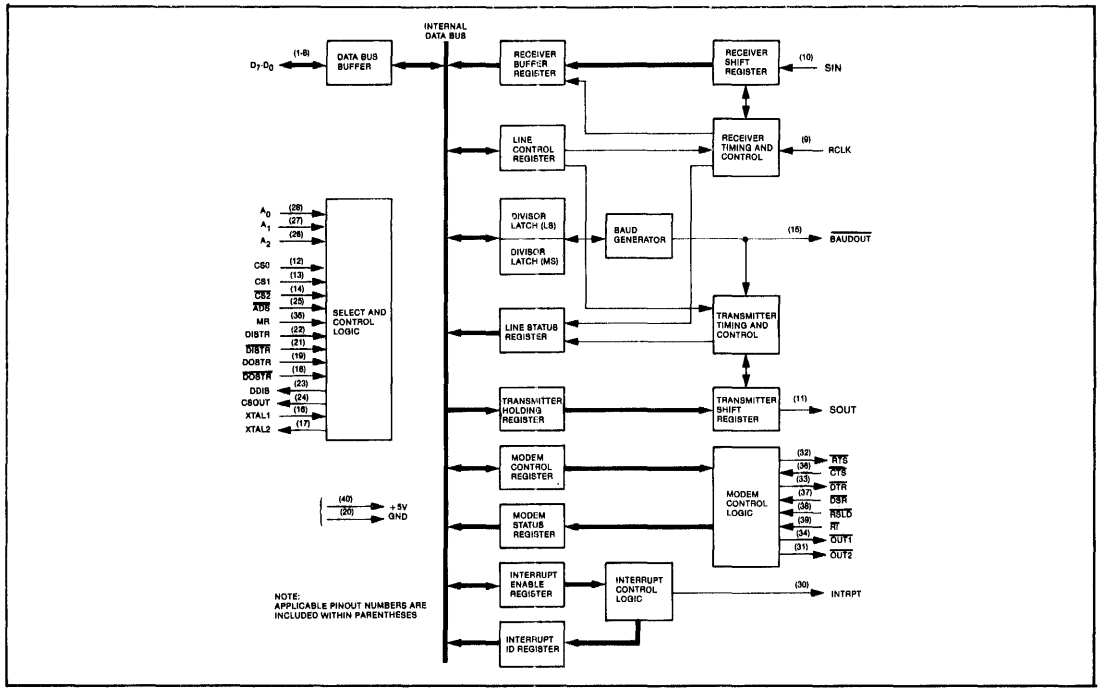
WD8250 OPERATIONAL DESCRIPTION

Master Reset

A high-level input on pin 35 causes the WD8250 to reset to the condition listed in Table 1.

WD8250 Accessible Registers

The system programmer has access to any of the registers summarized in Table 2. For individual register descriptions, refer to the following pages under register heading.



WD8250 BLOCK DIAGRAM

Table 1. Reset Control of Registers and Pinout Signals

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High and Bits 1-7 Are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 and 6 Are High
Modem Status Register	Master Reset MODEM Signal Inputs	Bits 0-3 Low Bits 4-7 — Input Signal
Divisor Latch (low order bits)	Writing into the Latch	Data
Divisor Latch (high order bits)	Writing into the Latch	Data
SOUT	Master Reset	High
$\overline{\text{BAUDOUT}}$	Writing into either Divisor Latch	Low
CSOUT	$\overline{\text{ADS}}$ Strobe Signal and State of Chip Select Lines	High/Low
DDIS	DDIS = $\overline{\text{CSOUT}} \cdot \text{RCLK} \cdot \overline{\text{DISTR}}$ (At Master Reset, the CPU sets RCLK and DISTR low.)	High
INTRPT	Master Reset	Low

$\overline{OUT\ 2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT\ 1}$	Master Reset	High
D7-D0 Data Bus Lines	In THREE-STATE Mode, Unless CSOUT • DISTR = High or CSOUT • DOSTR = High	THREE-STATE Data (ACE to CPU) Data (CPU to ACE)

Table 2. Summary of WD8250 Accessible Registers

	Register Address									
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	3	4	5	6	0 DLAB=1	1 DLAB=1
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Divisor Latch (LS)	Divisor Latch (MS)
0	Data Bit 0*	**Data Bit 0***	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DSLSD)	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Shift Register Empty (TSRE)	Ring Indicator (RI)	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Received Line Signal Detect (RLSD)	Bit 7	Bit 15

*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Line Control Register

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1½ Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. The feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

WD8250 Programmable Baud Rate Generator

The WD8250 contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3.1 MHz) and dividing it by any divisor from 1 to (2^{16} - 1). The output frequency of the Baud Generator is 16x the Baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Generator with two different driving frequencies. One is referenced to a 1.8432 MHz crystal. The other is a 3.072 MHz crystal.

NOTE

The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 6 and below, the maximum frequency is equal to 1/2 the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1/2 MHz. In no case should the data rate be greater than 56K Baud.

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of

Table 3. Baud Rates Using 1.8432 MHz Crystal.

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

NOTE: 1.8432 MHz is the standard 8080 frequency divided by 10.

Table 4. Baud Rates Using 3.072 MHz Crystal.

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired and Actual
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	—
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.23
9600	20	—
19200	10	—
38400	5	—
56000	3	14.285

the Line Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 may be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits).

NOTE

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the WD8250 is ready to accept a new character for transmission. In addition, this bit causes the WD8250 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register. Bit 6 is a read-only bit.

Bit 7: This bit is permanently set to logic 0.

Interrupt Identification Register

The WD8250 has an on chip interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the WD8250 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and source of that interrupt are stored in the Interrupt Identification Register (refer to table 5). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in table 5.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four interrupt sources of the WD8250 to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interurpt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1. Bit 0 is reset to logic 0 upon completion of a read of the Receiver Buffer Register.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to a logic 1. Bit 1 is reset to logic 0 upon a write to the Transmitter Holding Register.

Table 5. Interrupt Control Functions.

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1. Bit 2 is reset to logic 0 upon completion of the associated interrupt service routine.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1. Bit 3 is reset to logic 0 upon completion of the associated interrupt service routine.

Bits 4 through 7: These four bits are always logic 0.

MODEM Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in table 2 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

NOTE

The $\overline{DTR}$ output of the WD8250 may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a loopback feature for diagnostic testing of the WD8250. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the HIGH IMPEDANCE state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the WD8250.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The WD8250 interrupt system can be tested by writing into the lower six bits of the Line Status Register

and the lower four bits of the MODEM Status Register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal WD8250 operation. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to logic 0.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the $\overline{RLSD}$ input to the chip has changed state.

NOTE

Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input.

Bit 7: This bit is the complement of the Received Line Signal Detect ($\overline{RLSD}$) input.

Typical Applications

Figures 1 and 2 show how to use the WD8250 chip in an 8080A system and in a microcomputer system with a high-capacity data bus.

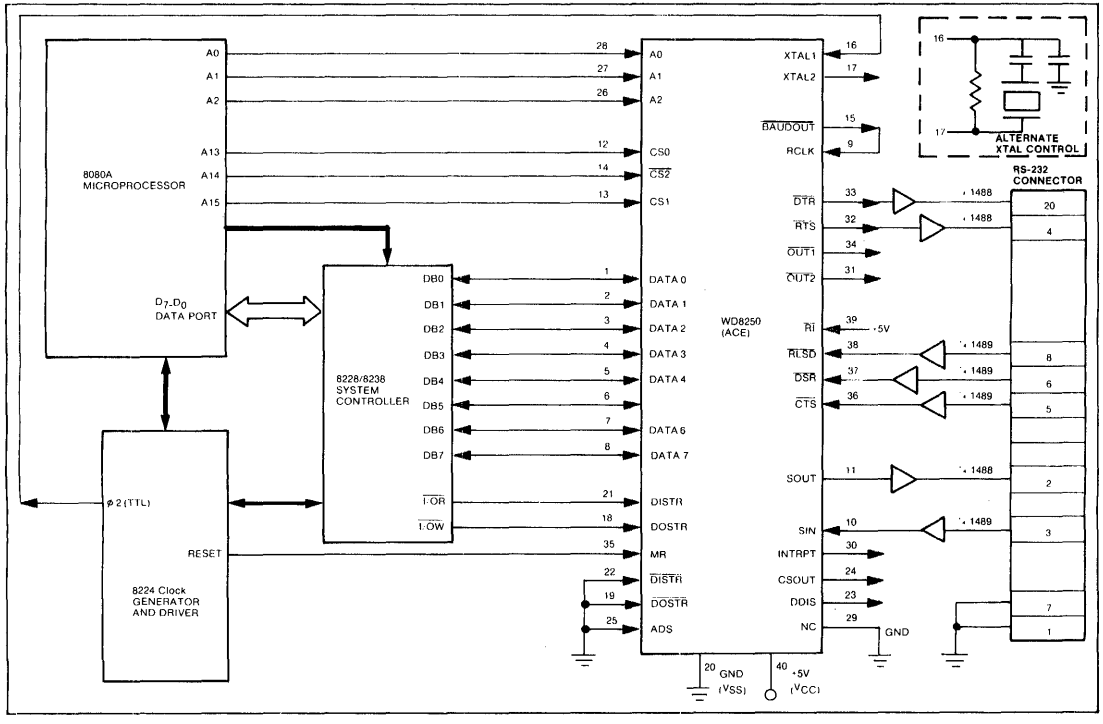


FIGURE 1. TYPICAL 8-BIT MICROPROCESSOR/RS-232 TERMINAL INTERFACE USING THE ACE.

Typical Applications (continued)

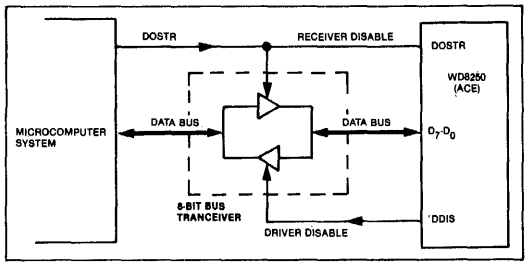


FIGURE 2. TYPICAL INTERFACE FOR A HIGH-CAPACITY DATA BUS.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature -65°C to +150°C (Ceramic)
-50°C to +125°C (Plastic)
All Input or Output Voltages with
Respect to V_{SS} ..... -0.5 V to +7.0 V
Power Dissipation ..... 750 mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{SS} = 0V, unless otherwise specified.

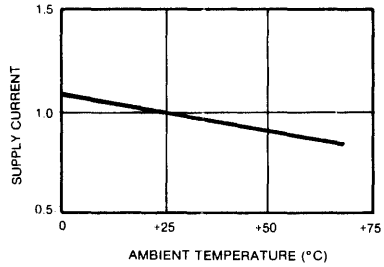
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V_{ILX}	Clock Input Low Voltage	-0.5		0.8	V	
V_{IHX}	Clock Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.4		V_{CC}	V	
V_{OL}	Output Low Voltage			.45	V	I_{OL}=1.6mA on all outputs
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-100 μA
$I_{CC(AV)}$	Avg Power Supply Current (V_{CC})			150	ma	
I_{IL}	Input Leakage			± 10	μA	
I_{CL}	Clock Leakage			± 10	μA	
I_{DL}	Data Bus Leakage			± 10	μA	V_{OUT} = 0.4V, V_{OUT} = 4.6V: Data Bus is at High-Impedance State

Capacitance

T_A = 25°C, V_{CC} = V_{SS} = 0V

Symbol	Parameter	Typ.	Max.	Units	Test Conditions
C_{XIN}	Clock Capacitance	10	15	pF	fc=1 MHz, Unmeasured pins returned to V_{SS}
C_{IN}	Input Capacitance	6	10	pF	
C_{OUT}	Output Capacitance	10	20	pF	

Typical Supply Current vs. Temperature, Normalized

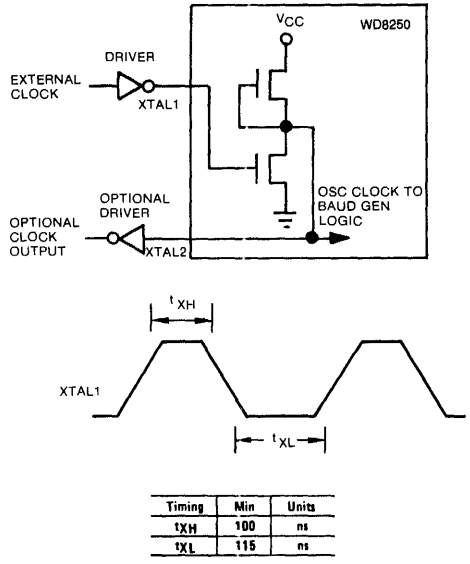


AC Electrical Characteristic $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Units	Min	Max	Test Conditions
t_{AW}	Address Strobe Width	ns	120		1TTL Load
t_{ACS}	Address and Chip Select Setup Time	ns	100		1TTL Load
t_{AH}	Address Hold Time	ns	0		1TTL Load
t_{CSS}	Chip Select Output Delay from Latch	ns		160	1TTL Load
t_{DID}	$\overline{DISTR}$/DISTR Delay from Latch	ns	50		1TTL Load
t_{DIW}	$\overline{DISTR}$/DISTR Strobe Width	ns	300		1TTL Load
t_{RC}	Read Cycle Delay	ns	655		1TTL Load
RC	Read Cycle = $t_{ACS} + t_{DID} + t_{DIW} + t_{RC} + 20$ ns	ns	1125		1TTL Load
t_{DD}	$\overline{DISTR}$/DISTR to Driver Disable Delay	ns		200	1TTL Load
t_{DDD}	Delay from $\overline{DISTR}$/DISTR to Data	ns		300	1TTL Load
t_{HZ}	$\overline{DISTR}$/DISTR to Floating Data Delay	ns	60		1TTL Load
t_{DOD}	$\overline{DOSTR}$/DOSTR Delay From Latch	ns	20		1TTL Load
t_{DOW}	$\overline{DOSTR}$/DOSTR Strobe Width	ns	175		1TTL Load
t_{WC}	Write Cycle Delay	ns	685		1TTL Load
WC	Write Cycle = $t_{ACS} + t_{DOD} + t_{DOW} + t_{WC} + 20$ ns	ns	1000		1TTL Load
t_{DS}	Data Setup Time	ns	175		1TTL Load
t_{DH}	Data Hold Time	ns	60		1TTL Load
t_{CSC}	Chip Select Output Delay from Select	ns		260	1TTL Load
t_{DIC}	$\overline{DISTR}$/DISTR Delay from Select	ns	150		1TTL Load
t_{DOC}	$\overline{DOSTR}$/DOSTR Delay from Select	ns	150		1TTL Load

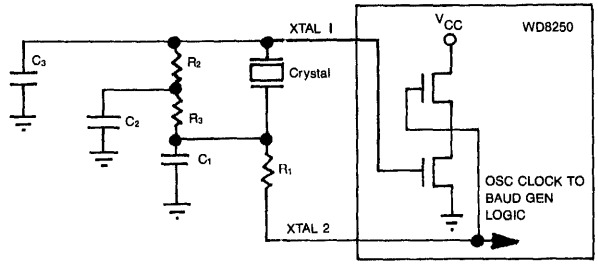
Symbol	Parameter	Min.	Max.	Units	Test Conditions
Baud Generator					
N	Baud Rate Divisor	1	$2^{16}-1$		
t_{BLD}	Baud Output Negative Edge Delay		250 typ	ns	100pF Load
t_{BHD}	Baud Output Positive Edge Delay		250 typ	ns	100pF Load
t_{LW}	Baud Output Down Time	425 Typ		ns	100pF Load
t_{HW}	Baud Output Up Time	330 Typ		ns	100pF Load
Receiver					
t_{SCD}	Delay from RCLK to Sample Time		2 typ	μs	
t_{SINT}	Delay from Stop to Set Interrupt		2 typ	μs	100pF Load
t_{RINT}	Delay from $\overline{DISTR}$/DISTR (RD RBR) to Reset Interrupt	.250	1 typ	μs	100pF Load
Transmitter					
t_{HR}	Delay from $\overline{DOSTR}$/DOSTR (WR THR) to Reset Interrupt	.250	1 typ	μs	100pF Load
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		16 typ	$\overline{BAUDOUT}$ Cycles	
t_{SI}	Delay from Initial Write to Interrupt		24 typ	$\overline{BAUDOUT}$ Cycles	
t_{SS}	Delay from Stop to Next Start	.250	1 typ	μs	
t_{STI}	Delay from Stop to Interrupt (THRE)		8 typ	$\overline{BAUDOUT}$ Cycles	
TIR	Delay from $\overline{DISTR}$/DISTR (RD IIR) to Reset Interrupt (THRE)	.250	1 typ	μs	100pF Load
Modem Control					
t_{MDO}	Delay from DOSTR/$\overline{DOSTR}$ (WR MCR) to Output	.250	1 typ	μs	100pF Load

t_{SIM}	Delay to Set Interrupt from MODEM Input	.250	1 typ	μs	100pF Load
t_{RIM}	Delay to Reset Interrupt from $\overline{DISTR}$/DISTR (RD MSR)	.250	1 typ	μs	100pF Load



Timing	Min	Units
t_{XH}	100	ns
t_{XL}	115	ns

FIGURE 3. EXTERNAL CLOCK INPUT (3.1 MHz MAX.)



Crystal	R_1	R_2	R_3	C_1	C_2	C_3
3.1 MHz	2K	O.SM	O.SM	40-60pF	O.OuF	10-30pF

FIGURE 4. TYPICAL CRYSTAL OSCILLATOR NETWORK

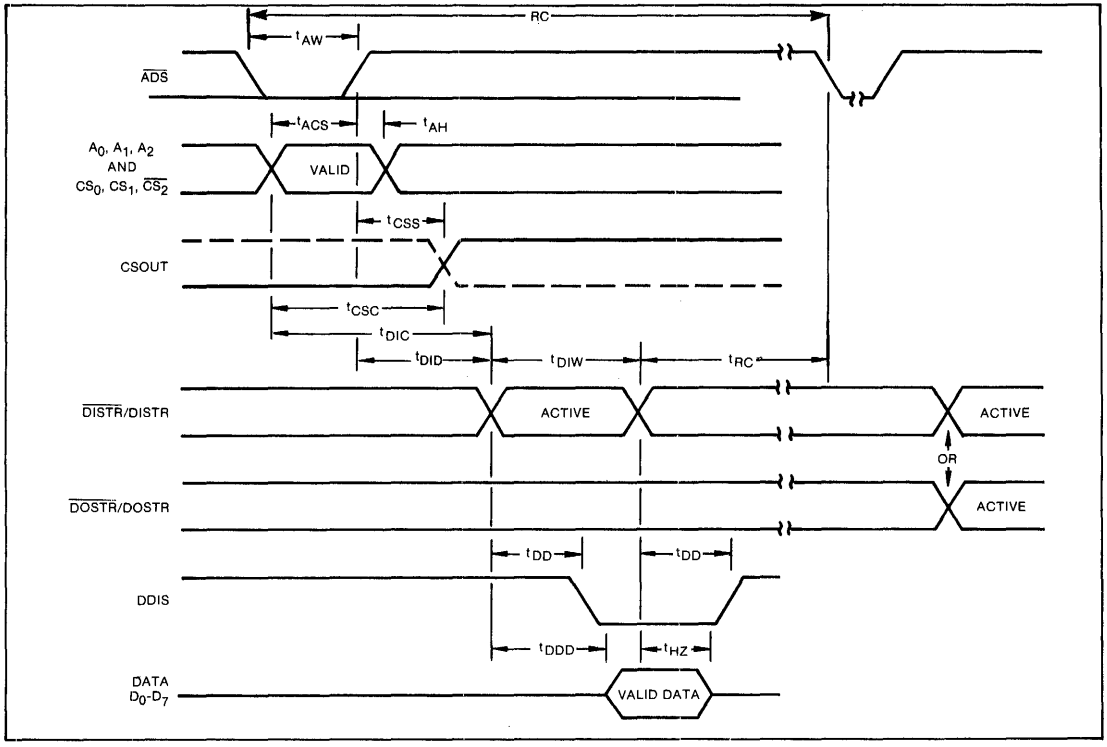


FIGURE 5. READ CYCLE TIMING

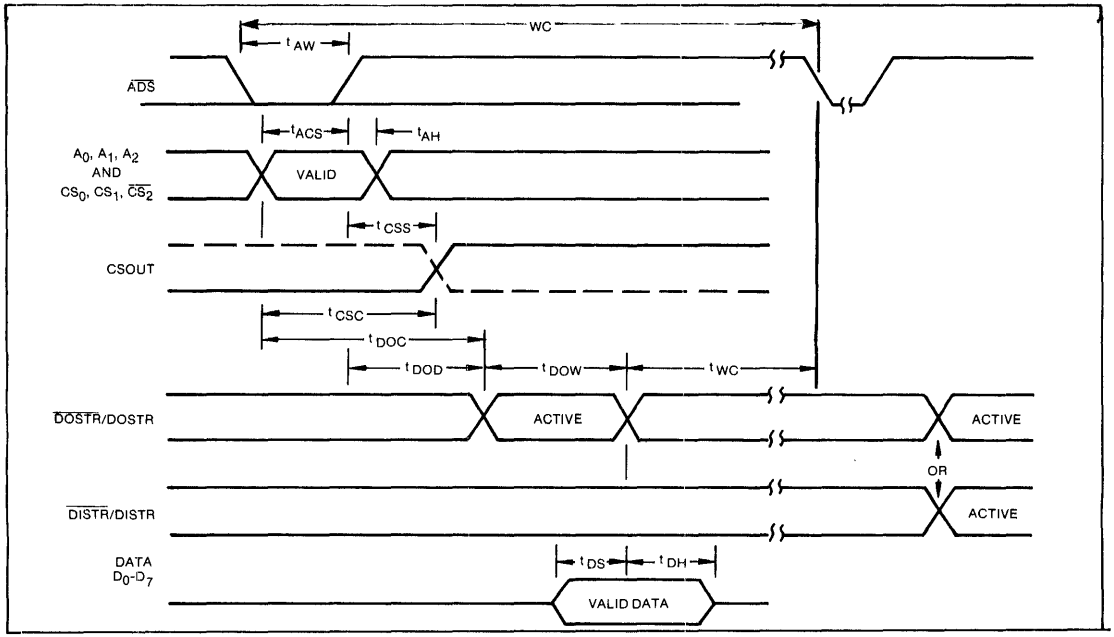


FIGURE 6. WRITE CYCLE TIMING

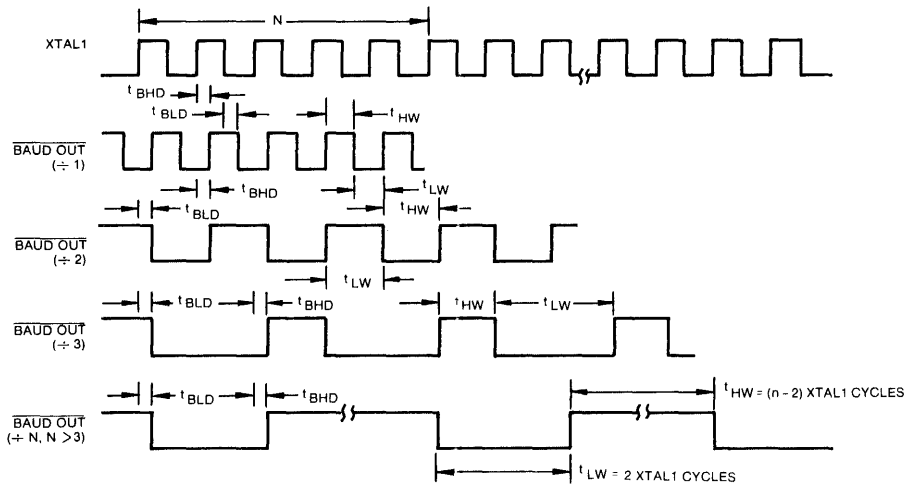
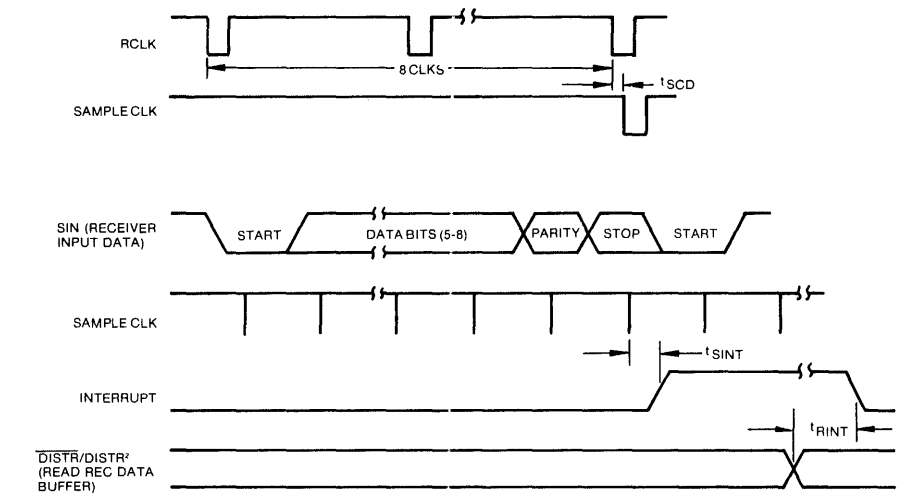
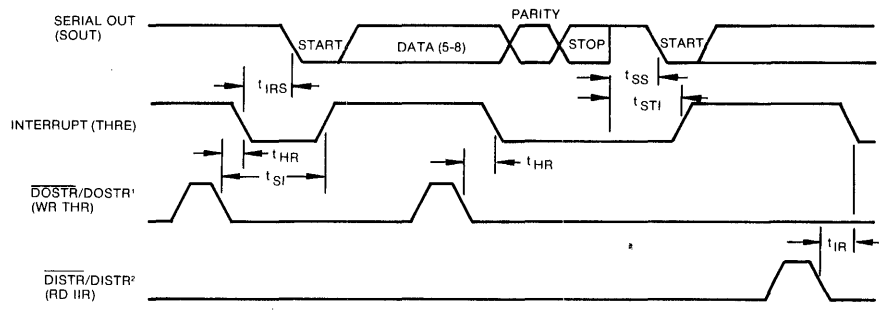


FIGURE 7. BAUDOUT TIMING



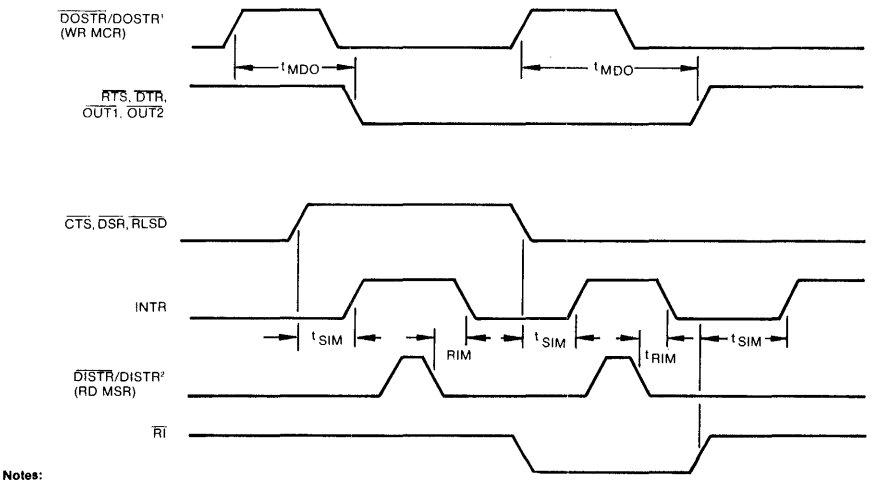
Notes:
¹See Write Cycle Timing
²See Read Cycle Timing

FIGURE 8. RECEIVER TIMING



Notes:
[1]See Write Cycle Timing
[2]See Read Cycle Timing

FIGURE 9. TRANSMITTER TIMING



Notes:
[1]See Write Cycle Timing
[2]See Read Cycle Timing

FIGURE 10. MODEM CONTROLS TIMING

ORDERING INFORMATION

Part Number	Max Clock Rate[1]	Bits/Character
WD8250*-00	3.1 MHz	5, 6, 7, 8
WD8250*-20	3.1 MHz	6, 7, 8
WD8250*-30	500 kHz	5, 6, 7, 8

NOTES:

1. This is the maximum clock rate that can be applied to pins 16 or 17.
   * Consult your local Western Digital Sales Representative for information regarding package availability, price, and delivery.

See page 725 for ordering information.

Printed in U.S.A.

WD2123 DEUCE
Dual Enhanced Universal Communications Element

FEATURES

- TWO INDEPENDENT ASYNCHRONOUS FULL DUPLEX DATA COMMUNICATION CHANNELS (2 BOARTS)
- TWO INDEPENDENT BAUD RATE GENERATORS (ONE PER CHANNEL)
- EACH CHANNEL WITH FOLLOWING FEATURES:
- SELECTABLE 5 TO 8 BIT CHARACTERS
- 1X, 16X, 64X CLOCK RATES
- 16 SELECTABLE BAUD RATE CLOCK FREQUENCIES (INTERNAL)
- LINE BREAK DETECTION AND GENERATION
- 1, 1½, OR 2 STOP BIT SELECTION
- FALSE START BIT DETECTION
- ODD OR EVEN PARITY GENERATE AND DETECTION
- OVERRUN AND FRAMING DETECTION
- DOUBLE BUFFERING OF DATA
- TTL COMPATIBLE INPUTS AND OUTPUTS
- COMPATIBLE WITH 8251A (ASYNC ONLY) AND WD1983 DEVICES
- DIAGNOSTIC LOCAL LOOP-BACK MODE
- RXD INITIALIZATION UPON MASTER RESET
- ON-BOARD OSCILLATOR FOR EASE OF USE WITH A CRYSTAL
- VERSATILE CLOCK SELECT OPTIONS FOR INDEPENDENT TRANSMIT AND RECEIVE RATES

INTRODUCTION

The Western Digital WD2123 Dual Enhanced Universal Communications Element (DEUCE) is a single chip MOS/LSI Data Communications Controller Circuit that contains two independent full-duplex asynchronous RECEIVER/TRANSMITTER CHANNELS and two independent BAUD RATE GENERATORS. The WD2123 is fabricated in N-Channel silicon gate technology and is packaged in a 40 pin plastic or ceramic package. All inputs and outputs are TTL compatible.

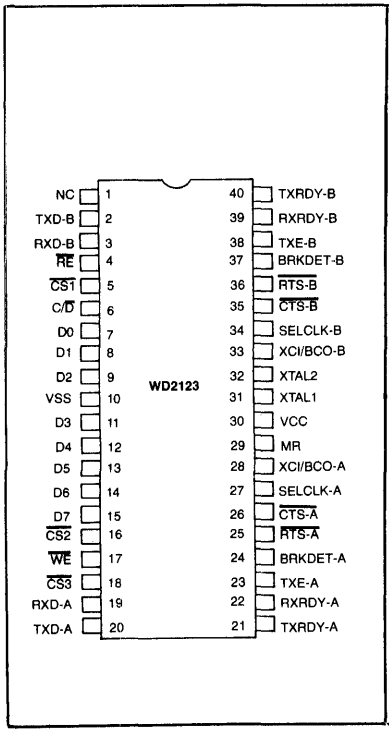


Figure 1. WD2123 PINOUT DIAGRAM

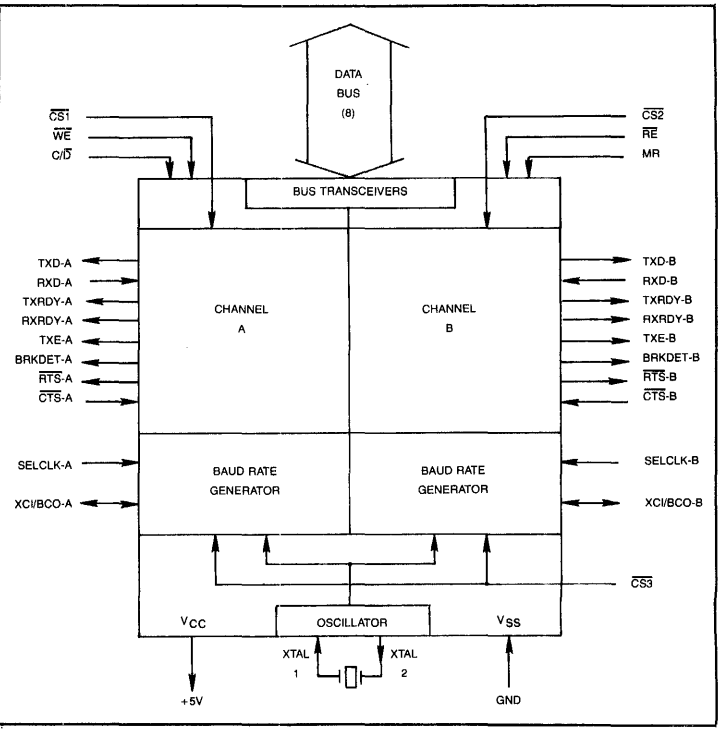


Figure 2. WD2123 BLOCK DIAGRAM

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
10	GROUND	VSS	Ground
30	POWER SUPPLY	VCC	+5VDC power supply input.
7 8 9 11 12 13 14 15	DATA BUS	D0 D1 D2 D3 D4 D5 D6 D7	This is the 8 bit Bidirectional Data Bus. It is the means of communication between the WD2123 and the CPU. Data, control, mode and status registers are accessed via this bus.
5	CHIP SELECT ONE	$\overline{CS1}$	V_{IL} on this input selects Channel A and enables computer communications with Channel A Data, control and status registers.
16	CHIP SELECT TWO	$\overline{CS2}$	V_{IL} on this input selects Channel B and enables computer communications with Channel B Data, control and status registers.
18	CHIP SELECT THREE	$\overline{CS3}$	V_{IL} on this input select the Baud Rate registers for programming.
6	CONTROL or DATA SELECT	C/$\overline{D}$	This input is used in conjunction with the appropriate Chip Select and an active read or write operation to determine register access via the Data Bus.
4	READ ENABLE	$\overline{RE}$	V_{IL} on this input allows the CPU to read data, or status information from the selected register.
17	WRITE ENABLE	$\overline{WE}$	V_{IL} on this input allows the CPU to write data or control information into the selected register.
29	MASTER RESET	MR	V_{IH} on this input resets both channels to the idle state and resets the status, command, mode and Data registers.
31	CRYSTAL OSCILLATOR INPUT	XTAL1	This is the input side of the on-chip oscillator. It can also be driven by an external clock source.
32	CRYSTAL OSCILLATOR OUTPUT	XTAL2	This is the output side of the on-chip oscillator.
27	SELECT CLOCK (Channel A)	SELCLK-A	This input is used in conjunction with the Clock Select bit (CR1) in the command register to determine the baud clock source for Channel A.
34	SELECT CLOCK (Channel B)	SELCLK-B	This input is used in conjunction with the Clock Select bit (CR1) in the command register to determine the baud clock source for Channel B.
28	EXTERNAL CLOCK INPUT/BAUD CLOCK OUTPUT-(Channel A)	XCI/BCO-A	This is a bidirectional port, which is used as the externally applied baud clock input or the internal baud rate generator output depending on the states of SELCLK and CR1 command bit. (Channel A)
33	EXTERNAL CLOCK INPUT/BAUD CLOCK OUTPUT-(Channel B)	XCI/BCO-B	This is a bidirectional port, which is used as the externally applied baud clock input or the internal baud rate generator output depending on the states of SELCLK and CR1 command bit. (Channel B)
26	CLEAR-TO-SEND (Channel A)	$\overline{CTS-A}$	V_{IL} on this input enables Channel A to transmit serial data if the Transmitter is enabled.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
35	CLEAR-TO-SEND (Channel B)	$\overline{\text{CTS-B}}$	V_{IL} on this input enables Channel B to transmit serial data if the Transmitter is enabled.
20	TRANSMIT DATA (Channel A)	TXD-A	This is the Serial Data Output from Channel A.
2	TRANSMIT DATA (Channel B)	TXD-B	This is the Serial Data Output from Channel B.
19	RECEIVE DATA (Channel A)	RXD-A	This is the Serial Data Input for Channel A.
3	RECEIVE DATA (Channel B)	RXD-B	This is the Serial Data Input for Channel B.
21	TRANSMITTER READY (Channel A)	TXRDY-A	This output, when high (V_{OH}), alerts the CPU that Channel A is ready to accept a new data character. The TXRDY output is automatically reset whenever a character is written into the Transmit Holding Register and can be used as an interrupt to the system.
40	TRANSMITTER READY (Channel B)	TXRDY-B	This output, when high (V_{OH}), alerts the CPU that Channel B is ready to accept a new data character. The TXRDY output is automatically reset whenever a character is written into the Transmit Holding Register and can be used as an interrupt to the system.
22	RECEIVER READY (Channel A)	RXRDY-A	This output, when high (V_{OH}), alerts the CPU that Channel B contains a data character that is ready to be input. This output is automatically reset whenever the new character is read from the Receive Holding Register and can be used as an interrupt to the system.
39	RECEIVER READY (Channel B)	RXRDY-B	This output, when high (V_{OH}), alerts the CPU that Channel B contains a data character that is ready to be input. This output is automatically reset whenever the new character is read from the Receive Holding Register and can be used as an interrupt to the system.
23	TRANSMITTER EMPTY (Channel A)	TXE-A	This output, when high (V_{OH}), indicates that Channel A Transmitter has no new characters to send and is waiting in an idle state.
38	TRANSMITTER EMPTY (Channel B)	TXE-B	This output, when high (V_{OH}), indicates that Channel B Transmitter has no new characters to send and is waiting in an idle state.
24	BREAK DETECT (Channel A)	BRKDET-A	This output, when high (V_{OH}), indicates that the Receiver for Channel A has detected a break condition.
37	BREAK DETECT (Channel B)	BRKDET-B	This output, when high (V_{OH}), indicates that the Receiver for Channel B has detected a break condition.
25	REQUEST-TO-SEND (Channel A)	$\overline{\text{RTS-A}}$	A general purpose output that is controlled by the command register bit CR5 for Channel A.
36	REQUEST-TO-SEND (Channel B)	$\overline{\text{RTS-B}}$	A general purpose output that is controlled by the command register bit CR5 for Channel B.
1		NC	No Internal Connection.

Table 1 WD2123 PIN DESCRIPTIONS

GENERAL DESCRIPTION

The WD2123 Block Diagram is shown in Figure 2. The WD2123 is a merger of two WD1983s and one WD1941 from WDC's line of communications devices on one piece of silicon. The 1983 is an asynchronous only version of the 8251A and the 1941 is a baud rate generator. In this manner, 8251A compatibility is maintained with the WD2123 with the added features of 2 channels and 2 baud rate generators on a single chip.

As depicted from the block diagram, the channels are referred to as CHANNELS A and B. CHANNEL A, which is an asynchronous 8251A, is addressed or controlled by the input signal $\overline{CS1}$. CHANNEL B is similarly controlled by $\overline{CS2}$. Finally, the BAUD RATE GENERATORS are controlled by $\overline{CS3}$.

Each channel of the WD2123 can be programmed to receive and transmit asynchronous serial data. The WD2123 performs serial-to-parallel conversion on data characters received from an input/output device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the status of either channel at any time. Status information on a per channel basis reported includes the type and the condition of the transfer operations being performed by the WD2123 as well as any transmission error conditions (parity, overrun, or framing). Programming the WD2123 is identical to the 8251A in the asynchronous mode, remembering that $\overline{CS1}$, when low, selects CHANNEL A and when $\overline{CS2}$ is low, selects CHANNEL B.

The WD2123 BAUD RATE GENERATORS may be selected either internally or externally. The clock select logic includes a clock select control bit CR1 (CS) in each COMMAND INSTRUCTION REGISTER. This control bit allows selection of the internal baud clock or an externally applied clock and works in conjunction with the select clock pin, "SELCLK" and the external clock input/baud clock output pin, "XCI/BCO". When CS is logic 1, the external clock select mode is selected. This means that the transmit and receive clocks (TXC and RXC) are internally tied together and the select clock pin, SELCLK, will determine whether those clocks are driven from the internal baud rate generator (SELCLK is high) or from the external clock input pin, "XCI/BCO", (SELCLK is low).

If the internal BRG clock is selected, (SELCLK is high) then the external clock input pin becomes a BRG clock output. Hence, the mnemonic, "XCI/BCO".

When CR1 (CS) is logic 0, then internal clock select mode is selected. The transmit clock (TXC) is driven by the internal BRG clock and the receive clock is driven by the select clock pin, (SELCLK). The XCI/BCO pin becomes the baud clock output (the same signal that is being applied to TXC).

The WD2123 also provides a local loop-back test mode of operation for each channel. This diagnostic mode is independently controlled via the LB(CR7) bit of the COMMAND REGISTER. When LB is logic 1, the channel is programmed for Local Loop-Back. In this diagnostic mode, the TXD output is set to the marking (logic "1") state; the output of the TRANSMIT REGISTER is "looped-back" into the RECEIVER REGISTER input; $\overline{RTS}$ output is held high; the $\overline{CTS}$ and RXD inputs are ignored. An additional requirement is that the TEN(CR0) command bit and the REN(CR2) be logic 1. The status and output flags operate normally.

Each channel is also provided with break character generation and detection. (A break character is defined as all zero data bits, parity bit and stop bits after a valid start bit.) For break character generation, SBRK (CR3) command bit is set to a logic 1. This causes the TXD output to be forced low (spacing) for as long as SBRK is programmed high. The break detect output and status bit (SR6) is set to logic 1, indicating that the receiver has detected a break character. The framing error flag is also set to 1 for this condition.

ORGANIZATION

The WD2123 is an eight bit bus-oriented device. Communication between the controlling CPU and the two RECEIVER/TRANSMITTER CHANNELS or the two BAUD RATE GENERATORS occurs via the 8 bit data bus through a common set of bus transceivers.

A diagram of one of the two communication controllers is shown in Figure 3. There are two accessible data registers, which buffers transmit and receive data. They are the TRANSMIT HOLDING REGISTER and the RECEIVE HOLDING REGISTER. There is a parallel-to-serial shift register, the TRANSMIT REGISTER and a serial-to-parallel shift register, the RECEIVE REGISTER.

Operational Control and monitoring of the CHANNEL is performed by two CONTROL REGISTERS (the COMMAND INSTRUCTION REGISTER and the MODE INSTRUCTION REGISTER) and the STATUS REGISTER.

A read/write control circuit allows programming/monitoring or loading/reading of data in the CONTROL, STATUS and HOLDING REGISTERS by activating the appropriate control lines: Chip Select ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$), READ ENABLE ($\overline{RE}$), WRITE ENABLE ($\overline{WE}$) and CONTROL or DATA SELECT (C/$\overline{D}$).

Internal control of each channel is by means of two internal microcontrollers: one for transmit and one for receive. The control registers, various counters and external signals provide inputs to the microcontrollers, which generate the necessary control signals to send and receive serial data according to the programmed protocol.

A diagram of one of the two BAUD RATE GENERATORS is shown in Figure 4. The 4 low order DATA BUS bits, DO-D3, are used to program the desired rate by loading the RATE REGISTER. Control signals $\overline{CS3}$, $\overline{WE}$ and C/$\overline{D}$ are used to select and load the appropriate register.

The contents of the RATE REGISTER is decoded and addresses a FREQUENCY SELECT ROM for the proper frequency, which is generated by the DIVIDER circuitry and the control logic.

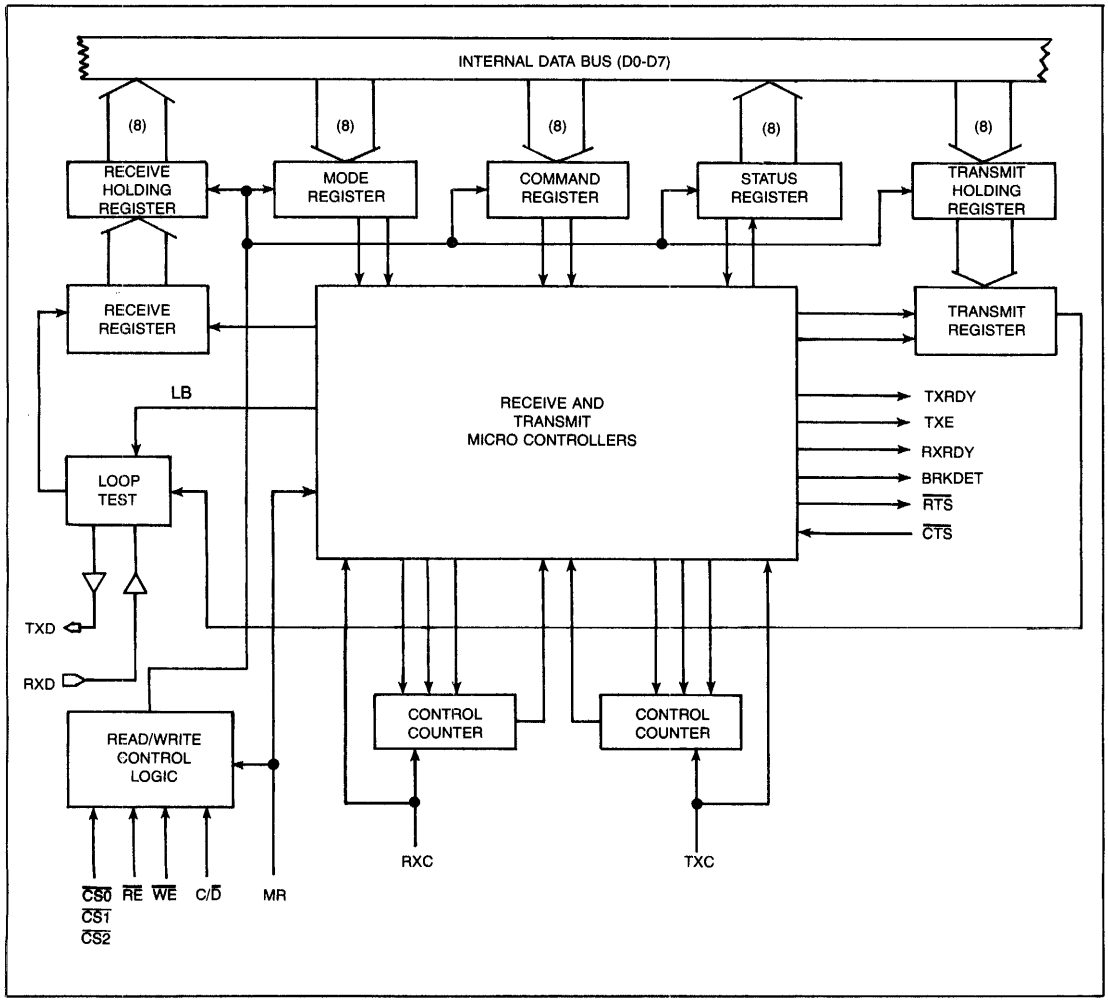


Figure 3. RECEIVE/TRANSMIT COMMUNICATIONS CONTROLLER DIAGRAM

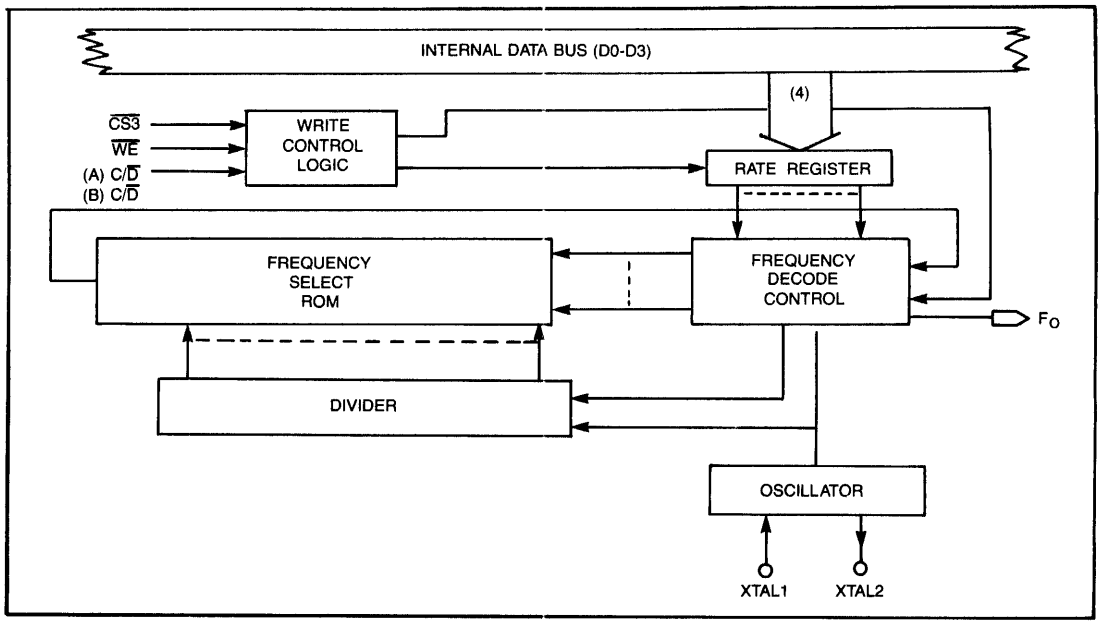


Figure 4 WD2123 BAUD RATE GENERATOR DIAGRAM

The WD2123 registers are addressed by the following table:

C/D	RE	WE	CS1	CS2	CS3	REGISTER SELECTED		
L	L	H	L	H	H	RECEIVE HOLDING REG.	—	CHA
L	H	L	L	H	H	TRANSMIT HOLDING REG.	—	CHA
H	L	H	L	H	H	STATUS REG.	—	CHA
H	H	L	L	H	H	MODE AND COMMAND REG.	—	CHA
L	L	H	H	L	H	RECEIVE HOLDING REG.	—	CHB
L	H	L	H	L	H	TRANSMIT HOLDING REG.	—	CHB
H	L	H	H	L	H	STATUS REG.	—	CHB
H	H	L	H	L	H	MODE and COMMAND REG.	—	CHB
L	H	L	H	H	L	RATE REG.	—	CHA
H	H	L	H	H	L	RATE REG.	—	CHB
X	X	X	H	H	H	DATA BUS IN HIGH IMPEDANCE MODE		

Table 2 WD2123 REGISTER ADDRESSING

Note:
"L" means V_{IL} at pins.
"H" means V_{IH} at pins.
"X" means don't care.

The WD2123 contains two MODE REGISTERS—one for each channel. The format and definition of the MODE REGISTERS are shown below:

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
S2	S1	EP	PEN	L2	L1	B2	B1

B2	B1	BAUD RATE FACTOR
0	0	Undefined
0	1	1X
1	0	16X
1	1	64X
L2	**L1**	**CHARACTER LENGTH**
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits
PEN		**PARITY ENABLE**
0		Disable Parity
1		Enable Parity
EP		**PARITY SELECT**
0		Odd Parity
1		Even Parity
S2	**S1**	**NUMBER OF STOP BITS**
0	0	Invalid
0	1	1 Bit
1	0	1½ Bits
1	1	2 Bits

Table 3 WD2123 MODE REGISTERS

The WD2123 contains two COMMAND REGISTERS—one per channel. The format and definition of the COMMAND REGISTERS are shown below:

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
LB	IR	RTS	ER	SBK	REN	CS	TEN

TEN		**TRANSMIT ENABLE**
CR4	1	Enable
	0	Disable
CS		**CLOCK SELECT**
1	1	External Clock Select Mode
	0	Internal Clock Select Mode
REN		**RECEIVE ENABLE**
2	1	Enable
	0	Disable
SBK		**SEND BREAK CHARACTER**
3	1	Force TXD Low
	0	Normal Operation
ER		**ERROR RESET**
4	1	Reset Error Flags
	0	No Reset
RTS		**REQUEST TO SEND**
5	1	Force $\overline{RTS}$ pin = 0 (V_{OL})
	0	Force $\overline{RTS}$ pin = 1 (V_{OH})
IR		**INTERNAL RESET**
6	1	Next Write to Mode Register
	0	Next Write to Command Register
LB		**LOOP BACK ENABLE**
7	0	Normal Operation Mode
	1	Local Loop-Back Mode

Table 4 WD2123 CONTROL REGISTERS

The WD2123 contains two STATUS REGISTERS—one per channel. The STATUS REGISTER is a read-only register. The format and definition of the STATUS REGISTERS are shown below:

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
CTS	BRK DET	FE	OE	PE	TXE	RX RDY	TX RDY

TXRDY	**TRANSMITTER READY**
1	Denotes THR is empty and ready for a new character
0	THR not empty. (Reset when THR is loaded by CPU)
RXRDY	**RECEIVER READY**
1	Denotes that the RHR contains a valid character
0	RHR does not contain a valid character. (Reset when the CPU reads the RHR)
TXE	**TRANSMITTER EMPTY**
1	Denotes that the TR is empty
0	Denotes that the TR is not empty
PE	**PARITY ERROR**
1	Denotes Parity Error
0	No Parity Error. (Reset by ER bit of command register)
OE	**OVERRUN ERROR**
1	Denotes Overrun Error
0	No Overrun Error. (Reset by ER bit of command register)
FE	**FRAMING ERROR**
1	Denotes Framing Error
0	No Framing Error. (Reset by ER bit of command register)
BRKDET	**BREAK DETECT**
1	Indicates that the receiver has detected a line break condition. (FE will also be set)
0	No Break Condition detected for at least one bit time
CTS	**CLEAR-TO-SEND**
1	Indicates that the $\overline{CTS}$ pin is active (V_{IL})
0	Indicates that the $\overline{CTS}$ pin is not active (V_{IH})

Table 5 WD2123 STATUS REGISTERS

The WD2123 contains two RATE REGISTERS that are used to select 16 BAUD rates when CR1 = 1 and SELCLK = 1. The Format of the RATE REGISTERS is shown below. Note that the Receiver and the Transmitter of any channel run off the same Baud clock except when CR1 = 0, then the Transmitter runs off the Baud Clock and the Receiver runs off an externally applied signal input on the SELCLK pin.

D7							D0
X	X	X	X	RA3 RB3	RA2 RB2	RA1 RB1	RA0 RB0

When C/D = 0, RA3 to RA0 are loaded.
When C/$\overline{D}$ = 1, RB3 to RB0 are loaded.

The C/$\overline{D}$ line is used in conjunction with $\overline{CS3}$ and $\overline{WE}$ to program the desired BAUD rate. When C/$\overline{D}$ is low, Channel A is selected, and when C/$\overline{D}$ is high, Channel B is selected. The low order 4 bits of the DATA BUS are loaded into the selected rate register, and the high order 4 bits are ignored.

When the crystal frequency equals 1.8432 MH_z the following baud rates may be programmed.

R3	R2	R1	R0	BAUD RATE	FREQUENCY
0	0	0	0	50	.800 KHZ
0	0	0	1	75	1.200
0	0	1	0	110	1.760
0	0	1	1	134.5	2.150
0	1	0	0	150	2.400
0	1	0	1	200	3.200
0	1	1	0	300	4.800
0	1	1	1	600	9.600
1	0	0	0	1200	19.200
1	0	0	1	1800	28.800
1	0	1	0	2400	38.400
1	0	1	1	3600	57.600
1	1	0	0	4800	76.800
1	1	0	1	7200	115.200
1	1	1	0	9600	153.600
1	1	1	1	19,200	307.200

Table 6 WD2123 BAUD RATE REGISTERS

OPERATING DESCRIPTION

The WD2123 is primarily designed to operate in an 8 bit microprocessor environment, although other control logic schemes are easily implemented. The DATA BUS and the interface control signals ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, C/$\overline{D}$, $\overline{RE}$, $\overline{WE}$) should be connected to the microprocessor's data bus and system control bus. A 1.8432 MHz crystal should be connected to the WD2123 as shown in figure 5. The appropriate TXC (RXC) clock frequencies should be programmed via system software. Different Baud clock configurations are possible, such as separate transmit and receive frequencies, and are outlined in the general description.

For typical data communication applications, the RXD and TXD input/outputs can be connected to RS-232C interface circuits. Interface control signals, $\overline{CTS}$ and $\overline{RTS}$, are controlled and sensed by the CPU through the COMMAND and STATUS REGISTERS and can be configured in several ways. The $\overline{CTS}$ input can be used to synchronize the transmitter to external events.

The TXRDY, RXRDY, TXE and BRKDET FLAGS may be connected to the microprocessor system as interrupt inputs or the STATUS REGISTER can be periodically read in a polled environment to support data communication control operations.

The SBRK bit of the COMMAND REGISTER (CR3) is used to send a Break Character. (A Break Character is defined as a start bit, and all zero data, parity and stop bits.) When the CR3 bit is set to a "1", it causes the transmitter output, TXD,

to be forced low after the last bit of the last character is transmitted.

The Receiver is equipped with logic to look for a break character. When a break is received, the BREAK DETECT (BRKDET) FLAG and STATUS bit are set to "1". When the receiver input line goes high (V_{IH}) for at least one clock period, the receiver resets the BRKDET FLAG and resumes its search for a start bit.

PROGRAMMING PROCEDURE

The programming sequence of the two channels will be different, depending on whether it is an initialization sequence (that is, one performed right after a hardware master reset occurs) or a re-programming sequence (that is, one performed to change the protocol characteristics (Parity, rate, character length, etc.) after the device has been previously operating in the system). The programming sequence differs, in that, after a master reset, the chip is set to expect the first *control write* operation ($C/\overline{D}=1$) to contain a *mode instruction.* Any *subsequent control write* operations will be transferred to the *command instruction* register.

Now when it is desired to *change* the *mode instruction* register contents, the following re-programming sequence should be performed. A Command Control word of "40" Hex is written to the Chip. This turns off the Receiver and Transmitter and sets the IR (Internal Reset) bit. This bit causes the read/write control logic to expect the *next control write* operation to be a *new mode instruction.* After the new mode instruction is written to the chip, all subsequent control write operations will again be interpreted as *command instructions.* Therefore, after the *new mode instruction* is performed, the next command would turn the receiver and transmitter back on and resume normal Data operations.

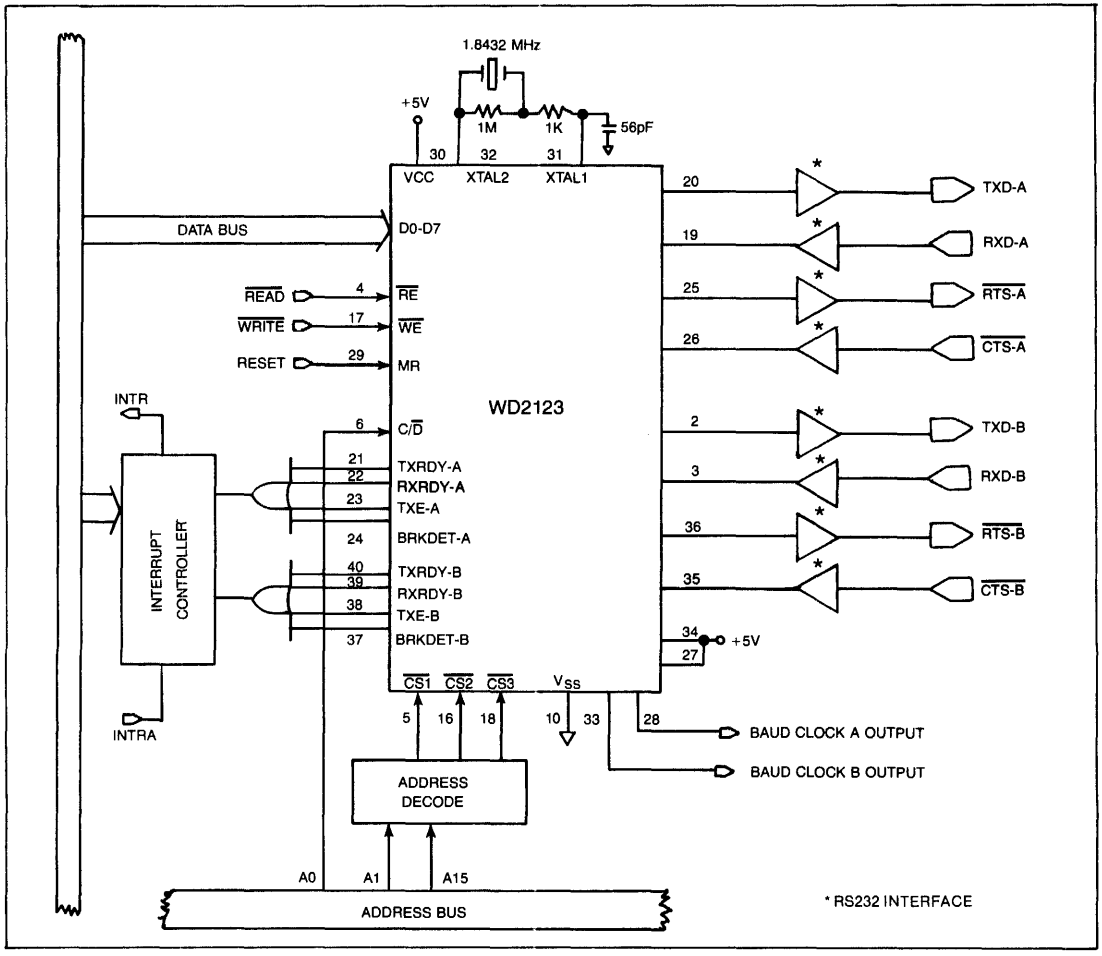


Figure 5 WD2123 MICROPROCESSOR APPLICATION

ABSOLUTE MAXIMUM RATINGS

V_{DD} with respect to V_{SS} ..... 0.5V to +12V
Voltage on Any Pin with Respect to Ground ..... —0.5V to +7V
Power Dissipation ..... 500Mw.

STORAGE TEMPERATURE:
Ceramic: —65°C to +150°C
Plastic: —55°C to +125°C

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%; GND = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	—0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = —100 uA
I_{DL}	Data Bus Leakage (High Impedance State)			—50 10	uA uA	V_{OUT} = 0.45V V_{OUT} = V_{CC}
I_{IL}	Input Leakage			10	uA	V_{IN} = V_{CC}
I_{CC}	Power Supply Current		100	125	mA	V_{CC} = 5.25V No Load

Table 7 WD2123 D.C. PARAMETERS

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	f_C = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND.

Table 8 WD2123 CAPACITANCE LEVELS

AC ELECTRICAL CHARACTERISTICS

Table 9 WD2123 A.C. PARAMETERS

T_A = 0°C to + 70C; V_{CC} = 5.0V ±5%; GND = 0V

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
BUS PARAMETERS Read Cycle					
t_{AR}	Address Stable Before READ (CS,C/D)	50		ns	
t_{RA}	Address Hold Time for READ (CS,C/D)	50		ns	
t_{RE}	READ Pulse Width	230		ns	
t_{RD}	Data Delay from READ		200	ns	C_L = 50 pF
t_{RDH}	READ to Data Floating	25	200	ns	C_L (Max) = 50 pF C_L (Min) = 15 pF
Write Cycle					
t_{AW}	Address Stable Before WRITE	50		ns	
t_{WA}	Address Hold Time for WRITE	50		ns	
t_{WE}	WRITE Pulse Width	230		ns	
t_{DS}	Data Set-Up Time for WRITE	TWE		ns	
t_{WDH}	Data Hold Time for WRITE	100		ns	
OTHER TIMINGS					
t_{TXC}	Transmit Clock Period	1.6		us	
t_{DTX}	TxD Delay from Falling Edge of TxC		1000	ns	C_L = 100 pF
t_{SRX}	Rx Data Set-Up Time to Sampling Pulse	200		ns	C_L = 100 pF
t_{HRX}	Rx Data Hold Time to Sampling Pulse	200		ns	C_L = 100 pF
f_{TX}	Transmitter Input Clock Frequency 1x Baud Rate 16x and 64x Baud Rate	 DC DC	 500 600	 kHz kHz	 Clock 50% Duty Cycle
t_{TPW}	Transmitter Input Clock Pulse Width 1x Baud Rate 16x and 64x Baud Rate	 1.0 800		 us ns	
t_{TPD}	Transmitter Input Clock Pulse Delay 1x Baud Rate 16x and 64x Baud Rate	 1.0 800		 us ns	
t_{MR}	Master Reset	500		ns	

Table 9 WD2123 A.C. PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
f_{RX}	Receiver Input Clock Frequency 1x Baud Rate 16x and 64x Baud Rate	 DC DC	 500 600	 kHz kHz	Clock 50% Duty Cycle
t_{RPW}	Receiver Input Clock Pulse Width 1x Baud Rate 16x and 64x Baud Rate	 1.0 800		 us ns	
t_{RPD}	Receiver Input Clock Pulse Delay 1x Baud Rate 16x and 64x Baud Rate	 1.0 800		 us ns	
t_{TX}	TxRDY Delay from Center of Stop Bit		8	t_{RXC}	C_L = 50pF (16X)
t_{RX}	RxRDY Delay from Center of Stop Bit		½	t_{RXC}	
t_{IS}	Internal BRKDET Delay from Center of Data Bit		1	RXC	
t_{TRD}	TxRDY Delay from Falling Edge of WRITE		450	ns	
t_{TOD}	TXD Output from Falling Edge of WRITE		1½	t_{TXC}	
t_{WC}	Control Delay from Rising Edge of WRITE (RTS)		200	ns	
t_{CR}	Control to READ Set-Up Time (CTS)		1	t_{TXC}	
t_{MR}	Master Reset	500		ns	

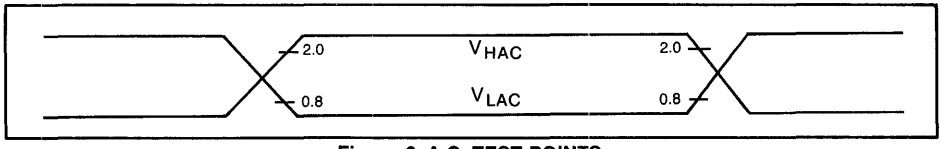


Figure 6 A.C. TEST POINTS

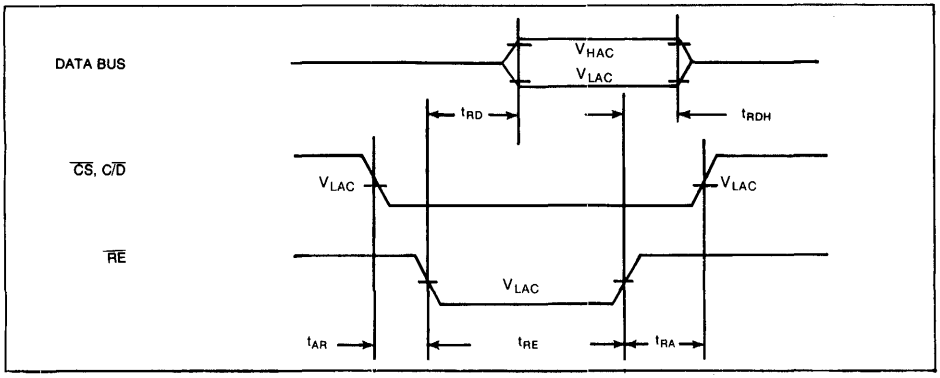


Figure 7 WD2123 READ TIMING

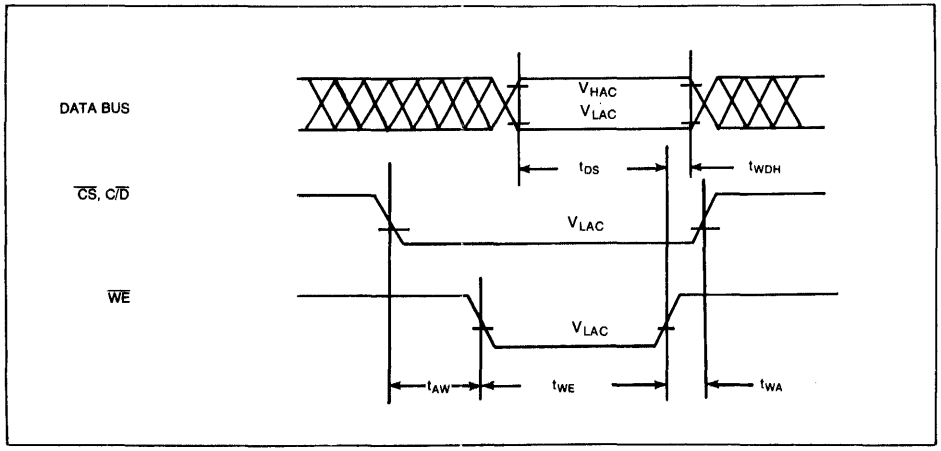


Figure 8 WD2123 WRITE TIMING

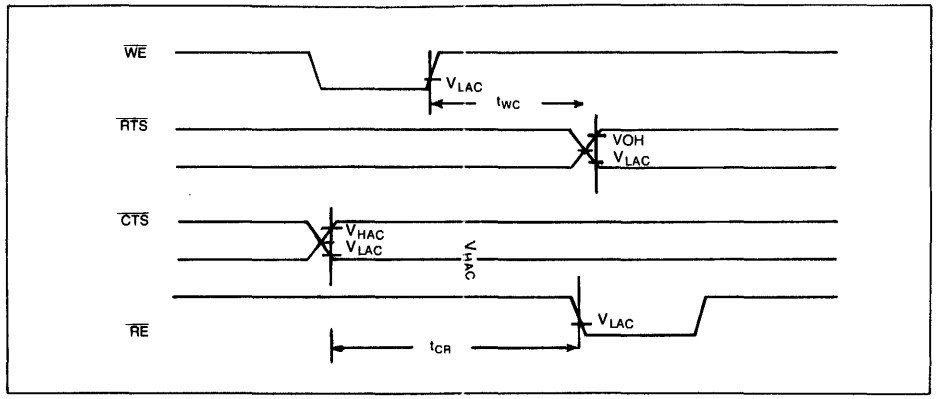


Figure 9 WD2123 INTERFACE CONTROL TIMING

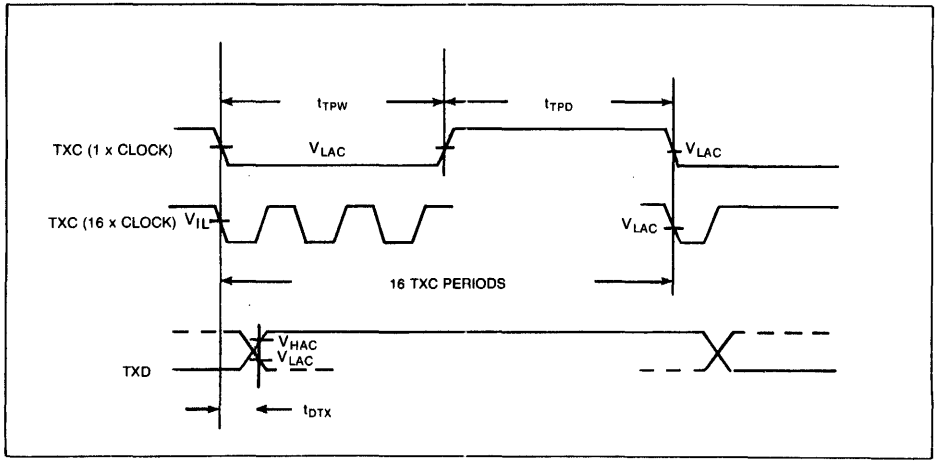


Figure 10 WD2123 TRANSMITTER CLOCK AND DATA TIMING

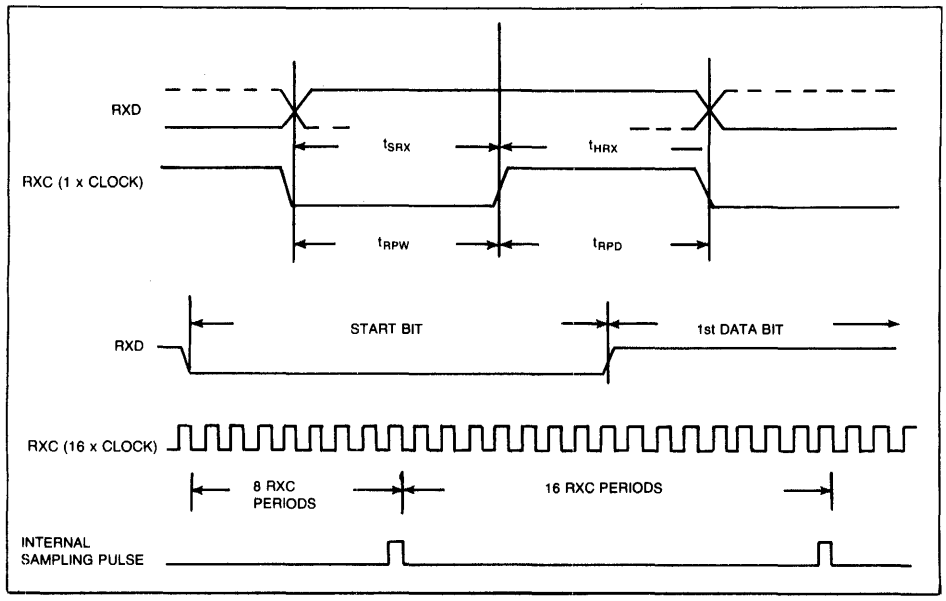


Figure 11 WD2123 RECEIVER CLOCK AND DATA TIMINGS

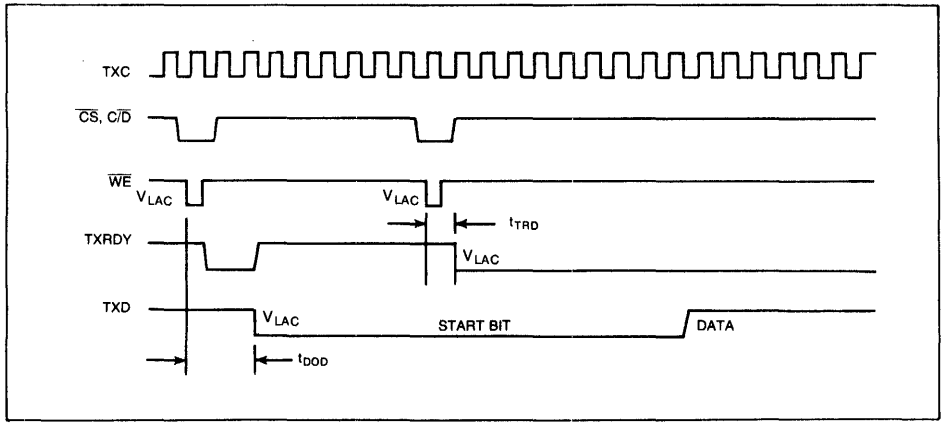


Figure 12 WD2123 TRANSMITTER OUTPUT TIMINGS WITH RESPECT TO TRANSMIT CLOCK

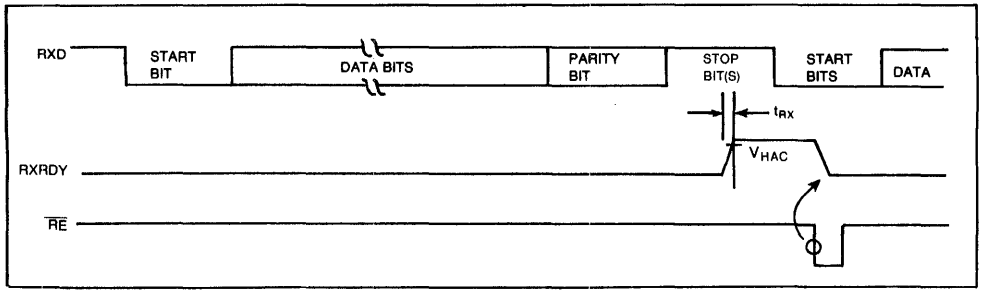


Figure 13 WD2123 RXRDY TIMING

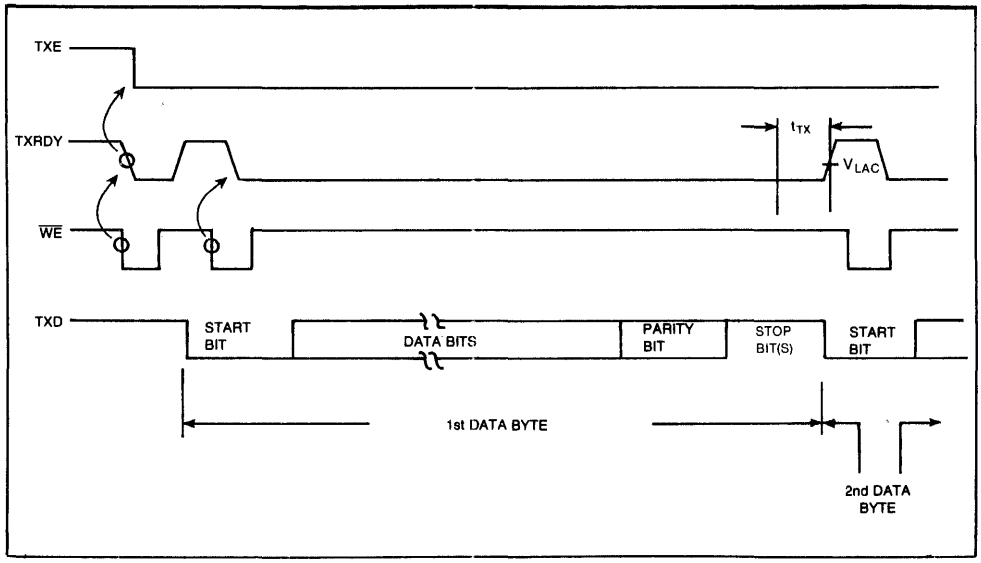


Figure 14 WD2123 TXRDY TIMING

See page 725 for ordering information.

Printed in U.S.A.

BR1941(5016) Dual Baud Rate Clock

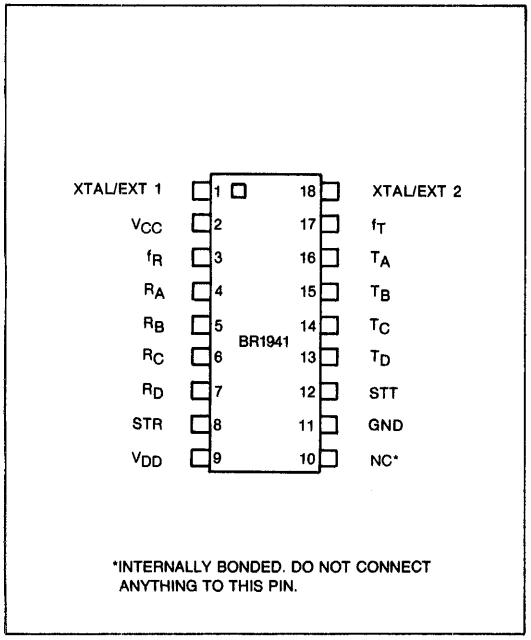
FEATURES

- 16 SELECTABLE BAUD RATE CLOCK FREQUENCIES
- SELECTABLE 1X, 16X OR 32X CLOCK OUTPUTS FOR FULL DUPLEX OPERATIONS
- OPERATES WITH CRYSTAL OSCILLATOR OR EXTERNALLY GENERATED FREQUENCY INPUT
- ROM MASKABLE FOR NON-STANDARD FREQUENCY SELECTIONS
- INTERFACES EASILY WITH MICROCOMPUTERS
- OUTPUTS A 50% DUTY CYCLE CLOCK WITH 0.01% ACCURACY
- 6 DIFFERENT FREQUENCY/DIVISOR PAIRS AVAILABLE
- TTL, MOS COMPATIBILITY
- PIN COMPATIBLE WITH COM5016

GENERAL DESCRIPTION

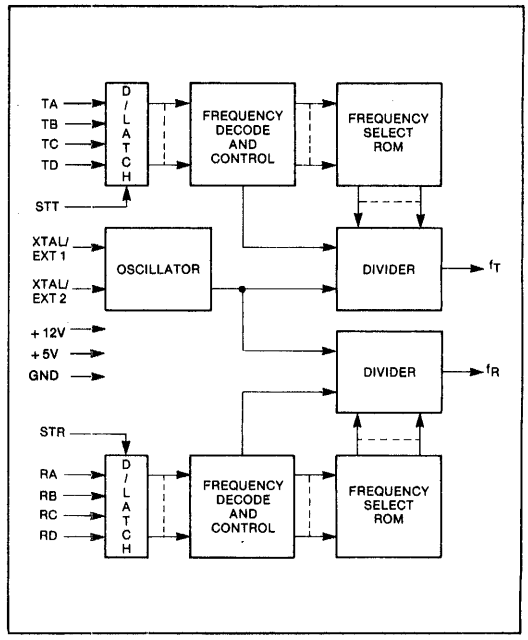
The BR1941 is a combination Baud Rate Clock Generator and Programmable Divider. It is manufactured in N-channel MOS using silicon gate technology. This device is capable of generating 16 externally selected clock rates whose frequency is determined by either a single crystal or an externally generated input clock. The BR1941 is a programmable counter capable of generating a division from 2 to $(2^{15} - 1)$.

The BR1941 is available programmed with the most used frequencies in data communication. Each frequency is selectable by strobing or hard wiring each of the two sets of four Rate Select inputs. Other frequencies/division rates can be generated by reprogramming the internal ROM coding through a MOS mask change. Additionally, further clock division may be accomplished through cascading of devices. The frequency output is fed into the XTAL/EXT input on a subsequent device.



*INTERNALLY BONDED. DO NOT CONNECT ANYTHING TO THIS PIN.

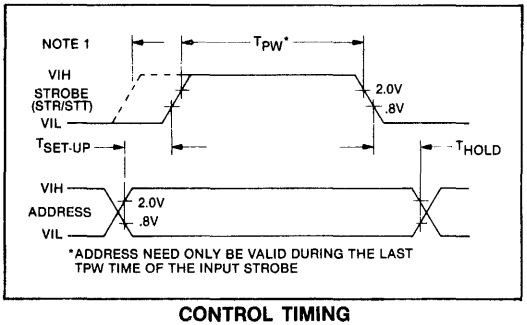
PIN CONNECTIONS



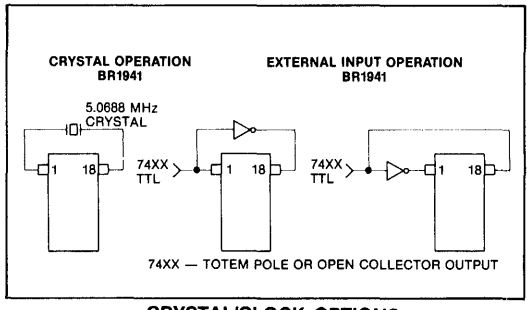
BR1941 BLOCK DIAGRAM

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	XTAL/EXT 1	Crystal or External Input 1	This input receives one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+5 volt Supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver Address inputs.
4-7	R_A, R_B, R_C, R_D	Receiver Address	The logic level on these inputs as shown in Tables 1 through 6, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver Address	A high-level input strobe loads the receiver address (R_A, R_B, R_C, R_D) into the receiver address register. This input may be strobed or hard wired to +5V.
9	V_{DD}	Power Supply	+12 volt Supply
10	NC	No Connection	Internally bonded. Do not connect anything to this pin.
11	GND	Ground	Ground
12	STT	Strobe-Transmitter Address	A high-level input strobe loads the transmitter address (T_A, T_B, T_C, T_D) into the transmitter address register. This input may be strobed or hard wired to +5V.
13-16	T_D, T_C, T_B, T_A	Transmitter Address	The logic level on these inputs, as shown in Tables 1 through 6, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter Address inputs.
18	XTAL/EXT 2	Crystal or External Input 2	This input receives the other pin of the crystal package or the other polarity of the external input.



CONTROL TIMING



CRYSTAL/CLOCK OPTIONS

ABSOLUTE MAXIMUM RATINGS

Positive Voltage on any Pin, with respect to ground	+20.0V
Negative Voltage on any Pin, with respect to ground	−0.3V
Storage Temperature	(plastic package) −55°C to +125°C (cerdip package and ceramic package) −65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+325°C

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and Functional Operation of the device at these or at any other condition above those indicated in the operational sections of this specification are not implied.

ELECTRICAL CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	See Note 1
High-level, V_{IH}	V_{CC} – 1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL} = 3.2 mA
High-level, V_{OH}	V_{CC} – 1.5	4.0		V	I_{OH} = 100μA
INPUT CURRENT					
Low-level, I_{IL}			0.3	mA	V_{IN} = GND, excluding XTAL inputs
INPUT CAPACITANCE					
All Inputs, C_{IN}		5	10	pf	V_{IN} = GND, excluding XTAL inputs
INPUT RESISTANCE					
Crystal Input, R_{XTAL}	1.1			KΩ	Resistance to ground for Pin 1 and Pin 18
POWER SUPPLY CURRENT					
I_{CC}		20	60	mA	
I_{DD}		20	70	mA	
AC CHARACTERISTICS					T_A = +25°C
CLOCK FREQUENCY					See Note 2
PULSE WIDTH (T_{PW})					
Clock					50% duty cycle ± 10%. See Note 2
Receiver strobe	150		DC	ns	
Transmitter strobe	150		DC	ns	
INPUT SET-UP TIME (T_{SET-UP})					
Address	50			ns	See Note 3
OUTPUT HOLD TIME (T_{HOLD})					
Address	50			ns	

NOTE 1: BR1941 — XTAL/EXT inputs are either TTL compatible or crystal compatible. See crystal specification in Applications Information section.
All inputs except XTAL/EXT have internal pull-up resistors.
NOTE 2: Refer to frequency option tables for maximum input frequency on XTAL/EXT pins.
Typical Clock Pulse width is 1/2xCL.
NOTE 3: Input set-up time can be decreased to ≥0 ns by increasing the minimum strobe width by 50 ns to a total of 200 ns.

OPERATION

Standard Frequencies

Choose a Transmitter and Receiver frequency from the table below. Program the corresponding address into TA-TD and RA-RD respectively using strobe pulses or by hard wiring the strobe and address inputs.

Non-Standard Frequencies

To accomplish non-standard frequencies do one of the following:

1. Choose a crystal that when divided by the BR1941 generates the desired frequency.
2. Cascade devices by using the frequency outputs as an

input to the XTAL/EXT inputs of the subsequent BR1941.

3. Consult the factory for possible changes via ROM mask reprogramming.

FREQUENCY OPTIONS

TABLE 1. CRYSTAL FREQUENCY = 5.0688 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	0.8	—	50/50	6336
0	0	0	1	75	1.2	1.2	—	50/50	4224
0	0	1	0	110	1.76	1.76	—	50/50	2880
0	0	1	1	134.5	2.152	2.1523	0.016	50/50	2355
0	1	0	0	150	2.4	2.4	—	50/50	2112
0	1	0	1	300	4.8	4.8	—	50/50	1056
0	1	1	0	600	9.6	9.6	—	50/50	528
0	1	1	1	1200	19.2	19.2	—	50/50	264
1	0	0	0	1800	28.8	28.8	—	50/50	176
1	0	0	1	2000	32.0	32.081	0.253	50/50	158
1	0	1	0	2400	38.4	38.4	—	50/50	132
1	0	1	1	3600	57.6	57.6	—	50/50	88
1	1	0	0	4800	76.8	76.8	—	50/50	66
1	1	0	1	7200	115.2	115.2	—	50/50	44
1	1	1	0	9600	153.6	153.6	—	48/52	33
1	1	1	1	19,200	307.2	316.8	3.125	50/50	16

BR1941-00

TABLE 2. CLOCK FREQUENCY = 2.76480 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	0.8	—	50/50	3456
0	0	0	1	75	1.2	1.2	—	50/50	2304
0	0	1	0	110	1.76	1.76	−0.006	50/50	1571
0	0	1	1	134.5	2.152	2.152	−0.019	50/50	1285
0	1	0	0	150	2.4	2.4	—	50/50	1152
0	1	0	1	200	3.2	3.2	—	50/50	864
0	1	1	0	300	4.8	4.8	—	50/50	576
0	1	1	1	600	9.6	9.6	—	50/50	288
1	0	0	0	1200	19.2	19.2	—	50/50	144
1	0	0	1	1800	28.8	28.8	—	50/50	96
1	0	1	0	2000	32.0	32.15	+0.465	50/50	86
1	0	1	1	2400	38.4	38.4	—	50/50	72
1	1	0	0	3600	57.6	57.6	—	50/50	48
1	1	0	1	4800	76.8	76.8	—	50/50	36
1	1	1	0	9600	153.6	153.6	—	50/50	18
1	1	1	1	19,200	307.2	307.2	—	50/50	9

BR1941-02

TABLE 3. CRYSTAL FREQUENCY = 6.018305 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	.7999	0	50/50	7523*
0	0	0	1	75	1.2	1.2000	0	50/50	5015*
0	0	1	0	110	1.76	1.7597	0	50/50	3420
0	0	1	1	134.5	2.152	2.1517	0	50/50	2797*
0	1	0	0	150	2.4	2.3996	0	50/50	2508
0	1	0	1	200	3.2	3.1995	0	50/50	1881*
0	1	1	0	300	4.8	4.7993	0	50/50	1254
0	1	1	1	600	9.6	9.5986	0	50/50	627*
1	0	0	0	1200	19.2	19.2279	+0.14	50/50	31.3*
1	0	0	1	1800	28.8	28.7959	0	50/50	209*
1	0	1	0	2000	32.0	32.0125	0	50/50	188
1	0	1	1	2400	38.4	38.3334	−0.17	50/50	157*
1	1	0	0	3600	57.6	57.8687	+0.46	50/50	104
1	1	0	1	4800	76.8	77.1583	+0.46	50/50	78
1	1	1	0	9800	153.6	154.3166	+0.46	50/50	39*
1	1	1	1	19,200	307.2	300.9175	−2.04	50/50	20

BR1941-03

TABLE 4. CLOCK FREQUENCY = 5.52960 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	1.6	1.6	—	50/50	3456
0	0	0	1	75	2.4	2.4	—	50/50	2304
0	0	1	0	110	3.52	3.52	−0.006	50/50	1571
0	0	1	1	134.5	4.304	4.303	−0.019	50/50	1285
0	1	0	0	150	4.8	4.8	—	50/50	1152
0	1	0	1	200	6.4	6.4	—	50/50	864
0	1	1	0	300	9.6	9.6	—	50/50	576
0	1	1	1	600	19.2	19.2	—	50/50	288
1	0	0	0	1200	38.4	38.4	—	50/50	144
1	0	0	1	1800	57.6	57.6	—	50/50	96
1	0	1	0	2000	64.0	64.3	+0.465	50/50	86
1	0	1	1	2400	76.8	76.8	—	50/50	72
1	1	0	0	3600	115.2	115.2	—	50/50	48
1	1	0	1	4800	153.6	153.6	—	50/50	36
1	1	1	0	9600	307.2	307.2	—	50/50	18
1	1	1	1	19,200	614.4	614.4	—	50/50	9

BR1941-04

TABLE 5. CRYSTAL FREQUENCY = 4.9152 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(32X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	0.8	—	50/50	6144
0	0	0	1	75	1.2	1.2	—	50/50	4096
0	0	1	0	110	1.76	1.7598	−0.01	*	2793
0	0	1	1	134.5	2.152	2.152	—	50/50	2284
0	1	0	0	150	2.4	2.4	—	50/50	2048
0	1	0	1	300	4.8	4.8	—	50/50	1024
0	1	1	0	600	9.6	9.6	—	50/50	512
0	1	1	1	1200	19.2	19.2	—	50/50	256
1	0	0	0	1800	28.8	28.7438	−0.19	*	171
1	0	0	1	2000	32.0	31.9168	−0.26	50/50	154
1	0	1	0	2400	38.4	38.4	—	50/50	128
1	0	1	1	3600	57.6	57.8258	0.39	*	85
1	1	0	0	4800	76.8	76.8	—	50/50	64
1	1	0	1	7200	115.2	114.306	−0.77	*	43
1	1	1	0	9600	153.6	153.6	—	50/50	32
1	1	1	1	19,200	307.2	307.2	—	50/50	16

BR1941-05

TABLE 6. CRYSTAL FREQUENCY = 5.0688 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(32X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	1.6	1.6	—	50/50	3168
0	0	0	1	75	2.4	2.4	—	50/50	2112
0	0	1	0	110	3.52	3.52	—	50/50	1440
0	0	1	1	134.5	4.304	4.303	.026	50/50	1178
0	1	0	0	150	4.8	4.8	—	50/50	1056
0	1	0	1	200	6.4	6.4	—	50/50	792
0	1	1	0	300	9.6	9.6	—	50/50	528
0	1	1	1	600	19.2	19.2	—	50/50	264
1	0	0	0	1200	38.4	38.4	—	50/50	132
1	0	0	1	1800	57.6	57.6	—	50/50	88
1	0	1	0	2400	76.8	76.8	—	50/50	66
1	0	1	1	3600	115.2	115.2	—	50/50	44
1	1	0	0	4800	153.6	153.6	—	*	33
1	1	0	1	7200	230.4	230.4	—	50/50	22
1	1	1	0	9600	307.2	298.16	2.941	*	17
1	1	1	1	19,200	614.4	633.6	3.125	50/50	8

*When the duty cycle is not exactly 50% it is 50% ± 10%

BR1941-06

CRYSTAL SPECIFICATIONS

User must specify termination (pin, wire, other)
Frequency — See Tables 1-6.
Temperature range 0°C to + 70°C
Series resistance ≤ 50Ω
Series resonant
Overall tolerance ± .01%

CRYSTAL MANUFACTURERS (Partial List)

American Time Products Div.
Frequency Control Products, Inc.
61-20 Woodside Ave.
Woodside, New York 11377
(212) 458-5811

Bliley Electric Co.
2545 Grandview Blvd.
Erie, Pennsylvania 16508
(814) 838-3571

M-tron Ind. Inc.
P.O. Box 630
Yankton, South Dakota 57078
(605) 665-9321

Erie Frequency Control
453 Lincoln St.
Calisle, Pennsylvania 17013
(714) 249-2232

APPLICATIONS INFORMATION

OPERATION WITH A CRYSTAL

The BR1941 Baud Rate Generator may be driven by either a crystal or TTL level clock. When using a crystal, the waveform that appears at pins 1 (XTAL/EXT 1) and 18 (XTAL/EXT 2) does not conform to the normal TTL limits of $V_{IL} \leq 0.8V$ and $V_{IH} \geq 2.0V$. Figure 1 illustrates a typical crystal waveform when connected to a BR1941.

Since the D.C. level of the waveform causes the least positive point to typically be greater than 0.8V, the BR1941 is designed to look for an edge, as opposed to a TTL level. The XTAL/EXT logic triggers on a rising edge of typically 1V in magnitude. This allows the use of a crystal without any additional components.

OPERATIONS WITH TTL LEVEL CLOCK

With clock frequencies in the area of 5 MHz, significant overshoot and undershoot ("ringing") can appear at pins 1 and/or 18. The BR1941, may, at times, be triggered on a rising edge of an overshoot or undershoot waveform, causing the device to effectively "double-trigger." This phenomenon may result as a twice expected baud rate, or as an apparent device failure. Figure 2 shows a typical waveform that exhibits the "ringing" problem.

The design methods required to minimize ringing include the following:

1. Minimize the P.C. trace length. At 5 MHz, each inch of trace can add significantly to overshoot and undershoot.
2. Match impedances at both ends of the trace. For example, a series resistor near the BR1941 may be helpful.
3. A uniform impedance is important. This can be accomplished through the use of:
   a. parallel ground lines
   b. evenly spaced ground lines crossing the trace on the opposite side of PC board
   c. an inner plane of ground, e.g., as in a four layered PC board.

In the event that ringing exists on an already finished board, several techniques can be used to reduce it. These are:

1. Add a series resistor to match impedance as shown in Figure 3.
2. Add pull-up/pull-down resistor to match impedance, as shown in Figure 4.
3. Add a high speed diode to clamp undershoot, as shown in Figure 5.

The method that is easiest to implement in many systems is method 1, the series resistor. The series resistor will cause the D.C. level to shift up, but that does not cause a problem since the BR1941 is triggered by an edge, as opposed to a TTL level.

The BR1941 Baud Rate Generator can save both board space and cost in a communications system. By choosing either a crystal or a TTL level clock, the user can minimize the logic required to provide baud rate clocks in a given design.

POWER LINE SPIKES

Voltage transients on the AC power line may appear on the DC power output. If this possibility exists, it is suggested that one by-pass capacitor is used between + 5V and GND and another between + 12V and GND.

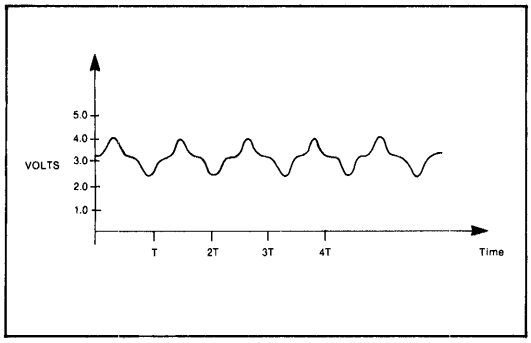


Figure 1 TYPICAL CRYSTAL WAVEFORM

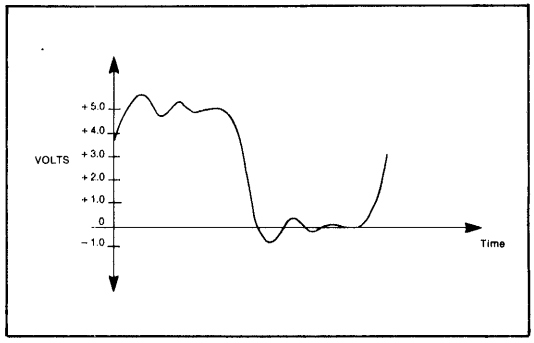


Figure 2 TYPICAL "RINGING" WAVEFORM

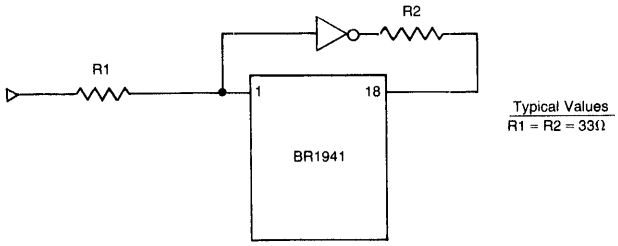


Figure 3 SERIES RESISTOR TO MATCH IMPEDANCE

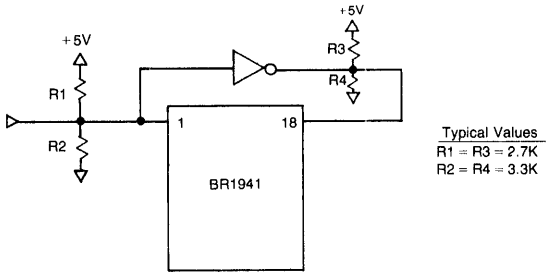


Figure 4 PULL-UP/PULL-DOWN RESISTORS TO MATCH IMPEDANCE

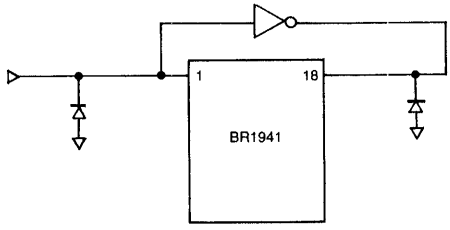


Figure 5 HIGH-SPEED DIODE TO CLAMP UNDERSHOOT

See page 725 for ordering information.

Printed in U.S.A.

WD1943(8116)/WD1945(8136) Dual Baud Rate Clock

FEATURES

- 16 SELECTABLE BAUD RATE CLOCK FREQUENCIES
- OPERATES WITH CRYSTAL OSCILLATOR OR EXTERNALLY GENERATED FREQUENCY INPUT
- ROM MASKABLE FOR NON-STANDARD FREQUENCY SELECTIONS
- INTERFACES EASILY WITH MICROCOMPUTERS
- OUTPUTS A 50% DUTY CYCLE CLOCK WITH 0.01% ACCURACY
- 6 DIFFERENT FREQUENCY/DIVISOR PAIRS AVAILABLE
- SINGLE +5V POWER SUPPLY
- COMPATIBLE WITH BR1941
- TTL, MOS COMPATIBILITY

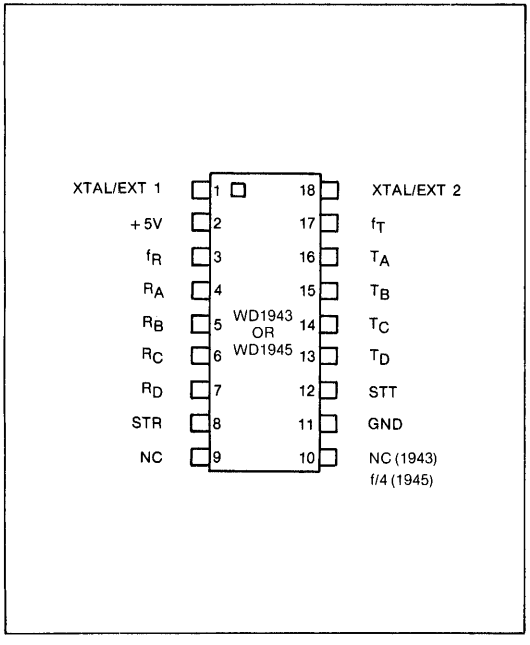
- WD1943 IS PIN COMPATIBLE TO THE COM8116
- WD1945 IS PIN COMPATIBLE TO THE COM8136 AND COM5036 (PIN 9 ON WD1945 IS A NO CONNECT)

GENERAL DESCRIPTION

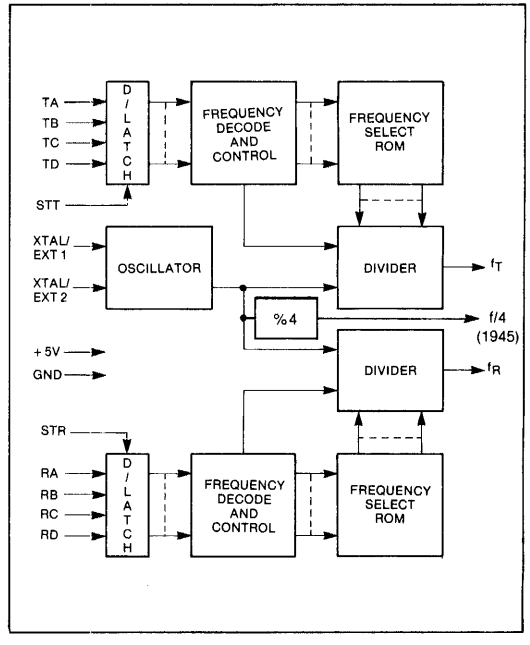
The WD1943/45 is an enhanced version of the BR1941 Dual Baud Rate Clock. The WD1943/45 is a combination Baud Rate Clock Generator and Programmable Divider. It is manufactured in N-channel MOS using silicon gate technology. This device is capable of generating 16 externally selected clock rates whose frequency is determined by either a single crystal or an externally generated input clock. The WD1943/45 is a programmable counter capable of generating a division by any integer from 4 to $2^{15} - 1$, inclusive.

The WD1943/45 is available programmed with the most used frequencies in data communication. Each frequency is selectable by strobing or hard wiring each of the two sets of four Rate Select inputs. Other frequencies/division rates can be generated by reprogramming the internal ROM coding through a MOS mask change. Additionally, further clock division may be accomplished through cascading of devices. The frequency output is fed into the XTAL/EXT input on a subsequent device.

The WD1943/45 can be driven by an external crystal or by TTL logic.



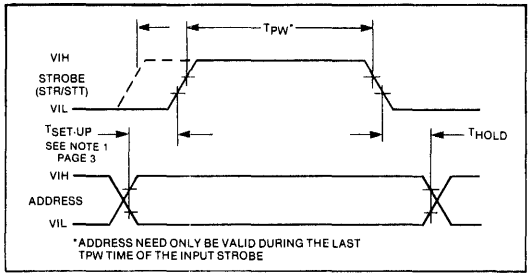
PIN CONNECTIONS



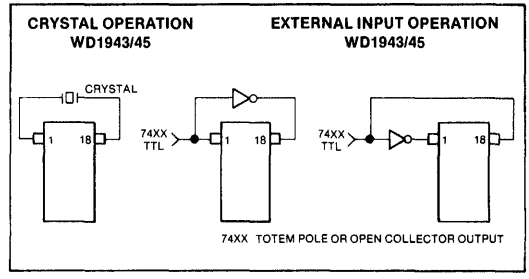
BLOCK DIAGRAM

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	XTAL/EXT 1	Crystal or External Input 1	This input receives one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+5 volt Supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver Address inputs.
4-7	R_A, R_B, R_C, R_D	Receiver Address	The logic level on these inputs as shown in Table 1 thru 6, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver Address	A high-level input strobe loads the receiver address (R_A, R_B, R_C, R_D) into the receiver address register. This input may be strobed or hard wired to +5V.
9	NC	No Connection	No Internal Connection
10	NC (1943) f/4 (1945)	No Connection freq/4 Output	No Internal Connection XTAL1 input freq divided by four.
11	GND	Ground	Ground
12	STT	Strobe-Transmitter Address	A high-level input strobe loads the transmitter address (T_A, T_B, T_C, T_D) into the transmitter address register. This input may be strobed or hard wired to +5V.
13-16	T_D, T_C, T_B, T_A	Transmitter Address	The logic level on these inputs, as shown in Table 1 thru 6, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter Address inputs.
18	XTAL/EXT 2	Crystal or External Input 2	This input receives the other pin of the crystal package or the other polarity of the external input.



CONTROL TIMING



CRYSTAL/CLOCK OPTIONS

ABSOLUTE MAXIMUM RATINGS

Positive Voltage on any Pin, with respect to ground	+7.0V
Negative Voltage on any Pin, with respect to ground	−0.3V
Storage Temperature	(plastic package) −55°C to +125°C (Cerdip package and Ceramic package) −65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+325°C

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and Functional Operation of the device at these or at any other condition above those indicated in the operational sections of this specification are not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = +5V ±5% standard.)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	See Note 1
High-level, V_{IH}	2.0		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL} = 3.2 mA
High-level, V_{OH}	V_{CC}-1.5	4.0		V	I_{OH} = 100μA
INPUT CURRENT			−10	μA	V_{IN} = V_{CC} STR (8) and STT (12)
High-level, I_{IH}			10	μA	V_{IN} = GND Only
Low-level, I_{IL}			300	μA	V_{IN} = GND (All inputs except XTAL, STR and STT)
Low-level, I_{IL}			10	μa	V_{IN} = GND STR, STT
INPUT CAPACITANCE					
All Inputs, C_{IN}		5	10	pf	V_{IN} = GND, excluding XTAL inputs
EXT. INPUT LOAD		4	5		Series 7400 unit loads
INPUT RESISTANCE					
Crystal Input, R_{XTAL}	1.1			KΩ	Resistance to ground for Pin 1 and Pin 18
POWER SUPPLY CURRENT I_{CC}		40	80	mA	
AC CHARACTERISTICS					T_A = +25°C
CLOCK FREQUENCY					See Note 2
PULSE WIDTH (T_{PW})					
Clock					50% Duty Cycle ± 10%. See Note 2
Receiver strobe	150		DC	ns	See Note 3
Transmitter strobe	150		DC	ns	See Note 3
INPUT SET-UP TIME (T_{SET-UP})					
Address	50			ns	See Note 3
OUTPUT HOLD TIME (T_{HOLD})					
Address	50			ns	
STROBE TO NEW FREQUENCY DELAY			6	CLK	

NOTE 1: XTAL/EXT inputs are either TTL compatible or crystal compatible. See crystal specification in Applications Information section.
All inputs except XTAL, STR and STT have internal pull-up resistors.

NOTE 2: Refer to frequency option tables for maximum input frequency on XTAL/EXT pins.
Typical clock pulse width is 1/2 x CL

NOTE 3: Input set-up time can be decreased to >0 ns by increasing the minimum strobe width (50 ns) to a total of 200 ns.
T_{A-D} and R_{A-D} have internal pull-up resistors.

OPERATION

Standard Frequencies

Choose a Transmitter and Receiver frequency from the table below. Program the corresponding address into TA-TD and RA-RD respectively using strobe pulses or by hard wiring the strobe and address inputs.

Non-Standard Frequencies

To accomplish non-standard frequencies do one of the following:

1. Choose a crystal that when divided by the WD1943 generates the desired frequency.
2. Cascade devices by using the frequency outputs as an input to the XTAL/EXT inputs of the subsequent WD1943/45.
3. Consult the factory for possible changes via ROM mask reprogramming.

FREQUENCY OPTIONS

TABLE 1. CRYSTAL FREQUENCY = 5.0688 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	0.8	—	50/50	6336
0	0	0	1	75	1.2	1.2	—	50/50	4224
0	0	1	0	110	1.76	1.76	—	50/50	2880
0	0	1	1	134.5	2.152	2.1523	0.016	50/50	2355
0	1	0	0	150	2.4	2.4	—	50/50	2112
0	1	0	1	300	4.8	4.8	—	50/50	1056
0	1	1	0	600	9.6	9.6	—	50/50	528
0	1	1	1	1200	19.2	19.2	—	50/50	264
1	0	0	0	1800	28.8	28.8	—	50/50	176
1	0	0	1	2000	32.0	32.081	0.253	50/50	158
1	0	1	0	2400	38.4	38.4	—	50/50	132
1	0	1	1	3600	57.6	57.6	—	50/50	88
1	1	0	0	4800	76.8	76.8	—	50/50	66
1	1	0	1	7200	115.2	115.2	—	50/50	44
1	1	1	0	9600	153.6	153.6	—	48/52	33
1	1	1	1	19,200	307.2	316.8	3.125	50/50	16

WD1943-00 or WD1945-00

TABLE 2. CLOCK FREQUENCY = 2.76480 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	0.8	—	50/50	3456
0	0	0	1	75	1.2	1.2	—	50/50	2304
0	0	1	0	110	1.76	1.76	−0.006	50/50	1571
0	0	1	1	134.5	2.152	2.152	−0.019	50/50	1285
0	1	0	0	150	2.4	2.4	—	50/50	1152
0	1	0	1	200	3.2	3.2	—	50/50	864
0	1	1	0	300	4.8	4.8	—	50/50	576
0	1	1	1	600	9.6	9.6	—	50/50	288
1	0	0	0	1200	19.2	19.2	—	50/50	144
1	0	0	1	1800	28.8	28.8	—	50/50	96
1	0	1	0	2000	32.0	32.15	+0.465	50/50	86
1	0	1	1	2400	38.4	38.4	—	50/50	72
1	1	0	0	3600	57.6	57.6	—	50/50	48
1	1	0	1	4800	76.8	76.8	—	50/50	36
1	1	1	0	9600	153.6	153.6	—	50/50	18
1	1	1	1	19,200	307.2	307.2	—	50/50	9

WD1943-02 or WD1945-02

TABLE 3. CRYSTAL FREQUENCY = 6.018305 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	.7999	0	50/50	7523*
0	0	0	1	75	1.2	1.2000	0	50/50	5015*
0	0	1	0	110	1.76	1.7597	0	50/50	3420
0	0	1	1	134.5	2.152	2.1517	0	50/50	2797*
0	1	0	0	150	2.4	2.3996	0	50/50	2508
0	1	0	1	200	3.2	3.1995	0	50/50	1881*
0	1	1	0	300	4.8	4.7993	0	50/50	1254
0	1	1	1	600	9.6	9.5986	0	50/50	627*
1	0	0	0	1200	19.2	19.2279	+0.14	50/50	31.3*
1	0	0	1	1800	28.8	28.7959	0	50/50	209*
1	0	1	0	2000	32.0	32.0125	0	50/50	188
1	0	1	1	2400	38.4	38.3334	−0.17	50/50	157*
1	1	0	0	3600	57.6	57.8687	+0.46	50/50	104
1	1	0	1	4800	76.8	77.1583	+0.46	50/50	78
1	1	1	0	9800	153.6	154.3166	+0.46	50/50	39*
1	1	1	1	19,200	307.2	300.9175	−2.04	50/50	20

WD1943-03 or WD1945-03

TABLE 4. CLOCK FREQUENCY = 5.52960 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(32X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	1.6	1.6	—	50/50	3456
0	0	0	1	75	2.4	2.4	—	50/50	2304
0	0	1	0	110	3.52	3.52	−0.006	50/50	1571
0	0	1	1	134.5	4.304	4.303	−0.019	50/50	1285
0	1	0	0	150	4.8	4.8	—	50/50	1152
0	1	0	1	200	6.4	6.4	—	50/50	864
0	1	1	0	300	9.6	9.6	—	50/50	576
0	1	1	1	600	19.2	19.2	—	50/50	288
1	0	0	0	1200	38.4	38.4	—	50/50	144
1	0	0	1	1800	57.6	57.6	—	50/50	96
1	0	1	0	2000	64.0	64.3	+0.465	50/50	86
1	0	1	1	2400	76.8	76.8	—	50/50	72
1	1	0	0	3600	115.2	115.2	—	50/50	48
1	1	0	1	4800	153.6	153.6	—	50/50	36
1	1	1	0	9600	307.2	307.2	—	50/50	18
1	1	1	1	19,200	614.4	614.4	—	50/50	9

WD1943-04 or WD1945-04

TABLE 5. CRYSTAL FREQUENCY = 4.9152 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	0.8	—	50/50	6144
0	0	0	1	75	1.2	1.2	—	50/50	4096
0	0	1	0	110	1.76	1.7598	−0.01	*	2793
0	0	1	1	134.5	2.152	2.152	—	50/50	2284
0	1	0	0	150	2.4	2.4	—	50/50	2048
0	1	0	1	300	4.8	4.8	—	50/50	1024
0	1	1	0	600	9.6	9.6	—	50/50	512
0	1	1	1	1200	19.2	19.2	—	50/50	256
1	0	0	0	1800	28.8	28.7438	−0.19	*	171
1	0	0	1	2000	32.0	31.9168	−0.26	50/50	154
1	0	1	0	2400	38.4	38.4	—	50/50	128
1	0	1	1	3600	57.6	57.8258	0.39	*	85
1	1	0	0	4800	76.8	76.8	—	50/50	64
1	1	0	1	7200	115.2	114.306	−0.77	*	43
1	1	1	0	9600	153.6	153.6	—	50/50	32
1	1	1	1	19,200	307.2	307.2	—	50/50	16

WD1943-05 or WD1945-05

TABLE 6. CRYSTAL FREQUENCY = 5.0688 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(32X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	1.6	1.6	—	50/50	3168
0	0	0	1	75	2.4	2.4	—	50/50	2112
0	0	1	0	110	3.52	3.52	—	50/50	1440
0	0	1	1	134.5	4.304	4.303	.026	50/50	1178
0	1	0	0	150	4.8	4.8	—	50/50	1056
0	1	0	1	200	6.4	6.4	—	50/50	792
0	1	1	0	300	9.6	9.6	—	50/50	528
0	1	1	1	600	19.2	19.2	—	50/50	264
1	0	0	0	1200	38.4	38.4	—	50/50	132
1	0	0	1	1800	57.6	57.6	—	50/50	88
1	0	1	0	2400	76.8	76.8	—	50/50	66
1	0	1	1	3600	115.2	115.2	—	50/50	44
1	1	0	0	4800	153.6	153.6	—	*	33
1	1	0	1	7200	230.4	230.4	—	50/50	22
1	1	1	0	9600	307.2	298.16	2.941	*	17
1	1	1	1	19,200	614.4	633.6	3.125	50/50	8

*When the duty cycle is not exactly 50% it is 50% ± 10%

WD1943-06 or WD1945-06

APPLICATIONS INFORMATION

OPERATION WITH A CRYSTAL

The WD1943/45 Baud Rate Generator may be driven by either a crystal or TTL level clock. When using a crystal, the waveform that appears at pins 1 (XTAL/EXT 1) and 18 (XTAL/EXT 2) does not conform to the normal TTL limits of $V_{IL} \leqslant 0.8V$ and $V_{IH} \geqslant 2.0V$. Figure 1 illustrates a typical crystal waveform when connected to a WD1943/45.

Since the D.C. level of the waveform causes the least positive point to typically be greater than 0.8V, the WD1943/45 is designed to look for an edge, as opposed to a TTL level. The XTAL/EXT logic triggers on a rising edge of typically 1V in magnitude. This allows the use of a crystal without any additional components.

OPERATIONS WITH TTL LEVEL CLOCK

With clock frequencies in the area of 5 MHz, significant overshoot and undershoot ("ringing") can appear at pins 1 and/or 18. The clock oscilator may, at times be triggered on a rising edge of an overshoot or undershoot waveform, causing the device to effectively "double-trigger." This phenomenon may result as a twice expected baud rate, or as an apparent device failure. Figure 2 shows a typical waveform that exhibits the "ringing" problem.

The design methods required to minimize ringing include the following:

1. Minimize the P.C. trace length. At 5 MHz, each inch of trace can add significantly to overshoot and undershoot.
2. Match impedances at both ends of the trace. For example, a series resistor near the device may be helpful.
3. A uniform impedance is important. This can be accomplished through the use of:
   a. parallel ground lines
   b. evenly spaced ground lines crossing the trace on the opposite side of PC board
   c. an inner plane of ground, e.g., as in a four layered PC board.

In the event that ringing exists on an already finished board, several techniques can be used to reduce it. These are:

1. Add a series resistor to match impedance as shown in Figure 3.
2. Add pull-up/pull-down resistor to match impedance, as shown in Figure 4.
3. Add a high speed diode to clamp undershoot, as shown in Figure 5.

The method that is easiest to implement in many systems is method 1, the series resistor. The series resistor will cause the D.C. level to shift up, but that does not cause a problem since the OSC is triggered by an edge, as opposed to a TTL level.

The 1943/45 Baud Rate Generator can save both board space and cost in a communications system. By choosing either a crystal or a TTL level clock, the user can minimize the logic required to provide baud rate clocks in a given design.

POWER LINE SPIKES

Voltage transients on the AC power line may appear on the DC power output. If this possibility exists, it is suggested that a by-pass capacitor is used between + 5V and GND.

CRYSTAL SPECIFICATIONS

User must specify termination (pin, wire, other)
Frequency — See Tables 1-6.
Temperature range 0°C to + 70°C
Series resistance $\leqslant 50\Omega$
Series resonant
Overall tolerance ± 0.01%

CRYSTAL MANUFACTURERS (Partial List)

American Time Products Div.
Frequency Control Products, Inc.
61-20 Woodside Ave.
Woodside, New York 11377
(213) 458-5811

Bliley Electric Co.
2545 Grandview Blvd.
Erie, Pennsylvania 16508
(814) 838-3571

M-tron Ind. Inc.
P.O. Box 630
Yankton, South Dakota 57078
(605) 665-9321

Erie Frequency Control
453 Lincoln St.
Calisle, Pennsylvania 17013
(714) 249-2232

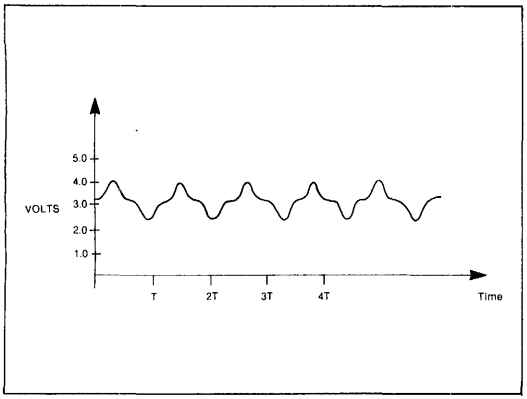


Figure 1. TYPICAL CRYSTAL WAVEFORM

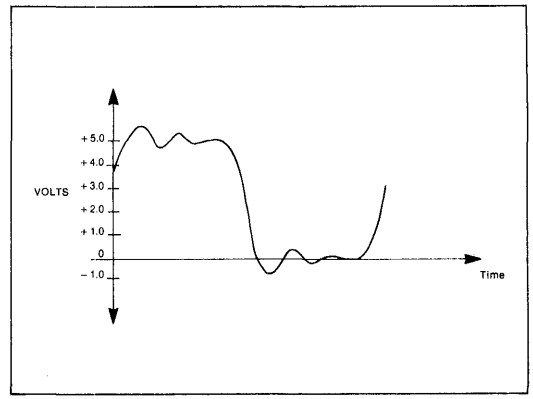


Figure 2. TYPICAL "RINGING" WAVEFORM from TTL INPUT

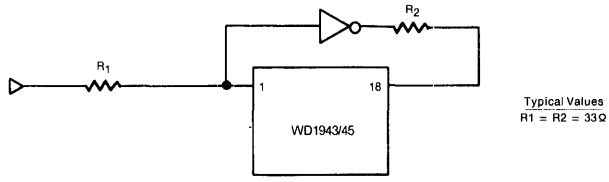


Figure 3. SERIES RESISTOR TO MATCH IMPEDANCE

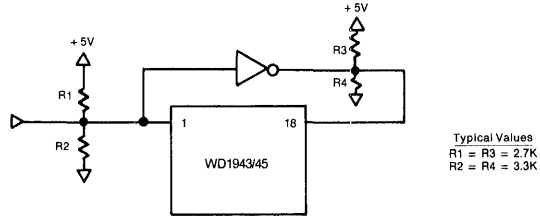


Figure 4. PULL-UP/PULL-DOWN RESISTORS TO MATCH IMPEDANCE

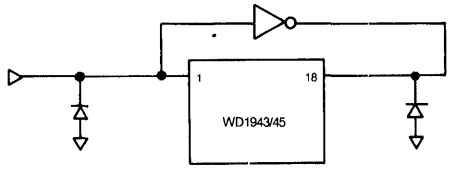


Figure 5. HIGH-SPEED DIODE TO CLAMP UNDERSHOOT

See page 725 for ordering information.

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WESTERN DIGITAL
CORPORATION

PR1472 (PSAR)
Programmable Synchronous & Asynchronous Receiver

FEATURES

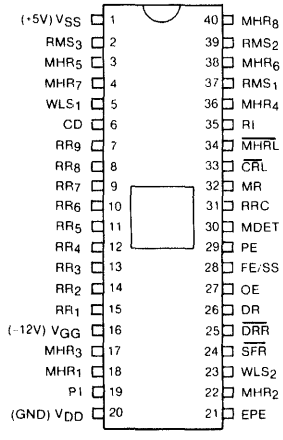
- SYNCHRONOUS, ASYNCHRONOUS OR ISOCHRONOUS OPERATION
- DC TO 640K BITS/SEC (1X CLOCK) PR1472-01; DC TO 100K BITS/SEC PR1472
- PROGRAMMABLE MATCH (FILL) CHARACTER WITH MATCH DETECT FLAG.
- INTERNAL OR EXTERNAL CHARACTER SYNCHRONIZATION
- NINE BIT WIDE RECEIVER HOLDING REGISTER
- SELECTABLE 5, 6, 7 OR 8 BITS PER CHARACTER
- EVEN/ODD OR NO PARITY SELECT
- PROGRAMMABLE CLOCK RATE; 1X, 16X, 32X OR 64X
- AUTOMATIC START AND STOP BIT STRIPPING
- AUTOMATIC CHARACTER STATUS AND FLAG GENERATION
- THREE STATE OUTPUTS — BUS STRUCTURE CAPABILITY
- DOUBLE BUFFERED
- TTL & DTL COMPATIBLE — INTERNAL ACTIVE PULLUP
- COMPATIBLE TRANSMITTER, PT1482

GENERAL DESCRIPTION

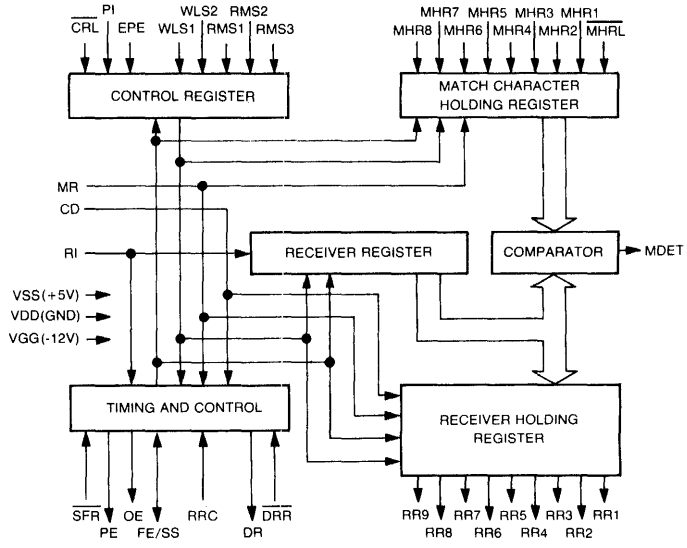
The Western Digital PR1472 (PSAR) is a programmable receiver that interfaces variable length serial data to a parallel data channel. The receiver converts a serial data stream into parallel characters with a format compatible with all standard Synchronous, Asynchronous, or Isochronous data communications media.

Contiguous synchronous serial characters are compared to a programmable Match-Character Holding Register, character synchronized and assembled. Programming the Asynchronous or Isochronous Mode provides assembly of characters with start and stop bit(s) which are stripped from the data. Four internal registers, in conjunction with Three-State Outputs provide full system versatility.

The PSAR is a TTL compatible device. The use of internal active pull-up devices and push-pull output drivers, provides direct compatibility with all forms of current sinking logic. Western Digital also offers a Compatible Transmitter, the PT1482.



PIN CONNECTIONS



PR1472 BLOCK DIAGRAM

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
1	POWER SUPPLY	V_{SS}	+5 Volt Supply
37, 39, 2	RECEIVER MODE SELECT	RMS_1, RMS_2, RMS_3	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables RMS_1, RMS_2, and RMS_3 inputs. The Receiver Mode Select Inputs, in conjunction with the Control Register Load and Chip Disable, select the Receiver operating mode. RMS_1, RMS_2, and RMS_3 may be strobed or hard-wired to the appropriate input voltage.
			RMS_3 / RMS_2 / RMS_1 / Selected Operating Mode 0 0 0 ASYNCH OR ISOCH, 1X CLOCK 0 0 1 ASYNCH OR ISOCH, 16X CLOCK 0 1 0 ASYNCH OR ISOCH, 32X CLOCK 0 1 1 ASYNCH OR ISOCH, 64X CLOCK 1 X 0 SYNCH-EXTERNAL CHARACTER SYNCHRONIZATION 1 X 1 SYNCH-INTERNAL CHARACTER SYNCHRONIZATION
			NOTE: When operating in asynchronous or isochronous mode with 1X clock there is no protection against false start bits.
			A high-level input voltage, V_{IH}, applied to CD disables RMS_1, RMS_2 and RMS_3.
18,22 17, 36, 3, 38, 4, 40	MATCH-CHARACTER HOLDING REGISTER DATA	MHR_1, MHR_2, MHR_3, MHR_4, MHR_5, MHR_6, MHR_7, MHR_8	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the inputs to the Match-Character Holding Register Load, $\overline{MHRL}$. Parallel 8-bit characters are input into the Match-Character Holding Register with the $\overline{MHRL}$ Strobe (pin 34). If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), only the least significant bits are accepted. These inputs may be strobed or hard-wired to the appropriate input voltage. A high-level input voltage, V_{IL}, applied to CD disables MHR_1 and MHR_8.
5,23	WORD LENGTH SELECT	WLS_1, WLS_2	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the inputs of the Control Register Load, $\overline{CRL}$. Parallel 8-bit characters are input into the Control Register with the $\overline{CRL}$ Strobe (pin 4), WLS_1 and WLS_2 select the transmitted character length from five (5) to eight (8) bits defined by the Truth Table below:
			WLS_2 / WLS_1 / Selected Word Length V_{IL} V_{IL} 5 BITS V_{IL} V_{IH} 6 BITS V_{IH} V_{IL} 7 BITS V_{IH} V_{IH} 8 BITS
			WLS_1 and WLS_2 may be strobed or hard-wired to the appropriate input voltage. A high-level input voltage, V_{IH}, applied to CD disables WLS_1 and WLS_2.

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
6	CHIP DISABLE	CD	This line controls the disable associated with busable inputs and Three-State outputs. A high-level input voltage, V_{IH}, applied to this line disables inputs and removes drive from push-pull output buffers causing them to float. Drivers of disables outputs are not required to sink or source current. The I/O Lines controlled by Chip Disable are defined below: **Input Lines** — **Three-State Output Lines** $\overline{CRL}$, $\overline{DRR}$, PE, RR_1-RR_8 EPE, $\overline{SFR}$, FE PI, $\overline{MHRL}$, OE WLS_1,WLS_2, MHR_1-MHR_8 RMS_1-RMS_3
7-15	RECEIVER HOLDING-REGISTER DATA OUTPUT	RR_9-RR_1	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the Receiver Holding Register outputs, RR_1-RR_9. The parallel data character, including parity (RR_9), appears on these lines. Program control selection of a word length less than eight (8) bits will cause the most significant bits of the character to be forced to a low-level output voltage, V_{OL}. The character will be right justified. RR_1 (pin 15) is the least significant bit of the character. A high-level input voltage, V_{IH}, applied to CD disables RR_1-RR_9.
16	POWER SUPPLY	V_{GG}	– 12 Volts Supply.
19	PARITY INHIBIT	PI	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the EPE and PI inputs.
20	POWER SUPPLY	V_{DD}	Ground = 0V
21	EVEN PARITY ENABLE	EPE	The Even Parity Enable Input and the Parity Inhibit Input to the Control Register, in conjunction with the Control Register Load and Chip Disable, select even, odd or no parity to be verified by the receiver. A high-level input voltage, V_{IH}, applied to EPE selects even parity and a low-level input voltage, V_{IL}, select odd parity if a low-level input voltage is applied to Parity Inhibit and Chip Disable. PI and EPE may be strobed or hard-wired to the appropriate input voltage. **PI** — **EPE** — **Selected Parity** — **Comments** V_{IL} — V_{IL} — Odd — CD = V_{IL} V_{IL} — V_{IH} — Even — CD = V_{IL} V_{IH} — X — None — CD = V_{IL} NOTE: If CD = V_{IH}, no programming is performed since inputs are disabled. X — either V_{IL} or V_{IH}. When programmed, the appropriate parity is verified following the last data bit of a character, immediately preceding the stop element of asynchronous and isochronous characters. A high-level input voltage, V_{IH}, applied to CD disables EPE, PI, and $\overline{CRL}$.
29	PARITY ENABLE	PE	A high-level input V_{IH} enables parity. A low level input V_{IH} disables parity.

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
24	STATUS FLAG RESET	$\overline{SFR}$	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the $\overline{SFR}$ input. A low-level input voltage, V_{IL}, applied to this line resets the PE, FE and OE Status Flags.
25	DATA RECEIVED RESET	$\overline{DRR}$	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the $\overline{DRR}$ input. A low-level input voltage, V_{IL}, applied to this line resets the DR Flag. A high-level input voltage, V_{IH}, applied to CD disables $\overline{DRR}$.
26	DATA RECEIVED FLAG	DR	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the Receiver Holding Register. When operating in the synchronous mode, the first SYN character, when located and transferred to the Receiver Holding Register, will not cause DR to go to a high-level output voltage, V_{OH}, but will cause MDET to go to a high-level output voltage. Character transfer to the Receiver Holding Register occurs in the center of the last bit of a synchronous character or the center of the first STOP element of an asynchronous or isochronous character at which time this flag is updated.
27	OVERRUN ERROR FLAG	OE	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the OE input. A high-level output voltage, V_{OH}, indicates that the prevously received character was not read (DR line not reset) and was, therefore, lost before the present character was transferred to the Receiver Holding Register. This transfer occurs in the center of the last bit of a received synchronous character or in the center of the first STOP element of an asynchronous or isochronous character at which time this flag is updated. A high-level input voltage, V_{OH}, applied to CD disables OE.
28	FRAMING ERROR/ SYN SEARCH	FE/SS	FE/SS is a two-way (I/O) bus. If programmed for the ASYNCHRONOUS or ISOCHRONOUS MODE, a low-level input voltage, V_{IL}, applied to CD (pin 6) enables the FRAMING ERROR FLAG output which indicates the status of the STOP BIT detection circuit. A high-level output voltage, V_{OH}, indicates that the character transferred to the Receiver Holding Register has no valid STOP BIT; i.e., the bit following the PARITY BIT is not a high-level input voltage, V_{IH}. This transfer occurs in the center of the first stop element at which time this flag is updated. When programmed for the SYNCHRONOUS MODE, this line is an input and is not under control of CD. This line should be driven by a tri-state or an open collector device. If programmed for INTERNAL CHARACTER SYNCHRONIZATION, a transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, initiates the automatic internal "SYN" CHARACTER search operation.

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
28	FRAMING ERROR/ SYN SEARCH	FE/SS	Prior to initiation of this operation, the Receiver Holding Register is "transparent" so that its contents are identical to that of the RECEIVER REGISTER. Upon receipt of a SYN character, (previously loaded into the Match-Character Holding Register during initialization), the Receiver Holding Register becomes non-transparent, the MATCH DETECT output (MDET) goes to a high-level output voltage. V_{OH}, but, the Data Received (DR) FLAG does not assume a high-level output voltage, V_{OH}. The P/SAR is now in character synchronization. Subsequent SYN or data character will be transferred to the RECEIVER HOLDING REGISTER as they are assembled (at the center of the last bit) and the DR FLAG will be raised. A transition from a high-level input voltage, V_{IH}, to a low-level input voltage, V_{IL}, causes the P/SAR to lose character synchronization and forces the Receiver Holding Register to become "transparent." If programmed for EXTERNAL CHARACTER SYNCHRONIZATION, the system external to the P/SAR examines the data stream for "SYN" characters when SYN SEARCH is a low-level input voltage, V_{IL}. The Receiver Holding Register is "transparent" which allows the contents of the RECEIVER REGISTER to be monitored as it ripples through the shift register. When the external logic locates a "SYN" CHARACTER, indicated by a high-level input voltage, V_{OH}, on MDET, the SYN SEARCH line is externally raised to a high-level input voltage, V_{IH}. This high-level input voltage causes character synchronization to be initiated, returns the Receiver Holding Register to a "non-transparent" condition, causing subsequent characters to be transferred to the RECEIVER HOLDING REGISTER (when the center of the last bit of a character is recognized) and raises the DR FLAG.
30	MATCH DETECT FLAG	MDET	A high-level output voltage, V_{OH}, indicates that the contents of the Transmitter Register are identical to the contents of the Match-Character Holding Register. This flag is set to a high-level output voltage, V_{OH}, at the center of the first STOP ELEMENT of an asynchronous or isochronous character.
31	RECEIVER REGISTER CLOCK	RRC	This fifty (50) percent duty cycle clock provides the basic receiver timing. The negative transition from a high-level input voltage, V_{IH}, to a low-level input voltage, V_{IL}, shifts data into the RECEIVER REGISTER at a rate determined by RMS_1, RMS_2 and RMS_3. Synchronous operation requires that this negative transition occur at the center of each data bit.

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
32	MASTER RESET	MR	A high-level input voltage, V_{IH}, applied to this line resets timing and control logic to an idle state, sets the contents of the Receiver Holding Register to a high-level output voltage, V_{OH}, resets the contents of the Match-Character Holding Register, the MDET, DR, PE, FE, and OE outputs to a low-level output voltage, V_{OL}, but does not effect the contents of the control register.
33	CONTROL REGISTER LOAD	$\overline{CRL}$	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the $\overline{CRL}$ input. A low-level input voltage, V_{IL}, applied to this line enables inputs to DC "D Type" Latches of the Control Register and loads it with Control Bits (EPE, PI, RMS_1, RMS_2, RMS_3, WLS_1, WLS_2). A high-level input voltage, V_{IH}, applied to this line disables the Control Register. This line may be strobed or hard-wired to a low-level input voltage, V_{IL}. A high-level input voltage, V_{IH}, applied to CD disables CRL.
34	MATCH CHARACTER HOLDING REGISTER LOAD	$\overline{MHRL}$	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the $\overline{MHRL}$ input. A low-level input voltage, V_{IL}, applied to this line enables input to DC "D Type" Latches of the Match-Character Holding Register and loads it with the Match-Character Holding Register. This line may be strobed or hard-wired to a low-level input voltage, V_{IL}. A high-level input voltage, V_{IH}, applied to CD disables $\overline{MHRL}$.
35	RECEIVER INPUT	RI	The serial input data stream received on this line enters the Receiver Register determined by the character length, parity and the number of stop bits programmed. A high-level input voltage, V_{IH}, must be present when no ASYNCHRONOUS data is being received.

ORGANIZATION

PR1472 block diagram is illustrated on page 1.

Control Register — Programming of the PSAR is accomplished by loading the 7 Bit Control register. Mode selection, clock division, word length, and parity are selected when the Control Register Load (CRL) signal is activated.

Receiver Register — The Receiver Register is used to store the incoming data stream. The contents of this register can be gated to the Holding register during the transparent mode, or compared with the Match Holding Register. When a character is assembled it is transferred to the Receiver Holding Register.

Receiver Holding Register — The Receiver Holding Register, a buffer register, is used to store the assembled character.

Match Holding Register — The Match Holding Register is used to store the match character. The contents of this register are compared with the receiver register to establish character synchronization.

Timing & Control — The Timing and Control Logic generates the required control signals to assemble characters, match comparison, bit stripping, and generation of status/flag signals.

SYNCHRONOUS MODE OPERATION

Synchronous data appears as a continuous bit stream of contiguous characters at the input to the receiver with no Start or Stop bits. Character synchronization (the "framing" of this continuous bit stream into characters of a predetermined fixed length), must be accomplished by a comparison of this bit stream and a synchronization sequence. The P/SAR is designed to accommodate internal or external character synchronization by program control.

Referring to the Block Diagram of the Receiver, the Chip Disable (CD) enables or disconnects various in-

puts and outputs of the P/SAR. This feature provides the device with the capability of being disconnected from the system bus. The inputs to the Control Register and Match-Character Holding Register and their respective load strobes, $\overline{CRL}$ and $\overline{MHRL}$ are under CD control. In addition, DRR, SFR, PE, and OE and the outputs of the Receiver Holding Register, are also controlled by CD. It is necessary that CD enable these lines to allow strobing information in these registers and to allow examination of these output flags and data.

Device operation is programmed subsequent to being forced into its "idle" state. The P/SAR will enter a defined "idle" state when the Master Reset (MR) line is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the contents of the Receiver Holding Register is set to a high-level output voltage and all output flags are reset to a low-level output voltage. The Master Reset also causes the contents of the Match-Character Holding Register to be reset to a low-level output voltage.

Enabled by CD, the Control Register is loaded by strobing $\overline{CRL}$ to a low-level input voltage which defines mode of operation and clock rate selection, character length and selected parity if required. Table 1 illustrates all programmable synchronous formats.

Character synchronization from the data stream requires Receiver recognition of specific bit pattern(s) which define the relative position of synchronous characters in the data stream and subsequent character assembly. The P/SAR programmably accommodates internal or external character synchronization.

Programmed for internal character synchronization, a high-level input voltage on the Sync Search line, the Receiver Holding Register is "transparent" and its contents are identical to the Receiver Holding Register. The data stream, gated into the Receiver Input (RI) by the negative transition of the Receiver Register Clock (RRC), shifts through the Receiver Register and is compared with the preprogrammed character in the Match-Character Holding Register. A match, indicated by a high-level output voltage on Match Detect (MDET), returns the Receiver Holding register to its non-transparent state and initializes timing and control logic but does not set the Data Received Flag to a high-level output voltage. The character following the match will be transferred to the Receiver Holding Register at the receipt of the center of its last bit and the Data Received Flag is set to a high-level output voltage. Depending on line discipline, this last character may also be a synchronizing character, in which case, Match Detect will continue to be a high-level output voltage when the Data Received Flag is set. Therefore, sequence verification can be performed by the system (additional hardware or software as desired).

Parity, if programmed, is verified upon receipt of the center of the parity bit which is the last bit of a synchronous character. If a parity error exists, the associated PE register is set to a high-level output voltage.

Transfer of a character to the Receiver Holding Register sets the associated Data Received Register Flag (DR) to a high-level output voltage. The transfer of a character to the Receiver Holding Register, if the Data Received Register Flag had already been set to a high-level output voltage, causes the previous character to be lost (written over) and is alerted by an Overrun Error Flag which is a high-level output voltage. In normal operation, the Data Received Flag is reset by $\overline{DRR}$ when the Receiver Holding Register is serviced (unloaded). The Status Flags, PE and OE, are also provided with an external reset $\overline{SFR}$ so that block status and character status may be (accumulated) verified. A low-level input voltage on Sync Search causes character synchronization to be lost and initiates transparency of the Receiver Holding Register.

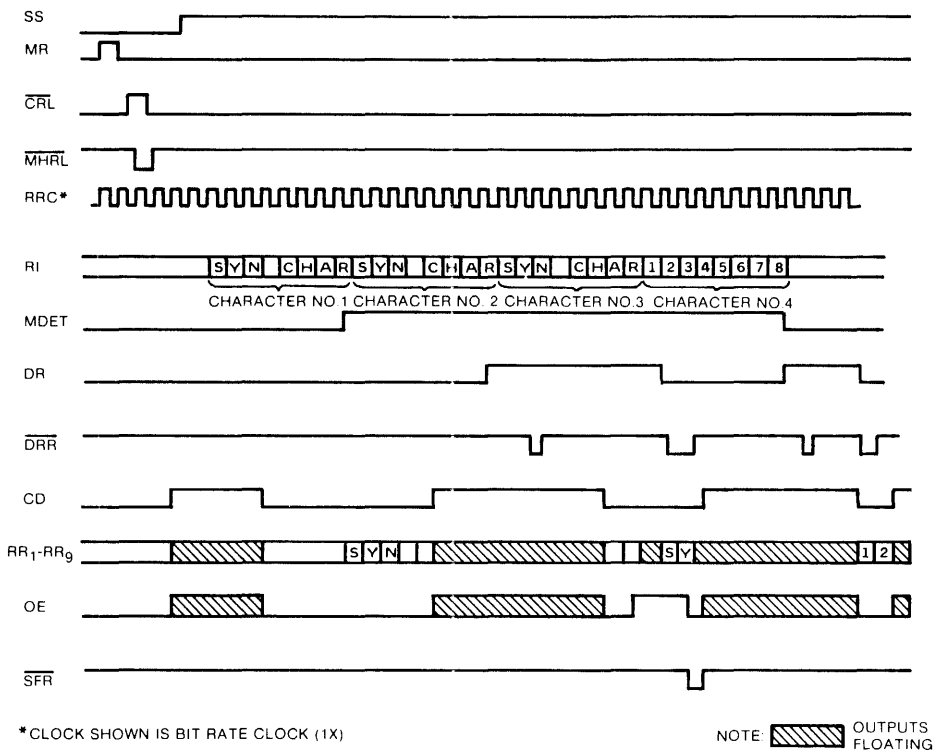
External character synchronization, programmed by the Control Register, is similar to the description above with the exception that the Sync Search line controls the nontransparency of the Receiver Holding Register directly and comparison is done externally. Upon recognition of the appropriate synchronizing pattern, the Sync Search line is set to a high-level input voltage prior to the end of the last bit. Raising the Sync Search line to a high-level input voltage causes the buffer to go "nontransparent", initializing timing and control circuitry to "frame" characters. The first bit received after a high-level input voltage is applied to Sync Search, defines the start of the "frame". Character length defined by the Control Register defines the end of the "frame".

Table 1. SYNC MODE CONTROL DEFINITION

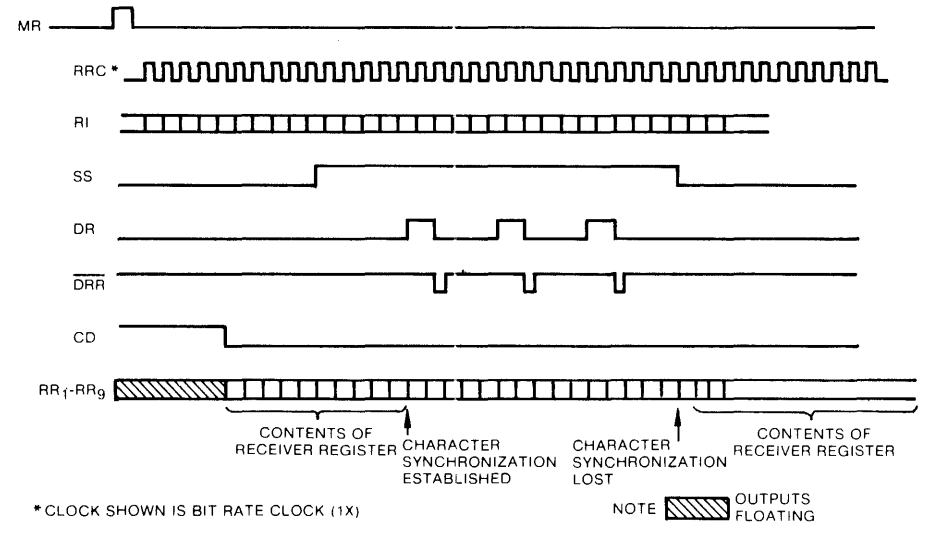
CONTROL WORD					CHARACTER FORMAT	
RMS3	WL2	WL1	PI	EPE	DATA BITS	PARITY BIT CHECKED
1	0	0	0	0	5	ODD
1	0	0	0	1	5	EVEN
1	0	0	1	X	5	NONE
1	0	1	0	0	6	ODD
1	0	1	0	1	6	EVEN
1	0	1	1	X	6	NONE
1	1	0	0	0	7	ODD
1	1	0	0	1	7	EVEN
1	1	0	1	X	7	NONE
1	1	1	0	0	8	ODD
1	1	1	0	1	8	EVEN
1	1	1	1	X	8	NONE
↑ Sets to SYNC Mode						

If RMS_1 = 1, the receiver operates in the internal character SYNC mode.

If RMS_1 = 0, character SYNC must be externally provided.



(INTERNAL SYNCHRONIZATION)



(EXTERNAL SYNCHRONIZATION)

SYNCHRONOUS TIMING DETAIL

ASYCHRONOUS & ISOCHRONOUS MODE

The completed assembly of a parallel character, by the P/SAR, from a serial data stream and buffered by its Receiver Holding Register is indicated by the status of the Data Received (DR) Flag. The assembly of character from a serial data stream consisting of a start bit, data, parity (if programmed), and a stop interval is initiated by the Start bit transition.

Verification of parity and receipt of a valid stop bit is accomplished prior to the character transfer to the Receiver Holding Register. Simultaneously, this data is compared with a preprogrammed character in the Match-Character Holding Register.

Status Flags, Data Received, Parity Error, Framing Error, Overrun Error and Match Detect are loaded into status registers during character transfer to the Receiver Holding Register.

Referring to the Block Diagram of the Receiver, the Chip Disable enables or disconnects various inputs and outputs of the P/SAR. This feature provides the device with the capability of being disconnected from the system bus. The inputs to the Control Register and Match-Character Holding Register and their respective load strobes, $\overline{CRL}$ and $\overline{MHRL}$ are under CD control. In addition, $\overline{DRR}$, $\overline{SFR}$, PE, FE, OE and the outputs of the Receiver Holding Register are also controlled by CD. It is necessary that CD enable these lines to allow strobing information into these registers and to allow examination of these output data and flags.

Device operation is programmed subsequent to being forced into its "idle" state. The P/SAR will enter a defined "idle" state when the Master Reset (MR) line is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the contents of the Receiver Holding Register is set to a high-level output voltage, and all output flags are reset to a low-level output voltage. The Master Reset also causes the contents of the Match-Character Holding Register to be reset to a low-level output voltage.

When the Receiver is enabled by CD, loading the Control Register by strobing the Control Register Load ($\overline{CRL}$) line to a low-level input voltage defines the mode of operation and clock rate selection, character length and selected parity if required. Table 2 illustrates all the programmable asynchronous formats.

A mark to space transition on the receiver input initializes the clock counter causing it to count to the theoretical center of the start bit. At this time, the input is sampled. A high-level input voltage at the Receiver Input causes the first mark to space transition to be interpreted as a noise spike and resets all timing and control logic. This provides one-half data bit noise immunity on all clock selection rates except 1X. A low-level input voltage at the Receiver Input at the theoretical center of the start bit causes timing and control circuitry to sample the theoretical center of succeeding data bits. This data is shifted through the Receiver Register. When an entire character (as defined by the Control Register) is assembled in the Receiver Register, the line is "tested" for a valid stop bit at its theoretical center. This character is also compared with the contents of the Match-Character Holding Register at the center of the stop bit and its parity is verified. A parallel transfer occurs, loading the contents of the Receiver Register (less start and stop bits) into the Receiver Holding Register. The status of the parity verification, framing error, and overrun error circuitry are also loaded into their approriate registers to provide output error flags when the Data Received Flag is set. If the Data Received Flag had not been reset prior to the assembly of the current character, the previous character is lost and this is indicated by a high-level output voltage on the Overrun Error Flag.

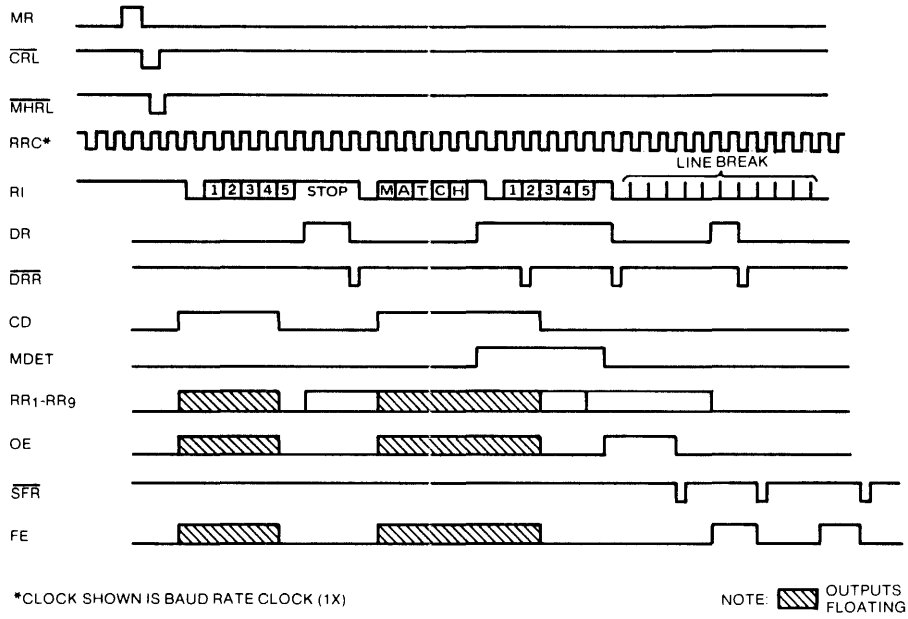
Table 2. ASYNCHRONOUS OR ISOCHRONOUS MODE CONTROL DEFINITION

RMS3	WLS2	WLS1	PI	EPE	Start Bit	Data Bits	Added Parity Bit	Stop Elements
0	0	0	0	0	1	5	Odd	1 or more
0	0	0	0	1	1	5	Even	1 or more
0	0	0	1	X	1	5	None	1 or more
0	0	1	0	0	1	6	Odd	1 or more
0	0	1	0	1	1	6	Even	1 or more
0	0	1	1	X	1	6	None	1 or more
0	1	0	0	0	1	7	Odd	1 or more
0	1	0	0	1	1	7	Even	1 or more
0	1	0	1	X	1	7	None	1 or more
0	1	1	0	0	1	8	Odd	1 or more
0	1	1	0	1	1	8	Even	1 or more
0	1	1	1	X	1	8	None	1 or more

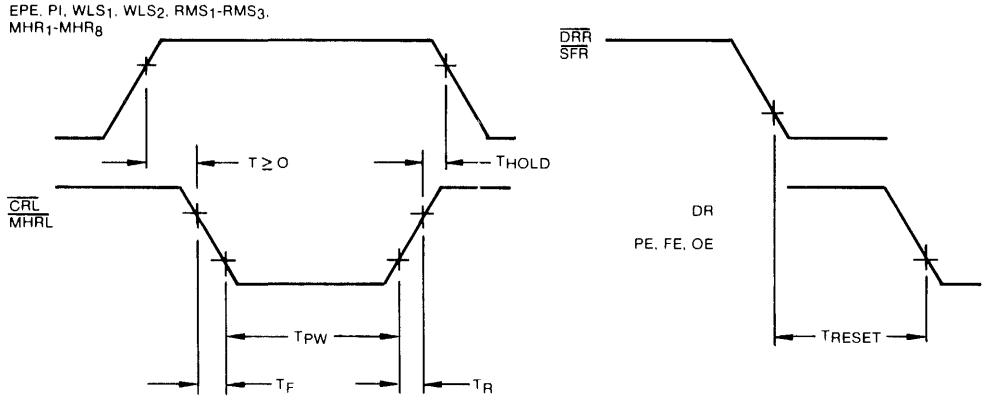
↑ Set to ASYNC or ISOC Mode

When RMS_3 is 0 (ASYNC or ISOC Mode), RMS_2 and RMS_3 determine the clock frequency according to the following table:

RMS_2	RMS_1	Clock Frequency
0	0	1X Baud Rate
0	1	16X Baud Rate
1	0	32X Baud Rate
1	1	64X Baud Rate

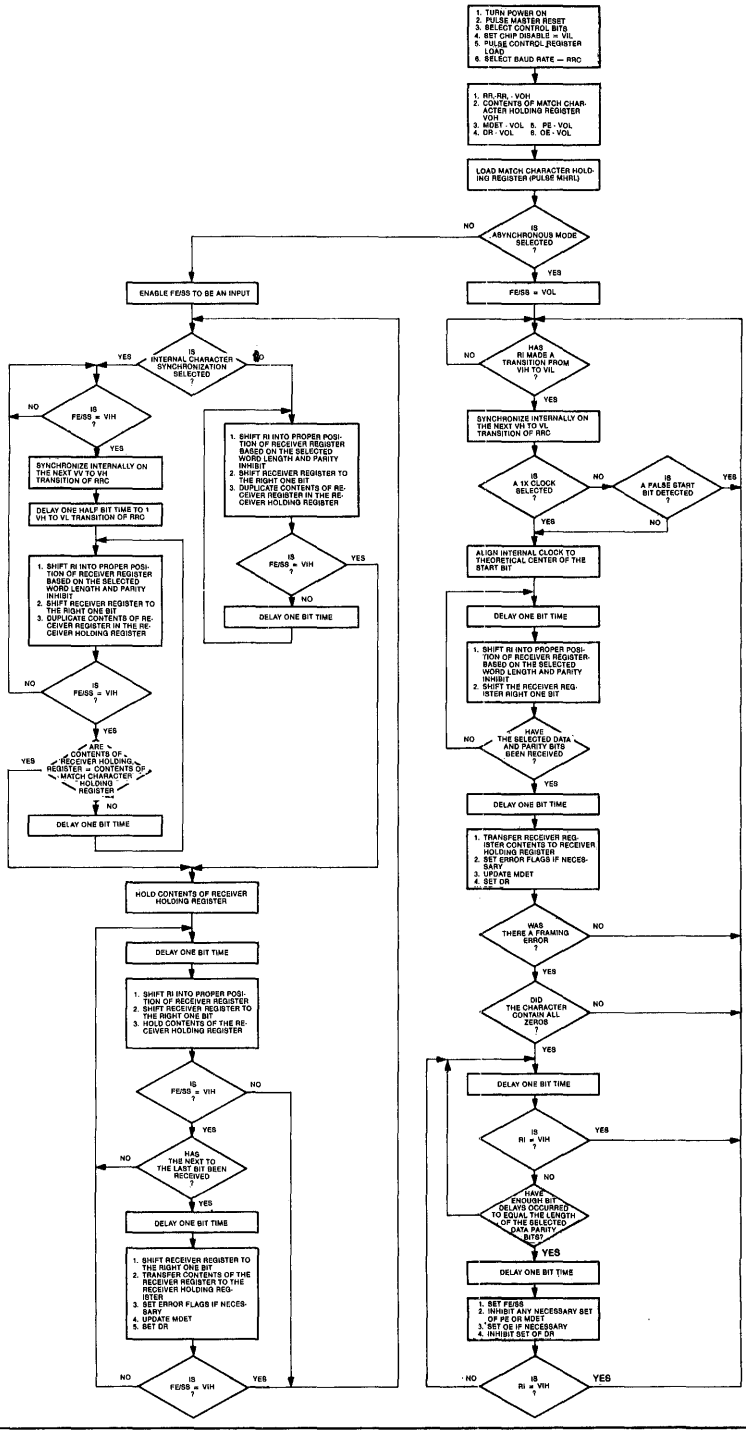


ASYNCHRONOUS & ISOCHRONOUS TIMING EXAMPLE

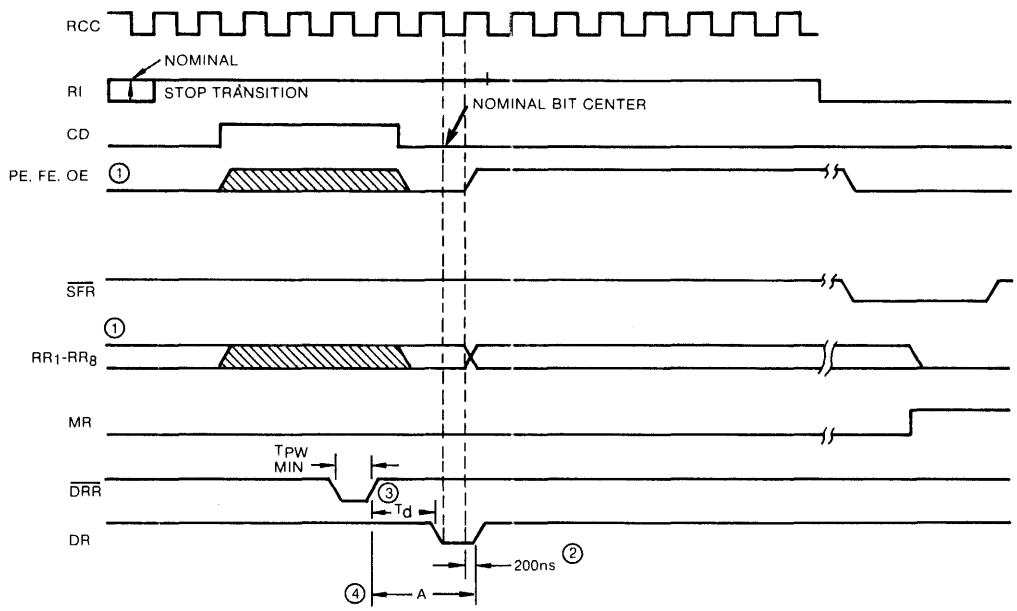


DATA INPUT LOAD CYCLE **RESET DELAY**

SWITCHING WAVEFORMS

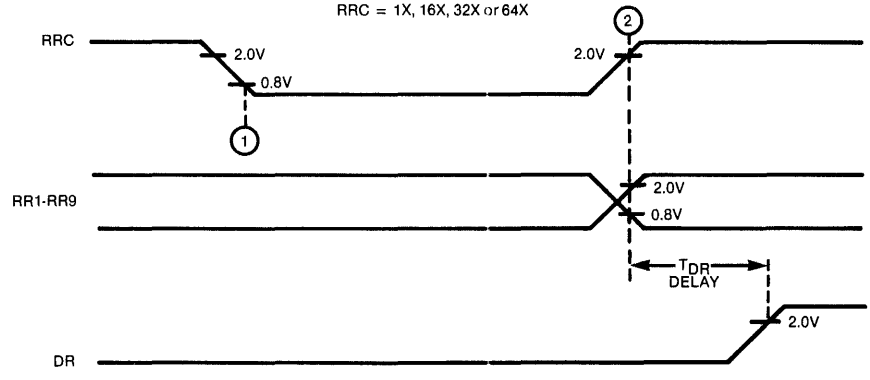


PR1472 SYNCHRONOUS ASYNCHRONOUS RECEIVER FLOW CHART



1. DATA AND ERROR FLAGS ARE VALID AT THE TIMENAL CENTER OF THE FIRST STOP BIT + ½ CLOCK.
2. DR IS DELAYED 200ns FROM DATA AND ERROR FLAGS
3. THE DELAY BETWEEN DRR AND DR = T_d = 500ns
4. DRR SHOULD BE HIGH A MINIMUM OF "A" ns (T_d + ½ CLOCK + 200ns) PRIOR TO THE NEXT RISING EDGE OF DR.

TIMING DETAIL



NOTES:
1. THE FALLING EDGE SHOWN REPRESENTS THE CENTER OF THE FIRST STOP BIT.
2. THE RISING EDGE SHOWN REPRESENTS THE FIRST RISING EDGE OF RRC AFTER THE CENTER OF THE FIRST STOP BIT.

Figure 1 PR1472 TIMING DETAIL

MAXIMUM RATINGS

V_{GG} Supply Voltage		+0.3V to −20V
V_{DD} Supply Voltage		+0.3V to −20V
Clock Input Voltage*		+0.3V to −20V
Logic Input Voltage*		+0.3V to −20V
Logic Output Voltage*		+0.3V to −20V
Storage Temperature	Ceramic	−65°C to +150°C
	Plastic	−55°C to +125°C
Operating Free-Air Temperature T_A Range		0°C to +50°C
Lead Temperature (Soldering, 10 sec)		300°C

*V_{GG} = V_{DD} = OV

NOTE: These voltages are measured with respect to V_{SS} (Substrate).

ELECTRICAL CHARACTERISTICS

(V_{SS} = V_{CC} = 5V ± 5%, V_{DD} = OV, V_{GG} = −12V ± 5%, T_A = 0°C to +50°C unless otherwise specified.)

SYMBOL	PARAMETER	MIN.	MAX.	CONDITIONS
	INPUT LOGIC LEVELS[1]			
V_{IL}	Low-level Input Voltage		0.8V	V_{SS} = 4.75V
V_{IH}	High-level Input Voltage	V_{SS}-1.5V		
	OUTPUT LOGIC LEVELS[2]			
V_{OL}	Low-level Output Voltage		0.5V	V_{SS} = 5.25V I_{OL} = 1.6mA
V_{OH}	High-level Output Voltage	V_{SS}-1.0V		V_{SS} = 4.75V I_{OH} = −100μA
	INPUT CURRENT[1]			
I_{IL}	Low-level Input Current (each input)		−1.6mA	V_{SS} = 5.25V V_{IN} = 0.4V
I_{LO}	Output Leakage Current		10μA	

NOTE: 1) Inputs under Chip Disable control when disabled, (V_{IH} applied to CD), are logically disabled and appear as a single TTL Load.

2) Outputs under Chip Disable control when disabled (V_{IH} applied to CD), are logically and electrically disconnected and caused to float. The Three-State Output has three stages; (1) Low impedance to V_{CC} (2) Low impedance to GND (3) High impedance OFF ≃ 10 Megohm.

SWITCHING CHARACTERISTICS

(V_{SS}-V_{CC} = 5V, V_{DD} = 0V, V_{GG} = −12V, T_A = 25°C, C_L = 20 pf)

SYMBOL	PARAMETER	MIN.	MAX.	CONDITIONS
F_C	Clock Frequency	DC	100 KHz	PR1472-00
		DC	640 KHz	PR1472-01
	PULSE WIDTH			
T_{HOLD}	Hold Time	20 nsec		
T_{CRL}	Control Register Load	250 nsec		
T_{MHRL}	Match-Character Holding Register Load	250 nsec		
T_{DRR}	Data Received Reset	200 nsec		
T_{SFR}	Status Flag Reset	200 nsec		
T_{MR}	Master Reset	500 nsec		
T_{PD}	Output Enable Delay		500 nsec	
T_R	Rise Time		150 nsec	
T_F	Fall Time		150 nsec	
$T_{DR\ DELAY}$	Data Ready Delay Time		200 nsec	

See page 725 for ordering information.

Printed in U.S.A.

PT1482 (PSAT)
Programmable Synchronous & Asynchronous Transmitter

FEATURES

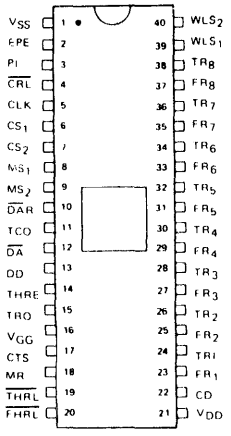
- SYNCHRONOUS, ASYNCHRONOUS OR ISOCHRONOUS OPERATION
- DC TO 640K BITS/SEC, 1X CLOCK PT1482-01
- DC TO 100K BITS/SEC, 1X CLOCK PT1482-00
- PROGRAMMABLE MATCH (FILL) CHARACTER
- SELECTABLE 5,6,7, OR 8 BIT PER CHARACTER
- EVEN/ODD PARITY GENERATOR. PARITY INHIBIT
- PROGRAMMABLE CLOCK RATE 1X, 16X, 32X, OR 64X.
- AUTOMATIC START & STOP BIT GENERATION IN ASYNCHRONOUS & ISOCHRONOUS MODES
- PROGRAMMABLE 1 AND 2 STOP BITS, (1½ IN 5 LEVEL MODE)
- AUTOMATIC CHARACTER STATUS AND DELIMITING SIGNAL GENERATION
- THREE STATE OUTPUTS — BUS STRUCTURE COMPATIBILITY
- DOUBLE BUFFERED
- TTL AND DTL COMPATIBLE — INTERNAL ACTIVE PULL UP
- COMPATIBLE RECEIVER, PR1472.

GENERAL DESCRIPTION

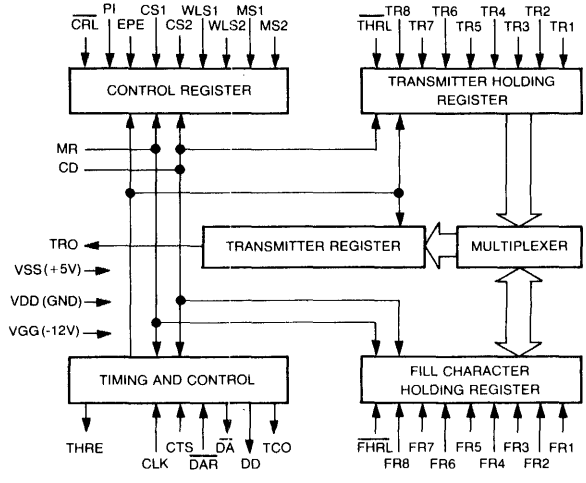
The Western Digital PT1482 (PSAT) is a programmable transmitter that interfaces variable length parallel data to a serial data channel. The transmitter converts parallel characters into a serial data stream with a format compatible with all standard Synchronous, Asynchronous or Isoschronous data communications media.

Contiguous serial characters are transmitted in the Synchronous Mode with the automatic insertion of a programmable Fill (Idle) Character during the absence of parallel input data. Programming the Asynchronous Mode selects serial transmission with automatic insertion of Start and Stop Bits. Isoschronous mode selects transmission with automatic fill character insertion during the absence of parallel input data. Four internal registers and a multiplexer, in conjunction with Three-State Output Lines, provide full system versatility.

The PSAT is a TTL compatible device. The use of internal active pull-up devices and push-pull output drivers, provides direct compatibility with all forms of current sinking logic. Western Digital also offers a compatible Receiver, PR1472.



PIN CONNECTIONS



PT1482 BLOCK DIAGRAM

PIN OUTS

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
1	V_{SS} POWER SUPPLY	V_{SS}	+ 5 Volt Supply
2	EVEN PARITY ENABLE	EPE	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the EPE and PI Inputs.
3	PARITY INHIBIT	PI	The Even Parity Enable Input and the Parity Inhibit Input to the Control Register, in conjunction with the Control Register Load and Chip Disable, select even, odd or no parity to be generated by the Transmitter. A high-level input voltage, V_{IH}, applied to EPE selects even parity and a low-level input voltage, V_{IL}, selects odd parity if a low-level input voltage is applied to Parity Inhibit and Chip Disable.
			PI / EPE / SELECTED PARITY / COMMENTS V_{IL} / V_{IL} / ODD / CD = V_{IL} V_{IL} / V_{IH} / EVEN / CD = V_{IL} V_{IH} / X / NONE / CD = V_{IL}
			NOTE: IF CD = V_{IH}, NO PROGRAMMING IS PERFORMED SINCE INPUTS ARE DISABLED.
			X – either V_{IL} or V_{IH} When programmed, the appropriate parity is generated following, and is contiguous with, the last data bit of a character, immediately preceding the stop element of asychronous and isochronous characters.
			A high-level input voltage, V_{IH}, applied to CD disables EPE, PI, and $\overline{CRL}$.
4	$\overline{CONTROL\ REGISTER\ LOAD}$	$\overline{CRL}$	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{CRL}$ input.
			A low-level input voltage, V_{IL}, applied to this line enables DC Latches of the Control Register and loads it with Control Bits (EPE, PI, CS_1, CS_2, MS_1, MS_2, WLS_1, WLS_2). A high-level input voltage, V_{IH}, applied to this line disables the Control Register. This line may be strobed or hard-wired to a low-level input voltage, V_{IL}. A high-level input voltage, V_{IH}, applied to CD, disables $\overline{CRL}$.
5	TRANSMITTER REGISTER CLOCK	TRC	This is a fifty (50) percent duty cycle clock. The positive going edge of this Clock shifts data out of the Transmitter Register at a rate determined by the Control Bits CS_1 and CS_2, and provides the basic time reference for all device functions.
6-7	CLOCK RATE SELECT	CS_1-CS_2	A low-level input voltage, V_{IL}, applied to CD enables the CS_1 and CS_2 inputs. These two lines select the internal clock rate divider ratio to produce the transmitter bit rate defined by the Truth Table below:
			CS_2 / CS_1 / SELECTED CLOCK INPUT RATE V_{IL} / V_{IL} / 1X BIT RATE V_{IL} / V_{IH} / 16X BIT RATE V_{IH} / V_{IL} / 32X BIT RATE V_{IH} / V_{IH} / 64X BIT RATE

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
			A high-level input voltage, V_{IH}, applied to CD disables CS_1 and CS_2.
8-9	MODE SELECT	MS_1-MS_2	These lines may be strobed or hard-wired to the appropriate input voltage. A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the MS_1 and MS_2 inputs. These lines select the transmitter operating mode. **MS_2 MS_1 MODE** V_{IL} V_{IL} ASYNCHRONOUS — ONE STOP BIT V_{IL}* V_{IH}*ASYNCHRONOUS — TWO STOP BITS V_{IH} V_{IL} SYNCHRONOUS V_{IH} V_{IH} ISOCHRONOUS *Selects 1.5 stop bits for 5-level codes. A high-level input voltage, V_{IH}, applied to CD disables MS_1 and MS_2.
10	$\overline{\text{DATA NOT AVAILABLE}}$ RESET	$\overline{\text{DAR}}$	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{\text{DAR}}$ input. A low-level input voltage, V_{IL}, applied to this line resets the Data Not Available Flag. A high-level Input, V_{IH}, applied to CD disables $\overline{\text{DAR}}$. This input is not used during asynchronous operation.
11	TRANSMITTER CLOCK OUTPUT	TCO	This output is a clock at the transmitted bit rate. The negative going edge of this clock corresponds to the center of each transmitted data bit. The positive going edge corresponds to the start of each data bit transmission. All waveforms in this specification are referenced to TCO.
12	$\overline{\text{DATA NOT AVAILABLE}}$ FLAG	$\overline{\text{DA}}$	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{\text{DA}}$ input. A high-level output voltage, V_{OH}, on this line indicates that a Fill-Character has been transmitted, since a character was not loaded into the Transmitter Holding Register by the center of the last bit of a Synchronous Character or the center of the Stop Element of an Isochronous character. A high-level input voltage, V_{IH}, applied to CD disables $\overline{\text{DA}}$. This input is not used during asynchronous operation.
13	DATA DELIMIT/ END OF CHARACTER	DD/EOC	During asynchronous operation, a high-level output voltage, V_{OH}, indicates data is being transmitted. A low-level output voltage, V_{OL}, indicates that a Start or Stop Element is being transmitted. A low-level output voltage during synchronous operation indicates that the last bit of a character is being transmitted.

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
14	TRANSMITTER HOLDING REGISTER EMPTY	THRE	A low-level input voltage applied to CD (pin 22) enables the THRE input. A high-level output voltage, V_{OH}, on this line indicates the Transmitter Holding Register is empty and has transferred its contents to the Transmitter Register and may be loaded with a new character. This line goes to a low-level output voltage, V_{OL}, when THRL goes to a low-level input voltage, V_{IL}. A high-level input voltage, V_{IH}, applied to CD disables THRE.
15	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the Transmitter Holding Register are serially shifted out as an NRZ waveform on this line provided that a character was loaded into the Transmitter Holding Register prior to $\overline{DA}$ Flag (in Synchronous or Isochronous Modes). If a character was not loaded prior to a $\overline{DA}$ Flag, the contents of the Fill-Character Register are transmitted as the next character.
16	V_{GG} POWER SUPPLY	V_{GG}	– 12 Volts Supply.
17	CLEAR-TO-SEND	CTS	The Clear-To-Send Control initiates or disables transmission as a function of the state of this line. A high-level input voltage, V_{IH}, initiates serial data transmission provided a character has been loaded into the Transmitter Holding Register. A low-level input voltage, V_{IL}, applied to this line during transmission allows completion of that character only, after which the output will continue to mark until a high-level input voltage is applied.
18	MASTER RESET	MR	The rising edge of a high-level input voltage, V_{IH}, applied to this line resets timing and control logic to an idle state, sets THRE, the contents of the Fill-Character Holding Register, and TRO to a high-level output voltage, V_{OH}.
19	$\overline{\text{TRANSMITTER HOLDING REGISTER LOAD}}$	$\overline{THRL}$	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{THRL}$ input. A low-level input voltage, V_{IL}, applied to this line enables DC Latches of the Transmitter Holding Register and loads it with the Transmitter Holding Register data and forces THRE to a low-level output voltage, V_{OL}. A high-level input voltage, V_{IH}, applied to this line disables the Transmitter Holding Register. A high-level input voltage, V_{IH}, applied to CD disables $\overline{THRL}$.
20	$\overline{\text{FILL-CHARACTER HOLDING REGISTER LOAD}}$	$\overline{FHRL}$	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{FHRL}$ input. A low-level input voltage, V_{IL}, applied to this line enables DC Latches of the Fill-Character Holding Register and loads it with the Fill-Character Register data FR_1-FR_8. A high-level input voltage, V_{IH}, applied to this line disables the $\overline{FHRL}$ Register. This line may be strobed or hard-wired to a low-

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
			level input voltage, V_{IL}. This input is not used during asynchronous operation. A high-level input voltage, V_{IH}, applied to CD disables $\overline{FHRL}$.
21	V_{DD} POWER SUPPLY	V_{DD}	Ground.
22	CHIP DISABLE	CD	This line controls the disconnect associated with busable inputs and Three-State outputs. A high-level input voltage, V_{IH}, applied to this line removes drive from push-pull outputs causing them to float. Drivers of disabled inputs are required to sink or source current. The I/O Lines controlled by Chip Disable are defined below: **INPUT LINES** / **TRI-STATE OUTPUT LINES** $\overline{CRL}$, $\overline{THRL}$, $\overline{DA}$ EPE, $\overline{FHRL}$, THRE PI, FR_1-FR_8 CS_1-CS_2, TR_1-TR_8 $\overline{MS_1}$-MS_2, WLS_1, WLS_2 $\overline{DAR}$
23, 25 27, 29 31, 33 35, 37	FILL-CHARACTER HOLDING REGISTER DATA INPUTS	FR_1-FR_8	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs of the Fill-Character Holding Register and associated Load Strobe, $\overline{FHRL}$. Parallel 8-bit characters are input into the Fill-Character Holding Register with the $\overline{FHRL}$ Strobe (pin 20). If a character of less than 8 bits has been selected (by WLS_1 and WLS_2) only the least significant bits are accepted. These lines may be strobed or hard-wired to the appropriate input voltage. These inputs are not used during asynchronous operation. During Synchronous or Isochronous transmission, the Fill-Character is transmitted if a character was not loaded into the Transmitter Holding Register prior to a $\overline{DA}$ Flag; i.e., the Transmitter Holding Register did not contain a character at the center of the last bit being transmitted from the Transmitter Register. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted, Least Significant Bit (FR_1) to Most Significant Bit (FR_n) order. A high-level input voltage, V_{IH}, applied to CD disables FR_1-FR_8.
24, 26 28, 30 32, 34 36, 38	TRANSMITTER HOLDING REGISTER DATA INPUTS	TR_1-TR_8	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs to the Transmitter Holding Register and associated Load Strobe, $\overline{THRL}$. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), only the least significant bits are accepted. A high-level input

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
39-40	WORD LENGTH	WLS_1-WLS_2	voltage, V_{IH}, will cause a high-level output voltage to be transmitted, Least Significant Bit (TR_1) to Most Significant Bit (TR_n) order. A high-level input voltage, V_{IH}, applied to CD disables TR_1-TR_8. A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs of the Control Register and Load, $\overline{CRL}$. Parallel 8-bit characters are input into the Control Register with the $\overline{CRL}$ Strobe (pin 4), WLS_1 and WLS_2 select the transmitted character length from five (5) to eight (8) bits defined by the Truth Table below: **WLS_2 / WLS_1 / SELECTED WORD LENGTH** V_{IL} V_{IL} 5 BITS V_{IL} V_{IH} 6 BITS V_{IH} V_{IL} 7 BITS V_{IH} V_{IH} 8 BITS A high-level input voltage, V_{IH}, applied to CD disables WLS_1 and WLS_2, forcing them to float.

ORGANIZATION

PT1482 block diagram is illustrated on page 1.

Control Register — Programming of the PSAT is accomplished by loading the 8 Bit Control Register. Mode selection, clock divisor, word length, and parity are selected when the Control Register Load signal is activated.

Transmitter Register — The Transmitter Register is used to store the outgoing data stream. The contents of this register are derived from either the Transmitter Holding Register or the Fill (Match) Character Holding Register with the Control and Timing Logic automatically adding the required start and stop bits during Asynchronous and Isoschronous Modes.

Transmitter Holding Register — The Transmitter Holding Register, a buffer register, is used to store the parallel character to be serially transmitted.

Fill Character Holding Register — The Fill Character Holding Register is used to store the Fill (Match) Character which is transmitted during the absence of characters in the Transmitter Holding Register.

Timing and Control — The Timing and Control Logic generates the required control signals to transmit Data and Fill Characters. Character transmission status signals are also derived from this logic.

SYNCHRONOUS MODE OPERATION

Synchronous transmission requires that characters (programmably variable from 5 to 8 data bits plus parity) are contiguous with no start or stop bits. Since the requirement that characters are contiuous does not imply that the system servicing the transmitter always has ample time to load the Transmitter Holding Register, it is necessary that a character be transmitted when data has not been loaded into the Transmitter Holding Register. This character is defined as the Fill or Idle Character and a separate register has been provided to load this character upon initialization. The Fill-Character Holding Register is loaded by strobing the Fill-Character Holding Register Load ($\overline{FHRL}$) line or hard-wiring it to a low-level input voltage.

Referring the Block Diagram of the Transmitter, it can be seen that the Chip Disable (CD) enables or disconnects various inputs and outputs of the P/SAT. The inputs to the Control Register, Transmitter Holding Register, Fill-Character Holding Register and their respective load strobes, $\overline{CRL}$, $\overline{THRL}$, and $\overline{FHRL}$ are under CD control. In addition, the Transmitter Holding Register Empty (THRE) Flag, Data Not Available ($\overline{DA}$) Flag, and the Data Not Available Reset ($\overline{DAR}$) are also controlled by CD. It is necessary that CD enable these lines to allow strobing information into these registers and to allow examination of these output flags. The P/SAT will enter a defined "idle" state when the Master Reset (MR) is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the Transmitter Register Output continues to mark, the Transmitter Holding Register Flag is set to a high-level output voltage, the Data Delimit/End of Character (DD/EOC) Flag

is set to a low-level output voltage, and the contents of the Fill-Character Holding Register are forced to a high-level output voltage.

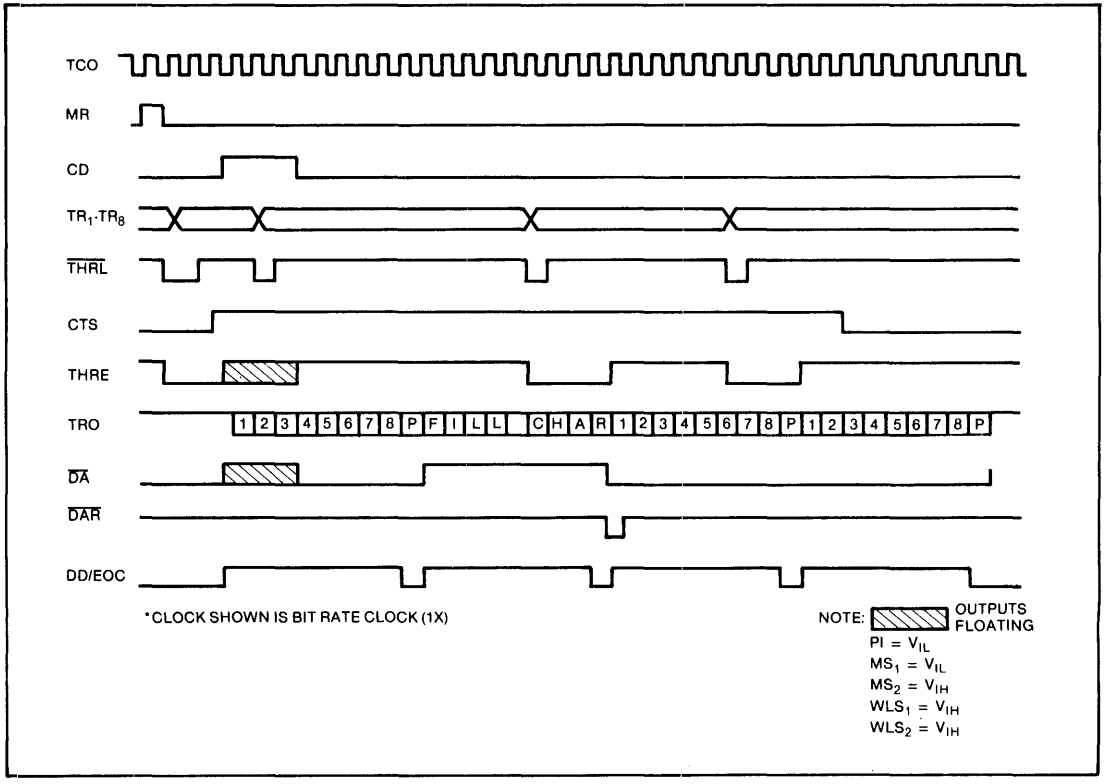
When the P/SAT is enabled by CD, loading the Control Register by strobing the Control Register Load ($\overline{CRL}$) line to a low-level input voltage, defines the mode of operation, character length, selected parity if required, and the clock rate selection. Table 1 illustrates all the programmable synchronous character formats.

To initialize transmission the CTS signal must be set to a high state and the transmitter holding register must be loaded with a character to be transmitted. The transmitter will remain in an idle state until this is accomplished.

The character transferred into the Transmitter Register (from the Transmitter Holding Register or the Fill-Character Holding Register) is determined at the center of the last bit of the character being transmitted. If, at this time, no character has been loaded into the Transmitter Holding Register, the Fill-Character is loaded into the Transmitter Register at the end of the bit being transmitted

Table 1. SYNC MODE CONTROL DEFINITION

CONTROL WORD						CHARACTER FORMAT	
MS 2	MS 1	WLS 2	WLS 1	PI	EP	DATA BITS	ADDED PARITY BIT
1	0	0	0	0	0	5	ODD
1	0	0	0	0	1	5	EVEN
1	0	0	0	1	X	5	NONE
1	0	0	1	0	0	6	ODD
1	0	0	1	0	1	6	EVEN
1	0	0	1	1	X	6	NONE
1	0	1	0	0	0	7	ODD
1	0	1	0	0	1	7	EVEN
1	0	1	0	1	X	7	NONE
1	0	1	1	0	0	8	ODD
1	0	1	1	0	1	8	EVEN
1	0	1	1	1	X	8	NONE
↑ Sets to SYNC Mode							



SYNCHRONOUS TIMING EXAMPLE

and a Data Not Available ($\overline{DA}$) Flag is set to a high-level output voltage. This Fill-Character will be repeatedly transmitted until a character is loaded into the Transmitter Holding Register, at which time, the Data Not Available Flag is reset, the Fill-Character will be completed and the newly loaded synchronous character will follow contiguously.

A high-level output voltage, on the THRE Flag indicates that the Transmitter Holding Register is empty and may be loaded with a character. Data on the inputs of the Transmitter Holding Register is loaded when the Transmitter Holding Register Load ($\overline{THRL}$) line is strobed to a low-level input voltage, forcing the THRE Flag to a low-level output voltage. This data must be stable prior to $\overline{THRL}$ going to a high-level input voltage since this register is a set of DC latches which are enabled by $\overline{THRL}$.

If the Clear-To-Send (CTS) line is at a low-level input voltage, or if the Transmitter Register is in the process of transmitting a character, the character in the Transmitter Holding Register will not be transferred down to the Transmitter Register and the THRE Flag will remain at a low-level output voltage. Raising the CTS line to a high-level input voltage or completion of transmission of a character from the Transmitter Register causes the automatic transfer of the character in the Transmitter Holding Register to the Transmitter Register which forces the THRE Flag to be set to high-level output voltage. The selected parity is added to the data during the transfer to the Transmitter Register and serial transmission is initiated as an NRZ waveform. A low-level input voltage applied to CTS during transmission allows completion of that character only, after which the device enters the idle state and the output will continue to mark until a high-level input voltage is applied.

The Data Delimit/End of Character Flag has been provided to indicate the transmission of serial data on the Transmitter Register Output. The Data Delimit/End of Character Flag is defined as a low-level output voltage during transmission of the last bit of a synchronous character and when the P/SAT is in the "idle" state.

ASYNCHRONOUS MODE OPERATION

An asynchronous character consisting of a start bit, followed by data (programmably variable from 5 to 8 data bits), parity (if so programmed), and a stop "element" is serially transmitted, in that order, as an NRZ waveform by the P/SAT. The stop interval is referred to as an "element" since its minimum length is under program control and may be 1 or 2 bits in length. When programmed for 2 stop bits, a 5-level (bit) code will be transmitted with 1.5 stop bits.

Referring to the Block Diagram of the Transmitter, it can be seen that the Chip Disable enables or disconnects various inputs and outputs of the P/SAT. The inputs to the Control Register, Transmitter Holding Register, Fill-Character Holding Register and their respective load strobes, $\overline{CRL}$, $\overline{THRL}$ and $\overline{FHRL}$ are under CD control. In addition, the Transmitter Holding Register Empty Flag (THRE), the Data Not Available Flag ($\overline{DA}$), and the Data Not Available Reset ($\overline{DAR}$) are also controlled by CD. It is necessary that CD enable these lines to allow strobing information into these registers and to allow examination of these output flags. It should be noted that the Fill-Character Holding Register and its associated load strobe, $\overline{FHRL}$, the Data Not Available Flag and its associated reset, $\overline{DAR}$, play no role in asynchronous communications and are only mentioned here for completeness.

The P/SAT will enter a defined "idle" state when the Master Reset (MR) line is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the Transmitter Register Output continues to mark, the Transmitter Holding Register Empty Flag is set to a high-level output voltage, V_{OH}, and the Data Delimit/End of Character (DD/EOC) Flag is reset to a low-level output voltage.

When the transmitter is enabled by CD, loading the Control Register by strobing the Control Register Load ($\overline{CRL}$) line to a low-level input voltage, V_{IL}, defines the mode of operation, character length, selected parity if required and the clock rate selection. Table 2 illustrates all the programmable asynchronous formats.

Continuous transmission, transmission of characters with the minimum number of stop bits programmed, is accomplished by loading the Transmitter Holding Register within a character time of when its "Empty Flag" becomes a high-level output voltage. A high-level output voltage, V_{OH}, on the Transmitter Holding Register Empty (THRE) Flag indicates that the Transmitter Holding Register is empty and may be loaded with a character. Data on the inputs of the Transmitter Holding Register is loaded when the Transmitter Holding Register Load ($\overline{THRL}$) line is strobed to a low-level input voltage, V_{IL}, forcing the THRE Flag to a low-level output voltage, V_{OL}. This data must be stable prior to $\overline{THRL}$ going to a high-level input voltage since this register is a set of DC latches which are enabled by $\overline{THRL}$. If the Clear-To-Send (CTS) line is at a low-level input voltage or if the Transmitter Register is in the process of transmitting a character, the character in the Transmitter Holding Register will not be transferred down to the Transmitter Register and the THRE Flag will remain at a low-level output voltage. Raising the CTS line to a high-level input voltage or comple-

tion of transmission of a character from the Transmitter Register causes the automatic transfer of the character in the Transmitter Holding Register to the Transmitter Register and the THRE flag will be set to a high-level output voltage.

The start bit, selected parity and stop bit(s), determined by the Control Register programming, are added to the data during the transfer to the Transmitter Register and serial transmission is initiated as an NRZ waveform.

A low-level input voltage, applied to CTS during transmission, allows completion of that character only, after which the output will continue to mark until a high-level input voltage is applied.

The Data Delimit/End of Character Flag has been provided to indicate the transmission of serial data on the Transmitter Register Output. Data Delimit is a low-level output voltage during start and stop bits and is a high-level output voltage during transmission of data and parity. Neither TRO, CTS nor DD/EOC is under control of Chip Disable.

ISOCHRONOUS MODE OPERATION

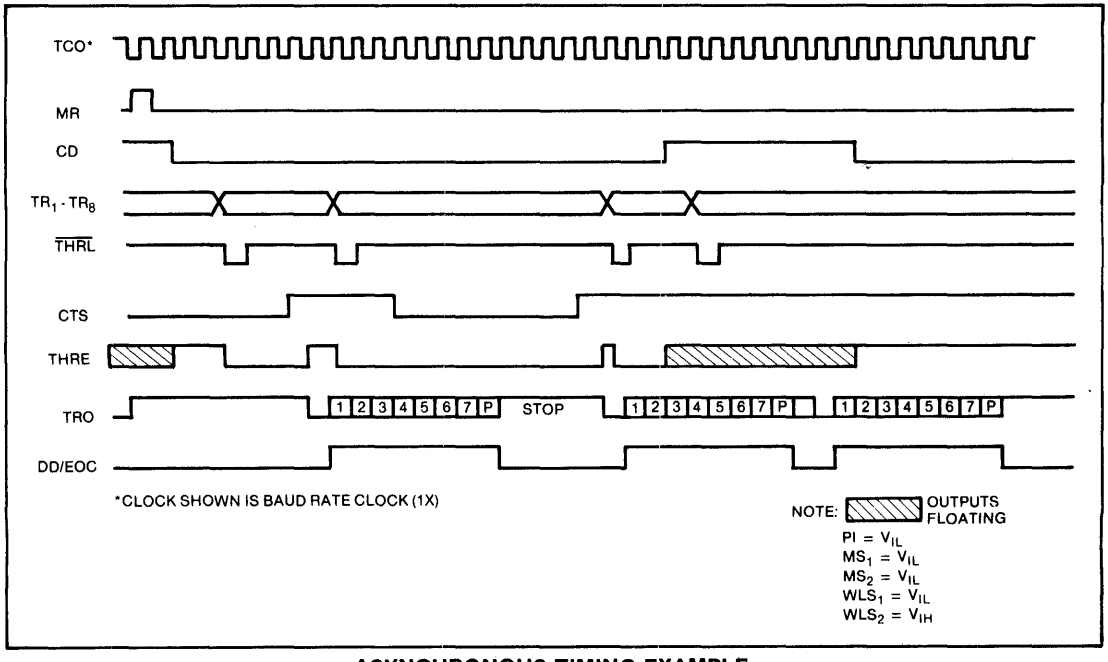
In the Isochronous Mode of operation all (Synchronous Mode) definitions apply with the exception of those for the Data Delimit/End of Character (DD/EOC) Flag and the Data Not Available Flag (DA).

This is the case since Isochronous Data Transmission requires contiguous characters with the addition of a start and a single stop bit added to each character.

Table 2. ASYNC MODE CONTROL DEFINITION

CONTROL WORD							CHARACTER FORMAT			
MSS2	MSS1	WLS2	WLS1	PI	EPE		START BIT	DATA BITS	ADDED PARITY BIT	STOP ELEMENTS
0	0	0	0	0	0		1	5	ODD	1
0	1	0	0	0	0		1	5	ODD	1.5
0	0	0	0	0	1		1	5	EVEN	1
0	1	0	0	0	1		1	5	EVEN	1.5
0	0	0	0	1	X		1	5	NONE	1
0	1	0	0	1	X		1	5	NONE	1.5
0	0	0	1	0	0		1	6	ODD	1
0	1	0	1	0	0		1	6	ODD	2
0	0	0	1	0	1		1	6	EVEN	1
0	1	0	1	0	1		1	6	EVEN	2
0	0	0	1	1	X		1	6	NONE	1
0	1	0	1	1	X		1	6	NONE	2
0	0	1	0	0	0		1	7	ODD	1
0	1	1	0	0	0		1	7	ODD	2
0	0	1	0	0	1		1	7	EVEN	1
0	1	1	0	0	1		1	7	EVEN	2
0	0	1	0	1	X		1	7	NONE	1
0	1	1	0	1	X		1	7	NONE	2
0	0	1	1	0	0		1	8	ODD	1
0	1	1	1	0	0		1	8	ODD	2
0	0	1	1	0	1		1	8	EVEN	1
0	1	1	1	0	1		1	8	EVEN	2
0	0	1	1	1	X		1	8	NONE	1
0	1	1	1	1	X		1	8	NONE	2

▲ Sets to ASYNC Mode



ASYNCHRONOUS TIMING EXAMPLE

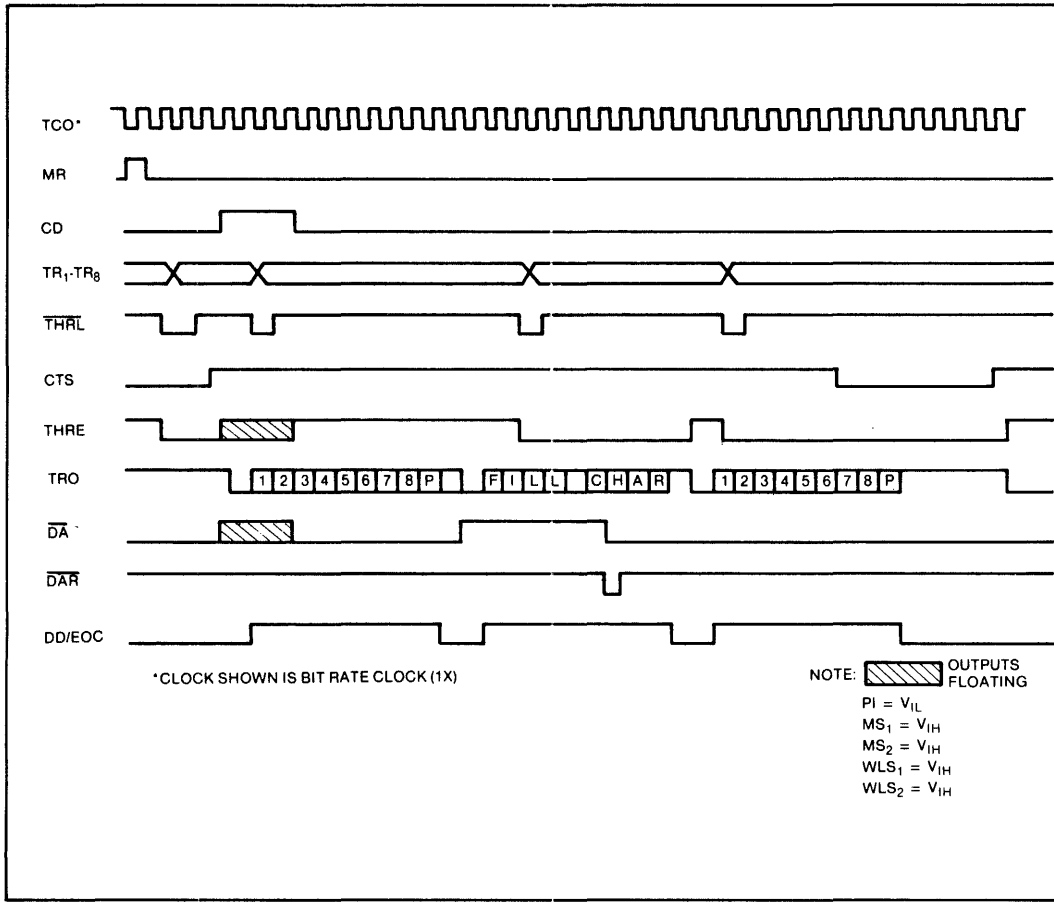
The Data Delimit/End of Character Flag is a low-level output voltage during start and stop bits and is a high-level output voltage during transmission of data and parity. The Data Not Available Flag ($\overline{DA}$) is set to a high-level output voltage at the end of the stop bit if a character has not been loaded into the Transmitter Holding Register at the center of the stop bit. The contents of the Fill-Character Holding Register will be transferred into the Transmitter Register and repeatedly transmitted until a character is loaded into the Transmitter Holding Register. At this time, the Fill-Character will be completed and the newly loaded isochronous character will follow contiguously.

Table 3 illustrates all the programmable isochronous character formats.

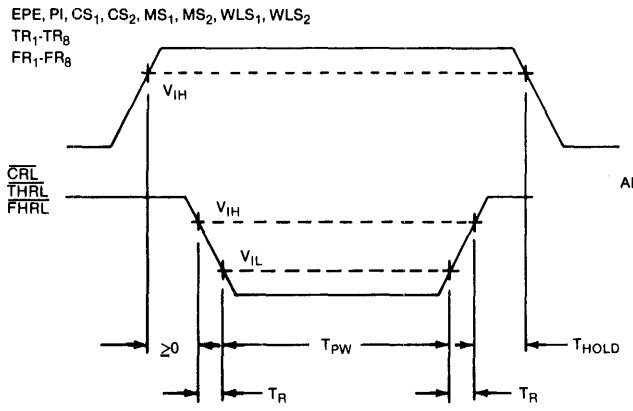
Table 3. ISOC MODE CONTROL DEFINITION

CONTROL WORD							CHARACTER FORMAT			
MSS2	MSS1	WLS2	WLS1	PI	PE		START BIT	DATA BITS	ADDED PARITY BIT	STOP ELEMENTS
1	1	0	0	0	0		1	5	ODD	1
1	1	0	0	0	1		1	5	EVEN	1
1	1	0	0	1	X		1	5	NONE	1
1	1	0	1	0	0		1	6	ODD	1
1	1	0	1	0	1		1	6	EVEN	1
1	1	0	1	1	X		1	6	NONE	1
1	1	1	0	0	0		1	7	ODD	1
1	1	1	0	0	1		1	7	EVEN	1
1	1	1	0	1	X		1	7	NONE	1
1	1	1	1	0	0		1	8	ODD	1
1	1	1	1	0	1		1	8	EVEN	1
1	1	1	1	1	X		1	8	NONE	1

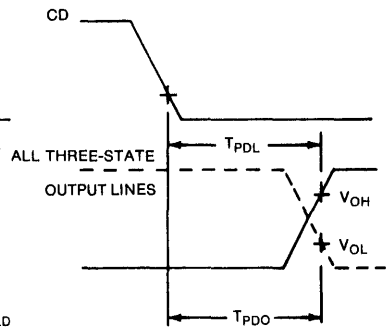
↑ Sets to ISOC Mode



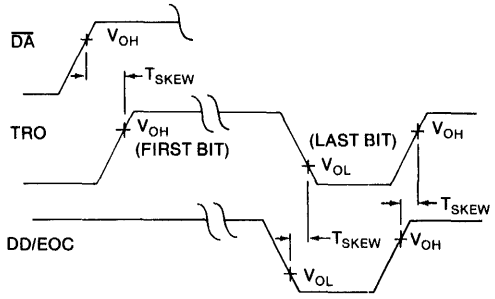
ISOCHRONOUS TIMING EXAMPLE



DATA INPUT LOAD CYCLE

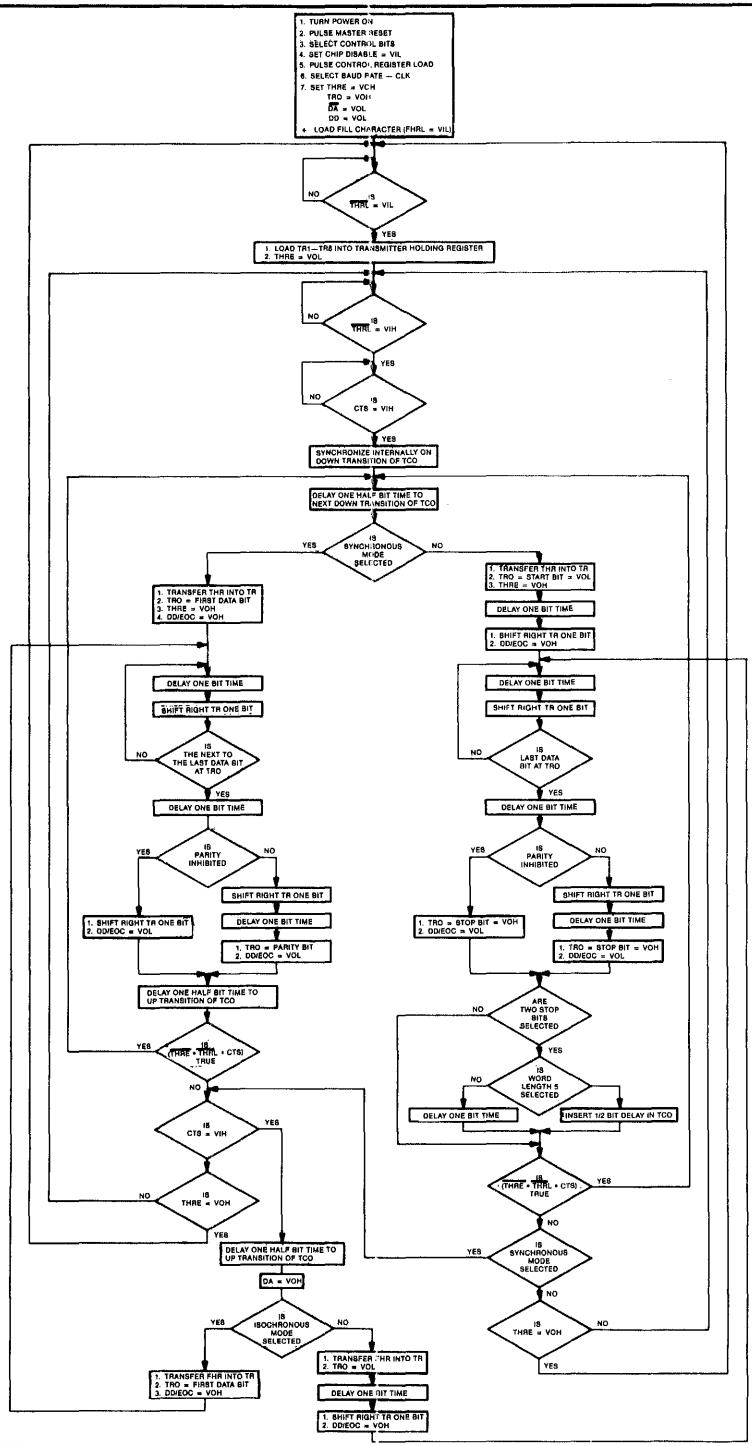


OUTPUT ENABLE DELAYS

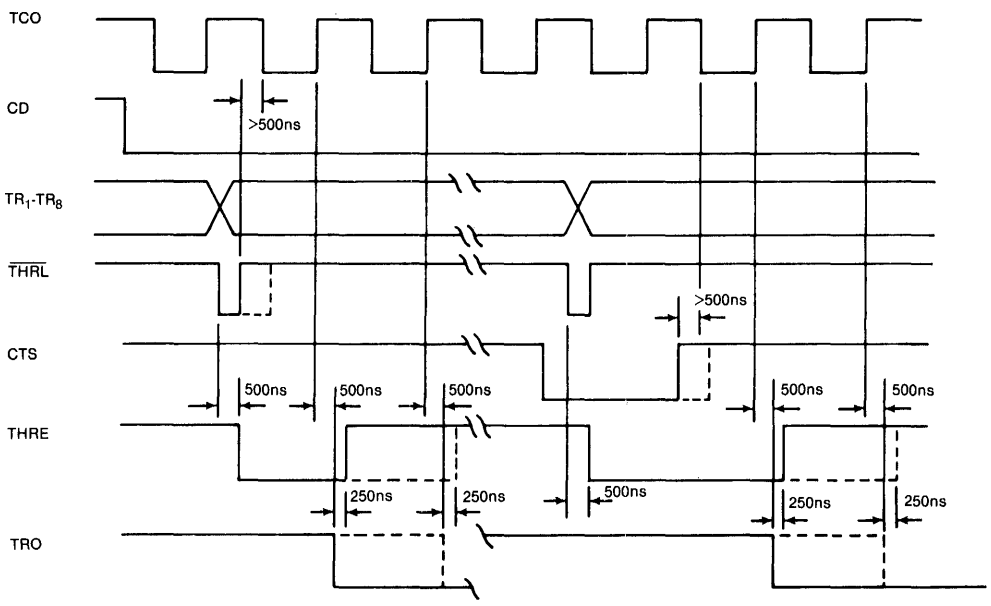


SKEW TIMES

SWITCHING WAVEFORMS



PT1482 SYNCHRONOUS ASYNCHRONOUS TRANSMITTER FLOW CHART



TIMING DETAIL

ABSOLUTE MAXIMUM RATINGS

V_{GG} Supply Voltage		+0.3V to −20V
V_{DD} Supply Voltage		+0.3V to −20V
Clock Input Voltage*		+0.3V to −20V
Logic Input Voltage*		+0.3V to −20V
Logic Output Voltage*		+0.3V to −20V
Storage Temperature	Ceramic	−65°C to +150°C
	Plastic	−55°C to +125°C
Operating Free-Air Temperature T_A Range		0°C to +50°C
Lead Temperature (Soldering, 10 sec.)		300°C

*$V_{GG} = V_{DD} = 0V$

NOTE: These voltages are measured with respect to V_{SS} (Substrate)

ELECTRICAL CHARACTERISTICS

($V_{SS} = V_{CC} = 5V \pm 5\%$, $V_{DD} = 0V$, $V_{GG} = -12V \pm 5\%$, $T_A = 0°C$ to $+50°C$ unless otherwise specified)

SYMBOL	PARAMETER	MIN.	MAX.	CONDITIONS
V_{IL} V_{IH}	**INPUT LOGIC LEVELS**[1] Low-level Input Voltage High-level Input Voltage	 V_{SS}-1.5V	0.8V	$V_{SS} = 4.75V$
V_{OL} V_{OH}	**OUTPUT LOGIC LEVELS**[2] Low-level Output Voltage High-level Output Voltage	 V_{SS}-1.0V	0.5V	$V_{SS} = 5.25V$ $I_{OL} = -1.6mA$ $V_{SS} = 4.75V$ $I_{OH} = -100\mu A$
I_{IL}	**INPUT CURRENT —** Low-level Input Current (each input)		−1.6mA	$V_{SS} = 5.25V$ $V_{IN} = 0.4V$
I_{LO}	Output Leakage Current[2]		10μA	

**Not more than one output should be shorted at a time.

NOTES: 1) Inputs under Chip Disable control when disabled (V_{IH} applied to CD), are logically disabled and appear as a single TTL load.

2) Outputs under Chip Disable control when disabled (V_{IH} applied to CD) are logically and electrically disconnected and caused to float.

3) All switching characteristics are measured at 0.8V and 2.0V.

SWITCHING CHARACTERISTICS

($V_{SS} = V_{CC} = 5V \pm 5\%$, $V_{DD} = 0V$, $V_{GG} = -12V \pm 5\%$, $T_A = 0°C$ to $+50°C$, $C_L = 20pf$)

SYMBOL	PARAMETER	MIN.	MAX.	CONDITIONS
F_C	Clock Frequency	DC DC	100 KHz 640 KHz	1482B-00 1482B-01
	PULSE WIDTH			
T_{HOLD}	Hold Time	20 nsec		
$T_{\overline{CRL}}$	Control Register Load	250 nsec		
$T_{\overline{THRL}}$	Transmitter Holding Register Load	250 nsec		
$T_{\overline{FHRL}}$	Fill-Character Holding RegisterLoad	250 nsec		
$T_{\overline{DAR}}$	Data Not Available Reset	200 nsec		
T_{MR}	Master Reset	500 nsec		
T_{PD}	Output Enable Delay		500 nsec	
T_{SKEW}	Skew Time		250 nsec	
T_R	Rise Time		150 nsec	
T_F	Fall Time		150 nsec	

See page 725 for ordering information.

UC1671 ASTRO

FEATURES

SYNCHRONOUS AND ASYNCHRONOUS
- Full Duplex Operations

SYNCHRONOUS MODE
- Selectable 5-8 Bit Characters
- Two Successive SYN Characters Sets Synchronization
- Programmable SYN and DLE Character Stripping
- Programmable SYN and DLE-SYN Fill

ASYNCHRONOUS MODE
- Selectable 5-8 Bit Characters
- Line Break Detection and Generation
- 1-, 1½-, or 2-Stop Bit Selection
- False Start Bit Detection Automatic Serial Echo Mode

SYSTEM COMPATIBILITY
- Double Buffering of Data
- 8-Bit Bi-Directional Bus For Data, Status, and Control Words
- All Inputs and Outputs TTL Compatible
- Up to 32 ASTROS Can Be Addressed On Bus
- On-Line Diagnostic Capability

TRANSMISSION ERROR DETECTION-PARITY
- Overrun and Framing

BAUD RATE — DC TO 1M BIT/SEC

8 SELECTABLE CLOCK RATES
- Accepts 1X Clock and Up to 4 Different 32X Baud Rate Clock Inputs
- Up to 47% Distortion Allowance with 32X Clock

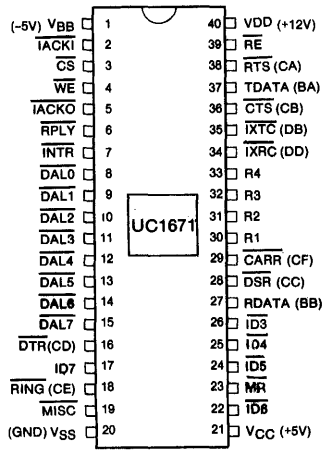
APPLICATIONS

SYNCHRONOUS COMMUNICATIONS
ASYNCHRONOUS COMMUNICATIONS
SERIAL/PARALLEL COMMUNICATIONS

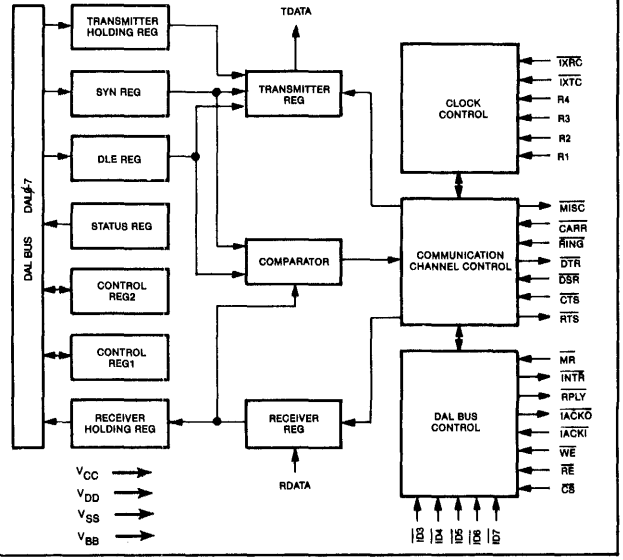
GENERAL DESCRIPTION

The UC1671 (ASTRO) is a MOS/LSI device which performs the functions of interfacing a serial data communication channel to a parallel digital system. The device is capable of full duplex communications (receiving and transmitting) with synchronous or asynchronous systems. The ASTRO is designed to operate on a multiplexed bus with other bus-oriented devices. Its operation is programmed by a processor or controller via the bus and all parallel data transfers with these machines are accomplished over the bus lines.

The ASTRO is fabricated in n-channel silicon gate MOS technology and is TTL compatible on all inputs and outputs.



PIN CONNECTIONS



UC1671 BLOCK DIAGRAM

PIN OUTS

The device is packaged in a 40-pin plastic or ceramic cavity package. The interface signals are defined below with all input/output signals complemented to facilitate bussing and interfacing with TTL. The Data Set controls and Status signals are also complemented to allow for an inversion when converting to EIA RS232C levels. The names and symbols assigned to the Data Set interface signals follows EIA standard nomenclature.

A bar over a signal ($\overline{\text{SIGNAL}}$), means active low (set = low).

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	POWER SUPPLIES	V_{BB}	– 5V
21		V_{CC}	+ 5V
40		V_{DD}	+ 12V
20		V_{SS}	Ground
23	MASTER RESET	$\overline{MR}$	The Control and Status Registers and other controls are cleared when this input is low.
8-15	DATA ACCESS LINES	$\overline{DAL0}$-$\overline{DAL7}$	Eight-bit bi-directional bus used for transfer of data, control, status, and address information.
17,22,24, 25,26	SELECT CODE	$\overline{ID7}$-$\overline{ID3}$	Five input pins which when hard-wired assign the device a unique identification code used to select the device when addressing and used as an identification when responding to interrupts.
3	CHIP SELECT	$\overline{CS}$	The low logic transition of CS identifies a valid address on the DAL bus during Read and Write operations.
39	READ ENABLE	$\overline{RE}$	This signal, when low, gates the contents of an addressed register from a selected ASTRO onto the DAL bus.
4	WRITE ENABLE	$\overline{WE}$	This signal, when low, gates the contents of the DAL bus into the addressed register of a selected ASTRO.
7	INTERRUPT	$\overline{INTR}$	This open drain output is made low when one of the communication interrupt conditions occur.
2	INTERRUPT ACKNOWLEDGE IN	$\overline{IACKI}$	This input becomes low when polling takes place on the bus by the Controller to determine the interrupting source. When this signal is received, the ASTRO places its ID code on the DAL if it is requesting interrupt, otherwise it makes IACKO a low.
5	INTERRUPT ACKNOWLEDGE OUT	$\overline{IACKO}$	This output is made a logic low in response to a low IACKI if the ASTRO receiving an IACKI input is not the interrupting device.
6	REPLY	$\overline{RPLY}$	This open drain output is made low when the ASTRO is responding to being selected by an address on the DAL during read or write operations or in affirming that it is the interrupting source during interrupt polling.
30-33	CLOCK RATES	R1-R4	These four inputs accept four different local 32X data rate Transmit and Receive clocks. The input on R4 may be divided down into a 32X clock from a 32X, 64X, 128X, or 256X clock input. The clock used in the ASTRO is selected by the Control Register.
37	TRANSMITTED DATA	TDATA (BA)	This output is the transmitted serial data from the ASTRO. This output is held in a Marking condition when the transmitter section is not enabled.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
27	RECEIVED DATA	RDATA (BB)	This input receives serial data into the ASTRO.
38	REQUEST TO SEND	$\overline{\text{RTS}}$ ($\overline{\text{CA}}$)	This output is enabled by the Control Register and remains in a low state during transmitted data from the ASTRO.
36	CLEAR TO SEND	$\overline{\text{CTS}}$ ($\overline{\text{CB}}$)	This input, when low, enables the transmitter section of the ASTRO.
28	DATA SET READY	$\overline{\text{DSR}}$ ($\overline{\text{CC}}$)	This input generates an interrupt when going On or Off while the Data Terminal Ready signal is On. It appears as a bit in the Status Register.
16	DATA TERMINAL READY	$\overline{\text{DTR}}$ ($\overline{\text{CD}}$)	This output is generated by a bit in the Control Register and indicates Controller readiness.
18	RING INDICATOR	$\overline{\text{RING}}$ ($\overline{\text{CE}}$)	This input from the Data Set generates an interrupt when made low with Data Terminal Ready in the "Off" condition.
29	CARRIER DETECTOR	$\overline{\text{CARR}}$ ($\overline{\text{CF}}$)	This input from the Data Set generates an interrupt when going On or Off if Data Terminal Ready is On. It appears as a bit in the Status Register.
35	TRANSMITTER TIMING	$\overline{\text{IXTC}}$ ($\overline{\text{DB}}$)	This input is the Transmitter 1X Data Rate Clock. Its use is selected by the Control Register. The transmitted data changes on the negative transition of this signal.
34	RECEIVER TIMING	$\overline{\text{IXRC}}$ ($\overline{\text{DD}}$)	This input is the Receiver 1X Data Rate Clock. Its use is selected by the Control Register. The Received Data is sampled by the ASTRO on the positive transition of this signal.
19	MISCELLANEOUS	$\overline{\text{MISC}}$	This output is controlled by a bit in the Control Register and is used as an extra programmable signal.

RECEIVER REGISTER — This 8-bit shift register inputs the received data at a clock rate determined by the Control Register. The incoming data is assembled to the selected character length and then transferred to the Receiver Holding Register with logic zeroes filling out any unused high-order bit positions.

RECEIVER HOLDING REGISTER — This 8-bit parallel buffer register presents assembled receiver characters to the DAL bus lines when requested through a Read operation.

COMPARATOR — The 8-bit comparator is used in the Synchronous mode to compare the assembled contents of the Receiver Register and the SYN register or DLE register. A match between the registers sets up stripping of the received character, when programmed, by preventing the data from being loaded into the Receiver Holding Register. A bit in the Status Register is set when stripping is performed. The comparator output also enables character synchronization of the Receiver on two successive matches with the SYN register.

SYN REGISTER — This 8-bit register is loaded from the DAL lines by a Write operation and holds the synchronization code used to establish receiver character synchronization. It serves as a fill character when no new data is available in the Transmitter Holding Register during transmission. This register cannot be read onto the DAL lines. It must be loaded with logic zeroes in all unused high-order bits.

DLE REGISTER — This 8-bit register is loaded from the DAL lines by a Write operation and holds the "DLE" character used in the Transparent mode of operation in which an idle transmit period is filled with the combination DLE-SYN pair of characters rather than a single SYN character. In addition the ASTRO may be programmed to force a single DLE character prior to any data character transmission while in the transmitter transparent mode.

TRANSMITTER HOLDING REGISTER — This 8-bit parallel buffer register holds parallel transmitted data transferred from the DAL lines by a Write operation. This data is transferred to the Transmitter Register when the transmitter section is enabled and the Transmitter Register is ready to send new data.

TRANSMITTER REGISTER — This 8-bit shift register is loaded from the Transmitter Holding Register, SYN register, or DLE register. The purpose of this register is to serialize data and present it to the transmitted Data output.

CONTROL REGISTERS — There are two 8-bit Control Registers which hold device programming signals such as mode selection, clock selection, interface signal control, and data format. Each of the Control Registers can be loaded from the DAL lines by a Write operation or read onto the DAL lines by a Read operation. The registers are cleared by a Master Reset.

STATUS REGISTER — This 8-bit register holds information on communication errors, interface data register status, match character conditions, and communication equipment status. This register may be read onto the DAL lines by a Read operation.

DATA ACCESS LINES — The DAL is an 8-bit bidirectional bus port over which all address, data, control, and status transfers occur. In addition to transferring data and control words the DAL lines also transfer information related to addressing of the device, reading and writing requests, and interrupting information.

ASTRO OPERATION

ASYNCHRONOUS MODE

Framing of asynchronous characters is provided by a Start bit (logic low) at the beginning of a character and a Stop bit (logic high) at the end of a character. Reception of a character is initiated on recognition of the first Start bit by a positive transition of the receiver clock, after a preceding Stop bit. The Start and Stop bits are stripped off while assembling the serial input into a parallel character.

The character assembly is completed by the reception of the Stop bit after reception of the last character or parity bit. If this bit is a logic high, the character is determined to have correct framing and the ASTRO is prepared to receive the next character. If the Stop bit is a logic low the Framing Error Status flag is set and the Receiver assumes this bit to be the Start bit of the next character. Character assembly continues from this point if the input is still a logic low when sampled at the theoretical center of the assumed Start bit. As long as the Receive input is spacing, all zero characters are assembled and error flags and data received interrupts are generated so that line breaks can be determined. After a character of all zeroes is assembled along with a zero in the Stop bit location, the first received logic high is determined as a Stop bit and this resets the Receiver circuit to a Ready state for assembly of the next character.

In the Asynchronous mode the character transmission occurs when information contained in the Transmitter Holding Register is transferred to the Transmitter Register. Transmission is initiated by the Insertion of a Start bit, followed by the serial output of the character least significant bit first with parity, if enabled, following the most significant bit; then the insertion of a 1-, 1.5-, or 2-bit length Stop condition. If the Transmitter Holding Register is full, the next character transmission starts after the transmission of the Stop bit of the present character in the Transmitter Register. Otherwise, the Mark (logic high) condition is continually transmitted until the Transmitter Holding Register is loaded.

In order to allow re-transmission of data received at a slightly faster character rate, means are provided for shortening the Stop bit length to allow transmission of characters to occur at the same rate as the reception of characters. The Stop bit is shortened by 1/16 of a bit period for 1-Stop bit selection and 3/16 of a bit period for 1.5-, or 2-Stop bit selection, if the next character is ready in the Transmitter Holding Register.

SYNCHRONOUS MODE

Framing of characters is carried out by a special Synchronization Character Code (SYN) transmitted at the beginning of a block of characters. The Receiver, when enabled, searches for two continuous characters matching the bit pattern contained in the SYN register. During the time the Receiver is searching, data is not transferred to the Receiver Holding Register, status bits are not updated, and the Receiver interrupt is not activated. After the detection of the first SYN character, the Receiver assembles subsequent bits into characters whose length is determined by contents of the Control Register. If, after the first SYN character detection, a second SYN character is present, the Receiver enters the Synchronization mode until the Receiver Enable Bit is turned off. If a second successive SYN character is not found, the Receiver reverts back to the Search mode.

In the Synchronous mode a continuous stream of characters are transmitted once the Transmitter is enabled. If the Transmitter Holding Register is not loaded at the time the Transmitter Register has completed transmission of a character, this idle time will be filled by a transmission of the character contained in the SYN register in the Nontransparent mode, or the characters contained in the DLE and SYN registers respectively while in the Transparent mode of operation.

DETAILED OPERATION

Receiver — The Receiver Data input is clocked into the Receiver Register by a 1X Receiver Clock from a modem Data Set, or by a local 32X bit rate clock selected from one of four externally supplied clock

inputs. When using the 1X clock, the Receiver Data is sampled on the positive transition of the clock in both the Asynchronous and Synchronous modes. When using a 32X clock in the Asynchronous mode, the Receive Sampling Clock is phased to the Mark-To-Space transition of the Received Data Start bit and defines, through clock counts, the center of each received Data bit within +0%, −3% at the positive transition 16 clock periods later.

In the Synchronous mode the Sampling Clock is phased to all Mark-To-Space transitions of the Received Data inputs when using a 32X clock. Each transition of the data causes an incremental correction of the Sampling Clock by 1/32nd of a bit period. The Sampling Clock can be immediately phased to every Mark-To-Space Data transition by setting Bit 4 of Control Register 1 to a logic high, while the Receiver is disabled.

When the complete character has been shifted into the Receiver Register it is then transferred to the Receiver Holding Register; the unused, higher number bits are filled with zeroes. At this time the Receiver Status bits (Framing Error/Sync Detect, Parity Error/DLE Detect, Overrun Error, and Data Received) are updated in the Status Register and the Data Received interrupt is activated. Parity Error is set, if encountered while the Receiver parity check is enabled in the Control Register. Overrun Error is set if the Data Received status bit is not cleared through a Read operation by an external device when a new character is ready to be transferred to the Receiver Holding Register. This error flag indicates that a character has been lost, as new data is lost and the old data and its status flags are saved.

The characters assembled in the Receiver Register that match the contents of the SYN or DLE register are not loaded into the Receiver Holding Register, and the DR interrupt is not generated, if Bit 3 of Control Register 2 (CR23 = SYN Strip) or Bit 4 of Control Register 1 (CR14 = DLE Strip) are set respectively, the SYN-DET and DLE-DET status bits are set with the next non SYN or DLE character. When both CR23 and CR14 are set (Transparent mode), the DLE-SYN combination is stripped. The SYN comparison occurs only with the character received after the DLE character. If two successive DLE characters are received only the first DLE character is stripped. No parity check is made while in this mode.

Transmitter — Information is transferred to the Transmitter Holding Register by a Write operation. Information can be loaded into this register at any time, even when the Transmitter is not enabled. Transmission of data is initiated only when the Request To Send bit is set to a logic one in the Control Register and the Clear To Send input is a logic low. Information is normally transferred from the Transmitter Holding Register to the Transmitter Register when the latter has completed transmission of a character. However, information in the DLE register may be transferred prior to the information contained in the Transmitter Holding Register if the Force DLE signal condition is enabled (Bit 5 = Force DLE and 6 = TX Transparent Control Register 1 set to a logic one). The control bit CR15 must be set prior to loading of a new character in the transmitter holding register to insure forcing the DLE character prior to transmission of the data character. The Transmitter Register output passes through a flip-flop which delays the output by one clock period. When using the 1X clock generated by the Modem Data Set, the output data changes state on the negative clock transition and the delay is one bit period. When using a local 32X clock the transmitter section selects one of the four selected rate inputs and divides the clock down to the baud rate. This clock is phased to the Transmitter Holding Register empty flag such that transmission of characters occurs within two data bit times of the loading of the Transmitter Holding Register when the Transmitter Register is empty.

When the Transmitter is enabled, a Transmitter interrupt is generated each time the Transmitter Holding Register is empty. If the Transmitter Holding Register is empty when the Transmitter Register is ready for a new character the Transmitter enters an idle state. During this idle time a logic high will be presented to the Transmitted Data output in the Asynchronous mode or the contents of the SYN register will be presented in the Synchronous Non-transparent mode (CR16 = 0). In the Synchronous Transmit Transparent mode (enabled by Bit 6 of Control Register 1 = Logic 1), the idle state will be filled by a DLE-SYN character transmission in that order. When entering the Transparent mode the DLE-SYN fill will not occur until the first forced DLE.

If the Transmitter section is disabled by a reset of the Request to Send, any partially transmitted character is completed before the transmitter section of the ASTRO is disabled. As soon as the CTS goes high the transmitted data output will go high.

When the Transmit parity is enabled, the selected Odd or Even parity bit is inserted into the last bit of the character in place of the last bit of the Transmitted Register. This limits transfer of character information to a maximum of seven bits plus parity or eight bits without parity. Parity cannot be enabled in the Synchronous Transparency mode.

DEVICE PROGRAMMING

The two 8-bit Control Registers of the ASTRO determine the operative conditions of the ASTRO chip. Control Register 1 is shown in the following table.

BIT 7 7	6	5	4	3	2	1	0
SYNC/ASYNC 0—LOOP MODE 1—NORMAL MODE	ASYNC 0—NON BREAK MODE 1—BREAK MODE SYNC 0—NON TRANSMITTER TRANSPARENT MODE 1—TRANSMIT TRANSPARENT MODE	ASYNC (TRANS. ENABLED) 0—1 1/2 or 2 STOP BIT SELECTION 1—SINGLE STOP BIT ASYNC (TRANS. DISABLED 0—$\overline{\text{MISC OUT}}$ RESET 1—$\overline{\text{MISC OUT}}$ SET SYNC (CR16 = 0) 0—NO PARITY GENERATED 1—TRANSMIT PARITY ENABLED SYNC (CR16 = 1) 0—NO FORCE DLE 1—FORCE DLE	ASYNC 0—NON ECHO MODE 1—AUTO ECHO MODE SYNC (CR12 = 1) 0—DLE STRIPPING NOT ENABLED 1—DLE STRIPPING ENABLED SYNC (CR12 = 0) 0—$\overline{\text{MISC}}$ RESET 1—$\overline{\text{MISC}}$ SET	ASYNC 0—NO PARITY ENABLED 1—PARITY CHECK ENABLED ON RECEIVER PARITY GENERATION ENABLED ON TRANSMITTER SYNC 0—RECEIVER PARITY CHECK IS DISABLED 1—RECEIVER PARITY CHECK IS ENABLED	SYNC/ASYNC 0—RECEIVER DISABLED 1—RECEIVER ENABLED	SYNC/ASYNC 0—$\overline{\text{RTS}}$ RESET 1—$\overline{\text{RTS}}$ SET	SYNC/ASYNC 0—$\overline{\text{DTR}}$ RESET 1—$\overline{\text{DTR}}$ SET

CONTROL REGISTER 1

Control Register 1

Bit 7 — A logic 0 configures the ASTRO into an Internal Data and Control Loop mode and disables the Ring interrupt. In this diagnostic mode the following loops are connected internally:

a. The Transmit Data is connected to the Receive Data with the TD pin held in a Mark condition and the input to the RD pin disregarded.

b. With a 1X clock selected, the Transmitter Clock also becomes the Receive Clock.

c. The $\overline{\text{Data Terminal Ready}}$ ($\overline{\text{DTR}}$) is connected to the $\overline{\text{Data Set Ready}}$ ($\overline{\text{DSR}}$) input, with the $\overline{\text{DTR}}$ output in held in an Off condition (logic high), and the $\overline{\text{DSR}}$ input pin is disregarded.

d. The Request to Send Control bit is connected to the $\overline{\text{Clear To Send}}$ ($\overline{\text{CTS}}$) and Carrier Detector inputs, with the $\overline{\text{RTS}}$ output pin held in an Off condition (logic high), and the $\overline{\text{CTS}}$ and $\overline{\text{Carrier Detector}}$ input pins are disregarded.

3. The $\overline{\text{Miscellaneous}}$ pin is held in an Off (logic high) condition.

A logic 1 on Bit 7 enables the Ring interrupt and returns the ASTRO to the normal full duplex configuration.

Bit 6 — In the *Asynchronous* mode a logic 1 holds the Transmitted Data output in a Spacing (Logic 0) condition, starting at the end of any current transmitted character, when the Transmitter is enabled. Normal Transmitter timing continues so that this Break condition can be timed out after the loading of new characters into the Transmitter Holding Register.

In the *Synchronous* mode a logic 1 sets the Transmitter in a transparent transmission which implies that idle transmitter time will be filled by DLE-SYN character transmission and a DLE can be forced ahead of any character in the Transmitter Holding Register when CR15 is a logic one in the sync mode.

Bit 5 — In the *Asynchronous* mode a logic 1, with the Transmitter enabled, causes a single Stop bit to be transmitted. A logic 0 causes 2-Stop bit transmission for character lengths of 6, 7, or 8 bits and one-and-a-half Stop bits for a character length of 5 bits.

With the Transmitter disabled this bit controls the Miscellaneous output on Pin 19, which may be used for Make Busy on 103 Data Sets, Secondary Transmit on 202 Data Sets, or dialing on CBS Data Couplers.

In the *Synchronous* mode a logic 1 combined with a logic 0 on Bit 6 of control Register 1 enables Transmit parity; if CR15 = 0 or CR15 = 1 no parity is generated. When set to a logic 1 with Bit 6 also a logic 1, the contents of the DLE register are transmitted prior to the next character loaded in the Transmitter Holding Register as part of the Transmit Transparent mode.

Bit 4 — In the *Asynchronous* mode a logic 1 enables the Automatic Echo mode when the receiver section is enabled. In this mode the clocked regenerated data is presented to the Transmit Data output in place of normal transmission through the Transmitter Register. This serial method of echoing does not present any abnormal restrictions on the transmit speed of the terminal. Only the first character of a Break condition of all zeroes (null character) is echoed when a Line Break condition is detected. For all subsequent null characters, with logic zero Stop bits, a steady Marking condition is transmitted until normal character reception resumes. Echoing does not start until a character has been received and the Transmitter is idle. The Transmitter does not have to be enabled during the Echo mode.

In the *Synchronous* mode a logic 1, with the Receiver enabled, does not allow assembled Receiver data matching the DLE register contents to be transferred to the Receiver Holding Register; also, parity checking is disabled.

When the Receiver is not enabled this bit controls the Miscellaneous output on Pin 19, which may be used for New Sync on a 201 Data Set. When operating with a 32X clock and a disabled Receiver a logic 1 on this bit also causes the Receiver timing to synchronize on Mark-To-Space transitions.

Bit 3 — In the *Asynchronous* mode a logic 1 enables check of parity on received characters and generation of parity for transmitted characters.

In the *Synchronous* mode a logic 1 bit enables check of parity on received characters only. **Note:** Transmitter parity enable is controlled by CR15.

Bit 2 — A logic 1 enables the ASTRO to receive data into the Receiver Holding Register, update Receiver Status Bits 1, 2, 3, and 4, and to generate Data Received interrupts. A logic 0 disables the Receiver and clears the Receiver Status bits.

Bit 1 — Controls the Request To Send output on Pin 38 to control the CA circuit of the Data Set. The RTS output is inverted from the state of CR11. A logic 1 combined with a low logic Clear To Send input enables the Transmitter and allows THRE interrupts to be generated. A logic 0 disables the Transmitter and turns off the external Request To Send signal. Any character in the Transmitter Register will be completely transmitted before the Transmitter is turned off. The Request To Send output may be used for other functions such as "Make Busy" on 103 Data Sets.

Bit 0 — Controls the Data Terminal Ready output on Pin 16 to control the CD circuit of the Data Set. A logic 1 enables the Carrier and Data Set Ready interrupts. A logic 0 enables only the telephone line Ring interrupt. The DTR output is inverted from the state of CR10.

Control Register 2

Control Register 2, unlike Control Register 1, cannot be changed at any time. This register should be changed only while both the receiver and transmitter sections of the ASTRO are in the idle state.

Bits 7-6 — These bits select the character length as follows:

Bits 7-6	Character Length
00	8 bits
01	7 bits
10	6 bits
11	5 bits

When parity is enabled it must be considered as a bit when making character length selection, i.e. 5 character bits plus parity = 6 bits.

Bit 5 — A logic 1 selects the Synchronous Character mode. A logic 0 selects the Asynchronous Character mode.

Bit 4 — A logic 1 selects odd parity and a logic 0 selects even parity, when parity is enabled by CR13 and/or CR15.

Bit 3 — In the *Asynchronous* mode a logic 0 selects the rate 1(-32X) clock input (pin 30) as the Receiver Clock rate and a logic 1 selects the same clock rate for the Receiver as selected by Bits 2-0 for the Transmitter. This bit must be a logic 1 for the 1X clock selection by Bits 2-0.

In the *Synchronous* mode a logic 1 causes all DLE-SYN combination characters in the Transparent mode when DLE strip CR14 is a logic 1, or all SYN characters in the Non-transparent mode to be stripped and no Data Received interrupt to be generated. The SYN Detect status bit is set with reception of the next assembled character as it is transferred to the Receiver Holding Register.

Bits 2-0 — These bits select the Transmit and Receive clocks. The Input Clock to the Rate 4 pin may be divided down to form the 32X clock from a multiple clock as shown:

Bits 2-0	Clock
000	1X clock for Transmit and Receive (Pins 35 and 34 respectively)
001	32X clock — Rate 1 input (Pin 30)
010	32X clock — Rate 2 input (Pin 31)
011	32X clock — Rate 3 input (Pin 32)
100	32X clock — Rate 4 input ÷ 1 (Pin 33)
101	32X clock — Rate 4 input ÷ 2 (Pin 33)
110	32X clock — Rate 4 input ÷ 4 (Pin 33)
111	32X clock — Rate 4 input ÷ 8 (Pin 33)

BIT 7 6	5	4	3	2 1 0
SYNC/ASYNC CHARACTER LENGTH SELECT 00 = 8 BITS 01 = 7 BITS 10 = 6 BITS 11 = 5 BITS	MODE SELECT 0—ASYNCHRONOUS MODE 1—SYNCHRONOUS MODE	SYNC/ASYNC 1—ODD PARITY SELECT 0—EVEN PARITY SELECT	ASYNC 1—RECEIVER CLOCK DETERMINED BY BITS 2-0 0—RECEIVER CLK = RATE 1 SYNC (CR14 = 0) 0—NO SYN STRIP 1—SYN STRIP SYNC (CR14 = 1) 0—NO DLE-SYN STRIP 1—DLE-SYN STRIP	SYNC/ASYNC CLOCK SELECT 000 - IX CLOCK 001 - RATE 1 CLOCK 010 - RATE 2 CLOCK 011 - RATE 3 CLOCK 100 - RATE 4 CLOCK 101 - RATE 4 CLOCK ÷ 2 110 - RATE 4 CLOCK ÷ 4 111 - RATE 4 CLOCK ÷ 8

CONTROL REGISTER 2

Status Register

The data contained in the Status Register define Receiver and Transmitter data conditions and status of the Data Set. The Status word is shown and defined below.

Bit 7 — This bit is set to a logic 1 whenever there is a change in state of the Data Set Ready or Carrier Detector inputs while Data Terminal Ready (Bit 0 of Control Register 1) is a logic 1 or the Ring Indicator is turned on, with DTR a logic 0. This bit is cleared when the Status Register is read onto the Data Access Lines.

Bit 6 — This bit is the logic complement of the Data Set Ready input on Pin 28. With 202-type Data Sets it can be used for Secondary Receive.

Bit 5 — This bit is the logic complement of the Carrier Detector input on Pin 29.

Bit 4 — In the *Asynchronous* mode a logic 1 indicates that received data contained a log 0 bit after the last data bit of the character in the stop bit slot, while the Receiver was enabled. This indicates a Framing error. This bit is set to a logic 0 if the proper logic 1 condition for the Stop bit was detected.

In the *Synchronous* mode a logic 1 indicates that the contents of the Receiver Register matched the contents of the SYN Register. The condition of this bit remains for a full character assembly time. If SYN strip (CR23) is enabled this status bit is updated with the character received after the SYN character. In both modes the bit is cleared when the Receiver is disabled.

Bit 3 — When the DLE Strip is enabled (Bit 4 of Control Register 1) the Receiver parity check is disabled and this bit is set to a logic 1 if the *previous character* to the presently assembled character matched the contents of the DLE register; otherwise it is cleared. The DLE DET remains for one character time and is reset on the next character transfer or on a Status Register Read. If DLE Strip is not enabled, this bit is set to a logic 1 when the Receiver is enabled, Receiver parity (Bit 3 of Control Register 1) is also enabled, and the last received character has a Parity error. A logic 0 on this bit indicates correct parity. This bit is cleared in either of the above modes when the Receiver is disabled.

Bit 2 — A logic 1 indicates an Overrun error which occurs if the previous character in the Receiver Holding Register has not been read and Data Received is not reset, at the time a new character is to be transferred to the Receiver Holding Register. This bit is cleared when no Overrun condition is detected, i.e., the next character transfer time or when the Receiver is disabled.

Bit 1 — A logic 1 indicates that the Receiver Holding Register is loaded from the Receiver Register, if the Receiver is enabled. It is cleared to a logic 0 when the Receiver Holding Register is read onto the Data Access Lines, or the Receiver is disabled.

Bit 0 — A logic 1 indicates that the Transmitter Holding Register does not contain a character while the Transmitter is enabled. It is set to a logic 1 when the contents of the Transmitter Holding Register is transferred to the Transmitter Register. It is cleared to a 0 bit when the Transmitter Holding Register is loaded from the DAL, or when the Transmitter is disabled.

INPUT/OUTPUT OPERATIONS

All Data, Control, and Status words are transferred over the Data Access Lines (DAL 0-7). Additional input lines provide controls for addressing a particular unit, and regulating all input and output operations. Other lines provide interrupt capability to indicate to a Controller than an input operation is requested by the ASTRO. All input/output terminology below is referenced to the Controller so that a Read or Input takes data from the ASTRO and places it on the DAL lines, while a Write or Output places data from the DAL lines into the ASTRO.

Read

A Read Operation is initiated by the placement of an *eight-bit address* on the DAL by the Controller. When the Chip Select signal goes to a logic low state, the ASTRO compares Bits 7-3 of the DAL with its hardwired ID code (Pins 17, 22, 24, 25, and 26) and becomes selected on a Match condition. The ASTRO then sets its REPLY line low to acknowledge its readiness to transfer data. Bits 2-0 of the address are used to select ASTRO registers to read from as follows:

Bits 2-0	Selected Register
000	Control Register 1
010	Control Register 2
100	Status Register
110	Receiver Holding Register

BIT 7	6	5	4	3	2	1	0
• DATA SET CHANGE	• DATA SET READY	• CARRIER DETECTOR	• FRAMING ERROR • SYN DETECT	• DLE DETECT • PARITY ERROR	• OVERRUN ERROR	• DATA RECEIVED	• TRANSMITTER HOLDING REGISTER EMPTY

STATUS REGISTER

When the Read Enable ($\overline{RE}$) line is set to a logic low condition by the Controller the ASTRO gates the contents of the addressed register onto the DAL. The Read operation terminates, and the devices becomes unselected, when both the Chip Select and Read Enable return to a logic high condition. Reading of the Receiver Holding Register clears the DR Status bit. Bit 0 DAL0 must be a logic high in read or write operations.

Write

A Write operation is initiated by the placement of an eight-bit address or the DAL by the Controller. The ASTRO compares Bits 7-3 of the DAL with its ID code when the Chip Select input goes to a logic low state. If a Match condition exists, the device is selected and makes it $\overline{RPLY}$ line low to acknowledge its readiness to transfer data. Bits 2-0 of the address are used to select ASTRO registers to be written into as follows:

Bits 2-0	Selected Register
000	Control Register 1
010	Control Register 2
100	SYN and DLE Register
110	Transmitter Holding Register

When the Write Enable ($\overline{WE}$) line is set to a logic low condition by the copntroller the ASTRO gates the data from the DAL into the addressed register. If data is written into the Transmitter Holding Register, the THRE Status bit is cleared to a logic zero.

The 100 address loads both the SYN and DLE registers. After writing into the SYN register the device is conditioned to write into the DLE if followed by another Write pulse with the 100 address. Any intervening Read or Write operation with other addresses resets this condition such that the next 100 will address the SYN register.

Interrupts

The following conditions generate interrupts:

1. **Data Received (DR) —** Indicates transfer of a new character to the Receiver Holding Register while the Receiver is enabled.
2. **Transmitter Holding Register Empty (THRE) —** Indicates that the THR register is empty while the Transmitter is enabled. The first interrupt occurs when the Transmitter becomes enabled if there is an empty THR, or after the character is transferred to the Transmitter Register making the THR empty.
3. **Carrier On —** Indicates Carrier Detector input goes low when DTR is on.
4. **Carrier Off —** Indicates $\overline{\text{Carrier Detector}}$ input goes high when DTR is on.
5. **DSR On —** Indicates the $\overline{\text{Data Set Ready}}$ input goes low when DTR is on.
6. **DSR Off —** Indicates the $\overline{\text{Data Set Ready}}$ input goes high when DTR is on.
7. **Ring On —** Indicates the $\overline{\text{Ring Indicator}}$ input goes low when DTR is off.

Each time an Interrupt condition exists the $\overline{INTR}$ output from the ASTRO is made a logic low. The following interrupt procedure is then carried out even if the interrupt condition is removed.

The Controller acknowledges the Interrupt request by setting the Chip Select ($\overline{CS}$) and the Interrupt Acknowledge Input ($\overline{IACKI}$) to the ASTRO to a Low state. On this transition all non-interrupting devices receiving the $\overline{IACKI}$ set their Interrupt Acknowledge Output ($\overline{IACKO}$) low, enabling lower priority daisy-chained devices to respond to the Interrupt request. The highest priority device that is interrupting will then set its $\overline{RPLY}$ low. This device places its ID code on Bit Positions 7-3 of the DAL when a low $\overline{RE}$ signal is received. In addition Bit 2 is set to a logic one if any of the interrupt numbers 1 and 3-7 above occurred, and remains a logic zero if the THRE has caused the interrupt (see note).

To reset the Interrupt condition ($\overline{INTR}$) Chip Select ($\overline{CS}$) and ($\overline{IACKI}$) must be received by the ASTRO. A setup time must exist between $\overline{CS}$ and the $\overline{RE}$ or $\overline{WE}$ signals to allow chip selection prior to read/write operations and deselection control through the latter signals. The data is removed from the DAL when the $\overline{RE}$ signal returns to the logic high state.

MAXIMUM RATINGS

V_{DD} With Respect to V_{SS} (Ground)		+20 to −0.3V
Max Voltage To Any Input With Respect to V_{SS}		+20 to −0.3V
Operating Temperature		0°C to 70°C
Storage Temperature	Plastic	−55°C to +125°C
	Ceramic	−65°C to +150°C
Power Dissipation		1000 mW

OPERATING CHARACTERISTICS

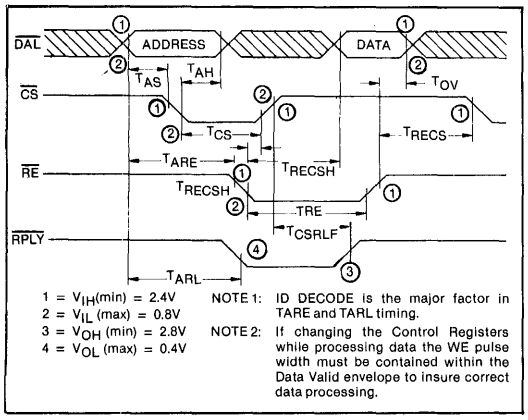
T_A = 0°C to 70°C, V_{DD} = +12.0V ±5%, V_{BB} = −5.0V ±5%, V_{SS} = 0V, V_{CC} = +5V ±5%

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	µA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	µA	$V_{OUT} = V_{DD}$
I_{BB}	V_{BB} Supply Current			1	mA	V_{BB} = −5V
I_{CCAVE}	V_{CC} Supply Current			80	mA	
I_{DDAVE}	V_{DD} Supply Current			10	mA	
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage (All Inputs)			.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = −100 µA
V_{OL}	Output Low Voltage			.4	V	I_O = 1.6 mA

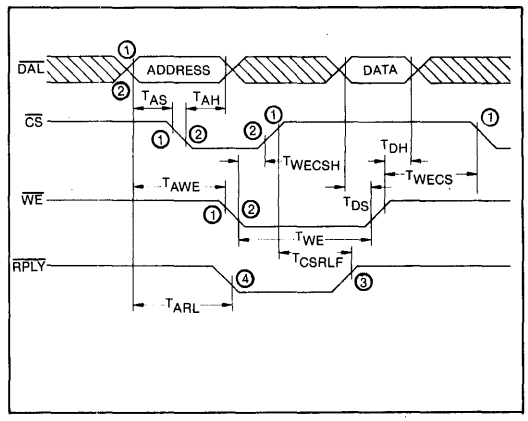
AC CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12.0V ±5%, V_{BB} = −5.0V ±5%, V_{CC} = +5.0 ±5%, V_{SS} = 0V
CL_{MAX} = 20 pf

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{AS}	Address Set-Up Time	0			ns	
t_{ah}	Address Hold Time	150			ns	
T_{ARL}	Address to $\overline{RPLY}$ Delay			400	ns	
T_{CS}	$\overline{CS}$ Width	250			ns	
T_{CSRLF}	$\overline{CS}$ to Reply OFF Delay	0		250	ns	R_L = 2.7 KΩ
READ						
T_{ARE}	Address and $\overline{RE}$ Spacing	250			ns	
T_{RECSH}	$\overline{RE}$ and $\overline{CS}$ Overlap	20			ns	
T_{RECS}	$\overline{RE}$ to $\overline{CS}$ Spacing	250			ns	
T_{RED}	$\overline{RE}$ to Data Out Delay			180	ns	C_L = 20 pf
T_{RE}	$\overline{RE}$ Width	200		1000	ns	
WRITE						
T_{AWE}	Address to $\overline{WE}$ Spacing	250			ns	
T_{WECSH}	$\overline{WE}$ and $\overline{CS}$ Overlap	20			ns	
T_{WE}	$\overline{WE}$ Width	200		1000	ns	
T_{DS}	Data Set-Up Time	150			ns	
T_{DH}	Data Hold Time	100			ns	
TWECS	$\overline{WE}$ to $\overline{CS}$ Spacing	250			ns	



READ CYCLE TIMING DIAGRAM

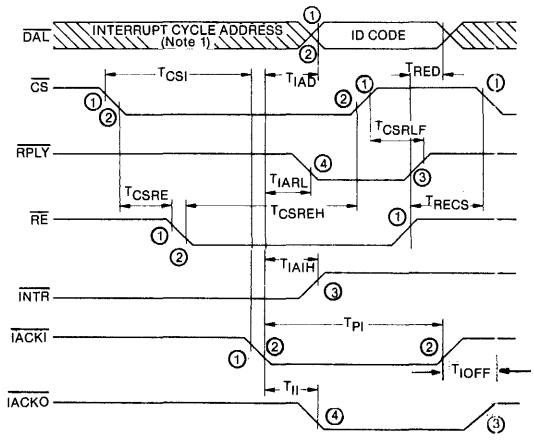


WRITE CYCLE TIMING DIAGRAM

INTERRUPT

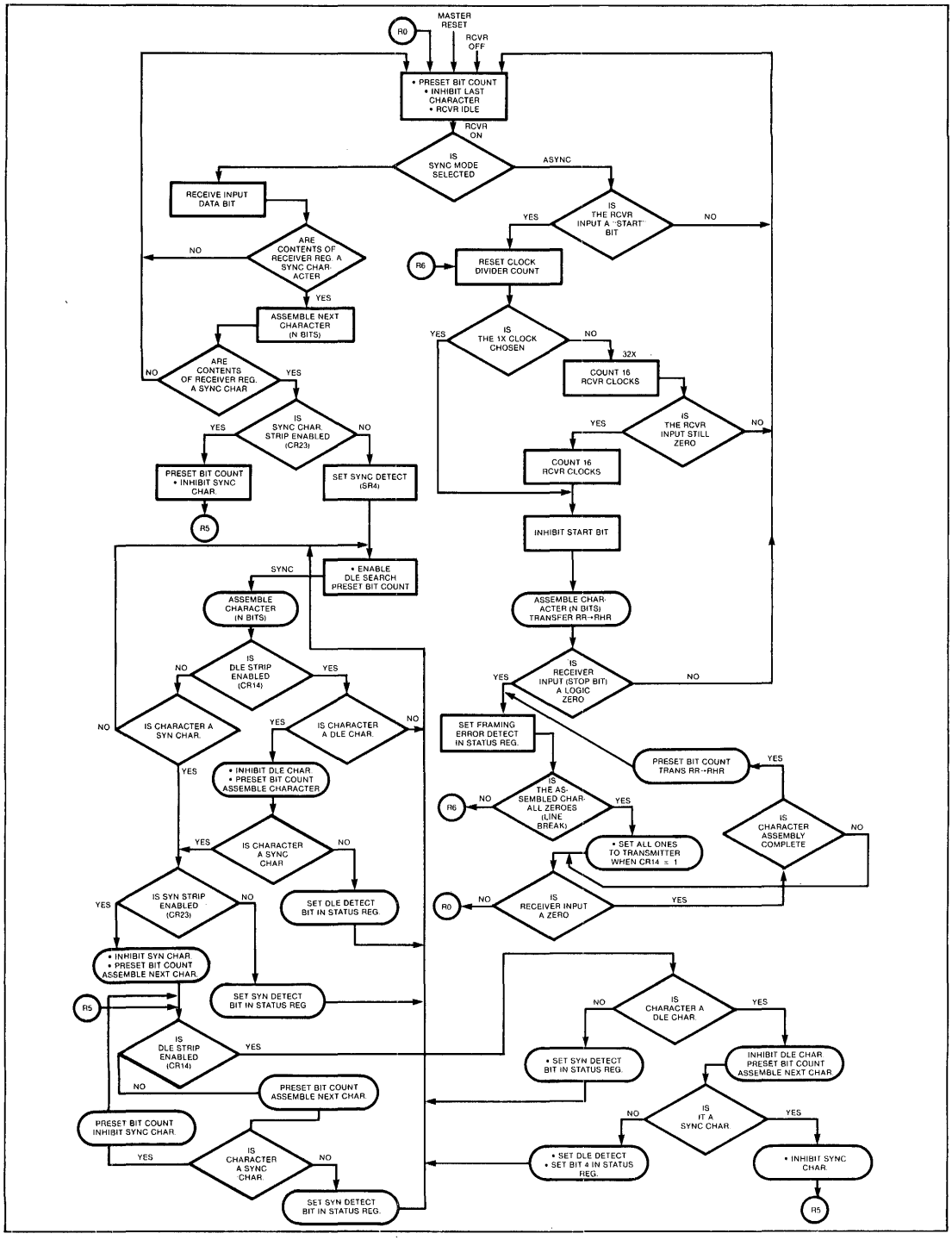
	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{CSI}	$\overline{CS}$ to $\overline{IACKI}$ Delay	0			ns	
T_{CSRE}	$\overline{CS}$ to $\overline{RE}$ Delay	250			ns	
T_{CSREH}	$\overline{CS}$ and $\overline{RE}$ Overlap	20			ns	
T_{RECS}	$\overline{RE}$ to $\overline{CS}$ Spacing	250			ns	
T_{PI}	$\overline{IACKI}$ Pulse Width	200			ns	
T_{IAD}	$\overline{IACKI}$ to Valid ID Code Delay			250	ns	See Note 1.
T_{RED}	$\overline{RE}$ OFF to $\overline{DAL}$ Open Delay			180	ns	
T_{IARL}	$\overline{IACKI}$ to $\overline{RPLY}$ Delay			250	ns	
T_{CSRLF}	$\overline{CS}$ to $\overline{RPLY}$ OFF Delay	0		250	ns	R_L = 2.7 KΩ
T_{IAIH}	$\overline{IACKI}$ ON to $\overline{INTR}$ OFF Delay			300	ns	
T_{II}	$\overline{IACKI}$ to $\overline{IACKO}$ Delay			200	ns	
T_{IOFF}	$\overline{IACKO}$ OFF Delay From $\overline{CS}$ OFF, $\overline{RE}$ OFF, or $\overline{IACKI}$ HIGH.			250	ns	See Note 2.

Note 1: If $\overline{RE}$ goes low after $\overline{IACKI}$ goes low, the delay will be from the falling edge of $\overline{RE}$.
Note 2: $\overline{IACKO}$ goes false after the last one of the following three signals go false: $\overline{CS}$, $\overline{RE}$ and $\overline{IACKI}$. T_{IOFF} is measured from the last signal going false.

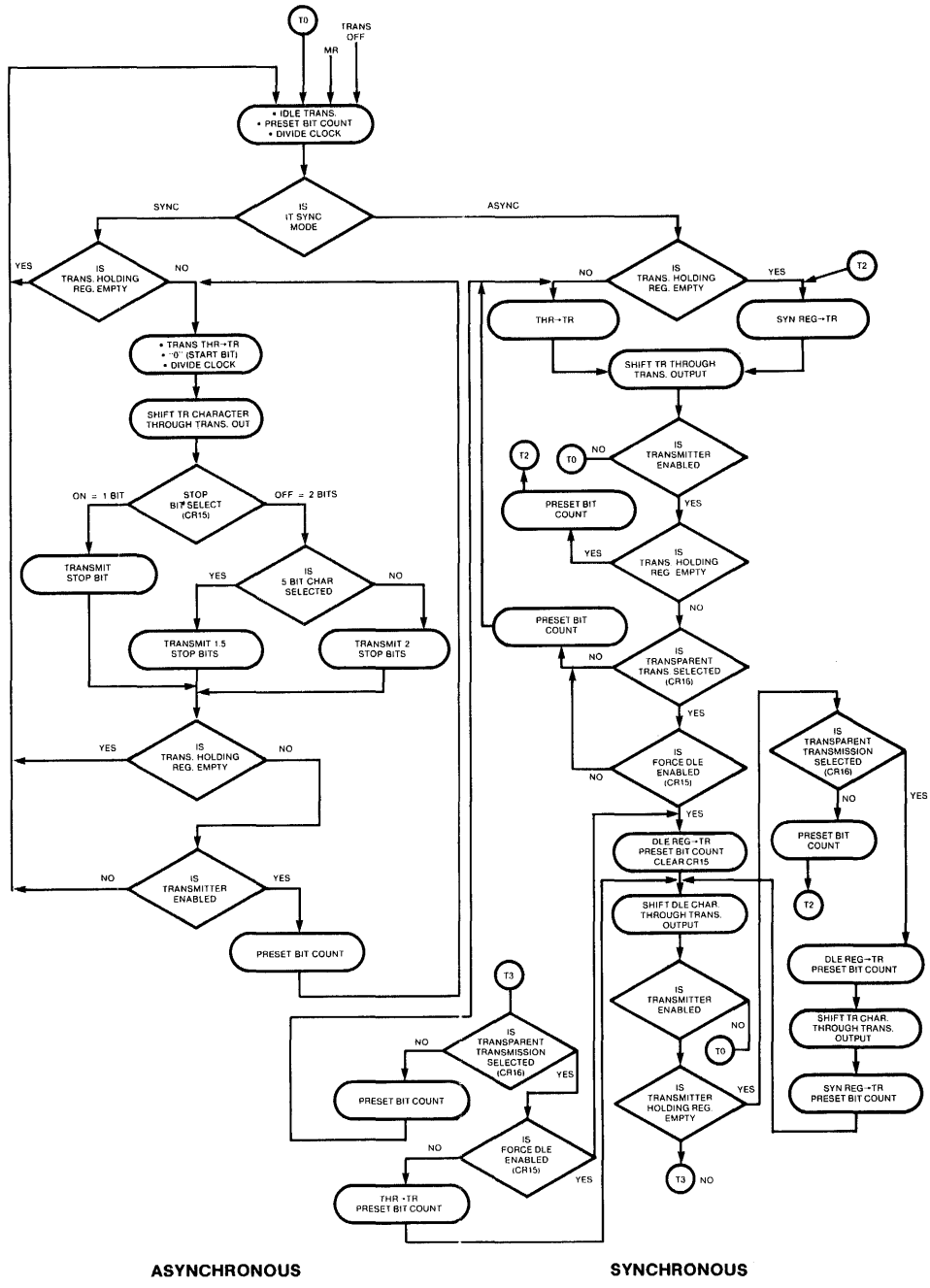


Note 1: $\overline{DAL0}$ must be a logic low during $\overline{CS}$ to form an Interrupt Cycle Address during Daisy Chain Interrupt Response.

INTERRUPT CYCLE TIMING DIAGRAM



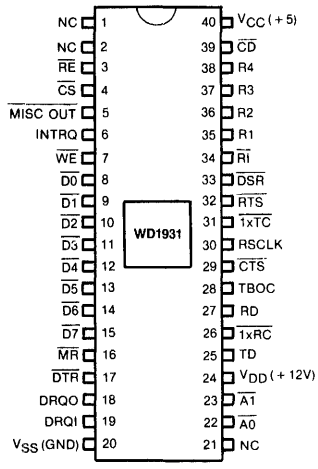
RECEIVER SECTION

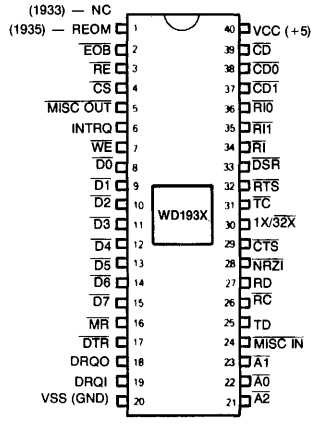


See page 725 for ordering information.

TRANSMITTER SECTION

WD1931 & WD193X Family Data Sheets





FEATURES

Asynchronous Operation
Character Synchronous Operation
Programmable Syn and DLE Character
8 Selectable Clock Rates

HLDC, SDLC, ADCCP, X.25 } Compatible
SDLC Loop Mode
NRZI and Digital Phase Lock Loop

ORDERING INFORMATION

Table 5. WD193X ORDERING INFORMATION

Part No.	Loop Mode	Maximum Data Rate	Temp. Range
WD193X *-00	no	500KBPS	0°C to +70°C
WD193X *-10	yes	500KBPS	0°C to +70°C
WD193X *-01	no	1.0MBPS	0°C to +70°C
WD193X *-11	yes	1.0MBPS	0°C to +70°C
WD193X *-02	no	1.5MBPS	0°C to +70°C
WD193X *-12	yes	1.5MBPS	0°C to +70°C
WD193X *-03	no	2.0MBPS	0°C to +70°C

* Please contact your local Western Digital Sales Representative for package availability and price information.

See page 725 for ordering information.

Printed in U.S.A.

WD1931 Asynchronous/Synchronous Receiver/Transmitter

FEATURES

SYNCHRONOUS AND ASYNCHRONOUS
- Full Duplex Operations
- Selectable Character Length (5, 6, 7 or 8 Bits)

SYNCHRONOUS MODE
- Two Successive SYN Characters Sets Synchronization
- Programmable SYN and DLE Character Detection and Stripping
- Programmable SYN and DLE-SYN Fill
- Transparent BI-SYNC Operation
- DDCMP Compatible

ASYNCHRONOUS MODE
- Line Break Detection and Generation
- 1-, 1½-, or 2-Stop Bit Selection
- False Start Bit Detection
- Automatic Serial Echo Mode
- Overrun and Framing Error Detection

SYSTEM COMPATIBILITY
- Double Buffering of Data
- 8-Bit Bi-Directional Bus for Data, Status, and Control Words
- All Inputs and Outputs TTL Compatible
- Chip Select, RE, WE, A0, A1 Interface to CPU
- On-Line Diagnostic Capability
- Data Set, Carrier Detect, and Ring Interrupts

BAUD RATE — DC TO 1M BIT/SEC

8 SELECTABLE CLOCK RATES
- Accepts 1X Clock and Up to Four Different 32X Baud Rate Clock Inputs
- Up to 47% Distortion Allowance with 32X Clock

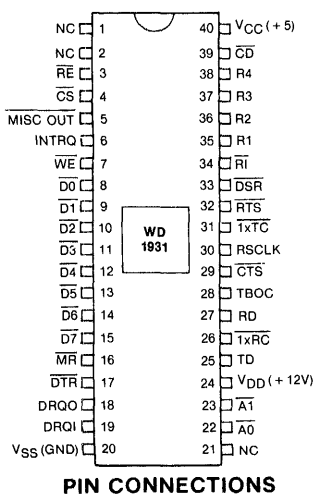
PINOUT COMPATIBLE TO WD193X FOR MULTIPROTOCOL BOARD APPLICATIONS

APPLICATIONS

SYNCHRONOUS COMMUNICATIONS
ASYNCHRONOUS COMMUNICATIONS
SERIAL/PARALLEL COMMUNICATIONS

GENERAL DESCRIPTIONS

The WD1931 is a MOS/LSI device which performs the functions of interfacing a serial data communications channel to a parallel digital system. This device is capable of full duplex communications with asynchronous and/or synchronous systems. Western Digital has made device pin assignments for the WD1931 to make it compatible with the WD193X (Synchronous Data Link Controller). This pin out allows the user to implement a one-board multi-protocol design. For character-oriented asynchronous and/or synchronous (bi-sync) protocols, the WD1931 is used, and for bit-oriented SDLC, HDLC and ADCCP protocols the WD193X is used (see WD193X data sheets and WD1931/WD193X compatibility application notes).



PIN CONNECTIONS

Figure 1. WD1931 PIN CONNECTIONS

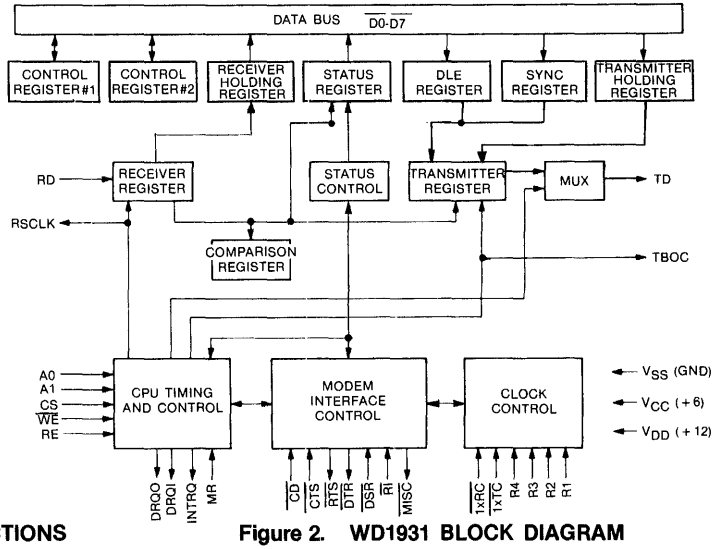


Figure 2. WD1931 BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

The WD1931 is packaged in a 40 pin DIP. The following is a functional description of each pin. A bar over a signal (SIGNAL), means active Low.

Table 1. DESCRIPTION OF WD1931 PIN FUNCTIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1		NC	No connection allowed to this pin. Used internally only.
2		NC	No connection.
3	READ ENABLE	$\overline{RE}$	This input, when low (and $\overline{CS}$ is active), gates the content of addressed register onto the Data bus.
4	CHIP SELECT	$\overline{CS}$	This input, when low, selects the WD1931 for a read or write operation to/from the Data bus.
5	MISC OUTPUT	$\overline{MISC\ OUT}$	This output is an extra programmable output signal for the convenience of the user. Is controlled by the CR4 bit (sync. mode) or CR5 bit (async mode).
6	INTERRUPT REQUEST	INTRQ	This output is high whenever any of the interrupt conditions occur. Reading the status register resets this signal (see Note 1).
7	WRITE ENABLE	$\overline{WE}$	This input when low (and $\overline{CS}$ is active), gates the content of the Data bus into the addressed register.
8-15	DATA BUS	$\overline{D0}$-$\overline{D7}$	Bidirectional three-state Data Bus. Bit 7 is MSB.
16	MASTER RESET	$\overline{MR}$	This input, when low, initializes all the registers, and forces the WD1931 into an idle state. The WD1931 will remain idle until a command is issued by the CPU.
17	DATA TERMINAL READY	$\overline{DTR}$	Modem Control Signal. This output when low, indicates to the Data Communication Equipment (DCE) that the WD1931 is ready to transmit or receive data.
18	DATA REQUEST OUTPUT	DRQO	This output, when high, indicates that the Transmitter Holding Register (THR) is empty and ready to receive a data character from the Data bus for a transmit operation. Loading THR resets this signal.
19	DATA REQUEST INPUT	DRQI	This output, when high, indicates that Receiver Holding Register (RHR) contains a newly received data character, available to be read onto the Data bus. Reading RHR resets this signal.
20	V_{SS}	V_{SS}	Ground. No connection.
21,22,23	ADDRESS LINES	NC, $\overline{A0}$, $\overline{A1}$	These inputs are used to address the CPU interface registers for read/write operations.
24	V_{DD}	V_{DD}	+12V.
25	TRANSMITTED DATA	TD	This output transmits the serial data to the Data Communications Equipment/Channel.
26	RECEIVE CLOCK	$\overline{IXRC}$	IX Receive Clock. This input is used to synchronize the received data. Data is sampled on the positive transition of this signal.

Table 1. PIN FUNCTIONS (Continued)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
27	RECEIVED DATA	RD	This input receives the serial data from the Data Communication Equipment/Channel.
28	TRANSMITTER BYTE OUTPUT COMPLETE	TBOC	This output goes high after the last bit of a byte is transmitted including parity if enabled, and is valid for one bit period.
29	CLEAR TO SEND	$\overline{CTS}$	Modem Control Signal. This input when low, indicates that the DCE is ready to accept data from the WD1931.
30	RECEIVER SAMPLE CLOCK	RSCLK	This output goes high when the receiver data is sampled, and is valid for one clock period.
31	TRANSMIT CLOCK 1X TRANSMIT CLOCK	$\overline{1XTC}$	This input is used to synchronize the transmitted data. The falling edge of this signal generates new transmitted data.
32	REQUEST TO SEND	$\overline{RTS}$	Modern Control Signal. This output, when low, indicates to the DCE that the WD1931 is ready to transmit data. If Bit 1 of Control Register 1 is reset during a transmission then $\overline{RTS}$ will go high on the falling edge of the transmitter clock that follows the last bit of the current transmission character.
33	DATA SET READY	$\overline{DSR}$	Modem Control Signal. This input, when low, indicates that the DCE is ready to receive or transmit data.
34	RING INDICATOR	$\overline{RI}$	Modem Control Signal. This input generates an interrupt when made low with DTR off.
35-38	CLOCK RATES	R1-R4	These four rate inputs are used for 32X Local Transmit and Receive clocks. The rate is selected by the Control Register. R1 is common to both Transmitter and Receiver. R2-R4 are clock rates for the Transmitter only.
39	CARRIER DETECT	$\overline{CD}$	Modem Control Signal. This input appears as Status Bit 5 and generates interrupts when going on or off if DTR is on.
40	V_{CC}	V_{CC}	+5V

ORGANIZATION

The WD1931 block diagram is illustrated on page 1. The primary sections include the control, buffer, status, receiver, transmitter, comparison and sync registers.

CONTROL REGISTERS — There are two 8-bit Control Registers which hold device programming signals such as mode selection, clock selection, interface signal control, and data format. Each of the Control Registers can be loaded from the Data Bus by a Write operation or read onto the Data Bus by a Read operation. The registers are cleared by a Master Reset.

RECEIVER HOLDING REGISTER — This 8-bit parallel buffer register presents assembled received characters to the Data Bus when requested through a Read operation.

STATUS REGISTER — This 8-bit register holds information on communication errors, interface data register status, match character conditions, and communication equipment status. This register may be read onto the Data Bus by a Read operation.

DLE REGISTER — This 8-bit register is loaded from the Data Bus by a Write operation and holds the DLE character used in the Transparent mode of operation in which an idle transmit period is filled with the combination DLE-SYN pair of characters rather than a single SYN character. In addition the WD1931 may be programmed to force a single DLE character prior to any data character transmission while in the transmitter transparent mode. This register cannot be read onto the Data Bus. It must be loaded with logic zeroes in all unused high-order bits.

SYN REGISTER — This 8-bit register is loaded from the Data Bus by a Write operation and holds the synchronization code used to establish receiver character synchronization. It serves as a fill character when no new data is available in the Transmitter Holding Register during transmission. This register cannot be read onto the Data Bus. It must be loaded with logic zeroes in all unused high-order bits.

TRANSMITTER HOLDING REGISTER — This 8-bit parallel buffer register holds parallel transmitted data transferred from the Data Bus by a Write operation. This data is transferred to the Transmitter Register when the transmitter section is enabled and the Transmitter Register is empty.

RECEIVER REGISTER — This 8-bit shift register inputs the received data at a clock rate determined by the selected receiver clock. This incoming data is assembled to the selected character length and then transferred to the Receiver Holding Register with logic zeroes filling out any unused high-order bit positions.

TRANSMITTER REGISTER — This 8-bit shift register is loaded from the Transmitter Holding Register, SYN register, or DLE register. The purpose of this register is to serialize data and present it to the transmitted Data output.

COMPARATOR — The 8-bit comparator is used in the Synchronous mode to compare the assembled contents of the Receiver Register to the SYN register or DLE register. A match between the registers sets up stripping of the received character, if so programmed, by preventing the data from being loaded into the Receiver Holding Register. A bit in the Status Register is set when stripping is performed. The comparator output also enables character synchronization of the Receiver on two successive matches with the SYN register.

DATA BUS — The Data Bus is an 8-bit inverted bidirectional bus port over which all data, control, and status transfers occur.

WD1931 OPERATION

ASYNCHRONOUS MODE

Framing of asynchronous characters is provided by a Start bit (logic zero) at the beginning of a character and a Stop bit (logic one) at the end of a character. Reception of a character is initiated on recognition of the first Start bit after a preceding Stop bit. The Start and Stop bits are stripped off while assembling the serial input into a parallel character. If enabled, the parity bit is checked and then stripped off.

The character assembly is completed by the reception of the Stop bit after reception of the last character or parity bit. If this bit is a logic one, the character is determined to have correct framing and the WD1931 is prepared to receive the next character. If the Stop bit is a logic zero, the Framing Error Status flag is set and the Receiver assumes this bit to be the Start bit of the next character. Character assembly continues from this point if the input is still a logic zero when sampled at the theoretical center of the assumed Start bit. As long as Received Data is spacing, all zero characters are assembled and error flags and data received interrupts are generated so that line breaks can be determined. After a character of all zeroes is assembled along with a zero in the Stop bit location, the first received logic one is determined as a Stop bit and this resets the Receiver circuit to a Ready state for assembly of the next character.

In the Asynchronous mode the character transmission occurs when information contained in the Transmitter Holding Register is transferred to the Transmitter Register. Transmission is initiated by the insertion of a Start bit, followed by the serial output of the character (least significant bit first) with parity, if enabled, following the most significant bit, then the insertion of a 1-, 1.5-, or 2-bit length Stop bit. If the Transmitter Holding Register is full, the next character transmission starts after the transmission of the Stop bit(s) of the present character in the Transmitter Register. Otherwise, the Mark (logic one) condition is continually transmitted until the Transmitter Holding Register is loaded.

In order to allow re-transmission of data received at a slightly faster character rate, means are provided for

shortening the Stop bit length to allow transmission of characters to occur at the same rate as the reception of characters. The Stop bit may be shortened a maximum of 1/16 of a bit period for 1-Stop bit selection and 3/16 of a bit period for 1.5-*, or 2-Stop bit selection. To shorten the Stop bit the user must load the Transmitter Holding Register exactly (X + 2) 16ths of a bit period before the end of a stop bit transmission, where X = the number of 16ths the user wishes to strip. If X + 2 exceeds the maximum then no shortening occurs. This feature does not work in 1X clocking mode.

***NOTE:** As a special case, the 1.5 stop bit mode can be shortened from 1/24 to 11/24 of the whole period if the Transmitter Holding Register is loaded (X + 2) 24ths (of the whole period) before the end of the stop bit transmission.

SYNCHRONOUS MODE

Framing of characters is carried out by a special Synchronization Character Code (SYN) transmitted at the beginning of a block of characters. The Receiver, when enabled, searches for two continuous characters matching the bit pattern contained in the SYN register. During the time the Receiver is searching, data is not transferred to the Receiver Holding Register, status bits are not updated, and the DRQI is not activated. After the detection of the first SYN character, the Receiver assembles subsequent bits into characters whose length is determined by contents of the Control Register. If, after the first SYN character detection, a second SYN character is present, the Receiver enters the Synchronization mode until the Act Rec bit is turned off. If a second successive SYN character is not found, the Receiver reverts back to the Search mode.

In the Synchronous mode a continuous stream of characters are transmitted once the Transmitter is enabled. If the Transmitter Holding Register is not loaded at the time the Transmitter Register has completed transmission of a character, this idle time will be filled by a transmission of the character contained in the SYN register in the Non-transparent mode, or the characters contained in the DLE and SYN registers respectively while in the Transparent mode of operation.

DETAILED OPERATION

Receiver — The Received Data input is clocked into the Receiver Register by a 1X Receive Clock from a modem Data Set, or by a local 32X bit rate clock selected from one of four externally supplied clock inputs (R1-R4). When using the 1X clock, the Received Data is sampled on the positive transition of the clock in both the Asynchronous and Synchronous modes. When using a 32X clock in the Asynchronous mode, the Receive Sampling Clock is phased to the Mark-To-Space transition of the Received Data Start bit and defines, through clock counts, the center of each received Data bit within +0%, −3% at the positive transition 16 clock periods later.

In the Synchronous mode the Sampling Clock is phased to all Mark-To-Space transitions of the Received Data inputs when using a 32X clock. Each transition of the data causes an incremental correction of the Sampling Clock by 1/32nd of a bit period. The Sampling Clock can be immediately phased to every Mark-To-Space Data transition by setting Bit 4 of Control Register 1 to a logic one while the Receiver is disabled.

After a complete character has been shifted into the Receiver Register, this is transferred to the Receiver Holding register. The unused higher number bits are filled with zeroes. At this time the Receiver Status bits (Framing Error/Syn Detect, Parity Error/DLE Detect, Overrun Error and DRQI) are updated in the Status Register and the DRQI interrupt is activated. Parity Error is set, if encountered and if the Receiver parity check is enabled in the Control Register. Overrun Error is set if the DRQI bit is not cleared through a Read operation when a new character is ready to be transferred to the Receiver Holding Register. This error flag indicates that new data is lost and the old data character and its status flags are saved.

The characters assembled in the Receiver Register that match the contents of the SYN or DLE registers are not loaded into the Receiver Holding Register and the DRQI is not set if Bit 3 of Control Register 2 (CR23 = SYN Strip) or Bit 4 of Control Register 1 (CR14 = DLE Strip) are set respectively. The SYN DETECT and DLE DETECT status bits are then set with the next non-SYN or DLE character. When both CR23 and CR14 are set (Transparent mode), the DLE-SYN combination is stripped. The SYN comparison occurs only with the character received after the DLE character. If two successive DLE characters are received only the first DLE character is stripped. No parity check is made while in this mode.

Transmitter — A character is transferred to the Transmitter Holding Register by a Write operation. This can be done at any time, even when the Transmitter is not enabled. Transmission of data is initiated only when the ACT TRAN bit is set in the Control Register and the $\overline{\text{Clear To Send}}$ input is Low. A character is normally transferred from the Transmitter Holding Register to the Transmitter Register when the latter has completed transmission of an earlier character. However, information in the DLE register may be transferred prior to this character contained in the Transmitter Holding Register if the Force DLE signal condition is enabled (CR15 and CR16 are set). The control bit CR15 must be set prior to loading of a new character in the transmitter holding register to ensure forcing the DLE character prior to transmission of this new data character. The Transmitter Register output passes through a flip-flop which delays the output by one serial data bit time. When using the 1X clock the output data changes state on the negative clock transition. When

using a local 32X clock the transmitter section selects one of the four selected clock rate inputs (R1-R4) and divides the clock (by 32) down to the baud rate. This clock is phased to the Transmitter Holding Register empty flag (DRQO) such that transmission of characters occurs within two data bit times of the loading of the Transmitter Holding Register when the Transmitter Register is empty.

When the Transmitter is enabled, the DRQO will set each time the Transmitter Holding Register is empty. If the Transmitter Holding Register still is empty when the Transmitter Register is ready for a new character, the Transmitter enters an idle state. During this idle time a logic one will be presented to the Transmitted Data output in the Asynchronous mode or the contents of the SYN register will be presented in the Synchronous Non-transparent mode (CR16 = 0). In the Synchronous Transmit Transparent mode (CR16 is set), the idle state will be filled by a DLE-SYN character transmission in that order. When entering the Transparent mode the DLE-SYN fill will not occur until the first forced DLE.

If the ACT TRAN bit is reset while a character is currently being transmitted, this character will be completed before the transmitter goes idle. When CTS goes high however, the transmitter (TD) immediately goes idle.

When the Transmit parity is enabled, the selected Odd or Even parity bit is inserted between the character and the Stop-bit/s. Parity cannot be enabled in the Synchronous Transparency mode.

CLOCKING

Two clocking schemes are used. In one case a 1X Receiver Timing and Transmitter Timing are used to clock their respective data. In the second case a 32X clock is used to clock the data. The device is capable of selecting from four externally supplied clock-rates (R1-R4).

The use of the 1X clock is the same for the receiver and the transmitter in both the Synchronous and Asynchronous Character modes.

The use of the 32X clock in the receiver differs depending on mode. In the Asynchronous Character mode the receive sampling clock is phased to the mark-space transition of Received Data input at the beginning of the Start bit, causing the Sampling clock to be approximately in the middle of the bit. The accuracy of sampling is +0%, −3%. In the Synchronous Character mode the Receive Sampling clock is phased to all the mark-space transitions on the Received Data input. Each such transition of the data causes an incremental correction of the Sampling clock of 1/32 of the bit period. The Sampling clock can be immediately phased with the data transitions by setting Bit 4 of Control Register 1 to a 1 bit with the receiver disabled. As long as this bit is a one the Sampling clock is locked to every mark-space data transition.

The transmitter divides the selected rate input down to the baud rate. This clock is phased to the DRQO so that character transmission starts within two clocks of the THR loading when the transmitter is idle.

AUTO ECHO FEATURE

The device is capable of serially echoing the received data with a one bit delay when in the Asynchronous mode and the Receiver on. This causes the clocked regenerated received data to be presented to the Transmit Data output rather than the output of the Transmitter Register and a steady marking on TD output. This serial method of echoing does not present any abnormal restrictions on the transmit speed of the terminal. Breaks are not echoed back. When the device detects a Zero Stop bit and a character of all zeroes, the echoing stops and a steady marking is transmitted until such time as normal character reception resumes. Because echoing is taking place during determination of a break condition, a single character of all zeroes (Null character) is echoed when a break is initiated at the terminal. The Echoing is enabled by setting Bit 4 of Control Register 1. Echoing does not start until the start of a receive character at a time when the transmitter is idle and $\overline{CTS}$ is low. If the Transmitter is forced out of the idle mode while a character is being echoed transmission of that character is halted. The Transmitter is idle when CR11 is a zero or the Transmitter is waiting for the THR to be loaded in the Asynchronous mode.

LOOP FEATURE

The device has on-line diagnostic capability. When bit CR17 is a zero (LOOP), the data and data set controls are appropriately looped as follows:

- Transmit Data is connected to Receive Data, with the TD output pin held in a MARK condition and the RD input pin disregarded.
- Transmitter clock is connected to the Receive clock.
- The Data Terminal Ready output is connected to the Data Set Ready input with the $\overline{DTR}$ output pin held in an OFF condition and the $\overline{DSR}$ input pin disregarded.
- The Request To Send output is internally connected to the Clear To Send input and Carrier Detect inputs, with the $\overline{RTS}$ output pin held in an OFF condition and the $\overline{CTS}$ and $\overline{CD}$ input pins disregarded.
- $\overline{MISCELLANEOUS}$ output is also held in an OFF condition.

INPUT/OUTPUT OPERATIONS

All data, control, and status information is when needed transferred to the Data bus. Control and address lines provide for controlling and addressing of input and output operations. In addition, other lines provide interrupt capability for alerting a CPU that input/output is required. Input/output terminology is referenced to the CPU; therefore, a Read or In-

put receives data from the device and places it on the Data bus, while a Write or Output places data from the Data bus into the device.

Read

A read operation is initiated when both $\overline{CS}$ and $\overline{RE}$ go low. When the Read Enable ($\overline{RE}$) line goes low, the device gates the contents of the addressed register onto the Data bus. The device becomes unselected when either the $\overline{CS}$ or $\overline{RE}$ go high. When the Receiver Holding Register is read, the DRQI is reset.

Write

A Write operation is initiated when both $\overline{CS}$ and $\overline{WE}$ go low. When the Write Enable ($\overline{WE}$) line goes low, the device gates the data from the Data bus into the addressed register. When either the $\overline{CS}$ or $\overline{WE}$ go high the device becomes unselected. When the Transmitter Holding Register is written into, the DRQO is reset.

After first writing into SYN the device is conditioned to write into DLE if followed by another Write to that same address. Any intervening Read or Write to other addresses reset this condition.

$\overline{A0}$ and $\overline{A1}$ address device registers for Read/Write operations are shown here:

Table 2. REGISTER ADDRESS FOR READ/WRITE OPERATIONS

$\overline{A1}$	$\overline{A0}$	Read	Write
LO	LO	Control Register 1	Control Register 1
LO	HI	Control Register 2	Control Register 2
HI	LO	Status Register	SYN & DLE Register
HI	HI	Receiver Holding Register	Transmitter Holding Register

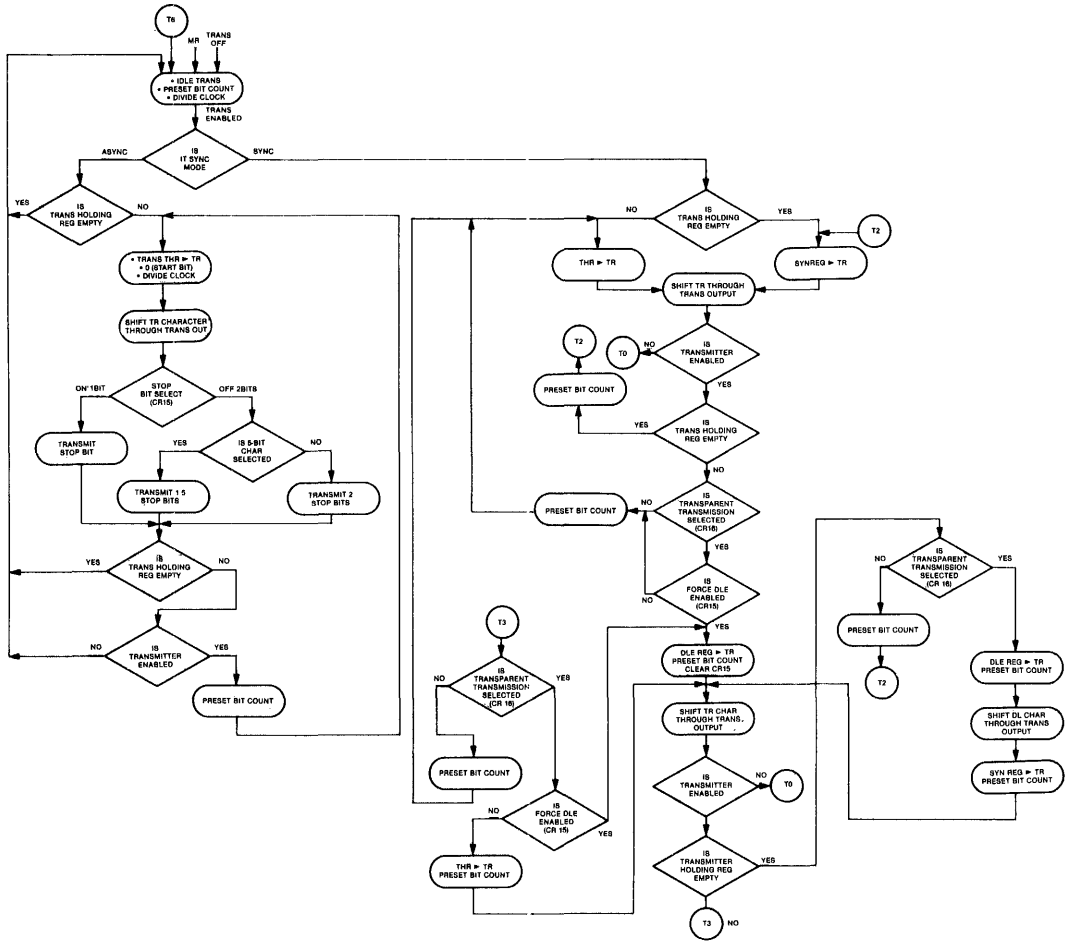
DEVICE PROGRAMMING

Programming, operating and monitoring of the WD1931 is done via two Control Registers, one Status Register, a SYN/DLE Register, and the Transmit and Receive Holding Registers. The two Control Registers are referred to as CR1 and CR2. The bits within CR1 are referred to as CR10 through CR17, and the bits within CR2 are referred to as CR20 through CR27. For any register bit 0 is the LSB.

Two general modes of operation exist for the WD1931, Asynchronous and Synchronous. Both modes of operation are discussed separately. BI-SYNC is a special case of Synchronous mode and is not treated separately.

Following figures below show CR1, CR2, and the Status Register bit definitions. The meaning of each bit in each register is described twice: once for Asynchronous mode and again for Synchronous mode. The figures combine and summarize both modes.

See page 725 for ordering information.



TRANSMITTER SECTION (ASYNCHRONOUS) **TRANSMITTER SECTION (SYNCHRONOUS)**

Figure 5. TRANSMITTER FLOW CHART

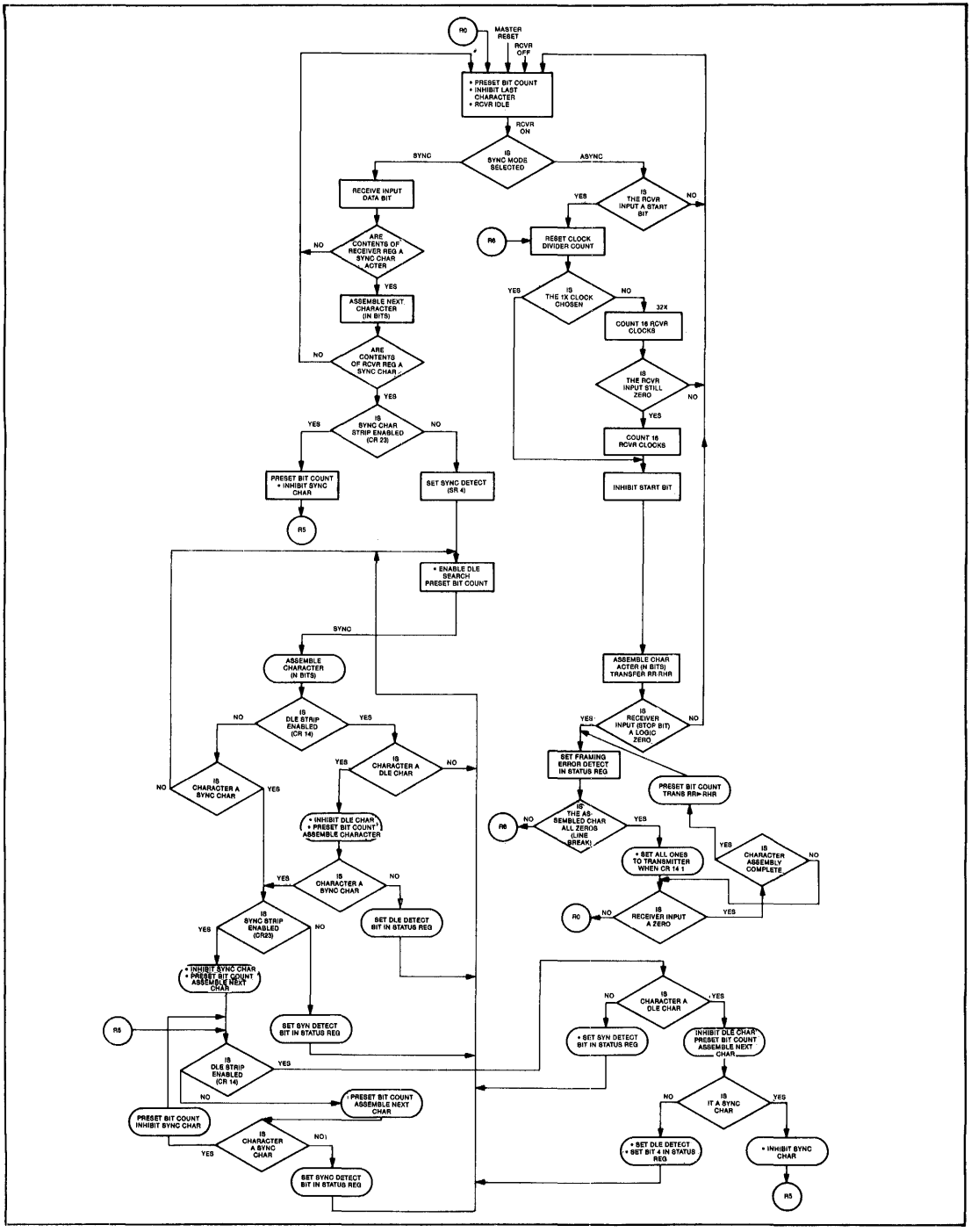


Figure 6. RECEIVER FLOW CHART

ASYNCHRONOUS MODE

Control Register 1

BIT	NAME	FUNCTION
0	DATA TERMINAL READY ($\overline{DTR}$)	This bit controls the data Terminal Ready ($\overline{DTR}$) signal to the data set. When CR10 is a logical 0, $\overline{DTR}$ is off. When CR10 is a logical 1, $\overline{DTR}$ is on. When the Self-Test mode is selected, $\overline{DTR}$ signal is forced to an off state
1	ACTIVATE TRANSMITTER (ACT TRAN)	This bit when set, enables the transmitter and sets $\overline{RTS}$ signal. When this bit is reset, the Transmitter is disabled and the $\overline{RTS}$ output turned off, but not till the end of any current character being transmitted. The $\overline{RTS}$ output may be used for other functions such as "Make Busy" on 103 data sets.
2	ACTIVATE RECEIVER (ACT REC)	When set, enables the receiver, allowing received characters to be placed in the Receiver Holding Register, Status Bits 1, 2, 3 and 4 to be updated, and the Data Request input to be generated. When reset, the above status bits are cleared. After this bit is set, character reception starts with the first bit after a valid start bit.
3	PARITY ENABLE	When set, enables check of parity on received characters and generation of parity for transmitted characters.
4	ECHO MODE	When set, and the RECEIVER is enabled, the clocked regenerated data is presented to the Transmitted Data output. The transmitter does not have to be enabled.
5	STOP BIT SELECTION/MISCELLANEOUS	When set, with the transmitter enabled, causes a single stop bit to be transmitted. When reset, causes two stop bits to be transmitted for character lengths of 6, 7, or 8 bits and 1.5 stop bits for a character length of 5 bits. When the transmitter is not enabled, this bit controls the $\overline{MISCELLANEOUS}$ output on Pin 5 to be used for Make Busy on 103 Data Sets, Secondary Transmit on 202 Data Sets, or dialing on CBS Data Couplers.
6	BREAK	When set, and the transmitter is enabled, the Transmitted Data is held in a spacing condition starting with the end of any current character. Normal transmitter timing continues so that the break can be timed out by loading characters into the THR, i.e., DRQOs are generated and the transmitter operates normally except for the output which remains low while this bit is a one.
7	LOOP/NORMAL	When this bit is reset, the device is configured to provide an internal data and control loop and the Ring Indicator interrupt is disabled. When this bit is set, the device is in normal full duplex configuration and the Ring Indicator interrupt is enabled.

Control Register 2

BIT	NAME	FUNCTION
2-0	CLOCK SELECT	Selects Transmit and Receive clock as follows: 0 — $\overline{IXRC}/\overline{IXTC}$ (IX) Transmitter Clock and if RX = 0, also Receive Clock 1 — Rate 1 (32X) 2 — Rate 2 (32X) 3 — Rate 3 (32X) 4 — Rate 4 (32X) 5 — Rate 4 (64X) 6 — Rate 4 (32X) (128X) 7 — Rate 4 (32X) (256X) } Transmitter Clock Only
3	ALTERNATE RECEIVER X CLOCK	When reset, selects Rate 1 as the Receiver clock rate. When set, provides the same rate as Transmitter Clock (R1-R4). This bit must be set if 1X clocking is selected in bits 2-0.
4	PARITY ODD/EVEN	When set, selects Odd Parity and reset selects Even Parity, when Parity is enabled.
5	CHARACTER MODE	When reset, selects Asynchronous Character Mode. When set selects Synchronous Character Mode.
7-6	CHARACTER LENGTH	Selects number of bits per character as follows (excluding parity bit): 0-8 bits 1-7 bits 2-6 bits 3-5 bits

SYNCHRONOUS MODE

Control Register 1

BIT	NAME	FUNCTION
0	DATA TERMINAL READY (DTR)	This bit controls the data Terminal Ready ($\overline{DTR}$) signal to the data set. When CR10 is a logical 0, $\overline{DTR}$ is off. When CR10 is a logical 1, $\overline{DTR}$ is on. When the Self-Test mode is selected, $\overline{DTR}$ signal is forced to an off state
1	ACTIVATE TRANSMITTER (ACT TRAN)	This bit when set, enables the transmitter and sets $\overline{RTS}$ signal. When this bit is reset, the Transmitter is disabled and the $\overline{RTS}$ output turned off, but not till the end of any current character being transmitted. The $\overline{RTS}$ output may be used for other functions such as "Make Busy" on 103 data sets.
2	ACTIVATE RECEIVER (ACT REC)	When set, enables the receiver, allowing received characters to be placed in the Receiver Holding Register, Status Bits 1, 2, 3 and 4 to be updated, and the Data Request input to be generated. When reset, the above status bits are cleared. After this bit is set, character reception starts after two matches to the contents of SYN Register.

Control Register 1 (Sync Mode continued)

BIT	NAME	FUNCTION
3	PARITY ENABLE	When set, enables check of parity on received characters only.
4	DLE STRIP/MISCELLANEOUS	When set, and the receiver is activated, received characters which match the contents of the DLE Register are stripped out. Also parity checking is disabled. When the receiver is not activated, this bit controls the $\overline{\text{MISCELLANEOUS}}$ output on Pin 5 to be used for New Sync on a 201 Data Set. When operating with a 32X clock and the receiver is not activated, this bit set also causes the receiver bit timing to synchronize on mark-space transitions.
5	TX PARITY ENABLE/ FORCE DLE	When set, with Bit 6 of Control Register 1 reset, Transmit Parity is enabled, otherwise no parity is generated. When set, with Bit 6 set, it causes the contents of the DLE Register to be transmitted prior to the next character loaded in the Transmitter Holding Register. (See description of Transparency)
6	TX TRANSPARENT	When set, the transmitter is conditioned for transparent transmission, which implies that idle fill will be DLE-SYN and a DLE can be forced ahead of any character in the THR by use of Bit 5. (See description of Transparency)
7	LOOP/NORMAL	When this bit is reset, the device is configured to provide an internal data and control loop (see Loop feature) and the Ring Indicator interrupt is disabled. When this bit is set, the device is in normal full duplex configuration and the Ring Indicator interrupt is enabled.

Control Register 2

BIT	NAME	FUNCTION
2-0	CLOCK SELECT	Selects Transmit and Receive clock as follows: 0 — $\overline{\text{IXRC}}/\overline{\text{IXTC}}$ (IX) Transmitter Clock, and if RX = 0, also Receive Clock 1 — Rate 1 (32X) 2 — Rate 2 (32X) 3 — Rate 3 (32X) 4 — Rate 4 (32X) 5 — Rate 4 (64X) 6 — Rate 4 (128X) 7 — Rate 4 (256X) } Transmitter Clock Only
3	STRIP SYN	When set, and the receiver is enabled, received characters which match the contents of the SYN Register are stripped out. Also the SYN Detect status bit will be set for the next input character. No SYN stripping occurs when reset.
4	PARITY ODD/EVEN	When set, selects Odd Parity, when reset, selects Even Parity, when parity is enabled.
5	CHARACTER MODE	When reset, selects Asynchronous Mode. When set, selects Synchronous Mode.
7-6	CHARACTER LENGTH	Selects number of bits per character as follows (excluding parity bit): 0-8 bits 1-7 bits 2-6 bits 3-5 bits

TRANSPARENCY

The Transmit Transparency mode causes Idle Fill to be the pair of characters DLE-SYN rather than a single SYN, and provides for preceding a character loaded into the THR with a DLE without the possibility of an intervening DLE-SYN fill. Transparency is enabled by Bit 6 of Control Register 1, which allows force DLE to be controlled by Control Register 1, Bit 5, but the DLE-SYN fill is not activated until after the first forced DLE. All aspects of Transparency are disabled when Bit 6 is reset. When forcing transmission of a DLE, Bit 5 should be set prior to loading the Transmitter Holding Register, otherwise the character in the Transmitter Holding Register may be transferred to the Transmitter Register prior to the setting of the Control Bit.

STATUS

The Status Register contains the following status information:

BIT	NAME	FUNCTION
0	DATA REQUEST OUTPUT (DRQO)	When set, indicates a Data Request Output, meaning THR is empty and CPU is allowed to load the new character to be transmitted into the THR register. This bit is a mirror image of DPQO signal (pin 18). Loading of THR resets DRQO.
1	DATA REQUEST INPUT (DRQI)	When set, indicates a Data Request Input meaning RHR is loaded with a new received character, and CDU is allowed to read RHR register. This bit is a mirror image of DRQI signal (pin 19). Reading RHR, resets DRQI.
2	OVERRUN ERROR (OE)	This bit is set, when the previous character in the Receiver Holding Register has *not* been read at the time a new character is ready to be transferred to the Receiver Holding Register. The bit is reset when a character is transferred to the Receiver Holding Register. It is also reset when the receiver is deactivated.
3	PARITY ERROR (PE)/ DLE DETECT	This bit is set, when the receiver is activated and Receive parity is enabled and the last received character has a parity error, and is reset if the character has correct parity. When the DLE strip is enabled, the Receiver parity check is disabled and this bit is set if the *previous character* matched the contents of the DLE Register and was stripped, otherwise it is reset. This bit is reset when the receiver is deactivated.
4	FRAMING ERROR (FE)/SYN DETECT (SD)	In the asynchronous mode this bit is set if the bit after the last data bit, in the stop-bit slot, is a zero and the receiver is enabled. This bit is reset if the stop-bit is a one. In the synchronous mode this bit is set when the contents of the Receiver Register matches the contents of the SYN Register and SYN strip is not enabled. In both modes the bit is reset when the receiver is deactivated. If SYN strip is enabled this status bit is updated when a character is received after the SYN character.
5	CARRIER DETECTOR (CD)	This bit is a mirror image of CD signal. When this signal is set, SR5 is set.
6	DATA SET READY (DRS)	This bit is a mirror image of $\overline{DSR}$ signal. When this signal is set SR6 is set. With 202-type data sets it can be used for Secondary Receive.
7	DATA SET CHANGE (DSC)	This bit is set when there is a change in the state of the Data Set Ready or Carrier Detect inputs when DTR is on, or when the Ring Indicator goes on and DTR is off. This bit is reset when the Status Register is read.

Control Registers 1, 2 and STATUS Bit Assignments

(See Note 1 and 2)

CONTROL REGISTER 1

BIT 7	6	5	4	3	2	1	0
SYNC/ASYNC 0—LOOP MODE 1—NORMAL MODE	ASYNC 0—NON BREAK MODE 1—BREAK MODE SYNC 0—NON TRANSMITTER TRANSPARENT MODE 1—TRANSMIT TRANSPARENT MODE	ASYNC (TRANS. ENABLED) 0—1 1/2 or 2 STOP BIT SELECTION 1—SINGLE STOP BIT SELECTION ASYNC (TRANS. DISABLED) 0—$\overline{\text{MISC OUT}}$ RESET (= HI) 1—$\overline{\text{MISC OUT}}$ SET (= LO) SYNC (CR16 = 0) 0—NO PARITY GENERATED 1—TRANSMIT PARITY GENERATED SYNC (CR16 = 1) 0—NO FORCE DLE 1—FORCE DLE	ASYNC 0—NON ECHO MODE 1—AUTO ECHO MODE SYNC (CR12 = 1) 0—DLE STRIPPING NOT ENABLED 1—DLE STRIPPING ENABLED SYNC (CR12 = 0) 0—$\overline{\text{MISC OUT}}$ RESET (= HI) 1—$\overline{\text{MISC OUT}}$ SET (= LO)	ASYNC 0—PARITY DISABLED 1—PARITY CHECK ENABLED ON RECEIVER PARITY GENERATION ENABLED ON TRANSMITTER SYNC 0—RECEIVER PARITY CHECK DISABLED 1—RECEIVER PARITY CHECK ENABLED	SYNC/ASYNC 0—RECEIVER DEACTIVATED 1—RECEIVER ACTIVATED	SYNC/ASYNC 0—TRANSMITTER DEACTIVATED 1—TRANSMITTER ACTIVATED	SYNC/ASYNC 0—RESETS $\overline{\text{DTR}}$ OUT (HI) 1—SETS $\overline{\text{DTR}}$ OUT (LO)

(See Note 1 and 2)

CONTROL REGISTER 2

BIT 7 6	5	4	3	2 1 0
SYNC/ASYNC CHARACTER LENGTH SELECT 00 = 8 BITS 01 = 7 BITS 10 = 6 BITS 11 = 5 BITS	MODE SELECT 0—ASYNCHRONOUS MODE 1—SYNCHRONOUS MODE	SYNC/ASYNC 1—ODD PARITY SELECT 0—EVEN PARITY SELECT	ASYNC 1—RECEIVER CLOCK DETERMINED BY BITS 2-0 0—RECEIVER CLK = RATE 1 0—NO SYN STRIP 1—SYN STRIP	SYNC/ASYNC CLOCK SELECT 000 - IX CLOCK 001 - RATE 1 CLOCK (32X) 010 - RATE 2 CLOCK (32X) 011 - RATE 3 CLOCK (32X) 100 - RATE 4 CLOCK (32X) 101 - RATE 4 CLOCK (64X) 110 - RATE 4 CLOCK (128X) 111 - RATE 4 CLOCK (256X)

NOTE 1. As a result of the WD1931's inverted data bus, to set a bit in above registers, the respective data bus line is to be set to low (V_{IL}).

(See Note 2)

STATUS REGISTER

BIT 7	6	5	4	3	2	1	0
• DATA SET CHANGE (DSC)	• DATA SET READY (DSR)	• CARRIER DETECTOR (CD)	• FRAMING ERROR/ SYN DETECT (FE/SD)	• DLE DETECT/ PARITY ERROR (DLE/PE)	• OVERRUN ERROR (OE)	• DATA REQUEST INPUT (DRQI)	• DATA REQUEST OUTPUT (DRQO)

NOTE 2. As a result of the WD1931's inverted data bus, when reading above registers, a data bus line set to low (V_{IL}), indicates the respective bit in the addressed register is set (logical 1).

REGISTER ADDRESS

LO = V_{IL} at pins

HI = V_{OH} at pins

Reg	$\overline{A1}$	$\overline{A0}$	Read	Write
0	LO	LO	Control Register 1	Control Register 1
1	LO	HI	Control Register 2	Control Register 2
2	HI	LO	Status Register	SYN & DLE Register
3	HI	HI	Receiver Holding Register	Transmitter Holding Register

DATA SET CHANGE INTERRUPTS

The following interrupts can be generated.

Carrier Detect On

The Carrier Detect On interrupt occurs when the Carrier Detect input ($\overline{CD}$) goes low and $\overline{DTR}$ is on.

Carrier Detect Off

The Carrier Detect Off interrupt occurs when the Carrier Detect input ($\overline{CD}$) goes high and $\overline{DTR}$ is on.

DSR On

The DSR On interrupt occurs when the Data Set Ready input ($\overline{DSR}$) goes low and $\overline{DTR}$ is on.

DSR Off

The DSR Off interrupt occurs when the Data Set Ready input ($\overline{DSR}$) goes high and $\overline{DTR}$ is on.

Ring Indicator On

The Ring Indicator On interrupt occurs when the Ring Indicator input ($\overline{RI}$) goes low and $\overline{DTR}$ is off.

When an interrupt condition exists, the INTRQ output is set. Reading the Status Register or activating Master Reset ($\overline{MR}$) will reset INTRQ.

DATA BUS CONTROLS

The following Data Bus controls can be generated.

Data Request Output

This control signal occurs when the THR is empty while the transmitter is enabled.

Data Request Input

This control signal occurs when the RHR is full while the receiver is enabled.

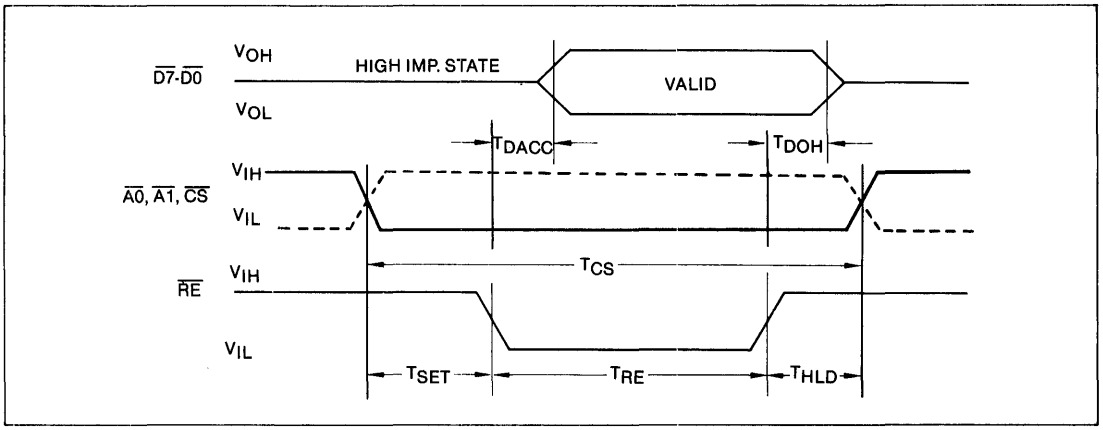


Figure 3. READ TIMING

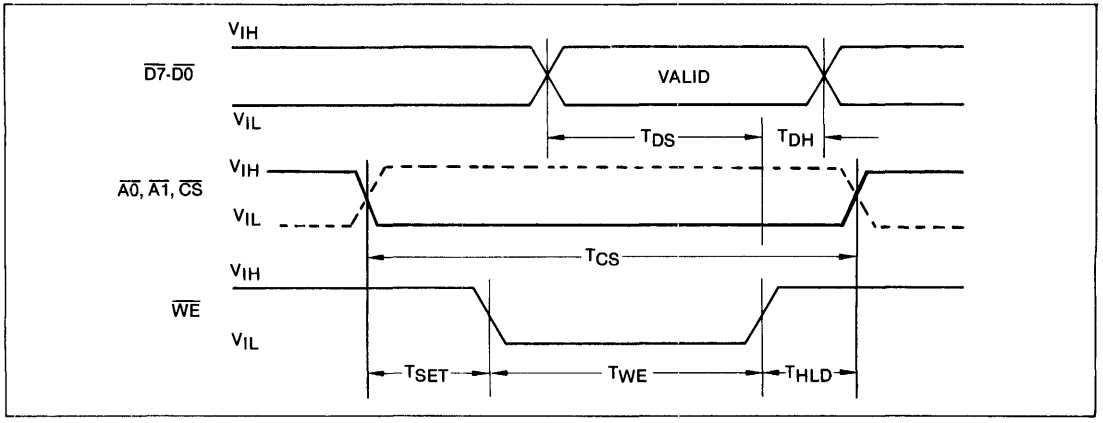


Figure 4. WRITE TIMING

MAXIMUM RATINGS

V_{DD} With Respect to V_{SS} (Ground)		+15 to −0.3V
Max. Voltage To Any Input With Respect to V_{SS}		+20 to −0.3V
Operating Temperature		0°C to +70°C
Power Dissipation		600 mW
Storage Temperature	Ceramic	−65°C to +150°C
	Plastic	−55°C to +125°C

Table 3. WD1931 DC CHARACTERISTICS

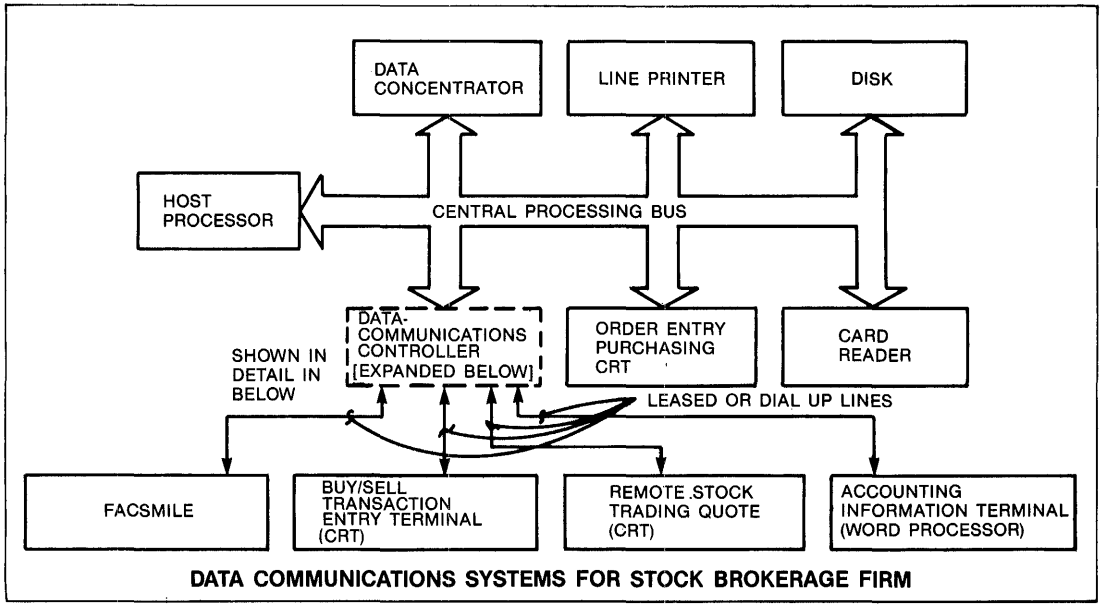
T_A = 0°C to +70°C, V_{DD} = +12.0V ± 0.6V, V_{CC} = +5.0V ± 0.25V, V_{SS} = 0V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	μA	$V_{OUT} = V_{CC}$
I_{CCAVE}	V_{CC} Supply Current			80	mA	
I_{DDAVE}	V_{DD} Supply Current			10	mA	
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage (All Inputs)			0.8	V	
V_{OH}	Output High Voltage	2.8			V	$I_O = -100\mu A$
V_{OL}	Output Low Voltage			0.45	V	I_O = 1.6 mA

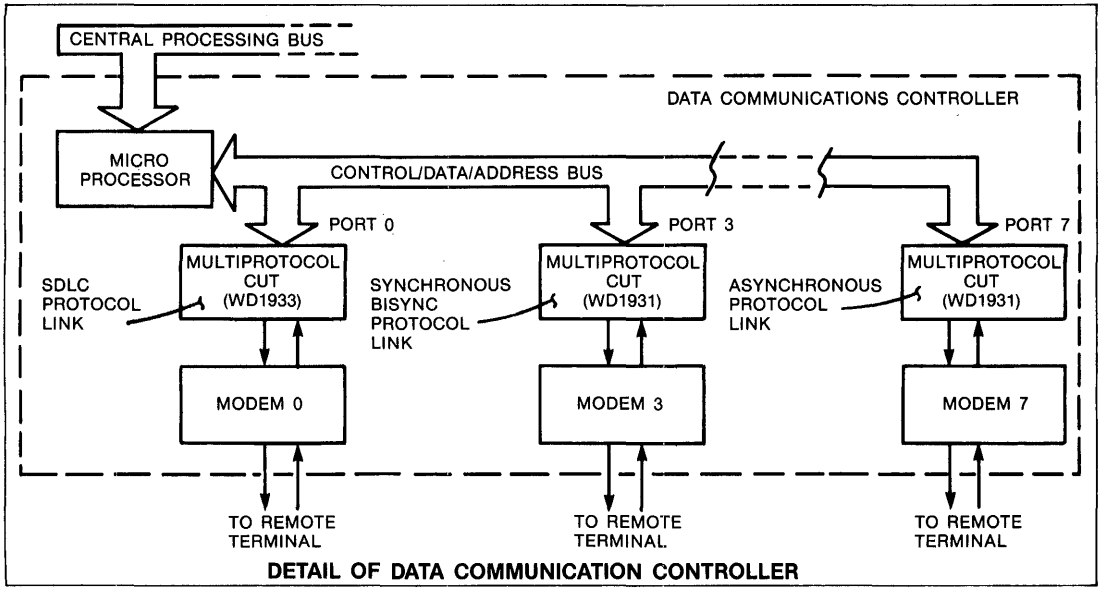
Table 4. WD1931 AC CHARACTERISTICS

T_A = 0°C to +70°C, V_{DD} = +12.0V ±0.6V, V_{SS} = 0V, V_{CC} = +5.0 ±0.25V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{HLD}	$\overline{A0}$, $\overline{A1}$ & $\overline{CS}$ Hold Time	5			ns	
T_{CS}	$\overline{A0}$, $\overline{A1}$ & $\overline{CS}$ Width	495			ns	
T_{SET}	$\overline{A0}$, $\overline{A1}$ & $\overline{CS}$ Set-Up time	240			ns	
T_{CYCLE}	Cycle Time	1000			ns	
T_{MR}	$\overline{MR}$ Pulse Width	450			ns	
READ						
T_{RE}	$\overline{RE}$ Width	250			ns	
T_{DACC}	Data Access from $\overline{RE}$			300	ns	CL = 25 pf
T_{DOH}	Data Hold from $\overline{RE}$	50		150	ns	CL = 25 pf
WRITE						
T_{WE}	$\overline{WE}$ Width	250			ns	
T_{DS}	Data Set-Up Time	250			ns	
T_{DH}	Data Hold Time	100			ns	



DATA COMMUNICATIONS SYSTEMS FOR STOCK BROKERAGE FIRM



DETAIL OF DATA COMMUNICATION CONTROLLER

DIGITAL COMMUNICATIONS SYSTEM

The diagrams above illustrate a typical digital system employing several processing levels and digital protocols. It is flexible enough to satisfy several applications. For example. the host processor and remote terminals could be located respectively in airline reservation offices and ticket counters, travel centers and travel agencies, central bank offices and branch banks, or department stores and individual cash registers. The exploded diagram of the Data-Communications Controller exemplifies the use of one common circuit board design with eight multi-protocol circuits. When the Port requires a character-oriented protocol (synchronous, asynchronous, or synchronous-bisync), the WD1931 is plugged into the appropriate socket. For SDLC, HDLC or ADCCP, the WD193X is used.

WESTERN DIGITAL
CORPORATION

WD193X
Synchronous Data Link Controller

FEATURES

- HDLC, SDLC, ADCCP AND CCITT X.25 COMPATIBLE
- SDLC LOOP DATA LINK CAPABILITY
- FULL OR HALF DUPLEX OPERATION
- DC TO 2.0 MBITS/SEC DATA RATE
- PROGRAMMABLE/AUTOMATIC FCS (CRC) GENERATION AND CHECKING
- PROGRAMMABLE NRZI ENCODE/DECODE
- FULL SET OF MODEM CONTROL SIGNALS
- DIGITAL PHASE LOCKED LOOP
- FULLY COMPATIBLE WITH MOST CPU'S
- MINIMUM CPU OVERHEAD
- ASYNCHRONOUS/SYNCHRONOUS MULTI-PROTOCOL BOARD CAPABILITY (PIN COMPATIBLE WITH WD 1931)
- FULLY TTL COMPATIBLE
- SINGLE +5V SUPPLY
- ERROR DETECTION: CRC, UNDERRUN, OVERRUN, ABORTED OR INVALID FRAME ERRORS
- STRAIGHT FORWARD CPU INTERRUPTS
- PROGRAMMABLE MODEM CONTROL INTERRUPTS
- DOUBLE BUFFERING OF DATA
- DMA COMPATABILITY
- END OF BLOCK OPTION
- VARIABLE CHARACTER LENGTH (5, 6, 7 OR 8 BITS)
- RESIDUAL CHARACTER CAPABILITY
- ADDRESS COMPARE
- GLOBAL ADDRESS RECOGNITION
- EXTENDABLE ADDRESS FIELD
- EXTENDABLE CONTROL FIELD
- AUTOMATIC ZERO INSERTION AND DELETION
- MAINTENANCE MODE FOR SELF-TESTING

APPLICATIONS

- COMPUTER COMMUNICATIONS
- TERMINAL COMMUNICATIONS
- COMPUTER TO MODEM INTERFACING

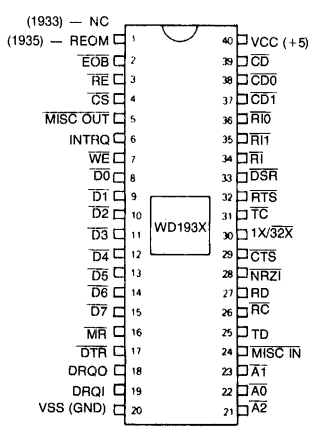


Figure 1. WD193X PIN CONNECTIONS

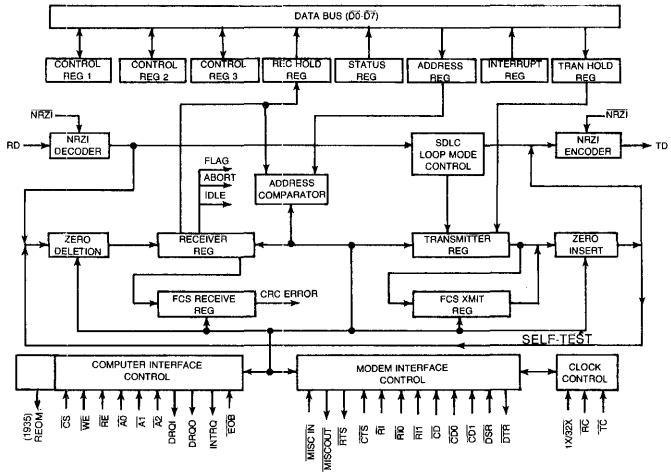


Figure 2. WD193X BLOCK DIAGRAM

- LINE CONTROLLERS
- FRONT END COMMUNICATIONS
- NETWORK PROCESSORS
- TELECOMMUNICATION SWITCHING NETWORKS
- MESSAGE SWITCHING
- PACKET SWITCHING
- MULTIPLEXING SYSTEMS
- DATA CONCENTRATOR SYSTEMS
- SDLC LOOP DATA LINK SYSTEMS
- DMA APPLICATIONS
- COMMUNICATION TEST EQUIPMENT
- LOCAL NETWORKS
- MULTIDROP LINE SYSTEMS

GENERAL DESCRIPTION

The WD193X is a MOS/LSI microcomputer peripheral device which performs the functioning of interfacing a parallel digital system to a synchronous serial data communication channel employing ISO's HDLC, IBM's SDLC or ANSI's ADCCP line protocol. These protocols are referred to as Bit-Oriented Protocols (BOP).

The chip is fabricated in N-channel depletion load MOS technology and is TTL compatible on all inputs and outputs. This controller requires a minimum of CPU software by supporting a comprehensive frame-level instruction set and by hardware implementation of the low level tasks associated with frame assembly/disassembly and data integrity. It can be programmed to encode/decode NRZI data. The internal clock is then derived from the NRZI data using a digital phase locked loop.

The receiver and transmitter logic operates as two total independent sections with a minimum of common logic. The frames are automatically checked for errors during reception by verifying correct Frame Check Sequence (FCS). In transmit mode, the FCS is automatically generated by this controller and sent before the final Flag. It also continuously checks for other errors. In case of an error, the CPU is interrupted.

The controller recognizes and can generate Flag, Abort, Idle and GA characters. WD193X can be used in an SDLC Loop configuration. An End of Block option is supplied to minimize CPU time. A full set of modem control signals are supplied to minimize external hardware.

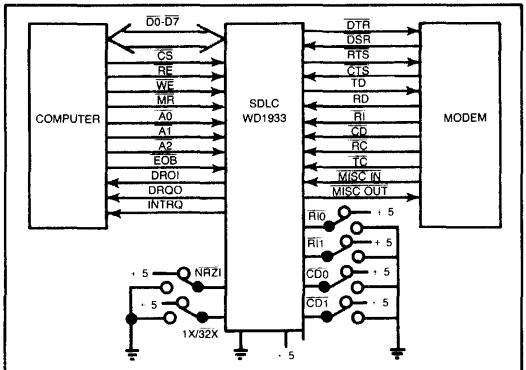


Figure 3. WD193X TYPICAL SYSTEM INTERFACE

A BRIEF DESCRIPTION OF HDLC, SDLC AND ADCCP PROTOCOLS

The WD193X is compatible with HDLC, SDLC and ADCCP standard communication Link Protocols. These are bit-oriented, code independent, and ideal for full duplex communication. A single communication element is called a FRAME, which can be used for both link control and data transfer purposes.

The elements of a frame are the beginning eight bit FLAG (F) consisting of one logical "0," six 1's and a 0, an eight bit ADDRESS-FIELD(A), an eight bit CONTROL-FIELD (C), a variable (N bits) INFORMATION-FIELD, a sixteen bit FRAME-CHECK-SEQUENCE (FCS), and an eight bit end FLAG (F), having the same bit-pattern as the beginning flag.

In HDLC, the address (A) and control (C) characters are extendable (more than one character). An important characteristic of a frame is that its contents are made code transparent by use of a zero bit insertion and deletion technique. Thus, the user can adapt any format or code suitable for his system. The frame is bit-oriented, meaning that, bits not characters in each field have specific meanings. The Frame Check Sequence (FCS) is an error detection scheme similar to the Cyclic Redundancy Checkword (CRC) widely used in magnetic disk storage devices. The frame format is shown in Figure 4.

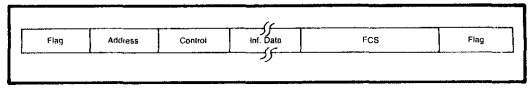


Figure 4. WD193X SDLC/HDLC/ADCCP FRAME FORMAT

Where:

FLAG = 01111110

Address field—One or more 8-bit characters defining the particular station

Control field—One or two 8-bit characters

Information field—Any number of bits (may be zero bits)

Frame Check Sequence—16-bit error checking field

The following features are also part of these protocols.

ZERO INSERTION/ZERO DELETION—Zero insertion/deletion is performed within the 2 Flags of a frame. If there are more than five 1's in a row, a 0 is automatically inserted after the fifth 1 and it is deleted upon reception by the receiver.

FRAME CHECK SEQUENCE (FCS)—A 16 bit cyclic redundancy check (CRC) calculation is performed during transmission of the data in between the 2 flags of the frame. The CRC is then transmitted after the I-field and before the final FLAG. Upon reception the receiver also performs a CRC calculation on the incoming data. If there were no transmission error, the Receiver CRC equals F0B8 (hex).

DESCRIPTION OF PIN FUNCTIONS

The WD193X is packaged in a 40 pin DIP. The following is a functional description of each pin. A bar over a signal (SIGNAL), means active Low.

Table 1. DESCRIPTION OF WD193X PIN FUNCTIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	No Connect	NC	WD1933 No Connection Allowed
	Received End of Message	REOM	Received End of Message with no Errors. Output on WD1935.
2	End of Block	$\overline{EOB}$	This input, when low, function as an FCS command. Is independent of $\overline{CS}$.
3	Read Enable	$\overline{RE}$	This input, when low (and $\overline{CS}$ is active), gates the content of addressed register onto the Data bus.
4	Chip Select	$\overline{CS}$	This input, when low, selects the WD193X for a read or write operation to/from the Data bus.
5	Misc Output	$\overline{MISC\ OUT}$	This output is an extra programmable output signal for the convenience of the user. Is controlled by the CR10 bit.
6	Interrupt Request	INTRQ	This output is high whenever any of the interrupt register bits IR7-IR3 are set.
7	Write Enable	$\overline{WE}$	This input when low (and $\overline{CS}$ is active), gates the content of the Data bus into the addressed register.
8–15	Data Bus	$\overline{D0}$–$\overline{D7}$	Bidirectional three-state Data Bus. Bit 7 is MSB.
16	Master Reset	$\overline{MR}$	This input, when low, initializes all the registers, and forces the WD193X into an idle state. The WD193X will remain idle until a command is issued by the CPU.
17	Data Terminal Ready	$\overline{DTR}$	Modem Control Signal. This output when low, indicates to the Data Communication Equipment (DCE) that the WD193X is ready to transmit or receive data.
18	Data Request Output	DRQO	This output, when high, indicates that the Transmitter Holding Register (THR) is empty and ready to receive a data character from the Data bus for a transmit operation.
19	Data Request Input	DRQI	This output, when high, indicates that Receiver Holding Register (RHR) contains a newly received data character, available to be read onto the Data bus.
20	V_{SS}	V_{SS}	Ground
21,22,23	Address Lines	$\overline{A2}$, $\overline{A0}$, $\overline{A1}$	These inputs are used to address the CPU interface registers for read/write operations.
24	Misc Input	$\overline{MISC\ IN}$	This input is an extra input signal for the convenience of the user. The state is shown by the SR4 bit.
25	Transmitted Data	TD	This output transmits the serial data to the Data Communications Equipment/Channel.
26	Receive Clock	$\overline{RC}$	This input is used to synchronize the received data.
27	Received Data	RD	This input receives the serial data from the Data Communication Equipment/Channel.
28	NRZI	$\overline{NRZI}$	This input, when low, sets the WD193X in NRZI mode.
29	Clear to Send	$\overline{CTS}$	Modem Control Signal. This input when low, indicates that the DCE is ready to accept data from the WD193X.
30	DPLL Select	1X/$\overline{32X}$	This input controls the internal clock. When high (1X clock), the external clock has the same frequency as the internal clock. When low (32X clock), the external clock is 32 times faster than the internal clock and the DPLL Logic is enabled.
31	Transmit Clock	$\overline{TC}$	This input is used to synchronize the transmitted data.

Table 1. DESCRIPTION OF WD193X PIN FUNCTIONS (Continued)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
32	Request to Send	$\overline{RTS}$	Modem Control Signal. This output, when low, indicates to the DCE that the WD193X is ready to transmit data.
33	Data Set Ready	$\overline{DSR}$	Modem Control Signal. This input, when low, indicates that the DCE is ready to receive or transmit data.
34	Ring Indicator	$\overline{RI}$	Modem Control Signal. This input, when low, indicates a ringing signal being received on the communication channel.
35,36	Ring Indicator Interrupt Control	$\overline{RI1}$, $\overline{RI0}$	These inputs are used to program Ring Indicator interrupts.
37,38	Carrier Detect Interrupt Control	$\overline{CD1}$, $\overline{CD0}$	These inputs are used to program Carrier Detect Interrupts.
39	Carrier Detect	$\overline{CD}$	Modem Control Signal. This input, when low, indicates there is a carrier signal received by the local DCE from a distant DCE.
40	V_{CC}	V_{CC}	+5VDC

Table 2. WD193X TERMINOLOGY

TERMINOLOGY

TERM	DEFINITION/DESCRIPTION
BOP	Bit-oriented protocols: SDLC, HDLC, and ADCCP
ABORT	11111111 (seven or more contiguous 1's)
GA	Go-ahead pattern. 01111111 (0(LSB) followed by seven 1's)
LSB	First transmitted bit and first received bit. (Least significant bit)
MSB	Last transmitted bit and last received bit. (Most significant bit)
IDLE	11111111 11111111 (15 or more contiguous 1's)
FLAG	01111110. Starts and ends a Frame.
A-FIELD	Address-field in the Frame. Consists of one or more 8-bit characters. Defines the address of a particular station.
C-FIELD	Control field in the Frame. Consists of one or two 8-bit characters.
I-FIELD	Information field in the Frame. Consists of any number of bits.
FCS	Frame Check Sequence. A 16-bit error checking field sequence.
FRAME	A communication element, consisting of a minimum of 32 bits, and delimited by FLAGS.
GLOBAL ADDRESS	An A-field character of eight 1's. When this is compared and matched in the Address comparator, the DRQI will be set, indicating a valid address
RESIDUAL CHARACTER	The last I-field character, consisting of a lesser amount of bits than the other I-field characters in the Frame.
DATA SET	Data Communication Equipment (DCE). May be a modem.
BIT TIME	Length in time of a serial data bit.

HARDWARE ORGANIZATION

The WD193X block diagram is illustrated in Figure 2 and described below.

CPU Interface Registers

All of these registers are addressable and to be read from and/or written into by the CPU via the Data bus. These are 8-bit registers and have to be enabled via Chip Select ($\overline{CS}$) before any data transfer can be done.

CONTROL REGISTER 1, 2, 3 (CR1, 2, 3) Operations are initiated by writing the appropriate commands into these registers. CR1 should be programmed last.

RECEIVER HOLDING REGISTER (RHR) When Data Request Input is set (DRQI=1), contains received assembled character.

ADDRESS REGISTER (AR) Contains the address of this WD193X which is to be compared to the received address character (A-field).

INTERRUPT REGISTER (IR) Contains the cause of the current interrupt request.

TRANSMITTER HOLDING REGISTER (THR) Is to be loaded with the next in line character to be transmitted, when Data Request Output is set (DRQO=1).

STATUS REGISTER (SR) Contains the overall status of the WD193X plus some information of the last received frame.

Non-Addressable, Internal Registers

These registers are transparent to the user, but is mentioned in these data sheets to help the understanding of the WD193X

TRANSMITTER REGISTER (TR) This 8-bit register functions as a buffer between the THR and the TD output. It is loaded from the THR (if Data Command) with the next character to be transmitted. A FLAG character may also be loaded into this register under program control. This character is automatically shifted out to the Transmit Data output. When the last bit of the current transmitted character has left the TR register, a new character will be loaded into this register, setting DRQO (Data command) or INTRQ (Abort, Flag or FSC command). If at the time when only one bit remains left in the TR register, and the THR is not loaded or a new command is not programmed (Data command), an underrun error will occur.

RECEIVER REGISTER (RR) The received data is, via the Zero-Deletion logic shifted into this 8-bit register. The data is here assembled to a 5, 6, 7 or 8-bit character length and then, under the right conditions, parallel transferred to the RHR register.

FCS RECEIVE REGISTER AND FCS XMIT REGISTER The WD193X contains a 16-bit CRC check register (FCS REC. REG.) and a 16-bit CRC generation register (FCS XMIT REG.). The generating polynomial is:

$$G(X) = X^{16} + X^{12} + X^5 + 1$$

The transmitter and receiver initialize the remainder value to all ones before CRC accumulation starts. The data is multiplied by X^{16} and is divided by G(X). Inserted 0's are not included in the accumulation. Under program control, the complement called the frame check sequence (FCS) is sent with high order bit first.

Various Internal Circuits

ADDRESS COMPARATOR This 8-bit comparator is used to compare the contents of the Address Register with the first address character of the incoming frame. This feature is enabled by a bit in the Command Register. If enabled and there is a match, the received frame is valid and DRQIs are generated for every character received (including the A-field). If enabled and there is not a match or there is no Global Address, the received frame is discarded. If not enabled, all received frames are valid and DRQIs are generated.

ZERO INSERTION The transmitted data stream is continuously monitored by this logic. A zero is automatically inserted following five contiguous 1 bits anywhere between the beginning FLAG and the ending FLAG of a frame. The insertion of the zero bit thus applies to the contents of the Address, Control, Information Data, and the FCS field.

ZERO DELETION The received data stream is continuously monitored by this logic. Upon receiving five contiguous 1 bits, the sixth bit is inspected. If the sixth bit is a 0, it is automatically deleted from the data stream. If the sixth bit is a 1, the seventh bit inspected; if it is a 0, a FLAG is recognized; if it is a 1 an ABORT or GO AHEAD is recognized.

DATA BUS ($\overline{D7}$-$\overline{D0}$) This is an inverted 8-bit bidirectional data bus.

SDLC LOOP-MODE CONTROL This logic supervises the WD193X running in SDLC Loop mode. It monitors the received data for a GO-AHEAD pattern in the case when SDLC LOOP MODE bit (CR22) and ACT TRAN bit (CR16) are set. When GO-AHEAD pattern is received, this logic suspends the repeater function and initiates the transmitter function. For more details, see functional description of SDLC Loop Mode.

NRZI ENCODER/DECODER When this mode is selected, the NRZI Encoder encodes the "normal" transmitted data to NRZI formatted data and the NRZI Decoder decodes the received NRZI data to "normal" data.

A binary 1 for "normal data" is TD = high.

A binary 1 for NRZI data is TD = no change.

A binary 0 for "normal data" is TD = low.

A binary 0 for NRZI data is TD = change of state.

COMPUTER INTERFACE CONTROL This logic interfaces the CPU, to the WD193X. It supervises the read and write functions to the addressable registers, generates data requests and interrupts, decodes and initiates commands, monitors the status of WD193X etc.

MODEM INTERFACE CONTROL This logic interfaces and supervises the modem control signals to/from the WD193X. It provides both dedicated (EIA Standard) and user defined control functions.

CLOCK CONTROL This logic interfaces the transmit and receive clocks to the WD193X. It converts the external clocks to the necessary internal clocks.

FUNCTIONAL DESCRIPTION

SDLC Loop Mode

The diagram below shows an SDLC Loop Data Link System. WD193X can be used in any of these stations.

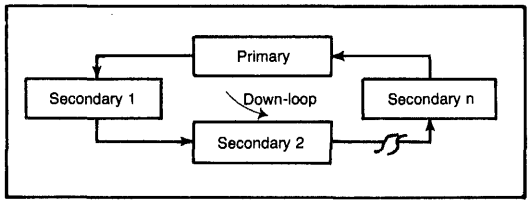


Figure 5. WD193X SDLC LOOP DATA LINK

Each secondary station is normally a repeater in Receive mode. The primary station is the loop controller. Signals sent out on the loop by the primary station are relayed from station to station, then back to the Primary. Any secondary station finding its address in the A-field captures the frame for action at that station. All received frames are relayed to the next station on the loop.

If anyone of the secondary stations wants to transmit a message, it sets its ACT TRAN bit and waits for a GO-AHEAD (GA) pattern. The WD193X recognizes seven or more contiguous logical 1's as a GO-AHEAD pattern. Until GA pattern is received, this secondary station continues operating as a repeater. When primary station is done transmitting, it may send a continuous stream of GA patterns down the Loop. This may be accomplished by going Idle. When the first in turn secondary station, with the ACT TRAN bit set, receives the GA pattern, it suspends the repeater function and immediately goes into transmit mode. It transmits its message and when completed, it resets the ACT TRAN bit. This converts the secondary station back to repeater mode. The GA-patterns still transmitted by the Primary Station, gets relayed down the Loop to the next secondary station. The next down-loop secondary station has the opportunity to transmit in the same manner. When the primary station receives the GA-pattern, all the secondary stations have been able to transmit their messages, and the cycle is completed. The Primary Station may then transmit or initiate another cycle as described above. As a repeater, the transmitted data is delayed by 4 bits (NRZI=5 bits) relative to the received data.

1X/32X Clock Option

When 1X clock is selected, the data rate equals the external clock (receiver and transmitter).

When 32X clock is selected, the external clock rate is 32 times faster than the data rate.

Digital Phase Locked Loop (DPLL)

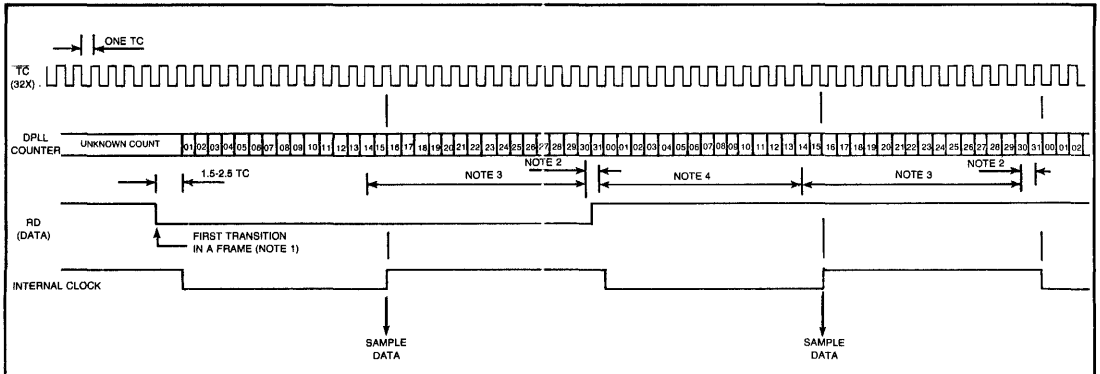
This feature is particularly useful in NRZI mode and/or when asynchronous modem is used. The purpose of the DPLL is to synchronize the internal 1X clock to the received data, thus insuring that this data is sampled in the middle of the incoming serial data bit. DPLL is automatically in operation when 32X clock is selected.

The DPLL Logic is initiated at the first received data transition in a frame. Corrections, if needed, are then made for each received data transition. A 32-counter is used for this operation. At the beginning of each frame and at the first received data transition, this 32 counter is reset. From this time on, the counter increments with one count for each external clock pulse. At count 16 the internal 1X clock is forced to change state to high (this transition = sampling time). At count 32, the counter resets itself. This forces the internal 1X clock again to change state back to low.

At each received data transition, if the internal clock and the received data is out of synchronization, a correction is automatically made by ± 1 external clock period. See DPLL Timing Diagram in Figure 6.

End Of Block (EOB)

This is an FCS command. The main purpose of EOB is to allow the user to initiate FCS and FLAG without the need of



NOTE 1. FIRST DATA TRANSITION (FIRST FLAG) SETS THE DPLL COUNTER TO 01.

NOTE 2. DATA TRANSITION IN BETWEEN HERE, OR NO DATA TRANSITION AT ALL, CAUSES NO CORRECTION OF THE DPLL COUNTER.

NOTE 3. DATA TRANSITION IN BETWEEN HERE, WILL INCREMENT ONE COUNT TO THE DPLL COUNTER (ADD 01 TO WHAT IS SHOWN).

NOTE 4. DATA TRANSITION IN BETWEEN HERE, WILL DECREMENT ONE COUNT TO THE DPLL COUNTER (SUBTRACT 01 TO WHAT IS SHOWN).

Figure 6. WD193X DPLL TIMING DIAGRAM

using extra computer time. This is particularly practical in DMA applications. At the end of a frame, when the last information data character has already been loaded into the THR and once again DRQO is set, either a regular FCS command is written into CR1 Register, or $\overline{EOB}$ is to be activated. At the end of FCS, when INTRQ is set (XMIT OPCOM), the $\overline{EOB}$ if activated is to be reset again.

Serial Data Synchronization

The serial data is synchronized by the externally supplied Transmit Clock ($\overline{TC}$) and Receive Clock ($\overline{RC}$). When 1X clock is selected, the falling edge of $\overline{TC}$ generates new transmitted data and the rising edge of $\overline{RC}$ is used to sample the received data. When 32X clock is selected, a 32-counter (in the DPLL Logic) is used to synchronize the internal clock. At time 0, when the counter is reset to 0, the new transmitted data is generated. At time 16 (counter = 16) the received data is sampled, insuring that sampling is done in the middle of the received serial data bit. At count 32, the counter is reset to 0 again.

Self Test (Diagnostic) Mode

This feature is a programmable Loop back of data, enabling the user to make a complete test of the WD1933 with a minimum of external circuitry. In this mode, transmitted data to the TD pin, is internally routed to the received data input circuitry, thus allowing a CPU to send a message to itself to verify proper operation of the WD193X. The modem control signals $\overline{DTR}$ and $\overline{RTS}$ are deactivated (off) to insure no interference to/from the Data Communication Equipment (DCE). $\overline{DSR}$ and $\overline{CTS}$ are internally activated for proper input conditions. $\overline{TC}$ and $\overline{RC}$ should be supplied by the same source if 1X clock is selected.

Auto Flag

If this is selected and Data Command is executed, continuous Flags will be sent between frames. This eliminates the need to execute the Flag Command. In DMA applications in particular, this is very practical.

Extended Addressing

This type of addressing means, that there is more than one address character in the A-field. In receive mode, the first address character is compared in the Address Comparator of the WD193X. The other address character/s is to be compared by the CPU. The last address character is recognized by the fact that the LSB (bit 2^0) is a 1.

PROGRAMMING

Controlling Operation

Prior to initiating data transmission or reception, CONTROL REGISTER 1-3 (CR1-3) must be loaded with control information from the CPU. The contents of these registers will configure the WD193X for the user's specific data communication environment. These registers should be loaded during power-on initialization and after a reset operation. They can be changed at any time that the respective transmitter or receiver is deactivated. The CR1-3 dictate what the transmitter will send: the type of character (DATA, ABORT, FLAG or FCS), the number of bits per character, and the number of bits in the residual character. Similarly, they tell the receiver the types of frames to look for: the number of bits per I-field character, whether to perform an address compare, and whether to watch for an extended address. The Control Register also control Data Terminal Ready ($\overline{DTR}$), $\overline{Misc\ Out}$ and the activation of both the transmitter and the receiver. For more detailed information, see Register Formats.

Monitoring Operation

Monitoring is done by use of the Interrupt Register (IR) and Status Register (SR). The IR register indicates when a frame is completed (transmitted or received), if there was an error and if there is a Data Set Change. It also monitors the states of INTRQ, DRQO and DRQI.

The SR register indicates if an error is recognized by IR, what type of error. It also monitors the modem control signals; Ring Indicator ($\overline{RI}$), Carrier Detect ($\overline{CD}$), Data Set Ready ($\overline{DSR}$) and $\overline{Misc\ In}$.

Furthermore, the SR register monitors if the Receiver is idle, and also if in receive mode if the user has programmed the Receiver Character Length to be 8 bits per character, this register indicates the number of residual bits received. For more detailed information, see Register Formats.

Read/Write Control Of CPU Interface Registers

These registers are directly accessible from the CPU bus ($\overline{D7}$-$\overline{D0}$) by a read and/or write operation by the CPU.

The CPU must set up the WD193X register address ($\overline{A2}$-$\overline{A0}$), Chip Select ($\overline{CS}$), Write Enable ($\overline{WE}$) or Read Enable ($\overline{RE}$) before each data bus transfer operation.

During a write operation, the falling edge of $\overline{WE}$ will initiate a WD193X write cycle. The addressed register will then be loaded with the content of the Data Bus ($\overline{D7}$-$\overline{D0}$). During a read operation, the falling edge of $\overline{RE}$ will initiate a WD193X read cycle. The addressed register will then place its content

onto the Data Bus ($\overline{D7}$-$\overline{D0}$). The read/write operation is completed, when $\overline{CS}$ or $\overline{RE}$/$\overline{WE}$ is brought high.

For more detailed information, timing, etc., see Read/Write Timing diagram.

For read and write operation, the CR1-3 registers normally need no external clock. After reset of CR1-3, $\overline{TC}$ clock is required. The AR and THR registers need no external clock, and can only be written into. The RHR, IR and SR registers need Transmit Clock ($\overline{TC}$) or Receive Clock ($\overline{RC}$) to set various bits, and are read-only.

All these registers will get initialized by a Master Reset. A read operation of RHR resets the DRQI. A write operation to THR, resets the DRQO. A read operation of IR, resets IR bits 0 and 3-7. A read operation of SR, resets SR bits 0-2.

For addressing and external clocks needed, see figure below.

$\overline{CS}$	$\overline{A2}$	$\overline{A1}$	$\overline{A0}$	Read	Write	External Clock
L	H	H	H	CR1	CR1	None*
L	H	H	L	CR2	CR2	None*
L	H	L	H	CR3	CR3	None*
L	H	L	L	RHR	AR	RHR=$\overline{RC}$. AR=None
L	L	H	H	IR	THR	IR=$\overline{TC}$. THR=None
L	L	H	L	SR	—	SR0-3=$\overline{RC}$. SR4-7=None.
H	X	X	X	X	X	

L = V_{IL} at pins
H = V_{IH} at pins
X = Don't care

* 2.5 $\overline{TC}$ clock cycles are required after a Master Reset to be able to read and write.

REGISTER FORMATS

Below shows a short form register format.

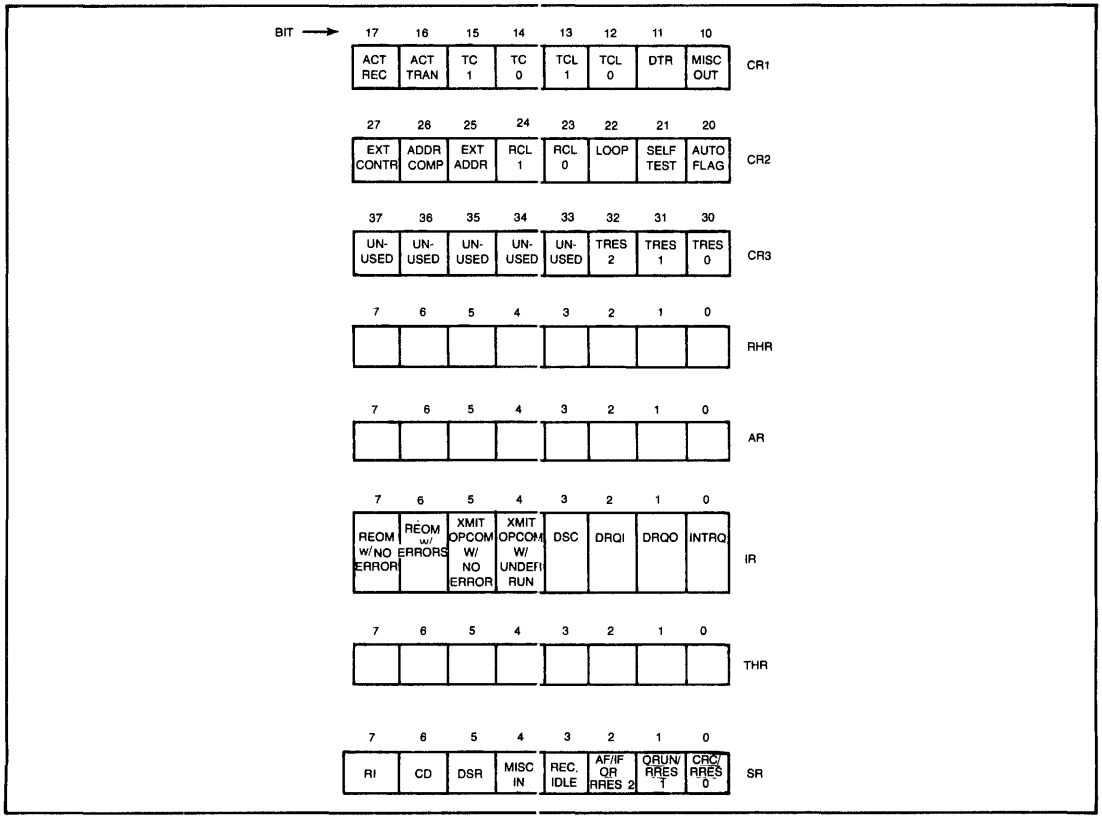


Figure 7. WD193X BIT ASSIGNMENTS

A more detailed description is shown here of each bit location. It should be known, that because the Data Bus Lines ($\overline{D7}$-$\overline{D0}$) has inverted logic, a logic 1 (set) means low state. Also, a modem control signal which is inverted (example $\overline{DTR}$), is in on-state (set) when low.

Control Register 1 (CR1)

When initiating a transmit/receive operation, this should be the last register programmed.

Miscellaneous Output (CR10) This bit controls the Miscellaneous Output signal to the data set. When CR10 is a logical 0, $\overline{Misc\ Out}$ is off, when it is a logical 1, $\overline{Misc\ Out}$ is on.

DTR Command (CR11) This bit controls the data Terminal Ready ($\overline{DTR}$) signal to the data set. When CR11 is a logical 0, $\overline{DTR}$ is off. When CR11 is a logical 1, $\overline{DTR}$ is on. When the Self-Test mode is selected, $\overline{DTR}$ signal is forced to an off state.

Transmitter Character Length (CR13, 12) These bits control the transmitted I-field data character length. The data character may be 5, 6, 7 or 8 bits long.

CR13 (TCL1)	CR12 (TCL0)	Bits Per Character
0	0	8
0	1	7
1	0	6
1	1	5

Transmitter Commands (CR15, 14) These bits control the transmission of DATA (A-field, C-field and I-field), ABORT, FLAG, and FCS (FCS plus FLAG). When these commands are programmed, the previous command currently still in progress, will complete the transmission of its character. When this is done, a new character generated by this new command, will be transmitted.

If DATA is programmed, the new character to be transmitted will be the character loaded (or still to be loaded) in the THR register. If ABORT is programmed, the new character will be eight logical 1's. If FLAG is programmed, the new character will be 01111110. If FCS is programmed, three new characters will be transmitted; first the 16-bit content of the FCS XMIT REGISTER, then a FLAG. One serial data bit time ahead of the first bit (LSB) of this new character (= FLAG character when FCS command) being transmitted, the CPU is signalled that the WD193X is again ready to receive a new command. This signal is an INTRQ (XMIT OPCOM), if the now current command is ABORT, FLAG or FCS. This signal is a DRQO, if the current command is DATA. However, in this latter case (DATA), the user has two choices; 1. Change the command. 2. Keep the DATA command and load a new character into the THR register. For more information, please see the Transmission Timing diagram, Figure 8.

Programming, see figure below.

Activate Transmitter (CR 16) This bit when set, enables the transmitter and sets $\overline{RTS}$ signal. If in SDLC Loop Mode (CR22 = set), the transmitter waits for a Go-Ahead pattern before the transmitter is enabled.

Activate Receiver (CR 17) This bit when set activates the receiver, which begins shifting in frames one character at a time into RR register for inspection.

CONTROL REGISTER 2 (CR2)

Auto Flag (CR20) When set, Flags (without INTRQs) will be continuously transmitted in between frames, when otherwise the transmitter would be in idle state.

Self-Test Mode (CR21) When set, the Transmitter Data Output is internally connected to the Receiver Data input circuitry. The modem control output signals are deactivated (off state). The modem control input signals are internally activated. This mode allows off-line diagnostic.

SDLC Loop Mode (CR22) When set, the WD193X is conditioned to operate in an SDLC Loop Data Link system (see SDLC Loop Mode).

Receiver Character Length (CR24, 23) These bits indicate to the receiver how many bits per character there are to assemble for the I-field. The I-field characters may be 5, 6, 7 or 8 bits long. The unused bits read from RHR will be logical 0.

CR24 (RCL1)	CR23 (RCL0)	Bits Per Character
0	0	8
0	1	7
1	0	6
1	1	5

Extended Address (CR25) When set, this bit indicates to the receiver that there is more than one address character in the A-field. The receiver will expect another address character if the LSB in the current address character is a logical 0. The purpose of this bit: If a non-8-bit I-field character length is expected, the DRQIs will get out of synchronization if the WD193X does not know exactly when the I-field will start. Not used in transmit mode.

Address Compare (CR26) When set, the first address character will be inspected in the Address Comparator. If there is a match with the AR register, or if the address compared is a Global Address (eight 1's) the frame is considered valid, causing DRQIs to be generated. Otherwise, the receiver does not react, and will continue comparing for a new valid address. If not set, all frames are considered valid.

Extended Control (CR27) When set, indicates that there are two control characters per frame. If not set, there is only one control character per frame. The purpose of this bit: If a non-8-bit I-field character length is to be received, the DRQIs will get out of synchronization if the WD193X does not know when the I-field will start. Not used in transmit mode.

CR15 (TC1)	CR14 (TC0)	Command	Character/s Transmitted	Signal to CPU
0	0	DATA	Content of THR	DRQO
0	1	ABORT	1111 1111	INTRQ
1	0	FLAG	0111 1110	INTRQ
1	1	FCS	FCS + 01111110	INTRQ

CR32 (TRES 2)	CR31 (TRES 1)	CR30 (TRES 0)	Residual Char. Length
0	0	0	No residual char. sent
0	0	1	1 bit
0	1	0	2 bits
0	1	1	3 bits
1	0	0	4 bits
1	0	1	5 bits
1	1	0	6 bits
1	1	1	7 bits

CONTROL REGISTER (CR3)

***Transmit Residual Character Length (CR32, 31, 30)** These bits inform the transmitter what bit-length the residual character will be. If no residual character is to be sent, these bits must be set to logical 0.

Unused (CR33-37) These bits are not used, and are always a logical 0.

INTERRUPT REGISTER (IR)

This register contains the information why an interrupt (INTRQ) was generated. An IR register read operation, will reset bits 0, and 3-7.

Loading the THR register, will reset DRQO (bit 1). Reading the RHR register, will reset DRQI (bit 2). A new interrupt will occur if one is pending.

If a new interrupt is generated while the CPU is reading the IR register, this new interrupt will set the respective bit in the IR register one bit time later (this to avoid losing any interrupt). The status of bits 3–7 will accumulate until the IR register is read by CPU.

INTRQ (IR0) When set, indicates an interrupt and that there are one or more bits set in positions 3 through 7 of this register. This bit is a mirror image of INTRQ signal (pin 6).

DRQO (IR1) When set, indicates a Data request output. This bit is a mirror image of DRQO signal (pin 18).

DRQI (IR2) When set, indicates a Data Request input. This bit is a mirror image of DRQI signal (pin 19).

Data Set Change (IR3) When set, indicates a change of state of the Data Set (Data Communication Equipment). This is a change of state of $\overline{DSR}$, $\overline{CD}$ or $\overline{RI}$. The type of change of $\overline{CD}$ and $\overline{RI}$ that this bit will react to, is programmed by use of input signals $\overline{CD1}/\overline{CD0}$ and $\overline{RI1}/\overline{RI0}$ and is shown below.

XMIT Operation Complete with Underrun Error (IR4) When set, indicates that the transmitter command has been completed and there was an Underrun error. An Underrun error occurs when the Data Request Output (DRQO) is set, but THR register is not loaded in time.

XMIT Operation with No Error (IR5) When set, indicates that the transmitter command has been completed and there was no error.

Received End of Message With Errors (IR6) When set, indicates that a Received End of Message is detected, and there was an error. Errors include CRC, Overrun, Invalid Frame and Aborted Frame.

The SR Register bits 0–2 will indicate the exact type of error.

Received End Of Message With No Error (IR7) When set, indicates that a Received End of Message is detected, and there was no error.

$\overline{CD1}$	$\overline{CD0}$	Interrupting edge of $\overline{CD}$	$\overline{RI1}$	$\overline{RI0}$	Interrupting edge of $\overline{RI}$
LO	LO	Rising and falling	LO	LO	Rising and falling
LO	HI	Falling	LO	HI	Falling
HI	LO	Rising	HI	LO	Rising
HI	HI	None	HI	HI	None

STATUS REGISTER (SR)

This register contains the status of the receiver and some modem control signals. It also indicates (if REOM w/Errors) exactly what type of errors. If the Receiver Character Length is 8 bits, this register indicates the amount of Residual bits that was received. A read operation will reset bits 0-2.

Received Error/Received Residual Character Length (SR 2-0) If REOM w/NO ERROR (IR7) is set, and the Receiver, Character Length (CR24, 23) is 8 bits, these bits (SR 2-0), indicate the number of residual bits received.

If REOM WITH ERROR (IR 6) is set, these bits indicate the type of error that occurred, as shown in figure below.

Bit Set	Error
SR0	CRC
SR1	Overrun
SR2	Aborted or Invalid frame

Receiver Idle (SR 3) When set, indicates that the receiver is currently IDLE.

Miscellaneous Input (SR4) This is a mirror image of $\overline{\text{MISC}}$ IN signal. When this signal is set, SR4 bit is set.

Data Set Ready (SR5) This is mirror image of $\overline{\text{DSR}}$ signal. When this signal is set, SR5 bit is set.

Carrier Detect (SR6) This is a mirror image of $\overline{\text{CD}}$ signal. When this signal is set, SR6 bit is set.

Ring Indicator (SR7) This is a mirror image of $\overline{\text{RI}}$ signal. When this signal is set, SR7 bit is set.

TRANSMITTER OPERATION

Prior to this operation, the programmable inputs and the transmit mode related register bits need to be programmed according to the user's specific data communications environment. The last bit to be set is always the ACT TRAN (CR16) bit.

Before this, the INTRQ has to be cleared, which can be done by reading the IR register. For more detailed information how to program the WD193X, see Programming.

As an example of how to program the WD193X, let's assume a 24-bit information is to be transmitted. The I-field would then consist of three 8-bit characters with no residual bits. CR3 should then be 00 (Hex).

If Auto Flag is selected, CR20 has to be set, CR21 and CR22 should be logical 0's, as this example is no Self-test and no SDLC Loop Mode.

Bits CR23-CR27 are for reception only (see Receiver Operation). The last register to be programmed is CR1. If MISC OUT is not used, this may be ignored. If a modem is used, DTR (CR11) is to be set. CR13 and CR12 should be logical 0's (8-bit char. length). CR15 and CR14 should be logical 0's (Data Command). ACT TRAN (CR16) bit is to be set. The ACT REC (CR17) is for reception only.

The DTR bit, when set, activates the $\overline{\text{DTR}}$ signal, indicating to the modem to prepare for communication. When the modem is ready, it sends back a Data Set Ready ($\overline{\text{DSR}}$) to the WD1933. This causes the DSC (IR3) bit to set, which in turn activates INTRQ. The IR register is now read. Simultaneously, when the ACT TRAN (CR16) bit is set, this activates the Request to Send ($\overline{\text{RTS}}$) signal, instructing the modem to enter into transmit mode. When the modem is ready to transmit data, it responds by activating the Clear to Send ($\overline{\text{CTS}}$) signal.

The WD193X is now conditioned to transmit. Now DRQO gets set, indicating to the CPU (or DMA) to load the first character (Address) into the THR. When this is done, DRQO will reset. As soon as the WD193X is ready to be loaded with the next character to be transmitted, DRQO is again set. When the THR register is again loaded with a character, DRQO will again reset.

This same sequence continues until the last I-field character to be transmitted is loaded into the THR. If CRC checking is to be used, the next time when DRQO is set, an FCS command has to be programmed. This is accomplished by either setting CR15, 14 to both logical 1's or by activating the $\overline{\text{EOB}}$ signal.

At the end of the FCS being transmitted, INTRQ will set indicating XMIT Operation Complete. The IR register is to be read to find out whether the frame was sent with or without error. Also the FCS Command which was used as described above has to be changed. If CR15, 14 were set, these have to be reset (to Data Command), or if $\overline{\text{EOB}}$ was activated, this signal has to be deactivated. At this same time, the ACT TRAN bit is allowed to be reset, causing the TD output to go idle after the end Flag is sent. If the ACT TRAN bit is kept set, continuous Flags will be sent following the FCS.

If a new frame is to be sent right after this first frame, only one Flag is needed in between frames, meaning the frames have one common Flag character. In this case, the second frame Address character may be loaded at the same time the FCS command is programmed during the first frame. Also, the ACT TRAN bit should be kept set in between frames. Every time DRQO gets set, the user must load the THR register before the last loaded character only has 1.5 bits left to be transmitted. In other words, when DRQO gets set, the user may wait (if 8-bit characters) up to 7.5 serial data bits before loading the THR. If THR is not loaded within this time, an Underrun error will occur.

If Auto Flag is not selected (CR20 = logical 0) the sequence will be a little different than described below. When the first DRQO is set, and after the Address character is loaded into THR, a Flag command is also programmed (CR15, 14 = 10).

This will set an interrupt (INTRQ), which indicates that the IR register must be read. Now, the Data Command is reprogrammed (CR15, 14 =00).

For more information, see Transmission Timing diagram.

ABORT CONDITIONS

The function of prematurely terminating a data link is called an "Abort." The transmitting station aborts by sending eight consecutive 1's. Unintentional Abort caused by 1's in the A-C- or I-field is prevented by zero insertion. Intentional Abort may be sent by programming an Abort command. Abort will also be sent in the case where THR is not loaded in time or FCS command is not programmed in time (= underrun). This means that after the DRQO is set, to avoid Abort; THR must be loaded, $\overline{\text{EOB}}$ activated or FCS command programmed before there is only 1.5 bits left of the last character to be transmitted.

If this is not done, INTRQ (XMIT OPCOM w/underrun) is set and Aborts are transmitted until, either the command is changed or the THR is loaded. If in this same case, Auto

Flag was programmed, one Abort (with INTRQ) would be generated, and thereafter continuous Flags (with no INTRQs) will be sent.

RECEIVER OPERATION

Prior to this operation, the programmable inputs and the receive mode related register bits have to be programmed according to the user's specific data communication environment. Also, the INTRQ has to be cleared. The last bit to be set is always the ACT REC (CR17) bit.

For more detailed information how to program the WD193X see Programming. As an example, let's assume a 26-bit information is to be received, and the I-field is made up by 8-bit characters. The CR3 register is only for transmit mode, and may be ignored here. CR20 and CR 12–16 bits are also for transmit mode only, and therefore may also be ignored. CR21 and CR22 are to be logical 0s (no Self-Test and no SDLC Loop Mode). CR24, 23 are to be logical 0's (8-bit character I-field). If only one A-field and one C-field character is expected, and this WD193X has a specific address, CR25 should be a logical 0, CR26 should be a 1, and CR27 should be a 0. The address to which the A-field should compare should be loaded into the AR register.

The status of the modem is monitored by the SR register, and it may be useful to read it at this time. CR1 is loaded as the last register. CR10 (Misc In) bit is optionable to the user. CR11 (DTR) is to be set if modem is used. CR17 (ACT REC) is now set, starting the input of frame characters into the Receiver Register (RR). When a Flag is detected, the next 8-bit character (address-character), when received, is compared to the character in the AR register. If these match, or if the received character is a Global address, this frame is valid, and the DRQI gets set. If the Address Comparator (CR26) bit is not set, all frames would be considered valid and generate DRQIs. When the RHR register is read, DRQI will be reset. All characters in a valid frame which are input into the RR register will set DRQI, and every time RHR is read by the CPU, DRQI will be reset.

During reception, the receiver also performs a CRC calculation on the incoming data. When the end Flag is received, INTRQ will get set, indicating Received End of Message. If the reception is completed with no error, IR7 (REOM w/no Error) bit will be set. When 8-bit characters are received SR 0-2 bits indicate the number of residual bits, in this case two. If IR6 (REOM w/Error) was set, SR 0-2 bits indicate the type of errors (see Receiver Error Indication).

When all characters including the A-field and the FCS-field are read, and when the REOM interrupt is recognized, it is up to the user to disassemble these mentioned characters from the received data. If non-8-bit characters are received, the amount of residual bits have to be calculated by the CPU after masking out the part of the ending Flag showing up in the last read character.

After end of frame, the receiver begins searching for a new frame.

For more information, see Reception Timing diagram.

RECEIVER ERROR INDICATION

When a frame is received, and REOM w/Error (IR6) is set, the type of error is indicated by the SR bits 0-2.

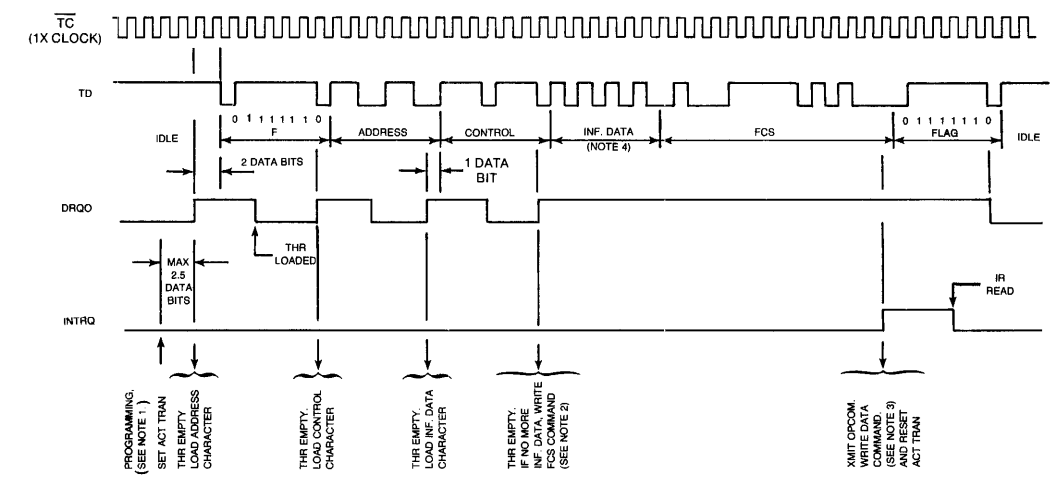
CRC Error (SR0) If the CRC calculation performed on the incoming data does not equal to F0B8 (HEX), this bit will be set.

Overrun Error (SR1) After DRQI is set, if the RHR is not read within one character minus one bit time, this bit will be set.

Aborted or Invalid Frame Error (SR2) If the frame is aborted, or it consists of less than 32 bits between flags, this bit will be set.

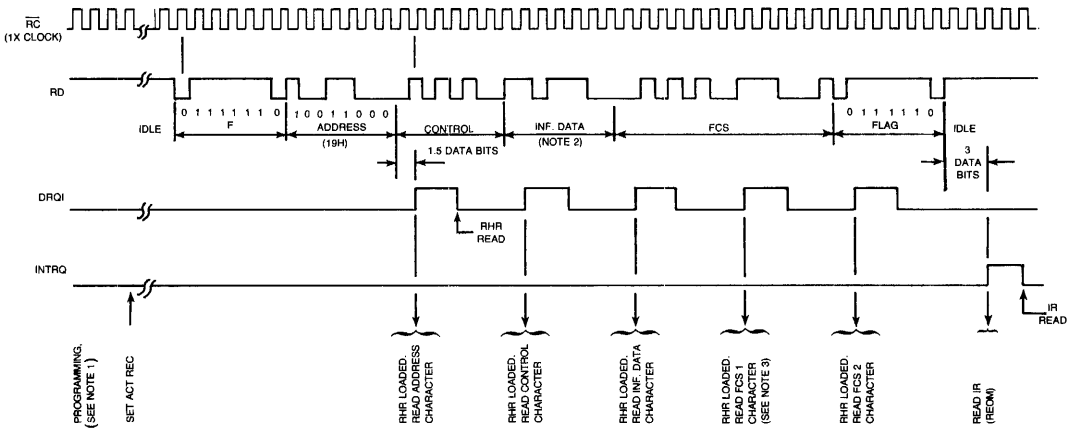
NOTES

1. TC-command—If two or more contiguous ABORTS or FLAGS are executed, the ACT TRAN (CR16) bit has to be reset before DATA-command can be executed.
2. Master Reset ($\overline{MR}$)—Needs no clock during activation of MR. However, 2.5 clock cycles are required to reset the WD193X after the falling edge of MR.
3. IR-register—Immediately when IR register is read, bit 0 will reset. Bits 3-7 are reset one bit time later.
4. SR-register—Bits 0-2 are reset one bit time after SR register is read.
5. SDLC Loop mode—Go-ahead pattern may be sent by either sending IDLE or ABORT after Flag.
6. $\overline{TC}$ and $\overline{RC}$ clocks are completely independent of each other.
7. It is recommended to verify that the INTRQ signal (pin 6) is set prior to reading the IR register.



NOTE 1. CR3 = 00H, CR2 = O1H, CR1 = 02H (FOR THIS EXAMPLE ONLY)
NOTE 2. WRITE FCS COMMAND, OR ACTIVATE $\overline{EOB}$.
NOTE 3. WRITE DATA COMMAND, OR DEACTIVATE $\overline{EOB}$.
NOTE 4. INF. DATA MAY CONSIST OF ANY NUMBER OF BITS.

Figure 8. WD193X TRANSMISSION TIMING DIAGRAM



NOTE 1. AR = 19H, CR2 = 40H, CR1 = 02H (FOR THIS EXAMPLE ONLY)
NOTE 2. INF. DATA (I-FIELD) MAY CONSIST OF ANY AMOUNT OF BITS.
NOTE 3. CPU DOES NOT KNOW UNTIL RECEIVED END OF MESSAGE (REOM) THAT THIS IS AN FCS CHARACTER.

Figure 9. WD193X RECEPTION TIMING DIAGRAM

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Storage Temperature	−55°C to +125°C (plastic package)
Storage Temperature	−65°C to +150°C (ceramic package)
Voltage on any pin with respect to GND (V_{SS})	−0.3 to +7.0V
Power Dissipation	1W

DC Characteristics

T_A = 0°C to +70°
V_{SS} = 0V, V_{CC} = +5 ± 0.25V

Table 3. WD193X DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{LI}	Input Leakage			10	μA	VIN = V_{CC}
I_{LO}	Output Leakage			10	μA	V_{OUT} = V_{CC} or V_{SS}
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage			0.8	V	All Inputs
V_{OH}	Output High Voltage	2.4			V	I_O = −100μA
V_{OL}	Output Low Voltage			0.4	V	I_O = 1.6mA
I_{CC}	Supply Current		70	210	ma	

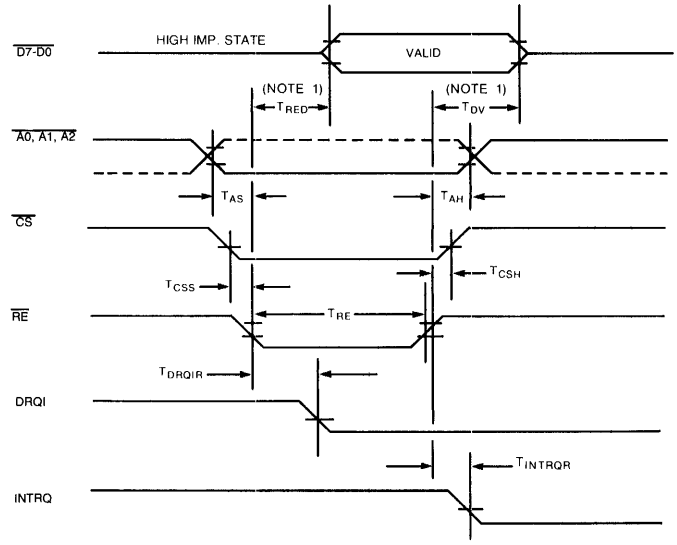
AC Characteristics

T_A = 0°C to +70°
V_{SS} = 0V, V_{CC} = +5 ± 0.25V

Table 4. WD193X AC CHARACTERISTICS

		−00,	−10	−01,	−11	−02,	−12	−03,	−13		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Units	Conditions
	READ & WRITE										
T_{AS}	Address Set-Up	20		20		20		20		ns	
T_{AH}	Address Hold	20		20		20		20		ns	
T_{CSS}	Chip Select Set-up	20		20		20		20		ns	
T_{CSH}	Chip Select Hold	20		20		20		20		ns	
	READ										
T_{RED}	Data Delay from $\overline{RE}$		315		290		265		240	ns	
T_{DV}	Data Valid from $\overline{RE}$	0	140	0	140	0	140	0	140	ns	
T_{DRQIR}	DRQI Reset Delay		280			280			280	ns	
T_{INTRQR}	INTRQ Reset Delay		280		280		280		280	ns	
T_{RE}	$\overline{RE}$ Pulse width	325		300		275		250		ns	
	WRITE										
T_{DS}	Data Set-up	200		180		160		140		ns	
T_{DH}	Data Hold	20		20		20		20		ns	
T_{DRQOR}	DRQO Reset Delay		330		330		330		330	ns	
T_{WE}	$\overline{WE}$ Pulse width	200		180		160		140			
	CLOCK										
$1xF_C$	1X Clock		.5		1.0		1.5		2.0	MH_Z	at 50% duty cycle
$32xF_C$	32X Clock		1.0		1.5		2.0		2.5	MH_Z	at 50% duty cycle
	RISE & FALL										
T_R	Rise Time		20		20		20		20	ns	See figure 1
T_F	Fall Time		20		20		20		20	ns	

NOTE: All A.C. Timing Measurements made at 0.8V and 193X .



NOTE 1. T_{RED} and T_{DV} starts from where both $\overline{CS}$ and $\overline{RE}$ are active.

Figure 10. WD193X READ TIMING DIAGRAM

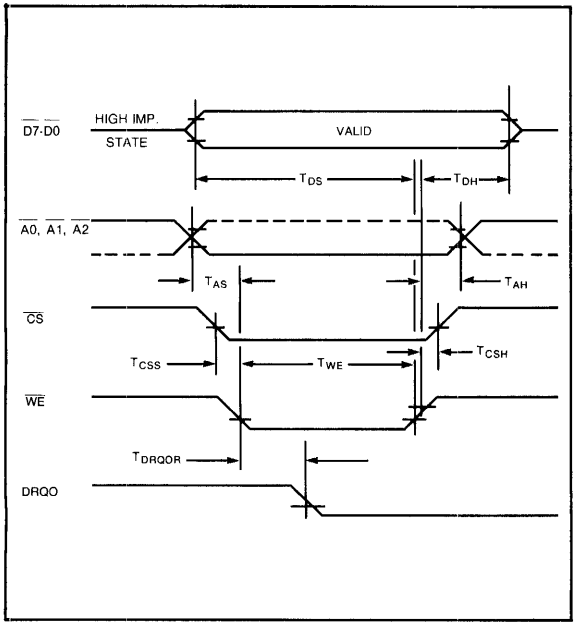


Figure 11. WD193X WRITE TIMING DIAGRAM

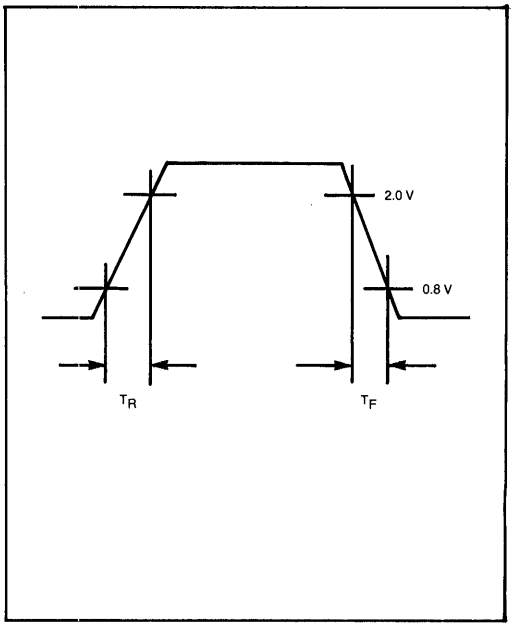


Figure 12. WD193X RISE AND FALL TIMING DIAGRAM

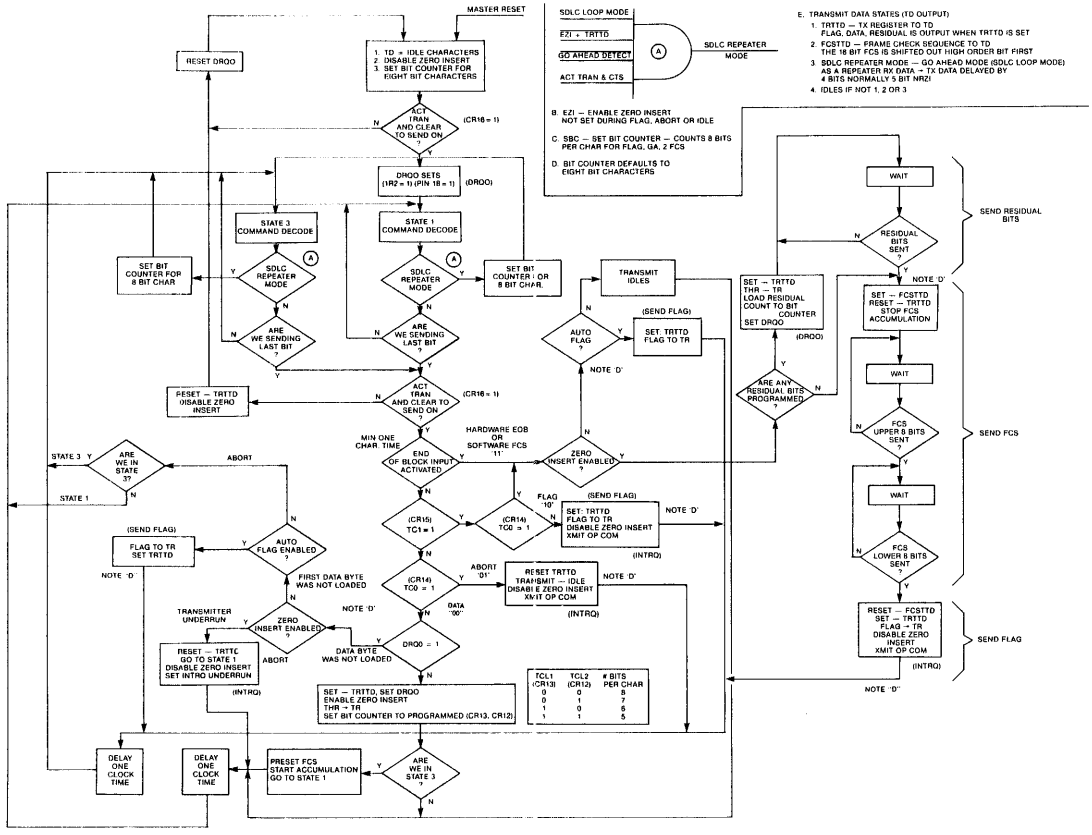


Figure 13. WD193X TRANSMITTER FLOW CHART

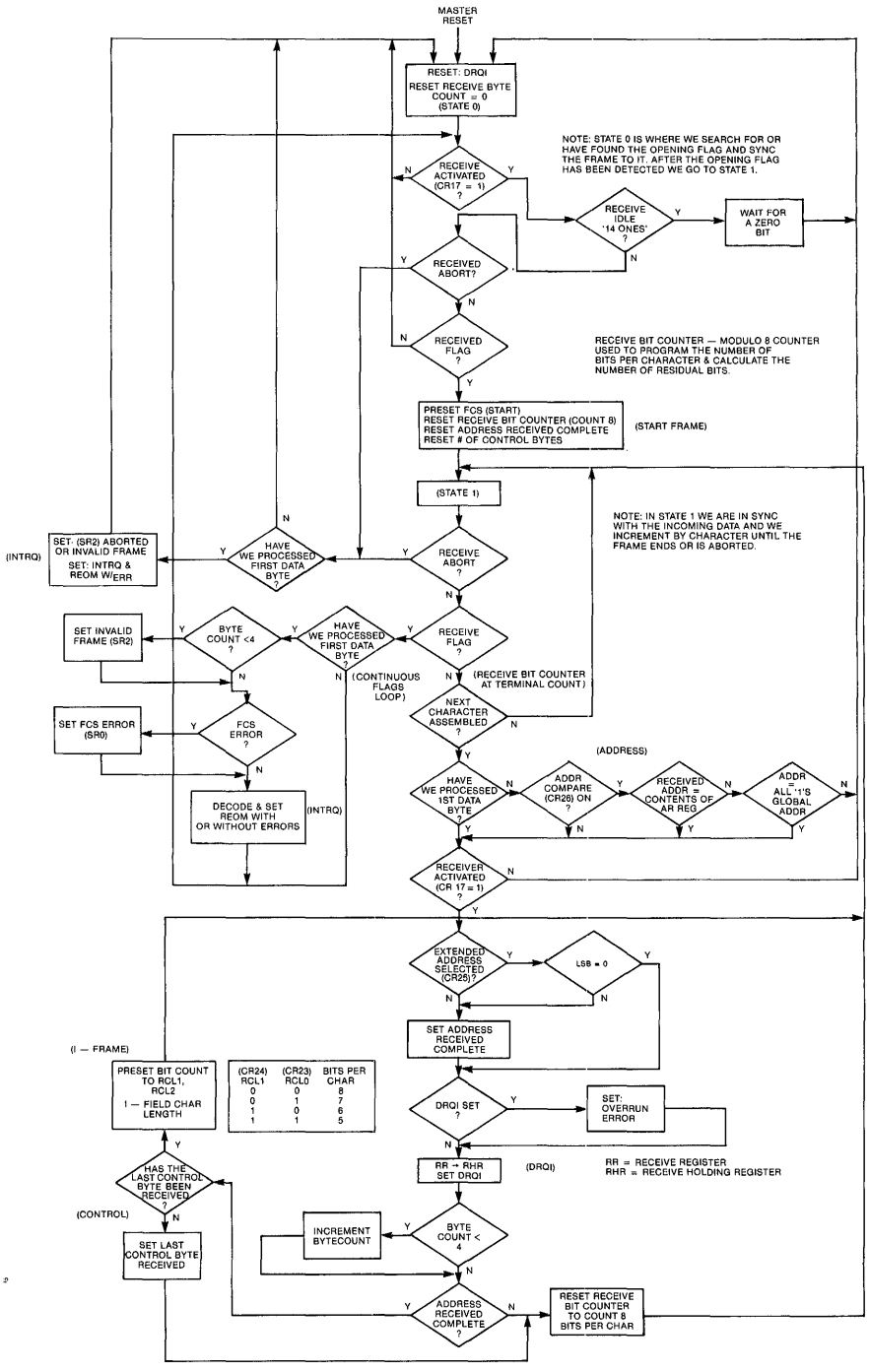


Figure 14. WD193X RECEIVER FLOW CHART

ORDERING INFORMATION

Table 5. WD193X ORDERING INFORMATION

Part No.	Loop Mode	Maximum Data Rate	Temp. Range
WD193X*-00	no	500KBPS	0°C to +70°C
WD193X*-10	yes	500KBPS	0°C to +70°C
WD193X*-01	no	1.0MBPS	0°C to +70°C
WD193X*-11	yes	1.0MBPS	0°C to +70°C
WD193X*-02	no	1.5MBPS	0°C to +70°C
WD193X*-12	yes	1.5MBPS	0°C to +70°C
WD193X*-03	no	2.0MBPS	0°C to +70°C
WD193X*-13	yes	2.0MBPS	0°C to +70°C

* Please contact your local Western Digital Sales Representative for package availability and price information.

See page 725 for ordering information.

Printed in U.S.A.

WD1931/WD1933 Compatibility Application Notes

INTRODUCTION

The purpose of this document is to provide the reader with information about the WD1931 and WD1933 devices, and how to take advantage of their compatibility. Various applications examples are given showing flowcharts and timing diagrams. As the devices are designed for use in a very large range of applications, many different features are described and illustrated for the benefit of the reader.

For detailed product information such as A.C. and D.C. parameters, please refer to the respective data sheets.

GENERAL DESCRIPTION

The WD1931 and the WD1933 are MOS/LSI devices which interface a parallel digital system to a serial data communication channel (and vice versa). Both circuits are capable of simplex, half duplex, and full duplex operation.

The WD1931 is designed for character-oriented asynchronous and/or synchronous (BI-SYNC) protocols. The WD1933 is designed for bit-oriented SDLC, HDLC and ADCCP protocols. The devices are programmable and compatible to most 8-bit microcomputers on the market. The pin assignments of these two devices have been chosen to allow the user to implement a one-board multiprotocol design. This board may then be used for any of the above mentioned protocols, by choosing the proper device (WD1931 or WD1933) and connecting some jumpers (see paragraph entitled "Multiprotocol Board Design"). The purpose of these circuits are to convert parallel data from a computer or terminal to a serial data stream at one end of a communication channel. At the other end of the channel, the data is converted back to the original parallel data.

Serial data communications minimizes the number of physical channels required to transfer data and therefore reduces the cost to send data between two (or more) distant points. A microcomputer could perform the same serial/parallel conversion function as these devices, but at much slower speeds. However, using the WD1931 and WD1933 devices to do this function is much more efficient. This makes the computer free to perform other tasks during transmission and reception. The only work that the computer is required to do is to initialize and write data characters to/from the WD1931 or WD1933. These devices will take care of the serialization or deserialization of this data, plus control and timing.

Some control signals on the computer side of the devices are needed for read, write, and control purposes. Additional signals can also be used for special purposes or modes for the convenience of the user. Typically, these other control signals are used to enable communication with a modem or DCE (Data Communications Equipment).

Interrupt outputs are provided to inform the microcomputer when to retrieve from, or to provide data to the holding registers. Also, interrupts can be generated to provide status information such as changes in modem control lines, or that events such as Transmission Complete or Received End of Message have occurred.

SYSTEM APPLICATIONS

WD1931/33 may be used in the following applications:
Switched network
Multipoint network
Non-switched point to point network
Simplex, half-duplex, or full duplex
Asynchronous or synchronous communication
Message switching
Multiplexing systems
Data concentrator systems
Loop data link systems
DMA applications
Parallel to serial data conversion (and vice versa)
Local Networks
Packet Switching
X.25
Multidrop line systems

A typical block diagram of a data link is shown in Figure 1. The communication media used could be a direct communication channel (such as a leased telephone line), a switched telephone line, or one of many other possibilities. Typically these applications would require the use of a modem.

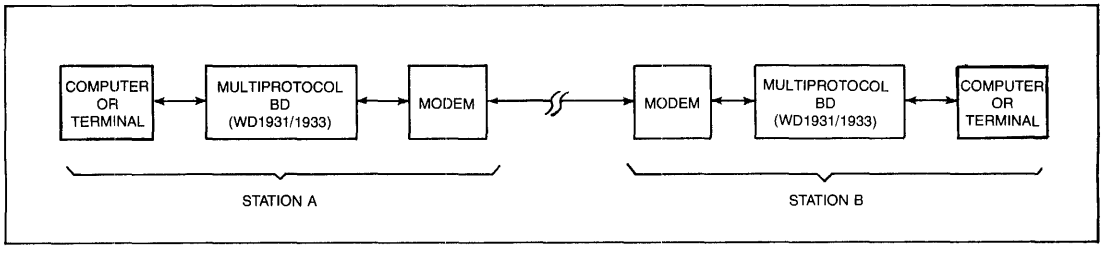


Figure 1. DATA LINK BLOCK DIAGRAM

The applications that these devices could be used in would be a combination of the previously mentioned. A modem would be needed for long distance communication lines. For shorter distance, line drivers/receivers may be sufficient. In some very well controlled environments, such as a laboratory, two devices may be connected without line drivers and receivers.

The WD1931 or WD1933 may be connected directly to a microcomputer bus, but buffers would normally be recommended. Figure 2 shows a typical schematic of an interface between a Z80 microcomputer and a modem. This is called a multiprotocol board, which is described later in this document.

Some examples of various WD1931/WD1933 systems are shown here by use of block diagrams. The station shown in Figure 3 consists of a computer or terminal, a multiprotocol board, and a modem. A station may consist of only the computer or terminal, and one WD1931 or WD1933 device. Whether the modem, line drivers and receivers, or CPU buffers are needed depends on the details of the particular design situation.

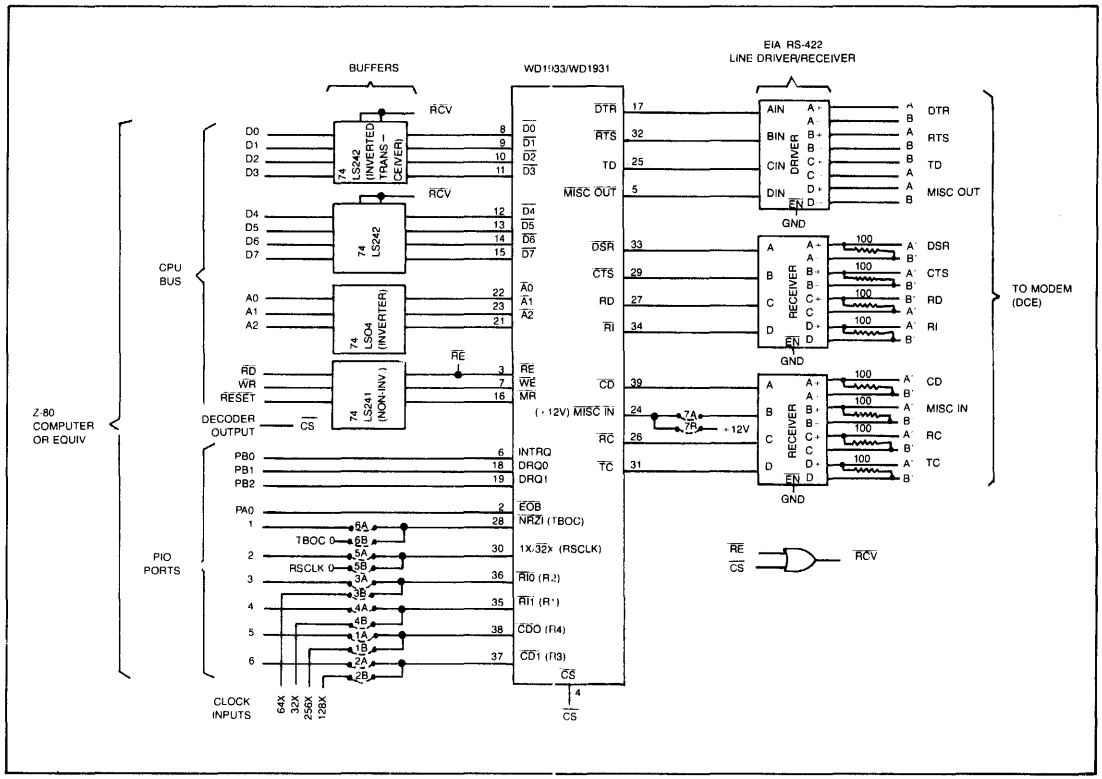
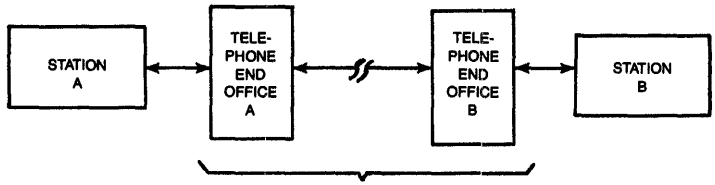
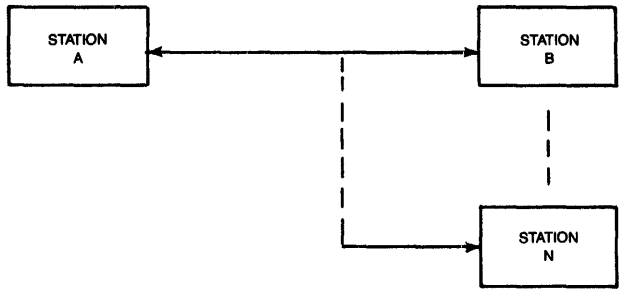


Figure 2. WD1931/1933 AND MICROCOMPUTER. (MULTIPROTOCOL BOARD)



SWITCHED NETWORK



MULTIPOINT NETWORK

NONSWITCHED POINT TO POINT NETWORK

Figure 3. TYPICAL NETWORKS

LOOP DATA LINK SYSTEM

The Loop Mode is used in SDLC only. A loop data link system consists of one primary station (Loop Controller), and a number of secondary stations all functioning normally as repeaters. Figure 4 illustrates a typical Loop Data Link system.

Any secondary station finding its address in the address field captures the frame for action at that station. All received frames are relayed to the next station down the loop.

A secondary station is allowed to suspend the repeater function and initiate its transmission when a Go-Ahead pattern is received.

DATA COMMUNICATIONS EXAMPLE NO. 1

The diagrams below (Figures 5 and 6) illustrate a typical digital system employing several processing levels and digital communications protocols. It is flexible enough to satisfy several applications. For example, the host processor and remote terminals could be located in airline reservation offices and ticket counters, travel centers and travel agencies, central bank offices and branch banks, or department stores and individual cash registers. The exploded diagram of the Data Communications Controller exemplifies the use of one common circuit board design with eight multiprotocol circuits. When one port requires a character-oriented protocol (asynchronous, character oriented synchronous, or bisync), the WD1931 is installed into the appropriate socket. For SDLC, HDLC or ADCCP, the WD1933 is used.

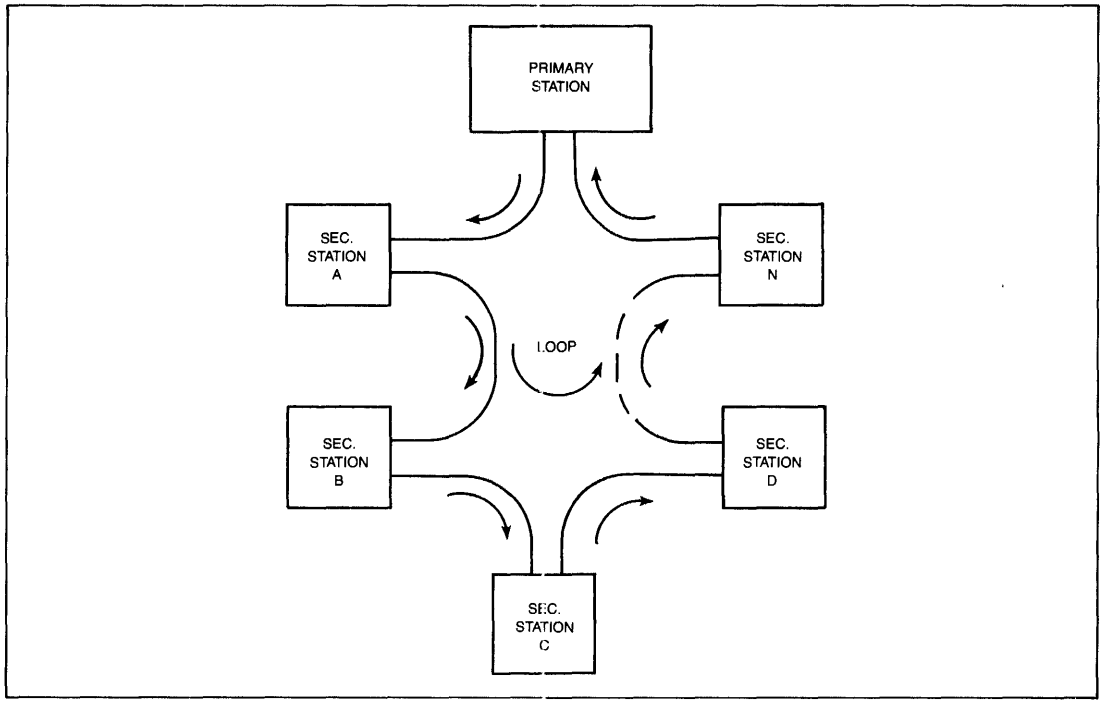


Figure 4. LOOP DATA LINK SYSTEM

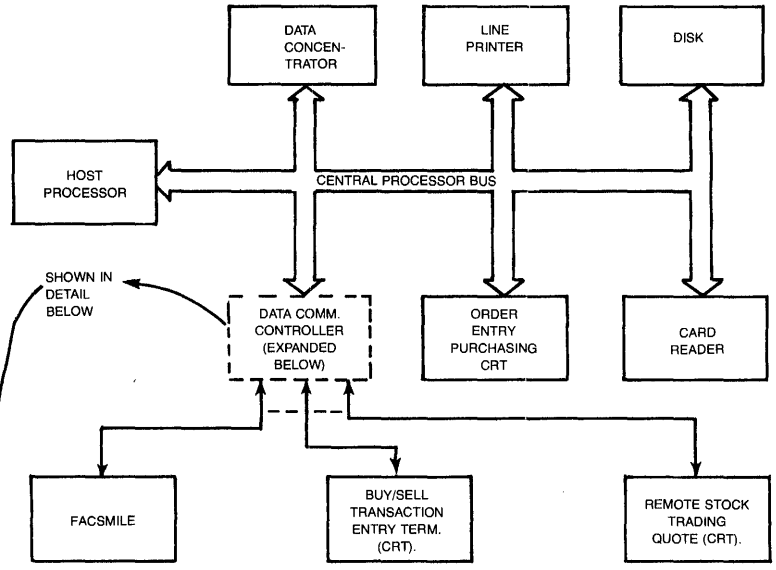


Figure 5. STOCK BROKERAGE SYSTEM

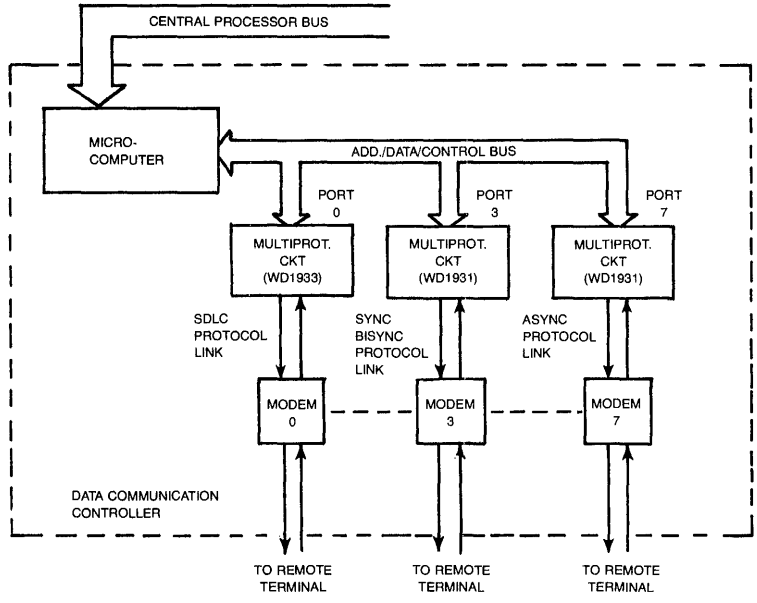


Figure 6. DATA COMMUNICATION CONTROLLER

DATA COMMUNICATIONS EXAMPLE NO. 2

Figure 7 illustrates a Host Computer that communicates through modems to a multiprotocol board. This in turn collects information from many remote stations through a Data Concentrator.

DATA COMMUNICATIONS EXAMPLE NO. 3

A simplified HDLC point to point connection is shown in Figure 8. In this example, no buffers or line drivers and receivers are used.

Figure 9 represents a more "real world" application with the use of modems through a communications channel.

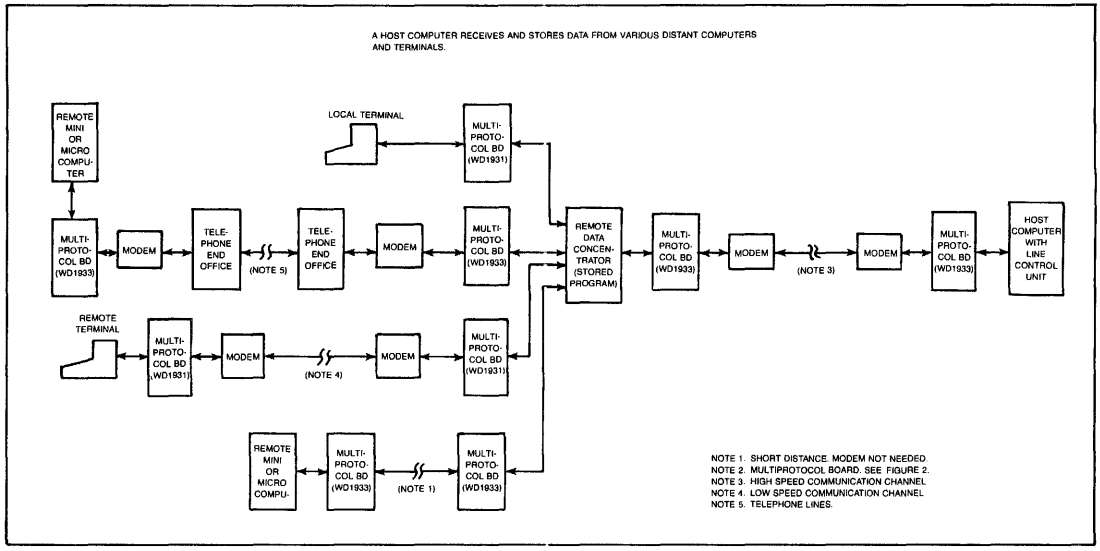


Figure 7. DATA CONCENTRATOR

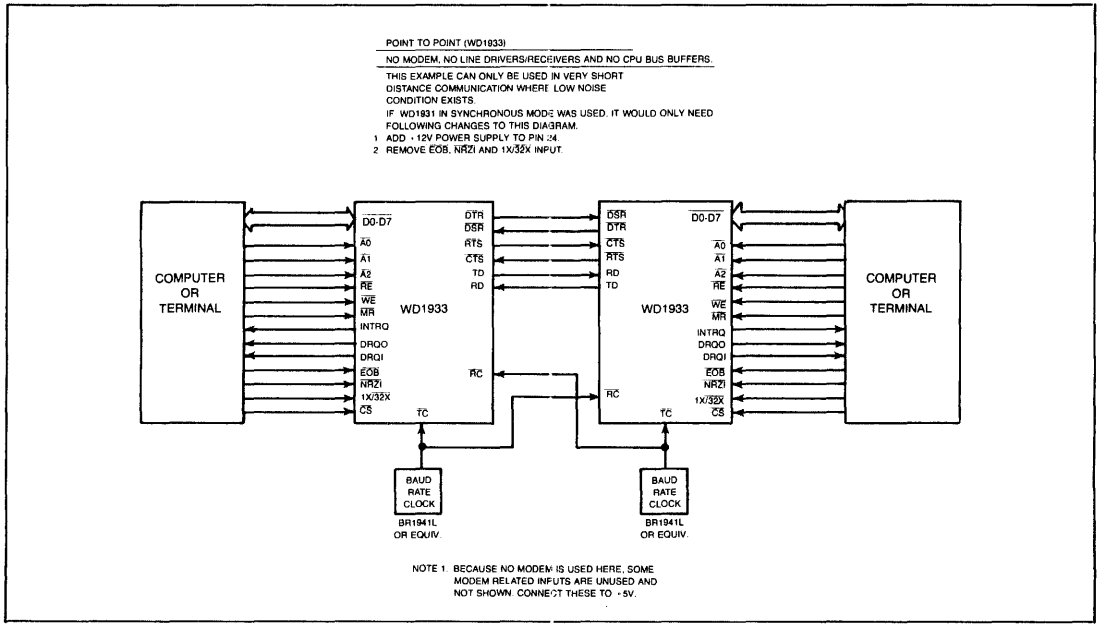


Figure 8. HDLC POINT TO POINT

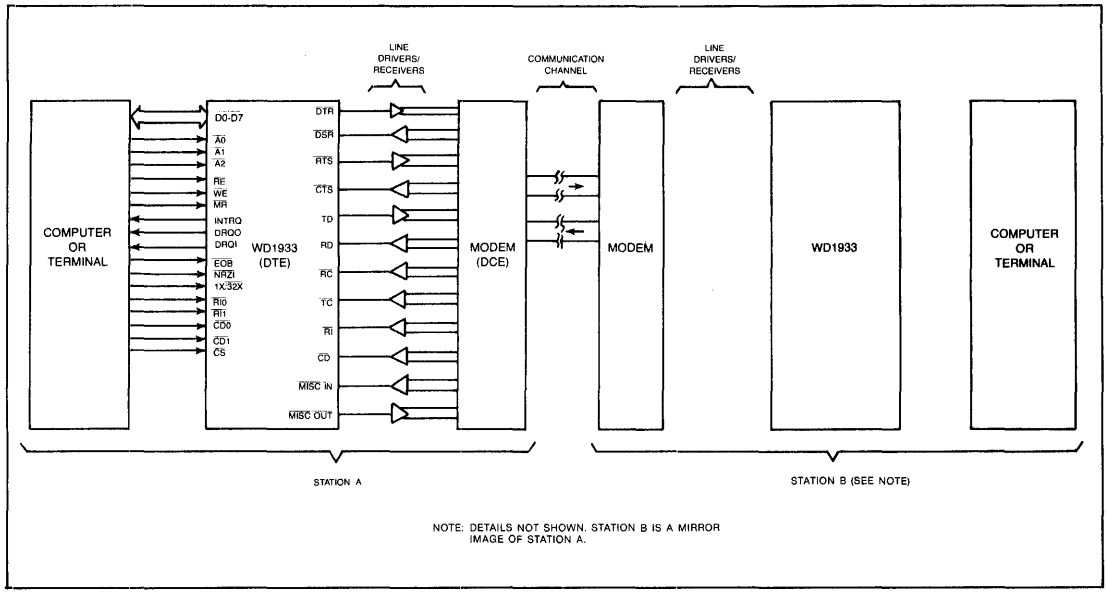


Figure 9. HDLC POINT TO POINT WITH MODEM

WD1931 AND WD1933 TECHNICAL DESCRIPTIONS

The WD1931 and WD1933 devices have been designed to provide a high degree of compatibility and interchangability. The pin-outs are similar, and the register operations are software compatible. This feature allows for the use of either device in a given socket.

WD1931 PIN-OUTS AND BLOCK DIAGRAM

The WD1931 pin assignments and the block diagram are shown in Figure 10.

WD1933 PIN-OUTS AND BLOCK DIAGRAM

The WD1933 pin assignments and the block diagram are shown in Figure 11.

SHORT FORM REGISTER FORMAT AND ADDRESSING

Information concerning operating modes and status conditions are passed to and from the WD1931 or WD1933 device through I/O addressable registers. Each register contains eight bits, where each bit represents a specific function and has its own mnemonics.

The state of each bit is represented by a "1" for TRUE and a "0" for FALSE. This may or may not correlate to a measurable voltage level at a pin, since some pins are TRUE when they are at 0 volts (this is indicated by a bar over the name, or a slash immediately preceeding the name).

The WD1931 registers are shown in Figure 12. Note that some bits are affected by the transmit clock ($\overline{TC}$) rate or the receive clock ($\overline{RC}$) rate.

The WD1933 registers are shown in Figure 13. Note that some bits are affected by the transmit clock ($\overline{TC}$) rate or the receive clock ($\overline{RC}$) rate.

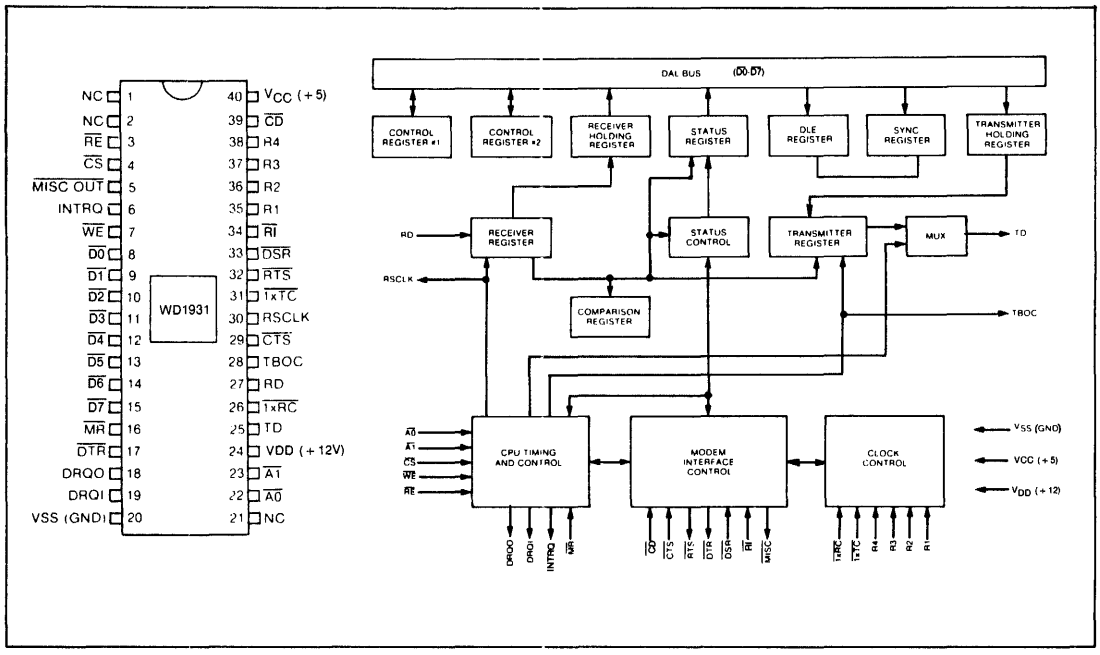


Figure 10. WD1931 PIN CONNECTIONS AND BLOCK DIAGRAM

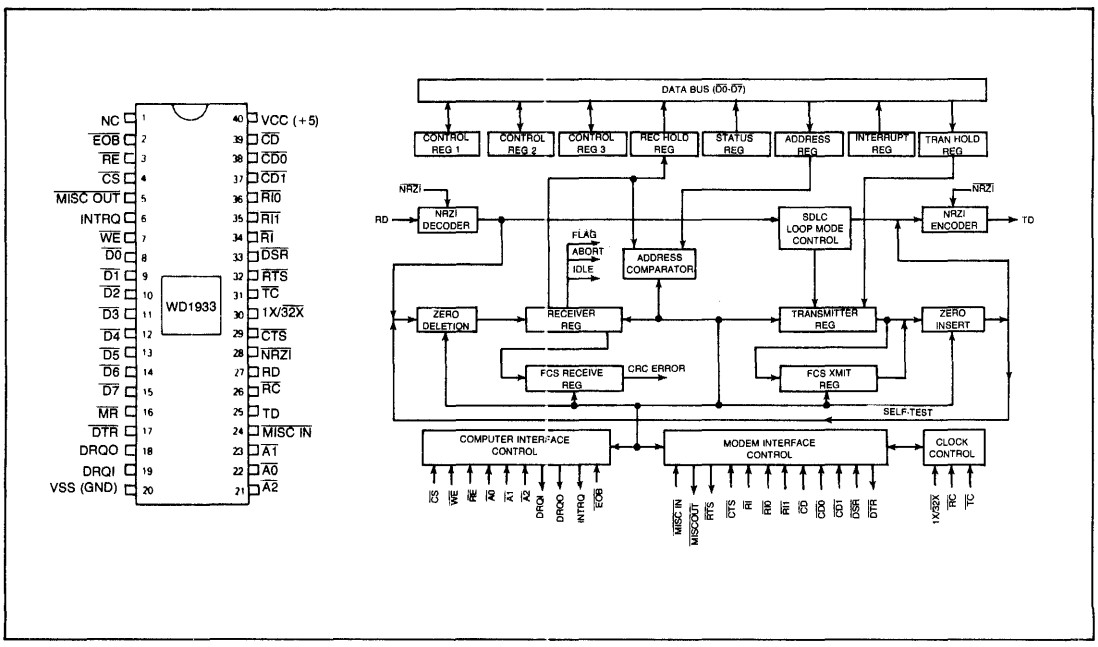
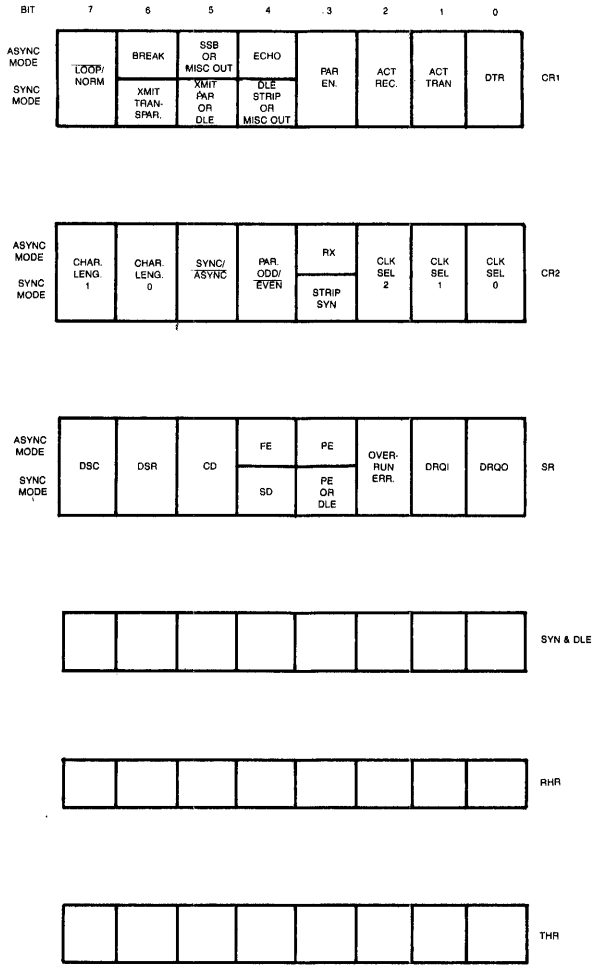


Figure 11. WD1933 PIN CONNECTIONS AND BLOCK DIAGRAM

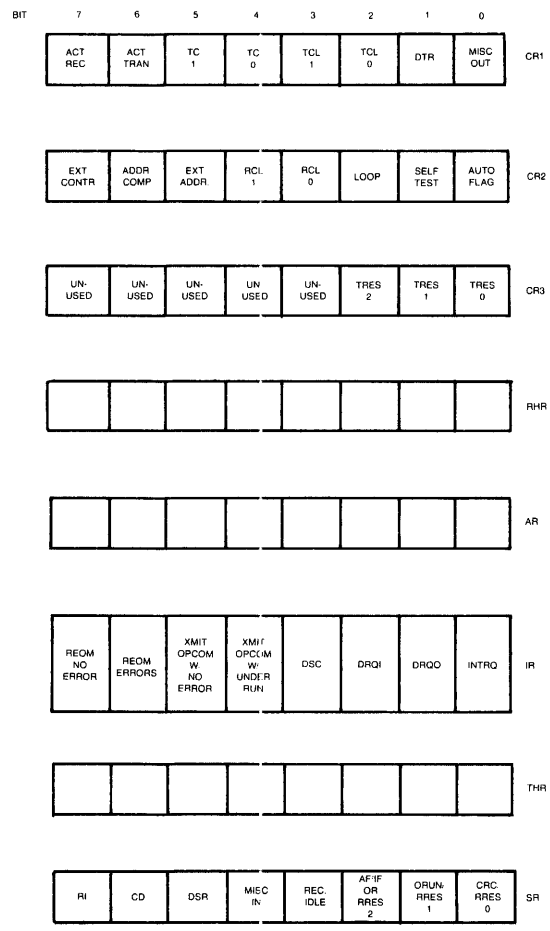


WD1931 BIT ASSIGNMENTS

$\overline{A1}$	$\overline{A0}$	READ	WRITE	CLOCK
LO	LO	CR1	CR1	NONE
LO	HI	CR2	CR2	NONE
HI	LO	SR	SYN & DLE	SR0 = $\overline{TC}$. SR1-4 = $\overline{RC}$. SR5-7, SYN, DLE = NONE
HI	HI	RHR	THR	RHR = $\overline{RC}$. THR = NONE

WD1931 REG. ADDRESSES AND CLOCKS

Figure 12. WD1931 REGISTERS



WD1933 BIT ASSIGNMENTS

$\overline{A2}$	$\overline{A1}$	$\overline{A0}$	READ	WRITE	CLOCK
HI	HI	HI	CR1	CR1	NONE*
HI	HI	LO	CR2	CR2	NONE*
HI	LO	HI	CR3	CR3	NONE*
HI	LO	LO	RHR	AR	RHR = $\overline{RC}$. AR = NONE
LO	HI	HI	IR	THR	IR = $\overline{TC}$. THR = NONE
LO	HI	LO	SR	—	SR0-3 = $\overline{RC}$. SR4-7 = NONE

*After a master reset operation, 2.5 TC clock cycles are required.

WD1933 ADDRESSES AND CLOCKS

Figure 13. WD1933 REGISTERS

MULTIPROTOCOL BOARD DESIGN

The WD1931 and WD1933 pin assignments were chosen so that a circuit board designer may use only one 40-pin socket, but have the choice of using either device on that board. Depending on the application, a few jumper wires may be needed, or perhaps none at all. Figure 2 shows a typical example of a multiprotocol board. This board may be designed with even less components and jumpers, dependent on the particular application it is intended for.

Jumpers 1A-7A are to be connected when WD1933 and all its options are used. Jumpers 1B-7B are to be connected when WD1931 and all its options are used.

For example, if the user does not need the NRZI signal mode, the 1X clock is only used, no Ring or Carrier Detect indication is needed, TBOC, RSCLK and MISC IN are not used, and then no jumpers are needed in the design. In this case, pin 24 may be permanently connected to +12V. Pins 28 and 30 may be connected to +5V via a 10K resistor, and pins 35 through 38 may be connected directly to +5V.

TRANSMISSION EXAMPLE 1 (ONE FRAME)

A typical sequence of events is shown here to transmit a message from computer A to another computer (or terminal) B through a switched network. The message to be sent is a synchronous SDLC protocol frame as shown below in Figure 14. For simplicity, the message sent in this example is very straightforward and short.

Line drivers and receivers are used, permitting transmission to a remote DCE or modem (see schematic in Figure 2). As the SDLC frame is sent, the WD1933 is used. The jumpers required are 1A-7A. Figure 15 illustrates the functional flow, and Figure 16 details the timing of the transmitted frame. Note that the device can be programmed in several different ways to allow for various requirements.

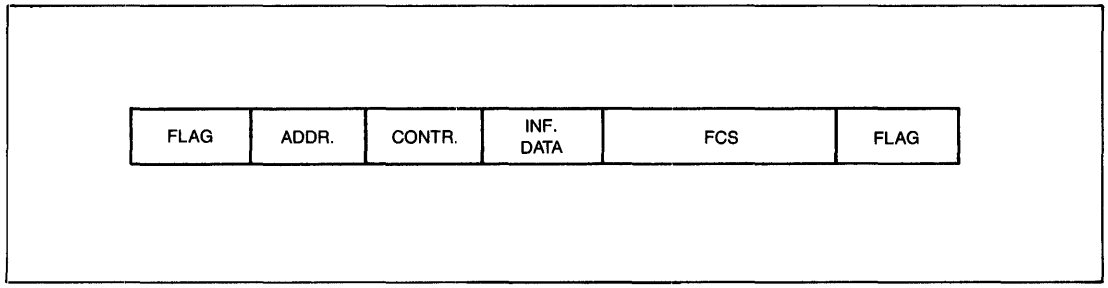


Figure 14. SDLC FRAME FORMAT

INTERRUPT MODE
AUTO FLAG
INF. DATA = 8 BITS (8-BIT CHARACTER WITH NO RESIDUAL BITS)
TC COMMAND IS USED TO INITIATE FCS.

INITIATE
TRANSMIT MODE

DTE AND DCE IDLE

PORT A = OUTPUT
PORT B = INTERRUPT INPUT

AUTO FLAG
DATA TERM. READY

COMPUTER DOING OTHER TASKS

DATA SET READY

INTERRUPT NO. 1

DATA SET CHANGE

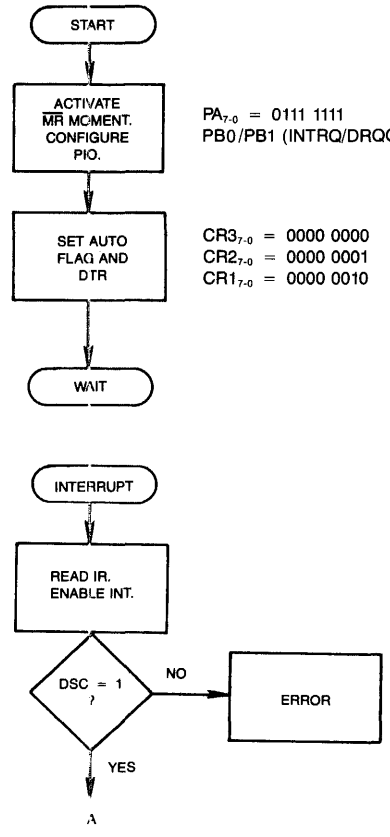


Figure 15. FLOW DIAGRAM OF FRAME TRANSMISSION

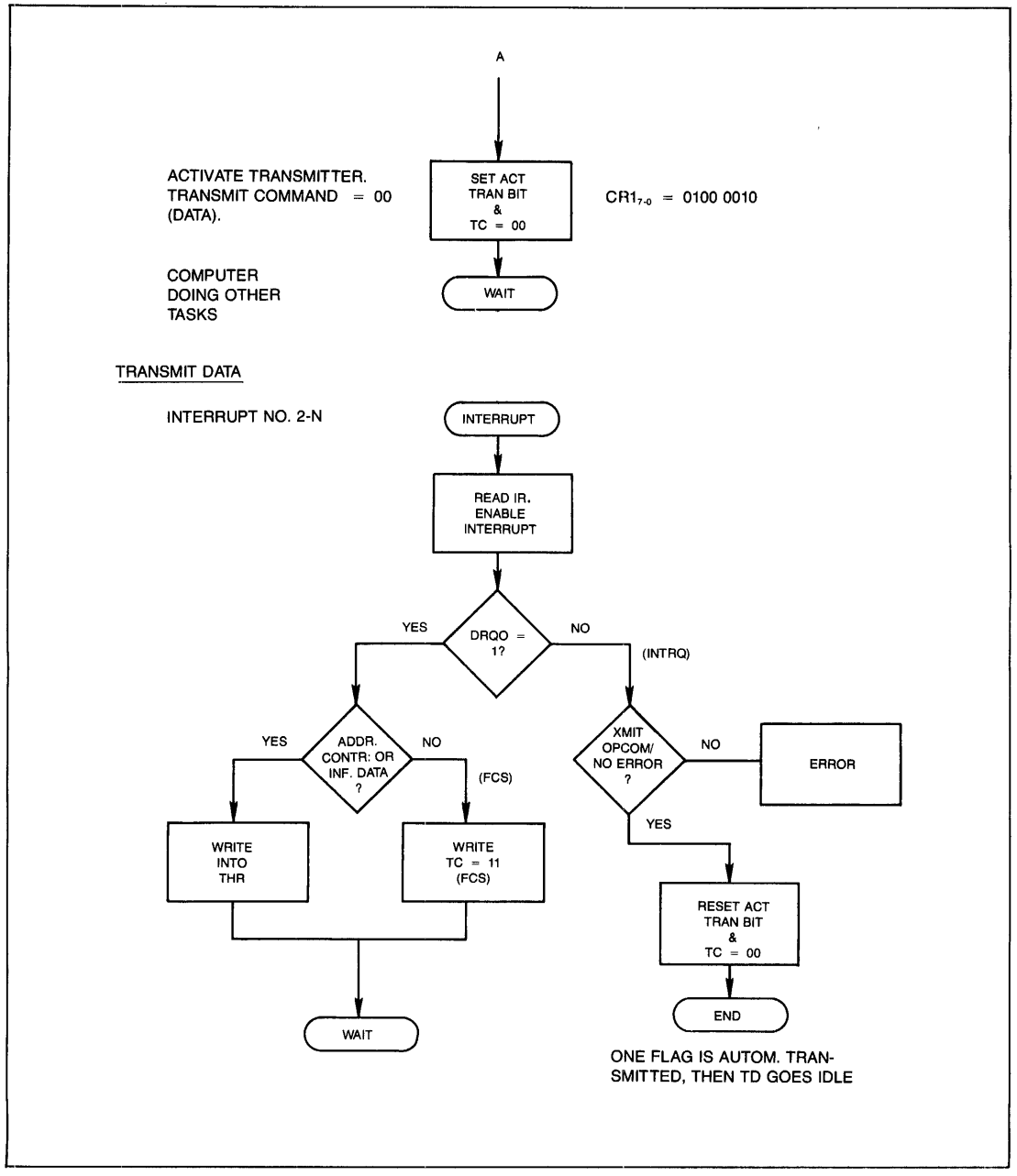


Figure 15. FLOW DIAGRAM OF FRAME TRANSMISSION

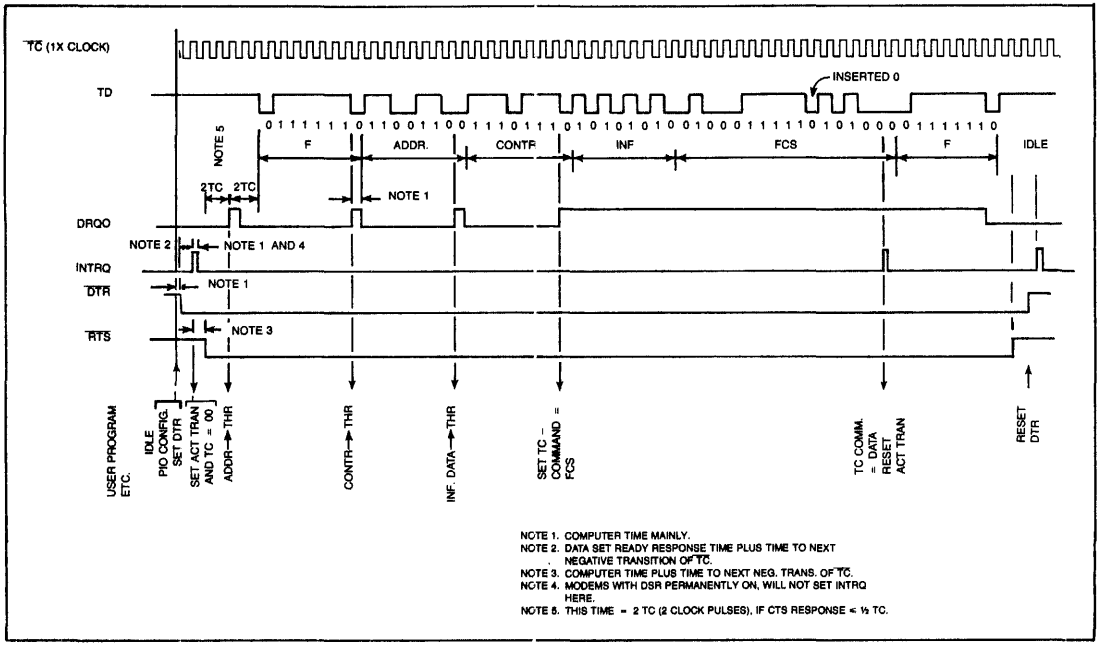


Figure 16. TIMING DIAGRAM OF FRAME TRANSMISSION

WD1933 TRANSMISSION EXAMPLE 2 (DMA APPLICATION)

The WD1933 is very efficient for DMA applications. The control registers are loaded to initiate the WD1933 for DMA mode in the same way as in Transmission Example 1. The Auto Flag bit is set, and the Transmitter Command is "DATA" (CR14 and CR15 bits = 00). The procedure to set up the link (initiate transmit mode and data set ready) is the same as in Transmission Example 1. When INTRQ is set and the Transmitter is activated, the DMA Controller Board takes over the control. From this time on, the DMA Controller Board responds on every DRQO (Data Request Out). When the last character is transmitted and the INTRQ is received, the control is switched back over to the CPU.

A very important feature of the WD1933 is the EOB (End of Block) input. Instead of using the normal (time-consuming) method of writing into a control register to start the FCS (Frame Check Sequence), the $\overline{EOB}$ input is activated at this time. At the next occurrence of INTRQ, the $\overline{EOB}$ signal is deactivated.

An example of a schematic/block diagram is shown in Figure 17, and a timing diagram is shown in Figures 18 through 20.

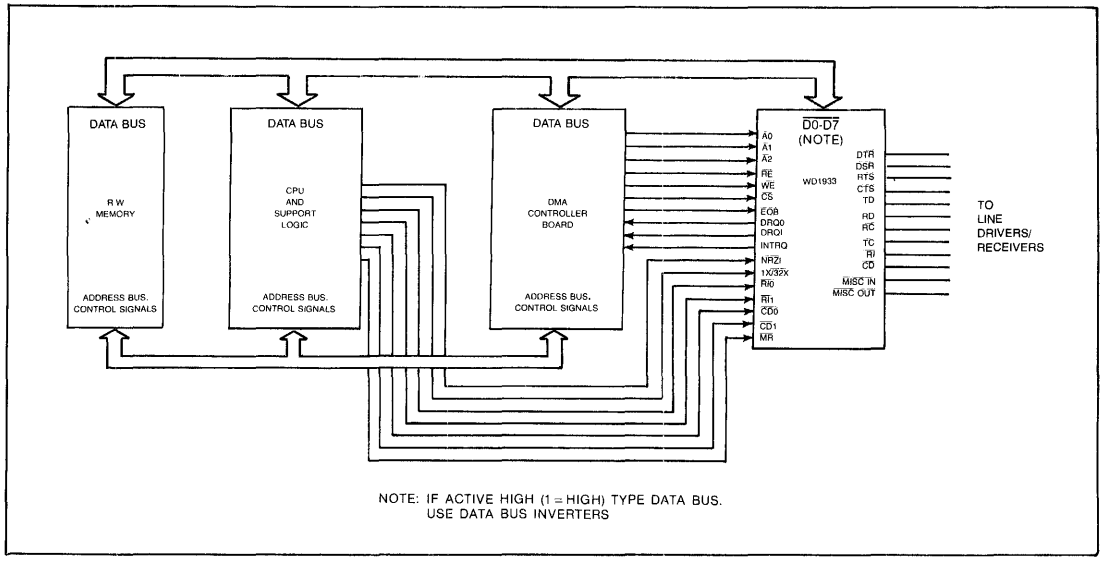


Figure 17. BLOCK DIAGRAM OF DMA APPLICATION

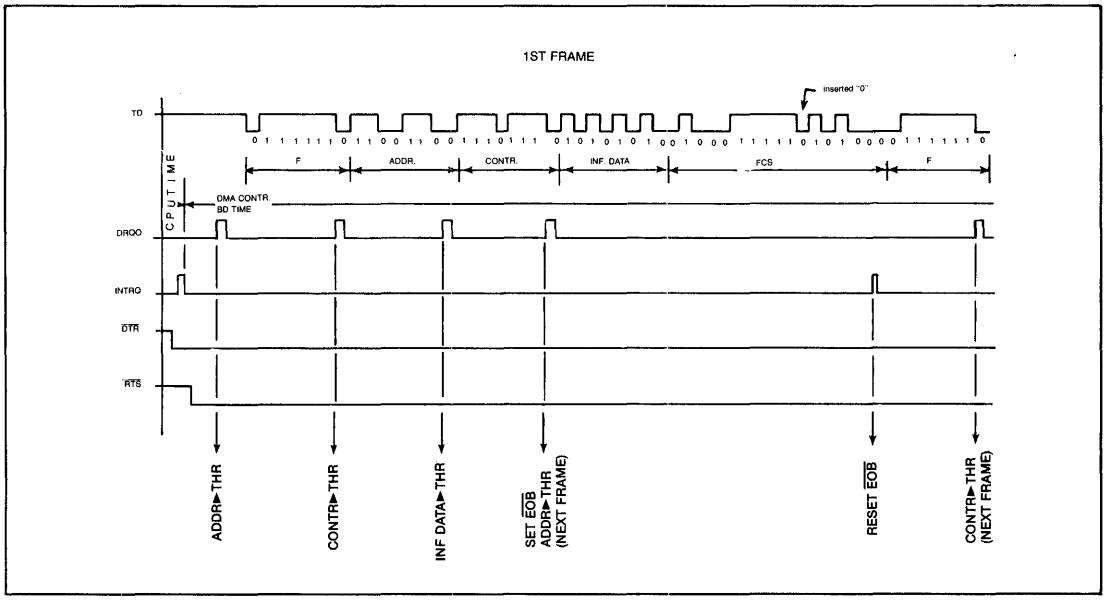


Figure 18. DMA TIMING OF FIRST FRAME

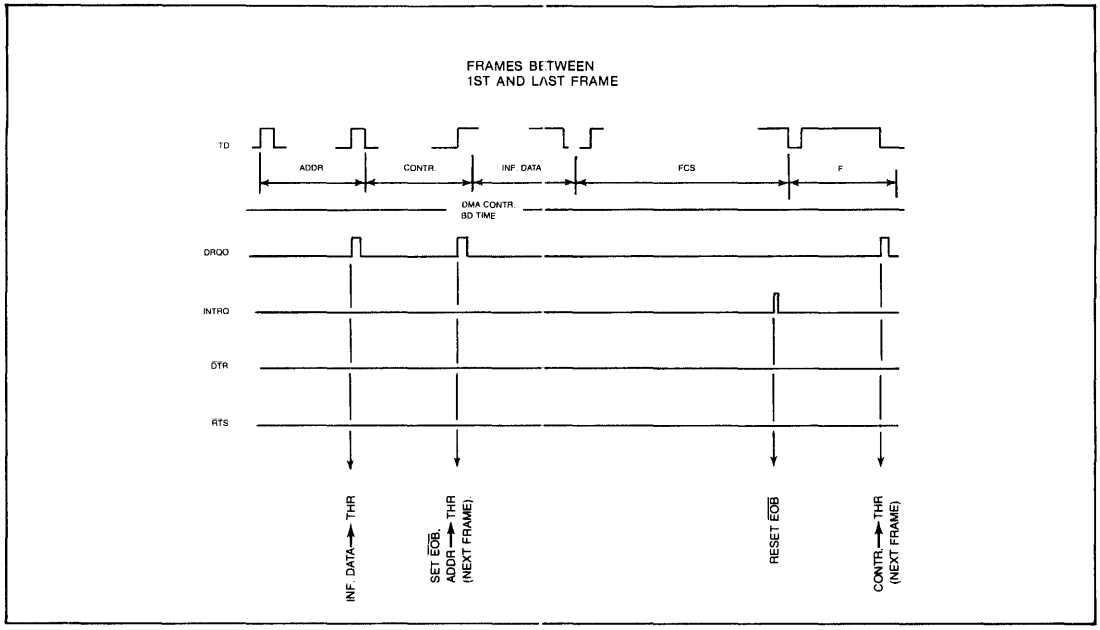


Figure 19. DMA TIMING OF MIDDLE FRAMES

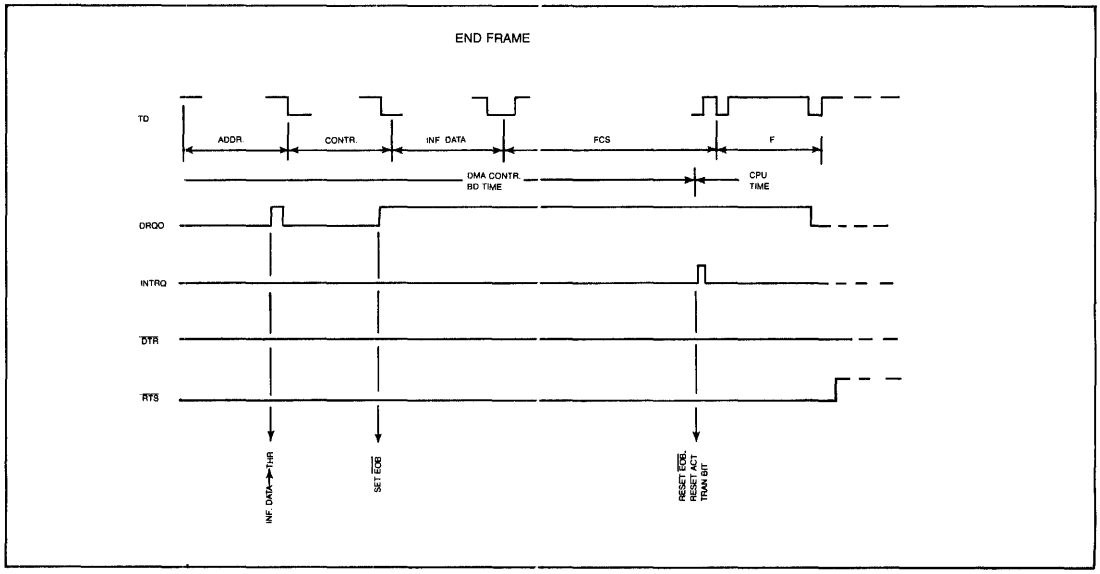


Figure 20. DMA TIMING OF LAST FRAME

WD1933 RECEPTION EXAMPLE 1

A sequence of events is shown in illustrating how to receive a message with the WD1933 device. For simplicity, the same SDLC frame structure is used as in Transmission Example 1. Also, please refer to the same interface circuitry shown in Figure 2.

Figure 21 illustrates the functional flow, and Figure 22 contains the timing information.

WD1933 RECEPTION EXAMPLE 2

This example shows a frame with two ADDRESS characters, two CONTROL characters, one 5-bit INFORMATION DATA character, and two residual bits. This example may not be a typical frame, but it shows how the WD1933 works in a wide range of frame structures.

The first FLAG and FCS are not shown in detail, and are not critical to this example.

Figure 23 illustrates the functional flow, and Figure 24 contains the timing information.

WD1933 LOOP DATA LINK EXAMPLE

This example shows how to program a secondary station to function in SDLC Loop mode. The functional flow is illustrated in Figure 25, and the interface circuit is shown in Figure 2.

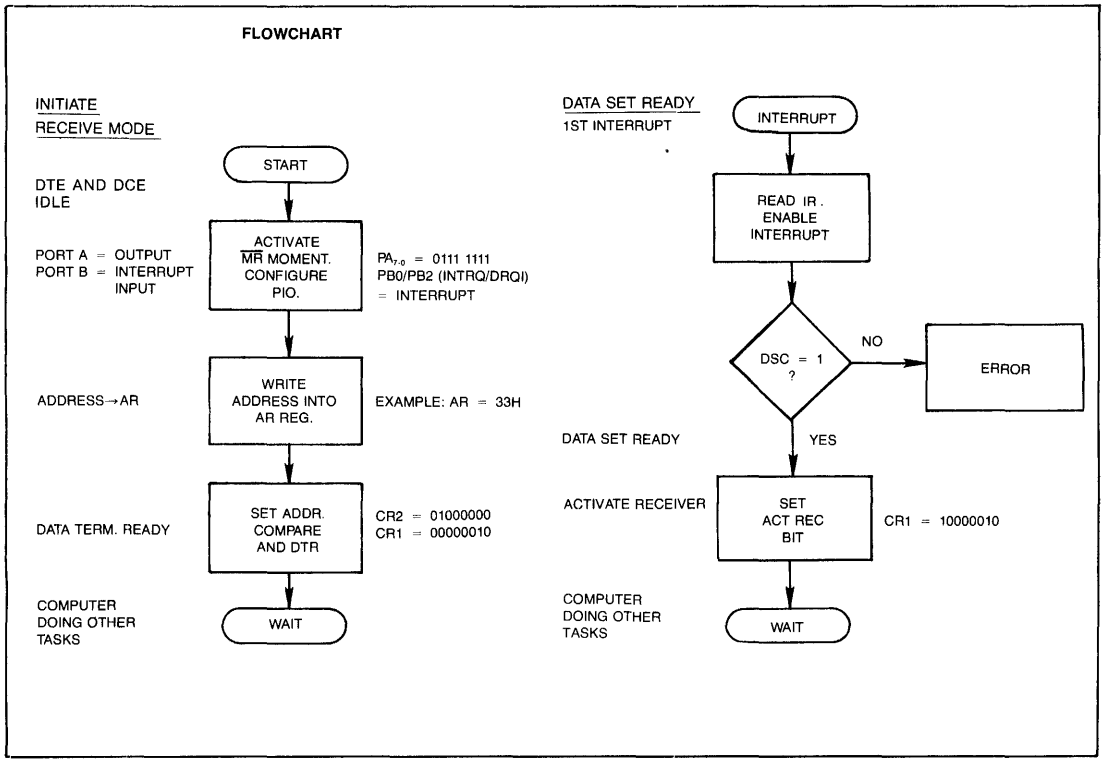


Figure 21. FLOW DIAGRAM OF FRAME RECEPTION (EXAMPLE NO. 1)

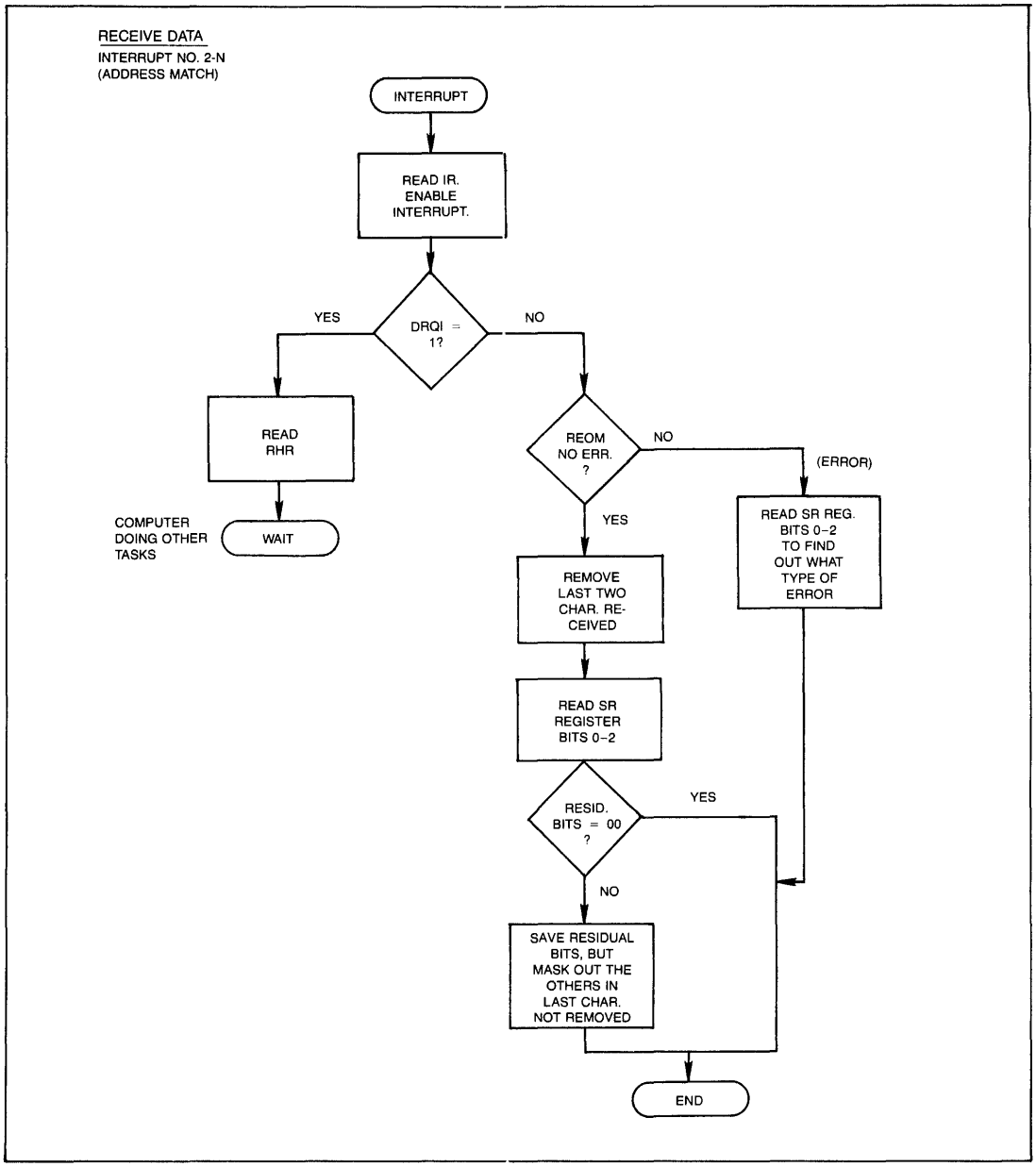


Figure 21. FLOW DIAGRAM OF FRAME RECEPTION

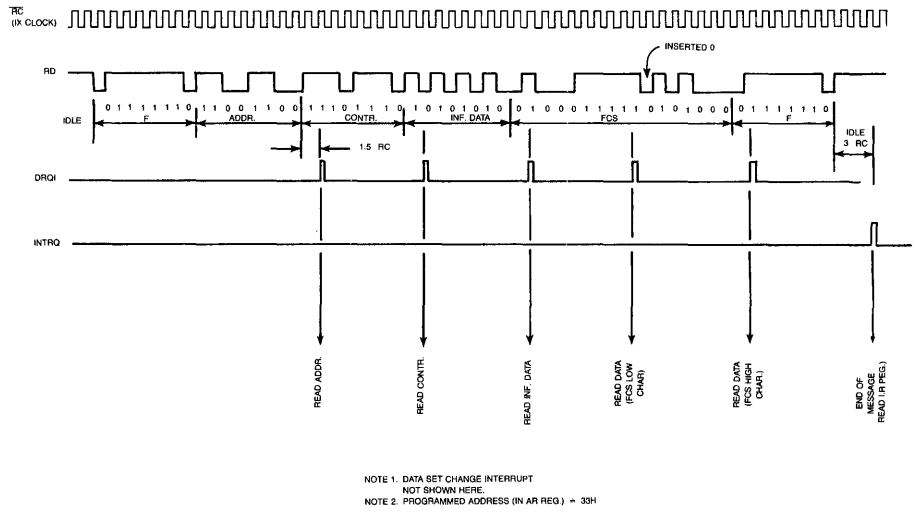


Figure 22. TIMING DIAGRAM OF FRAME RECEPTION (EXAMPLE NO. 1)

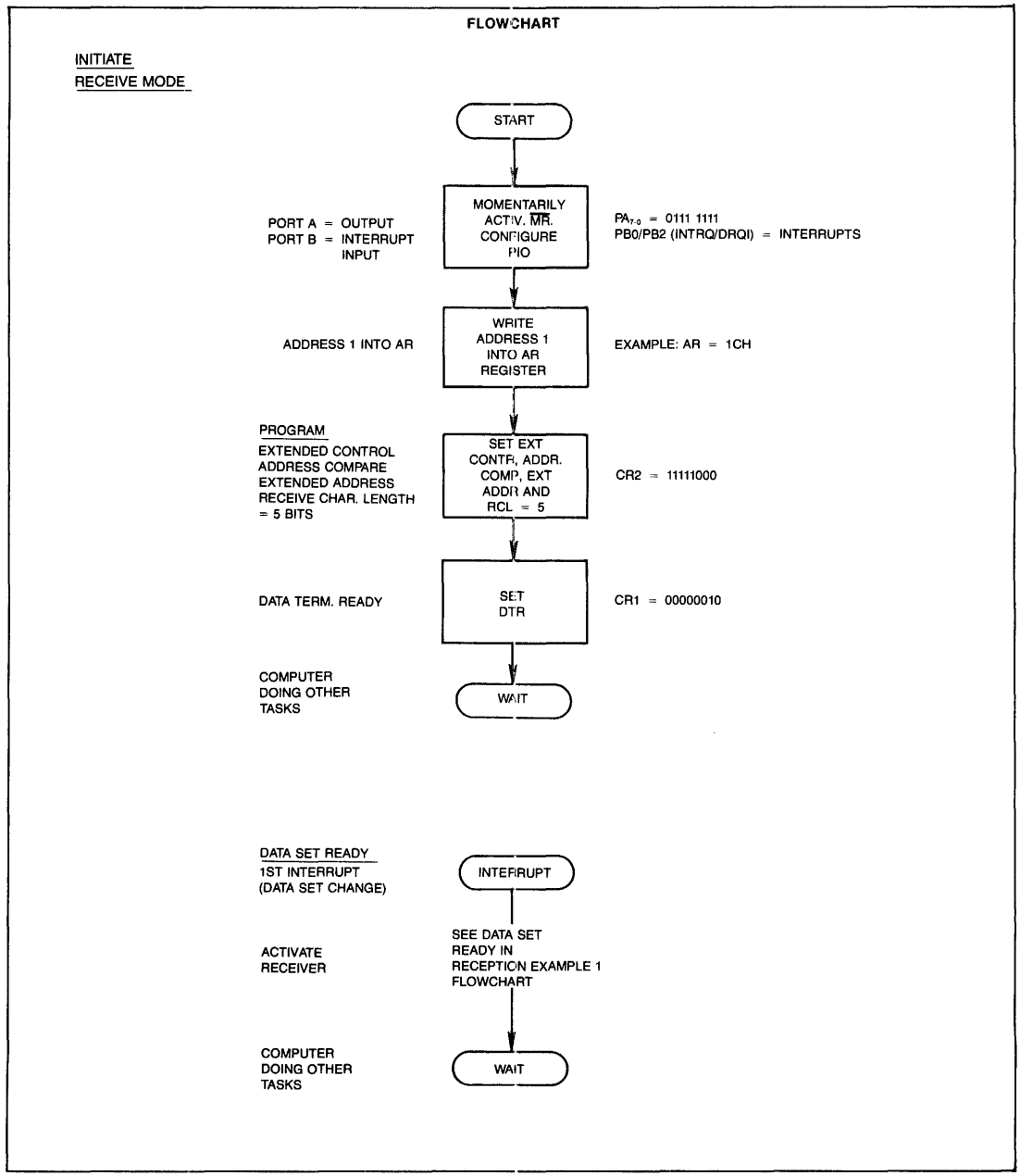


Figure 23. FLOW DIAGRAM OF FRAME RECEPTION (EXAMPLE NO. 2)

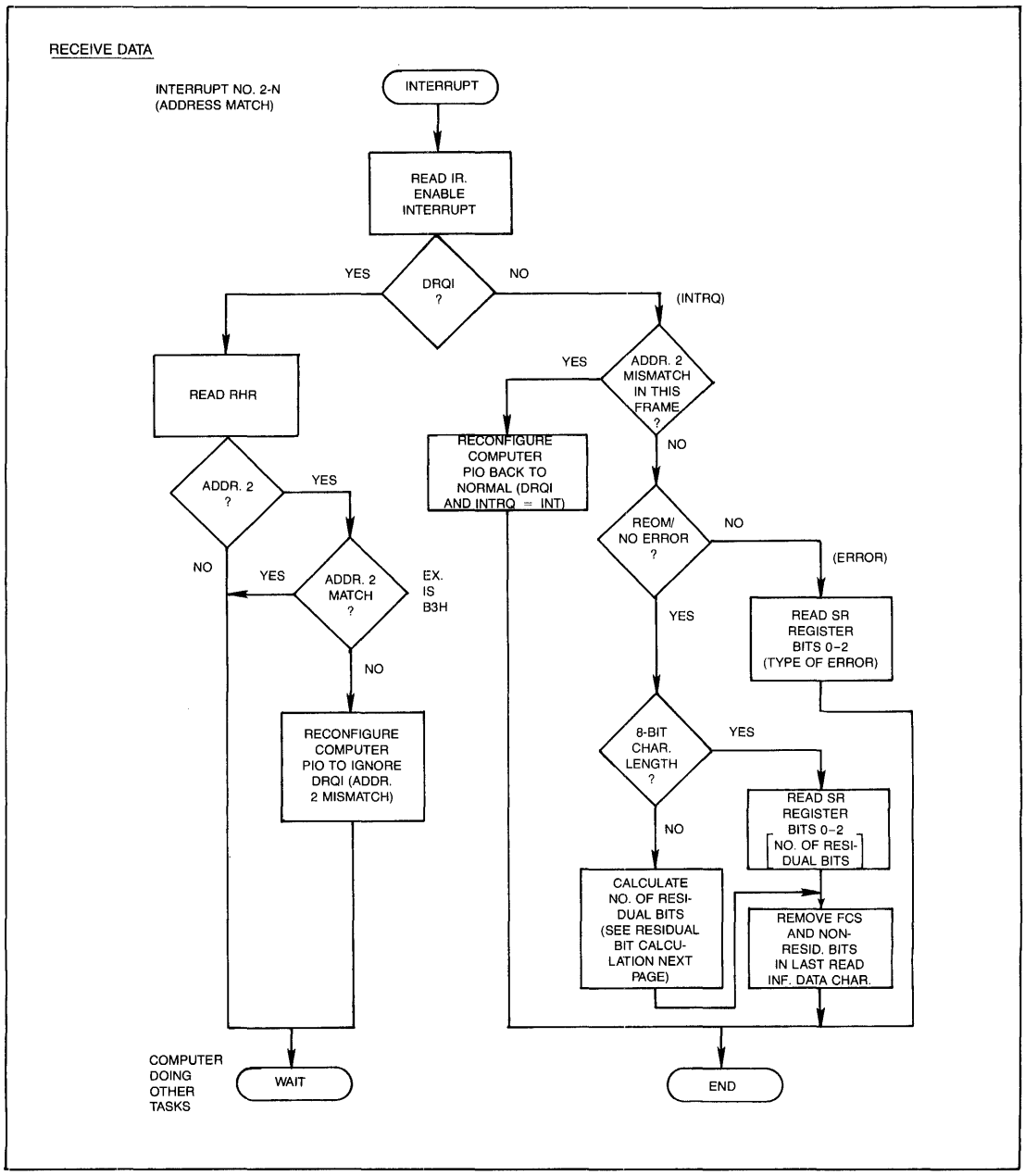


Figure 23. FLOW DIAGRAM OF FRAME RECEPTION

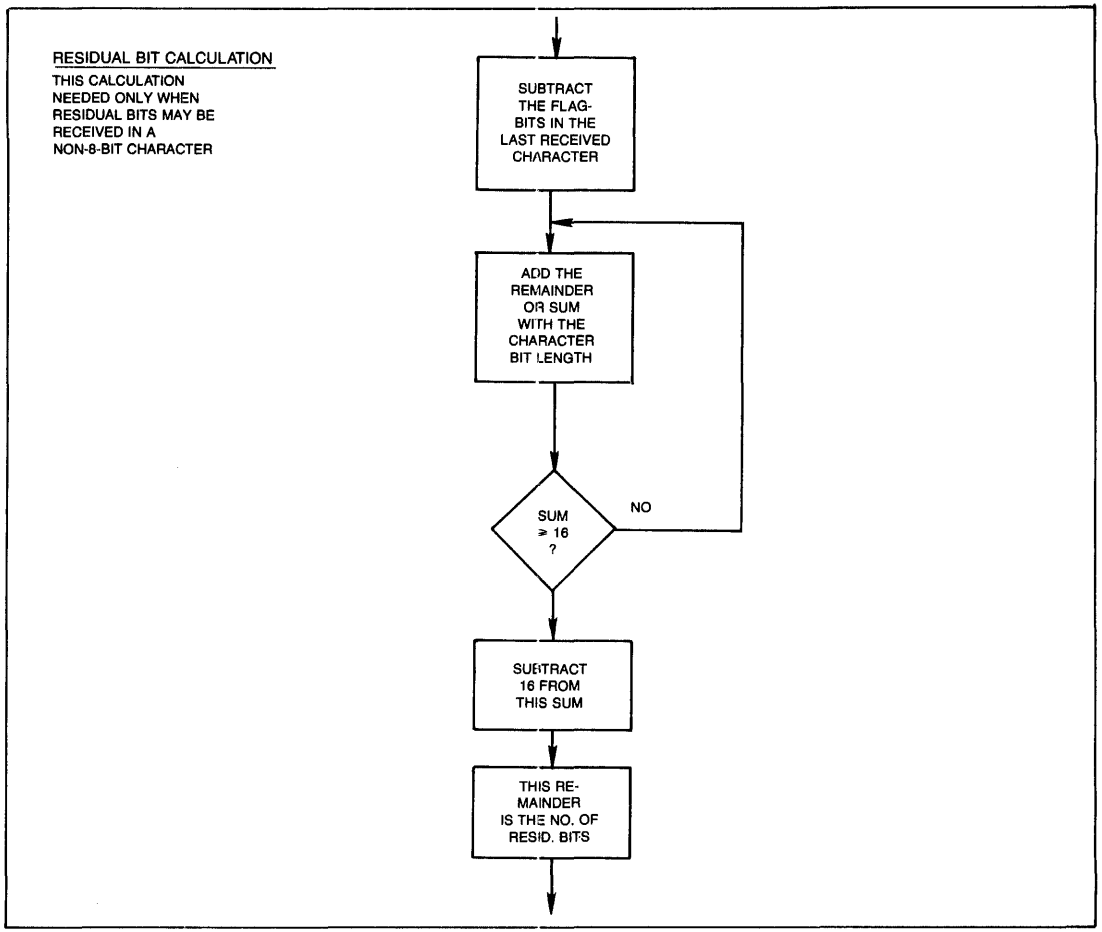


Figure 23. FLOW DIAGRAM OF FRAME RECEPTION

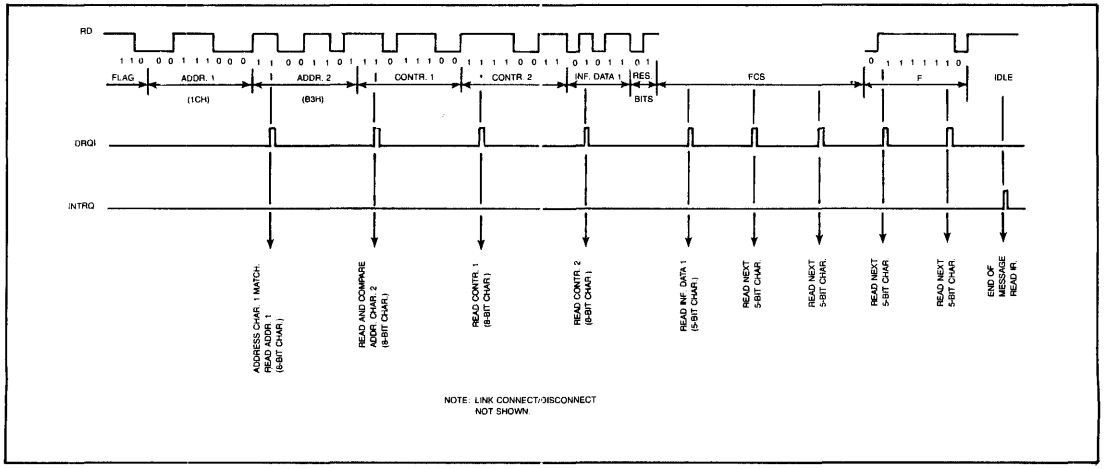


Figure 24. TIMING DIAGRAM OF FRAME RECEPTION (EXAMPLE NO. 2)

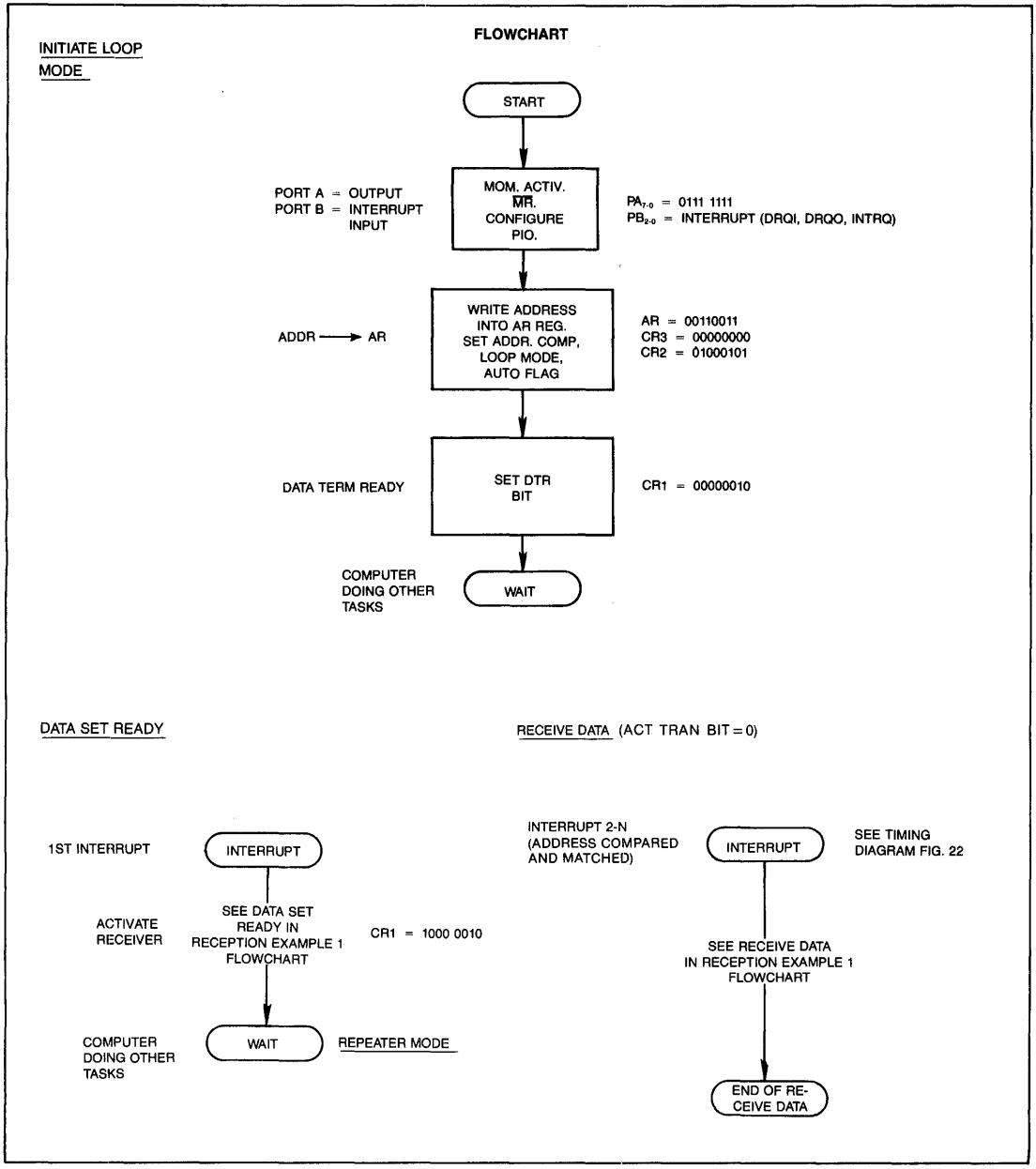


Figure 25. FLOW DIAGRAM OF SDLC LOOP MODE OPERATION

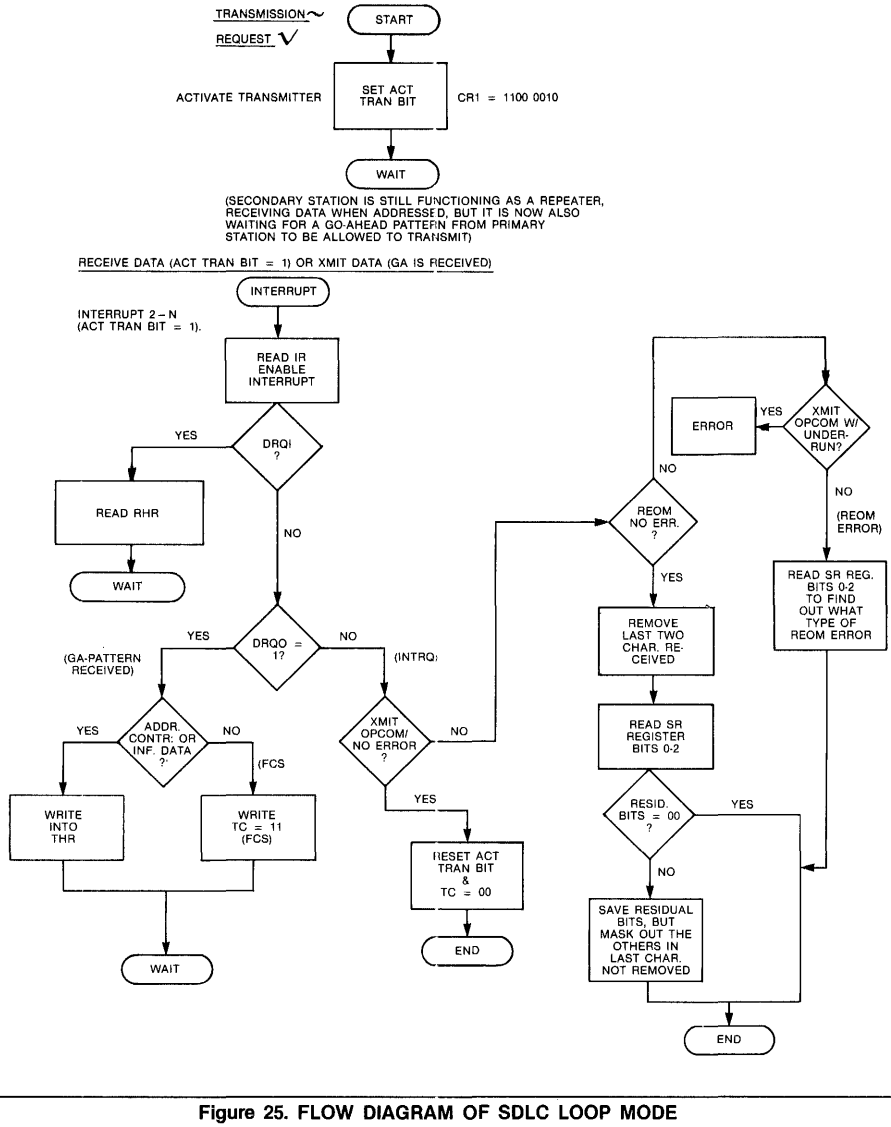


Figure 25. FLOW DIAGRAM OF SDLC LOOP MODE

CONCLUSION

The WD1931 and WD1933 devices are highly compatible, which allows the design of a multiprotocol communications board. This compatibility allows the use of asynchronous, character oriented synchronous, and bit oriented synchronous communications protocols with the same 40 pin socket.

APPENDIX

RELATED DOCUMENTS

WD1931 Data Sheet, Western Digital Corporation
WD1933 Data Sheet, Western Digital Corporation

See page 725 for ordering information.

Printed in U.S.A.

WD1993 Arinc 429 Receiver/Transmitter and Multi-Character Receiver/Transmitter

FEATURES

- PRESENT UPON MASTER RESET FOR ARINC 429 PROTOCOL
- PROGRAMMABLE WORD LENGTH FROM 1 CHARACTER TO 8 CHARACTERS
- PROGRAMMABLE CHARACTER LENGTH, 5, 6, 7, OR 8 BITS
- RETURN TO ZERO (RZ) OUTPUT
- AUTO SPACE GENERATION
- DOUBLE BUFFERED RECEIVER AND TRANSMITTER
- UNDERRUN ERROR DETECTION FOR TRANSMISSION
- OVERRUN, FRAMING AND PARITY ERROR DETECTION ON RECEIVER
- WORD ERROR FLAG FOR COMPREHENSIVE ERROR REPORTING
- FIRST CHARACTER OF WORD FLAG FOR SINGLE INTERRUPT APPLICATIONS
- DIAGNOSTIC LOCAL LOOP-BACK TEST MODE
- DC TO 200 KILOBITS PER SECOND OPERATION
- TTL COMPATIBLE INPUTS AND OUTPUTS
- SINGLE +5 VOLT SUPPLY
- TEMPERATURE RANGES 0°C to 70°C, — 1993-03, −40°C to +85°C — 1993-02, −55°C to +125°C — 1993-01

INTRODUCTION

The Western Digital WD1993 Avionic Receiver/Transmitter is designed to handle digital data transmission, according to the Avionic Arinc 429 protocol. Also, the word length is programmable from one to eight characters of 5, 6, 7, or 8 bits. Parallel data is converted into a serial data stream during transmission and serial to parallel during reception. The WD1993 is packaged in a 28 pin plastic or ceramic package and is available in three temperature ranges: Commercial, Industrial and Military.

GENERAL DESCRIPTION

The WD1993 is a bus-orientated MOS/LSI device designed to provide the Avionics Arinc 429 Data Communication Protocol, along with programmable character length capabilities.

Also, the WD1993 contains a local loop-back test mode of operation, which is controlled by the Loop Test Enable (LTE) bit in the command register. In this diagnostic mode, the transmitter output is "looped-back" into the receiver input. The REN and TEN control bits must also be active ("1") and the CTS input must be low. The status and output flags operate normally.

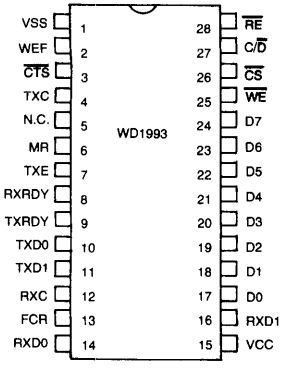


Figure 1 PIN DIAGRAM

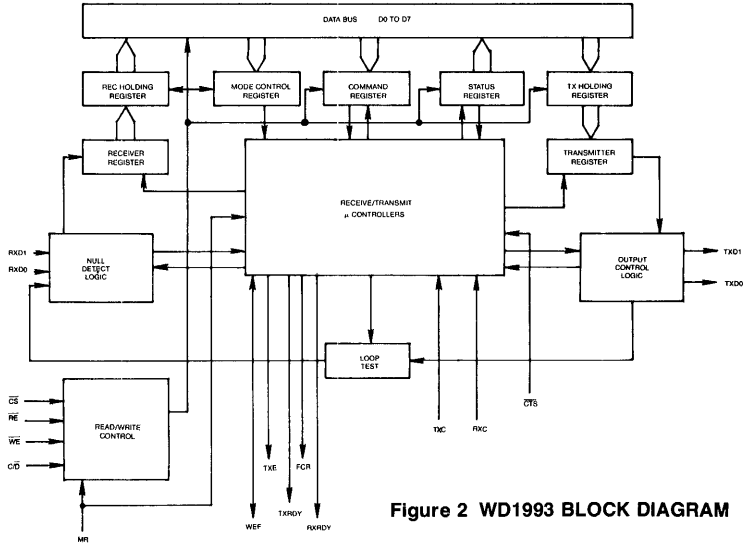


Figure 2 WD1993 BLOCK DIAGRAM

PIN NO.	SYMBOL	SIGNAL NAME	FUNCTION
1	VSS	GROUND	Ground
2	WEF	WORD ERROR FLAG	This pin is an output, which when active indicates an error in either the transmitter or receiver has been detected. It reflects an underrun, overrun, parity or framing (receive word) error and is intended as an error interrupt. The Status Register should be read to determine the specific error.
3	$\overline{CTS}$	CLEAR-TO-SEND	This input is activated (V_{IL}) to enable the transmitter logic.
4	TXC	TRANSMIT CLOCK	This input is the source clock for transmission. The data rate is a function of this clock frequency. ARINC MODE = 4 × bit rate
5	N.C.		No Internal Connection
6	MR	MASTER RESET	When active (V_{IH}), presets the WD1993 mode and command registers to the ARINC protocol. Master Reset also resets the data registers and places the WD1993 transmitter and receiver into idle states. After MR, the command register is set to 00100101 and the mode register is set to 00111100.
7	TXE	TRANSMITTER EMPTY	This output goes high to indicate the end of a transmit operation. TXE is automatically reset after the Transmit Holding Register is loaded.
8	RXRDY	RECEIVER READY	This output, when high, alerts the CPU that the Receiver Holding Register contains a data character that is ready to be input. This output is automatically reset whenever a character is read from the WD1993. RXRDY is enabled unless inhibited by setting command bit CR3 (RXRDYIN) to a logic "1." It is automatically enabled again after a receive sequence is completed.
9	TXRDY	TRANSMITTER READY	This output, when high, alerts the CPU that the Transmit Holding Register is ready to accept a data character. The TXRDY output is automatically reset whenever a character is written into the WD1993 and can be used as an interrupt to the system.
10	TXD0	TRANSMIT DATA ZERO	This output drives the V/Z circuit when a logic zero is to be transmitted and is active for one-half bit time.
11	TXD1	TRANSMIT DATA ONE	This output drives the V/Z circuit when a logic one is to be transmitted and is active for one-half bit time.

PIN NO.	SYMBOL	SIGNAL NAME	FUNCTION
12	RXC	RECEIVE CLOCK	This input is the source clock for reception. The data rate characteristics are the same as the transmit clock.
13	FCR	FIRST CHARACTER READY	This output goes high after the receiver has completed reception of the first character in a multi-character sequence.
14	RXD0	RECEIVE DATA ZERO	RXD0 is driven by the line V/Z receiver circuit. When the V/Z circuit detects a logic zero, a TTL logic one (active for one-half bit time) is provided to the WD1993.
15	VCC	POWER SUPPLY	+5V DC
16	RXD1	RECEIVE DATA ONE	The RXD1 input is driven by the V/Z line receiver. Each time the V/Z circuit detects a logic one, a TTL level logic one (active for one-half bit time) is provided to this input.
17 18 19 20 21 22 23 24	D0 D1 D2 D3 D4 D5 D6 D7	DATA BUS	This is the bi-directional data bus. It is the means of communication between the WD1993 and the CPU. Control, Mode, Data and Status Registers are accessed via this bus.
25	$\overline{WE}$	WRITE ENABLE	When active (V_{IL}), allows the CPU to write into the selected register.
26	$\overline{CS}$	CHIP SELECT	When active (V_{IL}), the device is selected. This enables communication between the WD1993 and a microprocessor.
27	C/$\overline{D}$	CONTROL/DATA	This input is used in conjunction with an active read or write operation to determine register access via the DATA BUS.
28	$\overline{RE}$	READ ENABLE	When active (V_{IL}), allows the CPU to read data or status information from the WD1993.

ORGANIZATION

A block diagram of the WD1993 is shown in figure 2.

As mentioned, the WD1993 is an eight bit bus-oriented device. Communication between the WD1993 and the controlling CPU occurs via the 8 bit data bus through the bus transceivers. There are 2 accessible data registers, which buffer transmit and receive data. They are the Transmit Holding Register and the Receive Holding Register. There is a parallel-to-serial shift register (parallel in-serial out), the transmit register and a serial-to-parallel shift register (serial in-parallel out), the receive register.

Operational control and monitoring of the WD1993 is performed by two control registers (the command instruction register and the mode instruction register) and the status register.

A read/write control circuit allows programming/monitoring or loading/reading of data in the control, status or holding registers by activating the appropriate control lines: Chip Select ($\overline{CS}$), Read Enable ($\overline{RE}$), Write Enable ($\overline{WE}$),and Control or Data Select (C/$\overline{D}$).

Internal control of the WD1993 is by means of two internal microcontrollers; one for transmit and one for receive. The control registers, null detect logic and various counters, provide inputs to the microcontrollers which generate the necessary control signals to send and receive serial data according to the Arinc 429-1 protocol, along with the programmable multicharacter capabilities.

OPERATION

Upon master reset (MR), the device is programmed to transmit and receive four 8-bit contiguous characters with the 32nd bit odd parity. (ARINC protocol.)

A minimum four bit time space is automatically inserted after the character transmission. Two receiver inputs, RXD1/RXD0 and two transmitter outputs, TXD1/TXD0, are provided to interface with voltage—impedance (V/Z) circuits to translate ± 10 volt ARINC line levels to 5 volt TTL logic levels. The transmit clock (TXC) and receive clock (RXC), in ARINC mode, are four times (4X) the bit rate desired.

The receiver monitors the received data input to detect a four bit time null, which delimits the word. If the communications link is broken during a word reception, the receiver will generate a word error flag to (WEF) to notify the CPU to request retransmission. When a null is detected, the receiver logic is reset and returned to an idle state awaiting the next word.

The WD1993 may also be programmed to support a multiple character word consisting of from one to eight characters. Also, the character length is programmable from 5 to 8 bits, and the parity bit if parity is used, may be either inside or outside the word.

The Command Register is used to select features such as parity options, loop test capability, RXRDY flag enabling, transmitter and receiver enabling, and may also cause the WD1993 to return to the Mode instruction.

The Mode Register is used to select features such as bits/character and characters/word.

The Status Register contains information such as Transmitter Ready, Transmitter Empty, Receiver Ready, error conditions, and First Character Ready.

OPERATING DESCRIPTION

The WD1993 is primarily designed to operate in an 8 bit micro-processor environment, although other control logic schemes are easily implemented. The DATA BUS and the Interface Control Signals ($\overline{CS}$, $\overline{RE}$, $\overline{WE}$ and C/$\overline{D}$) should be connected to the microprocessor's data bus and system control bus.

The appropriate TXC and RXC clock frequencies should be selected for the particular application, using a programmable baud rate generator such as a BR1941. A master reset pulse initializes the WD1993 and presets the control registers to the ARINC protocol.

The RXD1/RXD0 inputs are interfaced to the DITS data line via external level translators that provide TTL (5V) logic levels to the WD1993. The TXD1/TXD0 outputs are connected to high voltage (± 10V) driver circuits. Figures 16 and 17 show some typical ± 10V translator and driver circuits.

The TXRDY, RXRDY, FCR and WEF Flags may be connected to the microprocessor system as interrupt inputs. The status register can be periodically read in a polled environment to support WD1993 operations.

The $\overline{CTS}$ input can be used to synchronize the transmitter to external events.

The WD1993 is designed such that a control register write operation accesses the command instruction register.

The RXRDYIN bit of the command register is used to inhibit the RXRDY output pin for ARINC operations.

MULTI-CHARACTER OPERATIONS

As discussed above, the WD1993 is equipped with a multicharacter option which provides the user with the means of transmitting and receiving multiple contiguous characters of data within one set of delimiters—4 bit nulls for ARINC 429. Since the WD1993 is an 8 bit bus-oriented device, the controlling processor must read the WD1993 data from its holding register before the subsequent characters are assembled. This situation also exists on the transmit side, i.e., the Transmit Holding Register must be loaded before the previous 8 bits are completely shifted out of the transmit register.

Several "flags" are provided for interrupt purposes so that continuity is maintained and data integrity is preserved. These flags are First Character Ready (FCR), Receiver Ready (RXRDY), Transmitter Ready (TXRDY) and Transmitter Empty (TXE).

The Transmitter operates as follows:

a) With the mode and command registers programmed as desired, the transmitter is enabled, TEN (CR0) = "1".

b) The TXE and TXRDY flags are "1" (active).

c) The external $\overline{CTS}$ signal = "0".

d) The CPU loads data into the Transmitter Holding Register, TXE and TXRDY go Low.

e) The data is loaded into the transmit register and TXRDY goes high. This indicates the first data word is being sent and a character can be loaded into the holding register. If the WD1993 is programmed for more than one character (multi-character) then an underrun error will be generated if the next character is not loaded before the previous word is completely shifted out, unless the current character is the last character in a sequence.

f) If the last character is transmitted and no more new data is to be sent, the transmitter will indicate its status by raising the TXE flag. (No error is generated as a result of this condition.)

The Receiver operates similarly:

a) With the control registers suitably programmed, the receiver is enabled, REN (CR2) = "1".

b) The RXRDY and FCR flags are "0". (Inactive).

c) The incoming data word activates the receive logic and the data begins to be assembled in the receive register.

d) When the first character is completely assembled, the data is loaded into the Receive Holding Register, the FCR (First Character Ready) and RXRDY (Receiver Ready) flags become active, "1". The CPU should read the data prior to the reception of the next character or an overrun error will be generated as the receiver will overwrite the old data with the new data character just received.

The exception to this is in the ARINC mode, where the first character in the ARINC protocol contains a label. The FCR and RXRDY Flags become active to indicate the reception of the first character of data. The CPU reads the first character and decides whether or not it wants to acquire the subsequent characters. If not, then the CPU performs a "control write" to the COMMAND REGISTER, setting the RXRDYIN (CR3) bit to a "1". This bit in ARINC mode, inhibits the RXRDY flag from interrupting the CPU during the reception of the 3 remaining characters. The RXRDYIN bit is then automatically reset upon completion of the receive sequence and RXRDY is enabled again.

LOOP TEST MODE

As mentioned, the WD1993 is equipped with a diagnostic test mode, local loop-back. This mode is activated by setting the LTE command bit to a "1". The TEN and REN bits should be "1" and $\overline{CTS}$ should be "V_{IL}". The receiver inputs are ignored and the transmitter outputs are sending nulls. The transmitter is internally "looped-back" to the receiver and the error and status flags operate normally.

For basic testing, failing to reload the Transmit Holding Register in the middle of a data send sequence will cause an underrun error in the transmitter and a word error in the receiver. Failure to read the Receive Holding Register after a FCR or RXRDY flag will cause an overrun error to be generated.

For Loop-Back test operations, the user should be sure that the TXC and RXC clock frequencies are the same. This is normally implemented by placing the same clock signal on both pins (TXC and RXC).

ARINC BACKGROUND

Aeronautical Radio Inc. (ARINC) publishes the ARINC 429 specification. This document defines the air transport industries standards for the transfer of digital data between avionics systems elements. This specification was adopted by The Airlines Electronic Engineering Committee April 11, 1978. By the adoption of this specification the foundation is set for a standard protocol governing all intersystems equipment (Line Replaceable Units).

MARK 33 DIGITAL INFORMATION TRANSFER SYSTEM (DITS)

Basic Philosophy
Transmit from a designated output port over a single twisted and shielded pair of wires to designated receiver.

Bidirectional data flow not permitted on a given pair.

Data Transfer
Numeric
Iso Alphabet #5
Graphic

Data Format
32 bits or less (unused bit positions should be filled with binary zeros or valid data pad bits).

Bit #32 is assigned to parity.

Modulation
Return to Zero (RZ)

Transmit Voltage Levels

high	+10	±0.5V
null	0	±0.5V
low	−10	±0.5V

Receiver Voltage Levels:

	(in absence of noise)	(noisy environment)
high	+6.0V to +10V	+5.0V to +13V
low	−6.0V to +10V	−5.0V to −13V

No damage to receiver up to 20 vac rms between A & B; +28, A to Gnd; −28, B to Gnd.

Data Rate
100 kilo bit per second ± 1%
Low speed 12 to 14.5 kilo bit per second ± 1%

Word Synchronization
All zero gap of a minimum of 4 bit times

REGISTER DEFINITIONS

The format and definition of the Command Register is shown below:

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
EPS	IR	PEN	LTE	RXRDYIN	REN	PIA	TEN

TEN	Transmit ENable
1	Enabled
0	Disabled

PIA	Parity Inside or After
1	After the data word
0	Inside (the last data bit) of word

REN	Receive ENable
1	Enabled
0	Disabled

RXRDYIN	RXRDY Inhibit
1	Inhibit RXRDY output flag
0	Normal transmitter operation enable RXRDY output flag

LTE	Loop Test ENable
1	Local loop-back mode
0	Normal Operation

PEN	Parity ENable
1	Enabled
0	Disabled

IR	Internal Reset
1	Returns WD1993 to mode instruction
0	format

EPS	Even Parity Select
1	Even parity
0	Odd parity

The format and definition of the Mode Register is shown below:

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
X	N3	N2	N1	CLS2	CLS1	X	X

CLS2	CLS1	Character Length Select
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

N3	N2	N1	Characters Per Word Select
0	0	0	1 character
0	0	1	2 characters
0	1	0	3 characters
0	1	1	4 characters
1	0	0	5 characters
1	0	1	6 characters
1	1	0	7 characters
1	1	1	8 characters

The WD1993 registers are addressed according to the following table:

$\overline{CS}$	C/$\overline{D}$	$\overline{RE}$	$\overline{WE}$	Registers Selected
L	L	L	H	Read Receive Holding Register
L	L	H	L	Write Transmit Holding Register
L	H	L	H	Read Status Register
L	H	H	L	Write Control Registers
H	X	X	X	Data Bus Tri-Stated

L = V_{IL} at pins
H = V_{IH} at pins
X = don't care

The format of the Status Register is shown below:

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
UE	FCR	WEF	OE	PE	TXE	RXRDY	TXRDY

TXRDY — Transmitter Ready

1 — Active (THR can be reloaded)
0 — Inactive (transmitter is busy)

RXRDY — Receiver Ready

1 — Active (RHR should be read)
0 — Inactive

TXE — Transmitter Empty

1 — Transmitter idle
0 — Transmitter active

PE — Parity Error

1 — Error reported
0 — No error

OE — Overrun Error

1 — RHR has been overwritten
0 — No error

WEF — Word Error Flag

1 — Indicates improper receive sequence (word error), overrun error, parity error, framing error or underrun error.
0 — No error

FCR — First Character Ready

1 — This bit indicates the receiver has just completed assembly of the 1st character in a multi-character sequence and that the data is contained in the RHR.
0 — First character not ready.

UE — Underrun Error

1 — Indicates that the THR has not been loaded with a new character in time for a contiguous data transmission sequence.
0 — No error

ABSOLUTE MAXIMUM RATINGS

Storage Temperature −55°C to +125°C (Plastic Package)
−65°C to +150°C (Ceramic Package)

Voltage on any Pin with Respect to Ground . . −0.3V to +7V
Power Dissipation . . . . . 400 MW

Note: Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = 5.0V ± 5%; GND = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	−0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −100μA
I_{DL}	Data Bus Leakage			50	uA	Data Bus is in High Impedence State
				10	uA	
I_{IL}	Input Leakage			10	uA	V_{IN} = V_{CC}
I_{CC}	Power Supply Current		45	80	mA	V_{CC} = 5.25V No Load

CAPACITANCE

T_A = 25°C; V_{CC} = GND = ØV

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	f_C = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

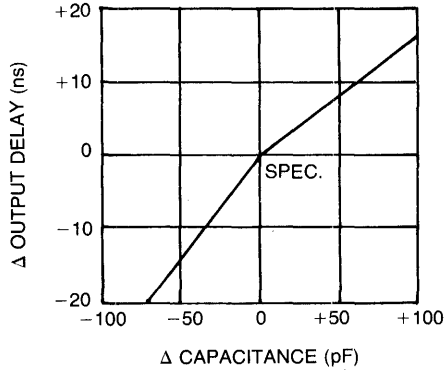


Figure 3 OUTPUT DELAY vs CAPACITANCE

A.C. TIMING PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
BUS PARAMETERS					
Read Cycle (Reference Figure 6)					
t_{AR}	Address Stable before $\overline{RE}$, ($\overline{CS}$, C/$\overline{D}$)	50		ns	
t_{RA}	Address Hold Time for $\overline{RE}$, ($\overline{CS}$, C/$\overline{D}$)	5		ns	
t_{RE}	$\overline{RE}$ Pulse Width	350		ns	
t_{RD}	Data Delay from $\overline{RE}$		200	ns	C_L = 50 pF
t_{RDH}	$\overline{RE}$ to Data Floating		200	ns	C_L = 50 pF
		25		ns	C_L = 15 pF
WRITE CYCLE (Reference Figure 7)					
t_{AW}	Address Stable before $\overline{WE}$	20		ns	
t_{WA}	Address Hold Time for $\overline{WE}$	20		ns	
t_{WE}	$\overline{WE}$ Pulse Width	350		ns	
t_{DS}	Data Set-Up Time for $\overline{WE}$	200		ns	
t_{WDH}	Data Hold Time for $\overline{WE}$	40		ns	
OTHER TIMINGS (Reference Figures 8, 9)					
t_{DTX}	TXD Delay from Falling Edge of TXC		500	ns	C_L = 100 pF
t_{SRX}	Rx Data Set-up Time to Sampling Pulse	200		ns	C_L = 100 pF
t_{NRX}	Rx Data Hold Time to Sampling Pulse	100		ns	C_L = 100 pF
t_{TX}	Transmitter Input Clock Frequency				
	4×	DC	800	kHz	
t_{TPW}	Transmitter Input Clock Pulse Width				
	4×	500		ns	
t_{TPD}	Transmitter Input Clock Pulse Delay				
	4×	500		ns	
t_{RX}	Receiver Input Clock Frequency				
	4×	DC	800	kHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	4×	500		ns	
t_{RPD}	Receiver Input Clock Pulse Delay				
	4×	500		ns	
				ns	
t_{TX}	TXRDY Delay from center of Data Bit		½	t_{TXC}	

A.C. TIMING PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
t_{TX}	TXRDY Delay from Center of Data Bit	200ns	2	t_{TXC}	(4x)
t_{RX}	RXRDY Delay from Center of Data Bit (FCR Delay from Center of Data Bit)		½	R_{RXC}	
	TXE Delay from Center of Data Bit		½	t_{TXC}	C_L = 50 pF 4 × Rate

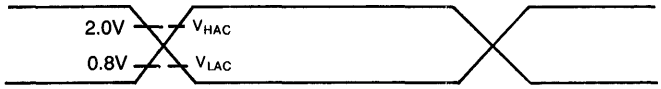


Figure 4 TEST POINTS FOR A.C. TIMING

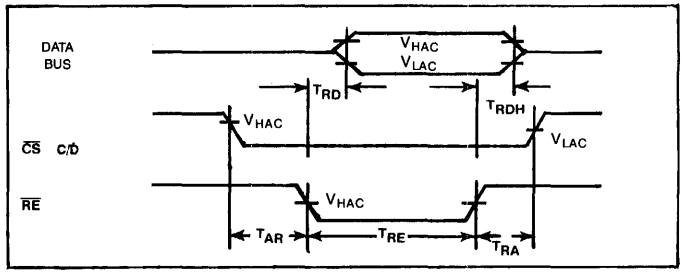


Figure 5 READ CYCLE TIMING

Note: AC timings measured at V_{OH} = 2.0V, V_{OL} = 0.8V and with test load circuit.

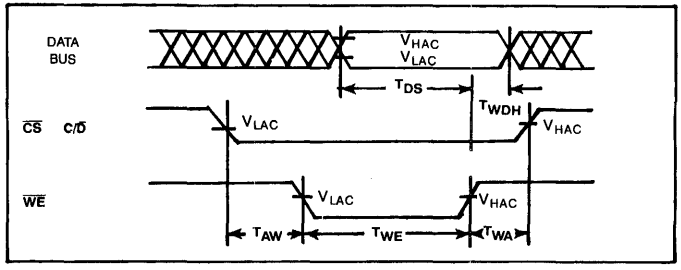


Figure 6 WRITE CYCLE TIMING

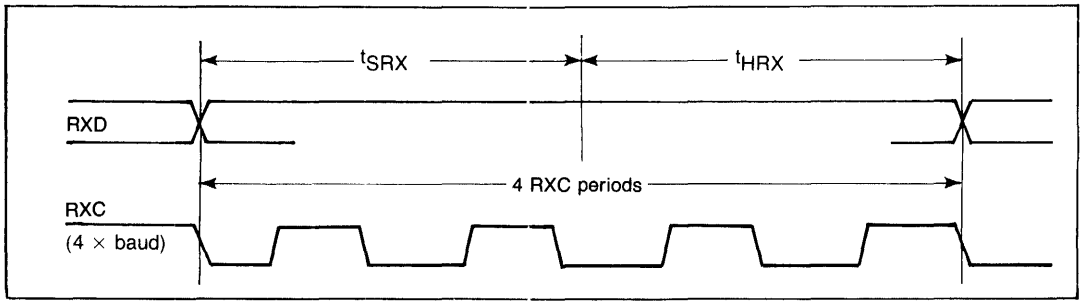


Figure 7 RECEIVER CLOCK AND DATA TIMINGS

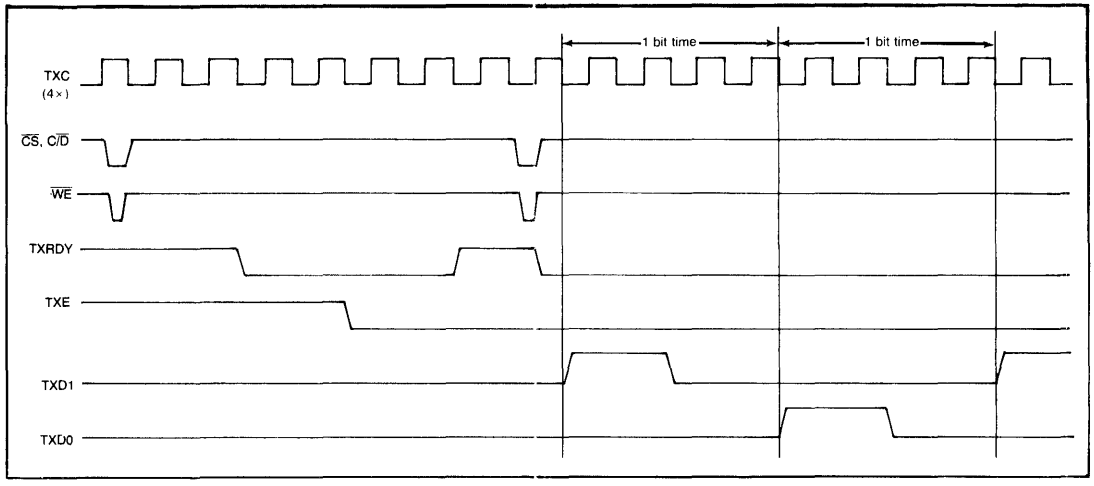


Figure 8 TRANSMITTER TIMINGS (ARINC MODE)

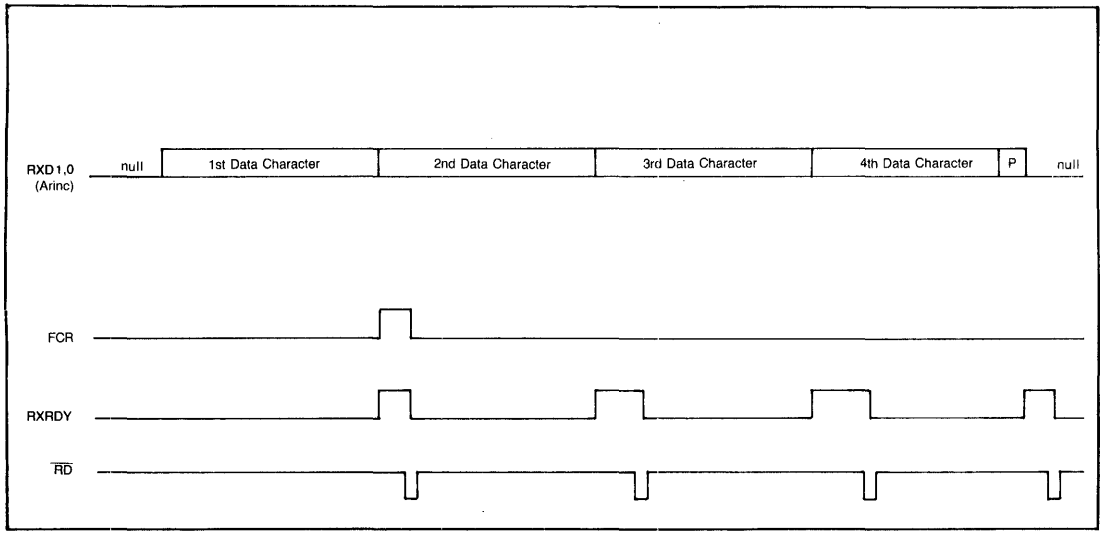


Figure 9 RXRDY AND FCR TIMING

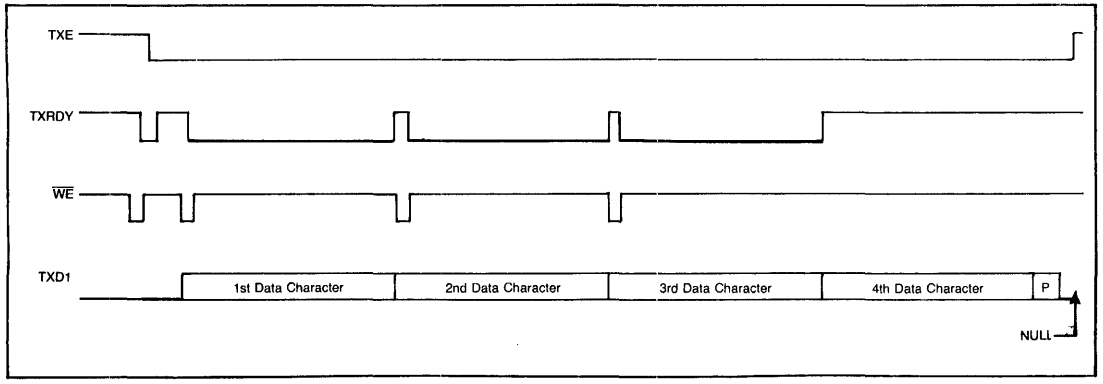


Figure 10 RXRDY AND TXE TIMINGS (4 Character Sequence)

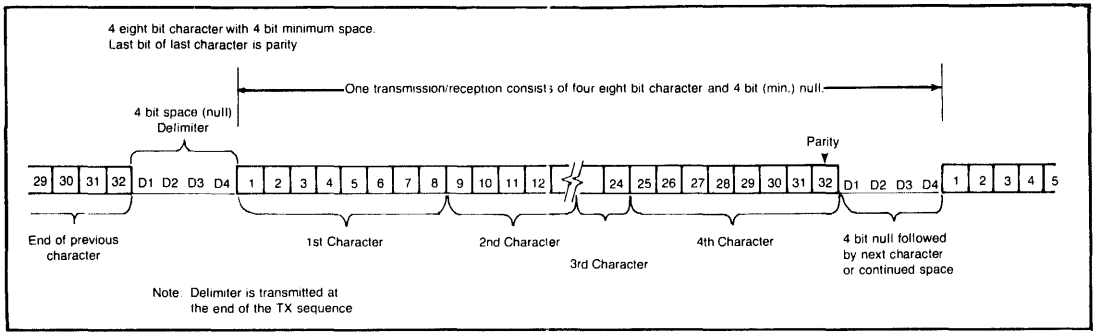


Figure 11 ARINC 429

The V/Z Receiver converts ±10 volt levels to TTL logic levels. It is composed of logic one and zero comparators. A logic one (RXD1) TTL output is derived when voltage rising to 1 (VR1) threshold is crossed and terminated at voltage falling to 1 (VF1). A logic zero (RXD0) TTL output is generated between voltage falling to zero (VFO) and voltage rising from zero (VRO). When input thresholds are not exceeded, neither output is active. The V/Z output can drive one TTL input.

The return to zero (RZ) format is shown below

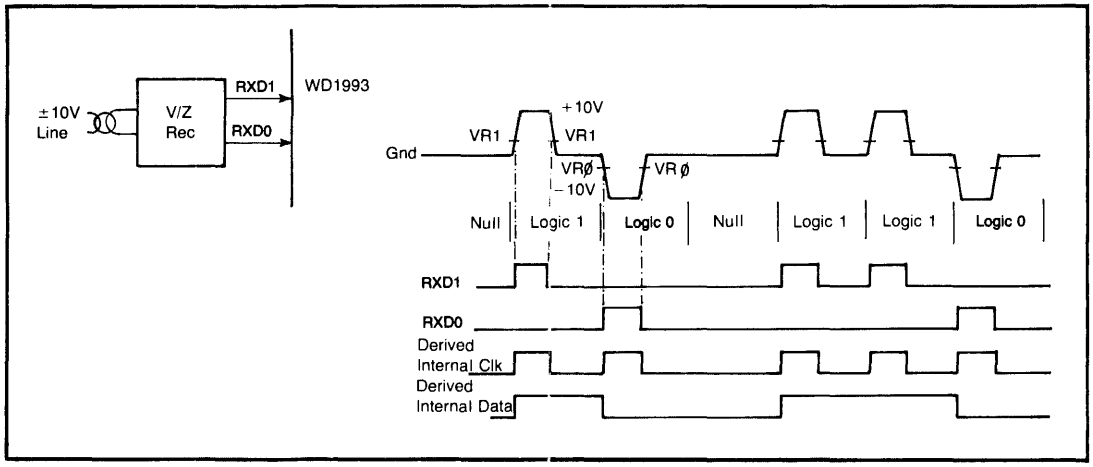


Figure 12 ARINC RECEIVER CIRCUIT

The V/Z Driver convert TTL logic levels into ± 10 volt levels. The TXD1 and TXD0 outputs of the WD1993 are used to drive the line drivers. Each output can drive one TTL load. When the outputs are not active, the line Driver should return to zero.

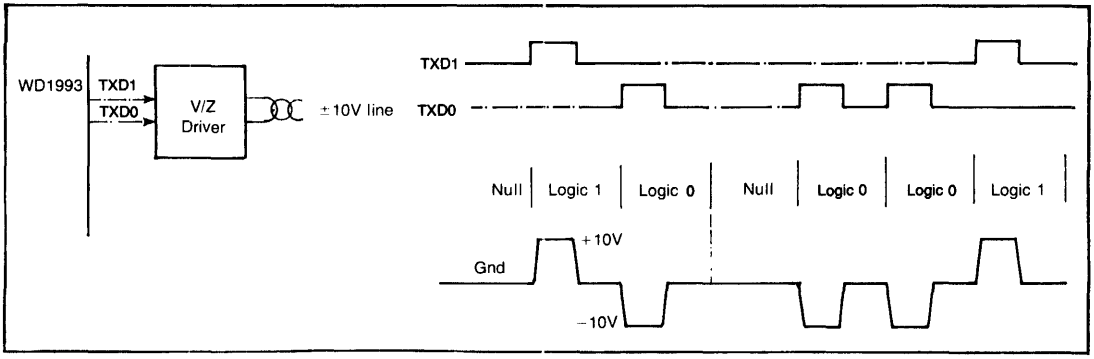


Figure 13 ARINC DRIVER CIRCUIT

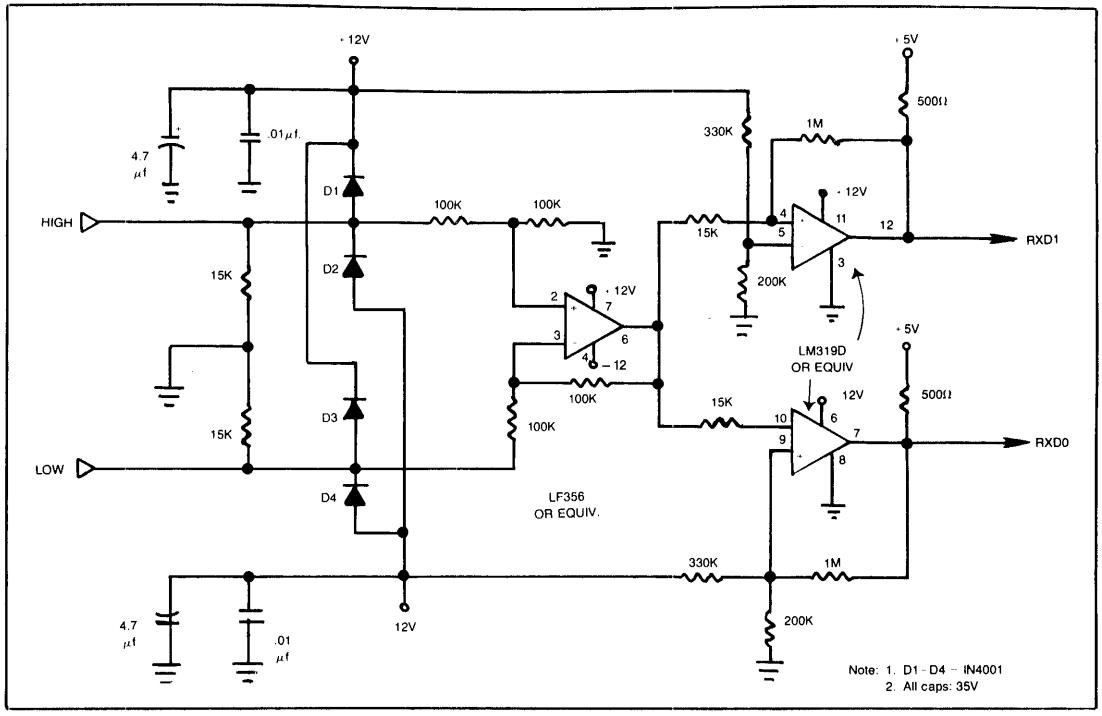


Figure 14 ARINC 429 LINE LEVEL TRANSLATOR (RECEIVER)

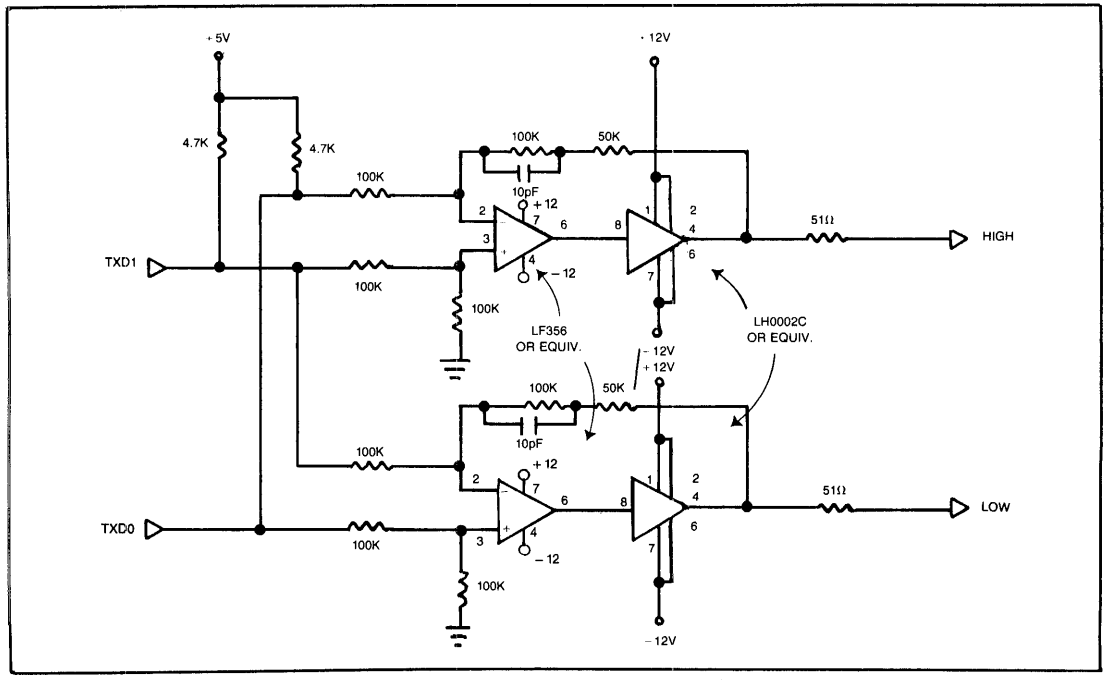


Figure 15 ARINC 429-1 LINE DRIVER

See page 725 for ordering information.

Printed in U.S.A.

PRELIMINARY

WD1984 Multi-Character Synchronous Asynchronous Receiver Transmitter

FEATURES

- TWO OPERATING MODES: SYNCHRONOUS & ASYNCHRONOUS
- 1 TO 8 CHARACTERS OF 5, 6, 7, OR 8 BITS PER CHARACTER TRANSMISSION
- SELECTABLE PARITY INSERTION IN OR AFTER LAST BIT OF WORD
- EVEN/ODD PARITY SELECT OR NO PARITY
- DOUBLE BUFFERED RECEIVER & TRANSMITTER
- ASYNCHRONOUS SELECTABLE CLOCK RATES (1x,16x)
- UNDERRUN ERROR DETECTION FOR TRANSMISSION
- OVERRUN, FRAMING AND PARITY ERROR DETECTION ON RECEIVER
- LINE BREAK GENERATION AND DETECTION (ASYNC MODE)
- FIRST CHARACTER OF WORD FLAG FOR SINGLE INTERRUPT APPLICATIONS
- DIAGNOSTIC LOCAL LOOP-BACK TEST MODE
- DC TO 1M BITS/SEC (1x) OPERATION
- TTL COMPATIBLE INPUTS AND OUTPUTS
- SINGLE +5 VOLT SUPPLY
- 28 PIN CERAMIC OR PLASTIC PACKAGE
- TEMPERATURE RANGES 0°C to 70°C, −40°C TO +85°C

INTRODUCTION

The Western Digital WD1984 is designed to handle digital data transmission, according to two protocols. These are the Synchronous and Asynchronous protocols. Parallel data is converted into a serial data stream during transmission and serial to parallel during reception.

The device can be programmed to transmit and receive words that are 1 to 8 characters in length; 5, 6, 7 or 8 bits per character. Error flags and control signals have been provided to broaden the application range of the device. The WD1984 is packaged in a 28 pin plastic or ceramic package and is available in two temperature ranges: Commercial and Industrial.

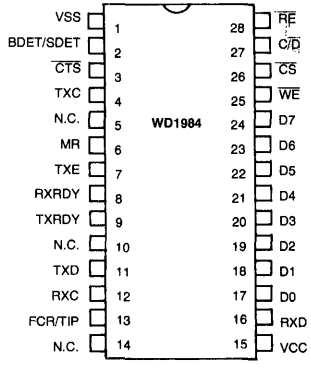


Figure 1 WD1984 PIN-OUT

N.C. No Internal Connection

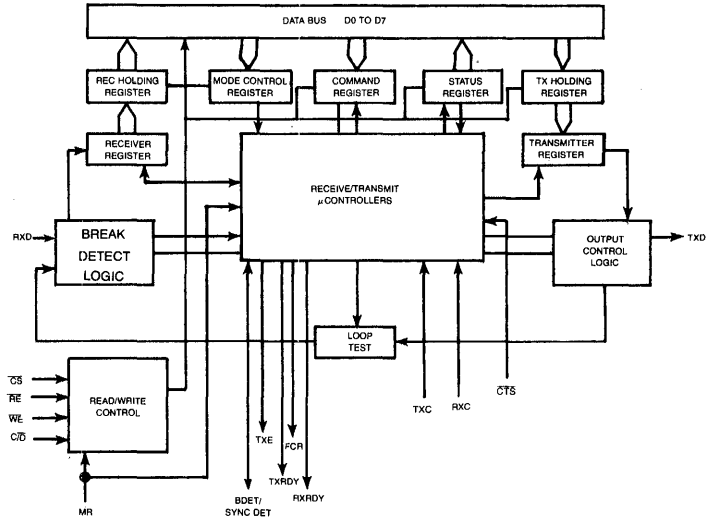


Figure 2 WD1984 BLOCK DIAGRAM

PIN NO.	SYMBOL	SIGNAL NAME	FUNCTION
1	VSS	GROUND	Ground
2	BDET/ SDET	BREAK DETECT/ SYNC DETECT	This pin is a bi-directional port. In ASYNC, it is an output, which goes high when the receiver logic detects a break character. In the SYNC mode, it is an input which causes the receiver to begin assembling data bytes as programmed.
3	$\overline{CTS}$	CLEAR-TO-SEND	This input is activated (V_{IL}) to enable the transmitter logic.
4	TXC	TRANSMIT CLOCK	This input is the source clock for transmission. The data rate is a function of this clock frequency. ASYNC MODE = 1× or 16× bit rate SYNC MODE = 16× bit rate
5	N.C.		No internal connection.
6	MR	MASTER RESET	When high (V_{IH}), presets the WD1984. The command register is set to 00100101 and the mode register is set to 00111100.
7	TXE	TRANSMITTER EMPTY	This output goes high to indicate the end of a transmit operation. TXE is automatically reset after the Transmit Holding Register is loaded.
8	RXRDY	RECEIVER READY	This output, when high, alerts the CPU that the Receiver Holding Register contains a data character that is ready to be input. This output is automatically reset whenever a character is read from the WD1984.
9	TXRDY	TRANSMITTER READY	This output, when high, alerts the CPU that the Transmit Holding Register is ready to accept a data character. The TXRDY output is automatically reset whenever a character is written into the WD1984 and can be used as an interrupt to the system.
10	N.C.		
11	TXD	TRANSMIT DATA ONE	This output is the serial data output.
12	RXC	RECEIVE CLOCK	This input is the source clock for reception. The data rate characteristics are the same as the transmit clock.
13	FCR/TIP	FIRST CHARACTER READY/TRANSMISSION IN PROGRESS	In the ASYNC mode, this output goes high after the receiver has completed reception of the first character in a multi-character sequence.
14	N.C.		
15	VCC	POWER SUPPLY	+5V DC
16	RXD	RECEIVE DATA ONE	This input is the serial data input.
17 18 19 20 21 22 23 24	D0 D1 D2 D3 D4 D5 D6 D7	DATA BUS	This is the bi-directional data bus. It is the means of communication between the WD1984 and the CPU. Control, Mode, Data and Status Registers are accessed via this bus.

PIN NO.	SYMBOL	SIGNAL NAME	FUNCTION
25	$\overline{WE}$	WRITE ENABLE	When low (V_{IL}), allows the CPU to write into the selected register.
26	$\overline{CS}$	CHIP SELECT	When low (V_{IL}), the device is selected. This enables communication between the WD1984 and a microprocessor.
27	C/$\overline{D}$	CONTROL/DATA	This input is used in conjunction with an active read or write operation to determine register access via the DATA BUS.
28	$\overline{RE}$	READ ENABLE	When low (V_{IL}), allows the CPU to read data or status information from the WD1984.

GENERAL DESCRIPTION

The WD1984 is a bus-oriented MOS/LSI device designed to provide two data communication protocols:

1. Asynchronous
2. Synchronous

The control registers are used to select the desired protocol and provide programmable format options within each protocol, as outlined below.

The WD1984 contains two control registers needed to specify formal options within each protocol. These registers are the command instruction register and the mode instruction register.

The format options available to the user are:

1) Parity Enable (PEN)

2) Parity Position (PIA)
The *P*arity bit (when enabled) can either be appended to the data word *A*fter the data bits or it can be *I*nside the data word in the last bit position.

3) Odd or Even Parity Select (EPS)

4) Character Length Select 5, 6, 7 or 8 Bits/Character) (CLS2 and CLS2)

The Asynchronous mode has the option of selecting the number of contiguous characters per transmission and receive sequence. This multicharacter option may facilitate data handling between peripheral devices with a non-standard number of data bits. Therefore, the user can change the mode register to transmit and receive any combination of one to eight characters per word and 5, 6, 7 or 8 bits per character.

Additionally, the Asynchronous mode has two options which determine the operational characteristics of the protocol:

1) Stop Bit Selection—(SPS)
This control bit selects 1 or 2 stop bits (1 or 1½ bits in 5 bit characters) at the end of the word, which is part of the character delimiting definition.

2) Asynchronous clock rate select (1× or 16× clock rate), which describes resolution and bit rate characteristics.

The WD1984 also contains a local loop-back test mode of operation, which is controlled by the Loop Test Enable (LTE) bit in the command register. In this diagnostic mode, the transmitter output is "looped-back" into the receiver input. The $\overline{REN}$ and TEN control bits must also be active ("1") and the $\overline{CTS}$ input must be low ("0"). The status and output flags operate normally.

ORGANIZATION

A block diagram of the WD1984 is shown in figure 1.

As mentioned, the WD1984 is an eight bit bus-oriented device. Communication between the WD1984 and the controlling CPU occurs via the 8 bit data bus through the bus transceivers. There are 2 accessible data registers, which buffer transmit and receive data. They are the Transmit Holding Register and the Receive Holding Register. There is a parallel-to-serial shift register (parallel in-serial out), the transmit register and a serial-to-parallel shift register (serial in-parallel out), the receive register.

Operational control and monitoring of the WD1984 is performed by two control registers (the command instruction register and the mode instruction register) and the status register.

A read/write control circuit allows programming/monitoring or loading/reading of data in the control, status or holding registers by activating the appropriate control lines: Chip Select ($\overline{CS}$), Read Enable ($\overline{RE}$), Write Enable ($\overline{WE}$) and Control or Data Select (C/$\overline{D}$).

Internal control of the WD1984 is by means of two internal microcontrollers; one for transmit and one for receive. The control registers, null detect logic and various counters, provide inputs to the microcontrollers which generate the necessary control signals to send and receive serial data according to the programmed protocols.

REGISTER DEFINITIONS

The format and definition of the Command Register is shown below:

TEN	Transmit ENable
1	Enabled
0	Disabled

PIA	Parity Inside or After
1	After the data word
0	Inside (the last data bit) of word

REN	Receive ENable
1	Enabled
0	Disabled

TXSM	Transmit Space or Mark
1	Send break character (force TXD low)
0	Normal transmitter operation

LTE	Loop Test ENable
1	Local loop-back mode
0	Normal Operation

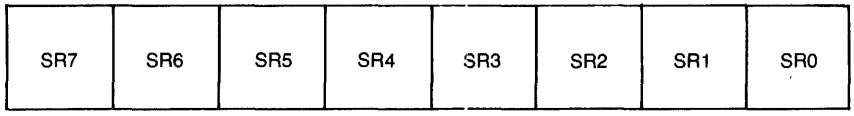
PEN	Parity ENable *
1	Enabled
0	Disabled

IR	Internal Reset
1	Returns WD1984 to mode instruction format
0	

EPS	Even Parity Select
1	Even parity
0	Odd parity

*Internally disabled in Synchronous mode.

The format of the Status Register is shown below:



TXRDY	Transmitter Ready
1	Active (THR can be reloaded)
0	Inactive (transmitter is busy)

RXRDY	Receiver Ready
1	Active (RHR should be read)
0	Inactive

TXE	Transmitter Empty
1	Transmitter idle
0	Transmitter active

PE	Parity Error
1	Error reported
0	No error

OE	Overrun Error
1	RHR has been overwritten
0	No error

FE	Framing Error
1	Indicates a framing error has been detected.
0	No error

BRKDET	Break Character Detect
1	In ASYNC mode, this bit indicates the receiver has detected a break character.
0	Inactive

UE	Underrun Error
1	In multi-character transmissions, indicates that the THR has not been loaded with a new character in time for a contiguous data transmission sequence.
0	No error

The format and definition of the Mode Register is shown below:

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
SBS	N3	N2	N1	CLS2	CLS1	MS2	MS1

MS2	MS1	Mode Selected
X	X	Undefined
0	0	Asynchronous mode (16X)
0	1	Asynchronous mode (1X)
1	X	Synchronous mode (16X)

CLS2	CLS1	Character Length Select
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

N3	N2	N1	Characters Per Word Select
0	0	0	1 character
0	0	1	2 characters
0	1	0	3 characters
0	1	1	4 characters
1	0	0	5 characters
1	0	1	6 characters
1	1	0	7 characters
1	1	1	8 characters

SBS	Stop Bit Select
1	2 stop bits (1-1/2 bits in 5 bit characters)
0	1 stop bit

The WD1984 registers are addressed according to the following table:

$\overline{CS}$	C/$\overline{D}$	$\overline{RE}$	$\overline{WE}$	Registers Selected
L	L	L	H	Read Receive Holding Register
L	L	H	L	Write Transmit Holding Register
L	H	L	H	Read Status Register
L	H	H	L	Write Control Registers
H	X	X	X	Data Bus Tri-Stated

L = V_{IL} at pins
H = V_{IH} at pins
X = don't care

ASYNCHRONOUS OPERATION

When the Asynchronous mode is selected, start, stop and parity bits are inserted as programmed. The receiver and transmitter clocks can be programmed as 1X or 16X. The transmitter output, TXD line will mark or space after transmission depending on command register programming. A line break condition can be programmed by setting the TXSM bit (command register bit CR3) to a logic "1". The TXD line will be forced to a low as long as this bit is logic "1". When the receiver detects the input line (RXD) low for a period equal to the word length including start, parity and stop bits, the break detect flag will become active.

The multi-character option is available to the Asynchronous protocol. The user can select any combination of one to eight characters per word and 5, 6, 7 or 8 bits per character. This allows a minimum word length of 5 bits and a maximum of 64 bits, plus parity, if enabled.

SYNCHRONOUS OPERATION

When the Synchronous mode is selected, start and stop bits are not transmitted. Parity is not available in Synchronous mode. The multi-character option is not available; however, the transmitter will continuously shift out data as long as the transmit holding register is buffered by the CPU. Two I/O sig-

nals are provided for synchronization, TIP (transmission in progress), an output which indicates that the transmitter is actively sending data and SYNCDET (SYNC detect), an input which notifies the receiver logic when to begin assembling characters.

Synchronization is obtained when the TIP signal from the transmitter is brought to the SYNCDET input of the associated receiver. Completion of a data transmission sequence occurs when the last character in the transmit register is sent and no further data is loaded into the transmit holding register. The TIP signal goes low. The receiver monitors the SYNCDET line and assembles data characters until it goes low, at which time it goes to an idle state.

PARITY MODES

The WD1984 is provided with some unique parity options as discussed above. If parity is enabled and the word length is eight bits, the parity is added to the transmitted word and stripped from the received word. When programmed for 5, 6 or 7 bits per character, the receiver checks and makes available the parity bit on the bus next to the MSB of data. Unused bits in an assembled character are zero when the receive holding register is read.

For example, in Asynchronous mode when two 8 bit characters are programmed with parity after the Data Word and two stop bits, 20 bits are transmitted. These are the Start bit, 16 Data bits, Parity and the 2 Stop bits. The Parity will be stripped off at the receiver since the character length is 8.

In Synchronous mode, Parity is not available and it is suggested the user provide his own software CRC as the last characters of his transmission.

OPERATING DESCRIPTION

The WD1984 is primarily designed to operate in an 8 bit micro-processor environment, although other control logic schemes are easily implemented. The DATA BUS and the Interface Control Signals ($\overline{CS}$, $\overline{RE}$, $\overline{WE}$ and $C/\overline{D}$) should be connected to the microprocessor's data bus and system control bus. The appropriate TXC and RXC clock frequencies should be selected for the particular application, using a programmable baud rate generator such as a BR1941. A master reset pulse initializes the WD1984 and presets the control registers to transmit and receive four 8-bit contiguous characters with the 32nd bit odd parity. If other protocols are desired, then the mode and command registers should be programmed as discussed previously.

For typical data communication applications, the RXD and TXD input/outputs can be connected to RS-232C interface circuits or a modem.

The TXRDY, RXRDY, FCR and FE/BRKDET Flags may be connected to the microprocessor system as interrupt inputs. The status register can be periodically read in a polled environment to support operations.

The $\overline{CTS}$ input can be used to synchronize the transmitter to external events.

The WD1984 is designed such that a control register write operation accesses the command instruction register. The mode instruction register is accessed by performing a control write operation setting the internal reset bit high, which allows the next control write operation to program the mode register. Subsequent control write operations will again access the command register until another internal reset is performed. Internal reset commands should also disable the receiver and transmitter until the new mode instruction is programmed. The next command should then reactivate the receiver and transmitter to resume operations. This minimizes any errors that may be generated as a result of an active receive line during reprogramming.

The TXSM bit of the command register causes the transmitter output to be forced low after the last word is transmitted. This is also used in Asynchronous mode to send a break character (all zero data and parity bits).

The receiver is equipped with logic to look for a break character in the Asynchronous mode. When a break character is received, the receiver activates the break detect flag and status bit. When the receiver input line goes high again for at least "one bit time", the receiver resets the break detect flag and resumes its search for a start bit.

MULTI-CHARACTER OPERATIONS

As discussed above, the WD1984 is equipped with a multi-character option which provides the user with the means of transmitting and receiving multiple contiguous characters of data within one set of start and stop bits. Since the WD1984 is an 8 bit bus-oriented device, the controlling processor must read the WD1984 data from its holding register before the subsequent characters are assembled. This situation also exists on the transmit side, i.e., the Transmit Holding Register must be loaded before the previous 8 bits are completely shifted out of the transmit register.

Several "flags" are provided for interrupt purposes so that continuity is maintained and data integrity is preserved. These flags are First Character Ready (FCR), Receiver Ready (RXRDY), Transmitter Ready (TXRDY) and Transmitter Empty (TXE).

The Transmitter operates as follows:

a) With the mode and command registers programmed as desired, the transmitter is enabled, TEN (CR0) = "1".

b) The TXE and TXRDY flags are "1" (active).

c) The external $\overline{CTS}$ signal = "0".

d) The CPU loads data into the Transmitter Holding Register, TXE and TXRDY go Low.

e) The data is loaded into the transmit register and TXRDY goes High. This indicates the first data word is being sent and the character can be loaded into the holding register. If the WD1984 is programmed for more than one character (multi-character) then an underrun error will be generated if the next character is not loaded before the previous word is completely shifted out, unless the current character is the last character in a sequence.

f) If the last character is transmitted and no more new data is to be sent, the transmitter will indicate its status

by raising the TXE flag. (No error is generated as a result of this condition.)

The Receiver operates similarly:

a) With the control registers suitably programmed, the receiver is enabled, REN (CR2) = "1".

b) The RXRDY and FCR flags are "0". (Inactive).

c) The incoming data word activates the receive logic and the data begins to be assembled in the receive register.

d) When the first character is completely assembled, the data is loaded into the Receive Holding Register, the FCR (First Character Ready) and RXRDY (Receiver Ready) flags become active, "1". The CPU should read the data prior to the reception of the next character or an overrun error will be generated as the receiver will overwrite the old data with the new data character just received.

LOOP TEST MODE:

As mentioned, the WD1984 is equipped with a diagnostic test mode, local loop-back. This mode is activated by setting the LTE command bit to a "1". The TEN and REN bits should be "1" and CTS should be "0". The receiver inputs are ignored and the transmitter outputs are held high V_{OH}. The transmitter is internally "looped-back" to the receiver and the error and status flags operate normally.

It is possible to program a test routine using the loop-back mode so that one can simulate "line breaks" and parity errors. This can be done using the TXSM command to interrupt a transmit sequence in "mid-stream", since setting the TXSM bit to a "1" while the transmitter is currently sending data will immediately cause zeroes to be sent until the TXSM bit is reprogrammed to a "0". This can only be done when in the loop-test mode, else the TXSM command is recognized only after the current transmission is complete.

For multicharacter operations, failing to reload the Transmit Holding Register in the middle of a data send sequence will cause an underrun error in the transmitter and a word error in the receiver. Failure to read the Receive Holding Register after a FCR or RXRDY flag will cause an overrun error to be generated.

For Loop-Back test operations, the user should be sure that the TXC and RXC clock frequencies are the same. This is normally implemented by placing the same clock signal on both pins (TXC and RXC).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic ("F" package) ..... −55°C to +125°C
Ceramic ("E" package) ..... −65°C to +150°C
Voltage on any Pin with respect to ground ... −0.5V to +7V
Power Dissipation 400MW

Absolute ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS

T_A=0°C to +70°C; V_{CC} =5.0V ± 5%; GND= 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITION
V_{IL}	Input Low Voltage	−0.5		.08	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −100μA
I_{DL}	Data Bus Leakage			−50	uA	V_{OUT} = 0.45V
				10	uA	V_{OUT} = V
I_{IL}	Input Leakage			10	uA	V_{IN} = V_{CC}
I_{CC}	Power Supply Current		45	80	mA	

CAPACITANCE

T_A = 25°C: V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITION
C_{IN}	Input Capacitance			10	pF	f_C = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

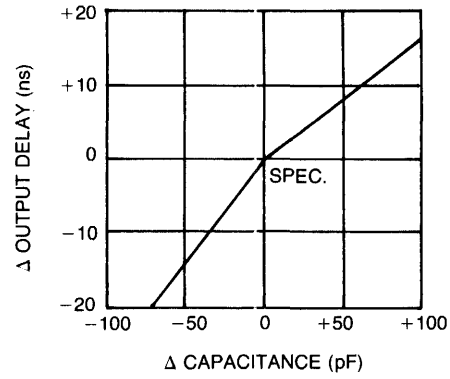


Figure 3 OUTPUT DELAY VS CAPACITANCE

A.C. TIMING PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
	BUS PARAMETERS Read Cycle (Reference Figure 5)				
t_{AR}	Address Stable before $\overline{RE}$, ($\overline{CS}$, C/$\overline{D}$)	50		ns	
t_{RA}	Address Hold Time for $\overline{RE}$, ($\overline{CS}$, C/$\overline{D}$)	5		ns	
t_{RE}	$\overline{RE}$ Pulse Width	350		ns	
t_{RD}	Data Delay from $\overline{RE}$		200	ns	C_L = 50 pF
t_{RDH}	$\overline{RE}$ to Data Floating	25	200	ns	C_L (Max) = 100 pF C_L (Min) = 50 pF
	WRITE CYCLE (Reference Figure 6)				
t_{AW}	Address Stable before $\overline{WE}$	20		ns	
t_{WA}	Address Hold Time for $\overline{WE}$	20		ns	
t_{WE}	$\overline{WE}$ Pulse Width	350		ns	
t_{DS}	Data Set-Up Time for $\overline{WE}$	200		ns	
t_{WDH}	Data Hold Time for $\overline{WE}$	40		ns	
	OTHER TIMINGS (Reference Figure 7, 8, 9)				
t_{DTX}	TXD Delay from Falling Edge of TXC		500	ns	C_L = 100 pF
t_{SRX}	RX Data Set-Up Time to Sampling Pulse	200		ns	C_L = 100 pF
t_{NRX}	RX Data Hold Time to Sampling Pulse	100		ns	C_L = 100 pF
t_{TX}	Transmitter Input Clock Frequency				
	1× Baud Rate	DC	500	kHz	
	4×, 16× Baud Rate	DC	750	kHz	
t_{TPW}	Transmitter Input Clock Pulse Width				
	1× Baud Rate	1.0		us	
	16× Baud Rate	500		ns	

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1× Baud Rate	1.0		us	
	16× Baud Rate	700		ns	
t_{Rx}	Receiver Input Clock Frequency				
	1× Baud Rate	DC	500	kHz	
	4×, 16× Baud Rate	DC	750	kHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1× Baud Rate	1.0		us	
	16× Baud Rate	500		ns	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1× Baud Rate	1.0		us	
	16× Baud Rate	700		ns	
				ns	
t_{TX}	TXRDY Delay from center of Data Bit	200 ns	½	t_{TXC}	(1x or 16x)

A.C. TIMING PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
t_{RX}	RxRDY Delay from Center of Data Bit (FCR Delay from Center of Data Bit)		½	R_{RXC}	
	Internal BRKDET Delay from Center of Data Bit		1	t_{RXC}	
	External SynDet Set-up time before rising edge of RXC	200		ns	
	TXEMPTY Delay from Center of Data Bit		½	t_{TXC}	C_L = 50 pF (1 × Rate)

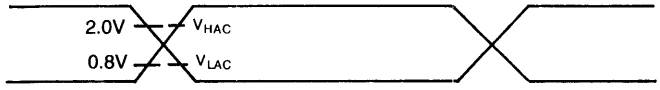


Figure 4 TEST POINTS FOR A.C. TIMING

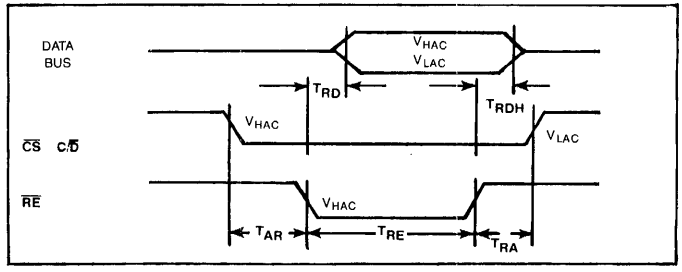


Figure 5 READ CYCLE TIMING

Note: AC timings measured at V_{OH} = 2.0V, V_{OL} = 0.8V

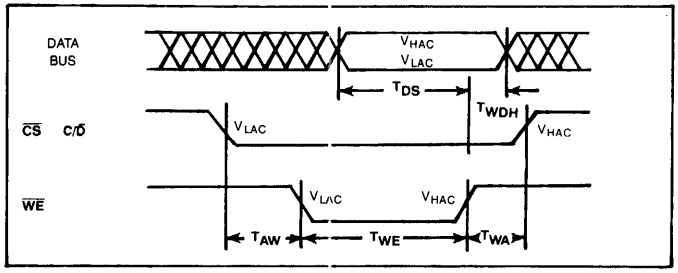


Figure 6 WRITE CYCLE TIMING

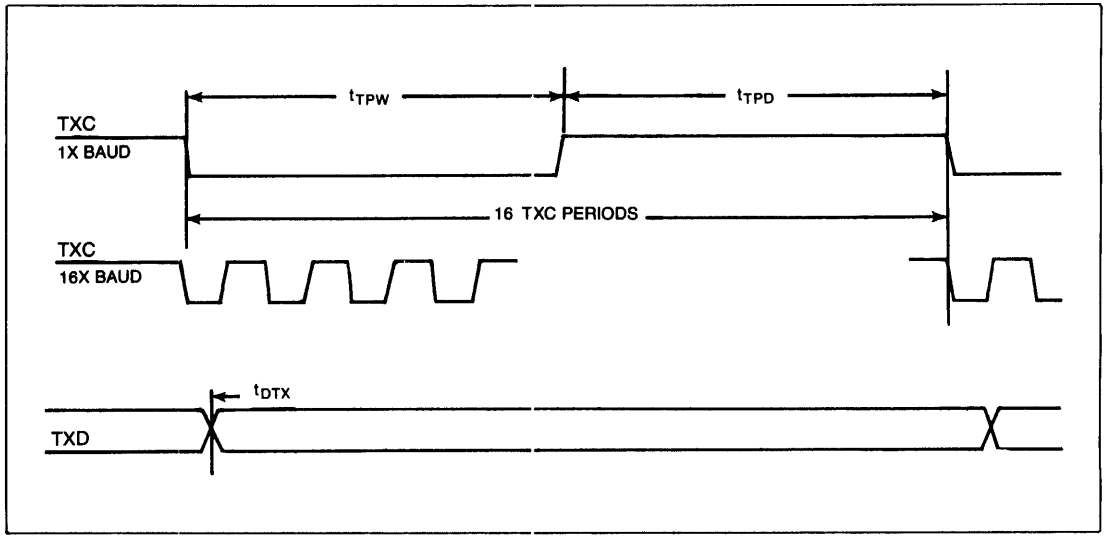


Figure 7 TRANSMITTER CLOCK AND DATA TIMINGS

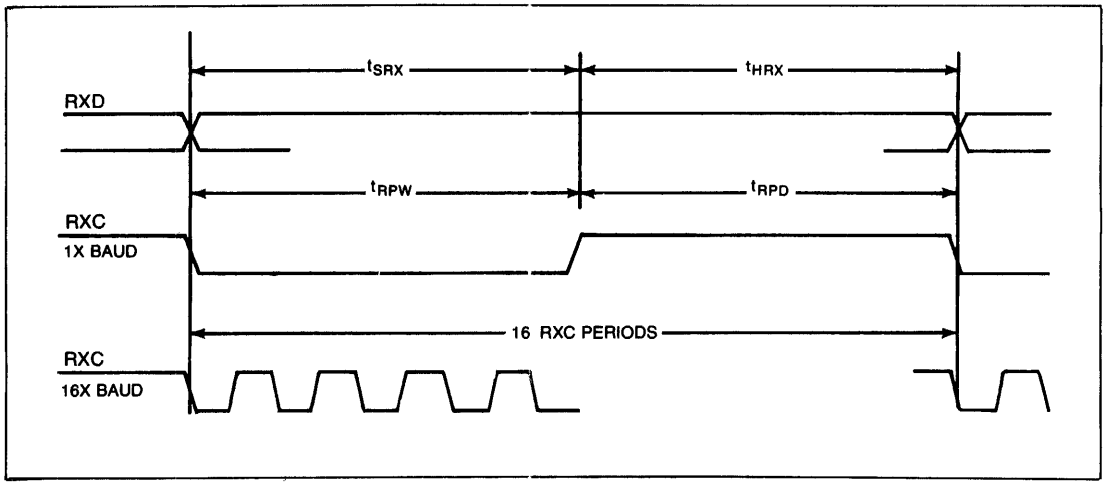


Figure 8 RECEIVER CLOCK AND DATA TIMINGS

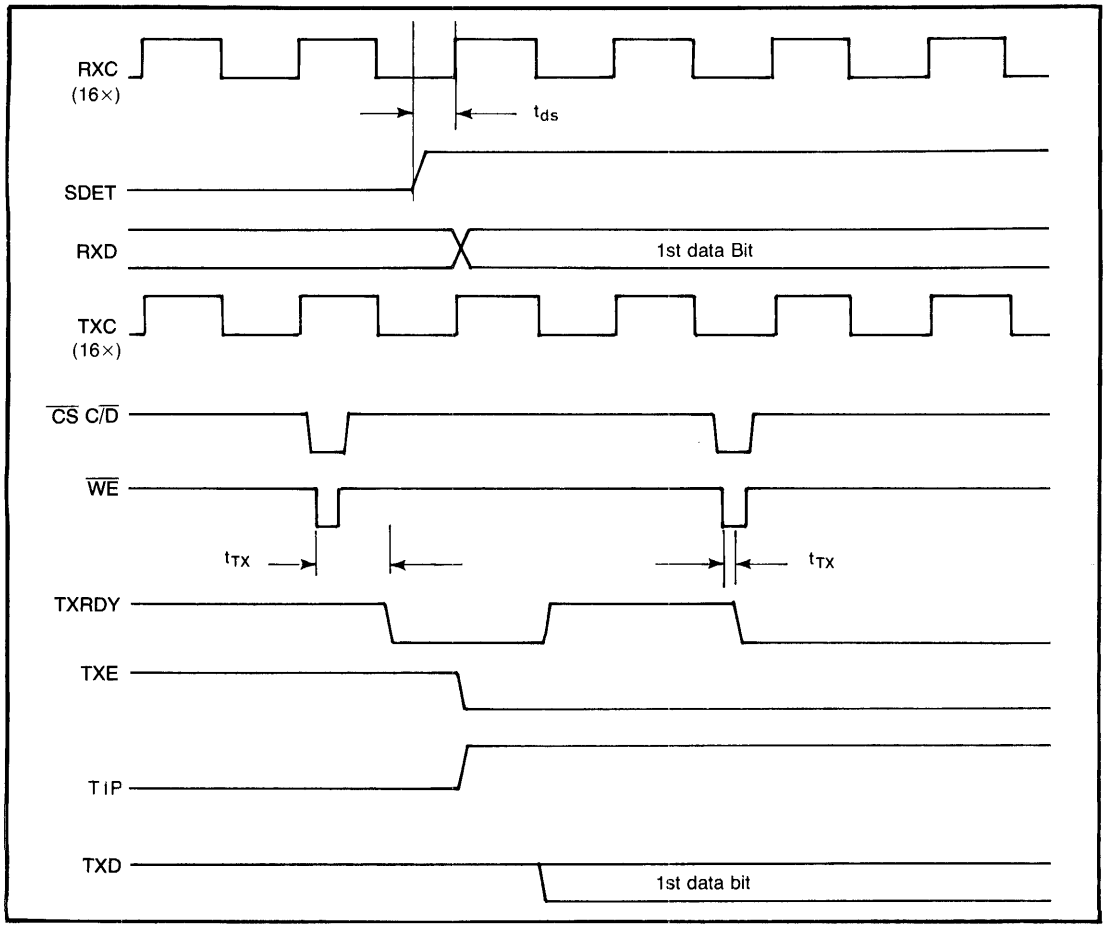


Figure 9 SYNCHRONOUS MODE TIMINGS

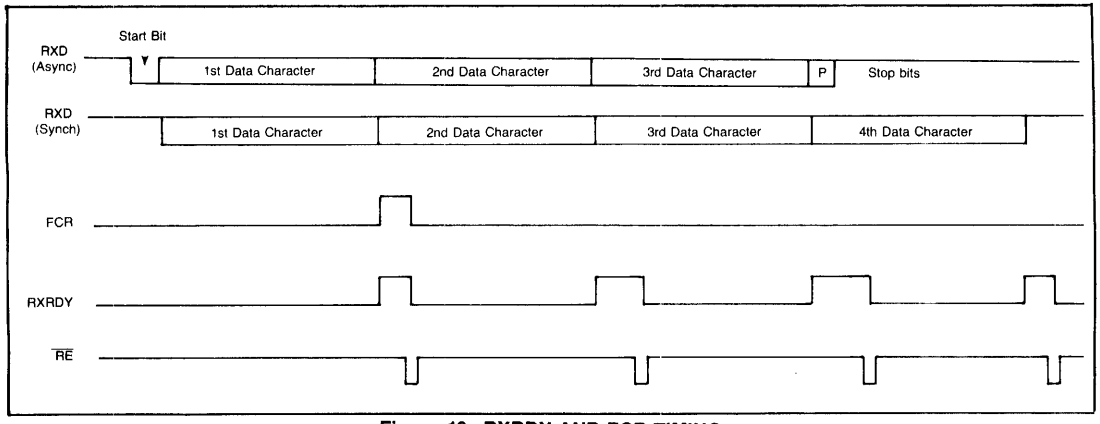


Figure 10 RXRDY AND FCR TIMING

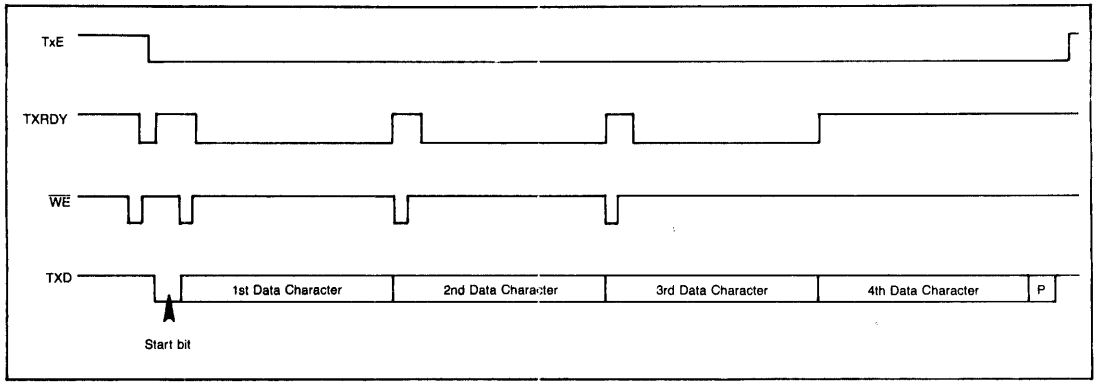


Figure 11 TXRDY AND TXE TIMINGS (4 CHARACTERS SEQUENCE)

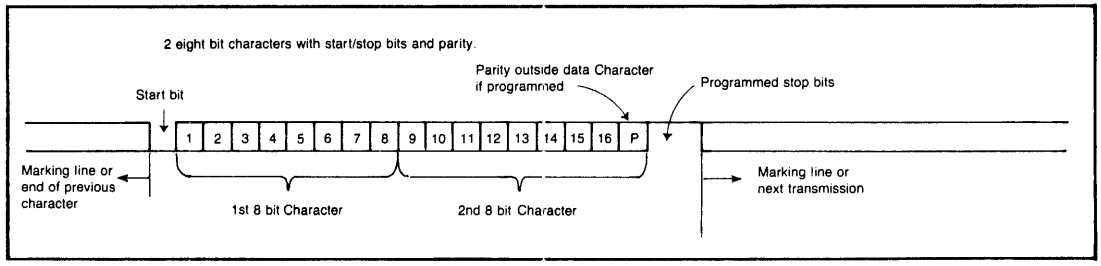


Figure 12 16 BIT ASYNCHRONOUS

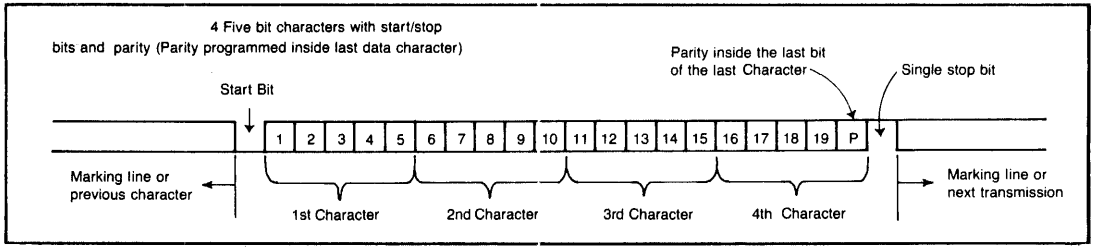


Figure 13 20 BIT ASYNCHRONOUS

See page 725 for ordering information.

Printed in U.S.A

Security Products

WD2001/WD2002 Data Encryption Devices

FEATURES

- CERTIFIED BY NATIONAL BUREAU OF STANDARDS.
- TRANSFER RATE:
  WD2001/2-05 300Kbs with 500KHz clock
  WD2001/2-20 1.3 Mbs with 2MHz clock
  WD2001/2-30 1.8 Mbs with 3MHz clock
- ENCRYPTS/DECRYPTS 64 BIT DATA WORDS USING 56 BIT KEY WORD
- SINGLE PORT 28 PIN PACKAGE WD2001 OR DUAL PORT 40 PIN PACKAGE WD2002
- COMMAND BIT PROGRAMMING VIA DAL BUS OR INPUT PINS
- DMA COMPATIBLE (SEE WESTERN DIGITAL DM1883)
- PARITY CHECK ON KEY WORD LOADING
- STANDARD 8 BIT MICROPROCESSOR INTERFACE
- INPUTS AND OUTPUTS TTL COMPATIBLE
- KEY STORED ON CHIP IS NOT EXTERNALLY ACCESSIBLE

  SEPARATE CLEAR AND CIPHER BUS STRUCTURE ON WD2002

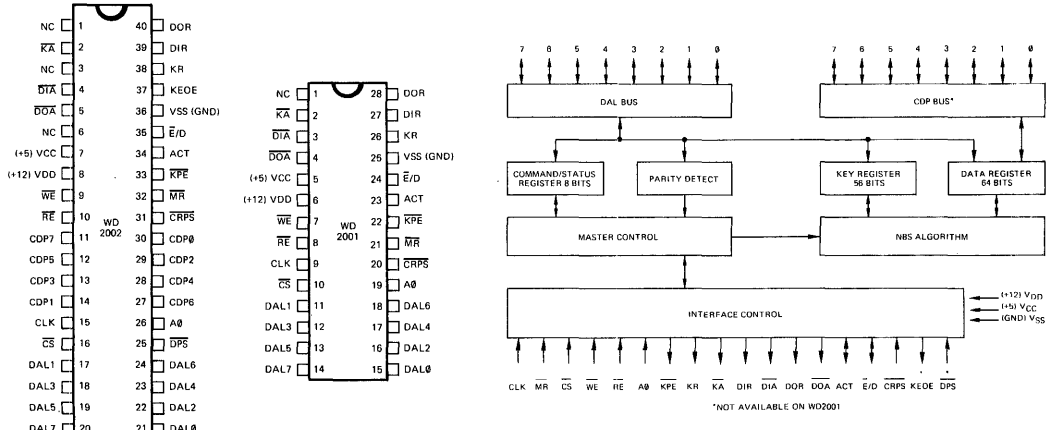
APPLICATIONS

- SECURE BROKERAGE TRANSACTIONS
- ELECTRONIC FUNDS TRANSFERS
- SECURE BANKING/BUSINESS ACCOUNTING
- MAINFRAME COMMUNICATIONS
- REMOTE AND HOST COMPUTER COMMUNICATIONS
- SECURE A/D
- SECURE DISK OR MAG TAPE DATA STORAGE
- SECURE PACKET SWITCHING TRANSMISSION

GENERAL DESCRIPTION

The Western Digital WD2001 and WD2002 Data Encryption/Decryption devices are designed to encrypt and decrypt 64-bit blocks of data using the algorithm specified in the Federal Information Processing Data Encryption Standard (#46). These devices encrypt a 64-Bit clear text word using a 56-Bit user-specified key to produce a 64-Bit cipher text word. When reversed, the cipher text word is decrypted to produce the original clear text word.

The DE2001/2 are fabricated in N-channel silicon gate MOS technology and are TTL compatible on all inputs and outputs.



WD2001/WD2002 BLOCK DIAGRAM

PIN OUTS

PIN NO. WD2001	PIN NO. WD 2002	PIN NAME	SYMBOL	FUNCTION
11-18	17-24	DATA LINES	DAL 0 → DAL 7	Eight active true three-state bi-directional I/O lines used for information transfer to and from the DES chip's registers. During single port operation, all COMMAND/STATUS, KEY WORD and DATA WORD transfers are via this bus. During dual port operation, all COMMAND/STATUS, KEY WORD and clear DATA WORD transfers are via this bus. (Cipher DATA WORD transfers are via the CIPHER DATA PORT (CDP) bus.)
N/A	11-14 27-30	CIPHER DATA PORT	CDP 0 → CDP 7	Eight active true three-state bi-directional I/O lines used only in dual port operation. Cipher DATA WORD transfers are via this bus. These pins are available on the WD2002 40 pin package version only.
6	8	POWER SUPPLY	V_{DD}	+ 12v
5	7	POWER SUPPLY	V_{CC}	+ 5v
25	36	GROUND	V_{SS}	GROUND
9	15	CLOCK	CLK	System clock input.
21	32	$\overline{\text{MASTER RESET}}$	$\overline{\text{MR}}$	$\overline{\text{MR}}$ active low resets the COMMAND/STATUS REGISTER and resets internal circuitry. (Requires active clock for reset operation.)
10	16	$\overline{\text{CHIP SELECT}}$	$\overline{\text{CS}}$	$\overline{\text{CS}}$ is made low to access registers within the device.
8	10	$\overline{\text{READ ENABLE}}$	$\overline{\text{RE}}$	The contents of the selected register are placed on the DAL (or CDP) bus lines when $\overline{\text{CS}}$ and $\overline{\text{RE}}$ are made low.
7	9	$\overline{\text{WRITE ENABLE}}$	$\overline{\text{WE}}$	Information on the DAL (or CDP) bus lines is written into the selected DES register when $\overline{\text{CS}}$ and $\overline{\text{WE}}$ are made low.
19	26	A0	A0	When this input is active high (during $\overline{\text{CS}}$ active) the COMMAND/STATUS REGISTER is addressed. (A0 active high will override internally generated addressing of the KEY and DATA REGISTERS as described on page 6.) This input is ignored when $\overline{\text{CRPS}}$ is active.
26	38	KEY REQUEST	KR	This output is active high when the DES chip is requesting that a byte of the KEY WORD be written into the KEY REGISTER. (The KEY REGISTER is automatically addressed when KR is active, unless overriden by A0.)
2	2	$\overline{\text{KEY ACKNOWLEDGE}}$	$\overline{\text{KA}}$	This output is active low when $\overline{\text{WE}}$ is made low while the KEY REGISTER is addressed. (Can be used for handshake.)
27	39	DATA-IN REQUEST	DIR	This output is active high when the DES chip is requesting that a byte of the DATA WORD be written into the DATA REGISTER. (The DATA REGISTER is automatically addressed when DIR is active, unless overriden by A0.)
3	4	$\overline{\text{DATA-IN}}$ $\overline{\text{ACKNOWLEDGE}}$	$\overline{\text{DIA}}$	This output is active low when $\overline{\text{WE}}$ is made low while the DATA REGISTER is addressed. (Can be used for handshake.)

PIN NO.		PIN NAME	SYMBOL	FUNCTION
WD2001	WD2002			
28	40	DATA-OUT REQUEST	DOR	This output is active high when the DES chip is requesting that a byte of the DATA WORD be read from the DATA REGISTER. (The DATA REGISTER is automatically addressed when the DOR is active, unless overridden by A0.)
4	5	$\overline{\text{DATA-OUT ACKNOWLEDGE}}$	$\overline{\text{DOA}}$	This output is active low when $\overline{\text{RE}}$ is made low while the DATA REGISTER is addressed. (Can be used for handshake.)
22	33	$\overline{\text{KEY PARITY ERROR}}$	$\overline{\text{KPE}}$	This output is active low when enabled via the COMMAND/STATUS REGISTER BIT 2 (KEOE) and a parity error has been detected during loading of the KEY REGISTER.
20	31	$\overline{\text{COMMAND REGISTER PIN SELECT}}$	$\overline{\text{CRPS}}$	This input selects DAL bus or input pin programming of the COMMAND/STATUS REGISTER. $\overline{\text{CRPS}}$ high or open selects DAL bus programming. $\overline{\text{CRPS}}$ low selects input pin programming.
23	34	ACTIVATE	ACT	When $\overline{\text{CRPS}}$ is high or open, this pin is an output reflecting the status of the ACTIVATE bit (bit 1) of the COMMAND/STATUS REGISTER. When $\overline{\text{CRPS}}$ is low, this pin is an input that overrides the ACTIVATE bit of the COMMAND/STATUS REGISTER.
N/A	37	KEY ERROR OUTPUT ENABLE	KEOE	This output indicates the status of the KEY ERROR OUTPUT ENABLE bit (bit 2) of the COMMAND/STATUS REGISTER. This output is active when input pin programming is selected ($\overline{\text{CRPS}}$ low). This pin is available on the WD2002 40 pin package version only.
24	35	$\overline{\text{ENCRYPT}}$/DECRYPT	$\overline{\text{E}}$/D	When $\overline{\text{CRPS}}$ is high or open, this pin is an output reflecting the status of the $\overline{\text{ENCRYPT}}$/DECRYPT bit (bit 3) of the COMMAND/STATUS REGISTER. When $\overline{\text{CRPS}}$ is low, this pin is an input pin that overrides the $\overline{\text{ENCRYPT}}$/DECRYPT bit of the COMMAND/STATUS REGISTER.
N/A	25	$\overline{\text{DUAL PORT SELECT}}$	$\overline{\text{DPS}}$	When this input is high or open, single port operation is selected and all DES chip transfers are via the DAL bus. When $\overline{\text{DPS}}$ is low, dual port operation is selected and both the DAL bus and the CDP bus are used [separate busses for clear data (DAL bus) and cipher data (CDP bus)]. This pin is available on the WD2002 40 pin package version only.

NOTE: The WD2001 28 pin package version does not have the following pins:
The 8 CDP pins, the KEOE pin, and the $\overline{\text{DPS}}$ pin.

ORGANIZATION

The Data Encryption Standard chip consists of a 56-bit KEY REGISTER, a 64-bit DATA REGISTER, an 8-bit COMMAND/STATUS REGISTER, plus the necessary logic to check KEY parity and implement the NBS algorithm. A typical system implementation is shown on page 10 and the block diagram is shown on page 1. Although the DES chip interfaces to a wide variety of processors including mini-computers, the interface is tailored to the 8080A class microprocessor.

GENERAL OPERATING DESCRIPTION

The user programs the DES chip for encryption or decryption, and single or dual port operation.* Data is encrypted/decrypted with a 64-bit user defined KEY WORD. Data encrypted with a given KEY WORD can be decrypted only using that KEY WORD. The KEY REGISTER is loaded by the computer with eight successive 8-bit bytes. Parity is checked on each byte of the KEY WORD as it is loaded into the KEY REGISTER (The 8th bit (DAL0) of each 8-bit byte is reserved for odd parity for that byte and is not used in the algorithm calculation.) Similarly the DATA REGISTER is loaded with eight successive 8-bit bytes. The DATA REGISTER is read by reading eight successive 8-bit bytes.

When the DES chip is programmed for encryption, the DATA REGISTER is loaded with eight bytes of plain or clear text. The DES chip encrypts the data, then the encrypted data may be read from the DATA REGISTER (64-bits of encrypted text). When the DES chip is programmed for decryption, the DATA REGISTER is loaded with eight bytes of encrypted or cipher text. The DES chip decrypts the data, then the plain text may be read from the DATA REGISTER (64-bits of plain text). Note that all transfers to and from the KEY REGISTER and/or DATA REGISTER must occur in eight successive 8-bit bytes.

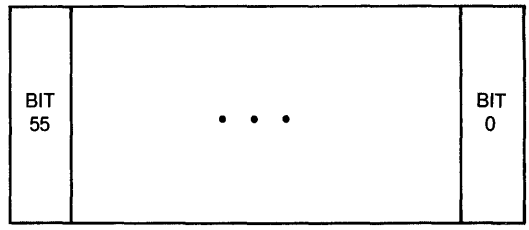
***Note:** Dual port operation available with WD2002 40 pin package version only. (Single and dual port operation is described in detail under PART V. OPERATION.)

REGISTER DESCRIPTION

The following describes the KEY, DATA, and COMMAND/STATUS REGISTERS of the DES chip.

Key Register

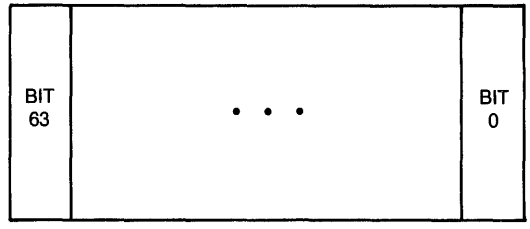
This 56-bit register contains the KEY by which the Data Encryption Algorithm operates. Eight successive bytes are needed to load the KEY REGISTER. The KEY REGISTER can be loaded only when there is a KEY REQUEST (Status bit and output). THIS REGISTER IS LOAD ONLY AND CANNOT BE READ.



KEY REGISTER (LOAD ONLY)

Data Register

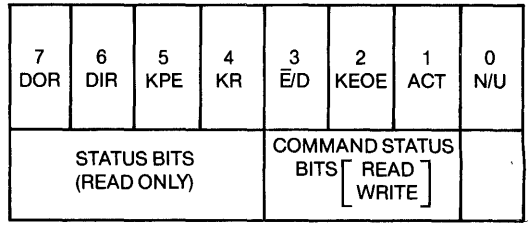
This 64-bit register contains plain or cipher text. When in the encrypt mode, the DATA REGISTER is loaded with plain text, and when read contains cipher text. When in the decrypt mode, the DATA REGISTER is loaded with cipher text, and when read contains plain text. The DATA REGISTER is always read or loaded with eight successive byte transfers. The DATA REGISTER can be loaded only when there is a DATA-IN REQUEST (status bit and output); similarly the DATA REGISTER can be read only when there is a DATA-OUT REQUEST (status bit and output).



DATA REGISTER

Command/Status Register (C/S R)

This 8-bit register controls the operation of the DES chip and monitors its status. Bits 7, 6, 5 and 4 are status-only bits (read only). Bits 3, 2 and 1 are COMMAND/STATUS bits (read/write). Bit 0 is not used. The COMMAND/STATUS bits (bits 3, 2, and 1) are normally loaded only once for an entire encrypt or decrypt process.



COMMAND/STATUS REGISTER

COMMAND/STATUS REGISTER (C/S R)

Bit	Name	Function
C/S R0	NOT USED	
C/S R1	ACTIVATE	This bit must be set from '0' to '1' to initiate loading the KEY REGISTER. This bit must be '1' for encrypt/decrypt operation. This is a read/write bit.
C/S R2	KEY ERROR OUTPUT ENABLE (KEOE)	When '0', the $\overline{\text{KEY PARITY ERROR}}$ output pin ($\overline{\text{KPE}}$) remains inactive regardless of the status of the $\overline{\text{KEY PARITY ERROR}}$ bit (bit 5). When '1', the $\overline{\text{KEY PARITY ERROR}}$ output pin is active when the KPE bit (bit 5) is '1'. This bit is set to '1' upon a MASTER RESET. This is a read/write bit.
C/S R3	$\overline{\text{ENCRYPT}}$/DECRYPT ($\overline{\text{E}}$/D)	When '0' data is to be encrypted. When '1' data is to be decrypted. This is a read/write bit.
C/S R4	KEY REQUEST (KR)	This bit is set one clock period after the ACTIVATE bit is set (from '0' to '1'). It is reset upon loading of the 8th and final byte of the KEY REGISTER. This is a read only bit.
C/S R5	KEY PARITY ERROR (KPE)	This bit is set internally upon detection of a parity error during loading of the KEY REGISTER. It is reset when the ACTIVATE bit is programmed from '1' to '0' (i.e., chip is deactivated). This is a read only bit.
C/S R6	DATA-IN REQUEST (DIR)	This bit is set upon either: a) Completion of KEY REGISTER loading - or - b) Completion of DATA REGISTER reading, (ie, the last DATA-OUT REQUEST has been serviced by an 8-byte read and the DATA REGISTER is now empty and ready to be loaded with the next DATA WORD). It is reset upon loading of the 8th and final byte of the DATA REGISTER. This is a read only bit.
C/S R7	DATA-OUT REQUEST (DOR)	This bit is set upon completion of the internal encrypt/decrypt calculation of a DATA WORD. It is reset upon reading of the 8th and final byte of the DATA REGISTER. This is a read only bit.

Note: All bits of the COMMAND/STATUS REGISTER are reset to '0' upon MASTER RESET, except bit 2 (KEOE) which is set to '1' and bit 0 (not used) which will read '1' by default during a COMMAND/STATUS REGISTER read.

DETAILED OPERATING DESCRIPTION

The DES chip is initiated by programming a '1' in the ACTIVATE bit of the COMMAND/STATUS REGISTER. The DES chip will respond by activating the KEY REQUEST (KR) bit (bit 4) of the STATUS REGISTER and the KEY REQUEST output.

The user must deactivate A0 (allowing the chip to internally address the KEY REGISTER), and load the KEY REGISTER with the 64-bit KEY WORD. The KEY REGISTER is loaded with 8 consecutive 8-bit bytes by activating $\overline{WE}$ 8 times (with $\overline{CS}$ active).

When $\overline{WE}$ is made active, the DES chip deactivates the KR output. When $\overline{WE}$ is deactivated, the KR output is again activated. The DES chip will activate 8 KEY REQUESTs in this fashion until the KEY REGISTER is full.

Also, when $\overline{WE}$ is made active, the DES chip responds by activating the $\overline{KEY\ ACKNOWLEDGE}$ ($\overline{KA}$) output. Thus, 8 $\overline{KA}$ activations will be made.

The KR and $\overline{KA}$ outputs can be used for asynchronous handshaking (as in DMA control) or further activations following the first KR can be ignored and the KEY REGISTER can be loaded in a synchronous (programmed I/O) manner via 8 successive activations of $\overline{WE}$.

Each byte of the KEY WORD is checked for odd parity as it is loaded. If a parity error is found, the chip will set the KEY PARITY ERROR (KPE) bit (bit 5) of the COMMAND/STATUS REGISTER. If the KEY ERROR OUTPUT ENABLE bit (bit 2) of the COMMAND/STATUS REGISTER has been set, the DES chip will also activiate the $\overline{KPE}$ output. The KPE bit will be reset when the ACTIVATE bit is re-programmed to a '0'.

After loading the last (8th) byte of the KEY WORD into the KEY REGISTER, the DES chip will set the DATA-IN REQUEST bit (bit 6) of the STATUS REGISTER and activate the DATA-IN REQUEST (DIR) output. The 64-bit DATA WORD must then be loaded into the DATA REGISTER. The DATA REGISTER is loaded in the same manner as the KEY REGISTER via 8 successive activations of DATA-IN REQUEST (DES output), $\overline{WE}$ (DES input, and DATA-IN ACKNOWLEDGE (DES output).

After the last (8th) byte of the DATA WORD has been loaded, the chip begins the internal calculation of the NBS algorithm. Upon completion of the calculation, the new data is internally loaded into the DATA REGISTER, and the DES chip sets the DATA-OUT REQUEST bit (bit 7) of the STATUS REGISTER and activates the DATA-OUT REQUEST (DOR) output. The DATA WORD must then be read from the DATA REGISTER. The DATA REGISTER is read in the same manner as it was loaded via 8 successive activations of DATA-OUT REQUEST (DES output), $\overline{RE}$ (DES input), and $\overline{DATA\text{-}OUT\ ACKNOWLEDGE}$ (DES output).

Again, for both data-in and data-out, further activations of the DIR, DOR and $\overline{DIA}$, $\overline{DOA}$ outputs, after the first request, can be ignored and the DATA REGISTER loaded (read) by 8 successive activations of $\overline{WE}$ ($\overline{RE}$).

After the last (8th) byte of the DATA REGISTER has been read, the DES chip will reactivate the DATA-IN REQUEST. This cycle of loading the DATA REGISTER, internal algorithm calculation, and reading the new data from the DATA REGISTER can continue indefinitely until all desired data has been encrypted or decrypted with the current KEY WORD.

After all desired data has been encrypted/decrypted with the current KEY WORD, the ACTIVATE bit of the COMMAND/STATUS REGISTER should be programmed to '0'. When the ACTIVATE bit has been reset to '0', an unauthorized user will not have access to the last KEY loaded into the DES chip since to resume operation, the ACTIVATE bit must be programmed to '1' which activates KEY REQUEST and a new KEY must be loaded before access to the DATA REGISTER is possible.

To encrypt plain data, plain data is loaded into the DATA REGISTER, and encrypted data is read from the DATA REGISTER. (The $\overline{ENCRYPT}$/DECRYPT bit (bit 3 of the COMMAND/STATUS REGISTER) must have been previously programmed to '0'.)

To decrypt encrypted data, encrypted data is loaded into the DATA REGISTER, and plain data is read from the DATA REGISTER. (The $\overline{ENCRYPT}$/DECRYPT bit must have been previously programmed to '1'.)

Note: If it is desired to switch from encrypt to decrypt (or vice versa) under the same KEY WORD, this can be accomplished before a DATA WORD transfer is initiated. By making A0 high, the DES chip will override the internal addressing of the DATA REGISTER, and address the COMMAND/STATUS REGISTER. The COMMAND/STATUS REGISTER can be re-programmed. When A0 is returned to a low state, the DES chip will internally address the DATA REGISTER awaiting loading of the next DATA WORD.

DUAL PORT OPTION

(Available on WD2002 40 Pin Version Only)

When the $\overline{DUAL\ PORT\ SELECT}$ ($\overline{DPS}$) input is high or left open (ie., single port operation is selected), all transfers to/from the DES chip are via the DAL bus. The CDP bus is not used and remains three-stated.

When $\overline{DPS}$ is made low (ie., dual port operation is selected), all transfers to/from the COMMAND/STATUS REGISTER, and transfers to the KEY REGISTER are still via the DAL bus. Clear DATA WORDS are also transferred via the DAL bus. However, cipher DATA WORDS are now transferred via the CDP bus. This provides separate busses for clear and ciphered text.

Encryption during dual port operation requires loading clear data via the DAL bus, and reading cipher data via the CDP bus.

Decryption during dual port operation requires loading cipher data via the CDP bus, and reading clear data via the DAL bus.

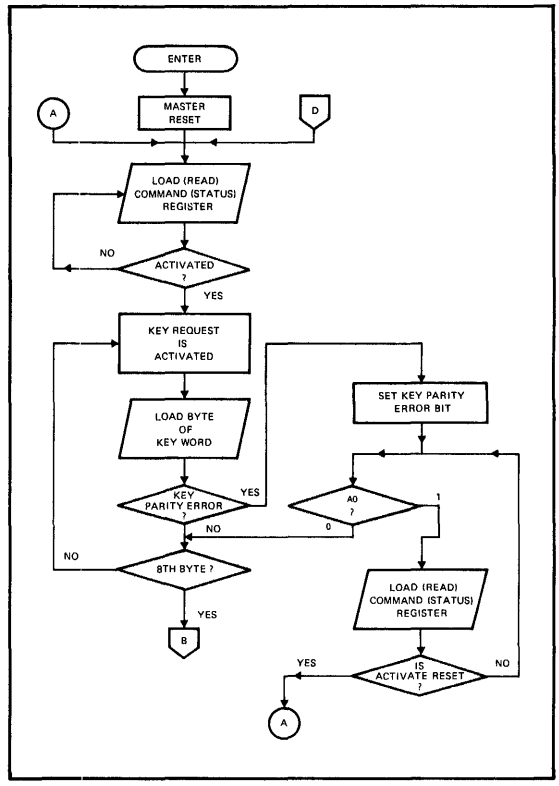
COMMAND SELECT OPTION

When the $\overline{\text{COMMAND REGISTER PIN SELECT}}$ ($\overline{\text{CRPS}}$) input is made low, the ACT and $\overline{E}$/D pins are enabled as inputs. These inputs override bits 1 and 3 (respectively) of the COMMAND/STATUS REGISTER. This allows input pin control of the DES chip. The KEOE bit (bit 2) of the COMMAND/STATUS REGISTER will be held to '1'.

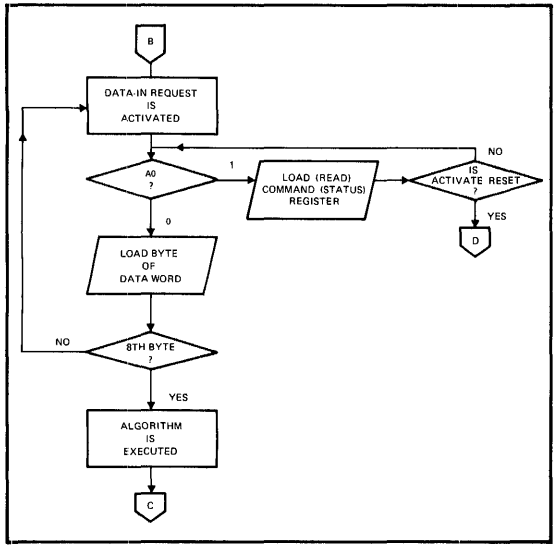
Input A0 will be disregarded in this mode of operation, and the COMMAND/STATUS REGISTER cannot be accessed via the DAL lines.

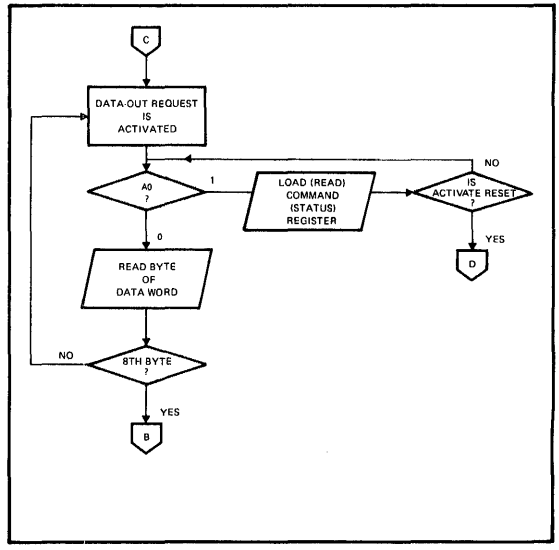
Note that the ACT pin must be toggled from '1' to a '0' to clear a parity error detection in this mode of operation.

All other operation remains as described previously.



WD2001/WD2002 FLOW CHARTS





MAXIMUM RATINGS

V_{DD} with Respect to V_{SS} (Ground)	+15 to - 0.3V	Storage Temp. Ceramic	-65°C to +150°C
Max. Voltage to any Input with Respect to V_{SS}	+15 to - 0.3V	Plastic	-55°C to +125°C
Operating Temperature	0°C to 70°C		
Power Dissipation	1 W		

OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12.0V ± .6V, V_{CC} = + 5.0V ± .25V, V_{SS} = OV

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	uA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	uA	$V_{OUT} = V_{CC}$
I_{CCAVE}	V_{CC} Supply Current		68	100	mA	
I_{DDAVE}	V_{DD} Supply Current		17	25	mA	
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage (All Inputs)			.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = -100uA
V_{OL}	Output Low Voltage			.4	V	I_O = 1.6 mA

2001/2002-05 500KHz CLOCK

AC CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12.0V ± 0.6V, V_{SS} = OV, V_{CC} = +5.0 ± .25V

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
READ						
T_{ACS}	A0, $\overline{CS}$ Set up to $\overline{RE}\downarrow$	100			ns	
T_{RDV}	$\overline{RE}\downarrow$ to DAL (CDP) Valid			500	ns	C_{LOAD} = 50PF
T_{RD}	$\overline{RE}$ Pulse Width	500			ns	
T_{DF}	$\overline{RE}\uparrow$ to DAL Float	50		250	ns	
T_{ACH}	A0, $\overline{CS}$ Hold From $\overline{RE}\uparrow$	0			ns	
WRITE						
T_{ACS}	A0, $\overline{CS}$ Set up to $\overline{WE}\downarrow$	100			ns	
T_{DVW}	DAL (CDP) Set up to $\overline{WE}\uparrow$	300			ns	
T_{WR}	$\overline{WE}$ Pulse Width	300			ns	
T_{DH}	DAL (CDP) Hold From $\overline{WE}\uparrow$	90			ns	
T_{ACH}	A0, $\overline{CS}$ Hold From $\overline{WE}\uparrow$	0				
HAND-SHAKE						
T_D	KR (DIR)↓, $\overline{KA}$ (DIA)↓ From $\overline{WE}\downarrow$ KR (DIR)↑, $\overline{KA}$ (DIA)↑ From $\overline{WE}\uparrow$ DOR↓, $\overline{DOA}$↓ From $\overline{RE}\downarrow$ DOR↑, $\overline{DOA}$↑ From $\overline{RE}\uparrow$		450	700	ns	C_{LOAD} = 50PF

NOTE: All output timing specifications reflect the following: High Output 2.0V
Low Output 0.8V

2001/2002-20 2MHz CLOCK

AC CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12.0V ± 0.6V, V_{SS} = OV, V_{CC} = +5.0 ± .25V

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
READ						
T_{ACS}	A0, $\overline{CS}$ Set up to $\overline{RE}\downarrow$	80			ns	
T_{RDV}	$\overline{RE}\downarrow$ to DAL (CDP) Valid			330	ns	C_{LOAD} = 50PF
T_{RD}	$\overline{RE}$ Pulse Width	330			ns	
T_{DF}	$\overline{RE}\uparrow$ to DAL Float	30		200	ns	
T_{ACH}	A0, $\overline{CS}$ Hold From $\overline{RE}\uparrow$	0			ns	
WRITE						
T_{ACS}	A0, $\overline{CS}$ Set up to $\overline{WE}\downarrow$	80			ns	
T_{DVW}	DAL (CDP) Set up to $\overline{WE}\uparrow$	200			ns	
T_{WR}	$\overline{WE}$ Pulse Width	200			ns	
T_{DH}	DAL (CDP) Hold From $\overline{WE}\uparrow$	90			ns	
T_{ACH}	A0, $\overline{CS}$ Hold From $\overline{WE}\uparrow$	0				
HAND-SHAKE						
T_D	KR (DIR)↓, $\overline{KA}$ ($\overline{DIA}$)↓ From $\overline{WE}\downarrow$ KR (DIR)↑, $\overline{KA}$ ($\overline{DIA}$)↑ From $\overline{WE}\uparrow$ DOR↓, $\overline{DOA}\downarrow$ From $\overline{RE}\downarrow$ DOR↑, $\overline{DOA}\uparrow$ From $\overline{RE}\uparrow$		300	450	ns	C_{LOAD} = 50PF

NOTE: All output timing specifications reflect the following: High Output 2.0V
Low Output 0.8V

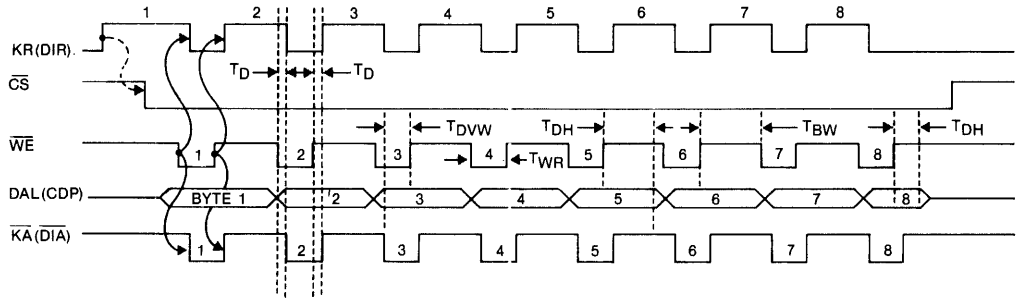
2001/2002-30 3MHz CLOCK

AC CHARACTERISTICS

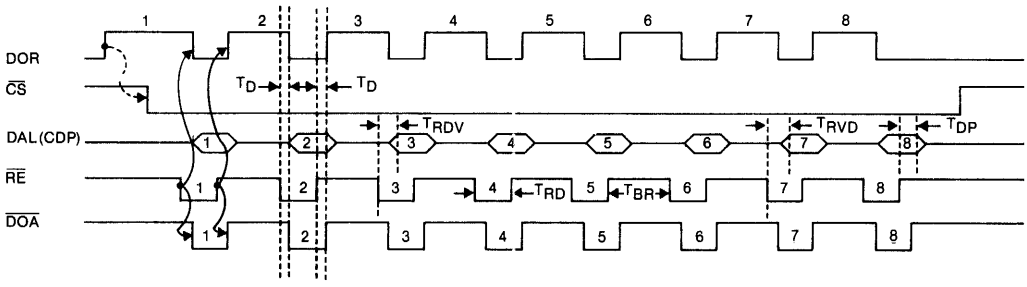
T_A = 0°C to 70°C, V_{DD} = +12.0V ± 0.6V, V_{SS} = OV, V_{CC} = +5.0 ± .25V

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
READ						
T_{ACS}	A0, $\overline{CS}$ Set up to $\overline{RE}\downarrow$	50			ns	
T_{RDV}	$\overline{RE}\downarrow$ to DAL (CDP) Valid			220	ns	C_{LOAD} = 50PF
T_{RD}	$\overline{RE}$ Pulse Width	300			ns	
T_{DF}	$\overline{RE}\uparrow$ to DAL Float	20		130	ns	
T_{ACH}	A0, $\overline{CS}$ Hold From $\overline{RE}\uparrow$	0			ns	
WRITE						
T_{ACS}	A0, $\overline{CS}$ Set up to $\overline{WE}\downarrow$	50			ns	
T_{DVW}	DAL (CDP) Set up to $\overline{WE}\uparrow$	130			ns	
T_{WR}	$\overline{WE}$ Pulse Width	175			ns	
T_{DH}	DAL (CDP) Hold From $\overline{WE}\uparrow$	60			ns	
T_{ACH}	A0, $\overline{CS}$ Hold From $\overline{WE}\uparrow$	0				
HAND-SHAKE						
T_D	KR (DIR)↓, $\overline{KA}$ ($\overline{DIA}$)↓ From $\overline{WE}\downarrow$ KR (DIR)↑, $\overline{KA}$ ($\overline{DIA}$)↑ From $\overline{WE}\uparrow$ DOR↓, $\overline{DOA}\downarrow$ From $\overline{RE}\downarrow$ DOR↑, $\overline{DOA}\uparrow$ From $\overline{RE}\uparrow$		150	300	ns	C_{LOAD} = 50PF

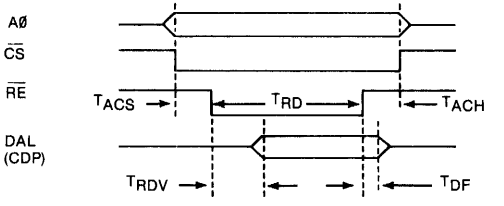
NOTE: All output timing specifications reflect the following: High Output 2.0V
Low Output 0.8V



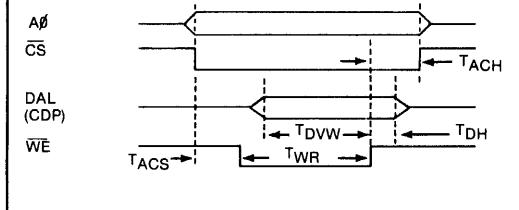
TYPICAL KEY OR DATA REGISTER LOAD



TYPICAL DATA REGISTER READ & TIMING



READ TIMING



WRITE TIMING

MISCELLANEOUS TIMING

1. CLOCK INPUT

FREQUENCY MAX.	FREQUENCY MIN.	PULSE WIDTH MIN
500KHz	100KHz	500nsec
2 MHz	100KHz	250nsec
3 MHz	100KHz	165nsec

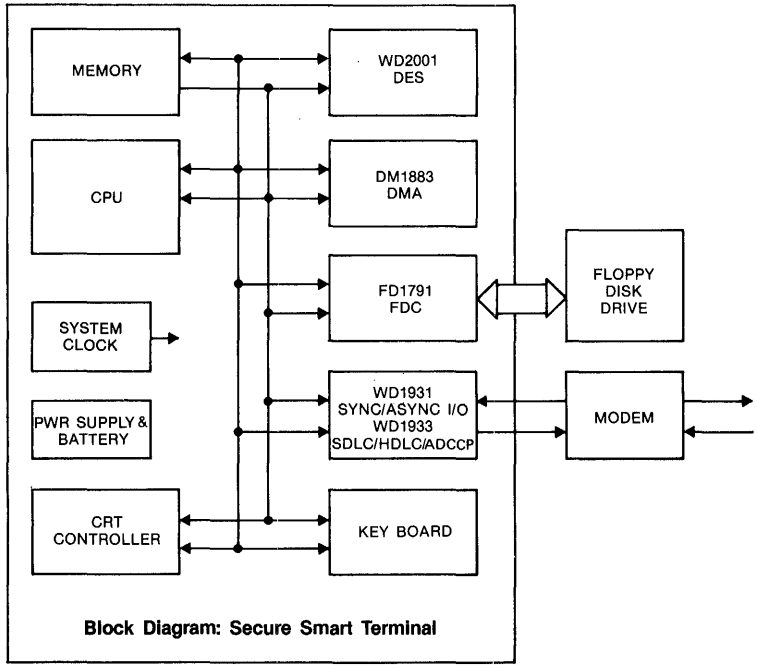
2. MASTER RESET PULSE WIDTH: 10 Clock Periods
3. Time between consecutive $\overline{RE}$ or $\overline{WE}$ pulses: $T_{BR} = T_{BW}$ = 2 CLOCK PERIODS MINIMUM
4. ACT, $\overline{E}$/D, KEOE OUTPUTS
   These pins will be valid within 2 CLK↓ + 450 nsec from $\overline{WE}$ ↑ of a COMMAND REGISTER write operation.
5. $\overline{KPE}$ OUTPUT
   This pin will be active within 2 CLK ↓ + 450 nsec from $\overline{WE}$ ↑ of a write of a KEY WORD byte that results in a parity error.
6. $\overline{CRPS}$, $\overline{DPS}$, E/D INPUTS require a 300 ns set-up time.
7. The initial KR activation will be valid within 3 CLK ↓ + 450 nsec from $\overline{WE}$ ↑ of a write operation that programs a '1' into the COMMAND REGISTER ACTIVATE bit (or 2 CLK ↓ + 450 nsec from ACT input ↑, if $\overline{CRPS}$ = 0).
8. The initial DIR activation will be valid within 2 CLK ↓ + 450 nsec from $\overline{WE}$ ↑ of the 8th write into the KEY REGISTER.
9. The initial DOR activation will be valid within 49 CLK ↓ + 450 nsec from $\overline{WE}$ ↑ of the 8th write into the DATA REGISTER.
10. When reading the DATA REGISTER (in response to DOR), subsequent data bytes are made available internally to the DAL (CDP) output buffers within 2 CLK ↓ + 450 nsec from $\overline{RE}$ ↑

NOTE: All output timings assume C_{LOAD} = 50 PF

TYPICAL APPLICATION

Shown below is a block diagram for a floppy disk based DES secure smart terminal. The Direct Memory Access (DMA) controller optimizes data transfer operations for not only the floppy but also for file encryption and decryption operations. Secure features for the terminal include: secure file storage on floppy disks, optical clear/secure transmission via the communications I/O and battery backup of the Terminal ID key.

Tampering with the Terminal by unauthorized persons either through the key board power supply interrupt interlock or attempting to open the service panel results in memory scrambling and terminal ID key destruction. Finally, a hardware option was also included to allow the use of the pin compatible WD1933 device in place of the WD1931 for bit oriented SDLC, HDLC, or ADCCP protocols.



Block Diagram: Secure Smart Terminal

See page 725 for ordering information.

Printed in U.S.A.

WD2001/2 Applications Note
"One Bit Cipher Feedback In A Synchronous System"

INTRODUCTION

The WD2001/2 Data Encryption device interfaces easily to both microcomputer and hard-wired logic circuits. This Applications Note provides suggestions for the implementation of a synchronous circuit to perform system timing in a one bit cipher feedback application.

SYSTEM TIMING CONSIDERATIONS

The synchronous operation of a digital circuit often leads to both minimal hardware count and simple, easy to understand timing relationships. In addition, the concern over individual device characteristics become non-critical through the use of a worst case design approach. Common problems such as race conditions and temperature sensitivity can be virtually eliminated by synchronizing all logical events to a well defined clock edge.

WD2001/2 TIMING REQUIREMENTS

The WD2001/2 may be operated from a 2 MHZ clock. This provides a fundamental time period of 500 nSec that easily fits into the timing requirements for the device. For example, the minimum pulse width for a read (RD) or write (WR) pulse is 450 nSec.

Generation of the RD or WR pulse can be directly obtained from a synchronous device that transitions at each edge of the synchronous clock (SYNCLK). Figure 1 illustrates the timing relationship between SYNCLK and RD or WR.

Once the timing relationship is understood, the implementation becomes quite straightforward. The circuit of Figure 2 suggests a possible method of RD or WR generation.

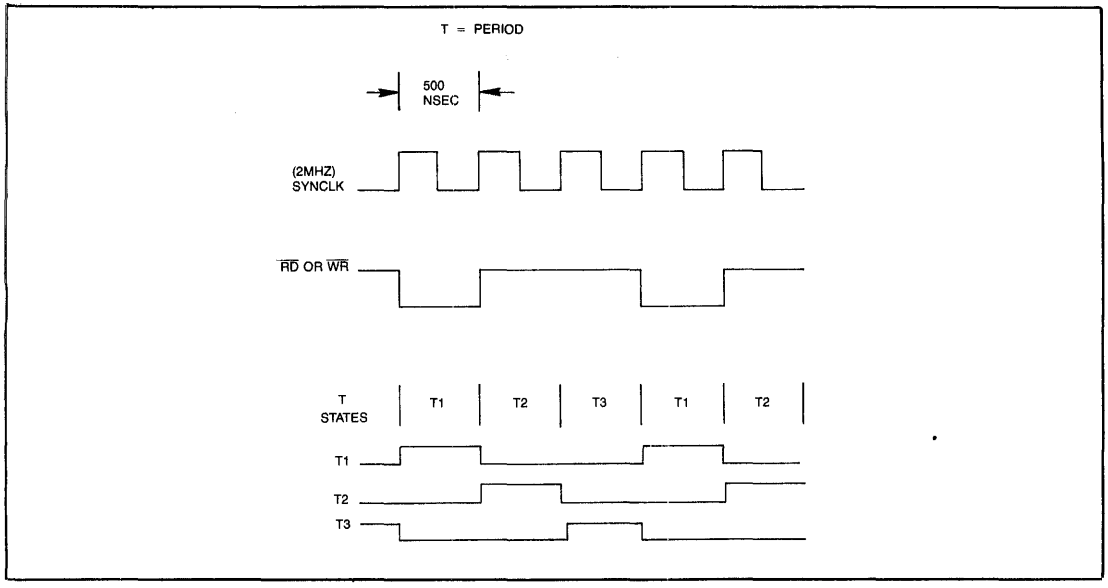
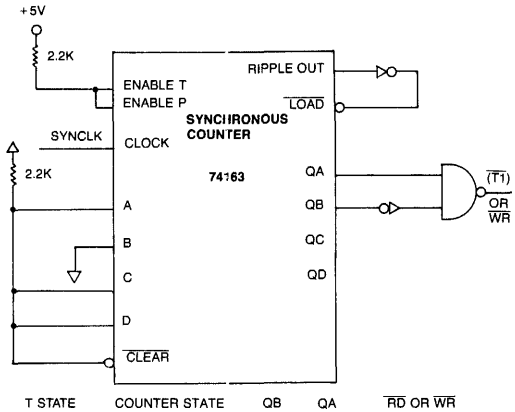


Figure 1 SYNCLK, RD, AND WR TIMING RELATIONSHIPS.



T STATE	COUNTER STATE	QB	QA	RD OR WR
T1	13	0	1	0
T2	14	1	0	1
T3	15	1	1	1

Figure 2 RD AND WR TIMING GENERATION

FUNDAMENTAL TIMING SEQUENCES

Any cryptographic implementation using the Data Encryption Standard (DES) can be broken down into four fundamental timing sequences. First, the key is loaded into the WD2001/2 (Load Key). Second, the data to be encrypted or decrypted is loaded into the device (Load Data). Next, the DES is executed. Finally, the result of the DES is unloaded from the WD2001/2 (Unload Data). Figure 3 lists the timing requirements for each timing sequence.

The Load Key, Load Data, and Unload Data sequences are highly similar. Figure 4 shows the logical flow associated with the Key Load or Data Load, or Data Unload. The Data Encryption Algorithm sequence can be derived from the timing associated with the other three sequences. For simplicity, the DES timing is accomplished by counting groups of three clock periods in a fashion similar to the method shown in Figure 4. The logical flow for the DES timing is shown in Figure 5.

SEQUENCE	NUMBER OF CLOCK PERIODS	TOTAL
Load Key	8 bytes × 3 clocks	24
Load Data	8 bytes × 3 clocks	24
DES	17 × 3 clocks	51
Unload Data	8 bytes × 3 clocks	24

Figure 3 FUNDAMENTAL TIMING SEQUENCES

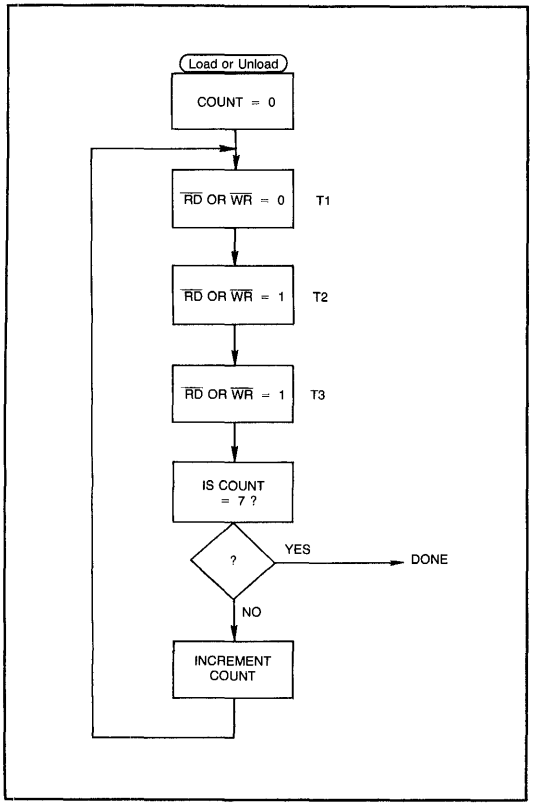


Figure 4 KEY LOAD, DATA LOAD, AND DATA UNLOAD FLOW

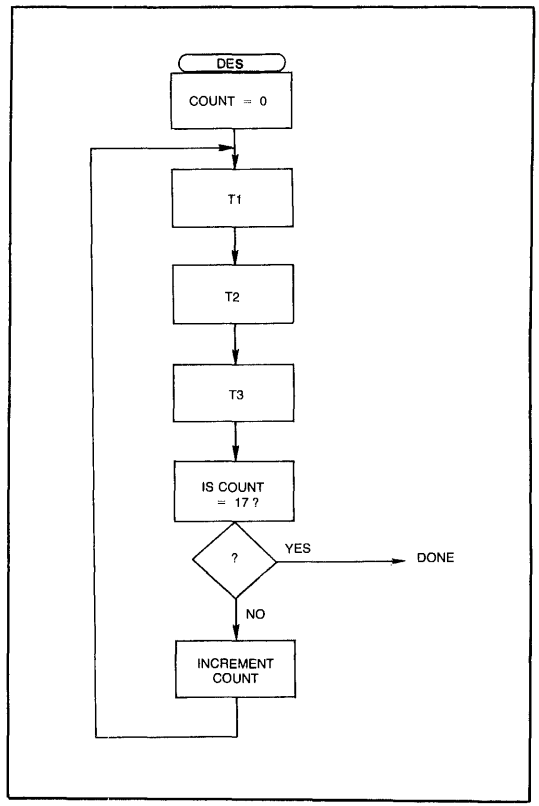


Figure 5 DES LOGICAL FLOW

SYSTEM TIMING OVERVIEW

The normal operation of a cryptographic system would require three classes of input/output (I/O) operations with the WD2001/2. First, the key is loaded (Key Load) through eight consecutive write cycles. Second, the data to be encrypted or decrypted is loaded (Load Data) in a similar fashion. After the Data Encryption standard is completed, the data is unloaded (Unload Data) through eight consecutive read cycles. Typically, the Key Load sequence would occur much less frequently than the Load Data or Unload Data sequences.

The flow diagram of Figure 6 shows the relationship between the four fundamental timing sequences defined previously, and also highlights the three I/O operations. Note that the Key Load sequence is outside of the tight loop.

Using the four fundamental timing sequences as logical building blocks, a functional block diagram of system timing can be designed. Figure 7 illustrates the overall system timing functions.

An implementation of the functions shown in Figure 7 is suggested in Figure 8. Note that all timing transitions are synchronous with the rising edge of SYNCLK.

Figure 9 details the timing of the Load Key sequence, and is similar to the Load Data, Unload Data, and DES sequences also.

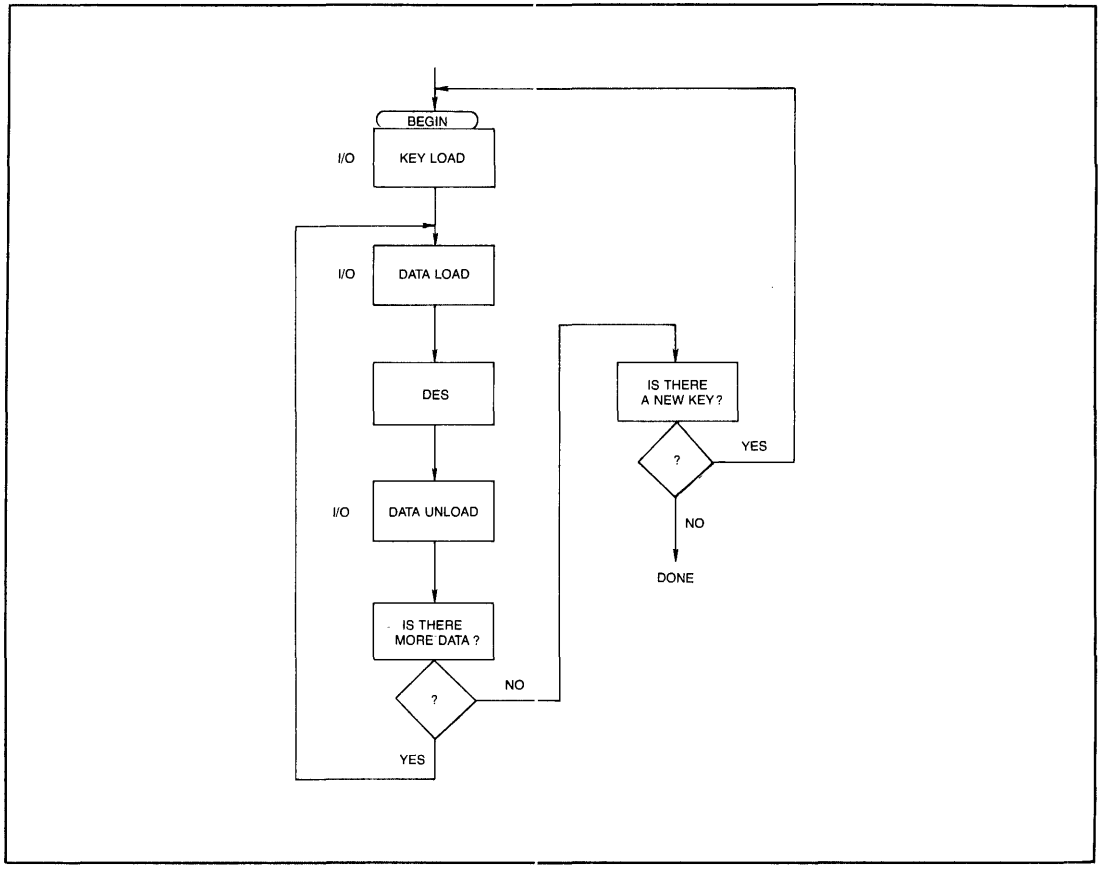


Figure 6 FUNDAMENTAL TIMING SEQUENCES INTERRELATIONS

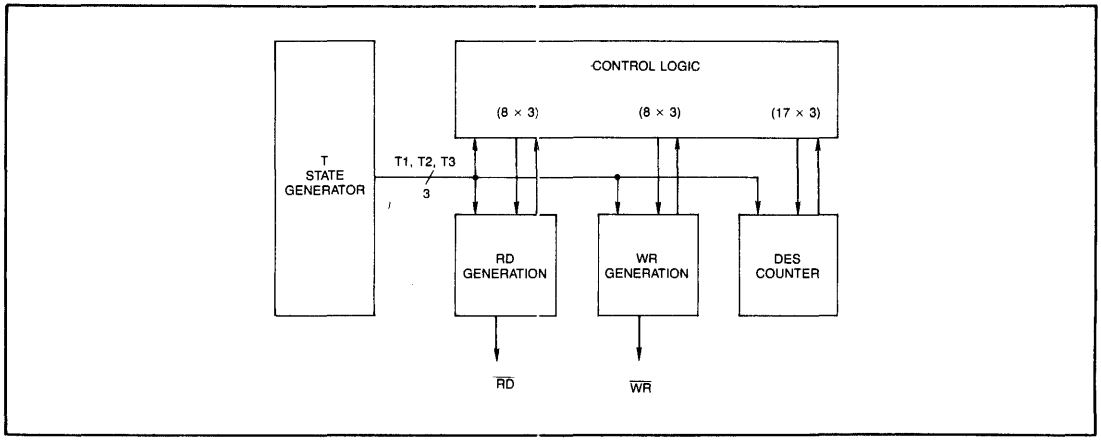
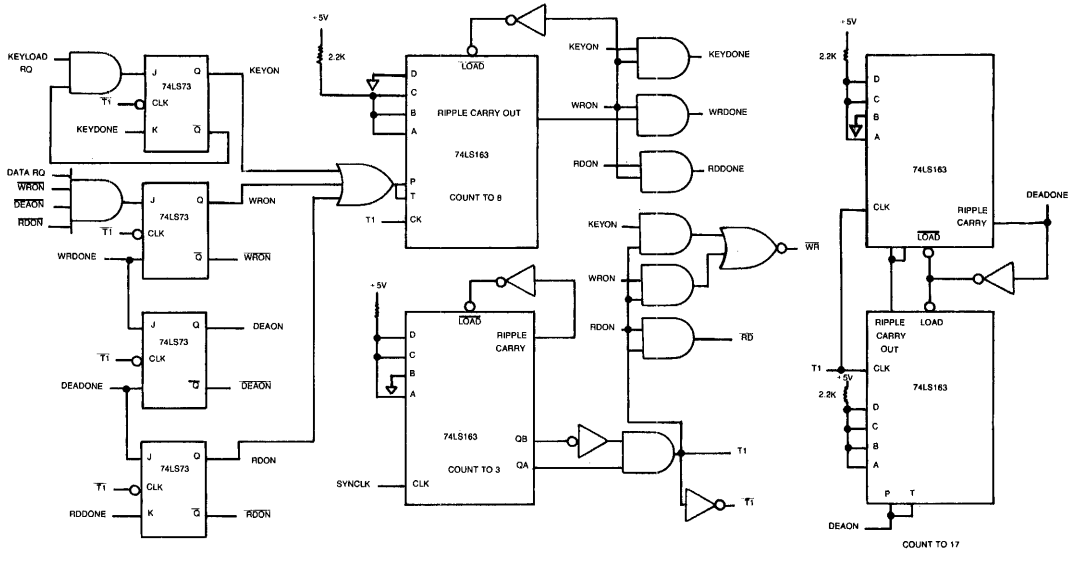


Figure 7 SYSTEM TIMING BLOCK DIAGRAM



1. KEYLOAD RQ AND DATA RQ DO NOT OCCUR SIMULTANEOUSLY.
2. ALL J-K PRESETS TO +5V.
3. ALL J-K CLEARS TO "RESET".
4. RESET SHOULD LOAD ALL 74LS163 COUNTERS.

Figure 8 SYSTEM TIMING IMPLEMENTATION

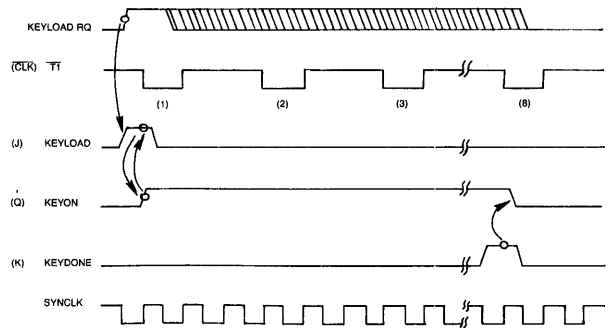


Figure 9 SINGLE KEYLOAD SEQUENCE

ONE BIT CIPHER FEEDBACK

The one bit cipher feedback (OBCFB) architecture is widely used in Data Communications. The WD2001/2 device, when operated with a 2 MHZ clock, will run at an effective bit rate of over 19,200 bits/second, which is the practical upper limit of many communications links.

FUNDAMENTAL LOGICAL COMPONENTS OF OBCFB

A one bit cipher feedback system can be broken down into nine logical components, as listed in Figure 10.

NAME	DESCRIPTION
KEY	56 bit number that maps INV to OV
IV	Initialization Vector
INV	Input Vector
DES	Data Encryption Standard
OV	Output Vector
SDI	Serial Data In
SDO	Serial Data Out
SR	Shift Register (used with INV)
MOD2	Modulo 2 Adder

Figure 10

NINE FUNDAMENTAL COMPONENTS OF OBCFB

FUNCTIONAL DESCRIPTION OF OBCFB

The OBCFB algorithm operates on a one bit wide data input, hence it is ideally suited to serial Data Communications applications. In encryption mode, the serial data in is added modulo 2 with the most significant bit (msb) of the 64 bit output vector. The result of this operation is then fed into the least significant bit (lsb) of a 64 bit shift register, and also is used as the serial data output. The shift register is then shifted from the lsb to the msb, and the result becomes the next input vector. After the Data Encryption Standard is completed, the process is repeated again for the next single bit of serial input data. Because each serial data bit requires an entire 64 bit INV and OV, the effective bit rate of this operation is 64 times less than that of a operation which uses all 64 bits of the OV, such as Code Book. Figure 11 shows a block diagram of a OBCFB circuit operating in encryption mode.

To decrypt, the operation is changed in one way. Instead of feeding the result of the modulo 2 adder to the shift register, the unmodified serial data is used. All other operations are identical. Figure 12 shows a circuit which supports both encryption and decryption.

Because the OBCFB algorithm uses a 64 bit shift register on the INV, each SDO bit is a function of its corresponding SDI bit and the 64 previous operations. This implies that the past history of the encryption operation is necessary to initialize a system. The IV is used to supply the history required to allow immediate use of the OV from the DEA. Typically, the IV is either a predefined value, or the last 64 SDO bits from the data stream being encrypted or decrypted. This allows the encryption process to be accomplished with discrete blocks of data, and hence the WD2001/2 can be used in a multichannel communications environment.

In OBCFB, the WD2001/2 is always set to encrypt mode. The selection of either the SDI as the feedback element to the shift register, or the SDO as the feedback element, determines whether the incoming data is encrypted or decrypted.

Another factor involved with OBCFB is the propagation of errors through a 64 bit block of data. Because of the 64 bit shift register that feeds the INV, a single bit error will cause the following 63 bits to be in error also. After the last bit of the 64 erred bits, the data will become resynchronized and the effect of the shift register will no longer cause bad data.

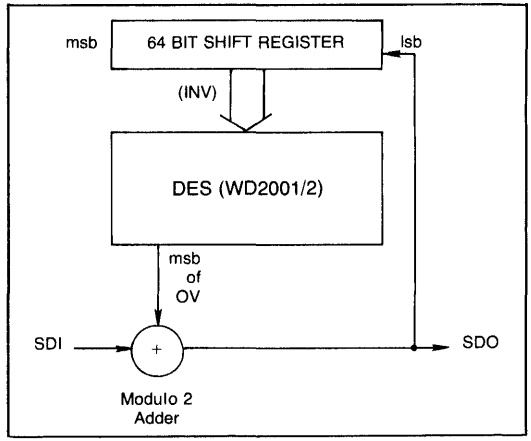


Figure 11 OBCFB ENCRYPTION BLOCK DIAGRAM

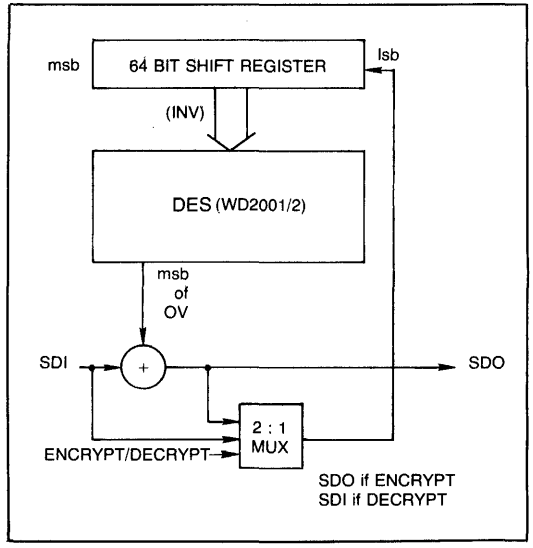


Figure 12

OBCFB ENCRYPTION/DECRYPTION BLOCK DIAGRAM

ONE BIT CIPHER FEEDBACK IMPLEMENTATION

Since the WD2001/2 is a byte input/output oriented device, the implementation of a OBCFB circuit can be accomplished without the 64 bit shift register shown in Figures 11 and 12. Through the use of a 9 bit wide FIFO, a "virtual" 64 bit shift register can be built. Figure 13 illustrates this with a Western Digital FR1502 FIFO and some common TTL logic.

Once the modulo 2 adder, the encrypt/decrypt selector, and the shift register are defined, the overall circuit can be generated by combining these pieces along with the logic shown in Figure 8. The overall block diagram of the one bit cipher feedback system is given in Figure 14.

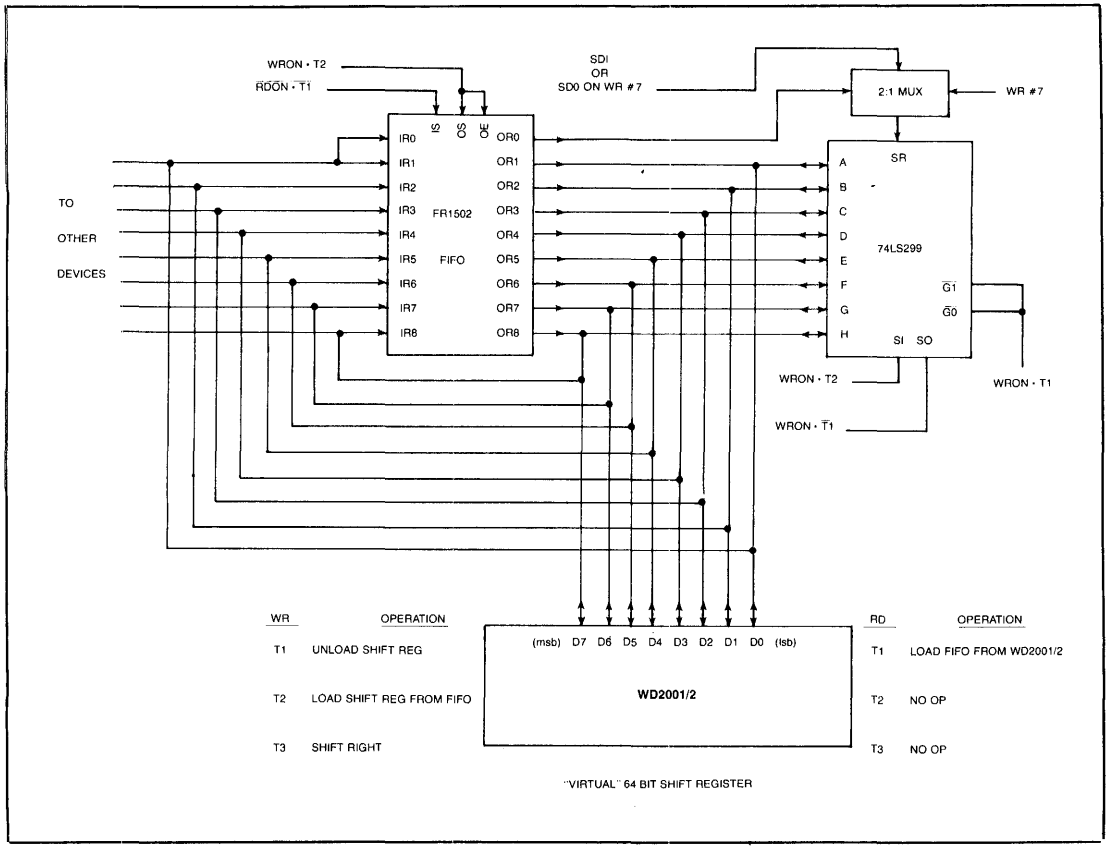


Figure 13 "VIRTUAL" 64 BIT SHIFT REGISTER

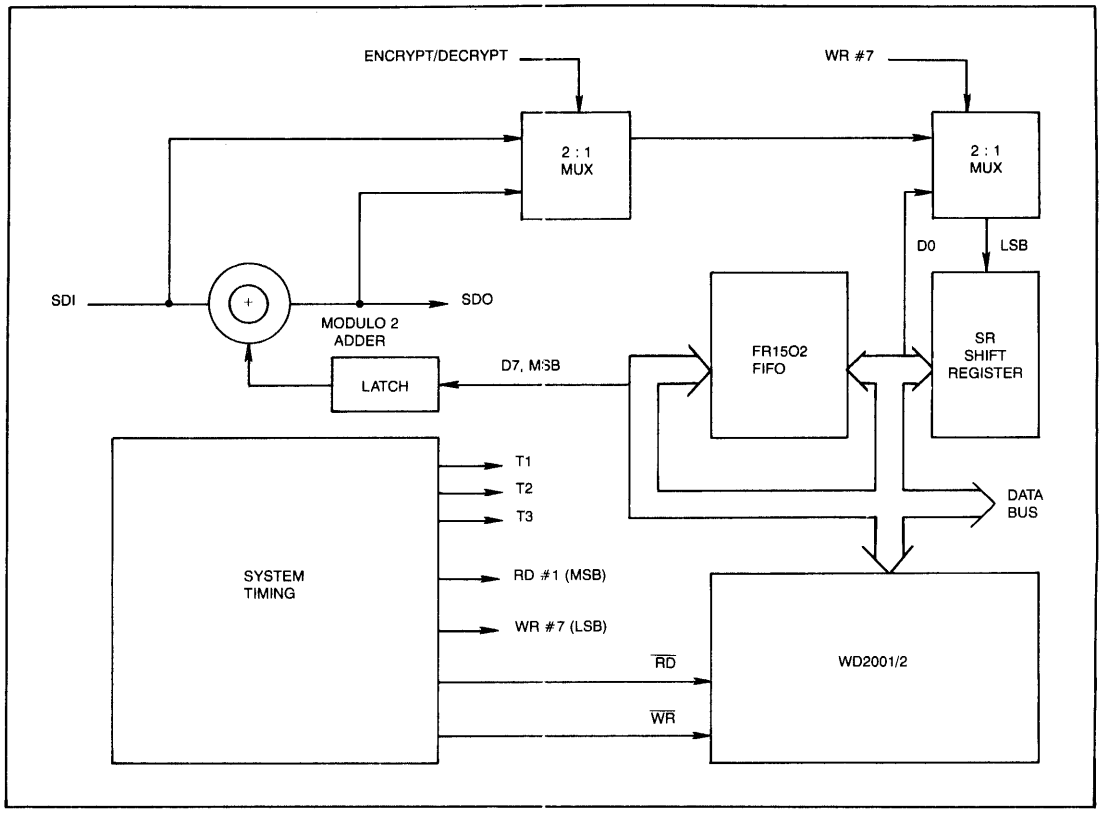


Figure 14 OBCFB SYSTEM BLOCK DIAGRAM

CONCLUSION

The WD2001/2 device lends itself readily to the most common of all Data Communications encryption techniques. The one bit cipher feedback algorithm can be implemented easily through the use of synchronous timing generation and circuit design techniques.

See page 725 for ordering information.

RELATED DOCUMENTS

WD2001/2 Data Sheet, Western Digital Corporation

FIPS 46
Federal Information Processing Standard
National Bureau Of Standard
Department of Commerce

Printed in U.S.A

Cipher Feedback Cryptography Technical Note

CIPHER FEEDBACK CRYPTOGRAPHY

The United States Government in proposed Federal Standard 1026 describes three different approved ways of using the National Bureau of Standard's Data Encryption Standard (DES): Electronic Codebook; Cipher Feedback; and Cipher Block Chaining. Western Digital's WD2001 and WD2002, as delivered, implement the DES in Electronic Codebook Mode. This Technical Note will describe how to build an "N" bit Cipher Feedback (CFB) circuit using the WD2001.

WHAT IS CIPHER FEEDBACK?

Cipher feedback cryptography produces, as a function of previous cipher text, a pseudorandom bit stream which is added modulo 2 to the plain text to produce the next cipher text.

DES IN CIPHER FEEDBACK (CFB)

Obviously, both the receiver and transmitter must start their cryptographic operation with the same cryptographic keys to be able to acquire and maintain crytographic synchronization, i.e. produce the same pseudorandom bit stream at the same point in time.

For DES this means that both the 64 bit cryptographic variable (56 bit key) and the initial input to the algorithm must be identical at both ends. The initial input to DES in CFB is called the Initializing Vector (IV). Its format and generation are described in detail in Federal Standard 1026.

The functional description of using the WD2001 in CFB mode below assumes that communication synchronization has been achieved; that identical decrypted IV's and cryptographic keys are available to both the transmit and receive ends of the link; that encryption is to be a 1 bit cipher feedback; and that the plain text character size (1 in the example) equals the transmitted character size (Method A in proposed Federal Standard 1026).

ENCRYPTION

At time 0, the 64 bit cryptographic variable is loaded into the WD2001 with the key load sequence. A 64 bit block consisting of not more than 16 leading 0's and the 48 bit (or longer) IV is loaded into a 64 bit shift register (R) and into the input register, as if it were data, and encrypted. The WD2001 will automatically encrypt the IV under control of the cryptovariable and present a 64 bit block, 8 bits at a time as output. This output is stored in a shift register(S) with the most significant bit (MSB), to the left and the least significant bit on the right.

The MSB of S is added modulo 2 to the first bit of plain text to produce the first cipher bit. The contents of R are shifted 1 bit to the left and the just created cipher bit is inserted as the least significant bit (LSB) in R. The cipher bit is now available for buffering, transmission, etc.

The new contents of R are now loaded into the WD2001 as data, encrypted, and the new output placed in S.

The above procedure is repeated until the entire message text is encrypted, one bit at a time.

DECRYPTION

Decryption is accomplished in a similar manner: the IV is stored in R; loaded into the WD2001 as data; ENCRYPTED (even though the operation on the message text is to be decrypted); the results stored in S; and R shifted 1 bit to the left. Now, because the unit is receiving cipher rather than creating it, the first received bit is placed in the LSB of R. This cipher bit is also added, modulo 2, to the leftmost bit in S to reproduce the original plain text.

NOTES

Of particular significance is that the DES chip is in the ENCRYPT mode for CFB cryptography regardless whether the operation is to be performed to create cipher text or to recreate plain text. This is because the DES is being used to generate a pseudorandom bit stream. It is the exclusive OR operating on that bit stream and the received text which accomplishes the actual encryption/decryption of data.

S was nominally defined to be 64 bits long. It need be no longer than the number of text bits to be exclusive OR'd at one setting of the pseudorandom stream. In the example it was one bit. In reality it could be any character or block size from 1 to 64 bits long.

The convention used in this note is to organize a shift register with the MSB to the left. In practice, what is important is to use the MSB of S for the MOD 2 addition and to shift the R register content, so that the MSB is dropped and the cipher bit becomes the LSB. It is also important to perform the shift and generate a new pseudorandom block after each character has been encrypted or decrypted.

OTHER CIPHER FEEDBACK METHODS

Cipher Feedback can be done for any feedback size of 1 through 64 bits. One bit cipher feedback has the overall advantage of being transparent to the data being protected.

CHARACTERISTICS OF CFB

CFB has two properties which must be considered when selecting it for data encryption: 1) error extension and 2) self synchronization. Both of these properties exist because the encryption process synchronizes on the received cipher to produce the pseudorandom bit stream.

In the case of DES in one bit CFB, a one bit error in the received cipher message will affect the next 64 pseudorandom blocks—it will take 64 iterations to shift the one "bad" bit out of the 64 bit register above. If 8 bit CFB is used, then only 8 blocks will be affected, but that will still represent 64 bits used to decrypt incoming data.

In the same way, receiving 64 consecutive good bits of cipher will have filled the data-in register on the receiver end with the same 64 bits of data as in the transmit unit and proper decryption can again take place, assuming both ends have the same cryptographic key. This is what is meant by self-synchronizing.

APPLICATIONS OF CFB

In the data communications world error extension and self-synchronization are not important because of the excellent conditions of the lines and the protocols and error correcting codes used to insure proper receipt of data. In some applications, these properties of CFB cryptography can be turned to the user's benefit. This is especially true in situations where the data stream contains highly redundant information, where an incorrect recovery of 64 bits is hardly noticed—particularly when compared with the overall communications benefit of having the cryptography automatically resynchronize itself.

WD2001 CHARACTERISTICS IN CFB

The WD2001 is rated as having 1.304 megabits per second throughput when driven by a 2 MHZ clock. This figure is based on processing 64 bits of data at each operation. Using the WD2001 in an 8 bit cipher feedback circuit will reduce that to 163 kilobits per second. A 1 bit cipher feedback circuit would further reduce effective throughput to 20.385 kilobits per second. This is true of any DES implementation. The algorithm is designed to process 64 bits of plain (cipher) text at a time to produce 64 bits of cipher (plain) text; cipher feedback is designed to operate on a basic character size and shift after that character has been encrypted. In the 1 bit case, the user "throws away" 63/64ths throughput capacity for each encryption.

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Microcontrollers

WD51 Irrigation Controller

FEATURES

- CONTROLS UP TO 6 IRRIGATION STATIONS
- PUMP CONTROL/MASTER VALVE OUTPUT
- USER PROGRAMMABLE FOR UP TO 3 WATERING CYCLES DURING A 24 HOUR DAY
- USER PROGRAMMABLE RUN TIMES OF 1 TO 99 MINUTES FOR EACH STATION
- USER SELECTION OF WATERING DAYS OF 0 TO 7 DAYS PER WEEK
- TIME OF DAY AND DAY OF WEEK CONTINUOUSLY DISPLAYED
- RAIN INHIBIT MODE
- EASY TO DESIGN IN

GENERAL DESCRIPTION

Preprogrammed Controller for Irrigation Applications. The WD-51 is a single-chip controller preprogrammed to operate a 6 station irrigation system. It is implemented using P-channel silicon gate MOS/LSI technology and requires minimal support circuitry. All program and data storage are on-chip, as well as input switch matrix scan, 7 segment display decode and drive, and output control logic.

FUNCTIONAL DESCRIPTION

The logic symbol and block diagram of the WD-51 is shown in Figure 1.

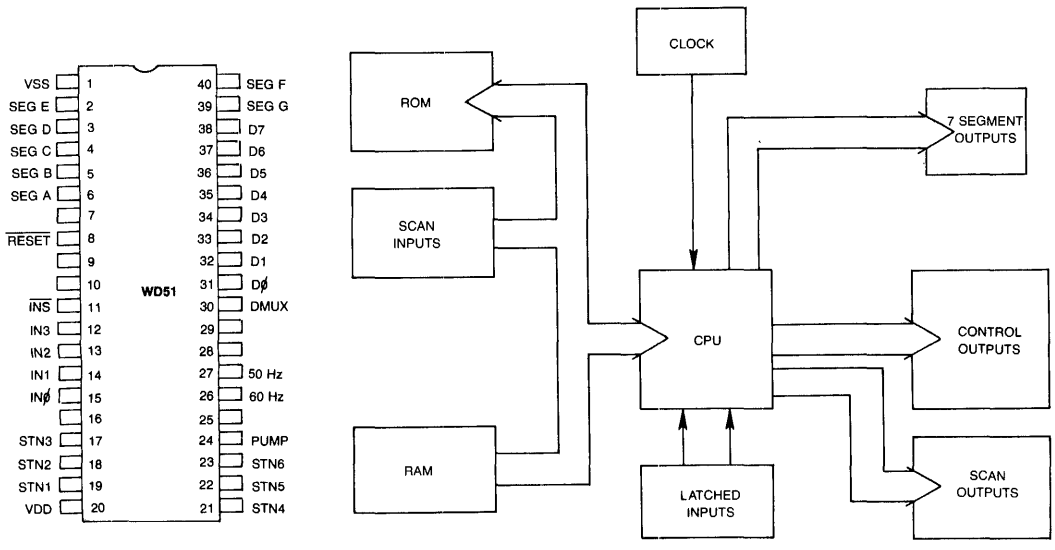

FIGURE 1 BLOCK DIAGRAM

PIN DESCRIPTION

SYMBOL	PIN NO.	FUNCTION
V_{SS}	1	Positive Supply voltage
V_{DD}	20	Negative Supply voltage
Seg A,B,C, D,E,F,G	2-6, 39-40	Decoded 7-Segment Multiplexed outputs, 15 mA source.
$\overline{\text{RESET}}$	8	A low-level input voltage resets internal logic and initializes RAM data.
IN0, 1N1, 1N2, 1N3	12-15	Scanned inputs, 1N3 is MSB
STN 1,2,3, 4,5,6	17-19, 21-23	Station Output control for solenoid drivers.
PUMP	24	Pump control output- a high-level output indicates a manual or automatic cycle is in progress.
60HZ	26	60 HZ time base input
50HZ	27	50 HZ time base input
DMUX	30	4-digit display control output
D0-D7	31-38	Digit scan outputs, (D7=MS_D, D0=LS_D)

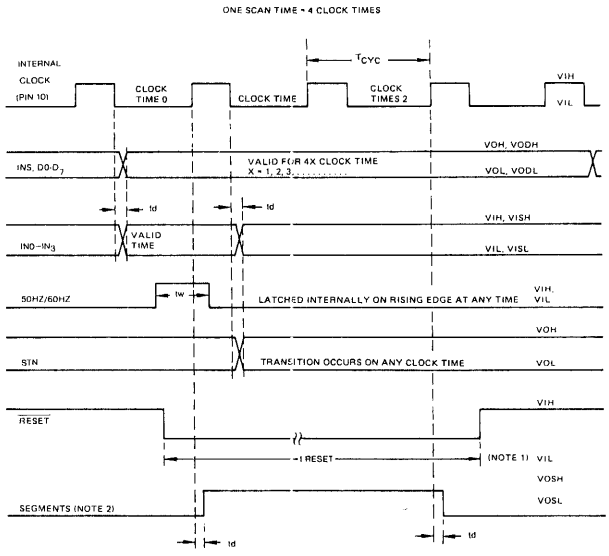

FIGURE 2

TIMING DIAGRAM

NOTE 1: RISING EDGE OF RESET GENERATES SCAN TIME 0 WITHIN 4 CLOCK TIMES

NOTE 2: SEGMENT OUTPUTS ARE VALID DURING CLOCK TIMES 1 TO 3 ONLY THEY ARE LOW AT TIME 0

INPUTS

INPUT SWITCH MATRIX—The WD-51 may be used with any switch configuration which is matrix compatible, such as a keyboard, rotary switch, slide switch, or combinations of both. All multiplexing and decoding is performed on-chip, thus requiring no external components, other than the switch matrix.

SETTING DAY OF WEEK—If SET DAY is depressed in conjunction with ADVANCE, the Day digit (D4) will increment, with rollover from 7 to 1. Note that since the day is numerically displayed (as opposed to alphanumeric), the numbering is arbitary, i.e., if Sunday is considered to be "1", then Wednesday is "4", Friday is "6", etc.

		DIGIT SCAN TIME OUTPUTS							
		D7 (38)	D6 (37)	D5 (36)	D4 (35)	D3 (34)	D2 (33)	D1 (32)	D0 (31)
SCANNED INPUTS	IN0 (15)	ADVANCE	3-STATION STRAP	SET MINUTES	ACTIVE DAY 4	ACTIVE DAY 1	START TIME #1	RUN TIME #4	RUN TIME #1
	IN1 (14)			SET HOURS	ACTIVE DAY 5	ACTIVE DAY 3	START TIME #1	RUN TIME #5	RUN TIME #2
	IN2 (13)			SET DAY	ACTIVE DAY 6	ACTIVE DAY 3	START TIME #3	RUN TIME #6	RUN TIME #3
	IN3 (12)			SKIP -A-DAY	ACTIVE DAY 7		MANUAL OFF	MANUAL ON	RUN

FIGURE 3 INPUT SWITCH MATRIX

The basic functions of the Irrigation Controller are selected by one or more switches as defined in Figure 2. Inputs IN0-IN3 form a 4 bit wide input port which is scanned by the Digit Scan Outputs D0-D7, forming an 8 × 4 matrix which connects to the user-supplied keyboard/switches.

SWITCH FUNCTIONS—The switch functions shown in Figure 3 are defined as follows:

ADVANCE—For all setting operations, a common key is used to increment the selected data (time, day, start-time, or run-time). Immediately after the detection of the advance switch, the data increments by 1, waits 1½ seconds, then begins incrementing at the rate of 3 per second. This allows the operator to move rapidly to the desired value without "overshooting" and then "tapping" the advance key when close to the find value.

SETTING TIME OF DAY—Two separate switch inputs for setting hours and minutes in conjunction with the ADVANCE key. If SET MINUTES is selected while ADVANCE is depressed, the minutes digits (D0 & D1) will increment. Minutes rollover is from 59 to 00 with no carry into the hours. If SET HOURS is selected while ADVANCE is depressed, the hours digits (D2 & D3) will advance. Hours rollover is from 24 to 01, with midnight equal to 2400.

SETTING START TIMES—There are up to 3 automatic watering cycle times available in a 24 hour period. To examine them, START TIME 1, 2, or 3 is selected and displayed in hours on digits D7 and D6. If it is desired to change the data, the ADVANCE key is depressed. The rollover is from 24 to 00, with 00 being a start-time "skip" value. Thus 1, 2, or 3 cycles per day may be selected.

SETTING RUN-TIMES—Each one of 6 stations may be set to a run time of 0 to 99 minutes, with 00 being a "skip station" value. To examine the stored data, the desired station RUN TIME key (1–6) is selected with the time in minutes being displayed on digits D7 and D6. To change the data, the ADVANCE key is depressed. The selected run time will then increment with rollover from 99 to 00 minutes.

SETTING ACTIVE DAYS—The WD51 reads active day information from the switch matrix, with typically slide, toggle, or "DIP" switches being used. An automatic watering cycle may be set for 0 to 7 days a week simply by closing the switch for the respective day. An ALTERNATE DAY switch position is provided, which, when activated, causes the controller to ignore the 7 active-day switches and to run an automatic cycle every other day.

MANUAL ON—This switch position immediately activates a timed watering cycle beginning with station No. 1, regardless of the setting of the start-times or active days. The run times programmed for stations 1–6 are automatically run.

The cycle may be terminated anytime with the MANUAL OFF key. If it is desired to start with a specific station other than station No. 1, that station ONE-TIME-key should be depressed *first,* then the manual key. The cycle will then begin at the selected station and continue through station No. 6.

RUN MODE—This is the normal automatic operating mode of the Irrigation Timer. When in this mode, the START and RUN-TIME data cannot be displayed or modified, preventing accidental erroneous entry of data.

RAIN INHIBIT (MANUAL OFF)—This switch is used to cancel or prevent a watering cycle, either manual or automatic. When activated during a current cycle, it immediately turns off all station outputs and returns to a time-keeping mode only. With external signal conditioning circuitry, this input could be used to interface with a moisture or rain sensor. This function is normally implemented by paralleling a toggle switch ("rain") with a momentary key ("manual off").

3 STATION OPTION—By connecting IN3 to D5 through a diode, run times for Stations 4, 5 and 6 will be continuously set to zero, thus they will always be skipped. Also, if switch positions for Run Times 4, 5 and 6 are not provided to the user, these stations cannot be examined.

RESET—This is the reset input of the micro-controller. An external capacitor of approximately 2 μf is recommended between 8 and VDD to generate a reset signal when power is first applied.

OUTPUTS

DISPLAY SEGMENT OUTPUTS (SEG A-SEG F)—The WD-51 is designed to directly drive vacuum flourescent (V-F) displays or common-cathode LED displays up to 0.3 inches. The seven segment outputs are high current outputs and are multiplexed in synchronization with D0 - D7 with sufficient interdigit blanking to prevent "ghosting". The display register is shown in Figure 4.

The time of day is displayed as a four digit number in 24 hour format (9AM = 0900, 5PM = 1700, MIDNIGHT = 2400, etc.) and the day of the week is displayed as a number between 1 and 7. The time and day are continuously displayed regardless of the mode selection. Zero blanking is not provided for any of the digits.

The selected station (1–6) is shown in digit D5. The station number is displayed when a RUN-TIME key is depressed or the controller is active during a manual or automatic watering cycle; otherwise a zero is displayed.

The start time and run times are displayed in digits D6 and D7. When any of the start-time switches are selected, the D6 and D7 digits display the hour of the day the watering cycle is to start. If a run-time switch is activated, the selected station run-time is displayed in a minutes format. During a manual or automatic watering cycle, the time remaining for the currently active station is displayed in minutes. Otherwise, 00 is displayed.

STN1-STN6—The station outputs are latched logic outputs designed to control the solenoid drives in an irrigation system. These outputs are normally a low-level voltage (solenoid drive is off). When a manual or automatic watering cycle occurs, the appropriate station output goes to a logic "high" voltage for the selected run-time interval. Station-to-station switching is essentially instantaneous. It is recommended that these outputs be buffered by a current driver to supply sufficient current for triacs, relays, or other high-power switching devices.

PUMP CONTROL OUTPUT—This output is a latched logic output which is normally a logic "low" voltage for the pump off condition. It goes to a logic "high" voltage at the beginning of a watering cycle, either manual or automatic, and remains high until the last station goes off. With suitable buffering, this output may be used to turn a pump motor on and off when needed or simply to drive a "cycle on" LED status indicator, or to act as a "master valve" output.

DMUX OUTPUT—This output, in conjunction with minimal external logic, provides a means of using a 4 digit display with the WD51. It is a logic high when a RUN-TIME, START-TIME, or SET-DAY key is depressed and a logic low voltage at all other times, hence it may be used to externally select digit times D4–D7 when high and D0–D4 when low.

DIGIT SCAN TIME

D7	D6	D5	D4	D3	D2	D1	D0
START/RUN TIME (MSD)	START/RUN TIME (LSD)	STATION NUMBER	DAY OF WEEK	T 10's HOURS	I HOURS	M 10's MINUTES	E MINUTES

FIGURE 4 DISPLAY REGISTER

DEFAULT INITIALIZATION—Upon the occurrence of a RESET the micro-controller defaults to the following: Time of day to 12:00; day to 1; start time 1 to 0200 hours; start times 2 and 3 to 00; and run time 1–6 to 10 minutes each. Thus if power is lost to the microcomputer, a default program will be executed without user intervention.

SPECIFICATIONS

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

ABSOLUTE MAXIMUM RATINGS

Operating Free-Air Temperature
T_A Range ..... 0°C to 70°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

Storage Temperature. .....−65°C to +150°C (Ceramic)
−55°C to +125°C (Plastic)

Power Dissipation 2.5 Watt at 25°C
Positive Voltage on any Pin with Respect to V_{SS}: +0.3V
Negative Voltage on any Pin with Respect to V_{SS}: −20.0V

ELECTRICAL CHARACTERISTICS

TA = 25°C, $V_{SS}-V_{DD}$ = 13.2V unless noted otherwise

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage ($V_{SS}-V_{DD}$)	All inputs and outputs open	11.5	13.2	14.5	V
Operating Current		6		15	mA
Input Voltage Levels All Inputs Except IN0–IN3					
Logic High (V_{IH})	Note 1	$V_{SS}-1.0$		V_{SS}	V
Logic Low (V_{IL})		V_{DD}		$V_{SS}-4.2$	V
Inputs IN0–IN3	Note 2				
Logic High (V_{ISH})		$V_{SS}-3.75$		V_{SS}	V
Logic Low (V_{ISL})		V_{DD}		$V_{SS}-9.0$	V
Output Voltage Levels All Outputs Except D0-D7 and SEG A-SEG G					
Logic High (V_{OH})	$I_{OH}=+100\ \mu A$ Min.	$V_{SS}-1.0$		V_{SS}	V
Logic Low (V_{OL})	$I_{OL}=-1.6$ mA Min.	V_{DD}		$V_{SS}-4.6$	V
D0-D7 Outputs					
Logic High (V_{ODH})	$I_{ODH}=1.5$ mA+1 Input (IN0-IN3)	$V_{SS}-1.5$		V_{SS}	V
	$I_{ODH}=5.0$ mA+1 Input	$V_{SS}-3.0$		V_{SS}	V
V_{ODL}	Note 3	$V_{SS}-3.5$		V_{SS}	V
Seg Outputs Seg A-G	$I_{OSH}=16$ mA			$V_{SS}-6.0$	V
Segment Output Current Seg A-G I_{OSH}	Note 3	10	15	40	mA
AC Electrical					
T_{CYC} Instruction Cycle Time			10		μsec
td/tw		5.0			μsec
t $\overline{\text{RESET}}$		15			msec
TBase		0	60	500	HZ

Note 1: Internal Pullup Resistors of Approximately 6K to V_{SS} Across Each Input.

Note 2: Internal Pulldown Resistors of Approximately 12K to V_{DD} Across Each Input.

Note 3: Single Transistor to V_{SS} Output Only.

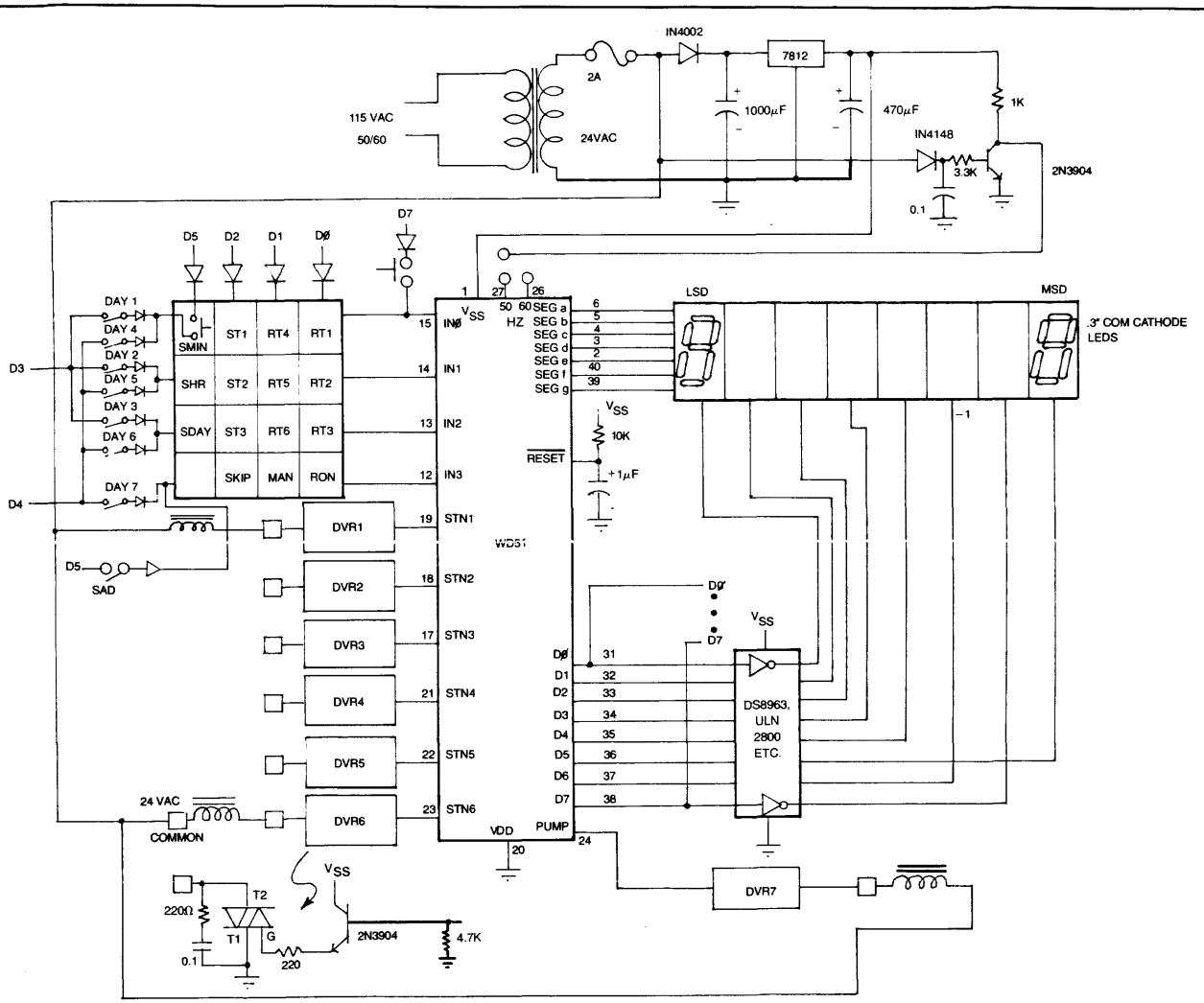

FIGURE 5 COMPLETE 6-STATION IRRIGATION CONTROLLER

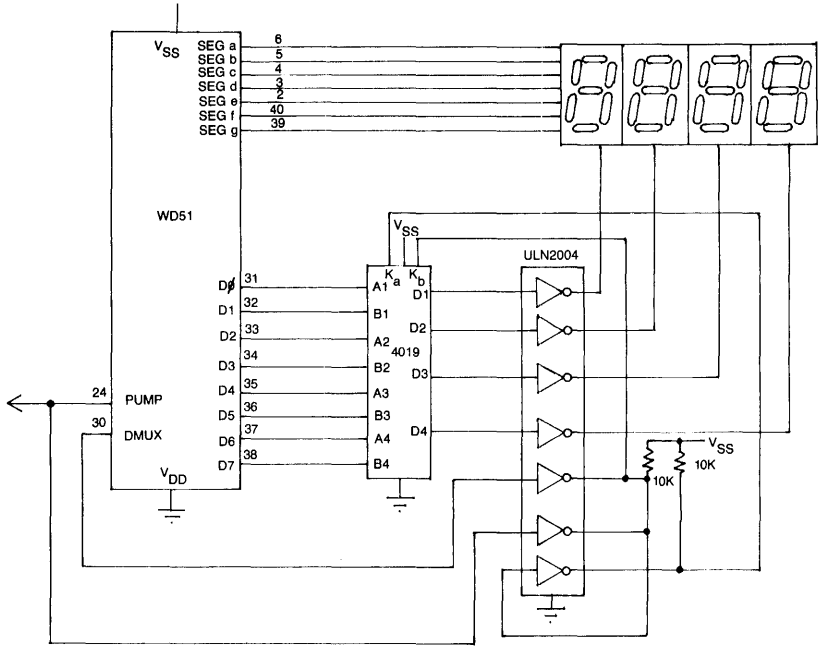

FIGURE 6 WD51 WITH 4-DIGIT DISPLAY OPTION

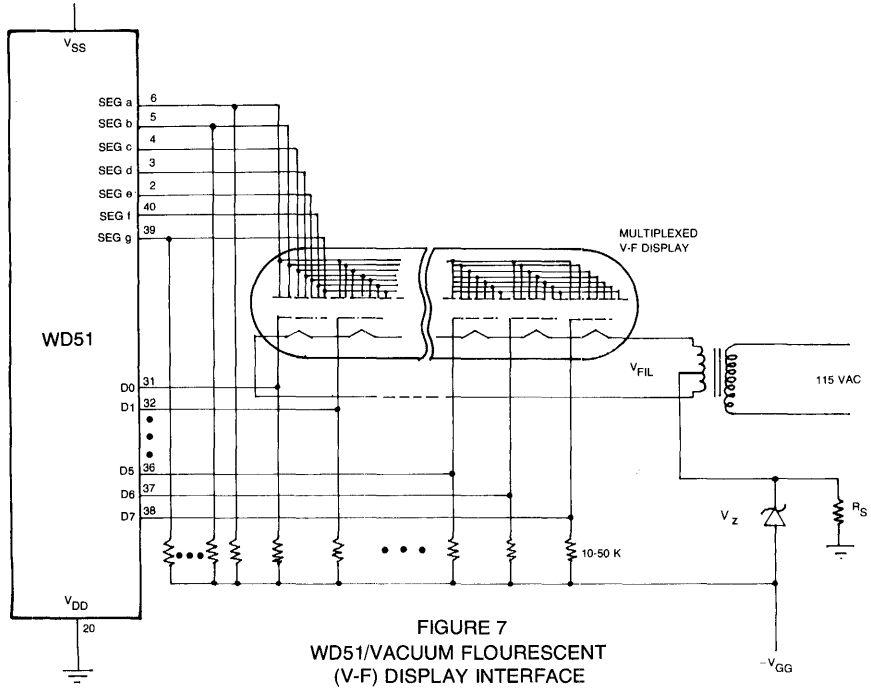

FIGURE 7
WD51/VACUUM FLOURESCENT
(V-F) DISPLAY INTERFACE

See page 725 for ordering information.

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WD55 Industrial Timer/Controller

FEATURES:

- LOW COST PREPROGRAMMED MICROCONTROLLER
- USEABLE WITH KEYBOARD OR DISCRETE SWITCHES
- HIGH CURRENT LED OUTPUTS OR DIRECT DRIVE OF VACUUM FLUORESCENT (V-F) DISPLAYS
- UP TO 7 SEQUENTIAL OUTPUTS
- SYNCHRONIZED WITH 50/60 HZ TIME BASE OR EXTERNAL OSCILLATOR
- SINGLE TIME OPTION
- CONTINUOUS OR SEMI-AUTOMATIC OPTION
- DEDICATED TIMER OPTION-WORKS WITHOUT KEYBOARD OR DISPLAY
- RESOLUTIONS OF FROM 0.1 SEC. TO 999 HOURS WITH DIGITAL ACCURACY
- ALARM OUTPUT FOR AUDIBLE BUZZER
- RELAY AND TRIAC OUTPUTS
- AUDIBLE FEEDBACK FOR USE WITH MEMBRANE SWITCHES
- 100 MW TYPICAL POWER CONSUMPTION

APPLICATIONS:

- DARKROOM TIMER
- PROCESS CONTROLLER
- PROCESS SEQUENCER
- TIME DELAY RELAY
- APPLIANCE TIMERS
- DEFROST CONTROLLERS
- "DRIP" AND "MIST" IRRIGATION CONTROLLERS
- ON/OFF TIMER
- DIGITALLY CONTROLLED TIME DELAY
- TRAFFIC LIGHT SEQUENCER
- SECURITY SYSTEMS
- LIGHTING CONTROL
- INTERVAL TIMER
- RECYCLING TIMER

GENERAL DESCRIPTION

The WD-55 is a versatile, self-contained digital timer/controller/sequencer designed to replace many of the timing and control functions currently being performed by gears, cams, levers, and motors. It is another in a series of "silicon software" preprogrammed microcontrollers based on the WD40 family of 4-bit microprocessors. The WD-55 may be used in conjunction with a matrix keyboard and numeric display to implement a programmable timer/sequencer or with suitable "strap" options, may be used as a dedicated, stand-alone on/off controller. It is implemented in P-channel Silicon Gate MOS and is available in 40 pin plastic and ceramic DIP packages.

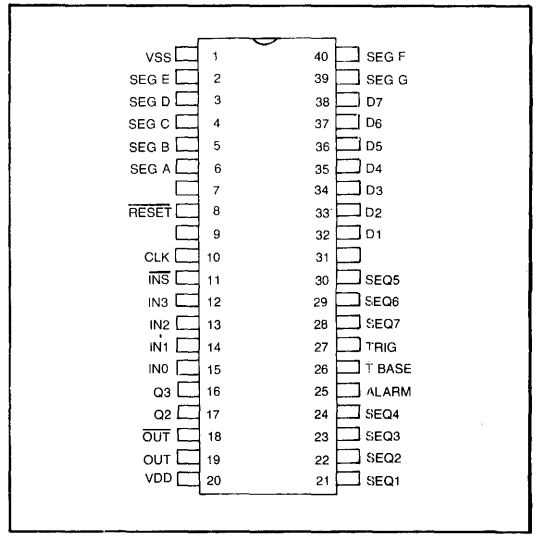


FIGURE 1.
WD-55 PIN CONNECTION

WD-55 PIN DESCRIPTION

PIN NO.	SYMBOL	FUNCTION
1	VSS	+V
2	SEG E	One of 7 high current (20 MA source) outputs for direct LED drive
3	SEG D	One of 7 high current (20 MA source) outputs for direct LED drive
4	SEG C	One of 7 high current (20 MA source) outputs for direct LED drive
5	SEG B	One of 7 high current (20 MA source) outputs for direct LED drive
6	SEG A	One of 7 high current (20 MA source) outputs for direct LED drive
8	$\overline{\text{RESET}}$	Power turn-on reset input, active low
10	CLK	Internal RC clock oscillator output, approx. 100 KHZ
11	INS	Input select, not used in this application
12	IN3	Scanned input, MSB
13	IN2	Scanned input
14	IN1	Scanned input
15	IN0	Scanned input, LSB
16	Q3	Latched output, not used in this application
17	Q2	Latched output, not used in this application
18	$\overline{\text{OUT}}$	Timer output, active low
19	OUT	Timer output, active high
20	VDD	−V
21	SEQ1	One of 7 sequencer outputs, active high during preset timing interval 1
22	SEQ2	One of 7 sequencer outputs, active high during preset timing interval 2
23	SEQ3	One of 7 sequencer outputs, active high during preset timing interval 3
24	SEQ4	One of 7 sequencer outputs, active high during preset timing interval 4
25	ALARM	Audible alarm control output, active high
26	TBASE	Time base input, used as reference for all timing modes
27	TRIG	Trigger input, used in on/off mode, rising edge sensitive
28	SEQ7	One of 7 sequencer outputs, active high during preset timing interval 7
29	SEQ6/TIM2	One of 7 sequencer outputs, active high during preset timing interval 6

WD-55 PIN DESCRIPTION (Continued)

PIN NO.	SYMBOL	FUNCTION
30	SEQ5/TIM1	One of 7 sequencer outputs, active high during preset timing interval 5
31	D0	Digit output, LSD
32	D1	Digit output
33	D2	Digit output
34	D3	Digit output
35	D4	Digit output
36	D5	Digit output
37	D6	Digit output
38	D7	Digit output, MSD
39	SEG F	One of 7 high current (20 MA source) outputs for direct LED drive
40	SEG G	One of 7 high current (20 MA source) outputs for direct LED drive

FUNCTIONAL DESCRIPTION

The WD-55 is a versatile digital timing element designed to replace mechanical timing devices of the synchronous motor, cams, and lever variety. It is a preprogrammed mask-ROM single chip 4-bit microcontroller with different features determined by external strap options. It has essentially two distinct modes of operation: a keyboard programmable timer/sequencer using on-chip RAM for data storage and a 4-digit 7-segment display for data recall, or as an on/off timer which uses thumbwheel switches or even diodes for data storage and recall and does not require a display. These two different modes are selected by the absence or presence of a diode between the D7 digit output (38) and the IN0 scanned input (15). If the diode is absent, upon the occurrence of a reset pulse at pin (8), the device enters the keyboard programmable timer/sequencer mode. If the diode is present, a reset forces the device into the on/off timer mode.

In the timer/sequencer mode, the WD-55 operates with a matrix keyboard and a 4 digit numeric display to form a simple but flexible digital timing device for use in applications such as a dark room timer or programmable sequencer. The configuration table shown in Figure 1 provides the definition of keys, display digits, and strap options.

Keyboard: The WD-55 is useable with a standard 4x4 matrix keyboard (or 3x4 with two off-board switches) of the electromechanical or "membrane" type; audible feedback through the alarm output is provided for use with membrane or other switches which have little or no tactile feel. The debounce time is approximately 100 ms using a 60HZ timebase.

Scanned Input → / Digit Time ↓	IN0 (15)	IN1 (14)	IN2 (13)	IN3 (12)
D0(31)	1	2	3	Start/ Stop
D1(32)	4	5	6	Manual On/Off
D2(33)	7	8	9	1 Seq. Strap
D3(34)	Set/ Clear	0	Advance	50 HZ Strap
D4(35)				
D5(36)				
D6(37)				
D7(38)	NC	.1 sec Strap	Auto-matic	Auto-continuous
OUTPUTS	OUT (19) SEQ1 (21) SEQ5 (30) $\overline{OUT}$ (18) SEQ2 (22) SEQ6 (29) ALARM (25) SEQ3 (23) SEQ7 (28) SEQ4 (24)			
Digit Time →	D3	D2	D1	D0
Seg. a-f	Sequence NR.	MSD	Time	LSD

DISPLAY REGISTER

FIGURE 1. CONFIGURATION TABLE PROGRAMMABLE TIMER/SEQUENCER

KEY DEFINITIONS

ADVANCE: The key is used to access the 7 storage locations in RAM. Each time this key is depressed, the sequence number (digit 3) is incremented by one and the current value of the respective sequence is fetched and displayed in digits D0-D2 (least to most significant). If the current sequence number is 7, depressing the advance key will rollover to sequence #1. If the "1 sequence" strap is present (see strap options), this key is not required.

SET/ CLEAR: This key enables the entry of data into the RAM location currently being displayed by digit 3. When depressed, it enables the "SET" mode and clears display digits D0-D2 to zero as well as the respective memory location. Successive entry of data with the numeric keys (0 through 9) is then allowed. The set mode is terminated by depressing any non-numeric key. Note that there is no need for an "enter" or "store" key since the data displayed on digits D0-D2 is always automatically stored. If "SET/ CLEAR" has not been depressed prior to a numeric key, the numeric key is ignored, preventing the accidental or unwanted entry of data.

MANUAL ON/OFF: This key acts as a push on/ push off switch to manually force the output pins (OUT (19) and $\overline{OUT}$ (18)) to toggle. This is used to manually force an output on, such as in a darkroom timer application where the enlarger needs to be turned on and adjusted before proceeding with a timed interval. These outputs will remain in their current state indefinitely until either the manual key is depressed again or a timed interval is initiated. It has no effect on any of the sequencer outputs, SEQ1-7.

START/STOP: This key is used to initiate or terminate a timed sequence. If a timing cycle is not being performed, depressing this key will initiate a cycle beginning with the sequence currently being displayed in digit 3. If a cycle is currently running, it will terminate it, returning the two complementary outputs (OUT and $\overline{OUT}$) to their normal state and incrementing the sequence digit by 1. In fact, when a timing sequence is currently active, this is the only key which is scanned. This key may be paralleled with an external start/stop or footswitch if dictated by the application.

NUMERIC KEYS (0-9): These keys are used to enter numeric data when in the "SET" mode. Data entry is accomplished by right to left entry; that is, digits 0 to 2 are left-shifted by 1 digit (with the old value of digit 2 discarded) and the most recently depressed numeric key data entered into digit zero. There is no limit to the number of numeric keys which are entered, but only the most recent 3 are displayed and stored. If the "SET/CLEAR" key has not been previously depressed, these keys are ignored.

STRAP CONFIGURATION

Considerable versatility is accomplished with the WD-55 by the use of strap options in the form of diodes to select or delete specific functions. In the timer/sequencer mode, the following options are available.

50 HZ STRAP: The WD55 uses an external time base to accomplish its timing functions. It is optimized for use with 50 or 60 HZ AC line applications. For operation with 60HZ, no strap is necessary. For 50HZ applications, a diode should be connected between D3(34) and IN3(12).

1 SEQ STRAP: This strap (a diode between D2(33) and IN3(12)) forces the device to operate as though it had only 1 time available. At the end of the timed sequence, the SEQ digit does not advance and the SEQ1 data is restored to digits 0-2. When this strap is employed, the advance key should not be used and the sequence digit (Digit 3) is always a "1" and hence could be eliminated.

.1 SEC STRAP: Without this strap, the basic resolution of the 7 sequences is 1 sec. That is, intervals of from 1 to 999 seconds are possible. With a diode (or diode plus SPST switch for variable applications) between D7(38) and IN1(14), the minimum resolution is decreased to .1 seconds; that is, the intervals are now from .1 to 99.9 seconds.

"AUTOMATIC" STRAP: With a diode between D7(38) and IN2(13), the automatic mode is enabled. In this mode, once the START key is depressed, sequences 1 through 7 are executed without further intervention. The cycle stops at the conclusion of sequence 7; that is, SEQ 1 data is being displayed and the keyboard is again being scanned. This is useful when the WD-55 is being used as a sequencer to cycle a complete 7-event sequence.

"AUTOCONTINUOUS" STRAP: This is used in conjunction with the "automatic" strap mentioned previously. If a diode is connected between D7(38) and IN3(12), the device will operate continuously once triggered by the start/stop key. This strap must be connected through a switch, since there is no means of terminating the sequence once initiated. Sequence 7 will be followed immediately by sequence 1. Depressing the start/stop key during the cycle will only terminate the current sequence in progress and begin execution of the next. This mode would typically be used in process control, machine sequencer, "moving lights" displays, etc.

INITIALIZATION

A low going pulse of sufficient duration (see Electrical Data) on the $\overline{RESET}$ pin (8) will force an initialization state, usually as the result of a power-turn-on reset. All 7 sequence times are set to zero and the sequence number digit (Digit 3) is set to "1". The complementary outputs OUT and $\overline{OUT}$ are set to logic LOW and logic HIGH respectively, and all sequencer outputs are logic LOW.

STOPWATCH/ELAPSED TIME CONTROLLER: If a nonzero time is entered into any sequence location, the WD-55 will count that time down to zero before advancing to the next sequence. However, if the stored data is already zero, depressing the START/STOP key will initiate an "UP" count mode starting from zero. The outputs (OUT and SEQ) function as before. If the START/STOP key is activated during this count cycle, the count will stop, the elapsed time will be displayed, the outputs will return to their "off" state, but the sequence number will not advance. This allows the WD55 to act as a "stopwatch" with a cumulative time capability and as an elapsed time controller to time and control a variable event.

ALARM OPERATION

The alarm output (Pin 25) serves several functions in the timer/sequencer mode. First, it provides a .1 sec pulse, active HIGH ("BEEP") whenever a valid key closure is detected. This provides audio feedback for use with non-tactile membrane keyboards. When counting down in a sequence mode, a single "BEEP" is enabled when the count reaches 10.0 seconds, giving an early warning of the end of cycle. When the count reaches zero, two "BEEPS" are output to give audible indication of end of cycle. This output can be buffered and used with self contained buzzers such as a Mallory Sonalert or may be used in conjunction with piezoelectric transducers (see Figure 9).

ON/OFF TIMER MODE

In the ON/OFF timer mode, the WD-55 is programmed to act as a digital programmable timer with one or two time periods which may vary from .1 sec to 999 hours. The data is input to the device by means of switches, thumbwheels, or even diodes. The use of a display is optional, which if employed, will show the current time remaining during each timing cycle. The timebase reference is again externally provided, usually from the 50 or 60 HZ AC line. Strap options are available to instruct the device as to whether it is to run one or two times, whether it is to be operated continuously or in the triggered mode, and whether the BCD switch data is to be interpreted as hours, minutes, or seconds. This mode is intended for use as a digital time delay relay, on/off timer/controller, set point timer, digital one-shot, etc. The timing is performed with digital accuracy and repeatability; it is not dependent upon bulky resistor/capacitor components and their inherent tolerance and temperature problems. For example, the WD-55 can generate a time delay of 999 hours with an accuracy of a fraction of a second with only a handful of diodes as external components, over a temp range of 0 to 55°C, a difficult feat to accomplish by analog means.

The configuration table shown in Figure 2 defines the strap and switch options required in this mode of operation.

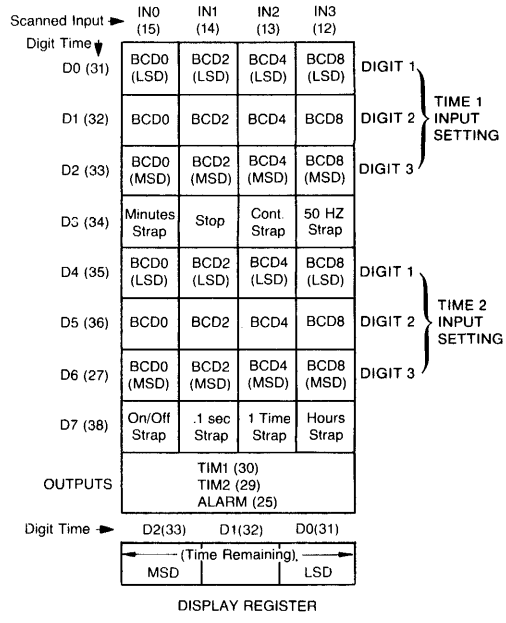


FIGURE 2. CONFIGURATION TABLE ON/OFF TIMER MODE

ON/OFF STRAP: A diode MUST be connected between D7(38) and IN0(15) to inform the WD-55 that it is to operate in this mode. This strap is scanned at the time a reset occurs and causes the microprocessor to access the ON/OFF timer program. Without the strap, the WD-55 will operate as a programmable timer/sequencer as described before.

50 HZ STRAP: As described before, the WD-55 is optimized to use a 50 or 60 HZ timebase. No strap is required for 60 HZ operation. If 50HZ is used, a diode should be connected between D3(34) and IN3(12).

.1 SEC STRAP: If this strap is present (diode between D7(38) and IN1(14)), the input data is evaluated as XX.X secs; that is, times of from .1 to 99.9 seconds are attainable. If this strap is absent and there are no minutes or hours straps present, the data is evaluated as XXX. seconds.

MINUTES STRAP: If a diode is connected between D3(34) and IN0(15), the data is evaluated as XXX minutes. That is, times of from 1 to 999 minutes are attainable.

HOURS STRAP: If a diode is connected between D7(38) and IN3(12), the data is evaluated as XXX hours. That is, times of from 1 to 999 hours are attainable.

TIME 1 STRAP: There are normally two time periods available with the WD-55 which are executed in sequence. If a diode is present between D7(38) and IN2(13), the device will act on only time 1. In other words, when triggered it will count down time 1 to zero, stop, and reload time 1 rather than advancing and loading time 2.

CONTINUOUS STRAP: If this strap is not present, the WD-55 will operate in the "triggered mode". A rising edge (low to high transition) at the trigger input (Pin 27) will initiate a timing cycle beginning with the current time (one or two). At the end of the cycle, the outputs return to their active low state, the next time is loaded and displayed, and the device waits for another trigger input. If a diode is connected between D3(34) and IN2(13), continuous operation is selected. Here the trigger input is ignored. This strap allows the WD-55 to operate as a dedicated purpose timer, such as a defrost controller, which begins operation upon application of power.

STOP INPUT: If an input is detected between D3(34) and IN1(14) during a timing cycle, the cycle will terminate immediately. This can allow a manual overide to stop a cycle in progress. However, if the "CONTINUOUS" strap is present, this input serves only to stop the current timing cycle and cause an advance to the next time.

DATA INPUTS: The time data is input during digit times D0 to D2 (LSD to MSD) for time 1 and during D4 to D6 (LSD to MSD) for time 2 (if used), as shown in the configuration table. The data may be input by means of encoded switches, thumbwheels, or even discrete diodes. The WD-55 has on-chip pull-down resistors across inputs IN0-IN3, so that with the absence of an input during a given digit time is interpreted as a "0". Thus it would be possible to set a time of 080 hours by using only one diode. The data format must be 8421 BCD, with BCD8 connected to IN3 and BCD1 connected to IN0.

TRIGGER (PIN27): If the triggered mode is selected, a positive going transition at this input will initiate a timing cycle. This input is edge sensitive and has an internal pull-up resistor so that a momentary pushbutton switch may be used to manually trigger an event. Since this is not a scanned input, interface to other external logic is simple.

OUTPUTS

TIM1 (30): This output is active HIGH when timing cycle 1 is active, and LOW otherwise.

TIM2 (29): This output is active HIGH when timing cycle 2 is active, and LOW otherwise.

ALARM (25): This output is logic LOW when a timing cycle (1 or 2) is in progress and is logic HIGH otherwise. It may be buffered to drive an audible alarm or it may be used as a third timing output to turn a single device on for two different intervals.

INITIALIZATION

A logic low of sufficient duration on Pin 8 (RESET) will cause initialization of the WD55. In the on/off timer mode, TIM1, TIM2, and alarm will be logic low, and the first time (TIME 1) data is loaded into the display register. If the CONTINUOUS mode is selected, the device will immediately begin counting down time 1, else it will wait for a trigger pulse to occur.

APPLICATIONS CIRCUITS

The following are several circuits designed to give the user an idea of the range of applications that the WD-55 is capable of being utilized.

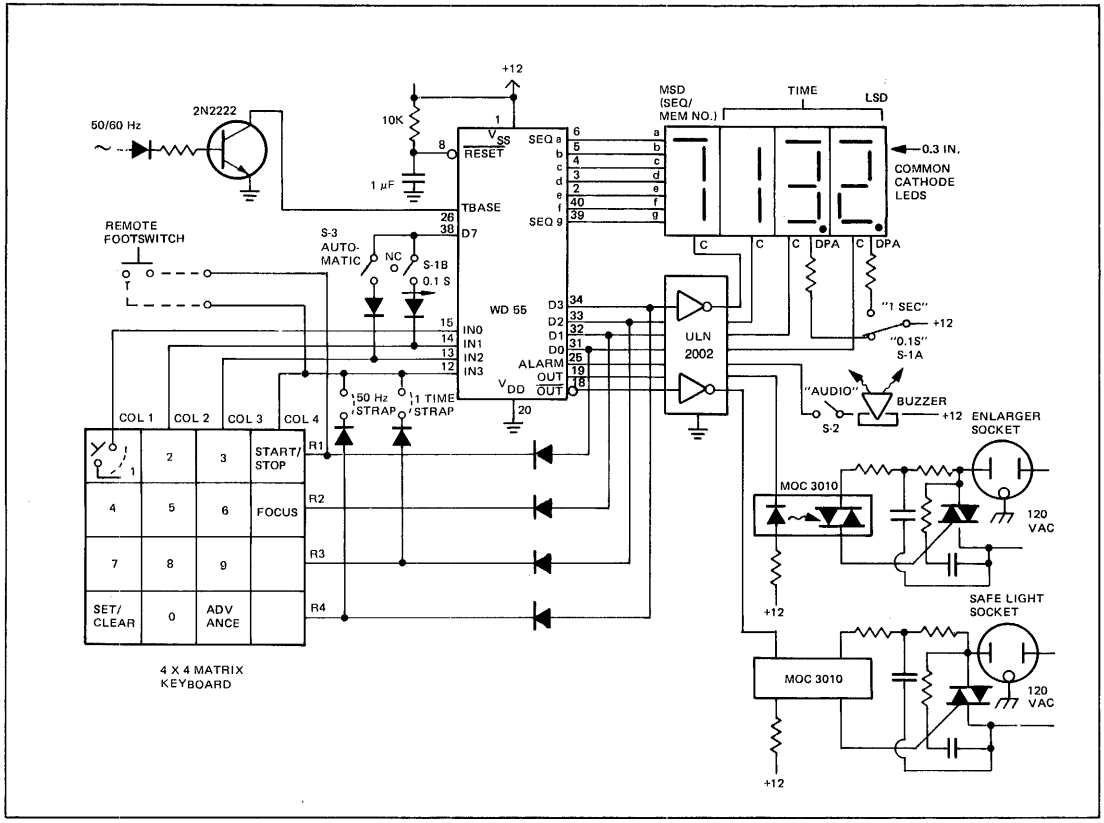


FIGURE 3. DARKROOM TIMER

DARKROOM TIMER

Figure 3 shows a complete schematic (except for power supply) of a dark room timer/controller using the WD-55. Note that the only external components required are a display, a digit driver, keyboard, and output switching devices. A 4-digit common-cathode LED display is used since their inherently red radiation is desirable for dark room environments. Note that the high current sourcing capability of the WD-55 segment outputs allows easy drive of instrument-size LEDS. The time base is provided by shaping up the 50/60HZ AC line input to Pin 26 (TBASE). A complete matrix keyboard is used to allow access to all 7 memory locations. A DPDT switch (S1) is used to select a resolution of .1 or 1 seconds and to simultaneously move the decimal point.

A good dark room timer/controller normally has two switched AC outlets, one for the enlarger and one for the "safe" light. They are the complements of each other in that the safe light is "on" when the enlarger is not active and is "off" when the enlarger is printing. The circuit shown makes use of the complementary outputs OUT (19) and $\overline{\text{OUT}}$ (18) to allow solid-state switching in the form of optically-isolated triacs by buffering them through two unused sections of the high-current digit driver. The value of "snubber" components depends upon the load, which in the case of enlargers and safe lamps is often inductive. If desired, a single SPDT relay may be used in place of the triacs and opto-isolators shown.

The buzzer shown is of the self-contained oscillator variety and operates with DC drive. The WD-55 may also be used with piezoelectric elements (see Figure 9). A switch is provided to disable the beeper when not desired. Another switch (S-3) is used to enable the automatic mode for making up to 7 sequential timed prints by depressing the start key only once. If the possibility of depressing two keys exists, the keyboard should be diode isolated to avoid "sneak" paths.

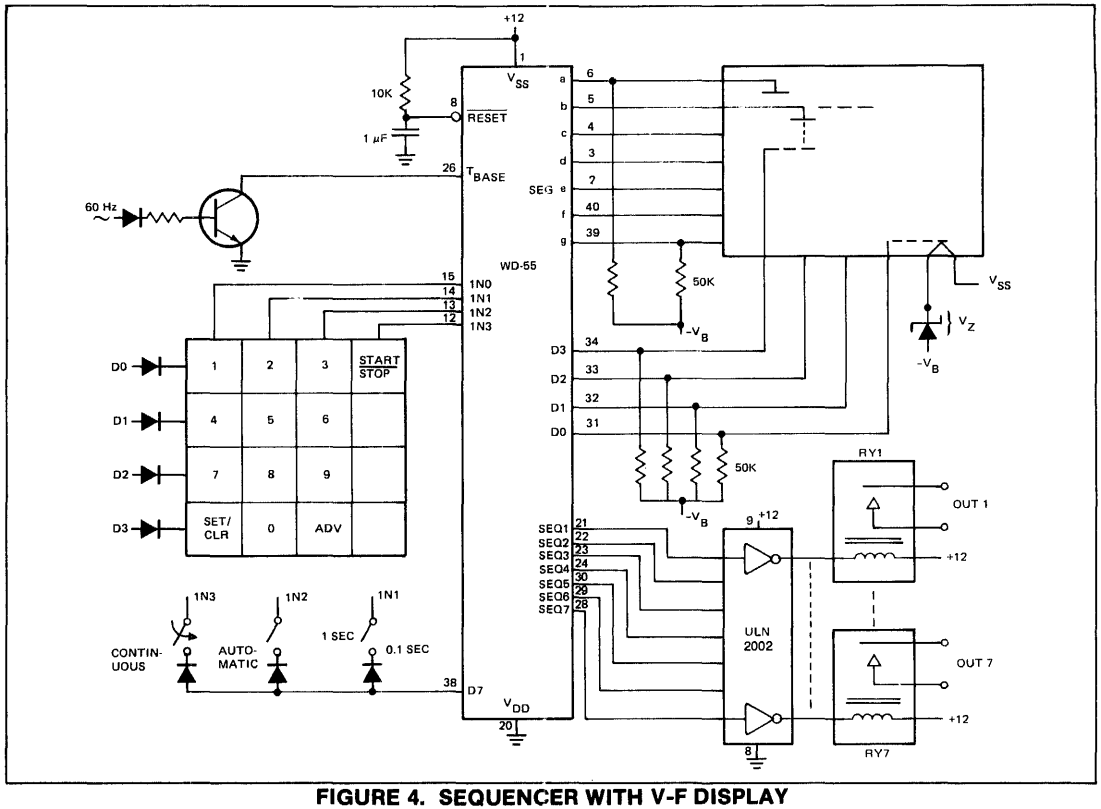


FIGURE 4. SEQUENCER WITH V-F DISPLAY

Figure 4 shows the WD-55 used to implement a keyboard programmable sequencer with 7 outputs. It features a vacuum-fluorescent (V-F) display which takes advantage of the fact that the WD-55 can drive it directly with no high voltage buffers — only external pull-down resistors are required. A conventional matrix keyboard is used as in the dark room timer application. Toggle switches are provided to allow strap options for .1 sec resolution and user-selectable continuous operation. In the auto-continuous mode, once set up, the 7 sequencer outputs will operate in succession to cycle up to 7 processes. The sequencer outputs are buffered by a high current driver interface to 7 relays which perform the output switching task.

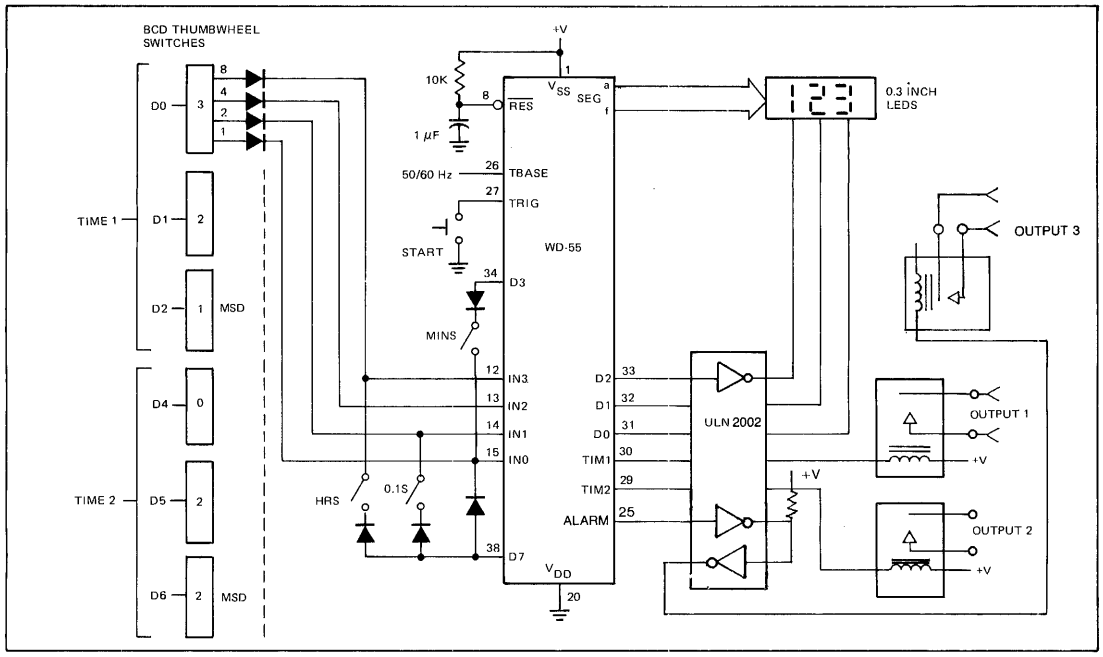


FIGURE 5. THUMBWHEEL PROGRAMMABLE INTERVAL TIMER

Figure 5 shows the WD-55 in its second mode of operation, that of a switch programmable on/off or interval timer. The circuit shown has three relay switched outputs, labelled one, two, and three. Output one is active for the duration of time 1, output two is active for the duration of time 2, and output three is active for the duration of both one and two.

Timing data is input through 6 BCD-encoded thumbwheel switches. Three SPST switches inform the WD-55 to interpret this data as NN.N seconds. NNN seconds, NNN minutes, or NNN hours. The LED display will show the time remaining and the countdown when operating. Since the data is input through switches, the display may be deleted if this feature is not desired. Also, since the timing information is read from switches, the data is non-volatile and no battery backup would be required of the device.

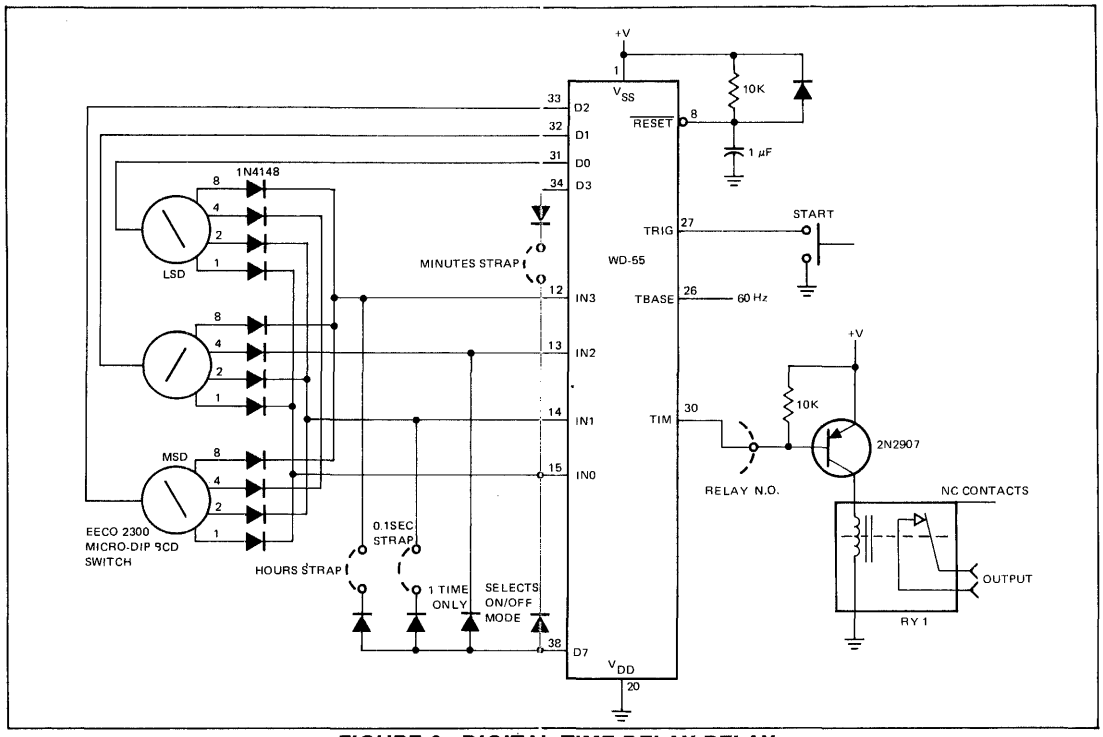


FIGURE 6. DIGITAL TIME DELAY RELAY

Figure 6 shows a digital programmable time delay relay using the WD-55 to give "ON" or "OFF" time delays of from .1S to 999 hours. the "Time 1 only" strap option is used here so that when triggered, the device loads and counts down only one time and then resets. Simple screw-driver slot programmable DIP switches are used here for low cost. Note that a display is not required, but could be added to produce a unique time delay relay with digital readout of time remaining.

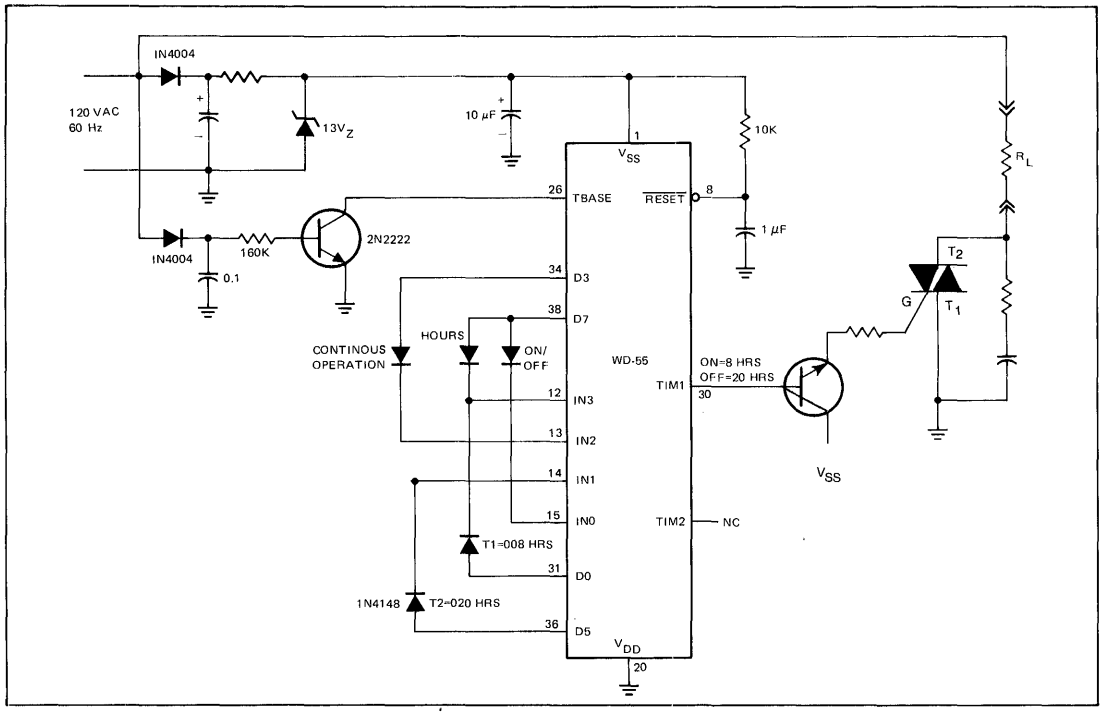


FIGURE 7. ON/OFF CONTROLLER

Figure 7 is an AC line-operated on/off controller. In this application, the WD-55 is programmed simply by diodes and does not require a keyboard, switches, or a display. It is a simple, reliable solid-state alternative to a motor driven cam switch. In this application the non-triggered, two-time mode is selected. Time 1 and Time 2 are programmed by diodes to be 8 hours and 20 hours respectively. The TIM1 output is buffered by a transistor to supply gate current to a triac which switches the output load. When power is applied to the circuit, the output load is switched "ON" for 8 hours then "OFF" for 20 hours repeatedly.

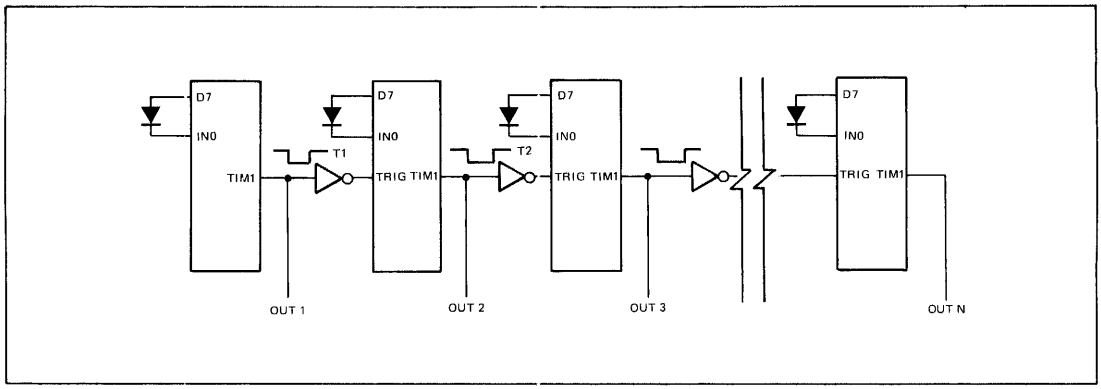


FIGURE 8. DAISY-CHAIN N-SEQUENTIAL INTERVAL CONTROLLER

Finally, Figure 8 shows how multiple, independent WD-55's may be configured for triggered mode operation may operate in daisy chain fashion to produce an N-sequential programmable interval controller.

These are but a few of the many applications for the WD-55. For custom versions, please contact the factory.

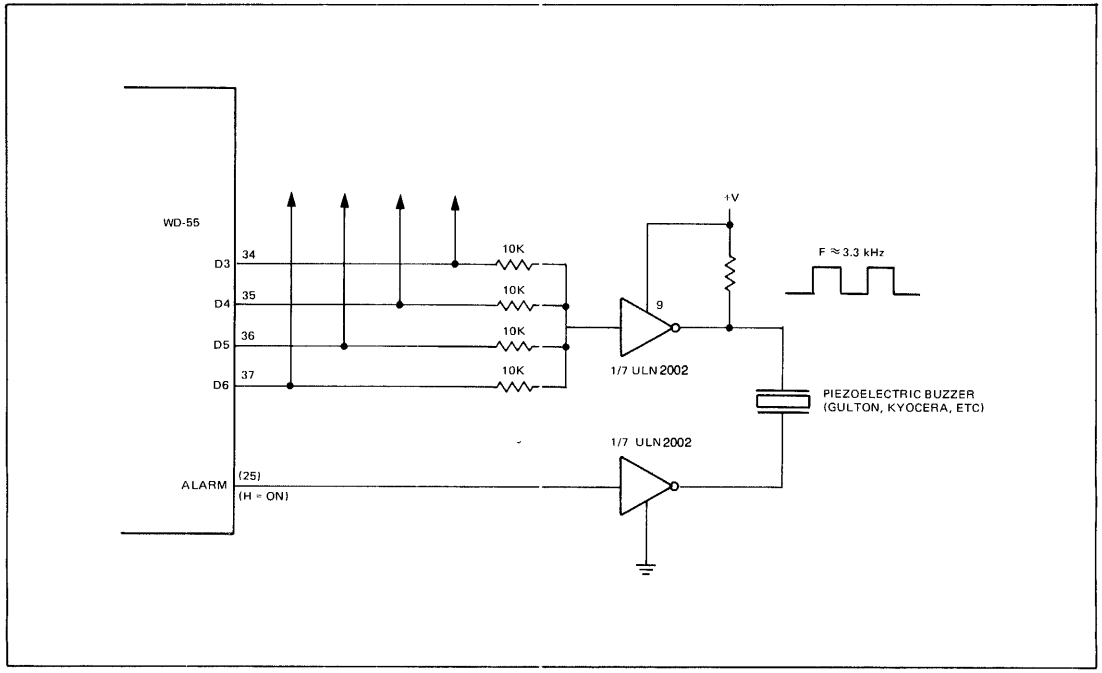


FIGURE 9. WD-55 USED WITH PIEZOELECTRIC BUZZER

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ....−65°C to +150°C Ceramic
−55°C to +125°C Plastic
Operating Free-Air Temperature
T Range ..... 0°C to 70°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C
Power Dissipation 2.5 Watt at 25°C
Positive Voltage on any Pin with Respect to V_{SS}: +0.3V
Negative Voltage on any Pin with Respect to V_{SS}: 20.0V

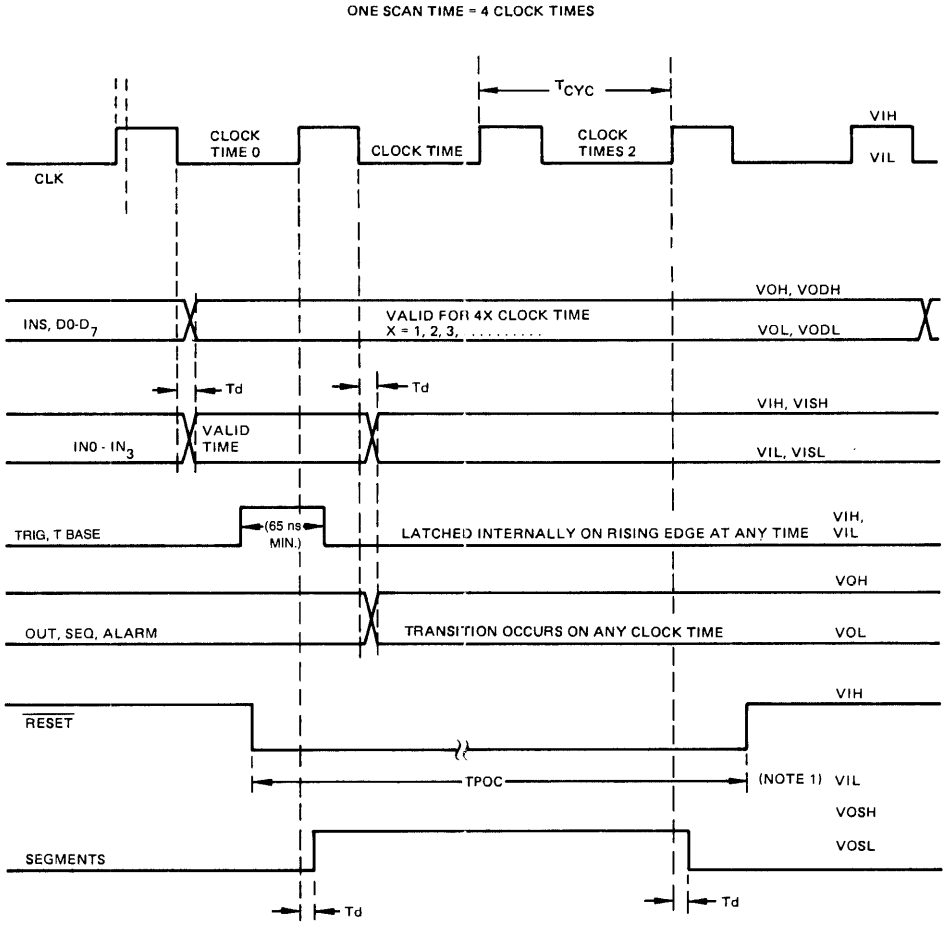
Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

ELECTRICAL CHARACTERISTICS

TA = 25°C, $V_{SS}-V_{DD}$ = 13.2V unless noted otherwise

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage (V_{SS}-V_{DD})		11.5	13.2	14.5	V
Operating Current	All inputs and outputs open	6		15	mA
Input Voltage Levels					
All Inputs Except IN0-IN3					
Logic High (V_{IH})	Note 1	$V_{SS}-1$		V_{SS}	V
Logic Low (V_{IL})		V_{DD}		$V_{DD}-4.2$	V
Inputs IN0−IN3	Note 2				
Logic High (V_{ISH})		$V_{SS}-3.75$		V_{SS}	V
Logic Low (V_{ISL})		V_{DD}		$V_{SS}-9.0$	V
Output Voltage Levels					
All Outputs Except D0-D7 and SA-SG					
Logic High (V_{OH})	I_{OH}=+100 μA Min.	$V_{SS}-2$		V_{SS}	V
Logic Low (V_{OL})	I_{OL}=−1.6 mA Min.	V_{DD}		$V_{SS}-4.6$	V
D0-D7 Outputs					
Logic High (V_{ODH})	I_{ODH}=1.5 mA	$V_{SS}-1.5$		V_{SS}	V
	I_{ODH}=1.5 mA+I Input (IN0-IN3)	$V_{SS}-3.0$		V_{SS}	V
	I_{ODH}=5.0 mA+1 Input	$V_{SS}-3.5$		V_{SS}	V
V_{ODL}	Note 3				
Seg Outputs Seg a-f	I_{OSH}=16 mA			1.0	V
Segment Output Current Seg a-f I_{OSH}	Note 3	10	15	40	mA
AC Electrical					
TcYC			10		μs
$\overline{\text{Reset}}$		15			msec
TBase		0	60	500	HZ
Timing error (TOUT)	Note 4			±1	ms

Note 1: Internal Pullup Resistors of Approximately 6K to V_{SS} Across Each Input.
Note 2: Internal Pulldown Resistors of Approximately 12K to V_{DD} Across Each Input.
Note 3: Single Transistor to V_{SS} Output Only.
Note 4: TBase = 60.000 HZ.



NOTE 1: RISING EDGE OF $\overline{\text{RESET}}$ GENERATES SCAN TIME 0 WITHIN 4 CLOCK TIMES

Note 2: td = μs MAX

WD-55 TIMING DIAGRAM

See page 725 for ordering information.

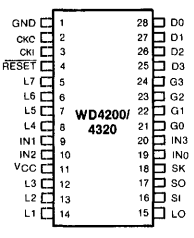
WD4200/WD4210 and WD4320/WD4321 Single-Chip N-Channel Microcontrollers

FEATURES

- Low cost
- Powerful instruction set
- 1K x 8 ROM, 64 x 4 RAM
- 23 I/O lines
- True vectored interrupt, plus restart
- Three-level subroutine stack
- 4.0 μs instruction time
- Single supply operation (4.5V to 6.3V)
- Internal time-base counter for real-time processing
- Internal binary counter register with serial I/O capability
- General purpose and TRI-STATE® outputs
- TTL/CMOS compatible in and out
- LED direct drive outputs
- MICROBUS™ compatible
- Software/hardware compatible with other members of WD4200 family
- Extended temperature range device available (−40°C to +85°C) WD4320/4321

GENERAL DESCRIPTION

The WD4200/4320 and WD4210/4321 Single Chip N-Channel Microcontrollers are members of the Control Oriented Processor family, fabricated using N-channel, silicon gate MOS technology. They are complete microcomputers containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The WD4210/4321 is identical to the WD4200/4320, except with 19 I/O lines instead of 23. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized Control Oriented Processor at a low end-product cost.



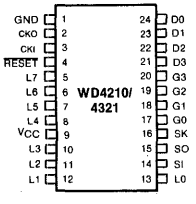


Figure 1
PIN CONNECTIONS

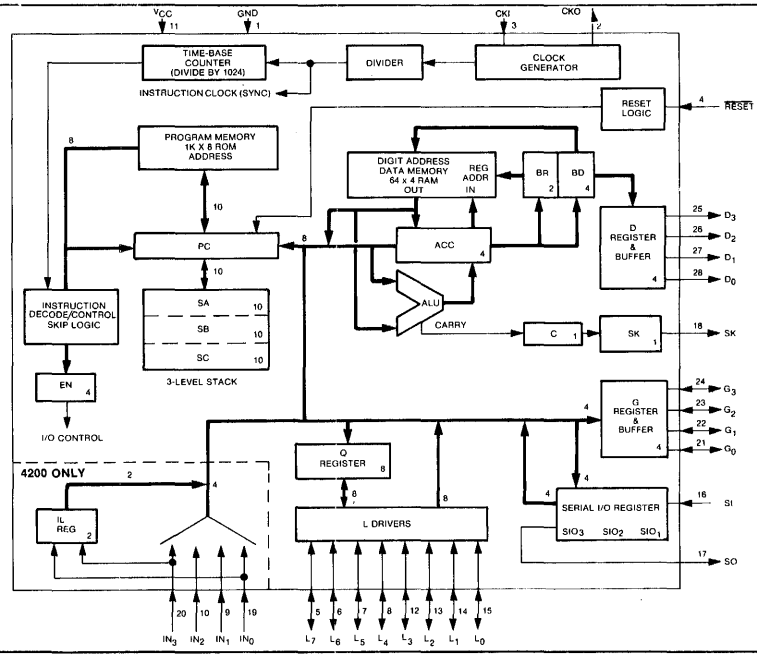


Figure 2 WD4200/4210 AND 4320/4321 BLOCK DIAGRAM

PIN DESCRIPTION	
L_7-L_0	8 bidirectional I/O ports with TRI-STATE®
G_3-G_0	4 bidirectional I/O ports
D_3-D_0	4 general purpose outputs
IN_3-IN_0	4 general purpose inputs (WD4200 only)
SI	Serial input (or counter input)
SO	Serial output (or general purpose output)
SK	Logic-controlled clock (or general purpose output)
CKI	System oscillator input
CKO	System Oscillator output (or general purpose input or RAM power supply)
$\overline{\text{RESET}}$	System reset input
V_{CC}	Power supply
GND	Ground

FUNCTIONAL DESCRIPTION

A block diagram of the WD4200 is given on page 1. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is logic "1" (greater than 2 volts). When a bit is reset, it is a logic "0" (less than 0.8 volts).

Program Memory

Program Memory consists of a **1,024-byte ROM.** As can be seen by an examination of WD4200/4210 instruction set, these words may be program instructions, program data or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID and LQID instructions, ROM must often be thought of as being organized into 16 pages of 64 words each.

ROM addressing is accomplished by a **10-bit PC register.** Its binary value selects one of the 1,024 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 10-bit binary count value. Three levels of subroutine nesting are implemented by the **10-bit subroutine save registers, SA, SB and SC,** providing a last-in, first-out (LIFO) hardware subroutine stack.

ROM instruction words are fetched, decoded and executed by the Instruction Decode, Control and Skip Logic circuitry.

Data Memory

Data Memory consists of a **256-bit RAM,** organized as four data registers of 16 4-bit digits. RAM addressing is implemented by a **6-bit B** register whose upper two bits (Br) select one of four data registers and lower 4 bits (Bd) select one of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected **RAM digit (M)** is usually loaded into or from, or exchanged with, the A register (accumulator), it may also be loaded into or from the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the 6-bit contents of the operand field of these instructions. The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

Internal Logic

The 4-bit **A register** (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Br and Bd portions of the B register, to load and input four bits of the 8-bit Q latch data, to input four bits of the 8-bit L I/O port data and to perform data exchanges with the SIO register.

A **4-bit adder** performs the arithmetic and logic functions of the WD4200/4210, storing its results in A. It also outputs a carry bit to the 1-bit **C register,** most often employed to indicate arithmetic overflow. The C register, in conjunction with XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time (see XAS instruction and EN register description below).

Four **general-purpose inputs,** IN_3-IN_0, are provided; IN_1, IN_2 and IN_3 may be selected, by a mask-programmable option, as Read Strobe, Chip Select and Write Strobe inputs, respectively, for use in MICROBUS™ applications.

The **D register** provides four general-purpose outputs and is used as the destination register for the 4-bit contents of Bd.

The **G register** contents are outputs to four general-purpose bidirectional I/O ports. G_0 may be mask-programmed as an output for MICROBUS™ applications.

The **Q register** is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are output to the L I/O ports when the L drivers are enabled under program control (see LEI instruction). With the MICROBUS™ option selected, Q can also be loaded with the 8-bit contents of the L I/O ports upon the occurrence of a write strobe from the host CPU.

The **eight L drivers,** when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and M. As explained above, the MICROBUS™ option allows L I/O port data to be latched into the Q

register. L I/O ports can be directly connected to the segments of a multiplexed LED display (using the LED Direct Drive output configuration option) with Q data being outputted to the Sa-Sg and decimal point segments of the display.

The **SIO register** functions as a 4-bit serial-in/serial-out shift register or as a binary counter depending on the contents of the EN register (see EN register description below). Its contents can be exchanged with A, allowing it to input or output a continuous serial data stream. SIO may also be used to provide additional parallel I/O by connecting SO to external serial-in/serial-out shift registers. For example of additional parallel output capacity, see Application No. 2.

The **EN register** is an internal 4-bit register loaded under program control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN_3-EN_0).

1. The least significant bit of the enable register, EN_0, selectes the SIO register as either a 4-bit shift register or a 4-bit binary counter. With EN_0 set, SIO is an asynchronous binary counter, *decrementing* its value by one upon each low-going pulse ("1" to "0") occurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of C upon execution of XAS and remains the same until the execution of another XAS instruction. The SO output is equal to the value of EN_3. With EN_0 reset, SIO is a serial shift register shifting left each instruction cycle time. The data present at SI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time (see 4 below). The SK output becomes a logic-controlled clock, providing a SYNC signal each instruction time. It will start outputting a SYNC pulse upon the execution of an XAS instruction with C = 1, stopping upon the execution of a subsequent XAS with C = 0.
2. With EN_1 set the IN_1 input is enabled as an interrupt input. Immediately following an interrupt, EN_1 is reset to disable further interrupts.
3. With EN_2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN_2 disables the L drivers, placing the L I/O ports in a high-impedance input state. If the MICROBUS™ option is being used, EN_2 does not affect the L drivers.
4. EN3, in conjunction with EN_0, affects the SO output. With EN_0 set (binary counter option selected) SO will output the value loaded into EN_3. With EN_0 reset (serial shift register option selected), setting EN_3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN_3 with the serial shift register option selected disables SO as the shift register output: data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0". The table below provides a summary of the modes associated with EN_3 and EN_0.

Interrupt

The following features are associated with the IN_1 interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

a. The interrupt, once acknowledged as explained below, pushes the next sequential program counter address (PC + 1)onto the stack, pushing in turn the contents of the other subroutine-save register to the next lower level (PC+1 → SA → SB → SC). Any previous contents of SC are lost. The program counter is set to hex address 0FF (the last word of page 3) and EN_1 is reset.

b. An interrupt will be acknowledged only after the following conditions are met:
   1) EN_1 has been set.
   2) A low-going pulse ("1" to "0") of at least two instruction cycles wide occurs on the IN_1 input.
   3) A currently executing instruction has been completed.

ENABLE REGISTER MODES — BITS EN_3 AND EN_0

EN3	EN0	SIO	SI	SO	SK AFTER XAS
0	0	Shift Register	Input to Shift Register	0	If C = 1, SK = SYNC If C = 0, SK = 0
1	0	Shift Register	Input to Shift Register	Serial Out	If C = 1, SK = SYNC If C = 0, SK = 0
0	1	Binary Counter	Input to Binary Counter	0	If C = 1, SK = 1 If C = 0, SK = 0
1	1	Binary Counter	Input to Binary Counter	1	If C = 1, SK = 1 If C = 0, SK = 0

4) All successive transfer of control instructions and successive LBIs have been completed (e.g., if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed.

c. Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon the execution of a subsequent RET instruction. For example, if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address 0FF. At the *end* of the interrupt routine, a RET instruction is executed to "pop" the stack and return program control to the instruction following the original ASC. *At this time*, the skip logic is enabled and skips this instruction because of the previous ASC carry. Since, as explained above, it is the RET instruction which enables the previously saved status of the skip logic, subroutines should not be nested within the interrupt servicing routine since their RET instruction will enable any previously saved main program skips, interfering with the orderly execution of the interrupt routine.

d. The first instruction of the interrupt routine at hex address 0FF must be a NOP.

e. A LEI instruction can be put immediately before the RET to re-enable interrupts.

MICROBUS™ Interface

The WD4200 has an option which allows it to be used as a peripheral microprocessor device, inputting and outputting data from and to a host microprocessor (μP). IN_1, IN_2, and IN_3 general purpose inputs become MICROBUS™ compatible read-strobe, chip-select, and write-strobe lines, respectively. **IN_1 becomes $\overline{RD}$** — a logic "0" on this input will cause Q latch data to be enabled to the L ports for input to the μP. **IN_3 becomes $\overline{CS}$** — a logic "0" on this line selects the WD4200 as the μP peripheral device by enabling the operation of the $\overline{RD}$ and $\overline{WR}$ lines and allows for the selection of one of several periopheral components. **IN_3 becomes $\overline{WR}$** — a logic "0" on this line will write bus data from the L ports to the Q latches for input to the WD4200. **G_0 becomes INTR** a "ready" output, reset by a write pulse from the μP on the WR line, providing the "hand-shaking" capability necessary for asynchronous data transfer between the host CPU and the WD4200.

This option has been designed for compatibility with National's MICROBUS™ - a standard interconnect system for 8-bit parallel data transfer between MOS/LSI CPUs and interfacing devices. (See MICROBUS™, National Publication.) The functioning and timing relationships between the WD4200 signal lines affected by this option are as specified for the MICROBUS™ interface, and are given in the AC electrical characteristics and shown in the timing diagrams (figures 11 and 12). Connection of the WD4200 to the MICROBUS™ is shown in MICROBUS™ Option interconnect illustration.

Initialization

The Reset Logic, internal to the WD4200/4210 will initialize (clear) the device upon power-up if the power supply rise time is less than 1 ms and greater than 1 μs. If the power supply rise time is greater than 1 ms, the user must provide an external RC network and diode to the $\overline{RESET}$ pin as shown below. The $\overline{RESET}$ pin is configured as a Schmitt trigger input. If not used it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the $\overline{RESET}$ input, provided it stays low for at least two instruction cycle times.

Upon initialization, the **PC register is cleared** to 0 (ROM address 0) and the **A, B, C, D, EN, and G registers are cleared. The SK output is enabled as a SYNC output,** providing a pulse each instruction cycle time. *Data Memory (RAM) must be cleared by the user's program.* The first instruction at address 0 must be a CLRA.

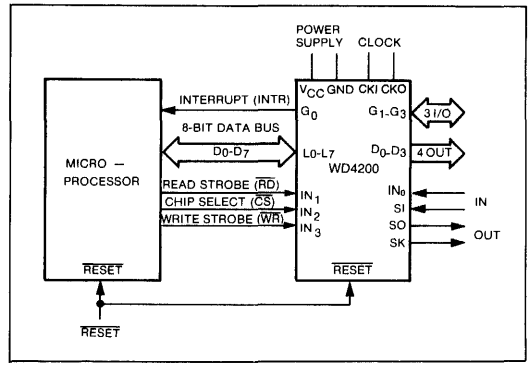


Figure 3 **MICROBUS™ OPTION INTERCONNECT**

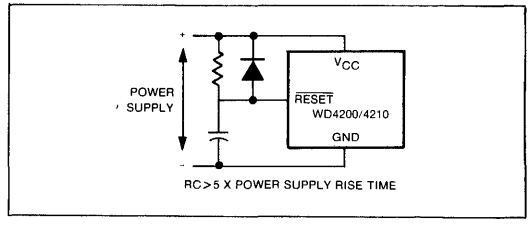


Figure 4 **POWER-UP CLEAR CIRCUITS**

Oscillator

There are four basic clock oscillator configurations available as shown below.

a. **Crystal Controlled Oscillator.** CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency divided by 16 (optional by 8).

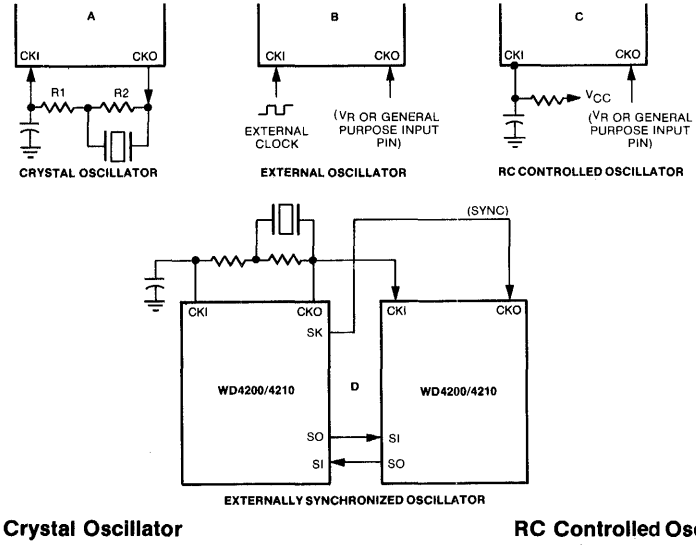
b. **External Oscillator.** CKI is configured as a TTL compatible input accepting an external clock signal. The external frequency is divided by 16 (optional by 8 or 4) to give the instruction cycle time. CKO is now available to be used as the RAM power supply (V_R) or as a general purpose input.

c. **RC Controlled Oscillator.** CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is available for non-timing functions.

d. **Externally Synchronized Oscillator.** Intended for use in multi-WD systems, CKO is programmed to function as an input connected to the SK output of another WD4200/4210 with CKI connected as shown. In this configuration, the SK output connected to CKO must provide a SYNC (instruction cycle) signal to CKO, thereby allowing synchronous data transfer between the WDs using only the SI and SO serial I/O pins in conjunction with the XAS instruction. Note that on power-up SK is automatically enabled as a SYNC output (see Functional Description, Initialization, above).

CKO Pin Options

In a crystal controlled oscillator system, CKO is used as an **output to the crystal network.** As an option CKO can be a **general purpose input,** read into bit 2 of A (accumulator) upon execution of an INIL instruction. As another option, CKO can be a **RAM power supply** pin (V_R), allowing its connection to be a standby/backup power supply to maintain the integrity of RAM data with minimum power drain when the main supply is inoperative or shut down to conserve power. Using either option is appropriate in applications where the WD4200/4210 system timing configuration does not require use of the CKO pin.



Crystal Oscillator

Crystal Value	Component Values		
	R1	R2	C
4 MHz	1K	1M	27 pF
3.58 MHz	1K	1M	27 pF
2.09 MHz	1K	1M	56 pF

RC Controlled Oscillator

R (kΩ)	C (pF)	Instruction Cycle Time in μs
12	100	5± 20%
6.8	220	5.3 ± 23%
8.2	300	8 ± 29%
22	100	8.6 ± 16%

Figure 5 WD4200/4210 OSCILLATOR

I/O Options

WD4200/4210 outputs have the following optional configurations, illustrated below.

a. **Standard.** An enhancement-mode device to ground in conjunction with a depletion-mode device to V_{CC} compatible with TLL and CMOS input requirements.

b. **Open-Drain.** An enhancement-mode device to ground only, allowing external pull-up as required by the user's application.

c. **Push-Pull.** An enhancement-mode device to ground in conjunction with a depletion-mode device paralleled by an enhancement-mode device to V_{CC}. This configuration has been provided to allow for fast rise and fall times when driving capacitive loads.

d. **LED Direct Drive.** An enhancement-mode device to ground and to V_{CC}, meeting the typical current sourcing requirements of the segments of an LED display. The sourcing device is clamped to limit current flow. These devices may be turned off under program control (see Functional Description, EN Register), placing the outputs in a high-impedance state to provide required LED segment blanking for a multiplexed display.

e. **Three-State Push-Pull.** An enhancement-mode device to ground and V_{CC} intended to meet the requirements associated with the MICROBUS™ option. These outputs are TRI-STATE® outputs, allowing for connection of these outputs to a data bus shared by other bus drivers.

WD4200/4210 inputs have the following optional configurations:

f. An on-chip depletion **load device to V_{CC}.**

g. **A Hi-Z input** which must be driven to a "1" or "0" by external components.

The above input and output configurations share common enhancement-mode and depletion-mode devices. Specifically, all configurations use one or more of six devices (numbered 1-6, respectively). Minimum and maximum current (I_{OUT} and V_{OUT}) curves are given on figure 7 for each of these devices to allow the designer to effectively use these I/O configurations in designing a WD4200/4210 system.

The SO, SK outputs can be configured as shown in A, B, or C. The D and G outputs can be configured as shown in A or B. Note that when inputting data to the G ports, the G outputs should be set to "1". The L outputs can be configured as A, B, D, or E.

An important point to remember if using configuration A or D with the L drivers is that even when the L drivers are disabled, the depletion load device will source a small amount of current.

WD4210

If the WD4200 is bonded as a 24-pin device, it becomes the WD4210, illustrated in figure 1, WD4200/4210 Connection Diagrams. Note that the WD4210 does not contain the four general purpose IN inputs (IN_3-IN_0). Use of this option precludes, of course use of the IN options, interrupt feature, and the MICROBUS™ option which uses IN_1-IN_3. All other options are available for the WD4210.

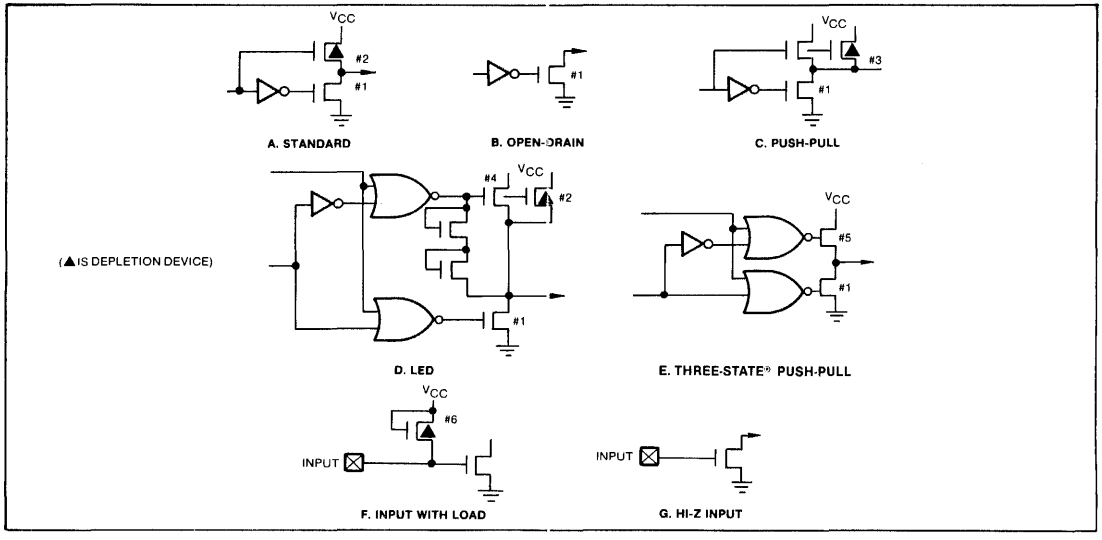


Figure 6 OUTPUT CONFIGURATIONS

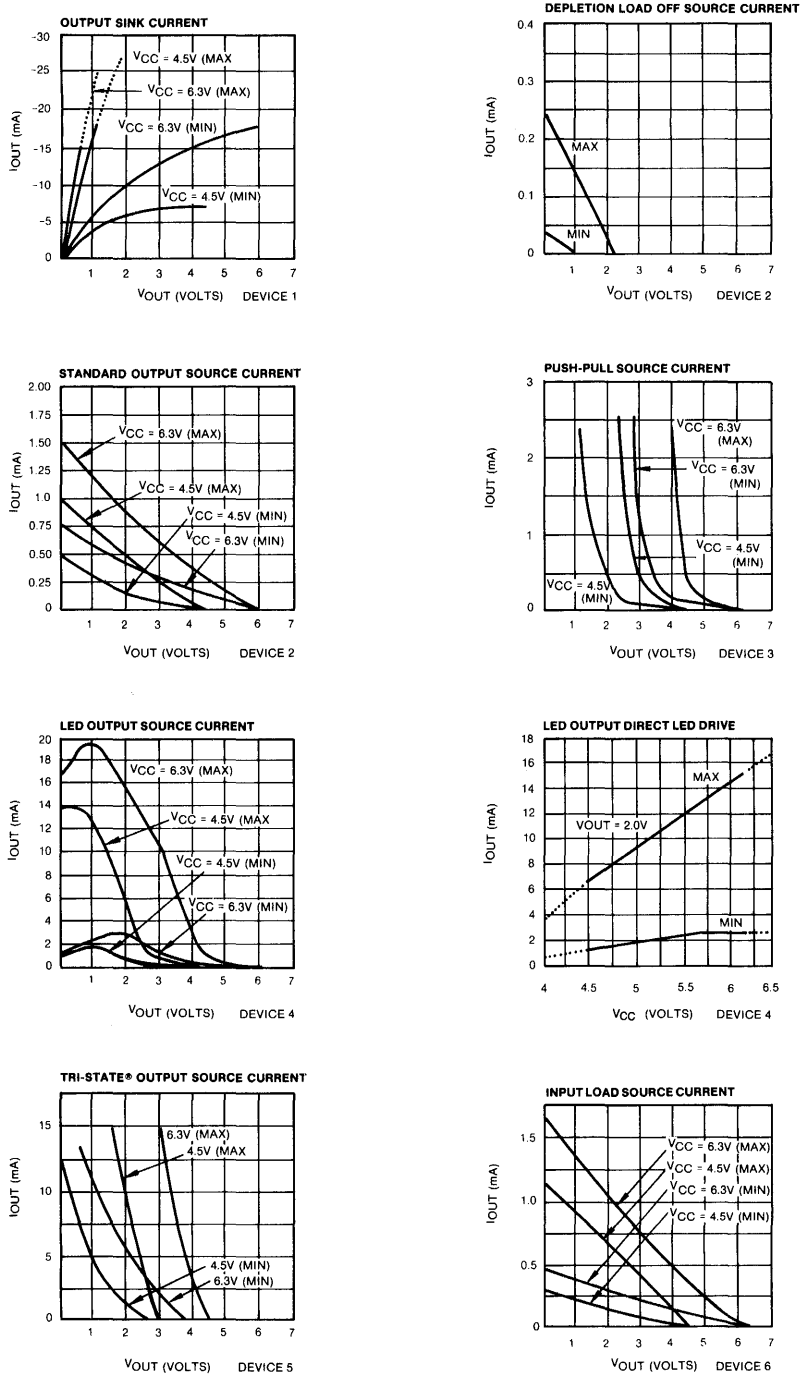


Figure 7 WD4200/4210 OUTPUT CHARACTERISTICS

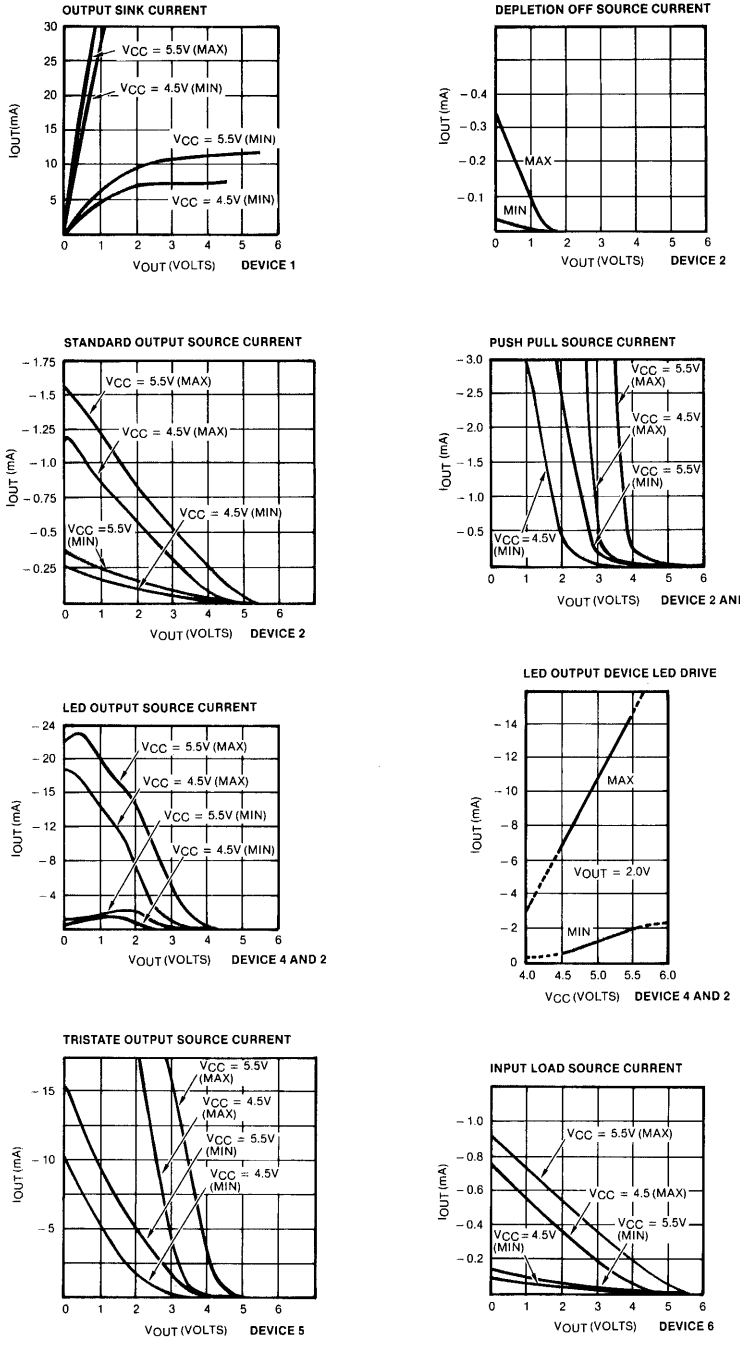


Figure 8 WD4320/4321 OUTPUT CHARACTERISTICS

WD4200/4210 INSTRUCTION SET

Table 1 is a symbol table providing internal architecture, instruction operand, and operational symbols used in the instruction set table.

Table 2 provides the mnemonic, operand, machine code, data flow, skip conditions, and description associated with each instruction in the WD4200/4210 instruction set.

TABLE 1. WD4200/4210 INSTRUCTION SET TABLE SYMBOLS

Symbol	Definition	Symbol	Definition
INTERNAL ARCHITECTURE SYMBOLS		**INSTRUCTION OPERAND SYMBOLS**	
A	4-bit Accumulator	d	4-bit Operand Field, 0-15 binary (RAM Digit Select)
B	6-bit RAM Address Register	r	2-bit Operand Field, 0-3 binary (RAM Register Select)
Br	Upper 2 bits of B (register address)	a	10-bit Operand Field, 0-1023 binary (ROM Address)
Bd	Lower 4 bits of B (digit address)	y	4-bit Operand Field, 0-15 binary (Immediate Data)
C	1-bit Carry Register	RAM(s)	Content and RAM location addressed by s
D	4-bit Data Output Port	ROM(t)	Content and ROM location addressed by t
EN	4-bit Enable Register		
G	4-bit Register to latch data for G I/O Port		
IL	Two 1-bit Latches associated with the IN_3 or IN0 Inputs	**OPERATIONAL SYMBOLS**	
IN	4-bit Input Port	+	Plus
L	8-bit TRI-STATE® I/O Port	-	Minus
M	4-bit contents of RAM Memory Pointed to by B Register	→	Replaces
PC	10-bit ROM Address Register (program counter)	↔	Is exchanged with
Q	8-bit Register to latch data for L I/O Port	=	Is equal to
SA	10-bit Subroutine Save Register A	$\overline{A}$	The ones complement of A
SB	10-bit Subroutine Save Register B	⊕	Exclusive-OR
SC	10-bit Subroutine Save Register C	:	Range of values
SIO	4-bit Shift Register and Counter		
SK	Logic-Controlled Clock Output		

TABLE 2. WD4200/4210 INSTRUCTION SET TABLE (Note 1)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	0 0 1 1 | 0 0 0 0	A + C + RAM(B) → A Carry → C	Carry	Add with Carry, Skip on Carry
ADD		31	0 0 1 1 | 0 0 0 1	A + RAM(B) → A	None	Add A to RAM
ADT		4A	0 1 0 0 | 1 0 1 0	A + 10_{10} → A	None	Add Ten to A
AISC	y	5-	0 1 0 1 | y	A + y → A	Carry	Add Immediate, Skip on Carry (y ≠ 0)
CASC		10	0 0 0 1 | 0 0 0 0	$\overline{A}$ + RAM(B) + C → A Carry → C	Carry	Complement and Add with Carry, Skip on Carry
CLRA		00	0 0 0 0 | 0 0 0 0	0 → A	None	Clear A
COMP		40	0 1 0 0 | 0 0 0 0	$\overline{A}$ → A	None	Ones complement of A to A
NOP		44	0 1 0 0 | 0 1 0 0	None	None	No Operation
RC		32	0 0 1 1 | 0 0 1 0	"0" → C	None	Reset C
SC		22	0 0 1 0 | 0 0 1 0	"1" → C	None	Set C
XOR		02	0 0 0 0 | 0 0 1 0	A ⊕ RAM(B) → A	None	Exclusive-OR A with RAM

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
TRANSFER OF CONTROL INSTRUCTIONS						
JID		FF	1 1 1 1 | 1 1 1 1	ROM (PC9:8, A, M) → $PC_{7:0}$	None	Jump Indirect (Note 3)
JMP	a	6_	0 1 1 0 | 0 0 | $a_{9:8}$	a → PC	None	Jump
		--	$a_{7:0}$			
JP	a	--	1 | $a_{6:0}$ (Pages 2, 3 only)	a → $PC_{6:0}$	None	Jump within Page (Note 4)
			or			
		--	1 1 | $a_{5:0}$ (all other pages)	a → $PC_{5:0}$		
JSRP	a	--	1 0 | $a_{5:0}$	PC + 1 → SA → SB → SC 0010 → $PC_{9:6}$ a → $PC_{5:0}$	None	Jump to Subroutine Page (Note 5)
JSR	a	6_	0 1 1 0 | 1 0 $a_{9:8}$	PC + 1 → SA → SB → SC a → PC	None	Jump to Subroutine
		--	$a_{7:0}$			
RET		48	0 1 0 0 | 1 0 0 0	SC → SB → SA → PC	None	Return from Subroutine
RETSK		49	0 1 0 0 | 1 0 0 1	SC → SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip
MEMORY REFERENCE INSTRUCTIONS						
CAMQ		33	0 0 1 1 | 0 0 1 1	A → $Q_{7:4}$ RAM(B) → $Q_{3:0}$	None	Copy A, RAM to Q
		3C	0 0 1 1 | 1 1 0 0			
CQMA		33	0 1 1 0 | 0 1 1 1	$Q_{7:4}$ → RAM(B) $Q_{3:0}$ → A	None	Copy Q to RAM, A
		2C	0 0 1 0 | 1 1 0 0			
LD	r	_5	0 0 | r | 0 1 0 1	RAM(B) → A $BR^{\oplus}$ r → Br	None	Load RAM into A, Exclusive-OR Br with r
LDD	r, d	23	0 0 1 0 | 0 0 1 1	RAM(r,d) → A	None	Load A with RAM pointed to directly by r, d
		--	0 0 | r | d			
LQID		BF	1 0 1 1 | 1 1 1 1	ROM($PC_{9:8}$, A, M) → Q SB → SC	None	Load Q Indirect (Note 3)
RMB	0	4C	0 1 0 0 | 1 1 0 0	0 → $RAM(B)_0$	None	Reset RAM Bit
	1	45	0 1 0 0 | 0 1 0 1	0 → $RAM(B)_1$		
	2	42	0 1 0 0 | 0 0 1 0	0 → $RAM(B)_2$		
	3	43	0 1 0 0 | 0 0 1 1	0 → $RAM(B)_3$		
SMB	0	4D	0 1 0 0 | 1 1 0 1	1 → $RAM(B)_0$	None	Set RAM Bit
	1	47	0 1 0 0 | 0 1 1 1	1 → $RAM(B)_1$		
	2	46	0 1 0 0 | 0 1 1 0	1 → $RAM(B)_2$		
	3	4B	0 1 0 0 | 1 0 1 1	1 → $RAM(B)_3$		

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
MEMORY REFERENCE INSTRUCTIONS (Continued)						
STII	y	7_	0 1 1 1 | y	y → RAM(B) Bd + 1 → Bd	None	Store Memory Immediate and Increment Bd
X	r	_6	0 0 | r | 0 1 1 0	RAM(B) ↔ A Br ⊕ r → Br	None	Exchange RAM with A, Exclusive OR Br with r
XAD	r, d	23	0 0 1 0 | 0 0 1 1	RAM(r,d) ↔ A	None	Exchange A with RAM pointed to directly by r, d
		--	1 0 | r | d			
XDS	r	_7	0 0 | r | 0 1 1 1	RAM(B) ↔ A Bc - 1 → Bd Br⊕ r → Br	Bd decrements past 0	Exchange RAM with A and Decrement Bd, Exclusive-OR br with r
XIS	r	_4	0 0 | r | 0 1 0 0	RAM(B) ↔ A Bd + 1 → Bd Br ⊕ r → Br	Bd increments past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	0 1 0 1 | 0 0 0 0	A → Bd	None	Copy A to Bd
CBA		4E	0 1 0 0 | 1 1 1 0	BD → A	None	Copy Bd to A
LBI	r, d	--	0 0 | r | (d	r,d → B	Skip until not a LBI	Load B Immediate with r, d (Note 6)
			(d = 0, 9:15)			
			or			
		33	0 0 1 1 | 0 0 1 1			
		--	1 0 | r | d			
			(any d)			
LEI	y	33	0 0 1 1 | 0 0 1 1	y → EN	None	Load EN Immediate (Note 7)
		6_	0 1 1 0 | y			
XABR		12	0 0 0 1 | 0 0 1 0	A ↔ Br(0, 0 → A_3, A_2)	None	Exchange A with Br
TEST INSTRUCTIONS						
SKC		20	0 0 1 0 | 0 0 0 0		C = "1"	Skip if C is True
SKE		21	0 0 1 0 | 0 0 0 1		A = (RAM(B)	Skip if A Equals RAM
SKGZ		33	0 0 1 1 | 0 0 1 1		$G_{3:0}$ =0	Skip if G is Zero (all 4 bits)
		21	0 0 1 0 | 0 0 0 1			
SKGBZ		33	0 0 1 1 | 0 0 1 1	1st byte		Skip if G Bit is Zero
	0	01	0 0 0 0 | 0 0 0 1	2nd byte	G_0 = 0	
	1	11	0 0 0 1 | 0 0 0 1	2nd byte	G_1 = 0	
	2	03	0 0 0 0 | 0 0 1 1	2nd byte	G_2 = 0	
	3	13	0 0 0 1 | 0 0 1 1	2nd byte	G_3 = 0	
SKMBZ	0	01	0 0 0 0 | 0 0 0 1		$RAM(B)_0$ = 0	Skip if RAM Bit is Zero
	1	11	0 0 0 1 | 0 0 0 1		$RAM(B)_1$ = 0	
	2	03	0 0 0 0 | 0 0 1 1		$RAM(B)_2$ = 0	
	3	13	0 0 0 1 | 0 0 1 1		$RAM(B)_3$ =0	
SKT		41	0 1 0 0 | 0 0 0 1		A time-base counter carry has occurred since last test	Skip on Timer (Note 3)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
INPUT/OUTPUT INSTRUCTIONS						
ING		33	0 0 1 1 0 0 1 1	G → A	None	Input G ports to A
		2A	0 0 1 0 1 0 1 0			
ININ		33	0 0 1 1 0 0 1 1	IN → A	None	Input IN inputs to A
		28	0 0 1 0 1 0 0 0			(Note 2)
INIL		33	0 0 1 1 0 0 1 1	IL_3, CKO, "0", IL_0 → A	None	Input IL Latches to A (Notes 2 and 3)
		29	0 0 1 0 1 0 0 1			
INL		33	0 0 1 1 0 0 1 1	$L_{7:4}$ → RAM(B)	None	Input L Ports to RAM, A
		2E	0 0 1 0 1 1 1 0	$L_{3:0}$ → A		
OBD		33	0 0 1 1 0 0 1 1	Bd → D	None	Output Bd to D Outputs
		3E	0 0 1 1 1 1 1 0			
OGI	y	33	0 0 1 1 0 0 1 1	y → G	None	Output to G Ports Immediate
		5-	0 1 0 1 y			
OMG		33	0 1 1 0 0 1 1 1	RAM(B) → G	None	Output RAM to G Ports
		3A	0 0 1 1 1 0 1 0			
XAS		4F	0 1 0 0 1 1 1 1	A ↔ SIO, C → SK	None	Exchange A with SIO (Note 3)

Note 1: All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register.

Note 2: The ININ and INIL instructions are not available on the 24-pin WD4210 since this device does not contain the IN inputs.

Note 3: For additional information on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.

Note 4: The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of page 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 5: A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Note 6: LBI is a single-byte instruction if d = 0, 9, 10, 11, 12, 13, 14, or 15. The machine code for the lower 4 bits equals the binary view of the "d" data *minus 1*, e.g., to load the lower four bits of B (Bd) with the value 9 (1001_2), the lower 4 bits of the LBI instruction equal B (1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 5 (1111_2).

Note 7: Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection of deselection of a particular function associated with each bit (see Functional Description, EN Register).

The following information is provided to assist the user in understanding the operation of several unique instructions and to provide notes useful to programmers in writing WD4200/4210 programs.

XAS Instruction

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. An XAS instruction will also affect the SK output, providing a logic controlled clock if SIO is selected as a shift register or C → SK if SIO is selected as a binary counter. (See Functional Description, EN Register, above). If SIO is selected as a shift register, an XAS instruction must be performed once every 4 instruction cycles to effect a continuous data system.

JID Instruction

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the *contents* of ROM addressed by the 10-bit word, $PC_{9:8}$, A, M. PC_9 and PC_8 are not affected by this instruction.

Note that JID requires two instruction cycles.

INIL Instruction

INIL (Input IL Latches to A) inputs two latches, IL_3 and IL_0 (see figure 8) and CKO into A. The IL_3 and IL_0 latches are set if a low-going pulse ("1" to "0") has occurred on the IN_3 and IN_0 inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction times. Execution of an INIL inputs IL3 and IL0 into A3 and A0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the IN3 and IN0 lines. If CKO is mask programmed as a general purpose input, an INIL will input the state of CKO into A_2. If CKO has not been so programmed, a "1" will be placed in A_2. A "0" is always placed in A_1 upon the execution of an INIL. The general purpose inputs IN_3—IN_0 are input to A upon the execution of an ININ instruction (see table 2, ININ Instruction). INIL is useful in recognizing pulses of short duration or pulses which occur too often to be read conveniently by an ININ instruction.

LQID Instruction

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 10-bit word PC_9, PC_8, A, M. LQID can be used for table look-up or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC + 1 → SA → SB → SC) and replaces the least significant 8 bits of PC as follows: A → $PC_{7:4}$, RAM(B) → $PC_{3:0}$, leaving PC_9 and PC_8 unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SC → SB → SA → PC), restoring the saved value of PC to continue sequential program execution. Since LQID pushes SB → SC, the previous contents of SC are lost. Also, when LQID pops the stack, the previously pushed contents of SB are left in SC. The net result is that the contents of SB are placed in SC (SB → SC). Note that LQID takes two instruction cycle times to execute.

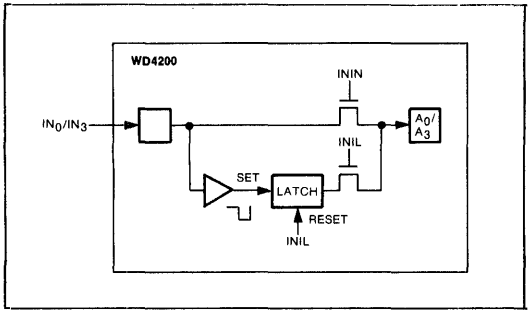


Figure 9 INIL HARDWARE IMPLEMENTATION

SKT Instruction

The SKT (Skip on Timer) instruction tests the state of an internal 10-bit time-base counter. This counter divides the instruction cycle clock frequency by 1024 and provides a latched indication of counter overflow. The SKT instruction tests this latch, executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction, therefore, allow the WD4200/4210 to generate its own time-base for real-time processing rather than relying on an external input signal.

For example, using a 2.097 MHz crystal as the time-base to the clock generator, the instruction cycle clock frequency will be 131 kHz (crystal frequency ÷ 16) and the binary counter output pulse frequency will be 128 Hz. For time-of-day or similar real-time processing, the SKT instruction can call a routine which increments a "seconds" counter every 128 ticks.

Instruction Set Notes

a. The first word of a WD4200/4210 program (ROM address 0) must be a CLRA (Clear A) instruction.

b. Although skipped instructions are not executed, one instruction cycle time is devoted to skipping each byte of the skipped instruction. Thus all program paths take the same number of cycle times whether instructions are skipped or executed.

c. The ROM is organized into 16 pages of 64 words each. The Program Counter is a 10-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID, or LQID instruction is located in the last word of a page, the instruction operates as if it were in the next page. For example: a JP location in the last word of a page will jump to a location in the next page. Also, a LQID or JID located in the last word of pages 2, 7, 11, or 15 will access data in the next group of four pages.

OPTION LIST

The WD4200/4210 mask-programmable options are assigned numbers which correspond with the WD4200 pins.

TABLE 3 is a list of WD4200 options. When specifying a WD4210 chip, Options 9, 10, 19, 20, and 29 must all be set to zero. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

TABLE 3 WD4200 MASK OPTIONS

Option 1 = 0: Ground Pin — no options available

Option 2: CKO Pin
- = 0: clock generator output to crystal
- = 1: pin is RAM power supply (V_R input)
- = 2: general purpose input, load device to V_{CC}
- = 3: multi-COP SYNC input
- = 4: general purpose input, Hi-Z input

Option 3: CKI Input
- = 0: crystal input divided by 16
- = 1: crystal input divided by 8
- = 2: TTL external clock input divided by 16
- = 3: TTL external clock input divided by 8
- = 4: single-pin RC controlled oscillator

Option 4: $\overline{\text{RESET}}$ Pin
- = 0: load devices to V_{CC}
- = 1: Hi-Z input

Option 5: L_7 Driver
- = 0: Standard output (Figure 6A)
- = 1: Open-Drain output (Figure 6B)
- = 2: LED direct drive output (Figure 6D)
- = 3: TRI-STATE®push-pull output (Figure 6E)

Option 6: L_6 Driver
Same as Option 5

Option 7: L_5 Driver
Same as Option 5

Option 8: L_4 Driver
Same as Option 5

Option 9: IN_1 Input
- = 0: load device to V_{CC} (Figure 6F)
- = 1: Hi-Z input

Option 10: IN_2 Input
Same as Option 9

Option 11 = 0: V_{CC} Pin — no options available

Option 12: L_3 Driver
Same as Option 5

Option 13: L_2 Driver
Same as Option 5

Option 14: L_1 Driver
Same as Option 5

Option 15: L_0 Driver
Same as Option 5

Option 16: SI Input
Same as Option 9

Option 17: SO Driver
- = 0: Standard output (Figure 6A)
- = 1: Open-Drain output (Figure 6B)
- = 2: Push-Pull output (Figure 6C)

Option 18: SK Driver
Same as Option 17

Option 19: IN_0 Input
Same as Option 9

Option 20: IN_3 Input
Same as Option 9

Option 21: G_0 I/O Port
- = 0: Standard output (A)
- = 1: Open-Drain output (B)

Option 22: G_1 I/O Port
Same as Option 21

Option 23: G_2 I/O Port
Same as Option 21

Option 24: G_3 I/O Port
Same as Option 21

Option 25: D_3 Output
- = 0: Standard output (A)
- = 1: Open-Drain output (B)

Option 26: D_2 Output
Same as Option 25

Option 27: D_1 Output
Same as Option 25

Option 28: D_0 Output
Same as Option 25

Option 29: COP Function
- = 0: normal operation
- = 1: MICROBUS™ option

Option 30: COP Bonding
- = 0: WD4200 (28-pin device)
- = 1: WD4210 (24-pin device)

TEST MODE (Non-Standard Operation)

The SO output has been configured to provide for standard test procedures for the custom-programmed WD4200. With SO forced to logic "1", two test modes are provided, depending upon the value of SI:

a. RAM and Internal Logic Test Mode (SI = 1)

b. ROM Test Mode (SI = 0)

These special test modes should not be employed by the user; they are intended for manufacturing test only.

APPLICATION NO. 1: WD4200 General Controller

The diagram below shows an interconnect diagram for a WD4200 used as a general controller. Operation of the system is as follows:

1. The L_7-L_0 outputs are configured as LED Direct Drive outputs, allowing direct connection to the segments of the display.
2. The D_3-D_0 outputs are buffered by transistors to drive the digits of the multiplexed display and to scan the columns of the 4x4 keyboard matrix rows.
3. The IN_3-IN_0 inputs are used to input the four drives of the keyboard matrix. Reading the IN lines in conjunction with the current value of the D outputs allows detection, debouncing, and decoding of any one of the 16 keyswitches.
4. CKI is configured as a single-pin oscillator input allowing system timing to be controlled by a single pin RC network. CKO is therefore available for use as a VR RAM power supply pin. RAM data integrity is thereby assured when the main power supply is shut down.
5. SI is selected as the input to a binary counter input. With SIO used as a binary counter, SO and SK may be used as general purpose outputs.
6. The four bidirectional G I/O ports (G_3-G_0) are available for use as required by the user's application.

APPLICATION NO. 2

Provides an interconnect diagram for a versatile application of the WD4200 as a keyboard/display interface to a microprocessor (μP). Generally, operation of the WD4200 in this configuration is as follows:

1. The MICROBUS™ option has been selected.
2. System timing is provided by an external crystal. The time base for the real-time (counter and clock) modes is provided by the internal time-base counter, tested by the SKT instruction.
3. The SIO register is used as a serial-in/serial-out shift register. In this configuration, however, SI is shifted into SIO to be tested as one of the four row lines tied to the keyboard matrix. SO is used to output display segment data (loaded into SIO with an XAS instruction) to the cascaded 74C164s (8-bit parallel out serial shift registers). SK functions as a logic-controlled clock, sending a SYNC signal to clock serial data into the 74C164s.
4. The 16 bits of data shifted into the 74C164s are buffered through the DS8867s (8-segment LED drivers) to the 16 segments of the alpha-numeric LED displays.
5. The D_0-D_1 outputs are decoded by the DS8664 (14-digit decoder/driver) and used to select one of the 14 digits of the multiplexed display as well as to scan the 13 columns of the keyboard matrix and the strap switch scan line (D14).

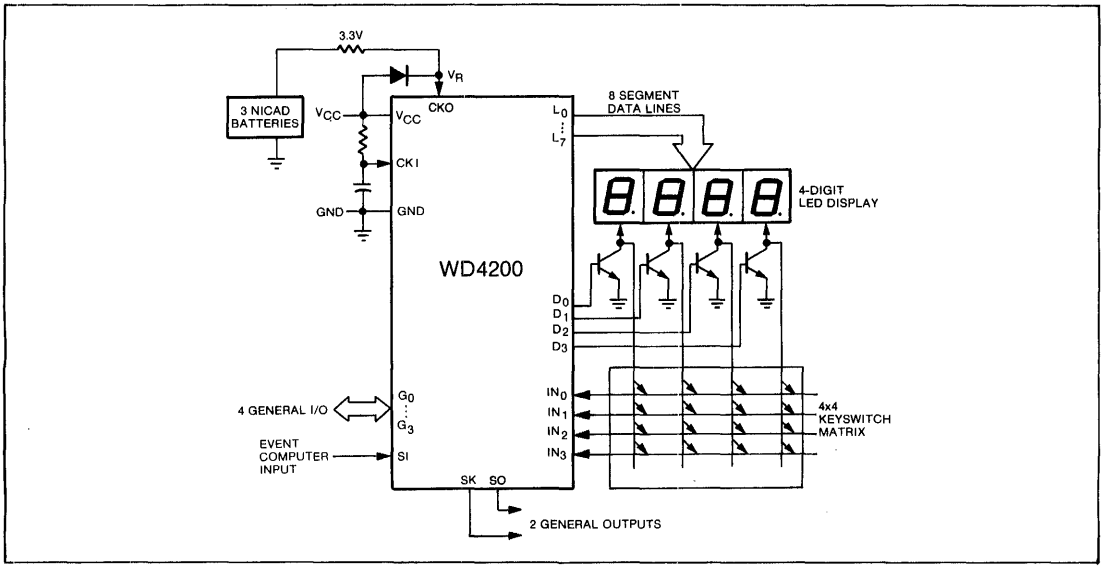


Figure 10 WD4200 KEYBOARD/DISPLAY INTERFACE

6. The G_1-G lines together with SI are connected to the four rows of the keyboard matrix and the four strap switch lines to input key or strap switch data to the WD4200. The strap switches can be used to select one of several of the system modes listed below.
7. The L_0L_7 THREE-STATE bidirectional I/O ports are connected to the microprocessor data bus to allow for input or output of data to and from the microprocessor and the WD4200.
8. The various operations which can be performed by the system include the following "handshaking" and WD4200 "stand-alone" modes:
   a. keyboard to μP (7-bit ASCII)
   b. keyboard to WD4200 buffer to μP (7-bit ASCII)
   c. μP to display
   d. display to μP
   e. μP to clock
   f. clock to μP
   g. μP to timer
   h. timer to μP
   i. keyboard to display
   j. clock to display
   k. timer to display

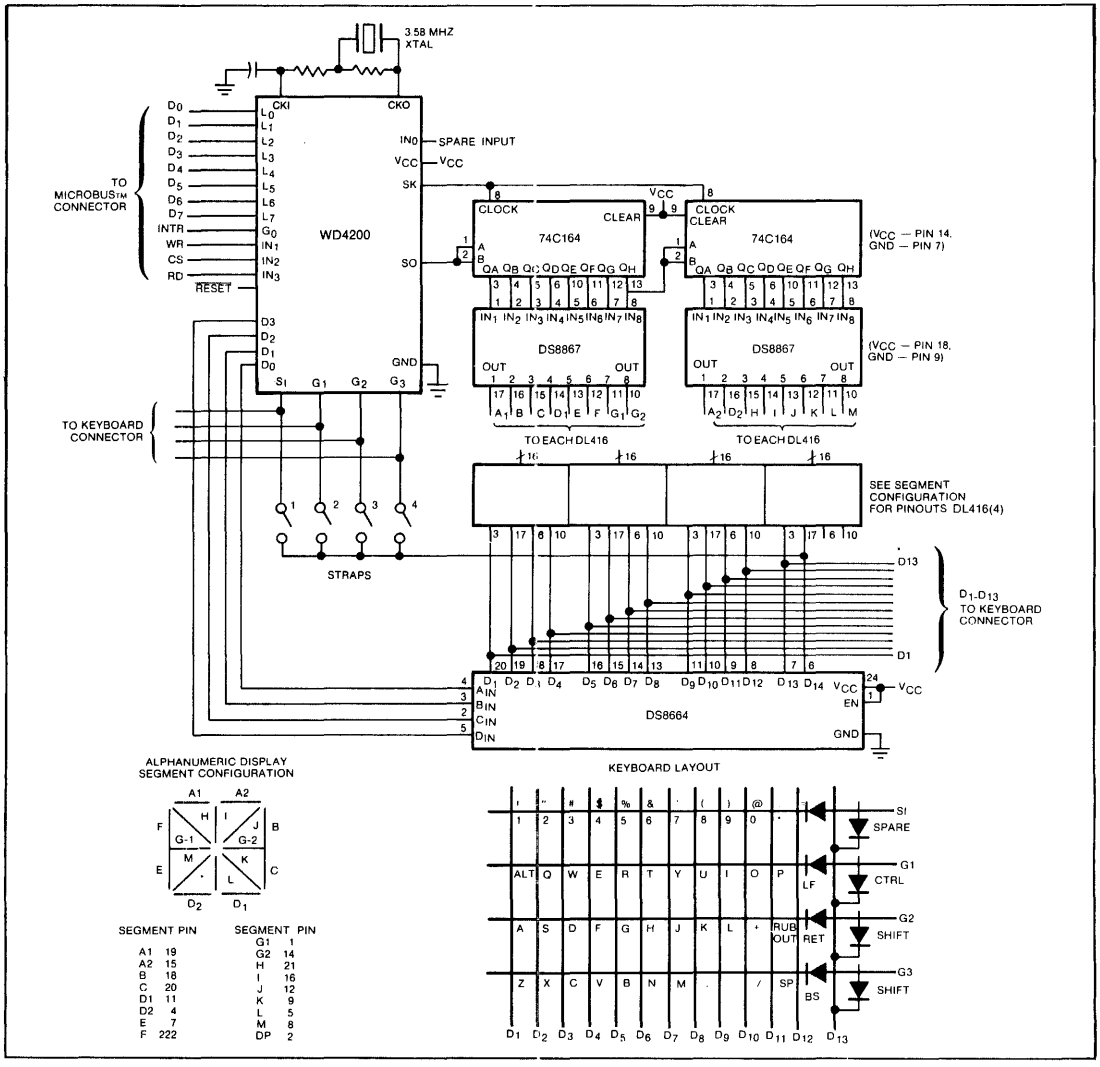


Figure 11 WD4200 KEYBOARD/DISPLAY INTERFACE

WD4200/4210
ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin Relative to GND −0.5V to +7V
Ambient Operating Temperature (Note 1)
0°C to +70°C
Ambient Storage Temperature
−65°C to +150°C
Ceramic Plastic −55°C to +125°C
Lead Temperature (Soldering, 10 sec.) 300°C
Power Dissipation 0.75 Watt at 25°C
0.4 Watt at 70°C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS

0°C≤TA≤+70°C, 4.5V≤VCC≤6.3V unless otherwise noted.

TABLE 4

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Operating Voltage (V_{CC})		4.5	6.3	V
Operating Supply Current	V_{CC} = 5V, T_A = 25°C (all inputs and outputs open)		35	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input				
Logic High (V_{IH})		2.0		V
Logic Low (V_{IL})			0.4	V
TTL Input	V_{CC} = 5V ± 5%			
Logic High (V_{IH})		2.0		V
Logic Low (V_{IL})			0.8	V
Schmitt Trigger Input				
Logic High (V_{IH})		0.7 V_{CC}		V
Logic Low (V_{IL})			0.6	V
$\overline{RESET}$ Input Levels				
Logic High		0.7 V_{CC}		V
Logic Low			0.6	V
$\overline{RESET}$ Hysteresis		1.0		V
SO Input Level (Test Mode)		2.0	3.0	V
All Other Inputs				
Logic High	V_{CC} = Max	3.0		V
Logic High	V_{CC} = 5V ± 5%	2.0		V
Logic Low			0.8	V
Output Voltage Levels				
Standard Output				
TTL Operation	V_{CC} = 5V ± 5%			
Logic High (V_{OH})	I_{OH} = 100 μA)	2.4		V
Logic Low (V_{OL})	I_{OL} = -1.6 mA		0.4	V
CMOS Operation				
Logic High (V_{OH})	I_{OH} = 10μA	V_{CC}-1		V
Logic Low (V_{OL})	I_{OL} = -10μA		0.2	V
Output Current Levels				
LED Direct Drive Output	V_{CC} = 6V			
Logic High (I_{OH})	V_{OH} = 2.0V	2.5	14	mA
TRI-STATE® Output Leakage Current		-10	+10	μA
CKO Output				
VR Power Saving Option	V_R = 3.3V			
Power Requirements			3	mA

WD4200/4210

AC Electrical Characteristics

$0°C \leq TA \leq +70°C$, $4.5V \leq V_{CC} \leq 6.3V$ unless otherwise stated.

TABLE 5

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Instruction Cycle Time — t_C	figure 13a	4	10	μs
CKI Using Crystal (figure 5A)				
Input Frequency — f_1	÷16 mode	1.6	4	MHz
	÷ 8 mode	0.8	2	MHz
Duty Cycle (Note 2)	figure 13b	30	55	%
CKI Using External Clock (figure 5B)				
Input Frequency	÷16 mode	1.6	4	MHz
	÷ 8 mode	0.8	2	MHz
Duty Cycle (Note 2)		30	60	%
Rise Time	f_1 = 4 MHz		60	ns
Fall Time	f_1 = 4 MHz		40	ns
CKI Using RC (figure 5C)				
Frequency	R = 15K ± 5%, C = 100 pF ± 10%	0.5	1.0	MHz
Instruction Cycle Time		4	8	μs
CKO as SYNC Input (figure 5D)				
t_{SYNO}	figure 13b	50		ns
Inputs (figure 13a):				
IN_3-IN_0, G_3-G_0, L_7-L_0				
t_{SETUP}		1.7		μs
t_{HOLD}		100		ns
SI				
t_{SETUP}		0.3		μs
t_{HOLD}		100		ns
Outputs:				
COP to CMOS Propagation Delay	$4.5V \leq V_{CC} \leq 6.3V$, C_L = 50 pF, $V_{OH} = 0.7\ V_{CC}$, $V_{OL} = 0.3\ V_{CC}$			
SK as a Logic-Controlled Clock				
t_{PD1}			1.1	μs
t_{PD0}			0.3	μs
S0, SK as a Data Output				
t_{PD1}			1.4	μs
t_{PD0}			0.3	μs
t_{PD1}	V_{OH} = 2V		0.7	μs
D_3-D_0, G_3-G_0				
t_{PD1}			1.6	μs
t_{PD0}			0.6	μs
L_7-L_0 (Standard)				
t_{PD1}			1.4	μs
t_{PD0}			0.3	μs
L_7-L_0 (LED Direct Drive)				
t_{PD1}	V_{OH} = 2V		2.4	μs
t_{PD0}			0.4	μs
COP to TTL Propagation Delay	fanout = 1 Standard TTL Load, V_{CC} = 5V ± 5%, C_L = 50 pF, V_{OH} = 2.4V, V_{OL} = 0.4V			
SK as a Logic-Controlled Clock				
t_{PD1}			0.8	μs
t_{PD0}			0.8	μs

TABLE 5 Continued

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Outputs (continued):				
SK as a Data Output, SO				
t_{PD1}			1.0	μs
t_{PD0}			1.0	μs
D_3-D_0, G_3-G_0				
t_{PD1}			1.3	μs
t_{PD0}			1.3	μs
L_7-L_0				
t_{PD1}			1.4	μs
t_{PD0}			0.4	μs
L_7-L_0 (Push-Pull)				
t_{PD1}			0.4	μs
t_{PD0}			0.3	μs
CKO (figure 13C)				
t_{PD1}			0.2	μs
t_{PD0}			0.2	μs
MICROBUS™ Timing	CL = 50 pF, V_{CC} = 5V ± 5%			
Read Operation (figure 11)				
Chip Select Stable Before $\overline{RD}$ - t_{CSR}		50		ns
Chip Select Hold Time for $\overline{RD}$ - t_{RCS}		5		ns
$\overline{RD}$ Pulse Width - t_{RR}		300		ns
Data Delay from $\overline{RD}$ - $t_{\overline{RD}}$			250	ns
$\overline{RD}$ to Data Floating - t_{DF}			200	ns
Write Operation (figure 12)				
Chip Select Stable Before $\overline{WR}$ - t_{CSW}		20		ns
Chip Select Hold Time for $\overline{WR}$ - t_{WCS}		20		ns
$\overline{WR}$ Pulse Width — t_{WW}		300		ns
Data Set-Up Time for $\overline{WR}$ - t_{DW}		200		ns
Data Hold Time for $\overline{WR}$ - t_{WD}		40		ns
INTR Transition Time from $\overline{WR}$ - t_{WI}			700	ns

Note 1: Duty Cycle = $t_{W1}/(t_{W1} + t_{W0})$.
Note 2: See figure 7 for additional I/O characteristics.

WD4320/43421

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin Relative to GND −0.5V to +7V
Ambient Operating Temperature (Note 1)
−40°C to +85°C
Ambient Storage Temperature
Ceramic −65°C to +150°C
Plastic −55°C to +125°C
Lead Temperature (Soldering, 10 sec.) 300°C
Power Dissipation 0.75 Watt at 25°C
0.25 Watt at 85°C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS

$-40°C \leq TA \leq +85°C$, $4.5V \leq V_{CC} \leq 5.5V$ unless otherwise noted.

TABLE 6

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Operating Voltage (V_{CC})		4.5	5.5	V
Operating Supply Current	(all inputs and outputs open)		40	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input				
Logic High (V_{IH})		2.2		V
Logic Low (V_{IL})			0.3	V
TTL Input	V_{CC} = 5V ± 5%			
Logic High (V_{IH})		2.2		V
Logic Low (V_{IL})			0.6	V
Schmitt Trigger Input				
Logic High (V_{IH})		0.7 V_{CC}		V
Logic Low (V_{IL})			0.4	V
$\overline{\text{RESET}}$ Input Levels				
Logic High		0.7 V_{CC}		V
Logic Low			0.1	V
$\overline{\text{RESET}}$ Hysteresis		0.5		V
SO Input Level (Test Mode)		2.2	3.0	V
All Other Inputs				
Logic High	V_{CC} = Max	3.0		V
Logic High	V_{CC} = 5V ± 5%	2.2		V
Logic Low			0.6	V
Output Voltage Levels				
Standard Output				
TTL Operation	V_{CC} = 5V ± 5%			
Logic High (V_{OH})	I_{OH} = −75μA	2.4		V
Logic Low (V_{OL})	I_{OL} = −1.6 mA		0.4	V
CMOS Operation				
Logic High (V_{OH})	I_{OH} = 10μA	V_{CC}−1		V
Logic Low (V_{OL})	I_{OL} = −10μA		0.2	V
Output Current Levels				
LED Direct Drive Output	V_{CC} = 5V			
Logic High (I_{OH})	V_{OH} = 2.0V	1.0	12	mA
THREE-STATE Output Leakage Current		−10	+10	μA
CKO Output				
VR Power Saving Option	V_R = 3.3V			
Power Requirements			4	mA

WD4320/4321

AC Electrical Characteristics

$40°C \leq TA \leq +85°C$, $4.5V \leq V_{CC} \leq 5.5V$ unless otherwise stated.

TABLE 7

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Instruction Cycle Time — ^tC	figure 13a	4	10	μs
CKI Using Crystal (figure 5A)				
Input Frequency — f_1	÷16 mode	1.6	4	MHz
	÷ 8 mode	0.8	2	MHz
Duty Cycle (Note 2)	figure 13b	40	55	%
CKI Using External Clock (figure 5B)				
Input Frequency	÷16 mode	1.6	4	MHz
	÷ 8 mode	0.8	2	MHz
Duty Cycle (Note 2)		40	60	%
Rise Time	f_1 = 4 MHz		60	ns
Fall Time	f_1 = 4 MHz		40	ns
CKI Using RC (figure 5C)				
Frequency	R = 15K ± 5%, C = 100 pF ± 10%	0.5	1.0	MHz
Instruction Cycle Time		4	8	μs
CKO as SYNC Input (figure 5D)				
$^tSYN0$	figure 13b	50		ns
Inputs (figure 13a):				
IN_3-IN_0, G_3-G_0, L_7-L_0				
^tSETUP		1.7		μs
^tHOLD		100		ns
SI				
^tSETUP		0.3		μs
^tHOLD		250		ns
Outputs:				
COP to CMOS Propagation Delay	$4.5V \leq V_{CC} \leq 5.5V$, C_L = 50pF, $V_{OH} = 0.7\ V_{CC}$, $V_{OL} = 0.3\ V_{CC}$			
SK as a Logic-Controlled Clock				
$^tPD1$			1.3	μs
$^tPD0$			0.4	μs
S0, SK as a Data Output				
$^tPD1$			1.6	μs
$^tPD0$			0.4	μs
$^tPD1$	V_{OH} = 2V		.75	μs
D_3-D_0, G_3-G_0				
$^tPD1$			2.0	μs
$^tPD0$			1.0	μs
L_7-L_0 (Standard)				
$^tPD1$			2.0	μs
$^tPD0$			1.0	μs
L_7-L_0 (LED Direct Drive)				
$^tPD1$	V_{OH} = 2V		3.0	μs
$^tPD0$			1.0	μs
COP to TTL Propagation Delay	fanout = 1 Standard TTL Load V_{CC} = 5V ± 5%, C_L = 50 pF, V_{OH} = 2.4V, V_{OL} = 0.4V			
SK as a Logic-Controlled Clock				
$^tPD1$			1.0	μs
$^tPD0$			1.0	μs

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Outputs (continued):				
SK as a Data Output, SO				
t_{PD1}			1.2	μs
t_{PD0}			1.2	μs
D_3-D_0, G_3-G_0				
t_{PD1}			1.5	μs
t_{PD0}			1.5	μs
L_7-L_0				
t_{PD1}			1.6	μs
t_{PD0}			0.5	μs
L_7-L_0 (Push-Pull)				
t_{PD1}			0.5	μs
t_{PD0}			0.5	μs
CKO (figure 13C)				
t_{PD1}			0.25	μs
t_{PD0}			0.25	μs
MICROBUS™ Timing	CL = 50 pF, V_{CC} = 5V ± 5%			
Read Operation (figure 11)				
Chip Select Stable Before $\overline{RD}$ - t_{CSR}		60		ns
Chip Select Hold Time for $\overline{RD}$ - t_{RCS}		10		ns
$\overline{RD}$ Pulse Width - t_{RR}		400		ns
Data Delay from $\overline{RD}$ - $t_{\overline{RD}}$			350	ns
$\overline{RD}$ to Data Floating - t_{DF}			250	ns
Write Operation (figure 12)				
Chip Select Stable Before $\overline{WR}$ - t_{CSW}		100		ns
Chip Select Hold Time for $\overline{WR}$ - t_{WCS}		50		ns
$\overline{WR}$ Pulse Width — t_{WW}		400		ns
Data Set-Up Time for $\overline{WR}$ - t_{DW}		350		ns
Data Hold Time for $\overline{WR}$ - t_{WD}		50		ns
INTR Transition Time from $\overline{WR}$ - t_{WI}			800	ns

Note 1: Exercise great care not to exceed maximum power dissipation limits when direct driving LEDs or similar loads at high temperatures.
Note 2: Duty Cycle = $t_{W1}/(t_{W1} + t_{W0})$.
Note 3: See figure 8 for additional I/O characteristics.

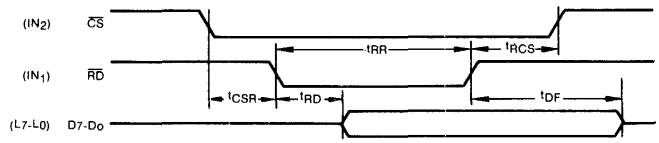


Figure 12 MICROBUS™ READ OPERATION TIMING

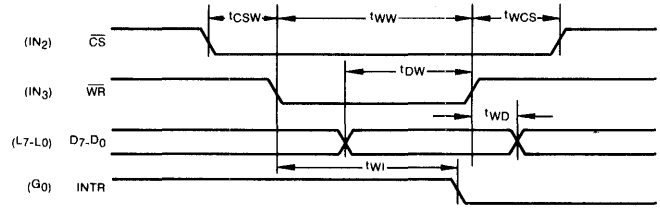


Figure 13 MICROBUS™ WRITE OPERATION TIMING

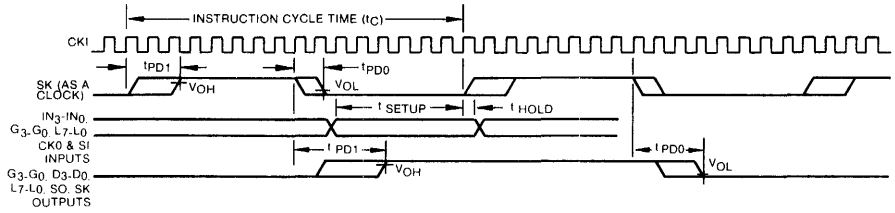


Figure 14A **INPUT/OUTPUT TIMING DIAGRAM (CRYSTAL + 16 MODE)**

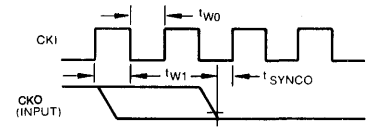


Figure 14B **SYNCHRONIZATION**

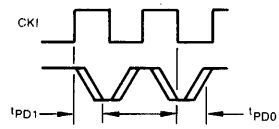


Figure 14C **CKO OUTPUT TIMING**

Figure 14 TIMING

See page 725 for ordering information.

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4 Bit Microcomputers

Western Digital Components Group offers both PMOS and NMOS single chip microcomputers for dedicated controller applications. Both of these families are true microcomputers in that they have on-chip mask ROM, RAM, I/O, and clock generation — all of the elements required to implement a programmable microcontroller solution for your dedicated control problem.

PREPROGRAMMED MICROCONTROLLERS

Western Digital offers several preprogrammed microcontrollers which were developed to solve timing and control problems which previously had been implemented by electromechanical systems consisting of motors, cam switches, levers, etc. or for which a large number of random-logic IC's were required. Several more devices are being developed; for customized versions of these standard products, please contact the factory.

WD-51 IRRIGATION CONTROLLER

The WD-51 performs all of the timing and control functions required by a 6-station irrigation (sprinkler) control system for residential and commercial applications.

The only support circuitry required is a simple power supply, display, keyboard/switch matrix, and triac or other high-current solenoid driver. The device is fully programmable for a 7-day week and each station output is programmable from 0 to 99 minutes duration. Up to 3 complete watering cycles per 24 hour period are available, as well as a pump/master valve output and a rain-inhibit switch input.

WD-55 TIMER/CONTROLLER

The WD-55 is a general purpose timing element for use as a dark room timer, process sequencer, appliance timer, time-delay relay, recycling timer, etc. It may be configured for two different modes of operation: one mode utilizes a conventional matrix keyboard for data entry, in conjunction with a 4-digit LED or V-F display for generating up to seven timed sequential outputs. Another mode allows data entry through BCD-encoded switches for triggered or continuous control of 2 outputs.

WD4200/4210

These devices are fabricated using N-channel technology, and are hardware and software compatible with National Semiconductor's COP 420/421 devices. The WD4200 is available in a 28-pin package and features 23 I/O lines. The WD4210 is a bonding option which deletes the 4-bit IN-port and is available in a 24-pin package. They both feature 1K x 8 ROM, 64 x 4 RAM, a 4.0μs instruction cycle time, 4.5 to 6.3V operation, a 3-level subroutine stack, single-level interrupt, serial I/O plus sync, on-chip counter/timer, and a high current 8-bit bidirectional port capable of directly driving LED displays.

WD4320/4321

These devices are functionally identical to the WD4200/4210, but operate over an extended temperature range of $-40°C$ to $+85°C$.

SUBMISSION OF MASK ROM CODE

To submit mask ROM code for the WD4200/4210, or WD4320/4321 two items need to be received:

(1) Completed I/O options list describing the desired configured of the mask-programmable options.

(2) The object code itself.

The object code may be in the form of a diskette containing the XXX.TRT and XXX.LM files generated by a COP400 PDS development system, or EPROMS (5204, 2708, 2716, etc.), paper tape, etc. (we prefer the diskette or EPROMS), and a hard copy printout of the object code. Western Digital will review and duplicate the media submitted and will return copies to the customer.

Upon written confirmation as to the correctness of the data, masks are generated and an engineering pilot run is commenced. At the completion of the pilot run, approximately 10 devices are submitted to the customer for verification and approval. Upon written verification by the customer, the remainder of the pilot run (usually several hundred devices) are shipped as part of a pre-production delivery, and the production wafers are started for predetermined, scheduled delivery.

MASK OPTION CONFIGURATION TABLE FOR WD4200/4210 and WD4320/4321

MASK OPTION	SELECTED* OPTION	COMMENT
1		Ground Pin
2		CKO Pin
3		CKI Input
4		$\overline{\text{RESET}}$ Pin
5		L7 Driver
6		L6 Driver
7		L5 Driver
8		L4 Driver
9		IN_1 Input NA 4210
10		IN_2 Input NA 4210
11		V_{CC} Pin
12		L3 Driver
13		L2 Driver
14		L1 Driver
15		L0 Driver
16		SI Input
17		SO Driver
18		SK Driver

MASK OPTION	SELECTED* OPTION	COMMENT
19		IN_0 Input NA 4210
20		IN_3 Input NA 4210
21		G0 I/O Port
22		G1 I/O Port
23		G2 I/O Port
24		G3 I/O Port
25		D3 Output
26		D2 Output
27		D1 Output
28		D0 Output
29		Function
30		Bonding

Customer: _____

WDC P/N: _____

Customer P/N: _____

*Note: Refer to the data sheet for a description of the available options.

See page 725 for ordering information.

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Special Products

WD1801 Octal Comparator

FEATURES

- +5 VOLT ONLY
- CASCADABLE USING $\overline{E}_{IN}$
- N-MOS SILICON GATE TECHNOLOGY
- 20 PIN PLASTIC OR CERAMIC DIP
- TTL COMPATIBLE
- BUILT IN PULL-UP RESISTORS ON A INPUTS

APPLICATIONS

- ADDRESS COMPARATOR
- BUS COMPARATOR
- STATUS LINE DECODER
- BREAK POINT GENERATOR

GENERAL DESCRIPTION

The WD1801 is an 8 bit wide comparator. It has been designed to minimize the logic required to implement address decoding or break point indications. It is capable of comparing two 8-bit words and is easily expanded by using the external enable input $\overline{E}_{IN}$.

The matching of two 8 bit inputs plus a logic low on $\overline{E}_{IN}$ produces an active low on output $\overline{E}_{OUT}$.

The A bank inputs are implemented with internal pull-up resistors to facilitate programming with inactive devices such as DIP switches

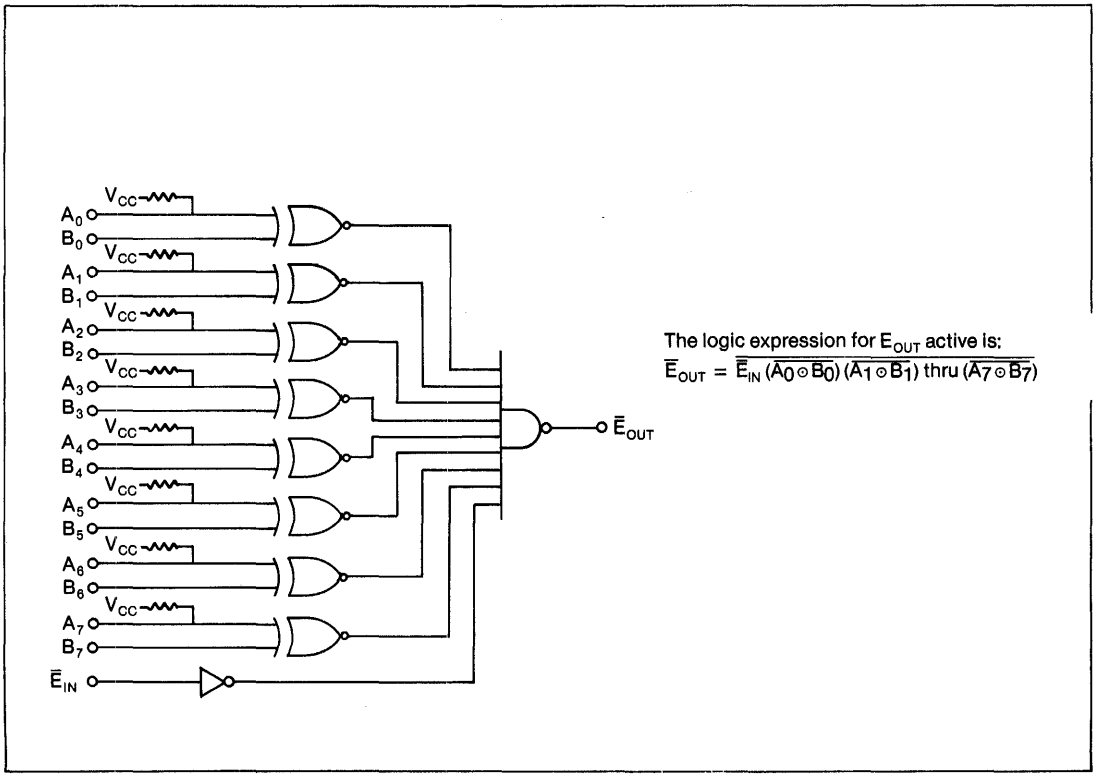


FIGURE 1
LOGIC DIAGRAM

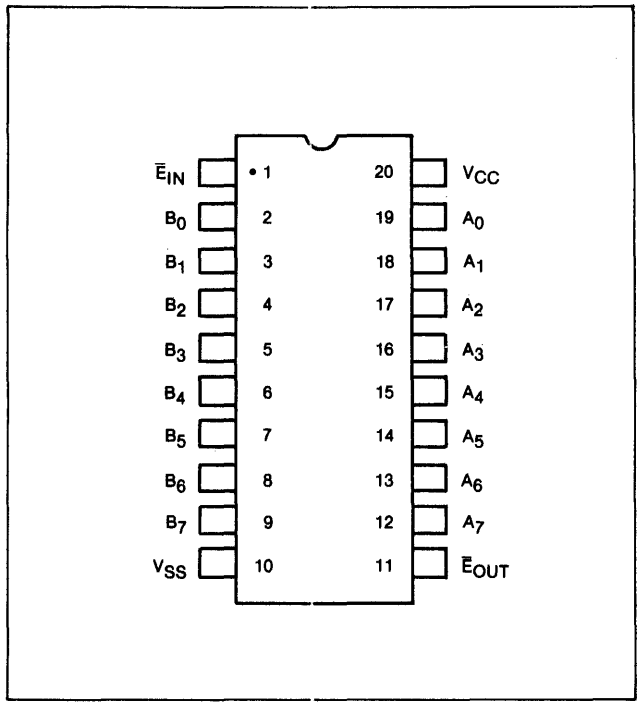


FIGURE 2
PIN CONNECTIONS

PIN DEFINITIONS TABLE I PIN DEFINITIONS

PIN	NAME	SYMBOL	FUNCTION
1	External Enable	$\overline{E}_{IN}$	Active Low Input Enable
2-9	B Inputs	B_0-B_7	8 Bit B Input to Comparator
10	Vss	Vss	Ground
11	Equal Out	$\overline{E}_{OUT}$	Active Low Output for A = B
12-19	A Inputs	A_7-A_0	8 Bit A Input to Comparator
20	Vcc	Vcc	+5V ± 10% Power Supply

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias ..... −40°C to 70°C
Voltage on any pin with respect to Ground (V_{SS}) ..... −0.2 to +7V
Power Dissipation 0.5W
Storage Temp. — Ceramic −65°C to +150°C
Plastic −55°C to +125°C

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

TABLE 2
DC ELECTRICAL CHARACTERISTICS

T_A = 0° to 70°C; V_{CC} = 5.0V ± 10%; V_{SS} = 0V;

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage			+0.8	V	
V_{IH}	Input High Voltage	2.2			V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 3.2MA
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = −200μa
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current		40	100	MA	All outputs open

TABLE 3
DC ELECTRICAL CHARACTERISTICS

T_A = 0° to 70°C; V_{CC} = 5V ± 10%; V_{SS} = 0V; CL = 50pF

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
t_{PHL}	A_i or B_i to $\overline{E}_{OUT}$ Active		55	70	nsec	$\overline{E}_{IN}$ Active
t_{PLH}	A_i or B_i to $\overline{E}_{OUT}$ Inactive		45	60	nsec	$\overline{E}_{IN}$ Active
t_E	$\overline{E}_{IN}$ to $\overline{E}_{OUT}$		40	50	nsec	A_i = B_i

NOTE: A.C. Timing Measurements at V_{OH} = 2.0V and V_{OL} = 0.8V.

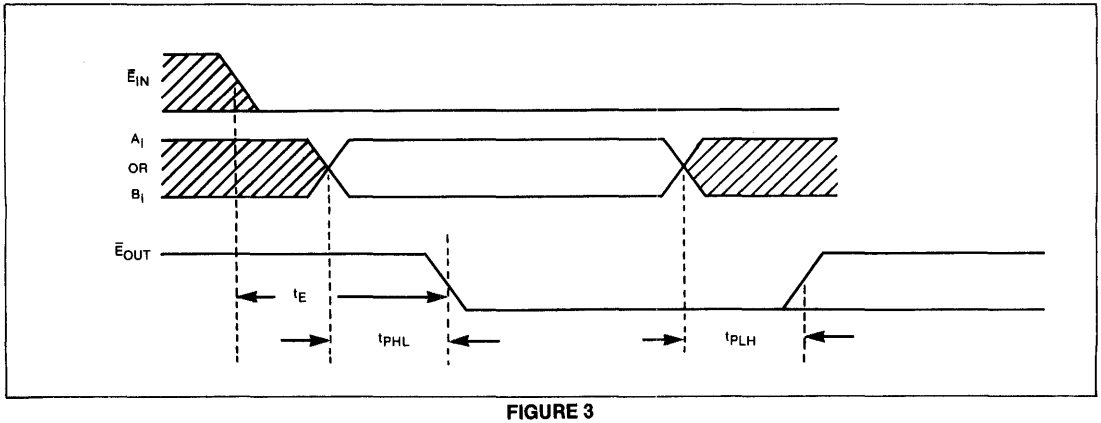


FIGURE 3
TIMING DIAGRAM

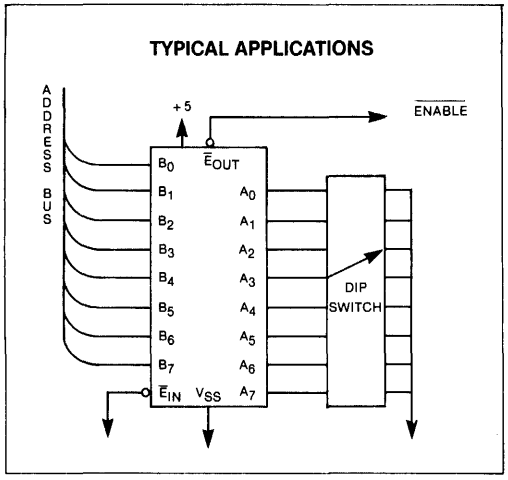


FIGURE 4
8 BIT PROGRAMMABLE ADDRESS BUS COMPARATOR

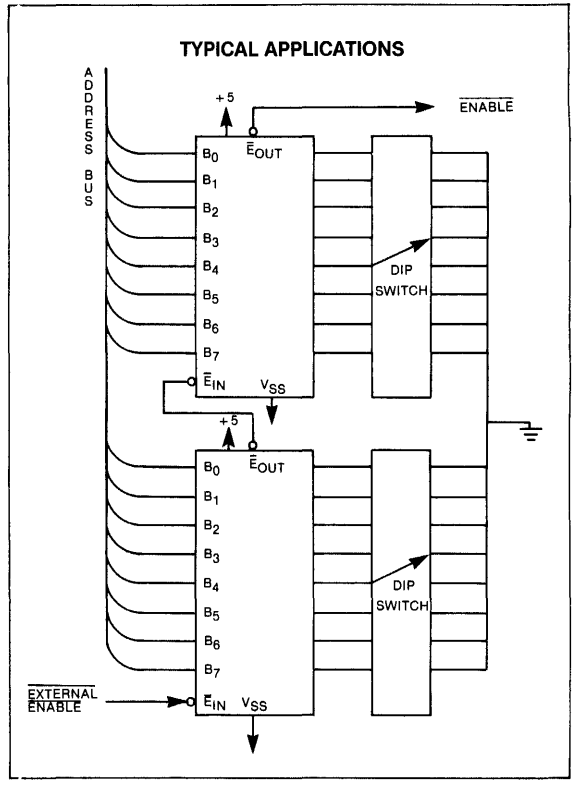


FIGURE 5
16 BIT PROGRAMMABLE ADDRESS BUS COMPARATOR

See page 725 for ordering information.

WD1802 Octal Comparator

FEATURES

- +5 VOLT ONLY
- CASCADABLE USING $\overline{E}_{IN}$
- N-MOS SILICON GATE TECHNOLOGY
- 20 PIN PLASTIC OR CERAMIC DIP
- TTL COMPATIBLE
- BUILT IN PULL-UP RESISTORS ON A INPUTS
- EQUATES FOR COMPLEMENTARY INPUTS

APPLICATIONS

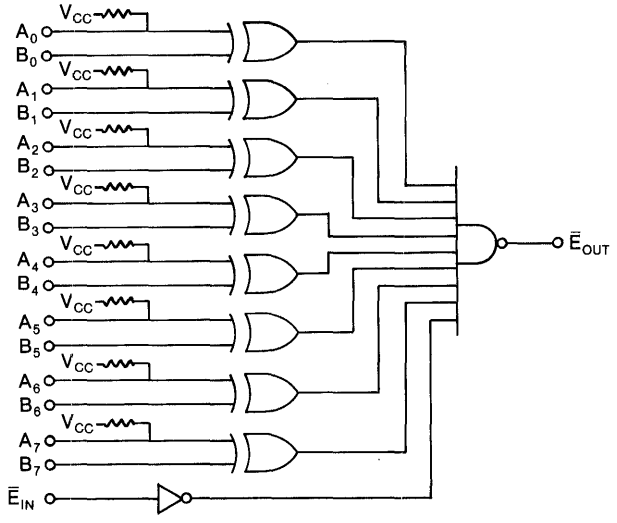
- ADDRESS COMPARATOR
- BREAK POINT GENERATOR
- BUS COMPARATOR
- STATUS LINE DECODER

GENERAL DESCRIPTION

The WD1802 is an 8 bit wide comparator. It has been designed to minimize the logic required to implement address decoding or break point indications. It is capable of comparing two 8-bit words and is easily expandable using the external enable input $\overline{E}_{IN}$.

The WD1802 is implemented with exclusive – OR (XOR) gates. It equates when the A inputs are complementary to the B inputs. The combination of complementary 8 bit inputs plus a logic low on $\overline{E}_{IN}$ produces an active low on the output $\overline{E}_{OUT}$.

The A bank inputs are implemented with internal pull-up resistors. The pull-up resistors plus the complementary logic make this device extremely easy to use with inactive devices such as DIP switches.



The logic expression for $\overline{E}_{OUT}$ active is:

$$\overline{E}_{OUT} = \overline{\overline{E}_{IN}(A_0 \oplus B_0), (A_1 \oplus B_1), (A_2 \oplus B_2), (A_3 \oplus B_3), (A_4 \oplus B_4) (A_5 \oplus B_5), (A_6 \oplus B_6), (A_7 \oplus B_7)}$$

FIGURE 1.
LOGIC DIAGRAM

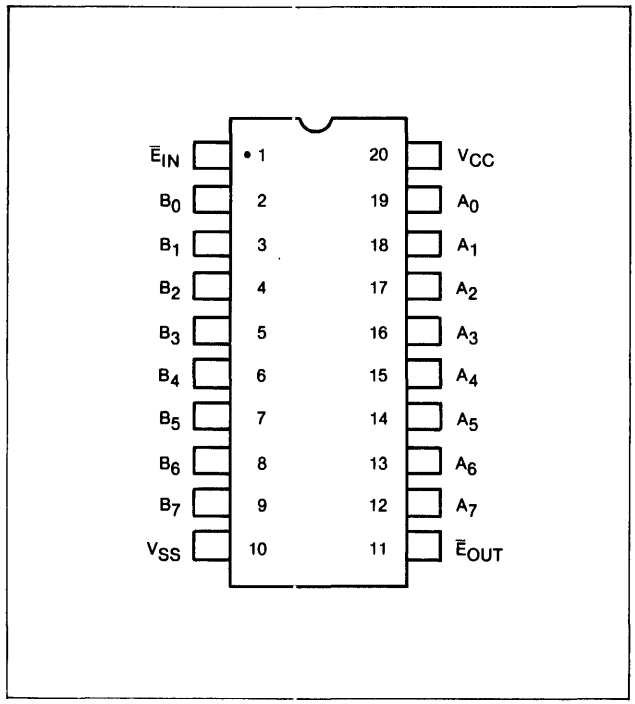


FIGURE 2
PIN CONNECTIONS

PIN DEFINITIONS TABLE I

PIN	NAME	SYMBOL	FUNCTION
1	External Enable	$\overline{E}_{IN}$	Enable Active Low
2-9	B Inputs	B_0-B_7	8 Bit B Input to Comparator
10	V_{SS}	V_{SS}	Ground
11	Equal Out	$\overline{E}_{OUT}$	Active Low Output for A = $\overline{B}$
12-19	A Inputs	A_7-A_0	8 Bit A Input to Comparator
20	V_{CC}	V_{CC}	+5V ± 10% Power Supply

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . . . . – 40°C to 70°C
Voltage on any pin with respect
to Ground (vss). . . . . – 0.2 to + 7V
Power Dissipation. 0.5W
Storage Temp. — Ceramic – 65°C to + 150°C
Plastic – 55°C to + 125°C

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

TABLE 2
DC ELECTRICAL CHARACTERISTICS

T_A = 0° to 70°C; V_{CC} = 5.0V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage			+ 0.8	V	
V_{IH}	Input High Voltage	2.2			V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 3.2MA
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = – 200μa
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current		40	100	MA	All outputs open

TABLE 3
AC ELECTRICAL CHARACTERISTICS

T_A = 0° to 70°C; V_{CC} = 5V ± 10%; V_{SS} = 0V; C_L = 50 pF

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
t_{PHL}	A_i or B_i to $\overline{E}_{OUT}$ Active		55	70	nsec	$\overline{E}_{IN}$ Active
t_{PLH}	A_i or B_i to $\overline{E}_{OUT}$ Inactive		45	60	nsec	$\overline{E}_{IN}$ Active
t_E	$\overline{E}_{IN}$ to $\overline{E}_{OUT}$		40	50	nsec	A_i = $\overline{B}_i$

NOTE: A.C. Timing Measurements at V_{OH} = 2.0V and V_{OL} = 0.8V.

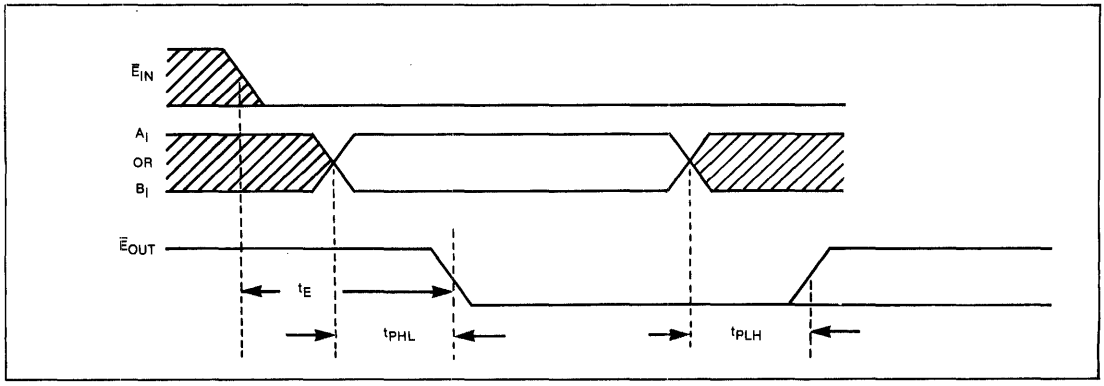


FIGURE 3
TIMING DIAGRAM

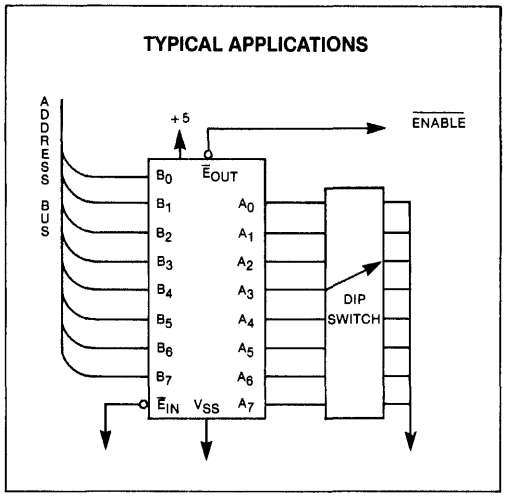


FIGURE 4
8 BIT PROGRAMMABLE ADDRESS BUS COMPARATOR

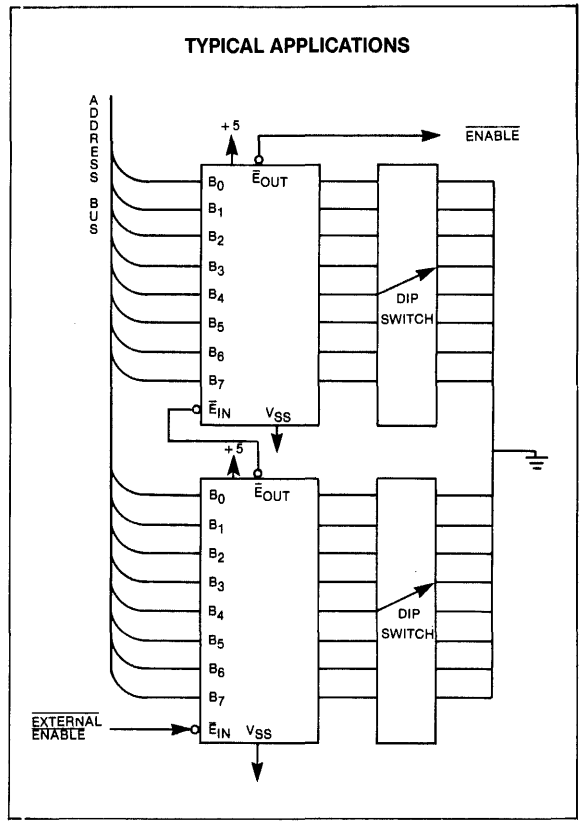


FIGURE 5
16 BIT PROGRAMMABLE COMPARATOR

See page 725 for ordering information.

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ADVANCE INFORMATION

WD2412 Time of Day Clock

FEATURES

- SELF CONTAINED TIMEBASE USING COMMON BAUD RATE CRYSTAL
- SOFTWARE SELECTABLE EXTERNAL 50 AND 60 Hz TIMEBASES
- PROVIDES HOURS, MINUTES, SECONDS, DAY, MONTH, DATE, AND YEAR
- TIME OF DAY IS AVAILABLE IN 12 AND 24 HOUR BCD AND BINARY
- BINARY TIME IS INTERNALLY CALCULATED FROM BCD TIME
- INTERRUPT AT ABSOLUTE TIME OF DAY OR TIME AND DATE
- INTERRUPT AT RELATIVE TIME
- AUTO RELOAD FOR PERIODIC INTERRUPTS
- PERIODIC INTERRUPTS CAN BE SET FROM 0.1 SEC TO 1 DAY
- TIME, DATE AND INTERRUPT REGISTERS MAY BE READ ON THE FLY
- TIME, DATE OR USER CAN BE DISPLAYED ON 6 DIGIT BY 7 SEGMENT DISPLAY
- AM, PM, DATE, AND TIME DISPLAY MODE INDICATORS
- DISPLAYED TIME CAN BE IN 12 OR 24 HOUR FORMATS
- POWER FAIL FLAG
- INPUTS AND OUTPUTS ARE TTL/CMOS COMPATIBLE
- SINGLE +4.5 TO +6.3 VOLT SUPPLY
- 28 PIN CERAMIC OR PLASTIC PACKAGE
- TEMPERATURE RANGES: 0° TO +70°C, −40° TO +85°C

GENERAL DESCRIPTION

The WD2412 Time of Day clock (TDC) is a complete timekeeping system offering hours, minutes, seconds, day of week, month, date and year. Time of day is available in both 24 and 12 hour BCD and straight binary formats. The BCD calendar automatically corrects for leap years up to the year 2100. The WD2412 can be programmed to provide relative or absolute real time interrupts with resolutions to a tenth of a second. Absolute interrupts can be based on time or time and date. The relative interrupt down counter can be read on the fly and reloads itself after an interrupt. 12 or 24 hour time of day, date, or user registers can be output to an external 6 digit by 7 segment display. Also TIME, DATE, AM and PM status indicators are provided. A flag is available to inform the host system that a catastrophic power failure has occurred. The WD2412 includes an 8 bit bi-directional bus so that it may be easily interfaced to most popular microcomputers. It is fabricated on a single NMOS LSI chip including all bus interface logic and crystal timebase oscillators. All inputs and outputs are TTL compatible.

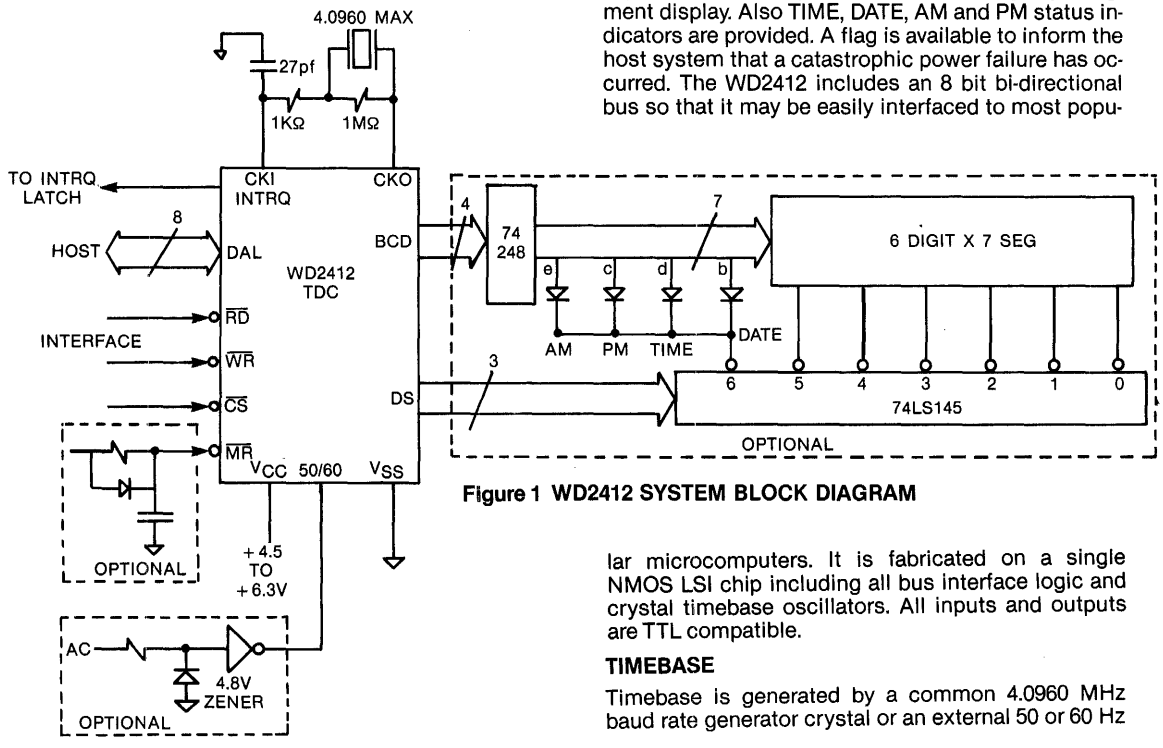


Figure 1 WD2412 SYSTEM BLOCK DIAGRAM

TIMEBASE

Timebase is generated by a common 4.0960 MHz baud rate generator crystal or an external 50 or 60 Hz

signal. On power up, the timebase defaults to the internal crystal, but a software command can be issued to the WD2412 to change its timebase over to 50 or 60 Hz or back to crystal again. Due to the fact that the 50/60 Hz timebase is not synchronized to the crystal oscillator, there may be a slight timebase error incurred when switching from internal to external timebases or back again. This timebase error is guaranteed not to exceed 0.1 second per timebase switch. When operating the WD2412 from an external timebase, it is not necessary to provide a crystal oscillator. Internal timing needs of the WD2412 can be satisfied by injecting a 4 MHz TTL level signal into the CKI terminal.

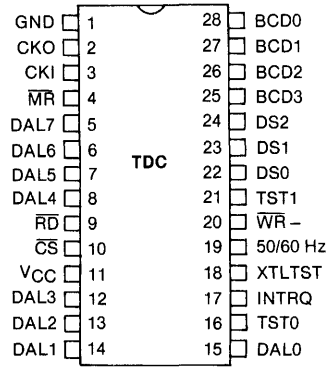


Figure 2
PIN DESIGNATIONS

PIN DESIGNATIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	POWER SUPPLY	V_{DD}	Ground
2	CLOCK OUT	CKO	Crystal oscillator output.
3	CLOCK IN	CKI	Crystal oscillator input.
4	MASTER RESET	MR	A logic low on this input clears all internal logic after power up. If rise time of power supply is less than 1 mS, then the external RC is optional. Normally, this line should not be tied to the system reset.
11	POWER SUPPLY	V_{CC}	+4.5 to +6.3 VDC
16	TEST0	TST0	Test pin. User leave open.
18	CRYSTAL TEST	XTLTST	When $\overline{MR}$ is held true this output toggles at CKI divided by 16.
19	EXT. TIMEBASE	50/60 Hz	This optional input provides the timebase if the 50 or 60 Hz external timebases are selected. The input signal should be of TTL levels with a rise time of better than 1μs and a low time of greater than 20μs. If this line is not used, it should be tied high or left open.
21	TEST1	TST1	Test pin. User leave open.

COMPUTER INTERFACE

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
5-8 12-15	DATA LINES	DAL 0-7	Eight active true three state bi-directional data I/O lines used for information transfer to and from the combined status/data register.
9	READ ENABLE	$\overline{RD}$	A low on read enable in conjunction with $\overline{CS}$ gates the contents of the status/data register onto the DAL lines.
10	CHIP SELECT	$\overline{CS}$	A low on chip select enables access to internal status/data register.
20	WRITE ENABLE	$\overline{WR}$	A low on write enable in conjunction with $\overline{CS}$ writes the state of the DAL lines to the status/data register.
17	INTERRUPT REQ.	INTRQ	Makes a low to high transition when the interrupt register needs servicing.

OPTIONAL DISPLAY INTERFACE

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
22-24	DIGIT SELECT	DS 0-2	Digit select for multiplexed display.
25-28	BCD OUT	BCD 0-3	BCD data for multiplexed display.

COMMAND DESCRIPTION

The WD2412 will accept and execute 24 commands. Command words should only be loaded onto the status/data register when the command ready status word appears on the status/data register. The command ready byte is EEH. Whenever a data transfer takes place, the receiving device (either the TDC or the host) must acknowledge the transfer by sending a FFH. For ease of discussion, commands are divided into three types.

Type I Commands

Type I commands set internal flags and operating modes. They are all considered completed after transfer of the command.

E0H DISPLAY OFF
E1H DISPLAY 12 HOUR TIME
E2H DISPLAY 24 HOUR TIME
E3H DISPLAY DATE
E4H DISPLAY USER
E5H SELECT CRYSTAL TIMEBASE
E6H SELECT EXTERNAL 50 Hz TIMEBASE
E7H SELECT EXTERNAL 60 Hz TIMEBASE
E8H DISABLE INTERRUPTS

COMPUTER DIALOG WITH TDC FOR TYPE I COMMANDS

STATUS 1	COMPUTER	←	TDC
if TDC ready:			
COMMAND	COMPUTER	→	TDC

Type II Commands

Type II commands set internal registers. They are all followed by three bytes of data. They are considered completed after transfer of data. All type II commands are non interruptable.

The commands are:

E9H SET 12 HOUR BCD TIME (BIN and BCD24 also set)
EAH SET 24 HOUR BCD TIME (BIN and BCD12 also set)
EBH SET DATE
ECH SET DAY OF WEEK
EDH SET USER
EFH SET ABSOLUTE 12 HOUR TIME INT (Interrupts are enabled)
F0H SET ABSOLUTE 24 HOUR TIME INT (Interrupts are enabled)
F1H SET ABSOLUTE DATE INTERRUPT (Interrupts are enabled)
F2H SET RELATIVE INTERRUPT (Interrupts are enabled)

COMPUTER DIALOG WITH TDC FOR TYPE II COMMANDS

STATUS 1	COMPUTER	←	TDC
if TDC ready:			
COMMAND	COMPUTER	→	TDC
STATUS 2	COMPUTER	←	TDC
if TDC ready:			
BYTE 1	COMPUTER	→	TDC
STATUS 2	COMPUTER	←	TDC
if TDC ready:			
BYTE 2	COMPUTER	→	TDC
STATUS 2	COMPUTER	←	TDC
if TDC ready:			
BYTE 3	COMPUTER	→	TDC

Type III Commands

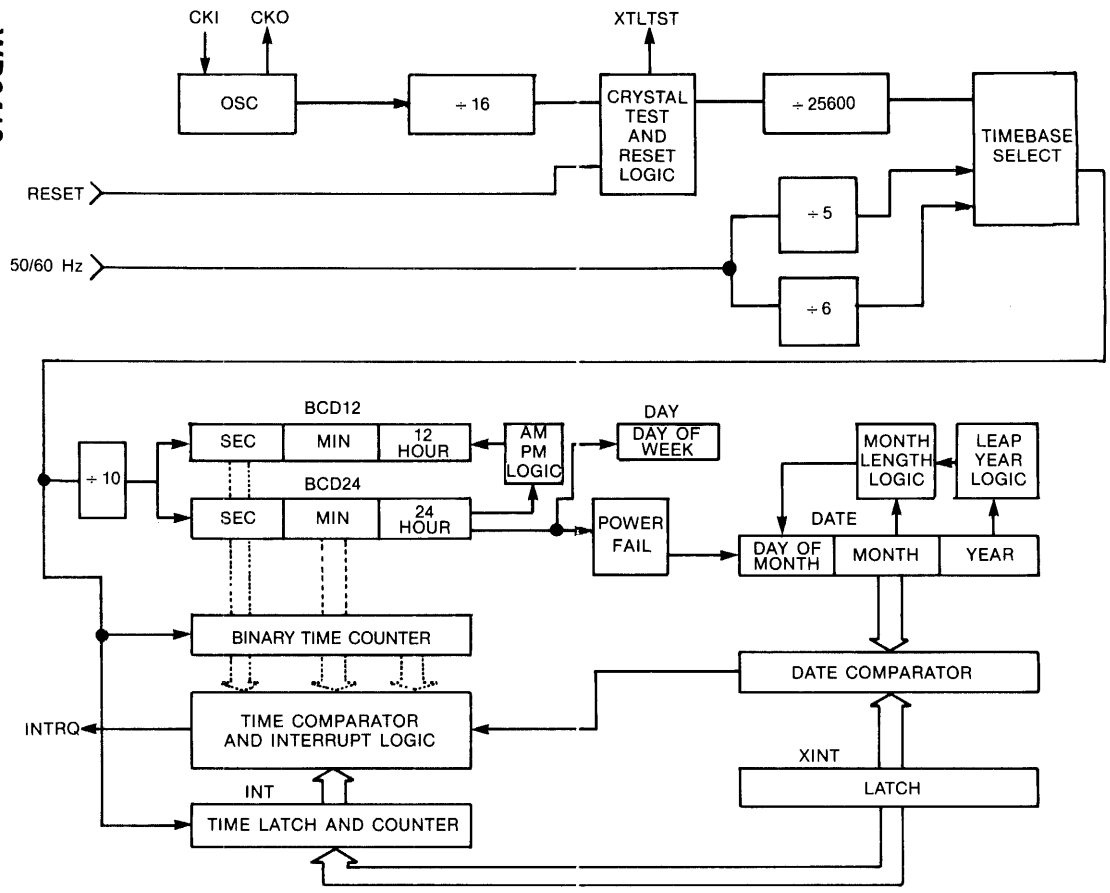
Type III commands read internal registers. They are all followed by three bytes of data. They are considered completed after transfer of data. All type III commands are non interruptable.

The commands are:

F3H READ 12 HOUR BCD TIME
F4H READ 24 HOUR BCD TIME
F5H READ BINARY TIME
F6H READ DATE/POWER FAIL FLAG
F7H READ DAY OF WEEK
F8H READ RELATIVE INTERRUPT

COMPUTER DIALOG WITH TDC FOR TYPE III COMMANDS

STATUS 1	COMPUTER	←	TDC
if TDC ready:			
COMMAND	COMPUTER	→	TDC
STATUS 3	COMPUTER	←	TDC
if TDC ready:			
BYTE 1	COMPUTER	←	TDC
ACKNOWLEDGE	COMPUTER	→	TDC
STATUS 4	COMPUTER	←	TDC
if TDC ready:			
BYTE 2	COMPUTER	←	TDC
ACKNOWLEDGE	COMPUTER	→	TDC
STATUS 4	COMPUTER	←	TDC
if TDC ready:			
BYTE 3	COMPUTER	←	TDC
ACKNOWLEDGE	COMPUTER	→	TDC



WD2412 FUNCTIONAL BLOCK DIAGRAM

Master Reset

Upon receipt of a Master Reset, the WD2412 defaults to the following values:

BCD24	00:00:00 (Midnight)
BCD12	12:00:00 AM
BIN	0
DATE	00/00/00
DAY	0 (Sunday)
RELATIVE INT	0
TIMEBASE	Crystal
DISPLAY	Off
INTERRUPTS	Disabled
POWER FAIL FLAG	Set

Power Fail Flag

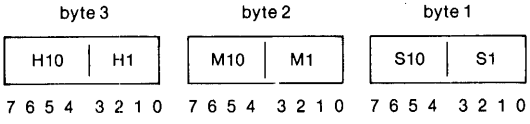
When power is restored to the WD2412, it initiates a master reset. As part of this, the Power Fail Flag is set. Normally, at the end of a day, the DAY and DATE registers are incremented. When the Power Fail Flag is set, the DATE register remains at 00/00/00 to indicate that the power failed although the DAY register is still incremented. Elapsed time since WD2412 power up can be determined by reading any time of day register in conjunction with the DAY register.

ORGANIZATION

The WD2412 includes eight 3-byte user addressable registers. These registers are 12 hour BCD Time of Day (BCD12), 24 hour BCD Time of Day (BCD24) Binary Time of Day (BIN), Date (DATE), Day (DAY), User (USR), Time of Day Absolute and relative interrupt register (INT) are extended (Date Absolute) interrupted register (XINT).

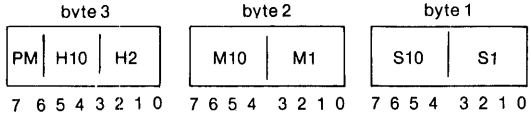
BCD24 Register

This read/write register holds the present time of day in a 24 hour BCD format. Data are arranged in a packed BCD format with two digits per byte.



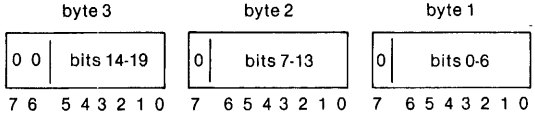
BCD12 Register

This read/write register holds the present time of day in a 12 hour BCD format. Data are arranged in a packed BCD format with two digits per byte. An AM/PM indicator is available on the most significant bit of the most significant byte. This bit is reset for AM and set for PM.



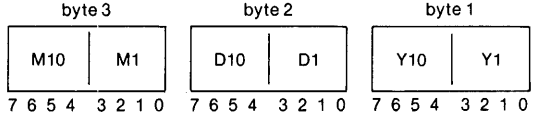
Bin Register

This read only register also holds the present time of day, but in a straight binary format. The format is in one-tenth second ticks since midnight. The value of this 20 bit register can vary from 0 through 863,999 decimal. Data is arranged in a seven bit per byte format with the most significant bit of the byte always set to zero.



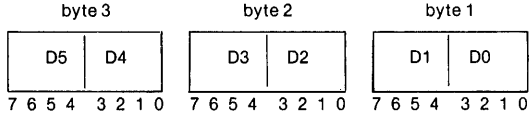
Date Register

This read/write register holds the present date in a BCD format. Again, data is arranged in a packed BCD format with two digits per byte.



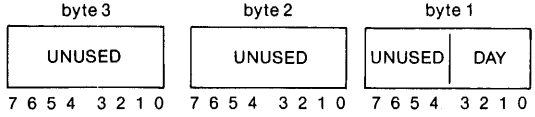
User Display Register

This write only register is used for user programmable outputs to the optional six digit display. Valid characters are 0-9 and blank. Blanks are entered as 10's.



Day Register

This read/write register holds the day of the week as a binary integer ranging in value from 0 to 6. Sunday is usually considered 0, but this is a completely arbitrary designation. For software simplicity, set day and read day are standard Type II and Type III commands respectively. On set day, the unused fields can be set to anything that won't interfere with the command protocol. On read day, the unused fields are zeroed.



INT and XINT Registers

These registers have three modes, depending on how they are set. In the relative mode, a binary countdown value is loaded into the INT register and an interrupt is generated when this value is decremented to zero. When the terminal value is reached, the register is automatically re-loaded, unless specifically disabled by the interrupt service routine. This feature allows periodic interrupts with no software overhead. The period can be set anywhere from 100 mS to 1 day.

If the INT register is read while in the relative mode, the number of ticks until interrupt will be returned. The data pattern is in the same format as in the BIN register.

In the absolute time mode, a time of day in the same format as the BCD24 register is loaded into the INT register. When this time is matched, a single interrupt will be produced and then the interrupts will be disabled. To enter the absolute time/date mode, load the INT register with the absolute time then load the XINT register with the absolute date. An interrupt will only be generated when both time and date match.

OPTIONAL DISPLAY

The WD2412 can interface to a seven segment by six digit display and four status indicators. 12 or 24 hour time, date, or user defined numeric message can be displayed. Four status indicators are provided as follows:

NAME	SEG	DESCRIPTION
AM	e	Lit only when displaying 12 hour time
PM	c	Lit only when displaying 12 hour time
TIME	d	Lit when displaying 12 or 24 hour time
DATE	b	Lit when displaying date

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin Relative to GND. . . −0.5V to +7V
Ambient Operating Temperature
(Note 1). . . . . 0°C to +70°C
Ambient Storage Temperature
Ceramic . . . . . −65°C to +150°C
Plastic. . . . . −55°C to +125°C
Lead Temperature (Soldering, 10 sec.) . . . . . 300°C
Power Dissipation . . . . . 0.75 Watt at 25°C
0.4 Watt at 70°C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

NOTE 1: An extended temperature range WD2412 is available which will operate within an ambient temperature range of −40°C to +85°C.

DC ELECTRICAL CHARACTERISTICS

$0°C \leqslant T_A \leqslant +70°C$, $4.5V \leqslant V_{CC} \leqslant 6.3V$ unless otherwise noted.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Operating Voltage (V_{CC})		4.5	6.3	V
Operating Supply Current	V_{CC} = 5V, T_A = 25°C (all inputs and outputs open)		40	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input				
Logic High (V_{IH})		2.0		V
Logic Low (V_{IL})			0.4	V
All Other Inputs				
Logic High	V_{CC} = Max	3.0		V
Logic High	V_{CC} = 5V ± 5%	2.0		V
Logic Low			0.8	V
Output Voltage Levels				
Standard Output				
TTL Operation	V_{CC} = 5V ± 5%			
Logic High (V_{OH})	I_{OH} = 100 μA)	2.4		V
Logic Low (V_{OL})	I_{OL} = −1.6 mA		0.4	V
THREE-STATE Output Leakage Current		−10	+10	μA

AC ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN/MAX	UNITS
Read Operation (Figure 4)			
Chip Select Stable Before RD — t_{CSR}	C_L = 50pf; V_{CC} = 5V ± 5%	50 min	ns
Chip Select Hold Time for RD — t_{RCS}		5 min	ns
RD Pulse Width — t_{RR}		300 min	ns
Data Delay from RD — t_{RD}		250 max	ns
RD to Data Floating — t_{DF}		200 max	ns
Write Operation (Figure 3)			
Chip Select Stable Before WR — t_{CSW}		20 min	ns
Chip Select Hold Time for WR — t_{WCS}		20 min	ns
WR Pulse Width — t_{WW}		300 min	ns
Data Set-Up Time for WR — t_{DW}		200 min	ns
Data Hold Time for WR — t_{WD}		40 min	ns

Figure 5 INPUT/OUTPUT TIMING DIAGRAM (CRYSTAL ÷ 16)

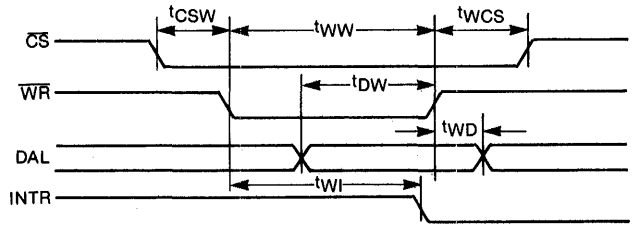


Figure 3 WRITE OPERATION TIMING

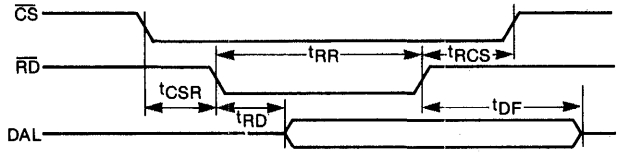


Figure 4 READ OPERATION TIMING

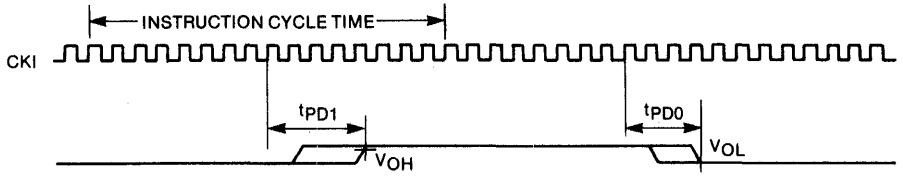


Figure 5 INPUT/OUTPUT TIMING DIAGRAM (CRYSTAL ÷ 16)

See page 725 for ordering information.

Printed in U.S.A.

Memory Products

FR1502 First-In/First-Out Buffer Register

FEATURES

- 40 CHARACTERS BY 9 BITS
- EXPANDABLE CHARACTER AND BIT SIZE (CASCADE CAPABILITY)
- DC TO 1 MHz ASYNCHRONOUS I/O ACCESS
- INPUT/OUTPUT READY STATUS FLAGS
- THREE STATE OUTPUTS
- SEPARATE INPUT AND OUTPUT ENABLES
- DIRECTLY TTL AND DTL COMPATIBLE
- MASTER RESET
- NO EXTERNAL CLOCKS REQUIRED
- AVAILABLE IN REL-PAC (F) OR CERAMIC (E) PACKAGES

APPLICATIONS

POINT OF SALE TERMINALS

DATA TRANSMISSION BUFFER

LINE PRINTER INPUT BUFFER

KEY-TO-TAPE/KEY-TO-DISC EQUIPMENT

CARD/TAPE READERS

AUTO DIALERS

CRT BUFFER MEMORY

CONTROL STACK SILO ORIENTED MACHINES

COMPUTER/TERMINALS I/O INTERFACE BUFFER

TELEPRINTER BUFFER

GENERAL DESCRIPTION

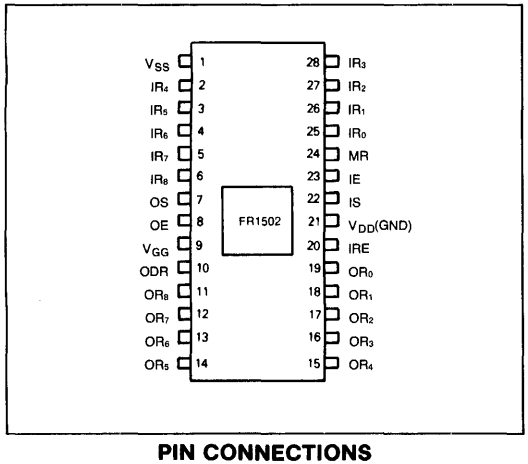
The FIFO (First-In/First-Out) Storage Chip is an asynchronous memory organized in a nine-bit by forty-character stack. Characters are loaded at the top of the stack and then "sink" to the bottom of the stack, or to the level of previously entered data, without external clocks being applied. As a character is taken from the bottom of the stack, all of the previously loaded characters will automatically propagate toward the output (bottom of stack).

Data can be entered whenever the INPUT REGISTER EMPTY line is high by strobing INPUT STROBE. The INPUT ENABLE line must also be high while strobing. The INPUT STROBE resets INPUT REGISTER EMPTY and latches the input data. As soon as this data is latched, INPUT REGISTER EMPTY will again go high and additional data can be loaded.

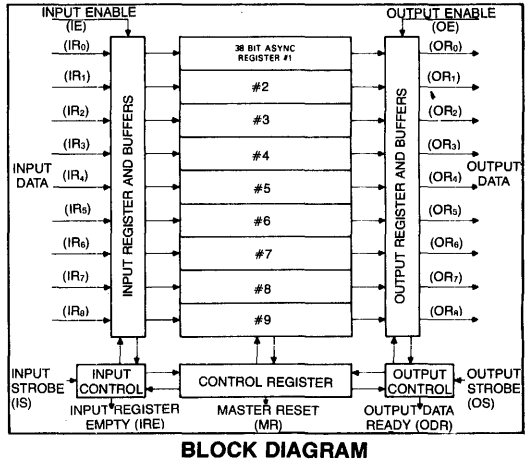
When data reaches the FIFO output, the OUTPUT DATA READY line will go high. The data is then valid at the outputs (providing the OUTPUT ENABLE line is high). The falling edge of the OUTPUT STROBE causes the OUTPUT DATA READY line to go low and to shift new data into the output register. When the new data is available, the OUTPUT DATA READY signal again goes high.

The FIFO output data lines are in high impedance state whenever the OUTPUT ENABLE line is low.

The logic conventions and internal delays designed into the FIFO allow direct expansion of the memory without external hardware (Cascade Mode).



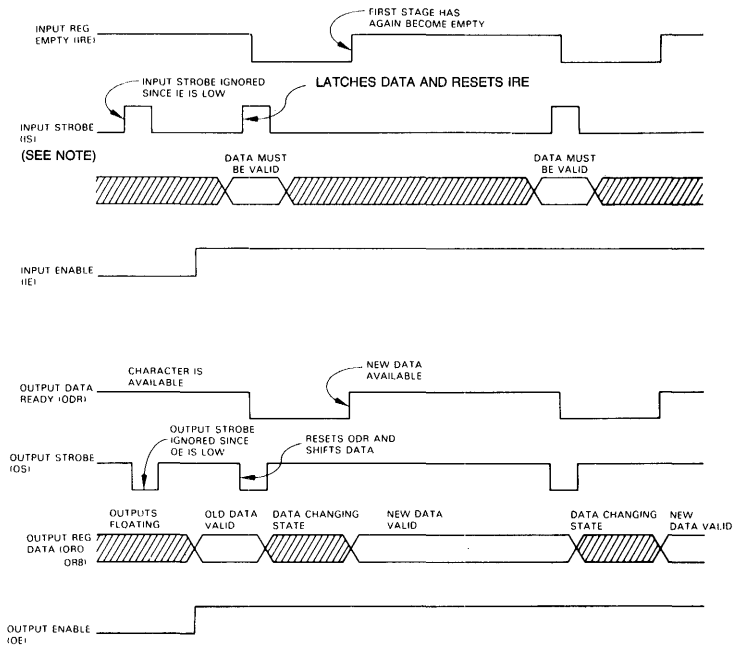
PIN CONNECTIONS



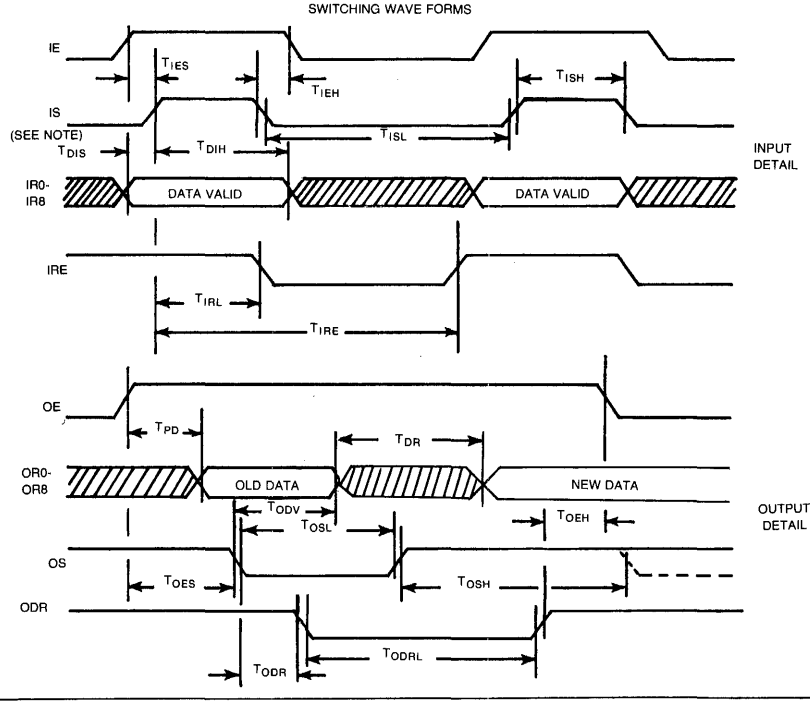
BLOCK DIAGRAM

INTERFACE SIGNALS DESCRIPTIONS

PIN NUMBER	SIGNAL NAME	SYMBOL	FUNCTION
25-28, 2-6	INPUT REGISTER	IR0-IR8	Input datalines. These are input (but not latched) to the FIFO independently of the INPUT ENABLE or INPUT STROBE.
20	INPUT REGISTER EMPTY	IRE	When high, indicates that data can be loaded into the FIFO. It is reset to a low by falling edge of the Input Strobe.
22	INPUT STROBE	IS	Latches INPUT DATA in the FIFO on rising edge.
24	MASTER RESET	MR	When high, clears the FIFO control registers. This leaves the OUTPUT REGISTER DATA (OR0-OR8) in an undefined state, sets INPUT REGISTER EMPTY (IRE) to high and resets OUTPUT DATA READY (ODR) to low.
19-11	OUTPUT REGISTER DATA	ORO-OR8	Three state data outputs. When OE is low, the outputs are in the high impedance state. When OE is high, these lines present the previous latched data in a first-in/first-out manner.
10	OUTPUT DATA READY	ODR	ODR is high when data is latched and available at the data output lines. Is reset to low by the falling edge of OUTPUT STROBE (OS) if OUTPUT ENABLE (OE) is high.
7	OUTPUT STROBE	OS	A falling edge of this signal resets the OUTPUT DATA READY (ODR) line and then shifts the data one step towards the output if OUTPUT ENABLE (OE) is high.
23	INPUT ENABLE	IE	When high, enables the input control logic. At any state of IE or IS, the INPUT DATA will be transferred into the FIFO, but can not be latched unless IE is high.
8	OUTPUT ENABLE	OE	When low, OE puts the output lines (OR0-OR8) in high impedance state. When high, the output lines present the output data.
1	V_{SS} POWER SUPPLY	V_{SS}	+5VDC
21	V_{DD} POWER SUPPLY	V_{DD}	0 Volt—GND
9	V_{GG} POWER SUPPLY	V_{GG}	−12VDC



SWITCHING CHARACTERISTICS



SWITCHING WAVE FORMS

ABSOLUTE MAXIMUM RATINGS

V_{GG} Supply Voltage	+0.3V to -20V
V_{DD} Supply Voltage	+0.3V to -20V
Clock Input Voltage*	+0.3V to -20V
Logic Input Voltage*	+0.3V to -20V
Logic Output Voltage*	+0.3V to -20V
Storage Temperature (Ceramic)	−65°C to +150°C
Storage Temperature (Plastic)	−55°C to +125°C

*V_{GG} = VDD = 0V

NOTE: These voltages are measured with respect to V_{SS} (Substrate)

ELECTRICAL CHARACTERISTICS

(V_{SS} = +5V ± 5%; V_{DD} = 0V; V_{GG} =-12V ± 5%; TA = 0°C to +70°C unless otherwise specified)

SYMBOL	PARAMETER	MIN	MAX	CONDITIONS
	INPUT LOGIC LEVELS			
V_{IL}	Low-level Input Voltage		0.8V	V_{SS} = 4.75V
V_{IH}	High-level Input Voltage	V_{SS}−1.5V		(NOTE 1)
	OUTPUT LOGIC LEVELS			(NOTE 2)
V_{OL}	Low-level Output Voltage		0.4V	V_{SS} = 5.25V I_{OL} = −1.6mA
V_{OH}	High-level Output Voltage	V_{SS}−1.0V		V_{SS} = 4.75V I_{OH} = +200 uA
	INPUT CURRENT			
I_{IL}	Low-level Input Current (each pin)		−1.6mA	V_{SS} = 5.25V V_{IN} = 0.4V
I_{SS}	SUBSTRATE SUPPLY CURRENT		65 mA	V_{SS} = 5.25V V_{GG} = −12.6V
I_{GG}	GATE SUPPLY CURRENT		−30mA	V_{IN} = 0.4V

NOTE 1: All inputs have pull-up resistors. This allows unloaded TTL outputs of 2.0V to be connected and operate properly. When connected, this voltage (2.0V) will become V_{SS} −1.5V.

NOTE 2: V_{OL} and V_{OH} when OE = V_{IH} (low impedance output). High impedance (OE = V_{IL}) ≈ 10 Mohm.

SWITCHING CHARACTERISTICS — See "Switching Waveforms"

(V_{SS} = +5V, V_{DD} = 0V, V_{GG} = −12V, T_A = 0°C to +70°C, C_{LOAD} = 10 pf)

SYMBOL	PARAMETER	MIN	MAX	CONDITIONS
T_{IES}	Input Enable Setup Time	0 ns		
T_{IEH}	Input Enable Hold Time	0 ns		
T_{DIS}	Data Input Setup Time	0 ns		
T_{DIH}	Data Input Hold Time	250 ns		
T_{IRL}	Input Register Load Time		250 ns	
T_{IRE}	Input Register Empty Time		800 ns	
T_{ISL}	Input Strobe Low Time	450 ns		
T_{ISH}	Input Strobe High Time	150 ns		
T_{OES}	Output Enable Setup Time	50 ns		
T_{OEH}	Output Enable Hold Time	50 ns		(NOTE 1)
T_{OSL}	Output Strobe Low Time	150 ns		
T_{ODR}	Output Data Ready Time		200 ns	
T_{DR}	Data Reset Time		600 ns	
T_{PD}	Output Propagation Delay Time		250 ns	
T_{ODRL}	Output Data Ready Low		600 ns	
T_{OSH}	Output Strobe High Time	500 ns		
T_{ODV}	Output Data Valid Time		200 ns	
T_R	Maximum Ripple Time		10 μs	(NOTE 2)
T_B	Maximum Bubble Time		25 μS	(NOTE 3)
T_{MR}	Master Reset Pulse Time	500 ns		
f_D	Maximum Data Rate		1 MHz	(NOTE 4)

NOTE 1: $T_{rise} = T_{fall} = 10nS$.

NOTE 2: Ripple Time—time required for a single data character to propagate from the input to the output of an empty FIFO (IS strobing edge to ODR rising edge).

NOTE 3: Bubble Time— time required for a "hole" to propagate from the output to the input of a full FIFO (falling edge of OS to rising edge of IRE).

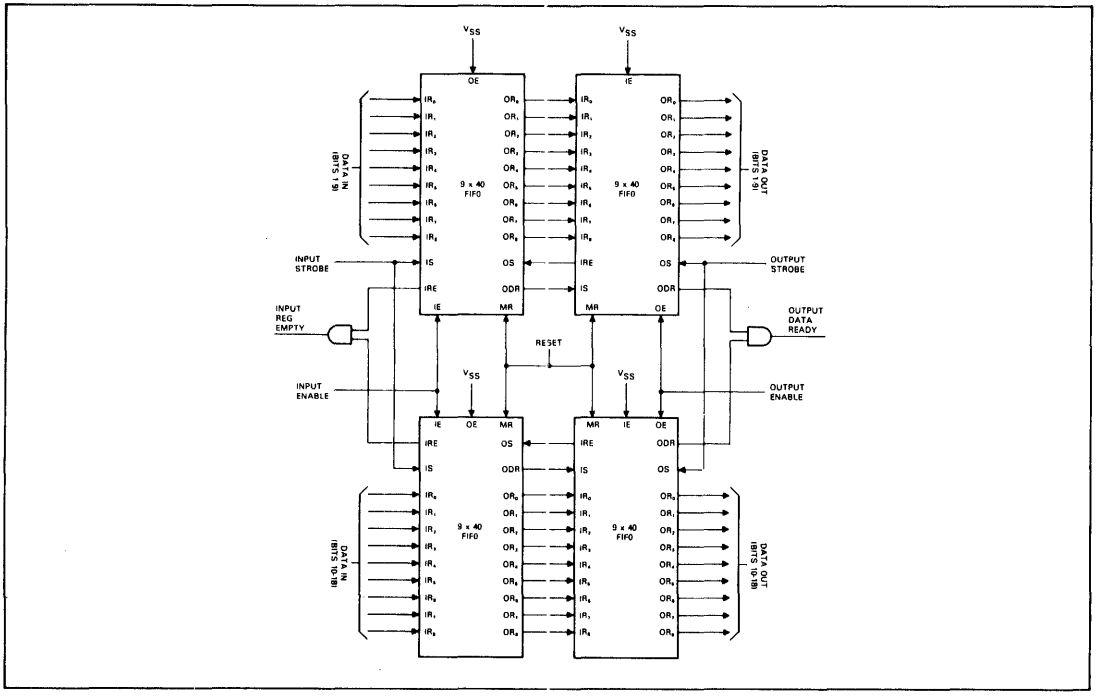
NOTE 4: The maximum data rates for a "single" FIFO (not cascaded) and for FIFO's cascaded together are the same.

GENERAL NOTE: All A.C. test points are at 0.8V or 2.0V.

ORDERING INFORMATION

T_A = O°C to +70°C

PART NO.	PACKAGE TYPE	CASCADABLE	MAX. DATA RATE
E-10	CERAMIC	YES	1.0 MHz
F-10	PLASTIC	YES	1.0 MHz
E-11	CERAMIC	NO	500 KHz
F-11	PLASTIC	NO	500 KHz



EXPANSION EXAMPLE
FR1502E/F-10

See page 725 for ordering information.

WD1510-00,-01,-02 LIFO/FIFO Buffer Register

FEATURES

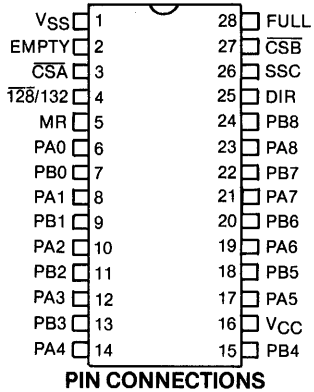
- WORD LENGTH SELECTABLE: 128 OR 132
- 9 BIT WORD WIDTH
- DC TO 650 KHZ (–00), 1 MHz (–01), 1.2 MHz (–02)
- EMPTY AND FULL FLAGS
- THREE-STATE DATA LINES
- 5-VOLT ONLY
- NO EXTERNAL CLOCKS REQUIRED
- TTL COMPATIBLE ON ALL INPUTS AND OUTPUTS
- 28 PIN PLASTIC OR CERAMIC DIP
- CASCADABLE WITH WD1511 SUPPORT CHIP
- FULLY ASYNCHRONOUS DUAL PORT OPERATION

GENERAL DESCRIPTION

The WD1510 is an MOS/LSI Memory Buffer which is organized as a 9-bit by 128 or 132 word stack. The chip has 2 bidirectional data ports and may be read from or written into either port. Thus, the chip can function as a LIFO from either port or it can function as a FIFO, with data flow from either port A to port B or vice versa. The DIRECTION input pin is used to specify the data flow direction. The WD1510 is fabricated in 5-volt only N-channel technology.

APPLICATIONS

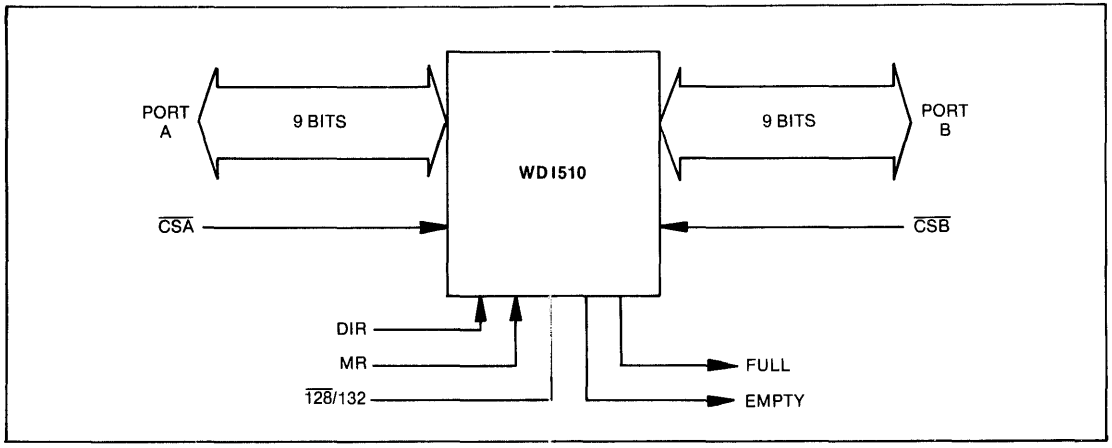
- POINT OF SALE TERMINALS
- COMPUTER-TO-PERIPHERAL BUFFER
- CRT BUFFER MEMORY
- LINE PRINTER BUFFER
- INTERRUPT STACK (LIFO MODE)



PIN CONNECTIONS

PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	VSS	VSS	Ground
2	EMPTY	EMPTY	Indicates when there is no data in the buffer
3	CHIP SELECT PORT A	$\overline{CSA}$	Used to select Port A for either a Read or Write operation
4	128 OR 132	$\overline{128}$/132	Used to set word length. When low word length = 128, when high word length = 132
5	MASTER RESET	MR	When pulsed will clear the buffer and set the EMPTY pin
6,8,10,12,14, 17,19,21,23	PORT A DATA LINES	PA0-PA8	Bidirectional DATA Port for reading or writing
7,9,11,13,15 18,20,22,24	PORT B DATA LINES	PB0-PB8	Bidirectional DATA Port for reading or writing
16	VCC	VCC	+5 volts ±.25V
25	DIRECTION	DIR	When low DIR specifies that Port A may be read from and Port B may be written into. When high DIR specifies that Port A may be written into and Port B may be read from.
26	SYSTEM SENTINEL™ CHECKOUT	SSC	No connection (For future use)
27	CHIP SELECT PORT B	$\overline{CSB}$	Used to select Port B for either a Read or Write Operation
28	FULL	FULL	Indicates that all 132 or 128 words of memory are loaded with data



OPERATION

The WD1510 contains a 132 x 9 buffer which may be programmed for 128 x 9 operation. Setting the $\overline{128}$/132 pin to a Logic 0 enables the EMPTY and FULL lines to be activated when 128 bytes are read or written. When the $\overline{128}$/132 line is set to a Logic 1 or left open, the 132 byte operation is enabled. This line contains an internal pull-up resistor of approximately 5KΩ.

When the Master Reset Line (pin 5) is set to a Logic 1, all internal counters are reset and the EMPTY Flag is set. Prior to reading or writing data, the DIRECTION Line (pin 25) must be set to select the desired operation:

DIR	PORT A	PORT B
1	WRITE	READ
0	READ	WRITE

To operate the device in the FIFO mode, both Ports must be used. If the DIRECTION Line is set to a Logic 1, then data is written into Port A and read out of Port B. Reading/Writing to the two ports can be done asynchronously.

In the LIFO mode only one port is used. For example, if using Port A, the DIRECTION Line is set to a Logic 1 to enter data, and is reset to a Logic 0 to read data.

Reading or writing is performed by setting the appropriate $\overline{CS}$ (Chip Select) Line to a Logic 0. After the specified hold time has expired, data may be entered or read on the rising edge of $\overline{CSA}$ or $\overline{CSB}$. In a Read mode, data is valid as long as $\overline{CS}$ remains active. Both Ports return to the high impedance state when $\overline{CS}$ is returned to a Logic 1.

The EMPTY Line (Pin 2) and the FULL Line (Pin 28) are used as status or interrupt lines to determine the status of the buffer. When both EMPTY and FULL are at a Logic 0, the buffer contains 1 thru 127 bytes ($\overline{128}$/132 = 0) or 1 thru 131 bytes ($\overline{128}$/132 = 1).

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{CC} with respect to V_{SS} (Ground) ..... +7V
Max Voltage on any Pin with respect to V_{SS} ..... −0.5V to +7V
Operating Temperature ..... 0°C to 70°C
Storage Temperature
Plastic ..... −55°C to +125°C
Ceramic ..... −65°C to +150°C

OPERATING CHARACTERISTICS (DC)

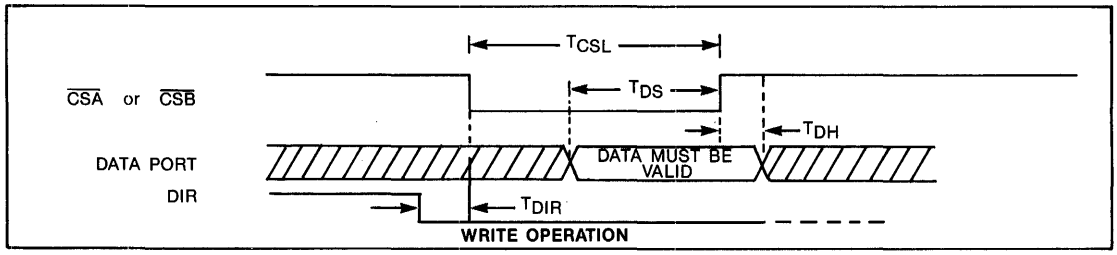
TA = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	μA	V_{IN} = V_{CC}
I_{LO}	Output Leakage			10	μA	V_{OUT} = V_{CC}, V_{SS}
V_{IH}	Input High Voltage	2.2			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH}	Output High Voltage	2.4			V	I_O = −100μA
V_{OL}	Output Low Voltage			.4	V	I_O = 1.6 mA
I_{CC}	Power Supply Current		125	200	mA	All outputs open

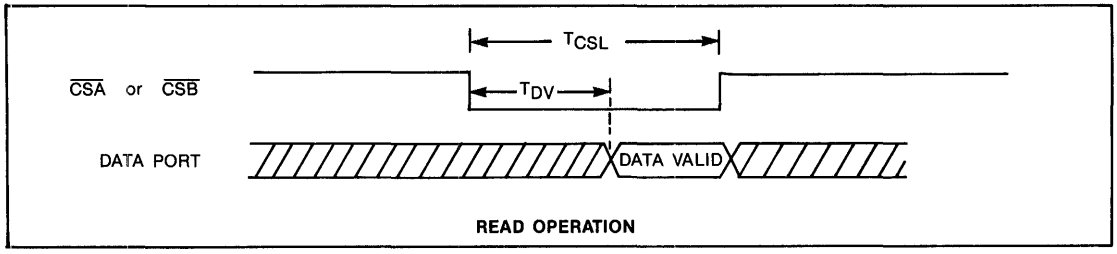
A.C. TIMING CHARACTERISTICS

TA = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ± .25V, V_{OH} = 2.0V, V_{OL} = 0.8V

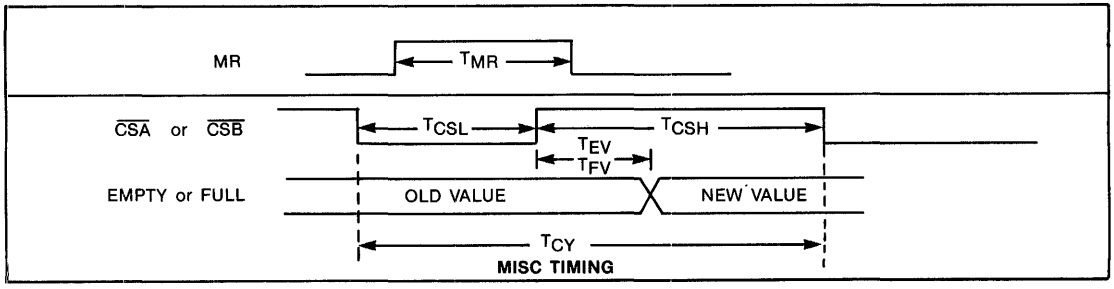
SYMBOL	CHARACTERISTICS	WD1510-00		WD1510-01		WD1510-02		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
T_{MR}	Master Reset Time	400		250		250		NS.
T_{DV}	Data Valid from CS		550		350		300	NS.
T_{DH}	Data Hold from CS	150		100		80		NS.
T_{DIR}	DIR Setup Time	1500		1000		834		NS.
T_{EV}	EMPTY Valid from CS		550		350		250	NS.
T_{FV}	FULL Valid from CS		550		350		250	NS.
T_{CSL}	CS Pulse Width Low	600		500		417		NS.
T_{CSH}	CS Pulse Width High	600		500		417		NS.
T_{CY}	CS Cycle Time	1540		1000		834		NS.
T_{DS}	Data Setup Time	80		50		50		NS.
F_{MAX}	Data Transfer Rate		.65		1.0		1.2	MHZ



WRITE OPERATION



READ OPERATION



MISC TIMING

See page 725 for ordering information.

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ADVANCE INFORMATION

WD1511 LIFO/FIFO Support Device

FEATURES

- CASCADES UP TO 4 ASYNCHRONOUS RAM BASED LIFO'S/FIFO'S
- CONTROLS 2-TO-1 OR 4-TO-1 BUFFERED BUS CONVERSION
- PIN SELECTABLE OPERATING MODES
- LOGICALLY TRANSPARENT TO HOST INTERFACE
- ALL INPUTS AND OUTPUTS TTL COMPATIBLE
- SINGLE +5V SUPPLY
- 20 PIN DUAL-IN-LINE PACKAGE
- DIRECT COMPATIBILITY WITH THE WD1510 LIFO/FIFO

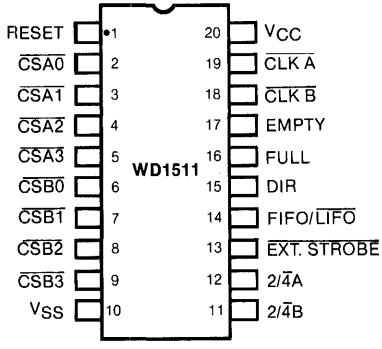
DESCRIPTION

The WD1511 is designed to cascade RAM based FIFO's without resorting to 'bucket brigade' architectures. Cascading is implemented by logically demultiplexing sequential data bytes into two (or four) FIFO's. Data read out of the FIFO's is logically multiplexed, restoring the original order.

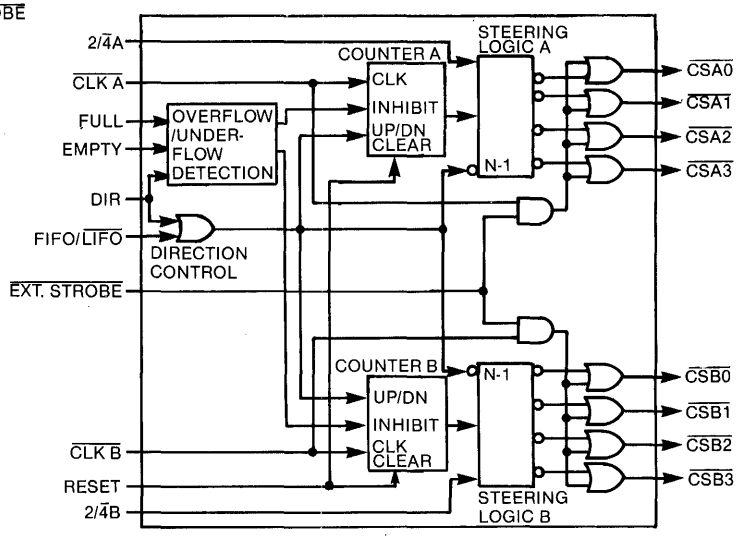
The WD1511 provides all of the necessary data strobe steering logic to demultiplex/multiplex the data stream for both FIFO and LIFO applications. This technique is also employed in implementing 2-to-1 or 4-to-1 bus conversion.

Normally, data strobes are routed through the WD1511. However, in applications where data hold times are critical, grounding the $\overline{\text{EXT. STROBE}}$ pin makes it possible to reduce propagation delays by gating the strobes externally to the WD1511.

The WD1511's cascading technique reduces the duty factor for each FIFO device and may make higher throughput possible.



PIN DESIGNATION



FUNCTIONAL BLOCK DIAGRAM

ORGANIZATION

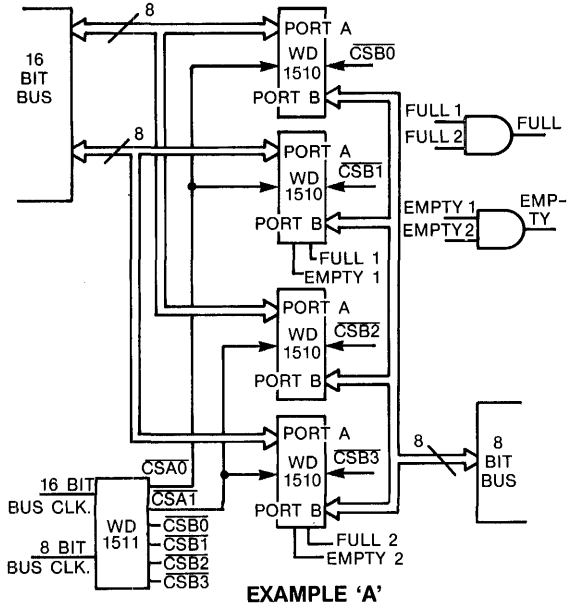
The WD1511 is organized as a pair of synchronous up/down Gray counters with fully decoded outputs. Clocking occurs on low-to-high transitions of the clock inputs. FULL and EMPTY FIFO status inputs are gated with DIR to inhibit counting during FIFO overflow or underflow. A logic one on either DIR or FIFO/$\overline{\text{LIFO}}$ causes the counters to increment when clocked and the decoders to decode for N. A logic zero on both the DIR and FIFO/$\overline{\text{LIFO}}$ inputs causes the counters to decrement when clocked and the decoders to decode for N-1. A2/$\overline{4}$ and B2/$\overline{4}$ determine the number of active discrete outputs for each decoder. A logic one on $\overline{\text{EXT. STROBE}}$ causes both decoders' active low outputs to be "OR-ED" with the counter clocks. Reset forces the counters to asynchronously clear.

WD1511 PIN DEFINITIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	RESET	RESET	Active high input. Asynchronously clears counter A and counter B.
2, 3, 4, 5	CHIP SELECT 'A' OUTPUTS	CSA0-CSA3	Active low, 1-of-4 CSA steering logic outputs. $\overline{\text{CLKA}}$ or $\overline{\text{EXT. STROBE}}$ must be low to enable the active output.
6, 7, 8, 9	CHIP SELECT 'B' OUTPUTS	CSB0-CSB3	Active low, 1-of-4 CSB steering logic outputs. $\overline{\text{CLKB}}$ or $\overline{\text{EXT. STROBE}}$ must be low to enable the active output.
10	V_{SS}	V_{SS}	Ground
11	2/$\overline{4}$B	2/$\overline{4}$B	This input selects the number of active CSB outputs. When 2/$\overline{4}$B is open or held high, 1-of-2 decoding is performed on counter 'B'; $\overline{\text{CSB2}}$ and $\overline{\text{CSB3}}$ are inactive and remain high, independently of the state of counter 'B'. When 2/$\overline{4}$B is low, 1-of-4 decoding is performed on counter 'B'. This input includes an internal pull-up resistor of approximately 6.5KΩ.
12	2/$\overline{4}$A	2/$\overline{4}$A	This input selects the number of active CSA outputs. When 2/$\overline{4}$A is open or held high, 1-of-2 decoding is performed on counter 'A'; $\overline{\text{CSA2}}$ and $\overline{\text{CSA3}}$ are inactive and remain high, independently of the state of counter 'A'. When 2/$\overline{4}$A is low, 1-of-4 decoding is performed on counter 'A'. This input includes an internal pull-up resistor of approximately 6.5KΩ.
13	EXTERNAL STROBE	$\overline{\text{EXT. STROBE}}$	This active low input enables the CSA and CSB outputs independently of the levels of $\overline{\text{CLKA}}$ and $\overline{\text{CLKB}}$. With $\overline{\text{EXT. STROBE}}$ low, several options are available; the chip select outputs can be clocked externally with a 74LS02 or equivalent to generate active high data strobes; a 74LS32 or equivalent can be used to generate active low data strobes; WD1511's can be cascaded without additive propagation delays; the WD1511 can be used as a dual, 4-output Johnson counter. This input includes an internal pull-up resistor of approximately 6.5KΩ.
14	FIFO/$\overline{\text{LIFO}}$	FIFO/$\overline{\text{LIFO}}$	When this input is open or held high, or when the DIR input is high, the active steering logic outputs are equal to the current states of the counters and the counters will increment when clocked. When both the FIFO/$\overline{\text{LIFO}}$ and DIR inputs are low, the active steering logic outputs are equal to the current states of the counters, logically minus one, and the counters will decrement when clocked. This input includes an internal pull-up resistor of approximately 6.5KΩ.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
15	DIRECTION	DIR	This input determines which counter shall be inhibited when the full or empty inputs are active. It is also gated with the FIFO/$\overline{\text{LIFO}}$ input to control steering logic decoding and provide counter up/down control.
16	FULL	FULL	This active high input is used to prevent the data pointers (chip selects) from being invalidated during overflow conditions. When both the FULL and DIR inputs are high, counter 'A' is inhibited or frozen at its current count. When FULL is high and the DIR input is low, counter 'B' is inhibited. This input must be held low if unused.
17	EMPTY	EMPTY	This active high input is used to prevent the data pointers (chip selects) from being invalidated during underflow conditions. When both the EMPTY and DIR inputs are high, counter 'B' is inhibited or frozen at its current count. When EMPTY is high and the DIR input is low, counter 'A' is inhibited. This input must be held low if unused.
18	CLOCK B	$\overline{\text{CLK B}}$	This input clocks counter 'B' on the low-to-high transition. The active 1-of-4 CSB output is enabled when either CLKB or EXT. STROBE is low.
19	CLOCK A	$\overline{\text{CLK A}}$	This input clocks counter 'A' on the low-to-high transition. The active 1-of-4 CSA output is enabled when either $\overline{\text{CLKA}}$ or $\overline{\text{EXT. STROBE}}$ is low.
20	V_{CC}	V_{CC}	+5VDC ±5%

16 x 256 TO 8 x 512 BIDIRECTIONAL FIFO BUFFER

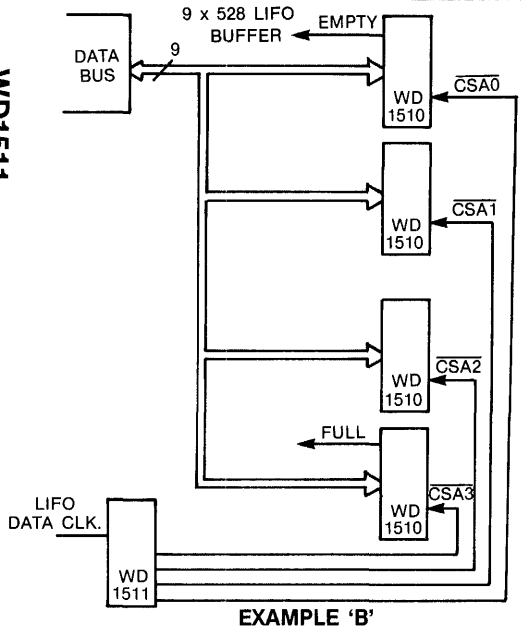


EXAMPLE 'A'

Example 'A' shows the WD1511 used to convert a 16 bit data bus to an 8 bit data bus. With the availability of 4 steering logic outputs, the implementation shown also utilizes the cascade feature providing a 256x16 to 512x8 FIFO Buffer. By placing a logic high on 2/$\overline{4}$B of the WD1511, decoding would be reduced to 1 of 2 allowing a reduced buffer of 128x16 to 256x8.

A key feature of this implementation is the ability to obtain a speed enhancement for both sides of the data bus. As shown with the WD1510-01, the 8 bit data may be read out at a 2MHz rate. This is due to the FIFO's T_{CSH} time being met during the access times of the other devices. Another key feature with a WD1510 implementation is the completely asynchronous 16 and 8 bus clocks, thereby allowing bidirectional reads and writes asynchronously.

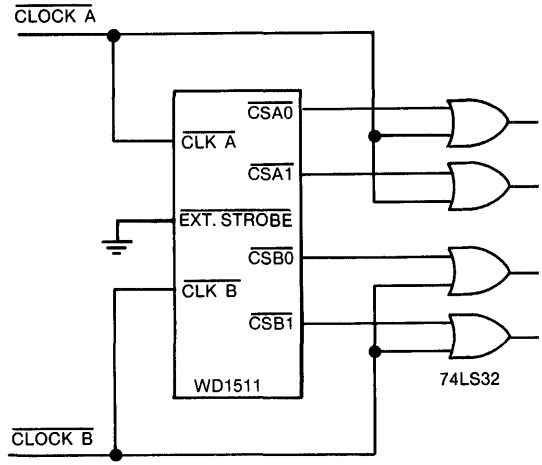
The basic system shown is easily modified to provide many variations. Some of these are: 16 to 16 bit FIFO, 264x18 to 512x9 conversion, 512x9 to 512x9 FIFO, all of which can be bidirectional.



EXAMPLE 'B'

Example 'B' illustrates the simplicity in implementing four WD1510s cascaded for a 528x9 LIFO. This circuit provides the same speed enhancement as Example 'A'. With the WD1510-01, a 2MHz byte rate transfer can be obtained.

It also is easily modified to provide many reduced variations such as 256x8 or 9, or 512x8 or 9.



EXAMPLE 'C'

Example 'C' is shown with $\overline{\text{EXTSTROBE}}$ enabled. This feature reduces the propagation delay of the WD1511 to zero. This feature is required for systems unable to meet data hold times. It is also recommended for use where WD1511s are cascaded for large buffer size applications.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias ..... 0 to 70°C
Voltage On Any Pin With Respect to Ground (V_{SS}) ..... −0.5 to +7V
Power Dissipation 0.5W

Storage Temperature
Ceramic ..... −65°C to +150°C
Plastic ..... −55°C to +125°C

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

DC ELECTRICAL CHARACTERISTICS

T_A = 0 to 70°C; V_{CC} = 5.0V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	−0.5		+0.8	V	
V_{IH}	Input High Voltage	2.2			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0mA
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current		70	100	mA	All outputs open

See page 725 for ordering information.

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ADVANCE INFORMATION

WD5010 Single/Dual Read Content — Addressable Memory

FEATURES

- DUAL READ CAPABILITY
  16x64 BIT WORDS
  TWO LOCAL VARIABLE ADDRESSES
- SINGLE READ CAPABILITY
  32x32 BIT WORDS
  ONE LOCAL VARIABLE ADDRESS
- WRITEABLE CONTENT WORDS
- VERTICAL CASCADING CAPABILITY
- REPLACES CACHE ADDRESSING SYSTEMS

A Content Addressable Memory (CAM) is a memory device in which all memory cells are selected by contents rather than by addresses. The CAM's function is to compute local variable addresses from global addresses by means of a fully associative memory.

APPLICATIONS

Cache Memory Replacement
Cache Disk Controller
Pattern Recognition
Station Address Recognition
Primary Key Locater
Programmable PLA

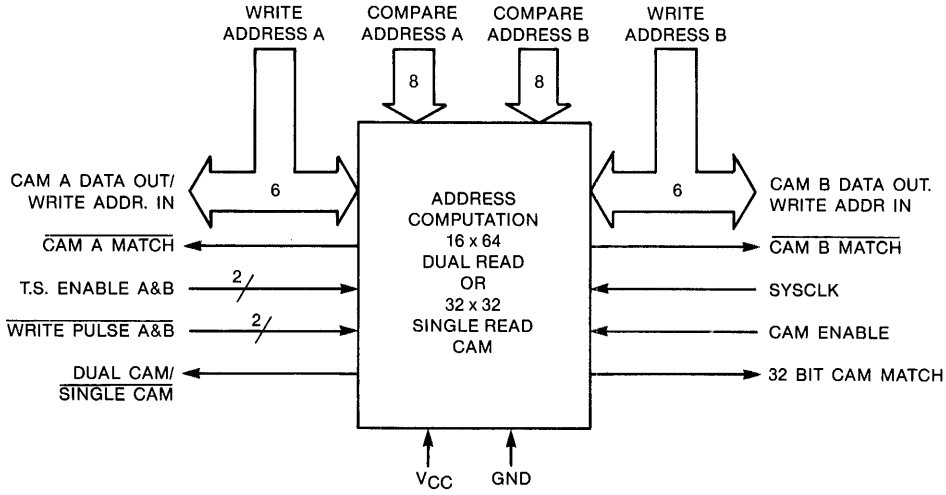
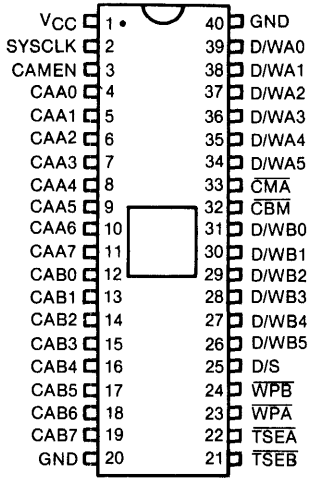


Figure 1 — WD5010 CAM OVERVIEW BLOCK DIAGRAM



PIN CONNECTIONS

FUNCTIONAL DESCRIPTION

The central component of the CAM is a RAM cell with dual compare logic. When the address computation is in dual read configuration 6 bits of CAM data are provided when the Compare Address is matched with one of the 64 content words in the CAM. The 6 bit CAM Data Out numbers range from 000000_2 to 111111_2 and are non-volatile. A CAM Match signal is provided for each of the Compare A and Compare B Addresses and indicates if the content words of the CAM match the Compare Address. See Figure 1.

Each content word address inside the CAM is directly related to the Data Out number. By enabling the Write Address Enable and providing a Write Pulse and the desired Write Address on the DATA OUT/WRITE ADDRESS IN LINES, the contents of the CAM related to that Data Out number are written.

In the dual read mode, the CAM compares the contents within itself and the Compare Address. If a match occurs between the Compare Address and one of the content words, then the data associated with that content word will appear on the CAM Data Out lines and a CAM Match signal will occur. In the single CAM read mode, the Compare Addresses A and B concatenate to form a 32 bit word. This word is compared with a 32 bit CAM word formed by two consecutive 16 bit content words. If a match occurs the associated CAM data appears at both the CAM data A and B lines and both A&B CAM Match signal occurs.

During write mode, the Compare Address is the information which will be written into the content word. The CAM has two sets of Compare Address and Write Address lines which allows two content words to be written at the same time.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	POWER SUPPLY	V_{CC}	+5 Volt
2	SYSTEM CLOCK	SYSCLA	Provides clock to CAM.
3	CAM ENABLE	CAMEN	Enables CAM operation.
4-11	COMPARE ADDRESS A	CAA0-CAA7	During a dual read operation two 16 bit addresses are latched into the CAM through these two 8 bit ports.
12-19	COMPARE ADDRESS B	CAB0-CAB7	The CAM then compares the contents within itself and outputs the data if a match occurs. In the single read mode, the Compare Addresses A and B concatenate to form a 32 bit word for comparison with a 32 bit content word. If a match occurs both the CMA and CMB lines will be active. During a write mode, the Compare Address is the data which will be written into the content word indicated by the Write Address In.
20	GROUND	V_{SS}	Ground
21	$\overline{\text{3-STATE ENABLE B}}$	$\overline{\text{TSEB}}$	A logic low indicates the D/WA is in the 3-state mode.
22	$\overline{\text{3-STATE ENABLE A}}$	$\overline{\text{TSEA}}$	A logic low indicates the D/WB is in the 3-state mode.
23, 24	$\overline{\text{WRITE PULSE A}}$ $\overline{\text{WRITE PULSE B}}$ RESPECTIVE	$\overline{\text{WPA}}$, $\overline{\text{WPB}}$	A logic low pulse used to write the Compare Address A or B information into the content word A or B of the CAM. $\overline{\text{WP}}$ A or B is only effective when $\overline{\text{TSEA}}$ or $\overline{\text{TSEB}}$ are enabled.
25	$\overline{\text{DUAL CAM/}}$ $\overline{\text{SINGLE CAM}}$	D/$\overline{\text{S}}$	This signal is used to configure the CAM from a dual read 16x64 CAM to a single read 32x32 CAM.
26-31	CAM DATA OUT B/ WRITE ADDRESS IN B	D/WB5-D/WB0	In dual read configuration 6 bits of data are output when the Compare Address B is matched with one of the 64 content words in the CAM. Each content word in the CAM is directly related to the Data Out number 000000_2 to 111111_2. During a write mode, Compare Address B is written into the word selected by the 6 bit Write Address B when $\overline{\text{TSEB}}$ is enabled and $\overline{\text{WPB}}$ occurs.
32	$\overline{\text{CAM MATCH B}}$	$\overline{\text{CMB}}$	A logic low during a read mode indicates a match has occurred between the Compare Address B and a content word within the CAM.
33	$\overline{\text{CAM MATCH A}}$	$\overline{\text{CMA}}$	A logic low during a read mode indicates a match has occurred between the Compare Address A and a content word within the CAM.
34-39	CAM DATA OUT A/WRITE ADDRESS IN A	D/WA5-D/WA0	In dual read configuration 6 bits of data are output when the Compare Address A is matched with one of the 64 content words in the CAM. Each content word in the CAM is directly related to the Data Out number 000000_2 to 111111_2. During a write mode, Compare Address A is written into the word selected by the 6 bit Write Address A when $\overline{\text{TSEA}}$ is enabled and $\overline{\text{WPA}}$ occurs.
40	GROUND	V_{SS}	Ground

See page 725 for ordering information.

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WD5869 Dynamic Shift Register

FEATURES

- DUAL 640 BIT
- ADDITIONAL TAPS AT 512 ON EACH REGISTER
- INTERNAL CLOCKING
- HIGH SPEED
- 3 STATE OUTPUT BUFFER

GENERAL DESCRIPTION

The WD5869 Dual 640 Bit Dynamic Shift Register is a monolithic MOS integrated circuit designed for use in computer display peripherals. The clocks and recirculate logic are internal to reduce system component count, and 3 state output buffers provide bus interface. The WD5869 is available in a 16 pin molded plastic package, or a 16 pin ceramic package.

APPLICATIONS

- CRT DISPLAYS
- COMPUTER PERIPHERALS
- CRYPTOGRAPHY

DUAL IN-LINE PACKAGE

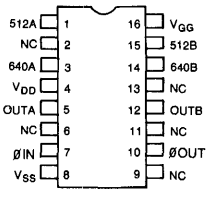

Figure 1
WD5869 PIN CONNECTIONS

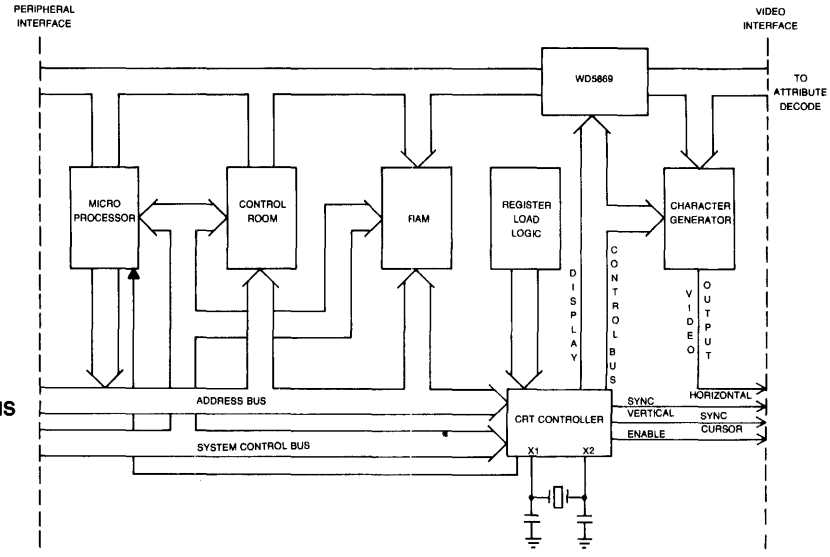

Figure 2 WD5869 TYPICAL APPLICATION BLOCK DIAGRAM

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Data and Clock Input Voltage and Supply Voltages with respect to VSS	+0.3V to −20V
Power Dissipation	800mW at TA = 25°C
Storage Temperature	−55°C to +125°C (Plastic Package) −65°C to +150°C (Ceramic Package)

TABLE 1 D.C. PARAMETERS

ELECTRICAL CHARACTERISTICS (DC)

TA = 0°C to + 50°C, V_{SS} = +5V ± 5%, V_{DD} = −5V + 5%, V_{GG} = −12V ± 5%

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
I_{DD}	POWER SUPPLY CURRENT		−50	mA	
	DATA INPUT LEVELS				
V_{IL}	Logical Low Level	V_{SS}−17.9	V_{SS}−4.2	V	
V_{IH}	Logical High Level	V_{SS}−1.7	V_{SS}+0.3	V	
I_{IL}	DATA INPUT LEAKAGE		10	μA	V_{IN} = −5V; All other Pins GND
C_{di}	DATA INPUT CAPACITANCE		10	pf	V_{IN} = 0V; f = 1MHZ, All other Pins GND
	CLOCK INPUT LEVELS				
V_{OH}	Logical High Level	V_{SS}−1.0	V_{SS}+0.3	V	
V_{OL}	Logical Low Level	V_{SS}−17.9	V_{SS}−14.5	V	
I_{CL}	CLOCK INPUT LEAKAGE		10	μA	V_O = −17.9V; All other Pins GND
C_{ci}	CLOCK INPUT CAPACITANCE		200	pf	V_O = 0V; f = 1MHZ, All other Pins GND
	DATA OUTPUT LEVELS				
V_{OH}	Logical High Level	2.4		V	I Source = −50mA
V_{OL}	Logical Low Level		V_{SS}−0.4	V	I Sink = 1.6 mA

TABLE 2 A.C. PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
Øf	CLOCK FREQUENCY	10	2000	KHz	Øtr = Øtf = 20 ns
Øpw in	CLOCK PULSE WIDTH, In	0.15	1.0	uS	Øtf + Øpw + Øtr ≤ 3.0 uS
Øpw out	CLOCK PULSE WIDTH, Out	1	1	Øpw in	
Ød	CLOCK PHASE DELAY TIME, from rising edge	10		ns	
Ød	CLOCK PHASE DELAY TIME, from falling edge	10		ns	
Øtr	CLOCK TRANSITION TIME, rising edge		1.0	us	Øtf + Øpw + Øtr ≤ 3.0 uS
Øtf	CLOCK TRANSITION TIME, falling edge		1.0	us	
tds	DATA INPUT SET-UP TIME	80		ns	
tdh	DATA INPUT HOLD TIME	40		ns	
tpdl	DATA OUTPUT PROPAGATION DELAY, to low level		200	ns	
tpdh	DATA OUTPUT PROPAGATION DELAY, to high level		200	ns	

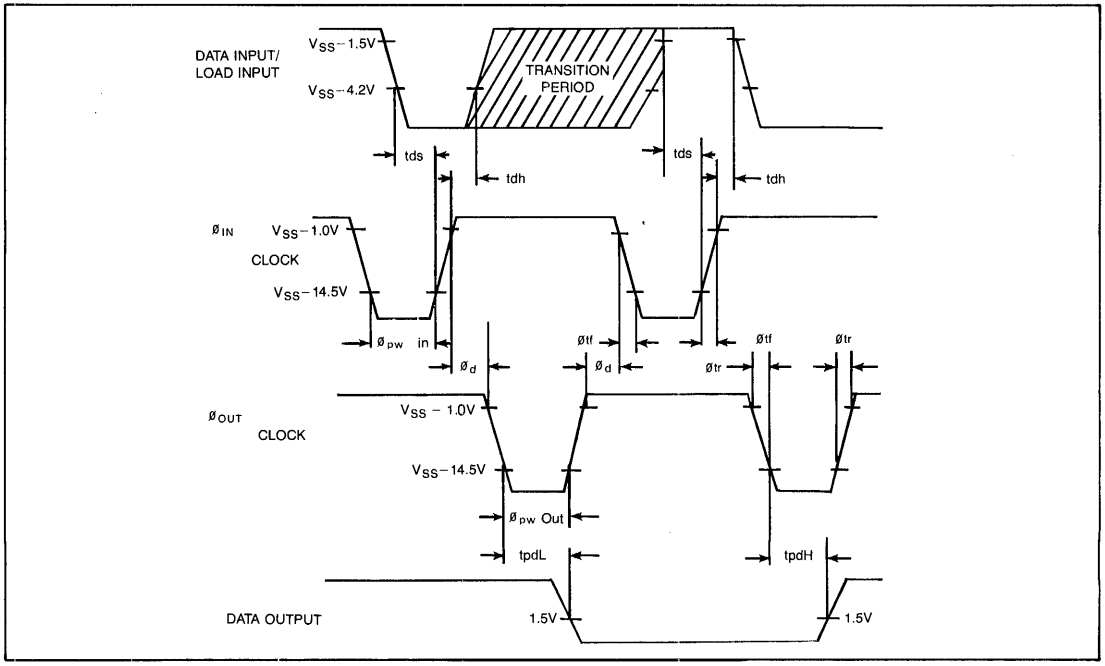

Figure 3 WD5869 TIMING DIAGRAM

See page 725 for ordering information.

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PRELIMINARY INFORMATION

WD74HC200 256 x 1 CMOS Static RAM

FEATURES

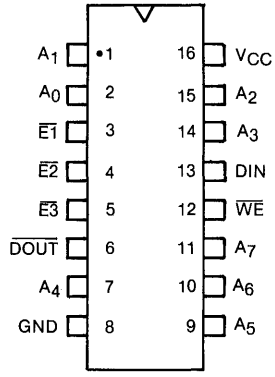
- PIN COMPATIBLE WITH 74LS200
- LOW POWER DISSIPATION .48 MW/BIT TYPICAL
- BATTERY-BACK UP/STANDBY MODE
- COMPLETELY STATIC
- SINGLE +5V SUPPLY
- FULLY TTL COMPATIBLE
- 35 ns TYPICAL ACCESS TIME

GENERAL DESCRIPTION

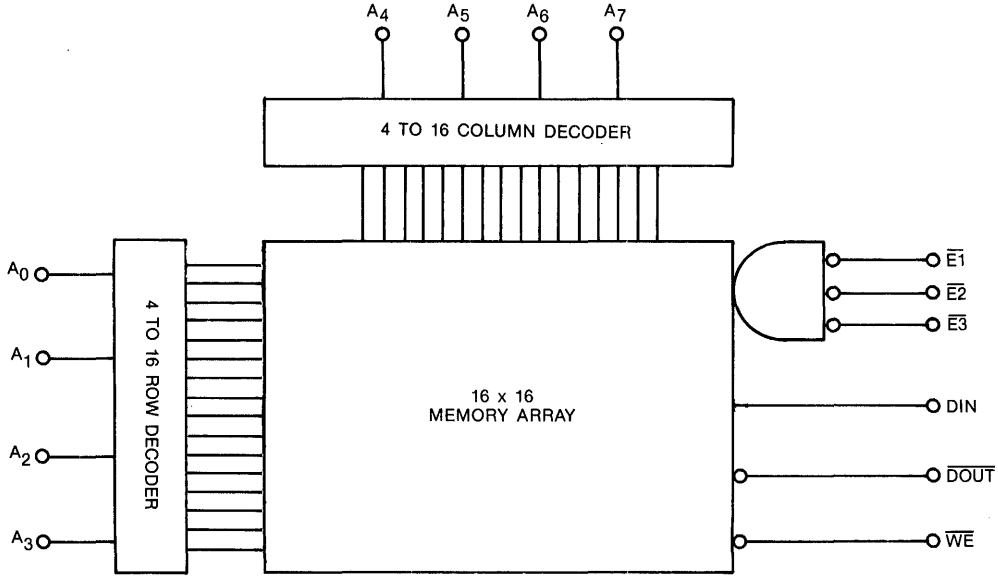
The WD74HC200 256x1 RAM is both pin and speed compatible to the SN74LS200 and AM27LS00. The device is fabricated in CMOS, offering a dramatic decrease in power dissipation and increased noise immunity. It is well suited for high-speed buffer memories in digital systems and bit-slice designs.

The memory is organized as a 256-word by 1-bit width with an 8 bit binary address field and separate data in and data output lines. It has 3 active low chip selects and a three-state output.

The WD74HC200 operates from a single +5 volt supply and is available in a dual-in-line plastic or ceramic package.



PIN DESIGNATION



BLOCK DIAGRAM

PIN NUMBER	SYMBOL	PIN NAME	FUNCTION
1, 2, 7, 9-11, 14-15	A_0-A_7	ADDRESS 0-7	8-bit address input used to select one of 256 memory bits.
3-5	$\overline{E1}$-$\overline{E3}$	$\overline{\text{ENABLE 1-3}}$	Three active-low inputs which must be at a logic zero to perform R/W functions.
6	$\overline{DOUT}$	$\overline{\text{DATA OUT}}$	Inverted data output from a selected memory address.
8	GND	GROUND	Ground
12	$\overline{WE}$	$\overline{\text{WRITE ENABLE}}$	Active low input used to write data into the device.
13	DIN	DATA IN	Data Input Line used in conjunction with $\overline{WE}$.
16	V_{CC}	V_{CC}	+5V ±5% power supply input.

FUNCTIONAL DESCRIPTION

When any of the Enable inputs are high ($\overline{E1}$, $\overline{E2}$, or $\overline{E3}$) the $\overline{DOUT}$ (Pin 6) line will remain in a high impedance state. During this condition, the $\overline{WE}$ (Pin 12) Write line is a "don't care" state and will not affect the high impedance state of $\overline{DOUT}$.

To perform a Write function, an address is placed on the address lines, with $\overline{WE}$ and all three Enable Lines at a Logic 0. Data is entered into the selected memory bit specified by the address inputs.

A read operation is performed in a similar fashion. Address Lines and the three Enable lines are made active, while $\overline{WE}$ is held high. The complement of the selected data bit then appears on the $\overline{DOUT}$ (Pin 6) line.

To retain data in a stand-by or battery back-up mode, the $\overline{E1}$, $\overline{E2}$ or $\overline{E3}$ line should be held at a Logic 1, while $\overline{WE}$ and the address lines are at a Logic 0. At nominal supply voltage, power consumption will be less than 1 milliampere D.C. in this configuration.

ABSOLUTE MAXIMUM RATINGS

V_{CC} With Respect to Ground ..... −0.3 to +7V
Voltage On Any Input With
Respect to Ground ..... −0.3 to +7V
Storage Temperature
Ceramic ..... −65°C to +150°C
Plastic ..... −55° to +125°C
Operating Temperature ..... 0°C to +75°C
Power Dissipation ..... 125 mW

NOTE: Maximum ratings indicate limits which permanent device damage may occur. Continuous operation at these ratings is not intended and should be limited to the DC electrical characteristics listed below.

DC ELECTRICAL CHARACTERISTICS

$T_A = 0°C$ to $75°C$, $V_{CC} = 5V + 5\%$

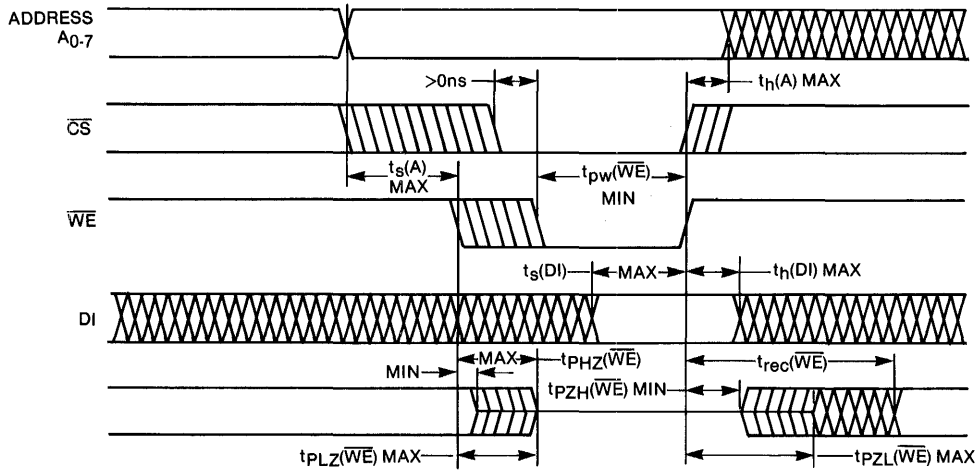
SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -2.6mA$
V_{OL}	Output Low Voltage		.45	V	$I_{OL} = 16.0mA$
I_{IL}	Input Low Current		.8	mA	
I_{IH}	Input High Current		20	μA	
I_{CC}	Power Supply Current		25	mA	All Outputs Open
I_{LK}	Output Leakage Current		30	μA	Three-state

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

V_{CC} = 5V ± 5%; C_L = 50pF

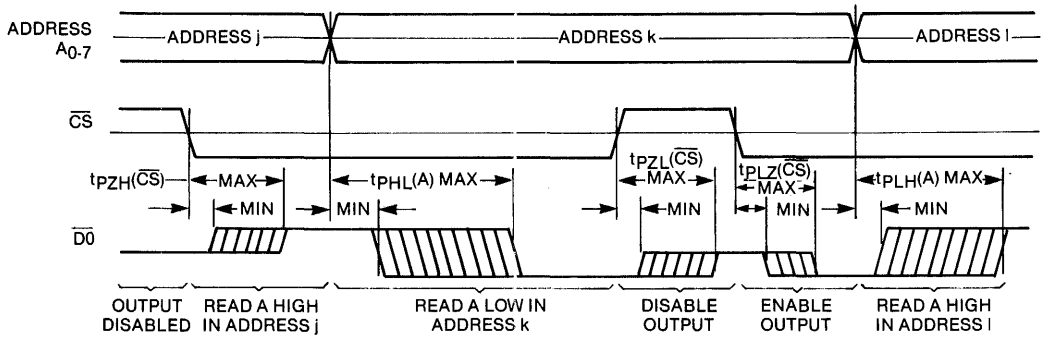
PARAMETERS	DESCRIPTION		T_A = 25°C TYP.	T_A = 0°C to 75°C MIN.	MAX.	UNITS
$t_{PLH}(A)$ $t_{PHL}(A)$	Delay from Address to Output	See Fig. 2	35	15	45	ns
$t_{PZH}(CS)$ $t_{PZL}(CS)$	Delay from Chip Select to Active Output and Correct Data	See Fig. 2	15	5	25	ns
$t_{PHZ}(CS)$ $t_{PLZ}(CS)$	Delay from Chip Select to Inactive Output	See Fig. 2	15	5	25	ns
t_{rec} (WE)	Delay from Write Enable (HIGH) to Correct Output Data	See Fig. 1	25		45	ns
$t_{PZH}(WE)$ $t_{PZL}(WE)$	Delay from Write Enable (HIGH) to Active Output	See Fig. 1		5		ns
$t_{PHZ}(WE)$ $t_{PLZ}(WE)$	Delay from Write Enable (LOW) to Inactive Output	See Fig. 1	20		30	ns
$t_s(A)$	Set-up Time Address	See Fig. 1	0	0		ns
$t_h(A)$	Hold Time Address		0	0		ns
$t_s(DI)$	Set-up Time Data Input	See Fig. 1	20	30		ns
$t_h(DI)$	Hold Time Data Input	See Fig. 1	0	0		ns
$t_{pw}(WE)$	Write Enable Pulse Width	See Fig. 1	20	30		ns

SWITCHING WAVEFORMS



Write Cycle Timing. The cycle is initiated by an address change. After t_S (A) max, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h (A) max must be allowed before the address may be changed again. The output will be floating while the write enable is LOW. Ordinarily, the chip select should be LOW during the entire write pulse.

Figure 1



Switching delays from address and chip select inputs to the data output. Disabled output is floating when "OFF," and represented by a single center line.

Figure 2

See page 725 for ordering information.

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PRELIMINARY

WD8206 Error Detection and Correction Unit

FEATURES

- Detects and Corrects All Single Bit Errors.
- Detects All Double Bit and Most Multiple Bit Errors
- 52 ns Maximum for Detection; 67 ns Maximum for Correction (16 Bit System)
- Expandable to Handle 80 Bit Memories
- Syndrome Outputs for Error Logging
- Separate Input and Output Busses — No Timing Strobes Required
- Supports Reads With and Without Correction, Writes, Partial (Byte) Writes, and Read-Modify-Writes
- HMOS Technology for Low Power
- 68 Pin Leadless JEDEC Package
- Single +5V Supply

GENERAL DESCRIPTION

The HMOS 8206 Error Detection and Correction Unit is a high-speed device that provides error detection and correction for memory systems (static and dynamic) requiring high reliability and performance. Each 8206 handles 8 or 16 data bits and up to 8 check bits. 8206's can be cascaded to provide correction and detection for up to 80 bits of data. Other 8206 features include the ability to handle byte writes, memory initialization, and error logging.

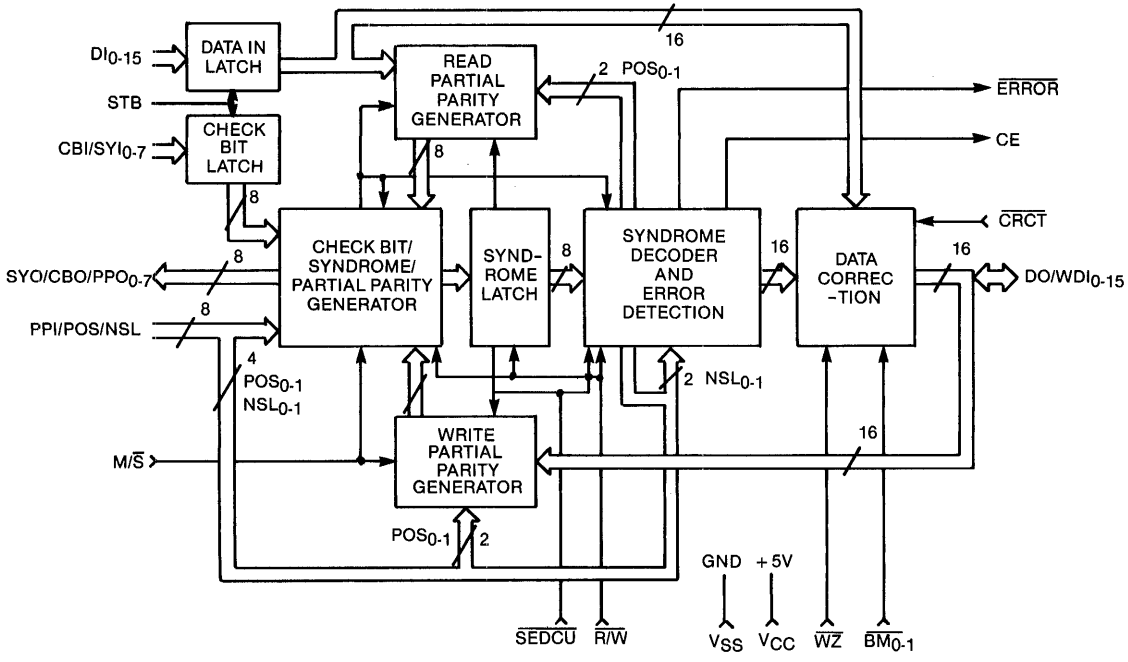


Figure 1. 8206 BLOCK DIAGRAM

Table 1. PIN DESCRIPTION

PIN NUMBER	SYMBOL	TYPE	NAME AND FUNCTION
1, 68-61, 59-53	DI_{0-15}	I	**Data In:** These inputs accept a 16 bit data word from RAM for error detection and/or correction.
5	CBI/SYI_0	I	**Check Bits In/Syndrome In:** In a single 8206 system, or in the master in a multi-8206 system, these inputs accept the check bits (5 to 8) from the RAM. In a single 8206 16 bit system, CBI_{0-5} are used. In slave 8206's these inputs accept the syndrome from the master.
6	CBI/SYI_1	I	
7	CBI/SYI_2	I	
8	CBI/SYI_3	I	
9	CBI/SYI_4	I	
10	CBI/SYI_5	I	
11	CBI/SYI_6	I	
12	CBI/SYI_7	I	
51	DO/WDI_0	I/O	**Data Out/Write Data In:** In a read cycle, data accepted by DI_{0-15} appears at these outputs corrected if CRCT is low, or uncorrected if CRCT is high. The BM inputs must be high to enable the output buffers during the read cycle. In a write cycle, data to be written into the RAM is accepted by these inputs for computing the write check bits. In a partial-write cycle, the byte not to be modified appears at either DO_{0-7} if BM_0 is high, or DO_{8-15} if BM_1 is high, for writing to the RAM. When WZ is active, it causes the 8206 to output all zeroes at DO_{0-15}, with the proper write check bits on CBO.
50	DO/WDI_1	I/O	
49	DO/WDI_2	I/O	
48	DO/WDI_3	I/O	
47	DO/WDI_4	I/O	
46	DO/WDI_5	I/O	
45	DO/WDI_6	I/O	
44	DO/WDI_7	I/O	
42	DO/WDI_8	I/O	
41	DO/WDI_9	I/O	
40	DO/WDI_{10}	I/O	
39	DO/WDI_{11}	I/O	
38	DO/WDI_{12}	I/O	
37	DO/WDI_{13}	I/O	
36	DO/WDI_{14}	I/O	
35	DO/WDI_{15}	I/O	
23	$SYO/CBO/PPO_0$	O	**Syndrome Out/Check Bits Out/Partial Parity Out:** In a single 8206 system, or in the master in a multi-8206 system, the syndrome appears at these outputs during a read. During a write, the write check bits appear. In slave 8206's the partial parity bits used by the master appear at these outputs. The syndrome is latched (during read-modify-writes) by R/W going low.
24	$SYO/CBO/PPO_1$	O	
25	$SYO/CBO/PPO_2$	O	
27	$SYO/CBO/PPO_3$	O	
28	$SYO/CBO/PPO_4$	O	
29	$SYO/CBO/PPO_5$	O	
30	$SYO/CBO/PPO_6$	O	
31	$SYO/CBO/PPO_7$	O	
13	PPI_0/POS_0	I	**Partial Parity In/Position:** In the master in a multi-8206 system, these inputs accept partial parity bits O and 1 from the slaves. In a slave 8206 these inputs inform it of its position within the system (1 to 4). Not used in a single 8206 system.
14	PPI_1/POS_1	I	
15	PPI_2/NSL_0	I	**Partial Parity In/Number of Slaves:** In the master in a multi-8206 system, these inputs accept partial parity bits 2 and 3 from the slaves. In a multi-8206 system these inputs are used in slave number 1 to tell it the total number of slaves in the system (1 to 4). Not used in other slaves or in a single 8206 system.
16	PPI_3/NSL_1	I	
17	PPI_4/CE	I/O	**Partial Parity In/Correctable Error:** In the master in a multi-8206 system this pin accepts partial parity bit 4. In slave number 1 only, or in a single 8206 system, this pin outputs the correctable error flag. CE is latched by R/W going low. Not used in other slaves.
18	PPI_5	I	**Partial Parity In:** In the master in a multi-8206 system these pins accept partial parity bits 5 to 7. The number of partial parity bits equals the number of check bits. Not used in single 8206 systems or in slaves.
19	PPI_6	I	
20	PPI_7	I	

Table 1. PIN DESCRIPTION (CONTINUED)

PIN NUMBER	SYMBOL	TYPE	NAME AND FUNCTION
22	ERROR	O	**Error:** This pin outputs the error flag in a single 8206 system or in the master of a multi-8206 system. It is latched by R/W going low. Not used in slaves.
52	CRCT	I	**Correct:** When low this pin causes data correction during a read or read-modify-write cycle. When high, it causes error correction to be disabled, although error checking is still enabled.
2	STB	I	**Strobe:** STB is an input control used to strobe data at the DI inputs and check-bits at the CBI/SYI inputs. The signal is active high to admit the inputs. The signals are latched by the high-to-low transition of STB.
33 32	BM_0 BM_1	I I	**Byte Marks:** When high, the Data Out pins are enabled for a read cycle. When low, the Data Out buffers are tristated for a write cycle. BM_0 controls DO_{0-7}, while BM_1 controls DO_{8-15}. In partial (bytes) writes, the byte mark input is low for the new byte to be written.
21	R/W	I	**Read/Write:** When high this pin causes the 8206 to perform detection and correction (if CRCT is low). When low, it causes the 8206 to generate check bits. On the high-to-low transition the syndrome is latched internally for read-modify-write cycles.
34	WZ	I	**Write Zero:** When low this input overrides the BM_{0-1} and R/W inputs to cause the 8206 to output all zeros at DO_{0-15} with the corresponding check bits at CBO_{0-7}. Used for memory initialization.
4	M/S	I	**Master/Slave:** Input tells the 8206 whether it is a master (high) or a slave (low).
3	SEDCU	I	**Single EDC Unit:** Input tells the master whether it is operating as a single 8206 (low) or as the master in a multi-8206 system (high). Not used in slaves.
60	V_{CC}	I	**Power Supply:** + 5V
26	V_{SS}	I	**Logic Ground**
43	V_{SS}	I	**Output Driver Ground**

FUNCTIONAL DESCRIPTION

The 8206 Error Detection and Correction Unit provides greater memory system reliability through its ability to detect and correct memory errors. It is a single chip device that can detect and correct all single bit errors and detect all double bit and some higher multiple bit errors. Some other odd multiple bit errors (e.g., 5 bits in error) are interpreted as single bit errors, and the CE flag is raised. While some even multiple bit errors (e.g., 4 bits in error) are interpreted as no error, most are detected as double bit errors. This error handling is a function of the number of check bits used by the 8206 (see Figure 2) and the specific Hamming code used. Errors in check bits are not distinguished from errors in a word.

A single 8206 handles 8 or 16 bits of data, and up to 5 8206's can be cascaded in order to handle data paths of 80 bits. For a single 8206 8 bit system, the DI_{8-15}, DO/WDI_{8-15} and BM_1 inputs are grounded. See the Multi-Chip systems section for information on 24-80 bit systems.

The 8206 has a "flow through" architecture. It supports two kinds of error correction architecture: 1) Flow-through, or correct-always; and 2) Parallel, or check-only. There are two separate 16-pin busses, one to accept data from the RAM (DI) and the other to deliver corrected data to the system bus (DO/WDI). The logic is entirely combinatorial during a read cycle. This is in contrast to an architecture with only one bus, with bidirectional bus drivers that must first read the data and then be turned around to output the corrected data. The latter architecture typically requires additional hardware (latches and/or transceivers) and may be slower in a system due to timing skews of control signals.

DATA WORD BITS	CHECK BITS
8	5
16	6
24	6
32	7
40	7
48	8
56	8
64	8
72	8
80	8

Figure 2: NUMBER OF CHECK BITS USED BY 8206

READ CYCLE

With the R/W pin high, data is received from the RAM outputs into the DI pins where it is optionally latched by the STB signal. Check bits are generated from the data bits and compared to the check bits read from the RAM into the CBI pins. If an error is detected the ERROR flag is activated and the correctable error flag (CE) is used to inform the system whether the error was correctable or not. With the BM inputs high, the word appears corrected at the DO pins if the error was correctable, or unmodified if the error was uncorrectable.

If more than one 8206 is being used, then the check bits are read by the master. The slaves generate a partial parity output (PPO) and pass it to the master. The master 8206 then generates and returns the syndrome to the slaves (SYO) for correction of the data.

The 8206 may alternatively be used in a "check-only" mode with the CRCT pin left high. With the correction facility turned off, the propagation delay from memory outputs to 8206 outputs is significantly shortened. In this mode the 8206 issues an ERROR flag to the CPU, which can then perform one of several options: lengthen the current cycle for correction, restart the instruction, perform a diagnostic routine, etc.

A syndrome word, five to eight bits in length and containing all necessary information about the existence and location of an error, is made available to the system at the $SYO_{0\text{-}7}$ pins. Error logging may be accomplished by latching the syndrome and the memory address of the word in error.

WRITE CYCLE

For a full write, in which an entire word is written to memory, the data is written directly to the RAM, bypassing the 8206. The same data enters the 8206 through the WDI pins where check bits are generated. The Byte Mark inputs must be low to tristate the DO drivers. The check bits, 5 to 8 in number, are then written to the RAM through the CBO pins for storage along with the data word. In a multi-chip system, the master writes the check bits using partial parity information from the slaves.

In a partial write, part of the data word is overwritten, and part is retained in memory. This is accomplished by performing a read-modify-write cycle. The complete old word is read into the 8206 and corrected, with the syndrome internally latched by R/W going low. Only that part of the word not to be modified is output onto the DO pins, as controlled by the Byte Mark inputs. That portion of the word to be overwritten is supplied by the system bus. The 8206 then calculates check bits for the new word, using the byte from the previous read and the new byte from the system bus, and writes them to the memory.

READ-MODIFY-WRITE CYCLES

Upon detection of an error the 8206 may be used to correct the bit in error in memory. This reduces the probability of getting multiple-bit errors in subsequent read cycles. This correction is handled by executing read-modify-write cycles.

The read-modify-write cycle is controlled by the R/W input. After (during) the read cycle, the system dynamic RAM controller or CPU examines the 8206 ERROR and CE outputs to determine if a correctable error occurred. If it did, the dynamic RAM controller or CPU forces R/W low, telling the 8206 to latch the generated syndrome and drive the corrected check bits onto the CBO outputs. The corrected data is available on the DO pins. The DRAM controller then writes the corrected data and corresponding check bits into memory.

The 8206 may be used to perform read-modify-writes in one or two RAM cycles. If it is done in two cycles, the 8206 latches are used to hold the data and check bits from the read cycle to be used in the following write cycle. The WD8207 Advanced Dynamic RAM controller allows read-modify-write cycles in one memory cycle. See the System Environment section.

INITIALIZATION

A memory system operating with ECC requires some form of initialization at system power-up in order to set valid data and check bit information in memory. The 8206 supports memory initialization by the write zero function. By activating the WZ pin, the 8206 will write a data pattern of zeros and the associated check bits in the current write cycle. By thus writing to all memory at power-up, a controller can set memory to valid data and check bits. Massive memory failure, as signified by both data and check bits all ones or zeros, will be detected as an uncorrectable error.

MULTI-CHIP SYSTEMS

A single 8206 handles 8 or 16 bits of data and 5 or 6 check bits, respectively. Up to 5 8206's can be cascaded for 80 bit memories with 8 check bits.

When cascaded, one 8206 operates as a master, and all others as slaves. As an example, during a read cycle in a 32 bit system with one master and one

slave, the slave calculates parity on its portion of the word — "partial parity" — and presents it to the master through the PPO pins. The master combines the partial parity from the slave with the parity it calculated from its own portion of the word to generate the syndrome. The syndrome is then returned by the master to the slave for error correction. In systems with more than one slave the above description continues to apply, except that the partial parity outputs of the slaves must be XOR'd externally. Figure 3 shows the necessary external logic for multi-chip systems. Write and read-modify-write cycles are carried out analogously. See the System Operation section for multi-chip wiring diagrams.

There are several pins used to define whether the 8206 will operate as a master or a slave. Tables 2 and 3 illustrate how these pins are tied.

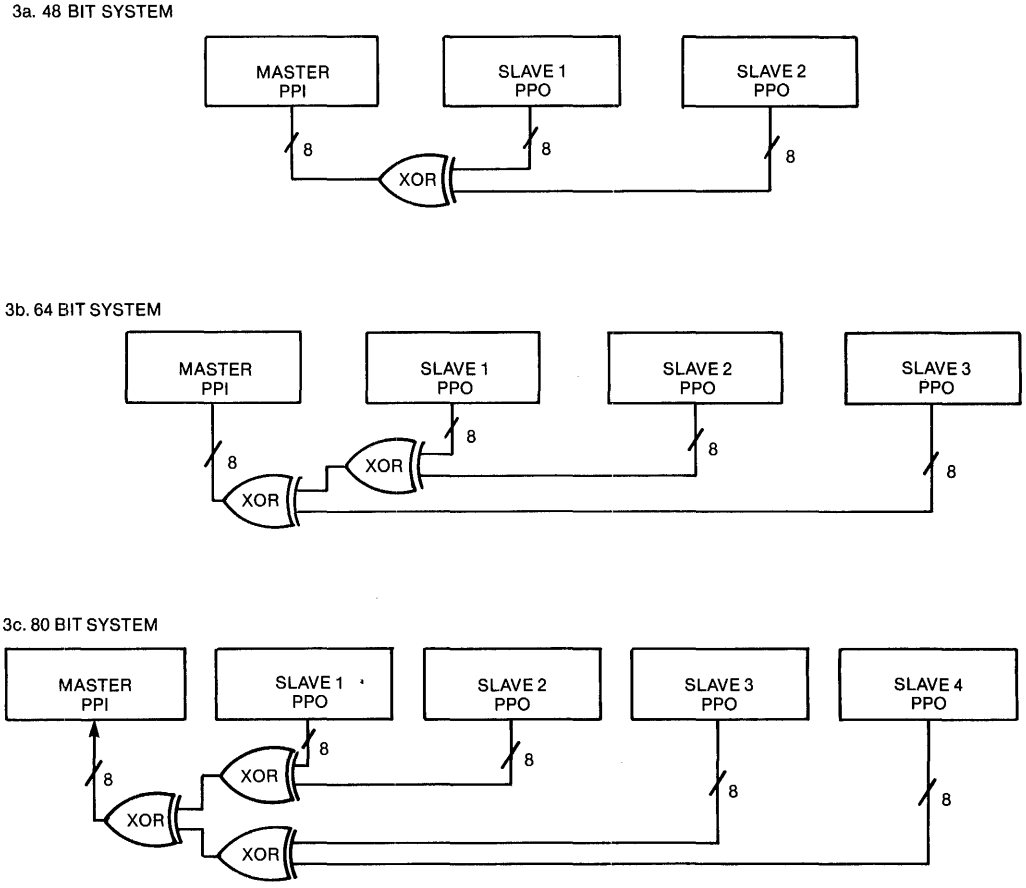


Figure 3. EXTERNAL LOGIC FOR MULTI-CHIP SYSTEMS

Table 2. MASTER/SLAVE PIN ASSIGNMENTS

PIN NO.	PIN NAME	MASTER	SLAVE 1	SLAVE 2	SLAVE 3	SLAVE 4
4	M/S	+5V	Gnd	Gnd	Gnd	Gnd
3	SEDCU	+5V	+5V	+5V	+5V	+5V
13	PPI_0/POS_0	PPI	Gnd	+5V	Gnd	+5V
14	PPI_1/POS_1	PPI	Gnd	Gnd	+5V	+5V
15	PPI_2/NSL_0	PPI	*	+5V	+5V	+5V
16	PPI_3/NSL_1	PPI	*	+5V	+5V	+5V

* See Table 3.

NOTE:
Pins 13, 14, 15, 16 have internal pull-up resistors and may be left as N.C. where specified as connecting to +5V.

Table 3. NSL PIN ASSIGNMENTS FOR SLAVE 1

	NUMBER OF SLAVES			
PIN	1	2	3	4
PPI_2/NSL_0	Gnd	+5V	Gnd	+5V
PPI_3/NSL_1	Gnd	Gnd	+5V	+5V

The timing specifications for multi-chip systems must be calculated to take account of the external XOR gating in 3, 4, and 5-chip systems. Let tXOR be the delay for a single external TTL XOR gate. Then the following equations show how to calculate the relevant timing parameters for 2-chip (n = 0), 3-chip (n = 1), 4-chip (n = 2), and 5-chip (n = 2) systems:

Data-in to corrected data-out (read cycle) =
TDVSV + TPVSV + TSVQV + ntXOR

Data-in to error flag (read cycle) =
TDVSV + TPVEV + ntXOR

Data-in to correctable error flag (read cycle) =
TDVSV + TPVSV + TSVCV + ntXOR

Write data to check-bits valid (full write cycle) =
TQVQV + TPVSV + ntXOR

Data-in to check-bits valid (read-mod-write cycle) =
TDVSV + TPVSV + TSVQV + TQVQV + TPVSV + 2ntXOR

Data-in to check-bits valid (non-correcting read-modify-write cycle) =
TDVQU + TQVQV + TPVSV + ntXOR

HAMMING CODE

The 8206 uses a modified Hamming code which was optimized for multi-chip EDCU systems. The code is such that partial parity is computed by all 8206's in parallel. No 8206 requires more time for propagation through logic levels than any other one, and hence no one device becomes a bottleneck in the parity operation. However, one or two levels of external TTL XOR gates are required in systems with three to five chips. The code appears in Table 4. The check bits are derived from the table by XORing or XNORing together the bits indicated by 'X's in each row corresponding to a check bit. For example, check bit 0 in the MASTER for data word 1000110101101011 will be "0." It should be noted that the 8206 will detect the gross-error condition of all lows or all highs.

Error correction is accomplished by identifying the bad bit and inverting it. Table 4 can also be used as an error syndrome table by replacing the 'X's with '1's. Each column then represents a different syndrome word, and by locating the column corresponding to a particular syndrome the bit to be corrected may be identified. If the syndrome cannot be located then the error cannot be corrected. For example, if the syndrome word is 00110111, the bit to be corrected is bit 5 in the slave one data word (bit 21).

The syndrome decoding is also summarized in Table 5, which can be used for error logging. By finding the appropriate syndrome word (starting with bit zero, the least significant bit), the result is either: 1) no error; 2) an identified (correctable) single bit error; 3) a double bit error; or 4) a multi-bit uncorrectable error.

Table 4. MODIFIED HAMMING CODE CHECK BIT GENERATION

Check bits are generated by XOR'ing (except for the CB0 and CB1 data bits, which are XNOR'ed in the Master) the data bits in the rows corresponding to the check bits. Note there are 6 check bits in a 16-bit system, 7 in a 32-bit system, and 8 in 48-or-more-bit systems.

BYTE NUMBER	0								1								OPERATION
BIT NUMBER	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
CB0 =	X	X	—	X	—	X	X	—	X	—	—	X	—	X	—	—	XNOR
CB1 =	X	—	X	—	—	X	—	X	—	X	X	—	X	—	X	—	XNOR
CHECK CB2 =	—	X	X	—	X	—	X	X	—	—	X	—	X	—	—	X	XOR
CB3 =	X	X	X	X	X	—	—	—	X	X	X	—	—	—	—	—	XOR
BITS CB4 =	—	—	—	X	X	X	X	X	—	—	—	—	—	X	X	X	XOR
CB5 =	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	XOR
CB6 =	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XOR
CB7 =	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XOR
DATA BITS	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	
	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	

16 BIT OR MASTER

	2								3								OPERATION
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
	—	X	X	X	—	X	X	—	—	X	X	—	—	X	—	—	XOR
	X	X	X	—	—	X	—	X	X	X	—	—	—	—	—	X	XOR
	—	X	X	X	—	X	X	X	—	—	X	X	—	—	—	—	XOR
	X	X	—	—	X	—	X	X	X	—	—	X	X	—	—	—	XOR
	X	X	—	—	X	X	X	X	—	—	—	—	X	—	X	—	XOR
	—	—	—	X	X	X	X	X	—	—	—	—	—	X	X	X	XOR
	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	XOR
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XOR
	1	1	1	1	2	2	2	2	2	2	2	2	2	2	3	3	
	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	

SLAVE #1

BYTE NUMBER	4								5								6								7								8								9								OPERATION
BIT NUMBER	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
CB0 =	X	X	—	X	—	X	X	—	X	—	—	X	—	X	—	—	X	—	X	X	—	—	X	—	—	X	X	X	—	X	X	—	—	X	X	—	—	X	—	—	XOR
CB1 =	X	—	X	—	—	X	—	X	—	X	X	—	X	—	X	—	—	X	X	—	—	—	X	X	X	X	X	—	—	X	X	X	—	X	X	—	X	—	—	—	—	X	X	—	—	—	—	—	XOR
CHECK CB2 =	—	X	X	—	X	—	X	X	—	—	X	—	X	—	—	X	—	X	X	X	—	X	X	—	—	X	X	—	—	X	—	—	X	—	—	X	X	—	X	—	—	X	X	—	X	—	X	—	XOR
CB3 =	X	X	X	X	X	—	—	—	X	X	X	—	—	—	—	—	X	—	X	—	—	X	X	—	X	X	—	—	X	X	X	—	—	X	X	X	—	—	X	—	X	X	—	—	X	—	—	—	XOR
BITS CB4 =	—	—	—	X	X	X	X	X	—	—	—	—	—	X	X	X	—	—	—	X	X	X	X	X	—	—	—	X	X	X	—	X	—	X	X	X	—	—	—	X	X	X	—	—	—	X	—	—	XOR
CB5 =	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	X	—	—	—	X	X	X	X	—	—	—	X	—	—	—	X	XOR
CB6 =	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	X	X	—	—	X	X	X	X	—	—	—	—	X	—	X	—	XOR
CB7 =	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	XOR
DATA BITS	3	3	3	3	3	3	3	3	4	4	4	4	4	4	4	4	4	4	5	5	5	5	5	5	5	5	5	5	6	6	6	6	6	6	6	6	6	6	6	7	7	7	7	7	7	7	7	7	
	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	

SLAVE #2 | SLAVE #3 | SLAVE #4

Table 5. SYNDROME DECODING

Syndrome Bits 7	6	5	4	0 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 2 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 3 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1
0	0	0	0	N CB0 CB1 D CB2 D D 18 CB3 D D 0 D 1 2 D
0	0	0	1	CB4 D D 5 D 6 7 D D 3 16 D 4 D D 17
0	0	1	0	CB5 D D 11 D 19 12 D D 8 9 D 10 D D 67
0	0	1	1	D 13 14 D 15 D D 21 20 D D 66 D 22 23 D
0	1	0	0	CB6 D D 25 D 26 49 D D 48 24 D 27 D D 50
0	1	0	1	D 52 55 D 51 D D 70 28 D D 65 D 53 54 D
0	1	1	0	D 29 31 D 64 D D 69 68 D D 32 D 33 34 D
0	1	1	1	30 D D 37 D 38 39 D D 35 71 D 36 D D U
1	0	0	0	CB7 D D 43 D 77 44 D D 40 41 D 42 D D U
1	0	0	1	D 45 46 D 47 D D 74 72 D D U D 73 U D
1	0	1	0	D 59 75 D 79 D D 58 60 D D 56 D U 57 D
1	0	1	1	63 D D 62 D U U D D U U D 61 D D U
1	1	0	0	D U U D U D D U 76 D D U D U U D
1	1	0	1	78 D D U D U U D D U U D D D U
1	1	1	0	U D D U D U U D D U U D U D U
1	1	1	1	D U U D U D D U U D D U D U U D

N = No Error
CBX = Error in Check Bit X
X = Error in Data Bit X
D = Double Bit Error
U = Uncorrectable Multi-Bit Error

SYSTEM ENVIRONMENT

The 8206 interface to a typical 32 bit memory system is illustrated in Figure 4. For larger systems, the partial parity bits from slaves two to four must be XOR'ed externally, which calls for one level of XOR gating for three 8206's and two levels for four or five 8206's.

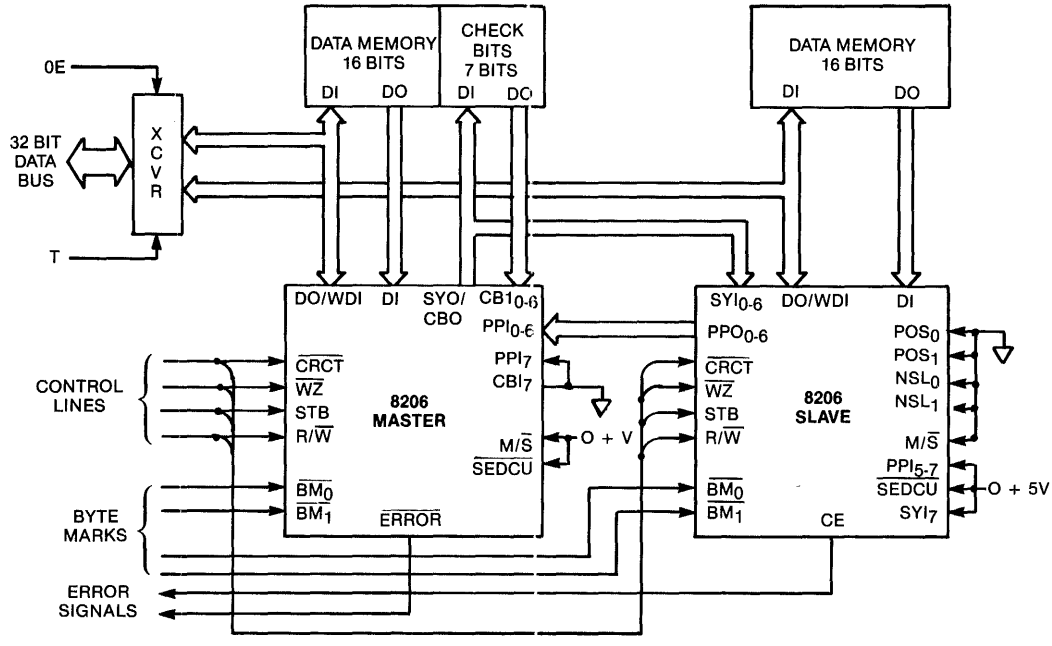


Figure 4. 32-BIT 8206 SYSTEM INTERFACE

The 8206 is designed for direct connection to the WD8207 Advanced Dynamic RAM Controller, due to be sampled in the first quarter of 1983. The 8207 has the ability to perform dual port memory control and Figure 5 illustrates a highly integrated dual port RAM implementation using the 8206 and 8207. The 8206/8207 combination permits such features as automatic scrubbing (correcting errors in memory during refresh), extending RAS and CAS timings for Read-Modify-Writes in single memory cycles, and automatic memory initialization upon reset. Together these two chips provide a complete dual-port, error-corrected dynamic RAM subsystem.

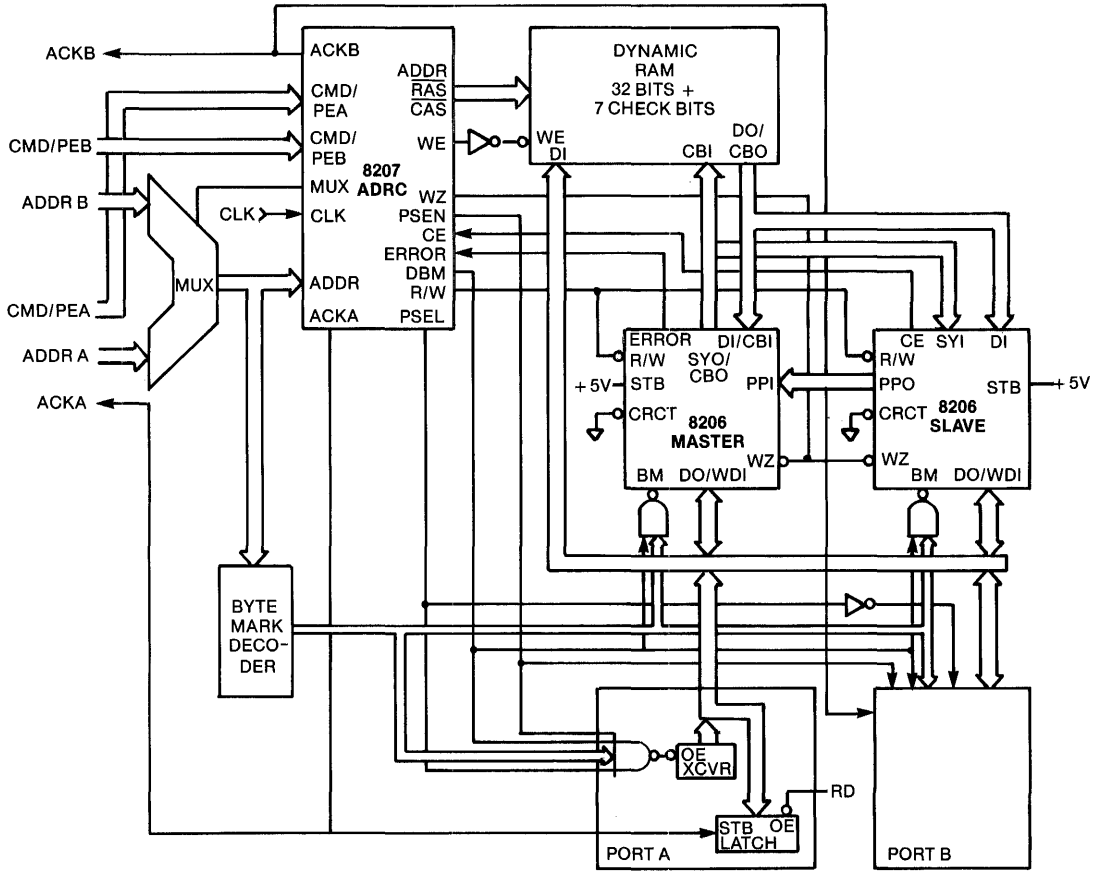


Figure 5. DUAL PORT RAM SUBSYSTEM WITH 8206/8207 (32-BIT BUS)

MEMORY BOARD TESTING

The 8206 lends itself to straightforward memory board testing with a minimum of hardware overhead. The following is a description of four common test modes and their implementation.

Mode 0 — Read and write with error correction.
Implementation: This mode is the normal 8206 operating mode.

Mode 1 — Read and write data with error correction disabled to allow test of data memory.
Implementation: This mode is performed with CRCT deactivated.

Mode 2 — Read and write check bits with error correction disabled to allow test of check bits memory.
Implementation: Any pattern may be written into the check bits memory by judiciously choosing the proper data word to generate the desired check bits, through the use of the 8206 Hamming code. To read out the check bits it is first necessary to fill the data memory with all zeros, which may be done by activating WZ and incrementing memory addresses with WE to the check bits memory held inactive, and then performing ordinary reads. The check bits will then appear directly at the SYO outputs, with bits CB0 and CB1 inverted.

Mode 3 — Write data, without altering or writing check bits, to allow the storage of bit combinations to cause error correction and detection.
Implementation: This mode is implemented by writing the desired word to memory with WE to the check bits array held inactive.

PACKAGE

The 8206 is packaged in a 68-pin, leadless JEDEC type A hermetic chip carrier. Figure 6 illustrates the package, and Figure 7 is the pinout.

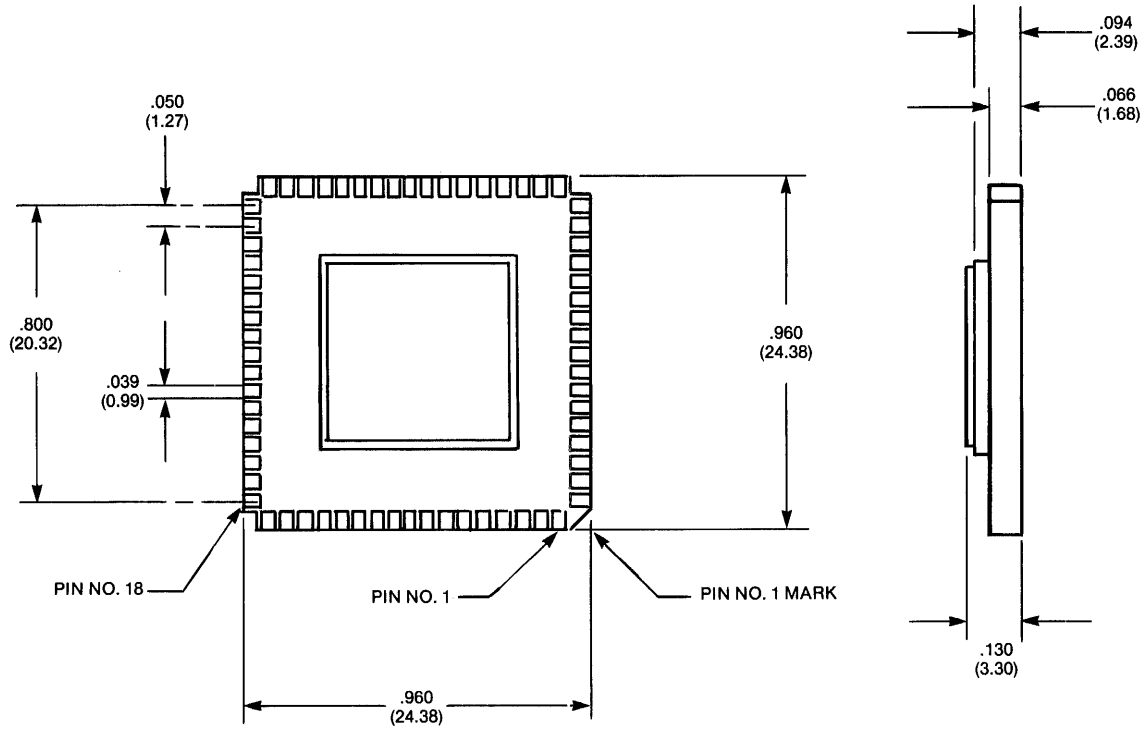


Figure 6. 8206 JEDEC TYPE A PACKAGE

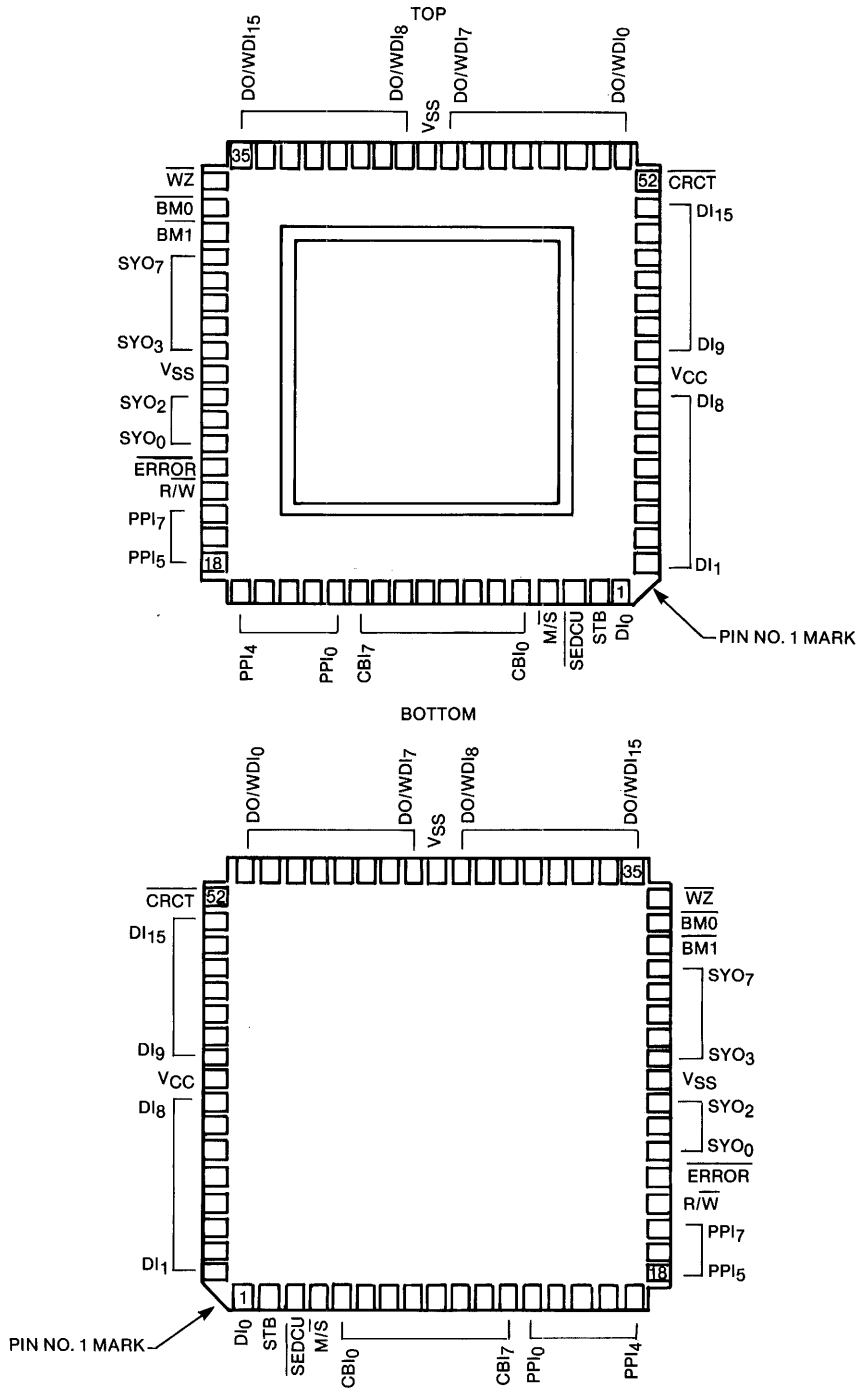


Figure 7. 8206 PINOUT DIAGRAM

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin
With Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 2.5 Watts

***NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

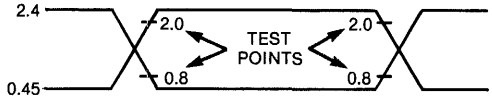
D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V ± 10%, V_{SS} = GND)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{CC}	Power Supply Current				
	— Single 8206 or Slave #1		270	mA	
	— Master in Multi-Chip or Slaves #2, 3, 4		230	mA	
V_{IL}[1]	Input Low Voltage	−0.5	0.8	V	
V_{IH}[1]	Input High Voltage	2.0	V_{CC} + 0.5V	V	
V_{OL}	Output Low Voltage				
	— DO		0.4	V	I_{OL} = 8mA
	— All Others		0.4	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage				
	— DO, CBO	2.6		V	I_{OH} = −2mA
	— All Other Outputs	2.4		V	I_{OH} = 0.4mA
I_{LO}	I/O Leakage Current				
	— PPI_4/CE		± 20	μA	0.45V ≤ $V_{I/O}$ ≤ V_{CC}
	— DO/WDI_{0-15}		± 10	μA	
I_{LI}	Input Leakage Current				
	— $PPI_{0-3, 5-7}$, CBI_{6-7}, SEDCU[2]		± 20	μA	0V ≤ V_{IN} ≤ V_{CC}
	— All Other Input Only Pins		± 10	μA	

NOTES:

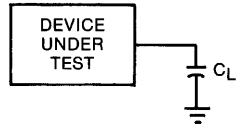
1. SEDCU (pin 3) and M/S (pin 4) are device strapping options and should be tied to V_{CC} or GND. V_{IH} min = V_{CC} − 0.5V and V_{IL} max = 0.5V.
2. PPI_{0-7} (pins 13-20) and CBI_{6-7} (pins 11, 12) have internal pull-up resistors and if left unconnected will be pulled to V_{CC}.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC 1 and 0.45V FOR A LOGIC 0. TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC 1 AND 0.8V FOR A LOGIC 0.

A.C. TESTING LOAD CIRCUIT



C_L INCLUDES JIG CAPACITANCE

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 10%, V_{SS} = 0V, C_L = 100pF; all times are in nsec.)

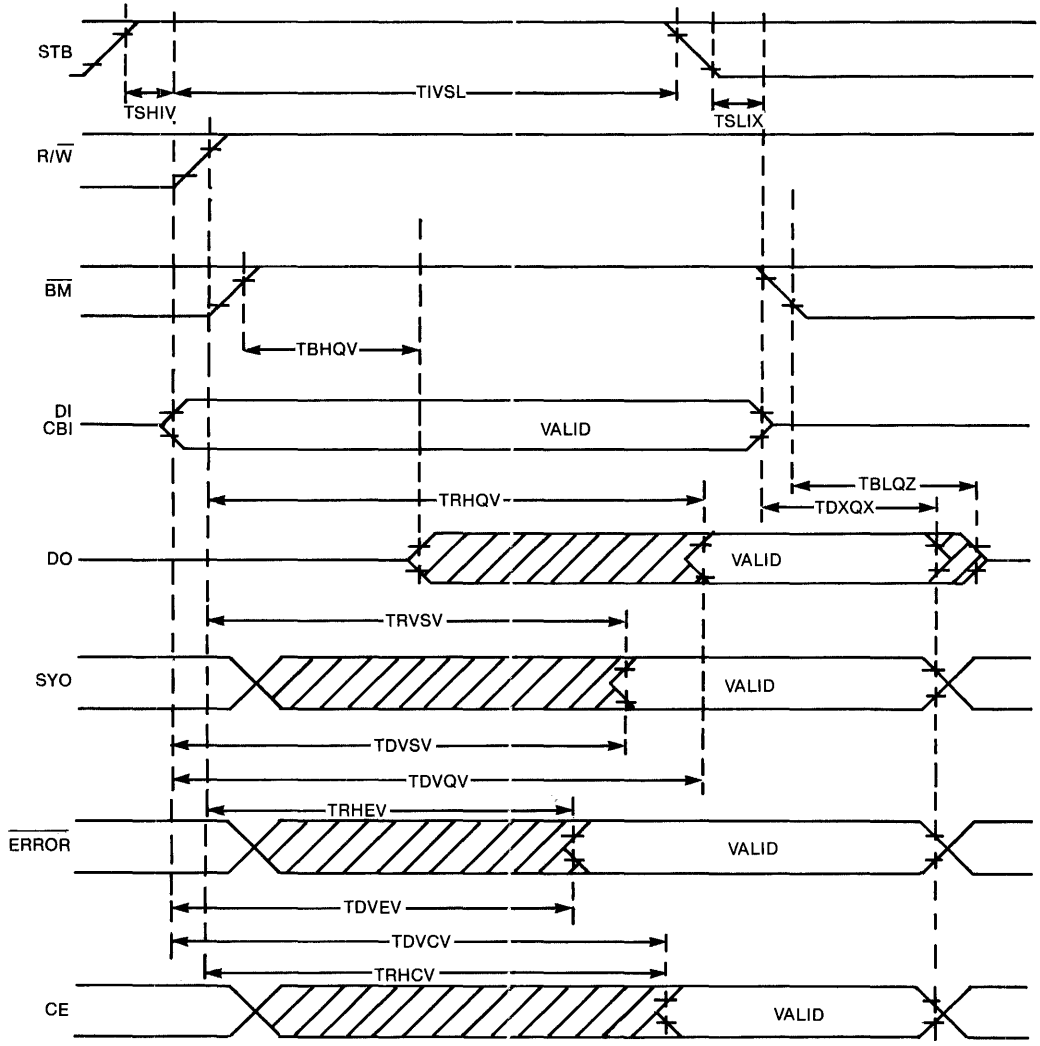
SYMBOL	PARAMETER	8206		8206-8		NOTES
		MIN.	MAX.	MIN.	MAX.	
TRHEV	ERROR Valid from R/W↑		25		34	
TRHCV	CE Valid from R/W↑ (Single 8206)		44		59	
TRHQV	Corrected Data Valid from R/W↑		54		66	1
TRVSV	SYO/CBO/PPO Valid from R/W		42		56	1
TDVEV	ERROR Valid from Data/Check Bits In		52		70	
TDVCV	CE Valid from Data/Check Bits In		70		94	
TDVQV	Corrected Data Valid from Data/Check Bits In		67		90	
TDVSV	SYO/PPO Valid from Data/Check Bits In		55		74	
TBHQV	Corrected Data Access Time		37		43	
TDXQX	Hold Time from Data/Check Bits In	0		0		1
TBLQZ	Corrected Data Float Delay	0	28	0	38	1
TSHIV	STB High to Data/Check Bits in Valid	30		40		2
TIVSL	Data/Check Bits In to STB↓ Set-up	5		5		
TSLIX	Data/Check Bits In from STB↓ Hold	25		30		
TPVEV	ERROR Valid from Partial Parity In		30		40	
TPVQV	Corrected Data (Master) from Partial Parity In		61		76	1
TPVSV	Syndrome/Check Bits Out from Partial Parity In		43		51	1
TSVQV	Corrected Data (Slave) Valid from Syndrome		51		69	
TSVCV	CE Valid from Syndrome (Slave number 1)		48		65	
TQVQV	Check Bits/Partial Parity Out from Write Data In		64		80	1
TRHSX	Check Bits/Partial Parity Out from R/W, WZ Hold	0		0		1
TRLSX	Syndrome Out from R/W Hold	0		0		
TQXQX	Hold Time from Write Data In	0		0		1
TSVRL	Syndrome Out to R/W↓ Set-up	17		22		
TDVRL	Data/Check Bits In to R/W Set-up	39		46		1
TDVQU	Uncorrected Data Out from Data In		32		43	
TTVQV	Corrected Data Out from CRCT↓		30		40	
TWLQL	WZ↓ to Zero Out		30		40	
TWHQX	Zero Out from WZ↑ Hold	0		0		

NOTES:

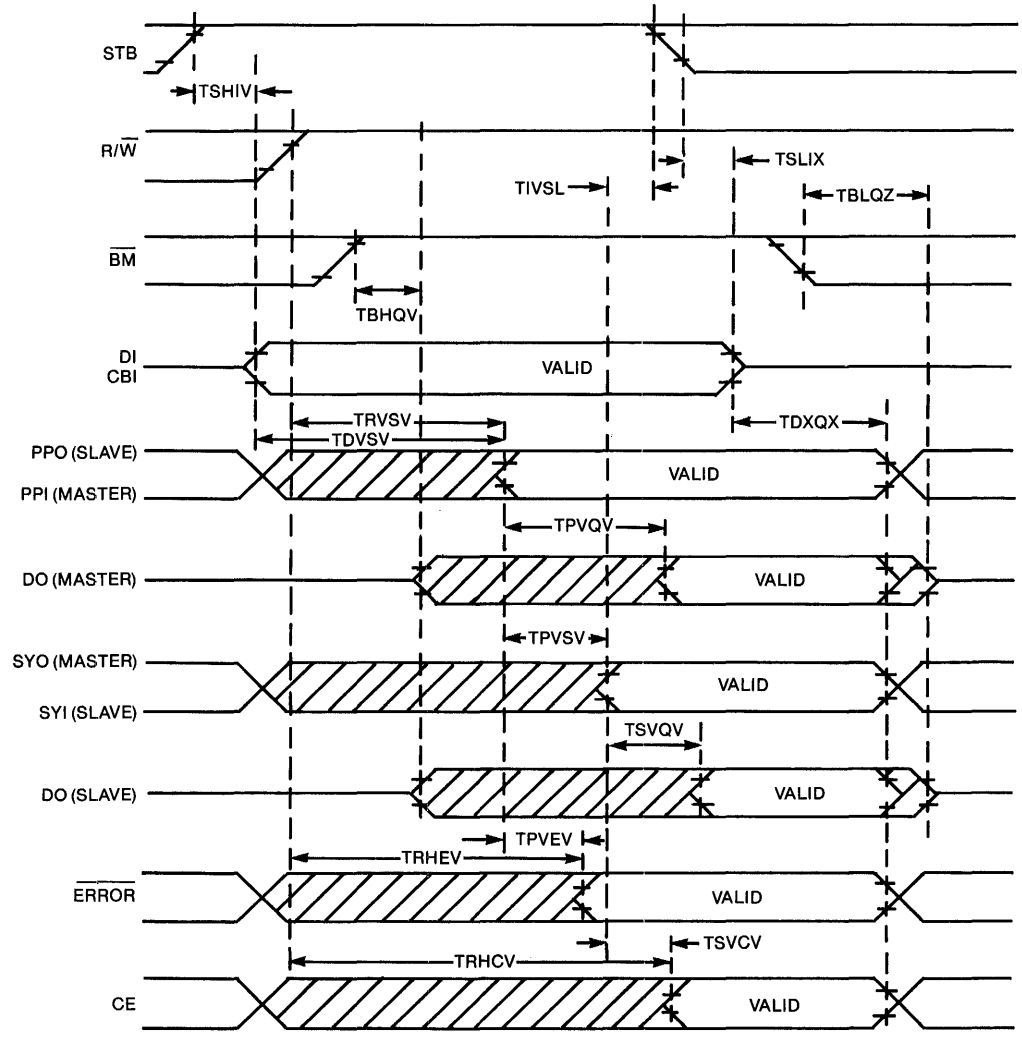
1. A.C. Test Levels for CBO and DO are 2.4V and 0.8V.
2. T_{SHIV} is required to guarantee output delay timings: T_{DVEV}, T_{DVCV}, T_{DVSV}. T_{SHIV} + T_{IVSL} guarantees a min STB pulse width of 35 ns (45 ns for the 8206-8).

WAVEFORMS

READ — 16 BIT ONLY

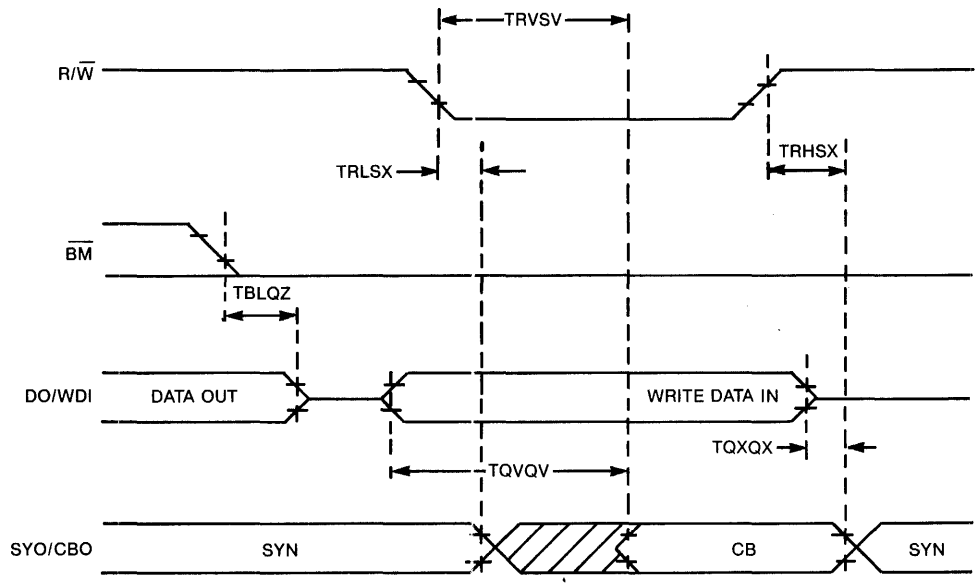


READ — MASTER/SLAVE

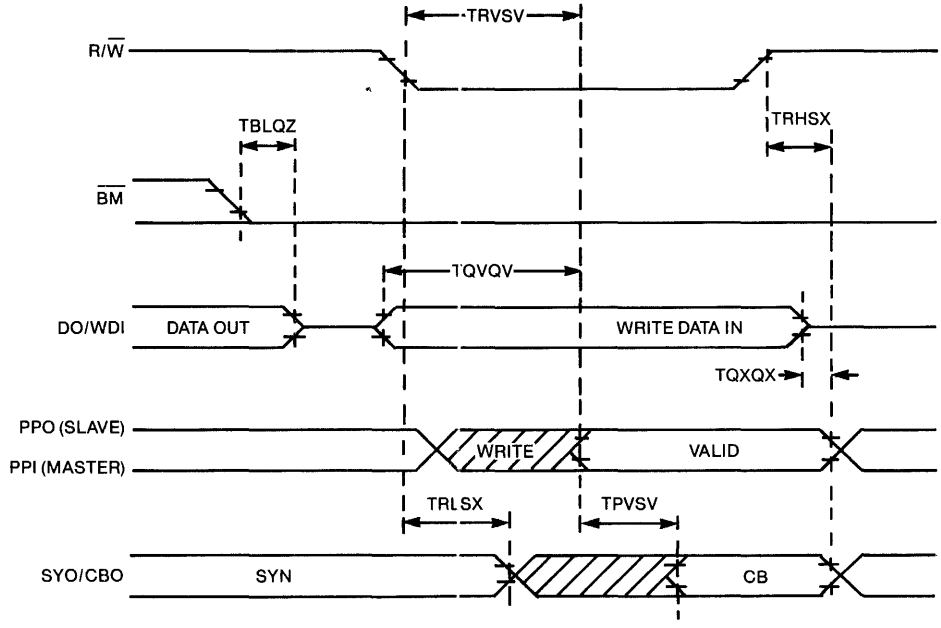


WAVEFORMS (Continued)

FULL WRITE — 16 BIT ONLY

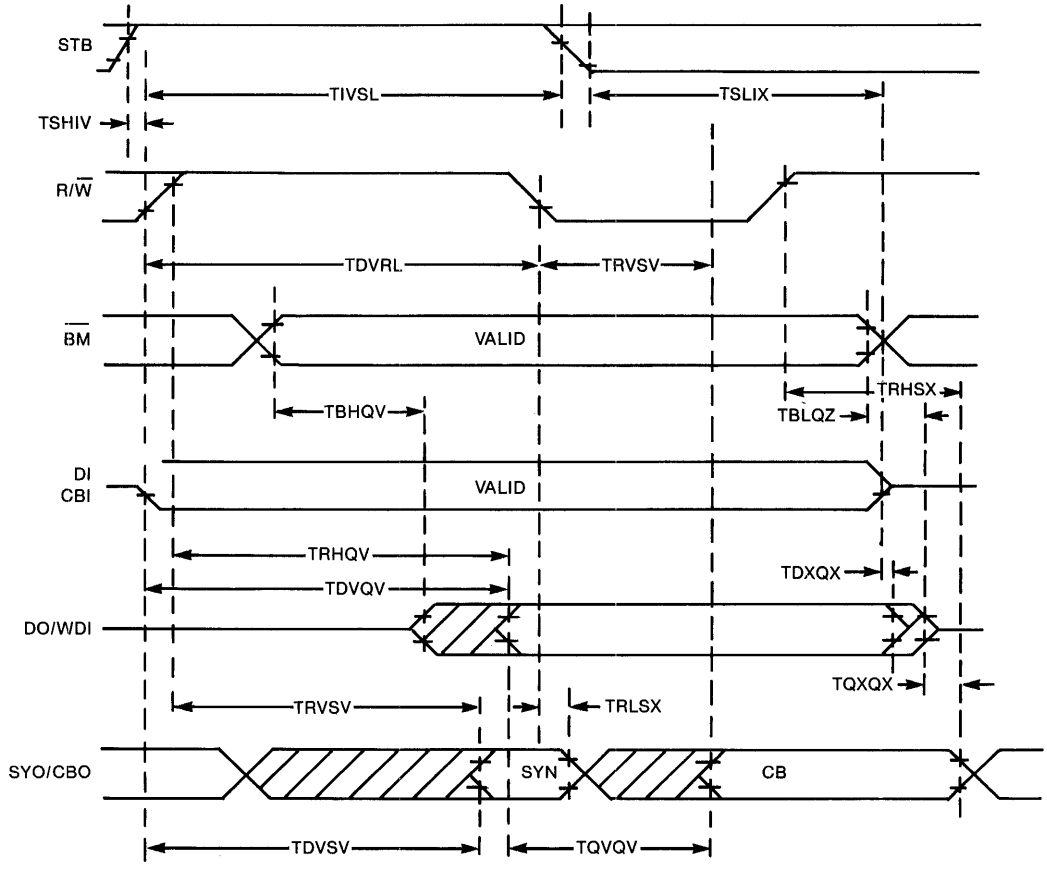


FULL WRITE — MASTER/SLAVE



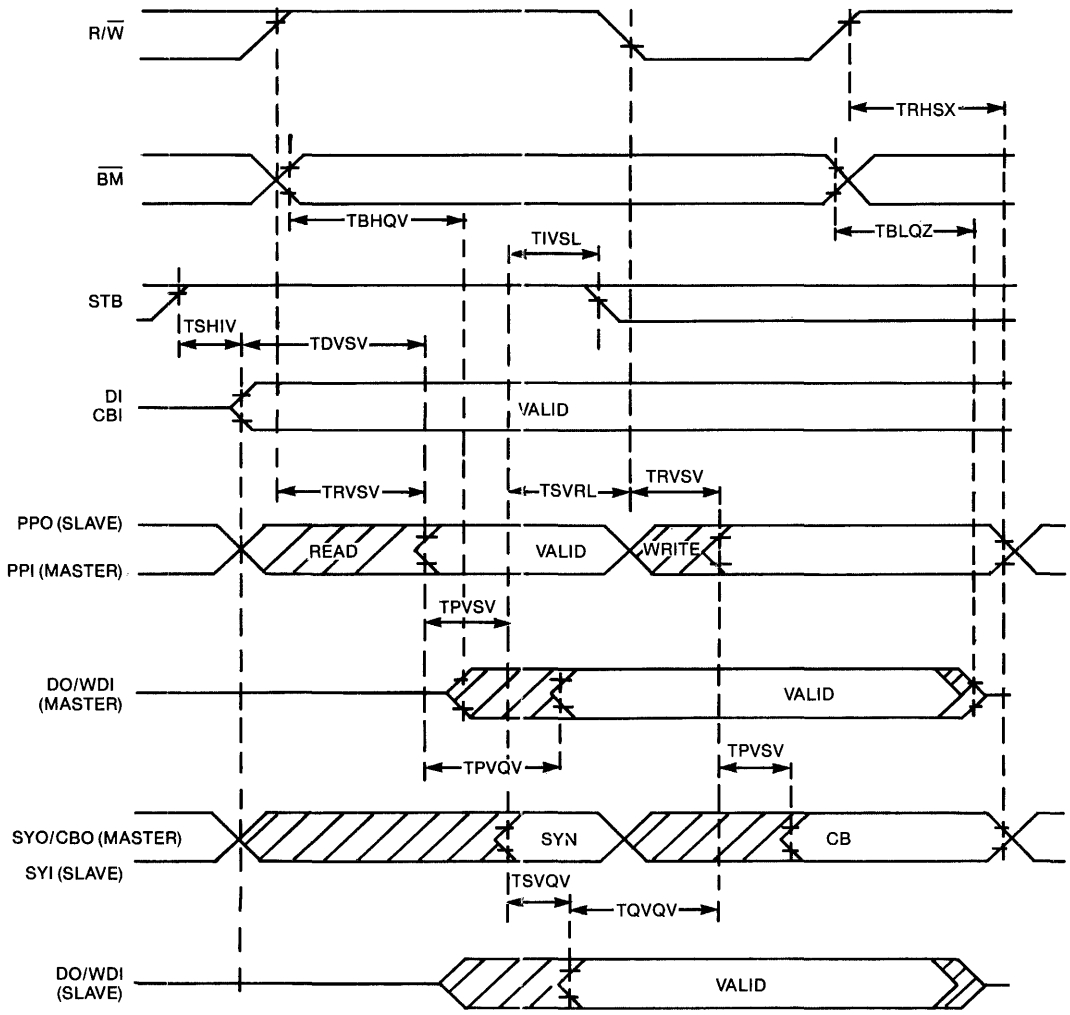
WAVEFORMS (Continued)

READ MODIFY WRITE — 16 BIT ONLY



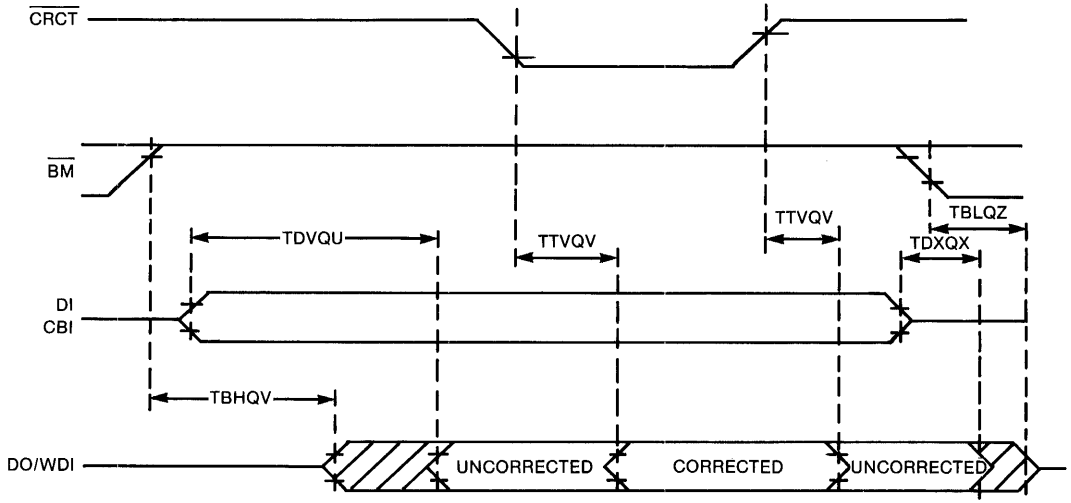
WAVEFORMS (Continued)

READ MODIFY WRITE — MASTER/SLAVE

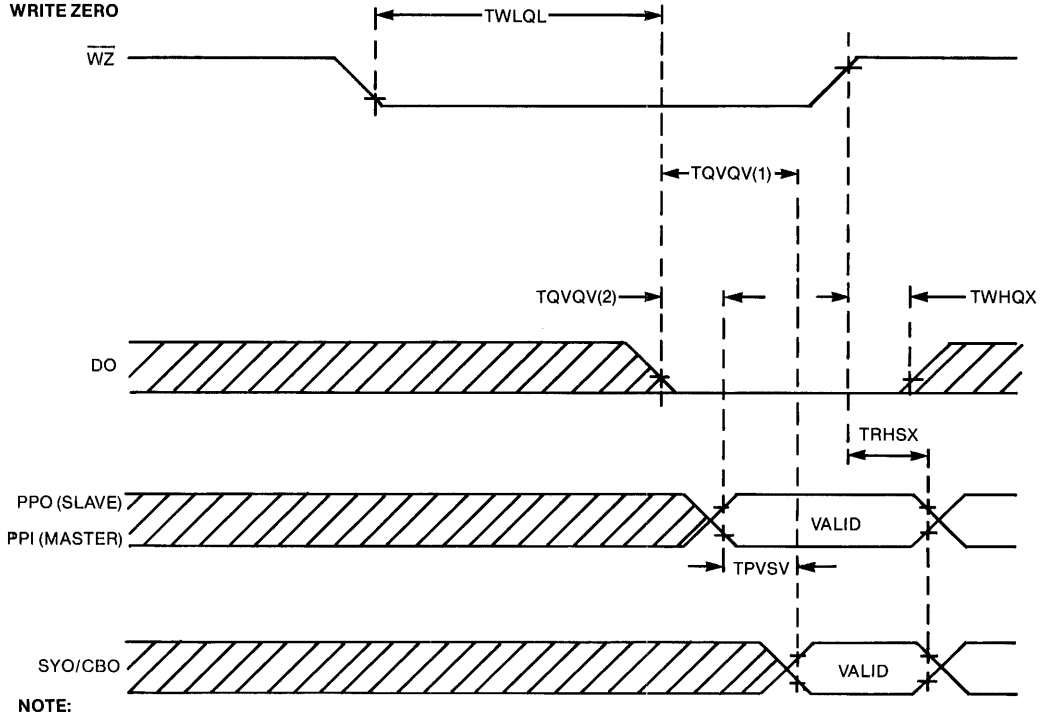


WAVEFORMS (Continued)

NON-CORRECTING READ



WRITE ZERO



NOTE:
(1): 16 BIT ONLY
(2): MASTER/SLAVE

See page 725 for ordering information.

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WD8207 ADVANCED DYNAMIC RAM CONTROLLER

- **Provides All Signals Necessary to Control 16K (2118), 64K (2164A) and 256K Dynamic RAMs**
- **Directly Addresses and Drives up to 2 Megabytes without External Drivers**
- **Supports Single and Dual-Port Configurations**
- **Automatic RAM Initialization in All Modes**
- **Five Programmable Refresh Modes**
- **Transparent Memory Scrubbing in ECC Mode**
- **Supports Intel IAPX 86, 88, 186, and 286 Microprocessors**
- **Data Transfer Acknowledge Signals for Each Port**
- **Provides Signals to Directly Control the 8206 Error Detection and Correction Unit**
- **Supports Synchronous or Asynchronous Operation on Either Port**
- **+5 Volt Only HMOSII Technology for High Performance and Low Power**

The WD8207 Advanced Dynamic RAM Controller (ADRC) is a high-performance, systems-oriented, Dynamic RAM controller that is designed to easily interface 16K, 64K and 256K Dynamic RAMs to Western Digital and other microprocessor Systems. A dual-port interface allows two different busses to independently access memory. When configured with an 8206 Error Detection and Correction Unit the 8207 supplies the necessary logic for designing large error-corrected memory arrays. This combination provides automatic memory initialization and transparent memory error scrubbing.

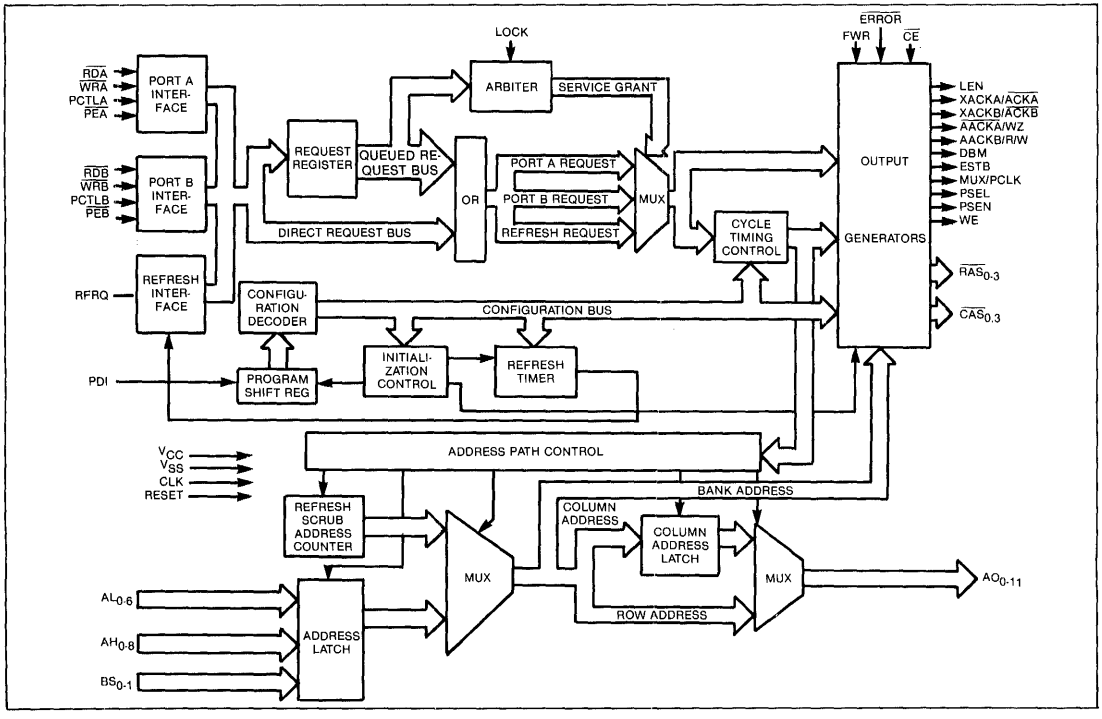

Figure 1. 8207 Block Diagram

See page 725 for ordering information.

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Logic Arrays

WD1820 Logic Array Device

FEATURES

- SINGLE +5V SUPPLY
- REPLACES 74LSXX LOGIC
- MASK PROGRAMMABLE
- THREE-STATE, OPEN COLLECTOR, OR TOTEM-POLE OUTPUTS
- PROGRAMMABLE PULL-UP/PULL-DOWN RESISTORS ON ALL PINS
- 130 LOGIC ELEMENTS
- 10 "LS" LOAD DRIVE CAPABILITY
- LOW POWER DISSIPATION
- QUICK TURN-AROUND
- 20 PIN DUAL-IN-LINE PACKAGE

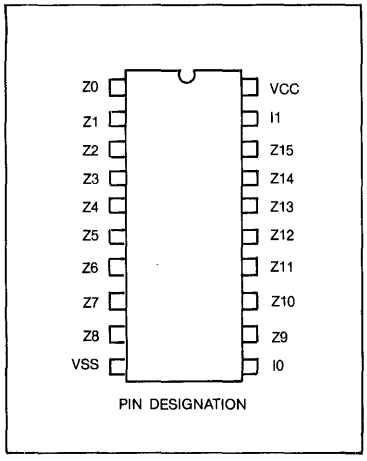


Figure 2

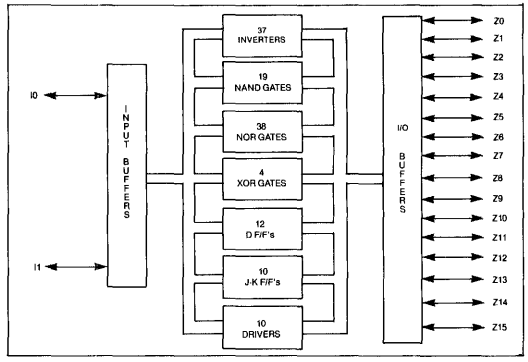


Figure 1

DEVICE DESCRIPTION

The WD1820 Logic Array Device contains 130 uncommitted logic elements that can be interconnected to replace a large amount of discrete S.S.I. Logic functions. Unlike a cell matrix or gate array, this mask programmable device contains prefabricated logic elements such as NAND gates, NOR gates, 'D' and 'JK' Flip/Flops, and a variety of other functions. Gates and Flip/Flops are interconnected using a special coding sheet, which is easily prepared directly from the user's schematic. This coding sheet is then digitized at the factory to produce a two-level mask. The mask is then applied to a pre-fabricated wafer, producing qualification samples typically 4 weeks after receipt of coding form.

For Bus-Oriented applications, sixteen pins of the device may be programmed for Three-State operation. These pins provide I/O capability, with standard TTL Totem-Pole or Open Collector configurations. Two pins are provided as input only pins. All pins are programmable with Pull-Up or Pull-Down resistors on-chip.

The WD1820 is implemented in N-Channel Silicon Gate Technology operating from a single 5 volt power supply. The device is available in either a plastic or ceramic 20 pin Dual-In-Line package.

Table 1

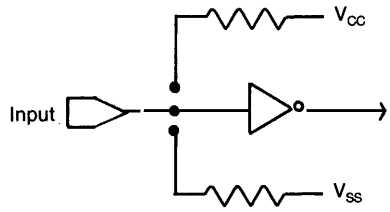
PIN	SYMBOL	NAME	DESCRIPTION
1-9 and 12-18	Z_0-Z_{15}	Three-state 0 to Three-state 15	Three-state, Totem-pole, or Open Collector I/O pins
11,19	I_0, I_1	Input 0, Input 1	Input only pins
V_{SS}	V_{SS}	GND	Ground
V_{CC}	V_{CC}	+5V	+5Volts ± 10% power supply input

I/O LOGIC ELEMENTS

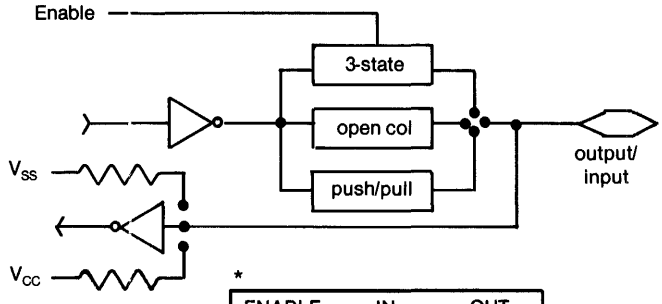
The WD1820 contains sixteen input/output buffers and two input only buffers. The I/O buffers are high current inverting drivers and receivers used to interface an external pin to the internal logic elements. These 16 pins may be programmed for either three-state, totem pole, or open collector operation. When programmed for three-state operation an active high enable signal may be controlled by internal logic, or externally by connecting to an adjacent input pin. The two inverting input only buffers are used to interface directly to TTL logic. All 18 inputs/outputs have programmable pull-up, pull-down, or no resistor options.

INTERFACE ELEMENTS

Input Inverting Buffer
Quantity: 2
Options: Pull-up Resistor
Pull-down Resistor
(6.5KΩTypical)



Input/Output Inverting Buffer
Quantity: 16
Input Options:
Pull-up Resistor
Pull-down Resistor
Output Options:
Totem-Pole
Open Collector
Three-state*



*

ENABLE	IN	OUT
0	0	HI-Z
0	1	HI-Z
1	0	1
1	1	0

Figure 3

INTERNAL LOGIC ELEMENTS

The Internal Logic Elements consist of the following:

Table 2

QTY	LOGIC ELEMENT
37	Inverters
38	2-Input NOR gates
19	2-Input NAND gates
4	2-Input XOR gates
12	D type Flip-Flops
10	JK type Flip-Flops
10	Non-Inverting Drivers

GATES

Inverters, NOR, NAND, and XOR gates comprise the Random Logic elements. The outputs of these gates are connected to a "load device" which applies power to the gate and performs the logic inversion. This method achieves two key features:

1) Gates that are unused do not draw any power (except for leakage currents).
2) All of the above gates may be "Wire-Or'ed" to produce AND-OR-INVERT gates, N-input NOR gates, or complex boolean functions.

FLIP/FLOPS

Both the 'D' and 'JK' types have edge-triggered inputs with programmable low-to-high or high-to-low transition triggering. The 'JK' types may be programmed to perform as 'D' types, providing the user with 22 'D' type Flip/Flops. Independent SET, RESET, Q, and Q signals are available on each type.

NON-INVERTING DRIVERS

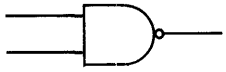
Ten Non-Inverting Drivers provide high-fanout capability for internal logic. These drivers may be used for common CLOCK or SET/RESET lines on heavily loaded nodes of other logic elements.

Random Logic Elements

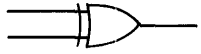
Inverting Buffer
Quantity: 37

2-Input NOR GATE
Quantity: 38

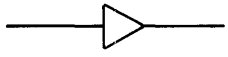
2-Input NAND GATE
Quantity: 19



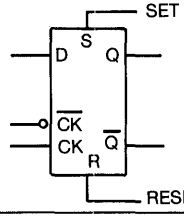
2-Input XOR GATE
Quantity: 4



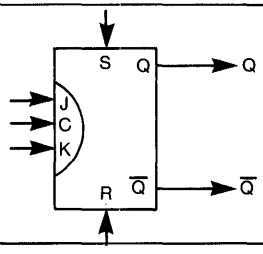
Non-Inverting Driver
Quantity: 10



D Flip/Flop
Quantity: 12
Options: Positive Edge-triggered
Negative Edge-triggered



JK Flip/Flop
Quantity: 10
Options: Positive Edge-triggered
Negative Edge-triggered
Can be 'D' programmed



ABSOLUTE MAXIMUM RATINGS

Operating Temperature ..... 0°C to +70°C
Voltage on any pin with
respect to V_{SS} ..... −0.5V to +7.0V
Storage Temperature ..... −55°C to +125°C plastic
−65°C to +150°C ceramic

NOTE: Maximum ratings indicate limits beyond which permanent device damage may occur. Continuous operation at these ratings is not intended and should be limited to the DC electrical characteristics.

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$, $V_{SS} = 0V$

Maximum Power Ratings ..... 1.0 watt

Table 3

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IH}	High Level Input Voltage	2.2V			V	
V_{IL}	Low Level Input Voltage	−0.5		.8	V	
I_{IH}	High Level Input Current			20	ua	No resistor
I_{IL}	Low Level Input Current			−200	ua	No resistor
C_L	Input Capacitance			10	pf	
P_R	Programmable Resistor	3.3	6.5	10	KΩ	
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -200$ua
V_{OL}	Output Low Voltage			.4	V	$I_{OL} = 4.0$ma
P_D	Power Dissipation					
	Input Buffer			6.5	mw	50% duty cycle
	Logic Gate			3.2	mw	50% duty cycle
	Driver			10.0	mw	
	I/O Buffer			30.0	mw	
	D Flip/Flop			17.6	mw	
	JK Flip/Flop			17.6	mw	
I_L	Output Leakage			10	ua	

TIMING CHARACTERISTICS

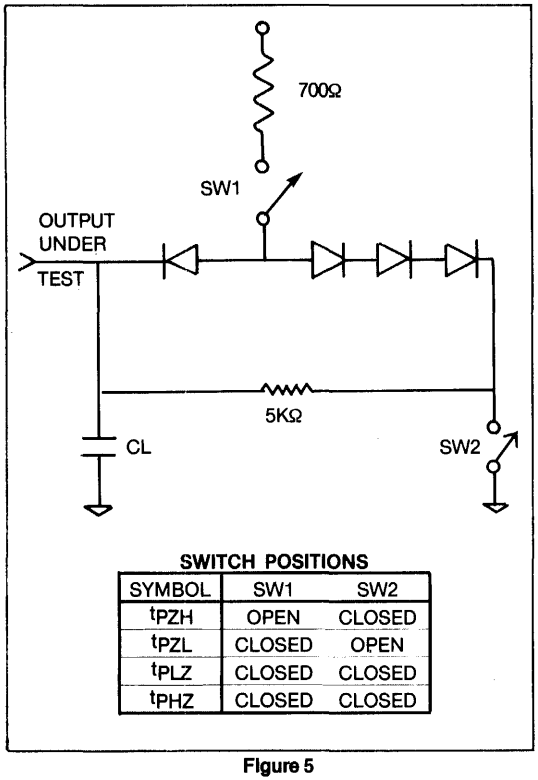
T_A = 0°C to +70°C, V_{CC} +5V ± 10%, V_{SS} = 0V

Table 4

PARAMETER	MIN	MAX	CONDITIONS
Logic Gate Delay (NOR, NAND, Inverter)			
Delay to Low Level (t_{PHL})		18 ns	Figure 7
Delay to High Level (t_{PLH})		21 ns	Figure 7
Input Buffer Propagation Delay			
Delay to Low Level (t_{PHL})		6 ns	Figure 7
Delay to High Level (t_{PLH})		19.5 ns	Figure 7
Output Buffer Propagation Delay			
Delay to Low Level (t_{PHL})		45 ns	C_L = 75pf Figure 7
Delay to High Level (t_{PLH})		40 ns	Figure 7
Output Enable Time to High Level (t_{PZH})		65 ns	C_L = 75pf Figure 9
Output Enable Time to Low Level (t_{PZL})		65 ns	Figure 9
Output Disable Time from Low Level (t_{PLZ})		50 ns	C_L = 5pf Figure 9
Output Disable Time from High Level (t_{PHZ})		60 ns	Figure 9
Flip-Flop, Positive Going Edge			
Type D			
Delay to High Level (t_{PLH})		55 ns	Figure 7
Delay to Low Level (t_{PHL})		50 ns	Figure 7
Set, Reset Propagation Delay		45 ns	Figure 7
Type JK			
Delay to High Level (t_{PLH})		65 ns	Figure 7
Delay to Low Level (t_{PHL})		60 ns	Figure 7
Set, Reset Propagation Delay		55 ns	Figure 7
Type D and JK			
Data Set-Up Time (t_s)	30 ns		Figure 6
Data Hold Time (t_h)	5 ns		Figure 6
CLK, Set, Reset Pulse Width (t_w)	100ns		Figure 8
Flip-Flop, Negative Going Edge			
Type D			
Delay to High Level (t_{PLH})		55 ns	Figure 7
Delay to Low Level (t_{PHL})		60 ns	Figure 7
Set, Reset Propagation Delay		45 ns	Figure 7
Type JK			
Delay to High Level (t_{PLH})		65 ns	Figure 7
Delay to Low Level (t_{PHL})		70 ns	Figure 7
Set, Reset Propagation Delay		55 ns	Figure 7
Type D and JK			
Data Set-up Time (t_s)	30 ns		Figure 6
Data Hold Time (t_h)	5 ns		Figure 6
CLK, Set, Reset Pulse Width (t_w)	100 ns		Figure 8

Parameter Measurement Information

Load Circuit



SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	OPEN	CLOSED
t_{PZL}	CLOSED	OPEN
t_{PLZ}	CLOSED	CLOSED
t_{PHZ}	CLOSED	CLOSED

Figure 5

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

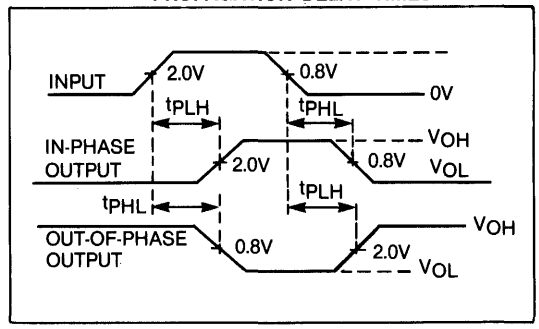


Figure 7

VOLTAGE WAVEFORMS PULSE WIDTHS

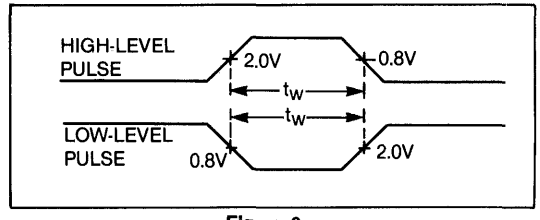


Figure 8

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

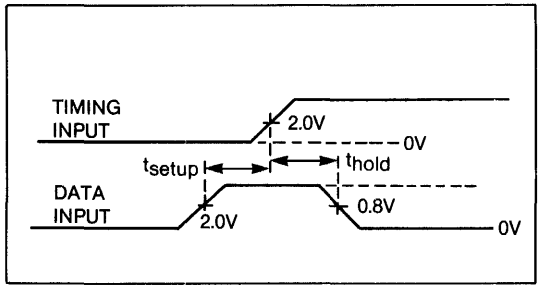


Figure 6

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

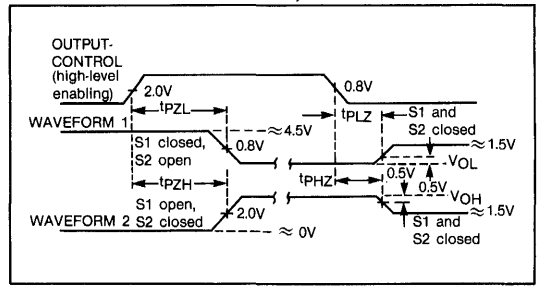


Figure 9

See page 725 for ordering information.

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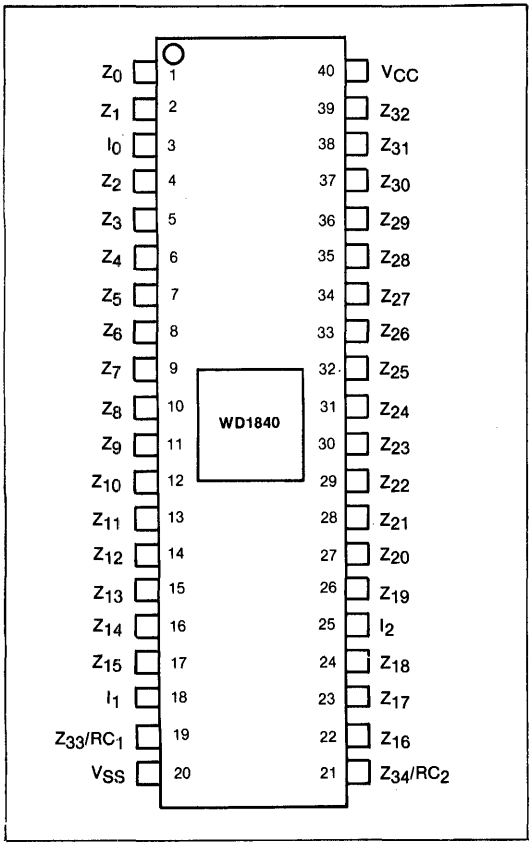
ADVANCE INFORMATION

WD1840 Logic Array Device

FEATURES

- SINGLE +5V SUPPLY
- REPLACES 74LSXX LOGIC
- MASK PROGRAMMABLE
- 35 PROGRAMMABLE THREE-STATE OPEN COLLECTOR, OR TOTEM POLE OUTPUTS
- OVER 400 LOGIC ELEMENTS
- 2 ON-CHIP MULTIVIBRATORS
- ON CHIP PLA FOR STATE MACHINE IMPLEMENTATION
- TTL COMPATIBLE
- QUICK TURNAROUND
- AVAILABLE IN EITHER 40 OR 28 PIN DUAL-IN LINE PACKAGE



PIN DESIGNATION

DEVICE DESCRIPTION

The WD1840 Logic Array Device contains over 400 uncommitted logic elements that can be interconnected to replace a large amount of discrete MSI logic functions. It is an addition to the WD1820 family, offering the designer extended I/O capability and more logic elements. The device also contains dual monostable multivibrators and a general purpose PLA configured as a state machine.

Unlike a cell matrix or gate array, this mask programmable device contains prefabricated logic elements such as NAND, NOR, XOR, and Invertor gates, plus 'D' and 'JK' or 'J̄K' Flip/Flops. Gates and Flip/Flops are interconnected using a special coding sheet, which is easily prepared from the user's schematic. This coding sheet is then digitized at the factory to produce a two-level mask. The mask is then applied to a prefabricated wafer, producing qualified samples typically 6 weeks after receipt of the coding form.

The WD1840 is implemented in N-channel silicon gate technology operating from a single +5V power supply. It is available in either plastic or ceramic DIP.

TABLE 1

PIN NUMBER	SYMBOL	DESCRIPTION
1, 2, 4-17, 22-24, 26-39	Z_0-Z_{32}	Programmable I/O pins with 3-state, open collector, or push pull capability.
3, 18, 25	I_0-I_2	Input only pins.
19 and 21	Z_{33}/RC_1 Z_{34}/RC_2	Programmable I/O pins which at S_0 can function as the external RC inputs for one-shot operations.
20	V_{SS}	Ground
40	V_{CC}	+5V ± 10% power supply input.

LOGIC ELEMENTS

The WD1840 contains thirty-five input/output buffers and three input only buffers. The I/O buffers are high current inverting drivers and receivers used to interface an external pin to the internal logic elements. These 35 pins may be programmed for either three-state, totem pole, or open collector operation. When programmed for three-state operation an active high

enable signal may be controlled by internal logic, or externally by connecting to an adjacent input pin. The three inverting input only buffers are used to interface directly to TTL logic. All 38 inputs/outputs have programmable pull-up, pull-down, or no resistor options.

Two input-output pins can be programmed as the RC input for selected one-shot control.

INTERNAL LOGIC ELEMENTS

The Internal Logic Elements consist of the following:

TABLE 2

QTY	LOGIC ELEMENT
112	Inverters
112	2-Input NOR gates
88	2-Input NAND gates
22	2-Input XOR gates
62	D type Flip-Flops
5	JK type Flip-Flops
17	Non-Inverting Drivers
1	24x24x16 PLA

GATES

Inverters, NOR, NAND, and XOR gates comprise the Random Logic elements. The outputs of these gates are connected to a "load device" which applies power to the gate and performs the logic inversion. This method achieves two key features:

1) Gates that are unused do not draw any power (except for leakage currents).
2) All of the above gates may be "Wire-Or'ed" to produce AND-OR-INVERT gates, N-input NOR gates, or complex boolean functions.

FLIP/FLOPS

Both the 'D' and 'JK' types have edge-triggered clock inputs with programmable low-to-high or high-to-low transition triggering. The 'JK' types may be programmed to perform as 'D' types or as 'JK.' Independent SET, RESET, Q, and $\overline{Q}$ signals are available on each type.

NON-INVERTING DRIVERS

Seventeen Non-Inverting Drivers provide high-fanout capability for internal logic. These drivers may be used for common CLOCK or SET/RESET lines on heavily loaded nodes of other logic elements.

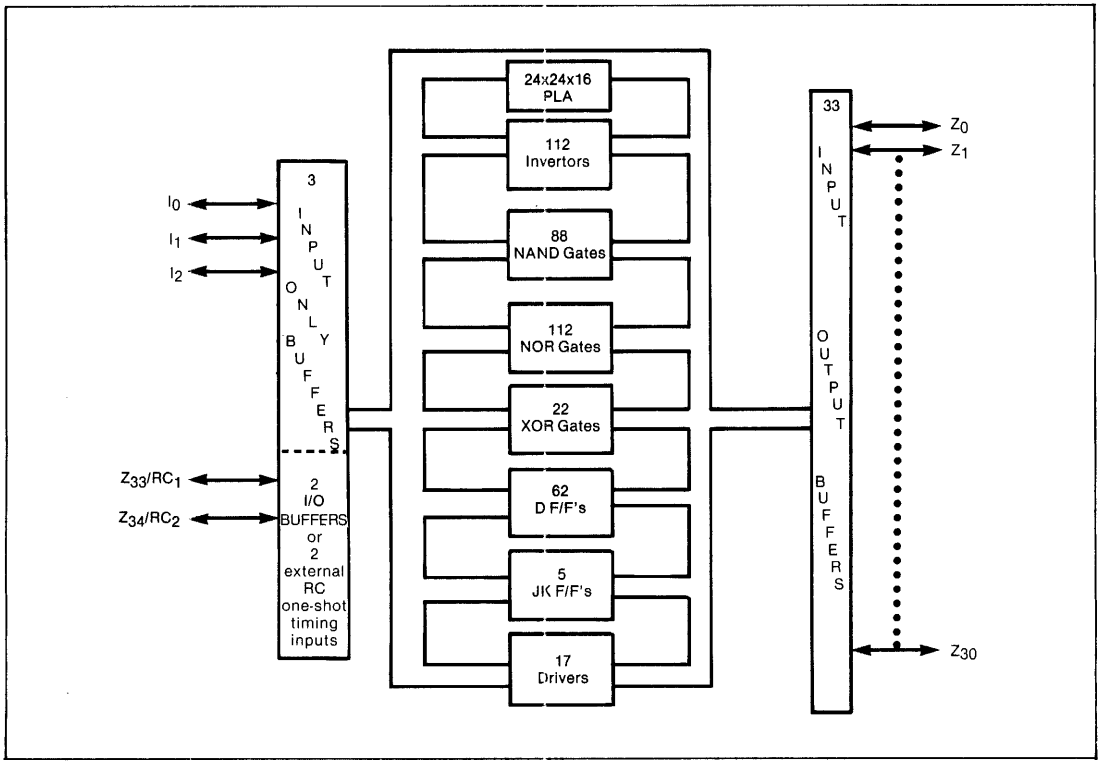


Figure 2 WD1840 BLOCK DIAGRAM

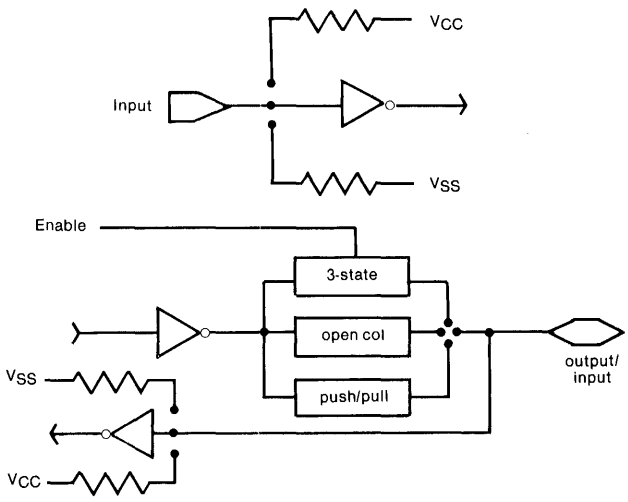
INTERFACE ELEMENTS

Input Inverting Buffer
Quantity: 3
Options: Pull-up Resistor
Pull-down Resistor
(6.5KΩ Typical)

Input/Output Inverting Buffer
Quantity: 35
Input Options:
Pull-up Resistor
Pull-down Resistor
Output Options:
Totem-Pole
Open Collector
Three-state*

*

ENABLE	IN	OUT
0	0	HI-Z
0	1	HI-Z
1	0	1
1	1	0



RANDOM LOGIC ELEMENTS

Inverting Buffer
Quantity: 112

2-Input NOR GATE
Quantity: 112

2-Input NAND GATE
Quantity: 88

2-Input XOR GATE
Quantity: 22

Non-Inverting Driver
Quantity: 17

D Flip/Flop
Quantity: 63
Options: Positive Edge-triggered
Negative Edge-triggered

JK Flip/Flop
Quantity: 5
Options: Positive Edge-triggered
Negative Edge-triggered
Can be 'D' programmed
Can be 'JK' programmed

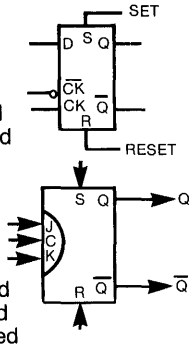


Figure 4

GENERAL-PURPOSE PLA

The general-purpose PLA consists of two internally connected gate matrices. The upper "AND" matrix is a 24x24 array with synchronizing flip/flop inputs. The lower "OR" matrix is a 24x16 array with internal state counter. In addition, a 2 phase clock generator has been included to generate appropriate clocks to keep synchronism between the two matrices.

Twenty-four sub-term outputs (S_0, S_2, ... S_{23}) are available for further interconnect throughout the WD1840. Sixteen independent term outputs (0_0 — 0_{15}) can be user defined to create any type of control signal desired.

To program the PLA, the user simply "circles" a cross point in the matrix to enable that transistor.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature ..... 0°C to +70°C
Voltage on any pin with
respect to V_{SS} ..... −0.5V to +7.0V
Storage Temperature
Ceramic ..... −65°C to +150°C
Plastic ..... −55°C to +125°C
Maximum Power Dissipation ..... 1.5 watt ceramic;
1.0 watt plastic

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ± 10%, V_{SS} = 0V

NOTE:
Maximum ratings indicate limits beyond which permanent device damage may occur. Continuous operation at these ratings is not intended and should be limited to the DC electrical characteristics.

TABLE 3

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IH}	High Level Input Voltage	2.2V			V	
V_{IL}	Low Level Input Voltage			.8	V	
I_{IH}	High Level Input Current			20	μA	No resistor
I_{IL}	Low Level Input Current			−200	μA	No resistor
C_L	Input Capacitance			10	pf	
P_R	Programmable Resistor	3.0	6.5	10	KΩ	
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{OL}	Output Low Voltage			.4	V	I_{OL} = 4.0ma
P_D	Power Dissipation					
	Input Buffer		6	9	mw	50% duty cycle
	Logic Gate		3	4	mw	50% duty cycle
	Driver		7	10.0	mw	
	I/O Buffer		20	30.0	mw	
	D Flip/Flop		9	14.0	mw	
	JK Flip/Flop		9	17.0	mw	
	D Flip/Flop Reduced Power		4.5	7.0	mw	
I_L	Output Leakage			±10	μA	

See page 725 for ordering information.

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Network Products

WD2501/2511 Packet Network Interface (LAP/LAPB)

FEATURES

- Packet switching controller, compatible with CCITT recommendation X.25, level 2, LAP (2501) or LAPB (2511)
- Programmable primary timer (T1) and retransmission counter (N2)
- Programmable A-field which provides a wider range of applications than defined by X.25. These include: DTE-to-DTE connection, multipoint and loop-back testing
- Direct memory access (DMA) transfer: two channels; one for transmit and one for receive. Send/receive data accessed by indirect addressing method. Sixteen output address lines.
- Zero bit insert and delete
- Automatic appending and testing of FCS field
- Computer bus interface structure: 8 bit bi-directional data bus. CS, WE, RE and four input address lines
- DC to 1.1 MBPS data rate
- TTL compatible
- 48 pin dual in-line packages
- Higher bit rates available by special order

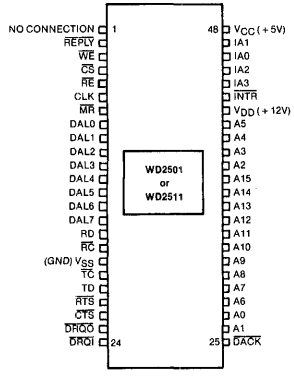
APPLICATIONS

X.25 PACKET SWITCHING CONTROLLER
PART OF DTE OR DCE
PRIVATE PACKET NETWORKS
LINK LEVEL CONTROLLER

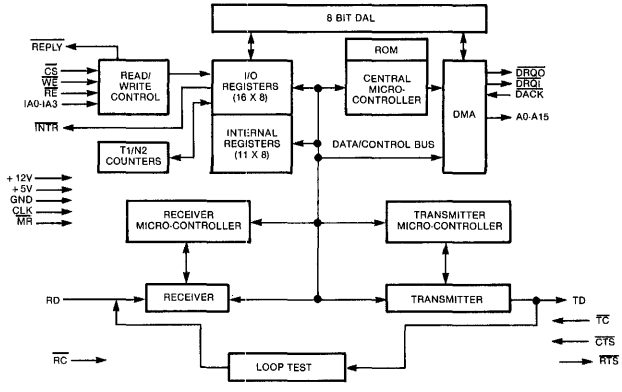
GENERAL DESCRIPTION

The WD2501/2511 is a MOS/LSI device which handles bit-oriented, full-duplex serial data communications with DMA, which conforms to CCITT X.25 with programmable enhancements.

The device is fabricated in N-Channel silicon gate MOS technology and is TTL compatible on all inputs and outputs.



PIN ASSIGNMENTS

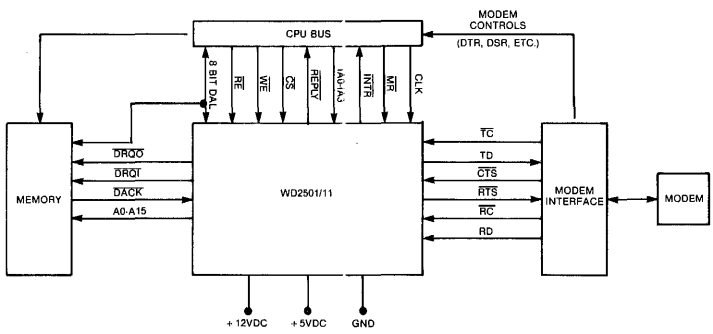


BLOCK DIAGRAM

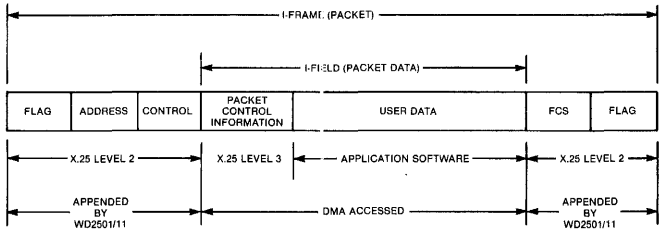
INTERFACE SIGNAL DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
48	POWER SUPPLY	V_{CC}	+5VDC power supply input.
42	POWER SUPPLY	V_{DD}	+12VDC power supply input.
18	GROUND	V_{SS}	Ground
6	CLOCK	CLK	Clock input used for internal timing. Must be square wave from 1.0 to 2.0/2.5 MHz. See ordering information.
7	MASTER RESET	$\overline{MR}$	Initialize on active low. All registers reset to zero, except control bits MDISC and $\overline{LINK}$ are set to 1 $\overline{DACK}$ must be stable high before $\overline{MR}$ goes high.
4	CHIP SELECT	$\overline{CS}$	Active low chip select for CPU control of I/O registers.
8-15	DATA ACCESS LINES	DAL0-DAL7	An 8 bit bi-directional three-state bus for CPU and DMA controlled transfers.
5	READ ENABLE	$\overline{RE}$	The contents of the selected register are placed on DAL when $\overline{CS}$ and $\overline{RE}$ are low.
3	WRITE ENABLE	$\overline{WE}$	The data on the DAL are written into the selected register when CS and WE are low. RE and WE must not be low at the same time.
2	REPLY	$\overline{REPLY}$	An active low output to indicate that either a $\overline{CS}$•$\overline{WE}$ or $\overline{CS}$•$\overline{RE}$ input is active.
43	INTERRUPT REQUEST	$\overline{INTR}$	An active low interrupt service request output. Returns high when Status Register #1 is read.
46, 47, 45, 44	ADDRESS LINES IN	IA0-IA3	Four address inputs to the 2501/11 for CPU controlled read/write operation with registers in the 2501/11. If ADRV = 0, these may be tied to A0-A3.
27, 26 38-41, 28-37	ADDRESS LINES OUT	A0-A15	Sixteen address outputs from the 2501/11 for DMA operation. If the control bit ADRV is 1, the outputs are TTL drives at all times. If ADRV is 0, the outputs are 3-state, and are HI-Z whenever $\overline{DACK}$ is high. (ADRV is in Control Register #1.)
23	DMA REQUEST OUT	$\overline{DRQO}$	An active low output signal to initiate CPU bus request so that 2501/11 can output onto the bus.
24	DMA REQUEST IN	$\overline{DRQI}$	An active low output signal to initiate CPU bus request so that data may be input to the 2501/11. $\overline{DRQI}$ and $\overline{DRQO}$ cannot be low at the same time.
25	DMA ACKNOWLEDGE	$\overline{DACK}$	An active low input from the CPU interface logic in response to $\overline{DRQO}$ or $\overline{DRQI}$. $\overline{DACK}$ must not be low if $\overline{CS}$ and $\overline{RE}$ are low or if $\overline{CS}$ and $\overline{WE}$ are low.
20	TRANSMIT DATA	TD	Transmitted serial data output.
16	RECEIVE DATA	RD	Receive serial data input.
19	TRANSMIT CLOCK	$\overline{TC}$	A 1X clock input. TD changes on the falling edge of $\overline{TC}$.
17	RECEIVE CLOCK	$\overline{RC}$	This is a 1X clock input, and RD is sampled on the rising edge of $\overline{RC}$.

21	REQUEST-TO-SEND	$\overline{RTS}$	An open collector (drain) output which goes low when the 2501/11 is ready to transmit either flags or data. May be hard-wired to ground.
22	CLEAR-TO-SEND	$\overline{CTS}$	An acive low input which signals the 2501/11 that transmission may begin. If high, the TD output is forced high. May be hard-wired to ground.
1	NO CONNECTION		Leave pin open.



SYSTEM CONNECTION



According to the X.25 protocol, there are three types of frames: supervisory (S-frame), unnumbered (U-frame), and information (I-frame). All S- and U frames are generated and tested by the 2501. The user's CPU handles only the I-field of I-frames, which are packet data.

NOTE: X.25 Level 1 is the physical interface.

FRAME FORMAT CONTROL

The WD2501/11 is controlled and monitored by sixteen I/O registers.

Control, status and error bits will be referred to as CR, SR and ER, respectively, along with two digits. For example, SR16 refers to status register #1 and bit 6, which is "XBA."

REG. #	IA3	IA2	IA1	IA0	REGISTER	REGISTER GROUPING
0	0	0	0	0	CR0	
1	0	0	0	1	CR1	OVERALL CONTROL
2	0	0	1	0	*SR0	AND
3	0	0	1	1	*SR1	MONITOR
4	0	1	0	0	*SR2	
5	0	1	0	1	*ER0	
6	0	1	1	0	*CHAIN MONITOR	RECEIVER
7	0	1	1	1	*RECEIVED C-FIELD	MONITOR
8	1	0	0	0	T1	TIMER
9	1	0	0	1	N2/T1	
A	1	0	1	0	TLOOK HI	
B	1	0	1	1	TLOOK LO	DMA SET-UP
C	1	1	0	0	CHAIN/LIMIT	
D	1	1	0	1	(UNUSED)	
E	1	1	1	0	XMT COMMAND	"A" FIELD
F	1	1	1	1	XMT RESPONSE	

*CPU READ ONLY. (Write not possible)

CONTROL, STATUS, ERROR REGISTERS

REGISTER	7	6	5	4	3	2	1	0
CR0	$\overline{\text{A DISC}}$*	0	HALF/ $\overline{\text{FULL}}$*	ACTIVE/ $\overline{\text{PASSIVE}}$	LOOP TEST	RAMT	RECR	MDISC
CR1	TXMT*	TRCV*	$\overline{\text{XI}}$*	ADRV	0	0	0	SEND
SR0	NA2	NA1	NA0	RNRR	NB2	NB1	NB0	RNRX
SR1	[1]PKR	[1]XBA	[1]ERROR		NE2	NE1	NE0	
SR2	T1OUT	$\overline{\text{IRTS}}$	REC IDLE					$\overline{\text{LINK}}$
ER0	ER07	ER06	ER05	ER04	ER03	ER02	ER01	ER00

[1]Causes Interrupt (INTR Goes Low). *Used on 2511, only.

BIT	DESCRIPTION
CR07	$\overline{\text{ADISC}}$ is used when CR04 = 1 (ACTIVE). When the 2511 actively initiates link set-up, a DISC will be transmitted and acknowledged prior to transmission of the SABM if CR07 = 0. Otherwise, the 2511 will send the SABM for link set-up, but not preceed the SABM with a DISC if CR07 = 1.
CR06	Unused control bits, like CR06, should remain at 0.
CR05	H/F selects full duplex if CR05 = 0, and half duplex if CR05 = 1. (See Appendix B).
CR04	This bit will cause the 2501/11 to initiate link set-up if CR04 = 1, or to wait for a link set-up from the remote device if CR04 = 0.
CR03	The LOOP TEST bit will connect the transmitted data output to the receiver input. The receiver input pin, RD, is gated-out. The "E" and "F" registers of the A-field should be equal.
CR01	This bit is RECR which defines the CPU's receiver buffer as Ready (CR01 = 1) or as Not Ready (CR01 = 0).
CR00	MDISC is a mandatory disconnect command. MDISC will cause a logical disconnect in the DTE/DCE link. No DMA accessed data may be transferred as long as MDISC = 1. After Master Reset ($\overline{\text{MR}}$ pin transition from low to high), MDISC will be set. The 2501/11 will neither transmit nor accept received data until MDISC = 0.
CR14	The ADRV bit (CR14) is the control for the 16 bit output addresses (A0-A15). if ADRV = 0, the outputs are 3-state and are in HI-Z, except when $\overline{\text{DACK}}$ goes low. If ADRV = 1, the outputs are always low impedance (TTL), and are high when $\overline{\text{DACK}}$ is high.
CR17, CR16, CR15	TXMT and TRCV selects the transparent modes.
CR10*	The SEND bit (CR10) is used to command the 2501/11 to send the next packet or packets. If SEND = 1, the 2501/11 will read from TLOOK the BRDY bit of the next segment for transmission. If BRDY = 0, the 2501/11 will clear SEND and no action occurs. If BRDY = 1, the 2501/11 will then read TSADR and TCNT, followed by the transmission of that buffer. After transmission, the 2501/11 clears BRDY of the segment just transmitted, and reads BRDY of the next segment. If 1, the next segment is transmitted. If 0, the SEND bit is cleared, and transmission of packets is stopped.
SR07-SR05*	NA2-NA0. Next block of transmitted data to be Acknowledged.
SR04	RNRR. An RNR has been received.
SR03-SR01*	NB2-NB0. Next block to be transmitted.

BIT	DESCRIPTION
SR00	RNRX. As a result of RECR (CR01) = 0, an RNR has been transmitted.
SR17	The PKR bit stands for Packet Received. This means that a packet has been received error-free and in correct sequence according to the received N (S) count. The data (I-field) has been placed in the CPU's RAM memory. NE is advanced. The three interrupt-causing bits are SR17, SR16, and SR15. Any of the three will cause an interrupt request ($\overline{INTR}$ goes low) when that bit goes to a 1. After SR1 is read, all three bits are reset to 0, and $\overline{INTR}$ returns high.
SR16	The XBA bit means that a previously transmitted Block, or Blocks, have been acknowledged by the remote device. Upon acknowledgement, the ACK'ED bit is set to "1" for each segment in TLOOK which was acknowledged.
SR15	The ERROR bit indicates: 1) An error has occurred which is not recoverable by the 2501/11, or 2) A significant event has occurred. The "significant events" are: change in link status (link-up or down), the 2501/11 is progressing to the next segment in a chained receive buffer, or one-direction of the link has been reset. The exact nature of the reason for the ERROR bit is given in ER0.
SR13-SR11*	NE2-NE0. Next Expected packet segment number of RLOOK.
SR27	T1OUT bit means that timer T1 has timed-out. This bit returns to 0 when T1 is re-started.
SR26	$\overline{IRTS}$ stands for the Internal Request-To-Send bit, and indicates that the transmitter is attempting (successful or not) to send either data or flags. If the $\overline{RTS}$ pin is not tied to ground or WIRE-ORED with another signal, then $\overline{IRTS}$ = $\overline{RTS}$.
SR25	REC IDLE indicates that the 2501/11 has received at least 15 contiguous 1's.
SR20	If the link is established, $\overline{LINK}$ = 0. If the link is logically disconnected, $\overline{LINK}$ = 1.

*See "Memory Access Method" Section

ERROR REGISTER (ER0)

ER07	ER06	ER05						
0	0	0	ER00 = NOSFR (2501 only) ER01 = ROR ER02 = TUR ER03 = Not Used ER04 = RLNR					
0	0	1	ER04	ER03	ER02	ER01	ER00	
			0	0	0	0	1	LINK is up. (Was down)
			1	0	0	0	0	Received DISC or DM while LINK up.
			0	0	1	0	0	DISC sent, since SARM sent N2 times without UA.
			0	0	0	1	0	DISC sent, RED IDLE for T1xN2.
0	1	0	CHAIN STATUS ER00 = GNCS ER01 = CNR					
1	0		LINK RESET RECEIVED if ER05 - ER00 = 000000 LINK RESET TRANSMITTED if ER05 - ER00 = non-zero ER00 similar to W ER01 similar to X ER02 similar to Y ER03 similar to Z ER05 means received F = 1, but did not send P = 1 ER04 means I-frame was sent N2 times without acknowledge					
1	1		COMMAND REJECT RECEIVED if ER05 - ER00 = 000000 TRANSMITTED if ER05 - ER00 = non-zero ER00 = W ER01 = X ER02 = Y ER03 = Z					

NOTES:
1. Whenever a command reject (CMDR) is received, the I-field will have been placed in appropriate memory by DMA, and a link reset SARM will be transmitted. The NB is not advanced.
2. Definitions of W, X, Y, Z as stated in CCITT X.25.

TERMS USED IN ERROR REGISTER

GNCS

Going to Next Chain Segment.

RLNR

RLOOK Not Ready. REC RDY bit of next segment is 0.

ROR

Receiver Over-Run. The Receiver Register (RR) had a character to load into the FIFO, but the FIFO was full.

TUR

Transmitter Under-Run. The Transmitter Register (TR) needed a character from the Transmitter Holding Register (THR), but the THR was not ready.

NOSFR

No S-frame received for T1 x N2.

MEMORY ACCESS METHOD

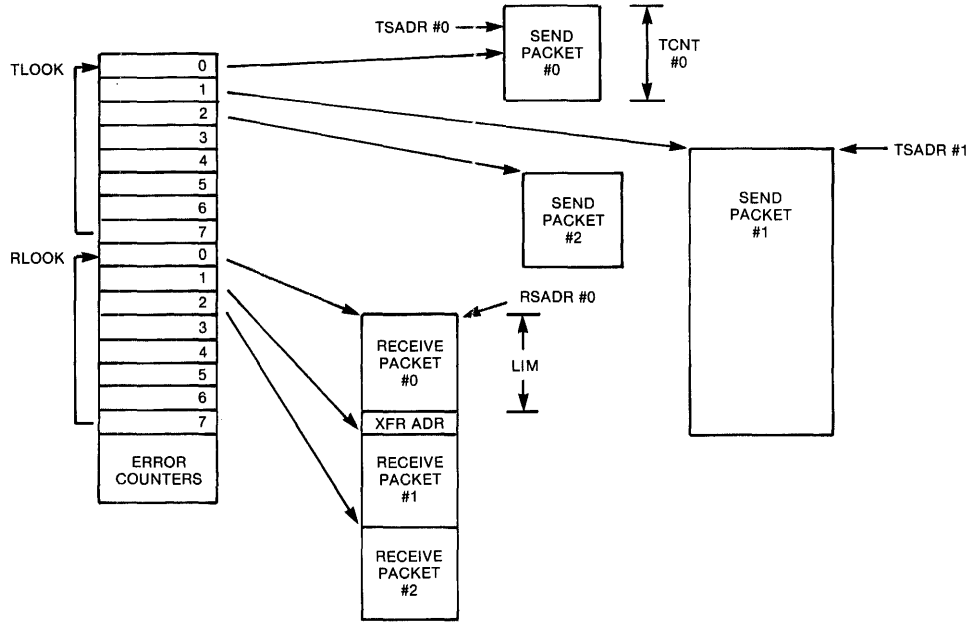
The memory access method, which includes DMA, is designed to take full advantage of the bit-oriented protocol which allows up to 7 I-frames to be outstanding (i.e., unacknowledged) in each direction of a communications link. The memory access method used two "look-up" tables: One for transmit and one for receive. These tables contain addresses and control for the inidividual send/receive packets. Thus, packet data are DMA addressed indirectly. This method is bet suited for most software applications.

The 16 bit starting address for the look-up table TLOOK is loaded into the 2501/11 by the CPU. (I/O Registers "A" and "B"). RLOOK must immediately follow TLOOK in contiguous fashion. TLOOK and RLOOK are in the RAM memory external to the 2501/11. There are a total of 8 segmented control sections for each table. Each segment contains eight bytes. Four bytes are used for data memory starting address and length, two bits of one byte are used for control, one byte defines variable bit length and residual, and the other two bytes are open for user definition.

In transmit, the 2501/11 will have read from TLOOK the starting address and length of the first packet to be transmitted. The 2501/11 will automatically transmit the flag, address, and control fields. Next, the information field data will be transmitted using DMA from the "SEND #0 PACKET" memory. At the end of the information field, the 2501/11 will automatically send the FCS and closing Flag. The 2501/11 will then move on to the next packet.

If retransmission of one or more (up to seven) packets becomes necessary, the 2501/11 will automatically retrace the previous transmissions through the TLOOK table. The user's CPU software does not become involved in the retransmission. However, an ERROR COUNTER is incremented. (See Error Counter Section.)

To receive, each frame is checked for correct address and FCS fields and for type of control field. If the frame is a packet, the information field is placed in the assigned memory location in a method similar to that used in transmit. After the packet is received error-free and in proper N(S) sequence count, an interrupt is generated, and the 2501/11 is ready for the next packet which will be placed in the next location.



MEMORY ACCESS SCHEME

"DEADLY EMBRACE" PREVENTION

A "deadly embrace" can occur when two processors reach a state where each is waiting for the other. In this case, the two processors are the user's CPU and the micro-controller inside the 2501/11. Therefore, to prevent the "deadly embrace," the following rule is obeyed by the 2501/11 and should also be obeyed by the user's CPU. This rule applies to TLOOK, RLOOK, and to the I/O registers. The Error Counters do not apply to this rule.

RULE:
If a bit is set by the CPU, it will not be set by the 2501/11, and vice versa. If a bit is cleared by the 2501/11, it will not be cleared by the CPU, and vice versa.

As an example, the BRDY bit in the TLOOK segment is set by the CPU only, but cleared by the 2501/11 only.

ERROR COUNTERS

Following contiguously after RLOOK is ten 8-bit error counters. The 2501/11 will increment each counter at the occurrence of the defined event. However, the 2501/11 will not increment past 255 (all 1's). The CPU has the responsibility of clearing each counter. The first counter past RLOOK is #1, etc.

ERROR COUNTER	COUNT
1	Received Frames with FCS Error or Aborted
2	Received Short Frames (less than 32 bits)
3	Number of times T1 ran-out (completed)
4	Number of I-Frame Retransmissions (2501 only)
5	REJ Frames Received
6	REJ Frames Transmitted

BYTE # IN SEGMENT	7	6	5	4	3	2	1	0
1	ACK'ED	RESERVED						BRDY
2	TSADR HI							
3	TSADR LO							
4	RESERVED				TCNT HI			
5	TCNT LO							
6*	SPARE*							
7*	SPARE*							
8*	SPARE*							

*Spare. Must be present. User may use these bytes.

TLOOK SEGMENT

BYTE # IN SEGMENT	7	6	5	4	3	2	1	0
1	FRCML	RESERVED			RES2	RES1	RES0	REC RDY
2	RSADR HI							
3	RSADR LO							
4	RESERVED				RCNT HI			
5	RCNT LO							
6*	SPARE							
7*	SPARE							
8*	SPARE							

RES2, RES1, RES0 describes number of received residual bits.

*Spare. User may use these bytes.

RLOOK SEGMENT

BRDY means that the transmit buffer is ready. The 2501/11 will send the block only after the CPU makes BRDY = 1. (BRDY is used in conjunction with the SEND bit.) At the completion of the transmission, the 2501/11 will make BRDY = 0, and then read the BRDY of the next segment.

After transmitting a packet, an acknowledgement must be received from the remote device. The acknowledgement is contained in the received N (R) count of an I-frame, RR frame, or RNR frame. Upon acknowledgement, the 2501/11 will make ACK'ED = 1, and generate a block-acknowledged interrupt. Before assigning a new block to a segment in TLOOK, the CPU must make sure that the previous block which used that segment number has been acknowledged.

REC RDY informs the 2501/11 that the receive buffer is ready. The 2501/11 will not receive a packet into a buffer referenced by a particular segment until REC RDY = 1. If the 2501/11 progresses to a segment which has REC RDY = 0, an error interrupt will be generated.

After receiving an error-free packet in proper sequence, the 2501/11 will set FRCML, clear REC RDY, and generate a Packet Received Interrupt. The 2501/11 will also write the value of the binary length of the received packet in RCNT HI and RCNT LO. The NE count is advanced. The 2501/11 will acknowledge received packets at the first opportunity. This will be in either the next transmitted I-frame, or by an RR frame if RECR = 1, or by an RNR frame if RECR = 0. (RECR is in CRO.)

In the address bytes, HI represents the upper 8 bits and LO represents the lower 8 bits. In the count bytes, HI represents the upper 4 bytes.

TSADR is the starting address of the buffer to transmit and TCNT is the binary count of the number of characters in the I-field.

RSADR is the starting address of the receive buffer. After successfully receiving the packets, the 2501/11 will write the value of RCNT which is the binary count of the number of characters in the I-field.

Whether the 2501/11 accesses a look-up table or a memory block a DMA Cycle is required for each access.

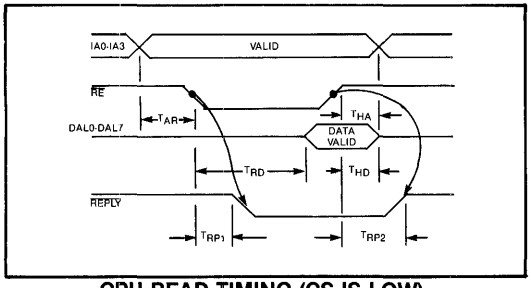
TLOOK AND RLOOK POINTERS

There are three 3-bit counters for the status of the segments in TLOOK and RLOOK. Status Register #0 (SRO) contains counters NA and NB which are used in conjunction with TLOOK. NB is the segment number of the next block to be transmitted, and is advanced at the end of each DMA transmission. NA is the value of the segment of the next block which will be acknowledged. If all transmitted blocks have been acknowledged, then NA = NB.

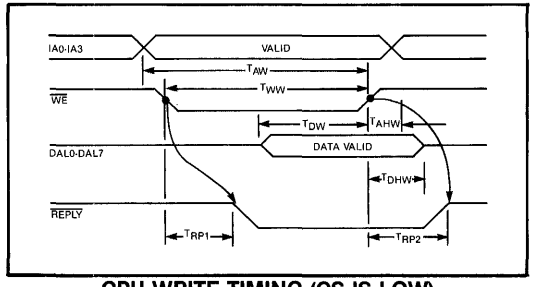
In SR1 is a 3-bit counter, NE, used with RLOOK. NE is the value of the segment number where the next received packet will be placed.

PRELIMINARY TIMING SPECIFICATIONS

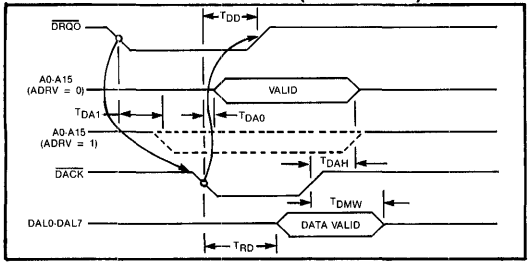
SYMBOL	PARAMETER	MIN. (NS)	MAX. (NS)	COMMENT
T_{AR}	Input Address Valid to $\overline{RE}$	0		
T_{RD}	Read Strobe (or $\overline{DACK}$ Read) to Data Valid		200 375	C (DAL) = 50 pf C (DAL) = 100 pf
T_{HD}	Data Hold Time from Read Strobe		80	
T_{HA}	Address Hold Time from Read Strobe	80		
T_{AW}	Input Address Valid to Trailing Edge of $\overline{WE}$	200		
T_{WW}	Minimum $\overline{WE}$ Pulse	200		
T_{DW}	Data Valid to Trailing Edge of $\overline{WE}$ or Trailing Edge of $\overline{DACK}$ for DMA Write	100		
T_{AHW}	Address Hold Time after $\overline{WE}$	80		
T_{DHW}	Data Hold Time after $\overline{WE}$ or after $\overline{DACK}$ or DMA Write	80		
T_{DA1}	Time from $\overline{DRQO}$ (or $\overline{DRQI}$) to Output Address Valid if ADRV = 1		80	C (ADDRESS) = 100 pf
T_{DA0}	Time from $\overline{DACK}$ to Output Address Valid if ADRV = 0		360	C (ADDRESS) = 100 pf
T_{DD}	Time from Leading Edge of $\overline{DACK}$ to Trailing Edge of $\overline{DRQO}$ (or $\overline{DRQI}$)		200	C ($\overline{DRQ}$) = 50 pf
T_{DAH}	Output Address Hold Time from $\overline{DACK}$		120	
T_{DMW}	Data hold Time from $\overline{DACK}$ for DMA Read		80	
T_{RP1}	$\overline{REPLY}$ Response Leading Edge		160 240	C_{LOAD} = 50 pf C_{LOAD} = 100 pf
T_{RP2}	$\overline{REPLY}$ Response Trailing Edge		200 260	C_{LOAD} = 50 pf C_{LOAD} = 100 pf



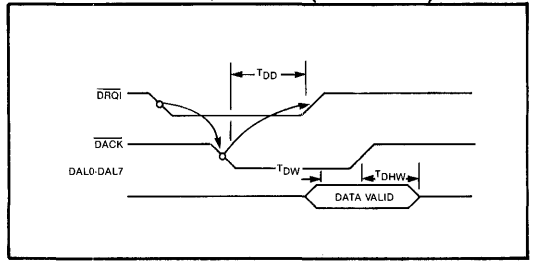
CPU READ TIMING (CS IS LOW)



CPU WRITE TIMING (CS IS LOW)



DMA OUT TIMING



DMA IN (A0-A15 SAME AS DMA OUT)

WD2501/11 ORDERING INFORMATION

PART NO.	MAX. DATA RATE
WD25XX-01	100 KBPS
WD25XX-05	500 KBPS
WD25XX-11	1.1 MBPS

See page 725 for ordering information.

Printed in U.S.A.

PRELIMINARY

WD2520 CCITT #7 Data Link Controller

FEATURES

- Performs most of the controls of the Message Transfer part of CCITT #7.
- Dual Channel DMA for full-duplex operation.
- Unique memory access method for buffer management.
- All formatting of bit-oriented control included: zero bit insertion and deletion. Automatic appending and testing of flags and FCS Fields.
- Automatic control of sequence numbers FSN and BSN, and of control bits FIB and BIB.
- Optional selection of either "Basic" error correction method or the preventive cyclic retransmission error correction method.
- Computer bus interface structure: 8-bit bi-directional data bus. 16-bit address bus for DMA. 4-bit input address bus (may be tied to lower 4 bits of 16 bit address). CS, RE, WE.
- 48-pin dual in-line package. Pin assignment compatible with the WD2501 and WD2511 packet network interface chips.
- TTL compatible.
- Speeds to 1.1MBit/Sec Transmit-Receive Rate.
- Telephone central office signalling.

GENERAL DESCRIPTION

The WD2520 is a MOS LSI device which is compatible with the CCITT Recommendation #7 (Signalling System Number 7). The overall objective of Signalling System #7 is to provide one internationally standardized general purpose common channel signalling system for information transfer within telecommunications networks. (i.e. signalling from one central office switch to another).

The WD2520 performs most of the controls of the Message Transfer Part of CCITT#7. The device includes a unique buffer management scheme with dual channel DMA.

The WD2520 is pin-for-pin compatible with the WD2501/2511 popular Level 2 X.25 controller.

See page 725 for ordering information.

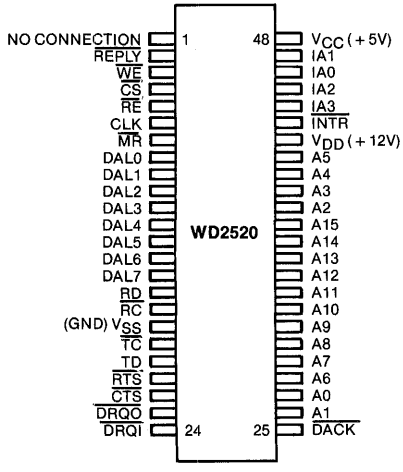


Figure 1.
PIN CONNECTION

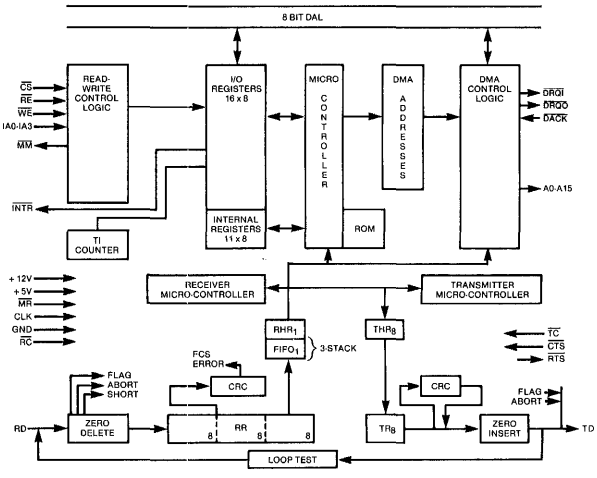


Figure 2. BLOCK DIAGRAM

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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PRELIMINARY

WD2840 Local Network, Token Access Controller

FEATURES

- Broadcast Medium Oriented (Coax, RF, CATV, IR, etc.)
- Up to 254 nodes/1.1 Mbps
- Dual DMA/Highly efficient Memory Block Chaining
- Token based protocol
- Acknowledge option on each datagram
- Adjustable fairness, stations may be prioritized
- Frame format similar to industry standard HDLC
- Supports Global Addressing
- Diagnostic Support: Self-Tests, System and Network
- TTL Compatible

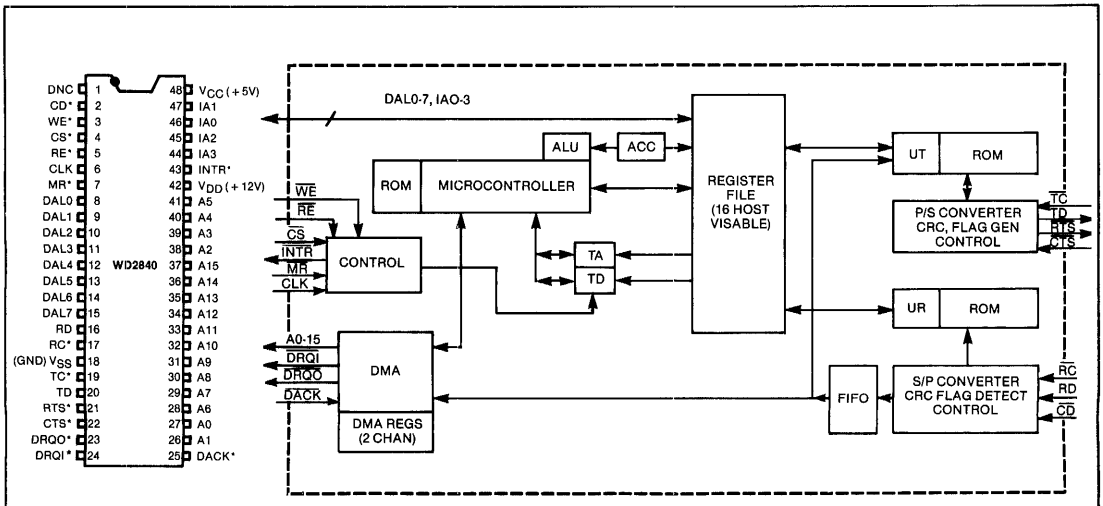
APPLICATIONS

The 2840 is a general purpose Local Network Token Controller applicable to virtually all types of multi-point communications applications. The token protocol allows the sharing of one bus by up to 254 nodes. 2840's will be designed into process control equipment, micro-computers, mini-computers, personal computers, proprietary micro-processor based applications, intelligent terminals, front-end processors, and similar equipment.

The great advantage for the design engineer is the ease with which he can implement a local network function. The 2840 handles autonomously all major communcations tasks as they relate to the local network function.

GENERAL DESCRIPTION

The WD2840 is a MOS/LSI device intended for local network applications, where reliable data communications over a shared medium is required. The device uses a buffer chaining scheme to allow efficient memory utilization. This scheme minimizes the host CPU time requirements for handling packets of data. The WD2840 frees the host CPU from extensive overhead by performing network initialization, addressing, coordination, data transmission, acknowledgements and diagnostics.



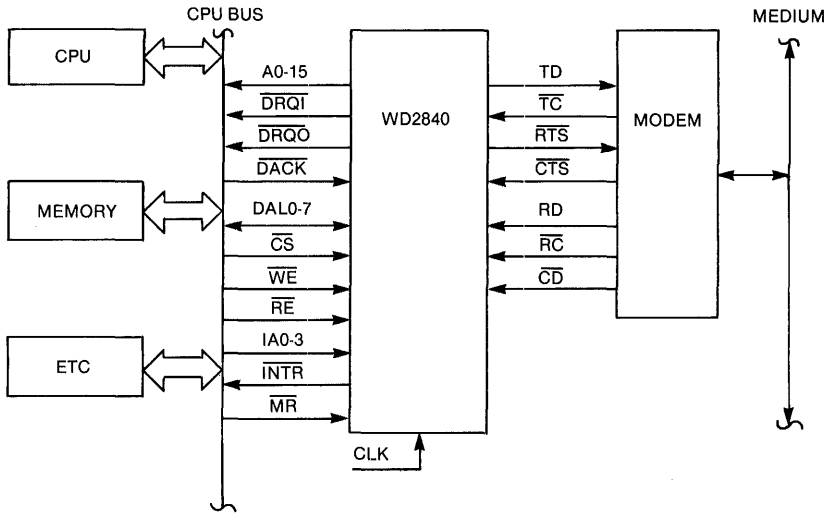
PIN CONNECTIONS

BLOCK DIAGRAM

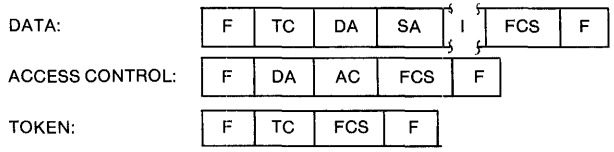
The WD2840 is packaged in a 48 pin DIP. The following is a functional description of each pin. An asterisk after a signal name (SIGNAL*) means active Low.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
48	POWER SUPPLY	V_{CC}	+5VDC power supply input
42	POWER SUPPLY	V_{DD}	+12VDC power supply input
18	GROUND	V_{SS}	Ground
6	CLOCK	CLK	Clock input used for internal timing. Must be square wave and 1.0-2.5 MHz.
7	MASTER RESET	MR*	Initialize on active low for at least 10 ms. All registers reset to zero, except control bits ISOL and ALONE are set to 1. DACK* must be stable high before MR* goes high.
4	CHIP SELECT	CS*	Active low chip select for CPU control of I/O registers.
8-15	DATA ACCESS LINES	DAL0-7	An 8-bit bi-directional three-state bus for CPU and DMA controlled data transfers.
5	READ ENABLE	RE*	The content of the selected register is placed on DAL when CS* and RE* are low.
3	WRITE ENABLE	WE*	The data on the DAL are written into the selected register when CS* and WE* are low. RE* and WE* must not be low at the same time.
43	INTERRUPT REQUEST	INTR*	An active low interrupt service request output. Returns high when Interrupt Register is read.
44-47	ADDRESS LINES IN	IA0-IA3	Four address inputs to the 2840 for CPU controlled read/write operations with registers in the 2840. If ADRV = 0, these may be tied to A0-A3.
26-41	ADDRESS LINES OUT	A0-A15	Sixteen address outputs from the 2840 for DMA operation. If the output control bit ADRV = 1, the outputs are TTL driven at all times. If ADRV = 0, the outputs are tri-state, and are HI-Z whenever DACK* is high.
23	DMA REQUEST OUT	DRQO*	An active low output signal to initiate CPU bus request so the 2840 can output onto the bus.
24	DMA REQUEST IN	DRQI*	An active low output signal to initiate CPU bus requests so that data may be input to the 2840.
25	DMA ACKNOWLEDGE	DACK*	An active low input from the CPU in response to DRQO* or DRQI*. DACK* must not be low if CS* and RE* are low or if CS* and WE* are low.
20	TRANSMIT DATA	TD	Transmitted serial data output.
16	RECEIVE DATA	RD	Receive serial data input.
19	TRANSMIT CLOCK	TC*	A 1X clock input. TD changes on the falling edge of TC*.
17	RECEIVE CLOCK	RC*	This is a 1X clock input, and RD is sampled on the rising edge of RC*.
21	REQUEST-TO-SEND	RTS*	An open collector output which goes low when the 2840 is ready to transmit either data or flags. May be hardwired to ground.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
22	CLEAR-TO-SEND	CTS*	An active low input which signals the 2840 that transmission may begin. May be hardwired to ground.
2	CARRIER DETECT	CD*	An active low input which signals the WD2840 that a frame may be received. CD* should remain active throughout the received frame. The modem may negate this signal if its receive signal quality is below a reliability threshold, ensuring that the 2840 will not accept the frame.
1	DO NOT CONNECT	DNC	Leave pin open.



TYPICAL SYSTEM CONNECTION



FRAME FORMATS

FRAME FORMAT

The frame format the 2840 uses to transmit all data and control frames is similar to the industry standard HDLC. A 16 bit CRC is implemented and standard zero insertion is used for framing. This framing method allows the use of standard network monitoring and diagnostic equipment such as data scopes and logic analyzers.

Additional address fields and control points are defined as required to support the protocol.

Normal Frame Format:

F — TC — DA — SA — I — FCS — F

F = Flag, binary pattern 01111110
TC = Token Control (8 bit)
DA = Destination Address (8 bit)
SA = Source Address (8 bit)
I = Information Field (0 to 2048 bytes) or 16 buffers, whichever is less.
FCS = Frame Check Sequence (16 bit)

Access Control Format:

F — DA — AC — FCS — F

F = Flag, Binary pattern 01111110
DA = Destination Address (8 bit)
AC = Access Control Field (8 bit)
FCS = Frame Check Sequence (16 bit)

Token Pass Format:

F — TC — FCS — F

F = Flag, binary pattern 01111110
TC = Token Control (8 bit)
FCS = Frame Check Sequence (16 bit)

REGISTER DEFINITION

The WD2840 is controlled and monitored by sixteen 8 bit I/O registers:

REG (1)	NAME	DESCRIPTION
0	CR0	Control Register 0
1	CR1	Control Register 1
2(2)	SR0	Status Register 0
3(2)	IR0	Interrupt Type Register
4(2)	SR1	Status Register 1
5(2)	SR2	Status Register 2
6(2)	CTR0	Counter Register 0
7(2)	NA	Next Address
8	TA	ACK Timer
9	TD	Net Dead Timer
A	CBPH	Control Block Pointer (MSByte)
B	CBPL	Control Block Pointer (LSByte)
C	NAR	Next Address, Request
D	AHOLT	Access Hold-Off Limit
E	TXLT	Transmit Limit
F	MA	My Address

(1) = Hexadecimal representation of IA0-IA3.
(2) = CPU read only, write not possible.

Control, status, and interrupt bits will be referred to as CR, SR, or IR, respectively, along with two digits. For example, SR21 refers to status register #2 and bit 1, which is "STATE."

SUMMARY — CONTROL, STATUS, INTERRUPT REGISTERS

REGISTER	BIT # 7	6	5	4	3	2	1	0
CR0	TXDEN	TXEN	RXEN	TOFF	ILOOP	COPY	NOINT	ISOL (1)
CR1 (2)	DIAGC	PIGT	INIT	ADRV	GIRING	0	0	NEWNA
CR1 (4)	DIAGC	0	0	0	DMAT	LOOP	RAMT	NUDIAG
SR0	LASTF	SENDACK	L2	0	BSZ3.....	BSZ2.....	BSZ1.....	BSZ0
SR1	TAOUT	IRTS*	RECIDL	0	0	0	0	0
SR2	NXTTO	NXTRO	TR	ACKRQ	RETRY	TSENT	STATE	INRING
IR0 (2,3)	ITUR	IRUR	INS	ITRAN	IREC	ITOK	ITA	ITD/M

NOTE: Zero bits (0) shown above are reserved and should not be used.

FOOTNOTES:
(1) = Is set to 1 on power-up or master reset.
(2) = Network mode only (CR17 — DIAGC cleared).
(3) = Any bit set causes host interrupt (INTR* goes true) when Master Interrupt Suppress (CR01) is clear. All bits are cleared when register is read by the host.
(4) = Diagnostic mode only (CR17 — DIAGC set). See diagnostic section for register usage in diagnostic mode.

CONTROL REGISTER 0 DEFINITIONS

BIT	NAME	DESCRIPTION
CR00	ISOL	Isolate. Is set after a master reset. Will get reset when the Control Block and other WD2840 registers have been set. When ISOL set, the WD2840 will logically disconnect from the network.
CR01	NOINT	Master Interrupt Suppress. When clear, the 2840 will generate host interrupt requests (INTR* low) if any bit in the 2840 interrupt request register (IR0) is set. When set, only the interrupt request is suppressed, not the setting of bits in IR0.
CR02	COPY	Enables COPY mode, (a diagnostic.)
CR03	ILOOP	Instructs the 2840 to loop data internally from transmitter to receiver. Used with the LOOP diagnostic. Must NOT be set while in network mode.
CR04	TOFF	When set causes 2840 to ignore timers. This is NOT intended to be used in an operational network but is provided to support network diagnosis. CAUTION: This control bit disables all automatic network error recovery.
CR05	RXEN	Receiver Data Enable — When set allows the receiver to DMA appropriate frames into memory.
CR06	TXEN	Master Transmit Enable — When set allows at least non memory referenced transmissions (e.g. ACK and NAK). Must normally be set when TXDEN is set.
CR07	TXDEN	Transmit Data Enable — When set allows transmitter to DMA information from memory and transmit it when access rights (token) are received.

CONTROL REGISTER 1 DEFINITIONS (NETWORK MODE)

BIT	NAME	DESCRIPTION
CR10	NEWNA	Update NA register. When set causes 2840 to copy the contents of register NAR into register NA. The 2840 clears this bit after the function is complete.
CR11	—	(Not used, Reserved.)
CR12	—	(Not used, Reserved.)
CR13	GIRING	Get in logical ring. Instructs the 2840 to gain entry into the logical ring at the next opportunity (i.e. respond to a token pass).
CR14	ADRV	Address Driver Enable. Enables the sixteen output address (A0-A15). If ADRV = 0, the outputs are tri-state and are in HI-Z, except when DACK* is low. If ADRV = 1, the outputs are always TTL levels.
CR15	INIT	Network Initialization Enable. When set, TD timer expiration causes the WD2840 to enter SCAN mode.
CR16	PIGT	Piggy Back Token. If set, instructs the WD2840 to piggy back token on last frame transmitted.
CR17	DIAGC	Enables diagnostic mode. In network mode this bit should be zero.

CONTROL REGISTER 1 DEFINITIONS (DIAGNOSTIC MODE)

BIT	NAME	DESCRIPTION
CR10	NUDIAG	Perform a new diagnostic. When set causes 2840 to perform one of the four diagnostics. The host initializes the appropriate registers for the particular diagnostic and by setting this bit can initiate the test. The 2840 clears this bit after completion of the diagnostic.
CR11	RAMT	Selects internal RAM test when in diagnostic mode.
CR12	LOOP	Selects Loop Test if in diagnostic mode.
CR13	DMAT	Selects DMA Test if in diagnostic mode.
CR14	—	(Not used, Reserved.)
CR15	—	(Not used, Reserved.)
CR16	—	(Not used, Reserved.)
CR17	DIAGC	Enables diagnostic mode.

STATUS REGISTER DEFINITION

BIT	NAME	DESCRIPTION
SR00-SR03	BSZ0-BSZ3	Buffer Size, multiples of sixty-four bytes (the multiple ranges from 0 to 15, meaning buffers are 64 to 1024 bytes).
SR04	—	Not used.
SR05	L2	An internal flag set during frame transmission if the length value of the current frame is equal to eight.
SR06	SENDACK	An internal flag set during data frame reception to indicate that the incoming frame should be acknowledged (send ack/nak frame). This flag is cleared when the acknowledgement has been transmitted.
SR07	LASTF	An internal flag set during data frame transmission to indicate that the current frame will be the last to be transmitted during this access period.
SR10-SR14	—	(Not used, Reserved.)
SR15	RECIDL	Receiver Idle.
SR16	IRTS*	Internal Request To Send. Indicates the transmitter is attempting (successful or not) to send either data or flags. If the RTS* pin is not tied to ground or WIRE-ORED with another signal, then IRTS* = $\overline{RTS}$.
SR17	TAOUT	Timer TA expired.
SR20	INRING	In logical ring. Indicates the node has had the token and has successfully passed it at least once (therefore it is included in a logical ring of at least two nodes).
SR21	STATE	Mode confirmation. Depending on DIAGC (CR17), the 2840 is either in Isolate or Diagnostic state. When ISOL (CR00) is set, STATE set confirms the 2840 is not in Network State. When ISOL is clear, STATE clear confirms Network State.
SR22	TSENT	An internal flag. TSENT is set when the 2840 passes the token. It may have been either a piggyback or explicit token pass frame. TSENT is cleared when the next frame is received.
SR23	RETRY	An internal flag which is set when either a data frame or a token pass frame must be retransmitted.
SR24	ACKRQ	An internal flag set during data frame transmission if an acknowledgement is requested for the specific frame.
SR25	TR	An internal flag set when the 2840 receives a token passed to it. It is cleared when the token is passed (or if it is ignored for any reason).
SR26	NXTR0	Internal Receive Buffer Pointer State. When set it indicates the 2840 has the address of the next buffer and that all prior frames (denoted by posted FSB's) can be removed from the chain for received frame processing by the host. When NXTR0 is clear it indicates that the 2840 has advanced to a zero link (end of chain).
SR27	NXTT0	Internal Transmit Buffer Pointer State. When NXTTO is set it indicates that the 2840 has the address of the next frame to transmit in its internal register. However when clear, it indicates that the transmit chain internal register points to the link field of the last buffer of the last transmitted frame.

INTERRUPT REGISTER DEFINITION

The setting of any bit in this register by the 2840 causes an interrupt ($\overline{INTR}$ = true). The reading of this register clears all bits.

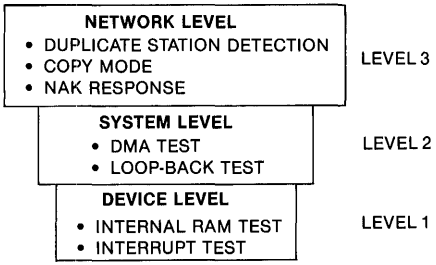
BIT	NAME	DESCRIPTION (1)
IR00	ITD/M	Network dead. Timer TD expired.
IR01	ITA	Data Frame Transmission unsuccessful. NAK or no response after two tries. Exact cause is determined by reading appropriate FSB.
IR02	ITOK	The token has been received.

BIT	NAME	DESCRIPTION
IR03	IREC	Indicates data frame(s) have been received with address destined for this 2840.
IR04	ITRAN	Indicates data frames have been transmitted. The number of frames transmitted and the status of each (e.g. ACK/NAK Retry Count) is determined by following the transmit chain and interrogating the FSB's.
IR05	INS	New successor. The 2840 has identified a new successor in the logical ring.
IR06	IROR	Receiver over-run.
IR07	ITUR	Transmitter under-run.

[1] = Non diagnostic mode only.

DIAGNOSTIC MODES

The WD2840 has been designed to support (3) three levels of diagnostics. These levels shown in the diagram can be used separately or together to perform such varied tasks as receiving inspection to network fault isolation. As is shown in the diagram, each level is actually composed of modules which test particular areas of each level.



Diagnostic Mode Control

CR00 ISOL	CR17 DIAGC	SR21 STATE	MEANING
1	0	0	2840 "Isolated." Power up condition or isolate request.
0	0	0	2840 active.
1	0	1	Isolate request function confirmed.
1	1	0	Host request to enter diagnostic mode.
1	1	1	Diagnostic mode confirmed. Diagnostic functions of CR1 apply.
0	1	0	Illegal
0	1	1	Illegal
0	0	1	Illegal

Once in diagnostic mode, the desired test is selected via CR1. Specific tests, and expected results, are described below.

LEVEL 1, DEVICE SELF-TESTING

There are two self-test features: 1) Internal Ram Test, and 2) Interrupt Test. Both tests are suitable for manufacturing testing and user incoming inspection testing.

These self tests may be instigated by the user anytime the 2840 is in diagnostic mode. This mode may be entered after power-up or from network mode by manipulation of the mode control bits. The mode transition is confirmed by the 2840 via the DIAG status bit.

Internal RAM Test

There are eleven eight bit registers in the 2840 which are not directly accessable by the users CPU. This test provides a means to check those registers. The contents of register A are placed in six even internal registers, and the contents of register B in five odd internal registers. The eleven registers are then added together without carry and the result is placed in registers 2, 5, 6, 7.

Use the following procedure to initiate the RAM test:

1. Enter diagnostic mode.
2. Set up registers A and B
3. Set RAMT.
4. Set CR10.
5. Wait for CR10 to be cleared.
6. Read registers 2, 5, 6 and 7.
7. Clear RAMT.

Interrupt Test

This test is to validate the correct operation of the interrupt sub-system. This test reads value of registers 8 through F and it compares the lower half (bits 3-1) of each register to the upper half (bits 7-5) of the same register. If the comparison fails an interrupt bit is set. Interrupt bits IR00 to IR07 correspond to comparison test of register 8 to F respectively.

LEVEL 2. SYSTEM DIAGNOSTICS

DMA Test

This test verifies proper operation of the DMA subsystem by reading the value from a register and writing it into the user memory. Then reading the value from the same location and writing it into another register.

The value is read from register C. Using the transmitter DMA sub-system, it is written into memory location addressed by the register A and B (location N). The receiver DMA sub-system is used and contents of the same address is read and it is stored into the register 7. Next the receiver DMA is used and the contents from register D is written into location N + 1. The transmitter DMA reads the value from location N + 1 and stores it into register 6.

It is the host responsibility to check if the contents of registers C and register 7 and memory location N match. The same is true for registers D and 6 and memory location N + 1.

Loop Back Test

The 2840 is able to tests its parallel to serial and serial to parallel converters, CRC, and framing logic by sending a known pattern to itself and verifying its correct reception. The pattern is looped internally to the device if ILOOP (CR03) = 1, or may be looped externally (with outside logic) if ILOOP (CR03) = 0.

The following procedure should be followed in order to run the loop-back test:

1. Enter diagnostic mode.
2. Set up register A and B to point to a buffer that is initialized with a pattern for transmission.
3. Set up register C and D to point to a buffer to receive the frame. (It is a good practice to initialize this buffer with all '00' or all 'FF' value bytes.)
4. Set up the buffer size in bits 3-0 of register E. (NOTE: In this test the last two bytes of the buffer will not be transmitted.)
5. Set ILOOP bit (CR03). (This is optional, if internal loop-back test is desired.)
6. Set LOOP bit (CR12).
7. Set CR10.
8. Wait for CR10 to be cleared.
9. Compare the two buffers to verify correct reception of the frame.

LEVEL 3. NETWORK DIAGNOSTIC

Duplicate Station Detection

Duplicate stations (more than one station with the same address) can result from the faulty programming of internal register MA (due to wrong address switch settings on the user's device, for example). This is expected to occur often enough to warrant the addition of a detection algorithm in the users 2840 initialization procedure.

After initializing all required parameters, the user places the 2840 in network mode (by setting ISOL false). The 2840 monitors all frames on the network. If one is observed as having been transmitted by it's address (source address of the frame equals the value in register MA), an event counter is incremented.

The user should monitor the SA-MA event counter at least long enough for the token to have circulated all the way around the access ring (time is configuration dependent) before enabling the 2840's transmitter.

It is useful to note that this constraint requiring each node which is participating in the network logical ring to have a unique address does not extend to nodes which are "listening" but not "in the ring." It might be useful to a network designer to have groups of receive only nodes which have the same node address but do not participate in the network token passing (see GIRING — CR13). Data frames transmitted to such clusters must not request acknowledgement since all nodes in the cluster would simultaneously respond.

Copy Mode

The COPY Mode is selected by setting the COPY control bit (CR02). Normally the 2840 receives (DMA's into the receive buffer chain) data frames only if they contain the general broadcast destination address or if they are specifically addressed to the 2840. This occurs when the frame's destination address (DA) matches the 2840 node address in register MA (set by the host).

However, when COPY mode is selected data frames which are specifically addressed to other nodes will be treated as broadcast frames by this node. The COPY mode allows a specific node to "evesdrop" on data frame traffic on the network.

NAK Response

The 2840 sends negative acknowledgements (NAK's) on response to received frames under several circumstances. The NAK prevents the transmitting node from wasting bandwidth retrying indiscriminately, and further, lends visability to individual network node problems. The NAK includes a reason code which is available to the transmitter's software (via the TFSB).

Each data frame to be transmitted can be specifically marked (via the FSB) by the host to require an ACK/NAK response from the receiving 2840. In the absence of errors, an Acknowledge (ACK) frame will be returned to the transmitter as confirmation.

However, several circumstances cause a Negative Acknowledge (NAK) to be returned:

1. Insufficient buffer space
2. Receiver not enabled (RXEN — CR05 cleared)
3. Receiver overrun
4. Frame exceeded 16 buffers in length

2.0 INTERFACES

There are two interfaces to the 2840: the host computer side, and the network side. The network side is conventional from an electrical point of view, the 2840 performs all logical functions required to ensure communications capability on broadcast media (such as coax or RF).

The host interface involves two separate functional interfaces: the status/control registers described in section one, and a DMA interface that is described in the next subsection.

2.1 HOST

The 2840 uses a complex memory buffer architecture allowing it to respond in real time to its network obligations (e.g., to meet network data rate and processing delay requirements). These memory structures are managed cooperatively by the host and the 2840.

Memory management functions requiring real time response (e.g. traversing chains) are completely handled by the 2840. Other important, but not time critical operations are the responsibility of the host software (such as removing used buffers from the transmit chain).

All memory references by the 2840 are pointed to by memory locations (and internal registers) initially defined and set up by software. Initial values and memory based registers are grouped together and called the 2840 Control Block.

The location of this control block is written into the registers CBPH and CBPL anytime the 2840 is in Isolate State. This control block has the following structure:

CBP →	+0	NXTR (H)	Receive Buffer Chain (MSByte)
	+1	NSTR (L)	Receive Buffer Chain (LSByte)
	+2	NXTT (H)	Transmit Buffer Chain (MSByte)
	+3	NXTT (L)	Transmit Buffer Chain (LSByte)
	+4	BSIZE	Buffer Size / 16 (O-F = 64-1024 bytes)
	+5	EVT0	Eleven separate Event
	+6	EVT1	Counters.
	***		
	+F	EVT10	

As the 2840 transitions to Network State, it reads and uses the first five bytes of the control block. The remaining eleven bytes of event counters are accessed by the 2840 only when each specific event condition occurs.

Either the Receive (NXTR) or Transmit (NXTT) chain entries in the control block may initially be zero; in such a case the 2840 expects the chain to be extended by the host's changing the zero link field in the control block. Thereafter any such zero link would be in a buffer.

The 2840 uses consistant size buffers, their length is set by the value in location BSIZE. The buffer size is indicated by a 4-bit count in the least significant 4 bits of the BSIZE byte in the 2840 control block. The buffer sizes available are multiples of 64; BSIZE value 64 is the buffer size used by the 2840. Thus a BSIZE range of 0-15 corresponds to actual buffer sizes of 64 through 1024 bytes. This buffer length is inclusive of control bytes and buffer link pointers.

The 2840 includes a chained-block feature which allows the user more efficient use of memory, particularly in situations where the maximum packet size is much larger than the average packet size. One or up to 16 buffers may make up a frame but only one frame is allowed per buffer.

Byte counters are associated with each frame (at the memory interface, not actually transmitted within the frame) so that frames on the network need not be integer multiples of buffers. The byte counters include all buffer management overhead. Therefore, a frame consists of 100 transmitted bytes, occupying two 64 byte buffers, would have a byte count of 108.

Since the 2840 receive and transmit buffer chains are linked lists and are "followed" by the 2840 but managed by the host; it is expected that the host will maintain both a FIRST and a LAST address for each chain. On transition into Network State, the chain origin information in the 2840 control block is the same as FIRST. In fact, since the 2840 does not change these control block entries, they can be maintained directly as FIRST by the host. An explicit LAST could be placed in an extended control block section.

The 2840 "follows" the linked buffer chains by maintaining a NEXT address internally for each chain. This NEXT address can be in one of two states: 1) it can be the address of the next buffer in the chain, or 2) at the chain end (zero link), it can be the address of the buffer containing the zero link. The 2840 uses a status bit for each chain; NXTRO (receive) and NXTTO (transmit). When set they indicate the 2840 chain NEXT address is in state 1 above; when clear they indicate state 2 above. This is an IMPORTANT distinction since it indicates whether the last buffer posted in a chain can be removed by the host (because the 2840 has advanced to the buffer beyond) or must be left until the chain can be extended so the 2840 can advance.

The host software monitors the progress of the NEXT pointer, and updates FIRST and LAST as it adds (and removes) buffers to (from) the chains as required. The

2840 provides Interrupt Events (see IRO) and NXTRO, NXTTO status bits to indicate when it advances along the two chains and exactly what state its NEXT address registers are in.

"Deadly Embrace" Prevention

A "Deadly Embrace" can occur when two processors reach a state here each is waiting for the other. In this case, the two processors are the user's CPU and the micro-controller inside the 2840. Therefore, to prevent the "deadly embrace," the following rule is obeyed by the 2840 and should also be obeyed by the user's CPU. This rule applies to the 2840 memory registers and to the I/O registers. The Error Counters are an exception to this rule.

RULE:
If a bit is set by the CPU, it will not be set by the 2840, and vice versa. If a bit is cleared by the 2840, it will not be cleared by the CPU, and vice versa.

As an example, the NEWNA (CR10) control bit is only set by the host and is only cleared by the 2840.

Dual DMA

The 2840 may, for efficiency, interleave frame data fetch/store operations with fetches and stores of pointers and flags in memory. In all cases, operation sequencing is such as to prevent deadlocks and ambiguities between the 2840 and software.

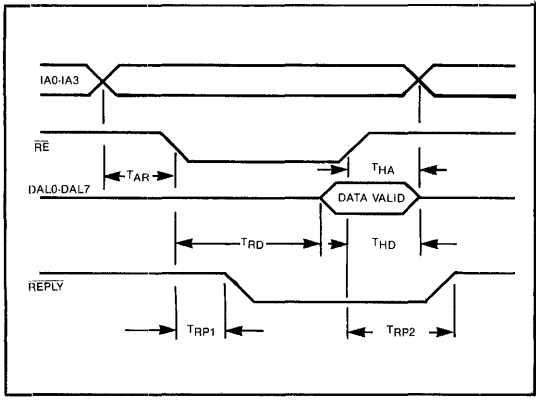
Event Counters

Several non-fatal logical events are tabulated by the 2840 and made visible to the host via memory based event counters The 2840 will increment each counter at the occurence of the specified event. However, the 2840 will not increment past 255 (all 1's). The host has the responsibility of clearing each counter.

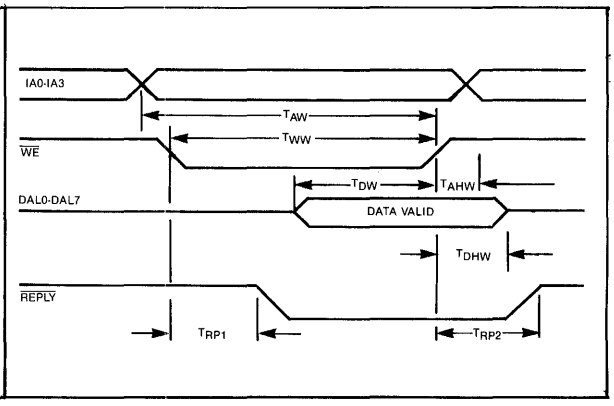
COUNTER	DESCRIPTION
EVT0	"Set scan mode" frame received from the network. The NA register was redefined to MA + 1 at the time.
EVT1	Transmission error first attempt, second try successful. Can only occur for frames requiring an acknowledgement. It indicates no response was received for the first transmission; however, the second transmission was either ACK'ed or NAK'ed.
EVT2	Transmission error. Attempt aborted due to either transmitter underrun or frame length exceeded 16 buffers.
EVT3	Timer TD (network dead) expired.
EVT4	Access Control Frame Reception Error. A one or two byte supervisory frame (ACK/NAK, Token Pass, Scan Mode) has been received in error. This may be due to an FCS error, frame abort, or carrier lost detection.
EVT5	Data Frame Reception Error. An incoming data frame was incorrectly received due to an FCS error, frame abort, or carrier lost detection.
EVT6	NAK sent. Can occur for any of the following reasons: 1. Insufficient buffers in chain 2. Receiver not enabled (RXEN clear) 3. Receiver overrun 4. Frame length exceeded 16 buffers
EVT7	Invalid frame received. Caused by the detection of certain abnormal network conditions such as receiving an ACK/NAK frame when not expecting one, receiving a Scan mode frame when expecting an ACK/NAK frame, or receiving an invalid supervisory frame.
EVT8	Duplicate token detected. This counter will be incremented when the 2840 determines that more than one token exists in the network logical ring. This happens if a token pass is received when the 2840 already has the token, or a data frame is received when the 2840 is waiting for an acknowledgement frame.
EVT9	Diagnostic state pass count. Counted each time the 2840 begins to execute the selected set of diagnostics.
EVT10	Duplicate node address. This counter will be incremented when a data frame being DMA'ed into memory has a source address (SA) equal to the 2840 node address (MA). This counter when used with COPY mode (CR02) is useful for detecting other nodes with the same node number (MA).

PRELIMINARY TIMING SPECIFICATIONS

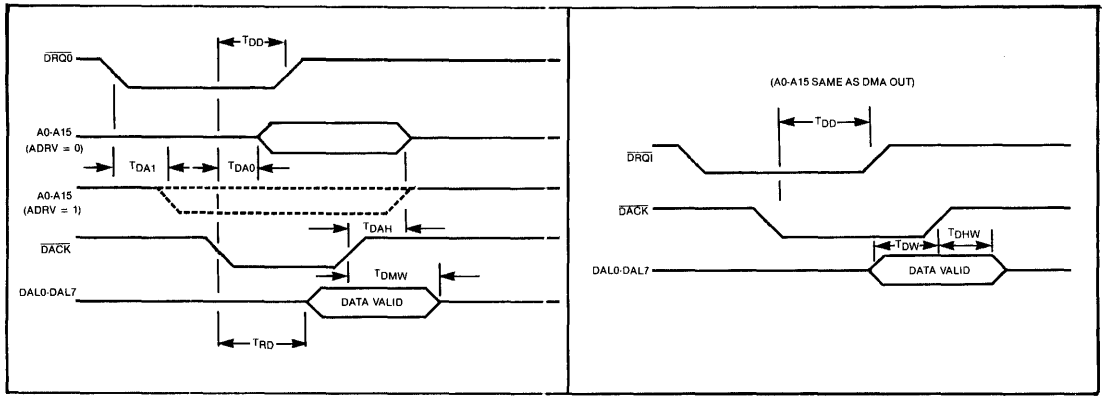
SYMBOL	PARAMETER	MIN. (NS)	MAX. (NS)	COMMENT
T_{AR}	Input Address Valid to $\overline{RE}$	0		
T_{RD}	Read Strobe (or $\overline{DACK}$ Read) to Data Valid		200 375	C (DAL) = 50 pf C (DAL) = 100 pf
T_{HD}	Data Hold Time from Read Strobe		80	
T_{HA}	Address Hold Time from Read Strobe	80		
T_{AW}	Input Address Valid to Trailing Edge of $\overline{WE}$	200		
T_{WW}	Minimum $\overline{WE}$ Pulse	200		
T_{DW}	Data Valid to Trailing Edge of $\overline{WE}$ or Trailing Edge of $\overline{DACK}$ for DMA In	100		
T_{AHW}	Address Hold Time after $\overline{WE}$	80		
T_{DHW}	Data Hold Time after $\overline{WE}$ or after $\overline{DACK}$ or DMA In	80		
T_{DA1}	Time from $\overline{DRQO}$ (or $\overline{DRQI}$) to Output Address Valid if ADRV = 1		80	C (ADDRESS) = 100 pf
T_{DA0}	Time from $\overline{DACK}$ to Output Address Valid if ADRV = 0		360	C (ADDRESS) = 100 pf
T_{DD}	Time from Leading Edge of $\overline{DACK}$ to Trailing Edge of $\overline{DRQO}$ (or $\overline{DRQI}$)		200	C ($\overline{DRQ}$) = 50 pf
T_{DAH}	Output Address Hold Time from $\overline{DACK}$		120	
T_{DMW}	Data Hold Time from $\overline{DACK}$ for DMA Read		80	
T_{RP1}	$\overline{REPLY}$ Response (Leading Edge)		160 240	C_{LOAD} = 50 pf C_{LOAD} = 100 pf
T_{RP2}	$\overline{REPLY}$ Response (Trailing Edge)		200 260	C_{LOAD} = 50 pf C_{LOAD} = 100 pf



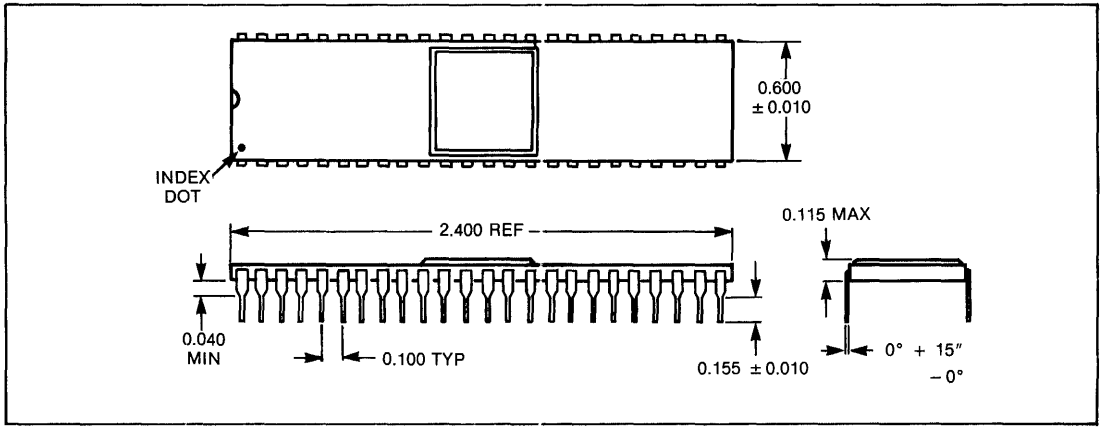
CPU READ ($\overline{CS}$ IS LOW)



CPU WRITE ($\overline{CS}$ IS LOW)



DMA OUT **DMA IN**



WD2840 CERAMIC PACKAGE

See page 725 for ordering information.

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PRELIMINARY

WDK25001 PACKIT

FEATURES

- X.25 (WD2501 OR WD2511) NETWORK CONTROLLER
- BAUD RATE GENERATOR
- RS-423 INTERFACE
- 8 SOCKETS FOR OPTIONAL USER RAM, ROM, EPROM
- WIRE-WRAP HOST INTERFACE AREA
- INTERNAL DATA RATE TO 64 KBPS
- +5°C TO +50°C OPERATION

GENERAL DESCRIPTION

The Western Digital WDK25001 PACKIT is a preconfigured breadboard designed to be an instant development tool for the implementation of bit-oriented, full duplex, serial X.25 data communication systems. Most of the hardware interfacing (Level 1/2 interfacing) is already done on the board. Level 2/3 interfacing is described in the long form specification. To perform Link Control (Level 2) functions, the PACKIT utilizes the Western Digital LSI Packet Network Interface Device. Two versions of the LSI Packet Network Interface Device are available for use with the PACKIT: the WD2501 and the WD2511. The WD2501 LSI device handles the LAP (Link Access Procedure). The WD2511 LSI device handles LAPB (Link Access Procedure Balanced).

The PACKIT is composed of two major physical areas. One side of the printed circuit board contains the factory installed circuitry required to perform X.25 Link Level operations: the other side of the circuit board contains the wire-wrapping area for user implementation of the individual system design.

The wire-wrapping area of the circuit board is designed to accommodate any industrial standard IC package. IC width is defined in 0.15 inch increments, with IC pin separation of 0.1 inch. The wire-wrap area is large enough to permit the installation of approximately one hundred 16-pin IC's.

ORGANIZATION

The WDK25001 "PACKIT", is composed of two major physical areas. The printed circuit area contains factory installed circuitry which handles the Packet Network Interface device, programmable bit rate generator, memory address decoder, and the EIA RS-423 interface. The wire-wrap area is set up to allow the user to design and implement their own host interface and or level 3 and higher modules.

INTERFACES

The PACKIT interfacing (Level 1/2) is divided into two classifications: the user interface and the serial communications interface.

USER INTERFACE

Voltage Levels:

TTL

Architecture:

Microprocessor interface oriented. 16 Address lines, 8 data lines, 10 control lines.

SERIAL COMMUNICATIONS INTERFACE

Electrical Characteristics:

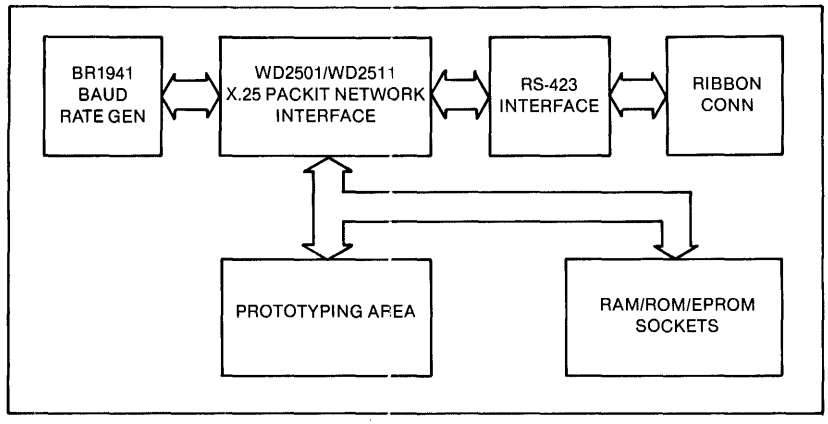
RS-423

Mode:

Synchronous, Bit stuffing oriented, full-duplex, X.25 Asynchronous Response Mode (WD2501) or X.25 Asynchronous Balanced Mode (WD2511).

Clock Rates:

Independent transmit and receive clocks. Either internal or external clock source, selected by jumper strapping. Internal clock rates selectable by DIP switches or under user program control via the User Interface.



PACKIT BLOCK DIAGRAM

ELECTRICAL SPECIFICATIONS

Voltage Requirements:

+5v, +/− 5%
+12v, +/− 5%
−5v, +/− 5%

Maximum Voltage Ripple:

100mv, PTP

Factory-Installed Circuitry Power Requirements:

+5v @ .76A (max.)
(No memory device) +12v @ .20A (max.)
−5v @ .04A (max.)

MEMORY SPECIFICATIONS

Maximum Size Allowable:

64K x 8.

Memory Type:

8-bit wide RAM, ROM, EPROM

Package Type:

24-pin or 28-pin

ENVIRONMENTAL SPECIFICATIONS

Operating Temperatures:

+5 to +50 °C (Maximum temperature is reduced by 1.8 degree centigrade per 1000 meters altitude above sea level.)

Relative Humidity:

10 to 95%, maximum wet bulb of 32 degrees Centigrade and a minimum dew-point of 2 degrees Centigrade (90 degrees and 36 degrees Farenheit, respectively.)

PHYSICAL DIMENSIONS

Size:

Single printed circuit board, 8 inches by 14 inches (203.2 by 355.6mm)

Weight:

2 Pounds (0.907Kg).

THE LSI PACKIT NETWORK INTERFACE DEVICE

The Packit Interface Device is a 48-pin, n-channel silicon-gate, MOS chip designed to perform CCITT X.25 Level 2 (link control), with selected enhancements. In addition to the link control functions required by X.25, the Device eliminates the need for separate DMA circuits, timing chips, and the system software previously required to perform the link control between a data terminal equipment (DTE) and a data circuit-terminating equipment (DCE).

The WD2501/WD2511 interfaces directly with the on-board memory (when installed) or with the user's memory data and address lines. The WD2501/WD2511 is controlled through nine user interface lines: Master Reset ($\overline{MR}$), $\overline{REPLY}$, DMA Request Out ($\overline{DRQO}$), DMA Request In ($\overline{DRQI}$), DMA Acknowledge ($\overline{DACK}$), Interrupt Request ($\overline{INTR}$), Write Enable ($\overline{WE}$), Read Enable ($\overline{RE}$), and Chip Select ($\overline{CS}$).

Additionally, the WD2501/WD2511 is driven by the 1 MHz system clock.

THE PROGRAMMABLE BIT RATE GENERATOR

Circuit board IC location U3 contains a Western Digital BR1941 Programmable Bit Rate Clock. This n-channel MOS silicon-gate device is capable of generating sixteen externally selected clock rates, where-of six are standard rates.

The bit rate for both transmit and receive frequencies may be selected independently through the on-board

DIP switch, S1, or through the user's program via the TA, TB, TC, TD, RA, RB, RC, and RD user interface control lines.

To further increase PACKIT flexibility, the bit rate generator is installed in an IC socket to enable easy removal for specialized user bit rates not conforming to those available from the BR1941.

PACKIT MEMORY

Located on each PACKIT printed circuit board are eight 28-pin IC sockets designed for optional user-installed RAM, ROM, or EPROM memory chips. These sockets present the user with the option of either using the system memory or off-loading the PACKIT memory functions to on-board memory of the user's choice. Once the optional memory is installed it may be accessed by both the user's computer and by the WD2501/WD2511 Network Interface Device via DMA.

NOTE:
All memory devices installed on the PACKIT board must be 8-bit wide devices. Total memory installed must not exceed 64K-bytes.

The design of the memory sockets permits the user a wide range of RAM, ROM, and EPROM selectability. Memories such as the 4802 (2K x 8 RAM), 4118 (1K x 8 RAM), and the 2716 (2K x 8 EPROM), allow the user to select the type, capacity, and expense of memory desired for each individual application.

Also, the design of the sockets provides for the use of either 28-pin or 24-pin memory circuits. If a 24-pin circuit is to be installed, the chip is simply inserted in a manner that places pin 1 of the memory chip in IC socket position 3. Polarization of the sockets is indicated by a white dot, on the PC board, adjacent to both Pin 1 and Pin 3 of the socket.

When calculating the size of on-board memory, for a particular application, it is imperative that the user remember that the on-board memory must be large enough to contain five major arrays.

1. The data to be transmitted,
2. The data received,
3. The transmit-data look-up table (TLOOK),
4. The receive-data look-up table (RLOOK),
5. The PACKIT error counters.

For a detailed description of the use of memory by the Packit Network Interface Device, refer to the WD2501/WD2511 Long Form Specification.

Industrial standard memory types like 4118 or 4801 (1K x 8), 4802 or 2716 (2K x 8), and 37000 or 2764 (8K x 8) can be used in the PACKIT.

THE EIA RS-423 INTERFACE

The communications link between the Western Digital PACKIT and the Data Communications Equipment (DCE) is provided through the EIA RS-423 interface. This interface contains a subset of the RS449 signals. The interface signals are supplied to a 40-pin ribbon cable connector. Each of the RS-449 signals are buffered by 26LS29-type RS-423 line drivers and 26LS32 RS-423 line receivers.

If RS-232-C interfacing is desired, instead of RS-449 interfacing, the ribbon connector may be jumpered to provide RS-232-C signal compatability. However, due to differences in signal voltage levels, certain precautions must be taken when converting to RS-232-C interfacing.

BIT RATE GENERATOR — PROGRAMMING AND STRAPPING

The Western Digital BR1941 Bit Rate Generator, on board the PACKIT, may be programmed for receive and transmit bit rate, by on-board switch setting or by program command from the user circuitry. The selection between these two options is controlled by the S1 switchpack. To use program control all switches of S1 must be in the "OFF" position otherwise the bit rate is the "wired-and" of the program control and the setting of the switches. Transmit and receive bit rates are independently selected.

Program control of the bit rate, when enabled, is received by the PACKIT via the TA, TB, TC, and TD jumper pads, for the transmit bit rate, and via the RA, RB, RC, and RD jumper pads, for the receive bit rate. (Each of these control lines is tied to +5v via a 2.2K resistor pull-up.)

THE PACKIT USER INTERFACE

The Western Digital PACKIT user interface defines all of the signals available to the user. These signals include: the microprocessor oriented address, data, and control lines, the RS-423 communications interface signals, the programmable bit rate generator control lines and on-board strapping.

USER INTERFACE SIGNALS

The user designed circuitry interfaces with the PACKIT through the interface signal jumper pads located at the center of the PACKIT PC board. The signals are listed in the table on following page. Signals are defined as "IN", "OUT", or "BI", to denote input from or output to the user interface, or bidirectionality, respectively. RS-449 mnemonics are presented in parenthesis.

USER INTERFACE SIGNALS

SIGNAL NAME	DIR	SIGNAL DEFINITION
A0-A15	BI	The sixteen memory address lines. These lines may be connected to the user's memory address bus or to the PACKIT on-board optional memory chips, when installed. These lines also carry the memory address outputs of the Packit Network Interface Device for DMA operations.
D0-D7	BI	The eight bit data lines used to transmit and receive byte-oriented data between the interface chip and the user circuitry. These lines also carry data between the WD2501/WD2511 and the optional on-board memory (when installed).
TMI (TM)	OUT	Test mode Indication. Signal returned from the RS-423 communications interface indicating that the local DCE is in the test mode. This signal is propagated to the user interface.
RDY REC (RR)	OUT	Ready to receive. Signal returned from the RS-423 communications interface indicating that the communications link is ready to receive data. This signal is propagated to the user interface.
$\overline{\text{DACK}}$	IN	DMA Acknowledge. The CPU signal generated in response to the WD2501/WD2511 transmitted DRQO or DRQI DMA request signals. An active low, sent to the PACKIT, on this line informs the PACKIT that the DMA request is acknowledged and the CPU has relinquished control of the system bus.
$\overline{\text{DRQI}}$	OUT	DMA Request IN. The WD2501/WD2511 requests a DMA bus access. A $\overline{\text{DRQI}}$ is a request for a transmission of data FROM the memory TO the WD2501/WD2511. This signal is active low.
$\overline{\text{DRQO}}$	OUT	DMA Request OUT. The WD2501/WD2511 initiated signal requesting access for a DMA data transfer. The $\overline{\text{DRQO}}$ signal requests a DMA cycle to enable transfer of data FROM the WD2501/WD2511 TO the memory. This signal is active low.
$\overline{\text{MR}}$	OUT	Master Reset. The master reset, generated by the on-board RESET momentary closure switch, clears all of the WD2501/WD2511 control and status registers, with the exception of two internal control bits (refer to the WD2501/WD2511 Long Form Data Sheet, sheet 2). This signal is active low.
$\overline{\text{INTR}}$	OUT	Interrupt Request. The WD2501/WD2511 issues $\overline{\text{INTR}}$ to request an interrupt. This signal is active low.
$\overline{\text{CS}}$	IN	Chip Select. $\overline{\text{CS}}$ is driven low, by the user's circuitry to enable the WD2501/WD2511 for programmed I/O read or write operations. $\overline{\text{CS}}$ may be permanently activated by jumpering pad location S11 to ground.
DATA MODE (DM)	OUT	The DATA MODE signal is returned from the communications link, over the RS-423 interface, to inform the PACKIT that the data link is in the data mode.
$\overline{\text{REPLY}}$	OUT	Reply. An active low signal, generated by the WD2501/WD2511 to indicate that it is selected ($\overline{\text{CS}}$ is low) and it is either read enabled ($\overline{\text{RE}}$ is low) or it is write enabled ($\overline{\text{WE}}$ is low).
$\overline{\text{MWE}}$	IN	An active low signal generated by the user's system to enable the PACKIT on-board memory chips for a memory-write operation. Not applicable on 24-pin memories. All 24-pin memories are enabled through the J2-0 through J2-7 interface signal lines. This signal is connected to pin 27 of all 28-pin memories.
J2-0 to J2-7	IN	User activated signal lines to individually enable each of the PACKIT on-board memory sockets. Each active low signal enables the Write Enable ($\overline{\text{WE}}$) input of the respective memory socket where: J2-0 write-enables memory socket U13 J2-1 write-enables memory socket U14 J2-2 write-enables memory socket U15 J2-3 write-enables memory socket U16 J2-4 write-enables memory socket U17 J2-5 write-enables memory socket U18 J2-6 write-enables memory socket U19 J2-7 write-enables memory socket U20 Each signal is connected to Pin 23 of the corresponding memory socket.

CONTINUED USER INTERFACE SIGNALS

SIGNAL NAME	DIR	SIGNAL DEFINITION
TA, TB, TC, TD	IN	These four inputs combined select the Transmit bit rate to be generated by the Western Digital BR1941 Programmable Bit Rate Clock. The values presented to the bit rate clock generator, over these lines, may be determined either by the user program or by on-board switch setting, as determined by switch-pack S1.
REMOTE LOOP TEST (RL)	IN	When activated, the REMOTE LOOP TEST line forces the communications link into a diagnostic test. Data is transferred from the memory, to the communications link, to the remote DCE, and back to the PACKIT for verification.
TERM RDY (TR)	IN	Terminal Ready. Input line to the PACKIT, from the user circuitry, informing the DCE that the PACKIT is ready to set-up the communications link. This signal is optionally generated, on a permanent basis, by the PACKIT when jumper S12 is connected to ground.
LOCAL LOOP TEST (LL)	IN	The LOCAL LOOP TEST performs a diagnostic operation similar to that of the REMOTE LOOP TEST with the exception that the data being tested is transmitted to the local DCE and then returned to the PACKIT for verification.
$\overline{\text{MOE}}$	IN	Memory Output Enable. A user supplied low active signal used to enable the 3-state output of the optional on-board PACKIT memory, when installed. This signal is connected to pin 22 (28-pin) and pin 20 (24-pin) of the memory devices.

See page 725 for ordering information.

Printed in U.S.A.

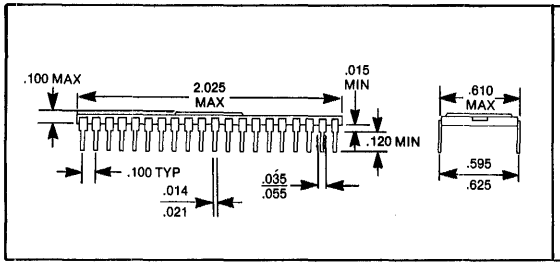
ORDERING INFORMATION

The following listing indicates the available packages for each product. The letter designation refers to the package diagrams, beginning on page 727.

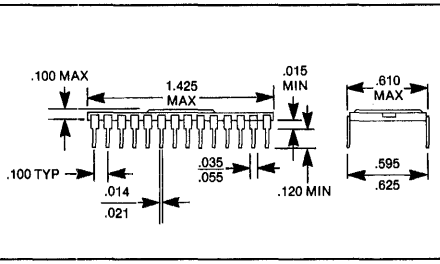
Part No.	Total Encapsulated	Ceramic	Rel-Pak	Cer-Dip
WD1100-01	V	U		
WD1100-02	V	U		
WD1100-12	V	U		
WD1100-03	V	U		
WD1100-04	V	U		
WD1100-05	V	U		
WD1100-06	V	U		
WD1100-07	V	U		
WD1100-09	V	U		
WD1010	PL	AL	BL	CL
WD1011	PD	AD	BD	CD
WD1012	PC	AC	BC	CC
WD1014	PL	AL	BL	CL
WD1050		DS		
FD1761	PL	A	B	CL
FD1763	PL	A	B	CL
FD1765	PL	A	B	CL
FD1767	PL	A	B	CL
FD1771	PL	A	B	CL
FD1781		A	B	
FD1791	PL	A	B	CL
FD1973	PL	A	B	CL
FD1795	PL	A	B	CL
FD1797	PL	A	B	CL
FD279X	PL	AL	BL	CL
WD1691	U	V		CE
DM1883		A	B	CL
WD2143	M	L		CD
WD2001-05		E	F	
WD2001-20		E	F	
WD2001-30		E	F	
WD2002-05		A	B	
WD2002-20		A	B	
WD2002-30		A	B	
TR1402-00	P	A	B	CL
TR1602-00	P	A	B	CL
TR1602-01	P	A	B	CL
TR1863-00	P	A	B	CL
TR1863-02	P	A	B	CL
TR1863-04	P	A	B	CL
TR1865-00	P	A	B	CL
TR1865-02	P	A	B	CL
TR1865-04	P	A	B	CL
WD8250-00	P	A	B	CL
WD2123-00	P	A	B	CL
BR1941-XX	M	L		CD

Part No.	Total Encapsulated	Ceramic	Rel-Pak	Cer-Dip
WD1943-XX	M	L	N/A	CD
WD1945-XX	M	L	N/A	CD
PR1472-00		A	B	CL
PR1472-01		A	B	CL
PT1482-00		A	B	CL
PT1482-01		A	B	CL
UC1671-00		A	B	CL
WD1931-00		A	B	CL
WD1933-00		A	B	CL
WD1933-01		A	B	CL
WD1933-02		A	B	CL
WD1933-03		A	B	CL
WD1933-10		A	B	CL
WD1933-11		A	B	CL
WD1933-12		A	B	CL
WD1993-01		E	F	
WD1993-02		E	F	
WD1993-03		E	F	
WD1983-00		E	F	CH
WD1984-00		E	F	
WD2501		T		
WD2511		T		
WD2520		T		
WD2530		T		
WD2840		T		
WD51		T	B	
WD55		A	B	
WD4200	PH	E	F	
WD4210	PG	C		
WD4320		E	F	
WD4321		C		
FR1502-10		E	F	
FR1502-11		E	F	
WD1510-00	PH	E	F	CH
WD1510-01	PH	E	F	CH
WD1511	V	U		
WD1801	V	U		
WD1802	V	U		
WD2412	PH			CH
WD5869	K	J		
WD74HC200	PC			CC
WD1820	PE	AE		
WD1840	PL/PH	AL/AH	BL/BH	
WD8206		DS		
WD8207		DS		
WD9216-00/ 9216-01	PA			
WD8275	PL	AL	BL	CL
WD8276	PL	AL	BL	CL

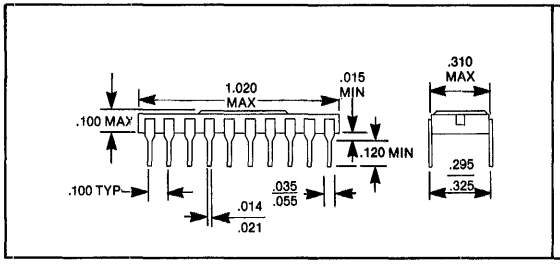
Package Diagrams



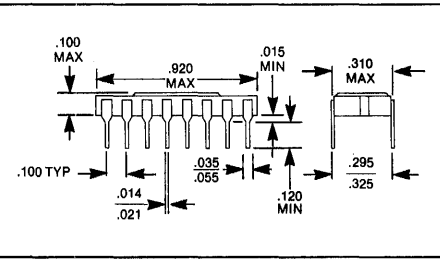
40 LEAD CERAMIC "A" or "AL"



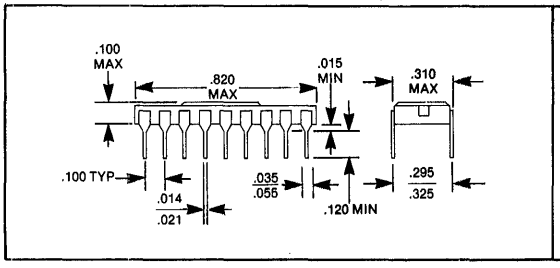
28 LEAD CERAMIC "E" or "AH"



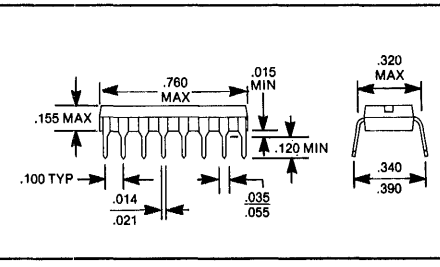
20 LEAD CERAMIC "U" or "AE"



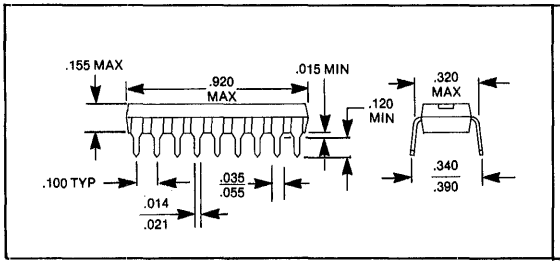
18 LEAD CERAMIC "L" or "AD"



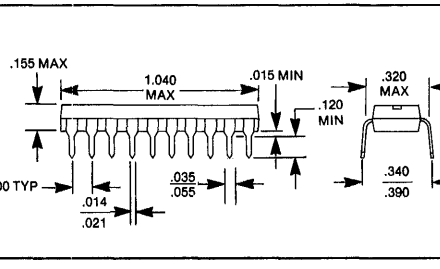
16 LEAD CERAMIC "J" or "AC"



16 LEAD PLASTIC "K" or "PC"

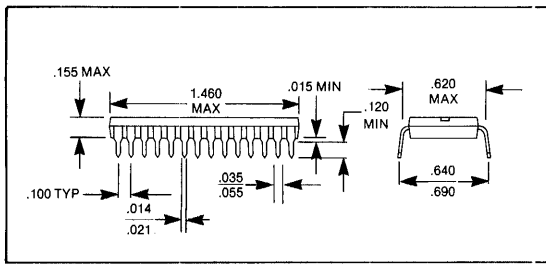


18 LEAD PLASTIC "M" or "PD"

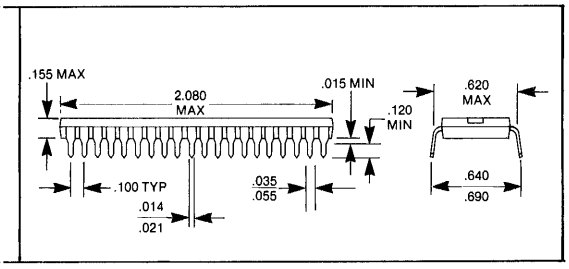


20 LEAD PLASTIC "V" or "PE"

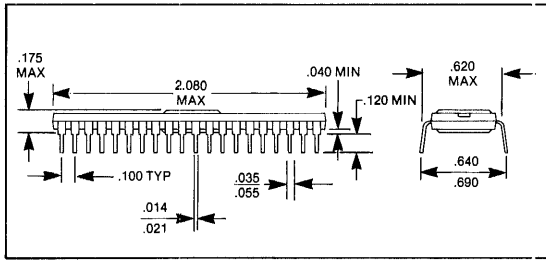
Package Diagrams



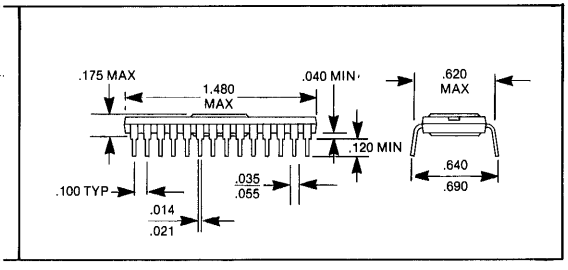
28 LEAD PLASTIC "R" or "PH"



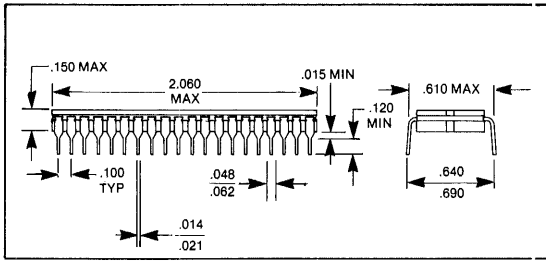
40 LEAD PLASTIC "P" or "PL"



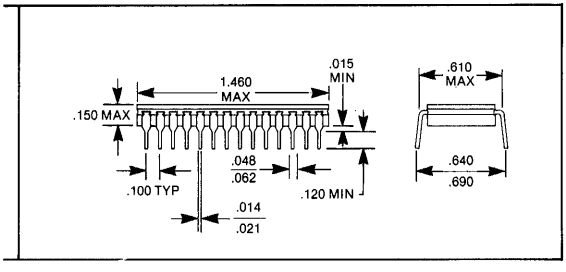
40 LEAD RELPACK "B" or "BL"



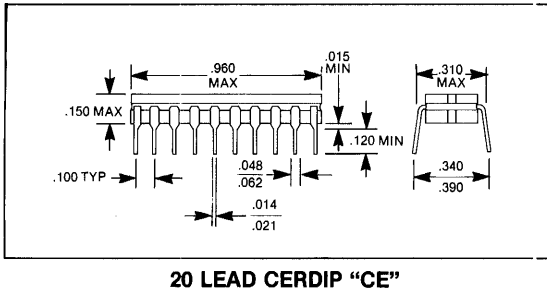
28 LEAD RELPACK "F" or "BH"



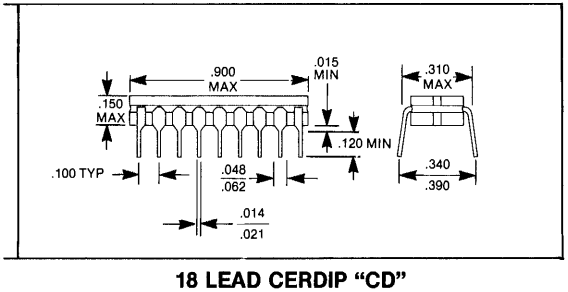
40 LEAD CERDIP "CL"



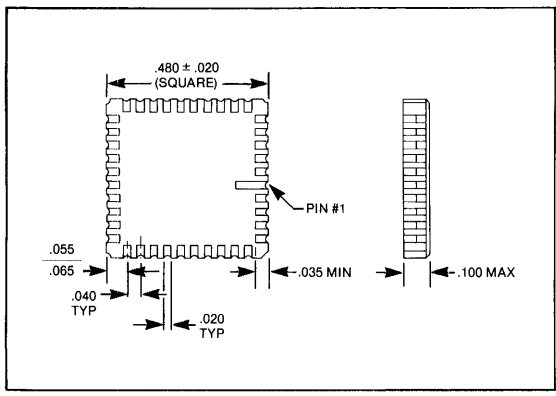
28 LEAD CERDIP "CH"



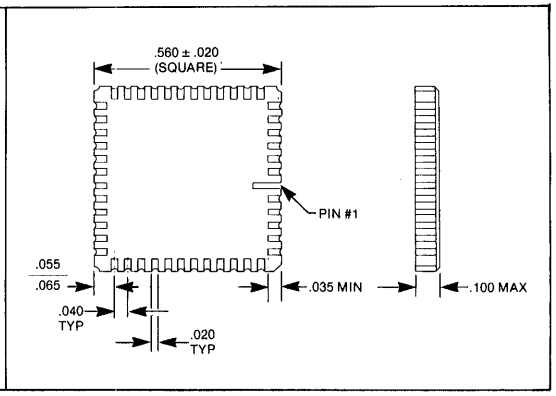
20 LEAD CERDIP "CE"



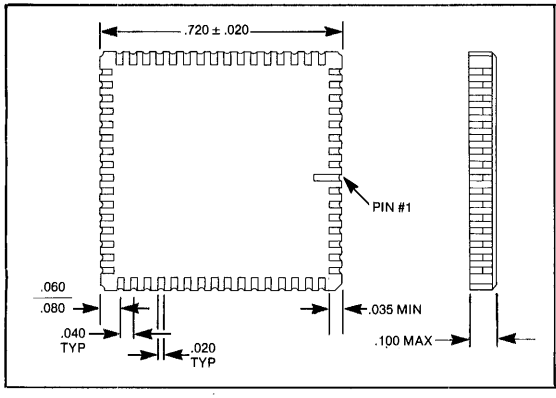
18 LEAD CERDIP "CD"



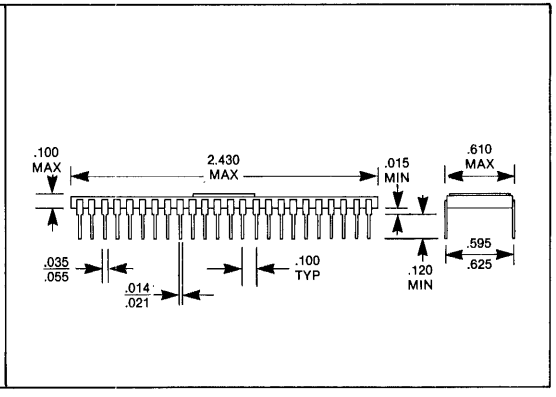
40 LEAD CERAMIC CHIP CARRIER "DL"



48 LEAD CERAMIC CHIP CARRIER "DN"



64 LEAD CERAMIC CHIP CARRIER "DS"



48 LEAD CERAMIC "T" or "AN"

See page 725 for ordering information.

WESTERN DIGITAL
CORPORATION

Pin Compatibility Chart

	AMD	AMI	FUJITSU	GI	HARRIS	HUGHES	INTEL	INTERSIL
TR 1402		S1757 S1883		AY-5-1013A AY-6-1013				
TR 1602		S1602			HM6402			IM6402
TR 1863				AY-3-1014A	HM6403			IM6405
TR 1865			WB8868A	AY-3-1015D		HCMP1854		
PR 1472				AY-3-1472B[4]				
PT 1482				AY-3-1482B[4]				
UC 1671								
WD 8250								
WD 1983[1]							8251A[1]	
BR 1941[2]								
WD 1943								
WD 1945								
WD 1010							82062	
FD 1771-01								
FD 179X								
WD 4200								
WD 4210								
WD 4320								
WD 4321								
WD 74HC200	AM27LS00							

	NATIONAL	NITRON	RCA	SIEMENS	SIGNETICS	SMC	TI
TR 1402					2536	COM2502 COM2502H	TMS6010[4]
TR 1602						COM2017 COM2017H	TMS6011[4]
TR 1863	MM5303		CDP1854			COM8502 COM8017 COM1863	
TR 1865						COM8018	
PR 1472		NC2259					
PT 1482		NC2257 NC2260					
UC 1671	INS1671					COM1671	
WD 8250	INS8250						
WD 1983[1]	INS8251A[1]					COM8251A	
BR 1941[2]						COM5016 COM5036[3]	
WD 1943						COM8016	
WD 1945						COM8036	
WD 1010						COM8116	
FD 1771-01	INS1771-1					COM8136	
FD 179X				SAB179X			
WD 4200	COPS420						
WD 4210	COPS421						
WD 4320	COPS320						
WD 4321	COPS321						
WD 74HC200							SN74LS200

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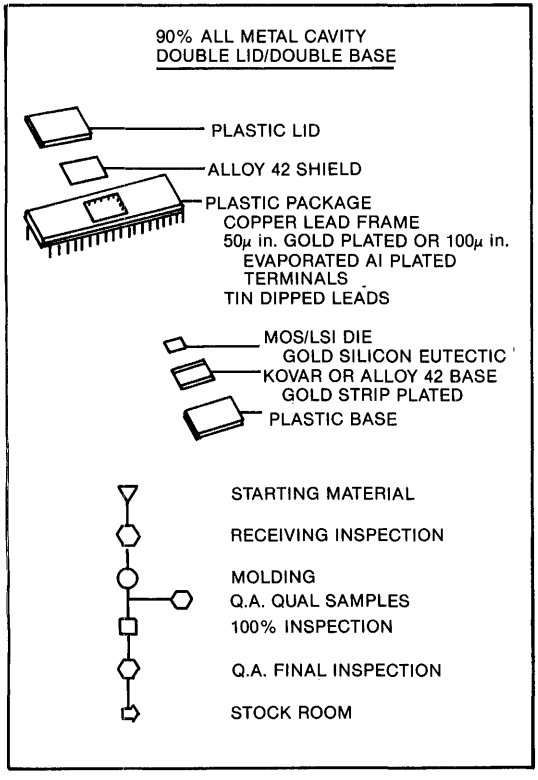
WESTERN DIGITAL
C O R P O R A T I O N

High Reliability Relpak Plastic Package Specification

FEATURES

- LOW COST CERDIP ALTERNATIVE
- RELIABILITY ADVANTAGES OF A CERAMIC PACKAGE
- SUPERIOR MECHANICAL QUALITIES
- OUTSTANDING ELECTRICAL CHARACTERISTICS
- CONSTRUCTION MATERIALS ELIMINATE SOURCES OF RUST AND CORROSION
- ELIMINATES HOT INTERMITTENT OPEN PROBLEMS
- ELIMINATES DEVICE INSTABILITY DUE TO IONIC CONTAMINATION
- MOISTURE 85/85 PERFORMANCE DRAMATICALLY IMPROVED
- SUPERIOR THERMAL PERFORMANCE



AVAILABILITY

WDC has been supplying satisfied customers for over nine years with this package. Because this package was developed in-house, we have a completely self-sustained production line with very little dependence on suppliers. The package was developed alongside the ceramic package, which means equipment interchangeability on the assembly line. This production versatility has enabled WDC customers to benefit from quick turn around times. We patented this package in 1973 because of its reliability similarities to ceramic packages.

RELIABILITY AT LOW COST

Western Digital Corporation's RELPAK Plastic Package is unique to the industry in that it contains many of the cost advantages of the industry accepted total encapsulated package while it also contains many of the reliability advantages of a ceramic package.

CONSTRUCTION DETAILS

The RELPAK is a cavity approach which allows the use of aluminum wire for cost purposes and direct aluminum-aluminum bond, while the plastic will never come in contact with the active circuit and wires. This eliminates the Hot Intermittent Open HIO problems associated with industry standard plastic packages and also eliminates device instability due to ionic contamination caused by plastic being in direct contact with the device.

The die is attached to its metal base separately from the plastic package body. This allows for a true AuSi Eutectic die attachment prior to the marriage with the plastic body. This process design again eliminated the chance for ionic contamination upon the active circuit areas.

The package structure is such that 90% of the internal surface area is composed of metal. The possible paths for moisture penetration are confined to the parameters of the cavity, thereby increasing the mean distance of moisture paths to its maximum.

This package is constructed using a proprietary high thermal conduction copper lead frame material, which eliminates sources of rust or corrosion. Our proprietary molding process allows WDC to mold without the lead frame bonding surface ever making contact with the molding material, again eliminating possible sources for ionic contamination.

We use an Ortho Creasol Novolac Epoxy resin and a Phenolic Novolac curing agent as the base transfer molding compound. Together with our proprietary

lead frame material we have achieved a true chemical mechanical bond during the molding process. This bond is so strong, we are able to place a device prior to lid seal upside down on a helium leak detector and pass a 1 x 10^{-8} std cc/sec open face leak test.

Using standard stress acceleration factors, the projected life expectancy of the WDC RELPAK Package is well in excess of 100 years.

The basic RELPAK design employes a "see thru" construction. The lead frames are stamped from 10 mil thick sheets of copper into strips of four, which are then spot Ni spot Au plated or evaporated Al plated. The quality levels of the lead frames and molding powders are rigorously controlled by incoming Q.C. The lead frames and molding powders are controlled by lot numbers. Each incoming lot is individually assessed by W.D.C. material assurance.

ADVANTAGES OF THE RELPAK

The most obvious is its lower cost compared to its ceramic counterpart without any reduction in reliability — by retaining the premolded cavity package concept, essentially all the problems of a total encapsulated package are avoided such as work damage to the bonding wires during the molding operation, concern for adverse effects from direct contact of the molding epoxy with the die surface, and the hot intermittent open reliability problem. The use of a solid metal lead frame coupled with the gold plated Kovar (or Alloy 42) base to which the die is eutectically attached provide excellent thermal paths for power dissipation, a primary reliability consideration.

See page 725 for ordering information.

Careful adherence to sound engineering design practices during package development coupled with the use of a metallurgical bond at chip bond and conventional aluminum wire bonding has resulted in a plastic cavity package which can be subjected to the same product assurance screening operations as its ceramic counterparts without adversely affecting the package or device parameters.

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Component Products
Terms and Conditions

1. **ACCEPTANCE:** Unless otherwise provided, it is agreed that sales are made on the terms, conditions and warranties contained herein and that to the extent of any conflict, the same take precedence over any terms or conditions which may appear on Buyer's order form. Seller shall not be bound by Buyer's terms and conditions unless expressly agreed to in writing. In the absence of written acceptance of these terms, acceptance of or payment for any of the articles covered hereby shall constitute an acceptance of these terms and conditions.

2. **F.O.B. POINT:** All sales are made F.O.B. point of shipment. Seller's title passes to Buyer and Seller's liability as to delivery ceases upon making delivery of articles purchased hereunder to carrier at shipping point in good condition; the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Unless specific instructions from Buyer specify which method of shipment is to be used, the Seller will exercise his own discretion.

3. **DELIVERY:** Shipping dates are approximate only. Seller shall not be liable for any loss or expense (consequential or otherwise) incurred by Buyer if Seller fails to meet the specified delivery schedule because of unavoidable production or other delays. Seller may deliver the articles in installments, Seller shall not be liable for any delay in delivery or for non-delivery, in whole or in part, caused by the occurrence of any contingency beyond the control either of Seller or Seller's suppliers, including, by way of illustration but not limitation, war (whether an actual declaration thereof is made or not), sabotage, insurrection, riot or other act of civil disobedience, act of a public enemy, failure or delay in transportation, act of any government or any agency or subdivision thereof, judicial action, labor dispute, accident, fire, explosion, flood, storm or other act of God, shortage of labor, fuel, raw material or machinery or technical failure where Seller has exercised ordinary care in the prevention thereof. If any contingency occurs, Seller may allocate production and deliveries among Seller's customers.

4. **TERMS AND METHODS OF PAYMENT:** Where seller has extended credit to Buyer, terms of payment shall be net thirty (30) days from date of invoice. The amount of credit or terms of payment may be changed or credit withdrawn by Seller at any time. If the articles are delivered in installments, Buyer shall pay for each installment in accordance with the terms hereof. Payment shall be made for the articles without regard to whether Buyer has made or may make any inspection of the articles. If shipments are delayed by Buyer, payments are due from the date when Seller is prepared to make shipments. Articles held for Buyer are at Buyer's sole risk and expense.

5. **TAXES:** All prices are exclusive of all federal, state and local excise, sales, use, and similar taxes. Such taxes; when applicable to this sale or to the articles sold, will appear as separate additional items on the invoice unless Seller receives a properly executed exemption certificate from Buyer prior to shipment.

6. **PATENTS:** The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents or trademarks arising from compliance with Buyer's designs or specifications or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements. Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information and assistance (at the Seller's expense) for the defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is in such suit held to constitute infringement and the use of said product or part is enjoined, the Seller, shall at its own expense, either procure for the Buyer the right to continue using said product or part, or replace same with non-infringing product, or modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. The foregoing states the entire liability of the Seller for patent infringement by the said products of any part thereof.

7. **ASSIGNMENT:** The Buyer shall not assign his order or any interest therein or any rights thereunder without the prior written consent of Seller.

8. **WARRANTY:** Seller warrants articles of its manufacture against defective materials or workmanship for a period of one year from date on which Seller delivers said articles. The liability of Seller under this warranty is limited at Seller's option, solely to repair, replacement with equivalent articles, or an appropriate credit adjustment not to exceed the original sales price of articles returned to the Seller provided that (a) Seller is promptly notified in writing by Buyer upon discovery of defects, (b) the defective article is returned to Seller, transportation charges prepaid by Buyer, and (c) Seller's examination of such article disclosed to its satisfaction that defects were not caused by negligence, misuse, improper installation, accident, or unauthorized repair or alteration by the Buyer. In the case of equipment articles, this warranty does not include mechanical parts failing from normal usage nor does it cover limited life electrical components which deteriorate with age. In the case of accessories, not manufactured by Seller, but which are furnished with the Seller's equipment, Seller's liability is limited to whatever warranty is extended by the manufacturers thereof and transferable to the Buyer. This Warranty is expressed in lieu of all other Warranties, expressed or implied, including the implied Warranty of fitness for a particlar purpose, and of all other obligations or liabilities on the Seller's part, and it neither assumes nor authorizes any other person to assume for the Seller any other liabilities. This Warranty should not be confused with or construed to imply free preventative or remedial maintenance, calibration or other service required for normal operation of the equipment articles. These Warranty provisions do not extend the original Warranty period of any article which has either been repaired or replaced by Seller. In no event will Seller be liable for any incidental or consequential damages.

9. **TERMINATION:** Buyer may terminate this contract in whole or from time to time in part upon 60 days written notice to Seller. In such event Buyer shall be liable for termination charges which shall include a price adjustment based on the quantity of articles actually delivered, and all costs, direct and indirect, incurred and committed for this contract together with a reasonable allowance for pro-rated expenses and profits. Any termination or back off in scheduling will not be allowed on shipments scheduled for the month in which the request is made and for the month following.

10. **GOVERNMENT CONTRACTS:** If the articles to be furnished under this contract are to be used in the performance of a Government contract or subcontract and a Government contract number shall appear on Buyer's purchase order, those clauses of the applicable Government procurement regulation which are mandatorily required by Federal Statute to be included in Government subcontracts shall be incorporated herein by reference.

11. **ORIGIN OF ARTICLES:** Seller engages in off-shore production, assembly and/or processing and makes no warranty or representation, expressed or implied, that the articles delivered hereunder are United States articles or of U.S. origin for the purpose of any statute, law, rule, regulation or case thereunder. If Buyer ships the articles hereunder out of the U.S. for assembly, then at Buyer's request in writing, Seller shall provide information applicable to identification of any articles not of U.S. origin.

Corita Kent, the cover artist, is an American whose work presents an optimistic, yet philosophical view of the world we live in. A former Catholic nun and teacher, Corita now devotes her life and energies to her artwork and the "human needs she feels transcend national and religious barriers." A true "citizen of the world," Corita's philosophy positions her "on the positive side of hope." Her depiction of the Western Digital mission . . . "Making the leading edge work for you" . . . dramatizes the spectrum of solutions we provide our customers.

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