SYSTEMS LOGIC/PERIPHERAL

5

FE3021A

Address Buffer and Memory Controller

WESTERN DIGITAL

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The FE3021A Address Buffer And Memory Controller device is an enhancement of the FE3021. Although the two devices are very similar in design, it is important to use the appropriate document when designing around the use of this device. The FE3021 literature order number is I0505. The FE3021A literature order number is I0503.

Some of the areas affected by the enhancement of the device are:

The FE3021A operates as a 20 MHz address buffer and memory controller using 80 ns DRAMs, as well as a 16 MHz using 100 ns DRAMs as does the FE3021.

The version numbers read from the Version Number Register (FFF01) are 010 = FE3021A and 100 = FE3021.

Bits 3 and 2 of the Hot Reset Register (FFF07) have been redefined. Bit 3 = 1 to tri-state ADDR0 (pin 105), bit 2 no longer has a function and bits 1 and 0 remain unchanged.

Page Mode 2 now operates at 16 MHz with 80 ns DRAMs as well as 12.5 MHz with 120 ns DRAMs.

The efficiency of all timing parameters have been increased considerably.

1.0 DESCRIPTION

The FE3021A is a 20 MHz AT address buffer and memory controller in a 132-pin PQFP package. Chip count is significantly reduced by integrating the memory controller, AT bus address buffers, and I/O into one chip. The memory controller is a high performance design, with programmable modes of operation. It controls page mode DRAM or static column DRAM. Up to 4 banks of DRAM, allowing a maximum of 8 Mbytes of memory can be controlled by the FE3021A. The DRAM bank locations are programmable on 128 Kbyte boundaries. One memory bank allows split addressing, so that one portion may be placed in conventional memory with the remainder in extended memory.

Additional features of the FE3021A include EMS 4.0 support, on-chip address and control signal buffers for directly driving the AT bus, zero wait state access at 16 MHz using 100 ns DRAM with page mode access, generation of chip selects for floppy controller, 8042 keyboard controller, 80287 numeric processor, and NMI, and mapping main and EGA/VGA BIOS into one physical PROM.

1.1 FEATURES

- Page mode DRAM access with interleaved memory banks
- Controls up to 4 banks (up to 8 Mbytes) of memory
- On-chip RAS and CAS drivers for DRAM chips
- On-chip DRAM address multiplexer
- LIM (Lotus, Intel, Microsoft) standard EMS expanded memory hardware (supports EMS 4.0 multi-tasking)
- On-chip address and control signal buffers for directly driving AT bus
- Zero wait state access at 16 MHz using 100 ns DRAM with page mode access and up to 20 MHz with 80 ns DRAM
- Generates chip selects for floppy controller, 8042 keyboard controller, 80287 numeric processor, and NMI (Non-maskable Interrupt)
- Generates programmable chip selects for four additional devices
- Address buffer and memory controller for the four chip core logic set
- Maps system BIOS and EGA BIOS into one physical PROM
- "Hot" reset generation for quick 80286 switch from protected to real mode
- Fast Alternate Gate A20 generation
- Interfaces with the FE3600/B/C chip set devices FE3001/A, FE3010/B/C, and FE3031/A
- 132-pin JEDEC PQFP (plastic quad flat package)

1.2 INTRODUCTION

The FE3021A device is designed to reduce chip count, increase flexibility, and provide improved operating speed and functionality when used with the FE3001/A, FE3010B/C, and FE3031/A devices to implement a low cost, high performance AT compatible computer at speeds up to 20 MHz. Together these four chips make up the FE3600B/C chip set.

Chip count is reduced by integrating the memory controller, AT bus address buffers, and I/O Management functions into one chip.

The memory controller is a high performance design, with programmable modes of operation. It controls page mode DRAM or static column DRAM.

Up to 4 banks of DRAM may be controlled. The DRAM bank locations are programmable on 128 Kbyte boundaries. One memory bank allows split addressing, so that one portion may be placed in conventional memory with the remainder in extended memory, with an additional mode to allow copying BIOS code from ROM to RAM for faster execution.

A major function of the FE3021A is to generate chip select decodes for peripheral chips on the system board; for instance, the floppy controller, hard disk controller, serial, and parallel port chips. The floppy and hard disk chip selects may be disabled or may be enabled for either the primary or secondary address decode, as defined by IBM. Four programmable chip selects are available, for supporting serial, parallel, mouse, or other types of ports. Refer to Figure 7 for Pin assignment and locations.

To reduce chip count and improve performance, particularly when an EGA or VGA graphics controller is placed on the system board, separate blocks of ROM may be mapped into a single physical ROM. For instance, the EGA BIOS and standard BIOS may be placed into the same pair of ROM chips or into a single 8-bit wide ROM. Besides reducing chip count, EGA operating speed will be improved, since EGA BIOS will be accessed 16 bits at a time. To improve BIOS performance, ROM code may be copied into RAM, and the BIOS ROM mapped out and replaced by RAM.

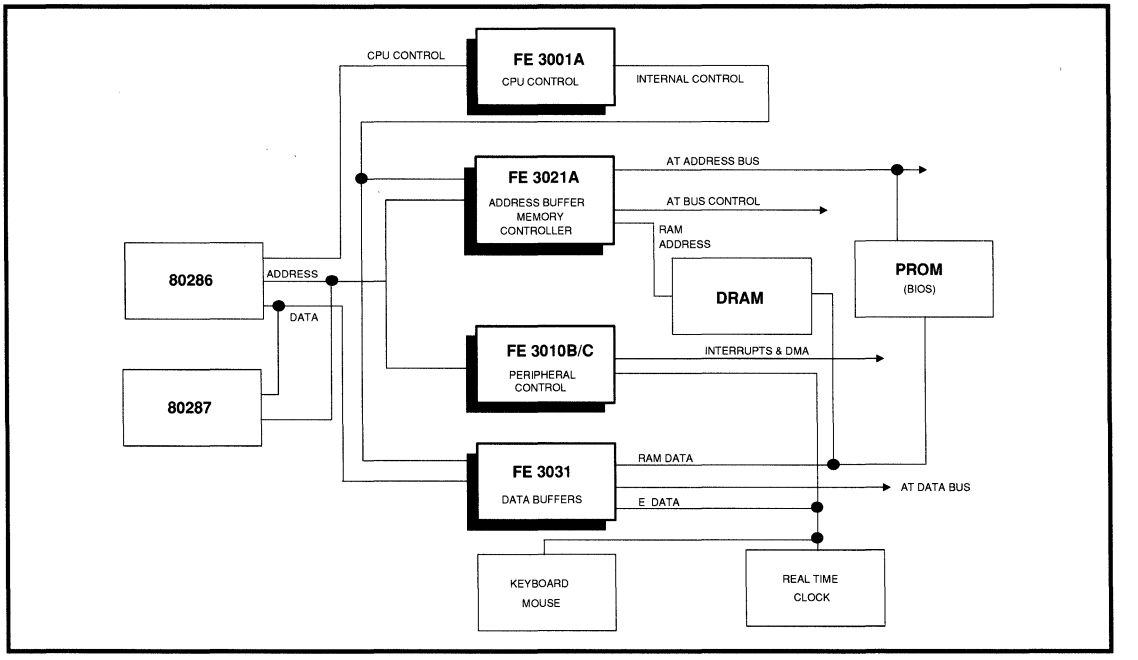

FIGURE 1. FE3600B/C CHIP SET FUNCTIONAL BLOCK DIAGRAM

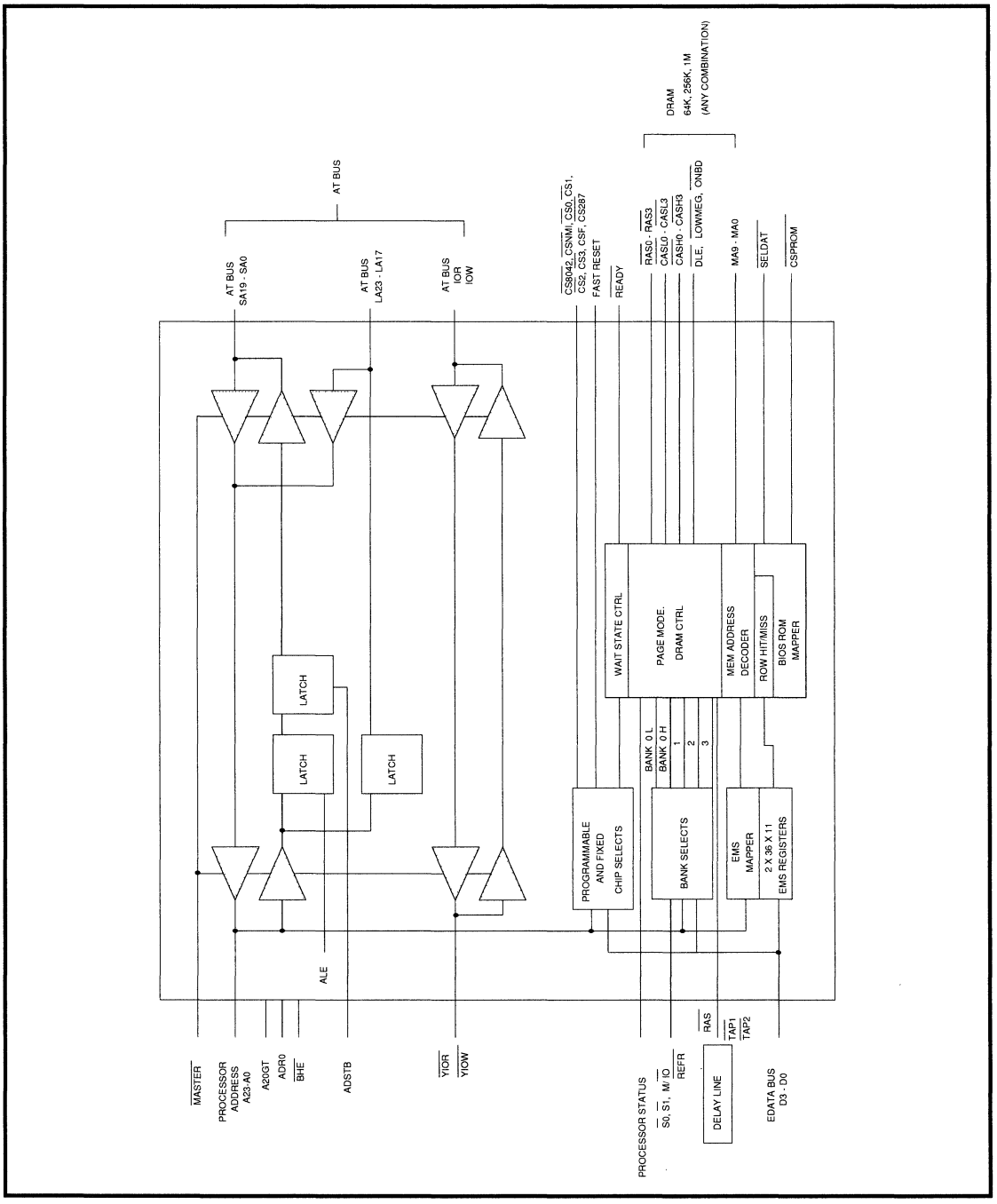

FIGURE 2. FE3021A FUNCTIONAL BLOCK DIAGRAM

2.0 80286 INTERFACE

This interface port connects with the 80286 address lines and the 80286 bus status lines. By connecting directly to the 80286 and by duplicating a portion of the bus controller logic, early determination of memory or I/O accesses may be made, as well as whether the access will be 8 bits or 16 bits. Pins A23-A0 are normally inputs, receiving addresses from the 80286. When $\overline{\text{MASTER}}$ is asserted, these pins become outputs.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
74	A23	I/O	80286 ADDRESS LINE
78	A22	I/O	" "
79	A21	I/O	" "
80	A20	I/O	" "
81	A19	I/O	" "
82	A18	I/O	" "
83	A17	I/O	" "
84	A16	I/O	" "
85	A15	I/O	" "
86	A14	I/O	" "
87	A13	I/O	" "
88	A12	I/O	" "
89	A11	I/O	" "
90	A10	I/O	" "
109	A9	I/O	" "
110	A8	I/O	" "
111	A7	I/O	" "
112	A6	I/O	" "
113	A5	I/O	" "
114	A4	I/O	" "
115	A3	I/O	" "
116	A2	I/O	" "
117	A1	I/O	" "
118	A0	I/O	" "
119	$\overline{\text{S0}}$	I	80286 STATUS LINE
120	$\overline{\text{S1}}$	I	80286 STATUS LINE
121	M/$\overline{\text{IO}}$	I	80286 STATUS LINE
122	CPUCLK	I	80286 CLOCK
123	HLDA	I	80286 HOLD ACKNOWLEDGE LINE
21	$\overline{\text{BHE}}$	I	80286 BYTE HIGH ENABLE

TABLE 1. 80286 INTERFACE PIN ASSIGNMENTS

3.0 DATA BUS INTERFACE

The data bus port is 4 bits wide, which should connect to the EDATA local data bus, and is used to access the internal FE3021A control registers. The upper 4 bits should be ignored when reading the control registers. Refer to Table 2 for pin assignments.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
17	EDATA3	I/O	Control Register Data Line
16	EDATA2	I/O	" "
15	EDATA1	I/O	" "
14	EDATA0	I/O	Control Register Data Line

TABLE 2. DATA BUS INTERRFACE PIN ASSIGNMENTS

4.0 I/O CHIP SELECTS

This logic section generates chip selects for standard system board functions such as the 8042 keyboard controller, 80287 math coprocessor, floppy controller, and hard disk controller. It also generates chip selects for up to 4 additional I/O ports which may have programmable addresses and wait state characteristics. Refer to Table 3 for pin assignments.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
48	$\overline{CS0}$	O	Programmable Chip Select 0
47	$\overline{CS1}$	O	Programmable Chip Select 1
46	$\overline{CS2}$	O	Programmable Chip Select 2
45	$\overline{CS3}$	O	Programmable Chip Select 3 or H. D. Controller Chip Select
49	CSF	O	Floppy Disk Controller Chip Select or Operation or Config. Register Select
60	$\overline{CS8042}$	O	8042 Keyboard Controller Select
56	$\overline{CS287}$	O	80287 Coprocessor Select/ROM Chip Select
20	$\overline{CSNMI}$	O	NMI Logic Chip Select
22	$\overline{CSPTB}$	O	Memory Parity and I/O Check

TABLE 3. I/O CHIP SELECT PIN ASSIGNMENTS

5.0 I/O CONTROL

This logic section contains control logic for the I/O bus.

The IORDY signal will go low when generating wait states. For 12 MHz systems, this signal may be tied directly to the bus signal IOCHRDY. For 16 MHz or 20 MHz systems, this signal should be sent to the FE3001A directly. The IOCHRDY bus signal should be buffered through an open collector driver and wire-ORed with the IORDY signal. The IORDY pin will normally be at a high impedance state. When generating wait states, it will go low. When going from a low to a high state, the IORDY pin will be actively driven high for one processor clock time, then the output will tri-state. An external pullup resistor should be used to keep the IORDY signal high when the IORDY pin is at a high impedance state. The state of IORDY is sampled at the rising edge of $\overline{\text{RESET}}$; if IORDY is low at this time, the FE3021A will fetch data and instructions from the BIOS ROM 8 bits at a time over the EDATA bus, otherwise a 16-bit wide ROM on the MDATA bus is assumed.

The PORT 0, PORT 1, PORT 2, and PORT 3 addresses are fully programmable, with the choice of either using nine I/O addresses for decode, or masking the A8 address bit (for instance, for decoding dual serial ports). The LSB (A0) address is always ignored. The lower 2, 3, or 4 bits of the address may also be ignored so that 2, 4, 8, or 16 bytes may be allocated for the port.

All FE3021A control registers, except those used for EMS page mapping, are accessed by first writing eight times to address FFF00 (in an area allocated for ROM BIOS). Any memory access outside of the ROM BIOS address space, either data access or instruction fetch, will abort the unlocking process. Once unlocked, memory accesses outside of the ROM BIOS area may be made without affecting the unlocked state. When unlocked, the address space from FFF01 to FFFFE becomes register controls for the FE3021A device. The controls are locked again by reading location FFFFF. This access method guarantees that all control register changes will be made through the BIOS.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
127	IORDY	I/O	Ready line, modified open drain, input at reset time for 8-bit ROM sizing.
40	$\overline{\text{SELDAT}}$	O	Direction of data transceiver data to EDATA bus.
8	$\overline{\text{IOR}}$	I/O	System I/O Read Command signal, drives expansion bus. An input in master mode.
9	$\overline{\text{IOW}}$	I/O	System I/O Write Command signal, drives expansion bus. An input in master mode.
10	$\overline{\text{YMEMR}}$	I	Ungated system memory Read Command signal from FE3001A.
11	$\overline{\text{YMEMW}}$	I	Ungated system memory Write Command signal from FE3001A.
53	ADSTB	I	Address strobe from FE3001A and FE3010B/C.
12	$\overline{\text{YIOR}}$	I/O	Ungated I/O read strobe from FE3001A. An output in master mode.
13	$\overline{\text{YIOW}}$	I/O	Ungated I/O write strobe from FE3001A. An output in master mode.
19	$\overline{\text{FRES}}$	I/O	"HOT" reset output
25	$\overline{\text{LOMEG}}$	O	To FE3031 memory strobe gating.
28	$\overline{\text{RESET}}$	I	Master Reset for FE3021A.
52	$\overline{\text{MASTER}}$	I	Bus master signal from the AT bus.
54	A20GT	I	From 8042. When high, A20 is ungated.
57	$\overline{\text{ONBD}}$	O	To FE3001A. Indicates high speed on-board access.

TABLE 4. I/O CONTROL PIN ASSIGNMENTS

PIN NUMBER	MNEMONIC	I/O	FUNCTION
59	ADDR19	O	AT BUS SA19
61	ADDR18	O	AT BUS SA18
62	ADDR17	O	AT BUS SA17
64	ADDR16	I/O	AT BUS SA16
65	ADDR15	I/O	AT BUS SA15
66	ADDR14	I/O	AT BUS SA14
68	ADDR13	I/O	AT BUS SA13
69	ADDR12	I/O	AT BUS SA12
72	ADDR11	I/O	AT BUS SA11
73	ADDR10	I/O	AT BUS SA10
75	ADDR9	I/O	AT BUS SA 9
94	ADDR8	I/O	AT BUS SA8
96	ADDR7	I/O	AT BUS SA7
97	ADDR6	I/O	AT BUS SA6
98	ADDR5	I/O	AT BUS SA5
100	ADDR4	I/O	AT BUS SA4
101	ADDR3	I/O	AT BUS SA3
104	ADDR2	I/O	AT BUS SA2
106	ADDR1	I/O	AT BUS SA1
105	ADDR0	I/O	AT BUS SA0
63	LA23	I/O	AT BUS LA23
70	LA22	I/O	AT BUS LA22
71	LA21	I/O	AT BUS LA21
93	LA20	I/O	AT BUS LA20
95	LA19	I/O	AT BUS LA19
102	LA18	I/O	AT BUS LA18
103	LA17	I/O	AT BUS LA17

TABLE 4. I/O CONTROL PIN ASSIGNMENTS (Cont.)

A Version Number register provides information on the version of the FE3021A chip. It also contains a bit which toggles between '0' and '1' when the register is read, which provides indication that the register set has been unlocked.

VERSION NUMBER

	7	6	5	4	3	2	1	0
FFF01	X	X	X	X	VER			T

T : toggles between 0 and 1 with every read access of the Version Number register.

VER : 000 when T=0
010 when T=1 for version FE3021A
100 when T=1 for version FE3021

System board devices may be located on the EDATA bus rather than on the I/O expansion slot DATA bus. The $\overline{\text{SELDAT}}$ signal which controls the DATA to EDATA bus direction is affected by the two port location registers. This option is available for peripheral devices which cannot directly drive the high current I/O slot DATA bus. Note, however, that DMA transfers cannot be made to devices on the EDATA bus.

The $\overline{\text{SELDAT}}$ signal is active (low) when $\overline{\text{IOR}}$ is active and address bits A8 and A9 are low, or the PORTS LOCATION register indicates that an addressed port is on the EDATA bus. The $\overline{\text{SELDAT}}$ signal is also low when $\overline{\text{MEMR}}$ is active and the **8-bit** BIOS is being accessed.

PORTS LOCATION REGISTER

	7	6	5	4	3	2	1	0
FFF06	X	X	X	X	A	B	C	D

The Ports Location Register is cleared by a master reset.

A = 0 Port 0 On Data Bus
A = 1 Port 0 On Edata Bus

B = 0 Port 1 On Data Bus
B = 1 Port 1 On Edata Bus

C = 0 Port 2 On Data Bus
C = 1 Port 2 On Edata Bus

D = 0 Port 3 On Data Bus
D = 1 Port 3 On Edata Bus

HOT RESET REGISTER

	7	6	5	4	3	2	1	0
FFF07	X	X	X	X	T	X	A	H

The Hot Reset Register is cleared by a master reset.

Register FFF07 is used to generate a hot reset to the processor or to generate an alternate A20 gate. The state of the A bit is ORed with the A20GT pin. If either the A bit is set or the A20GT pin is high, the A20 line is undisturbed. If both are low, then the A20 line is gated low. A hot reset is generated by changing the H bit from a '0' to a '1'. 131 clocks after the trailing edge of the $\overline{\text{MEMW}}$ strobe, the $\overline{\text{FRES}}$ pin is pulled low. The reset pulse lasts for 32 clocks, then the $\overline{\text{FRES}}$ pin is actively pulled high for one clock cycle, then is tri-stated. If the $\overline{\text{FRES}}$ pin is pulled low externally (e.g. if wire-OR'ed with the 8042 CPU reset line), then the internal FE3021A registers will relock. If the $\overline{\text{FRES}}$ pin is not used, then it should be pulled up externally.

When the T bit is set, ADDR0 is tri-stated (pin 105).

ENABLE PORTS REGISTER

	7	6	5	4	3	2	1	0
FFF10	X	X	X	X	EN3	EN2	EN1	EN0

The Enable Ports Register is cleared by a master reset.

The programmable PORT 0, PORT 1, PORT 2, and PORT 3 chip selects are enabled with the Enable Ports register. If the Enable bit is 0, the port chip select bit will always be at an inactive (high) state. All four ports are disabled after master reset. EN3 enables $\overline{CS3}$ only when $\overline{CS3}$ is a programmed chip select. When $\overline{CS3}$ is a HDC chip select, CS3 is enabled by register FFF49, bit 1.

For ports 0, 1, and 2, the access will have the default wait states: 1 wait state for 16 bit accesses and 4 wait states for 8 bit accesses, with the wait states set from the FE3001A. The selected chip must generate $\overline{IOCS16}$ if it is a 16-bit peripheral.

PORT 3 CONTROL REGISTER

	7	6	5	4	3	2	1	0
FFF08	X	X	X	X	WS		WSE	OB

The Port 3 Control Register is cleared by a master reset.

WS	HDC DATA PORT HIGH SPEED WAIT STATES
00	1
01	2
10	3
11	4

0B	$\overline{CS3}$ WAIT STATES
0	Default (slow)
1	High speed hard disk controller

WSE	HIGH SPEED HDC WAIT STATE ENABLE
0	High speed HDC wait states set by FE3001A
1	High speed HDC Wait States set by WS field

For port 3, the access will normally have the default wait states but may also be programmed to have high speed wait state timing when $\overline{CS3}$ is programmed as a hard disk chip select and the on-board 16-bit hard disk controller is capable of high speed access. When the high speed disk controller configuration is used, the WSE and OB fields should be set to '1', and the WS field will set the number of high speed wait states, timed from the CPUCLK, rather than from SYSCLK. The other disk controller ports will always be accessed at low speed.

When 0B is set to a 1, the FE3021A will generate the $\overline{ONBD}$ signal to the FE3001A during HDC accesses through port 3. The FE3001A will provide the same number of wait states it does for on-board memory. If it is desired, the number of wait states for the HDC can be extended using the WS and WSE fields.

When implementing a high speed disk controller port, it is necessary to provide a separate address path for the hard disk controller. The HDC receives ungated I/O read and write strobes at the full CPU speed. The following schematic illustrates the required connections.

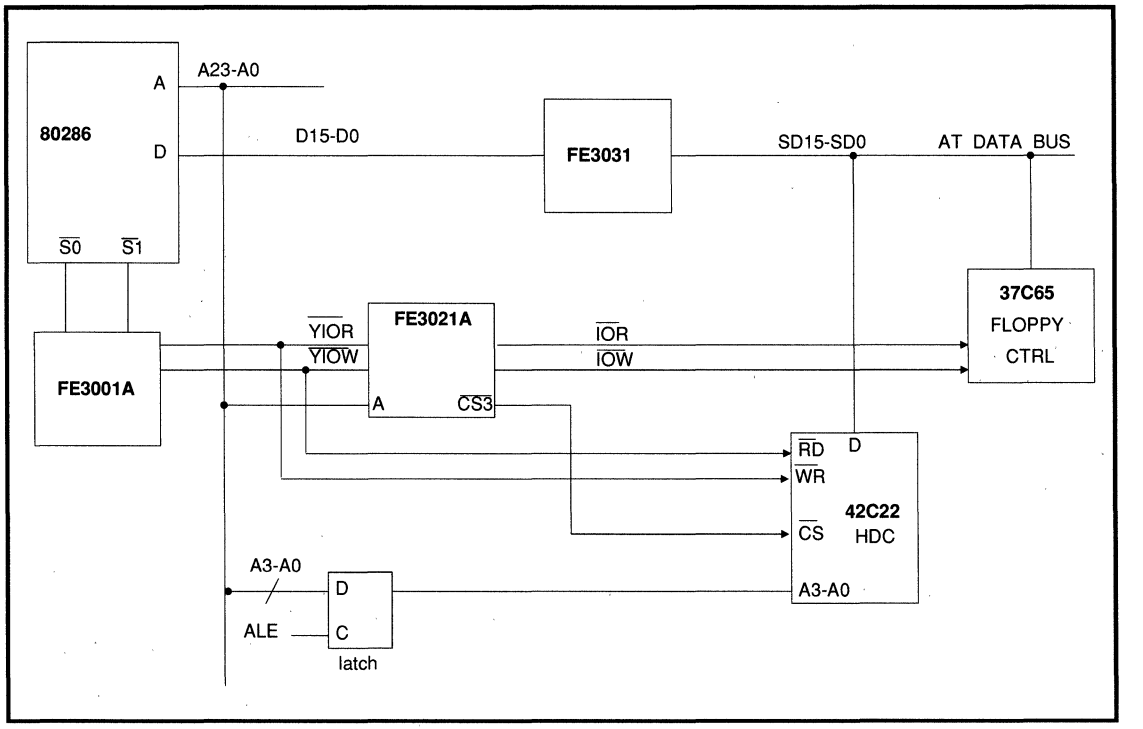

FIGURE 3. HIGH SPEED HDC CONFIGURATION

PORT ADDRESS MASK REGISTER

FFF09
FFF11
FFF19
FFF21

X	X	X	X	O	U	LMASK	
7	6	5	4	3	2	1	0

The Port Address Mask Register is cleared by a master reset.

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LMASK	ADDRESS BITS COMPARED									
00	A9	A8	A7	A6	A5	A4	A3	A2	A1	X
01	A9	A8	A7	A6	A5	A4	A3	A2	X	X
10	A9	A8	A7	A6	A5	A4	A3	X	X	X
11	A9	A8	A7	A6	A5	A4	X	X	X	X

U = 0 : Include A8 In Address Comparison

LMASK	ADDRESS BITS COMPARED									
00	A9	X	A7	A6	A5	A4	A3	A2	A1	X
01	A9	X	A7	A6	A5	A4	A3	A2	X	X
10	A9	X	A7	A6	A5	A4	A3	X	X	X
11	A9	X	A7	A6	A5	A4	X	X	X	X

U = 1 : Ignore A8 In Address Comparison

PORT	PORT CONTROL REGISTER ADDRESS
0	FFF09
1	FFF11
2	FFF19
3	FFF21

NOTE: Bit 3 is not writable and is always '0'.

PORT ADDR - LOWER MSB

FFF0A
FFF12
FFF1A
FFF22

X	X	X	X	X	X	A9	A8
7	6	5	4	3	2	1	0

PORT ADDR - UPPER LSB

FFF0B
FFF13
FFF1B
FFF23

X	X	X	X	A7	A6	A5	A4
7	6	5	4	3	2	1	0

PORT ADDR - LOWER LSB

FFF0C
FFF14
FFF1C
FFF24

X	X	X	X	A3	A2	A1	0
7	6	5	4	3	2	1	0

The Port I/O Address registers for all four ports are set to all zeros by a master reset.

PORT	PORT I/O ADDRESS REGISTERS		
	A9-A8	A7-A4	A3-A0
0	FFF0A	FFF0B	FFF0C
1	FFF12	FFF13	FFF14
2	FFF1A	FFF1B	FFF1C
3	FFF22	FFF23	FFF24

	ADDR2	ADDR1	CSF
OPERATIONS REGISTER ACCESS	0	X	1
CONFIG REGISTER ACCESS	1	1	1
FLOPPY CHIP SELECT ACTIVE	X	0	1

Table 5 lists the I/O addresses and chip selects generated for each fixed port type. The chip selects are not gated with $\overline{IOR}$ or $\overline{IOW}$. The $\overline{CSNMI}$ signal is decoded for both even and odd addresses, so that access may be made to the FE3001A control register at address 073.

The floppy controller operations register select, configuration register select, and floppy disk controller chip select may be generated from the CSF pin and the ADDR2 and ADDR1 lines.

PORT	BIT SIZE	I/O ADDRESS	ACTIVE SIGNAL	FUNCTION
FLOPPY	8	3F2 372	CSF	FDC operation select. 3F2 is primary address, 372 is secondary.
	8	3F4-3F5 374-375	CSF	3F4-3F5 are primary addresses, 374-375 are secondary.
	8	3F6 376	$\overline{CS3}$*	Hard disk controller chip select. 3F6 is primary address, 376 is secondary.
	8	3F7 377	CSF $\overline{CS3}$*	$\overline{CS3}$ and CSF pins will be asserted. 3F7 is primary address, 377 is secondary.
80287	8	0E0-0FF	$\overline{CS287}$	80287 Chip Select.
8042	8	060-06E (EVEN)	$\overline{CS8042}$	8042 Chip Select.
NMI LOGIC	8	070-07F	$\overline{CSNMI}$	Real Time Clock and NMI logic select.
PARITY CHECK	8	061-06F (ODD)	$\overline{CSPTB}$	Parity check select and Port B decode. External logic must separate the signals.
HARD DISK	16	1F0 170	$\overline{CS3}$ *	HDC Chip Select - Data Port access. 1F0 IS primary address, 170 is secondary.
	8	1F1-1F7 171-177	$\overline{CS3}$	HDC Chip Select - Task File. 1F1-1F7 are primary addresses, 171-177 are secondary.

TABLE 5. I/O ADDRESS/CHIP SELECTS FOR FIXED PORTS

*When $\overline{CS3}$ pin is programmed as HDC Chip Select .

PRIMARY / SECONDARY PORT FUNCTION SELECT

	X	X	X	X	DH	PS	H	F
FFF49	7	6	5	4	3	2	1	0

DH, PS, H, and F are cleared to '0' by master reset

DH=0: $\overline{CS3}$ pin will respond to address programmed by FFF22-FFF24
DH=1: $\overline{CS3}$ pin will respond to hard disk addresses

PS=0: Primary hard disk and floppy disk address
PS=1: Secondary hard disk and floppy disk address

H=0: On-board hard disk controller enabled
H=1: Disable on-board hard disk controller

F=0: On-board floppy disk controller enabled
F=1: Disable on-board floppy disk controller

NOTE: For early production version (ID Register= 0000, 1011) bits 2 - 0 had different definitions:

Bit 2 = 0 : Enable CSF Output
Bit 1 = 0 : Primary Hard Disk Address
Bit 0 = 0 : Primary Floppy Disk Address

6.0 MEMORY CONTROL

Four RAS pins are available for controlling up to four 16-bit wide banks of system board RAM. Eight CAS pins control the low and high bytes of each bank. During a refresh cycle, all RAS signals will be active (ignoring the RAM configuration register FFF57) and CAS signals will stay inactive.

The RAS and CAS lines drive the DRAM array directly.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
128	$\overline{RAS0}$	O	RAS signal for DRAM Memory Bank 0
129	$\overline{RAS1}$	O	RAS signal for DRAM Memory Bank 1
130	$\overline{RAS2}$	O	RAS signal for DRAM Memory Bank 2
132	$\overline{RAS3}$	O	RAS signal for DRAM Memory Bank 3
125	$\overline{CASL0}$	O	CAS signal for DRAM Memory Bank 0, low byte
126	$\overline{CASL1}$	O	CAS signal for DRAM Memory Bank 1, low byte
2	$\overline{CASL2}$	O	CAS signal for DRAM Memory Bank 2, low byte
3	$\overline{CASL3}$	O	CAS signal for DRAM Memory Bank 3, low byte
4	$\overline{CASH0}$	O	CAS signal for DRAM Memory Bank 0, high byte
5	$\overline{CASH1}$	O	CAS signal for DRAM Memory Bank 1, high byte
6	$\overline{CASH2}$	O	CAS signal for DRAM Memory Bank 2, high byte
131	$\overline{CASH3}$	O	CAS signal for DRAM Memory Bank 3, high byte
18	$\overline{REFR}$	I	Memory Refresh signal
43	$\overline{CSPROM}$	O	BIOS PROM select
26	$\overline{TAP2}$	I	Second tap output of RAS delay line
44	$\overline{TAP1}$	I	First tap output of RAS delay line
58	$\overline{RAS}$	O	To RAS delay line input
23	$\overline{DLE}$	O	To FE3031 memory data bus latch enable
24	ADR0	I	From FE3001A byte conversion

TABLE 6. MEMORY CONTROL PIN ASSIGNMENTS

7.0 MEMORY ADDRESS MULTIPLEXER

The memory address multiplexer generates the row and column addresses for the DRAM. The memory address multiplexer outputs should be buffered by external drivers when driving the memory array.

The memory address multiplexer supports three sizes of DRAM: 64K, 256K, and 1 MB. The three sizes of DRAM's may be intermixed in any order.

The memory address multiplexer is designed so that SIMM mounted DRAM's of the three different sizes may be inserted into SIMM sockets without the need to change board jumpers.

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PIN NUMBER	MNEMONIC	I/O	FUNCTION
31	RA0	O	Memory address multiplexer output bit 0 (LSB)
32	RA1	O	Memory address multiplexer output bit 1
33	RA2	O	Memory address multiplexer output bit 2
34	RA3	O	Memory address multiplexer output bit 3
35	RA4	O	Memory address multiplexer output bit 4
36	RA5	O	Memory address multiplexer output bit 5
37	RA6	O	Memory address multiplexer output bit 6
38	RA7	O	Memory address multiplexer output bit 7
39	RA8	O	Memory address multiplexer output bit 8
41	RA9	O	Memory address multiplexer output bit 9 (MSB)

TABLE 7. MEMORY ADDRESS MULTPLEXER OUTPUT PIN ASSIGNMENTS

MEMORY MODE		MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
64K DRAM ADDRESS MULTIPLEXER CONFIGURATION											
INDEPENDENT	RAS	(A10	A9)	A8	A7	A6	A5	A4	A3	A2	A1
NON PAGE MODE	CAS	(A20	A18)	A16	A15	A14	A13	A12	A11	A10	A9
INDEPENDENT	RAS	(A20	A18)	A16	A15	A14	A13	A12	A11	A10	A9
PAGE MODE	CAS	(A10	A9)	A8	A7	A6	A5	A4	A3	A2	A1
2 WAY INTLV	RAS	(A20	A18)	A16	A15	A14	A13	A12	A11	A10	A17
PAGE MODE	CAS	(A10	A9)	A8	A7	A6	A5	A4	A3	A2	A1
4 WAY INTLV	RAS	(A20	A18)	A16	A15	A14	A13	A12	A11	A18	A17
PAGE MODE	CAS	(A10	A9)	A8	A7	A6	A5	A4	A3	A2	A1
256K DRAM ADDRESS MULTIPLEXER CONFIGURATION											
INDEPENDENT	RAS	(A10)	A9	A8	A7	A6	A5	A4	A3	A2	A1
NON PAGE MODE	CAS	(A20)	A18	A16	A15	A14	A13	A12	A11	A10	A17
INDEPENDENT	RAS	(A20)	A18	A16	A15	A14	A13	A12	A11	A10	A17
PAGE MODE	CAS	(A10)	A9	A8	A7	A6	A5	A4	A3	A2	A1
2 WAY INTLV	RAS	(A20)	A18	A16	A15	A14	A13	A12	A11	A19	A17
PAGE MODE	CAS	(A10)	A9	A8	A7	A6	A5	A4	A3	A2	A1
4 WAY INTLV	RAS	(A20)	A18	A16	A15	A14	A13	A12	A20	A19	A17
PAGE MODE	CAS	(A10)	A9	A8	A7	A6	A5	A4	A3	A2	A1
1 MBIT DRAM ADDRESS MULTIPLEXER CONFIGURATION											
INDEPENDENT	RAS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
NON PAGE MODE	CAS	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17
INDEPENDENT	RAS	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17
PAGE MODE	CAS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
2 WAY INTLV	RAS	A20	A18	A16	A15	A14	A13	A12	A21	A19	A17
PAGE MODE	CAS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
4 WAY INTLV	RAS	A20	A18	A16	A15	A14	A13	A22	A21	A19	A17
PAGE MODE	CAS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
REFRESH ADDRESS - ALL DRAM SIZES											
		A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

TABLE 8. ADDRESS MULTIPLEXER CONFIGURATIONS

Note: Addresses in parentheses are not used by DRAM

SYSTEM BOARD ROM WAIT STATE CONTROL REGISTER

	7	6	5	4	3	2	1	0
FFF50	X	X	X	X	RWS		0	RWSE

This register is cleared to zero by master reset.

RWS	HIGH SPEED WAIT STATE
00 *	1
01	2
10	3
11	4

RWSE=1: Enables RWS, otherwise on-board ROM and RAM Wait States will be set by FE3001A.

The FE3021A can extend the number of processor wait states for an on-board BIOS access by setting the RWSE bit to a '1'. The number of wait states will then be determined by the value of the RWS field. If the RWSE bit is set to a '0', the number of wait states for an on-board BIOS access is controlled by the FE3001A.

The ability to add wait states for BIOS accesses is important for a 16-bit BIOS because the on-board memory read wait states programmed into the FE3001A apply to both on-board BIOS and on-board DRAM. That value will be programmed to optimize DRAM access time (typically zero wait states for page mode operations). This very fast access time will likely be too quick for BIOS ROMs and can therefore be extended for BIOS accesses by setting the RWSE bit.

Bit 1 is used for diagnostic purposes and should remain '0'.

The system BIOS address space may be from F0000 to FFFFF or E0000 to FFFFF. If the EGA BIOS is to be mapped, then the BIOS ROM chip select is also active when the region from C0000 to C3FFF or C0000 to C7FFF is addressed. The address output onto the expansion bus will be automatically translated. The BIOS PROM size and number of wait states will then apply to both the system BIOS region F0000-FFFFF and C0000-C3FFF.

The BIOS EPROM size may either be 8 bits or 16 bits. The EPROM size is determined at reset time, and is signaled by the IORDY line. If the IORDY line is high at the trailing edge of master reset, then the EPROM size is set to 16 bits. If the IORDY line is low at the trailing edge of master reset, then the EPROM size is set to 8 bits. No external logic is required for the 16 bit EPROM size. To select the 8 bit EPROM size, the IORDY line should be pulled low by a master reset. The MDATA bus is used for 16 bit EPROM's while the EDATA bus is used for 8 bit EPROM's.

The $\overline{\text{CSPROM}}$ signal is only active when $\overline{\text{MEMR}}$ is active.

MEMORY ADDRESS RANGE FOR ACTIVE $\overline{\text{CSPROM}}$	FUNCTION
0F0000-0FFFFF FF0000-FFFFFF	BIOS Size = 64K (Default)
0E0000-0FFFFF FE0000-FFFFFF	BIOS Size = 128K
0C0000-0C3FFF	16K EGA BIOS mapping enabled addresses translated to 0F8000-0FBFFF or 0F0000 - 0F3FFF
0C0000-0C7FFF	32K EGA BIOS mapping enabled addresses translated to 0F8000-0FFFFF or 0F0000 - 0F7FFF

EPROM / RAM MAP CONTROL REGISTER

	7	6	5	4	3	2	1	0
FFF51	X	X	X	X	EGA		MS	PS
FFF52	X	X	X	X	XLA	'0'	MLA	FAD

The EPROM/RAM Map Control Register is cleared to zero by a master reset.

EGA=00 MS=X: No EGA mapping.

EGA=01 MS=0: 16K EGA map. C0000 - C3FFF mapped to F8000 - FBFFF

MS=1: 16K EGA map. C0000 - C3FFF mapped to F0000 - F3FFF

EGA=10 MS=0: 32K VGA map. C0000 - C7FFF mapped to F8000 - FFFFF

MS=1: 32K VGA map. C0000 - C7FFF mapped to F0000 - F7FFF

PS = 0: PROM chip select will be active when address is 0F0000-0FFFFF or FF0000-FFFFFF, for 64K of BIOS. Default case after master reset.

PS = 1: PROM chip select will be active when address is 0E0000-0FFFFF or FE0000-FFFFFF, for 128K of BIOS.

XLA=0: LA23 - LA17 low speed timing

XLA=1: LA23 - LA17 high speed timing

MLA=0: LA23 - LA17 latches are transparent during refresh cycles

MLA=1: LA23 - LA17 gated to '0' during refresh cycles

FAD=0: 3 wait state EMS misses

FAD=1: 2 wait state EMS misses

Register FFF52 controls logic for various speed enhancement and diagnostic modes. The XLA bit controls the timing of the LA23 - LA17 signals. Use of this bit can affect compatibility of plug-in bus cards.

When XLA=0, LA23 - LA17 signals are generated by latching the processor addresses by active $\overline{S0}$ or $\overline{S1}$. The LA23 - LA17 latches become transparent when a $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$, or $\overline{IOW}$ strobe occurs. This bit should be 0 when running at 8 MHz, when the FE3001A is using the low speed clock.

When XLA=1, LA23 - LA17 signals are latched by active $\overline{S0}$ or $\overline{S1}$, but do not become transparent again until two CPU clocks after $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$, or $\overline{IOW}$. This delay provides proper 8 MHz bus emulation of the LA23 - LA17 signals when the processor is running at 16 MHz or 20 MHz.

The MLA bit is provided for diagnostic purposes. Bit 2 of register FFF52 is reserved and must be '0'.

The FAD bit can be used to enhance EMS performance for lower speed systems. EMS misses are normally three wait states, which are necessary for 16/20 MHz operation. At 12 MHz and below, EMS misses only need to be two wait states. This bit can be used for the non-page or page mode 2 operation at 12 MHz or below. This bit should remain 0 for page mode 3 or 16/20 MHz operation.

A single contiguous block of memory may be write protected, so that when BIOS ROM is copied into RAM, the RAM copy will not be inadvertently altered. Write protection is accomplished by not asserting CAS when MEMW is active.

RAM Write Protect - Upper Address Boundary

FFF53	X	X	X	X	'1'	A18	A17	A16
	7	6	5	4	3	2	1	0

The Upper Address Boundary Register is cleared by master reset

RAM Write Protect - Lower Address Boundary

FFF55	X	X	X	X	'1'	A18	A17	A16
	7	6	5	4	3	2	1	0

The Lower Address Boundary Register is preset to all 1's by master reset

Master reset clears the upper address boundary registers and presets the lower address boundary registers, which disables write protection. Write protection is enabled on the address range where the RAM address is less than or equal to the upper address boundary as well as greater than or equal to the lower address boundary. Write protection is programmable on 64K boundaries, and the write protection boundaries must be equal to or above 80000H and equal to or below FFFFFH. Write protection will not affect EMS writing even if the EMS window address range is covered by write protection boundaries. This allows protection of BIOS code copied into RAM without affecting operation of EMS.

The memory banks may be programmed to various sizes on 128K boundaries, except the upper split of bank 0, which is programmable on 64K boundaries.

A pair of window registers determines the address range for each memory bank. This allows the banks to be positioned at varying points and in different order than the bank number. If one bank of memory is defective, it can be disabled and the other banks can be programmed to replace it.

Video BIOS is shadowed instead by mapping the EGA/VGA BIOS to F0000 or F8000 and then shadowing the F0000 - FFFFF BIOS area. This method also allows a ROM resident setup program to reside at F0000 in ROM, which can be replaced with EGA/VGA BIOS by shadowing. This method allows a 512K bank to be allocated as 128K of conventional memory, 64K of shadowed VGA and system BIOS, and 320K of extended or EMS memory.

BANK 0 - LOWER SPLIT

Upper Address Boundary

FFF57	**X**	**X**	**X**	**X**	**A19**	**A18**	**A17**	**0/1***
	7	6	5	4	3	2	1	0

Upper boundary must be 0FXXXX or below

BANK 0 - LOWER SPLIT

Lower Address Boundary

FFF59	**X**	**X**	**X**	**X**	**A19**	**A18**	**A17**	**0/1***
	7	6	5	4	3	2	1	0

Lower boundary must be 0FXXXX or below

Upper Address Boundary = 09XXXX (Hex) by master reset

Lower Address Boundary = 09XXXX (Hex) by master reset

BANK 0 - UPPER SPLIT

Upper Address Boundary - MSD

FFF5A	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

Lower Address Boundary - MSD

FFF5C	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

Upper Address Boundary = 00XXXX (Hex) by master reset
Lower Address Boundary = FFXXXX (Hex) by master reset
(upper split disabled)

BANK 0 - UPPER SPLIT

Upper Address Boundary - LSD

FFF5B	X	X	X	X	A19	A18	A17	A16**
	7	6	5	4	3	2	1	0

Lower Address Boundary - LSD

FFF5D	X	X	X	X	A19	A18	A17	A16**
	7	6	5	4	3	2	1	0

* Don't care

** A16 is ignored in early production version (0000, 1011)

BANK 1

Upper Address Boundary - MSD

FFF62	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

Lower Address Boundary - MSD

FFF64	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

Upper Address Boundary = 07XXXX (Hex) by master reset
Lower Address Boundary = 00XXXX (Hex) by master reset

BANK 1

Upper Address Boundary - LSD

FFF63	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

Lower Address Boundary - LSD

FFF65	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

* Don't care

BANK 2

Upper Address Boundary - MSD

FFF66	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

Registers FFF66 and FFF67 are cleared by master reset

BANK 2

Upper Address Boundary - LSD

FFF67	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

Lower Address Boundary - MSD

FFF68	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

Registers FFF68 and FFF69 are preset to all '1s' by master reset

(Bank 2 disabled by master reset)

Lower Address Boundary - LSD

FFF69	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

* Don't care

BANK 3

Upper Address Boundary - MSD

FFF6A	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

Registers FFF6A and FFF6B are cleared by master reset

BANK 3

Upper Address Boundar - LSD

FFF6B	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

Lower Address Boundary - MSD

FFF6C	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

Registers FFF6C and FFF6D are preset to all '1s' by master reset

(Bank 3 is disabled by master reset)

Lower Address Boundary - LSD

FFF6D	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

* Don't care

The RAM banks may be either independent or two-way or four-way page interleaved. DRAM banks which are interleaved must be the same DRAM size.

DRAM SIZE	PAGE SIZE
64K	512 bytes
256K	1024 bytes
1M	2048 bytes

FFF6F	X	X	X	X	0/1*		CFG	
	7	6	5	4	3	2	1	0

* Don't care

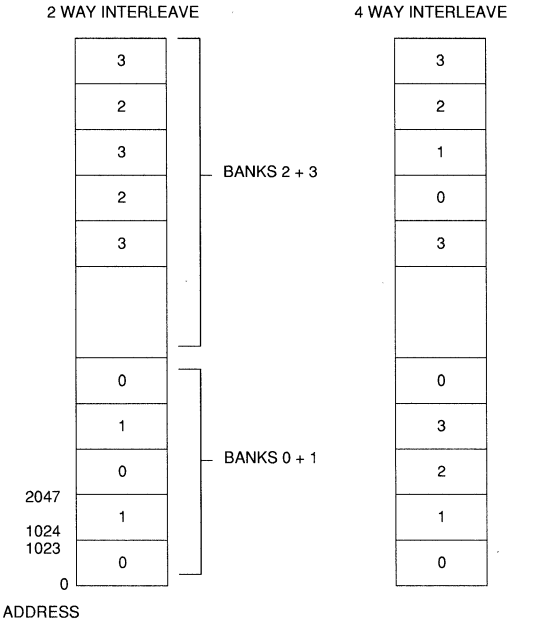
Register FFF6F is not used in non-page mode.

When the memory system operates in page mode, the banks of memory may operate independently or may be interleaved. Interleaving may decrease the average number of wait states, thus increasing performance, but interleaving may only be done if the memory banks to be interleaved are the same size.

CFG	FUNCTION
000*	All banks are independent
011	Bank 2 paired with Bank 3, Banks 0 and 1 are independent
101	Bank 0 paired with Bank 1, Banks 2 and 3 are independent
111	Bank 0 paired with Bank 1, Bank 2 paired with Bank 3
110	All four Banks are interleaved

* Default after master reset

When the memory system operates in page mode, accesses to DRAM in the same page are made with zero wait states. An access to a different page, or the first access to a page after a refresh, DMA, or master cycle will be made either with two wait states for memory mode 2, or three wait states for memory mode 3. The actual page size is variable, depending on the DRAM size.



Multiple banks of memory operating in page mode may operate independently or may be interleaved. Interleaving may decrease the average number of wait states, thus increasing performance, but interleaving may only be done if the memory banks to be interleaved are the same size. Only banks 0 and 1 or banks 2 and 3 may be interleaved together when implementing 2-way interleave. When banks 0 and 1 are interleaved, bank 1 boundary registers should be programmed so that the bank is disabled and the bank 0 boundaries should be programmed as if bank 0 were twice the normal size. As an example, for a system with 2 banks of 256K DRAM operating independently, the banks could be programmed as shown in Figure 4.

When the banks are interleaved, the banks would be programmed as shown Figure 5.

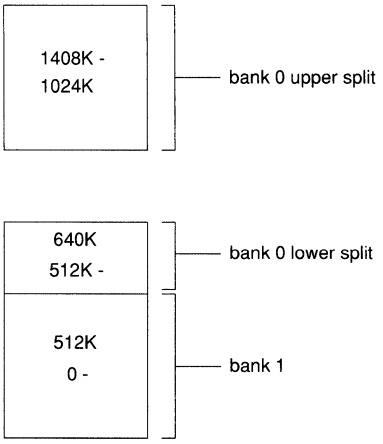


FIGURE 4. BANKS OPERATING INDEPENDENTLY

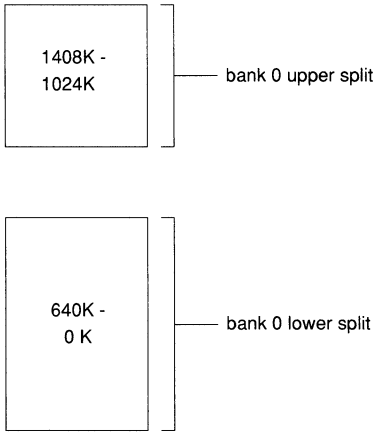


FIGURE 5. BANKS INTERLEAVED

The following tables illustrate memory system characteristics with various configurations of memory and processor speed, both for page mode and non-page mode DRAM access.

For a page mode hit, the read and write accesses may have different performance. For a page mode miss or the first access to a page, the read and write accesses have the same performance. In a page mode miss, $\overline{RAS}$ starts out low and must be brought high for a RAS precharge time before the memory can be accessed.

NON-PAGE MODE	CPU FREQUENCY	WAIT STATES READ	WRITE	EMS MISS	DRAM SPEED
MODE 4	8 MHz	0	0	2	120 ns
MODE 0	16 MHz	1	1	3	80 ns
MODE 4	12.5 MHz	1	1	2	120 ns

PAGE MODE	CPU FREQUENCY	WAIT STATES READ	WRITE	NON-EMS MISS	EMS MISS	DRAM SPEED
MODE 2	16 MHz	0	1	2	3	80 ns
MODE 3	20 MHz	0	1	3	3	80 ns
MODE 3	16 MHz	0	1	3	3	100 ns
MODE 3	12.5 MHz	0	1	3	3	120 ns

The DRAM timing is set by an external delay line for DMA or master mode transfers. The RAS leading edge becomes active from the active level of the $\overline{MEMR}$ or $\overline{MEMW}$ signals.

The DRAM timing modes are programmed by writing into register FFF72. The DRAM timing mode is actually switched during a processor hold state caused by a refresh, DMA, or bus master cycle. The Present DRAM Timing Mode register contains the current timing mode. Registers FFF72 and FFF73 will thus disagree until after a processor hold state occurs; typically, a refresh cycle will occur in 10 to 15 microseconds.

RAM SIZE CONFIGURATION REGISTER - BANK 1 AND 0

FFF70

BNK 1 SZ		BNK 0 SZ	
3	2	1	0

SZ = 00 *: 256K
01 : 1M
10 : RESERVED
11 : 64K

DRAM TIMING MODE

FFF72

X	X	X	X	D	DTYP		
7	6	5	4	3	2	1	0

DRAM TIMING MODE WILL GO INTO EFFECT AFTER REFRESH, DMA, OR OTHER HOLD CYCLE

RAM SIZE CONFIGURATION REGISTER - BANK 3 AND 2

FFF71

BNK 3 SZ		BNK 2 SZ	
3	2	1	0

SZ = 00 *: 256K
01 : 1M
10 : RESERVED
11 : 64K

PRESENT DRAM TIMING MODE

FFF73

X	X	X	X	D	DTYP			READ-ONLY
7	6	5	4	3	2	1	0	

DTYP	DRAM MODE	
000*	Non-page	(MODE 0)
001	Zero wait state read, one wait state write	(MODE 1)
010	Page mode DRAM at 12.5 MHz CPU rate	(MODE 2)
011	Standard page mode for 8-20 MHz CPU rate	(MODE 3)
100	Identical to mode 0, but RAS delayed one-half CPU clock	(MODE 4)
101	Non-page for 8-12 MHz CPU rate,with 0 wait states, RAS pulse width is 2 CPU clocks	(MODE 5)

* Default after master reset
D = 0: Normal operation (default)
D = 1: Reserved for diagnostics; disables DRAM page mode hit/miss logic

8.0 EMS MEMORY

RAM memory above 1024K may be used both for expanded or extended memory. EMS memory may be as small as 128 Kbytes or as large as 7168 Kbytes. The EMS memory is accessed by two sets of EMS Page Registers, which reside in user I/O space. Each set of EMS Page Registers points to 36 blocks of memory, each block 16 Kbytes in size, which make up the EMS Page Frame. Four of the blocks are located above 640K, with the other 32 blocks located between 128K and 640K.

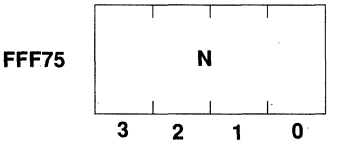
Each EMS Page Register is associated with one page of the EMS Page Frame, and consists of an enable bit and a 10-bit page number. When enabled, a 24-bit real address is formed by taking the 10-bit page number and appending the 14 bit address referencing the byte or word in the EMS page. The 24-bit address is then used to access the DRAM memory controlled by the FE3021A.

In either page mode or non-page mode, if the DRAM row address does not change, then no additional wait states are required for EMS translation. This will allow EMS access without additional wait states if accesses are made to the same 512, 1024, or 2048 byte page, depending on DRAM size.

The EMS hardware must first be configured by programming the EMS control registers located in the FFF00-FFFFF register space, which is unlocked by writing to memory location FFF00 eight times. The I/O port locations of the EMS Page Registers are in user I/O space and their locations are selected with EMS Configuration Registers FFF75 and FFF78.

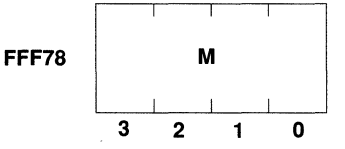
EMS Configuration Register FFF79 is used to completely enable or disable EMS, as well as to switch between the two sets of EMS Page registers. When the 'E' bit is '0', EMS operation is disabled and the EMS registers in user I/O space are inaccessible. When this is '0', it is as if the EMS hardware had been "unplugged" from the bus. When the 'E' bit is a '1', the EMS registers in the user I/O space become accessible. Registers FFF75 and FFF78 (which determine the I/O port addresses for the EMS logic), should be programmed prior to setting the 'E' bit to '1'.

EMS CONFIGURATION REGISTER N



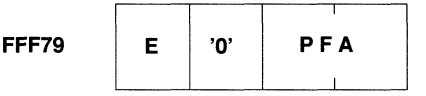
This register is set to '0110' by master reset

EMS CONFIGURATION REGISTER M



This register is set to '1000' by master reset

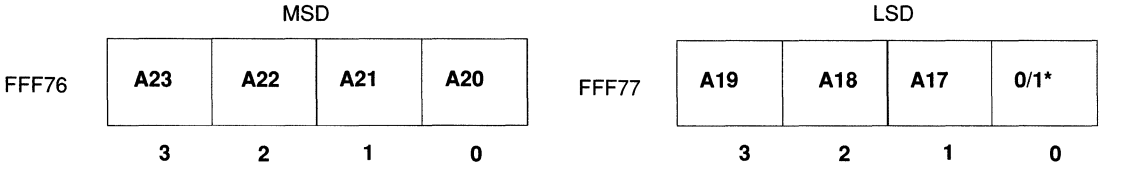
EMS CONFIGURATION REGISTER



E=1: MASTER ENABLE FOR EMS
BIT 2 RESERVED, '0'

PFA = 00 : EMS PAGE FRAME C4000-D3FFF
PFA = 01 : EMS PAGE FRAME C8000-D7FFF
PFA = 10 : EMS PAGE FRAME CC000-DBFFF
PFA = 11 : EMS PAGE FRAME D0000-DFFFF

This register is cleared by master reset



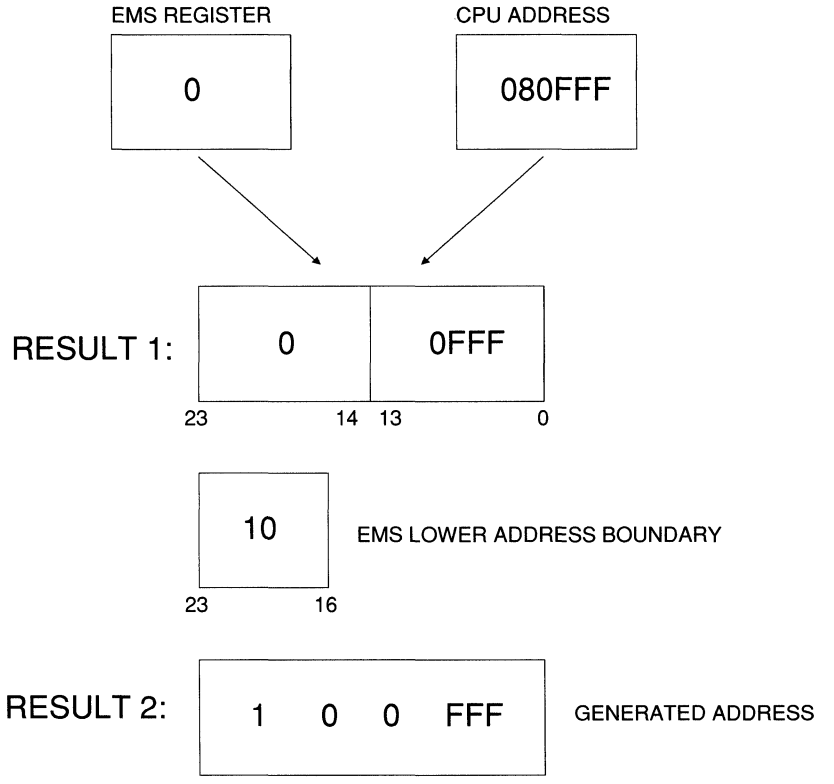
LOWER EMS BOUNDARY

These registers are set to '1111' by master reset

* Don't care

Registers FFF76 and FFF77 are used to allocate memory for EMS, on 128 Kbyte boundaries. Memory with addresses below the EMS boundary is accessed normally, as conventional or extended memory.

On-board memory with addresses above the EMS boundary is reserved for use only as EMS memory. DRAM memory accesses to addresses above the EMS boundary are made to the expansion bus. This allows EMS, off-board, and on-board extended memory to be used simultaneously.



Any CPU address above 1 MB (the EMS lower address boundary), is assumed to reference memory on the expansion bus, rather than on-board memory, which prevents extended memory references from affecting on-board EMS memory.

EMS DMA Control Register FFF7A is used to control the selected EMS map register set during DMA or master transfers. This allows DMA transfers to be made to a particular EMS task, whether or not it is the currently selected task.

On-board memory may be allocated either to extended or to EMS memory in 128 Kbyte blocks. EMS memory is allocated from the top of on-board memory down to the desired limit.

As an example, if the system contained 2 MB of DRAM, the memory map (without EMS) might look similar to Figure 6 (a) on the following page. The system would contain 640K of conventional memory and 1,280K of extended memory. The 1,280K of extended memory is composed of two parts: the original 1,024K and 256K of memory relocated from 0A0000 - 0E0000. The 128K area from 0E0000 - 0F0000 could also be relocated but in this example, it is not.

Figure 6 (b) illustrates the memory map after EMS has been installed. The EMS boundary registers have been programmed so that on-board memory above 1,152K is reserved for EMS. 128K of on-board extended memory remains between 100000 - 120000. Additional extended memory could be added on the expansion bus, starting at 120000. Two EMS areas are shown, one 64K area at 0D0000 - 0E0000, and the other at 020000 - 0A0000.

Figure 6 (c) shows the possible EMS page numbers ranging from 0 - 4F for the 1,280K of memory available for EMS paging.

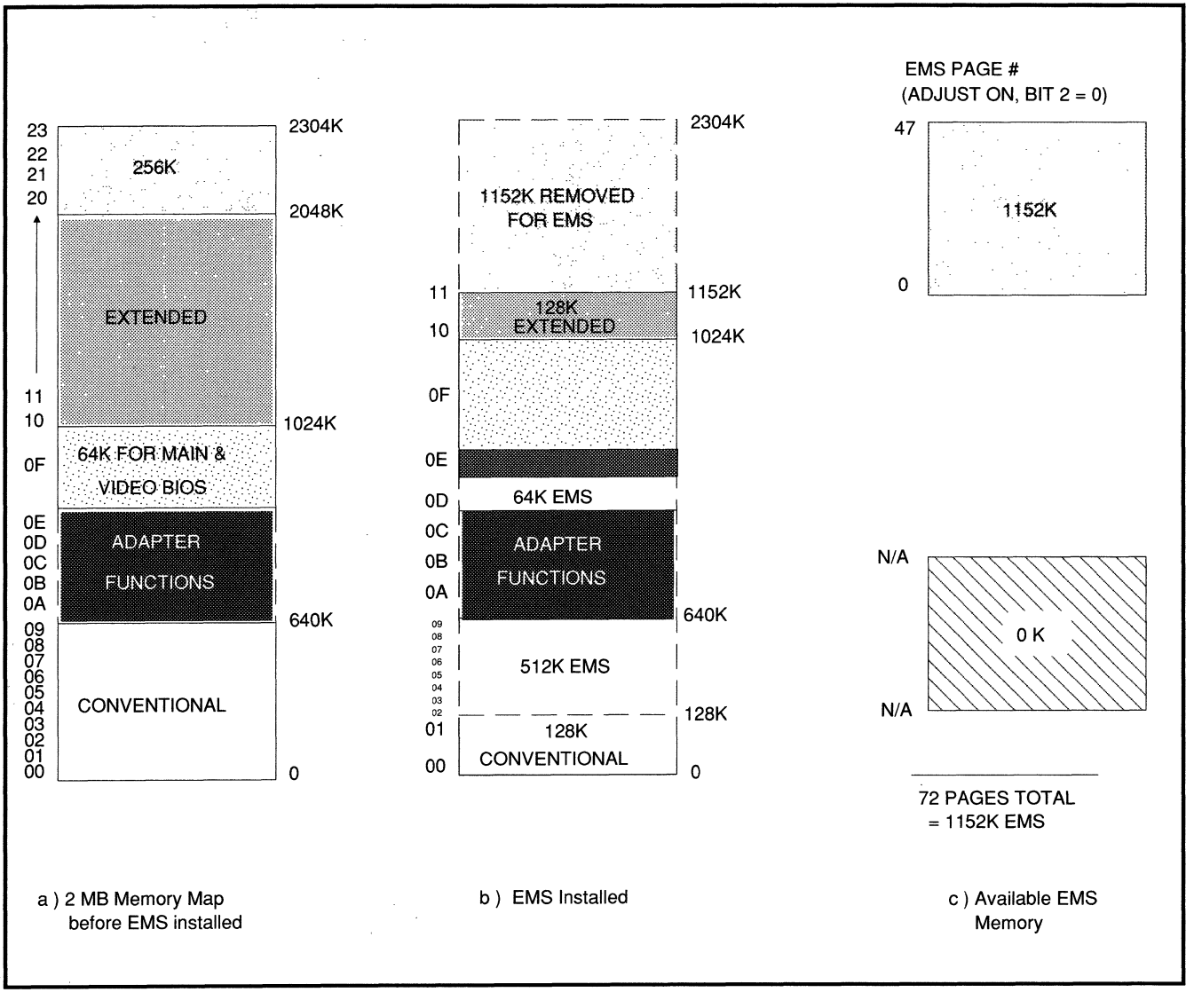


FIGURE 6. EMS/MEMORY MAP CONFIGURATIONS

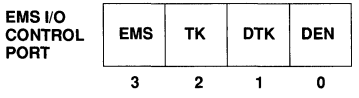
The EMS Control Register and EMS Page Registers are addressed in the user I/O port address space, I/O ports 100 (hex) through 3FF (hex). The EMS Control Registers and EMS Page Registers are selected when the I/O port address bits 9 - 6 match the value 'M' programmed by register FFF78 and the I/O port address bits 5 - 2 match the value 'N' programmed by register FFF75.

The EMS I/O Control Port is used to enable or disable EMS translation. When EMS translation is disabled, the EMS I/O control port and EMS page registers may still be accessed, but EMS page swapping will not occur.

The EMS I/O Control Port is also used to select the active page register set. When the processor accesses EMS memory, it always uses the register set specified by the TK bit. Normally, when DMA accesses EMS memory, it also uses the register set specified by the TK bit. Alternatively, the DMA transfer may be made using a particular register set, independently of the register set currently being used by the processor. This allows a DMA operation to start, continue, and finish while the processor is time-slicing and swapping back and forth between two programs.

The P and W fields for each page register are specified in the following table. Each EMS Page register is composed of a one bit enable bit (E) and a 10-bit page number (Q9-Q0). EMS translation for the EMS page is enabled when the E bit is a '1'.

EMS CONTROL REGISTER

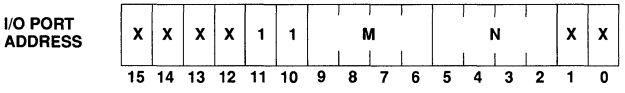


EMS = 1: EMS TRANSLATION ENABLED

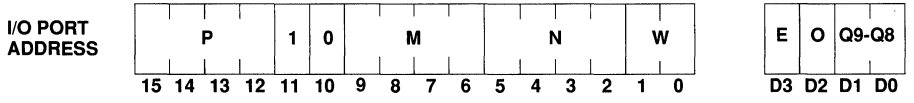
DEN = 0 : DMA TRANSFERS MADE TO MAP REGISTER SET SPECIFIED BY "TK" BIT

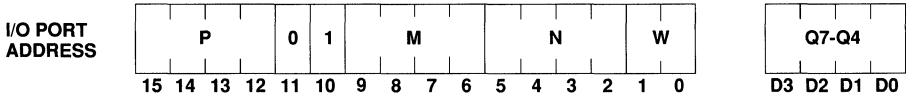
DEN = 1 : DMA TRANSFERS MADE TO MAP REGISTER SET SPECIFIED BY "DTK" BIT

EMS CONTROL REGISTER ADDRESS LOCATION

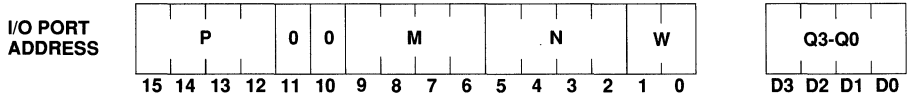


EMS PAGE REGISTER - MSD





EMS PAGE REGISTER - LSD



P	W	EMS PAGE			
		PFA=00	PFA=01	PFA=10	PFA=11
0000	11	D0000-D3FFF	D4000-D7FFF	D8000-DBFFF	DC000-DFFFF
0000	10	CC000-CFFFF	D0000-D3FFF	D4000-D7FFF	D8000-DBFFF
0000	01	C8000-CBFFF	CC000-CFFFF	D0000-D3FFF	D4000-D7FFF
0000	00	C4000-C7FFF	C8000-CBFFF	CC000-CFFFF	D0000-D3FFF
1001	11	9C000-9FFFF	624K TO 640K		
1001	10	98000-9BFFF	608K TO 624K		
1001	01	94000-97FFF	592K TO 608K		
1001	00	90000-93FFF	576K TO 592K		
1000	11	8C000-8FFFF	560K TO 576K		
1000	10	88000-8BFFF	544K TO 560K		
1000	01	84000-87FFF	528K TO 544K		
1000	00	80000-83FFF	512K TO 528K		
0111	11	7C000-7FFFF	496K TO 512K		
0111	10	78000-7BFFF	480K TO 496K		
0111	01	74000-77FFF	464K TO 480K		
0111	00	70000-73FFF	448K TO 464K		
0110	11	6C000-6FFFF	432K TO 448K		
0110	10	68000-6BFFF	416K TO 432K		
0110	01	64000-67FFF	400K TO 416K		
0110	00	60000-63FFF	384K TO 400K		
0101	11	5C000-5FFFF	368K TO 384K		
0101	10	58000-5BFFF	352K TO 368K		
0101	01	54000-57FFF	336K TO 352K		
0101	00	50000-53FFF	320K TO 336K		
0100	11	4C000-4FFFF	304K TO 320K		
0100	10	48000-4BFFF	288K TO 304K		
0100	01	44000-47FFF	272K TO 288K		
0100	00	40000-43FFF	256K TO 272K		
0011	11	3C000-3FFFF	240K TO 256K		
0011	10	38000-3BFFF	224K TO 240K		
0011	01	34000-37FFF	208K TO 224K		
0011	00	30000-33FFF	192K TO 208K		
0010	11	2C000-2FFFF	176K TO 192K		
0010	10	28000-2BFFF	160K TO 176K		
0010	01	24000-27FFF	144K TO 160K		
0010	00	20000-23FFF	128K TO 144K		

TABLE 9. EMS PAGE REGISTER INFORMATION

9.0 TEST MODE

All output pins will become tri-stated if $\overline{\text{YMEMR}}$ and $\overline{\text{YMEMW}}$ are active simultaneously while $\overline{\text{MR}}$ is active. The outputs will remain tri-stated if $\overline{\text{MR}}$ is brought inactive while $\overline{\text{YMEMR}}$ and $\overline{\text{YMEMW}}$ are both active. The outputs will become active drivers again when $\overline{\text{MR}}$ is brought low without both $\overline{\text{YMEMR}}$ and $\overline{\text{YMEMW}}$ active. This "all output tri-state" mode allows an in-circuit board tester to drive the FE3021A output pins.

10.0 FE3021A PINOUT

The FE3021A is packaged in a 132-pin plastic quad flat pack. Table 10 lists the pins according to their function.

AT BUS	
LA23	63
LA22	70
LA21	71
LA20	93
LA19	95
LA18	102
LA17	103
ADDR19	59
ADDR18	61
ADDR17	62
ADDR16	64
ADDR15	65
ADDR14	66
ADDR13	68
ADDR12	69
ADDR11	72
ADDR10	73
ADDR9	75
ADDR8	94
ADDR7	96
ADDR6	97
ADDR5	98
ADDR4	100
ADDR3	101
ADDR2	104
ADDR1	106
ADDR0	105
$\overline{\text{MASTER}}$	52

DATA BUS	
EDATA3	17
EDATA2	16
EDATA1	15
EDATA0	14

CHIP SELECTS & CONTROL	
$\overline{\text{CS0}}$	48
$\overline{\text{CS1}}$	47
$\overline{\text{CS2}}$	46
$\overline{\text{CS3}}$	45
CSF	49
$\overline{\text{CS8042}}$	60
$\overline{\text{CS287}}$	56
$\overline{\text{CSNMI}}$	20
$\overline{\text{CSPTB}}$	22
ADSTB	53
$\overline{\text{SELDAT}}$	40
$\overline{\text{YMEMR}}$	10
$\overline{\text{YMEMW}}$	11
$\overline{\text{YIOR}}$	12
$\overline{\text{YIOW}}$	13
$\overline{\text{IOR}}$	8
$\overline{\text{IOW}}$	9

MEMORY ADDRESS MUX	
RA9	41
RA8	39
RA7	38
RA6	37
RA5	36
RA4	35
RA3	34
RA2	33
RA1	32
RA0	31
$\overline{\text{RAS}}$	58
$\overline{\text{TAP1}}$	44
$\overline{\text{TAP2}}$	26

80286 INTERFACE	
A23	74
A22	78
A21	79
A20	80
A19	81
A18	82
A17	83
A16	84
A15	85
A14	86
A13	87
A12	88
A11	89
A10	90
A9	109
A8	110
A7	111
A6	112
A5	113
A4	114
A3	115
A2	116
A1	117
A0	118
$\overline{\text{S0}}$	119
$\overline{\text{S1}}$	120
M/$\overline{\text{IO}}$	121
CPUCLK	122
HLDA	123
IORDY	127

RESET	
$\overline{\text{RESET}}$	28
$\overline{\text{FRES}}$	19

MEMORY CONTROL	
$\overline{\text{RAS0}}$	128
$\overline{\text{RAS1}}$	129
$\overline{\text{RAS2}}$	130
$\overline{\text{RAS3}}$	132
$\overline{\text{CASL0}}$	125
$\overline{\text{CASL1}}$	126
$\overline{\text{CASL2}}$	2
$\overline{\text{CASL3}}$	3
$\overline{\text{CASH0}}$	4
$\overline{\text{CASH1}}$	5
$\overline{\text{CASH2}}$	6
$\overline{\text{CASH3}}$	131
$\overline{\text{REFR}}$	18
$\overline{\text{CSPROM}}$	43
$\overline{\text{ONBD}}$	57
$\overline{\text{BHE}}$	21
$\overline{\text{DLE}}$	23
ADR0	24
$\overline{\text{LOMEG}}$	25
A20GT	54

GROUND	POWER
1	7
27	30
29	50
42	55
51	77
67	92
76	107
91	
99	
108	
124	

TABLE 10. PIN LISTING

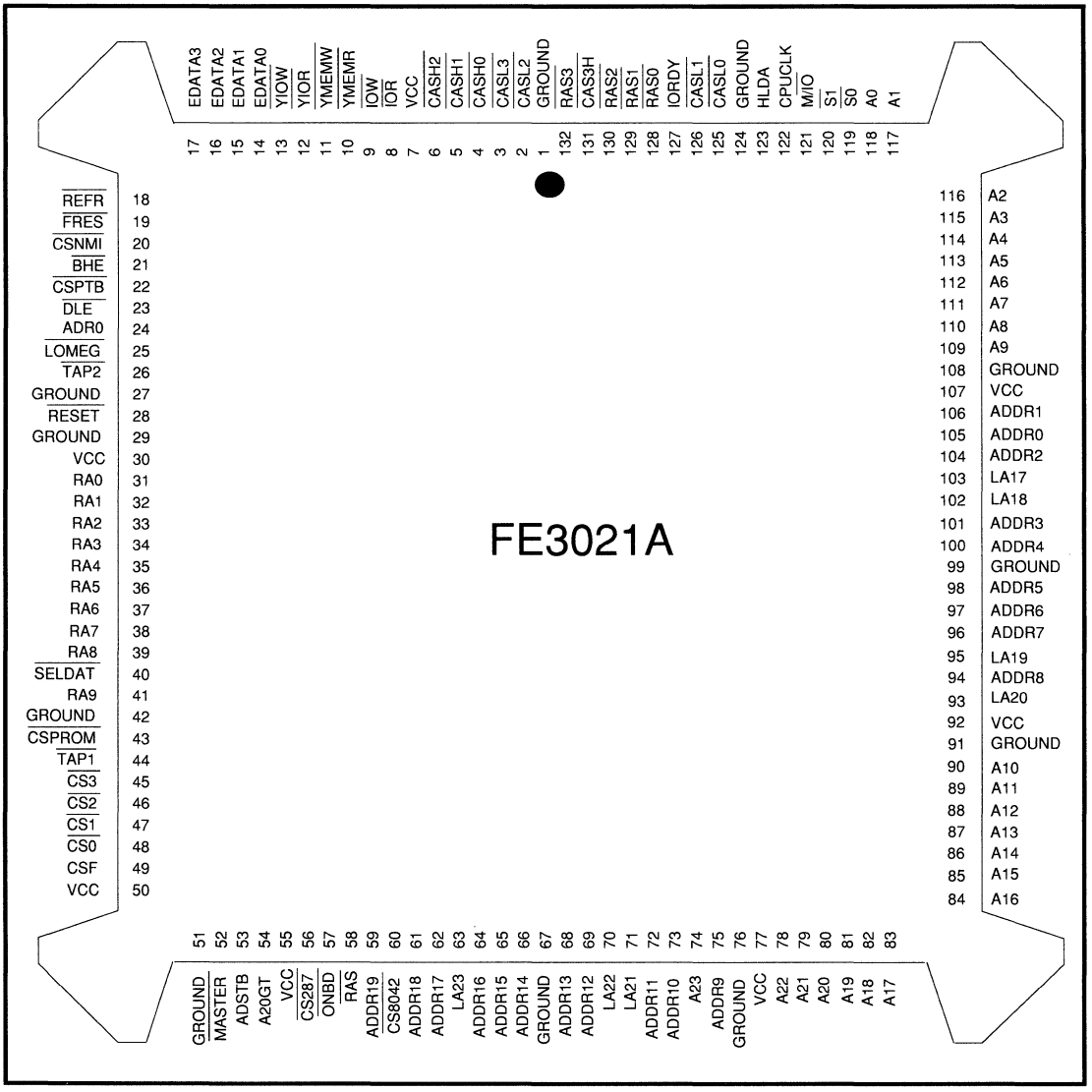


FIGURE 7. (PQFP) PLASTIC QUAD FLAT PACK PIN ASSIGNMENTS

11.0 ELECTRICAL SPECIFICATIONS

11.1 MAXIMUM RATINGS

Supply Voltage (VCC) with respect to VSS (ground) . . . . . -0.5V to +7V
Operating temperature . . . . . 0°C (32°F) to 70°C (158°F)
Storage temperature . . . . . -40°C (-40°F) to 125°C (257°F)
Power dissipation . . . . . 500 mW

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Operating Characteristics.

11.2 DC OPERATING CHARACTERISTICS

T_a = 0°C (32°F) to 70°C (158°F), Vcc = 5 V ± .25 V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
IIL	Input Leakage		±10	µA	VIN = .4 TO VCC
IOZ	Tri-state And Open Drain Output Leakage		±10	µA	VOUT = .4 TO VCC
VIH	Input High Voltage	2.0		V	
VIL	Input Low voltage		.8	V	
VIHC	CPU Clock Input High Voltage	.6		V	
VILC	CPU Clock Input Low Voltage		.6	V	
ICC	Supply Current		50	mA	All outputs open, inputs at 2.0V, CPUCLK = 16 MHz

TABLE 11. DC OPERATING CHARACTERISTICS

For outputs $\overline{YIOR}$, $\overline{YIOW}$, RA[9:0], $\overline{ONBD}$, $\overline{LOMEG}$, A[23:0], CSF, $\overline{CS[3:0]}$, $\overline{CS8042}$, $\overline{CS287}$, $\overline{CSNMI}$, $\overline{CSPTB}$, $\overline{RAS}$, $\overline{RAS[3:0]}$, $\overline{CASL[3:0]}$, $\overline{CASH[3:0]}$, $\overline{CSPROM}$, $\overline{DLE}$, $\overline{FRES}$, $\overline{SELDAT}$, and EDATA[3:0]

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
VOH	Output High Voltage	2.4		V	IOUT = -1 mA
VOL	Output Low Voltage		.4	V	IOUT = 1 mA

TABLE 11. DC OPERATING CHARACTERISTICS cont.

For outputs ADDR[19:0], LA[23:17], $\overline{IOR}$, $\overline{IOW}$, IORDY

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
VOH	Output High Voltage	2.4		V	IOUT = -3 mA
VOL	Output Low Voltage		.4	V	IOUT = 12 mA*

TABLE 11. DC OPERATING CHARACTERISTICS cont.

* 10 mA for $\overline{IOR}$, $\overline{IOW}$.

11.3 AC TIMING CHARACTERISTICS

Load Capacitance = 20 pF for output: $\overline{DLE}$

Load Capacitance = 50 pF for outputs: CSF, $\overline{CS[3:0]}$, $\overline{CS8042}$, $\overline{CS287}$, $\overline{CSNMI}$ $\overline{CSPTB}$, $\overline{SELDAT}$, $\overline{RA[9:0]}$, $\overline{ONBD}$, $\overline{LOMEG}$, $\overline{RAS}$, $\overline{CSPROM}$, $\overline{YIOR}$, $\overline{YIOW}$, $\overline{FRES}$

Load Capacitance = 100 pF for output: IORDY, A[19:0], EDATA[3:0], $\overline{CASL[3:0]}$, $\overline{CASH[3:0]}$

Load Capacitance = 200 pF for outputs: $\overline{RAS[3:0]}$, LA[23:17], ADDR[19:0], $\overline{IOR}$, $\overline{IOW}$

SYMBOL	CHARACTERISTIC	PRELIMINARY 12 MHz		PRELIMINARY 16 MHz		PRELIMINARY 20 MHz	
		MIN	MAX	MIN	MAX	MIN	MAX
T1	CPUCLK Cycle	40		31		25	
T2	CPUCLK High Pulse	13		12			
T3	CPUCLK Low Pulse	11		10			
T4	A[23:0], M/$\overline{IO}$ Setup To $\overline{S0}$ Or $\overline{S1}$ Falling	22		16		12	
T5	A[23:0], M/$\overline{IO}$ To $\overline{ONBD}$, Memory Cycle		56		33		27
T5a	A[23:6], M/$\overline{IO}$ to $\overline{ONBD}$, I/O cycle		56		33		22
T6	$\overline{S0}$, $\overline{S1}$ Setup To CPUCLK Falling	20		11		8	
T7	$\overline{S0}$, $\overline{S1}$ Hold From CPUCLK Falling	3		2		1	
T10	M/$\overline{IO}$, A[23:0] To LA[23:17]		50		45		45
T13	$\overline{YMEMR}$ To $\overline{CSPROM}$		45		46		46

TABLE 12. SYSTEM TIMING

SYMBOL	CHARACTERISTIC	PRELIMINARY 12 MHz		PRELIMINARY 16 MHz		PRELIMINARY 20 MHz	
		MIN	MAX	MIN	MAX	MIN	MAX
T14	ADSTB To $\overline{CS[3:0]}$, $\overline{CSPTB}$, CSF, $\overline{CSNMI}$, $\overline{CS8042}$		45		37		37
T14a	ADSTB To $\overline{CS287}$		45		37		30
T14b	CPUCLK Falling To CS287 ROM Cycle		44		44		44
T15	CPUCLK Falling To $\overline{LOMEG}$		43		43		43
T17a	$\overline{YIOR}$ To $\overline{IOR}$		40		35		35
T17	$\overline{YIOW}$ To $\overline{IOW}$		40		35		35
T18	ADSTB To ADDR[19:1]		78		59		45
T19	ADR0 To ADDR0		45		40		40
T20	Data Valid From $\overline{YMEMR}$ Or $\overline{YIOR}$ Active		180		150		140
T22	LA[23:17] From CPUCLK Falling		50		45		45
T24	Data Setup To $\overline{YMEMW}$ Or $\overline{YIOW}$ Inactive		180	150		150	
T25	Data Hold From $\overline{YMEMW}$ Or $\overline{YIOW}$ Inactive	10		10		10	
T26	$\overline{YIOR}$ Or $\overline{YMEMR}$ To $\overline{SELDAT}$		55		55		55
T27	$\overline{IOR}$ To $\overline{SELDAT}$, Master Mode Cycle		50		45		45
T28	ADSTB To Row Address; DMA Cycle, NON-EMS		50		47		47
T28a	ADSTB To Row Address; DMA Cycle, EMS		180		147		147
T29	$\overline{YMEMR}$ To $\overline{RAS}$, $\overline{RAS[3:0]}$, Refresh Cycle		36		36		36
T30	$\overline{YMEMR}$ Or $\overline{YMEMW}$ To $\overline{RAS}$; DMA Cycle		35		30		30
T31a	TAP1 Falling To ROW Address Invalid	5		5		5	
T31b	$\overline{TAP1}$ Falling To Column Address Valid		45		T33+18		T33+12
T32	$\overline{YMEMR}$ Or YMEMW To $\overline{RAS[3:0]}$, DMA Cycle		35		30		30

TABLE 12. SYSTEM TIMING cont.

SYMBOL	CHARACTERISTIC	PRELIMINARY 12 MHz		PRELIMINARY 16 MHz		PRELIMINARY 20 MHz	
		MIN	MAX	MIN	MAX	MIN	MAX
T33	$\overline{TAP2}$ Falling To $\overline{CASL[3:0]}$, $\overline{CASH0}$, DMA Cycle		30		29		29
T34	$\overline{YMEMR}$ Or $\overline{YMEMW}$ Rising To $\overline{CASL[3:0]}$ Or $\overline{CASH[3:0]}$ Inactive		35		29		29
T35	$\overline{YMEMR}$ Active To $\overline{DLE}$ Active; DMA Or Master Mode		40		32		32
T36	$\overline{YMEMR}$ inactive To $\overline{DLE}$ Inactive: DMA Or Master Mode		40		32		32
T37	$\overline{BHE}$ Or ADR0 Setup To CPUCLK Falling	25		20		20	
T38a	ADR0 Setup To CPUCLK Falling	25		20		20	
T38b	$\overline{BHE}$ Setup To CPUCLK Falling	25		20		20	
T39	A[23:1] To RA[9:0] Row Address; Mode 0, 1, 4, 5		45		27		27
T40	$\overline{TAP1}$ Falling To RA[9:0] Column Address; Mode 0, 1, 4, 5		45		29		29
T41	RA[9:0] Row Address Valid From CPUCLK At End Of $\overline{CAS[3:0]}$		50		47		47
T43	CPUCLK Falling To $\overline{RAS}$; Mode 0, 1, 5		35		30		30
T44	CPUCLK Falling To $\overline{RAS[3:0]}$, Mode 0, 1, 5		35		30		30
T47	$\overline{TAP2}$ Falling To $\overline{CASL[3:0]}$, Or $\overline{CASH[3:0]}$, Active; Mode 0, 1, 4, 5		35		29		29
T48	CPUCLK Falling To $\overline{CASL[3:0]}$, Or $\overline{CASH[3:0]}$ Inactive; Mode 0, 1, 4, 5		35		27		27
T49	ROW Address From Middle Of TS		52		52		
T50	$\overline{TAP2}$ Falling To $\overline{DLE}$ Active; Mode 0, 1, 4, 5		35		32		32

TABLE 12. SYSTEM TIMING cont.

SYMBOL	CHARACTERISTIC	PRELIMINARY 12 MHz		PRELIMINARY 16 MHz		PRELIMINARY 20 MHz	
		MIN	MAX	MIN	MAX	MIN	MAX
T51	CPUCLK Falling To $\overline{DLE}$ Inactive; Mode 0, 1, 4, 5		35		35		35
T52a	Ready Low From $\overline{S0}$ Or $\overline{S1}$ Low		35		30		25
T52b	Ready Low From CPUCLK Rising		35		30		25
T53	Ready High From CPUCLK Falling		35		30		30
T54	Column Address From CPUCLK Falling				T57+30		N/A
T56	$\overline{RAS[3:0]}$ Active From CPUCLK Falling				30		N/A
T57	$\overline{CAS[3:0]}$ Active From CPUCLK Rising				23		N/A
T58	$\overline{CAS[3:0]}$ Inactive From CPUCLK Rising				23		N/A
T59a	$\overline{DLE}$ Active From CPUCLK Falling		35		30		30
T59b	$\overline{DLE}$ Inactive From CPUCLK Rising		T68+5		T68+5		T68+5
T60	Row Address Valid From CPUCLK Falling; Mode 3		52		52		52
T61a	$\overline{RAS[3:0]}$ Inactive From CPUCLK Falling		30		30		30
T62	$\overline{RAS[3:0]}$ Inactive From HLDA Active		40		35		35
T63	Column Address Hold From End Of $\overline{CAS[3:0]}$	1		1		1	
T64	Column Address From CPUCLK; Mode 2 & 3		50		T67+30		T67+21
T65	Column Address From A[23:1]		45		T67+19		T67+13
T66	$\overline{RAS[3:0]}$ Active From CPUCLK Rising; Mode 3		35		30		26
T67	$\overline{CASL[3:0]}$ Or $\overline{CASH[3:0]}$ Active From CPUCLK; Mode 3		28		19		19

TABLE 12. SYSTEM TIMING cont.

SYMBOL	CHARACTERISTIC	PRELIMINARY 12 MHz MIN	PRELIMINARY 12 MHz MAX	PRELIMINARY 16 MHz MIN	PRELIMINARY 16 MHz MAX	PRELIMINARY 20 MHz MIN	PRELIMINARY 20 MHz MAX
T68	$\overline{CASL}$[3:0] Or $\overline{CASH}$[3:0], Inactive From CPUCLK Rising; Mode 3		28		23		23
T6867	Difference Of $\overline{CAS}$[3:0] Inactive And Active Time (T[68:67])		4		4		N/A
T69	$\overline{REFR}$ To $\overline{ONBD}$		50		50		50
T70	Refresh Address Valid From $\overline{REFR}$		50		50		50
T72	$\overline{MASTER}$ Active To LA[23:17], ADDR[16:0] High Impedance		45		45		45
T73	$\overline{MASTER}$ Inactive To LA [23:17], ADDR [16:0] Low Impedance		45		45		45
T74	ADDR[9:0] To Chip Selects		65		65		65
T75	$\overline{MASTER}$ Active to A[23:0], ADR0 Low Impedance		45		45		45
T76	$\overline{MASTER}$ Inactive To A[23:0], ADR0 High Impedance		45		45		45
T77	LA[23:17], ADDR[16:1] To RA[9:0]		45		42		42
T77a	LA[23:17], ADDR [16:1] To RA [9:0] - EMS Cycle		198		198		198
T78	$\overline{MASTER}$ Active To $\overline{YIOR}$, $\overline{YIOW}$ Low Impedance		45		45		45
T79	$\overline{MASTER}$ Inactive To $\overline{YIOR}$, $\overline{YIOW}$ High Impedance		45		45		45
T80	$\overline{MASTER}$ Active To $\overline{IOR}$, $\overline{IOW}$ High Impedance		45		45		45
T81	$\overline{MASTER}$ Inactive To $\overline{IOR}$, $\overline{IOW}$ Low Impedance		45		45		45
T82a	$\overline{IOR}$ To $\overline{YIOR}$		30		25		25
T82b	$\overline{IOW}$ To $\overline{YIOW}$		30		25		25
T83	LA[23:17], ADDR[16:0] To A[23:0], ADR0		40		35		35

TABLE 12. SYSTEM TIMING cont.

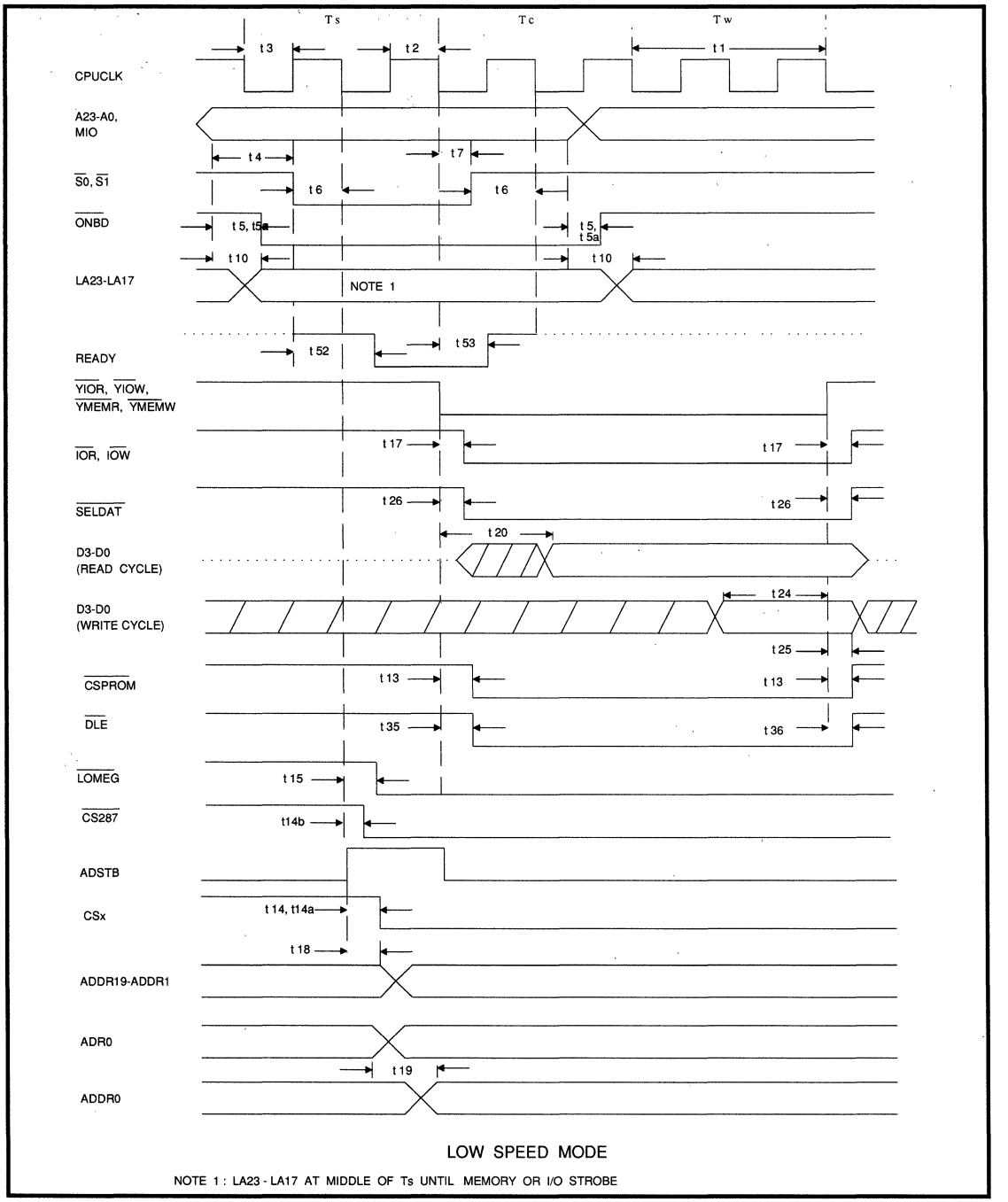


FIGURE 8. BASIC TIMING

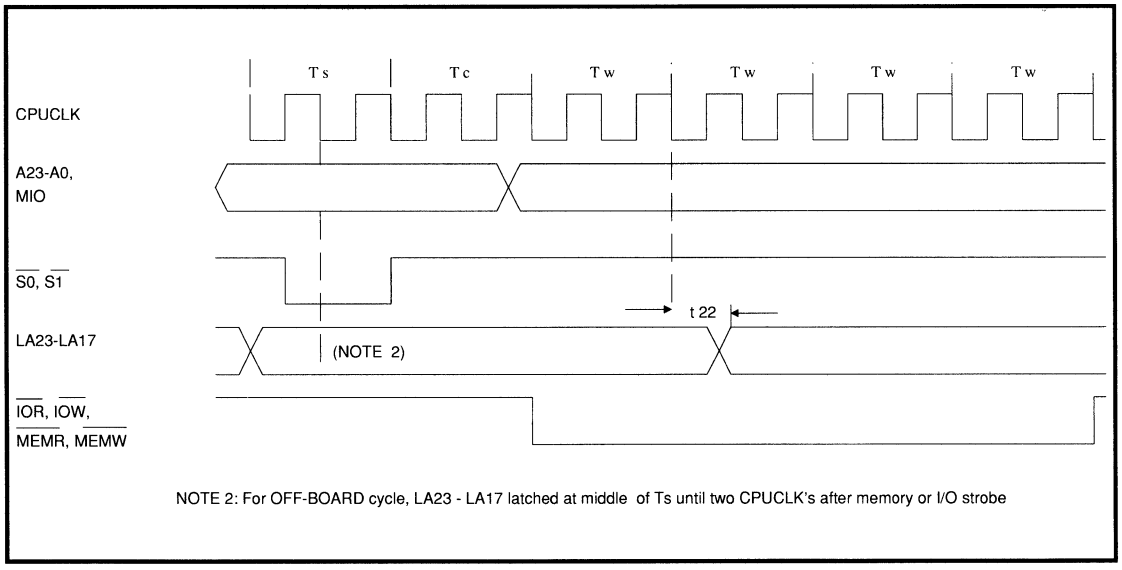


FIGURE 9. HIGH SPEED MODE LA23-LA17 TIMING

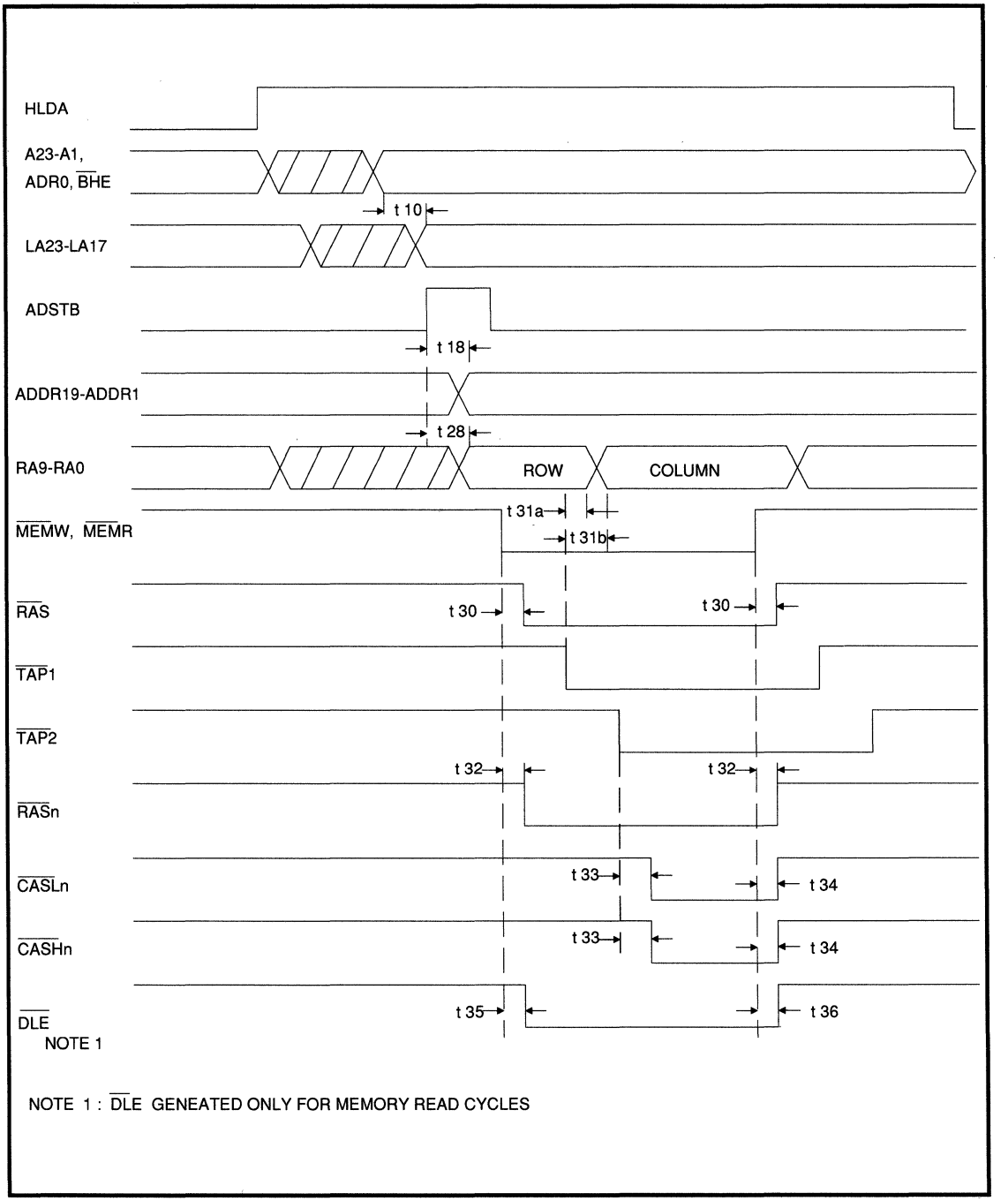


FIGURE 10. DMA MEMORY CYCLE

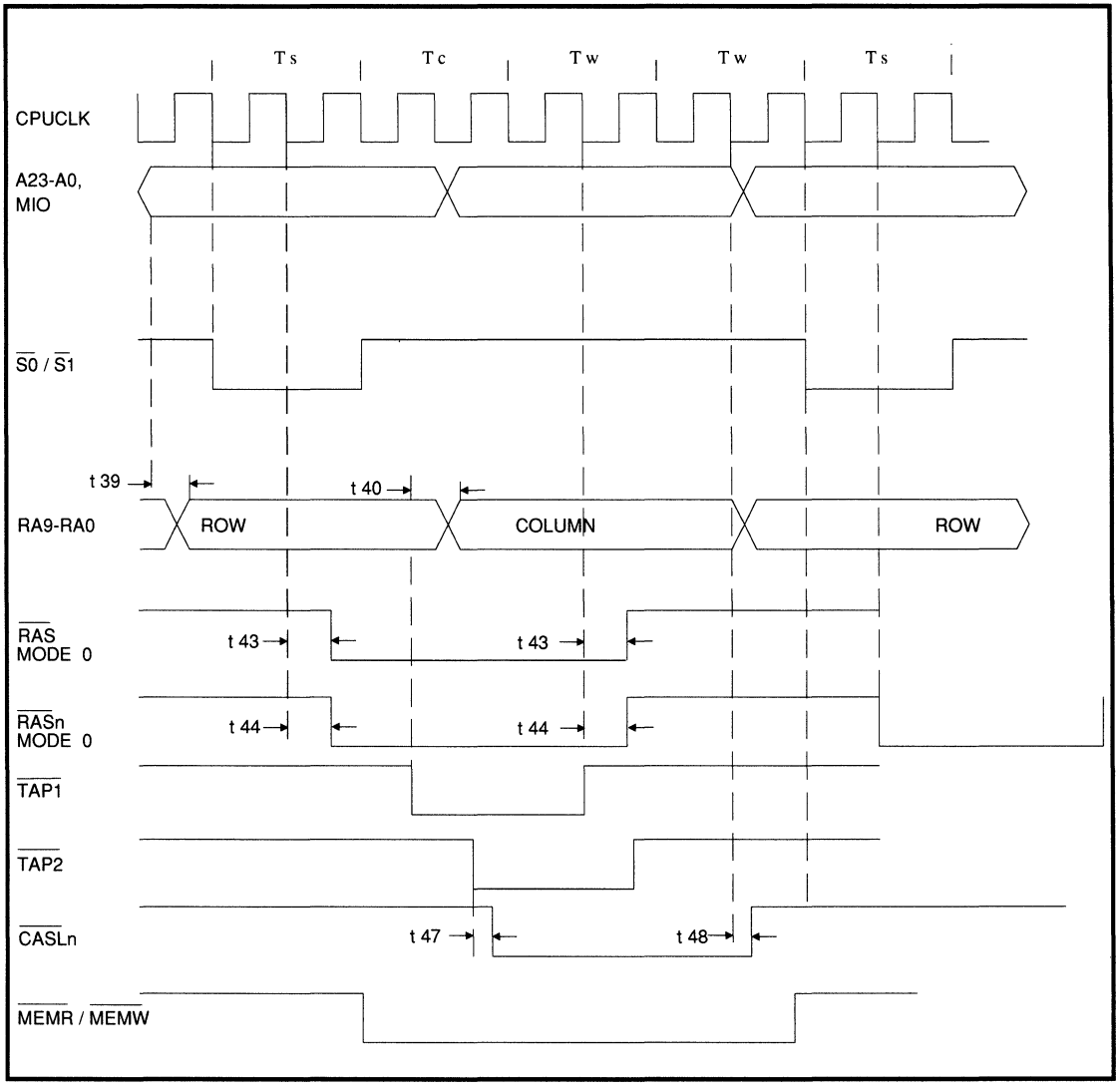


FIGURE 11. MEMORY MODE 0 (NON-PAGE MODE)

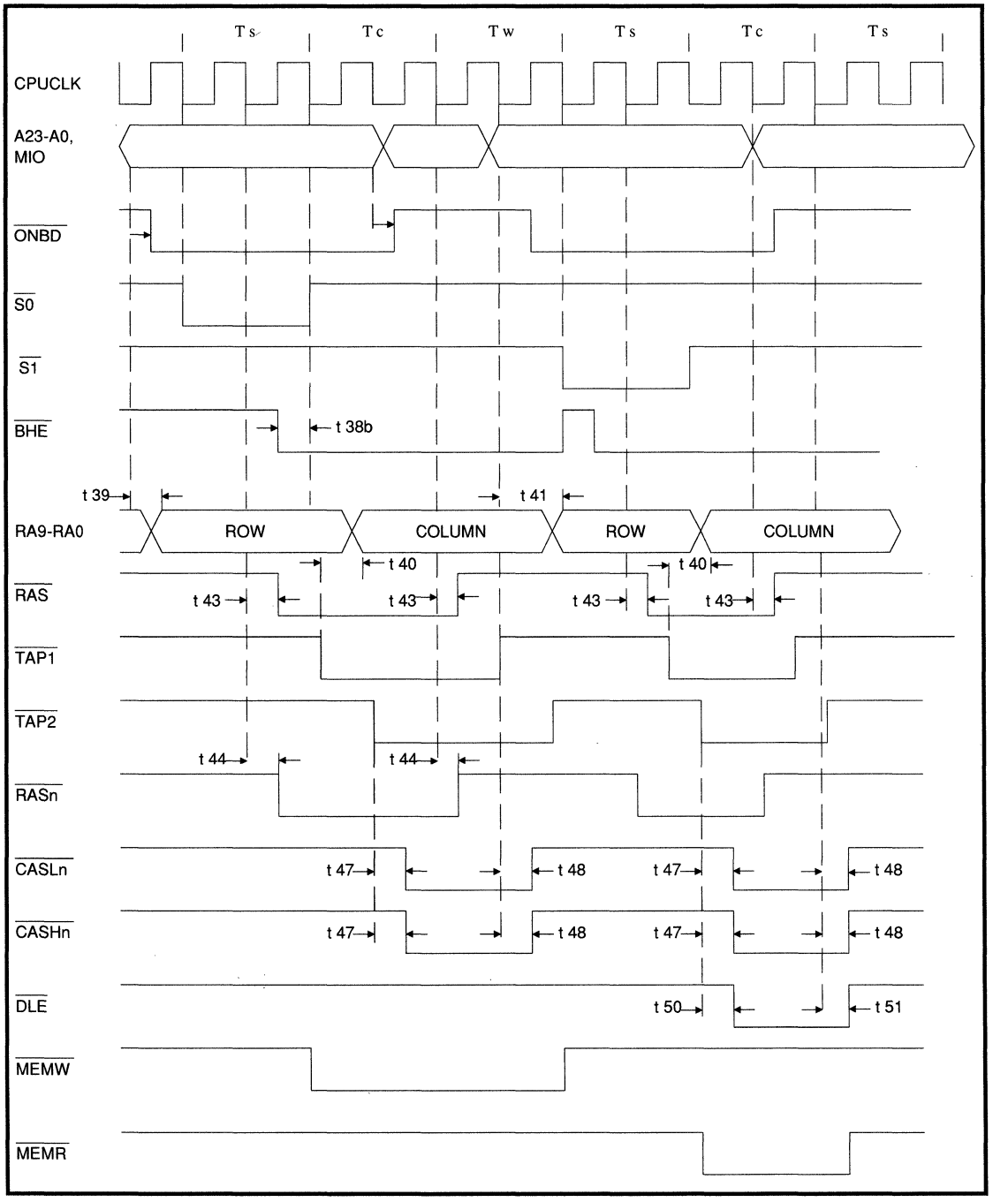


FIGURE 12. MEMORY MODE 1 (NON-PAGE 0 WS READ - 1 WS WRITE)

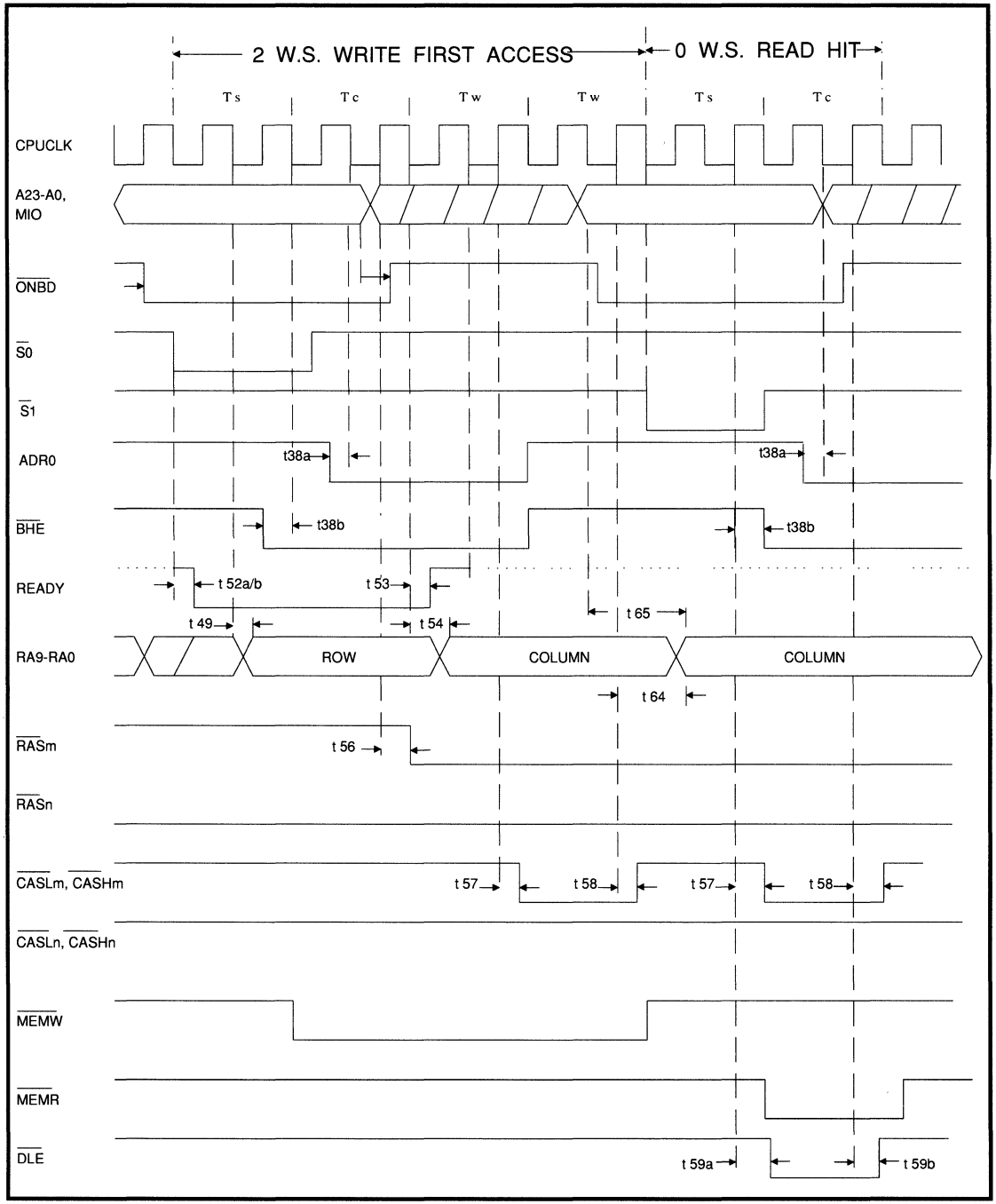


FIGURE 13. MEMORY MODE 2 (PAGE) 1 OF 2

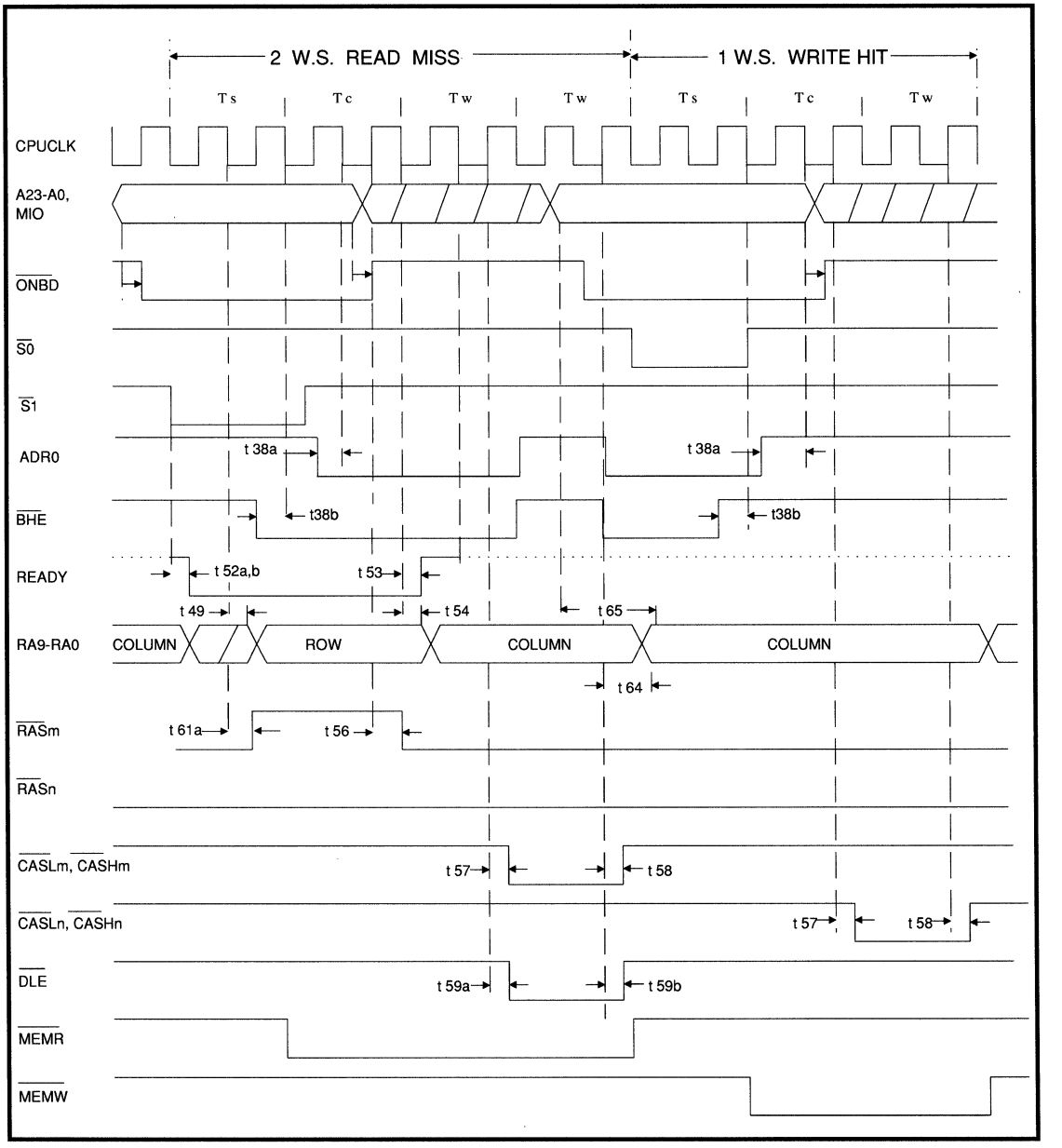


FIGURE 14. MEMORY MODE 2 (PAGE) 2 OF 2

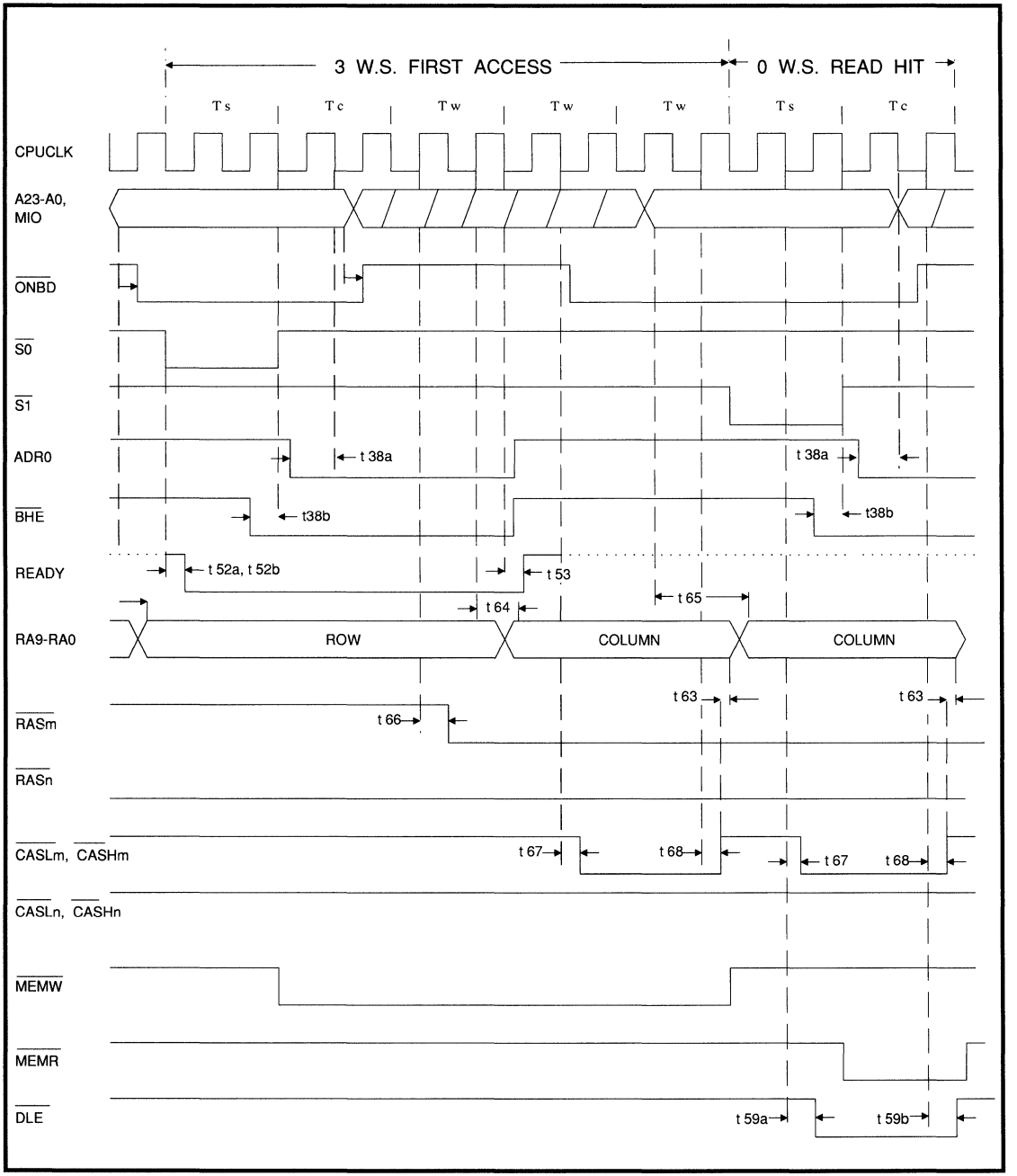


FIGURE 15. MEMORY MODE 3 (PAGE) 1 OF 2

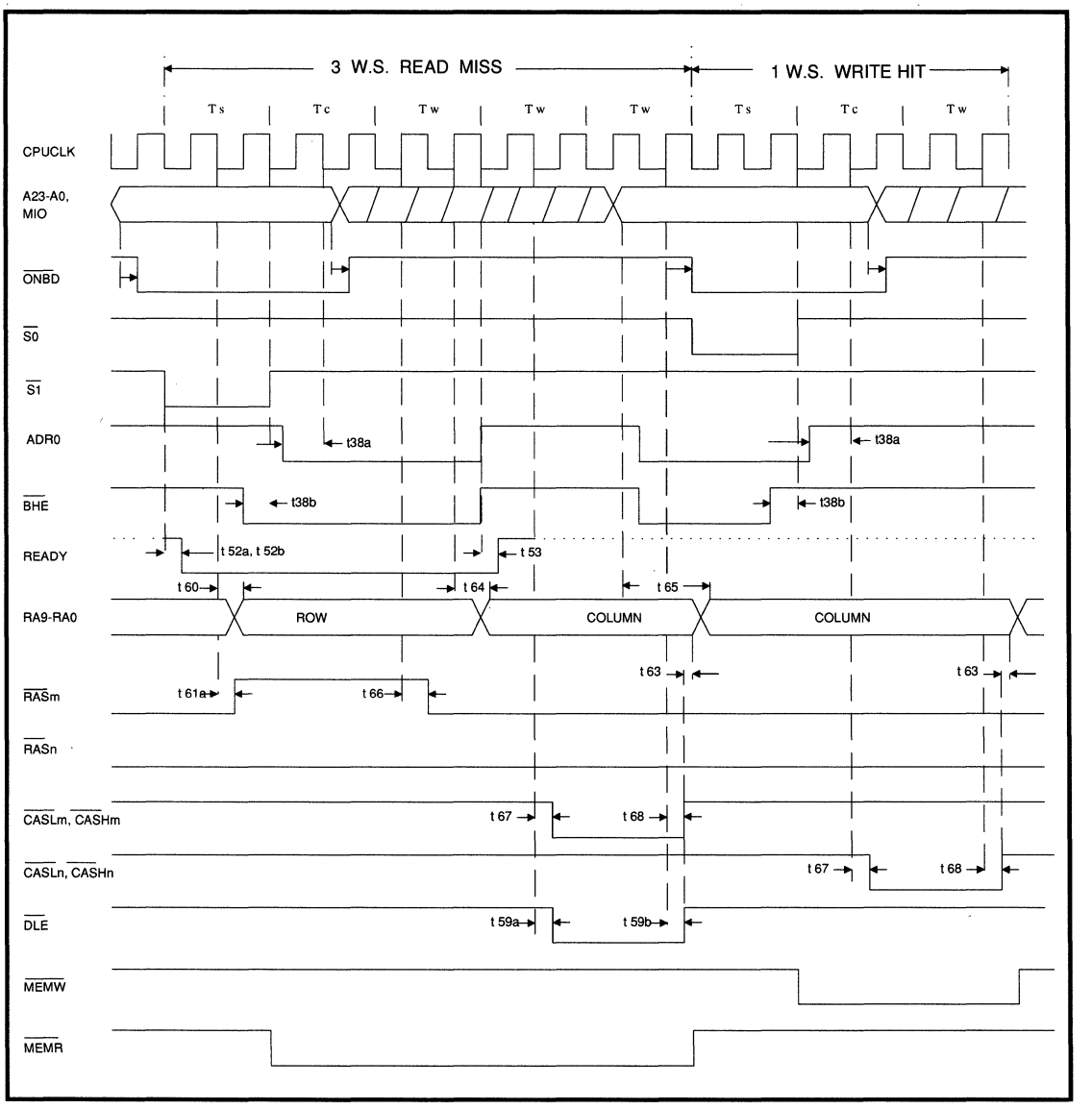


FIGURE 16. MEMORY MODE 3 (PAGE) 2 OF 2

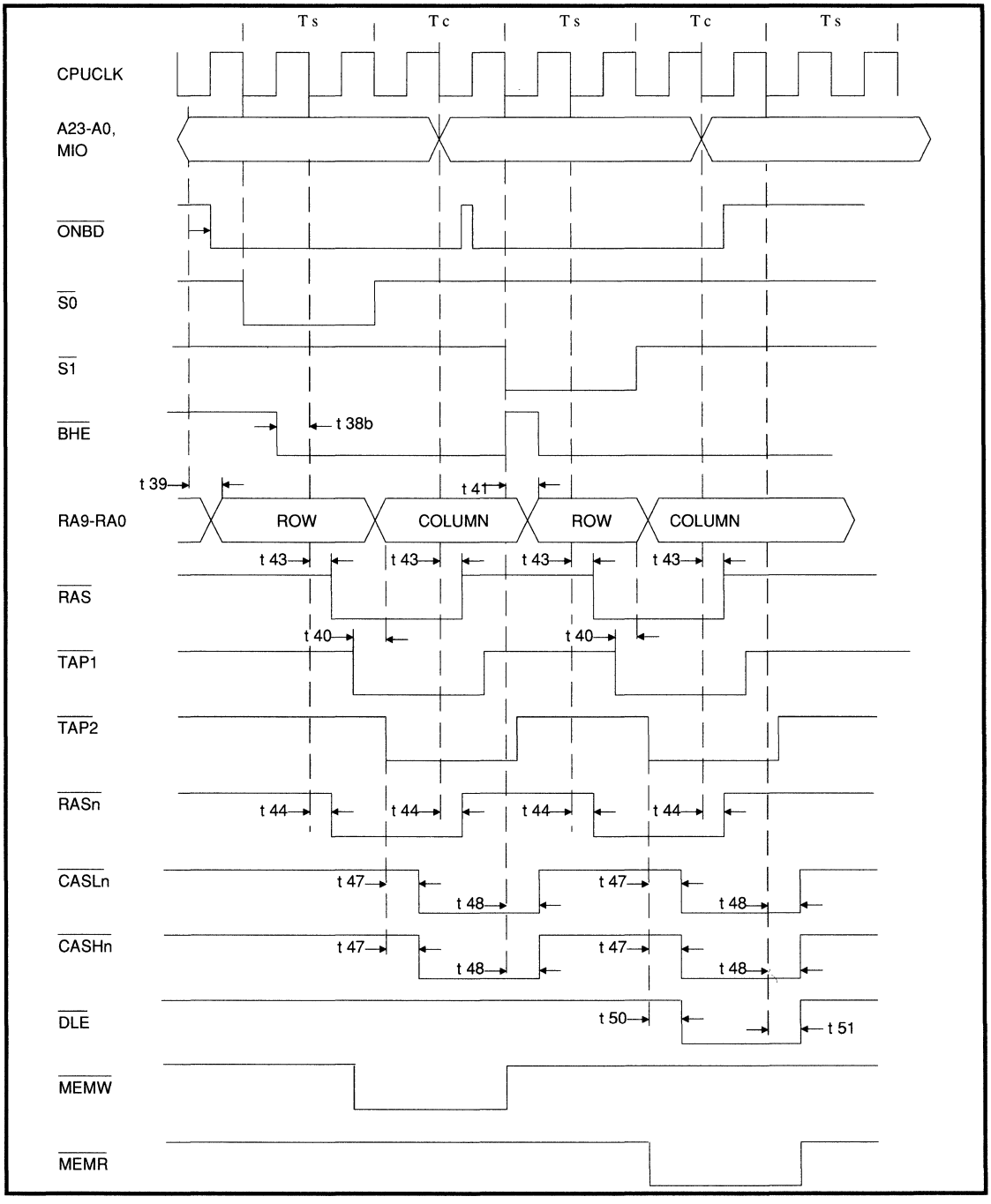


FIGURE 17. MEMORY MODE 5 (NON-PAGE) 0 WS READ AND WRITE

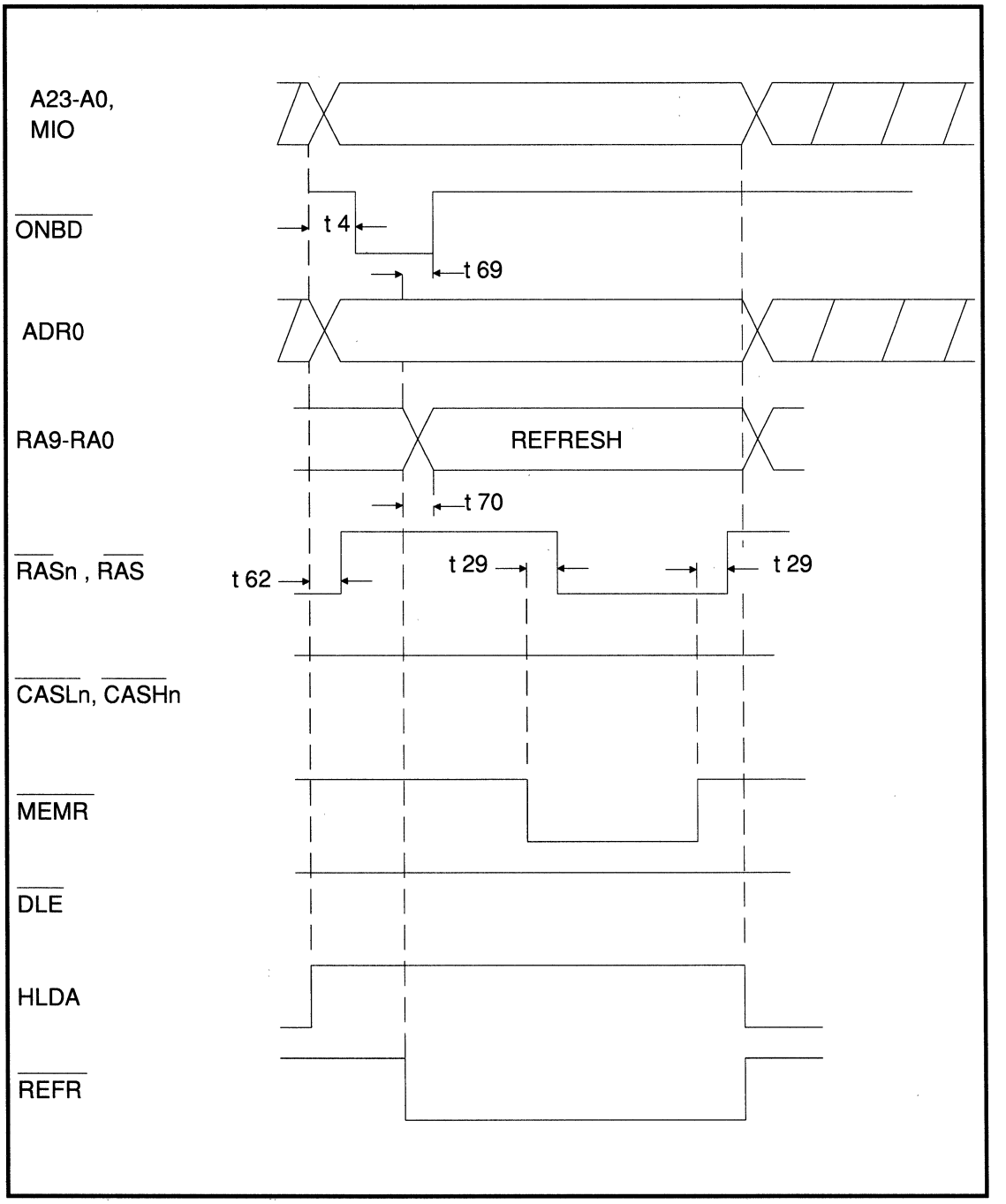
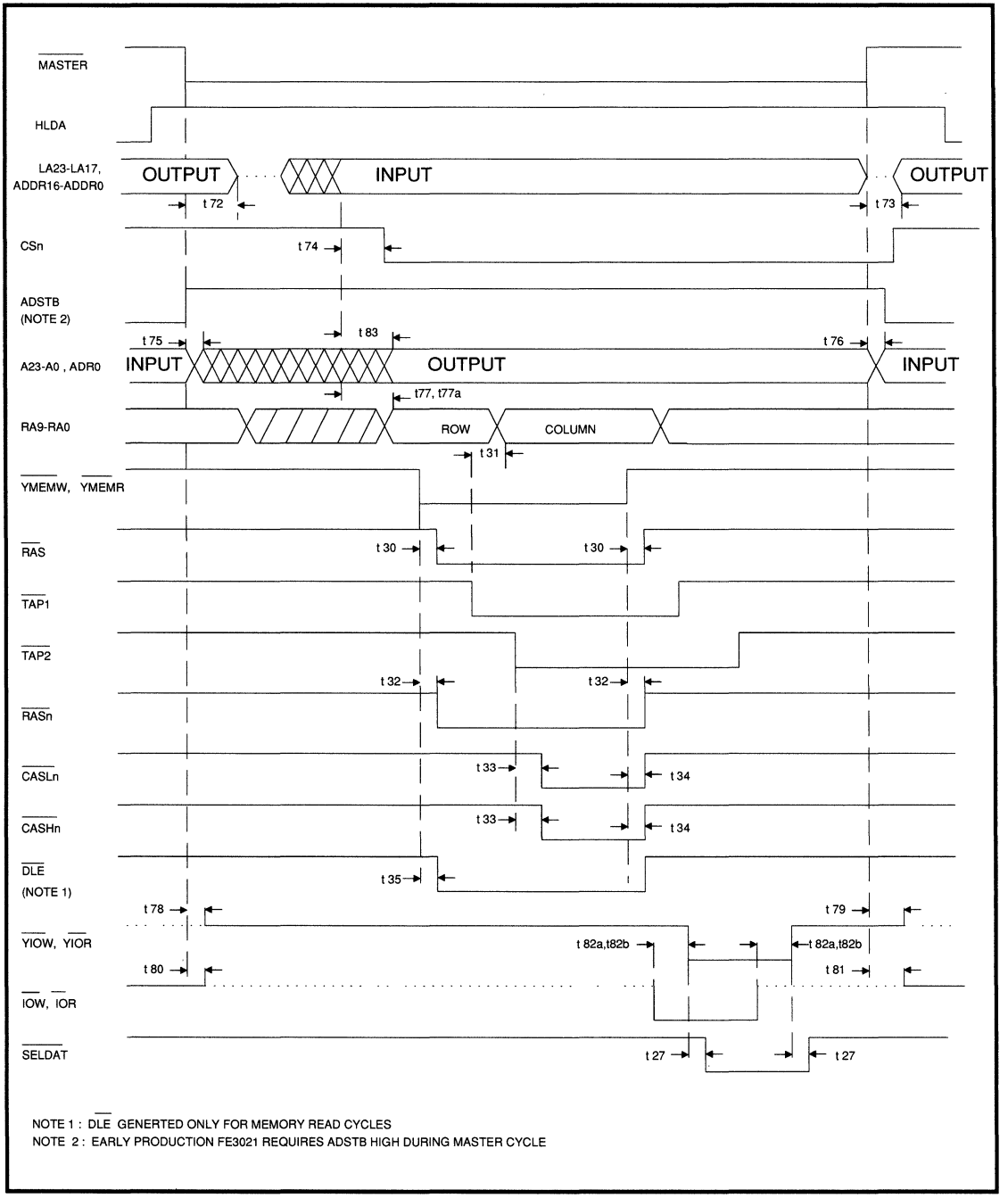


FIGURE 18. REFRESH CYCLE



NOTE 1 : DLE GENERTED ONLY FOR MEMORY READ CYCLES
NOTE 2 : EARLY PRODUCTION FE3021 REQUIRES ADSTB HIGH DURING MASTER CYCLE

FIGURE 19. BUS MASTER CYCLE

12.0 PACKAGE DIAGRAM

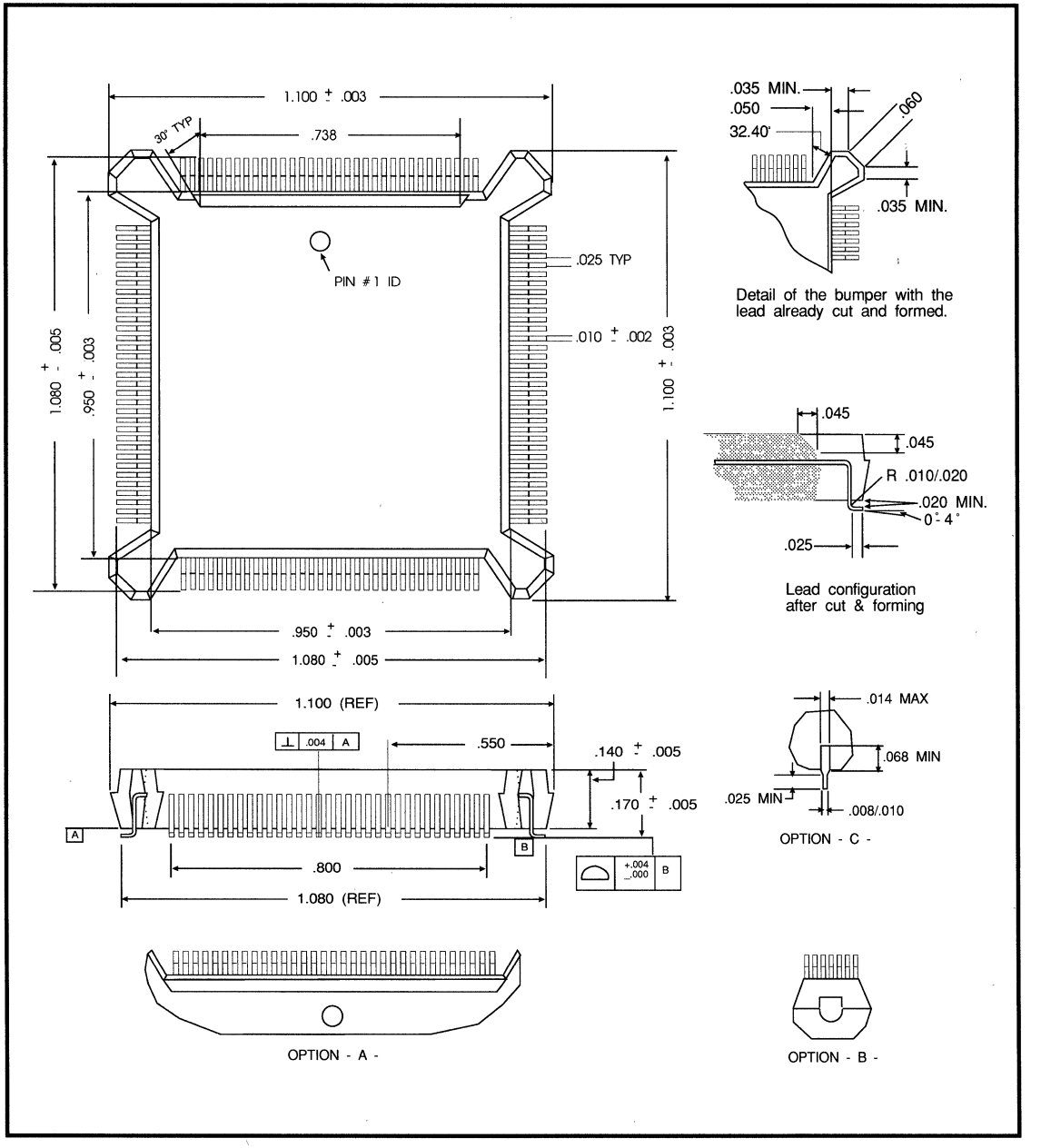


FIGURE 20. 132-PIN PQFP PACKAGE