CPU Core Logic for 80386 MCA-Compatibles

FE6500

Advance Information

Features

- Five Chip Core Logic Implementation of 80386-based Micro Channel* Architecture-Compatible Computers
  - FE6000 CPU and Peripheral Control Device
  - FE6010 DMA & Arbitration Control Device
  - FE6022 Address or Data Buffer Device *(2 Devices Required)*
  - FE6030 Cache DRAM, and Channel Control Device
- 100% Hardware (Register Level) and Software-Compatible with the IBM* Micro Channel Architecture
- Operates at 16, 20, 25, or 33 MHz CPU Clock Rates
- Hierarchical Caching Subsystem
  - Direct-Mapped, Write-through Implementation
  - Cache Line Size up to 4 Bytes
  - Page Mode Hits on Cache Misses
- 256K, 1 MB, or 4 MB DRAM support
- Shadow RAM
- Highest Level of Integration Available
- Extended Setup Facility™ (ESF)™
- 1.25 Micron CMOS Implementation
- Available in Surface Mountable 132-pin JEDEC Plastic Quad Flat Packaging (PQFP)

Product Overview

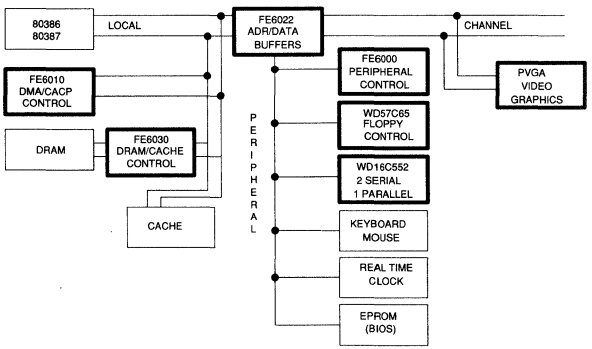
The Western Digital ® FE6500 Chip Set provides the critical core logic to build a highly integrated Micro Channel Architecture-compatible system board using the 32-bit Intel * 80386 Central Processing Unit.

The FE6500 Chip Set is 100% Hardware (Register Level) and Software-Compatible with IBM's Micro Channel Architecture. All IBM* Micro Channel timing specifications are met.

The FE6500 Chip Set operates at 16, 20, 25, or 33 MHz CPU clock rates, so Original Equipment Manufacturers can choose the optimal price/performance for the market in which they choose to compete.

The Extended Setup Facility (ESF) is a fully-compatible enhancement that allows designers to add more functionality (i.e., Winchester Controller, LAN Adapter, Additional Serial Port) to the system board.

The FE6500 Chip Set significantly facilitates the design and implementation of system boards that have higher performance, more features, reduced EMI, less power consumption, and a smaller footprint.



FE6500 CHIP SET FUNCTIONAL BLOCK DIAGRAM

CPU Core Logic for 80386 MCA-Compatibles

FE6500 Devices

The FE6500 Chip Set consists of five devices: The FE6000, FE6010, FE6022 (2), and FE6030.

The FE6000 CPU and Peripheral Control Logic Device contains the equivalent functions of two Intel 8259 Interrupt Controllers (16 Channels), a 3-Channel 8254 Timer, Watchdog Timer Logic, System Board I/O Decode Logic, the Peripheral Bus Control Generator, NMI Generator, Error Control Logic, Programmable Option Select (POS) Logic. Weitek* 3167 and 80387 Math Coprocessor Support is provided. Clock Generation Logic for the Keyboard Controller is included. Support for External CMOS RAM for Storage of Configuration Data is provided.

The FE6010 DMA and Arbitration Control Logic Device contains two 8237-compatible DMA controllers with extensions and the Central Arbitration Control Logic (CACP). An optional Enhanced Mode extends the DMA address space up to 4 Gigabytes. The DMA Controller has an 80386-compatible bus interface and runs at the full speed of the 80386. Controls to support the 80387 at half the processor speed are provided. The FE6010 also includes Reset and Generation Logic.

The FE6022 Address or Data Buffer Device interfaces directly to the Channel and meets all Channel AC/DC specifications including a 24 milliamp output drive capability. The FE6022 may be configured as an address buffer or a data buffer, as determined by a mode pin. ***Two FE6022s are required.***

The FE6030 is a Cache, DRAM, and Channel Control Device.

Cache: To ensure the best possible performance at higher speeds, the FE6030 supports an external cache of any size, with a direct-mapped, write-through cache for the 80386 with a line-size of up to four bytes, that executes 80386 bus cycles, DMA, and Channel master bus cycles.

The cache subsystem delivers high performance by ensuring zero wait state cache read-hits, and a low, one wait state miss overhead. Zero wait state access is achieved on a cache read-hit , and cache misses are supported by page mode DRAMs which provide fast, one wait state access for page hits. Implementing a cache will improve performance by up to 45% over ordinary RAS/CAS operations.

DRAM Controls: The FE6030 supports page mode reducing the wait states to main memory. Shadow RAM is provided for fast BIOS execution.

The FE6030 supports 256 KB, 1 MB, and 4 MB DRAMs, including the ability to mix DRAM types. Up to 4 banks of DRAM are supported on the System Board. Up to 16 MB can be supported on the system board using 256 KB DRAMs; 16 MB using 1 MB DRAMs; 64 MB using 4 MB DRAMs. The memory configuration and wait states are programmable.

Channel Controls : The FE6030 provides control for a 32-bit Channel interface.

Integration: The FE6500 chip set is a highly integrated chip set. The benefits of integration include increased reliability, reduced board space, lower power consumption, and reduced product cost.

Packaging: The FE6500 Chip Set devices are all manufactured in JEDEC Standard surface mountable 132-pin Plastic Quad Flat Packs (PQFP). This type of packaging facilitates the design of devices having a higher level of logic integration.

AMP* Inc., which is headquartered in Harrisburg, Pennsylvania, produces sockets for the 132-pin JEDEC Standard Package (Part Number 821932-5). Contact your local AMP representative for more information.

Western Digital Corporation
2445 McCabe Way
Irvine, CA 92714
(800) 847-6181 (714) 863-0102
FAX (714) 660-4909 Telex 910-595-1139

WESTERN DIGITAL

WD 00261 5/89

80386 MCA-Compatible System Design Kit

FE6500-SK

Advance Information

Features

- ❑ 100% Hardware (Register Level) and Software Compatible with IBM's Micro Channel* Architecture
- ❑ 20 MHz CPU Clock Rate
- ❑ Intel* 80387 and Weitek* 3167 Coprocessor Support
- ❑ Western Digital's FE6500 CPU Core Logic
- ❑ Western Digital/Phoenix* BIOS, 100% Model 80-Compatible
- ❑ 1 MB DRAM, Expandable to 16 MB On-Board
- ❑ Page Mode
- ❑ 64 KB of Cache Memory
- ❑ VGA Controller with 16-Bit High Speed Interface (PVGA1)
- ❑ Built-in Floppy Disk Controller (WD57C65)
- ❑ Buffered, High Speed Serial Port; Bi-directional Parallel Port (WD16C552)
- ❑ Seven Expansion Slots, Including an Auxiliary Video Extension
- ❑ Model 80 Form Factor
- ❑ Through-hole PCB

Product Overview

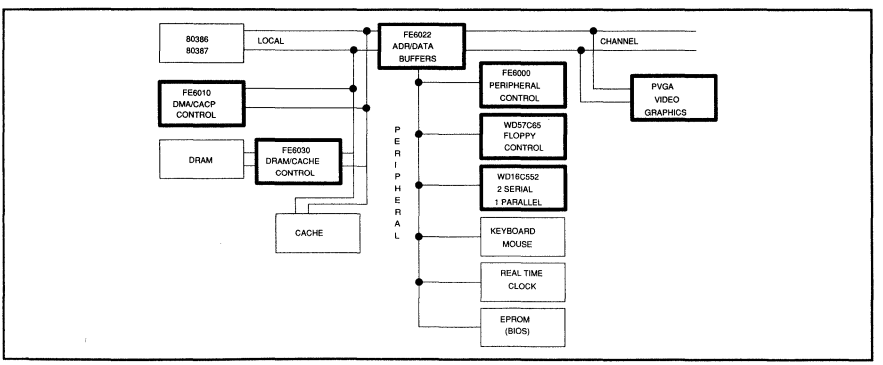
The Western Digital ® FE6500-SK System Design Kit is an evaluation board designed to demonstrate the capabilities of the FE6500 chip set. It is compatible with the Model 70/80 on both hardware register level and software level. The FE6500-SK is form factor-compatible with the Model 80 chassis.

Based on the FE6500 core logic chip set, the FE6500-SK operates at 20 MHz. The board also provides a 64KB cache subsystem, which increases performance significantly.

The FE6500-SK contains a fully-integrated VGA controller, a floppy disk controller, an RS232C serial port, and a fully bi-directional parallel port. It is also equipped with a keyboard port, an auxiliary port, a reset port, a speaker port, seven expansion slots and a cache connector.

System memory is implemented with Single In-Line Memory Modules (SIMMs). Sixteen SIMM sockets allow OEM designers to increase on-board system memory from 1MB (using 256KB x 1 SIMMs) to a maximum of 16 MB bytes (using 1 MB x 1 SIMMs). System memory resides on the CPU local bus; this improves program run times, as local bus cycles execute faster than Channel bus cycles. Page Mode is employed to reduce processor wait states. This allows the use of slower DRAMs, lowering the overall cost.

Manufactured using through-hole technology, and combined with highly-integrated CMOS devices, the FE6500-SK demonstrates that the FE6500 Chip Set forms an effective basis for a high-performance, functionally-rich system board, which is reliable and draws little power.



WESTERN DIGITAL

80386 MCA-Compatible System Design Kit

Technical Description

CPU

The main processor on the board is an Intel* 80386 microprocessor that operates at 16 or 20 MHz. A socket is provided for an optional Intel 80387 or Weitek 3167 coprocessor.

CORE LOGIC

The Western Digital FE6500 Core Logic Chip Set supports the 80386 and provides peripheral, DMA, Channel, cache, and DRAM control logic and address and data buffers.

RAM MEMORY

The FE6500-SK System Design Kit comes standard with 1 MB of DRAM, implemented with four 256 KB x 9 SIMM modules. The board contains a total of sixteen SIMM sockets which can accept 256 KB x 9 or 1 MB x 9 SIMM modules. On-board system memory can be expanded to a maximum of 16 megabytes.

CACHE SUBSYSTEM

A connector is provided to add a cache subsystem. This consists of 64 K bytes of direct-mapped data cache, which increases sytem performance up to 45%.

BIOS

The Western Digital/Phoenix BIOS supports OS/2*, DOS 3.3, 4.0, and all other applicable operating systems and software. The BIOS resides in two 27512 EPROMs (128 KB). It is copied to unused RAM space for faster code execution.

VGA CONTROLLER

The VGA Controller is based on the Western Digital/Paradise* PVGA VLSI circuit. For maximum performance, the interface path is sixteen bits wide. The video interface supports PS/2*-compatible analog monitors. 256KB bytes of video memory is provided. Video interface signals are terminated via a 15-pin female mini-D shell connector.

FLOPPY CONTROLLER

The floppy disk controller (based on the WD57C65) is capable of driving a 720 KB or a 1.44 MB 3.5" drive, or a 1.2 MB 5.25" drive. The signals for the floppy disk interface are terminated via a 40-pin Model 80-compatible connector.

CLOCK/CALENDAR

Configuration parameters, time, and date information are held in a CMOS clock/calendar RAM device.

SERIAL PORT

The board contains an RS232C serial port which utilizes 16550-compatible UARTs with FIFO capability. Signals for the serial port are terminated via a 25-pin male D connector.

PARALLEL PORT

The parallel port is capable of operating in two modes. The normal mode supports a bi-directional interface which is compatible with the IBM Model 70/80 printer port; the alternate mode is compatible with the IBM Model 70/80 printer port. Parallel port signals are terminated via a 25-pin female D connector.

KEYBOARD/AUX PORT

The board contains two identical ports, one of which drives a Model 80-compatible keyboard, and the other drives an auxiliary peripheral such as a mouse. Signals for the ports are terminatetd via two 6-pin mini-DIN connectors.

RESET PORT

A port is provided to allow an external reset to be applied to the board.

SPEAKER PORT

The FE6500-SK includes an on-board speaker which is controlled by a timer in the FE6000.

EXPANSION SLOTS

Two 32-bit, and five 16-bit expansion slots are provided. One slot contains the AVE (Auxiliary Video Extension) signals.

Western Digital Corporation
2445 McCabe Way
Irvine, CA 92714
(800) 847-6181 (714) 863-0102
FAX (714) 660-4909 TLX 910-595-1139

WESTERN DIGITAL

WD 0025I 5/89