WD90C24

Windows Accelerated High Resolution

VGA LCD Controller for

Low Power Applications

WESTERN DIGITAL

TABLE OF CONTENTS

Section	Title	Page
1.0	INTRODUCTION	13-1
	1. 1 FEATURES	13-1
	1. 2 GENERAL DESCRIPTION	13-2
2.0	ARCHITECTURE	13-2
	2. 1 INTRODUCTION	13-2
	2. 2 CRT CONTROLLER MODULE	13-4
	2. 3 SEQUENCER	13-4
	2. 4 GRAPHICS CONTROLLER	13-4
	2. 5 ATTRIBUTE CONTROLLER	13-4
	2. 6 FLAT PANEL CONTROLLER AND INTERFACE	13-4
	2. 7 WEIGHT AND MAPPING LOGIC	13-5
	2. 8 DITHERING ENGINE	13-5
	2. 9 HARDWARE WINDOW ACCELERATOR (BITBLT)	13-5
	2. 10 HARDWARE CURSOR CONTROLLER	13-5
	2. 11 RAMDAC	13-6
	2. 12 CLOCK SYNTHESIZER	13-6
	2. 13 POWER DOWN MANAGEMENT	13-6
	2.13.1 System Power-Down Mode	13-6
	2.13.2 Suspend/Resume Mode	13-7
	2.13.3 Display Idle Mode	13-7
3.0	INTERFACES	13-9
	3. 1 INTRODUCTION	13-9
	3. 2 CPU AND BIOS ROM INTERFACE	13-9
	3. 3 DRAM INTERFACE	13-9
	3.3.1 Configurations	13-9
	3.3.2 Features	13-10
	3. 4 CRT DISPLAY INTERFACE	13-10
	3. 5 FLAT PANEL INTERFACE	13-10
4.0	MEMORY MODE CONFIGURATION	13-11
	4. 1 HOST INTERFACE	13-11
5.0	CONFIGURATIONS	13-12
	5. 1 INTRODUCTION	13-12
	5. 2 SINGLE MEMORY INTERFACE CONFIGURATION	13-13

5. 3 1 MB MEMORY CONFIGURATION 13-14
5. 4 SIMULTANEOUS DISPLAY CONFIGURATION 13-15
5. 5 512 KB HIGH-PERFORMANCE CONFIGURATION 13-16
5. 6 256 KB WITH SIMULTANEOUS DISPLAY CONFIGURATION 13-17
6.0 SIGNAL DESCRIPTIONS 13-18
6. 1 INTRODUCTION 13-18
6. 2 SIGNAL MNEMONIC TO PIN LOCATION 13-19
6. 3 DETAILED SIGNAL DESCRIPTIONS 13-22
6.3.1 Host Interface Pin Definitions 13-23
6.3.2 Display Buffer Memory Interface Pins 13-31
6.3.2.1 Bank A Video Memory Bus 13-31
6.3.2.2 Bank B Video Memory Bus 13-33
6.3.3 RAM DAC/CRT Interface Pins 13-35
6.3.4 Clock Generation Interface Pins 13-37
6.3.5 Panel Interface Pins 13-38
6.3.6 Power and Ground Pins 13-44
6. 4 PIN MULTIPLEXING REFERENCE TABLES 13-45
6.4.1 Host Interface Pins 13-46
6.4.2 Display Buffer Memory Interface Pin Multiplexing 13-48
6.4.3 RAM DAC/CRT Interface Pin Multiplexing 13-50
6.4.4 Clock Generation Interface Pin Multiplexing 13-50
6.4.5 Panel Interface Pin Multiplexing 13-51
6.4.6 Power and Ground Pins 13-52
7.0 REGISTER SUMMARY 13-53
7. 1 INTRODUCTION 13-53
7. 2 VGA REGISTERS 13-53
7. 3 SEQUENCER REGISTERS 13-53
7. 4 CRT CONTROLLER REGISTERS 13-54
7. 5 GRAPHICS CONTROLLER REGISTERS 13-54
7. 6 ATTRIBUTE CONTROLLER REGISTERS 13-54
7. 7 VIDEO PALETTE REGISTERS 13-54
7. 8 PARADISE REGISTERS 13-55
7.8.1 General Paradise Registers 13-55
7.8.2 Paradise Extended Registers 13-56
7.8.3 Flat Panel Paradise Registers 13-57
7.8.4 Local Bus Registers 13-58
7. 9 COMPATIBILITY REGISTERS 13-60

8.0 VGA GENERAL REGISTERS 13-61
8. 1 MISCELLANEOUS OUTPUT REGISTER 13-61
8. 2 INPUT STATUS REGISTER 0 13-62
8. 3 INPUT STATUS REGISTER 1 13-62
8. 4 FEATURE CONTROL REGISTER 13-63
9.0 VGA SEQUENCER REGISTERS 13-63
9. 1 SEQUENCER INDEX REGISTER 13-63
9. 2 RESET REGISTER 13-64
9. 3 CLOCKING MODE REGISTER 13-64
9. 4 MAP MASK REGISTER 13-65
9. 5 CHARACTER MAP SELECT REGISTER 13-65
9. 6 MEMORY MODE REGISTER 13-66
10.0 VGA CRT CONTROLLER REGISTERS 13-67
10. 1 CRT ADDRESS REGISTER 13-67
10. 2 HORIZONTAL TOTAL REGISTER 13-67
10. 3 HORIZONTAL DISPLAY ENABLE END REGISTER 13-67
10. 4 START HORIZONTAL RETRACE PULSE REGISTER 13-67
10. 5 END HORIZONTAL RETRACE REGISTER 13-67
10. 6 VERTICAL TOTAL REGISTER 13-68
10. 7 OVERFLOW VERTICAL REGISTER 13-68
10. 8 PRESET ROW SCAN REGISTER 13-69
10. 9 MAXIMUM SCAN LINE REGISTER 13-69
10. 10 CURSOR START REGISTER 13-70
10. 11 CURSOR END REGISTER 13-70
10. 12 START ADDRESS HIGH REGISTER 13-70
10. 13 START ADDRESS LOW REGISTER 13-71
10. 14 CURSOR LOCATION HIGH REGISTER 13-71
10. 15 CURSOR LOCATION LOW REGISTER 13-71
10. 16 VERTICAL RETRACE START REGISTER 13-71
10. 17 VERTICAL RETRACE END REGISTER 13-71
10. 18 VERTICAL DISPLAY ENABLE END REGISTER 13-72
10. 19 OFFSET REGISTER 13-72
10. 20 UNDERLINE LOCATION REGISTER 13-73
10. 21 START VERTICAL BLANK REGISTER 13-73
10. 22 END VERTICAL BLANK REGISTER 13-73
10. 23 CRT MODE CONTROL REGISTER 13-74
10. 24 LINE COMPARE REGISTER 13-75

11.0 GRAPHICS CONTROLLER REGISTERS 13-76
11. 1 GRAPHICS INDEX REGISTER 13-76
11. 2 SET/RESET REGISTER 13-76
11. 3 ENABLE SET/RESET REGISTER 13-76
11. 4 COLOR COMPARE REGISTER 13-76
11. 5 DATA ROTATE REGISTER 13-77
11. 6 READ MAP SELECT REGISTER 13-77
11. 7 GRAPHICS MODE REGISTER 13-78
11. 8 MISCELLANEOUS REGISTER 13-80
11. 9 COLOR DON'T CARE REGISTER 13-80
11. 10 BIT MASK REGISTER 13-80
12.0 ATTRIBUTE CONTROLLER REGISTERS 13-81
12. 1 ATTRIBUTE INDEX REGISTER 13-81
12. 2 PALETTE REGISTERS (00h-0Fh) 13-81
12. 3 ATTRIBUTE MODE CONTROL REGISTER 13-81
12. 4 OVERSCAN COLOR REGISTER 13-82
12. 5 COLOR PLANE ENABLE REGISTER 13-83
12. 6 HORIZONTAL PEL PANNING REGISTER 13-83
12. 7 COLOR SELECT REGISTER 13-84
13.0 REGULAR PARADISE REGISTERS 13-84
13. 1 ADDRESS OFFSET REGISTERS PR0(A) and PR0(B) 13-84
13. 2 PR1 - MEMORY SIZE 13-85
13. 3 PR2 - VIDEO SELECT REGISTER 13-89
13. 4 PR3 - CRT LOCK CONTROL REGISTER 13-90
13. 5 PR4 - VIDEO CONTROL REGISTER 13-91
13. 6 PR5 - GENERAL PURPOSE STATUS BITS/ UNLOCK PR0 THROUGH PR4 13-92
13. 7 PR10 UNLOCK PR11 - PR1A 13-93
13. 8 PR11 EGA SWITCHES 13-93
13. 9 PR12 SCRATCH PAD 13-94
13. 10 PR13 INTERLACE H/2 START 13-94
13. 11 PR14 INTERLACE H/2 END 13-94
13. 12 PR15 MISCELLANEOUS CONTROL 1 13-95
13. 13 PR16 MISCELLANEOUS CONTROL 2 13-97
13. 14 PR17 MISCELLANEOUS CONTROL 3 13-98
13. 15 PR18A CRTC VERTICAL TIMING OVERFLOW 13-98
13. 16 PR20 UNLOCK SEQUENCER EXTENDED REGISTERS 13-99
13. 17 PR21 DISPLAY CONFIGURATION AND SCRATCH PAD 13-99
13. 18 PR22 SCRATCH PAD REGISTER 13-99

13. 19 PR23 SCRATCH PAD REGISTER 13-99
13. 20 PR30(A) WRITE BUFFER AND FIFO CONTROL REGISTER 13-99
13. 21 PR31 SYSTEM INTERFACE CONTROL 13-100
13. 22 PR32 MISCELLANEOUS CONTROL 4 13-101
13. 23 PR33(A) DRAM TIMING AND ZERO WAIT STATE CONTROL REGISTER 13-102
13. 24 PR34(A) VIDEO MEMORY MAPPING REGISTER 13-103
13. 25 PR35(A) USR0, USR1 OUTPUT SELECT REGISTER 13-103
13. 26 PR45 VIDEO SIGNATURE ANALYZER CONTROL REGISTER 13-104
13.26.1 PR45A Signature Analyzer Data I 13-104
13.26.2 PR45B Signature Analyzer Data II 13-104
13. 27 PR57 FEATURE REGISTER I 13-104
13. 28 PR58 FEATURE REGISTER II 13-106
13. 29 PR58(A) MEMORY MAP TO I/O REGISTER FOR BLT ACCESS IN PI/LOCAL BUS 13-106
13. 30 PR59 - MEMORY ARBITRATION CYCLE SETUP REGISTER 13-107
13. 31 PR60 FRAME BUFFER CONTROLLER I TEST REGISTER 13-107
13. 32 PR61 FRAME BUFFER CONTROLLER II TEST REGISTER 13-108
13. 33 PR62 - FR TIMING REGISTER 13-108
13. 34 PR63 READ/WRITE FIFO CONTROL REGISTER 13-109
13. 35 PR64 RESERVED FOR FUTURE NEED 13-109
13. 36 PR65 RESERVED FOR FUTURE NEED 13-109
13. 37 PR66 RAMDAC/PCLK REGISTER 13-109
13. 38 PR68 PROGAMMABLE CLOCK SELECTION REGISTER 13-109
13. 39 PR69 PROGAMMABLE VCLK FREQUENCY REGISTER 13-110
13. 40 PR70 MIXED VOLTAGE OVERRIDE REGISTER 13-110
13. 41 PR71 PROGRAMMABLE REFRESH TIMING REGISTER 13-110
13. 42 PR72 PROGRAMMABLE CLOCK UNLOCK 13-110
13. 43 PR73 VGA STATUS DETECT 13-111
14.0 FLAT PANEL PARADISE REGISTERS 13-111
14. 1 PR18 FLAT PANEL STATUS REGISTER 13-111
14. 2 PR19 FLAT PANEL CONTROL I REGISTER 13-113
14. 3 PR1A FLAT PANEL CONTROL II REGISTER 13-114
14. 4 PR1B FLAT PANEL UNLOCK REGISTER 13-115
14. 5 PR30 MAPPING RAM UNLOCK REGISTER 13-115
14. 6 PR33 MAPPING RAM ADDRESS COUNTER REGISTER 13-115
14. 7 PR34 MAPPING RAM DATA REGISTER 13-115
14. 8 PR35 MAPPING RAM AND POWER-DOWN CONTROL REGISTER 13-115
14. 9 PR36 PANEL HEIGHT SELECT REGISTER 13-118

13

14. 10 PR37 FLAT PANEL BLINKING CONTROL 13-118
14. 11 PR39 COLOR LCD CONTROL REGISTER 13-120
14. 12 PR41 VERTICAL EXPANSION INITIAL VALUE REGISTER 13-120
14. 13 PR44 POWER-DOWN MEMORY REFRESH CONTROL REGISTER.... 13-121
15.0 COMPATIBILITY REGISTERS 13-121
15. 1 HERCULES/MDA MODE CONTROL REGISTER, MDA OPERATION... 13-121
15. 2 HERCULES REGISTERS 13-122
15. 3 ENABLE MODE REGISTER 3B8h 13-122
15. 4 HERCULES COMPATIBILITY REGISTER 13-122
15. 5 COLOR CGA OPERATION REGISTER 13-123
15. 6 CGA COLOR SELECT REGISTER 13-123
15. 7 CRT STATUS REGISTER MDA OPERATION 13-124
15. 8 CRT STATUS REGISTER CGA OPERATION 13-124
15. 9 AT&T/M24 REGISTER 13-125
16.0 EXTENDED REGISTER ACCESS FOR HARDWARE CURSOR, BITBLT, AND LINE DRAWING 13-126
16. 1 ACCESSING INDEXED REGISTERS 13-126
16. 2 INDEX CONTROL REGISTER - PORT 23C0h/23C1h 13-126
16. 3 INTERRUPT STATUS REGISTER, SYSTEM CONTROL REGISTERS BLOCK - INDEX 0 13-127
16.3.1 Global Interrupt Map 13-127
17.0 HARDWARE CURSOR 13-128
17. 1 CURSOR CONTROL REGISTER, INDEX 0 13-128
17. 2 CURSOR PATTERN ADDRESS 13-129
17.2.1 Cursor Pattern Address Low, Index 1 13-129
17.2.2 Cursor Pattern Address High, Index 2 13-129
17. 3 CURSOR ORIGIN, INDEX 5 13-129
17. 4 CURSOR DISPLAY POSITION 13-129
17.4.1 Cursor Display Position X, Index 6 13-129
17.4.2 Cursor Display Position Y, Index 7 13-130
17. 5 CURSOR COLOR REGISTERS 13-130
17.5.1 Cursor Primary Color, Index 3 13-130
17.5.2 Cursor Secondary Color, Index 4 13-130
17.5.3 Cursor Auxiliary Color, Index 8 13-130
18.0 HARDWARE BITBLT 13-131
18. 1 CONTROL AND STATUS 13-131
18.1.1 BITBLT Control - Part 1, Index 0 13-131
18.1.2 BITBLT Control - Part 2, Index 1 13-132

18. 2 SOURCE AND DESTINATION 13-133
18.2.1 BITBLT Source Low, Index 2 13-134
18.2.2 BITBLT Source High, Index 3 13-134
18.2.3 BITBLT Destination Low, Index 4 13-134
18.2.4 BITBLT Destination High, Index 5 13-134
18. 3 ADDRESS MAPPING 13-134
18.3.1 Monochrome and Planar Modes 13-134
18.3.2 Packed Modes 13-134
18. 4 DIMENSIONS AND ROW PITCH 13-135
18.4.1 BITBLT Dimension X, Index 6 13-135
18.4.2 BITBLT Dimension Y, Index 7 13-135
18.4.3 BITBLT Row Pitch, Index 8 13-135
18. 5 FOREGROUND AND BACKGROUND COLORS 13-136
18.5.1 BITBLT Foreground Color, Index A 13-136
18.5.2 BITBLT Background Color, Index B 13-136
18. 6 MAP AND PLANE MASK 13-136
18.6.1 BITBLT Mask - VGA, Index E 13-136
18. 7 RASTER OPERATIONS 13-137
18.7.1 BITBLT Raster Operation, Index 9 13-137
18. 8 PATTERNS 13-137
18.8.1 BITBLT Pattern Storage - Monochrome and Planar Modes .. 13-138
18.8.2 BITBLT Pattern Storage - Packed Modes 13-138
18. 9 MONOCHROME TO COLOR EXPANSION 13-138
18. 10 EXTRACTING MONOCHROME DATA 13-139
18. 11 COLOR TRANSPARENCY 13-139
18.11.1 BITBLT Transparency Color, Index C 13-139
18.11.2 BITBLT Transparency Mask, Index D 13-139
18. 12 FILLED RECTANGLES 13-140
18. 13 SYSTEM MEMORY TO DISPLAY MEMORY OPERATION 13-140
18. 14 DISPLAY MEMORY TO SYSTEM MEMORY OPERATIONS 13-140
18. 15 SYSTEM MEMORY TO DISPLAY MEMORY TRANSFERS WITH COLOR EXPANSION 13-141
19.0 HARDWARE LINE DRAWING 13-141
19. 1 STRIP LINE DRAWING 13-141
19.1.1 Conditions 13-141
19.1.2 Altered BLT Register Functions 13-141
19.1.3 Line Draw Operation 13-141

13

20.0 APPLICATIONS AND PROGRAMMING 13-142
20. 1 USING THE HARDWARE CURSOR IN 16-BIT PER COLOR MODE 13-142
20. 2 BITBLT OPERATIONS IN VGA MODES 4, 5, AND 6 13-143
20. 3 BITBLT OPERATIONS IN TEXT MODE 13-143
20. 4 USING BITBLT IN 16-BIT PER COLOR MODE 13-143
20. 5 PATTERNS 13-144
20.5.1 Using BITBLT For Arbitrary Sized Patterns 13-145
20.5.2 Patterns Built On-Screen 13-145
20.5.3 Use Of Patterns In Text Mode 13-145
20. 6 SUPPORT FOR KANJI CHARACTERS 13-146
20. 7 READING AND WRITING THE VGA READBACK LATCHES 13-147
20. 8 TRANSFERRING MONOCHROME SOURCES TO COLOR 13-147
20. 9 EXTRACTING MONOCHROME DATA 13-147
20. 10 COLOR TRANSPARENCY 13-148
20. 11 DRAWING FILLED RECTANGLES 13-148
20. 12 SYSTEM MEMORY TO VIDEO MEMORY OPERATIONS 13-148
20. 13 VIDEO MEMORY TO SYSTEM MEMORY OPERATIONS 13-148
20. 14 SYSTEM MEMORY TO DISPLAY MEMORY TRANSFERS WITH COLOR EXPANSION 13-149
20. 15 CONTROL AND STATUS 13-149
20. 16 AUTOMATIC DESTINATION UPDATE 13-152
20. 17 QUICK START MODE 13-152
20. 18 ABORTED BITBLT 13-153
20. 19 REGISTER ACCESS 13-153
21.0 EMBEDDED CLOCK GENERATOR 13-153
21. 1 FEATURES 13-153
21. 2 DESCRIPTION 13-154
21.2.1 System Bus Interface 13-154
21.2.2 Firmware Interface 13-154
21.2.3 Analog Interface 13-155
21.2.4 External Clock Mode 13-155
21.2.5 ISO Support 13-155
22.0 WD90C24 CONFIGURATION REGISTERS 13-156
23.0 I/O MAPPING 13-159
23. 1 DESCRIPTION 13-159
24.0 OPERATING SPECIFICATIONS 13-162
25.0 DC/AC CHARACTERISTICS 13-163
25. 1 DC POWER DISTRIBUTION 13-163
25. 2 INTERNAL CLOCK DC CHARACTERISTICS 13-167
25. 3 INTERNAL CLOCK AC CHARACTERISTICS 13-168

LIST OF TABLES

Table	Title	Page
4-1	MEMORY MODE CONFIGURATION	13-11
4-2	HOST INTERFACE	13-11
5-1	CONFIGURATIONS AND MODES SUPPORTED	13-12
6-1	SIGNAL TO PIN LOCATION	13-19
6-2	HOST INTERFACE PIN SIGNAL DEFINITIONS	13-23
6-3	BANK A VIDEO MEMORY SIGNALS	13-31
6-4	BANK B VIDEO MEMORY SIGNALS	13-33
6-5	INTERNAL DAC INTERFACE PINS	13-35
6-6	CLOCK GENERATION INTERFACE PIN TABLE	13-37
6-7	PANEL INTERFACE PINS	13-38
6-8	POWER AND GROUND SIGNAL DEFINITIONS	13-44
6-9	HOST INTERFACE PIN MULTIPLEXING	13-46
6-10	DISPLAY MEMORY INTERFACE PIN MULTIPLEXING	13-48
6-11	RAMDAC PIN MULTIPLEXING	13-50
6-12	CLOCK SYNTHESIZER INTERFACE PIN MULTIPLEXING	13-50
6-13	PANEL INTERFACE PIN MULTIPLEXING	13-51
6-14	POWER AND GROUND PIN MULTIPLEXING	13-52
7-1	VGA REGISTERS SUMMARY	13-53
7-2	SEQUENCER REGISTERS SUMMARY	13-53
7-3	CRT CONTROLLER REGISTERS SUMMARY	13-54
7-4	GRAPHICS CONTROLLER REGISTERS SUMMARY	13-54
7-5	ATTRIBUTE CONTROLLER REGISTERS SUMMARY	13-54
7-6	VIDEO PALETTE REGISTERS SUMMARY	13-54
7-7	GENERAL PARADISE REGISTERS	13-55
7-8	PARADISE EXTENDED REGISTERS SUMMARY	13-56
7-9	FLAT PANEL PARADISE REGISTERS SUMMARY	13-57
7-10	LOCAL BUS REGISTERS	13-58
7-11	COMPATIBILITY REGISTERS SUMMARY	13-60
13-1	IBM COMPATIBLE MEMORY ORGANIZATION - 256K TOTAL	13-86
13-2	64K/PLANE WD90C24 MEMORY ORGANIZATION - 256K TOTAL	13-86
13-3	128K PLANE WD9030 MEMORY ORGANIZATION - 1M TOTAL	13-87
13-4	256K PLANE MEMORY ORGANIZATION -1M TOTAL	13-87
14-1	DISPLAY TYPE AND OPERATION SELECTION SUMMARY	13-112
17-1	CURSOR REGISTERS	13-128
18-1	BITBLT REGISTERS INDEX	13-131
18-2	RESULTS OF COMBINED SOURCE AND DESTINATION VALUES	13-137
18-3	RASTER OPERATION CODE FUNCTIONS	13-137

LIST OF TABLES (Continued)

Table	Title	PaGE
19-1	BLT FUNCTIONS ALTERED BY LINE DRAW	13-141
21-1	VCLK SELECTION	13-154
21-2	MCLK SELECTION	13-154
22-1	WD90C24 CONFIGURATION REGISTERS	13-156
22-2	WD90C24 CONFIGURATION REGISTER BITS, CNF[31:0]	13-157
23-1	I/O MAPPING GROUPS	13-159
25-1	WD90C24 POWER DISTRIBUTION	13-163
25-2	DC POWER DISTRIBUTION	13-164
25-3	DC TIMING CHARACTERISTICS	13-167
25-4	AC TIMING CHARACTERISTICS	13-168

LIST OF FIGURES

Figure	Title	Page
2-1	ARCHITECTURE	13-3
2-2	BLOCK DIAGRAM	13-8
5-1	SINGLE MEMORY INTERFACE CONFIGURATION	13-13
5-2	1 MB MEMORY CONFIGURATION	13-14
5-3	SIMULTANEOUS DISPLAY CONFIGURATIO	13-15
5-4	512 KB HIGH-PERFORMANCE CONFIGURATION	13-16
5-5	256 KB WITH SIMULTANEOUS DISPLAY CONFIGURATION	13-17
6-1	PIN CONFIGURATION	13-21
14-1	SYSTEM POWER DOWN MODE/DISPLAY IDLE MODE	13-117
21-1	CLOCK GENERATOR CONNECTIONS	13-155
23-1	ENABLING I/O MAPPING ON THE WD90C24	13-159
23-2	I/O MAPPING GROUP DIAGRAM	13-161

1.0 INTRODUCTION

1.1 FEATURES

- new frame buffer architecture that supports:
  - simultaneous display and BITBLT without changing the performance.
  - simultaneous display for all standard modes
- 16-bit true color resolution for both CRT and color flat panel display
- hardware window accelerator support (BITBLT)
- hardware line drawing (for both Bresenham and draw assist strip paint of Microsoft™ Window compatible)
- 256K color support for STN and TFT color LCDs
- single chip for 8 or 16 - bit AT, MicroChannel, PI - bus, and 32-bit local bus interface
- supports 16 or 32 bit memory interface
- 64K simultaneous color support for CRT, color DSTN LCD, and color TFT LCD
- direct interface to CRT with built-in RAMDAC
- direct interface to dual panel mono LCD, single panel color DSTN or TFT color LCD and plasma display
- 64 gray shades for monochrome STN LCD display
- 256 colors simultaneous display on one frame out of 256K possible choices of colors for CRTs, color DSTN LCD, and color TFT LCD display in none-true color mode
- on-chip programmable clock frequency synthesizer
- up to 80 Mhz video clock for the CRT display and up to 50 Mhz video clock for the flat panel display
- up to 50 Mhz memory clock
- 256K to 1 Mbytes of memory configuration with 64K x 16 or 256K x 16 memory
- with 256K DRAM, supports all IBM VGA modes for CRT and LCD display
- with more DRAM installed, supports up to 1024 x 768 x 256 colors for CRT display and up to 640 x 480 x 256 colors for LCD display
- 8- or 16- bit host data bus interface for CPU I/O and memory cycles.
- high performance graphic controller that supports high resolution graphics with up to 1024 x 768 x 256 color in CRT mode and 640 x 480 x 256 in flat panel mode
- operates with 5 volt and 3.3 volt power supplies
- 16-bit true color for CRT or flat panel display at up to 640 x 480 resolution to support 64K color simultaneous display on one frame for CRT, color DSTN LCD, and color TFT LCD displays
- true fast page display memory fetching for both graphic and text modes
- programmable virtual memory addressing for CPU memory address space
- four levels of write cache for zero wait state CPU memory write performance
- emulates planer mode addressing for packed pixel mode operation to achieve faster block transfers
- intelligent power management control:
  - 3.3V Normal Mode 0.3 W Max
    Display Idle 6.6 MW Max
    PWRDN Mode 1.65 MW Max
  - 5.0V Normal Mode 0.5 W Max
    Display Idle 30 MW Max
    PWRDN Mode 2.5 MW Max
- signature analyzer to help the IC and board level test for video data output from the chip
- I/O mapping allows the IC to enter a test mode, to help for quick open and short checks in board level test
- 208-pin EIAJ package
- 64 gray shades for monochrome flat panel displays
- on-chip PS/2-compatible RAMDAC with integral monitor detection logic
- on-chip WD90C63-compatible clock synthesizer with user programmable frequency for both video dot clock (VCLK) and video memory clock (MCLK)
- hardware support for the graphic cursor, which has 64 x 64 or 32 x 32 pattern sizes for CRT displays and a 32 x 32 pattern size for flat panel displays
- intelligent power management control to reduce the power requirement for the display subsystem
- drives directly without external components for all 640 x 480 (400) monochrome and color flat panel displays, such as STN, DSTN, TFT, and plasma displays

13

1.2 GENERAL DESCRIPTION

The Western Digital WD90C24 is a 0.9 micron CMOS VLSI device that drives standard CRTs and flat panel displays. The WD90C24 allows simultaneous display for a CRT and a dual monochrome panel, or a CRT and signal color panel. It is backwards compatible with previous video standards such as MDA, EGA, CGA, Hercules, and AT&T 6300.

2.0 ARCHITECTURE

2.1 INTRODUCTION

The WD90C24 is made up of the following major internal modules:

- CRT Controller
- Sequencer
- Graphics Controller
- Attribute Controller
- Flat Panel Controller and Interface
- VLBI, or Local Bus Interface
- PI Bus Interface
- Hardware Cursor Controller
- Dithering Engine
- Weighting and Mapping Logic
- RAMDAC, Clock Synthesizer
- Power Down Management
- BITBLT, or Window Accelerator Controller
- Line Drawing Engin
- Frame Buffer Controller for Simultaneous display on CRT and LCD Panel

Each module described in detail in this section. Their relationships to each other are shown in Figure 2-1.

A 4-level deep write cache is used internally to achieve fast memory write. The zero wait state may be achieved for most memory write operations with a 32-bit video memory interface.

Utilize Fast Page mode memory fetching to improve memory bandwidth. A FIFO is also used internally to achieve the video display bandwidth necessary to interleave CPU accesses and display refresh cycle.

Weighting and Mapping Logic is used for color to gray scale mapping. A dithering engine works as a digital DAC to generate the gray scale level for monochrome flat panel displays, and generates colors for color flat panel display.

The internal Row Buffer supports the split screen panel display while driving the flat panel only. An external Frame Buffer, which resides in the off-screen memory of the display memory, supports split screen display while driving the CRT and flat panel at same time.

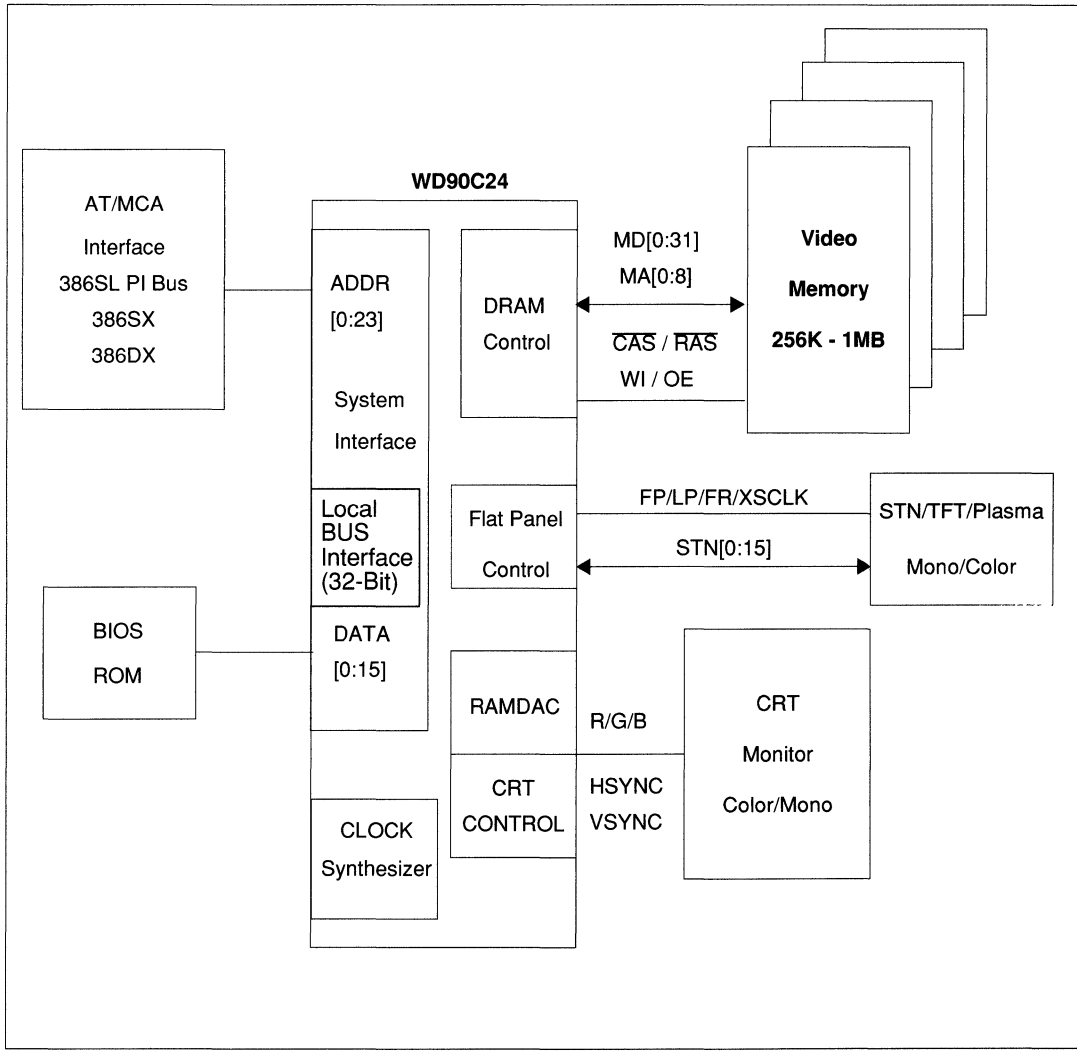


FIGURE 2-1 ARCHITECTURE

13

2.2 CRT CONTROLLER MODULE

This module is used to perform the functions described below:

- generates horizontal sync (HSYNC) and vertical sync (VSYNC) for the CRT display monitor
- simultaneous CRT and dual flat panel display is performed using frame buffer architecture
- hidden display timing registers meet the fixed display timing for the flat panel display
- CRT display screen refresh is maintained for the various display modes defined by the BIOS ROM resident firmware
- performs video split screen refresh and screen size mapping

2.3 SEQUENCER

The Sequencer Module provides the following functions:

- functions as a timing generator for the video memory cycles
- provides the character clock in the alphanumeric mode, and the dot clock in the graphics mode
- arbitrates between the video display refresh, memory refresh, and CRT access of the video memory for CRT only, flat panel only, or simultaneously CRT and single panel display
- arbitrates between the video display refresh, frame buffer access, memory refresh, and CRT access of the video memory for simultaneous CRT and dual panel display
- arbitrates cursor pattern access to the off-screen display memory when the hardware cursor is activated
- provides the write cache control for CPU memory write to the video display memory

2.4 GRAPHICS CONTROLLER

The Graphics Controller manipulates the data flow between the CPU and the video memory for CPU write and read cycles.

2.5 ATTRIBUTE CONTROLLER

The Attribute Controller allows the following functions:

- serializes the video memory data into a video data stream according to different display formats
- controls the following features in all display modes:
  - blinking
  - underlining
  - text cursor
  - pixel panning
  - reverse video
  - background and foreground color

2.6 FLAT PANEL CONTROLLER AND INTERFACE

The Flat Panel Controller and Interface performs the following functions:

- controls the video data flow after video data exits the RAMDAC's palette RAM, until the video data output to the flat panel interface
- generates the flat panel control signals:
  - Frame Rate (FR)
  - Frame Pulse (FP)
  - Latch Pulse (LP)
  - Shift Clock (XSCLK)
  - Data Enable (ENABLE)

  These signals are generated in different timing and polarity in order to drive different types of panels without external components
- split screen refresh for dual panel display and screen size mapping for both signal and dual panel displays
- controls the video data flow in and out of the frame buffer
- performs split screen refresh and screen size mapping using frame buffer architecture (screen mapping includes vertical expansion and auto-centering)
- controls the video data flow into and out of the row buffer (using row buffer architecture)
- generates different video data formats to drive different types of flat panels without external components

2.7 WEIGHT AND MAPPING LOGIC

For monochrome panel displays, this logic converts color information from the palette RAM into gray scale information using the following equation:

$$I = .3R + .59G + .11B.$$

Select from the following modes for monochrome display panels:

- Frame-Rate Modulation
  to select the shade code from the Mapping RAM, which is loaded with user-selected codes of shades with the optimum intensity
- 64-Shade Display Mode
  to select the shade from the Dithering Engine
- Pulse-Width Modulation
  to truncated or round off the information and send it to the panel directly

For color panel displays, the red, green, and blue color information that comes from the palette RAM is the code of the shade for each color.

Select from the following modes for color panel displays:

- Frame Rate Modulation
  to select the shade code is from the Dithering Engine
- Pulse-Width Modulation
  to truncate the R, G, B color information and send it to the panel directly

2.8 DITHERING ENGINE

The Dithering Engine uses a dithering pattern and frame rate modulation to constantly generate 64 gray shades. The dithering pattern for each shade is chosen so that it creates minimum flicker on the panel screen.

2.9 HARDWARE WINDOW ACCELERATOR (BITBLT)

The WD90C24 was designed with hardware support for Microsoft Windows, resulting in accelerated Windows performance.

WD90C24 BITBLT increases speed. With BITBLT, blocks of pixels are transferred directly between regions of display memory and between display memory and system memory through an I/O port.

2.10 HARDWARE CURSOR CONTROLLER

The Hardware Cursor Controller provides up to a 64 x 64 pattern. Each pixel in the pattern is represented by two bits. These two bits determine how the cursor is displayed based on the color mode selected. The pattern is stored the off-screen display memory. The hardware cursor is controlled by the following registers:

- Cursor Control
- Cursor Pattern Address
- Cursor Primary Color
- Cursor Secondary Color
- Cursor Auxiliary Color
- Cursor Origin
- Cursor Display Address X
- Cursor Display Address Y

The Cursor Display Address is the location for the origin of the cursor on the display screen. The Cursor Pattern Address is the starting memory location where the cursor pattern is stored in the display memory.

The Cursor Origin and the Cursor Display Address are used to calculate the cursor's starting display address. The cursor pattern is displayed on the window and the controller clips off the pattern. The pattern fetching request is sent to the sequencer. The cursor pattern is displayed when the display location matches the cursor start location.

2.11 RAMDAC

The on-chip RAMDAC is low-power, PS/2-compatible with power-down control and built-in monitor detection logic with the following features:

- 3 256 x 6 RAMs as R, G, B
- color look-up table
- 3 6-bit DACs
- mask register
- supports 16-bit true color

The 16 bits of video data are formed by:

- 5 bits red
- 6 bits green
- 5 bits blue

  or
- 5 bits of each color with one bit ignored

When in true color mode, video data bypasses the color palette RAM but maintains a four pipe delay for the DAC output.

The LSB bit of the three DACs are forced to zero for 5-bit color configuration. The LSB bits of the Red DAC and Blue DAC are forced to zero for the 5-bit red, 6-bit green, and 5-bit blue configuration.

The DAC generates RS-343A/RS-170 compatible output and has +1/2 LSB of integral and differential linearity errors.

2.12 CLOCK SYNTHESIZER

The on-chip Clock Synthesizer is a dual clock generator for VGA applications. It simultaneously generates video memory clock (MCLK) and video dot clock (VCLK).

Both clock frequencies can be programed by the user and are derived from the 14.318Mhz system clock available in the IBM PC/XT/AT and PS/2 computer systems.

The clock synthesizer has power-down control to achieve a lower power requirement.

When programing a new clock frequency for both MCLK and VCLK, the Clock Synthesizer requires 50 ms to achieve a stable frequency. All the registers, palette RAM, and Mapping RAM must be reloaded after the clock frequency is stable.

2.13 POWER DOWN MANAGEMENT

The WD90C24 provides two major power down modes:

- System Power-Down Mode
- Display Idle Mode

Each mode is described below.

2.13.1 System Power-Down Mode

System power down mode is partitioned into three separate modes:

- Sleep Mode
- Suspend/Resume Mode
- Display Idle Mode

Sleep Mode

Sleep Mode is designed for when the system is not used for a long period of time and power savings is desired. Power consumption in this mode is less than 50uA. The disadvantage to Sleep Mode is that all registers and the RAM contents are lost after shutting down the V_{CC}, therefore a software routine is required to restore the registers and RAM value.

In Sleep Mode, all the V_{CC} pins are turned off except the $\overline{PDOWN}$ V_{CC}, which provides power for the logic generating memory refresh signals.

Entering Sleep Mode:

- Execute a power-down software routine that stores all data in the registers and RAM to the system main memory.
- The $\overline{PDOWN}$ signal is driven low by the power down control manager.
- After 300 ms, the power down control manager drives the RESET signal high.
- After another 300 ms, the power down control manager shuts off all the VCC pins except $\overline{PDOWN}$ V_{CC} pin.
- During this time, WD90C24 is in the Sleep Mode. The logic powered by the $\overline{PDOWN}$ V_{CC} receives the user-defined slow toggling signal from REFCKIN to generate CAS before RAS memory refresh cycles. The REFCKIN signal is the PCLK output in the normal active display

Leaving Sleep Mode:

- The power down control manager turns on the V_{CC} for Clock synthesizer, then all other V_{CC}'s.
- After 300 ms, the 14.318 Mhz system clock that drives the CKIN must be stable. The power down control manager drives the RESET signal low. The falling edge RESET wakes up the Clock Synthesizer.
- After another 100ns, the Clock Synthesizer generates stable default MCLK and VCLK signals. The power-down control manager then activates the software routine to restore all registers and RAM data.
- After another 300 ms, the power-down control manager drives the $\overline{\text{PDOWN}}$ high.
- After another 300 ms, the WD90C24 should be in the normal active display mode.

2.13.2 Suspend/Resume Mode

This mode is designed for when the system is not used for a reasonably long time. All V_{CC}s are kept alive and the Clock Synthesizer is shut down. All registers and the RAM contents are maintained, therefore, minimum software control is required. In this mode, the following rules apply:

- The CPU can write to some registers but *not* to the RAM.
- The CPU can not read from WD90C24 and all outputs are tri-stated.
- All inputs are required to be in a known state and stable.

The only logic still toggling in this mode is the memory refresh generation logic. Power consumption is less than 1mA.

Entering Suspend/Resume Mode:

- The power down manager drives the $\overline{\text{PDOWN}}$ signal low to start entering the Suspend/ Resume Mode.
- After 10ms, the power-down control manager activates a software routine to write a "one" to the PR52 bit 7 to shut down the Clock synthesizer. This bit is power-up reset to zero.
- The WD90C24 then enters the Suspend/ Resume Mode. The memory refresh generation logic takes the slow toggling signal from REFCKIN pin and generate the CAS before RAS memory refresh cycles.

Leaving Suspend/Resume Mode:

- The power-down manager ensures that the 14.318 Mhz clock is stable, then activates a software routine to write the PR52 bit 7 to zero. This wakes up the Clock Synthesizer.
- After 100ms, the Clock Synthesizer generates stable VCLK and MCLK. The power-down manager then drives $\overline{\text{PDOWN}}$ high to leave the Suspend/Resume mode. The rising edge of $\overline{\text{PDOWN}}$ causes the MCLK and VCLK to start driving the WD90C24.
- After 300 ms, the WD90C24 is in normal active display mode.

2.13.3 Display Idle Mode

Display Idle Mode is designed for when the system is not used for a short period of time. In this mode all the V_{CC}s and the Clock Synthesizer remain on. The MCLK and VCLK are slowed down by a user programmable frequency. In this mode:

- the CPU can access all the registers, RAM and display memory
- the DAC and the LCD logic is shut down

The memory refresh cycle is generated by the same logic for normal display mode but with slower MCLK and VCLK. By programming the memory refresh period and memory refresh cycles per horizontal line the user-defined memory refresh cycle can be achieved. In this mode, these two registers override the horizontal total register and memory refresh cycles per horizontal line register.

Entering Display Idle Mode:

- The power down manager drives the $\overline{\text{PDOWN}}$ signal low to enter Display Idle Mode. The falling edge of $\overline{\text{PDOWN}}$ causes the MCLK and VCLK switch to program slower frequency. The WD90C24 enters the Display Idle Mode immediately.

Leaving Display Idle Mode:

The power-down manager drives the $\overline{\text{PDOWN}}$ signal high. The rising edge of $\overline{\text{PDOWN}}$ causes MCLK and VCLK to switch to the normal frequency. The WD90C24 is back to the normal display mode.

13

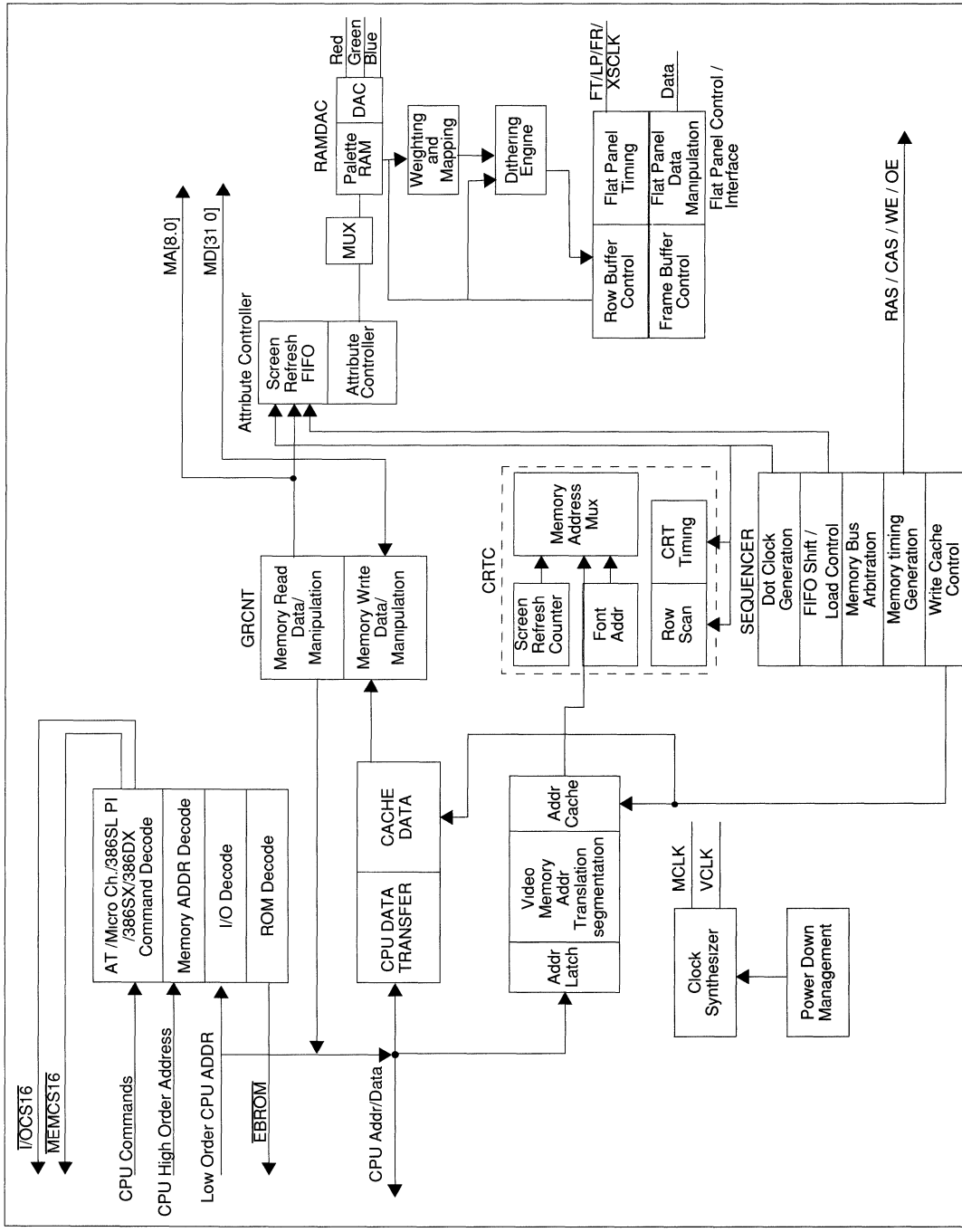


FIGURE 2-2 BLOCK DIAGRAM

3.0 INTERFACES

3.1 INTRODUCTION

The WD90C24's five major interfaces are described in this section.

- CPU and BIOS ROM Interface
- DRAM Display Memory Interface
- CRT Display Interface
- Flat Panel Display Interface

3.2 CPU AND BIOS ROM INTERFACE

The WD90C24's VGA subsystem CPU and BIOS ROM interface operate in the following bus configurations:

- PC/XT/AT bus for CPU and BIOS ROM I/F
- IBM MicroChannel bus
- Direct interface with INTEL 386SL PI bus
- 386SX local bus
- 386 DX local bus

The selection of the mode depends on the setting of configuration register bits CNF(14), CNF(13), and CNF(2). These settings are determined upon power-up reset, and is described in the section called "Configurations".

The $\overline{\text{IOCS16}}$ and $\overline{\text{MEMCS16}}$ signals are generated to indicate 16-bit operation.

Interface features are as follows:

- minimal use of external circuitry
- provides all signals, decodes all memory and I/O addresses to interface with any of the bus configurations in 8- or 16-bit mode.
- decoding for video BIOS ROM while in extension card application (8-bit operation only)
- reduced CPU wait states while writing to video memory with use of a display memory data and address write cache that hold CPU write data until it can be transferred to the display memory
- improved performance of CPU display memory access -- PROA and PROB registers may be addressed indirectly
- improved performance of CPU display memory access -- 32-bit memory data latch is addressable by the I/O port
- emulation of the planer mode operation in pack pixel mode to improve CPU block transfer speed
- 16 segments of 1 Mbyte virtual memory addressing range or 32 segments of 512K-byte virtual memory addressing range for flexibility in memory allocation

3.3 DRAM INTERFACE

For a16-bit memory interface the following DRAM configurations can be used:

- 1 256K x 16 DRAM
- 2 256K x 16 DRAMs
- 3 64K x 16 DRAMs

For a 32-bit memory interface the following DRAM configurations can be used:

- 4 64K x 16 DRAMs
- 2 256K x 16 DRAMs

Refer to Table 5-1 for a summary of configurations.

In all cases, WD90C24 uses DRAM fast page mode for optimum performance.

3.3.1 Configurations

In the minimum configuration, 2 64 x 16 DRAMS, the WD90C24 can support all standard IBM VGA modes.

When additional DRAMs are installed, the WD90C24 is capable of supporting high color resolution video modes, up to 1024 x 768 x 256 colors, non-interlaced.

13

3.3.2 Features

- supports 60ns/70ns/80ns/100ns DRAMs with the dedicated MCLOCK which can operate from 32 MHz to 50 MHz
- fast page DRAM timing is used for all CPU access, graphics display and text display (a choice of page mode and non-page mode operation is provided to access fonts in text modes)
- generates CAS before RAS DRAM refresh for the display memory

3.4 CRT DISPLAY INTERFACE

- on-chip RAMDAC provides the RED, GREEN, and BLUE signals directly to the analog CRT monitor
- provides HSYNC and VSYNC signals to control the monitor
- allows use of an external RAMDAC to drive the CRT
- supports Bt/471/478/476 compatible RAMDAC interface

3.5 FLAT PANEL INTERFACE

- direct interface with 640 x 480(400) STN, DSTN, TFT 1024 x 768 LCD, and plasma panels
- flat panel interface signals change function to support the panel type chosen
- programmable timing and polarity for the flat panel control signals to meet the requirements of different panels
- video data groupings to meet the requirement for different panels
- controller supplies 8 pixel per shift clock with 8 bits of data for monochrome display with STN panel
- controller supplies one pixel per shift clock with 4 bit of data for 16 shade for plasma panel
- controller supplies 3-bit(1 pixel per shift clock) interface, 8-bit(2 and 2/3 pixel per shift clock) interface, and 16-bit(5 and 1/3 pixel per shift clock) interface for color display with STN panel
- controller supplies 3-bit, 6-bit, 9-bit, 18-bit (all are one pixel per shift clock) interface for TFT panel.

4.0 MEMORY MODE CONFIGURATION

The following table defines how to set up each register for the desired memory configuration (refer to Pages 12 through17 for additional information).

MEMORY			CNF (16)	CNF (14)	CNF (13)
MODE	DRAMS TYPE	DRAMS QTY			
1	256Kx16	1	1	0	1
2	256Kx16	2	1	0	0
3	256Kx16 and 64Kx16	1 1	1	1	1
4	64Kx16	4	0	0	1
5	64Kx16	3	0	0	0
NOTE: CNF(16), CNF(14), and CNF(13) are readable via PR 11 register bits 7, 6, and 5, respectively (refer to Section 22).					

TABLE 4-1 MEMORY MODE CONFIGURATION

In memory modes 1 and 5, the display memory data path is always 16 bits wide.

Memory modes 2, 3, and 4 should be used with a 32-bit wide display memory data path, unless one of the DRAM banks is used as the LCD panel frame buffer. For example, one DRAM bank is used as the LCD panel frame buffer when simultaneous display with an LCD panel and CRT is used, and also when 16-bit STN color dual panel is used.

By default, memory modes 2, 3, and 4 use a 32-bit data path, unless one of the following conditions have been set up to use a 16-bit data path. However, only one of the following conditions is required to setup a 16-bit video memory data path.

1. PR30 register bit 5 is set to 1.
2. PR19 register bits 4 and 5 are both set to 1, which is used for simultaneous display.
3. Configure for memory mode 1 (refer to Table 5-1.
4. Configure for memory mode 5 (refer to Table 5-1.

4.1 HOST INTERFACE

The following table lists the conditions required for each type of host interface.

CNF(17)	CNF(2)	HOST MODES
0	0	MicroChannel Bus
0	1	AT Bus
1	0	PI (also AT or ISA)
1	1	Local Bus

TABLE 4-2 HOST INTERFACE

13

5.0 CONFIGURATIONS

5.1 INTRODUCTION

The WD90C24 can be configured in five different ways. The following table summarizes the configurations. Illustrations are also provided:

- Single-Memory Interface Configuration
- 1 Megabyte Memory Configuration
- Simultaneous Display Configuration
- 512 KB High-Performance Configuration
- 256 KB with Simultaneous Display Configuration

MODES	1[2]	2[1]	3[1]	4[1]	5[2]
1024 x 768 x 256		C,L			
1024 x 768 x 16	C,L	S,C,L	C,L	C,L	
800 x 600 x 256	C	C	C	C	
800 x 600 x 16	C	C	C	C	C
640 x 480 x 256	C,L	S,C,L	S,C,L	C,L	
640 x 480 x 16	S,C,L	S,C,L	S,C,L	S,C,L	S,C,L
640 x 400 x 256	C,L	S,C,L	S,C,L	S,C,L	S,C,L
All IBM Standard Modes	S,C,L	S,C,L	S,C,L	S,C,L	S,C,L

NOTES
S = Simultaneous Display
C = CRT Only
L = LCD Only
[1]In C and L modes, has 32-bit interface.
[2]In C and L modes, has 16-bit interface.

TABLE 5-1 CONFIGURATIONS AND MODES SUPPORTED

5.2 SINGLE MEMORY INTERFACE CONFIGURATION

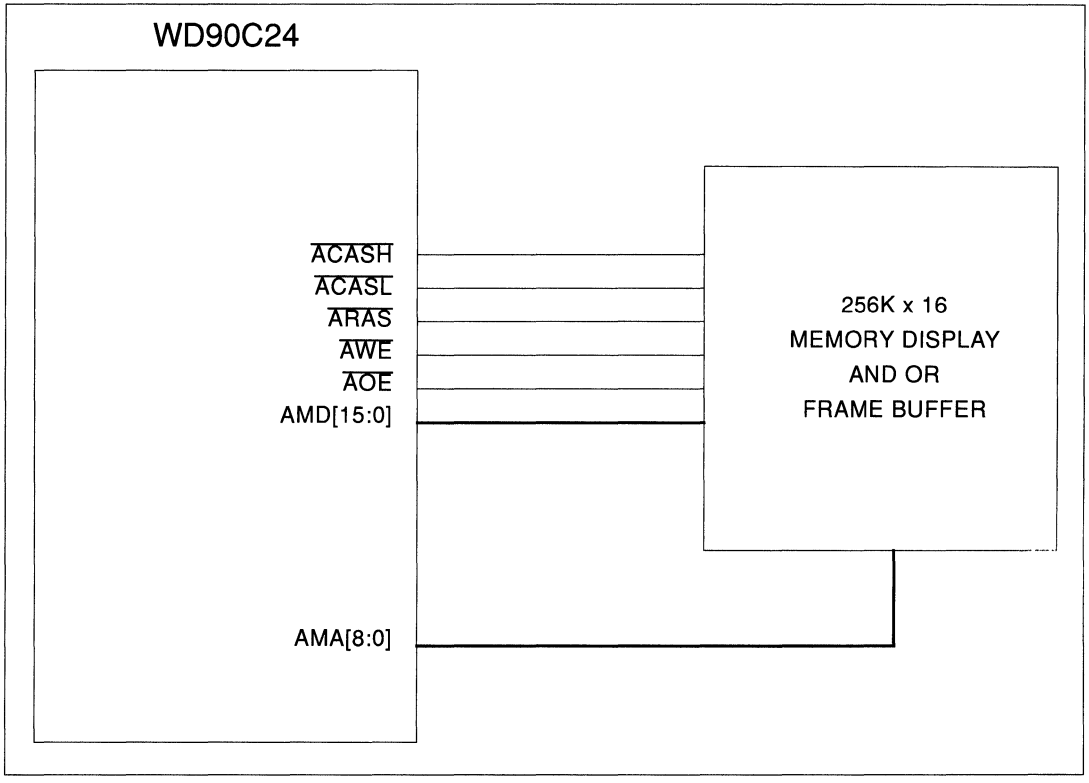


FIGURE 5-1 SINGLE MEMORY INTERFACE CONFIGURATION

5.3 1 MB MEMORY CONFIGURATION

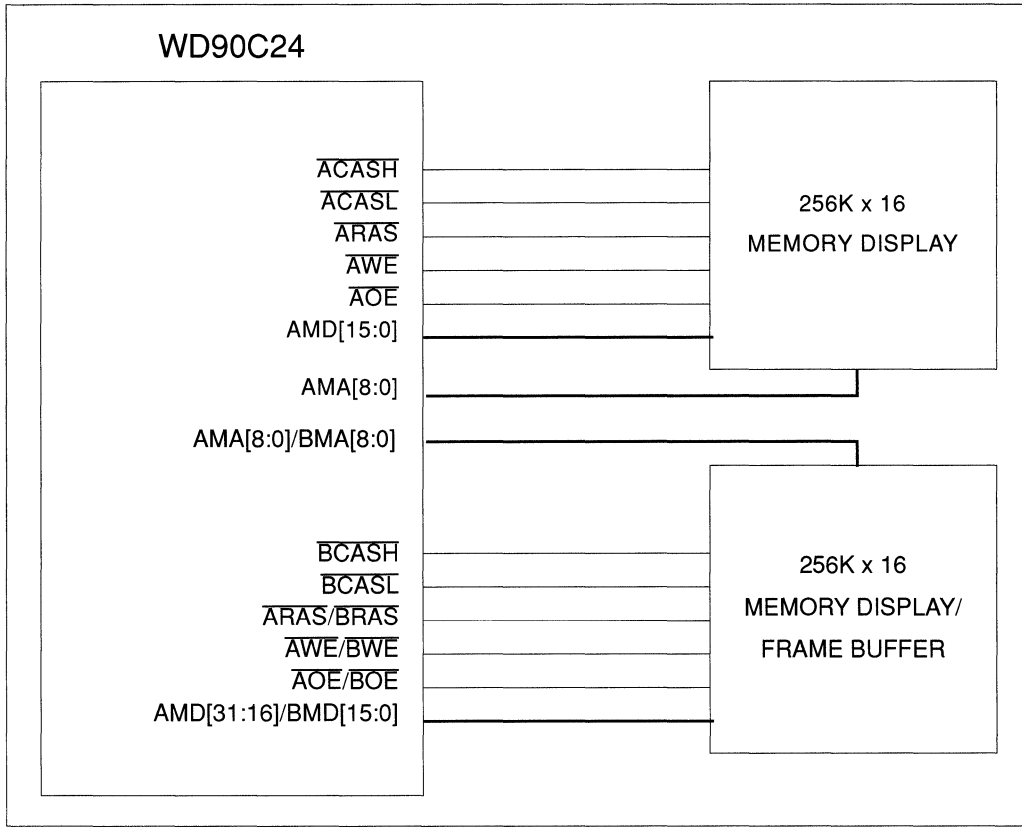


FIGURE 5-2 1 MB MEMORY CONFIGURATION

5.4 SIMULTANEOUS DISPLAY CONFIGURATION

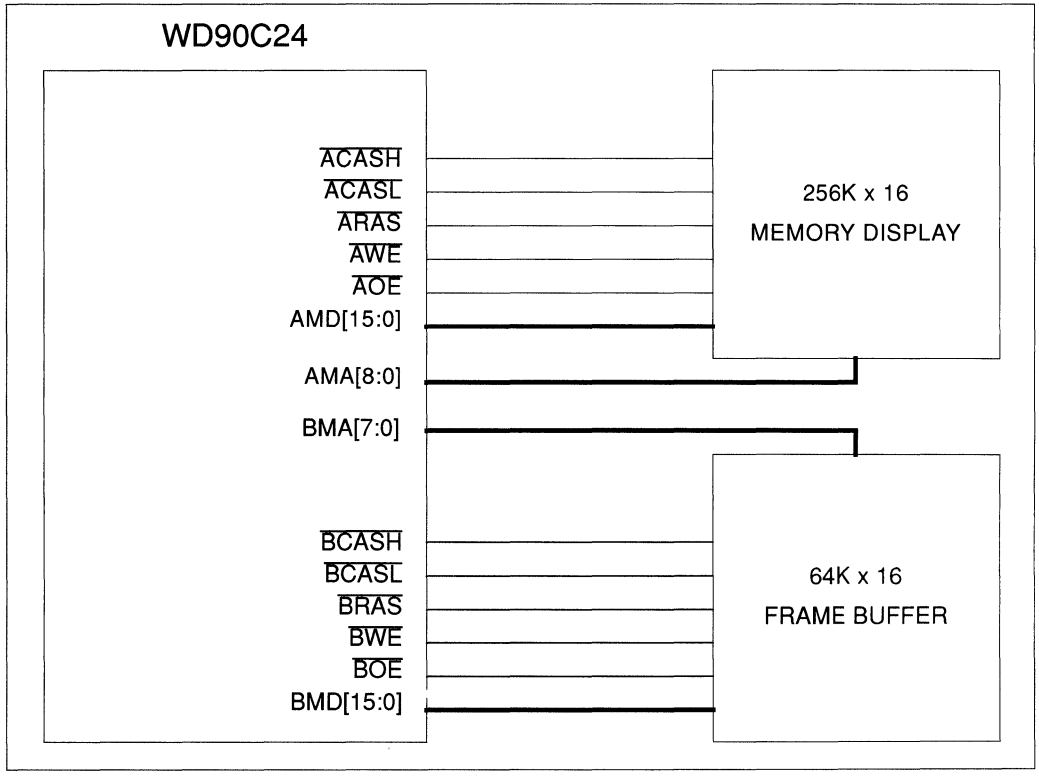


FIGURE 5-3 SIMULTANEOUS DISPLAY CONFIGURATION

13

5.5 512 KB HIGH-PERFORMANCE CONFIGURATION

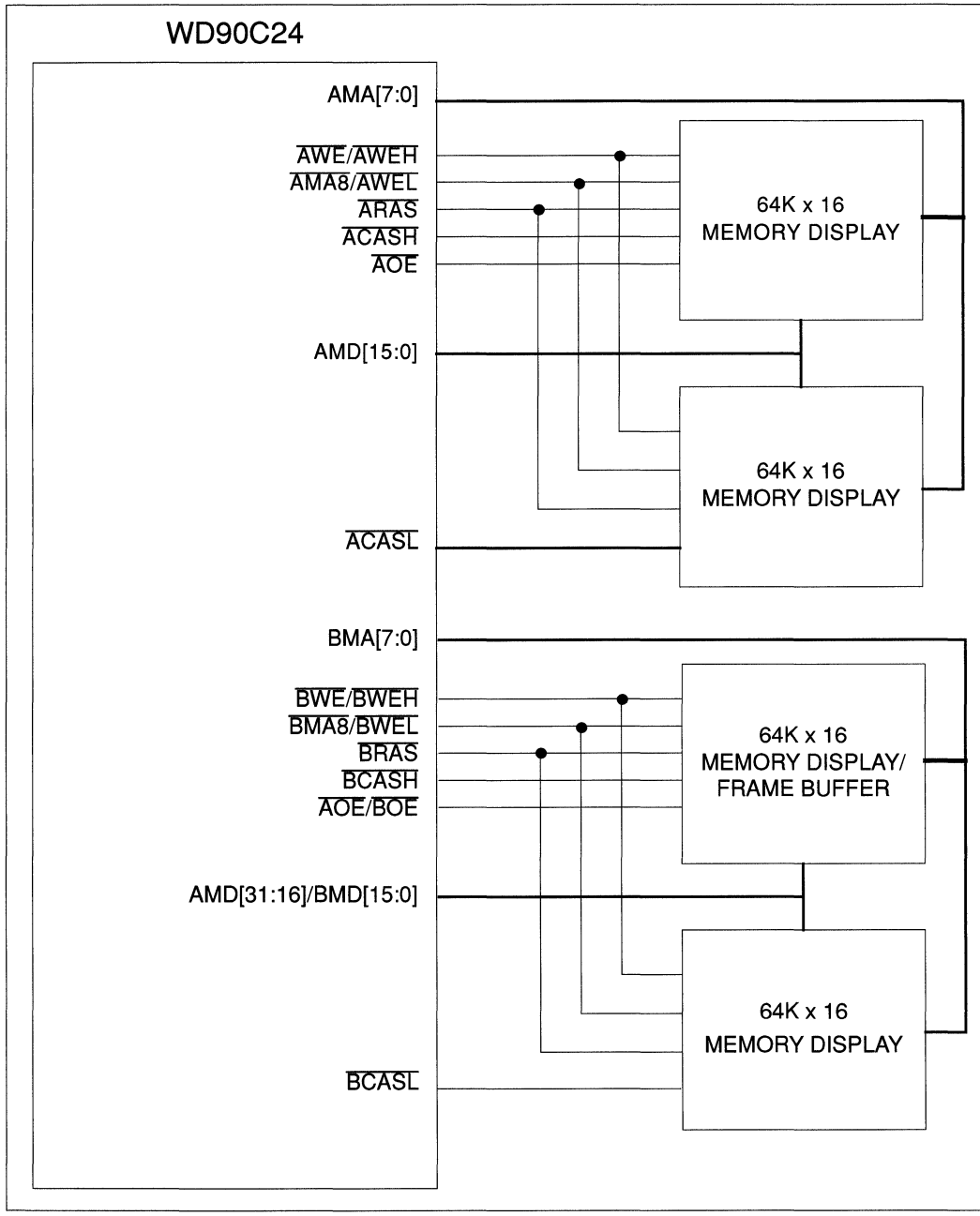


FIGURE 5-4 512 KB HIGH-PERFORMANCE CONFIGURATION

5.6 256 KB WITH SIMULTANEOUS DISPLAY CONFIGURATION

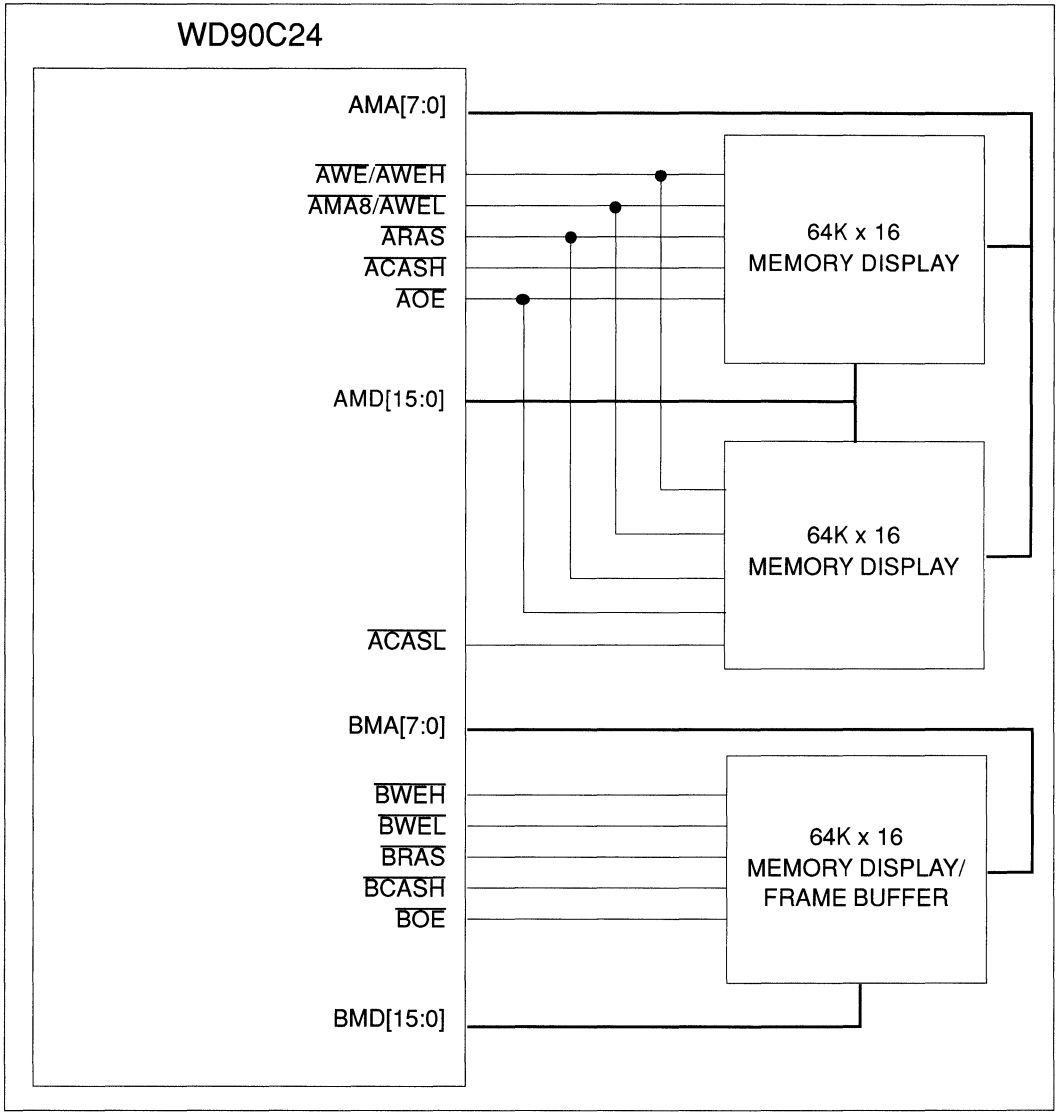


FIGURE 5-5 256 KB WITH SIMULTANEOUS DISPLAY CONFIGURATION

13

6.0 SIGNAL DESCRIPTIONS

This section contains detailed information concerning signals and pin outs for the WD90C24 controller 208-pin package.

6.1 INTRODUCTION

This section contains the following information:

- Signal Mnemonic to Pin Location Table
- Signal and Pin Configuration Diagram
- Detailed Signal Descriptions
- Pin Multiplexing Reference Tables

6.2 SIGNAL MNEMONIC TO PIN LOCATION

1.	BMD0	33.	BMA5[1]	65.	SLA19[2]	97.	SA16[2]
2.	BMD15	34.	BMA3[1]	66.	SLA20[2]	98.	$\overline{IOR}$/DC[2]
3.	BMD1	35.	BMA4[1]	67.	SLA21[2]	99.	$\overline{IOW}$/$\overline{BE1}$[2]
4.	BMD14	36.	VSS[3]	68.	SLA22[2]	100.	$\overline{MEMR}$/MIO[2]
5.	VSS[3]	37.	PD29	69.	SLA23[2]	101.	$\overline{MEMW}$/WR[2]
6.	BMD2	38.	PD28	70.	CLK486[2]	102.	AVDD1[3]
7.	BMD13	39.	PD27	71.	$\overline{IOCS16}$/$\overline{BOFF}$	103.	XMCLK[2]
8.	BMD3	40.	PD26	72.	$\overline{MEMCS16}$/ PD31	104.	MCAP[2]
9.	BMD12	41.	PD25	73.	SBHE/ CPURESET[2]	105.	VCAP[2]
10.	VDD[3]	42.	PD24	74.	ALE/NADS[2]	106.	VCLK2[2]
11.	BMD4	43.	VDD[3]	75.	IRQ/PD30	107.	AVSS1[3]
12.	BMD11	44.	PD23	76.	$\overline{EIO}$/$\overline{BE0}$[2]	108.	RVSS[3]
13.	BMD5	45.	PD22	77.	IOCHRDY/ $\overline{CPURDY}$	109.	SD0
14.	BMD10	46.	PD21	78.	$\overline{ZWST}$/ VLBIBUSY[1]	110.	SD1
15.	BMD6	47.	PD20	79.	VSS[3]	111.	SD2
16.	BMD9	48.	VSS[3]	80.	SA0/$\overline{BE3}$[2]	112.	SD3
17.	BMD7	49.	PD19	81.	SA1/$\overline{BE2}$[2]	113.	BVDD[3]
18.	BMD8	50.	PD18	82.	SA2[2]	114.	SD4
19.	MVDD[3]	51.	PD17	83.	SA3[2]	115.	SD5
20.	$\overline{BCASL}$[1]	52.	PD16	84.	SA4[2]	116.	SD6
21.	VSS[3]	53.	SD15	85.	SA5[2]	117.	SD7
22.	$\overline{BWE}$[1]	54.	SD14	86.	SA6[2]	118.	VSS[3]
23.	$\overline{BCASH}$[1]	55.	SD13	87.	SA7[2]	119.	XSCLKL[1]/ RGB17
24.	$\overline{BRAS}$[1]	56.	SD12	88.	RVDD[3]	120.	$\overline{WPLT}$[1]/RGB16
25.	$\overline{BOE}$[1]	57.	BVDD[3]	89.	SA8[2]	121.	$\overline{RPLT}$[1]/RGB15
26.	VDD[3]	58.	SD11	90.	SA9[2]	122.	STN14[1]/ RGB14
27.	BMA8[1]	59.	SD10	91.	SA10[2]	123.	STN13[1]/ RGB13
28.	BMA0[1]	60.	SD9	92.	SA11[2]	124.	STN12[1]/ RGB12
29.	BMA7[1]	61.	SD8	93.	SA12[2]	125.	VDD[3]
30.	BMA1[1]	62.	VSS[3]	94.	SA13[2]	126.	STN11[1]/RGB0
31.	BMA6[1]	63.	SLA17[2]	95.	SA14[2]	127.	STN10[1]/RGB1
32.	BMA2[1]	64.	SLA18[2]	96.	SA15[2]	128.	STN9[1]/RGB2

NOTE: Refer to notes at the end of this table.

TABLE 6-1 SIGNAL TO PIN LOCATION

129.	STN8[1]/RGB3	149.	SA27[2]	169.	PVDD[3]	189.	AMD6
130.	FPVDD[3]	150.	SA28[2]	170.	CKIN/XVCLK[2]	190.	AMD9
131.	VUD3/RGB11	151.	SA29[2]	171.	$\overline{\text{EBROM}}$/HRQ	191.	AMD7
132.	VUD2/RGB10	152.	SA30[2]	172.	$\overline{\text{VLBICS}}$/PRDY[1]	192.	AMD8
133.	VUD1/RGB9	153.	SA31[2]	173.	VSYNC[1]	193.	MVDD[3]
134.	VUD0/RGB8	154.	AVDD2[3]	174.	HSYNC[1]	194.	$\overline{\text{ACASL}}$[1]
135.	VLD3/RGB7	155.	MDETECT/ FSADJ[2]	175.	PCLK[1]	195.	VSS[3]
136.	VLD2/RGB6	156.	VREF[2]	176.	VSS[3]	196.	$\overline{\text{AWE}}$[1]
137.	VLD1/RGB5	157.	BLUE[1]	177.	AMD0	197.	$\overline{\text{ACASH}}$[1]
138.	VLD0/RGB4	158.	GREEN[1]	178.	AMD15	198.	$\overline{\text{ARAS}}$[1]
139.	VSS[3]	159.	RED[1]	179.	AMD1	199.	$\overline{\text{AOE}}$[1]
140.	SCLK/XSCLK[1]	160.	AVSS2[3]	180.	AMD14	200.	AMA8[1]
141.	RVDD[3]	161.	EXCKEN[2]	181.	AMD2	201.	AMA0[1]
142.	LP[1]	162.	RESET/ SYSRES[2]	182.	AMD13	202.	AMA7[1]
143.	FP[1]	163.	$\overline{\text{PDOWN}}$[2]	183.	AMD3	203.	AMA1[1]
144.	FR/BLANK/ ENDATA	164.	$\overline{\text{LCDENA}}$[1]	184.	AMD12	204.	AMA6[1]
145.	RVSS[3]	165.	PNLOFF[1]	185.	AMD4	205.	AMA2[1]
146.	SA24/VGACS[2]	166.	$\overline{\text{REFRESH}}$/ $\overline{\text{RDYIN}}$[2]	186.	AMD11	206.	AMA5[1]
147.	SA25[2]	167.	FPUSR0[1]	187.	AMD5	207.	AMA3[1]
148.	SA26[2]	168.	VCLK1/FPUSR1	188.	AMD10	208.	AMA4[1]

NOTES:

[1] Indicates output only signal names.

[2] Indicates input only signal names.

[3] Indicates VDD and VSS supply pins.

[4] Indicates proprietary test pins for internal use only.

Signal names not otherwise indicated are input/output.

TABLE 6-1 SIGNAL TO PIN LOCATIONS

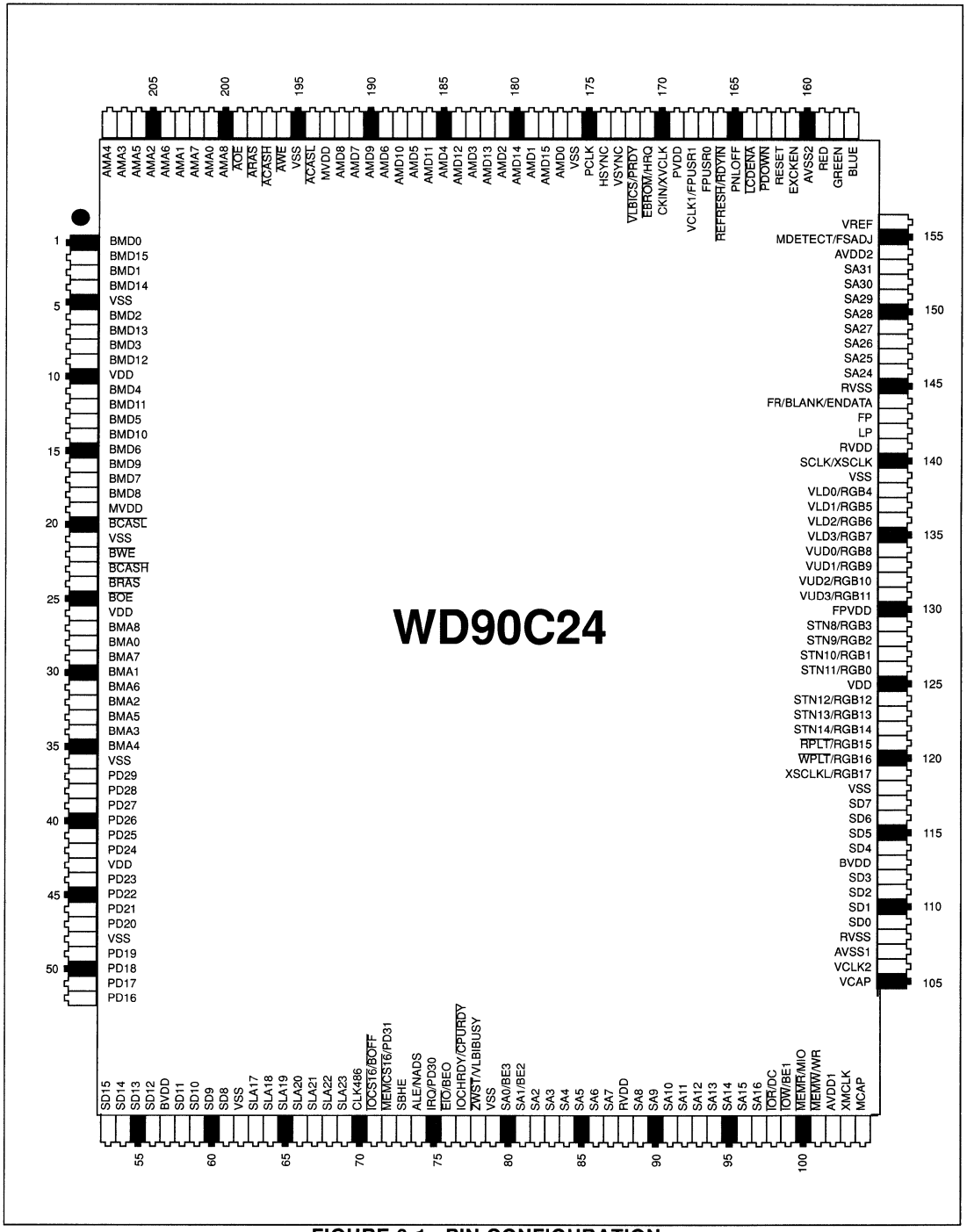


FIGURE 6-1 PIN CONFIGURATION

13

6.3 DETAILED SIGNAL DESCRIPTIONS

The following tables provide detailed signal descriptions for the WD90C24 controller 208-pin package. The signal descriptions are listed by the pin number and mnemonic given in Table 6-1. The definitions are listed in pin number order, as far as practical, within functional groups. Some signal definitions may appear in more than one functional group, if applicable, to aid the user in quick recovery of information for a particular group. The functional groups are listed below:

- Host Interface Pins
- Display Buffer Memory Interface Pins
- RAM DAC/CRT Interface Pins
- Clock Generation Interface Pins
- Panel Interface Pins
- Power and Ground Pins

Where more than one signal name is indicated on the same pin, the signal names are separated by a virgule (/) in Table 6-1. The pin usage, as described in Table 6-2, changes for each signal name depending upon the bus interface as follows:

1. The letters AT in the bus column indicate an Industry Standard Architecture (ISA) bus compatible signal. The terms AT bus and ISA bus are used interchangeably unless otherwise indicated.
2. The letters MC in the bus column indicate an IBM MicroChannel bus compatible signal.
3. The letters PI in the bus column indicate an Intel 386SL Peripheral Interface bus compatible signal.
4. The letters LOC in the bus column indicate a local bus compatible signal.

NOTE

The PI bus does not use MEMCS16 or IOCS16 type signals and cannot distinguish between 8-bit and 16-bit transfers. The WD90C24 uses PI bus signals for I/O transfers and memory cycles. Therefore, if there is a coresident VGA device, it must use the ISA bus for I/O transfers and memory cycles. Because the IOR, IOW, and AEN (EION) signals are not multiplexed with the PI bus, these lines should not be connected on the WD90C24 controller.

6.3.1 Host Interface Pin Definitions

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
71	$\overline{\text{IOCS16}}$	AT	Active Low Output	**I/O Chip Select 16 Bits** In AT mode, this signal used to respond to the host to allow 16-bit access to the I/O bus.
		PI	Active Low Output	**I/O Chip Select 16 Bits** In PI mode, since no 8-bit access will occur, this signal should be connected to Vss so it is always low.
	$\overline{\text{BOFF}}$	LOC	Active Low Output	**Bus Backoff** Connects to the 80486 BOFF pin. When active low, the 80486 retracts its last cycle and enables other masters to control the local bus. Its operation is similar to a read cycle for the VGA when the write buffers are full.
	$\overline{\text{CDSETUP}}$	MC	Active Low Input	**Card Setup** This signal is driven by the host to individually select channel connector slots during system configuration.
72	$\overline{\text{MEMCS16}}$	AT	Active Low Output	**Memory Chip Select 16 Bits** This line is used to respond to the host to enable 16-bit video memory data transfer.
	PM/$\overline{\text{IO}}$	PI	Active Low Input	**PI Bus Memory or I/O** Indicates the type of cycle currently executing on the PI bus. When high, the cycle is a memory operation, and when low the cycle is an Input/Output operation.
	PD31	LOC	Active High Input/ Output	**CPU Data Bus Bit 32** Provides bit 32 on the Local bus. This bit is combined with PD30 (pin 75), PD29:PD16, and SD15:SD0 to provide a 32-bit Local Data bus.
	$\overline{\text{CDDS16}}$	MC	Active Low Output	**Card Data Size 16 Bits** Indicates that a 16-bit resource is available at the current address.
73	SBHE	AT PI MC	Active High Input	**System Byte High Enable** Indicates a data transfer on the upper byte of the data bus (SD15:8).
	CPURESET	LOC	Active High Input	**CPU Reset** Local bus reset operation similar to AT bus RESET.

TABLE 6-2 HOST INTERFACE PIN SIGNAL DEFINITIONS

13

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
74	ALE	AT	Active High Input	**Address Latch Enable** Address bits SLA23:SLA17 are latched internally on the falling edge of the ALE.
	$\overline{\text{PSTART}}$	PI	Active Low Input	**PI Bus Start Signal** Indicates the start of a PI bus cycle. This signal is used to latch the address bus and command lines PM/IO, PW/R, and VGACS.
	$\overline{\text{ADS}}$	LOC	Active Low Input	**Address Status** Indicates the start of a Local bus cycle.
	$\overline{\text{ADL}}$	MC	Active Low Input	**Address Decode Latch** Latches address bits SLA23:SLA17.
75	IRQ	AT	Active High Output	**Interrupt Request** Programmable processor interrupt request. It is enabled via bit 5 in the Vertical Retrace End register. When the end of Vertical Display occurs, this signal goes active, causing an interrupt. It stays active until CRTC11 bit 4 clears it. In an AT system IRQ is usually not connected, but may be connected if desired.
	$\overline{\text{IRQ}}$	MC	Active Low Output	**Interrupt Request** Works similar to AT bus mode except that it is active low instead of active high.
	PD30	LOC	Active High Input/ Output	**CPU Data Bus Bit 30** Provides bit 31 on the Local bus. This bit is combined with PD31 (pin 72), PD29:PD16, and SD15:SD0 to provide a 32-bit Local Data bus.
76	$\overline{\text{EIO}}$	AT	Active Low Input	**Enable I/O** This signal is used to enable I/O address decoding and is connected directly to the system bus signal AEN (address enable).
	$\overline{\text{BE0}}$	LOC	Active Low Input	**Byte Enable 0** Byte enable for Local bus data bits SD7:SD0. $\overline{\text{BE3}}$:$\overline{\text{BE1}}$ are located on pins 80, 81, and 99, respectively.
	$\overline{\text{3C3D0}}$	MC	Active High Input	**Video Subsystem Enable Port** When pulled high, this signal "wakes up" the WD90C24 in a manner identical to setting the Wakeup Register (3C3h) bit 0 to 1. This signal enables video subsystem memory and I/O address decoding

TABLE 6-2 HOST INTERFACE PIN SIGNAL DEFINITIONS

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
77	IOCHRDY	AT	Active High Output	**Ready** Indicates to the system processor that a memory access is completed. It is used to add wait states to the CPU bus cycles during video memory accesses. It may be pulled inactive by the WD90C24 to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM.
	$\overline{\text{CPURDY}}$	LOC	Active Low Output	**CPU Ready** Ready signal to host processor.
	$\overline{\text{CDCHRDY}}$	MC	Active Low Output	**Channel Ready** This signal is normally active, and is driven not active by the WD90C24 to allow additional time to complete a channel cycle.
78	$\overline{\text{ZWST}}$	AT	Active Low Output	**Zero Wait State** This signal can be used to generate zero wait states to the AT bus. This signal can be programmed by the PR33(A) register, bits 7,6 in the following ways: **A.** $\overline{\text{0WS}}$ = 0 if write cache is not full. **B.** $\overline{\text{0WS}}$ = 0 if valid memory address decode AND write cache is not full. In this case $\overline{\text{0WS}}$ = 0 should be ANDed externally with $\overline{\text{MWR}}$ to generate zero wait state strobe. **C.** $\overline{\text{0WS}}$ = 0 if valid memory address decode AND write cache is not full, AND $\overline{\text{MWR}}$ is active. **D.** $\overline{\text{0WS}}$ = 0 if valid memory address decode AND write cache is not full AND $\overline{\text{MWR}}$ is active, OR valid I/O address decode AND $\overline{\text{IOW}}$ is active.
	$\overline{\text{PCMD}}$	PI	Active Low Input	**PI Bus Cycle Command** When asserted during write cycles, this signal indicates valid data on the PI bus, or that data bytes are ready to read. This signal must be asserted during read cycles to provide an output enable.
	VLBIBUSY	LOC	Active High Output, Open Collector	**VGA Local Bus Busy Signal** Local bus interface busy signal.
	$\overline{\text{CSFR}}$	MC	Active Low Output, Open Collector	**Card Selected Feedback** Asserted by WD90C24 to acknowledge its selection. Cannot be asserted if $\overline{\text{CDSETUP}}$ is asserted.

TABLE 6-2 HOST INTERFACE PIN SIGNAL DEFINITIONS

13

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
98	$\overline{IOR}$	AT, PI	Active Low Input	**I/O Read** I/O read strobe. This strobe signals an I/O read.
	D/C	LOC	Active Low Input	**Data or Code Indicator** Provides data or code indicator for the local bus.
	$\overline{S1}$	MC	Active Low Input	**S1 Cycle Decode** MicroChannel status. Used with $\overline{S0}$, M/$\overline{IO}$, and $\overline{CMD}$ to decode Microchannel bus cycles.
99	$\overline{IOW}$	AT, PI	Active Low Input	**I/O Write** Active low write strobe. This strobe signals an I/O write.
	$\overline{BE1}$	LOC	Active Low Input	**Byte Enable 1** Byte enable for Local bus data bits SD15:SD8. $\overline{BE3}$, $\overline{BE2}$, and $\overline{BE0}$ are located on pins 80, 81, and 76, respectively.
	$\overline{CMD}$	MC	Active Low Input	**Command** MicroChannel command. Used with $\overline{S0}$, $\overline{S1}$, and M/$\overline{IO}$ to decode Microchannel bus cycles.
100	$\overline{MEMR}$	AT	Active Low Input	**Memory Read** This signal indicates that a memory read cycle is occurring. $\overline{MEMR}$ is internally gated with $\overline{REFRESH}$.
	M/$\overline{IO}$	LOC	Active High/Low Input	**Memory or I/O Cycle** Local bus indicator for memory or I/O cycle. Low indicates I/O cycle and high indicates memory cycle.
	M/$\overline{IO}$	MC	Active High/Low Input	**Memory or I/O Cycle** MicroChannel memory or I/O cycle indicator. Low indicates I/O cycle; high indicates memory cycle.Used with $\overline{S0}$, $\overline{S1}$, and $\overline{CMD}$ to decode Microchannel bus cycles.
101	$\overline{MEMW}$	AT	Input	**Memory Write** This signal indicates that a memory write cycle is occurring. $\overline{MEMW}$ is internally gated with $\overline{REFRESH}$.
	PW/$\overline{R}$	PI	Active High/Low Input	**Write or Read Cycle** Indicates the type of access occurring on the PI bus. When high, the access is a write operation, and when low the access is a read operation.
	W/$\overline{R}$	LOC	Active High/Low Input	**Write or Read Cycle** Indicates the type of access occurring on the Local bus. When high, the access is a write operation, and when low the access is a read operation.
	$\overline{S0}$	MC	Active Low Input	**S0 Cycle Decode** MicroChannel status. Used with $\overline{S1}$, M/$\overline{IO}$, and $\overline{CMD}$ to decode Microchannel bus cycles.

TABLE 6-2 HOST INTERFACE PIN SIGNAL DEFINITIONS

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
162	RESET	AT, PI	Active High Input	**Reset** This signal resets the WD90C24. MCLK and VCLK should be connected to WD90C24 in order for the WD90C24 to initialize during Reset. Western Digital configuration bits are initialized at power-up reset based on the logic level on the Display Buffer Memory bus as determined by pull-up/pull-down resistors. The reset pulse width should be at least 10 MCLK clock periods.
	$\overline{\text{SYSRES}}$	LOC	Active Low Input	**System Reset** This signal resets the WD90C24. MCLK and VCLK should be connected to WD90C24 in order for the WD90C24 to initialize during Reset. Western Digital configuration bits are initialized at power-up reset based on the logic level on the Display Buffer Memory bus as determined by pull-up/pull-down resistors. The reset pulse width should be at least 10 MCLK clock periods.
	CHRESET	MC	Active High Input	**Channel Reset** Microchannel reset operation similar to AT bus RESET.
166	$\overline{\text{REFRESH}}$	AT, PI, MC	Active Low Input	**DRAM Refresh** Initiates video buffer memory refresh. This signal must be inactive (high) for memory reads or writes to occur.
	$\overline{\text{RDYIN}}$	LOC	Active Low Input	**Ready In** This signal is used for synchronizing the local bus with the host processor.
171	$\overline{\text{EBROM}}$	AT, MC	Active Low Output	**Enable BIOS ROM** This is an active low signal to enable BIOS ROM (C0000h - C7FFFh) if enabled by PR1(0). A WRITE to WD90C24 internal I/O port address 46E8h causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping.
	HRQ	LOC	Active High Input	**Hold Request** Indicates that a System Bus Request was received via a REFRESH, DMA, or MASTER signal. The host CPU responds by relinquishing the bus and asserting HOLD ACKNOWLEDGE.
172	$\overline{\text{PRDY}}$	PI	Active Low Output	**Bus Ready** Terminates a PI-bus cycle. The PI bus default is not ready and a bus cycle continues until $\overline{\text{PRDY}}$ is asserted by holding it low until the rising edge of $\overline{\text{PCMD}}$. The bus cycles is also terminated if $\overline{\text{PRDY}}$ is not asserted within a programmed time-out interval.
	$\overline{\text{VLBICS}}$	LOC	Active Low Output, Tristate	**Video Local Bus Interface Chip Select** Local bus chip select. This line is driven low only if the current cycle requires service by the Local bus interface. Otherwise, the line is tristated.

TABLE 6-2 HOST INTERFACE PIN SIGNAL DEFINITIONS

13

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
153 152 151 150 149 148 147	SA31 SA30 SA29 SA28 SA27 SA26 SA25	LOC	Active High Input	**Host System Address Bus (SA31 - SA23)** These local address bits should be connected to the host CPU address bus. These bits are combined with SLA23:SLA17, SA24 and SA16:SA2 to provide a 30-bit Local Bus Address. Internal pullup resistors are provided on these pins.
146	SA24	LOC	Active High Input	**Host System Address Bus (SA24)** This bit is combined with SLA23:SLA17 and SA16:SA2 to provide a 30-bit Local Bus Address. An internal pullup resistor is provided on this pin.
	$\overline{\text{VGACS}}$	PI	Active Low Input	**VGA Chip Select** Indicates access to user-defined VGA memory address space. It is not asserted during I/O cycles.
69 68 67 66 65 64 63	SLA23 SLA22 SLA21 SLA20 SLA19 SLA18 SLA17	All	Active High Input	**Host System/Latchable Address Bus (SLA23:SLA16)** These address bits should be connected to the host CPU address bus. For the AT, PI, and MC bus interfaces, these bits are combined with SA16:SA0 to provide a 24-bit address bus. For the Local bus interface, these bits are combined with SA31:SA24 and SA16:SA2 to provide a 30-bit Address Bus.
97 96 95 94 93 92 91 90 89 87 86 85 84 83 82	SA16 SA15 SA14 SA13 SA12 SA11 SA10 SA9 SA8 SA7 SA6 SA5 SA4 SA3 SA2	All	Active High Input	**Host System Address Bus (SA16 - SA2)** These address bits should be connected to the host CPU address bus. For the AT, PI, and MC bus interfaces, these bits are combined with SLA23:SLA17, SA1, and SA0 to provide a 24-bit address bus. For the Local bus interface, these bits are combined with SA31:SA24 and SLA23:SLA17 to provide a 30-bit Address Bus.

TABLE 6-2 HOST INTERFACE PIN SIGNAL DEFINITIONS

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
81	SA1	AT, PI, MC	Active High Input	**Host System Address Bus (SA1)** This address bit should be connected to the host CPU address bus. For the AT, PI, and MC bus interfaces, this bit is combined with SLA23:SLA17, SA16:SA2, and SA0 to provide a 24-bit address bus.
	BE2	LOC	Active Low Input	**Byte Enable 2** Local bus Byte Enable: for a 16-bit host CPU, $\overline{BE2}$ = SA1; for a 32-bit host CPU, $\overline{BE2}$ enables SD[23:16] $\overline{BE3}$, $\overline{BE1}$, and $\overline{BE0}$ are located on pins 80, 99, and 76, respectively.
80	SA0	AT, PI, MC	Active High Input	**Host System Address Bus (SA0)** This address bit should be connected to the host CPU address bus. For the AT, PI, and MC bus interfaces, this bit is combined with SLA23:SLA17, SA16:SA2, and SA1 to provide a 24-bit address bus.
	BE3	LOC	Active Low Input	**Byte Enable 3** Local bus Byte Enable: for a 16-bit host CPU, $\overline{BE3}$ is tied to an external pullup resistor; for a 32-bit host CPU, $\overline{BE3}$ enables SD[31:24] $\overline{BE2}$:$\overline{BE0}$ are located on pins 81, 99, and 76, respectively.
53 54 55 56 58 59 60 61 117 116 115 114 112 111 110 109	SD15 SD14 SD13 SD12 SD11 SD10 SD9 SD8 SD7 SD6 SD5 SD4 SD3 SD2 SD1 SD0	All	Active High Input/ Output	**DATA BUS (SD15 - SD0)** These bidirectional signals may be connected directly to a local data bus requiring less than 8 mA of source/sink, or may be connected through two external buffers. One external buffer for SD15:8 and the other external buffer for SD7:SD0. For the AT, PI, and MC bus interfaces, these bits provide a 16-bit system data bus. For the Local bus, these bits are combined with PD31 (pin 72), PD30 (pin 75), and PD29:PD16 to provide a 32-bit data bus.

TABLE 6-2 HOST INTERFACE PIN SIGNAL DEFINITIONS

13

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
37 38 39 40 41 42 44 45 46 47 48 50 51 52	PD29 PD28 PD27 PD26 PD25 PD24 PD23 PD22 PD21 PD20 PD19 PD18 PD17 PD16	LOC	Active High Input/ Output	**CPU Data Bus Bits (PD29:PD16)** Provide bits 29:16 on the WD909C24 Local bus. These bits are combined with PD30 (pin 75), PD31 (pin 72), and SD15:SD0 to provide a 32-bit Local Data bus.
163	$\overline{\text{PDOWN}}$	All	Active Low Input	**Power Down Selected** This active low input signal is used to disable the screen refresh cycle.

TABLE 6-2 HOST INTERFACE PIN SIGNAL DEFINITIONS

6.3.2 Display Buffer Memory Interface Pins

The display buffer memory interface is designed for connection of up to four 256Kx4 or one 256Kx16 fast-page-mode DRAMs. Also, memory data lines AMD[15:0] and BMD[15:0] are used to input configuration data (CNF[31:0]) at system power up and reset. For additional information on configuration bits, refer to the *WD90C24 Configuration Register* description in Section 22.

This section is divided into the following subsections, which list the bus lines as follows:

- Bank A Video Memory Bus
- Bank B Video Memory Bus

6. 3.2.1 Bank A Video Memory Bus

PIN	MNEMONIC	TYPE	DESCRIPTION
BANK A VIDEO MEMORY DATA/CONFIGURATION BITS			
178	AMD15	I/O	Bank A Memory Data Bit 15:Configuration Bit CNF15
180	AMD14	I/O	Bank A Memory Data Bit 14:Configuration Bit CNF14
182	AMD13	I/O	Bank A Memory Data Bit 13:Configuration Bit CNF13
184	AMD12	I/O	Bank A Memory Data Bit 12:Configuration Bit CNF12
186	AMD11	I/O	Bank A Memory Data Bit 11:Configuration Bit CNF8
188	AMD10	I/O	Bank A Memory Data Bit 10:Configuration Bit CNF10
190	AMD9	I/O	Bank A Memory Data Bit 9:Configuration Bit CNF9
192	AMD8	I/O	Bank A Memory Data Bit 8:Configuration Bit CNF11
191	AMD7	I/O	Bank A Memory Data Bit 7:Configuration Bit CNF7
189	AMD6	I/O	Bank A Memory Data Bit 6:Configuration Bit CNF6
187	AMD5	I/O	Bank A Memory Data Bit 5:Configuration Bit CNF5
185	AMD4	I/O	Bank A Memory Data Bit 4:Configuration Bit CNF4
183	AMD3	I/O	Bank A Memory Data Bit 3:Configuration Bit CNF3
181	AMD2	I/O	Bank A Memory Data Bit 2:Configuration Bit CNF2
179	AMD1	I/O	Bank A Memory Data Bit 1:Configuration Bit CNF1
177	AMD0	I/O	Bank A Memory Data Bit 0:Configuration Bit CNF0
BANK A VIDEO MEMORY ADDRESS BITS			
200	AMA8	Output	Bank A Memory Address Bit 8
202	AMA7	Output	Bank A Memory Address Bit 7
204	AMA6	Output	Bank A Memory Address Bit 6
206	AMA5	Output	Bank A Memory Address Bit 5

TABLE 6-3 BANK A VIDEO MEMORY SIGNALS

PIN	MNEMONIC	TYPE	DESCRIPTION
BANK A VIDEO MEMORY ADDRESS BITS (Continued)			
208	AMA4	Output	Bank A Memory Address Bit 4
207	AMA3	Output	Bank A Memory Address Bit 3
205	AMA2	Output	Bank A Memory Address Bit 2
203	AMA1	Output	Bank A Memory Address Bit 1
201	AMA0	Output	Bank A Memory Address Bit 0
NOTE: AMA8 through AMA0 form the primary 9-bit video buffer DRAM address bus. AMA8 is the MSB and AMA0 the LSB.			
BANK A VIDEO MEMORY CONTROL LINES			
194	$\overline{\text{ACASL}}$	Active Low Output	**CAS Bank A Low** Lower column address strobe for video memory buffer DRAM bank A.
196	$\overline{\text{AWE}}$	Active Low Output	**Write Enable Bank A** Write Enable control for video memory buffer DRAM bank A. When a 256Kx16 DRAM is used this is the DRAM write enable output.
197	$\overline{\text{ACASH}}$	Active Low Output	**CAS Bank A High** Upper column address strobe for video memory buffer DRAM bank A.
198	$\overline{\text{ARAS}}$	Active Low Output	**RAS Bank A** Row address strobe for video memory buffer DRAM bank A.
199	$\overline{\text{AOE}}$	Active Low Output	**Output Enable Bank A** Output Enable control for video memory buffer DRAM bank A. When a 256Kx16 DRAM is used, this is the DRAM output enable strobe.

TABLE 6-3 BANK A VIDEO MEMORY SIGNALS

6. 3.2.2 Bank B Video Memory Bus

PIN	MNEMONIC	TYPE	DESCRIPTION
BANK B VIDEO MEMORY DATA BITS/CONFIGURATION BITS			
2	BMD15	I/O	Bank B Memory Data Bit 15:Configuration Bit CNF31
4	BMD14	I/O	Bank B Memory Data Bit 14:Configuration Bit CNF30
7	BMD13	I/O	Bank B Memory Data Bit 13:Configuration Bit CNF29
9	BMD12	I/O	Bank B Memory Data Bit 12:Configuration Bit CNF28
12	BMD11	I/O	Bank B Memory Data Bit 11:Configuration Bit CNF27
14	BMD10	I/O	Bank B Memory Data Bit 10:Configuration Bit CNF26
16	BMD9	I/O	Bank B Memory Data Bit 9:Configuration Bit CNF25
18	BMD8	I/O	Bank B Memory Data Bit 8:Configuration Bit CNF24
17	BMD7	I/O	Bank B Memory Data Bit 7:Configuration Bit CNF23
15	BMD6	I/O	Bank B Memory Data Bit 6:Configuration Bit CNF22
13	BMD5	I/O	Bank B Memory Data Bit 5:Configuration Bit CNF21
11	BMD4	I/O	Bank B Memory Data Bit 4:Configuration Bit CNF20
8	BMD3	I/O	Bank B Memory Data Bit 3:Configuration Bit CNF19
6	BMD2	I/O	Bank B Memory Data Bit 2:Configuration Bit CNF18
3	BMD1	I/O	Bank B Memory Data Bit 1:Configuration Bit CNF17
1	BMD0	I/O	Bank B Memory Data Bit 0:Configuration Bit CNF16
BANK B VIDEO MEMORY ADDRESS BITS			
27	BMA8	Output	Bank Memory Address Bit 8
29	BMA7	Output	Bank Memory Address Bit 7
31	BMA6	Output	Bank Memory Address Bit 6
33	BMA5	Output	Bank Memory Address Bit 5
35	BMA4	Output	Bank Memory Address Bit 4
34	BMA3	Output	Bank Memory Address Bit 3
32	BMA2	Output	Bank Memory Address Bit 2
30	BMA1	Output	Bank Memory Address Bit 1
28	BMA0	Output	Bank Memory Address Bit 0

TABLE 6-4 BANK B VIDEO MEMORY SIGNALS

PIN	MNEMONIC	TYPE	DESCRIPTION
BANK B VIDEO MEMORY ADDRESS CONTROL LINES			
20	$\overline{\text{BCASL}}$	Active Low Output	**CAS Bank B Low** Lower column address strobe for video memory buffer DRAM bank B.
22	$\overline{\text{BWE}}$	Active Low Output	**Write Enable Bank B** Write Enable control for video memory buffer DRAM bank B.
23	$\overline{\text{BCASH}}$	Active Low Output	**CAS Bank B High** Upper column address strobe for video memory buffer DRAM bank B.
24	$\overline{\text{BRAS}}$	Active Low Output	**RAS Bank B** Row address strobe for video memory buffer DRAM bank B.
25	$\overline{\text{BOE}}$	Active Low Output	**Output Enable Bank B** Output Enable control for video memory buffer DRAM bank B.

TABLE 6-4 BANK B VIDEO MEMORY SIGNALS

6.3.3 RAM DAC/CRT Interface Pins

Internal DAC interface pins are described in the following table.

PIN	MNEMONIC	TYPE	DESCRIPTION
155	FSADJ	Analog Input	**Full Scale Adjust** A resistor (RSET) on this pin sets the full scale output current of the RED, GREEN, and BLUE DACs. FSADJ if pin 155 is above Vss. **CAUTION:** Do not ground this pin.
	$\overline{\text{MDETECT}}$	Active Low Input	**Monitor Detect** When pin 155 is grounded, this pin is used as a monitor detect input. The result of this input is read from 3C2h bit 4. MDETECT if pin 155 is tied to Vss.
156	VREF	Analog Input	**Voltage Reference Input** An external voltage reference of 1.2V is connected to this input for normal operation of the internal RAMDAC.
157	BLUE	Analog Output	**Blue Current Output** High impedance current source can directly drive a double-terminated 75-Ohm coaxial cable.
158	GREEN	Analog Output	**Green Current Output** High impedance current source can directly drive a double-terminated 75-Ohm coaxial cable.
159	RED	Analog Output	**Red Current Output** High impedance current source can directly drive a double-terminated 75-Ohm coaxial cable.
173	VSYNC	Active High Output	**CRT Vertical Sync** VSYNC is the CRT vertical sync control signal output. It may be directly attached to CRT monitor connections. Its active low or high level is programmable. Control of vertical sync polarity is done by setting register bits in the VGA Miscellaneous Output Register.
174	HSYNC	Active High Output	**CRT Horizontal Sync** HSYNC is the CRT horizontal sync control signal output. It may be directly attached to CRT monitor connections. Its active low or high level is programmable as is its position and duration. Control of horizontal sync polarity is done by setting register bits in the VGA Miscellaneous Output Register.

TABLE 6-5 INTERNAL DAC INTERFACE PINS

13

PIN	MNEMONIC	TYPE	DESCRIPTION
175	PCLK	Active High Input/ Output	**Pixel Clock** Video pixel clock output used by the external RAMDAC to latch pixel data from the WD90C24 controller's video output bus into an external RAMDAC or panel interface. Pixel data from the WD90C24 changes on the rising edge of PCLK and is intended to be latched into an external RAMDAC or panel interface by the falling edge of PCLK. In Auxiliary Video Extender (AVE) Mode, this pin provides the input for the internal RAMDAC PCLK signal.

TABLE 6-5 INTERNAL DAC INTERFACE PINS

6.3.4 Clock Generation Interface Pins

Clock generation interface pins are described in the following table.

PIN	MNEMONIC	TYPE	DESCRIPTION
70	CLK486	Input	**CPU Clock** Provides the clock input for the Local bus.
103	XMCLK	Input	**External Master Clock** In external PCLK mode, this signal is the MCLK input.
104	MCAP	Analog Input	**Analog Input** Connects to discrete filter network.
105	VCAP	Analog Input	**Analog Input** Connects to discrete filter network.
106	VCLK2	Input/ Output	**Video Clock 2** VCLK2 is one of three possible video clock inputs to the WD90C24. The three clock inputs (XVCLK, VCLK1, and VCLK2) are internally selected to provide video shift clock rates for various screen formats and display types.
161	EXCKEN	Active High Input	**External Clock Enable** Asserted to select external clock mode
168	VCLK1	Input/ Output	**Video Clock 1** VCLK1 is one of three possible video clock inputs to the WD90C24. The three clock inputs (XVCLK, VCLK1, and VCLK2) are internally selected to provide video shift clock rates for various screen formats and display types. In internal PCLK mode, VCLK1 is an output configured as FPUSR1.
170	CKIN	Input	**System Clock Input** Provides the CPU clock (14.318 MHz) when using the internal clock synthesizer, which is the default state.
	XVCLK	Input	**External Video Clock** Provides VCLK when using an external clock synthesizer.

TABLE 6-6 CLOCK GENERATION INTERFACE PIN TABLE

13

6.3.5 Panel Interface Pins

PIN	MNEMONIC	TYPE	DESCRIPTION
119	XSCLKL	Active High Output	**External Shift Clock Low** Used for 8-bit STN color LCD
	RGB17	Output	**Red Green Blue Bit 17** Data bit 17 for 18-bit TFT color LCD
120	$\overline{\text{WPLT}}$	Active Low Output	**Write Palette** If the WD90C24 has been configured for external DAC mode, $\overline{\text{WPLT}}$ is the write pulse to the external RAMDAC or equivalent circuit.
	RGB16	Output	**Red Green Blue Bit 16** Data bit 16 for 18-bit TFT color LCD
121	$\overline{\text{RPLT}}$	Active Low Output	**Read Palette** If not configured for a color TFT interface, this pin is the active low read pulse to the external RAMDAC or equivalent circuit.
	RGB15	Output	**Red Green Blue Bit 15** Data bit 15 for 18-bit TFT color LCD
	STN15		**Super Twisted Nematic Bit 15** Data bit 15 for 16-bit STN color LCD
122	RGB14	Output	**Red Green Blue Bit 14** Data bit 14 for 18-bit TFT color LCD
	STN14		**Super Twisted Nematic Bit 14** Data bit 14 for 16-bit STN color LCD
123	RGB13	Output	**Red Green Blue Bit 13** Data bit 13 for 18-bit TFT color LCD
	STN13		**Super Twisted Nematic Bit 13** Data bit 13 for 16-bit STN color LCD
124	RGB12	Output	**Red Green Blue Bit 12** Data bit 12 for 18-bit TFT color LCD
	STN12		**Super Twisted Nematic Bit 12** Data bit 12 for 16-bit STN color LCD
126	RGB0	Output	**Red Green Blue Bit 0** Data bit 0 for 18-bit TFT color LCD
	BD0		**Blue Data Bit 0** Data Bit 0 for 3-bit, 9-bit, and 12-bit TFT color LCD
	STN11		**Super Twisted Nematic Bit 11** Data bit 11 for 16-bit STN color LCD

TABLE 6-7 PANEL INTERFACE PINS

PIN	MNEMONIC	TYPE	DESCRIPTION
127	RGB1	Output	**Red Green Blue Bit 1** Data bit 1 for 18-bit TFT color LCD
	BD1		**Blue Data Bit 1** Data Bit 1 for 9-bit and 12-bit TFT color LCD
	STN10		**Super Twisted Nematic Bit 10** Data bit 10 for 16-bit STN color LCD
128	RGB2	Output	**Red Green Blue Bit 2** Data bit 2 for 18-bit TFT color LCD
	BD2		**Blue Data Bit 2** Data Bit 0 for 9-bit and 12-bit TFT color LCD
	STN9		**Super Twisted Nematic Bit 9** Data bit 9 for 16-bit STN color LCD
129	RGB3	Output	**Red Green Blue Bit 3** Data bit 3 for 18-bit TFT color LCD
	BD3		**Blue Data Bit 3** Data Bit 3 for 9-bit and 12-bit TFT color LCD
	STN8		**Super Twisted Nematic Bit 8** Data bit 8 for 16-bit STN color LCD
131	RGB11	Input/ Output	**Red Green Blue Bit 11** Data bit 11 for 18-bit TFT color LCD
	RD3		**Red Data Bit 3** Data bit 3 for 12-bit TFT color LCD
	STN7		**Super Twisted Nematic Bit 7** Data bit 7 for 8-bit and 16-bit STN color LCD
	VD7		**Video Data Bit 7** Data bit 7 for the 8-bit CRT interface
	VUD3		**UPPER PANEL DATA BIT 3:** In a dual-panel LCD interface, VUD3 through VUD0 are used for the upper panel data bus. In a single-panel LCD interface these pins also provide video data to the panel. In a plasma interface, they provide the pure 4-bit video data interface. In a CRT interface, they are the upper four bits of pixel video outputs to the RAMDAC. In Auxiliary Video Extender (AVE) Mode, this pin provides the P7 input for the internal RAMDAC.

TABLE 6-7 PANEL INTERFACE PINS

PIN	MNEMONIC	TYPE	DESCRIPTION
132	RGB10	Input/ Output	**Red Green Blue Bit 10** Data bit 10 for 18-bit TFT color LCD.
	RD2		**Red Data Bit 2** Data bit 2 for 9-bit and 12-bit TFT color LCD
	STN6		**Super Twisted Nematic Bit 6** Data bit 6 for 8-bit and 16-bit STN color LCD
	VD6		**Video Data Bit 6** Data bit 6 for the 8-bit CRT interface
	VUD2		**Upper Panel Data Bit 2** Refer to VUD3, pin 131 In Auxiliary Video Extender (AVE) Mode, this pin provides the P6 input for the internal RAMDAC.
133	RGB9	Input/ Output	**Red Green Blue Bit 9** Data bit 9 for 18-bit TFT color LCD.
	RD1		**Red Data Bit 1** Data bit 1 for 9-bit and 12-bit TFT color LCD
	STN5		**Super Twisted Nematic Bit 5** Data bit 5 for 8-bit and 16-bit STN color LCD
	VD5		**Video Data Bit 5** Data bit 5 for the 8-bit CRT interface
	VUD1		**Upper Panel Data Bit 1** Refer to VUD3, pin 131 In Auxiliary Video Extender (AVE) Mode, this pin provides the P5 input for the internal RAMDAC.
134	RGB8	Input/ Output	**Red Green Blue Bit 8** Data bit 8 for 18-bit TFT color LCD.
	RD0		**Red Data Bit 0** Data Bit 0 for 3-bit, 9-bit, and 12-bit TFT color LCD
	STN4		**Super Twisted Nematic Bit 4** Data bit 4 for 8-bit and 16-bit STN color LCD
	VD4		**Video Data Bit 4** Data bit 4 for the 8-bit CRT interface
	VUD0		**Upper Panel Data Bit 0** Refer to VUD3, pin 131 In Auxiliary Video Extender (AVE) Mode, this pin provides the P4 input for the internal RAMDAC.

TABLE 6-7 PANEL INTERFACE PINS

PIN	MNEMONIC	TYPE	DESCRIPTION
135	RGB7	Input/ Output	**Red Green Blue Bit 17** Data bit 17 for 18-bit TFT color LCD.
	GD3		**Green Data Bit 3** Data bit 3 for 12-bit TFT color LCD
	STN3		**Super Twisted Nematic Bit 3** Data bit 3 for 8-bit and 16-bit STN color LCD
	VD3		**Video Data Bit 7** Data bit 7 for the 8-bit CRT interface
	VLD3		**Lower Panel Data Bit 3** In a dual-panel LCD interface, VLD3 through VLD0 are used for the lower panel data bus. In a 4-bit plasma interface, they are reserved. In an 8-bit plasma interface they provide the second pixel of video data to the panel. In a CRT interface, they are the lower four bits of pixel video outputs to the RAMDAC. In Auxiliary Video Extender (AVE) Mode, this pin provides the P3 input for the internal RAMDAC.
136	RGB6	Input/ Output	**Red Green Blue Bit 6** Data bit 6 for 18-bit TFT color LCD.
	GD2		**Green Data Bit 2** Data bit 2 for 9-bit and 12-bit TFT color LCD
	STN2		**Super Twisted Nematic Bit 2** Data bit 2 for 8-bit and 16-bit STN color LCD
	VD2		**Video Data Bit 2** Data bit 2 for the 8-bit CRT interface
	VLD2		**Lower Panel Data Bit 2** Refer to VLD3, pin 135 In Auxiliary Video Extender (AVE) Mode, this pin provides the P2 input for the internal RAMDAC.

TABLE 6-7 PANEL INTERFACE PINS

13

PIN	MNEMONIC	TYPE	DESCRIPTION
137	RGB5	Input/ Output	**Red Green Blue Bit 5** Data bit 5 for 18-bit TFT color LCD.
	GD1		**Green Data Bit 1** Data bit 1 for 9-bit and 12-bit TFT color LCD
	GD0		**Green Data Bit 0** Data bit 0 for 3-bit TFT color LCD
	STN1		**Super Twisted Nematic Bit 1** Data bit 1 for 8-bit and 16-bit STN color LCD
	VD1		**Video Data Bit 1** Data bit 1 for the 8-bit CRT interface
	VLD1		**Lower Panel Data Bit 1** Refer to VLD3, pin 135 In Auxiliary Video Extender (AVE) Mode, this pin provides the P1 input for the internal RAMDAC.
138	RGB4	Output	**Red Green Blue Bit 4** Data bit 4 for 18-bit TFT color LCD.
	GD0		**Green Data Bit 0** Data bit 0 for 9-bit and 12-bit TFT color LCD
	STN0		**Super Twisted Nematic Bit 0** Data bit 0 for 8-bit and 16-bit STN color LCD
	VD0		**Video Data Bit 0** Data bit 0 for the 8-bit CRT interface
	VLD0		**Lower Panel Data Bit 0** Refer to VLD3, pin 135 In Auxiliary Video Extender (AVE) Mode, this pin provides the P0 input for the internal RAMDAC.
140	XSCLK	Active High Output	**X Driver Shift Clock** In a dual panel interface, this signal is used to shift the upper and lower panel data into the X-driver.
	SCLK		**Shift Clock** In a Monochrome LCD panel interface, this signal is used to shift the upper and lower panel data into the display drivers.
142	LP	Active High Output	**Latch Pulse** The LP output is intended to be used by a panel to latch all the current panel data into the current scan line of the panel.
143	FP	Active High Output	**Frame Pulse** FP is output as an indication to attached panels that a frame has begun.

TABLE 6-7 PANEL INTERFACE PINS

PIN	MNEMONIC	TYPE	DESCRIPTION
144	FR	Active High Output	**Frame Rate Signal** Whenever the WD90C24 is operating in any LCD mode, FR is a free-running clock, which is intended to be connected to FR inputs on some LCD panels. Frequency of its signal is programmable and is controlled by setting PR62.
	$\overline{\text{BLANK}}$	Active Low Input/ Output	**Blanking Control Signal** BLANK is the standard analog VGA RAMDAC blanking signal. Output when the WD90C24 is not operating in any LCD modes. In Auxiliary Video Extender (AVE) Mode, this pin provides the $\overline{\text{BLANK}}$ input for the internal RAMDAC.
	ENDATA	Active High Output	**Enable Data** This is a data enable output for panels. In a plasma interface, it is an "enable video" signal.
164	$\overline{\text{LCDENA}}$	Active Low Output	**LCD Panel Enable** $\overline{\text{LCDENA}}$ is used to control the power supply for the attached panel.
165	PNLOFF	Active High Output	**Panel Power Off** Provides the power off signal to the bias supply circuit of an LCD panel. The PNLOFF signal is used as a power enable/disable to the high voltage bias inverter of a panel, and is tied to the WD90C24 controller's power management circuit. The WD90C24 sequences this signal as part of the panel powerup/powerdown procedures designed to protect panel power circuit. A high at this output indicates power-off to the panel and a low power-on.
167	FPUSR0	Output	**User Programmable Output 0** This line can be programmed by the user to initiate or confirm an action.
168	FPUSR1	Output	**User Programmable Output 1** This line can be programmed by the user to initiate or confirm an action. **NOTE:** In external PCLK mode, FPUSR1 is configured as VCLK1.

TABLE 6-7 PANEL INTERFACE PINS

13

6.3.6 Power and Ground Pins

PIN NO.	MNEMONIC	DESCRIPTION
5, 21, 36, 48, 62, 79, 118, 139, 176, 195	VSS (9:0)	Ground VSS=0V
10, 26, 43, 125	VDD (3:0	Main VDD Power to Core Logic and Memory
19,193	MVDD[1:0]	Memory Interface VDD Supply
57,113	BVDD (1:0)	System Bus Interface Supply (VDD)
88,141	RVDD (1:0)	RAM Filtered Palette VDD Supply
102	AVDD1	PCLK Analog Power
107	AVSS1	PCLK Analog Ground
108,145	RVSS (1:0)	RAM Palette VSS Ground
130	FPVDD	Panel Interface VDD Supply
154	AVDD2	RAMDAC Analog Power
160	AVSS2	RAMDAC Analog Ground
169	PVDD	Power-Down Section VDD Supply

TABLE 6-8 POWER AND GROUND SIGNAL DEFINITIONS

6.4 PIN MULTIPLEXING REFERENCE TABLES

This subsection contains the following tables:

- Host Interface Pin Multiplexing
- Display Buffer Memory Interface Pin Multiplexing
- RAM DAC/CRT Interface Pin Multiplexing
- Clock Generation Interface Pin Multiplexing
- Panel Interface Pin Multiplexing
- Power Pin Multiplexing

6.4.1 Host Interface Pins

PIN NO.	AT BUS	MICRO-CHANNEL	PI BUS	LOCAL BUS
37-42, 44-47, 49-52	Reserved	Reserved	Reserved	PD(29:16)
53-56, 58- 61, 117 -114, 112-109	SD(15:0)	SD(15:0)	SD(15:0)	PD(15:0)
69	SLA23	SLA23	SLA23	SA23
68	SLA22	SLA22	SLA22	SA22
67	SLA21	SLA21	SLA21	SA21
66	SLA20	SLA20	SLA20	SA20
65	SLA19	SLA19	SLA19	SA19
64	SLA18	SLA18	SLA18	SA18
63	SLA17	SLA17	SLA17	SA17
71	$\overline{IOCS16}$	$\overline{CDSETUP}$	See NOTE 1	$\overline{BOFF}$
72	$\overline{MEMCS16}$	$\overline{CDDS16}$	PM/IO	PD31
73	SBHE	SBHE	SBHE	CPURESET
74	ALE	See NOTE 2	$\overline{PSTART}$	$\overline{ADS}$
75	IRQ	IRQ	Reserved	PD30
76	$\overline{EIO}$	$\overline{3C3D0}$	Reserved	$\overline{BE0}$
77	IOCHRDY	CDCHRDY	Reserved	$\overline{CPURDY}$
78	$\overline{ZWST}$	$\overline{CSFR}$	$\overline{PCMD}$	VLBIBUSY
97	SA16	SA16	SA16	SA16
96	SA15	SA15	SA15	SA15
95	SA14	SA14	SA14	SA14
94	SA13	SA13	SA13	SA13
93	SA12	SA12	SA12	SA12
92	SA11	SA11	SA11	SA11
91	SA10	SA10	SA10	SA10
90	SA9	SA9	SA9	SA9
89	SA8	SA8	SA8	SA8
87	SA7	SA7	SA7	SA7
86	SA6	SA6	SA6	SA6
85	SA5	SA5	SA5	SA5
84	SA4	SA4	SA4	SA4
83	SA3	SA3	SA3	SA3
82	SA2	SA2	SA2	SA2
81	SA1	SA1	SA1	$\overline{BE2}$

TABLE 6-9 HOST INTERFACE PIN MULTIPLEXING

PIN NO.	AT BUS	MICRO-CHANNEL	PI BUS	LOCAL BUS
80	SA0	SA0	SA0	$\overline{BE3}$
99	$\overline{IOW}$	$\overline{CMD}$	See NOTE 1	$\overline{BE1}$
98	$\overline{IOR}$	$\overline{S1}$	See NOTE 1	D/C
100	$\overline{MEMR}$	M/$\overline{IO}$	Reserved	M/$\overline{IO}$
101	$\overline{MEMW}$	$\overline{S0}$	PW/$\overline{R}$	W/$\overline{R}$
153 152 151 150 149 148 147	Reserved	Reserved	Reserved	SA31 SA30 SA29 SA28 SA27 SA26 SA25
146	Reserved	Reserved	VGACS	SA24
162	RESET	CHRESET	RESET	SYSRES
163	$\overline{PDOWN}$	$\overline{PDOWN}$	$\overline{PDOWN}$	$\overline{PDOWN}$
166	$\overline{REFRESH}$	$\overline{REFRESH}$	$\overline{REFRESH}$ See NOTE 3	$\overline{RDYIN}$
171	$\overline{EBROM}$	$\overline{EBROM}$	Reserved	HRQ
172	Reserved	Reserved	$\overline{PRDY}$	$\overline{VLBICS}$

NOTES:

1. In PI Bus Interface mode, a external pullup or pulldown resistor is needed on this pin.
2. In MicroChannel mode, ALE is not used and should be connected to VSS (ground).
3. In PI Bus Interface mode, $\overline{REFRESH}$ active during power down mode only.

TABLE 6-9 HOST INTERFACE PIN MULTIPLEXING

13

6.4.2 Display Buffer Memory Interface Pin Multiplexing

PIN NO.	ONE 256K x 16 CNF1	TWO 256K x 16 CNF 2	ONE 256K x 16 + ONE 64K x 16 CNF3	FOUR 64K x 16 CNF4	THREE 64K x 16 CNF 5
2	Reserved	BMD15	BMD15	BMD15	BMD15
4	Reserved	BMD14	BMD14	BMD14	BMD14
7	Reserved	BMD13	BMD13	BMD13	BMD13
9	Reserved	BMD12	BMD12	BMD12	BMD12
12	Reserved	BMD11	BMD11	BMD11	BMD11
14	Reserved	BMD10	BMD10	BMD10	BMD10
16	Reserved	BMD9	BMD9	BMD9	BMD9
18	Reserved	BMD8	BMD8	BMD8	BMD8
17	Reserved	BMD7	BMD7	BMD7	BMD7
15	Reserved	BMD6	BMD6	BMD6	BMD6
13	Reserved	BMD5	BMD5	BMD5	BMD5
11	Reserved	BMD4	BMD4	BMD4	BMD4
8	Reserved	BMD3	BMD3	BMD3	BMD3
6	Reserved	BMD2	BMD2	BMD2	BMD2
3	Reserved	BMD1	BMD1	BMD1	BMD1
1	Reserved	BMD0	BMD0	BMD0	BMD0
20	Reserved	$\overline{\text{BCASL}}$	$\overline{\text{BCASL}}$	$\overline{\text{BCASL}}$	Reserved
22	Reserved	$\overline{\text{BWE}}$	$\overline{\text{BWE}}$	$\overline{\text{BWE}}$	$\overline{\text{BWE}}$
23	Reserved	$\overline{\text{BCASH}}$	$\overline{\text{BCASH}}$	$\overline{\text{BCASH}}$	$\overline{\text{BCASH}}$
24	Reserved	$\overline{\text{BRAS}}$	$\overline{\text{BRAS}}$	$\overline{\text{BRAS}}$	$\overline{\text{BRAS}}$
25	Reserved	$\overline{\text{BOE}}$	$\overline{\text{BOE}}$	$\overline{\text{BOE}}$	$\overline{\text{BOE}}$
27	Reserved	BMA8	Reserved	BMA8	BMA8
29	Reserved	BMA7	BMA7	BMA7	BMA7
31	Reserved	BMA6	BMA6	BMA6	BMA6
33	Reserved	BMA5	BMA5	BMA5	BMA5
35	Reserved	BMA4	BMA4	BMA4	BMA4
34	Reserved	BMA3	BMA3	BMA3	BMA3
32	Reserved	BMA2	BMA2	BMA2	BMA2
30	Reserved	BMA1	BMA1	BMA1	BMA1
28	Reserved	BMA0	BMA0	BMA0	BMA0
178	AMD15	AMD15	AMD15	AMD15	AMD15
180	AMD14	AMD14	AMD14	AMD14	AMD14
182	AMD13	AMD13	AMD13	AMD13	AMD13

TABLE 6-10 DISPLAY MEMORY INTERFACE PIN MULTIPLEXING

PIN NO.	ONE 256K x 16 CNF1	TWO 256K x 16 CNF 2	ONE 256K x 16 + ONE 64K x 16 CNF3	FOUR 64K x 16 CNF4	THREE 64K x 16 CNF 5
184	AMD12	AMD12	AMD12	AMD12	AMD12
186	AMD11	AMD11	AMD11	AMD11	AMD11
188	AMD10	AMD10	AMD10	AMD10	AMD10
190	AMD9	AMD9	AMD9	AMD9	AMD9
192	AMD8	AMD8	AMD8	AMD8	AMD8
191	AMD7	AMD7	AMD7	AMD7	AMD7
189	AMD6	AMD6	AMD6	AMD6	AMD6
187	AMD5	AMD5	AMD5	AMD5	AMD5
185	AMD4	AMD4	AMD4	AMD4	AMD4
183	AMD3	AMD3	AMD3	AMD3	AMD3
181	AMD2	AMD2	AMD2	AMD2	AMD2
179	AMD1	AMD1	AMD1	AMD1	AMD1
177	AMD0	AMD0	AMD0	AMD0	AMD0
194	$\overline{\text{ACASL}}$	$\overline{\text{ACASL}}$	$\overline{\text{ACASL}}$	$\overline{\text{ACASL}}$	$\overline{\text{ACASL}}$
196	$\overline{\text{AWE}}$	$\overline{\text{AWE}}$	$\overline{\text{AWE}}$	$\overline{\text{AWEH}}$	$\overline{\text{AWEH}}$
197	$\overline{\text{ACASH}}$	$\overline{\text{ACASH}}$	$\overline{\text{ACASH}}$	$\overline{\text{ACASH}}$	$\overline{\text{ACASH}}$
198	$\overline{\text{ARAS}}$	$\overline{\text{ARAS}}$	$\overline{\text{ARAS}}$	$\overline{\text{ARAS}}$	$\overline{\text{ARAS}}$
199	$\overline{\text{AOE}}$	$\overline{\text{AOE}}$	$\overline{\text{AOE}}$	$\overline{\text{AOE}}$	$\overline{\text{AOE}}$
200	AMA8	AMA8	AMA8	AMA8	AMA8
202	AMA7	AMA7	AMA7	AMA7	AMA7
204	AMA6	AMA6	AMA6	AMA6	AMA6
206	AMA5	AMA5	AMA5	AMA5	AMA5
208	AMA4	AMA4	AMA4	AMA4	AMA4
207	AMA3	AMA3	AMA3	AMA3	AMA3
205	AMA2	AMA2	AMA2	AMA2	AMA2
203	AMA1	AMA1	AMA1	AMA1	AMA1
201	AMA0	AMA0	AMA0	AMA0	AMA0

TABLE 6-10 DISPLAY MEMORY INTERFACE PIN MULTIPLEXING

13

6.4.3 RAM DAC/CRT Interface Pin Multiplexing

PIN NO.	NORMAL DAC MODE	EXTERNAL RAMDAC MODE	NON-DAC FUNCTIONS
120		$\overline{\text{WPLT}}$	RGB16
121		$\overline{\text{RPLT}}$	RGB15
144		BLANK	FR/ENDATA
155	FADJUST	MDETECT	---
156	VREF	Ground	---
157	BLUE		---
158	GREEN		---
159	RED		---
173	VSYNC		---
174	HSYNC		---
175	PCLK	PCLK	---

TABLE 6-11 RAMDAC PIN MULTIPLEXING

6.4.4 Clock Generation Interface Pin Multiplexing

PIN NO.	SIGNAL NAME	DESCRIPTION	NON-CLOCK FUNCTIONS
70	CLK486		---
103	XMCLK	Proprietary Test Pin	---
104	MCAP	Analog Input	---
105	VCAP	Analog Clock	---
106	VCLK2	Video Clock Input (3 of 3)	---
119	XSCLKL	External Shift Clock Low	RGB17
140	XSCLK	X Driver Shift Clock	---
	SCLK	Shift Clock	---
144	FR	Frame Rate Signal	BLANK/ENDATA
161	EXCKEN	Internal/External Clock Enable	---
168	VCLK1	Video Clock Input (2 of 3)	FPUSR1
170	CKIN	System Clock Input	---
	XVCLK	Video Clock Input (1 of 3)	---
175	PCLK	Pixel Clock	---

TABLE 6-12 CLOCK SYNTHESIZER INTERFACE PIN MULTIPLEXING

6.4.5 Panel Interface Pin Multiplexing

PIN NO.	MONO LCD	CRT	STN COLOR LCD		TFT COLOR LCD			
			8-BIT	16-BIT	3-BIT	9-BIT	12-BIT	18-BIT
119	Reserved	Reserved	XSCLKL	Reserved	Reserved	Reserved	Reserved	RGB17
120	$\overline{\text{WPLT}}$	$\overline{\text{WPLT}}$	$\overline{\text{WPLT}}$	$\overline{\text{WPLT}}$	$\overline{\text{WPLT}}$	$\overline{\text{WPLT}}$	$\overline{\text{WPLT}}$	RGB16
121	$\overline{\text{RPLT}}$	$\overline{\text{RPLT}}$	$\overline{\text{RPLT}}$	STN15	$\overline{\text{RPLT}}$	$\overline{\text{RPLT}}$	$\overline{\text{RPLT}}$	RGB15
122	Reserved	Reserved	Reserved	STN14	Reserved	Reserved	Reserved	RGB14
123	Reserved	Reserved	Reserved	STN13	Reserved	Reserved	Reserved	RGB13
124	Reserved	Reserved	Reserved	STN12	Reserved	Reserved	Reserved	RGB12
126	Reserved	Reserved	Reserved	STN11	BD0	BD0	BD0	RGB0
127	Reserved	Reserved	Reserved	STN10	Reserved	BD1	BD1	RGB1
128	Reserved	Reserved	Reserved	STN9	Reserved	BD2	BD2	RGB2
129	Reserved	Reserved	Reserved	STN8	Reserved	Reserved	BD3	RGB3
131	VUD3	VD7	STN7	STN7	Reserved	Reserved	RD3	RGB11
132	VUD2	VD6	STN6	STN6	Reserved	RD2	RD2	RGB10
133	VUD1	VD5	STN5	STN5	Reserved	RD1	RD1	RGB9
134	VUD0	VD4	STN4	STN4	RD0	RD0	RD0	RGB8
135	VLD3	VD3	STN3	STN3	Reserved	Reserved	GD3	RGB7
136	VLD2	VD2	STN2	STN2	Reserved	GD2	GD2	RGB6
137	VLD1	VD1	STN1	STN1	GD0	GD1	GD1	RGB5
138	VLD0	VD0	STN0	STN0	Reserved	GD0	GD0	RGB4
140	SCLK	Reserved	XSCLK	XSCLK	XSCLK	XSCLK	XSCLK	XSCLK
142	LP	Reserved	LP	LP	LP	LP	LP	LP
143	FP	Reserved	FP	FP	FP	FP	FP	FP
144	FR	BLANK	FR	FR	ENDATA	ENDATA	ENDATA	ENDATA
164	$\overline{\text{LCDENA}}$	$\overline{\text{LCDENA}}$	$\overline{\text{LCDENA}}$	$\overline{\text{LCDENA}}$	$\overline{\text{LCDENA}}$	$\overline{\text{LCDENA}}$	$\overline{\text{LCDENA}}$	$\overline{\text{LCDENA}}$
165	PNLOFF	PNLOFF	PNLOFF	PNLOFF	PNLOFF	PNLOFF	PNLOFF	PNLOFF
167	FPUSR0	FPUSR0	FPUSR0	FPUSR0	FPUSR0	FPUSR0	FPUSR0	FPUSR0
168	FPUSR1	FPUSR1	FPUSR1	FPUSR1	FPUSR1	FPUSR1	FPUSR1	FPUSR1

NOTE
In External PCLK mode, FPUSR1 is configured as VCLK1.

TABLE 6-13 PANEL INTERFACE PIN MULTIPLEXING

6.4.6 Power and Ground Pins

PIN NO.	MNEMONIC	DESCRIPTION
102	AVDD1	PCLK Analog Power
154	AVDD2	RAMDAC Analog Power
107	AVSS1	PCLK Analog Ground
160	AVSS2	RAMDAC Analog Ground
57,113	BVDD (1:0)	System Bus Interface Supply (VDD)
130	FPVDD	Panel Interface VDD Supply
19,193	MVDD[1:0]	Memory Interface VDD Supply
163	$\overline{\text{PDOWN}}$	**Power Down Selected** This active low input signal is used to disable screen refresh cycle.
169	PVDD	Power-Down Section VDD Supply
88,141	RVDD (1:0)	RAM Filtered Palette VDD Supply
108,145	RVSS (1:0)	RAM Palette VSS Ground
10, 26, 43, 125	VDD (3:0	Main VDD Power to Core Logic and Memory
5, 21, 36, 48, 62, 79, 118, 139, 176, 195	VSS (9:0)	Ground VSS=0V
NOTE: Signals are listed in alphabetic order of the mnemonic.		

TABLE 6-14 POWER AND GROUND PIN MULTIPLEXING

7.0 REGISTER SUMMARY

7.1 INTRODUCTION

All the standard IBM registers incorporated in the WD90C24 are functionally equivalent to the VGA implementation. Additional Western Digital registers provide functional equivalence for AT&T, Hercules, MDA, and CGA standards defined earlier using the 6845 CRT Controller. This section describes all registers in detail. For more information, refer to the reference literature.

7.2 VGA REGISTERS

REGISTERS	RW	MONO	MONO	COLOR	EITHER
Miscellaneous Output Register	W			3C2h	
	R			3CCh	
Input Status Register 0	RO			3C2h	
Input Status Register 1	RO	3BAh	3DAh		
Feature Control Register	W	3BAh	3DAh		
	R			3CAh	
*Video Subsystem Enable Register	RW			3C3h	

TABLE 7-1 VGA REGISTERS SUMMARY

NOTES

* Video Subsystem Enable Register. I/O Port 3C3h can be used to replace 46E8h (if CNF (9) = 0) for setup in AT mode. In Micro Channel Mode, writes to 3C3h, bit 0 = 1 enables memory and I/O address decoding.

1. Reserved bits should be set to zero.
2. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

0 = B in Monochrome Modes

1 = D in Color Modes

7.3 SEQUENCER REGISTERS

REGISTERS	RW	MONO	COLOR	EITHER
Sequencer Index Register	RW			3C4h
Sequencer Data Register	RE			3C5h

TABLE 7-2 SEQUENCER REGISTERS SUMMARY

13

7.4 CRT CONTROLLER REGISTERS

REGISTERS	RW	MONO	COLOR	EITHER
Index Register	RW	3B4h	3D4h	
CRT Controller Data Register	RW	3B5h	3D5h	

TABLE 7-3 CRT CONTROLLER REGISTERS SUMMARY

7.5 GRAPHICS CONTROLLER REGISTERS

REGISTERS	RW	MONO	COLOR	EITHER
Index Register	RW			3CEh
Other Graphics Register	RW			3CFh

TABLE 7-4 GRAPHICS CONTROLLER REGISTERS SUMMARY

7.6 ATTRIBUTE CONTROLLER REGISTERS

REGISTERS	RW	MONO	COLOR	EITHER
Index Register	RW			3C0h
Attribute Controller Data Register	W			3C0h
	R			3C1h

TABLE 7-5 ATTRIBUTE CONTROLLER REGISTERS SUMMARY

7.7 VIDEO PALETTE REGISTERS

REGISTERS	RW	MONO	COLOR	EITHER
Write Address	RW			3C8
Read Address	W			3C7
DAC State	R			3C7
Data	RW			3C9
Pel Mask	RW			3C6

NOTES
1. RO = Read-Only, RW = Read/Write, W = Write, and R = Read.
2. All Register addresses are in hex.

TABLE 7-6 VIDEO PALETTE REGISTERS SUMMARY

7.8 PARADISE REGISTERS

There are three sets of Paradise Registers in the WD90C24:

- General Paradise Registers
- Extended Paradise Registers
- Flat Panel Paradise Registers

Each category of Paradise Registers is summarized in the following tables, and described in the subsequent sections of this document.

7.8.1 General Paradise Registers

REGISTERS	RW[1]	DESIGNATION[2]	I/O LOCATION[3]	SECTION
Address Offset A	RW	PR0 (A)	3CF.09	13.1
Address Offset B	RW	PR0 (B)	3CF.0A	13.1
Memory Size	RW	PR1	3CF.0B	13.2
Video Select	RW	PR2	3CF.0C	13.3
CRT Lock Control	RW	PR3	3CF.0D	13.4
Video Control	RW	PR4	3CF.0E	13.5
Unlock PR0 - PR4/General Purpose Status	RW	PR5	3CF.0F	13.6
Unlock PR11 - PR1A	RW	PR10	3?5.29	13.7
EGA Switches	RW	PR11	3?5.2A	13.8
Scratch Pad	RW	PR12	3?5.2B	13.9
Interlace H/2 Start	RW	PR13	3?5.2C	13.10
Interlace H/2 End	RW	PR14	3?5.2D	13.11
Miscellaneous Control 1	RW	PR15	3?5.2E	13.12
Miscellaneous Control 2	RW	PR16	3?5.2F	13.13
Miscellaneous Control 3	RW	PR17	3?5.30	13.14
CRTC Vertical Timing Overflow	RW	PR18A	3?5.3D	13.15
NOTE Refer to notes following Table 7-9.				

TABLE 7-7 GENERAL PARADISE REGISTERS

13

7.8.2 Paradise Extended Registers

REGISTERS	RW[1]	DESIGNATION[2]	I/O LOCATION[3]	SECTION
[7]Unlock Sequencer Extended	W	PR20	3C5.06	13.18
[7]Display Configuration and Scratch Pad	RW	PR21	3C5.07	13.19
[7]Scratch Pad	RW	PR22	3C5.08	13.20
[7]Scratch Pad	RW	PR23	3C5.09	13.21
[7]Memory Interface Write Buffer and FIFO Control	RW	PR30(A)	3C5.10	13.22
[7]System Interface Control	RW	PR31	3C5.11	13.23
[7]Miscellaneous Control 4	RW	PR32	3C5.12	13.24
[7]DRAM Timing and ZERO Wait State Control	RW	PR33(A)	3C5.13	13.25
[7]Video Memory Mapping	RW	PR34(A)	3C5.14	13.26
[8]USR0, USR1 Output Select	RW	PR35(A)	3C5.15	13.27
[8]Video Signature Analyzer Control	RO	PR45	3C5.16	13.28
[8]Signature Analyzer Data I	RO	PR45(A)	3C5.17	13.28.1
[8]Signature Analyzer Data II	RO	PR45(B)	3C5.18	13.28.2
[8] Feature Register I	RW	PR57	3C5.19	13.29
[8] Feature Register II	RW	PR58	3C5.20	13.30
[9]Memory Map to I/O Register for BLT Access in PI/Local Bus	RW	PR58(A)	3C5.26	13.31
[8] Memory Arbitration Cycle Setup	RW	PR59	3C5.21	13.32
[8] Frame Buffer Controller I Test	RW	PR60	3C5.22	13.33
[8] Frame Buffer Controller II Test	RW	PR61	3C5.23	13.34
[8]FR Timing	RW	PR62	3C5.24	13.35
[9]Read/Write FIFO Control	RW	PR63	3C5.25	13.36
[9]Reserved for Future Need	RW	PR64	3C5.27	13.37
[9]Reserved for Future Need	RW	PR65	3C5.28	13.38
[9]RAMDAC/PCLK	RW	PR66	3C5.29	13.39
[9]Programmable Clock Selection	RW	PR68	3C5.31	13.40
[9]Programmable VCLK Frequency	RW	PR69	3C5.32	13.41
[9]Mixed Voltage Override	RW	PR70	3C5.33	13.42
[9]Programmable REFRESH Timing	RW	PR71	3C5.34	13.43
[9]Programmable Clock Unlock	RO	PR72	3C5.35	13.44
[9]VGA Status Detect	RO	PR73	3C5.36	13.45
NOTE: Refer to notes following Table 7-9.				

TABLE 7-8 PARADISE EXTENDED REGISTERS SUMMARY

7.8.3 Flat Panel Paradise Registers

REGISTERS	RW[1]	LOCATION		SECTION
		MONO-CHROME	COLOR	
PR18 Flat Panel Status	R[6]	3B5.31	3D5.31	14.1
PR19 Flat Panel Control I	RW	3B5.32	3D5.32	14.2
PR1A Flat Panel Control II	RW	3B5.33	3D5.33	14.3
PR1B Flat Panel Unlock	W	3B5.34	3D5.34	14.4
PR30 Mapping RAM Unlock	W	3B5.35	3D5.35	14.5
PR33 Mapping RAM Address Counter	RW	3B5.38	3D5.38	14.6
PR34 Mapping RAM Data	RW	3B5.39	3D5.39	14.7
PR35 Mapping RAM and Powerdown Control	RW[6]	3B5.3A	3D5.3A	14.8
PR36 LCD Panel Height Select	RW	3B5.3B	3D5.3B	14.9
PR37 Flat Panel Blinking Control	RW	3B5.3C	3D5.3C	14.10
PR39 Color LCD Control	RW	3B5.3E	3D5.3E	14.11
PR41 Vertical Expansion Initial Value	RW	3B5.37	3D5.37	14.13
PR44 Power Down Memory Refresh Control	RW	3B5.3F	3D5.3F	14.14

TABLE 7-9 FLAT PANEL PARADISE REGISTERS SUMMARY

NOTES FOR TABLES 7-7, 7-8 and 7-9

1. RO - Read-Only, WO = Write-only, RW = Read/Write
2. In the PR register notation, XXX.YY,XXX is the data port address and YY is the register index.
3. All register addresses are in hex.
4. The designation 3?5 means that the register is mapped into either 3B5 in monochrome mode or 3D5 in color modes.
5. This register is loaded during power on.
6. Not all bits in PR18 and 35 are readable.
7. These registers are compatible with registers in the WD90C31 VGA controller.
8. These registers are compatible with registers in the WD90C26 VGA controller.
9. These registers were not used in any previous Western Digital VGA controller.

13

7.8.4 Local Bus Registers

ADDRESS	DEFAULT VALUE	PROGRAMMED BY	DESCRIPTION
2DF0[1:0]	00	BIOS	**Enable dual display** **Bits[1:0]** CGA MDA 00 = Disable Disable 01 = Disable Disable 10 = Disable Enable 11 = Enable Disable
2DF0[2]	1	BIOS	**Enable BOFF** 0 = Enable $\overline{\text{BOFF}}$ 1 = Disable $\overline{\text{BOFF}}$
2DF0[3]	0	BIOS	**VGA Data Path** 0 = 16-bit Data Path 1 = 32-bit Data Path
2DF0[4]	---	BMD[2]	**Determines the pulse width of RAMDAC IOR and IOW command, high/low duration** 0 = 9 clock 1 = 18 clock
2DF0[5]	---	BMD[13]	**Enable Local Bus Interface Logic** 0 = Disable Logic 1 = Enable Logic
2DF0[6]	---	BMD[14]	**External/Local Bus RAMDAC** 0 = External RAMDAC 1 = Local Bus RAMDAC
2DF0[7]	---	BMD[15]	**External/Local Bus BIOS** 0 = External BIOS 1 = Local Bus BIOS
2DF1[0] 2DF1[1]	--- ---	BMD[6] BMD[7]	**Memory Read or Write Low Duration Bits[1:0]** 00 = 2 clocks 01 = 3 clocks 10 = 4 clocks 11 = 5 clocks
2DF1[2] 2DF1[3]	--- ---	BMD[8] BMD[9]	**Memory Read or Write High Duration Bits[3:2]** 00 = 2 clocks 01 = 3 clocks 10 = 4 clocks 11 = 5 clocks

TABLE 7-10 LOCAL BUS REGISTERS

ADDRESS	DEFAULT VALUE	PROGRAMMED BY	DESCRIPTION
2DF1[4] 2DF1[5]	--- ---	BMD[10] BMD[11]	**$\overline{IOR}$ or $\overline{IOW}$ High/Low Duration Bits[5:4]** 00 = 2 clocks 01 = 3 clocks 10 = 4 clocks 11 = 5 clocks
2DF1[6]	1	BIOS	**Enable Wait State** 0 = 0 Wait States 1 = 1 Wait State
2DF1[7]	---	---	**Reserved**
2DF2[7:0]	00	BIOS	**High Address A[31:24] decode compare**

TABLE 7-10 LOCAL BUS REGISTERS

7.9 COMPATIBILITY REGISTERS

FUNCTIONS	RW	MDA	CGA	AT&T	HERCULES
Mode Control Register	WO	3B8	3D8	3D8	3B8
Color Select Register	WO		3D9	3D9	
Status Register	RO	3BA	3DA	3DA	3BA
Preset Light Pen Latch	WO	3B9	3DC	3DC	
Clear Light Pen Latch	WO	3BB	3DB	3DB	
AT&T/M24 Register	WO			3DE	
Hercules Register	WO				3BF
*CRTC	RW	3B0 - 3B7	3D0 - 3D7	3D0 - 3D7	3B0 - 3B7

NOTES

1. RO = Read-Only, WO = Write-Only, RW = Read/Write.
2. All Register addresses are in hex.
3. * = 6845 Mode Registers.
4. ** = This register is loaded during power-on.
5. Throughout this section, all bit graphics and definitions apply to VGA mode followed by their brief description.

TABLE 7-11 COMPATIBILITY REGISTERS SUMMARY

8.0 VGA GENERAL REGISTERS

This section contains complete descriptions of all the VGA General Registers. Refer to section 5 for a register summary.

8.1 MISCELLANEOUS OUTPUT REGISTER

Read Port = 3CCh, Write Port = 3C2h

BIT	FUNCTION
7	Vertical Sync Polarity Select
6	Horizontal Sync Polarity Select
5	Odd/Even Memory Page Select
4	Reserved
3	Clock Select 1
2	Clock Select 0
1	Enable Video RAM
0	I/O Address Select

Bit 7 *

Vertical Sync Polarity Selection.

0 = Positive vertical sync polarity.
1 = Negative vertical sync polarity.

Bit 6 *

Horizontal Sync Polarity Selection.

0 = Positive horizontal sync polarity.
1 = Negative horizontal sync polarity.

NOTE

* These bits determined the vertical size of the vertical frame by the monitor. Their encoding is shown below:

BIT 7	BIT 6	VERTICAL FRAME
0	0	Reserved
0	1	400 lines/scan
1	0	350 lines/scan
1	1	480 lines/scan

Bit 5

Odd or Even Memory Page Select.

When in modes 0 - 5, one memory page is selected from the two 64KB pages.

0 = Lower page is selected.
1 = Upper page is selected.

Bit 4

Reserved in VGA.

BIT (3:2) Clock Select 1,0

BIT 3	BIT 2	FUNCTION
0	0	Selects VCLK0 for VGA applications. Can be connected to allow 640 dots/line (25.175 MHz)
0	1	Selects VCLK1 for VGA applications. Can be connected to allow 720 dots/line (28.322 MHZ) if Configuration Register bit 3 = 0.
1	0	Selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.
1	1	Reserved. Also selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.

13

Bit 1

System Processor Video RAM Access Enable.

0 = CPU access disabled.
1 = CPU access enabled.

Bit 0

CRT Controller I/O Address Range Selection. Selection for Monochrome (3B4 and 3B5), or Color (3D4 and 3D5) mode. Bit 0 also maps Input Status Register 1 at MDA (3BA) or CGA (3DA).

0 = CRTC and status addresses for MDA mode (3BX).
1 = CRTC and status addresses for CGA mode (3DX).

8.2 INPUT STATUS REGISTER 0

Read Only Port = 3C2h

BIT	FUNCTION
7	CRT Interrupt
6:5	Reserved
4	Monitor Detect Bit for Color/ Monochrome Display
3: 0	Reserved

Bit 7

CRT Vertical Retrace Interrupt Pending or Cleared.

0 = Vertical retrace interrupt cleared.
1 = Vertical retrace interrupt pending.

Bit (6:5)

Reserved in VGA.

Bit 4

Monitor Detection in VGA mode. DA15 monitor status
(pin 20) is sampled and can be read from this bit.

Bit 3:0

Reserved.

8.3 INPUT STATUS REGISTER 1

Read Only Port = 3?Ah

BIT	FUNCTION
7:6	Reserved
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2	Reserved
0	Display Enable

Bit 7:6

Reserved.

Bit 5:4

Color Plane Diagnostics.

These bits allow the processor to set two out of eight colors by activating the Attribute Controller's Color Plane Enable Register bits 4 and 5. Their status is defined in the following table:

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
BIT 5	BIT4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit 3

Vertical Retrace Status.

0 - Vertical frame is displayed.
1- Vertical retrace is active.

Bit 2:1

Reserved.

Bit 0

Display Enable Status.

0 - CRT screen display is process.
1 - CRT screen display disabled for horizontal or vertical retrace interval.

8.4 FEATURE CONTROL REGISTER

Read Port = 3CAh
Write Port = 3?Ah

BIT	FUNCTION
7:4	Reserved
3	Vertical Sync Control
2:0	Reserved

Bits 7:4

Reserved.

Bit 3

Vertical Sync Control:

0 = Vsync output enabled
1 = Vsync output is logical "OR" of vsync and Vertical Display Enable.

Bit (2:0)

Reserved.

9.0 VGA SEQUENCER REGISTERS

PORT	INDEX	NAME
3C4	---	Sequencer Index
3C5	00	Reset
3C5	01	Clocking Mode
3C5	02	Map Mask
3C5	03	Character Map Select
3C5	04	Memory Mode

NOTE
Reserved bits should be set to zero.

9.1 SEQUENCER INDEX REGISTER

Read/Write Port = 3C4h

BIT	FUNCTION
7:5	Reserved
4:0	Sequencer Address/Index Bits

Bits 7:5

Reserved.

Bits 4:0

Sequencer Address/Index. The Sequencer Address Register is written with the index value (00h-04h) of the Sequencer register to be accessed. Sequencer extension registers are also indexed by this register.

13

9.2 RESET REGISTER

Read/Write Port = 3C5h, Index = 00h

BIT	FUNCTION
7:2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

Bit 7:2

Reserved.

Bit 1

Synchronous Reset.

0 = Sequencer is cleared and halted synchronously.
1 = Operational mode (Bit 0 = 1).

Bit 0

Asynchronous Reset.

0 = Sequencer is cleared and halted asynchronously.
1 = Operational mode (Bit 1 = 1).

9.3 CLOCKING MODE REGISTER

Read/Write Port = 3C5h, Index = 01h

BIT	FUNCTION
7:6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load if Bit 4 = 0
1	Reserved
0	8/9 Dot Clocks

Bits 7:6

Reserved.

Bit 5

Screen Off

0 = Normal screen operation.
1 = Screen turned off. SYNC signals are active and this bit may be used for quick full screen updates.

Bit 4

Video Serial Shift Register Loading.

0 = Serial shift registers loaded every character or every other character clock depending on bit 2.
1 = Serial shift registers loaded every 4th character clock (32 bit fetches).

Bit 3

Dot Clock Selection

0 = Normal dot clock selected by VCLK input frequency.
1 = Dot Clock divided by 2 (320/360) pixels).

Bit 2

Shift Load. (Effective only if bit 4 = 0).

0 = Video serializer is loaded every character clock.
1 = Video serializer are loaded every other character clock.

Bit 1

Reserved.

Bit 0

8/9 Dot Clock.

Commands Sequencer to generate 8 or 9 dot wide character clock.

0 = 9 dot wide character clock.
1 = 8 dot wide character clock.

9.4 MAP MASK REGISTER

Read/Write Port 3C5h, Index = 02h

BIT	FUNCTION
7:4	Reserved
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Bit 7:4

Reserved

Bit 3:0

Controls Writing to Memory Maps (0-3) respectively.

0 = Writing to maps (0-3) disallowed.
1 = Maps (0-3) accessible.

9.5 CHARACTER MAP SELECT REGISTER

Read/Write Port = 3C5h, Index = 03h

BIT	FUNCTION
7:6	Reserved
5	Character map Select A Bit 2
4	Character map Select B Bit 2
3	Character map Select A Bit 1
2	Character map Select A Bit 0
1	Character map Select B Bit 1
0	Character map Select B Bit 0

If Sequencer Register 4 bit 1 is 1, then the attribute byte bit 3 in text. modes is redefined to control switching between character sets. A 0 selects character map B. A 1 selects character map A. Character Map selection from either plane 2 or plane 3 is determined by PR2(2), PR2(5) and bit 4 of the attribute code.

Bit 7:6

Reserved.

Bit 5

Character Map A MSB Select.

The Most Significant Bit (MSB) of character map A along with bits 3 and 2, select the location of character map A as shown in the following table:

Bits 532	Map Selected	Font/Plane 2 or 3 Location
000	0	1st 8 Kbyte
001	1	3rd 8 Kbyte
010	2	5th 8 Kbyte
011	3	7th 8 Kbyte
100	4	2nd 8 Kbyte
101	5	4th 8 Kbyte
110	6	6th 8 Kbyte
111	7	8th 8 Kbyte

Bit 4

Character Map B MSB Select.

The MSB of character map B along with bits 1 and 0, select the location of character map B as shown below:

Bits 410	Map Selected	Font/Plane2 or 3 Location
000	0	1st 8 Kbyte
001	1	3rd 8 Kbyte
010	2	5th 8 Kbyte
011	3	7th 8 Kbyte
100	4	2nd 8 Kbyte
101	5	4th 8 Kbyte
110	6	6th 8 Kbyte
111	7	8th 8 Kbyte

Bit 3:2

Character Map Select A.

Refer to bit 5 table.

Bit 1:0

Character Map Select B.

Refer to bit 4 table

9.6 MEMORY MODE REGISTER

Read/Write Port = 3C5h, Index = 04h

Bit 7:4

BIT	FUNCTION
7:4	Reserved
3	Chain 4 mode
2	Odd/Even mode
1	Extended Memory
0	Reserved

Bit 3

Chains 4 Maps.

0 = Processor sequentially accesses data using map mask register.

1 = Directs the two lower order video memory address pins (MA0, MA1) to select the map to be addressed. The map selections are listed in the following table.:

MA1	MA0	MAP SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2

Odd/Even Map Selection.

0 = Even processor addresses to access maps 0 and 2. Odd processor addresses to access maps 1 and 3.

1 = sequential processor access as defined by map mask register.

Bit 1

Extended Video Memory.

0 = 64 KB of video memory.

1 = Greater than 64 KB of memory for VGA/ EGA modes.

Bit 0

Reserved.

10.0 VGA CRT CONTROLLER REGISTERS

10.1 CRT ADDRESS REGISTER

Read/Write Port = 3?4h

BIT	FUNCTION
7:5	Reserved
4:0	Index bits

Bit 7:5

Reserved

Bit 4:0

Index Register Bits.

CRT Controller Index pointer bits to specify the register to be addressed. Its value is programmed in hex.

10.2 HORIZONTAL TOTAL REGISTER

Read/Write Port = 3?5h, Index = 00h

BIT	FUNCTION
7:0	Count Plus Retrace Less 5

Bit 7:0

Count Plus Retrace Less 5.

In VGA mode, the total character count is the total number of characters including retrace time less 5, per horizontal scan line.

10.3 HORIZONTAL DISPLAY ENABLE END REGISTER

Read/Write Port = 3?5h, Index = 01h

Bit 7:0

The total displayed characters less one are programmed in this register. This register is locked if PR3(5) = 1 or the vertical retrace end register bit 7 = 1.

10.4 START HORIZONTAL RETRACE PULSE REGISTER

Read/Write Port = 3?5h, Index = 04h

BIT	FUNCTION
7:0	Start Horizontal Retrace Character Count

Bit 7:0

Start Horizontal Retrace Character Count.

Hex value in character count at which horizontal retrace output pulse becomes active. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1

10.5 END HORIZONTAL RETRACE REGISTER

Read/Write Port = 3?5h, Index = 05h

BIT	FUNCTION
7	End Horizontal Blank bit 6
6:5	Horizontal Retrace Delay
4:0	End Horizontal

This register is locked if PR3 (5) = 1 or Vertical Retrace End Register bit 7 = 1.

Bit 7

MSB (Sixth) Of End Horizontal Blanking Register.

Bit 6:5

Horizontal Retrace Delay.

These bits define horizontal retrace signal delay.

Refer to the following table.:

BIT6	BIT5	CHARACTER CLOCK DELAY
0	0	0
0	1	1
1	0	2
1	1	3

BIT 4:0

End Horizontal Retrace

Start retrace register value is added to the width of the horizontal retrace in character clock count. The least significant five bits are programmed in this register. When the least significant five bits of the Horizontal character counter matches these five bits. the horizontal retrace signal is turned off.

10.6 VERTICAL TOTAL REGISTER

Read/Write Port = 3?5h, Index = 06h

BIT	FUNCTION
7:0	Vertical Total Scan Lines

Bit 7:0

Raster Scan Line Total Less 2.

The least significant eight bits of a eleven bit count of raster scan lines for a display frame. The loaded value includes vertical total scan lines minus 2. Time for vertical retrace, and vertical sync are also included. The bit 8 and bit 9 of this count are loaded into the Vertical Overflow Register (index = 07h) bit 0 and bit 5 respectively. The bit 10 of this count is in the 3?5, index 3E, bit 0. In 6845 modes, total vertical display time in rows is programmed into bit 6-bit 0, while bit 7 is reserved. Scan count reduction is not necessary. (The number of scan lines in a row is determined by the maximum Scan Line Register (index 09h bits 4:0). This register is locked if the PR Register PR3 (0) = 1 or the Vertical Retrace End Register bit 7 = 1.

10.7 OVERFLOW VERTICAL REGISTER

Read/Write Port = 3?5h, Index - 07h

BIT	FUNCTION
7	Vertical Retrace Start Bit 9
6	Vertical Display Enable End Bit 9
5	Vertical Total Bit 9
4	Line Compare Bit 8
3	Start Vertical Blank Bit 8
2	Vertical Retrace Start Bit 8
1	Vertical display Enable End Bit 8
0	Vertical Total Bit 8

Bit 7[1]

Vertical retrace Start Bit 9 (index = 10h).

Bit 6[2]

Vertical Display Enable End Bit 9 (index = 12h)

Bit 5[1]

Vertical total Bit 9 (index = 06h).

Bit 4

Line Compare Bit 8 (index = 18h).

Bit 3[2]

Start Vertical Blank Bit 8 (index = 18h).

Bit 2[2]

Start Vertical Retrace Start Bit 8 (index 10h).

Bit 1[1]

Vertical Total Bit 8 (index = 06h).

NOTES

This register is locked if PR3 (5) = 1
OR the Vertical Retrace End Register bit 7 = 1.

[2]This Register is locked if PR3(1) = 0
AND Vertical Retrace End Register bit 7 = 1.

[1]This register is locked if PR3 (0) = 1 OR
Vertical Retrace End Register bit 7 = 1.

10.8 PRESET ROW SCAN REGISTER

Read/Write Port = 3?5h, Index = 08h

BIT	FUNCTION
7	Reserved
6:5	Byte Panning Control
4:0	Preset Row Scan Count

Bit 7

Reserved.

Bit 6:5

Byte Panning Control.

These bits allow up to 3 byte to be panned in modes programmed as multiple shift modes.

BIT 6	BIT 5	OPERATION
0	0	Normal
0	1	1 byte left shift
1	0	2 bytes left shift
1	1	3 bytes left shift

Bit 4:0

Preset Row Scan count.

These bits preset the vertical row scan counter once after each vertical retrace. This counter is incremented after each horizontal retrace period, until the maximum row scan count is reached. When maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scrolling of text.

10.9 MAXIMUM SCAN LINE REGISTER

Read/Write Port = 3?5h, Index 09h

BIT	FUNCTION
7	200 to 400 Line Conversion
6	Line Compare bit 9
5	Start Vertical Blank bit 9
4:0	Maximum Scan Line

Bit 7

200 to 400 Line conversion.

0= Normal operation.
1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes display 400 scan lines (each line is double scanned).

Bit 6

Line Compare.

Bit 9 of the Line Compare Register (index = 18h).

Bit 5

Start Vertical Blank.

Bit 9 of the Start Vertical Blank Register (index = 15h). This register is locked if the PR Register PR3 (0) = 1.

Bit 4:0

Maximum Scan Line.

Maximum number of scanned lines for each row of characters. The value programmed is the maximum number of scanned rows per character minus 1. In 6845 mode, bits 7:5 are reserved, and bits 4:0 are programmed with the maximum scan line count less 1 for non-interlace mode. Interlaced mode is not supported

13

10.10 CURSOR START REGISTER

Read/Write Port = 3?5h, Index = 0Ah

BIT	FUNCTION
7:6	Reserved
5	Cursor Control
4:0	Cursor Start Scan Line

Bit 7:6

Reserved.

Bit 5

Cursor control.

0 = Cursor on.
1 = Cursor off.

Bit (4:0)

These bits specify the row scan counter value within the character box where the cursor begins. These bits contain the value of the character row less 1. If this value is programmed with a value greater than the Cursor End Register (index = 0Bh), no cursor is generated. For 6845 modes, bit 7 is reserved. Bit 5 controls the cursor operation and bits 4:0 contain the cursor start value. Bit 6 is not used.

10.11 CURSOR END REGISTER

Read/Write Port = 3?5h, Index = 0Bh

BIT	FUNCTION
7	Reserved
6:5	Cursor Skew
4:0	Cursor End Scan Line

Bit 7

Reserved.

Bit 6:5

Cursor Skew Bits.

Delays the displayed cursor to the right by the skew value in character clocks e.g., 1 character clock skew moves the cursor right by 1 position on the screen. Refer to the following table.:

BIT6	BIT5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4:0

these bits specify the last row scan counter value within the character box during which the cursor is active. If this value is less than the cursor start value, no cursor is displayed. In 6845 mode, bits 7:5 are reserved and bits 4:0 contain row value of the cursor end.

NOTE

There are three types of cursors generated, depending upon the mode i.e., EGA, VGA, or 6845 (non-VGA). The above description refers to the VGA cursor only.

10.12 START ADDRESS HIGH REGISTER

Read/Write Port = 3?5h, Index = 0Ch

BIT	FUNCTION
7:0	Start Address High Byte

Bit 7:0

Display Screen Start Address Upper Byte Bits.

Eight high order bits of the 16 bit video memory address, used for screen refresh. The low order eight bit register is at index 0Dh. The PR Register PR3 bits 3 and 4 extend this video memory start register to 18 bits. In 6845 modes bits 6 & 7 are

forced to 0 regardless of this register's contents, while the lower order 8 bits are at index register 0Dh.

10.13 START ADDRESS LOW REGISTER

Read/Write Port = 3?5, Index = 0Dh

BIT	FUNCTION
7:0	Start Address Low Byte

Bit 7:0

The lower order eight bits of the 16 bit video memory address in VGA or 6845 modes.

10.14 CURSOR LOCATION HIGH REGISTER

Read/Write Port = 3?5h, Index = 0Eh

BIT	FUNCTION
7:0	Cursor Location High Byte

Bit 7:0

Cursor Address Upper Byte bits.

The eight higher order bits of 16 bit cursor location in VGA mode. For the lower order eight bits, see the Cursor Location Low Register at index 0Fh. In VGA mode, the PR Register PR3 bits 3 and 4 extend the cursor location High Register to 18 bits. For 6845 modes, bits 6 and 7 are reserved, while bits 5:0 are the high order bits of the cursor.

10.15 CURSOR LOCATION LOW REGISTER

Read/Write Port = 3?5h, Index = 0Fh

BIT	FUNCTION
7:0	Cursor Location Low Byte

Bit 7:0

Cursor Address Lower Byte Bits.

The lower order eight bits of the 16 bit video memory address in VGA or 6845 mode.

10.16 VERTICAL RETRACE START REGISTER

Read/Write Port = 3?5h, Index = 10h

BIT	FUNCTION
7:0	Vertical Retrace Start (lower eight bits)

Bit 7:0

Vertical Retrace Start Pulse Lower Eight Bits.

The lower eight bits of the eleven bit vertical retrace start register. Bits 8 and 9 are located in the Overflow Register (index = 07h). Bit 10 is located in 3?5, index 3E, bit 2. In 6845 compatible mode, this register shows the high order six bits in positions 5:0 as the light pen read back value, and bits 6 and 7 are reserved. The lower order eight bits of the light pen read back register are at the index 11h. In EGA compatible mode this register shows the high order eight bits as the light pen value. This register is locked if PR register PR3 (0) = 1.

10.17 VERTICAL RETRACE END REGISTER

Read/Write Port = 3?5h, Index = 11h

BIT	FUNCTION
7	CRTC 0:7 Write Protect
6	Select 3/5 DRAM Refresh
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
3:0	Vertical Retrace End

This register is locked if the PR Register PR3 (0) = 1.

Bit 7

CRTC Registers Write Protect.

0 = Enables writes to CRT index registers 00h-07h.
1 = Write protects CRT Controller index registers in the range of index 00h-07h. The line compare bit 4 in the Overflow Register (07h) is not protected.

Bit 6

DRAM Refresh/Horizontal Scan Line.

Selects DRAM refresh cycles per horizontal scan line.

0 = Generates 3 refresh cycles for each horizontal scan line for normal VGA operation.
1 = Generates 5 DRAM refresh cycles per horizontal scan line.

Bit 5

Enable Vertical Retrace Interrupt.

0 = Enables vertical retrace interrupt.
1 = Disable vertical retrace interrupt and tristates the IRQ output pin.

Bit 4

Clear Vertical Retrace Interrupt.

0 = Clears vertical retrace interrupt by resetting (writing a 0 to) and internal flip flop.
1 = Vertical retrace interrupt. Allows an interrupt to be generated after the last displayed scan of the frame has occurred (i.e. the start of the bottom border).

Bit 3:0

Vertical Retrace End.

They specify scan count at which vertical sync becomes inactive. For retrace signal pulse width "W", add scan counter for "W" to the value of the Vertical Retrace Start Register. The 4 bit result is written in the Vertical Retrace End Register. In 6845 or EGA compatible mode, this register allows the read back value of the lower eight bits of Light Pen Register.

10.18 VERTICAL DISPLAY ENABLE END REGISTER

Read/Write Port = 3?5h, Index = 12h

BIT	FUNCTION
7:0	Vertical Display Enable End (Lower eight bits)

Bit 7:0

Vertical Display Enable End Loser Eight Bits.

The eight lower bits of this eleven bit register define where the active display frame ends. The programmed count is in scan lines minus 1. Bits 8 and 9 are in the Overflow Register (index 07h) at bit 1 and 6 respectively. Bit 10 is in 3?5, index 3E, bit 10.

10.19 OFFSET REGISTER

Read/Write Port = 3?5h, Index 13h

BIT	FUNCTION
7:0	Logical Line Screen width

Bit 7:0

Logical Line Screen Width.

This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or double word display memory access. It is calculated as follows:

Next Row Scan Start Address = Current Row scan Start Address + (K * Value in Offset Register), where K=2 in byte mode and K=4 in word mode.

10.20 UNDERLINE LOCATION REGISTER

Read/Write Port = 3?5h, Index = 14h

BIT	FUNCTION
7	Reserved
6	Doubleword Mode
5	Count by 4
4:0	Underline Location

Bit 7

Reserved.

Bit 6

Doubleword Mode.

0 = Display memory addressed for byte or word access.
1 = display memory addressed for double word access.

Bit 5

Count By 4 for Double word Access

0 = Memory address counter clocked for byte or word access.
1 = Memory address counter is clocked at the character clock rate divided by 4.

Bit 4:0

Underline Location

These bits specify the row scan counter value within a character matrix where under line is to be displayed. Load a value 1 less than the desired scan line number.

10.21 START VERTICAL BLANK REGISTER

Read/Write Port = 3?5h, Index = 15h

This register is locked if PR3 (0) = 1.

BIT	FUNCTION
7:0	Start Vertical Blank (lower eight bits)

Bit 7:0

Start Vertical Blank Lower Eight Bits.

The lower eight bits of this eleven bit Start Vertical Blank Register. Bit 8 is in the Overflow Register (index = 07h) and bit 9 is in the Maximum Scan Line Register (index = 09h).Bit 10 is in 3?5, index 3E, bit 3. The eleventh bit value is reduced by 1 from the desired scan line count where the vertical blanking signal starts.

10.22 END VERTICAL BLANK REGISTER

Read/Write Port = 3?5h, Index = 16h

This register is locked if the PR Register PR3 (0) = 1.

BIT	FUNCTION
7:0	End Vertical Blank

Bit 7:0

Vertical Blank Inactive Count.

End Vertical is an 8 bit value calculated as follows:

8 bit End Vertical Blank value =

(value of Start Vertical Blank minus 1) + (value of Vertical Blank signal width in scan lines).

10.23 CRT MODE CONTROL REGISTER

Read/Write Port = 3?5h, Index = 17h

This register is locked if PR3 (5) = 1.

BIT	FUNCTION
7	Hardware Reset
6	Word or Byte Mode
5	Address Wrap
4	Reserved
3	Count by 2
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CGA Compatibility

Bit 7

Hardware Reset.

0 = Horizontal and vertical retrace outputs to be inactive.
1 = Horizontal and vertical retrace outputs enabled.

Bit 6

Word Or Byte Mode.

0 = Word address mode. All memory address counter bits shift down by 1 bit and the MSB of the address counter appears on the LSB. Refer to the following table.
1 = Byte address mode.

CRT14h	CRT17h	ADDRESS
Bit 6	Bit6	Mode
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5

Address Wrap.

0 = In word address mode, this bit enables bit 13 to appear at MA0, otherwise bit 0 appears on MAO.
1 = Select MA15 for odd/even mode when 256KB of video memory is used on the system board.

Bit 4

Reserved.

Bit 3

Count by 2

0 = Character clock increments memory address counter.
1 = Character clock divided by 2 increments the address counter.

Bit 2

Horizontal Retrace Clock Rate Select for Vertical Timing Counter.

0 = Selects horizontal retrace clock rate
1 = Selects horizontal retrace clock rate divided by 2.

Bit 1

Select Row Scan Counter.

0 = Selects row scan counter bit 1 as output at MA14 address pin.
1 = Selects bit 14 of the CRTC address counter as output at MA14 pin.

Bit 0

6845 CRT Controller compatibility mode support for CGA operation.

0 = Row scan address bit 0 is substituted for memory address bit 13 at MA13 output pin during active display time.
1 = Enable memory address pin 13 to be output at MA13 address pin.

MEMORY ADDRESS MODE	BYTE ADDRESS MODE	WORD ADDRESS MODE	DOUBLE WORD ADDRESS MODE
MA0/RF0	MA0	*MA15 OR MA13	MA12
MA1/RF1	1	0	MA13
MA2/RF2	2	1	0
MA3/RF3	3	2	1
MA4/RF4	4	3	2
MA5/RF5	5	4	3
MA6/RF6	6	5	4
MA7/RF7	7	6	5
MA8/RF8	8	7	6
MA9	9	8	7
MA10	10	9	8
MA11	11	10	9
MA12	12	11	10
MA13	13	12	11
MA14	14	13	12
MA15	15	14	13

NOTE: * See bit 5, defining address wrap. This table is only applicable when PR Register PR1 bits 7 and 6 equal zero, or PR16 bit 1 equals one. The CRT Underline Location Register (index = 14h) bit 6 also controls addressing. However, when CRT 14h (6) = 0, only the CRT Mode Control Register (index 17h) bit 6 controls addressing.

10.24 LINE COMPARE REGISTER

Read/Write Port = 3?5h, Index = 18h

BIT	FUNCTION
7:0	Line Compare (lower eight bits)

Bit 7:0

Line Compare Lower Eight Bits.

Lower eight bits of the ten bit Scan Line Compare Register. Bit 8 is in the Overflow Register (index = 07h) and bit 9 is in the Maximum Scan Line Register (index = 09h). When the vertical counter reaches this value, the internal start of the line counter is cleared.

13

11.0 GRAPHICS CONTROLLER REGISTERS

See Section 5 for a summary of Graphics Controller registers.

11.1 GRAPHICS INDEX REGISTER

Read/Write Port = 3CEh

BIT	FUNCTION
7:4	Reserved
3:0	Graphics Address Bits

Bit 7:4

Reserved

Bit 3:0

Graphics Controller Register Index Pointer Bits. Note that some of the PR registers reside with the index pointer extension beyond the standard VGA Graphics Controller registers.

11.2 SET/RESET REGISTER

Read/Write Port = 3CFh, Index = 00h

BIT	FUNCTION
7:4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bit 7:4

Reserved.

Bit 3:0

Set/Reset Map.

When the CPU executes display memory write with Write Mode 0* selected and the Enable Set/Reset Register (index = 01h) activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. It is an eight bit fill operation. The map designations are defined in the following list:

0 = Reset.
1 = Set

BIT	SET/RESET
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE

* The selection of Write Mode 0 is determined by the Graphics Mode Register (index = 05h) bit 1 and bit 0.

11.3 ENABLE SET/RESET REGISTER

Read/Write Port = 3CFh, Index = 01h

BIT	FUNCTION
7:4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bit 7:4

Reserved

Bit 3:0

Enable Set/Reset Register (Index 00h)

0 = When Write Mode 0 is selected, these bits, set to 0, disable the Set/Reset Register (index = 00h) memory map access and the map is written with the rotated 8-bit data from the system microprocessor as defined by the Data Rotate Register.

1 = When Write Mode 0 is selected, these bits enable memory map access defined by the Set/Reset Register (index = 00h), and the respective memory map is written with the bit value in the Set/Reset Register (index = 00h).

11.4 COLOR COMPARE REGISTER

Read/Write Port 3CFh, Index = 02h

BIT	FUNCTION
7:4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bit 7:4

Reserved

Bit 3:0

Color Compare.

The color compare bit contains the value to which all 8 bits of the corresponding memory map are compared. This comparison also occurs across all four maps, and a 1 is returned for the map positions where the bits of all four maps equal the Color Compare Register. If a system read is done with bit 3 = 0 for the Graphics Mode Register (index = 05h), data is returned without comparison. Color compare map coding is shown on the next page.

BIT	COLOR COMPARE
3	Map 3
2	Map 2
1	Map 1
0	Map 0

11.5 DATA ROTATE REGISTER

Read/Write Port = 3CFh, Index = 03h

BIT	FUNCTION
7:5	Reserved
4	Function Select 1
3	Function Select 2
2	Rotate Count Bit 2
1	Rotate Count Bit 1
0	Rotate Count Bit 0

Bit 7:5

Reserved

Bit 4:3

Function Select.

Function select for any of the write mode operations defined in the Graphics Mode Register (index = 05h), is defined as follows

:

BIT 4	BIT3	FUNCTION *
0	0	Data unmodified
0	1	Data ANDed with the data the read latches
1	0	Data ORed with the data the read latches
1	1	Data XORed with the data the read latches

NOTES:

* The data refers to CPU data after going through the data rotation.
* The latches contain the memory data from the last memory read.

Bit 2:0

Rotate Count

It specifies number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register (index = 05h)

11.6 READ MAP SELECT REGISTER

Read/Write Port = 3CFh, Index = 04h

BIT	FUNCTION
7:2	Reserved
1	Map Select 1
0	Map Select 0

Bit 7:2

Reserved

Bit 1:0

Map Select.

These bits select Memory Map in memory read operations. It has no effect on the color compare read mode. In odd/even modes, the value can be 00b or 01b to select chained maps 0 & 1 or value 10b or 11b to select the chained maps 2 & 3. Map read is defined as follows:

BIT1	BIT 0	READ MAP
0	0	0
0	1	1
1	0	2
1	1	3

13

11.7 GRAPHICS MODE REGISTER

Read/Write Port = 3CFh, Index = 05h

BIT	FUNCTION
7	Reserved
6	256 Color Mode
5	Shift Register
4	CGA Odd/Even
3	Read Type
2	Reserved
1	Write Mode bit 1
0	Write Mode bit 0

Bit 7

Reserved

Bit 6

256 Color Mode.

0 = Enables bit 5 of this register to control loading of the shift registers. Four bit pixel is expanded to six bits through the internal palette and is sent out on the lower six bits (VID5-VID0) pins every dot clock. The remaining two video outputs (VID6, VID7) are determined by bits 2 and 3 of the Color Select Register located at index = 14h within the Attribute Controller.

1 = Load video shift registers to support 256 color mode.

Bit 5

Shift Register.

Shift Register Load controls the way in which memory data is formatted in the four video shift registers. MSB is shifted out in all cases.

0 = For Map 0-Map 3 data is loaded into the shift register for normal operations.

1 = For CGA graphics mode compatibility, even numbered bits from all the maps are shifted out of even numbered shift registers, odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4

Odd/Even Mode.

0 = normal

1 = CGA compatible odd/even system access mode. Sequential addressing as defined by bit 2 of the sequencer memory mode register (index = 04h). Even system addresses access maps 0 or 2 and odd system addresses access maps 1 or 3.

Bit 3

Read Mode.

0 = System reads data from memory maps selected by Read Map Select Register (index = 04h) This setting has no effect if bit 3 of the Sequencer Memory Mode Register = 1.

1 = System reads the comparison of the memory maps and the Color Compare Register.

Bit 2

Reserved

Bit 1:0

Write Mode.

The following table defines the four write modes.

BIT 0	BIT 1	WRITE MODE
0	0	**Write Mode 0**. If the Set/Reset Register function is enabled for any of the maps, the eight bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data which is right rotated by the number of bits defined in the Data rotate Register, with the old LSB now the new MSB.
0	1	**Write Mode 1**. This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	**Write Mode 2**. Memory maps are filled with the 8 bit value of the corresponding CPU data bits (3:0). The 32 bit output of the four memory maps is then operated on by the Bit Mask Register and the resulting data is written to the four memory maps.
1	1	**Write Mode 3**. Eight bits of the value contained in the Set/Reset Register (index = 00h) is written into the corresponding map, regardless of the Enable Set/Reset Register (index = 01h). The right rotated CPU data (see Write Mode 0) is ANDed with Bit Mask Register data to form an 8-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

11.8 MISCELLANEOUS REGISTER

Read/Write Port = 3CFh, Index = 06h

BIT	FUNCTION
7:4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bit 7:4

Reserved.

Bit 3:2

Memory Map 1,0

Display memory map control into the CPU address space is shown below:

BIT 3	BIT 2	CPU ADDRESS RANGE	LENGTH
0	0	A000:0h	128KB BFFF:Fh
0	1	A000:0h	64KB AFFF:Fh
1	0	B000:0h	32KB B7FF:Fh
1	1	B800:0h	32KB BFFF:Fh

Bit 1

Odd/Even Mode.

0 = CPU address bit A0 is the memory address bit MA0.
1 = CPU address bit A is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects map 0 or 2, while A0 = 1 selects map 1 or 3.

Bit 0

Graphics/Alphanumeric Mode

This bit is programmed the same way as bit 0 of the Attribute Mode Control Register.

0 = Alphanumeric mode selects.
1 = Graphics mode selected.

11.9 COLOR DON'T CARE REGISTER

Read/Write Port 3CFh, Index = 07h

BIT	FUNCTION
7:4	Reserved
3	Memory Map 3
2	Memory Map 2
1	Memory Map 1
0	Memory Map 0

Bit 7:4

Reserved.

Bit 3:0

Memory Map Color Compare Operation.

0 = Disable color compare operation.
1 = Enable color compare operation.

11.10 BIT MASK REGISTER

Read/Write Port = 3CFh, Index = 08h

BIT	FUNCTION
7:0	Bit mask

Bit 7:0

Bit mask operation applies simultaneously to all the four maps. In Write Modes 0 and 2, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation is applicable to any data written by the processor.

0 = Bit position value is masked or is not changeable
1 = Bit position value is unmasked and can be changed in the corresponding map.

12.0 ATTRIBUTE CONTROLLER REGISTERS

Refer to Section 7 for a summary of Attribute Controller registers.

12.1 ATTRIBUTE INDEX REGISTER

Read/Write Port = 3C0h

BIT	FUNCTION
7:6	Reserved
5	Palette Address Source
4:0	Attribute Address Bits

Bit 7:6

Reserved.

Bit 5

Palette Address Source.

0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers (index 00-0Fh).
1 = Enable internal color palette and normal video translation.

Bit 4:0

Attribute Controller Index Register Address Bits

NOTE

The Attribute Index register has an internal flip-flop, rather than an input bit, which controls the selection of the Address and Data Registers. Reading the Input Status Register 1 (port = 3?A) clears the flip-flop and selects the Address Register, which is read through address 3C1 and written at address 3C0. Once the Address Register has been loaded with an index the next write operation to 3C0 loads the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address hex 3C0, but does not toggle for reads to address 3C1.

12.2 PALETTE REGISTERS (00h-0Fh)

Read Port = 3C1h/Write Port = 3C0h

BIT	FUNCTION
7:6	Reserved
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit 7:6

Reserved.

Bit 5:0

Palette Pixel Colors.

They are defined as follows:

0 = Current pixel color deselected.
1 = Enable corresponding pixel color per the following table.

BIT 5	VID5
Bit 4	VID4
Bit 3	VID3
Bit 2	VID2
Bit 1	VID1
Bit 0	VID0

12.3 ATTRIBUTE MODE CONTROL REGISTER

Read Port = 3C1h/Write Port = 3C0h, Index = 10h

BIT	FUNCTION
7	VID5, VID4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved
3	Enable Blink/Select Background Intensity
2	Enable Line Graphics Character Code
1	Mono-Emulation
0	Graphics/Alphanumeric Mode

13

Bit 7

VID5, VID4 Select

0 = VID5 and VID4 palette register outputs are selected.
1 = Color Select Register (index 14h) bits 1 and 0 are selected for outputs at VID5 and VID4 pins.

But 6

Pixel Width

0 = Disable 256 color mode pixel width. The PCLK output is the same as the internal dot clock rate.
1 = Enable pixel width for 256 color mode. The PCLK output is the internal dot clock divided by two.

Bit 5

PEL Panning Compatibility Line Compare in the CRT Controller.

0 = A line compare has no effect on the PEL Panning Register.
1 = Allows a successful line compare to disable the PEL Panning Register and also bits 5 and 6 of the CRT Controller Register 08 until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

BIT 4

Reserved.

Bit 3

Background Intensity/Blink Selection.

0 = Selects background intensity from the MSB of the attribute byte.
1 = Selects blink attribute.

Bit 2

Enable Line Graphics Character Code. Set this bit to zero for character fonts that do not utilize line graphics character codes.

0 = Forces ninth dot to be the same color as background in line graphics character codes.
1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1

Mono/Color Emulation.

0 = Color display attributes.
1 = MDA attributes

Bit 0

Graphics/Alphanumeric Mode Enable.

0 = Alphanumeric mode.
1 = Graphics mode.

12.4 OVERSCAN COLOR REGISTER

Read Port = 3C1h/Write Port = 3C0h,

Index = 11h

BIT	FUNCTION
7	VID7
6	VID6
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit 7:0

Overscan/Border Color.

They determine the overscan of order color. For Monochrome display, this register is set to 0. Border colors are set as shown above.

12.5 COLOR PLANE ENABLE REGISTER

Read Port = 3C1h/Write Port = 3C0h, Index 12h

BIT	FUNCTION
7:6	Reserved
5	Video Status MUX1
4	Video Status MUX0
3:0	Enable Color Plane

Bit 7:6

Reserved.

Bit 5:4

Video Status Control.

These bits select 2 out of 8 color outputs which can be read by the Input Status Register 1 (port = 03?A) bits 4 and 5.

COLOR PLANE		INPUT STATUS REGISTER	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID 2	VID 0
0	1	VID 5	VID 4
1	0	VID 3	VID 1
1	1	VID 7	VID 6

Bit 3:0

Color Plane Enable.

0 = Disables respective color planes. Forces pixel bit to 0 before it addresses palette.
1 = Enables the respective display memory color plane.

12.6 HORIZONTAL PEL PANNING REGISTER

Read Port = 3C1h/Write Port = 3C0h, Index = 13h

BIT	FUNCTION
7:4	Reserved
3:0	Horizontal PEL Panning

Bit 7:4

Reserved

Bit 3:0

Horizontal pixel Panning.

It is available in text or graphics modes. These bits select pixel shift to the left horizontally. For 9 dots/character modes, up to 8 pixels can be shifted horizontally to the left. Likewise, for 8 dots/character up to 7 pixels can be shifted horizontally to the left. For 256 color, up to a 3 position pixel shift can occur. The following table defines the shift in different modes.

LEFT SHIFT PIXEL VALUE			
Register	9 Dots	8 Dots	256
Value	Char-acter	Char-acter	Color Mode
0	1	0	0
1	2	1	---
2	3	2	1
3	4	3	---
4	5	4	2
5	6	5	---
6	7	6	3
7	8	7	---
8	0	---	---

13

12.7 COLOR SELECT REGISTER

Read Port = 3C1h/Write Port = 3C0h,

Index = 14h

BIT	FUNCTION
7:4	Reserved
3	S_Color 7
2	S_Color 6
1	S_Color 5
0	S_Color 4

Bit 7:4

Reserved.

Bit 3:2

Color Value MSB

Two most significant bits of the eight digit color value for the video DAC. They are normally used in all modes except 256 color graphics.

Bit 3 = Set color bit VID 7.

Bit 2 = Set color bit VID 6.

Bit (1:0)

Substituted Color Value Bits.

These bits can be substituted for VID 5 and VID 4 output by the Attribute Controller palette registers, to create eight bit color value. They are selected by the Attribute Controller Mode Control Register (index = 10h).

13.0 REGULAR PARADISE REGISTERS

A summary of Paradise Registers is provided in Section 7.

13.1 ADDRESS OFFSET REGISTERS PR0(A) and PR0(B)

PR0(A) - Address Offset Register A
Read/Write Port = 3CFh, Index = 09h

BIT	FUNCTION
7:0	Primary Address Offset bits

PR0(B) - Address Offset Register B

Read/Write Port = 3CFh, Index = 0Ah

BIT	FUNCTION
7:0	Alternate Address Offset bits

The WD90C24 can control up to 1 Mbytes of display memory. However, DOS only assigns 128 Kbytes total memory space for display memory, which starts at A0000h and ends at BFFFFh. To help VGA to reach the memory beyond this range, the WD90C24 has two CPU address offset registers PR0(A) and PR0(B) which can be used to support more than 128 Kbytes of linear display memory address space.

The contents of PR0(A) (bit 6:0) or PR0(B) (bit 6:0) are always added to the CPU address A(19:12) before they are translated to display memory address. This can be thought of as segment register DS and ES in the 8088/80X86 architecture, PR0(A) and PR0(B) then provides a 4 Kbyte segment of the display memory. (Increment PR0(A) or PR0(B) by one equivalents to a jump from a 4 Kbyte segment to another 4 Kbyte segment of the display memory.)

PR0(A) and PR0(B) are all set to zero value at Power on Reset. There are two ways to control whether PR0(A) or PR0(B) gets added into the CPU address.

- Sequencer extension register 3C5h (index 11) bit 7 = 0.

Case 1: PR1 bit 3 = 0, Then PR0(A) is always selected as the CPU address offset Register.

Case 2: PR1 bit 3 = 1; depending on memory mapping, if the display memory is mapped into A0000h - BFFFFh (128K bytes), the PR0(A) offset CPU address range from B0000h - BFFFFh, and the PR0(B) offset CPU address range from A0000h - AFFFFh. (CPU address A16 = 1, selects PR0(A). Otherwise PR0(B) is selected)

If the display memory is mapped into A0000h - AFFFFh (64KB) or B0000h - B7FFFh or B8000h - BFFFFh (32KB), then PROB offset CPU address range from A0000h - A7FFFh or B0000h - B7FFFh. The PROA offset CPU address range from A8000h - AFFFFh or B8000h - BFFFFh. (CPU address A15 = 1, selects PR0(A). Otherwise PR0(B) is selected)

- Sequencer extension register 3C5h (index 11) bit 7 = 1.

Both PR0(A) and PR0(B) are enabled, A CPU memory write selects PR0(B) as the offset register. Otherwise, PR0(A) is selected as the offset register.

13.2 PR1 - MEMORY SIZE

Read/Write Port = 3CFh, Index = 0Bh

BIT	FUNCTION
7:6	Memory Size Select
5:4	Memory Mapping
3	Enable Alternate address Offset Register PR0(B)
2	16-Bit Video Memory
1	16-Bit BIOS ROM
0	BIOS ROM Map Out

This register is 8 bits wide. Bits PR1 (1:0) are latched internally at power on reset from the corresponding memory data bus pins MD(10:0), using either pull-up or pull-down external resisters. Pull-up resistors on MD(10:0) cause PR1(1:0) bits to be latched low.

Bit 7:6

Memory Size.

These two bits control memory size and memory organization. They both must be set to reflect the amount of memory installed. These bits in conjunction with PR0(A), PR0(B), PR16 (1) select the way memory is mapped into the CPU address space. If PR16 (1) is set to 1, the IBM compatible memory mapping is selected regardless of PR1 (7), or PR1 (6).

The following tables list the different settings on these two bits for different memory organizations.

Also, refer to the notes following the tables

13

PR1(7) = 0, PR1(6) = 0

VIDEO RAM ADDRESS BIT	BYTE		WORD		DOUBLE WORD	
	CPU	CRT	CPU	CRT	CPU	CRT

TABLE 13-1 IBM COMPATIBLE MEMORY ORGANIZATION - 256K TOTAL

PR1(7) = 0, PR1 (6) = 1

VIDEO RAM ADDRESS BIT	BYTE		WORD		DOUBLE WORD	
	CPU	CRT	CPU	CRT	CPU	CRT

TABLE 13-2 64K/PLANE WD90C24 MEMORY ORGANIZATION - 256K TOTAL

PR1(7) = 1, PR1(6) = 0, 512

VIDEO RAM ADDRESS BIT	BYTE		WORD		DOUBLE WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
ADDR BIT	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	PA	PA	PA	PA	PA	PA
MA(16)	A(16)	CA(16)	A(17)	CA(16)	A(18)	CA(16)
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
----	----	----	----	----	----	----
----	----	----	----	----	----	----
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16) or (3) XRN5	CA(15)	A(16	CA(14)

TABLE 13-3 128K PLANE WD9030 MEMORY ORGANIZATION - 1M TOTAL

PR1(7) = 1, PR1(6) = 1,

VIDEO RAM ADDR BIT	BYTE		WORD		DOUBLE WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	A(17)	CA(17)	A(17)	CA(16)	A(17	CA(15)
MA(16)	A(16)	CA(16)	A(16)	CA(15)	A(16)	CA(14)
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
MA(13)	A(13)	CA(13)	A(13)	CA(12)	A(13)	CA(11)
----	----	----	----	----	----	----
----	----	----	----	----	----	----
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(2)	A(1)	CA(1)	A(1)	CA(0)	A(19)	CA(17)
MA(0)	A(0)	CA(0)	A(16) or (3) XRN(5)	CA(15)	A(18)	CA(16)

TABLE 13-4 256K PLANE MEMORY ORGANIZATION -1M TOTAL

13

NOTES

1. A(19:0) are WD90C24 internally modified system Addresses.(CPU address + offset address).
2. CA(17:0) are CRT Controller Character Address Counter Bits.
3. XRN(5) is Miscellaneous Output Register 3C2h, inverted bit 5. XRN(5) can be used to replace CPU address bits to select memory pages in word mode.In IBM compatible memory mapping, 3C5.4 bit 1 = 1 selects XRN(5) to replace CPU address bits. In other memory mapping schemes (PR1(7,6) ≠ 00, 3C5.4 bit 1 = 1 and PR16_2 = 1 selects XRN(5) to replace address bits.
4. CA(15) is selected as MA(15) if CRTC Mode Register 17 bit 5 = 1 in word addressing modes.
5. PA is the memory plane select bit when DRAM interface is set for 16 bits.

   PA = 0 select Plane 1, 0

   PA = 1 select Plane 2,3
6. MA 17-MA0 are divided into RAS, CAS addresses as follows:

For 256K x 16 DRAM	MA(16)-MA(8)	⇒ RAS(8)-RAS(0)
	MA17, MA(7)-MA(0)	⇒ CAS(8)-CAS(0)
For 64K x 16 DRAM	MA(15)-MA(8)	⇒ RAS(7)-RAS(0)
	MA(7)-MA(0)	⇒ CAS(7)-CAS(0)

MA(17,16) =	00	Select 1st	64K bank
	01	Select 2nd	64K bank
	10	Select 3rd	64K bank
	11	Select 4th	64K bank

Bits 5:4

PR1(5,4)

Memory Map Select

BIT 5	BIT 4	FUNCTION
0	0	IBM VGA Mapping, CPU addresses are decoded from 0A0000h-0BFFFFh from the lowest 1M byte CPU address space, (depending on 3CF.06 bits 2, & 3)
0	1	1st 256K byte in any 1M byte CPU addressing space, X00000h-X3FFFFh
1	0	1st 512K byte in any 1M byte CPU addressing space, X00000h-X7FFFFh)
1	1	In any 1M byte CPU address space, X00000h-XFFFFFh

* PR34(3C5.14) bits 3:0 controls which 1M byte of CPU address space the WD90C24 is mapped to.

Bit 3

Enable Alternate Address Offset Register PR0(B)

Bit 2

Enable 16 bit CPU interface for Video Memory

When set to 1, $\overline{\text{MEMCS16}}$ is active low for all of the video memory cycles.

Bit 1

When set to 1, the BIOS ROM has a 16 bit data path ($\overline{\text{ROM16}}$ responds to ROM access). Otherwise, the BIOS ROM has an 8 bit data path.

A pull down resistor on MD (10) sets this bit to 1 after power-on reset. This bit can be set to 1 by an I/O write cycle only if CNF(1) = 1.

Bit 0

If set to 1 the BIOS ROM is mapped out. A pull-down resistor on MD(0) sets this bit to a 1 at power on reset.

13.3 PR2 - VIDEO SELECT REGISTER

Read/Write Port = 3CFh, Index = 0Ch

BIT	FUNCTION
7	AT&T/M24 Mode Enable
6	6845 Compatibility
5	Character Map Select
4:3	Character Clock Period Control
2	Underline/Character Map
1	Reserved
0	Force VCLK (overrides SEQ1 bit 3)

Bit 7

Enable AT&T/M24 Register & mode.

Bit 6

0 = VGA or EGA mode.
1 = NON-VGA (6845) mode.

Bit 5

Character Map Select. The following functions are overridden by setting PR15 (2). This bit in conjunction with PR2 (2) and bit 3 of the attribute code, enables character maps from planes 2 or 3 to be selected per the following table.

PR2(5)	PR2 (2)	ATT (4)	PLANE SELECT
0	0	X	2
0	1	X	2
1	0	X	3
1	1	0	2
1	1	1	3

13

NOTE

Selecting page mode addressing (setting PR15 register bit 2 to 1) overrides the plane selected in the previous table.

Bit 4:3

Character clock period control

BIT4	BIT3	FUNCTION
0	0	IBM VGA Character Clock (8 or 9 dots)
0	1	7 dots (used for 132 character mode)
1	0	9 dots
1	1	6 dots if PR17(5) = 0 10 dots if PR17(5) = 1

NOTE

The character clock period control functions have no effect in graphics modes (Graphics mode always uses eight dots).

Bit 2

Underline and Character Map Select. Setting this bit to 1 enables underline for all odd values of attribute codes, e.g. Programming 1 gives blue underline. It overrides the background color function of the attribute code bit 3, which is forced to 0. Therefore, only eight choices of background colors are selectable. This function allows trading background colors for more character maps. In conjunction with PR2 (5), this bit is also decoded to enable character maps from planes 2 or 3. See PR2 (5) for details.

Bit 1

Reserved

Bit 0

Forces horizontal sync timing clock of the CRTC to VCLK.

Uses VCLK when sequencer register 1 bit 3 is set for VCLK/2. This is for compatibility modes that require locking the CRTC timing parameters.

13.4 PR3 - CRT LOCK CONTROL REGISTER

Read/Write Port = 3CFh, Index = 0Dh

BIT	FUNCTION
7	Lock VSYNC Polarity
6	Lock HSYNC Polarity
5	Lock Horizontal Timing
4	Bit 9 Control
3	Bit 8 Control
2	CRT Control
1	Lock Prevention
0	Lock Vertical Timing

Bit 7

Lock VSYNC polarity, as programmed in 3C2 bit 7

Bit 6

Lock HSYNC polarity, as programmed in 3C2 bit 6

Bit 5

Lock Horizontal Timing.

Locks CRTC registers of Group 0 and 4. Prevents attempts by applications software to unlock Group 0 registers by setting 3?5.11h bit 7 = 0.

Bit 4

Bit 9 of CRT Controller Start Memory Address High Register 3?5.0Ch, and bit 9 of Cursor Location High 3?5.0Eh. This bit corresponds to Character Address CA(17h).

Bit 3

Bit 8 of CRT Controller Start Memory Address High Register 3?5.0Ch, and bit 8 of Cursor Location High 3?5.0Eh. This bit corresponds to Character Address CA (16h).

Bit 2

Cursor Start, Stop, Preset Row Scan, and Maximum Scan Line Address registers values multiplied by two.

Bit 1

Lock Prevention.

1 = Prevents attempts by applications software to lock registers of Group 1 by its setting 3?5.11 bit 7 = 1.

Bit 0

Lock vertical timing. 1 = Locks CRTC registers of Groups 2 and 3. Overrides attempts by applications software to unlock Group 2 registers by its setting 3?5.11 bit 7 = 0.

13.4.1 CRT Controller Register Locking

Register locking is controlled by 4 bits. They are PR3 (5, 1, 0) and 3?5.11 (7) (i.e. IBM Vertical Retrace End Register bit 7 controlled by index register 11). When 3?5.11 bit 7 is 1, CRT controller registers (R0-R7) are write protected per VGA definition. For more information on the five groups, and their locking schemes, refer to the sections below.

- **Group 0**

  These registers are locked if PR3 (5) = 1 OR 3?5.11(7) = 1.

  3?5 index 00 --- Horizontal Total Characters per scan.
  3?5 index 01 --- Horizontal Display Enable End.
  3?5 index 01 --- Start Horizontal Blanking
  3?5 index 03 --- End Horizontal Blanking
  3?5 index 04 -- Start Horizontal Retrace
  3?5 index 05 --- End Horizontal Retrace

- **Group 1**

  These registers are locked if PR3 (1) = 0 AND 3?5.11 (7) = 1.

  3?5 index 07 (Bit 6) - Vertical Display Enable End bit 9
  3?5 index 07 (Bit 1) - Vertical Display Enable End Bit 8
  3?5 index 3E (Bit 1) - Vertical Display Enable End bit 10

- **Group 2**

  These registers are locked if PR3 (1) = 0 OR 3?5.11 (7) =1

  3?5 index 06 -- Vertical total
  3?5 index 07 (Bit 7) - Vertical Retrace Start bit 9
  3?5 index 07 (bit 5) - Vertical Total bit 9
  3?5 index 07 (bit 3) - Start Vertical Blank bit 8
  3?5 index 07 (bit 2) - Vertical Retrace Start bit 8
  3?5 index 07 (bit 0) - Vertical Total bit 8
  3?5 index 09 (bit 5) - Start Vertical Blank bit 9
  3?5 index 3E (bit 0) vertical total bit 10
  3?5 index 3E (bit 2) Vertical Retrace Start bit 10
  3?5 index 3E (bit3) Start Vertical Blank bit 10

- **Group 3**

  These registers are locked if PR3 (0) = 1

  3?5 index 10 - Vertical Retrace Start
  3?5 index 11 - [(bits 3:0)] - Vertical Retrace End
  3?5 index 15 - Start Vertical Blanking
  3?5 index 16 - End Vertical Blanking

- **Group 4**

  This register is locked if PR3 (5) = 1

- CRTC mode control register 17 (bit 2) - Selects divide by two vertical timing

13.5 PR4 - VIDEO CONTROL REGISTER

Read/Write Port = 3CFh, Index = 0Eh

The video monitor output control register (PR4) can be programmed to tri-state the CRT display control outputs as well as video data for the RAMDAC, and memory control outputs.

BIT	FUNCTION
7	$\overline{\text{BLNK}}$ / Display Enable
6	PCLK = VCLK
5	Tri-state Video Outputs
4	Tri-state Memory Control Outputs
3	Override CGA Enable Video bit
2	Lock Internal Palette and Overscan Registers
1	EGA Compatibility
0	Ext 256 color Shift Register control

13

Bit 7

This bit controls the output signal $\overline{BLNK}$. Normally in the VGA mode, $\overline{BLNK}$ is used by the external video DAC to generate blanking. If this bit = 1, the $\overline{BLNK}$ output supplies a display enable signal. A choice of two types of display enable timings can be selected, and is determined by PR15 (1).

Bit 6

Select PCLK equal to VCLK.

0 = PCLK is the inverted internal video dot clock, or half the dot clock frequency, depending upon the video mode.
1 = PCLK is always the non-inverted VCLK input clock.

Bit 5

Tri-state the outputs VID7-VID0, HSYNC, VSYNC, and $\overline{BLNK}$.

Bit 4

Tri-state the memory control outputs. The memory address bus MA(8:0), and all ten DRAM control signals are tri-stated when this bit is set to 1

Bit 3

Overrides the CGA "enable video" bit 3 of mode register 3D8, only in 80 x 25 alpha CGA (Non-VGA) mode. Override effectively forces this bit to 1. Power-on-reset causes no override.

Bit 2

Set to 1 to lock Internal palette and overscan registers.

Bit 1

EGA compatibility bit where 1 = EGA Compatible Mode. It disables reads to all registers which are write-only registers in the IBM EGA. Also, registers at 3C0/3C1 change to write-only mode if the EGA compatibility bit is set. In addition to selecting EGA compatibility bit, setting this bit to 1, disables reading PR0 - PR5, In VGA mode (PR(4) bit 1 is zero) 3C0 register is read/write while 3C1 register is read only, per the Attribute Controller registers definitions.

Bit 0

Extended Shift Register Control

These bits should be set to one for extended 256 color modes (IBM mode 13 is not included).

13.6 PR5 - GENERAL PURPOSE STATUS BITS/ UNLOCK PR0 THROUGH PR4

Read/Write Port = 3CFh, Index = 0Fh

BIT	FUNCTION
7	Read CNF (7) Status
6	Read CNF (6) Status
5	Read CNF (5) Status
4	Read CNF (4) Status
3	Read CNF (8) Status
2	PR0-PR4 Unlock
1	PR0-PR4 Unlock
0	PR0-PR4 Unlock

Bits (2:0) are READ/WRITE bits and cleared to 0 by reset. This provides lock or unlock capability for PR registers PR0 through PR4. The PR0-PR4 registers are unlocked when "X5h" is written to PR5. They remain unlocked until any other value is written to PR5. This register also provides readable status for the configuration register bits 4 through 8. Setting PR(4) bit 1 to 1, read protects registers PR0-PR5.

Bit 7 Read CNF (7) [READ ONLY]
Bit 6 Read CNF (6) [READ ONLY]
Bit 5 Read CNF (5) [READ ONLY]
Bit 4 Read CNF (4) [READ ONLY]
Bit 3 Read CNF (8) [READ ONLY]

Bits 2:0

READ/WRITE bits are cleared to 0 by reset. They control writing to PR registers PR0-PR4 as follows:

210 PR0-PR4
0XX Write Protected
X1X Write Protected
XX0 Write Protected
101 Write enable

13.7 PR10 UNLOCK PR11 - PR1A

Read/Write Port = 3?5h, Index = 29h

This register is READ/WRITE and cleared to 0 by reset. PR10 can be loaded if it contains XXXXX101, and can only be read if it has 1XXX0XXX. Bits (7,3), Bits (6:4), and Bits (2:0) control access to PR registers PR10 through PR1A. Bits 7 and 3 enable register read operation for PR10 through PR1A. Bits (6:4) may be used as scratch pad. Bits (2:0) enable register write operations for PR11-PR17.

BIT	FUNCTION
7	PR10-PR1A - Read Enable Bit 1
6:4	PR10 (6:4) - Scratch Pad
3	PR10-PR1A - Read Enable Bit 0
2:0	PR11 - PR1A - Write Enable

Bit 7	Bit 3	PR10 - PR17
0	X	Read Protected, read back data FFh
X	1	Read protected, read back data FFh
1	0	Read Enabled

Bit 2	Bit 1	Bit 0	PR11 - PR17
0	X	X	Write protected
X	1	X	Write protected
X	X	0	Write protected
1	0	1	Write enabled

Bit 6	Bit 5	Bit 4	PR10 (6:4)
0	X	X	Scratch Pad
X	1	X	Scratch Pad
X	X	0	Scratch Pad
1	0	1	Reserved for manufacturing test.

13.8 PR11 EGA SWITCHES

Read/Write Port = 3?5h, Index = 2Ah

The EGA switch configuration details are stored in the PR11 register bits.

BIT	FUNCTION
7	EGASW4
6	EGASW3
5	EGASW2
4	EGASW1
3	EGA Emulation on Analog Display
2	Lock Clock Select
1	Lock Graphics and Sequencer Screen Control
0	Lock 8/9 Character Clock

Bits 7:4

EGA Configuration Switches SW4-SW1.

These bits are READ/WRITE and latched internally at power-on-reset from corresponding memory data bus pins MD(15:12), provided with either pull-up or pull-down external resistors. PULLING UP MD(15:12) causes PR11(7:4) to be latch HIGH. These bits can be read as bit 4 of port 3C2 if the EGA COMPATIBILITY BIT [PR4 (1)] has been set to 1. Selection of the bit to be read is determined by bits 3 & 2 of the Miscellaneous Output Register 3C2, as follows:

WRITE		READ
3C2 bit 3	3C2 bit 2	3C2 bit 4
0	0	PR11 (7) [=EGA SW4]
0	1	PR11 (6) [=EGA SW3]
1	0	PR11 (5) [=EGA SW2]
1	1	PR11 (4) [=EGA SW1]

PR11 Bits 3 through 0 are READ/WRITE and cleared to 0 at power on reset.

Bit 3

Select EGA emulation on a PS/2 (VGA-compatible, analog) display.

Bit 2

Lock Clock Select. This bit locks the internal video clock select multiplexer and disables loading of an external clock chip through VCLK1.

Bit 1

Lock Graphics Controller/Sequencer screen control. Setting PR11(1) to 1 prevents modification of the following bits in the Graphics controller as well as the Sequencer:

Graphics controller	3CF.05 bits (6:5)
Sequencer	3C5.01 bits (5:2)
Sequencer	3C5.03 bits (5:0)

Although the internal functions selected by these graphics controller and sequencer bits are locked by setting PR11 bit 1 to 1, they appear unlocked to the system processor during read operation.

Bit 0

Lock 8/9 dots. Setting this bit to 1 prevents modification of clocking mode sequencer register 3C5.01 bit 0. Although 8 or 9 character timing is locked by setting PR11 bit 0 to 1, the 3C5.01 bit 0 appears unlocked to the system processor during reads.

13.9 PR12 SCRATCH PAD

Read/Write Port = 3?5h, Index = 2Bh

BIT	FUNCTION
7:0	Scratch Pad Bits 7:0

The data in this register is unaffected by hardware reset and undefined at power up.

13.10 PR13 INTERLACE H/2 START

Read/Write port = 3?5h, Index = 2Ch

BIT	FUNCTION
7:0	Interlaced H/2 Start

The data in this register is unaffected by hardware reset and undefined at power up. This register defines the starting horizontal character count at which vertical timing is clocked on alternate fields in interlaced operation. Interlaced operation is enabled by setting PR14(5) to 1. All other standard non-interlaced modes are unaffected by the contents of this register. This register must be programmed into the Horizontal Retrace Start Register (3?5.04h) and Horizontal Total Register (3?5.00h):

PR13(7:0) = [HORIZONTAL RETRACE START] - [(HORIZONTAL TOTAL + 5)/2] + HRD

NOTE

In the above expression, HRD = Horizontal Retrace Delay, determined by bits 6 and 5 of the Horizontal Retrace End Register (3?5.05).

13.11 PR14 INTERLACE H/2 END

Read/Write Port = 3?5h, Index = 2Dh

Bits 4 through 0 are unaffected by hardware reset and undefined at power up. Bits 7 through 5 are cleared to 0 by reset.

BIT	FUNCTION
7	Enable IRQ
6	Vertical Double Scan for EGA on PS/2 Display
5	Enable Interlaced Mode
4:0	Interlaced H/2 End

Bit 7

Enable IRQ. This bit may be set to enable CRT interrupts to be generated when configured for AT BUS operation, allowing EGA compatibility support for interrupt-driven EGA applications. For VGA operation with an AT BUS, interrupts are not used, and this bit should be set to 0. This bit should not be set to 1 in Micro Channel operation.

Bit 6

Vertical Double Scan. This bit should be set to 1 when emulating EGA on PS/2 display. Setting this bit to 1 causes the CRTC's Vertical Displayed line counter and Row Scan counter to be clocked by divide-by-two horizontal timing if vertical sync polarity (3C2 bit 7 = 0) is programmed to be positive. Therefore, the relationship between the actual number of line displayed [N] and the data [n] programmed in to the Vertical Display Enable End register is:

N = 2(n + 1)

Likewise, the relationship between the actual number of scan lines per character row [N] and the data [n] programmed in the maximum Scan Line register holds true.

Bit 5

Interlaced mode.

Setting this bit to 1 selects interlaced mode. The interlaced mode can be used in those video modes in which the data programmed into the Maximum Scan Line Address register [3?5.09] = 0XX00000.

Line compare and double scan are not supported.

Bits (4:0)

Interlaced H/2 end bits (4:0). Add the contents of the Interlaced H/2 Start Register PR(13) to the horizontal sync width (same as defined by 3X5.04,05). Program 5 LSB of the sum into these bit locations.

13.12 PR15 MISCELLANEOUS CONTROL 1

Read/Write Port = 3?5h, Index = 2Eh

BIT	FUNCTION
7	Read 46E8 Enable
6	High VCLK
5	Reserved
4	VCLK = MCLK
3	8514/A Interlaced Compatibility
2	Enable Page Mode
1	Select Display Enable
0	Disable Border

Bit 7

Enable Reading Port 46E8h. This bit is functional only if AT BUS architecture [CNF (2) = 1] is selected. Setting this bit to 1 enables I/O port 46E8h to be read, regardless of the state of its own bits 3 and 4 of port 102 bit 0 (sleep bit). Only bits (4:0) of port 46E8h are readable; bits (7:5) are 0.

Bit 6

Setting this bit to 1 adjusts the memory timing to allow use of a video clock (VCLK) frequency which is much higher than the memory clock (MCLK) frequency. This bit should be set to 1 if (MCLK in MHz) / VCLK in MHz) = 1.5

This bit also should be set to 1 in all extended 256 color modes.

13

Bit 5

Reserved

Bit 4

Select MCLK as video clock. Setting this bit to 1 causes the MCLK input to be selected for the source of all video timing. The other three VCLK inputs can not be selected when this bit is set.

Bit 3

Interlaced Compatibility. This bit should be used only if interlaced mode is selected (see PR14). This bit should be set to 1 if exact timing emulation of the IBM 8514/A's interlaced video timing is required. Setting this bit to 1 causes vertical sync to be generated form the trailing edge of non-skewed horizontal sync. Instead of leading edge, as generated for VGA timing. Setting this bit to 1 also removes two VCLK delays from the default VGA video dot path delay chain.

Bit 2

Select Page Mode Addressing. Setting this bit to 1 forces screen refresh memory read cycles to use page mode addressing in alpha modes. Page mode addressing is automatically used in the graphics modes. Page mode addressing requires less time than RAS-CAS addressing; therefore, selecting page mode addressing increases the bandwidth for the CPU to access video memory by 30-40%. Set this bit to 1 if 132 character mode timing is selected (see description of PR (2). Setting this bit to one in any alpha mode overrides the character map select functions of PR2 (2) and PR2 (5). When this bit is set to 1, it redefines the Character Map Select Register (3C4.03). One of eight, 8K memory segments containing a pair of maps in Plane 2 or Plane 3 is addressed by bits (2:0) of this register while the map selection is determined by the bits (4:3). A pair of adjacent 8K character maps in planes 2 and 3, (adjacent in the sense that they have the same addressing) may be selected by bit 3 of the attribute code.

The character attribute bit 3, in conjunction with bits 3 and 4 of the Character Map Select register (3C5.03), determine a character map from either Plane 2 or Plane 3 as shown by the following table:

3C5.03 BIT 4	3C5.03 BIT 3	ATT BIT 3	PLANE SELECT
0	0	X	2
1	1	X	3
1	0	0	2
1	0	1	3
0	1	0	3
0	1	1	2

NOTE

The above Character Map Select functions override the functions of PR2 register bit 5.

This bit must be set to 1 before loading the character maps in the video DRAM, because the addressing of the page mode character maps differs from the addressing of the default, non-page mode. However, setting this bit to 1 internally redirects all necessary addressing to make loading the character maps the same, whether in page mode or non-page mode.

Bit 1

Display Enable Timing Select. This bit is used to select between two types of display enable timings available at output pin BLNKN if PR4 (7) = 1. If PR4 (7) = 0, this bit has no effect.

0 = BLNKN supplies Pre-Display enable. Pre-Display Enable timing precedes active video by one dot clock.

1 = BLNKN supplies Display Enable. The display enable timing coincides with active video timing.

Bit 0

Disable border. Setting this bit to 1 forces the video outputs to 0 during the interval when border (overscan) color would be active.

13.13 PR16 MISCELLANEOUS CONTROL 2

Read/Write Port = 3?5h, Index = 2Fh

BIT	FUNCTION
7	External register 46E8h lock
6	CRTC Address Count Width bit 1
5	CRTC Address Count Width bit 0
4	CRTC Address Counter Offset bit 1
3	CRTC Address Counter Offset bit 0
2	Enable Odd/Even Page bit
1	VGA Mapping Enable
0	Lock RAMDAC Write Strobe

Bit 7

Lock External 46Eh register.

Setting this bit to 1 causes $\overline{\text{EBROM}}$ output to be forced high (inactive) during I/O writes to port 46E8h. This bit has no effect on loading the internal port 46E8h.

Bits 6:5

CRTC Address Counter Width.

Power on reset clears these bits to 0. These two bits determine the modulus of the CRT controller's address counter, allowing its count width to be limited to 64K or 128K locations (Byte, Word, Double Word). These bits may be used in virtual VGA applications containing 512KB or 1024KB of video memory in which CRT controller is limited to only 64K or 128K locations. Bit PR16 (6) should be set to 1 to ensure VGA and EGA compatible operation of the address counter, limited to 64K locations. The following table lists the appropriate bit settings.

PR16 (6)	PR16 (5)	COUNT WIDTH
0	0	256KB
0	1	128KB
1	X	64KB

Bit 4:3

CRTC Address Counter Offset

Bits 4 and 3 are summed with the CRT Controller's Address Counter bits CA(17) and CA(16), respectively, and the 2-bit result defines the starting location of the displayed video buffer at one of the four 64K boundaries.

Bit 2

Enable Page Bit for Odd/Even

This bit affects addressing of memory by the system processor, if chain 2 (Odd/Even) has been selected by setting 3CF.06 (1) to 1, setting 3C5.04 (3) to 0 to deselect chain 4 addressing. It enables the "Page Bit for Odd/Even" [3C2 (5)] to select between two pages of memory, by controlling video RAM address 0, regardless of the Memory Size bits PR1 (7:6).

Bit 1

VGA Memory Mapping

1 = Selects 256KB IBM VGA Mapping, regardless of the Memory Size bits PR1 (7:6).

Bit 0

Lock RAMDAC write strobe (3C6h - 3C9h)

0 = Normal operation
1 = Output WPLTN to be forced to 1 disabling I/O writes to the video DAC registers. The DAC state register, located inside the WD90C24 is also protected from the modification but may still be read at the port 3C7h.

13.14 PR17 MISCELLANEOUS CONTROL 3

Read/Write Port = 3?5h, Index = 30h

BIT	FUNCTION
7:6	Reserved
5	Character clock period select
4	Reserved
3	Map out 4 K of BIOS ROM
2	Enable 64K BIOS ROM
1	Hercules Compatibility
0	Map out 2 K of BIOS ROM

Bit 7:6

Reserved

Bit 5

Character clock period select. When PR2 (3CF.0C) bits 4:3 = 11, then setting this bit to 0 selects the 6 dot font. Setting this bit to 1, selects the 10 dot font. Otherwise this bit has no effect.

Bit 4

Reserved

Bit 3

Map out 4K of BIOS ROM.

Setting this bit to 1 disables access of the BIOS ROM in the system address range C600:0h-C6FF:Fh. Power on reset sets this bit to 0.

Bit 2

Enable 64K BIOS ROM.

Setting this bit to 1 enables address of the BIOS ROM in the system address range C600:0h-C6FF:Fh. Power on reset sets this bit to 0.

Bit 1

Setting this bit to a 1 locks Hercules compatibility register (I/O port 3BFh). Power on reset sets this bit to 0.

Bit 0

Map out 2K of BIOS ROM.

Setting this bit to 1 disables access of the BIOS ROM in the system address range C600:0h-C67F:Fh. Power on reset sets this bit to 0.

13.15 PR18A CRTC VERTICAL TIMING OVERFLOW

Read/Write Port = 3?5h, Index = 3Dh

These bits combined with other vertical timing overflow bits in CRTC constitutes a eleven bit vertical timing control. These bits are set to zero at power on reset.

BIT	FUNCTION
7:5	Reserved
4	Line compare bit 10
3[1]	Start vertical blank bit 10
2[1]	Start vertical retrace bit 10
1[2]	Vertical display enable end bit 10
0[1]	Vertical total bit 10

NOTES

[1] The bit is locked if PR3(0) = 1 OR the 3?5 Index 11 bit 7 = 1

[2] The bit is locked if PR3(1) = 0 AND the 3?5 Index 11 bit 7 = 1

13.16 PR20 UNLOCK SEQUENCER EXTENDED REGISTERS

Read/Write Port = 3C5h, Index = 06h

(Reset State = Locked)

A value of x1x01xxxx (48h) must be loaded to allow read/write of the Sequencer Extended Registers. When the extended registers are locked, then the Sequencer index is readable as three bits only. When unlocked, the Sequencer index read returns a 6 bit value.

13.17 PR21 DISPLAY CONFIGURATION AND SCRATCH PAD

Read/Write Port = 3C5h, Index = 07h

This register provides a convenient location for determining the current VGA configuration state. This information is needed for many of the BIOS calls.

BIT	FUNCTION
7:4	Scratch Pad Bits
3	Status of 3C2 bit 0
2	Status of PR2 bit 6
1	Status of PR4 bit 1
0	Status of PR5 bit 3

Bits 7:4

Read/Write scratch pad for any BIOS status data that may need to be saved. Reset state is 1111.

Bit 3

Reflects the setting of the I/O address select bit in the Miscellaneous Output Register.

0 = MDA (3Bx) addresses have been picked.
1 = CGA (3Dx) addresses have been selected by this read-only bit

Bit 2

Reflects the setting of the VGA/6845 select bit in PR2 (3CF index C).

0 = VGA or EGA compatibility has been picked.
1 = 6845 compatibility has been selected by this read-only bit

Bit 1

Reflects the setting of the VGA/EGA select bit in PR4 (3CF index E).

0 = VGA was picked.
1 = EGA compatibility has been selected by this read-only bit.

Bit 0

Reflects the setting of the Analog/TTL status bit in PR5 (3CF index F).

0 = Analog monitor selected by this read-only bit.
1 = TTL-type monitor picked.

13.18 PR22 SCRATCH PAD REGISTER

Read/Write Port = 3C5h, Index = 08h

Bit 7:0

Scratch pad bits

13.19 PR23 SCRATCH PAD REGISTER

Read/Write Port = 3C5h, Index = 09h

Bit 7:0

Scratch pad bits

13.20 PR30(A) WRITE BUFFER AND FIFO CONTROL REGISTER

Read/Write Port = 3C5h, Index = 10h

This register controls display memory data width and its bandwidth. All of the bits are reset to zero at power on reset.

13

BIT	FUNCTION
7,6	Write buffer control
5	32 or 16-bit Memory data path
4	Disable 16-bit CPU interface
3	2 level FIFO
2	4 or 8 level FIFO
1,0	Display FIFO control

Bits 7:6

Bits 6 and 7 control the depth of the write buffer.

BITS 7, 6	FUNCTION
00	Write buffer is one level deep
01	Write buffer is two levels deep
10	Write buffer is three levels deep
11	Write buffer is four levels deep

PR31 bit 2 must be set to 1 for these two bits to have any effect.

Bit 5

When set to 1, the display memory data path becomes 16-bits wide. Otherwise, the data path is 32-bits wide.

Bit 4

0 = Normal conditions
1 = 16-bit interface, unchained mode is disabled. This is for debug only.

Bit 3

0 = The FIFO is 4 or 8 level deep depending on bit 2 of tis register.
1 = The FIFO is 2 levels deep regardless of bit 2.

Bit 2

0 = FIFO set to 8 levels deep
1 = FIFO set to 4 levels deep.

Bit 1:0

Display FIFO Control

These two bits can be used to adjust the display memory bandwidth. In general it is recommended that these two bits be set to 01 to accommodate most applications. These bits have no effect in any text mode. They are locked into 00 internally when a text mode is set

BITs	FUNCTION	
00	FIFO requests for memory cycle when FIFO is	one level empty
01	FIFO requests for memory cycle when FIFO is	two levels empty
10	FIFO requests for memory cycle when FIFO is	three levels empty
11	FIFO requests for memory cycle when FIFO is	four levels empty

13.21 PR31 SYSTEM INTERFACE CONTROL

Read/Write Port = 3C5h, Index = 11h

(Reset State = 00h)

This register provides the control bits for the system interface. This register should be set during the Post initialization routines of the VGA BIOS. The reset state is 100% IBM VGA compatible. Bit 7 is used during some of the enhanced display modes.

BIT	FUNCTION
7	Read/Write Offset Enable
6	Turbo Mode for Blanked Lines
5	Turbo Mode for Text
4	CPU Read RDY release Control 1
3	CPU Read RDY release Control 0
2	Enable Write Buffer
1	Enable 16-bit Attribute Controller
0	Enable 16-bit CRTC, Sequencer and GRC

Bit 7

0 = Normal (Refer to PR0(A) and PR0(B) definitions).
1 = The offset register PR0(A) is added to CPU address for read cycles, while PR0(B) is added for write cycles.

Bit 6

0 = normal
1 = System performance is improved by 10% by removing extra screen refresh memory cycles on vertical blank.

Bit 5

0 = Normal
1 = Improve text mode performance

Bit 4:3

CPU Read RDY Release Controls 1,0. These two bits set the CPU's RDY timing to be optimized for different system timing. For slower systems, the RDY line may be released earlier because it takes longer for the read cycle to be completed.

00 = Power on reset condition. RDY is inserted at the end of a CPU memory cycle
01 = RDY is inserted 1MCK before the end of a CPU memory cycle.
10 = RDY is inserted 2MCK before the end of a CPU memory cycle.
11 = RDY is inserted 1MCK after the end of a CPU memory cycle.

For 10 MHz or slower systems, the 01 setting is recommended. For 12 MHz or faster systems, the 11 setting is recommended.

Bit 2

1 =Write buffer is enabled. This greatly reduces the number of wait states for CPU writes to display memory.
0 = write buffer disabled

Bit 1

If this bit and bit 0 are both set to 1, then the Attribute Controller (3C0/3C1) is configured for 16-bit access. The index is at 3C0, while the data is at 3C1, and the address toggle is disabled for 16-bit reads or writes. The address toggle functions in the standard way for 8-bit cycles. IOPCS16 is asserted for all cycles to 3C0 or 3C1.

Bit 0

1 = Enables 16-bit access to the CRTC (3?4/3?5), Sequencer (3C4/3C5), and Graphics Controller (3CE/3CF). The output $\overline{\text{IOCS16}}$ is active for any I/O read or write to these addresses.
0 = The VGA I/O is all 8-bit.

13.22 PR32 MISCELLANEOUS CONTROL 4

Read/Write Port = 3C5h, Index = 12h (Reset State = 00h)

This register provides control for several different features. Some of these features help to support Genlock of the WD90C24 to another display controller for overlay.

BIT	FUNCTION
7	Enable External Sync Mode
6	Disable Cursor Blink
5	USR1 Function Select
4	USR1 Control
3	USR0 Function Select
2	USR0 Control
1	Allow readback in backward compatible modes
0	Force standard CPU addressing in 132-column mode

13

Bit 7

0 = normal operation mode.
1 = $\overline{\text{EXVID}}$ is configured to input external Horizontal Sync, and $\overline{\text{EXPCLK}}$ inputs external Vertical Sync. The external $\overline{\text{HSYNC}}$ signal also synchronizes the character clock timing. In this configuration, $\overline{\text{EXVID}}$ and $\overline{\text{EXPCLK}}$ do not control the VID 7:0 and PCLK output buffers, but they are used to genlock the WD90C24 to another display controller.

Bit 6

1 = The text cursor blink is disabled, and the cursor remains on. This option can be used if cursor blink is not desired.
0 = blink is enabled.

Bit 5

0 = Causes the USR1 output to reflect the state of bit 4, which can be used to control new features that the system board designer may wish to add.
1 = The USR1 output is selected by PR35 bit 5, 4, 3. See PR35 description.

Bit 4

Controls the USR1 output when selected by bit 5.

Bit 3

0 = Causes the USR0 output to reflect the state of bit 2, which can be used to control new features that the system board designer may wish to add.
1 =The USR0 output is selected by PR35 bits 2,1,0. See PR35 description.

Bit 2

Controls the USR0 output when selected by bit 3.

Bit 1

1 = This bit allows reading the registers that are not readable in backward compatibility modes This option may be used either as a test feature or by the BIOS during mode changes.

Bit 0

1 = The special CPU address mapping for page mode font address in 132-column text is set for standard mapping without disturbing the display. This is used only for special virtual VGA applications.

13.23 PR33(A) DRAM TIMING AND ZERO WAIT STATE CONTROL REGISTER.

Read/Write Port = 3C5h, Index = 13ht

BIT	FUNCTION
7:6	Zero Wait State Output Pin
5	Reserved
4:3	CAS Timing
2	Select CAS Cycle Start
1:0	RAS Precharge

Bit 7:6

These 2 bits control the operation of the $\overline{\text{OWS}}$ output pin.

BIT7	BIT6	FUNCTION
0	0	$\overline{\text{OWS}}$ = 0 if the internal write is buffer ready
0	1	$\overline{\text{OWS}}$ = 0 if (The internal write buffer is ready) AND (Memory address is decoded)
1	0	$\overline{\text{OWS}}$ = 0 if (The internal write buffer is ready AND (Memory address is decoded) AND ($\overline{\text{MWR}}$ = 0)
1	1	$\overline{\text{OWS}}$ = 0 if (the condition 1 0 is true) OR (I/O write to WD90C24 is occurring

Bit 5

Reserved

Bit 4:3

These 2 bits control the CAS timing.

BIT	VALUE	FUNCTION
4:3	00	CAS cycle is 2 mclocks. CAS low is 1 mclock + (4-7) ns. CAS high is 1 mclock - (4-7) ns.
4:3	01	CAS cycle is 2 mclocks. CAS low is 1 mclock + (8-14) ns. CAS high is 1 mclock - (8-14) ns.
4:3	10	CAS cycle is 2 mclocks. CAS low is 1.5 mclocks. CAS high is 0.5 mclocks.
4:3	11	Reserved.

Bit 2

Select CAS Cycle Start

BIT	VALUE	FUNCTION
2	0	CAS cycle starts 2.5 mclocks after RAS low.
2	1	CAS cycle starts 1.5 mclocks after RAS low.

Bit 1:0

These 2 bits control RAS precharge.

BIT	VALUE	FUNCTION
1:0	00	$\overline{RAS}$ high is two and half mclocks plus a 4-7 ns delay.
1:0	01	$\overline{RAS}$ high is three mclocks wide.
1:0	10	$\overline{RAS}$ high is two mclocks wide.
1:0	11	$\overline{RAS}$ high is two and a half mclocks.

Refer to DRAM timing adjustments in Section 6

13.24 PR34(A) VIDEO MEMORY MAPPING REGISTER

Read/Write Port = 3C5h, Index = 14

Bits 7:0

BITS	FUNCTION
7:4	Reserved
3:0	The contents of these four bits are compared with the CPU address A_[23:20] as part of the video memory address decoding. This allows the VGA to be mapped into any 1M CPU memory space. This register does not affect the $\overline{ROM16}$ decoding. ROM16 can still decode at A_[23:20] = 0h. Used with proper setting on PR1 bits 5:4, this register supports virtual VGA application. These four bits are set to 0 at power on reset.

13.25 PR35(A) USR0, USR1 OUTPUT SELECT REGISTER

Read/Write Port = 3C5h, Index = 15

This register select which internal signals can be observed through USR0 and USR1 output pins. This is for debug purposes, and may be useful for using internal signals to control external functions, PR35 bit 5, & 3 must be set to 1 for this register to have any effect.

Bits 7:6

Reserved

Bits 5:3

5	4	3	USR1 =
0	0	0	1, if WD90C24 is fetching font from DRAM
0	0	1	1, if WD90C24 is fetching graphics data from DRAM
0	1	0	1, if the internal write buffer is ready
0	1	1	1, if CPU write cycle is occurring
1	0	0	0, if a CPU write cycle is not caused by write buffer
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

13

Bits 2:0

Bit Function

2	1	0	USR0 =
0	0	0	1, if I/O address is decoded
0	0	1	1, if WD90C24 is fetching character attribute from DRAM
0	1	0	0, if the internal write buffer is not empty
0	1	1	1, if CPU read cycle is occurring
1	0	0	0, if a write buffer cycle is occurring
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

13.26 PR45 VIDEO SIGNATURE ANALYZER CONTROL REGISTER

Read/Write Port = 3C5, Index = 16h
Unlock: PR20 (3?5.06h) = 48h

Bit	Function
7:4	Reserved
3	Unlock Signature Read Registers
2	Test Pattern
1	Initialize
0	Start

Bits 7:4

Reserved
Should be set to 0000 on writes to PR45. Undefined on reads.

Bit 3

Unlock Signature Read Registers

Setting this bit to 1 enables reading of PR45A and PR45B. The setting of this bit is readable.

Bit 2

Test Pattern

Setting this bit to 1 substitutes a fixed all zeros test pattern instead of the RAMDAC inputs into the signature analyzer. This all zeros test pattern is used, along with the capability of initializing the signature to 0001, to test the signature analyzer circuit. Setting of this bit is readable.

Bit 1

Initialize

Setting this bit to a 0 causes an initialization of the signature analyzer by preloading the signature to 0001h. This bit must be set to 1 before a video signature can be generated The setting of this bit is readable.

Bit 0

Start

Setting this bit to a 1 causes the signature analyzer to generate a signature of a video frame.

This bit must be set to 0 and then back to1 to restart generation of a new signature. The setting of this bit is readable.

13.26.1PR45A Signature Analyzer Data I

Read/Write Port = 3C5, Index = 17h
Unlock: PR20 (3?5.06h) = 48h, PR45 bit 3 = 1.
Value after Reset: 01h.

Bit	FUNCTION
7:0	Low Data Byte

13.26.2PR45B Signature Analyzer Data II

Read/Write Port = 3C5, Index = 18h
Unlock: PR20 (3?5.06h) = 48h, PR45 bit 3 = 1.
Value after Reset: 00h.

Bit	FUNCTION
7:0	High Data Byte

13.27 PR57 FEATURE REGISTER I

Read/Write Port = 3C5h, Index 19h.

BIT	FUNCTION
7:6	Reserved
5	Self-Refresh
4:3	TFT Dithering Mode Select
2	Panel Power Control
1	Selects Source for REFRESH Timing
0	Bank B Enable

Bit 7:6

Reserved

Should be set to 00.

Bit 5

Self-Refresh

The self-refresh control-high setting causes the power-down block REFRESH signal to go high.

This bit is write only.

Bits 4:3

TFT Dithering Mode Select

Bit 4 = TFTSEL1
Bit 3 = TFTSEL0

These bits are used with PR66 register bit 2 to select the mode of operation and colors for the TFT dithering engine. Selection of modes depends upon the TFT interface as listed in Tables 13-1 through 13-3.

:

PR57		PR66	
BIT 4	BIT 3	BIT 2	MODE
0	0	0	2-Frame Dithering, 27K Colors (Default)
0	0	1	2-Frame Dithering, 180K Colors
0	1	0	Invalid Setup
0	1	1	2 and 3 Frame Dithering, 256K Colors
1	0	0	No Dithering, 512 Colors
1	0	1	No Dithering, 512 Colors
1	1	0	Space Dithering, 27K Colors
1	1	1	Invalid Setup

TABLE 13-5 MODES FOR 9-BIT TFT

PR57		PR59	
BIT 4	BIT 3	BIT 3	MODE
0	0	x	2-Frame Dithering, 226K Colors (Default)
0	1	x	2-Frame Dithering, 226K Colors
1	0	x	No Dithering, 4K Colors
1	1	x	Space Dithering, 226K Colors

TABLE 13-6 MODES FOR 12-BIT TFT

PR57		PR59	
BIT 4	BIT 3	BIT 3	MODE
0	0	x	Invalid Setup
0	1	x	Invalid Setup
1	0	x	No Dithering, 256K Colors (Setup Only)
1	1	x	Invalid Setup

TABLE 13-7 MODES FOR 18-BIT TFT

Bit 2

Panel Power Control

When PR19 register bit 4 is set to 1, setting this bit to 1 causes the PNLOFF pin to output a low.

Setting this bit to 0 causes a high level to appear at PNLOFF.

This bit is set to 0 at reset causing PNLOFF to go active high. PNLOFF automatically goes high whenever PR19 register bit 4 is shut off, RESET is activated, or PWRDOWN is activated. Once the conditions causing PNLOFF to go high are removed, PNLOFF may be set low again writing a 1 to PR57 register bit 2.

Bit 1

Selects Source for REFRESH Timing

0 = REFRESHN pin input
1 = CKIN divided by PR71

13

Bit 0

Bank B Enable

When this bit is set to 1, memory accesses and refresh operations to Bank B video memory are enabled. Bank B operation occurs as dictated by the setting of bit 1 of this register.

When this bit is set to 0 all accesses and refresh operations to Bank B are halted. The Bank B address and control lines are static and the control lines at inactive levels. Bank B data lines are three-stated, being pulled high or low by their power-on configuration pullups or pulldowns.

This bit is set to 1 by default at reset.

13.28 PR58 FEATURE REGISTER II

Read/Write Port = 3C5h, Index = 20h
Unlock: PR5 (3C5.0Fh) = 05h

BIT	FUNCTION
7:1	Reserved
0	Scratch Pad Bit

Bit 7:1

Reserved

Bit 0

Scratch Pad Bit

13.29 PR58(A) MEMORY MAP TO I/O REGISTER FOR BLT ACCESS IN PI/LOCAL BUS

Read/Write Port = 3C5h, Index 26h.

BIT	FUNCTION
7-4	Reserved
3:2	Select True Color Modes (TRCLR[1:0])
1	Enable Mapping of High Memory Addresses to I/O Port 23C4h
0	Enable Mapping of High Memory Addresses to I/O Ports 23C0h through 23C5h.

Bits 7:4

Reserved

Bits 3:2

Select True Color Modes (TRCLR[1:0])

True color mode uses 16 bits per pixel and is partitioned into red, green, and blue bits (with red at the MSB and blue at the LSB). For example, 6-5-5 would have 6 red bits, 5 green bits, and 5 blue bits.

BIT 3	BIT 2	FUNCTION
0	0	Standard Color Palette Mode
0	1	5-6-5 64K True Color Mode
1	0	6-5-5 64K True Color Mode
1	1	5-5-5 32K True Color Mode

0 - Disabled
1 - Enabled

Bit 1

Enable Mapping of High Memory Addresses to I/O Port 23C4h

When PR57 register bits 1 and 0 are set high (11), this bit enables mapping of memory addresses A0000h through BFFFFh to I/O Port 23C4h.

0 - Mapping Disabled
1 - Mapping Enabled

Bit 0

Enable Mapping of High Memory Addresses to I/O Ports 23C0h through 23C5h.

When this bit is set to 1, memory addresses A0000h through BFFFFh are mapped to I/O Ports 23C0h through 23C5h.

0 - Mapping Disabled
1 - Mapping Enabled

Three address bits (SA2 through SA0) are use to decode the selected I/O port as follows:

SA2	SA1	SA0	I/O PORT SELECTED
0	0	0	23C0h
0	0	1	23C1h
0	1	0	23C2h
0	1	1	23C3h
1	0	0	23C4h
1	0	1	23C5h

13.30 PR59 - MEMORY ARBITRATION CYCLE SETUP REGISTER

Read/Write Port = 3C5h, Index = 21h
Unlock: PR5 (3C5.0Fh) = 05h

This register is used to setup the total length of the frame buffer memory fixed arbitration cycle, as a method of adjusting arbitration cycle length to the speed of the memory and speed of the CRT and Flat Panel Displays.

BIT	FUNCTION
7:3	Reserved
2	FCP2
1	FCP1
0	FCP0

Bits 7:3

Reserved

Bits 2:0

Setting these bits adjusts the arbitration cycle length in increments of 160 ns. The default arbitration cycle at reset is the 101b setting, or 800 ns. Cycle increments are based on a VCLK rate of 25 MHz and should be scaled accordingly for differing VCLK values.

13.31 PR60 FRAME BUFFER CONTROLLER I TEST REGISTER

Read/Write Port = 3C5h, Index = 22h

This register along with PR61 are used to set up various modes of operation of the frame buffer controller for testing. All register bits are set to 0 at reset.

BIT	FUNCTION
7	BAMUX Disable
6	WRCA Increment
5	RDCA Increment
4	RDCA Load
3	Add Offset
2	Clear RDS Register
1	Disable RDMA Counter and put in Test Mode
0	32 Word Offset Select

Bit 7

BAMU Disable

This bit controls the frame buffer test bus signal FBTST_7. Its function is to disable the normal flow of BAMUX signals allowing test signals to be multiplexed to the FBC address outputs for observation purposes. A 1 causes this selection of test outputs instead of the normal BAMUX outputs.

Bit 6

WRCA Increment

This bit controls the frame buffer test bus signal FBTST_6.

1 = Forces the FBCNT block's WRCHRINC signal active high, causing the WRCA counter to increment.

Bit 5

RDCA Increment

This bit controls the frame buffer test bus signal FBTST_5.

1 = Forces the FBCNT block's RDCHRINC signal active high, causing the RDCA counter to increment.

Bit 4

RDCA Load

This bit controls the frame buffer test bus signal FBTST_4.

1 = Forces the FBCNT block's RDBCALD signal active high, causing the RDCA register to be loaded with the contents of the RDS register.

Bit 3

Add Offset

This bit controls the frame buffer test bus signal FBTST_3.

1 = Forces the FBCNT block's RDSACCN signal active low, causing the selected offset value to be added into the RDS register.

Bit 2

Clear RDS Register

This bit controls the frame buffer test bus signal FBTST_2.

1 = Forces the FBCNT block's SLDZERON signal active low causing the RDS register to be cleared.

NOTE

Bit 1 of this register must be set to 1 in order for this action to occur.

Bit 1

Disable RDMA Counter and put in Test Mode

This bit controls the frame buffer test bus signal FBTST_1.

1 = The RDMA counter does not count in its normal fashion but instead enters a test mode.

Bit 0

32 Word Offset Select

This bit controls the frame buffer test bus signal FBTST_0. Its function is to control whether the frame buffer uses its normal address offset value of 320 or an abbreviated address offset of 32 for test.

1 = Causes the abbreviated offset value of 32 to be selected.

13.32 PR61 FRAME BUFFER CONTROLLER II TEST REGISTER

Read/Write Port = 3C5h, Index = 23h

This register along with PR60 is used to set up various nodes of operation of the frame buffer controller for testing.

Register bits 3-0 are set to 0 at time of reset. Other register bits are not implemented but should be written as 0s. Registers bit settings are directly readable.

BIT	FUNCTION
7:4	Reserved
3	Default 0
2	BMD SEL H
1	BMD SEL L
0	BAMUX CAS

Bits 7-4

Reserved

Bit 3

Set to 1: Puts 18 bits of address into RGB inputs of dithering engine for testability.

Bit 2

BMD[3:0] Select Hi

Bit 1

BAMUX CAS Address output

This bit controls the frame buffer test bus signal FBTST_8. Setting this bit to 1 caused the BAMUX to output the CAS address.

1 = Causes the RAS address to be output and 3?5.11(7) to control these registers.

Bit 0

BMD[3:0] Select Low

Bits 2 and 1 are select lines to a multiplexer that outputs internal nodes from the FBCNT block out onto the B memory data bus lower nibble.

13.33 PR62 - FR TIMING REGISTER

Read/Write Port = 3C5h, Index = 24h
Unlock: PR5 (3C5.0Fh) = 05h

BIT	FUNCTION
7:0	FR Timing

For color flat panels, this register controls the period of the Frame Rate (FR) signal in relation to the refresh rate. For monochrome flat panels, the FR rate is fixed at 480 line intervals.

The FR signal appears at the FR/$\overline{\text{BLANK}}$ pin anytime that PR19 register bit 4 is set to 1.

The default rate of the FR signal is once every 480 lines for a default-at-reset FR signal synchronized with the panel refresh rate of 480 line panels.

The rate of the FR signal may be adjusted faster or slower in increments of 8 lines.

The FR pulse rate generated is at a line count rate of 8 times the value stored in PR62.

For an FR pulse rate of once every 480 lines, PR62 should be set to 60d (3Ch).

The FR pulse is 50% duty cycle.

PR62 should not be set to 00h as this setting is reserved for test purposes.

13.34 PR63 READ/WRITE FIFO CONTROL REGISTER

Read/Write Port = 3C5h, Index 25h.

BIT	FUNCTION
7:2	Read/Write FIFO Control
1	Control Read FIFO Arbitration in Single Simultaneous Display Mode
0	Control Write FIFO Arbitration in Single Simultaneous Display Mode

Bits 7:0

Controls FIFO requests for the read and write FIFOs of the Frame Buffer Controller.

Bit 1

Controls Read FIFO Arbitration in Single Simultaneous Display mode.

Bit 0

Controls Write FIFO Arbitration in Single Simultaneous Display mode.

13.35 PR64 RESERVED FOR FUTURE NEED

Read/Write Port = 3C5h, Index 27h

13.36 PR65 RESERVED FOR FUTURE NEED

Read/Write Port = 3C5h, Index 28h

13.37 PR66 RAMDAC/PCLK REGISTER

Read/Write Port = 3C5h, Index 29h.

BIT	FUNCTION
7	Enable Auxiliary Video Extender (AVE) Mode
6	Select 12-bit TFT interface for dithering
5	Force LP and FP to be the same as HSYNC and VSYNC, respectively
4:3	Reserved, set to 0
2	Select TFT dithering
1:0	Reserved, set to 0

Bit 7

Enable Auxiliary Video Extender (AVE) Mode

This mode allows the internal RAMDAC to be used by an external source. The PCLK, BLANK, AND VID[7:0] pins become inputs to give direct access to the RAMDAC.

Bits 6

Select 12-bit TFT interface for dithering.

0 = Disable TFT Dithering
1 = Enable TFT Dithering

Bits 5

Force LP and FP to be the same as HSYNC and VSYNC, respectively.

0 = LP and FP normal
1 = LP is the same as HSYNC and FP is the same as VSYNC

Bits 4:3

Reserved, set to 0

Bit 2

Select TFT Dithering.

This bit is used with PR57 bits 4:3 to select the TFT dithering mode. Refer to the PR57 description for additional information.

Bits 1:0

Reserved, set to 0.

13.38 PR68 PROGAMMABLE CLOCK SELECTION REGISTER

Read/Write Port = 3C5h, Index 31h.

BIT	FUNCTION
7	Selects PCLKOFF
6:5	Reserved
4:3	VSEL[3:2]
2:0	MSEL[2:0]

Bit 7

Selects PCLKOFF

Places PCLK into powerdown mode (PCLKOFF). When in External Clock Mode. the internal PCLK is automatically placed in powerdown mode.

Bits 6:5

Reserved.

Bits 4:3

VSEL[3:2]

Enables VSEL[3:2] of the internal clock. Refer to the description of the Internal Programmable Clock.

VSEL[1:0] are provided by register 3C2h bits 3:2.

Bits 2:0

MSEL[2:0]

Enables MSEL[2:0] of the internal clock. Refer to the description of the Internal Programmable Clock.

13.39 PR69 PROGAMMABLE VCLK FREQUENCY REGISTER

Read/Write Port = 3C5h, Index 32h.

BIT	FUNCTION
7:0	N-Value of user programmable VCLK frequency.

Bit 7

N-Value

Holds the N-value that defines the VCLK frequency and is enabled when VSEL[3:0] = 0010.

13.40 PR70 MIXED VOLTAGE OVERRIDE REGISTER

Read/Write Port = 3C5h, Index 33h.

BIT	FUNCTION
7:6	Reserved
5	Override Voltage Detector Outputs
4:0	Manually Set Detector Latches

Bit 7:6

Reserved

Bit 5

Override Voltage Detector Outputs

Enables bits 4:0 to override all voltage detector outputs.

Bits 4:0

Manually Set Detector Latches

Independently sets five detector latches for 3.3V or 5V. The detector output latches set by bits 4:0 are PVDD, BVDD, FPVDD, MVDD, and AVDD2, respectively.

13.41 PR71 PROGRAMMABLE REFRESH TIMING REGISTER

Read/Write Port = 3C5h, Index 34h.

BIT	FUNCTION
7:0	Divide Clock

Bit 7:0

Divide Clock

Holds the upper 8 bits of the 10 bit divisor, which is used to divide CKIN/XVCLK and generate a refresh cycle. This register is enabled by setting PR57 register bit 1 to 1.

13.42 PR72 PROGRAMMABLE CLOCK UNLOCK

Read/Write Port = 3C5h, Index 35h.

BIT	FUNCTION
7	Reserved
6:4	Unlock Programmable Clock Selection Register
3:0	Reserved

Bit 7

Reserved

Bits 6:4

Unlock Programmable Clock Selection Register

Set to X101XXXXb to unlock PR68; the Programmable Clock Selection register. For ISO Monitor support, this is used as an ISO register lock of PR68 register.

Bits 3:0

Reserved

13.43 PR73 VGA STATUS DETECT

Read/Write Port = 3C5h, Index 36h.

BIT	FUNCTION
7	Enable/Disable Status Detect
6:5	I/O and Memory Detect
4	Select Status Signal Polarity
3:0	Reserved

Bits 7

Enable/Disable Status Detect

0 = Disable
1 = Enable

Bits 6:5

BITS		FUNCTION
6	5	
0	0	Reserved
0	1	I/O Detection
1	0	Memory Detection
1	1	Both I/O and Memory Detection

Bit 4

Select Status Signal Polarity

0 = Status Signal from FPUSR0 is active high.
1 = Status Signal from FPUSR0 is active Low.

Bits 3:0

Reserved.

14.0 FLAT PANEL PARADISE REGISTERS

NOTE

Combinations of bits from Paradise registers PR18, PR19, PR1A, and PR39 are used to select the display type and operation. Table 14-1 provides a summary of the selections.

14.1 PR18 FLAT PANEL STATUS REGISTER

Read/Write Port = 3?5h, Index = 31h

BIT	FUNCTION
7	DAC Shut Off
6	Enable Free Running Clock for Plasma or TFT Panel
5	Enable 256 Kbyte Colors in STN Color LCD
4	Enable Reverse Video in Flat Panel Mode
3	Enable Highest Contrast Intensity in Text Mode
2	TFT Color LCD Select*
1:0	Flat Panel Select
NOTE: Bits 1:0 are used to select display type and operation. Refer to Table 14-1.	

Bit 7

DAC Shut Off

This bit is used to shut off the internal DAC outputs. Usually, the DAC is shut off whenever PR19 bit 5 is low. Should an external DAC be used, the setting of this bit keeps the internal DAC disabled even when PR19 bit 5 is high.

0 = The internal DAC is enabled as normal.
1 = The internal DAC is held disabled.

Bit 6

Enable Free Running Clock for Plasma or TFT Panel.

0 - Disable free running.
1- Enable free running.

(This bit is used for the WD90C22 only.)

13

CASE	DISPLAY TYPE AND OPERATION	MONO/ COLOR	CRT	LCD		TFT	PANEL SEL		STN CONT		HRS
		PR39	PR19			PR18			PR1A		PR1A
		5	7	5	4	2	1	0	6	5	7
1	Mono-Dual-LCD-STD	0	0	0	1	0	0	0	0	0	0
2	Mono-Dual-LCD-HRS	0	0	0	1	0	0	0	0	0	1
3	Mono-Single-LCD-STD	0	0	0	1	0	1	1	0	0	0
4	Mono-Single-LCD-HRS	0	0	0	1	0	1	1	0	0	1
5	Color-Single-TFT-STD	1	0	0	1	1	1	1	0	0	0
6	Color-Single-TFT-HRS	1	0	0	1	1	1	1	0	0	1
7	Color-Single-STN-STD	1	0	0	1	0	1	1	0	1	0
8	Color-Single-STN-STD-16	1	0	0	1	0	1	1	1	1	0
9	Color-Dual-STN-STD-16	1	0	0	1	0	0	0	1	1	0
10	CRT Only	0	0	1	0	0	0	0	0	0	0
11	Plasma 8	0	1	0	1	0	0	1	0	0	0
12	Plasma	0	0	0	1	0	0	1	0	0	0
13	Simu CRT&LCD-Mono-Dual-STD	0	0	1	1	0	0	0	0	0	0
14	Simu CRT&LCD-Mono-Dual-HRS	0	0	1	1	0	0	0	0	0	1
15	Simu CRT&LCD-Mono-Single-STD	0	0	1	1	0	1	1	0	0	0
16	Simu CRT&LCD-Mono-Single-HRS	0	0	1	1	0	1	1	0	0	1
17	Simu CRT&LCD-Color-Single-TFT	1	0	1	1	1	1	1	0	0	0
18	Simu CRT&LCD-Color-Single-STN 8	1	0	1	1	0	1	1	0	1	0
19	Simu CRT&LCD-Color-Single-STN 16	1	0	1	1	0	1	1	1	1	0
20	Simu CRT&LCD-Color-Dual-STN 16	1	0	1	1	0	0	0	1	1	0

TABLE 14-1 DISPLAY TYPE AND OPERATION SELECTION SUMMARY

Bit 5

Enable 256 Kbyte Colors in STN Color LCD.

0 - Select 4 Kbyte colors.
1 - Select 256 Kbyte colors.

(This bit is used for the WD90C22 only.)

Bit 4

Enable Reverse Video in Flat Panel Mode.

This bit is used to reverse the polarity of video output data UC(3:0) and LD (3:0).

0 - Disable reverse video, positive polarity.
1 - Enable reverse video, negative polarity.

Bit 3

Enable Highest Contrast Intensity in Text Mode.

0 - Disable.
1 - Enable.

(This bit is used for the WD90C22 only.)

Bit 2

TFT Color LCD Select.

This bit is not readable.

0 - Disable TFT type color LCD panel interface.
1 - Enable TFT type color LCD panel interface.

Bit 1:0

Panel Select Bit 1 and Bit 0.

These two bits are used to select different sets of parameters which is loaded into the CRT controller. The parameters should be locked after loading.

PSB(1)	PSB(0)	PANEL TYPE
0	0	Dual Panel LCD Display
0	1	Plasma Display
1	0	EL Display
1	1	Single Panel LCD Display

14.2 PR19 FLAT PANEL CONTROL I REGISTER

Read/Write Port = 3?5h, Index 32h

BIT	FUNCTION
7	Plasma Panel Select
6	FP Timing Select
5	CRT Display Enable*
4	Flat Panel Display Enable*
3	Screen Auto-Centering/Vertical Expansion Select
2	Enable Auto Centering and Vertical Expansion
(1:0)	Number of Gray Scale Select
NOTE: Bit 7 is used to select display type and operation. Refer to Table 14-1.	

Bit 7

Plasma Panel Select.

This bit is used to select two different plasma panels.

0 - Select 4 data bits/1 pixel interface.
1 - Select 8 data bits/2 pixel interfaces (4 bits/ pixel).

Bit 6

FP Timing Select.

This bit is used to select two different frame pulse (FP) timings for different LCD panels.

0 - Select ON time during first horizontal line.
1 - Select ON time during second horizontal line.

Bit 5

CRT Display Enable.

This bit selects either CRT or Flat Panel to be the main (current) display. When the bit is enabled, the CRT controller is loaded with the parameters

13

based on the CRT monitor. If bit 5 has been enabled, bit 4 should be disabled. If bit 5 is disabled, bit 4 can be either enabled or disabled.

0 - Disable CRT (default).
1 - Enable CRT.<R>

When the CRT is the selected display, outputs LD03 and UD0-UD3 are active and can be used to drive an external RAMDAC.

Bit 4

Flat Panel Display Enable.

This bit selects the flat panel as the main display.

0 - Disable Flat Panel display.
1 - Enable Flat Panel display (default).

Bit 3

Screen Auto Centering/Vertical Expansion Select.

0 - Auto-centering (default).
1 - Reserved for Vertical Expansion (set to 0).

Bit 2

Enable Auto-Centering and Vertical Expansion.

0 - Disable (default).
1 - Enable.

This bit is used only for pulse wave modulation on the LCD panel.

Bit (1:0)

Number of Gray Scale Select

PR19(1)	PR19(0)	Gray Scale Number
0	0	2 (mono)
0	1	4
1	0	8
1	1	16

14.3 PR1A FLAT PANEL CONTROL II REGISTER

Read/Write Port = 3?5h, Index 33h.

BIT	FUNCTION
7	Enable 1024 Mode
6:5	Enable STN Control*
4	Enable 1280 Mode
3	Reserved
2	Shading Method Select
1	Select # (Number of) Memory Refresh Cycles
0	Select Memory Refresh Cycles Control
NOTE: Bit 7 is used to select display type and operation. Refer to Table 14-1.	

Bit 7

Enable 1024 High Resolution (HRS) Mode

Enables 1024 high resolution (HRS) mode. Also, used with bit 4 to select panel width.

Bits 6:5

Enable STN Control

Enable 8-bit and 16-bit STN type panels.

BIT 6	BIT 5	FUNCTION
0	0	Not STN
0	1	8-bit STN
1	1	16-bit STN

Bit 4

Enable 1280 Mode (Reserved for future need.)

Used with Bit 7 to select panel width.

BIT 7	BIT 4	FUNCTION
0	0	640 Pixel Width
1	0	1024 Pixel Width
X	1	1280 Pixel Width (Reserved for future need.)

Bits 3
Reserved

Bit 2

Shading Method Select.

0 - Frame rate modulation (default).
1 - Pulse width modulation.

Bit 1

Select Number of Memory Refresh Cycles.

0 - Select 1 refresh cycle/horizontal line.
1 - Select 2 refresh cycles/horizontal line.

Bit 0

Select Memory Refresh Cycles Control.

0 - Memory refresh cycles controlled by CRT controller.
1 - Memory refresh cycles controlled by PR1A(1).

14.4 PR1B FLAT PANEL UNLOCK REGISTER

Write Only Port 3?5, Index = 34

This register is used to protect PR18, PR19, PR1A, PR36 - PR41, and PR44 from being read from or written to. In order to access PR18, PR19, and PR1A, PR1B must be loaded first with 101XXXXX. In addition, PR36-PR41 must remain unlocked (until another value is written to PR1B). PR1B is also used to lock all Shadow registers (PR36-PR41). To unlock the Shadow registers, PR1B must be loaded first with XXXXX110; all Shadow registers remain unlocked until another value is written to the PR1B register.

14.5 PR30 MAPPING RAM UNLOCK REGISTER

Write Only Port = 3?5H, INDEX = 35H

This register is used to protect mapping RAM registers (PR33 through PR35) from being accessed. In order to read or write to these registers, PR30 must be loaded first with 30h. The mapping RAM registers remain unlocked until another value is written to the PR30 register.

14.6 PR33 MAPPING RAM ADDRESS COUNTER REGISTER

Read/Write Port = 3?5h, Index = 38h

This register is used to select the RAM ADDRESS COUNTER register.

NOTE

Any I/O Read or Write to the I/O port 3?5.39h (Mapping RAM Data register) increments the Mapping RAM Address Counter by one.

14.7 PR34 MAPPING RAM DATA REGISTER

Read/Write Port = 3?5h, Index = 39h

This register is used to select the RAM data register for memory read or memory write.

14.8 PR35 MAPPING RAM AND POWER-DOWN CONTROL REGISTER

Read/Write Port = 3?5h, Index = 3Ah

BIT	FUNCTION
7	Select System Power-Down Mode/ Display Idle Mode
6	Select Internal Divided By 8 Clock to Control General Power Down Mode
5	Host Release Control
4	Reserved, set to 1.
3	Select 64 Gray Scale Levels
2	Reserved, set to 1
1	Enable Weighting Equation
0	Reserved; set to 1.

Bit 7

Select System Power Down Mode/Display Idle Mode. Refer to Figure 14-1.

0 - Display idle mode (default).
1 - System power down mode; MCLK and VCLK turned off.

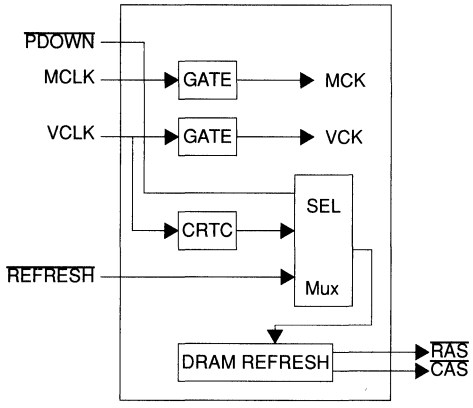
Bit 6

Select Internal Divided by 8 Clock to Control General Power Down Mode. This bit is active only when PR44(7) is set at 1.

0 - Disable internal clock.
1 - Enable internal clock; clock is divided by 8.

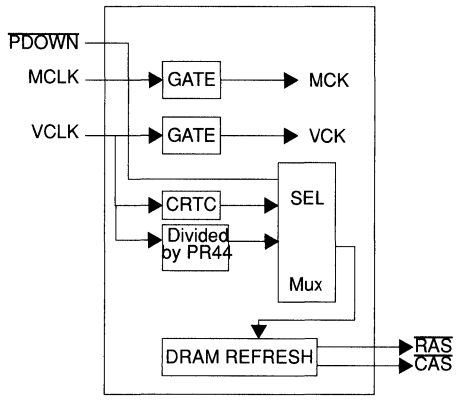
13

PR44 (7)	PR35 (7)	PR35 (6)	MODE
0	1	X	System Power Down Mode: MCLK and VCLK are turned off. Video memory refresh is generated from PDREF. Neither memory nor I/O can be accessed. RAMDAC and Mapping RAM must be reloaded.
0	0	X	Display Idle Mode: MCLK and VCLK are divided by 8 before being distributed across the chip. Video memory refresh is generated from PDREF. Only I/O can be accessed.
1	X	0	General Power Down (External Clock Used): MCLK and VCLK inputs are used to drive the chip. The assumption is made that MCLK and VCLK have been reduced by some other part of the system. The video memory refresh period is readjusted for the slower clock by PR44 (6:0). Both memory and I/O can be accessed.
1	X	1	General Power Down (internal Clock Used): MCLK and VCLK inputs are divided by 8 before being distributed across the chip. The video memory refresh period is readjusted for the slower clock by PR44 (6:0). Both memory and I/o can be accessed.



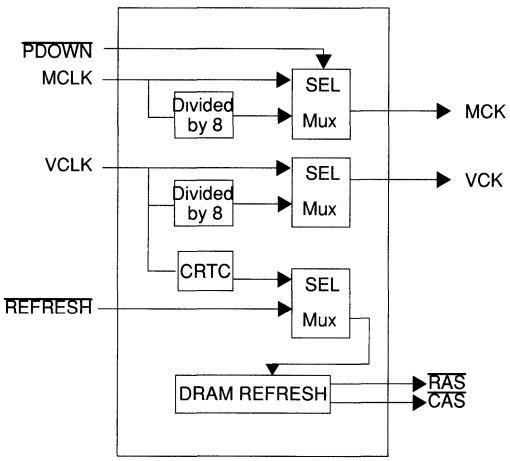
SYSTEM POWER DOWN MODE (SLEEP)

A. RAMDAC is off.
B Clock Inputs are turned of as they enter the chip
C. CAS before RAS video memory refresh is generated from REFRESH input
D. Neither video memory or I/O can be accessed in this mode.
E RAMDAC and Mapping RAM contents are lost and must be reloaded to resume



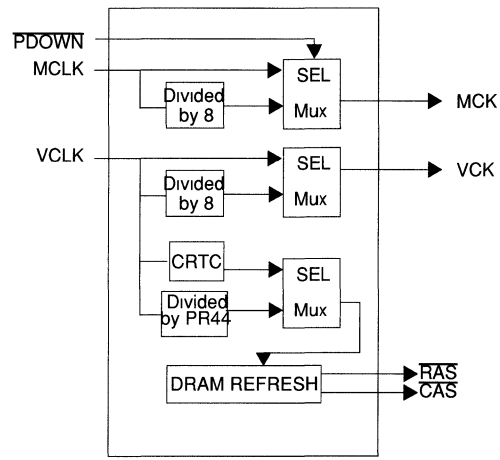
GENERAL POWER DOWN MODE (EXTERNAL CLOCK)

A. RAMDAC is off.
B. MCLK and VCLK are not modified, their speed is reduced by system resources.
C. Refresh cycles triggered by PR44 may be RAS only or CAS before RAS
D. Video memory and I/O are accessible.



DISPLAY IDLE MODE (SUSPEND/RESUME)

A RAMDAC is off.
B. MCLK and VCLK are divided by 8
C Refresh is CAS before RAS and is generated by REFRESH input
D I/O is accessible and memory is not accessible.



GENERAL POWER DOWN MODE (INTERNAL CLOCK)

A. RAMDAC is off.
B MCLK and VCLK are divided by 8.
C. Refresh cycles triggered by PR44 may be RAS only or CAS before RAS. PR44 can be RAS only.
D. Video memory and I/O are accessible.

FIGURE 14-1 SYSTEM POWER DOWN MODE/DISPLAY IDLE MODE

Bit 5

Host Release Control.

This bit is designed to allow another VGA controller on the I/O bus. When PR35(5) is set to 1 and PDOWN input is set to 0, the WD90C24 does not respond to any CPU memory or I/O accesses. All output buffers of the system interface are turned off (tri-state).

There four power down modes. the following conditions are true in each power down mode.

1. Video memory is maintained
2. RAMDAC outputs are turned off.
3. Panel outputs are turned off.

Bit 4

Reserved, set to 1.

Bit 3

Select 64 Grey Scale Levels.

0 = Select disabled; selects 32 grey scale levels.
1 = Select enabled; select 64 grey scale levels.

Bit 2

Reserved, set to 1.

Bit 1

Enable Weighting Equation.

This bit is used to turn the IBM VGA weighting equation on an off in either color mode or monochrome mode.

0 = Disable weighting equation.
1 = Enable weighting equation.

Bit 0

Reserved. Tis bit is set at 1.

14.9 PR36 PANEL HEIGHT SELECT REGISTER,

Read/Write Port = 3?5h, Index = 3Bh

This register is loaded with the height, less 1, of a single panel. This information is used to calculate auto-centering, vertical expansion, and related values. In a 640 by 480 dual panel display, this register should be loaded with EFh. (480/2)-1 = 239 10 = EFh. In a 640 by 400 dual panel display, the equation is: (400/2)-1 = 199 10 = C7h.

14.10 PR37 FLAT PANEL BLINKING CONTROL

Read/Write Port = 3?5h, Index = 3Ch

This register is used to select cursor or character blinking rate on flat panels. In CRT mode, this register is ignored.

Bit 2	Bit1	Bit0	CURSOR BLINKING RATE SELECT
0	0	0	No cursor blinking
0	0	1	8 frames (8 on, 8 off)
0	1	0	16 frames (16 on, 16 off)
0	1	1	32 frames
1	0	0	64 frames
1	0	1	128 frames

Bit 5	Bit 6	Bit3	CHARACTER BLINKING RATE SELECT
0	0	0	No cursor blinking
0	0	1	8 frames (8 on, 8 off)
0	1	0	16 frames (16 on, 16 off)
0	1	1	32 frames
1	0	0	64 frames
1	0	1	128 frames

Bit6			PLASMA SHIFT CLOCK SELECT
0			Select falling edge of the clock to latch data
1			Select rising edge of the clock to latch data

Bit6			PLASMA SHIFT CLOCK SELECT
0			Disable LP during vertical blanking period
1			Generate LP continuously during vertical blanking period (SCLK is turned off)

14.11 PR39 COLOR LCD CONTROL REGISTER

Read/Write Port = 3?5h, Index = 3Eh

This register is used to support color LCD panels.

BIT	FUNCTION
7	Enable Border LP Control
6	Color LCD Panel Border Select
5	Enable Color LCD Pane
4	Synchronous Extended I/O cycle
3	Enable Reverse Video
2	Enable CRT VSYNC and HSYNC
1	FP Polarity Select
0	LP Polarity Select

Bit 7

Enable Border LP Control

This bit is used to generate a special LP pulse to latch border information (black or white).

0 = Disable LP border control.
1 = Enable LP border control.

Bit 6

Color LCD Panel Border Select

0 = Select black border.
1 = Select white border.

Bit 5

Enable Color LCD Panel

This bit is used to select monochrome or color LCD interface support (refer to Table 14-1). When set to 1, this bit enables ENDATA for TFT panel, selects color panel FP, LP, and FR timing, and selects color dithering.

0 = Monochrome LCD panel interface.
1 = Color LCD panel interface.

Bit 4

Synchronous Extended I/O Cycle Enable

When in MicroChannel mode, this bit when set allows the WD90C24 to operate in Synchronous Extended I/O Cycle mode. CDCHRDY timing is modified accordingly.

Bit 3

Enable Reverse Video

See PR18 register bit 4.

Bit 2

Enable CRT VSYNC and HSYNC.

PR39 (2)	Pin 109 $\overline{\text{VSYNC}}$	Pin 108 $\overline{\text{HSYNC}}$
0	Inactive High	Inactive High
1	CRT VSYNC	CRT HSYNC

At reset, PR39 register bit 2 defaults to 0. Also, it may be set to 0 for power saving when CRT support is not needed.

Bit 1

FP Polarity Select

If PR39 (1)=0, then FP has normal polarity.
If PR39 (1)=1, then FP has reverse polarity.

Bit 0

LP Polarity Select

If PR39 (0)=0, then LP has normal polarity.
If PR39 (1)=1, then LP has reverse polarity.

14.12 PR41 VERTICAL EXPANSION INITIAL VALUE REGISTER

Read/Write Port = 3?5h, Index = 37h

BITS	FUNCTION
7:0	Vertical Expansion Initial Value

Bit 7:0

This register is used to decide which horizontal line is repeated in the very beginning when vertical expansion is enabled. It is very useful to implement smooth scrolling when 200, 350 or 400 line-mode displayed on a 480-line panel.

14.13 PR44 POWER-DOWN MEMORY REFRESH CONTROL REGISTER

Read/Write Port = 3?5h, Index = 3Fh

This register controls two power saving features when in the general power down modes. Bit 7 is used with PR35(7:6) to determine which power down mode is to be used. With some power down modes, the clocks used to refresh memory are slowed or stopped. This is done because the power consumption of the CMOS chip is proportional to its clock frequency. PR44(6:0) are loaded with a value that modifies the video memory refresh period during power down.

BIT	FUNCTION
7	General Power Down Mode Enable
6:0	Memory Refresh Cycle Period

Bit 7

General Power Down Mode Enable Bit.

This bit enables general power down mode.

0 - Disables general power down.
1 - Enables general power down.

Bit 6:0

Memory Refresh Cycle Period.

These bits are loaded with the value Z, which is used to determine the refresh period when general power down mode is used. Refresh period = VCLK x 8 x (Z+5). For example, assume:

1. Two memory refresh cycles are selected during horizontal blanking period in Flat Panel display mode.
2. Each horizontal line has 96 character clocks.
3. MCLK = 36 MHz, VCLK = 25 MHz.
4. PR44 = 8Eh.

When in power-down mode, POWRDN = 0, MCLK = VCLK = 5 MHz.

1. Z = 14.
2. Refresh Cycle = 200 ns x 8 x (14 + 5).
3. Maximum Refresh Period = 200 ns x 8 x (14 + 5 - 7) = 19.2 microseconds.
4. Refresh Active Time = MCLK x 9 x 2 (cycle) = 200 ns x 9 x 2 = 3.6 microseconds

15.0 COMPATIBILITY REGISTERS

Refer to Section 7 for a summary of Compatibility registers.

15.1 HERCULES/MDA MODE CONTROL REGISTER, MDA OPERATION

Write Only Port = 3B8h

BIT	FUNCTION
7	Reserved/Display Memory Page Select
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Reserved/Port 3BFh Enable
0	High Resolution Mode

Bit 7

Reserved in MDA mode. If Bit 1 = 1 and Port 3BFh bit 0 = 1, then this bit in Hercules Graphics mode selects the Display Memory Page.

0 - Display memory page address starts at B000:0h.
1 - Display memory page address starts at B800:0h.

Bit 6

Reserved.

Bit 5

Enable Blink.

0 - Disable Blinking
1 - Enable Blinking

Bit 4

Reserved.

Bit 3

Video Enable.

0 - Video Disable
1 - Video activated

13

Bit 2

Reserved.

Bit 1

Port 3BFh enable.

0 - Prevents setting of Port 3BFh bit 1:0, thereby forcing the alpha mode operation.
1 - Allows the Port 3BFh bits (1:0) to switch for the alpha or graphics mode selection.

Bit 0

High Resolution Mode.

Should be 1.

0 - High resolution disabled.
1 - High resolution is enabled.

15.2 HERCULES REGISTERS

The Hercules Mode Register is a 2-bit write only register located at I/O port address 3BFh. It affects the device operation only in the 6845 mode. The enable mode register located at the address 3B8 overrides the write port 3BFh functions defined by its bits 0 and 1. The associated details are shown below.

15.3 ENABLE MODE REGISTER 3B8h

BIT	FUNCTION
7	Display Memory Page Address Graphics Mode
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Port 3BFh Bit 0 Override
0	High Resolution Mode = 1

Bit 7

Display memory Page Address In Graphics Mode.

0 - Display memory page address starts at B000:0h.
1 - Display memory page address starts at B800:0h.

Bit 6

Reserved.

Bit 5

Enable Blink.

Bit 4

Reserved.

Bit 3

Video Enable.

Bit 2

Reserved.

Bit 1

Port 3BF Bit 0 override.

0 - Prevents setting of Port 3BF bit 0, thereby forcing the alpha mode operation.
1 - Allows the Port 3BF bit 0 to switch for the alpha or graphics mode selection.

Bit 0

High Resolution Mode.

15.4 HERCULES COMPATIBILITY REGISTER

Write Only Port - 3BFh

BIT	FUNCTION
7:2	Reserved
1	Upper Memory Page Address
0	Enable Graphics

Bits 7:2

Reserved.

Bit 1

Upper Memory Page Address.

Enable Mode Control Register (3B8) bit 7 selects the displayed memory page address in the graphics mode. When it is reset, bit 1 prevents access to the second memory page, located at B000:0h for the 32KByte memory space.

0 - Upper memory page is mapped out.
1 - Upper memory page is accessible.

Bit 0

Enable Graphics.

Allows the Enable Mode Register (3B8) bit 1 to override.

0 - Alpha mode display.
1 - Graphics modes may be displayed.

15.5 COLOR CGA OPERATION REGISTER

Write Only Port - 3D8h

BIT	FUNCTION
7:6	Reserved
5	Enable Blink
4	B/W Graphics Mode
3	Enable Video
2	B/W/Color Mode Select
1	Graphics/Alpha Mode Select
0	Alpha Mode

Bit 7:6

Reserved.

Bit 5

Enable Blink Function.

0 - Disables blinking function.
1 - For normal operation, set this bit to allow blinking

Bit 4

B/W Graphics Mode Enable.

0 - Deselect 640 x 200 B/W graphics mode.
1 - Enable 640 x 200 B/W graphics mode.

Bit 3

Activate Video Signal.

0 - Deactivates video signal. This is done during mode changes.
1 - B/W mode enabled.

Bit 1

Text or Graphics Mode Selection.

0 - Alpha mode enable.
1 - graphics mode (320 x 200) activated.

Bit 0

(40 x 25) or (80 x 25) Text Mode Selection.

0 - 40 x 25 alpha mode enabled.
1 - 80 x 25 alpha mode activated.

15.6 CGA Color Select Register

Write Only Port - 3D9h

BIT	FUNCTION
7:6	Reserved
5	Graphics Mode Color Set
4	Alternate Color Set
3	Border Intensity
2	Red Border
1	Green Border
0	Blue Border

Bit 7:6

Reserved.

Bit 5

320 x 200 Color Set Select for the CGA 2 bits per pixel.

0 - Background, Green, Red, Brown colors.
1 - Background, Cyan, Magenta, White colors.

Bit 4

Alternate Color Set Enable.

0 - Background color in alpha mode.
1 - enable alternate color set in graphics mode.

Bit 3

Border Intensity.

Border color select in text modes, and screen background color in 320 x 200 and 640 x 200 graphics mode.

Alphanumeric Mode.

1 - Selects intensified border color.

320 x 200 Graphics mode.

1 - Selects intensified background and border color (C0 - C1).

640 x 200 Graphics Mode.

1 - Selects red foreground color.

13

Bit 2

Red Border/Background

Border color select in text modes, and screen background color in 320 x 200 and 640 x 200 graphics modes.

Text mode:

1 - select red border color

320 x 200 graphics mode:

1 - Select red background and border color

640 x 200 graphics mode:

1 - select red foreground color.

Bit 1

Green border/Background.

Border Color select in text modes, and screen background color in 320 x 200 and 640 x 200 graphics mode.

Alphanumeric Mode.

1 - Selects green border color.

320 x 200 Graphics mode.

1 - Selects green background and border color (C0 - C1).

640 x 200 Graphics Mode.

1 - Selects green foreground color.

Bit 0

Blue border/Background.

Border Color select in text modes, and screen background color in 320 x 200 and 640 x 200 graphics mode.

Alphanumeric Mode.

1 - Selects Blue border color.

320 x 200 Graphics mode.

1 - Selects Blue background and border color (C0 - C1).

640 x 200 Graphics Mode.

1 - Selects Blue foreground color.

15.7 CRT STATUS REGISTER MDA OPERATION

Read Only Port - 3BAh

BIT	FUNCTION
7	VSYNC Inactive
6:4	Reserved
3	B/W Video Enabled
2:1	Reserved
0	Display Enable Inactive

Bit 7

Vertical Retrace.

0 - Indicates the raster is in vertical retrace mode.
1 - Indicates vertical retrace is inactive (inverted VSYNC if I/O is mapped into 3BX).

Bit 6:4

Reserved.

Bit 3

B/W Video Status.

0 - B/W Video disabled.
1 - B/W Video enabled.

Bit 2:1

Reserved.

Bit 0

Display Enable.

0 - Display enable is active.
1 - Indicates the screen border or blanking is active; Display Enable is inactive.

15.8 CRT STATUS REGISTER CGA OPERATION

Read Only Port - 3DAh

BIT	FUNCTION
7:4	Reserved
3	VSYNC Active
2	Light Pen Switch Status
1	Light Pen Latch Set
0	Display Enable Inactive

Bit 7:4

Reserved.

Bit 3

Vertical Retrace.

0 - Indicates vertical retrace is inactive.
1 - Indicates the raster is in vertical retrace mode

Bit 2

Light Pen Switch Status.

0 - Light pen switch closed.
1 - Light pen switch open

Bit 1

Light Pen Latch.

0 - Light Pen Latch cleared.
1 - Light Pen Latch set.

Bit 0

Display Enable.

0 - Display Enable is active.
1 - Indicates the screen border or blanking active; Display Enable is inactive.

15.9 AT&T/M24 REGISTER

Write Only Port - 3DEh

This is a write only, 8-bit register located at address 3DEh. It is used to control the 640 x 400 AT&T graphics mode. All bits are set to zero by reset. This register is enabled by setting bit 7 in PR Register 2 (PR2).

BIT	FUNCTION
7	Reserved
6	White/Blue Underline
5,4	Reserved
3	Memory Map display
2	Character Set Select
1	Reserved
0	AT&T Mode Enable

Bit 7

Reserved.

Bit 6

White/Blue Underline.

Defines underline attribute according to the MDA display requirements.

0 - Underline attributes selects blue foreground in-color text modes.
1 - Underline attribute selects white underlined foreground.

Bits 5:4

Reserved.

Bit 3

Page Select.

Selects between one or two 16 Kbyte RAM page for display in 200 line graphics mode.

0 - Display memory address starts at B800:0h (16KB length).
1 - Display memory address starts at BC00:0h (16KB length).

Bit 2

Character Set Select.

Selects between two character font planes.

0 - Standard character font from plane 2.
1 - Alternate character font from plane 3.

Bit 1

Reserved.

Bit 0

M24 or non-IBM Graphics Mode. 400 line mode, (A 400 line monitor is required for this mode).

0 - 200 line graphics mode active, using paired lines.
1 - AT&T mode enabled for 400 line graphics.

16.0 EXTENDED REGISTER ACCESS FOR HARDWARE CURSOR, BITBLT, AND LINE DRAWING

All of the WD90C24 enhanced functions are controlled by one or more extended registers, most of which are above and beyond standard VGA registers.

Enhanced functions are controlled by indexed register blocks. Each indexed register block can contain up to 16 12-bit indexed registers. The 4-bit register index is written, along with the 12-bit data field, to form a 16-bit word.

Access to VGA-type registers is described in Section 20. This section describes the access to indexed register blocks.

16.1 ACCESSING INDEXED REGISTERS

To write to one or more indexed registers within any register block, the register block must first be selected by loading its address into the Register Block Pointer fields of the Index Control Register. This causes the selected register block to appear at the Register Access port.

A 16-bit word is then written to the Register Access port. The 4 high-order bits specify the Index of the register to be written, while the 12 low-order bits are the data to be written. Then, additional registers within the same register block can be written without reselecting the same register block.

To read one or more indexed registers within a register block, first, the address of the register block is written to the Register Block Pointer Field (bits 7:0) of the Index Control Register at port 23C0h/23C1h. Then, the desired starting register to be read within the block is written to the Register Index Field (bits 11:8). Both fields are set with the same 16-bit write. This causes the selected register to appear at the Register Access Port located at 23C2h//23C3h.

A 16-bit word is then read from the Register Access port. When reading an indexed register, the four high-order bits of the value returned contain the index of the register.

If the Auto-increment Disable bit in the Index Control Register is reset, consecutive reads to the Register Access port will return consecutively indexed registers within the same register block. Registers are read in ascending order through register Fh (the sixteenth register in the block), followed by register 0 and cycling indefinitely as long as reads continue. Addressing a non-existent register results in zeros being returned in the 12-bit data field.

If the Auto-increment Disable bit is set, consecutive reads return the same index register.

GLOBAL PORT MAP	
PORT	**DESCRIPTION**
23C0h	Index Control Register, Low Byte
23C1h	Index Control Register, High Byte
23C2h	Register Access Port, Low Byte
23C3h	Register Access Port, High Byte
23C4h	BITBLT I/O Port
23C5h	BITBLT I/O Port
23C6h	Reserved
23C7h	Reserved

16.2 INDEX CONTROL REGISTER - PORT 23C0h/23C1h

Except for bit 13, which is read-only, the Index Control Register is a read/write register that controls reads and writes to indexed register blocks.

BITS	FUNCTION
15:14	Reserved
13	Invalid Register Block (read-only bit)
12	Auto-increment Disable
11:8	Register Index
7:0	Register Block Pointer

Bits 15:14

Reserved

Bit 13

Invalid Register Block (Read Only)

0 = Currently addressed register block exists on this device.
1 = Currently addressed register block does not exist on this device.

Bit 12

Auto-increment Disable

0 = Consecutive Reads return consecutive indexed registers.
1 = Consecutive Reads return the same indexed register.

Bits 11:8

Register Index

The index of the desired starting register to be read within a block is written to these bits. When read, these bits return the index of the next register to be read.

Bits 7:0

Register Block Pointer

To read one or more indexed registers within a register block, the address of the register block is written to this field.

REGISTER BLOCK MAP	
POINTER	**REGISTER/PORT ACCESS**
00	System Control Registers
01	BITBLT Registers
02	Hardware Cursor Registers

16.3 INTERRUPT STATUS REGISTER, SYSTEM CONTROL REGISTERS BLOCK - INDEX 0

Interrupt Status information is provided by the Interrupt Status Register in the System Control Register Block. This register returns information regarding which part of the WD90C24 caused an interrupt.

Reading this register does not reset any interrupts. Resetting of each interrupt is handled independently.

Unassigned interrupts are returned as zeros.

BITS	FUNCTION
15:12	0000 (Index)
11	Interrupt 10 Active
⇓	⇓
8	Interrupt 7 Active
7	High when at least one of interrupts 10 through 7 is active.
6	Interrupt 6 Active
⇓	⇓
1	Interrupt 1 Active
0	Any Interrupt is Active

16.3.1 Global Interrupt Map

INTERRUPT	DESCRIPTION
1	VGA Interrupt
2	BITBLT Interrupt

13

17.0 HARDWARE CURSOR

The hardware cursor supports a user-defined pattern of up to 64 x 64 pixels defined at 2 bits per pixel. The cursor pattern should be stored in a non-visible part of display memory. The cursor operates in all packed and planar VGA graphics modes, as well as VGA text modes.

Each register is defined by the index number in bits 15:12.

INDEX	FUNCTION
0	Cursor Control
1	Cursor Pattern Address Low
2	Cursor Pattern Address High
3	Cursor Primary Color
4	Cursor Secondary Color
5	Cursor Origin
6	Cursor Display Position X
7	Cursor Display Position Y
8	Cursor

TABLE 17-1 CURSOR REGISTERS

17.1 CURSOR CONTROL REGISTER, INDEX 0

This register controls operation of the hardware cursor.

BIT	FUNCTION
15:12	0000 (Index)
11	Cursor Enable
10:9	Cursor Pattern type
8	Cursor Plane Protection
(7:5)	Cursor Color Mode
1:0	Reserved

Bits 15:12

Index 0.

Bit 11

Cursor Enable

0 = Cursor is not displayed
1 = Cursor is displayed

Bits 10:9

Cursor Pattern Type

00 = Cursor is 2 bits per pixel, 32 x 32 pixels
01 = Cursor is 2 bits per pixel, 64 x 64 pixels
10 = Reserved
11 = Reserved

Bit 8

Cursor Plane Protection

0 = Cursor plane protection disabled
1 = Cursor plane protection enabled

Bits 7:5

Cursor Color Mode

BITS 7:5			FUNCTION
0	0	0	Straight monochrome (compatibility)
0	0	1	Two-color cursor with inversion
0	1	0	Two-color cursor with special inversion
0	1	1	Three-color cursor
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Bits 4:0

Reserved

17.2 CURSOR PATTERN ADDRESS

The two cursor pattern address registers form a 20-bit address which specifies the location in the non-visible portion of display memory where the first byte of the cursor pattern is stored. This value is independent of the cursor origin.

Generally, this address represents the CPU address at which the pattern begins minus the CPU address of the top-left corner of the screen, in whatever VGA mode is currently in use. All addresses are not valid in all modes. See the section on "Cursor Address Mapping".

NOTE

A write to either Cursor Pattern Address register or to the Cursor Origin register does not take effect until the beginning of a video frame following the next write to the cursor control register.

17.2.1 Cursor Pattern Address Low, Index 1

The lower order twelve bits of the 20 bit cursor pattern address.

BIT	FUNCTION
15:12	0001 (Index)
11:0	Cursor pattern address bits 11:0

17.2.2 Cursor Pattern Address High, Index 2

The high order eight bits of the 20 bit cursor pattern address.

BIT	FUNCTION
15:12	0001 (Index)
11:9	Reserved
8:0	Cursor pattern address bits 19:12

17.3 CURSOR ORIGIN, INDEX 5

The cursor origin register specifies the offset from the top-left corner of the pattern which is displayed at the cursor display position. This value is often referred to as the cursor's "hot spot".

NOTE

For 32 x 32 cursor patterns each field is restricted to the values 31 through 0.

BIT	FUNCTION
15:12	0101 (Index)
11:6	Cursor origin Y bits 63:0
5:0	Cursor origin X bits 63:0

17.4 CURSOR DISPLAY POSITION

The cursor display position X and Y registers specify the location on the screen at which the cursor origin is displayed. These values represent a position in pixels, referenced to the top-left corner of the screen, regardless of the display mode.

In text modes, the cursor position still represents pixels, not characters. The cursor can be displayed at any position on the screen, including between characters.

NOTE

A write to the cursor display position X or Y register does not take effect until the beginning of the next video frame. (In interlaced mode, the next video field.)

17.4.1 Cursor Display Position X, Index 6

BIT	FUNCTION
15:12	0110 (Index)
11	Reserved
10:0	Cursor Display Position X

17.4.2 Cursor Display Position Y, Index 7

BIT	FUNCTION
15:12	0111 (Index)
11	Reserved
10:0	Cursor Display Position Y

17.5 CURSOR COLOR REGISTERS

The cursor color resisters control display of 2-bit per pixel cursor patterns.

The cursor primary color, cursor secondary color, and cursor auxiliary color resisters specify eight-bit colors to be displayed for different parts of the cursor pattern.

NOTE

Even in planar mode, with four-bits per pixel, these colors are 8 bits per pixel

17.5.1 Cursor Primary Color, Index 3.

BIT	FUNCTION
15:12	0011 (Index)
11	Reserved
7:0	Cursor Primary Color

17.5.2 Cursor Secondary Color, Index 4

BIT	FUNCTION
15:12	0100 (Index)
11	Reserved
7:0	Cursor Secondary Color

17.5.3 Cursor Auxiliary Color, Index 8

BIT	FUNCTION
15:12	1000 (Index)
11	Reserved
7:0	Cursor Auxiliary Color

18.0 HARDWARE BITBLT

The BITBLT hardware supports accelerated data transfers between regions of display memory. Display memory regions may be rectangular or linear.

A full complement of raster operations are available. Color expansion and transparency, useful for accelerating text modes as well as plane masking, are also supported.

This same hardware can be used to rapidly copy 8 by 8 patterns and fill rectangles.

The BITBLT hardware supports text modes and monochrome, 4-bit and 8-bit color modes, as well as the 16-bit color mode. The BITBLT registers are listed by their index number in Table 18-1.

INDEX NUMBER	BITBLT REGISTER NAME
0	Control - Part 1[1]
1	Control - Part 2
2	Source Low/XSTEP
3	Source High/RSTEP
4	Destination Low[1]
5	Destination High[1]
6	Dimension X/Delta-X
7	Dimension Y/Delta-Y
8	Row Pitch
9	Raster Operation
A	Foreground Color
B	Background Color
C	Transparency Color
D	Transparency Mask
E	Map and Plane Mask

1. All or part of these registers can change automatically.
2. The BITBLT ports (23C4 and 23C5) are accessed as extended registers. Refer to Extended Register Access, Section 16.

TABLE 18-1 BITBLT REGISTERS INDEX

18.1 CONTROL AND STATUS

18.1.1 BITBLT Control - Part 1, Index 0

BITS	FUNCTION
15:12	0000 (Index)
11	BITBLT Activation/Status*
10	BITBLT Direction
9:8	BITBLT Addressing Mode
7:6	BITBLT Destination/Source Linearity
5:4	BITBLT Destination Select
3:2	BITBLT Source Format
1:0	BITBLT Source Select

* Bit 10 is automatically reset when BITBLT is complete.

Bits 15:12

Index 0.

Bit 11

BITBLT Activation Status

Writing a one to this bit starts a BITBLT operation using the currently loaded register values. This bit is reset automatically when the BITBLT operation is complete. Therefore, reading a 1 from this bit indicates that a BITBLT operation is in progress.

Writing a 0 to this bit will not start a BITBLT operation but may be useful in "quick start" mode to set the other bits in the register for the coming series of quick-start operations.

CAUTION

Writing a 0 to this bit while a BITBLT operation is in progress may cause unexpected and unrecoverable results.

0 = Do not start BITBLT (write), BITBLT complete (read).
1 = Start BITBLT (write), BITBLT in progress (read).

13

Bit 10

BITBLT Direction

0 = BITBLT direction is top to bottom and left to right.
1 = BITBLT direction is bottom to top and right to left.

Bits 9:8

BITBLT Address Mode

00 = Planar Mode (includes monochrome modes).
01 = Packed mode (includes text and 256-color modes).
1x = Reserved for future expansion.

Bits 7:6

BITBLT Destination/Source Linearity

When the Destination or Source region of a BITBLT operation is specified as linear, each row of that region is considered to begin at the doubleword immediately following the doubleword containing the last pixel of the proceeding row. The alignment of the first pixel in each line is the same. No doubleword will straddle two lines and there may be gaps at unused pixels between adjacent lines.

Bit 7 controls the destination area and bit 6 controls the source area.

0 = Region is rectangular.
1 = Region is linear.

Bits 5:4

BITBLT Destination Select

00 = Destination is screen memory.
10 = Destination is system I/O location.
1x = Reserved for future expansion.

Bits 3:2

BITBLT Source Format

00 = Source format is color.
10 = Source format is monochrome from color comparators.
10 = Source format is fixed color (filled rectangle).
11 = Source format is monochrome from host.

Bits 1:0

BITBLT Source Select

00 = Source is screen memory.
10 = Source is system I/O location, 32 bits.
1x = Reserved for future expansion.

18.1.2 BITBLT Control - Part 2, Index 1

BITS	FUNCTION
15:12	0001(Index)
11	Enable Line Drawing
10	BITBLT Interrupt Enable
9	X or Y Major
8	Y Direction
7	BITBLT Quick Start
6	BITBLT Update Destination
5:4	BITBLT Pattern Select
3	BITBLT Monochrome Transparency
2	BITBLT Transparency Polarity
1	Reserved, must be 0
0	BITBLT Transparency Enable

Bits 15:12

Index 1

Bit 11

Enable Line Drawing

0 = Enable any other BITBLT function
1 = Enable Line Drawing

Bit 10

BITBLT Interrupt Enable

0 = Do not interrupt on completion of BITBLT.
1 = Interrupt on completion of BITBLT.

Bits 9

X or Y Major (Valid only when bit 11 is set to 1)

0 = X Major
1 = Y Major

Bits 8

Y direction (Valid only when bit 11 is set to 1)

0 = Down
1 = Up

Bit 7

BITBLT Quick Start

When bit 7 is set, BITBLT starts automatically as soon as the BITBLT Destination Low register (Index 4) is written; unless, automatic destination update is enabled for BITBLT. If automatic destination update is enabled, BITBLT starts automatically when the BITBLT Source Low Register (Index 2) is written.

Quick Start permits a chain of BITBLT operations to be performed with one less register write operation than would otherwise be required. All other bit in the BITBLT Control Register operate as they were last written, and the BITBLT activation bit is physically set and can be read back normally.

0 = BITBLT starts on when explicitly enabled.
1 = BITBLT starts automatically when the destination register is written or when the source register is written if destination update is enabled.

Bit 6

BITBLT Update Destination

A host doing multiple BITBLT operations only needs to update the registers that change from one BITBLT to the next. Most BITBLT registers do not change unless written to by the host. The exceptions are the two BITBLT Destination Registers (Index 4 and 5) and the status bit in the BITBLT Control Register (Index 0).

When bit 6 of this register is set, the BITBLT Destination Registers are automatically updated at the end of each BITBLT operation. When updated the registers point to the rectangular region immediately to the right of the previous destination region. When the destination region is specified as linear rather than rectangular, the destination registers point to the location immediately past the previous destination region. This feature specifically improves text output operations.

0 = Do not update destination on completion of BITBLT operation.
1 = Update destination on completion of BITBLT operation.

Bits 5:4

BITBLT Pattern Select

00 = Patterns are not used.
01 = 8x8 patterns are used for source.
1x = Reserved for future expansion.

Bit 3

Monochrome Transparency

0 = Monochrome transparency is not enabled.
1 = Monochrome transparency is enabled.

Bit 2

BITBLT Transparency Polarity

0 = Matching pixels are transparent.
1 = Matching pixels are opaque.

Bit 1

Reserved, must be set to 0.

Bit 0

BITBLT Transparency Enable

0 = Destination transparency is not enabled.
1 = Destination transparency is enabled.

18.2 SOURCE AND DESTINATION

The BITBLT Source Low and BITBLT Source High registers specify the source address for BITBLT operations. The BITBLT Destination Low and BITBLT Destination High registers specify the destination address for BITBLT operations. The high and low fields of each register pair are concatenated to form a 21-bit address pointing to the starting corner of the source or destination region.

The starting corner for the source and destination will be either the top-left or bottom-right corner. The corner specified must be coordinated with the BITBLT Direction bit of the BITBLT Control Register.

When the source and destination regions do not overlap, BITBLT can be started in either corner. When these regions do overlap, the corner and direction must be selected to prevent parts of the source region from being overwritten by the destination array before they are copied.

When the BITBLT Update Destination bit in the BITBLT Control Register is set, the host should not read the BITBLT Destination Registers while a BITBLT operation is in progress. This is because the BITBLT Destination Registers will change just before the end of the operation.

When the BITBLT Quick Start bit in the BITBLT Control Register is set, writing to the BITBLT Destination Registers may automatically start BITBLT operations.

18.2.1 BITBLT Source Low, Index 2

BITS	FUNCTION
15:12	0010 (Index)
11:0	BITBLT Source Position, Bits 11:0
NOTE: For Line Drawing, XSTEP uses bits 9:0 only.	

18.2.2 BITBLT Source High, Index 3

BITS	FUNCTION
15:12	0011 (Index)
11:9	Reserved, must be 0
8:0	BITBLT Source Position, Bits 20:12
NOTE: For Line Drawing, RSTEP uses bits 9:0 only.	

18.2.3 BITBLT Destination Low, Index 4

BITS	FUNCTION
15:12	0100 (Index)
11:0	BITBLT Destination Position, Bits 11:0

18.2.4 BITBLT Destination High, Index 5

BITS	FUNCTION
15:12	0101 (Index)
11:9	Reserved, must be 0
8:0	BITBLT Destination Position, Bits 20:12

18.3 ADDRESS MAPPING

The source and destination addresses are partially mode dependent. Addresses represent the character or pixel at the starting corner of the move, which may be the top-left or bottom-right corner.

18.3.1 Monochrome and Planar Modes

CPU ADDRESS	BITBLT REGISTER ADDRESS	DISPLAY MEMORY LOCATION (ALL MAPS)
A0000	0	Location 0, bit 7 (leftmost pixel).
	1	Location 0, bit 6
⇓		
	7	Location 1 bit 0 (rightmost pixel)
A0001	8	Location 1, bit 7
⇓		
A????	2M-1	Location 256K -1, bit 0[1]
[1]Last location in a 1 MB system. Smaller system memory configurations have fewer display memory locations.		

18.3.2 Packed Modes

CPU ADDRESS	BITBLT REGISTER ADDRESS	DISPLAY MEMORY LOCATION (ALL MAPS)
A0000	0	Map 0, Location 0 (leftmost pixel)
A0001	1	Map 1, Location 0
A0002	2	Map 2, Location 0
A0003	3	Map 3, Location 0
A0004	4	Map 0, Location 1 (leftmost pixel)
⇓	⇓	⇓
A0007	7	Map 3, Location 1 (rightmost pixel)
⇓		
A????	1M-1	Map 3, Location 256K -1[1]
[1]Last location in a 1 MB system. Smaller system memory configurations have fewer display memory locations.		

The locations referred to in the previous lists are the CPU address offsets in bytes from the top of display memory for any given mode. For example, where display memory starts at CPU address A0000h, location 123h would correspond to CPU address A0123h. Where display memory is divided into pages, the location is calculated as if all pages were consecutive. For example, with display memory pages of 64 Kbytes, location 10123h would correspond to CPU address A0123h in the second page of the display memory.

When the source or destination of a BITBLT operation is not a memory location, the corresponding pair of position registers are unused and may contain any value, except that the two or three low order bits of the BITBLT Source Low Register are still used to specify a source alignment of the data.

18.4 DIMENSIONS AND ROW PITCH

18.4.1 BITBLT Dimension X, Index 6

BITS	FUNCTION
15:12	0110 (Index)
11:0	BITBLT Dimension X[1]

NOTES:
1. For BITBLT Dimension X, the legal range is 1 to 2K pixels
2. For Line Drawing, Delta -X uses bits 9:0 only.

The BITBLT Dimension X register specifies the width of the rectangular region to be copied.

In Line Drawing mode, this register specifies the length of the line in the X- coordinate.

In Graphics Modes, this value is expressed in pixels.

In Text Modes, this value is expressed in the number of characters multiplied by eight (even though each character is stored using only two bytes).

18.4.2 BITBLT Dimension Y, Index 7

BITS	FUNCTION
15:12	0110 (Index)
11:0	BITBLT Dimension Y*

NOTES:
1. For BITBLT Dimension Y, the legal range is 1 to 2K pixels
2. For Line Drawing, Delta -Y uses bits 9:0 only.

The BITBLT Dimension Y register specifies the width of the rectangular region to be copied.

In Line Drawing mode, this register specifies the length of the line in the Y- coordinate.

In Graphics Modes, this value is the height of the rectangular region expressed in pixels.

In Text Modes, this value is the height of the region expressed in character rows.

18.4.3 BITBLT Row Pitch, Index 8

BITS	FUNCTION
15:12	1000 (Index)
11:0	BITBLT Row Pitch*

* In Packed Mode, the two low order bits of this field must be zero.
In Planar Mode, the three low order bits of this field must be zero.

The BITBLT Row Pitch Register specifies the linear offset from any location in a given row to the same location in the next row. This offset is in the same units as the source and destination fields to which it applies.

When both the source and destination are rectangular regions, the BITBLT Row Pitch value applies to both regions. When either or both are not rectangular, the offset does not apply to that range.

13

18.5 FOREGROUND AND BACKGROUND COLORS

The BITBLT Foreground and Background registers specify 8-bit or 4-bit digital colors to be used when expanding monochrome source areas. Also, the foreground color can be specified as the source of a BITBLT to produce a filled rectangle.

18.5.1 BITBLT Foreground Color, Index A

BITS	FUNCTION
15:12	1010 (Index)
11:8	Reserved
7:0	BITBLT Foreground Color*
* In Planar Mode, only bits 3:0 are used to specify color.	

18.5.2 BITBLT Background Color, Index B

BITS	FUNCTION
15:12	1011 (Index)
11:8	Reserved
7:0	BITBLT Background Color*
* In Planar Mode, only bits 3:0 are used to specify color.	

18.6 MAP AND PLANE MASK

The BITBLT Mask Register controls both the plane and map masks used in BITBLT.

The BITBLT Map Mask field specifies a 4-bit mask that prevents data in the specified maps from being updated. This mask is needed for BITBLT in all text modes to prevent font data from being overwritten in a character-attribute and vice versa move. This also applies to VGA mode F, and it can be used in VGA modes 4, 5, and 6 for partial hardware support. In addition, it can be used in VGA modes D, E, 10, 11, and 12 and extended Planar modes as a Plane Mask.

The BITBLT field specifies an 8-bit mask that prevents data in the specified planes from being updated. It is useful in VGA mode 13 and in extended Packed modes when Plane masking is desired.

18.6.1 BITBLT Mask - VGA, Index E

BITS	FUNCTION
15:12	1110 (Index)
11:8	Reserved
7:0	BITBLT Plane Map Mask Mode*
* In Planar Mode, only bits 3:0 are used.	

BITS 3:0	BITBLT MAP MASK
XXX0	Map 0 Disabled
XXX1	Map 0 Enabled
⇓	⇓
0XXX	Map 3 Disabled
1XXX	Map 3 Enabled

BITS 7:0	BITBLT PLANE MASK
XXXX XXX0	Plane 0 Disabled
XXXX XXX1	Plane 0 Enabled
⇓	⇓
0XXX XXXX	Plane 7 Disabled
1XXX XXXX	Plane 7 Enabled

18.7 RASTER OPERATIONS

The BITBLT Raster Operation Register specifies a bitters logical operation to be performed on the source and destination fields. These fields are always active and must be loaded with the appropriate value even when a simple source copy is to be performed.

18.7.1 BITBLT Raster Operation, Index 9

BITS	FUNCTION
15:12	1001 (Index)
11:8	BITBLT Raster Operation (abcd in Table 18-3).
7:0	Reserved

All BITBLT operations apply a source color, pattern, or area to a destination region. The result, which is written to the destination, is a logical function of the source and destination pixels for each location.

The Raster Operation code is defined as follows:

The source (S) and Destination (D) form a 2-bit value. Table 18-2 lists the logical results of these combined Source and Destination values.

The four 1-bit results from Table 18-2 form the Raster Operation code (abcd). The 'a' in the code is defined as the high order bit.

While the Raster Operation code represents a two-input operation (any two results form one code), both inputs are not always relevant to the operation. For example, codes 0011 (source copy) and 1100 (inverted source copy) are independent of the destination value.

S	D	RESULT
0	0	a
0	1	b
1	0	c
1	1	d

TABLE 18-2 RESULTS OF COMBINED SOURCE AND DESTINATION VALUES

RASTER OP CODE (abcd)	FUNCTION	RASTER OP CODE (abcd)	FUNCTION
0000	Zero	1000	NOR
0001	AND	1001	XNOR
0010	$S \bullet \overline{D}$	1010	Inverted Destination
0011	Source	1011	$S+\overline{D}$
0100	$\overline{S} \bullet D$	1100	Inverted Source
0101	Destination	1101	$\overline{S}+D$
0110	XOR	1110	NAND
0111	OR	1111	One

TABLE 18-3 RASTER OPERATION CODE FUNCTIONS

18.8 PATTERNS

The WD90C24 has a special mode to accelerate the copying of 8x8 source pattern. In this mode, an 8x8 full-color or monochrome pattern can be repetitively applied to a large destination region in an efficient manner.

To perform a pattern copy, the host first writes the 8x8 pattern to display memory in a linear fashion, usually in a non-visible location, depending on the current addressing mode as described in Sections 18-4 and 20. The host then loads the BITBLT Source Registers with the location of pixel within the pattern corresponding to the top-left corner of the destination region. The BITBLT Pattern Select field of the BITBLT Control Register must be set to 8x8 patterns.

To specify a monochrome pattern, the host must write a color pattern in the current mode, planar or packed, and then use the control registers to specify a single plane of the source to be used.

13

18.8.1 BITBLT Pattern Storage - Monochrome and Planar Modes

In planar mode, the 8x8 source pattern must be stored in display memory in a 32-byte aligned area. It is stored as 64 consecutive pixels, not as a rectangular region. When performing the pattern copy, the source address may point to any pixel with the 64-pixel region. This pixel is anchored to the top-left corner of the destination region, and the pattern wraps to the right and down from that point.

REGISTER ADDRESS	DISPLAY MEMORY CONTENTS
⇓	
n - 1	Any data
n* to n+7	All maps, top row of 8x8 pattern
n+8 to n+15	All maps, second row of 8x8 pattern
⇓	
n+56 to n+63	All maps, bottom row of 8x8 pattern
n+64 to...	Any data
*n must be a multiple of 64	

18.8.2 BITBLT Pattern Storage - Packed Modes

In packed mode, the 8x8 source pattern must be stored in display memory in a 64-byte aligned area. It is stored as 64 consecutive bytes, not as a rectangular region. When performing the pattern copy, the source address may point to any pixel with the 64-pixel region. This pixel is anchored to the top-left corner of the destination region, and the pattern wraps to the right and down from that point.

REGISTER ADDRESS	DISPLAY MEMORY CONTENTS
⇓	
n - 1	Any data
n*	Top row of 8x8 pattern (left-most pixel)
n+1	All maps, second row of 8x8 pattern
⇓	
n+7	
n+8	
⇓	
n+63	All maps, bottom row of 8x8 pattern
n+64	Any data
*n must be a multiple of 64	

18.9 MONOCHROME TO COLOR EXPANSION

When the source of a BITBLT operation is monochrome, each 0 in the source region is replaced with the specific background color, while each 1 is replaced with the foreground color. All other processing options, including mask and raster operations, remain active and operate on the expanded colors.

When the source is specified as a fixed color, the entire destination will be filled with the foreground color, subject to masks, raster operations, and destination transparency. Filled rectangles are generated in this manner.

When a monochrome source is generated by the color comparators, color destination transparency is generally not available since the transparency color registers are in use.

18.10 EXTRACTING MONOCHROME DATA

Monochrome data can be extracted from color data read from display memory by the color comparators. Data extracted in this manner is replicated to each plane or map as if it had been read from memory.

Also, monochrome data can be extracted from host data when the BITBLT source is the I/O port. In this case, each 32-bit word written to the I/O port is treat in the same manner as if it was read from display memory. Alternately, the host may send monochrome data through the I/O port that does not require extraction (refer to Section 18.14).

To extract a single plane from a color source field, the BITBLT Transparency Color Register should be loaded with FFh (all ones), while the BITBLT Transparency Mask Register should be loaded with a 0 in the map or plane position to be extracted, and with a 1 in all other positions.

Monochrome data is usually extracted as a specific bit of each 4-bit or 8-bit pixel. However, the color comparators can be used to extract any color, or any maskable group of colors, into the monochrome color 1, with all other colors returning a monochrome 0.

When the Monochrome Transparency bit is set in the BITBLT Control Register, monochrome source pixels of 0 do not modify the destination, regardless of any selected raster operation.

The Transparency Enable and Polarity bits in this register have no effect on the monochrome data extraction.

18.11 COLOR TRANSPARENCY

Color transparency is the concept that a certain color or range of colors in the source or destination field of a BITBLT are actually transparent, with the rest being opaque. Transparent source colors do not overwrite the background. Opaque destination colors cannot be overwritten. A common simplified form of source transparency is the logical OR of the source and destination, in which the source field of zero is effectively a transparent color, since when ORed with the destination, it does not change.

Color destination transparency is supported by the WD90C24, in addition to the more limited monochrome transparency described elsewhere.

18.11.1 BITBLT Transparency Color, Index C

The BITBLT Transparency Color Register specifies an 8-bit or 4-bit color to be used as the transparency color.

BITS	FUNCTION
15:12	1100 (Index)
11:8	Reserved
7:0	BITBLT Transparency Color*
* In Planar Mode, only the four low order bits (3:0) are used.	

18.11.2 BITBLT Transparency Mask, Index D

The BITBLT Transparency Mask Register specifies an 8-bit or 4-bit mask for use in comparison with the transparency color.

BITS	FUNCTION
15:12	1101 (Index)
11:8	Reserved
7:0	BITBLT Transparency Mask*
* In Planar Mode, only the four low order bits (3:0) are used.	

The pixels of the destination are compared with the transparency color under control of the transparency mask. Each bit of the Transparency Mask Register that is set to 1 makes the corresponding bit of the Transparency Color Register a "don't care."

The BITBLT Transparency Enable bit of the BITBLT Control Register, Index 1 specifies whether color transparency is enabled or disabled. The BITBLT transparency polarity bit specifies whether the pixels matching the transparency color are considered transparent. In this case, only destination pixels matching the transparent color can be overwritten, or transparent, and only non-matching pixels cannot be overwritten.

18.12 FILLED RECTANGLES

Filled rectangles can be drawn efficiently by the BITBLT hardware. A filled rectangle is a BITBLT with a source of a fixed color. To draw a filled rectangle, the host sets the Source Format field in the BITBLT Control Register (Index 0) to "fixed color" and the Foreground Color Register (Index A) to the desired fill color. A source address is not required. All other BITBLT options are available in a normal manner.

18.13 SYSTEM MEMORY TO DISPLAY MEMORY OPERATION

To copy data from system memory to display memory, the host may specify the source of a BITBLT as a system I/O location rather than display memory. In this case, display memory reads come from the 32-bit readback latch written by the host.

After starting the BITBLT operation, the host writes a series of doublewords to the readback latch. The 32-bit register is accessed by two consecutive writes to the 16-bit BITBLT I/O port, with the low order word of this register written first. Also, this port may be accessed by two 8-bit writes as long as the even port is accessed first. At the beginning of each BITBLT operation, the internal pointer is reset to the low-order word.

When a source read is required and data from the host is unavailable, the WD90C24 suspends the BITBLT operation until the data becomes available. Similarly, when the host attempts to write the register before the previous data in it has been processed, the WD90C24 hold off the host.

Conceptually, the 32 bits written by the host exactly replace the 32 bits that would have been read from display memory. Just like the destination, the source may have any alignment. The two or three low-order bits (Packed or Planar Mode) of the BITBLT Source Low Register (Index 2) specify the alignment of the source region. The other bit of the BITBLT Source Low Register may have any value. That is, the pixel of the source word pointed to by those low-order bits corresponds to the first pixel of the destination.

NOTE

Source writes from the host are always performed in 32-bit groups. However, the data are written to a 16-bit port. Therefore, the host must always perform two consecutive 16-bit I/O writes to the port even when the remaining width is less than four or eight bits.

Similar to display memory, no source doubleword from the host may straddle two lines of the destination.

18.14 DISPLAY MEMORY TO SYSTEM MEMORY OPERATIONS

To copy data from display memory to system memory, the host may specify the destination of a BITBLT as a system I/O location rather than display memory. In this case, display memory writes are replaced by writes to a 32-bit register read by the host.

This 32-bit register is accessed by two consecutive reads of the 16-bit BITBLT I/O port. The low-order word of this register id read first. Also, this port may be accessed by two 8-bit reads, as long as the even port is accessed first. At the beginning of each BITBLT operation, the internal pointer is reset to the low-order word.

When a destination write is required and the host has not read data from the previous write, the WD90C24 suspends the BITBLT operation until the host catches up. Similarly, when the host attempts to read the register before data are available, the WD90C24 holds off the host.

Conceptually, the 32 bits read by the host exactly match the 32 bits that would have been written to the display memory. Unlike outputting to display memory, the destination is always doubleword aligned. That is, the first pixel of the source corresponds to the first pixel of the destination.

NOTE

Source reads by the host are always performed in 32-bit groups. However, the data are read from a 16-bit port. Therefore, the host must always perform two consecutive 16-bit I/O reads from the port, even when less that 32-bits remain on the current line.

Similar to display memory, no destination double-word to the host may straddle two lines of the source.

18.15 SYSTEM MEMORY TO DISPLAY MEMORY TRANSFERS WITH COLOR EXPANSION

The host may transfer monochrome data from system memory to display memory and, in the process, expand it to any two colors or any one color plus transparent.

To accomplish this, the host set the BITBLT Source Select field in the BITBLT Control Register (Index 0) to "System I/O Location" and the BITBLT Source Format field to "Monochrome From Host." If transparency is desired, the Monochrome Transparency bit is also set. Also, the BITBLT Foreground and Background Color Registers (Index A and B) may be set.

The host then issues a series of 16-bit I/O writes to the BITBLT I/O port which are expanded to eight 4-bit pixels. The remaining eight high-order bits are ignored. In Packed Mode, the four low-order bits are expanded to four 8-bit pixels and the remaining 12 bits are ignored.

The low-order bits of the BITBLT Source Register (Index 2) work as any other system-to- video memory transfers.

No source word may straddle two lines of the destination. All other BITBLT options work normally in this mode.

19.0 HARDWARE LINE DRAWING

19.1 STRIP LINE DRAWING

Strip line drawing is Microsoft Windows compatible.

19.1.1 Conditions

The following conditions must be met for strip line drawing to function properly.

- The line drawing must always start from left to right, regardless of other parameters such as top to bottom, bottom to top, Y-major, or X-major.
- The software must set up the BLT registers as if it were performing a rectangular fill.
- Software must also provide information concerning XSTEP, RSTEP, DELTA X, DELTA Y, X-DIRECTION, Y-DIRECTION, X-MAJOR, AND Y-MAJOR.

19.1.2 Altered BLT Register Functions

Some BLT register functions are altered during line draw. The altered register functions are given in the following list

BLT INDEX	BLT FUNCTION	LINE DRAW FUNCTION
1.11	Reserved	1 = Line Draw 0 = other BLT function
1.8	Reserved	0 = X-Major 1 = Y-Major
1.9	Reserved	Y-Direction
2	Source Low	XSTEP [9:0]
3	Source High	RSETP [9:0]
6	DIMX	DELTA X
7	DIMY	DELTA Y

TABLE 19-1 BLT FUNCTIONS ALTERED BY LINE DRAW

19.1.3 Line Draw Operation

At the start of Line Draw operation, the software must set up all necessary BLT registers for proper operation.

After completion of a Line Draw operation, BLT Register Index 1 must be set to 0 before the next BLT operation.

13

20.0 APPLICATIONS AND PROGRAMMING

This section contains descriptions of the different applications and how to program the WD90C24. The following subjects are included:

- Using the Hardware Cursor in 16-Bit per Color Mode
- BITBLT Operations in VGA Modes 4, 5, and 6
- BITBLT Operations in Text Mode
- Patterns
- Using BITBLT in 16-Bit Per Color Mode
- Support for Kanji Characters
- Reading and Writing the VGA Readback Latches
- Changing Monochrome Sources to Color
- Extracting Monochrome Data
- Color Transparency
- Drawing Filled Rectangles
- System Memory to Video Memory Operations
- Video Memory to System Memory Operations
- System Memory to Display Memory Transfers with Color Expansion
- Control and Status
- Automatic Destination Update
- Quick Start Mode
- Aborted BITBLT
- Registers Access

20.1 USING THE HARDWARE CURSOR IN 16-BIT PER COLOR MODE

The hardware cursor, while not specifically designed for "high-color" mode operation, can still be used, with certain limitations in that mode.

The hardware cursor is unaware of the existence of high-color mode, but can still be used by specifying two adjacent 2-bit pixel codes for each high-color cursor pixel. A "transparent" high-color pixel would be specified using two adjacent transparency codes, ("1010"), while a "color" high-color pixel would usually be specified using adjacent primary and secondary color codes, such as "0100". The desired 16-bit cursor color would then be split between the 8-bit primary and 8-bit secondary color registers. Inversion is also available as "1111" but the results might not be visually desirable.

Note that this limits the effective maximum cursor width in high-color mode to 32 pixels. Further, the cursor origin and position are defined in terms of 8-bit, not the displayed 16-bit, pixels. Therefore, these values should be horizontal multiples of two.

A developer could use the secondary and auxiliary color registers to create additional cursor colors by mixing cursor codes within a 16-bit pixel region. However, the developer should be aware of the effects of inversion in systems that use one bit to switch between false color and high-color modes on a pixel-by-pixel basis.

20.2 BITBLT OPERATIONS IN VGA MODES 4, 5, AND 6

VGA modes 4, 5, and 6 are partially supported on the WD90C24. Since these modes are not commonly used in Windows™, the additional hardware required to support the even/odd scan line offset technique employed in these modes is not supported.

However, a BITBLT operation in these VGA modes can often be broken up into two or three BLT operations, each of which operates on a contiguous area of memory.

When the vertical offset between source and destination is an even number of rows, the desired operation can be broken into two BITBLTs, one for the even rows and one for the odd rows. This requires careful consideration of the register parameters, especially the BITBLT Dimension Y register.

Where the offset is an odd number of rows, it may still be possible to break up the operation into only two BITBLTs, providing that there is no overlap between the source and destination regions. This is because information is being "swapped" between the even and odd scan line regions.

Where source and destination do overlap, it may be possible to use a scratch space in off-screen memory and break up the operation into three BITBLTs.

Another possibility is to break up a BITBLT into a series of one-line high operations that might be referred to as Line-BLTs. In this manner, a BITBLT may be simulated by the driver as a series of Line-BLTs.

20.3 BITBLT OPERATIONS IN TEXT MODE

BITBLT acceleration is available in VGA text modes, Text mode BITBLTs generally consist of moving only character and attribute data (in maps 0 and 1), while leaving the font data (in maps 2 and 3) alone. The BITBLT mask is set to prevent update to those maps. For this reason, planar (not packed) mode must be used, Similarly, the BITBLT mask can be set to move only character data, or only font data.

Each display memory location consists of four bytes: one character, one attribute, and two font plane bytes the are not part of the character but happen to fall in the same location as the character, but on maps 2 and 3. In planar mode, this is a space of eight pixels. Therefore, the source and destination of a character BLT must be multiples of 8. The X dimension is the number of character columns to be copied times 8, but the Y dimension is simply the number of character rows with no multiplying. The row pitch is set to the CPU address offset between character rows times 8.

20.4 USING BITBLT IN 16-BIT PER COLOR MODE

The BITBLT hardware can be used in 16-bit per color "High-color" mode with a few changes and a few limitations.

High-color BITBLTs should be performed in packed mode, remembering that each high-color pixel takes up two adjacent normal packed pixels. The BITBLT Source and Destination registers should point to the first byte of the respective regions. Generally, the values in these register pairs is double the corresponding values for normal packed mode.

In a right-to-left BITBLT in high-color mode, the source and destination values must point to the second byte of each region.

The BITBLT dimensions is twice number of pixel columns, but the correct number of pixel rows. The Row Pitch Register contains eight times the number of bytes between rows on the screen. Linear source and destination operate normally.

Monochrome to color expansion is not, as a rule, usable. Neither is plane masking. Raster operations are available but often produce undesired results. Similarly, color transparency is rarely usable.

Pattern fills are available, however, the effective pattern is only 4x8 pixels. This may be usable where an 8x8 pattern is identical in the left and right halves.

Filled rectangles are available in two ways. First, where the desired fill color is the same in the high and low bytes (generally meaning all black or all white), rectangle fill can be used normally.

In the more general case of filling a rectangle with an arbitrary 16-bit color, the host should create a 4x8 pattern of the fill color and use pattern fills to create the rectangle.

Host I/O BITBLTs can operate normally by treating each 16-bit high-color pixel as two adjacent, aligned 8-bit packed mode pixels.

The user is cautioned regarding implementations that use one of the 16 bits in a high-color pixel as a switch between false color and high-color, as no mask exists to protect this flag bit during operations.

20.5 PATTERNS

The device has a special mode to accelerate the copying of 8x8 source patterns. In this mode, an 8x8 full-color or monochrome pattern can be repetitively applied to a large destination area in an efficient manner.

To perform a pattern copy, the host writes the 8x8 pattern to display memory in a linear fashion, depending on the current addressing mode, as defined below. The host then loads the *BITBLT Source* registers with the location of the pixel within the pattern corresponding to the top-left corner of the destination region. The *BITBLT Source Select* field of the BITBLT *Control* register must be set to source pattern.

To specify a monochrome pattern, the host must write a color pattern in the current (planar or packed) mode, and then use the control registers to specify a single plane of the source to be used.

In planar mode, the 8x8 source pattern must be stored in display memory in an 32-byte aligned area. It is stored as 64 consecutive pixels, not as a rectangular region. When performing the pattern copy, however, the source address may point to any pixel within the 64-pixel region. This pixel is anchored to the top-left corner of the destination region, and the pattern wraps to the right and down from that point

BITBLT PATTERN STORAGE - MONOCHROME AND PLANAR MODES

ADDRESS	DISPLAY MEMORY CONTENTS
fl	
n- 8	(any data)
n*	All maps, top row of 8x8 pattern
n+ 8	All maps, second row of 8x8 pattern
fl	
n+ 56	All maps, bottom row of 8x8 pattern
n+ 64	(any data)
fl	

*'n' *must be a multiple of* 64

In packed mode, the 8x8 source pattern must be stored in display memory in a 64-byte aligned area. It is stored as 64 consecutive bytes, not as a rectangular region. When performing the pattern copy, however, the source address may point to any pixel within the 64-pixel region. This pixel is anchored to the top-left corner of the destination region, and the pattern wraps to the right and down from that point.

BITBLT PATTERN STORAGE - PACKED MODES	
ADDRESS	DISPLAY MEMORY CONTENTS
fl	
n-1	(any data)
n*	Top row of 8x8 pattern, left most pixel
n+1	Top row of 8x8 pattern, second pixel
fl	
n+7	Top row of 8x8 pattern, right most pixel
n+8	Second row of 8x8 pattern, left most pixel
fl	
n+63	Bottom row of 8x8 pattern, right most pixel
n+64	(any data)
*'n' *must be a multiple of 64*	

20.5.1 Using BITBLT For Arbitrary Sized Patterns

While the BITBLT hardware specifically accelerates 8x8 patterns, patterns of arbitrary size can be accelerated by use of the BITBLT, albeit to a lesser degree.

To copy an arbitrary size pattern to a destination region, the pattern should be stored in non-visible memory as a rectangular region, not a linear strip. With destination update enabled, one copy of the pattern should be BLTed to the top-left corner of the destination. The BITBLT source is then set to point to the pattern now in the destination region.

A series of BLTs is then performed, each doubling the width of the patterned area, simply by adjusting the X dimensions register. (The last of this series of BLTs fill out the destination region.)

A new series of BLTs is then performed, taking the horizontally complete pattern and doubling it in height each time. Note that destination update should be turned off, and the destination must be set for each new BLT. (Again, the final BLT is probably not a double of the last one as it fills out the region.)

20.5.2 Patterns Built On-Screen

Normally, a pattern to be used in BITBLT is stored in a non-visible portion of display memory. This requires an aligned strip of 32 or 64 bytes to be available.

Where this is not available, it is often possible to still perform a pattern BLT by placing the pattern in the last line of the destination region. This can be done if the raster operation is a source copy (or source inversion), and if the destination region can accommodate the specified aligned strip on a single line. This technique works because each row of the pattern is read at the beginning of the row in which it is used, and the pattern wont be overwritten until it after it has been read for the last time.

Where a full strip is unavailable, the destination can be broken up into a series of line-BLTs, with one line the pattern, requiring only 4 or 8 aligned bytes, placed on each destination line before the BLT is started for that line. This method is substantially slower than other pattern BLTs.

An acceptable alternative might be to write the pattern in a visible portion of memory, first saving the underlying area and restoring it after the BLT. This momentary "borrowing" of a visible region might be visible to the user. This might be lessened by using the last line of the destination and saving and restoring only those regions that overhand the destination.

20.5.3 Use Of Patterns In Text Mode

Patterns may be in text mode to quickly set character and/or attribute bytes in a rectangular area to a common value. A pattern space must be created containing eight consecutive copies of the four-byte area consisting of the character, the attribute, and two "font map" bytes, all aligned to a 64-pixel boundary. The BITBLT map mask is then used to protect the font maps. This pattern should be created in off-screen memory.

If an off-screen pattern space is not available, one may be created on screen by loading an aligned group of 8 character/attribute pairs within the destination area, then pointing to that as the pattern source.

If the first character of the destination space happens to be on an 8-byte boundary (such as the conventional top of screen) then, as long as the destination is at least 8 character wide, only the first character/attribute pair must be loaded, and the BITBLT operation "creates its own pattern" as it goes along. This also works if the destination is less than 8 characters wide, but is still wider than it is high.

If this is not possible, then the operation can be performed one character row at a time, loading the first character of each row to be used as an on-screen pattern.

Filled rectangles have a very limited application in text mode, but could be used to clear out a section of a font map or to set a section of a character or attribute map to all zeroes or all ones. Different values are not easily set in this manner because, in order to protect the font maps, planar mode, rather than packed mode, must be used.

20.6 SUPPORT FOR KANJI CHARACTERS

The BITBLT hardware can support generation of Kanji characters very efficiently. The common implementation of Kanji characters calls for a character box of 28x28 pixels with five possible scoring lines for each character box.

Kanji characters are best drawn in two passes. The first pass draws the characters while erasing any old ones. The second pass adds the score lines.

The Kanji font should be stored in non-visible display memory. Since the font is monochrome, multiple characters can be stored one per plane, one under the other. The color compare registers are used to switch between banks of characters stored on different planes.

A group of 32 special characters is generated along with the font, consisting of all possible combinations of scoring lines.

The dimension registers are loaded with the size of the character box. Foreground and background colors are set as desired. Destination update and quick BLTs are enabled.

For each character row, the source destination registers are set to the beginning of the row, and monochrome expansion is enabled. A series of quick BLTs is performed, one per character, by loading the source address of each desired character. If a font-plane change is required, this is done before loading the source registers, which start the BLT automatically.

After the character row is complete, the destination registers are reset to the beginning of the row. Monochrome transparency is enabled, and a second pass is done over the character drawn to add score lines as needed, one special score-line character per Kanji character.

Where a Kanji character requires no score lines, either a BLT of a special "blank" score-line character is performed, or the destination registers may simply be updated to skip the position. The driver may add additional intelligence to skip entire character rows or parts where score lines are not required.

20.7 READING AND WRITING THE VGA READBACK LATCHES

The 32-bit VGA readback latch may be written and read by the host. This ability is primarily useful in context switching.

To write the contents of the VGA readback latches, the host may set up a system-to-display memory transfer with a width and height of 1 pixel. The BITBLT Mask is then set to all zeroes to prevent destination update. The host then starts the operation and word pointer is reset on power-up and whenever a BITBLT operation begins or ends.

This technique is guaranteed only for this revision of the device, and may or may not work on future revisions.

20.8 TRANSFERRING MONOCHROME SOURCES TO COLOR

When the source of a BITBLT operation is monochrome, each'0' in the source region is replaced with the specified background color, while each'1' is replaced with the foreground color. All other processing options, including masks and raster operations remain active and operate on the expanded colors.

When the source is specified as a fixed color, the entire destination is filled with the foreground color, subject to masks, raster operations, and destination transparency. Filled rectangles are generated in this manner.

When a monochrome source is generated by the color comparators, color destination transparency is generally not available, since the transparency color registers are in use.

20.9 EXTRACTING MONOCHROME DATA

Monochrome data can be extracted from color data read from display memory by the color comparators. Data so extracted is replicated to each plane or map as if it was so read from the memory.

When extracted, monochrome data is usually extracted from color data in display memory. However, when the BITBLT source is the system I/O location, monochrome data can be extracted in the same way.

To extract a single plane from a color source field, load the *BITBLT Transparency Color* register with 'FFF' (all ones), and load the *BITBLT Transparency Mask* register with a '0' in the map or plane position to be extracted, and load a '1' in all other positions. (As described in the section on color transparency, one of the two fields of each of these registers is actually a don't care at any given time.)

Monochrome data is usually extracted as a specific bit of each 4- or 8-bit pixel. However, the color comparators can be used to extract any color, or any maskable group of colors, into the monochrome color '1', with all other colors returning a monochrome '0'.

When the *Monochrome Transparency* bit is set in the *BITBLT Control* register, monochrome source pixels of '0' do not affect the background, regardless of the selected raster operation.

The *Transparency Enable* and *Polarity* bits in this register have no effect on monochrome data extraction.

20.10 COLOR TRANSPARENCY

Color transparency is the concept that a certain color or range of colors in the source or destination field of a BITBLT are actually "transparent", with the rest being "opaque". Transparent source colors do not overwrite the background. Opaque destination colors cannot be overwritten. A common simplified form of source transparency is the logical OR of source and destination, in which a source field of zero is effectively a transparent color since it does not change the destination when ORed with it.

20.11 DRAWING FILLED RECTANGLES

Color destination transparency is supported on this device, in addition to the more limited monochrome transparency described elsewhere.

Filled rectangles can be drawn very efficiently by the BITBLT hardware. A filled rectangle is simply a BITBLT with a source of a fixed color. To draw a filled rectangle, the host sets the *Source Format* field in the *BITBLT Control* register to "fixed color", and the *Foreground Color* register to the desired fill color. A source address is not required. All other BITBLT options are available normally.

20.12 SYSTEM MEMORY TO VIDEO MEMORY OPERATIONS

To copy data from system memory to host memory, the host may choose to have the source of a BITBLT come from a system I/O location rather than from display memory. In this case, display memory reads from the 32-bit readback latch written by the host.

After starting the BITBLT operation, the host writes a series of doublewords to the readback latch. This 32-bit register is accessed by two consecutive writes to the 16-bit *BITBLT I/O* port. The low-order word of this register is written first. This port may itself be accessed by two 8-bit writes, as long as the even port is accessed first. At the beginning of each BITBLT operation, the internal pointer is reset to the low-order word.

When a source read is required and data from the host is unavailable, the device suspends the BITBLT operation until data becomes available. Similarly, when the host attempts to write the register before previous data in it has been processed, the device holds off the host.

Conceptually, the 32 bits written by the host exactly replace the 32 bits that would have been read from the display memory. Just like the destination, the source may have any alignment. The 2 or 3 (packed or planar mode) low-order bits of the *BITBLT Source Low* register specify the alignment of the source region. The other bits of the register may have any value. That is, the pixel of the source word pointed to by those low-order bits corresponds to the first pixel of the destination.

Source writes from the host are always performed in 32-bit groups, however the data is written to a 16-bit port. Therefore, the host must always perform two 16-bit I/O writes to the port at a time, even when the remaining destination width is less than 4 (or 8) pixels. Just like display memory, no source doubleword from the host may straddle two lines of the destination.

20.13 VIDEO MEMORY TO SYSTEM MEMORY OPERATIONS

To copy data from host memory to system memory, the host may choose to have the source of a BITBLT written to a system I/O location rather than to display memory. In this case, display memory writes is replaced by writes to a 32-bit register read by the host.

This 32-bit register is accessed by two consecutive reads of the 16-bit *BITBLT I/O* port. The low-order word of this register is read first. This port may itself be accessed by two 8-bit read, as long as the even port is accessed first. At the beginning of each BITBLT operation, the internal pointer is reset to the low-order word.

When a destination write is required and the host has yet to read data from the previous write, the device suspends the BITBLT operation until the host catches up. Similarly, when the host attempts to read the register before data is available, the device holds off the host.

Conceptually, the 32 bits read by the host exactly match the 32 bits that would have been written to the display memory. Unlike outputting to display memory, the destinations always doubleword aligned, that is, the first pixel of the source corresponds to the first pixel of the destination.

Source reads by the host are always performed in 32-bit groups, however the data is read from a 16-bit port. Therefore, the host must always perform two 16-bit I/O reads to the port at a time, even when less than 32 bits remain in the current line.Just like display memory, no destination doubleword to the host may straddle two lines of the source.

20.14 SYSTEM MEMORY TO DISPLAY MEMORY TRANSFERS WITH COLOR EXPANSION

The host may transfer monochrome data from system memory to display memory, expanding it in the process to any two colors, or to one color plus transparent.

To accomplish this, the host sets the BITBLT Source Select field in the BITBLT Control register to "system I/O location" and the BITBLT Source Format field to "monochrome from host". If transparency is desired, the Monochrome Transparency bit is also set. The BITBLT Foreground and Background Color registers may also be set.

The host then issues a series of 16-bit I/O writes to the BITBLT I/O port are expanded to eight 4-bit pixels. The remanding 8 high-order bits are ignored. In packed mode, the 4 low-order bits are expanded to four 8-bit pixels, and the remaining 12 bits ignored.

The low-order bits of the BITBLT Source register work as in other system-to-video memory transfers, and again no source word may straddle two lines of the destination. All other BITBLT options word normally in this mode.

20.15 CONTROL AND STATUS

BITBLT Control Part 1	Index 0
D1:0	BITBLT source select
D3:2	BITBLT source format
D5:4	BITBLT destination select
D6	BITBLT source linearity
D7	BITBLT destination linearity
D9:8	BITBLT addressing mode
D10	BITBLT direction
D11	BITBLT activation/status*
D15:12	0000 (index)
	* this bit is automatically reset when BITBLT is completed

D1:0	BITBLT Source Select
0 0	Source is screen memory
0 1	Source is system memory
1 0	Source is system I/O location, 32 bits
	other values are reserved for future expansion

13

D3:2	BITBLT Source Format
0 0	Source format is color
0 1	Source format is monochrome from color comparators
1 0	Source format is fixed color (filled rectangle)
1 1	Source format is monochrome from host

D9:8	BITBLT Address Mode
0 0	Planar mode (includes monochrome modes)
0 1	Packed mode (includes text and 256-color modes)
1 1	(reserved for adder test)
	other values are reserved for future expansion

D5:4	BITBLT Destination Select
0 0	Destination is screen memory
0 1	Destination is system memory
1 0	Destination is system I/O location
	other values are reserved for future expansion

D10	BITBLT Direction
01	BITBLT direction is top to bottom, left to right
1	BITBLT direction is bottom to top, right to left

D6	BITBLT Source Linearity
0	Source area is rectangular
1	Source area is linear

D11	BITBLT Activation/Status
0	Abort BITBLT/ BITBLT completed
1	Begin BITBLT / BITBLT in progress*
* This bit is reset automatically when BITBLT is completed. Writing a '0' to this bit aborts a BITBLT operation in progress	

D7	BITBLT Destination Linearity
0	Destination area is rectangular
1	Destination area is linear

BITBLT Control - Part 2 Index 1	
D0	BITBLT transparency enable
D1	(reserved, must be 0)BITBLT transparency select
D2	BITBLT transparency polarity
D3	BITBLT monochrome transparency
D5:4	BITBLT pattern select
D6	BITBLT update destination
D7	BITBLT quick start
D9:6	(unused)
D9	BITBLT auto-direction detect mode
D10	BITBLT interrupt enable
D11	BITBLT VGA register unlock
D11	(unused)
D15:12	0001 (index)

D0	BITBLT Transparency Enable
0	Transparency is not enabled
1	Transparency is enabled

D1	BITBLT Transparency Select
0	Destination pixels control transparency
1	Source pixels control transparency

D2	BITBLT Transparency Polarity
0	Matching pixels are transparent
1	Matching pixels are opaque

D3	BITBLT Monochrome Transparency
0	Monochrome transparency is not enabled
1	Monochrome transparency is enabled

D5:4	BITBLT Pattern Select
0 0	Patterns are not used
0 1	8x8 patterns are used for source
	other values are reserved for future expansion

D6	BITBLT Update Destination
0	Do not update destination on completion of BITBLT
1	Update destination on completion of BITBLT

13

D7	BITBLT Quick Start
0	BITBLT starts only when explicitly enabled
1	BITBLT starts automatically when destination* register is written
	* or source register, if destination update is enabled

D10	BITBLT Interrupt Enable
0	Do not interrupt on completion of BITBLT
1	Interrupt on completion of BITBLT

D11	BITBLT VGA Register Unlock
0	All VGA registers are VGA-compatible
1	BITBLT VGA overlay registers are writable

20.16 AUTOMATIC DESTINATION UPDATE

A host doing multiple BITBLTs need only update those registers that change from one BITBLT to the next. Most BITBLT registers never change unless written by the host. The exceptions to this rule are the two BITBLT Destination registers and the status bit in the BITBLT Control register.

When the BITBLT Update Destination bit in the BITBLT Control register is set, the BITBLT Destination registers are automatically updated at the end of each BITBLT operation to point to the rectangular region immediately to the right of the previous destination region. This is specifically aimed at improving text output operations. When the destination area is specified as linear rather than rectangular, the destination registers points to the location immediately past the previous destination area.

20.17 QUICK START MODE

When the BITBLT Quick Start bit is set in the BITBLT Control register, then BITBLT starts automatically as soon as the BITBLT Destination Low register is written, unless automatic destination update is enabled for BITBLT, in which case the BITBLT starts automatically when the BITBLT Source Low register is written.

This mode permits a chain of BITBLT operations to be performed with one less register write operation than would otherwise be required. All other bits in the BITBLT Control register operates as they were last written, and the BITBLT Activation bit is physically set and can be read back normally.

20.18 ABORTED BITBLT

The host may abort a BITBLT in progress by resetting the BITBLT Activation bit in the BITBLT Control register. The operation then terminates within a few memory clocks.

When a BITBLT is aborted, the destination registers are generally be unchanged, unless the operation was coincidentally aborted near the very end.

Aborted BITBLTs cannot generally be continued, since it is unknown what remains to be copied, and even if it were known, the region remaining to be copied might not be rectangular. Further, BITBLTs that use certain logical operations or transparency settings might not produce correct results if simply repeated with the original parameters.

20.19 REGISTER ACCESS

If the Auto-Increment Disable bit in the Index Control register is reset, consecutive reads to the Register Access port returns consecutively indexed registers within the same register block. Registers is read in ascending order through register F (the 16th register in the block), followed by register 0 and cycling indefinitely as long as reads continue. Registers that do not exist return unknown data when read.

If the Auto-Increment Disable bit is set, consecutive reads return the same indexed register.

21.0 EMBEDDED CLOCK GENERATOR

This section describes the Embedded Clock Generator that is capable of providing various video memory clock (MCLK) and video dot clock (VCLK) frequencies.

21.1 FEATURES

The main features of the Embedded Clock Generator are:

- Dual clock generator based on the Western Digital WD90C65 VGA Clock Generator.
- Generates 15 preprogrammed video clock frequencies (including 25.057 MHz and 28.189 MHz) that are derived from a 14.31818 MHz system clock reference frequency.
- Generates 8 preprogrammed memory clock frequencies.
- External clock mode allows users to bypass the internal PCLK to input a video clock and memory clock.
- With the WD90C24 in powerdown mode, the clock generator is placed in a low-current state.
- The AVDD1 analog power supply to the clock generator can be powered off when the system is in powerdown mode.

21.2 DESCRIPTION

The Embedded Clock Generator is a dual clock synthesizer capable of generating two different internal clock frequencies under firmware control. One clock frequency is for the video memory clock, and the other frequency is for the video dot clock. The operating frequencies are derived from a 14.31818 MHz system clock input available in IBM PC/XT/AT and Personal System/2 computers.

The VCLK may be one of 15 internally generated frequencies as shown in Table 21-1. The VCLK frequency is selected via Paradise Extended Register PR68 (3C5h, index 31h) bits 4:3 and VGA Miscellaneous Output Register 3C2h bits 3:2 (Write Only).

The VCLK is also user-programmable in a range from 25.057 MHz to 85.014 MHz, in 447.443 KHz increments. The user can also enter an external clock mode that bypasses the clock generator by generating VCLK and MCLK from primary chip inputs. The internal clock generator is held in low-current mode during external clock mode.

VSEL				N	VCLK FREQ (MHz)
3C5.31h		3C2h			
BIT 4	BIT 3	BIT 3	BIT 2		
0	0	0	0	67	29.979
0	0	0	1	173	77.408
0	0	1	0	--	See note
0	0	1	1	179	80.092
0	1	0	0	56	25.057
0	1	0	1	63	28.189
0	1	1	0	146	65.327
0	1	1	1	81	36.242
1	0	0	0	89	39.822
1	0	0	1	112	50.114
1	0	1	0	94	42.060
1	0	1	1	99	44.297
1	1	0	0	71	31.768
1	1	0	1	80	35.795
1	1	1	0	167	74.723
1	1	1	1	112	50.114
NOTE: Programmable frequency					

TABLE 21-1 VCLK SELECTION

The MCLK may be one of 8 internally generated frequencies, which are selected via PR68 (3C5h, index 31h) bits 2:0 as shown in Table 21-2.

MSEL			N	MCLK FREQ (MHz)
3C5.31h				
BIT 2	BIT 1	BIT 0		
0	0	0	67	29.979
0	0	1	74	33.111
0	1	0	80	35.795
0	1	1	84	37.585
1	0	0	94	42.060
1	0	1	99	44.297
1	1	0	106	47.429
1	1	1	110	49.219

TABLE 21-2 MCLK SELECTION

The various VCLK and MCLK operating frequencies are achieved by multiplying the 14.31818 MHz input frequency by a factor of N/32. External filter components are attached to the VCAP and MCAP pins for the internal phase lock loops.

21.2.1 System Bus Interface

The only system bus interface used by the clock generator is the CKIN pin (14.31818 MHz).

21.2.2 Firmware Interface

The clock generator receives inputs from three internal registers. VGA register 3C2h bits 3:2 hold the VSEL1:0 bits. These bits allow for compatibility in switching between standard frequencies. Paradise Register 3C5h, index 31h, bits 4:3 hold the VSEL2:3 bits. The MSEL2:0 bits are held by the same 3C5h, index 31h register in bits 2:0. Paradise Register PR69 (3C5h, index 32h) holds the 8-bit N value of the user-programmable VCLK. The N value is calculated by dividing the desired frequency (in MHz) by 0.447443 MHz. The resulting value must be rounded to give an integer value, which is loaded into Paradise Register 3C5h, index 32h. At reset the default frequencies are 25.057 Mhz for VCLK and 44.297 Mhz for MCLK.

21.2.3 Analog Interface

MCAP and VCAP are analog filters. The component values of the filters are critical. Care must be taken to ensure proper values over the entire operating range desired for the final product. Figure 21-1 shows the filter circuit. The capacitor tolerances are ±20%. The resistor tolerance is ±2%.

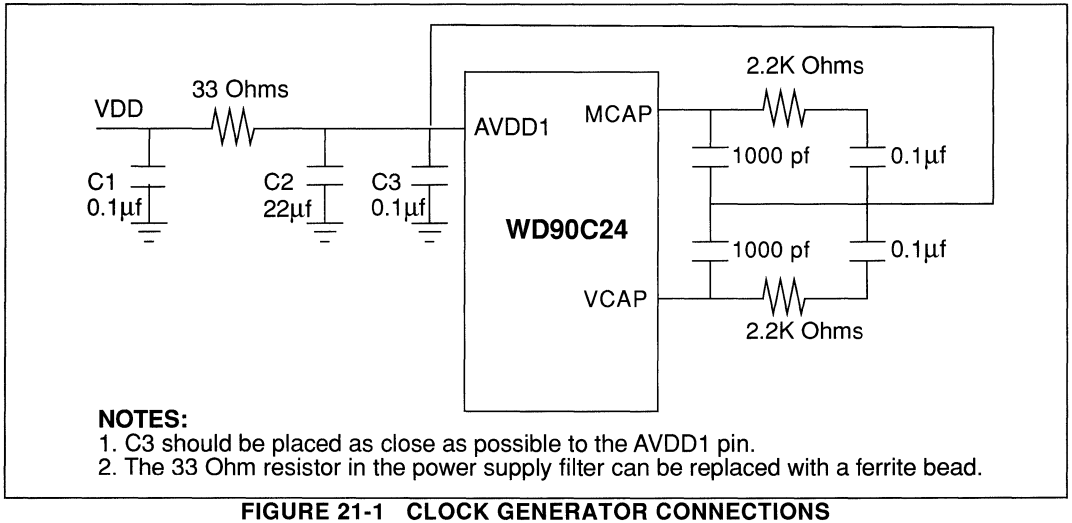
21.2.4 External Clock Mode

Setting EXCKEN high enables the external clock mode, which allows the user the option to bypass the internal clock generator. The following list defines the pins in external clock mode.

INTERNAL PCLK MODE	EXTERNAL CLOCK MODE
EXCKEN=0	EXCKEN=1
XMCLK (not used)	MCLK
XVCLK (not used)	VCLK
FPUSR1	VCLK1
CKIN (14.318mhz)	VCLK2

21.2.5 ISO Support

For ISO monitor operation, unlock PR68 (3C5h, index 31h) by writing 50h to PR72 (3C5h, index 35h), and then write 11b to PR68 register bits 4:3.



NOTES:
1. C3 should be placed as close as possible to the AVDD1 pin.
2. The 33 Ohm resistor in the power supply filter can be replaced with a ferrite bead.

FIGURE 21-1 CLOCK GENERATOR CONNECTIONS

13

22.0 WD90C24 CONFIGURATION REGISTERS

Memory data lines AMD[15:0} and BMD[15:0] are used to input configuration data (CNF[31:0]) at system power-on or reset. External pull-up or pull-down resistors are used to set the state of the internal configuration registers. The resistors cause bits to be set in internal registers, which then establish the operating configuration at start up. Some configuration bits are contained in non-writable registers while others can be modified after start up. The non-writable bits set features such as "bus type" that are not modified after start up. Configuration bits CNF15:12, CNF10, and CNF0 can be changed by software after start up. The memory data lines (AMD[15:0] and BMD[15:0]) are alll internally pulled up by 100 Kohm resistors.

Table 22-1 lists the WD90C24 Configuration Registers by the register number, and then provides the signal pin name and the CNF register function.

CONFIGURATION (CNF) REGISTER	CONNECTOR PIN NAME	REGISTER FUNCTION
0*	AMD0	BIOS ROM Mapping
1*	AMD1	General Purpose
2	AMD2	Works with CNF17 to determine the host interface (refer to Table 4-2).
3*	AMD3	Video Clock Source Control
7:4*	AMD7:AMD4	General Purpose Status
8	AMD11	Select Operating Voltage
9*	AMD9	46E8h/3C3h Select
10	AMD10	Reserved
11*	AMD8	General Purpose
12*	AMD12	General Purpose
13	AMD13	Used with CNF14 and CNF 16 to determine the memory mode configuration (refer to Table 4-1).
14	AMD14	Used with CNF13 and CNF 16 to determine the memory mode configuration (refer to Table 4-1).
15*	AMD15	General Purpose
16	BMD0	Used with CNF13 and CNF 14 to determine the memory mode configuration (refer to Table 4-1).
17	BMD1	Works with CNF2 to determine the host interface (refer to Table 4-2).
18	BMD2	Reserved
19	BMD3	Reserved
20	BMD4	486 Host Indicator Bit
21	BMD5	External Ready Sampling Control Bit
27:22	BMD[11:6]	Configuration bits for VLBI Register 2DF1[5:0]
31:28	BMD[15:12]	Configuration bits for VLBI Register 2DF0[7:4]]
* These configurations are WD90C31 compatible.		

TABLE 22-1 WD90C24 CONFIGURATION REGISTERS

PIN NAME	READ/ WRITE	CNF	REGISTER [BITS]	DESCRIPTION
AMD0*	R/W	0^+	PR1[0]	0 = (No Pulldown) Enable BIOS ROM
				1 = (Pulldown) BIOS ROM is Mapped Out
AMD1*	R	1^+	PR1[1]	0 = (No Pulldown) General Purpose
				1 = (Pulldown) General Purpose
AMD2	---	2	---	0 = (Pulldown) Works with CNF17 to determine the host interface (refer to Table 4-2).
				1 = (Pullup) Works with CNF17 to determine the host interface (refer to Table 4-2).
AMD3*	---	3^+	---	0 = (Pulldown) Select VCLK1 and VCLK2 as Input
				1 = (Pullup) Select VCLK1 and VCLK2 as Output
AMD4*	R	4^+	PR5[4]	0 = (Pulldown) General Purpose Status Bit
				1 = (Pulldown) General Purpose Status Bit
AMD5*	R	5^+	PR5[5]	0 = (Pulldown) General Purpose Status Bit
				1 = (Pulldown) General Purpose Status Bit
AMD6*	R	6^+	PR5[6]	0 = (Pulldown) General Purpose Status Bit
				1 = (Pulldown) General Purpose Status Bit
AMD7*	R	7^+	PR5[7]	0 = (Pulldown) General Purpose Status Bit
				1 = (Pulldown) General Purpose Status Bit
AMD8*	R/W	11^+	---	0 = (Pulldown) Force All Voltage Detectors to 5 VDC
				1 = (No Pulldown) Allow Automatic Voltage Detect
AMD9*	R/W	9^+	---	0 = (Pulldown) 3C3h or 46Eh I/O Port
				1 = (Pulldown) 3C3h or 46Eh I/O Port
AMD10	R/W	10	PR1[1]	0 = (No Pulldown) Reserved
				1 = (No Pulldown) Reserved
AMD11*	R/W	8^+	PR5[3]	0 = (No Pulldown) Analog/TTL Display Status Bit
				1 = (No Pulldown) Analog/TTL Display Status Bit
AMD12	R/W	12^+		0 = (Pulldown) Reserved
				1 = (No Pulldown) Reserved
AMD13	R/W	13	PR11[5]	0 = (Pulldown) Select Memory Mode Configuration
				1 = (No Pulldown) Select Memory Mode Configuration (Refer to Table 4-1)
AMD14	R/W	14	PR11[6]	0 = (Pulldown) Select Memory Mode Configuration
				1 = (No Pulldown) Select Memory Mode Configuration (Refer to Table 4-1)

TABLE 22-2 WD90C24 CONFIGURATION REGISTER BITS, CNF[31:0]

PIN NAME	READ/ WRITE	CNF	REGISTER [BITS]	DESCRIPTION
AMD15*	W	15+	---	0 = (Pulldown)
				1 = (No Pulldown) General Purpose for BIOS
BMD0	R	16	PR11[7]	0 = (Pulldown) Select Memory Mode Configuration
				1 = (No Pulldown) Select Memory Mode Configuration (Refer to Table 4-1)
BMD1	---	17	PR11[4]	0 = (Pulldown) Works with CNF2 to determine the host interface (refer to Table 4-2).
				1 = (No Pulldown) Works with CNF2 to determine the host interface (refer to Table 4-2).
BMD2	R/W	18	PR18[0]	0 = (Pulldown) Select Display Panel (Refer to Panel Select Table)
				1 = (No Pulldown)
BMD3	R/W	19	PR18[1]	0 = (Pulldown)
				1 = (No Pulldown) Select Display Panel (Refer to Panel Select Table)
BMD4	---	20	---	0 = (Pulldown) 486 Host Indicator Bit
				1 = (No Pulldown)
BMD5	---	21	---	0 = (Pulldown) External Ready Sampling Bit
				1 = (No Pulldown)
BMD[11:6]	---	27:22	2DF1[5:0]	0 = (Pulldown) Configuration Bits for VLBI Registers 2DF1[5:0]
				1 = (No Pulldown)
BMD[15:12]	---	31:28	2DF0[7:4]	0 = (Pulldown) Configuration Bits for VLBI Registers 2DF0[7:4]
				1 = (No Pulldown)

NOTES:

* These configurations are WD90C31 compatible.

+ A pulldown resistor sets these bits to 1.

TABLE 22-2 WD90C24 CONFIGURATION REGISTER BITS, CNF[31:0]

23.0 I/O MAPPING

This section provides the following information:

- A Description of WD90C24 I/O Mapping
- A list of I/O Mapping groups (Table 6-12)
- An I/O Mapping Group Diagram (Figure 6-31)

23.1 DESCRIPTION

The I/O Mapping allows the WD90C24 to enter a test mode where all of its pins are divided into groups with inputs and outputs. The path for each group goes from the input pin(s), through the WD90C24, and to the output pin. Each group can be treated as a separate resistive path to check for open and shorted circuits within the group and between groups. Table 23-1 lists each group (path) with its corresponding input and output pins.

The WD90C24 must meet the following four requirements in order to enter the I/O Mapping test mode.

- $\overline{\text{MEMR}}$ is LOW
- $\overline{\text{IOR}}$ is LOW
- CNF(2) is HIGH (AMD2 is pulled high)
- RESET is ACTIVE HIGH then goes LOW
- $\overline{\text{PWRDOWN}}$ is HIGH

If both $\overline{\text{MEMR}}$ and $\overline{\text{IOR}}$ are low at the same time, it becomes an illegal condition in ISA(AT) machines and a reserved condition in the PS/2 machines. AMD2 high ensures that WD90C24 is in ISA(AT) mode.

Reset controls a transparent latch as shown in Figure 23-1.

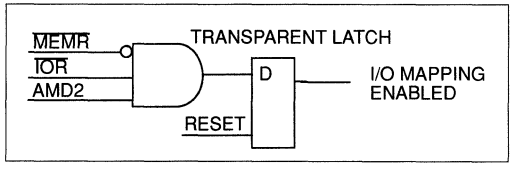


FIGURE 23-1 ENABLING I/O MAPPING ON THE WD90C24

Figure 23-2 provides a diagram of the I/O mapping groups (paths).

INPUT		OUTPUT	
PIN	NAME	PIN	NAME
1, 16	BMD0, BMD9	201	AMA0
3, 14	BMD1, BMD10	203	AMA1
6, 12	BM2, BMD11	205	AMA2
8, 9	BMD3, BMD12	207	AMA3
7, 11	BMD13, BMD4	208	AMA4
4, 13	BMD14, BMD5	206	AMA5
2, 15	BMD15, BMD6	204	AMA6
17, 52	BMD7, PD16	202	AMA7
18, 51	BMD8, PD17	200	AMA8
42, 47	PD24, PD20	198	$\overline{\text{ARAS}}$
41, 46	PD25, PD21	196	$\overline{\text{AWE}}$
40, 45	PD26, PD22	24	$\overline{\text{BRAS}}$
39, 44	PD27, PD23	22	$\overline{\text{BWE}}$
20, 23	$\overline{\text{BCASL}}$, $\overline{\text{BCASH}}$	25	$\overline{\text{BOE}}$
39	PD28	164	$\overline{\text{LCDENA}}$
37	PD29	165	PNLOFF
53, 115	SD15, SD5	123	STN13
54, 114	SD14, SD4	124	STN12
55, 112	SD13, SD3	126	STN11
56, 111	SD12, SD2	127	STN10

TABLE 23-1 I/O MAPPING GROUPS

13

INPUT		OUTPUT	
PIN	NAME	PIN	NAME
58, 110	SD11, SD1	128	STN9
59, 109	SD10, SD0	129	STN8
60, 75, 78	SD9, IRQ, $\overline{\text{ZWST}}$	119	XSCLK
61, 74	SD8, ALE	120	$\overline{\text{WPLT}}$
63, 85, 151	SLA17, SA5, SA29	137	VLD1
64, 86, 152	SLA18, SA6, SA30	136	VLD2
65, 87, 153	SLA19, SA7, SA31	135	VLD30
66, 89, 99	SLA20, SA8, $\overline{\text{IOW}}$	134	VUD0
67, 90, 98	SLA21, SA9, $\overline{\text{IOR}}$	133	VUD1
68, 91, 101	SLA22, SA10, $\overline{\text{MEMW}}$	132	VUD2
69, 92, 100	SLA23, SA11, $\overline{\text{MEMR}}$	131	VUD30
70, 71, 72	CLK486, $\overline{\text{IOCS16}}$, $\overline{\text{MEMCS16}}$	77	IOCHRDY
73, 117	SBHE, SD7	121	$\overline{\text{RPLT}}$
76, 116	$\overline{\text{EIO}}$, SD6	122	STN14
80, 93, 146	SA0, SA12, SA24	144	FR

TABLE 23-1 I/O MAPPING GROUPS

INPUT		OUTPUT	
PIN	NAME	PIN	NAME
81, 94, 147	SA1, SA13, SA25	143	FP
82, 94, 148	SA2, SA14, SA26	142	LP
83, 96, 149	SA3, SA15, SA27	140	SCLK
84, 97, 150	SA4, SA16, SA28	139	VLD0
103	XMCLK	172	VLBICS
161	EXCKEN	173	VSYNC
170	CKIN	167	FPUSR0
171	$\overline{\text{EBROM}}$	174	HSYNC
175	PCLK	106	VCLK2
177, 190	AMD0, AMD9	28	BMA0
179, 188	AMD1, AMD10	30	BMA1
181, 186	AMD2, AMD11	32	BMA2
183, 184	AMD3, AMD12	34	BMA3
182, 185	AMD13, AMD4	35	BMA4
180, 187	AND14, AMD5	33	BMA5
178, 189	AMD15, AMD6	31	BMA6
50, 191	PD18, AMD7	29	BMA7
49, 192	PD19, AMD8	27	BMA8
194, 197	$\overline{\text{ACASL}}$, $\overline{\text{ACASH}}$	199	$\overline{\text{AOE}}$

TABLE 23-1 I/O MAPPING GROUPS

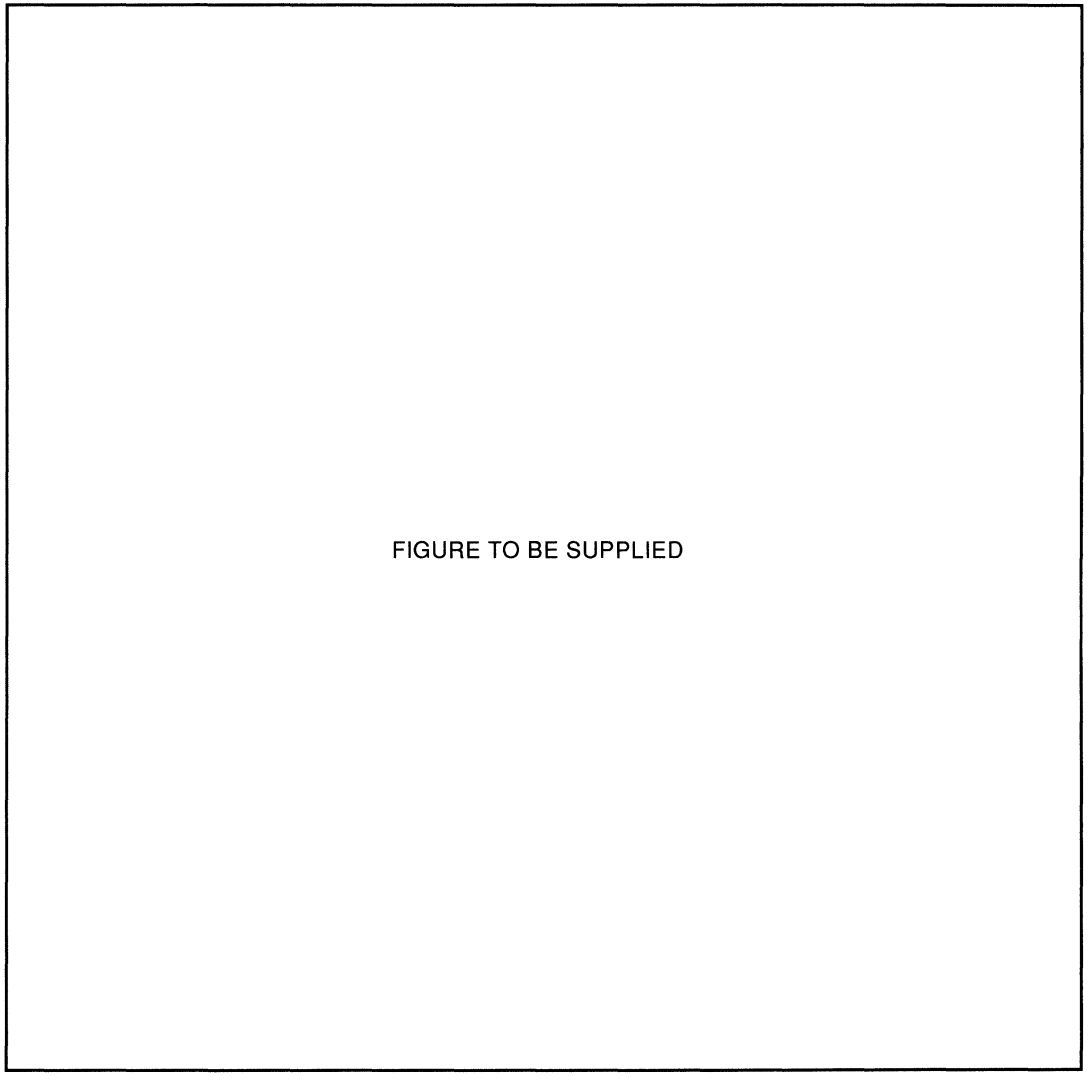


FIGURE 23-2 I/O MAPPING GROUP DIAGRAM

24.0 OPERATING SPECIFICATIONS

The operating temperature and voltage ranges are given in the following list. The DC and AC characteristics depend upon operation within the specified temperature and voltage ranges.

Operating Temperature Range	0°C to 70°C
Power Supply Voltage	3.0 VDC to 5.25 VDC

NOTES

1. All voltages are referenced to VSS (0V Ground).
2. Positive current flows into the referenced pin.

25.0 DC/AC CHARACTERISTICS

25.1 DC POWER DISTRIBUTION

The WD90C24 Controller supports supply voltages of 3.3 VDC or 5.0 VDC. In addition, the WD90C24 Controller operates with a mix of both supply voltages. This allows the WD90C24 to be used in situations where portions of the design operate at 3.3 VDC for power savings, while other portions operate at the traditional 5.0 VDC for interface compatibility. Table 25-1 lists the power level required for each power designator depending on which power configuration is used.Table 25-2 lists each WD90C24 pin with the associated signal name and its power designator.

POWER DESIGNATOR	OPERATING DC VOLTAGE			SYSTEM POWER DOWN DC VOLTAGE		
	3.3	5.0	MIXED	3.3	5.0	MIXED
VDD (Core)	3.3	5.0	3.3	0	0	0
PVDD	3.3	5.0	3.3	3.3	5.0	3.3
BVDD	3.3	5.0	3.3/5.0	0	0	0
MVDD	3.3	5.0	3.3/5.0	3.3	5.0	3.3/5.0
FPVDD	3.3	5.0	3.3/5.0	0	0	0
RVDD	3.3	5.0	3.3	0	0	0
AVDD1	3.3	5.0	3.3	0	0	0
AVDD2	3.3	5.0	3.3	0	0	0

TABLE 25-1 WD90C24 POWER DISTRIBUTION

When operating in the mixed voltage configuration, the following 3.3 VDC-powered buffers can be driven with 5.0 VDC signals:

RESET
CKIN
$\overline{\text{REFRESH}}$
$\overline{\text{PDOWN}}$

The following pins have internal pullup resistors (minimum value = 100 Kohms):

AMD[15:0]
SA[31:24]
BMD[15:0]
$\overline{\text{PDOWN}}$

The following pins have internal pulldown resistors (minimum value = 100 Kohms):

CLK496
CKIN

13

PIN NO.	NAME	POWER DESIGNATOR	PIN NO.	NAME	POWER DESIGNATOR
1	BMD0	MVDD	36	VSS	---
2	BMD15	MVDD	37	PD29	BVDD
3	BMD1	MVDD	38	PD28	BVDD
4	BMD14	MVDD	39	PD27	BVDD
5	VSS	---	40	PD26	BVDD
6	BMD2	MVDD	41	PD25	BVDD
7	BMD13	MVDD	42	PD24	BVDD
8	BMD3	MVDD	43	VDD	---
9	BMD12	MVDD	44	PD23	BVDD
10	VDD	---	45	PD22	BVDD
11	BMD4	MVDD	46	PD21	BVDD
12	BMD11	MVDD	47	PD20	BVDD
13	BMD5	MVDD	48	VSS	BVDD
14	BMD10	MVDD	49	PD19	---
15	BMD6	MVDD	50	PD18	BVDD
16	BMD9	MVDD	51	PD17	BVDD
17	BMD7	MVDD	52	PD16	BVDD
18	BMD8	MVDD	53	SD15	BVDD
19	MVDD	---	54	SD14	BVDD
20	$\overline{\text{BCASL}}$	MVDD	55	SD13	BVDD
21	VSS	---	56	SD12	BVDD
22	$\overline{\text{BWE}}$	MVDD	57	BVDD	---
23	$\overline{\text{BCASH}}$	MVDD	58	SD11	BVDD
24	$\overline{\text{BRAS}}$	MVDD	59	SD10	BVDD
25	$\overline{\text{BOE}}$	MVDD	60	SD9	BVDD
26	VDD	---	61	SD8	BVDD
27	BMA8	MVDD	62	VSS	---
28	BMA0	MVDD	63	SLA17	BVDD
29	BMA7	MVDD	64	SLA18	BVDD
30	BMA1	MVDD	65	SLA19	BVDD
31	BMA6	MVDD	66	SLA20	BVDD
32	BMA2	MVDD	67	SLA21	BVDD
33	BMA5	MVDD	68	SLA22	BVDD
34	BMA3	MVDD	69	SLA23	BVDD
35	BMA4	MVDD	70	CLK486	BVDD

TABLE 25-2 DC POWER DISTRIBUTION

PIN NO.	NAME	POWER DESIGNATOR	PIN NO.	NAME	POWER DESIGNATOR
71	IOCS16/BOFF	BVDD	106	VCLK2	RVDD
72	MEMCS16/PD31	BVDD	107	AVSS1	---
73	SBHE/CPURESET	BVDD	108	RVSS	---
74	ALE/NADS	BVDD	109	SD0	BVDD
75	IRQ/PD30	BVDD	110	SD1	BVDD
76	EIO/BE0	BVDD	111	SD2	BVDD
77	IOCHRDY/CPURDYN	BVDD	112	SD3	BVDD
78	ZWST/VLBIBUSY	BVDD	113	BVDD	---
79	VSS	---	114	SD4	BVDD
80	SA0/BE3	BVDD	115	SD5	BVDD
81	SA1/BE2	BVDD	116	SD6	BVDD
82	SA2	BVDD	117	SD7	BVDD
83	SA3	BVDD	118	VSS	---
84	SA4	BVDD	119	XSCLK/RGB17	FPVDD
85	SA5	BVDD	120	WPLT/RGB16	FPVDD
86	SA6	BVDD	121	RPLT/RGB15	FPVDD
87	SA7	BVDD	122	STN14/RGB14	FPVDD
88	RVDD	---	123	STN13/RGB13	FPVDD
89	SA8	BVDD	124	STN12/RGB12	FPVDD
90	SA9	BVDD	125	VDD	---
91	SA10	BVDD	126	STN11/RGB0	FPVDD
92	SA11	BVDD	127	STN10/RGB1	FPVDD
93	SA12	BVDD	128	STN9/RGB2	FPVDD
94	SA13	BVDD	129	STN8/RGB3	FPVDD
95	SA14	BVDD	130	FPVDD	---
96	SA15	BVDD	131	VUD3/RGB11	FPVDD
97	SA16	BVDD	132	VUD2/RGB10	FPVDD
98	IOR/DC	BVDD	133	VUD1/RGB9	FPVDD
99	IOW/BE1	BVDD	134	VUD0/RGB8	FPVDD
100	MEMR/MIO	BVDD	135	VLD3/RGB7	FPVDD
101	MEMW/WR	BVDD	136	VLD2/RGB6	FPVDD
102	AVDD1	---	137	VLD1/RGB5	FPVDD
103	XMCLK	BVDD	138	VLD0/RGB4	FPVDD
104	MCAP	AVDD1	139	VSS	---
105	VCAP	AVDD1	140	SCLK/XSCLK	FPVDD

TABLE 25-2 DC POWER DISTRIBUTION

PIN NO.	NAME	POWER DESIGNATOR	PIN NO.	NAME	POWER DESIGNATOR
141	RVDD	---	176	VSS	---
142	LP	FPVDD	177	AMD0	MVDD
143	FP	FPVDD	178	AMD15	MVDD
144	FR/BLANK/ENDATA	FPVDD	179	AMD1	MVDD
145	RVSS	---	180	AMD14	MVDD
146	SA24/VGACS	BVDD	181	AMD2	MVDD
147	SA25	BVDD	182	AMD13	MVDD
148	SA26	BVDD	183	AMD3	MVDD
149	SA27	BVDD	184	AMD12	MVDD
150	SA28	BVDD	185	AMD4	MVDD
151	SA29	BVDD	186	AMD11	MVDD
152	SA30	BVDD	187	AMD5	MVDD
153	SA31	BVDD	188	AMD10	MVDD
154	AVDD2	---	189	AMD6	MVDD
155	MDETECT/FSADJ	AVDD	190	AMD9	MVDD
156	VREF	AVDD	191	AMD7	MVDD
157	BLUE	AVDD	192	AMD8	MVDD
158	GREEN	AVDD	193	MVDD	---
159	RED	AVDD	194	$\overline{\text{ACASL}}$	MVDD
160	AVSS2	---	195	VSS	---
161	EXCKEN	PVDD	196	$\overline{\text{AWE}}$	MVDD
162	RESET/SYSRES	PVDD	197	$\overline{\text{ACASH}}$	MVDD
163	$\overline{\text{PDOWN}}$	PVDD	198	$\overline{\text{ARAS}}$	MVDD
164	$\overline{\text{LCDENA}}$	PVDD	199	$\overline{\text{AOE}}$	MVDD
165	PNLOFF	PVDD	200	AMA8	MVDD
166	$\overline{\text{REFRESH}}$/$\overline{\text{RDYIN}}$	PVDD	201	AMA0	MVDD
167	FPUSR0	PVDD	202	AMA7	MVDD
168	VCLK/FPUSR1	PVDD	203	AMA1	MVDD
169	PVDD	---	204	AMA6	MVDD
170	CKIN/XVCLK	PVDD	205	AMA2	MVDD
171	$\overline{\text{EBROM}}$/HRQ	BVDD	206	AMA5	MVDD
172	$\overline{\text{VLBICS}}$/$\overline{\text{PRDY}}$	BVDD	207	AMA3	MVDD
173	VSYNC	BVDD	208	AMA4	MVDD
174	HSYNC	BVDD	---	---	---
175	PCLK	BVDD	---	---	---

TABLE 25-2 DC POWER DISTRIBUTION

25.2 INTERNAL CLOCK DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
Vil	Input Low Voltage	Vss	0.8	V	
Vih	Input High Voltage	2.0	Vdd	V	
Iil	Input Leakage Current	--	±10	µA	Vss < Vin < Vdd
Cin	Input Pin Capacitance	--	8	pF	Fc = 1 MHz
Idd	AVDD1 & RVDD Supply Current for PCLK	--	40	mA	Vdd = 5.25 V

TABLE 25-3 DC TIMING CHARACTERISTICS

25.3 INTERNAL CLOCK AC CHARACTERISTICS

The following conditions apply to all of the AC parameters presented in this section:

- REFCLK = 14.31818 MHz
- All units are in nanoseconds (ns) unless otherwise specified.
- Maximum jitter within a range of 30 us after triggering on a 400 MHz scope.
- Internal CLK rise and fall time between 0.8 and 2.0V at the output of the PCLK.
- External Clock Mode rise and fall time between 0.8 and 2.0V.
- Internal duty cycle measured at 1.4V, at the output of the PCLK.
- External Clock Mode duty cycle measured at 1.4V.

SYMBOL	PARAMETER	MIN	MAX	NOTES
Reference Input Clock				
tr	Rise Time	--	10	0.8 to 2.0 VDC
tf	Fall Time	--	10	2.0 to 0.8 VDC
tj	Phase Jitter	--	1	
--	Duty Cycle	42.5%	57.5%	Measured at 1.4 V.
External Input Clock				
tr	Rise Time	--	3	0.8 to 2.0 VDC
tf	Fall Time	--	3	2.0 to 0.8 VDC
tjv	VCLK Jitter	--	3	
tjm	MCLK Jitter	--	5	
--	Duty Cycle	40%	60%	Measured at 1.4 V.
Internal MCLK & VCLK Timing				
tr	Rise Time	--	3	
tf	Fall Time	--	3	
tjv	VCLK Jitter	0	3	
tjm	MCLK Jitter	0	5	
--	Duty Cycle	40%	60%	Measured at 1.4 V.
--	Frequency Error	--	±0.5%	
--	Frequency Range	25	85	MHz

TABLE 25-4 AC TIMING CHARACTERISTICS

NOTE

Unless otherwise specified, AC Timing is with respect to Vil/Vih = 0.4/2.4 and Vol/Voh = 0.8/2.0.