

**W83310S-N/W83310G-N**



**Winbond**  
**Bus Termination Regulator**  
**W83310S-N**  
**W83310G-N**



## W83310S-N/W83310G-N Data Sheet Revision History

	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1	N.A.	02/Dec.	0.51	N.A.	The versions before 0.5 are only for internal reference.
2	3	03/Feb.	0.60	N.A.	Recommend circuit update
3	5	03/Mar.	0.61	N.A.	AC specification update
4	3	03/May	0.7	N.A.	Internal block diagram update
5	4,6	03/Jul.	0.71	N.A.	Recommend circuit update
6	4	03/Oct.	0.72	N.A.	<ul style="list-style-type: none"><li>AC specification update</li></ul>
7		06/Jan..	0.73	N.A.	<ul style="list-style-type: none"><li>Add Pb-free part no:W83310G-N</li></ul>

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**Table of Contents-**

- 1. GENERAL DESCRIPTION ..... 2
- 2. FEATURES ..... 2
- 3. APPLICATIONS ..... 2
- 4. PIN CONFIGURATION AND DESCRIPTION ..... 3
- 5. APPLICATION CIRCUIT ..... 4
- 6. INTERNAL BLOCK DIAGRAM ..... 5
- 7. ELECTRICAL CHARACTERISTICS ..... 6
  - 7.1 AC CHARACTERISTICS ..... 6
- 8. TYPICAL OPERATING WAVEFORM..... 7
- 9. PACKAGE DIMENSION ..... 8
- 10. ORDERING INFORMATION ..... 9
- 11. HOW TO READ THE TOP MARKING..... 9



## 1. GENERAL DESCRIPTION

The W83310S-N is a linear regulator which provides achieves 1.5Amp bi-directional sinking and driving capability for DDR SDRAM bus terminator application. The chip simply implement a stable power supply which can track half of input power dynamically for bus terminator with a single chip; that is the chip integrates two power MOSFETs. There is no any external power device needed. The W83310S-N is promoted with small footprint 8-SOP 150mil package. With W83301S-R/N design, a high integration, high performance, and cost-effective solution is promoted.

## 2. FEATURES

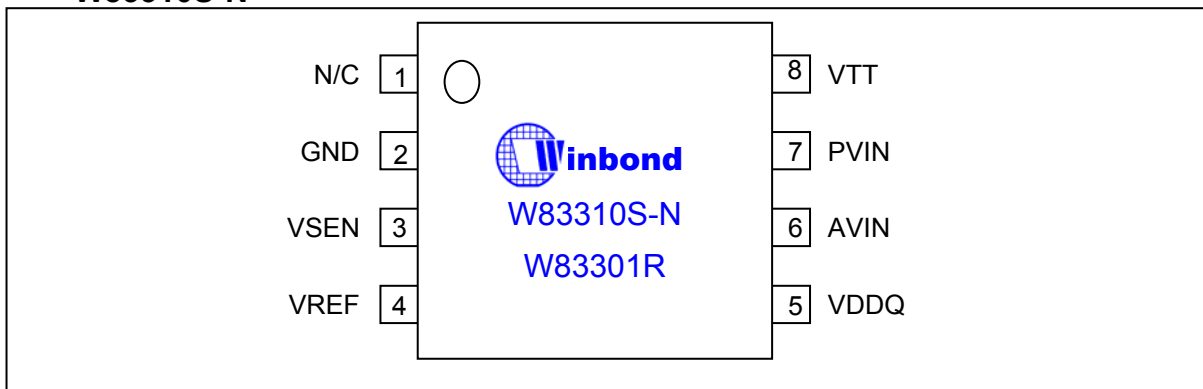
- Regulates a bi-directional power with driving and sinking capability
- Provides achieve 1.5Amp driving and sinking current
- Power MOSFET integrated
- Low external component count
- Low output voltage offset
- Operates with +5V,+3.3V and +2.5V control power
- Small package
- Low cost and easy to use

## 3. APPLICATIONS

- DDR Bus Termination Regulator
- Active Termination Bus
- SSTL-2
- SSTL-3

## 4. PIN CONFIGURATION AND DESCRIPTION

### -W83310S-N

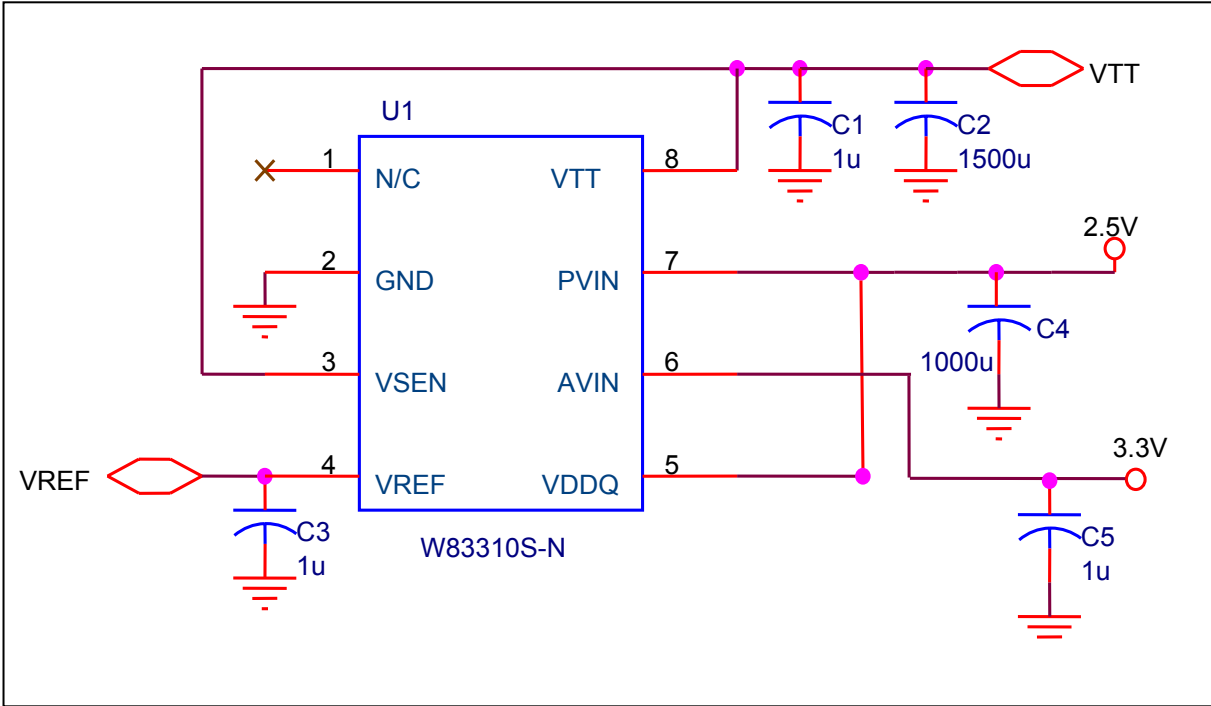


SYMBOL	PIN	FUNCTION
N/C	1	No internal connection.
GND	2	Ground.
VSENSE	3	Feedback pin for regulating VTT.
VREF	4	Internal reference voltage of VDDQ/2.
VDDQ	5	Input for internal reference equal to VDDQ/2.
AVIN	6	Analog input pin.
PVIN	7	Power input pin.
VTT	8	Output voltage for connection to termination resistors.

# W83310S-N/W83310G-N

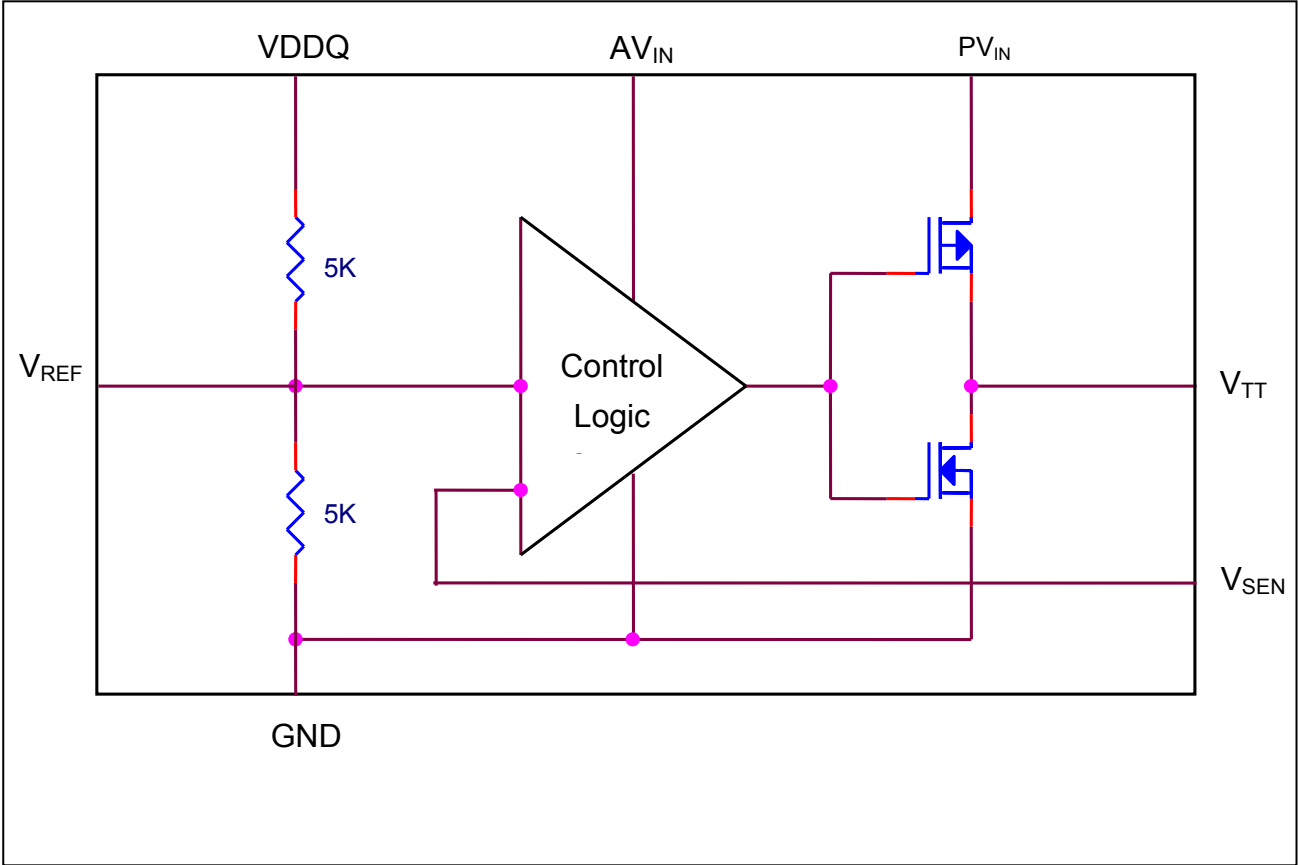


## 5. APPLICATION CIRCUIT -W83310S-N





6. INTERNAL BLOCK DIAGRAM  
-W83310S-N





## 7. ELECTRICAL CHARACTERISTICS

### 7.1 AC CHARACTERISTICS

W83310S-N						
<i>AVIN=3.3V; PVIN=2.5V is recommended, VDDQ =2.5V, VREF=1.25V, Cout=100uF, TA = 0°C to +70°C</i>						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Output Offset Voltage	$V_{OS}$	-5	0	+5	mV	$I_{OUT}=0A$
Load Regulation			0.8		%	Loading: 0A→1.5A
			0.8			Loading: 0A→-1.5A
Input Voltage Range	VDDQ		2.5		V	A specific power sequence should be followed that is $AV_{IN} \geq PV_{IN}$ during operating.
	PVIN	2.2	2.5	5.5		
	AVIN	2.2	3.3	5.5		
Operating Current of AVIN	IAVIN		0.5	1	mA	No Load ( $I_{OUT}=0A$ )

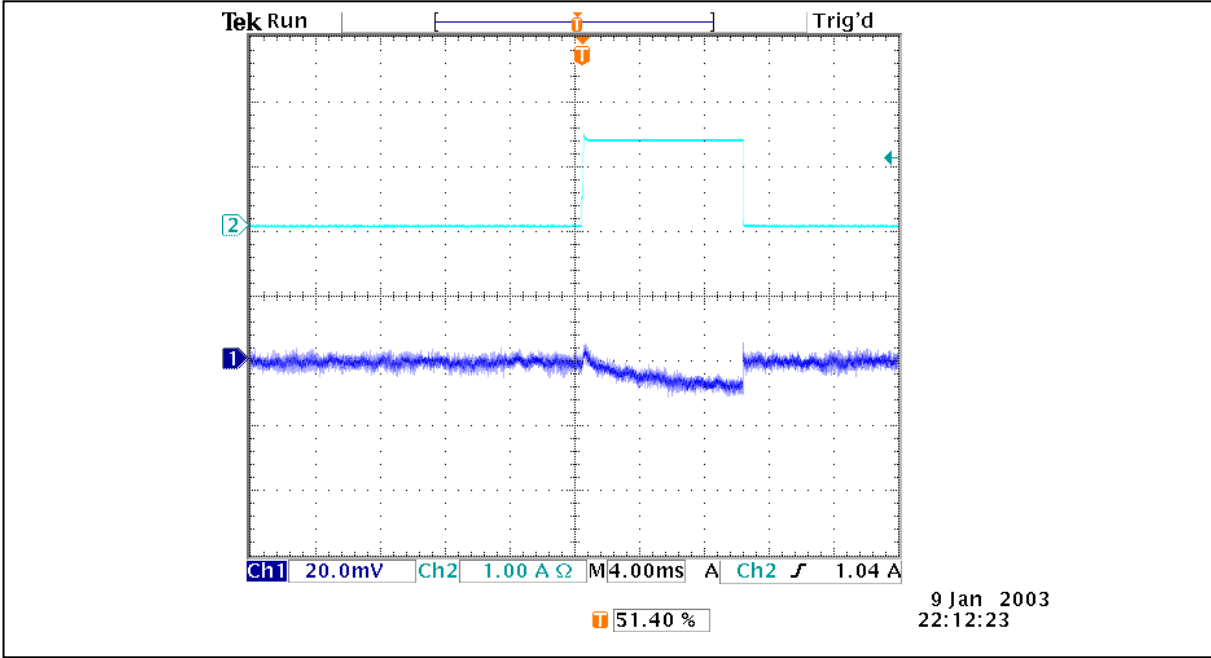
**Note:** Load regulation is tested with a 10ms pulse current and measuring  $V_{TT}$ .



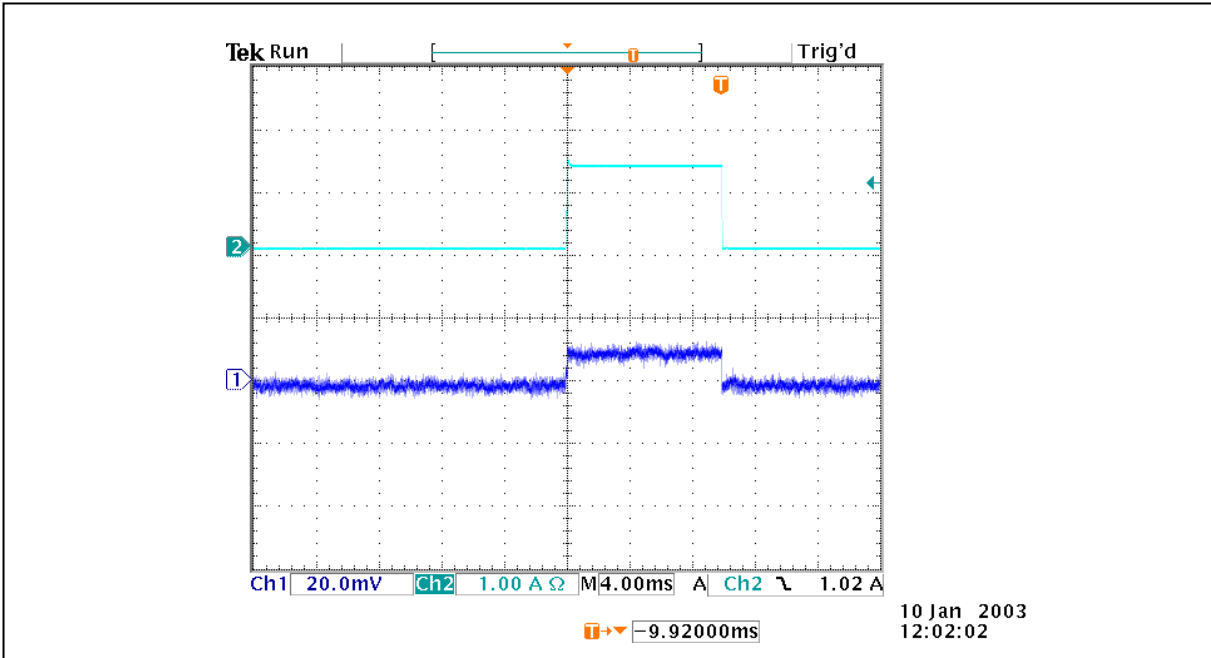


8. TYPICAL OPERATING WAVEFORM

W83310S-N  $V_{TT}$  offset with a 1.5A/10ms driving pulse current.



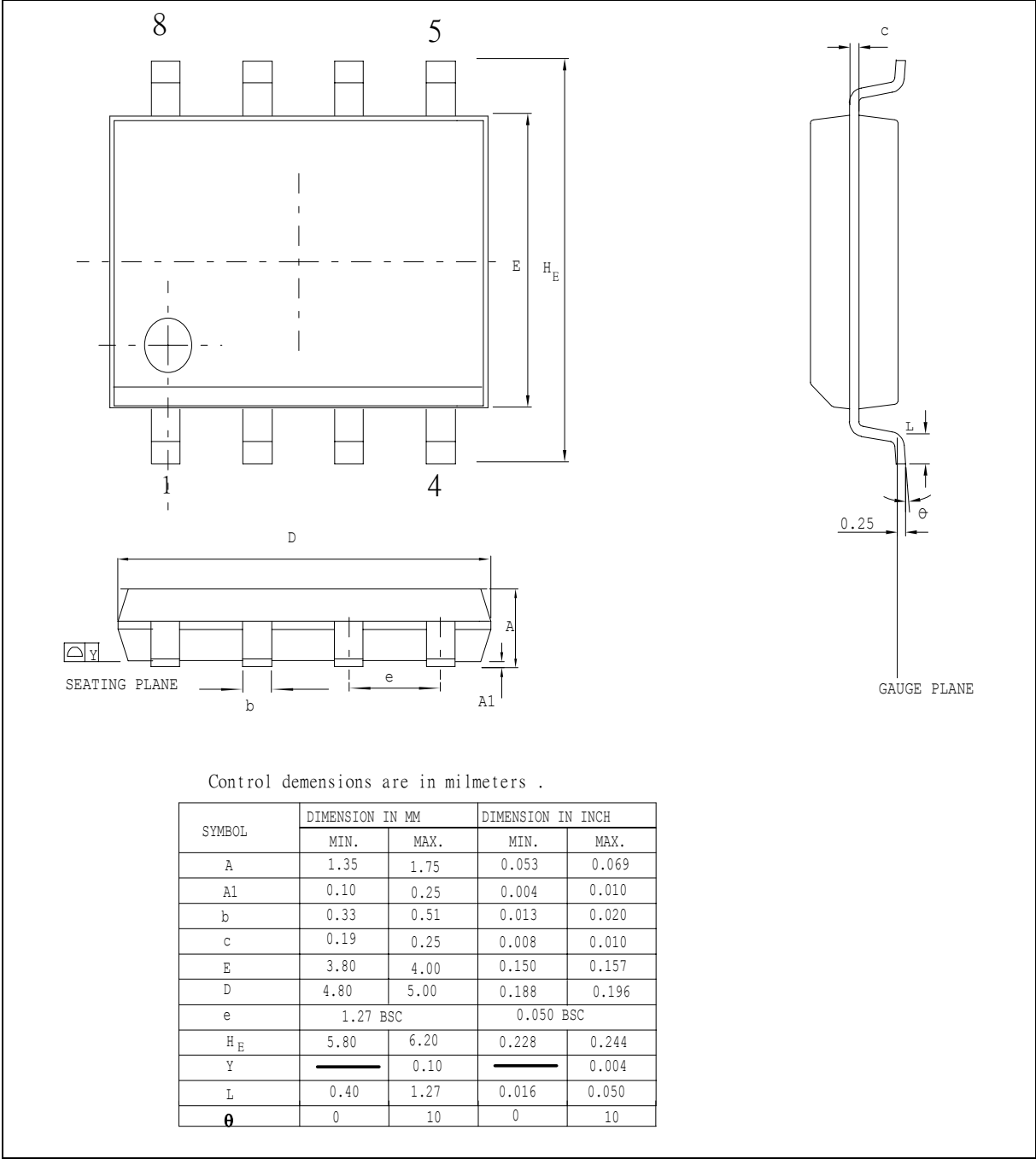
W83310S-N  $V_{TT}$  offset with a 1.5A/10ms sinking pulse current.





9. PACKAGE DIMENSION

8L SOP 150mil



# W83310S-N/W83310G-N



## 10. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83310S-N	8PIN SOP	Commercial, 0°C to +70°C
W83310G-N	8PIN SOP(Pb-free package)	Commercial, 0°C to +70°C

## 11. HOW TO READ THE TOP MARKING



Left line: Winbond logo

1<sup>st</sup> & 2<sup>nd</sup> line: W83310S-N, W83310G-N – the part number (W83310G-N is Pb-free package)

3rd line: Tracking code Tracking code 249 O A

249: packages assembled in Year 02', week 49

O: assembly house ID; O means OSE, G means GR, etc.

B: the IC version



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### Headquarters

No. 4, Creation Rd. III,  
Science-Based Industrial Park,  
Hsinchu, Taiwan  
TEL: 886-3-5770066  
FAX: 886-3-5665577  
<http://www.winbond.com.tw/>

### Taipei Office

9F, No.480, Rueiguang Rd.,  
Neihu District, Taipei, 114,  
Taiwan, R.O.C.  
TEL: 886-2-8177-7168  
FAX: 886-2-8751-3579

### Winbond Electronics Corporation America

2727 North First Street, San Jose,  
CA 95134, U.S.A.  
TEL: 1-408-9436666  
FAX: 1-408-5441798

### Winbond Electronics Corporation Japan

7F Daini-ueno BLDG, 3-7-18  
Shinyokohama Kohoku-ku,  
Yokohama, 222-0033  
TEL: 81-45-4781881  
FAX: 81-45-4781800

### Winbond Electronics (Shanghai) Ltd.

27F, 2299 Yan An W. Rd. Shanghai,  
200336 China  
TEL: 86-21-62365999  
FAX: 86-21-62365998

### Winbond Electronics (H.K.) Ltd.

Unit 9-15, 22F, Millennium City,  
No. 378 Kwun Tong Rd.,  
Kowloon, Hong Kong  
TEL: 852-27513100  
FAX: 852-27552064

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