Product Brief
December 2006
Revision 1.2

WPCD374L
Desktop SuperI/O with Glue Functions

General Description

The Winbond WPCD374L Advanced I/O product allows for a smaller system board size and saves on total system cost. It includes legacy SuperI/O functions, system glue functions, health monitoring and control, commonly used functions such as GPIO, and ACPI-compliant Power Management support.

The WPCD374L integrates miscellaneous analog and digital system glue functions to reduce the number of discrete components required. The host communicates with the functions integrated in the WPCD374L device through an LPC Bus Interface.

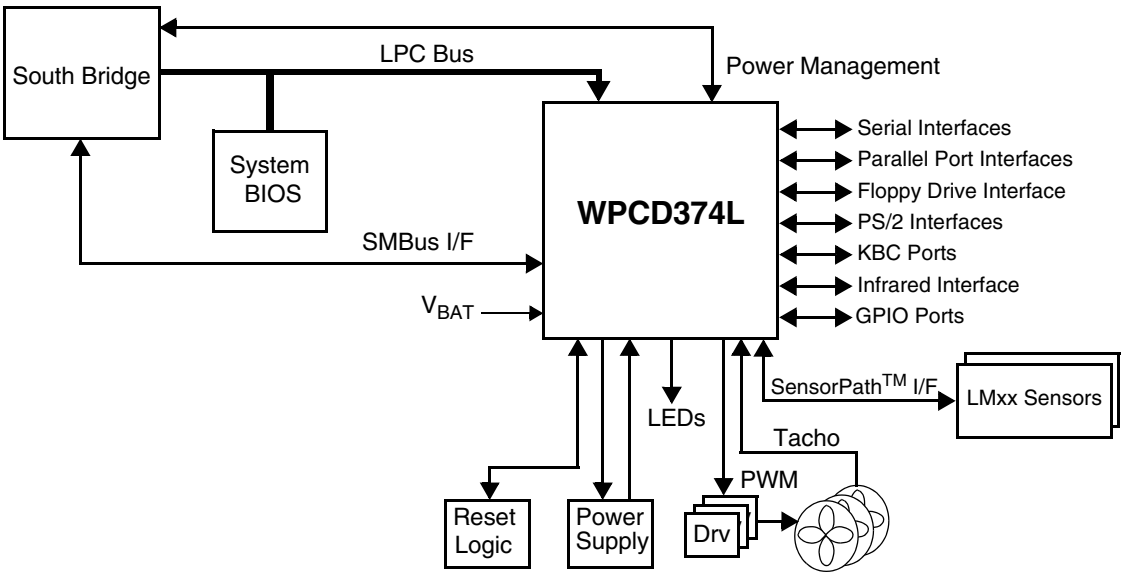
The WPCD374L extended wake-up support complements the ACPI controller in the chipset. The System Wake-Up Control (SWC) module, powered by V_{SB3}, supports a flexible wake-up mechanism.

The WPCD374L supports both I/O and memory mapping of module registers, enables building legacy-free systems, and is pin- and software-compatible with the Winbond 8374L.

Outstanding Features

- Fan monitor and control
- Heceta6-compatible register set, accessible via the LPC interface and SMBus
- Glue functions to complement the South Bridge functionality
- V_{SB3}-powered Power Management with 19 wake-up sources
- Controls three LED indicators
- 16 GPIO ports with a variety of wake-up options
- SensorPath™ interface to LMxx sensor devices for system health support
- I/O-mapped and memory-mapped registers
- Legacy modules: Parallel Port, Floppy Disk Controller (FDC), two Serial Ports, Slow InfraRed Port and a Keyboard and Mouse Controller (KBC)
- LPC interface, based on Intel's *LPC Interface Specification Revision 1.1, August 2002*
- *PC01 Revision 1.0* and *Advanced Configuration and Power Interface (ACPI) Specification Revision 2.0* compliant
- Pin- and software-compatible with the Winbond 8374L
- 128-pin PQFP package

Block Diagram



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Features

System Health Support

- SensorPath interface to sensors optimizes digital/analog partitioning
  - Simplifies board design and routing
  - Supports distributed sensors and centralized control
  - Health monitoring is self-contained and requires minimal host attention
  - Faster boot time
  - Off loads SMBus, and enables ASF compliance
- Fan Monitor and Control
  - Three PWM-based fan controls
  - Four 16-bit resolution tachometer inputs
  - Software or local temperature feedback control
- Heceta6-compatible register set accessible via the LPC interface and SMBus
  - Supports the following combinations of LMxx devices:
    - LM96011 and optional LM95010
    - LM96012
    - LM96010
  - Simultaneous read support via LPC interface and SMBus

Glue Functions

- Generates the power-related signals:
  - Main Power good
  - Power distribution control (for switching between Main and Standby regulators)
  - Resume reset (Master Reset) according to the 5V standby supply status
  - Main power supply turn on ($\overline{PS\_ON}$)
- Voltage translation between 2.5V or 3.3V levels (DDC) and 5V levels (VGA) for the SMBus serial clock and data signals
- Isolation circuitry for the SMBus serial clock and data signals
- Buffers $\overline{PCI\_RESET}$ to generate two reset output signals
- Buffers $\overline{PCI\_RESET}$ to generate IDE reset output.
- Generates "highest active supply" reference voltage
  - Based on 3.3V and 5V Main supplies
  - Based on 3.3V and 5V Standby supplies
- High-current LED driver control for Hard Disk Drive activity indication
- Software selectable alternative functionality, through pin multiplexing

General-Purpose I/O (GPIO) Ports

- All 16 GPIO ports powered by V_{SB3}
- Each pin individually configured as input or output
- Programmable features for each output pin:
  - Drive type (open-drain, push-pull or TRI-STATE®)
  - TRI-STATE on detection of falling V_{DD3} for V_{SB3}-powered pins driving V_{DD}-supplied devices
- Programmable option for internal pull-up resistor on each input pin (some with internal pull-down resistor option)
- Lock option for the configuration and data of each output pin
- 15 GPIO ports generate IRQ/$\overline{SIOPME}$ for wake-up events; each GPIO has separate:
  - Enable control of event status routing to IRQ
  - Enable control of event status routing to $\overline{SIOPME}$ (via SWC)
  - Polarity and edge/level selection
    - Programmable debouncing

Power Management

- Supports *ACPI Specification Revision 2.0b, July 27, 2000*
- System Wake-Up Control (SWC)
  - Optional routing of events to generate SCI ($\overline{SIOPME}$) on detection of:
    - Keyboard or Mouse events
    - Ring Indication $\overline{RI}$ on each of the two serial ports
    - General-Purpose Input Events from 15 GPIO pins
    - IRQs of the Keyboard and Mouse Controller
    - IRQs of the other internal modules
  - Optional routing of the SCI ($\overline{SIOPME}$) to generate IRQ (SERIRQ)
  - Implements the GPE1_BLK of the ACPI General Purpose (Generic) Register blocks with "child" events
  - V_{SB3}-powered event detection and event-logic configuration
- Enhanced Power Management (PM), including:
  - Special configuration registers for power down
  - Low-leakage pins
  - Low-power CMOS technology
  - Ability to disable all modules
  - High-current LED drivers control (two LEDs) for power status indication with:
    - Standard blinking, controlled by software
    - Advanced blinking, controlled by power supply status, sleep state or software
    - Special blinking, controlled by power supply status, sleep state and software bit
  - V_{BAT}-powered indication of the Main power supply state before an AC power failure
- Keyboard Events
  - Wake-up on any key
  - Supports programmable 8-byte sequence "Password" or "Special Keys" for Power Management
  - Simultaneous recognition of three programmable keys (sequences): "Power", "Sleep" and "Resume"
  - Wake-up on mouse movement and/or button click

Bus Interface

- LPC Bus Interface
  - Based on Intel's *LPC Interface Specification Revision 1.1, August 2002*
  - I/O, Memory and 8-bit Firmware Memory read and write cycles
  - Up to four 8-bit DMA channels
  - Serial IRQ (SERIRQ)
  - Supports registers memory and I/O mapping

Features (Continued)

- Configuration Control
  - PnP Configuration Register structure
  - *PC01 Specification Revision 1.0, 1999-2000* compliant
  - Base Address strap ($\overline{\text{BADDR}}$) to setup the address of the Index-Data register pair (defaults to 2Eh/2Fh)
  - Flexible resource allocation for all logical devices:
    - Relocatable base address
    - 15 IRQ routing options to serial IRQ
    - Up to four optional 8-bit DMA channels
  - Configurable feature sets:
    - Software selectable
    - V_{SB3}-powered pin multiplexing

Legacy Modules

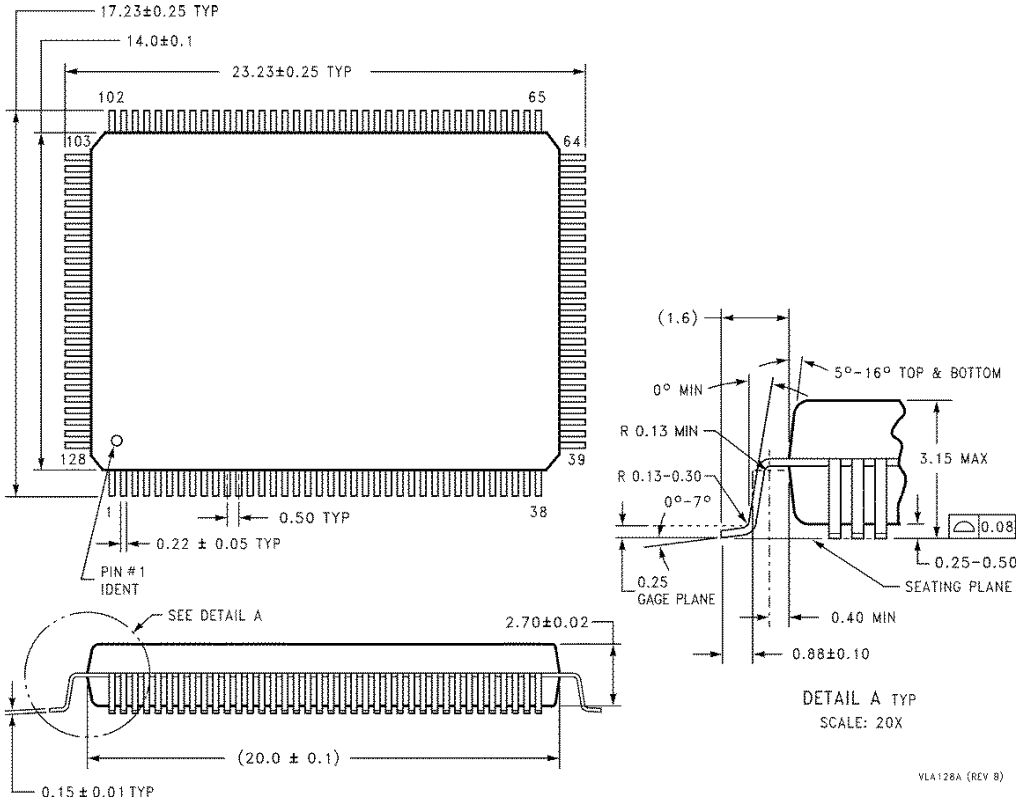
- Serial Ports 1 and 2
  - Software-compatible with the NS16550A and NS16450
  - Support shadow register for write-only bit monitoring
  - Data rates up to 1.5 Mbaud
- Serial Infrared Port (SIR)
  - Software compatible with the 16550A and the 16450
  - Shadow register support for write-only bit monitoring
  - HP-SIR
  - ASK-IR option of SHARP-IR
  - DASK-IR option of SHARP-IR
  - Consumer Remote Control supports RC-5, RC-6, NEC, RCA and RECS 80
- IEEE 1284-compliant Parallel Port
  - ECP, with Level 2 (14 mA sink and source output buffers)
  - Software or hardware control
  - Enhanced Parallel Port (EPP) compatible with EPP 1.7 and EPP 1.9
  - Supports EPP as mode 4 of the Extended Control Register (ECR)
  - Selection of internal pull-up or pull-down resistor for Paper End (PE) pin
  - Supports a demand DMA mode mechanism and a DMA fairness mechanism for improved bus utilization
  - Protection circuit that prevents damage to the parallel port when a printer connected to it is powered up or is operated at high voltages (in both cases, even if the WPCD374L is in power-down state)
- Floppy Disk Controller (FDC)
  - Software compatible with the PC8477 (the PC8477 contains a superset of the FDC functions in the μDP8473, NEC μPD765A/B and N82077 devices)
  - Error-free handling of data overrun and underrun
  - Programmable write protect
  - Supports FM and MFM modes
  - Supports Enhanced mode command for three-mode Floppy Disk Drive (FDD)
  - Perpendicular recording drive support for 2.88 MBytes
  - Burst (16-byte FIFO) and Non-Burst modes
  - Full support for IBM Tape Drive Register (TDR) implementation of AT and PS/2 drive types
  - High-performance digital data separator
  - Supports standard tape drives (1 Mbps, 500 Kbps and 250 Kbps)
- Keyboard and Mouse Controller (KBC)
  - 8-bit microcontroller, software compatible with 8042AH and PC87911
  - Standard interface (60h, 64h, IRQ1 and IRQ12)
  - Supports two external swapable PS/2 interfaces for keyboard and mouse
  - Programmable, dedicated quasi-bidirectional I/O lines (GA20/P21, $\overline{\text{KBRST}}$/P20)

Clocking, Supply, and Package Information

- Clocks
  - LPC (PCI) clock input (up to 33 MHz)
  - On-chip Clock Generator:
    - Generates 48 MHz clock
    - Generates 32.768 KHz internal clock
    - V_{SB3} powered
    - Based on the 14.31818 MHz clock input
- Protection
  - All pins are 5V tolerant and back-drive protected (except LPC bus pins)
  - High ESD protection of all the pins
  - Pin multiplexing selection lock
  - Configuration register lock
- Testability
  - XOR tree structure
    - Includes all the pins (except supply, analog and not connected pins)
    - Selected at power-up by strap input ($\overline{\text{TEST}}$)
  - TRI-STATE pins, selected at power-up by strap input ($\overline{\text{TRIS}}$)
- Power Supply
  - 3.3V supply operation
  - Separate pin pairs for main (V_{DD3}) and standby (V_{SB3}) power supplies
  - Backup battery input (V_{BAT}) for SWC indications
  - Low standby power consumption
  - Very low power consumption from backup battery (less than 0.5 μA)
- Package
  - 128-pin PQFP

Physical Dimensions

All dimensions are in millimeters



Plastic Quad Flatpack (PQFP), JEDEC

Order Number: WPCD374L_xFG ("_" = chip revision A, B, C, etc.; "x" is the ROM code: U = IBU, W = IBW)

(Refer to your local Winbond representative for further details.)

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