XC95216 In-System Programmable CPLD

April, 1997 (Version 1.0)

Product Specification

Features

- 10 ns pin-to-pin logic delays on all pins
- f_{CNT} to 111 MHz
- 216 macrocells with 4800 usable gates
- Up to 166 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full commercial voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs
- 3.3 V or 5 V I/O capability
- PCI compliant (-10 speed grade)
- Advanced CMOS 5V FastFLASH technology
- Supports parallel programming of more than one XC9500 concurrently
- Available in 160-pin PQFP, 352-pin BGA, and 208-pin HQFP packages

Description

The XC95216 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of twelve 36V18 Function Blocks, providing 4,800 usable gates with propagation delays of 10 ns. See Figure 2 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC95216 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) =

MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

Figure 1 shows a typical calculation for the XC95216 device.

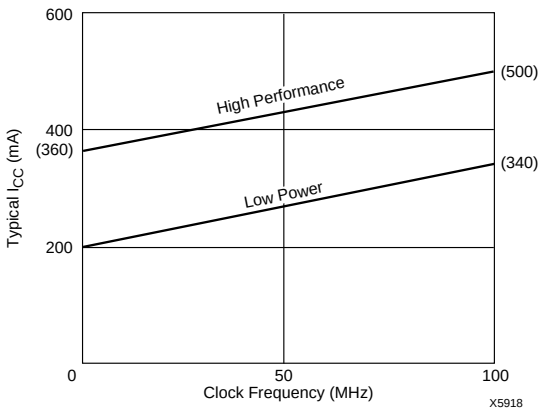


Figure 1: Typical I_{CC} vs. Frequency For XC95216

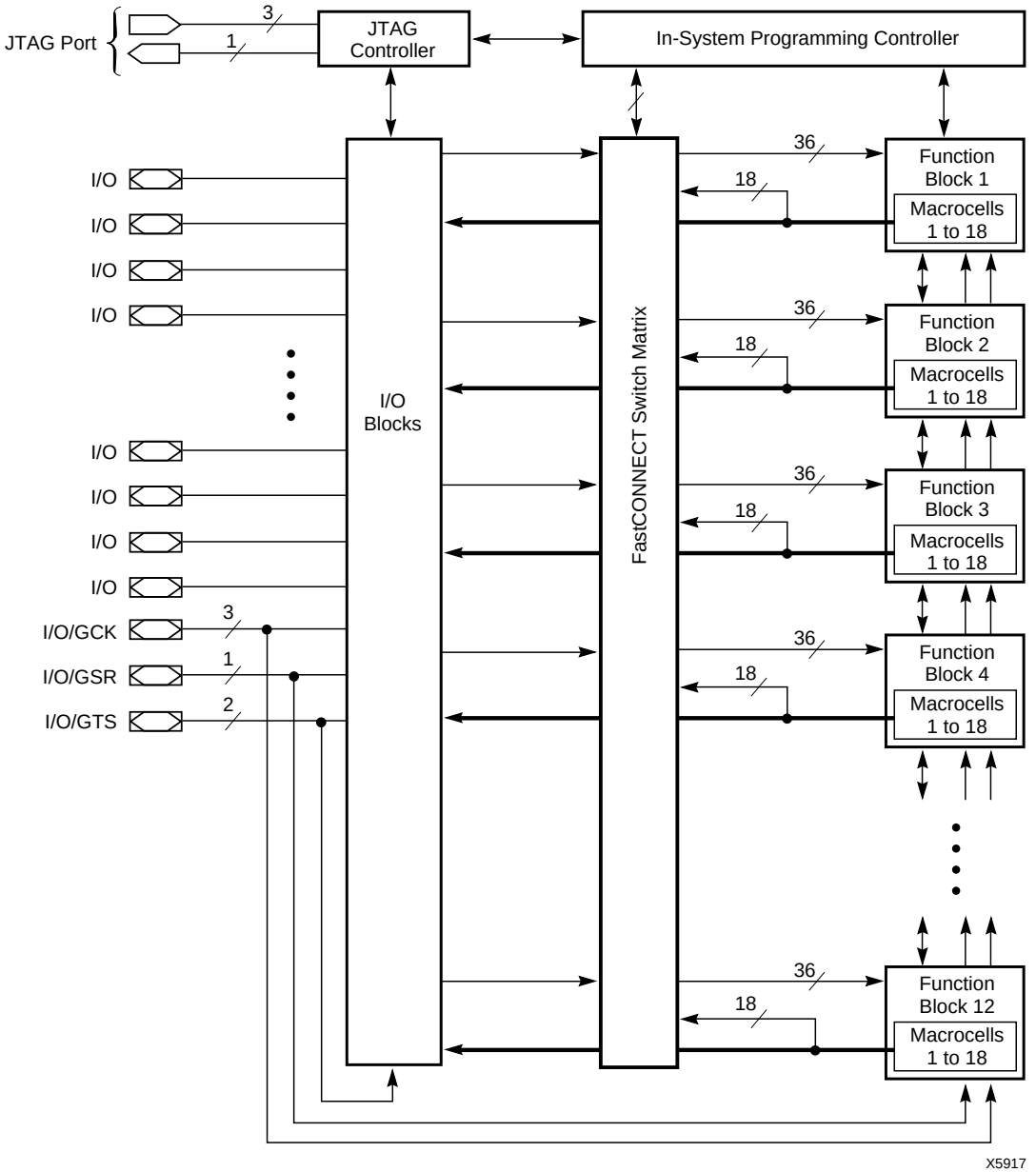


Figure 2: XC95216 Architecture

Function Block outputs (indicated by the bold line) drive the I/O Blocks directly

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage relative to GND	-0.5 to 7.0	V
V_{IN}	DC input voltage relative to GND	-0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} + 0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Max soldering temperature (10 s @ 1/16 in = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions[1]

Symbol	Parameter	Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffer	4.75 (4.5)	5.25 (5.5)	V
V_{CCIO}	Supply voltage for output drivers for 5 V operation	4.75 (4.5)	5.25 (5.5)	V
	Supply voltage for output drivers for 3.3 V operation	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.80	V
V_{IH}	High-level input voltage	2.0	V_{CCINT} +0.5	V
V_O	Output voltage	0	V_{CCIO}	V

Note: 1. Numbers in parenthesis are for industrial-temperature range versions.

Endurance Characteristics

Symbol	Parameter	Min	Max	Units
t_{DR}	Data Retention	20	-	Years
N_{PE}	Program/Erase Cycles	10,000	-	Cycles

DC Characteristics Over Recommended Operating Conditions

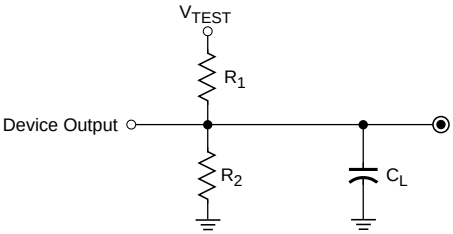
Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 5 V operation	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	Output high voltage for 3.3 V operation	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	Output low voltage for 5 V operation	I_{OL} = 24 mA V_{CC} = Min		0.5	V
	Output low voltage for 3.3 V operation	I_{OL} = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		±10.0	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		±10.0	µA
C_{IN}	I/O capacitance	V_{IN} = GND f = 1.0 MHz		10.0	pF
I_{CC}	Operating Supply Current (low power mode, active)	V_I = GND, No load f = 1.0 MHz	200 (typ)		ma

AC Characteristics

Symbol	Parameter	XC95216-10		XC95216-15		XC95216-20		Units
		Min	Max	Min	Max	Min	Max	
t_{PD}	I/O to output valid		10.0		15.0		20.0	ns
t_{SU}	I/O setup time before GCK	6.5		8.0		10.0		ns
t_{H}	I/O hold time after GCK	0.0		0.0		0.0		ns
t_{CO}	GCK to output valid		6.5		8.0		10.0	ns
f_{CNT}[1]	16-bit counter frequency	111		95		83		MHz
f_{SYSTEM}[2]	Multiple FB internal operating frequency	67		56		50		MHz
t_{PSU}	I/O setup time before p-term clock input	2.5		4.0		4.0		ns
t_{PH}	I/O hold time after p-term clock input	4.0		4.0		6.0		ns
t_{PCO}	P-term clock to output valid		10.5		12.0		16.0	ns
t_{OE}	GTS to output valid		10.0		15.0		20.0	ns
t_{OD}	GTS to output disable		10.0		15.0		20.0	ns
t_{POE}	Product term OE to output enabled		15.5		18.0		22.0	ns
t_{POD}	Product term OE to output disabled		15.5		18.0		22.0	ns
t_{WLH}	GCK pulse width (High or Low)		4.5		5.5		5.5	ns

Preliminary

Note: 1. f_{CNT} is the fastest 16-bit counter frequency available, using the local feedback when applicable. f_{CNT} is also the Export Control Maximum flip-flop toggle rate, f_{TOG}.
2. f_{SYSTEM} is the internal operating frequency for general purpose system designs spanning multiple FBs.



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X5906

Figure 3: AC Load Circuit

Internal Timing Parameters

Symbol	Parameter	XC95216-10		XC95216-15		XC95216-20		Units
		Min	Max	Min	Max	Min	Max	
Buffer Delays								
t_{IN}	Input buffer delay		3.5		4.5		6.5	ns
t_{GCK}	GCK buffer delay		3.0		3.0		3.0	ns
t_{GSR}	GSR buffer delay		6.0		7.5		9.5	ns
t_{GTS}	GTS buffer delay		10.0		15.0		20.0	ns
t_{OUT}	Output buffer delay		3.0		4.5		6.5	ns
t_{EN}	Output buffer enable/disable delay		0.0		0.0		0.0	ns
Product Term Control Delays								
t_{PTCK}	Product term clock delay		3.5		2.5		2.5	ns
t_{PTSR}	Product term set/reset delay		2.5		3.0		3.0	ns
t_{PTTS}	Product term 3-state delay		12.0		13.5		15.5	ns
Internal Register and Combinatorial delays								
t_{PDI}	Combinatorial logic propagation delay		1.0		3.0		4.0	ns
t_{SUI}	Register setup time	3.5		3.5		3.5		ns
t_{HI}	Register hold time	3.0		4.5		6.5		ns
t_{COI}	Register clock to output valid time		0.5		0.5		0.5	ns
t_{AOI}	Register async. S/R to output delay		7.0		8.0		9.0	ns
t_{RAI}	Register async. S/R recovery before clock	10.0		15.0		20.0		ns
t_{LOGI}	Internal logic delay		2.5		3.0		3.0	ns
t_{LOGILP}	Internal low power logic delay		11.0		11.5		11.5	ns
Feedback Delays								
t_F	FastCONNECT matrix feedback delay		8.5		11.0		13.0	ns
t_{LF}	Function Block local feeback delay		2.5		3.5		5.0	ns
Time Adders								
t_{PTA}[3]	Incremental Product Term Allocator delay		1.0		1.5		1.5	ns
t_{SLEW}	Slew-rate limited delay		4.5		5.0		5.5	ns

Preliminary

Note: 3. t_{PTA} is multiplied by the span of the function as defined in the family data sheet.

XC95216 I/O Pins

Function Block	Macrocell	PQ160	HQ208	BG352	BScan Order	Notes
1	1	–	–	–	645	
1	2	18	22	M25	642	
1	3	19	23	M26	639	
1	4	–	28	N26	636	
1	5	21	25	N25	633	
1	6	22	30	P23	630	
1	7	–	–	–	627	
1	8	23	31	P24	624	
1	9	24	32	R26	621	
1	10	–	12	G26	618	
1	11	25	33	R24	615	
1	12	26	34	T26	612	
1	13	–	–	–	609	
1	14	27	35	T25	606	
1	15	28	36	T23	603	
1	16	29	37	V26	600	
1	17	30	38	U24	597	
1	18	–	–	–	594	
2	1	–	–	–	591	
2	2	6	7	E25	588	[1]
2	3	7	8	G24	585	
2	4	–	29	P25	582	
2	5	8	9	F26	579	[1]
2	6	9	10	H23	576	
2	7	–	–	–	573	
2	8	11	15	K23	570	
2	9	12	16	K24	567	
2	10	–	-	–	564	
2	11	13	17	J25	561	
2	12	14	18	L24	558	
2	13	–	–	–	555	
2	14	15	19	K25	552	
2	15	16	20	L26	549	
2	16	–	14	H25	546	
2	17	17	21	M24	543	
2	18	–	–	–	540	

Function Block	Macrocell	PQ160	HQ208	BG352	BScan Order	Notes
3	1	–	–	–	537	
3	2	32	43	AA26	534	
3	3	33	44	Y24	531	[1]
3	4	–	39	U23	528	
3	5	34	45	AB25	525	
3	6	35	46	AA24	522	[1]
3	7	–	–	–	519	
3	8	36	47	Y23	516	
3	9	37	49	AA23	513	
3	10	–	67	AD18	510	
3	11	38	50	AB24	507	
3	12	39	51	AD25	504	
3	13	–	–	–	501	
3	14	42	55	AD23	498	[1]
3	15	43	56	AF24	495	
3	16	–	80	AE12	492	
3	17	44	57	AE23	489	
3	18	–	–	–	486	
4	1	–	–	–	483	
4	2	152	198	D18	480	
4	3	153	199	A21	477	
4	4	–	196	B19	474	
4	5	154	200	B20	471	
4	6	155	201	C20	468	
4	7	–	–	–	465	
4	8	156	202	B22	462	
4	9	158	205	B24	459	
4	10	–	-	–	456	
4	11	159	206	C23	453	[1]
4	12	2	3	E23	450	[1]
4	13	–	–	–	447	
4	14	3	4	C26	444	
4	15	4	5	E24	441	[1]
4	16	–	203	D20	438	
4	17	5	6	F24	435	
4	18	–	–	–	432	

XC95216 I/O Pins (continued)

Function Block	Macrocell	PQ160	HQ208	BG352	BScan Order	Notes
5	1	–	–	–	429	
5	2	45	58	AE22	426	
5	3	47	60	AE21	423	
5	4	–	41	W25	420	
5	5	48	61	AF21	417	
5	6	49	63	AD19	414	
5	7	–	–	–	411	
5	8	50	64	AE20	408	
5	9	52	70	AF18	405	
5	10	–	109	AD1	402	
5	11	53	71	AE17	399	
5	12	54	72	AE16	396	
5	13	–	–	–	393	
5	14	55	73	AF16	390	
5	15	56	74	AE14	387	
5	16	–	40	Y26	384	
5	17	57	75	AF14	381	
5	18	–	–	–	378	
6	1	–	–	–	375	
6	2	140	180	A12	372	
6	3	142	182	A13	369	
6	4	–	208	D22	366	
6	5	143	185	C14	363	
6	6	144	186	A15	360	
6	7	–	–	–	357	
6	8	145	187	B15	354	
6	9	146	188	C15	351	
6	10	–	183	B14	348	
6	11	147	191	A16	345	
6	12	148	192	C16	342	
6	13	–	–	–	339	
6	14	149	193	C17	336	
6	15	150	194	B18	333	
6	16	–	169	D9	330	
6	17	151	197	C19	327	
6	18	–	–	–	324	

Function Block	Macrocell	PQ160	HQ208	BG352	BScan Order	Notes
7	1	–	–	–	321	
7	2	58	76	AE13	318	
7	3	59	77	AC13	315	
7	4	–	54	AE24	312	
7	5	60	78	AD13	309	
7	6	62	82	AD12	306	
7	7	–	–	–	303	
7	8	63	83	AC12	300	
7	9	64	84	AF11	297	
7	10	–	91	AD8	294	
7	11	65	85	AE11	291	
7	12	66	86	AE9	288	
7	13	–	–	–	285	
7	14	67	87	AD9	282	
7	15	68	88	AC10	279	
7	16	–	48	AC26	276	
7	17	69	89	AF7	273	
7	18	–	–	–	270	
8	1	–	–	–	267	
8	2	126	162	B5	264	
8	3	128	164	B6	261	
8	4	–	143	J1	258	
8	5	129	166	D8	255	
8	6	130	167	B7	252	
8	7	–	–	–	249	
8	8	131	170	C10	246	
8	9	132	171	B9	243	
8	10	–	195	A20	240	
8	11	133	173	A9	237	
8	12	134	174	D11	234	
8	13	–	–	–	231	
8	14	135	175	B11	228	
8	15	138	178	C12	225	
8	16	–	189	D15	222	
8	17	139	179	B12	219	
8	18	–	–	–	216	

XC95216 I/O Pins (continued)

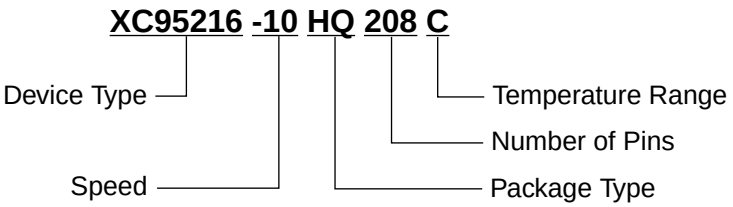
Function Block	Macrocell	PQ160	HQ208	BG352	BScan Order	Notes
9	1	–	–	–	213	
9	2	72	95	AD7	210	
9	3	74	97	AE5	207	
9	4	–	101	AD4	204	
9	5	76	99	AC7	201	
9	6	77	100	AE3	198	
9	7	–	–	–	195	
9	8	78	102	AC5	192	
9	9	79	103	AD3	189	
9	10	–	90	AE8	186	
9	11	82	110	AA4	183	
9	12	83	111	AB2	180	
9	13	–	–	–	177	
9	14	84	112	AC1	174	
9	15	85	113	AA2	171	
9	16	–	62	AC19	168	
9	17	86	114	AA1	165	
9	18	–	–	–	162	
10	1	–	–	–	159	
10	2	113	147	H3	156	
10	3	114	148	J4	153	
10	4	–	144	K3	150	
10	5	115	149	G2	147	
10	6	116	150	G3	144	
10	7	–	–	–	141	
10	8	117	152	E2	138	
10	9	118	154	D2	135	
10	10	–	168	A7	132	
10	11	119	155	F4	129	
10	12	122	158	B3	126	
10	13	–	–	–	123	
10	14	123	159	A3	120	
10	15	124	160	D6	117	
10	16	–	165	A6	114	
10	17	125	161	C6	111	
10	18	–	–	–	108	

Function Block	Macrocell	PQ160	HQ208	BG352	BScan Order	Notes
11	1	–	–	–	105	
11	2	87	115	Y1	102	
11	3	88	116	V4	99	
11	4	–	119	U4	96	
11	5	89	117	V3	93	
11	6	90	118	W2	90	
11	7	–	–	–	87	
11	8	91	121	V2	84	
11	9	92	122	U2	81	
11	10	–	107	AC3	78	
11	11	93	123	T2	75	
11	12	95	125	R4	72	
11	13	–	–	–	69	
11	14	96	126	R3	66	
11	15	97	127	R2	63	
11	16	–	120	U3	60	
11	17	98	128	R1	57	
11	18	–	–	–	54	
12	1	–	–	–	51	
12	2	101	131	P1	48	
12	3	102	133	N2	45	
12	4	–	106	AD2	42	
12	5	103	134	N4	39	
12	6	104	135	N3	36	
12	7	–	–	–	33	
12	8	105	136	M1	30	
12	9	106	137	M3	27	
12	10	–	151	F2	24	
12	11	107	138	M4	21	
12	12	108	139	L1	18	
12	13	–	–	–	15	
12	14	109	140	L2	12	
12	15	111	145	G1	9	
12	16	–	142	L3	6	
12	17	112	146	H2	3	
12	18	–	–	–	0	

XC95216 Global, JTAG and Power Pins

Pin Type	PQ160	HQ208	BG352
I/O/GCK1	33	44	Y24
I/O/GCK2	35	46	AA24
I/O/GCK3	42	55	AD23
I/O/GTS1	6	7	E25
I/O/GTS2	8	9	F26
I/O/GTS3	2	3	E23
I/O/GTS4	4	5	E24
I/O/GSR	159	206	C23
TCK	75	98	AD6
TDI	71	94	AF6
TDO	136	176	D12
TMS	73	96	AE6
V_{CCINT} 5 V	10,46,94,157	11, 59, 124, 153, 204	H24, AF23, T1, G4, C22
V_{CCIO} 3.3 V/5 V	1,41,61,81,121,141	1, 26, 53, 65, 79, 92, 105, 132, 157, 172, 181, 184	A10, A17, B2, B25, D7, D13, D19, G23, H4, K1, K26, N23, P4, U1, U26, W23, Y4, AC8, AC14, AC20, AE25, AF10, AF17
GND	20, 31, 40, 51, 70, 80, 99, 100, 110, 120, 127, 137, 160	2, 13, 24, 27, 42, 52, 66, 68, 69, 81, 93, 104, 108, 129, 130, 141, 156, 163, 177, 190, 207	A1, A2, A5, A8, A14, A19, A22, A25, A26, B1, B26, E1, E26, H1, H26, N1, P26, W1, W26, AB1, AB26, AE1, AE26, AF1, AF2, AF5, AF8, AF13, AF19, AF22, AF25, AF26
No Connects	–	–	

Ordering Information



Speed Options

- 20 20 ns pin-to-pin delay
-15 15 ns pin-to-pin delay
-10 10 ns pin-to-pin delay

Packaging Options

PQ160 160-Pin Plastic Quad Flat Pack (PQFP)
HQ208 208-Pin Heat Sink Quad Flat Pack (HQFP)
BG352 352-Pin Ball Grid Array (BGA)

Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	–40°C to 85°C

Component Availability

Pins		**160**	**160**	**352**
Type		**Plastic PQFP**	**Power QFP**	**Plastic BGA**
Code		**PQ160**	**HQ208**	**BG352**
XC95216	–20	C(I)	C(I)	C(I)
	–15	C	C	C(I)
	–10	C	C	C

C = Commercial = 0° to +70°C I = Industrial = –40° to 85°C