XCELL

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XILINX®

The Programmable Logic Company℠

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Meet Mr. Logic

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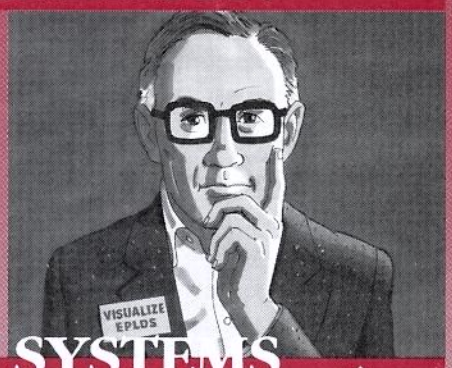
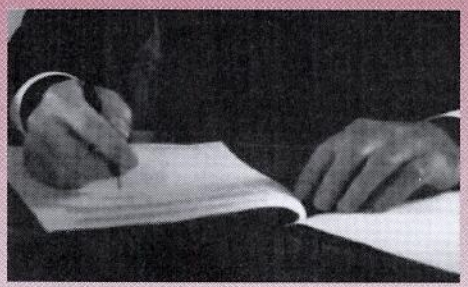


DEVELOPMENT SYSTEMS



Xilinx-Synopsys

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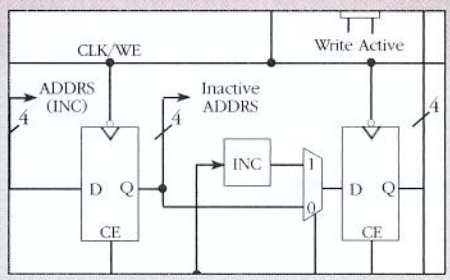

Looking Forward to the Next Ten Years

By BRADLY FAWCETT ◆ Editor

February 1994 marks the 10th anniversary of the founding of Xilinx Inc. and the invention of field programmable gate arrays. Like most successful inventions, the FPGA combined an inspirational idea with leading-edge technology to meet a market need. The market needed higher levels of logic integration combined with low risk and short time-to-market; the inspirational idea was high-density programmable logic based on SRAM programming and a gate-array-like logic cell array architecture with programmable routing; the leading-edge technology was fine-geometry CMOS fabrication processes. FPGAs fulfill designers' needs by combining the speed and density of a custom gate array with the design flexibility of a programmable logic device.

The First 10 Years

FPGA technology has advanced dramatically in its first 10 years. The first FPGA, the XC2064, boasted a maximum of 1,200 gates (about 800 usable gates), 58 user I/Os, and a 20 MHz flip-flop toggle rate. Designs were implemented on PC/XT systems using a graphical, interactive design editor in which the user defined the logic functions that went into each logic block.

Xilinx devices now reach 13,000 usable gates and 192 I/Os; even larger parts are on the immediate horizon. The fastest devices have toggle rates exceeding 250 MHz.

The third-generation FPGAs, the XC4000 family, includes dedicated system-integration features such as on-chip RAM, wide decoders, carry logic and built-in boundary scan test support. Designs are implemented on PCs or workstations, entered using schematics or HDLs, automatically mapped into the FPGA's logic resources and automatically placed and routed.

In the meantime, component prices have decreased dramatically, falling 25 to 30 percent each year. FPGAs are a cost-effective logic solution for thousands of applications, ranging from supercomputers to hand-held instruments, from central office switches to centrifuges, and from missile guidance systems to guitar synthesizers. (And, by the way, the venerable XC2064 is still a popular device, available now with toggle rates up to 130 MHz, and at a cost of less than $5 when purchased in large quantities and plastic packages.)

The Next 10 Years

The FPGA market continues to grow by more than 30 percent annually, primarily as a result of continuing technology improvements. Continued innovation in FPGA architectures, VLSI circuit design, process technologies, and 'place and route' algorithms will lead to faster, denser, and more cost-effective devices. FPGA technology is readily adaptable to the 3V, sub-half-micron, multi-metal-layer IC technologies of the near future. Gate densities in the 50,000 to 100,000 gate range and system clock rates of 200 MHz should be achievable by the turn of the century.

XILINX TENTH ANNIVERSARY

On the software side, FPGA-specific synthesis technology will continue its rapid evolution, driven by the demand of a community of FPGA designers that has

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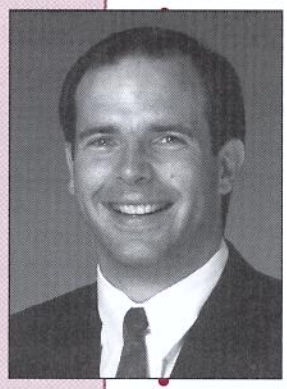
XILINX®

Who Should Supply FPGA Implementation Tools?

by HANS SCHWARZ ◆ Director, Development System Marketing

The three main steps of the FPGA development cycle are design entry, implementation, and verification. Xilinx was the first PLD vendor to offer an open system, in that the user can choose from a wide variety of design entry and verification tools from any of a number of third-party EDA vendors. However, Xilinx has been and remains the primary supplier of the design implementation software, often referred to as the 'place and route' or 'backend' tools, that support our FPGA families.



Some EDA vendors have recently entered the market with their own FPGA implementation tools, and a few new FPGA vendors are relying exclusively on third-party EDA vendors for their 'place and route' tools. These EDA suppliers suggest that they will eventually take over the market for FPGA implementation software.

While we appreciate the attractiveness of the FPGA tool market to the EDA suppliers, Xilinx must continue to develop and market the implementation tools that support our EPLD and FPGA products. The rationale behind this decision relates directly to the differing motivations of silicon vendors and EDA vendors for offering these products.

Our primary motivation is to sell programmable logic ICs. We develop implementation software because our users need a timely and economical solution — a solution that includes both IC devices and software. We want to expand the programmable logic market by lowering the cost of the technology and making it easy to use. Thus, our software is priced as low as feasible to encourage the use of the technology. Furthermore, the software must take advantage of the special features of our architectures to provide all the performance and capacity that the ICs are designed to deliver.

> *"Xilinx must continue to develop and market the implementation tools that support our EPLD and FPGA products"*

The EDA vendors are motivated to sell only software, and must sell a common solution to address many needs. EDA vendors are more likely to develop 'general-purpose' software to address a broad market than to develop customized tools for a particular architecture. While this 'universality' is attractive to a customer interested in exploring solutions from multiple IC vendors, it may also inadequately address the unique features of a specific architecture and negate a silicon vendor's competitive advantages. So, while the EDA vendor tries to satisfy the desire for a universal environment ("learn on one system and it will work with every vendor "), the user needs to ask if this concept benefits the user, or if it's even true.

Similarly, Xilinx is highly motivated to improve the silicon efficiency and performance of the ICs. Therefore, after the initial software release, we have a

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The 1994 Data Book is Here

The new 1994 Xilinx Data Book is now available. It is a revision of the 1993 Data Book, with many improvements and 72 new pages.

New information in the 1994 Data Book includes AC timing parameters for the XC4000-4, XC3000A, XC3000L, and XC2000L FPGA families. Product specifications were added for the new XC3100A family, the XC7336 EPLD, and the XC7354 EPLD, as well as advance product information for the XC73144. Other additions include new package drawings, updated development system descriptions, updated quality and reliability information, and several new application notes.

If you have not yet received a copy of the 1994 Xilinx Data Book, please contact your local Xilinx sales representative or distributor. ◆

GUEST EDITORIAL

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strong motivation to improve the software and deliver updates to our users, thereby enhancing the capabilities of the ICs. Such motivation does not exist for the EDA vendor.

Xilinx believes that the following strategy can provide the tools needed to achieve the designer's goals:

- Provide for the use of popular, general-purpose tools for the 'generic' portions of the design cycle: design entry and design verification.
- Provide low-cost, architecturally-specific implementation tools within the EDA vendor's framework.
- Provide a tight coupling between the two environments.
- Provide timely support for all new architectures.
- Continue to improve the speed and density of the ICs through software improvements and enhancements.

"We welcome the opportunity to benchmark ourselves against the best that others can offer.."

This solution offers universal capabilities at the front-end where design decisions are made. Tight coupling allows for excellent design analysis and feedback. The designer has access to the software when the silicon is ready and accessibility to the features of each architecture.

To support these objectives, we established our Alliance Program in 1990 to work with key EDA vendors to provide a tight interface to popular entry and simulation tools. The more-recently formulated Syndicate Program focuses on FPGA interfaces and compilers for synthesis tools.

Through internal development of EPLD and FPGA implementation tools, Xilinx retains control over product introduction schedules, ensuring the timely availability of tools to support new leading-edge architectures. Furthermore, by developing our own implementation tools, we retain valuable in-house expertise and benefit from the synergy that results when both the designers of the IC architectures and the designers of the development tools work closely together on a continuing basis.

High-density programmable logic devices are becoming sufficiently pervasive that both silicon and EDA vendors will have opportunities to market implementation tools. We welcome the opportunity to benchmark ourselves against the best that others can offer. The resulting competition can only result in all suppliers being pushed harder to provide the best solutions, to the ultimate benefit of all users of PLD software development tools. ◆

Fast-Rising Cabletron Chooses Xilinx For Time-to-Market, Synthesis Support

Cabletron Systems, reputedly a lean and mean operation, has never been content to rest on its laurels. Since 1983, the Rochester, NH, maker of wiring hubs, the "central nervous system" of local area networks, has seen annual revenues grow at a meteoric rate of 95 percent per year.

By creating "materials acquisition teams," purchasing teams comprised of finance, inventory planning and manufacturing personnel, Cabletron has been successful at shortening product delivery schedules from 50 to 35 days.

Shared Philosophies

When Cabletron considered designing Xilinx XC4010 FPGAs into a new universal hub called the MMAC-Plus, it found that Xilinx uses similar team approaches when the company combined sales representatives, field applications engineers and factory service personnel into its "Cabletron support team."

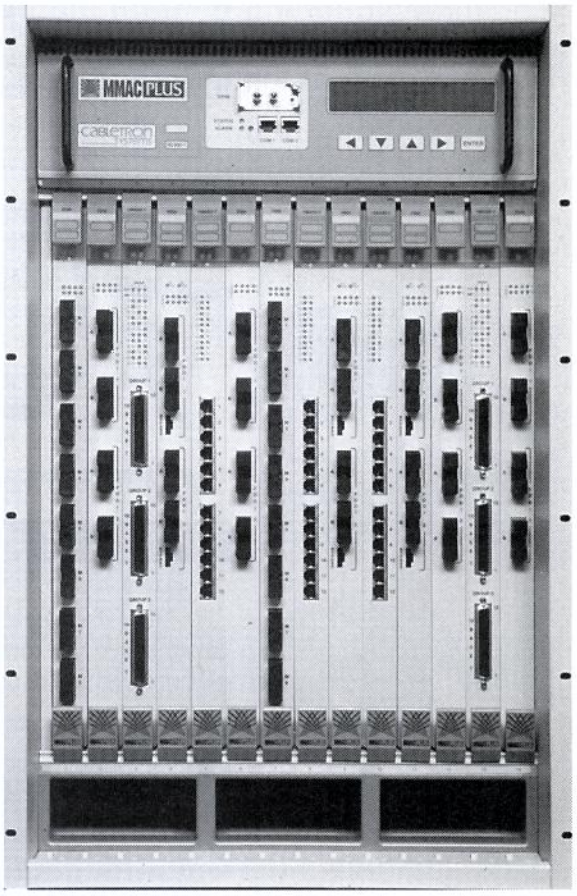
According to Julius Baskys of sales representative firm Genesis Associates, "Xilinx was put through rigorous evaluations along with a number of other programmable logic suppliers. Xilinx won the account based largely on three factors: a corporate commitment to surround Cabletron with the highest level of support for their project, a broad base of silicon products and our support of VHDL and synthesis through our alliances with Cadence and Synopsys."

High-Density Design

Several of the MMAC-Plus modules contain 22 XC4010 FPGAs (approximately 220,000 logic gates) each. The FPGAs are used to implement nearly all of the logic required for the design, including protocol converters and bus interfaces.

Rapid Time-to-Market With FPGAs and Synthesis

Getting the MMAC-Plus to market quickly was a top goal of the design project. The design was entered using Verilog-HDL, synthesized with Synopsys tools and implemented in Xilinx devices. By switching from schematics to a high-level description language, Cabletron was able to minimize design entry and verification times. Time-to-production was further decreased by using field-programmable Xilinx devices.



The MMAC-Plus universal hub uses 22 XC4010 FPGAs.

Looking to the Future

Cabletron has already completed 25 different designs for high volume production using Xilinx XC4000 devices, testimony to the working relationship between the two companies. According to Dennis Rainville, Cabletron's Manager of Hardware Development, "We're especially excited about the recent announcement of a five-year partnership between Xilinx and Synopsys. Their joint efforts to streamline high-level design for FPGAs should help to further improve development cycles for our future products." ◆

New Product Literature

Learn about the newest Xilinx products and services through our extensive library of product literature. The most recent pieces are listed below. To order please contact your local Xilinx sales representative. ♦

TITLE	DESCRIPTION	PART NUMBER
FPGAs		
XC3000A Family Overview	Features/benefits	#0010178-01
XC4000 vs. Altera FLEX	White paper	#0010189-01
EPLDs		
XC7336 Family Datasheet	Technical data	#0010190-01
XEPLD Translator Software Overview	Features/benefits	#500650-01
XC7000 vs. AMD MACH	White paper/features comparison	#0010188-01
Development Systems		
Xilinx Development Systems (with XACT 5.0) Overview	Features/benefits	#0010101-03
Corporate		
1994 Xilinx Databook	Technical data on FPGAs, EPLDs, PROMs, and development systems. Includes applications notes	#0401224-01

For a complete list, please contact your sales representative or see XCELL Issue #10.

THE FAWCETT

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grown larger and continues to grow faster than the gate array design community. Increasingly, logic synthesis tools are incorporating knowledge of FPGA architectures, both logically and topologically, leading to more efficient resource utilization. Future FPGA architectures will be influenced by the needs and capabilities of these synthesis tools.

Bidirectional links will be established between the synthesis/simulation tools and the FPGA 'place and route' implementation tools, allowing time and area constraints to be easily passed back and forth. The result will be a top-down design methodology that encompasses design creation, analysis, and physical implementation in a seamless software environment, improving both designer productivity and silicon efficiency.

Besides replacing older logic technologies, SRAM-based FPGAs have brought an important new capability to systems design — the ability to reconfigure logic "on-the-fly" during system operation. The coming decade will see the continued expansion of reprogrammable end-use applications, such as advanced ASIC emulation systems. *(This subject is worthy of a column of its own, so let's save it for a future XCELL ...)*

Xilinx is proud to be the world's leading supplier of CMOS programmable logic, and we are looking forward to continuing to expand the high-density programmable logic market that we pioneered and developed. But most of all, we are looking forward to continuing to serve the needs of you — our customers — who have made this all possible. Thanks for a great ten years! ♦

UPCOMING EVENTS

Mark Your Calendars

The fourth annual **PLD Design Conference and Exhibit** will be held April 11-13 at the San Jose Convention Center in San Jose, CA. This conference is intended for system-level engineers and engineering managers interested in the use of programmable logic devices. The first day is dedicated to tutorials, followed by two days of paper and panel sessions. Meanwhile, leading programmable logic and CAE suppliers will be exhibiting their products on the convention floor.

Xilinx products are prominently mentioned in several of the papers scheduled for presentation. Of particular interest is a Wednesday afternoon session on data communications applications that will feature case histories of three Xilinx-based designs. Bill Carter, Vice-President of Product Development for Xilinx, is a member of the Tuesday evening panel discussion on the future of programmable logic technology.

Our thanks to the many Xilinx users who submitted papers to this conference. Nearly 200 abstracts were submitted for the conference, and, with just 30 presentation slots available, the conference's technical program committee had to reject many worthy submissions.

The conference is sponsored by CMP Publications, the publishers of *Electronic Engineering Times*. For registration information, look for registration forms in *EE Times* magazine, or contact Kathleen Pizzo here at Xilinx (Tel: 408-879-5377 Fax: 408-879-4676). Be sure to drop by to visit us at the Xilinx booth!

Xilinx will be participating in several other conferences and workshops this spring. Look for Xilinx technical papers and/or product demonstrations at these upcoming industry forums:

Mid-Lantic Electronics Show
March 29 - 30, King of Prussia, PA

IEEE Workshop on FPGAs for Custom Computing Machines (FCCM '94)
April 10-13, Napa, California

Colloquium on Software Support & CAD Techniques For FPGAs
April 13, London, England

Fourth Annual Advanced PLD & FPGA Day
May 18, London, England

Canadian Workshop on FPGAs
June 13-16, Kingston, Ontario

Design Automation Conference (DAC)
June 6-10, San Diego, CA

PLD Design Conference
June 21-23, Tokyo, Japan

For further information about any of these conferences, contact Kathleen Pizzo (Tel: 408-879-5377 Fax: 408-879-4676).

FINANCIAL REPORT

Rapid Revenue Growth Continues

Xilinx Inc. achieved double-digit growth in the third quarter of FY94 (ended Jan 1, 1994). Sales revenues rose to $66.5 million, a 10.7 percent increase from the immediately preceding quarter. For the first nine months of the fiscal year, revenues increased 42 percent to $181 million compared to the same period in the prior fiscal year. *(Xilinx stock is traded on the NASDAQ exchange under stock symbol XLNX.)*

Revenues from all Xilinx logic families increased during this quarter. The major contributors were the high-density XC4000 and high-speed XC3100 FPGA families, with sales increases of 30 and 35 percent, respectively, compared to the previous quarter. The XC3100 family set a Xilinx record for the fastest sales growth of any product line in its first year of introduction, generating a total of $12 million in revenue over the last four quarters. ♦

COMPONENT AVAILABILITY CHART - FEBRUARY 1994

PINS	TYPE	CODE	XC2064	XC2018	XC2064L	XC2018L	XC3020	XC3030	XC3042	XC3064	XC3090	XC3020A	XC3030A	XC3042A	XC3064A	XC3090A	XC3020L	XC3030L	XC3042L	XC3064L	XC3090L	XC3120	XC3130	XC3142	XC3164	XC3190	XC3195	XC4003	XC4005	XC4006	XC4008	XC4010	XC4010D	XC4013	XC4002A	XC4003A	XC4004A	XC4005A	XC4003H	XC4005H	XC4025	XCZ236	XCZ272	XCZ236A	XCZ272A	XCZ336	XCZ354	XCZ372	XC3108
44	PLASTIC PLCC	PC44	◆	◆				◆				◆										◆																			◆		◆		N	◆			
	CERAMIC CLCC	WC44																																								◆		◆		N	◆			
48	PLASTIC DIP	PD48	◆																																															
64	PLASTIC VQFP	VQ64		◆	◆	◆						◆					◆																																		
68	PLASTIC PLCC	PC68	◆	◆	◆		◆	◆				◆	◆									◆	◆																					◆		◆		◆	◆			
	CERAMIC CLCC	WC68																																								◆		◆		◆	◆			
	CERAMIC PGA	PG68	◆																																															
84	PLASTIC PLCC	PC84		◆		◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	N	N	N	N	◆	◆	◆	◆					◆		◆			◆	◆		
	CERAMIC CLCC	WC84																																								◆		◆			◆	◆		
	CERAMIC PGA	PG84		◆			◆	◆	◆			◆	◆	◆								◆	◆	◆																			◆		◆			◆			
100	PLASTIC PQFP	PQ100					◆	◆	◆			◆	◆	◆								◆	◆	◆				◆							◆	◆														
	PLASTIC TQFP	TQ100		◆				◆	◆														◆	◆																											
	PLASTIC VQFP	VQ100				◆						◆	◆				◆	◆																		◆	◆														
	TOP BRZ. CQFP	CB100					◆		◆																											◆														
120	CERAMIC PGA	PG120																									◆							◆	◆	◆														
132	PLASTIC PGA	PP132							◆	◆				◆	◆								◆	◆																											
	CERAMIC PGA	PG132							◆	◆				◆	◆								◆	◆																											
144	PLASTIC TQFP	TQ144												◆	◆			◆	◆				◆															◆	◆											
	CERAMIC PGA	PG144																																																◆
156	CERAMIC PGA	PG156																										◆	◆									◆												
160	PLASTIC PQFP	PQ160								◆	◆			◆	◆								◆	◆	◆			◆	◆		N	N	N				◆	◆										◆
164	TOP BRZ. CQFP	CB164									◆																	◆																				
175	PLASTIC PGA	PP175									◆			◆											◆	◆																							
	CERAMIC PGA	PG175									◆			◆											◆	◆																							
176	PLASTIC TQFP	TQ176												◆						◆																													
191	CERAMIC PGA	PG191																													◆	◆				◆													
196	TOP BRZ. CQFP	CB196																														◆																	
208	PLASTIC PQFP	PQ208									◆			◆											◆	◆				◆	◆							◆	◆											
	METAL MQFP	MQ208																													◆	◆		◆															
223	CERAMIC PGA	PG223																								◆								◆							◆	N								
225	PLASTIC BGA	PB225																																																◆
	CERAMIC BGA	WB225																																																◆
	CERAMIC BGA	CG225																														N		N															
240	PLASTIC PQFP	PQ240																																																
	METAL MQFP	MQ240																																◆							◆								
299	CERAMIC PGA	PG299																																								N								

◆ = Product currently shipping or planned N = New since last XCELL

XILINX RELEASED SOFTWARE STATUS -FEBRUARY 1994

Product Category	Product Description	Product Function	Xilinx Part Number	Previous Ver. Rel.	Current Version By Platform					Last Update
					PC1 *5.0*	NC2 *3.30*	SN2 *4.1.x*	AP1 *10.4*	HP7 *9.01*	
XILINX INDIVIDUAL PRODUCTS										
CORE FPGA	XC2,3,4K Support	Core Implementation	DS-502-xxx	1.41	1.42	1.42	1.42	1.42	1.42	07/93
CORE EPLD	XC7K Support	Core Implementation	DS-550-xxx	4.00	4.10		4.10			08/93
Mentor[1]	V7	I/F and Libraries	DS-343-xxx	4.00				4.10		02/93
Mentor[1]	V8	I/F and Libraries	DS-344-xxx	1.00			1.10	1.10	1.10	07/93
OrCad[2]		I/F and Libraries	DS-35-xxx	4.22a	4.23	4.20				06/93
Synopsys[1]		I/F and Libraries	DS-401-xxx	2.00			3.01	3.01	3.01	09/93
Viewlogic[2]	ViewDraw	I/F and Libraries	DS-390-xxx	4.14	4.15					06/93
Viewlogic[2]	ViewSim	I/F and Libraries	DS-290-xxx	4.14	4.15					06/93
Viewlogic[2]		I/F and Libraries	DS-391-xxx	4.14	4.15		5.01			06/93
XABEL[2]		Entry, Sim, Lib, Opt.	DS-371-xxx	1.03	4.30		1.03			10/93
X-BLOX[1]		Architectural Synthesis	DS-380-xxx	1.03	1.04	1.04	1.04	1.04	1.04	10/92
XILINX PACKAGES										
Mentor 8	Standard		DS-MN8-STD-xxx	1.00			1.10	1.10	1.10	07/93
Mentor 8	Extended		DS-MN8-EXT-xxx	1.00			1.10	1.10	1.10	07/93
Mentor 7	Standard		DS-MN7-STD-xxx	1.00				1.10		07/93
Mentor 7	Extended		DS-MN7-EXT-xxx	1.00				1.10		07/93
OrCad	Base		DS-OR-BAS-xxx	1.10	1.20					07/93
OrCad	Standard		DS-OR-STD-xxx	1.10	1.20					07/93
Synopsys	Standard		DS-SY-STD-xxx	1.01			1.10	1.10	1.10	09/93
Viewlogic	Base		DS-VL-BAS-xxx	1.10	1.20		1.20			07/93
Viewlogic	Standard		DS-VL-STD-xxx	1.10	1.20		1.20			07/93
Viewlogic	Extended		DS-VL-EXT-xxx	1.10	1.20		1.20			07/93
Viewlogic/S	Base		DS-VLS-BAS-xxx	1.10	1.20					08/93
Viewlogic/S	Standard		DS-VLS-STD-xxx	1.10	1.20					08/93
Viewlogic/S	Extended		DS-VLS-EXT-xxx	1.10	1.20					08/93
XILINX HARDWARE										
Prom Pgmr.	Conf. Prom. Pgmr.	Software	HW-112	3.30	3.31					04/93
Programmer	Conf. Pgmr.		HW-120		3.14					
THIRD PARTY PRODUCTION SOFTWARE VERSIONS										
Cadence	Composer	Schematic Entry	N/A	4.2.2			4.30		4.30	N/A
Cadence	Verilog	Simulation	N/A	1.6.c.5			1.7BP		1.7BP	N/A
Cadence (Valid)	Concept	Schematic Entry	N/A	1.3-P3			1.60		1.60	N/A
Cadence (Valid)	Rapidsim	Simulation	N/A	2.0-P11			3.0BP		3.0BP	N/A
Mentor	NETED	Schematic Entry	N/A					7.XX		N/A
Mentor	QuickSim	Simulation	N/A					7.XX		N/A
Mentor	Design Architect	Schematic Entry	N/A	8.2			8.2_5	8.2_5	8.2_5	N/A
Mentor	QuickSim II	Simulation	N/A	8.1			8.2_5	8.2_5	8.2_5	N/A
OrCad	SDT	Schematic Entry	N/A			4.00				N/A
OrCad	VST	Simulation	N/A			4.00				N/A
OrCad	SDT 386+	Schematic Entry	N/A		1.10					N/A
OrCad	VST 386+	Simulation	N/A		1.10					N/A
Synopsys	FPGA/Design Comp.	Synthesis	N/A	3.0b			3.0c	3.0c	3.0c	N/A
Viewlogic	ViewDraw	Schematic Entry	N/A		4.1.3a		5.1			N/A
Viewlogic	ViewSim	Simulation	N/A		4.1.3a		5.1			N/A
Data I/O	ABEL Compiler	Entry and Simulation	N/A		4.3		1.03			N/A

NOTE: [1]FPGA Only [2]FPGA and EPLD

ALLIANCE PROGRAM - COMPANIES & PRODUCTS - FEBRUARY 1994

Company	Product Name	Version	Function	Vendor Interface Name	Libraries 2K/3K	Libraries 4K	X-BLOX Entry
Accel	Tango	1.3	Schematic Entry	SCH2XNF	✓	✓	
ALDEC	Susie	6.12	Simulation	SusieXNF	✓	✓	
Altium	P-CAD	6.0	Schematic Entry	PC-Xilinx	✓	*	
Cadence (Valid)	Concept	1.3	Schematic Entry	Xilinx Front End	✓	✓	✓
	Rapidsim	2.0	Simulation	Xilinx Front End	✓	✓	
	Composer	4.2	Schematic Entry	Xilinx Front End	✓	✓	✓
	Verilog	1.6	Simulation	Xilinx Front End	✓	✓	
Compass	Asic Navigator		Capture/Synthesis	Xilinx Design Kit	✓	✓	
CV (Prime)	Design Entry	2.0	Schematic Entry	Xilinx Kit	✓	✓	
Data I/O	FutureNet 6.0	5.03	Schematic Entry		✓	✓	✓
	Synario	1.0	Schematic Entry	Xilinx Library	✓	✓	
EPS	SIMETRI	2.0	Simulation	XNF2SIM	✓	✓	
Exemplar Logic	CORE	1.2	Synthesis	FS-001	✓	✓	
GenRad	System Hilo	4.3	Simulation	Xilinx Tool Kit	✓	✓	
IKOS	IKOS 2800/2900	5.02	Hardware Accelerator	Xilinx Tool Kit	✓	✓	
	Voyager	1.2	VHDL Simulation	Xilinx Tool Kit	✓	✓	
Intergraph	ACE Plus	4.7.5.5	Schematic Entry	Xilinx Design Kit 2.0	✓	✓	✓
	Advansim	7.0	Simulation	Xilinx Design Kit 2.0	✓	✓	
ISDATA	LOG/iC	3.4	Synthesis	XNF-PP	✓	✓	
Logic Modeling	Smart Model Library		Simulation Models	(In Library)	✓	✓	✓
	LM1200		Hardware Modeler	Xilinx Logic Module	✓	✓	
MINC	PLDesigner-XL	3.0	Synthesis	Xilinx Design Module	✓	✓	
Nishimura	G-DRAW	5.0	Schematic Entry	GDL2XNF	✓	✓	
	G-LOG	4.03	Simulation	XNF2GDL	✓	✓	
Omation (Division of Accel)	Schema III	3.34	Schematic Entry	Schema Xilinx Interface	✓	✓	
Phase Three Logic	CapFast	2.2	Schematic Entry	SCH2XNF	✓	✓	
Quad Design (Viewlogic Division)	Motive	3.4 Plus	Timing Analysis	XNF2MTV	✓	✓	
Racal-Redac (Viewlogic Division)	Visula	5.2	Schematic Entry	Xilinx Design Kit	✓	✓	
	CADAT	8.1&2000	Simulation	Xilinx Design Kit	✓	✓	
	Silcsyn	2.1	Synthesis	Xilinx Design Kit			
Simucad	Silos III	92.115	Simulation	Included	✓	✓	
Sophia Systems	Case Vanguard	4.1	Schematic Entry	Vanguard I/F Kit	✓	✓	
Teradyne	Lazar	6.4	Simulation	Laser I/F Kit	✓	✓	

* Call Altium at (408) 534-4148

New Training Courses

Xilinx has updated its training classes with the release of the XACT 5.0 Development System. At the same time, many new Regional Training Centers have been added around the world. It's now easier than ever to quickly become an expert on the latest Xilinx products!

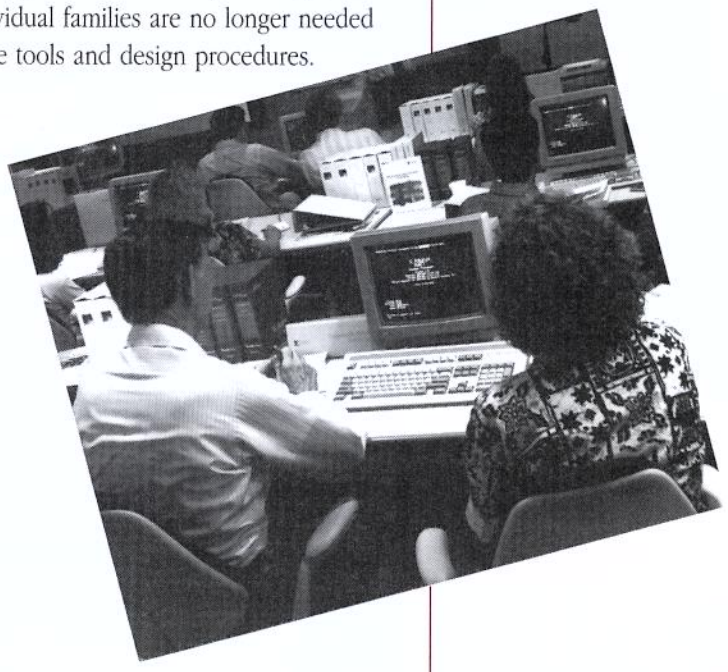
New XACT 5.0 Class

Starting in April, classes will cover the new products and features of the XACT 5.0 software. The classes have also been re-structured around the user's complete design flow instead of individual Xilinx tools. As a result, the classes should be even more effective in helping the new user become more productive in less time.

The standard Xilinx Training Class now lasts only three days, due to greater ease-of-use in the XACT 5.0 software. Also, only one class type will be offered, covering both the XC3000A and XC4000 families. Classes on individual families are no longer needed since XACT 5.0 allows both families to use the same tools and design procedures.

Course Outline

- Choosing a Device
- Design Entry Methods
  - Good Design Practices
- Designing for the Xilinx Architecture
  - Using Special Architecture Features
- Xilinx Translation Flow
  - Automatic Translation
  - Debugging and Verifying Translation
  - Incremental Design Flow
- Optimization of Designs
  - Floorplanning
- Choosing Configuration Options
  - Configuration Debugging
- Verifying Timing
  - Simulation Flow



All classes include detailed lab exercises, with one or two students per computer. The classes are not specific to any particular design entry or verification tool, but Viewlogic schematic entry tools are typically used in the lab examples.

New Regional Training Centers

Xilinx Training Classes are now taught in 42 locations in North America and 20 locations throughout the rest of the world! There are approximately eight classes per month in North America, allowing customers to attend when and where it is most convenient. International locations offer the added benefit of being taught in the native language by local instructors. Xilinx also has the ability to bring the training class to your own facility if you have a large group of engineers to train. ♦

For general information on training, contact your local sales office, or Xilinx Training at 408-879-5090 (Fax: 408-879-4676).

30% IN FIVE YEARS

FPGA Prices Continue to Fall

The notion that high-density programmable logic is a costly production solution is a thing of the past. Component price reductions effective in January marked the beginning of a more aggressive campaign to consistently lower prices on Xilinx devices, making them increasingly affordable for volume production. In fact, through increased unit volume, submicron process technology and new architectures, Xilinx has been able to reduce component prices up to 30% per year over the past five years.

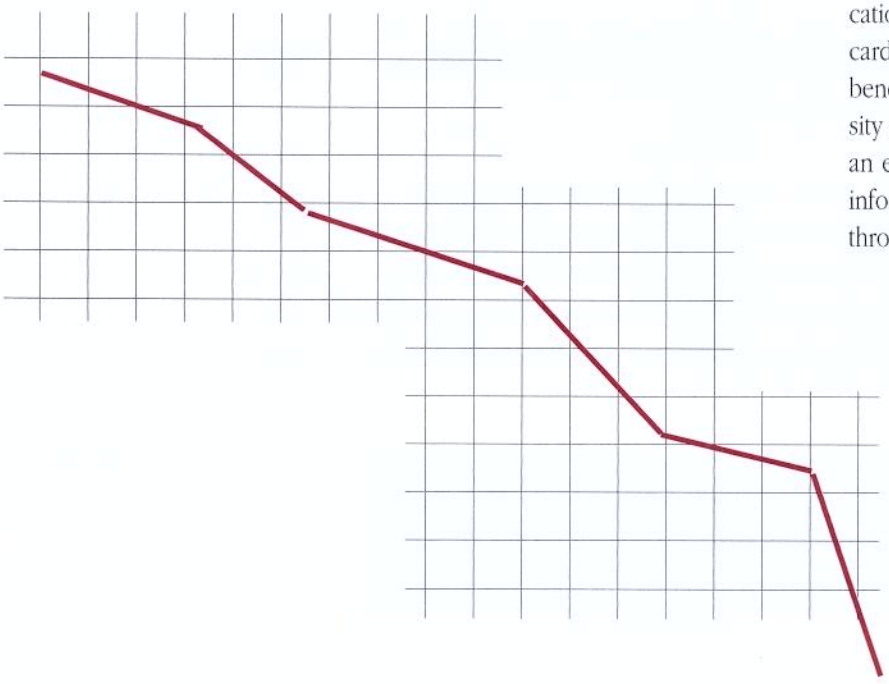
List prices for the XC2000, XC3000, and XC3000A families were reduced an average of 10%, reinforcing their position as the undisputed low-cost FPGA families. In addition, up to 15% price reductions for the XC3100 family provide increased value for high-performance applications.

XC4000 family pricing was reduced at an even higher rate — up to 40% — due mainly to the migration to more advanced sub-micron processes. With these new prices, the XC4000 family remains the ideal solution for high-density applications.

Our ability to consistently lower FPGA prices is based largely on cost savings made possible by continuous process technology improvements. In 1994, Xilinx is bringing a 0.6µ micron process into production. This miniaturization enables even the relatively mature XC3000 family devices to continue to follow a steep downward cost trend.

About 80% of Xilinx customers currently use FPGAs as a production solution; 25% of the designs involve volumes over 5000 units per year. The 1994 price reductions open the door for higher volume designs to realize the benefits of programmable logic. More importantly, new applications such as decoder boxes, add-on cards and motherboards will be able to benefit from the reprogrammability, density and peed of programmable logic — at an excitingly low cost. Look for more information on additional price reductions throughout 1994. ♦

"Xilinx has been able to reduce component prices up to 30% per year over the past five years."



Introducing the Logic Professor

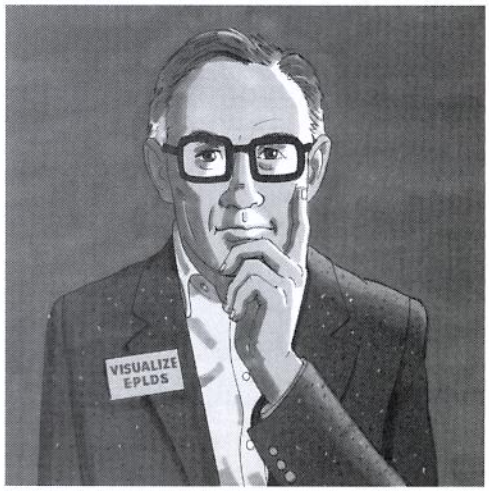
An Interactive Teaching Tool that Maps the Move from PALs and MSI to EPLDs

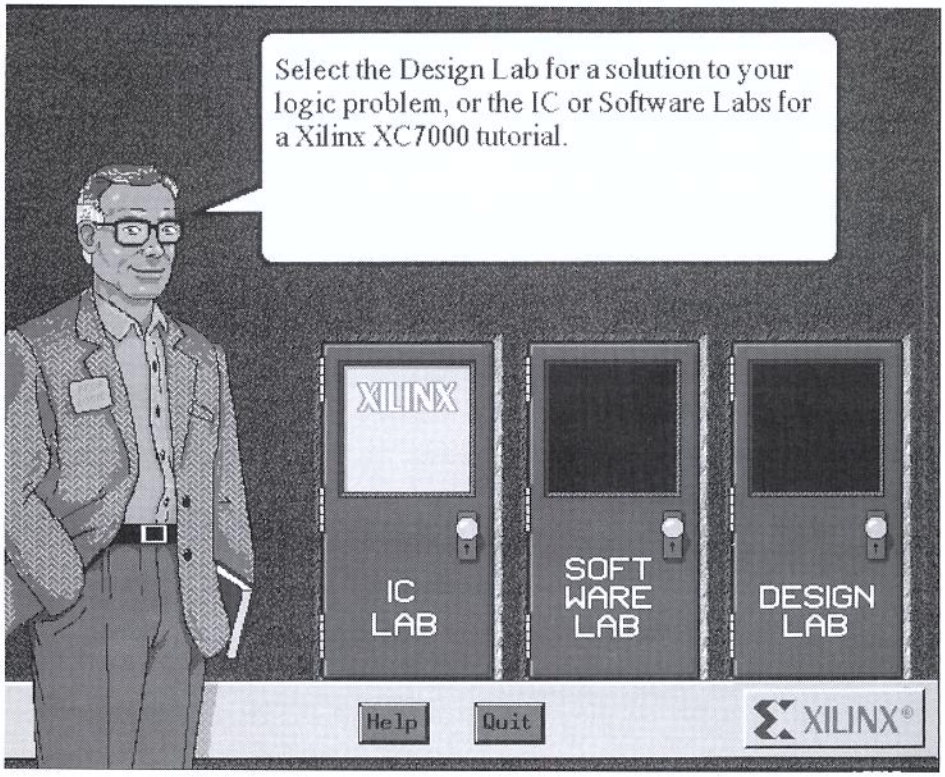
The Logic Professor is a free design estimator/demonstration for PAL/TTL and EPLD users, showing how Xilinx EPLDs can quickly and easily integrate multiple PAL, TTL, or EPLD devices while using less board space and lowering power consumption. The Logic Professor also acts as an interactive teaching tool that illustrates the IC and software benefits of Xilinx EPLDs.

Designed to run on IBM PCs and compatibles, the Logic Professor prompts the user to enter new or existing design specifications with the help of a "pop-up" menu listing of PAL, TTL, and EPLD devices. The Logic Professor then estimates the number and type of Xilinx EPLDs needed for the application.

The user also receives a print-out with the optimum solution highlighted. This print-out can be faxed to Xilinx to request pricing, technical or other information related to the design estimation.

The software is available at no cost by calling 1-800-231-3386. Call now for a copy of the Logic Professor and get your Logic PhD from Xilinx. ♦

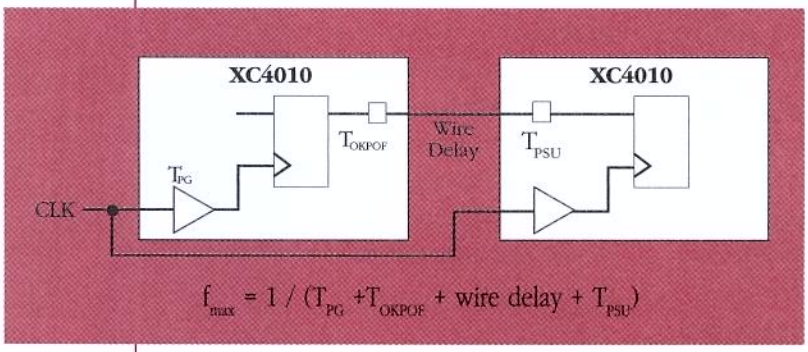




XILINX®

XC4000 I/O Boosts System Performance

In most synchronous systems, the data throughput rate is limited by the I/O timing parameters. The max data rate is determined by the sum of the max clock pad to output pad delay of the transmitting chip, plus the max input set-up time on the receiving chip. For reliable operation at any frequency, the designer must also evaluate potential hold-time problems that might occur when the delays are at their min extremes.



Xilinx has redesigned and re-specified the XC4000-4 devices for improved input set-up times, which are reflected in the guaranteed pin-to-pin specifications published in the 1994 Data Book.

For data transfer from one XC4000 device to another, the designer has three choices on the receiving device:

- Clock data into the input flip-flop (IFF) with delay. *This is the simplest method. There are no hold-time issues, but the max guaranteed data rate is only 40 MHz.*
- Clock data into the IFF without the extra input delay. *This is also very simple, and it gives the highest performance, 70 MHz, but the input has a hold-time requirement that makes this solution unusable in most cases.*
- Clock data without extra delay into the nearest CLB flip-flop. *This requires more attention to CLB placement, but it achieves high performance while avoiding hold-time problems.*

The first two methods can easily be analyzed using the published pin-to-pin parameters. For the third method, input set-up and hold times must be calculated from the IOB, CLB and clock-distribution parameters.

The max input set-up time is the sum of the max input and routing delays plus the max set-up time of the CLB flip-flop, minus the shortest clock distribution delay that is consistent with the assumption of max values for the input delays. Xilinx recommends a very conservative assumption of 70% on-chip delay tracking, which means that only 70% of the max clock distribution delay should be subtracted in the set-up time calculation.

The hold-time analysis follows the same path, but uses the CLB flip-flop hold time, uses the max value for the clock distribution delay, and uses only 70% of the data input delay, consistent with the assumption of 70% delay tracking. This analysis shows a hold time requirement on the input, albeit only a few ns.

On the output, Xilinx guarantees a min delay that is 25% of the max delay specified for the fastest speed-version of the device. This guaranteed min output delay is longer than the required hold time on the input, which makes the design safe.

Using CLB flip-flops as data inputs is the recommended method for high-performance designs, IFF with delay are recommended for less demanding systems. ◆

XC4005-4 I/O Data Transfer Worst-Case Timing Parameters

Method	CLK-out	Trace	Set-Up Time	Hold Time	Total	Frequency
IFF with delay	12.0	1.0	12.0	0	25.0 ns	40 MHz
IFF fast	12.0	1.0	1.2	4.5	14.2 ns	70 MHz
CLB-FF, fast	12.0	1.0	3.25	2.63	16.25 ns	62 MHz

XC3195 Benchmarks Demonstrate High Speed and Density

The PREP™ benchmark results for the XC3195™ FPGA are being prepared for submission to the PREP committee for verification.

The PREP capacity results *(see table)* reflect the fact that the XC3195 array is 50 percent larger than the XC3090/XC3190. While logic utilization in actual system-level designs may not increase as much as the PREP benchmarks indicate, the higher capacity of the XC3195 makes it an ideal device for XC3090 users who need additional logic.

The PREP capacity of the XC3195 indicates that it is larger than a XC4006, ignoring the on-chip RAM, JTAG, and other features of the XC4006. This makes the XC3195 the most cost-effective part for designs larger than 5,000 usable gates which do not need the system features of the XC4000 family.

The XC3195-3 performance benchmarks are in the final stages of preparation; preliminary results confirm that the XC3195 is the fastest device in production at this density level. The XC3195's performance is as fast as the rest of the XC3100 family. Unlike most competitive offerings, there is no performance penalty when moving to larger arrays in the Xilinx FPGA families. ♦

"The XC3195-3 performance benchmarks are in the final stages of preparation; preliminary results confirm that the XC3195 is the fastest device in production at this density level."

A PREP COMPANY

Presentations use or include the most recent uncertified(*) PREP PLD Benchmark data which was measured according to Benchmark Suite #1, Version 1.3. Any analysis is ***not endorsed by PREP.***

PREP Capacity benchmarks (automatic, no manual intervention):

Benchmark	Number of Instances XC3090A	XC3195
1. Datapath*	35	56
2. Timer/Counter	13	20
3. Small State Machine	20	29
4. Large State Machine	9	14
5. Multiply/Accumulator	13	21
6. 16-Bit Accumulator	20	30
7. 16-Bit Counter	26	40
8. 16-Bit Prescaled Counter	13	20
9. Memory Map*	25	36
Average	**19.3**	**29.6**

** Benchmarks 1 & 9 - the use of logic synthesis results in some logic common to each instance being implemented only once.*

New Standard Military Drawings (SMDs) for FPGAs

Xilinx is an active participant in the SMD (Standard Military Drawing) program promoted by the U.S. Government. By specifying SMDs, users obtain a product intended for high-reliability and military applications, without having to generate their own device specifications. These standard military products are available at lower cost and with shorter lead times than customer-specific versions.

New SMDs have been released for a number of Xilinx FPGA products, including the high-density XC4005 and XC4010 FPGAs, and -100 speed grade versions of the XC3000 family devices. Also, previously-issued SMD numbers for some XC3000 family FPGAs have been revised to match the Department of Defense's latest part numbering conventions. The accompanying table lists the current SMD numbers for Xilinx FPGAs.

"B" grade P/N	Current SMD P/N	Comments
XC3020-50PG84B	5962-8994801MXC	New number replaces 5962-8994801XC
XC3020-70PG84B	5962-8994802MXC	New number replaces 5962-8994802XC
XC3020-100PG84B	5962-8994803MXC	New -100 speed grade
XC3020-50CQ100B	5962-8994801MYA	New number replaces 5962-8994801YA
XC3020-70CQ100B	5962-8994802MYA	New number replaces 5962-8994802YA
XC3020-100CQ100B	5962-8994803MYA	New -100 speed grade
XC3042-50PG84B	5962-8971301MXC	New number replaces 5962-8971301XC
XC3042-70PG84B	5962-8971302MXC	New number replaces 5962-8971302XC
XC3042-100PG84B	5962-8971303MXC	New -100 speed grade
XC3042-50CQ100B	5962-8971301MYA	New number replaces 5962-8971301YA
XC3042-70CQ100B	5962-8971302MYA	New number replaces 5962-8971302YA
XC3042-100CQ100B	5962-8971303MYA	New -100 speed grade
XC3042-50PG132B	5962-8971301MZC	New number replaces 5962-8971301ZC
XC3042-70PG132B	5962-8971302MZC	New number replaces 5962-8971302ZC
XC3042-100PG132B	5962-8971303MZC	New -100 speed grade
XC3090-50PG175B	5962-8982301MXC	New number replaces 5962-8982301XC
XC3090-70PG175B	5962-8982302MXC	New number replaces 5962-8982302XC
XC3090-100PG175B	5962-8982303MXC	New -100 speed grade
XC3090-50CQ164B	5962-8982301MYA	New number replaces 5962-8982301YA
XC3090-70CQ164B	5962-8982302MYA	New number replaces 5962-8982302YA
XC3090-100CQ164B	5962-8982303MYA	New -100 speed grade
XC3090-50CB164B	5962-8982301MZC	New number replaces 5962-8982301ZC
XC3090-70CB164B	5962-8982302MZC	New number replaces 5962-8982302ZC
XC3090-100CB164B	5962-8982303MZC	New -100 speed grade
XC4005-10PG156B	5962-9225201MXC	
XC4005-6PG156B	5962-9225202MXC	
XC4005-10CB164B	5962-9225201MZC	Quad flat pack with body mark
XC4005-6CB164B	5962-9225202MZC	Quad flat pack with body mark
XC4005-10CB164B	5962-9225201MYC	Quad flat pack with lid mark
XC4005-6CB164B	5962-9225202MYC	Quad flat pack with lid mark
XC4010-10PG191B	5962-9230501MXC	
XC4010-6PG191B	5962-9230502MXC	
XC4010-10CB196B	5962-9230501MYC	Quad flat pack with body mark
XC4010-6CB196B	5962-9230502MYC	Quad flat pack with body mark
XC4010-10CB196B	5962-9230501MZC	Quad flat pack with lid mark
XC4010-6CB196B	5962-9230502MZC	Quad flat pack with lid mark ◆

And the Survey Says ...

Customer Response to Survey Provides High-Quality Information

In late 1993, we surveyed nearly 1,000 randomly-selected Xilinx customers worldwide. A few of the interesting results:

- More than 80 percent of Xilinx users employ FPGAs in volume production. About 50 percent use them in system level beta testing. Also, 30 percent use FPGAs for ASIC prototyping.
- The four reasons cited most often as to why FPGAs are used instead of other design alternatives:
  - Design flexibility: 85 percent
  - Board space: 70 percent
  - Ease-of-implementation: 60 percent
  - Time-to-market: 60 percent
- Almost two-thirds of XC4000 users have taken advantage of the speed and density benefits of using the on-chip RAM capability in their applications. The three most often cited uses of on-chip RAM are:
  - Blocks of memory of less than 1K bits
  - Register files or data registers
  - FIFOs or data buffers.

One lucky user will receive an Apple Newton in our random drawing of survey respondents. Thanks to all of you who took the time to respond. ♦

High-Density, High-Speed Serial PROM Family Expanded

The XC1700 family of Serial Configuration PROMs is being extended with the addition of the XC17128D and XC17256D products. These devices are fabricated with our proven, highly-reliable EPROM technology, and are designed to mate perfectly with the Xilinx XC2000, XC3000 and XC4000 FPGA families. A single XC17256D PROM can be used to completely configure any Xilinx FPGA up to and including the XC4013. The XC17128D replaces the existing XC17128.

Both devices provide significant benefits:

- Higher speed: > 10 MHz serial access rate
- Improved ESD protection
- Small space requirement - available in the SO8 package

The XC17256D and XC17128D will be sampling in the second quarter of 1994, with full production planned for the third quarter. ♦

Table

In the table below, FPGA device types are listed under the smallest XC1700 family serial PROM that can hold an entire single configuration bitstream for that FPGA. Multiple PROMs can be cascaded to support multiple FPGAs and/or multiple configurations.

XC1718D	XC1736D	XC1765D	XC17128D	XC17256D
XC2064	XC3x30/A	XC3x64/A	XC3195/A	XC4008
XC2018	XC3x42/A	XC3x90/A	XC4005/A/H	XC4010
XC3x20/A	XC4002A	XC4003/A/H	XC4006	XC4013
		XC4004A		

Synopsys and Xilinx Announce Partnership

Synopsys and Xilinx announced a five-year agreement to co-develop an advanced high-level design solution for field-programmable gate arrays (FPGAs) on January 24, 1994. The two companies will streamline high-level design for FPGAs in order to improve design methodology and silicon efficiency.

Synopsys President Aart deGeus and Xilinx COO Wes Patterson discuss the five-year partnership agreement.

The two companies will focus on reducing the two critical elements of time-to-market:

- Time-to-design using high level design automation tools
- Time-to-production using low-cost, user-programmable logic.

Synopsys and Xilinx are developing a fully-integrated design environment, including the first bi-directional link between synthesis and simulation tools and FPGA design software. This spring, Synopsys will deliver a new release of FPGA Compiler™, and Xilinx will ship a new version of its timing-driven router (PPR) in XACT 5.0. Synopsys' FPGA Compiler will forward-annotate synthesis timing constraints to be read by XACT-Performance™, that will then partition, place and route the design to meet those constraints. This is a technique being used successfully in ASIC design.

Xilinx expects to release a new version of the FPGA libraries for Synopsys' FPGA Compiler in the first half of 1994. The release will include Xilinx's first VHDL gate-level simulation models generated by Synopsys' Library Compiler™ to be used with Synopsys' VHDL System Simulator™ (VSS). FPGA Compiler will provide a new XNF reader to enable back-annotation of delays from Xilinx's XACT to Synopsys' simulation and synthesis tools.

Another result of the agreement is the on-going development of Xilinx libraries using Synopsys' DesignWare Developer™ to automatically insert Xilinx X-BLOX™ modules into synthesized designs. The X-BLOX modules are compiled library components that automatically use the unique features of the Xilinx FPGA families.

Synopsys and Xilinx will also develop additional features in the FPGA Compiler that will take full advantage of future Xilinx architectures. The goal of this work is to increase the performance of customer designs and minimize routing congestion.

One year ago, Synopsys introduced FPGA Compiler, a synthesis compiler that includes algorithms to target Xilinx's configurable logic blocks (CLBs). This modification enabled FPGA Compiler to utilize Xilinx XC4000 family devices more efficiently and very accurately predict chip area usage. Since the two companies began working together, Synopsys and

Xilinx have improved device performance and utilization up to 20 percent by enhancing synthesis tools for FPGAs.

"Production FPGA solutions require the most efficient use of silicon — the highest performance and lowest possible cost," said Wes Patterson, chief operating officer of Xilinx. "This agreement will result in optimized gate utilization, allowing designers to pack as much as possible into a device." Longer term, the companies are collaborating on new FPGA architectures under design at Xilinx. These new FPGA architectures are expected to produce even better results with a high-level design methodology.

> *"Since the two companies began working together, Synopsys and Xilinx have improved device performance and utilization up to 20 percent by enhancing synthesis tools for FPGAs."*

"Customers who are designing programmable logic above 10,000 gates realize that productivity decreases dramatically if they do not synthesize. The higher the gate count, the more significant the need for automated design becomes," said Dr. Aart de Geus, president and CEO of Synopsys. "Working together, Synopsys and Xilinx will develop the software, methodologies, and silicon that respond to these needs." ◆

XACT 5.0
ACCELERATING YOUR PRODUCTIVITY

XACT 5.0 SCHEDULE UPDATE

Ambitious New Version to Ship in April

XACT 5.0 contains many exciting new features that will improve the EPLD and FPGA design process. *(See XCELL Issue 11, pages 17-23.)* It is the most ambitious software update in Xilinx history, and reflects our continuing commitment to provide the most-advanced development tools for EPLD and FPGA design.

As part of the XACT 5.0 development effort, Xilinx has instituted a more rigorous testing process to ensure delivery of a high-quality product. This process is designed not only to eliminate bugs, but to also test for smoother design flows, increased routing completion rates, and decreased compilation times. In order to achieve these improved standards, the XACT 5.0 release is now scheduled for initial shipment in April, 1994. Approximately six weeks will be required to update our large user community; all registered users should receive their updates before the end of May.

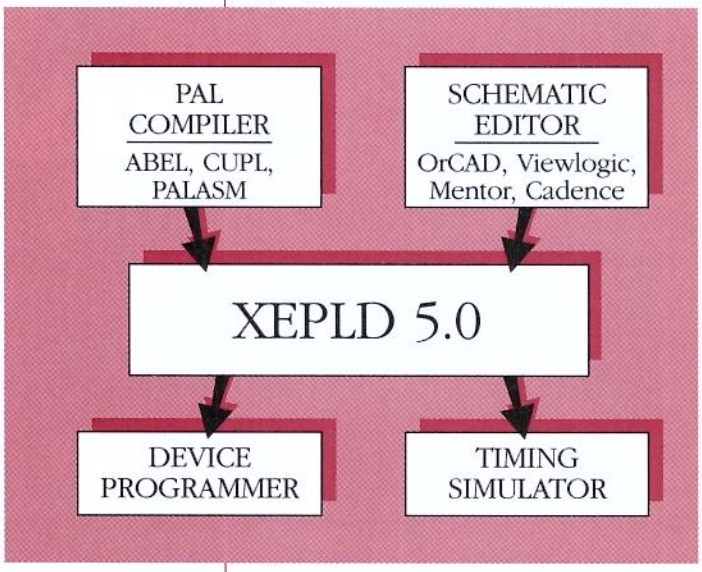
Users that have let their software maintenance agreements lapse and are interested in reinstating support should contact their local Xilinx sales representative or distributor.

Users unsure of their maintenance status should contact Xilinx Customer Service (Tel: 408-559-7778, FAX: 408-559-0115). ◆

Advanced EPLD Developmen

XEPLD 5.0 is the latest version of the Xilinx EPLD development software. It provides a complete, low-cost, user-friendly design environment for creating behavioral or schematic designs on a variety of development platforms.

New users can quickly produce high-performance efficient designs since XEPLD 5.0 is easy-to-learn, easy-to-use, and provides a full range of automatic features. A detailed understanding of the EPLD architecture is not required. Advanced users can override the automatic features and fine-tune every aspect of the design.



XEPLD 5.0 is a total solution for creating Xilinx EPLD designs. Now priced at only $89.95, the benefits of this comprehensive development environment are available to every designer. The beta version of the software is shipping now, and production shipments will begin in late March, 1994.

Third-Party Support

For behavioral design entry, XEPLD supports industry-standard PLD compilers such as ABEL, CUPL, and PALASM, in addition to the built-in PLUSASM Boolean equation assembler. Many PLD users are already familiar with these design tools.

For schematic entry, a comprehensive unified component library allows the user to target either a Xilinx EPLD or FPGA device. The library includes familiar TTL and PAL components for use with industry-standard schematic editors such as those available from OrCAD, ViewLogic, Mentor Graphics, and Cadence Design Systems.

For design verification, XEPLD supports various third-party simulators such as ViewLogic ViewSim, OrCAD VST, Mentor Quicksim, Cadence Verilog, and Cadence Rapidsim. EPLD device models are available from Logic Modeling Corp. for board-level simulation on a variety of platforms.

Feature Summary

- **Automatic Optimization and Mapping**
  Designs are automatically minimized and mapped into the device for optimal efficiency and high performance. Critical logic functions are assigned to special resources such as input registers, high speed clocks, and global output enable signals. This allows the user to concentrate on design functionality without concern for physical implementation.
- **Automatic Use of UIM® Resources**
  The Universal Interconnect Matrix (UIM) used in Xilinx EPLDs provides an additional level of logic with no additional delay. XEPLD 5.0 automatically uses the inherent logic capability of the UIM whenever possible to reduce macrocell requirements and increase speed.
- **Automatic Arithmetic Functions**
  The EPLD architecture includes high-

XACT 5.0 ACCELERATING YOUR PRODUCTIVITY

Software Released

speed ALUs with dedicated fast-carry signal routing. These interconnections between ALUs are created automatically, simplifying the process of arithmetic logic design.

- **Automatic PAL Conversion**
  XEPLD automatically converts existing PAL equation files that can be used in behavioral or schematic designs. Combined with the PAL-like architecture of the EPLDs, this allows the user to quickly and easily consolidate multiple PALs into a single EPLD.
- **Complete Design Control**
  Users have the option to override the automatic features of XEPLD and selectively control any or all device resources. In addition, design iterations are easily accomplished because the pinouts can be retained; updating old designs does not require printed circuit board changes.
- **High Speed Compilation**
  Design changes are easily performed and the results are quickly reported.
- **Multiple Platform Support**
  XEPLD runs on Sun, HP, PC (DOS), and IBM RS6000 platforms. ♦

"XEPLD 5.0 is a total solution for creating Xilinx EPLD designs."

3-Volt Adapter for XChecker Cable Now Available

The XChecker cable has proven an invaluable tool to designers using Xilinx FPGAs. With the XChecker, users can download bitstreams directly from a PC or workstation to FPGAs in the target system, and readback FPGA memory and register contents. The XChecker cable is included with the XACT Development System, and additional cables can be purchased as a separate product.

A 3-volt adapter for the XChecker Cable is now available to designers using the Zero+ XC2000L and XC3000L family devices. This adapter connects between the XChecker cable and the target board. The new adapter is available to all users as a separately priced option *(Order Code: HW-XCH3V, Price: $95).*

Key features of the 3V adapter include:

- Connects to existing XChecker cable, using the 18-pin connector
- On-Board DC to DC converter
- Level translation for logic signals
- Accepts any V_{CC} supply voltage from 2.9 V to 5.2 V

To order the 3-volt adapter contact your distributor or Xilinx Sales representative. ♦

New EPLD Fitter for Open ABEL 5.1 and CUPL

Xilinx has introduced its first EPLD fitter supporting both Open ABEL 5.1 and CUPL. The fitter operates within the host compiler and provides fully automatic operation, translating the logical design into a device programming file. The user does not need to know Xilinx devices or software to produce efficient, high-performance EPLD designs.

Advanced Features

The Xilinx fitter offers many automatic features that reduce design time:

- Dual Block Architecture support - creates both high density and high speed designs.
- Arithmetic Logic support - uses the on-chip ALUs to increase speed and density.
- Global Optimization - assigns high-speed clocks, three-state controls, input registers.
- Local Optimization - controls component collapsing and partitioning.
- Input Register Assignment - reduces macrocell resource requirements.
- UIM AND Gate support - provides an additional level of logic with zero delay.

Familiar Design Environment

Both CUPL and ABEL provide the user with a complete design environment that includes state machine, HDL, and Boolean equation entry, as well as functional simulation. This allows the user to quickly create designs using familiar development tools that are independent of the target device. When the design is complete, the user simply selects a Xilinx EPLD from the device menu to begin the automatic fitting process.

Automatic Logic Optimization

The fitter minimizes the design equations and optimizes the logic to produce the most efficient implementation for the target device. This allows the user to concentrate on design functionality without regard to physical device implementation, achieving an efficient use of device resources as well as high performance, automatically.

Precise Design Control

Though the fitter is fully automatic and transparent to the user, every aspect of the fitting process can be controlled with property statements. This allows the user to control design optimization, specify logic placement, and fine-tune design performance.

> *"The user does not need to know Xilinx devices or software to produce efficient, high-performance EPLD designs."*

Comprehensive Design Reports

The fitter produces detailed reports that show all relevant design parameters, such as pin assignments and chip resource utilization. In addition, an equation report shows the final design solution after logic collapsing and minimization in the form of a readable equation file. These reports allow the user to effectively correct and manipulate designs at any level of detail.

Customer Support

The Xilinx EPLD fitter is ordered through Data I/O Corp. (for ABEL) or Logical Devices Inc. (for CUPL). Support is provided by these companies through their technical support hot-lines.

Customers may also contact Xilinx for additional information about the fitter. ◆

Cadence Design Systems Enhances Its Xilinx Design Kits

Cadence Design Systems has continued to enhance the Xilinx Design Kits for the Cadence Design Environment. A number of bug fixes and enhancements have been included in the latest release, including improvements to the GXILINX utility, which enables Concept logical information and constraints to be passed to the Xilinx 'place and route' tools. A number of library components also were recently enhanced.

Cadence and Xilinx are working together to ensure a timely release of the new Unified Library associated with the upcoming XACT 5.0 release. The new release of the Cadence Design Kit to support XACT 5.0 will be available in the second quarter of 1994.

As a member of the Xilinx Syndicate Program, Cadence is improving the efficiency and performance of the Synergy Synthesis software. The Synergy Synthesis compiler for Verilog-HDL and Leapfrog-VHDL will be enhanced to support XBLOX mapping and constraint passing, and is also targeted for a second quarter 1994 release.

"As a member of the Xilinx Syndicate Program, Cadence is improving the efficiency and performance of the Synergy Synthesis software."

For further information, contact Itzhak Shapiro at 408-428-5739 or your local Cadence sales office. ◆

ISDATA Improves Support for Xilinx FPGAs

Release 4.0 of the LOG/IC Gates compiler from ISDATA incorporates a new technology mapper developed by Xilinx, resulting in more efficient implementations when targeting Xilinx FPGAs. The compiler supports the design of state machines and other complex logic circuits using a high-level syntax, producing an output in the Xilinx Netlist Format (XNF). Release 4.0 supports the XC2000, XC3000 and XC4000 FPGA families.

ISDATA, a German CAE company, has offered innovative solutions for design synthesis for the past ten years, and was one of the first companies to offer logic synthesis for both PLDs and FPGAs. ISDATA is an active member of the Xilinx Alliance Program and worked closely with Xilinx in the development of this latest release.

For further information, please contact Paul Hoy at 408-373-7359 (USA), Ralph Remme at 49-721-751087 (Germany) or your local ISDATA sales representative. ◆

XACT 5.0 ACCELERATING YOUR PRODUCTIVITY

The XACT 5.0 Release:

What's in the Box?

The XACT 5.0 Release Update box has been carefully organized to make your transition to XACT 5.0 tools fast and easy. All boxes are organized in a top-to-bottom or left-to-right manner so you can quickly get what you need.

- **Getting Started Envelope** - Contains everything you need to get going: your registration card, the product release note, and Installation Guide. The release note has been restructured since the last update so that explanations of product contents, new software features, and known problems and workarounds are clear. The new Installation Guide provides easy-to-follow instructions for all Xilinx software products. Please don't forget to fill out and mail your registration card!
- **Additional Information Packet** - The latest news and technical information, including information on Xilinx training, special offers and services.
- **Disks** - Your Xilinx software is packaged as either one CD-ROM disk or a set of floppy disks. CD-ROM quick installation instructions are printed right on the case. Floppies are installed by inserting the first disk and issuing the drive:install command.
- **Manuals** - Updated manuals are at the bottom of the box, along with Quick-Reference Cards for selected products. New features and new product tutorials have been added in the XACT 5.0 documentation.

> *"The new Installation Guide provides easy-to-follow instructions for all Xilinx software products."*

We recommend the following procedure for getting started with your XACT 5.0 update:

- **Step 1 : Fill out and return your Registration Card.** Fill out and return the registration card for each product you own. This ensures that you receive future updates and important product information. Save the card stubs with the serial number information in your envelope — these serial numbers act as your proof of purchase.
- **Step 2 : Read the Release Note for your product.** Next, become acquainted with the release note. Verify that you have everything listed in the "product contents" section. Make note of the new features that are of interest to you so you can remember to read more about them in your updated manuals. A new document, the "Design Migration Guide," describes how to use XACT 5.0 with existing designs. Unless you plan to use XACT 5.0 with new designs only, this information is extremely important to understand. The "problems and workarounds" section alerts you to common tool issues. The notes also indicate who to contact at Xilinx when you need assistance.
- **Step 3: After consulting the Installation Guide, install your software.** Now you are ready to install your new software. The Installation Guide details

XILINX®

the basic installation steps as well as important issues like using your PC authorization key or workstation license, managing your hard disk space and installing over existing software.

- **Step 4 : Try a tutorial or read about new features.**
  Xilinx has tutorials for each supported interface product that guide you through sample uses, often demonstrating new features in the process. The manuals provide detailed information about all new features and design flows.

- **Step 5 : Contact Xilinx with any questions that arise.**
  We want to ensure that your transition to XACT 5.0 goes as smoothly as possible. Contact our technical support hotline or local Xilinx Application Engineer whenever you have a question that is not answered by the documentation. ♦

XACT 5.0
ACCELERATING YOUR PRODUCTIVITY

XACT 5.0 Update Contents:

Getting Started Envelope	Registration Card, Release Notes, Installation Guide
Additional Information Packet	*XCELL* journal, special offers and services, training course brochure.
Software	Software media (for specific PC products, software protection keys will be included as well — *see XCELL, Issue 11, Fourth Quarter 1993*)
Manuals	Updated documentation for your products

Design Methodology Notes Now Available For Synopsys

A designer's style in using a hardware description language (HDL) has a major effect on the characteristics of the resulting synthesized implementation logic. The organization of (and choice of constructs in) an HDL description determine the basic architecture of a design.

While HDL Compiler from Synopsys automates most of the logic-level decisions and relieves a designer from many implementation details, there are fundamental differences in coding for ASICs versus FPGAs. These differences can greatly affect the quality of results and therefore should be understood before starting a design. To highlight these differences, Xilinx has published "Xilinx Synopsys Interface: Design Methodology Notes for Synopsys." This application note includes examples of how to efficiently code HDL designs and how to use Synopsys commands to increase the performance and/or improve the density of an FPGA design.

Copies of this application note have been mailed to registered owners of the DS401 Synopsys Interface. To obtain a copy, contact your local Xilinx representative or distributor. ♦

Implementing High-Performanc

The ability to implement blocks of RAM memory within an XC4000 FPGA allows the implementation of memory structures such as FIFO buffers. Including FIFO buffers on-chip increases the level of system integration and contributes to system performance by eliminating the I/O delays associated with accessing a discrete FIFO buffer device.

The four components of a RAM-based FIFO are shown in Figure 1. To control the RAM, the address-logic block maintains two addresses, one for the current write location, where data is PUSHed, and one for the current read location, from which data is POPped. Following a PUSH or a POP, the corresponding address is incremented, causing data to be written and read sequentially.

The flag logic uses the read and write addresses to determine the status of the memory. If the memory contains no valid data, an EMPTY flag is created; a FULL flag is created when all memory locations are occupied.

The arbitration logic, for the most part, simply passes PUSH and POP requests to the RAM. Simultaneous PUSH and POP requests, however, must be resolved. The simplest schemes have a fixed priority, with either PUSH or POP being designated as the priority operation. If the priority operation is not possible because the RAM is full or empty, the priority should be overridden. Other schemes can alternate in priority between PUSH and POP, or favor one operation while its request persists.

The FIFO design described here depends on read-modify-write operation of the RAM, with Write Enable asserted every cycle. A data multiplexer permits "non-write" cycles by rewriting existing data into the RAM *(see XCELL Issue 11, page 26)*. The same multiplexer provides bank selection for RAM expansion, permitting any size FIFO.

Figure 2 shows the RAM and its address counters. A key element is the use

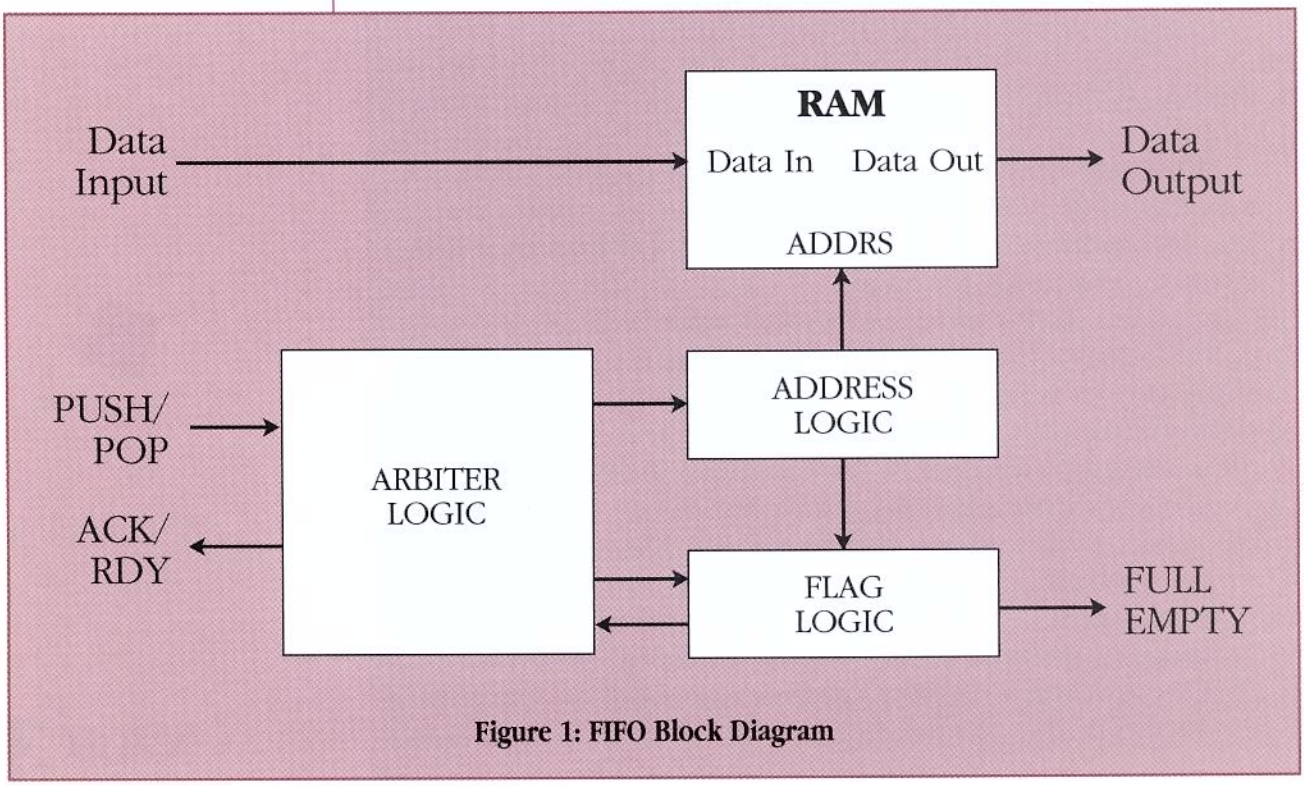


Figure 1: FIFO Block Diagram

RAM-Based FIFOs

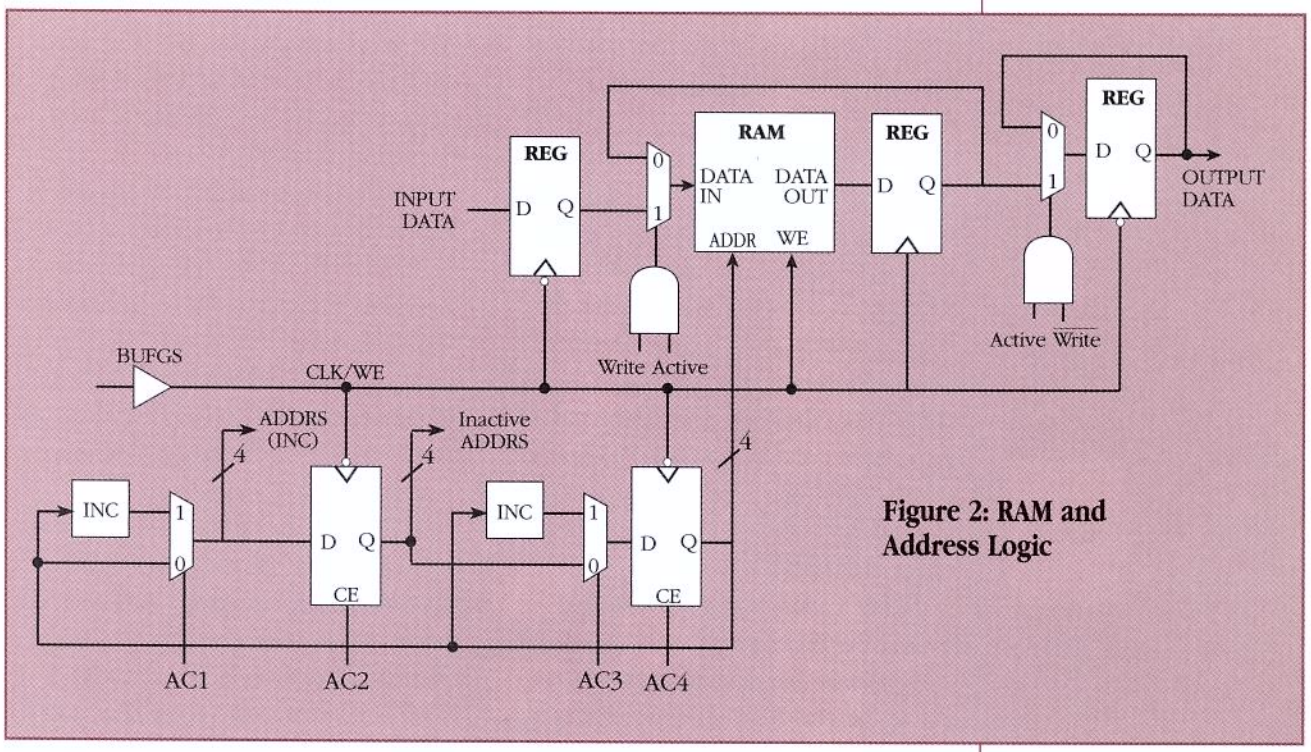


Figure 2: RAM and Address Logic

of a BUFGS to drive the RAM Write Enable and clock the address register. The low skew of the global net ensures that the data and address hold times are met. The RAM is written every clock cycle, and the multiplexer preceding the RAM determines whether new data is entered or the old data is re-entered. If it is necessary to expand the RAM, a bank select signal, derived from the address counter, can be ANDed with the Active signal to limit writing to a single bank of RAM. In addition, a read-data-select multiplexer must be provided.

The address-generation logic is shown in the lower portion of Figure 2. The right-hand register contains the address currently being used by the RAM, the write address during a PUSH and the read address during a POP. The left-hand register contains the address that is not in use.

The address-logic instruction set *(see table)* permits the active address to be incremented and remain active for successive PUSHes or POPs, or be incremented and become inactive for a PUSH followed by a POP, or vice versa. It also permits the addresses to remain unchanged or simply interchanged.

FULL and EMPTY flags are generated in the flag logic, Figure 3. Flags can only be asserted or de-asserted during active PUSH or POP cycles, and both are triggered when the incremented active RAM address becomes equal to the inactive

Continued on the next page

Table: Address Logic Instruction Set

Current Operation		Next Operation	AC
R/W	Act/Inact	R/W	1 2 3 4
Read	Active	Read	1 0 1 1
Read	Inactive	Read	X 0 X 0
Write	Active	Read	1 1 0 1
Write	Inactive	Read	0 1 0 1
Read	Active	Write	1 1 0 1
Read	Inactive	Write	0 1 0 1
Write	Active	Write	1 0 1 1
Write	Inactive	Write	X 0 X 0

Continued from the previous page

address. If this equality occurs during a PUSH cycle, the new write address contains the next data to be POPed, and the FIFO is full. If equality is reached during a POP, the FIFO is empty since the new read address is waiting to be written in the next PUSH operation.

Consequently, the flags can be generated by gating the comparator output with the Write signal and registering it during active RAM cycles. The address-logic instruction set is constructed such that the inactive address and the incremented active address are always available to the comparator. The flags clear on the next active RAM cycle, when the addresses become non-equal. For correct operation, this cycle must be a PUSH if the FIFO is empty or a POP if it is full.

Figure 4 shows a simple arbitration circuit. The PUSH and POP inputs control a multiplexer that determines the operation in the next RAM cycle. If PUSH only

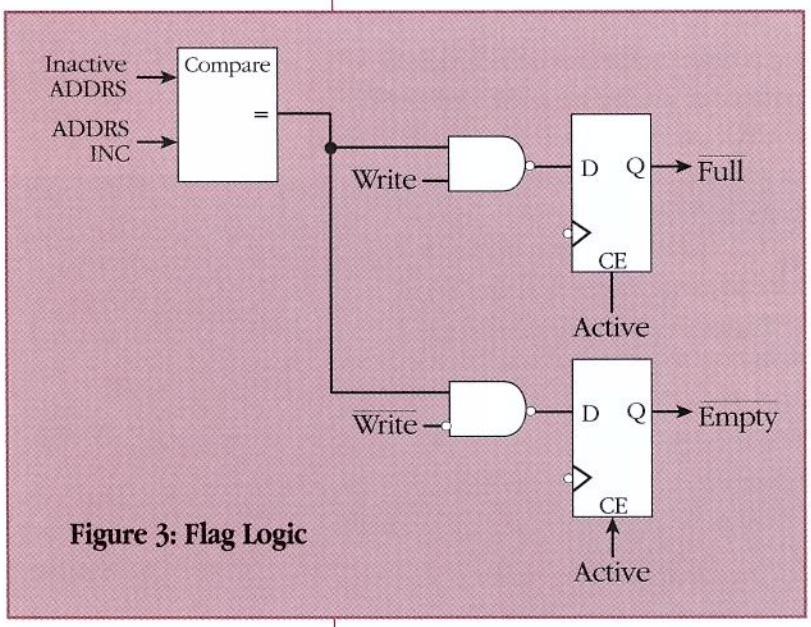


Figure 3: Flag Logic

is asserted, the next cycle is a write. If POP only is asserted, it is a read cycle. If both are asserted together, the next operation in the next RAM cycle is determined by a user-defined Priority signal. Several options for the Priority signal are discussed later.

If a PUSH or a POP is requested and the FIFO is not full or empty, respectively, the next cycle is declared active. A write or a read occurs and the corresponding address is incremented. Otherwise, the cycle is inactive; no read or write occurs and the addresses remain unchanged. In an inactive cycle, the Write signal is deasserted by default.

Two handshake signals are generated. ACK acknowledges that a PUSH request will be honored in the next RAM cycle. Input data is captured on the falling clock edge that starts the RAM cycle. RDY indicates that a POP request will be honored during the next RAM cycle. Output data is made available on the falling clock edge that ends the RAM cycle.

In deciding the next operation when both PUSH and POP are asserted, the most straightforward Priority functions simply default to one operation or the other. To write every time, a logic High could be used. To read every time, a logic Low could be used. In practice, however, this can lead to wasted cycles. For example, PUSH could win when the FIFO is full and the operation cannot be performed. A better choice is to use FULL as Priority to select write every time unless the FIFO is full. Similarly, using EMPTY will cause POP to win every time unless the FIFO is empty.

The above priorities are useful when receiving data from a burst source, such as a bus, or when transmitting burst data. While a burst is in progress, however, the other operation can be locked out for many cycles. If a more even resource allocation is required, Write can be used as Priority. In this case, requesting PUSH and POP results in alternating reads and writes.

While the time to acquire the FIFO is reduced to no more than one cycle, the guaranteed peak PUSH/ POP rate is also reduced. In the limit, PUSH and POP may only operate at half the RAM cycle rate. The average data throughput is unaffected, however. In the long term, it is

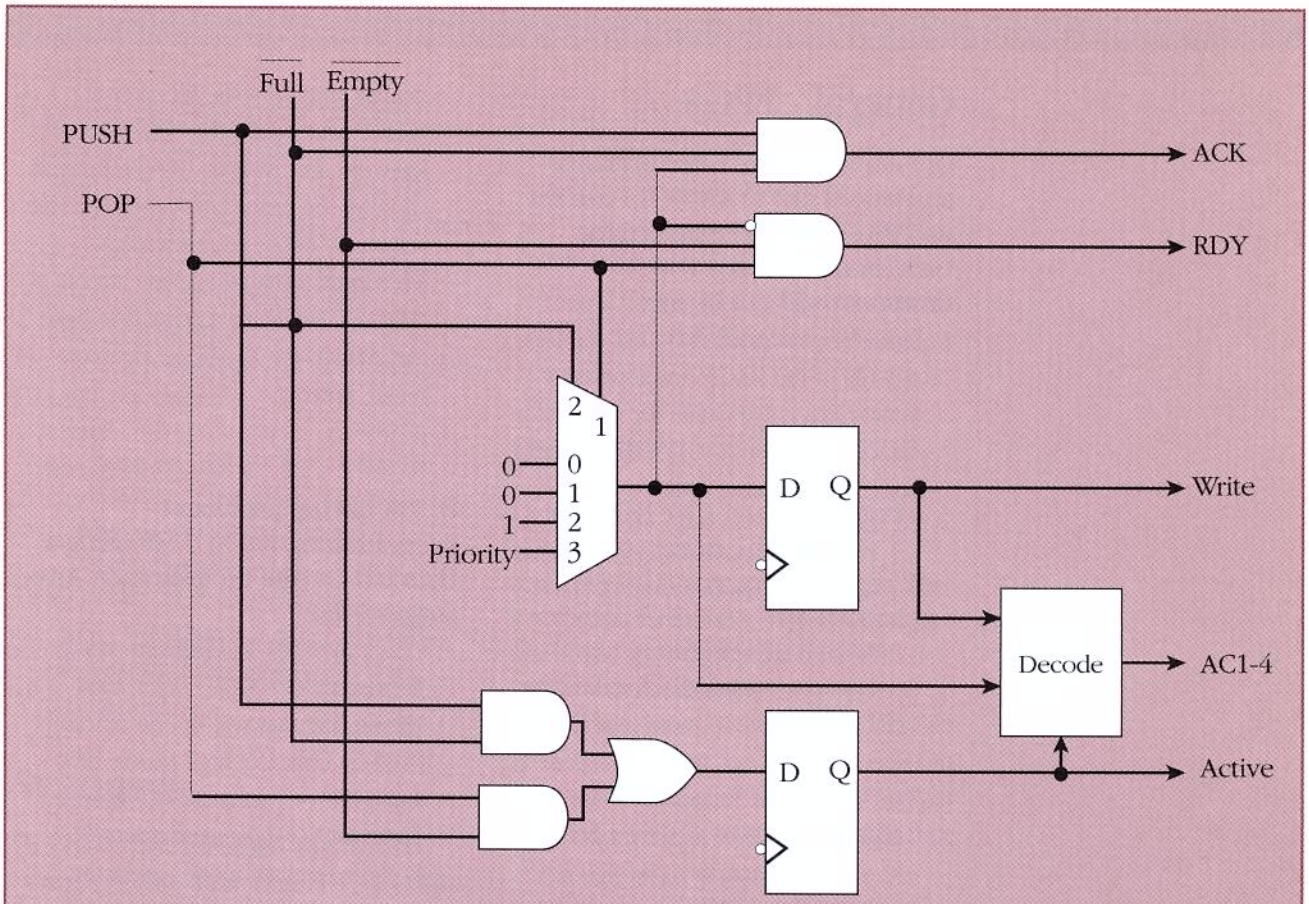


Figure 4: PUSH/POP Arbitration Logic

obvious that no more than half the RAM cycles can be PUSHes. Attempting to achieve more will fail when the FIFO becomes full. Similarly, no more than half the cycles can be POPs, since the FIFO will become empty.

A third option permits both burst reads and burst writes, although either PUSH or POP may experience a long delay acquiring the FIFO if it is busy. Priority is connected to Write. As a result, the FIFO repeats its last operation whenever there is a conflict. A burst read or write will continue, and lock out the other operation until the burst is complete.

Arbitration permits any RAM cycle to be a PUSH or a POP. XC4000 RAM performance is improved through read-modify-write operation, and the fastest clock required is at the RAM-cycle rate. The design is expandable to any size FIFO. The estimated maximum clock frequency for a 16 x 8 FIFO buffer is 30 MHz in an XC4005-5 device.

Design variations can increase the speed of small FIFO buffers to 40 MHz *(see page 8-142 of the 1994 Data Book).* ◆

General - FPGA

Q: I am using XACT-Performance and would like to know if I can set up PPR so that I can determine early in my PPR run which timespecs will not be met.

A: Inside of your XACTINIT.DAT file (see p 3-149 of the XACT Development System Reference Guide for more information about the XACTINIT.DAT file), insert the following options:

```
pa_show_details=true
pa_pins_to_show=<some number
  of worst case endpoints>
pa_paths_to_show=<some
  number of paths>
```

For example, assume that you wish to halt PPR after you have more than five timespecs that will not meet your specified timing. The options to include in the XACTINIT.DAT file are as shown below.

```
pa_show_details=true
pa_pins_to_show=5
pa_paths_to_show=5
```

When you see the failing paths show up on the screen output, you can suspend PPR with either Ctrl-Break (DOS) or Ctrl-C (UNIX). Please be aware that these are preliminary estimates at this point, utilizing only partitioning information, and do not reflect actual delays.

In addition, if you wish to get a complete report of which timespecs were not met after the design is completely routed, add the following to the XACTINIT.DAT. Of course, you must allow PPR to complete entirely.

```
/ppr/report_paths=true
```

General - EPLD

Q: How do I use the master reset (MR) pin as an input pin on the XC7336 and XC7354 devices?

A: DS550 version 5.0 is required to use this feature. In a behavioral design, include the keyword MRINPUT in the header section of the file after the "CHIP" and before the "EQUATION" keyword. For designs using schematic capture, the procedure depends in the schematic editor you are using:

Viewlogic - Simply add the attribute "MRINPUT=ON" to a schematic page.

OrCAD - Using the Place Text command, enter:

```
global
mrinput=on
```

Q: I'm having problems programming my XC7236 using a Data I/O Unisite Programmer. Any suggestions?

A: Check the Data I/O software version. If the version is UNISITE V4.4, there is a known bug that will not be officially fixed by Data I/O until March 1994 when the v4.5 software is released.

There are a couple work-arounds:

1) From terminal mode, select the devices using one of the following family pin-out codes: XC7236-ILCC 18F/168 or XC7236-PLCC 18F/168.

2) If a more permanent solution is needed, a self-extracting file called U44SEL.EXE may be downloaded from the Data I/O bulletin board service (Tel: 206-882-3211).

Mentor Graphics

Q: When using Mentor Graphics Design Architect, occasionally the lca_technology parameter , used to evaluate models for different symbols, will be lost. The following error messages may occur:

```
warning: unable to evaluate
  property model on the
  instance
unable to resolve expression
  symbol lca_technology
warning: unable to evaluate
  property _qp_prim on the
  instance
bad triplet case control
  expression
```

A: Despite the warnings, the problem is harmless. Users should be able to continue with no problems. To reset the parameter and to eliminate the warnings, type the following while in Design Architect (for the XC3000 family):

```
$set_parameter
   ("lca_technology","xc3000","string");
```

Or using the menus:

```
check
parameter set:
 property name:lca_technology
   property_value:xc3000
   type:string
```

Then, re-execute a check sheet.

(Note: Substitute xc2000 or xc4000 as the property_value when using those device families.)

Synopsys

Q: I have just installed the Xilinx-Synopsys Interface DS401 v3.01. The following error message occurs when I try to compile a simple VHDL (or Verilog) source file targeted to the XC4000 family:

```
Error: The entity
   'entity_name' depends on
   the package
   'std_logic_1164' which
has been analyzed more
   recently.
Please re-analyze the source
   file for 'entity_name' and
   try again.
(LBR-28)
```

A: The Xilinx X-BLOX DesignWare library shipped with DS401 v3.01 was created with Synopsys software release v3.0b (Design Compiler or FPGA Compiler). Consequently, if you are using a Synopsys release after v3.0b (including v3.0b-12954 and v3.0c), then you will encounter the above message whenever you attempt to compile a XC4000 design that utilizes the X-BLOX DesignWare library. Note, this error message will only occur if the design uses the X-BLOX DesignWare library.

Xilinx has since re-analyzed the X-BLOX source files with Synopsys v3.0b-12954 and v3.0c. Please contact Xilinx Technical Support for the updated library.

OrCAD

Q: SDT2XNF v4.2 has been known to generate errors, including unexpected interrupt messages, for a variety of reasons. The following are some guidelines all OrCAD users should follow:

A: 1. Output nets of OBUFTs and TBUFs must be labeled.

2. All busses and bus nets must be labeled, especially if the busses pass through levels of hierarchy.

3. Schematic sheet filenames must have the .SCH extension.

4. If the design is very large and contains hierarchy, run XMAKE to tranlsate the design. XMAKE will run SDT2XNF with the -x option, which will translate the schematic in smaller stages, therefore using less memory.

Viewlogic

Q: I recently purchased the Viewsynthesis package from Xilinx. I cannot find the VHDL Analyzer portion of the software.

A: The VHDL Analyzer was not shipped with the package. You can download the file from the Xilinx Technical Bulletin Board. The filename is VHDLANAL.ZIP. See section 6 of the Programmable Logic Data Book to learn how to use the Xilinx Technical Bulletin Board. ♦

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To: Brad Fawcett, *XCELL* Editor **Xilinx Inc. FAX**: 408-879-4676

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