XCELL

Issue 26
Third Quarter 1997

THE QUARTERLY JOURNAL FOR XILINX PROGRAMMABLE LOGIC USERS

XILINX®

The Programmable Logic Company℠

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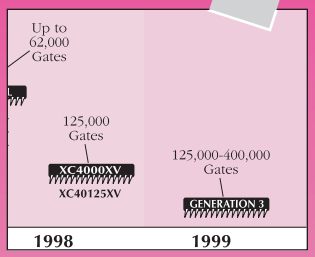

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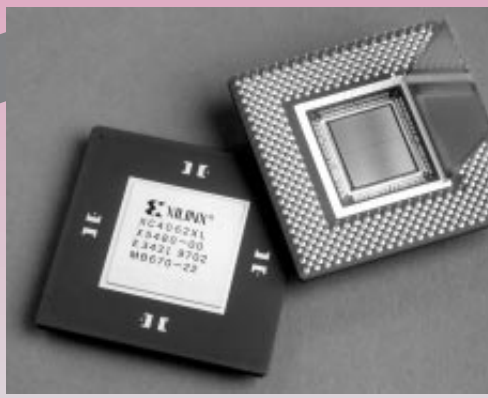

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What Would You Like to See in *XCell*?

XCell reaches well over 30,000 readers worldwide. Our surveys show that most of you read *XCell* regularly, and keep it for reference, because it provides a wealth of useful and timely information. We are now asking you to help us improve *XCell* and make it an even more meaningful and useful publication.

> *"We are now asking you to help us improve* XCell *and make it an even more meaningful and useful publication."*

In future editions, we intend to provide more "how-to" information, including articles submitted by our technology partners showing you how to use their products to develop Xilinx designs. We intend to keep you informed of the fast changing trends and technology advances in our industry, so you can be prepared. We intend to provide reviews, highlighting the latest products, literature, and services available both from Xilinx and from our technology partners. And, we intend to show you how your peers are meeting their specific design challenges.

To accomplish this, we need your help. For example, what kinds of articles would you like to see more of, or less of? Do you use the reference information printed in the back, such as the component availability chart, or do you visit WebLINX for the latest updates? What sections do you read most, and least? What can we provide that will make a positive difference and help you do your job better? Are you interested in submitting articles of your own, describing how you solved a common problem or achieved a unique solution? This is your opportunity to influence the future of *XCell*.

Please E-mail your comments and suggestions to editor@xilinx.com.

With your help, we will continue to provide you with the best possible support.

Note: Bradly Fawcett, the editor of *XCell* since 1993 (*XCell* #10), has left Xilinx to pursue even greater challenges. His contribution to Xilinx has been exemplary and we wish him well. Great job, Brad! ◆

Xilinx Adds Building to HQ Facility

Due to our continuing success, we are expanding. Ground breaking is now underway for a new building on our San Jose campus. This new, two-story, 180,000 sq. ft. building on 9.8 acres, will house up to 700 people. This environmentally conscious, open-floor-plan, high-tech building will house the Xilinx Corporate staff, Sales, Marketing, Accounting, and Human Resources departments, among others. Construction is expected to be complete by August 1998. ◆

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CPLDs Provide Needed Design Flexibility in Vision Systems

At the world's top machine vision company, **Cognex**, designers of the new Checkpoint 900C have taken full advantage of the proven pin-locking capabilities and in-system programmability (ISP) of the XC9500 family. This new line of machine vision and pattern recognition products greatly accelerates image analysis for color vision applications running on high-speed production lines.

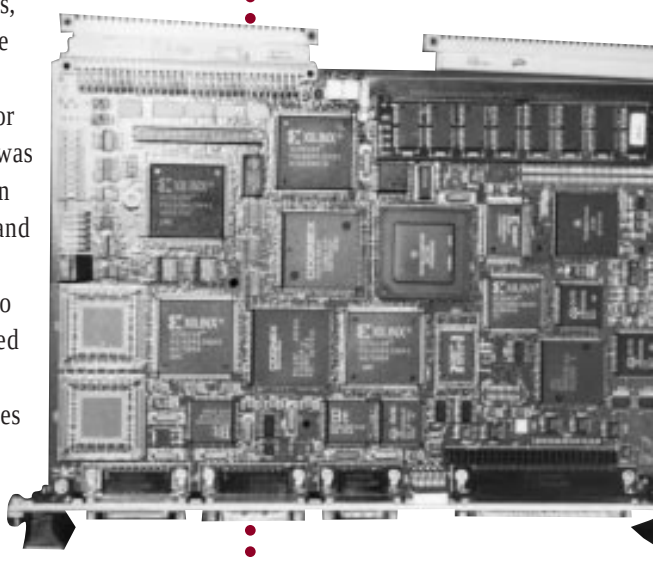
Based in Natick, Massachusetts, Cognex has been using Xilinx XC9500 devices since early 1996 in a multitude of new designs. It began shipments of this new system in June 1997.

"XC9500 components are key to the Checkpoint 900C, Cognex's first color vision processor. Xilinx's flexible pin-locking architecture, high-speed CPLD specs, and in-system programming capability have been instrumental in the development of our latest Checkpoint product. Changes to the design have been quick to implement — the re-programmability through the JTAG port has allowed quick transition from prototypes to production," noted Cognex's Steven Goodspeed.

Cognex has focused on keeping pace with ever faster production lines, resulting in improved productivity, higher quality, and reduced costs for manufacturers. The robust performance and re-programmability of its systems have fueled its worldwide popularity.

As the first full-scale color machine vision system designed for the PC, the Checkpoint 900C is capable of a wide range of challenging machine vision applications in a number of major industries. For example, the Checkpoint 900C system can be used in the pharmaceutical industry to inspect blister packs and sort color tablets and capsules; in the automotive industry to verify that color fuses have been inserted in the correct position in fuse blocks; and in the electronics industry to ensure that LEDs, cellular phone keys, and pager buttons are the correct color.

Cognex's Checkpoint 900C color system.



"The primary reason for selecting ISP technology was that this part of our design was extremely complex, and large functional blocks could be incorporated into single devices," Goodspeed said. "During the debug process, hardware changes could be contained and fixed within a single Xilinx XC9500 device, then quickly evaluated by reloading the device through the ISP JTAG connection. No messy rework and component replacements were required."

System components include an embedded 68060 processor, a PCI interface, vision processing ASICs, CPLDs, and FPGAs. The CPLDs implement the major control logic, including the SDRAM controller and IO controller.

"Pin-locking and ISP have been key to upgrade flexibility of the Checkpoint 900C system. New product functionality can be downloaded using the JTAG port," said Goodspeed. "Not having to remove a component eliminates any need for sockets and extra handling of the hardware if rework is ever required."

The XC9500 family is a proven winner, especially in those applications that take advantage of the rock-solid pin-locking and ISP capability for design re-programmability. ◆

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New Product Literature

Learn about the newest Xilinx products and services through our extensive library of product literature. The most recent pieces are listed below. To order or to obtain a complete list of all available literature, please contact your local Xilinx sales representative. ◆

TITLE	DESCRIPTION	NUMBER
Xilinx Packaging Guide	Technical Data	#100120
CPLD Pin-Locking Quick Reference Guide	Technical Data	#500855
Xilinx Education/Training Brochure	Features & Benefits	#0010134-07
Product Overview Brochure	Features & Benefits	#0010130-06

UPCOMING EVENTS

Look for Xilinx technical papers and product exhibits at these upcoming industry forums. For information about any of these conferences, please contact Kathleen Pizzo:
Tel: 408-879-5377
FAX: 408-879-4676.
◆

DSP World Expo / ICSPAT '97
September 15-17
San Diego, CA

DSP France
September 17-19
Paris, France

DSP Germany
September 30-October 1
Munich, Germany

PCI France
October 1-2
Paris, France

High-level Electronic System Design Conference and Exhibition (HESDC '97)
October 7-9
San Jose, CA
Keynote address by Richard Sevcik, Senior Vice President, Software at Xilinx

IP '97
October 20-21
Bracknell, United Kingdom

Telecom & Industrial PCI Conference (TIPCIC '97)
October 21-23
Framingham, MA.

Xilinx Inc. stock is traded on the NASDAQ exchange under the symbol XLNX.

FINANCIAL RESULTS

New Products Lead 3Q97 Growth

Revenues for the fiscal quarter ending June 28, 1997 totaled $160.8 million, up 6% from $151.8 million in the fourth quarter of the prior fiscal year, and up 7% from $150.2 million in the first quarter of fiscal 1997. Net income was $33.4 million, up 10% from the preceding quarter, and up 3% from the first quarter of the last fiscal year. Gross margin rose to just over 62%, while operating expenses as a percentage of revenues decreased relative to the preceding quarter.

"I continue to be pleased by the revenue contributions of our new products which constituted nearly $7 million this quarter," remarked Wim Roelandts, Xilinx chief executive officer. "The XC9500 family of in-system programmable (ISP) CPLDs doubled in revenue this quarter, and the high-density, high-speed XC4000XL family is currently the fastest ramping FPGA in the industry's history. On the software side, we shipped approximately 1,700 revenue seats this quarter, and our new Alliance Series version M1 software continues to be well received in the marketplace."

First quarter North American sales to major end markets were as follows: communications, 37%; data processing, 29%; and industrial, 15%. In addition, Xilinx continued to realize strong revenues from networking companies, which represented an all-time high 15% of North American revenues. Geographically, revenues from North America, Europe, and Asia/Pacific were up sequentially, while revenues from Japan declined. ◆

New CORE Solutions Data Book Available

The new data book focused on programmable logic cores and related products provides one definitive source and detailed product descriptions. Xilinx CORE Solutions improve both time-to-market and device utilization. They include:

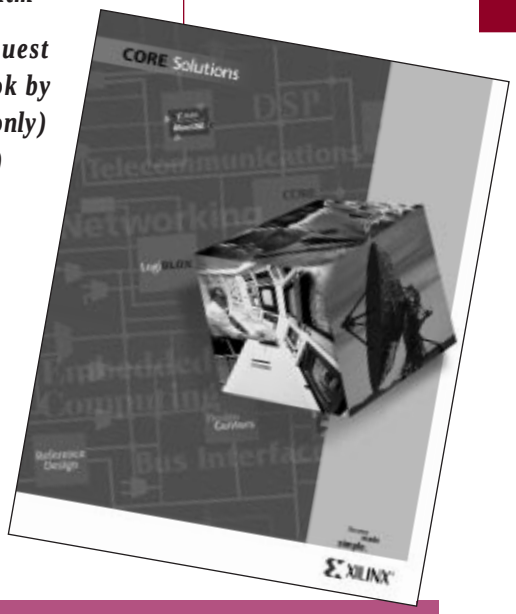
- **LogiCORE™ products** - PCI, DSP, and the CORE generators.
- **AllianceCORE™ products** - Complete solutions for PCMCIA, USB, and Reed-Solomon, plus eight other cores and development tools from third-party partners.
- **LogiBLOX™** - Parameterized small building blocks.
- **Reference Designs** - A listing of all application notes on WebLINX accompanied by design files.

Pages 5 and 6 in section 1 list all of the functions described in the catalog by application segment, and are your best guide to locating a specific product that is available *today*. If you don't see what you need, check the *Areas of Expertise* in the profiles of our AllianceCORE partners, starting on page 3-75. Our partners are happy to discuss the possibility of making a core for your specific needs.

The entire catalog can be downloaded from WebLINX at: http://www.xilinx.com/products/logicore/core_sol.htm

To order a hard copy, request the CORE Solutions Data Book by calling 1-800-231-3386 (U.S. only) or 408-879-5017 (worldwide) or e-mailing your request to literature@xilinx.com. ◆

NOTE: *New products and updates, made since the last publish date, can be found on WebLINX at http://www.xilinx.com/products/logicore/logicore.htm*



TECHNICAL TRAINING UPDATE

Training Now Available Worldwide

The new *Alliance Software version M1 Tools Course* and the *Alliance Software version M1 Update Course* are now being offered on a regularly scheduled basis worldwide.

The *Alliance M1 Tools Course*, for new users, is two-and-a-half days long. The *Alliance Software version M1 Update Course*, for existing users, is one day long.

The dates for these courses, held at the Xilinx San Jose facility, are:

Alliance Software version M1 Tools:
- August 5, 18
- September 9, 15
- October 13, 27
- November 3, 17
- December 1, 17

Alliance Software version M1 Update:
- August 1, 25
- September 5, 22
- October 6, 20

Xilinx distributors worldwide offer these same courses at regional or local sites. For dates and locations, check with your distributor, see the Xilinx Educational Services brochure, or visit the training section under "support" at WebLINX (www.xilinx.com).

The 1997 brochure was updated at the end of July. It describes the contents of each training course and the latest dates (at time of publication) of scheduled training courses.

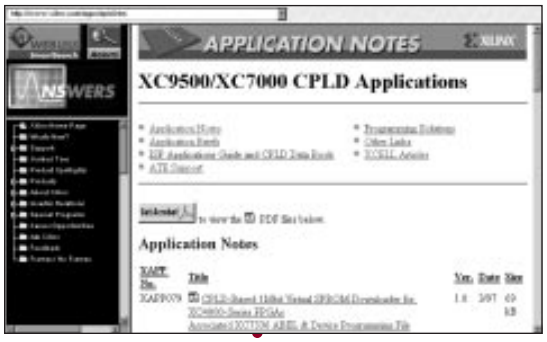
The customer education group will continue to develop new training courses to address future Xilinx software releases and the needs of ourcustomers. ◆

Information regarding training can always be obtained by calling the registrar at 408-879-5090 or via e-mail at customer.training@xilinx.com.

New XC9536 ISP CPLD Demo Board

Designers may use the new XC9536 in-system-programming (ISP) demo board to prototype, debug, and troubleshoot small designs. When used with the new Foundation Series or Alliance Series software, the board demonstrates the benefits of combining a robust pin-locking architecture with ISP.

The board includes an XC9536-VQ44 CPLD, 555 surface-mount oscillator, eight surface-mount LEDs, a JTAG interface, and a sea-of-holes prototyping area.



Find it on the Web at: www.xilinx.com/apps/epld.htm

The eight surface mount LEDs are connected to the right side of U1, the XC9536 CPLD, as shown in **Figure 1**. A sample design for a Johnson shift counter is included, producing a shifting LED pattern.

As a test of the XC9500 family pin-locking capability, the design of the Johnson shift counter can be easily modified to generate a different LED pattern (counting up instead of down, for example). Once the new design has been processed, you can immediately reprogram the demo board to test the change. This quickly shows that the pinouts can remain locked, even after making design changes.

We have an application note to support the demo board as well. It includes a description of operation, a schematic, VHDL and ABEL demo files, and stock numbers for all components. It is available now by visiting WebLINX (www.xilinx.com/apps/epld.htm). You can select application note number XAPP078, the XC9536 ISP Demo Board, and the associated VHDL or ABEL Johnson shift counter demo files. To process the ABEL demo file, use the Xilinx Foundation Series software. To process the VHDL file, use the Alliance Series software.

Programming the demo board can be accomplished using either the Xilinx EZTag software, or the new JTAG programmer software contained in the Foundation or Alliance Series Software.

You can order the demo board, part number HW-CPLD-DEMOBD, by contacting your local Xilinx Distributor. ◆

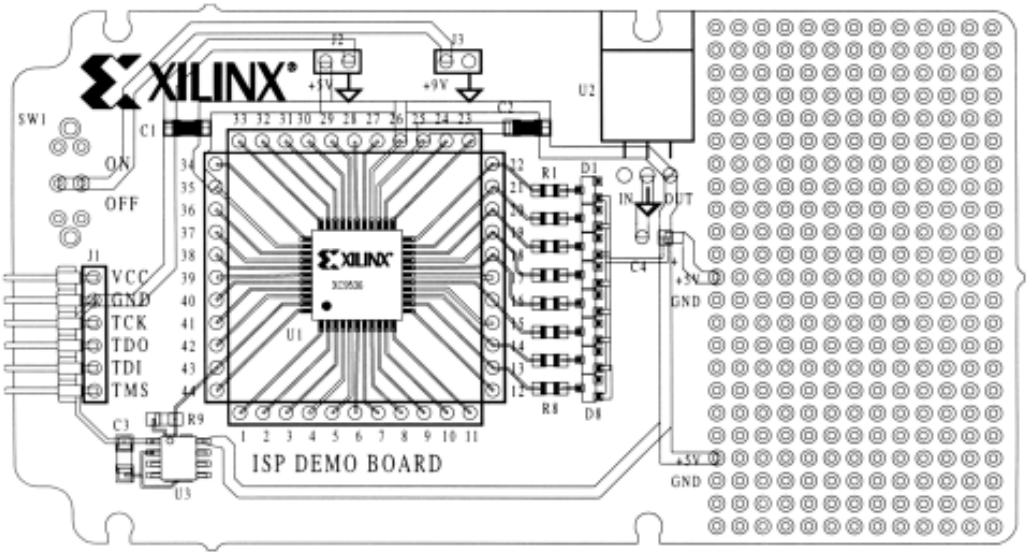


Figure 1: *ISP Demo Board*

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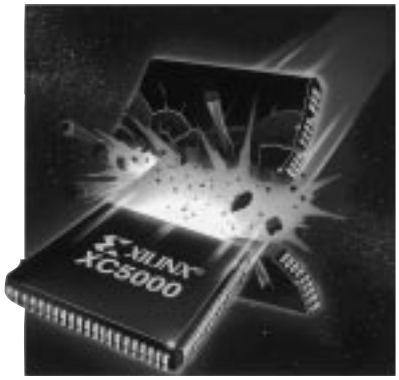
The XC5200 Series

The Lowest-Cost FPGAs Anywhere

The XC5200 family is now shipping into new, high-volume applications such as CD players, PC add-in cards, set-top boxes and personal communications devices. Because of cost sensitivity, many of these applications have relied on gate arrays in the past. Success in these markets has rocketed sales of the XC5200 family to a million units, in record time—twice as fast as any previous device.

According to Masato Yorifuji, senior engineer for Hitachi, Ltd., Japan, "… . while designing the world's first MPEG camera for digital photography, we needed the advantages of re-programmability to deliver leading edge products to the market. Although we historically considered only a mask-programmed solution for our product, the Xilinx XC5200 family delivered a compatible cost-per-logic-cell and reduced our time-to-production by six months."

Matrox Graphics, a Montreal-based company whose sales of PC graphics add-in cards have more than doubled each of the last three years, has selected the Xilinx XC5204 device for the high-volume Rainbow Runner daughtercard, used on the Matrox Millenium. The XC5204 was chosen for this consumer application because of its low cost, high I/O count and reprogrammability. Plus, further design changes are possible simply by providing a new software driver because the XC5204 configuration data is part of the driver. This allows the board to change not only software, but also hardware, to adapt to the latest 3D and video applications. Configuring from the driver also eliminates the need for a serial PROM, further optimizing board space.



The XC5200 family has succeeded in replacing low density gate arrays where other PLD vendors have failed because it leverages leading-edge process technology with specific architectural innovations that minimize die area and cost.

Ask your local Xilinx sales representative for more information. ◆

XC9500 Family Price Reductions

Effective September 1, the prices for the XC9500 CPLD family have been reduced up to 30%, depending on speed and package. The price reductions result from improvements in wafer yields and manufacturing efficiencies, along with dramatic increases in production volumes.

Now it is easier for designers to take advantage of the most advanced CPLD technology available. For example, price is no longer a barrier to using in-system programmability (ISP) because the ISP-–capable XC9500 family is now the same price or lower than other non-ISP devices.◆

For specific pricing information, contact your local Xilinx sales representative.

XC9500 Family Price Reductions (in 100+ units)

Device	Old Price	New Price	% Reduction
XC9536-15VQ44C	$3.95	$3.05	23%
XC9572-15PC44C	$5.70	$3.20	44%
XC95108-20PC84C	$15.30	$8.05	47%
XC95216-20PQ160C	$48.50	$23.65	51%

Hi-Rel Product Roadmap Provides High-Density Leadership

Even as defense spending continues to decrease, the funds devoted to electronics for "smart" weapons and defense systems are expected to grow. Designers in the Hi-Rel/Military applications market are spending wisely, focusing on development time and time-to-market in a highly competitive industry, and using the latest technologies.

Xilinx has created a high-density FPGA roadmap that, in conjunction with QML certification, makes Xilinx FPGAs the technology of choice for defense system designers.

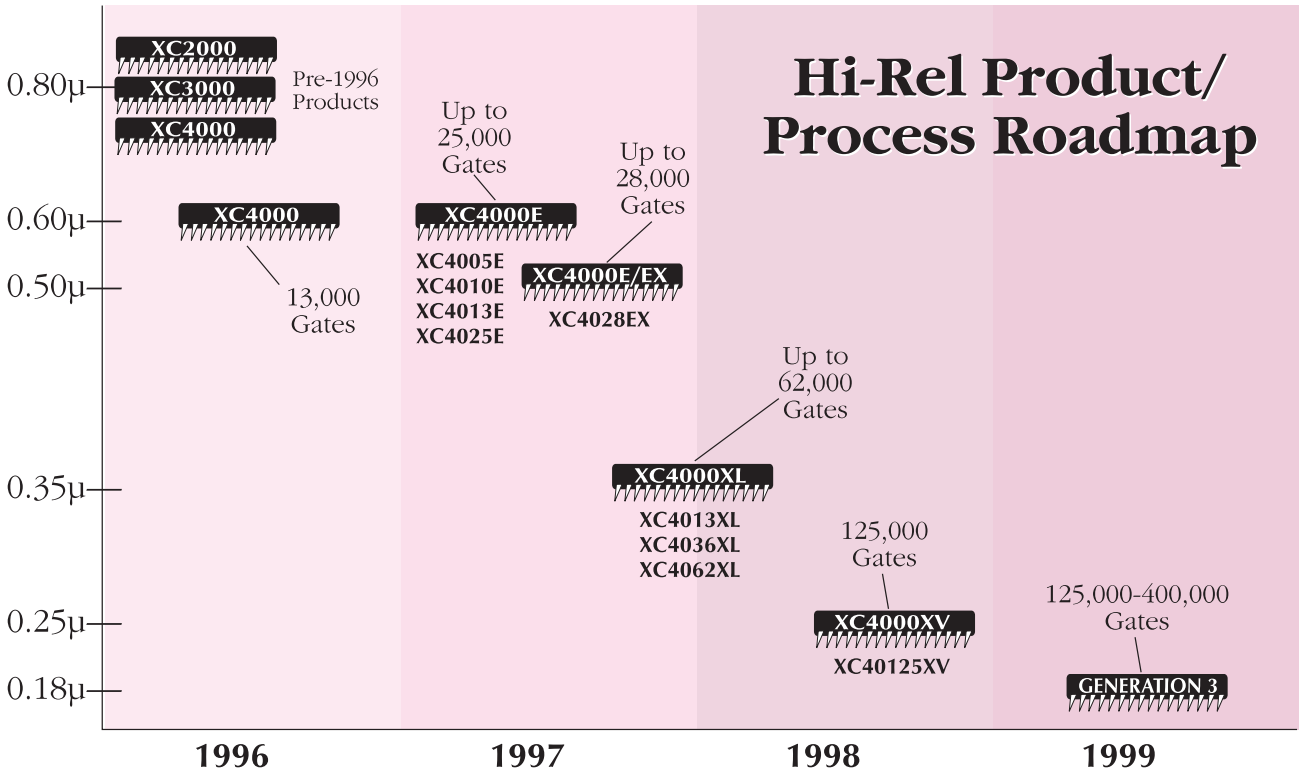
As it becomes more and more difficult to obtain Hi-Rel ASICs, high-density FPGAs will become the standard for Hi-Rel logic design. This will be accomplished by focusing on selected products and offering both through-hole and surface mount packaging options.

Xilinx is already shipping the industry's largest QML-compliant FPGA — the 25,000-gate XC4025E device.

With the trend towards lower supply voltages, the 3.3 volt XC4000XL family is destined to become the flagship of the Xilinx Hi-Rel product lines. The 62,000-gate XC4062XL FPGA will be available as a QML product in the first half of 1998.

Out strong product leadership will be further enhanced with the 2.5 volt, 125,000-gate XC40125XV device before the end of 1998, followed by a third generation family that will provide up to 400,000 gates of QML programmable logic in 1999.

Because FPGAs solve many of the problems facing the defense electronics industry, they have been successfully designed into hundreds of military and aerospace applications, such as electronic warfare, countermeasures, missile guidance, radar, sonar, communications and avionics systems. ◆



Xilinx DSP LogiCORE Advantages

The Xilinx CORE Generator, in conjunction with the XC4000XL segmented architecture, automatically produces highly efficient DSP designs that are predictable for any size device. Xilinx is the only FPGA supplier that can achieve this.

In the past, high-level VHDL designs (originally intended for gate arrays) could be used in FPGAs, but they produced inefficient, slow, and unpredictable results. Now, using the DSP LogiCOREs that are created from your design specifications, you can get performance and density that is equivalent to hand crafted designs.

In addition to logic design, the CORE Generator also produces a physical layout for each parameterized core, containing relative placement information for each CLB. Once the CLBs are mapped and placed relative to each other, multiple cores can be dropped into a Xilinx FPGA and still meet the predefined performance specifications of each individual core. This is made possible by our unique segmented routing architecture.

Xilinx is the only FPGA manufacturer that produces a physical layout in parallel with the core logic design. Our competition uses cores that must rely on the place and route software to build the physical design each time they are used. And, their non-segmented routing architecture means you cannot predict performance, which decreases as more logic is added to a device and varies between different software runs, as shown in **Figure 1.**

The Xilinx core performance is also independent of device size. For example, a 12x12 parallel multiplier achieves the same maximum clock rate when it's used in an XC4005XL as when it's used in an XC4085XL. Our competitor's non-segmented architecture cannot achieve this because their metal interconnections get longer as the device size increases, as illustrated in **Figure 2**. Because of this, our competitor's core performance cannot be specified or controlled during the design phase; you must wait until the design is completed to determine if your system requirements were met. The Xilinx segmented routing does not have this problem and therefore timing is always predictable, as illustrated in **Figure 3.**

Xilinx CORE Solutions and the new CORE Generator, provide predictable, consistent, high-performance designs that get your product to market in the least time with the least effort. See our *CORE Solutions Data Book* for more information. ◆

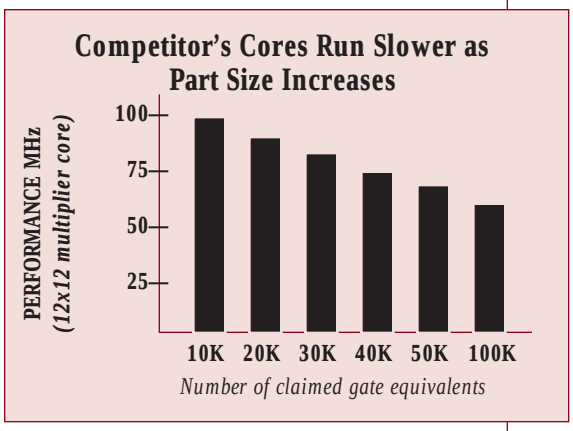


Figure 1: *Our competitor's FPGAs exhibit performance degradation as the device size grows, due to the increased capacitance of long non-segmented interconnections.*

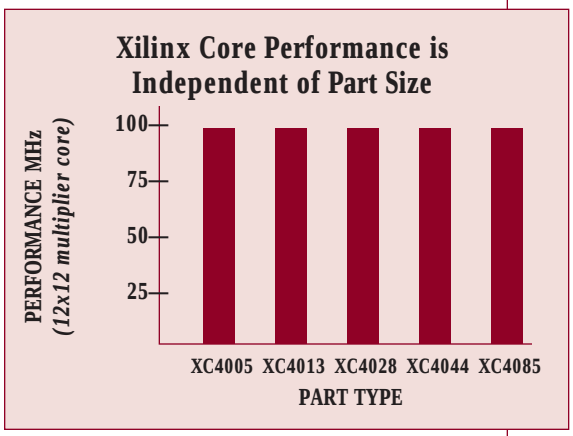


Figure 2: *The Xilinx segmented routing guarantees consistent performance as more logic is added.*

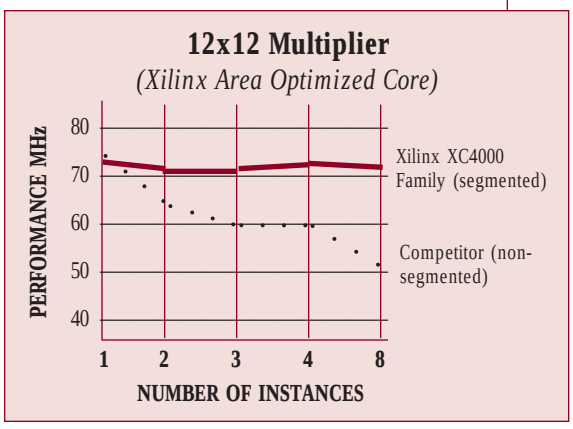


Figure 3: *Segmented routing and the Xilinx CORE Generator guarantee consistent performance between small and large FPGAs*

"A Leap Forward"

Signaal Evaluates the Xilinx Alliance Series Software Tools

Hollandse Signaalapparaten B.V. (Signaal), a subsidiary of Thomson-CSF, recently performed an evaluation of the new Alliance Series software. The design was for an interface between an MC68360 CPU and a SHARC bus running at a clock frequency of 25 MHz, and was implemented in an XC4010E-4PQ208 FPGA. About 70% of the CLBs and 80% of the IOBs were used. All I/O pins were locked to enable concurrent design of the PCB layout.

The evaluation used the Synopsys FPGA Compiler for synthesis, and the Cadence Leapfrog simulator for behavioral (RTL), functional, and timing simulation. However, any synthesis tool and VITAL-compliant simulator could have been used because all interfaces are based on standard formats such as VHDL, SDF, and EDIF. *See "design flow" at right.*

The Customer Evaluation Report

Jaap Mol of Signaal wrote, "The new Alliance Series software is a leap forward; improvements have been made in all areas." His report included many other key insights:

Usability of the Software

"The usability has been improved by the new GUI. It is intuitive and allows for better control, which is especially important for the first time user of the tools."

Controllability of the Tools

"The controllability has been improved using the flow engine and user-definable templates. Design constraints can be specified during synthesis (netlist constraints) and during place and route (user and physical constraints). Constraint-driven place and route is essential for timing-critical, high-density designs."

New JTAGProgrammer Software for ISP

The new JTAGProgrammer tool represents a major step forward in the evolution of in-system programming (ISP) download and test software.

Using the new JTAGProgrammer graphical user interface, designers have immediate access to all of the ISP functionality provided by XC9500 CPLD 1149.1-compliant devices. The structure of the boundary-scan chain is readily visible and the status of each part in the chain is clearly indicated on the topology diagram.

The JTAGProgrammer user interface is identical in its look and feel across all platforms (Sun, HP, PC). The same GUI can be used to download either via the parallel download cable (JTAG) or serial download cable (XChecker) as well as being used to generate serial vector format (SVF) files for easy interfacing to embedded processors, automatic test equipment, or third-party tools.

As with EZTag, JTAGProgrammer provides a simple-to-use interface that shields the end user from the intricacies of the boundary-scan protocol. JTAGProgrammer, however, adds more flexibility including the support of additional programming options like:

Version and Revision Control

"Version and revision control capability have proven to be very useful in performing design trade-offs. The best possible solution for the design can be selected from implemented versions and revisions. This is especially useful when using Xilinx FPGA technology to do rapid prototyping of a system. The Design Manager offers the capability for doing version and revision control on designs. In the Design Manager a design is referred to as a project. If there have been changes to a logic design (e.g. the netlist), this is referred to as a new version of the design. If the design is mapped into another device, package, or speed-grade, this can be referred to as a new revision. This way, the user can easily make trade-offs, without losing previous results."

Report Browsing

"During implementation of the design, many reports are generated. For instance, there are reports concerning timing, place and route, and pad assignments."

On-Line Help

"The on-line help is available from within the design manager. The help function is based on Windows Hyperhelp, has a search function, and is easy-to-use."

The Signaal Design Flow:

- A VHDL (RTL) model was verified using the VHDL simulator. This model also functioned as an input for logic synthesis.
- The synthesis tool translated the VHDL model to gates. (The required synthesis libraries are provided by Xilinx or the synthesis tool vendor.)
- An EDIF netlist was generated during synthesis, containing the connectivity between Xilinx primitives. This netlist was later transferred to the place and route software.
- Optionally, functional (pre-layout) simulation could be performed using the Xilinx VITAL library, to verify the correctness of the synthesis process before proceeding with place and route.
- The EDIF netlist was processed by the place and route software. After place and route was completed, a VHDL netlist and SDF timing information were generated. These were used for Timing Simulation, once again making use of the Xilinx VITAL library. In addition, static timing analysis was performed during synthesis and during place and route.

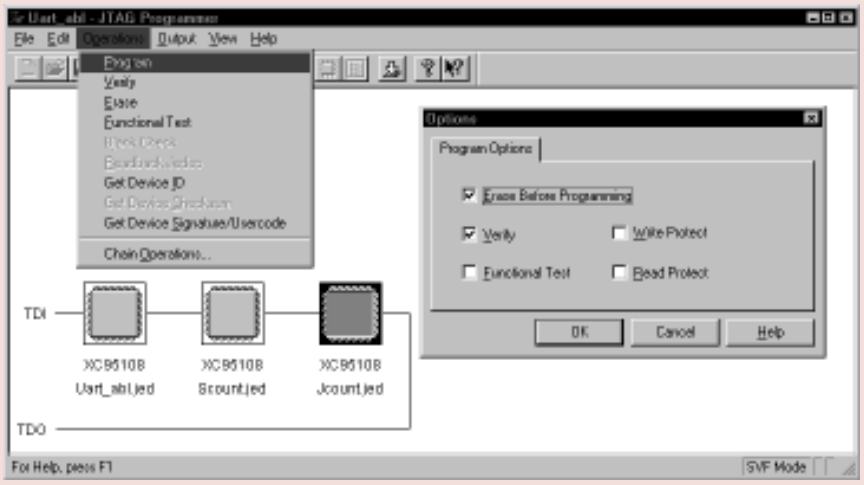
Interface Formats to Other Tools

"The interface to and from Xilinx tools is dramatically improved by the move to standard formats like EDIF, VHDL, and SDF. This was the major reason why the interfaces from the synthesizer and simulator did not cause any major problems. The availability of a

Continued on the following page

- Ability to skip erase before programming.
- Automatic detection of new XC9500 silicon features.
- Ability to override write protection.
- Automatic detection of programming characteristics of silicon.

JEDEC files generated from XACT*step* version 6.X software are 100% compatible with JTAGProgrammer so you can use your archived JEDEC files without modification in the new JTAGProgrammer environment.



JTAGProgrammer runs on SunOS 4.x (Solaris 1.X), SunOS 5.X (Solaris 5.X), HP UX 9.X and 10.X, Windows 95, and Windows NT 4.0. ◆

A Leap Forward

Continued from the previous page

VITAL-compliant VHDL library makes it possible to use one testbench, one simulator, and one language for simulation on any level of abstraction.

"Apart from the tools, which are called from the flow engine, the following functions are also available:

- "The **timing analyzer** provides a timing analysis of specific paths in the design, and helps to verify that the timing constraints are met by the place and route tools.
- "The **epic design editor** can be used to manually place and route any or all parts of the design.
- "The **hardware debugger** provides an interface to the XChecker cable, which can be used for reconfiguring an FPGA, while prototyping the system.
- "The **PROM file formatter** generates one or more PROM files in a suitable format for an EPROM programmer. It can merge multiple bitstreams into the resulting PROM files. Both serial and byte-wide PROMs are supported.

"It is quite visible that Xilinx has put a lot of effort into the development of this release. The new tools are intuitive, have good controllability, and support industry standards. The support of industry standards makes the interface to third-party EDA vendors easy and seamless. The tools helped cut down our design time significantly, which translates into reduced time-to-market. We hope Xilinx will continue investing resources in this direction." ◆

New Alliance and Foundation CPLD Fitter Option

The new Alliance Series and Foundation Series software contain a CPLD fitter option called "use advanced fitting." This new feature allows the software to group equations that have the same input signals into the same function block. You would typically use this option on large designs that cannot fit because of function block input restrictions.

If your design is unable to fit into a particular device, take a look at the top of the report (.RPT) file. Designs which appear to have plenty of I/O pins, product terms, and macrocells when mapped into an XC9500 device may not fit because of the 36-signal input limit to each function block.

```
_*********Function Block Resource Summary*******
Func-    # of      FB
tion     Macro-    Inputs    Signals    Total     O/IO     IO
Block    cells     Used      Used       Pt Used   Req      Avail
FB1      10        36        36         35        8/0      10
FB2      14        36        40         66        4/0      14
FB3      12        36        37         87        9/0      9
FB4      12        36        36         76        8/0      10
FB5      11        34        34         45        5/0      13
FB6      9         36        36         34        5/0      13
```

Figure 1: *Function Block Resource Summary from Fitter Report.*

In the example in **Figure 1**, we see that almost all of the FB inputs are being used. However, the total number of product terms and macrocells in each function block are not fully utilized. This would be a perfect candidate for trying the "advanced fitting" algorithm.

What exactly does this new algorithm do differently? There are 36 inputs to a function block in the XC9500 CPLD architecture. The CPLD fitter software will default to fitting designs based on a pin-locking algorithm. This pin-locking algorithm tends to spread equations throughout the CPLD, ensuring room for growth and change for all of the equations.

This spreading function, however, tends to use up the number of function block inputs very quickly. By selecting the "advanced fitting" algorithm, the software weights common signal usage higher and tends to group equations with the same signals into the same function block. As a result, it provides a denser fit for larger designs by freeing the otherwise used inputs from other function blocks. ◆

TECHNICAL QUESTIONS & ANSWERS

Will I still be able to target XC3000/A and XC5200 devices with the Foundation Series software?

As long as the XACT*step* version 6 implementation software remains installed on your system (located in C:\XACT by default), and the XACT variable and path point to this location, you will still be able to target XC3000/A and XC5200 devices with the Foundation Series tools.

When you open an existing Foundation Series project, targeting an XC3000/A or XC5200 device, it will ask if you wish to enable the XACT*step* v6 flow. Once the XACTstep v6 flow is enabled, the Foundation Project Manager will revert back to the XACT*step* v6 menus, and will launch the XACT*step* v6 Design Manager instead of the Foundation Series Design Manager.

The project type can always be switched between the XACT*step* v6 and Foundation Series flows by selecting "file ➡ project type" from the Project Manager.

If the XACT*step* v6 flow is not listed as an available project type, and you wish to create a new project targeting either an XC3000/A or XC5200 device, add the following lines to the bottom of the SUSIE.INI file, located in the Windows directory:

```
[Flow_26] XILINX6=ON
```

If the desired libraries are no longer present, they must be copied from the Foundation 6.0.1 CD-ROM from the \ACTIVE\SYSLIB directory to C:\ACTIVE\SYSLIB (where C:\ACTIVE is the location of the Foundation Series Design Entry software), and manually added to the Foundation Series project by selecting "file ➡ project libraries" from the Project Manager, and adding the appropriate libraries.

Do I still need a hardware key with the Foundation Series software?

If you have either a Foundation Series STD-V or BAS-V package, you will need to have a Xilinx hardware security key attached to your PC's parallel port in order to enable the VHDL features of the product. Existing Foundation Series VHDL customers may use their existing key with the Foundation Series version M1.3 software. New Foundation Series VHDL customers will receive a pre-programmed hardware key with their new software.

How do I compile the Foundation Series HDL simulation libraries so I can perform timing or post-synthesis simulation in QuickHDL?

The Foundation Series version M1.3.7 includes Verilog and VHDL compile scripts that run the HDL-compilation commands automatically.

For more information, see the files:

```
$XILINX/mentor/data/verilog/README
$XILINX/mentor/data/vhdl/README
```


TECHNICAL SUPPORT RESOURCES

Need technical help right now? Here's where to start:

1. **Find us on the Internet at www.xilinx.com** — We update our **"Answers"** Web tool daily with the latest application notes, data sheets, patches, and solutions to your technical questions. Get immediate answers 24 hours per day!

If you don't have access to the Web or can't locate an answer via step #1, then...

2. **Contact your nearest Customer Support Hotline (see below)**

NORTH AMERICA

(Mon, Tues, Wed, Fri 6:30am-5pm, Thur 6:30am - 4:00pm Pacific Time)
Hotline: 800 255 7778
or 408 879 5199
Fax: 408 879 4442
BBS: 408 559 9327
Email: hotline@xilinx.com

UNITED KINGDOM

(Mon, Tues, Wed, Thur 9:00am-12:00pm, 1:00-5:30pm, Fri 9:00am-12:00pm, 1:00-3:30pm)
Hotline: (44) 1932 820821
Fax: (44) 1932 828522
Email: ukhelp@xilinx.com

FRANCE

(Monday-Friday 9:30am-12:30pm, 2:00-5:30pm)
Hotline: (33) 1 3463 0100
Fax: (33) 1 3463 0959
Email: frhelp@xilinx.com

GERMANY

(Mon, Tues, Wed, Thur 8:00am-12:00pm, 1:00-5:00pm, Fri 8:00am-12:00pm, 1:00pm-3:00pm)
Hotline: (49) 89 93088 130
Fax: (49) 89 93088 188
Email: dlhelp@xilinx.com

JAPAN

(Mon, Tues, Thur, Fri 9:00am-5:00pm, Wed 9:00am-4:00pm)
Hotline: (81) 3 3297 9163
FAX: (81) 3 3297 0067
Email: jhotline@xilinx.com

Need a software update, authorization code, or documentation update?

Contact Customer Service: U.S.: 800 624 4782 Europe: (44) 1932-349401 International: 408 559 7778

High Performance Design

XC4000XL-1 FPGAs Exceed 100MHz

In addition to being the world's highest density FPGAs, the Xilinx XC4000XL-1 family is also the world's fastest. They offer greater than 100 MHz internal system clocks and more than 70 MHz in I/O speed. This combination of speed and density comes with low power and total compatibility with 3.3 volt or 5.0 volt logic.

The increase in speed can be quite substantial. Designs for the XC4000E-3 family will run 80-100% faster on the equivalent XC4000XL-1 devices. The pin compatibility among all XC4000 Series devices makes it simple to test actual design speeds — just retarget any design for an existing XC4000 Series FPGA to the appropriate XC4000XL-1 device using the Alliance Series or Foundation Series software.

Article Summary

This article describes the achievable performance (maximum clock frequency) in top-of-the-line FPGAs. It analyzes the performance of seven typical sub-functions and lists the achievable performance levels for the fastest available Xilinx XC4000XL device, compared with the fastest available Altera 10K100 device. All data was derived from the manufacturers' worst-case timing analyzer.

The remainder of this article describes the dramatic performance impact of three different design styles. It shows that you can often double the performance of the FPGA by spending some effort on optimizing the design structure for the specific FPGA architecture.

An expanded version of this article is available on WebLINX (www.xilinx.com), as an application note, under the title "Speed metrics for high performance FPGAs."

Selected Component Frequency Measurements

FREQ.	EXPLANATION	XC4062XL-1	10K100-3
Fio(int)	Clocked I/O referenced to internal clock	196 MHz	na
Fio(ext)	Clocked I/O referenced to external clock	74 MHz	54 MHz
Fio(lut)	Clocked I/O to CLB regs (referenced to external clock)	31MHz	29 MHz
Fdst(4,4)	Distance within 4 rows and 4 columns	196 MHz	156MHz
Fdst (0,128)	Distance across largest chip horizontally or vertically	79 MHz	71 MHz
Fdst (64,128)/2	Distance across largest chip diagonally and back	28MHz	28MHz
Flut(4,2)	Two cascaded 4 input LUTs between registers	130 MHz	82 MHz
Flut(4,4)	Four cascaded 4LUTs between registers	73 MHz	49 MHz
Flut(4,8)	Eight cascaded 4LUTs between registers	36 MHz	27 MHz

FREQ.	EXPLANATION	XC4062XL-1	10K100-3
Fmux(2)	64:32 Mux between registers	131 MHz	105 MHz
Fmux(8)	64:8 Mux between registers	80 MHz	60 MHz
Fmxu(64)	64:1 Mux between registers	56 MHz	38 MHz
Fequ(4)	16 x 4 bit AND terms between registers	164 MHz	86 MHz
Fequ(16)	4 x 16 bit AND term between registers	81 MHz	54 MHz
Fequ(64)	1 x 64 bit AND term between registers	30 MHz	17 MHz
Fadd(1,5)	5-bit adder between registers	135 MHz	148 MHz
Fadd(1,32)	32-bit adder between registers	73 MHz	43 MHz
Fadd(4,32)	4 cascaded 32-bit adders between registers	32 MHz	21 MHz
Fmem(16)	16 Bit 16 element dual port RAM between registers	128 MHz	na
Fmem(128)	16 Bit 128 element dual port RAM between registers	68 MHz	25 MHz
Fmem(1024)	16 Bit 1024 element dual port RAM between registers	40 MHz	na

"This combination of speed and density comes with low power and total compatibility with 3.3 volt or 5.0 volt logic."

XILINX®

FPGA Component Speeds

To determine the maximum speed of the components used in FPGA designs, a set of test designs was created. These designs, written in VHDL, measure fundamental aspects of FPGA performance. The following components were entered and tested for frequency:

- **I/O –** three configurations of I/O pins and clocks.
- **Interconnect –** registers separated by "N" rows and columns.
- **State Machines –** 1 to 6 levels (3-, 4-, and 5-input look-up tables).
- **Multiplexers –** 64:32, 64:16, 64:8, 64:4, 64:2, and 64:1 mux.
- **Constant Comparators ("AND" terms) –** 4-, 8-, 16-, 32-, and 64-bit AND terms.
- **Adders –** 4-, 8-, 16-, 24-, and 32-bit adders as well as 2- and 4-bit cascaded adders.
- **Memory–**Dual Port RAMs, 16-bits wide; 16-, 32-, 64-,128-, 256-, 512- and 1024-bits deep.

FPGA Design Style Affects Performance

In general, FPGA designs with a low ratio of registers to look-up tables (LUTs) run at lower clock rates than designs with equal numbers of registers and LUTs. Even higher clock rates can be achieved if additional registers are used to break up interconnect delays. Design styles can be characterized as low, medium, and high frequency based on the register-to-LUT ratio. They might also be called "easy," "medium," and "difficult." It is important to understand that this difference is not affected by the design entry method. It is just as easy to include registers in a VHDL design as in a schematic. In fact, high-level tools can include register re-timing methods which can significantly increase system frequency.

"No Problems" Design Style

If you've ever done a low-speed design for an FPGA, you know how convenient it is to ignore logic depth, pipelining, and placement issues. Logic synthesizers will often generate designs in this style because pipelining and logic placement are not automatically handled. The "no problem" design style requires that timing and placement not be an issue; if the design passes functional simulation, then it will route and meet the non-demanding timing.

Medium Frequency FPGA Design Style

Most designs intended for FPGAs fall into this design style. Your designs will tend to fall into this category, if you use one-hot state machines, Global Low Skew (GLS) buffered clocks, register all your big data-path components, and practice moderate floor-planning.

High Frequency Design Style

A high clock frequency allows little margin for such things as routing delay or carry propagation. To work at this level, the physical aspect of a design must be considered. It may mean adding registers to cover interconnect delay, or detailed floor-planning.

Design Style Summaries

Design Style	Characteristic Freq.	Registers /LUTs	Interconnect distance	Design Effort	Normalized Freq.	Density
Low Freq	Fmin	~0.5	Long	Lowest	0.5	Highest
Medium Freq	Ftyp	=1.0	Medium	Medium	1.0	Medium
High Freq	Fmax	~2.0	Short	Highest	2.0	Lowest

FPGA System Frequency Definitions

For maximum frequency designs, the type of functionality available to you is restricted. In fact, the types of components that run at the same maximum frequency can be used to define these design styles in a formal sense.

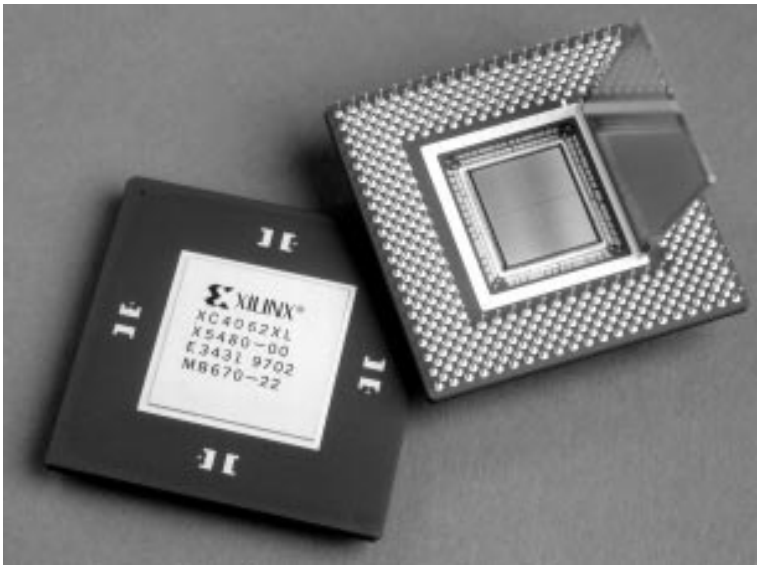
Continued on the following page

High Performance Design

Continued from the previous page

The components can be adders, I/O pins, state machines, or anything else you can build in an FPGA. For proper operation, all the components used must run at the selected system frequency. If the types of components used in a design are known, you can estimate the speed of a new design without detailed knowledge of the actual design. Alternatively, you can limit the types of components used in a design to insure hitting a target frequency.

The following table defines the types of components that are available within each design style; the selected components are generally compatible with each other, and a formal definition allows frequency measurements to be taken.



Component	Parameters Defined	High Freq.	Medium Freq.	Low Freq.
State machines	Number of cascaded 4LUTs	2 Logic Levels	4 Logic Levels	8 Logic Levels
Multiplexers	Number of input bits/ Number of output bits	64-bits/32-bits	64-bits/8-bits	64-bits/1-bit
"AND-OR" Terms	Number of Inputs bits/ Number of cascaded AND-OR terms	4-bit/1 level	16-bit/1 level	64-bit/2 levels
Adders	Number of input bits/ Numbers of cascaded adders	4-Bit/1 level	32-Bits/ 1 Level	32-Bits/4 Levels
Inputs/Outputs	Type of Input/Type of Output/ Timing Reference for Clock	"NoDelay" inputs/ "Fast" outputs/ internal clock	"Full Delay" inputs/ "Fast" outputs/ external GLS clock	"Full Delay" input via 4LUT/ "Slow" Outputs via 4LUT/ external GLS clock
Memory	Number of locations Dual Ported Memory	16-elements	128-Elements	1024 Elements
Interconnect	Distance between registers	4 CLBs	64 CLBs	128 CLBs

System Frequency Measurements

The system frequencies for the three associated design styles can now be measured. First the component frequencies required for a design style are measured, then the system frequency is determined. The system frequency is defined as the minimum speed of all the components necessary for each design style. To illustrate the point that Xilinx XC4000XL-1 devices are the world's fastest high-density FPGAs, these same measurements were made for a competitor's FPGA; the Altera 10K100-3 device is roughly the same size as the Xilinx XC4052XL. ◆

Frequency	Design Style	XC4062XL-1	10K100-3
Fmax	High Frequency	128 MHz	82 MHz
Ftyp	Typical system	68 MHz	43 MHz
Fmin	Low frequency	28 MHz	17 MHz

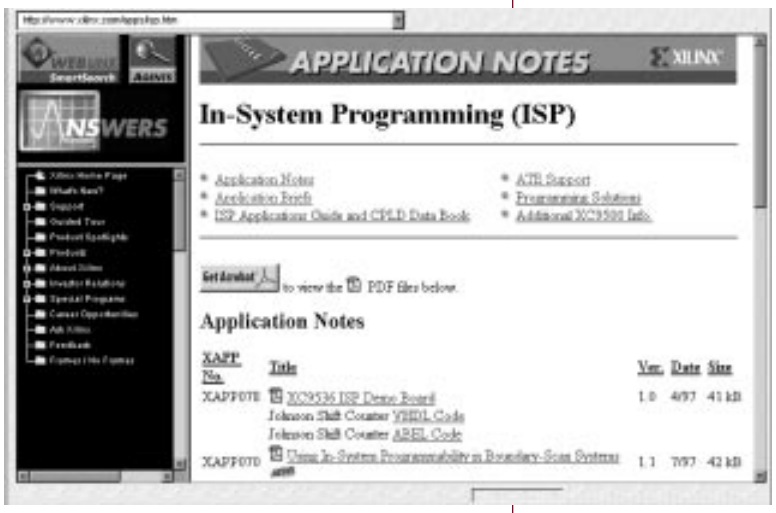
Integrating XC9500 ISP Capabilities With Manufacturing Test on the Teradyne Z1800

In-system programming (ISP) allows you to program and re-program devices that are already soldered on a system board. ISP streamlines manufacturing flows, allows you to update and reconfigure remote systems, and makes prototyping much easier. The XC9500 family integrates ISP functionality through the IEEE 1149.1 (JTAG) test access port without requiring any externally applied voltages greater than 5V. This allows JTAG-compatible automatic test equipment, such as the Teradyne Z1800, to program XC9500 devices.

Z1800 Configuration and Fixturing

The Teradyne Board Test System performs ISP as an integrated part of the manufacturing test process. In order to integrate programming into the system test flow, you need:

- A Teradyne Z1800 tester with the digital functional processor board running the F1 software.
- The Xilinx EZTag or JTAGProgrammer software.
- The zip file containing the Teradyne SVFP translator, C files, and software libraries (downloaded from WebLINX).
- A C compiler capable of producing a16-bit DOS executable for the Z1800. The computers provided with Teradyne board test systems support Microsoft Visual C++ and Borland Turbo C++ version 3.0 compilers.



Find it on the Web at: http://www.xilinx.com /apps/isp.htm

Availability

The svfp translator, C files, libraries, and accompanying documentation are available on WebLINX (www.xilinx.com), the Xilinx Web site. Point your browser to http://www.xilinx.com/apps/isp.htm and select the topic titled *Programming Xilinx XC9500 on a Teradyne Z1800 with DFP - EZTag Version*.

Xilinx now offers you full JTAG/ISP support for the top three ATE manufacturers: Teradyne, HP, and GenRad. The necessary software and documentation for all three ATE platforms is available free of charge from WebLINX.

With complete ATE support and the industry's most extensive JTAG capability, Xilinx is the ISP CPLD vendor of choice. ◆

Using Technology-Independent Intellectual Property *Are You Ready for 2*

By the year 2000, Xilinx will be producing devices containing more than 100,000 logic cells (2 million gates). You will soon have a canvas so broad that it will be difficult to paint all the landscape. We estimate that it will take a full 12 months and 20-30 engineers to fill a device of this density, if designing from scratch.

Clearly the solution to maintaining a trouble-free design cycle is to stop creating every design from scratch, and to start using technology-independent intellectual property. Just as it's easier to paint by numbers, it's easier to re-use blocks of logic. The use of intellectual property or core-based design modules is an essential component of a high-end "system on a chip" solution. The LogiCORE and AllianceCORE modules from Xilinx offer proven, pre-implemented, and fully verified cores that provide the fast time-to-market solutions you need.

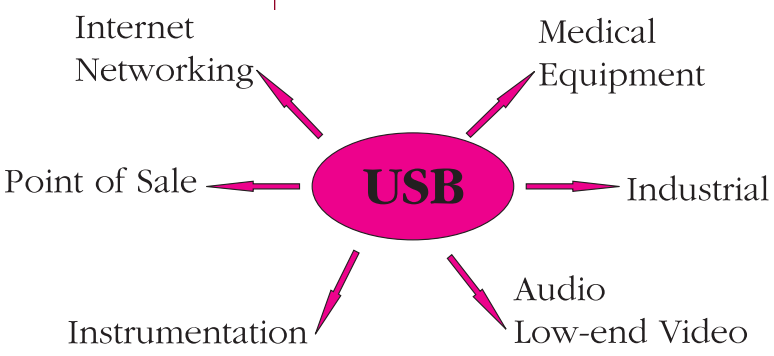
This article demonstrates the use of technology-independent intellectual property (IP) through the design of a Universal Serial Bus application.

Universal Serial Bus Case Study

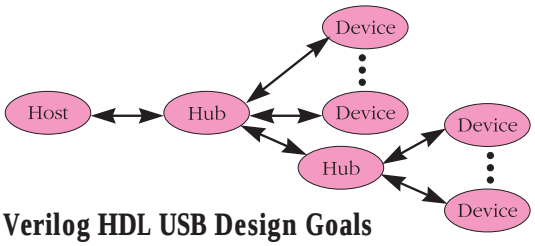
The Universal Serial Bus (USB) protocol was created to provide a standardized serial bus to be used in the personal and mobile computer markets. Just as PCI is becoming a standard parallel bus, USB is now becoming a standard PC serial bus for lower-bandwidth PC peripherals such as mice, keyboards, modems, and so on.

USB Protocol Description

The USB protocol uses a differential-twisted shielded pair for its physical medium. The signal coding is NRZI with bit stuffing, and has been designed to transmit data at two rates: 1.5 Mbps (low speed) and 12 Mbps (full speed). It can support up to 127 devices.



The USB architecture defines a host PC and "devices" or "functions" (such as keyboard or mouse) with "hubs" in the middle as necessary for fan-out.



Verilog HDL USB Design Goals

Mentor Graphics Inventra, a member of the Xilinx AllianceCORE partnership, has developed a family of USB functions and hub controller soft cores. These cores can be combined with application-specific back-end logic.

Inventra USB cores come in low speed and full speed versions for applications such as micro-controllers, audio, and generic user definable USB interfaces. These cores have been designed with the following goals in mind:

- A technology independent design methodology.
- Design implementation and mapping directed by synthesis timing constraints.
- Synthesis tools select state machines.
- Ability to re-use the bus interface with application-specific logic.

For this USB case study, an Inventra USB function controller core was selected. The USB function controller's hierarchy and logic was originally designed with its full-speed timing characteristics in mind. The USB function controller's hierarchy is illustrated in **Figure 1**.

While the full-speed USB Function Controller runs at 12 MHz, the design involves several blocks that run at 4X the basic rate, or 48 MHz. This 48 MHz clock is

Million Gates?

used to over-sample and drive both the data and the 12 MHz data clock from the serial NRZI USB data signal.

Controlling Timing

The design's logic was divided into different timing blocks as illustrated in **Figure 2**. This was done to understand the timing relationships both within and between blocks of logic.

By implementing the design using these timing blocks as the hierarchical boundaries, the Inventra engineers where able to clearly define timing specifications and constraints for the blocks of logic that needed to run at a rate of 48 MHz and those that needed to run only at 12 MHz. They were also able to control the timing interaction between these blocks.

By using the Xilinx Alliance series timing constraint capability, the global timing of 12 MHz was applied to the entire design. Then the more critical constraint of 48 MHz was applied to the flip-flops and I/O pads that needed to run at the 4X rate.

State Machines

The synthesis tools were also used to select the most efficient and highest performance state machines. The USB function controller consists of, among other things, five state machines. The Inventra engineers found that two of the state machines would not meet the system timing requirements if standard encoding methods were used for synthesis. By directing the synthesis tools to use "one hot" encoding for these two machines, performance requirements for these two blocks were met. To maintain the core's design re-use capability, the Verilog RTL code was not modified; only the synthesis options were changed.

Module Re-use

By developing the USB function controller as a reusable IP, Inventra is able to maintain a single version of RTL source code with a range of interfacing options for various back-end applications. This back-end application logic can also be developed using this technology independent methodology, allowing the modules to interface easily.

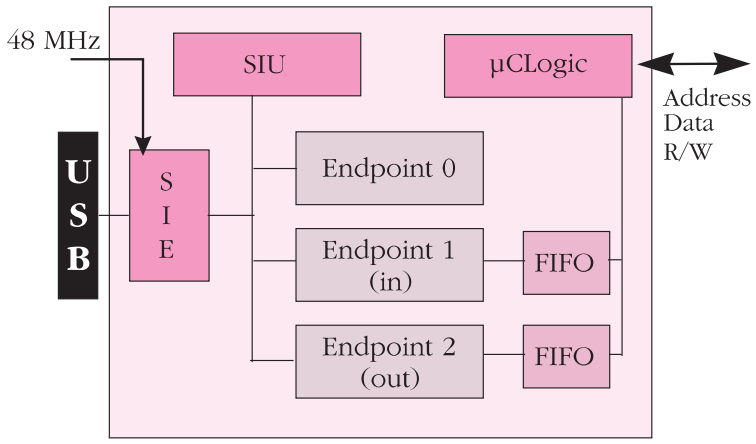


Figure 1:
USB Core Hierarchy

Summary

This USB IP development case study shows how generic Verilog RTL code was used to define the register transfer level functions while synthesis was used to produce the gate level implementation. The constraint files and directives are used to drive both the synthesis and the Alliance Series place and route tools.

In this technology-independent IP design flow, the Xilinx design tools used the new timing-driven placement and routing algorithms. The robust timing analysis tools were also used to verify that the timing requirements were met. There was no hand placement or routing, and no floor-planing was required.

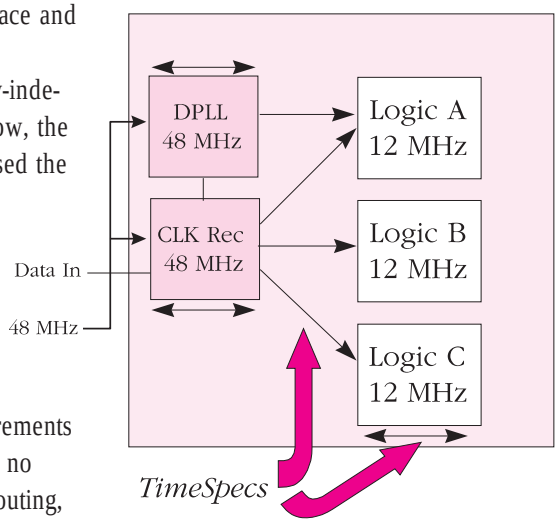


Figure 2:
Timing Blocks

The use of this technology independent methodology will become more and more important as device densities increase. Xilinx is committed to delivering not only the highest performance and highest density devices, but also to providing you with the tools you need to develop them quickly and easily.

For information on the Xilinx LogiCORE, AllianceCORE, or Mentor Graphics Inventra USB products, check out the Xilinx CORE Solutions web site at: http://www.xilinx.com/products/logicore/logicore.htm ◆

Plan Now for Lower Supply Voltages

The relentless pressure to achieve higher speed, higher density, lower cost, and lower power consumption is driving Xilinx (and other IC manufacturers) to use ever-thinner gate oxides and smaller geometries, resulting in a requirement for lower supply voltages.

At 0.35 microns, devices cannot reliably tolerate a 5 volt supply, and require a 3.3 volt supply instead. At 0.25 microns, the supply voltage must be lowered to 2.5 volts. At 0.18 microns, a 1.8 volt supply will be likely. To take advantage of the technical and economic benefits of these smaller process geometries, you will face several challenges:

- Distributing multiple supply voltages on the PC board.
- Interfacing between CMOS devices using different supply voltages.
- Sequencing supply voltages.

Distributing Multiple Supply Voltages on the PC Board

At today's speeds, the analog characteristics of a PC board play a strong role in determining digital system performance. Even modest-length (3 inch) interconnects must be treated as transmission lines. Pay attention to each signal path, including the complete current loop from the positive supply connection, through the IC and interconnects, through the ground distribution, through the decoupling capacitors, back to the positive supply terminal.

> *"At 0.35 microns, devices cannot reliably tolerate a 5 volt supply, and require a 3.3 volt supply instead."*

Modern designs require PC boards with at least four layers (and usually more). At least one inner layer must be dedicated as a ground plane and kept as undisturbed as possible. Any major hole in the ground plane forces the ground current to take detours — increasing the inductance and causing ground voltage spikes. In simple designs, 5 volt and 3.3 volt supplies can share a common power plane.

To demonstrate the importance of good Vcc decoupling, assume that you have a 40 MHz clock and the device consumes 1 amp. Most of the current flow will be in the first 5 ns of the 25 ns clock period. This 5 amp peak current must be supplied by the sum of the decoupling capacitors. In this example, 5 amps times 5 ns causes a 250 mV drop on a 0.1 µF decoupling capacitance, creating a possible problem. Here are some recommendations:

- Decoupling capacitors must have very low inductance and series resistance. The total capacitance value is less important, as long as it exceeds 0.1 µF. The best way to achieve low impedance at gigahertz speeds is to use multiple capacitors in parallel. Use 0.01 to 0.1 µF ceramic capacitors mounted very close to each Vcc pin and directly connected to the ground plane.
- Signal lines must be kept short. A narrow, 0.25 inch (6 mm) trace represents an inductance of 20 nH. A current transient of 100 mA/ns causes a voltage drop of 2 volts across this inductance, which is unacceptable.
- Some PC boards can use an extremely thin dielectric layer between the ground and Vcc planes to achieve excellent distributed decoupling capacitance.
- Ground bounce, cross-talk, and other external noise must be minimized. Xilinx provides a slew-rate-limited output option, individually programmable for each pin, so you can slow the transition rate on all non-critical outputs.

Interfacing Between Devices with Different Supply Voltages

Because all supply voltages share a common ground, there are no problems interfacing at Low logic levels. All potential problems occur when interfacing at High logic levels. For example:

- **3.3 volt logic High driving a 5 volt input** — There is no problem when the 5 volt device has a TTL-level input threshold of approximately 1.3 volt. This is true for most CMOS devices. The driving 3.3 volt output

High level is close to Vcc, and thus well above the required Vih of 2 volts.

- **5 volt logic High driving 3.3 volt input** — In most cases, the High 5 volt output voltage will force excessive current into the 3.3 volt input. The pins on older Xilinx 3.3 volt FPGAs, and on most other manufacturers' 3.3 volt devices have a clamp diode between each pin and Vcc to protect the circuit against electrostatic discharge (ESD). This diode starts conducting when the pin is driven more than 0.7 volts positive with respect to its Vcc. This diode presents a problem in mixed-voltage systems, because it clamps whenever a 5 volt logic High is connected to a 3.3 volt input.

  Xilinx has overcome this problem by eliminating the clamp diode between the pin and Vcc in the circuit structure of the Xilinx XC4000XL family. The pin can thus be driven as high as 5.5 volts without regard to the actual supply voltage on the receiving input. Therefore, these devices are unconditionally 5 volt tolerant, and you can ignore all interface precautions. Excellent
  ESD protection (several thousand volts) is achieved by means of a patented diode-transistor structure that does not connect to Vcc. Directly connecting an active High 5 volt CMOS output to an active High 3.3 volt output creates contention and must be avoided.

  When 3.3 volt inputs are being driven from a TTL-level output using an n-channel pull-up transistor — available as an option on all XC4000 and XC4000E and XC4000EX devices — the input current is naturally limited to less than a few mA, even when the 5 volt supply is at 5.25 volts while the 3.3 volt supply is at 3.0 volts; a very unlikely combination. At nominal supply voltage levels, the current is approximately 1 mA.

  When non-5-volt-tolerant inputs are driven from a CMOS-level, complementary, rail-to-rail output, you must somehow limit the current. A 1 Kohm resistor limits the current to less than 2 mA, but causes a slight speed penalty (1 Kohm x 35 pF = 35 ns)

- **3.3 volt logic High driving a "CMOS threshold" 5 volt input** — This interface situation should be avoided. An active High 3.3 volt output cannot be pulled higher, because the internal pull-up transistor represents an impedance of approximately 50 ohms for any current in either direction. A pull-up resistor to 5 volts is therefore useless. If the internal pull-up transistor is disabled (open drain output) the pin can be pulled higher, until the ESD clamp becomes conductive. The pins on the Xilinx XC4000X famil can thus be configured as open drain, and an external resistor can pull them all the way to 5 volts (with a resulting RC speed penalty).

> *"At 0.25 microns, the supply voltage must be lowered to 2.5 volts. At 0.18 microns, a 1.8 volt supply will be likely."*

Sequencing Supply Voltages

Any system with more than one supply voltage faces the possibility of these voltages being applied in an undefined or uncontrolled sequence. For most ICs, this means you must calculate the maximum current flowing into the pins of the non-powered device. The current value depends on the powered-up device's output structure (complementary outputs drive the highest current) and on the voltage compliance (impedance) of the non-powered Vcc distribution net. If it is held rigidly to ground, the undesired current will be high. If the non-powered Vcc can easily be pulled High, the current will be far less. Most inputs will tolerate 50 mA for a few seconds, and 10 mA for unlimited time. For significantly higher currents there might be the short-term risk of latch-up, and the long-term risk of metal migration if the high current persists for thousands of hours.

The Xilinx XC4000XL family is 5 volt tolerant, even when their Vcc is zero. Therefore, these devices have no problem with arbitrary power sequencing or even with "hot plug-in". When 5 volt power is applied first, there is no current into the Xilinx FPGAs. When 3.3 volt power is applied first, the device outputs can be kept in a 3-state condition by connecting the 5 volt Vcc line as an active-Low Global 3-state input to the

Continued on the following page

HardWire: *Ensuring a Successful FPGA to*

"Here are some of the critical issues for ensuring a successful FPGA conversion."

HardWire™ conversion of FPGAs into ASICs gives system designers the power of programmability, greatly accelerating the design phase, while adding the cost-effectiveness of a true ASIC solution, especially for density ranges of 25,000 gates and above.

Since 1991, Xilinx's HardWire service has completed more than 700 conversions of flexible FPGA designs to low-cost ASICs ready for volume production.

Here are some of the critical issues for ensuring a successful FPGA conversion.

1. Use Synchronous Design Methods

We recommend that you design your FPGA with the production solution (ASIC) in mind. FPGAs can sometimes "hide" design flaws. These flaws can manifest themselves in the ASIC version when the design speeds up. The most common issues are with asynchronous paths and simultaneous switching output noise.

To ensure consistent timing, your design must be synchronous. Because FPGAs are RAM-based devices, an ASIC conversion will remove all the programmable elements and replace them with metal vias. In almost every case, the device timing speeds up substantially. If a design is asynchronous, the timing relationships may not behave the same in the ASIC as they did in the FPGA, perhaps causing race conditions.

In asynchronous FPGA designs, the small glitches generated by unstable outputs can be filtered by the pass transistors used to control the routing of long nets. However, in the ASIC version, those pass transistors are replaced by metal vias, possibly allowing an unfiltered glitch to propagate throughout the system.

If your design must be asynchronous, it is imperative that you carefully plan the timing relationships on the device itself, and between chips at the system level. Building in generous timing margins can help.

Lower Supply Voltages *Continued from the previous page*

3.3 volt devices, again eliminating any undesirable current.

Converting to Lower Voltage Designs

Xilinx 3.3 volt FPGAs are fully compatible with their 5 volt equivalents. You can start a design using 5 volt supplies, later plugging in the 3.3 volt devices with no concern for functionality, speed, pin locations, or logic levels.

The next transition — to 2.5 volts — will arrive within a year. This change will be less of a challenge because Xilinx will, at first, use 2.5 volts only for the internal logic, while running the I/O with 3.3 volt power. You must provide the additional Vcc, but you need not be concerned about signal level incompatibilities. However, we will increase the number of Vcc and ground pins.

To ease these transitions, the IC industry plans to accommodate direct interfacing between three successive generations: first between 5, 3.3, and 2.5 volt devices, and then in 1999, 3.3, 2.5, and 1.8 volt devices.

Conclusion

New improvements in IC technology enable a wealth of new, smaller systems with higher performance and lower power requirements. To take advantage of these improvements, designers must provide new supply voltages — 3.3 volts now and 2.5 volts in the near future.

In many cases, these new, lower-voltage devices will be used side-by-side with older, 5 volt parts. These mixed-voltage environments could create a variety of design challenges, especially when using FPGAs that are not specifically designed to operate in mixed-voltage environments. The new 3.3 volt Xilinx FPGA families are immune to all power sequencing problems and can be interfaced directly with 5 volt devices, making them an ideal solution for many mixed-voltage systems. ◆

An expanded version of this article appears in the August 18, 1997 edition of Electronic Design.

ASIC Conversion

2. Thoroughly Simulate Your FPGA Design

Xilinx does not require functional or timing simulations, prior to FPGA/ASIC conversion. However, the FPGA design destined for an ASIC should be exhaustively simulated.

Unit delay simulation can be thought of as "best-case" simulation, since the logic will usually perform under the actual unit delay. This can set the "timing minimum" pole. The maximum simulation sets the "timing maximum" pole. If there are no functional differences between the maximum and minimum, then the design is likely to be free of timing dependencies.

3. Plan Your RAM Usage

RAM on an FPGA device is very efficient. However, RAM on an ASIC can be inefficient if not well planned,; and large RAM blocks may require extensive silicon area. Generally, if a design's RAM requirements exceed 25-35% of the total CLBs used, the die size will increase substantially, perhaps requiring triple-level metal for additional routing. One single-port RAM bit equals roughly four to six gate array gates; one dual port RAM bit can require seven to ten gates. If large amounts of RAM are required, it may be appropriate to leave part off-chip, or in extreme cases, consider a standard cell implementation.

4. Pay Attention to FPGA Configuration Modes

FPGA configuration modes are key. In the FPGA, data is stored in the PROM. The PROM is downloaded to the FPGA via one of many configuration modes, allowing the system to "wake up" in an orderly manner. During conversion, the normal configuration mode is "instant on." If the ASIC device is still dependent on other events prior to "waking up," you should implement the configuration mode into the ASIC. Otherwise, system-level timing errors may result or ASICs might appear non-functional. Prior to ASIC conversion, the configuration scheme must be well documented so that configuration logic can be included in the ASIC version.

5. Select Your Best Vendor

Finally, select a vendor who can handle the features, density, and volume production of the resulting ASIC. Many ASIC vendors offer a "conversion service" that is nothing more than netlist translation into a third-party library. After the netlist translation, customers must re-simulate and re-validate both timing and functionality.

Xilinx supports full turnkey conversion, using Xilinx-specific tools and technology. The Xilinx-converted ASIC has Xilinx-specific features built into the die to eliminate the mismatch between the FPGA features and the ASIC implementation.

HardWire is the only FPGA conversion method that supports Xilinx devices with state-of-the-art technology and guarantees success. Xilinx design engineers work closely with you to ensure that all considerations have been reviewed. The FPGA is converted to a Xilinx HardWire device using the same fabrication facilities used to make the FPGA, with greater than 90% first-attempt success rates.

When considering an FPGA to ASIC conversion project, it is wise to review all the design considerations, perform the critical system level testing, and most of all choose a vendor who can support your specific requirements. ◆

"When considering an FPGA to ASIC conversion project, it is wise to review all the design considerations, perform the critical system level testing, and most of all choose a vendor who can support your specific requirements."

COMPONENT AVAILABILITY CHART

PINS	TYPE	CODE	XC3020A	XC3030A	XC3042A	XC3064A	XC3090A	XC3020L	XC3030L	XC3042L	XC3064L	XC3090L	XC3142L	XC3190L	XC3120A	XC3130A	XC3142A	XC3164A	XC3190A	XC3195A	XC4003E	XC4005E	XC4006E	XC4008E	XC4010E	XC4013E	XC4020E	XC4025E	XC4028EX	XC4036EX	XC4005XL	XC4010XL	XC4013XL	XC4020XL	XC4028XL	XC4036XL	XC4044XL	XC4052XL
44	PLASTIC LCC	PC44		◆												◆																						
	PLASTIC QFP	PQ44																																				
	PLASTIC VQFP	VQ44																																				
	CERAMIC LCC	WC44																																				
64	PLASTIC VQFP	VQ64		◆					◆							◆																						
68	PLASTIC LCC	PC68	◆	◆											◆	◆																						
	CERAMIC LCC	WC68																																				
84	PLASTIC LCC	PC84	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆						◆	◆						
	CERAMIC LCC	WC84																																				
	CERAMIC PGA	PG84	◆	◆	◆										◆	◆	◆																					
100	PLASTIC PQFP	PQ100	◆	◆	◆										◆	◆	◆				◆	◆									◆	◆						
	PLASTIC TQFP	TQ100														◆	◆																					
	PLASTIC VQFP	VQ100		◆	◆				◆	◆			◆			◆	◆				◆										❖								
	TOP BRZ. CQFP	CB100	◆		◆										◆	◆	◆																					
120	CERAMIC PGA	PG120																			◆																	
132	PLASTIC PGA	PP132			◆	◆											◆	◆																				
	CERAMIC PGA	PG132			◆	◆											◆	◆																				
144	PLASTIC TQFP	TQ144			◆	◆	◆			◆	◆	◆	◆	◆			◆	◆	❖			◆	◆								❖	❖						
	CERAMIC PGA	PG144																																				
	HI-PERF TQFP	HT144																															❖	❖					
156	CERAMIC PGA	PG156																				◆	◆															
160	HI-PERF QFP	HQ160																																	❖	❖	❖	
	PLASTIC PQFP	PQ160				◆	◆											◆	◆	◆		◆	◆	◆	◆	◆					◆	◆	◆	◆				
164	TOP BRZ. CQFP	CB164					◆												◆	◆		◆															
175	PLASTIC PGA	PP175					◆												◆	◆																	
	CERAMIC PGA	PG175					◆												◆	◆																	
176	PLASTIC TQFP	TQ176					◆					◆		◆					◆													❖					
	HI-PERF TQFP	HT176																															❖	❖				
191	CERAMIC PGA	PG191																						◆	◆												
196	TOP BRZ. CQFP	CB196																							◆												
208	PLASTIC PQFP	PQ208					◆												◆	◆		◆	◆	◆	◆	◆					◆	◆	◆	◆				
	HI-PERF QFP	HQ208																							◆	◆	◆		◆						◆	◆	❖	
223	CERAMIC PGA	PG223																		◆						◆	◆	◆				◆					
225	PLASTIC BGA	BG225																							◆	◆											
228	TOP BRZ. CQFP	CB228																								◆		◆									
240	PLASTIC PQFP	PQ240																								◆						◆	◆				
	HI-PERF QFP	HQ240																								◆	◆	◆	◆	◆				◆	◆	◆	◆
256	PLASTIC BGA	BG256																														◆	◆	◆	❖			
299	CERAMIC PGA	PG299																										◆	◆						◆			
304	HI-PERF. QFP	HQ304																										◆	◆	◆					◆	◆	❖	❖
352	PLASTIC BGA	BG352																											◆	◆					◆	◆	◆	
411	CERAMIC PGA	PG411																												◆						◆	◆	◆
432	PLASTIC BGA	BG432																												◆						◆	◆	◆
475	CERAMIC PGA	PG475																																				
559	CERAMIC PGA	PG559																																				
560	PLASTIC BGA	BG560																																				◆

AUGUST 1997

PINS	TYPE	CODE	XC4062XL	XC4085XL	XC4005L	XC4010L	XC4013L	XC5202	XC5204	XC5206	XC5210	XC5215	XC6216	XC6264	XC9536	XC9572	XC95108	XC95216	XC95288
44	PLASTIC LCC	PC44													◆	❖			
	PLASTIC QFP	PQ44																	
	PLASTIC VQFP	VQ44																	
	CERAMIC LCC	WC44																	
64	PLASTIC VQFP	VQ64																	
68	PLASTIC LCC	PC68																	
	CERAMIC LCC	WC68																	
84	PLASTIC LCC	PC84			◆	◆		◆	◆	◆	◆					◆	◆		
	CERAMIC LCC	WC84																	
	CERAMIC PGA	PG84																	
100	PLASTIC PQFP	PQ100						◆	◆	◆						◆	◆		
	PLASTIC TQFP	TQ100														◆	◆		
	PLASTIC VQFP	VQ100						◆	◆	◆									
	TOP BRZ. CQFP	CB100																	
120	CERAMIC PGA	PG120																	
132	PLASTIC PGA	PP132																	
	CERAMIC PGA	PG132																	
144	PLASTIC TQFP	TQ144						◆	◆	◆	◆		◆						
	CERAMIC PGA	PG144																	
	HI-PERF TQFP	HT144																	
156	CERAMIC PGA	PG156						◆	◆										
160	HI-PERF QFP	HQ160																	
	PLASTIC PQFP	PQ160							◆	◆	◆	◆					◆	◆	
164	TOP BRZ. CQFP	CB164																	
175	PLASTIC PGA	PP175																	
	CERAMIC PGA	PG175																	
176	PLASTIC TQFP	TQ176				◆				◆	◆								
	HI-PERF TQFP	HT176																	
191	CERAMIC PGA	PG191							◆										
196	TOP BRZ. CQFP	CB196																	
208	PLASTIC PQFP	PQ208			◆	◆	◆			◆	◆								
	HI-PERF QFP	HQ208										◆						◆	◆
223	CERAMIC PGA	PG223									◆								
225	PLASTIC BGA	BG225					◆				◆	◆	◆						
228	TOP BRZ. CQFP	CB228																	
240	PLASTIC PQFP	PQ240					◆				◆								
	HI-PERF QFP	HQ240	◆									◆	◆	◆					
256	PLASTIC BGA	BG256																	
299	CERAMIC PGA	PG299										◆	◆						
304	HI-PERF. QFP	HQ304	❖									◆	◆						
352	PLASTIC BGA	BG352										◆		◆				◆	◆
411	CERAMIC PGA	PG411												◆					
432	PLASTIC BGA	BG432	◆																
475	CERAMIC PGA	PG475	◆																
559	CERAMIC PGA	PG559	◆	◆															
560	PLASTIC BGA	BG560	◆	◆															

◆ = Product currently shipping or planned

❖ = New since last issue of *XCell*

XILINX RELEASED SOFTWARE STATUS - AUGUST 1997

XILINX INDIVIDUAL PRODUCTS

KEY	PRODUCT CATEGORY	PRODUCT DESCRIPTION	PRODUCT FUNCTION	XILINX PART REFERENCE NUMBER	CURRENT VERSION BY PLATFORM PC1 *6.2*	SN2 *4.1.x*	HP7 *9.01*	LAST UPDT COMP	PREVIOUS VERSION RELEASE	NOTES/ FEATURES
U	CORE XEPLD	Support	Core Implementation	DS-550-xxx	6.0.1	5.2.1	5.2.1	7/96	5.2/6.0	PC update by request only
U*	XABEL-CPLD	XC9500 Support	Entry/Simulation/Core	DS-571-PC1	6.1.2			11/96	6.1.1	New version w/Win 95 to 3.11, update by request
*	XACT-CPLD	XC9500 Support	Core + Interface	DS-560-xxx	6.0.1	6.0.1	6.0.1	7/96	6.0	
I	Mentor	8.4=A.4	Interface and Libraries	DS-344-xxx		5.2.1	5.2.1	7/96	5.20	
I	Synopsys		Interface and Libraries	DS-401-xxx		5.2.1	5.2.1	7/96	5.20	DA1 platform remains at v5.2
I	Viewlogic		Interface and Libraries	DS-391-xxx	6.0.1	5.2.1	5.2.1	7/96	6.0	
	XABEL		Entry,Simulation,Lib, Optimizer	DS-371-xxx	5.2.1	5.2.1	5.2.1	7/96	5.2/6.0	Now available on HP7
I	XBLOX		Module Generator & Optimizer	DS-380-xxx	5.2.1	5.2.1	5.2.1	7/96	5.2/6.0	
E, I	Verilog	2K,3K,4K,4KE,5K Lib.	Models & XNF Translator	ES-VERILOG-xxx		1.00	1.00	na	na	Sun and HP
	Alliance Base PC	4KE/L/XL/XC9500	FPGA/CPLD support to 8K gates	DS-ALI-BAS-PC	1.3			na	1.2	Win 95 & NT 4.0
	Alliance Std. PC	4KE/L/EX/XL/XC9500	FPGA/CPLD support unlim. gates	DS-ALI-STD-PC	1.3			na	1.2	Win 95 & NT 4.0
	Alliance Base Workstation	4KE/L/XL/XC9500	FPGA/CPLD support to 8K gates	DS-ALI-BAS-WS		1.3	1.3	na	1.2	Solaris 5.4, 5.5; OS 2.4, 2.5; HP-UX, HP715
	Alliance Std. Workstation	4KE/L/EX/XL/XC9500	FPGA/CPLD support unlim. gates	DS-ALI-STD-WS		1.3	1.3	na	1.2	Solaris 5.4, 5.5; OS 2.4, 2.5; HP-UX, HP715
	Turns Engine 10-pk Dev. Sys. Opt.	4KE/L/EX/XL/XC9500	Cap. 10 P&R runs on multi. WS	DO-ALI-TE1-WS		1.3	1.3	na	1.2	Solaris 5.4, 5.5; OS 2.4, 2.5; HP-UX, HP715
	Turns Engine 50-pk Dev. Sys. Opt.	4KE/L/EX/XL/XC9500	Cap. 50 P&R runs on multi. WS	DO-ALI-TE5-WS		1.3	1.3	na	1.2	Solaris 5.4, 5.5; OS 2.4, 2.5; HP-UX, HP715
	Workview Office Dev. Sys. Opt.	4KE/L/EX/XL/XC9500	FPGA/CPLD schem., sim., lib, intf.	DO-ALI-WVO-PC	1.3			na	1.2	Win 95 & NT 3.5.1, 4.0
	Alliance Evaluation Kit	4KE/L/EX/XL/XC9500	Eval. kit for Alliance base & wkstns	DS-ALI-EVAL	1.3	1.3	1.3	na	1.2	Solaris, OS, HP-UX, HP715, Win95, NT

XILINX PACKAGES

		SILICON SUPPORT 2K	3K	4K/E	5K	7K	9K						
I	Cadence	X	X		X			DS-CDN-STD-xxx		5.2.1	5.2.1	7/96	5.20	
I	Mentor	X	X		X			DS-MN8-STD-xxx		5.2.1	5.2.1	7/96	5.20	No AP1 update
I	Mentor	X	X		X			DS-MN8-ADV-xxx		7.00	7.00	na	na	
I	Synopsys		X		X			DS-SY-STD-xxx		5.2.1	5.2.1	7/96	5.20	Includes DS-401 v5.2
I	Viewlogic	X	X		X			DS-VL-STD-xxx	6.0.1	5.2.1	5.2.1	7/96	5.26.0	DA1 platform remains at v6.0
I	Viewlogic/S	X	X		X			DS-VLS-STD-PC1	6.0.1			7/96	6.0	Currently updating in-warranty cust. w/WVO
U, I	3rd Party Alliance	X	X		X			DS-3PA-BAS-xxx	6.0.1			7/96	na	Customer w/v6.0 will receive v6.0.1 update
I	3rd Party Alliance	X	X		X			DS-3PA-STD-xxx	6.0.1	5.2.1	5.2.1	7/96	5.2/6.0	Includes 502/550/380
	Foundation Series			X		X	X	DS-FND-BAS-PC	1.3			8/97	6.0.2	Includes support for XC4000E/X & XC9500
	Foundation Series			X		X	X	DS-FND-BSV-PC	1.3			8/97	6.0.2	Includes support for XC4000E/X & XC9500
	Foundation Series			X		X	X	DS-FND-STD-PC	1.3			8/97	6.0.2	Includes support for XC4000E/X & XC9500
	Foundation Series			X		X	X	DS-FND-STV-PC	1.3			8/97	6.0.2	Includes support for XC4000E/X & XC9500
	Foundation Series			X		X	X	DL-FND-BAS-PC	1.3			8/97	6.0.2	XC4000 not supported. Bill only additional lic.
	LogiCore-PCI Slave							LC-DI-PCIS-C	1.10	1.10	1.10	na	na	Requires signed license agreement
	LogiCore-PCI Master							LC-DI-PCIM-C	1.10	1.10	1.10	na	na	Requires signed license agreement
	Evaluation	X	X		X			DS-EVAL-XXX-C	2.00	2.00	2.00	4/96	01/04	PC, Sun, HP kits with v5.2.1 and v6.0.1

KEY: *N=New Product U= Update by request only I=Libraries, interfaces and XBLOX are included with versions 1.2 & 1.3 * = Check FTP site for most current revision of EZTAG programming software..*

Programmer Support For Xilinx XC1700 Serial Proms - August 1997

MANUFACTURER	MODEL	XC1718D XC1736D XC1765D	XC1718L XC1765L	XC17128D XC17256D	XC17128L XC17256L
ADVANTECH	PC-UPROG LABTOOL-48	NOT QUALIFIED			
ADVIN	PILOT-U24	10.84B		10.84B	
	PILOT-U28	10.84B		10.84B	
	PILOT-U32	10.84B		10.84B	
	PILOT-U40	10.84B		10.84B	
	PILOT-U84	10.84B		10.84B	
	PILOT-142	10.84B		10.84B	
	PILOT-143	10.84B		10.84B	
	PILOT-144	10.84B		10.84B	
	PILOT-145	10.84B		10.84B	
AMERICAN RELIANCE, iNC.	SPECTRUM-48				
B&C MICROSYSTEMS INC.	PROTEUS-UP40	3.7Q		3.7Q	
BP MICROSYSTEMS	CP-1128				
	EP-1140				
	BP-1200	V3.15	V3.15	V3.15	V3.15
	BP-1400	V3.15	V3.15	V3.15	V3.15
	BP-2100	V3.15	V3.15	V3.15	V3.15
	BP-2200	V3.15	V3.15	V3.15	V3.15
BYTEK	135H-FT/U	8E	8E	8E	8E
	MTK-1000	8E	8E	8E	8E
	MTK-2000	8E	8E	8E	8E
	MTK-4000	8E	8E	8E	8E
	FIREMAN-8M	8E	8E	8E	8E
	FIREMAN-8X	8E	8E	8E	8E
	CHIPBURNER-40	1.0a	1.0a	1.0a	1.0a
DATAMAN	DATAMAN-48	V1.30		V1.30	
DATA I/O	UniSite	V5.4	V5.4	V5.4	BBS
	2900	V5.4	V5.4	V5.4	BBS
	3900	V5.4	V5.4	V5.4	BBS
	AutoSite	V5.4	V5.4	V5.4	BBS
	ChipLab	V5.4	V5.4	V5.4	BBS
	2700	V5.4	V5.4	V5.4	BBS
DEUS EX MACHINA	XPGM	V1.60	V1.60	V1.60	V1.60
ELECTRONIC ENGINEERING TOOLS	ALLMAX/ALLMAX+	V2.4U	V2.4U	V2.4U	
	MEGAMAX	V1.1E	V1.1E	V1.1E	
ELAN DIGITAL SYSTEMS	3000-145 5000-145 6000 APS	NOT QUALIFIED			
EQUINOX					
HI-LO SYSTEMS RESEARCH	All-03A	V3.19	V3.19	V3.19	V3.19
	All-07	V3.19	V3.19	V3.19	V3.19
	All-11				
ICE TECHNOLOGY LTD	Micromaster 1000/E	V3.17	V3.17	V3.17	V3.17
	Speedmaster 1000/E	V3.17	V3.17	V3.17	V3.17
	Micromaster LV	V3.17	V3.17	V3.17	V3.17
	LV40 Portable	V3.17	V3.17	V3.17	V3.17
	Speedmaster LV	V3.17	V3.17	V3.17	V3.17

MANUFACTURER	MODEL	XC1718D XC1736D XC1765D	XC1718L XC1765L	XC17128D XC17256D	XC17128L XC17256L
LEAP ELECTRONICS	LEAPER-10	V2.0		V2.0	
	LP U4	V2.0		V2.0	
LINK COMPUTER GRAPHICS	CLK-3100	V5.61		V5.61	
LOGICAL DEVICES	ALLPRO-40				
	ALLPRO-88	V2.7		V2.7	
	ALLPRO-88XR	V2.7		V2.7	
	ALLPRO-96	6.5.10	6.5.10	6.5.10	6.5.10
	CHIPMASTER 2000	V2.4U		V2.4U	
	CHIPMASTER 6000	V1.31A		V1.31A	
	XPRO-1	SPROM.310		SPROM.310	
MICROPROSS	ROM 5000 B	V1.94		V1.94	
	ROM 3000 U	V3.84		V3.84	
MQP ELECTRONICS	MODEL 200	6.46	6.46	6.46	
	SYSTEM 2000	2.25	2.25	2.25	
	PIN-MASTER 48	V1.25	V1.25	V1.25	V1.25
NEEDHAM'S ELECTRONICS	EMP20	V3.10		V3.10	
OMC	Typro C				
	Typro S				
Phyton	Multiprog				
RED SQUARE	IQ-180 IQ-280 Uniwriter 40 Chipmaster 5000	NOT QUALIFIED			
SMS	Expert Optima Multisyte Sprint Plus48	NOT QUALIFIED			
STAG	Eclipse Quasar	6.5.10	6.5.10	6.5.10	6.5.10
SUNRISE	T-10 UDP T-10 ULC	NOT QUALIFIED			
SUNSHINE	POWER-100	V8.40		V8.40	
	EXPRO-60/80	V8.40		V8.40	
SYSTEM GENERAL	TURPRO-1	V2.26H	V2.26H	V2.26H	V2.26H
	TURPRO-1 F/X	V2.26H	V2.26H	V2.26H	V2.26H
	TURPRO-1 T/X				
	APRO	V1.24			
	MULTI-APRO	V1.16	V1.16	V1.16	V1.16
TRIBAL MICROSYSTEMS	TUP-300	V3.19	V3.19	V3.19	V3.19
	TUP-400	V3.19	V3.19	V3.19	V3.19
	FLEX-700	V3.19	V3.19	V3.19	V3.19
XELTEK	SuperPRO				
	SuperPRO II	2.4B		2.4B	
	SuperPRO II/P	2.4B		2.4B	
XILINX	HW-112	5.20		BBS/FTP	
	HW-130	V2.03	V2.03	V2.03	V2.03

CHANGES SINCE LAST ISSUE PRINTED IN COLOR

Programmer Support For XC9500 CPLDs — August 1997

MANUFACTURER	MODEL	9536/F	9572/F	95108/F	95216/F	95288/F
ADVANTECH	PC-UPROG LABTOOL-48	Sept-97	Sept-97			
ADVIN SYSTEMS	PILOT-U24 PILOT-U28 PILOT-U32 PILOT-U40 PILOT-U84 PILOT-U142 PILOT-U143 PILOT-U144 PILOT-U145					
AMERICAN RELIANCE, INC.	SPECTRUM-48					
B&C MICROSYSTEMS, INC.	Proteus					
BP MICROSYSTEMS	CP-1128 EP-1140 BP-1200 BP-1400 BP-2100 BP-2200	 V3.21 V3.21 V3.21 V3.21	 BBS BBS BBS BBS	 V3.21 V3.21 V3.21 V3.21		
BYTEK	135H-FT/U MTK-1000 MTK-2000 MTK-4000					
DATAMAN	DATAMAN-48					
DATA I/O	2700 2900 3900/AutoSite Chiplab UniSite	 BBS BBS BBS	 BBS BBS	 BBS BBS		
DEUS EX MACHINA ENGINEERING	XPGM					
ELECTRONIC ENGINEERING TOOLS	ALLMAX/ALLMAX+ MEGAMAX					
ELAN	3000-145 5000-145 6000 APS			NOT QUALIFIED		
EQUINOX						
HI-LO SYSTEMS RESEARCH	All-03A All-07 All-11	V3.02	V3.02	V3.02		
ICE TECHNOLOGY LTD	Micromaster 1000/E Speedmaster 1000/E Micromaster LV Speedmaster LV LV40 Portable					
LEAP ELECTRONIC CO., LTD.	LEAPER-10 LP U4					
LINK	CLK-3100					
LOGICAL DEVICES	ALLPRO-40 ALLPRO-88 ALLPRO-88XR ALLPRO-96 Chipmaster 2000 Chipmaster 6000 XPRO-1	 Sept-97 V7.3.27	 Oct-97 Oct-97	 Sept-97 V7.3.27		
MICRPROSS	ROM 5000 B ROM 3000 U					
MINATO	M1881					
MQP ELECTRONICS	MODEL 200 SYSTEM 2000 PIN-MASTER 48					
NEEDHAM'S ELECTRONICS	EMP20					
OMC	Typro C Typro S					
Phyton	Multiprog					
Red Square	IQ-180 IQ-280 Uniwriter 40 Chipmaster 5000			NOT QUALIFIED		
SMS	EXPERT OPTIMA MULTISYTE SPRINT PLUS48	BBS BBS	BBS BBS	BBS BBS		
STAG	ECLIPSE QUASAR	V7.1.30	Sept-97	V7.1.30		
SUNRISE	T-10 UDP T-10 ULC		NOT QUALIFIED			
SUNSHINE	POWER-100 EXPRO-60/80					
SYSTEM GENERAL	TURPRO-1 TURPRO-1 FX TURPRO-1 TX APRO MULTI-APRO	Sept-97 Sept-97 Sept-97	Sept-97 Sept-97 Sept-97	Sept-97 Sept-97 Sept-97		
TRIBAL MICROSYSTEMS	Flex-700 TUP-300 TUP-400	V3.02	V3.02	V3.02		
XELTEK	SUPERPRO SUPERPRO II SUPERPRO II/P	 2.4B 2.4B				
XILINX	HW-130	V4.00	V4.00	V4.00	V4.10	V4.10

XILINX ALLIANCE-EDA CONTACTS - AUGUST 1997

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Changes since last issue normally printed in color. ***There have been no changes since XCell 25.***
Inquiries about the Xilinx Alliance Program can be e-mailed to alliance@xilinx.com

XILINX ALLIANCECORE PARTNERS - AUGUST 1997

Additional information is available on WebLINX, starting at: http://www.xilinx.com/products/logicore/alliance/tblpart.htm

PARTNER NAME	PHONE	EMAIL/WEB URL	EXPERTISE
ARM Semiconductor (USA), Inc. 1095 E. Duane Ave., Suite 211 Sunnyvale, CA 94086 (USA)	Tel: 408-733-3344 Fax: 408-733-9922	armsemi@netcom.com www.armsemi.com	Microprocessors, microcontrollers, peripherals, communications
CAST, Inc. 24 White Birch Drive, Pomona, NY 10970 (USA)	Tel: 914-354-4945 Fax: 914-354-0325	info@cast-inc.com www.cast-inc.com	AM29xx peripherals, DSP
Comit Systems 1250 Oakmead Pkwy, Suite 210 Sunnyvale, CA 94088 (USA)	Tel: 408-988-2988 Fax: 408-988-2133	preeth@comit.com www.comit.com	Base functions, communications
CoreEL Microsystems 46750 Fremont Blvd #208 Fremont, CA 94538 (USA)	Tel: 510-770-2277 Fax: 510-770-2288	sales@coreel.com www.coreel.com	ATM, communications
Digital Objects 3550 Mowry Ave., Suite 101 Fremont, CA 94538 (USA)	Tel: 510-795-2212 Fax: 510-795-2219	sales@digitalobjects.com www.digitalobjects.com	CardBus
Eureka Technology 4962 El Camino Real, #108 Los Altos, CA 94022 (USA)	Tel: 415-960-3800 Fax: 415-960-3805	info@eurekatech.com	PCI, PowerPC peripherals
Integrated Silicon Systems, Ltd. 29 Chlorine Gardens Belfast, BT9 5DL (North. Ireland)	Tel: +44-1232-664664 Fax: +44-1232-669664	info@iss-dsp.com www.iss-dsp.com	DSP functions
Inventra/Mentor 1001 Ridder Park Drive, San Jose, CA 95131-2314 (USA)	Tel: 503-685-8000 Fax: 408-451-5690	www.mentorg.com/inventra	USB, PCI, DSP, telecom, microprocessor peripherals
Logic Innovations 6205 Lusk Boulevard San Diego, CA 92121 (USA)	Tel: 619-455-7200 Fax: 619-455-7273	fpga@logici.com www.logici.com	PCI, MPEG-2, ATM, communications
Memec Design Services 1819 S. Dobson Rd., Suite 203, Mesa, AZ 85202 (USA)	Tel: 602-491-4311 Fax: 602-491-4907	info@memecdesign.com www.memecdesign.com	Microprocessor peripherals, base functions, Xilinx design services
Mobile Media Research, Inc. 39675 Cedar Blvd., Suite 295A, Newark, CA 94560 (USA)	Tel: 510-657-4891 Fax: 510-657-4892	sales@mobmedres.com www.mobmedres.com	PCMCIA, CardBus
NMI Electronics, Ltd., Fountain House, Great Cornbow, Halesowen, West Midlands, B63 3BL (UK)	Tel: +44 121 585 5979 Fax: +44 121 585 5764	ip@nmi.co.uk www.nmi.co.uk	Design services and base-level functions for the XC9500
Phoenix Technologies/Virtual Chips 2107 N. First Street, Suite 100, San Jose, CA 95113 (USA)	Tel: 408-570-1000 Fax: 408-452-0952	virtualchips-info@phoenix.com www.phoenix.com	PCI, USB, CardBus, ATM
Rice Electronics PO Box 741 Florissant, MO 63032 (USA)	Tel: 314-838-2942 Fax: 314-838-2942	ricedsp@aol.com	DSP
SAND Microelectronics 3350 Scott Blvd., #24, Santa Clara, CA 95131 (USA)	Tel: 408-235-8600 Fax: 408-235-8601	sales@sandmicro.com www.sandmicro.com	PCI, USB
SICAN Microeletronics Corp. 400 Oyster Point Blvd., #512, So. San Francisco, CA 94080 (USA)	Tel: 650-871-1494 Fax: 650-871-1504	infor@sican-micro.com www.sican-micro.com	CAN bus, DSP, communications
Technology Rendezvous, Inc. 3160 De La Cruz Blvd., Suite 101, Santa Clara, CA 95054 (USA)	Tel: 408-556-0280 Fax: 408-556-0284	info@trinic.com www.trinic.com	FireWire
VAutomation 20 Trafalgar Square Suite 443 (4th Floor) Nashua, NH 03063 (USA)	Tel: 603-882-2282 Fax: 603-882-1587	sales@vautomation.com www.vautomation.com	Microprocessors, microcontrollers, communications

Xilinx Alliance-EDA Companies & Products - August 1997 - 1 of 2

Company Name	Product Name	Version	Function	3K/ 4K	XC 5200	CPLD 7K9K	Uni Lib	PLATFORMS PC	Sun	RS6000	HP7
Accolade Design Automation	Peak VHDL	3.2	Simulation	✓	✓			✓			
ACEO Technology, Inc.	Asyn	5.0	Synthesis	✓	✓		✓	✓	✓		✓
Acugen Software, Inc.	Sharpeye	2.63	Testability Analysis	✓	✓	7k		✓	✓		✓
	ATGEN	2.63	Automatic Test Generation	✓	✓	7k		✓	✓		✓
	AAF-SIM	2.63	Fault Simulation	✓	✓	7k		✓	✓		✓
	PROGBSDL	2.63	BSDL Customization	✓	✓	7k		✓	✓		✓
	TESTBSDL	2.63	Boundary Scan ATG	✓	✓	7k		✓	✓		✓
Aldec	Active-CAD	2.2	Schematic Entry, State Machine & HDL Editor, FPGA Synthesis & Simulation	✓	✓	✓	✓	✓			
ALPS LSI Technologies	Edway Design Systems		Synthesis/Simlulation	✓		✓		✓			
Aptix Corporation	System Explorer	3.1	System Emulation	✓	✓	✓			✓		✓
	ASIC Explorer	2.3	ASIC Emulation	4K	✓		✓				
Aster Ingenierie S.A.	XILLAS	4.2	LASAR model generation	✓		7k		✓	✓		✓
Auspy Development Co.	APS	1.2.3	Multi-FPGA Partitioning	✓	✓			✓	✓		
Cadence	Verilog	97A	Simulation	✓	✓	7k	✓		✓	✓	✓
	Concept	97A	Schematic Entry	✓		7k	✓		✓	✓	✓
	FPGA Designer	97A	Topdown FPGA Synthesis	✓	✓	7k	✓		✓	✓	✓
	Synergy	97A	FPGA Synthesis	✓	✓	7k	✓		✓	✓	✓
	Composer	97A	Schematic Entry	✓		7k	✓		✓	✓	✓
Capilano Computing	Design Works	3.1	Schematic Entry/Sim	✓			✓	✓			
Chronology Corporation	TimingDesigner	3.0	Timing Specification and Analysis	✓	✓	✓	✓	✓	✓		✓
	QuickBench	1.0	Visual Test Bench Generator	✓	✓	✓	✓	✓	✓		✓
CINA-Computer Integrated Network Analysis	SmartViewer	1.0e	Schematic Generation	✓		7k		✓			
Compass Design Automation	ASIC Navigator		Schematic Entry	✓	✓	7k			✓		✓
	X-Syn		Synthesis	✓					✓		✓
	QSim		Simulation	✓	✓	7k			✓		✓
Epsilon Design Systems	Logic Compressor		Synthesis optimization	✓	✓			✓			
Escalade	DesignBook	2.0	Design Entry	✓			✓	✓	✓		
Exemplar Logic	Galileo	4.1	Synthesis/Timing Analysis/Simulation	✓	✓	✓	✓	✓	✓		✓
	Leonardo	4.0.3	Synthesis/Timing Analysis/Simulation	✓	✓	✓	✓	✓	✓		✓
Flynn Systems	Probe	3.0	Testability Analysis	✓	✓	7k		✓			
	FS-ATG	3.0	Test Vector Generation	✓	✓	7k		✓			
	CKTSIM	3.0	Logic Analysis	✓	✓	7k		✓			
	FS-SIM	3.0	Simulation	✓	✓	7k		✓			
Fujitsu LSI	PROVERD		Top-Down Design System	✓				✓			
Harmonix Corporation	PARTHENON	2.3	Synthesis	4k		7k		✓	✓		
IK Technology Co.	Ishizue Professionals	1.06	Schematic Entry/Simulation	✓				✓	✓		✓
IKOS Systems	Voyager	2.31	Simulation	✓	✓				✓		✓
	Gemini	1.21	Simulation	✓	✓				✓		✓
INCASES Engineering GmbH	Theda	5.0	Design Entry	✓				✓	✓	✓	✓
ISDATA	LOG/iC2	5.0	Synthesis Simulation	✓	✓	✓	✓	✓			
Logic Modeling Corp. (Synopsis Division)	Smart Model		Simulation Models	✓	✓	✓		✓	✓	✓	✓
	LM1200		Hardware Modeler	✓		✓		✓	✓	✓	
Logical Devices	Total Designer	4.7	Simulation & Synthesis	✓	✓	✓	✓	✓			
	Ulysa	1.0	VHDL Synthesis	✓	✓	✓	✓	✓			

Items that have changed since the last issue (XCell 25) are in color.

Xilinx Alliance-EDA Companies & Products - August 1997 - 2 of 2

Company Name	Product Name	Version	Function	3K/ 4K	XC 5200	CPLD 7K9K	Uni Lib	PLATFORMS PC	Sun	RS6000	HP7
Mentor Graphics	Design Architect	B.x	Schematic Entry	✓	✓	✓	✓		✓	✓	✓
	Galileo	4.1	Synthesis/Timing Analysis	✓	✓	✓	✓		✓	✓	✓
	Leonardo	4.0.3	Synthesis/Timing Analysis	✓	✓	✓	✓		✓	✓	✓
	QuickSim II	B.x	Simulation	✓	✓	✓	✓		✓	✓	✓
	QuickHDL	B.x	HDL Simulation	✓	✓	✓	✓		✓	✓	✓
MicroSim	MicroSim Design Lab		Schematic Entry, Mixed A/D & FPGA Simulation, PCB Layout and Routing	✓	✓		✓	✓			
MINC	PLDesigner-XL/PL-Synthesizer	3.3/3.2.2	Synthesis	✓				✓	✓		✓
Model Technology	V-System/VHDL	4.6G+	Simulation	✓		✓	✓	✓	✓	✓	✓
OrCAD	OrCAD Express	7.0	Schematic Entry, VHDL, Mixed-mode Entry, Simulation, Synthesis, Brd Design	✓	✓	✓	✓	✓			
Protel Technology	Advanced Schematic	3.2	Schematic Entry	✓	✓	7k	✓	✓			
	Advanced PLD	3	PLD/FPGA Design & Simulation	✓	✓	7k		✓			
Quad Design Technology	Motive	4.3	Timing Analysis	✓				✓	✓	✓	✓
SimuCad	Silos III	96.1	Schematic Entry & Simulation	✓	✓		✓	✓			
Sophia Sys & Tech	Vanguard	5.31	Schematic Entry	✓		✓		✓	✓		✓
Summit Design Corp.	Visual HDL	3.0	Graphical Design Entry/ Simulation/Debug	✓	✓	✓	✓	✓	✓	✓	✓
Synario Design Automation	ABEL	6.3	Synthesis, Simulation			✓	✓	✓			
	Synario	2.3	Schematic Entry, Synthesis & Simulation	✓	✓	✓	✓	✓			
Synopsys	FPGA Express	1.2	Synthesis	✓	✓	TBD		✓			
	FPGA Compiler	3.4b+	Synthesis	✓	✓	✓	✓		✓	✓	✓
	Design Compiler	3.4b+	Synthesis	✓	✓	✓	✓		✓	✓	✓
	VSS	3.4b+	Simulation	✓	✓	✓	✓		✓	✓	✓
Synplicity, Inc.	Synplify-Lite	3.0	Synthesis	✓	✓	✓	✓	✓	✓		✓
	Synplify	3.0	Synthesis	✓	✓	✓	✓	✓	✓		✓
	HDL Analyze	3.0	Schematic	✓	✓	✓	✓	✓	✓		✓
TopDown Design Solutions	info to come										
Trans EDA Limited	TransPRO	1.2	Synthesis	✓					✓		✓
VEDA Design Automation Inc	Vulcan	4.5	Simulation	✓					✓		✓
Veribest	Veribest VHDL	14.0	Schematic Entry	✓			✓	✓	✓		✓
	Veribest Verilog	14.0	Simulation	✓			✓	✓	✓		✓
	VeriBest Simulator	14.0	Simulation	✓	✓		✓	✓	✓		✓
	DMM	14.x	Design Management	✓	✓		✓	✓	✓		✓
	VeriBest Synthesis	14.0	Synthesis	✓	✓		✓	✓	✓		✓
	Synovation	12.2	Synthesis	✓			✓	✓	✓		✓
	PLDSyn	12.0	Design Entry Synthesis	✓		7k		✓	✓		✓
	VerBest Design Capture	14.x	Design Capture	✓	✓		✓	✓	✓		✓
Viewlogic	WorkView Office	7.1.2/7.2	Schem/Sim/Synth	✓	✓	✓	✓	✓			
	ProSynthesis	5.02	Synthesis	✓		7k	✓	✓	✓	✓	✓
	ProSim	6.1	Simulation, Timing Analysis	✓		7k	✓	✓	✓	✓	✓
	ProCapture	6.1	Schematic Entry	✓		7k	✓	✓	✓	✓	✓
	PowerView	6.0	Schem/Sim/Synth/Timing Analysis	✓	✓	✓	✓		✓	✓	✓
Visual Software Solutions	Statecad	3.0	Grph. Design Entry, Sim., Debug	✓	✓	✓	✓	✓	✓		✓
Zuken	Tsutsuji		Synthesis/Simulation	✓					✓	✓	✓
Zycad	Paradigm RP		Rapid Prototyping	✓					✓		✓
	Paradigm XP		Gate-level Sim	✓					✓		✓

Items that have changed since the last issue (XCell 25) are in color.

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