Issue 39
Spring 2001

# Xcell journal

THE AUTHORITATIVE JOURNAL FOR PROGRAMMABLE LOGIC USERS



## Cover Story

Mentor Graphics' VP and Gen. Mgr. Anne Sanquini Discusses the FPGA as System-on-Chip

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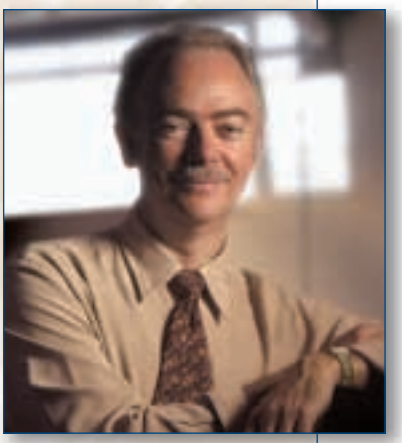
# Win a Handspring™ Visor PDA and Help Us Improve Xcell





Xcell journal

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I need your help. This journal intends to bring you the best possible information about the latest technology from Xilinx and its partners; it is written for you and it has no other purpose than to help make your job easier – so your feedback is very important to our success. I'm asking for just a few minutes of your time, to tell us what you like and don't like about the Xcell Journal, and in return you could win a Handspring™ Visor Personal Digital Assistant.

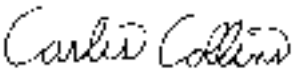
To simplify the survey process and make it as quick and easy as possible, we've created a website where you can provide your suggestions and comments, and give us the specific information we need to better serve you. Each month, for as long as the survey is active, we will pick one winner, at random, from all of the survey entries that month.

Our industry is changing rapidly; there are many new advances in silicon, software, and services that you must understand if you are to remain competitive. We intend for Xcell to be one of your best ways to stay informed, and with your help, we will continue to improve Xcell and continue bringing you the information you want and need most.

Please visit the Xcell Survey website and complete the brief online questionnaire. Your feedback will help Xcell to remain a winner, and you could be a winner too.

**You'll find the survey at: www.ifulcrum.com/apps/survey/xilinx/journal/**

Thanks in advance for your help.



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Editor in Chief

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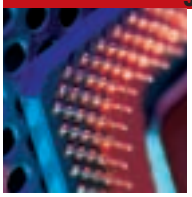

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View
from the top

# FPGAs Are Changing the Consumer Marketplace

Our latest, low cost, high performance FPGAs are ideal for high volume, dynamically changing, consumer applications such as home networking.

by Wim Roelandts, CEO, Xilinx

The market for all types of electronic consumer products is growing constantly and changing rapidly. New products are being developed faster than ever before to meet the demands of consumers, while new standards quickly obsolete yesterday's innovations. Now, more than ever before, companies must adapt quickly to a changing marketplace and bring new innovations to consumers at an ever increasing rate. To remain competitive, many consumer-oriented companies now recognize the enormous benefits of programmable logic for accelerating their time to market and increasing the life span of their products.

### Programmable Logic Thrives on Change

Xilinx technology is gaining momentum in the consumer marketplace because programmable logic devices (PLDs) are ideal in applications where standards are constantly changing. By designing with PLDs, companies can quickly make last minute design changes, keep new products on schedule, and evolve along with the current standards. In addition, our FPGAs now have advanced features, high performance, and low prices – all essentials needed to meet the requirements for high volume consumer designs. For example, our FPGAs now operate with clock rates exceeding 800Mbps, with huge gate capacities, 800MHz I/O capability, delay-locked loop clock management, and many other advanced features – and you can purchase a 100K gate Spartan-II device for less than $10.

With programmable logic, you can begin your system design long before your full design specification is finalized. Then, even after your product is in your customers' hands, you can make changes as needed to keep your product in the market longer. For example, using our Internet Reconfigurable Logic™ (IRL) capability, you can change your hardware design, in the field, over the Internet. You can add features, fix bugs, or adapt to new standards without replacing your hardware. The possibilities of this technology are enormous. Companies that use this capability will have a significant advantage over their competition, because they can reduce costs, offer unique features, and provide better service.

### Innovation Is the Key

The consumer marketplace requires low cost, high volume devices, and in the past, ASICs were the best choice for consumer-oriented designs. However, the price, performance, and features of our latest generation Spartan-II FPGAs are now competitive with ASICs, and our FPGAs bring the added benefits of fast development, lower up-front costs (no NRE charges), reprogrammability, remote field upgradability, and off-the shelf delivery – all significant advantages in today's fast-paced marketplace. Our technology innovations have opened the consumer marketplace to programmable logic.

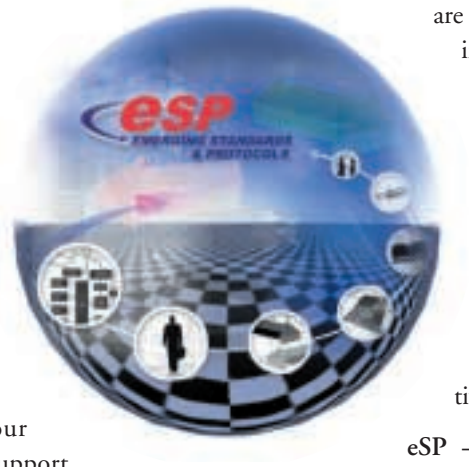
The developers of consumer products have not been our usual customers, however, so many are not aware of the most recent advances that are fundamentally changing the industry. Therefore, we must be innovative in our approach to find and support these developers, and help them to understand and use our solutions.

To meet the challenge of supporting consumer-oriented designers, we have taken bold steps to provide unique and valuable services, over and above our core technologies. To focus our efforts, and to be most effective, we have targeted the key consumer markets where we can be of most benefit.

### Home Networking

One key market is home networking – a huge emerging market where many different standards are competing for dominance. In the near future, a wide assortment of intelligent appliances and systems for the home will all need to work together through some sort of network. To manage your household, your computer will need to interface with your refrigerator, your entertainment center, your alarm system, your environmental controls, and other devices, some not even invented yet. Long before these futuristic applications become commonplace, you will need an efficient way to connect all of the computers and peripherals you already own – many households today have three or more computers, with various peripherals, spread throughout the home.

It's easy to build a network infrastructure (wiring) into a new home. But, for the vast majority of existing homes, the dedicated wiring is not already in place. That's why there are many competing networking methods: power lines, phone lines, radio/wireless, and infrared are all possible networking media that do not require dedicated wiring. Each of these possibilities represents a new standard you must be aware of if you intend to compete in this dynamic and lucrative marketplace.




**eSP – Emerging Standards and Protocols**

Because the home networking marketplace is still very young, and somewhat chaotic, we found that we could be a great benefit to you by creating a clearinghouse for the latest networking information – the Xilinx eSP Web portal. We are already actively involved in all of the key standards-making committees, and we continue to develop easy-to-use networking reference designs, so we decided to share what we know with you – to save you time and effort, to keep you informed about all of the important standards, and to help you make the best possible choices.

The Xilinx eSP Web portal provides you with comprehensive solutions to accelerate

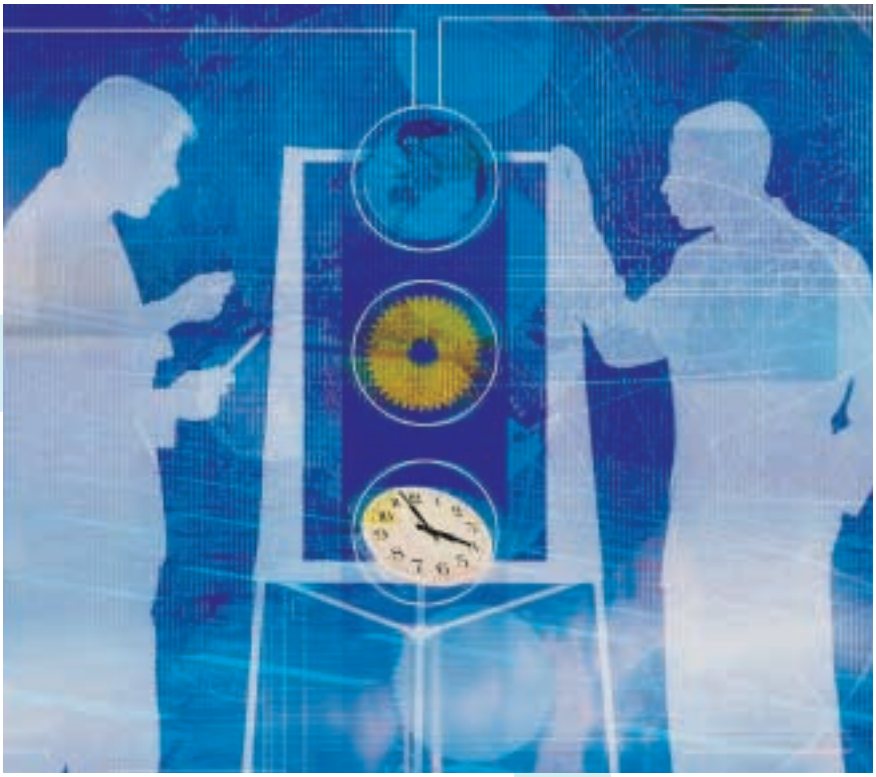
the development of your products based upon emerging standards and protocols. At our eSP website, you'll find:

- **Updates to industry standards and protocols** – Keeping you well informed as the standards continue to evolve.
- **Reference Designs** – Saving you the risk and effort of creating new designs by giving you system solutions that fully comply with the latest standards and protocols, while maintaining flexibility for easily upgrading to the next generation standards.
- **System Block Diagrams** – Giving you a head start with detailed solutions and system block diagrams for home networking technologies.
- **Standards Tutorials and Reference Materials** – Explaining how the different technologies work together to create a home networking environment.
- **Application Notes and White Papers** – Providing detailed information on how to efficiently use specific technologies.
- **A forum for discussing home networking technologies** – Offering you fast and accurate answers from the most qualified experts.
- **Strategic Alliances** – Giving you access to our partners, including ASSP vendors, mixed-signal solution providers, intellectual property providers, software providers, design services providers, memory vendors, processor vendors, and others.

### Home Networking Trade Shows

In a further effort to help you understand the dynamics of the home networking marketplace, we recently organized a trade show and invited industry experts to discuss the relevant issues. The show (held in Santa Clara California, in February, 2001) was a big success.

Xilinx is in a unique position to promote and educate the home networking marketplace; we are unbiased, because our technology supports all the emerging standards. By bringing people together, and freely distributing relevant information, we intend to provide you with a key service in addition to our technology.



### The Xilinx Difference

Innovation is the lifeblood of Xilinx, and we make great efforts to create an atmosphere where innovation is nurtured and rewarded. This is a key reason why Xilinx is a worthy partner in your design efforts. We are innovative at every level of the company, and our overall effectiveness is constantly improving. I believe one good idea is worth more than thousands of hours of hard work.

By definition, innovation is change – and people don't like change. It is usually risky, and always influenced by unknown factors. So, to be innovative, we must overcome the fear of change and minimize the risks of stepping outside our normal boundaries. At Xilinx, we do this by creating a supportive environment where failure is accepted and expected as a necessary part of any creative effort. We encourage all our employees to be creative in their jobs, not just the engineers who are developing unique new technologies. Innovation at every level of Xilinx has a profound impact on you, because we are always striving for excellence in everything we do.

Xilinx was ranked number 14 out of the Fortune 100 Best Companies to Work for in America. Our attrition rate is about one third of that for other companies here in Silicon Valley, which indicates that Xilinx is a company that cares about people. Our culture makes Xilinx not only a great place to work, it also makes Xilinx a great company to work with.

### Conclusion

Xilinx is dedicated to providing the products and services you need to be competitive in the consumer marketplace. Working with us is the fastest and easiest way to get your new product to market ahead of your competition.

Within the next 10 years, you will find programmable logic devices used in almost every piece of electronic equipment. The advantages of programmable logic are overwhelming, and they increase dramatically with each new generation. Decreasing costs, increasing performance, unique new features, and design flexibility – combined with fast and efficient development tools – give you compelling reasons to use programmable logic for all your designs.

# Xilinx eSP Initiative Will Accelerate Time-to-Market for Consumer Products


## Xilinx debuts a Web portal for emerging standards and protocols for consumer products and services.

by Amy Hills
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As the pace of market change continues to accelerate, design cycles continue to shrink. If you are a designer of high tech consumer products, you are probably finding yourself compelled to develop products based upon emerging standards and protocols. By their very nature, emerging standards and protocols are moving targets. Until now, you've had few resources you could rely on to assist you in accelerating your just-in-time-to-market products while they are still compliant with the latest standards and protocols.

Now, however, Xilinx presents the eSP (emerging Standards and Protocols) Initiative™ — a powerful array of comprehensive tools and solutions for consumer product manufacturers and vendors. The centerpiece of this initiative is the eSP website — www.xilinx.com/esp/. The eSP site serves as a total portal for tracking, learning, and acquiring the resources necessary to succeed in today's fast-evolving market.

"The eSP Initiative underscores our commitment to provide solutions that deliver time-to-market advantage, while reducing risk," said Wim Roelandts, Xilinx president and CEO. "Traditional FPGA customers will benefit from the eSP Initiative, but we also expect a broader community, specifically ASIC designers and system architects, to benefit as well."

The initial focus of the eSP site will be on home networking, a market in which designers face significant challenges as they work with complex and conflicting standards. (For an in-depth analysis of the home networking market, see "FPGA-Enabled Home Networking Bridges Isolated Islands of Technology" in this issue of *Xcell Journal*.) The first home networking technology to get the Xilinx eSP treatment will be the standards and protocols of Bluetooth™, a popular wireless home networking system for cellular phones, PDAs, and notebook PCs.

### Simplifying Complex and Conflicting Standards

In order to design products based upon emerging standards and protocols, you must make a significant investment in both time and resources to review and understand complex specifications (exceeding 1,000 pages is not uncommon). To remain current on these changes, designers are often required to attend conferences, seminars, and meetings, frequently necessitating extensive travel and downtime.

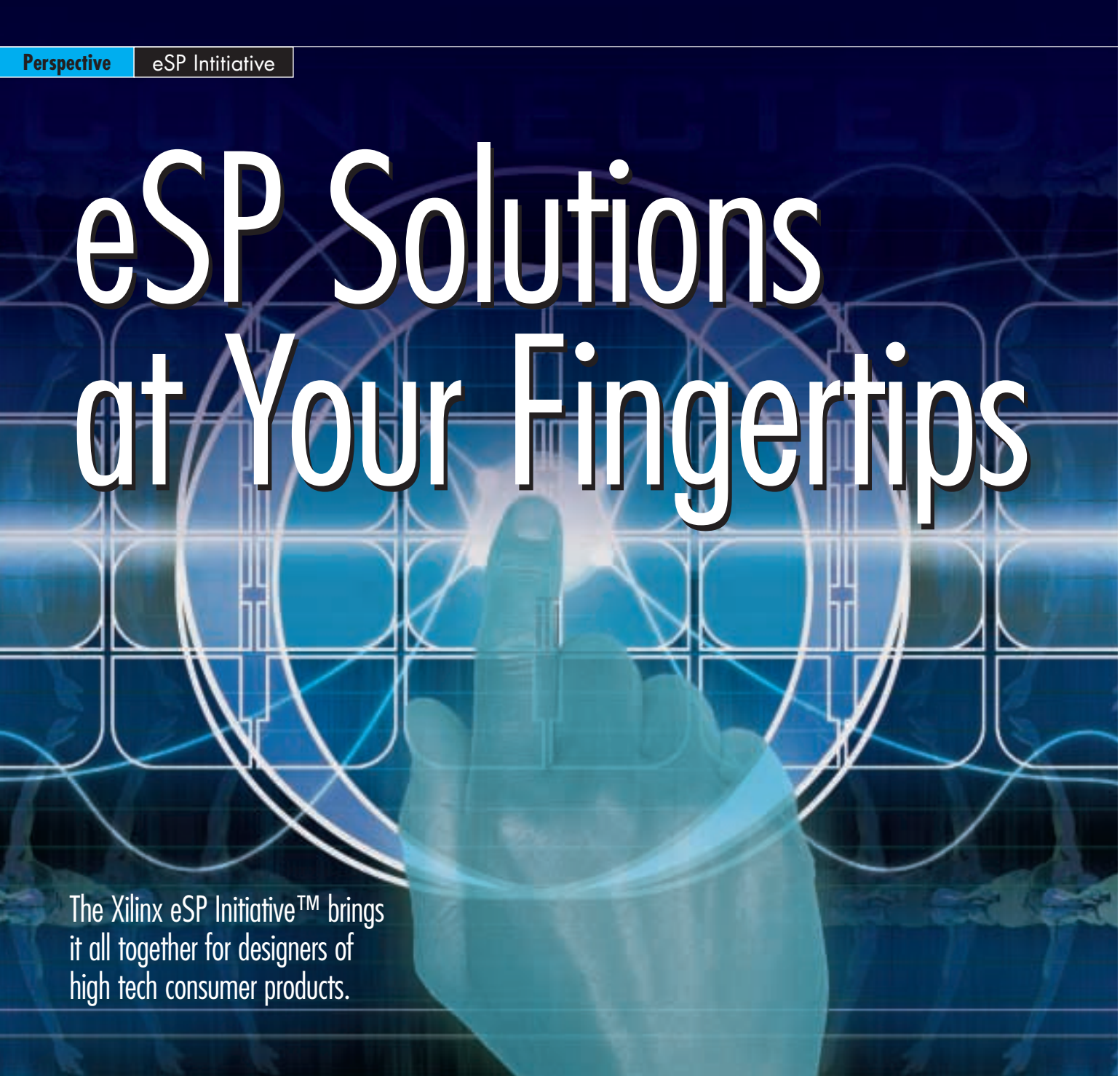
Without this investment in time and resources, however, a company runs the risk of building noncompliant products. "In the consumer market, it's quite clear that being first to market isn't a luxury, it's a necessity. Yet, while getting a product to market rapidly is important, if it's not compliant with the latest standard, it could very well be obsolete at introduction," said Robert Bielby, director of strategic applications at Xilinx.

Through the eSP website, you have access to a wide range of solutions, all of which can assist you to accelerate your time-to-market. For the first time, you have a single location where you can find everything that you need. The site includes the following major components:

- Reference designs
- Ask the Experts discussion forum
- Tutorials
- White papers
- Application notes
- Updates and changes to standards and protocols
- Block diagrams
- Directory of consultants
- Intellectual property cores
- Industry links
- Glossary
- Applicable Xilinx solutions.

As the flagship component of the eSP Initiative, the eSP website is a comprehensive, one-stop resource. To learn more about what the eSP website can do for you, see the article "eSP Solutions at Your Fingertips" on page 8 of this issue.

# eSP Solutions at Your Fingertips



The Xilinx eSP Initiative™ brings it all together for designers of high tech consumer products.

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The digitization of consumer products has greatly accelerated the rate at which products and standards become obsolete. For manufacturers of consumer products, being able to quickly design and deliver a product to market – and keep it there – can have a direct impact on their ability to survive.

Moreover, consumer manufacturers must be able to design a product that can operate with multiple standards, and maintain the ability to rapidly upgrade to new standards or add new features. The ability to be interoperable and upgradeable will prove critical for manufacturers to either increase market share or simply maintain market share. For example, cellular phone manufacturers that offer one cellular phone to meet the different standards all across the globe have been able to gain market share.

Because time to market is of the essence, Xilinx has launched the eSP Initiative – a Web-based project to collect, share, discuss, track, and develop programmable logic system solutions to comply with emerging standards and protocols (eSP). Key to the eSP Inititative are Xilinx IP (Intellectual Property) cores and Spartan-II™ FPGAs (Field Programmable Gate Arrays).

### The Absolute Need for Programmable Solutions

As digital convergence becomes reality instead of theory, programmable logic solu-

tions become a necessity instead of an alternative. This is why:

### Multiple Standards

Typically, there is not just one single alternative (or standard) available to address any given design challenge. Rather, there are several emerging standards and protocols. This introduces tremendous risk for manufacturers in selecting a solution, because not every contender will succeed in the long term. Programmable logic solutions are not exempt from this risk, but they are far better positioned to convert and adapt should the chosen architecture falter.

### Complexity

The scope and complexity of these emerging technologies are immense – and, their specifications are correspondingly large, not to mention being subject to ambiguity and error. Further, they are, by definition, new and to some extent unproven. This often mandates a chaotic development cycle where the implementation is cycled through numerous prototype, test, and debug iterations before it becomes stable. The versatility of reprogrammable logic is virtually the only way to effect such rapid design changes efficiently and quickly.

### Rapid Specification Changes

Emerging standards are seldom static. They are often updated on an irregular basis. And, as much as designers may try to maintain transparent backward compatibility, this cannot be guaranteed. Reprogrammable logic solutions are virtually the only platform that can perform rapid response to specification changes.

### Shrinking Product Development Cycles

ASICs and ASSPs cannot react fast enough to keep up with the changing of consumer market requirements. Short product life cycles do not make designing ASICs a cost-effective proposition. To achieve maximum success in the marketplace, manufacturers must be able to send upgraded, updated products to market early. There is no superior alternative to designing with reprogrammable logic to get your product to market on time.

Changing standards, multiple standards, and rapidly evolving features make programmable logic the natural fit for the consumer world. The prices offered by Spartan-II™ FPGAs from Xilinx are perfect for this cost-sensitive and quickly evolving market.


*Figure 1 - eSP program details*

## Introducing eSP – Extending the Traditional Value of FPGAs

The digitization and convergence of consumer and communications technologies are driving new products based on emerging standards and protocols. The consumers' desire to gain faster and easier access to the Internet – and from anywhere – is already leading to new standards such as:

- Wireless communications standards like IEEE 802.11, HomeRF™, and Bluetooth™
- Serial digital communications standards like IEEE 1394 (FireWire) and USB 2.0
- Streaming communications technologies for Internet audio and video content distribution
- Interactive conferencing
- And more.

All of this technology is progressing very quickly, placing extraordinary challenges and pressures on new product development.

Another challenge in deploying products for emerging standards is simply finding the appropriate resources. Because many of these technologies are so new, there is no critical mass of talent, IP cores, and tools to draw upon. Further, what resources are available are most likely decentralized and diffused. This all magnifies the challenge of developing a product using these technologies in a timely and efficient manner.

The Xilinx eSP Initiative is a program designed and tailored to address the issues. It is targeted at system architects and ASIC/FPGA designers with the intent to:

- Help them understand these technologies.
- Promote the benefits of programmable solutions and deploy them.
- Provide support resources for Xilinx-based solutions.

Figure 1 illustrates how the eSP program will help manufacturers further accelerate the time to market for emerging standards and protocols. The traditional time-to-product advantage of FPGAs is well known. Where the eSP Initiative kicks in is with tools and resources to help accelerate the time-to-learn and time-to-design components of product development.

### eSP Overview

The Xilinx eSP Initiative is the industry's first Web portal dedicated solely to addressing the challenges of developing products contingent upon emerging standards and protocols. Simply put, eSP delivers complete suites of solutions to accelerate product development time in the face of emerging standards and protocols.

### Standards Tutorials

eSP tutorials give designers a high level of the various specifications, and help them understand the complexities associated with each specification. The tutorials are carefully crafted to contain enough detail to inform – but not overwhelm – designers.

The material also addresses to a wide audience ranging from the curious hobbyist to the serious system architect. As an example, every major aspect of the home networking market segment is covered by more than 2,600 carefully documented pages. The topics covered include:

- Market research
- Overview of various technical specifications
- Hurdles faced by designers
- Projections on the future
- System block diagrams
- Industry links
- FAQs
- Detailed glossary.

It's all available directly through the Internet at www.xilinx.com/esp/.

### Keeping Current on Changes

Another key feature of the eSP Initiative is to allow you to learn about the changes to standards and protocols when they happen – and to help you understand how they impact your product design. Truly, eSP is a one-stop shop to get an update on all the specifications related to a specific consumer market segment.

### Ask the Experts

Xilinx has put together a panel of experts to answer your most pressing questions. Each market segment explored and discussed under the eSP Initiative has its own discussion forum. Staffed by some of the industry's leading experts, these forums have the answers to the toughest design challenge questions.

As an example, the home networking effort has more than 10 experts on the panel who have a very strong understanding of the home networking industry.

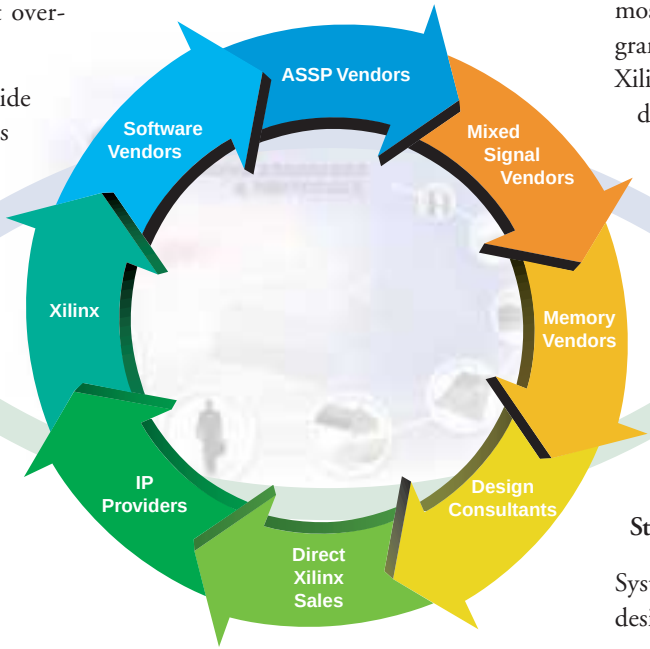


*Figure 2 - The Xilinx Ecosystem*

### Application Notes, White Papers, and Glossary

Whether you need to learn more about a standard or protocol, or you are simply trying to figure out what a term means, eSP can help. You are likely to find an application note or white paper on the very topic you're looking for. The eSP website contains up-to-date application notes and white papers, as well as current market and technical analyses. The website also hosts a glossary of more than 1,000 terms, many of them as new as the emerging standards and protocols they describe.

### System Block Diagrams

If you're trying to figure out the best way to build your next product, simply peruse the system block diagram pages. The eSP website has an extensive set of system block diagrams. The home networking market segment offers more than 60 block diagrams that cover broadband access devices, residential gateways, home networking technologies, and information appliances.

### Intellectual Property

Xilinx is the first programmable logic company to embrace the concept of cores for FPGAs through the LogiCORE™ program. Today, LogiCORE products form the most successful core program in the programmable logic industry. As a result, Xilinx has gained considerable experience developing and selling cores, and servicing FPGA core customers.

The AllianceCORE™ program is a cooperative effort between Xilinx and independent third-party core developers to expand and share the availability of the highest quality cores for use in Xilinx programmable logic devices. Today, Xilinx offers more than 60 different IP cores, which can be accessed from www.xilinx.com/ipcenter/.

### Strategic Alliances – The Ecosystem Era

System designers face many obstacles to designing consumer products in an environment where standards continue to evolve. This makes the selection of critical system components extremely challenging. Therefore, Xilinx has introduced the eSP Ecosystem™ – a new approach to creating complete cutting-edge systems solutions that offer you a sustainable competitive advantage. The eSP Ecosystem consists of Xilinx and industry partners striving jointly to provide complete system solutions to enhance productivity. Of course, the solutions will comply with the relevant emerging standards and protocols. Because this is an integral part of the eSP Initiative, the ecosystem is committed to providing an update path to future standards and protocols. An example of a typical eSP ecosystem is shown in Figure 2.

**Home Networking –**
**An Ecosystem Example**

The home networking market provides a great example of how effective the eSP Ecosystem can be. There are many home networking standards, which are currently evolving, for example, IEEE 1394a to IEEE 1394b, HomeRF™, HomePNA™, HomePNA 2.0, and HomePlug™, among others.

Let's take an example of a residential gateway. To design a successful residential gateway, a manufacturer must decipher and comprehend complex standards. There are many decision points:

- Should the residential gateway support:
  - Cable modems?
  - xDSL modems?
  - Satellite modems?
  - Wireless modems?
- What home networking technology should the gateway support:
  - IEEE 1394a?
  - IEEE 1394b?
  - HomePNA?
  - HomePlug?
  - IEEE 802.11b?
  - HomeRF,
  - Bluetooth?
  - WirelessLAN?
  - USB 1.1?
  - USB 2.0?
  - Ethernet?
  - FOLS (Fiber Optics LAN Section of the Telecommunications Industry Association).

To make the problem more complex, the technology required for each solution is typically available from more than one vendor. And one vendor's solution is not always optimized to interface with another vendor.

Xilinx and the eSP Ecosystem are the solution to the problem. The ecosystem involves strategic alliances with industry leaders to jointly provide a proven residential gateway design that meets and conforms to all of the industry standards. Moreover, the very nature of programmable logic, allows the eSP Ecosystem to construct the residential gateway so that it can be upgraded in the field to support fast implementation of changing standards. Of course, the eSP Ecosystem also works very closely to insure that all solutions provide transparent interoperability.

However, the solution doesn't stop there. The eSP Ecosystem is also committed to providing all the necessary support, whether it is hardware or software. You can use the proven design as is, or make any modifications for product differentiation by utilizing the "spare programmable logic gates" or by using vertical migration (a method of using higher density programmable logic devices in the same package, without changing the pinout).

The real advantage of the eSP Ecosystem, is that every member of the ecosystem benefits. Each ecosystem member also gains expanded market coverage, because all ecosystem members will promote proven designs through their own sales and marketing channels.

**Reference Designs – Tying It All Together**

As part of the eSP Initiative, Xilinx has partnered with a wide range of industry experts, application specific standard product manufacturers, and intellectual property providers to develop, deliver, and support hardware reference designs for specific emerging standards. These reference designs will accelerate product development while addressing the flexibility and price constraints of the targeted end application.

These are not just reference designs, however. They are complete system solutions designed to conform to all of the necessary standards and protocols.

The reference designs are tested to comply with industry consortia specifications as well as the relevant standards bodies. These system solutions contain everything necessary to build the final product (except the cover). The reference designs include:

- Bill of materials
- Gerber files
- Software
- Software drivers
- Hardware
- VHDL or Verilog code
- Programming software
- Design tools
- IP cores
- Datasheets
- Schematics
- Applications notes
- License agreements.

Because the system solutions are based upon the low-cost Spartan-II™ FPGA family, the reference design can be easily customized for product differentiation or to add extra features.

**eSP – Solutions at Your Fingertips**

The eSP Initiative extends the traditional benefits of flexibility and time-to-market offered by FPGAs. Moreover, the initiative helps with the learning and design phases of product development. The eSP Initiative provides revolutionary solutions for products dependent on emerging standards and protocols. Because eSP takes the guesswork out of understanding these standards, you can focus on the important matters like product marketing. You'll find everything you need to get ahead and stay ahead of emerging standards and protocols at www.xilinx.com/esp/.

# FPGA-Enabled Home Networking Bridges Isolated Islands of Technology

## Field programmable gate arrays show great promise to interconnect disparate home networking systems.

by Amit Dhir
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Chaos reigns in the home networking marketplace. Too many conflicting technologies and standards are competing to gain preeminence in home networking. Moreover, these technologies and standards are constantly evolving to add more functionality, to fix bugs, and to interface with as many competing standards and technologies as possible. The fierce competition inevitably leads to a counterproductive development model. Although a product should be planned for the longest possible life cycle, this tenet is often overridden by pressure to get the product to market as fast as possible.

As a consequence, technology leaders must proactively participate in multiple consortia and standards committees to keep track of the market. Until the market stabilizes under a single standard, leading technology players must support several, if not all, possible standards.

Conflicting specifications and the lack of a clear direction for future technology have created a pressing demand for home network bridges that can interconnect the various information appliances found in the modern home. As we will show, Xilinx Spartan-II™ field programmable gate arrays are the logical choice to form the infrastructure of these bridges now and in the future.

### An Introduction to Home Networking

Home networking involves the distribution of audio, video, and data around the home.

| | Market Requirements | Solutions Available |
|---|---|---|
| **Broadband Access** | High speed access for data, voice, and video; always on; simultaneous uplink & downlink communication; support simultaneous and multi-user access | xDSL, cable, ISDN, powerline, satellite, mobile/wireless |
| **Residential Gateway or Home Gateway or Services Gateway** | Provides access into the home; remote management access platform; bridging between different networks; firewall and security; e-services capabilities | Open System Gateway initiative(OSGi)<br>Jini™<br>UPnP (Universal Plug and Play)<br>HAVi (Home Audio-Video interoperability) standard |
| **Information Appliances** | Digital electronics with advanced computational capabilities add more value and convenience when networked. | Digital TV/HDTV, set-top boxes, Internet screen phones, digital VCRs, gaming consoles, MP3 players, cordless phones, security systems, utility meters, PCs, Web pads, Web terminals, PDAs, digital cameras, auto PCs, etc. |
| **Home Networking Technologies** | Low cost; speed; mobility; quality of service (QoS); security; reliability; ubiquity; ease of use | No new wires: phonelines, powerlines<br>New wires: Ethernet, IEEE 1394/FireWire, USB 2.0<br>Wireless: HomeRF, Bluetooth, wireless LANs (IEEE 802.11, HiperLAN2) |

*Table 1 - Aspects of home networking*

In a perfect world, home networking ensures interoperability among various information appliances in your home. At present, however, home networking represents a collection of more than 20 end technologies.

As shown in Table 1, home networking has four aspects:

- Broadband access
- Residential gateways
- Information appliances
- Home networking technologies.

No one technology dominates the home networking arena. Therefore, different technologies must co-exist without being able to communicate with one another. For example:

- Bluetooth™ networks mobile devices such as cellular phones, PDAs, and notebook PCs.
- USB/USB 2.0 networks PC-centric devices such as desktop PCs, printers, and scanners.
- FireWire™ networks digital TVs, set-top boxes, gaming consoles, and other bandwidth-heavy entertainment appliances.

These co-existing, disparate technologies are like islands in need of bridges to connect them.

## Islands of Home Networking Technologies

As illustrated in Figure 1, three technological islands, each with their own market niches, exist in the home networking environment:

### No New Wires

The "no new wires" technology utilizes the existing infrastructure available in most homes across the world. The technology utilizes existing powerlines and phonelines. The advantage of using no new wires is that consumers do not need to rewire their homes. Furthermore, products based on this technology can be cost-effectively deployed immediately.

The two power players on the no new wires island are HomePNA (Phone Networking Alliance) and PowerPlug™ Power Alliance. The ability, however, to handle high-speed video and other high bandwidth applications under a noisy electromagnetic environment is a formidable obstacle to overcome.

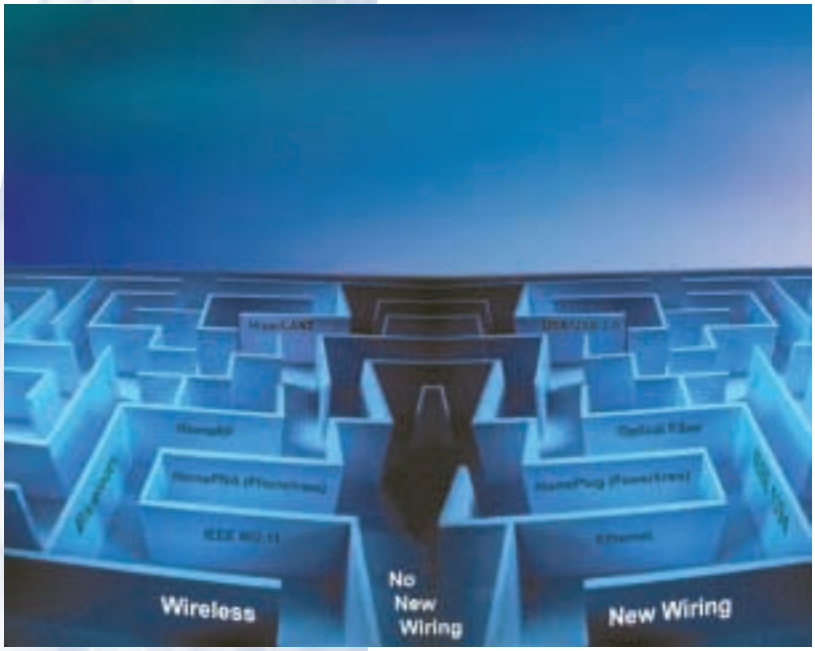


*Figure 1 - Disparate islands of home networking technologies*

### New Wires

Consumer devices that require high-speed data and video packets use Ethernet (IEEE 802.3), FireWire (IEEE 1394), optical fiber, or USB 2.0 (Universal Serial Bus) technologies. The downside of all of these technologies, is that they require additional special wiring around the house. Although it is relatively inexpensive to include network wiring in new home construction, retrofitting existing homes with network wiring can be quite expensive.

### Wireless

Wireless technologies such as Bluetooth, HomeRF™, IEEE-802.11a, IEEE-802.11b, and HiperLAN2 provide users with mobility, but bandwidth remains an issue. Whereas Bluetooth is a popular personal area network technology, IEEE 802.11 and HiperLAN2 are wireless LAN technologies that provide connectivity to telecommuters, SOHOs (small office/home office), and hospitals. HomeRF remains focused on cordless transmission of voice and data around the home.

### FPGA-Based Home Networking Bridges the Islands

Home networking bridges exist at the periphery of each technology island. These bridges need a flexible, reprogrammable, and low-cost platform to accommodate time-to-market pressures, specification changes, and short product lifecycles.

Aggressive process technology adoption has enabled FPGAs to obtain more die per wafer, provide more logic, offer increased performance, and accommodate various ASIC-like features required for system integration. This fast-evolving process technology has been fundamentally instrumental in narrowing the wide gap between FPGAs and ASSPs (Application Specific Standard Products). FPGA vendors, by virtue of the benefits reaped through process technology, now have the capability to bring traditional FPGA benefits to the cost-sensitive home networking market.

As previously noted, conflicting specifications and the lack of a clear direction of

future technology have created the need for FPGA-based home networking bridges. Figures 2 and 3 show two examples of FPGA-enabled bridges: a wireless LAN-to-Ethernet bridge, and a USB-to-HomePNA-and-Ethernet bridge. Xilinx Spartan-II FPGAs – highlighted in red – are at the heart of both network bridges.

Home network bridges operate in the second layer of the classic, seven-layer OSI (Open System Interconnect) network reference model. The first layer PHY (physical) defines the electrical, mechanical, and procedural specifications that provide the transmission of bits over a communication medium or channel. The second layer - the data link layer – consists of an upper sub-layer, logical link control (LLC), and a lower sub-layer, media access control (MAC). The MAC ensures error control and synchronization between the two engaged network segments. It is also responsible for determining priority and allocation to access the channel to the third layer – the network layer.

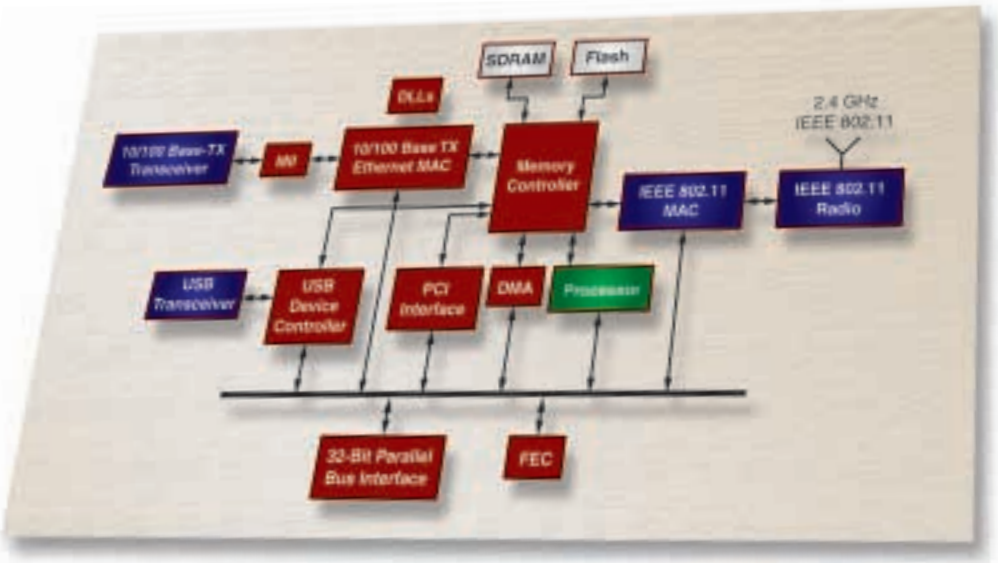


*Figure 2 - Wireless LAN-to-Ethernet home networking bridge*

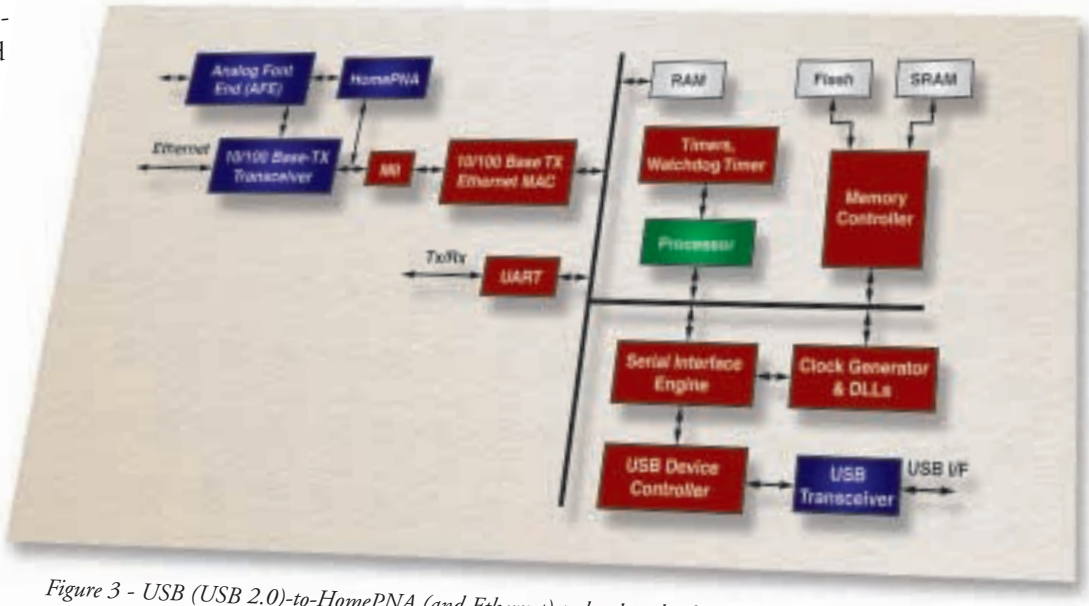


*Figure 3 - USB (USB 2.0)-to-HomePNA (and Ethernet) technology bridge*

While the Ethernet MAC has been around for a long time, the HomePNA specification that defines the MAC and PHY layers is quickly evolving. With the HomePNA 2.0 specification already defined (and a faster, higher bandwidth phoneline specification is on the way) it seems ideal for the MAC and media independent interface to be programmed in an FPGA. Similarly, the IEEE 802.11, HomeRF, FireWire, USB, HiperLAN2, and Bluetooth are all technologies with evolving specifications ripe for FPGA-enabled system integration and upgrades.

### Spartan-II FPGAs Bridge the Gap

Spartan-II FPGAs not only provide critical parts of the technology bridges at low costs, they also offer system-level features such as DLLs (delay-locked loops), BlockRAM, and SelectI/O™ technology to provide additional savings. FPGA gates left over from programming the MAC may be used to customize the end product. They may also be used for additional functionality, such as memory controllers, (SRAM, DRAM, and flash) PCI controllers UARTs, and forward error correction.

Xilinx FPGAs are based on SRAM technology and can be reprogrammed an unlimited number of times. Field upgradability gives you the ability to upgrade functionality of the FPGA through a simple update to the FPGA configuration bitstream. FPGAs allow you to gain market share by bringing products to market sooner than with stand-alone ASSPs. Moreover, FPGAs enable you to upgrade your hardware in the field and stay in the marketplace longer. This ability to adapt to specification changes maximizes profitability.

Interoperability is the key to market success in home networking. Technology bridges based on Xilinx FPGAs address some of the most fundamental challenges facing home networking today: they can connect different information appliance home networks and ensure seamless interoperability. As the world leader in field programmable gate arrays, Xilinx is uniquely positioned to be the matchmaker between incompatible technologies.

# Design FPGAs Using Free, Downloadable WebPACK Software

## Free WebPACK ISE software tools are now available for the Spartan-II family of FPGAs.

by Marc Baker
Applications Engineer, Spartan FPGA Marketing, Xilinx
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You can now implement your Xilinx FPGA designs by downloading free WebPACK™ ISE™ (Integrated Synthesis Environment) tools from Xilinx.com. WebPACK ISE software is popular because it provides excellent, free software support for CPLD designs, and it has been extended to include support for the entire Spartan-II™ FPGA family and the Virtex™ XCV300E device. WebPACK ISE software is a complete development system with no expiration date.

You can try your hand at FPGA design without having to make the up-front investment in software. WebPACK ISE software supports VHDL and Verilog™ design entry for FPGAs with dedicated XST™ (Xilinx Synthesis Technology) software. You may also download industry-leading Model Technology™ HDL test vector generation, and Synopsis VSS™ simulation tools to help verify your designs. With reprogrammable FPGA technology, you can easily download designs and try them out in-system, encouraging an iterative design process. WebPACK ISE tools include the JTAG Programmer™ software, which you can use to download designs with a JTAG cable to any development board, using JTAG cable. Development boards are available from Xilinx and several third-party vendors.

WebPACK ISE software provides a modular set of tools, allowing you to download and install only what you need for your requirements. All WebPACK ISE downloadable software solutions are supported on Windows 98, NT 4.0, and 2000 platforms. You can register to be notified by e-mail when updates are made available to the WebPACK ISE tools.

| Device | System Gates | I/Os | Block RAM bits |
|---|---|---|---|
| XC2S15 | 15,000 | 86 | 16K |
| XC2S30 | 30,000 | 132 | 24K |
| XC2S50 | 50,000 | 176 | 32K |
| XC2S100 | 100,000 | 196 | 40K |
| XC2S150 | 150,000 | 260 | 48K |
| XC2S200 | 200,000 | 284 | 56K |
| XCV300E | 300,000 | 316 | 128K |

*Table 1 – FPGAs supported by WebPACK ISE software*

WebPACK ISE software for FPGAs includes:

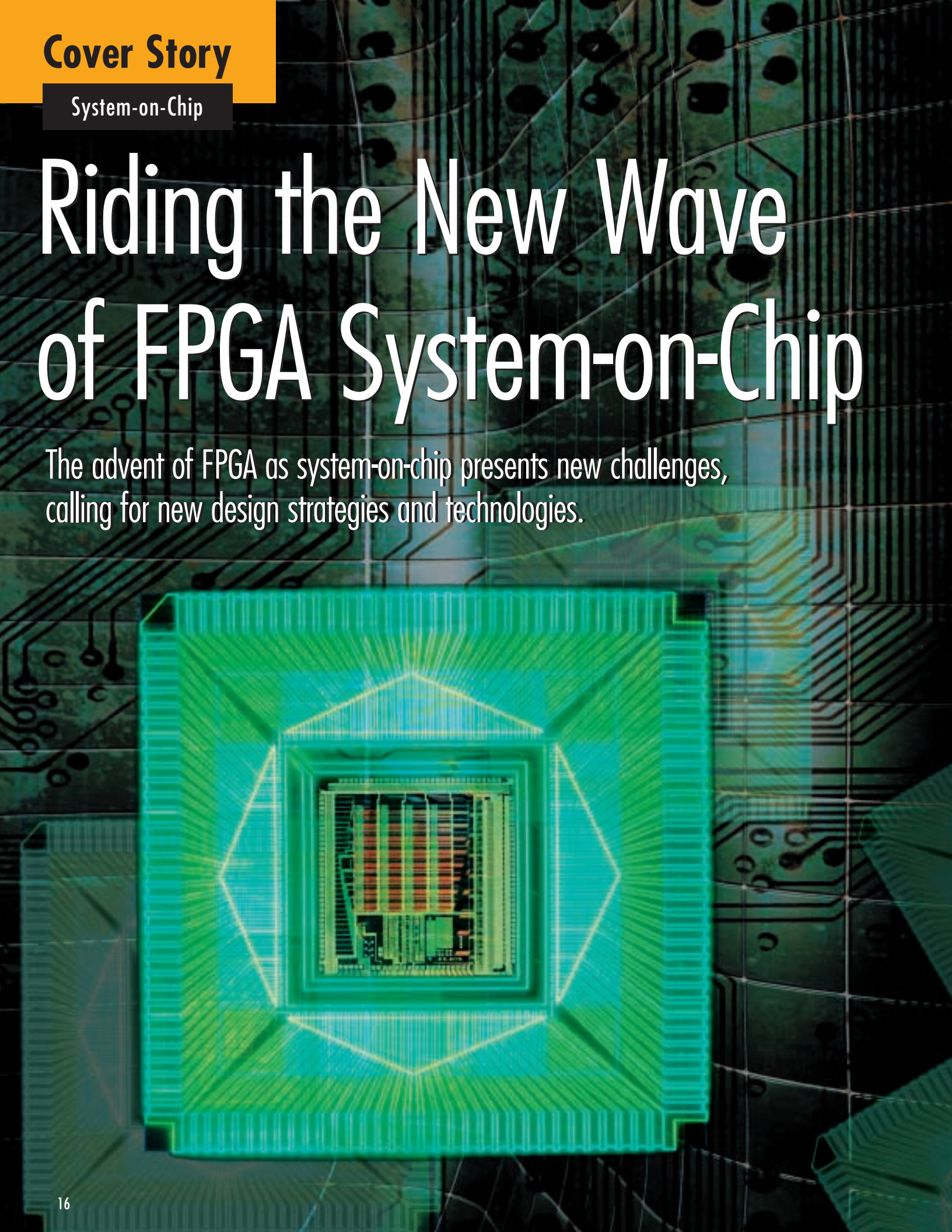
- Project Navigator™
- XST VHDL and Verilog synthesis
- HDL testbench generation
- HDL simulation
- User constraints editor
- Timing-driven implementation
- Multipass place-and-route
- Floorplanning
- Static timing analysis
- Functional and timing simulation
- Third-party simulation support
- Error navigation to the Web
- 1149.1 JTAG programming
- Bitstream and PROM configuration.

WebPACK ISE software is based on the award-winning Xilinx Foundation ISE Series™ software package. It is different from Foundation ISE software, however, in that it is focused on CPLDs and Spartan-II FPGAs, is instantly accessible, and it's free. Support is provided for all CPLDs and the FPGA devices listed in Table 1.

***WebPACK ISE software is the programmable logic design system that is the easiest to learn, easiest to use, and easiest to get. You will be up and running fast with the Xilinx modular approach to Web-based delivery. See for yourself. Download the tools you need today from www.xilinx.com/sxpresso/webpack.htm.***

# Riding the New Wave of FPGA System-on-Chip

The advent of FPGA as system-on-chip presents new challenges, calling for new design strategies and technologies.



by Anne Sanquini
VP & General Manager, HDL Design Division, Mentor Graphics
anne_sanquini@mentor.com

Adoption and assimilation have always been the modus operandi for successful, lasting conquest. We are witnessing the advance of FPGAs (Field Programmable Gate Arrays) against ASICs (Application Specific Integrated Circuits) in terms of performance, complexity, size, and revenue. The unfamiliar challenges and frustrations that FPGA designers are beginning to face are not new to the ASIC world, as manifested in SoC (System-on-Chip) design. Ten-million-gate platform devices call for a complete design environment, not just one that borrows from the ASIC world, but one designed with knowledge of and explicitly for the FPGA world.

## ASIC vs. FPGA - Not Your Grandmother's FPGA

The FPGA market has undergone an interesting revolution. As FPGAs have improved in terms of speed, volume, and size, programmable logic silicon has cut deeper into the ASIC market. The performance, complexity, and density gap is closing, and FPGAs enjoy lower development costs, while those of ASICs continue to rise.

Plus, unless you're building as many as 50,000 or 100,000 units a year, you're probably better off going to production with an FPGA. Because you can customize an FPGA, you don't have to spend time "in the fab" (in the fabrication process). The results are significant cost savings and much faster time to market.

## FPGA - The Darling of Fab

Another relevant development is the takeover of semiconductor manufacturing by specialty fab houses. In the past, FPGAs lagged behind ASICs in performance and density because FPGAs were not welcomed in the fab houses owned and operated by the big semiconductor companies. These internal fabrication operations favored high volume, uniform chips like DRAMs – chips that run over and over again without changing. Therefore, companies didn't put the energy and resources into developing FPGAs.

That's all changed. FPGAs are now the leading-edge semiconductor process technology drivers. New fab foundries have replaced DRAMS with FPGAs as their process drivers, because identical FPGAs can be run in very high volumes – unlike most ASICs. FPGAs, by definition, are programmable by the customer. Now, through partnerships with fab houses, Xilinx has their semiconductors built directly for them. For these and other reasons, FPGAs are an increasingly valuable technology, providing liberating flexibility at a low cost.

## The Price of Success – The Challenge of the Ten-Million-Gate Platform Device

The rapidly evolving FPGA market will continue to erode the ASIC market, not only because of programmable logic's traditional advantages, but also because of its greater capabilities – potential and actual. FPGAs are getting bigger, faster, and richer in functionality. This is important for improving ASIC prototyping, yet it also drives the migration of FPGA to SoC.

The competitive advantage of FPGA SoCs has arrived. Today, close to 50% of FPGA designs are SoCs. That means you'll be running up against SoC issues. The combination of large, complex IP (Intellectual Property) blocks and embedded software,

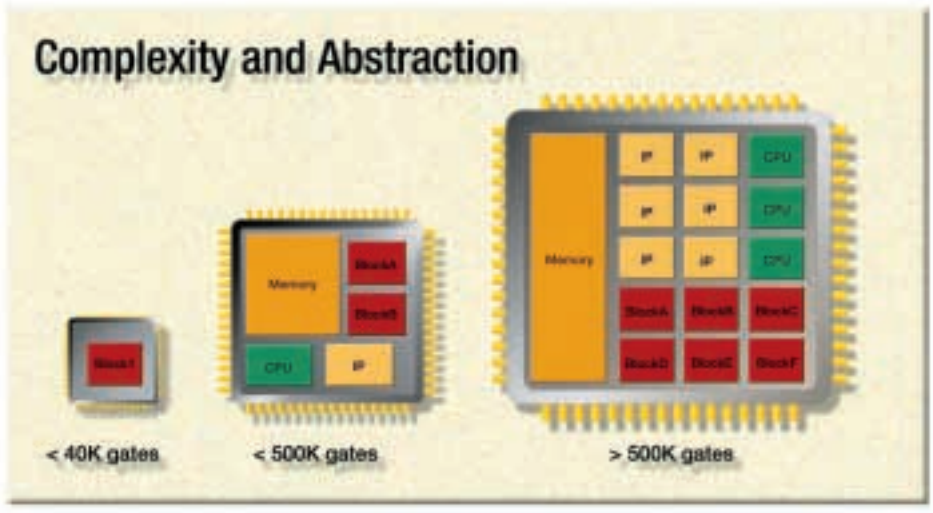



*Figure 1 - The increasing density, higher speeds, and application of mixed design with IP cores has enabled the new FPGA/SoC environment.*

combined with soaring transistor count, tax the capabilities of traditional design methodologies – particularly verification tasks, which now can consume 60% to 80% of design resources. The high densities, small geometries, and increased role of interconnects in device behavior present daunting challenges during synthesis.

Historically, FPGAs were small devices, so FPGA designers were able to experiment with various programming options until they got it right. Yet, as FPGAs have increased in density and performance, they've become too large for ad hoc design. The time cost of just figuring out where the bugs are has become too great.

Today's FPGAs cause problems for ASIC and board designers as well, who now have to deal with high pin counts and high frequencies on their boards. In the past, FPGAs were considered just bits of programmable logic board designers could use to sweep up the stuff on the PCB that they forgot to put in their ASICs. All of that has changed by what Xilinx has done to improve FPGA functionality. Board designers can be overwhelmed by this "new" FPGA technology.

The challenges of SoC call for designs that take advantage of high production runs, accommodate fast debug and verification, adapt to changing standards, work with both IP cores and custom logic, and meet rigorous performance requirements. Designers demand tools that provide high QoR (Quality of Results) for their FPGAs, optimize their entire design at once in a top-down design flow, enable aggressive optimization of individual design blocks, and provide tight integration with vendor IP tools. Meeting all of these requirements while still getting to market quickly begs for team design. Designs are simply too big and complex for a single designer. Team design is supported by an incremental, modular approach that implements design reuse effectively. Modular design – combined with physical optimization – support the need for large high-performance designs, shorter design cycles, and a team-based approach.

Along with design complexity, verification is emerging as a critical design strategy. The focus has shifted from content creation to the problems of evaluating, integrating, and verifying multiple pre-existing blocks and software components. This methodology is characterized by more in-depth system-level design, concurrent hardware/software design and verification, and verification at all levels of the design process.

### Turning Silicon into Gold

FPGA designers must be able to handle and manage the enormous amount of data required for today's FPGAs. What's important is that whether you're an FPGA designer stepping up to the next level, or a board designer challenged with new FPGA devices, your tools must talk to each other. Integration is key. And the tools must be available for both FPGA and PCB designers.

You'll need an FPGA flow that provides a high QoR for faster devices and a synthesis flow that provides control over the design. You will want a complete flow that works with design creation and simulation. Furthermore, you'll need a flow that easily mixes legacy design with memory and IP. Finally, you'll look for the ability to quickly and easily insert IP cores from FPGA vendors and third parties.

Mentor Graphics has a history of expertise and investment in this kind of comprehensive, interlocking solution – in this case, a comprehensive set of FPGA development tools. Conversely, many EDA (Electronic Design Automation) companies are blind to what is going on with FPGAs. Their tools are tuned toward ASIC design. FPGA cus-

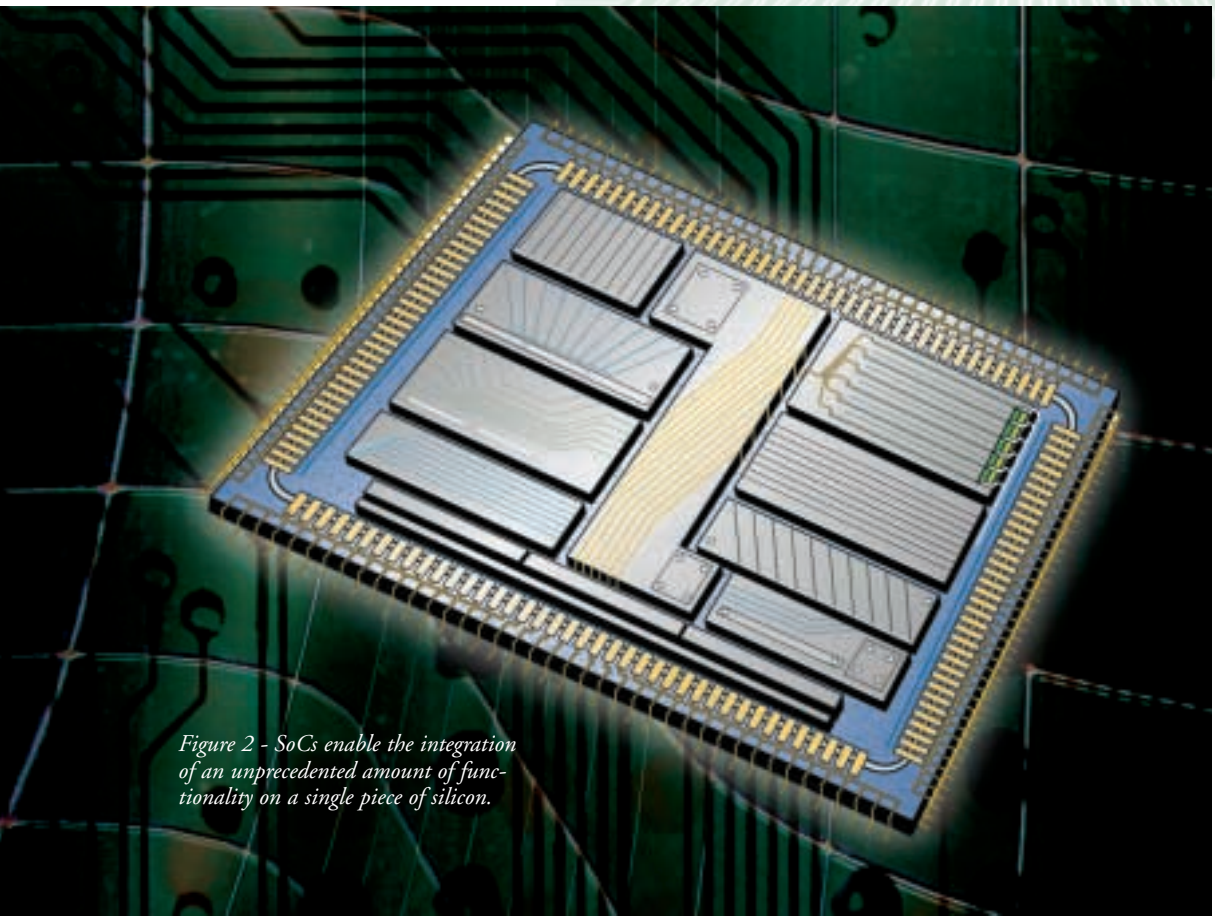


*Figure 2 - SoCs enable the integration of an unprecedented amount of functionality on a single piece of silicon.*

tomers are at a disadvantage, because to come up with the same solution, these ASIC-centric companies would have to turn their focus to another set of issues – issues faced specifically by the FPGA designer. For various reasons, they're reluctant to do that.

### A Complete, Interwoven Design Flow

Mentor Graphics is a leader in SoC design tools and design productivity solutions. In addition, the company has concentrated on and invested in FPGA technology. We're positioned to help FPGA design teams succeed by offering a complete tool suite for the entire FPGA design flow – from creation through simulation to synthesis – with FPGA Advantage™.

Mentor's LeonardoSpectrum™, the world's number one FPGA synthesis tool, provides physical integration for modular design and IP integration for design reuse. LeonardoSpectrum delivers high QoR for the latest FPGAs, optimizes the entire design at once in a top-down design flow, enables aggressive optimization of individual design blocks, and provides tight integration with vendor IP tools. Meanwhile, Mentor's TimeCloser™ technology provides physical optimization and bi-directional integration with the Xilinx place-and-route tools to help achieve desired performance levels.

The increased impact of debugging on design productivity means that designers need tools that allow them to rapidly create, modify, debug, and document sophisticated HDL designs using real-time syntax and semantic verification. FPGA Advantage enables both easy detection of bugs and quick design modifications. This solution also supports design reuse and team design. With hardware and software IP available through the Mentor Graphics Inventra™ IP cores and VRTXoc Real-Time Executive™, Mentor Graphics further supports the time-to-market and design productivity advantages of design reuse.

A multi-tiered verification methodology that takes full advantage of early-design simulation techniques enables concurrent hardware/software verification and minimizes dependence upon late-design verification. Seamless™ – the leading hardware/software co-verification tool – delivers hardware/software interface verification capabilities extensively and consistently throughout the design process.

Successful SoC design also requires a proven, reliable simulation environment supporting simulation at all levels of the design flow. Through functional and timing simulation, ModelSim™ and the industry-standard XRAY® Debugger provide verification at the chip level. Verification at the system level is handled by Tau™, utilizing STAMP models for board-level static timing analysis, and the ICX™ tools, which apply IBIS™ models for signal integrity analysis.

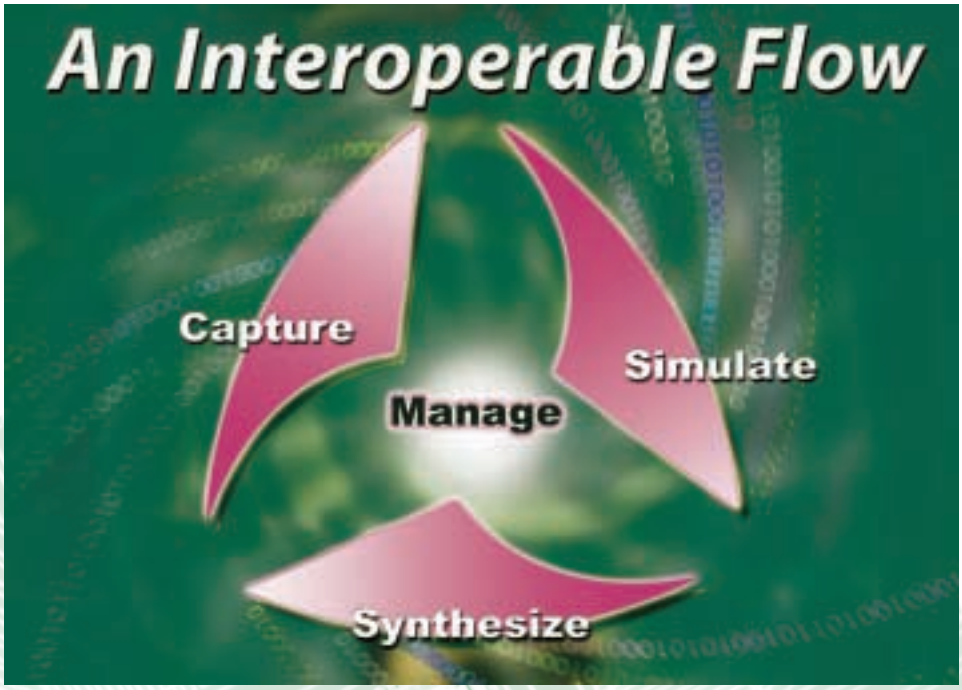



*Figure 3 - The team-based approach required by today's FPGA designs are best supported by a single, integrated design solution.*

### Single Vendor Design Flow

Mentor Graphics offers a tested, integrated solution that works for both FPGAs and SoCs, all from one company. FPGA designers are already discovering that working with a single development tools provider is both convenient and efficacious. Plus, by design, the Mentor Graphics EDA tools can be integrated with third-party products and IP. Mentor Graphics FPGA design tools are language and platform neutral because design teams need the ability to work in VHDL, Verilog, and mixed-language environments, as well as on UNIX and Windows-based platforms. Mentor Graphics is unique in the industry in that we can deal with both the embedded software customer – through our Embedded Software Design division – and the FPGA customer with our FPGA Advantage flow. Nobody else has that flow, in terms of tightness, completeness, and relevance to those specific customers.

As FPGAs have become more complex, Mentor Graphics has been well positioned to step in with the appropriate design solutions. Our complete design flow gains its integrity from advanced features for FPGA SoC creation, including incremental synthesis and modular design, leading device support, integration with vendor IP flows, and flexible design flows for million gate designs. Together, Mentor and Xilinx plan to speed the adoption of FPGAs because the benefits and opportunities are enormous.

# Xilinx FPGAs and IRL Keep ReplayTV on Target

by Wallace Westfeldt
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Jeff Hastings
Senior Vice-President of Engineering, ReplayTV

Field programmable gate arrays and Internet Reconfigurable Logic™ from Xilinx are critical elements of ReplayTV's strategy to be first to market and best in class.

The best way to hit a moving target is to move with it. As a business strategy, ReplayTV™ is leading the edge of the fast-moving personal video recording market. Based in Mountain View, Calif., ReplayTV Inc is a digital PVR (Personal Video Recorder) manufacturer and online service company that finds and records television shows - broadcast, cable, satellite – on a hard disk so you can watch them whenever and however you want. Besides offering all the functionality of high-end videotape recorders, ReplayTV features pause, rewind, slow motion, and instant replay of live television. Furthermore, it automates program selection and records up to 60 hours of television using the MPEG-2 audio/video protocol for DVD-quality viewing and listening.

The two enabling technologies are the Xilinx Spartan-II™ XC2S40 FPGA and the Xilinx IRL (Internet Reconfigurable Logic) system. Using the XC2S40 device, ReplayTV estimates it saved as much as four months in bringing their product to market. Moreover, combining the reprogrammability of an FPGA with IRL technology allows ReplayTV to perform transparent bug fixes, upgrades, and feature additions to PVRs in the field long after the sale. This makes it possible for ReplayTV to adapt to and adopt emerging standards and protocols, thus extending product life – and value. (For more on emerging standards and protocols, see "eSP Solutions at Your Fingertips" and "Xilinx eSP Initiative Will Accelerate Time-to-Market for Consumer Products" in this issue of Xcell Journal. Also, visit the new Xilinx eSP website www.xilinx.com/esp.)

PVRs (or DVRs – Digital Video Recorders) are among the newest consumer products. Both the market they serve and the feature sets they offer are continually changing. ReplayTV's forward-thinking business strategy, therefore, is to carry on the design and deployment cycle long after the original sale.

### What It Is and What It Does

Bigger than a black bread box, the ReplayTV PVR unit looks somewhat like a common VCR, but compared to a VCR, it's definitely next-generation technology. It does much more than a VCR – and it's much easier to use. With the free ReplayTV Service, the ReplayTV PVR can find, catalog, and record all the television you have access to – broadcast (antenna), satellite dish, and/or cable TV. Using an onboard 56K modem hooked into your telephone system, the PVR updates its program guide nightly from the ReplayTV Service Internet server. In addition to tracking program schedules, ReplayTV also offers other value-added services such as:

- ReplayZones™ – programming organized by categories such as situation comedies, sports, news, movies, and so on
- Closed-caption support – for secondary text for the hearing impaired


- MyReplayTV – a website that allows you to remotely program your PVR over the Internet
- Personal Theme Channels – consumer customizable Replay Zones that will record programming based on personal preferences, such as favorite actors
- ReplayTV Presents – original programming from ReplayTV
- QuickSkip™ – 30-second jump-forward (not fast forward) to skip commercials or undesirable scenes in recorded programming
- Instant Replay – jump 7 seconds back during live or recorded shows
- Universal remote control – full-featured ReplayTV remote controller for TV, VCR, DVD player, satellite receiver, and cable box.

The combination of reprogrammable hardware combined with reconfigurable software permits ReplayTV to stay on target with the moving market. Along with the nightly update of the program schedule, ReplayTV can transparently deliver to all its customers anything from a debug to an upgrade to an entirely new feature as soon as it is available. With no user intervention or attention required, the ReplayTV PVR continues to gain value-added service and functionality – after the sale.

For instance, ReplayTV was recently forced to deal with an edge condition that caused video noise in a few systems already in homes. One of the chips in the system had an undocumented clock threshold-switching problem. Because the control signals for this device were generated in the FPGA inside the PVR, it was possible to eliminate the problem by changing the timing of the FPGA-generated signal. As soon as the problem was debugged and certified, the company uploaded the fix to all ReplayTV systems in the field. Most customers never realized the change had been made, although some probably noticed improved video quality.

### Design by Layer

It all started with the decision to use an FPGA instead of an ASIC (Application Specific Integrated Circuit) semiconductor. The difference between an FPGA and an ASIC is the difference between a process and an event. Not only is the FPGA design cycle faster, it's open-ended. If you want to change an ASIC, you have to build a new one. All you have to do to change an FPGA is feed it a new bitstream – over the Internet.

By choosing the reprogrammable Spartan-II™ XC2S40 FPGA as the core of their design, ReplayTV engineers found themselves with a new, more convenient design cycle. Instead of designing and debugging the system as a whole, they found it easier and faster to "layer" capabilities one at a

time, debug them individually, and then add the next function or feature. This made debugging easier and faster because only the latest layer's code could contain major bugs or interact negatively with the already bug-free code stored in the lower layers.

Of course, the basic hardware and control logic were implemented in the first layer. The embedded operating system and drivers were designed into the second layer. The applications software were programmed into the third layer. The upper layers consisted of "feature algorithms" such as vendor-specific copy protection, V-Chip detection of "adult" programming, and software peculiar to a specific vendor's front panel design. (In addition to selling its own brand, ReplayTV also licenses its technology to original equipment manufacturers.)

With an FPGA, the designers could iterate their way toward design goals, correcting bugs as they were uncovered. Using the layered approach, the engineers were able to implement their design in the most straightforward fashion first, taking as many gates as needed, getting the function debugged, and only then optimizing the bitstream to make the best use of the FPGA.

As the design progressed, ReplayTV's engineers found themselves adding more and more functions to the FPGA – many more than originally envisioned. Engineers began with what they thought was excess capacity in the FPGAs, but they "filled" the FPGA several times. Then they used iterative place-and-route software to place more logic onto the chip. If performance was an issue, they made the place-and-route operation timing-driven and let it run until it came up with the solution needed for a function to perform at a given rate. The designs were implemented using Xilinx Alliance™ and Foundation ISE ™ series software.

### Marketing by Design

ReplayTV not only sells its system directly, but it also negotiates license agreements with companies such as Panasonic. In February, Panasonic introduced its 27-inch PV-SS2710 PanaBlack™ TV/ShowStopper® Hard Disk Recorder Combination with ReplayTV Service. Panasonic is the first OEM to integrate a television with a PVR. (ReplayTV just sells the PVR. You have to provide the television.)

For product differentiation, ReplayTV and its OEM partners each need slightly different feature sets, front-panel indicators, copy-protection algorithms, and other unique identifiers. Obviously, ReplayTV couldn't design different hardware for each market niche or OEM partner. The cost would have been prohibitive.

This is where the layered design approach enabled ReplayTV to service its respective partners' needs without compromising the underlying technology. For example, the basic PVR system must accommodate various copy-protection schemes. Not only are there several different copy-protection alliances throughout the world, but even for a given protection standard, each OEM must execute its own unique copy-protection agreement. (This is where lawyers effectively dictate standards and protocols to engineers.) Top-layer reprogrammability accommodates the nuances of each copy-protection agreement, worldwide, without changing the baseline system.

### Moving with the Target Market

It's one thing for ReplayTV to proclaim itself best in class. It's quite another when the worldwide consumer electronics industry validates that claim. At the Consumer Electronics Shows in 2000 and 2001, ReplayTV was named the CES Innovations winner for both Video Software and Video Hardware. In 1999, ReplayTV won Best of Show in the entire video category. Popular Science magazine gave ReplayTV its Best of What's New Award, and Popular Mechanics magazine gave ReplayTV its 1999 Editor's Choice Award.

ReplayTV is not without competition, however, and the target market is still moving. By choosing a Xilinx-based FPGA/IRL solution, ReplayTV has intelligently positioned itself to dynamically move with the market, selling a product and service specifically designed to accommodate the emerging standards and protocols of consumer electronics.

# Use the WebPACK Project Navigator to Set Design Constraints in CoolRunner CPLDs

Here's an introduction to User Constraint Files for designing CoolRunner CPLDs with WebPACK, the complete design tool that you can download from the Web.

by Jennifer Jenkins
Applications Engineer, Xilinx Inc.
jennifer.jenkins@xilinx.com

WebPACK™ Project Navigator™ software allows you to control a variety of design attributes in CoolRunner™ XPLA3 CPLD designs. You can generally set a design constraint on a whole device through the WebPACK Navigator GUI. But if you want to set characteristics for an individual signal in your design, you have to set up UCFs. Setting user-defined constraint files is easy to do – and this allows you to maintain your design specifics throughout the iterations of the design life cycle.

### Available Design Constraints

WebPACK Project Navigator gives you the capability to manually control the following attributes in a CoolRunner CPLD design:

- Pin and node assignments
- Output slew rate control
- Initial register state
- Input pin characteristics
- Signal optimization options.

The WebPACK Project Navigator GUI allows you to define some of these constraints for the device generally. Only a UCF, however, lets you set specific characteristics for an individual signal in a design.

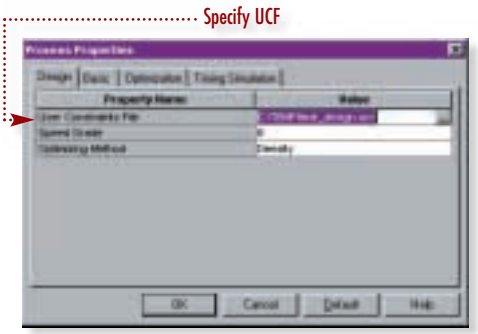


*Figure 1 - WebPACK specification of UCF*

### Specification of Design Constraints

The WebPACK GUI allows you to specify a UCF during design implementation. The WebPACK Process Properties window in Figure 1 illustrates how to specify the UCF.

The WebPACK GUI can also automatically create a UCF that can assign pin locations. You can then edit the UCF to fit your design specifications. For instance, the following example shows how to assign a certain signal to a specific pin. Note the syntax depends on the type of package used.

For PLCC (Plastic Leadless Chip Carrier), PQFP (Plastic Quad Flat Pack), TQFP (Thin Quad Flat Pack), and similar packages, the syntax would be:

```
PIN <signal_name> LOC=Pnn;
```

and the code might read:

```
PIN qout<0> LOC = P20;
```

For CS (Chip Scale), BG (Ball Grid), and similar packages, the syntax would be:

```
PIN <signal_name> LOC=RC;
```

and the code might read:

```
PIN qout<1> LOC = G2;
```

Another attribute the UCF offers you is the capability to control the slew rate for a specific output signal. The WebPACK GUI allows you to set the slew rate for all outputs in a design. To control the slew rate for an individual output, the UCF syntax would be:

```
PIN <signal_name> <slewrate>;
```

and the code might read:

```
PIN qout<0> SLOW;
PIN qout<1> FAST;
```

These are just a few examples of the value UCFs bring to you. With UCFs, you can maintain consistency during design iterations and control a design during the implementation process.

For more information on using a UCF to enter design attributes, refer to XAPP352 "Utilizing a User Constraint File for CoolRunner CPLDs" (www.xilinx.com/xapp/xapp352.pdf).

*To learn about the entire line of free, downloadable WebPACK ISE™ (Integrated Synthesis Environment) software, go to www.xilinx.com/webpack/index.html.*

# Smart Phones—From Luxury Item to Lifestyle Necessity


To capture the market for replacement handsets, the next wave of mobile phones must be smarter, lighter, and last longer on one charge.

by Karen Parnell
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Just as second generation digital wireless technology is ramping up, third generation (3G) wireless services are already under development – and in production. The mobile phone telecommunication industry is targeting "replacement phones" as the market's biggest revenue window.

Analog (1G) cellular and digital (2G) PCS (Personal Communications Services) phones are too new a phenomenon to just wear out. Industry analysts have defined the mobile phone saturation point to be 65% of the population. According to this statistic, Finland and the UK have just reached saturation, with Central Europe and North America to follow in the next few years. So, creating a demand for new handsets from existing subscribers means mobile phones must provide value-added services to be competitive as replacement handsets.

CoolRunner™ CPLDs (Complex Programmable Logic Devices) – available in very small, lightweight packages and utilizing Fast Zero Power™ technology – work ideally to add advanced features to handheld devices, and as such, they are already being used by mobile phone manufacturers. Additionally, using CoolRunner devices in mobile phones shortens time to market and enables field upgrades.

### Growth in Replacement Handsets

Figure 1 shows how important the replacement market is to wireless handset manufacturers. As shown, about 40% of the new phones sold in 1999 were replacement handsets. This figure is forecasted to rise to 61% in 2003, which means only about 40% of handset sales in 2003 will be to new customers. Therefore, in the future, it will become increasingly critical for the cellular handset supplier to convince existing subscribers that they "need" the newest technology.

In the coming years, six major types of handsets are (or will be) sold in the wireless phone marketplace:

- Analog cellular
- Digital GSM (Global System for Mobile Communications)
- Digital CDMA (Code Division Multiple Access)
- Digital TDMA (Time Division Multiple Access)
- Digital PDC (Personal Digital Cellular)
- Digital 3G.

Handsets that can handle two frequencies are called "dual-band," and those that can accommodate three frequencies are labeled "tri-band." Some handsets are categorized as "dual-mode" or "tri-mode." A typical multiple-mode handset can access analog AMPS (Advanced Mobile Phone Service) as well as digital PCS. In mid-1999, Nokia introduced a tri-mode CDMA 800/1900/AMPS handset (Nokia 6185) as well as a dual-mode CDMA 800/AMPS handset (Nokia 5180). Handsets sold today are predominantly digital. GSM technology dominates the European market while CDMA-type handsets rule the North American market.

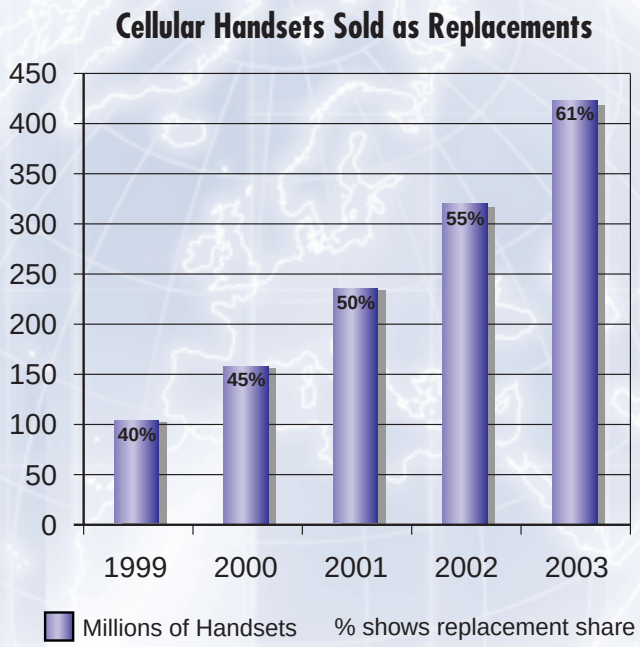


*Figure 1 - Cellular handsets sold as replacements*

Many handset manufacturers are worried the handset could become a commodity product, much like the simple calculator. In order to prevent this, and to increase the replacement handset market, some handset manufacturers are adding extra "must-have" functionality.

### 3G Enables New Handset Functionality

Third generation wireless services facilitate applications that were not previously practical or available over mobile networks because of the limitations in data transmission speeds. 3G technology increases available bandwidth up to 384 Kbps for handheld devices that are stationary or moving at pedestrian speed, 128 Kbps in cars, and 2 Mbps in fixed applications.

Because of the 3G bandwidth capabilities, high bandwidth applications are now more feasible than they were with interim technologies such as GPRS (General Packet Radio Service). The new EDGE (Enhanced Data rate for Global Evolution) air interface was specifically developed to utilize 3G bandwidth.

Newly enabled 3G applications range from Web browsing to e-mail to file transfers to home automation – the ability to remotely access and control appliances and machines in the home. Some of the most radical changes in 3G wireless and mobile technology include the following:

- People will look at their mobile phones as much as they listen to them. Television, e-mail, and multimedia services tend to attract attention to themselves. This means 3G devices will be even less safe for motorists. Instead of hands-free kits, we might need eyes-free kits – or heads-up displays.
- Data uses of 3G equipment will be as important as, and very different from, the traditional voice usage.

- Mobile communications will be so similar in capabilities to fixed communications that many users may only need one phone.

The mobile phone will become an integral part of many people's lives. A 3G handset will not be an accessory but rather a necessity. These phones will be like a remote control or a magic wand that lets people do what they want, when they want, wherever they want.

### "Must-Have" Functionality

In an attempt to keep the Average Selling Price (ASP) high, handset manufacturers such as Samsung have introduced "smart phones." Smart phones offer standard mobile communications services such as voice telephony, short message services (SMS), phone number memories, and Internet access. The Samsung smart phone, however, also features a Bible, hymnal, Buddhist Canon and songbook, English-Korean and Korean-English dictionaries, an engineering calculator, and electronic games.

Next generation mobile phones will also offer the following multimedia functions:

- Personal Digital Assistant (PDA) utilities
- Wireless Access Protocol (WAP), Internet services, and full Web browsing
- MP3 playing functions
- "Smart card" readers for on-line purchases and verification
- Digital radio reception
- Tri-mode and tri-band capability
- Video phone capability
- TV reception
- Global Positioning System (GPS) service
- Games console.

The aim is to integrate and converge as much functionality as possible to increase market share into other electronic equipment sectors, making the mobile phone a "must have" necessity for everyday life.

The next-generation mobile phone "tablet" will feature wireless home/office networking capability. Users will be able to take advantage of landline call rates by connecting via short-range wireless networking systems like Bluetooth™. When wireless phone call charges become equal to those of landlines, and when mobile phones have the capability to change contact number and functionality upon entering a new environment, they will potentially be able to replace all types of communication devices available today.

### Component Integration and Glue Logic

We are already seeing the integration of the basic handset IC components such as:

- Microprocessor
- DSP core
- Audio codec (analog-to-digital coder/decoder)
- 13 Kbps QCELP (Qualcomm Code Excited Linear Prediction) and EVRC (Enhanced Variable Rate Codec) vocoders (voice compression algorithm codecs)
- CDMA/AMPS modem.

Integration of components allows mobile phone manufacturers to save on the size and weight of the overall mobile handset – even while adding extra functionality. Moreover, to gain market share, manufacturers must be able to add extra functions ahead of the competition. It is well known that the manufacturer who is first to market wins the largest percentage of the available market.

Programmable logic devices give manufacturers a major time to market advantage over chipset manufacturers and ASIC developers. Thus, we are seeing increased use of low power programmable logic devices to "glue" chipsets together, and more recently, to add extra functionality, like MP3 players and PDA functions. Increasingly, Xilinx ultra low power CoolRunner CPLDs are populating must-have mobile phones.

We have already seen a CoolRunner device in a handset with a GPS add-on module. The GPS module can not only be used as a route planner and directional aid, but it can quickly dial emergency services and let them know where you are if you are in danger. CoolRunner devices are also being employed in tri-band (GSM 1900/1800 & 900 MHz) handsets as chipset glue logic to gain time to market advantage.

Two key selling points of mobile phones are "talk time" and "standby time". These times must be as long as possible – without compromising the size and weight of the handset. CoolRunner CPLDs are being used in handsets because of their exceedingly low power consumption (<100 µA). What's more, they are available in innovative, small footprint packages. Figure 2 shows a new chip scale package that measures 6 mm by 6 mm and has a pin pitch of only 0.5mm.


*Figure 2 - Xilinx CoolRunner CPLD in a chip scale package – small, light, and ultra low power*

### Soft Radio

In the future, we may see "soft radio" technology bring down the IC count in state-of-the-art mobile phones to only two chips – one highly integrated analog RF component and one all-encompassing digital processor/memory device. This very complex "on-the-fly" (through the RF front-end) software-programmable radio technology won't be widely available until 2005 at the earliest. When soft radio does become mainstream, however, it will enable true interoperability among mobile phones.


*Figure 3 - Reconfigurable logic in mobile phones*

Soft radio technology will be made possible by field programmable gate arrays like Spartan-II™ and Virtex-E™ FPGAs from Xilinx. By using wireless Xilinx Internet Reconfigurable Logic™ (IRL), handsets can be upgraded in the field to enhance hardware functionality or to add completely new options – or to disable the handset if it is stolen.

The next generation mobile phone could feasibly be sold as a blank tablet with as much or as little functionality as you want. For example, you could purchase the tablet with only cellular phone and PDA capability. Later, long after purchase, you might decide to increase or enhance its features. This enhancement could take the form of an MP3 player, for instance. You could simply dial into your tablet manufacturer's website and pay for an MP3 player hardware description file to be downloaded to your tablet. Then using wireless IRL technology, you could reconfigure your handset to play MP3 audio files.

### Internet Reconfigurable Logic in Action

Figure 3 shows the use of reprogrammable logic in today's mobile phones for chipset glue logic – and tomorrow's fully field reconfigurable and customizable wireless handsets. Celoxica™, Marconi Communications Limited, and Xilinx have already developed a proof-of-concept MultiMedia Terminal (MMT) to demonstrate IRL. (See "Celoxica Implements 'Soft Hardware' in Internet MultiMedia Terminals" on Page 52). In a process similar to downloading software, the device is able to download FPGA configuration files for instantaneous reconfiguration. The device shows how value-added services, such as new applications and upgrades, can be remotely configured to FPGA-based products. The proof-of-concept terminal demonstrates that high-gate-count FPGAs can be used to achieve "processor-like" functionality – without the need for a separate embedded processor.

The major design challenge for proof-of-concept IRL was to "fill" these very large FPGAs with complex applications such as VoIP (Voice over Internet Protocol), TCP/IP, MP3, games console, and graphics display. Celoxica's system-level design suite was used for rapidly designing and prototyping these different applications to target Xilinx FPGAs – in just three months.

### Conclusion

Demand for wireless handsets for new subscribers will decrease in the next few years as we reach regional saturation points. To combat this slowdown in new subscribers, mobile handset manufacturers are striving to add more functionality, such as PDA utilities, GPS navigation, Internet access and browsing, real-time video services, and MP3 music players. These value-added services will make wireless handsets must-have devices and will boost the replacement handset market.

Time to market is key to these new technologies. With reprogrammable logic and IRL, handset manufacturers can beat the ASIC competition to market and sell highly versatile blank tablet devices that can be reconfigured on the fly over wireless connections to perform whatever services the consumer wants today – and tomorrow.

**Further Information**

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| Xilinx Spartan FPGAs | www.xilinx.com: Products: Devices: Spartan II |
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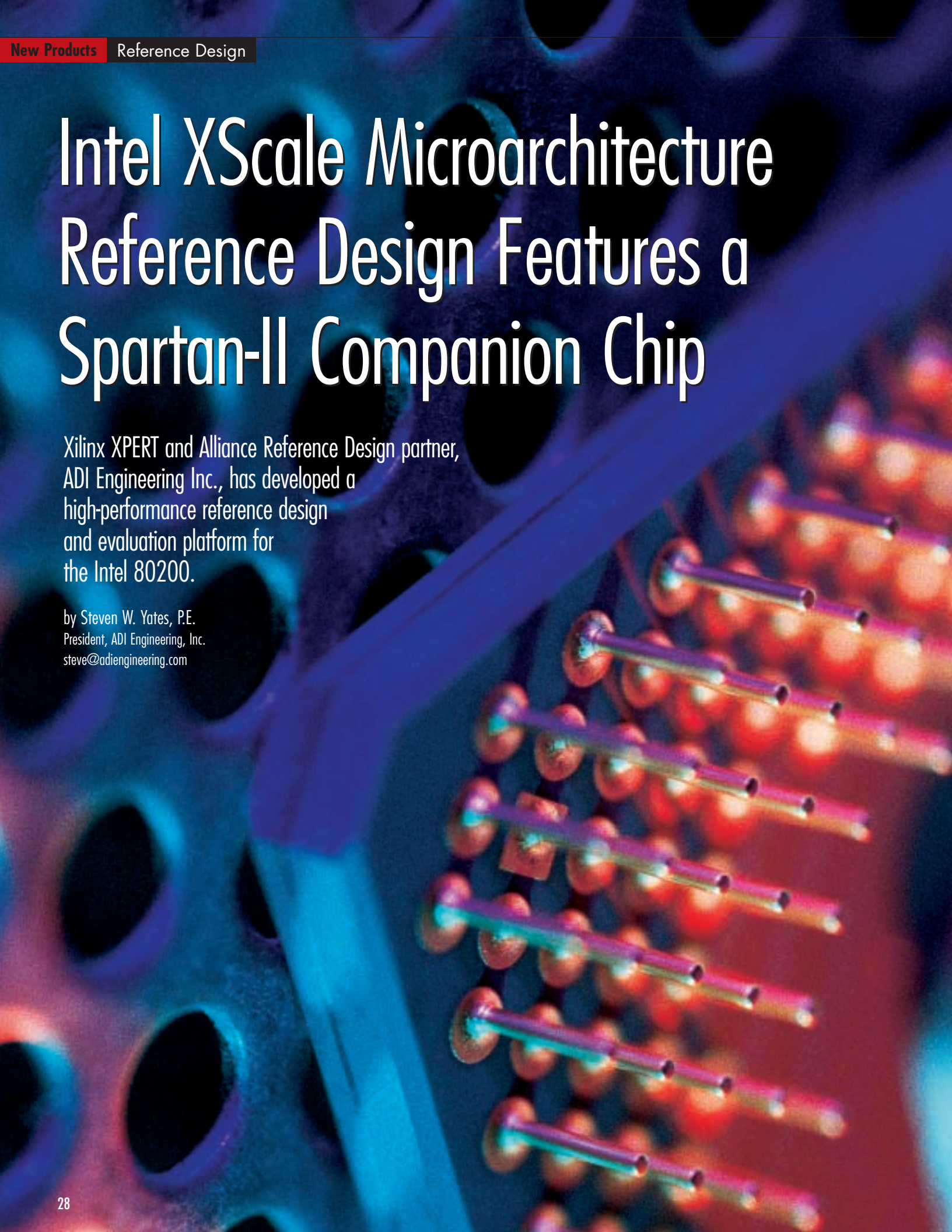
# Intel XScale Microarchitecture Reference Design Features a Spartan-II Companion Chip

Xilinx XPERT and Alliance Reference Design partner, ADI Engineering Inc., has developed a high-performance reference design and evaluation platform for the Intel 80200.

by Steven W. Yates, P.E.
President, ADI Engineering, Inc.
steve@adiengineering.com



The Intel 80200 is the first processor based on the Intel® XScale™ microarchitecture: It integrates an external bus controller and an interrupt controller around the ARM™-compliant processor core. The 80200EVB reference design features a Xilinx XC2S150 Spartan-II™-based 80200 FPGA Companion Chip (80200FCC), providing 80200-optimized SDRAM control, a peripheral bus interface, and a 64-bit, 33 MHz PCI 2.2 interface.

### The Intel XScale Microarchitecture

The Intel XScale microarchitecture represents a major advancement in high-performance, ultra-low power, embedded computing for applications including Internet appliances, handheld devices, networking and wireless equipment, and remote access servers. With its unique power-optimized, performance-oriented design, this microarchitecture offers highly scalable power and performance – from 125 MIPS at 10mW to 1,000 MIPS at less than 1W – to fit a wide range of applications.

As the successor to the popular StrongARM™ architecture, the Intel XScale microarchitecture features an ARM v.5TE instruction-set-compliant execution core with a wide array of performance enhancing and power saving technologies. Performance and power are scalable not only to suit the requirements of specific end applications, they can be adapted on the fly to match specific content as well.

### The 80200EVB Reference Design

ADI Engineering's 80200EVB enables you to evaluate the Intel XScale microarchitecture, and to leverage the proven 80200FCC and board-level designs to accelerate your time to market.

### Design Overview

The 80200EVB is a complete reference design for the Intel 80200 processor. Major features of the 80200EVB are:

- Intel 80200 processor running at up to 733 MHz
- Spartan-II 80200FCC companion chip implementing a high-performance SDRAM controller, 8-bit peripheral bus interface, and future 64-bit, 33 MHz PCI 2.2 interface
- 32 MB PC100 SDRAM, expandable to 128 MB
- 1 MB flash memory, expandable to 4 MB
- JTAG debugger interface
- RS-232 port
- Seven-segment LED display
- On-board power supply, operates from a single 9 - 15 VDC input.

A block diagram of the 80200EVB is shown in Figure 1.

### 80200 Bus Interface

The 80200 processor's external bus interface is deeply pipelined to hide external memory latency. This works well with pipelined memory technologies such as SDRAM.

The 80200 external bus interface is split into separate request and data buses, both of which are synchronous with respect to the 100 MHz memory clock. Requests for data read and write cycles are issued to the 80200FCC memory controller by the 80200 (or other bus masters) on the request bus. Up to four requests can be pending at a time.

Some time after a request is made on the request bus, data must be transferred for that request on the data bus. Each request has a corresponding transaction of one or more data cycles. Data bus transactions must occur in the same order as the requests were made but the request and data buses are otherwise independent. The data bus consists of a 32-bit or 64-bit wide data path and associated data check bits for use with ECC memory.

For burst read accesses, the 80200 supports a Critical Word First (CWF) protocol, which allows the data to be returned starting with the requested DWORD instead of starting at the beginning of the block of data. The 80200FCC supports the CWF protocol for SDRAM and peripherals on the peripheral bus.

### 80200FCC Memory Controller

The 80200FCC memory controller is a full-featured, high-performance SDRAM controller designed from the ground up to take advantage of the 80200's pipelined

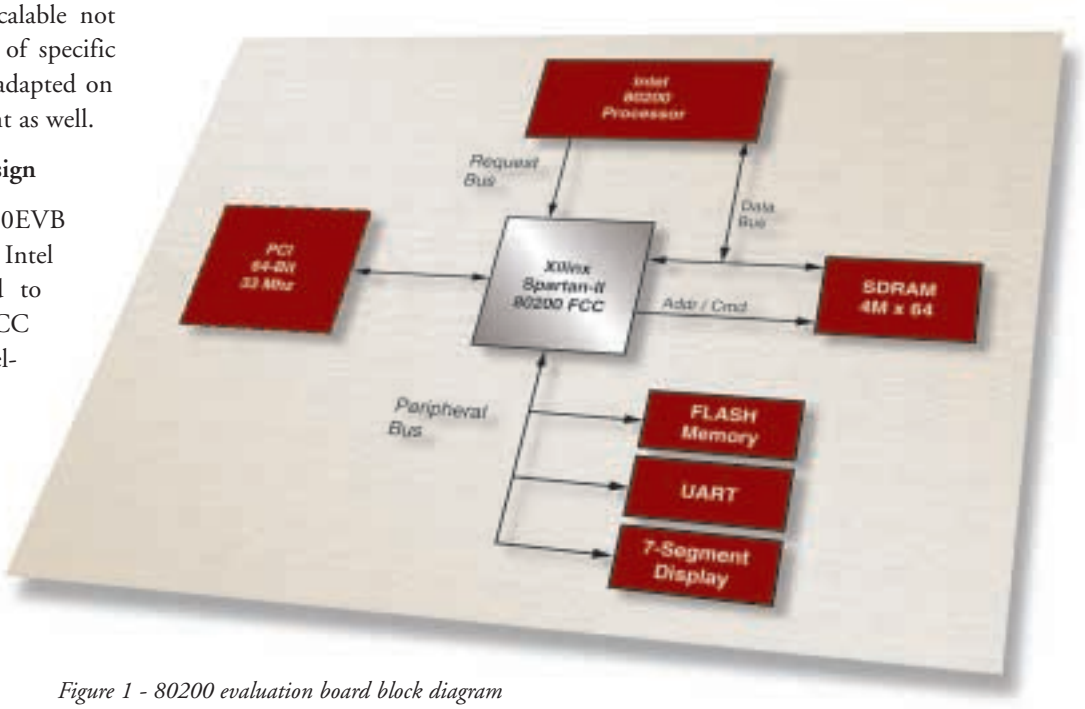



*Figure 1 - 80200 evaluation board block diagram*

external bus. Sequences of 80200 requests are examined and tracked by the 80200FCC memory controller as they enter into and propagate through its internal request queue. This enables the 80200FCC memory controller to look ahead at requested SDRAM transactions to determine how best to fulfill the requests while keeping the 80200 external bus operating at peak efficiency.

Major features of the 80200FCC memory controller include:

- Automatic SDRAM initialization
- Maintains row state for each SDRAM bank, closing rows only when necessary
- Automatically guarantees SDRAM command sequence timing
- Manages 80200 data bus by automatically inserting bus turnaround cycles when required
- Queues up to four pending 80200 requests
- Implements a two-level SDRAM refresh request priority scheme to minimize refresh overhead, queuing up to eight refresh cycles for burst execution
- Pipelines SDRAM commands to keep data bus fully utilized
- Supports Critical Word First protocol for SDRAM and peripherals
- Aborts illegal bus requests
- Provides a separate 8-bit peripheral bus, minimizing SDRAM performance impact
- Provides single stage write posting to the peripheral bus
- Achieves a sustained SDRAM bandwidth of 800 MB/s at 100 MHz.

The 100 MHz operation of the 80200FCC is made possible by the many performance-enhancing architectural features of the Xilinx Spartan-II family, including on-chip DLLs, I/O cell flip-flops, configurable I/O drivers, internal three-state buffers, and low-skew global routing resources. The Spartan-II family is able to provide these critical performance-enhancing features yet still maintain a low cost point.

To match the performance of the memory controller to a variety of SDRAM devices, many SDRAM timing parameters such as CAS latency, RAS precharge, RAS to CAS delay, and others are configurable. Configurable timing parameters may be

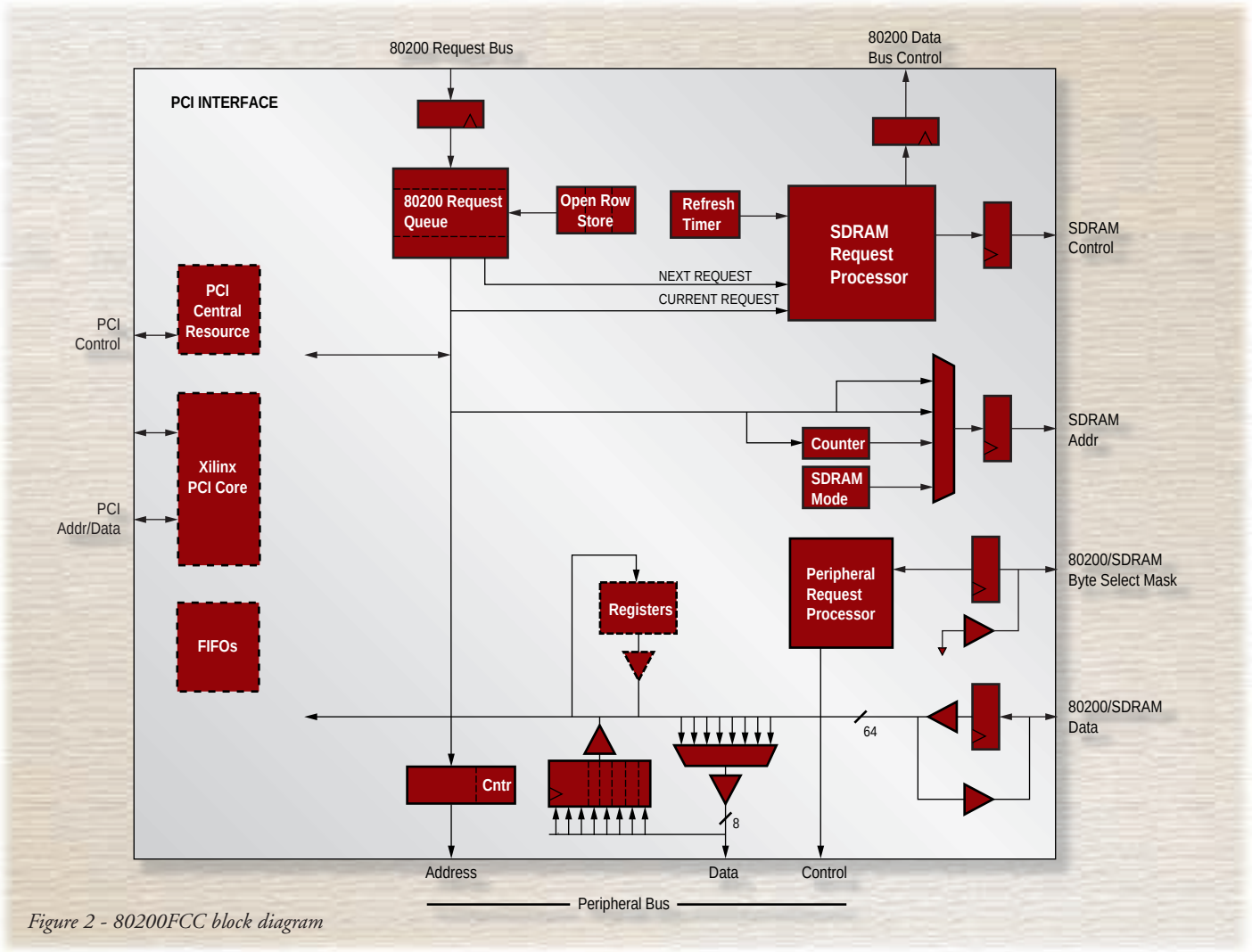



*Figure 2 - 80200FCC block diagram*

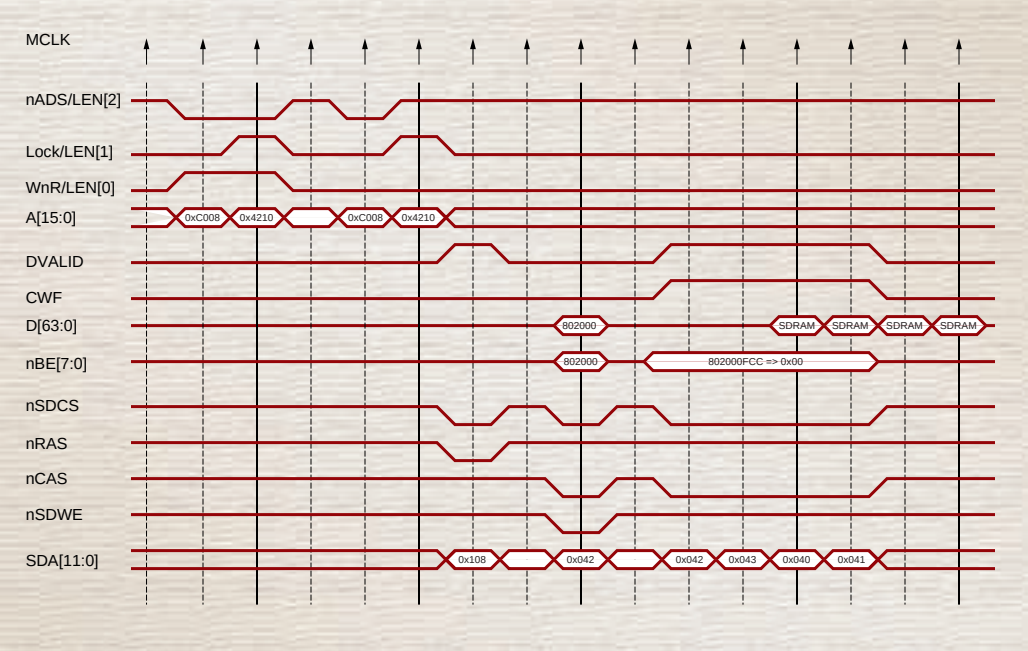



*Figure 3 - Typical 80200 SDRAM access (write to idle SDRAM bank followed by a 32-byte read)*

modified by changing VHDL constants and re-synthesizing the design.

A block diagram of the 80200FCC is shown in Figure 2.

A typical sequence of 80200 requests and corresponding SDRAM cycles is illustrated in Figure 3, which shows a write to an idle SDRAM bank followed by a 32-byte read.

### PCI Interface

The 80200EVB board design supports one 64-bit, 33 MHz PCI 2.2 slot, although the initial 80200FCC release does not support PCI. ADI Engineering is currently adding PCI functionality to the 80200FCC.

The Xilinx LogiCORE™ PCI64 interface for Spartan-II devices will provide the basis for the 80200FCC PCI interface. This Xilinx IP enables the 80200EVB to leverage the Spartan-II XC2S150 to provide a low-cost integrated PCI interface while still providing ample spare CLBs for future enhancements and customization.

### Peripheral Bus

A lower speed peripheral bus, separate from the 80200 100 MHz data bus, is provided by the 80200FCC for connection of flash memory and other peripherals. Because of the many different peripherals that could be connected to this bus, it is highly configurable. On the 80200EVB, the peripheral bus consists of an 8-bit data bus, four chip selects, read and write strobes, and 22 bits of address for 4 MB of address space per chip select. Peripheral bus data width, number of chip selects, wait state delays, and address space size are all configurable by modifying VHDL constants and re-synthesizing the design.

The 80200FCC performs data conversion between the 80200 processor and peripheral devices by steering data between the 8-bit peripheral bus and one of the eight byte lanes of the 80200 data bus, as shown in Figure 2. Byte lane selection is determined by the length and address of the peripheral bus request.

The 80200FCC peripheral bus interface handles any length 80200 read request (including 32-byte burst reads) by executing multiple peripheral accesses. Data are assembled in up to eight byte lane latches and returned in a single 80200 data cycle. For multi-byte reads, the peripheral bus address is incremented by a counter inside the 80200FCC. This counter supports the 80200 CWF protocol.

### Conclusion

The ADI Engineering 80200EVB is a high-performance reference design and evaluation platform for the Intel 80200 processor. The Xilinx Spartan-II family plays a key role by providing a high performance yet low cost solution for the 80200FCC companion chip, and the Xilinx LogiCORE PCI64 interface will further leverage the low cost 80200FCC to provide an integrated PCI interface.

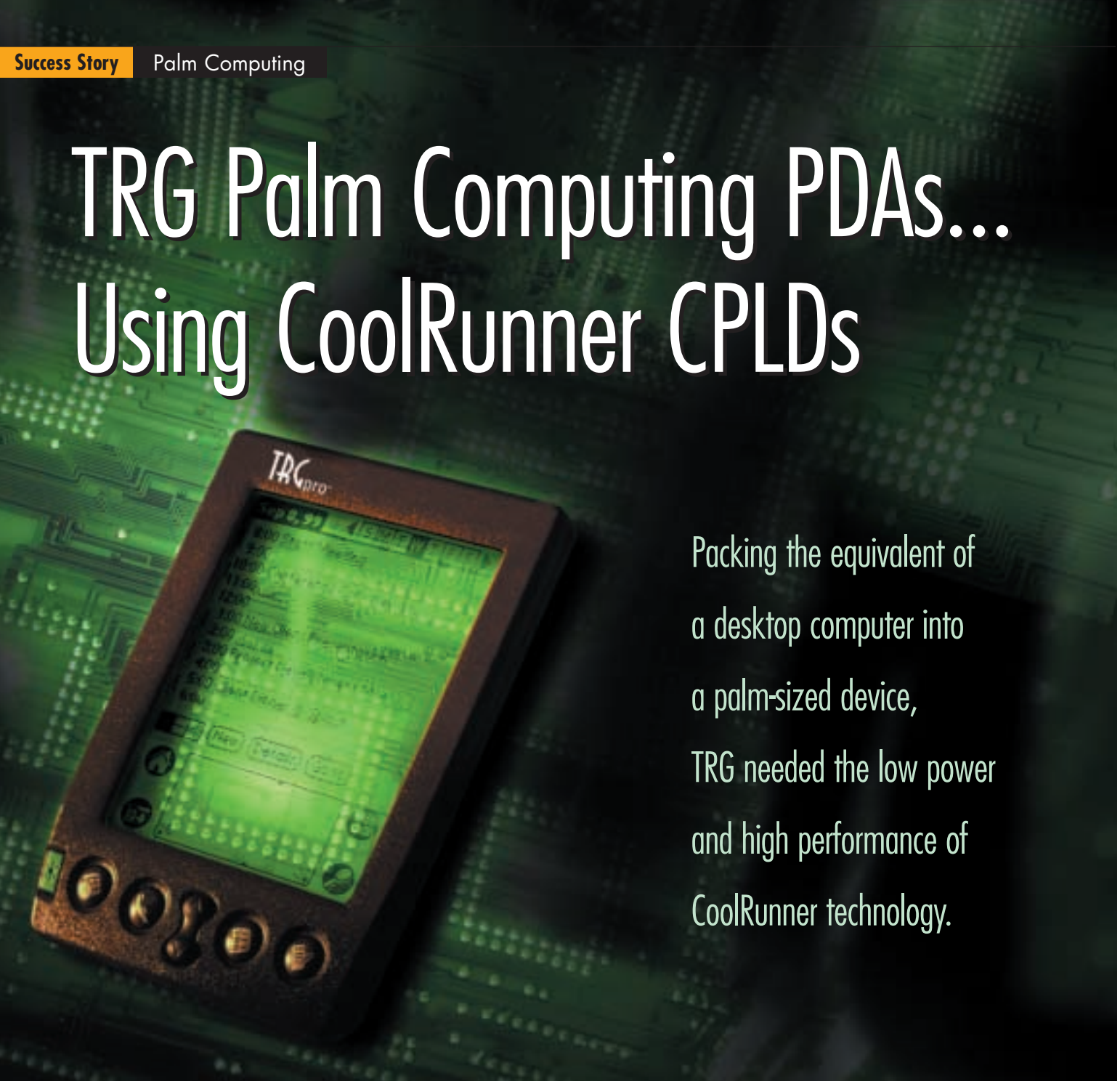
Design collateral for the 80200EVB and the 80200FCC is available free of charge to accelerate the time to market of custom 80200-based designs. You may obtain 80200EVB board schematic diagrams, 80200FCC VHDL source code, parts lists, and user documentation free of charge from Intel and ADI Engineering. Also, 80200EVB evaluation boards and custom design services are available from ADI Engineering.

### Ordering Information

**80200EVB evaluation boards may be ordered directly from ADI Engineering at 804-978-2888, ext. 1, or sales@adiengineering.com. Design collateral for the 80200EVB and the 80200FCC are available online at www.adiengineering.com.**

**ADI Engineering also is available to provide support and design services to develop custom solutions based on the Intel XScale microarchitecture. Additional information on the Intel XScale microarchitecture is available online at http://developer.intel.com /design/intelxscale/.**

# TRG Palm Computing PDAs... Using CoolRunner CPLDs




Packing the equivalent of a desktop computer into a palm-sized device, TRG needed the low power and high performance of CoolRunner technology.

by Tamara Snowden
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If there is a more demanding design challenge than cell phones, it's palm computing: Personal Digital Assistants, or PDAs. In developing these devices, you often face quick, repeated design changes. In addition, you need high-speed, small size, light weight, and very low power consumption – all applied to a product that has the power of a desktop computer in a tiny fraction of the volume and at a much lower price. In facing all these demands, one company, TRG Inc. of Des Moines, Iowa, found programmable logic devices from Xilinx to be a much better design solution than ASICs.

Think of TRG's TRGpro palm computer as a combination of drag racer and minivan. It's got speed and horsepower to spare, and plenty of storage space too. While retaining full compatibility with the PalmOS, the TRGpro adds quantities of memory almost unheard of in handheld computing: 8 MB of RAM and up to 16 MB of flash memory, on special order. The flash memory can be either onboard, or in removable modules (which present their own design challenges).

### Choosing the CoolRunner Family

Engineers usually expect maximum performance and minimum power consumption with custom ASICs. However, Xilinx CPLDs proved superior in TRG's designs, according to Douglas DeVries, vice president for hardware engineering. TRG has been

using the Xilinx Cool Runner family of CPLDs since 1997 and continues to do so today. They use a variety of models and sizes ranging from the XCR3032 to the XCR3256, all of which have excellent quiescent current drain – a key specification.

Although low current drain was a major consideration, DeVries says other factors weighed into TRG's choice of Xilinx CPLDs, including "their low and predictable pin-to-pin delay characteristics, low operating (as opposed to quiescent) power consumption, nonvolatility, in-system programmability, availability of both chip scale and TSOP packaging, and relatively low cost."

> "We highly recommend the CoolRunner family of devices from Xilinx. They have served us well in numerous designs. They continue to play an important role in removing the risk and shortening our development cycle."

### Very Low Power Consumption

The TRGpro's battery life in typical situations is twelve weeks, which means the device has minimal current drain. "The systems that we design typically have overall quiescent currents in the 100µA to 500µA range. Of that total, the CPLD might get budgeted 20µA to 50µA," said DeVries. "CoolRunner CPLDs are the only low-cost devices out there that allow us to realize these goals without using special shut-down modes, which complicate designs and increase system complexity."

### Lower Cost

Reducing system material costs for a consumer product like a PDA can mean hundreds of dollars at retail, where hitting the right price point can mean the difference between dominating a market niche and not even being a competitor. In using Xilinx programmable logic, TRG not only met its desired price point, but also enjoyed additional advantages only available with programmable logic – advantages like speed, ease of use, and reprogrammability. Flexibility in low-cost packaging is also a must for units like PDAs, so the Xilinx chip scale packaged devices were a definite plus.

Having used Cool Runner CPLDs since 1997 in a variety of products, from microstepping motors to complex image-capture systems, TRG realized that when it needed a memory controller for 8-MB memory boards for Palm Pilot computers, it could use CPLDs to great advantage. DeVries says that, "By using a CoolRunner device to generate the necessary DRAM address and control signals, we interfaced the Motorola 68328 DragonBall processor (used in the Palm computer) to inexpensive DRAM instead of more expensive SRAM – providing substantial savings in system memory cost."

### Reprogrammability

Reprogrammability was also an important factor in selecting Xilinx CPLDs, and in the development of TRG's products. According to DeVries, "Reprogrammabilty meant that we were able to move forward confidently with PCB layout once pin assignments and general functionality had been determined. This alone saved weeks in the schedule." And it wasn't just the design cycle that profited; Xilinx CPLDs helped TRG engineers speed through the beta testing and pre-production phases. "Once beta testing and pre-production began, we could quickly perform system updates to correct any problems that were reported. Even after production started, we made several small tweaks to the CPLD to improve performance or fix obscure problems."

### Multiple Uses

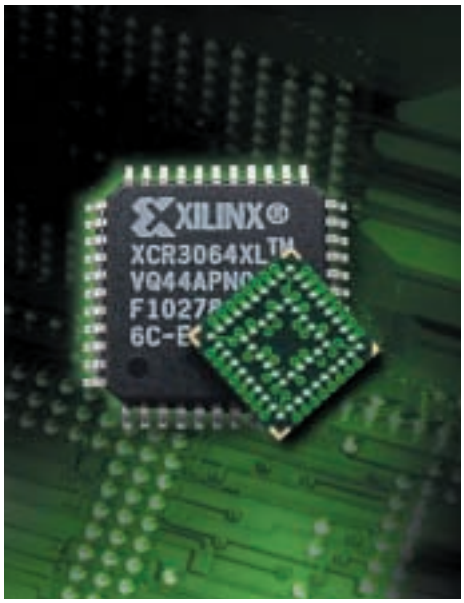
Due to the many advantages of CoolRunner technology, TRG not only uses Xilinx CPLDs in its Palm-compatible TRGpro PDA, but also in a variety of accessory and aftermarket devices: SuperPilot memory board family, XtraXtra and XXPro memory board lines, IDEO's PEG digital imager product for HandSpring, boards for the Visor PDA, and subsystems for certain models of 3Com's PalmPilot.

### Advantages over ASICs

Did TRG even consider ASICs? Yes, but the price-performance ratio was not attractive, and by their very nature, ASICs are not reprogrammable. According to DeVries, "We continue to consider ASICs for some designs. Once a product is really mature, all of the kinks have been worked out of the system, and things are ready to be cast in stone, ASICs can make sense and save money. However, in most of our applications, the difference in pricing between ASICs and CPLDs in high volume hasn't been compelling enough to make us switch to an ASIC. And since we tend to use the same CPLD device in multiple designs, we can aggregate CPLD volumes across product lines. This lowers CPLD unit price and decreases inventory risk because parts used in one product line that might be phasing out can be reprogrammed and used in a new product line – not so with an ASIC."

### Conclusion

"We highly recommend the CoolRunner family of devices from Xilinx. They have served us well in numerous designs," concluded DeVries. "They continue to play an important role in removing the risk and shortening our development cycle."



# Save Prime PCB Real Estate with Chip Scale Packaging

With innovative chip scale packaging, Xilinx CPLDs provide high speed, low power, and design density solutions.

by Frank Wirtz
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Size does matter when it comes to designing for space sensitive applications such as personal electronic equipment. As the industry leader in advanced packaging technology, Xilinx sells CPLDs (Complex Programmable Logic Devices) in CSPs (Chip Scale Packages) at competitive cost points. Xilinx was the first company in the programmable logic industry to offer CSPs in 0.8 mm BGA (Ball Grid Array) spacing (pitch) with the 9500 series of CPLDs. Now, Xilinx also offers 0.5 mm BGA spacing with the CoolRunner™ XPLA3 devices. These inexpensive CPLDs further decrease system costs by minimizing the amount of PCB (Printed Circuit Board) space and total system packaging required for any solution.

Because of the expensive nature of multiple layer, high speed digital PCBs, chip scale CPLDs provide cost-reduced solutions by consuming less real estate for any application, regardless of size. Consider the replacement of a 44-pin PLCC (Plastic Leadless Chip Carrier) package (PC44) by a 56-ball CSP with a 0.5 mm pitch (CP56). The CP56 solution requires only 11% of the space previously occupied by the PLCC package (Figure 1). Moreover, the CP56 provides 33% more user I/Os. (Ed. note: The CP56 has 48 user I/Os, and the PC44 has 36 user I/Os - thus, 33%.) Finally, CSPs offer reduced chip-to-chip delays (because the devices can be placed closer together), increased thermal performance, and higher reliability.

## Mount 'Em Up!

Designing PCBs for BGA packages requires a slightly different technique than typical surface mount components, but most PCB designers can learn the technique easily. Many pad geometries are used in the design and application of CSP solutions, from circular to diamond shaped mounting pads.

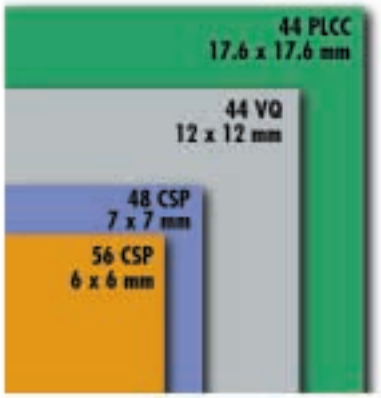


*Figure 1 - A 56 CSP (CP56) occupies 11% of the space of a 44 PLCC and offers 33% more I/Os.*

The circular pad is the preferred mounting method employed by most PCB designers today. Geometry details will be briefly provided here, but for additional information, obtain PDF copies of XAPP157 "Board Routability Guidelines with Xilinx Fine Pitch BGA Packages" (www.xilinx.com/xapp/xapp157.pdf) and Virtex Tech Topic "Xilinx Fine-Pitch BGA and CSP Packages: The Technological Edge" (www.xilinx.com/products/virtex/techtopic/bga_csp.pdf).

BGA packages come in two types of surface mount pads: SMD (Solder Mask Defined) and NSMD (Non Solder Mask Defined). As the names imply, these describe the way the copper is revealed on the surface of the PCB for solder attachment to the BGA package. SMD pads have portions of solder mask overlapping the pad; NSMD pads have an annulus of space around the perimeter of the pad (Figure 2).


*Figure 2 - Cross section of SMD and NSMD pads*

Xilinx recommends using NSMD pads be used. For a brief summary of the dimensions of the pads, refer to Table1. A note of cau-

| Pitch (mm) | Package | NSMD Pad (mm) | Thru Via (mm) | Via Capture (mm) | Inner Trace (mm) | Outer Trace (mm) | Space (mm) |
|---|---|---|---|---|---|---|---|
| 0.8 | CS280 | 0.33 | 0.30 | 0.50 | 0.1 | 0.127 | 0.120 / 0.100 |
| 0.8 | CS144 | 0.33 | 0.30 | 0.50 | 0.1 | 0.127 | 0.120 / 0.100 |
| 0.8 | CS48 | 0.33 | 0.30 | 0.50 | 0.1 | 0.127 | 0.120 / 0.100 |
| 0.5 | CP56 | 0.27 | 0.30 | 0.55 | 0.1 | 0.127 | 0.127 |

*Table 1 - Basic pad and layout geometries*

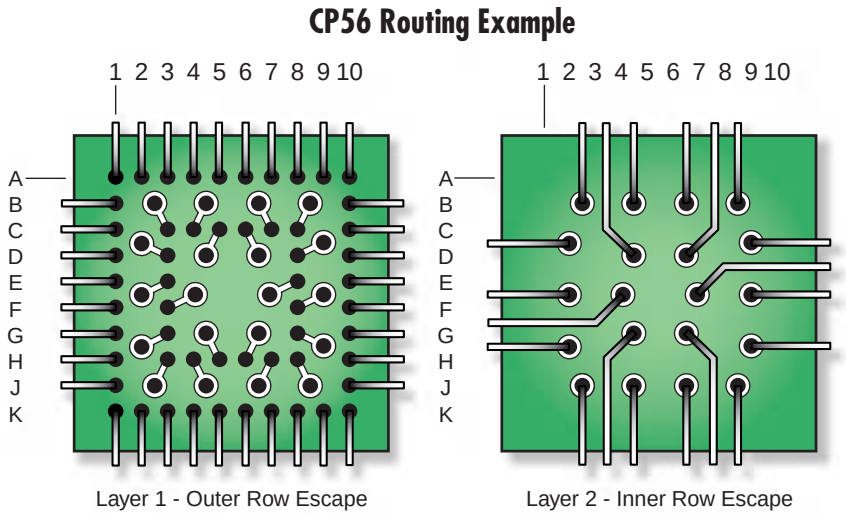


*Figure 3 - 56-ball grid array in a chip scale package*

tion: You should discuss the choice of the pad geometry, the width of the signal traces, and the solder mask/trace clearances with your PCB vendor to determine feasibility.

### Escape to Higher Reliability

CSPs provide higher reliability and performance. Their ball grid packages provide superior bonding integrity in applications subjected to vibration, flex, and thermal fluctuations. Ball grid packages are self-aligning during the soldering process, and they are naturally immune to manufacturing issues such as pin non-coplanarity and other pin-related damage. When it comes to routing a CSP device, Xilinx provides an access and escape pattern that is easy to use. Because the I/O signals are placed on the outer ring of the ball grid pattern (power and ground are typically positioned inside), the escape pattern is simple and straightforward (Figure 3).

### Don't Sweat the Heat

Due to the basic form factor of a BGA package, the solder balls mounted in a uniform array under the device help to dissipate heat from the CPLD and allow use of the PCB as a heat sink much more efficiently. Consider the 1.0mm quad flat package VQ44 volume (105 $mm^3$) compared with the CS48 package volume (66 $mm^3$) for the XC9536XL. Even though the CS48 device is significantly smaller than the VQ44 package (Figure 1), the thermal resistance of the CS48 is slightly less than the thermal resistance of the larger VQ44 package.

Refer to Table 2 for thermal resistances of some of the Xilinx CSP CPLD devices. Note that these values may be calculated rather than measured.

Using the thermal resistance ($\theta_{JA}$) of a package to calculate junction temperature is quite simple. Thermal resistances are given in (C/W degrees Celsius per Watt) dissipated. For junction temperatures, multiply the thermal resistance by the amount of power (in watts) dissipated by the device, and add in the ambient temperature. Note, this is valid for calculations in still air. If forced air-cooling is used, other thermal resistance values are available that are applicable to a flow rate. These flow rate related thermal resistances and other temperature and package information can be found at www.xilinx.com/partinfo/databook.htm#packages.

### Shrink Your Sockets, Not Your Options

As shown in Table 3, Xilinx already has almost a dozen CSP CPLDs in production, with plans to produce even more devices in space-saving chip scale packages. CSP CPLDs are being manufactured in both 0.8 mm (CS) and 0.5 mm (CP) ball grid spacing. Note the CS and CP designators (Figure 4) are used in the actual part numbers to designate package type. Refer to the device data sheets for information on creating the full part number.

Clearly, Xilinx CSP CPLDs are the product of choice for space conscious designers of personal and portable equipment. Just as clearly, they are the choice for engineers of any application requiring maximum performance, reliability, and cost efficiency under any conditions.

*Figure 4 -CS (0.8mm) and CP (0.5mm) CSP pitch designators are stamped on the CPLDs.*

| Device | CP56 | CS48 | CS144 | CS280 |
|---|---|---|---|---|
| XCR3064XL | 65°C / W | | | |
| XC9536 | | 45°C / W | | |
| XC9536XL | | 45°C / W | | |
| XC9572XL | | 45°C / W | | |
| XCR3128XL | | | 34°C / W | |
| XC95144XL | | | 34°C / W | |
| XC95144XV | | | 34°C / W | |
| XCR3256XL | | | | 30.5°C / W |
| XC95288XL | | | | 30.5°C / W |

*Table 2 - Thermal resistances of some Xilinx CSP CPLD devices*

| CS48 7 mm X 7 mm (0.8 mm pitch) | CP56 6 mm X 6 mm (0.5 mm pitch) | CS144 12 mm X 12 mm (0.8 mm pitch) | CS280 16 mm X 16 mm (0.8 mm pitch) |
|---|---|---|---|
| XC9536 | XCR3064XL | XC95144XL | XC95288XL |
| XC9536XL | | XCR3128XL | XCR3256XL |
| XC9572XL | | | |
| XCR3032XL | | | |
| XCR3064XL | | | |

*Table 3 - Xilinx chip scale package CPLDs are being manufactured in both 0.8 mm (CS) and 0.5 mm (CP) ball grid spacing.*

# Get the Most Out of Microcontroller-Based Designs: Put a Xilinx CPLD Onboard

## Partitioning your design over a CPLD and a microcontroller enhances speed and performance – and reduces system design costs and time to market.

by Karen Parnell
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Microcontrollers don't make the world go round, but they most certainly help us get around in the world. You can find microcontrollers in automobiles, microwave ovens, automatic teller machines, VCRs, point of sale terminals, robotic devices, wireless telephones, home security systems, and satellites, just to name a very few applications.

In the never-ending quest for faster, better, cheaper products, advanced designers are now pairing complex programmable logic devices (CPLDs) with microcontrollers to take advantage of the strengths of each. Microcontrollers are naturally good at sequential processes and computationally intensive tasks, as well as a host of non-time-critical tasks. CPLDs such as Xilinx CoolRunner™ devices are ideal for parallel processing, high-speed operations, and applications where lots of inputs and outputs are required.

Although there are faster and more powerful microcontrollers in the field, 8-bit microcontrollers own much of the market because of their low cost and low power characteristics. The typical operational speed of an 8-bit microcontroller is around 20 MHz, but some microcontroller cores divide clock frequency internally and use multiple clock cycles per instruction (operations often include fetch-and-execute instruction cycles). Thus, with a clock division of two and with each instruction taking up to three cycles, the actual speed of a 20 MHz microcontroller is divided by six. This works out to an operational speed of only 3.33 MHz.

CoolRunner CPLDs are much faster than microcontrollers and can easily reach system speeds in excess of 100 MHz. Today, we are even seeing CoolRunner devices with input to output delays as short as 3.5 ns, which equates to impressive system speeds as fast as 285 MHz. CoolRunner CPLDs make ideal partners for microcontrollers, because they not only perform high-speed tasks, they perform those tasks with ultra low power consumption.

Also, Xilinx offers free software and low cost hardware design tools to support CPLD integration with microcontrollers. The Xilinx CPLD design process is quite similar to that used on microcontrollers, so designers can quickly learn how to partition their designs across a CPLD and a microcontroller to maximum advantage.

So far, a design partition over a microcontroller and a CPLD sounds good in theory, but will it work in the field? We will devote the rest of this article to design examples that show how you can enhance a typical microcontroller design by utilizing the computational strengths of the microcontroller and the speed of a CoolRunner CPLD.

### Conventional Stepper Motor Control

A frequent use of microcontrollers is to run stepper motors. Figure 1 depicts a typical four-phase stepper motor driving circuit. The four windings have a common connection to the motor supply voltage (Vss), which typically ranges from 5 volts to 30 volts. A high power NPN transistor drives each of the four phases. (Incidentally, MOSFETs – metal oxide semiconductor field effect transistors – can also be used to drive stepper motors.)

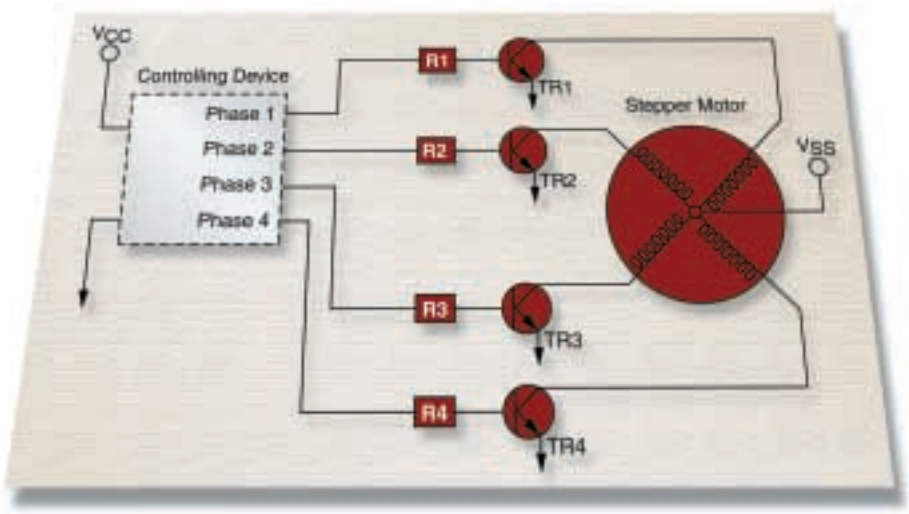


*Figure 1 - Stepper motor controller*

Each motor phase current may range from 100 mA to as much as 10 A. The transistor selection depends on the drive current, power dissipation, and gain. The series resistors should be selected to limit the current to 8 mA per output to suit either the microcontroller or CPLD outputs. The basic control sequence of a four-phase motor is achieved by activating one phase at a time.

At the low cost end, the motor rotor rotates through 7.5 degrees per step, or 48 steps per revolution. The more accurate, higher cost versions have a basic resolution of 1.8 degrees per step. Furthermore, it is possible to half-step these motors to achieve a resolution of 0.9 degrees per step. Stepper motors tend to have a much lower torque than other motors, which is advantageous in precise positional control.

The examples that follow show how either a microcontroller or a CPLD can be used to control stepper motor tasks to varying degrees of accuracy. We can see from Figure 2 that the design flow for both is quite similar.

Both flows start with text entry. Assembly language targets microcontrollers. ABEL (Advanced Boolean Expression Language) hardware description language targets CPLDs. After the text "description" is entered, the design is either compiled (microcontroller) or synthesized (CPLD). Next, the design is verified by some form of simulation or test. Once verified, the design is downloaded to the target device – either a microcontroller or CPLD. We can then program the devices in-system using an inexpensive ISP (in-system programming) cable.

One of the advantages of a CPLD over a microcontroller occurs during board level testing. Using a JTAG boundary scan, the CPLD can be fully tested on the board. The CPLD can also be used as a "gateway" to test the rest of the board functionality. After the board level test is completed, the CPLD can then be programmed with the final code in-system via the JTAG port.

(A JTAG boundary scan – formally known as IEEE/ANSI standard 1149.1_1190 – is a set of design rules, which facilitate testing, device programming, and debugging at the chip, board, and system levels.)

Microcontrollers can include monitor debug code internal to the device for limited code testing and debugging. With the advent of flash-based microcontrollers, these can now also be programmed in-system.

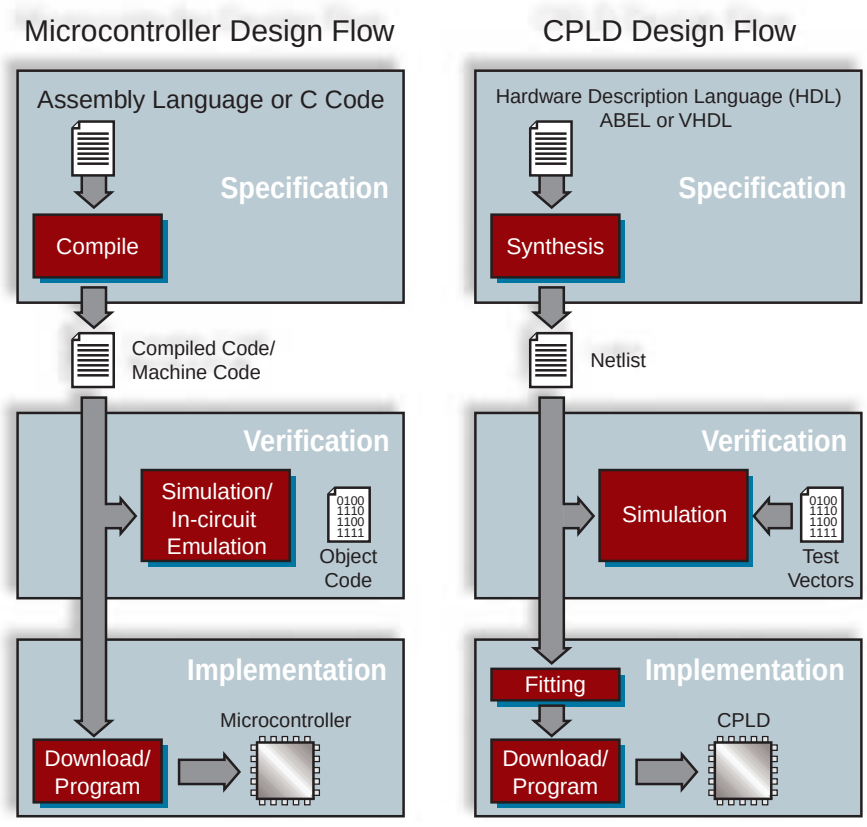


*Figure 2 - Design flow comparisons*

### Using a Microcontroller to Control a Stepper Motor

Figure 3 shows assembly language targeting a Philips 80C552 microcontroller. The stepper motor the microcontroller will control has four sets of coils. When logic level patterns are applied to each set of coils, the motor steps through its angles. The speed of the stepper motor shaft depends on how fast the logic level patterns are applied to the four sets of coils. The manufacturer's motor specification data sheet provides the stepping motor code. A very common stepping code is given by the following hexadecimal numbers:

A 9 5 6

Each hex digit is equal to four binary bits:

1010 1001 0101 0110

These binary bits represent voltage levels applied to each of the coil driver circuits. The steps are:

| | | | | |
|---|---|---|---|---|
| 1010 | 5V | 0V | 5V | 0V |
| 1001 | 5V | 0V | 0V | 5V |
| 0101 | 0V | 5V | 0V | 5V |
| 0110 | 0V | 5V | 5V | 0V |

If you send this pattern repeatedly, then the motor shaft rotates. The assembly language program in Figure 3 continually rotates the stepper motor shaft. By altering the value of R0 in the delay loop, this will give fine control over speed; altering the value of R1 will give coarse variations in speed.

```
$MOD552             ; include file for 80C552
      ORG 0    ; reset address
      SJMP START  ; jump over reserved area
      ORG 30H:program start address
START:   MOV P1,#0AH ;move hex 0A into lower
            ;4 bits of port 1
      ACAL DELAY  ;call subroutine step hold
            ;delay
      MOV P1, #09H       ;move hex 09 into lower
            ;4 bits of port 1
      ACALL DELAY
      MOV P1,#05H
      ACALL DELAY
      MOV P1, #06H
      ACALL DELAY
      SJMP START         ;repeat stepping pattern
                  ;
                  ;Double loop delay
DELAY:         MOV R1, #0FFH ;put hex FF into register 1
OUTER:         MOV R0, #0FFH ;put hex FF into register 0
INNER:   DJNZ R0, INNER;decrement r0 until it is 0
            DJNZ R1,OUTER;dec r1, go to outer until
                  ; r1 = 0
            RET ;return from subroutine
```

*Figure 3 - Assembly language program to rotate the stepper motor shaft*

### Stepper Motor Control Using a CPLD

Figure 4 shows a design written in ABEL hardware description language. Within the Xilinx CPLD, four inputs are required to fully control the stepper motor. The clock (clk) input synchronizes the logic and determines the speed of rotation. The motor advances one step per clock period. The angle of rotation of the shaft will depend on the specific motor used. The direction (dir) control input changes the sequence at the outputs (ph1 to ph4) to reverse the motor direction. The enable input (en) determines whether the motor is rotating or holding. The active low reset input (rst) initializes the circuit to ensure the correct starting sequence is provided to the outputs.

The phase equations (ph1 to ph4) are written with a colon and equal sign (:=) to indicate a registered implementation of the combinatorial equation. Each phase equation is either enabled (en), indicating that the motor is rotating, or disabled (!en), indicating that the current active phase remains on and the motor is locked. The value of the direction input (dir) determines which product term is used to sequence clockwise or counterclockwise. The asynchronous equations (for example, ph1.AR=!rst) initialize the circuit.

The ABEL hardware description motor control module can be embedded within a macro function and saved as a reuseable standard logic block, which can be shared by many designers within the same organization – this is the beauty of design re-use. This "hardware" macro function is independent of any other function or event not related to its operation. Therefore, it cannot be affected by extraneous system interrupts or other unconnected system state changes. Such independence is critical in safety systems. Extraneous system interrupts in a purely software-based system could cause indeterminate states that are hard to test or simulate.

```
MODULE step1
Title 'step1_abl'

Declarations
clk  PIN;     //input to determine speed of rotation
en   PIN;   //determines whether motor rotating or holding
dir  PIN;   //motor direction control
rst  PIN;   //resets & initialises circuit
ph1  PIN istype 'reg';       //output to motor phase 1
ph2  PIN istype 'reg';       // output to motor phase 2
ph3  PIN istype 'reg';       // output to motor phase 3
ph4  PIN istype 'reg' ;      // output to motor phase 4

Equations
//Stepper motor controller description
ph1 := !dir * en * (!ph1 * !ph2 * !ph3 * !ph4)
        + dir * en * (!ph1 * ph2 * !ph3 * !ph4)
        + !en * ph1;

ph2 := !dir * en * (!ph1 * !ph2 * !ph3 * !ph4)
        + dir * en * (!ph1 * ph2 * !ph3 * !ph4)
        + !en * ph2;

ph3 := !dir * en * (!ph1 * !ph2 * !ph3 * !ph4)
        + dir * en * (!ph1 * ph2 * !ph3 * !ph4)
        + !en * ph3;

ph4 := !dir * en * (!ph1 * !ph2 * !ph3 * !ph4)
        + dir * en * (!ph1 * ph2 * !ph3 * !ph4)
        + !en * ph4;

ph1.PR = !rst;
ph2.AR = !rst;
ph3.AR = !rst;
ph4.AR = !rst;

end step1
```

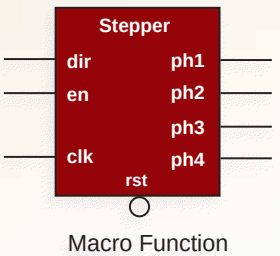


*Figure 4 - Using a CPLD to control a stepper motor*

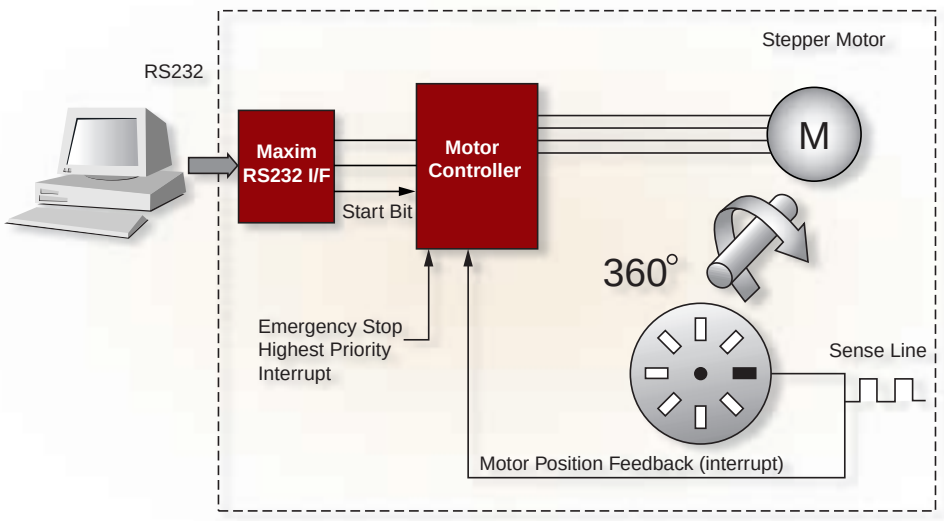


*Figure 5 - Design partitioning*

## PC-Based Motor Control

Our next example (Figures 5 and 6) is more complex, because now the motor is connected to a PC-based system via an RS232 serial connection. This implementation has a closed loop system controlling rotation, speed, and direction. There is also the addition of a safety-critical emergency stop, which has the highest level of system interrupt. This means that if the emergency stop is activated, it will override any other process or interrupt and will immediately stop the motor from rotating.

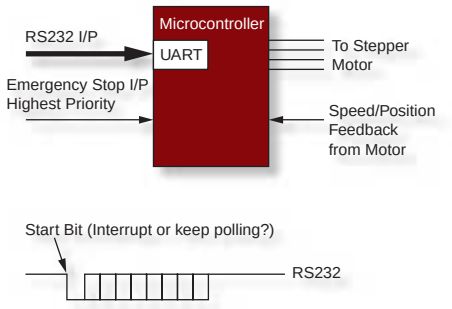


*Figure 6 - Microcontroller Implementation*

This design example uses only a microcontroller. The main functions it performs are:

- Interrupt control
- Status feedback to the PC
- Accurate motor control.

This configuration would probably be implemented in a single microcontroller device with specific motor control peripherals, such as a capture-compare unit. This configuration would also need a built-in UART (Universal Asynchronous Receiver Transmitter). These extra functions usually add extra cost to the overall microcontroller device.

Due to the nature of the microcontroller, the interrupt handling must be thoroughly mapped out, because interrupts could affect the speed of the motor. In a safety-critical system, emergency stops implemented in software require exhaustive testing and verification before they can be used in the final system to ensure that they operate properly under all software related conditions, including software bugs and potential software states. The output from the motor rotation sensor is very fast, so control of the speed of the motor could cause problems if system interrupts occurred.

## Design Partitioning

As we noted before, microcontrollers are very good at computational tasks, and CPLDs are excellent in high speed systems and have an abundance of I/Os. Figure 7 shows how we can use a microcontroller and a CPLD in a partitioned design to achieve the greatest control over a stepper motor.

The microcontroller:

- Interprets ASCII commands from the PC.
- Reports status of the motor to the PC.
- Converts required speed into control vectors (small mathematical algorithm).
- Decides direction of rotation of the motor.
- Computes stop point and sets a value into the pulse count comparison register.
- Monitors progress (control loop) and adapts speed.
- Recovers from emergency stops.

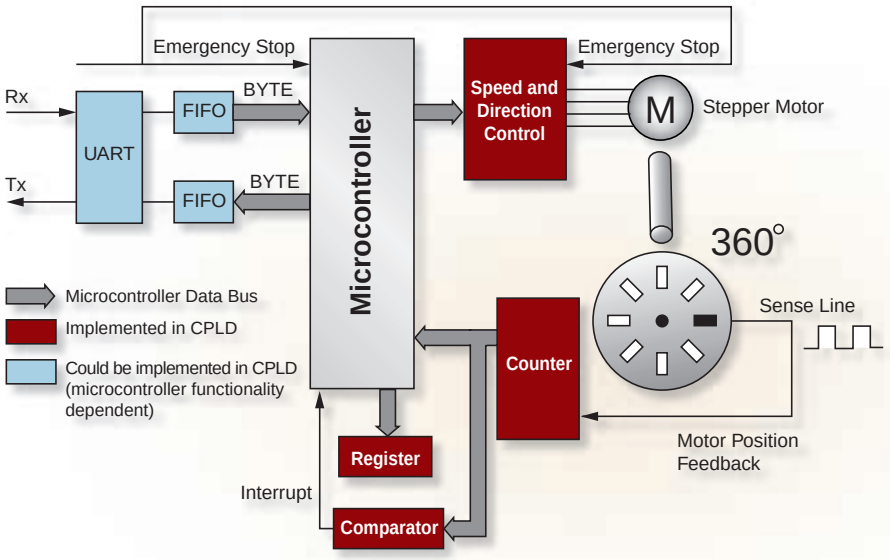


*Figure 7 - Partitioned Design: Microcontroller and CPLD*

Although the microcontroller performs recovery from emergency stops, the actual emergency stop is implemented by the CPLD, because this is the safety-critical part of the design. Because the CPLD is considered independent hardware, safety-critical proving and sign off are more straightforward than software safety systems. Additionally, all of the high-speed interface functions are also implemented in the CPLD, because it is very fast and has abundant inputs and outputs.

Meanwhile, the UART and FIFO (First in, First Out) sections of the design can be implemented in the microcontroller in the form of a costed microcontroller peripheral or may be implemented in a larger more granular programmable logic device like a field programmable gate array (FPGA) – for example, a Xilinx Spartan™ device. Using a programmable logic device in a design has the added benefit of the ability to absorb any other discrete logic elements on the printed circuit board or in the total design into the CPLD. Under this new configuration, we can consider the CPLD as offering hardware-based subroutines or as a mini co-processor.

The microcontroller still performs ASCII string manipulation and mathematical functions, but it now has more time to perform these operations – without interruption. The motor control is now independently stable and safe.

Microcontroller/CPLD design partitioning can reduce overall system costs. This solution uses low cost devices to implement the functions they do best – computational functions in the microcontroller and high speed, high I/O tasks in the CPLD. In safety-critical systems, why not put the safety critical functions (e.g., emergency stop), in hardware (CPLDs) to cut down safety system approval time scales?

System testing can also be made easier by implementing the difficult-to-simulate interrupt handling into programmable logic. Low cost microcontrollers are now in the region of US$1.00, but if your design requires extra peripherals (e.g., capture-compare unit for accurate motor control, analog-to-digital converters, or UARTs), this can quadruple the cost of your microcontroller. A low cost microcontroller coupled with a low cost CPLD from Xilinx can deliver the same performance – at approximately half the cost.

In low power applications, microcontrollers are universally accepted as low power devices and have been the automatic choice of designers. The CoolRunner family of ultra low power CPLDs are an ideal fit in this arena and may be used to complement your low power microcontroller to integrate designs in battery powered, portable designs (<100 µA current consumption at standby).

## Conclusion

Microcontrollers are ideally suited to computational tasks, whereas CPLDs are suited to very fast, I/O intensive operations. Partitioning your design across the two devices can increase overall system speeds, reduce costs, and potentially absorb all of the other discrete logic functions in a design – thus presenting a truly reconfigurable system.

The design process for a microcontroller is very similar to that of a programmable logic device. This permits a shorter learning and designing cycle. Full functioning software design tools for Xilinx CPLDs are free of charge and may be downloaded from the Xilinx website. Thus, your first project using CPLDs can not only be quick and painless, but very cost-effective.

***The following URLs provide detailed information on the topics and hardware discussed in this article:***

***Xilinx Website: www.xilinx.com***

***Xilinx CoolRunner CPLDs: www.xilinx.com/products/xpla3.htm***

***Xilinx Free CPLD design software: www.xilinx.com/products/software/webpowered.htm***



## Year 2001 Worldwide Xilinx Event Schedules

### Year 2001 North American Event Schedule

| | |
|---|---|
| April 10-12 | Embedded Systems Conference 2001<br>San Francisco, CA |
| April 22-26 | NAB 2001<br>Las Vegas, NV |
| April 30 - May 2 | FCCM 2001<br>Rohnert Park, CA |
| May 8-10 | ICASSP 2001<br>Salt Lake City, UT |
| May 8-10 | Networld + Interop Spring 2001<br>Las Vegas, CA |
| May 15-16 | Applied Computing Conference 2001<br>Santa Clara, CA |
| May 22 | Embedded Computing Show 2001<br>Phoenix, AZ |
| May 24 | Embedded Computing Show 2001<br>Albuquerque, NM |
| June 18-20 | 38th Design Automation Conference<br>Las Vegas, CA |
| June 24-27 | 2001 ASEE Conference & Expo<br>Albuquerque, NM |
| June 21-23 | WITI Technology Summit 2001<br>Santa Clara, CA |
| July 16-20 | NSREC 2001<br>Vancouver, BC |
| Aug 14-16 | Embedded Internet Conference 2001<br>San Jose, CA |
| Sept 2001 | SNUG 2001 Boston<br>Boston, MA |
| Sept 26-28 | MAPLD 2001<br>Johns Hopkins, MD |
| Oct 1-4 | Communication Design Conf. 2001<br>San Jose, CA |
| Oct 10-13 | Frontiers in Education 2001<br>Reno, NV |
| Oct 29-Nov 1 | NCF Infovision 2001<br>Chicago, IL |
| Oct 30 | Embedded Computing Show 2001<br>San Diego, CA |

### Year 2001 European Event Schedule

| | |
|---|---|
| May 16 - 17 | ESS 2001 - Embedded Systems Show<br>London, England |
| Oct 9 - 11 | Embedded Systems Conference<br>Stuttgart, Germany |

### Year 2001 Asia Pacific Event Schedule

| | |
|---|---|
| March 26-27 | IIC 2001<br>Shanghai, China |
| March 29-30 | IIC 2001<br>Beijing, China |
| April 2-3 | IIC 2001<br>Shenzhen, China |
| June 27-28 | IIC Expo 2001<br>Seoul, Korea |
| July 2-3 | IIC Expo 2001<br>Taipei, Taiwan |
| Oct 3-4 | EDA&T 2001<br>Hsinchu, Taiwan |
| Nov 2001 | Xilinx Technical Seminars 2001<br>Asia Pacific |

### Year 2001 Japanese Event Schedule

| | |
|---|---|
| June 2001 | Xilinx KK Expo 2001<br>Tokyo and Osaka, Japan |
| Nov 2001 | Xilinx Technical Seminars 2001<br>Japan and SE Asia |
| Nov 2001 | MST Fair 2001<br>Tokyo, Japan |

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# Synplicity Certify Software Integrates Xilinx ChipScope Debugging Tool

## An easy to use graphical interface makes it simple to conduct data signal probes.

by Brian Caslis
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Synplicity Certify™ 3.1 software now supports debug insertion for multiple FPGA-based ASIC prototypes via Xilinx ChipScope™ Tools. Figure 1 shows the current ChipScope usage model and which formerly manual steps are now handled automatically by Certify ASIC – prototyping software. ChipScope core generation – both ILA™ (Integrated Logic Analysis) and ICON™ (Integrated CONtrol) – and insertion are now automatic.

You can specify signals to be probed during or after partitioning. The procedure is similar to the current probe feature of the Certify software.

Figure 2 shows how ChipScope probes are organized into the Certify user interface. You can add ChipScope ICON cores to multiple FPGA configurations, but only one ICON core can exist per FPGA. The ICON core can have multiple ILA cores (up to a maximum of 15), and each ILA core can contain a set of signals to be probed (up to a maximum of 256 bits).

ILA cores can also have sections – one for the clock signal, one for the trigger signal(s), and one for the data signals (probed signals). The ILA core requires one clock signal, which must be related to the data being captured. When no unique trigger bus is specified, the data bus is used as the trigger. The data signals are the actual signal being probed. Dragging a signal into an ILA data signal section will enable its tracing through the ChipScope logic analyzer.

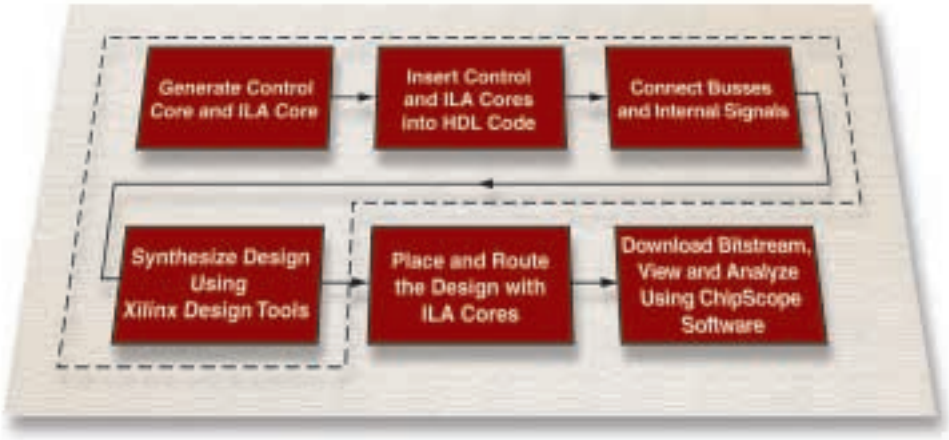


*Figure 1 - ChipScope flow handled by Certify software*

ChipScope Tools can generate and insert the ILA and ICON cores after all the partitioning is done. EDIF netlists will be created for each ILA and ICON core. They can be inserted into the design and connected using the information in the probe section of the partition information view. They can be marked as "black box," to be left untouched during the synthesis process. The EDIF files can be placed into the implementation directory.

By using the ChipScope integration with Synplicity Certify software, you can easily chose which signals to observe for debugging from an RTL (Register Transfer Level) view in an easy to use intuitive fashion.

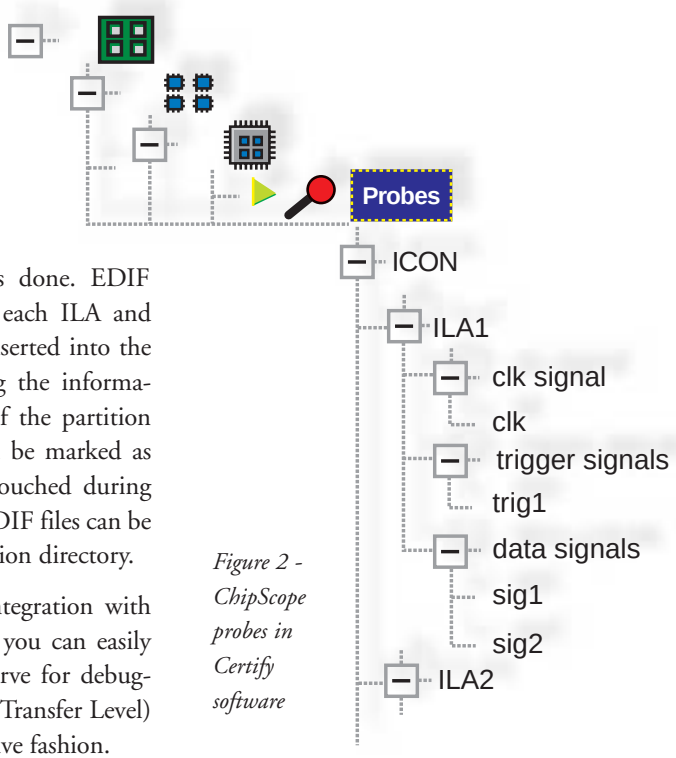


*Figure 2 - ChipScope probes in Certify software*

# Avnet Design Services Evaluation Kits Make It Easy to Design with Xilinx Products

## New kits for Spartan-II, Virtex-E, and CoolRunner architectures enable you to prototype and evaluate your designs quickly and easily.

by Warren Miller
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Whether it's consumer applications using the low power CoolRunner™ family, high-volume communications gear using the low cost Spartan™-II family, or network switching infrastructure using the high-capacity Virtex™-E family, Avnet Design Services (ADS) provides an evaluation kit that is right for virtually any application using Xilinx FPGAs and software.

### Spartan-II and Virtex-E Evaluation Kits

Both the Spartan-II and Virtex-E development boards feature a Xilinx XC18V01 serial PROM (SPROM), a digital thermometer, and a variety of I/O and breakout connectors. A demonstration program uses the digital thermometer to display the temperature in binary code on the boards' eight LEDs.

Also included in the kits are all the schematics, design files, demonstration code, and even the bill of materials used to create the evaluation board. This documentation shows the power-up circuitry, interconnect to ISPROMs, JTAG, and mode-selection pins – all the details you need to know to incorporate the evaluation board into your overall application design.

You can create your design on a PC and download it to either the FPGA or the SPROMs via a JTAG port download cable. This hands-on approach to familiarizing yourself with Xilinx FPGA architectures and products allows you to build confidence in your design and to verify that the parts you have selected will meet the goals of your application.

Special connectors have been added to the boards so you can access key portions of your application to interface, test, and verify your design. Three AMP Mictor connectors, compatible with Tektronix logic analyzers, provide high-speed signals you can use as stimulus and response to specific FPGA I/Os. Used in conjunction with the Xilinx ChipScope Integrated Logic Analyzer™ tool, these test points can display internal as well as external signals, making debugging even complex designs easier than ever.

Two 50-pin general-purpose header connectors provide access to additional signals and can be used to attach special purpose hardware to customize the boards for specific applications. You can use ribbon cables to connect the boards to additional data sources or destinations – or you can attach daughtercards directly to the Spartan-II or Virtex-E motherboards if signal integrity is important.

A 140-pin AVE (Avnet Vertical Expansion) bus connector on each board provides a way to attach the evaluation boards to other AVE-compliant boards. This allows a building block approach to hardware development. (See accompanying sidebar "AVE Bus Sets a Standard for Modular Design.")

The Spartan-II Evaluation Kit (Figure 1) hosts a Xilinx XC2S100-5PQ208 Spartan-II device. The Spartan-II kit costs US$249.

*Figure 1 - Spartan-II Evaluation Kit*

*Figure 2 - Virtex-E Evaluation Kit*

The Virtex-E Development System kit (Figure 2) uses a Xilinx Virtex-E XCV100E-6PQ240 device. The Virtex-E board also comes with a two-digit seven-segment liquid crystal display (LCD). The Virtex-E board with Xilinx Alliance Series™ software costs US$1,495. With Xilinx Foundation Series™ software, the Virtex-E board costs US$2,495.

### CoolRunner XPLA3 Evaluation Kit

The ultra low power CoolRunner family of FPGAs achieved fame and credibility in the programmable logic industry for their ability to function solely on the electricity generated by six grapefruit. The ADS kit fully supports a grapefruit power supply.

Because CoolRunner FPGAs consume so little power, the design of the development board is significantly different from the Spartan-II and Virtex-E kits. The ADS XPLA3™ Evaluation Kit (Figure 3) hosts a CoolRunner XCR3256XL-7TQ144 device, a low-power two-digit seven-segment LCD, a location for a 9V transistor battery (if grapefruit are out of season), JTAG programming header, and a prototype area. The kit comes with complete documentation, demonstration code, and a bill of materials for the board. The XPLA3 Evaluation Kit costs US$89.95.

### Other Complementary Kits from Avnet Design Services

Avnet Design Services also fabricates evaluation kits for popular microprocessors and microcomputers. The Intel StrongARM® development kit includes everything required to develop an Internet appliance. It contains a Xilinx Spartan-II FPGA that contains the Xilinx PCI core adapted by ADS to interface directly with the StrongARM processor bus.

Other ADS evaluation kits feature Motorola microprocessors, such as the 68HC908JL3 and 68HC908GP32. These complementary kits can be used in applications that require an "off-FPGA" processor for configuration or housekeeping control.

### Conclusion

The Xilinx-based evaluation kits from ADS provide a complete suite of hardware platforms for selecting, evaluating, and designing with any Xilinx FPGA family. And, to make it even easier, Avnet Design Services offers customer-training workshops on how to use the Xilinx evaluation kits and software. Visit the Avnet Design Services website at www.ads.avnet.com to find the costs, times, and places of workshops most convenient for you.

Avnet Design Services is the technical organization of Avnet, Inc, a leading global electronics distributor based in Phoenix, Arizona, United States. A Fortune 300 company, Avnet is one of the world's largest distributors of semiconductors, interconnects, passive and electromechanical components, and computer products from leading manufacturers, including Xilinx.

*Figure 3 - CoolRunner XPLA3 Evaluation Kit*

## AVE Bus Sets a Standard for Modular Design

**The Spartan™ -II and Virtex™ -E evaluation kits are compatible with the AVE (Avnet Vertical Extension) bus standard. This standard allows all AVE-compliant boards to interconnect using a high-performance "daughtercard" style connection. Boards can be added, like building blocks, to configure the exact platform required to develop even the most complicated design.**

**Avnet Design Services created the Virtex-E System Development Platform to serve as the motherboard to host this configuration of connectable hardware modules. The platform contains most of the major building blocks that applications require: Xilinx Virtex-E XCV1000E-6 logic device, 64-bit/33 MHz PCI connector (3.3V), PCI Mezzanine card, 64 MB Micron SDRAM, 32 MB flash memory, USB 2.0 PHY and connector, RS232 connector, controller area network (CAN) bus, 10/100 Ethernet PHY and connector, video encoder and decoder, and 24-bit stereo DAC.**

**Using an ADS evaluation kit with an AVE bus, you can:**

- **Plug in modules to provide processors, additional memory, modem, or DSP functions.**
- **Develop applications code and FPGA designs in parallel.**
- **Evaluate, integrate, and test complex IP cores, including multiple cores at the same time.**

**By customizing your own unique development platform with AVE-compliant boards, you can cut development time and accelerate time to market. For the most up-to-date information on this development methodology, visit the Avnet Design Services website at www.ads.avnet.com.**

# Use Multiple Configuration Bitstreams to Enhance Your Next FPGA-Based Design

Silver Engineering Inc. used multiple bitstreams to reduce test time and to provide versatility in their new VME Command Encoder Unit.

*Figure 1 - VCEU card with XCV400 FPGA and Configurator*

by Dennis Silver
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Silver Engineering Inc, and Configurator Inc.
silver@fpgaconfigurator.com

Most of us who have used fuse-based FPGAs really appreciate the forgiveness of reprogrammable RAM-based FPGA designs. But are you actually taking full advantage of the possibilities?

At Silver Engineering Inc., we recently developed a VME (VersaModule Eurocard) bus card specifically created for future field upgrades and design reuse. The VCEU (VME Command Encoder Unit) card (Figure 1) is primarily used as a ground-support satellite uplink/downlink (command/telemetry) processing card.

The VCEU is capable of generating both analog BPSK (Bi-Phase Shift Keyed) and AM/FSK (Amplitude Modulated/Frequency Shift Keyed) command formats. It incorporates a variety of digital I/O and on-card resources, allowing the card to emulate/test various spacecraft components during integration and test phases. Figure 2 illustrates the interface to the XCV400 on the VCEU card.

In this article, I will show how you can use multiple bitstreams to add extra value to your designs with minimal additional cost. To take full advantage of RAM-based FPGAs, consider the following three opportunities:

- Diagnostic/test bitfiles – To simplify board bring-up and test, you can implement multiple simple test designs. This accelerates hardware debugging, because the test hardware does not interfere with the system application hardware.
- Multiple bitfiles for different functionality or for reuse – You can use multiple bitstreams to perform completely different functions within a single card design. Moreover, these designs will not interfere with each other, and you can utilize the entire FPGA for each design.
- Easy field upgrades — Most engineers have had the experience of having to fix bugs or add features when a design is in the field. RAM-based FPGAs give you the flexibility of re-programmability so, with some planning, you may not have to make board modifications. Updating your design can be as easy as e-mailing a new bitfile.

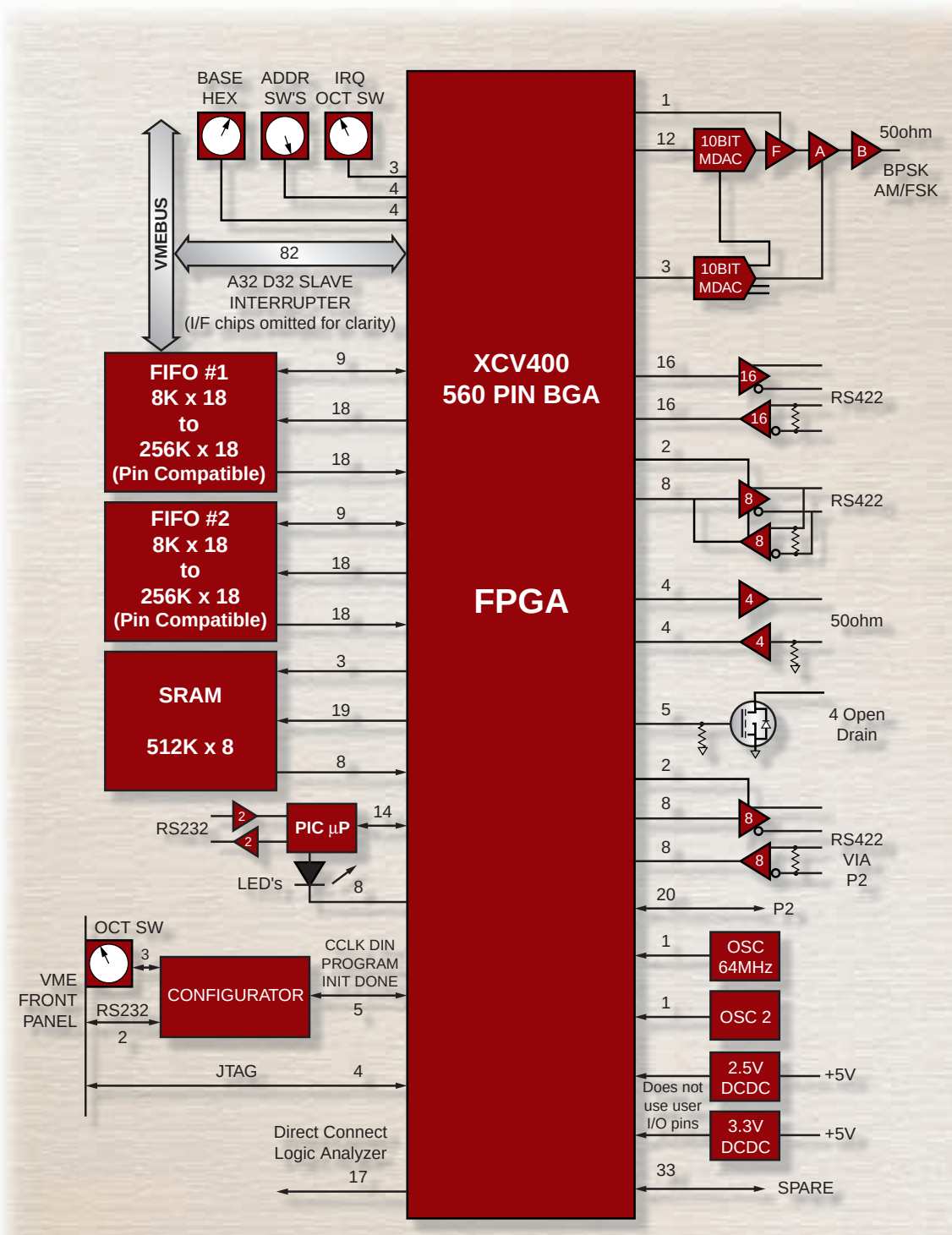


*Figure 2 - VCEU FPGA interfaces*

### Multiple Bitstreams Using the Configurator Module

The VCEU card incorporates a device called the Configurator. (See www.fpgaconfigurator.com for details.) We chose to use the Configurator module because it provides a prepackaged solution to storing multiple bitstreams. The Configurator programs up to eight FPGAs in parallel and can supply up to eight configuration bitfiles for each FPGA. The bitfiles are stored in reprogrammable flash memory. The size of the FPGAs and the number of different bitstreams for each are limited by the flash size.

The Configurator has an embedded serial port that can be utilized for field upgrades.

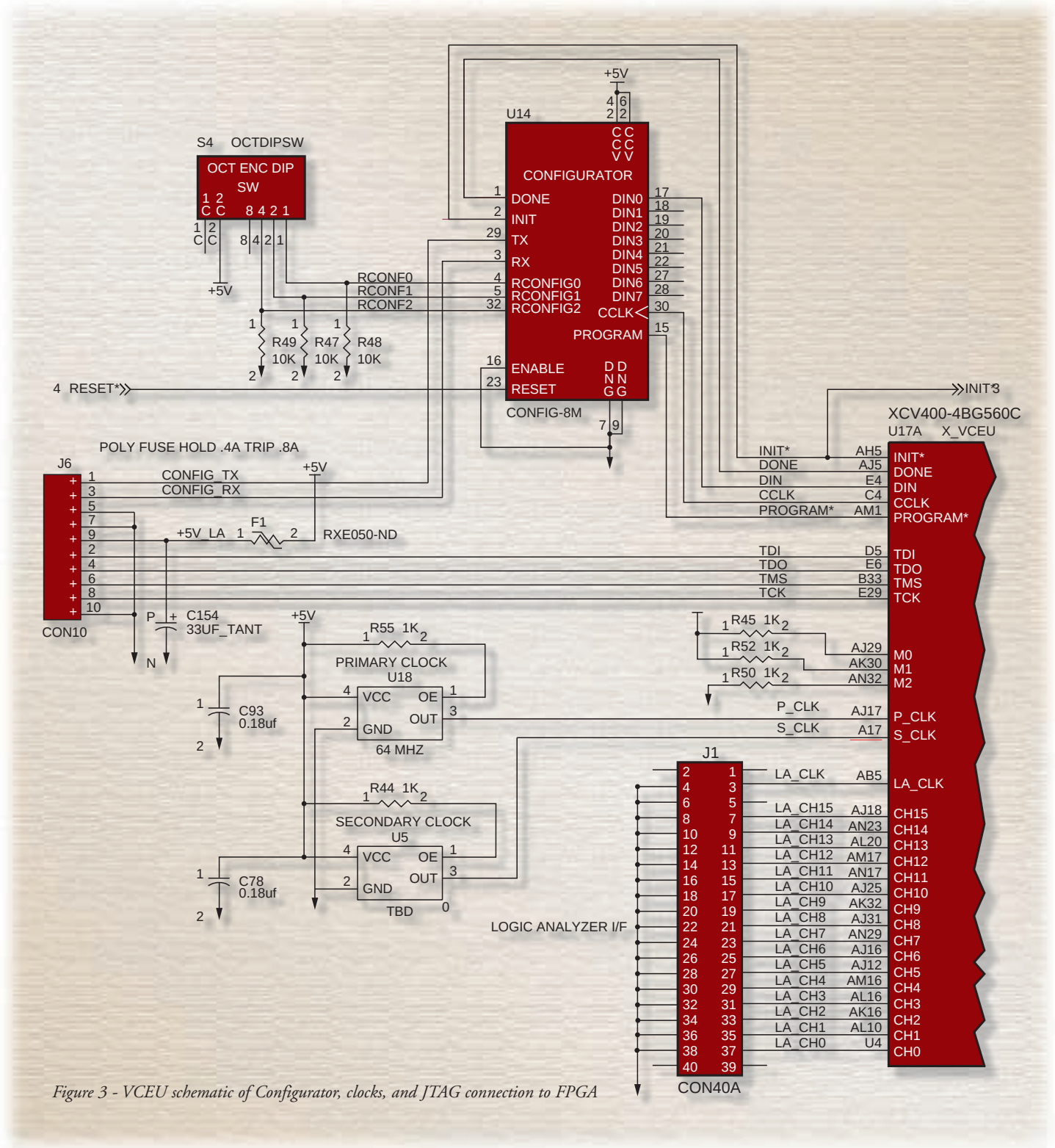


*Figure 3 - VCEU schematic of Configurator, clocks, and JTAG connection to FPGA*

The front panel of the VCEU card has an octal encoded rotary switch that connects to the Configurator and selects one of eight possible bitstreams to be loaded into the XCV400. In addition, the Configurator module's RS232 signals are connected to the VME front panel for easy downloading of new bitstreams from a field service laptop or any other device with a serial port. The VCEU card schematic of the Configurator interface is shown in Figure 3.

### Using Diagnostic/Test Bitfiles

Traditionally, we have tested circuit cards with only the card's main purpose in mind. In developing the VCEU, we took full advantage of multiple bitstream functionality for board bring-up and test.

A card that generates satellite uplink commands and receives downlink telemetry requires a lot of custom test equipment. To simplify basic testing of the VCEU card, we downloaded a series of diagnostic FPGA bitfiles into the Configurator module. The first set of diagnostic hardware files verified basic functions such as the front panel LEDs, hex rotary switches, and clocks feeding the FPGA. Once we had the basic functions confirmed, we used the LEDs switches as control and pass/fail indicators in complex diagnostic hardware tests. For example, we tested the SRAM, two large FIFOs, and drove test patterns for the D/A converters and other components. After all the diagnostic tests were completed, we then downloaded the "real" bitfile.

We retained all the previously used diagnostic bitfiles within the Configurator module on the VCEU card. To gain the maximum test coverage using diagnostic bitfiles, we connected most of the board's hardware to the FPGA. Additionally, we took some care to create complete signal paths so that signals driven out of the FPGA though the board hardware would be looped back into the FPGA for verification of signal integrity. By installing external loopback cables, we were able to check digital I/Os with a simple walking pulse test.

Along with diagnostic configuration files, we developed a configuration file for a built-in self-test. In the case of the self-test, which can happen at system power-up or on command, care must be taken so that the self-test does not interfere or conflict with external hardware from the board under test. This limits the self-test to testing only a portion of the board, but if you are creative with your board design (as we were), the only untested logic will be the input and output drivers.

### Multiple Functions for the Same Board

We specifically designed the VCEU board to allow different functions to be implemented in the future using the same physical hardware. For example, a future requirement might include the capability of driving signals out differentially. Because we incorporated differential drivers on the board along with the Xilinx FPGA, we will be able to support this new requirement without a costly board re-layout. The new design will just become another configuration bitstream selected by the front panel rotary switch.

To avoid the risk of premature obsolescence, when you are designing a new circuit board, ask yourself: "What other application might this board be required to do?" Then do a cost/benefit analysis of how much additional hardware would be needed on board to support the future scenarios. Remember, you don't necessarily have to have this additional hardware populated on the board. It might only be a matter of having enough board space and paying for a few extra board vias (plated through-holes in a printed circuit board).

### Easy Field Upgrades

Due to the often remote geographical locations of satellite ground stations, it is imperative that the FPGA can be easily updated to support feature additions or bug fixes. Therefore, the front panel of the VME card has a small connector that links to the Configurator module's serial port. When a new FPGA design is produced, the *.bit file is emailed to the designated field support personnel. Any on-site personnel can then simply connect the COM port of a laptop PC to the VME card front panel connector and download the new configuration file. The only disruption in service is the period of time that the FPGA is being reconfigured.

### Conclusion

With some careful planning, you can optimize your designs for now — and for the future — by using devices like the Configurator and reprogrammable Xilinx FPGAs. Multiple configuration files offer on-board support for diagnostic/testing, multiple functions utilizing the same card, and easy field upgrades. Make yourself a hero in your next design and do some "reconfigurable computing."


## About Silver Engineering, Inc.

**Silver Engineering Inc. (SEI) specializes in the design of hardware for spacecraft flight and ground-support systems utilizing Xilinx FPGAs.**

**Dennis Silver is president of Silver Engineering Inc. and vice president of Configurator Inc.**

**For more information, visit www.silvereng.com and www.fpgaconfigurator.com.**

# Clock Multiplication in Virtex-E and Virtex-II FPGAs

## How to set up clock multiplication into Virtex-E and Virtex-II devices using VHDL or Verilog hardware description languages and Synplify synthesis software.

by Howard Walker
Technical Marketing Engineer, Xilinx
howardw@xilinx.com

CLKDLLs (Clock Delay-Locked Loops) circuits can be used in a variety of applications ranging from clock multiplication and division to phase shifting and clock deskewing. In this article, we will show you how to implement clock multiplications in both Virtex™-E and Virtex-II devices using either VHDL or Verilog™ code and Synplify™ logic synthesis software.

The CLKDLLs components on the Virtex-E device have four primary and four secondary CLKDLLs. The secondary CLKDLLs have dedicated feedback loops that can be used to generate a 4X clock using only one BUFG (global clock buffer). Virtex-E devices have four clock networks that can be used to create different clock configurations. The primary/secondary CLKDLLs must be located in the same quadrant (top right, top left, bottom right, or bottom left) to create a 4X clock.

The Virtex-II devices offer even more versatility than the Virtex-E FPGAs. The Virtex-II devices have from four to twelve DCMs (Digital Clock Managers) depending on the device size. The DCM not only offers enhanced support for all DLL functionality found in Virtex-E devices, but the DCM also provides flexible frequency synthesis, precise fine-grained phase shifting, and spread spectrum clock generation. Virtex-II devices contain 16 global clock multiplexers and buffers that can be used with the DCMs to create different clock configurations. A DCM with a BUFG and an IBUFG (dedicated input clock pad) can be used to generate a 7X clock.

### Set Up a 4X Clock in a Virtex-E FPGA

The VHDL and Verilog™ code examples on the next page show how to implement a 4X clock for use in a Virtex-E device. The circuit includes two CLKDLLs (one primary and one secondary), an IBUFG, a SRL16 (shift register look-up table) and inverter for the reset control signal, and a BUFG used for the feedback from the primary CLKDLL.

The SRL16 is used to delay the reset signal to the second CLKDLL (the primary DLL), so that it will stay in reset until the first CLKDLL (the secondary DLL) has achieved a "lock" on the input clock. This insures that the second CLKDLL is sourcing a stable clock from the first CLKDLL to produce a clock signal that is 4X the frequency of the CLKIN (clock input) signal.

In all the examples in this article, we used Synplify logic synthesis software from Synplicity™ Inc.

If location constraints are required for the CLKDLLs and the associated input clock, these can be specified in a UCF (User Constraints File). Only one of the CLKDLLs or its associated global clock buffer or clock pad needs to be given a location constraint in the UCF. The Xilinx 3.1i Alliance Series™ software (or later release) will automatically place the other CLKDLL, IBUFG, or BUFG in the same quadrant (lower right, lower left, upper right, or upper left). The following constraints will place the CLKDLLs in the lower left quadrant of a Virtex-E device:

```
#UCF with LOCs for DLLs, IBUFG
and BUFG for dll_4x example

inst dll2x LOC = DLL1S;

inst dll4x LOC = DLL1P;
```

### Virtex-E DLL 4X VHDL Example

```
library ieee;
use ieee.std_logic_1164.all;
—Include your vendor-specific library references for running synthesis
software here

entity dll_standard is
      port (CLKIN, RESET : in  std_logic;
      CLK2X, CLK4X, LOCKED : out std_logic);
end dll_standard;

architecture structural of dll_standard is


component IBUFG
      port (O : out std_logic;
      I : in std_logic);
end component;

component CLKDLL
      port(CLKIN, CLKFB, RST: in std_logic;
      CLK0, CLK90, CLK180, CLK270, CLK2X, CLKDV, LOCKED : out
      std_logic);
end component;

signal CLKIN_w, RESET_w, CLK2X_dll, CLK2X_g, CLK4X_dll,
CLK4X_g : std_logic;
signal LOCKED2X, LOCKED2X_delay, RESET4X: std_logic;
signal logic1 : std_logic;

begin

      logic1 <= '1';

      clkpad : IBUFG  port map (I=>CLKIN, O=>CLKIN_w);

      rstpad : IBUF   port map (I=>RESET, O=>RESET_w);

      dll2x  : CLKDLL port map (CLKIN=>CLKIN_w,
            CLKFB=>CLK2X_g,
            RST=>RESET_w, CLK0=>open, CLK90=>open,
            CLK180=>open,
            CLK270=>open, CLK2X=>CLK2X_dll, CLKDV=>open,
            LOCKED=>LOCKED2X);

      clk2xg : BUFG   port map (I=>CLK2X_dll,   O=>CLK2X_g);

      rstsrl :      SRL16  port map (D=>LOCKED2X, CLK=>CLK2X_g,
                  Q=>LOCKED2X_delay, A3=>logic1, A2=>logic1,
                  A1=>logic1, A0=>logic1);

      RESET4X <= not LOCKED2X_delay;

      dll4x  :      CLKDLL port map (CLKIN=>CLK2X_g,
                  CLKFB=>CLK4X_g, RST=>RESET4X, CLK0=>open,
                  CLK90=>open, CLK180=>open, CLK270=>open,
                  CLK2X=>CLK4X_dll, CLKDV=>open,
                  LOCKED=>LOCKED);

      clk4xg : BUFG   port map (I=>CLK4X_dll,  O=>CLK4X_g);

      CLK2X <= CLK2X_g;

      CLK4X <= CLK4X_g;

end structural;
```

### Virtex-E DLL 4X Verilog Example

```
//
//Include your synthesis vendor-specific library references here

module dll_standard (CLKIN, RESET, CLK2X, CLK4X, LOCKED);

input CLKIN, RESET;

output CLK2X, CLK4X, LOCKED;

      wire CLKIN_w, RESET_w, CLK4X_dll, LOCKED2X,
      LOCKED4X;

      wire LOCKED2X_delay, RESET4X;

      wire logic1;

      assign logic1 = 1'b1;

      IBUFG clkpad (.I(CLKIN), .O(CLKIN_w));

      IBUF  rstpad (.I(RESET), .O(RESET_w));

      CLKDLL dll2x (.CLKIN(CLKIN_w), .CLKFB(CLK2X),
                  .RST(RESET_w), .CLK0(), .CLK90(), .CLK180(),
                  .CLK270(),  .CLK2X(CLK2X),
                  .CLKDV(),.LOCKED(LOCKED2X));

      SRL16  rstsrl (.D(LOCKED2X), .CLK(CLK2X),
                  .Q(LOCKED2X_delay),.A3(logic1),.A2(logic1),
                  .A1(logic1), .A0(logic1));

      assign RESET4X = ~LOCKED2X_delay;

      CLKDLL dll4x (.CLKIN(CLK2X), .CLKFB(CLK4X),
                  .RST(RESET4X), .CLK0(), .CLK90(),.CLK180(),
                  .CLK270(), .CLK2X(CLK4X_dll), .CLKDV(),
                  .LOCKED(LOCKED));

      BUFG   clk4xg (.I(CLK4X_dll),  .O(CLK4X));

endmodule
```

### Set Up a 7X Clock in a Virtex-II FPGA

The following VHDL and Verilog code examples show how to implement a 7X clock multiplication in a Virtex-II device. In these examples, attributes of the DCM are passed in the hardware description language code. Alternatively, they could be specified in the UCF.

The input clock first goes through an IBUFG component and then to the CLKIN pin of the DCM. The CLK0 pin from the DCM is connected to a BUFG, and this output feeds back to the CLKFB input pin of the DCM. Using the BUFG to connect the CLK0 output pin to the CLKFB input pin is only required if you want to have the CLKFX output phase-aligned with the CLK0 output. If this is not required, then the BUFG resource (and the power it consumes) can be saved for other uses. In order to create the desired frequency, two attributes are assigned to the DCM in the source code. These are the "CLKFX_MULTIPLY" (assigned a value of "7") and "CLKFX_DIVIDE" (assigned a value of "1"). These attributes can be any value between 1 and 4,096 as long as the input frequency is from 1-300 MHz and the output frequency is from 24-300 MHz.

As with the examples before, we used the Synplify logic synthesis engine.

### Using the CLKDLL and DCM in Simulations

The following hints will help guarantee the CLKDLL or DCM simulation will work correctly:

- The simulation resolution time must be set to display in pico-seconds as part of the simulation setup. In VHDL, the simulator resolution is set within the simulator. When running Verilog, set the following timing specification at the top of the main Verilog source code:
  `timescale 1 ns / 1 ps
- The simulation must run long enough for the LOCKED output signal of the Virtex-E CLKDLL and the Virtex-II DCM to go high. The CLKDLL hardware in Virtex-E using an input clock

### Virtex-II VHDL DCM/DLL Example

```
library IEEE;

use IEEE.std_logic_1164.all;

- - Include your synthesis vendor-specific library references here

entity clock_distribution_block is

      port (CLK_IN, RST_DLL : in std_logic;
      CLK7X, LOCKED : out std_logic);

end clock_distribution_block;

architecture STRUCT of clock_distribution_block is

attribute CLKFX_MULTIPLY : string;

attribute CLKFX_DIVIDE   : string;

attribute CLKFX_MULTIPLY of U2 : label is "7";

attribute CLKFX_DIVIDE of U2 : label is "1";


signal CLK, CLK_int, CLK_dcm, CLKFX_int, LCK_int, RST_int: std_logic;

signal DUMMY : std_logic := '0';

component IBUFG

      port (I : in  std_logic;  O : out std_logic);

end component;

component BUFG

      port (I : in  std_logic; O : out std_logic);

end component;

component DCM is

      port (CLKFB,CLKIN,DSSEN,PSCLK,PSEN,PSINCDEC,RST : in std_logic;
            CLK0,CLK90,CLK180,CLK270,CLK2X,CLK2X180,CLKDV,
            CLKFX,CLKFX180,LOCKED,PSDONE      : out std_logic;
            STATUS  : out std_logic_vector (7 downto 0));

end component;

begin

      U1 : IBUFG port map (I => CLK_IN, O => CLK_int);

      U2 : DCM port map (CLKIN => CLK_int, CLKFB => CLK,
            RST => RST_int, DSSEN  => DUMMY, PSINCDEC => DUMMY,
            PSEN => DUMMY, PSCLK => DUMMY, CLK0 => CLK_dcm,
            CLKFX => CLKFX_int, LOCKED => LCK_int);

      U3 : BUFG port map (I => CLK_dcm, O => CLK);

      RST_int <= RST_DLL;

      CLK7X <= CLKFX_int;

      LOCKED <= LCK_int;

end architecture STRUCT;
```

**Virtex-II Verilog DCM/DLL Example**

```
//Include your synthesis vendor-specific library references here

module clock_distribution_block

(CLK_IN,RST_DLL,CLK7X,LOCKED);

      input    CLK_IN, RST_DLL;

      output   CLK7X, LOCKED;

wire     CLK, CLK_int, CLK_dcm;

IBUFG U1  (.I(CLK_IN), .O(CLK_int));

DCM U2  (.CLKFB(CLK), .CLKIN(CLK_int), .RST(RST_DLL),          DSSEN(1'b0),
          .PSINCDEC(1'b0), .PSEN(1'b0), .PSCLK(1'b0),
.CLK0(CLK_dcm),
          .CLK90(), .CLK180(), .CLK270(), .CLK2X(), .CLK2X180(),
          .CLKDV(), .CLKFX(CLK7X), .CLKFX180(), .LOCKED(LOCKED))
          /* synthesis CLKFX_MULTIPLY=7 CLKFX_DIVIDE=1 */;

BUFG U3 (.I(CLK_dcm), .O(CLK));

endmodule // clock_distribution_block
```

If location constraints are required for the DCM, they can be specified in a UCF. In the following example, the DCM is placed in the upper left quadrant of 2v40 device:

```
#UCF with LOCs for DCM for Virtex-II DCM/DLL example

inst U2  LOC = DCM_X0Y1;
```

running at 40-50 MHz will take up to 50 microseconds to achieve a lock signal. (Refer to the DLL clock tolerance, jitter, and phase information in the *Xilinx Data Book 2000* for more information. *The Data Book* is online at www.xilinx.com/partinfo/databook.htm.)

The DCM in a Virtex-II device will exhibit similar lock times as the CLKDLL in Virtex-E, with the exception of the use of CLKFX and CLKFX180 outputs. If these outputs are used, the lock times may be significantly shorter or longer, with a maximum of a few milliseconds for very large CLKFX_MULTIPLY attribute values. When run in a simulator, such as ModelSim XE™, the LOCKED output signal of the CLKDLL and the DCM will go high approximately 1 microsecond after the reset signal goes from high to low.

- The CLKDLLs and DCM must also be run within certain frequencies to adhere to the timing specs. (Refer to the *Xilinx Data Book 2000* for the timing specs of the Virtex-E DLL and the *Virtex-II Platform FPGA Handbook* for the timing specs of the DCM.)

In order to run a simulation on these VHDL and Verilog examples, the Virtex-E or Virtex-II library references must be included. In the VHDL example, to prevent compiler problems when the VHDL is run through your chosen synthesis software, you must add the following lines in between the "translate_off" and "translate_on" statements:

```
library unisim;

use unisim.vcomponents.all;
```

In the Verilog examples, an "`include" statement is needed to reference the path to the Virtex-E or Virtex-II libraries. In addition, a global Verilog file must be referenced and compiled in the simulator (glbl.v). Refer to "XAPP108" (www.xilinx.com/xapp/xapp108.pdf) or the "Synthesis and Simulation Design Guide" (toolbox.xilinx.com/docsan/3_1i/).

**Conclusion**

DLLs and DCMs offer great flexibility for clock management in demanding designs. Just make sure you refer to the specifics in your vendor's synthesis tool when using attributes in HDL designs.

***For additional information about using CLKDLLs to generate or manage various clock signal configurations, refer to "XAPP132" (www.xilinx.com/xapp/xapp132.pdf).***

# Celoxica Implements "Soft Hardware" in Internet Reconfigurable MultiMedia Terminals

## Xilinx FPGAs enable rapid deployment of reconfigurable "soft hardware" over the Internet.

by Ranjith Kumaran
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*Figure 1 - MultiMedia Terminal*

So, you want your video game console to play MP3s, and you wish you could send your voice over the Internet using that digital audio appliance. Is it too much to ask one device to do it all? We don't think so. This article details the development of a flexible multimedia device with hardware that can be reconfigured over a network connection and that can run software applications built directly into silicon.

We call the platform we developed for this purpose an MMT (MultiMedia Terminal –Figure 1). The MMT features no dedicated stored programs and no CPU. It has no operating system, and the applications that it runs in hardware are kept on a server rather than on the board itself. Instead, programs are implemented in field programmable gate arrays. With FPGAs, you can control peripherals and process data to mimic CPU flexibility using only reconfigurable logic and a software design methodology.

FPGAs can be used to host "soft hardware" that runs applications without the overhead associated with microprocessors and operating systems. Such hardware can be totally reconfigured over a network connection to install program enhancements and fixes – or a completely new application.

Hardware platforms populated by FPGAs can stave off premature obsolescence because they are able to support evolving standards, as well as applications not imagined when the platform was designed. This soft hardware model also allows manufacturers to use Xilinx IRL™ (Internet Reconfigurable Logic) to remotely access and maintain their hardware designs at any time, regardless of where the MMT units reside.

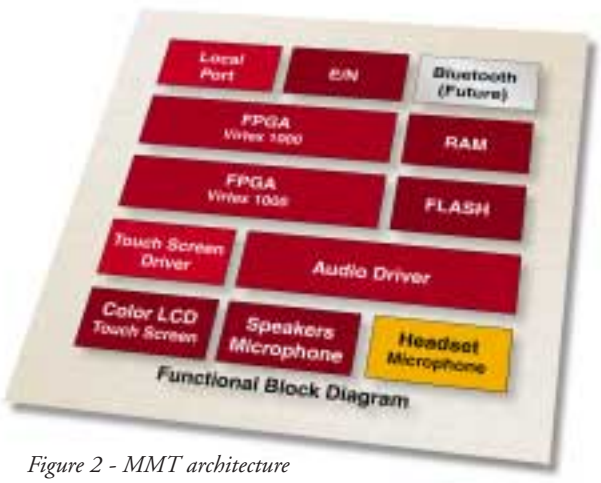


*Figure 2 - MMT architecture*

### Master/Slave Architecture Enables Reconfigurability

The MMT achieves reconfigurability by using two independent, one million-gate Xilinx XCV1000 Virtex™ FPGAs (Figure 2). One of the FPGAs – the master – remains statically configured with networking functionality when the device is switched on. The other FPGA – the slave – is reconfigured with data provided by the master. The two FPGAs communicate directly via a 36-bit bus with 4 bits reserved for handshaking and two 16-bit unidirectional channels. This protocol ensures that reliable communication is available even when the two FPGAs are being clocked at different speeds. The other components of the MMT are an LCD touch screen, audio chip, 10-Mbps Ethernet interface, parallel and serial ports, three RAM banks, and a single nonvolatile flash memory chip.

FPGA reconfiguration can be performed by using one of two methods. The first method implements the Xilinx SelectMAP™ programming protocol on the master FPGA, which can then program the slave. The second method supplies reconfiguration data from the network interface or from the flash memory on the MMT.

Reconfiguration from flash memory is used only to load the GUI (Graphical User Interface) for a VoIP (Voice-over-Internet Protocol) telephone into the slave FPGA upon power-up, when an application has finished, or when configuration via the network fails.

Network-based reconfiguration uses HTTP (HyperText Transfer Protocol) over a TCP (Transmission Control Protocol) connection to a server. A text string containing a file request is sent by the MMT to the server, which then sends back the reconfiguration data (a bitfile).

It's all well and good to have a flexible architecture that can run your application-of-the-day in an FPGA, but how do you write all those applications and how do you do it in a reasonable amount of time?

HDLs (Hardware Description Languages) are well suited for creating interface logic and for defining hardware designs with low-level timing issues. However, networking, VoIP, MP3s, and video games - that almost sounds like software. ...

### Getting a Handel–C on "Soft Hardware"

To meet the challenges of the system described above, the MMT was designed with a language called Handel-C™, which is featured in the Celoxica™ DK1 software design suite for reconfigurable hardware. The Handel-C language extends ANSI-C for efficient hardware implementation. If you are familiar with C software development, you can learn Handel-C quickly.

The Handel-C extensions support parallelism, variables of arbitrary width, and other features familiar in hardware design, but Handel-C very much targets software design methodologies (Figure 3). Unlike some of the other C-based solutions out there that translate C into an HDL, the Handel-C compiler directly synthesizes an EDIF (Electronic Design Interchange Format) netlist in a format that can be immediately placed and routed, and put onto an FPGA as soft hardware.

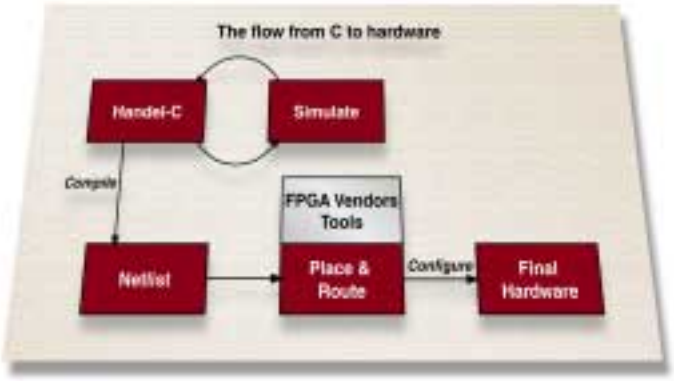


*Figure 3 - Handel-C design flow*

The default application that runs on the MMT upon power-up is a VoIP telephone complete with GUI. The VoIP consists of a call state machine, a mechanism to negotiate calls, and an RTP (Real Time Protocol) module for sound processing. A combination of messages from the GUI and the call negotiation unit are used to drive the call state machine. The protocol implemented by the call negotiation unit is a subset of H.323 Faststart (including H.225 and Q.931). This protocol uses TCP to establish a stream-based connection between the two IP (Internet Protocol) telephones. The RTP module is responsible for processing incoming sound packets and generating outgoing packets sent over UDP (User Datagram Protocol).

### Pipeline to Success

The development team consisted of four Celoxica engineers. It took the team only three weeks to get the VoIP prototype to send and receive voice calls. Algorithms for protocols such as RTP, TCP, IP, and UDP were derived from existing public domain C sources. The team optimized the source code to use features available in Handel-C, such as parallelism. Parallelism is useful for network protocols that generally require fields in a packet header to be read in succession and that can usually be performed by a pipeline with stages running in parallel. Each stage was tested and simulated within a single Handel-C environment. Once each stage tested okay, it was put directly into hardware by generating an EDIF netlist. The development team was able to quickly perform further optimizations and tuning simply by downloading the latest version onto the MMT over the network.

In order to demonstrate the flexibility of the architecture and to take advantage of Internet reconfigurability, the team developed a mixed bag of applications. These applications all run successfully in hardware on the MMT. Among them are a fully functional MP3 player with GUI, several video games, and some impressive graphics demonstrations that were all developed using Handel-C. These applications are hosted as bitfiles on a server that supplies these files upon demand from the user of the MMT over a network connection.

Three software engineers using Handel-C and one board designer took the MMT design from specification to hardware in just three months – a near impossible schedule using alternative hardware development methods. The final design included a TCP/IP stack that used about 48% of an XCV1000 Virtex device (13% of which could be moved off the FPGA into external or block RAM). A simple video game used 2% of an XCV1000, and the MP3 decoder used about 80% of an XCV1000.

Because the MP3 design implemented many pipeline stages in parallel, it required only an 8 MHz clock to perform real-time decoding. The MMT developers believe they can reduce the size of the decoder dramatically given time for further optimizations.

*To find out more about the rapid design capabilities of Handel-C, the DK1 software design suite for reconfigurable hardware, and the MMT architecture, visit Celoxica Inc. at www.celoxica.com.*

# Build Scalable DSP Systems with Nallatech DIME Modules Populated by Virtex-E FPGAs

By their nature, FPGAs are ideal for DSP systems that must grow and evolve on demand.

by Derek Stark
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Today's digital signal processing systems often require significant performance and resources beyond the capability of traditional DSP processor-based architectures. FPGAs offer quick turnaround, high performance, and reconfigurable technology. Therefore, FPGAs are finding applications in HDTV, base stations, and other high-speed DSP communications systems because of their distinctive combination of performance and flexibility.

Even high-end DSP systems can benefit further from parallel FPGA architectures, which introduce scalability into your system architecture. Scalable systems must cope with high I/O and processing bandwidth requirements, dynamic configurations, and real world interfaces. Implementing parallel FPGA configurations from the outset ensures your DSP systems will meet future demands and maximize silicon performance. Traditional DSP processors just can't keep up.

## High Speed DSP Development Platform

DIME™ (Dsp and Image processing Module for Enhanced fpgas) is an open modular standard from Nallatech Ltd. that provides the framework for a scalable systems approach, making it particularly suitable for high speed DSP applications. As shown in Figure 1, a fundamental example of a FIR/FFT (Finite Impulse Response/Fast Fourier Transform) processing combination demonstrates how DIME modules can be utilized to construct a multiple FPGA-based DSP system.

The system can be implemented on a Ballynuey2 DIME motherboard populated with two DIME modules – the Ballyriff and the BallyDAC. A high-level configuration tool for the Ballynuey2 carries out the configuration of the FPGA devices fitted to the two DIME modules and thus allows configuration of multiple FPGAs in a system.

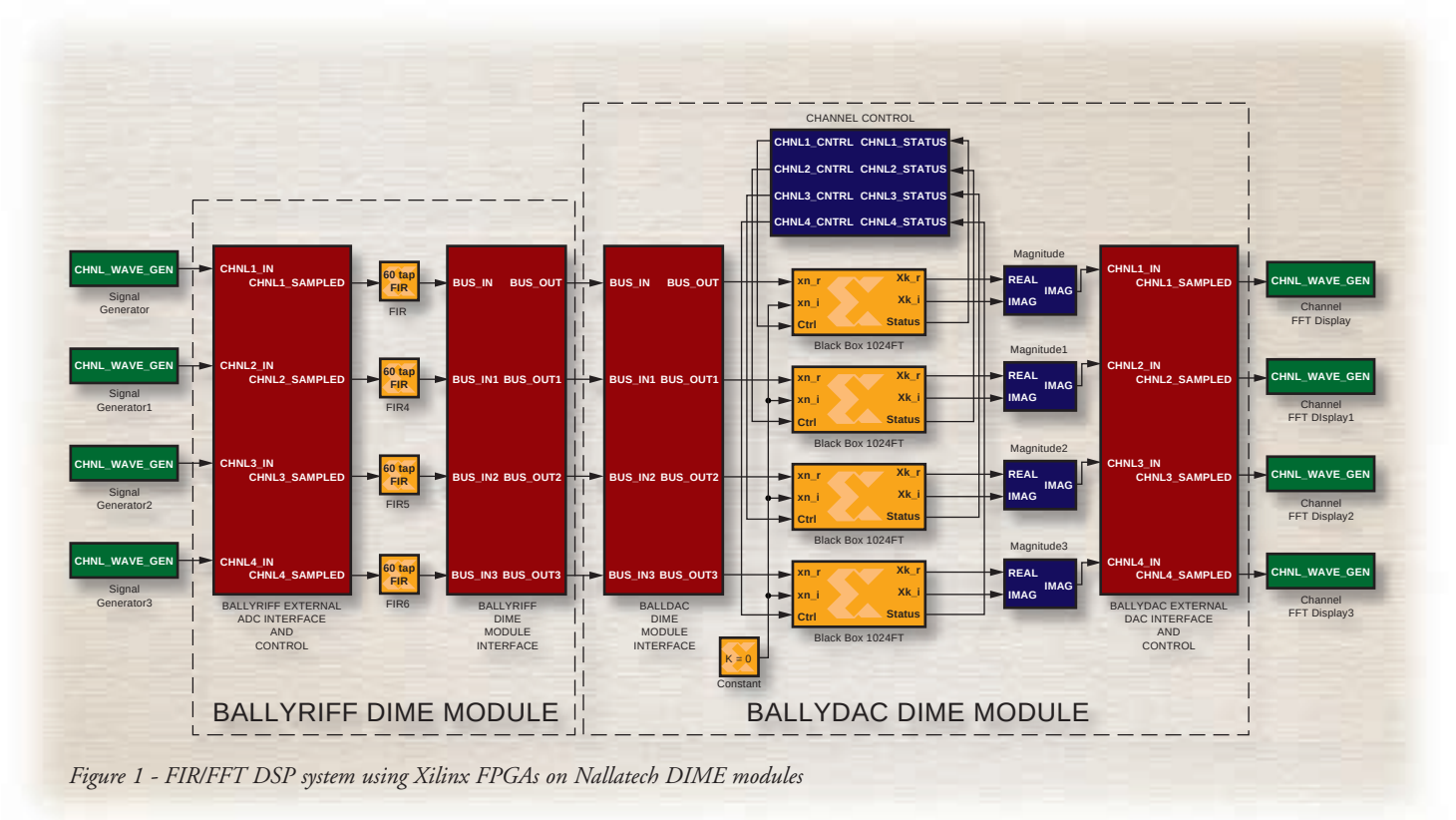


*Figure 1 - FIR/FFT DSP system using Xilinx FPGAs on Nallatech DIME modules*

As shown in Figure 2 (block diagram) and Figure 3 (actual module), the Ballyriff provides four 12-bit ADC (Analog to Digital Converter) channels, 100 MSPS (Mega Samples Per Second) conversion rate, 128 MB SDRAM for data storage, and can be

*Figure 2 - Ballyriff block diagram*

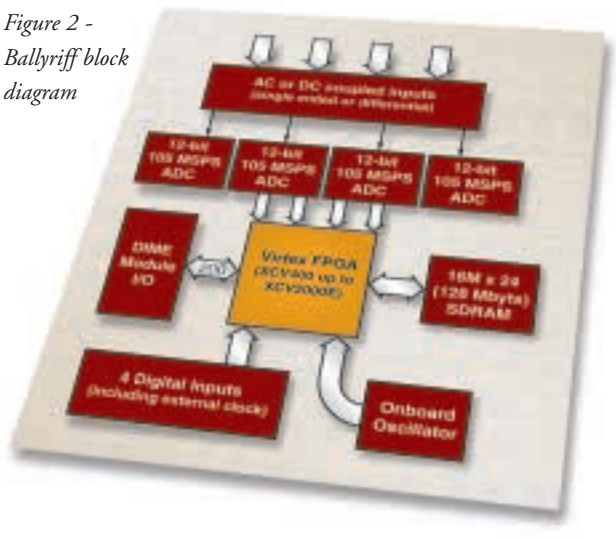


*Figure 3 - Ballyriff 4-Channel 100 MSPS 12-bit ADC DIME module*

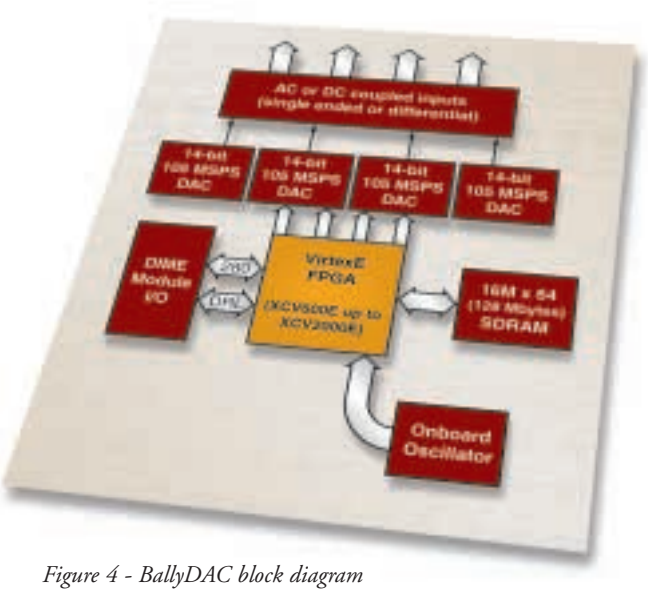


*Figure 4 - BallyDAC block diagram*

*Figure 5 - BallyDAC 4-Channel 150 MSPS 14-bit DAC DIME module*

fitted with up to a Virtex™ XCV2000E device (a XCV1000 FPGA is shown here). The Virtex-E FPGA can handle the 600 MB/S (MegaBytes per Second) of I/O bandwidth required to process the data from the ADCs. A 60-tap FIR filter is implemented for each input channel (Figure 1) to provide pre-filtering and noise reduction in the application. The processed data is passed to the adjacent BallyDAC module over the high-speed bus structures available on the Ballynuey2 motherboard.

The BallyDAC DIME module, shown in Figure 4 (block diagram) and Figure 5 (actual module), complements the specifications of the Ballyriff and provides four 14-bit DACs (Digital to Analog Converters), a 150 MSPS conversion rate, 128 MB of SDRAM for storage, and can be fitted with up to a Virtex XCV2000E FPGA to provide the required I/O and processing bandwidth for the DACs. (Figure 5 shows a Virtex XCV1000E device.) The Virtex-E FPGA is configured with a design that carries out a 1,024-point FFT and magnitude calculation, for simple frequency spectrum analysis, on each of the four channels of the captured data that is passed from the Ballyriff DIME module. The resulting magnitude output from the BallyDAC can then be used for further processing or subsequently displayed in real time.

The FFTs are configured in a triple-memory space configuration, and the four channels make full use of the 96 BlockRAM™ available in the XCV1000E device. This highlights just some of the key architectural features of today's FPGAs that prove their suitability for high speed DSP applications.

## The DSP Design Challenge

The example system in Figure 1 can be constructed from standard DSP cores from Xilinx. Although these cores can be combined through additional levels of VHDL (Very High Speed Integrated Circuit ((VHSIC)) Hardware Description Language), newer tools, such as the Xilinx System Generator™ for The MathWorks' Simulink™ program, allow designs to be created by DSP engineers without extensive VHDL knowledge.

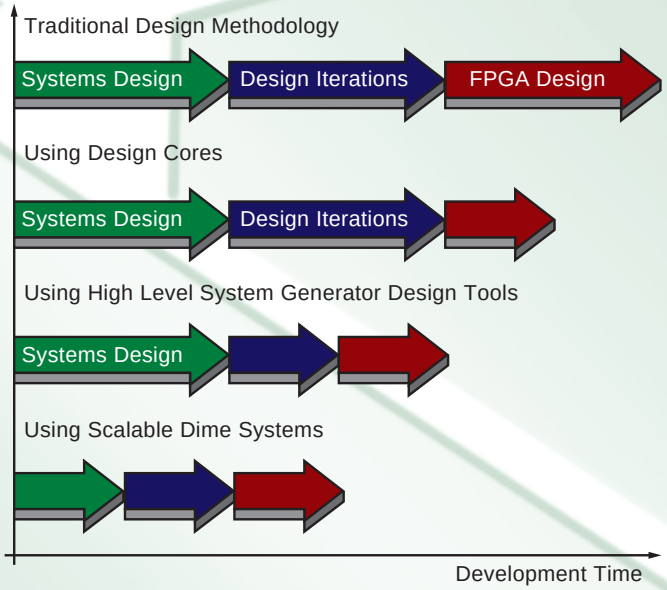


*Figure 6 - Development Time*

Although FPGAs support the increasing performance requirements, growing complexity, and shorter developments time of today's DSP design challenges, there is still a clear need for a suitable hardware platform to cope with the required external devices and interfaces – and the possibility of partitioning the platform for a multiple FPGA solution. DIME modules from Nallatech provide such a hardware platform. The Ballyriff and BallyDAC boards are just two examples of DIME modules that are particularly suitable for high performance DSP applications. The scalable platform architecture of DIME modules further reduces the development time of systems as illustrated in Figure 6.

## Conclusion

Today, system designers require suitable tools, development platforms, and hardware to efficiently create complex high performance DSP systems. Systems that can provide the flexibility of high speed DAC and DSP functionality with the advantages of FPGA resources and a reduced development time are ideal for DSP designers. The advent of tools, such as System Generator from Xilinx and The MathWorks, will ease the development of these DSP systems, aiding the migration of DSP designers to FPGA-based platforms in a familiar environment.

***For the latest information on the new Ballynuey3 DIME motherboard and how it uses Virtex-II devices to support encryption and IP protection, visit www.nallatech.com.***

# FUSE—Field Upgradeable Systems Environment

## Nallatech Ltd. offers a "circulation system" to link FPGA platforms with board platforms.

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Xilinx's "Platform FPGA" initiative provides a visionary way forward for the development of a new generation of embedded systems. The Virtex-II™ family of FPGAs are at the heart of the initiative with many new and flexible features from an extensive range of hard and soft intellectual property. Nallatech – a Xilinx XPERTS Partner – has consolidated its board level systems expertise and is complementing the Xilinx effort with the Nallatech systems framework called FUSE™. This "Field Upgradeable Systems Environment" framework provides the fusion between silicon systems and hardware systems, allowing accelerated time to market and in-field support.

### The FUSE Design Environment

The FUSE system was initially devised in 1998 as the first system framework to provide greater support to designers who require a distributed FPGA platform. Combined with a highly scalable board platform, the FUSE framework allows the rapid creation of new end products.

As illustrated in Figure 1, the FUSE system has evolved out of the proven framework used by the award-winning DIME (Dsp and Imaging Module for Enhanced fpgas) platforms. (For more information on DIME technology, see "Build Scalable DSP Systems with Nallatech DIME Modules" in this issue of *Xcell Journal*.) DIME-based platforms offer very flexible and scalable modular systems for FPGA-based product development. The goal of the FUSE framework is to provide product systems engineers with the following key benefits:

- **Intelligent hardware** – for Plug and Play
- **Harness latest FPGA developments** – to support Virtex-II family of FPGAs
- **Multiple platform support** – for Windows, Linux, etc.
- **Scalable systems** – to support high end applications
- **Flexibility** – to accelerate time to market
- **High performance and bandwidth** – for high speed communications
- **Field upgradeablity** – to streamline product support
- **Proven technology** – for risk reduction.

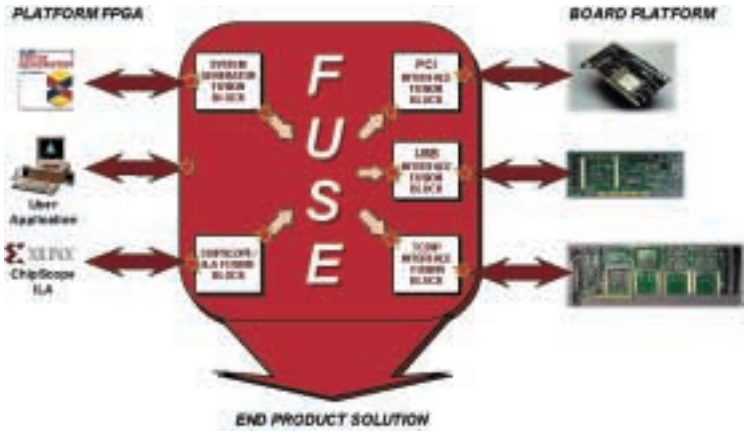


*Figure 1 - FUSE: the fusion of the FPGA platform and the board platform*

### Systems Silicon and Systems Hardware Fusion

The FUSE framework is the circulation system for linking the features currently available for the FPGA platform to those available on a board platform. The FUSE system allows for the integration of features and standards from the board platform, such as DIME modules, with many of the high level design tools such as the Xilinx ChipScope ILA (Integrated Logic Analysis) debugging tool and System Generator software. The FUSE framework offers the capability to easily control and configure distributed FPGA systems, whether they are tightly coupled, such as on a PCI board, or loosely coupled over the Internet. This flexibility, along with the abstraction of the communications channel and control, enables systems engineers to kick start product development and to provide added value.

The creation of this systems environment enables the use and control of intelligent hardware such as Plug and Play detection of attached DIME modules. System hardware, based on the DIME standard, gives the ability to rapidly create ideal physical hardware platforms for many requirements. This is accomplished by harnessing the arsenal of DIME modules that provide a variety of real world interfaces, such as high end ADCs (Analog to Digital Converters), DACs (Digital to

Analog Converters), and imaging devices. The variety of DIME modules and DIME carrier boards allows for the immediate construction of highly scalable systems suitable to the application at hand as shown in Figure 2.

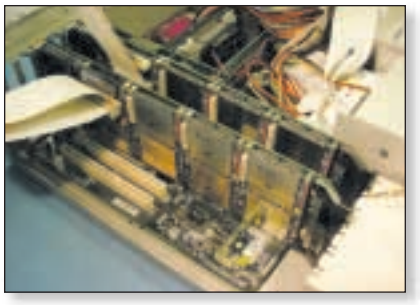

*Figure 2 - High performance FPGA system with 16 Virtex-E devices capable of over 200 billion MACs*

### Fusion Blocks

One of the key elements and openness of the FUSE system framework is the use of Fusion Block™ interfaces. These blocks allow for interfacing support between the board platform and FPGA platform tools. For example, a Fusion Block interface can be provided to allow transparent interfacing between an FPGA-based card and ChipScope ILA software. Similarly, a Fusion Block interface can be used to facilitate interoperability among MATLAB™ modeling tools, System Generator software, and DIME modules. This interfacing capability allows designers to utilize data received from the platform, which can feed back information on the capacities available, or present the real world interface models to the designer.

The integrated FUSE framework allows for straightforward integration of new boards and software tools by providing the hooks through the Fusion Block interfaces. The logical approach means that new tools can be rapidly integrated to provide designers with the latest design tools to increase their productivity.

### Virtex-II PCI Card Supports FUSE System

In accordance with the introduction of Virtex-II as the first platform FPGA, Nallatech has introduced a variant of its existing and successfully proven DIME Carrier Motherboard, the Ballynuey3™. The card is a 64-bit PCI-based card with four DIME module slots that allow for resource expansion through the use of specific DIME modules. The PCI interface is contained in a Xilinx FPGA, thus allowing for full field upgradeability of the interface to the board. The board sports an onboard Virtex-II FPGA with connected resources, such as independent banks of ZBT (Zero Bus Turnaround) SRAM. System services are provided through the PCI interface, allowing operability through the Fusion Block interfaces to other tools such as ChipScope ILA debugging software. A functional diagram of the board is provided in Figure 3.

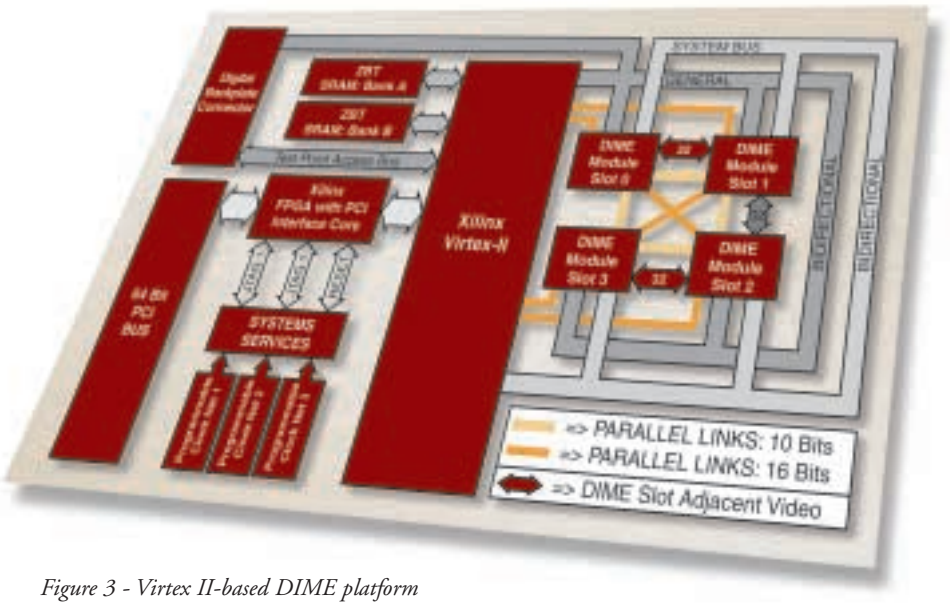


*Figure 3 - Virtex II-based DIME platform*

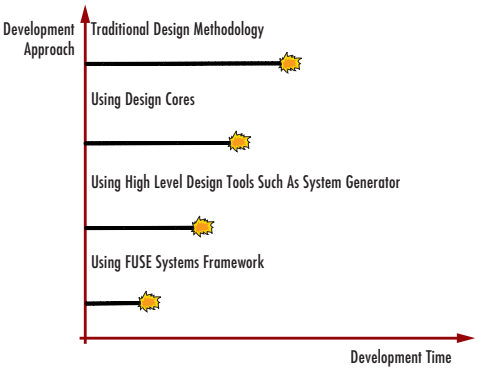


*Figure 4 - Accelerating time to market with FUSE*

### Conclusion

As the complexities of product design increase, the tools and infrastructure to accelerate time to market are critical. The power and flexibility of the Xilinx FPGA platform initiative, complemented by the FUSE system framework from Nallatech, enable the most rapid delivery of final product solutions to customers, as illustrated in Figure 4. The benefits of the FUSE system framework approach have already been proved – demonstrating that time to market savings by a factor of five are realistically achievable.

A typical use of the FUSE framework was explained by Richard Chamberlain, image simulation engineer at Matra BAE Dynamics, "With the FUSE platform and DIME hardware from Nallatech, we were able to reduce our overall design time for our FPGA-based 3D simulator system by around a factor of five. This clearly shows the power of utilizing a proven systems framework to create an end product solution in an optimal design time."

# Virtex-II and Virtex Series FPGAs

The combination of Virtex™-II and Virtex series FPGAs offer you unprecedented capability and flexibility. The Virtex-II devices, the first of the new platform FPGAs, deliver enhanced system memory and lightning-fast DSP through a flexible IP-immersion fabric. Virtex-II devices – with densities ranging from 40,000 up to 10 million system gates – offer new capabilities, including SystemI/O, XCITE, triple DES encryption, and digital clock managers to address system-level design issues.

The Virtex series FPGAs, consisting of Virtex-E, Virtex-EM, and Virtex devices, offer unique features to meet different application requirements.

- The Virtex-E family offers the highest logic gate count available for any FPGA, ranging from 50,000 up to 3.2 million system gates. The Virtex-E family supports 20 I/O standards, including LVPECL, LVDS, and Bus LVDS.
- The Virtex-EM (Extended Memory) family consists of two devices that have high RAM-to-logic ratios that target specific applications, such as gigabit-per-second network switches and high definition graphics.
- The Virtex family consists of devices that range from 50,000 up to one million logic gates. This family supports 17 I/O standards and offers 5 V PCI compliance.

*See www.xilinx.com for more information.*

**FPGA Product Selection Matrix**

| | | DENSITY | | | | | | | FEATURES | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEVICES | KEY FEATURES | Logic Cells | Maximum Logic Gates | Typical System Gate Range | Max. RAM Bits | CLB Matrix | CLBs | Flip-Flops | Max. I/Os | Output Drive (mA) | PCI Compliant | 1.5 Volt | 1.8 Volt | 2.5 Volt | 3.3 Volt | 5.0 Volt |
| XC2V40 | Virtex-II Family: Density/ Performance/ Leadership BRAM Distributed RAM System I/O XCITE Up to 12 DCMs | 576 | 6.9K | 40K | 78K | 8x8 | 64 | 256 | 88 | 2/24 | Y | X | – | I/O | * | – |
| XC2V80 | | 1152 | 13.8K | 80K | 160K | 16x8 | 128 | 512 | 120 | 2/24 | Y | X | – | I/O | * | – |
| XC2V250 | | 3456 | 41.5K | 250K | 480K | 24x16 | 384 | 1536 | 200 | 2/24 | Y | X | – | I/O | * | – |
| XC2V500 | | 6912 | 82.9K | 500K | 672K | 32x24 | 768 | 3072 | 264 | 2/24 | Y | X | – | I/O | * | – |
| XC2V1000 | | 11520 | 138K | 1M | 880K | 40x32 | 1280 | 5120 | 432 | 2/24 | Y | X | – | I/O | * | – |
| XC2V1500 | | 17280 | 207K | 1.5M | 1104K | 48x40 | 1920 | 7680 | 528 | 2/24 | Y | X | – | I/O | * | – |
| XC2V2000 | | 24192 | 290K | 2M | 1344K | 56x48 | 2688 | 10752 | 624 | 2/24 | Y | X | – | I/O | * | – |
| XC2V3000 | | 32256 | 387K | 3M | 2176K | 64x56 | 3584 | 14336 | 720 | 2/24 | Y | X | – | I/O | * | – |
| XC2V4000 | | 51840 | 622K | 4M | 2880K | 80x72 | 5760 | 23040 | 912 | 2/24 | Y | X | – | I/O | * | – |
| XC2V6000 | | 76032 | 912K | 6M | 3648K | 96x88 | 8448 | 33792 | 1104 | 2/24 | Y | X | – | I/O | * | – |
| XC2V8000 | | 104832 | 1.26M | 8M | 4480K | 112x104 | 11648 | 46592 | 1108 | 2/24 | Y | X | – | I/O | * | – |
| XC2V10000 | | 138240 | 1.66M | 10M | 5376K | 128x120 | 15360 | 61440 | 1108 | 2/24 | Y | X | – | I/O | * | – |
| XCV50E | Virtex-E Family: Density BlockRAM Distributed RAM SelectI/O 8 DLLs LVDS, BLVDS, LVPECL | 1728 | 21K | 47K-72K | 88K | 16x24 | 384 | 1536 | 176 | 2/24 | Y | – | X | I/O | I/O | ** |
| XCV100E | | 2700 | 32K | 105K-128K | 118K | 20x30 | 600 | 2400 | 196 | 2/24 | Y | – | X | I/O | I/O | ** |
| XCV200E | | 5292 | 64K | 215K-306K | 186K | 28x42 | 1176 | 4704 | 284 | 2/24 | Y | – | X | I/O | I/O | ** |
| XCV300E | | 6912 | 83K | 254K-412K | 224K | 32x48 | 1536 | 6144 | 316 | 2/24 | Y | – | X | I/O | I/O | ** |
| XCV400E | | 10800 | 130K | 413K-570K | 310K | 40x60 | 2400 | 9600 | 404 | 2/24 | Y | – | X | I/O | I/O | ** |
| XCV600E | | 15552 | 187K | 679K-986K | 504K | 48x72 | 3456 | 13824 | 512 | 2/24 | Y | – | X | I/O | I/O | ** |
| XCV1000E | | 27648 | 332K | 1,146K-1,569K | 768K | 64x96 | 6144 | 24576 | 660 | 2/24 | Y | – | X | I/O | I/O | ** |
| XCV1600E | | 34992 | 420K | 1,628K-2,189K | 1062K | 72x108 | 7776 | 31104 | 724 | 2/24 | Y | – | X | I/O | I/O | ** |
| XCV2000E | | 43200 | 518K | 1,857K-2,542K | 1240K | 80x120 | 9600 | 38400 | 804 | 2/24 | Y | – | X | I/O | I/O | ** |
| XCV2600E | | 57132 | 686K | 2,221K-3,264K | 1530K | 92x138 | 12696 | 50784 | 804 | 2/24 | Y | – | X | I/O | I/O | ** |
| XCV3200E | | 73008 | 876K | 2,608K-4,074K | 1846K | 104x156 | 16224 | 64896 | 804 | 2/24 | Y | – | X | I/O | I/O | ** |
| XCV405E | Virtex Extended Memory Capabilities | 10800 | 130K | 1,068K-1,307K | 710K | 40x60 | 2400 | 9600 | 404 | 2/24 | Y | – | X | I/O | I/O | ** |
| XCV812E | | 21168 | 254K | 2,569K-3,062K | 1414K | 56x84 | 4704 | 18816 | 556 | 2/24 | Y | – | X | I/O | I/O | ** |
| XCV50 | Virtex Family: Density BlockRAM Distributed RAM SelectI/O 4 DLLs | 1728 | 21K | 34K-58K | 56K | 16x24 | 384 | 1536 | 180 | 2/24 | Y | – | – | – | X | * |
| XCV100 | | 2700 | 32K | 72K-109K | 78K | 20x30 | 600 | 2400 | 180 | 2/24 | Y | – | – | – | X | * |
| XCV150 | | 3888 | 47K | 93K-165K | 102K | 24x36 | 864 | 3456 | 260 | 2/24 | Y | – | – | X | I/O | * |
| XCV200 | | 5292 | 64K | 146K-237K | 130K | 28x42 | 1176 | 4704 | 284 | 2/24 | Y | – | – | X | I/O | * |
| XCV300 | | 6912 | 83K | 176K-323K | 160K | 32x48 | 1536 | 6144 | 316 | 2/24 | Y | – | – | X | I/O | * |
| XCV400 | | 10800 | 130K | 282K-468K | 230K | 40x60 | 2400 | 9600 | 404 | 2/24 | Y | – | – | X | I/O | * |
| XCV600 | | 15552 | 187K | 365K-661K | 312K | 48x72 | 3456 | 13824 | 512 | 2/24 | Y | – | – | X | I/O | * |
| XCV800 | | 21168 | 254K | 511K-888K | 406K | 56x84 | 4704 | 18816 | 512 | 2/24 | Y | – | – | – | X | * |
| XCV1000 | | 27648 | 332K | 622K-1,124K | 512K | 64x96 | 6144 | 24576 | 512 | 2/24 | Y | – | – | – | X | * |

* I/Os are voltage tolerant
** 5 V tolerant I/Os with external resistor
X = Core and I/O voltage
I/Os = I/O voltage supported


Say hello to a new level of performance: the Spartan™-II family now includes devices with more than 200,000 system gates. You get 100,000 system gates for under $10, at speeds of 200 MHz and beyond, giving you design flexibility that's hard to beat. These low-powered, 2.5V devices feature I/Os that operate at up to 3.3V with full 5V tolerance. Spartan-II devices also feature multiple delay locked loops, on-chip RAM (block and distributed), and versatile I/O technology that supports over 16 high-performance interface standards. You get all this in an FPGA that offers unlimited reprogrammability, and can even be upgraded in the field, remotely, over any network.

### Robust Feature Set

- Flexible on-chip distributed and block memory
- Four digital delay-locked loops for efficient chip-level/board-level clock management
- Select I/O™ Technology for interfacing with all major bus standards such as HSTL, GTL, SSTL, and so on
- Full PCI compliance
- System speeds over 200 MHz
- Power management

### Extensive Design Support

- Complete suite of design tools
- Extensive core support
- Compile designs in minutes

### Advantages over ASICs

- No costly NRE charges
- No time consuming vector generation needed
- All devices are 100% tested by Xilinx
- Field upgradeable (remotely upgradeable, using Xilinx Online technology)
- No lengthy prototype or production lead times
- Priced aggressively against comparable ASICs

*See www.xilinx.com for more information.*

**FPGA Product Selection Matrix**

| | | DENSITY | | | | | | | FEATURES | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEVICES | KEY FEATURES | Logic Cells | Maximum Logic Gates | Typical System Gate Range | Max. RAM Bits | CLB Matrix | CLBs | Flip-Flops | Max. I/O | Output Drive (mA) | PCI Compliant | 1.8 Volt | 2.5 Volt | 3.3 Volt | 5.0 Volt |
| XCS05 | Spartan Family: High Volume ASIC Replacement/ High Performance/ SelectRAM Memory | 238 | 3K | 2K-5K | 3K | 10x10 | 100 | 360 | 77 | 12 | Y | – | – | – | X |
| XCS10 | | 466 | 5K | 3K-10K | 6K | 14x14 | 196 | 616 | 112 | 12 | Y | – | – | – | X |
| XCS20 | | 950 | 10K | 7K-20K | 13K | 20x20 | 400 | 1120 | 160 | 12 | Y | – | – | – | X |
| XCS30 | | 1368 | 13K | 10K-30K | 18K | 24x24 | 576 | 1536 | 192 | 12 | Y | – | – | – | X |
| XCS40 | | 1862 | 20K | 13K-40K | 25K | 28x28 | 784 | 2016 | 205 | 12 | Y | – | – | – | X |
| XCS05XL | Spartan-XL Family: High Volume ASIC Replacement/ High Performance/ SelectRAM Memory | 238 | 3K | 2K-5K | 3K | 10x10 | 100 | 360 | 77 | 12/24 | Y | – | – | X | * |
| XCS10XL | | 466 | 5K | 3K-10K | 6K | 14x14 | 196 | 616 | 112 | 12/24 | Y | – | – | X | * |
| XCS20XL | | 950 | 10K | 7K-20K | 13K | 20x20 | 400 | 1120 | 160 | 12/24 | Y | – | – | X | * |
| XCS30XL | | 1368 | 13K | 10K-30K | 18K | 24x24 | 576 | 1536 | 192 | 12/24 | Y | – | – | X | * |
| XCS40XL | | 1862 | 20K | 13K-40K | 25K | 28x28 | 784 | 2016 | 224 | 12/24 | Y | – | – | X | * |
| XC2S15 | Spartan-II Family: High Volume BlockRAM Distributed RAM SelectI/O 4 DLLs | 432 | 5K | 5K-15K | 22K | 8x12 | 96 | 384 | 86 | 2/24 | Y | – | X | I/O | * |
| XC2S30 | | 972 | 12K | 12K-30K | 36K | 12x18 | 216 | 864 | 132 | 2/24 | Y | – | X | I/O | * |
| XC2S50 | | 1728 | 21K | 21K-50K | 56K | 16x24 | 384 | 1536 | 176 | 2/24 | Y | – | X | I/O | * |
| XC2S100 | | 2700 | 32K | 32K-100K | 78K | 20x30 | 600 | 2400 | 196 | 2/24 | Y | – | X | I/O | * |
| XC2S150 | | 3888 | 47K | 47K-150K | 102K | 24x36 | 864 | 3456 | 260 | 2/24 | Y | – | X | I/O | * |
| XC2S200 | | 5292 | 64K | 64K-200K | 130K | 28x42 | 1,176 | 4704 | 284 | 2/24 | Y | – | X | I/O | * |

* I/Os are tolerant
X = Core and I/O voltage
I/Os = I/O voltage supported





# XC9500 and CoolRunner CPLDs

Whether performing high-speed networking or power-conscious portable designs, Xilinx CPLDs provide you with a complete range of value oriented products.

**XC9500™** – Offers industry-leading speeds, while giving you the flexibility of an enhanced customer-proven pin-locking architecture along with extensive IEEE Std. 1149.1 JTAG boundary-scan support.

**CoolRunner™** – Offers the patented Fast Zero Power (FZP) design technology, combining low power and high speed. These devices offer standby currents of less than 100 microamps, operating currents 50-67% lower than traditional CPLDs, and pin-to-pin speeds of 5.0 ns.

- **WebPOWERED™ Software Solutions** – Offers you the flexibility to target Xilinx CPLD and FPGA products online or on the desktop, including:
- **WebFITTER™** – An online device-fitting and evaluation tool that accepts HDL, ABEL, or netlist files, and provides all reports, simulation models, and programming files, along with price quotes. Available to support all Xilinx CPLD products.
- **WebPACK™ ISE** – Downloadable desktop solutions that offer free CPLD and FPGA software modules for ABEL/HDL synthesis and simulation, device-fitting, and JTAG programming.

Through leading performance, free Internet-based WebPOWERED software, and the industry's lowest power consumption, Xilinx has the right CPLD and FPGA for every designer's need.

***See www.xilinx.com for more information.***

| CPLD Product Selection Matrix | | | | Density | | Features | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Core Voltage | CPLD Family | Device | Key Features | Macrocells | Max. I/O | Pin-to-Pin Delay (ns) | System Frequency | Individual OE Ctrl | JTAG | Ultra Low Power |
| 2.5 VOLT ISP | XC9500XV | XC9536XV | Best Pin-Locking JTAG w/Clamp High Performance High Endurance | 36 | 36 | 3.5 | 278 | √ | √ | – |
| | | XC9572XV | | 72 | 72 | 4 | 250 | √ | √ | – |
| | | XC95144XV | | 144 | 117 | 4 | 250 | √ | √ | – |
| | | XC95288XV | | 288 | 192 | 5 | 222 | √ | √ | – |
| 3.3 Volt ISP | XC9500XL | XC9536XL | Best Pin-Locking JTAG w/Clamp High Performance High Endurance | 36 | 36 | 5 | 222 | √ | √ | – |
| | | XC9572XL | | 72 | 72 | 5 | 222 | √ | √ | – |
| | | XC95144XL | | 144 | 117 | 5 | 222 | √ | √ | – |
| | | XC95288XL | | 288 | 192 | 6 | 208 | √ | √ | – |
| | CoolRunner XPLA3 | XCR3032XL | Ultra Low Power JTAG Increased Logic Flexibility | 32 | 36 | 5 | 175 | – | √ | √ |
| | | XCR3064XL | | 64 | 68 | 6 | 145 | – | √ | √ |
| | | XCR3128XL | | 128 | 108 | 6 | 145 | – | √ | √ |
| | | XCR3256XL | | 256 | 164 | 7.5 | 140 | – | √ | √ |
| | | XCR3384XL | | 384 | 220 | 7.5 | 127 | – | √ | √ |
| | | XCR3512XL | | 512 | TBD | TBD | TBD | – | √ | √ |
| 5 Volt ISP | XC9500 | XC9536 | Best Pin-Locking JTAG High Endurance | 36 | 34 | 5 | 100 | √ | √ | – |
| | | XC9572 | | 72 | 72 | 7.5 | 83.3 | √ | √ | – |
| | | XC95108 | | 108 | 108 | 7.5 | 83.3 | √ | √ | – |
| | | XC95144 | | 144 | 133 | 7.5 | 83.3 | √ | √ | – |
| | | XC95216 | | 216 | 166 | 10 | 66.7 | √ | √ | – |
| | | XC95288 | | 288 | 192 | 10 | 66.7 | √ | √ | – |

XC18V
XC17V
XC17S

# FPGA Configurations PROM

Xilinx offers a full range of configuration memory devices optimized for use with Xilinx FPGAs. Our PROM product lines are designed to meet the same stringent demands as our high-performance FPGAs, taking full advantage of the same advanced processing technologies. In addition, they were developed in close cooperation with Xilinx FPGA designers for optimal performance and reliability.

**XC18V00** – Our in-system reprogrammable family provides a feature-rich, fast configuration solution available today, and provides a cost-effective method for reprogramming and storing large Xilinx FPGA bitstreams. This family is JTAG ready and boundry-scan enabled for exceptional ease-of-use, system integration, and flexibility.

**XC17V00/XC17S00** – Our low cost XC17V and XC17S families are an ideal configuration solution for cost-sensitive applications. XC17V PROMs are pin-compatible with our XC18V family to allow for a cost-reduction migration path as your production volumes increase. The XC17S family is specially designed to provide a low cost, integrated solution for our Spartan families of FPGAs.

**Configuration PROMs for Virtex-E/Virtex-EM**

| Device | Configuration Bits | XC17xx Solution | XC18Vxx Solution | 8-pin TSOP | 20-pin PLCC | 20-pin SOIC | 44-pin PLCC | 44-pin VQFP |
|---|---|---|---|---|---|---|---|---|
| XCV50E | 630,048 | 17V01 | 18V01 | X* | X | X | – | X** |
| XCV100E | 863,840 | 17V01 | 18V01 | X* | X | X | – | X** |
| XCV200E | 1,442,106 | 17V02 | 18V02 | X* | X* | X* | X** | X** |
| XCV300E | 1,875,648 | 17V02 | 18V02 | – | X* | – | X | X |
| XCV400E | 2,693,440 | 17V04 | 18V04 | – | X* | – | X | X |
| XCV405E | 3,430,400 | 17V04 | 18V04 | – | X* | – | X | X |
| XCV600E | 3,961,632 | 17V04 | 18V04 | – | X* | – | X | X |
| XCV812E | 6,519,648 | 17V08 | 2 of 18V04 | – | – | – | X | X |
| XCV1000E | 6,587,520 | 17V08 | 2 of 18V04 | – | – | – | X | X |
| XCV1600E | 8,308,992 | 17V08 | 2 of 18V04 | – | – | – | X | X |
| XCV2000E | 10,159,648 | 17V16 | 2 of 18V04 | – | – | – | X | X |
| XCV2600E | 12,922,336 | 17V16 | 3 of 18V04 + 18V512 | – | X*** | – | X** | X |
| XCV3200E | 16,283,712 | 17V16 | 4 of 18V04 | – | – | – | X | X |

* Available in XC17Vxx only.
** Available in XC18Vxx only.
*** Available in XC18V512 only.

**Configuration PROMs for Virtex**

| Device | Configuration Bits | XC17xx Solution | XC18Vxx Solution | 8-pin TSOP | 20-pin PLCC | 20-pin SOIC | 44-pin PLCC | 44-pin VQFP |
|---|---|---|---|---|---|---|---|---|
| XCV50 | 559,200 | 17V01 | 18V01 | X* | X | X | – | X** |
| XCV100 | 781,216 | 17V01 | 18V01 | X* | X | X | – | X** |
| XCV150 | 1,041,096 | 17V01 | 18V01 | X* | X | X | – | X** |
| XCV200 | 1,335,840 | 17V01 | 18V02 | X* | X* | X* | X** | X** |
| XCV300 | 1,751,808 | 17V02 | 18V02 | – | X* | – | X | X |
| XCV400 | 2,546,048 | 17V04 | 18V04 | – | X* | – | X | X |
| XCV600 | 3,607,968 | 17V04 | 18V04 | – | X* | – | X | X |
| XCV800 | 4,715,616 | 17V08 | 18V04 + 18V512 | – | X*** | – | X** | X |
| XCV1000 | 6,127,744 | 17V08 | 18V04 + 18V02 | – | – | – | X | X |

* Available in XC17Vxx only.
** Available in XC18Vxx only.
*** Available in XC18V512 only.

**Configuration PROMs for Spartan-XL/Spartan-II**

| Device | PROM Solution | 8-pin PDIP | 8-pin VOIC | 20-pin SOIC | 44-pin VQFP |
|---|---|---|---|---|---|
| XCS05XL | XC17S05XL | X | X | – | – |
| XCS10XL | XC17S10XL | X | X | – | – |
| XCS20XL | XC17S20XL | X | X | – | – |
| XCS30XL | XC17S30XL | X | X | – | – |
| XCS40XL | XC17S40XL | X | X | X | – |
| XC2S15 | XC17S15A | X | X | X | – |
| XC2S30 | XC17S30A | X | X | X | – |
| XC2S50 | XC17S50A | X | X | X | – |
| XC2S100 | XC17S100A | X | X | X | – |
| XC2S150 | XC17S150A | X | X | X | – |
| XC2S200 | XC17S200A | X | X | – | X |

# QML-Certified FPGAs and PROMs

The Xilinx QPro™ family of radiation hardened FPGAs and PROMs are finding homes in many new satellite and space applications. Both the XQR4000XL and XQVR Virtex™ products are being designed into space systems that will utilize reconfigurable technology. Numerous communications and GPS satellites, space probes, and shuttle missions are included on the growing list of programs that will be flying these devices.

The Virtex QPro family of high reliability products is experiencing a high degree of success in the defense market. As designers find it more and more difficult to find components suitable for the harsh environments seen by defense systems, they are discovering that they can incorporate the functions of obsolete parts into Virtex QPro products. This has the added long term advantage of significantly reducing the costs of future requalifications, because their systems can retain consistent form, fit, and function through the use of Virtex QPro FPGAs. This cannot be achieved with costly and inflexible ASICs or custom logic.

Please visit www.xilinx.com/products/hirel_qml.htm for all the latest information about these products, including some new applications notes.

## FPGA Product Selection Matrix

| | | DENSITY | | | | | | | FEATURES | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Device | Key Features | Logic Cells | Maximum Logic Gates | Typical System Gate Range | Max. RAM Bits | CLB Matrix | CLBs | Flip-Flops | Max. I/O | Output Drive (mA) | PCI Compliant | 1.8 Volt | 2.5 Volt | 3 Volt | 5 Volt |
| **XQR/XQ4013XL | XC4000 Series: Density Leadership/ High Performance/ SelectRAM Memory | 1,368 | 13K | 10K-30K | 18K | 24x24 | 576 | 1,536 | 192 | 12/24 | Y | – | – | X | * |
| **XQR/XQ4036XL | | 3,078 | 36K | 22K-65K | 42K | 36x36 | 1,296 | 3,168 | 288 | 12/24 | Y | – | – | X | * |
| **XQR/XQ4062XL | | 5,472 | 62K | 40K-130K | 74K | 48x48 | 2,304 | 5,376 | 384 | 12/24 | Y | – | – | X | * |
| XQ4085XL | | 7,448 | 85K | 55K-180K | 100K | 56x56 | 3,136 | 7,168 | 448 | 12/24 | Y | – | – | X | * |
| XQV100 | Virtex Family: Density/ Performance Leadership BlockRAM Distributed RAM SelectI/O 4 DLLs | 2,700 | 32K | 72K-109K | 78K | 20x30 | 600 | 2,400 | 180 | 2/24 | Y | – | X | I/O | * |
| **XQVR/XQV300 | | 6,912 | 83K | 176K-323K | 160K | 32x48 | 1,536 | 6,144 | 316 | 2/24 | Y | – | X | I/O | * |
| **XQVR/XQV600 | | 15,552 | 187K | 365K-661K | 312K | 48x72 | 3,456 | 13,824 | 512 | 2/24 | Y | – | X | I/O | * |
| **XQVR/XQV1000 | | 27,648 | 332K | 622K-1,124K | 512K | 64x96 | 6,144 | 24,576 | 512 | 2/24 | Y | – | X | I/O | * |

* I/Os are tolerant
** XQR and XQVR devices are radiation hardened
X = Core and I/O voltage
I/Os = I/O voltage supported

(1) Selected XQ4000E/EX devices also available

## QPro QML-Certified PROMs

| | | Package | | | |
|---|---|---|---|---|---|
| Device | Density | DD8 | SO20 | CC44 | VQ44 |
| XC1736D | 36Kb | X | | | |
| XC1765D | 64Kb | X | | | |
| XC17128D | 128Kb | X | | | |
| XC17256D | 256Kb | X | | | |
| XQR/XQ1701L* | 1Mb | | X | X | |
| XQR/XQ18V04* | 4Mb | | | X | X** |

* XQR devices are radiation hardened.
** XQ devices only.

# Xilinx Intellectual Property Solutions

## The Most Comprehensive and Highest Quality Solution in the PLD Industry

The Xilinx Intellectual Property Solutions Division offers the best selection of Intellectual Property solutions for a wide variety of industries and applications. Xilinx Smart-IP™ Technology delivers high performance, flexibility, and predictability, with optimized cores that give you both reduced cost and faster time to market.

**LogiCORE™ Products** – More than 40 LogiCORE products, such as parameterizable DSP building blocks and memory cores, are included with the Xilinx CORE Generator™ software which is a component of your Xilinx Foundation Series™ or Alliance Series™ software. LogiCORE products, such as PCI, PCI-X, Reed-Solomon, and other advanced function cores, are separately licensed and available on the IP Center website.

**AllianceCORE™ Products** – A cooperative program with third-party IP suppliers who sell and support their cores directly with Xilinx customers. AllianceCORE products must meet criteria that ensure they deliver value and performance in a Xilinx device.

**Reference Design Alliance Program** – Xilinx proactively supports development of third-party, system-level reference designs to provide fully functional, modular designs that offer considerable development time savings.

**XPERTS™ Partner Program** – The worldwide XPERTS Program provides more than 70 consultants certified in delivering turnkey system designs for the Xilinx architecture, including PCI designs, new design methodologies, and system-level design, along with IP customization and integration.

**IP Delivery Tools** – The Xilinx CORE Generator™ tool enables cataloging and generation of parameterized cores that are high performance, predictable, and integrated with our system-level design reuse tools. The cores are provided in VHDL and Verilog™ behavioral description languages.

**The IP Center Internet Portal** – This website provides access to the latest LogiCORE and AllianceCORE products and reference designs via the Smart Search™ engine. You can easily find the IP that you need at www.xilinx.com/ipcenter. Advanced function cores are available for IP evaluation and can be purchased from the IP Center.

**Design Reuse** – Download the "FPGA Reuse Field Guide" from Xilinx the IP Center website. Then use the Xilinx IP Capture Tool to package your IP with simulation models, testbenches, and PDF or HTML files. Then, you can catalog and share your IP using the CORE Generator.

**The REALPCI/PCI-X 64/66 Cores** – Xilinx complete solutions offer the performance, compliance, and flexibility needed by systems that have high bandwidth requirements. Parameterizable PCI/PCI-X cores, reference designs, prototyping boards, education, and Xilinx PCI/PCI-X XPERTS, combined with a proven design and guaranteed timing, make Xilinx PCI/PCI-X the lowest risk solution in the market.

**The Xilinx XtremeDSP™ Solution** – Our exclusive FPGA partnership with The MathWorks enables you to create complex, high performance DSP designs in a familiar environment with huge time to market advantages. Xilinx and its partners offer a complete set of cores for high-performance, low-cost DSP implementations that provide:

- **Xtreme Flexibility** – Distributed DSP resources (such as look up tables, registers, multipliers, memory) and segmented routing allow optimized implementation of algorithms. Plus, you get all the traditional FPGA benefits:
  - RAM-based FPGA technology, for fast and easy design changes
  - Fast time to market, to give you a competitive advantage
  - Field upgradeable systems (using IRL™), for extended product lifecycle.
- **Xtreme Productivity** – The industry's first System Generator for Simulink® bridges the gap between FPGA and conventional DSP design flows, and features:
  - Unique constraint-driven Filter Generator, for performance/cost optimization
  - Power estimator tool (Xpower), for very low-power DSP implementations
  - Eleven optimized DSP algorithms (cores) that cut development time by weeks
  - New DSP features added to the ChipScope ILA tool, rapidly reduces hardware debugging time.
- **Xtreme Performance** – Table 1 illustrates the amazing performance you can achieve with Xilinx XtremeDSP.

**Table 1 - Extreme Performance**

| Function | Industry's Fastest DSP Processor Core | Xilinx VIRTEX |
|---|---|---|
| **MACs per second**<br>- Multiply and accumulate<br>- 8 x 8-bit | 8.8 Billion | **600 Billion** |
| **FIR Filter**<br>- 256-tap, linear phase<br>- 16-bit data/coefficients | 17 MSPS<br>@ 1.1 GHz | **180 MSPS**<br>@ 180 MHz |
| **FFT**<br>- 1024 point, complex data<br>- 16-bit real and imaginary comp. | 7.7 µs<br>@ 800 MHz | **<1 µs**<br>@ 140 MHz |


"I have taken a number of courses offered by Xilinx Education Services and have benefited from their instructors' high levels of expertise, professional presentation and materials. The San José facilities are superb. I highly recommend Xilinx Education Services to anyone who chooses to design with Xilinx FPGAs."

- Jeffrey E. Journey,
Image Capture Development, IBM

Extend your technical capabilities and accelerate your time to market with Xilinx Global Services. Our portfolio of education, support, and design services, along with our award-winning website (support.xilinx.com), will give you the expert help you need to stay ahead of your competition and be the first to market with the most efficient and cost effective designs. We can reduce your learning curve, speed up your design time, jump-start your product development cycle, and get your products to market faster than ever before.

### Education Services
**Move to the head of the class**

Xilinx Education Services keep your technical skills sharp. A broad range of classes are available for designers of all levels, from the novice to the most experienced. Hands-on training classes, led by instructors who are experienced designers themselves, are conducted at the Xilinx headquarters in San Jose and at other sites worldwide throughout the year. The classes cover a wide range of topics, including:

- Using cores
- Using high level design languages
- System and configuration design issues
- Migration from ASIC to FPGA.

### support.xilinx.com
**Knowledge at your fingertips**

Support.xilinx.com is our online solution for resolving your design issues. Here, you'll find:

- Our Answers Database which contains more than 4,000 proven design solutions.
- Problem Solvers to help you troubleshoot device configuration, software installation, and JTAG issues.
- Discussion forums that let you share ideas and questions with other designers.
- A Web support interface that allows you to easily submit a problem, and can get your answer quickly.

Support.xilinx.com is always available to you, 24 hours a day.

### Support Services
**Experts on Call**

Our Gold and Platinum Technical Services improve your productivity and accelerate your design process by reducing your design and troubleshooting time. As a Platinum customer, you receive access to a dedicated toll-free number (in North America only) so you can get quick assistance with any design problem; you have first priority to our dedicated team of skilled senior application engineers - the best in the business. You also get ten education credits for Xilinx training courses to improve your skills. As a Gold customer, you receive our standard level of service, at no charge. With either Platinum or Gold service, our team of professionals is ready to help you use the tools and techniques that have made Xilinx the market leader in FPGA technology.

### Design Services
**Your Virtual Project Team**

With Xilinx Design Services you can take full advantage of our design expertise, so you're free to focus on what you do best. A Xilinx Design Services team - made up of best-in-class designers, silicon experts, and software specialists - becomes your virtual in-house project team, so you can immediately extend your technical staff's bandwidth and eliminate ramp-up time. The Xilinx Design Services team gives you our unique expertise with Xilinx tools and techniques, and the fruits of our extensive R&D investment.

***See www.support.xilinx.com for more information on all of our services.***

| Features | Platinum | Gold** |
|---|---|---|
| Senior Application Engineers | ✔ | |
| Dedicated Toll-Free Number | ✔ | |
| Proactive Status Updates | ✔ | |
| Priority Case Resolution | ✔ | |
| Ten Education Credits | ✔ | |
| Service Packs and Software Updates | ✔ | ✔ |
| Application Engineer/Customer Ratio* | 2X Gold Level | Standard |

**Applicable in North America Only*

*** Gold is the standard level of service we provide.*

# Software Solutions Version 3 Development Systems Quick Reference Guide

Xilinx development systems give you the speed you need. With the initial release of our version 3 solutions, Xilinx place-and-route times are as fast as two minutes for our 200,000-gate XC2S200 Spartan™-II device, and 30 minutes for our one-million-gate, system-level XCV1000E Virtex™-E device. That makes Xilinx development systems the fastest in the industry for the design of programmable logic devices (PLDs).

And with the push of a button, our timing-driven tools are creating designs that support I/O speeds in excess of 800 Mbps and internal clock frequencies in excess of 300 MHz.

The newest devices in the Virtex series, the Virtex-II family, are fully supported by the Xilinx development systems. Advanced design flows, including modular and incremental design, are now available for use in the designing of Virtex-II FPGAs

Xilinx desktop design solutions combine powerful technology with an easy to use interface to help you achieve the best possible designs within your project schedule, regardless of your experience level. For more information on any Xilinx product, visit www.xilinx.com.


**Alliance Series™ Solutions:**
The Alliance Series solutions contain powerful open systems implementation tools that are engineered to plug and play within your existing design flow. This combination of advanced features delivers high performance results on the toughest designs.


**Xilinx Foundation Series™ ISE Solutions:**
The Xilinx Foundation Integrated Synthesis Environment (ISE) is our next-generation, complete, ready-to-use design environment, optimized to deliver the benefits of an HDL methodology. Foundation ISE is packed with advanced technologies, in addition to Xilinx Alliance design entry tools, helping you bring your product to market faster.

Xilinx Web-based design solutions give you the ability to engage in digital design activities online using Xilinx application servers, or download design and implementation software modules for use in your own design environment. These applications include:

**WebFITTER™:**
The WebFITTER is a free Web-based design tool that allows you to evaluate your designs using Xilinx XC9500™ series CPLDs and CoolRunner™ series CPLDs.

**WebPACK™ ISE:**
The WebPACK ISE is a collection of free downloadable software modules, including ABEL v7.3, VHDL, and Verilog synthesis, design implementation tools, and device programming software.

WebPACK ISE now includes support for all Xilinx CPLD families (XC9500 series and CoolRunner series) and the entire Spartan-II FPGA family, as well as the 300,000-system-gate Virtex XCV300E FPGA.

**WebFITTER URL:**
www.xilinx.com/sxpresso/webfitter.htm

**WebPACK ISE URL:**
www.xilinx.com/sxpresso/webpack.htm

# Version 3 Development Systems

## Feature Comparison Guide

| Design Entry | Alliance | Foundation | Foundation ISE | WebPACK |
|---|---|---|---|---|
| Schematic | | ● | ● | ● |
| VHDL, Veriolog HDL, ABEL, HDL | | ● | ● | ● |
| State Diagram Editor | | ● | ●(1) | ●(1) |
| Floorplanner | ● | ● | ● | ● |
| CORE Generator | ● | ● | ● | ● |
| Timing Constraint | ● | ● | ● | ● |
| Modular Design | (Optional) | | (Optional) | |
| **Design Synthesis** | **Alliance** | **Foundation** | **Foundation ISE** | **WebPACK** |
| Xilinx Synthesis Technology (XST) | | | ● | ● |
| FPGA Express / Incremental Synthesis | | ●(5) | ● | |
| **Design Verification** | **Alliance** | **Foundation** | **Foundation ISE** | **WebPACK** |
| Timing Simulation | ● | ● | ● | ● |
| Gate Level Simulator | | ● | ●(2) | ● |
| HDL Simulator | ●(1) | ●(1) | ●(1) | ●(1) |
| HDL Testbench Generator | | | ●(1) | ●(1) |
| Integrated Logic Analysis (ChipScope ILA) | (Optional) | (Optional) | (Optional) | |
| Static Timing Analysis | ● | ● | ● | ● |
| **Design Implementation** | **Alliance** | **Foundation** | **Foundation ISE** | **WebPACK** |
| Constraints Editor | ● | ● | ● | ● |
| CPLD ChipViewer | ● | ● | ● | ● |
| FPGA Editor | ● | ● | ● | ● |
| Error Navigation to Xilinx Web | | | ● | ● |
| Command Line Operation | ● | | ● | ● |
| HTML Timing Reports | ● | ● | ● | ● |
| Data Book I/O Timing | ● | ● | ● | ● |
| Timing-Driven Place-and-Route | ● | ● | ● | ● |
| Multipass Place-and-Route | ● | ● | ● | |
| Project Archiving | ● | ● | ● | ● |
| **System Interfaces** | **Alliance** | **Foundation** | **Foundation ISE** | **WebPACK** |
| EDIF In | ● | ● | | CPLD Only |
| PROM File Generator | ● | ● | ● | ● |
| JTAG Download Software | ● | ● | ● | ● |
| IBIS | ● | ● | ● | ● |
| STAMP | ● | ● | ● | ● |
| VHDL, Verilog Out | ● | ● | ● | ● |
| HDL Simulation Libraries | ● | ● | ● | ● |
| **Environment** | **Alliance** | **Foundation** | **Foundation ISE** | **WebPACK** |
| Operating System | PC / UNIX | PC | PC | PC |

## Device Comparison Guide

| Elite | Standard/Express | Base/Base Express | WebPACK ISE |
|---|---|---|---|
| All Virtex-II Family | Virtex-II Family up to XC2V1000 | Virtex-II Family up to XC2V80 | Virtex XCV300E only |
| All Virtex-E Family | Virtex-E Family up to XCV1000E | Virtex-E XCV50E only | All Spartan-II Family |
| All Virtex Family | All Virtex Family | Virtex XCV50 only | All CoolRunner Series(4) |
| All Spartan Series | All Spartan Series | All Spartan Series | All XC9500 Series |
| All XC9500 Series | All XC9500 Series | All XC9500 Series | |
| All XC4000E/L/EX | All XC4000E/L | All XC4000E/L | |
| All XC4000XL/XLA | All XC4000XL/XLA/EX/XV(3) | XC4000XL/XLA up to XC4020 | |
| All XC3000(3) | All XC3000(3) | All XC30003 | |
| All XC5200(3) | All XC5200(3) | All XC52003 | |

1. Evaluation functionality available through the Xilinx ALLSTAR program. For more information on the ALLSTAR program, go to www.xilinx.com.
2. Functional and timing simulation is performed using a HDL simulator in the ISE product.
3. XC3000, XC5200, and XC4000XV devices are not supported in the Foundation Series ISE configurations.
4. CoolRunner series is only available in WebFITTER and WebPACK tools at this time.
5. Foundation Base does not include a license for FPGA Express.

# ATTENTION, PORTABLE SYSTEM DESIGNERS!

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- Winner will receive $10,000 CASH
- Winner's design will be published in Portable Design magazine

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- Register online: www.xilinx.com/contest.
- Submit your paper design by April 30, 2001.
- Top 10 Finalists will be announced on May 14, 2001.
- Top 10 Finalists will submit their working designs by June 30, 2001.
- Designs will be judged by HandSpring Chief Product Officer Jeff Hawkins, Xilinx CTO Bill Carter, and Portable Design Editor-In-Chief Richard Nass.

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