COMPUTER DESIGN

THE DESIGN AND APPLICATION OF DIGITAL CIRCUITS, EQUIPMENT & SYSTEMS

APRIL 1964

HIGHLIGHTS OF SPRING JOINT COMPUTER CONFERENCE

MEMORY TEST EQUIPMENT

DESIGN OF MODULAR 250 MC CIRCUITS

TCM-32

Front Access 5 Microsecond General Purpose Core Memory

SPECIFICATIONS

Capacity: 128 to 4096 words
8 to 48 bits per word

Speed: Full cycle - 5 usecs
Half cycle - 3 usecs

STANDARD OPTIONS

ADDRESSING

Random
Sequential
Random Sequential
Sequential Interlace
Serial

EXTERNAL CONTROL

Memory Clear
Address Register Clear
Information Register Clear
Address Register Set
Information Register Set
Address Register Count
Information Register Count

FAILURE SENSING

Voltage Failure Sensing

INFORMATION IN-OUT

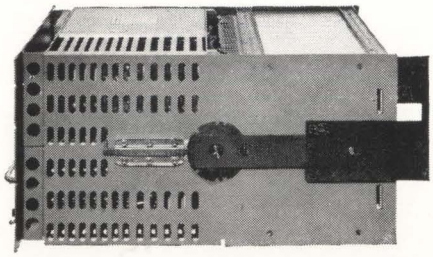
Partial Substitution
Serial

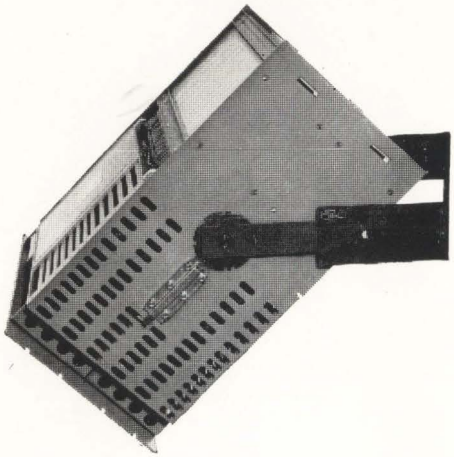
STATE (INDICATION)

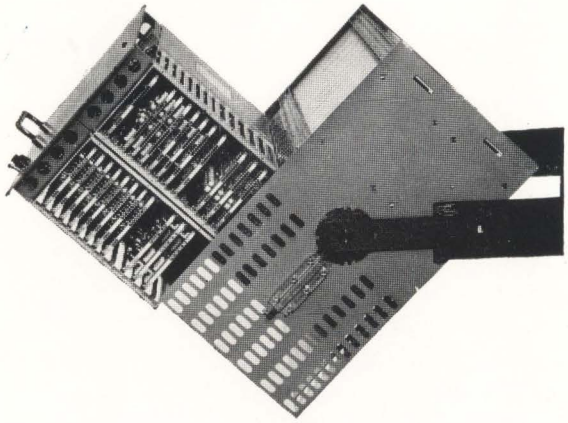
Load or Unload
End of Cycle
Random or Sequential
Information Available
Busy

MODES OF OPERATION

CLEAR/WRITE READ/RESTORE
LOAD UNLOAD
READ/MODIFY/WRITE







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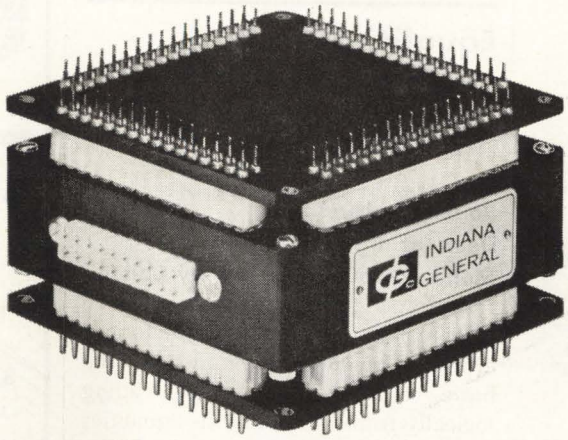

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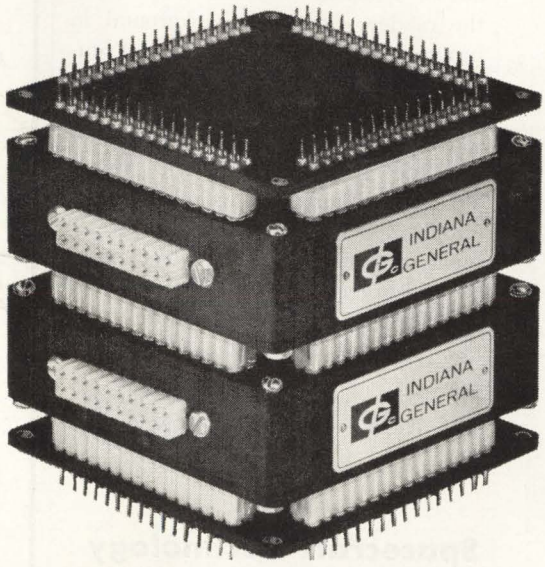

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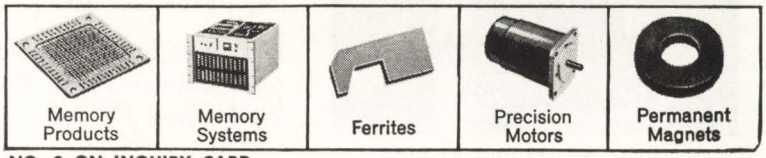

CIRCLE NO. 2 ON INQUIRY CARD

NEW BOOKS

Equalities and Approximations with Fortran

Robert D. Larsson,
Dean of Instruction,
Mohawk Valley Community College

The book develops some of the foundations of modern algebra and the basic concepts of analysis, leading logically from the notion of equalities to that of inequalities, and emphasizing resulting modifications that figure importantly in the theory and methods of solution. The author provides the reader with solid background in program theory, pointing out the limitations as well as the capabilities of a high-speed computer. This book is said to be the first to combine equalities and approximations with FORTRAN programming, to relate FORTRAN specifically to a math treatment of varied areas of subject matter and to explore such illustrated material with scope and penetrating detail. Price: $5.50.

Publisher: John Wiley & Sons, Inc.
605 Third Ave., N.Y. 16, N.Y.

Spacecraft Technology

Dr. Edward A. Wolff, Director,
Space Technology Institute

This 278-page textbook was derived from material prepared for a one-semester course in spacecraft technology given duing 1962 to senior engineering students in the Aerospace Engineering Dept. of Texas A&M College. The material gives an over-all view of space technology and the problems encountered in each area. The subject matter is divided into 19 parts which include a historical review, the significance of space study, space science, space launch and reentry environment, power supplies, instruments, trajectories and orbits, guidance and contol, tracking, data acquisition, and data processing.

Publisher: Spartan Books,
6411 Chillum Place, N.W.,
Washington 12, D.C.

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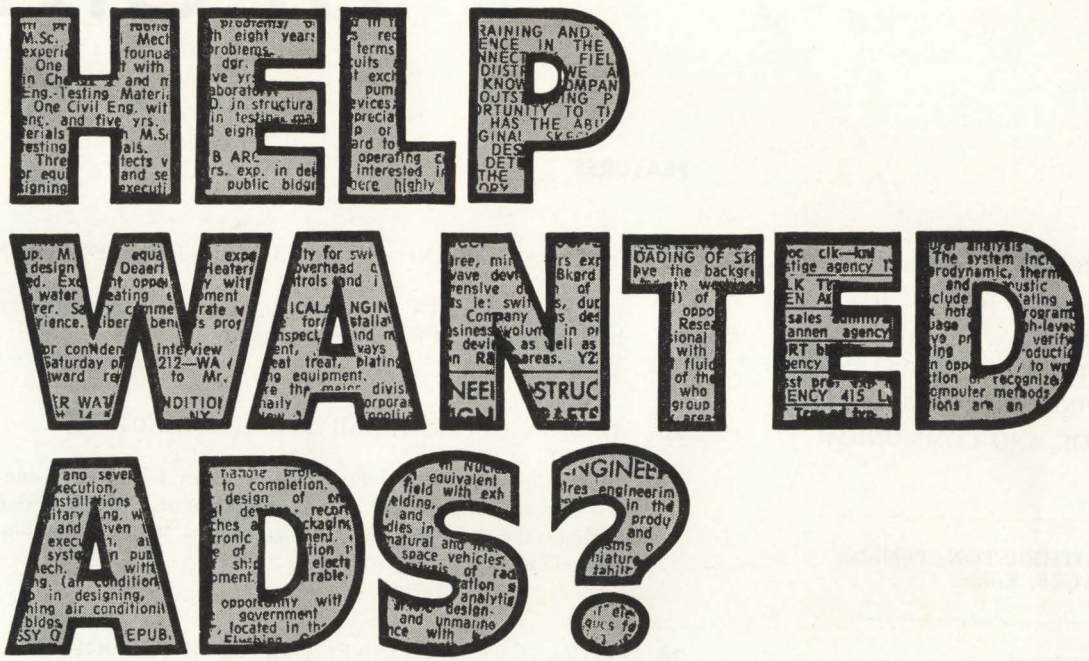

You're not alone. Most engineers and other professionals make it a habit to leaf through their Sunday paper, taking note of which company is working what space project, staffing a new facility, or just offering "challenging opportunities" in some Eldorado.

In your own browsing, you may have noticed advertisements from Honeywell Electronic Data Processing.

What's our story? No space vehicles, that's another division. No Eldorados either, although our Engineering and Research Center is located in one of Boston's more Eldorado-like communities. As to "challenging opportunities"—to that, we plead guilty.

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COMPUTER DESIGN

FOR ENGINEERING PERSONNEL RESPONSIBLE FOR THE DESIGN & APPLICATION OF DIGITAL CIRCUITS, EQUIPMENT, AND SYSTEMS IN COMPUTING, DATA PROCESSING, CONTROL AND COMMUNICATIONS.

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BPA

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26 ADVANCES IN CONNECTOR TECHNOLOGY

As part of a continuing series of CD editorial reports on new circuit connectors and interconnection systems, this article describes one company's design approaches to connector reliability in digital equipment.

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Tests and check-out operations on magnetic core memories have to be carried out by both the memory manufacturer and the user. The major performance characteristics and design criteria of memory exercisers, plane and stack testers, and core testers are discussed.

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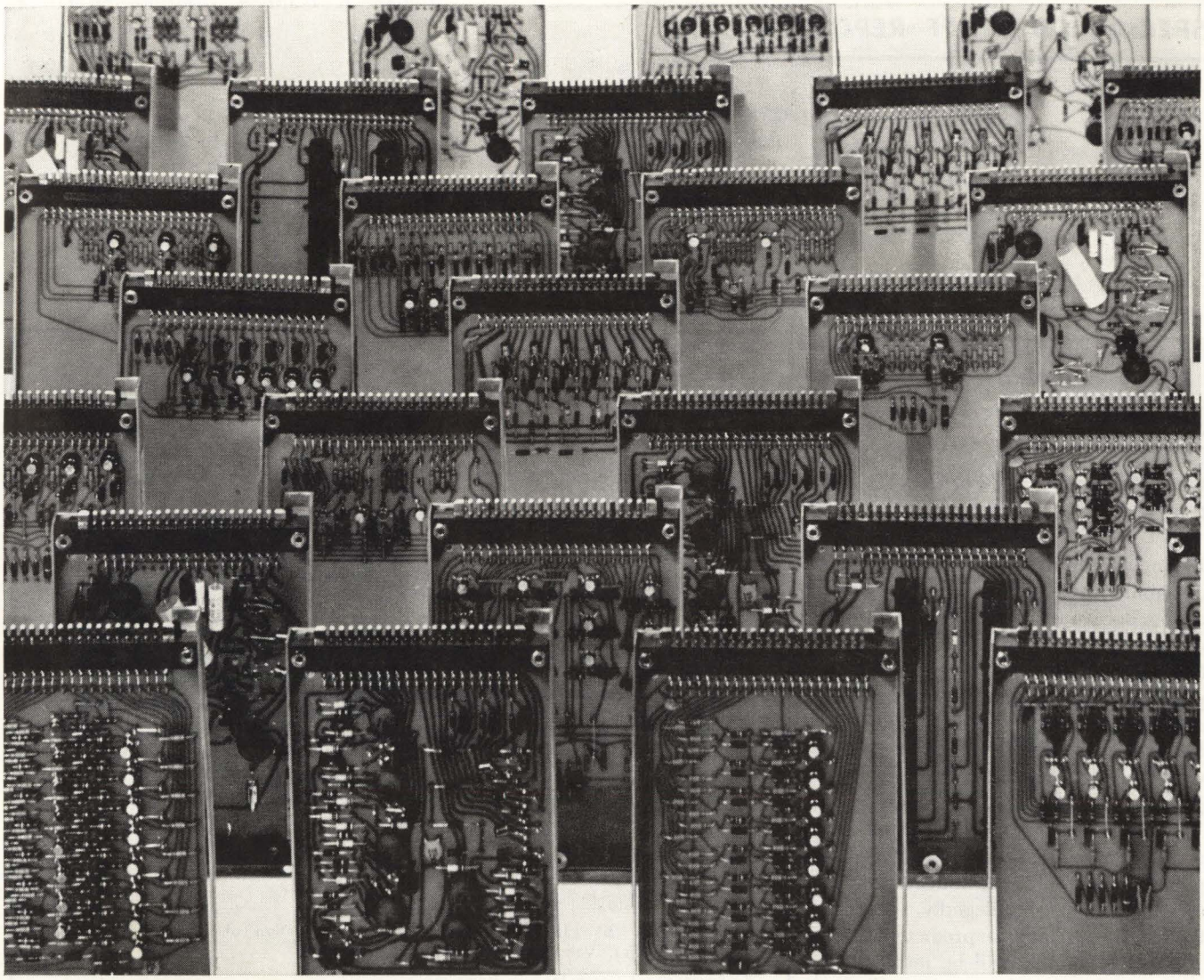

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CIRCLE NO. 3 ON INQUIRY CARD

William A. Gannon, Contributing Editor

THE COMPUTER... challenge to education

More emphasis must be placed on the basic concepts underlying the broad spectrum of digital technology.

Beginning with the first commercial electronic digital computer installed at the Bureau of the Census in 1951, a whole new industry has emerged that employs more than one million people and has reached an annual sales level (in 1963) of nearly two billion dollars. As of Jan., 1964, there were an estimated 14,000 general-purpose digital computers installed. These include over 100 different models; manufactured by 25 companies. The number of unfilled orders as of Jan., 1964, allegedly exceeds 9,000. By 1970, it is predicted that 100,000 computers will be installed.

Employment is also on the rise. It is estimated that over one million people are presently employed in the combined areas of computer design, development, operation, programming, and maintenance. However, a critical manpower shortage exists and the situation is expected to become even more severe before any significant improvement may be evident. The U.S. Dept. of Labor, which is keeping a watchful eye on the personnel placement and displacement situation, reports that in the programming profession alone, 50 thousand people are employed, and that by 1970, 200 thousand programmers will be required.

TABLE 1

Introductory Courses

1. History and Development of Computers
(a) Analog and Digital (b) Survey of Applications: business, scientific, misc. (c) Functional Sections of a Digital Computer: input, memory, control, arithmetic output.
2. Number Systems
(a) Radix Ten or Decimal System (b) Arbitrary Radix or Base N (c) Binary Number System (d) Conversion from One Radix to Another.
3. Binary Arithmetic
(a) Addition (b) Subtraction (c) Multiplication (d) Division (e) Iterative Processes
4. Binary Nature of Storage Devices
(a) The Flip-flop (b) Electrical Switches (c) Magnetic Devices
5. Logic
(a) Inductive and Deductive Logic (b) Assertion and Negation (c) AND, OR, NOT Logic Functions (d) NAND, NOR Variations
6. Boolean Algebra
(a) Postulates (b) Laws (c) Theorems (d) Simplification of Boolean Expressions (e) Truth Tables, Venn Diagrams, Veitch Charts
7. Synthesis of Computer Subassemblies
(a) Counters (b) Shift Registers (c) Half Adder, Full Adder (d) Half Subtractor, Full Subtractor (e) Serial and Parallel Adders (f) Accumulators (g) Logical Multiplication (h) Encoders and Decoders
8. Control Functions
(a) Comparators (b) Recognition Gates (c) Parity Generation (d) Parity Checking
9. Organization of a General-Purpose Digital Computer
(a) Input Unit: Data format and types of input devices (b) Memory Unit: Internal and external storage media, buffering, memory access and addressing techniques (c) Arithmetic Unit: Information handling and calculations (d) Control Unit: Directing the sequence of operations in a computer (e) Output Unit: Data format and types of output devices
10. Introduction to Programming
(a) Concept of a Stored Program (b) The Instruction Repertoire (c) Instruction Words and Operands (d) Storage Organization, Coding and Addressing (e) Flow Charts (f) Translating Flow Charts to Coded Instructions (g) Loops, Indexing, Branching, and Subroutines (h) Diagnostic Programming and Program Debugging (i) Assemblers and Compilers

Accelerated Growth

Certainly more important than statistics and predictions is a full realization of the socio-economic implications of the computer age. This young industry has spread its influence so diversely and so rapidly that it is being heralded by many as a second industrial revolution. In the wake of this accelerated growth is a preponderance of public misconception, distorted views and general unawareness of the capabilities, limitations and applications of general-purpose digital computers.

Computer uses have grown to include a vast range of jobs — with the major user categories being the federal government, automobile and machinery manufacturers, process industries, insurance and finance. Computers are calculating spacecraft orbits, process-

"Oww!" said Mblvt, hopping around on three legs and holding the fourth in his hands. Clumsy as usual, the brat had stumbled getting out of the spacescooter.

"Quiet!" I whispered sharply. "Do you want an Earther to see us like this?" I looked across from the grove of trees to the long, low building, but there was no sign that anyone had heard.

I set the scanner-synther to find and analyze some examples of the dominant Earth life-form. Then I set it to synth two individualized, self-powered, bioplastiform replicas of the adult male type, complete with concealed aerogills and appropriate clothing. They have two sexes just like us. Otherwise, their appearance and behavior is pretty weird. For instance, instead of nice, clean water, they breathe a mixture of air, smoke and fog.

Wearing the replicas, we stepped out onto the sidewalk and approached the building entrance. A sign said "Electronic Engineering Company of California." Mblvt was having trouble controlling his replica's two (!) legs. Why did he have to tag along, I thought, when the success of the entire invasion could depend on our getting information on the Earthers' most advanced data-handling technology.

After dealing with a live female receptionist (they don't have annuncimats) we found ourselves talking to a personable adult male Earther.

"Where did you say you're from?" he asked, as my autotrans unit interpreted for me.

"We're from, uh—" My portable scanner had found the name of one of their data-handling customers in a nearby file cabinet. "—from Hughes Aircraft. We'd like to investigate buying something that accepts analog or asynchronous digital data and prepares a blocked computer tape." As I rattled this off glibly into the autotrans I was glad I'd studied hard enough in elementary school to get a B in Comparative Infotronics.

"You couldn't have come to a better source,"[1] said the Earther. "In the past few years we've built over forty systems of that type for agencies all over the country. We call our general system the EECO 751 Computer Format Control Buffer. Step right this way, and— Oops!"

Mblvt had stumbled again. He swung one of his replica's arms to regain his balance and a piece of test equipment clattered to the floor. From across the room an older man, probably some kind of supervisor, gave us a sharp look. For some reason I didn't understand our guide seemed to be trying to smell Mblvt's Earther-replica's breath. Of course there wasn't any to smell, and the Earther looked puzzled.

"Here's a unit in final checkout," he said, gesturing toward an Earther-high cabinet. "The 751 can take data from many analog sources such as transducers or analog mag tape. Or from digital sources such as A-to-D converters, PCM telemetry decommutators and so on. And can put either kind into IBM-compatible tape. It's available with many options, depending on what you need."[2]

"How convenient," I said politely.

"Another thing," he went on. "Did you people ever have the experience of noodling around with this kind of equipment for weeks after delivery, before you could get it to produce acceptable tapes?"

"Uh, yes," I said at random. Out of the corner of my visual input I noticed the older Earther beckoning.

"Thanks to our experience with just about every kind of digital computer," our Earther said, "we know their characteristics inside and out. So we can usually have the customer's computer accepting tapes from a 751 within a matter of hours after we set the unit down on his floor. And the price! That's the big surprise. *Starts at forty K.*"

I was surprised, all right. I'd been told their unit of exchange was the "dollar."

"Say, would you excuse me for just a moment?" He walked over to the supervisor type. They were out of normal earshot. I readjusted for tight directional input and turned up the gain.

"—know everybody in those sections at Hughes,"[3] the older Earther was saying. "We recently delivered a 751 to their Culver City plant. Neither of these two characters looks familiar."

"You don't suppose they're spies from the competish?" the younger one suggested. "Trying to get the scoop on our latest products?"

My autotrans drew a blank on the word "competish." I scanned frantically among the EECO filing cabinets for a "Competish Company." Or an enemy nation. Nothing.

"That must be it," the older Earther said. "I'm surprised they'd send a heavy drinker on that kind of errand."

Heavy drinker! Suddenly it dawned on me what "Competish" must be their word for.

"Mblvt!" I hissed. "They're wise to us! They know we're from the Deuterium Planet! Let's get out of here! This may cancel the entire plan to invade Earth!" We made a dash for the door.

Moments later we lifted off in the spacescooter. I turned on the turbuloscreen so if any Earthers happened to be watching we would merely look like a medium-sized dust-devil as we ascended.

At 187,000 feet altitude a familiar voice blasted into my input, "Tgpdk! Where have you been?" It was Pa.

"Your mother and I have been frantic!" he scolded, sucking the spacescooter through the in-hatch of our spacehouse. "Have you been down there playing Invasion again?"

I hung my head guiltily.

"You know how we disapprove of that silly, anachronistic game! And letting your baby brother come along! Why, he's hardly old enough to know how to walk! I thought you had more sense!"

"I'm sorry, Pa," I said. But I wasn't. Those EECO guys had been real neat fun to talk to.[4]

ing payrolls, updating banking transactions, controlling chemical blending processes, and assisting in medical diagnoses. They are simulating business enterprizes and aircraft flight characteristics, automating airline reservation procedures, controlling inventories and analyzing weather data. Either directly or indirectly, the benefits of modern computing systems are serving engineers, businessmen, doctors, scientists, educators, lawyers, bankers, publishers, printers, and many others.

The Role of Education

Prominent educators, government officials and industry leaders are actively promoting the acceptance of computing and data processing as a vital part of a formal education. Reaction to these efforts is clearly demonstrated by the increasing number of computer courses being offered at the secondary, vocational, undergraduate and graduate levels. Courses in computer fundamentals are preparing students for careers in the computer industry, thus providing a partial solution to the industry's manpower shortage problem. And, perhaps more important, is the fact that students pursuing other careers will be alerted to the efficiencies of modern computing systems, and will be in a better position to benefit fully from computers employed within their own particular fields of endeavor.

Concluding the conference on "Computer Oriented Mathematics and the Secondary School", held in May, 1963 by the National Council of Teachers of Mathematics, was a resolution that an exhaustive national effort would be undertaken to introduce computer-related subjects in the high school curriculum. It was further recommended that "units of study in computer-oriented mathematics be introduced early in the curriculum and continued with increasing emphasis throughout the mathematics curriculum". The conference participants agreed that all secondary school students, whether planning to continue their formal education or not, and whether planning to pursue careers in the computer industry or not, would benefit from the study of computing and data processing.

Several educational associations, schools and industrial groups have not only recognized the urgency of the computer education situation, but have taken commendable action in instituting, expanding and improving curricular at all levels of instruction. Some of the major programs of particular importance are:

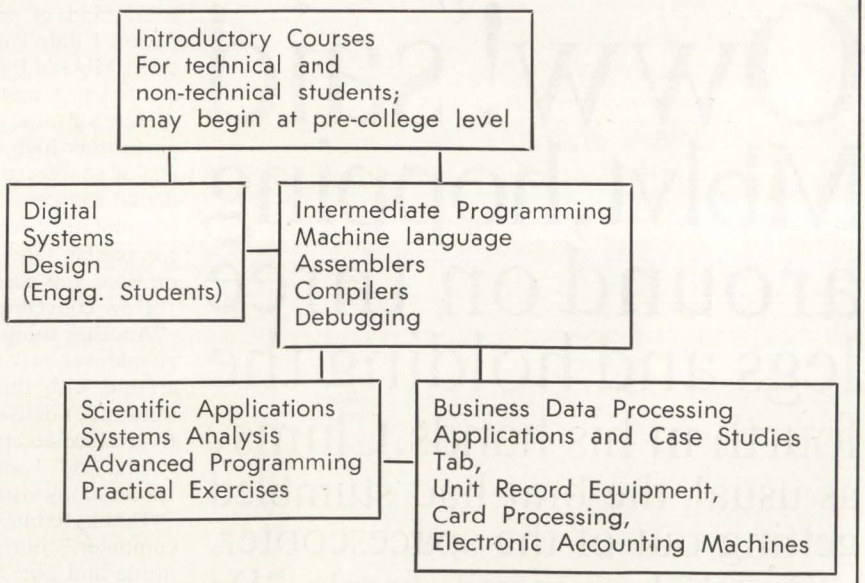


Fig. 1 Typical Curriculum Outline

- The Nat'l. Science Teachers Assoc. has established the Project on Information Processing to serve as an information exchange center concerning computer-related activities in the Nation's high schools. The Project is under the direction of Dr. Hugh Allen, Jr., who maintains headquarters at Montclair State College, Upper Montclair, N.J.

- The Division of Vocational and Technical Education of the U.S. Office of Education has published "A Suggested 2-Year Post High School Curriculum for Computer Programmers and Business Application Analysts". This curriculum guide is being distributed to vocational schools and junior colleges offering courses in business oriented computing.

- The Nat'l Council of Teachers of Mathematics has instituted a continuing program for reviewing and evaluating equipment and course materials and stimulating the development of computer courses at the secondary school level. The NCTM sponsored the Computer Oriented Mathematics Project which began in 1960. In 1963, the Project committee published a book to illustrate to teachers how a digital computer can serve as a tool to motivate the study of math.

- The Ford Foundation sponsored the "Project on the Use of Computers in Engineering Education" which was a 3-year study program conducted by the College of Engineering of the Univ. of Mich. A major objective of the Project was the development of computer courses for under-graduate engineering students.

- An increasing number of vocational schools and junior colleges are offering courses in data processing with the support of federal funds provided under Titles III and VIII of the Nat'l. Defense Education Act.

- The Wash., D.C., Chapter of the Assoc. for Computing Machinery (ACM) conducted extensive pilot courses in 5 school districts in the Wash., D.C., area. Under the direction of George C. Heller, Nat'l Educ. Chairman of ACM, and with the assistance of various local industry personnel, the 2-year experimental program elicited considerable interest from high school students and educators. Over 350 high school students were enrolled.

- Summer workshops and seminars to indoctrinate secondary school teachers in computer fundamentals are being organized at many colleges and universities. Many secondary school teachers are attending these programs on Nat'l Science Foundation fellowships.

- Over 300 colleges are offering formal courses in computer-related sub-

jects. According to a recent survey, about 200,000 college students have been exposed in the past year to some form of computer course or project involving the use of a computer.

• The Data Processing Management Assoc. has developed and administers the "Examination for Certificate in Data Processing". In 1963 the examination was administered at 56 colleges and universities.

Proceed with Caution

Reaction to the much publicized shortage of experienced computer personnel has had some rather negative effects. The rush to close the EDP education gap in many instances has inadertently resulted in placing undue emphasis on learning manipulative skills and design details of specific computers rather than the basic concepts underlying the broad spectrum of digital technology. In an industry well noted for its rapid growth and continual advancements, persons trained in isolated specialties could very likely become victims of technological unemployment. Certainly operating skills are desirable, but not nearly as important as the understanding of and the ability to apply the principles around which digital computer technology evolves.

Perhaps another potential danger is the tendency to rush immediately to the more glamorous lessons involving programming and machine operation and there-by alloting insufficient time to fundamentals. Reducing instruction to the problem-solving framework of a specific computer and actually executing student-prepared programs is an obvious goal of any computer course. However, this goal should be approached from the right direction in a well-balanced curriculum.

Introductory Courses

The successful development of modern computing and information processing systems is largely attributed to the extensive application of digital logic, Boolean algebra and binary arithmetic. Consequently, these concepts and the techniques used in applying them are recognized as vital areas of knowledge. While the design of computer equipment and programming techniques are in a constant state of evolution, these basic concepts remain unchanged.

The curriculum outline in Table I

provides a nucleus of subject material that should be included in an introductory computer course. The study units in Table I are basic to an understanding of electronic digital computers irrespective of end-use or specific areas of application. This curriculum outline encompasses the minimum requirements from which students may proceed to the next higher level of instruction as shown in Fig. 1.

The introductory course outlined may be given to technical and nontechnical students as no electronics and no math other than algebra are required; course may begin at precollege level. Students completing the introductory course may enroll in more advanced courses which are oriented toward their specific interests and needs. Major course offerings at subsequent levels of instruction include scientific applications, digital systems design, and business data processing. END

IFIP CONGRESS 65 CALL FOR PAPERS

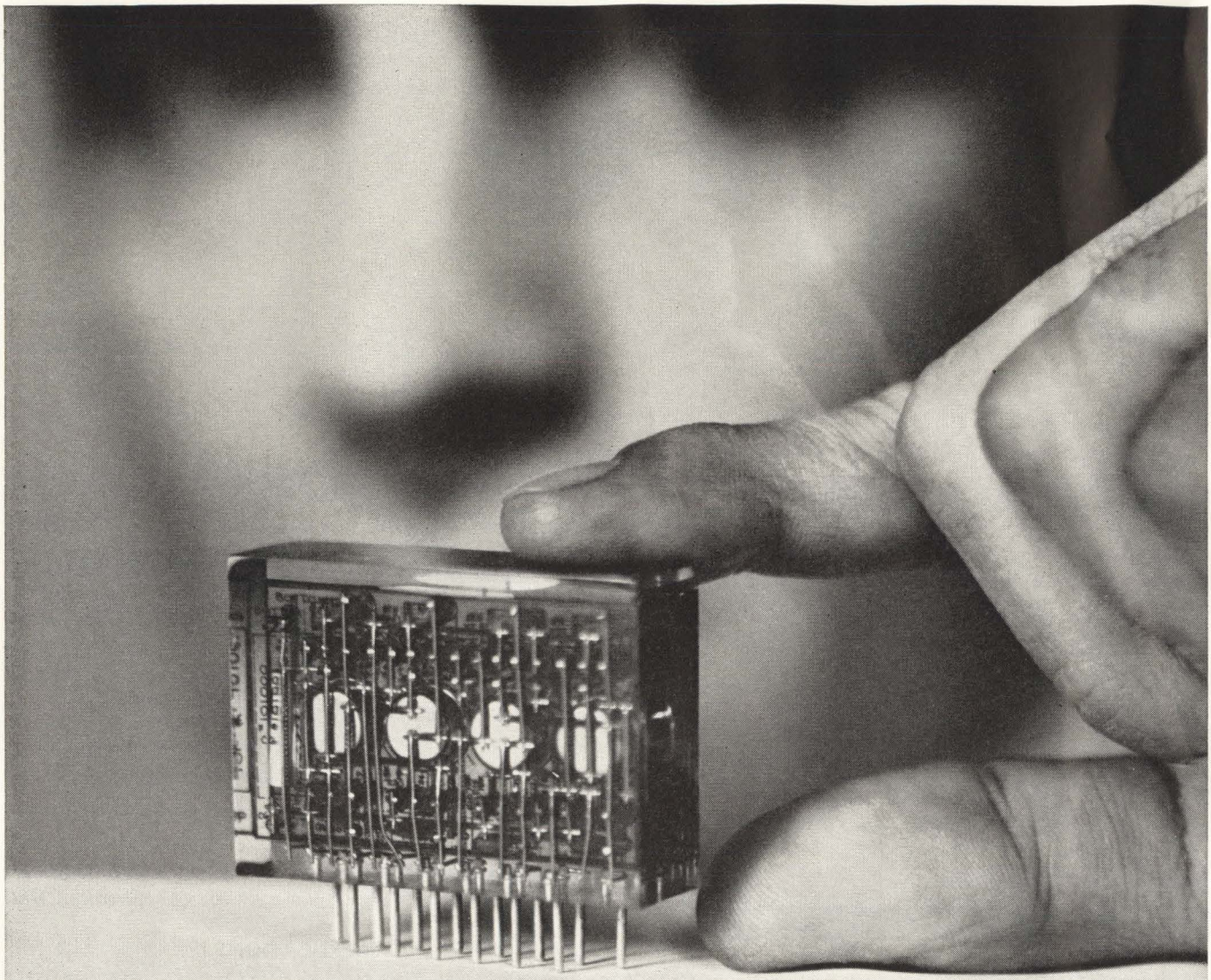
A call for scientific papers on information processing has been issued by the Program Committee of IFIP CONGRESS 65. Members of this program committee are among the world's leading information scientists. But the information processing field is growing with such astonishing rapidity that they are seeking evidence of work so new it might be overlooked at the time the official invitation list is issued later this year. Consequently, while there will not be the open competition normally associated with the development of technical conference programs, submitted papers of sufficient merit will be added to the total list of speaker candidates whose work is already known to the Program Committee.

IFIP Congress 65 is a triennial international congress on information processing sponsored by a 23-nation Federation for Information Processing. It will convene at the New York Hilton May 24th to 29th, 1965 and will attract the leaders of the scientific and business community most concerned with the development or use of computers and information processing techniques.

The scientific program of IFIP Congress 65 will cover the entire spectrum of information processing. Broadly speaking, this includes automata theory and mechanical linguistics, mathematical methods, programming languages and techniques, information systems, and hardware (components, circuits, equipment). These subjects have been exploded into an enormous number of topics to be treated in the six days of the technical program.

Because the information sciences involve so many disciplines, the program of IFIP Congress 65 has been especially constructed to assure interdisciplinary communication among specialists of various fields in an Orientation Program while providing a Specialist Program for communication between workers in the same fields.

Although background information will be presented at the start of talks in the Orientation Program, the lectures themselves will not be tutorial surveys. They will be comprehensive presentations of significant work or professional reviews by distinguished researchers or pioneers in their respective fields. On the other hand, the Specialist Program, consisting of lecture sessions, panels, and symposia, will limit the length of paper presentations to allow much time for discussion. The IFIP Congress 65 official call for papers is only for the symposia portion of the Specialist Program. Because the Program Committee is an extraordinarily well-informed jury, they have set stringent rules for paper submission. These are detailed in an official document, entitled "IFIP CONGRESS 65 Call for Papers" available from: IFIP Congress 65, Inc., 345 East 47th St., (at United Nations Plaza), New York 17, N.Y.



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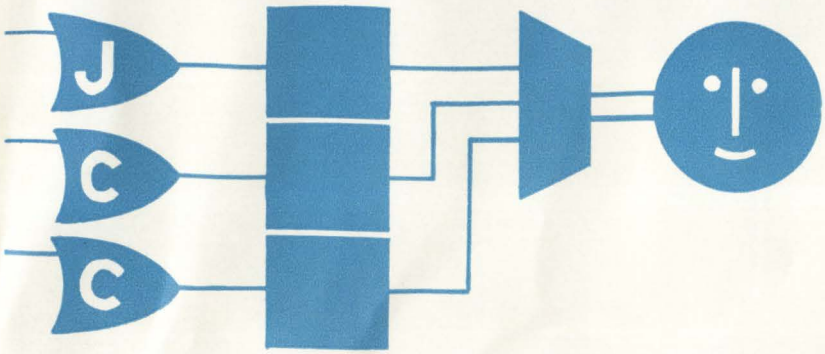

THE 1964 SPRING

JOINT COMPUTER CONFERENCE

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SUMMARY OF TECHNICAL PROGRAM

The largest number of exhibitors in the history of the JCC are scheduled to display their products at the Sheraton-Park Hotel's Exhibition Hall. All technical sessions will also take place at the hotel.

The 1964 SJCC officially opens Tuesday morning, April 21, however, you can register in advance on Monday evening, 5 to 9:30 P.M., in the Continental Room of the Sheraton-Park.

Special activities during the conference include some interesting field trips, a Computer Science Theatre presenting continuous movies on computers and information processing technology, and an educational symposium.

The Technical Program will cover, for the most part, the applications of computers and data processing equipment. Many of the papers appear to be software oriented, however, there is much to interest the digital systems designer. Here is a brief summary of some of the scheduled papers.

Tuesday, April 21 ..... *2-5:30 P. M.*
..... *Sheraton Hall*

APPLICATIONS

A COMPUTER TECHNIQUE FOR PRODUCING ANIMATED MOVIES
Kenneth C. Knowlton, Bell Telephone Labs

A computer technique has been developed for the production of animated diagram movies. It has been implemented on the IBM 7090 by MACRO FAP programming.

SIMULATION OF BIOLOGICAL CELLS
Walter R. Stahl, Robert W. Coffin, and Harry E. Goheen, Oregon Regional Primate Research Center

A cell model that uses string-processing finite automata as its central feature is presented. Numerical rate factors are given a less primary position than in systems described by differential equations. A simulation of this type, based on 43 "algorithmic enzymes" has been programmed on an SDS-920 computer.

SIMULATION OF HUMAN INTERACTION IN SMALL GROUPS
John T. and Jeanne E. Gullahoun, Michigan State Univ.

An operating computer program simulating simple face-to-face interaction among humans is described. Participants in small groups are programmed to be capable of receiving and evaluating stimuli, predicting the reward value of alternative responses, selecting socially profiable activities, and modifying their perceptions of group members during the course of interaction so that their behavior will increasingly adapt to the situation.

REAL-TIME COMPUTER STUDIES OF BARGAINING BEHAVIOR

Robert J. Meeker, Gerald H. Shure and William H. Moore, Jr., System Development Corporation

This paper reports on a two-person, non-zero sum bargaining game in which the computer is used as an experimental tool for on-line analysis, umpiring, control, and recording of subject behavior.

REAL-TIME QUICK-LOOK ANALYSIS FOR THE OGO SATELLITES

R. J. Coyle and J. K. Stewart, Datatrol Corporation

Real-time programming system provides quick-look analysis and control for the NASA Orbiting Geophysical Observatory series of satellites. Telemetry data is transmitted from tracking stations to Central Control, an installation consisting of an SDS-920 computer and NASA-designed special-purpose consoles and equipment.

Tuesday, April, 21 ..... *5-5:30*
..... *Cotillion Room-A*

COMPILERS — TECHNICAL

A GENERAL-PURPOSE TABLE-DRIVEN COMPILER

Stephen Warshall and Robert M. Shapiro, Computer Associates, Inc.

This report describes a general-purpose language and machine-independent compiling algorithm, together with a method for partially automating the process of particularizing the algorithm to a specific source language and target machine. The compiling algorithm was devised with generality of application and efficiency of object code as the primary design considerations, and is therefore not the fastest possible compiler for a given source target-pair.

Wednesday, April 22 ..... *9-11:30 A. M.*
..... *Cotillion Room-A*

COMMAND AND CONTROL

ON THE EVALUATION OF THE COST-EFFECTIVENESS OF COMMAND AND CONTROL SYSTEMS

N. P. Edwards, Weapons System Evaluation Group

The expression "command and control" is widely used and many "C and C" systems are being developed. Some facets of the problem of determining the cost-effectiveness of these systems are examined and conclusions are drawn regarding the utility of analytical techniques for assessing the cost-effectiveness of command and control systems. Definitions of terms are presented and control systems are reviewed as a basis for the discussions of command systems.

SOME COST CONTRIBUTORS TO LARGE-SCALE PROGRAMS

Burt Nanus and Leonard Farr, System Devel. Corp.

This paper reports on a recent attempt to identify those factors which contribute most significantly to the cost of large-scale programs; that is, to the number of programmer man-months and computer-hours that will be required for a given job.

FRACTIONIZATION OF THE MILITARY CONTEXT

Frederick B. Thompson, General Electric Company

The task of expanding our understanding and knowledge is self-accelerating. The extent of our understanding and its rate of expansion ultimately exceed the means of communication. Consistency cannot be maintained, and the over-all context fractionates. The resulting breakdown in communication is rapidly reaching crisis proportions. At the same time, advances are being made in the technology of information. Will these advances provide ways to resolve the crisis, to re-establish channels of communication, or will they contribute to the further fractionization of our undertsanding? A perspective is presented from which we can explore the dynamics of information as it affects today's institutions. From this perspective, requirements for constructive application of the new technological tools in command and control will be developed.

SOME PROBLEMS ASSOCIATED WITH LARGE PROGRAMMING EFFORTS

Almon E. Daniels, Institute for Defense Analyses

A plea is made for full user-technician collaboration throughout the design, construction, and testing of the large data systems. It is recommended that an incremental approach be taken to implementation in anticipation of charging requirements. The need for exercising the system in a simulated environment is stressed. Problems relating to documentation, level of effort, and estimation of time required are discussed.

Wednesday, April 22 ..... *1:30-3:30 P. M.*
..... *Cotillion Room-A*

HYBRID SYSTEMS: TUTORIAL

HYBRID COMPUTATION — WHAT IS IT? — WHO NEEDS IT?

Thomas D. Truitt, Electronics Associates, Inc.

The elements of present day hybrid simulators are discussed; their incompatibilities and limitations are examined. The relationship of the computer system to the simulation problem is analyzed. The application domains in which hybrid computation is and is not appppropriate are discussed with emphasis on those basic characteristics that make hybrid simulation appropriate.

Wednesday, April 22 ..... *3:30-5:30 P.M.*
..... *Cotillion Room-A*

HYBRID SYSTEMS: TECHNICAL

A HYBRID ANALOG-DIGITAL PARAMETER OPTIMIZER FOR ASTRAC II

Baker A. Mitchell, Jr., University of Arizona

A new automatic multi-parameter optimizer for iterative differential analyzers employs sequential random parameter perturbation. Binary counters operate simple digital-to-analog converters to implement parameter storage, multiplication, and step-size changes. All-digital logic yields different types of random perturbations.

A HYBRID ANALOG-DIGITAL PSEUDO-RANDOM-NOISE GENERATOR

R. L. T. Hampton, University of Arizona

Intended to replace conventional random-noise generators in analog and hybrid computer simulations, this hybrid generator is capable of producing four essentially incorrelated binary outputs from a single 25-stage shift register. The length of the pseudo-random output sequence is 33,554,431 bits which is equivalent to several thousand computer runs. This hybrid noise generator has several striking features not generally shared by existing analog noise source.

A 2MC BIT-RATE DELTA-SIGMA MODULATION SYSTEM FOR ANALOG FUNCTION STORAGE

H. Handler and R. H. Mangels, University of Arizona

Modified delta modulation (delta-sigma modulation) permits magnetostrictive delay line function storage of analog data with the significant advantages of pulse regeneration with clock-gated logic and relatively inexpensive conversion equipment. Five to 10 msec delay lines with a 2 mc bit-rate accommodate analog signals of up to 8 kc with phase shift below 2 degrees; total dynamic error is within 0.2 per cent of half scale up to 1 kc. An adaptive filter permits a further trade-off of accuracy for bandwidth during computation.

Wednesday, April 22 ..... *2-4:30 P.M.*
..... *Cotillion Room-B*

ARTIFICIAL INTELLIGENCE

A COMPUTER-SIMULATED ON-LINE LEARNING CONTROL SYSTEM

J. Douglas Hill, G. McMurtry, and K. S. Fu, Purdue University

The structure of a learning control system combines digital memory and logic circuitry with an adaptive system. Data obtained through adaptation is stored (remembered) and later utilized to improve the system performance. The learning control system will operate satisfactorily under changing environmental conditions in which an adaptive system fails to improve the performance. The general learning system operation is outlined in this paper and a simple experimental system which illustrates the improved performance is discussed.

A HEURISTIC PROGRAM TO SOLVE GEOMETRIC-ANALOGY PROBLEMS

Thomas G. Evans, Office of Aerospace Research

A program has been developed which is capable of solving a wide variety of intelligence-test problems of the "geometric-analogy" type. The task involved in these problems can be characterized by the question: Figure A is to Figure B as Figure C is to which of the given answer figures? The program, written in the LISP language, has solved a number of problems of this class.

EXPERIMENTS WITH A THEOREM-UTILIZING PROGRAM

Larry E. Travis, System Development Corporation

This paper raises the issue of the importance for machines acquiring skill by learning theorems and developing sensitivity to the occasion on which it is appropriate to apply them. A theorem-learning-and-utilizing program has been written and tested in a simple but paradigmatic problem domain.

Wednesday, April 22 ..... *2-5:00 P.M.*
..... *Sheraton Hall*

EVALUATING COMPUTER SYSTEMS

ANALYTICAL TECHNIQUE FOR AUTOMATIC DATA PROCESSING EQUIPMENT ACQUISITION

Solomon Rosenthal, Headquarters, USAF

The Analytical Technique for ADP equipment acquisition is designed to facilitate competitive selection of electronic data processing equipment whenever acquisition is contemplated. The four-part technique is based on use of standard formats for preparation of specifications, standard formats for submission of proposals by vendors, validation of proposals, and scoring of these proposals by using standardized factors, weights, and formulae. Factors and weights can be varied to best suit each individual selection, making the technique flexible and universally applicable. Each of the four parts is presented in sufficient detail to permit its adoption by anyone. If the built-in mechanics for modification are used, competitive selection

of any kind of product or service is possible within the framework of the technique.

COST-VALUE TECHNIQUE FOR EVALUATION OF COMPUTER SYSTEM PROPOSALS

Edward O. Joslin

This paper discusses the requirements for any objective evaluation technique, points out some of the major strengths and weaknesses of the Weighted Scoring Technique, and describes how the Cost-Value Technique not only fulfills the requirements of an objective evaluation technique, but overcomes some of the weaknesses found in the Weighted Scoring Technique. It also contains a detailed description of the Cost-Value Technique, with examples of the types of items to be considered in the evaluation as well as the methods of determining the cost-value of these items. Some possible additional improvements that might be made in the Cost-Value Technique are indicated.

THE USE OF A COMPUTER TO EVALUATE COMPUTERS

Donald J. Herman, Compress, Inc.

This paper will discuss the assistance which can be given to management in making proper decisions regarding the use of computers through the art of simulating data processing problems on data processing equipments. SCERT—Systems and Computers Evaluation and Review Technique — is a simulation program which will be discussed in terms of the inputs required for describing a computer problem, its environment, the computers to be evaluated, and the output reports which will be generated. The data contained in these reports are detailed projections of time, manpower, and costs associated with using a computer to process a problem which has been defined to the SCERT program.

Thursday, April 23 ..... *9:00 A.M.-12 Noon*
..... *Cotillion Room*

LOGIC, LAYOUT AND ASSOCIATIVE MEMORIES

ON THE ANALYSIS AND SYNTHESIS OF THREE-VALUED DIGITAL SYSTEMS

Prof. J. Santos and H. Arango, Argentina

Post algebras have been treated quite extensively from a purely logical point of view. In this paper, some techniques of analysis, minimization, and synthesis of Postian functions are first introduced, as more or less obvious extensions of Boolean methods. That theory leads to a systematic implementation procedure for combinational and sequential functions.

AN ALGORITHM FOR PLACEMENT OF INTERCONNECTED ELEMENTS BASED ON MINIMUM WIRE LENGTH

R. A. Rutman, AC Spark Plug Div., G.M.C.

The layout and interconnection of microminiaturized components have become such complex tasks that automatic layout programs are proving very useful. Layout is usually a three-step process consisting of the allocation of components to boards, their placement on the boards, and finally routing of their interconnections. This paper describes in detail a computer program which automatically performs the placement of the components so that the overall interconnection wire length tends to a minimum. The procedure uses integral linear programming and consists of essentially two parts. The first part reduces the lengths of the longest wires and the second reduces the total wire length. This process is shown to be more effective in decreasing total wire length than the usual one-step process.

STUDIES OF AN ASSOCIATIVELY ADDRESSED DISTRIBUTED MEMORY

G. J. Simmons, Sandia Corporation

A memory model is proposed which uses associative addressing and distributed storage. The addressing is accomplished by a non-linear mapping of points in the input space onto the vertices of a hypercube embedded in a much higher dimensional space. The dimension of this image space is chosen to be sufficiently great so that a hyperplane can be passed through the origin and such that the distances to the image points are the scaled functional values which are to be stored. The distributed memory is achieved in the n-tuple representation of the hyperplane. The storing of data in such a memory implicitly involves the solution of extremely large linear systems, under the unusual restraints that only one linear element be available to any one time, and that there be no detailed memory of previous elements. The algorithm developed to deal with this class of problems is discussed.

DESIGN OF AN EXPERIMENTAL MULTIPLE INSTANTANEOUS RESPONSE FILE

E. L. Younker, C. H. Heckler, Jr., D. P. Masher, and J. M. Yarborough, Computer Techniques Lab, Stanford Research Institute

An experimental model of an electronic reference retrieval file in which all file entries are interrogated simultaneously has been designed and constructed. The experimental model is designed to store the indexes to 5000 documents. Each document index consists of an accession number and up to eight English words (descriptors) that are closely related to the contents of the document. The descriptors are selected from a 3000-word dictionary. A search question, consisting of one to eight descriptors in their natural English form, is entered by means of an electric typewriter. The document indexes and the dictionary words are stored in wiring patterns associated with arrays of linear ferrite magnetic cores. During entry of the search question, the dictionary magnetic store is interrogated by the alphabetic code of each search word. If the word is not contained in the dictionary, it is automatically rejected. After all words of the search question have been entered, the document magnetic store is interrogated by the search question in superimposed code form. Response to a word validity test or to the file search is obtained in less than 6 microseconds.

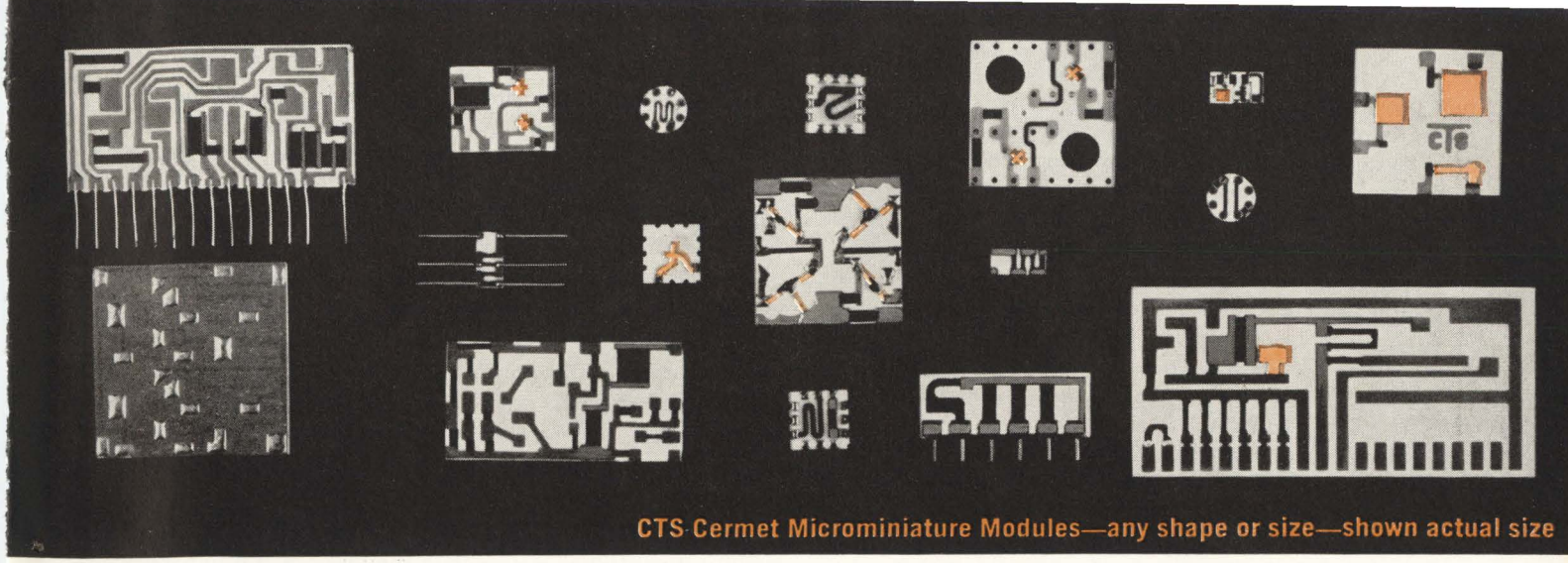
Thursday, April 23 ..... *2-5:30 P.M.*
..... *Sheraton Hall*

INFORMATION RETRIEVAL

RESEARCH IN AUTOMATIC GENERATION OF CLASSIFICATION SYSTEMS

Harold Borko, System Development Corporation

In an information storage and retrieval system, classifica-



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- **Extremely tight quality control** in purchased materials inspection, in-process control of production procedures, step-by-step product inspection, and quality assurance program on completed product.
- **Fired at temperatures exceeding 650°C** so cermet resistors, capacitors and conductive circuit take excessive overloads without failure. Cermet resistors and capacitors operate continuously at 275°C; take short periods of 500°C.

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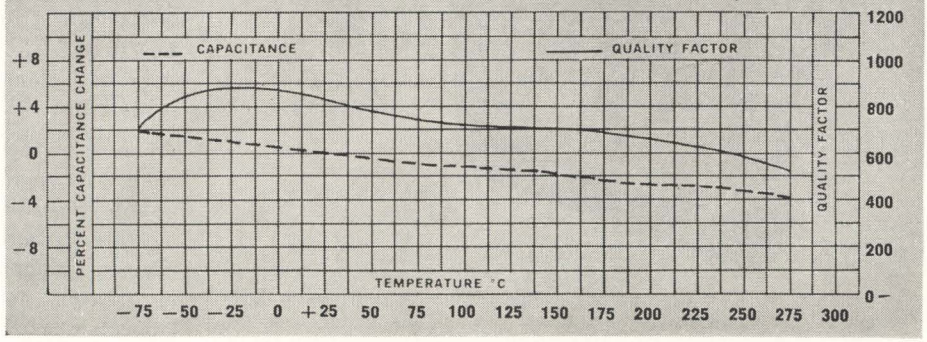

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tion provides a means for organizing a mass of material into groups so that related items are brought together in a systematic fashion. By grouping documents into categories, the number of items to be scanned in response to a search request can be reduced and the efficiency of the system increased. To design a classification system, one must specify the number of classes to be established and the principle to be used in determining class membership. A number of mathematical procedures for devising classification schedules are reviewed; these include factor analysis clump theory, and latent class analysis. These and similar techniques can also be used to classify documents into correct categories automatically and thus speed up the processing of incoming material. Results appear promising, and further research is being undertaken to determine the retrieval effectiveness of automated indexing and classification systems.

INFORMATION STORAGE AND RETRIEVAL: ANALYSIS OF THE STATE-OF-THE-ART

George Arnovick, J. A. Liles, A. H. Rosen, and J. S. Wood, Space and Information Systems Division, North American Aviation

The state-of-the-art of information storage and retrieval (IS&R) is outlined and presented in a form assimilable by those whose background is technical or, more specifically, computer hardware oriented, but whose knowledge of IS&R techniques and applications is at best limited. The presentation is necessarily comprehensive but not discursive. On the generally-accepted presumption that retrieval of information is as sucessful as its representation in the file, greater attention is focused on indexing. Some of the controversial issues and unsettled problems, such as the role of relationships and context of index terms, are critically examined. Potential solutions to these problems, including automatic input techniques and statistical approaches, are also discussed. Subsequent consideration is given to the problems of information dissemination, abstracting, storage, retrieval, display, reproduction, and communication links.

TRAINING A COMPUTER TO ASSIGN DESCRIPTORS TO DOCUMENTS: EXPERIMENTS IN AUTOMATIC INDEXING

M. E. Sterens and G. H. Urban, National Bureau of Standards

Preliminary results are reported for 64 test items run against two 100-item teaching samples. A presumably representative sample of documents indexed on the basis of human subject-content analyses is processed by computer to provide **ad hoc** statistical associations between significant words occurring in the titles and texts of abstracts of these sample items, and each of the descriptors manually assigned to them.

EXPERIMENTS IN INFORMATION CORRELATION

J. L. Kuhns and C. A. Montgomery, Computer Division, Thompson Ramo Wooldridge

In a technical information system, it is supposed that many users will want output in order to verify hypotheses or answer questions, or form new hypotheses. The information correlation experiments presented in this paper suggest an approach to the problem of assimilating information for the second purpose, and were designed along the following lines. Assuming that structured information is easier to assimilate than unstructured information and consequently that degrees of assimilability correspond to degrees of structure, two different degrees of structure were developed for a set of sentence fragments. The structured data was then tested for assimilability by asking experimental participants to derive inferences from the fragment sets. Results of these experiments are given in detail and a system for quantitative evaluation of inferences is discussed.

SOME FLEXIBLE INFORMATION RETRIEVAL SYSTEMS USING STRUCTURE MATCHING PROCEDURES

Gerard Salton and E. H. Sussenguth, Jr., Harvard University

Many constructs of interest in data processing are conveniently represented in two dimensions by abstract graphs consisting of sets of points (nodes) and interconnections (branches) between certain pairs of nodes. Typical examples are physical systems such as electrical or pipeline networks, computer process charts, storage allocation schemes, and code marks of various kinds. In information retrieval, the nodes may represent keywords or terms, and the branches may represent relations between terms. To retrieve information, it is then necessary to compare the two-dimensional structures representing items of information, or documents, with the structures representing search requests. In the present study an efficient structure matching procedure is outlined which can be used to alter the search requests so as to force agreement with the stored information identifications.

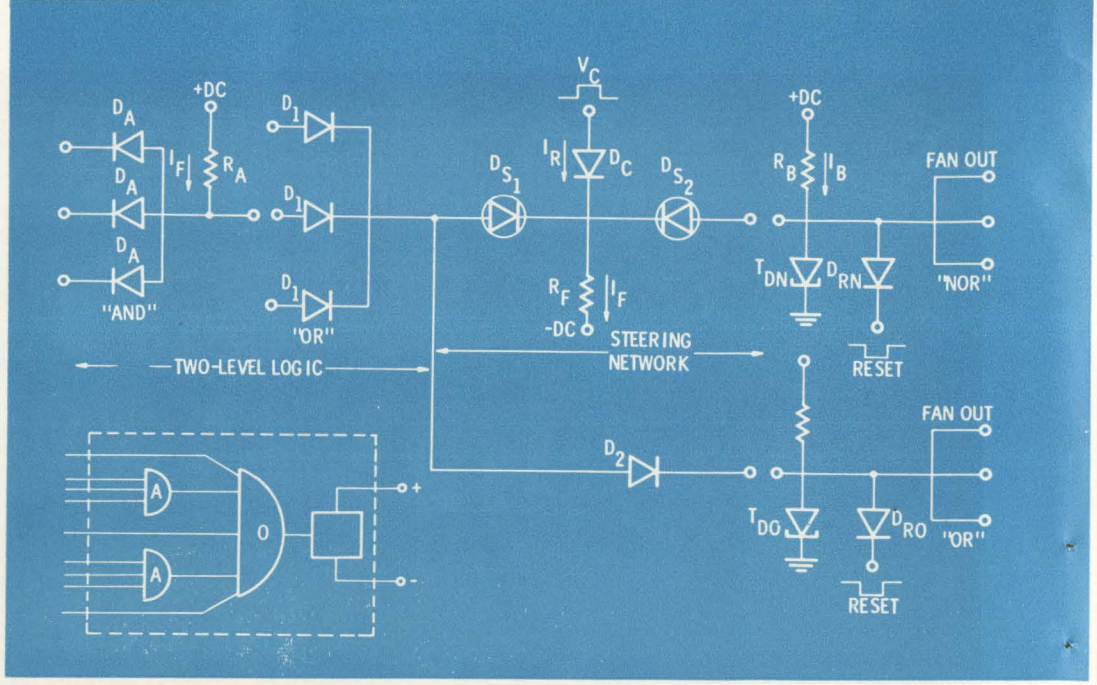

Fig. 1 General Purpose And-Or-Nor Circuits and Equivalent Logic Function

Brian E. Sear, *Research Scientist, Martin Company, Baltimore, Md.*

DESIGN OF MODULAR 250 MC CIRCUITS

For several years, the transistor has reigned supreme as a logic switching device. Properties such as high gain, reasonable speed, logical variability, low cost, and small size have created and maintained its widespread acceptance. Although the advent of the tunnel diode in 1958 made such an impact that it was heralded as the switching device of the next generation computers, interest quickly waned when the tolerance problem was appreciated. Several researchers (Refs. 1 through 6) have shown that single-stage tunnel diode circuits have a low logical gain with tight tolerances, which make these circuits of little or no value for general purpose computer logic.

The recent development of circuits which combine a storage diode (charge transformer) with the tunnel diode has made available general purpose computer circuits with a gain bandwidth tolerance performance and logical flexibility previously unattainable in nanosecond logic (Refs. 7 through 9). The key to this success is the charge transformer which gives considerable interstage current gain with a gain bandwidth product compatible with the tunnel diode on the order of 10 kilomegacycles. This combination provides a 10-to-1 improvement over transistors or tunnel diode circuits, while allowing a variety of logical functions to be generated by different modes of coupling connections.

This article, based on a paper presented at the 1963 National Electronics Conference, discusses the achievement of the gain bandwidth tolerance improvements into practical modular hardware at a 250-megacycle information rate, similar in logical and mechanical versatility to transistor modular equipment which is only capable of up to 25-megacycle rates (Ref. 10). The design objectives were large fan-in/fan-out ratios, wide tolerances, reasonable power consumption, logical flexibility, modular packaging, standard-sized components and repairability. These objectives were, in general, achieved by the circuits outlined in the following section.

The physical operation of the storage diode (charge transformer) is not described because it is covered in detail in Refs. 7 and 9.

And-Or-Nor Logic

The circuit arrangement, Fig. 1, can be used as three separate circuits or as a combined two-level three-function logic module (Ref. 9).

The ability of this circuit to generate a signal and its complement simultaneously at the phase rate is due to the storage diode pair, D_{S1} and D_{S2}, in the steering network. If all the inputs to the OR level D_1 are 0 ($+V_P$), I_F flows in D_{S2} but not in D_{S1}; therefore, the set clock drives reverse current through D_{S2} (setting T_{DN}, but not T_{DO}, because no reverse current can flow in D_{S1}). On the other hand, if any input is 1 ($+V_F$), I_F flows in D_1, D_{S1} and not in D_{S2}; therefore, the set

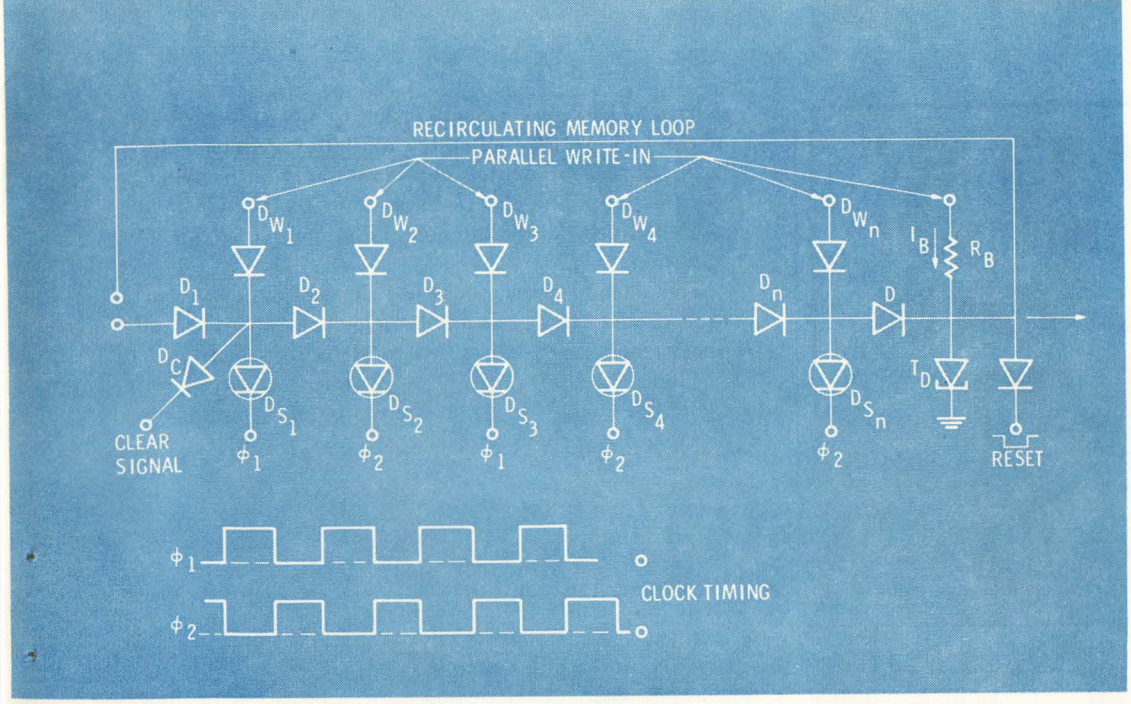

Fig. 2 Charge transformer shift register or serial memory

Illustrating the practicability of 250 megacycle circuits using the tunnel diode charge transformer, this article pinpoints difficult design areas and outlines the problems in clock generation and distribution for nanosecond circuits.

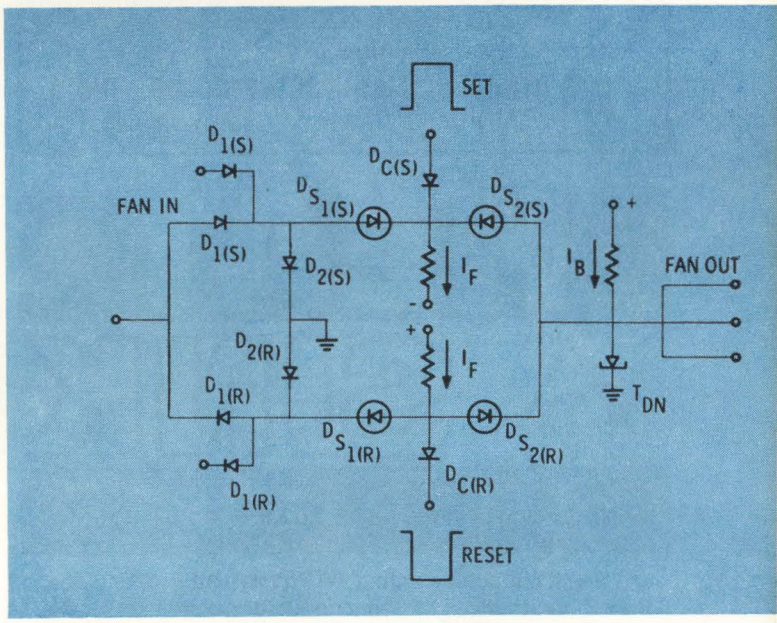

Fig. 3 NRZ "NOR" Circuit

clock drives reverse current through D_{S1} and D_2, setting T_{DO} to the high state. This fact says that the output of T_{DO} is the same as the input, and that the output of T_{DO} is the inverse of T_{DO} at the same time. Each stage is reset by applying a negative pulse to D_{RN} and D_{RO} that is 180 degrees out of phase to the set pulse; this arrangement gives an output wave form for the 1 output of a 1-to-1 duty ratio. To ensure correct propagation, a 2-phase clock system is used in which Phase 2 is 180 degrees out of phase with Phase 1.

To complete the logical possibilities, a level of diode AND logic is included by using backward diode D_A as a current steering level with +DC and R_A.

Charge Transformer Shift Register

The circuit in Fig. 2 is very useful to this module family because of its simplicity and low cost. D_1, D_{W1} and D_{S1} replace a complete flip-flop in other forms of recirculating shift registers. The object is to transfer the charge (or no charge) in the Phase 1 storage diodes to the Phase 2, on the application of the Phase 1 clock. Then, the Phase 2 clock transfers the storage in the Phase 2 storage diodes to the Phase 1 diodes. The coupling diodes D_1, D_2 . . . D_N give directionality of information flow. The loop from T_{D1} to D_1 can be closed for recirculation or left open for single-shot shift functions. Parallel write-in is obtained by injecting charge at D_{W1}, D_{W2} . . . D_{Wn}. The register can be cleared by applying a dc level at the input to D_C.

NRZ Logic (250 Megabit)

As in all multiphase systems, the information rate of the circuits in Fig. 2 is given by the clock rate which is 125 megacycles. However, the information rate can be made 250 megacycles by the parallel operation of

two branches of logic. In order to get into and out of the logic serially, circuitry must be available which has a 250-megabit rate. The circuit in Fig. 3 achieves this by controlling the reset clock in the same manner as the set clock, thereby obtaining nonreturn to zero operation.

The set and reset clocks are applied simultaneously to $D_{C(S)}$ and $D_{C(R)}$ at a 250-megacycle rate. The same phase clock signal is applied to all NRZ stages. When the input is 1 $(+V_P)$, $D_{S2(R)}$ stores a charge from $I_{F(R)}$ but $D_{S2(S)}$ does not; therefore, on the application of V_S and V_R, the reset clock is routed through to T_{DN}

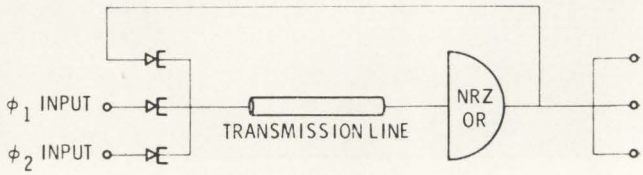

Fig. 4 Serial Transmission Line Storage

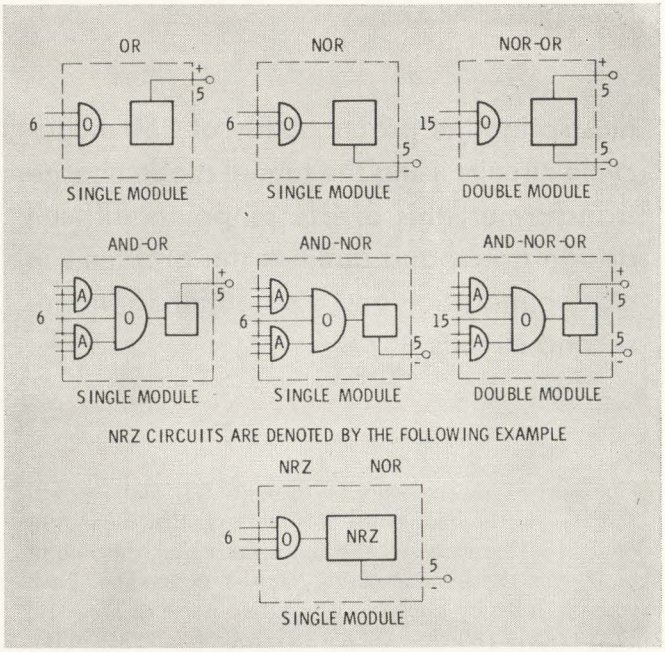

Fig. 5 Logic Functions and their Symbols

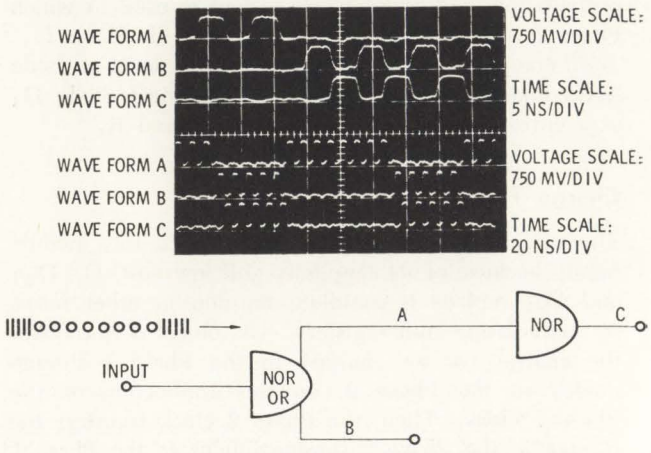

Fig. 6 Wave Forms of "NOR" "OR" Logic at 250 MC

TABLE 1

Dynamic Operating Range Test on NOR-OR Circuit

Circuit	Min. Bias Level (ma)	Max. Bias Level (ma)	I_p (ma)	Fan-Out
NOR	11.4	19	22	50 Ω resistive load
NOR	10.2	17	22	470 Ω resistive load
NOR	12.0	17	22	3 loads single wire coupling
NOR	15.0	19.5	22	6 loads single wire coupling
NOR	16.0	20.3	22	7 loads single wire coupling
OR	13.1	18.2	22	50 Ω resistive load

resetting or maintaining T_{DN} in the low state (0). Conversely, if the input had been 0, $D_{S2}(_S)$ would have stored, enabling the set clock to be routed through to T_{DN}, thus setting T_{DN} to the high state 1. Since the clock arrives at a 250-megacycle rate, the information can change every 4 nanoseconds with an output which is of NRZ form.

By connecting both phases of the circuits previously described (Fig. 2) to the output, the Phase 1 information is selected by the Phase 1 circuit and the Phase 2 information by the Phase 2 circuit, thereby enabling two logic networks to operate in parallel at a bit rate of 250 megacycles. In order to obtain the output of the two parallel paths in a serial 250-megabit form, a summing output is used as described below. It can be clearly seen that the NRZ operation described here can be extended to the NOR, OR circuit (Fig. 1) giving NRZ NOR, OR logic.

Serial Memory

The use of transmission lines to provide serial storage has proven to be a practical and economical means of obtaining nanosecond memory capabilities (Ref. 11). The circuit shown in Fig. 4 enables the information to be stored at the phase rate by using an NRZ OR circuit as a recirculating amplifier.

The backward diodes B_{D1}, B_{D2} and B_{D3} form an isolating sum input for the Phase 1 and Phase 2 drivers and the feedback recirculating information. This configuration enables the outputs of two logical paths in parallel to be read out from the NRZ OR circuit in serial form at a 250-megabit rate.

Logical Capability

The logical possibilities with this complete module family are numerous, particularly when combined with passive delay elements which are no more than lengths of transmission line. These delay elements are either fabricated from printed circuit strip line or miniature coaxial cable.

A fan-in of 6 and fan-out of 5 have been selected as the standard interconnection arrangement. This condition was not limited by circuit performance but by a compromise between maximum fan-in/fan-out, the optimum size of a module and the number of interconnection pins available on the interconnection surface. The current gain per stage at 250 megacycles is on the order of 14, which allows for wide margins on component and parameter tolerances. Typical performance figures allowed for in the worst case design were ±25% clock voltage, ±5% peak current, and ±5% constant current supplies.

The logic function and its symbol are given in Fig. 5 with the fan-in/fan-out interconnection capability.

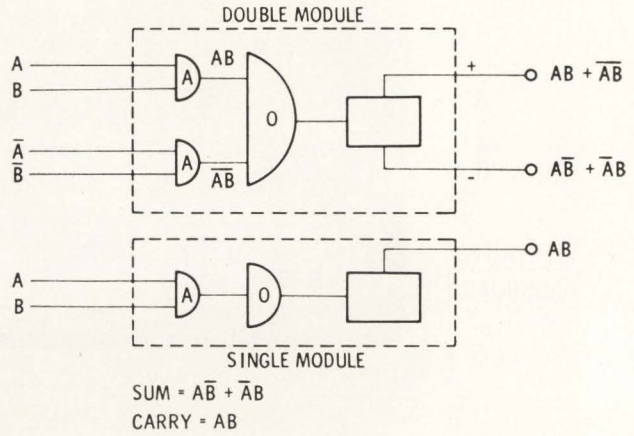

Fig. 7 Logic Diagram of a Half Adder with Sum and Complement Output

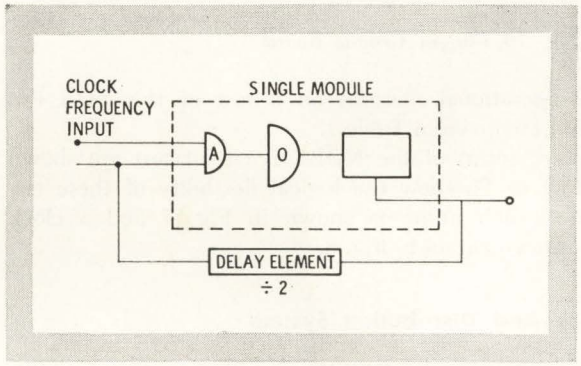

Fig. 8 Logic Diagram for a Frequency Divider

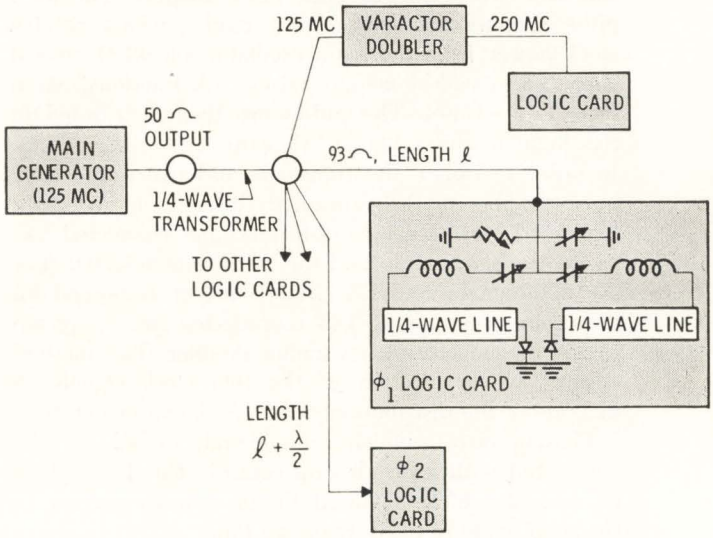

Fig. 9 Clock Generator and Distribution System

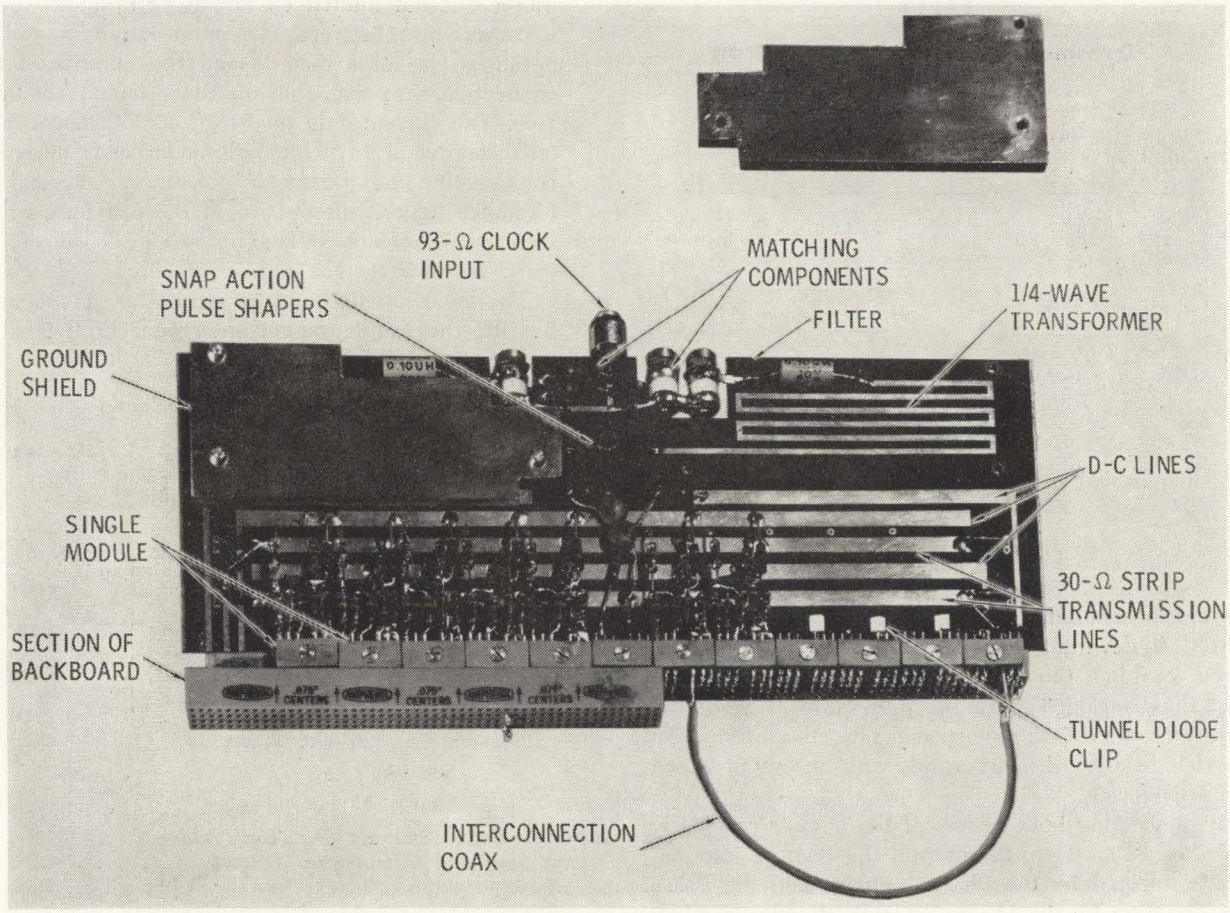

Fig. 10 Plug-in Circuit Board

The operational margins on a test of the NOR OR circuit are given in Table 1.

Wave forms of the NOR-OR circuit test are shown in Fig. 6. To show the logical flexibility of these circuits, a half adder is shown in Fig. 7 and a clock countdown circuit in Fig. 8.

Clock And Distribution System

The clock generator consists of a main oscillator amplifier at a frequency of 125 megacycles, which supplies sufficient power for 10 local pulse shapers. The local pulse shapers are snap action diodes which receive clock power from the main oscillator via 93 Ω coaxial cable, and locally generate pulses with fractional nanosecond rise times. The pulses are then distributed to the logic modules via 30 Ω strip transmission lines. In order to isolate the transients and match the local pulse shapers to the sinusoidal distribution system, a filter and impedance transformer are connected between the snap diode and the 93 Ω source signal. For the 250-megacycle NRZ circuits, power is tapped off the main generator at 125 megacycles and converted to 250 megacycles by a varactor doubler. This method ensures synchronization of the two clock signals. A diagram of the distribution system is shown in Fig. 9.

Phasing errors, which are generally small, can be eliminated with a dc phasing control. This is simply a dc current which is added to the storage current in the snap diode to delay the snap time.

Each logic card is matched at the input to a real impedance of 93 Ω, thereby minimizing the VSWR on the distribution cables. In general, a VSWR of less than 1.1 is achievable; this is well within the tolerance requirements placed on the clock voltage.

Packaging And Interconnections

Because of the large values of di/dt required suitably to drive the tunnel diode, it is necessary to place all components in the path from clock voltage to tunnel diode close to a ground plane with a minimum lead length from clock transmission line to tunnel diode ground. For this reason, a mothercard (7 x 3 inches) has been designed which houses the snap diode pulse generator and strip distribution lines, thereby enabling the logic modules to be attached with a minimum lead inductance. A photograph of one of the cards is shown in Fig. 10.

A single module size is 0.55 by 0.2 by 1 inch and is attached to the main board by one fixing screw and approximately four soldered leads. For those circuits requiring two modules, a double-header module is designed which is 1.1 by 0.2 by 1 inches. All the circuit configurations previously discussed can be fitted into one of these two module sizes. The tunnel diode is grounded to the main board and contacts the spring clip on the module to close the circuit when the module is fixed into place.

The module header is made from two layers of an Amphenol strip connector which provides a total of 12 pins on the interconnection surface. These pins are

for 6 inputs, 5 outputs, and one monitoring point. Below the module header are two more layers of strip connectors, with pins attached permanently to the ground plane. This arrangement provides an additional 12 pins for ground connection to each module with a total interconnection surface of 0.55 by 0.4 inch.

The card with modules attached is plugged into a tray or backboard which consists of a layer of socket-type strip connectors. The backboard size is 8 by 7 inches, and the cards are placed side by side enabling 20 cards to be placed in one tray. Interconnections are made on the backboard by crimping the socket pins to the center and outer conductors of miniature 120 Ω coaxial cables, and inserting into the strip layer. The maximum lead length between circuits is restricted to 8 inches by the propagation time of the signal along the coupling transmission line; however, no timing errors are accumulated because each stage is retimed by the clock pulse. The insensitivity of these circuits to noise (due to the integration of charge by the storage diode) has enabled many interconnections of under 2 inches to be made with open wire.

Each module consumes approximately 100 mw of clock power and 100 mw of dc power, which gives a total power per motherboard of 1 watt clock and 1 watt dc.

This family of logic modules, capable of reliable operation at 250-megacycle information rate, is available to the system designer in a variety of logical configurations. The increased gain bandwidth of TDCT logic has enabled the performance described to be achieved without resorting to special packaging techniques and tight tolerances. The modules are designed using standard commercially available hardware, and are removable—enabling them to be repaired. END

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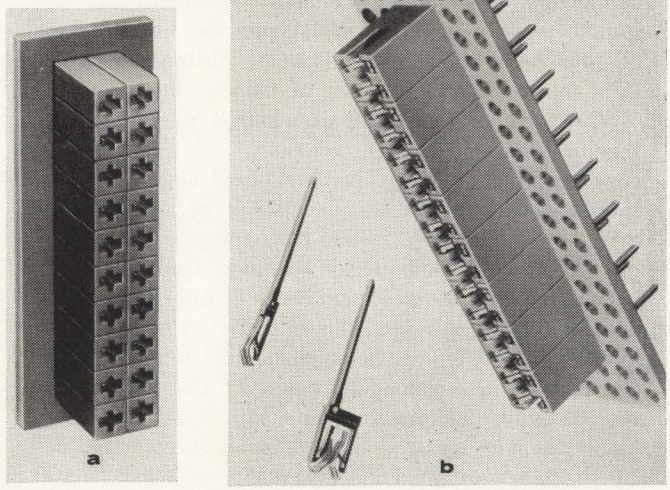


Fig. 1 One of Elco's newer connector systems, tradenamed Variplate, is built around the use of a soft aluminum base plate, usually H1100, in which standard size holes are drilled and punched. (a) The standard plates are 1/8" thick and are available in sizes over 2 feet by 2 feet. The holes are on 0.200" centers and are held to within ±0.005" accuracy. Plastic insulators are pressed into the holes and contacts are held within the insulators. (b) Miniature Variplates are also available; the plates are somewhat thinner and hole centers are usually 0.100" or 0.125" on centers. Shown here is a miniature Variplate printed-circuit-card edge connector.

Advances in Connector Technology ➤

S. V. WORTH, *Chief Engineer, Elco Corp., Willow Grove, Pa.*

EDITOR'S NOTE: As part of a continuing series of CD editorial reports on new circuit connectors and interconnection systems, this article describes one company's design approaches to connector reliability in digital equipment.

For the most part, a connector may be simply defined as a component containing metal contacts for attaching to circuit lines, one to the other, and usually allowing for disconnection of the circuit lines. A thorough knowledge of connectors and their use clearly indicates the many reasons for their extensive incorporation into electronic equipment:

- Sub-units can be built to be incorporated into the entire electronic network at a later date
- With intelligent design of sub-units, manufacturing economies can be achieved as the number of units is increased, or sub-units are isolated so as to permit more automatic or more simple assembly
- In many instances, a network is physically possible only by first breaking it down into sub-units
- Permanent connections of sub-units introduce the very real probability of disturbing adjacent components; conversely, the use of connectors minimizes the possible damage to components
- Connectors permit less skillful personnel to accomplish trouble-shooting and adjustment of equipment by isolating sub-units
- A very obvious factor, one which becomes more and more important as the profit margin narrows, relates to the reduction of replacement time of defective components as allowed by the use of connectors
- Wiring errors are drastically reduced as connectors are used, resulting in an immediate saving, as well as an indirect saving, since less skillful operators can be used
- Connectors greatly reduce the number of poor or questionable repair connections.

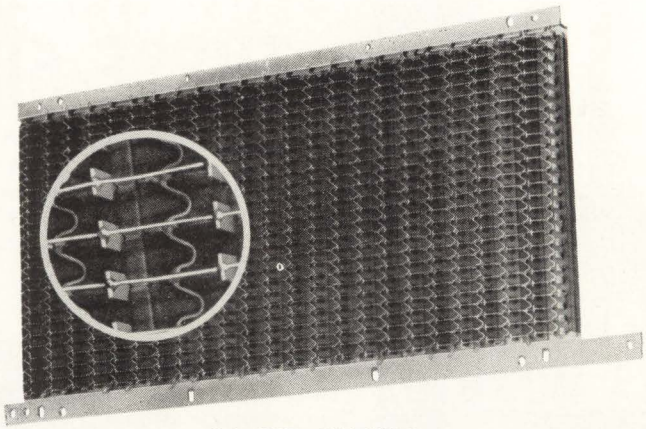
It is quite obvious that connectors play a most important part in the proper design, functioning, maintenance, and repair of computers and data processing equipment. Three broad areas define and describe the connector and its applications in today's equipment: versatility of the connector itself and versatility of its contacts; reliability; and non-degradation of properties as the connector or its contacts are miniaturized.

Versatility

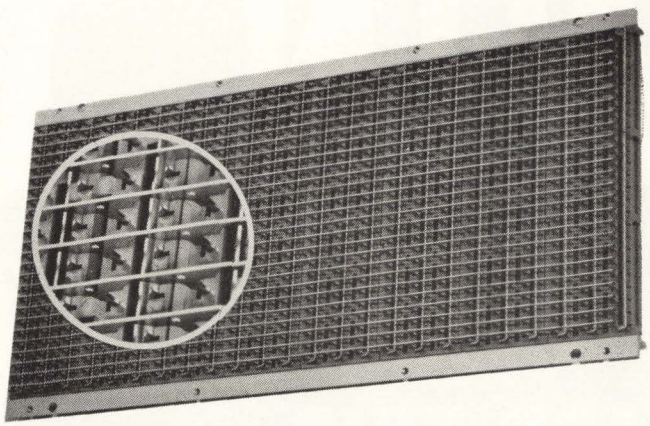
To serve a rapidly-changing technology, a connector must have sufficient flexibility in its design to meet demands imposed upon it with a minimum of redesign, and with a minimum of variations. In recent years, Elco Corp. has developed a variety of distinct connectors and systems which allow for wide versatility in computer design. Some of the major ones are shown and briefly described in Figs. 1-8.

Reliability

In the past, an electronic system might have used a dozen connectors; but today hundreds or even thou-



(a) OLD METHOD



(b) NEW METHOD

Fig. 2 Bus Strip Wiring. A truly significant advancement in interconnections was made with the development of contacts on busses. Essentially, the use of bus contacts eliminates the need for individual connections used in the old method of bus strip wiring shown in (a). Elco's award-winning, new method of bus strip wiring (b) assures positive, 100% contact. Triple nose and feed through, or double nose contacts are also available which are, in essence, miniature busses.

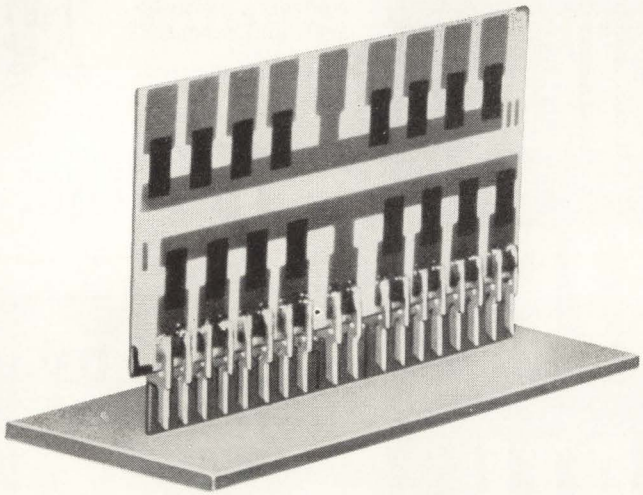


Fig. 3 Contacts for Substrates. To meet the demands of the more recent developments in substrates and thin-film circuitry, Elco developed "fork tail" contacts. They press-fit onto the substrate making a fine connection; however, they should be soldered for additional security. Extremely close centers can be obtained — 0.050" or less.

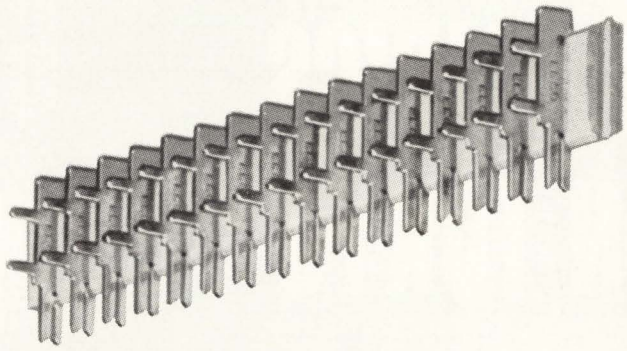


Fig. 4 Board-to-Board Contacts. Outstanding contact versatility of these contacts is evidenced by their direct use in printed circuit boards. The contacts are supplied in loose form, or on standard centers imbedded in a plastic strip as shown here. The contact legs are then inserted into pre-drilled, or punched holes, where they are then readily staked in place. If desired, the plastic strip can be removed.

sands are common numbers. Furthermore, as systems become more complex and non-breakdown features become of greater importance, reliability requirements increase at a faster and faster rate. Today, we must talk of a million non-failing connector hours to obtain good computer performance; it is not uncommon to achieve results ten times this figure.

Connectors, as components, have fared very well in reliability compared with other electronic components. Studies by the Autonetics Division of North American Aviation in a model of an average electronic system, indicated that the failure rate, based upon one million operating hours, was only 2.2 percent. In other words, if all the connectors in the system were removed, the Mean-Time-To-Failure would be reduced from 277.3 to 271.2 hours or 2.2 percent – a small percentage of total failure rate. Studies by IBM Corp. and Collins Radio Co. have agreed closely with these figures.

Additional studies have pointed to some of the reasons for connector failures and have indicated means for increasing their reliability. Thus, it was shown that 20 percent of failures are caused by electrolytic corrosion, which is the result of moisture. This indicates a need for a more gas tight contact.

The major cause (approx. 50%) for connector failure is mishandling. Some common problems are loosened pins or contacts, breakage of insulators, bending contacts, careless mating of connectors, deforming pro-

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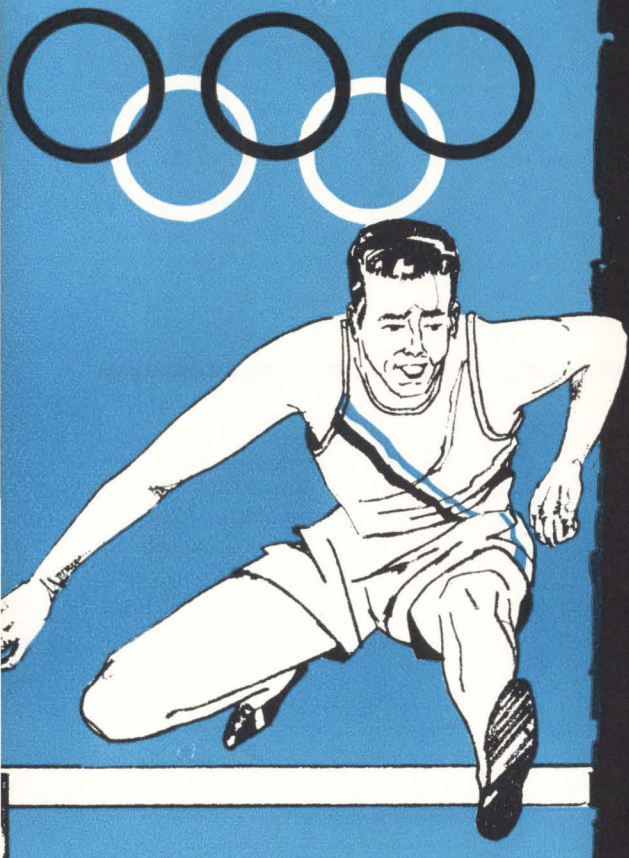

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1. This competition, where not prohibited by local or state law, is open to anyone who resides within the United States of America except employees, representatives, or agents of Motorola Inc., and its related companies and members of their families.

2. Entries must be based upon a circuit design using standard Motorola PNP and NPN silicon annular transistors. Circuits using both PNP and NPN devices in combination (not exceeding 10 transistors) will be considered of higher merit.

3. Each entry submitted must include:
A. Schematic drawing of circuit
B. Brief description of purpose and function of circuit
C. The unique features of the circuit
D. A signed entry blank

4. Merit of design will be weighed with respect to circuit efficiency, performance, size and weight reduction, and the reduction of component count made possible by the design. Consideration will also be given to how the circuit utilizes the low leakage, linearity, and broad gain range characteristics of Motorola annular transistors.

5. Judging will also take into account problems solved with respect to temperature or power supply variations, and elimination of excessively tight component tolerance requirements. Above all, simplicity and economy of design is preferred.

6. Circuit design entries may be in all areas of application — digital, amplifier, power supply, instrumentation, timing circuits, etc.

7. Joint entries are acceptable under the contest rules, however, prize awards will be shared jointly by such entries. There will be no limitation on the number of entries any contestant may submit.

8. Awards will also be judged on the following points:
A. Directness of the circuit design.
Example: The utilization of a minimum number or best combination of components to perform a circuit function.
B. The originality of the circuit design — the newness of the circuit approach.
C. Technical feasibility — the ease with which the entry can be reduced to practice.

9. Screening will be performed by Motorola's Applications Engineering Department. Final judging will be performed by leading electronic authorities outside Motorola. The decision of the judges will be final.

10. Winners will be notified by mail prior to September 1, 1964. A list of winners may be obtained by sending a stamped, self-addressed envelope to Motorola Semiconductor Products Inc., Box 955, Phoenix, Arizona 85001.

11. All entries must be postmarked no later than July 15, 1964, and in Motorola's hands by July 19. Entries should be mailed to Motorola Semiconductor Products Inc., Silicon Circuit Contest, Box 955, Phoenix, Arizona 85001.

The receipt of a circuit from a contestant does not create or imply a confidential relation between the contestant and Motorola Inc. or any of the judges of the contest. The contestant shall retain all patent rights in circuit he submits in this contest, but waives all other rights such as those relating to publication of the circuits. Company clearances required for the submission of proprietary circuits submitted by any contestant shall be the responsibility of the contestant.

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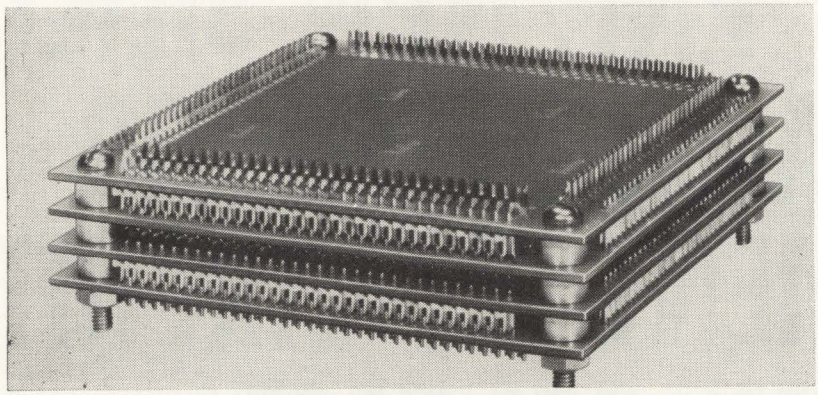


Fig. 5 Memory Plane Contacts. Centers as low as 0.100" are common for these contacts used in memory plane applications as shown in this memory stack example. Another application is in the module packaging, wherein the module can be plugged into its mother board by use of board-to-board contacts.

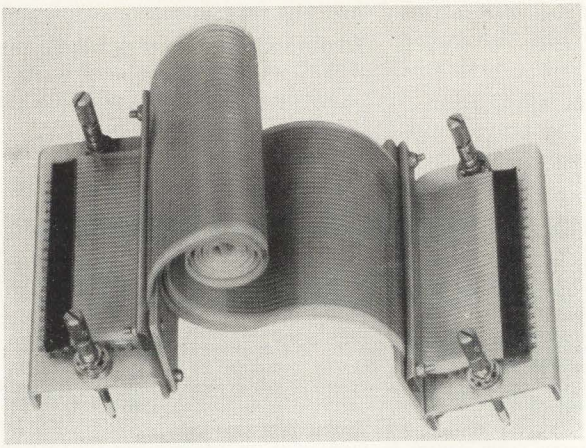


Fig. 6 Logic Drawer Tape Cable Connections. An advanced approach to the connection of computer logic drawers involves the use of flexible cable. It involves the use of coiled, multiple cables, with a connector attached to each end. The coil effect of the wound cables retract the drawers which can be exposed for service or test, with "power on." As many as four cables have been successfully coiled into one unit. Tests have indicated this solution to be positive, safe and remarkably free from maintenance.

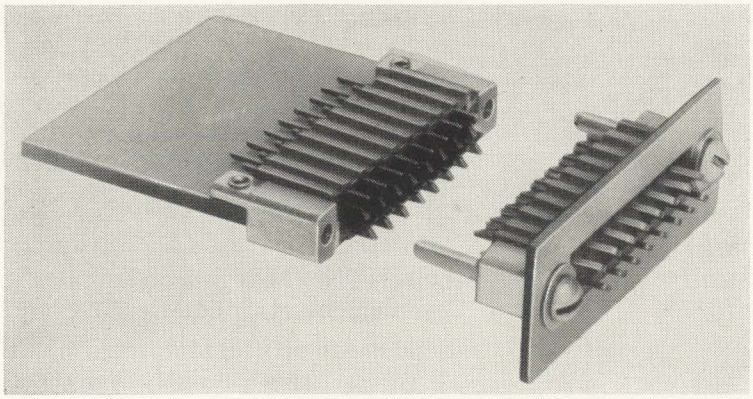


Fig. 7 Stacking Connectors in Strips. Recent break-throughs in microminiaturization were made not only by reduction of connector size, but also by development of strips of connectors, which can be staked in multiple rows of contacts. An example of this approach is the "Zig-Zag" connector, shown here. It contains two rows of contacts, 0.100" apart and on 0.100" centers. The rows are offset 0.050". Each connector strip is available in 2 to 96 contact lengths. One of the main features of the connector allows one row to be interlaced with another, permitting a build up of a multitude of rows.

jecting connectors, snagging or stepping on cable emanating from connectors. Therefore, the human factor becomes quite important. It is also interesting to note that the above factors do not relate to printed circuit connectors. PC connectors do not have projecting contacts and should be even more reliable.

Proper plating plays a most important part in the reliability of contacts. Tests have shown that the force between contact surfaces and electrical resistance is linear and inversely proportional. It is also true that resistance decreases as the true contact area increases. (This area can be increased by adoption of plating that has much more plasticity or low yield pressure.) Futhermore, minimum resistance is assured with the use of a non-oxidizing metal. Thus, a relatively soft, noble, metal is indicated for plating on contacts having relatively high contact pressures. Conversely, lower pressures reduce wear, and provide ease of operation.

The ideal contact surface has the following properties:

- Sufficient plating to minimize diffusion of base metal
- High electrical conductance
- Low coefficient of friction
- Relatively soft plating
- Tarnish and corrosion-free surface
- Maximum flexibility

An ideal contact combination is almost pure gold on a base of a good, flexible nickel plate. The gold is deposited in thickness, usually from 5 to 100 millionths, with the lower figure used in industrial applications, and the higher figure used in Military applications.

Non-Degradation of Properties

Unfortunately, many designers and manufacturers have taken for granted the statement, that "as a product is miniaturized, its cost is increased as a result of the increased difficulty of production, and its properties are degraded". This is certainly not true of properly-designed contacts. Table I clearly proves the point. As illustrated in Table I, a standard Elco VARICON connector is 0.004 square

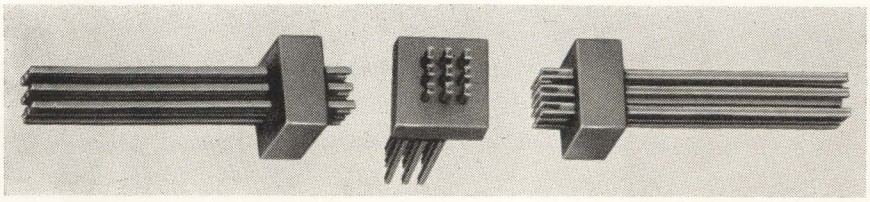
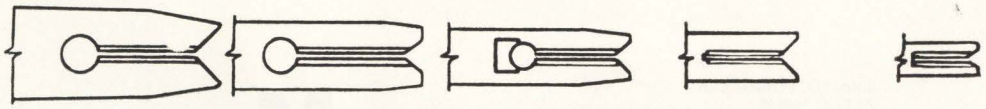


Fig. 8 A new miniaturized connector is the BI/CON Connector. Contacts are on 0.050" centers but rows can be offset 0.025" centers. The BI/CON contact is of true hermaphroditic design. Its four mating surfaces are 0.100" long but one half of this length is rigidized with a web, so that this contact has outstanding strength and electrical properties.

TABLE 1

	STANDARD	MINIATURE	SUBMINIATURE	MICROCON	BI/CON
					
MAXIMUM WIDTH	.154"	Type 1 .115" Type 2 .126" Type 3 .126"	.093"	.082"	.035"
LENGTH OF COINED AREA (Approx.)	.185"	Type 1 .185" Type 2 .135" Type 3 .135"	.125"	.125"	.088"
WIDTH OF COINED AREA (.008" SLOT)	.0125"	Type 1 .0125" Type 2 .0102" Type 3 .011"	.0075"	.009"	.009"
MATERIAL THICKNESS	.026"	Type 1 .026" Type 2 .0225" Type 3 .024"	.016"-.018"	.020"	.020"
TOTAL CONTACT AREA, SQ. IN. (Approx.)	.00925"	Type 1 .00925 Type 2 .00551 Type 3 .00594	.00375"	.00450"	.00317"
CROSSECTION AREA	.00400"	Type 1 .00299 Type 2 .00277 Type 3 .00302	.00167	.00164	.00070"
CURRENT RATING	10 AMPS	10 AMPS	3 AMPS	7 AMPS	3.5 AMPS
CONTACT RESISTANCE	.005 OHM MAX	.005 OHM MAX	.005 OHM MAX	.005 OHM MAX	.0035 OHM MAX
WITHDRAWAL FORCE	> 4.0 but <16.0 oz.	> 4.0 but <16.0 oz.	> 4.0 but <16.0 oz.	> 4.0 but <16.0 oz.	> 4.0 but <16.0 oz.
CLOSEST POSSIBLE CENTERS	.200"	Type 1 .125" Type 2 .150" Type 3 .150"	.100"	.075"	.050"
COST PER CONTACT	$30.00/M	Type 1 $30.00/M Type 2 $30.00/M* Type 3 $30.00/M*	$30.00/M	$30.00/M	$30.00/M

*Quantities under 25,000

inches in cross sectional area, as opposed to its minute counter part, the new BI/CON connector which is 0.0007 square inches in cross sectional area — a reduction factor of about 6 to 1. However, the contact areas are reduced only 3 to 1; the current carrying capacity less than 3 to 1; while the resistance, and withdrawal force remain virtually the same. These particular contacts also use the very same manufacturing techniques and standards to assure maximum reliability at a minimum cost.

In conclusion, it is clear that the connector manufacturer has been rapidly expanding his products to meet the imposed demands of the industry. It is evident, too, that a connector is a highly reliable component, particularly when properly applied, and correctly used.

Circle No. 110 on Inquiry Card

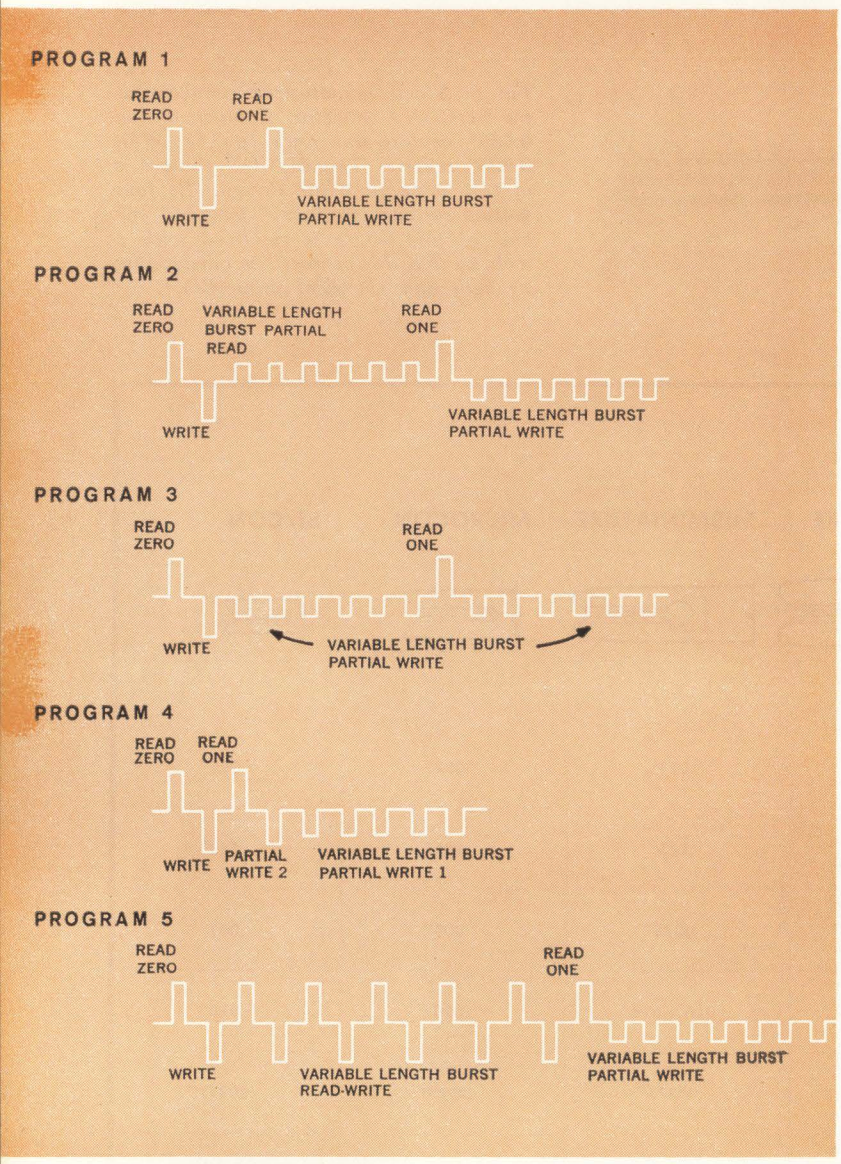


Fig. 1 Any one of five fixed pulse programs may be selected with Digital Equipment Corp.'s Type 2113 Automatic Memory Core Tester. Each program utilizes a specific ordering of pulse types and although this ordering is fixed within each program, all other program parameters such as pulse width, rise and fall times, amplitude, and repetition frequency are completely adjustable. Core amplitude is measured by two highly stable linear calibrated sense amplifiers which have a gain of 10, bandwidth of 20 megacycles, and a common mode noise rejection ratio of 100:1. One amplifier measures the ONE output signals from the core and the other measures the ZERO. If desired, a single amplifier can measure both the ONE and ZERO outputs. The sense amplifier outputs are compared with eight precisely regulated adjustable reference levels. The result of this comparison is sampled at up to five specific sample times during the read ZERO and read ONE test core-output pulses.

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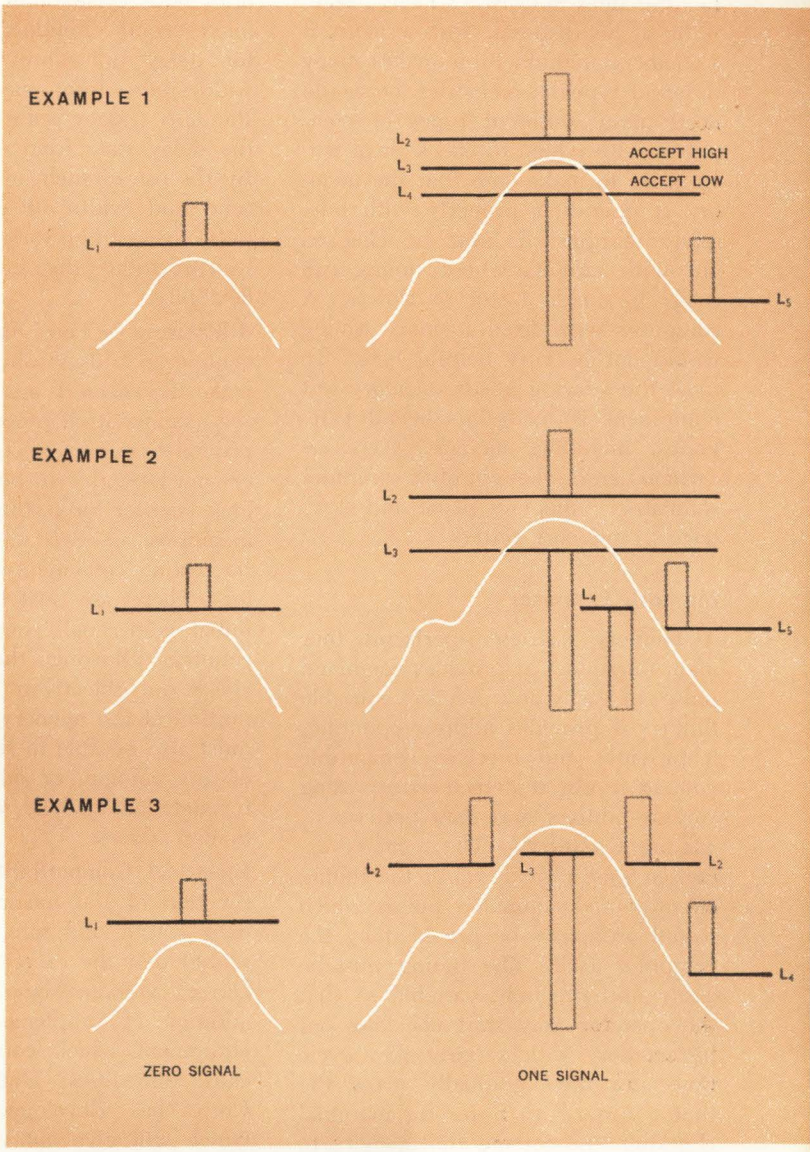
Memory Test Equipment

Many of the failures of present-day digital computers originate in the memory system. Magnetic core memories are probably the most reliable type of rapid storage memory yet invented for computers. Theoretically, such a memory should have infinite life, since the cores do not wear out. Nevertheless, one of the most time consuming and difficult tasks involved in the checkout of a new computer is the checkout of the memory system, and although the failure rate of memories is becoming smaller and smaller, it is still high enough to cause considerable concern to reliability engineers.

The reason for this difficulty, of course, is that the memory is essentially an analog device. It is a fairly simple matter to build sufficient design margins into AND and OR gates, flip-flops, pulse amplifiers, etc., so that short of a catastrophic failure, they will always work. Core memories, however, give out a relatively small output which must be sampled at a particular time and then amplified to the digital signal level. Cores not only produce an output when they are fully switched, the uV_1, but they also give an output when they are only partially switched, the dV_Z. Consequently, there is always the problem of a finite signal-to-noise ratio. Furthermore, as the computer manufacturers try to manufacture faster and faster computers, the memories must have faster and faster cycle times. This inherently means cores of

Tests and check-out operations on magnetic core memories have to be carried out by both the memory manufacturer and the user. The major performance characteristics and design criteria of memory exercisers, plane and stack testers, and core testers are discussed here.



NOTE: VERTICAL BARS INDICATE STROBE TIMES. BARS APPEAR ON REJECT SIDES OF SLICE LEVELS.

Fig. 2 Examples of accept-reject criteria used in DEC's Automatic Core tester. Core amplitude is subjected to a maximum of eight accept-reject decisions. Eight slicers compare the output of sense amplifiers with eight independently variable calibrated reference levels. This information is strobed into the flip-flop part of the circuit by 70 milli-microsecond pulses at five specified times to determine whether the output pulse signal is greater or less than the calibrated level. Each strobe pulse can be used either during the READ ONE time or the READ ZERO time. Vertical bars in the examples indicate strobe times. The bars appear on reject sides of slice levels. The information on the eight flip-flops is then subject to the accept-reject decisions based upon pre-determined specification.

a smaller and smaller physical size, relatively lower output, and more critical timing. Consequently, the memory manufacturer is faced with greater and greater difficulties when he must deliver a reliable system.

Digital Equipment Corp. has attacked many facets of memory testing problems and has designed several types of testing systems which are of help both to the memory manufacturer, who must test out his product before he sells it, and also to the computer manufacturer, who must provide an incoming inspection test to the memory before he accepts it and puts it into his computer.

More exactly, the memory manufacturer needs to control the quality of his product by testing the performance of its component parts as well as overall performance, while the memory user will want to ascertain that the memory meets the requirements that will insure that his computing system performs according to specifications. If the memory manufacturer is producing a large number of memories of few types, he will need several testers of relatively simple design, and they probably will be operated by junior test engineers. On the other hand, the research company working on memories of advanced design will require equipment of great sophistication and flexibility, operated by senior design engineers.

Of course, a memory system could be completely checked out by insertion into a computer, but the manu-

facturer does not always have a computer at his disposal. Furthermore, if a memory manufacturer makes many different types of memories, he would need many different types of computers with which to check them out. In order to make sure that the memory is operating properly with adequate margins, it must be checked out with circuits whose timing can easily be made faster or slower. A computer with fixed memory timing would not be very helpful here. To meet the varying needs, memory test equipment is made in several categories, including memory exercisers (which can be thought of as computer simulators), memory plane and stack testers, and core testers.

Memory Exerciser

A memory exerciser performs four main functions: it provides command pulses of easily and precisely variable timing; it provides address counting; it provides and receives compatible voltage levels; it detects errors using various address and data patterns.

Timing Circuitry — The memory exerciser must provide all of the timing circuitry and command pulses which would ordinarily be provided by the computer itself. This timing must be easily and precisely variable so that the operator may start checking out his memory with a fairly slow cycle time and then gradually make the timing faster and faster for marginal checking. By forcing the memory to operate at a somewhat faster cycle time than it will operate in the computer itself, the memory manufacturer is assured that there are adequate timing margins in all of the circuitry. Furthermore, by being able to vary the timing of each command pulse independently, the operator is able to discover the optimum timing for each command pulse. This optimum timing may, indeed, be slightly different from that which he calculated when he designed the memory. The memory exerciser becomes not only a checking device but an aid in design.

Along with providing variable timing, the memory exerciser should provide timing and counting circuits faster than normal cycle time for marginal checking purposes, as well as for testing out even faster memories still in the design stage. Digital Equipment Corp., for instance, is able to provide timing and addressing circuitry adequate for testing out memories with cycle times as low as 0.6 microsecond. Single-shot multivibrator delay units provide a variable width pulse from one output and a standard trigger pulse at the end of the delay time from another output. By the use of such units, the starting time and width of each command pulse then can be varied independently, providing the greatest possible flexibility.

Addressing — The exerciser must contain an address counter which will make the memory address register in the memory itself proceed in a logical fashion from core to core. The counters must be able to be set up as one long counter for testing word-address memories, or two separate counters for testing coincident-current memories. There are switches for setting initial and final conditions of the counter, allowing the operator to check out selectively any particular portion of the memory. The operator must also be able to stop on any line or any column, or on any one core for detailed analysis work of a particular address.

Electrical Compatibility — The third function of the memory exerciser is data output and interface. It is essential that the exerciser provide the correct voltage signals without the addition of supplementary interface equipment which could conceivably cause difficulties. Digital Equipment Corp. has developed bus drivers which will give out variable voltage levels ranging from 2 to 6.5 volts either positive or negative. The memory exerciser must also be able to accept different voltage levels back from the memory under test. Different memory systems require different write-read patterns, including the normal double checkerboard patterns as well as more complicated ones. Flexibility in the selection of both address and data patterns is especially necessary when the exerciser is to be used for checking out new types of memories in which the worst-case patterns are not yet known.

Error Detection — Since the information which is being read out from the memory is already in digital form, the exerciser has merely to differentiate between two voltage levels and compare this data with the data which it had previously written into that address. The memory exerciser checks all bits of the memory in parallel, address by address. Indicator lights, showing the individual address and bit position, display the error location if the exerciser is programmed to stop an error.

Memory Testers

The heart of a memory system is the memory stack, consisting of a number of either word-organized or coincident-current memory planes. The problems involved in testing memory planes and stacks are considerably different from those presented by complete memory systems. Since memory stacks are produced in larger quantities than memory systems, the memory plane and stack tester becomes more of a production device. It is operated by test technicians or by junior engineers. The memory tester is no longer concerned merely with whether the output is a ONE or a ZERO; it must make precise measurements of core output amplitude. Consequently, the criteria for memory tester design are accuracy, stability, ease of operation, and flexibility.

The memory plane tester is also beginning to be used as a design tool. A new more complicated and more flexible type of tester has been designed which can be programmed to provide almost any conceivable type of pattern for each core. It can be programmed to select particular cores in a plane in many different modes of operation. Thus, the memory plane designer can use this machine to discover valuable information concerning the response of various core and winding configurations to many different driving conditions.

To assure reliability of a memory stack, it should be tested under conditions as close as possible to that which the stack will encounter when used in the computer memory. Core driving scheme, rise and fall time, pulse width, and amplitude of the driving pulses must approximate as closely as possible computer conditions. These requirements call for a memory tester of the following basic parts: addressing and decoding scheme by which the current drive pulses can be routed to the proper X, Y, and Z lines; current generators; sensing system and sense switches; and error detection circuitry.

Addressing — The equipment for addressing is extremely simple. It allows the operator to check any particular portion of his memory stack.

Switches allow the operator to scan along any one X line, Y line, or Z line, or any combination of X, Y, and Z. Thus, any particular line, column, plane, or single core can be checked out individually. To observe the dV_1 output of a given core, the operator syncs a viewing oscilloscope on that core while scanning the entire memory plane. The current driver pulses are switched from line to line by solid state switches using silicon control rectifiers. It is not necessary for a memory tester to proceed at the same cycle time as the computer as long as the shape of the drive pulses are similar to those in the computer. The pulse repetition frequency of Digital Equipment Corp.'s memory tester is approximately 20 kc. It is important that the rise time of the pulses be maintained through the switches. SCR's are an excellent component to use in this position because they can carry a large pulse current (1 ampere) at relatively high back voltages ($\pm$50 volts) without causing any deterioration of wave shape. Two SCR's are used back to back in each switch so as to be able to pass both positive and negative pulses. Capacitance to ground is isolated by high frequency diodes in series with the SCR.

Current Generators — The most difficult problem in developing a satisfactory memory tester is to develop current drivers that are fast, versatile, and amplitude stable in time. They must have a range of rise and fall times which will test anything from slow cores, requiring almost a microsecond rise time, up to the fastest memory cores made today, which require rise times better than 0.1 microsecond. Current amplitudes must be easily variable over a wide range, for example, from 10 milliamps to an ampere, and yet must remain absolutely stable after they have been set. Magnetic cores act as an amplifier. A 1 per cent change in drive current causes approximately a 3 per cent change in core output voltage at the normal driving point. To measure core output amplitude to an accuracy of $\pm$1 per cent, the currents must remain stable to an accuracy of $\pm\frac{1}{3}$ per cent. This stability is achieved by means of careful line voltage regulation and temperature compensation. In Digital Equipment Corp.'s testers, line voltage is first regulated by a Sola Electric Co.'s constant voltage transformer. Each power supply then

has its own constant voltage transformer built in. The critical voltages for the current drivers are further regulated by means of Zener diodes. Temperature stability is maintained by a careful balance of silicon and germanium diodes. The results of these design considerations are a set of positive and negative drivers with a temperature coefficient of 0.02 per cent per degree C., and an output amplitude stability which varies less than 0.1 per cent when the line voltage is changed ±15 per cent of nominal. The drivers are designed as current sources so that the outputs may be easily mixed together on a common bus and so that the output current will change a minimum amount with changes in back voltage. Actual output inpedance of the drivers is greater than 5000 ohms.

In the art of memory testing, one of the most important design considerations is repeatabiilty. Measurements made on a particular core plane at one time on one machine should be able to be repeated at another time on a different machine. It is essential that the rise and fall times of the current drivers be as linear as possible since this is the only type of slope that can be exactly specified. To assure repeatability, there must be an accurate means of setting the current levels at the start of tester operation. In Digital Equipment's testers, a current calibrator, utilizing two mercury relays, switches automatically between current pulse waveform and 2 reference levels, which may be set with an accuracy better than 0.1%.

Sensing — In the design of the sensing system, stability is once again the most important criterion. The core output is first amplified by a differential sense amplifier whose gain of 10 is kept constant by means of negative feedback around each stage. The sense amplifier has a band-width of at least 20 megacycles, more than adequate for testing the fastest cores made today. It is then necessary to compare the output of the sense amplifier with some absolute standard. This is done by means of a slicer flip-flop comparison circuit which compares the output of the sense amplifier with fixed reference levels at strobe times which are variable in position and width. The final output is a digital signal which goes from ground to —3 volts if the core pulse output is greater than the reference level at strobe time. Three independent reference levels and three independent strobes are used so that the core output can be measured for both maximum and minimum values at peak time, and also for some other value part way down the curve to measure switching time. Besides stability, design considerations for this part of the system are ease of operation and maintenance of high band-width throughout the sensing system.

Since only one sense amplifier is used in the memory tester, it must be switched from plane to plane when testing a memory stack, or from line to line when testing a word-address plane. This is accomplished by means of transistor switching, using special bilateral transistors with very low collector-to-emitter drop. The transistor switches must be carefully matched so that the drop across all of them will be the same. Otherwise one would obtain a different measurement depending upon which switch is closed. Compared to relay switching, transistor switching offers higher speed, reliability, and longer life.

Error Detection — Here the design criterion is one of flexibility. In marginal checking, the operator will want to continue the tests in spite of errors, yet be warned of the errors by means of a visual signal. In another mode of operation, the machine stops on error so that the actual address of the error can be noted, while the timing and driving circuitry continues to operate so that the output of the bad core can be studied on an oscilloscope. An auto-start mode causes the machine to halt on error and then continue automatically. An automatic printer could be used in this mode of operation to print out the X, Y, and Z addresses of the bad cores.

Core Testers

The expense of replacing a bad core in a memory plane is great enuogh to justify thorough testing of every core before assembly of the plane. Because the number of cores is very large, automatic test equipment is a necessity.

A core tester consists of two separate kinds of equipment: the core handler and the test equipment. The handler feeds cores to a test station, inserts a probe for the test, and sorts the cores into two or three categories, depending on the test mode. The other half of the system consists of electronic circuits which provide the drive program for the core, compare the core output with given reference levels, and make a decision as to whether the core is good or bad.

Unlike the memory tester and memory exerciser, both requiring a fairly skilled operator in order to perform the tests, the automatic core tester is designed to work for long periods of time unattended. Accordingly, there are several types of safeguards that must be built into such a system. It is much cheaper to throw away several good cores than to accept one bad core and then have to remove it from the matrix later on. First of all, each of the test cores is tested four times. The first test is used to put the core in a known state. The next three tests are all identical, and the core must pass all three tests in order to be accepted. If it fails any one of them, it is rejected. The second safe-guard is that before each test core is tested, a standard core is also tested four times. If the standard core is rejected, the test core that is tested immediately afterwards is automatically rejected whether or not it passes the test. This helps to guard against a transient causing a bad core to be accepted by mistake. The operator sets special very tight limits on the ONE output of the standard core. Thus, if any parameter in the core tester varies, such as the drive current or the sense amplifier gain, or there is any temperature change, the standard core will be rejected. After the standard core is rejected eight times in a row, the machine automatically comes to a halt and turns on a red light. Other automatic circuits detect whether or not a core is present in the test position and whether or not the length of the program is properly timed with respect to the testing time available. If any of these conditions is incorrect, the machine automatically comes to a halt with the improper condition indicated by a red light.

The DEC Automatic Core Tester utilizes the same current drivers used in the memory tester. Thus, the same variations in rise and fall times, amplitude control, back voltage, etc. are available. To provide the greatest possible ease for setting up the core tester for various tests, five fixed pulse programs are provided, any one of

which can be selected by means of a rotary switch. The five programs are diagrammed in Fig. 1. The burst length is controlled by a single-shot multivibrator so that it can be varied at will by the operator. Pulse amplitude and pulse width are individually controlled for each driver. The pulse repetition frequency is also variable in order to provide for the many different testing specifications.

The sensing system is similar to that used in the memory tester except that the test cores are subjected to comparison with five different reference levels at five different strobe times. The reason for this is that generally it is necessary to make a more detailed analysis of the core output when testing the core itself than when testing the memory plane which is made up of already tested cores. The amplitude measurements are made with respect to fixed reference levels which are set up on dials on the front panel. These levels can be adjusted from 0 to 100 millivolts. Two sense amplifiers and two pulse attenuators are used. Thus, if the ONE signal is larger than 100 millivolts, it may be attenuated before being amplified by the sense amplifier. The ZERO signal can be routed through a different attenuator and sense amplifier and therefore not be attenuated. This results in an improvement in the measurement accuracy.

Once the output of the core has been accurately measured, these measurements are logically combined in digital form in order to make the decision into which bottle the cores should be dropped. The cores can be sorted into accept or reject containers, or they can be measured for two levels of acceptance and one of rejection. In the latter case, cores within a preset range above a given level would be accepted in one category, those within a preset range below the given level would be accepted in a second category, and those outside of both ranges would be rejected (see diagram in Fig. 2).

Mechanical counters count the total number of cores tested, the total number of cores accepted, and the total number of cores rejected for each reason. Thus, at the end of a run, the operator has a complete picture of how well his cores met the required specifications and also the reasons for the failures. END

Digital Light Deflector

High-Speed Directional Control of Laser Light for Computer Applications.

Light deflection at electronic speeds has been a major problem in harnessing light for use in data processing; deflection under mechanical control is far too slow for most computer applications. Scientists at IBM report that they have developed an experimental device for electronically deflecting a laser beam to precise locations on any surface. The new device, called a digital light deflector, uses laser light to project letters, numbers or other images at high-speed to exact positions. IBM scientists say that with further development several million deflections per second can be achieved. The capabilities of the deflector point to potential applications in high-speed display systems, or in other areas of computer technology where data might be transmitted or processed using light rather than electrical signals.

Operation of the digital deflector is based on crystal optics. For example, if an alphabetic character is to be projected, the laser beam is first passed through a stencil-like mask of the character. The beam then enters the deflection assembly, which contains a series of crystals arranged in pairs. The first crystal in each pair operates as an optical switch. Actual deflection of the light beam occurs in the second crystal. By proper setting of the switch, the beam can be caused to follow one of two paths through the second crystal. Each succeeding pair of crystals placed in the beam's path doubles the number of positions to which the character can be projected.

The optical switches used in the deflector are potassium dihydrogen phosphate (KDP) crystals covered by semi-transparent electrodes. Birefringent calcite crystals are used as deflectors. Ordinarily, a beam of light entering a calcite crystal will split into two identical parts; in a properly oriented crystal, one beam will continue in the original direction while the other is diverted at an angle of approximately six degrees (see Fig. 1). The two rays emerge from the crystal in the same direction, but displaced a distance proportional to the length of the crystal. Thus, the placement of the image projected is determined by the number and length of the calcite crystals. Switching is controlled by the electrodes attached to the KDP crystals (see Fig. 2). Voltage applied to the electrodes changes the polarization of the light beam, causing it to pass through the calcite crystal on one or the other of the beam paths exclusively. The combination of a birefringent crystal and an electro-optic switch constitutes one stage of the deflector. Several stages are shown in Fig. 3. High-resolution deflection is performed in the convergent-beam version of the deflector shown in Fig. 4.

The light absorption in the deflector is reasonably small, so that with a laser as the light source, the outcoming beam can be very bright. The laser used in the digital deflector experiments is a commercially available He-Ne gas laser of 1.5 mw output. The new optical light deflector was described by IBM physicists Werner Kulcke, Thomas J. Harris, Kurt Kosanke, and Erhard Max in IBM's Journal of Research and Development.

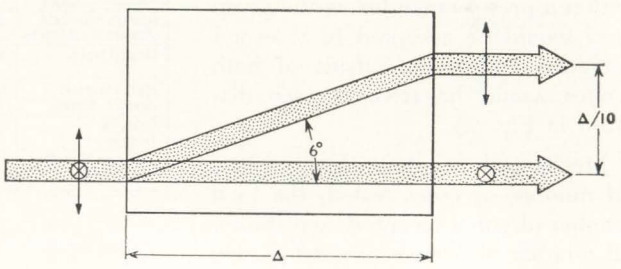


Fig. 1 The electro-optic light deflector design is based on crystal optics. The rectangular box shown represents the cross section through a transparent, birefringent calcite crystal. A collimated light beam enters this crystal and splits into two components, the ordinary ray and the extraordinary ray. At normal incidence, the ordinary ray propagates straight through the crystal, while the extraordinary ray is diverted. The ray separation angle depends on the birefringence of the crystal and on its orientation. In a properly oriented calcite crystal, this angle is approximately 6°. Both rays leave the crystal in their original direction but are displaced from each other by a distance proportional to the length of the crystal. The ordinary ray and the extraordinary ray are linearly polarized. Their polarization directions are perpendicular to each other. If, therefore, the incident beam is linearly polarized in one or the other of these directions, it passes the crystal as either the ordinary or the extraordinary ray exclusively.

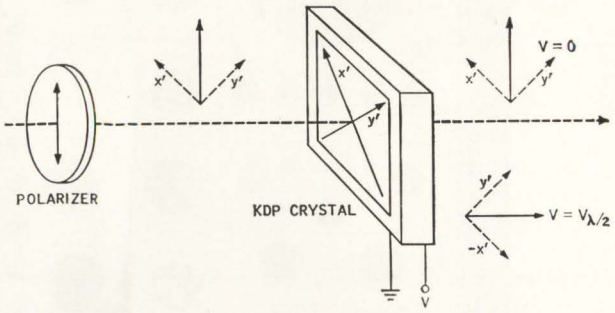


Fig. 2 This electro-optic switch controls the polarization direction of the light beam. The switch consists of a potassium dihydrogen phosphate (KDP) crystal. The water-clear KDP crystals are cut perpendicular to their optic axis. At normal incidence, a linearly polarized light beam splits into two components in the directions of the crystallographic x' and y' directions. Both components have the same optical path length in the crystal. Therefore, behind the crystal they recombine into a beam polarized in the original direction. Semi-transparent Nesa electrodes are cemented to the front and back surfaces of the crystals. If immersed in an index-matching fluid, these electrodes yield a transparency of 93 per cent. A voltage applied to the electrodes causes in the crystal an electric field which is longitudinal to the direction of the light beam. This field in turn induces an additional birefringence. At the so-called half-wavelength voltage, a path difference of a half wavelength exists between the components. The components behind the crystal now recombine to form a beam with a polarization direction oriented 90° relative to the original direction.

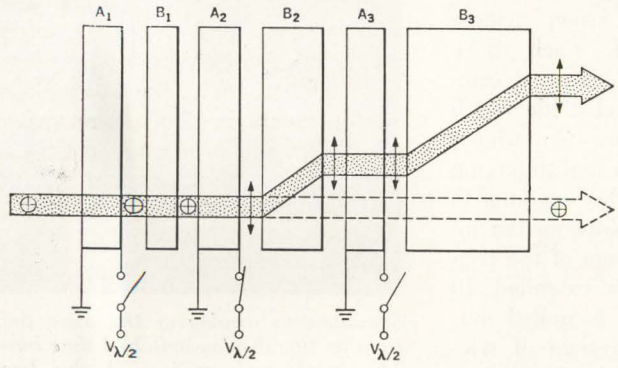


Fig. 3 Digital light deflector for collimated beams. The combination of a birefringent crystal, shown in Fig. 1, and an electro-optic switch, shown in Fig. 2, constitutes one stage of the deflector. In the six stages shown here, A denotes electro-optic switches, and B denotes birefringent calcite crystals. The incident collimated light beam is linearly polarized in the horizontal direction. Because switch A_1 is open, the light passes straight through calcite crystal, B_1, as the ordinary ray. Since switch A_2 is closed, the plane of polarization behind A_2 is vertical, and the light passes through B_2 as the extraordinary ray. As switch A_3 is open, the polarization direction remains vertical and the beam passes also through B_3 as the extraordinary ray. The displacement between the ordinary and extraordinary rays is proportional to the length of the calcite crystals. In sequential stages, lengths are chosen which increase as 1:2:4:8: . . . Thus, each stage yields a displacement one unit larger than the sum of the displacements of the preceding stages. If there are n stages, the number of beam positions is $N=2^n$; thus 10 stages yield 1000 positions. Generally, economical considerations will limit the aperture of the crystals to 30 mm. At a reasonable beam diameter of about 1 mm, less than 30 positions would be resolvable.

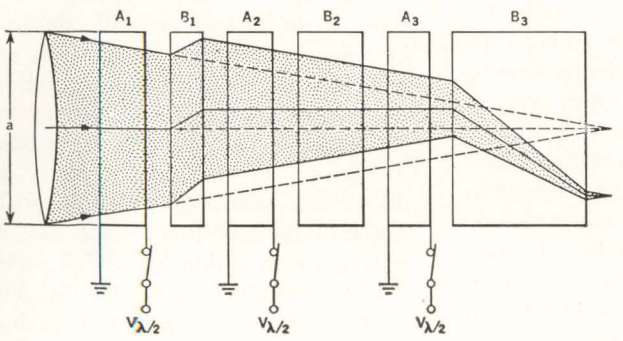
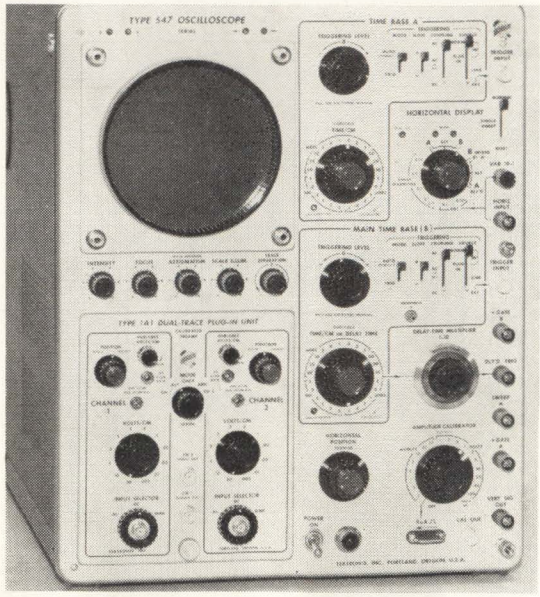


Fig. 4 High-resolution deflection is performed in the convergent-beam version of the deflector shown here. A lens is set in front of the deflector to focus the incoming light in a plane behind the deflector. This illustration depicts a case where all three electro-optic switches are closed. The light therefore passes through the first calcite crystal as the extraordinary ray. It passes through the second crystal as the ordinary ray, and through the third crystal again as the extraordinary ray. For reasons of symmetry, the third calcite crystal is turned upside down and yields a deflection in a direction opposite to that of the other calcite crystals. In this convergent-beam version, the spot size is very small compared to the aperture of the deflector. A large number of different output positions can therefore be resolved at reasonable crystal sizes. As a further advantage, the full aperture at the entrance is used. Thus the light output compared to that in the collimated beam version, is also increased. In the described deflector, the beam is deflected in one dimension. Two-dimensional deflection can be obtained if two one-dimensional deflectors are used in series, each yielding deflection in a direction perpendicular to that of the other.

AUTOMATIC DISPLAY SWITCHING OSCILLOSCOPE

New Model Offers Dual-Beam Performance At Single-Beam Cost



Tektronix's Type 547 oscilloscope features automatic display-switching of two identical time base generators. When used with dual-trace plug-in, as shown here it provides the user with two independent scopes in one cabinet, time sharing a single-beam CRT.

A dc-to-50 mc oscilloscope — Type 547 — featuring automatic display switching, plug-in preamp versatility and wide range sweep, has been developed by Tektronix, Inc. Automatic display switching is provided by alternate electronic switching between two identical widerange time bases — 0.1 usec/cm to 5 sec/cm. In this mode, the vertical signal from a single-channel plug-in can be alternately displayed on two different time bases. With a dual-trace plug-in unit, channel 1 can be locked to one time base, and channel 2 can be locked to the other. For many applications, one has dual-beam performance at a considerable saving of cost over a dual-beam scope. Price of the Type 547 is $1875.

When the two time bases are used for delayed sweep operation, a continuously-variable and calibrated delay is available from 0.1 usec to 50 sec. In this mode, each vertical signal — from a single or multi-channel plug-in — can be alternately displayed on time base B intensified by A, and time base A delayed by B.

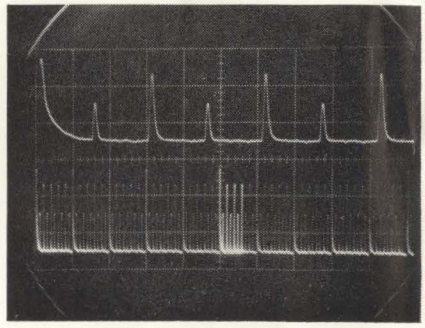
A front-panel control allows individual adjustment of trace separation when using automatic switching.

Triggering is stable over the full passband of the vertical-deflection system, providing triggered presentations to beyond 50 mc. The triggering circuitry includes automatic mode with bright reference trace.

Tunnel Diode Circuits

The two time base sweep trigger circuits are identical. Each is a wide-band hybrid amplifier and comparator driving a tunnel diode which produces uniform, fast-rise trigger pulses. The comparator and triggering level control enable the operator to select the triggering point on the incoming signal. The range of the triggering level control is extended 10 times when the knob is pulled out; this permits a wider range of triggering on higher amplitude signals.

The two identical time base generators consist of a basic vacuum tube Miller run-up circuit with a tunnel diode-transistor circuit to recognize input trigger pulses and form the sweep control gate. Use of a stable high-speed tunnel diode circuit to recognize the narrow fast-rise input trigger pulses eliminates need for the usual "sweep stability" control. Use of relatively high value timing capacitors and low value timing resistors provides improved accuracy and stability. Individual capacitor values to 10 ufd permit use of more-stable resistor values no higher than 7 megohms. Use of lower value timing resistors and limiting the excursion of sweep ramp to 100 v eliminates need for +500 v supply and provides the inherent stability of lower voltage operation. Although both time base generators are capable of equal accuracy, Time Base A cannot be calibrated to to the same accuracy as Time Base B because of measurement resolution limitations for Time Base A display. Time Base B can be calibrated to with-in 1% accuracy because Time Base A can be incrementally delayed by Time Base B and used as an expanded-scale, high-resolution indicator for measuring the accuracy of Time Base B. Accuracy of Time Base A can only be measured directly on the 10 cm horizontal graticule scale which limits resolution. Time Base A is accurate to within 2% of full scale.



Simultaneous display of the same pulse train on two display-switched time bases. The brightened portion of the lower sweep is displayed on the expanded and delayed upper sweep. The signal source is connected to input of a single channel vertical plug-in unit.

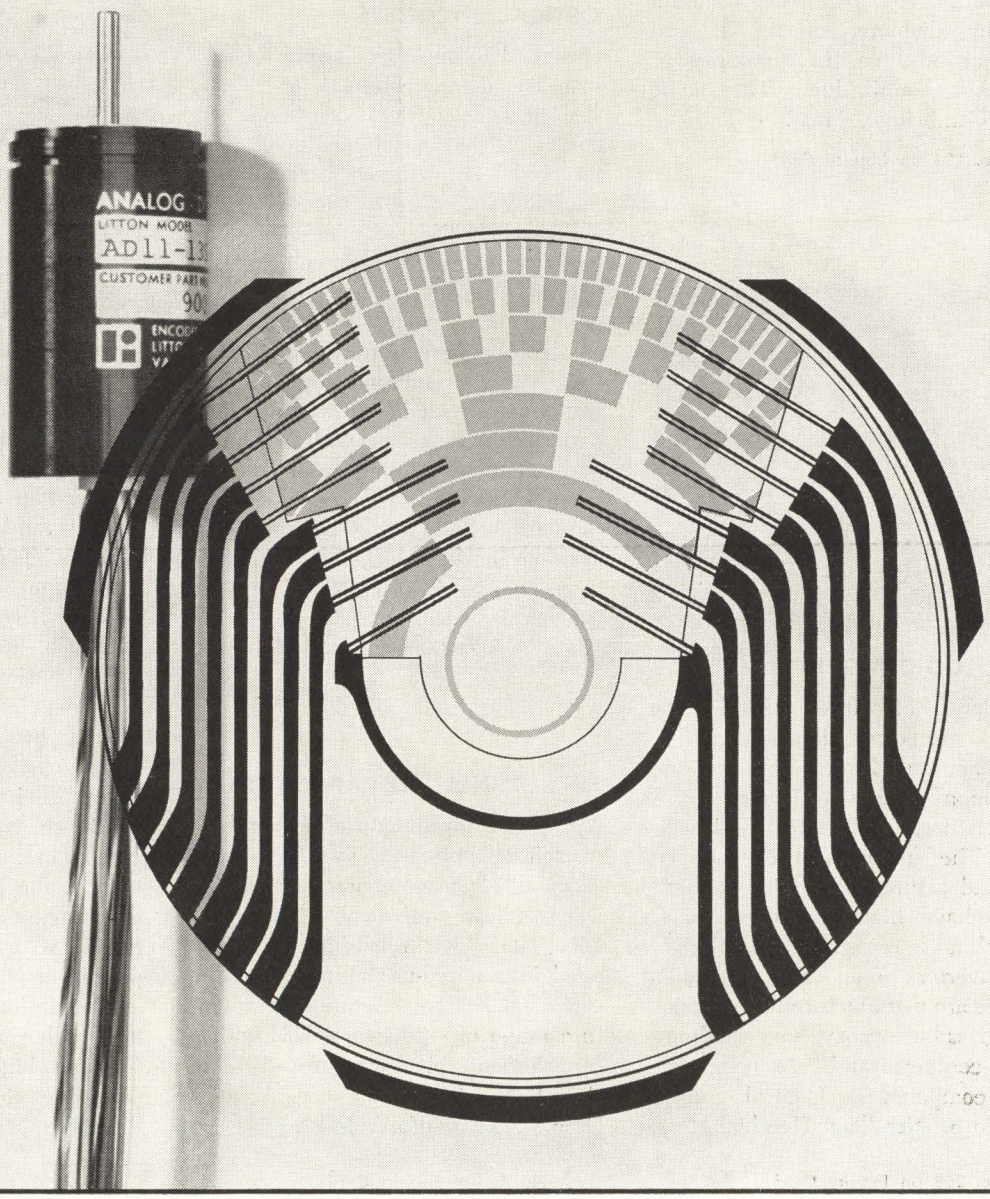
Literature giving more detailed description of the design and performance of the new scope is available from the company.

Circle No. 104 on Inquiry Card

WHO KNOWS MOST ABOUT SIZE 11'S?

Well, Litton did design the first practical Size 11, V-scan, natural binary, shaft angle encoder. And they've been mass producing them for years. In fact, most people refer to Litton as the Size 11, V-scan, natural binary outfit. Litton is flattered, but not entirely happy. This is because their encoder capability is by no means limited to a single size and type. They've done considerable engineering and development work on non-contact types, other sizes, and a variety of code schemes, including BCD, gray, sine-cosine and ARINC. So, if you've also been in the habit of thinking of Litton as a one-product house, please stand corrected. Talk to them about all of your shaft encoder applications and be assured of getting the same high quality and reliability exemplified by their well-known Size 11, V-scan's—2,000,000-revolution life expectancy; resolution of one part in 8,192 over full range of 32 turns; 0.3 oz–in maximum starting torque at room temperature; environmentally equal or superior to military specifications; and immediate availability in production quantities. All Litton encoders are dynamically tested in a computer environment more stringent than actual conditions. For details, write 7942 Woodley Avenue, Van Nuys, California. Or telephone 213-781-2111.

ENCODER DIVISION
LITTON INDUSTRIES



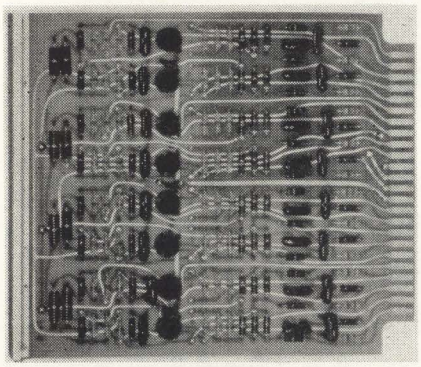
CIRCLE NO. 20 ON INQUIRY CARD

NEW PRODUCTS

WIRE-WRAP TERMINALS

A feed-thru insulated terminal was designed expressly for high-volume wire-wrap applications, such as telephone and data processing equipment. The new terminal is a press-mount type that can be mounted with standard hand insertion tools or punches and anvils. It is available for panel thicknesses from 0.031″ to 0.148″, has maximum lengths of 0.563″ above-board, and 0.461″ below board, and a mounting diameter of 0.172″ and priced at $.09 ea. in quantities of 250-499. Cambridge Thermionic Corp., Cambridge, Mass.

Circle No. 231 on Inquiry Card



500KC LOGIC MODULES

New Series of 500kc digital logic modules are compatible with company's 2mc and 10mc series, and use a common system of logic levels, nomenclature, connections, and voltages. The modules use clamped loads and saturated circuits, and are said to have high fanout capability and high noise rejection. Both NAND and inverter logic are available. Modules are manufactured of military-grade glass base epoxy, have rhodium-plated contacts, and use computer-grade components. Control Equipment Corp., Needham Heights, Mass.

Circle No. 208 on Inquiry Card

NATURAL CODE OPTICAL ENCODERS

Designed to supersede cyclic (Gray) code encoders, a complete new line of natural code optical shaft-angle encoders is said to eliminate all need for code converters. Reliability is markedly improved by the use of low-voltage long-life incandenscent lamp modules instead of high-voltage flash lamps. The outputs are dc levels in parallel form and are continuously available. There is no limit to interrogation rate. Integral code displays can be provided. Units providing natural binary codes with resolution and accuracy ranging from 5 digits through 20 digits per revolution and in natural BCD codes of equivalent accuracy and resolution are available. Wayne-George Corp., Newton, Mass.

Circle No. 219 on Inquiry Card

MICROMINIATURE CAPACITORS

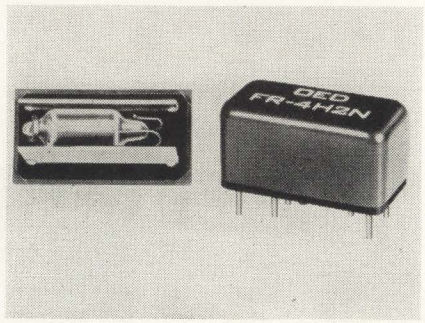
A new "ultra-miniature" electrolytic capacitor Type TTC is said to have excellent electrical characteristics, low leakage, low equivalent series resistance, and high reliability—all packaged in a micro-miniature case. The capacitor has an operating temperature range of −30C to +65C with a capacitance tolerance of −10% to +100% of rated capacitance. Aerovox Corp., New Bedford, Mass.

Circle No. 124 on Inquiry Card

DIGITAL SWITCHES

New models in a series of digital switch indicators include colored switch and spacer modules for greater visual identification. The use of colored Digiswitches, as they are called, provides user with visual separation and identification of multiple functions in single, easy-to-install assemblies. More than 40 standard models are available, covering a wide range of codes and functions such as octal-to-decimal conversion, decimal-to-binary conversion, conversion-to-binary with complement, voltage divider, resistance decades, etc. The Digitran Co., Pasadena, Cal.

Circle No. 134 on Inquiry Card



OPTICAL RELAYS

Two series of photo-electronic Opto-Electronic relays, called Logitron offers completely isolated input and output circuits coupled only by a light beam. Visual state indication is standard in all Logitron relays making fast and simplified system check possible. Typical ratings are 120 vdc, 2 ma input, 350 mw per cell dissipation for two-pole and 125 mw for four-pole, and up to 300 vdc. The FR-N Series provides high power gain, switching ratios greater than 10^4 with typical dynamic response of up to 100 cps. The "ON" or conducting resistance is 5K or less and "OFF" resistance greater than 10 megohms. Nominal input rating for all four Logitrons in the FR-I series is 12V, 12ma. Construction of all Logitrons is compatible with printed circuit board or plug-in assembly. Overall dimensions are 1 inch long x ½ inch wide and ¾ inch high. Installed, Logitron is only ½ inch high. Opto-Electronic Devices, Inc., Sub. of Sigma Instruments, Braintree, Mass.

Circle No. 221 on Inquiry Card

SUBMINIATURE LAMPHOLDERS

Space-saving lampholders have been designed for use with midget-grooved base incandescent lamps, including the distinctive lens-end lamp. Units can be equipped with a variety of mounting brackets. They may be either grounded with one solder terminal or one wire lead; or they may be insulated with two solder terminals or two wire leads. The lampholders provide for rapid lamp insertion and have a built-in lamp ejection feature. Lens-end lamps can be easily rotated for desired focusing while maintaining positive contact. They are said to be especially effective in data processing equipment. The lamps produce a minimum of 750 foot-candles of light and have an expected life of over 10,000 hours. The exacting beam tolerances of these lamps make them essential in scanning and readout applications and computer operations using punched cards or running tapes. Leecraft Mfg. Co., Long Island City, N.Y.

Circle No. 138 on Inquiry Card

TAPE TRANSPORTS

A precision-engineered, 100 track tape transport stores 20,000 five-minute messages on 600 feet of 3-inch wide magnetic tape. Five head stacks of 20 channels each are used in a staggered arrangement giving 100-parallel track capability. Tape speeds are 15/16 and 1⅞ ips, with 10 second rewind access time. By use of a four track search head, storage for 19,200 5 minute messages with a 30 second interval between messages is accomplished. All search control devices are included in the one package. Extremely gentle tape handling is accomplished by the use of rotary guides. Rollers and guides are grooved to assure proper contact between the tape and guides and also to prevent tape jitter while in motion. Tape lifters allow the tape to contact the heads only in play mode. However, in the moderate and fast modes of operation, the tape contacts the search head only. Telectro Industries Corp., Long Island City, N. Y.

Circle No. 165 on Inquiry Card

SUBMINIATURE COAXIAL CONNECTOR

New connector uses a "Fast-Lok" connecting principle instead of standard bayonet method. It is said to have extreme utility in all applications where coaxial connectors are used and especially in large computer harnesses where maintenance becomes a very important factor. According to the company, its small size, 0.225″ O.D. by 13/16″ long, makes it a true miniature in relation to the old style threaded versions. In wiring bundles it provides easy connections and disconnections while assuring high reliability in contact connection. The positive mechanical lock is not dependent upon spring tension. There is no twisting or turning necessary. Only a straight push-pull action. Closely-held manufacturing tolerances plus the simplicity of mechanical design eliminates variable fitting problems which sometimes defeat the utility of this type of connector. National Connector Corp., Minneapolis, Minn.

Circle No. 141 on Inquiry Card

NEW PRODUCTS

WIRE HARNESS TESTER

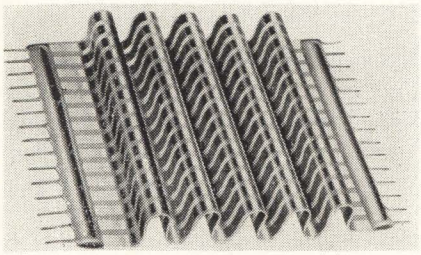
Designed, developed and built for production tests of computer wiring and cables, a self-testing wiring harness tester probes each point for continuity as well as discontinuity with respect to all other points, scanning up to 3120 points per test bay. In the automatic mode, a master chassis or unit known to be wired correctly is compared with the chassis or unit under test. An OPEN error lamp lights during the first test phase if one or more wires is missing. A SHORT error lamp lights during the second test phase if one or more wires is connected to the wrong pin. Nixie tubes indicate which pin was transmitted to at the time of failure. Neon bulbs on the front of each test bay indicate which wire or group of wires are involved in the error. Thus isolated, the error then can be corrected, without removing the unit under test. Each test bay checks over 3000 wiring points in 5 minutes. The tester can also be used in business machine checkout, terminal communications maintenance, switchboard network checkout, and missile test facility wiring network checkout. California Computer Products, Anaheim, Cal.

Circle No. 121 on Inquiry Card

HIGH-SPEED A/D CONVERTERS

Solid-state high-speed analog-to-digital converter has a bit rate capacity of 160 kc including recovery time. For special requirements, bit rates to 300 kc are available with the accuracy of 0.05% $\pm\frac{1}{2}$ LSB. Bipolar inputs from a few millivolts to 100 volts are accepted and a decimal readout display is optional. Sample and hold capabilities are included to allow true time and data collation. The converter, which mounts in a standard 19″ relay rack, is fully compatible with company's standard multiplexers. Gulton Industries, Inc., Metuchen, N.J.

Circle No. 139 on Inquiry Card



PC BOARD JUMPERS

New flexible printed circuit board jumpers, called Flex-Weld, withstand millions of flex cycles without failure. Flex-Weld jumpers provide electrical characteristics identical to printed circuit boards. Compatible with printed circuit boards, the prepositioned pins and modular design of these jumpers permit them to be quickly removed, joined, and reshaped to changing needs. Flex-Weld jumpers offer simplified soldering, installation, and checkout procedures; eliminate wiring mistakes, coding, lacing, and quality assurance inspections. Conductors are isolated for minimum intercapacitance. Flat, thin, lightweight, these jumpers are available in 8 standard models — straight or corrugated. The straight type is flexible; the corrugated type is flexible, stretchable, and compressible to eliminate custom jumpers required to fit "remaining environments". Insulation is either Mylar or Teflon. Digital Sensors Inc., Los Angeles, Cal.

Circle No. 213 on Inquiry Card

MINIATURE REED RELAYS

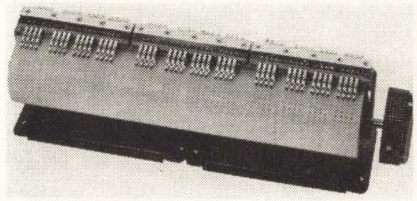
New series of reed relays have a life expectancy of 200 million operations at signal currents. They are said to have exceeded this in field tests to one billion trouble-free operations within specification. The entire reed/coil assembly is encapsulated in a specially formulated, highly stable epoxy material, which combines optimum electrical and physical properties that assures high dielectric strength and insulation resistance. This very resilient material prevents glass switch enclosure stress over specified temperature, vibration, mechanical and thermal shock ranges. Axial leads can be easily bent during installation without changing performance characteristics. Elec-Trol, Inc., Northridge, Cal.

Circle No. 133 on Inquiry Card

COMPUTER POWER SUPPLIES

A new series of four transistorized dc power supplies were especially designed for use in computer circuits and communications equipment. Units are rated at 50 volts dc. Four models are available in 25, 50, 100, and 200 watt capacities. Maximum output currents are 0.5, 1, 2, and 4 amperes. Output can be adjusted over a 2:1 adjustment range. Regulation is within ±0.01% (line and load combined) and ripple is less than 300 microvolts rms. Transient reponse time of 25 microseconds or less permits rapid recovery from abrupt changes in input voltage or output load to provide an exceptionally smooth, "spike free" output for use with critical systems, particularly transistorized ones. Featuring constant current, programmability and remote sensing capability, the supplies can be used in either series or parallel operation (up to 20 in parallel or four in series). Sorensen, Raytheon Co., So. Norwalk, Conn.

Circle No. 129 on Inquiry Card



PROGRAMMER DRUM

A new switch programmer features 48 positions, each having 48 independent selectable switching stations. Multiple stacked contacts can be provided at each switching station. These contacts can be supplied in practically any combination of SPST, (normally open); SPST, (normally closed), DPDT, (make before break), DPDT (break before make) functions. The AP48D48, as it is designated, has the capacity for storing 48 independent programs and is programmed by inserting actuating pins in the programming drum to activate the appropriate contact desired at each position. Contacts are rated at 2 amps at 24 vdc and 115 vac. Mechanical life is in excess of 100 million operations. This unit is available with either standard solder lug terminals or with integral flat wire cabling. Sealectro Corp., Mamaroneck, N. Y.

Circle No. 222 on Inquiry Card

for more information on editorial or advertised items use free inquiry card opposite page 41

NEW PRODUCTS

MICROELECTRONIC WELDING

Synchronous timing — said to be a vital requirement for providing repeated, identical bonds in microelectronic circuits — has been achieved in a new "Microwelder" Mark II. It is a resistance welder operating on a 120 vac, 60 cycle, single-phase circuit. Among its unique characteristics is the single tip, which contains both electrodes in a very small diameter. This feature permits the welding of lead materials as small as 0.0005 inches to positions on 0.003 inch centers. For precise control of pressure, gram weights are placed on the top of the tip itself, providing absolute force control from 10 to 1,600 grams. Synchronous timing gives precise control of energy, resulting in identical weld pulses. Three power ranges make possible the welding of a wide variety of material and sizes with accurate resolution within each power range. Weld energy can be completely adjusted with controls that regulate pulse amplitude and duration and number of pulses in the weld cycle. Either pre-heating or post-heating also can be applied. Aerojet-General Corp., Azusa, Cal.

Circle No. 122 on Inquiry Card

MINIATURE MYLAR CAPACITORS

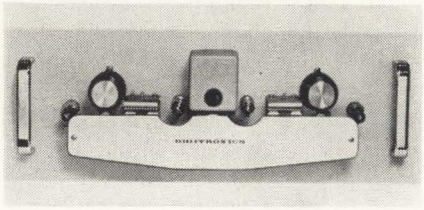
Designed for use in miniaturized solid-state circuitry, a new series of metallized Mylar epoxy encapsulated capacitors feature tiny size with high ratings for 200 dc working volts operation. Designated Type QCA, 12 sizes have been standardized ranging in capacities from 0.01 mfd to 1.00 mfd. Dimensions of the smallest size are 0.38″ x 0.32″ x 0.23″. Operating temperature is from —55C to +125C at full rated voltage. All sizes come with optional straight leads or formed leads. Insulation resistance is 50,000 megohm microfarads at 25C. Dissipation factor is less than 1 percent at 1 kc and +25C. Hopkins Engineering Co., San Fernando, Cal.

Circle No. 149 on Inquiry Card

MINIATURE REED RELAYS

Nylon encapsulation is a new insulating housing for miniature reed relays. Several advantages are claimed for the new use of nylon over conventional plastics as an encapsulation material, the most important being high resistance to thermal and physical shock encountered under conditions of rapidly changing temperature and high vibration frequencies. Other advantages include excellent dielectric strength with relatively thin coatings which permits more turns of magnet wire within conventional specified miniature relay dimensions to meet a much broader range of operating conditions. The new nylon-encapsulated reed relay is rectangular in shape and measures 1.375″ x 0.425″ x 0.425″. Operating voltages are 6, 12, and 24 vdc at 250 milliwatts. Grigsley-Barton, Inc., Arlington Heights, Ill.

Circle No. 150 on Inquiry Card



PAPER TAPE READER

Two new low-cost, photo-electric perforated tape readers operate at speeds up to 700 characters-per-second. Model B3000 reader is bi-directional and is priced at approximately $1,800. Model 3000 reader is uni-directional and is priced at approximately $1,500. Both models are all solid-state, have self-adjusting brakes, and read 5, 6, 7, or 8-level tapes. Silicon photo-diodes in the read head service all eight data channels, plus sprocket channel. Compatible spoolers (Model 6070 and 6050) are available for operating with the readers. They can handle 8-inch reels up to 700 characters-per-second, or 10½ inch reels at 500 characters-per-second. The readers measure 19 inches in width and 7 inches in height; panel thickness is ⅛ of an inch; depth behind the front panel is 8½ inches; extension beyond the front panel is 2⅛ inches. Each reader weighs 28 lbs. Digitronics Corp., Albertson, N.Y.

Circle No. 218 on Inquiry Card

LOGIC MODULES

With the addition of eight new logic modules, company now offers a full line of 40-logic modules which permit the performance of 96% or more of all the driver operations any user may require. Of the eight new modules, four are drivers, two are binary counters, and two are translators. The driver modules are: the AO 30114, containing ten single-stage NPN lamp drivers; the AO 30115, with ten single-stage PNP crossbar actuator drivers; the AO 30117, which contains six single-stage NPN lamp drivers; and the AO 30118, with six single-stage PNP cross-bar actuator drivers. The binary counters are: the AO 30112, a four-bit saturated binary counter with flip-flop reset and maximum count restricted to ten, and a weighting of 1-2-4-8; and the AO 30133, a three-bit saturated binary counter with maximum count restricted to 6, 3, or 2 and a weighting of 1-2-4. The translators are: the AO 30133, a decade diode translator externally enabled by 1-2-4-8 BCD; and the AO 30116, a diode translator externally enabled by 1-2-4 BCD and having six outputs. James Cunningham Son & Co., Honeoye Falls, N. Y.

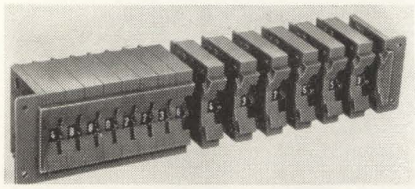
Circle No. 225 on Inquiry Card

COUNTER-TIMER

A new all transistor dc to 50 megacycle universal counter-timer features inline Nixie readout, display storage (memory), floating input with respect to ground, and dc amplifiers for precise measurement of single and mutiple periods. Trigger level error has been reduced to less than 1 usec with a 1 kc sine wave of 100 mv rms. The Model 727D combines the functions of a counter, time interval meter, and frequency/period meter. It consists of three input channels, a special decade countdown time base which eliminates the need for divider adjustment, and a series of plug-in decade counting units. BCD output information from each counting unit is brought out to a rear connector for use with digital printers, punches, remote readouts and other data processing equipment. Computer Measurements Co., San Fernando, Cal.

Circle No. 155 on Inquiry Card

NEW PRODUCTS



NUMERIC DISPLAY CONTROL

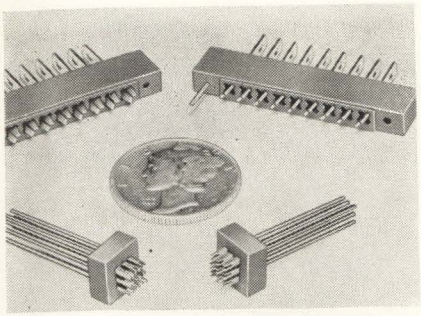
A new series of switches were designed to provide reliable, low-cost decoding for electroluminscent display readouts. The "Decaswitches", as they are called, decode thumbwheel positions directly to numeric display without the need for any additional electronic components. According to the company, the Decaswitches offer virtually unlimited stacking possibilities, are rugged, reliable, and will maintain position regardless of power continuity. Decaswitches will work with either electroluminescent, incandescent, or neon display devices. Data and Controls Div., Lear Siegler, Inc., N. Y., N. Y.

Circle No. 161 on Inquiry Card

GRAPHICAL DISPLAY SYSTEMS

Based on an entirely new engineering concept in digitally controlled display systems, a new, low-cost, all-digital display system, the VP 600, offers at a selling price of less than $20,000 many features which have been available only in systems selling at many times this price, according to the manufacturer's report. The all-solid-state system is designed to meet many requirements of E. I. A. and N. A. S. specifications for N/C Drafting Machines. It is basically a continuous path automatic drafting machine capable of producing a high-quality graphic display of digital information on drafting film, paper, vellum, cloth, Mylar, sensitized sheet metal, or comparator screen material to a standard size of 50 x 60 in. Input data in the form of punched paper tape containing the incremental distance to be traversed between coordinate points is entered into the electronic control unit via the self-contained tape reader. The operator may select any two axes from three-axis tape. Controls are provided for producing right and left hand drawings from a single tape. Drawing speeds up to 200 in. per minute are internally computed. Manual speed reduction is available for high-precision applications. Full jog controls are provided to allow the operator to position manually each axis independently at a preselected speed. The resulting graphic display is produced with an overall maximum accumulative accuracy of ±0.010 in. anywhere on the plotting surface. Repeatability is ±0.004 in. As an automatic drafting machine the VP 600 is said to be ideal for the preparation of preliminary design and detailed drawings and an ideal output device for computer-aided design activities. The VP 600 can also be utilized wherever graphic retrieval of data from digital devices is desired. Displays can be made in conjunction with telemetry records, oceanographic studies, highway planning, statistical and test data, mapping and surveying and various other applications. Computer output can be displayed directly by online operation of the VP 600. The Gerber Scientific Instr. Co., Hartford, Conn.

Circle No. 152 on Inquiry Card



ULTRA-MINIATURE CONNECTOR

New connector, tradenamed the BI/CON, makes it possible to "substrate", with rapid disconnect features, units previously integrated or unitized because of space limitations. New ultraminiature connector is said to be ideally suited for magnetic core memory stacks which presently do not possess advantage of convenient stack assembly. Therefore, the company reports, the current, contact density and retention capabilities of BI/CON are compatible with the needs and requirements of any miniaturized equipment. Photo shows comparative size of 9-contact BI/CON with previous 9-contact microminiature model. Mating area, along with the 0.020" diameter bi-channel tails of the new BI/CON models readily permits contact spacing at 0.050" square grid pattern. Terminations can be soldered or welded to wires for printed circuit cards or card edge to card edge components. Contact tails can be made to specific lengths to facilitate individual terminating applications. ELCO Corp., Willow Grove, Pa.

Circle No. 177 on Inquiry Card

TRANSISTORIZED DIGITAL CLOCK

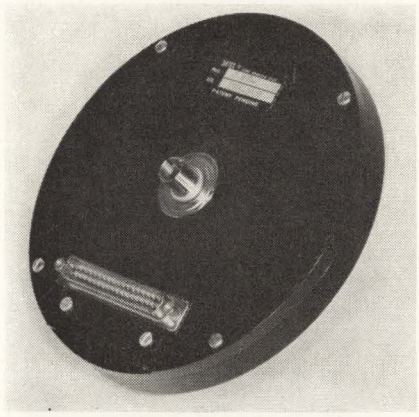
A completely self-contained digital clock which utilizes no moving parts was specifically designed to work in conjunction with data acquisition and handling systems. The clock has three unique features: a power failure indication, essential to applications for unattended operation; a 10-position logging control for starting external processes on a repetitive basis; and a built-in storage capability that allows the clock readings to be held stationary for up to 3 seconds so that readings may be automatically printed. Electro Instr. Inc., San Diego, Cal.

Circle No. 137 on Inquiry Card

A/D CONVERTER

Especially designed for applications using BCD format, a new A/D converter can make 50,000 conversions per second, including its built-in sample and hold feature. Accuracy is ±0.05% FS ±1 LSD. Important specifications include input impedance greater than 100 megohms, voltage ranges from 1 to 10 volts, and aperture time of 100 nanoseconds. Manual or external range selection is provided. Single conversions can be made with a front panel push-button. Texas Instruments Inc., Industrial Products Group, Houston, Texas.

Circle No. 130 on Inquiry Card



SHAFT POSITION ENCODERS

Designated C-759 and C-950 Series, a series of shaft position encoders featuring high resolution for a single turn input are available with outputs up to 2400 counts in company's code and 2048 counts in Gray code for 360° input rotation. Models are available with hollow shafts for mounting directly on strip chart recorders and solid shafts for general purpose applications. Encoder output is in the form of contact closures with a closed circuit representing a binary one and an open circuit a binary zero. The brush/disc contact arrangement is rated for 30 vdc, 2 ma (non-inductive) with encoder rotating or 30 vdc, 30 ma (non-inductive) with encoder stationary. Maximum operating speed for "on-the-fly" readout is 90 rpm and maximum slew speed is 600 rpm. Diameter of the encoder is 6.125 inches. Accuracy is ±1 count over any output range. Datex Corp., Monrovia, Cal.

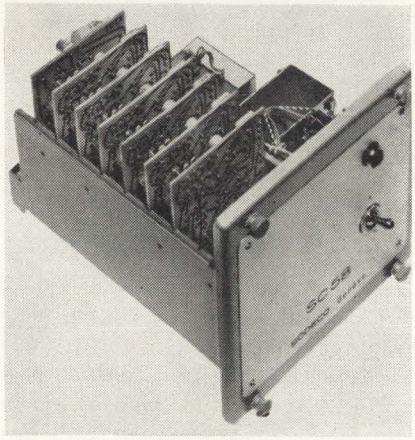
Circle No. 186 on Inquiry Card

NEW PRODUCTS

MINIATURE DELAY LINE

New miniature delay lines were designed for computer printed circuit, pulse forming, and coding applications. They feature delay times from 0 - 5 usec, ±3% or better, with a maximum rise time equal to 15% of delay time, and an impedance up to 4000 ohms. Phase response is 1% up to 3db, with a frequency response of up to 10mc. Attenuation is less than 0.1db/-usec, and the temperature coefficient equals 0.1%/degrees C. Units are encased in epoxy, completely potted in a maximum case size of 1.3 cu. in. Data Delay Devices, Dover, N.J.

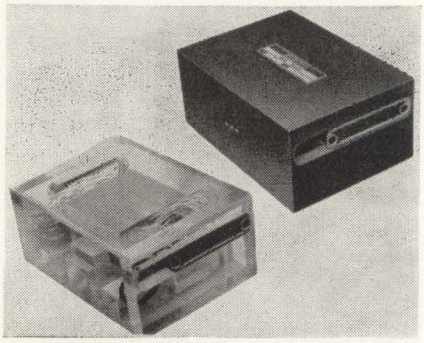
Circle No. 125 on Inquiry Card



IMPULSE SUMMER

A new device, called the SC58 Summator receives and stores input signals originating from several different sources then scans the transistorized storage and summarizes the impulses on a single counter. Input signals may be generated by photocell systems, electrical impulses or electro-mechanical contacts. Output goes to high speed electronic counter, or, with amplification to an electro-magnetic counter. The SC58 may be specified for any number of circuits from 2 to 8. Use of an auxiliary unit, the SC59, increases the unit capacity to 24 circuits. Landis & Gyr, Inc., New York, N.Y.

Circle No. 156 on Inquiry Card



REED RELAY PACKAGE

One hundred dry reeds are incorporated into a single package for a new missile ground control computer. A new method of encapsulation was used, involving polyurethane foam, which affords, according to the company, lighter weight and repairability not possible with solid potting materials. All 100 reeds operate from a single coil with 5.0 milliseconds response at nominal coil voltage. Outside dimensions of the package are approximately 4½" x 6¼" x 2¾". Wintronics Div., Michigan Magnetics, Inc. Hawthorne, Cal.

Circle No. 153 on Inquiry Card

GATE EXPANDER MODULE

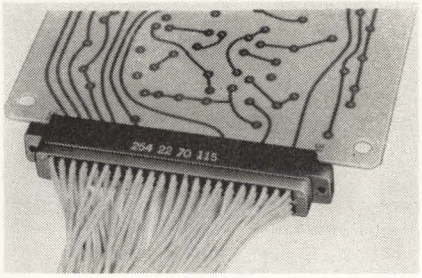
A new, all-silicon gate expander module contains twelve 2-diode AND gates and seven gate load resistors. The individual circuits can be used to expand gate structures on other modules in order to form combinations of AND/OR logic constructions. All semiconductors are silicon, giving the module a reliable operating range from 0C to 100C. Cost, however, is said to be comparable to that of lower performance germanium modules. Noise rejection is said to be twice that of competitive circuits. Reliability is further increased by the use of metalfilm resistors and by a conservative design approach. All components are derated far below manufacturer's specifications. "Worst case" design analysis provides for normal operation even if all components simultaneously assume their worst possible condition. Three models are available, with maximum operating frequencies of 300 kc, 1 mc, and 5 mc respectively. Scientific Data Systems, Santa Monica, Cal.

Circle No. 184 on Inquiry Card

VOLTAGE/CURRENT CALIBRATOR

Magnetic memory core characteristics, and similar complex signal sequences, can be precisely calibrated by a new Model 1085 Dual Level Voltage/Current Calibrator that superimposes two independent reference voltages upon input waveforms so that they may be compared on a display oscilloscope. Analysis of ac, pulse, or dc signals ranging from 1 mv to 10 volts may be made with the 1085, and with the use of an external attenuator, signals up to 200 volts can be measured. The Model 1085 generates two highly stable dc voltages which are independently variable from 0 to 10 volts. These voltages are referenced to cascaded zener diode circuits which can be sub-divided into increments as small as 1 mv by temperature-compensated precision resistors. Reference amplitudes are controlled by two precision linear potentiometers. Reference voltage levels may be positive or negative and adjusted to correspond visually with a specific point on the unknown waveform. Computer Test Corporation, Cherry Hill, N. J.

Circle No. 224 on Inquiry Card



EDGE CONNECTORS

A line of edge connectors with crimp-on, snap-in pins combines the reliability of permanently assembled bifurcated contacts with the convenience and versatility of a crimp-on, snap-in connector. The lead wire side of the connector is designed for crimp-on, snap-in removable wire pins inserted into twin-barrel contact receptacles, permitting two wires per contact and four wires per connector position, (two wire leads per board position on each side). The new connector, called the Twin-Con meets MIL-C-21097, latest revision, and is designed for use with double-sided 0.062" printed circuit boards. Cinch Mfg., Chicago, Ill.

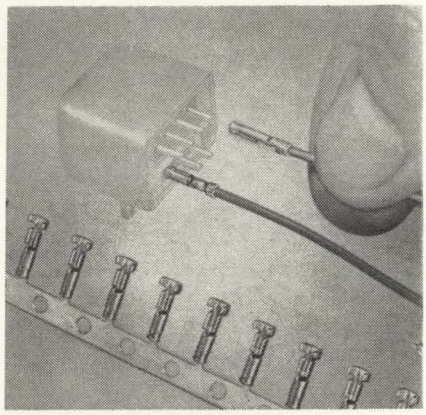
Circle No. 123 on Inquiry Card

NEW PRODUCTS

MINIATURE TUBULAR CAPACITORS

A new miniature tubular ceramic capacitor is housed in a molded plastic case measuring 0.400″ long by 0.140″ in diameter. It is available with axial tinned copper or weldable gold plated dumet leads for cordwood packaging. Capacitance values range from 12,000 to 100,000 mmf in tolerances of ±10% and ±20%. The capacitors are rated at 50 vdc over a temperature range from —55C to +125C. Units exceed the requirements of MIL-C-110-15C. Gulton Ind., Metuchen, N.J.

Circle No. 176 Inquiry Card



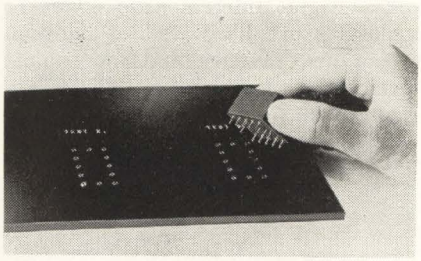
MINIATURE TERMINALS

Newly available miniature female receptacles reduce wiring time, speed production, and save assembly costs. Said to be the first self-retaining terminals developed specifically for application to magnetic tape heads, new female receptacles were designed for permanent connections and where quick connect and disconnect terminations are desired. The terminal can be solderless wire crimped to size 26 to 22 insulated wires. The receptacle has an I.D. slightly smaller than the O.D. of the 0.050 pin to provide positive holding tension. The receptacles can be supplied in chain form for automatic feeding and crimping operations. Malco Mfg. Co., Chicago, Ill.

Circle No. 171 on Inquiry Card

MODULE TESTING

Assembled circuit modules may be electrically tested, individually or in combinations, by use of standard plug-in boards that feature sockets



which accept 0.032″ pins or a 0.100″ standard grid with 0.100″ minimum spacing, or 0.040″ pins on a 0.100″ grid with 0.200″ minimum spacing. The plug-in test boards, machine-molded from glassfilled epoxy or diallylpthalate, are ⅛″ thick and are available off-the-shelf in a variety of sizes from 0.590″ x 0.790″ up to 5″ x 8″. The sockets may be positioned to the user's specifications at random on the 0.100″ grid. For convenience in mounting on test panels, most of the plug-in test boards have mounting tabs with 0.093″ diameter holes. After mounting of the test boards, circuit modules may be plugged in securely and removed instantly, on a production line for example, to receive the next module for testing. For module reliability programs, the circuit package may remain plugged in to the test board for life or environmental testing. U.S. Dielectric Inc., Worcester, Mass.

Circle No. 173 on Inquiry Card

ELECTROLUMINESCENT DISPLAY

New high reliability electroluminescent display in a compact package includes power supply and encoding circuits. Forming numbers and letters, the display has an internal power supply that generates the excitation signal and requires only low voltage dc in the 6 to 48 volt range. The display will operate from any type of input signal and accepts decimal or BCD inputs. A self-contained encoder converts these input signals and provides the control for excitation of the desired character. Vogue Instrument Corp., College Point, N. Y.

Circle No. 228 on Inquiry Card

POWER SUPPLIES

Easy to use power supply catalog lists 132 standard production models subdivided into 11 design groups. Each of these design groups is described in terms of its outstanding characteritics. In order to save the users' time and to simplify the finding of a regulated power supply for a particular application or set of requirements, a second listing in the form of an "Index By Output Voltage" is included. The catalog includes basic regulation figures, voltage and current ranges, prices and shipping weights. Units are voltage and current regulated. Kepco, Incorporated, Flushing, N.Y.

Circle No. 146 on Inquiry Card

SELF-DECODING BINARY READOUT

A self-decoding binary readout has been re-designed to provide complete alpha-numeric display capability. Now featuring up to 41-message capacity, the "Bina-View", as it is called, takes any binary code up to six bits, decodes it automatically, and displays the required message (up to 1⅜″ in height) on a single-plane viewing screen. In addition to the alpha-numeric capability, the device also displays colored, symbols, words. Floating right or left decimal points are available from a separate lamp circuit and are additional to the basic 41-message capacity. Decoding to digital messages by the electromagnetic readout is entirely self-contained; no additional translators, relays, or diodes are required. It provides automatic memory and retains the last message displayed after signal and set-pulse power have been removed. "Bina-View" may also include auxiliary contact closures that can be used for check-back to verify input signals and to transmit input signals back into source equipment. Industrial Electronic Engineers, Inc., No. Hollywood, Cal.

Circle No. 167 on Inquiry Card

LITERATURE

Paper Tape Reader

Data sheet describes a paper tape reader that reads up to 8-channel paper tape, bi-directionally, at a speed of 30 cps. Sensing of the punched holes is accomplished by the use of star wheels. When a star wheel enters a hole, an arm carrying the star wheel closes a switch. The switch construction is similar to the switches in wire relays. Bounce time of the sensing switches is well under a millisecond. A switch is also provided on the tape hold-down arm. When tape is being loaded into the unit this switch is open. A simple tape-driving mechanism drives the tape in either direction in response to an input pulse and does not require complicated timing logic. Full specs are given. Ohr-Tronics, Inc. South Hackensack, N.J.

Circle No. 148 on Inquiry Card

Tape Recording Glossary

A 12-page monograph titled, "Glossary of Terms Used in Magnetic Tape Recording," defines and explains the more fundamental terms common to a wide range of magnetic recording applications. Many of 177 items listed are defined for the first time. Memorex Corp., Santa Clara, Cal.

Circle No. 158 on Inquiry Card

Pulse Transformer Design Notes

A new technical paper "Design Notes on Low Power Pulse Transformers", is intended to help designers of digital circuitry, blocking oscillators circuits, radar circuits, and others understand basic problems involved in supplying pulse transformers to meet their circuit needs. The operating characteristics and physical factors of these magnetic components are fully explained in this excellent 12-page dissertation. For a free copy of paper, send your request on your company letterhead to:

Technical Literature Service
Sprague Electric Co.
Marshall Street
North Adams, Mass.

Real-Time Computer

A 16-page brochure describes a "real-time" data processing system and explains "real-time" data processing for business applications such as inquiry handling, data collection, and management controls, and defines much of the terminology associated with data communications. Honeywell EDP, Wellesley Hills, Mass.

Circle No. 144 on Inquiry Card

Computer Services

A new 20-page brochure describes in detail a company's experience and capabilities in such areas as management science, economics, mathematics and statistics, computer service, and programming applications. Also included in the brochure is a bibliography of problem-solving literature produced by, and available from, the company. These publications range in subject matter from linear programming to the newest techniques in management science such as PERT, CPM, and RAMPS (Resource Allocation and Multi-Project Scheduling). C-E-I-R Inc., Arlington, Va.

Circle No. 154 on Inquiry Card

Non-Snap Switch

Specifically designed for cam actuation up to 1200 impulses-per-minute with no measureable contact bounce and for applications such as cam actuated timers, programmers, and data processing card punching equipment, a new non-snap-action switch operates for a minimum of 100 million cycles at 350 ma-170 vac, or 10 ma-30 vdc. Unique blade design provides high contact pressure and no measureable contact bounce. Only 0.190″ thick, the Type 40 switch has a built-in fastener to interlock with other Type 40 switches to facilitate gang mounting side by side. Data sheet fully describes the switch with illustrations, dimensional line drawing and ordering information. Licon Div., Illinois Tool Works, Inc., Chicago, Ill.

Circle No. 206 on Inquiry Card

Zener Diodes

A silicon zener diode reference chart lists approximately 550 zener diode types with dissipation ratings ranging from 500 milliwatts to 50 watts and zener voltages from 6.8 volts to 200 volts. Eight different case styles or enclosures are illustrated in addition to outline drawings and mechanical specifications for each. National Transistor, a sub. of ITT, Lawrence, Mass.

Circle No. 200 on Inquiry Card

Tubular Capacitors

Technical data is given on miniature Type PTT capacitors that were designed specifically for transistor circuitry and miniaturized assemblies. Capacity ratings of the electrolytic tubular capacitors are listed with physical dimensions and catalog numbers for each voltage rating available from 3 volts to 50 volts. Typical curves of capacitance and equivalent series resistance with temperature are also included, together with typical curves of impedance versus frequency at 25C. Despite their size, they are capable of handling full sized loads within an operating temperature range of —30C to +65C. Plastic case provides excellent protection against humidity to assure maximum capacitor life. Aerovox Corp., New Bedford, Mass.

Circle No. 145 on Inquiry Card

Memory Core Selector

For selecting appropriate cores for specific memory applications, a handy selector chart-card is arranged to allow the designer to locate easily cores which fall into particular performance categories determined by his design parameters. Detailed data on those cores of interest are readily available on the reverse side of the chart. Included in the selector are a comprehensive listing of many of the company's core types and their characteristics, as well as a cross-reference index of various other manufacturers' core types. For one of these Selector Charts, send your request to:

LOCKHEED ELECTRONICS CO.,
Avionics & Industrial Products Div.,
6201 East Randolph St.,
L. A. 22, Cal. 90022
Attention: Electronic Ceramics Dept.

Lighted Displays/Switches

A 24-page catalog covering lighted display and pushbutton switch devices has 57 new items. Included are low-force switch units which enable rapid keyboard-type operation, and display screens with up to four different colors, each color segment illuminated by an individual lamp. Center pages of the catalog are split to show how 38 pushbutton actuators and 24 different switch units can be combined to provide hundreds of control options. The split-page format, plus a handy ordering guide makes proper selection of modules quick and easy. The catalog also has detailed information on mounting, legend practices, display color schemes, and brightness values. Micro Switch, Division of Honeywell, Freeport, Ill.

Circle No. 132 on Inquiry Card

Thermistor Selector

Special kit contains three, 6-page, folders; one on "where to get thermistors", one on "what you need in thermistors", and one on "what to do with thermistors". Covering composition types B, D, J, E, F, G, and H, these brochures include complete specs, options available, and the complete range of applications on both disc and washer-type thermistors for military and commercial use. Over 200 standard items are available "off-the-shelf", with operating temperatures to +400C without leads; +500C with platimum leads: time constants to 0.4 seconds; high betas; initial resistances as low as 2 ohms; and ratios to 22.1. Thermonetics Inc., Canoga Park, Cal.

Circle No. 201 on Inquiry Card

"Systems" Computer

Recently-announced Model 420 "Systems" computer is described in a new bulletin which gives a detailed description of the computer's applications, specification, command list, and theory of operation, including a block diagram illustrating computer organization. Defined as a special-purpose digital computer designed for real-time data processing, the Model 420 provides up to 32,000 words of memory, up to eight input/output channels, and a 3.2 microsecond read/restore cycle time. Beckman Instruments, Fullerton, Cal.

Circle No. 147 on Inquiry Card

LITERATURE

Read Amplifier Cards

Read amplifier card contains two identical circuits, each having a transformer input driving a temperature-stabilized differential amplifier. The output of the differential amplifier is buffered by an emitter follower stage. In turn the first emitter follower is rc coupled to a first common emitter amplifier whose collector circuit contains a low-pass filter for rejection of high-frequency noise. A potentiometer at the base of the common emitter amplifier serves as a gain adjustment for the read amplifier. Primarily, the read amplifier is designed for use in systems employing the return-to-bias recording method. However, it can be utilized in systems using phase modulation providing no voltage dwell occurs in the playback at or near crossover. Designed to meet two specific applications; clock, index, and register inputs, and general storage inputs from a read-write buss – the read amplifier is one of a family of curcuit modules. Bryant Computer Products, Walled Lake, Mich.

Circle No. 142 on Inquiry Card

Teflon Terminals

A 40-page catalog covers a complete line of "Press-Fit" Teflon insulated terminals and includes comprehensive guides for selection and installation. Configurations include stand-offs, feed-thrus, bushings, test point jacks, taper pin receptacles, probes and plugs, transistor holders and sockets – and others designed to specific customer requirements. Sealectro Corp., Mamaroneck, N.Y.

Circle No. 128 on Inquiry Card

Core Memories

Design economies resulting in improved noise rejection and a more attractive physical appearance of a new series of magnetic core memories are described in a 4-page brochure. Complete descriptions, applications, characteristics, and specifications are included with a list of complementary data handling equipment. Electronic Eng. Co. of Cal., Santa Ana, Cal.

Circle No. 126 on Inquiry Card

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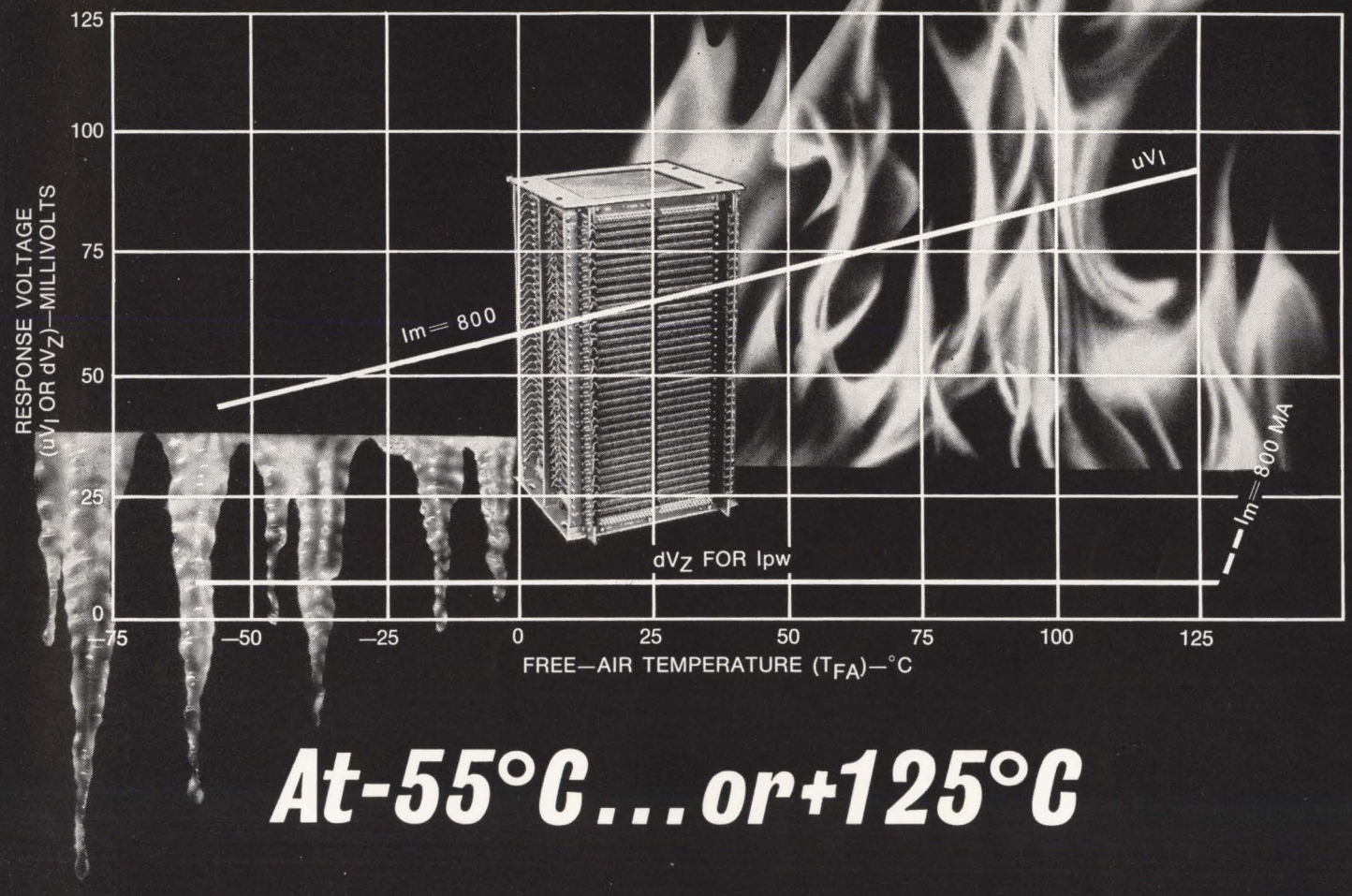
NOW YOU CAN ELIMINATE TEMPERATURE CONTROLS FROM FERRITE MEMORIES...

EVEN FROM 2 μSEC HIGH-SPEED SYSTEMS



At-55°C...or+125°C

New RCA Wide-Temperature-Range Memory Cores Switch in ½ Microsecond

RCA high-speed, wide-temperature-range ferrite memory planes and stacks operate without temperature controls or current compensation over any 100 centigrade degree range between the limits of −55°C and +125°C.

Memory planes and stacks using RCA 0146M5 ferrite cores provide high-speed operation over the full temperature range with less than 480 ma partial-write current. At full driving current of 800 ma, these temperature-stable cores have a switching time of approximately 0.5 μsec, making them particularly suitable for memory systems with 2 μsec operating cycles.

RCA wide-temperature-range cores are also available for low-drive operation at slower speeds.

The full line of RCA cores, planes and stacks offers a wide variety of types for coincident-current, word-address, and switching applications at speeds to 250 nsec. Complete RCA memory systems range in size from 256 words x 8 bits to 16,384 words x 20 bits and offer speeds to 250 nsec.

Whatever your memory requirements, call your RCA Representative for a coordinated application service for RCA memory components and devices, ranging from cores and transistors to complete memory systems. For technical data, write: RCA Electronic Components and Devices, Memory Products Operation, Section F-ZB-4, 64 "A" Street, Needham Heights 94, Mass.

RCA **The Most Trusted Name in Electronics**

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CIRCLE NO. 33 ON INQUIRY CARD

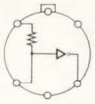
F/P-1664-A

Off the shelf

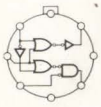
18 MICROLOGIC ELEMENTS

Two versatile families of silicon Planar epitaxial microcircuits

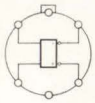
MICROLOGIC μL™



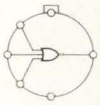
BUFFER (900) A low impedance inverting driver circuit.



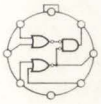
COUNTER ADAPTER (901) Provides gated, non-inverted complementary outputs from a single-valued input.



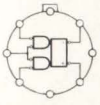
FLIP-FLOP (902) A bistable flip-flop storage unit.



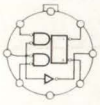
THREE-INPUT GATE (903) A three-input NAND /NOR circuit.



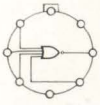
HALF ADDER (904) A two-level AND/OR gate suited for use as a complete half-adder, an exclusive OR gate or any similar logic function.



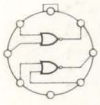
HALF-SHIFT REGISTER (905) A gated input storage element with inverter.



HALF-SHIFT REGISTER (906) A gated input storage element without inverter (reduces power dissipation).

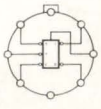


FOUR-INPUT GATE (907) A four-input NAND/ NOR circuit.



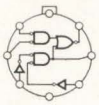
DUAL TWO-INPUT GATE (914) Dual NAND/ NOR gates capable of forming a flip-flop, noninverting gate, or gate plus inverter.

DUAL THREE-INPUT GATE (915) A dual combination of three-input circuits, one of three similar basic NAND/NOR gates.

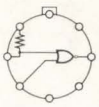


J-K FLIP-FLOP (916) A complete, general purpose, storage element suitable for use in shift registers, counters, or any type of control function.

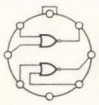
MILLIWATT MICROLOGIC MWμL™



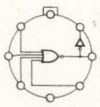
MODULO 2 ADDER (908) Generates the Mod. 2 addition or exclusive OR function. Average power dissipation: 10 mW.



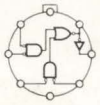
GATED BUFFER (909) A low impedance inverting driver circuit. Used typically as a line driver, in multivibrators, or for pulse differentiation. Average power dissipation: 10 mW @ 50% duty cycle.



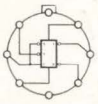
DOUBLE GATE (910) Used as a pair of NOR gates R-S Flip-Flop, pair of inverters, or double inverter. Average power dissipation: 4 mW.



4-INPUT GATE (911) Used as an OR gate by applying true inputs. Average power dissipation: 4 mW.



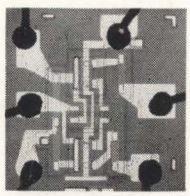
HALF ADDER (912) A multipurpose combination of three basic RTL circuits for a complete half adder or an exclusive OR gate. Average power diss: 8 mW.



TYPE D FLIP-FLOP (913) This element is a gated Flip-Flop for use as a binary in registers and counters. Average power dissipation: 12 mW.

GATE EXPANDER (921) A dual 2 input gate without node resistors, to be used when increased fan-in is required.

Logic symbols drawn in accordance with Military Standard 806B.



	μLogic*	MWμLogic*
tpd	15 ns typ	40 ns typ
Pdiss	15mW/node	2mW/node
Fan-in	3	4
Fan-out	5	4
TA	−55° to 125°C.	

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