COMPUTER DESIGN

THE MAGAZINE OF MODERN DIGITAL ELECTRONICS

MARCH 1967

DELAY EQUALIZATION IN DATA COMMUNICATIONS

LOGIC MINIMIZATION BEYOND THE KARNAUGH MAP

ONLY HONEYWELL OFFERS
TOMORROW'S BREED OF I/C COMPUTER...

...AND THEY'RE BEING DELIVERED TODAY!

I/C construction . . . 16-bit word . . . 960 nano-second speeds . . . strong software support — unprecedented computer capability in a low cost compact. And these are only some of the features that put 3C's two new μ-COMP machines in tomorrow's computer class today.

THE DDP-516, at $25,000, is the most advanced I/C 16-bit computer now available. Both hardware and software are already operational. Hardware includes high-speed multiply and divide (optional), a 4096-word memory (expandable to 32K), 960 nsec cycle time. The command repertoire includes 72 instructions with such capabilities as byte manipulation, skip-branch conditioning, and extensive memory reference and control.

250 field proven programs are available with every DDP-516 . . . including ASA FORTRAN IV compiler, selectable one- or two-pass assembler with a unique DESECTORIZING loader that lets you ignore memory restrictions. DDP-516 delivery: as few as 90-days.

THE DDP-416, at $16,900, was engineered for a price/performance ratio that can't be beat by any other on-line real-time computer. Hardware features include a 4096-word memory (expandable to 16K), 960 nsec cycle time, 1.92 μsecs add, with indirect addressing.

A 30-command repertoire, priority interrupt and power failure protection are standard. Both the DDP-516 and the DDP-416 may be mounted in standard 19" racks. Best of all, if you decide to get the more powerful DDP-516 in the future, you can continue to use your DDP-416 programs because of direct compatibility. DDP-416 delivery: second quarter of 1967.

Write today for information on both μ-COMP computers. You can't go wrong with either one. Honeywell, Computer Control Division, Old Connecticut Path, Framingham, Massachusetts.

Honeywell

3C COMPUTER CONTROL DIVISION

CIRCLE NO. 1 ON INQUIRY CARD

MARCH 1967 • VOLUME 6 • NUMBER 3

COMPUTER DESIGN

FOR ENGINEERING PERSONNEL RESPONSIBLE FOR THE DESIGN & APPLICATION OF DIGITAL CIRCUITS, EQUIPMENT, AND SYSTEMS IN COMPUTING, DATA PROCESSING, CONTROL AND COMMUNICATIONS.

Editorial & Executive Offices
Professional Bldg.
Baker Ave. • W. Concord Mass.
Tel. 369-6660

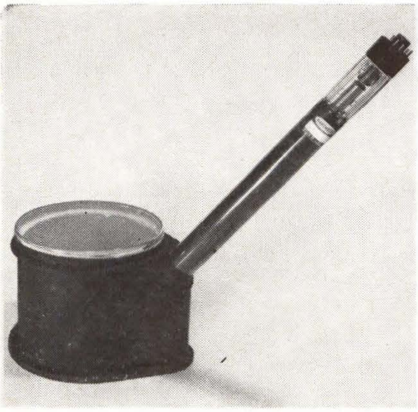
Computer Design is published monthly. Copyright 1967 by Computer Design Publishing Corporation. Accepted as controlled circulation publication at Post Office at Boston, Massachusetts. No material may be reprinted without permission. Postmaster: CHANGE OF ADDRESS — FORM 3579 to be sent to Computer Design, Circulation Dept., P. O. Box A, Winchester, Mass. 01890. Subscription rate to non-qualified subscribers is $15.00 per year; $1.50 per issue. Subscription rate to all foreign subscribers is $25.00 per year; $2.50 per copy.

BPA

Circulation over 32,000

FEATURES

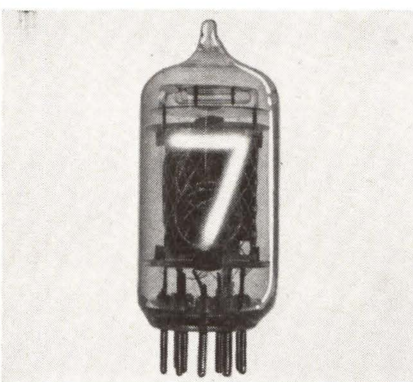
DEPARTMENTS



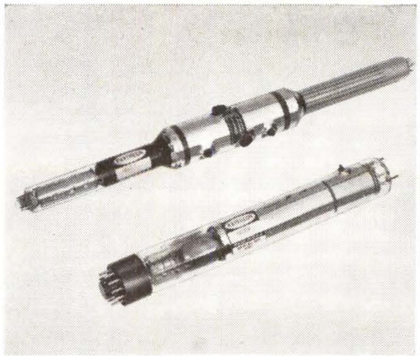
New Raytheon Projectoray* Tube produces more than double the light output of standard projection-type cathode ray tubes. The tube's light output is 30,000 foot lamberts, which results in a light level of 15-foot lamberts on a 3' x 4' lenticular screen.

The tube's expected minimum operating life is 500 hours — 20 times the life of a standard projection tube.

The Projectoray's high light output and long life are due to its novel design. The design incorporates liquid cooling of the phosphor backplate. This allows the phosphor to be energized with a very intense electron beam. At high beam levels, very high peak light output is obtained. The light image is projected through a 5" optical window in the face of the tube. The electron gun is set at an angle to the phosphor and the deflection system compensates for keystone effects.



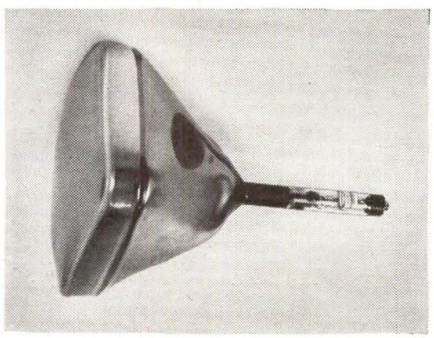
Datavue* Side-View Tubes. New Type CK8650, with numerals close to the front, permits wide-angle viewing. These side-view, in-line visual readout tubes display single numerals 0 through 9 or preselected symbols such as + and − signs. Their 5/8"-high characters are easily read from a distance of 30 feet. Less than $5 each in 500 lots, they also cost less to use because the bezel and filter assembly can be eliminated and because their mating sockets are inexpensive.



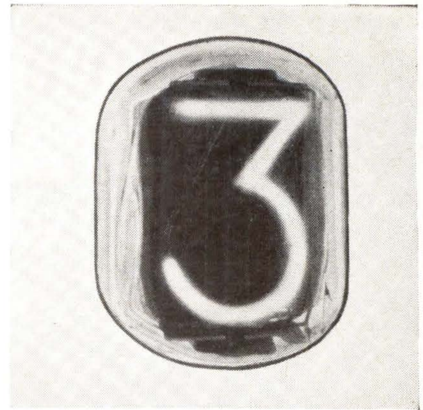
Recording Storage Tubes. The miniature tubes shown here are Raytheon's single-gun (CK1516) and dual-gun (CK1519). They provide high resolution, long storage, and fast erase capability.

Raytheon electronic input-output storage devices feature the above capabilities and immediate readout. Information can be written and stored by sequential techniques or by random-access writing. Complete, gradual or selective erasure is possible.

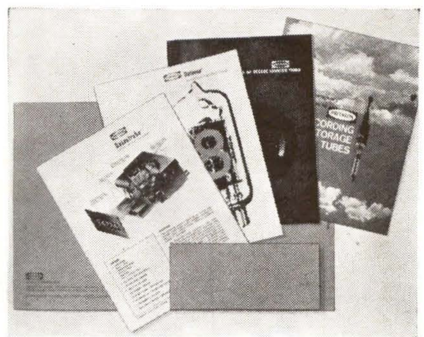
Raytheon storage tubes are readily available for applications in radar scan conversion, slow-down video, signal processing, signal enhancement, time delay, and stop motion.



Dataray* Cathode Ray Tubes. Raytheon makes a wide range of industrial CRTs —including special types—in screen sizes from 7" to 24". Electrostatic, magnetic, and combination deflection types are available for writing alphanumeric characters while raster scanning. All standard phosphors are available and specific design requirements can be met. Combination deflection or "diddle plate" types include CK1395P (24" rectangular tube), CK1400P (21" rectangular), and CK1406P (17" rectangular).



Datavue* End-View Tubes. These tubes are easily read in high ambient light — do not wash out like other displays. Erroneous readings due to segment failure do **not** occur because the characters are fully formed. Raytheon Datavue End-View Tubes fit existing sockets and conform to EIA ratings. Models include round (CK8421) and rectangular (CK8422). Ultra-long-life types are designed for 200,000 hours or more of dynamic operation.



Send Reader Service Card for literature on the:

Symbolray CRT	4
Projectoray CRT	5
Datavue Indicator Tubes	6
Recording Storage Tubes	7
Dataray CRTs	8

Or call your Raytheon regional sales office. Or write to *Raytheon Company, Components Division, Quincy, Mass 02169.*

*Trademark of Raytheon Company

RAYTHEON

Industrial Components Operation—A single source for Circuit Modules/Control Knobs/Display Devices/Filters/Hybrid Thick-Film Circuits/Industrial Tubes/Optoelectronic Devices/Panel Hardware

← **Circle No. 9 on Inquiry Card**

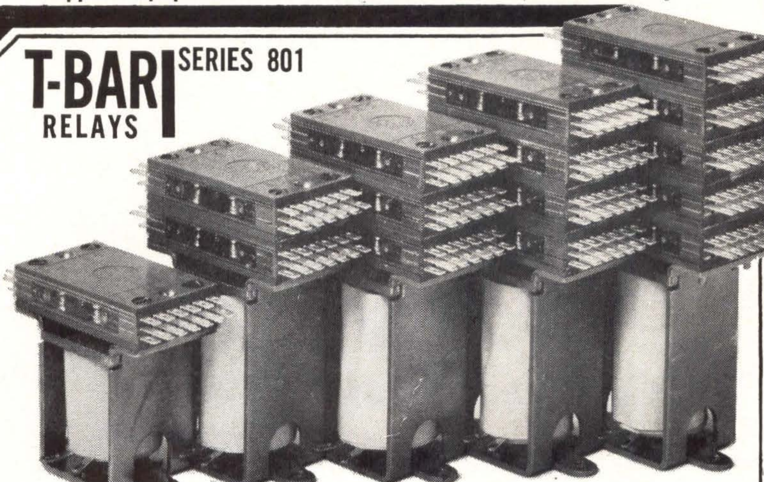
the simplest solution to switching problems...

from 12 PDT to 144 PDT:

"off-the-shelf" T·BARS®!

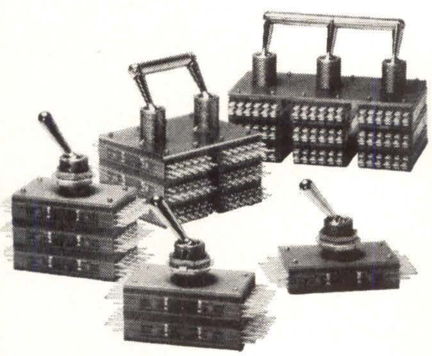
T-BARS are for switching in computers . . . automatic testers . . . communications . . . process controls . . . telemetry . . . ground support equipment . . . aircraft . . . in fact, almost everywhere!

T-BAR SERIES 801 RELAYS



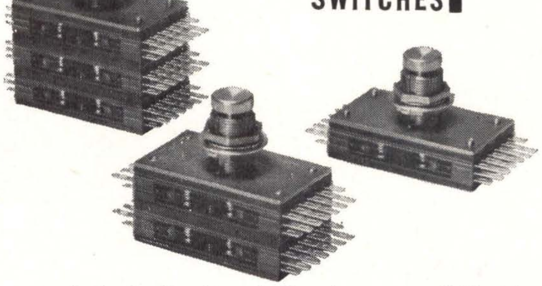
12 Poles 1 Wafer Relay | 24 Poles 2 Wafer Relays | 36 Poles 3 Wafer Relays | 48 Poles 4 Wafer Relays | 60 Poles Single Throw 5 Wafer Relays

BAT HANDLE T-BAR SERIES 802 SWITCHES



Switch up to 144 PDT . . . in less space! Available in Single, Double and Triple . . . as well as Ganged Toggles for controlling 48, 72, 108 poles . . . even more!

MOMENTARY PUSH BUTTON T-BAR SERIES 803 SWITCHES



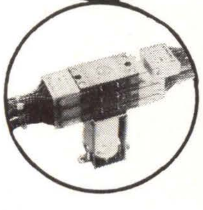
Available in 12, 24 and 36 poles . . . reliable high density multipole switches . . .

low component cost

36 PDT—$21.78 ea. in lots of 100
48 PST—$23.54 ea. in lots of 100

mounting ease

2 simple screws . . . can mount on panel in any orientation . . . eliminates chassis.



wiring economy

Simple crimp snap-on contacts fit into single block connectors for pre-harnessing.

Now available "off-the-shelf" in your immediate area from:

CALIFORNIA
Newark Electronics
4747 W. Century Blvd.
Inglewood(213)678-0441
Fisher Switches, Inc.
3199 Park Boulevard
Palo Alto(415)321-4080

CONNECTICUT
Westconn Electronics
195 Colorado Avenue
Bridgeport(203)367-7747
Cramer Electronics
60 Connolly Parkway
Hamden (203) 288-7771
Westchester Electronics
181 Stillwater Road
Stamford (203) 348-7361

FLORIDA
Electronic Equip. Co.
2701 N. W. 42nd Ave.
Miami
(305) 635-0421
Electronic Equip. Co.
Orlando
(305) 644-4833

ILLINOIS
Allied Electronics
100 No. Western Ave.
Chi. (312) 829-9100

ILLINOIS (Cont'd)
Newark Elec. Corp.
500 No. Pulaski Rd.
Chi. (312) 638-4411

MASSACHUSETTS
Cramer Electronics
817 Boylston Street
Boston (617) 267-4700

MISSOURI
Texas Instr. Supply Co.
2828 McGee Street
Kan. City (815)421-5670

NEW YORK
Westchester Electronics
602-610 Mamaroneck
Ave. White Plains
(914) 949-2400

OKLAHOMA
Texas Instr. Supply Co.
1124 East Fourth St.
Tulsa (918) 583-8121

TEXAS
Texas Instr. Supply Co.
6000 Denton Drive
Dallas (214) 357-6121
Busacker Elec. Equip.
1216 West Clay Street
Houston(718)526-4661

For additional information on these and other T-Bar items refer to Distributor Catalogs, "eem," "R/M" or write to E-C-I for Bulletin TB 801-3.

MANUFACTURED BY:

electronic controls, inc.
T-Bar Switch/Relay Div. • Danbury Road, Wilton, Conn.
phone (203) 762-8351
See us at IEEE Booth 3B52

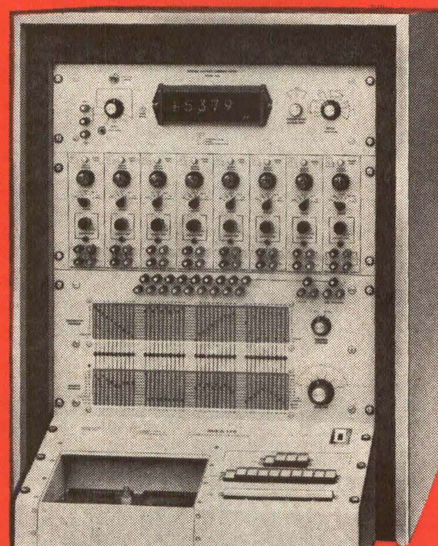
CIRCLE NO. 16 ON INQUIRY CARD

Circle No. 17 on Inquiry Card →

NEW

semi-automatic integrated circuit analyzer

MICA 150



COMPUTER TEST CORPORATION

Now the integrated circuit user can get all the flexibility and performance of an expensive, large scale IC test system in an accurate and reliable DC bench top analyzer.

The new MICA-150 Modular Integrated Circuit Analyzer tests all IC configurations of up to 40 pins with unique programming, fast pushbutton sequencing and built-in DVM readout.

Fast, Versatile Programming Two independent 10x40 crossbar switches and rapid pushbutton sequencing provide up to 40 tests on a single device without re-programming. For example, it's now quick and easy to check a 10 pin device using four completely different test programs without resetting any switches to advance the test from pin-to-pin or program-to-program. Additional flexibility allows the built-in DVM to measure current on one pin of the device and voltage on another—all pre-programmed.

Universal Test Adapters Through use of universal test adapters, the MICA-150 is designed to check ICs according to the number of pins of a particular package, not device or circuit type. Adapters are available for diode, transistor, TO-5, flat-pack, dual in-line and other package configurations, and can also be provided for Kelvin connections.

Accurate Digital Readout Specifically designed for the MICA-150 analyzer, the built-in Digital Volt/Ammeter has a conservatively rated readout accuracy of 0.1% with a four digit display. Other features include automatic ranging and polarity selection, self-calibration, automatic voltage or current readout selection. Measures currents as low as 1 nanoamp, voltages to 1 mv.

Modular Design Modular construction allows users to select an economical, customized tester without obsolescence problems. Maximum capacity of eight function generators permits later expansion, including modules for AC and pulse testing, without additional modifications.

Variable Soak Time Marginal device operation can be easily detected through use of an adjustable test time control which provides a period for thermal stabilization prior to measurement. A continuous position on the control allows parameters to be varied while observing results.

Precision, Wide Range Power Supplies Highly precise supplies utilize multi-turn calibrated potentiometer controls with high resolution and repeatability. Constant current supplies are continuously variable from 0-100 ma with voltage compliance adjustable to 100v. Constant voltage supplies are variable from 0-100v with automatic current limiting to 100 ma to provide device protection.

QUICK ACTION REPLY

Detailed technical literature on the MICA-150 will be mailed immediately upon receipt of this request.

Attn.: A. Norman Into, Marketing Manager
Computer Test Corporation, Three Computer Drive
Cherry Hill, N.J. 08034 • Phone: (609) 424-2400

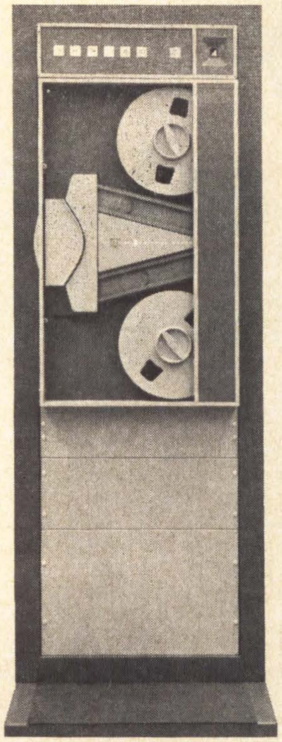
Name__________

Company__________

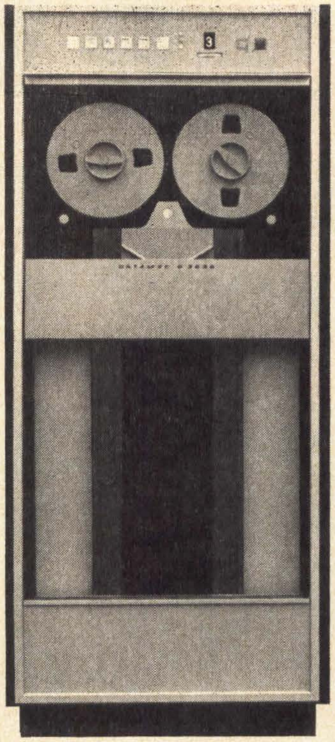
Address__________

City__________ State_____ Zip_____

How good are Datamec Tape Units?



Datamec D 2020



Datamec D 3030

Ask any of the people who build or use these computer systems.*

1. **Digitronics Corporation**
   System 600 Dial-o-verter
2. **Electro-Mechanical Research**
   EMR 6050 Computer System
3. **Scientific Control Corporation**
   SCC-650 Computer System
4. **Stromberg-Carlson Data Products Div.**
   S-C 4400 System
5. **Photon, Inc.**
   713 Textmaster Phototypesetter
6. **Gerber Scientific Instrument Co.**
   Series 2000 Control

**Or ask us for our complete customer list. It's long.*

Perhaps you, too, have a program that would profit from **low cost / high reliability** in computer tape handling. Check with the company that stresses service to its customers. Write us at 690 Middlefield Road, Mountain View, California 94041. Better yet, call your nearby Hewlett-Packard sales office.

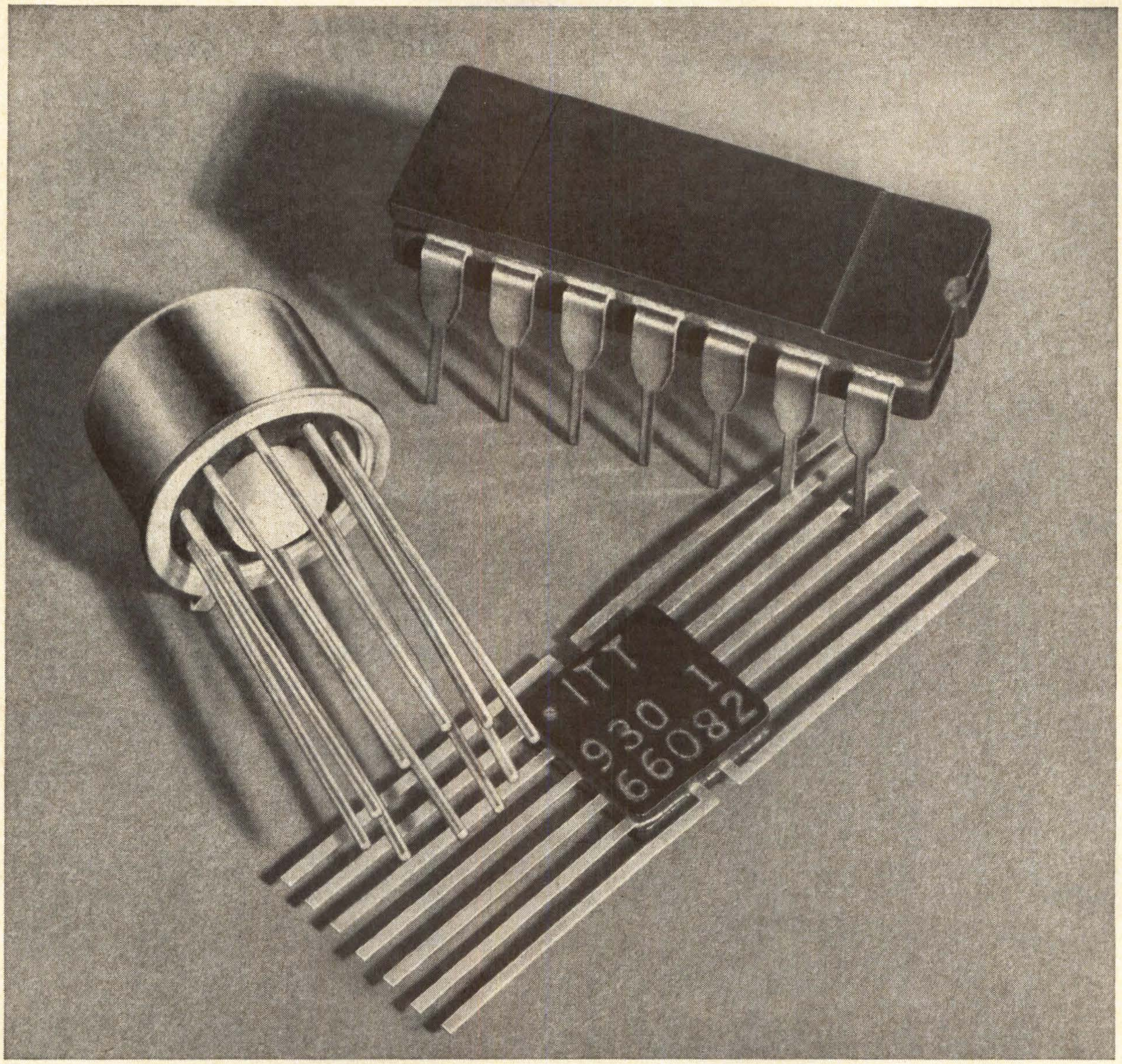
HEWLETT PACKARD hp DATAMEC DIVISION

an extra measure of dependability

42703

CIRCLE NO. 18 ON INQUIRY CARD

The Predictables.



100% DC and dynamic testing verifies the performance of every circuit in ITT's full line of Series 930 DTL

When your order of ITT Series 930 DTL arrives, you can have absolute confidence in its performance. First of all, every circuit gets full DC and dynamic testing at 25°C, plus temperature cycling, centrifuge, and fine leak tests. Then there's 1% AQL testing at −55°C, +25°C and +125°C for 15 DC parameters and at +25°C for 2 dynamic parameters. If circuits flunk, we just don't ship them.

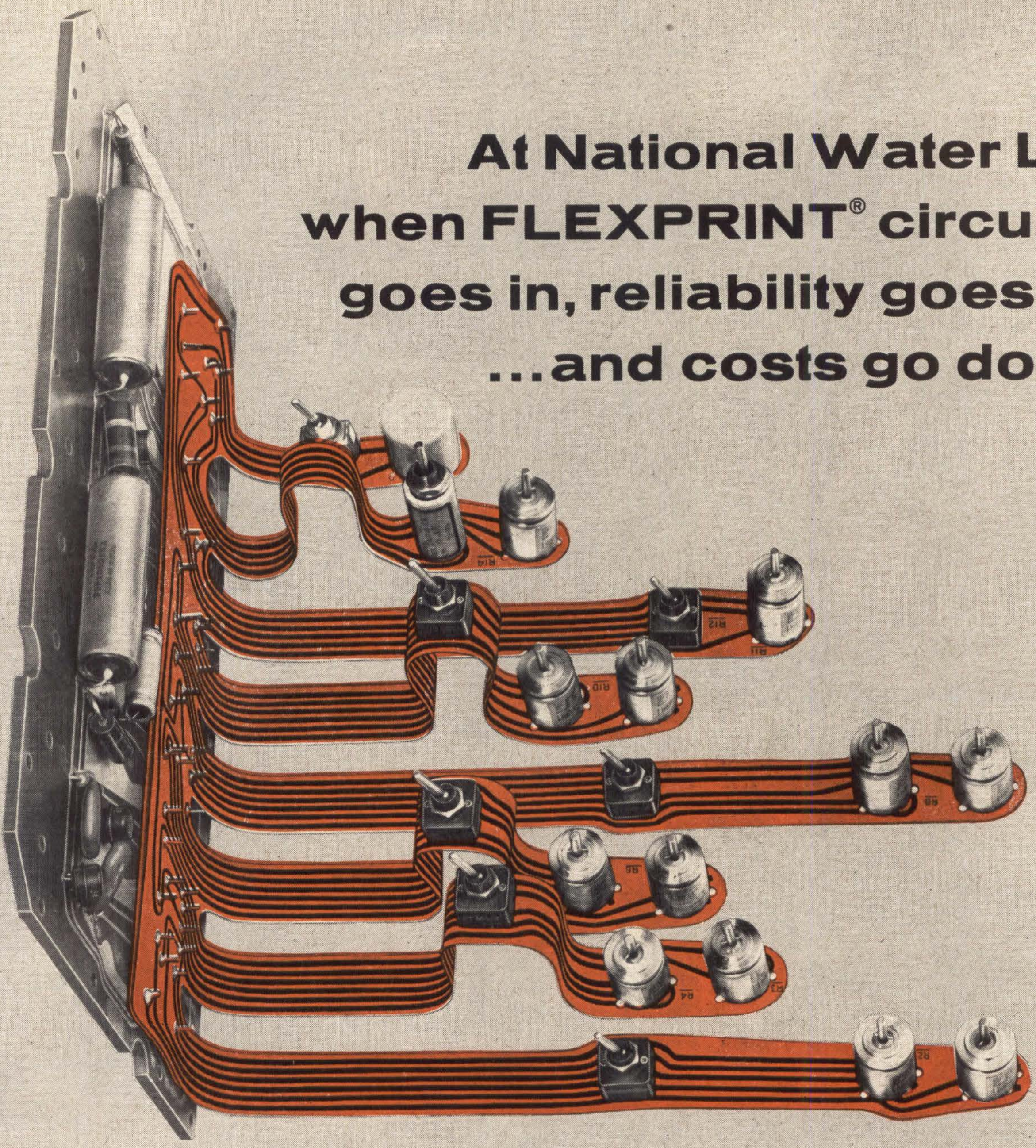
ITT's Series 930 "predictables" come in 15 circuit functions and three package styles. If you're tired of rejecting and returning DTL, try ordering it from ITT. It's available off-the-shelf from your distributor or direct from the factory through your ITT representative. ITT Semiconductors is a Division of International Telephone & Telegraph Corporation.

integrated circuits ITT

FACTORIES IN WEST PALM BEACH, FLORIDA; PALO ALTO, CALIFORNIA; LAWRENCE, MASSACHUSETTS; HARLOW AND FOOTSCRAY, ENGLAND; FREIBURG AND NURENBERG, GERMANY

CIRCLE NO. 19 ON INQUIRY CARD

SOLUTIONS TO INTERCONNECTION PROBLEMS



At National Water Lift, when FLEXPRINT® circuitry goes in, reliability goes up ...and costs go down

With FLEXPRINT circuitry, National Water Lift gets increased reliability *plus* a 20% saving on installed wiring costs on every STOW weight-and-balance computer produced for the C-130 transport.

Because the FLEXPRINT circuit is made of strong, flexible KAPTON† film, it withstands vibration better than ordinary wire . . . even under extreme conditions. And because it is custom-engineered for the National Water Lift application, wiring errors and troubleshooting are virtually eliminated. Greater reliability is built right into the entire circuit system.

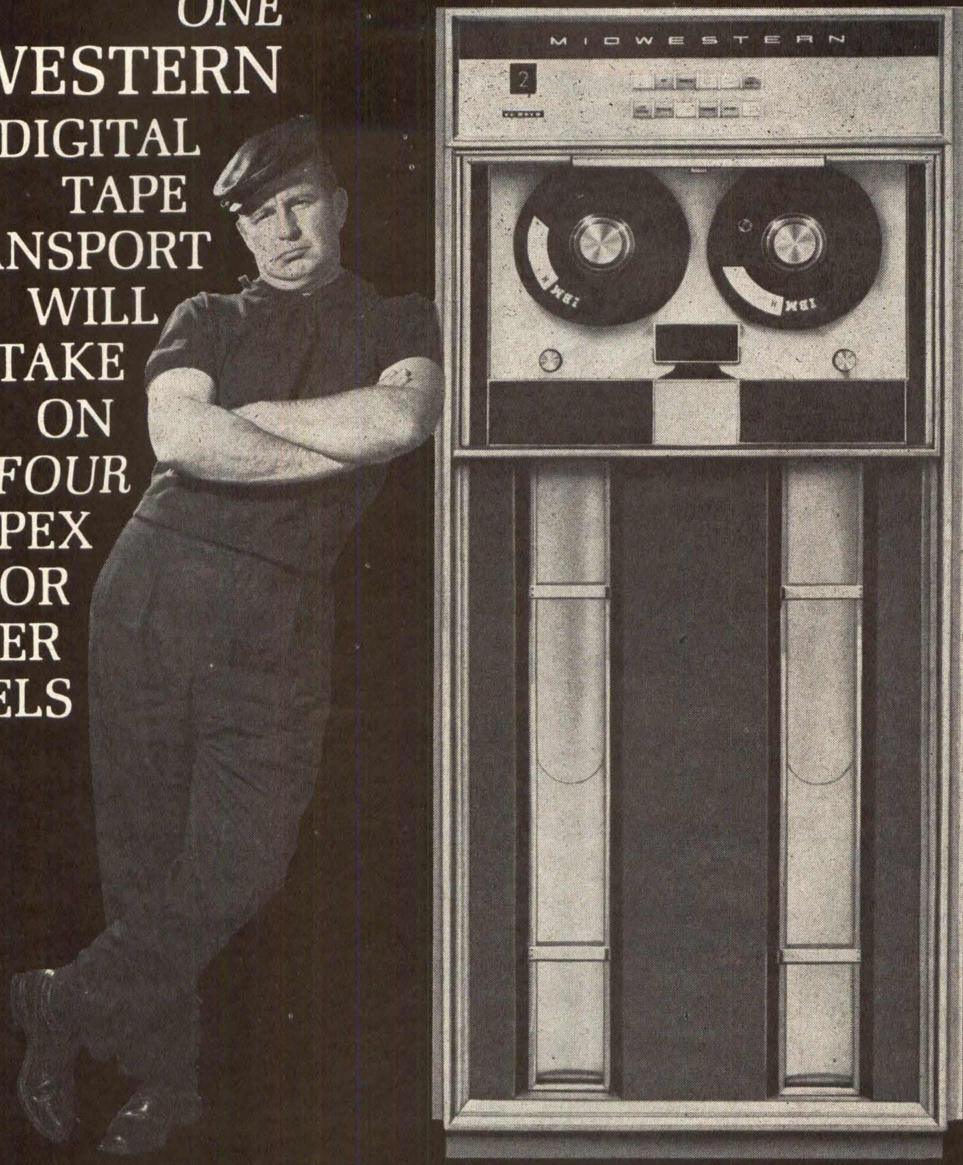
Production economies, too, are a built-in feature of the FLEXPRINT circuitry. The STOW computer circuit lies flat for easy insertion of 21 individual components — then folds neatly into the exact space allowed in the package. Assembly time, quality control and rework are reduced to a minimum, and the completed assembly always fits the package.

If you have a similar assembly or packaging problem, call a Sanders FLEXPRINT expert. Our representatives cover the country. Ask them about FLEXPRINT circuitry, FLEXMAX flexible multilayer circuitry, and INTRAMAX* multilayer hardboard. For detailed information, call or write Sanders Associates, Inc., FLEXPRINT Products Division, Grenier Field, Manchester, New Hampshire 03103. Phone: (603) 627-3811.

SANDERS ASSOCIATES, INC.*
FLEXPRINT PRODUCTS DIVISION
Creating New Directions in Electronics

*Trademark of Sanders Associates, Inc. †Trademark of DuPont

ONE
MIDWESTERN DIGITAL TAPE TRANSPORT WILL TAKE ON *FOUR* AMPEX OR POTTER MODELS !



One Midwestern Model M4000 digital tape transport is as versatile as other manufacturers' complete line of four models.

The M4000 offers you complete selections of operating speeds—from a low of 25 ips and 5 kc data rates to a high of 150 ips and 120 kc data rates. There are no servo or program restrictions at either the highest or lowest data transfer rates, and the M4000 is completely compatible with both 7 and 9 track recording formats.

INVESTIGATE MIDWESTERN INSTRUMENTS' M4000 DIGITAL TAPE TRANSPORT SYSTEM!

You'll discover it covers the complete range from low to high performance in tape speed, recording density and data transfer rates. The M4000 provides a total solution to digital tape storage requirements. And, it is fully flexible with either conventional solid state or integrated circuitry.

FOR A BLOW BY BLOW DESCRIPTION OF THE **M4000** CONTACT YOUR NEAREST MIDWESTERN REPRESENTATIVE.

MIDWESTERN INSTRUMENTS / TELEX

6422 E. 41st STREET • TULSA, OKLAHOMA 74135
PHONE (918) 627-1111 • TWX (918) 627-6030 • TELEX 049-589

CIRCLE NO. 21 ON INQUIRY CARD

← Circle No. 20 on Inquiry Card

Tantalum's best for the big brains. It figures.

The all-new KEMET W-Series Solid Tantalum capacitor. The smallest molded solid tantalum available... in an ultra-thin profile square case for peak form factor ... standard card mounting for instant plug-in—all at a new low price.

It's an ideal by-pass or coupling capacitor for computers ... color and portable TV... quality electronic instruments. It features ultra-low leakage and is, effectively, air cooled. Its case is only 0.345" x 0.228" x 0.105".

Want a hard-working, stackable, tiny tantalum capacitor? That's the new KEMET W-Series. See your representative or mail the coupon.

Capacitance Range: KEMET W-Series

Voltage (85°C)	Min./Max. (Microfarads)
6	0.082/22
10	0.082/15
15	0.082/8.2
20	0.082/6.8
25	0.082/4.7
35	0.082/2.7
50	0.082/1.5

Clip, fill in name and title, attach to letterhead.

Union Carbide Corporation
Electronics Division
Dept. CD-3
270 Park Avenue
New York 10017

UNION CARBIDE ELECTRONICS

Please send details on "W" Series KEMET Solid Tantalum Capacitors

Name____________________

Title____________________

KEMET is a registered trade mark of Union Carbide Corporation.

REGIONAL SALES OFFICES. New England: T. J. Roper, 300 First Ave., Needham Heights, Mass. Phone: 617-444-5400. **Mid-Atlantic:** R. H. Robecki, 1341 Hamburg Turnpike, Wayne, New Jersey 07472. Phone: 201-696-2710. **Mid-West and South:** K. S. Collart, P. O. Box 6087, Cleveland, Ohio 44101. Phone: 216-221-0600. C. F. Fields, 2 Talcott Road, Park Ridge, Ill. 60068. Phone: 312-825-8189. **West Coast:** D. Purcell, 701 East Whittier Boulevard, Whittier, California 90605. Phone: 213-698-8077. C. E. Volpe, 2680 Bay Shore Frontage Road, Mountain View, California 94041. Phone: 415-969-9390. **For Overseas Inquiries contact:** J. G. Egan, 1341 Hamburg Turnpike, Wayne, New Jersey 07472. Phone: 201-696-2710.

CIRCLE NO. 22 ON INQUIRY CARD

Circle No. 23 on Inquiry Card

have you noticed how everybody's just introducing big, fast, core-memory systems that we've been delivering for more than a year?

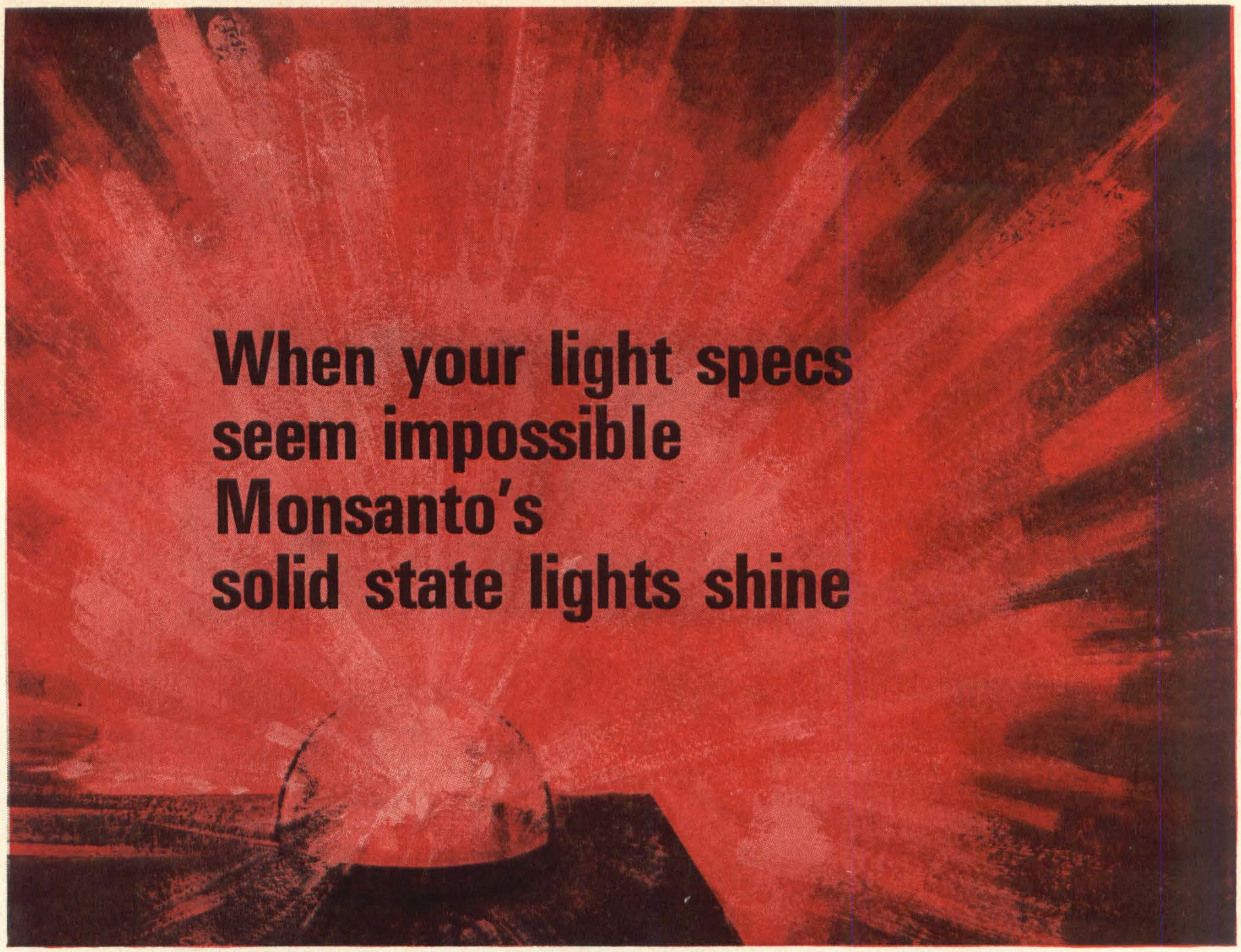
When we first introduced our NANOMEMORY™ 900 at the 1964 Fall Joint Computer Conference, we claimed an access time of 350 nanoseconds and a memory capacity of 16,384 words of 84 bits. A little later we developed the NANOMEMORY 650. Same capacity *but with* an access time of 300 nanoseconds.

Soon after we started shipping, reports came in calling our claims, if anything, too conservative. Operating margins were indeed wider. And with the stack connections reduced by 80%, the reliability gave maintenance managers no end of pleasure.

But more gratifying than the compliments were the re-orders. Of the many systems being assembled on the floor right now, 80% are engaged. If you want to stay ahead of *your* competition, call or write us about the 20% that are still unattached. Ask for Litpak 6C.

EM electronic memories

12621 Chadron Avenue, Hawthorne, California 90250
Telephone (213) 772-5201



Now you can get a new line of visible and infrared emitting diodes that feature long life, maximum reliability and fast switching speed . . . at low cost.

These rugged light sources from Monsanto offer you design opportunities never before available in their price range. Just look at the following specifications and unit costs and see why they fit into your design for profit.

MVE-100 Visible Light Emitter. The MVE-100 gallium arsenide phosphide diode is suitable for use as an instrument signal light, panel indicator and for many computer uses. Price ranges from $14.50 each in lots of one to nine, to $8.00 each in lots of 1,000.

MVE-101A Visible Light Emitter. The MVE-101A gallium arsenide phosphide diode is packaged in a smaller coaxial package allowing high packing density for those applications where space is critical. Use the MVE-101A for film annotating, reticle illuminations and as indicators. Price ranges from $16.50 each in lots of one to nine, to $8.00 each in lots of 1,000.

MVL-150 Visible Laser. The MVL-150 is a gallium arsenide phosphide semiconductor laser which is available with emission at any desirable wave length between 6,500 A and 8,300 A. This laser is designed for operation at 77 K. Price ranges from $19.50 each in lots of one to nine, to $13.00 each in lots of 1,000.

MIE-200 Infrared Emitter. An infrared radiation source consisting of a gallium arsenide mesa diode. It matches efficiency with silicon detectors, providing enough radiated power to work in common mode isolation, card reading, and chopping applications. Price ranges from $9.85 each in lots of one to nine, to $6.00 each in lots of 1,000.

MVA-300A Visible Light Emitter Array. The MVA-300A 5x7 Array is a solid state read-out made with 35 MVE-101A diodes mounted on a metal heat sink. The display is used for visual read-out and film annotation applications. Price $495.00 each.

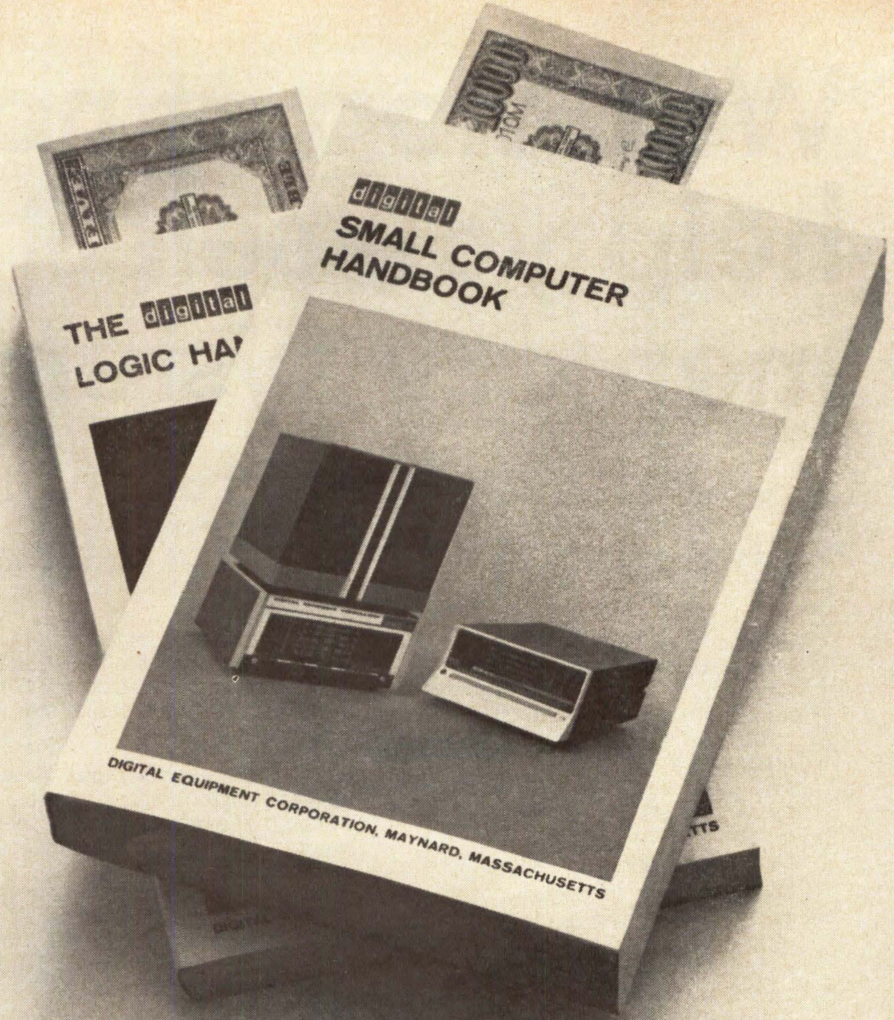
For more information on low-cost Monsanto light sources, call (314) OXford 4-2136 or write: Monsanto Company, 800 N. Lindbergh Boulevard, St. Louis, Missouri 63166

Monsanto

ELECTRONICS

CIRCLE NO. 24 ON INQUIRY CARD

Circle No. 25 on Inquiry Card →



A post-graduate course in money-making

Some people think of Digital Equipment as a manufacturer of digital computers and modules for the university and scientific community exclusively. They're wrong.

Since the PDP-8/S was introduced in August of 1966, more than 300 such machines have been sold to be part of other people's money-making devices — blood analyzers, X-ray diffractometers, spectrum analyzers, batch controllers for cookie baking. One pipeline manufacturer ordered 25 PDP-8/S computers just to log data. (PDP-8/S is the world's first under-$10,000 computer.)

For bigger, faster problems, the bigger, faster PDP-8 has been incorporated into money-making automatic transistor check out equipment, petroleum controllers, thickness testers for rolled steel. (PDP-8 costs $18,000.) PDP-9 is bigger yet.

And modules. We sell more digital logic circuit modules to manufacturers who resell them as part of their instruments and systems than to all our university customers combined.

So we're very big in the universities. True.

But if you make instruments or systems (and particularly if you sell these instruments to the scientific disciplines) maybe you should discover us. Before we get too well known.

digital
COMPUTERS · MODULES

DIGITAL EQUIPMENT CORPORATION, Maynard, Massachusetts 01754. Telephone: (617) 897-8821 • Cambridge, Mass. • New Haven • Washington, D.C. • Parsippany, N.J. • Rochester, N.Y. • Philadelphia • Huntsville • Pittsburgh • Chicago • Denver • Ann Arbor • Houston • Los Angeles • Palo Alto • Seattle • Carleton Place and Toronto, Ont. • Reading, England • Paris, France • Munich and Cologne, Germany • Sydney and West Perth, Australia • Modules distributed also through Allied Radio

We'll stop at nothing to help you select the right memory system

...we'll even lend you one (with or without the applications engineer) for a free trial

We can help if you have no experience with core memories, but are designing industrial control systems that must handle and store data. To see how they can profit by the use of a low cost core memory, give us a call. We'll send an applications engineer around with the system best suited to your needs. He'll help you get it on line for evaluation.

We can help if you're familiar with core memories, but don't see how a standard off-the-shelf design could satisfy your requirements. Send us your block diagram. We'll study it and send you back a complete blueprint showing you how a general purpose core memory can be used as a versatile data-manipulating system capable of many more logic functions than storage. (We may even be able to eliminate some redundant functions required by less versatile storage techniques.)

We can help even if you're already using core storage, but aren't convinced that a mass produced memory can provide many of the control, access and operating mode functions formerly associated (usually one at a time) with custom design. Drop us a line. We'll lend you a small system for a 10-day free trial. See for yourself what it can do. If at the end of the trial period you can't bear to part with it, we'll work something out.

Our point—to prove that our line of catalog standards is broad enough to satisfy most data storage requirements and that we'll do almost anything to help you apply them to your system. Our FX-12 and FX-14 Series Systems are available in some 200 types. Sizes range from 128 words x 8 bits to 4K x 32, with cycle times from 4 to 8 microseconds. Prices start at $1,190. If you'd like to check details and specifications before we talk, write for Bulletins M6612 and M6614.

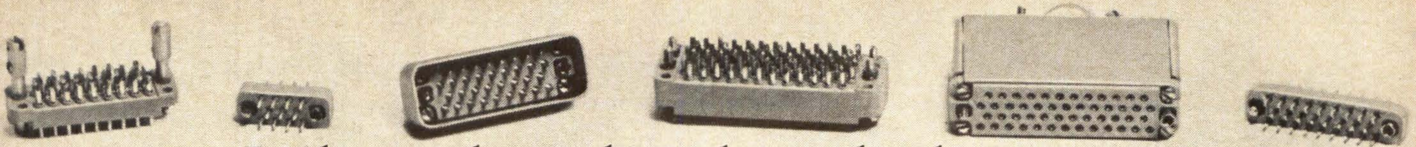
Ferroxcube
Systems Division Englewood, Colorado

FERROXCUBE CORPORATION OF AMERICA
Systems Division
5455 S. Valentia Way
Englewood, Colorado
303-771-2000

Boston	Chicago	Dallas	Los Angeles	Minneapolis	New York Area	Phoenix	Philadelphia
617-899-3110	312-261-7880	214-255-0441	213-837-1484	612-888-4681	201-267-5888	602-265-1792	215-927-6262

CIRCLE NO. 26 ON INQUIRY CARD

Circle No. 27 on Inquiry Card →

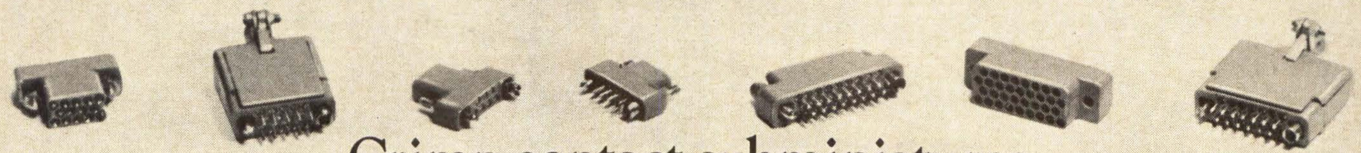


Lightweight rack and panel subminiatures

Series SRM, XSRM. For aircraft, instrumentation and portable equipment. Compact, lightweight rack and panel types. With accessories.

High current capacity subminiatures

Series JF, JFA. For television, radio and communications applications. Flat mounting. With accessories.

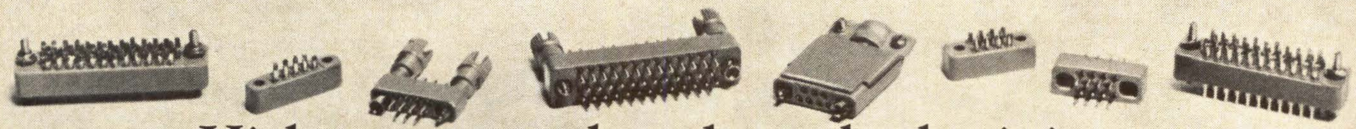


Crimp contact subminiatures

Series SREC. For aircraft, instrumentation and portable equipment. Compact, lightweight rack and panel types. With accessories.

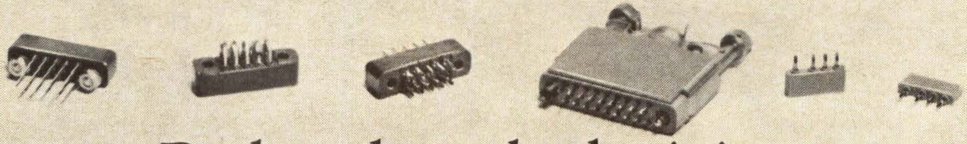
Printed circuit subminiatures

Series PC. For integrated thin film and semiconductor circuitry. With accessories.



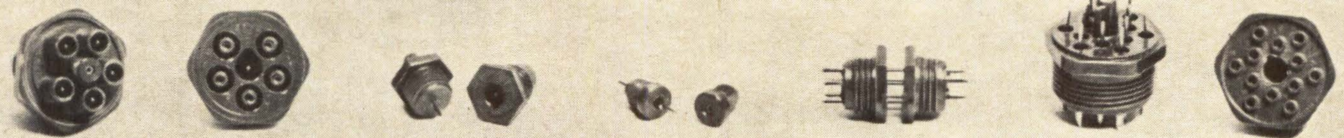
High current rack and panel subminiatures

Series SRE. For applications where current rating or voltage drop requirements dictate large wire size. Meet MIL C 8384. With accessories.



Rack and panel subminiatures

Series SMRE. For airborne and portable applications where space and weight savings are mandatory. High current for size. With accessories.



High voltage subminiatures

Series M, PM, SM. For photoflash, aircraft, instrumentation and communications. Single contact. Cable or panel mounted. With accessories.

High contact density subminiatures

Series SRD. For instrumentation, small modular packages, logic units, computers...cable or panel mounting types. With accessories.

For information write Main St. & Hillside Ave., Oakville, Conn.

WINCHESTER ELECTRONICS
DIVISION OF LITTON INDUSTRIES

Everything was in order (you thought). The transducer was connected to the preamp; the preamp was plugged in. The drive motors worked o.k. The signal came . . . and left . . . without a trace!

Familiar? Frankly, we had the same problem some years back. So we designed our own heat-writing system to get the quality we demanded. It performed so well that we've put it on the market. We wouldn't have done so if it didn't come up to BLH Electronics standards.

The heart of the system is the BLH THERMOTIP STYLUS with its signal-regulated automatic heat control. Set the heat control once and the system automatically adjusts to changes in signal without manual readjustment. Great for those long-wait situations where one-of-a-kind transients must be caught. Great for those multichannel applications where several different signals (each with its own variation characteristics) must be handled.

To be sure, BLH Electronics Recorders have a variety of plug-in preamplifiers. They all fit all our systems: 2, 4, 6 and 8 channels . . . portable, console or lowboy configurations.

Don't do a slow burn about sloppy recording traces. Get a real "cool" oscillograph . . . the BLH High Speed Strip Chart Recorder with the BLH THERMOTIP STYLUS.

To arrange for a demonstration in your plant, or for information on this new BLH THERMOTIP STYLUS Recorder, call BLH Electronics or your nearest BLH Representative. BLH Electronics, Inc. a Subsidiary of Baldwin-Lima-Hamilton Corporation, Waltham, Mass. Plants in Waltham, Mass., Pasadena, Calif., and Darmstadt, West Germany.

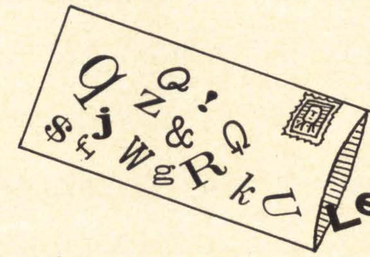
BLH ELECTRONICS, INC. BLH

A subsidiary of Baldwin • Lima • Hamilton Corporation

STRAIN GAGES • TEMPERATURE SENSORS • LOAD CELLS • PRESSURE CELLS • TORQUE PICKUPS • RECORDERS • INSTRUMENTATION • INTEGRATED SYSTEMS

Ever do a slow burn over a sloppy Strip Chart Recorder Trace?

CIRCLE NO. 29 ON INQUIRY CARD



Letters to the editor

BLACK BOX REVEALED

To the Editor:

The ladder network on page 60 of the October issue of **COMPUTER DESIGN** illustrated a new design approach but neglected to disclose the component configuration within the new "black box."

As a result of a recent job assignment, I know what should be in that rectangle and I am pleased to present it herewith.

Jay Freeman,
Flushing, N.Y.

BINARY CODED DECIMAL RESISTOR LADDER

JAY FREEMAN

When the straight binary code (. . . 16, 8, 4, 2, 1) is replaced with a BCD code in a D-A or A-D converter, the resistor ladder must be altered such that the inputs contribute the following weighting: (8, 4, 2, 1) + 0.1 (8, 4, 2, 1) + 0.01 × (8, 4, 2, 1), etc. The brute force method of constructing such a ladder is illustrated in Fig. 1, which was shown in the October article. However, this ladder has the disadvantages of a wide range of resistance values (which prevents all the resistors from being made from the same batch of resistance material, resulting in non-uniform temperature and aging characteristics), and large variations in input impedance (which load the sources differently, causing possible inaccuracy in the sources).

The well known R/2R ladder used in straight binary code has resistors and input impedances of similar value (Fig. 2). Converting this type of ladder into a BCD ladder is the ideal solution to the problem at hand. The network, achieved by the author after a combination of paper analysis and trial and error, established the need for a 9R terminating resistor and 8.1R coupling resistors between decade groups, and is shown in Fig. 3. The ladder output may be loaded with any resistance value, and the linearity will be maintained assuming the input sources are not affected by variations in the load. The unloaded output level is 56% of the input source level.

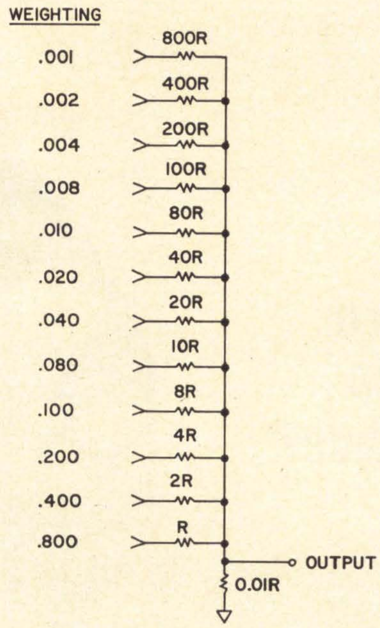


Fig. 1. Brute-force ladder.

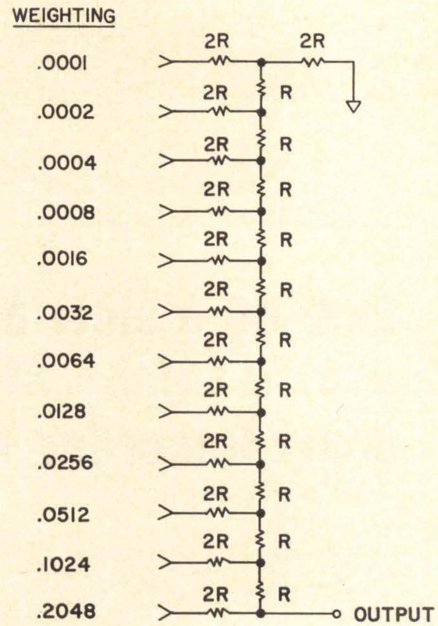


Fig. 2. R/2R binary ladder.

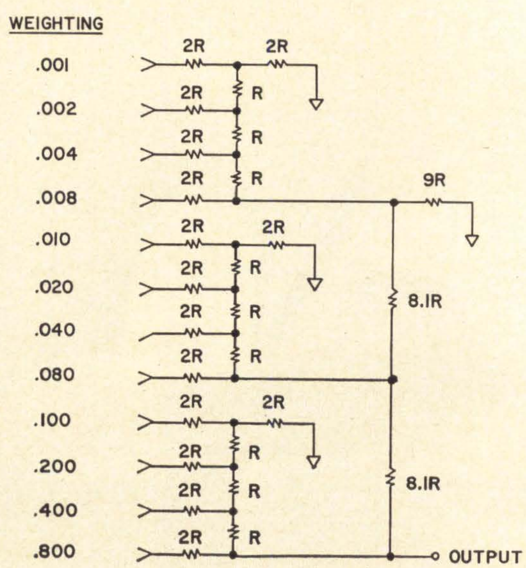
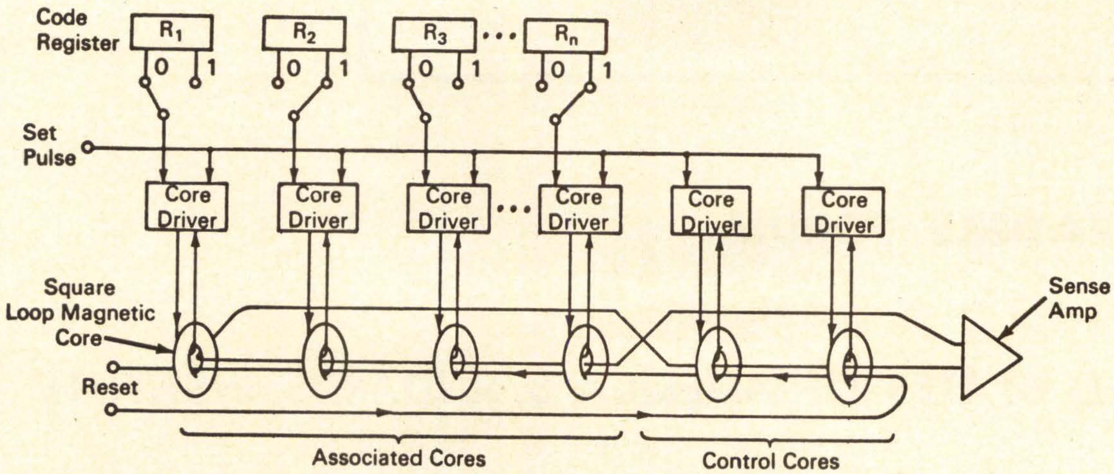


Fig. 3. Freeman's BCD ladder.

Digital System Detects Binary Code Patterns Containing Errors



THE PROBLEM:

In pulse code modulation (PCM) systems, digital code patterns containing errors frequently result in loss of telemetry information. Prior methods of overcoming this deficiency, including conversion to analog voltage pulses and comparison to a reference, have been costly in equipment and time consuming.

THE SOLUTION:

A system of square loop magnetic cores associated with code input registers to react to input code patterns by reference to a group of control cores in such a manner that errors are cancelled and patterns containing errors are accepted for amplification and processing.

HOW IT'S DONE:

All cores are initially in the zero or "reset" state. The code to be compared with the desired code is stored in the Register R_1 through R_N. Each register stage has an associated magnetic core and drive circuit. To test for the desired code, each core is "set" if the associated bit is **not** the desired bit. (Thus if the register contains the desired code, no cores would be "set".) In addition the control core or cores are also "set". All cores are now given a "reset" pulse, but only those cores that were "set" will induce a voltage on the sense wire. The sense winding is threaded through the register cores so that the induced voltage will be minus one unit for each core that was "reset". The sense winding is threaded through the control cores so that a voltage of plus one unit of voltage will be induced for each core threaded. The sense amplifier is adjusted to respond to voltages in excess of $+3/4$ unit voltage. If only one control core is used, the sense voltage will exceed $+3/4$ unit only if a perfect code is contained in the register. If one error is to be allowed, two control cores are used. In this way, one of the control cores will cancel the induced voltage from the error core and the second control core will cause the sense voltage to exceed $+3/4$ unit voltage. If a perfect code is in the register, both control cores will give $+2$ units of voltage to the sense amplifier which is more than enough to give an output from the sense amplifier.

NOTES:

1. Any number of errors may be tolerated by this embodiment by simply adding additional control cores such that there is one more control core than the number of errors to be tolerated.
2. This technique should improve reception capabilities in PCM telemetry systems.
3. Inquiries concerning this innovation may be directed to: Technology Utilization Officer, Goddard Space Flight Center, Greenbelt, Maryland 20771. Reference: B66-10516

PATENT STATUS:

No patent action is contemplated by NASA. **END**

What do you think?

This department is devoted to a continuous interchange of ideas, comments, and opinions on significant problems facing the industry. What do you think about the impact of a computer-automated world and the engineer/scientist's role in it? What do you think about engineering unions — professional societies — industry conferences? Or any significant facet of your professional life. COMPUTER DESIGN will print your views here. Write to: CD Readers' Forum, Computer Design, Baker Ave., West Concord, Mass. 01781.

CD READERS' FORUM

UNITED STATES OF AMERICA STANDARDS INSTITUTE

STATUS REPORT ON NATIONAL STANDARDS FOR COMPUTERS AND INFORMATION PROCESSING

Editor's Note: *In view of the interest and comments expressed over the past year-and-a-half on the subject of logic symbol standards, CD Readers' Forum presents two items of related interest. In the first, this month, the current status of the USASI (formerly the ASA) is reviewed. The second item, to be presented next month, is an extract of the "Proposed USA Standard Character Structure and Character Parity Sense for Parallel-by-Bit Data Communication in ASCII." The CD Readers' Forum invites comments from the readership on the activities of the USASI, in general, and on specific standards of interest to the digital engineering profession. We gratefully acknowledge the cooperation of Mr. Paul B. Goodstat, Director of Standards for BEMA, for providing this material for publication.*

The following USA Standards have received final approval and are available in published form from the United States of America Standards Institute, 10 East 40th Street, New York, N. Y., under the titles and numbers shown.

- USA Standard Signaling Speeds for Data Transmission, X3.1-1962, approved August 8, 1962.
- USA Standard Print Specifications for Magnetic Ink Character Recognition, X3.2-1963, approved November 7, 1963.
- USA Standard Bank Check Specifications for Magnetic Ink Character Recognition, X3.3-1963, approved November 7, 1963.
- USA Standard Code for Information Interchange, X3.4-1965, approved December 28, 1965.
- USA Standard Perforated Tape Code for Information Interchange, X3.6-1965, approved July 9, 1965.
- USA Standard Interchange Perforated Tape Variable Block Format for Positioning and Straight Cut Numerically Controlled Machine Tools, X3.7-1965, approved July 9, 1965.
- USA Standard and Interchangeable Perforated Tape Block Format for Contouring and Contouring/Positioning Numerically Controlled Machine Tools, X3.8-1965, approved July 9, 1965.
- USA Standard FORTRAN, X3.9-1966, approved March 7, 1966.
- USA Standard Basic FORTRAN, X3.10-1966, approved March 7, 1966.
- USA Standard Specification for General Purpose Paper Cards for Information Processing, X3.11-1966, approved March 7, 1966.
- USA Standard Flowchart Symbols for Information Processing, X3.5-1966, approved June 8, 1966 (Amended).

• USA Standard Vocabulary for Information Processing, X3.12-1966, approved June 14, 1966.

• USA Standard for Parallel Signaling Speeds for Data Transmission, X3.13-1966, approved June 14, 1966.

• USA Standard for Recorded Magnetic Tape (200 CPI, NRZI), X3.14-1966, approved June 14, 1966.

• USA Standard Character Set for Optical Character Recognition, X3.17-1966, approved July 5, 1966.

• USA Standard for Bit Sequencing of the USA Standard Code for Information Interchange in Serial-by-Bit Data Transmission (Low Order), X3.15-1966, approved August 19, 1966.

• USA Standard for Character Structure and Character Parity Sense in Serial-by-Bit Data Communication in the USA Standard Code for Information Interchange, X3.16-1966, approved August 19, 1966.

The following proposed USA Standards have been approved by Sectional Committee X3 and submitted for final review and approval by the Information Processing Systems Standards Board and the USA Standards Institute Board of Review.

• Proposed USA Standard for One-Inch Perforated Paper Tape for Information Interchange.

• Proposed 1966 Revision to the USA Standard Code for Information Interchange (X3.4-1965).

The following proposed USA Standards are being balloted on by USA Standards Institute Sectional Committee X3.

• Proposed USA Standard Recorded Magnetic Tape (800 CPI, NRZI).

• Proposed USA Standard 11/16" Perforated Tape for Information Interchange.

• Revised proposed USA Standard for Take-up Reels for One Inch Perforated Tape for Information Interchange.

• Proposed USA Standard for Rectangular Holes in Twelve-Row Punched Cards.

The following proposed USA Standard has been submitted to X3 by the subcommittee and is awaiting X3 authorization for letter ballot.

• Proposed USA Standard Character Structure and Character Parity Sense for Parallel-by-Bit Data Communication of the USA Standard Code for Information Interchange.

The following work is in process in X3 subcommittees.

• X3.1 — **Optical Character Recognition:** reviewing draft proposal on print quality.

• X3.2 — **Codes and Input/Output:** developing a new proposed punched card code standard; reviewing the 800 cpi proposed standard to resolve some questions concerning permissible track skew; other work involves the areas of edge punched cards, magnetic tape label formats, code extension of USASCII, 1600 cpi phase encoded magnetic tape, graphic assignments to USASCII control functions, and the representation of USASCII in other than 7 bit environments.

• X3.3 — **Data Transmission:** working in such areas as data transmission formats, functional control requirements, system performance characteristics, and signaling speeds.

• X3.4 — **Common Programming Languages:** it is planned to have a complete COBOL standard prepared by the end of the year; other work is in the areas of APT, ALGOL, PL/1, and FORTRAN.

• X3.5 — **Vocabulary:** considering new terms and definitions for inclusion in an updated version of the USA Standard Vocabulary for Information Processing.

• X3.6 — **Problem Definition and Analysis:** a draft proposed standard for flowchart conventions has been written and approved by the subcommittee; other work in the areas of graphics and decision table standards.

• X3.7 — **Magnetic Ink Character Recognition:** studying a proposal from the National Bureau of Standards for a stable MICR signal level standard.

• X3.8 — **Data Elements and Their Coded Representation:** work in the areas of standard techniques and criteria for structuring data and codes; specific code standards for identification of individuals, businesses, and geographic units; standard representation of calendar dates, time, and time intervals; and possible standardization of error detection techniques.

GOVERNMENT REPORTS ★★

A CATHODE RAY READOUT SYSTEM

An instrument designed by the Space Agency satisfies the need of modern digital telemetry systems for improved methods of monitoring large quantities of digital information during the design and testing phases of many programs. It was devised in conjunction with the NIMBUS B, IRLS (Interrogation Recording and Location System) experiment design. With the exception of complex data handling equipment, devices used in present-day practice are inherently slow, making data analysis very time consuming. Therefore, an instrument which provides a high data handling capability combined with a convenient display technique is highly desirable. The NASA device provides a means of visually displaying, in numeric form, the ones and zeroes contained in a serial pattern of binary bits formatted into a frame containing up to several hundred bits. The result of this innovation has been a great saving in both time and expense, since system operation can be quickly and accurately checked for bit errors or other malfunctions in discrete system components or in the RF link.

Order from Clearinghouse, U. S. Dept. of Commerce, Springfield, Va. 22151. Order No. N66-19758. Price: $1.00.

commentary

Comments and opinions on topics of current interest to digital design engineering personnel. A monthly column organized and prepared under the direction of **T. PAUL BOTHWELL, Contributing Editor.**

LET'S SIMPLIFY INGENIOUS MECHANISMS

EARL MASTERSON

From its earliest days, the computing community has been plagued with the shortcomings of mechanical equipment. Even in the electronic world of today, progress in the data processing field is still impeded by the limitations of mechanical devices. Fortunately, the brief review of mechanism evolution which follows indicates that we are, at long last, on the verge of a much needed breakthrough.

Is Complexity Ingenuity?

More than a century ago, Charles Babbage, the acknowledged father of computers, spent much of his time and fortune trying to perfect his Difference Engine and his Analytic Engine. It is sad to reflect that even these early efforts were thwarted by mechanical design complexities. It is interesting to speculate where the state-of-the-art would be today if he had invented fluid logic. Ironically, in the decades following Babbage, designers continued to produce a seemingly endless stream of mechanisms, each more complex than the last. The apogee of this trend is well documented by a three-volume set of books, titled, "Ingenious Mechanisms for Designers and Inventors," published by The Industrial Press in 1930. The amazing array of mechanisms seemed to indicate that any motion could be generated if a designer used enough cams, linkages, odd-shaped gears, etc.

The author of this month's CD Commentary, Earl Masterson, is the Associate Director of Peripheral Engineering at Honeywell's EDP division. He is responsible for the development of high-speed printers, punched card equipment, document readers, and mass memories.

Judging from the appearance of the 11th printing in 1957, many designers apparently came to consider these three volumes as mechanical design handbooks. In fact, one might speculate further that the designs for many of the first commercially-successful computing machines were taken directly from the pages of these books. Punched card printing tabulators, desk calculators, and parallel feed card punches, readers, reproducers and sorters are typical examples. Only the tremendous increase in productivity made possible by these machines, compared to hand manipulation of data, overshadowed the limitations in speed, efficiency, and reliability inherent in their design. It is apparently difficult for many designers to resist the novelty of a complex mechanism. The pressures of an impartial, competitive market, however, soon dictate the development of better devices.

Prodding Puffing Peripherals

With the advent of electronic data processing came a need for peripheral equipment which would more closely complement the speed and efficiency of the computer itself. Although still far behind the spectacular advances in electronics, the machines developed to answer this need represent the beginning of a trend away from complex mechanisms.

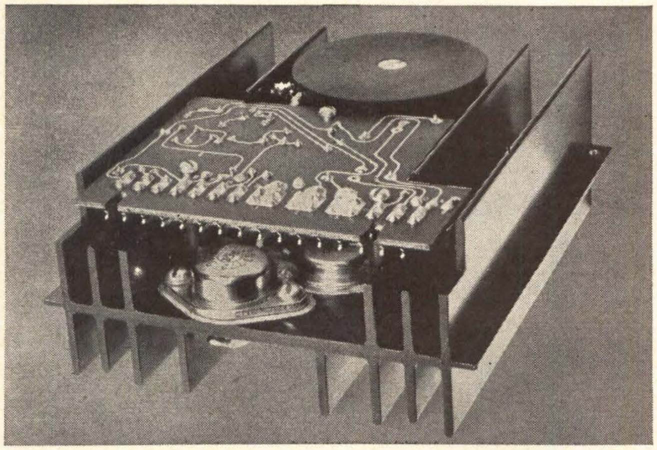
Today's line printer, for example, runs about 10 times as fast as a printing tabulator and has perhaps 1/10 as many moving parts. The almost universal switch from parallel to serial punched card processing has contributed greatly to the simplification of punching and reading devices. Feed rates have changed little, but the number of moving parts has been reduced greatly and reliability has improved accordingly.

Before concluding that future improvements in

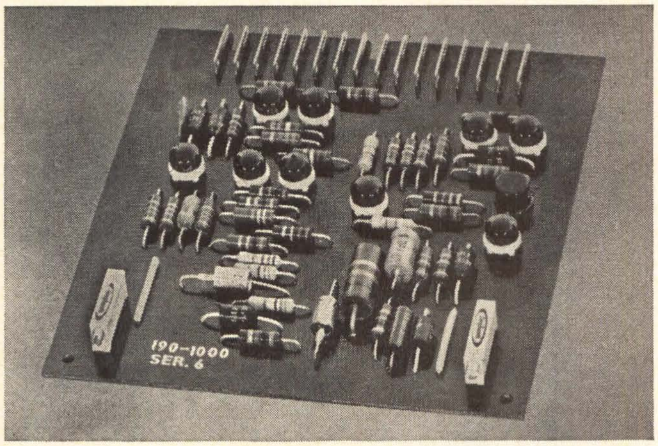
Does your present custom power supply give you...

70% to 90% efficiency? ?	Instant fault repair by plug-in module replacement? ?	Add-on power capability by using more modules? ?	Ability to handle full load steps while maintaining out put in regulation band? ?

New Omnimod does!



Omnimod power control module.



Omnimod control amplifier.

OMNIMOD gives you all these features—*and* more—*and* at a lower price! Want to know more?

OMNIMOD is a dc to dc converter using transistors in a CONSTANT PULSE WIDTH, variable repetition rate switching mode to regulate output voltage or current. Two small plug-in units make-up the OMNIMOD concept—a power control module and a control amplifier.

Output can be regulated between $\pm$ 2 and $\pm$ 60 dc at up to 20 amperes using the OMNIMOD family of modules WITHOUT MODIFICATION OR ADJUSTMENT. Higher current ratings are obtained by paralleling power control modules.

Any number of power controller modules can be controlled by one amplifier. OMNIMOD has a current limiting parameter, over voltage protection, voltage sequencing, and remote sensing.

To design a custom power supply, one must simply

1. design one input power converter to change unregulated line ac power to unregulated dc power
2. select the number of plug-in OMNIMOD power control modules to supply the power needed for each output
3. package these elements with filter capacitors and a plug-in amplifier module for each output

All the power used by every element in a typical data processing system could be supplied by custom power supplies constructed with interchangeable OMNIMOD modules.

Isn't this enough to consider OMNIMOD for your custom requirement? We will design an OMNIMOD custom power supply to your specs, or will help you design your own system using our plug-in OMNIMOD modules.

Write for the complete story. We'll have it to you within 48 hours.

CONTEMPORARY ELECTRONICS

EXTRA SERVICE TO THE DATA PROCESSING INDUSTRY

4838 West 35th Street, St. Louis Park, Minnesota 55416 • 612/920-6444

CIRCLE NO. 31 ON INQUIRY CARD

computer peripheral equipment will necessarily be based on design simplicity, a review of the trends in other fields is in order. Even a cursory examination soon reveals that:

- Jet engines with a single rotating shaft are rapidly replacing the more complex reciprocating aircraft engine;
- The complex internal combustion engine, for half a century the stalwart of the automotive industry, is presently being challenged by the less complex electrical motor;
- Ultrasonic drilling and pile driving techniques, although relatively new, are already beginning to replace conventional methods;
- In both black and white and color television, early designs were impractical until the mechanical scanning disk was removed;
- The age-old principle of the tuning fork, combined with modern electronics, has resulted in a timepiece of simpler design and greater accuracy than the conventional watch movements.

Simplifying For Cost-Savings

Simplification is indeed a widespread trend. Without a doubt, the peripheral equipment designer of today must categorically reject many time-honored concepts in his search for improved performance. Instead, he must learn to combine simple mechanisms with modern electrical and electronic components, thereby achieving optimum cost/performance ratios. Demonstrating the success of this approach, there is now in production a high-speed card punch which contains no gears, cams, ratchets, genevas, detents, clutches or brakes, and which requires no field lubrication. Competitive both in cost and performance, this machine is typical of the breakthrough possible in other areas of peripheral equipment design.

In the area of printers, the next generation likely will utilize non-impact printing techniques. Similar to our earlier comparison of line printers with tabulators, the non-impact printer can be expected to operate at 10 times the speed of its predecessor and contain perhaps 1/10 as many moving parts. Simplifications are also taking place in the unit record area. Optical document reading equipment is starting to replace, in certain applications, the mechanically more complex punched card equipment.

One of today's most pressing needs is in the area of remote terminals where a typical character serial printer must operate at approximately the same cyclic rate as the paper feed in a line printer. Although serial printers generally contain as many moving parts as line printers, to be practical, their maintenance cost must be much lower. This device and related devices are the challenge to the ingenious designer of today. There is virtually no limit to the breakthroughs possible with an outlook ingenious in its simplicity instead of its complexity.

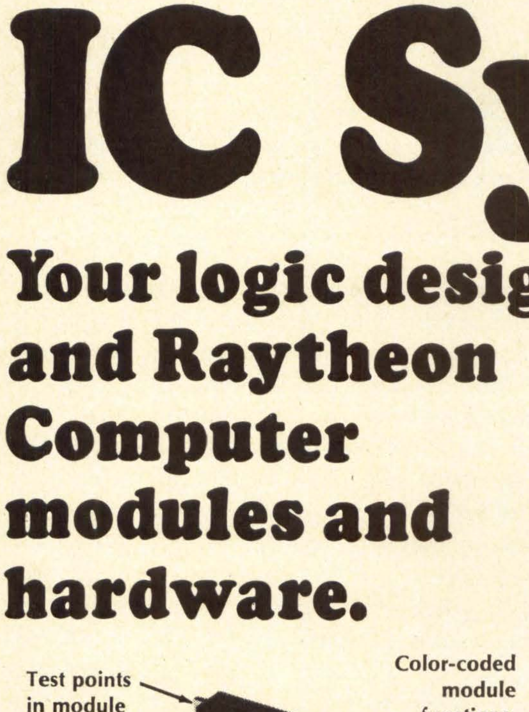
The Unbeatable IC System:

Your logic design and Raytheon Computer modules and hardware.

Test points in module handle.

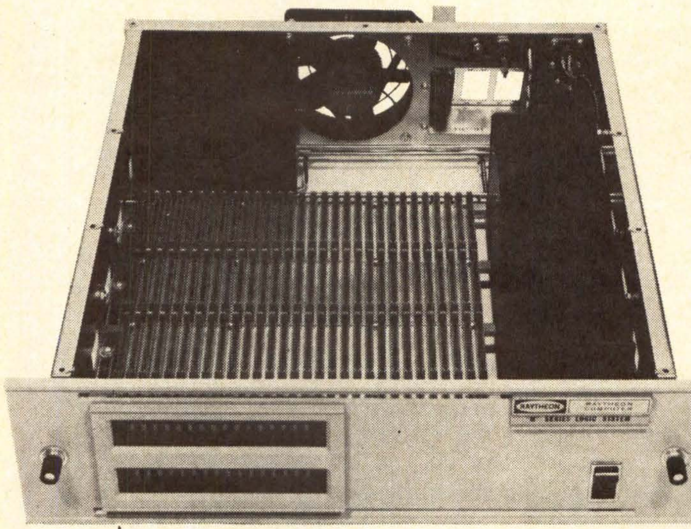
Color-coded module functions.

Connectors in blocks of 10, 30 and 40 for fast system assembly.



Ready for our automatic wire wrap service.

Laminated power bus bars installed and wired in each module case. Reduces noise, eliminates power inter-connections, cuts hours from assembly and test time.



Indicator lights display system operation.

This case holds 120 modules. There's also one for 40; another for 400.

Raytheon Computer's M-Series — more than 30 modules—connectors, cases, power supplies and power distribution are so thoroughly engineered you can concentrate on logic and electronic design, not mechanical details. Every step—design, assembly, test, check-out, troubleshooting—is easier than you thought it could be.

We'll even help you design your logic. Call or write today for a visit from a helpful applications engineer or for the whole story in print. Ask for Data File M-136. Raytheon Computer, 2700 S. Fairview St., Santa Ana, Calif., 92705, Phone: (714) 546-7160.

RAYTHEON

CIRCLE NO. 30 ON INQUIRY CARD

DC OUTPUT

from our man in Washington

Value of EDP machine and associated equipment shipments is expected to increase 9.9 percent from 1966 to 1967 compared to an estimated 12% growth from 1965 to 1966, according to the 1967 outlook report of the U. S. Department of Commerce. According to the report, the trend toward time-sharing suggests a greater demand for large-scale computers as users tie-in multiple organizational elements by console to a central computer. This trend will also be aided by the growth of computer utility companies selling computer time to remote customers tied-in to the central computer by telephone lines. It is likely that the demand for small and medium computers will stay firm as users of time-sharing systems may still prefer their own additional on-site small or medium-size computers.

EDP is expected to be used to an increasing extent by the telephone industry during the coming decade, according to a manpower study of the telephone industry by the U. S. Department of Labor. Increases will be especially significant among functions for which computers have been used to only a limited extent. The impact will fall primarily on clerical workers, although other occupation groups will also be affected, the study states. The electronic central office (ECO) promises to be more revolutionary to the telephone industry than any other technology that will be introduced in the next decade. The performance of the ECO is similar to that of a high-speed, general-purpose computer with a stored program, according to the Labor Department study. However, it is much more complicated than the typical computer. The ECO will contain about a million components — 45,000 diodes, 13,000 transistors, 35,000 resistors, 225,000 soldered connections, and 56,000 connector terminals.

Rapidly-expanding foreign demand for computers provided the impetus for a significant gain in exports of office machinery during the first ten months of 1966, the U. S. Department of Commerce reports. Users in Canada, the United Kingdom, and several eastern European countries have accelerated their purchases of U. S. computers and parts as well as accessories for accounting and bookkeeping machines.

Better computers will mean better weather forecasts, Government speakers told the national meeting of the American Association for the Advancement of Science. Presently nature has set a limit of about two weeks on how far ahead weather can be predicted. The computer and the satellite have placed meteorology on the threshold of major new advances in the science of weather prediction and in the scientific theory of climate, making the time ripe for the nations of the world to embark on the World Weather Program, according to Dr. Robert M. White, Administrator, Environmental Science Services Administration. Dr. Joseph Smagorinsky, Director of ESSA's Geophysical Fluid Dynamics Laboratory, added that to simulate the evolution of air in the Northern Hemisphere through a single day requires 10 billion computer operations. The difficulty is to devise a computer that can solve the problem before the weather does so. A good deal of information will have to be poured into the computer to make forecasts more meaningful, he said.

Coordination of highway and transit planning through the utilization of computer technology is the objective of a $160,000 research project contract which was recently awarded by the U. S. Department of Housing and Urban Development to the Alan M. Voorhees and Associates consulting firm of McLean, Va. The project will include the development of a package of computer programs to aid metropolitan areas in the analysis of their individual transit planning requirements.

During fiscal 1966, the U. S. Government avoided costs of $26 million through its Automatic Data Processing Sharing Exchange Program through which EDP re-

continued on page 69

Decision Control's VersaSTORE core memories have the best operating margins in the business

Here's why

Magnetic cores used in memory systems change characteristics with temperature, causing shifts in operating margins. Older memory systems used stack heaters in an effort to maintain a constant temperature. Heaters had several drawbacks — warm-up time, temperature gradients throughout the stack, etc.

VersaSTORE overcame the need for a stack heater with a unique and simple servo which allows stack temperature to follow ambient temperature, but compensates by optimizing drive currents, and insures excellent margins under all conditions. Both our standard VersaSTORE and our mainframe VersaSTORE use the unique D.C.I. servoed drive system.

To further improve these margins, sense amplifier gain is uniformly maintained to 1 mv without adjustment. And, these VersaSTORE margins are guaranteed at the customer end of the cable — 25 feet for mainframe VersaSTORE.

VersaSTORES are available from 256 to 4096 words of up to 24 bits per word for use in buffers, I/O equipment, etc. Mainframe VersaSTORES for computer mainframes and large digital systems are available from 4096 to 65,536 words of up to 36 bits or 72 bits.

For more data about VersaSTORE's integrated circuit construction, compact sizes, and compact prices, please write.

dci **DECISION CONTROL, INC.**

1590 Monrovia Avenue, Newport Beach, Calif. Tel. (714) 646-9371 • TWX (910) 596-1358

CIRCLE NO. 34 ON INQUIRY CARD

INDUSTRY NEWS

THE ADVANCED RESEARCH PROJECTS AGENCY OF THE DEPT. OF DEFENSE HAS APPROVED THE SELECTION OF BURROUGHS CORP. for the engineering development of ILLIAC IV. When completed, this giant computer system will be capable of doing one billion calculations every second. The ILLIAC IV will have four control units interacting with more than 250 arithmetic and data storage units which will increase the speed of data processing from 500 to 700 times over that of present computers and over 100 times faster than any computer known to be in development. The University of Illinois, the Agency's prime contractor for parallel processing computer research, will negotiate the contract with Burroughs Corp. The contract is expected to amount to several million dollars. The ILLIAC IV project is a part of ARPA's research on information processing and will be directed by Professor Daniel Slotnick of the University of Illinois. Examples of ILLIAC IV's use would be the simulation of the atmosphere for weather prediction, the modeling of large economic systems and simulation of large and extremely complex military logistics problems.

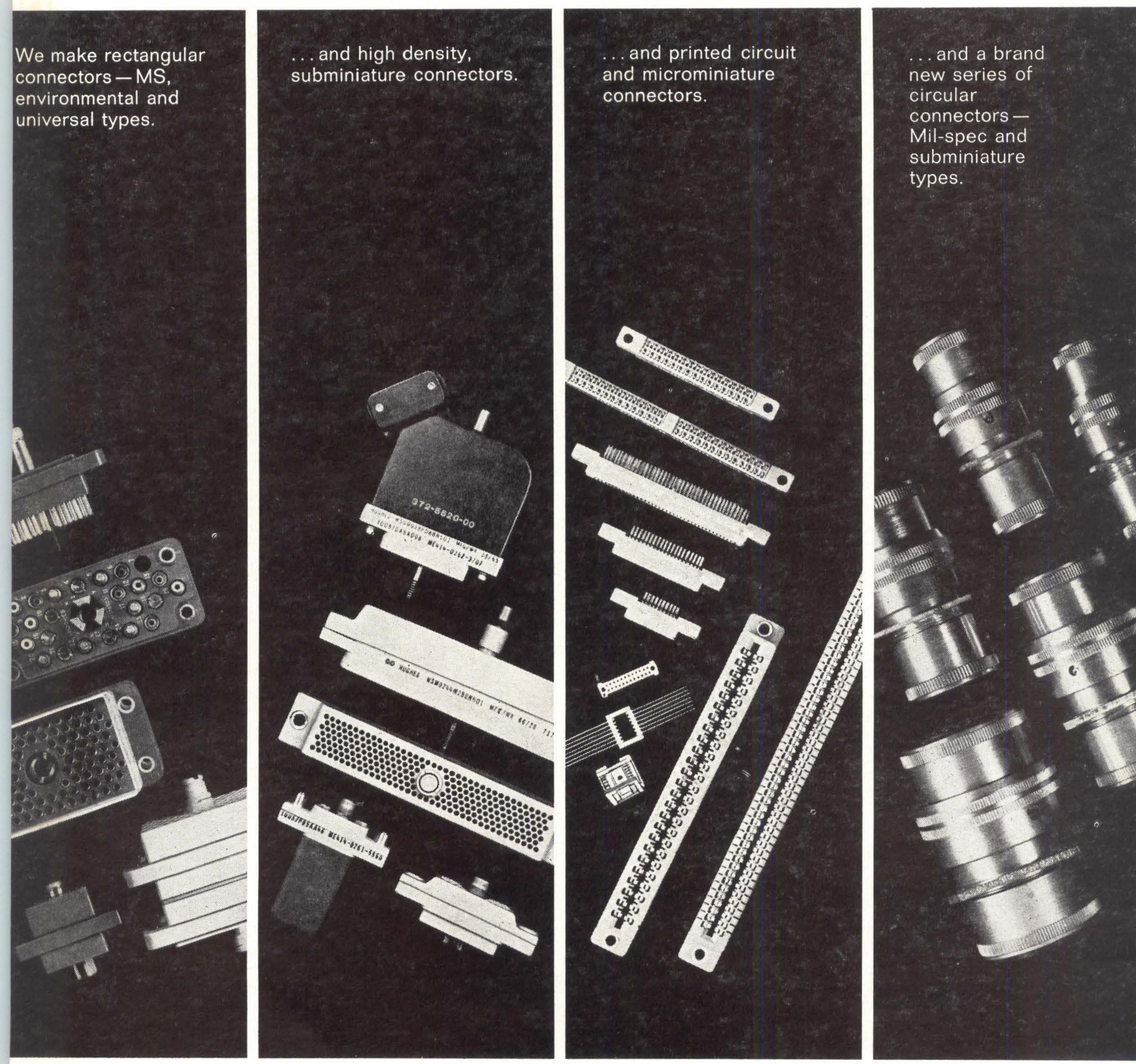
In commenting on the selection, Ray W. Macdonald, Burroughs President, said "We consider ILLIAC IV to be the most significant undertaking in the field of electronic computer design in the past several years. The techniques which will be employed, including the use of large-scale arrays of integrated circuits combined with extremely high-speed thin-film memory storage, will have important effects upon the design of systems of the future. The LSI devices will be developed by Texas Instruments, Inc." Macdonald said that the development of ILLIAC IV will be performed by the Company's Defense, Space, and Special Systems Group headquartered in Paoli, Pa.

WHAT IS CLAIMED TO BE THE FIRST COMMERCIAL MULTI-ACCESS COMPUTER FACILITY has been established in the Washington area by C-E-I-R. Teletype terminals linked via standard telephone lines to a large central computer at the C-E-I-R center have been set up in the offices of over 60 users, most located in the metropolitan Washington area, but some situated hundreds of miles away. Many government agencies and private research firms are among the clients which have tied into the C-E-I-R "MAC" system. For instance, the National Bureau of Standards now has nine such terminals in use at its Gaithersburg "campus", and the Institute for Defense Analysis is using three terminals. While problem-solving capacity through a Teletype is limited, due to restrictions on the size of programs that can be accepted, the multi-access concept has proved to be a boon to the worker who encounters problems in the course of his day's work that can be best handled with "MAC" assistance.

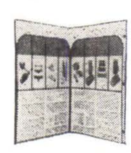
HONEYWELL'S COMPUTER CONTROL DIVISION HAS BEEN AWARDED A $1.4 MILLION CONTRACT TO SUPPLY 21 COMPUTERS TO KEYDATA CORP. Keydata, which offers a computer-sharing service to business subscribers, expects to install five new DDP-516 machines at its Cambridge, Mass., headquarters to supplement 3 DDP-116's already in service there.

THE OVERWORKED AND OFTEN MISPLACED HYPHEN HAS BEEN VIRTUALLY ELIMINATED IN A NEW COMPUTERIZED TYPESETTING SYSTEM developed jointly by the Western Electric Company and the Radio Corporation of America. Combining an RCA Spectra 70/25 computer system with a phototypesetter, the new process is being used to produce a continuous flow of Bell System technical documents, covering the installation, test, and maintenance of products manufactured by Western Electric. Called "AutoSCRIPT" (representing an "Automated System for Composing, Revising, Illustrating, and Phototypesetting"), the computer-controlled process effects a substantial reduction in time and money, as well as an improvement in quality, according to RCA. Prior to the new installation, type was set on a manual linecaster and the machine operator was concerned with hyphenation of words and justification of lines. In addition, making copy revisions was complicated and time-consuming. Using AutoSCRIPT, the computer and phototypesetter have the flexibility to justify lines on the 2-column pages, without resorting to hyphenation except under most unusual circumstances. Since the system went into full operation on August 1, it has not been necessary to hyphenate.

What's our line?



Our real line is solutions to tough interconnection problems. What we show above is just a cross section of the precision connecting devices we've developed to solve both standard and special problems. Chances are, we've already solved yours. If not; we'd welcome a crack at it. May we send you our descriptive literature? Or answer your questions about special types? You'll receive a prompt answer.



INDUSTRY NEWS

THE SOVIET UNION IS MAKING CONSIDERABLE EFFORT TO INTEGRATE CYBERNETICS WITH THE BELIEFS AND INSTITUTIONS OF SOVIET SOCIETY, and the future of the USSR possibly depends on the way this integration is finally effected. This and other assessments of cybernetics in the USSR are made in a recently completed study by Dr. Robert W. Brainard and Dr. William D. Hitt of the Columbus Laboratories of Battelle Memorial Institute. In the Soviet Union, cybernetics is being applied to an extremely broad range of activities, from factory production control to economics, law, medicine, and education. The most ambitious application is in the field of economies, where a bold national program aimed at establishing a cybernetic system for controlling the entire economy is being vigorously developed. At the heart of this proposal is a dynamic mathematical model of the entire Soviet economy. Planning and control would be implemented through an integrated nation-wide network of computer centers. Soviet experts predict that this program, when introduced, will raise the national economic output by one-third, and will double the present rate of economic growth. In general, Dr. Brainard and Dr. Hitt find that there are fundamental differences between the U. S. and the USSR in the development and application of cybernetics. The environment in the U. S. appears to be more conducive to creative breakthroughs in cybernetic theory, while the Soviet environment appears to be more conducive to large-scale application of cybernetics.

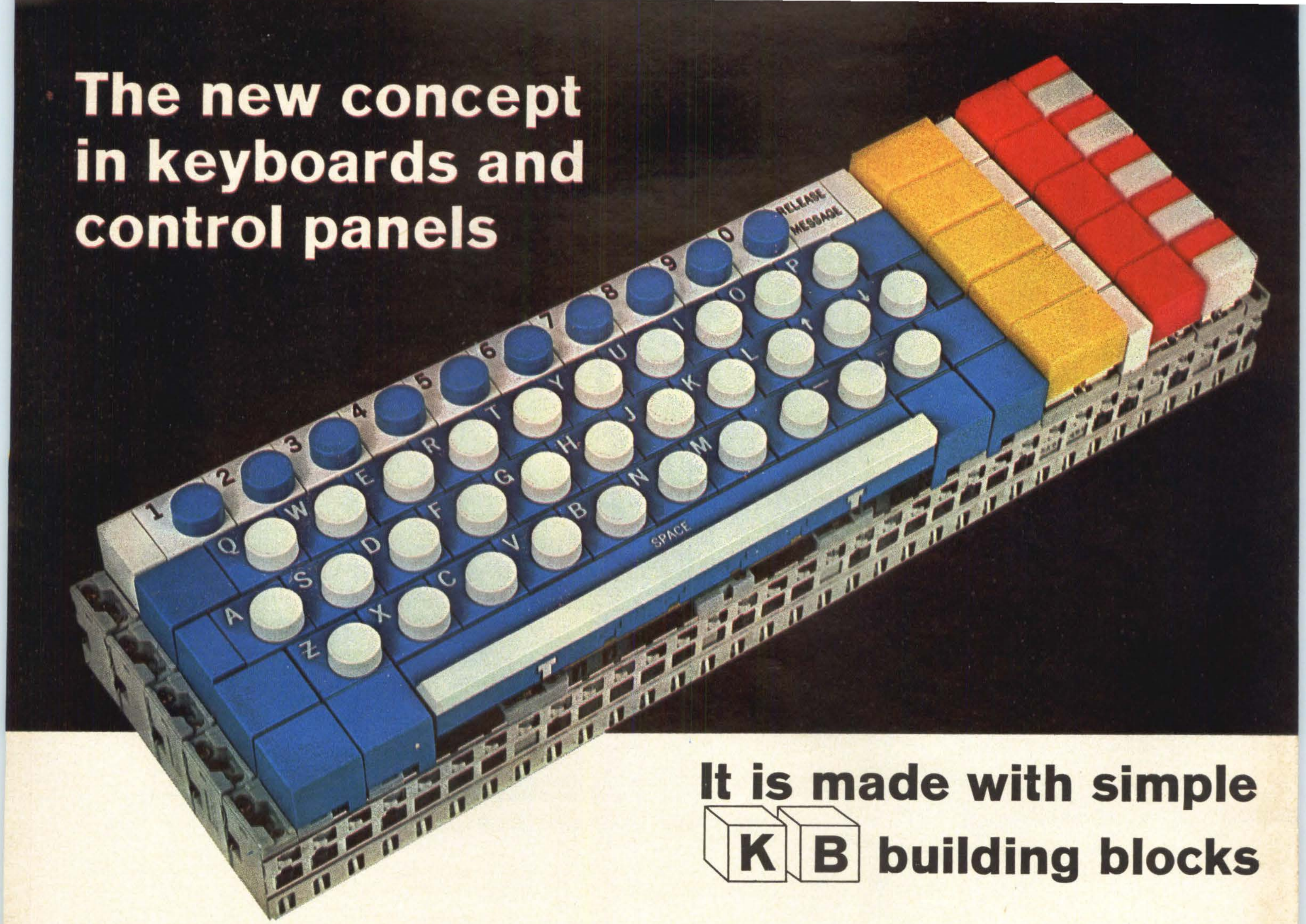
INDUSTRY NEWS

UNDER A RECENT CONTRACT WITH NASA, THE UNIVERSITY OF GEORGIA HAS ESTABLISHED A CENTER FOR THE DISSEMINATION OF COMPUTER PROGRAMS AND COMPUTER INFORMATION. This center known as Computer Software Management and Information Center (COSMIC) is working through the NASA Technology Utilization Office at the Marshall Space Flight Center in conjunction with other Nasa Centers and Nasa headquarters. Through this joint effort, computer programs and computer information developed by or for Nasa will be made available to primarily non-aerospace industry. By disseminating these computer programs Nasa hopes to contribute directly to our national industrial effort and offer industries the opportunity to avoid duplication and to shorten the task of developing certain computer programs. Due to the inventory and control problems of maintaining tape and program deck libraries and the associated cost and rapid retrieval problem, COSMIC has been established as the central dissemination center. The computer programs to be disseminated will be obtained from Nasa supported activities. These programs, many of which have been or will be designed for broad applicability, will be examined and evaluated to determine which offers the most probable application to industrial use. The programs (source decks) will be disseminated in tape or card form depending upon the requestor's preference. However, it is recommended that program decks over 2000 cards be requested in tape form. If a tape copy is requested, the requestor must furnish a copy tape for processing. Each requestor will be charged for the handling and mailing of programs. There will be no charge for requests for copies of computer program documentation.

The charge for program requests is $20 per program for a card deck or tape copy. If, however, more than one program is requested on one order and these programs can be copied onto a single tape, the charge for the additional programs will be $10 each. A complete inventory listing with abstracts of all available programs will be disseminated periodically, to be added to the mailing list for dissemination of this listing, or for additional information, write to COSMIC, Computer Center, University of Georgia, Athens, Georgia 30601.

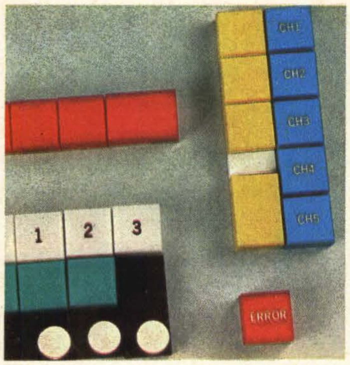
A THREE-YEAR $20 MILLION PROGRAM TO EXPAND THE DEVELOPMENT AND MANUFACTURE OF SEMICONDUCTOR PRODUCTS IN THE UNITED STATES AND OVERSEAS was announced by the ITT Semiconductors Worldwide group of International Telephone and Telegraph Corporation. The expansion, to be completed in 1968, was disclosed by George Williams, group general manager, ITT Semiconductors Worldwide. Mr. Williams said, "Our program of worldwide expansion is currently expediting our growth at twice the industry average rate. It has quadrupled our dollar volume in the past five years, and we confidently expect we will continue at this growth rate and be one of the three leaders by 1971. The $20 million expenditure will be divided approximately 50% in the United States and 50% overseas. But the major program in the U. S. will be a $5.3 million expansion of the present West Palm Beach semiconductor manufacturing plant.

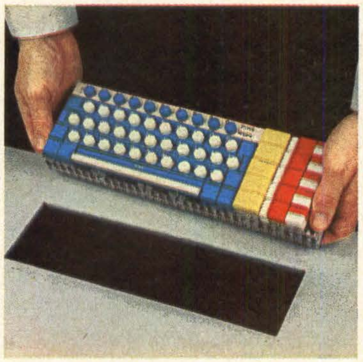
The new concept in keyboards and control panels

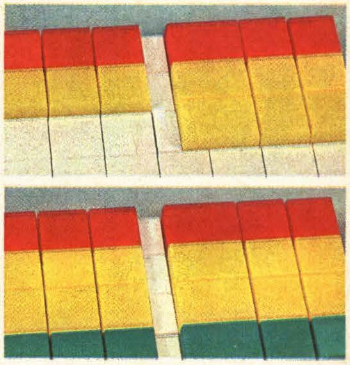


It is made with simple KB building blocks

KB offers these exclusive advantages:







KB allows new freedom of arrangement. Modular construction makes it easy to customize your panels—economical, too.
Switches and indicators available in a wide variety of colors, shapes, sizes. Arrange in vertical columns, horizontal rows, compact rectangles, or individually—all, in a single cutout.

KB allows bench assembly. Assemble a complete keyboard matrix at the bench where the job is easier, faster. Even the wiring is done before the matrix is set into the console.
And only one panel cutout is required because KB forms its own self-supporting matrix—no additional support required.

KB provides plug-in modularity. With KB plug-in switches, simply loosen two screws, lift out the unit and plug-in a replacement—all from the front of the panel.
Store a reserve unit right in the board—or "borrow" one that is not as urgently needed elsewhere on the panel. Downtime is practically eliminated.

KB simplifies expansion. KB modular construction makes planned or unplanned expansion easy, economical. In many cases, you simply remove spacers and plug-in additional switch or indicator modules to up-date your panel. No additional cut-outs, no wiring, no soldering, no behind-the-panel work required.

What is KB? The KB system provides all the components necessary for a complete, self-supporting matrix, including: Power Switches and Indicators with lighted display, Encoding Switches with up to eight output bits, Mechanical Interlock Modules for a variety of sequential functions, and a unique Modular Framework System.

Find out what KB can save you in engineering time, tooling costs, assembly costs, panel space and weight—and how KB can put more sales appeal into your panels.

For a KB demonstration, call a MICRO SWITCH Branch Office (see Yellow Pages). Or, write for literature.

MICRO SWITCH
FREEPORT, ILLINOIS 61032
A DIVISION OF HONEYWELL

HONEYWELL INTERNATIONAL • Sales and service offices in all principal cities of the world. Manufacturing in United States, United Kingdom, Canada, Netherlands, Germany, France, Japan.

CIRCLE NO. 39 ON INQUIRY CARD

A 10^{13} BIT MASS MEMORY READS AND WRITES WITH LASER

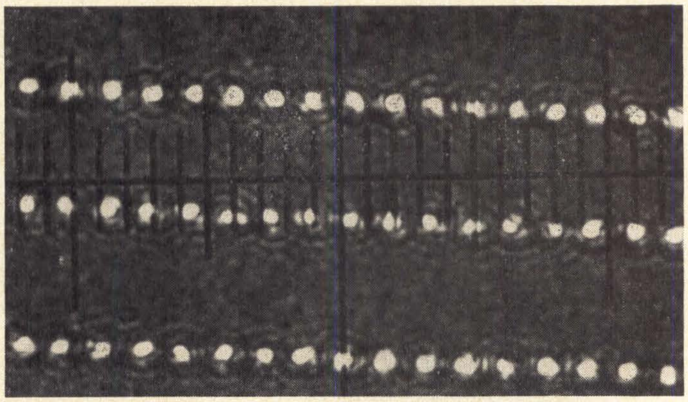


Fig. 1. Micro-photographs of 1.5 micron holes in recorded Unidensity tape.

An experimental laser-recorded digital data mass memory process provides a packing density of 645,000,000 bits per square-inch. Based on the UNICON (Unidensity Coherent Light Recording) process, it is the result of five years of basic research and development. The process makes use of a 1-watt CW Argon laser to burn minute holes in the tape storage medium. It is not a photographic process. The continuous radiation of the laser is gated by an electro-optical modulator to produce optical bits corresponding to the digital data input.

Opaque-coated Unidensity polyester tape is moved by a helical-scan transport around the imaging circle of the laser aperture, which is formed by diffraction-limited objectives rotating at 1800 rpm. The laser aperture produces a three-dimensional Debye ellipsoid image with a temperature of 3,000°K in the 4-micrometer-thick opaque coating of the tape. This vaporizes the coating and produces an ellipsoidal hole with a cross-sectional diameter of 1 micrometer. The clear polyester tape backing itself is not harmed, since the image is precisely located in the coating. The rotating objectives sweep the gated beam across the helically-transported tape at an angle of incidence of 1°43′ to produce lines of 1-micrometer holes 60 cm long on standard 16 millimeter tape. Each line has a capacity of 600,000 holes. As the tape advances, successive parallel lines are recorded. A track at the upper edge provides a binary file-accession code to locate each individual track for readout. A micro-photograph of 1.5 micron holes in recorded Unidensity tape is shown in Fig. 1.

As light passes through the vaporized 1-micrometer holes and the clear tape during recording, it is collected in a plexiglass light guide, conducted to a central photomultiplier, and translated into electrical impulses which are compared with the data input to verify the recording. This provides the immediate "Read-After-Write" capability that has been the ultimate objective of memory sys-

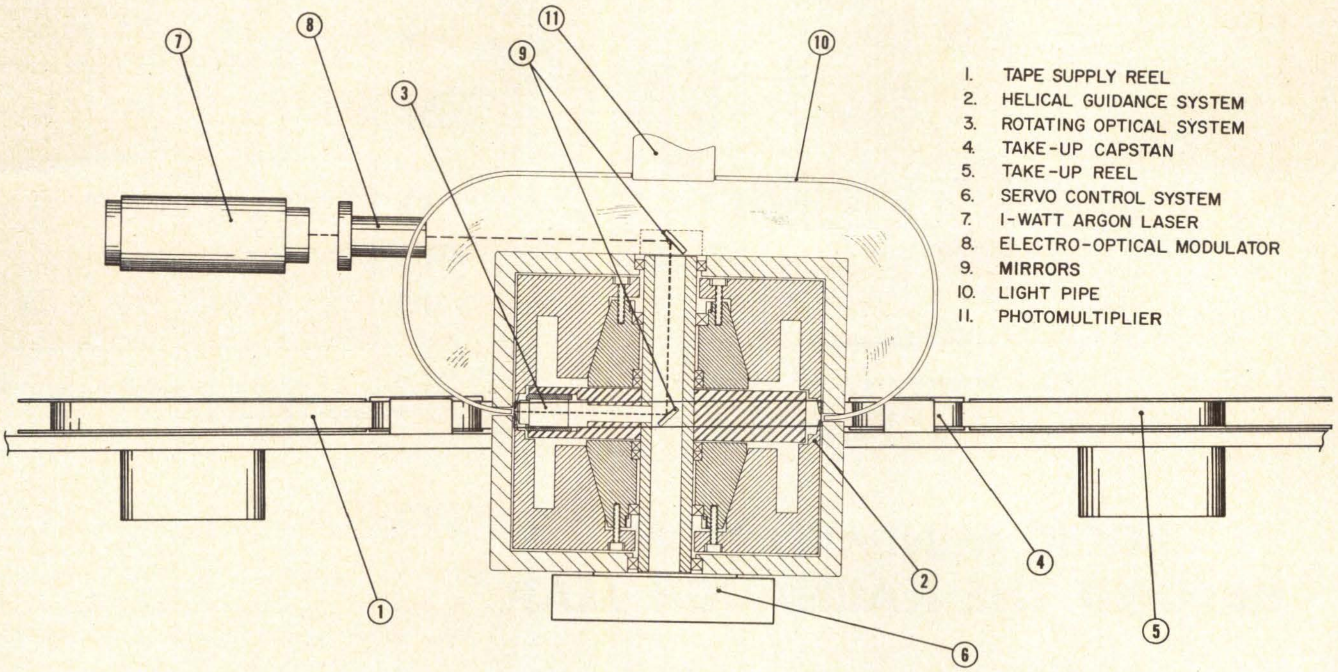


Fig. 2. Cross-section view of Unicon system.

tem designers. Fig. 2 shows a cross-sectional view of the UNICON recording system.

Retrieval is accomplished by similar helical transport of the tape across the imaging circle of a CW laser of much lower power. Light passing through the holes is detected to produce the same bits that were recorded and verified originally. The power of the read-out laser is insufficient to alter the opaque coating of the tape.

An important element of the memory system is the uniformly-coated Unidensity tape, a proprietary development of Precision Instrument Co., the designers of this new mass memory.

The UNICON process provides a two-dimensional memory system utilizing tape, which does not require stopping to move cards, change circular writing and reading positions on discs, or vary head positions on drums. The UNICON system overcomes the disadvantage of magnetic tape and microfilm storage. Magnetic tape has been increased to about 10,000 bits per square-inch, but magnetic tape is too expensive for a permanent storage medium, and its storage density cannot be increased much more. Furthermore, it loses its magnetic properties over a period of time, and can be erased accidentally. Microfilm in the familiar roll form cannot be read by computers, is still too bulky for extremely compact storage of huge masses of data, and access is slow. And the intermediate step of film-development increases delay, expense, and hazard of loss.

Basic research has been underway for many years on approaches to higher density, highly-stable and highly-accessible mass data storage or "memory" systems. The three principal approaches which have resulted so far involve recording either photographically, or by electron beams, or by lasers. Although these approaches can increase storage density fantastically, they require a costly and time-consuming film-developing step and they provide no way to verify accuracy before the film is developed.

The UNICON process provides the following:

- **Capacity** — the 645 million bits-per-inch is the greatest storage density presently known. A standard 2400-foot reel of UNICON tape could store as much data as 47,500 reels of modern magnetic tape. The entire 44-million-item file of the Library of Congress could be put on 5½ UNICON reels.

- **Speed** — recording rates of 12 million bits per second are demonstrable.

- **Permanence** — the process is suitable for archives. Data in the form of holes cannot be erased, does not fade.

- **Accuracy** — recording is verified simultaneously with writing.

This experimental system was developed under the guidance of Dr. Carl H. Becker, Research Director of Precision Instrument Co., Palo Alto, California. **END**

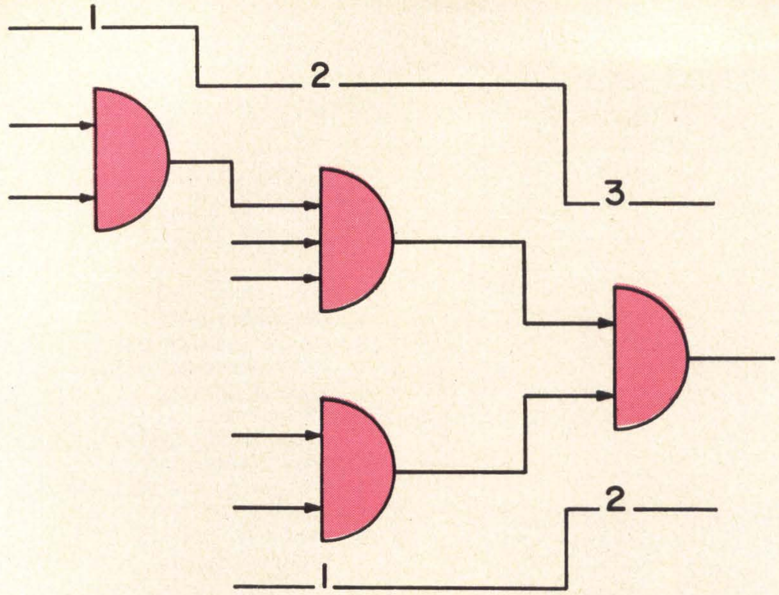


Fig. 1. A three-level logic system.

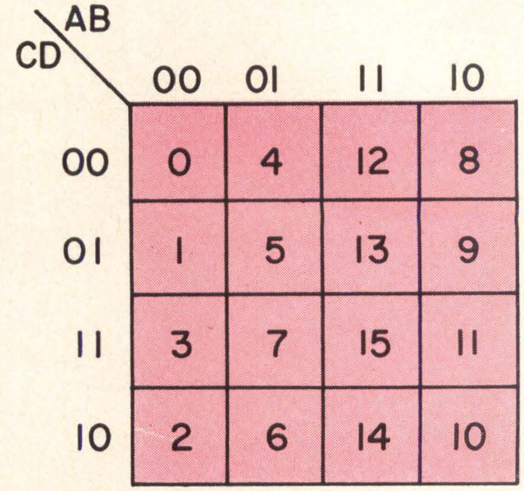


Fig. 2. Decimal description of a 4-variable Karnaugh map.

LOGIC MINIMIZATION BEYOND THE KARNAUGH MAP

ROBERT IRVING LEVINE,

Realtime Systems, Inc., N. Y., N. Y.

This article describes a technique for reducing the number of inputs used to implement a logical function beyond that "minimized" function which results from the common Karnaugh map technique. Use is made of the Karnaugh map and a gain-loss table.

The basis of the minimization technique described in this article is that ONEs (or ZEROs) are added to the Karnaugh map to create a more simplified expression, and these additions are then inhibited in order to preserve the original logical truth. In effect, the simplifications are achieved by allowing the levels of logic to expand beyond the usual two-level logic implementation. The technique is described specifically for 4 variables but may easily be expanded to more than 4.

Definitions

- A unit level of logic is defined as the logical ANDing or ORing of K variables. For example, the circuit shown in Fig. 1 contains two different logical paths. The lower path has 2 levels of logic, and the upper path, which is larger and therefore the determining factor, contains 3 levels of logic.
- The total number of inputs of a circuit is the sum of the inputs to all the AND and OR circuits. The circuit of Fig. 1 contains 9 inputs.
- A subcube is an even number of adjacent squares (of a Karnaugh map) which may be combined for simplification.
- The criterion for simplifying a circuit is that the total number of inputs is reduced.

Simplification

1. Reference all squares of the Karnaugh map according to their decimal equivalents, as shown in Fig. 2.

2. Record the ONEs and ZEROs on the Karnaugh map for the function of interest. Determine the number of inputs resulting from the minimum function obtained from the Karnaugh map.

3. Add ONEs (or ZEROs) to the map to create a more simplified expression; create a map for the corresponding inhibiting function (the added ONEs or Zeros). Repeat for all possible simplifying additions.

4. Create a table (a Gain-Loss table) to determine the modification(s) which produce the minimum input function. Column 1 of the table should list the subcube of the map where ONEs were added. Column 2 should tabulate the difference between the inputs of the

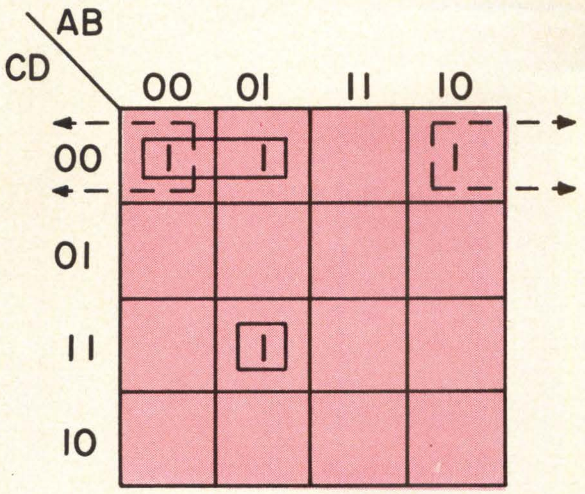


Fig. 3. Karnaugh representation of the function: = f $\overline{A}\overline{C}\overline{D} + \overline{B}\overline{C}\overline{D} + \overline{A}BCD$.

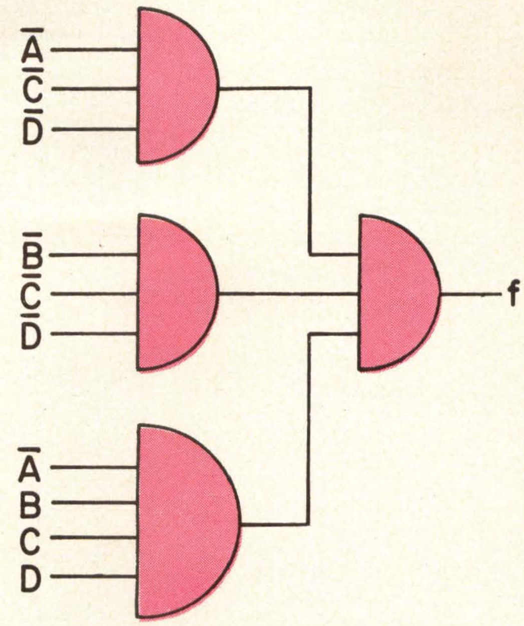


Fig. 4. Circuit representation of f.

modified function (f_m) and the original function(f). Column 3 should tabulate the inputs added by the inhibiting circuit. Column 4 should be the difference between Columns 2 and 3, and is the net loss or gain in inputs due to that particular subcube modification.

5. Choose the subcube resulting in the greatest input loss to be the primary simplification. If there is more than one minimum primary reduction, consider each separately in making a secondary reduction.

6. Perform a secondary reduction by applying the above procedure to the primary simplification (s).

7. The process ends when any of the reduction steps fail to produce a loss in the number of inputs.

Illustrative Example

The Karnaugh representation of the function to be simplified is shown in Fig. 3. The circuit representation of this function, which is shown in Fig. 4, contains 13 inputs. Consider a simplification involving the addition of ONEs in subcube 1, 5, 13, and 9, as shown in Fig. 5(a). The modified function now becomes:

$$f_m = \overline{A}\overline{C} + \overline{B}\overline{C} + \overline{A}BD.$$

The inhibiting function is:

$$f_d = \overline{C}D.$$

TABLE I: PRIMARY GAIN-LOSS TABLE

ZERO SUBCUBES	LOSS	GAIN	NET LOSS(GAIN)
1,5,13,9	3	4	(1)
2,6,14,10	3	4	(1)
12,13,15,14	6	4	2
1,3,9,11	2	4	(2)
3,2,11,10	2	4	(2)

TABLE II: SECONDARY GAIN-LOSS TABLE

ZERO SUBCUBES	LOSS	GAIN	NET LOSS(GAIN)
1,5,13,9	2	4	(2)
2,6,14,10	2	4	(2)
1,3,9,11	1	4	(3)
3,2,11,10	1	4	(3)

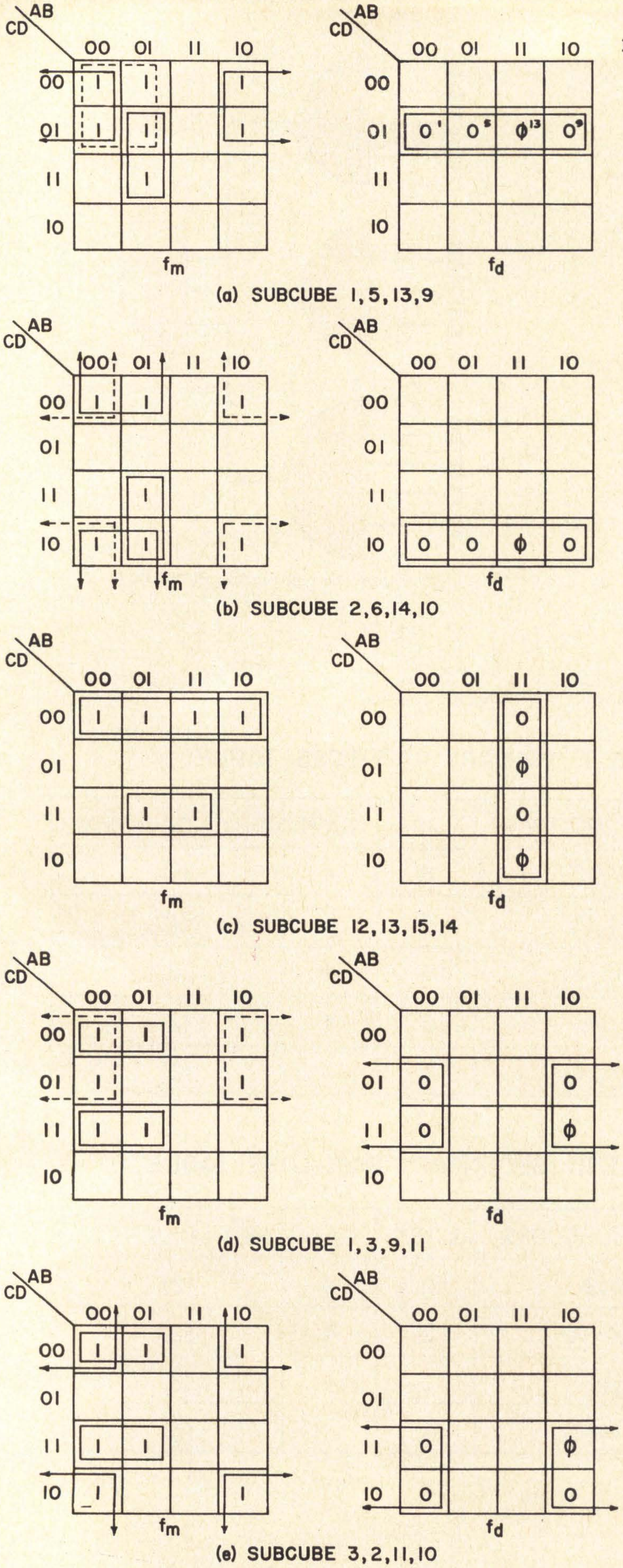


Fig. 5. Primary modifications.

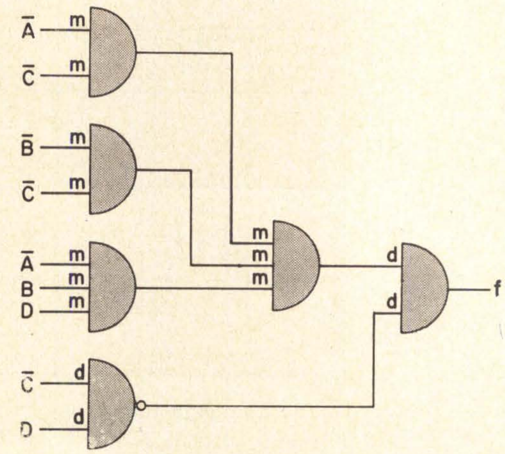


Fig. 6. Subcube 1, 5, 13, 9 circuit.

The circuit representing the function is shown in Fig. 6. The "don't care" states, represented as Ø, in the maps, need not enter into the inhibiting function since no ONEs were added in these squares, but they are used in creating a more simplified inhibiting function. "Don't care" states may only be inserted in those squares not containing a ONE in the original function. Since f_m contains 10 inputs (represented by "m" on the input of Fig. 6) this reduction represents a loss of 3 inputs from the original function. Therefore, "3" is inserted into column 2, rows 1, 5, 13, and 9 of Table 1, a primary Gain-Loss table. The inhibiting circuit requires 4 inputs which are inserted into column 3. The result is a gain of 1 input, which is inserted into column 4, and 3 levels of logic. This modification is rejected.

Let us now examine the simplification involving subcube 12, 13, 15 and 14 as shown in Fig. 5(c). ONEs are inserted in squares 12 and 15 of Fig. 5(c). This produces the modified function of:

$$f_m = BCD + \overline{CD}$$

and an inhibiting function of

$$f_d = AB.$$

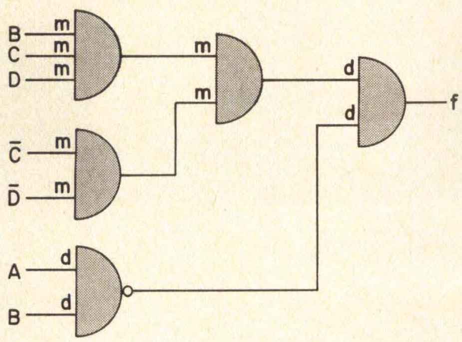


Fig. 7. Subcube 12, 13, 15, 14 circuit.

The resulting circuit is shown in Fig. 7; f_m contains 7 inputs, resulting in a loss of 6 inputs which are inserted in column 2 of Table 1. The inhibiting function, f_d, contains 4 inputs which are inserted in column 3. The result is a net loss of 2 inputs and 3 levels of logic. This arrangement produced the minimum number of inputs and is chosen for possible secondary simplification. Several attempts at secondary simplification are shown in Fig. 8 and Table 2.

For this particular example, further attempts at reduction do not succeed so the minimum circuit is assumed to be that of Fig. 7.

Conclusion

The reduction of the number of inputs through the above procedure must be balanced with the resulting number of levels of logic, since the increased propagation delay of more logic levels may require a lower clock frequency. Also, integrated circuits which have a fixed number of inputs may not warrant the input reduction since all inputs are available. In general, however, fewer inputs imply a more economical implementation of a given logical function. END

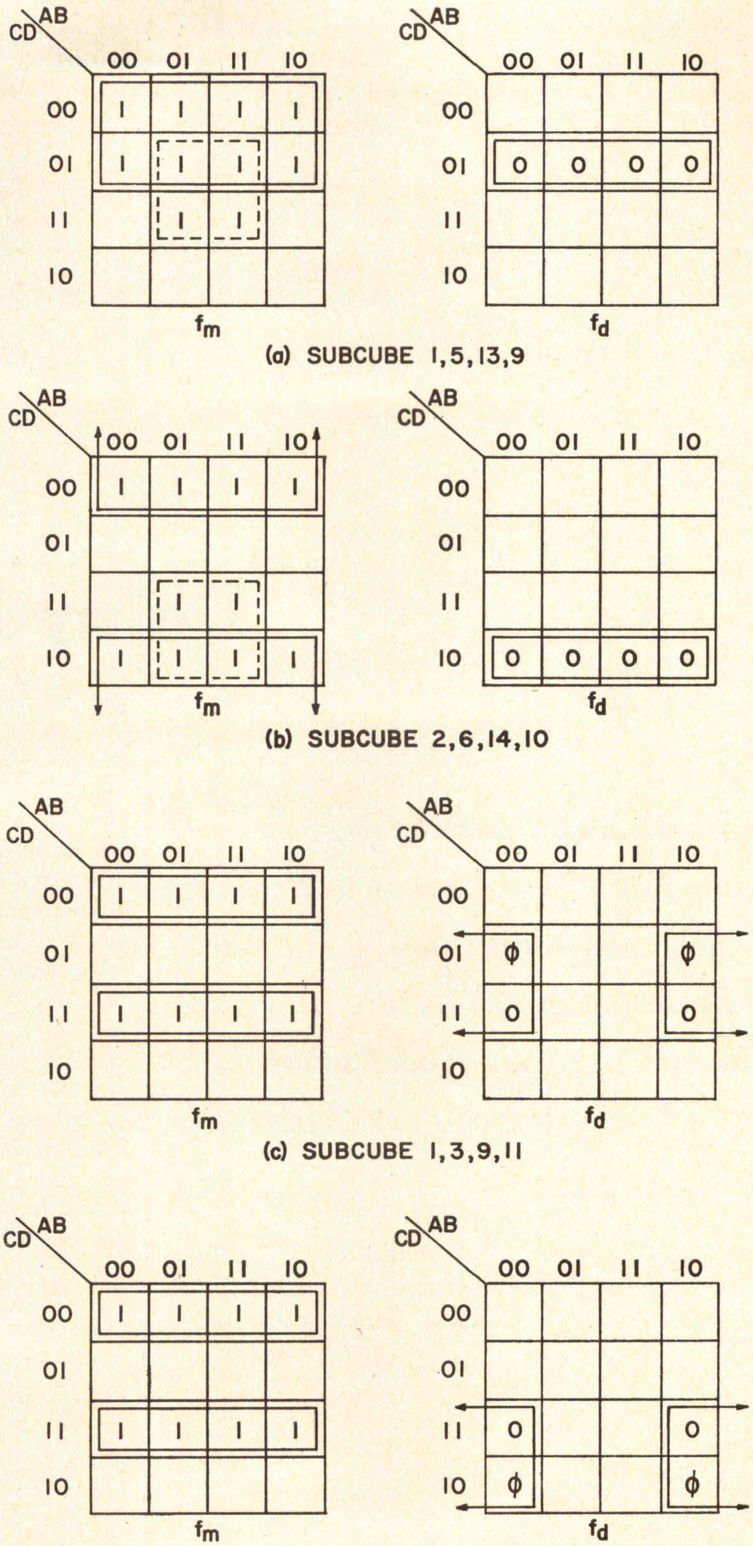
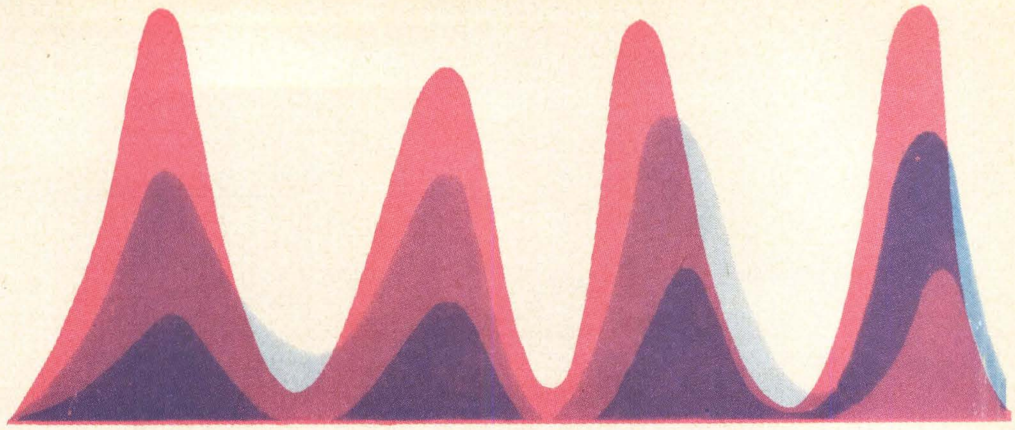


Fig. 8. Secondary modifications.



Delay Equalization in

This article discusses the problems of making voice paths equal to the task of data communications. The basic problems of delay distortion and how one delay equalizer system solves these problems are explained.

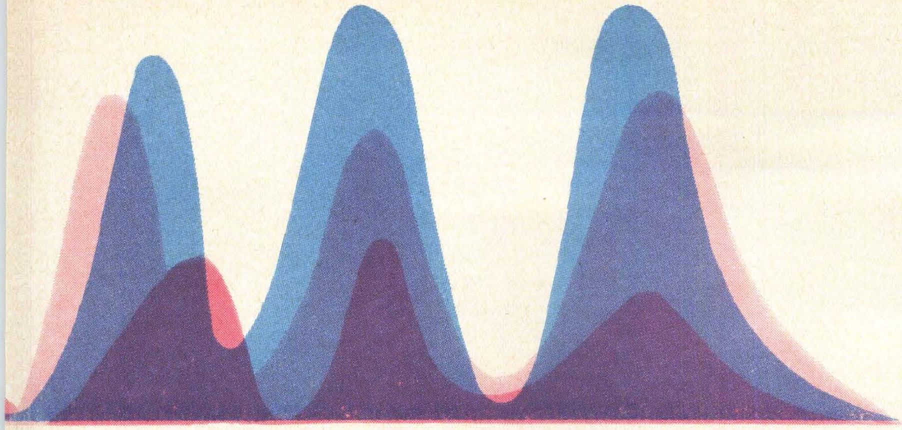
Allen G. Gatfield,
V.P. Research and Engrg.
Rixon Electronics, Inc.
Silver Spring, Md.

The usual pathways for data communications are telephone lines created for voice, and are not quite up to the needs of data communications. In order to bring a telephone line up to the quality required for data, the delay characteristic must be equalized or corrected. A plot of the delay characteristic of a line would be similar to curve A in Fig. 1. The line is equalized by correcting the delay curve to make it flat with respect to frequency. This is accomplished by adding a series network which has the opposite or complementary delay characteristic, as in curve B of Fig. 1. By adding the network in series with the original line, the composite circuit or equalized line having a flat delay characteristic is obtained, as illustrated by curve C of Fig. 1. This correction would make the line suitable for high-speed data communication.

This is the basic problem and solution. It seems simple. But there are a number of elements in the problem that make it complex.

Design Problems

First, there is a class of problems associated with the realization of the delay characteristic of curve B in Fig. 1. Since, in the general problem presented above, we have placed no limit on the given curve A, there is no limit to the shape required of curve B. Even if we place certain limits on the maximum deviation of curve A, as is so often done in specifications for delay equalizers, we are still faced with the fact that curve A may have any slope and thus requires that curve B have an equal and opposite slope. Intuitively, we realize that this is not possible with a finite number of real networks. Therefore, there will be certain inherent limitations to the shape of curve



Data Communications

B which will have to be taken into account before we consider the nature of networks available to generate curve B.

We have not yet considered the amplitude characteristic of the given line. If, to simplify the problem, we consider only the delay characteristic, it must nevertheless be apparent that the networks making up the delay characteristic of curve B must be flat in amplitude. Simple lead-lag networks or tuned circuits cannot be used to generate the delay function because they also have their own characteristic amplitude functions. There is only one class of network which can be used to generate the delay correction characteristic — the all-pass network. An all-pass network will have a flat amplitude response if perfectly implemented; however, perfection in this case would require zero loss components, that is, capacitors with a dissipation factor of zero and inductors with infinite Q. Detailed mathematical consideration of all-pass networks will reveal that the effects of nonperfect components are greater for some network configurations than for others. Thus, we find certain limitations on the portion of the total population of all-pass networks which may be used. These limitations are functions of the quality of the components which are to be used, and of the amplitude characteristic variations which we will allow.

If we now consider the restricted class of networks remaining, we find that the basic delay characteristics of all all-pass networks are similar. A set of delay characteristics for such an all-pass network is shown in Figs. 2, 3, and 4. Fig. 2 is for a network tuned to 600 Hz while Figs. 3 and 4 show the characteristic for the same network tuned to 1600 Hz and 2800 Hz, respectively. The

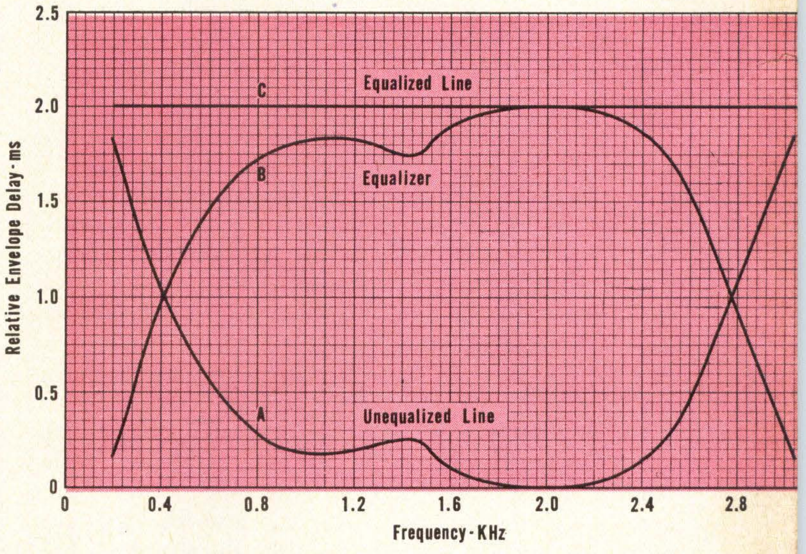


Fig. 1. Delay characteristic of a voice circuit.

network shown here is an active circuit with an adjustable delay. The numbers 1, 5, and 10 on the curves correspond to three different settings of a continuous control.

There are several important features to be noted from these curves. First, these curves are typical of all all-pass networks, whether active or passive. Note that the curves do not simply scale down in delay, but that the delay characteristic gets broader as the peak delay (control setting) is lowered. This is a fundamental characteristic resulting from the fact that the total phase shift from

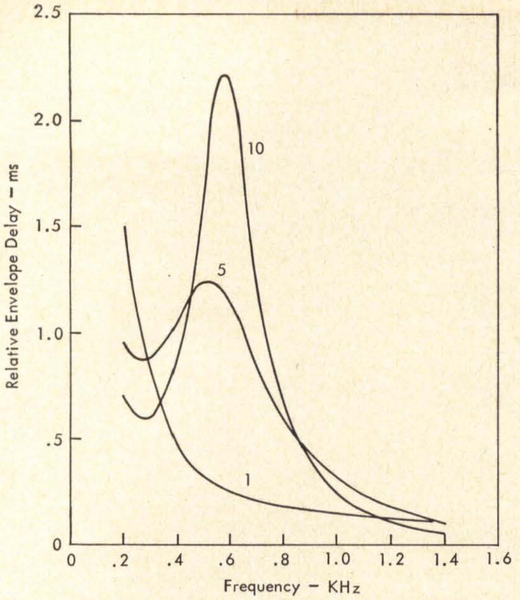


Fig. 2. Delay characteristic, 600 Hz equalizer.

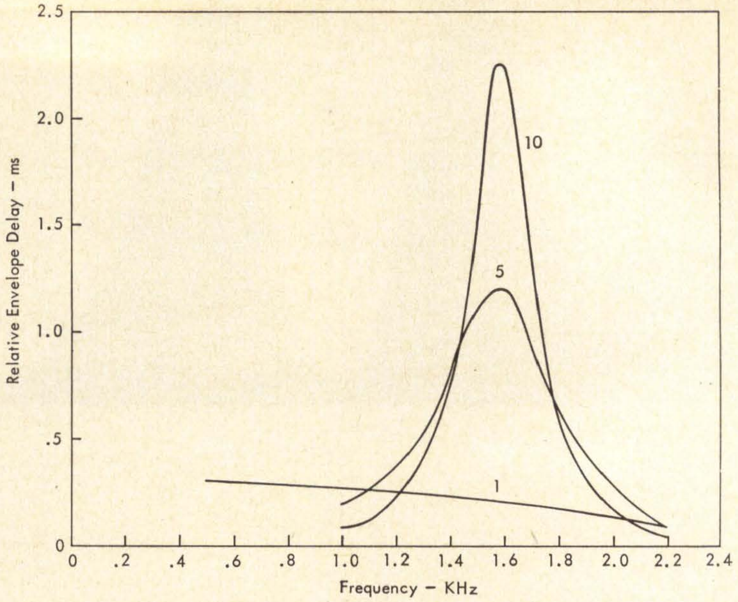


Fig. 3. Delay characteristic, 1600 Hz equalizer.

zero to infinite frequency remains constant (at 360° for the network shown). It is obvious that one limiting factor on our ability to obtain any correction curve is this fixed relationship between slope of delay characteristic and maximum delay.

(It should also be noted that the higher the delay peak for a given network, the more difficult it will be to maintain constant amplitude. Thus, the amplitude limitation discussed above results in a limitation of the range of adjustment of the network which may be used.)

Another important feature of the delay characteristics in Figs. 2, 3, and 4 is the lack of symmetry. In Figs. 3 and 4 this lack of symmetry may not be obvious without careful study, but it is pronounced in Fig. 2. This lack of symmetry is not due to faulty implementation or to non-perfect components, but is a basic characteristic of all all-pass networks. It can be minimized by the proper basic network configuration, but remains a problem in implementing a delay characteristic to correct a given line.

Another factor, not obvious in the figures but which can be shown mathematically or by careful large scale plotting, is that when two or more such networks are connected in series, their delay characteristic will not necessarily be flat. In other words, the shape of the curves are such that a perfectly-flat delay curve will not be obtained in the overlap region between the peaks of the adjacent networks. In general, the resultant composite delay curve does tend to become flatter as the amount of overlap increases. This, of course, indicates that the conditions for maximum flatness, or freedom from ripple, are opposed to those for correcting steep slopes in the given curve.

Now two final points. It may be obvious from what has been stated above that the larger the absolute amount of delay which must be corrected (the maximum deviation of the given delay characteristic between specified limits of frequency), the greater the problem of ripple will be. If we attempt to correct too great a relative delay, we may find that the corrector all-pass networks themselves have introduced a ripple in the composite or "corrected" delay characteristic that is greater than the system equalization tolerance. Furthermore, the number of all-pass networks required increases in direct relation to the amount of delay which must be corrected and the bandwidth over which it must be possible to make the correction.

Measurement Problems

The foregoing discussion, while not complete, illustrates the class of problems which are associated with the realization of a given delay correction characteristic. There are, however, other problems to be considered. One problem is related to the original delay characteristic for the given line (curve A in Fig. 1). *How is this characteristic obtained and to what accuracy?* One might also ask how the corrector characteristic B is to be measured, however, we will see that the problem of measuring a passive or active delay corrector is less severe than that of measuring the original line.

The factor which introduces the greatest problem in the measurement of the delay characteristic of a real line is frequency translation. Since most long line telephone service is provided by carrier facilities, the lines of interest to the data communications system engineer will almost invariably exhibit some degree of frequency translation. The effect of this is to make each discrete frequency component of an input waveform ($A \sin \omega t$) be recovered at the receive end of the line with a small offset $\Delta\omega$, i.e., $[A \sin (\omega + \Delta\omega) t]$. The offset $\Delta\omega$ is the same for all frequencies in the band. The effect is to make it impossible to measure the phase response directly. This is the principal difference between the problem of measuring the actual line and that of measuring a correction network, since the correction network does not, in general, exhibit frequency offset and a direct phase measurement may be made. A detailed consideration of the functioning of a delay measuring set designed to operate over real lines having input and output separated

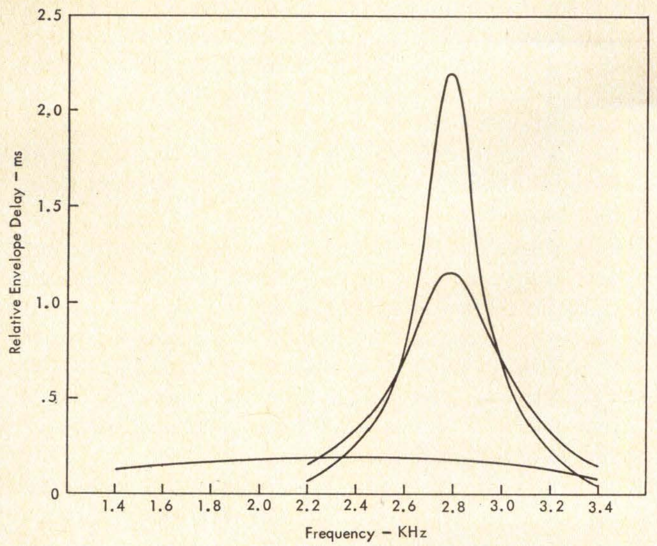


Fig. 4. Delay characteristic, 2800 Hz equalizer.

by large distances is beyond the scope of this article. It should be noted here, however, that the measurement is not a simple one to make, that it requires some method of obtaining a measurement reference at the receive end, and that accuracies of greater than 50 μsec are not generally claimed.

Combining and Adjusting Problems

A third class of problems to be considered is related to the mechanism for obtaining the correction delay characteristic needed. Assume that an accurate curve of envelope delay vs frequency for the given line has been obtained. This curve may be inverted to yield the delay corrector curve required. Further assume that we have designed a finely-incremented range of suitable all-pass networks having the sort of curves shown in Figs. 2, 3, and 4. *How, then, will we select and combine the necessary networks to provide the best equalization?* (We have already established that a perfect equalization may not be possible.)

If we consider first the actual physical method of combining, we see that many variations are possible. We might select fixed networks from a large selection and permanently wire these into the circuit. Or, we might use a smaller number of variable or adjustable networks permanently wired together to make up an adjustable equalizer. The possibilities are endless, and unfortunately, they are all compromises of the various factors of desirability which might be considered. If it is elected to use a group of adjustable sections connected together to form an adjustable delay equalizer, we still must determine the degree of adjustment to be provided, whether to provide adjustability both in frequency and in peak delay, whether these factors should be adjustable by increment or continuously adjustable — to how fine a degree, over what range, ganged or separate controls. All of these are engineering decisions; compromises among the factors of cost, complexity, degree of correction sought, and ease of operation.

Ease of operation is a complex problem in itself. This is so because it leads us to the question of how we will actually make the adjustment. (Whether it is made by network selection or by adjustable networks, we must make an adjustment and then determine if the desired result has been reached.) The adjustment can be made with successive alternation of measurement — adjustment, measurement, adjustment — using a delay set to measure the entire circuit including the delay corrector. The corrector is adjusted until the composite line measurement falls within the specification limits. The adjustment can also be made by monitoring the data modem in actual operation and adjusting for the least distortion in the recovered modulation. This is called the "eye pattern" method since the recovered modulation may best be observed by synchronizing the oscilloscope with the receive clock and viewing many overlapping traces which form an eye-shaped pattern. The eye pattern method provides an easy and quick adjustment but does not assure any given limits on the delay curve. For more detail on this subject, the reader is referred to another paper by the author.[1]

In summary, we see that the problem is not one but many inter-related problems, and that delay equalization calls for many compromises; no best single solution seems possible.

The Rixon Solution

One solution is embodied in the Rixon DDAE-4 delay equalizer. This equalizer, like all others known to the author, is a compromise, however, it has been proved to be an extremely valuable tool in many data communications problems and achieves a large measure of flexibility with reasonable cost and ease of operation. The equalizer consists of twelve active delay sections. Each section is fixed in frequency and the twelve sections are distributed evenly across the frequency band. Each section has a separate delay control, allowing adjustment of delay in each section of the band. Each section control has a switch which, at extreme CCW rotation, removes the section completely.

The individual active sections employed in this equalizer are believed to represent a significant improvement over earlier delay equalizers. They provide a more nearly-flat amplitude response even at high delay settings, and they provide a more symmetrical delay characteristic. The actual measured delay characteristics for three selected sections are those shown in Figs. 2, 3, and 4.

The number of sections used reflects consideration of many factors. A lower limit on the number of sections required can be found from basic design equations by assuming a constant delay across the frequency band, specifying that we expect to correct delay up to 3 ms across the band from 400 to 3000 Hz, and knowing that each section contributes 2π radians of phase shift. We find that a minimum of 8 sections are required.

However, there are other factors to consider, the most significant of which are the magnitude of the delay and amplitude ripple which will be acceptable in the equalized line. As already stated, the shape of the delay vs frequency curve for each section is not ideally-suited to the concept of combining sections to obtain a flat delay.

A flatter delay is obtained when the delay sections are not adjusted for high Q but are allowed a significant degree of overlap. Furthermore, the amplitude response of each section shows a greater departure from the flat condition as the Q of the section is increased. When limits of 80 μs on delay ripple and ± 1 db on amplitude are established for the overall performance of the equalizer, we find that the number of sections required is increased from 8 to 12.

Once the number of sections had been established, the question of the number or type of controls or variability to be provided for each section was considered. Basically each section can be varied in center frequency and Q, or peak delay, at center frequency. It was felt that fixed frequencies would be adequate; with the twelve sections spaced across the band of 2600 Hz, there would be a section approximately every 200 Hz and frequency adjustment could be obtained, in effect, by simply selecting the sections nearest the point at which it was desired to add delay. Therefore the center frequencies of the sections are evenly spaced across the band and are not adjustable.

Then the number of delay controls had to be considered. It is possible to adjust delay across the entire band with one control, by ganging the controls of all 12 sections. Or, we might combine the controls of 2, 3, 4, or 6 sections to provide 6, 4, 3, or 2 controls, respectively. This is a question of balancing simplicity and ease of adjustment with maximum flexibility and greatest equalizing ability. The Rixon DDAE-4 was intended to provide accurate equalization of lines where other equalizers had failed, therefore maximum flexibility was required, and twelve separate controls are provided.

Since each section's delay control was provided with a switch which removes delay sections completely when the control is turned fully CCW, it is not necessary to adjust all twelve controls in most cases. One simply uses only those sections corresponding to a portion of the band where added delay is required, and turns all other sections off (which leaves only a constant delay or linear phase amplifier in the circuit). Many times, only one or two sections are required and often it is possible to obtain a better correction with only one or two sections than could be obtained by using all sections. This key feature of this equalizer means that it is not always a 12-control equalizer, but it may be so in the extreme case where it is required.

Operational Use

The question of operational use was touched on briefly in the section above. There are, basically, two different ways in which an equalizer such as the DDAE-4 may be employed to solve the data communication system problem of delay equalization. It can equalize the delay characteristic of a given line, so that, after equalization, the delay characteristic falls within specified limits; it may be employed to correct the line so that a given data modem performs within the system limits. If the first choice is followed, it is necessary that some form of delay measuring equipment be employed, since the first step in the procedure is to measure the delay characteristic of the line. This is a rather tedious process, requiring a technician at each end of the line to be measured and a voice communications link in addition to the line being measured. The result of such a measurement is a table or graph showing delay vs frequency. If the delay characteristic is not within acceptable limits, the measured data will indicate the delay correction required. If the line curve shows a dip at 1000 Hz then the delay control for 1000 Hz should be advanced to insert delay at that frequency.

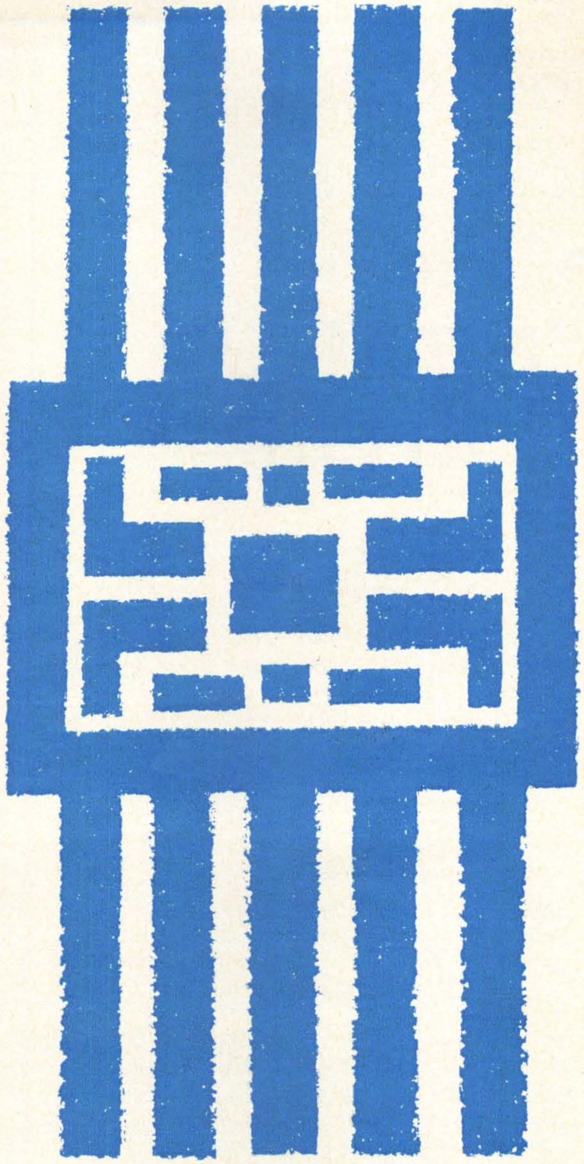
Several operational variations are possible at this point. If both transmit and receive portions of a delay set are available at the site, the technician may connect the delay set to the delay equalizer alone and adjust the equalizer until its delay characteristic is the complement of that of the line, and would, therefore, be expected to correct it to a constant delay. The equalizer is then connected in series with the line and the "corrected line" re-measured to assure that equalization within the set limits has been achieved. Alternatively, the technician may connect the equalizer directly to the line and make adjustments while measuring the composite of real line and equalizer. In this method, once the equalizer is adjusted the job is complete and no final checking measurement is required. However, if the line is a difficult one to correct, the first method may require less time since measurements made locally are much easier and quicker to make than those made over the real circuit. Other variations of these two methods may also be used.

In delay equalization, to obtain specified modem performance, one is not concerned with any actual measurements of the delay characteristic of the line. The modems to be employed in the system are connected to both ends of the line, and random data is introduced at the modulator or transmitter. (Some modems have a random data source as a built in feature.) At the receiver, an oscilloscope is used to view the demodulated data with sync obtained from the receive clock since clock phasing is recovered by the modem. The result is many overlapping traces of the recovered random digital data in band-limited form. This is the "eye pattern," so named because of its resemblance to the human eye.

When the modem is first connected to the line, the received eye pattern may be so poor as to be barely recognizable The delay equalizer, connected in series with the modem and line, is now adjusted to improve the eye pattern, that is, to make the pattern look more nearly as it does when the modem is operating back-to-back or with a perfect line. The adjustment is one of trial and error, however, anything that is known about the line characteristic or the modem may reduce the amount of trial and error. For example, the likelihood that this is a normal line is helpful since we expect the normal line characteristic to have the typical U shape, and we know that we will need to add more delay in mid-band than at either end. Any more exact information we may have about the location of dips or bumps in the delay characteristic will further reduce the range of likely settings of the controls.

Knowledge of the modem is also helpful in that we know the modem is more sensitive to variations in envelope delay near the carrier frequency. Starting with adjustments of delay near the carrier frequency will often make the trial and error process easier.

Almost every engineer who uses our IC bandpass amplifier says it's better than a discrete amplifier.



(Charlie Wisgard says it's just as good.)

But, at the price, we know that you won't be able to get a discrete or IC bandpass amplifier that can out-perform the PA 7601.

Look at the performance. It has a gain control circuit which provides 12 db of gain reduction with typically less than 10% variation in output terminal impedance. In broadband applications, gain control from 0 to 12 db produces negligible effect on bandwidth over a frequency range of 30 to 150 MHz.

Our PA 7601 is your best solution to high-frequency phase and amplitude distortion problems. For narrowband applications, you can use a bandpass filter or selective feedback components.

Don't take our word for it. Try the PA 7601 for yourself. It's available in 10-lead flat pack or TO-5 can. Temperature range: $-55°C$ to $100°C$.

Call or write: **Philco-Ford Corporation Microelectronics Division Sales Offices:** 2920 San Ysidro Way, Santa Clara, California (408-245-2966) / 999 North Sepulveda, El Segundo, California (213-772-6226) / Northwest Industrial Park, Second Ave., Burlington, Mass. (617-272-1600) / Benson Manor, Suite 114B, Washington Lane, Jenkintown, Pa. (215-885-0430) / 1215 Drew Street, Clearwater, Florida (813-446-0124) / 815 Connecticut Avenue, N. W., Washington, D. C. (202-298-7810) / Suite 208, 700-108th St., N. E., Bellevue, Wash. (206-454-5061) / New York, N. Y. (212-244-1373).

PHILCO Ford

PHILCO-FORD CORPORATION
Microelectronics Division
Santa Clara, California • 95051

CIRCLE NO. 41 ON INQUIRY CARD

The principal advantage of the eye pattern method is that it is fast, effective, and requires little extra equipment. The principal disadvantage is that when the adjustment has been made so that good performance results, no knowledge of the corrected line characteristic is available. This may not be immediately apparent but it is due to the fact that variation in conventional envelope delay normally specified for data lines is not directly related to distortion in the recovered modulation. The relationship is rather complex and a given degree of eye pattern distortion may result from an unlimited number of different delay characteristics.

REFERENCE

1. Gatfield, Allen G., **"Delay Distortion in Telephone Lines,"** 1961 IRE International Convention Record, Volume 9, Part 8, Page 109.

GOVERNMENT REPORTS ★★

BAR-MULTIPLIER

A very simple device called a bar-multiplier was recently invented in China for effecting numerical multiplication, division, and extracting square roots, all without the use of a multiplication table. Invented by Yu Chan-Hsan, this bar-multiplier is to the process of multiplication what the abacus is to addition, and it is becoming part of the standard tools of China. The Mitre Corp. explains the bar-calculator as a prototype of a new idea and then generalizes it to the multiplication of many numbers so the numerical computation of the N-th root becomes simple and fast. Application of the principle of the prototype in data processing equipment gives the possibility of reducing computing time with some increase in computing elements. For the generalized case, further reduction is possible by a further increase of the computing elements. The key lies in the separation of the pure multiplying operation of individual digits from the carrying-over process, which can be performed in the subsequent adding step.

Order from Clearinghouse, U. S. Dept. of Commerce, Springfield, Va. 22151. Order No. AD-625764. Price: $2.00.

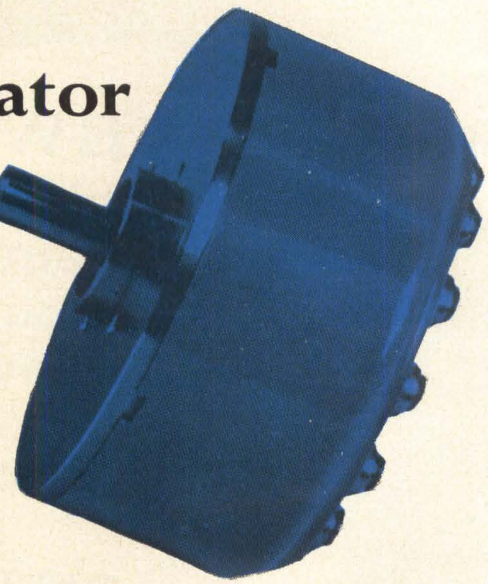
TWO-WORD BINARY CODES

A table of 1800 two-word binary codes with word length up to eight has been prepared by Parke Mathematical Laboratories. Their report gives information about the codes' capabilities for error-correction and for decodability with finite delay. The work is of interest for theoretical studies and for the construction of larger codes. The Parke report notes that two-word codes are unimpressive by themselves. Their importance and the reason for the table, lies in the fact that every two-word subcode of an error-correcting code must also correct the same number of errors, and any two-word subcode of a code which is decodable with finite delay, must also be decodable with infinite delay. Hence, two-word codes are the basic building blocks of all larger codes.

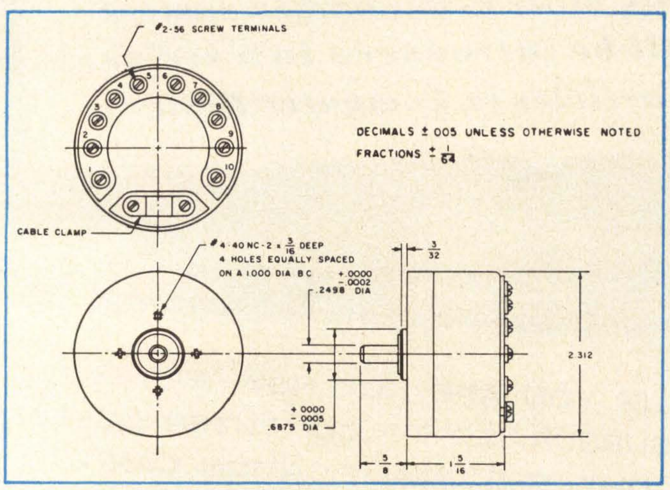
Order from Clearinghouse, U. S. Dept. of Commerce, Springfield, Va. 22151. Order No. AD-621-486. Price: $3.00. Microfiche: 75 cents.

DRC-77

for applications requiring-
Incremental encoder
Bidirectional pulse generator
Shaft-angle transducer
Digital tachometer



For years systems designers have been waiting for digital components that compete head on with analog devices and offer proven in-service operational reliability. The new DRC-77 shaft-angle digitizer has this kind of performance, and at a price level that will meet your costing requirements for commercial equipment. Designed for simplicity and reliability, the DRC-77 is especially suited to laboratory, test area, and general industrial environments. **Resolution:** up to **4,096** pulses per shaft revolution. **Accuracy:** down to **2.6** arc minutes. **Starting torque: 0-1** oz. in. **Output signal levels: 200 mv** peak to peak sine wave, or **6 volt** square waves. Two configurations are available: One provides dual channel, quadrature-phased quasi-sinosoidal output signals of up to 1024 cycles per shaft revolution; the other provides dual channel, quadrature-phased square waves. A bidirectional pulse multiplier card is available to produce (by various interconnections) one, two, or four output pulses per square wave cycle. A once-per-revolution **zero reference** pulse is also available.



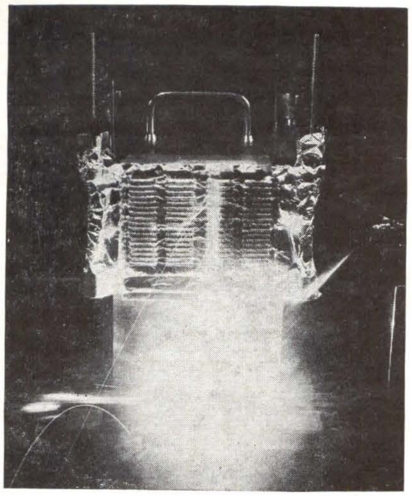
For more information on the versatile new DRC-77 encoder, write for brochure DR6-1066 with detailed performance charts, specification tables, and dimension drawings.

DYNAMICS RESEARCH CORPORATION

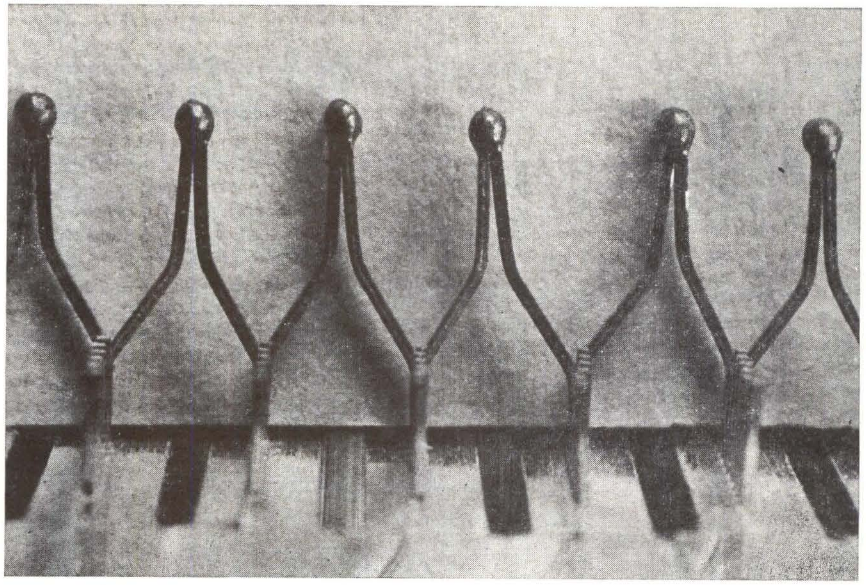
The Components Department / 38 Montvale Avenue, Stoneham, Massachusetts 02180

Phone: (617) 438-3770

CIRCLE NO. 43 ON INQUIRY CARD



As a memory array is welded with the electron beam process, an entire column of terminals is struck by the beam in a single operation. Each column is welded in sequence as the array passes automatically through the electron beam.



This is a magnified view of the welds made by the electron beam welder. The terminals are joined only at the tips with little or no material flow beyond the ball-shaped nugget.

NEW PRODUCTION TECHNIQUE — ELECTRON BEAM WELDING OF MEMORY ARRAYS

A sharply-focused beam of electrons is being used to perform tiny precision welds on critical electrical connections for computer memory arrays. This application of electron beam welding now being used on production lines at IBM's Kingston, N.Y. plant is believed to be the first such use of this technique in manufacturing computer memories. The beam welder is used to connect the terminals of ferrite core planes with those immediately above and beneath them in a memory array. Using the electron beam technique, these precise welds can be done in a continuous operation. Conventional welding normally requires that each terminal be welded individually.

IBM manufacturing engineers have adapted a Hamilton Standard Model W-2 Electron Beam Welder. The following are the operations it performs. Electrons are thermionically emitted from a cathode (a heated tungsten wire filament) and accelerated toward the anode by a high potential difference existing between these elements. A control grid, located between the cathode and anode, controls the density of the beam and shapes it so that it is directed toward a hole in the center of the anode. A wide variety of beam powers is available.

The accelerated electrons pass through the hole in the center of the anode and continue in a straight line path. Traveling downward, they pass through a magnetic lens and deflection coil. The magnetic lens focuses the beam to points from about one-half inch to 25 inches below the top of the vacuum chamber. The deflection coil is used to deflect the beam in a variety of patterns.

An X-Y positioning table, located in the chamber, positions the column of terminals to be welded under the electron beam. The table can be traversed at rates from about three inches to 120 inches per minute in either the X or Y direction. The welding process is performed under vacuum to reduce energy loss and scatter loss due to collision with air molecules at higher pressures. Normal operation takes place at pressures less than 10^{-4} mm Hg. The welding parameters are determined primarily from experimentation and experience. Depending upon the results obtained, the initial settings are then varied in a wide range until reasonably good parameters are found. These parameters are then ranged, one at a time, in both positive and negative directions until an optimum setting is obtained.

The proper beam current assures full penetration of each column of terminals. After the beam current has been selected, the traverse rate is selected. This combination is what creates the uniform weldments throughout the memory array. A traverse rate which is too slow results in a match-head type weldment with a considerable amount of material overflow along the terminal length and between the terminal pairs. A high rate tends to draw the molten material out sideways resulting in an oblong "ball." The proper rate results in a uniform ball-shaped nugget located directly at the tip of the terminal pair.

An optical viewing system enables the operator of the welder to locate the target with respect to the electron beam. The operator may continuously observe the welding procedure and maintain full control of it. END

NEW AUTOMATIC MEMORY TESTER

One Standard System Can Test 2D, 2½D, and 3D Configurations

A new precision testing system tests core memories by operating them in the ultimate system environment. Memory response is measured at each address under imposed worst-case electrical and logical conditions. The ability of each bit to store data with prescribed reliability is verified. The modular format of the system is shown in the simplified block diagram of Fig. 1, which illustrates a standard configuration for testing 2D, 2½D, 3D, and a wide range of sophisticated memories having complex sense and digit wire geometries.

The program generator module establishes the prescribed current pulse program. In 3D memories this may be a simple two-step, read/write program. In 2D memories and memories using multiapertured ferrites, a complex eight-step pulse sequence may be programmed. Current drivers are adjusted for specified amplitude, rise and fall time, pulse position, and width.

The programmed switch driver modules, interposed between scanner and current/sense switches of each axis, lend a switching versatility to the system. Using prewired, programming plugs, the access switches may be operated in practically any sequence — maximum address left or right, block switching for memories with built-in diode decoding, block switching of sense wires, etc. The switches connect to the memory under test through front panel connectors.

The pattern generator module, operating on digit drivers or through the logic of the program generator, establishes the basic pattern of stored data in the memory. Frequently-used, worst-case patterns are selected by a single switch setting, while special patterns are established by diode plug boards and toggle switches.

Sense switch outputs are coupled to the differential sense amplifier module which is designed to reject a high-level of error-generating common mode noise and still provide the very wide bandpass necessary for testing of sub-microsecond switching memory cores.

2½D Memory Analysis

The demanding switching requirements of the 2½D memory are readily satisfied by the testing system using either solid-state or reed relay switches on both the X and Y axes. X-axis switches access through decoding diodes or direct, while Y-axis switches are connected as reversing switches.

In the example shown in Fig. 2, when X-axis relay 1 is closed, current flows into memory line 1 and returns through memory line 2. This current is coincident with the X-axis current at the intersecting core on line 1 and is anti-coincident with X-axis current at the intersecting core on line 2. Therefore, only the core on line 1 is selected. When X-axis relay 2 is closed, the current in the Y line is reversed with respect to the X-axis. Accordingly, currents are coincident at line 2 and are anti-

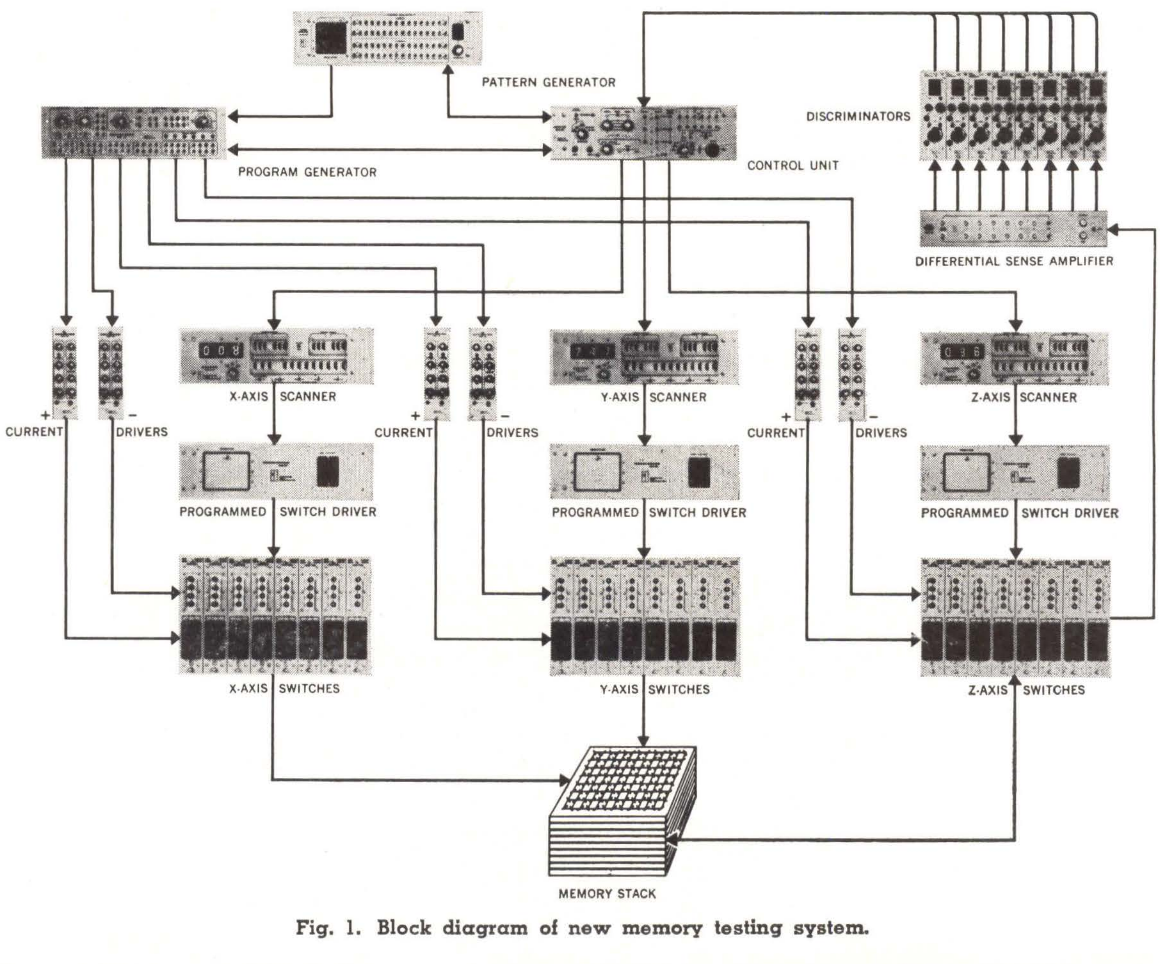


Fig. 1. Block diagram of new memory testing system.

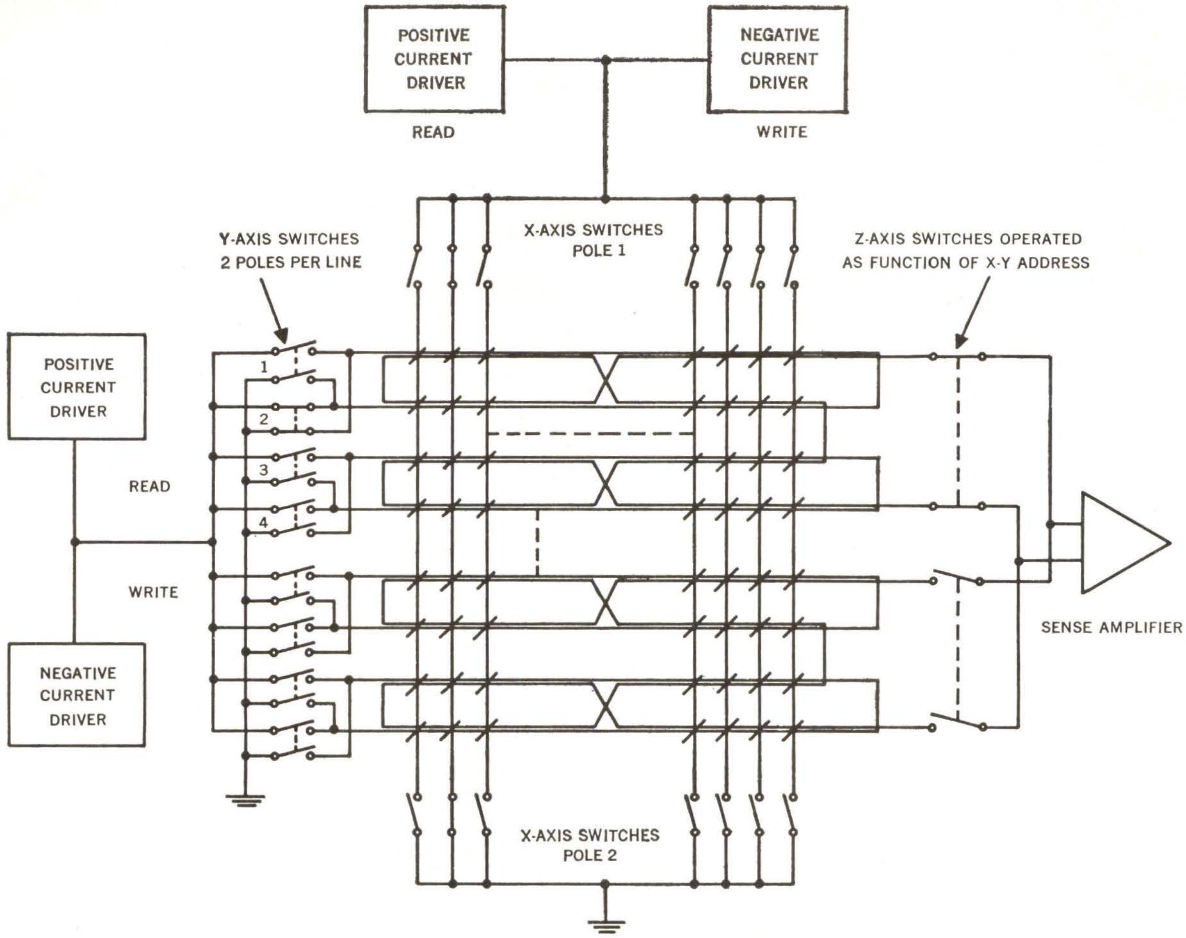


Fig. 2. An example of testing a 2½D memory.

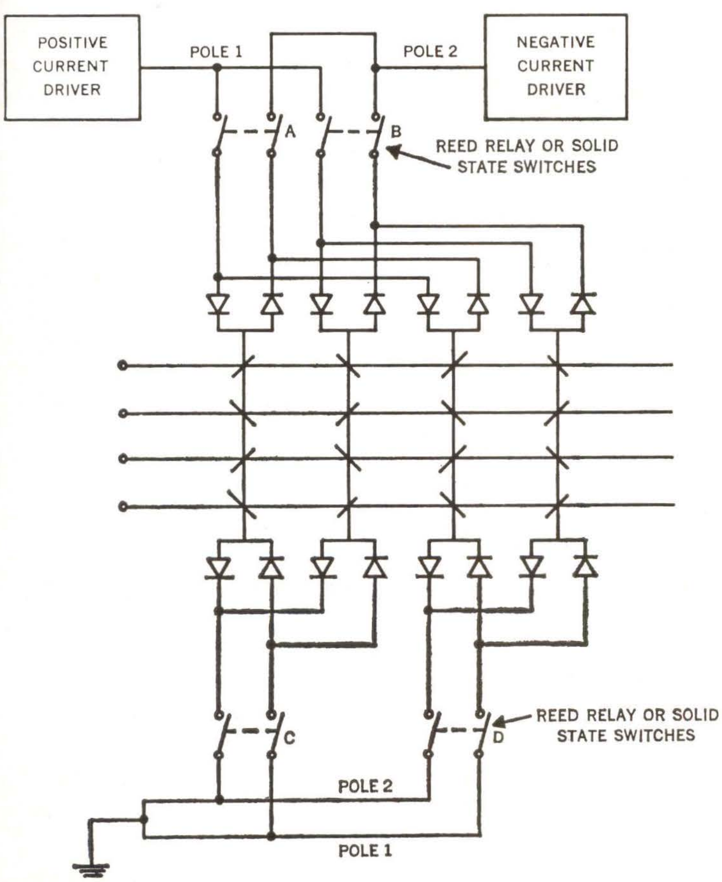


Fig. 3. Testing memories that have built-in diode decoding.

coincident at line 1, selecting the core on line 2 only.

The test shown here uses reed relays on the Y-axis. Since four poles per address are available using reed relays, two of these poles may be used to switch the sense wires as a function of Y address. If the higher scan speeds provided by the solid-state switches are desired, Z-axis reed relay switches can be programmed to operate at the three cross-over points set up on the Y-axis address scanner.

Built-in Diode Decoding

Memories which are designed with built-in decoding diodes are driven by the system using either reed relays or solid-state switches for access. To accommodate such memories, the system is first programmed for double pole operation to provide separate switch closures for both drive current polarities. The system is then programmed for dimensions of the diode matrix, such as 16 x 16 or 8 x 32 for a 256 line axis. Both of these programming steps are executed in the programmed switch driver.

In the simple example shown in Fig. 3, switch combinations A-C, B-C, A-D, and B-D select the four vertical access lines in consecutive order. Various other matrix dimensions are possible within the 256 address decode capability, including 32 x 8, 10 x 25, etc.

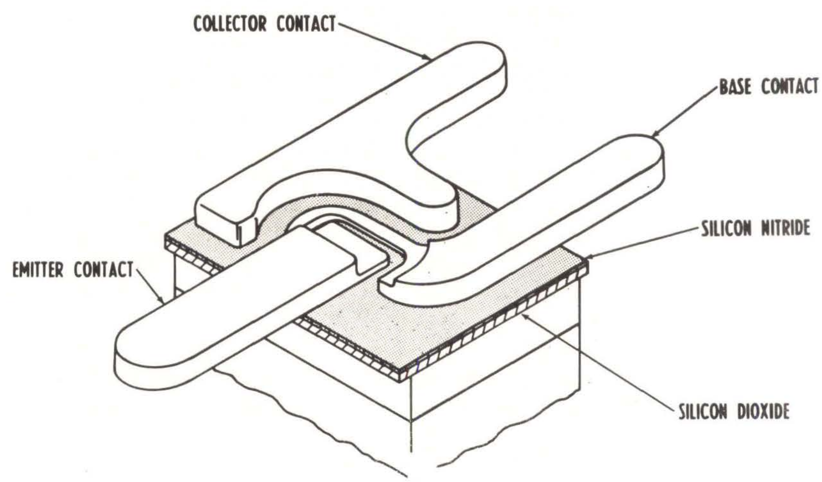
The new testing system, Model M-201, was developed by Computer Test Corp., Cherry Hill, N. J. **For more information on the new system:**

Circle No. 106 on Inquiry Card

NEW TECHNIQUE DEVELOPED FOR SEALING SEMICONDUCTOR DEVICES

A sealing technique that gives silicon semiconductor devices greater reliability than the usual, expensive, vacuum-tight encapsulation has been developed at Bell Telephone Laboratories. The seal — a materials system consisting of a metal-insulator-semiconductor combination — is formed by applying a layer of silicon nitride along with beam lead contacts to the silicon dioxide layer of the semiconductor device.

The new technique brings "batch processing" to the encapsulating step for transistors and integrated circuits, that is, thousands of devices can be encapsulated simultaneously while they are still on a single silicon slice. With standard encapsulation techniques, the slice must be cut into individual integrated circuits, and each circuit is encapsulated separately (usually in vacuum-tight metal cans for high-reliability devices).



A new junction seal developed at Bell Telephone Laboratories is formed by applying a thin layer of silicon nitride along with beam lead contacts to the silicon dioxide layer of the semiconductor device. Shown above is the configuration of the seal on a typical epitaxial silicon transistor.

To deposit the silicon nitride layer onto the silicon epitaxial devices, the silicon slice is first heated to 875° centigrade in a closed chamber containing pure hydrogen gas. Then a mixture of two gases — silicon hydride (diluted in hydrogen) and ammonia — is introduced into the chamber. When this mixture makes contact with the heated slice, the heat causes the two gases to react chemically to form silicon nitride. The silicon nitride adheres to the slice, forming a protective barrier against the penetration of sodium and other metallic ions.

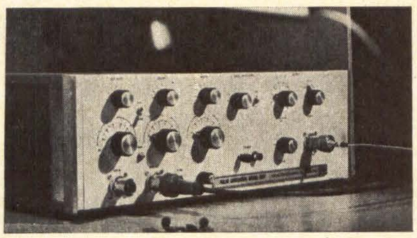
The beam lead contacts — multilayer combinations of a titanium-platinum-gold alloy and platinum silicide — are also applied to the devices while they are on a single slice of silicon. The contacts form a strong chemical bond with the silicon nitride layer, thus sealing the required contact areas against ion penetration. Beam lead contacts were invented by M. P. Lepselter of Bell Laboratories and first reported in 1964.

In order for the beam lead contacts to make electrical contact with the interior regions of the semiconductor device, "windows" must be opened in the silicon nitride coating. These windows are usually opened by etching with boiling phosphoric acid. In an alternative method, the silicon nitride in the window areas is anodized, or converted electrolytically, into silicon oxide. The silicon oxide windows are then etched open with hydrofluoric acid.

To test the new structure, epitaxial silicon transistors with the new seal were deliberately contaminated with sodium ions. (Metallic ions in the atmosphere commonly contaminate semiconductor devices; because of their small size, sodium ions easily penetrate many protective materials.) The transistors were then subjected to accelerated power aging, that is, they were operated under normal voltage bias but at a power considerably above their rated level. The higher power accelerates failure by raising the temperature at the transistor junctions to about 300° centigrade. Although this and other tests are still continuing, the transistors with the new structure have already exhibited a longer median life than the median life (1,000 hours) of hermetically-sealed transistors power aged at 300° centigrade. The latter transistors had not been deliberately contaminated with sodium ions. END

Pulse Generator Offers Independent Amplitude And Baseline Controls

Pulse testing, particularly for logic systems designers, is said to be quite easy with a new pulse generator. It has a controllable pulse-repetition-rate of 1 KHz to 0.1 GHz, an independently-adjustable baseline, and a sync "countdown" feature for jitter-free display on oscilloscopes. In addition to ordinary lab usage, the Model 6901 is suitable for integrated-circuit testing of medium-speed RTL circuits to very high-speed ECL circuits. It is also said



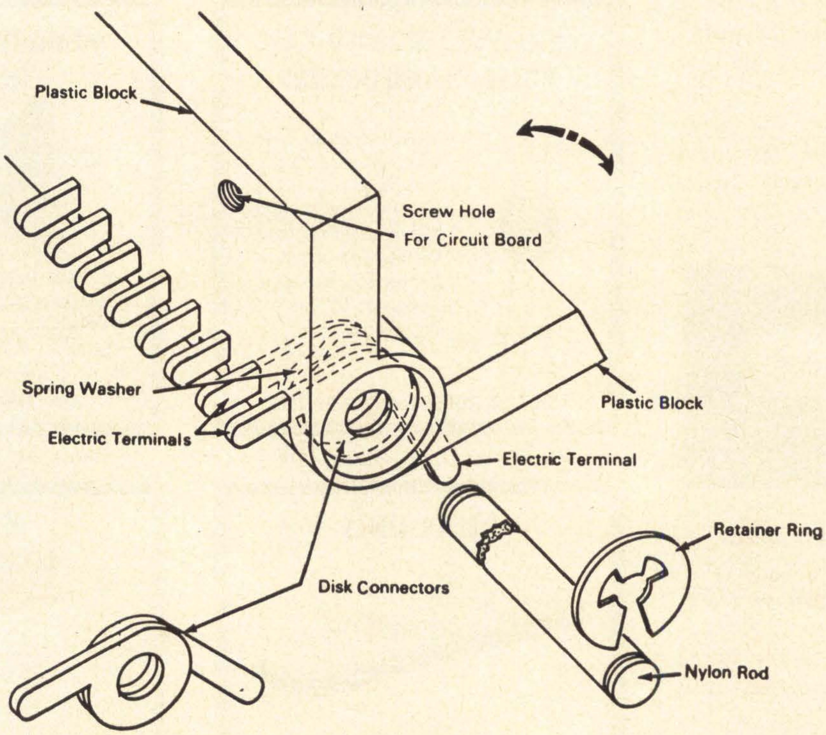
to be tailored to the test needs of fourth-generation computers. Major features include six ranges of pulse repetition rates (1 KHz to 0.1 GHz), with jitter less than 0.1 per cent of period +50 psec; variable-baseline control so that baseline may be adjusted to ±2 volts (with no attenuation) without affecting pulse amplitude or waveshape; variation in baseline (at full attenuation) is ±1 volt; normal sync output at clock repetition rates is a 1.5 square wave, suitable for driving networks, scopes, or other pulse generators. The pulse generator offers completely independent pulse amplitude and baseline controls. Variations in one parameter do not affect the other because the offset current source has been placed after, not before, the output attenuator, and the instrument uses a load-compensating resistor network to maintain a constant 50 ohm output impedance. Texas Instrument Inc., Houston, Texas.

Circle No. 265 on Inquiry Card

NASA TECH BRIEF

A SUMMARY OF A SPECIFIC TECHNICAL INNOVATION DERIVED FROM THE SPACE PROGRAM. ISSUED BY THE TECHNOLOGY UTILIZATION DIVISION OF NASA.

Device Serves as Hinge and Electrical Connector for Circuit Boards



THE PROBLEM:

To design a device that will make both sides of electrical circuit boards readily accessible for component checkout and servicing.

THE SOLUTION:

A hinge that provides for the mounting of two circuit boards and incorporates connectors which will maintain continuous electrical contact between the components on both boards.

HOW IT'S DONE:

The hinge consists of two plastic blocks with pairs of electrically conductive disks internally spaced along the hinge. Each disk has an arm that serves as an electric terminal, and the two disks in each pair are held in constant contact by spring washers and are arranged so that the arms extend in opposite directions. The hinge block assembly is held together by a single nylon rod with snap-on retainer rings at each end of the rod. The terminal arms on each hinge block are inserted into corresponding terminal slots on each circuit board. Plastic screws are used to secure the boards to the blocks.

NOTE:

Inquiries concerning this invention may be directed to: Technology Utilization Officer, Marshall Space Flight Center, Huntsville, Alabama 35812. Reference: B66-10359

PATENT STATUS:

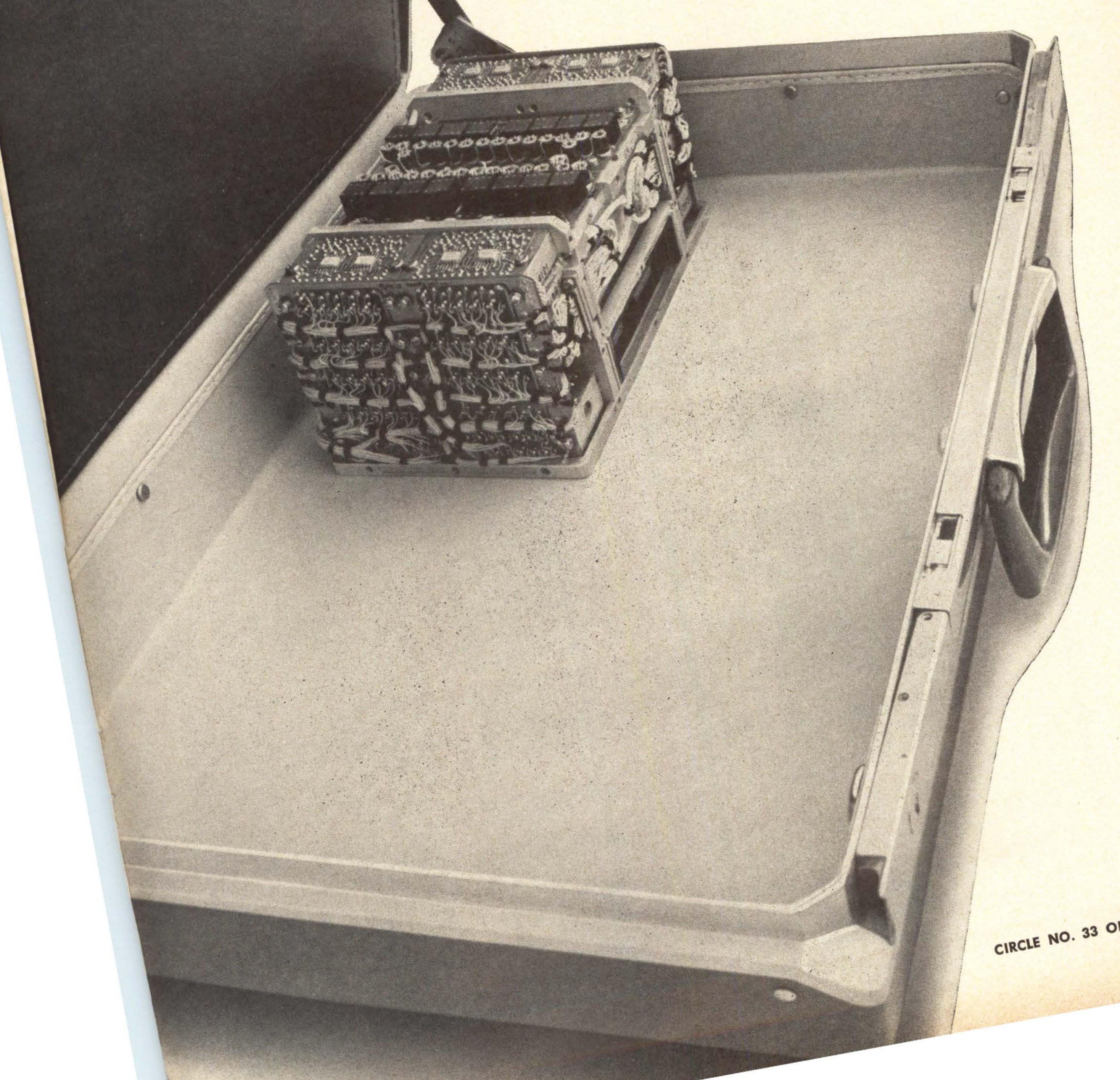
Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D. C. 20546. **END**

if you're ready to buy the smallest, fastest, military memory available, put on the coffee and call us. we'll be right over.

Our SEMS 5 weighs less than 7 pounds, operates on 60 watts maximum at a data transfer rate of 16,000,000 bits per second. It has a 2 μsec cycle time and stores 4096 words of 32 bits. And it meets applicable portions of MIL-E-5400, MIL-E-4158 and MIL-E-16,400.
Our number: (213) 772-5201. That's black, one sugar.

electronic memories

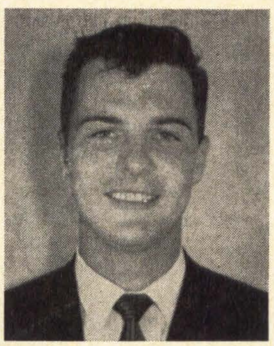
12621 Chadron Avenue, Dept. 3C,
Hawthorne, California 90250



CIRCLE NO. 33 ON INQUIRY CARD

USING DTL GATES AS DELAY LINE TAPS

One of the most common applications for tapped delay lines is in the generation of time-spaced pulses used to control digital systems, sequentially. In most cases, the circuits used to tap the delay line have a very high input impedance to prevent harmful reflection in the delay line. In the system described here, no such high-impedance circuits were available and it was necessary to use standard DTL gates as delay line taps.



Edmund B. Daly
Member of Technical Staff
Automatic Electric Co.
Northlake, Ill.

Edmund B. Daley holds M.S. and B.S. degrees in Electrical Engineering, University of Illinois, and is presently attending the University of Chicago for an M.B.A. in "Mathematical Models of Computers."

The following analysis was initiated because of the need for time-spaced pulses to control sequentially the operations of a high-speed ferrite core memory. The use of tapped delay lines as clocking devices in memory systems is not unusual but in this system no such high-input impedance circuits were available and it was necessary to use standard DTL gates as delay line taps. This article presents both a method of analyzing the problems which occur when DTL gates are used as delay line taps and the limitations which must be adhered to when such taps are used. Special attention should be focused on the section titled "Delay Line Attenuation", which contains a mathematical approximation which linearizes the exponential transmission line equations. It is by means of this derivation that a completely linear delay line analysis is obtainable.

Delay Line Analysis

In the analysis which follows, a delay line of characteristic impedance, R_o, is driven by a constant voltage source and tapped by DTL gates. The specific objective of this analysis is to calculate the maximum number of logic gates that may directly and safey tap the delay line. Consideration is given to both the quiescent and the pulsed state of the delay line and the associated tapping arrangement. **It is found that the maximum**

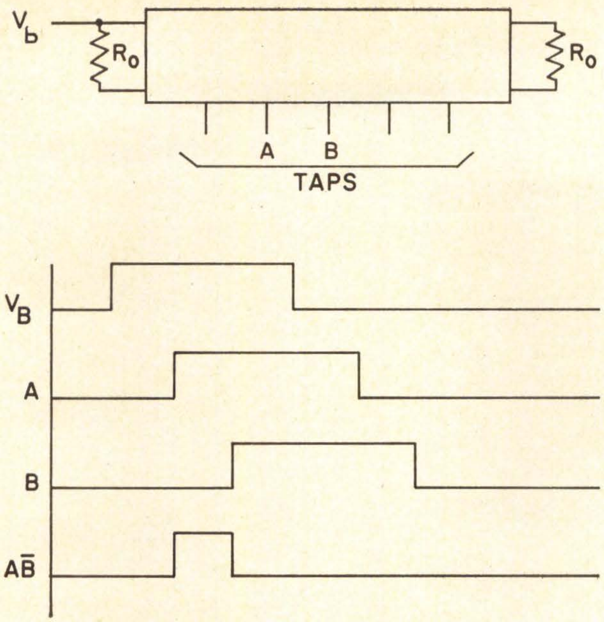


Fig. 1 Tapped delay line and output waveforms.

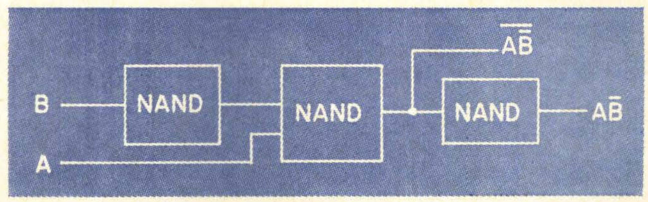


Fig. 2 NAND logic taps on delay line.

number of DTL taps is limited by two conditions. The first limitation occurs in the quiescent state when all tapping gates are assumed to be delivering current into the delay line. The second limitation occurs during the pulsed state when it is assumed that the pulse propagation down the delay line is of sufficient magnitude to cause the tapping DTL logic to change state. This upper limit on the number of taps is very important since it determines the number of control pulses that may be generated by the delay line arrangement.

Fig. 1 suggests a method that may be used to generate control pulses when using DTL NAND gate logic as delay line taps. The symbol V_b represents an input voltage pulse presented to the delay line by a constant voltage generator. The control pulse $A\bar{B}$ is formed from the delayed input voltage appearing at taps A and B. (All control functions should be generated using only the leading edge of the propagation pulse; for this reason the functional output $A\bar{B}$ is advised.) Fig. 2 shows a logical configuration that may be used to generate this control pulse. No buffering stages are used between the delay line taps and the pulse forming logic gate; any type of DTL gate may be used to generate the output function $A\bar{B}$, however, only NAND gate taps are considered, in this analysis.

To analyze a delay line which is tapped by NAND gates, the assumption is made that each NAND gate acts as an active current source during its quiescent state. As a positive edge propagates down the line it effectively shuts off each current source (NAND gate) upon time intersection. By assuming the existence of current sources, an analysis can be made to explain the characteristics of both the quiescent and pulsed line conditions.

Quiescent State Considerations

The delay line is in a quiescent state when transistor Q_2 in Fig. 3 is off. During this state all NAND gate taps should be delivering current to the delay line. A realistic approach to the tapping arrangement is to assume all NAND gate taps are equally distributed along the delay line. Fig. 4 represents a dc equivalent circuit of the delay line in the quiescent state, loaded by n equally-distributed NAND loads. The symmetrical distribution of NAND loads allows an equivalent lumped load midway between the input and output. Since each tap presents an apparent current source of I_L (current through D_1 in Fig. 3), n lumped taps present a current source of nI_L.

A necessary condition that must exist on the quiescent delay line is that the most positive line potential be less than, or equal to, zero volts. This condition insures that the n NAND gate taps are delivering current into the line and in their correct quiescent OFF state. Referring to Fig. 4, V_A is the most positive potential on the delay line. By setting this potential less than, or equal to, zero volts a limitation on the number of NAND gate taps can be established. Using superposition:

$$V_B = \frac{V_1\,(R_o + R_{dc})}{2R_o + R_{dc}} + \frac{n\,I_L\,R_o}{2} \tag{1}$$

$$V_A = \frac{V_1\,R_o}{2R_o + R_{dc}} + \frac{n\,I_L\,R_o}{2} \tag{2}$$

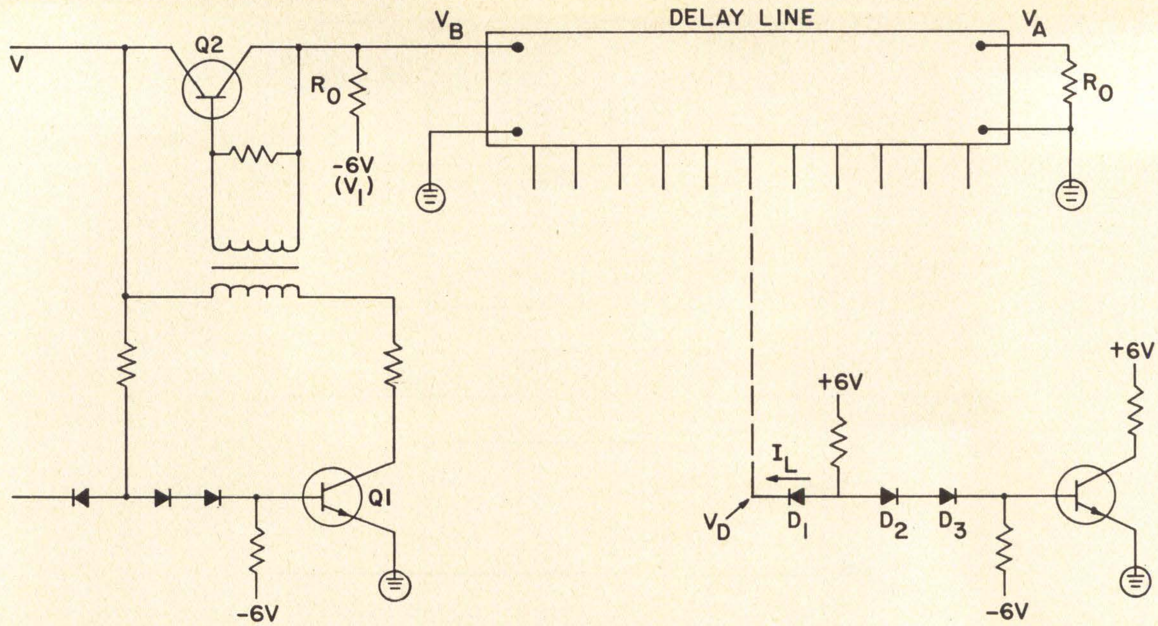


Fig. 3 Schematic of line driver and NAND tap.

where R_{dc} equals the dc resistance of the delay line, R_o equals the characteristic resistive line termination, and I_L equals the standard load current due to one NAND gate tap. Setting $V_A \leq 0$ volts, Equation (2) can be solved for n, where n represents the maximum number of equally-distributed NAND gates that can safely tap the delay line during its quiescent state:

$$n \leq \frac{-V_1}{I_L\,(R_o + \frac{R_{dc}}{2})} \tag{3}$$

The additional current delivered into the delay line by using more gates than that specified in Equation (3) would cause the dc line potential to rise above zero volts. Once this condition exists a marginal NAND gate tap could switch from its quiescent OFF state to its ON state, causing a system malfunction.

Pulsed State Considerations

Referring to Fig. 3, when Q_2 turns on, an ac voltage pulse appears at the input to the delay line. As this pulse propagates down the line, its magnitude is forced to diminish by two conditions:

1. Delay line attenuation — from transmission line theory, delay line attenuation can be represented by $e^{-\alpha t_d}$ where α is a positive real number with dimensions of neper/μsec. and t_d is the delay time in μsec.
2. Delay line reflections — reflections occurring at every loaded tap.

Since the initiating ac voltage pulse may rise from a negative reference (quiescent voltage at V_B), a distinction should be made between the magnitude and the positive amplitude of the pulses (e.g., a pulse rising from a negative potential of -2 volts to a positive potential of $+6$ volts has a magnitude of 8 volts and a positive amplitude of 6 volts). Even though attenuation is determined using the magnitude, it is the positive amplitude that causes a NAND gate tap to trigger. If this amplitude diminishes below a certain level, defined as V_T, the tapping gates may not change from their quiescent state when the propagating pulse reaches their input.

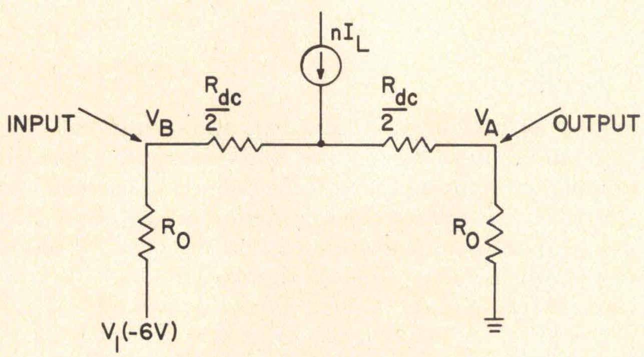


Fig. 4 DC equivalent of tapped delay line.

Delay Line Attenuation

The following analysis is used to find the amount of attenuation a pulse incurs as it propagates down a delay line. From transmission line theory, we find that the input and output voltages of any transmission line are related by the general equation:

$$\frac{E_o}{E_{in}} = e^{-(\alpha + j\beta)x} \tag{4}$$

where α is an attenuation constant with dimensions neper per unit of x, β is a phase shift constant, and x is the line variable. In the present analysis only pulse

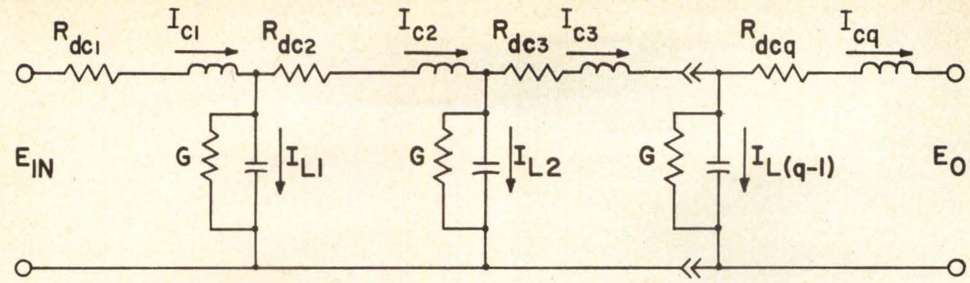


Fig. 5 Equivalent circuit for attenuation analysis.

attenuation is considered. The phase shift or delay can be easily calculated from the reactive components of the line, e.g., $t_d = k\ (LC)^{1/2}$. In order to simplify the analysis, an approximation is used which assumes a linear decay in both voltage and current. The results obtained are reasonably accurate for most practical delay lines where the voltage attenuation is less than 33%, and the dominant frequency of the input voltage pulse is less than f_c of the line (f_c is defined as the upper cutoff frequency of the delay line).

Moskowitz and Racker* point out that the constant α, in Equation (4), may be represented by:

$$\alpha = \frac{0.014}{8.686} \frac{R_{dc}'}{(N\, Z_o\, f_c^2)^{1/3}} \text{ neper/cell} \tag{5}$$

where R_{dc}' (artificial line) = dc resistance of 1,000 ft. of wire, N = constant (construction property), $Z_o = \left(\frac{L_o}{C_o}\right)^{1/2}$ (characteristic impedance), and $f_c = \frac{1}{\pi\ (L_o\, C_o)^{1/2}}$. For a given line N, Z_o and f_c are constant. Assuming we know the number of feet of wire per delay line cell (one lumped section of the delay line), Equation 5 may be rewritten:

$$\alpha = K\, R_{dc}/\text{cell} \tag{6}$$

where α is now expressed in neper/cell.

If q is the number of cells in the delay line, then the attenuation portion of Equation (4) may be rewritten as:

$$\frac{E_o}{E_{in}} = e^{-K(R_{dc}/\text{cell})\,(q)} \tag{7}$$

Expanding this exponential into its series form and using only the linear portion ($e^x = 1 - x$), a linear approximation is obtained:

$$\frac{E_o}{E_{in}} = 1 - K(R_{dc}/\text{cell})\ (q) \tag{8}$$

This equation may be rewritten as:

$$E_o = E_{in} - (E_{in}K)\ (R_{dc}/\text{cell})\ (q)$$

Dimensionally, $(E_{in}K)$ must equal current per cell, therefore:

$$E_o = E_{in} - \sum_{k=1}^{q} I_{c_k} R_{dc_k} \tag{9}$$

*Moskowitz and Racker, **Pulse Techniques**, Prentice-Hall, 1951, Page 115.

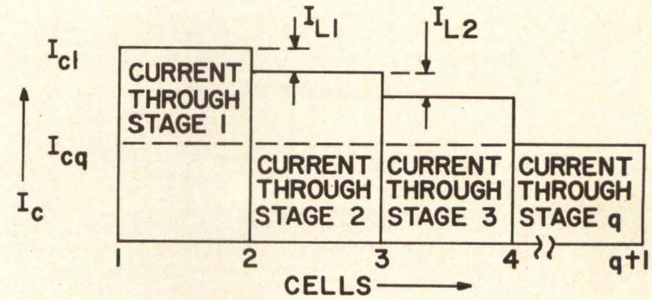


Fig. 6 Total current in the line.

Where I_{c_k} is the current flowing through the k cell, and R_{dc_k} is the dc resistance of the k cell. Referring to Fig. 5, which represents the delay line, it is noticed that the current in each cell (I_{c_k}) is less than the current in the preceding cell by the factor of $I_{L(k-1)}$. By assuming a linear decay in delay line current, we may set $I_{L_1} = I_{L_2} = I_{L(q-1)}$. Referring to Equation (9):

$$\sum_{k=1}^{q} I_{c_k} R_{dc_k} = I_{c_1} R_{dc_1} + I_{c_2} R_{dc_2} + \ldots\ I_{c_q} R_{dc_q} \tag{10}$$

Since every delay line section is identical:

$$R_{dc_1} = R_{dc_2} = R_{dc_q} \text{ therefore:}$$

$$\sum_{k=1}^{q} I_{c_k} R_{dc_k} = R_{dc_k} \left[I_{c_1} + I_{c_2} + \ldots I_{c_q}\right] \tag{11}$$

Regardless of the number of sections, the sum of $I_{c_1} + I_{c_2} + \ldots I_{c_q}$ can be calculated from the area under the curve in Fig. 6.

$$\text{Area} = \sum_{k=1}^{q} I_{c_k} = \left[\frac{I_{c_1} + I_{c_q}}{2}\right] (q) \tag{12}$$

Combining Equation (9) and Equation (12):

$$E_o = E_{in} - \left[\frac{I_{c_1} + I_{c_q}}{2}\right] q\, R_{dc_k} \tag{13}$$

where: $q\, R_{dc_k}$ = total dc resistance of the line = R_{dc}.

$I_{c_1} = I_{in}$ (input current to line)

$I_{c_q} = I_o$ (output current from line)

Equation 13 may be rewritten as:

$$E_o = E_{in} \left[\frac{I_{in} + I_o}{2}\right] R_{dc} \tag{14}$$

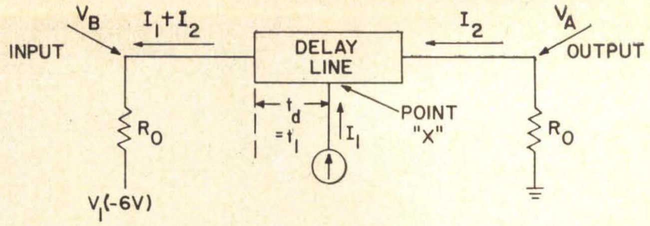


Fig. 7 Equivalent circuit for reflection analysis.

The next step is to find some relation between E_o and I_o, E_{in} and I_{in}. From transmission line theory, where Z_o is the characteristic impedance of the delay line:

$$E_{in} = I_{in} Z_o \tag{15}$$

$$E_o = I_o Z_o \tag{16}$$

Combining Equations (14), (15), and 16):

$$E_o = E_{in} - \left[\frac{E_{in}}{2Z_o} + \frac{E_o}{2Z_o}\right] R_{dc} \tag{17}$$

$$E_o\left[1 + \frac{R_{dc}}{2Z_o}\right] = E_{in}\left[1 - \frac{R_{dc}}{2Z_o}\right] \tag{18}$$

$$\frac{E_o}{E_{in}} = \frac{Z_o - R_{dc}/2}{Z_o + R_{dc}/2} \tag{19}$$

From Equation 19, the ratio E_o/E_{in} can be calculated by taking two simple delay line measurements: dc resistance and characteristic impedance. The simplified results obtained from the linear approximation can be observed by comparing Equation (19) to the attenuation term of Equation (4).

Delay Line Reflections

The magnitude of an ac pulse propagating down a delay line can be decreased by line reflections as well as line attenuation. When the delay line is tapped by NAND gates, each gate is considered a current source — the delay line is acting as the current sink. Referring to Fig. 3, in steady state (i.e., "Q_2" off) all NAND gate loads are considered to be active current sources. When Q_2 turns on, a positive voltage pulse travels down the delay line — turning off each NAND load upon time intersection. Somehow this information, a current source being deactivated, must get back to the line input, and thus a reflection occurs at the point of deactivation. This reflection informs the input that it need no longer act as a sink for the deactivated gate. Neglecting internal line attenuation, Fig. 7 illustrates a simple method of calculating the magnitude of a voltage reflection which has been initiated by a current discontinuity of magnitude I_1.

In steady state, both I_1 and I_2 are flowing in the directions indicated in Fig. 7. If I_1 turns off, a voltage wave front is developed at point x. This front propagates in two directions: toward the input V_B and toward the output V_A. When this front reaches the input or the output, it sees a characteristic termination R_o and no reflection occurs. A new steady-state voltage now exists at V_A and V_B. This change in steady-state voltage is caused by, and equal to, the wave-front developed at point x.

Since zero internal line attenuation is assumed, the dc resistance of the delay line is zero. Therefore, referring to Fig. 7, in steady state, we may set $V_A = V_B$. Steady state when I_1 is flowing:

$$V_B = V_1 + (I_1 + I_2)\, R_o \tag{20}$$

$$V_A = -I_2\, R_o \tag{21}$$

Setting $V_A = V_B$:

$$I_2 = \frac{-V_1}{2R_o} - \frac{I_1}{2} \tag{22}$$

Steady state when I_1 is not flowing:

$$V_B = V_1 + I_2'\, R_o \tag{23}$$

where I_2' is the value of current that flows when I_1 stops flowing.

$$V_A = -I_2'\, R_o \tag{24}$$

Setting $V_A = V_B$:

$$I_2' = \frac{-V_1}{2R_o} \tag{25}$$

The change in steady state voltage at V_B can be calculated by subtracting Equation (20) from Equation (23) and substituting values of I_2 and I_2' from Equations (22) and (25):

$$\Delta V_{B(dc)} = \frac{-\,I_1\, R_o}{2} \tag{26}$$

$\Delta V_{B(dc)}$ is equal in magnitude to the voltage wavefront developed at point x by a discontinuity in current equal to I_1.

A current discontinuity such as the one described above can occur if a positive pulse, traveling down a delay line, intersects a NAND gate tap connected as in Fig 3. Before the positive pulse appears at the NAND gate input, the current I_L flows into the delay line. After the appearance of the positive pulse at the NAND gate input, the current I_L stops flowing, causing the NAND gate to switch state (output transistor goes from the off state to the saturated state). This current discontinuity of I_L causes a negative voltage level of magnitude $I_L R_o/2$ to be initiated at the tapping point.

The reflection, as well as traveling back toward the input, detracts from the positive amplitude of the initiating pulse. Referring to Fig. 7, if the positive amplitude of the initiating pulse at $t_d = t_1^-$ is V_p, then the positive amplitude at $t_d = t_1^+$ is $V_p - I_L\ (R_o/2)$. If a line is tapped by n loads, a total attenuation of $nI_L R_o/2$ will result if all n NAND gate loads switch as the positive pulse propagates down the line.

Second Reflections

If a reflected negative voltage reaches the input V_B while Q_2 is still conducting, it will see an ac short circuit. The shorted termination causes the reflection to reverse in polarity and travel back down the delay line in a positive sense. This effect is not detrimental to circuit operation since the second reflection algebraically adds to the positive driving voltage (V_2 − V_{CESQ_2}). If a reflected voltage reaches the input V_B after Q_2 has ceased conducting, the ac input termination presents R_o to the reflected voltage and a second reflection does not occur. Second reflections at the delay line input are, therefore, not considered germane to the following arguments.

AC Pulse Amplitude

When Q_2 in Fig. 3 saturates, the voltage at V_B changes from its quiescent value given by Equation (1) to a positive value equal to $(V_2 - V_{CESQ_2})$. The change in voltage at V_B generates an ac level which starts to propagate down the delay line. As this level propagates down the line its positive amplitude is affected by three line conditions. The first is the dc potential existing on the line during its quiescent state, the second is attenuation due to the dc line resistance, and the third is attenuation due to discontinuities on the line (NAND gate taps).

It has already been established that the minimum positive amplitude of this ac level must be greater than V_T volts to insure proper switching of all NAND gate taps. **Therefore, by applying the three line conditions mentioned above and insuring that the positive amplitude of the ac level is always greater than V_T volts, a second limiting value on n (number of equally distributed NAND gate taps) can be established.** The first limiting value on n occurred during the quiescent state of the delay line. During this period, the maximum dc voltage of the line must not have exceeded zero volts).

Delay Line Input Voltage

The ac input voltage that propagates down the delay line is equal in magnitude to the change in V_B. When the delay line is in its quiescent state V_B is given by Equation (1). After Q_2 saturates, V_B takes on the potential:

$$V_B' = V_2 - V_{CESQ_2} \tag{27}$$

The change in potential at V_B is positive since V_B' is more positive than V_B. This potential change $(\Delta V_{B(ac)})$ equals:

$$\Delta V_{B(ac)} = V_B' - V_B = V_2 - V_{CESQ_2} - \frac{V_1 (R_o + R_{dc})}{2R_o + R_{dc}} - \frac{n\, I_L\, R_o}{2} \tag{28}$$

Pulse Propagation

For simplicity of analysis, the equally distributed NAND gate taps are again grouped together as one lumped load at the center of the line (see Fig. 4). The positive pulse $\Delta V_{B(ac)}$, can then be assumed to propagate half way down the delay line unattenuated by delay line taps. At the half-way point, the pulse encounters a lumped tap of nI_L. This lumped tap causes the propagating pulse to attenuate by $nI_LR_o/2$ — see Equation (26). After this lumped attenuation occurs, the pulse continues down the delay line, again unhampered by taps until it reaches the R_o termination of the line where it is completely absorbed.

The magnitude of a pulse traveling down a lossy delay line is also attenuated due to the dc resistance in the line itself. This attenuation is represented by Equation (19). Applying both modes of attenuation to the propagating pulse, the following situation occurs: at the input to the delay line, the magnitude of the ac pulse is equal to $\Delta V_{B(ac)}$; half way down the delay line this pulse has attenuated to:

$$\Delta V_{B(ac)} \left[\frac{Z_o - \frac{R_{dc}}{4}}{Z_o + \frac{R_{dc}}{4}}\right] \qquad (29)$$

Since only half of the total line is considered, $R_{dc}/4$ is used in place of $R_{dc}/2$. After the pulse intersects the lumped load, its magnitude diminishes to:

$$\Delta V_{B(ac)} \left[\frac{Z_o - \frac{R_{dc}}{4}}{Z_o + \frac{R_{dc}}{4}}\right] - \frac{n\, I_L\, R_o}{2} \qquad (30)$$

The pulse now continues down the line where at the R_o termination its magnitude has attenuated to:

$$\Delta V_{B(ac)} \left[\frac{Z_o - \frac{R_{dc}}{4}}{Z_o + \frac{R_{dc}}{4}} - \frac{n\, I_L\, R_o}{2}\right] \left[\frac{Z_o - \frac{R_{dc}}{4}}{Z_o + \frac{R_{dc}}{4}}\right] \qquad (31)$$

Adding this ac magnitude to the dc reference existing at the R_o termination, Equation (2), the *positive* amplitude of the pulse can be established. Since the positive amplitude of the pulse will be at its minimum value when it reaches the R_o termination, proper switching of all tapping NAND gates can be assumed if this level is more positive than V_T. After substituting Equation (28) for $\Delta V_{B(ac)}$ we can set the sum of Equation (31) and Equation (2) less than V_T, and solve for n:

$$n \leq \frac{V_T - \left[\left[V_2 - V_{CESQ_2} - \frac{V_1(R_o + R_{dc})}{2R_o + R_{dc}}\right] x^2 + \frac{V_1 R_o}{2R_o + R_{dc}}\right]}{\frac{R_o I_L}{2}(1 - x^2 - x)} \qquad (32)$$

where:

$$x = \frac{Z_o - \frac{R_{dc}}{4}}{Z_o + \frac{R_{dc}}{4}}$$

The denominator of Equation (32) is very interesting: if $x^2 + x = 1$, then n goes to infinity. This occurs when the dc resistance of the delay line is such that an increase in n shifts V_A in a positive direction at a faster rate than it decreases the pulse magnitude reaching V_A. Such an equality, however, is not a panacea, for the second limitation on n, given by Equation (3), must also be satisfied.

Numerical Example

In the following example a lumped constant, 5.0 μsec. delay line, is used. This line has a characteristic impedance (Z_o) of 50 ohms and a series dc resistance (R_{dc}) of 16.2 ohms. Power supplies used for V_1 and V_2 are -6 volts $\pm 5\%$ and $+6$ volts $\pm 5\%$, respectively. The maximum collector-emitter saturation voltage of Q_2 (V_{CESQ_2}) is 0.5 volt. The minimum positive input voltage needed to trigger a NAND gate (V_T) is 2.0 volts. In the quiescent state each NAND gate tap acts as a current source

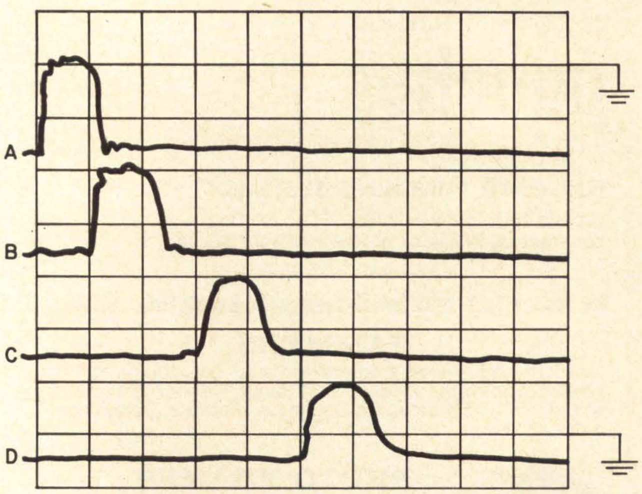


Fig. 8 Pulse propagation down an unloaded line. Waveform A is input voltage; waveform B is input voltage delayed 1.0 usec; C is input voltage delayed 3.0 usec; and D is input voltage delayed 5.0 usec. Scale is 5 volts/cm and 1 usec/cm.

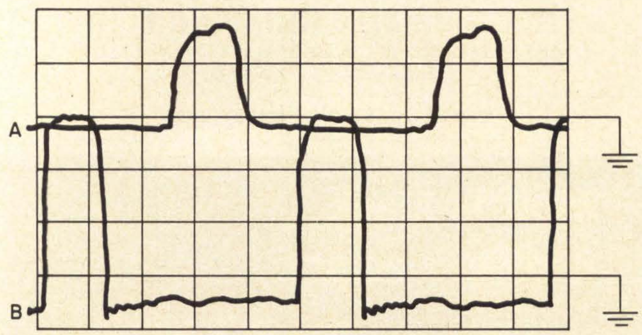


Fig. 9 Propagation on line with 30 distributed taps. Waveform A is the delay line voltage at $t_d = 5.0$ usec. B is delay line voltage at $t_d = 0$ usec. Scale is 2 volts/cm and 2 usec/cm.

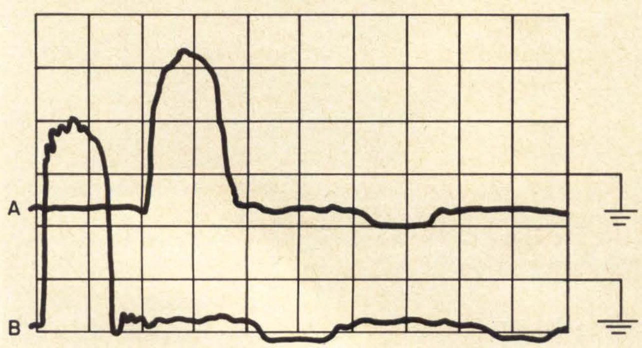


Fig. 10 Line with parallel loads. A is voltage waveform at $t_d = 2.0$ usec and B is voltage waveform at $t_d = 0$ usec.

of 3.0 ma. This value is arrived at by assuming the average dc quiescent voltage of the line rides at -0.5 volt. After the analysis is complete, this assumed value of I_L should be checked and re-evaluated, if necessary. It has already been established that there are only two line conditions limiting the number of equally-distributed NAND gates that may safely tap the delay line.

• **Quiescent State:** n is limited in the quiescent state by setting the most positive line potential less than, or equal to, zero volts. Using Equation (3), this limiting value can be found:

$$n \le \frac{5.7}{3.0 \times 10^{-3}\left(\frac{16.2}{2} + 50\right)}$$

$$n \le 32 \text{ gates.}$$

• **Pulsed State:** n is limited by setting the minimum positive amplitude of the pulse less than, or equal to, V_T. Using Equation (32), this limiting value can be found:

$$x = \frac{E_o}{E_{in}}\Bigg|\, 2.5\ \mu\text{sec.} = \frac{50 - \frac{16.2}{4}}{50 + \frac{16.2}{4}}$$

$$x = 0.85$$

$$n \le \frac{1.5 - \left[\left[5.7 - 0.5 + \frac{6.3\ (66.2)}{116.2}\right] 0.72 - \frac{6.3\ (50)}{116.2}\right]}{\frac{50\ (3 \times 10^{-3})}{2}\ (1 - 0.72 - 0.85)}$$

$$n \le 37 \text{ gates.}$$

The above results show that the number of tapping gates is limited by the quiescent state of the delay line where n is smaller than or equal to 32. Note that the power supply tolerances are included in all calculations so as to give the least value of n.

• **Checking:** before the analysis is complete, the original assumption of the magnitude of I_L must be checked. The value of I_L (3.0 ma) was established by considering the average dc line potential in quiescent state to be at -0.5 volt. If the actual average potential is less negative than this value, I_L will be less than 3.0 ma and the above results will be slightly pessimistic but still valid. The average line potential equals:

$$\frac{V_B + V_A}{2}$$

Using Equations (1) and (2):

$$\frac{V_B + V_A}{2} = \frac{V_1}{2} + \frac{n\, I_L\, R_o}{2} \qquad (33)$$

Since the limitation on n (32 gates) was arrived at using $V_1 = -5.7$ volts, this same value must be used in Equation (33):

$$\frac{V_B + V_A}{2} = \frac{-5.7}{2} + \frac{32\ (3.0 \times 10^{-3})\ (50)}{2}$$

$$\frac{V_B + V_A}{2} = -0.415 \text{ volt}$$

When the delay line is fully loaded with 32 NAND gate taps, I_L will, therefore, be slightly less than 3.0 ma.

Conclusion

Oscillograms illustrating delay line operation are shown in Figs. 8, 9, and 10. Fig. 8 shows a pulse propagating down an unloaded delay line with the driving arrangement as was shown in Fig. 3. These oscillograms illustrate both pulse attenuation and dc level shift. In Fig. 9, the delay line is tapped by 30 distributed NAND gate taps. The first two wave shapes show the NAND gate input voltages at $t_d = 0$ μsec and at $t_d = 5.0$ μsec. In Fig. 10, the delay line is tapped by ten parallel loads at $t_d = 2.0$ μsec and ten parallel loads at $t_d = 4.0$ μsec. These oscillograms clearly illustrate the negative reflections which occur when a NAND gate changes state, causing a current discontinuity in the delay line.

The purpose of this article has been to present a method to analyze a delay line which is directly driving DTL logic gates. This discussion has considered only equally-distributed loads; however, the analysis can be applied to lumped or asymmetrical loading. The results obtained in this article have been experimentally justified using low impedance artificial lines. END

DC OUTPUT

continued from page 30

sources are shared among agencies for work that otherwise would have been accomplished through contracts with non-governmental facilities. The Administrator of the General Services Administration, Lawson B. Knott, Jr., expects savings to rise significantly in this fiscal year. Excess EDP equipment valued at $29 million was reported to GSA during the last fiscal year for re-utilization by other Federal agencies.

Recent Government Contracts

LEAR SIEGLER, INC., Grand Rapids, Mich., has been issued a $1,133,139 increment to a previously-awarded contract for production of aircraft bombing computers. The Aeronautical Systems Division is the issuing agency.

SYSTEM DEVELOPMENT CORP., Santa Monica, Calif., has been awarded a $12,570,000 cost-plus-incentive-fee contract for updating computers and preparation of system training programs. The Sacramento Air Materiel Area (AFLC), McClellan AFB, California, is the contracting agency.

IBM CORP., Owego, N. Y., has received a $1,500,000 initial increment to a $3,000,000 cost-plus-incentive-fee contract for production of data processing equipment. The Aeronautical Systems Division (AFSC), Wright-Patterson AFB, Ohio, is the issuing agency.

NEW PRODUCTS

HIGH DENSITY PATCH PANEL

A patch panel accommodates 800 pin and socket contacts in a space approximately 12 x 8 x 5 in. The same design principle can also be used to provide 1200 circuits in a single unit. According to the company, contact densities of this magnitude have previously presented problems due to the excessive mating forces required, contact bending, misalignment, molding, and manufacturing tolerances. In the new patch panels, these excessive mating and unmating forces are said to be overcome by utilizing a cam-type engaging device which converts rotary motion into an axial motion and provides a mechanical advantage to allow easy manual mating and unmating. Misalignment, contact bending, molding, tolerance problems were solved by dividing the contacts into smaller groups. Multiple insulation blocks contain independent guide-pin systems which automatically align the individual groups of contacts. Socket inserts are held firm while pin inserts float for proper contact alignment. Inserts have closed entry to prevent marginal continuity problems. The patch panel is said to be the first of its size to use pin and socket contacts with their inherent reliability and low millivolt drop (one mv max at one amp dc). Versatility in design allows many combinations of circuitry to be pre-programmed and sealed, permitting permanent, removable programming to coincide with data processing tapes. The unit can also be utilized as an in-work patch panel since the inserts can be reprogrammed while mated or unmated. Inserts can be mounted individually with a single engaging mechanism utilized for stationary data processing applications where substantial quantities of inserts would be required. Amphenol Space & Missile Systems, Chatsworth, Cal.

Circle No. 255 on Inquiry Card

FIBER OPTIC FACEPLATES

The transmission characteristics of new fiber optic faceplates are said to permit efficient optical coupling in image conversion and intensification systems. Electronic applications include their use as faceplates in image converters, vidicons, image orthicons, and other special electron tubes, and in high ambient light-viewing systems and display panels. Absorbing glass, generally used in the faceplates, enhances contrast by reducing "cross-talk", or light leakage between fibers. Fiber diameter and the use of absorbing glass may be controlled to produce an optimum balance of transmission, resolution, and contrast in a faceplate suitable for any application. Corning Glass Co., Corning, N. Y.

Circle No. 208 on Inquiry Card

SWITCHING SYSTEM

A Teletypewriter switching system uses a stored-program time-division multiplex technique. All critical paths and functions are either double or triple redundant with majority vote takers, error detectors, and status indicators. The system package consists of a three bay electronics rack and an operator's console. The electronics racks contain input and output isolator units, circuit monitoring and analyzing equipment, control and interface logic, memories, and power supplies. The console contains a 200 card-per-minute card reader, a dual keyboard, a printer, a voice communications set, and operator's control and status indicators. Operators may query status of any line or manually change switch status with the console keyboard. The system will accept data rates to 4800 bits per second. A store and forward operation mode is available with expansion of the dual memory within the switch system. Other input, line monitoring, and output peripherals are available. D. Brown Assoc., Incorporated, Eau Gallie, Fla.

Circle No. 207 on Inquiry Card

MULTIPLE PULSE GENERATOR

Multiple pulse generator operates at stepping rates from 10 mc to 1 kc and has twelve parallel output channels. Programming is accomplished by inserting diode pins into an eight by twelve program matrix board. The eight time steps constitute a single pass through the program and the program may be repeated a given number of times under the control of a variable delay prior to being initiated again. The number of program repeats depends on the program, the stepping rate, and the duration of the variable delay. The cycle may be started again either by an external control pulse or by a built-in slow (1 mc to 10 cps) cycle initiate clock. Step and pair repeats are controlled by toggle switches associated with time step and two variable analog delays with a range from one microsecond to 100 milliseconds. An "endless" position on the step repeat switch allows for a very long step or pair repeat period under control of the operator. When the switch is manually moved, the next time step is generated. Each channel output will contain a variable delay in step starting time and a variable duration of the pulse level output. The output amplitude may be varied from 0 to +7 volts under open conditions. The output stages may be run at very high duty cycles (100%) and perfectly match a 51 ohm line in both the "on" and "off" condition. The Model SQ-150 is well suited to act as the clock and controller for any system which requires sequencing such as memory testers. It is also ideal for testing for hazards in logic networks and effect of irregular duty cycles. Adar Assoc., Inc., Lincoln, Mass.

Circle No. 205 on Inquiry Card

DIGITAL DISPLAYS

A new time-saving system of digital displays is for use with laboratory spectrophotometers and related instruments. Modules include linear or linear-log readouts, a sample identification sequencer, concentration display, and data printer. System capabilities include automatic readout or printout of absorbance, transmittance, concentration, and sample sequence. Linear-log models are available with BCD output to allow use with a printer, remote indicators, or other data handling equipment. A solid-state amplifier and absence of stepping switches and relays are said to assure dependable accuracy over a wide range of operating conditions. The systems have an electrical span of 0-100 millivolts. Beckman Instruments, Inc., Fullerton, Cal.

Circle No. 211 on Inquiry Card

DESKTOP COMPUTER

The latest advances in desktop computer technology and design are said to be incorporated in a new model. New ½ power (square root) function mathematically closes parentheses and computes power to the ½ of either a single quantity or the computation enclosed. This function may be entered at any point or points in a computation at the touch of a single key. A significant digit retention feature allows the operator to enter numbers of unlimited length. The unit automatically preserves the nine most significant digits and adds all additional entries to the exponent. An electronic memory lock device protects the data in the storage registers and the memory bank while the instrument is turned off. Mathatronics, Waltham, Mass.

Circle No. 232 on Inquiry Card

IC LOGIC CARDS

Two new integrated circuit cards are dual in-line DTL and TTL circuit cards. Logic levels are consistent with flat-pack cards in entire product line. The cards are designed to fit into files which hold 16 to 32 cards each. Monitor Systems Inc., Fort Washington, Pa.

Circle No. 244 on Inquiry Card

VOLTAGE MEMORY CARD

A voltage memory card is said to provide an economical approach to the monitoring of single or repetitive transients in pulse widths from dc to 100 microseconds. Designated the Model 5221, the card is used with an external meter and power supplies, and mounts in the user's equipment. The card converts the peak amplitude of any input signal of 100 microseconds or longer duration into a dc output and holds it indefinitely in an electronic memory until reset or until a higher amplitude input pulse is received. Input impedance is 10K ohms minimum, and the input circuit has a 20% over-range capability. Output of the memory card is 0 to 100 microamps dc, full scale, and is internally adjustable to full scale for meters of 500 to 1000 ohms internal resistance. Accuracy is $\pm 2\%$ of full scale. Micro Instrument Co., Hawthorne, Cal.

Circle No. 237 on Inquiry Card

FLIP-FLOP CARD

As many as 16 reset-set flip-flops can be placed on a new single card assembly. These cards are priced at less than $3 per gate. Eight quadruple 2-input DTL integrated circuits are used to achieve speed and noise immunity by cross-coupling gate pairs. The set and reset inputs and outputs of all flip-flops are accessible through a 70-pin connector. Logic levels are compatible with TTL circuits. In-line circuit packages mounted on circuit cards are printed on both sides to form a compact and highly economical unit. Glass epoxy boards are spray etched and wave soldered. Eyelets are used to connect etch patterns on each side of the board. All copper circuit conductors are 0.020" wide with 0.020" minimum spacing. Power conductors are 0.1" wide with 0.025" minimum spacing. Cambridge Thermionic Corp., Cambridge, Mass.

Circle No. 242 on Inquiry Card

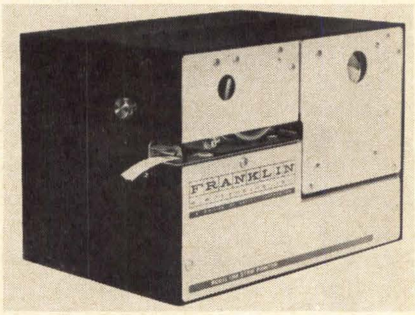
REED SWITCH MODULE

New reed switch module for pushbutton switches is described as ideal for handling low-energy circuits in data-processing systems, programmers, logic circuits, intercoms, sensitive audio and visual circuitry, as well as more prosaic applications such as vending machines and antenna switchgear. The modules are available in two momentary versions, each having two single-pole normally open contacts: One (2D802) has an actuating detent that gives a tactile feedback when the pushbutton has been depressed; the other (2D842) has no detent, meaning a lower operating force. Both designs can operate up to 12 reed switches with any combination or normally open (form A) or normally closed (form B) reeds. Heart of the module is a fiber-reinforced thermoplastic case holding two normally open dry-type reed switches, plus a single-loaded plunger that moves a cylindrical magnet. Pushing the plunger moves the magnet down near the reed contacts, pulling them together. Hook-shaped color-coded terminals all come out of the same end of the case for easy wiring. To prevent stray electro-magnetic fields from accidentally closing the contacts or influencing operating characteristics, a ferromagnetic shield encloses the plastic case. Besides giving magnetic protection the shields also furnish physical protection for the case. Because they are hermetically sealed inside individual glass envelopes, the gold-plated reed contacts are impervious to damaging atmospheres and contaminants. Moreover, the envelopes are filled with an inert gas having a high dielectric strength to reduce arcing and thus extend contact life. Micro Switch Div. of Honeywell, Inc., Freeport, Ill.

Circle No. 238 on Inquiry Card

BUFFERED STRIP PRINTER

The Model 120AX strip printer has a full 64 character font and provides continuous printout along a ½" wide paper tape at a rate of 1200 characters per minute. It includes the electronics for operating and controlling the printer. The printer was designed for systems manufacturers who prefer a complete operating printer. However, manufacturing details are freely given to other manufacturers who customarily provide their own electronics. Franklin Electronics, Inc., Bridgeport, Pa.



Circle No. 248 on Inquiry Card

COMPLEX HYBRID ARRAYS

Complex arithmetic units for use in central processors and interface applications utilize diode-transistor logic in a 32-lead flatpack (1 by 8/10 inches) to achieve high levels of speed and reliability. The new design program seeks to provide complex hybrid arrays which are easily adaptable to systems now being designed using integrated circuits. This approach is said to allow for maximum flexibility at minimum cost to the system manufacturer. Fairchild Semiconductor, Mountain View, Cal.

Circle No. 269 on Inquiry Card

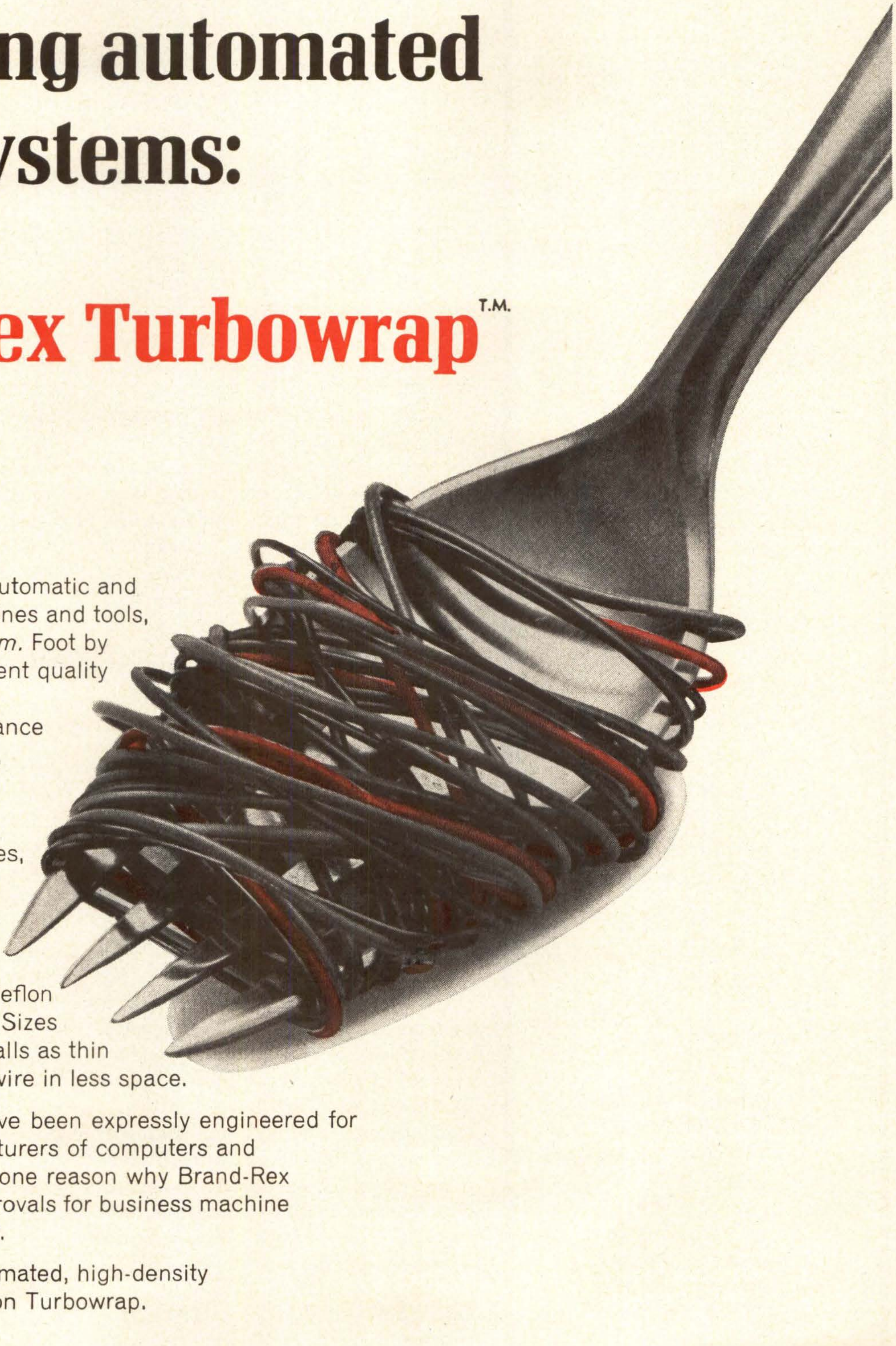
HIGH-SPEED DIODES

Small size and outstanding electrical and mechanical features are said to make a new diode suited for applications such as a core driver in avalanche circuitry or any high-speed, high-conductance application. Designated the Mono-diode, the silicon planar epitaxial device is hermetically sealed in a glass package. A series of surface stabilization and protection steps have made this device immune to reverse parameter degradation, according to the manufacturer. Continental Device Corp., Hawthorne, Cal.

Circle No. 201 on Inquiry Card

The wire that's specially-made for feeding automated wiring systems:

Brand-Rex Turbowrap[T.M.]



Turbowrap runs like silk in automatic and semi-automatic wiring machines and tools, because it's *unusually uniform.* Foot by foot, and lot by lot — consistent quality in electricals, physicals and mechanicals reduces the chance of jammed or erratic feeding, nicks, strains, cuts or shorts.

And Turbowrap, in a broad choice of insulations and sizes, gives you almost unlimited design freedom. Standard insulations include semi-rigid PVC and PVC/nylon, Teflon FEP and FEP/nylon, Teflon TFE, Kynar and Polysulfone. Sizes as small as #30 AWG, and walls as thin as .004", help you put more wire in less space.

Various Turbowrap types have been expressly engineered for the world's leading manufacturers of computers and business machines. They're one reason why Brand-Rex has chalked up more UL approvals for business machine wire than any other company.

Want to get more out of automated, high-density wiring? Write us for details on Turbowrap.

AMERICAN ENKA CORPORATION
BRAND-REX DIVISION
WILLIMANTIC, CONNECTICUT 06226
PHONE 203 423-7771

CIRCLE NO. 55 ON INQUIRY CARD

NEW PRODUCTS

PULSE COUNTER

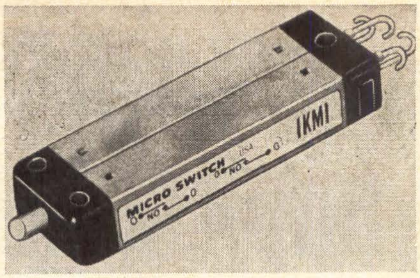
High-speed pulse counter has recently undergone life tests at 40 pulses per second which resulted in more than 500,000,000 counts without malfunction. The new pulse counters are seen as filling a void between low-cost, low-speed electromechanical counters and the large, sophisticated, and expensive electronic counters. Major advantages of the new counters are said to be extremely long life; high reliability and high response rate; large digits of 5/16" high; low power consumption, 3 watts average (ac or dc); reading retained during power interruption or transients; and no power consumed between pulses. Units are available in non-resettable versions and with manual or electrical reset to zero. Design features include a unique 2-wire stepper motor that does not require logic circuitry. Pulse signals are transmitted through a SPST switch or equivalent solid-state switching device. Haydon Switch & Instrument, Inc., Waterbury, Conn.

Circle No. 231 on Inquiry Card

PULSE STANDARDIZER

A pulse standardizer for computer-controlled systems is said to provide a reliable, trouble-free data link between any process system or automatic machine and a computer. The pulse standardizer, designated Model S-100, is used as an interface between system contact closures and the controlling computer. The S-100 delivers a uniform 20 milliseconds contact closure as an output whenever an input contact closure or voltage level is applied that has a duration greater than 15 milliseconds. The output closure duration is then independent of the input duration. Input pulses having a duration less than 10 milliseconds will not cause any output whatsoever. The S-100 design uses silicon, solid-state circuitry for stable temperature characteristics and is housed in a rugged case with gasketed cover. Optimized Devices, Inc., Pleasantville, N. Y.

Circle No. 213 on Inquiry Card



TWO-REED SWITCH

Features of a 2-reed basic switch include hermetically-sealed reed contacts, 10 million operations at rated load, extremely short contact bounce time, small size, and color-coded terminals. The switch units contain two nickel-iron alloy reeds with diffused gold contacts that are hermetically sealed in inert gas at approximately 1 atmosphere. Resistive rating is 100 milliamperes at 120 volts ac (12 volt-amperes maximum) and 250 milliamperes at 32 volts dc (8 watts maximum). Maximum applied voltage not to exceed 250 volts ac or dc. Maximum current not to exceed 250 milliamperes. Micro Switch, a Div. of Honeywell, Freeport, Ill.

Circle No. 254 on Inquiry Card

MODULAR POWER SUPPLIES

Two new 0-120 vdc all-silicon, fixed-voltage power supplies have multiple current ratings based on ambient temperatures of up to 71C. Model LM 267 has a current rating of 0.10 amps at 40C, 0.09 at 50C, 0.08 at 60C, and 0.07 at 71C. Because the power supplies can be mounted on any of three vertical surfaces, dimensions can not be given in conventional height, width, and depth. Package A is 3⅛" x 3-11/16" x 6½". All current ratings for these convection-cooled power supplies are based on operation without forced air cooling. The ventilated construction of these units is said to afford substantial increases in ratings with small amounts of air flowing over surfaces of the power supply. All models are remotely programmable — 200 ohms/volt over voltage range. Line regulation is 0.05% +4mv; load regulation is 0.03% +3mv; ripple is 1mv rms, 3 mv peak-to-peak. Lambda Electronics Corp., Melville, L. I., N. Y.

Circle No. 204 on Inquiry Card

PUSHBUTTON SWITCHES

Highly-versatile series of pushbuttons is said to magnify substantially the flexibility and adaptability of illuminated and non-illuminated versions of the company's pushbutton line. By coupling two stations, the new buttons increase multiple switching capabilities without adding to the overall height of a switch stack. A single pushbutton will actuate up to 12 PDT circuitry on a standard switch frame. Through the use of a wide variety of available display screen styles, color filters, split face inserts, and light dividers, the Series 409 pushbuttons can be adapted to produce any of the following displays: (1) solid color bar, illuminated or non-illuminated; (2) two section split-screen with two-lamp illumination, utilizing one lamp in each section; (3) three section split-screen, using one lamp in each section with various color filters. The buttons are designed for either horizontal or vertical switch frame mounting. Switchcraft, Inc., Chicago, Ill.

Circle No. 217 on Inquiry Card

LOW-THERMAL SWITCHES

New switching systems are for use with thermocouples or for similar applications requiring minimum switching thermals. Standard units are panel mounted, 19″ wide x 7″ high, and include features such as a rotary instrument switch for 12 or more inputs plus solid silver contacts, fully enclosed wipers, and an indexed knob providing for manual switching and position indication. Automatic and manual operations are selectable by a front panel-mounted selector switch. They are designed for precision switching of thermocouple inputs into a single channel reference junction and readout instrumentation with minimum introduction of errors due to generation of emf's in the switch. They can also be used with any low level sensing elements, such as thermistors, which require a minimum of thermals in the circuit. Joseph Kaye & Co., Inc., Cambridge, Mass.

Circle No. 266 on Inquiry Card

NEW PRODUCTS

BIT ERROR RATE DETECTOR

A bit error rate detector is a precision instrument designed to analyze the fidelity of the record/playback cycle of digital magnetic tape recorders. Analysis of bit error rate due to packing density, data pattern, adjacent channel cross talk, wow, and flutter is possible with this test set. The detector operates in two modes. The record mode provides a PCM output for a magnetic tape recorder consisting of a selectable number of repetitive frames. The frame consists of sixteen independent words, the first two of which are utilized for the frame sync I.D. word. In the playback mode, the detector accepts the PCM data from the tape recorder and compares it with the actual data generated. The detector compares each incoming data bit for each data word. If an error occurs, the bit error counter for that word is incremented. Each error counter accumulates the total number of errors for its corresponding word over the tape run up to a maximum of 1000. The number of errors accumulated for each word may be displayed on the front panel by selecting that word with the word select switch. Another error counter that accumulates the total number of errors, up to 9,999, is also provided. Space Craft, Incorporated, Houston, Texas.

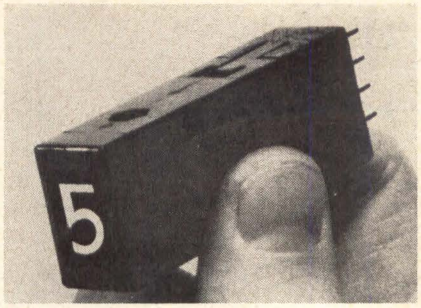
Circle No. 234 on Inquiry Card

D/A CONVERTER

Solid-state, 14-bit, digital-to-analog converter features digital and analog signal isolation and full output for over-range input. The unit accepts 19 bits of binary input, from which the appropriate 14 bits are selected. This is accomplished from either the front panel, or remotely, for one of four ranges. An external reference voltage between +90 and 140 volts is used to generate the dc output which varies between zero and the reference voltage. The only power required for operation is nominal 120 vac at 50 to 400 cps. Gap Instrument Corp., Westbury, N. Y.

Circle No. 200 on Inquiry Card

FRONT PLANE READOUT



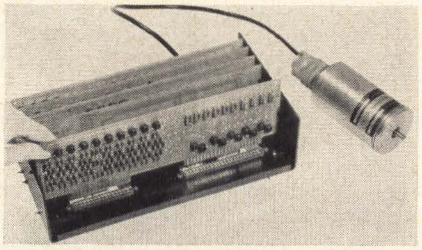
Miniaturized front plane readout has a viewing area of 3/8" H x 11/32" W. Exterior dimensions of the readout units are 0.83" H x 0.505" W x 2.50" L (not including 0.28" connector pins). Individual readout units may be ganged in any number. The lamps are standard for 5V or 6V operation, with 12 to 14 volts available on special order. Since each character projected is formed within its own individual lenticular element, character changes are sharply defined and, in effect, instantaneous. Industrial Electronic Engineers, Van Nuys, Cal.

Circle No. 252 on Inquiry Card

HEAT DISSIPATORS

A new series of heat dissipators and retaining devices for plastic-cased transistors offers models to cool, position, and prevent lead-pull, even in high shock and vibration applications. Each of the three designs of the series, designated "Fan-Top," "Clip-Type," and "Spade-Type," offers specific benefits for particular applications. The Fan-Top unit, which comes in three sizes suitable for plastic transistor case styles, is a universal dissipator of the familiar type used for metal-cased transistors. Because of its configuration, the Fan-Top can be used in high-density packaging with practically no loss in circuit-board area or vertical clearance space. Generally allowing a 33% increase in transistor operating power without an increase in case temperature, the Fan-Top will also reduce case temperature at fixed power levels. The Clip-Type dissipator acts as a retainer and reduces high shock and vibration loads that develop on the transistor leads in certain applications. In addition to incorporating heat dissipator and retainer functions, the Spade-Type Series properly positions plastic transistors when automatic soldering techniques are used. Here, the "standoff" legs of the dissipator form a 0.1 inch grid into which the transistor may be deposited for attachment onto a circuit board. Thus retained above the circuit board, the transistor is positioned at a height sufficient to eliminate any thermal damage during soldering of connections. International Electronic Research Corp., Burbank, Cal.

Circle No. 246 on Inquiry Card



ENCODER ELECTRONICS

A universal electronics module enables a single shaft encoder to be used for digital display, data logging, computer input, and set-point control. The new modular system is housed in a standard 19 in. chassis. Printed circuit boards, representing such functions as logic, code conversion, memory, and power amplification, are simply inserted into the chassis. The shaft encoder determines range and resolution only, while the electronics module may be varied for a choice of code format, voltage, current, and polarity. In addition to its versatility, the module permits exact interfacing between a shaft encoder and computer, printer, or card punch. Furthermore, load characteristics will in no way affect encoder life since the electronics module acts as a buffer stage. Theta Instrument Corp., Saddle Brook, N J.

Circle No. 256 on Inquiry Card

THUMBWHEEL SWITCHES

New line of thumbwheel switches was designed for use in any single-pole, double-pole or 4-pole switch application. They are available in decimal form or as coding and decoding types, which accept either a binary or decimal input. The units feature a built-in decoding diode gate in the rotor, thus saving the user the trouble of having to mount tiny diodes and running extra equipment leads. They are available with solder or wire-wrap terminals to meet the individual installation requirement. In addition, the switches incorporate the use of four independent wipers which provide a wide variety of decoding possibilities. Modularly styled, each switch is manually-operated by a tab on the thumbwheel. A series of switches, mounted within a panel, are available in various lengths to accommodate from 1 to 9 switches in cascade on ½-inch centers. Amperex Electronic Corp., Hicksville, N. Y.

Circle No. 229 on Inquiry Card

MILITARY CORE STACK

A rugged, militarized core memory stack is said to have bypassed inherent reliability problems of previous memory stacks. The new stack provides greater system tolerances, higher resistance to shock, vibration and temperature extremes, and built-in temperature dissipation. It stores the same amount of information in only ⅔ of the space used by an ordinary memory stack. Trademarked Semstak (Severe Environment Memory Stack), it was constructed using etched finger contacts allowing planes to be interconnected with one-half the number of solder joints usually required. The design also employs compression to actually increase solder joint reliability. The Semstak construction eliminates buss wire connections which have been a common source of stack failures. A typical 4,096-word by 24-bit Semstak, with 30 mil cores, measures 3 x 3 x 2 inches, and weighs 18 ounces with mounting hardware. The stack is available in sizes up to 16,384 words of any bit length. Electronic Memories, Hawthorne, Cal.

Circle No. 249 on Inquiry Card

NEW PRODUCTS

NEW COMPUTER MODELS

Two new versions of their DATA/620 computer series was announced by Data Machines. The first of these, designated 620A, features 16-bit memories and is priced at $30,900. The second, the 622A, features 18-bit memories and is priced at $32,100. Both are said to be highly-productionized versions of the 620 series, and incorporates many optional features as standard. Some of these are hardware multiply and divide, extended addressing, 8192-words of 16 or 18 bit memories, ASR-33 Teletype, and complete front access cabinets. According to the company, the production economies gained through standardization of the 620A and 622A resulted in price reductions of 25 to 35%. Data Machines, Inc., Newport Beach, Cal.

Circle No. 272 on Inquiry Card

PROGRAMMABLE PULSE GENERATOR

A multiple pulse generator operates at stepping rates from 10mc to 1kc and has 12 parallel output channels. Eight time steps make a single pass through the program which is repeatable a given number of times under a variable delay control prior to re-initiation. Another feature is step and pair repeat capability. The cycle may be started again with an external control pulse or a built-in, slow (1 mc to 10 cps) cycle initiate clock. Programmed by the insertion of diode pins into a program matrix board, the unit may be applied as a clock and control for a memory tester or any system which requires sequencing. It may be used to test for hazards in logic networks or to study the effects of irregular duty cycles. Adar Associates, Inc., Somerville, Mass.

Circle No. 235 on Inquiry Card

COMPUTER AIR CONDITIONING

A new 15-ton model of a factory-packaged controlled-atmosphere system for computer and data processing rooms is available as an air-cooled, water-cooled, or chilled water unit. Features include simplified design for low-cost installation and easy maintenance; solid-state electronic controls; dual refrigeration systems; dual air filtering; and infra-red dust-free humidification. A raised floor is used as the supply air plenum. Liebert Corp., Columbus, Ohio.

Circle No. 214 on Inquiry Card

INTERFACE SYSTEM

A new analog-to-digital interface system consists of control logic, interface electronics, and two 32-channel 50 kc A-D multiplexers and converters. The system receives instructions from the computer specifying when to convert, on which channel, and how many high-speed conversions to make. After each conversion, the data is stored in a buffer register and an input data request is sent to the computer. Upon acceptance, the computer sends an input acknowledge signal to the interface system. Datametrics Corp., No. Hollywood, Cal.

Circle No. 253 on Inquiry Card

CHIP CAPACITOR

The high degree of stability of a new miniaturized capacitor is said to be due to its construction and materials designed to be impervious to environmental conditions. The advantages of the chip unit include high capacitance-to-volume ratio, superior packaging flexibility, and mounting versatility — particularly for outboard mounting on integrated, thick-and-thin film circuitry. Dimensions with tinned terminals range from 0.070 x 0.065 x 0.070 with capacitance range of 4.7 pf to 82 pf, and 0.280 x 0.195 x 0.070 for 100 pf to 1000 pf. Voltage rating is 200 vdc. Nytronics, Incorporated, Berkeley Heights, N. J.

Circle No. 274 on Inquiry Card

CURVE TRACER

High-speed digitizer was designed specifically for reducing analog graphic data to digital form for computer processing and analysis. While the operator manually traces the curve, X and/or Y true plus and minus coordinate values are automatically recorded at operator-selected increments on to magnetic tape, punched paper tape, or punched cards. The data is formatted by way of an operator wired patch panel for direct computer entry. Resolution is 0.001″; accuracy is ±0.002″. Auto-Trol Corp., Arvada, Colo.

Circle No. 209 on Inquiry Card

EPOXY-MOLDED TRANSISTORS

New 10, low-cost, npn and pnp general-purpose transistors with unit prices in the order of 25¢ are said to have all the inherent performance and stability characteristics of silicon devices. The 10-unit line includes npn and pnp low-level/high-gain units, uhf transistors, and diffused epitaxial types for a variety of uses in data processing, communications, and other electronic equipment. Due to their unique construction, these units permit access to the transistor connections from the top of the printed circuit board for testing and trouble shooting. National Semiconductor Corp., Danbury, Conn.

Circle No. 220 on Inquiry Card

SOLID-STATE PROGRAMMER

A new series of solid-state industrial programmers permits quick program change without special tools. The basic model has 20 steps and controls up to 10 channels. Output is relay contact closure, or optional SRC or amplifier output. For industrial applications, stepping rate is less than one step per day to over 10,000 steps per minute. For laboratory wave pattern applications, step rate can exceed one million steps per minute. Step rate is controlled by an external generator or by an optional internal oscillator. United Computer Co., Tempe, Ariz.

Circle No. 257 on Inquiry Card

NEW PRODUCTS

PULSE TRANSFORMERS

A new line of micro-size pulse transformers was designed for printed circuit board applications. Sizes range from 0.200″ dia. x 0.200″ ht. to 0.500″ dia. x 0.500″ ht. featuring a capability for high density packaging. Dumet or nickel terminals are provided. Rise and fall times are less than 20 nanoseconds and pulse widths range to 20 microseconds. Fugle-Miller Laboratories, Inc., Clark, N.J.

Circle No. 222 on Inquiry Card

DIGITAL PROGRAMMER

New solid-state digital programmer features variable time base provisions for digital control of event turn ON and turn OFF. The Model 10315 has output switches capable of handling 10 amperes at 28vdc inductive. Individual channel select switches verify any program mode. The unit has been designed for automatic re-cycling, resetting, and stopping. The programmer indicates when it is in an armed condition and is capable of being placed in a "hold" at any point during its program. Artisan Electronics Corp., Parsippany, N. J.

Circle No. 258 on Inquiry Card

RUGGED TAPE RECORDER

New digital magnetic tape system was designed for geophysical, mobile, and shipboard field recording applications. The new system, identified as Model FT-152 and packaged to withstand adverse environmental conditions encountered in field seismic exploration operations, operates directly from a 12-volt battery with extremely conservative power consumption. The basic FT-152 is equipped with ten ½″ reels. The standard transport provides 3 selectable tape speeds with any combination from 15 ips to 120 ips. It is fully IBM-compatible for 7- and 9-channel (IBM 360, ASCII) tape formats. The FT-152 features versatile operation, modular construction, front access to all components for ease of maintenance, and minimum depth behind the front panel for mounting in confined areas. An added feature, a ¼″ clearance at the rear and around the periphery of the main transport panel is provided for mounting the transport in a carrying case. Low tape sensor and loop control arms are simultaneously retracted by the tape load handle for convenient reel loading and tape threading. Interlocks on the tension arms automatically turn the transport off to prevent tape damage. Potter Instrument Co., Inc., Plainview, L.I., N.Y.

Circle No. 221 on Inquiry Card

GRAPHIC DATA SYSTEM

A high-speed system of converting computer data into readable form consists of an entire family of compatible equipment that operates at computer speeds to record output in alphanumeric or in graphic form, coupled with necessary ancillary equipment to provide effective use of the recorded output. Key elements in the family of equipment are four new recorders. Each recorder, a system-within-a-system, takes digital codes from a computer or magnetic tape and translates the codes into ordinary language or graphic form at tape speeds. The information is presented on a special cathode ray tube where cameras automatically record it. Data may be recorded on special computerized microfilm for 16 mm roll cartridges or 35 mm aperture cards. An optional microfiche camera will be available in the system to produce titled microfiche records automatically with 72 images on a tab card size, or in other sizes and formats. Stromberg-Carlson, San Diego, Cal.

Circle No. 226 on Inquiry Card

HYBRID CIRCUIT

A new circuit module offers a general-purpose, high-speed sample and hold operation. The module features an accuracy of $\pm 0.01\%$ for a gain of 1, full scale input of ± 10 V ± 10 ma, and input impedance greater than 10 megohms at 1 kc. The unit can be used for high-speed application, since it settles to 0.01% in 5 microseconds and has an aperture time of less than 50 nanoseconds. The use of field-effect transistors and unique circuitry has enabled typical decay rates of less than 0.01% to be achieved in 10 ms. Redcor Corp., Canoga Park, Cal.

Circle No. 233 on Inquiry Card

AIR MODULES

A new line of environmental air modules is said to offer a standard system specifically designed to meet the higher performance requirements set by all leading manufacturers of computer equipment. The environmental air module is a self-contained unit which can be totally serviced from the front. The cabinetry design provides safe and easy accessibility to the control section and the coil section even while the unit is in operating cycle. This feature also makes it possible for the module to be located flush to the rear and/or side wall. The modules include all of the components necessary to achieve varying degrees of cooling, heating, humidifying, dehumidifying, filtering, and circulating of environmental air as required for the proper operation of all types of computers and related equipment. A remote control panel is furnished to provide automatic control for the system. The Glenmart Co., Inc., Los Angeles, Cal.

Circle No. 224 on Inquiry Card

COUNTER/TIMER

New model in a series of electronic counter/timers provides direct counting to more than 100 MHz. With an eight-digit readout it has six modes of operations: manual, frequency, frequency ration, period, time interval, and time interval A-B. Frequency range is 0-100 MHz. It measures average periods of 0.1 microsecond to 10 seconds and measures single periods of 1.0 microsecond to 10^8 seconds. Monsanto Electronic Instruments, West Caldwell, N.J.

Circle No. 273 on Inquiry Card

FLATPACK CONNECTOR

A flatpack stick connector series is suitable for motherboard-connection of up to 18 flatpacks. The new series, designated FPS, meets MIL-E-5400 and MIL-E-16400, and incorporates connector bodies molded from high-quality, glass-filled phenolic which conforms to MIL-M-14 type MFH. Plug contacts are made from ½-hard beryllium copper and are plated with 50 microinches of gold over a copper strike. Receptacle contacts, similarly plated, are formed from heat-treated beryllium copper. Receptacle contacts, which are removable, may be attached to the motherboard by either soldering or welding. A staggered contact pattern allows freedom for the designer when routing interconnecting circuitry within the motherboard laminates. The larger assembly in the series measures 5¼-inches in length, 0.550-inches in width, and ½-inch high; the smaller assembly, having the same cross section, is 3½-inches long. Hughes Connecting Devices, Newport Beach, Cal.

Circle No. 216 on Inquiry Card

PROCESS CONTROL COMPUTER

A new process control computer, designated the ITI 4901 computing simulator, is aimed at the market for the environmental testing of supersonic airplanes and space crafts. It also finds equal applications in chemical and steel plants for the monitoring and controlling of closed loop processes. The new system features a 4096-word core memory, with a cycle time of 1.75 usec. Monolithic integrated circuits are used exclusively for the unit. A Model 33 Teletype set complete with keyboard printer and paper tape reader-punch is the standard peripheral equipment. The system, incorporating a proprietary programming technique, can be operated and programmed by semi-skilled personnel. This feature, augmented by the ability to provide precisely-synchronized real-time channels, is said to offer substantial advantage over a general-purpose digital computer. The basic ITI 4901 computing simulator is offered at a price of $29,950. Information Technology Inc., Sunnyvale, Cal.

Circle No. 262 on Inquiry Card

NEW PRODUCTS

READER/SPOOLER

Photocell punched tape reader/spooler features a 500 character-per-second reader and a 50 inch-per-second spooler equipped with 10½ inch diameter reels. The unit is mounted on a 21 inch high panel, requiring minimum rack space. The electronics portion is in a common chassis. The unit is available in both unidirectional and bidirectional configurations and can be used for tape loop operation, if required. Remex Electronics, Hawthorne, Cal.

Circle No. 271 on Inquiry Card

DRUM MEMORY SYSTEM

Universal, packaged design of a drum memory system is said to give it plug-in adaptability to virtually every type, size, and make of high-speed digital computers. The Model 1116 System offers a total capacity exceeding 12,500,000 bits, and adaptability of 16-, 18-, and 24-bit word systems, an average access of 8.3 msec, a read/write capability of one to sixteen 64-word blocks with two IOT commands, and a memory bit cost of 0.35 cents. The complete system is mounted in a standard VRC cabinet with an external indicator light panel showing state of the drum and internal logic. A power supply and distribution within the drum system produce and control all operating voltages. One source of external ac power is required, and it may be controlled locally or remotely. Vermont Research Corp., No. Springfield, Vt.

Circle No. 228 on Inquiry Card

ENCODER SYSTEM

Any motor-controlled positioning system may be automated to respond to digital commands with a new encoder/control system. By coupling the new encoder to the system which is to be controlled, the resulting digital data is sufficient to exercise complete control over the starting and stopping of the motor. The encoder electronic package compares encoder output to set-point command and actuates output relays which are used to control the motor by starting, stopping, reversing, slowing, or braking the motor. The remote control system accepts manually-inserted position commands or digital set-points from a computer. Specifications include a resolution to 1 part per million and a max speed at encoder shaft of 1000 rpm. Theta Instrument Corp., Saddle Brook, N.J.

Circle No. 215 on Inquiry Card

CRYSTAL CAN RELAYS

New universal contacts, said to provide dry circuit to 1 amp operation with the same contact set, have been incorporated in DPDT crystal can relays. This development permits the specification of a single subminiature relay model to meet a variety of low profile, circuit-board applications. The Model BR10 measures 0.405″ x 0.230″ x 0.500″, and weighs 0.15 oz. It has a guaranteed life to 150,000 operations, minimum. Sensitivity is stated at 80 milliwatts; vibration performance, 30 g, 40-3000 cps; and operating temperature range, −65C to +125C. Babcock Relays, Costa Mesa, Cal.

Circle No. 261 on Inquiry Card

TAPE PREPARATION

A tape preparation system was designed for manually recording data on standard, one-inch wide tapes using conventional, 1/10-inch hole spacing. The system is said to be ideal for revising or editing tapes for numerically-controlled systems without resorting to expensive computer techniques. Standard features include eight, independently-operated "channel selector" pushbuttons to allow the operator to set up any hole pattern with a maximum of eight holes per line. Each of the buttons glows when depressed to allow the operator to verify the pattern before actually punching the selected holes. If an error is noted, the operator may push the "cancel" button and then repeat the set up. After the hole pattern is verified as correct, the operator pushes the "punch" button to initiate the punching cycle. When the punching is complete, the tape automatically advances, the "channel selector" pushbuttons return to their unoperated position, and a "lines punched" counter advances one count. Time-Trol, Inc., Van Nuys, Cal.

Circle No. 259 on Inquiry Card

MULTI-POLE RELAY

New 5-amp telephone type, multi-pole relay has a switching capacity ranging from 4-pole through 8-pole, while operating power remains at 1.2 to 1.5 watts. High, tight-tolerance contact pressures (30 gram minimum NC, 35 gram NO) combine with simple contact members to give maximum contact resistance of 15 milliohm, eliminating the possibility of jarring open in operation and very low contact capacity ideal for RF applications. The new relay offers multimillion mechanical operation life expectance, 500,000 electrical operation (2 amps, 30 vdc, or 120 vac) life, and features a novel 2-element contact circuit design that eliminates internal wiring, solder connections, and pigtails. American Monarch Div., Minneapolis Scientific Controls Corp., Minneapolis, Minn.

Circle No. 268 on Inquiry Card

LITERATURE

Precision Switches

A 28-page catalog is said to offer all the information a buyer needs to know about 19 different series of precision switches. Detailed illustrations of the switches are accompanied by information on special features, button and terminal variations, and operating characteristics. Among the switches shown and described are general-purpose, single and double pole, miniature, subminiature, low torque, open type cam follower, coin, stack type, one way action, and alternate action type. Switches are categorized according to such characteristics as size, electrical capacity, operating force, and mounting configuration. To facilitate use of the catalog, one page is devoted to a glossary of technical terms. Cherry Electrical Products Corp., Highland Park, Ill.

Circle No. 302 on Inquiry Card

Selecting Terminals/Splices

According to a new brochure, crimp terminals must not be selected by the "fit" of wire or wires in the terminal barrel but by the total circular mil area in cross-section of the wires used. The brochure contains newly-revised and updated series of tables to assist in the calculation of circular mil area. Included is a nomograph for simultaneously determining terminal size and circular mil area for rectangular wire. Instructions are provided for deforming flat bus wire to permit its use in circular or oval terminals. Formulae (with examples) are presented for computing circular mil area of various and combined wire shapes. A set of tables lists the circular mil area for over 200 solid, and stranded, wire types from AWG #26 to 1,000 MCM. Recommended hole sizes for use with 22 commonly-used studs are also included. Amp, Inc., Harrisburg, Pa.

Circle No. 316 on Inquiry Card

Data Analysis

Brochure describes a high-speed analog/digital data acquisition and analysis service which can handle large volumes of laboratory test data from analog magnetic tape recordings or from digital magnetic tape recordings or directly on-line with the test. According to the brochure, analog data recorded on one-inch 14-channel magnetic tape can be played back, in either the FM or direct mode, directly on-line to data conversion system for digital processing. Wyle Laboratories Testing Division, El Segundo, Cal.

Circle No. 310 on Inquiry Card

Terminal Junctions

A new 4-page brochure describes a new class of point-to-point interconnection and busing devices. These modular devices are for the interconnection of wires from size AWG 24 through AWG 4. The brochure describes the application and basic structure of the products plus typical busing and interconnection configurations. The Deutsch Co., Banning, Cal.

Circle No. 315 on Inquiry Card

Plastic Semiconductors

Claimed to be the semiconductor industry's broadest line, plastic-encapsulated economy devices are described in a 12-page booklet. The data covers product characteristics, application advantages, and typical uses for commercial, military, and industrial purposes. Among the low-cost semiconductors described are silicon and germanium bipolar and field-effect transistors, unijunction and power transistors, silicon rectifiers, and monolithic integrated circuits. The booklet also provides information on a 50-million transistor-hour reliability test-program now being conducted. Texas Instruments Inc., Dallas, Tex.

Circle No. 307 on Inquiry Card

Pulse Glossary

A booklet, called "The New Pulse," includes 45 basic pulse definitions, most of which are illustrated. It is believed that these definitions not only approximate what most time domain practitioners think these words mean, but at the same time, they will be found to be unambiguous, rigorous, and mathematically defensible. E-H Research Labs, Oakland, Cal.

Circle No. 322 on Inquiry Card

Fiber Optic Magnifier

Fiber optic magnifiers that magnify or reduce information through light transmission pathways considerably shorter than conventional lens systems are described in a data sheet. Made of attenuated fused glass fiber bundles, the device magnifies information at its large surface or reduces information at its small surface. According to the literature, magnifiers are ideal for film enlargers, photoelectric systems, and other display systems that require minimum optical degradation and excellent image display. Listed are current magnifier parameters, device configurations, optical characteristics, and fiber optic terminology. Communication Prods. Dept., Corning Glass Works, Corning, N.Y.

Circle No. 308 on Inquiry Card

Semiconductor Cooling

Two new catalogs on semiconductor cooling cover natural convection heat sinks, circuit board heat sinks, thermal retainers, mounting insulators, thermally conductive adhesives, thermal joint compounds, open airflow cooling assemblies, closed airflow cooling packages, liquid cooled plates, heat sink extrusions, and special assemblies. The first catalog describes heat sinks for milliwatt to high-power semiconductors. The second covers standard commercial and military forced convection assemblies, both open and closed airflow, plus a new line of liquid cooled plates, and extrusions. Thirty-five specially engineered cooling packages are illustrated. Wakefield Engineering, Inc., Wakefield, Mass.

Circle No. 301 on Inquiry Card

LITERATURE

Long-Life Lamps

Included in a 12-page catalog are sections on lamp terminology and design facts, selection of miniature lamps, automotive lamps, miniature indicator and panel lamps, microminiature lamps, and sub-miniature lamps. Tables provide quick reference information on types and styles, including base design, design voltage, approx. candlepower, hours of life, and dimensional data. Of particular interest are the small size microminiature lamps used for circuit components, computers, control panels, etc. Lengths are as short as 0.187″ and diameters as small as 0.094″. Most have approximate lives of 100,000 plus hours. Both based and unbased types are described, including new axial lead types. Hudson Lamp Co., Kearny, N. J.

Circle No. 303 on Inquiry Card

IC Logic Cards

A 20-page technical catalog describes dual in-line integrated circuit logic cards and related equipment. Price reductions from 32 to 40% for 16 integrated circuit modules are noted in the catalog. Physical characteristics, operating specifications, and data sheets information are included. Engineered Electr., Santa Ana, Cal.

Circle No. 312 on Inquiry Card

Microminiature Connectors

New 8-page catalog covers a line of microminiature plug and socket connectors. Full technical information, including outline drawings, electrical and mechanical specifications, illustrations, and ordering information are included. These connectors meet MIL-C-8384 specs and are available with a variety of contacts from 5 to 104. Hoods, polarizing screwlocks, and cable brackets are optional accessories. Continental Connector Corp., Woodside, N.Y.

Circle No. 324 on Inquiry Card

Oscilloscope Catalog

A 6-page brochure describes two broad classes of oscilloscopes — plug-in amplifier types and built-in amplifier types. Dual and single beam oscilloscopes are also covered as well as a unique rack-mounted main frame with plug-in amplifiers. The catalog contains an introduction which discusses the design, production, and specification philosophy which is said to make possible a low-cost oscilloscope with extremely high performance and reliability. To facilitate comparison of instruments, complete specifications and prices of all the oscilloscopes and amplifiers are presented in a single chart. Data Instruments Div., Pennsauken, N.J.

Circle No. 306 on Inquiry Card

Control Modules

Performance-proved control module boards for use in digital control systems are described in a new 4-page folder. The modules are comprised of NPE relays mounted on printed circuit boards. The NPE units are produced with either miniature or standard-size switch contacts for maximum design compatibility of space and load handling requirements. Descriptions of the functions performed by the modules — decimal counting, binary counting, logic, and selection — are included. Wabash Magnetics, Incorporated, Wabash, Ind.

Circle No. 319 on Inquiry Card

Telemetry Primer

"INTRODUCTION TO TELEMETRY" a comprehensive technical report, includes definitions of technical terms, history and applications, telemetry techniques, and equipment requirements. Telemetry techniques covered include FM/FM, PAM, PDM, and PCM. Equipment requirements are discussed for signal conditioners, sub-carrier oscillators, transmitters, RF amplifiers, antennas, preamplifiers, multicouplers, receivers, discriminators, data display, magnetic tape recording, and data processing. International Electronic Research Corp., Burbank, Cal.

Circle No. 300 on Inquiry Card

IC Hardware

New mounting package that makes possible solderless, pressure contact mounting of microcircuit flat-packs on pc cards is described in a 4-page brochure. The new packaging system consists of 3 pieces: a base in which the flat-pack is set with no fastening necessary; a positive lock, snap-on top which holds the flat-pack securely in place, yet leaves it visible for circuit identification, and a mounting stud which becomes part of the base. The mounting stud extends through the printed circuit board with a nut applied on the opposite side. Because the stud and nut are made of nickel-plated brass, heat conduction characteristics provide an effective heat sink. The brochure also outlines a complete series of components for mounting microcircuit cards in multi-card files. The system features low-silhouette card guides with either in-line or offset connectors. Complete dimensional drawings, specifications, and ordering data are provided. Scanbe Mfg. Corp., Monterey Park, Cal.

Circle No. 328 on Inquiry Card

Magnetic Tape Equipment

Described in a 28-page catalog are analog and digital magnetic tape recorder/reproducers, line recording oscillographs, thermal writing recorders, and signal conditioning equipment. Also, supplies such as oscillograph recording papers, developing chemicals, and magnetic instrumentation recording tape. CEC, Pasadena, Cal.

Circle No. 327 on Inquiry Card

Digital Modules

A 40-page catalog describes a complete proprietary line of digital plug-in modules. The catalog contains circuit diagrams of the modules and detailed engineering data to aid the design engineer. The family of modules is designed around three basic circuits, the NAND gate, the flip-flop, and the power amplifier, and is available in three speeds, 200 kc, 2 mc, and 8 mc. Decision Control, Inc., Newport Beach, Cal.

Circle No. 323 on Inquiry Card

SALES OFFICES

BOSTON

Lindsay H. Caldwell
Professional Bldg.
Baker Ave.
W. Concord, Mass.
phone: (617) 369-6660

NEW YORK

Robert J. Bandini
18 East 41st St.
Room 1501
New York, N.Y. 10017
phone: (212) 685-5854

CHICAGO

Brent Salmon
410 N. Michigan Avenue
Chicago 11, Illinois
phone: (312) 467-6240

DETROIT

James Stem
424 Book Bldg.
Detroit 26, Michigan
phone: (313) WO 1-0278

LOS ANGELES

David Barton
672 So. Lafayette Park Pl.
Los Angeles 57, California
phone: (213) 382-1121

SAN FRANCISCO

David Barton
672 So. Lafayette Park Pl.
Los Angeles 57, California
phone: (213) 382-1121

ADVERTISERS' INDEX